Ultra-Low Power Radio Transceiver for Wireless Sensor Networks

by

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Abstract

The objective of this thesis is to present the design and implementation of ultra-low power radio transceivers at microwave frequencies, which are applicable to wireless sensor network (WSN) and, in particular, to the requirement of the Speckled Computing Consortium (or SpeckNet). This was achieved through quasi-MMIC prototypes and monolithic microwave integrated circuit (MMIC) with dc power consumption of less than 1mW and radio communication ranges operating at least one metre.

A wireless sensor network is made up of widely distributed autonomous devices incorporating sensors to cooperatively monitor physical environments. There are different kinds of sensor network applications in which sensors perform a wide range of activities. Among these, a certain set of applications require that sensor nodes collect information about the physical environment. Each sensor node operates autonomously without a central node of control. However, there are many implementation challenges associated with sensor nodes. These nodes must consume extremely low power and must communicate with their neighbours at bit-rates in the order of hundreds of kilobits per second and potentially need to operate at high volumetric densities. Since the power constraint is the most challenging requirement, the radio transceiver must consume ultra-low power in order to prolong the limited battery capacity of a node. The radio transceiver must also be compact, less than 5×5 mm^2, to achieve a target size for sensor node and operate over a range of at least one metre to allow communication between widely deployed nodes.

Different transceiver topologies are discussed to choose the radio transceiver architecture with specifications that are required in this project. The conventional heterodyne and homodyne topologies are discussed to be unsuitable methods to achieve low power transceiver due to power hungry circuits and their high complexity. The super-regenerative transceiver is also discussed to be unsuitable method because it has a drawback of inherent frequency instability and its characteristics strongly depend on the performance of the super-regenerative oscillator. Instead, a more efficient method of modulation and demodulation such as on-off keying (OOK) is presented. Furthermore, design considerations are shown which can be used to achieve relatively large output voltages for small input powers using an OOK modulation system. This is important because transceiver does not require the use of additional circuits to increase gain or sensitivity and consequently it achieves lower power consumption in a sensor node.

This thesis details the circuit design with both a commercial and in-house device technology with ultra-low dc power consumption while retaining adequate RF performance.

It details the design of radio building blocks including amplifiers, oscillators, switches and detectors. Furthermore, the circuit integration is presented to achieve a compact transceiver and different circuit topologies to minimize dc power consumption are described. To achieve the sensitivity requirements of receiver, a detector design method with large output voltage is presented. The receiver is measured to have output voltages of 1mVp-p for input powers of -60dBm over a 1 metre operating range while consuming as much as 420μW.

The first prototype combines all required blocks using an in-house GaAs MMIC process with commercial pseudomorphic high electron mobility transistor (PHEMT). The OOK radio transceiver successfully operates at the centre frequency of 10GHz for compact antenna and with ultra-low power consumption and shows an output power of -10.4dBm for the transmitter, an output voltage of 1mVp-p at an operating range of 1 metre for the receiver and a total power consumption of 840μW. Based on this prototype, an MMIC radio transceiver at the 24GHz band is also designed to further improve the performance and reduce the physical size with an advanced 50nm gate-length GaAs metamorphic high electron mobility transistor (MHEMT) device technology.

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This thesis is dedicated to the memory of my father-in-law.

Chapter 1

Introduction

Wireless sensor network (WSN) creates an innovation in the way we interact with our environments. The vision of wireless sensor network (WSN) is ubiquitous wireless, with large networks of wirelessly connected nodes collecting and disseminating a wide variety of environmental data such as temperature, pressure and motion capture. Technology advances in device, energy scavenging, energy storage and IC packaging, coupled with the availability of low power, low cost digital and analogue/RF integrated circuits have made it conceivable to build and deploy dense wireless networks of heterogeneous nodes [1].

The SpeckNet project [2] is a consortium between University of Glasgow, University of Edinburgh, University of Strathclyde, University of St Andrews and Napier University, to comprehensively address the challenges in implementing WSN on a large scale, from high-level routing to physical layer electronics. The goal of the project is ubiquitous wireless that disappears into the environment with constant connectivity and without regular maintenance. Crucial to the success of these ubiquitous networks is the availability of small, lightweight, low-cost network elements, which are called wireless sensor nodes. More importantly, the nodes must be ultra-low power to eliminate frequent battery replacement. To reach these aggressive power consumption levels, the effective range of each node must be limited to a couple of meters at most. Extending the reachable data range requires a scalable network infrastructure that allows a distant node to communicate with any other node. A self-configuring ad-hoc networking approach is a key to the deployment of such a network with many hundreds of nodes.

Figure 1.1 shows the deployment, communication range and link between each node for an energy-efficient wireless network. Each node operates as a relay point to implement a multi-hop communication link by receiving data from one of its neighbours, and then processing it before routing it to the next neighbour towards the destination for energy-efficient wireless network as well as network without base station unlike long range communications. In the next section, challenges of wireless sensor networks will be discussed.

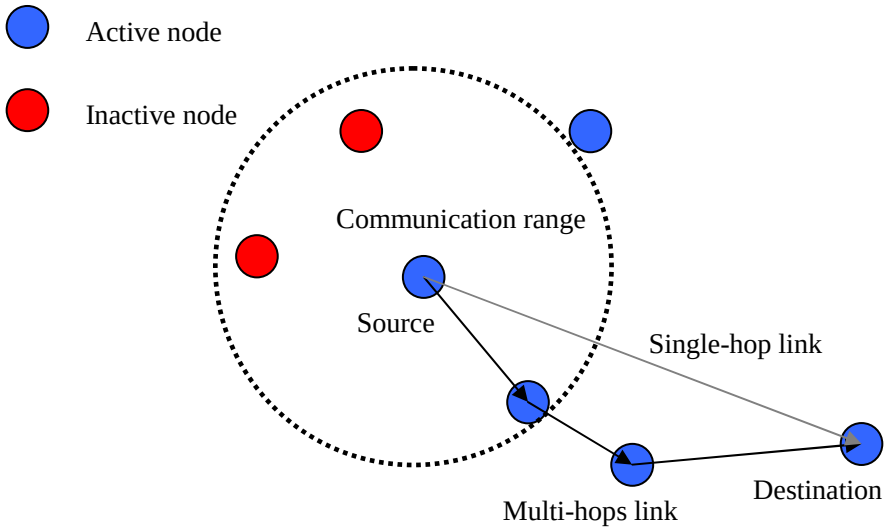


Figure 1. 1. Scenarios of node deployment for energy-efficient wireless network

1.1 Challenges of Wireless Sensor Networks

In order to make successful a large scale deployment of wireless sensor networks, each node must exhibit low power consumption, low operating and system cost and small size. Each of these three factors is somewhat intertwined. For example, electronic components are already so small that overall module size is limited by power supply or energy storage requirements. For this reason, reducing power consumption of the electronics is an effective way to shrink size as well. Another example is that highly integrated circuits with few external components can simultaneously reduce size and cost.

One of the most critical reasons to reduce power consumption is to enable the use of new power supply technologies like energy harvesting [3] and low cost printable batteries [4]. These early-stage developing technologies cannot supply much power, so any means of reducing power requirements will hasten the adoption of next generation power supplies.

Clearly, reducing power consumption is a key method to reach the goal of ubiquitous wireless. Among all the node functions such as computation, sensing, and actuation, the wireless communication link is still a dominant component [5]. Therefore, the high-level goal of this research is to reduce the energy dedicated to communication links in wireless sensor nodes.

1.2 Power Energy Sources

A large scale deployment of wireless sensor nodes can be achieved by the energy self-sufficiency of each node for their entire useful lifetime. Also, an energy efficient wireless network can extend the lifetime of each node. Even more importantly, wireless sensor nodes must reduce their consumed dc power and an efficient energy source must be developed for wireless sensor networks. The available power is determined by the power density and the size of the energy source. Hence, wireless sensor networks suffer from an available small power density due to small size. Several low cost energy sources for powering a sensor node are lithium battery, solar cell, fuel cell and other low cost batteries. Among all the energy sources, the lithium battery is the most versatile since its operation is relatively independent of its operating environment. However, its average power density is approximately 100μW/cm^3 with life time of 1 year [6]. For a small sensor node, the amount of storage the energy source has is not sufficient to operate the node for a long lifetime. Also, solar cells as scavenging energy sources perform well under strong sunlight and can be used to power sensor nodes placed near the windows and in the outdoors during the day. Hence, it is likely that sensor nodes will be powered by a combination of storage power sources. An example of such a hybrid power source is to use solar cells to charge the battery and power the node during the day, and employ the battery to operate the node at night. Combining both the storage and scavenging energy sources, the average power consumption of a 1cm^3 sensor node is ~100μW. This severe power requirement is the most challenging constraint and it greatly influences the design and implementation of wireless sensor nodes.

1.3 Transceiver Design Considerations

The radio transceiver is the most important system on a wireless sensor node since it is the primary energy consumer among all three of sensor, processor and radio transceiver. Modern low power, short range transceivers consume between 5mW and 300mW of power when transmitting and receiving [7]-[11]. A key hardware observation is that low power transceivers consume approximately the same amount of energy when in receive or transmit mode. This energy is consumed if the transceiver is powered on whether or not it is receiving actual data. The actual power emitted out of the antenna only accounts for a small fraction of the transceiver's energy consumption. A significant fraction goes to internal operation. Because of this, the overall cost of transceiver can easily be dominated

by the receiver power consumption. Therefore, the research in this thesis focuses on reducing the power consumption of the transceiver. In this section, the considerations of WSN transceiver design which affect power consumption are also described.

1.3.1 Transmission Range

The transmission range of a wireless sensor node is controlled by several factors. The most intuitive factor is that of radiated power for inter-node communication between two nodes. The more energy put into a signal, the farther it should travel. The relationship between power output and distance is shown in Equation 1.1,

$$P_{rad,\min} = \left(\frac{4\pi f}{c}\right)^2 \bullet \left(\frac{d^n}{G_t G_r}\right) \bullet R_{sens} \bullet LF \tag{1.1}$$

where f is the operating frequency, d is the distance between two nodes, G_r and G_t are the antenna gain of receiver's and transmitter's antennas respectively, R_{sens} is the receiver sensitivity, c is the speed of light, n is the path loss exponent and LF is the loss factor accounting for other losses (e.g. matching, cable loss, etc).

For WSN applications, an isotropic antenna (G_r and G_t =1) is desired as the relative orientation between sensors nodes are not predetermined. Also, multi-path is more severe in indoor environment and the path loss exponent n is typically between 3 and 4 [12]. For a range of about 1m, a 10GHz communication system requires about -10dBm of transmit power with a sensitivity of -60dBm.

Other factors in determining transmission range include the sensitivity of the receiver, the gain and efficiency of the antenna and the channel encoding mechanism. In general, wireless sensor network nodes cannot exploit high gain, directional antennas because they require special alignment and prevent ad-hoc network topologies. Omni-directional antennas are preferred in ad-hoc networks because they allow nodes to effectively communicate in all directions.

Hence, increased transmission range can be achieved by either increasing sensitivity or by increasing radiated power. When transmitting at 0dBm, a receiver sensitivity of -85dBm will result in an outdoor free space range of 25 to 50 metres, while a sensitivity of -110dBm will result in a range of 100 to 200 metres [12]. The use of a radio transceiver with a sensitivity of -110dBm instead of a radio transceiver with -85dBm allows one to decrease the radiation power by a factor of 30 and achieve the same range. However, a

good sensitivity of receiver leads to increase dc power consumption because an amplifier must be used to increase the receiver gain and a demodulator must also be used to increase receiver output voltage. Thus, the dc power consumption and sensitivity of receiver must be traded off in order to optimize the communication range.

1.3.2 Modulation Scheme

To reduce infrastructure costs and increase user capacity, traditional cellular and wireless local area network (WLAN) systems place a high value on both spectral efficiency and receiver sensitivity. Thus, transceivers employ bandwidth efficient modulation schemes like Gaussian minimum-shift keying (GMSK) or quadrature amplitude modulation (QAM) combined with coherent receiver architectures, however, these transceivers consume too much energy for sensor network applications. To address this problem, in 2003 the IEEE approved the 802.15.4 standard for low-power wireless personal area network (WPAN). The 802.15.4 supports both binary phase-shift keying (BPSK) and offset quadrature phase-shift keying (O-QPSK) modulation at a maximum data rate of 250 kbps [13]. Current 802.15.4 transceivers consume tens of milliwatts, which is less than cellular systems but still too high for many sensor network applications.

To achieve an improved power level lower than that specified by 802.15.4, on-off keying (OOK) modulation with non-coherent receiver architecture is a suitable modulation scheme. A non-coherent, OOK receiver enables the use of an envelope detection based receiver. In contrast with the coherent receiver architecture, no oscillator is required for phase synchronization and the receiver can turn on quickly. Furthermore, the power consumption can be dramatically decreased as little RF gain is required to achieve the short range communication and no RF oscillator must be sustained.

Two limitations of OOK modulation are that it is spectrally inefficient and that it is strongly susceptible to interferers. These two limitations, however, are acceptable given that low power consumption is the primary design consideration. For sensor nodes that are deployed in remote environments, there is ample bandwidth available and few interferers.

1.3.3 Data Rate

In typical deployment, data of interest such as temperature and pressure vary slowly with time, thus, to achieve sensor network for these applications, a data rate of only hundreds to thousands of bits per second is sufficient. In case of OOK transmitter, the

start-up time of RF oscillator directly limits the data rate of the transceiver. For low power consumption the oscillator start-up time is long, which seriously restricts the data rate of an OOK system. Therefore the traditional OOK transmitter is often used in low data rate applications of less than few Mbps. Methods have been proposed to increase the data rate with low power OOK system as the transceiver operates at a higher instantaneous data rate and turn off the radio periodically [14]. However, there is an upper limit above which increased duty cycling and higher instantaneous data rates decrease energy efficiency. One key problem is that the start-up time associated with turning on a transceiver has an associated energy that cannot be reduced by increasing data rates [15]. A second problem is that increased instantaneous power consumption results in worse battery efficiency or requires larger decoupling capacitors [16]. As alternative method for higher data rate that is required in high quality medical imaging system, a high data rate OOK transceiver is based on the mixer-based frequency up-conversion transmitter, but it is not suitable to realize low power consumption and compact size. Therefore, a transceiver architecture that meets the requirements of wireless sensor networks must be carefully chosen.

1.4 Thesis Organization

This chapter has introduced the concept of wireless sensor networks. There already exist some efforts to overcome the challenges in designing low cost, compact size and low power consumption transceivers. Therefore, the ultimate aim of this thesis describes device technology and design method to reduce the power consumption and size of radio transceiver and also implement a radio transceiver with these considerations.

Chapter 2 presents a survey of possible transceiver architectures for wireless sensor networks and highlights the factors limiting power consumption for other architectures. At the circuit implementation level, the consideration of device technology and operating frequency is discussed to satisfy the two requirements of ultra-low power consumption and compact transceiver.

Chapter 3 describes the design of the radio building circuits which constitute OOK radio transceivers, including all the necessary blocks to perform the radio transceiver function. Characteristic and design method of these building blocks with simulation analysis are presented to achieve complete radio transceiver. This chapter also illustrates the layout and performance of MMIC passive components such as metal-insulator-metal (MIM) SiN capacitor and spiral inductors that will be used in circuit design.

Chapter 4 details radio building blocks that are implemented on GaAs substrate and complete OOK radio transceivers which are integrated with them. An integrated quasi-MMIC transceiver is presented along with measured results. Chapter 4 also presents the reduction of power consumption in a complete radio transceiver with switched oscillator and envelope detector design method and then discusses the performance of a complete transceiver with ultra-low dc power consumption.

Chapter 5 details the device technology using an advanced III-V compound semiconductor process in University of Glasgow and the design and implementation of an MMIC OOK radio transceiver to achieve ultra-low power consumption and compactness. This chapter also illustrates the simulated results and layouts for switches, amplifiers, oscillators, and envelope detectors. Finally, the layout for a complete transceiver/antenna MMIC is presented.

Chapter 6 details the design and implementation of novel planar filters such as W- and G-Band bandpass filter (BPF) and wide band BPF. The experimental results are discussed and compared to simulations.

Chapter 7 concludes with a summary of the results achieved and a discussion of future research directions.

Chapter 2

Transceiver Design Approach

In the previous chapter, the concept of wireless sensor network (WSN) was introduced and the design considerations for transceivers in wireless sensor network applications were described. The Speckled Computing Consortium [2] focuses on the research and realization of a wireless ad-hoc sensor network comprising tiny nodes (specks). Each of these nodes will be autonomous, and capable of communicating via both optical and radio frequency (RF) links. Thousands of specks, scattered or sprayed on the person or surfaces, will collaborate as programmable computational networks called SpeckNet. The ultimate goal of SpeckNet is to achieve autonomous distributed wireless sensor networks that can perform data sensing, information processing and communicating into our daily environments. In this scenario, sensor nodes are deployed on a large scale and nodes automatically create sensing and processing networks with wireless connectivity. Wireless nodes must have modest resources due to their physical size and then their collective power is harnessed in a SpeckNet and significant processing capability will be realized.

Each speck is equipped with its own energy source within the stated volume and since this is severely restricted, battery dimensions must be kept to a minimum. At present, the smallest available rechargeable lithium battery will be suitable, but nevertheless a transceiver design exhibiting low power consumption is vital in order to provide a useful lifetime. Therefore minimising the power consumption of the overall design is a critical factor.

The radio transceiver is often the part of a sensor node which consumes the most power and since each node is equipped with only a limited amount of battery size and renewable energy source, the radio transceiver must be optimized to consume ultra-low dc power for energy efficient wireless networks. This thesis focuses on the circuit design method, modulation scheme and radio topologies operating at microwave frequencies which are suitable to achieve ultra-low power consumption and compactness for wireless sensor nodes.

The channel allocation is also a critical issue to realize the inter-node communication. The single channel sharing has been determined with channel estimation for short range wireless sensor network and collision avoidance algorithms by colleagues working at University of Edinburgh [17] and will be used in SpeckNet.

In summary, the SpeckNet radio transceiver must be designed to consume dc power of less than 1mW and fit within an area of less than 5×5 mm^2. The radio transceiver must also be able to operate over a distance of one metre to enable communication between each node.

2.1 Architecture Considerations

There are a wide variety of ways to build a wireless transceiver and modulate and demodulate an RF signal. On one hand are complex transceivers that can demodulate signals with very high sensitivity. On the other hand are simple transceivers such as RFID, which do not even have a power supply. We can view the wide variety of transceiver architectures on a continuum of power consumption and complexity versus performance, which tend to move together on the scale.

Traditional wireless transceivers basically are more complex architectures than RFID. These more complex transceivers utilize active devices to achieve high sensitivity and data throughput, far beyond what is possible with passive detectors. The high-level architectures used in these transceivers can generally be grouped into a few major categories. These architectures are referred to as traditional due to the fact the basic architectures used have not changed substantially in recent years, although the implementation details have become immensely more complex than in the early days of radio. This overview concentrates on narrowband transceivers.

2.1.1 Super-heterodyne Transceiver

The most common type of transceiver architecture utilizes frequency conversion, where the baseband signal is shifted to higher frequency to modulate data signal with carrier signal for modulating data signal and the input signal is shifted to lower frequency to ease implementation of signal processing blocks such as gain and filtering for demodulating data signal. Selectivity is achieved through careful frequency planning, combining narrowband low frequency responses with high purity oscillators and mixers to perform frequency conversion. For example, the super-heterodyne architecture utilizes two separate up/down-conversion operations. First, in the case of receiver, the input RF signal is amplified by low noise amplifier (LNA) in order to ease the noise requirements on the rest of the receiver chain. Then, the RF signal is converted to intermediate frequency (IF) with a high-accuracy, tuneable local oscillator (LO). This IF signal is amplified and filtered with

a fixed frequency filter to remove the image and spurious signals. A second mixer converts the signal to DC using a fixed frequency oscillator at the IF frequency. Figure 2.1 shows a typical block diagram for super-heterodyne transceiver. The advantage of this method is that most of the radio's signal path has to be sensitive to only a narrow range of frequencies which is selected by RF and IF filters. Hence, this transceiver has an advantage of a high sensitivity. RF filters are also used to isolate between transmitter and receiver. IF filters are used to remove an image response which is generated by frequency mixing. In some cases, multiple IF stages can be used to overcome the unwanted image response with two IFs of different values. The super-heterodyne method also offers excellent stability with a phase-locked loop (PLL) frequency synthesizer. Although super-heterodyne method has superior characteristics to simpler transceiver types in frequency, this method suffer from high power consumption by virtue of the use of power hungry components such as frequency synthesizer and mixers. Thus, in spite of their sensitivity and stability characteristics, this architecture is unsuitable to achieve a low power transceiver for SpeckNet project.

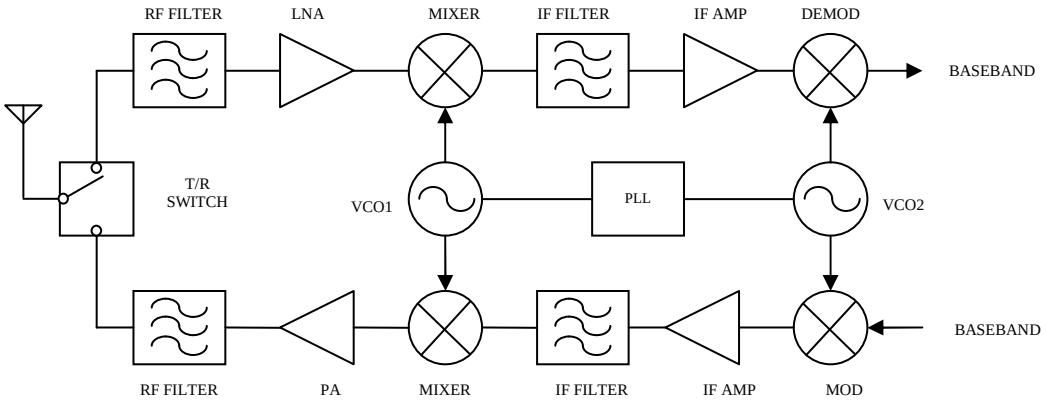


Figure 2. 1. Typical block diagram of super-heterodyne transceiver

2.1.2 Direct Conversion Transceiver

Figure 2.2 shows a typical block diagram of direct conversion transceiver. Direct conversion and low-IF transceivers avoid the image problem by quadrature mixing the baseband signal directly to RF signal and the RF signal directly to baseband using quadrature up/down-conversion. As in the case of super-heterodyne architecture, an LO with high spectral purity and stability is required to drive the mixers. The power consumption of these architectures, along with super-heterodyne, is fundamentally limited

by the local oscillator and PLL frequency synthesizer. The stringent frequency accuracy and phase noise performance typically requires a resonant LC oscillator, usually embedded in a phase locked loop (PLL). The limited quality factor (Q) of integrated passives leads to a power floor of a few hundred microwatts.

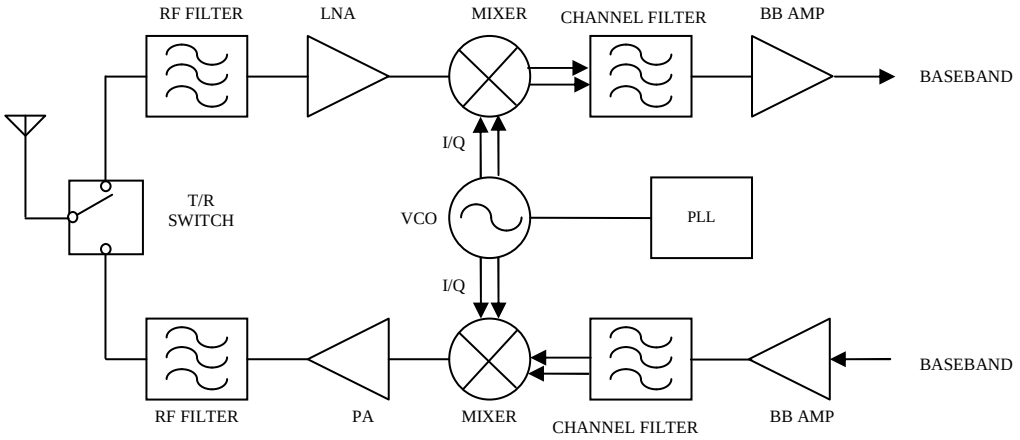


Figure 2. 2. Typical block diagram of direct conversion transceiver

As an example, consider the recent low-IF receiver implementation described in [18]. In order to save power, the design eliminates the typical LNA and feeds the RF input directly to the quadrature down-conversion mixers. The mixers are implemented as passive switching networks using MOSFET switches, so the mixing circuits consume zero DC current. Following the mixers, the receiver circuits process the baseband signal at the low IF frequency (less than 1MHz), so these amplifiers consume little power. The only remaining element is the oscillator to drive the LO port of the mixers. The oscillator must operate near the RF channel frequency with high accuracy and stability, while simultaneously driving the gates of the mixer switches with a large amplitude signal. For quadrature operation, the voltage controlled oscillator (VCO) must also provide both in-phase and quadrature outputs. It is not too surprising, therefore, that the LO generation is responsible for more than 80% of the overall power consumption in the receiver. Despite the use of a large modulation index to eliminate the need for a complete PLL, the VCO itself still consumes more than 300μW in single-phase, non-quadrature mode. This figure consequently increases the power budget for the entire transceiver. Clearly, the power devoted to the local oscillator must be dramatically reduced if this architecture is to be used for wireless sensor networks.

2.1.3 Super-regenerative Transceiver

The super-regenerative receiver (SRR) architecture can be used to realize a transceiver that is suitable for on-off keying (OOK) modulation. The advantages of the super-regenerative receiver are that it has high energy efficiency, low power consumption and small number of components allow for high integration. This makes it an attractive and preferred architecture for integrated ultra-low power radio transceivers. Figure 2.3 shows the typical block diagram of a super-regenerative transceiver, which consists of a matching network, an LNA with high isolation, a super-regenerative oscillator (SRO) which includes a time varying loop gain and a bandpass feedback network, and envelope detector for receiver and an optional power amplifier and an oscillator for transmitter [6]. The super-regenerative oscillator bias current is controlled by quench signal which has several times modulation bandwidth.

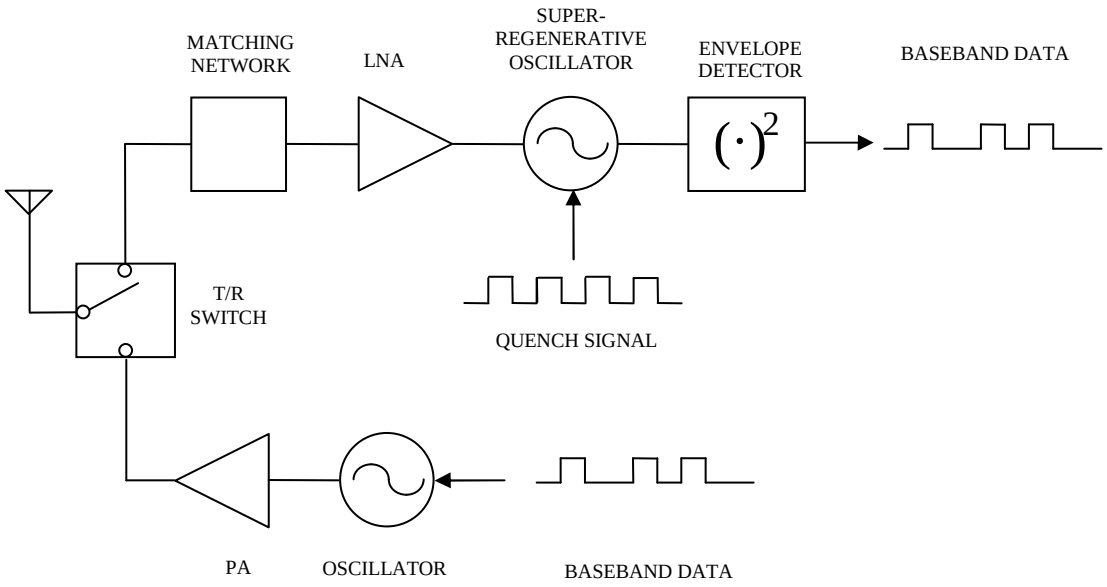


Figure 2. 3. Typical block diagram of super-regenerative transceiver

Although an SRR has advantages of high gain, simplicity, low cost, low power consumption and constant demodulated output over a wide range of input signal levels, however it has a drawback of inherent frequency instability and its characteristics strongly depends on the performance of the super-regenerative oscillator. Therefore the super-regenerative receiver requires a highly stable and low phase noise oscillator. In addition, interference is also caused by radiation from the quench oscillator and the addition of an oscillator in the receive path increases the overall power consumption of the transceiver.

2.1.4 Direct Modulation/Demodulation Transceiver

As an alternative to frequency conversion architectures, the simplest transceiver can be implemented with just one free-running oscillator, T/R switch, low noise amplifier (LNA) and envelope detector, similar to the early amplitude modulation (AM) transceiver. This architecture, also called direct modulation/demodulation transceiver, eliminates the power-hungry phase-locked LO altogether. Figure 2.4 shows a typical block diagram of direct modulation/demodulation transceiver with optional RF filter and power amplifier (PA).

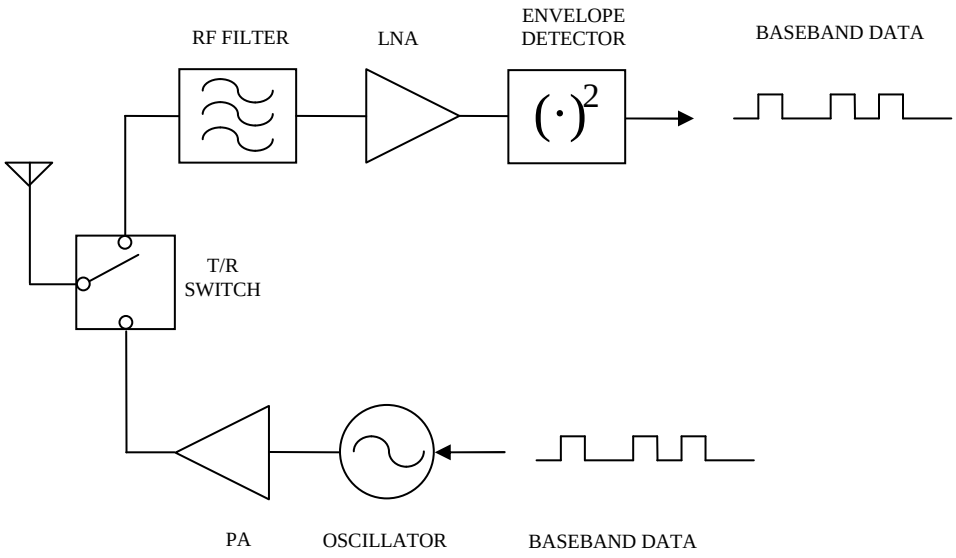


Figure 2. 4. Typical block diagram of direct modulation/demodulation transceiver

There are two main drawbacks with the direct modulation/demodulation architecture. First, selectivity must be provided through narrowband filtering directly at radio section since the self-mixing operation is insensitive to phase and frequency. Second, this architecture suffers from poorer sensitivity if there is no filter and due to limited sensitivity of a diode-based envelope detector. The direct modulation/demodulation transceiver is an enhanced version of the simple diode rectifiers used in RFID tags, which were shown earlier to have poor sensitivity. The addition of high frequency gain is expensive from a power perspective, so direct modulation/demodulation transceivers usually exhibit inferior sensitivity compared to frequency mixing architectures. Despite these drawbacks, the direct modulation/demodulation transceiver is a favourable architecture for wireless sensor networks which is required to have low complexity, low power consumption and low data rate. The direct modulation/demodulation transceiver is also suited for the on-off keying (OOK) modulation scheme which can be generated by switching the oscillator on and off, and the envelope detector rectifies the modulated signal for baseband processing.

2.2 Technology Considerations

The Speckled Computing Consortium is currently developing sensor nodes which will be 5mm×5mm×5mm in dimension and in addition to various sensors such as pressure, temperature etc, will also include a rechargeable battery, wireless communication link, on-board signal processing and a stripped down microprocessor in the 125 mm^3 volume.

An autonomous sensor node of this volume requires the majority to be occupied by the battery in order to maximize node lifetime. As a result, the antenna and radio transceiver must fit into an area of 5mm×5mm and also have a low profile to minimize the volume occupied. This would suggest operating at high carrier frequencies to minimize the antenna size, however this results in additional inter-node free space loss and therefore a requirement to consume more power in the radio transceiver to transmit higher power signals and produce higher gain in the receiver. Thus, sensitivity is decreased with larger bandwidth and higher noise of amplifier. Operating at lower frequencies has the advantage of reduced free space losses and therefore lower transmit power requirements, but at the expense of a larger antenna size. In both cases, an ultra-low power transistor technology is required to optimally utilize the available battery power for inter-node communication. Thus, the frequency band in which the transceivers will operate is considered to minimize the antenna size, and a suitable device technology is also considered to operate in the chosen frequency band.

2.2.1 Operating Frequency Band

Early transceivers designed for wireless sensor networks typically operated within the industrial, scientific and medical (ISM) radio bands such as 433MHz, 915MHz and 2.4GHz because these bands are typically intended for unlicensed operation. Therefore, these transceivers are predicted to suffer from a large antenna size which can increases a sensor node size since the wavelengths are decided by operating frequency and it is proportional to the size of the antenna. Consequently the communication frequency should be high in order to minimize the size of antenna and thus sensor node. The ISM band also has several higher frequency bands such as 5.8GHz and 24GHz. The power link budget must also be considered for the frequency plan because inter-node communication has a path loss for communication in free space and increases with frequency. To consider the frequency band, the power-link budget is needed to optimize a frequency band for transceiver. The power link budget is calculated by using transmission equation with

collected data from simulated and experimental results. A block diagram showing the parameters used to calculate the free space loss is shown in Figure 2.5. From Figure 2.5, the Friis transmission equation is given as the ratio of transmitter power and receiver power.

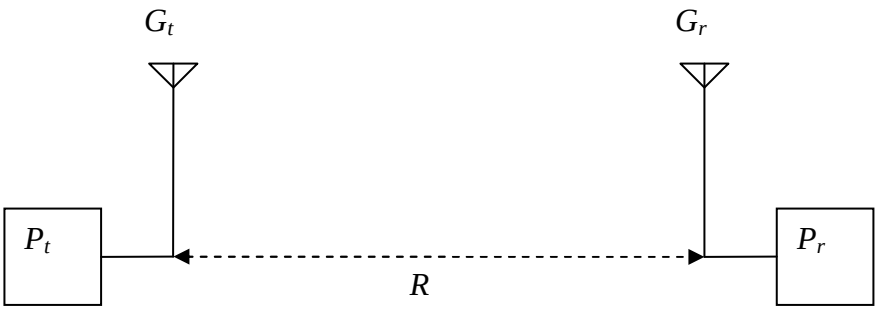


Figure 2. 5. Basic block diagram illustrating Friis transmission equation

The ratio of power received by the receiving antenna, P_r, to power input to the transmitting antenna, P_t, is given by

$$\frac{P_r}{P_t} = \left(\frac{\lambda}{4\pi RL}\right)^2 G_t G_r \tag{2.1}$$

$$P_{r(dBm)} = 10Log\left(\frac{P_r}{1\times 10^{-3}}\right) \tag{2.2}$$

where G_t and G_r are the antenna gain of the transmitting and receiving antennas, respectively, λ is the wavelength, R is the distance, and L is the loss factor. The antenna gains are with respect to isotropic. The free space loss according to Equations 2.1 and 2.2 is inversely proportional to the square of the wavelength. In other words, the loss increases as the frequency increases or the wavelength gets shorter. This also means that the effective area of an antenna will decrease with increasing frequency [19].

Lower frequencies imply larger antennas; if higher gain is needed to compensate for path loss, this also increases antenna size. However, higher frequencies must be used to realize a small size radio transceiver. In addition, the device gain performance at a chosen operating frequency must be considered to achieve the required performance of circuits and transceiver without additional power consumption and increasing circuit size.

These relations can be easily shown by plotting Equation 2.1 versus antenna separation distance in order to consider the power link budget at different operating frequencies.

Figure 2.6 shows the theoretical free space path loss versus antenna separation distance for the ISM frequency bands at 915MHz, 2.4GHz, 5.8GHz and 24GHz.

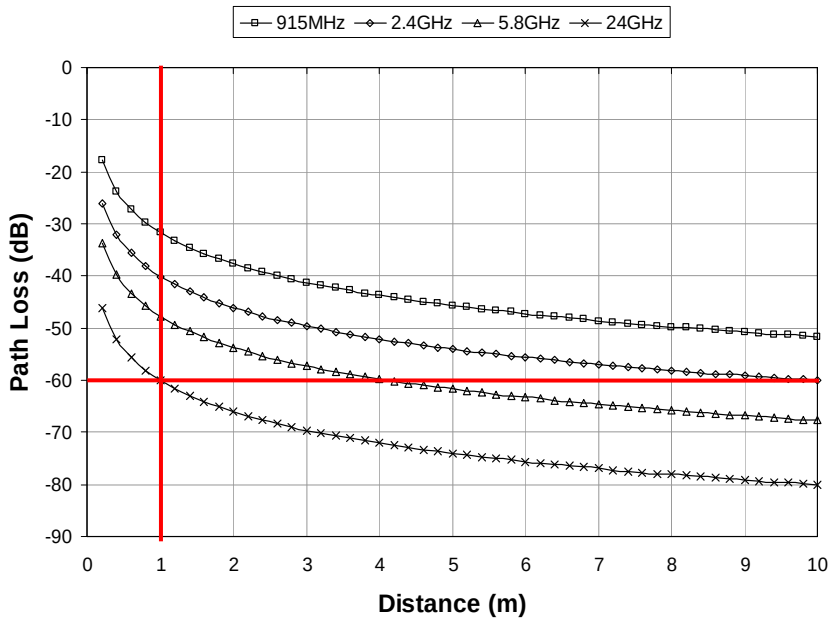


Figure 2. 6. Free space path loss versus distance for several ISM frequency bands

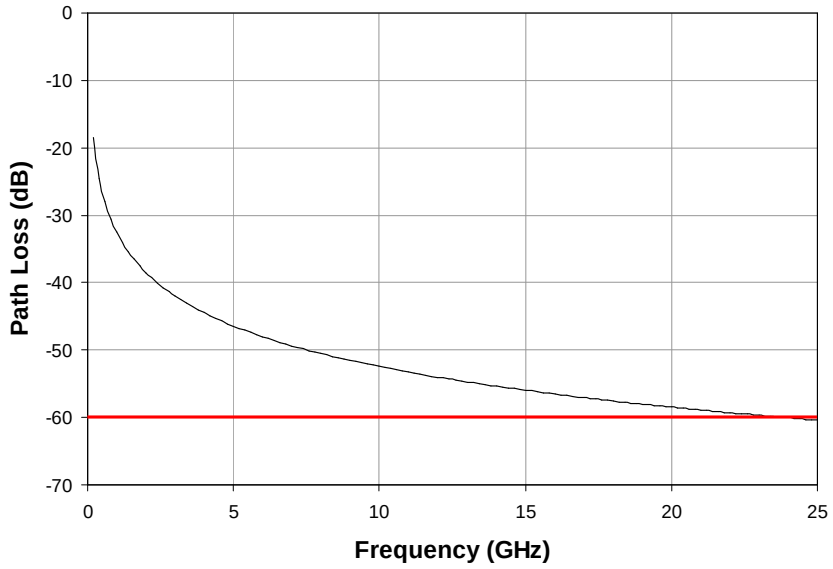


Figure 2. 7. Free space path loss versus frequency for 1metre distance

Figure 2.7 shows the operating frequency versus the path loss for a communication distance of one metre. For example, at 24GHz, $\lambda=0.0125\ m$ and if both antennas are considered to be isotropic radiators (*i.e.* gain of 1dB), with a separation of $R=1\ m$, loss factor of $L=1$ and the transmitting power of *0 dBm (1mW)*, then the received power will be *-60dBm* (*0.01μW*). This means that there is a 60dB loss in the channel. It is important to

remember that this only occurs if the antennas are pointing directly at each other and there is no polarization mismatch. In the case of transmit power of -10dBm, the receiving power will be -70dBm and this path loss will be agreeable loss for direct modulation/demodulation transceiver architecture with the 7dB gain of the receiver. Therefore, the use of 24GHz frequency for radio transceiver provides minimized antenna size and sensor nodes within the target volume of SpeckNet project.

2.2.2 Device Technology

For wireless sensor network applications, a reasonable choice for the transceiver circuitry is the standard complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC). Single-chip integration of digital, analogue, and communication circuitry is mandatory to reduce the hardware cost and scaled CMOS is proven to be a good platform for RF circuits as well as digital. For analogue and RF design, however, the performance of the active devices is not the only consideration. Passive devices also play a key role in determining the ultimate limits of gain and power consumption. In particular, the antenna is an important factor in determining the size of transceiver. Therefore, the frequency plan for reducing an antenna size is needed for compact transceiver which is targeted by SpeckNet project. At high frequency to reduce antenna size, advanced device technology is required to achieve the high gain, low noise, agreeable power, and high sensitivity of radio transceiver while radio transceiver still consumes low dc power. Also performances of active circuits are considered and designed for entire performance of transceiver.

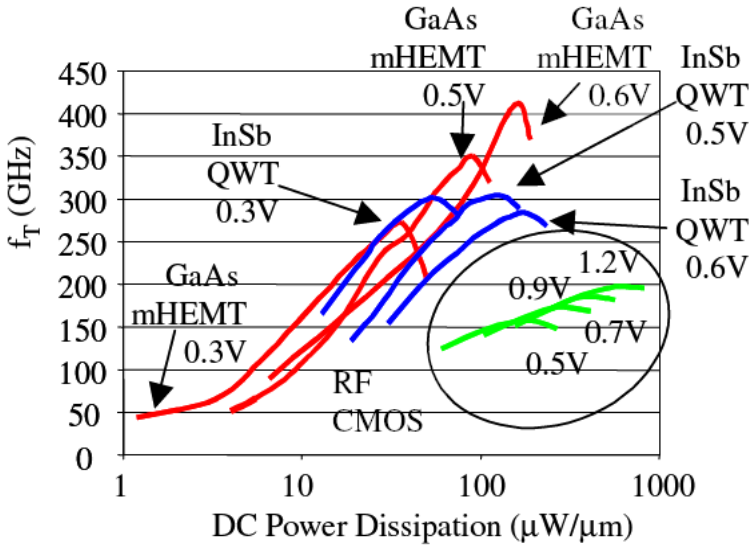


Figure 2. 8. Comparison of cut-off frequency (f_T) versus dc power consumption in different device technologies [21]

To minimize power consumption at high frequency, a GaAs metamorphic high electron mobility transistor (MHEMT) device technology is considered for SpeckNet project. This device technology is shown to significantly outperform high performance RF CMOS technologies. Recent study using CMOS technologies has reported the improvement of frequency performance up to millimetre-wave application, but GaAs MHEMT device technology is still the dominant technology for high gain, low noise and low power applications at high frequencies. Figure 2.8 shows the f_T versus dc power consumption performance for the 50nm GaAs MHEMT technology, 90nm (60nm physical gate length) RF CMOS and 85 nm InSb quantum well transistors (QWT) described in [20].

As can be seen, the GaAs MHEMT offer significant advantages in comparison with a RF CMOS technology and, whilst having slightly inferior performance for drain bias of 0.3V (10% lower), outperform the InSb QWT technology for drain biases of 0.5V and 0.6V (up to 33% higher). At a drain bias condition of 0.6V, the noise figure and associated gain of the devices are indicated in Table 2.1 for 24GHz ISM bands [21].

Frequency (GHz)	NF min (dB)	MSG(dB)
24	0.7	10.0

Table 2. 1. Noise performance of 50nm GaAs MHEMT technology

	Frequency (GHz)	Specification	DC Power (μW)
LNA	24	Gain >4.4dB Return Loss <-7dB	300
Oscillator	24	P_{out}: -10 dBm	300

Table 2. 2. Output of ultra-low power design

To verify performance of the device in the 24GHz, several circuits were demonstrated using simulation tool and this demonstration shows an agreeable performance for ultra-low power transceiver. Table 2.2 shows power consumption, gain and output power for low noise amplifier (LNA) and oscillator which mainly govern the majority of the power consumption in the direct modulation/demodulation transceivers [21].

Thus, GaAs MHEMT devices are particularly suitable because they have the properties of low noise, low operating voltage and high gain at high frequency for compact antenna and thus sensor node size.

2.2.3 Existing Transceivers for WSN

For wireless sensor network applications, short range radio transceivers are developed to achieve a small size and ultra-low power consumption with reasonable data rate. TRC103 in [7] is a single chip, multi-channel, low power RF transceiver. It is an ideal fit for low cost, high volume, two-way short range wireless application in the 863-960 MHz frequency bands. It has high sensitivity of -112dBm, low receiver current of 3.3mA, and high data rate up to 200 kbps with FSK or OOK modulation scheme. RFM also has 2.4GHz low power transceiver for short range wireless applications [8]. It has high sensitivity of -95dBm with 250 kbps, receive current of 18mA, transmit current of 13mA with 0dBm output power, and high data rate up to 1Mbps.

Texas Instrument is a company for low power RF transceiver has 1GHz and 2.4GHz low power RF transceiver chips. CC1000 is a true single-chip UHF transceiver designed for very low power and very low voltage wireless applications [9]. The circuit is mainly intended for the ISM and short range device (SRD) frequency bands at 315MHz, 433MHz, 868MHz and 915 MHz. This chip has receiver sensitivity of -110dBm, receiving current consumption of 7.4mA, transmit current consumption of 10.4mA and date rate of 76.8kbps with FSK or OOK modulation scheme. CC2420 is a single-chip 2.4GHz IEEE 802.15.4 compliant RF transceiver designed for low power and low voltage wireless applications [10]. It has receiving current consumption of 19.7mA, transmitting current consumption of 17.4mA and data rate of 250kbps with offset quadrature phase-shift keying (OQPSK) modulation scheme.

An energy-efficient OOK transceiver with power amplifier and SAW filter is shown in [11]. The receiver power consumption scales from 0.5mW to 2.6mW, with an associated sensitivity of -37dBm to -65dBm. The transmitter consumes 3.8mW to 9.1mW with output power from -11.4dBm to -2.2dBm. With target requirements of SpeckNet project, performances of the transceiver are compared with existing low power transceiver. Figure 2.9 shows the performance of state of the art low power radio transceiver for wireless sensor applications. Table 2.3 also shows the other performance of proposed transceiver to compare with existing low power radio transceivers. The power consumption of the transceiver for wireless sensor applications is important challenge since it must be used for a long time without frequent replacement, so the amount of current consumption in receiver and transmitter is very important to reduce dc power consumption in the radio transceiver. The proposed transceiver shows the lowest current consumption in the receiver and transmitter. Consequently, the proposed radio transceiver for SpeckNet project can

achieve ultra-low dc power consumption with data rate up to 200kbps and compactness for wireless sensor applications.

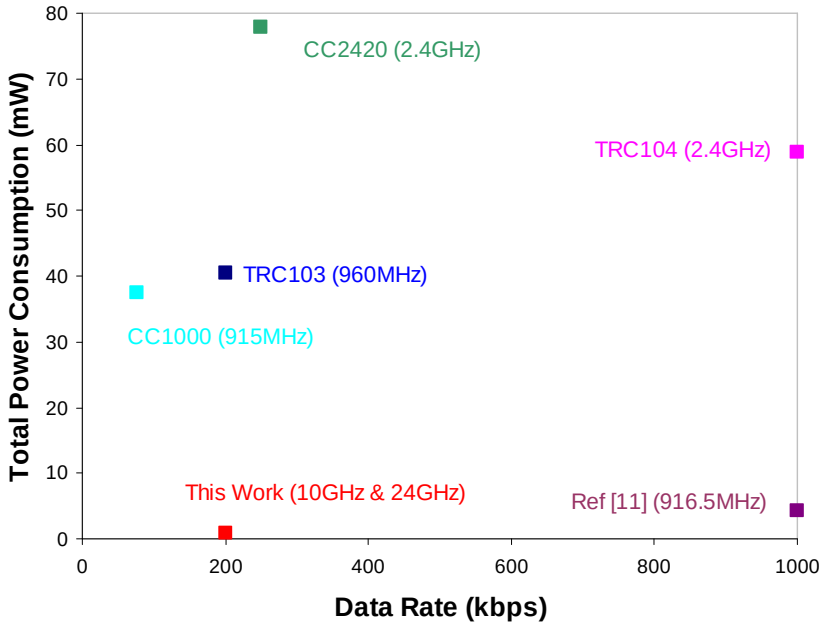


Figure 2. 9. Comparison of state-of-the art radio transceivers with total power consumption versus data rate

	Frequency (GHz)	Modulation	TX Current (mA)	RX Current (mA)	Size(mm^2)
TRC103	0.96	OOK/FSK	16	3.3	5×5
TRC104	2.4	OOK/FSK	13	18	4×4
CC1000	0.915	OOK/FSK	10.4	7.4	9.7×6.4
CC2420	2.4	OQPSK	17.4	7.4	6×6
Ref [11]	0.916	OOK	-	-	1.3×1.4
This work	10	OOK	1.4	1.4	5×12
This work	24	OOK	1.6	2.9	5×5

Table 2. 3. Features of state-of-the art radio transceivers for WSN

2.3 Conclusions

In this chapter, different transceiver architectures and considerations to implement a radio transceiver have been discussed. From the discussions in this chapter, it is concluded that the traditional transceiver architectures such as the super-heterodyne, zero-IF and low-IF transceivers are not suitable for sensor nodes because these architecture require

frequency conversion mixers and PLL synthesizers which are power-hungry elements. These architectures also are a complex in structure, thus they are unsuitable for realizing ultra-low dc power consumption and compact size of transceivers. The super-regenerative transceiver has also been discussed to be unsuitable method because it has a drawback of inherent frequency instability and its characteristics strongly depend on the performance of the super-regenerative oscillator. Therefore the super-regenerative receiver requires a highly stable and low phase noise oscillator. In addition, interference is also caused by radiation from the quench oscillator and the addition of an oscillator in the receive path increases the overall power consumption of the transceiver. In order to realize the simplest transceiver, an OOK radio transceiver consisting of a switched oscillator for direct modulation and passive envelope detector for direct demodulation is an appropriate choice because it minimizes the physical size and power consumption due to its simple structure. The considerations of transceiver performance suggest that operating around 24GHz to achieve maximum radio range with a small antenna size is a good choice to meet the target size and power consumption specifications for the SpeckNet project.

Chapter 3

Circuits Design

As mentioned in the previous chapter, the direct conversion transceiver suffers from power consumption and a large volume mainly due to its power-hungry frequency synthesizer with VCO. To overcome these problems, the direct modulation/demodulation transceiver can be employed. This chapter presents the design method of radio circuits for radio transceiver with direct modulation/demodulation transceiver architecture, the OOK modulation scheme and a HEMT device technology. The transmitter eliminates mixers and digital modulator, and replaces the power-hungry frequency synthesizer with a low power switched oscillator to reduce the power consumption. The receiver also eliminates mixers, digital demodulator, and replaced the power-hungry frequency synthesizer with a low power envelope detector to reduce power consumption and minimize its size.

The transceiver architecture is introduced, followed by a discussion on the design methodology of each individual circuit blocks to implement radio transceiver in this chapter. Prototypes of the individual circuits have been developed using a quasi-MMIC approach, in which the passive components are fabricated monolithically on GaAs substrate while commercial active devices are integrated using hybrid assembly techniques. This approach was taken to reduce the development costs and turnaround time.

3.1 Transceiver Architecture

As aforementioned, the direct modulation/demodulation transceiver architecture, an OOK modulation scheme and a HEMT device technology will be employed for radio transceiver of SpeckNet project with a single channel operation [21]. Figure 3.1 shows a block diagram of direct modulation/demodulation transceiver that is applied to complete an ultra-low power radio transceiver for wireless sensor node. The transceiver only has two active circuit blocks consisting of an oscillator and a low noise amplifier because a SPDT switch and an envelope detector will be a passive HEMT device which is pinched off for low power consumption.

The transmitter employs on-off keying (OOK) modulation by using the baseband data to power cycle the oscillator via a switch in its gate bias. Oscillators are turned on/off at the same time with baseband data for highly efficient OOK transmitter. But the start-up time

of oscillator is less than 1μsec to support up to 200 kbit/s data rate [22]. In conventional high data rate OOK transmitters, an oscillator and a buffer amplifier are both kept turned-on and then the signal is modulated by a lossy switch located at the end of buffer amplifier [23].

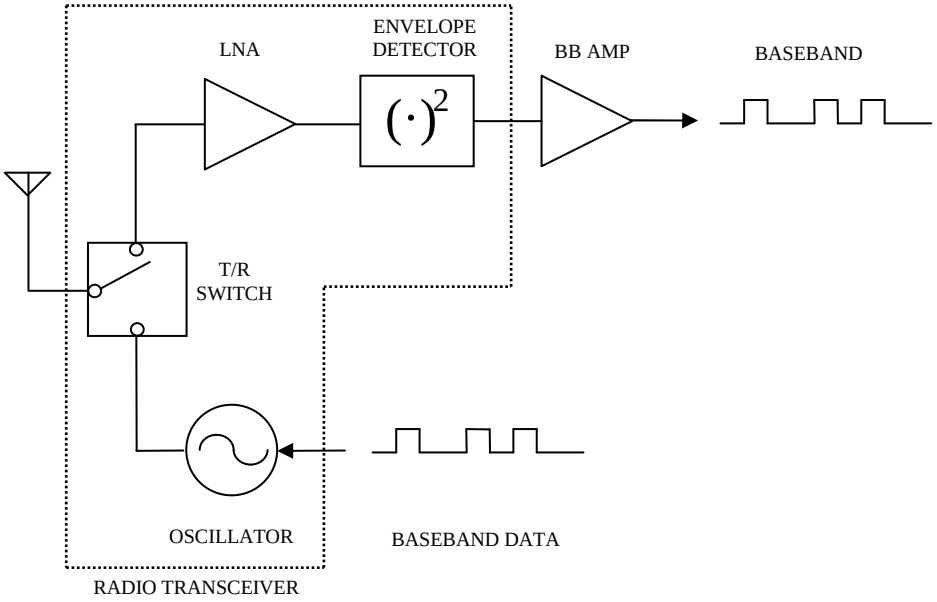


Figure 3. 1. Block diagram of direct modulation/demodulation transceiver

However, in order to design ultra-low dc power consumption OOK transmitter, transmitter only employs an oscillator that should be switched on/off with baseband data. Thus a fast start-up oscillator is required for ultra-low power and high data rate transmitter. Generally, an oscillator starting to oscillate from noise level needs a long start-up time since it undergoes a feedback loop many times to reach steady-state power level. But, when an oscillator biased by a power supply is turned on abruptly, the start-up time of the oscillator is decreased since the *LC* resonator which takes a step current is damped by its resonant frequency. Because the oscillator frequency and the damping frequency of the *LC* resonator are almost the same, the initial damping signal becomes the initial oscillation signal. Since this signal level is much larger than the noise level, the start-up time can be much reduced. Consequently, in order to design a fast start-up oscillator, the initial damping amplitude of resonator for each of various oscillators needs to be calculated. Since Colpitts oscillator is one of the most widely used oscillators of single ended type, it can be used to achieve ultra-low dc power and high data rate OOK transmitter.

The receiver directly detects modulated carrier signal by using the amplifier and envelope detector with low power consumption. Since the OOK receiver has simple structure, it can be implemented with a small chip size. Traditional super-heterodyne OOK receiver incorporates LNA, mixer, PLL, IF filter, IF amplifier and demodulator. Usually

off-chip resistor and capacitor are necessary for the loop filter in the PLL. The OOK receiver in [24] uses envelope detection technique to get rid of the frequency conversion circuits like the mixer and PLL, which improves integration and reduces power consumption. Based on this configuration, an OOK receiver is proposed for WSN.

The receiver is designed with narrow bandwidth to satisfy the requirement of high sensitivity with ultra-low dc power consumption. In the RF front-end, the LNA applied common source feedback structure to achieve narrowband matching and stability. Besides, a high frequency envelope detector realizes envelope amplitude demodulation. The value of the storage capacitor in the envelope detector is critical. Large capacitance can reduce the ripple and improve the sensitivity. But it degrades the tracking speed and limits the data rate. In this receiver, allowable range of the capacitance has been deduced according to the requirement of ripple and tracking speed. Most importantly, the way to relax the trade-off between sensitivity and data rate has been presented. The OOK modulated signal is received by the antenna and amplified by LNAs. Then the envelope detector demodulates the baseband signal by directly extracting the amplitude information of the input signal. In the baseband process, the AGC maintains the magnitude of the final output voltage constant against different receiving power. Finally, the output buffer generates the digital signal for the following ASIC chip.

To realize the radio transceiver, the specifications of individual circuits are very important to achieve a communication range more than 1 metre and power consumption less than 1mW. Therefore a link budget using a radio transceiver block diagram is required to confirm the specifications of individual circuits while the transceiver has a reasonable performance for this project. Figure 3.2 shows the block diagram to complete the link budget using ADS.

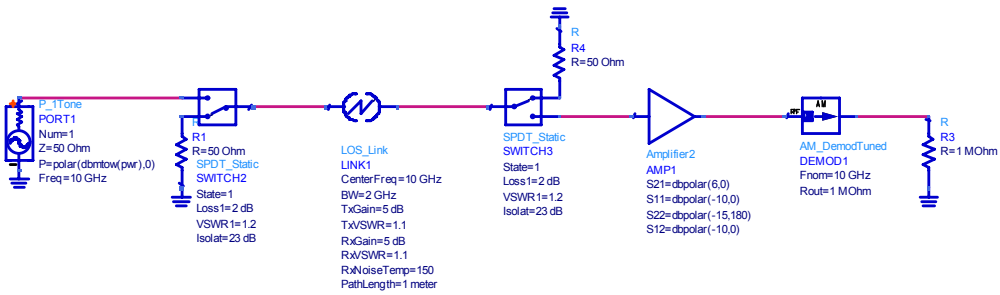


Figure 3. 2. Block diagram of power link budget simulation

The operating frequency is decided to achieve small antenna size and low power consumption simultaneously with considering device performance. Increasing the operating frequency will reduce the size of the transceiver due to small antenna size,

however, the device performance must be also considered to achieve a reasonable performance of individual circuit to realize an appropriate sensitivity and power consumption for low power transceiver that can be used over a communication range of a least 1 metre. Thus, the operating frequency is chosen to be 10GHz. A FET and HEMT normally have dc-to-ac conversion efficiency of 20~30%, therefore, in case of 25% efficiency, the output power of transmitted oscillator can be assumed to be -10dBm while the oscillator consumes dc power of 400μW. The switch is assumed to have insertion loss of 2dB and isolation of 20dB. This specification of switch is reasonable to achieve with a cold-HEMT topology. The amplifier is assumed to have 6dB gain, input return loss of 10dB, output return loss of 15dB and isolation of 10dB. The transceiver has no filter, thus, bandwidth of frequency is decided by antenna, switch and 3dB bandwidth of amplifier. The bandwidth is assumed to be 2GHz by considering the 3dB bandwidth of narrow band amplifier. Also, the antenna gain is important to realize a link budget due to influence of sensitivity. Here, both antenna gains are considered to be 1dB and 5dB. Figure 3.3 compares the output power of amplifier considering these two values of antenna gains and a 1metre separation distance.

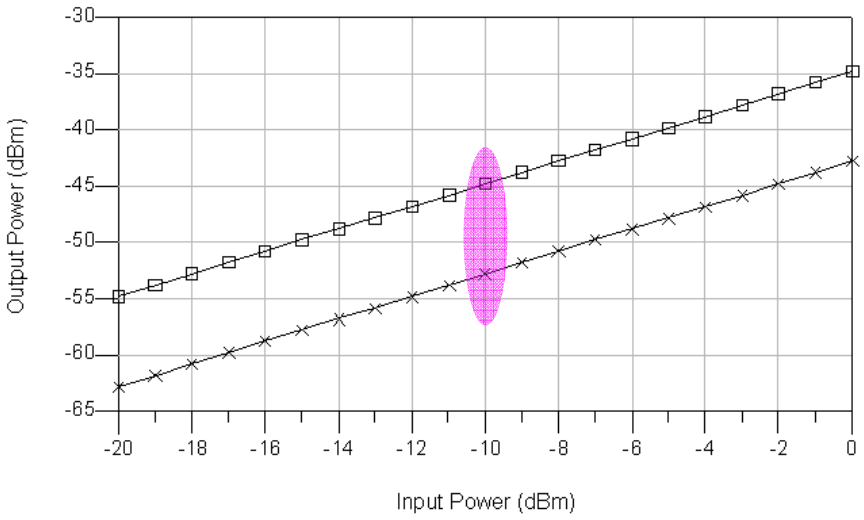


Figure 3. 3. Output power of amplifier with antenna gains of 1dB (×) and 5dB (□)

From Figure 3.3, the detector is required to achieve a sensitivity of -45dBm or -53dBm with output voltage of 1mV which is a reasonable value to process in baseband amplifier. Therefore, the performance of detector is very important to achieve OOK radio transceiver with low power consumption and range of 1 metre. The detector requires the choice of a good topology using diode or HEMT device for high sensitivity. By realizing individual circuits with this link budget, the transceiver can be completed to achieve low power consumption with a communication range of a least 1metre.

3.2 Description of MMIC Process

To implement a quasi-MMIC and MMIC radio transceiver, an advanced III-V compound semiconductor process based on semi-insulating GaAs substrates in University of Glasgow is used. CPW transmission lines are used to implement the circuit interconnection on the MMIC. It consists of a signal conductor placed between two ground planes, and since the dominant mode of CPW is quasi-TEM there is no low-frequency cut-off. Unlike microstrip, CPW does not require via-holes to realize a connection to common ground and it suffers from much less dispersion making CPW suitable for millimetre-wave circuits. The characteristic impedance can be also realized with almost any track width and gap combination of CPW line. With the back-face ground plane removed, lumped elements exhibit less parasitic capacitance. The air bridge is also used to avoid degeneration from quasi-TEM into a balanced coupled-slotline mode. The MMIC processing as part of this project were performed by Dr Harold M.H. Chong, Dr Richard Oxland, Susan Ferguson and Helen McLelland.

For fabrication of MMIC, several lithographic steps are required in the following order. Firstly, the gold metal layer of 133nm thickness which is used for markers, text, bottom metal of the metal-insulator-metal (MIM) Silicon Nitride (SiN) capacitor and a fine structure, is deposited on the substrate. The SiN layer of 150nm thickness is used as the dielectric for MIM SiN capacitors. A 33nm thick, 50 Ω/square, nichrome (NiCr) layer is deposited using the e-beam evaporation and lift-off technique for resistors. The gold layer of 1.2μm thickness is deposited for the CPW transmission lines and top metal of MIM SiN capacitors. Finally, for MMICs, electroplated air bridges are used to obtain a connection between two common ground planes.

3.3 Metal-Insulator-Metal (MIM) SiN Capacitors

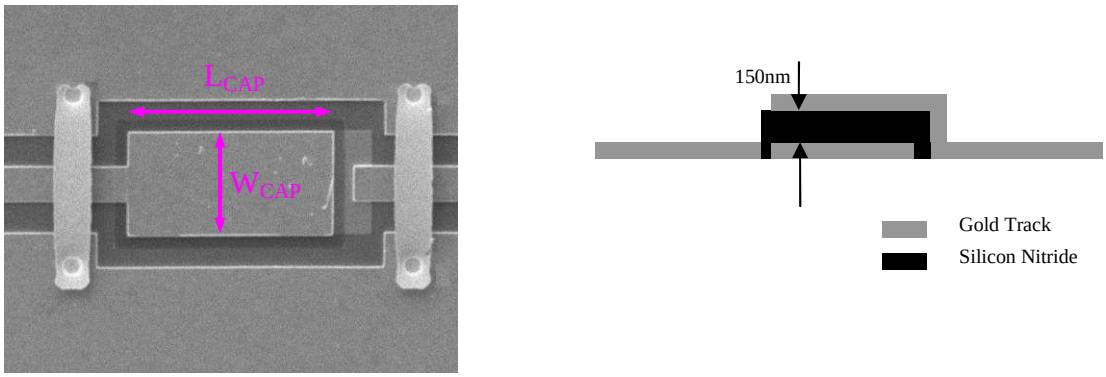


Figure 3. 4. The top and side views of a series MIM SiN capacitor

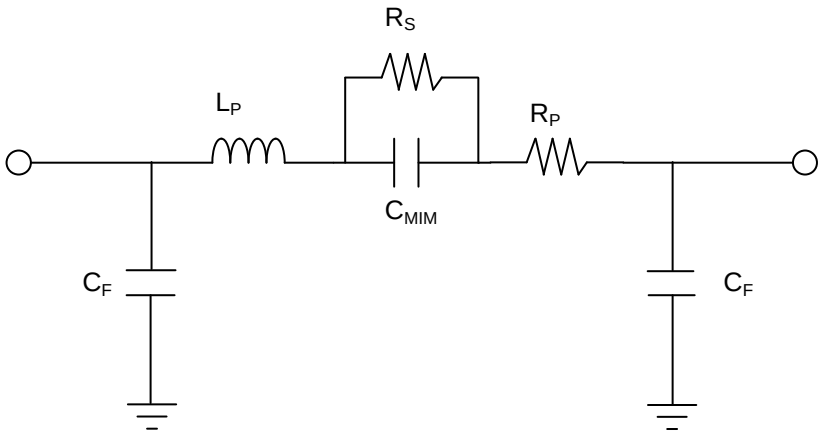


Figure 3. 5. The equivalent circuits of a series MIM SiN capacitor

The capacitor is formed by sandwiching a layer of silicon nitride dielectric between two metal plates, as shown in Figure 3.4. The MIM SiN capacitor is used for matching networks, supply bypass and dc blocking either in series or shunt connection. Figure 3.5 shows its equivalent circuit.

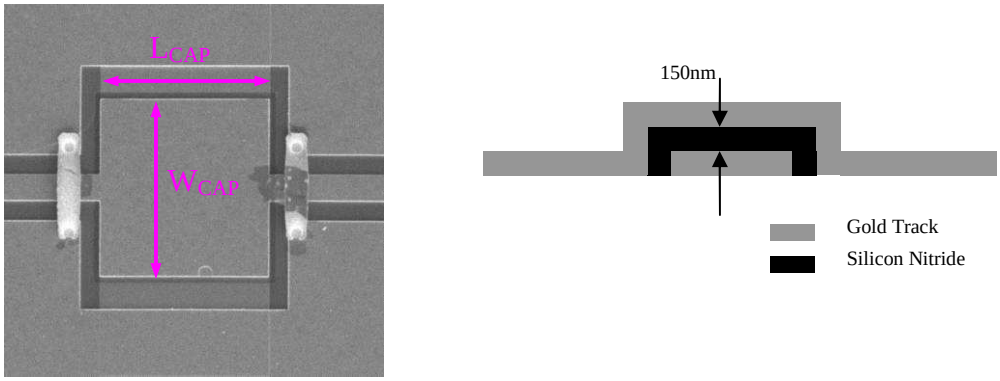


Figure 3. 6. The top and side views of a shunt MIM SiN capacitor

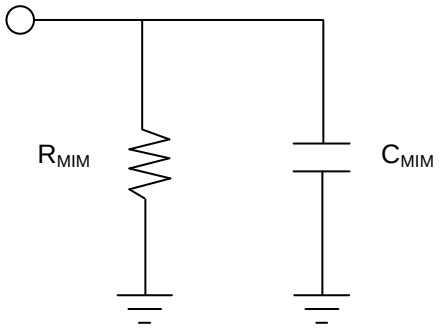


Figure 3. 7. The equivalent circuits of a shunt MIM SiN capacitor

Figure 3.6 shows the top and side views of a shunt MIM SiN capacitor and Figure 3.7 shows its equivalent circuit.

As shown in Figure 3.4, the series capacitor has a dielectric filled gap (*d*) which is placed between the gold metals. The top metal is directly connected in CPW transmission line but the bottom metal is separated with a dielectric gap of approximately 5μm from CPW transmission line. Therefore the series capacitor can be used for dc blocking.

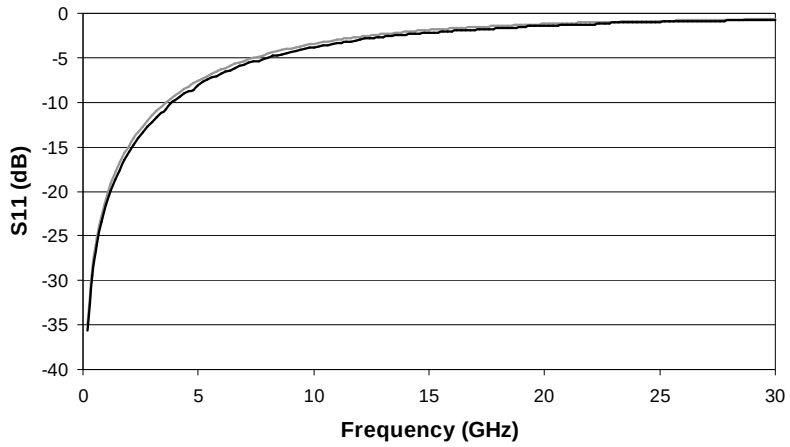


Figure 3. 8. Reflection of shunt capacitor: measurement (black), simulation (grey)

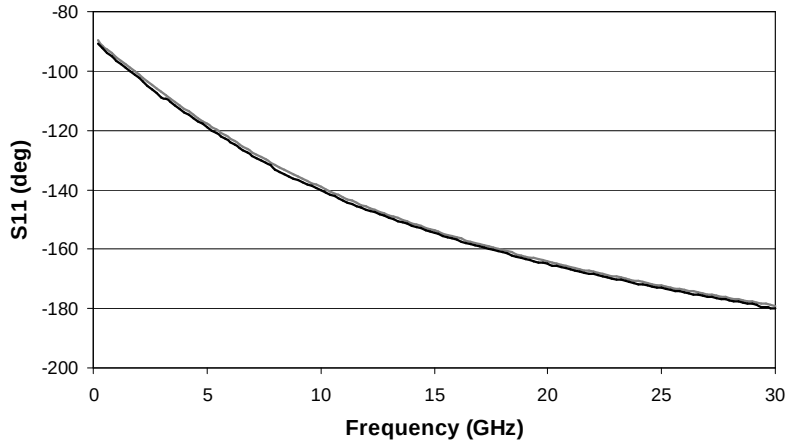


Figure 3. 9. Phase performance of shunt capacitor: measurement (black), simulation (grey)

Typical fabrication geometries and dielectric thickness mean that MIM structures are generally used for on-chip capacitance values in the range 0.1~20pF. In case of the dielectric thickness is 150nm and the relative permittivity is approximately 7.1, a typical unit area capacitance of 0.4fF/μm^2 is obtained. Figure 3.8 and 3.9 show the measured and simulated reflection characteristics for a two-port shunt capacitor which is 60μm in length and 20μm in width. Ansoft HFSS was used to simulate the structure and the measurement was performed on-wafer using Cascade Microtech GSG probe and an Agilent network analyzer. Other capacitors both series and shunt capacitors are obtained with a good agreement between simulation and measurement.

The approximate capacitance of a MIM SiN capacitor structure can be calculated using Equation 3.1.

$$C_{ideal} = \varepsilon_o \varepsilon_r \frac{wl}{d} \tag{3.1}$$

where ε_0 is the permittivity of free space, ε_r is relative permittivity of the dielectric, w is the plate width, l is the plate length and d is the thickness of the dielectric. To this, a term for the fringing capacitance must be added. By comparing the measured and ideal capacitance a term for the fringing capacitance per μm of edge can be derived. The empirically derived formula for the corrected capacitance including fringing term is given by Equation 3.2 [25].

$$C_{corr} = \varepsilon_o \varepsilon_r \frac{wl}{d} + 7.8 \times 10^{-5} wl \tag{3.2}$$

Table 3.1 shows the extracted parameter values for equivalent circuits of each different series capacitor structure.

L_{CAP} (μm)	W_{CAP} (μm)	C_{MIN} (fF)	L_P (pH)	C_F (fF)	R_S (kΩ)	R_P (Ω)
20	20	118	0.9	0.6	1	0.4
30	20	171	5.3	1.4	1	0.4
40	20	226	6	1.5	1	1
60	20	315	6.3	1.6	1	1.2

Table 3. 1. Extracted parameter values for equivalent circuits of series MIM capacitors

3.4 Spiral Inductors

The spiral inductor represents one of the basic passive elements in MMIC design. It allows lumped elements to be used instead of inductive transmission line structure, therefore reducing the size of the circuit. In order to design MMIC inductors using coplanar waveguides as the main transmission line it is necessary to characterize as many standard subsections of the layout as possible. Figure 3.10 shows the microphotograph of one coplanar waveguide (CPW) MMIC spiral inductor. Figure 3.11 shows the equivalent circuit of CPW MMIC spiral inductor with three turns and the width and space of the spiral track of 10μm. Several inductor structures with different turns and spaces were fabricated,

measured and compared with simulation results. Figure 3.12 and Figure 3.13 show a comparison of the simulated and measured S21 parameters of inductor with overall dimension of 120μm and two turns. Figure 3.14 shows some illustrative modelled and measured inductances for different spiral geometries.

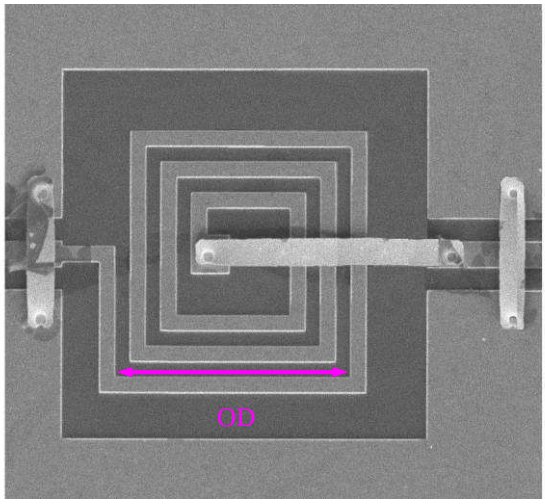


Figure 3. 10. Microphotograph for CPW MMIC spiral inductor

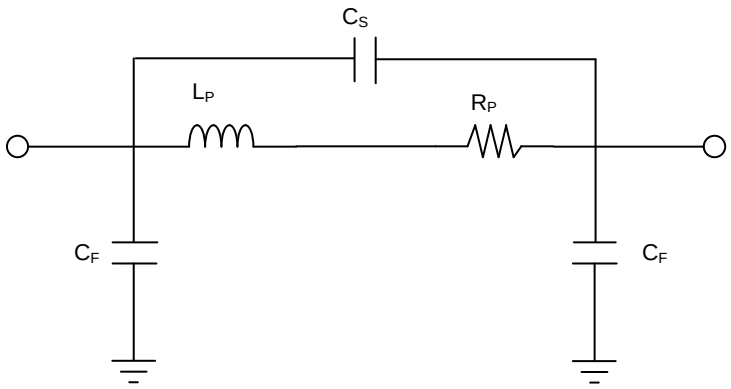


Figure 3. 11. Equivalent circuit of CPW MMIC spiral inductor

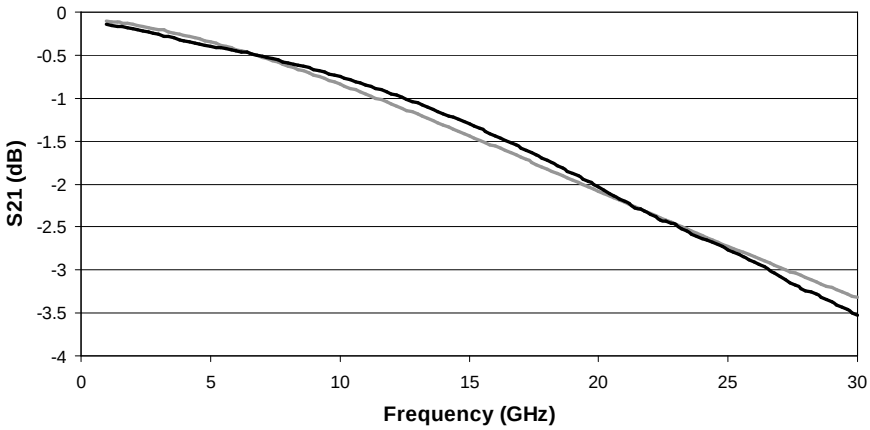


Figure 3. 12. Comparison of the modelled and measured S21 (dB): measurement (black) and model (grey)

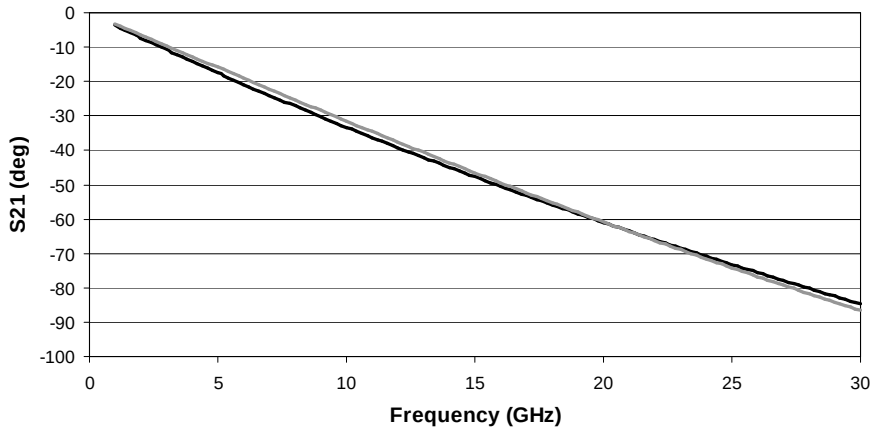


Figure 3. 13. Comparison of the modelled and measured phase (S21): measurement (black) and model (grey)

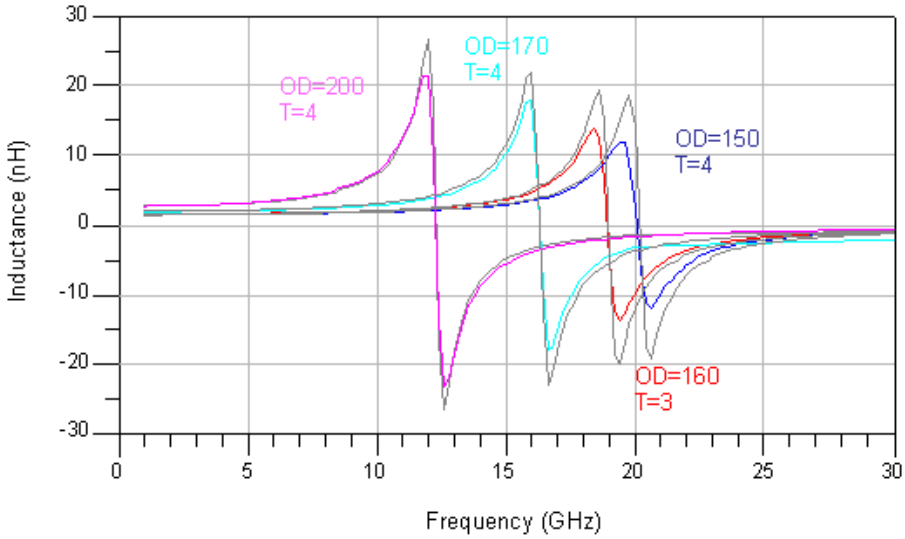


Figure 3. 14. Several illustrative modelled (grey) and measured inductances for different geometries

Table 3.2 shows the extracted parameter values for their equivalent circuits of each different structure.

OD (μm)	Turns	L_P (nH)	R_P (Ω)	C_S (fF)	C_F (fF)
120	2	0.82	4.4	0.01	37.5
150	4	1.41	6.56	0.01	44.1
160	3	1.49	6.6	0.01	47.2
170	4	1.95	8.56	0.01	48.8
200	4	2.73	10.5	0.01	61.3

Table 3. 2. Extracted parameter values for equivalent circuits of spiral inductors

3.5 PHEMT Device

For the circuit design, a commercial pseudomorphic HEMT device, RFMD FPD-200 was selected for its performance and availability. The FPD-200 is an AlGaAs/InGaAs pseudomorphic high electron mobility transistor (PHEMT), featuring a 0.25μm×200μm Schottky barrier gate, defined by high-resolution stepper-based photolithography [26]. The recessed gate structure minimizes parasitics to optimize frequency performance. The PHEMT device was measured on a coplanar waveguide (CPW) test structure with ground to signal gaps of 44μm and signal line width of 60μm which is fabricated on semi-insulating GaAs substrates. This structure was simulated using Ansoft HFSS and optimized comparing with dimensions. Figure 3.15 shows a CPW test substrate with bonded out PHEMT device.

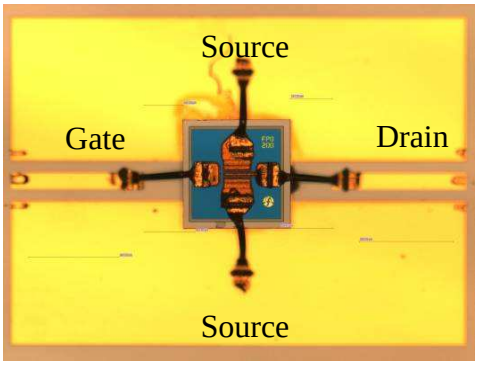


Figure 3. 15. Photograph of PHEMT device bonded out on CPW GaAs test substrate

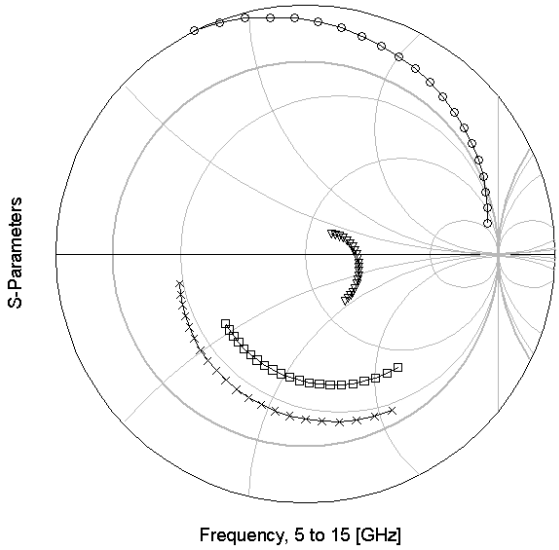


Figure 3. 16. Measured S-parameters of PHEMT device with embedded lines: S_{11} (×), S_{12} (∇), S_{21} (O), and S_{22} (□)

This substrate has embedded lines on input and output ports for probe measurement and the device was integrated using wire bond process with the gold wire diameter of 18μm. Measurements were taken with the substrate placed on top of quartz and after LRRM calibration with an alumina impedance standard substrate (ISS). Figure 3.16 shows the measured frequency responses with a bias condition of V_{gs}=-0.8V, V_{ds}=0.3V, and I_{ds}=1.4mA.

In order to obtain pure device S-parameters, the embedded lines for probe measurement must be de-embedded from measured S-parameters. Thus, the lengths of input and output which are 340μm and 350μm, respectively was de-embedded from measured S-parameters. Figure 3.17 shows device S-parameters with and without embedded lines. These S-parameters still include the gold wire connections but these S-parameters were used to design oscillator, amplifier, switch and detector because gold wires will still be used to integrate between substrate and device for implementation of individual circuits.

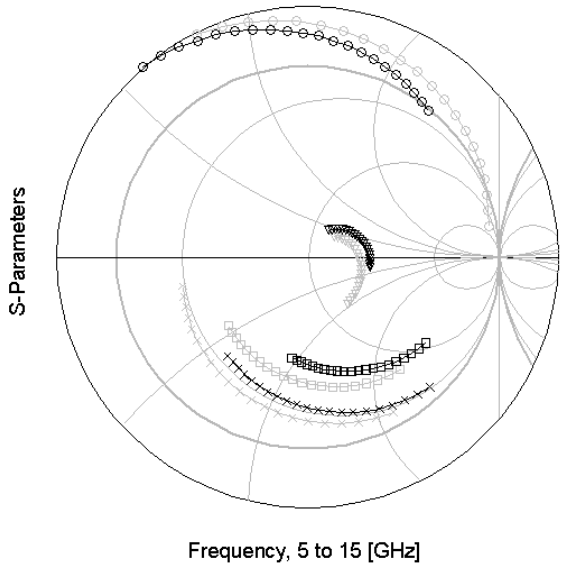
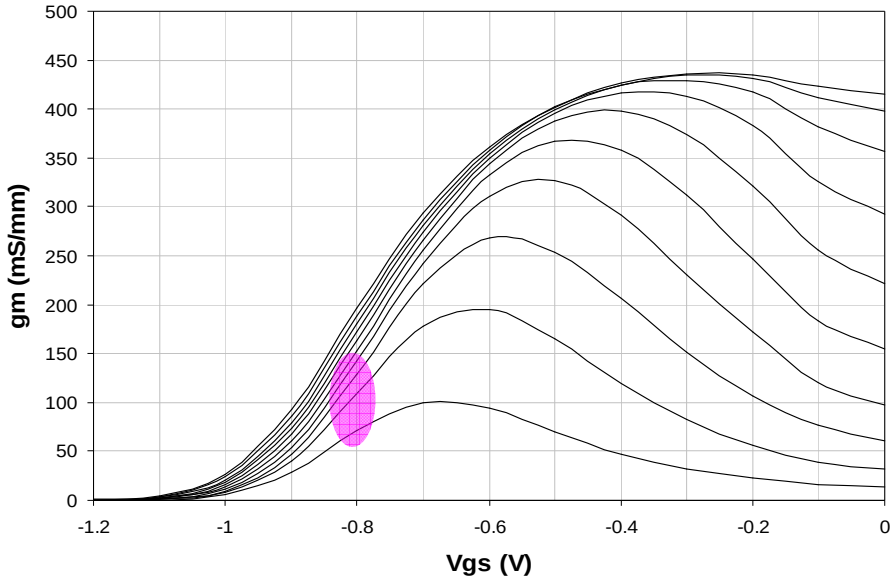


Figure 3. 17. Measured S-parameters of PHEMT device with embedded lines (grey) and de-embedded lines (black): S_{11} (×), S_{12} (∇), S_{21} (O), and S_{22} (□)

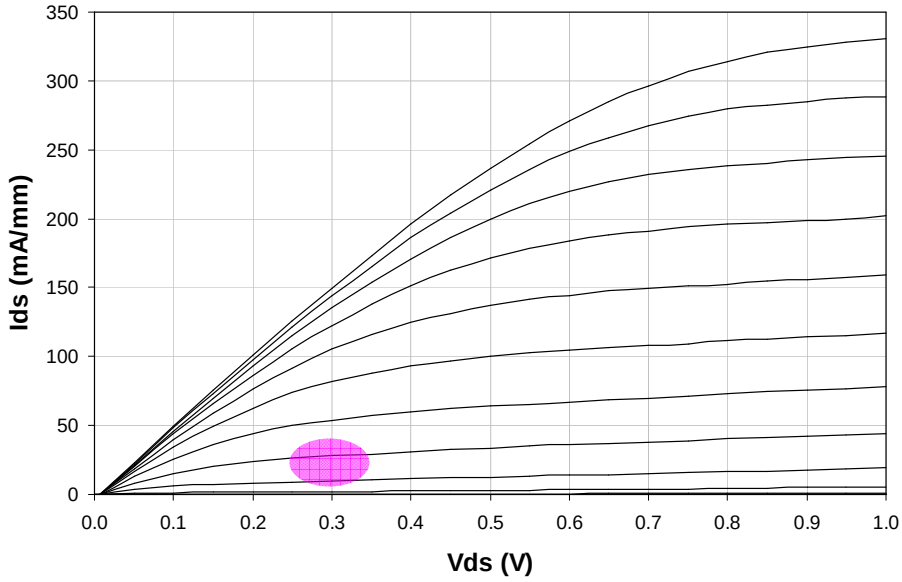
3.6 Non-linear Model of PHEMT Device

In the previous section, the pure S-parameters of PHEMT device were obtained with low power consumption. To increase design accuracy for integration of transceiver, non-linear simulation must be used with non-linear model of device. Especially, oscillator and detector must be designed with non-linear model to confirm the start-up time and envelope detection which determines the data rate and sensitivity of transceiver. In this section, a

non-linear model which is provided from a commercial simulation tool will be introduced. The non-linear parameters are extracted, and then the performance of extracted model is compared with measured *I-V* curves and S-parameters for the non-linear analysis of circuits.



(a)



(b)

Figure 3. 18. Measured (a) transconductance (g_m) and (b) *I-V* curves of the FPD-200 PHEMT (V_{ds}=0V to 1.0V and V_{gs}=-1.2V to 0V, 0.1V step)

Figure 3.18 shows the measured transconductance (g_m) versus gate voltage curve of device and *I-V* curves with gate voltage of 0V to -1.0V. Maximum g_m of device is 435 mS/mm when device is biased at a gate voltage of -0.2V and drain voltage of 1.0V with

drain current of 50mA. The grey areas shown on the *I-V* and g_m curves are the bias conditions used to realize the amplifier and oscillator for ultra-low power consumption. The model describes the device and the built-in inductance provided by the connecting bond wires. The metal fixture up until the connecting bond wires has been de-embedded.

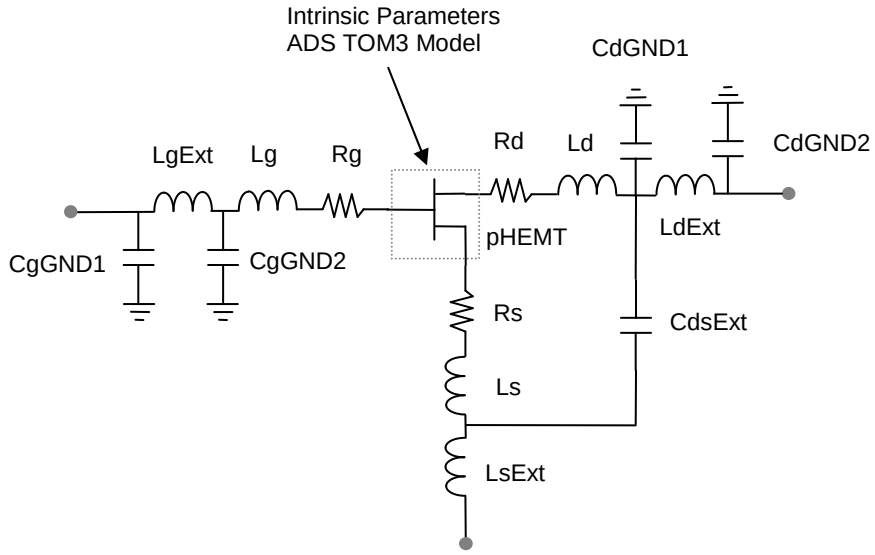


Figure 3. 19. The device model with external parameters

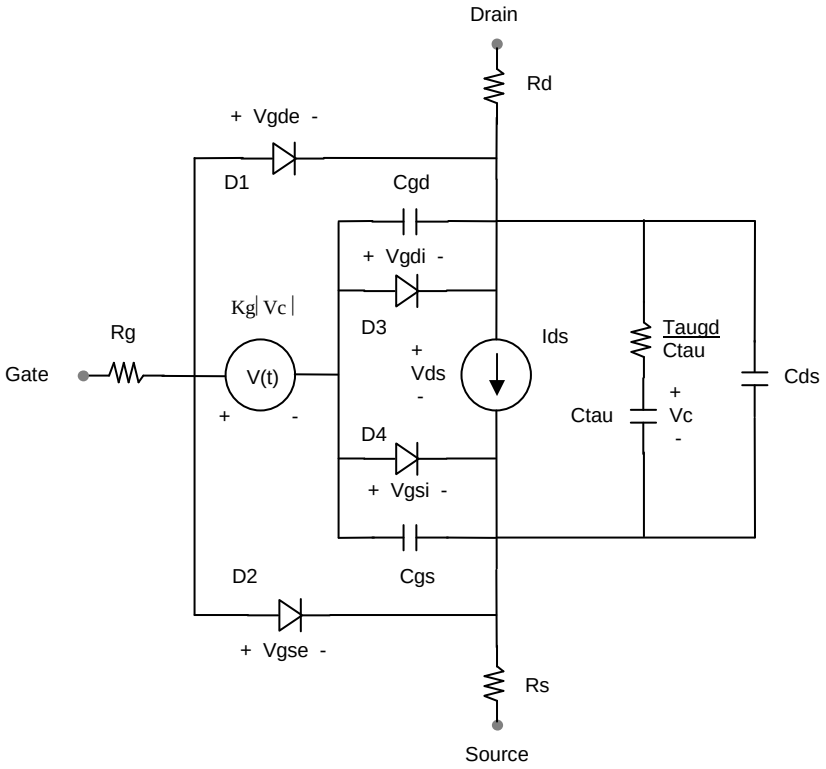


Figure 3. 20. Intrinsic equivalent circuit of TOM3 model

The TriQuint TOM3 model is a scalable non-linear model which provides a good fit to the measured data and has an advanced charge form with simple model parameters. Figure

3.19 shows the extrinsic networks which the external parameters present in the device model. The TOM3 model employs an excellent form for the charge relation within the PHEMT device. The TOM3 model is enhanced by providing charge-based models which are normally more robust and better justified theoretically [27].

Figure 3.20 shows the intrinsic equivalent circuit of the TOM3 model. R_d, R_g, and R_s are presented in this model but they are replaced by external parameters for this model which will be extracted. L_d, L_g, and L_s is also used with external parameters. The definition of model parameters is described in the Appendix.

The governing equations of the TOM3 model is based on charge relations, and the intrinsic parameters can be represented by DC drain-source current and gate charge as a function of the model parameters [27]. The TOM3 DC drain-source current equation is given by the following equation.

$$I_{ds} = I_0 \times (1 + \lambda V_{ds}) \tag{3.3}$$

where

$$I_0 = \beta \times (V_G)^Q \times f_k \tag{3.4}$$

$$f_k = \frac{\alpha V_{ds}}{(1 + (\alpha V_{ds})^k)^{1/k}} \tag{3.5}$$

$$V_G = Q \times V_{ST} \times \ln(1 + \exp(u)) \tag{3.6}$$

$$u = \frac{V_{gsi} - V_{TO} + \gamma V_{ds}}{Q \times V_{ST}} \tag{3.7}$$

$$V_{ST} = V_{ST0} \times (1 + M_{ST0} \times V_{ds}) \tag{3.8}$$

The model parameters for the drain current are λ, β, Q, α, k, V_{TO}, γ, V_{ST} and M_{STO}. For time-varying drain-source current, the voltage V_{gsi} is delayed by the transit time τ. The gate capacitances in the TOM3 model are derived from the following charge equations [27]-[28]. The total gate charge is given as

$$Q_{GG} = Q_{GL} \times f_T + Q_{GH} \times (1 - f_T) + Q_{GG0} \times (V_{gsi} + V_{gdi}) \tag{3.9}$$

where

$$f_T = \exp(-Q_{GGB} \times I_{ds} \times V_{ds}) \tag{3.10}$$

is a transition function combining the low power charge with the high power charge.

$$Q_{GL} = Q_{GQL} \times \exp(Q_{GAG} \times (V_{gsi} + V_{gdi})) \times \cosh(Q_{GAD} \times V_{ds}) + Q_{GCL} \times (V_{gsi} + V_{gdi}) \quad (3.11)$$

$$Q_{GH} = \left(Q_{GQH} \times \ln(1 + \frac{I_{ds}}{Q_{GI0}}) + Q_{GSH} \times V_{gsi} \right) + Q_{GDH} \times V_{gdi} \quad (3.12)$$

The model parameters for the gate charge are Q_{gg0}, Q_{ggb}, Q_{gql}, Q_{gag}, Q_{gcl}, Q_{gqh}, Q_{gi0}, Q_{gsh} and Q_{gdh}. There are two capacitance models (bias-dependent capacitances and charge models) in the TOM3 implementation in ADS. In the case of bias-dependent capacitances model, the gate-source and gate-drain self-capacitances are then defined as

$$C_{gs} = \left. \frac{\partial Q_{GG}}{\partial V_{gsi}} \right|_{V_{gdi}=const} \quad (3.13)$$

$$C_{gd} = \left. \frac{\partial Q_{GG}}{\partial V_{gdi}} \right|_{V_{gsi}=const} \quad (3.14)$$

and, correspondingly, their contribution to the drain, gate and source currents follows the partitioning as

$$I_{Cgsi} = C_{gs}(V_{gsi}, V_{gdi}) \times \frac{dV_{gsi}}{dt} \quad (3.15)$$

and

$$I_{Cgdi} = C_{gd}(V_{gsi}, V_{gdi}) \times \frac{dV_{gdi}}{dt} \quad (3.16)$$

In the case of charge mode, the total gate charge is partitioned equally onto the gate-source and gate-drain charge. Their derivatives with respect to the voltage V_{gsi} and V_{gdi} define the corresponding self-and trans-capacitances.

The four diodes in the TOM3 model represent the gate diode, leakage and breakdown. They are described by equations with parameters which represent diode operation for gate current control. The currents of diode 1 (*D1*) and 2 (*D2*) are given as

$$I_{gse} = I_s \times \left(\exp\left(\frac{V_{gse}}{\eta V_T} \right) - 1 \right) \quad (3.17)$$

$$I_{gde} = I_s \times \left(\exp\left(\frac{V_{gde}}{\eta V_T} \right) - 1 \right) \tag{3.18}$$

And the currents of diode 3 (*D3*) and 4 (*D4*) are given as

$$I_{Dgsi} = I_{LK} \times \left(1 - \exp\left(\frac{-V_{gsi}}{\varphi LK} \right) \right) \tag{3.19}$$

$$I_{Dgdi} = I_{LK} \times \left(1 - \exp\left(\frac{-V_{gdi}}{\varphi LK} \right) \right) \tag{3.20}$$

where V_T is the thermal voltage

$$V_T = \frac{k \times T}{q} \tag{3.21}$$

$k = 1.38 \times 10^{-23}$ (*Boltzmann's constant*)

$q = 1.602 \times 10^{-19}$ (*electron charge*)

I_s, η, I_{LK}, and ρLK are the model parameters. *T* is either equal to the device instance parameter *Temp*, or if *Temp* is not specified then *T=ambient_circuit_temperature+Trise*. V_{gse}, V_{gde}, V_{gsi} and V_{gdi} are instantaneous voltages across the respective diodes.

As mentioned above, the equations of the TOM3 model are in terms of model parameters that describe the operation of the device. The model consists of simple parameters to explain the gate charge and drain current of the device in low and high power operation [27]-[28]. The external parameters will be extracted from measured S-parameters of a cold-HEMT which has the probe pads de-embedded [29], and the intrinsic parameters will also be extracted by fitting to the measured S-parameters over bias conditions of V_{ds}=0V to 0.5V, V_{gs}=-1.2V to -0.5V.

With above method, the model parameters are extracted to achieve non-linear design for increasing design accuracy and the extracted model parameters for the FPD-200 device are shown in Table 3.3 and 3.4. Table 3.3 shows the extrinsic parameters which are fitted from cold PHEMT S-parameters [29]. Table 3.4 shows the intrinsic parameters which are extracted by fitting to the measured S-parameters with various bias conditions.

CdGND1	0.18 fF	Lg	57.07 pH
CdGND2	2.75 fF	LsExt	35.58 pH
CgGND1	7.25 fF	Ls	2.11 pH
CgGND2	41.66 fF	Rd	2.28 Ω
LdExt	99.82 pH	Rs	5.14 Ω
Ld	0 pH	Rg	7.42 Ω
LgExt	82.07 pH	CdsExt	54.47 fF

Table 3. 3. Extrinsic parameters of TOM3 model

Vto	-0.676659 V	Qgqh	9.29127E-16	Is	1.6516E-11 mA
Alpha	4.0024	Qgi0	1.5016E-6 A	Vbi	1 V
Beta	0.000856944	Qgag	1.9094	N	1
Lambda	-0.0185588	Qgad	2.86281	Xti	2
Gamma	0.0394972	Qggb	177.973	Eg	0.8
Q	0.856696	Qgcl	9.499E-17 F	NG	2
K	2.83507	Qgsh	4.627E-16 F	W	100 μm
Vst	0.0681122 V	Qgdh	2.0805e-17 F	Rgsh	0 Ω
Mst	0.209481	Qgg0	2.246E-16 F	Ls	0 nH
Ilk	1.8E-6 mA	Cds	0.000219 pF	Lg	0 nH
Plk	1.5 V	Tau	0.02 psec	Ld	0 nH
Kgamma	0.0142667	Rd	0.01 Ω	Qgql	1.18781E-15
Taugd	1000 nsec	Rg	0.01 Ω	Rs	0.01 Ω

Table 3. 4. Intrinsic parameters of TOM3 model

As mentioned, R_d, R_g and R_s are chosen as 0.01 Ω to avoid limitation value and repetition with external parameter of model. L_d, L_g and L_s are also chosen as 0 nH to avoid a repetition with external parameters of model. To confirm the accuracy of the extracted model parameters, *I-V* curves for gate voltage range of 0 to -1.0V and S-parameters at V_{ds}=0.3V and I_{ds}=1.4mA using model parameters are compared with measured *I-V* curve and S-parameters.

Figure 3.21 shows a comparison between measured and modelled *I-V* curve. Figure 3.22 shows a comparison between measured and modelled S-parameters at bias point of V_{ds}=0.3V and I_{ds}=1.4mA. This model shows a good agreement with measured *I-V* and S-

parameters, thus it is suitable to be used for designing linear and non-linear circuits with Harmonic Balance simulation.

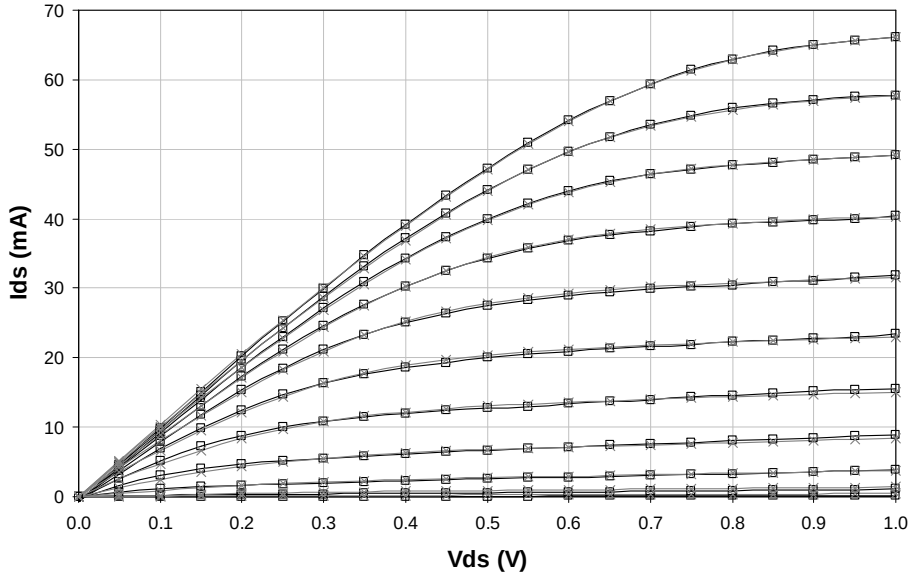


Figure 3. 21. Measured (□) and modelled (×) *I-V* curves of the FPD-200 PHEMT

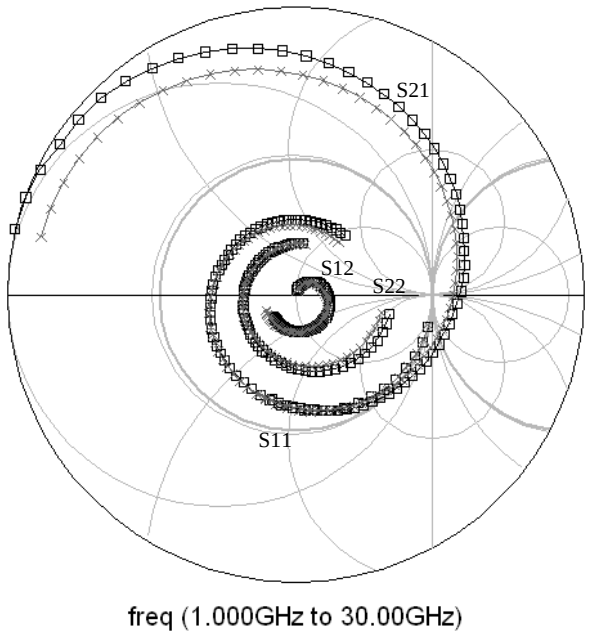


Figure 3. 22. Measured (□) and modelled (×) S-parameters of PHEMT at bias of V_{ds}=0.3V and I_{ds}=1.4mA

3.7 Oscillator

The oscillator is an essential component for microwave system. Oscillators can generally be categorized as negative resistance circuits [30]. In this section the analytical

techniques that are used in the design of negative resistance oscillator are discussed. The design principles of negative resistance oscillators are basically quite simple and straightforward. The negative resistance concepts are illustrated in Figure 3.23.

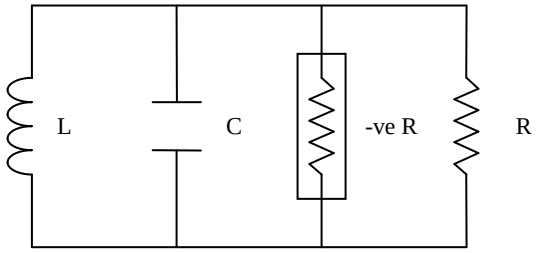


Figure 3. 23. The negative resistance concepts

At microwave frequencies, the negative resistance design technique is generally favoured. Negative resistors are easily designed by taking a three terminal active and applying the correct amount of feedback to a common port, such that the magnitude of the input reflection coefficient becomes greater than one. This implies that the real part of the input impedance is negative [31]. The input of the 2-port negative resistance circuit can now simply be terminated with one-third time resistance and opposite sign reactance to complete the oscillator circuit. Alternatively high-Q series or parallel resonator circuits can be used to generate higher quality and therefore lower phase noise oscillators. There are many configurations for negative resistance oscillators (e.g. Colpitts, Hartley and Clapp). The general block diagrams for two-port negative resistance oscillators are shown in Figure 3.24.

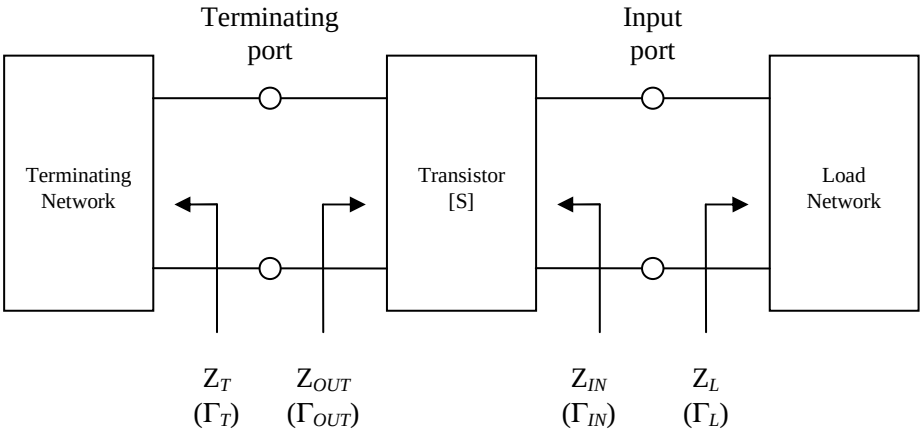


Figure 3. 24. General block diagram for two-port negative resistance oscillators

The transistor network is characterized by its S-parameters, Z_T is the terminating network impedance, and Z_L is the load impedance. In an oscillator, either port of the

transistor can be used as the terminating port. Once the terminating port is selected, the other port is referred to as the input port. The load-matching network is connected to the input port, in agreement with the one-port oscillator.

To design a negative resistance oscillator using two-port networks, firstly, a potentially unstable transistor at the frequency of oscillation ω_o is chosen and then the unstable region of the source stability circle can be plotted as shown in Figure 3.25. The terminal impedance, Γ_T is chosen to lie in the unstable region of the smith chart. This produces $|\Gamma_{IN}|>1$ (i.e. a negative resistance at the input port), so Γ_T is selected in this region for maximizing negative resistance. Series or shunt feedback can be used to increase $|\Gamma_{IN}|$.

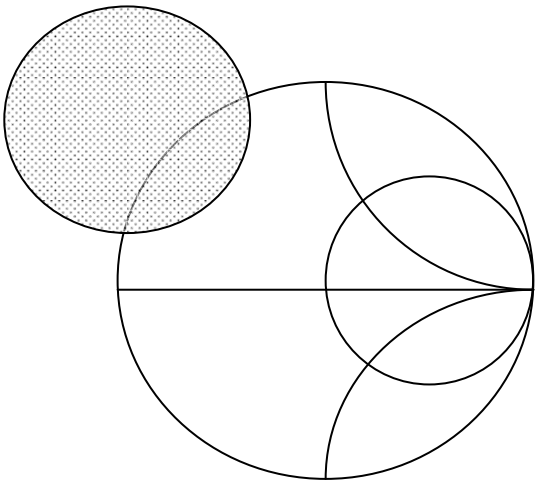


Figure 3. 25. Plot the unstable region of the source stability circle

The load network is designed to resonate Z_{IN} and satisfy the start of oscillation condition in Equation 3.22 and 3.23. That is, let

$$X_L(\omega_o) = -X_{IN}(\omega_o) \tag{3.22}$$

and

$$R_L = \frac{R_o}{3} \quad \text{(or, in general, } R_L = \frac{|R_{IN}(0,\omega)|}{3}\text{)} \tag{3.23}$$

This design procedure is popular due to its high rate of success. However, the frequency of oscillation will shift somewhat from its design value at $\omega_{o.}$ This occurs because the oscillation power increases until the negative resistance is equal to the load resistance and X_{IN} varies as a function of oscillation power [32]. Typically power efficiency is 20 to 30% for the HEMT device at 10GHz. Hence, if we fix the output power

at -10dBm we can expect the power consumption of the transmit oscillator to be 400μW assuming a power efficiency of 25%.

In order to design the oscillator circuit using ADS, the above procedure can be used with two-port S-parameter Touchstone files which are created by measurement of device (RFMD FPD-200) at a bias condition of V_{gs}=-0.8V, V_{ds}=0.3V, and I_{ds}=1.4mA. First of all, the source stability circle of device was plotted with measured S-parameters of the FPD-200 device using ADS simulation tool and the unstable region was selected and then any Γ_T in the unstable region was decided for producing $|\Gamma_{IN}|>1$ with short circuit or open circuit stubs. For the FPD-200 device at the bias condition of V_{gs}=-0.8V, V_{ds}=0.3V, and I_{ds}=1.4mA, the unstable region and any Γ_T were selected with open circuit stub as shown in Figure 3.26.

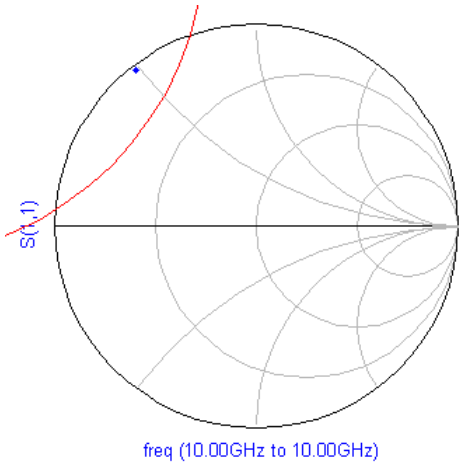


Figure 3. 26. Plot unstable region (red line) and any Γ_T point by open circuit stub

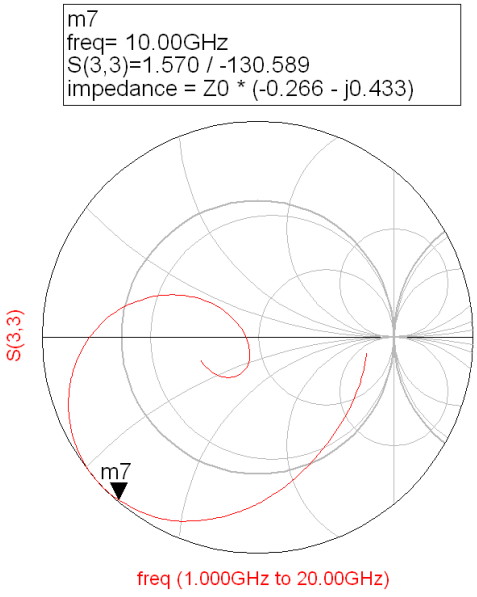


Figure 3. 27. The negative resistance of device for oscillation (Γ_{IN})

The terminating network which consists of open circuit stub was connected to input port of device and then the negative resistance was generated to oscillate at output port of a device. The negative resistance of device for oscillation is shown in Figure 3.27.

The load network can be implemented from output impedance of R_{IN} using Equation 3.22 and 3.23. Therefore, the impedance of the load network must be Z_O*(-0.088+j0.433) from the impedance of output port as shown in Figure 3.28. The impedance of load network which is designed using Equation 3.22 and 3.23 is shown in Figure 3.28.

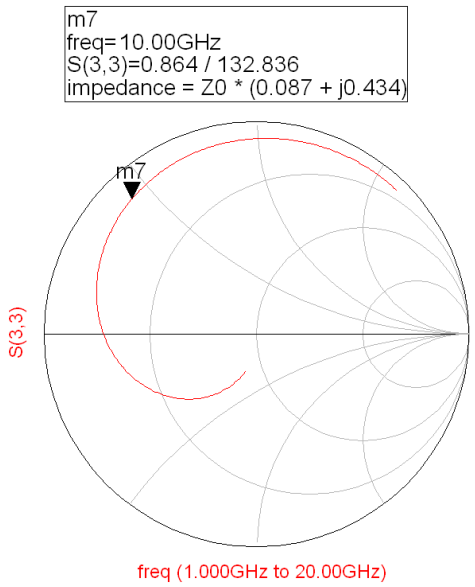


Figure 3. 28. Impedance of load network by Equation 3.22 and 3.23

The load network was connected to output port of device and then the circuit was simulated to oscillate at 10GHz with the condition of Re[Z_1]<-10 and Im[Z_1]=0 for steady state oscillation condition. Figure 3.29 shows the oscillation in 10GHz and real and imaginary of Z_1. Using simple design procedure, the oscillation performance was evaluated and oscillator circuit was simultaneously designed using PHEMT device (FPD-200). However, as previous mention, this procedure showed that the actual frequency of oscillation was somewhat shift from the designed value. Thus, the load network must be tuned to optimize the frequency of oscillation in the desired frequency. Consequently, the circuit can be designed for a higher frequency than required [25]. Also, the oscillation signal was transferred to load network for maximizing the output power of oscillator.

Figure 3.30 shows the optimal performance of oscillator using measured two port S-parameters. It has been shown that, by using the simple design method, an oscillator circuit can be optimized for output power whilst keeping the oscillator operating frequency constant. The oscillator has also been demonstrated with an optimized load network and maximized negative resistance circuit.

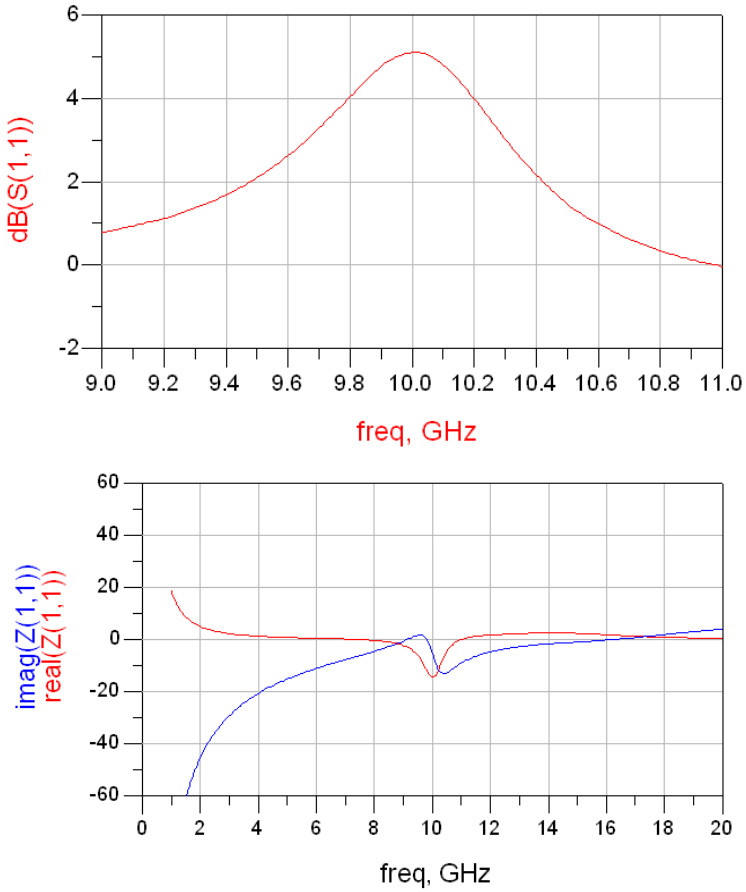


Figure 3. 29. Oscillation frequency and real and imaginary of Z_1

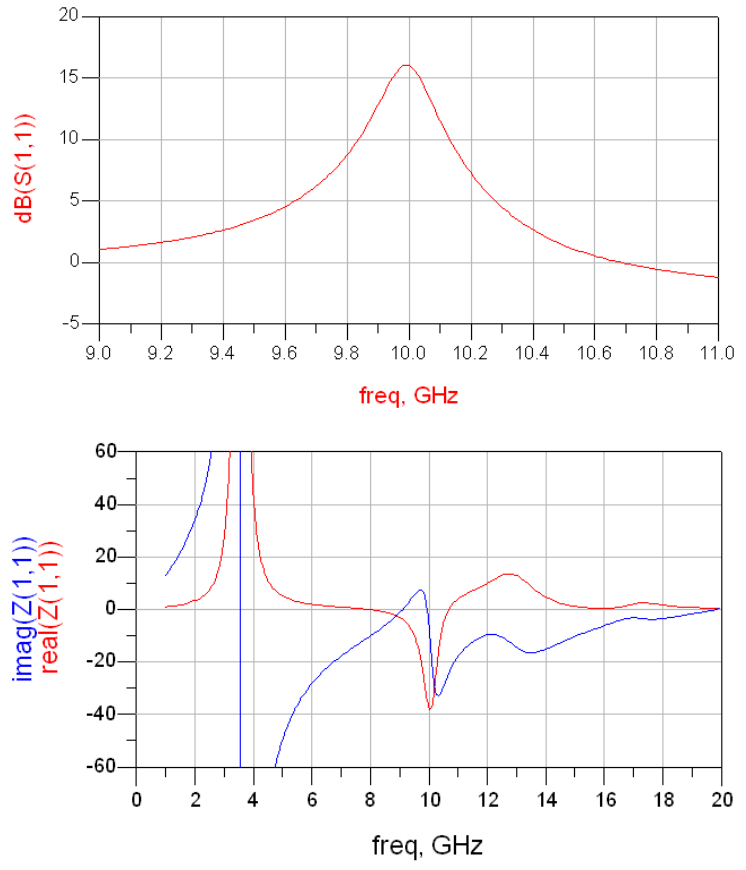


Figure 3. 30. Optimal performance of oscillator using measured two-port S-parameters

3.8 Amplifier

The amplifier in a transceiver performs the function of increasing the signal power from switch output. In the case of a direct demodulation receiver without any filter, the amplifier as well as envelope detector also needs a narrow bandwidth to maximize receiver sensitivity. Since the switch accepts a wideband input, the bandwidth of the amplifier directly affects the maximum sensitivity through the following Equation 3.24.

$$Sensitivity = -174dBm/Hz + 10\log(Bandwidth) + SNR + NF \quad (3.24)$$

In case of the measured 3dB bandwidth of the amplifier is 2GHz, and the NF of RF front-end is 5dB including the loss of switch, the receiver's required signal-to-noise ratio (SNR) is approximately 16dB for a 10^{-3} bit error rate (BER) [11]. The calculated sensitivity is -60dBm which satisfies the requirement for inter-node communication range of 1metre (in the transceiver system with the free space path loss of 52dB, antenna gain of 5dB, and transmitter output power of -10dBm). Thus, the amplifier must be designed for as narrow bandwidth as possible. Also, amplifier must achieve unconditional stability to prevent any oscillation by mismatch between amplifier and other circuits. Amplifiers can sometimes behave like an oscillator and generate unconditional oscillation signals in the system. Thus, amplifier must consider stability factor in their design. The stability can be determined from S-parameters, the matching networks, and the termination.

The two-port network shown in Figure 3.31 is said to unconditionally stable at a given frequency if the real parts of Z_{IN} and Z_{OUT} are greater than zero for all passive load and source impedances. If the two-port is not unconditionally stable, it is potentially unstable. That is, some passive load and source terminations can produce input and output impedance having a negative real part by mismatch.

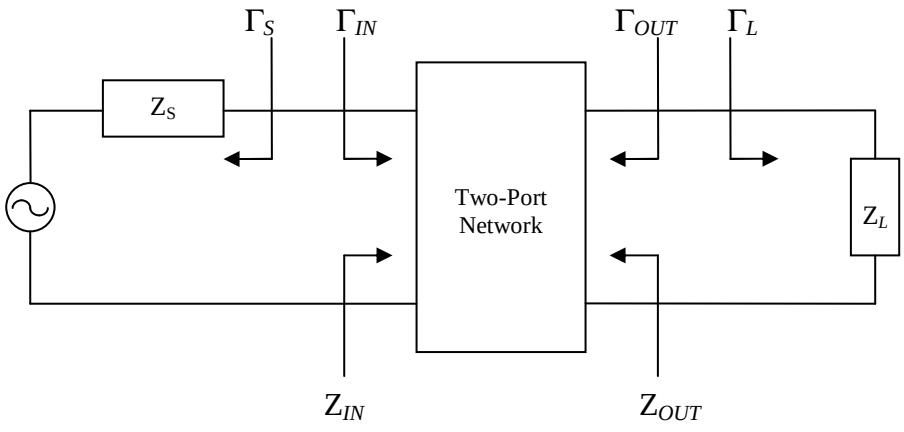


Figure 3. 31. Two-port network of amplifier

In terms of reflection coefficients, the conditions for unconditional stability at given frequency are shown in Equation 3.25, 3.26, 3.27, and 3.28.

$$|\Gamma_S| < 1 \tag{3.25}$$

$$|\Gamma_L| < 1 \tag{3.26}$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{3.27}$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{3.28}$$

where, all coefficients are normalized to the same characteristic impedance Z_O. A straightforward but somewhat lengthy manipulation of Equation 3.25 to 3.28 results in the following necessary and sufficient conditions for unconditional stability.

$$K > 1 \tag{3.29}$$

$$1 - |S_{11}|^2 > |S_{12}S_{21}| \tag{3.30}$$

$$1 - |S_{22}|^2 > |S_{12}S_{21}| \tag{3.31}$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{3.32}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.33}$$

There are other ways of expressing the necessary and sufficient conditions for unconditional stability [33]. Adding Equation 3.30 and 3.31 gives Equation 3.34.

$$2 - |S_{11}|^2 - |S_{22}|^2 > 2|S_{12}S_{21}| \tag{3.34}$$

Since $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \le |S_{11}S_{22}| + |S_{12}S_{21}|$, we use Equation 3.34 to obtain Equation 3.35 and 3.36.

$$|\Delta| < |S_{11}S_{22}| + 1 - \frac{1}{2}|S_{11}|^2 - \frac{1}{2}|S_{22}|^2 \tag{3.35}$$

$$|\Delta| < 1 - \frac{1}{2}(|S_{11}| - |S_{22}|)^2 \; or \; |\Delta| < 1 \tag{3.36}$$

The Equation 3.36 can be simply expressed as shown in Equation 3.37.

$$|\Delta| < 1 \tag{3.37}$$

Hence, a convenient way of expressing the necessary and sufficient conditions for unconditional stability is shown in Equation 3.29 and 3.37. If *K* is greater than 1 then the transistor is unconditionally stable, and if *K* is less than 1 the stability depends on the position of the source and load impedance relative to the stability circle, thus, in case of *K* of greater than 1 and Δ of less than 1, the transistor is unconditionally stable.

Figure 3.32 shows the simulated *K* stability factor and Δ for the FPD-200 PHEMT device at the bias condition of V_{gs}=-0.8V, V_{ds}=0.3V, and I_{ds}=1.4mA. It can be seen that *K* is less than 1 at low frequencies and that Δ is less than 1. In case of *K* of less than 1, there are some methods to realize an unconditional stable of the transistor and a resistive loading or series feedback method can be normally used at the drain side or source side of the transistor with producing lower noise figure (NF).

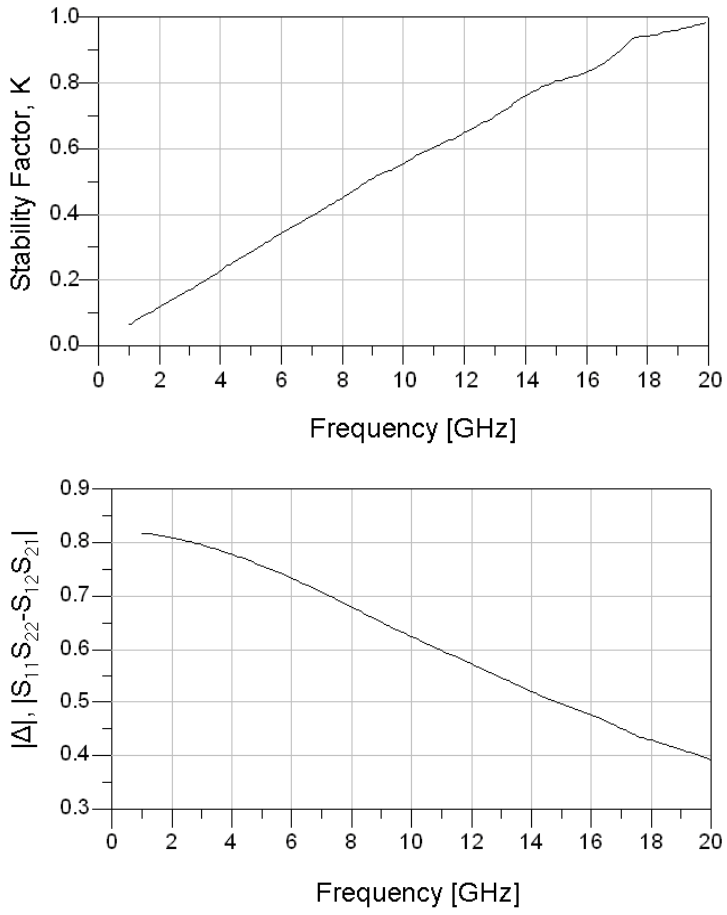


Figure 3. 32. *K* and $|\Delta|$ of FPD-200 PHEMT at the bias condition of V_{gs}=-0.8V, V_{ds}=0.3V, and I_{ds}=1.4*mA*

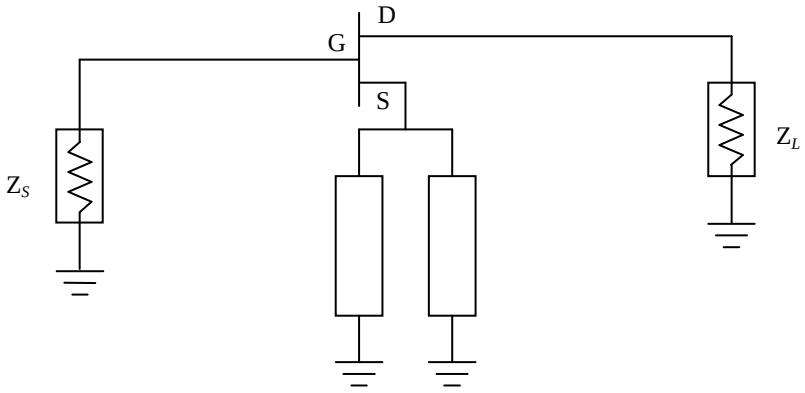


Figure 3. 33. Schematic of transistor with feedback inductance at the source side

Figure 3.33 shows the schematic of transistor with feedback inductance line at the source side. Figure 3.34 shows *K* and $|\Delta|$ for the same device with feedback inductance line that has 23° wavelengths at the source side.

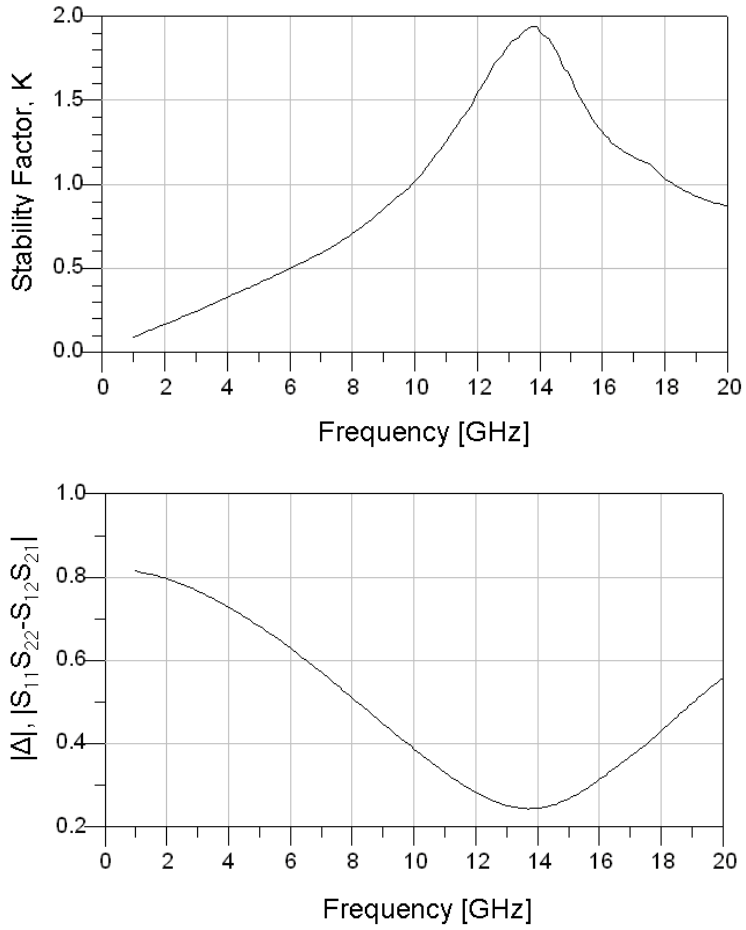
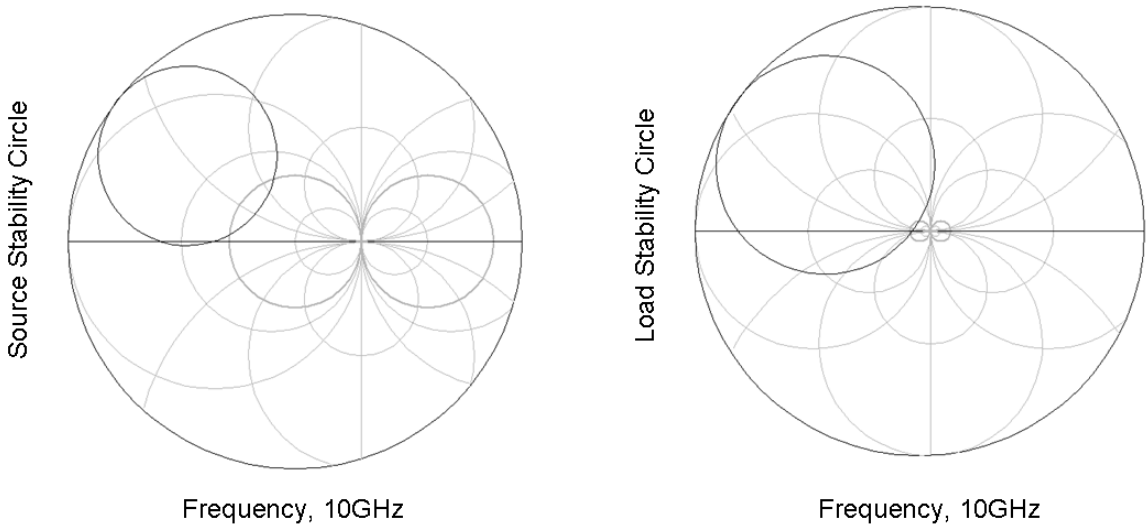
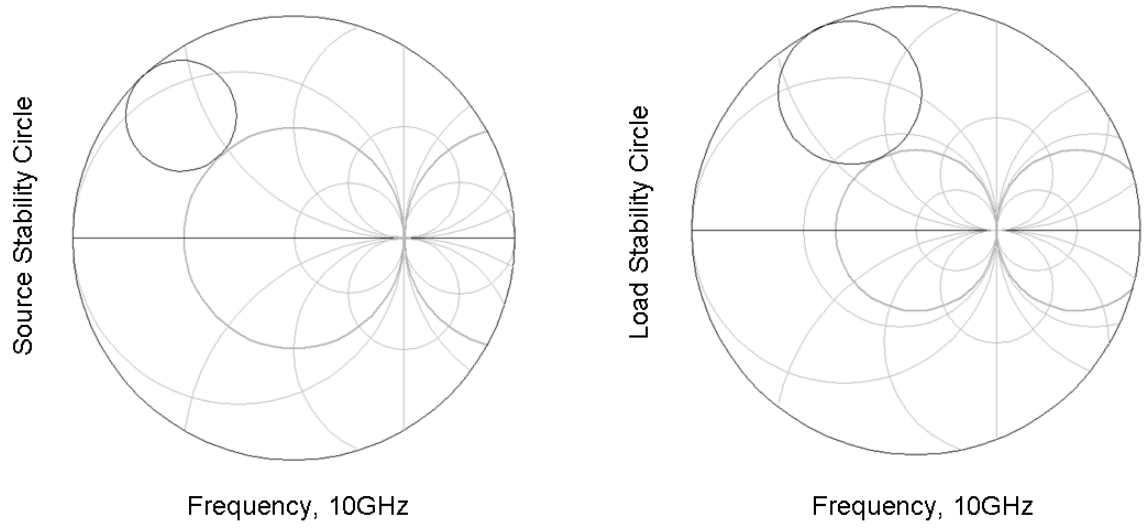


Figure 3. 34. *K* and $|\Delta|$ for the same transistor with feedback inductance line of 23° wavelength

Figure 3.35 shows the source and load stability circles at 10GHz before and after inserting feedback inductance. In both cases it can be seen that the effect of the feedback inductance is to move the stability circles outside the unity circle of the Smith chart. In the case of a transistor with feedback inductance, stability factor, *K*, is greater than 1, magnitudes of S11 and S22 are less than 1, and the stability circles place in outside the Smith chart the transistor can be conjugately matched.



(a)



(b)

Figure 3. 35. Source and load stability circles (a) before and (b) after inserting feedback inductance

For RF front-end amplifier of a receiver, the noise figure characteristic is an important factor with unconditional stability characteristic. Figure 3.36 shows the noise figure of two-stage amplifier.

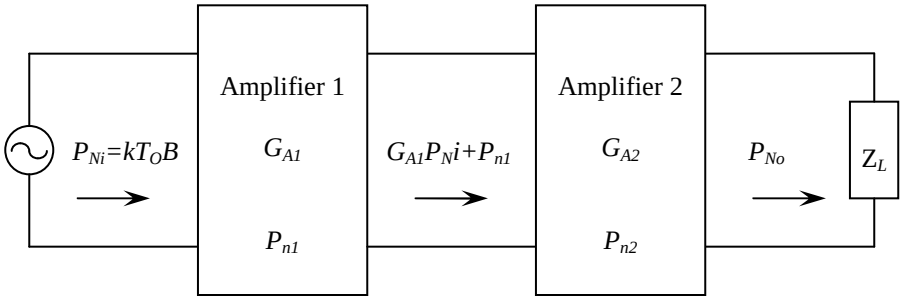


Figure 3. 36. Noise figure model of two-stage amplifier

P_{Ni} is the available input noise power, G_{A1} and G_{A2} are the available power gain of each stage, and P_{n1} and P_{n2} represent the noise power appearing at the output of amplifiers 1 and 2, respectively, due to the internal amplifier noise.

The total available noise figure at the output is given by Equation 3.40 [34].

$$P_{No} = G_{A2}(G_{A1}P_{Ni} + P_{n1}) + P_{n2} \tag{3.38}$$

$$F = \frac{P_{No}}{P_{Ni}G_{A1}G_{A2}} = 1 + \frac{P_{n1}}{P_{Ni}G_{A1}} + \frac{P_{n2}}{P_{Ni}G_{A1}G_{A2}} \tag{3.39}$$

$$F = F_1 + \frac{F_2 - 1}{G_{A1}} \tag{3.40}$$

Equation 3.40 shows that the NF of two stages cascaded amplifier depends most critically on the noise figure of the first stage (F_1) and that the contribution of the second stage (F_2) is reduced by the gain (G_{A1}) of the first stage.

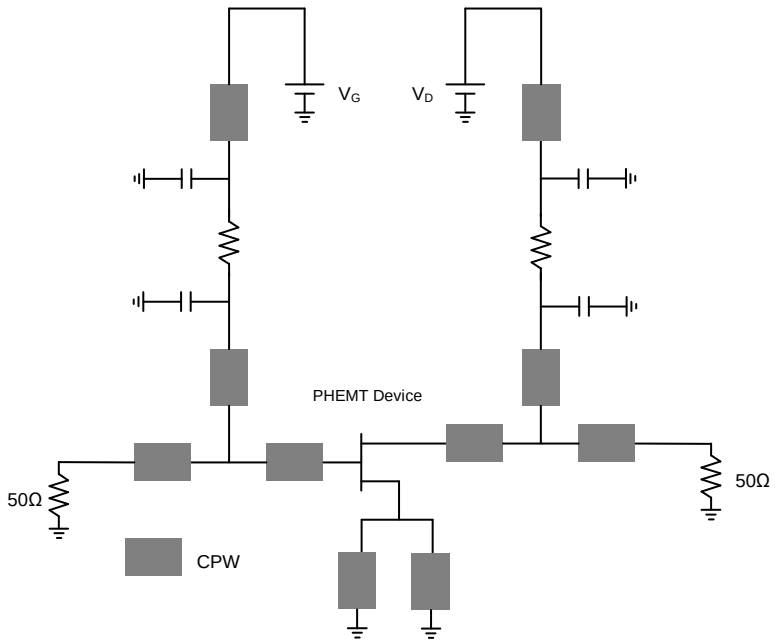


Figure 3. 37. Schematic of amplifier with source inductance

Figure 3.37 shows a schematic for a source feedback, reactively-matched amplifier. This schematic also has a resistance in the bias circuit to restrict low frequency oscillation and increase stability. As previously mentioned, the source inductor was formed by inserting two transmission lines between source electrodes of the PHEMT and ground plane. As shown in Figure 3.37, the short-circuit stub for matching also functions as biasing circuit in this schematic. It includes decoupling capacitor that enable the application of DC bias and resistor to suppress low frequency oscillation. As a stand-alone element, the bias line would have to be a quarter-wavelength long, which would be too large in most case. So the technique, which realizes the matching and biasing circuits by a stub and therefore greatly reduces the chip size, is quite attractive in MMIC design [35].

3.9 Envelope Detector

Detectors are used to provide an output dc signal that contains the 'information' of the input RF signal, that is, the amplitude or amplitude variation of the signal. The simplest form of envelope detector is the diode detector which is shown in Figure 3.38. A diode detector is simply a diode between the input and output of a circuit, connected to a resistor and capacitor in parallel from the output of the circuit to the ground.

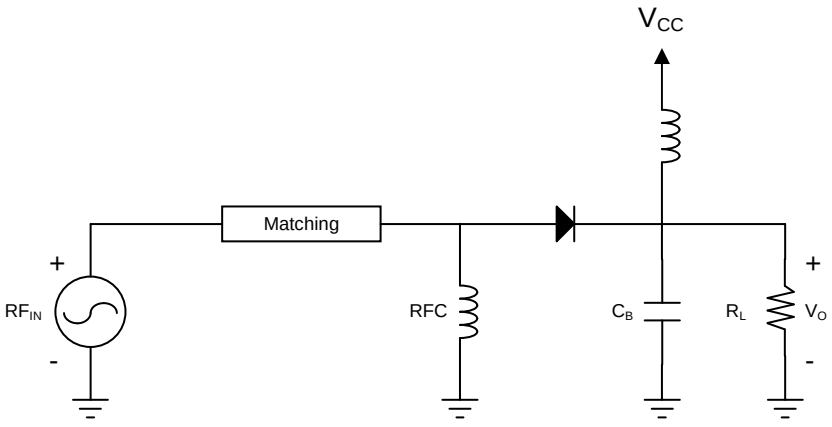


Figure 3. 38. Typical schematic of diode detector

For targeting a circuit topology which is simple and has zero power consumption, a Schottky diode has been mostly used for detector circuit with zero bias. Despite these advantages, the zero bias Schottky diode detector circuit suffers from lower sensitivity. Thus, other techniques with high sensitivity, low-cost and low-power consumption at the same time is required to achieve a significant improvement of detector sensitivity.

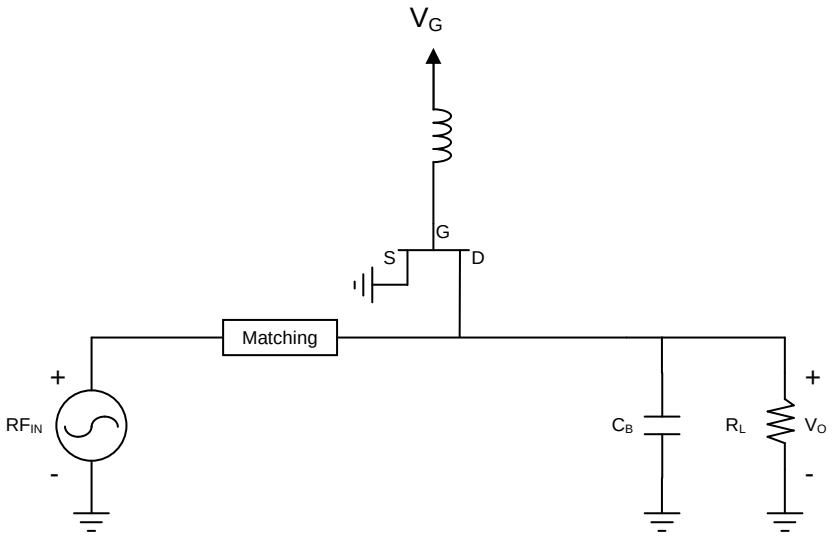


Figure 3. 39. Schematic of FET-based detector using pinch-off operation

A novel low-cost and low-power detector circuit using a single cold-HEMT is designed for demodulation, which will easily meet the aforementioned constraints. Figure 3.39 represents the circuit of the HEMT-based detector. The ASK or OOK signal is rectified at the nonlinear channel resistance of the transistor [36]. The detection does not make use of the Schottky contact of the PHEMT, which is inversely biased. The negative gate voltage level can be used to optimize the performance of the detector. Since there is no direct biasing current, there is no power consumption and no 1/*f* noise generated. This detector also has high-speed data transfer by the fast switching speed of PHEMT device.

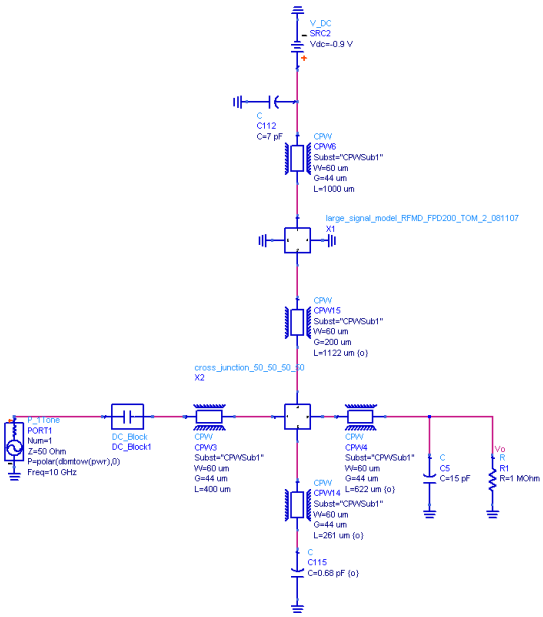


Figure 3. 40. Schematic of PHEMT detector

The semiconductor device employed in the detector circuits is the FPD-200 PHEMT. S-parameter measurements were first performed to determine the input impedance *Z1* of device in demodulation state. The circuits were designed for 10GHz band operation and integrated on GaAs substrate with CPW transmission line, MIM SiN capacitor and NiCr resistor for matching and bias circuits. The parallel load capacitor and resistor combination provides the function of low-pass filtering out the carrier signal and hence developing voltage output for original data. Figure 3.40 shows an ADS schematic of a PHEMT detector designed as outlined above.

Figure 3.41 shows a simulated input matching at operating frequency of 10GHz. A Harmonic Balance (HB) simulation was carried out at 10GHz to find the output voltage (V_O) vs. input power (P_{IN}) relationship using ADS TOM3 model which is shown in the previous section.

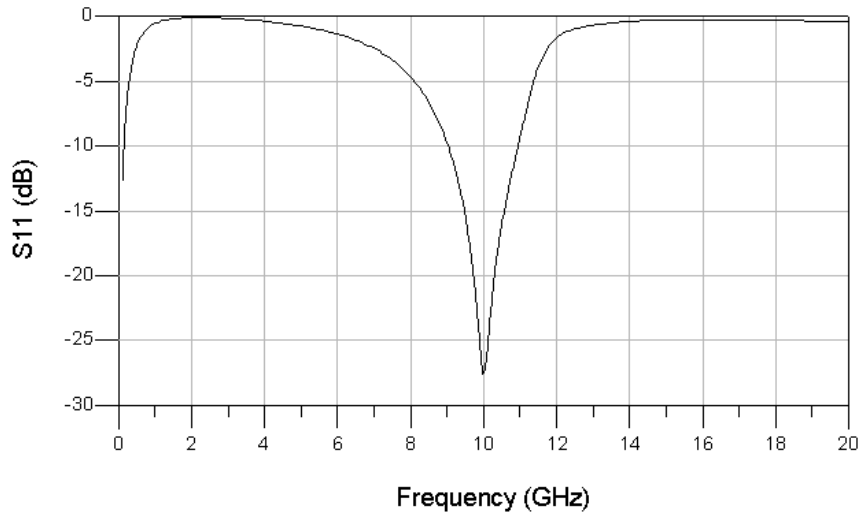


Figure 3. 41. Simulated input matching of detector

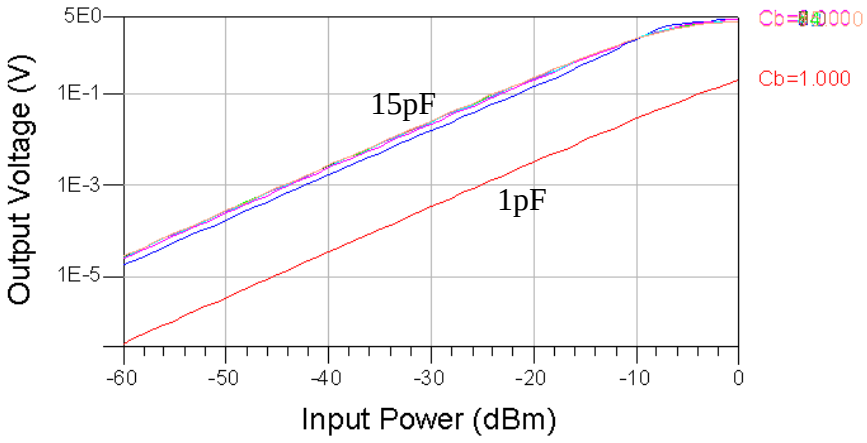


Figure 3. 42. Input power vs. output voltage with variation of capacitance (C_B)

This is shown in Figure 3.42 for different load capacitors (1pF to 15pF, in 1pF steps). In case of capacitor of 15pF, Figure 3.43 shows the simulated output voltage vs. input power with variation of load resistor (1kΩ to 1000kΩ, in 10kΩ steps). It can be seen that at -30dBm the output voltage increases with increasing load capacitor but at higher input powers the output voltages converge.

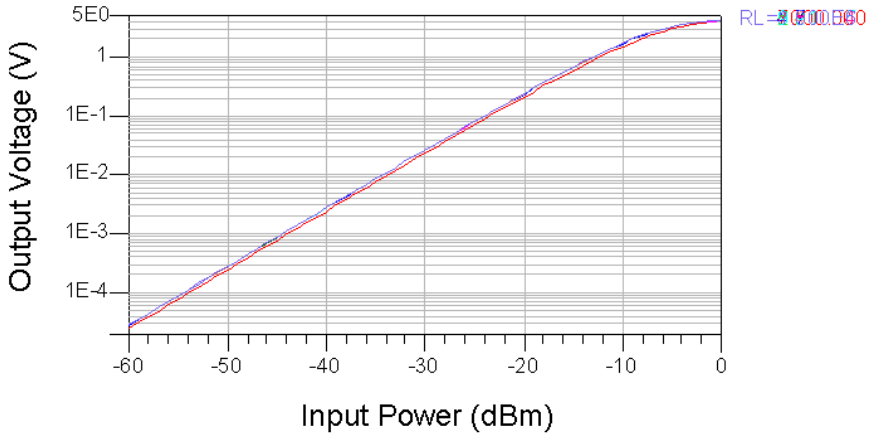


Figure 3. 43. Output voltage vs. input power with variation of load resistor value

If the resistor and capacitor are correctly chosen, the output of the envelope detector should approximate a voltage-shifted of the original (baseband) signal. An envelope detector can also be constructed to use a precision rectifier feeding into a low-pass filter, but it restrict data rate with its cut-off frequency. Consequently, they must be a trade-off.

3.10 SPDT Switch

The single pole double throw (SPDT) switch is an essential element for separating transmitter and receiver signal from the antenna diversity. Traditionally, PIN diode switches have been used for high speed and power applications, but for low power applications, PIN diode switches have been increasingly replaced by GaAs FET-based monolithic switches. The FET-based switch is a three-terminal device in which the gate bias voltage V_g controls the states of the switch. The FET acts as voltage controlled resistor in which the gate bias controls the drain-to-source resistance in the channel. The intrinsic gate-to-source and drain-to-gate capacitances and device parasitics limit the performance of the FET switch at higher frequencies.

In a typical switching mode a high impedance state is produced when a negative bias larger in magnitude than the pinch-off voltage ($|V_g| \geq |V_p|$) of the FET is applied across the

gate terminal. When a zero bias gate voltage is applied across the gate terminal, the FET switch is in a low impedance state. It is important to note that in either state virtually no DC power is required by the FET switch itself. Thus, for all practical purpose, from a power consumption point of view, these FET-based switches can be considered as passive devices [37]-[38]. Figure 3.44 shows the circuit model of a FET switch.

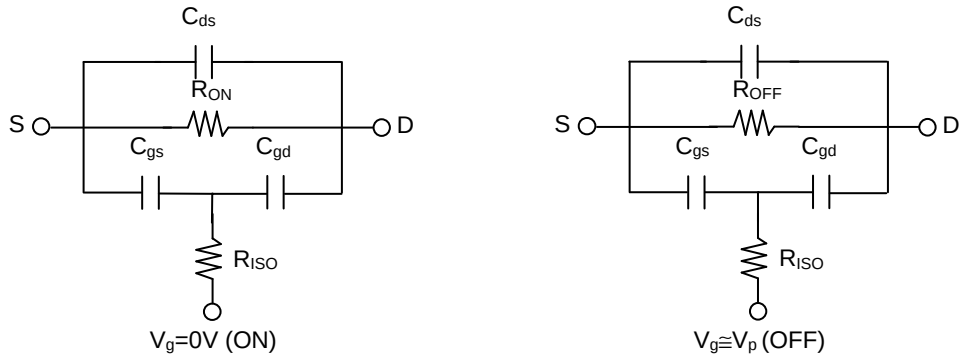


Figure 3. 44. Simplified equivalent circuits of FET switch for ON and OFF states

From equivalent device model, a simple circuit is extracted for each state of switch with zero bias and pinch-off voltage. Under the zero bias condition on gate terminal the channel region is virtually open except for the zero field depletion layer thickness. Thus, for current level less than the saturated channel current, I_{dss}, the FET can be modelled as a linear resistor, R_{ON}. When a negative voltage V_g is applied at the gate terminal such that $|V_g| \geq |V_p|$, where V_p is pinch-off voltage, the channel region is completely depleted of free charge carriers. Under these conditions the FET can be modelled by series and parallel combinations of resistors (R_{OFF}) and capacitors (C_{ds}). The gate terminal is isolated from the signal path through C_{gd}, C_{gs} and R_{ISO}. This method is virtually no power consumption since the current of gate terminal is as small as that can be negligible.

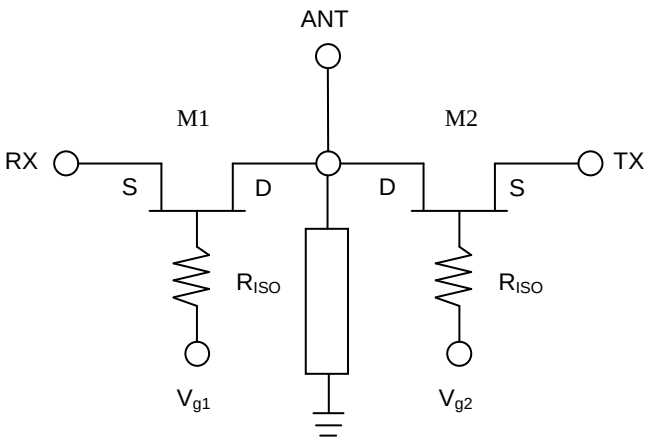


Figure 3. 45. Schematic of SPDT switch using two PHEMTs

A SPDT switch can be implemented from two PHEMTs, M1 and M2 as shown in Figure 3.45. In the two switch states the gate junction is either reverse biased or is biased at zero gate voltage. In both these states the gate draws negligible current which greatly simplifies the control circuit design requirements. In the off-state of the M2 HEMT, the gate voltage V_{g1} is zero and gate voltage V_{g2} is at pinch off, the antenna signal is passed to the receive amplifier since there is a short circuit between the antenna and the amplifier and an open circuit between the oscillator output and the antenna. In the on-state of the M2 HEMT, the gate voltage V_{g2} is zero and gate voltage V_{g1} is at pinch-off, the oscillator output is passed to the antenna. A short circuit stub between each drain of two PHEMT devices has a narrow band performance with a quarter wavelengths at the operating frequency, therefore, a SPDT switch with a short circuit stub results in a significant improvement in narrow band performance at the operating frequency. Figure 3.46 shows the simulated insertion loss and isolation performance of PHEMT SPDT switch.

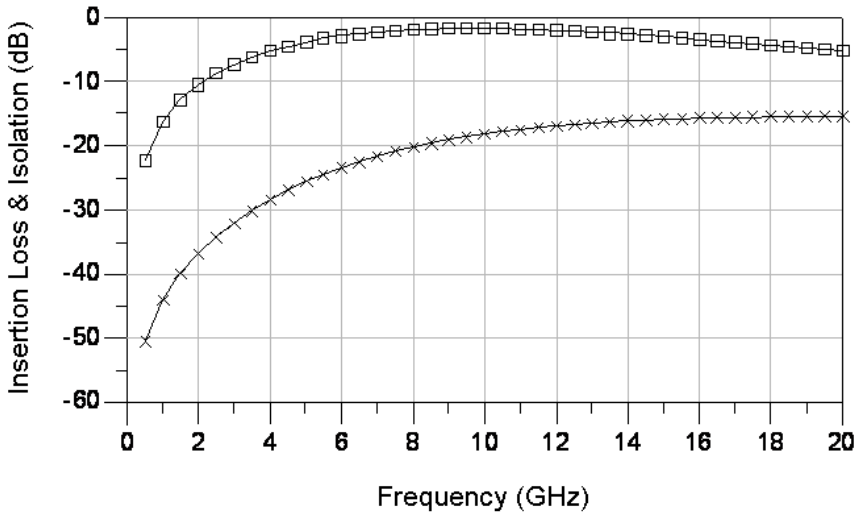


Figure 3. 46. The simulated insertion loss (□) and isolation (×) performance of SPDT switch

3.11 Conclusions

This chapter has described the MMIC process for passive circuit such as MIM SiN capacitor and spiral inductor, and discussed the function and design method of four important circuits in a whole transceiver.

The typical performance data of MIM SiN series and shunt capacitors have been presented. A good agreement between measured and modelled S-parameters has been shown for shunt and series capacitors. MIM SiN series and shunt capacitors were used for

bypass and dc block in circuits. At low frequencies, the spiral inductor is a popular component to use for RF choke and matching networks instead of a long length of transmission line. The typical performance data and inductance of different geometry spiral inductors have been presented. A good agreement between measured and modelled S-parameters has been shown. The library of passive components has been used in circuit designs.

Oscillator has been designed with considerations to implement a simple structure and reduction of dc power consumption. There are two types of oscillator circuit, namely the feedback and negative resistance oscillator. They differ from each other mainly in their principles of operation, circuit topologies and phase noise performances. In this chapter, negative resistance oscillator is used to design oscillator due to its simple design technique and easily predicted performance. A design procedure for negative resistance oscillators using the concept of two-port oscillator has been detailed [25], [32].

Amplifier has been designed to have an unconditionally stable using source feedback inductance and has also achieved a good input and output matching, thus it can be well integrated with other circuits to implement fully integrated radio transceiver with a good performance.

Envelope detectors have also been discussed and designed in this chapter. A passive PHEMT detector using pinch-off operation has been designed for low power consumption and higher sensitivity. The meander structure transmission line and shunt capacitor are used to realize the matching circuit and it significantly reduces the size of envelope detector with ultra-low dc power consumption and also a good sensitivity. The load resistor and capacitor of detector are analyzed and discussed to choose their optimal value for more precision rectify.

In this chapter, a SPDT switch using two transistors is also shown and detailed for low insertion loss and high isolation performance. Using gate voltage of 0V and pinch-off, the transistor exhibits an effective short circuit and open circuit with dominant resistance and capacitance between source and drain terminals, respectively. As a result, the passive HEMT switch achieved ultra-low power consumption, low insertion loss and high isolation. This switch also achieved a good return loss using short-circuit stubs between two transistors. The power consumption is negligible since the gate draws only a current of less than 10μA which greatly simplifies the control circuits.

In conclusion, the radio transceiver with OOK modulation scheme consists of one switched oscillator, amplifier, envelope detector and SPDT switch. Oscillator must have a simple structure and low power consumption and be easily predicted its performance such as output power level and optimal operating frequency. Amplifier must have unconditional

stability and a good matching performance with a moderate gain and low power consumption. Envelope detector must have a high sensitivity while retaining low power consumption. SPDT switch must have a good insertion loss and isolation with low power consumption to separate transmitter and receiver signals in whole radio transceiver and effectively share a single antenna.

Chapter 4

10GHz Quasi-MMIC Radio Transceiver

4.1 Introduction

As mentioned in Chapter 3, the direct modulation/demodulation transceiver uses a switched oscillator as transmit modulator and signal generator. The transceiver also uses a moderate gain amplifier and an envelope detector as a simple receiver with ultra-low power consumption, good noise and dynamic range. In the direct modulation transmitter, the data rate is determined by the oscillator's start-up time. If the start-up time constitutes 10% of the bit period, the oscillator is able to support data rates up to 80 kbps with on-off keying modulation. To achieve a higher data rate, the start-up current can be increased [39].

The modulated signal of switched oscillator is propagated by antenna and then the receiver which consists of amplifier and detector generates a demodulated signal as shown in Figure 4.1.

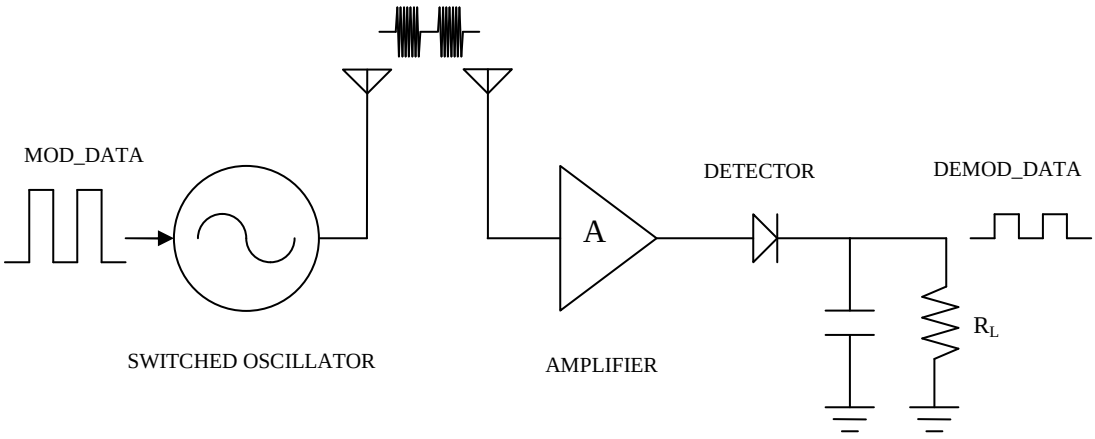


Figure 4. 1. Block diagram of transceiver for OOK modulation scheme

The signal received from an antenna is boosted by amplifier and isolated from the transmitter by SPDT switch. The reverse isolation of the amplifier between antenna and envelope detector also helps to avoid re-radiation. Figure 4.2 illustrates the operation of envelope detection. Most methods for envelope recovery from ASK or OOK signals rely upon some form of peak detection followed by a low-pass filter to remove the carrier and provide smoothing. Typically this is rectification followed by an RC network. When

carrier frequencies are large relative to modulation frequencies this approach presents no problem.

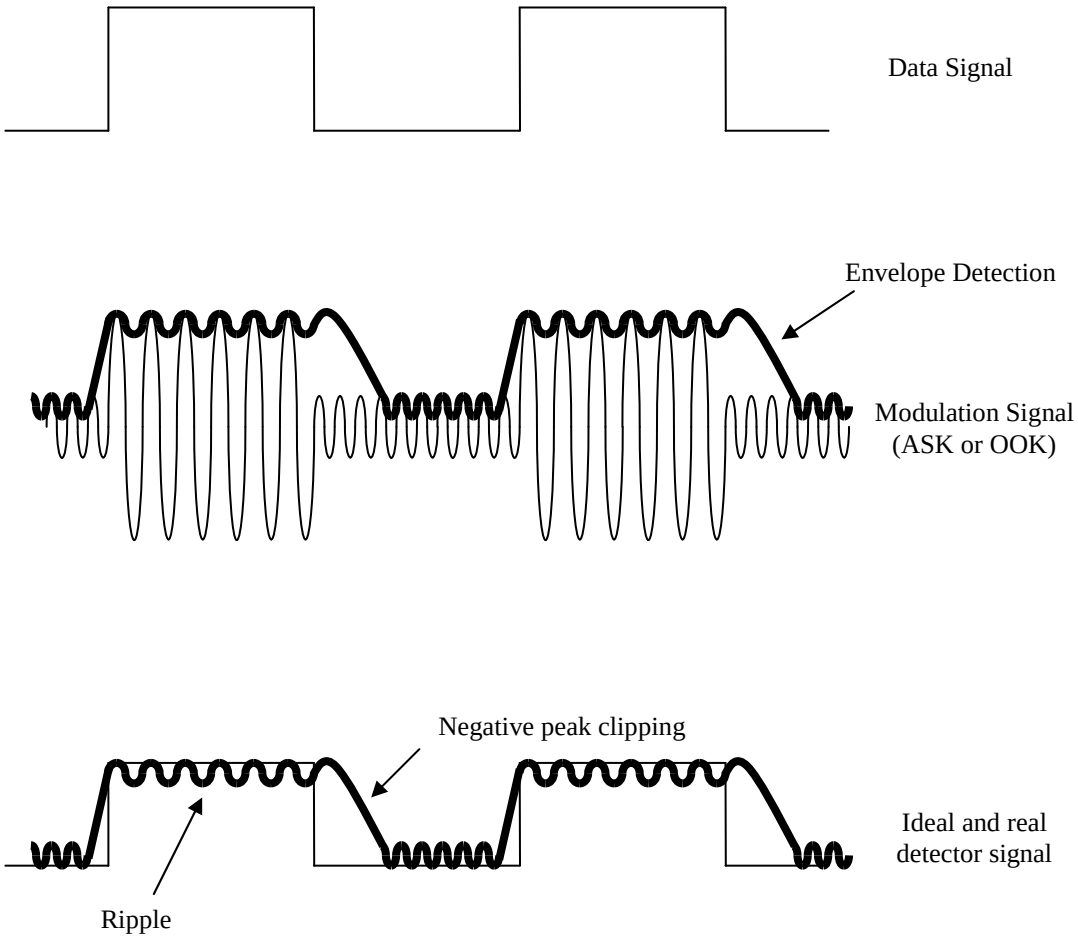


Figure 4. 2. Waveform of demodulated OOK signal

OOK detector or demodulator is called linear envelope detector because the output is proportional to the input envelope. Unfortunately the devices (diode or transistor) used can introduce appreciable level of harmonic distortion unless modulation levels are kept low. As a result theses detectors are unable to provide a suitable signal for high quality application. Thus, it is difficult to recover an accurate representation of the original modulating waveform. The circuit also suffers from the problem known as ripple and negative peak clipping. The ripple effect happens because the capacitor will be discharged a small amount in between successive peaks of the input wave. The time constant which is determined by the RC network is a small value for avoiding negative peak clipping and a large value for minimizing ripple effect. Thus in practice one should choose a value to minimize the signal distortions caused by these effects.

4.2 OOK Transmitter

4.2.1 Switched Oscillator Model

As shown in Figure 4.1, the oscillator in the proposed OOK transmitter is switched on and off when transmitting a “1” or “0” respectively. The data rate depends on how fast the oscillator’s output can be switched on and off. The decay to ‘0’ can be produced by simultaneously supplying pinch-off voltage in gate and drain current is off. On the other hand, the build-up to ‘1’ is limited by the start-up time of oscillator and can be produced by supplying operation voltage in gate and drain current is on. Figure 4.3 shows the schematic and equivalent circuit of a Colpitts oscillator where the transistor is modelled by a sinusoidal current source at carrier frequency [40], whose envelope is a step function.

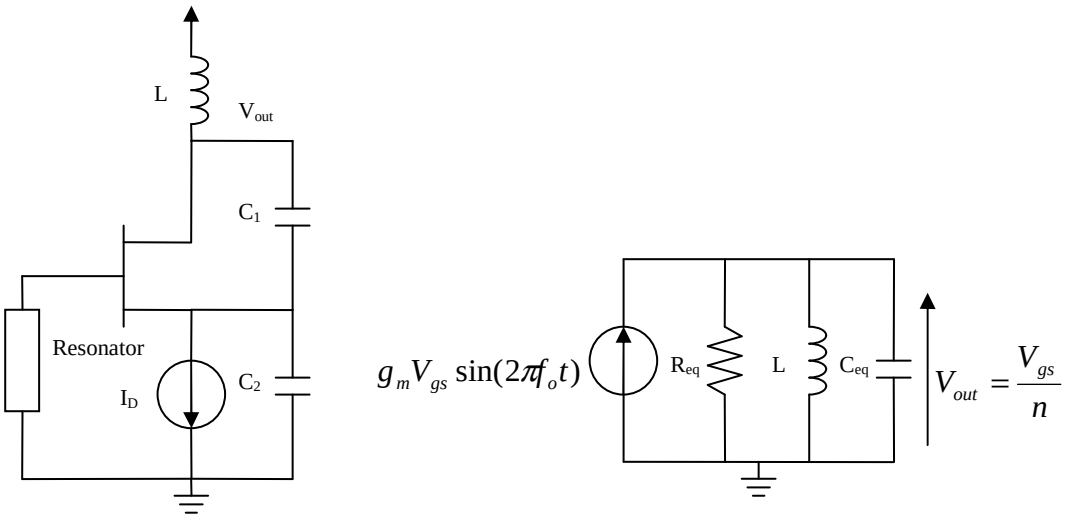


Figure 4. 3. Colpitts oscillator and equivalent circuit

The equivalent tank resistance and capacitance can be expressed as below, respectively.

$$R_{eq} = \frac{1}{n^2[g_m + g_{mbs} + g_{ds}]} \tag{4.1}$$

where

$$n = \frac{C_1}{C_1 + C_2} \tag{4.2}$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \tag{4.3}$$

When the oscillator is switched on (bias current is switched in), oscillator starts building up. An analysis of the equivalent circuit in Figure 4.3, yields,

$$V_{out}(t) = K_1(1 - e^{-t/2R_{eq}C_{eq}})\sin(2\pi f_o t) \tag{4.4}$$

where, K_1 is the final amplitude of the oscillator output, which is proportional to the dc drain current I_D and the tank impedance at resonant frequency f_o. The time constant for the envelope is $2R_{eq}C_{eq}$, and the time taken for the envelope to rise from 10% to 90% of its final value K_1 is

$$t_r = \frac{4.4C_{eq}}{n^2[g_m + g_{mbs} + g_{ds}]} \tag{4.5}$$

According to Equation 4.5, the oscillation can start faster if g_m or n is increased, or C_{eq} is decreased. However, increasing n beyond 0.3 may cause squegging and sometimes bring the circuit to stable region due to the nonlinear parasitic from gate to source [40], while C_{eq} can only be reduced to some extent as it is limited by f_o. It seems that, increasing the g_m is a better option; however, it increases the power consumption. To reduce the start-up time without compromising much power consumption, one needs to increase the g_m only during the build-up of the oscillator.

4.2.2 Start-up Time of Switched Oscillator

As mentioned in the previous section, the switched oscillator for high data rate OOK modulation in the transmitter requires reduced start-up time and this is achieved by increasing the g_m during the build-up of the oscillator. The g_m is varied in the device by both drain and gate bias. To realize the oscillator, the FPD-200 PHEMT device was used in a simple topology that creates a negative resistance.

To confirm the dependency of start-up time with variation of g_m, we used the extracted non-linear models of the FPD-200 PHEMT device. The start-up time is verified for different values of g_m (or bias condition) using Agilent ADS simulation. Figure 4.4 shows schematic of the switched oscillator.

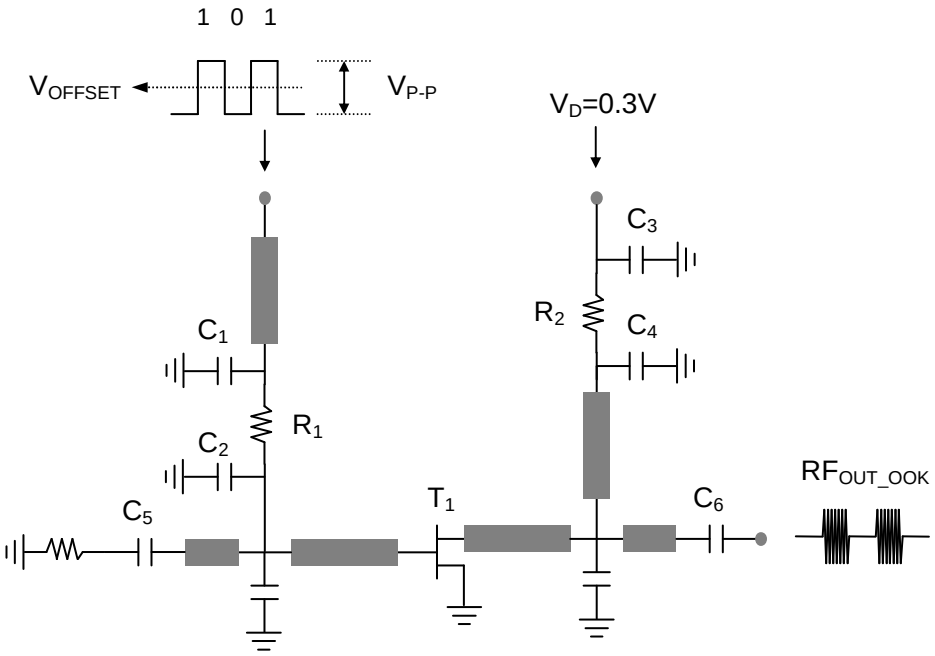


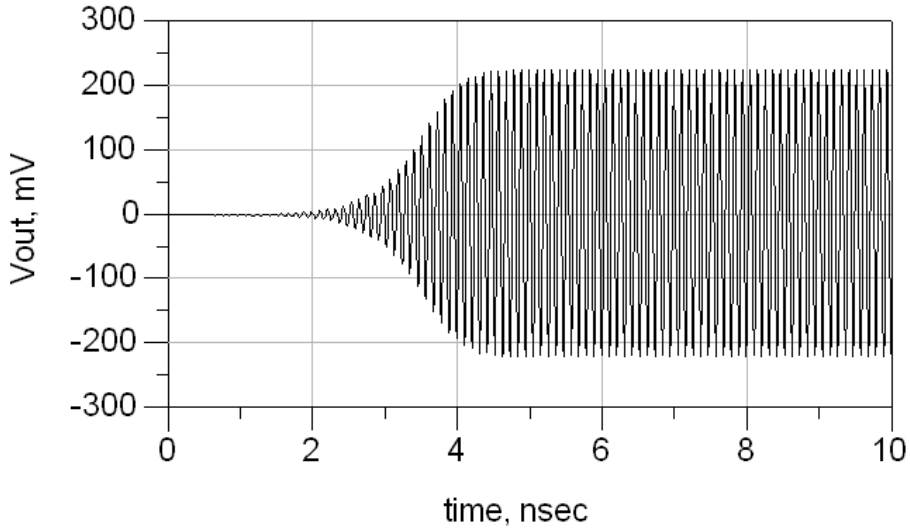
Figure 4. 4. Schematic of switched oscillator for OOK modulation

The oscillator is switched on and off when data waveform is '1' and '0', respectively to generate an OOK modulated signal. Figure 4.5 shows start-up time of oscillator circuit using non-linear model and ADS simulation tool. Different start-up times are achieved with different g_m values as shown in Figure 4.5. Table 4.1 shows the summary of g_m versus start-up time of switched oscillator.

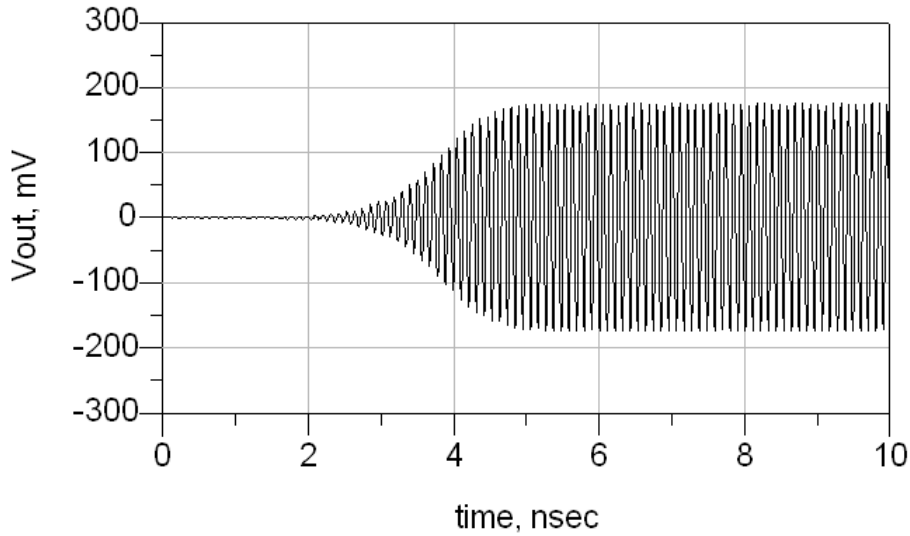
Drain Voltage (V)	Drain Current (mA)	g_m (mS/mm)	Start-up time (ns)
0.5	1.5	153	4.5
0.4	1.3	142	5.0
0.3	1.1	129	6.5

Table 4. 1. Summary of g_m versus start-up time

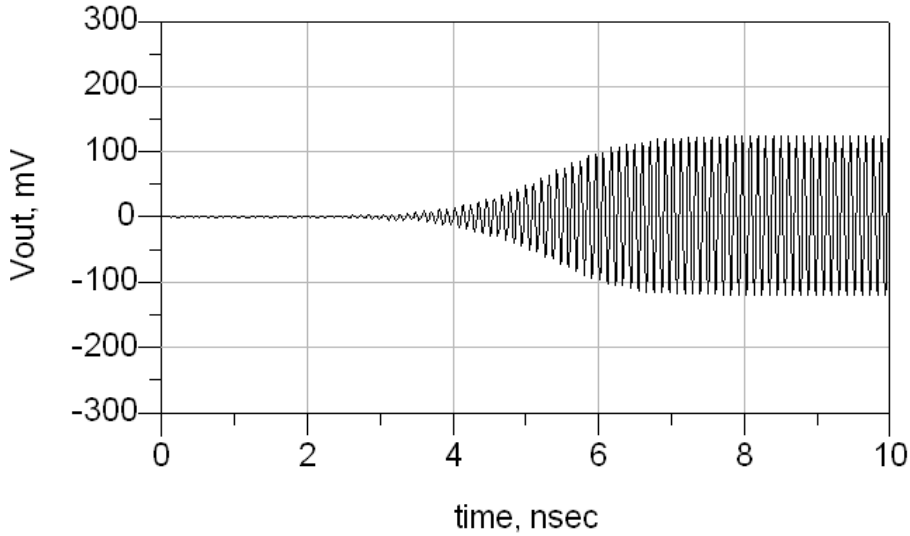
If the start-up time constitutes 10% of the bit period, the oscillator is able to support data rates up to 80 kbps with on-off keying modulation [39]. Thus, the designed oscillator is able to support data rates of more than 100 kbps even if bias condition with power consumption of less than 400μW. Using bias condition with power consumption as low as 400μW or 500μW, the switched oscillator is capable of generating OOK modulation for ultra-low power consumption transceiver.



(a)



(b)



(c)

Figure 4. 5. The start-up time with different g_m conditions (a) 153 mS/mm, (b) 142 mS/mm, and (c) 129 mS/mm

4.3 OOK Receiver

4.3.1 Shockley's Model

Figure 4.6 shows the principal circuit of the power detector. The field effect transistor (FET) detector exploits the non-linear channel conductance as a function of the drain voltage. Thus, the rectification is not based on the use of the transistor as a diode, as one might expect.

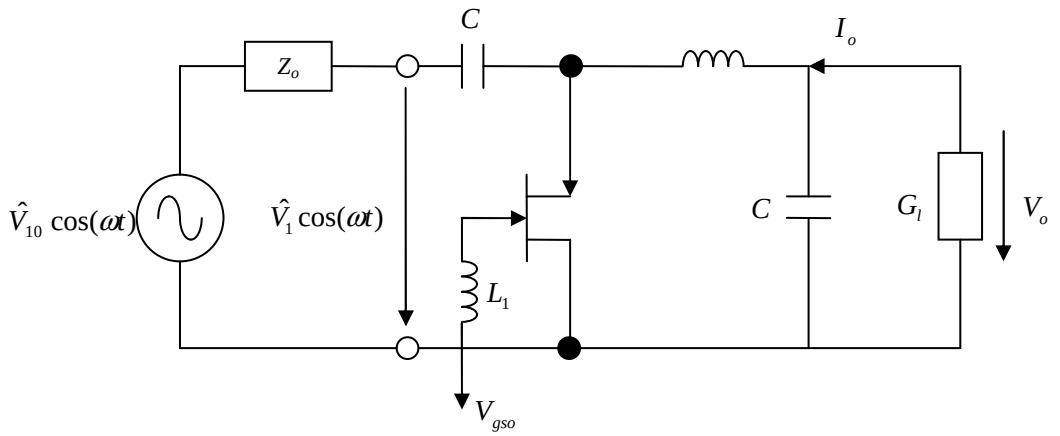


Figure 4. 6. Principal circuit of FET-based envelope detector

This principle of power detection was first published by Krekels *et al*. [36], who described its performance in a qualitative manner and examined a variety of circuit configurations, but did not put forward an analytical approach. The following analytical approach lead to a simple expression for the conversion factor of the FET-based detector and its dependence on the circuit parameters.

The FET detector does not make use of a direct biasing current. Owing to this passive state, there is no generation of 1/*f* noise and no hot-carrier effects to be considered over a large range of input power. Hence, the application of Shockley's model to a passive GaAs device promises reliable predictions of the performance of the device, unlike the application to an active device.

Shockley's model [41] formulates an analytical expression for the drain current I_d as a function of the drain-to-source and gate-to-source voltages V_{ds} and V_{gs}.

Using the normalized voltages

$$v_d = \frac{V_c - V_{gs} + V_{ds}}{V_P} \tag{4.6}$$

and

$$v_g = \frac{V_c - V_{gs}}{V_P} \tag{4.7}$$

with the contact voltage V_c of the Schottky barrier and the pinch-off voltage V_p of the transistor, V_c and V_p both being positive constants, the drain current can be written as

$$I_d = G_o V_P \cdot (v_d - \frac{2}{3} v_d^{3/2} - v_g + \frac{2}{3} v_g^{3/2}) \tag{4.8}$$

where G_o denotes the channel conductance in the absence of depletion of carriers, *i.e.* for $V_{gs} = V_{gd} = V_c$.

4.3.2 Conversion Factor

The sinusoidal RF voltage drop $\hat{V}_1 \cos(\omega \cdot t)$ and the rectified direct voltage V_o are separated by means of high-pass and low-pass elements, as seen in Figure 4.6. We define a conversion factor *CF* as

$$V_o = CF \cdot \hat{V}_1^2 \tag{4.9}$$

to describe the RF to DC signal conversion. The channel conductance is controlled by the gate bias voltage V_{gso}. With the normalized voltages

$$\hat{v}_1 = \frac{\hat{V}_1}{V_p} \quad \text{and} \quad v_o = \frac{V_o}{V_p} \tag{4.10}$$

the normalized drain voltage may then be expressed as

$$v_d = v_g + \hat{v}_1 \cos(\omega \cdot t) + v_o \tag{4.11}$$

which after insertion in Equation 4.8 leads to

$$I_d(t) = G_o V_p \cdot \left(\hat{v}_1 \cos(\omega \cdot t) + v_o - \underbrace{\frac{2}{3}(v_g + \hat{v}_1 \cos(\omega \cdot t) + v_o)^{3/2}}_{f(x)} + \frac{2}{3} v_g{}^{3/2} \right) \quad (4.12)$$

To determine a first-order approximation of its mean value $I_o = \overline{I_d(t)}$, the power series expansion of the function $f(x) = \frac{2}{3} x^{3/2}$ at x_o is useful:

$$f(x) = \frac{2}{3} x_o{}^{3/2} + x_o{}^{1/2} \cdot (x - x_o) + \frac{1}{4} x_o{}^{-1/2} \cdot (x - x_o)^2 - \ldots \quad (4.13)$$

The point of expansion x_o has to be chosen as v_g in order to enable cancellation of the term $v_g{}^{3/2}$ in Equation 4.12 to obtain a linear law for I_o as a function of the input power $\hat{v}_1{}^2$. Consequently, we have

$$x - x_o = \hat{v}_1 \cos(\omega \cdot t) + v_o \quad (4.14)$$

and the mean value of $f(x)$ becomes

$$\overline{f(x)} \approx \frac{2}{3} v_g^{3/2} + v_g^{1/2} v_o + \frac{1}{4} v_g^{-1/2} \cdot (\frac{1}{2} \hat{v}_1^2 + v_o^2) \quad (4.15)$$

which is valid for small RF magnitudes $\hat{V}_1$.

Under the assumption that v_o^2 is small compare to $\hat{v}_1^2$, the insertion of Equation 4.15 in Equation 4.12 yields

$$I_o = G_o V_p \cdot \left(v_o \cdot (1 - \sqrt{v_g}) - \frac{1}{8} \frac{\hat{v}_1^2}{\sqrt{v_g}} \right) \quad (4.16)$$

I_o can be replaced by use of the load conductance G_l

$$I_o = -V_o G_l \quad (4.17)$$

which finally leads to a square-law relation between the RF voltage $\hat{V}_1$ and the detector output voltage V_o:

$$V_o = \frac{1}{8V_p\sqrt{v_g \cdot (1+\frac{G_l}{G_o}-\sqrt{v_g})}} \cdot \hat{V}_1^2 \tag{4.18}$$

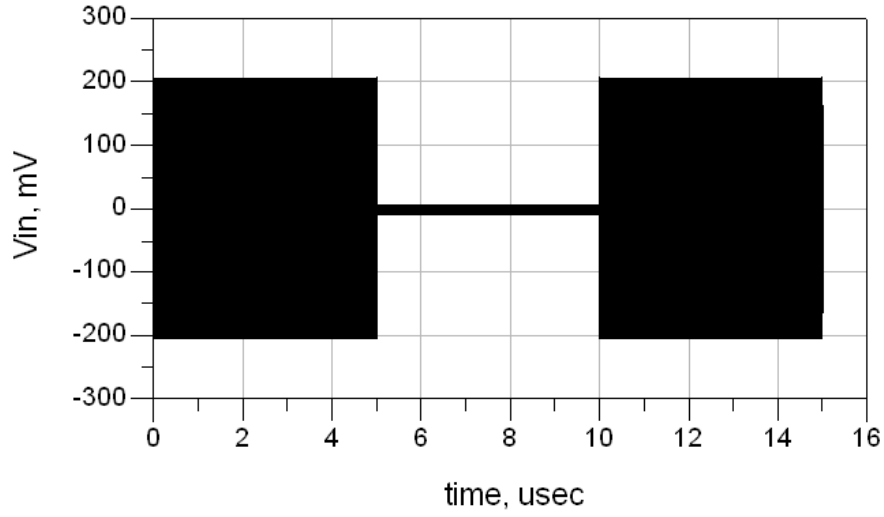
In practice, this relation is exact if $\hat{V}_1$ is small enough. In a large-signal simulation of the FET detector a non-linear FET model can be used which is embedded in an arbitrary linear circuit. The non-linear power detection is then precisely taken into account by measuring the RF magnitude $\hat{V}_1$ across the inner channel resistance of the FET and by applying Equation 4.18. As such, G_l represents the DC conductance of the entire DC path excluding the channel conductance.

The conversion performance of the FET detector can be maximized through the variation of two parameters, namely the gate bias V_{gso} and the load resistor $1/G_l$. This can easily be checked with the aid of Equation 4.18 [42]. A maximum output voltage is obtained for voltages V_{gso} slightly superior to the pinch-off voltage $V_{gs} = V_c - V_p$ and for the load matched to the channel conductance $G_o(1-\sqrt{v_g})$.

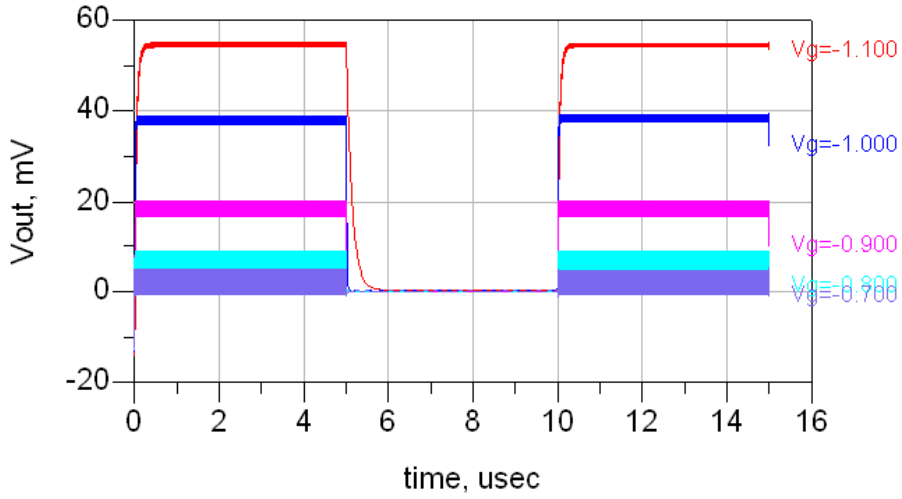
As an alternative, the bias point V_{gso} can be established such that the channel conductance is matched to the RF source, in order to avoid further matching networks. In terms of the demodulator realization we used gate bias voltage $V_{gso} = V_p$ and a load which provided the highest possible output voltage. The model proposed by Equation 4.18 has been verified by measurements which will be presented in Section 4.5.

4.3.3 Signal Detection

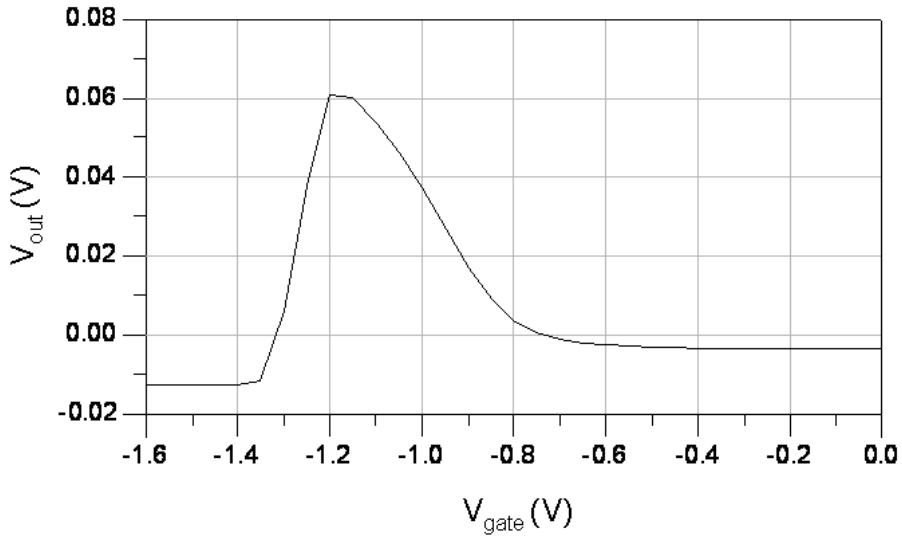
As mentioned in the previous section, the output voltage of detected signal is dependent on V_{gso} which is used in the detector bias networks and also the load. The output voltage amplitude of detected signal is particularly dependent on the gate voltage of device because the channel conductance is matched to the RF source to obtain the highest output voltage.



(a)



(b)



(c)

Figure 4. 7. The variation of output voltage versus the variation of gate voltage (a) input modulated signal (b) demodulated output signals, and (c) output voltage versus gate bias

To determine the relationship between gate voltage and the detector output voltage, a non-linear model of the FPD-200 PHEMT device was used. The model parameters shown in Tables 3.3 and 3.4 were used. Using this non-linear model, the detector was simulated in ADS to verify the variation of output voltage for different gate voltages applied. Figure 4.7 shows the different output voltage levels when different gate voltages are applied to the gate terminal of device.

For the simulation, a modulation signal with data frequency of 100 kHz and amplitude of 0.4V is applied to the input port of the detector. At gate voltage of -1.1V, the detector shows the highest output amplitude but the waveform becomes distorted with negative peak clipping. Thus, the gate voltage of detector must be chosen to achieve signal-to-noise ratio (SNR) of approximately 16dB for a 10^{-3} BER and output voltage level of greater than $1mV_{p-p}$ for low power baseband processing. For these reasons, the gate voltage of -0.9V is chosen to obtain a good SNR and output voltage level that can be processed by low power baseband.

4.4 Implementation of Radio Building Blocks

The circuit building blocks were implemented on GaAs substrate with CPW transmission lines, MIM SiN capacitor, NiCr thin film resistor, and gold wire bonds for air-bridges. The active device was attached to the substrate using silver epoxy and wire bonded out.

4.4.1 Oscillator

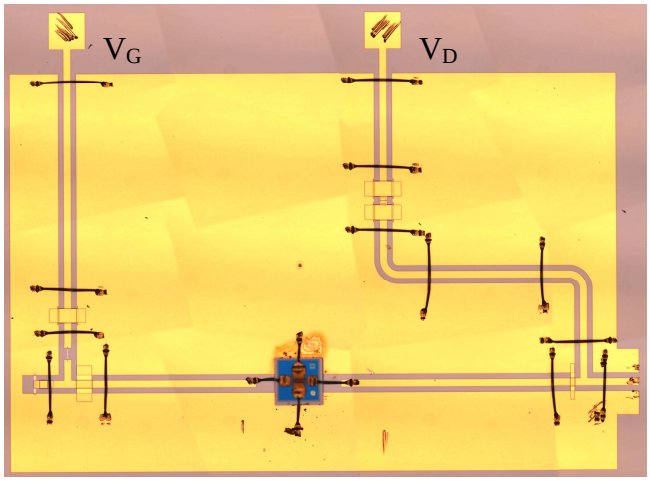


Figure 4. 8. Microphotograph of quasi-MMIC switched oscillator on GaAs substrate

Figure 4.8 shows the microphotograph of oscillator which was integrated using wire bond process between device and substrate. Figure 4.9 shows measured spectral responses of oscillator for its fundamental and 2nd harmonic signal. This response shows the harmonic rejection of -29.7dBc and fundamental signal output power of -10.4dBm at 10GHz.

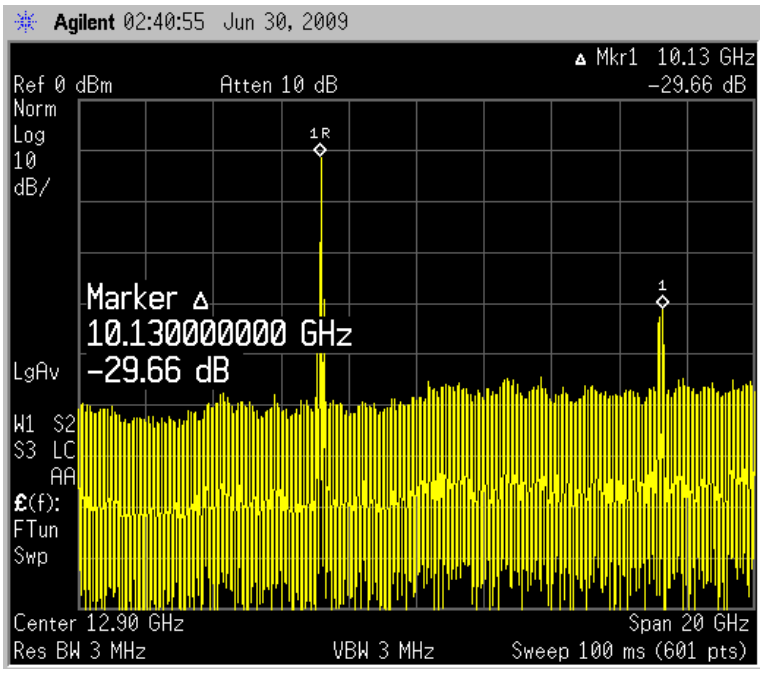


Figure 4. 9. Spectral responses of the fabricated oscillator

4.4.2 Amplifier

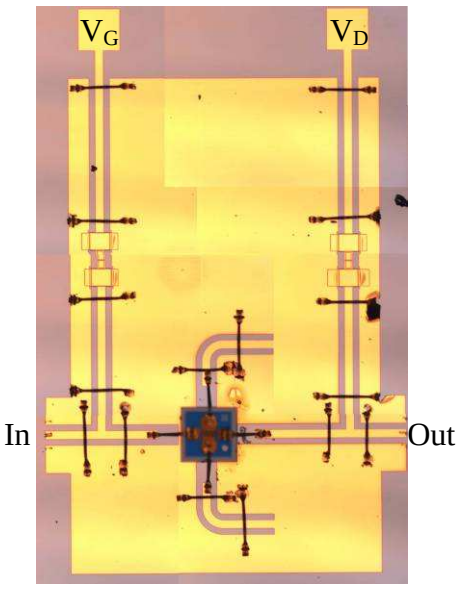


Figure 4. 10. Microphotograph of quasi-MMIC amplifier on GaAs substrate

Figure 4.10 shows a microphotograph of the fabricated 10GHz quasi-MMIC low noise amplifier. The source inductors formed by inserting CPW line were simulated using Ansoft HFSS and extracted S-parameters using Agilent ADS. Figure 4.11 shows the simulated and measured frequency responses of the quasi-MMIC amplifier. Measured responses show a gain of 6dB, return loss of less than -10dB and power consumption of less than 420μW. These results are suitable responses for amplifier and good agreement between simulation and measurement results was obtained.

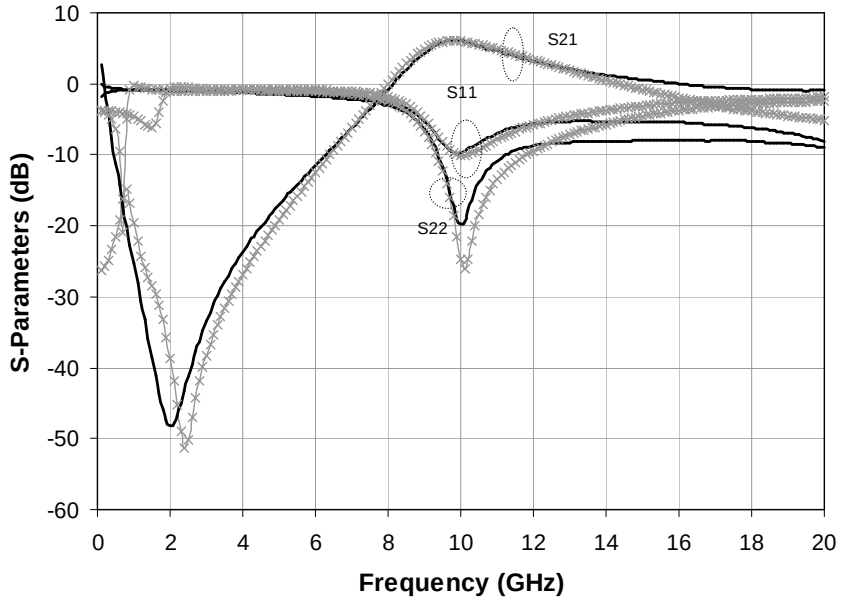


Figure 4. 11. Simulated and measured responses of amplifier: simulation (grey and ×) and measurement (black)

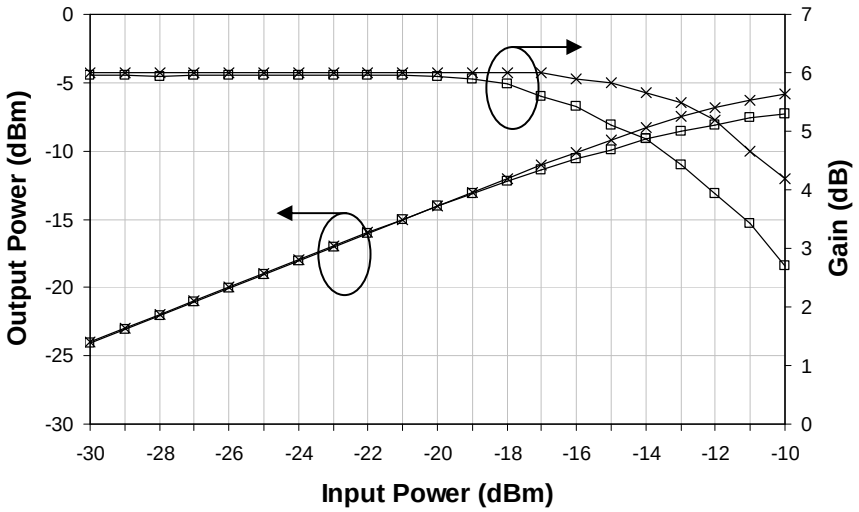


Figure 4. 12. P_{1dB} characteristic at 10GHz V_{ds}=0.3V, I_{ds}=1.4mA: simulation (×), measurement (□)

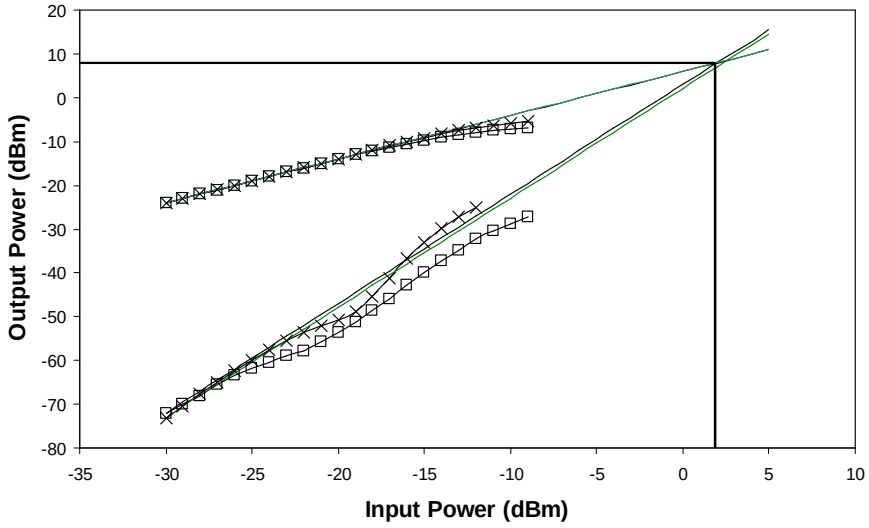


Figure 4. 13. IP_3 characteristic at 10GHz V_{ds}=0.3V, I_{ds}=1.4mA: simulation (×), measurement (□)

Figure 4.12 shows the output power 1dB compression point to be -9.8dBm for a dc power consumption of only 420μW. The output third-order intercept point (OIP_3) characteristic of the amplifier is shown in Figure 4.13 which was measured at 10GHz using a two-tone test with 1MHz separation. The measured output IP_3 of the amplifier is +8dBm. If a sensor node is placed in the closest area to any sensor node, a large input level is applied to the amplifier and it can make a distortion in the amplifier if the amplifier has not a linear characteristic, thus it is important to measure the linear characteristic of amplifier in large input power range. From above measured results, it means that amplifier can still operate in linear area in large input level due to communication between the closest nodes.

4.4.3 Envelope Detector

The detector was optimized to obtain a good sensitivity to envelope modulation signal with reduced distortion for recovering data signal. Thus, a gate voltage was chosen to achieve a high sensitivity and reduce distortion since they have a trade-off relationship. Figure 4.14 shows a microphotograph of PHEMT detector using pinch-off operation and with optimal load capacitance and resistance. The detector was integrated on GaAs substrate with CPW lines, MIM SiN capacitors, and gold wire for air bridges. The matching circuit was also simulated using Ansoft HFSS. Figure 4.15 shows simulated and measured results of PHEMT detector and the good agreement obtained between both.

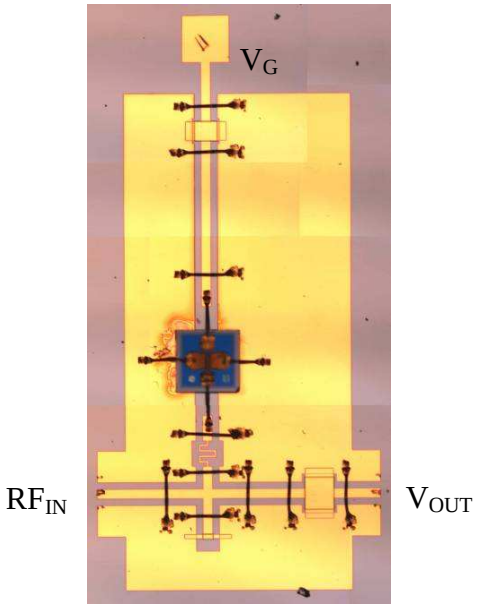


Figure 4. 14. Microphotograph of quasi-MMIC PHEMT detector on GaAs substrate

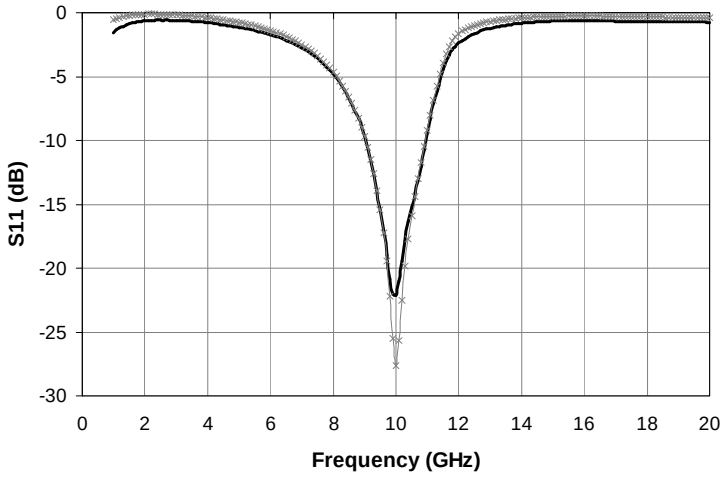


Figure 4. 15. Input matching responses of detector: simulation (grey) and measurement (black)

To measure the demodulation responses of detector, a data signal of 10 kHz was used to modulate the carrier signal and then the modulated signal was directly applied to the detector. For the modulation signal, a Wiltron 68187B synthesized sweep generator was used and the power levels of modulation signal were extended using a 16dB attenuator because of the limitation of lower power level by -20dBm. Figure 4.16 shows a test set-up for measuring the response of the detector.

The voltage levels of the demodulated signal by detector were observed using an oscilloscope for the input range of -36dBm to -14dBm. Figure 4.17 presents the dependence of the detected output voltage on the input power for the OOK demodulation. A good agreement between the simulated and the measured results was observed.

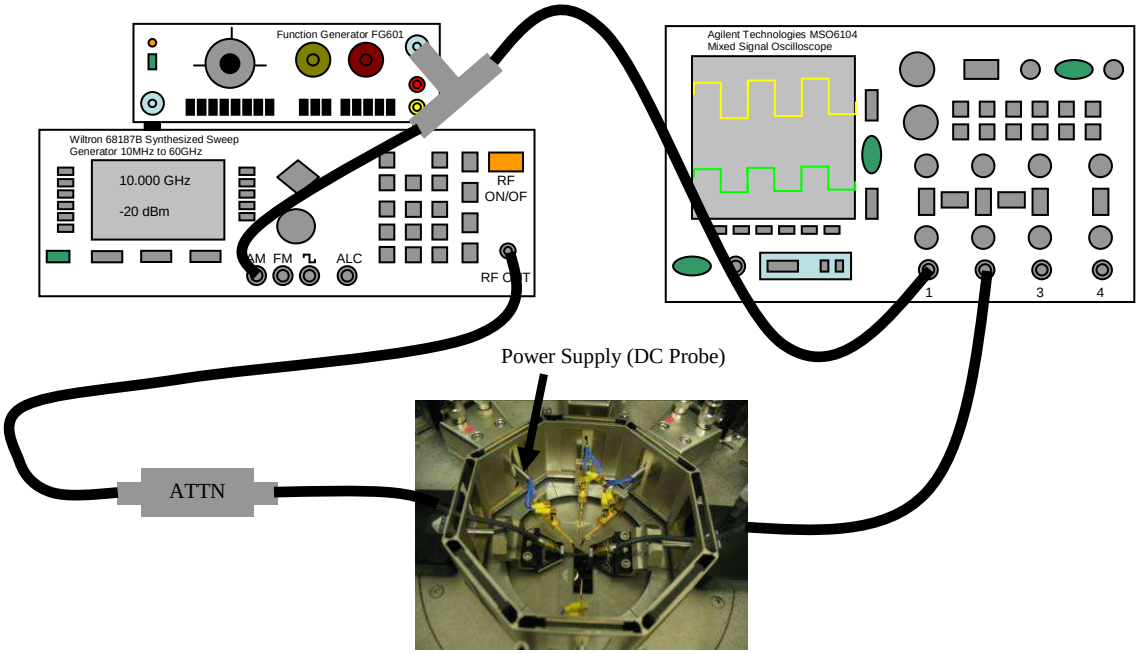


Figure 4. 16. Test set-up of output voltage versus input signal power for detector

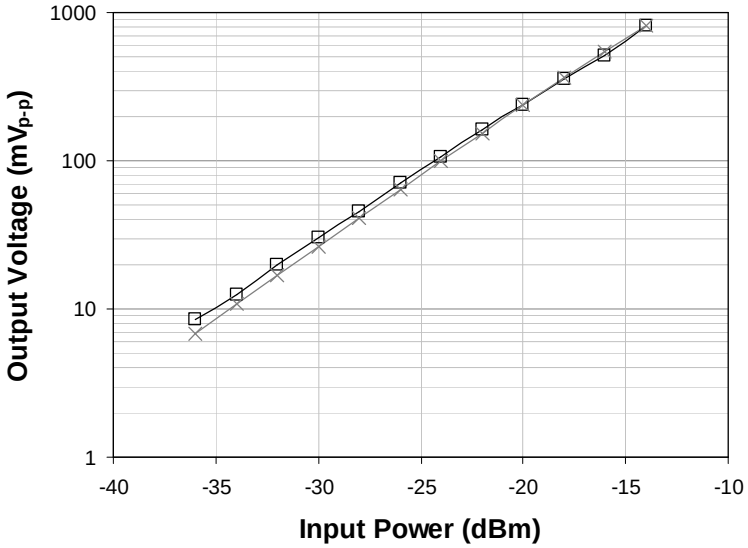


Figure 4. 17. Input power versus output voltage of PHEMT detector: simulation (×), measurement (□)

Figure 4.18 shows the demodulation responses of detector. A carrier signal of 10GHz with a power of -20dBm (not including cable loss) modulated by a 10 kHz square signal wave (top) was transmitted to the input of the detector circuits. A slight distortion of the demodulated signal (bottom) due to the noise performance of detector was observed in the detected signals.

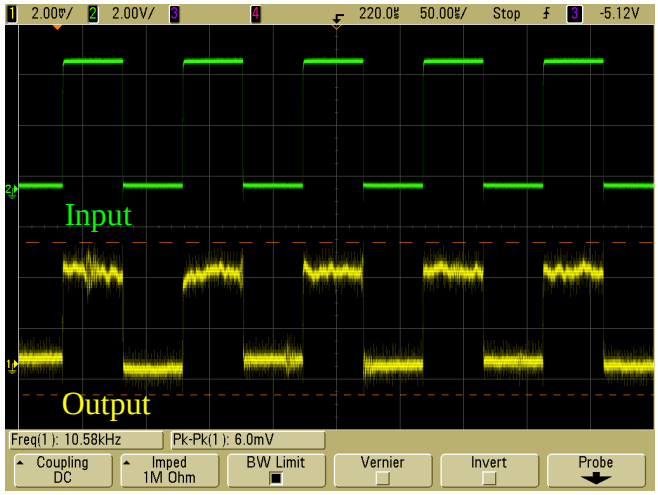


Figure 4. 18. Demodulation responses of PHEMT detector

4.4.4 SPDT Switch

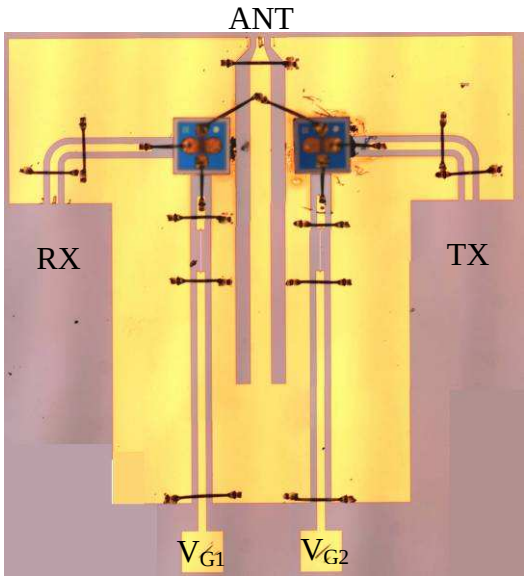


Figure 4. 19. Microphotograph of SPDT switch on GaAs substrate

Figure 4.19 shows a microphotograph of the implemented SPDT switch. The SPDT switch, constructed on CPW structure using two FPD-200 PHEMT devices, was measured to have an insertion loss of approximately 1.7dB at 10GHz whilst the isolation was measured to be approximately 23dB as shown in Figure 4.20. The linearity performance is also important for a switch, thus the insertion loss and isolation versus input power was measured using power level range of -17dBm to +16dBm for both ON and OFF states. Figure 4.21 shows 1dB degradation at +7dBm and +11dBm for insertion loss and isolation, respectively.

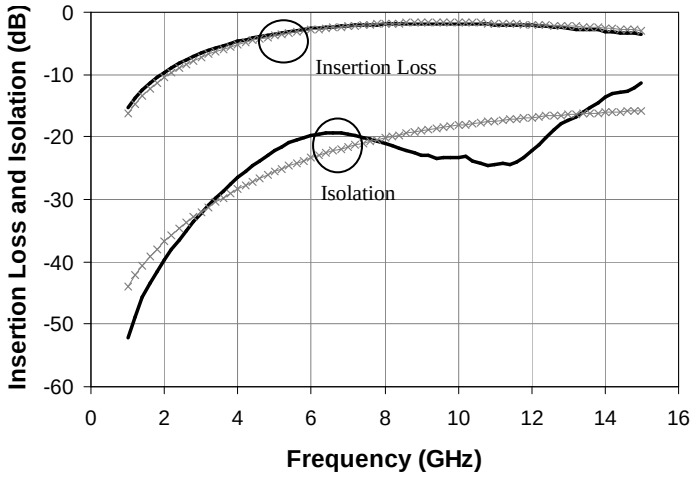


Figure 4. 20. Simulated (×) and measured (—) insertion loss and isolation performances of SPDT switch

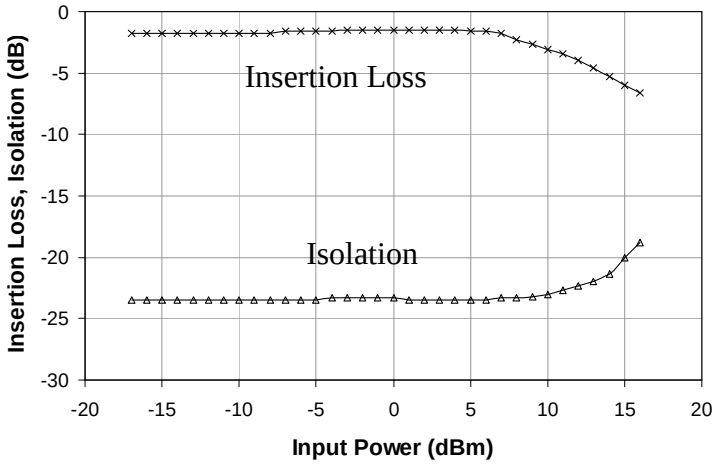


Figure 4. 21. Measured insertion loss and isolation versus input power at 10GHz: insertion loss (×), isolation (Δ)

4.5 Fully Integrated OOK Radio Transceiver

A block diagram of the complete OOK radio transceiver is shown in Figure 4.22. It consists of all the circuits – amplifier, oscillator, detector, and switch – which have been discussed so far. The principles of the switched oscillator and power detector using PHEMT device have also been described in the previous sections.

The data signal has dc offset voltage of -0.9V and the peak-to-peak voltage of 0.6V to turn the oscillator on and off for generating OOK modulation signal and it is consequently achieved by function generator signal with square wave. The detected signal goes through to baseband buffer amplifier to recover an original data signal with digital logic i.e. 0 and 1

in baseband processing. The circuit uses a simple architecture to lower the active component count and hence the power consumption.

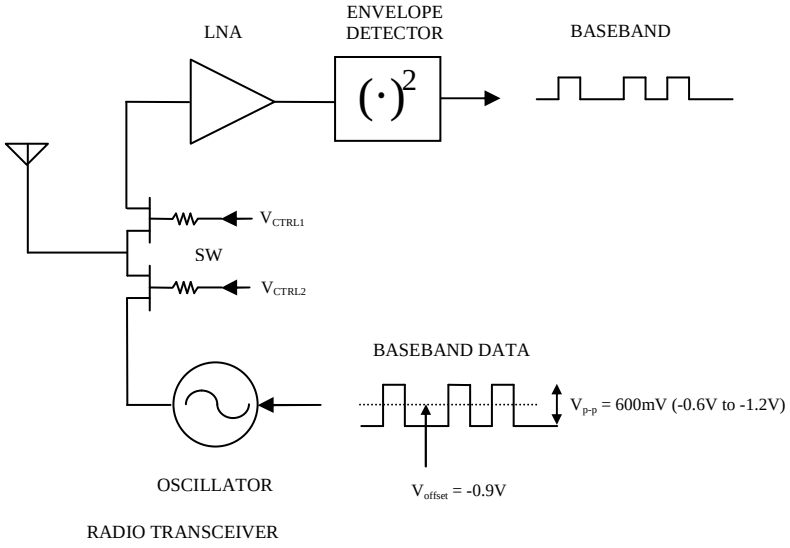


Figure 4. 22. Block diagram of complete OOK radio transceiver

The Schottky diode based envelope detector recovers the data by zero bias operating for low power application [43]. This architecture though suffers from low sensitivity even if this approach has low power consumption and therefore this approach introduces too much noise to the baseband signal. Another approach is based on the GaAs FET envelope detector with drain voltage that is introduced to improve the sensitivity of the detector. But this approach consumes dc current due to drain biasing. Instead it is found that the addition of a cold-HEMT envelope detector results in much better noise performance with higher sensitivity. In fact, the received signal appears largely noise free on an oscilloscope.

The receiver consists of amplifier which has 6dB gain and passive envelope detector without the need for band pass and low pass filter. The amplifier consumes 1.4mA and the passive envelope detector consumes 10nA. The drain and gate bias for amplifier is V_{ds}=0.3V, I_{ds}=1.4mA and V_{gs}=-0.8V, respectively. The overall power consumption of receiver is consequently 420μW. The modulation signal is processed by receiver circuits consisting of amplifier and passive envelope detector to recover the data signal. Amplifier plays a role which compensates an OOK modulation signal for free space path loss. The OOK modulation signal which is amplified by amplifier is passed to the drain terminal of cold-HEMT detector with a matching circuit at the same frequency of amplifier. The detector rectifies the OOK modulation signal with a large output voltage which can be processed by baseband buffer amplifier i.e. 1mV. The radio transceiver uses five HEMT

devices which are the FPD-200 PHEMT. Only two transistors of them consume dc power to realize switched oscillator and amplifier. The regions where the transistors in all of circuits are biased are shown in Figure 4.23.

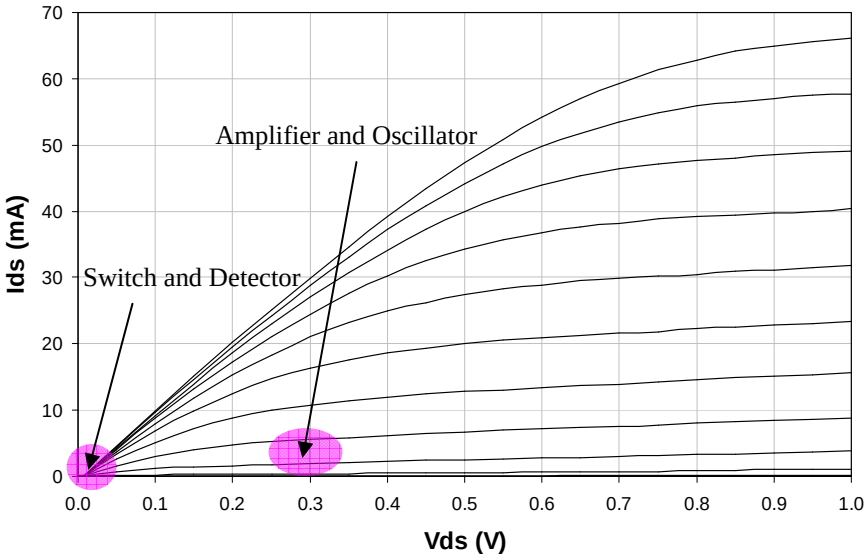


Figure 4. 23. Bias condition of individual circuits in the radio transceiver

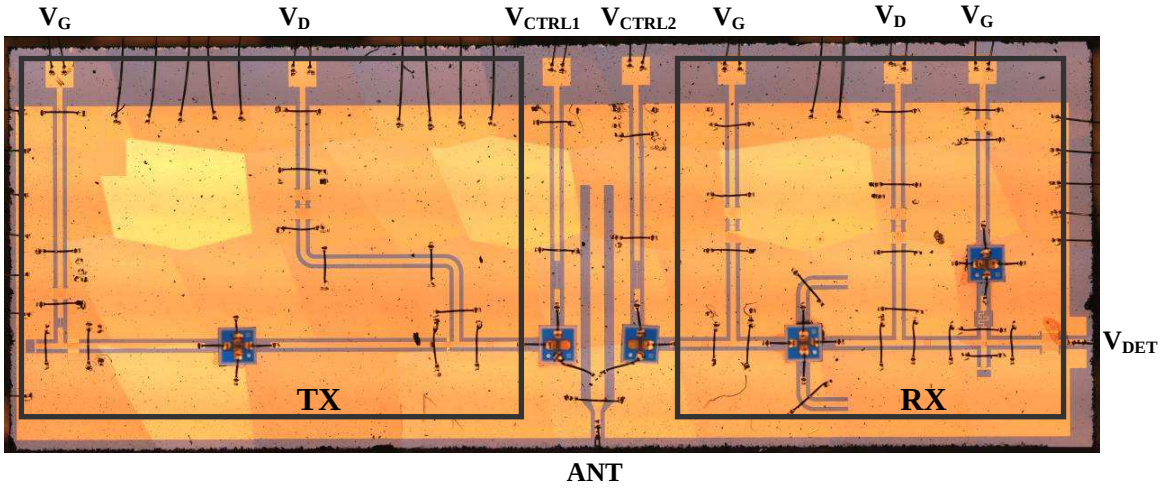


Figure 4. 24. Microphotograph of fabricated quasi-MMIC radio transceiver

The transceiver was fabricated on GaAs substrate which has relative dielectric constant of 12.9, dielectric thickness of 620μm, and gold thickness of 1.2μm. The matching networks and bias circuitry were implemented to achieve compact size transceiver using advanced GaAs MMIC process consisting of lumped-components and meandered transmission lines. The total chip size is 5×12 mm^2. The SPDT switches have an insertion loss of 1.7dB and an isolation of -23dB. The switch is turned off when the gate voltage is

driven to below pinch off (V_g=-1.2V) and presents a low impedance path when the gate voltage is zero. The switch allows one antenna to be shared between TX and RX. Figure 4.24 shows a microphotograph of the fabricated quasi-MMIC radio transceiver. This transceiver is also integrated with a patch antenna implemented on PCB substrate (Rogers RO4350). This patch antenna was designed by Dr Griogair Whyte. Figure 4.25 shows a photograph of the complete integrated transceiver chip with antenna. The total size of this is 15×12mm^2.

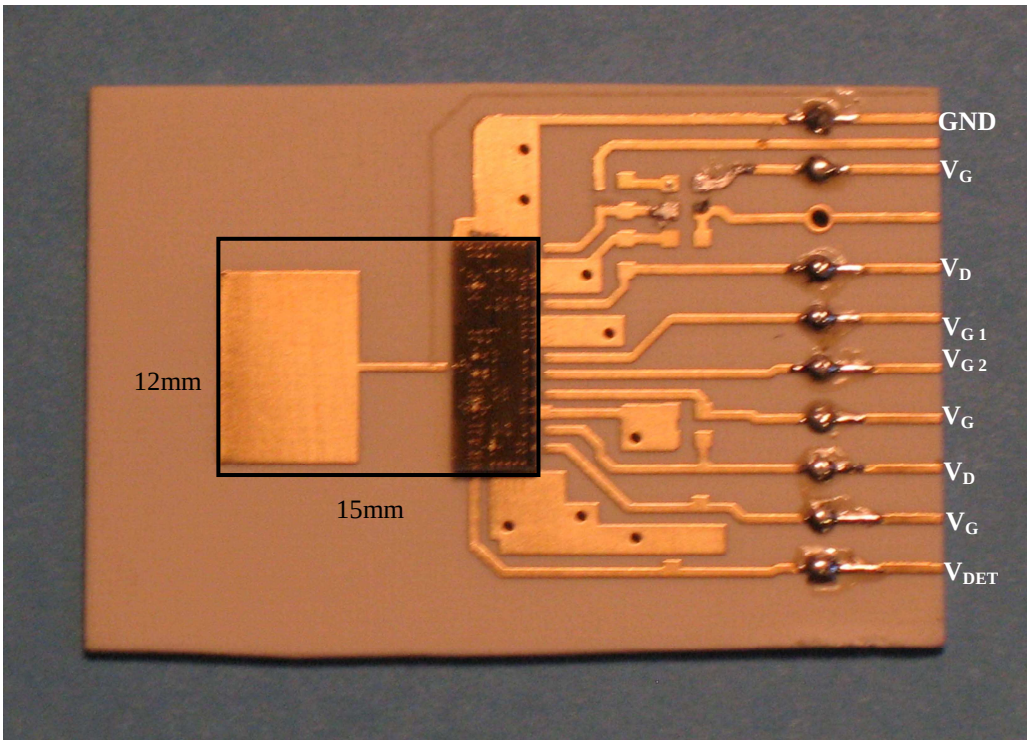


Figure 4. 25. Photograph of complete radio transceiver integrated with antenna on PCB

The switched oscillator as the transmitter directly produces an OOK modulated signal operates at 10GHz with an output power of -10.4dBm. The baseband is used a negative dc offset of -0.9V from function generator and is injected to the gate side with peak-to-peak voltage of 0.6V (-1.2V to -0.6V). The switched oscillator produces the OOK modulation signal with high logic in voltage range of -0.9V to -0.6V and low logic in voltage range of -1.2V to -0.9V. Figure 4.26 shows the variation in switched oscillator fundamental output frequency measured as a function of gate bias.

As shown in Figure 4.26, the switched oscillator frequency varies over a 1GHz span when the gate voltage in the switched oscillator is varied with ±10% from centre voltage of -0.75V. Therefore, the OOK modulation signal can still be detected by the receiver because the receiver can cover input frequency bandwidth of greater than 1GHz as mentioned in the

previous section and the power supply which is used in energy neutral platform is not varied more than 10%.

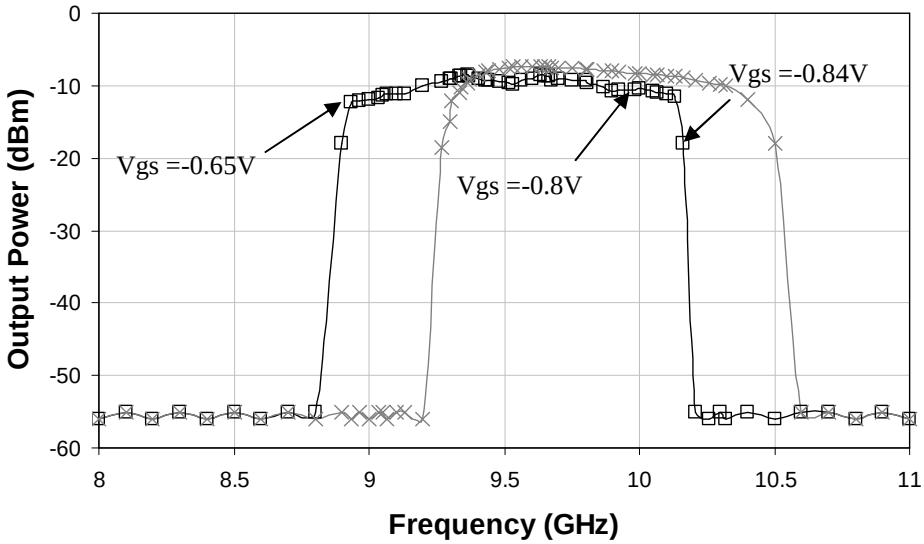


Figure 4. 26. Frequency and output fundamental power of switched oscillator versus gate voltage (V_{gs}): simulation (×), measurement (□)

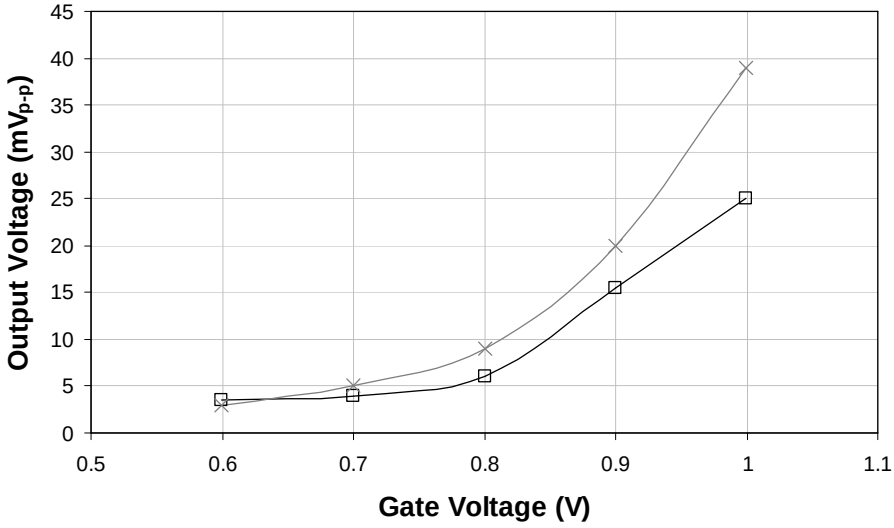


Figure 4. 27. The output voltage of detector versus gate voltage (V_{gs}) of detector: simulation (×), measurement (□)

Figure 4.27 shows the detector output voltage versus gate voltage (V_{gs}) of detector in the receiver which is made up of the switch, amplifier and detector. As aforementioned, as gate voltage is increased, the output voltage increases, but with distortion of data signal. Thus, the optimal gate voltage is chosen to remove the distortion and achieve high sensitivity. To measure this performance, the modulated signal from a signal source is used

and output voltage level is measured on the oscilloscope. The modulated signal from microwave signal source is directly given to SPDT switch without a leakage of signal and then output voltage of the receiver is measured on the oscilloscope by way of the amplifier and detector. From this measurement, the detector operation at the gate voltage of -0.9V shows a good sensitivity without a distortion in demodulated signal, thus this value is chosen to achieve high sensitivity performance of overall receiver. These results also show that gate bias voltage slightly above the pinch-off voltage is used to achieve the highest possible output voltage without further matching networks as mentioned in Equation 4.18.

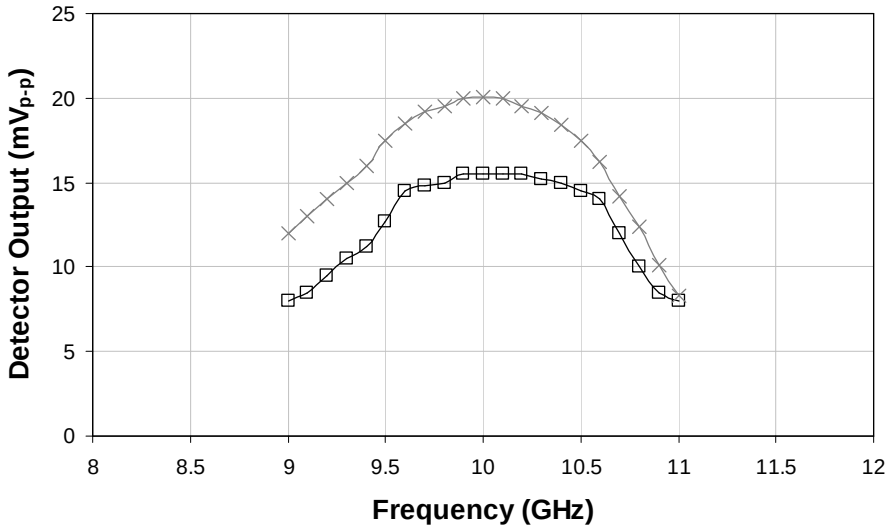


Figure 4. 28. The output voltage of detector versus RF input frequency: simulation (×), measurement (□)

With optimal gate voltage, the receiver is measured to confirm the performance for high sensitivity receiver. Figure 4.28 shows the output voltage versus the radio input frequency for a fixed input power of -20dBm from microwave signal source. As shown in Figure 4.28, the bandwidth is approximately 1 GHz and the output voltage falls off rapidly beyond the range of 9.5GHz to 10.5GHz. As aforementioned, the modulation signal can still be detected by the direct detection receiver while oscillator frequency varies by ±10%. Therefore, the transceiver can still be operated while the power varies with tolerance of ±10% from centre voltage and it is straightforward to make power supply from energy platform that will be integrated together. From Figure 4.26 to 4.28, the difference between simulated and measured results is caused by the hybrid integration for a complete radio transceiver. The hybrid integration with a manual wire bond process provides the variation of inductance and capacitance in the parameters and also mismatch between individual circuits. It can be reduced with repetition of device measurement to obtain more accurate parameter but this work is completed with a few samples to obtain parameters from

measured data. Although the simulation and measurement results show a difference, it is a reasonable result to predict the performance of a complete radio transceiver.

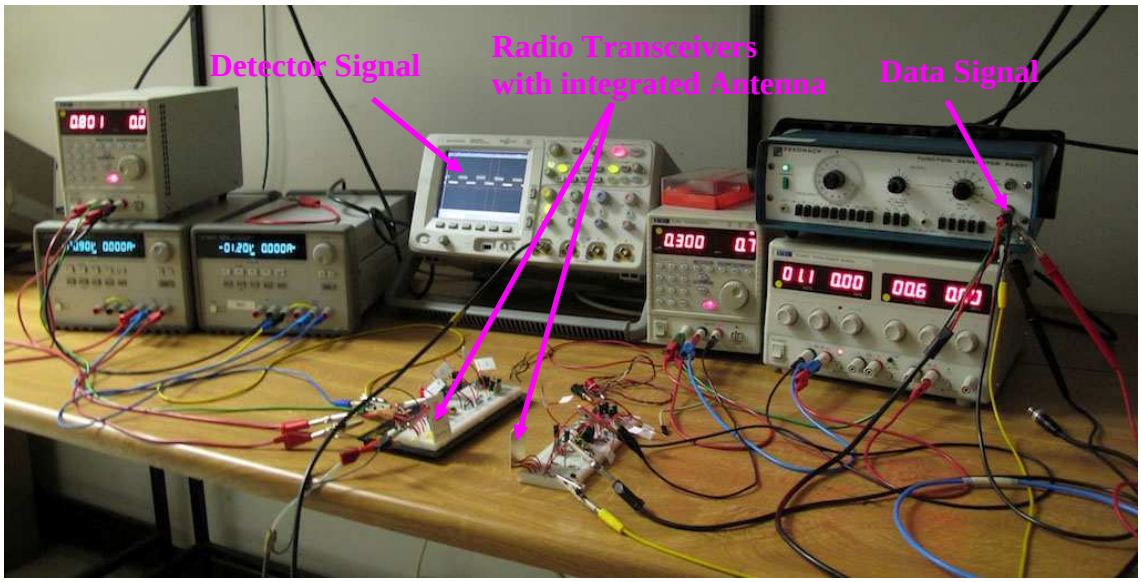
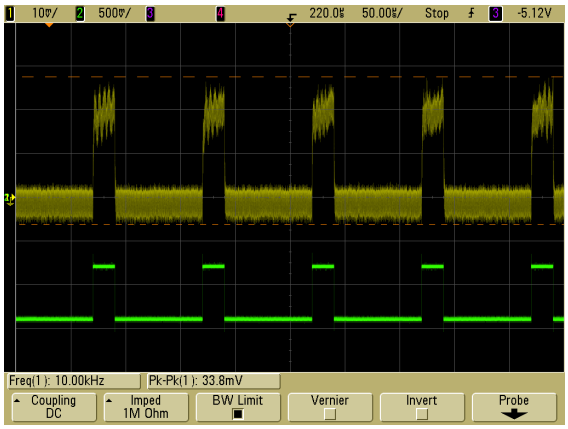
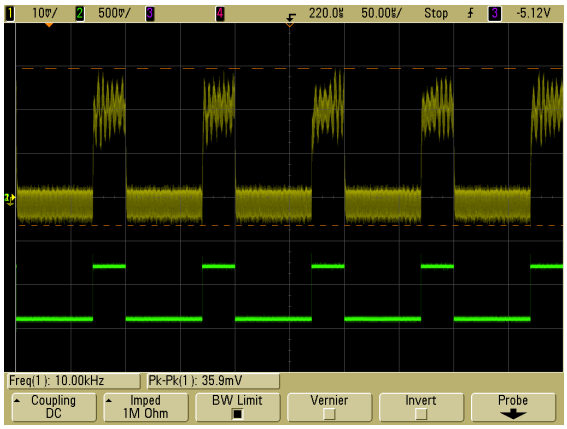


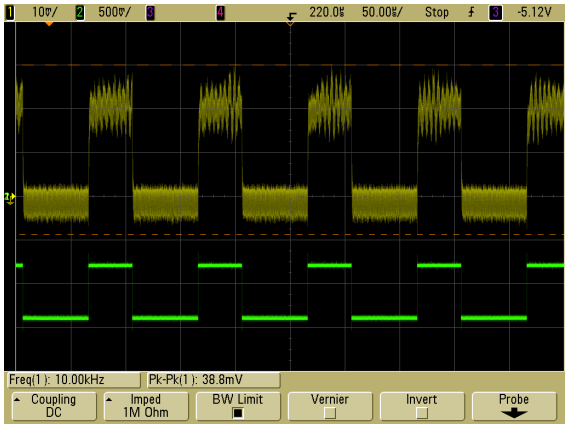
Figure 4. 29. Test set-up of direct modulation/demodulation transceivers



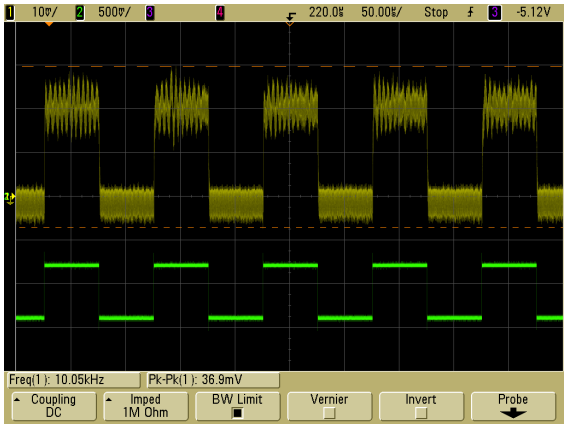
(a) 20%



(b) 30%



(c) 40%

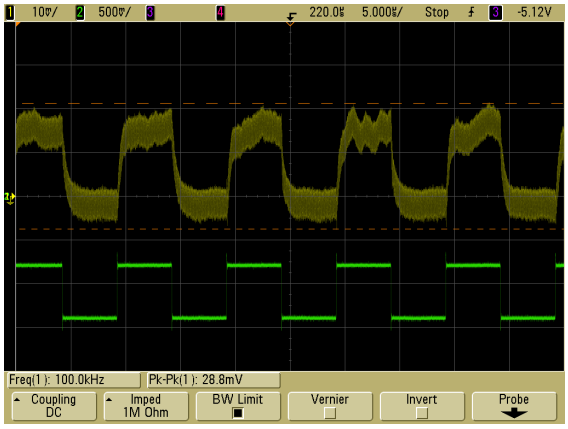


(d) 50%

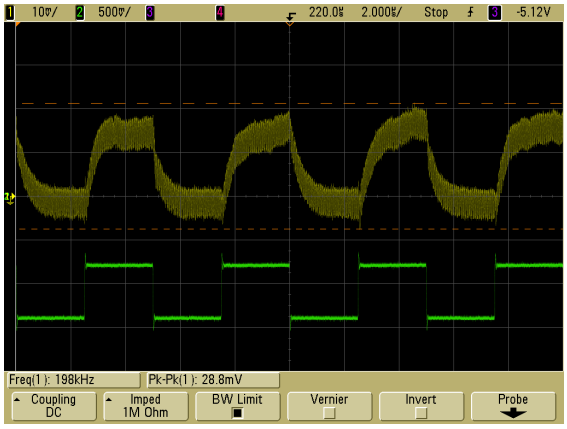
Figure 4. 30. Binary data waveform with duty cycles of 20, 30, 40, and 50% at 10 cm separation between transceivers: input data (green), detector output (yellow)

A complete direct modulation/demodulation prototype transceiver, which has been designed and fabricated using commercial PHEMTs, was successfully integrated on GaAs substrate and demonstrated a good communication between two transceivers. The results verify that it is possible to have ultra-low power consumption and communication range up to 1m between radio transceivers thus fulfilling the target requirements in SpeckNet. Figure 4.29 shows the test set-up used to demonstrate data communication with physical separation between two transceivers.

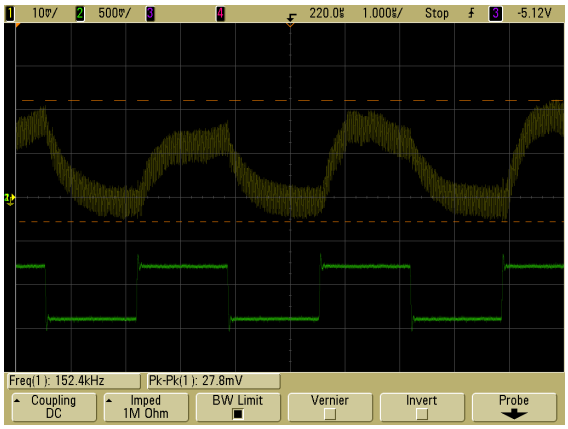
With 50% duty-cycle square wave signal, the transceiver demodulated data signal was measured to demonstrate the operation of transceiver. If the switched oscillator is only ON for a very short period of time relative to the length of data '1' then obviously the power consumed is lower than if the oscillator is ON for the same period of time as the data is at a '1'. This fact can be exploited to reduce the power consumption of the transmitter by duty cycling the transmit oscillator to a number lower than 50% [25].



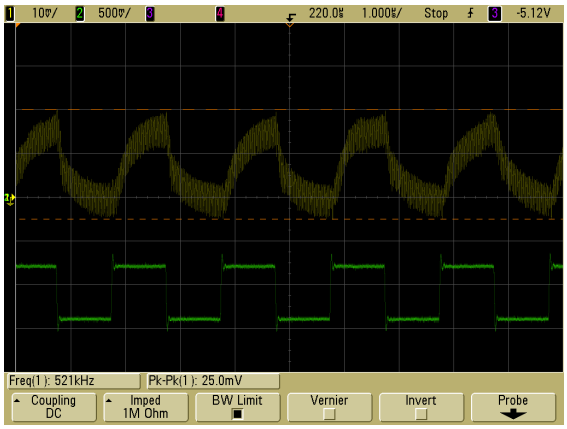
(a)100 kHz



(b) 200 kHz



(c) 300 kHz

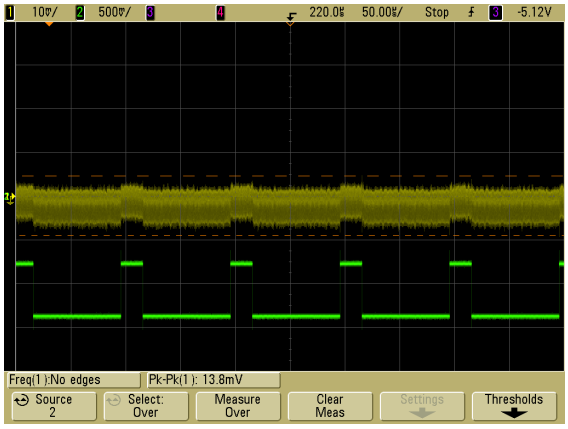


(d) 500 kHz

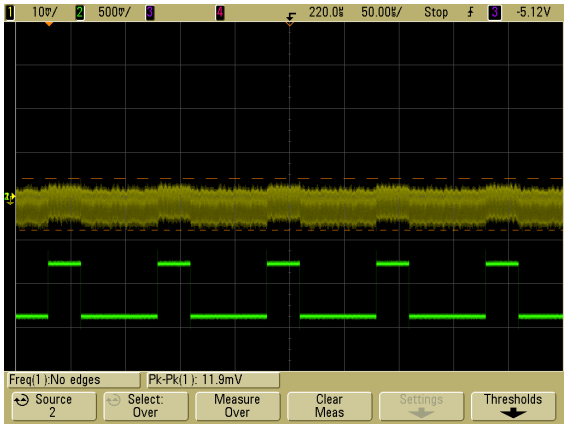
Figure 4. 31. Binary data waveform with different data rate and 50% duty cycle at 10 cm separation between transceivers: input data (green), detector output (yellow)

Figure 4.30 shows the binary data waveform with different duty cycles of 20%, 30%, 40% and 50% at 10 kHz data frequency and transceiver separation of 10cm. Current consumptions are 0.2mA and 1mA for duty cycles of 20% and 50%, respectively. From these measurements, it is clear that lower power is consumed at low duty cycles. However, as shown in Figure 4.30, detected signal is distorted by spikes which are related to the rise and fall of the demodulated waveform. This means that low duty cycle data requires additional low pass filtering to eliminate the distortion.

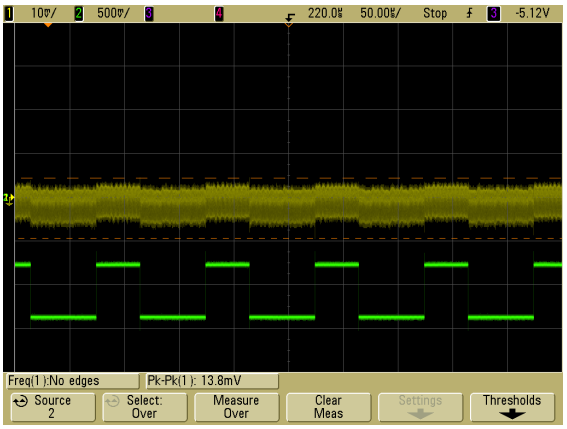
Figure 4.31 shows the binary data waveform with different data rates and 50% duty cycle at 10cm separation. With increasing data rate, the demodulated signal is distorted and it clearly decreases the transceiver sensitivity. The transceiver is therefore suitable for sensor nodes for SpeckNet which is required low data rate (<200kbps) operation. The small physical size and low power consumption also makes the transceiver ideally suited for wide range deployment and long unattended operation without battery replacement.



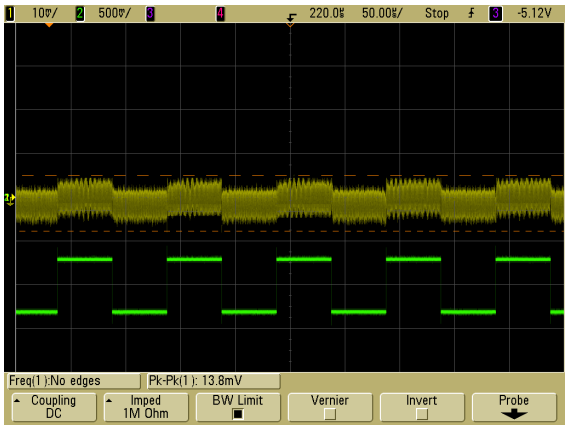
(a) 20%



(b) 30%



(c) 40%



(d) 50%

Figure 4. 32. Binary data waveform with duty cycles of 20, 30, 40%, and 50% at 1 metre separation between transceivers: input data (green), detector output (yellow)

Figure 4.32 also shows the binary data waveform with duty cycles of 20%, 30%, 40%, and 50% at 10 kHz data frequency and transceiver separation of 1m. The detector output shows a noisy signal but the signal and noise in the detector output can still be distinguished. They can also be improved by using low-pass filtering and baseband processing. Thus, the transceiver as it is can be used at a distance of 1 metre.

4.6 Conclusions

This chapter has introduced a quasi-MMIC OOK radio transceiver which has been fabricated and demonstrated with the concept of direct modulation and demodulation for ultra-low power radio transceiver. The data signal with 50% duty-cycle square waveform is used in the gate side of switched oscillator to produce the OOK modulation signal and it is produced at the drain port of switched oscillator to propagate via antenna. The modulated signal is transmitted and received by each antenna for communication. The demodulated signal is obtained at the load of detector by way of switch, amplifier and detector. This concept is very simple and exhibits low cost, ultra-low power performance simultaneously. The transceiver also exhibits small size.

The start-up time of switched oscillator and output voltage level of detector with gate voltage has been validated with a mathematical analysis and measurement results. With a mathematical analysis, the start-up time of oscillator is demonstrated to achieve the higher data rate operation and the operating voltage of detector is also analyzed to choose the gate voltage for achieving higher sensitivity and lower distortion. This chapter also gave a detailed description of quasi-MMIC OOK radio transceiver operating at 10GHz and with data rate up to 200 kbps. The transmitter consists of switched oscillator with negative resistance design concept. The switched oscillator consumes dc power of 420μW and it also achieves an efficiency of around 22% with the output power of approximately 100μW or -10dBm. To produce a modulation signal, the data signal with square wave is given a negative dc offset of -0.9V from function generator and is injected to the gate side with peak-to-peak voltage of 0.6V (-1.2V to -0.6V). The switched oscillator produces the OOK modulation signal when there is a voltage range of -0.9V to -0.6V which means a ‘1’, and is pinch off when there is a voltage range of -1.2V to -0.9V which means a ‘0’. The receiver consists of an amplifier and detector. In total the receiver consumes 420μW and generates an output voltage of 1mVp-p for a transceiver separation of 1 metre.

In conclusion, this chapter has provided a description of the operation of direct modulation/demodulation radio transceiver with OOK modulation scheme and has

provided an equation to describe the switched oscillator operation and output voltage level of a detector. The equation of start-up time for oscillator has also been derived together with a description of power consumption for increasing data rate. An implementation of an ultra-low power OOK radio transceiver has been described and measured results to demonstrate its performance. It has been shown that the power consumption of a complete radio transceiver, integrating both transmit and receive circuitry can be as low as 840μW. Further, the power consumption of the transceiver can be reduced by adjusting duty-cycle of data signal has been presented. Also, the output voltage of the receiver can be increased by a gate voltage of detector and thus operating range of the complete transceiver can be greatly increased by optimizing the gate voltage for the detector circuit.

Chapter 5

24GHz MMIC Radio Transceiver

5.1 Introduction

In the previous chapters, the 10GHz radio building blocks and direct modulation/demodulation transceiver were realized in quasi-MMIC form. This enable rapid prototypes to be developed for verifying the circuit ideas but it results in a larger size compared with the ultimate requirements of Specks (5×5 mm^2). Thus, further reduction of circuit and antenna size is needed to satisfy the target of SpeckNet project. Monolithic microwave integrated circuit (MMIC) technology can be used to reduce the size of circuits and antenna on GaAs substrate with a high operating frequency. The use of a high frequency, as well as MMIC technology, can produce fully integrated transceivers with compact size. For compact antenna size, the 24GHz frequency band (which is one of the ISM bands) can be used with high performance devices on a MMIC process. To achieve a compact transceiver, MMIC technology is better but it lacks capability for post-fabrication tuning. Thus, an accurate design method is required to realize good performances and reduce process cost. Accurate device measurement and modelling using simulation is also required.

In this chapter, the device technology used in the design of MMIC is discussed and then the devices are measured on-wafer in a coplanar waveguide (CPW) structure on GaAs substrate. To obtain a pure device S-parameters, the embedded structures which are inserted for measurement are simulated and measured to compare between them and then these structures are de-embedded from measured device S-parameters to use in the design. As mentioned in the Chapter 3, capacitors and inductors are measured on wafer and simulated with Ansoft HFSS and also validated with comparison between simulation and measurement results. They will be used to design individual circuit such as amplifier, oscillator, detector, and switch. To achieve an accurate design and implementation of MMIC circuits, passive circuit library such as cross-junction and tee-junction are required. They are already used in Chapter 3 to implement quasi-MMIC radio transceiver and will also be used to design MMIC circuits with the same methods. Individual circuits such as oscillators, envelope detector, switches and amplifiers of the radio transceiver are designed using de-embedded device data with libraries of lumped-components and discontinuities.

The use of the library with simulation data is an easy and accurate method to achieve MMIC circuit design without measurement and extraction and thus the performance of MMIC circuit can be accurately predicted.

The MHEMT device technology at University of Glasgow using an advanced III-V compound semiconductor will now be described and will be followed by a description of the design of individual circuits and finally the completely integrated transceiver with antenna that meets the target size of the SpeckNet project.

5.2 MHEMT Device

To realize the transceiver in MMIC technology, the metamorphic high electron mobility transistor (MHEMT) device with 50nm gate-length have used. The 50nm GaAs MHEMT structures with δ-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ profile, as shown in Figure 5.1, were grown by molecular-beam epitaxy on semi-insulating GaAs substrates.

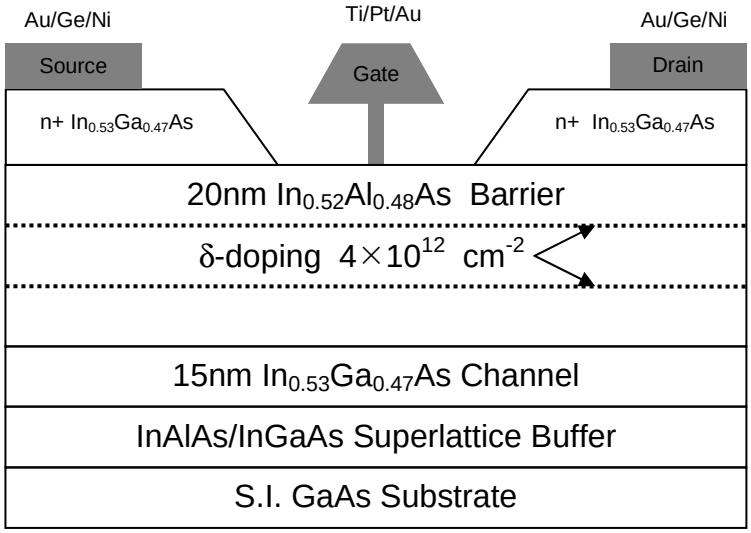


Figure 5. 1. Device cross section of the δ-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ 50nm gate-length GaAs metamorphic HEMTs

The double δ-doped strategy was used to increase drive current, reduce access resistance and enhance linearity [44]. The 1200nm metamorphic buffer graded linearly from GaAs to $In_{0.53}Ga_{0.47}As$ and followed by a 72nm thick $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ superlattice prior to the growth of the device layers. The relatively low value of mobility of 6470 cm^2/Vs was obtained due to the double δ-doping strategy which increases ionized impurity scattering. Ohmic contact resistances as low as 0.06Ω·mm were obtained using an annealed 150nm thick Au:Ge:Ni based metallization. Devices were realized using 1.1μm

source to drain separation between 50nm T-gates with 200nm thick Ti:Pt:Au [45]. As shown in Figure 5.2, a typical drain-to-source saturation current (I_{dss}) and maximum transconductance ($g_{m,max}$) versus gate-to-source voltage (V_{gs}) of the fabricated device are 770 mA/mm and 950 mS/mm, respectively. The RF measurements were performed on-wafer over a frequency range of 0.1 to 110GHz using an Agilent E8361A with N5260 mm-wave controller. At the bias condition of V_{ds} of 0.3V and I_{ds} of 1.1mA, the two-finger 50-μm gate width MHEMT device has a cut-off frequency (f_T) of 56 GHz and a maximum oscillation frequency (f_{max}) of 109GHz, respectively.

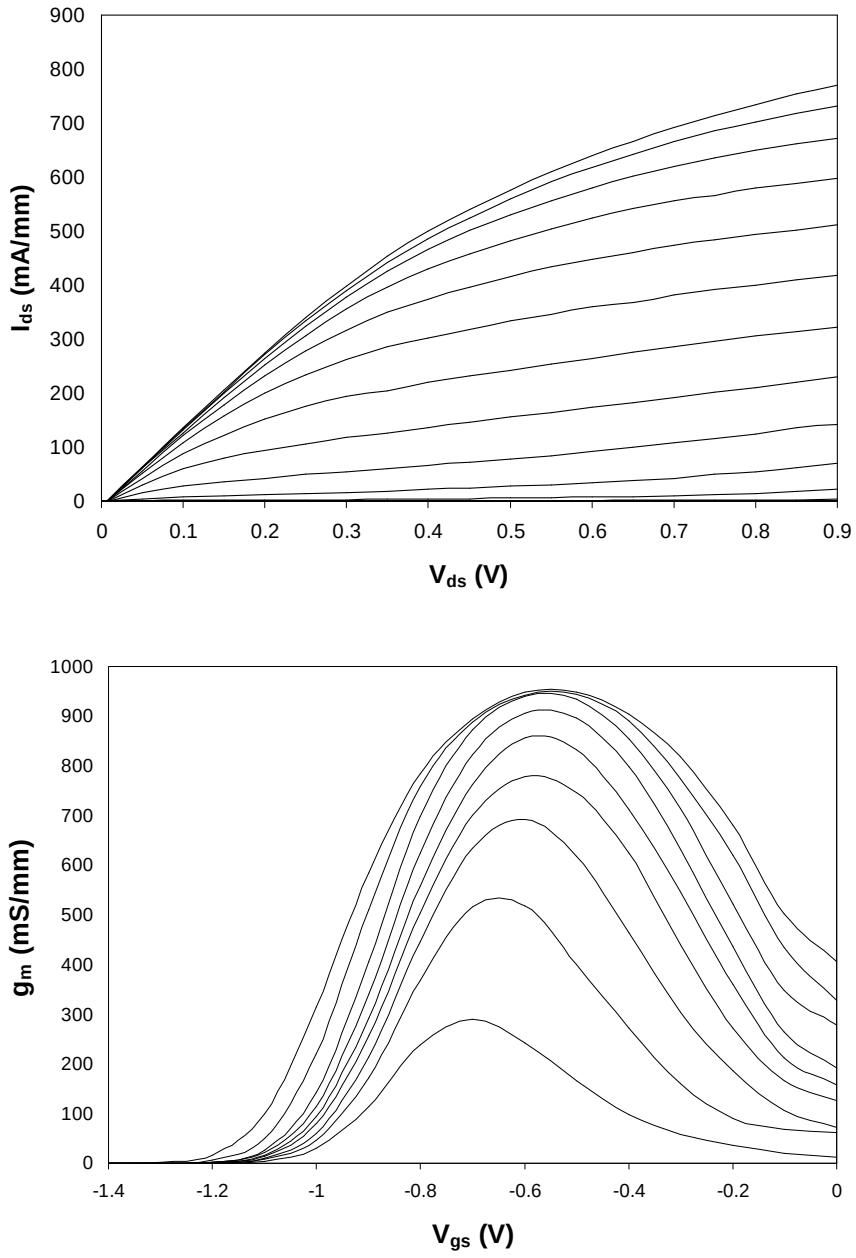


Figure 5. 2. *I-V* and transconductance (g_m) characteristics of 2×50μm, δ-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ 50nm gate-length T-Gate GaAs metamorphic HEMT (V_{ds}=0.1V to 0.9V and V_{gs}=0V to -1.4, 0.1V step)

5.2.1 Non-linear Model of 50nm MHEMT Device

To enable Harmonic Balance analysis of the individual circuit such as oscillator and detector, a non-linear model of the MHEMT device has been extracted using measured *I-V* and RF data over different bias conditions. As mentioned in the previous chapter, the TOM3 model as shown in Figure 3.10 is used to extract a non-linear model from measured S-parameters and *I-V* curve.

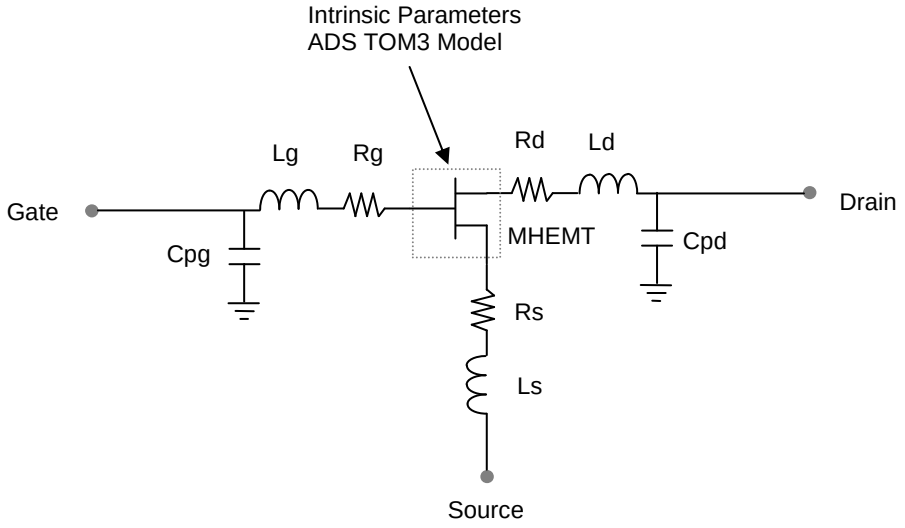


Figure 5. 3. The device model with external parasitic parameters

The TriQuint TOM3 scalable non-linear model is used to provide a good fit to the measured data. Figure 5.3 shows the networks which the external parameters present around the non-linear device model. The external parameters were extracted from measured S-parameters of cold-HEMT which are de-embedded from the probe pads [29] and then the intrinsic parameters, which are described by equations 3.3 to 3.21 in Chapter 3, were also extracted by fitting to the measured S-parameters taken at various bias conditions. Table 5.1 shows the extrinsic parameters extracted from measured cold-HEMT S-parameters [29]. Table 5.2 shows the intrinsic parameters which are extracted by fitting to the measured S-parameters over several different bias conditions.

Cpd	19.18 fF	Rd	2.21 Ω
Cpg	4.73 fF	Rs	3.53158 Ω
Ld	0 pH	Rg	6.60 Ω
Ls	0.016 pH		
Lg	0.01 pH		

Table 5. 1. Extrinsic parameters of TOM3 model for 50nm, 2×50μm MHEMT

Vto	-0.644261 V	Qgqh	7.29104E-16	Is	3.3386E-13 mA
Alpha	7.70356	Qgi0	1.19957E-6 A	Vbi	1 V
Beta	0.00149702	Qgag	1.881	N	1
Lambda	-0.121785	Qgad	3.21664	Xti	2
Gamma	0.128896	Qggb	144.034	Eg	0.8
Q	0.389345	Qgcl	1.01055E-16 F	NG	2
K	0.940054	Qgsh	5.87858E-16 F	W	50 μm
Vst	0.0767583 V	Qgdh	1.18716E-16 F	Rgsh	0 Ω
Mst	0.39525	Qgg0	2.98356E-17 F	Ls	0 nH
Ilk	1.8E-6 mA	Cds	0.0001373 pF	Lg	0 nH
Plk	1.5 V	Tau	0.488 psec	Ld	0 nH
Kgamma	0.00378975	Rd	0.01 Ω		
Taugd	1000 nsec	Rg	0.01 Ω		
Qgql	1.07693E-15	Rs	0.01 Ω		

Table 5. 2. Intrinsic parameters of TOM3 model for 50nm, 2×50μm MHEMT

To validate the accuracy of the extracted model parameters, an *I-V* curve for gate voltage range of 0 to -1.4V and S-parameters at V_{ds}=0.3V and I_{ds}=1.6mA using model parameters are compared with the measured data. Figure 5.4 shows a comparison between measured and modelled *I-V* curve. Figure 5.5 also shows a comparison between measured and modelled S-parameters at bias point of V_{ds}=0.3V and I_{ds}=1.6mA.

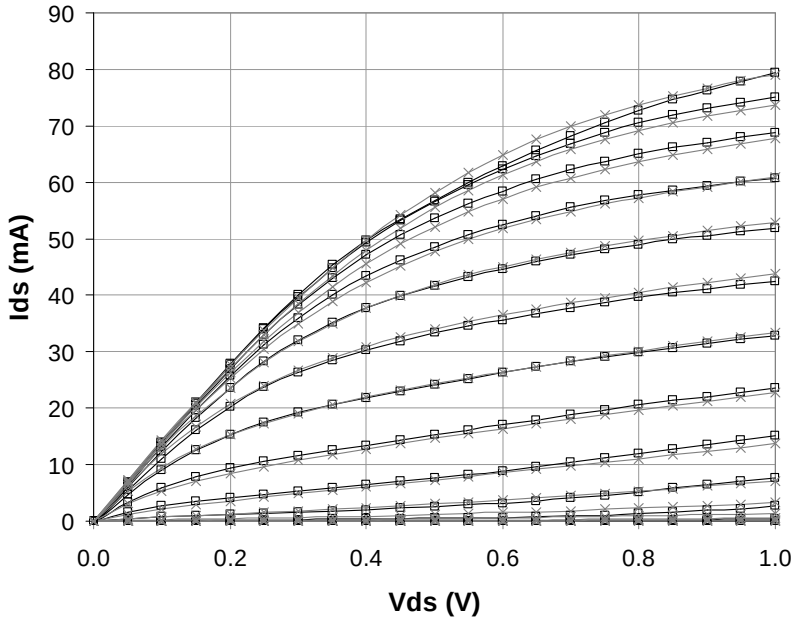


Figure 5. 4. Measured (□) and modelled (×) *I-V* curves of 50nm MHEMT

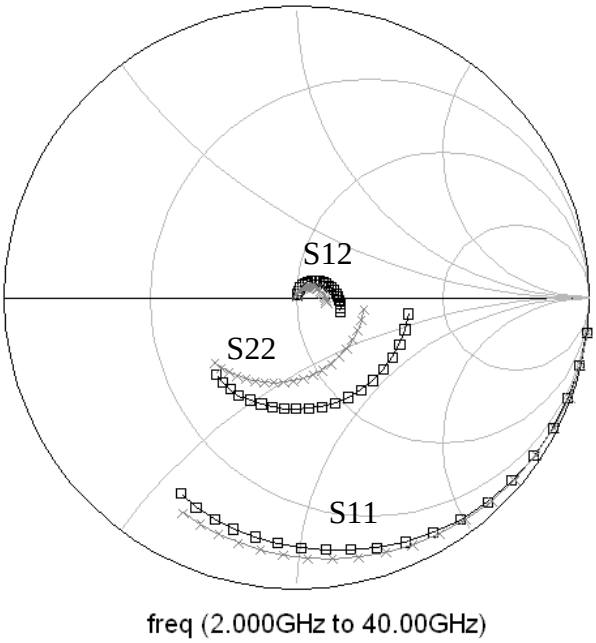


Figure 5. 5. Measured (□) and modelled (×) S-parameters of MHEMT at bias of V_{ds}=0.3V and I_{ds}=1.6mA

This model shows a good agreement with measured *I-V* data making it suitable for non-linear design of oscillators and detectors which are required accurate design for integration into a complete transceiver.

5.3 Oscillator

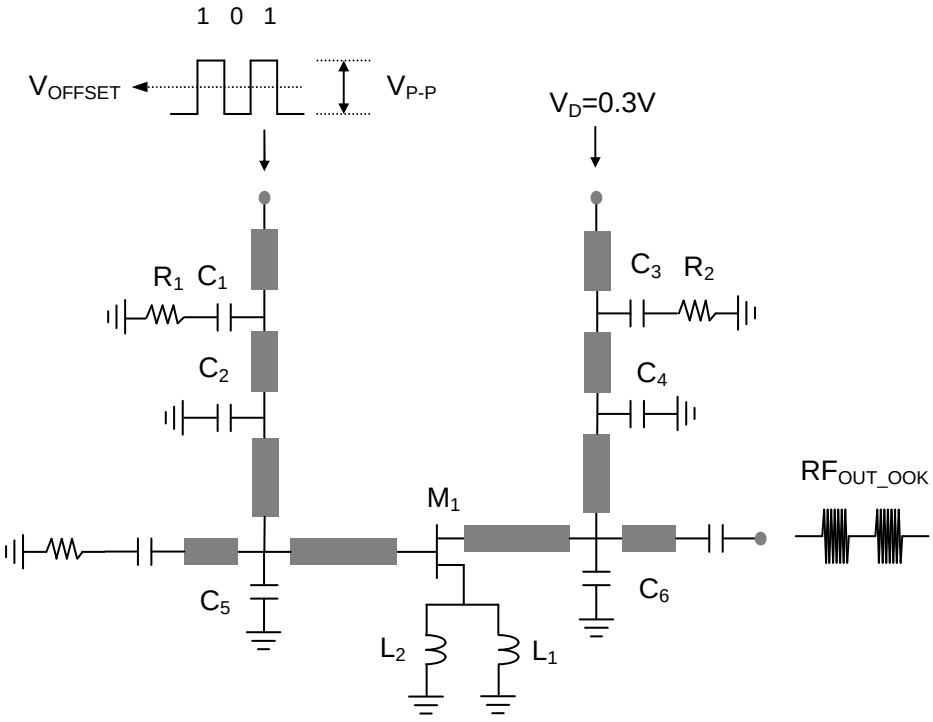


Figure 5. 6. Schematic of switched oscillator for OOK modulation

Figure 5.6 shows a schematic of the switched oscillator. The oscillator is switched on and off when data waveform is '1' and '0', respectively to generate an OOK modulated signal. Figure 5.7 shows the optimal performance of oscillator using measured two port S-parameters. It has been shown in Chapter 3, by using the simple design method, an oscillator circuit can be optimized for output power whilst keeping the oscillator operating frequency constant. The oscillator has also been demonstrated with an optimized load network and maximized negative resistance circuit. The biasing arrangement is V_{ds}=0.3V and I_{ds}=1.6mA.

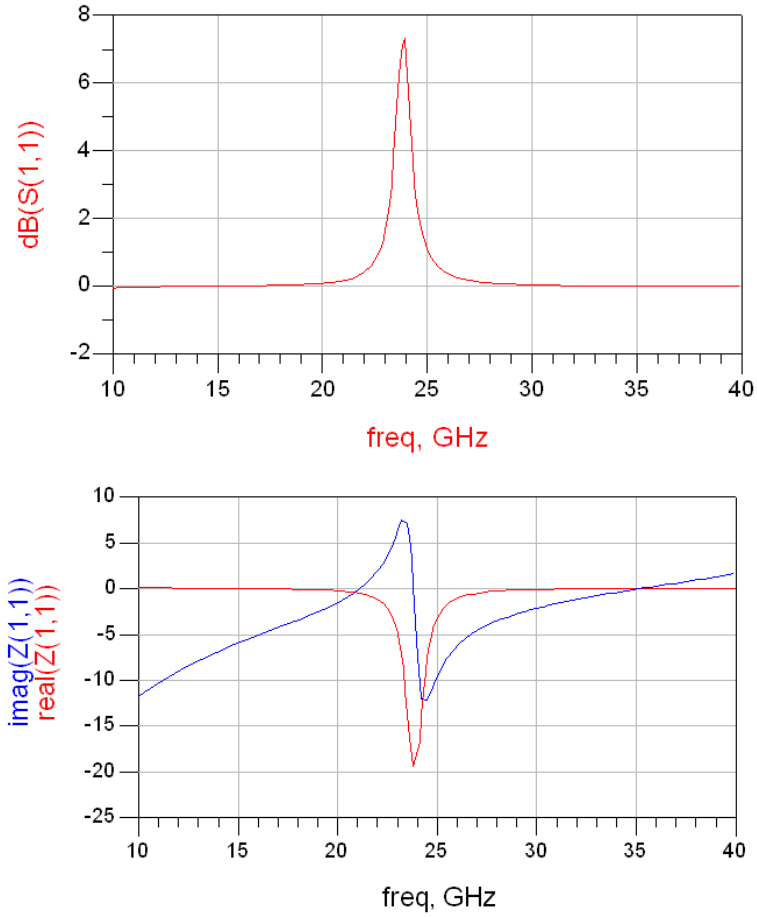


Figure 5. 7. Optimal performance of oscillator using measured two-port S-parameters

Figure 5.8 shows the layout of the MMIC oscillator. A series inductor connected at the source terminals increase the portion of unstable impedances in the Smith chart. This makes it easier to match for negative resistance. A negative resistance at the drain port is created by appropriately matching the gate circuit so that the reflection coefficient lies in the unstable region of the Smith chart. The negative resistance is then increased in value by the output matching network.

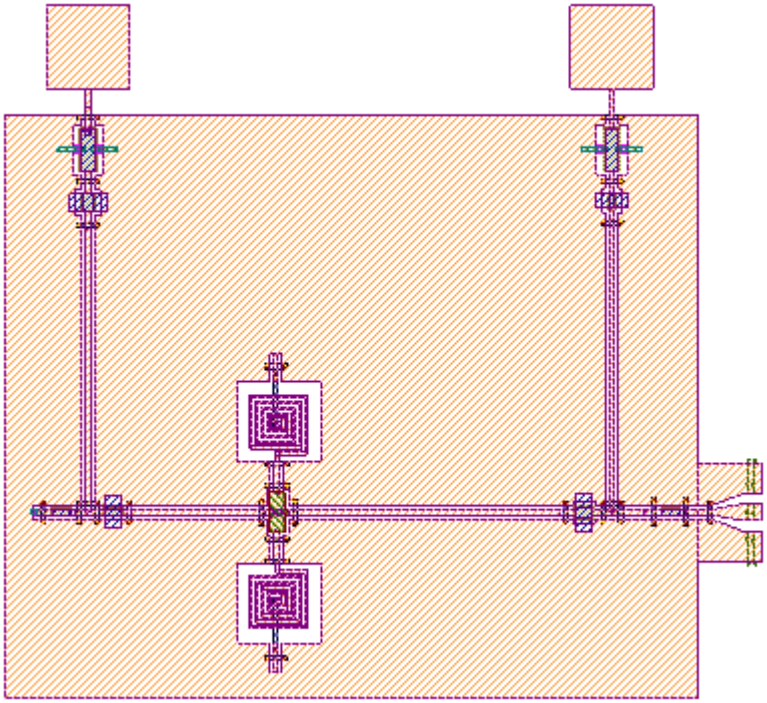


Figure 5. 8. The layout of MMIC oscillator

5.4 Amplifier

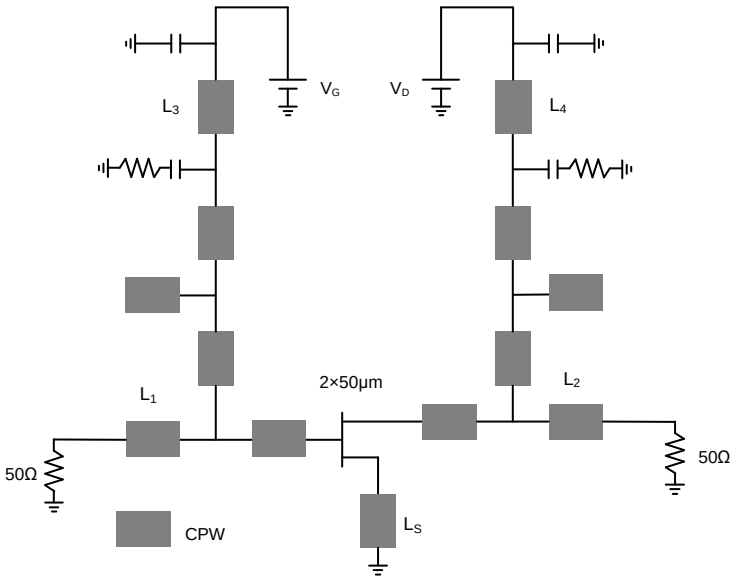
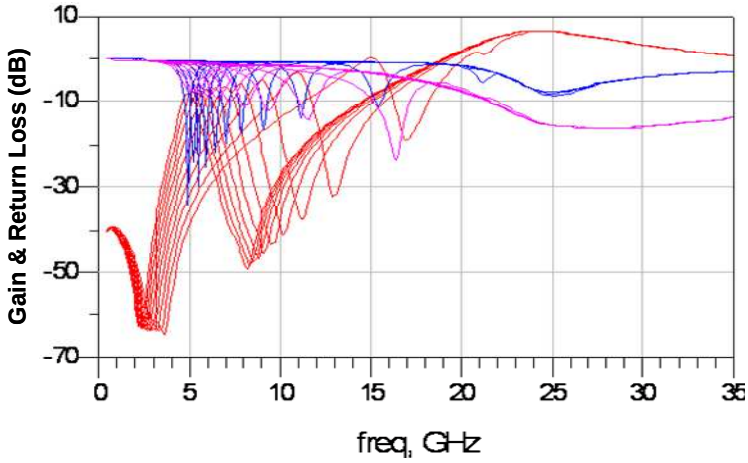


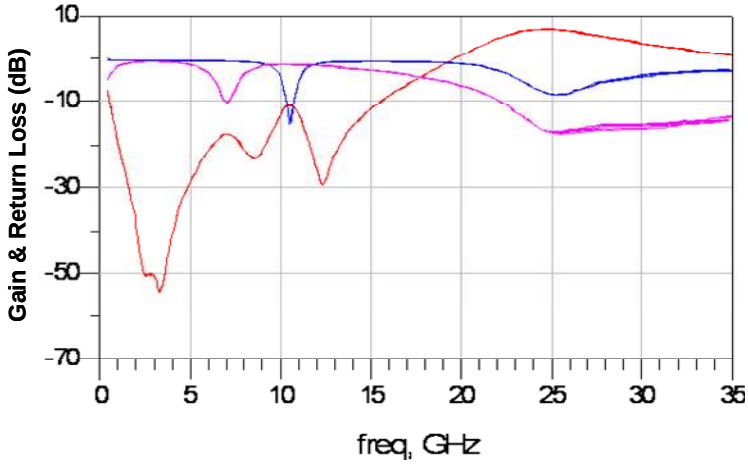
Figure 5. 9. The schematic of amplifier with source feedback

This section describes a 24GHz MMIC amplifier that meets the requirements of high gain, low noise and high isolation while achieving the lowest dc power consumption possible. Several amplifier architectures were considered for ultra-low power high gain

amplifier [46]-[48]. The single stage amplifier with series source feedback topology was designed to achieve the aggressive performance targets such as low power consumption, stability and high gain. The inductance of series source feedback is optimized to achieve the stability and high gain characteristics simultaneously. Moreover, the overall matching network of amplifier is kept simple and therefore a compact chip size is achieved. Also the out-of-band stability of the amplifier is improved by bias circuits [49]. The simplified schematic of the amplifier is presented in Figure 5.9. Bias condition is similar to that of the oscillator previously described.



(a)



(b)

Figure 5. 10. Gain and return loss of amplifier versus variation of line length at (a) bias circuits (L_3, L_4=100µm to 1000µm, 100µm step) and (b) input and output feeds (L_1, L_2 =100µm to 500µm, 100µm step)

By determining appropriate width and length for series inductance (L_S) and the biasing elements this amplifier was designed to be unconditionally stable from low megahertz up to the unity gain frequency of the transistor and exhibits high gain at 24GHz. Bias circuits

are connected to external line by wire bonding process so bias circuits provide increased inductance. Thus, an amplifier circuit must be designed by considering these variations. The amplifier was simulated with variation of line length in bias circuit (L_3, L_4) and input and output feeds (L_1, L_2). Figure 5.10 shows amplifier characteristics with these variations of line lengths.

The amplifier was designed with consideration of these effects and fabricated around a 2×50μm, 50nm gate-length MHEMT. Figure 5.11 shows SEM microphotographs of the MMIC amplifier chip which occupies 1.9×2.3 mm^2.

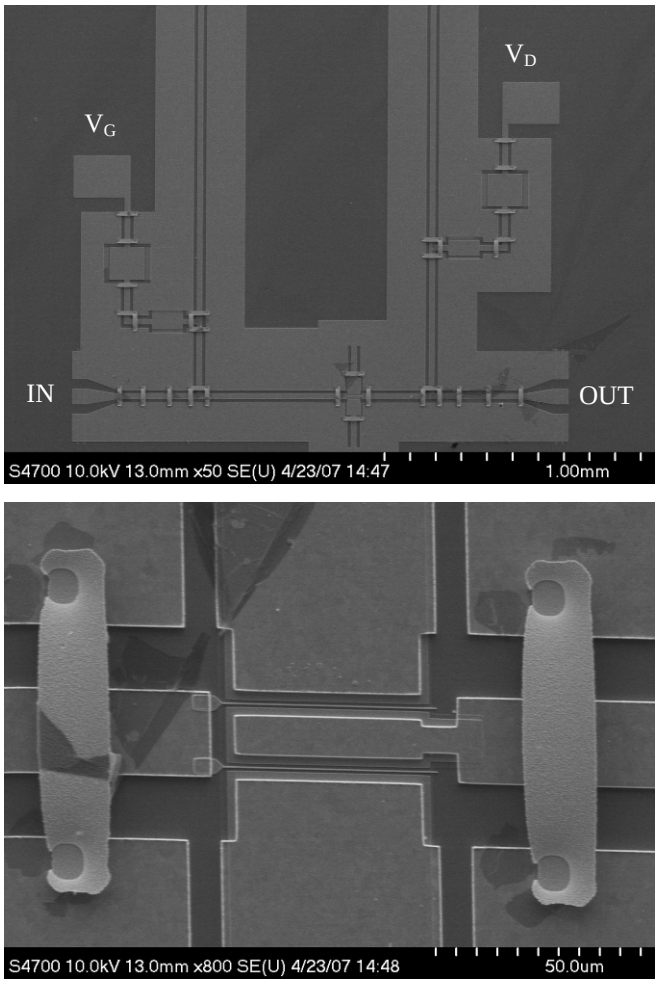


Figure 5. 11. SEM microphotograph of fabricated amplifier

The MMIC layout employs a single MHEMT device with distributed elements in coplanar waveguide, quarter wavelength open stubs, thin film NiCr resistor, and metal-insulator-metal SiN capacitors. In order to achieve stability, the amplifier used 50Ω impedance short circuit stubs at the source of the MHEMT device and shunt resistors with series capacitor on bias circuits [47]. The fabricated MMIC amplifiers were measured on-wafer using Agilent E8361A with N5260 mm-wave controller. In order to confirm dc

power consumption and transmission performance, the amplifier was biased at 0.3V and 1.1mA, 2.9mA, and 4.3mA.

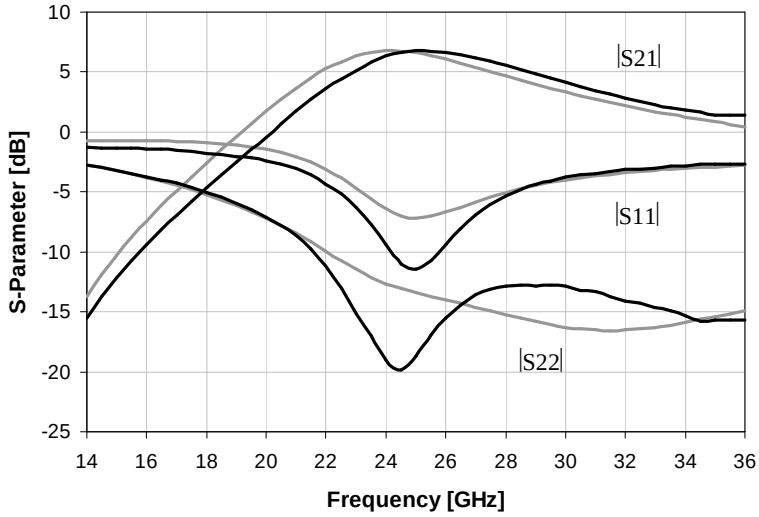


Figure 5. 12. Comparison between simulation (grey) and measurement result (black) with bias condition of V_{ds}=0.3V and I_{ds}=2.9mA

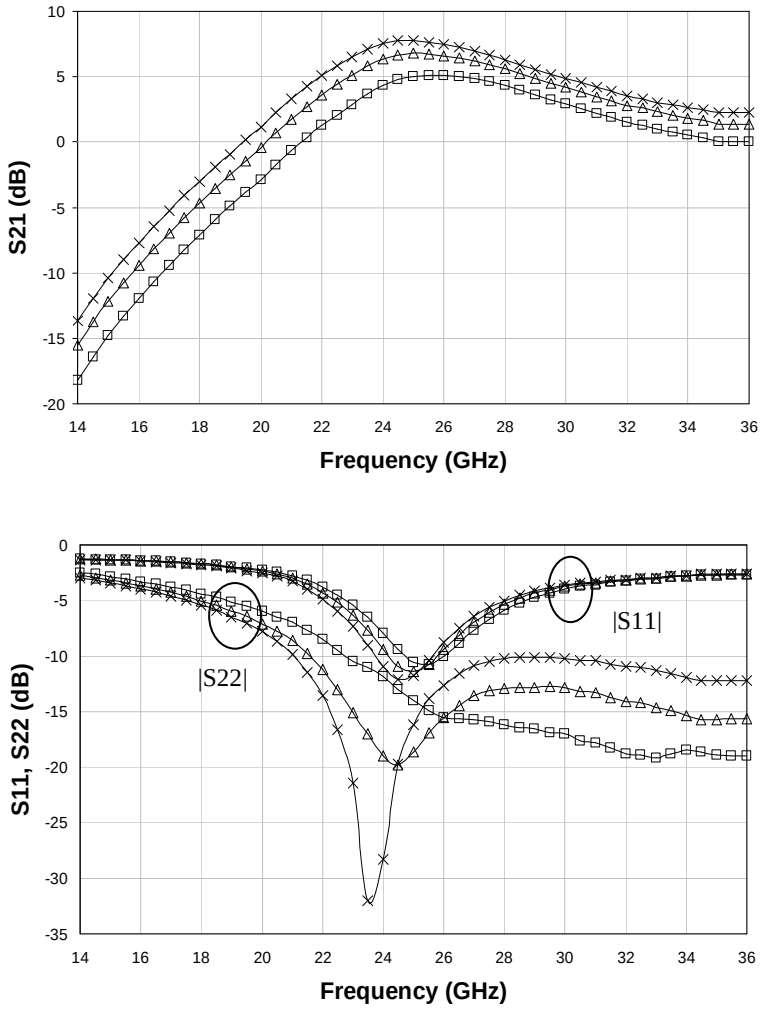


Figure 5. 13. Gain and return loss of the single-stage MMIC amplifier: V_{ds}=0.3V, I_{ds}=1.1mA (□), 2.9mA (Δ), and 4.3mA (×)

Figure 5.12 shows measurement results with bias condition of V_{ds}=0.3V and I_{ds}=2.9mA to compare with simulation results. Figure 5.13 shows measured S-parameters at bias point of 0.3V and 1.1mA, 2.9mA, and 4.3mA. The gain is typically 4.4dB and return loss is less than -7.9dB for the amplifier at bias point of 0.3V and 1.1mA. In the other bias points, the gain is 6.4dB and 7.6dB, respectively. The dc power consumption of this single stage amplifier is 870μW. This amplifier has typical gain of 6.4dB at this bias point. Figure 5.14 shows the output power 1dB compression characteristics to be -10.5dBm for a dc power consumption of only 330μW. The output third-order intercept point (OIP_3) characteristic of the amplifier is shown in Figure 5.15 which was measured at 24GHz using a two-tone test with 1MHz separation. The measured output IP_3 of the amplifier is +7.5dBm.

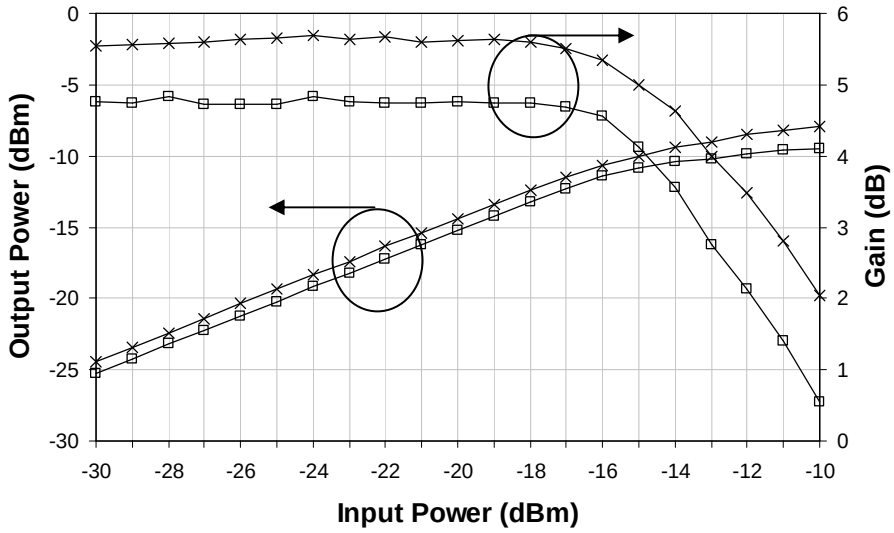


Figure 5. 14. P_{1dB} characteristic at 24GHz V_{ds}=0.3V, I_{ds}=1.1mA: simulation (×), measurement (□)

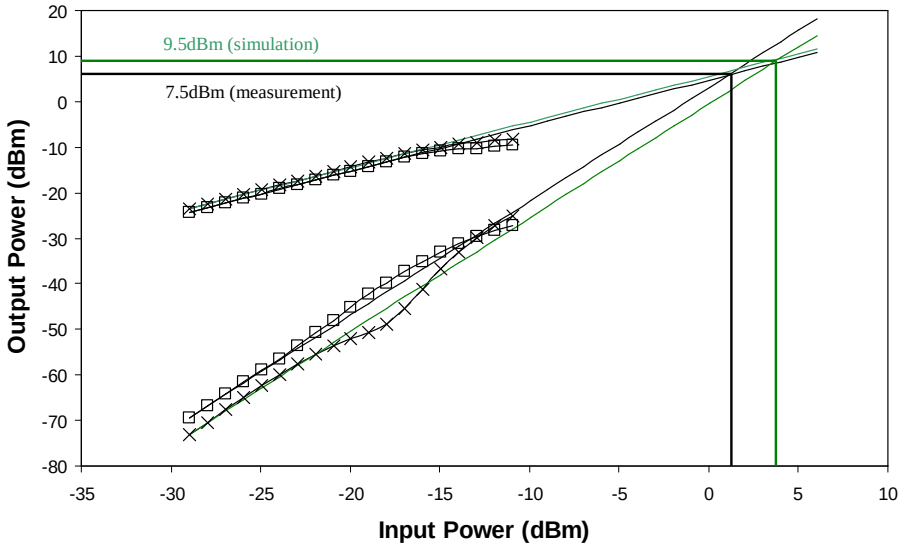


Figure 5. 15. IP_3 characteristic at 24GHz V_{ds}=0.3V, I_{ds}=1.1mA: simulation (×), measurement (□)

5.5 Envelope Detector

As mentioned in Chapter 3, there are two technologies using diode or cold-HEMT. A Schottky diode has generally been used for detector circuit with zero bias since this topology is simple and has zero power consumption. However, this topology has a disadvantage of low sensitivity as mentioned in Chapter 3. Thus, a novel low-cost, ultra-low power detector using a single cold-HEMT is designed for demodulation in this chapter.

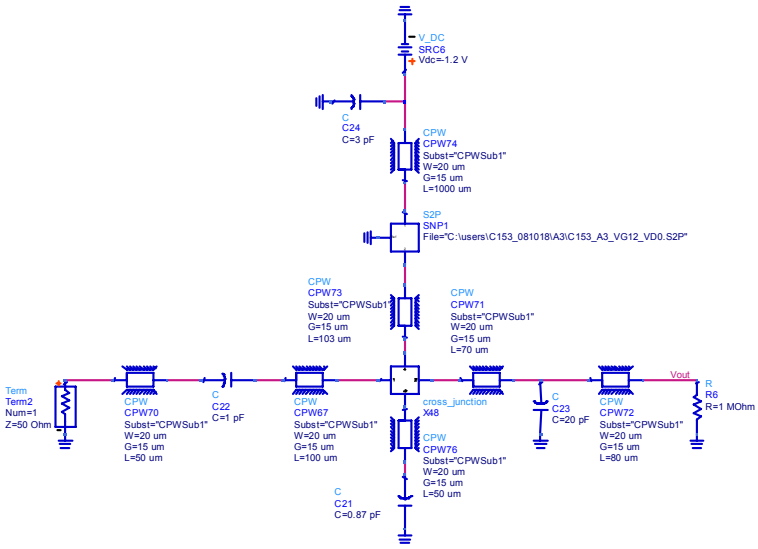


Figure 5. 16. Schematic of MHEMT detector

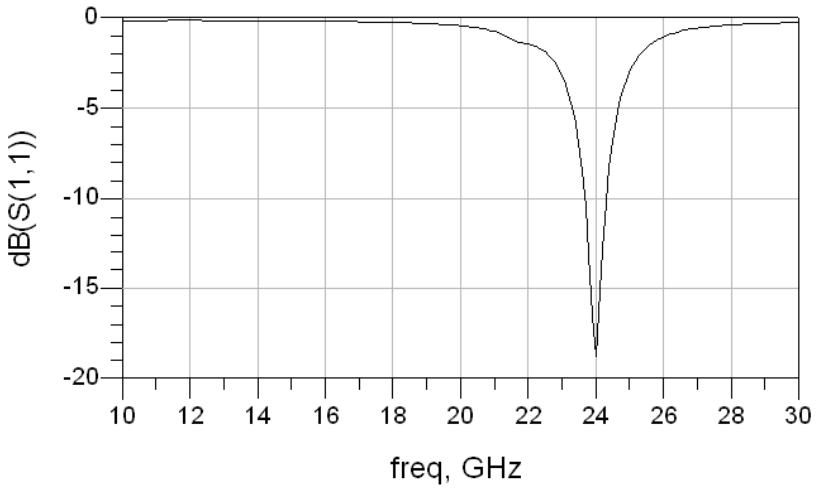


Figure 5. 17. Input matching performance of cold HEMT detector

The semiconductor device employed in the detector circuits is a 50nm gate-length GaAs MHEMT device. S-parameter measurements were first performed to determine the input impedance *Z1* of device in demodulation state. The circuits were designed for 24GHz

band operation and integrated on GaAs substrate with CPW transmission line, MIM SiN capacitor and NiCr resistor for matching and bias circuits. The load capacitor and resistor provides a load resistance so a voltage can be developed and it filters out any of the microwave signal present at the output. Figure 5.16 shows an ADS schematic of a MHEMT detector designed as outlined above. Figure 5.17 shows input matching performance of detector with cold-HEMT using Agilent ADS. Figure 5.18 shows the layout of a high sensitivity detector using a single cold-HEMT. The bias condition used is V_{gs} of -1.2V.

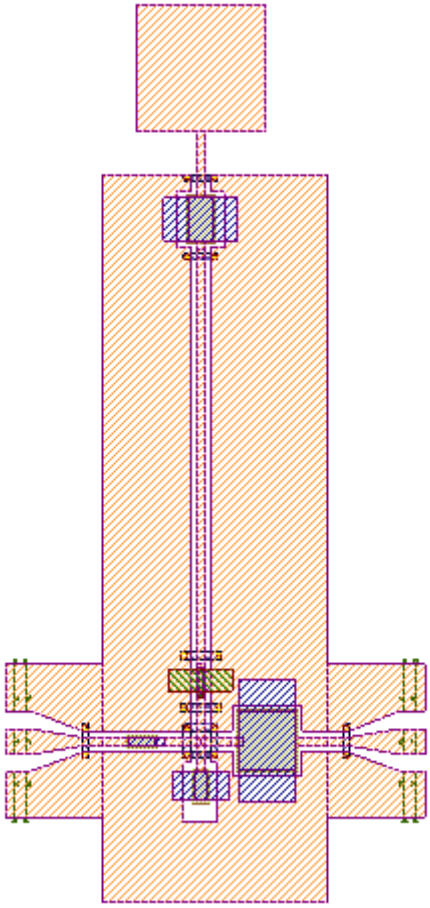
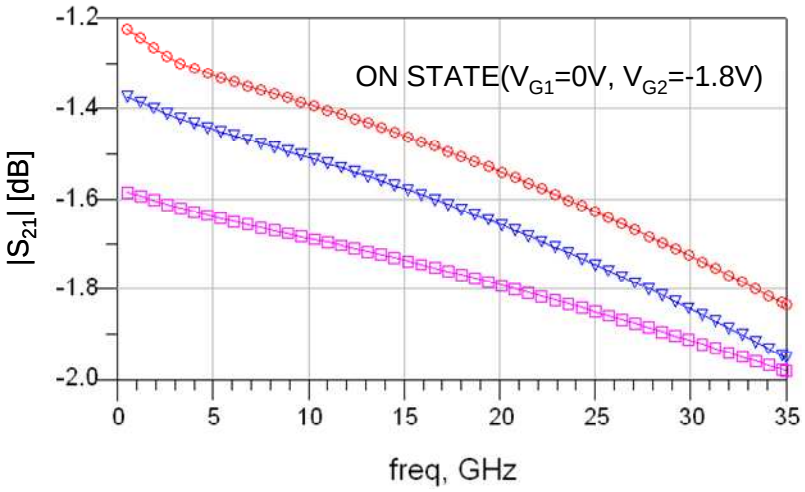


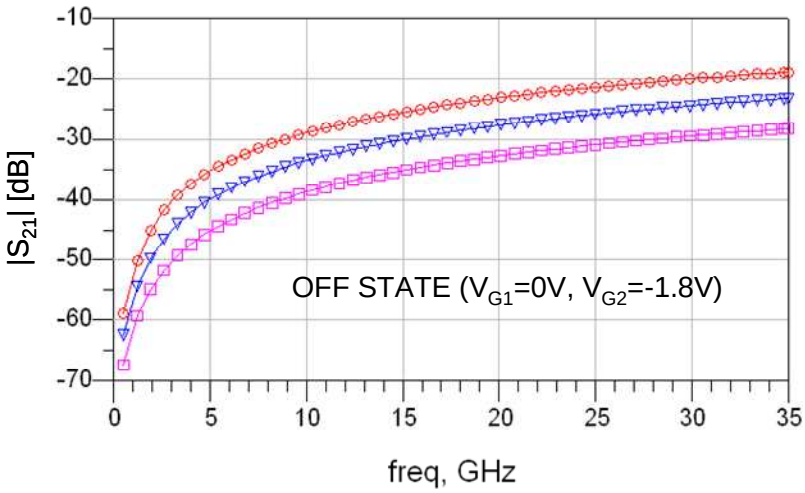
Figure 5. 18. The layout of MMIC detector using cold-HEMT

5.6 SPDT Switch

The design issues associated with the optimization of the series SPDT MHEMT switch are strongly influenced by choice of device width. Figure 5.19 shows insertion loss and isolation performances with different gate-widths of devices.



(a)



(b)

Figure 5. 19. Modelled transmission response in (a) ON-state and (b) OFF-state for 50nm GaAs MHEMT with different unit gate-width of 50µm (O), 25µm (∇) and 12.5µm (□)

Increasing the device width will result in smaller values of ON-state resistance R_{ON}, and therefore lower ON-state insertion loss. However, this reduction of insertion loss comes at the expense of reduced isolation in the OFF-state due to the increase of C_{ds} and C_{gs}. Therefore a trade-off for low loss, high isolation and circuit compactness is essential for high performance. Figure 5.20(a) show the schematic and layout, Figure 5.20(b) show simplified equivalent circuits of the MHEMT switch.

A single, two-finger MHEMT in a coplanar waveguide configuration was used as the switch and uses an optimal gate width of 25μm for low loss and high isolation. Independent bias of each gate finger controls the routing of the microwave signal from the drain terminal to one or other of the source terminals as shown schematically in Figure 5.20(a). This layout technique eliminates impedance mismatch and reduces transmission line interconnect loss [50]. Cold-HEMT operation is utilized to minimize power consumption. Figure 5.20(b) shows the equivalent circuits of the SPDT switch. In the ON-state, C_{ds}, C_{gs} and C_{gd} are not critical parameters compare with ON-state resistance (R_{ON}) therefore this equivalent circuit can simply be represented by R_{ON}. In the OFF-State, R_{OFF} is adequately large value for applying open circuit and consequently, C_{ds}, C_{gs} and C_{gd} are the dominant parameters for OFF-state switch performance [51]-[52]. Extracted values of R_{ON} and C_{OFF} for ON-state (V_g=0V) resistance and OFF-State (V_g=-1.8V) capacitance are 2~3Ω and 6~7fF, respectively. The circuitry controlling the gate bias included a 1kΩ resistor R_{ISO} to attenuate unwanted microwave signal leakage via the gates. Figure 5.21 shows an SEM microphotograph of the fabricated series SPDT MMIC switch with a 25μm unit width, 50nm gate-length MHEMT in CPW technology. The total chip area including probe pads is 1.5×1.2 mm^2.

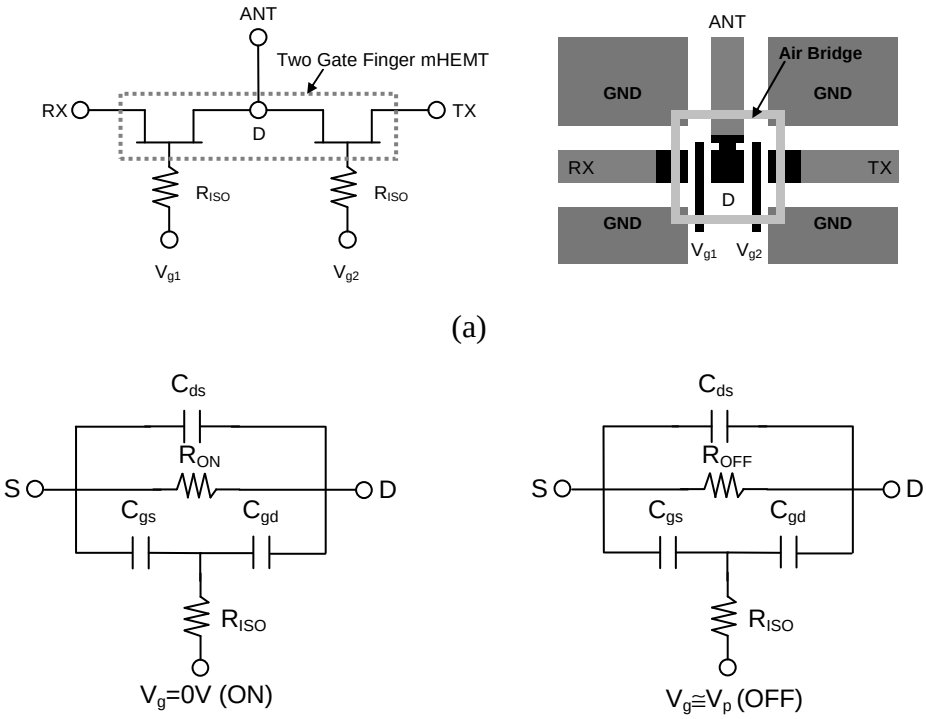


Figure 5. 20. Schematic and layout of SPDT switch circuit. (b) ON and OFF-states simplified equivalent circuit of the MHEMTs in the switch circuit

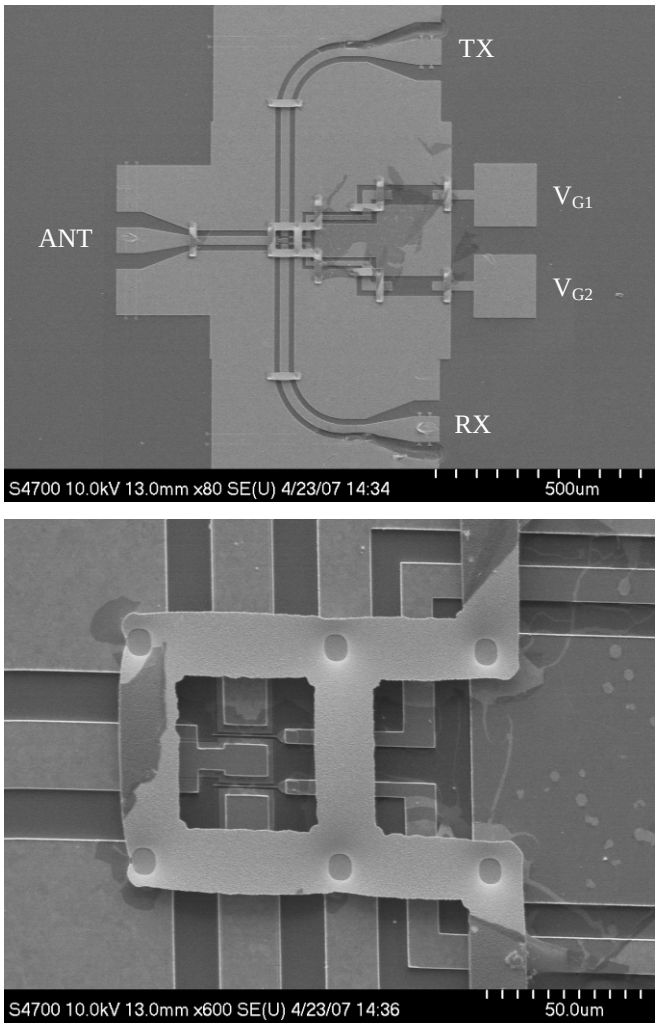


Figure 5. 21. SEM microphotograph of the fabricated SPDT MMIC switch

The switch was designed to achieve broadband characteristics from DC to 35GHz in order to cover a range of ISM bands being targeted. Figure 5.22 compares the simulated and measured insertion loss, isolation and return loss response of the MMIC switch utilizing the 25μm unit device width. Insertion loss is less than 1.9dB, isolation is greater than 27dB, and return loss is better than 12dB across the frequency range from DC to 35GHz. There is good agreement between simulated and measured results. Figure 5.23 shows the insertion loss and isolation response versus input power at 24GHz. The measured insertion loss degrades 1dB at the input power of +14dBm. The isolation starts to degrade at the input power of +11dBm and becomes 23dB when the input power reaches +15dBm. With signal input power of -10dBm, a leakage current of less than 1.3nA is observed. This dc power consumption in the ON-state is less than 0.1nW. The OFF-state voltage is -1.8V, with gate leakage current of less than 3.22μA, leading to a maximum power consumption of less than 6μW for the switch.

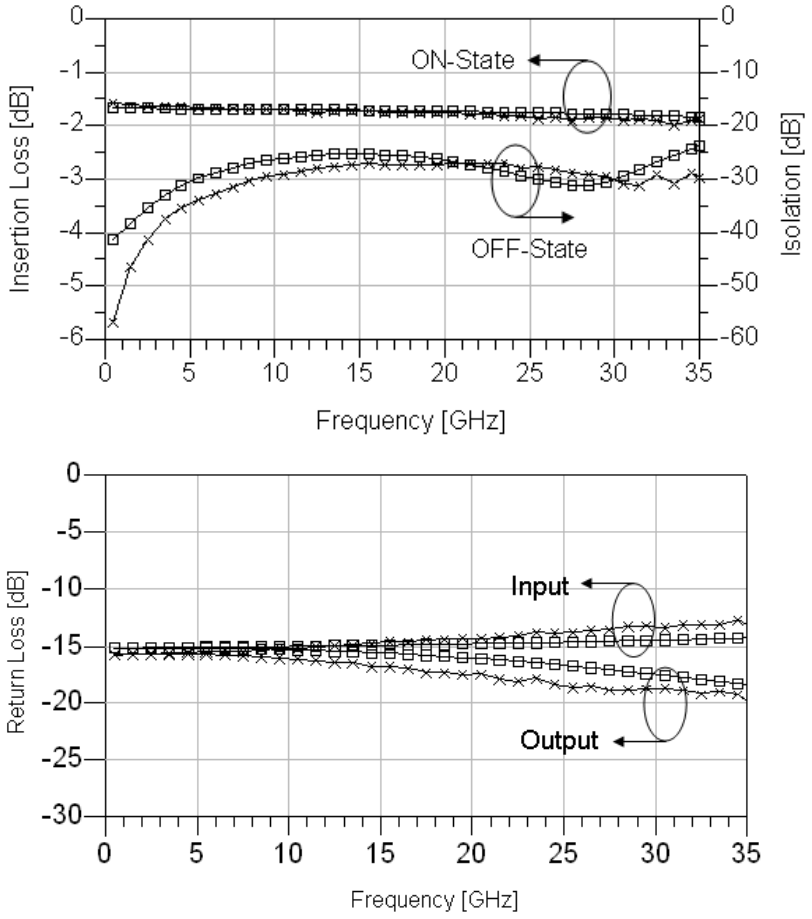


Figure 5. 22. Simulation and measurement results of series SPDT switch using 2×25μm, 50nm gate-length MHEMTs: Simulation (□) and Measurement (×)

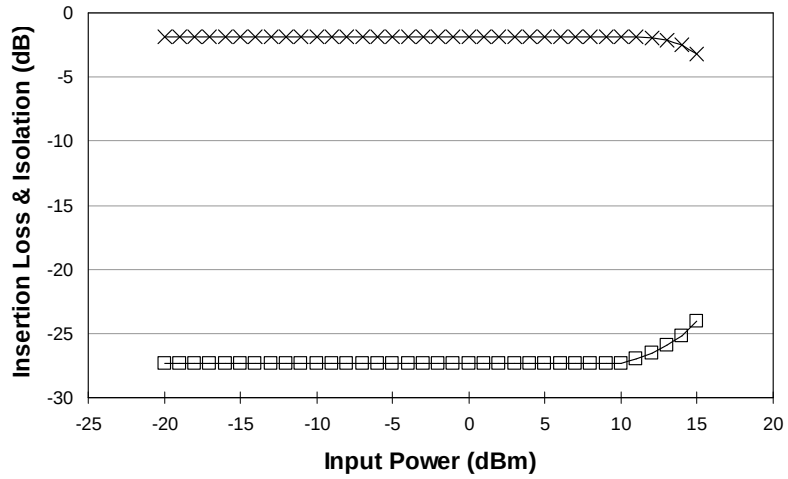


Figure 5. 23. Measured insertion loss and isolation versus input power at 24GHz: insertion loss (×), isolation (□)

5.7 Fully Integrated MMIC Radio Transceiver

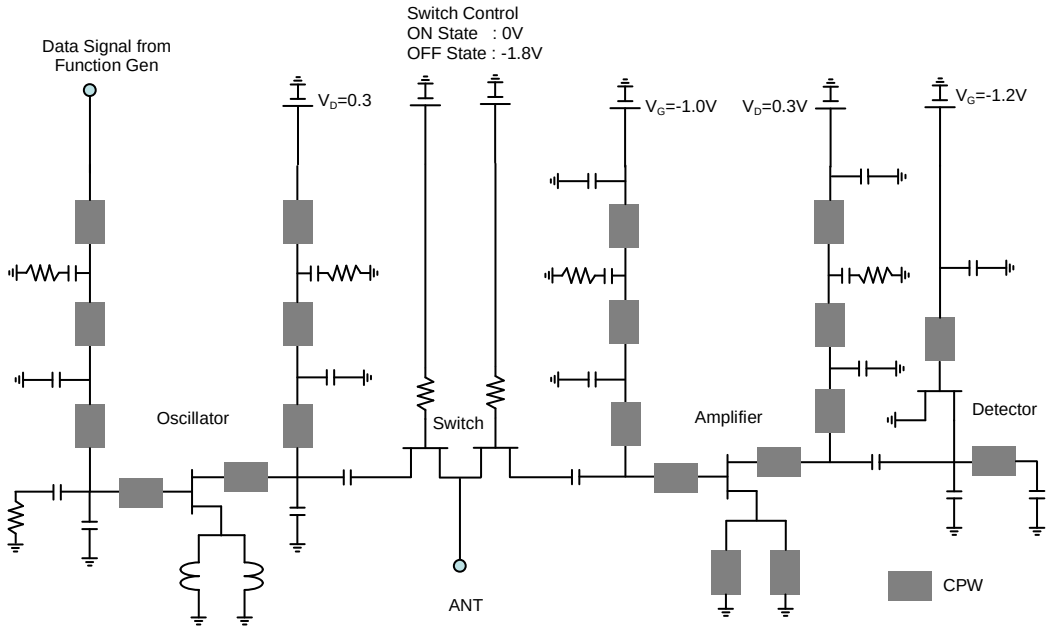


Figure 5. 24. The schematic of MMIC 24GHz radio transceiver

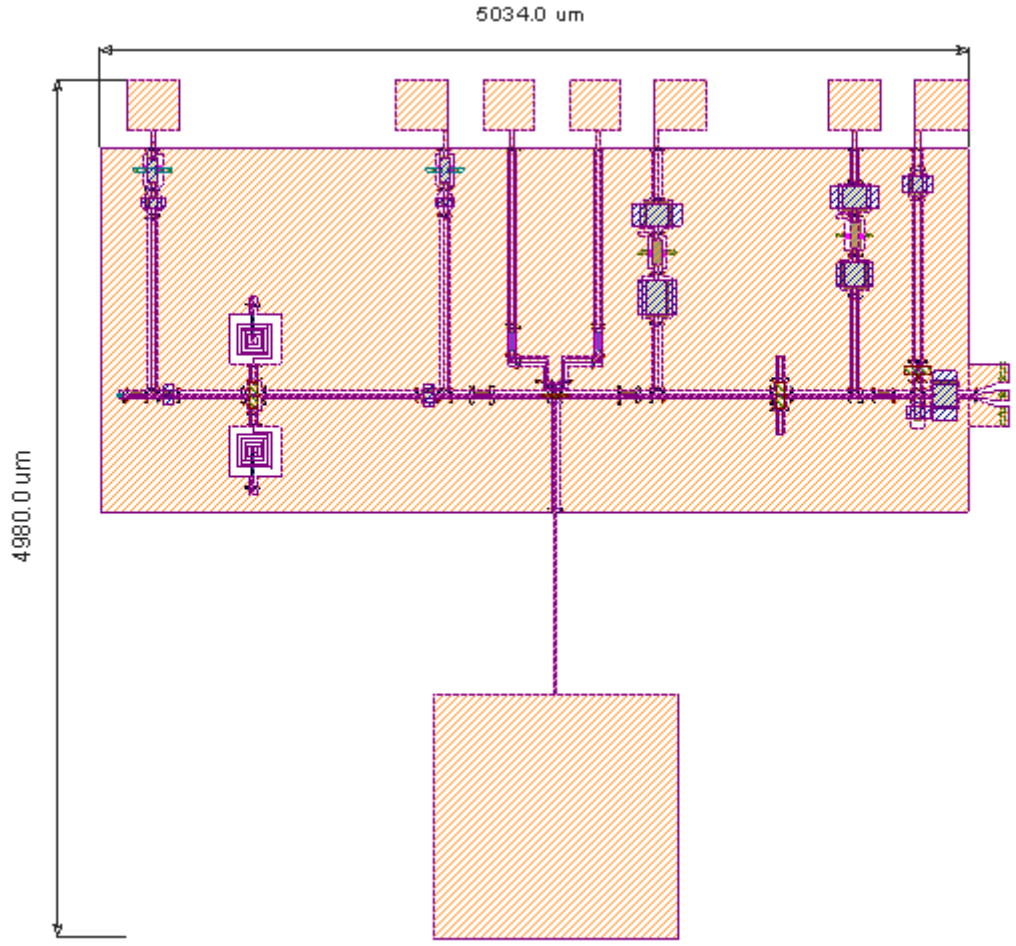


Figure 5. 25. Final integrated MMIC 24GHz radio transceiver with antenna

The radio building blocks that were designed in the previous section are integrated together to form the complete MMIC radio transceiver. Figure 5.24 shows a schematic of the fully integrated radio building blocks. The bias circuit of amplifier is changed to achieve a reduced size from first prototype using open circuit stub. Figure 5.25 shows the layout of the final transceiver integrated with the antenna. The power consumption is approximately 0.9mW for receiver and 0.5mW for transmitter. The antenna was designed by Dr Griogair Whyte and it has a gain of 2dBi at 24GHz. The final dimensions are 4.98×5.03 mm^2 while the transceiver consumes ultra-low dc power and operate at 24GHz. This fits into 5×5 mm^2 for SpeckNet project.

5.8 Conclusions

This chapter has presented a device technology and individual circuit design for MMIC radio transceivers based on libraries such as capacitors, inductors, tee-junction, cross-junction and impedance lines along with measured S-parameters and non-linear model for the active devices. The use of the library with simulation data has been validated in the Chapter 3 and 4 with the implementation of quasi-MMIC radio transceiver. A description of the MHEMT device using the advanced III-V technology in the University of Glasgow has been given and the measured S-parameters and non-linear model have been presented.

The non-linear TriQuint TOM3 model has been fitted to the measured S-parameters. It has been shown that excellent agreement is obtained between measured and modelled S-parameters for MHEMT device. Use of non-linear model provides an accurate design of oscillator and detector as shown in Chapter 3 and 4. With measured S-parameter and non-linear model, individual circuits have been designed using S-parameter and Harmonic Balance simulation method.

A switched oscillator as transmit oscillator has been designed to achieve an output power of -10dBm and power consumption of less than 0.5mW using 2×50μm MHEMT device and S-parameter and Harmonic Balance design method. Its performance is predicted for the operating frequency of 24GHz and has output power of -10dBm with an efficiency of 20%.

A MMIC amplifier operating at a centre frequency of 24GHz was designed as shown in Figure 5.12 exhibiting 6.4dB gain with return loss of less than -10dB while consuming only 0.9mW of dc power. To reduce the circuit size, the amplifier used shunt capacitors to implement bias circuits instead of open circuit stubs.

An envelope detector has been designed to obtain a target radio communication range with the same topology as a complete quasi-MMIC radio transceiver. The gate voltage is also optimized to achieve a large output voltage as 10GHz envelope detector.

A SPDT switch have been designed and fabricated by 2×25μm MHEMT device which is chosen to achieve a good performance from a comparison of several device dimensions. A SPDT switch has shown an insertion loss in the ON state of 1.9dB at 24GHz and the isolation in the OFF state of 27dB whilst the return loss is better than 12dB. The switch layout has been considered to improve the performance and reduce its size. The switch is compact and measures only 1.5×1.2 mm^2 including probe pads. The switch is passive and the gate current is less than 3.22μA.

The layout shows that all of individual circuit were successfully integrated on GaAs with an on-chip patch antenna provided by Dr Griogair Whyte. The overall chip size of 4.98×5.03 mm^2 fits the specification of 5×5 mm^2 at the operating frequency of 24GHz for SpeckNet.

Chapter 6

Novel Planar Filters

6.1 Introduction

In the previous chapters, details of active circuits for ultra-low power transceivers have been described. Another critical but optional building block in such transceivers is passive filters as shown in Figure 2.4. The receiver sensitivity is influenced by the frequency selectivity of the RF front-end, therefore, the sensitivity can be improved by using bandpass filter.

In this chapter, three bandpass filters concepts are demonstrated in MMIC and PCB process using semi-insulating GaAs and Rogers RO4350 substrates, respectively. No constraint was placed on the design frequency for these filters in order to ensure maximum generality.

W-band and G-band bandpass filter (BPF) have been designed on GaAs substrate with MMIC process of the University of Glasgow. A bandpass filter with wide out-of-band suppression has been designed with defected ground structure which makes it possible to use low phase noise oscillator with good out-of-band rejection characteristics on RO4350 substrate. Details of these filter circuits are explained in the next sections.

6.2 W-Band Bandpass Filter

Commercial applications such as passive imaging systems, inter-satellite communications, and collision avoidance radar are being developed using specific properties of free space propagation in the W-band frequency. In this frequency band, sophisticated filters are required in the development of high-performance millimetre-wave system for wideband and high speed data communication applications. In the design of planar BPFs, the major issue is realization of low insertion loss and high selectivity filtering performance to accomplish appropriate band selections by efficiently rejecting spurious signals and out-of-band noise. To realize high performance planar filters at W-band, sophisticated structures and advanced processes for achieving its structure are required. The interest in microstrip and coplanar waveguide (CPW) bandpass filters with sophisticated structure on GaAs substrate in this frequency band has been further increased

due to the realization of high performance, highly miniaturized and fully integrated MMICs. In W-band frequency, several planar filters have been recently reported [53]-[55]. Wide and narrow band planar filters at W-band have been presented by using traditional third-order quarter-wavelength shunt stubs and coupled-line resonators in coplanar waveguide (CPW) [55]. In this section, a W-band microstrip branch-line bandpass filter is proposed which exhibits high selectivity, low insertion loss, and simple structure that is compatible with monolithic integrated millimetre-wave circuits. This filter has been designed and fabricated on GaAs substrate and verified by simulation and measurements with good agreement up to 110GHz.

6.2.1 W-Band BPF Design

In this section, a bandpass filter structure that is based on the branch-line coupler in the W-band frequency is described. The details of the microstrip bandpass filter based on branch-line coupler are given in Figure 6.1.

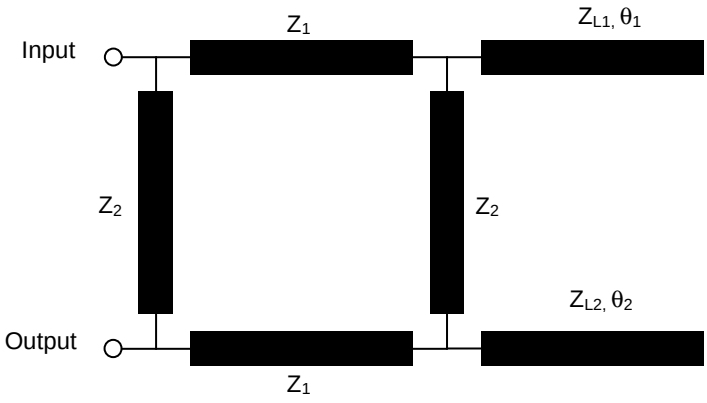


Figure 6. 1. Topology of microstrip bandpass filter based on branch-line coupler with open stub on coupled ports

The passband behaviour and out-of-band performance of the branch-line bandpass filter are strongly dependent on the characteristic impedance of design parameters such as Z_1, Z_2, Z_{L1}, and Z_{L2}. Thus, these parameters can be used for adjusting the main characteristics of the filter performance such as bandwidth, transmission zero point of lower and upper sides, and stop-band attenuation level. The best transfer function regarding close to passband selectivity and stop-band rejection performance is achieved by optimizing the lengths (θ_1 and θ_2) of the open-ended stubs [56]-[58]. The initial lengths of stubs are set to a half wavelength and five half wavelengths at the centre frequency, respectively [56]-[57]. The

characteristic impedance of open-ended stubs is chosen to satisfy the bandwidth specification for the bandpass filter.

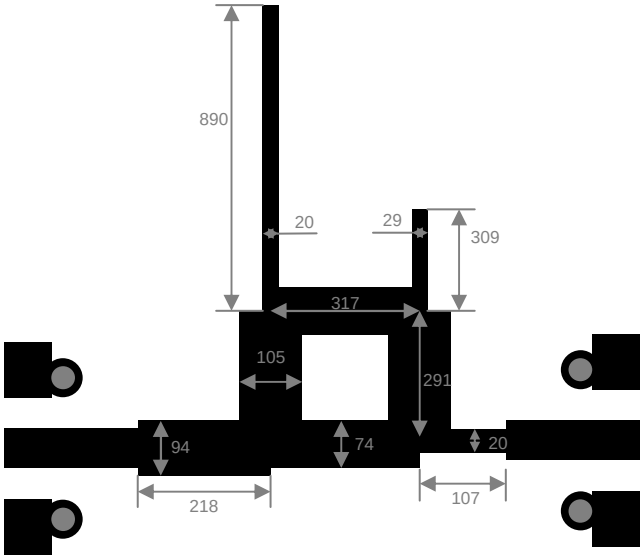
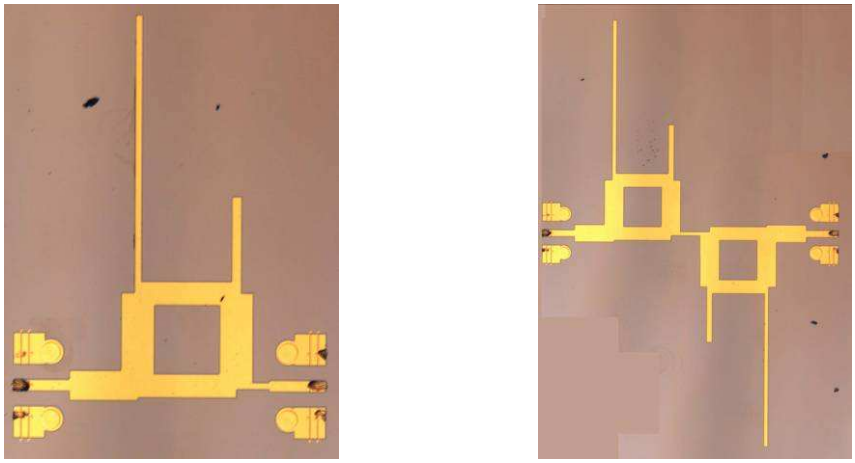


Figure 6. 2. The layout of proposed microstrip bandpass filter based on branch-line coupler with open stub (unit: μm)

The layout of a single-section branch-line filter with open-ended stubs on the coupled ports is shown in Figure 6.2 with the relevant physical dimensions. Two of these filter sections are directly cascaded and then the overall filter optimized as a unit using the design parameters of the single-section, the transmission line segment cascading the sections, and the filter input and output line. Consequently, the filter performance is also improved. For optimization of characteristic impedance and lengths of open-ended stubs, the commercial simulator Agilent ADS and Ansoft HFSS were used in the design and optimization of the filter.

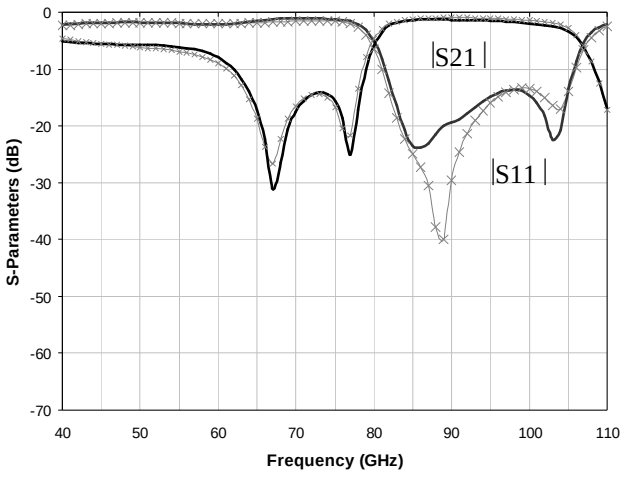
6.2.2 Simulation and Experiment Results

For an experimental demonstration, the designed filter was fabricated on 50μm thick GaAs substrate with relative dielectric constant of 12.9 and gold thickness of 1.2μm. Microphotographs of the fabricated single and two filtering sections are shown in Figure 6.3. As shown in Figure 6.3(b), overall filter has been accomplished by cascade connection of two filtering section based on branch-line coupler. The fabricated filters include input and output broadband CPW-to-microstrip transitions for probe measurement. Measurements were taken with the substrate placed on top of quartz and used LRRM calibration was used with an alumina impedance standard substrate (ISS).

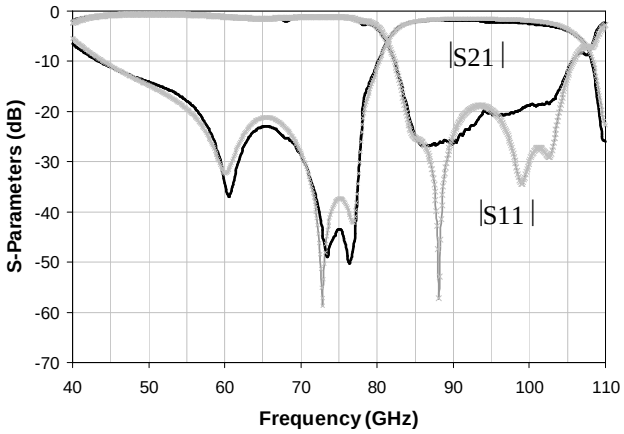


(a) (b)

Figure 6. 3. Microphotographs of (a) single-section filter and (b) overall filter based on branch-line directional coupler with open stub on coupled ports



(a)



(b)

Figure 6. 4. Frequency responses of (a) single-section filter, and (b) overall filter: simulation (×) and measurement (-)

Figure 6.4 shows the measured and simulated frequency responses from the fabricated single and two section filters. As shown in Figure 6.4(a), the measured 3dB bandwidth of a single section filter is from 81 to 107GHz, representing a fractional bandwidth (FBW) of 27% at the centre frequency of 94GHz. The insertion loss is less than 1.4dB at centre frequency. The measured return loss performance is more than 13dB. The out-of-band rejection level in both the lower and upper stop-band are below -15dB. The transmission zero on the lower side of the passband is around -25dB at 77GHz. As shown in Figure 6.4(b), the measured 3dB bandwidth of overall filter is from 81 to 107GHz, representing a FBW of 27% at the centre frequency of 94GHz. The insertion loss is less than 2.0dB at centre frequency. The measured return loss performance is more than 18dB. The out-of-band rejection level in the lower and upper stop-band are below -22dB. The transmission zero on the lower side of the passband is around -51dB at 76.4GHz. The proposed filter exhibits good bandpass behaviour as predicted by simulations. Its circuit size occupies only 1.6×2.4 mm^2. The filter design can be easily scaled to other frequencies.

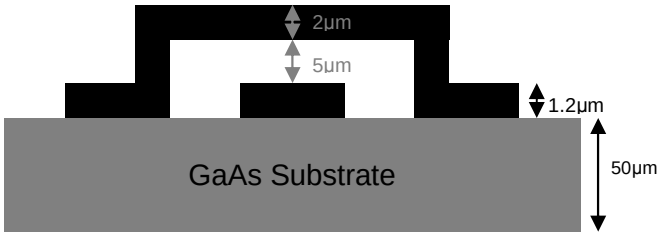
6.3 G-Band Bandpass Filter

The interest in narrow-band planar filter in G-band frequency range has increased due to the selectivity and performance requirements of applications such as passive imaging and inter-satellite communication systems. In addition, a narrow-band planar filter is required to have low loss and accurate bandwidth design. Beyond 100GHz, especially, the high resolution process appears as one of the most critical points. In the G-band frequency, several planar filters have been recently reported [53]-[54], [59]-[60]. To compare simulated and experimental results, traditional third-order quarter-wavelength shunt-stub filter has been presented with centre frequency of 165GHz [59]. The passive bandpass filters in Thin Film Microstrip (TFMS) technology for millimetre-wave application in the G-band frequency range have been realized on a BCB-based technology [60]. Narrow-band filter at G-band using photoimageable thick-film materials were presented in [53]. To compare between classical shunt-stub filter integrated in High Resistivity Silicon on Insulator (SOI) technology, standard CMOS and III-V technology, a bandpass filter in G-band frequency has also been designed [54]. This section presents a novel parallel coupled-line bandpass filter with branch-line shape in the G-band frequency range. This filter design uses open circuit stubs at the open end of parallel coupled-line and a half wavelength open circuit stubs on input and output coplanar waveguide (CPW) lines. The result is a more compact design that occupies an area of only 1×1.1 mm^2 and compatible to

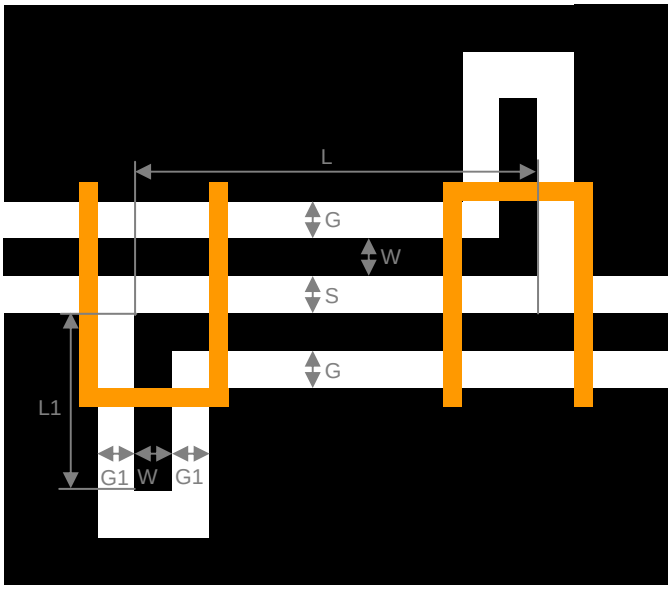
GaAs-based CPW MMIC devices. Moreover, this filter uses CPW technology on GaAs substrate without special materials or processes. Comparison with experimental results was performed up to 220 GHz.

6.3.1 G-Band Bandpass Filter Design

In this section, a fourth-order bandpass filter structure that is of narrow band performance in the G-band frequency range is developed. The geometric cross section of the CPW is shown in Figure 6.5(a). The layout of proposed unit parallel coupled-line resonator with open circuit stubs at the open end of conventional parallel coupled-line is shown in Figure 6.5(b).



(a)



(b)

Figure 6. 5. (a) G-band frequency CPW geometric cross section and (b) unit parallel coupled-line resonator with open circuit stubs

This configuration has the property of spurious suppression by adjusting the length of open-circuit stubs [61]-[63]. The initial lengths of stubs are set equal to a quarter-

wavelength (at double of centre frequency). The parallel coupled-line resonators are combined with branch-line shape with suitable lengths of coupled-line and open circuit stubs for performance of bandpass filter in desired frequency band.

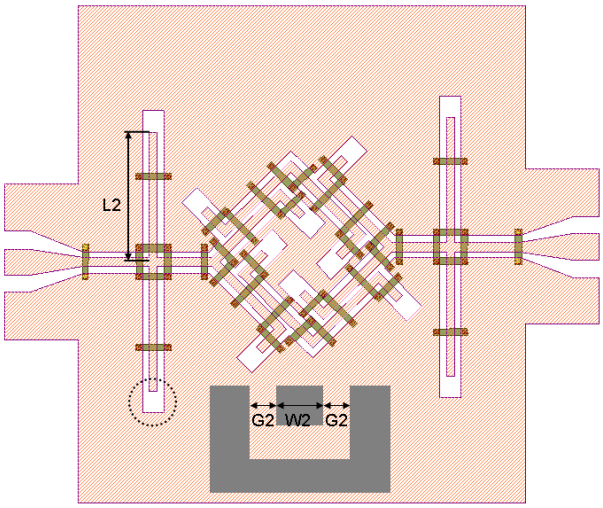


Figure 6. 6. The layout of proposed parallel coupled-line bandpass filter with branch-line shape

The combined parallel coupled-line filter with branch-line shape is shown in Figure 6.6. The physical dimensions of the parallel coupled-line planar filter with open circuit stubs are shown in Table 6.1.

Unit parallel coupled-line resonator with open-ended stubs						
W	G	S	L	W1	G1	L1
20	15	10	170	20	15	79
Open-circuit stubs on input and output ports						
W2	G2	L2				
20	15	300				

Table 6. 1. Physical dimensions of the parallel coupled-line bandpass filter with branch-line shape (unit: μm)

The parallel coupled-line filter with branch-line shape occupies less area because of its shape as hairpin resonator filter or ring resonator filter with coupled-line. The final structure also incorporates open circuit stubs of a half wavelength on input and output ports. These open circuit stubs enhance the rejection performance in the lower band because these stubs have a half wavelength at centre frequency. Moreover, the extension of the bandwidth at the desired centre frequency can be realized by these stubs. With this reduced

size compared to conventional coupled-line filters, this structure can realize a planar filter which has the narrow bandwidth and a high rejection of stop-band.

6.3.2. Simulation and Experiment Results

For an experimental demonstration, the designed filter with dimensions optimized by electromagnetic (EM) simulation of HFSS was fabricated on GaAs substrate which has relative dielectric constant of 12.9, dielectric thickness of 50μm, and gold thickness of 1.2μm. A microphotograph of fabricated planar filter is shown in Figure 6.7.

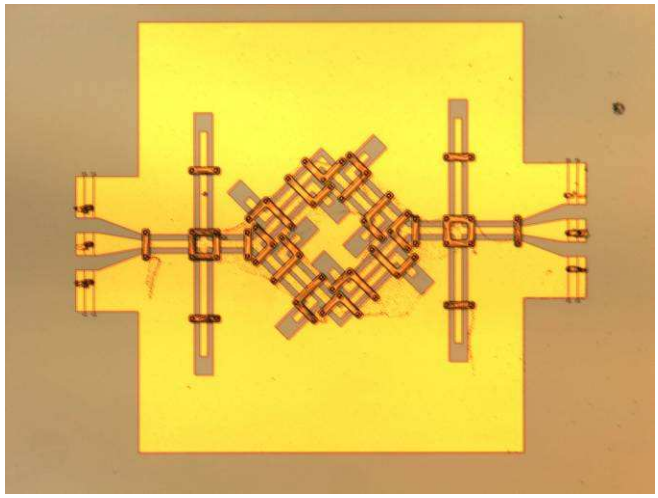


Figure 6. 7. Microphotograph of the parallel coupled-line bandpass filter with branch-line shape: The total chip size including probe pads is 1×1.1 mm^2

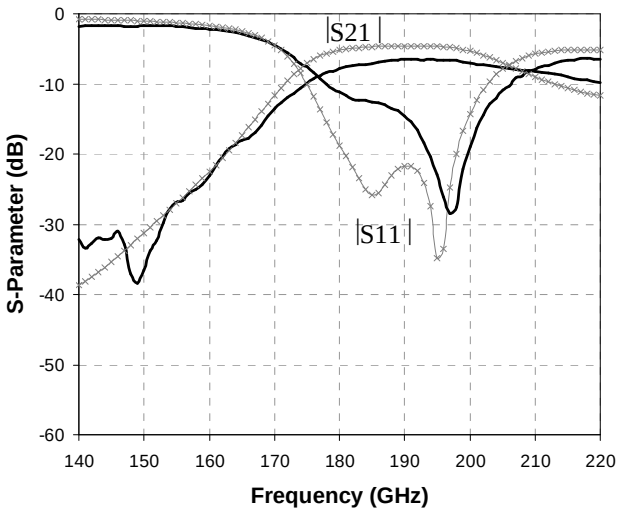


Figure 6. 8. Simulation and measurement results of parallel coupled-line bandpass filter with branch-line shape: simulation (×) and measurement (-)

The fabricated filter includes probe pads for on-wafer measurement and air-bridges for the common ground plane. Measurements were taken with the substrate placed on top of quartz and using LRRM calibration on an alumina impedance standard substrate (ISS). Figure 6.8 shows the measured and simulated S-parameter responses from fabricated planar BPF. The measured 3dB bandwidth is from 177 to 209GHz, representing a fractional bandwidth (FBW) of 17% at the centre frequency of 190GHz. The insertion loss is less than 6.5dB, which includes the input and output taper feed pads. The measured return loss (S11) performance is better than 12dB and out-of-band rejection level in the lower stop-band is below -30dB at 153GHz. The transmission zero on the lower side of the passband is about -38dB at 149GHz which is higher than simulation result due to a tolerance of placement. The measured S11 resonant frequency is 197GHz which matches well to the simulated value of 195GHz. The proposed filter exhibits good bandpass behaviour as predicted by simulations but it has the 2dB difference between measured and simulated passband insertion loss due to mismatch and taper feed probe pads.

6.4. Wide Bandpass Filter

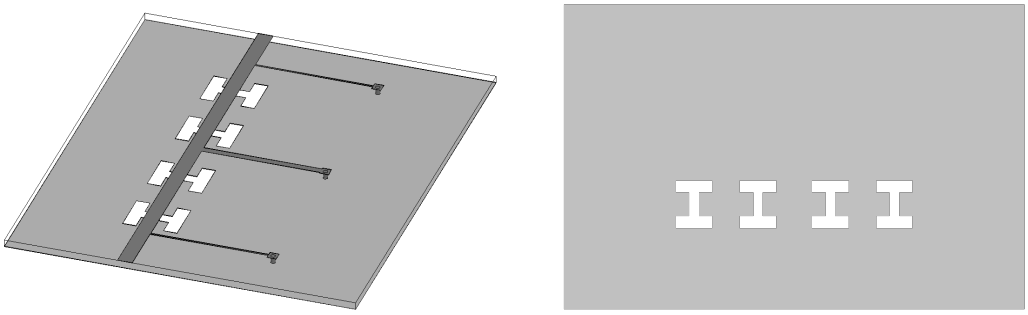
The interest in wide and ultra-wideband (UWB) bandpass filters have been increased due to the fast development of broadband communication systems. A wideband bandpass filter (BPF) is a very important passive component for broadband radio systems. To realize such wideband BPF, they are required to have ultra-wide bandwidth and low passband loss, a good harmonic out-of-band suppression, and at the same time have a good group delay performance for minimizing the distortion of pulse shape in the UWB system. It is very difficult to satisfy all these requirements simultaneously by conventional bandpass filter structure such as parallel coupling technique and a cascade structure of shunt stubs with quarter wavelength.

For the construction of ultra-wideband bandpass filters, several structures have been reported recently. For instance, the use of microstrip/coplanar waveguide [64]-[65], also BPFs using microstrip/slotline have been presented to achieve desired bandwidth, attenuation, and out-of-band suppression [66]. Broadside coupled microstrip/CPW structures have also been utilized to realize desired tight couplings for designing UWB filters, where either a half-wavelength or one full-wavelength long CPW resonators are used [67].

This section presents a new wideband BPF using a combination of a cascade of shunt stubs with equal length and defected-ground structures with equal shape. The filter uses

two defected-ground structures with lowpass filter property between shunt stubs. The filter shows a three-pole response with wideband harmonic out-of-band suppression. This filter also uses 50Ω impedance line for the signal line. The wideband bandpass filter with DGS patterns in the bottom ground plane was designed, fabricated and measured. Its structure and operation are described by electromagnetic (EM) simulated results and confirmed by experimental results.

6.4.1. Proposed Bandpass Filter



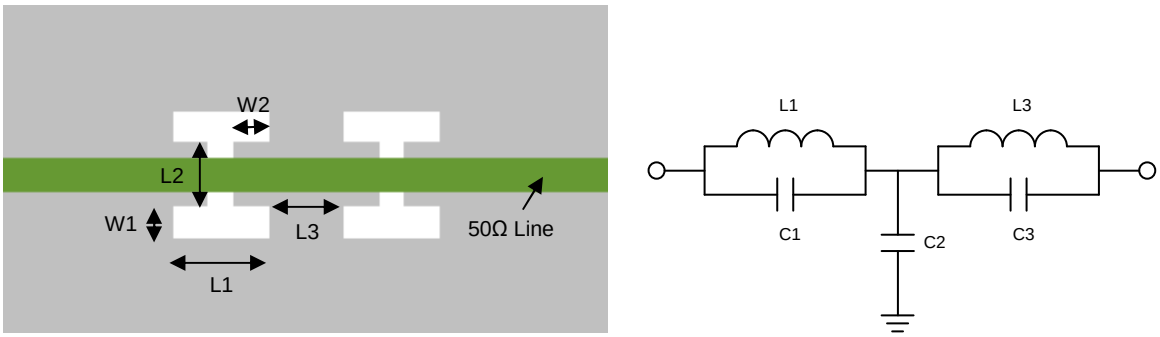
(a) (b)

Figure 6. 9. (a) Proposed wideband microstrip filter, (b) bottom view for the dumb-bell-shaped DGS

The schematic of the proposed wideband filter is shown in Figure 6.9(a), which is constructed on RO4350 substrate with a relative permittivity of ε_r = 3.66 and a thickness of h=0.762 mm. Dielectric and metallic losses, as well as the finite thickness of the metallic layers (T=35μm) were taken into account during design. The core part of the filter structure is a combination of three short circuit stubs which has the property of the wideband BPF [68], and a dumb-bell-shaped DGS pattern which fundamentally has the property of lowpass filter (LPF) when it is combined with microstrip line with the impedance of 50Ω [69]-[70]. As shown in Figure 6.9(a), dumb-bell-shaped DGS patterns are designed on the ground of the microstrip line, this then provides a very wide out-of-band suppression for wideband BPF. A bottom view for the dumb-bell-shaped DGS patterns is given in Figure 6.9(b).

The prototype wideband BPF of three short circuit stubs with centre frequency of 1.4GHz and stub length of 33° is designed. To determine the impedance values of the microstrip line and the short circuit stubs, the impedance values which are proposed in [71] were used. The impedance values were optimized to the impedance values of 124Ω and 80Ω for three short circuit stubs, respectively. The 50Ω impedance line was also used for

the microstrip line and this is applied to design of lowpass filter using dumb-bell-shaped DGS pattern.



(a) (b)

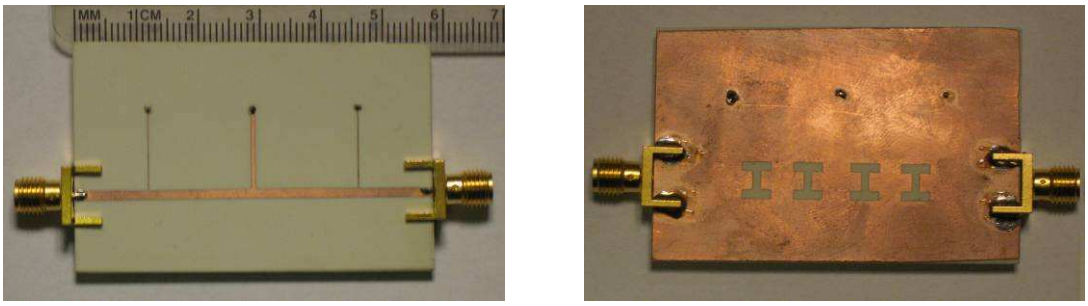
Figure 6. 10. (a) Schematic and (b) equivalent circuits of LPF with 50Ω microstrip line and periodic dumb-bell-shaped DGS patterns

The schematic of the lowpass filter with 50Ω microstrip line and the dumb-bell-shaped DGS pattern on the ground plane is shown in Figure 6.10(a). To realize a wideband BPF, a lowpass filter with cut-off frequency of 5.5 GHz was first designed. The dimensions shown in Figure 6.10(a) were optimized. An equivalent circuit of this LPF is shown in Figure 6.10(b). For wideband BPF, the physical length of 33° at 1.4GHz for the prototype BPF with three short circuit stubs and the line width of 50Ω impedance at the centre frequency of 3.5GHz are 12.9mm and 1.62mm, respectively. The line width of short circuit stubs by impedance values are 0.2 mm (two short circuit stubs in the in/out position) and 0.7 mm (a short circuit stub in the middle position), respectively. The LPF has dimensions of W1=1.47mm, W2=1.69mm, L1=4.6mm, L2=3.0mm, and L3=3.50mm by electromagnetic (EM) simulation. The wideband BPF which is combined with the prototype wideband BPF and dumb-bell-shaped DGS is also simulated by impedance values, physical length, and fixed dimensions of the prototype BPF and DGS pattern and achieves a good out-of-band suppression, the property of the wide passband, low insertion loss, and group delay simultaneously.

6.4.2. Simulation and Experiment Results

For an experimental demonstration, the designed filter with fixed dimensions by electromagnetic (EM) simulation was fabricated on RO4350 substrate which has relative dielectric constant of 3.66, thickness of 0.762mm, dielectric loss of 0.004, and metallic thickness of 35μm. The top and bottom views of the filter are shown in Figure 6.11(a) and

(b), respectively. The 50Ω impedance microstrip lines are extended for measurement purposes, while the actual size of the filter is only 34.5×15mm^2 on the substrate used.



(a) (b)

Figure 6. 11. Fabricated wideband BPF using dumb-bell-shaped DGS: (a) top view (microstrip) and (b) bottom view (DGS)

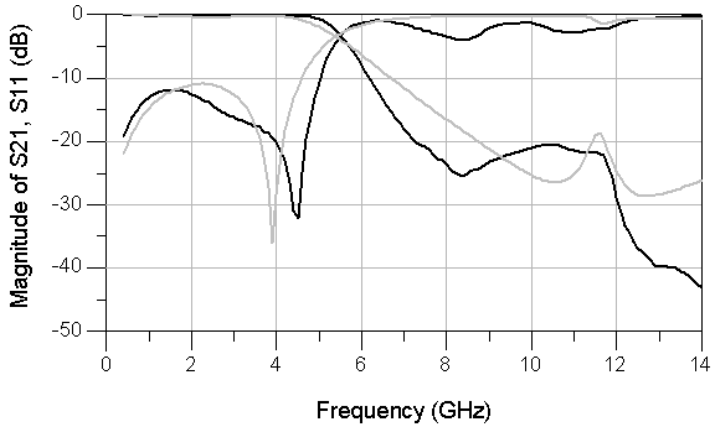


Figure 6. 12. Measured (black) and simulated (grey) results for the fabricated LPF using dumb-bell-shaped DGS

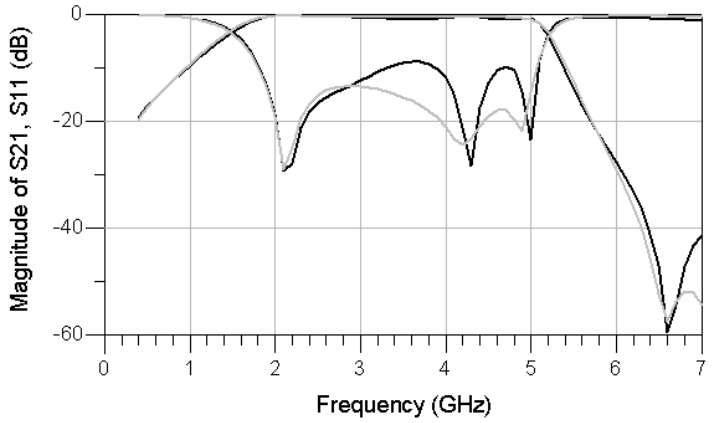


Figure 6. 13. Measured (black) and simulated (grey) S-parameter responses for the fabricated BPF with dumb-bell-shaped DGS on the ground plane

Measurements were taken using the E8362B microwave network analyzer. Figure 6.12 compares the measured and simulated S-parameter responses from the LPF. These results show a cut-off frequency of 5.5GHz and the insertion loss was measured to be 0.4dB including the loss from two SMA connectors. Figure 6.13 shows the measured and simulated S-parameter responses from the wideband BPF. The measured 3dB bandwidth is from 1.5 to 5.2GHz, representing a FBW of 105% at the centre frequency of 3.5GHz. The insertion loss is less than 0.9dB. The measured return loss performance is more than 9dB. This mismatch could be attributed to a misalignment between the top and bottom patterned circuits during fabrication.

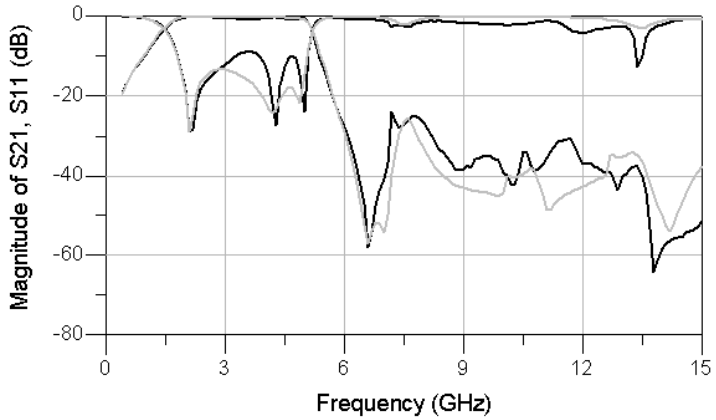


Figure 6. 14. Measured (black) and simulated (grey) out-of-band results for the fabricated BPF with dumb-bell-shaped DGS on the ground plane

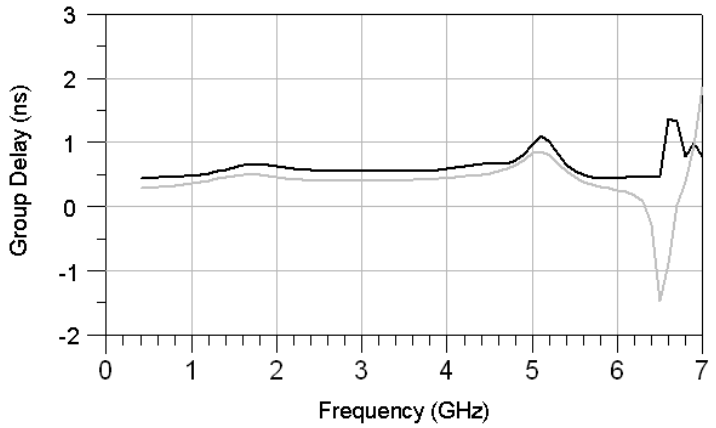


Figure 6. 15. Measured (black) and simulated (grey) group delay responses for the fabricated BPF with dumb-bell-shaped DGS on the ground plane

Figure 6.14 shows the measured and simulated out-of-band responses from the wideband BPF. Measured and simulated results of out-of-band suppression are greater than 24dB over a very broadband. The measured and simulated group delay responses of the

filter are plotted in Figure 6.15, where a good agreement between the two can be observed. The measured in-band group delay in the passband was only about 0.5ns.

In particular, the rejection-slope and out-of-band suppression characteristics of the proposed wideband BPF with DGS pattern on the ground are excellent even though it only has three poles. In the conventional design, much higher-order poles are required to get such level of skirt slope and out-of-band suppression. Also, it is true that the higher *N* leads to the higher the loss and the larger the size.

6.5 Conclusions

In this chapter, three novel compact filters with a sharp rejection or a wide out-of-band suppression for wireless communication applications have been introduced.

A W-band bandpass filter based on a microstrip branch line coupler has been designed using EM simulation and then fabricated using an MMIC process at the University of Glasgow. It has a good agreement between simulation and measurement results. The measured 3dB bandwidth of overall filter is from 81 to 107GHz, representing a FBW of 27% at the centre frequency of 94 GHz. The insertion loss is less than 2.0dB at centre frequency. The measured return loss performance is better than 18dB. The out-of-band rejection level in the lower and upper stop-band are less than -22dB. The transmission zero on the lower side of the passband is about -51dB at 76.4GHz. Its circuit size occupies only 1.6×2.4 mm^2. The proposed filter demonstrates low insertion loss with high selectivity compared to conventional coupled-line filters.

A G-band bandpass filter which used parallel coupled-line with branch line shape has also been designed using EM simulation and then fabricated on GaAs substrate using a MMIC process at the University of Glasgow. The filter demonstrates a high rejection performance of below -30dB and low insertion loss of 6.5dB with compact size compare to conventional coupled-line filter.

Wideband BPF with defected ground structure has been designed using EM simulation to achieve a wide out-of-band suppression and fabricated on RO4350 substrate using printed circuit board (PCB) process. The measured 3dB bandwidth is from 1.5 to 5.2GHz, representing a FBW of 105% at the centre frequency of 3.5GHz. The insertion loss is less than 0.9dB and the measured return loss performance is more than 9dB. Measured and simulated results of out-of-band suppression are greater than 24dB over a very broadband. The measured group delay in the passband was only about 0.5 ns.

The proposed bandpass filters has been demonstrated using optimized simulation and accurate fabrication process and have outstanding potential to realize a high performance millimetre-wave BPF and wide band BPF.

Chapter 7

Conclusions

7.1 Summary

This thesis has focused on the design and implementation of OOK radio transceivers which exhibit ultra-low power consumption, compact size and good performance for wireless sensor network applications. The sensor nodes must consume extremely low power, communicate with its neighbours at bit-rates of several hundred kilobits per second and potentially need to operate at high volumetric densities. Since the power constraint is the most challenging requirement, the radio transceiver must be ultra-low power in order to prolong the limited battery capacity. The radio transceiver must also be compact to achieve a target size of less than 5×5 mm^2 for each sensor node, and be able to operate over a range of at least one metre to allow nodes to be deployed sparsely. This thesis has demonstrated an OOK direct modulation/demodulation radio transceiver architecture that exhibits an ultra-low power consumption of 840μW, data rate of less than 200 kbit/s and communication range of greater than 1 metre to achieve the target specifications.

The direct modulation transmitter employs a switched oscillator without the need for pre-PA circuits like the traditional direct conversion transmitter and also substitutes the power hungry frequency synthesizer with an ultra-low power consumption oscillator. The transmitter oscillator consumes a dc power of 420μW with power conversion efficiency of 22% and delivers an output power of -10.4dBm. The transmitter oscillator directly generates OOK modulation signal by injecting data signal (0 and 1) on the gate terminal of the oscillator. The data rate is limited by the start-up time of the oscillator. Since the oscillator shows a start-up time of less than 5ns it is possible to realize data rate applications up to 200 kbps as required in the SpeckNet project.

The direct demodulation receiver employs a simple amplifier and envelope detector using a cold-HEMT to reduce power consumption by eliminating power hungry circuits. Since the availability of HEMT also is more flexible and the price is lower, the HEMT detector can be more cost effective than the GaAs Schottky diode detector. Based on this fact, the direct demodulation receiver achieves low cost and small size as well as ultra-low power consumption that is required to realize sensor node (speck) of SpeckNet project. The direct demodulation receiver consumes a dc power of 420μW as oscillator and shows the

detector output voltage of 1mV for an input power of -50dBm at the range of 1 metre that is required to establish communication between each node.

The direct modulation transmitter and demodulation receiver were integrated to implement an ultra-low power and small size OOK radio transceiver with a cold-HEMT SPDT switch to separate the transmitter signal from the oscillator and the receiver signal from the antenna. The transceiver showed a total dc power consumption of less than 900μW and this can be further reduced by approximately 50% by direct-modulation scheme in the transmitter since it has virtually no power consumption during data '0' state. Furthermore, the transceiver has more flexible operating range since it can be greatly increased by using gate voltage of the HEMT detector sacrificing virtually no power consumption.

By employing direct modulation and demodulation transceiver architecture and ultra-low power circuit design techniques, the work presented this thesis has shown the significant performance of radio transceiver for wireless sensor networks.

7.2 Future Works

The research work presented in this thesis has certainly allowed us to realize the potential of OOK radio transceiver for wireless sensor networks. However, much research is needed in the following areas to completely fulfil the potential of OOK radio transceiver.

Firstly, MMIC implementation of OOK radio transceiver is needed to further reduce the size of sensor node. Advanced device technology like MHEMT is needed to overcome the limitation of PHEMT device technology such as noise figure, gain and dc power consumption. Since the MHEMT device has low voltage operation, it can reduce dc power consumption by an order of magnitude compared with an equivalent GaAs PHEMT and InP HEMT. To achieve this goal, the fabrication of MMIC radio transceiver using MHEMT device is still undergoing fabrication by Dr Richard Oxland.

Next, to realize the full potential of OOK radio transceivers for wireless sensor networks, the operation range of transceiver needs to be increased while keeping a small size and ultra-low power consumption. As mentioned, the FET detector is improved with variation of operating gate voltage. Although the higher gate voltage in detector generates a bit distortion of detected signal, it can increase the communication range of transceiver by higher sensitivity of detector if it can be processed by baseband circuits. Therefore, the confirmation of performance with optimum integration between transceiver and baseband

circuits is needed to realize a high sensitivity of transceiver with no increase in power consumption.

Next, to improve the transceiver sensitivity, we can use the optional bandpass filter at the expense of increasing the size of radio transceiver. One of the novel filter topologies discussed in Chapter 6 can be used to improve the sensitivity with good signal-to-noise performance due to out-of-band performance.

Finally, the integration of transceivers with an energy-neutral platform is needed to efficiently use the limited energy of the battery with small size. It can allow us to realize ultra-low power and small size sensor node for wireless sensor networks due to the potential of ultra-low power and compact size radio transceiver.

With the above works, it becomes possible to achieve implementation of outstanding OOK radio transceiver for wireless sensor networks.

Appendix

The appendix shows the description of TOM3 model parameters [72].

Parameter	Description		
Ugw	Gate width to which model parameters are normalized		
Ngf	Number of gate fingers to which model parameters are normalized		
Vto	Threshold voltage		
Alpha	Saturation parameter in I_{ds} equation		
Beta	Transconductance (g_m) parameter in I_{ds} equation		
Lambda	Channel length modulation / output conductance		
Gamma	Coefficient for pinch-off change with respect to V_{ds}		
Q	Power generalizing the square-law for I_{ds} current		
K	Knee function power law coefficient		
Vst	Sub-threshold slope voltage		
Mst	Parameter for sub-threshold slope voltage dependence on V_{ds}		
Ilk	Reverse leakage saturation current – diode models		
Plk	Reverse leakage reference voltage – diode models		
Kgamma	Feedback coefficient for the internal VCVS		
Taugd	Series C_{tau}-R_{tau} time constant (implicit definition of R_{tau})		
Ctau	Dispersion model capacitance		
Qgqi	Low-power gate charge nonlinear term coefficient		
Qgqh	High-power gate charge nonlinear term coefficient		
Qgi0	Reference current in high-power gate charge nonlinear I_{ds} term		
Qgag	Low-power gate charge nonlinear term exponential coefficient		
Qgad	Low-power gate charge nonlinear term exponential V_{ds} coefficient		
Qggb	Transition coefficient for combined low-high power charge		
Qgcl	Low-power gate charge linear terms coefficient		
Qgsh	High-power gate charge linear V_{gsi} term coefficient		
Qgdh	High-power gate charge linear V_{gdi} term coefficient		
Qgg0	Combined low-high power additional linear terms coefficient		
Cds	Drain-source capacitance		
Tau	Transit time under gate		
Rd	Drain ohmic resistance		
Rg	Gate resistance		
Rgmet	Gate metal resistance		
Rs	Source ohmic resistance		
Is	Saturation current in forward gate current diode models		
Xti	Temperature exponent for saturation current		
Eg	Energy gap for temperature effect on I_s		

Publications

Hwang, C. -J., Lok, L. B., Thayne, I. G., and Elgaid, K., "W-Band Microstrip Bandpass Filter using Branch-Line Coupler with Open Stubs," *Microwave and Optical Technology Letters,* vol. 52, no. 6, pp. 1436-1439, 2010.

Hwang, C. -J., Chong, H. M. H., Holland, M., Thayne, I. G., and Elgaid, K., "DC-35 GHz low-loss MMIC switch using 50nm gate-length MHEMT technology for ultra-low-power applications," *IET Electronics Letters,* vol. 45, no. 12, pp. 632-634, 2009.

Hwang, C. -J., Lok, L. B., Thayne, I. G., and Elgaid, K., "Parallel coupled-line bandpass filter with branch-line shape for G-band frequency," *IET Electronics Letters,* vol. 45, no. 16, pp. 838-840, 2009.

Hwang, C. -J., McGregor, I., Oxland, R., Whyte, G., Thayne, I. G., and Elgaid, K., "An Ultra-Low Power OOK RF Transceiver for Wireless Sensor Networks", in *IEEE European Microwave Conference*, pp. 1323-1326, 29 Sep. - 1 Oct. 2009.

Hwang, C. -J., Lok, L. B., Thayne, I. G., and Elgaid, K., "A Wide Bandpass Filter with Defected Ground Structures for Wide Out-of-Band Suppression", in *IEEE Asia Pacific Microwave Conference (APMC)*, Dec. 2009.

McGregor, I., Lok, L. B., **Hwang, C. -J.**, Oxland, R., Whyte, G., Thayne, I. G., and Elgaid, K., "Low Complexity, Low Power, 10 GHz Super-Regenerative Transceiver", in *IEEE Asia Pacific Microwave Conference (APMC)*, Dec. 2009.

Lok, L. B., **Hwang, C.-J.**, Chong, H.M.H., Thayne, I. G., and Elgaid, K., "A W-Band MMIC Vector Modulator Utilizing Tandem Couplers and 50nm MHEMTs", in *IEEE European Microwave Conference*, pp. 1251-1254, 29 Sep. - 1 Oct. 2009.

Lok, L. B., **Hwang, C. -J.**, Chong, H. M.-H., Elgaid, K., and Thayne, I. G., "Measurement and Modeling of CPW Transmission Lines and Power Dividers on Electrically Thick GaAs Substrate to 220GHz", in *33rd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, 15 Sep. 2008.

Kian, K. S., Chong, H. M. H., **Hwang, C. J.**, Lok, L. B., Elgaid, K., and Kraft, M., "Development of a Low Actuation Voltage RF MEMS Switch," in *Eurosensors Conference XXVII*, Sep. 2008.

Hwang, C.-J., Lok, L. B., Thayne, I.G., and Elgaid, K.,"μ-Watt MMIC TX/RX for Wireless Sensor Applications," in *IET Seminar on RF and Microwave IC design*, London, Feb. 2008.

Lok, L. B., Elgaid, K., **Hwang, C.-J.**, Robertson, I. D., and Chongcheawchamnan, M., "Study of the Deleterious Effect of Common-Mode Behavior on CPS Branch-Line Couplers and Wilkinson Dividers," in *IEEE Asia-Pacific Microwave Conference*, pp. 2349-52, Dec. 2007.

References

[1] Rabaey, J., et al., "PicoRadios for Wireless Sensor Networks: The Next Challenge in Ultra-Low Power Design", *Digest of technical Papers, 2002 International Solid State Circuits Conference (ISSCC)*, pp. 200-201, Feb. 2002

[2] www.SpeckNet.org

[3] Steingart, D., Roundy, S., Wright, P., and Evans, J. W., "Micropower Materials Development for Wireless Sensor Networks," *Materials Research Society (MRS) Bulletin*, vol. 33, no. 4, pp. 408-409, Apr. 2008.

[4] Steingart, D., Ho, C. C., Salminen, J., Evans, J. W., and Wright, P., "Dispenser Printing of Solid Polymer-Ionic Liquid Electrolyte for Lithium Ion Cells," in *IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics (Polytronics 2007)*, pp. 261-264., Jan. 2007.

[5] Cook, B., "Low Energy RF Transceiver Design," Ph.D. Dissertation, University of California, Berkeley, 2007.

[6] Otis, B.P., "Ultra-Low Power Wireless Technologies for Sensor Networks," Ph.D. Dissertation, University of California, Berkeley, February 2005.

[7] RFM TRC103 868-960 MHz Transceiver Data Sheet. www.RFM.com, 2010.

[8] RFM TRC104 2.4GHz Transceiver Data Sheet. www.RFM.com, 2009.

[9] Texas Instrument CC1000 1GHz RF Transceiver Data Sheet. www.ti.com, 2007.

[10] Texas Instrument CC2420 2.4GHz RF Transceiver Data Sheet. www.ti.com, 2007.

[11] Daly, D. C. and Chandrakasan, A. P., "An Energy-Efficient OOK Transceiver for Wireless Sensor Networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003-1011, May 2007.

[12] Rappaport, T. S., *Wireless Communications: Principle and Practice*. Prentice Hall, 2nd Edition, 2002.

[13] IEEE Standard 802.15.4-2006, 2006.

[14] Lin, E.-Y., Rabaey, J., and Wolisz, A., "Power-Efficient Rendez-vous Schemes for Dense Wireless Sensor Networks," *IEEE International Conf. on Communications*, vol. 7, pp. 3769-3776, June 2004.

[15] Cho, S. and Chandrakasan, A. P., "A 6.5GHz CMOS FSK Modulator for Wireless Sensor Applications," in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 182-185, Jun. 2002.

[16] Pedram, M. and Wu, Q., "Design Considerations for Battery-Powered Electronics," in *Proc. 36th ACM/IEEE Conf. Design Automation (DAC'99)*, pp. 861-866, Jun. 1999.

[17] Wong, S., “Energy-Efficient Wireless Communication Protocols for Specknets”, Ph.D. Dissertation, University of Edinburgh, 2007.

[18] Cook, B., Berny, A., Lanzisera, S., Molnar, A., and Pister, K., “Low-Power 2.4-GHz Transceiver with Passive RX Front-End and 400-mW Supply,” *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757-2766, Dec. 2006.

[19] Friis, H. T., “A Note on a Simple Transmission Formula,” *Proc. IRE*, pp. 254-256, 1946.

[20] Datta, S., Ashley, T., Brask, J., Buckle, L., Doczy, M., Emeny, M., Hayes, D., Hilton, K., Jefferies, R., Martin, T., Phillips, T. J., Wallis, D., Wilding, P. and Chau, R., “85nm Gate Length Enhancement and Depletion Mode InSb Quantum Well Transistors for Ultra High Speed and Very Low Power Digital Logic Applications,” *IEEE Int. Electron Devices Meeting*, pp. 763-766, 2005.

[21] Thayne, I. G., Elgaid, K., Holland, M., McLelland, H., Moran, D., Thoms, S., and Stanley, C., “50nm GaAs mHEMTS and MMICs for Ultra-Low Power Distributed Sensor Networks Applications,” *Proc. on Indium Phosphide and Related Materials Conf.*, pp. 181-184, 2006.

[22] Yun, S. -J. and Lee, S. -G., “A 1mW Current-Reused CMOS Differential LC-VCO with Low Phase Noise,” *IEEE International Solid-State Circuits Conf. (ISSCC 2005)*, pp. 29-36, Feb. 2005.

[23] Han, S. W., “Single-MMIC Four-Channel Transmitter Module for Multichannel RF/Optical Subcarrier Multiplexed Communication Applications”, *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 4, pp. 1173-1178, Apr. 2002.

[24] Lin, Y. -T., Wang, T., Lu, S. –S and Huang, G. –W., “A 0.5 V 3.1 mW Fully Monolithic OOK Receiver for Wireless Local Area Sensor Network”, in *2005 Asian Solid-State Circuit Conf.*, pp. 373-376, Nov. 2005.

[25] McGregor, I., “Low power RF Transceivers”, PhD Dissertation, University of Glasgow, 2008.

[26] RFMD, “FPD200 General Purpose pHEMT Die Data Sheet,” Rev A1 DS090519.

[27] Hallgren, R. B. and Smith, D. S., “TOM3 Equations”, a document provided by TriQuint, Revised, 2 Dec. 1999.

[28] Hallgren, R. B. and Litzenberg, P. H., “TOM3 Capacitance Model: Linking Large- and Small-Signal MESFET Models in SPICE”, *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 5, pp. 556-561, 1999.

[29] Dambrine, G., Cappy, A., Heliodore, F., and Playez, E., “A New Method of Determining the FET Small-Signal Equivalent Circuit”, *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 5, pp. 1151-1159, 1988.

[30] Rhea, R. W., "Oscillator Design and Computer Simulation", Noble Publishing, 1995.

[31] Vendelin, G., "Design of Amplifier and Oscillators by the S-parameter Method," John Wiley & Sons, 1982.

[32] Guillermo Gonzalez, "Microwave Transistor Amplifier; Analysis and Design," Prentice Hall, 1984.

[33] Woods, D., "Reappraisal of the Unconditional Stability Criteria for Active 2-Port Networks in Terms of S-Parameters," *IEEE Trans. Circuits and Systems*, Vol. 23, No. 2, pp. 73-81, 1976.

[34] Fukui, H., "Available Power Gain, Noise Figure, and Noise Measure of Two-Ports and Their Graphical Representations," *IEEE Trans. Circuit Theory*, Vol. 13, No. 2, pp. 137-142, 1966.

[35] Yang, Z., Yang, T., Xie, J., and Xu, R., "The Design of a Ka-Band Two-Stage Monolithic Low Noise Amplifier," in *Proc. Asia Pacific Microw. Conf.*, 2005.

[36] Krekels, H.G., Schiek, B., and Menzel, E., "Power Detector with GaAs Field Effect Transistors," in *Proc. 22nd European Microwave Conference*, pp. 174-179, 1992.

[37] Ayasli, Y., Vourhaus, J., Pucel, R., and Reynolds, L., "Monolithic GaAs Distributed FET Switch Circuits," *IEEE GaAs IC Symposium*, 1981.

[38] Schindler, M.J. and Morris, A., "DC-40 GHz and 20-40 GHz MMIC SPDT Switches," *IEEE Trans. Microw. Theory Tech.*, vol. 35, no. 12, pp. 1486-1493, 1987.

[39] Toki, M. and Tsuzuki, Y., "Analysis of Start-up Characteristics of CMOS Crystal Oscillators", in Proc. *IEEE Frequency Control Symp.*, pp. 448-452, 1992.

[40] Lee, T. H., "The Design of CMOS Radio-Frequency Integrated Circuits", 2nd Edition, Cambridge University Press, 2004.

[41] Sze, S. M., "Physics of Semiconductor Devices", John Wiley & Sons, New York, 1969.

[42] Carrez, F. and Stolle, R., "Novel Low-Cost, Low-Power Modulator/Demodulator Using a Single GaAs Field Effect Transistor", *IEE Proc. Circuits Devices Syst.*, vol. 145, pp. 165-169, 1998.

[43] Hewlett Packard, "All Schottky Diodes are Zero Bias Detectors", Application Note 988, 1982.

[44] Moran, D.A.J., Boyd, E., Elgaid, K., McLelland, H., Stanley, C.R., and Thayne, I.G., "50nm T-Gate Lattice Matched InP-HEMTs with f_T of 430GHz Using a Nonannealed Ohmic Contact Process", in *Proc. 12th Gallium Arsenide and Other Compound Semiconductors Application Symp.*, pp. 311-314, 2004.

[45] Elgaid, K., McLellan, H., Holland, M., Moran, D.A.J., Stanley, C.R., Thayne, I.G., "50-nm T-Gate Metamorphic GaAs HEMTs with f_T of 440GHz and Noise Figure of 0.7dB at 26 GHz", *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 784-786, 2005.

[46] Varonen, M., Karkkainen, M., Kangaslahti, P., and Halonen, K., "Metamorphic HEMT Amplifier for K- and Ka-Band Applications", in *Proc. European Conf. on Circuit Theory and Design*, pp. 253-261, 2005.

[47] Lin, K.-Y., Deng, K.-L., Kuo, P.-W., Yang, S.-D., Wang, H. Chu, and T.-H., "K-Band Monolithic GaAs PHEMT Amplifiers", in *Proc. of Asia-Pacific Microwave Conf.*, pp. 153-156, 2000.

[48] Ma, B.Y., Bergman, J., Chen, P., Hacker, J.B., Sullivan, G., Nagy, G., and Brar, B., "InAs/AlSb HEMT and Its Application to Ultra-Low-Power Wideband High-Gain Low-Noise Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4448-4455, 2006.

[49] Fujimoto, S., Katoh, T., Ishida, T., Oku, T., Ishikawa, T., Sakamoto, S., and Mitsui, "A Ka-Band Ultra-Compact Low-Noise MMIC Amplifier", in *Asia-Pacific Microwave Conf.*, pp.638-641, 1987.

[50] Mizutani, H., Funabashi, M., Kuzuhara, M., and Takayama, Y., "Compact DC-60-GHz HJFET MMIC Switches Using Ohmic Electrode-Sharing Technology", *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 11, pp. 1597-1603, 1998.

[51] Schindler, M.J., Miller, M.E., and Simon, K.M., "DC-20 GHz N×M Passive Switches", *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 12, pp. 1604-1613, 1988.

[52] Lin, C.-K., Wang, W.-K., Chan, Y.-J., and Chiou, H.-K., "BCB-Bridged Distributed Wideband SPST Switch Using 0.25μm $In_{0.5}Al_{0.5}As$-$In_{0.5}Ga_{0.5}As$ Metamorphic HEMTs", *IEEE Trans. Electron Devices*, vol. 52, no. 1, pp. 1-5, 2005.

[53] Stephens, D., Young, P.R., and Robertson, I.D., "Millimeter-Wave Substrate Integrated Waveguides and Filters in Photoimageable Thick-Film Technology", *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 12, pp. 3832-3838, 2005.

[54] Prigent, G., Gianesello, F., Gloria, D., and Raynaud, C., "Bandpass Filter for Millimeter-Wave Application up to 220 GHz Integrated in Advanced Thin SOI CMOS Technology on High Resistivity Substrate", in Proc. on 37th *IEEE Euro. Microw. Conf.*, pp. 676-679, 2007.

[55] Rius, E., Prigent, G., Happy, H., Dambrine, G., Boret, S., and Cappy, A., "Wide-and Narrow-Band Bandpass Coplanar Filters in the W-Frequency Band", *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 784-791, 2003.

[56] Gomez-Garcia, R., Alonso, J.I., and Amor-Martin, D., “Using the Branch-Line Directional Coupler in the Design of Microwave Bandpass Filters”, *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 10, pp. 3221-3229, 2005.

[57] Lin, S.-C., Lin, Y.-S., and Chen, C.H., “Extended-Stopband Bandpass Filter Using Both Half- and Quarter-Wavelength Resonators”, *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 1, pp. 43-45, 2006.

[58] Tang, C.-W., and Chen, M.-G., “Wide Stopband Parallel-Coupled Stacked SIRs Bandpass Filter with Open-Stubs Lines”, *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 12, pp. 666-668, 2006.

[59] Wolf, G., Prigent, G., Rius, E., Demichel, S., Leblanc, R., Dambrine, G., and Happy, H., “Band-Pass Coplanar Filters in the G-Frequency Band”, *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 799-801, 2005.

[60] Prigent, G., Rius, E., Blary, K., Happy, H., Lepilliet, S., Dambrine, G., and Cappy, A., “Design of Narrow Band-pass Planar Filters for Millimeter-Wave Applications up to 220 GHz,” in *IEEE Int. Microwave Symp.*, pp. 1491-1494, 2005.

[61] Huang, X.D. and Cheng, K., “A Novel Microstrip Dual-Mode Bandpass Filter with Harmonic Suppression”, *IEEE Microw. Wireless Compon. Lett.*, vol. 16, no. 7, pp. 404-406, 2006.

[62] Hsieh, L.-H. and Chang, K., “Dual-Mode Quasi-Elliptic-Function Bandpass Filters Using Ring Resonators with Enhanced-Coupling Tuning Stubs”, *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 5, pp. 1340-1345, 2002.

[63] Cheong, P., Fok, S.-W., and Tam, K.-W., “Miniaturized Parallel Coupled-Line Bandpass Filter with Spurious-Response Suppression”, *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 5, pp. 1810-1816, 2005.

[64] Thomson, N. and Hong, J.-S., “Compact Ultra-Wideband Microstrip/Coplanar Waveguide Bandpass Filter”, *IEEE Microw. Wirelss Compon. Lett.*, vol. 17, no. 3, pp. 184-186, 2007.

[65] Baik, J.-W., Lee, T.-H., and Kim, Y.-S., “UWB Bandpass Filter Using Microstrip-to-CPW Transition with Broadband Balun”, *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 12, pp. 846-848, 2007.

[66] Li, R. and Zhu, L., “Ultra-Wideband (UWB) Bandpass Filters with Hybrid Microstrip/Slotline Structures”, *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 11, pp.778-780, 2007.

[67] Li, K., Kurita, D., and Matsui, T., “An Ultra-Wideband Bandpass Filter Using Broadside-Coupled Microstrip-Coplanar Waveguide Structure”, in *IEEE Int. Microwave Symp.*, pp. 675-678, 2005.

[68] Garcia, J.G., Bonache, J., and Martin, F., “Application of Electromagnetic Bandgaps to the Design of Ultra-Wide Bandpass Filters with Good Out-of-Band Performance”, *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4136-4140, 2006.

[69] Ahn, D., Park, J.-S., Kim, C.-S., Kim, J.-N., Qian, Y., and Itoh, T., “A Design of the Low-Pass Filter Using the Novel Microstrip Defected Ground Structure”, *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 1, pp. 86-93, 2001.

[70] Lim, J.-S., Kim, C.-S., Ahn, D., Jeong, Y.-C., and Nam, S.-W., “Design of Low-Pass Filters Using Defected Ground Structure”, *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 8, pp. 2539-2545, 2005.

[71] Hong, J.-S., and Lancaster, M.L., “Microstrip Filter for RF/Microwave Applications”, New York, Wiley, 2001.

[72] Agilent Technology TOM3 Model Parameter in ADS.