A SERIES FACTS CONTROLLER AS A VOLTAGE FLUCTUATION MITIGATION EQUIPMENT: AN EXPERIMENTAL INVESTIGATION

by

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Abstract

This research project addresses the mitigation of voltage fluctuations using a series-connected power electronics-based controller, which belongs to the family of Flexible AC Transmission Systems (FACTS) controllers. These are emerging technologies which have been under continuous development for over a decade, and are now available to the electricity supply industry world-wide, helping to ameliorate a wide range of power system phenomena, to increase power transfers and stability margins.

Voltage fluctuation is a complex phenomenon affecting adversely transmission and distribution networks. Bulky fluctuating load, wind farms and large induction motor are the major sources of voltage fluctuations. As the phenomenon propagates, it interacts with other voltage fluctuations contributed by different sources, and affecting neighbouring lighting circuits, giving raise to a phenomenon termed light flicker. To ameliorate such a problem, a well-coordinated operation of advanced voltage mitigation equipment, control strategy and specialised measurements instruments are required.

Considerable progress has been made in voltage fluctuations mitigation using shunt FACTS controllers. However, very little work has been reported in tackling the very complex issue of mitigation of voltage fluctuation propagating in the network using series FACTS controllers. To advance this area of research, this project addresses the design and construction of a three-phase scaled-down TCSC prototype and a voltage fluctuations experimental environment, suitable for real-time hardware-in-the-loop testing.

The research work carries out a fundamental study of TCSC resonances, which are termed resonance modes. It is found that a non-explicit resonance mode at α=90° exists, and it is termed intrinsic resonance mode. For a well-designed TCSC, only the fundamental and the intrinsic resonance mode should be active. To facilitate the design, a procedure has been identified, based in the synchronisation of resonance modes.

To achieve mitigation successfully, a new tailor-made TCSC control strategy, named RT-DIMR, and a flexible virtual flickermeter based on the IEC-61000-4-15 standard are thoroughly developed and integrated under the same real-time computing platform. The RT-DIMR demonstrates its capability for controlling the TCSC under different voltage fluctuation conditions. The IEC-Flickermeter provides online flicker severity indices, information which may be used to asses whether or not the electrical network has been effectively improved.

The aim of this research work is to experimentally evaluate the TCSC capabilities to mitigate travelling voltage fluctuations. A scaled-down network and voltage fluctuation sources are constructed to mimic a voltage fluctuations propagation environment. A comprehensive number of experiments are carried out to test the mitigation scheme under a wide range of conditions.

The robustness and effectiveness of the mitigation schemes have been thoroughly demonstrated. The newly developed TCSC prototype, scaled-down testing environment and RT-DIMR control strategy recommend themselves not only as an imaginative voltage fluctuations mitigation research tool, but also as a general advanced FACTS research tool.

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Abbreviations

FACTS	Flexible AC Transmission Systems
TCSC	Thyristor Controlled Series Capacitor
EAF	Electric Arc Furnace
DC-EAF	Dc Electric Arc Furnace
IFS	Instantaneous Flicker Sensation
P_{st}	Short-Term Flicker Severity Index
IEC	International Electrotechnical Commission
OSS	Operating Support System
SIM	Sensors Interface Module
AMS	Automatic Magnitude Stabiliser
SUVM	Signal Conditioning and Step-Up Module
PATCM	Phase Angle Triggering Control Module
RT-DIMR	Real-Time Dynamic Instantaneous Mitigation Response
SSR	Subsynchronous Resonance

HIL	Hardware-in-the-Loop
AFT	Actual Frame Time
RTS	Real Time Station
VTR	Voltage Triggering Reference
CTR	Current Triggering Reference
CCR	Capacitive- Capacitive TCSC operation
CIR	Capacitive- Inductive TCSC operation
IIR	Inductive-Inductive TCSC operation
FSC	Flicker Sensitive Customer
RVF	Residual Voltage Fluctuations
PCC	Point of Common Coupling
VFMF	Voltage Fluctuation Mitigation Factor
FCSC	Flexible Custom Series Controller

CHAPTER

1

INTRODUCTION

1.1 MODERN TRANSMISSION AND DISTRIBUTION ELECTRICAL SYSTEMS

Electrical power systems are undergoing a profound transformation worldwide, owing to market, regulatory, and environmental pressures. It is envisaged that systems will continue to grow to meet increasing demand to keep pace with population and industry expansion, and continued economic development around the world. For many years, the solutions adopted in power systems to meet the challenges imposed by increasing demand have implied one or more of the following actions:

- The addition of generating stations and transmission lines and transformers.
- The use of conventional controlling devices such as series capacitors and rapid switching breaking resistors.
- Operator actions such as load shedding are also used, but only as a tool of last resort.

In the era of over-engineered electrical power systems, electro-mechanical controllers served their intended duty quite well. However, in the present climate of privately owned and operated electrical power networks, conventional transmission systems are seen nowadays as exhibiting undesirable characteristics, such as [1]:

- Significant power losses over long distances
- Unwanted active power flow loops in parallel paths in several parts of the network
- Several forms of stability problems: Transient stability, steady state stability, and subsynchronous resonance
- Voltage limits problems leading to either voltage collapse or overvoltages
- Operation of transmission lines well below their thermal limits
- Cascade tripping
- Long restoration times

In the context of distribution systems, most current problems are related to the quality of electrical energy supplied to the customer. If the energy supplied to a customer with sensitive loads contains high levels of harmonic distortion, or any other undesirable phenomena such as interruptions, sags, or swells, the load may be damaged or the industrial process halted, representing a financial loss to the customer and to the utility.

As a result of such circumstances, as well as the ever increasing environmental land use and regulatory laws constraints, which makes it difficult to built new generation and transmission facilities, electric utilities are being forced to get a better utilisation of their existing assets. The solutions provided must, at the same time, improve the stability and reliability of the power system. Historically, a major preoccupation of the electricity supply industry has been to utilise transmission corridors fully. Two distinct lines of action have emerged from this objective

- To increase safely the power transfer capability of transmission networks
- To provide direct control of power flows over designated transmission routes

This has been achieved with the use of mechanically controlled series compensation and conventional phase-shifting transformers, respectively. However, over the last two decades, the major manufacturers of electrical equipments and utilities have been working around two innovative technologies: Flexible AC Transmission Systems and Custom Power. These concepts were first conceived in the late 1980s by Dr. N.G. Hingorani [2] at the Electric Power Research Institute (EPRI), Palo Alto, CA.

From the operational point of view, the technology provides the necessary correction to control the path of power flows along designated routes while, at the same time, minimise the gap between the stability and thermal limits. FACTS is an acronym for

"Flexible Alternating Current Transmission Systems", a relatively new concept in power systems which incorporates power electronics and microprocessor-based controllers whose main objective is to enhance the controllability of the network and to increase the power transfer capability.

1.2 FACTS AND CUSTOM POWER CONTROLLERS: A REVIEW

FACTS and Custom Power applications use the latest high-speed power electronics technology, modern control theory and advanced processors. FACTS controllers are connected to the high-voltage side of the transmission network to provide the necessary transmission line parameters compensation, in an adaptive fashion, to control the power flow in key transmission paths. These controllers have the ability to control the voltage magnitudes, the line impedance and the angles at the line ends of key transmission corridors, and, at the same time, enhance the security of the system.

Research organisations and manufacturers have participated very actively in developing FACTS and Custom Power technologies. EPRI has sponsored FACTS research programs for over a decade. Its development program involves full-scale demonstrations of FACTS controllers. To date, the most widely cited FACTS installations are:

- 330 MVAr TCSC at Kayenta Substation
- 208 MVAr TCSC at Slatt Substation
- ±100 MVAr STATCOM at Sullivan Substation
- ±160 MVA shunt and ± 160 MVA series UPFC at Inez Substation
- ±200 MVA static converter at Marcy Substation

The many advantages of the TCSC technology over conventional series compensation solutions have made this technology the preferred option in today's electric utilities.

Application areas relating to TCSC power systems studies have grown steadily over the last few years such as:

- Steady and transient stability studies
- Control of power flow analysis
- Voltage collapse studies
- Improvement of transmission and distribution system operation

- Mitigation of subsynchronous resonance
- Protection relaying for FACTS compensated lines
- Damping of power oscillations
- Investigation on improvements of TCSC performance

The first full-scale TCSC transmission systems have been installed in the United States; these are the 230 kV Kayenta substation and the 500 kV Slatt substation. Other TCSCs are now installed in Sweden and Brazil.

In the academic environment, there are a number of universities around the world generating new valuable research contributions in the area of FACTS and Custom Power. In particular, researchers at CERPD, at the University of Glasgow, have been contributing to FACTS and Custom Power controllers modelling as well as the development of scaled-down prototypes for quite some time [3-5]. Moreover, an advanced SVC prototype has been built at the University of Manchester [6]; including an application to voltage sag mitigation [7]. In Chalmers University of Technology, Göteborg Sweden, work has been reported on control strategies and digital modelling of voltage source converter for application to wind generation and sag mitigation [8-11].

A small single-phase TCSC prototype has been built in the University of Natal, South Africa to be used as a teaching tool [12]. In Southeast University, Nanjing, China, a single-phase TCSC prototype has been constructed in co-operation with University of Bath to study SSR mitigation schemes [13,14].

Three-phase TCSC prototypes for academic purposes are seldom reported in the open literature, two examples are the one built in Tsinghua University, Beijing, China [15], and in Kyoto University, Japan [16]. These controllers are discussed in more detail in Chapter 5.

1.3 VOLTAGE FLUCTUATIONS IN ELECTRICAL SYSTEMS: MEASUREMENT, PROPAGATION AND MITIGATION APPARATUS

1.3.1 Voltage Fluctuations, Light Flicker and Flickermeter

Voltage fluctuation is a class of power quality phenomena affecting adversely the electrical network, where the voltage magnitude cyclically deviates from the system nominal rating. Moreover, the voltage fluctuation propagates in the electrical network

affecting residential, commercial and industrial lighting circuits. This phenomenon may induce fluctuations in the light intensity of incandescent and fluorescent lamps giving rise to a phenomenon perceived by the naked eye termed light flicker or flicker. Depending on the frequency and magnitude of the intensity of the light fluctuations, the flicker perceived by an average individual varies from mild to very irritating sensations. At high flicker dosages, above a threshold limit, over a given period, the number of customer complaints to the utility company begins to increase.

The electronic instrument utilised to quantify the voltage fluctuation and the light flicker level is commonly referred to as flickermeter. Different kinds of flickermeters, using different definitions, are available; the flickermeter based on the standard IEC-6100-4-15 [17], gives accurate flicker perception levels and includes guidelines for the construction of the instrument. The statistical method used to evaluate the severity of flicker irritation over short and long observation intervals is also included in the standard; the former is termed short-term severity index, P_{st}, and the latter long-term severity index, P_{lt}.

1.3.2 Source of Voltage Fluctuation and Propagation Phenomena: A survey

The sources capable of producing voltage fluctuations are mainly the rapidly fluctuating loads. The current drawn by the load and the short-circuit level of the network at the point where the load is tapped-off play a key role in determining the voltage deviation from its nominal value. A neighbouring residential circuit may experience higher voltage fluctuations and flicker if the distribution feeder is weak [18].

Arguably, the electric arc furnace is the most common source of voltage fluctuation in today's electrical systems. Additionally, DC electric arc furnaces [19] and some kinds of embedded generators [20], especially large wind generator installations, are also contributors of voltage fluctuations. Some other sources of voltage fluctuation are identified in distribution systems, such as: industrial wood chipping mills, lumber mills, welder machines, plasma torches and heat pumps.

The voltage fluctuation produced by a given source is normally calculated by measuring P_{st} at the point of connection with the electrical network. As the voltage fluctuation propagates throughout the electrical network, at all voltage levels, the overall influence of voltage fluctuations in an electrical system must be assessed. Published work

addressing voltage fluctuation propagation phenomena is limited [21-23]. However, the study of propagation of voltage fluctuation in electrical systems is beyond the scope of this research project.

1.3.3 Voltage Fluctuation Mitigation: Conventional and Modern Practices

1.3.3.1 Mitigation Solutions

In electric arc furnace installations, voltage stabilisation at the point of common coupling has been a major preoccupation for many years [24]. This is also the case for other plant equipment such as DC electric arc furnaces and wind farms. Utilities and residential customers both obtain common benefits from voltage stability improvements and reduction of voltage fluctuation, which is amenable to a lower P_{st} in the electrical network.

In general, voltage stabilisation improvement and voltage fluctuation reduction are different problems to solve. However, experiences from techniques applied for voltage stabilisation may also be applied to reduce voltage fluctuations at a given node, particularly if shunt compensation equipment is used. A brief list of conventional and modern solutions for voltage fluctuation mitigation is given below:

- Stiffening of the supply [24, 25]
- Installation of a higher rated power transformer [24,26]
- Reduction of the rated power of the installation [27-29]
- Installation of series passive devices [28-31]
- Source of disturbance connected to a separate transformer [25]
- Installation of shunt compensators [18,24,32-37]

1.3.3.2 FACTS and Custom Power Controllers as Mitigation Equipment

The availability of improved power electronics controllers, mainly based on voltage-source-converter technology, have brought about better controllability into the electrical systems and thus better mitigation of voltage fluctuations.

A VSC-based FACTS compensator has been applied to compensate an electric arc furnace plant [34,36]. Moreover, STATCOM compensators can also be found in wind farm installations [33,35]. In distribution systems, mitigation equipment is used to ameliorate voltage fluctuations produced by large induction motors [30]. The Adaptive Flicker Controller [18] and the distribution STATCOM [37] are modern power electronic-based equipment used for such a purpose. The D-STATCOMs installed at a timber mill in British Columbia, Canada [38] and at Seattle Iron & Metals Corp., Seattle, USA [39], are representative examples of industrial plants where mitigation equipment finds favour.

The control strategy plays a key role in determining the overall performance of the compensator. The conventional d-q with PI regulation scheme [39,40] and instantaneous reactive power strategy [24,34,36] are the most popular schemes used in electric arc furnace applications. In cases of STATCOM for wind farm applications, the unity power factor [33,35] and the dynamic voltage-control [35] are the control schemes most often reported. In particular, dynamic voltage-control is suitable for controlling voltage rise, islanding phenomena and mitigation of voltage fluctuations.

Nevertheless, mitigation schemes are not perfect, and some voltage fluctuations will remain in the electrical system. These are termed residual voltage fluctuations in this research work, having a residual P_{st}, with the ability to propagate and to add to voltage fluctuations already present in the electrical system from other sources. The overall voltage fluctuation resulting from such a summation can lead to a P_{st} above the limit of irritability, leading to complains from customers. To the best of the Author's knowledge, the mitigation of residual voltage fluctuations propagating in transmission and distribution electrical systems using series-connected FACTS equipment has not yet been addressed in the open literature.

1.4 REAL-TIME SIMULATION AND REAL-TIME HARDWARE-IN-THE-LOOP EXPERIMENTATION

The steady state and transient state of transmission and distribution networks are normally studied using digital simulation tools such as EMTP [41] and PSCAD© [42]. Digital simulators are powerful tools that yield useful information for the better understanding of the electrical system. However, the speed at which they operate is one

of their weak points, since they do not operate on a real-time basis. To put this into perspective, take the case of a transient disturbance lasting only a few milliseconds in the actual network but one which may take second, minutes or even hours to reproduce by non-real time computer simulations [43]. Such a disadvantage renders these simulators unsuitable for hardware-in-the-loop testing.

A real-time digital simulator together with ancillary electronics equipment provides an ideal real-time environment for closed-loop experimentation of FACTS and Custom Power devices and their control strategy. Real-time studies, as conducted in the present work, require that the digital simulation of the modelled system be executed in real-world time. With the ever increasing complexity of modern transmission and distribution systems, the energy markets geared towards deregulation, the incorporation of advanced equipment and controllers, and imminent widespread incorporation of embedded generation units, there is a need to understand better the behaviour and interactions which may arise between the various components in the system. The real-time simulation and testing technology provides a convenient and powerful resource to meet some of these challenges.

1.5 RESEARCH LINES OF THIS WORK

The main research lines in this research project are listed below:

- **Voltage Fluctuation and Light Flicker Phenomena**: a) a critical review of definitions and standards is carried out; b) evaluation of a flicker severity index and measurement equipment; c) study sources of voltage fluctuation and shunt mitigation equipment; d) voltage fluctuation mitigation using a TCSC controller; e) development of a virtual instrument for real-time hardware-in-the-loop experimentation.

- **FACTS and Custom Power Controllers**: a) study of shunt and series controller topologies; b) evaluation of actual applications; c) design, construction, and testing of prototypes; d) investigation of new areas of application of FACTS controllers.

- **Control Systems**: a) study and development of control strategies for TCSC controllers for normal and abnormal operating conditions; b) digital simulation of new control strategies.

- **Real-Time Software and Hardware**: a) development of a real-time hardware-in-the-loop testing environment for laboratory experimentation; b) interactive testing of new control systems and scaled-down prototypes; c) development of instrumentation system for measuring electrical quantities on-line.

1.6 MOTIVATION BEHIND THE RESEARCH PROJECT

In order to determine the effectiveness of applying series FACTS and Custom Power equipment to control, mitigate, and damp abnormal voltage waveform phenomena in transmission and distribution systems, it is necessary to develop new control strategies and voltage fluctuation measurement tools or to use better the existing ones. However, before significant experimental progress can be made, it is envisaged that a real-time hardware-in-the-loop testing facility and reliable three-phase physical models for the electrical system and TCSC controller need to be built in the laboratory.

Over the last decade significant progress has been achieved in several fronts of FACTS technology. At the modelling and simulation levels, the following topics have received attention:

1. Power flows
2. State estimation
3. Transient stability analysis
4. Small-signal stability
5. Harmonic analysis
6. Time domain simulation for electrical networks and power electronic systems
7. Optimal power flows

This research is primarily concerned with the utilisation of modern power electronic-based controller suitable for the dynamic mitigation of voltage fluctuation phenomena in electrical networks. The effectiveness of the proposed scheme is experimentally proven in a real-time hardware-in-the-loop testing environment.

The mitigation of voltage fluctuations has been an area of great research interest for many years, where considerable and significant progress has been made by applying various kinds of equipment, including shunt FACTS and Custom Power controllers. However, very little research work has been reported in the open literature concerning propagation and mitigation of voltage fluctuation in the electrical network using series FACTS and Custom Power controllers as mitigation apparatus. In this research work a new FACTS application is pursued, namely the TCSC is investigated as tool for voltage fluctuation mitigation. It is shown in this investigation that in addition to the established practice of using TCSCs to alleviate abnormal system condition, such as the damping of power oscillations and the mitigation of subsynchronous resonances, the TCSC can also be used to ameliorate voltage fluctuations. This has required the implementation of both conventional and newly developed control schemes, as well as the development of instrumentation aimed at real-time applications.

A physical three-phase scaled-down TCSC prototype was designed and built in order to have access to an actual TCSC controller, operating in a real-time hardware-in-the-loop environment. This is series connected with a representative scaled-down version of a small-size electrical system.

The Kayenta substation and the Slatt substation are two well-known TCSC installations. The real-world operation experiences reported on these projects [44-46] is a highly valuable source of information, applicable to the implementation of realistic controllers.

Useful data is also provided in the few references that report on the construction of analogue-type TCSC prototypes. In one of these references [13], a single-phase TCSC prototype is implemented to carry out a closed-loop interaction with a digital model residing in a PC. Furthermore, the paper also reports on simulations concerning the mitigation of an abnormal operating system condition, this being the case of a subsynchronous resonance.

In spite of the great value that the data has, the information available barely touches on design procedures, characterisation of the prototype, and the ancillary systems that are required to support its operation. Bearing this in mind, this research work reports on the design and construction details of the TCSC prototype, in particular, the large number

of specialised software and hardware system tools that need to be created, verified and implemented in order to make the TCSC operate as a mitigation apparatus, and that enable its evaluation in a real-time, hardware-in-the-loop basis. The research is therefore also directed at developing the following systems:

- A new control strategy suitable for the flexible operation of the TCSC as dynamic voltage fluctuation mitigation equipment encompassing a wide range of varying frequencies and amplitudes. The control strategy adapts its response to follow the fluctuating rms emitted by the many sources of voltage fluctuation in the electrical systems.

- A virtual instrument for the accurate measurement of voltage fluctuation and light flicker severity, incorporating the most recent definitions on the topic, published by international standard-making bodies.

- A testing environment for hardware-in-the loop experimentation and the supporting measurement equipment to monitor the performance of the combined operation of the new control strategy and the TCSC prototype.

Concerning closed-loop hardware-in-the-loop applications, the flexibility of the real-time digital simulator is explored together with the robustness, accuracy and wide operating range of the scaled-down prototype. The expanding computational efficiency of the real-time simulators allows the development of more elaborated test beds.

1.7 OBJECTIVES AND PURPOSES OF THE PRESENT RESEARCH WORK

The main objectives of this research project are as follow:

- To investigate, in depth, the applicability of the TCSC as a mitigation apparatus for voltage fluctuation propagation, assessing the effectiveness of the equipment by carrying out comprehensive experiments over a wide range of voltage fluctuation and light flicker severity levels. The experiments will be based on closed-loop real-time hardware-in-the-loop facilities and the experimental results will be compared against available P_{st} measurements and additional information corresponding to full-scale shunt FACTS and Custom Power controllers.

- To develop a robust and flexible scaled-down, three-phase Thyristor Controlled Series Compensator (TCSC) capable of controlled operation under normal and abnormal conditions, at different power ratings. The prototype should be constructed using a number of interfaces to increase the flexibility of the hardware-in-the-loop experimentation. The monitoring of instantaneous voltage and current for both passive and active devices should be carried out using two purpose-built sensor interface modules and one commercially available power measurement instrument directly connected at the required point of measurement. The design and construction of the electronic systems that support the dynamic operation of the TCSC prototype and surrounding electrical network should be included. Comprehensive open loop testing will be carried out to evaluate the general performance of the equipment.

- To develop a flexible dynamic control strategy suitable for the operation of the TCSC prototype to act as a voltage fluctuation mitigation equipment under real-time hardware-in-the-loop environment. The proposed real-time control strategy, termed Real-Time Dynamic Instantaneous Mitigation Response (RT-DIMR), will be implemented using a commercially available real-time computing platform from ADI corp. This will be achieved by using both a set of FORTRAN programs specifically created for the real time application and the library of functional blocks provided by the EASY5 simulation package.

- To develop a laboratory-level, real-time testing environment to conduct reliable hardware-in-the-loop experimentation with the TCSC prototype, incorporating a scaled-down two-node electrical system with two controlled sources of sinusoidal and non-sinusoidal voltage. The system should contain a multi-variable measurement system for monitoring purposes, and a system protection unit. The TCSC prototype, RT-DIMR control strategy and real-time testing environment should be integrated into a single platform to enable real-time experimentation with ease.

- To investigate the sources of voltage fluctuation, propagation phenomena, measurement techniques and numeric figures used in the evaluation of the severity voltage fluctuation and light flicker phenomena affecting residential, commercial and industrial consumers.

1.8 CONTRIBUTIONS

- The capability of the TCSC as a voltage fluctuation mitigation apparatus has been experimentally demonstrated. This has been achieved by measuring the P_{st} and IFS in pre-mitigation and post-mitigation operating scenarios, made possible by the combined use of the RT-DIMR and the prototype working under real-time hardware-in-the-loop conditions. The results and measurements obtained demonstrate the applicability of the TCSC to control undesirable electrical phenomena other than the well-known power oscillations and subsynchronous resonances. In order to support the correct operation of the TCSC, a number of electronic systems were created and extensively tested.

- After an in-depth study of the TCSC resonances, which have been termed resonance modes, a non-explicit resonance at α=90° has been found and termed intrinsic resonance mode. For a well-designed TCSC only the fundamental and the intrinsic resonance modes should be active.

- A scaled-down, three-phase TCSC prototype rated at 3.3 KVA has been designed and built in the laboratory. The flexibility and characteristics of the prototype have been experimentally demonstrated. The new tools and methods developed as part of this research are documented in the thesis. A number of dynamic, transient and non-characteristic current and voltage waveforms resulting from the experimental processes have been presented. As additional contribution, a TCSC design procedure, based in the synchronisation of the resonance modes, has been identified. In this context, a couple of easy-to-use curves are provided in order to facilitate the calculation of the TCSC LC circuit.

- It has been established that mitigation schemes are not perfect and some voltage fluctuations will remain in the electrical system. These are termed residual voltage fluctuations, having a residual P_{st}, with the ability to propagate and to add to voltage fluctuations already present from other sources. An electrical system with multiple voltage fluctuation sources, and residual voltage fluctuations, is a very realistic situation. In addition, it has been perceived the TCSC capability to mitigate voltage fluctuations emitted by multiple sources. This would suggest that under certain circumstances various shunt-connected mitigating equipments could be substituted

with a single TCSC. Such scheme could be named wide area voltage fluctuations mitigation.

- A control strategy, termed RT-DIMR, for real-time hardware-in-the-loop application is developed to provide a flexible control tool suitable for time-varying three-phase voltage fluctuation mitigation applications. The algorithms are able to instantaneously track each single-phase rms fluctuation separately in a range of frequencies from 0.1 to 25 Hz. The capability of the RT-DIMR control strategy has been extensively tested using real-time experimentation.

- The concepts of P_{st} sensitive node, P_{st} sensitive load and flicker sensitive customer have been introduced and defined, which aim at facilitating the understanding of a voltage fluctuation phenomenon. In addition, a guideline is introduced in order to locate loads and customers adversely affected by voltage fluctuations and to place voltage fluctuation mitigation equipment.

- A real-time virtual flickermeter with the capability to measure instantaneous flicker sensation (IFL), short-term severity index (P_{st}), and long-term severity index (P_{lt}) has been developed and fully tested. The virtual instrument has been used to evaluate P_{st} while running the real-time hardware-in-the-loop experiment to determine the mitigation capacity of the TCSC. The design of the virtual flickermeter is based on the analogue flickermeter described in the IEC-61000-4-15 standard. A computer program has been written in Fortran to perform the quantification of P_{st} and P_{lt} on a real-time basis. This yields most valuable information since the method is not clearly described in the standard.

- Following successful P_{st} improvements, the application of the series mitigation equipment in distribution busbar feeders is proposed. This opens a new application area for TCSC equipment in distribution systems, which may be termed distribution TCSC or custom TCSC. Series-connected mitigation equipments using a variety of control schemes, different from RT-DIMR, are also suggested for application in distribution systems.

1.9 OUTLINE OF THE THESIS

The thesis is organised into eight chapters and three appendices, with seven of the chapters described in the following paragraphs:

Chapter 2 addresses the issue of voltage fluctuation phenomenon and related topics. The various definitions concerning voltage fluctuation and flicker are amply discussed and comparisons are drawn between them. Sources of voltage fluctuation such as electric arc furnaces, wind farms, welding machinery and large induction motors are analysed with the purpose of obtaining the most common range of fluctuation frequencies for every source. The chapter also presents the improved flickermeter described in the international standard IEC-61000-4-15, including the terms known as instantaneous flicker sensation (IFL), short-term severity index (P_{st}) and long-term severity index (P_{lt}). These figures find increased use in the evaluation of voltage fluctuation at key nodes of electrical networks. This chapter also reviews the main mitigation equipments and strategies currently available.

Chapter 3 gives a detailed description of the TCSC structure, operating regions and fundamental frequency impedance. In order to facilitate the TCSC design, terms such as resonance mode and intrinsic resonance mode are defined based on the characteristics of the TCSC steady-state impedance and its poles at fundamental frequency. The definition of the TCSC resonance modes; TCSC fundamental resonance mode; and active resonance mode, together with the finding of the intrinsic resonance mode, are among the major contributions presented in this chapter. The chapter also lists the main FACTS and Custom power controllers, giving a brief description of the controllers and applications.

Chapter 4 deals with the design of an advanced scaled-down TCSC prototype. The characteristics of the equipment are carefully selected for suitable operation in a laboratory-testing environment and, at the same time, ensuring a correspondence with real-word installations. For the appropriate and realistic functioning of the TCSC, great care was placed in avoiding more than one active resonance mode at the steady-state fundamental impedance of the controller. The chapter details the construction of the TCSC prototype and its operative support system (OSS). Digital simulations using

PSCAD™ were performed to verify the matching between the designed and actual characteristics, and also to observe the TCSC capacity to rapidly modulate the line current. These simulations are presented in Appendix A.

Chapter 5 introduces a real-time control strategy termed Real-Time Dynamic Instantaneous Mitigation Response (RT-DIRM). The real-time computing platform, the simulation software and the hardware tools used to develop the various systems employed in this research project are described. Moreover, various control schemes for SSR, power oscillation and steady-state power flow regulation are reviewed. The chapter describes the design and implementation of the RT-DIMR used to govern the TCSC prototype mitigation behaviour. The chapter includes a comprehensive number of simulations of the RT-DIMR control, which have been carried out using EASY5 ™.

Chapter 6 presents the different procedures and experiments carried out to characterise the flexibility of the scaled-down TCSC prototype and supporting electronic systems. The open loop experiments are centred on the operation of the controller at different triggering angles α; the dynamic response of the prototype to step and sinusoidal modulation; and the behaviour of the equipment close to the resonance point. For the running of the experiments, the prototype is inserted into a testing environment for three-phase operation. A selected number of voltage and current waveforms resulting from the experimental processes were recorded and are included in this chapter. This chapter also includes a description of the elements associated with real-time, hardware-in-the-loop testing environment.

Chapter 7 deals mainly with real-time, hardware-in-the-loop experiments. The key factors behind the selection of the TCSC to serve as a mitigation apparatus are put forward, as well as the need for series connected equipment to mitigate the residual voltage fluctuation propagating in the electrical system.

The RT-DIMR shows its capability during the real-time, hardware-in-the-loop testing, enabling flexible and effective control of the scaled-down TCSC prototype. In order to evaluate the severity of the voltage fluctuation, as well as the effectiveness of the TCSC as a mitigation apparatus, a real-time virtual flickermeter version of the analogue flickermeter described in the IEC-61000-4-15 standard, is implemented for the measurement of P_{st}, P_{lt} and IFL.

The experimental results confirm the prowess of the TCSC for the mitigation of voltage fluctuation, after effectively reducing the P_{st} level for a wide range of fluctuating frequencies. The results are compared against those available in references where the P_{st} figure was used for the evaluation of the mitigation of voltage fluctuation in full-scale electrical systems. Towards the end of the chapter, a number of ideas are advanced for further applications of the equipment, new series connected mitigation equipment and control techniques. The FORTRAN routines developed for the control strategy and the flickermeter are included in an Appendix B and C, respectively.

This chapter also introduces and defines the concepts of P_{st} sensitive node, P_{st} sensitive load and flicker sensitive customer, which aim at facilitating the understanding of voltage fluctuation phenomenon and at locating the nodes, load and customers adversely affected by such a problem.

Chapter 8 gives the overall conclusions for the research work and further investigation and research projects are discussed.

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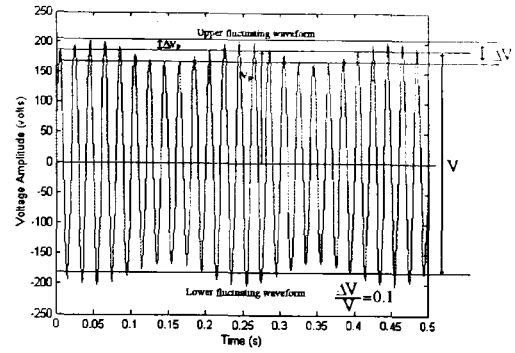
CHAPTER

2



VOLTAGE FLUCTUATIONS IN ELECTRICAL NETWORKS: SOURCES, MEASUREMENT, AND MITIGATION

2.1 INTRODUCTION

Voltage fluctuations are defined in this research work as repetitive voltage deviations varying at some particular frequency and amplitude. Owing to the complexity and size of the electrical system, the number of possible voltage fluctuations sources is quite large.

The relative voltage amplitude variation may be expressed as the ratio $\Delta V/V$, where ΔV is associated with the voltage deviation amplitude and can be identified as a signal modulating the line voltage. The ratio can be depicted in terms of instantaneous or rms values. If the rms value is used, V is the mean value of the fluctuating rms line voltage and ΔV represents the peak deviation of the fluctuating rms value. If the instantaneous value is used instead, V and ΔV represent the peak-peak value of the non-modulated signal amplitude of line voltage and the peak-peak value of the modulating signal, respectively. Considering $\Delta V(t)$ as a single sinusoidal waveform at frequency ω_f and V as the peak amplitude of the line voltage at the nominal frequency ω_o, with no harmonics and no modulation, the resulting voltage fluctuation $V_f(t)$ is expressed as:

$$V_f(t) = (1 + \Delta V_1)(V_p \sin(\omega_o t)) \tag{2.1}$$

$$\Delta V(t) = \Delta V_p \sin(\omega_f t) \tag{2.2}$$

$$\Delta V_p = \Delta V_1 V_p \tag{2.3}$$

where ΔV_p is the peak of the signal modulating the line voltage, $V=2V_p$ is the peak-peak value of the non-modulated line voltage, and $0 \leq \Delta V_1 \leq 0.5$. For this case $\Delta V/V$ is

$$\frac{\text{Modululating signal peak-peak value } (\Delta V)}{\text{non-modulated line voltage peak-peak value}(V)} = \frac{2\Delta V_p}{V} = \frac{\Delta V_p}{V_p} = \frac{2\Delta V_1 V_p}{2V_p} = \Delta V_1 \tag{2.4}$$

The voltage fluctuation, as rms value, can be expressed as:

$$V(t)_{rms} = V(1 + \Delta V(t)); \qquad V = V_p/\sqrt{2} \tag{2.5}$$

$$\Delta V(t) = \Delta V_r \sin(\omega_f t); \qquad \Delta V_r = \Delta V_1 V \tag{2.6}$$

$$\frac{\text{Peak deviation of the fluctuating rms } (\Delta V)}{\text{mean rms of line voltage } (V)} = \frac{\Delta V_r}{V} = \frac{\Delta V_1 V}{V} = \Delta V_1 \tag{2.7}$$

ΔV_1 in equations 2.3 to 2.7 has the same value. By way of example, Figure 2.1 illustrates voltage fluctuations calculated with MATLAB© at two different fluctuating frequencies, namely 5Hz and 25 Hz, and the corresponding ΔV and V levels.

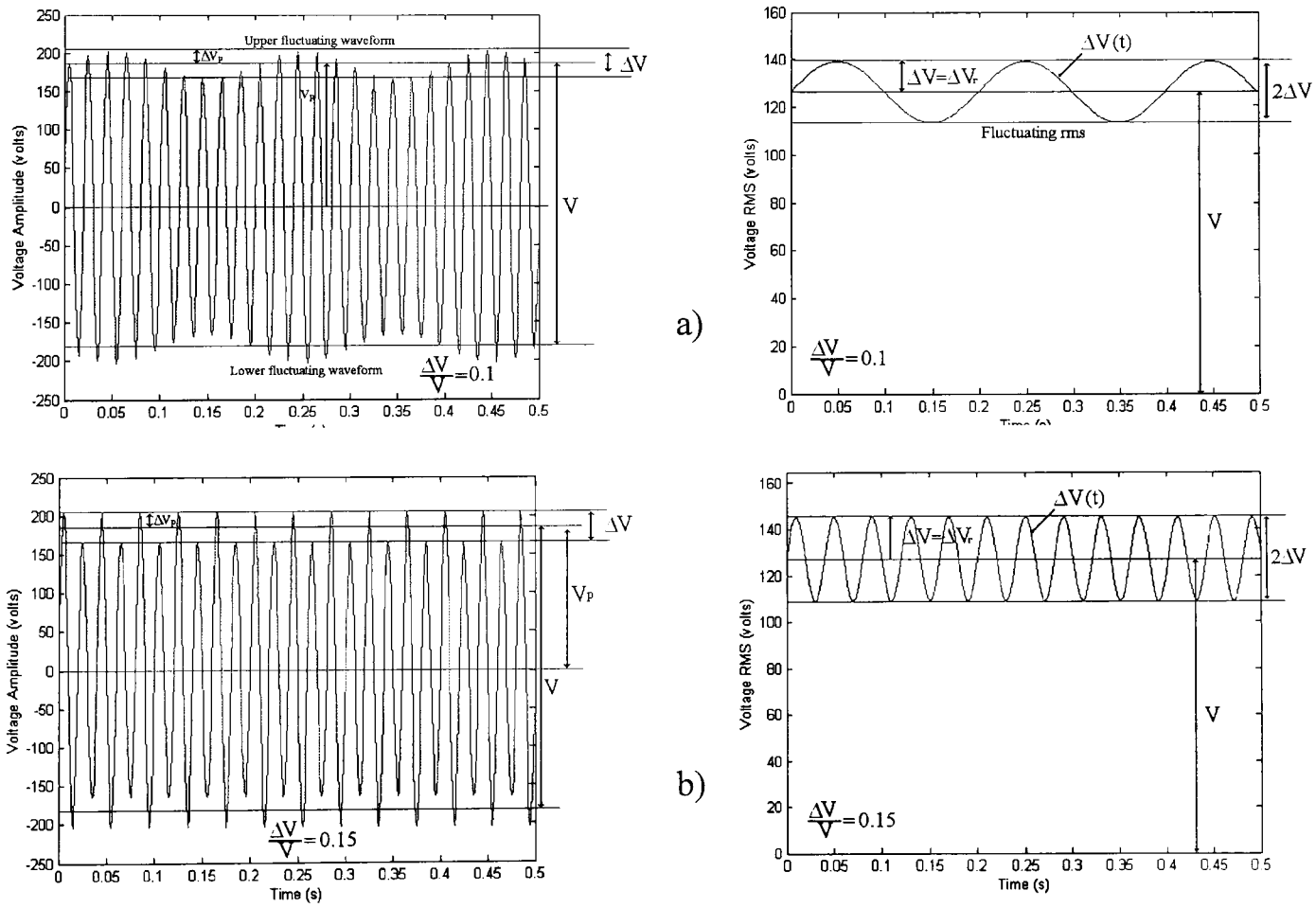


Figure 2.1. Voltage fluctuation and corresponding fluctuating rms: a) 5Hz modulation; b) 25Hz modulation. V_p=180 for both cases.

The sinusoidal waveform fluctuation at a single frequency and amplitude is not the general case by any means, the fluctuation can, for instance, be rectangular or a complex multi-frequency waveform with time-varying amplitude resulting from various sources. Figure 2.2 shows examples of a voltage signal with non-sinusoidal fluctuations.

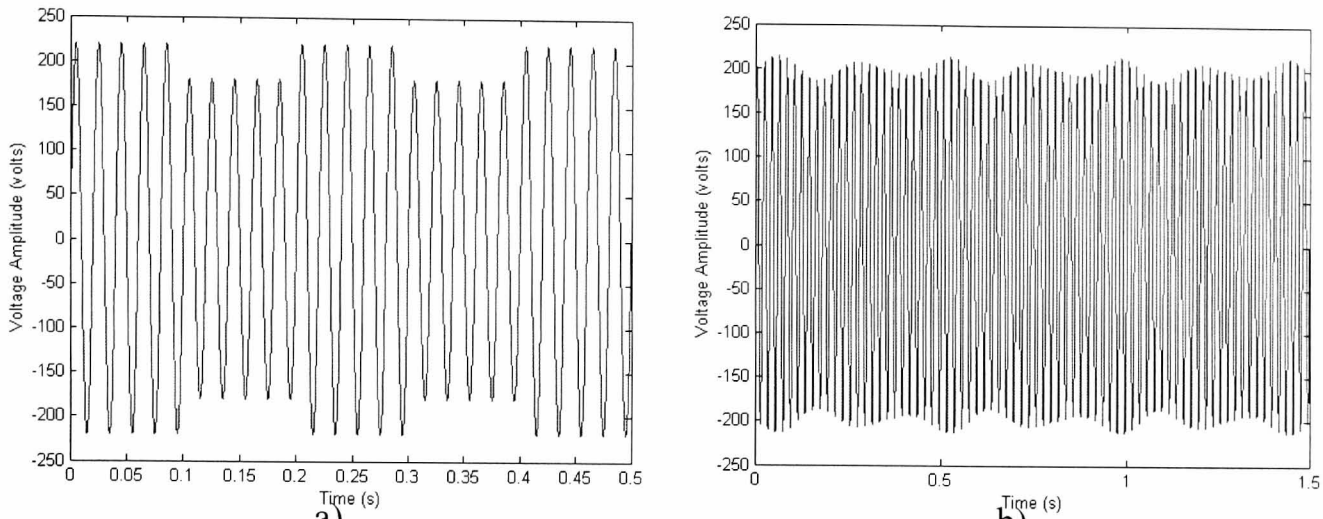


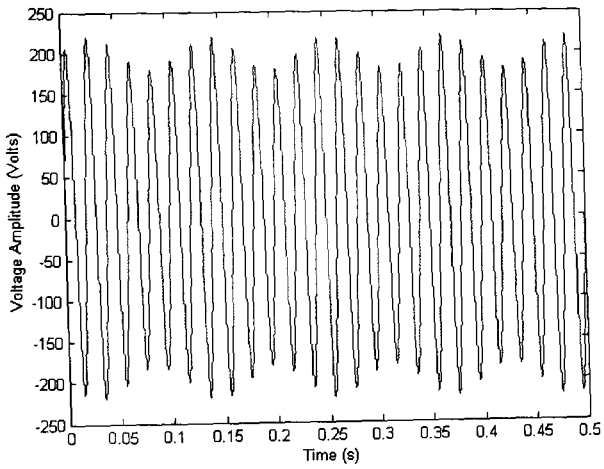
Figure 2.2. Non-sinusoidal voltage fluctuation. a) Rectangular-shaped modulation. b) Multi-frequency- shaped modulation.

Line voltage modulations at frequencies higher than $\omega_o/2$ produce voltage fluctuations at frequencies lower than $\omega_o/2$. For instance, modulations at 30Hz, 55Hz and 90 Hz produce voltage fluctuations at 20Hz, 5Hz, and 10Hz, respectively. In general, voltage fluctuations in the region $0> \omega_f \geq \omega_o/2$ will result from line voltage modulations at interharmonics and subharmonics of the nominal frequency ω_o. Figure 2.3 shows cases where the fluctuation is centred at 8.8 Hz. The calculations have been carried out using MATLAB© and different modulation frequencies. It should be pointed out that the frequency of the resulting fluctuations is always a subharmonic of ω_o.

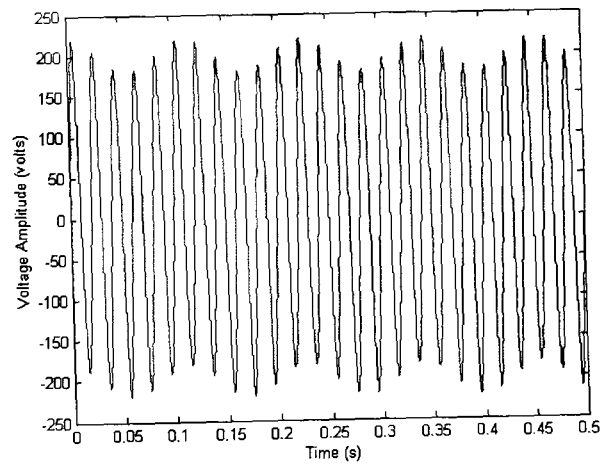
The upper and the lower waveform fluctuation profiles are out of phase for some cases, as is shown in Figures 2.3b, 2.3d, 2.3f and 2.3i. If ω_f is the modulating frequency and $0> \omega_f \geq \omega_o/2$ is defined as the base frequency region where the fluctuations occur, then the upper and lower fluctuations resulting from modulations above the base frequency region are described in Table 2.1.

Table 2.1. Relationship between upper and lower waveform fluctuation

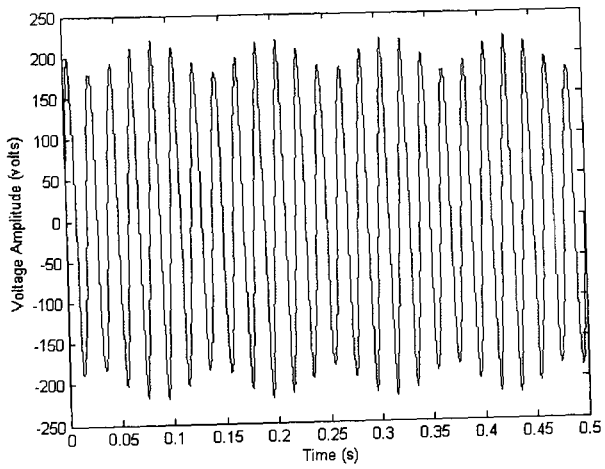
Modulating Frequency	Characteristic
$2n\omega_o \pm \omega_f \quad n = 1,2,3,4..$	Upper and lower fluctuations are in phase
$(2n-1)\omega_o \pm \omega_f \quad n = 1,2,3,4..$	Upper and lower fluctuations in phase opposition



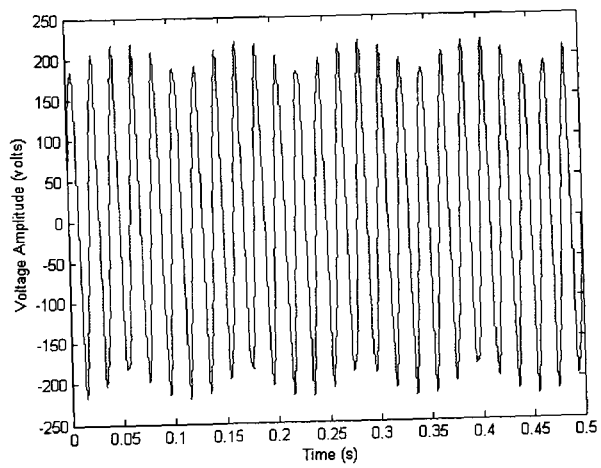
a) 8.8 Hz



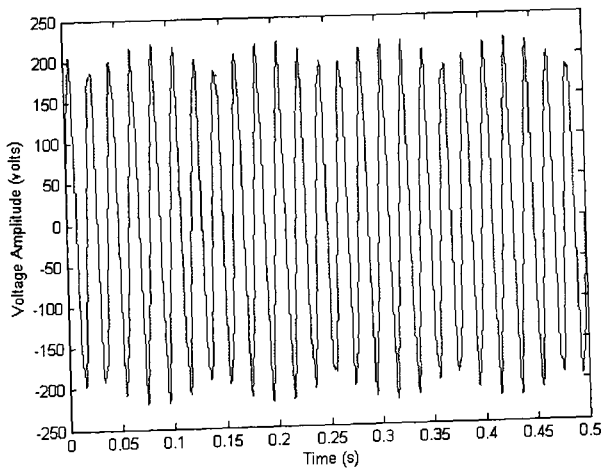
b) 41.2 Hz



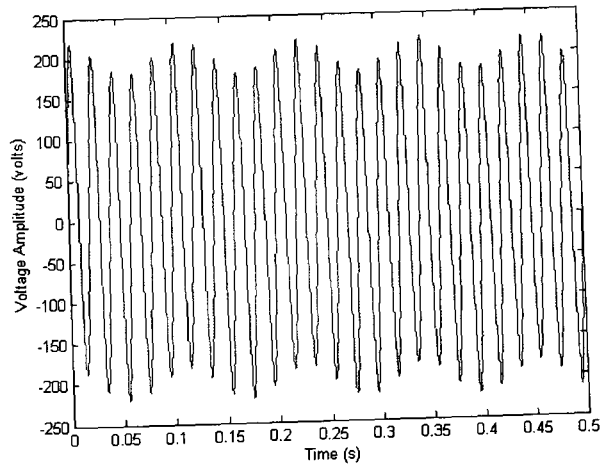
c) 108.8 Hz



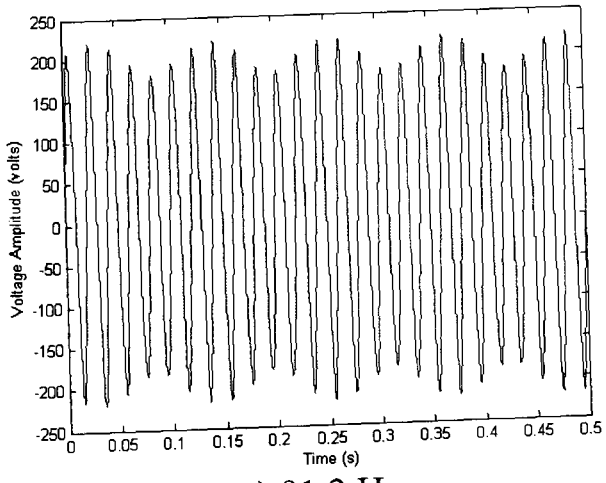
d) 141.2 Hz



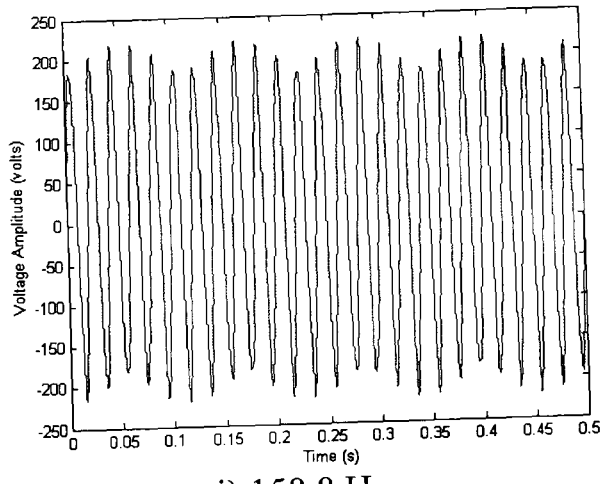
e) 191.2 Hz



f) 58.8 Hz



g) 91.2 Hz



i) 158.8 Hz

Figure 2.3. 8.8Hz Voltage fluctuation resulting from different modulating frequencies

One consequence on lighting circuits, particularly incandescent and fluorescent lamps being subjected to voltage fluctuations, is that the light intensity will fluctuate following the frequency of the repetitive rms deviations. The visual effect caused by this condition, perceived by individuals, is named light flicker or flicker [1-4].

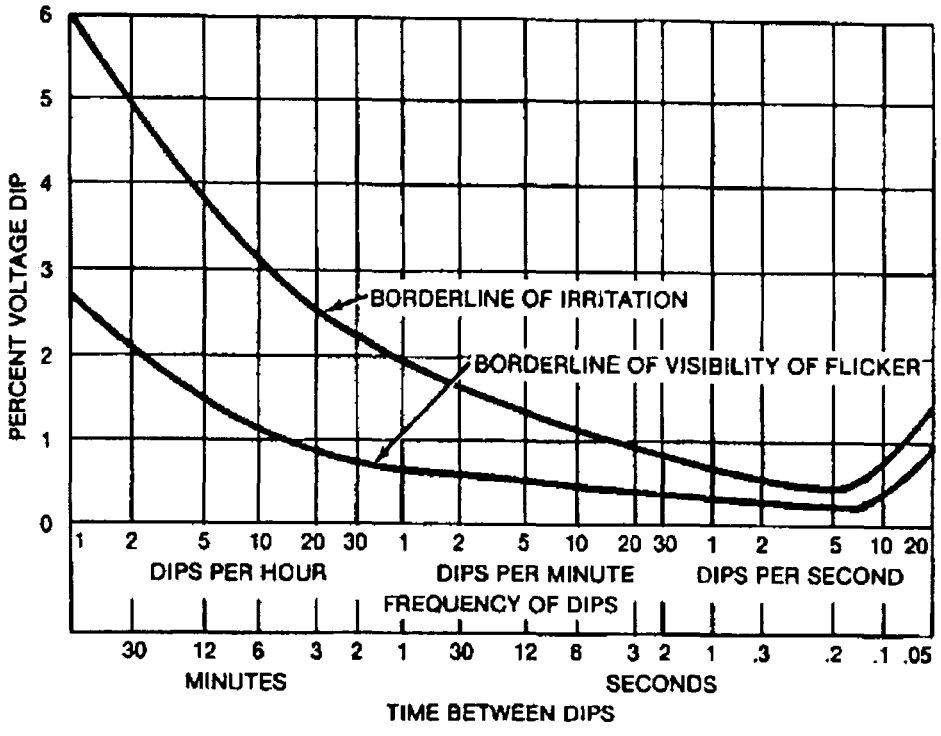
The voltage fluctuation and flicker terminology is not unanimous by any means. In the open literature, the terms voltage flicker or flicker have long been used to refer to voltage fluctuation. The former can be understood as a shortening for voltage fluctuation leading to light flicker [5], or as the term used to embrace all adverse effects of fast voltage fluctuations [6]. The latter leads itself to confusion between a visual and an electrical phenomenon. In this research project, the flicker and voltage flicker terms are not used. Instead, voltage fluctuation is the term used. It is worth pointing out that a widely-accepted terminology and standards are still lacking in this area. In this research work, voltage fluctuation and flicker are used in connection with electrical and visual phenomena, respectively.

When an individual, or a group of individuals, are subjected to flicker, they experience a low, mild or extremely irritating sensation depending on the fluctuation frequency and amplitude, and the eye sensitivity of those experiencing the phenomenon. The flicker which is perceptible and irritating to humans occurs at voltage fluctuations in the 0.5 - 25 Hz range in 50 Hz systems, and 0.5 – 30 Hz range in 60 Hz systems, with maximum sensitivity taking place between 5 and 15 Hz, and peaking in the vicinity of 8.8 Hz. At this point the flicker is extremely annoying even at a $\Delta V/V$ ratio as low as 0.5% [7].

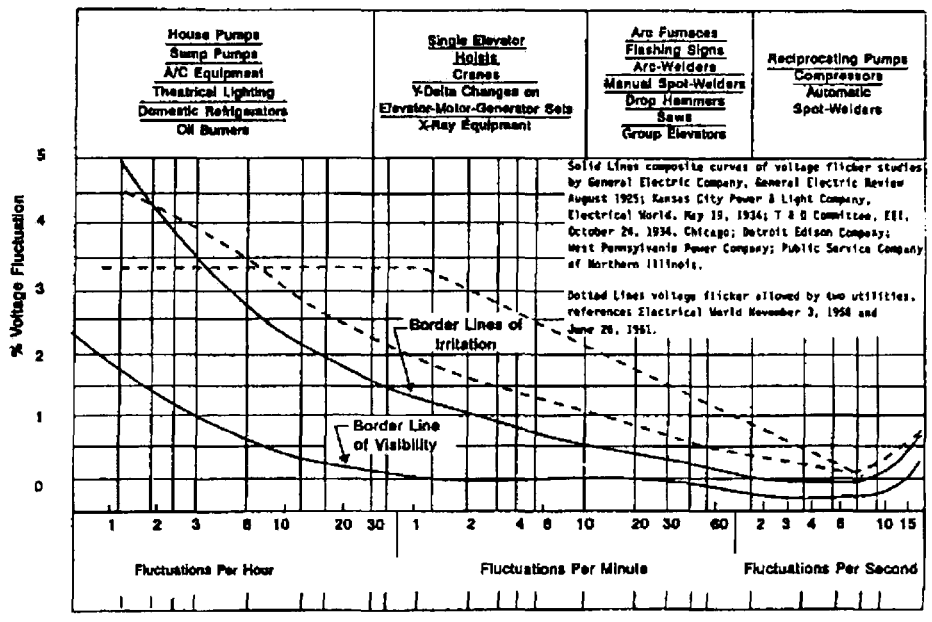
The human response to light intensity at different $\Delta V/V$ fluctuations and flicker measurements have been a topic of research, discussion and publication for more than 70 years. The contributing efforts are summarised in a number of standards and recommendations including curves relating the $\Delta V/V$ ratio to the frequency. The flicker curves, as they are usually called, are derived from controlled experiments with people subjected to different flicker dosages, using incandescent lamps, and recording the particular response. The flicker curves have borderlines separating tolerable from uncomfortable flicker sensations.

The $\Delta V/V$ ratio and flicker curves have been in use in industry for many years and have been enacted by standards making bodies such as IEEE and IEC. However, there is no word-wide agreement yet on the interpretation of the $\Delta V/V$ ratio, since the light flicker

dosage quantification using flicker curves depend very much on individual interpretations of those who are performing the voltage fluctuations evaluation. The IEEE has two recommendations including flicker curves, IEEE-141-1993 [1] and IEEE-519-1992 [2]. These flicker curves, named borderline of visibility and borderline of irritation, are shown in Figure 2.4.



a)



b)

Figure 2.4. IEEE Flicker curves: a) IEEE-141-1993; b) IEEE-519-1992.

When flicker is measured just below the borderline of visibility, some people may notice that the light is actually fluctuating. If the measurement is between borderlines, most the people will agree that the light is actually fluctuating and, probably, mildly

irritating for very sensitive persons. Above the borderline of irritation a good number of people will feel uncomfortable and irritated, at different grades, and complaints will start to be lodged at the local electricity company. These will increase for higher emissions of flicker, particularly in the range of 5 to 15 Hz. The similarity between the borderline of visibility and irritation, in Figure 2.4a and Figure 2.4b, is evident existing only slight differences in the weighting factor at the low range of fluctuation, particularly between one fluctuation per minute and one fluctuation per second.

A closer inspection of the flicker curve reveals a number of disadvantages when these are used as voltage fluctuation and flicker evaluation method. A summary of the most relevant shortcomings are listed below:

- These curves lead to open subjective interpretations, particularly when dealing with the amplitude of the fluctuation. Such ambiguous interpretations are reflected in the variety of equipment used in the measurement of flicker (flickermeter).

- Measurements of instantaneous flicker are the only form of measurement that can be carried out. In a normal flicker measurement procedure, a waveform is recorded and then the frequency and magnitude of the fluctuations are extracted. The flicker severity is then obtained using the flicker curve. It may be argued that such a procedure is not adequate for the evaluation of the total flicker sensation resulting from varying voltage fluctuations, over a given period of time.

- Evaluation of flicker produced by multi-frequency, periodic or non-periodic, time-varying voltage fluctuating waveforms cannot be carried out. This disadvantage implies that flicker resulting from a combination of multiple individual sources can not be evaluated using the flicker curve.

Despite its very severe shortcomings the flicker curve method is still widely used for the evaluation of flicker, primarily in the United States [8].

The International Electrotechnical Commission (IEC) is an international body engaged in the preparation of standards in all aspects of electrical, electronic and related technologies. These standards are the work of 179 technical committees and subcommittees. The IEC standards for flicker have been prepared by technical committee 77 and are broadly divided into three main categories:

- Limits on voltage fluctuations and flicker for equipment operating in low-voltage networks at different voltage and current ratings, which include the following standards IEC-61000-3-3 [9], IEC-61000-3-5 [10], and IEC-61000-3-11 [11].
- Assessment of emission limits for large fluctuating loads connected to electrical networks at different voltage levels, detailed in standard IEC-61000-3-7 [12].
- Specifications for flicker measuring apparatus and evaluation of flicker severity, detailed in standard IEC-61000-4-15 [7].

In the open literature, the acceptance of standard IEC-61000-4-15 is growing fast, particularly in Europe. The standard introduces the flicker perception measurement, named instantaneous flicker sensation (IFS), and includes the important concept of short, P_{st}, and long, P_{lt}, flicker severity indices as an effective form of statistical evaluation of flicker over a period of time. Two tables included in the standard relate $\Delta V/V$ to one unit of instantaneous flicker sensation for both sinusoidal and rectangular modulated voltage fluctuation. The indices P_{st} and P_{lt} are obtained by statistically processing the instantaneous flicker sensation and evaluating the data over a short period of time, normally 10 minutes, but can also be selected for 1, 5 and 15 minutes. The index P_{lt} is derived from P_{st} values over periods of time ranging from a few hours up to seven days. The conventional borderlines limits of flicker irritability are P_{st}=1 and P_{lt} = 0.65. Figure 2.5 shows the borderline of perception and Figure 2.6 shows the curve for P_{st}=1.

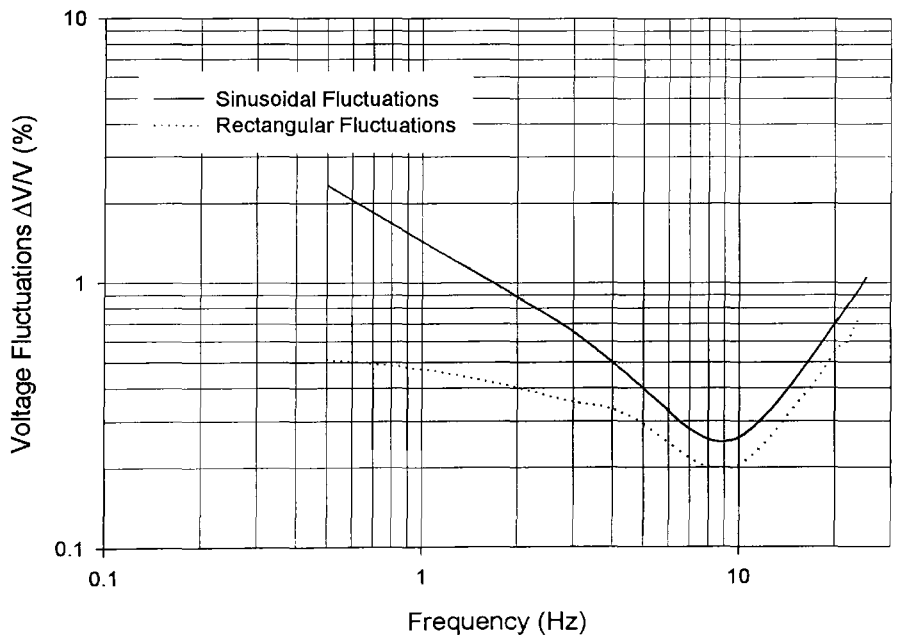


Figure 2.5. Borderline of perception, Std. IEC-61000-4-15

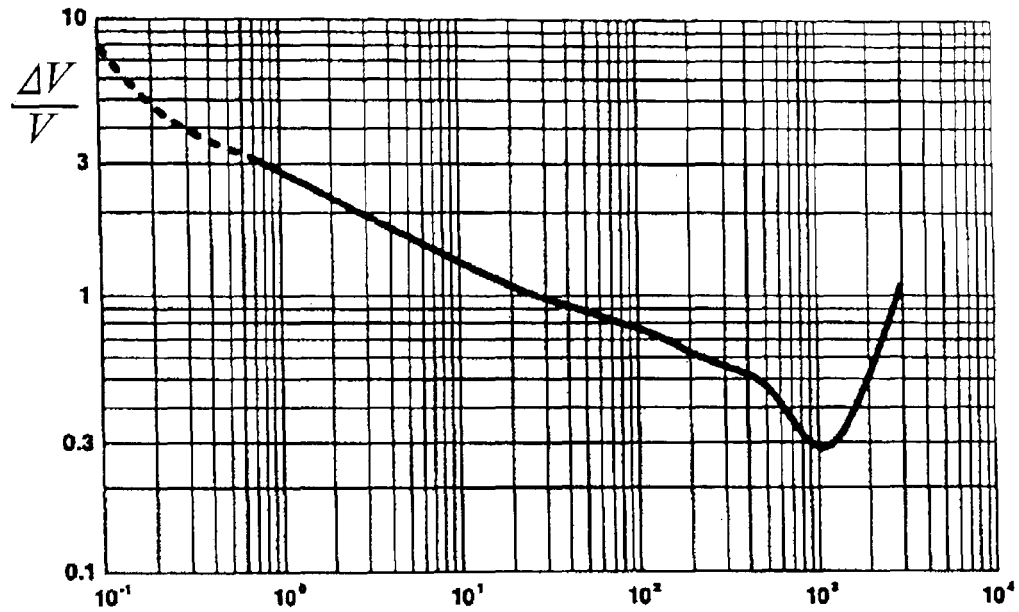


Figure 2.6. Flicker severity. Curve for P_{st}=1

Among the many advantages that the IEC-61000-4-15 standard offers, the following are the most obvious ones:

- Direct reading of a flicker curve is not required, avoiding the caveat of personal interpretation.
- It provides a continuous-time flicker perception measurement by means of a special output named IFS, which is obtained after continuously processing the instantaneous voltage fluctuations using blocks of weighting filters. The characteristic of the filters are such that they follow the lamp-eye-brain model of a representative human being.
- It includes design and construction guidelines for flickermeters. The instrument indicates the flicker perception level for all practical voltage fluctuation waveforms.
- It incorporates the P_{st} and P_{lt} figures indicating the severity of flicker for the short and long term, respectively.
- Capability to measure the total flicker contributed by the voltage fluctuation contributed to by many sources.

The flickermeter addressed in the standard is for an analogue device. The IEC-61000-4-15 document is not straightforward to read and the implementation of the P_{st} concept is difficult to achieve, as the statistical method is only partially detailed. An in-depth

comparative evaluation between the IEEE flicker curve method and the IEC-61000-4-15 standard is not needed, since in february 1998 the IEEE Task Force for Voltage Flicker voted unanimously to embrace and enhance the IEC Flickermeter measurement protocol (IEC 77A/341/CDV) which became the IEEE Recommended Practice [13]. The amendment 1 to IEC-61000-4-15 for 120 V and 60 Hz was published in february 2003 by IEC [14]. In this research project the standard IEC-61000-4-15 is used. It should be pointed out that the "% voltage fluctuation" in figure 2.4 might not have the exactly same interpretation that $\Delta V/V$ in figures 2.5 and 2.6. However, the definition given for the $\Delta V/V$ ratio fully agrees with $\Delta V/V$ stated in the standard IEC-61000-4-15 and figures 2.5 and 2.6.

2.2 SOURCES OF VOLTAGE FLUCTUATIONS

Voltage deviations from the nominal steady-state value are not confined to a specific voltage level. The source, or group of sources, causing the phenomenon is diverse in nature and vast in quantity.

A common scenario is where the vast majority of sources producing voltage fluctuation are fluctuating loads. In this case, the current demanded by the load and the short-circuit level of the network at the point where the load is tapped-off play a key role in determining the voltage deviation from its nominal value. A residential circuit connected in the neighbourhood of a load experiencing high voltage fluctuations and flicker is vulnerable if the feeder is weak [15].

The archetype source of voltage fluctuations in power and distribution systems is the electric arc furnace (EAF), which together with DC electric arc furnaces and some forms of embedded generation [16], especially wind generation, are major contributors of voltage fluctuations. Embedded generation, known also as dispersed generation, has increased its participation in the production of voltage deviation and, particularly, voltage fluctuations. It has been reported that the connection and disconnection of induction generators connected to distribution grids and the operation of photovoltaic generators are potential source of voltage deviations [4,16,38]. However, such claims require further evaluation.

Other sources of voltage fluctuation are also present in the distribution system. Some of them are listed below:

- Industrial wood chipping mill [15,17]
- Lumber mills [15]
- Welder machines [8,18-20]
- Plasma torches [19]
- Heat pumps [18,21]
- Rock crushing machinery [16]
- Intermittent motor starting [12]
- Manual and automatic welder [2]
- Mine hoists [6]

2.2.1 Electric Arc Furnace (EAF)

Gaining an understanding of the electrical behaviour of EAFs has required a great deal of research for quite a long time. The EAF has been catalogued as a bulky non-linear, time varying and unbalanced load [22,23]. The large current demanded by the EAF's operation is highly distorted and fluctuating, showing a complex non-periodic behaviour, which verges on the chaotic [1,6,22,24,25]. A one-line diagram of the EAF installation is shown in Figure 2.7 [6].

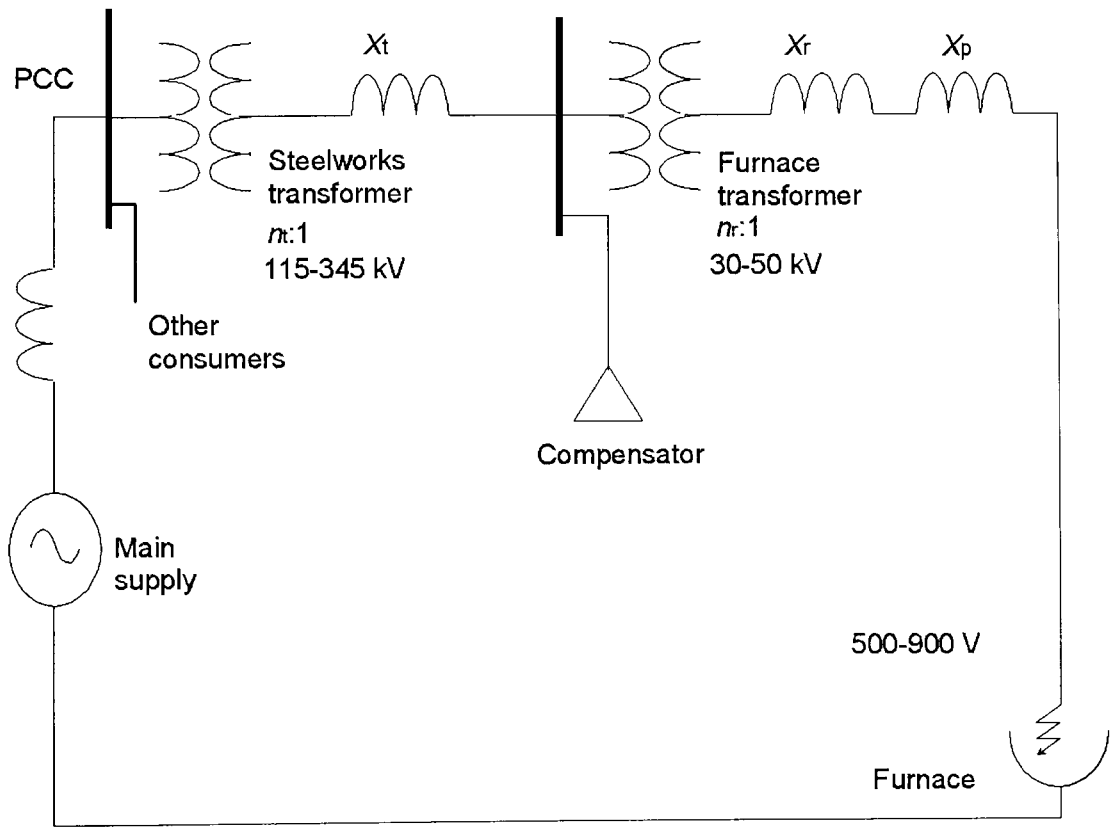


Figure 2.7. An electric arc furnace one-line diagram

The current changes at all the stages of EAF's operation, from the point when the scrap steel is put into the furnace vessel (bore down stage) until the steel is uniformly melted (refining stage). In the bore-down and melting stages the power factor ranges from 0.71 to 0.78, and in the refining stage it is close to 0.83 [6,26].

The spectral analysis of furnace currents reveals a continuous harmonic and inter-harmonic spectrum [1,27]. In Table 2.2, typical furnace harmonic currents values are presented [1]. On-site measurements have been reported indicating harmonics frequencies beyond 400 Hz [27,28].

Table 2.2. Harmonic content of EAF current during two stages

Furnace operation	Harmonic order (% of Fundamental) 2	3	4	5	7
Initial Melting (Active arc)	7.7	5.8	2.5	4.2	3.1
Refining (Stable arc)	2			2.1	

The frequency bands of voltage fluctuations provoked by EAFs ranges from 0.5 to 25 Hz [25] and 0.5 to 30 Hz [29], depending on whether the nominal frequency is 50Hz or 60Hz. It should be noted that the band upper limit in each case corresponds to half their nominal frequency, which agrees with the frequency limits of the voltage fluctuations given in Table 2.1. The compensation methods and apparatus for mitigating voltage fluctuation emitted by EAF are presented in Section 2.6.

2.2.2 DC Electric Arc Furnace (DC-EAF)

The DC arc furnace is an alternative to the EAF for steel production, with single units rated up to 140 MVA and 200 MVA. These plants employ large rectifiers and inductors to supply furnace electrodes. Figure 2.8 illustrates a generic one-line diagram of the DC-EAF.

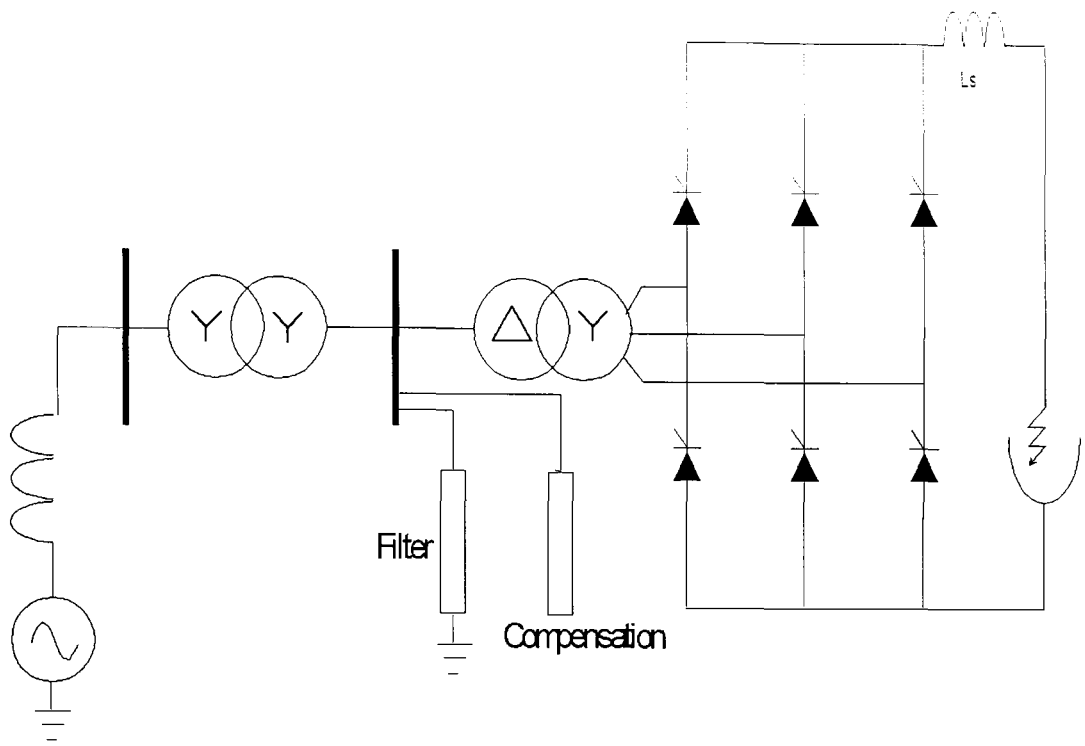


Figure 2.8. DC-EAF one-line diagram

The rectifier structure is based on six or twelve pulse thyristor bridges topologies, which are well suited to low voltage and high current applications, a requirement in the steel-making industry [30]. The EAF's advantages over DC-EAF are mainly in two areas: design simplicity and lower cost equipment and installation. Despite this, the popularity of DC-EAF is growing because of its improved performance. Some DC-EAF advantages are the following

- Significant reduction in voltage fluctuations [31]
- Improved furnace current control by controlling the electrodes current only [31]
- Enhanced efficiency by better control of active and reactive power [22]
- Less consumption of carbon electrodes [32]
- The filtering of harmonics is more effective because the harmonic spectrum is localised at frequencies $(6n+1)\ \omega_0$, $n = 0,1,2,3\ldots$[22]

The furnace current and reactive power vary quite rapidly resulting in voltage fluctuation, current and voltage harmonics and inter-harmonics emitted to the network. Higher inter-harmonics are typically located above 125 Hz [28,33]. Filtering banks and compensation equipment, typically in the form of SVCs, have been normally used to improve the power quality.

2.2.3 Wind Generation

Renewable energy sources (RES) such as biomass, solar, wind, and microhydro are beginning to play an important role in the generation of electrical power in modern system. The Kyoto protocol on climate change; the policies for the reduction of fume emission proposed by companies and governments and the encouraging measures implemented in different countries for the increase of the installed generation capacity based on RES, present a common front aimed at achieving a better environmental future.

From the many possible forms of RES, wind energy is one of the most promising. The wind power technology is mature and well able to compete with traditional power sources in both, technical and economical grounds [34].

The wind energy conversion technology is well developed. State-of–the–art wind turbines are very efficient and powerful. Turbine sizes range from a few kW to over 3.5 MW, with the largest turbine exceeding the 100m height. There are a number of issues still dominating the design and operation of wind turbines among manufacturer and researchers, including types of generators based on their operation, fixed-speed or variable-speed, and regulation types, which can be pitch or stall. Nowadays with the ample availability of power ratings, wind farms installations are as large as several hundred MW and as small as an individual turbine. Figure 2.9 shows the one-line diagram of a wind farm [35].

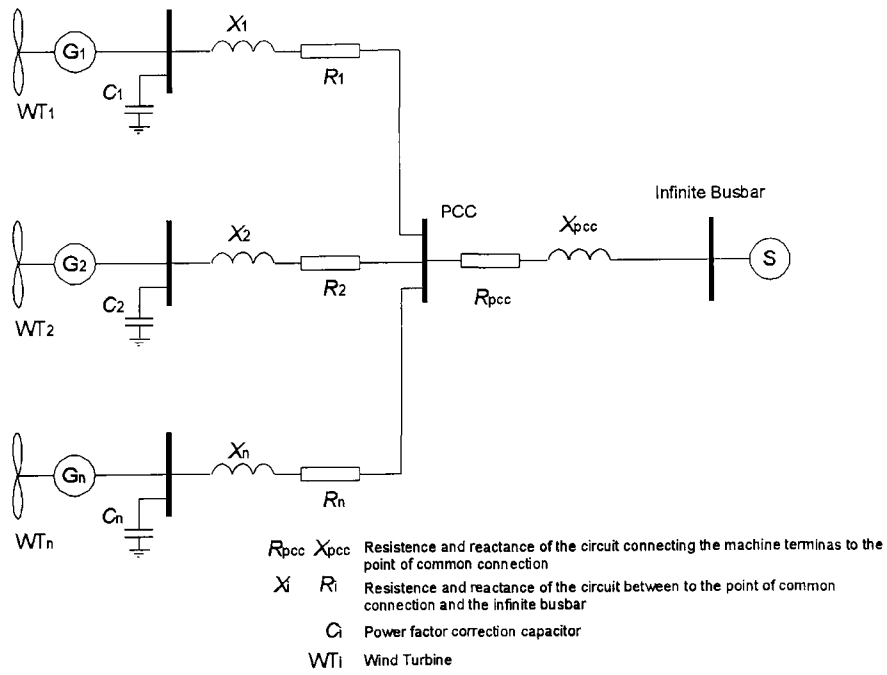


Figure 2.9. Wind farm. Basic one-line diagram

Wind farms are installed in locations where the available wind resources are high, using both in-shore and off-shore locations, and normally far away from the main distribution feeders. Grid connection of wind farms presents many challenges, one of which is power quality. Wind farms have two major adverse points in power quality: an uneven output power and harmonic generation [3,36]. In addition, voltage fluctuations result as a consequence of non-homogeneous power productions. The main mechanisms influencing the power fluctuation are wind speed variation and the operation of the wind turbine itself.

The main factors behind wind speed variations can be classified as external and internal to the wind farm. External factors are related to climate, weather, and other natural conditions. In this case wind turbines, especially fixed-speed types, present output power variations of up to 20% of the average power [3,37]. Internal factors are related to wind random trajectories between towers, the wind shear, aerodynamics effects when the wind turbine blades pass the tower [3] and other turbulence phenomena. The dominating power fluctuation periodic component is related to the number of times that a blade passes the tower per revolution. For three-blade turbines, which are the most common, the power output repeatedly peaks at a frequency termed $3p$, where p stands for rotational speed of the turbine [3]. Additional power pulsation frequencies can be found at $6p$, $9p$, $12p$ and higher [3]. The $3p$-pulsation frequency strongly depends on the wind turbine characteristics; a general frequency range is between 1 and 3 Hz [3,4]. A far less severe $3p$-pulsation impact is obtained with variable-speed turbines, as the rotor and the output power are de-coupled, however, 10Hz voltage fluctuations have been reported [4]. The voltage fluctuation increases at high wind turbulences for both types of wind turbines; being less with variable-speed turbines. Further factors affecting levels of voltage fluctuation are summarised as follows [3,4]:

- Correlated or uncorrelated operation of the wind turbines: The voltage fluctuation produced by a wind farm becomes smoother as the number of wind turbines increases, which is particularly evident when each individual turbine operates in a non-correlated fashion [3,16]. For short-term periods, however, the wind turbines operation can be correlated, as they fall into synchronism, and the smoothing effect disappears, increasing the voltage fluctuation following a linear additive law. The parameter P_{st} tends to be greater in a correlated situation than in an uncorrelated one.

It has been mentioned in the open literature that wind turbines synchronisation can occur if the wind farm is connected to a weak electric network and the voltage fluctuation amplitude is high [37]. However, it should be investigated further.

- Start ups and stop downs of wind turbines: Severe power fluctuations caused by wind turbines start ups and stop downs also lead to voltage fluctuation [4,38]. This power quality detrimental effect can be reduced by using a soft starter mechanism, limiting the inrush current during the turbine energisation period [39], combined with a centralised control strategy; effectively enforcing the non-coincident start-ups of the various wind turbines.

- Ratio between the network short-circuit level (SCL) and the wind farm at the point of common coupling: When the wind farm's SCL approaches the grid's SCL at the point of common coupling, the impact of voltage fluctuations on the network is greater [40,41]. In general, the wind farm active power fluctuation is the major contributor to voltage fluctuations when the system is connected to a weak electrical network whilst reactive power fluctuation is the major contributor to an electrical network with high SCL [3]. Furthermore, under specific critical conditions, a large wind farm connected to the remote end of a regional distribution network can present voltage stability problems and thermal overloads due to the long distance and the limited transmission capacity, resulting in a total voltage collapse if the maximum power wind generation level is exceeded [42]. As a general rule to keep voltage fluctuation increments at bay, an SCL ratio of around 20 between the electrical network and the connected wind farm yields acceptable results [3]. Most distribution systems were not designed for the connection of generators, as it is the case today. So far, the total generator power that can be injected into the grid can be very limited. It is clear that if no adequate solutions are found for connecting generator to weak networks, areas with substantial wind resources will not be adequately exploited.

2.2.4 Other Voltage Deviation as Sources of Flicker

Abnormal operating conditions such as voltage sags, voltage swells, impulses, and voltage interruptions provoke sudden deviation in the line voltage and therefore induce light fluctuations. Furthermore, this variation in voltage can adversely affect power apparatus and sensitive equipment supplied by the system. Depending on the typical

time interval of each voltage deviation event, they can be categorised as transient, short-duration or long-duration variations [43]. These phenomena are non-repetitive in nature, however, events with duration from 1 ms and over can cause light deviations to be noticed by very sensitive customers, a little blink or a transitory blackout, these can be quantified as low and very low frequency light flicker. The P_{st} curve, shown in Figure 2.6, clearly indicates that the longer the duration and amplitude of the event the longer the P_{st} being measured. It is important to remark, however, that deviations less frequent than one fluctuation per hour are not included because the P_{st} concept is not applicable to such case [44]. When evaluating P_{st} in a network, the contribution from non-fluctuating voltages could be considered in addition to the flicker contribution produced by repetitive voltage fluctuations.

2.3 FLICKERMETER IEC-61000-4-15

Many different types of flickermeters have been proposed in the open literature [45-51]. The flickermeter specified by the standard IEC-6100-4-15 [7], identified in this research as IEC-Flickermeter, gives an accurate flicker perception level, and provides guidelines for the instrument's construction. Based on the IEC-Flickermeter instantaneous output, the standard provides an additional statistical analysis method for steady and dynamic flicker severity evaluations over short and long observation intervals, P_{st} and P_{lt}, respectively. Many PC-based and DSP-based IEC-type flickermeters are reported in the open literature [18,21,52-57]. This in itself is an indicative of the increasing acceptance of the standard. The generic IEC-Flickermeter block diagram is depicted in Figure 2.10 the functional blocks of the IEC-Flickermeter are:

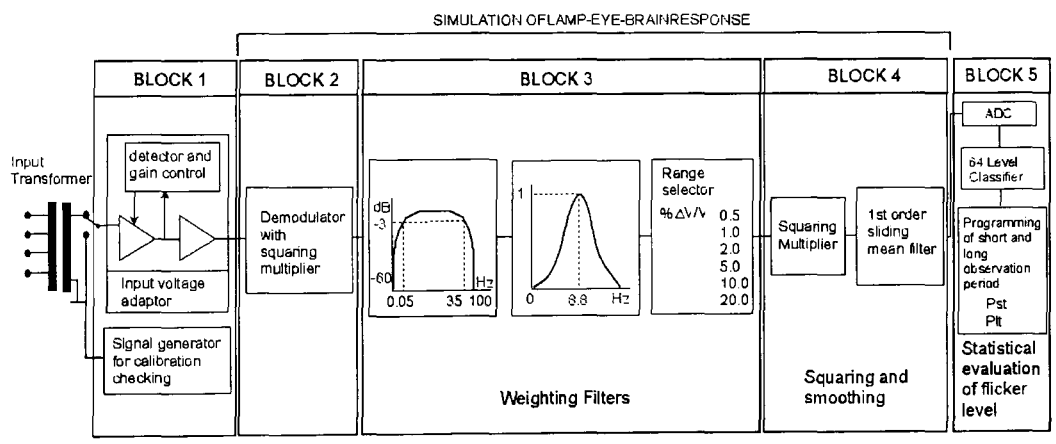


Figure 2.10. IEC-Flickermeter block diagram

- Block 1. Input voltage adaptor: The input line voltage from the mains is scaled down to an internal reference voltage level which remains constant, enabling the flicker measurement to be expressed as a percentage ratio.

- Block 2. Square law demodulator: The modulating waveform is extracted from the input voltage using a square law processing. This block output simulates the incandescent lamp behaviour.

- Block 3. Weighting filters: The dc, ripple and other undesirable frequency components accompanying the output are suppressed by using low-pass and high-pass filters. Also the modulating fluctuation is weighted according to the lamp-eye-brain sensitivity relation. The weighting transfer function for this block is:

$$F(s) = \left[\frac{k\omega_1 s}{s^2 + 2\lambda s + \omega_1^2}\right] * \left[\frac{1 + \frac{s}{\omega_2}}{\left(1 + \frac{s}{\omega_3}\right) * \left(1 + \frac{s}{\omega_4}\right)}\right] \tag{2.8}$$

The filter response for this function is based on a perceptibility threshold determined on the response of the majority of the persons tested in a range of voltage fluctuation frequencies and amplitudes.

- Block 4. Squaring and smoothing: There are two main functions in this block: a) the squaring of the weighted signal, to simulate the non-linear eye-brain behaviour; b) the storage mechanism effect in the brain simulated by a sliding mean averaging technique. A squaring multiplier accomplishes the former and a 300ms time constant first-order low-pass filter issued for the latter. The overall combined non-linear analogue response from blocks 2, 3 and 4 simulates the human flicker sensation due to the lamp, eye and brain system and corresponds to the curve presented in Figure 2.5. The output of block 4 represents the instantaneous flicker sensation, IFS.

- Block 5. On-line statistical analysis: The flicker severity indices are derived by statistical analysis from IFS measurements. The P_{st} is derived from IFS measurements observed in a short period of time, usually 10 minutes term. The P_{st} is calculated using the following equation

$$P_{st} = \sqrt{0.0314P_{0.1} + 0.0525P_{1s} + 0.0657P_{3s} + 0.28P_{10s} + 0.08P_{50s}} \qquad (2.9)$$

$P_{0.1}$, P_1, P_3, P_{10} and P_{50} are the percentiles representing the exceeded flicker levels for 0.1, 1, 3, 10, and 50 % of the time, during the observation interval. Furthermore "s" indicates the use of smoothed percentile values based on equations 2.10 to 2.13.

$$P_{1s} = (P_{0.7} + P_1 + P_{1.5})/3 \qquad (2.10)$$

$$P_{3s} = (P_{2.2} + P_3 + P_4)/3 \qquad (2.11)$$

$$P_{10} = (P_6 + P_8 + P_{10} + P_{13} + P_{17})/5 \qquad (2.12)$$

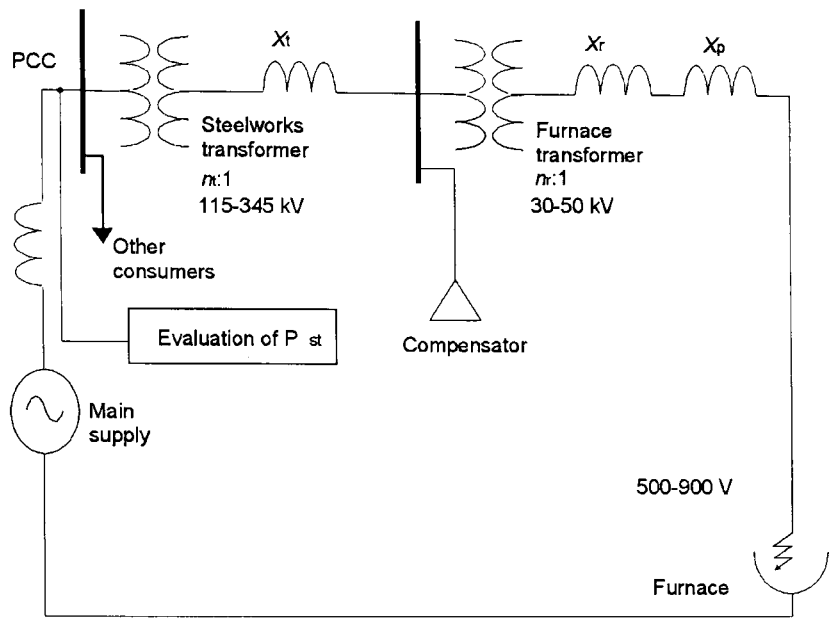
$$P_{50s} = (P_{30} + P_{50} + P_{80})/3 \qquad (2.13)$$

For flicker evaluations over long observation periods, the long-term severity index P_{lt} is used, expressed by equation 2.14.

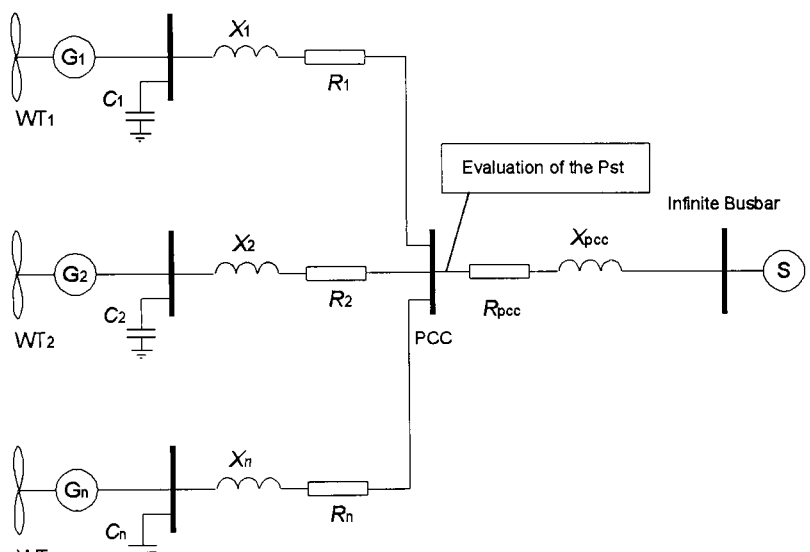
$$P_{lt} = \sqrt[3]{\frac{\sum_{i=1}^{N} P_{st_i}^3}{N}} \qquad \text{where } i = 0,1,2,... \qquad (2.14)$$

2.4 EVALUATION OF FLICKER SEVERITY USING IFS AND P_{st}

The instantaneous flicker sensation varies with the instantaneous line voltage fluctuation. Since the IFL and P_{st} exhibit a non-linear relationship, the estimation of P_{st} based on tables, with constant IFS, yields no meaningful insight on dynamic voltage fluctuations in the network. If the line voltage fluctuations have constant-amplitude and frequency (single sinusoidal waveform) over ten minutes or more, the IFL remains almost constant and so does the respective P_{st}, which can then be calculated from tables. For any practical purpose of voltage fluctuation, this can be considered a case of steady-state voltage fluctuation propagation, whose analysis is useful for the steady-state assessment of new voltage fluctuation sources. The voltage fluctuation injected into the electrical network is normally evaluated at the point of common coupling. Figure 2.11 illustrates the P_{st} measurement points for EAF and wind farm installations. Figure 2.12 shows multiple P_{st} measurement points needed for multiple sources of voltage fluctuation.



a)



b)

Figure 2.11. Points for P_{st} evaluation: a) EAF; b) wind farm.

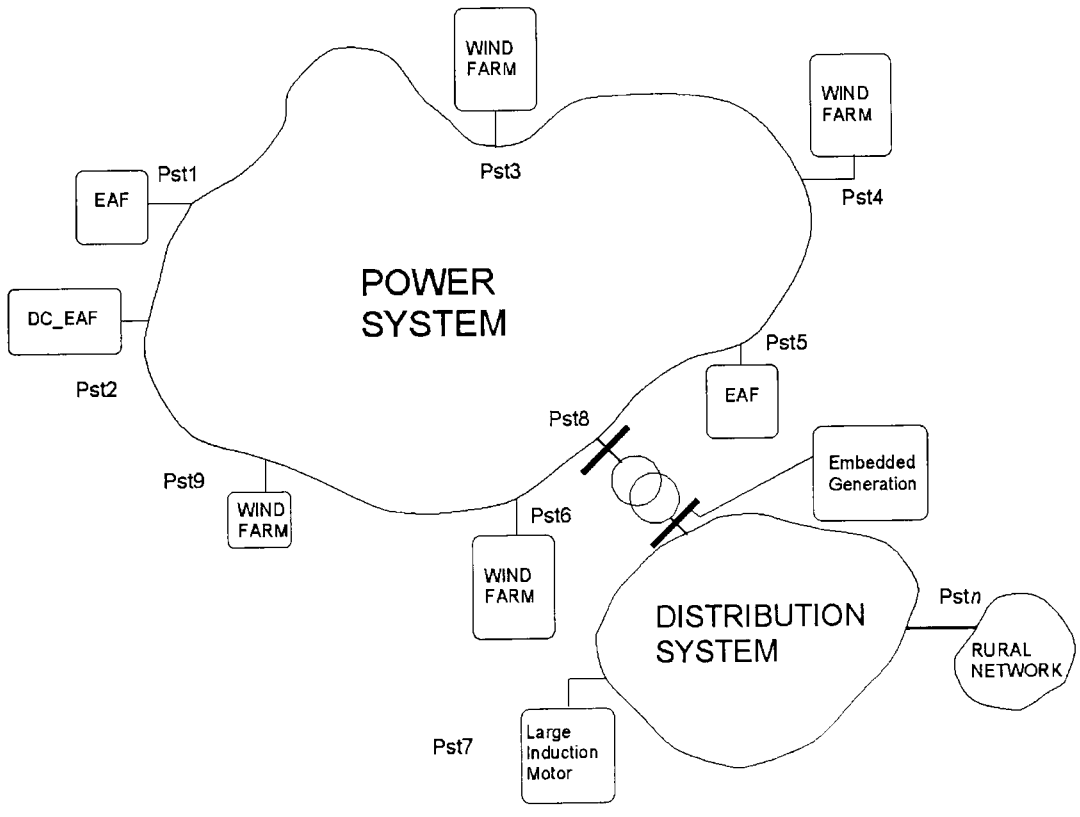


Figure 2.12. Multi-point P_{st} evaluation.

An indirect measurement technique for the instantaneous voltage fluctuation of a single source connected to the grid can be applied in order to minimise errors. The technique uses a fictitious grid circuit where the voltage fluctuations are calculated based on the direct measurement of the instantaneous current according to equation 2.15 [3]

$$V_{fic}(t) = v_o(t) + R_{fic}(t) * i_{meas}(t) + L_{fic}(t) * di_{meas}(t)/dt \qquad (2.15)$$

A direct simultaneous multiple point P_{st} measurement in a wide area is not an easy task to carry out. In fact, the few direct multi-point P_{st} measurements reported in the open literature have been carried out in networks with a single source of voltage fluctuation; both an EAF and a wind farm have been used [27,36,58-61]. Multiple P_{st} evaluations have resulted from simulated propagation analysis in steady-state, and reported for different nodes of transmission systems [24,36,58,62,63]. These multiple P_{st} calculated indices are useful for comparison purposes.

2.5 PROPAGATION OF VOLTAGE FLUCTUATIONS

A comprehensive propagation analysis of voltage fluctuation should focus on the flicker severity evaluation at all the network nodes. In the open literature a limited number of references address the subject. These propagation studies are based on a single source of disturbance, either electric arc furnaces or wind farms, but the information provided on techniques, procedures and modelling is useful for understanding the propagation phenomena. A summary of the steps used in the current propagation analysis of voltage fluctuation is as follows [24,36,62,64]

- Voltage fluctuation and network modelling are carried out in the frequency domain.
- Use of PSCAD/EMTDC, EMTP, HARMAC or tailor-made software for the evaluation of voltage fluctuation frequency spectra propagating throughout the network.
- Off-line determination of P_{st} for steady-state conditions using a flickermeter-type digital algorithm.
- Either, summation of individual P_{st} in each node or summation of the propagation of collective voltage fluctuations in each node and then calculation of P_{st}.
- Evaluation of results.

2.6 CONVENTIONAL AND MODERN SOLUTIONS FOR VOLTAGE FLUCTUATION MITIGATION

In modern utilities power quality is an issue of growing concern. Further to voltage and current harmonics, light flicker is becoming a relevant power quality issue, as the customer complains increase due to excessive P_{st}. Voltage stabilisation in the PCC improves the EAF, DC-EAF, and wind farm performance. The techniques used for voltage stabilisation are also aimed at reducing voltage fluctuations, particularly when shunt-connected compensation equipment is used. Current mitigation practices involve power electronic controllers, mainly based on voltage-source-inverter technology, giving a better voltage and current controllability to the electrical systems and, thus, mitigating voltage fluctuations.

IEC provides authoritative documents on flicker severity limits, in terms of P_{st}, for grid-connected equipment at different voltage levels [9-12], and power quality requirements for wind turbines [65]. Based on this parameter, it is possible to identify, at the design stage, whether or not there is a need for voltage fluctuation mitigation equipment in new installations (EAF, DC-EAF, wind farm). In the open literature, P_{st} level prediction techniques are also found for wind farms [66] and EAFs [6,67-71]. In the case of electric arc furnace, the non-P_{st} Short-Circuit Voltage Depression (SCVD) method [6] has been used in industry for quite some time to roughly estimate the voltage fluctuation at PCC. For existing installations, flicker severity is evaluated by direct P_{st} measurements at PCC or in a nearby point. If the flicker irritation limits are exceeded, the need for voltage fluctuation mitigation is taken under consideration. A summary of the common practices combining conventional and modern voltage fluctuation mitigation strategies are presented below:

- Stiffening the supply: In this case the wind farm or the EAF is tapped to a higher voltage level. Although this option is preferable from the utility point of view, it is expensive for the plant shareholders [1,6].

- Installation of a higher rated power transformer: This is also an expensive option but useful when expansion in the capacity of the EAF [6] is required. A typical application example for transformer replacement is reported in [72].

- Rated power reduction of the plant: This technique consists in the reduction of the EAF furnace load, which reduce the voltage fluctuation below flicker irritation levels. Commonly the utility request the reduction to the customer [27], but the solution is economically valid for only short periods of time [25,73].

- Installation of series passive devices: Inserting a series inductor at the supply side of the furnace transformer is a useful, proven resource. Extensive computer simulations have shown that this is a relatively effective method for voltage fluctuation minimisation. A reduction between 60% and 80% is reported in the open literature using this scheme [25,73]. The series inductor reduces the power factor but reactor size is limited by arc stability. This practice is common in Northern Italy.

In the distribution feeder, an economic practice for voltage fluctuation reduction has been the installation of a series fixed capacitor [74-77], which increases the short circuit level by effectively reducing the line inductive reactance, particularly at the point where the voltage fluctuation source is tapped-off.

In general, voltage fluctuations are less severe if the source of disturbance is connected closer to the supply source where the short-circuit level is higher. This phenomenon can be understood as an incremental or amplifying effect takes place during the propagation of the voltage fluctuation, and can be attributed to the increment of the total equivalent inductive reactance in the line, reducing the short-circuit capacity from the source of voltage fluctuation until the far away node where the P_{st} is measured. In a different context but similar circumstances, this amplifying effect has been reported following extensive evaluation measurements of voltage fluctuation in the neighbourhood of an EAF [27].

The fixed capacitor provides limited voltage fluctuation reduction in the line, particularly for wide-band frequency varying fluctuations. However, this cost-effective practice has been in use for well-established companies. Arkansas Power and Light installed a series capacitor for an industrial wood-chipping mill [17] and General Electric has installed a number of series capacitors as a solution for feeder voltage drop caused by chipper, EAF, and a 600 HP motor start among others [77]. Similarly, ABB connected a series capacitor at the

Bällefors substation, Sweden, to reduce voltage fluctuations and to increase the voltage level [76].

- Installation of the source of disturbance in a separate transformer: When sensitive equipment in a large plant is affected by voltage fluctuations, the source producing the phenomenon is isolated using a separate transformer or feeder, hence, diminishing the problem [1].

- Installation of shunt compensation equipment: In the 1950's, the earliest compensation apparatus were based on saturable reactors for use in the metal reduction industry [78]. Other solutions were also available, such as the synchronous condenser, which showed limited capacity for mitigation [78]. The shunt-connected thyristor-controlled compensator is currently the most-widely used equipment for both control of reactive power and for voltage fluctuations mitigation. Table 2.3 shows some the advantage and disadvantages of the various compensation technologies applied to EAF [6,74].

Table 2.3 EAF compensation techniques

Voltage Fluctuation Equipment/Technique	Advantages	Disadvantages
Thyristor-controlled reactor	Rapid response	Requires shunt capacitor for PF correction Generates harmonics
Thyristor-switched capacitor	No harmonics generated No reactor required Independent operation of phases	Limited speed of response
Tapped reactor/saturated reactor	Rapid response gives large mitigation Independent operation of phases Transformer-type construction	Requires large shunt capacitor for PF correction Generates harmonics Applicable only to one furnace
Harmonic-compensated saturated reactor	Rapid response Negligible harmonics generated Transformer-type construction	Requires shunt capacitor for PF correction Energising transients Phases not independently controlled
Synchronous condenser		Requires regular maintenance Limited voltage fluctuation mitigation even with buffer reactor

The use of shunt-connected advanced technology based on Voltage Source Converters (VSC) has shown great effectiveness in controlling the line voltage, power factor correction, and voltage fluctuations mitigation. Three major technical advantages have proved decisive for the adoption of this technology [16]:

- Extended capability to control reactive power, and real power for some configurations
- Greater flexibility and higher speed of operation
- Improved dynamic performance

The EAF plants are leading the way in the installation of advanced compensation technology [78-82]. The STATCOM installed in Structural Metals Inc, in Seguin, Texas [79], and the SVC-Light in Uddeholm Tooling AB, Hagfors, Sweden, are two examples of applications of this technology [80,81]. Currently CIGRE is preparing a document for application of STATCOM to EAF compensation [83].

The VSC-based power compensator has also been applied to improve the operation of wind farms [81,84-86]. The Rejsby Hede project is one the earliest projects where STATCOM GTO-based were installed [86]. The main purpose of the project is the dynamic reactive power compensation for power quality improvement and prevention of damaging overvoltages in the event of wind farm islanding. Further research on wind turbines corroborates the usefulness of the STATCOM as mitigation equipment [85].

Conventional thyristor-controlled type equipment has been developed and tested on site for cases of voltage fluctuation caused by the operation of a lumber mill operation at the end of a rural feeder [15] and a three-phase welder connected at a 480V line [57], although VSC-based equipment has also found favour in industry and distribution systems [81,87-90]. The D-STATCOM installed for a timber mill at the far end of a long distribution feeder [88] and the one installed at Seattle Iron & Metals for a 4000 Hp shredder motor are two relevant examples where the VSC technology is being used [87].

2.7 RESIDUAL VOLTAGE FLUCTUATIONS

Mitigation schemes are not ideal, and to a greater or lesser extent voltage fluctuations will remain in the electrical network. This phenomenon is identified and termed in this research work as residual voltage fluctuations, having a residual P_{st}, with the ability to

propagate and to add to voltage fluctuations already present in the electrical system from other sources. It is argued that the overall voltage fluctuation resulting from such a summation can eventually lead to a P_{st} well above the limit of irritability, leading to complains from customers. To the best of the author's knowledge, the mitigation of residual voltage fluctuations propagating in transmission and distribution electrical systems using shunt or series-connected FACTS equipment has not yet been addressed in the open literature.

The inclusion of a new range of compensators in combination with the well-established FACTS and Custom Power controllers should lead to near zero residual voltage fluctuation in upstream electrical networks from HV to LV voltage levels.

2.8 DISCUSSION

The voltage stability, and so the voltage fluctuations, at the point of common coupling is related with the ratio between short-circuit capacities of the utility and the source of voltage fluctuation. The flicker can be roughly estimated for EAFs using the so called "Short Circuit Voltage Depression" (SCVD) or another similar technique. The estimation or prediction of flicker at the design stage of a new installation can be helpful providing information to determine, for instance, the characteristics of mitigation equipment and control strategy.

Although some research has been made about the prediction of voltage fluctuation and flicker with EAF and wind farms, the estimation of IFL and P_{st} in a multi-voltage fluctuation sources scenario envisaging summation and propagation of correlated and non-correlated voltage fluctuations; which also include transmission system and distribution networks configuration, embedded generation, EAF, DC-EAF, large induction motors and other fluctuating load; still require more research attention.

For various decades several flickermeters, IEC and non-IEC type, have been proposed in industry and academia, some of them are modification to the actual standard IEC-61000-3-15. Rather than suggesting a complete new measurement procedure or instrumentation methodology, which includes the human response to flicker, most of the these proposal have been aimed at changing the data processing from analogue to digital using advanced digital processing.

In general, the results are supported with far from conclusive field tests or simulations but excluding in all cases an intensive testing of the device ranging from single frequency steady fluctuations to rapidly changing multi-frequency fluctuations. Problems associated with the FFT (such as windowing process, numerical truncation errors), an extensive testing methodology, and the loss of information while converting the input signals to digital data are some few points to take into consideration when working in a serious standard proposal for a digital IEC-flickermeter.

The use of artificial intelligence techniques; spectral analysis techniques and advanced signal processing techniques may in some few cases accelerate the calculation of frequency and magnitude of the fluctuations or the instantaneous flicker sensation. Digitalising the transfers functions of an analogue instrument (changing from the Laplace transform to the Z transform) does not make a better instrumentation or make any important improvement to the measurement process *per se*. Non-sinusoidal voltage and currents in the electrical networks, particularly in distribution systems, adversely affects the power quality. Harmonics, inter-harmonics and voltage fluctuations belong to this category.

In harmonics analysis, the techniques just mentioned have been well accepted and they have also contributed to better understanding electrical systems under non-sinusoidal situations in both steady and transient state. The main reason behind this can be the importance to rapidly predict and quantify the magnitude, frequency and relative phase of the distorted signal in order to determine their propagation in transmission and distribution systems, and the adverse impact in the operation of a sensitive load that can implicate economical losses for the industry. However, this is not the case when dealing with voltage fluctuations because most of the loads are not seriously disrupted, or damaged, and so far, no economical lost has been reported for such phenomenon. The main concern is focused to quantify the annoying effects in humans, provoked by light flicker, and the respective complains to the utility. As the flicker is a human related power quality issue, in a non-lighted network or in a circuit where no persons is present nearby, voltage fluctuations is not a problem for the utility.

An IEC-type flickermeter using spectral analysis and digital processing techniques, to faster calculate the instantaneous flicker sensation, does not have any realistic advantage over the basic analogue IEC-flickermeter, mainly because the procedure to quantify the flicker severity indexes, P_{st} and P_{lt}, remains unchanged. It is notorious that even when

the harmonic and inter-harmonics can be included in the calculation of the rms, the fluctuations caused by these non-sinusoidal signals may be significant only for highly distorted signals, condition that occurs for few minutes in the bore-down stage of melting process in the EAF and the DC-EAF. Moreover, because the 0.05-35 Hz filtering bank included in the IEC-Flickermeter, the harmonics and inter-harmonics do not represent a great challenge for the instrument, as they are strongly attenuated, representing only minor deviations in the subsequent processing to obtain IFS.

In the 10 minutes required the statistical evaluation of P_{st} and the 120 min for P_{lt}, the relevance of spectra analysis and frequency domain techniques in the design of a flickermeter came into a question, as they are not likely to be important.

2.9 CONCLUSIONS

A critical review of sources of voltage fluctuation and light flicker phenomenon has been presented in this chapter together with associated operational problems, measurements and remedial measures. As discussed, these phenomena affect negatively the electrical networks. The mechanisms causing voltage fluctuation, and its propagation in the electrical networks has been reviewed, which together with the use of standards, definitions, and IEC-Flickermeter description provide key knowledge for the evaluation of P_{st} and identification of potential high levels of voltage fluctuations at a given node, load, and circuits, helping also to select the best mitigation equipment.

The concepts and terminology of voltage fluctuation and flicker severity have definitions not yet widely accepted. The IEC-61000-4-15, however, has proven useful in practical measurements with real life electric systems, avoiding misinterpretations. The set of flicker-related IEC standards are becoming widely accepted standard documents.

The P_{st} is becoming an important voltage fluctuation and flicker evaluation parameter. The P_{st} obtained in different nodes of a network from direct measurements or digital simulations can be used to assess the voltage fluctuation propagation phenomenon in transmission and distribution systems. This helps to identify the badly affected nodes, loads, and sensitive customers. The residual voltage fluctuations, and correspondent residual P_{st}, has been identified as the remaining voltage fluctuations propagating in the network due to the no ideal mitigation of a voltage fluctuation sources. Modern series FACTS and Custom Power controllers have not been discussed yet in the open literature equipment capable of mitigating such residual voltage fluctuations.

The voltage fluctuation incremental phenomenon occurring while the distorted waveform travels in the electrical network has been briefly analysed. This condition becomes more noticeable when the network is weak and the PCC is electrically far away from the point where flicker evaluation takes place. The mitigation schemes and equipment for this condition require more attention.

High-frequency harmonics and inter-harmonics injected into the electrical network during the operation of a DC-EAF and EAF have been reported to be causes of flicker in fluorescent lamps. The mechanisms of this interaction are still not well understood. In this chapter, similarities in fluctuating waveforms are established between voltage fluctuations resulting from harmonic and inter-harmonic modulation, and those obtained by modulating frequencies not higher than half the nominal fundamental frequency. To the best of this author's knowledge, the mechanisms associated with this phenomenon have not been yet reported in the open literature. However, it should be noted that due to a frequency spectra relationship, the voltage line in transmission and distribution systems can not fluctuate at frequencies above half the nominal system fundamental frequency, even when the modulating frequency spectrum contains high frequencies.

The voltage fluctuating frequencies produced by the EAF, the DC-EAF, wind farms, large induction motors and other sources fall into the 0.1 – 25 Hz (50Hz systems) and 0.1 – 30 (60Hz systems) range. These frequency spectra ranges are useful in determining the voltage fluctuation propagation and the characteristics of the mitigating control schemes.

Several conventional and modern voltage fluctuation mitigating equipment and techniques have been analysed. The use of FACTS and Custom Power technologies has enhanced power quality in the electric systems. The STATCOM effectiveness has been proven in actual operation, improving the overall operation performance of wind farms and EAF. Moreover, the use of modern mitigation equipment, improved DC-EAF performance, and variable-speed wind turbines will decrease further voltage fluctuations in future electrical networks. A variety of control schemes are applied to the operation of compensating equipment. The possibility of using control strategies based on voltage fluctuation evaluation figures, such as P_{st}, is open.

Abnormal system phenomena such as voltage sags, voltage swells, voltage interruptions, and others similar events, deviate the line voltage from their ideal

sinusoidal waveform. The impact of these events on industrial equipment has been widely addressed in the open literature. However, the effect of these events on the IEC-Flickermeter and Pst index requires more research attention.

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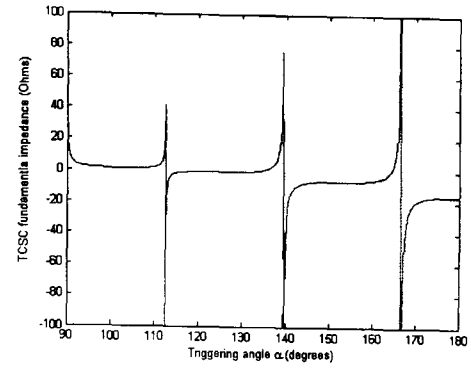
CHAPTER

3



THYRISTOR CONTROLLED SERIES CAPACITOR: MODELS, CHARACTERISTICS AND APPLICATIONS

3.1 FACTS AND CUSTOM POWER CONTROLLERS: A SURVEY

The FACTS and Custom Power technology is a recent development, of great strategic significance to the modern utility. At high-voltage transmission one of the aims is to increase power flows across key corridors, with total controllability and near-zero risk to security of supply. At low-voltage the aim is to improve all aspects of power quality and reliability of supply. In the fullness of time, once the incorporation of the new technology takes place in earnest, an increase in operational complexity is expected. The same holds true for the planning of transmission and distribution networks. These developments, no doubt, will also affect the way in which energy transactions are conducted, due to the high-speed control afforded by the new technology.

FACTS and Custom Power applications are based on the use of the latest high-speed power electronics technology, modern control methods and advanced processors. The FACTS controllers are connected to the high-voltage side of the transmission network to provide the necessary transmission line parameters compensation, in an adaptive

fashion, to control the power flow in key transmission paths. Such a control action will also result in an increase in power transfer by minimising the gap between stability and thermal limits. These controllers have the ability to control the voltage magnitudes, the line impedance and the phase angles at the line ends of key transmission corridors and, at the same time, enhance the security of the system.

3.1.1 FACTS Controllers

Conventional control of power flow relies upon generator control, transmission line reactive compensation switching, and voltage regulation via electro-mechanical tap-changer and phase-shifter transformers [1-6]. The non-flexible characteristics of the apparatus are reflected in the restricted operating range that some of them have shown by permanently functioning with fixed phase angles. Series capacitors are commonly used to compensate the inductive reactance of transmission lines, shortening the electrical length of the line and, consequently, increasing power flow [7-9].

The great many advances in power electronics during the last decade, has resulted in a large production of cost-effective devices capable of withstanding high voltages and currents at high speed. These achievements have opened the possibility of constructing equipment capable of operating at voltage and current levels commensurate with those used in power systems. Power electronic versions of conventional phase shifter and tap-changer transformers were the first type of FACTS equipment embraced by the proponents of this technology [1-6]. Further developments included the Thyristor Controlled Series Capacitor, the Unified Power Flow Controller, the Static Compensator and Interphase Power Controller [7-17]. It is worth mentioning that some power electronic-based controllers have been in existence for many years, long before the FACTS concept appeared [18,19]. The better known equipment is the shunt-connected Thyristor Switched Capacitors (TSC), the Thyristor Controlled Reactors (TCR) and the High-Voltage Direct Current (HVDC) power converters.

The variety of novel power controllers and applications that are emerging under the FACTS initiative continue to increase. These controllers are designed to function effectively during both steady state and transient operation, but some FACTS devices, are specially designed to operate exclusively under transient conditions. A case in point is the Subsynchronous Resonance Damper authored by Hingorani [17]. A description of representative FACTS controllers are detailed below [18-21]:

Thyristor Controlled Reactor (TCR): It is a shunt-connected equipment comprising a reactor in series with an anti-parallel thyristor, which provides smooth reactance control using its partial conduction control characteristics.

Thyristor Controlled Phase-Shifting Transformer (TCPST): This device consists of a phase-shifting transformer adjusted by a set of thyristor switches to provide a rapidly varying phase angle.

Thyristor Controlled Series Capacitor (TCSC): This FACTS controller functions as a series reactance, consisting of a series capacitor bank shunted by a thyristor controlled reactor; and designed to provide smooth variable series compensation, primarily capacitive.

Thyristor Switched Series Capacitor (TSSC): This controller behaves as a capacitive reactance compensator. It consists of a series capacitor bank shunted by anti-parallel thyristor switches to provide control of the series capacitive reactance.

Thyristor Controlled Braking Resistor (TCBR): This device is a shunt-connected thyristor switched resistor, designed to enhance power system stabilisation by reducing rotor acceleration in generating units following a disturbance.

Static Synchronous Compensator (STATCOM): This device has the operating characteristics of a static synchronous condenser operated as a shunt connected static var compensator. The capacitive or inductive output current of the device can be controlled independently of the ac system voltage magnitude. The magnitude of the voltage at the ac node is usually the reference variable to be controlled. Alternatively, the reactive power injection can also be used as reference. A Static Synchronous Generator (SSG) is the combination of a STATCOM and a suitable source from which to supply or absorb power.

Static Synchronous Generator (SSG): This controller is a static self-commuted switching converter supplied from a suitable electric source. The device is operated to produce a number of adjustable multiphase output voltages that may be coupled to an ac power system to exchange controllable active and reactive power, in an independent fashion

Static Synchronous Series Compensator (SSSC): This controller consists of a static synchronous generator operated as a series compensator, without an external energy-supplying source. The output voltage of this device is 90° out of phase respective to the line current in order to control the increase/decrease of the overall reactive voltage drop in the transmission line and, thereby, controlling the electric power to be transmitted. The output voltage is controlled independently of the line current. The SSSC enhances the dynamic behaviour of the system if a transiently rated energy storage exists

Interline Power Flow Controller (IPFC): This device is a novel concept recently added to the array of FACTS controllers. So far, there is no widely accepted definition for it. Dr. Hingorani has advanced the following [20]: *The IPFC is a combination of two or more Static Synchronous Series Compensators which are coupled via a common dc link to facilitate bi-directional flow of real power between the ac terminals of the SSSC's, and are controlled to provide independent reactive compensation for the adjustment of the real power flow in each line and maintain the desired distribution of reactive power among the lines.* The IPFC structure may also include a STATCOM, coupled to the IPFC's common dc link, to provide shunt reactive compensation and to supply or absorb the overall real power deficit of the combined SSSCs.

Unified Power Flow Controller (UPFC). This controller combines two well defined structures, namely the STATCOM and the SSSC, which are coupled through a common dc link. The controller allows bi-directional flow of real power between the series output terminals of the SSSC and shunt output terminals of the STATCOM. The UPFC, by means of an angularly unconstrained, series voltage injection, is able to control, concurrently or selectively, the transmission line impedance, the nodal voltage magnitude and the real and reactive power flow in the line. The UPFC may also provide independently controllable shunt reactive compensation.

Static Var Compensator (SVC): This equipment is a shunt-connected static var generator or absorber whose output is adjusted to exchange capacitive or inductive current so as to control specific parameters of the electrical power system.

NGH-SSR Damping Scheme: This is a FACTS controller developed for the special purpose of damping subsynchronous resonances. Its structure is similar to that of the TCSC, however, one of the main differences is in the inclusion of an additional resistor which is connected in series with the thyristor module and reactor.

The applications of FACTS controllers and their control attributes are presented in Table 3.1[20]

Table 3.1 FACTS controllers and its control attributes

FACTS Controllers	Control Attributes
Static Synchronous Compensator (STATCOM without storage)	Voltage control, VAR compensation, damping oscillations, voltage stability
Static Synchronous Compensator (STATCOM with storage)	Voltage control, VAR compensation, damping oscillations, transient and dynamic stability, AGC
Static VAR Compensator (SVC, TCR)	Voltage control, VAR compensation, damping oscillations, transient and dynamic stability
Thyristor Controlled Braking Resistor (TCBR)	Damping oscillations, transient and dynamic stability
Static Synchronous Series Compensator (SSSC without storage)	Current control, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting
Static Synchronous Series Compensator (SSSC with storage)	Current control, damping oscillations, transient and dynamic stability, voltage stability
Thyristor Controlled Series Capacitor (TCSC, TSSC)	Current control, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting
Thyristor Controlled Series Reactor (TCSR, TSSR)	Current control, damping oscillations, transient and dynamic stability, voltage stability, fault current limiting
Thyristor Controlled Phase Shifting Transformer (TCPST)	Active power control, damping oscillations, transient and dynamic stability, voltage stability.
Unified Power Flow Controller (UPFC)	Active and reactive power control, voltage control, VAR compensation, damping oscillations, transient and dynamic stability, voltage stability, voltage stability, fault current limiting
Interline Power Flow Controller (IPFC)	Reactive power control, voltage control, damping oscillations, transient and dynamic stability, voltage stability

3.1.2 CUSTOM POWER CONTROLLERS

Custom Power controllers are aimed at the distribution system, where novel power electronic products are capitalised. It focuses on two main factors affecting industrial, commercial, and residential customers: the reliability and quality of power flows. An expert group on distribution systems originally conceived the concept of Custom Power at EPRI in the late 1980's [21]. Soon after the concept was profusely disseminated in industry and academia for a faster technological development and further research on

improvements and applications. The proliferation of highly sensitive, end-user equipment requiring high power quality supply has been running along with the marked increase of power electronics-based equipment. The latter are non-linear equipment which may produce a significant amount of harmonics affecting both voltage and currents waveforms of the supply. The most common disturbances in the distribution networks and the sources for such events are given in Table 3.2 and Table 3.3, respectively [23].

Table 3.2 Representative network disturbances

Symptom	Possible Cause
Supply outage Total loss of supply	• Accidents • Planned maintenance • Line faults
Overvoltage Long term increase in supply voltage	• Light system load • Poor voltage regulation
Voltage surge Medium term (ms-seconds) Increase 10-30% in amplitude	• Circuit capacitance • Switching out large loads
Undervoltage Long term depressed supply amplitude	• Heavy network loading • Lack of VAR support • Peak demand operation
Voltage sag Medium term dips in the voltage amplitude	• Large loads being switched in • Circuits breakers in operation • Large demands on the power supply • Inductive loading • Short-circuit faults in the neighbourhood
Voltage transient Short duration (ms) impulse Voltage spike	• Current surges caused by fast switching • Low fault current trip protection • Non linear switching loads e.g. rectifying units, variable speed drives and power conditioners and converter units • Transmitted noise through the supply system
Current harmonics and Periodic waveforms	• Increased use of non-linear circuit elements • High frequency switches, large concentration computer and fluorescent lighting
Electrical noise	• Disturbances between supply and earth • Series: disturbance between supply and neutral
EMI Susceptibility and generation of em radiation	• Generated by unshielded electrical equipment • Interference with radio and TV receivers

Table 3.3 Sources of disturbance

Feature	Possible problems
Conventional switchgear	• Mechanical operation • Require regular maintenance • Too slow to limit fast transient
Distribution topologies	• Not designed to deal with sensitive loads • Ring main systems facilitate the transmission of electrical noise and harmonics • Radial systems have inherent reliability problems
Back-up supplies	• Unsuitable location and specification
Switch mode power supplies	• Chop up the supply waveform • Lower the power factor
Computer and microprocessor operations	• There are non-linear devices • High frequency switching • Disrupt the supply signal • They are found in high volume
Frequency and voltage controlled equipment	• Non linear rectification utilised • Chop the supply waveform
Large load switching	• Imposes strain on the network
System overload	• Demand exceeds the line capacity • Protection equipment is not flexible

Many attempts have been made to counteract the abnormal situations debasing the power quality and reliability of distribution systems; among these are advanced solutions where power electronic-based technology figures prominently. The generic term for these solutions is termed Custom Power where the following equipment is the most widely used: Dynamic Voltage Restorer (DVR), Solid State Transfer Switch (SSTS) and distribution STATCOM (D-STATCOM or STATCOM) [21,23-25]. The DVR and the D-STATCOM base their operation on the use of the Voltage Source Converter (VSC) technology, whereas the SSB uses back-to-back connected thyristor switches. A description of these Custom Power controllers is given below [21,22,24,25]:

D-STATCOM: This controller consists of a converter with dc storage and a transformer. It is connected to the feeder, where it absorbs or supplies reactive and active power, seeking to retain the voltage at the point of connection at the required level. The basic configuration of the equipment includes a two-level VSC. Rather elaborated versions utilise multi-pulse and/or multilevel configurations. The controller can provide the reactive compensation to the full MVA rating of the power electronic values.

DVR: This system configuration consists of a converter, a dc storage capacitor, and a transformer connected in series with a distribution feeder. The controller provides compensation for voltage disturbances at the point of connection. The DVR structure consists of similar components to the D-STATCOM but having a different transformer connection to the network. A DVR with a dc storage unit is capable of injecting or absorbing active and reactive component from the line through the transformer, so that it can restore the line voltage to nominal following a sudden voltage sag or swell. This Custom Power controller is a very effective solution to ameliorate voltage sags and swells [24-29] and, in economical terms, this it is a more cost-effective solution than using the D-STATCOM [24].

SSTS: The basic configuration of this controller consists of two sets of three-phase thyristor switch modules connected back-to-back, one for the main feeder and other for the backup feeder. A single module of thyristor switches is referred to as solid-state circuit breaker (SSB). The SSB, and so the SSTS, continuously monitors the line current level. After a fault has been detected, by evaluating the rate of change of the instantaneous current, the detection mechanism urges the SSB into operation.

3.2 THYRISTOR-CONTROLLED SERIES CAPACITOR (TCSC)

In an ac power transmission line, voltage magnitudes and the phase angle difference between end nodes, as well as the total impedance between the two ends, determine the active and reactive power transfer.

When no power flow control exists in a transmission line, the impedance of the transmission corridor dictates the active and reactive power flow transfers, in inverse proportion. For the case of a simplified transmission line segment, containing only series reactance, the power flow is governed by [30]:

$$P_{SR} = \frac{V_S V_R}{X_L} \sin\phi \tag{3.1}$$

where:

V_S is the voltage at the sending terminal

V_R is the voltage at the receiving terminal

ϕ is the phase angle difference θ_S - θ_R

X_L is the series reactance of the line between end points

This simplified equation yields great insight into the control of active power flow. At a first glance, the variation of voltage magnitudes at the line ends seems to be a reasonable option. However, in general, power systems are designed to maintain the voltage magnitudes in system nodes within narrow maximum and minimum limits; the room for voltage magnitude adjustment is in fact very restricted. A plausible option for controlling power flow is to adjust the angle difference ϕ.

As the power flow is inversely proportional to the reactance of the transmission line, this parameter is also an attractive option for controlling power flow. Using this concept, several forms of shunt reactive compensation have been used to increase power transfer capability. The most common ones are the switched shunt capacitor, the thyristor-controlled reactor and the SVC.

A traditional approach to improve power transfer consists in the insertion of series capacitors to compensate the transmission line series reactance. The insertion of series capacitive reactance in a transmission corridor is amenable to compensating the voltage drop caused by the inductive reactance of the line. The reduction of the total effective impedance increases the power flow transfer limits in the compensated transmission line and improves stability limits.

Mechanically controlled series capacitor banks have been used for compensation for many decades. Although they represent an economic solution, the device is not suitable for high-speed control. Additional drawbacks are [18]:

- Lack of effective controllability in highly-compensated environments
- Lack of smooth variations of the series impedance
- Capacitor reinsertion generates a voltage offset across the capacitor
- Fixed percentage of reactive capacitive compensation relative to the transmission line impedance

Research on FACTS technology has produced electronically controlled devices such as the Thyristor Controlled Series Compensator (TCSC) and the Thyristor Switched Series Capacitor (TSSC), which provide reliable and effective solutions for series compensation of transmission lines. Figure 3.1 shows general configurations of series compensation schemes [8,31,32].

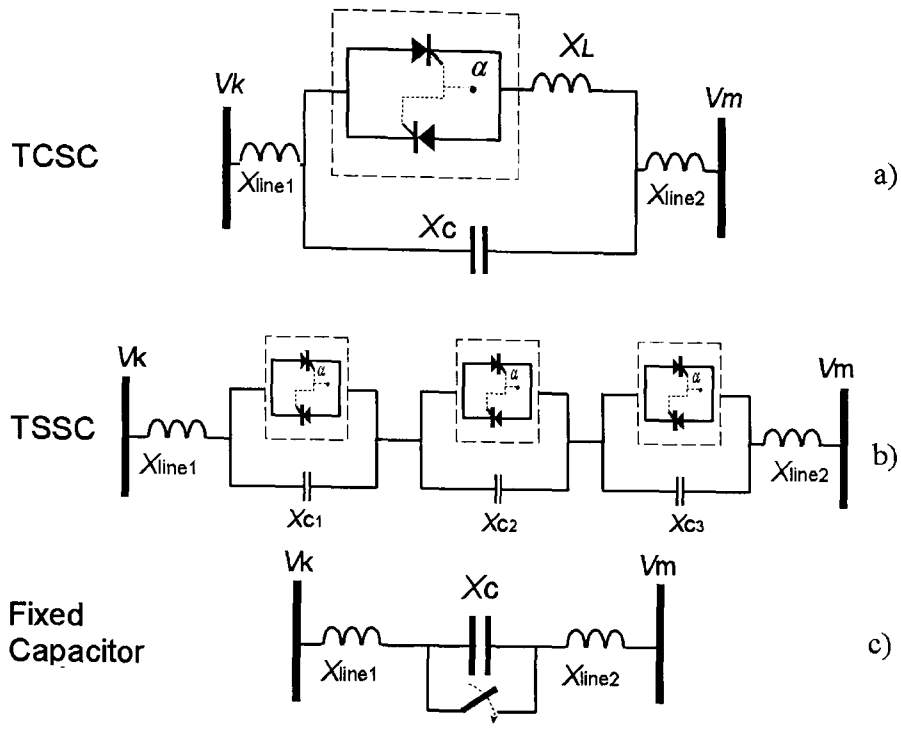


Figure 3.1. General configurations of series compensation schemes: a) single TCSC; b) multi-module TSSC; c) fixed capacitor

3.3 TCSC BASIC OPERATION

The TCSC is a FACTS controller developed to overcome the disadvantages of conventional series compensation. The application of the TCSC brings about many benefits, some of which are [18,30,32,33]:

- It permits operation of transmission systems with high levels of series compensation.
- It improves the transient and dynamic stability performance of the system.
- Mitigation of potential damages caused by subsynchronous resonance (SSR), by smoothly damping the oscillations
- To regulate power flow in the vicinity of the compensated transmission line helping to prevent undesirable conditions such as the loop flows.
- To adjust the transfer impedances of different sections of the network to minimise unscheduled power flows.
- High-speed modulation of effective impedances in response to power system dynamics

Figure 3.2 shows two different configurations of series compensation using TCSC controllers [32,34].

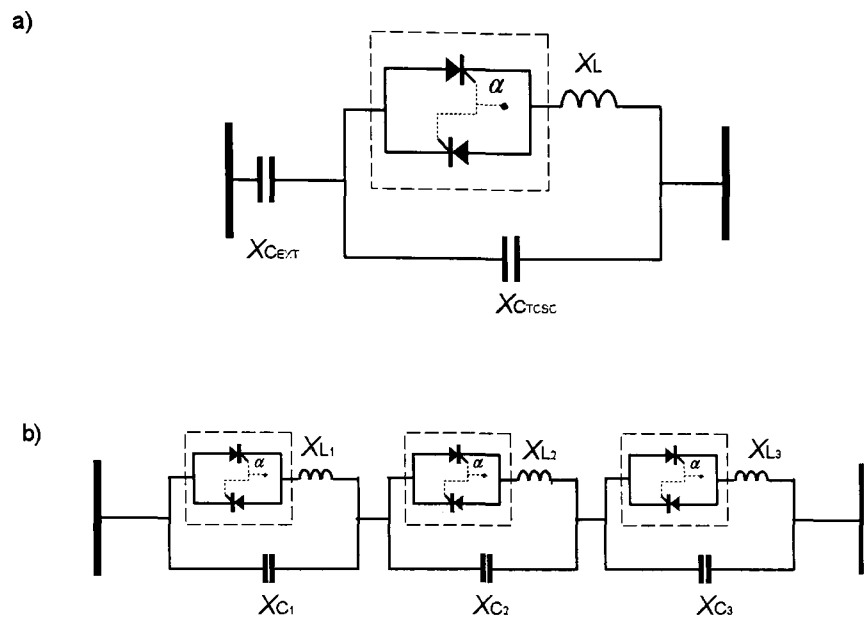


Figure 3.2. TCSC configurations for series compensation: a) single TCSC module with a series fixed capacitor; b) multiple TCSC modules

The thyristor module is the controllable element of the TCSC; triggered in the operating region where the capacitor voltage and current have opposite polarity, i.e. between 90° and 180° for the forward thyristor and between 270° and 360° for the reverse one. The reference for the triggering angle, termed α, is the positive going zero-crossing of the capacitor voltage. The basic circuit of a TCSC module consists of a series capacitor bank in parallel with a TCR, as shown in Figure 3.2a.

Once the thyristor is on, the current begins to flow through the inductor, as illustrated in Figure 3.3, in the opposite direction to the current flowing in the capacitor, creating a loop flow and provoking an immediate increase of compensation due to the increase of voltage across the capacitor [8].

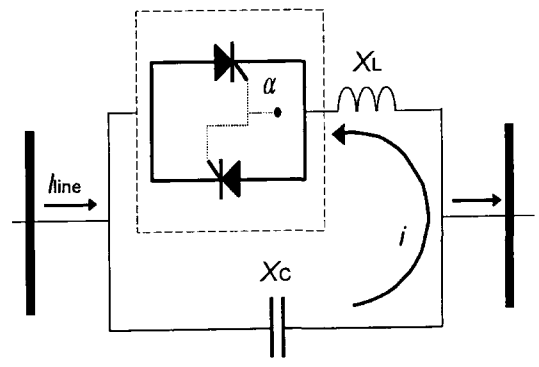
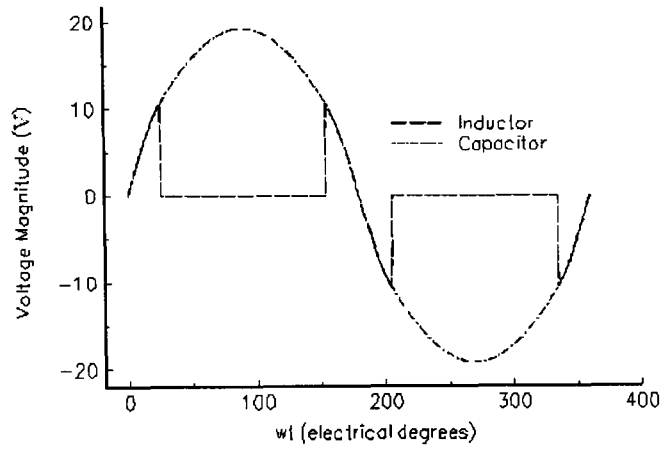


Figure 3.3. Current flow loop in TCSC

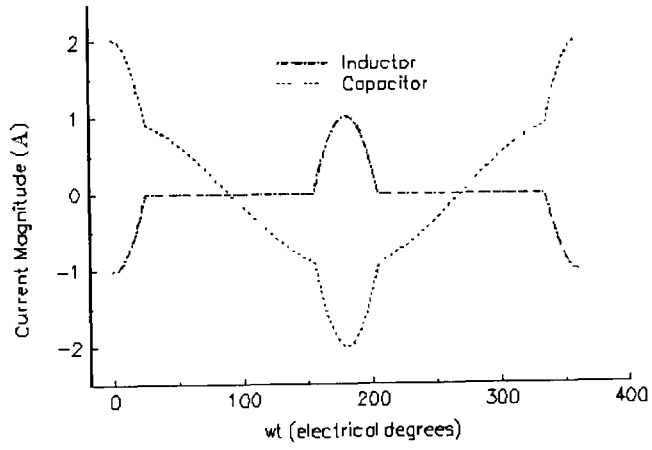
After firing, the thyristor conducts during an angular interval σ. The relation between the conduction angle σ and the triggering angle is given by equation 3.2 [34,35]

$$\sigma = 2(\pi - \alpha) \tag{3.2}$$

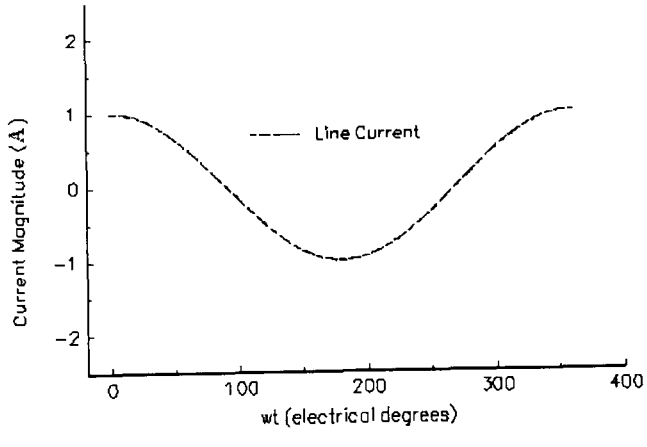
For steady state operation, the typical current and voltage profiles for the TCSC elements are shown in Figure 3.4. These waveforms correspond to values of inductance and capacitance of 6.8 mH and 177 μF, respectively [34,36]. These are the parameters of the Kayenta ASC scheme, which operates at fundamental frequency of 60 Hz.



a) Voltage waveforms in the TCSC inductor and capacitor



b) Current waveforms in the TCSC inductor and capacitor



c) Line current

Figure 3.4. TCSC steady state voltage and current waveforms at $\alpha = 155°$

3.4 TCSC MODULE OPERATING MODES

A TCSC module has three operating modes; thyristor blocked mode, thyristor-bypassed mode and vernier mode [35].

In the thyristor-blocked mode, the thyristor module does not receive triggering pulses, thus, zero conduction takes place in the inductor. Under this condition the TCSC is a capacitive reactance and the overall transmission line current flows only through the series capacitor. This operating mode is illustrated in Figure 3.5.

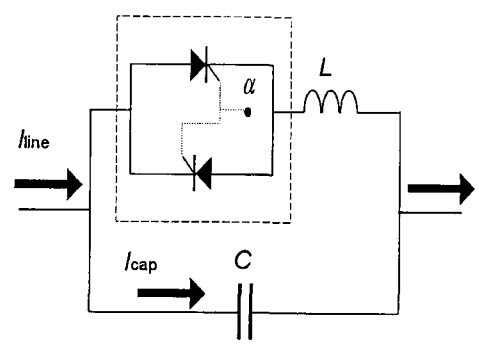


Figure 3.5. TCSC Thyristor blocked mode

When the thyristors are triggered at near 90° and 270° for the opposite thyristor, they are in near conduction, and the TCSC module is said to operate in the bypass mode. Figure 3.6 illustrates this mode.

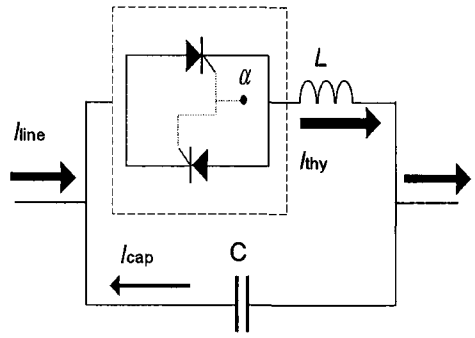


Figure 3.6. TCSC bypassed mode

In this case, the total transmission line current is the summation of the current flowing through the capacitor and thyristor paths, but most of the current flows through the inductive path. The TCSC impedance is determined by the value of the equivalent impedance of the parallel inductive and capacitive reactances, and usually results in small, net inductive impedance. In the vernier operating mode, the thyristor is triggered using phase control. This results in partial thyristor conduction. Depending on the triggering angle value the reactance of the TCSC changes in magnitude and polarity.

Thus, theoretically, two operating vernier region exists, inductive and capacitive. Figures 3.7a and Figure 3.7b illustrate the TCSC operating in the inductive region (high levels of conduction) and capacitive region (low levels of conduction), respectively [35]. In each case, the circulating current in the element produces a total equivalent impedance that surpasses the TCSC nominal impedance.

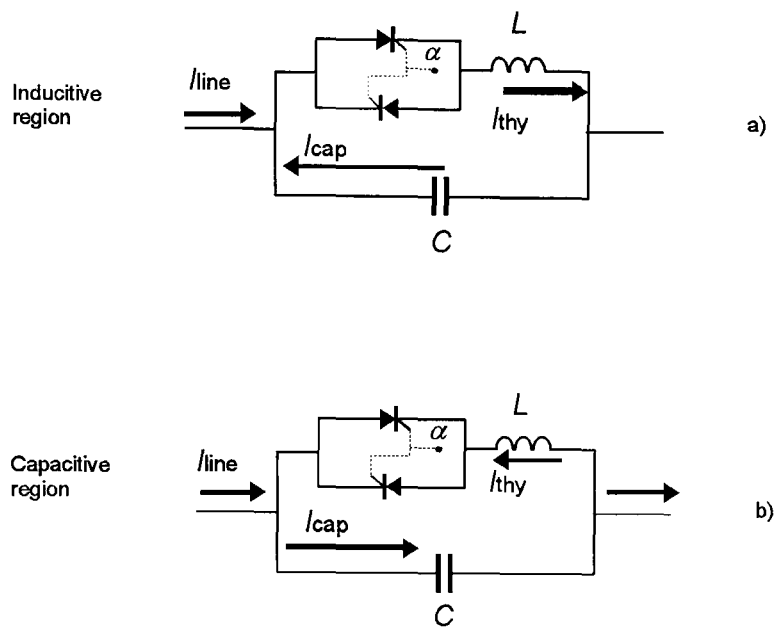


Figure 3.7. TCSC vernier mode: a) Inductive region; b) Capacitive region

The vernier control mode has an important impact on the TCSC currents and voltages. In this mode, the greater the triggering angle in the inductive region the greater the harmonic distortion in capacitor voltage, and smaller and more distorted the current flowing through the inductor. The voltage across the capacitor changes in polarity when the resonant point is crossed, this means that the direction of the current depends on the value of the triggering angle. Furthermore, the voltage magnitude increases near the resonant point.

3.5 TCSC FUNDAMENTAL IMPEDANCE

A general expression for the fundamental frequency TCSC impedance is given as [11,30,34,36]

$$X_{TCSC} = -X_C + (X_C + X_{LC})\left(\frac{2(\pi-\alpha)+\sin(2(\pi-\alpha))}{\pi}\right) - \frac{4X_{LC}\cos^2(\pi-\alpha)}{X_L}\left(\frac{k\tan(k(\pi-\alpha))-\tan(\pi-\alpha)}{\pi}\right) \quad (3.3)$$

where

$$X_{LC} = \frac{X_C X_L}{X_C - X_L} \tag{3.4}$$

$$k = \frac{\omega_o}{\omega} \tag{3.5}$$

$$X_C = 1/\omega C \tag{3.6}$$

$$X_L = \omega L \tag{3.7}$$

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.8}$$

Also, X_C is the reactance of the TCSC capacitor bank; X_L is the reactance of the TCSC inductor; α is the triggering angle measured from the voltage zero crossing point; ω is the fundamental angular frequency of the system, and ω_o is the natural resonance angular frequency of the LC circuit at α =90° (or thyristor bypassed).

In general, the poles of equation 3.3 given by [36]

$$\alpha = \pi - \frac{(2n-1)\pi\omega}{2\omega_O} \qquad n = 1,2,3..... \tag{3.9}$$

Equation 3.3 is derived using the equivalent circuit shown in Figure 3.8. Full derivation of equation 3.3 can be found in reference [34,37].

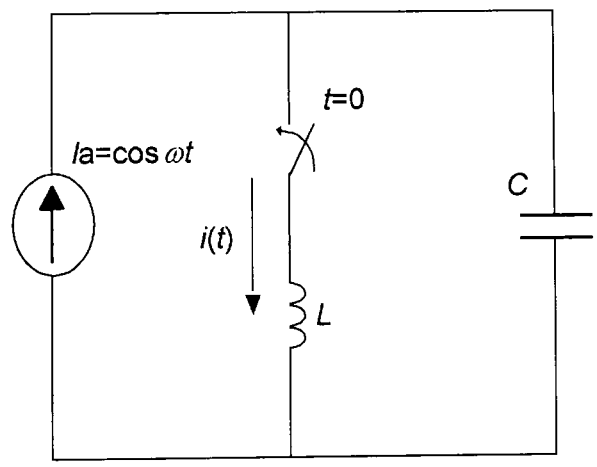


Figure 3.8. Equivalent circuit for the derivation of the TCSC fundamental impedance

The characteristic behaviour of the TCSC impedance at the fundamental frequency as a function of the triggering angle α is shown in Figure 3.9, which corresponds to the Kayenta scheme [34,36]. In this case the triggering angle is 143°.

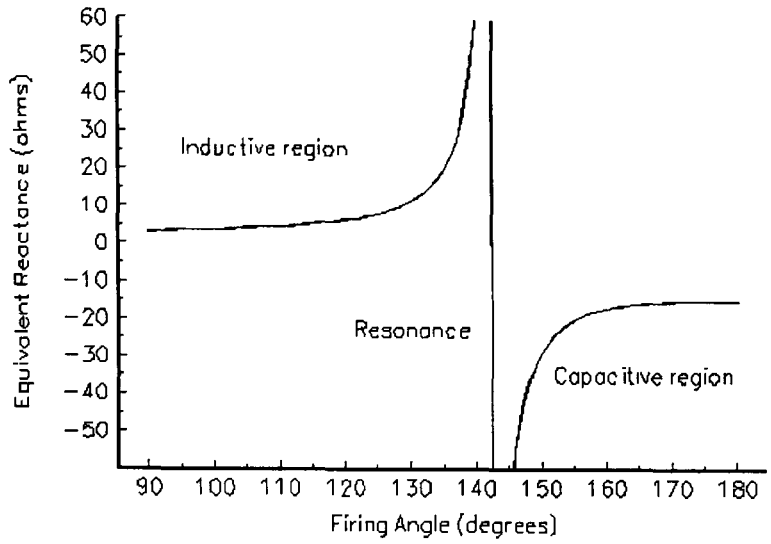


Figure 3.9. TCSC impedance versus triggering angle, exhibiting a resonant point at α=143°

When the thyristor is off the current flows only through the capacitor and it is equal to the transmission line current. When the thyristor is on, the current partially flows through the capacitor and the inductor, depending on α. The equations for capacitor and inductor currents and voltages are given by 3.10 to 3.15 [8].

Thyristor turned-off

$$V_{COFF} = \frac{I_M \sin\alpha}{\omega C}[1 - \sin(\omega t + \alpha) - \frac{I_M \cos\alpha}{\omega C}\cos(\omega t + \alpha)] + Vc' \tag{3.10}$$

$$I_C = I_M \sin\omega t \tag{3.11}$$

where:

V_{COFF} is the voltage across the capacitor

I_C is the current through the capacitor

I_M is the peak line current

V_C' is the voltage across the capacitor at time of thyristor commutation

Thyristor turned-on

$$I_{L_{ON}} = I_M \frac{\omega\omega_o^2 \sin\alpha}{\omega_o^2 - \omega^2}\left\{\frac{\sin\left[\omega_o t - \frac{\omega_o}{\omega}\left(\alpha - \frac{\pi}{2}\right)\right]}{\omega_o} - \frac{\cos(\omega t - \alpha)}{\omega}\right\}$$

$$-I_M \frac{\omega_o^2 \cos\alpha}{\omega_o^2 - \omega^2}\left\{\cos\left[\omega_o t - \frac{\omega_o}{\omega}\left(\alpha - \frac{\pi}{2}\right)\right] + \sin(\omega t - \alpha)\right\} \quad (3.12)$$

$$V_{C_{ON}} = I_M \frac{\omega_o^2 L \cos\alpha}{\omega_o^2 - \omega^2}\left\{\omega\cos(\omega t - \alpha) - \omega_o \sin\left[\omega_o t - \frac{\omega_o}{\omega}\left(\alpha - \frac{\pi}{2}\right)\right]\right\}$$

$$-I_M \frac{\omega_o^2 \omega L \sin\alpha}{\omega_o^2 - \omega^2}\left\{\sin(\omega t - \alpha) - \cos\left[\omega_o t - \frac{\omega_o}{\omega}\left(\alpha - \frac{\pi}{2}\right)\right]\right\}$$

$$+Vc''\cos\left[\omega_o - \frac{\omega_o}{\omega}\left(\alpha - \frac{\pi}{2}\right)\right] \quad (3.13)$$

$$I_{C_{ON}} = I_{L_{ON}} + I_M \sin\omega t \quad (3.14)$$

The theoretical harmonic current magnitudes generated by the TCSC are [34]:

$$I_n = \frac{2A}{\pi}\left[\frac{\sin\sigma(1-n)}{1-n} + \frac{\sin\sigma(1+n)}{1+n}\right]$$

$$-\frac{2\ A\cos\sigma}{\pi\cos\left(\frac{\omega_0}{\omega}\sigma\right)}\left[\frac{\sin\sigma\left(\frac{\omega_o}{\omega} - n\right)}{\frac{\omega_o}{\omega} - n} + \frac{\sin\sigma\left(\frac{\omega_o}{\omega} + n\right)}{\frac{\omega_o}{\omega} + n}\right] \quad n = 3,5,7,9.. \quad (3.15)$$

$$A = \frac{\omega_o^2}{\omega_o^2 - \omega^2} \quad (3.16)$$

The harmonic currents injected into the power transmission network are minimal. For moderate levels of line compensation the calculated theoretical line current distortion is 1 to 1.5% [34,39]. The TCR branch of the controller may generate relatively high odd harmonics, particularly 3rd harmonic. However, the low impedance of the TCSC capacitor relative to the equivalent impedance of the external system, at frequencies beyond the nominal, keeps most harmonics predominantly circulating inside the *LC* circuit [34]. The actual harmonic voltages and currents levels injected by the TCSC to power systems are still matters of research. An experimental investigation is proposed by the author in order to find the relation between the TCSC characteristics; the nominal line current; the SCL, the harmonic voltages and currents; and the triggering angle α.

3.6 TCSC RESONANCE MODES BEHAVIOURAL ANALYSIS

The poles for the TCSC fundamental impedance are given by equation 3.9. Multiple resonant points at the fundamental frequency may exist if the ratio between the nominal angular frequency of the system and the natural resonance frequency of the *LC* parallel circuit, $k=\omega/\omega_0$, is not adequately chosen. Figure 3.10 shows the TCSC fundamental impedance behaviour with multiple resonances, corresponding to using k=0.15.

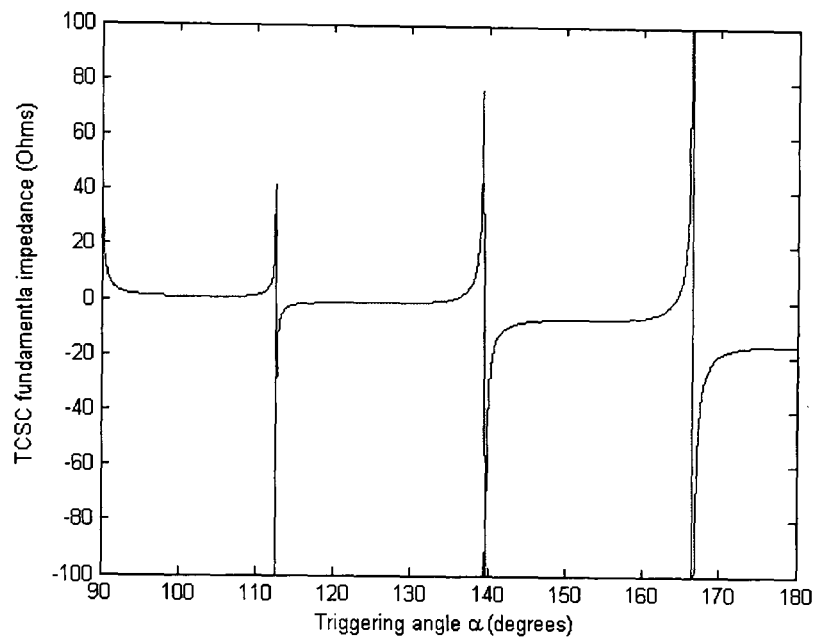


Figure 3.10. TCSC fundamental impedance with multiple resonances

The appropriate selection of ω/ω_0 ratio also implies an acceptable relation between the inductive and capacitive values of the *LC* circuit. Ratios between 0.41 and 0.36 have been used successfully in actual schemes [16-18]. However, little explanation exists on guiding design considerations and decisions taken to arrive at the final selection of the *LC* parameters. Table 3.4 and Table 3.5 present the TCSC parameters (ω/ω_0 ratios together with their respective *L* and *C* values) and the resonance angles, respectively, for both the Kayenta and Slatt TCSC schemes. Figure 3.11 shows their TCSC fundamental impedance.

Table 3.4. TCSC module parameter for the Kayenta and Slatt schemes [16-18]

Parameter	Kayenta scheme	Slatt scheme
$k=\omega/\omega_0$	0.41	0.36
L	2*3.4mH	1.99mH
C	177μF	470 μF

Table 3.5. TCSC resonance angles for the Kayenta and Slatt schemes

Resonance mode n	Kayenta scheme	Slatt scheme
1	142.77°	147.18°
2	68.32°	81.55°
3	353.87°	15.92°
4	279.43°	310.30°
5	204.98°	244.67°
6	130.53°	179.04°
7	56.08°	113.41°
8	341.63°	47.78°
9	267.18°	342.16°
10	192.74°	276.53°

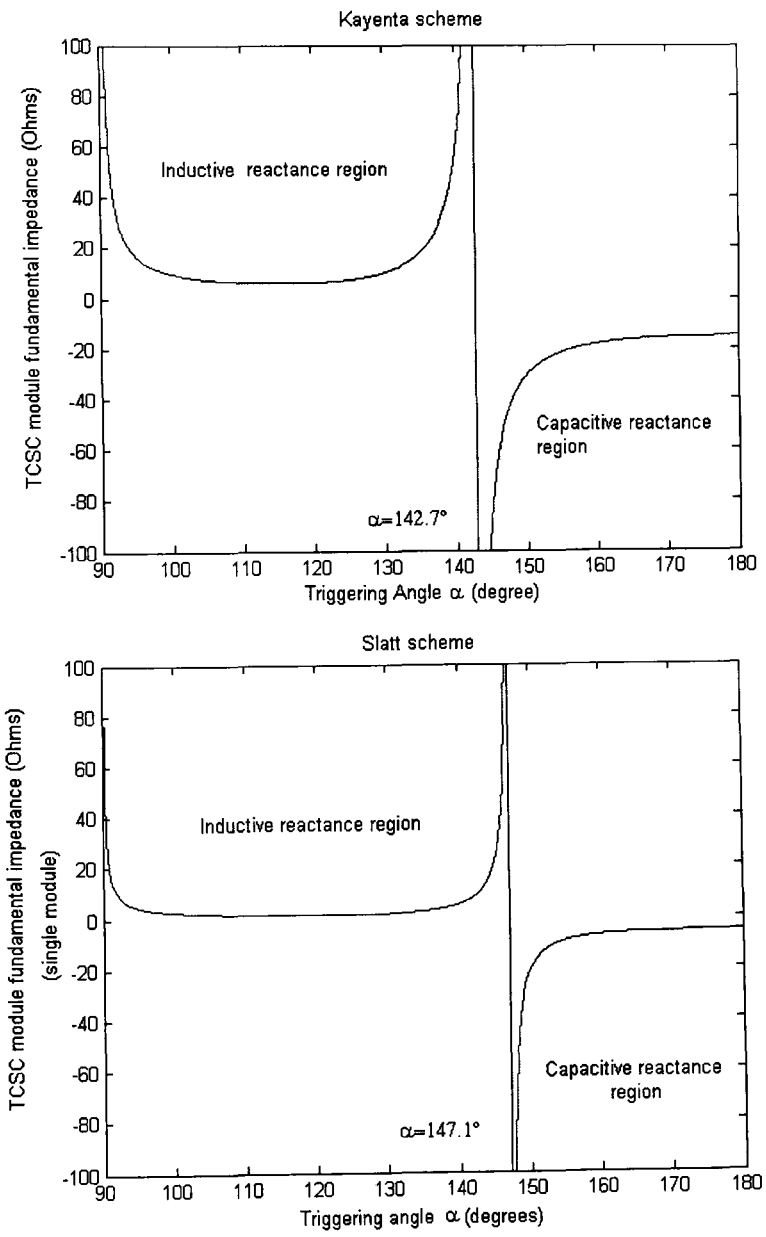


Figure 3.11. TCSC fundamental impedance. a) Kayenta scheme. B) Slatt scheme for a single-module

Equation 3.9 provides the n resonance angles where the TCSC will resonate, if appropriate conditions exist. In this research work, every one of the n resonance angles, at any fixed ω/ω_0 ratio, is defined as a TCSC resonance mode. The relation between n;

the TCSC resonance modes; and the corresponding resonance angles are determined by such equation. As a general rule, at any ω/ω_0 ratio the fundamental resonance mode, α_1, occurs at n=1; resonance mode 2, α_2, occurs at n=2; and so on. As can be figured out, a family of resonance mode angles is unique for every TCSC. A resonance mode is active if it is present in the TCSC fundamental impedance, when plotted as a function of the triggering angle. The remaining resonance modes are non-active or passive. The number of active resonance modes in a particular TCSC controller strongly depends upon the $k=\omega/\omega_0$ ratio. Figure 3.12 presents cases of active resonance modes for two different ratios.

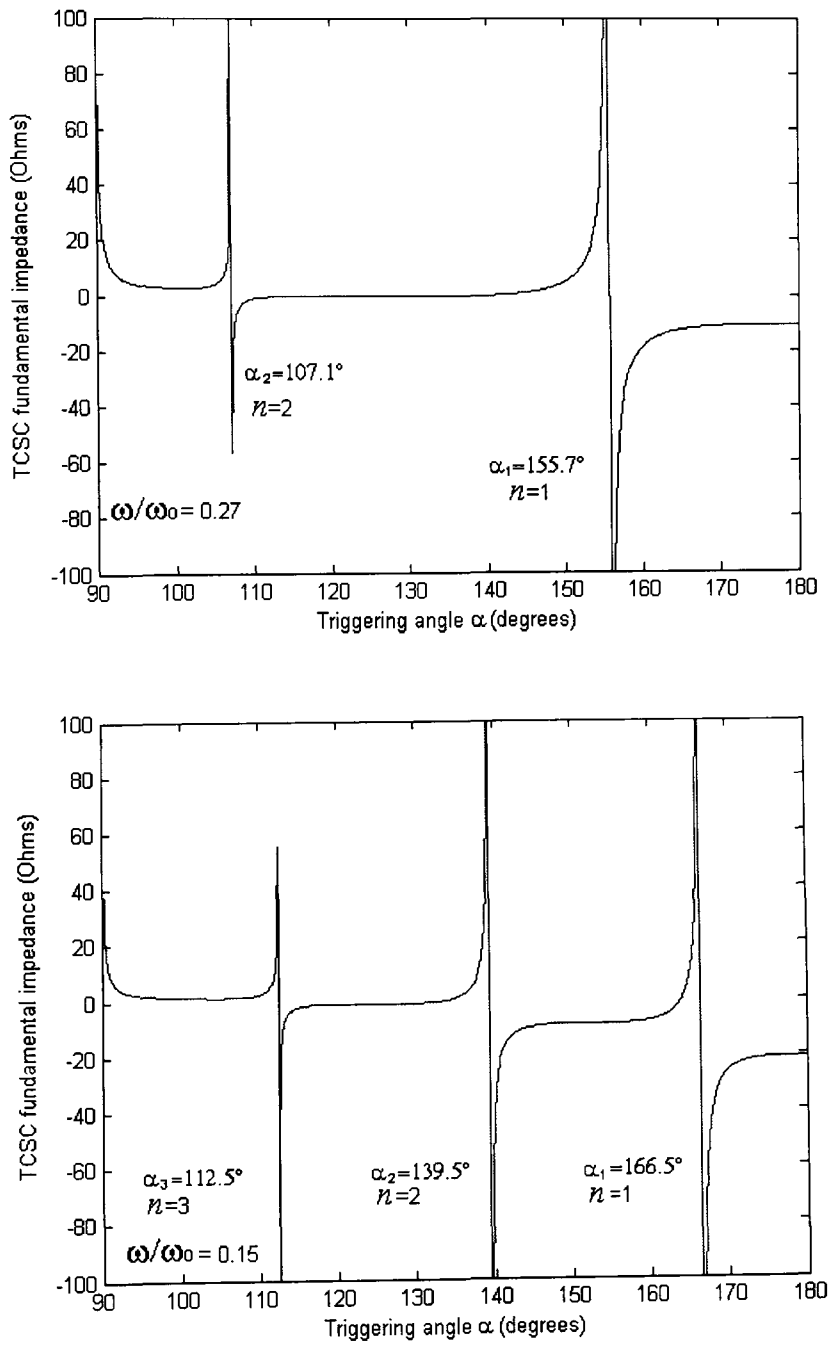


Figure 3.12. TCSC fundamental impedance with different resonance modes: a) double resonance mode; b) triple resonance mode

The TCSC fundamental impedance plots, always contain the resonance mode at α=90°, including those of the Kayenta and Slatt schemes shown in Figure 3.11. This singularity

is an all-time active resonance mode and it is called fundamental frequency intrinsic resonance mode, because this mode does not explicitly shows up when deriving the resonance modes using equation 3.9. This peculiarity can be understood by referring to the well known TCSC fundamental impedance equation 3.3.

It should be noted that the term $\tan(\pi- \alpha)$ becomes infinite at $\alpha=\pi/2$ for any $k=\omega/\omega_0$; confirming the existence of the intrinsic resonance mode, which must always be taken into consideration when designing and operating TCSC equipment.

$$\left(\frac{k\tan(k(\pi-\alpha))-\tan(\pi-\alpha)}{\pi}\right)\to\infty \qquad \forall\,\alpha=\pi/2 \tag{3.17}$$

Full-scale TCSC installations are normally operated in their capacitive region, at fundamental frequency. The TCSC inductive region is rarely used, except in theoretical studies. A case in point is the bang-bang control strategy used to damp oscillatory phenomena, which makes use of both regions, as is detailed in Chapter 5. In physical TCSCs, the use of such schemes, triggering the controller at 90° and 180°, is a risky strategy. Having said that, the controller may be operated with an apparent inductive reactance but only in pre-determined safe operating regions, where the apparent inductive reactance is low compared to the transmission system. For operation in the inductive region, the author suggests a region located in the vicinity of mid point between the intrinsic hidden resonance mode and resonance mode 1.

Further analysis of the resonance modes and the TCSC behaviour is carried out by calculating α for cases when the natural resonance angular frequency ω_0 of the equivalent LC circuit is an odd harmonic of the fundamental frequency ω. Table 3.6 shows the triggering angles for the active resonance mode for cases $\omega_0=\omega$ up to $\omega_0=11\,\omega$.

Table 3.6. TCSC resonance angles for different ω/ω_0 ratios at 50 Hz

TCSC resonance frequency	$k=\omega/\omega_0$	Fundamental resonance mode Angle
ω	1	90°
3ω	0.3333	150°
5ω	0.2	162°
7ω	0.1428	167.1°
9ω	0.1111	170°
11ω	0.0909	171.81°

The resonance angles in Table 3.6 mark the transition boundaries between the activation and de-activation of resonance modes in the TCSC fundamental impedance. As the ω/ω_0 ratio moves from 1 towards 0, the number of active resonance modes increases from 1 to infinite. The resonance modes activation is sequential, meaning that resonance mode m+1 is not active before resonance mode m. Table 3.7 presents the relation between the active resonance modes and the ω/ω_0 ratios from 1 to 1/11.

Table 3.7. Relation between the $k=\omega/\omega_0$ ratio and the active resonance modes

Range	Number of active resonance modes (including the intrinsic resonant mode)
$\omega/\omega_0 = 1$	1
$1 \geq \omega/\omega_0 \geq 1/3$	2
$1/3 \geq \omega/\omega_0 \geq 1/5$	3
$1/5 \geq \omega/\omega_0 \geq 1/7$	4
$1/7 \geq \omega/\omega_0 \geq 1/9$	5
$1/9 \geq \omega/\omega_0 \geq 1/11$	6

3.7 APPLICATION EXAMPLES OF TCSC

The many advantages of the TCSC technology over conventional series compensation solutions have made this technology the preferred option in today's electric utilities.

Several TCSCs have been installed in utilities around the world bringing about many benefits to real-life systems. After some years of continuous operation, this device has met the original expectations. The TCSC is under active investigation in research centres worldwide, including the University of Glasgow. Application areas relating to TCSC power systems studies have grown steadily over the last few years such as [35,37,38,40-53]:

- Steady and transient stability studies
- Control of power flow analysis
- Voltage collapse studies
- Improvement of transmission and distribution system operation
- Mitigation of subsynchronous resonance
- Protection relaying for FACTS compensated lines
- Damping of power oscillations
- Investigation on improvements of TCSC performance

The first full-scale TCSC transmission systems have been installed in the United States; these are the 230 kV Kayenta substation [30,35,36] and the 500 kV Slatt substation [47,52,54, 59-63]. Other TCSCs are now installed in Sweden [55] and Brazil [45,51,56]. The interest of electric power utilities in FACTS controllers is steadily increasing. Several TCSCs are planned to be installed soon such as the Yimin-Fengtun project of Northeast China Power System [57], and the New York State transmission system [58].

3.8 CONCLUSION

In this chapter, it has been shown that many resonant points at the fundamental frequency may exist if the $k=\omega/\omega_0$ ratio is not adequately chosen. The TCSC fundamental impedance tends asymptotically to $\pm\infty$ at each resonant point. Every possible resonance point has been identified as a TCSC operating mode and termed resonance mode for a better recognition of the phenomenon. It is important to mention that the number of active resonance modes varies as the ω/ω_0 ratio does.

The resonance modes can be active and passive. If active, the resonance mode is evident in the TCSC fundamental frequency impedance plots. The angle at which a resonance mode changes from inactive to active, and vice versa, has been named transition boundary. The resonance angles in Table 3.6 mark these transition boundaries. As the ω/ω_0 ratio moves from 1 towards 0, the number of active resonance modes increases from 1 to infinite. The resonance modes activation is sequential; meaning that resonance mode m+1 is not active before resonance mode m.

The TCSC fundamental impedance plots, always contain the resonance mode at α=90°. This singularity, which has not been presented in the open literature, is an all-time active resonance mode and it has been called fundamental frequency intrinsic resonance mode (intrinsic resonance mode for short).

The theoretical contributions of this Chapter are significant. These are intended to facilitate further understanding the TCSC behaviour and helps to in the controller design. Equation 3.1 clearly shows the need for careful design procedures for the TCSC controller. This implies the adequate selection of the angular range of α for each operating reactive region, in order to avoid multiple resonance points. An ill designed

TCSC has more than one resonant point. In this case the controller is unsuitable for realistic operation.

The TCSC is one of the key members of the FACTS controller conceptualised in the last decade. The effectiveness of this controller in improving the transmission system operation has been confirmed using both, digital simulations and real-life installations. The many successful solutions afforded by the TCSC pave the way for exploring new application opportunities for this power system controller, in areas such as voltage fluctuations, minimisation of the effects of power system sags, fault current limiting in power systems as well as wide range of distribution systems applications.

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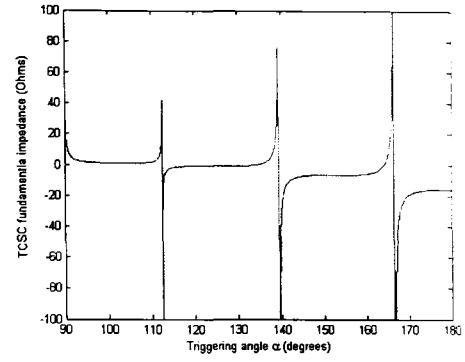
CHAPTER

4



DEVELOPMENT OF AN ADVANCED THREE-PHASE SCALED-DOWN TCSC PROTOTYPE

4.1 INTRODUCTION

The TCSC technology has introduced a number benefits to electric power systems. However, owing to the small number of schemes in operation around the world, there is limited operating experience with the technology. To understand it further and to characterise the TCSC under a range of network phenomena, a great deal of experimental research is still required.

So far, TNA-based and scaled-down prototypes have been used to carry out TCSC research, focusing in the following research areas:

- Steady state impedance control [1, 2]
- Steady state stability and dynamic characteristics [3]
- Smooth transition between inductive and capacitive operating regions [4,5]
- Transient behaviour of the controller [1]
- Damping of power system oscillations [2]
- Mitigation of subsynchronous resonance [6, 5,2,7]
- TCSC protection systems [6,2]
- Development of new control systems for the TCSC [6,2]
- The range of suitable TCSC capacitive reactance [8]

Besides facilitating the all-important academic inquisitiveness, experimentation with analogue prototypes is also a rich source of information for new industrial installations. Notwhithstanding the valuable experimental results available in the open literature, TCSC investigations in the following topics are currently lacking:

- Power flow transfer improvement under de-regulated environments
- Protective relaying for TCSC compensated transmission lines
- Waveform analysis under emergency conditions, e.g. internal and external faults
- Impact of TCSC on voltage collapse prevention
- Performance operation under harmonic, sub-harmonic and inter-harmonic polluted environments
- TCSC as a voltage fluctuation mitigation apparatus
- Effectiveness of TCSC-type controllers as fault current limiters
- Potential instabilities of the TCSC under transient conditions
- Fast switching PWM-TCSC-type configurations for distribution systems

4.2 REAL TIME EXPERIMENTATION WITH SCALED-DOWN TCSC PROTOTYPES: A REVIEW

The real-time hardware-in-the-loop experimentation using an advanced scaled-down TCSC prototype is a powerful tool for the investigation of TCSC characteristics and application benefits. Since all electrical quantities in the physical system model can be directly measured, scaled-down prototypes are used to investigate control schemes, new applications and related phenomena that are difficult to describe by mathematical models.

The main disadvantages of scaled-down prototypes and physical TNA-based models, as general research tools, lie on their comparatively high cost, less flexibility to change system parameters and long times involved in preparing the experiments.

TNA-based hardware system and single-phase prototypes are valuable physical tools to carry out research on TCSCs performance [2,4-6, 8-12]. However, as a common rule, TNA-based TCSCs do not dynamically interact with external computer-based controllers for hardware-in-the-loop testing. Furthermore, they use bulky, and very costly hardware.

Nevertheless, a number of experiments have been reported using single-phase prototypes on SSR mitigation, ANN-based control testing and TCSC operation on UHV transmission systems. These evidence the limitations of single-phase prototypes as advanced research tool, especially when the complexity of the electrical system or the abnormal operating conditions to simulate increase.

Three-phase scaled-down TCSC prototypes or physical models are scarcely reported in open literature. Nyati et al [13] developed a highly specialised hardware model to understand the particularities of the full-scale TCSC installed at the Slatt substation and its neighbouring system, focusing primarily on the subsynchronous resonance phenomena. Important results are reported on SSR mitigation strategies and the use of TCSC to neutralise to SSR. However, this hardware tool is inflexible since it represents only a single electrical system, the interaction user-experiment is low, and interfacing with an external computing platform for hardware-in-the-loop control purposes is not considered. This TCSC physical model is not a stand-alone equipment and it is not available for academic research.

On the other hand, Matsuki et al [14] researched the LC loop current dynamic behaviour on a three-phase 0.8 kV TCSC prototype, corroborating the response of a previously derived mathematical expression which describes the phenomena. Other authors have incorporated a resistor in series with the TCR and have evaluated the overall TCSC impedance for various L-R combinations. The reported results yield useful insights into the TCSC impedance behaviour at various natural resonance frequencies. However, the prototype structure is inflexible and only suitable to study TCSC steady state operation under open loop static triggering control, with no external dynamic control interaction permitted.

Another prototype is presented by Yin et al [3,15] at Tsinghua University, Beijing. In this case the research team reports on the steady state TCSC behaviour using open loop and PI close loop control schemes. The study presents comparative experimental analysis demonstrating the advantages of the PI-closed loop over the open loop as well as the loss of control of the three-phase TCSC when short-circuit fault to ground takes place in the external circuit. However, the control scheme in the three-phase TCSC does not permit independent single-phase operation. Moreover, the TCSC triggering scheme is neither dynamic nor interactive relaying upon a fixed PI regulation law or phase-

angle lock up tables. This scaled-down prototype has proven its capability as a FACTS teaching resource in the laboratory.

Very significant research results are available in the open literature but, as a general rule, the information does not include TCSC design procedures.

This chapter presents the design and construction of an advanced three-phase scaled-down TCSC prototype including its purpose-built operating support system. This research project focuses on the experimental evaluation of the TCSC as a voltage fluctuation mitigation equipment, using the newly developed scaled-down controller, which offers several advantages over the other three phase scaled-down prototypes reported in open literature as:

- Dynamic capacitive impedance modulation over a broad range of frequencies
- Wide capacitive reactance region
- Selectable amount of fixed and controllable series capacitive compensation
- Flexibility to operate on a single-phase or a three-phase basis
- Wide selection of line currents and voltages up to 5A, 220V per phase, respectively
- Flexible structure configuration rearrangement to simulate a wide variety of different small electrical systems
- Independent phase operation, and flexible monitoring and interfacing modules for interactive real-time hardware-in-the-loop experimentation
- Selectable static or dynamic control for angle triggering

4.3 TCSC MODULE DESIGN

The overall design of the TCSC module can be broadly divided into two main parts: the TCSC power hardware, and the operating support system. A fixed capacitor bank, the *LC* circuit, and the thyristor module constitute the power hardware. The support system, in turn, consists of two blocks: the signal interface and the triggering loop subsystems. The design of the TCSC power hardware and the operation support system are detailed in Sections 4.4.1 and 4.4.2, respectively.

4.3.1 TCSC Prototype: General Design Consideration

The design of the three-phase TCSC prototype is influenced by a number of technical requirements, which are inherent to the TCSC application, bearing in mind normal and abnormal operation, and the parameters and restrictions imposed by the external electrical network. Other important considerations impacting on the TCSC design procedure are related to the type of abnormal electrical phenomena generated during the testing of the TCSC, the characteristics of the power electronic devices used and those of the testing-bed environment. The characteristics required for the scaled-down TCSC prototype module are as follows:

1 Independent three-phase operation
2 Two operating regions: capacitive and inductive
3 Closed hardware-in-the-loop operation
4 Fast dynamic operation in vernier mode
5 Capability to interface with a real-time computing platform
6 Internal protection against high currents circulating in the LC loop
7 Compliance with electrical safety regulations
8 Utilisation of widely available, cost-effective devices

The prototype is intended for extensive use in the laboratory and this introduces a number of additional restrictions on the design, such as the maximum steady state voltage and current that can be safely handled in this environment. The main restrictions for the design of the scaled-down TCSC prototype are:

- Maximum load current magnitude: 5 A per phase
- Maximum input voltage magnitude: 220 V per phase
- Base fundamental frequency: 50 Hz
- Three-phase maximum power: 3.3 kVA

4.4 TCSC DESIGN BASED ON CHARACTERISTIC RESONANCE MODES

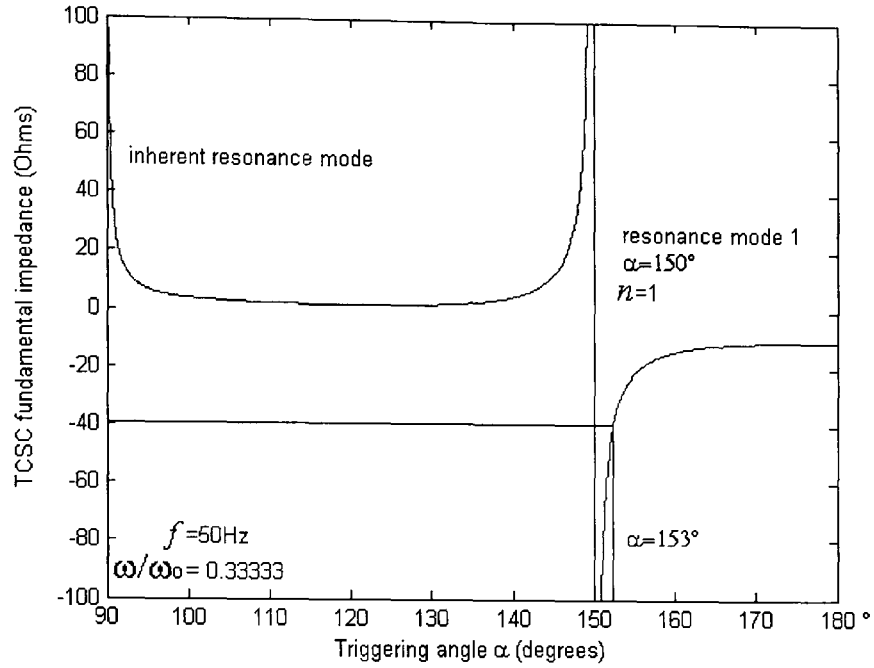
A TCSC design for a single resonance mode at 90° is not realistic, as the impedance is extremely large due the continuous resonance of the TCSC circuit. Notice that no inductive region would exist in this case.

For ratios ω/ω_0 higher than 0.3333, two or more other active resonance modes exists, in addition to the intrinsic resonance mode, which leads to an impractical design because the operating regions where the TCSC is smoothly controlled becomes increasingly narrow, making it difficult to control the equipment safely. It follows that, ω/ω_0 must be chosen in the range $1 \geq \omega/\omega_0 \geq 0.3333$ for well a designed TCSC, in order to avoid unnecessary activation of more than one resonance mode.

Once the TCSC design has been completed, the ω/ω_0 ratio is normally taken to remain invariable. However, the natural resonance angular frequency, ω_0, might vary due to parameters varying with the ageing of TCSC inductor and capacitor values. Furthermore, the network fundamental frequency may also suffer slight variations as a result of electrical phenomena, such as subsynchronous resonance, transient power oscillations, harmonics and inter-harmonic; all of these causing ω/ω_0 to vary.

Under these circumstances, if ω/ω_0 decreases lower than 0.3333, more than one active resonances will commence to apper and the TCSC tends to resonate at triggering angles different than those initially defined at design stage. The reason behind is because the resonance modes are "shifted" from initial designed operating regions due to unexpected variation of the ω/ω_0 ratio. A critical situation occurs in the vicinity of ω/ω_0 = 0.33333 as the fundamental resonance mode is located just at the transition boundary. In this case, any small variation in ω/ω_0 has an immediate effect in the number of active modes.

Figure 4.1 shows the shift and activation of resonance modes when the fundamental frequency varies ±2 Hz around its nominal value.



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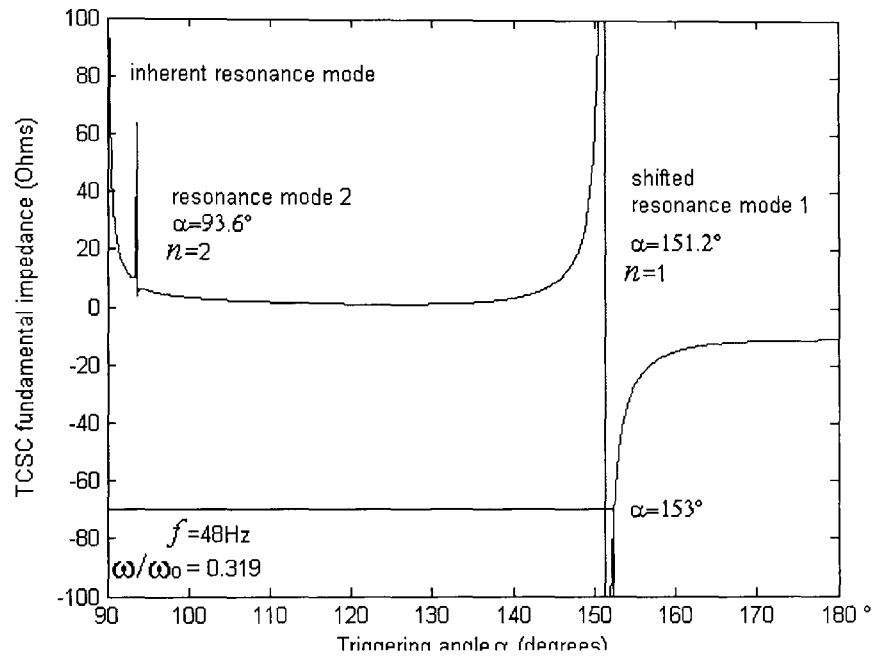

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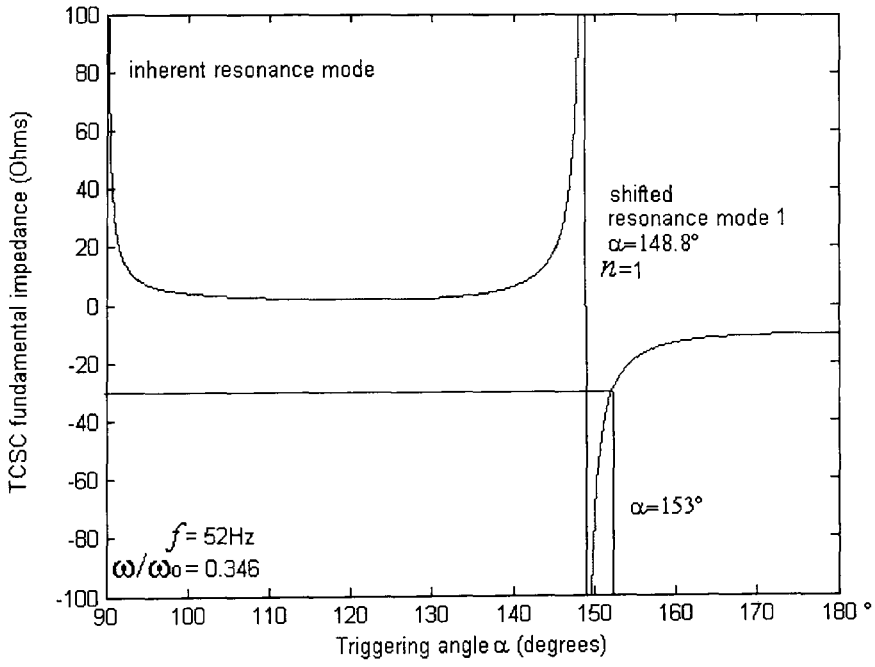


c)

Figure 4.1. Deviations of TCSC fundamental impedance resonance modes due to variations of the ω/ω_0 ratio: a) f=50Hz; b) f=48Hz; c) f=52Hz

The design of a TCSC based on the fundamental resonance mode in the vicinity of 150° is not desirable, mainly because of the large uncontrollable TCSC impedance variations that would take place if the frequency of the system deviates from nominal due to abnormal network conditions. To ensure a satisfactory TCSC design, a margin angle between the fundamental resonance mode and the transition boundary is required. It should be noticed that the very-well known equation for the fundamental TCSC impedance is neither intended for SSR studies nor for assessing the transitory behaviour of the TCSC impedance [19]. However, it provides valuable information on TCSC impedance variations for frequency excursions around the nominal network frequency, as it has been illustrated by the cases presented in Figure 4.1.

As has been mentioned in Chapter 3, in theory, the number of different resonance modes associated with a TCSC is infinite. So, while searching for an adequate ω/ω_0 ratio, considerable effort goes into reducing the universe of possible resonance modes to a realistic number. A technique proposed in this research work consists in equating and synchronising a higher resonance mode with a lower resonance mode. This is done in such a way that a number-limited, circularly repetitive, resonance modes is achieved. By ways of example, the equating and synchronising procedure for modes 1 and 4 is as follows:

$$\alpha_1 = \pi - \frac{\pi\omega}{2\omega_o};\ n=1$$

$$\alpha_4 = \pi - \frac{7\pi\omega}{2\omega_o};\ n=4$$

Equating modes:

$$\frac{7\pi\omega}{2\omega_o} - \frac{\pi\omega}{2\omega_o} = 0$$

Synchronising at 2π

$$\frac{7\pi\omega}{2\omega_o} - \frac{\pi\omega}{2\omega_o} = 2\pi$$

Solving to ω/ω_0

$$\frac{\omega}{\omega_o} = \frac{2}{3} \qquad (4.1)$$

The resonance modes using ω/ω_0 =0.6666 are limited from infinite to four, including the intrinsic resonance mode. Table 4.1 presents the synchronised resonance modes from n=1 to n=8 for $\omega/\omega_0 = 2/3$.

Table 4.1 Resonance modes n=1 to n= 8 at ω/ω_0= 2/3

n	Resonance mode	Angle	Angular difference between consecutive resonance modes $\Delta\alpha$
	Intrinsic	90°	-
1	α_1	120°	120°
2	α_2	240°	120°
3	α_3	360°	120°
4	α_4	120°	120°
5	α_5	240°	120°
6	α_6	360°	120°
7	α_7	120°	120°
8	α_8	240°	120°

Table 4.2 presents the ω/ω_0 ratios for the case when 4 to 7 resonance modes are repetitive.

Table 4.2. Resonance modes for various ω/ω_0 ratios

ω/ω_0	Resonance modes	Angular difference between consecutive resonance modes $\Delta\alpha$
$\frac{2}{4}$	$\alpha_1 = 135^\circ, \alpha_2 = 45^\circ, \alpha_3 = 315^\circ$ $\alpha_4 = 225^\circ$ + intrinsic hidden resonance mode	90°
$\frac{2}{5}$	$\alpha_1 = 144^\circ, \alpha_2 = 72^\circ, \alpha_3 = 0^\circ$ $\alpha_4 = 288^\circ, \alpha_5 = 214^\circ$ + intrinsic hidden resonance mode	72°
$\frac{2}{6}$	$\alpha_1 = 150^\circ, \alpha_2 = 90^\circ, \alpha_3 = 30^\circ$ $\alpha_4 = 330^\circ, \alpha_5 = 270^\circ, \alpha_6 = 210^\circ$	60°
$\frac{2}{7}$	$\alpha_1 = 154.28^\circ, \alpha_2 = 102.85^\circ, \alpha_3 = 51.42^\circ$ $\alpha_4 = 0^\circ, \alpha_5 = 308.57^\circ, \alpha_6 = 257.14^\circ$ $\alpha_7 = 205.71^\circ$ + intrinsic hidden resonance mode	51.42°
$\frac{2}{8}$	$\alpha_1 = 157.5^\circ, \alpha_2 = 112.5^\circ, \alpha_3 = 67.5^\circ$ $\alpha_1 = 22.5^\circ, \alpha_2 = 335.5^\circ, \alpha_3 = 292.5^\circ$ $\alpha_7 = 247.5^\circ, \alpha_8 = 202.5^\circ$ + intrinsic hidden resonance mode	45°

The TCSC capacitive and inductive values are determined to correspond with the ω/ω_0 ratios selected, and are finally derived using equation 4.2 as follow:

$$\omega_o = \frac{1}{\sqrt{L_T C_T}} \tag{4.2}$$

where ω_0 = natural resonance frequency

L_T = Inductance value of the LC circuit

C_T = Capacitive value of the LC circuit

Substituting ω_0 by ω/k in 4.2 and solving for L_T

$$L_T = \frac{k^2}{\omega^2 C_T} \tag{4.3}$$

$$L_{T50} = 1.0132e^{-5}\frac{k^2}{C_{T50}} \qquad \text{fundamental frequency = 50hz} \tag{4.4}$$

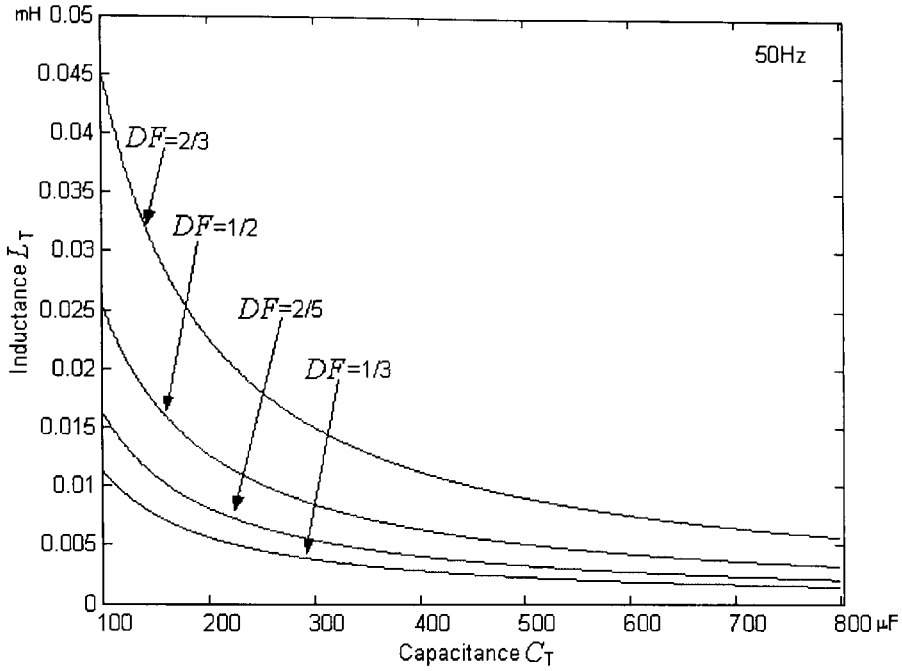
$$L_{T60} = 7.0358e^{-6}\frac{k^2}{C_{T60}} \qquad \text{fundamental frequency = 60hz} \tag{4.5}$$

Selection of the TCSC passive elements is facilitated if k factors lower than k=0.6666 are used, as can be appreciated from Table 4.2. The k^2/ω^2 factor is termed design factor DF. Table 4.3 presents four cases for the k factor at 50 and 60 Hz. Figure 4.2 shows the L_T versus C_T relationship.

$$L_T = \frac{DF}{C_T} \tag{4.6}$$

Table 4.3. Design factors at fundamental frequency

ω/ω_0	Fundamental resonance mode angle	Design Factor DF		$\Delta\alpha$
		50Hz	60Hz	
2/3	120°	4.503×10^{-6}	3.126×10^{-6}	120°
2/4	135°	2.533×10^{-6}	1.728×10^{-6}	90°
2/5	144°	1.621×10^{-6}	1.125×10^{-6}	72°
2/6	150°	1.125×10^{-6}	7.816×10^{-7}	60°



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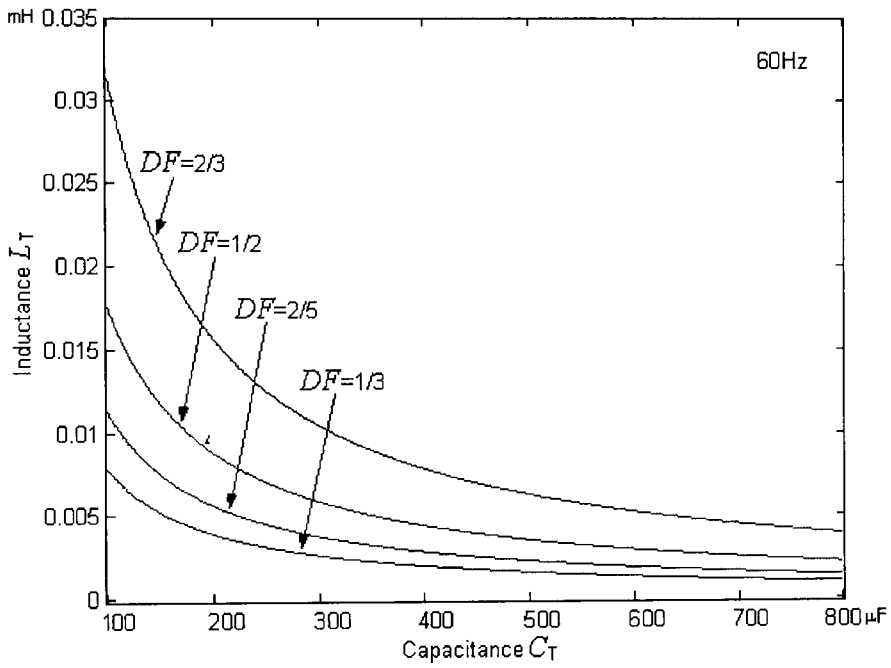


b)

Figure 4.2. Inductance and capacitance relationship for the TCSC *LC* circuit at different design factors: a) 50Hz case; b) 60 Hz case.

4.4.1 Selection of the fundamental resonance mode and calculation of the inductor and capacitor for the *LC* circuit.

The adequate selection of the capacitive and inductive operating regions plays a key role in determining the overall TCSC performance, impacting also on its effectiveness to carry out the intended application, e.g. voltage fluctuation mitigation, damping of power oscillations, SSR mitigation amd power flow control.

The TCSC passive elements are selected in full agreement with the selected active resonance mode. At ω/ω_0 >0.666, the capacitive operating region is wider than the

inductive operating region. Wide TCSC capacitive regions enable ample modulations around the nominal operating frequency or the implementation of fast transitions between maximum and minimum capacitive compensating levels. In such a case, changes in apparent capacitance with respect to the triggering angle is very smooth. Also, the possibility of activating a resonance mode is strongly minimised, as the margin angle becomes larger (35° for ω/ω_0=0.666). However, wider capacitive regions require greater conduction angles for the thyristor, and so, larger currents circulate in the *LC* circuit. This implies larger ratings and added stress to the thyristor modules, the capacitor and inductor in the TCSC prototype.

At ω/ω_0<0.4, the capacitive operating region narrows, with its respective fundamental resonance mode close to the transition boundary which can be eventually trespassed, activating an additional resonance mode as a consequence of an abnormal network condition, even if α remains constant. A narrow capacitive operating region intrinsically implies that the TCSC fundamental impedance is highly sensitive to very small changes in the α triggering angle. On the other hand, a wide inductive operating region is advantageous, in the sense that it allows an easier operation in the inductive-capacitive inter-regions, triggering the TCSC at angles where the apparent inductance of the TCSC is better controlled.

Taking due account of the factors previously discussed, and bearing in mind the TCSC application in voltage fluctuation mitigation, as well as the real-time hardware-in-the-loop testing environment requirements and constrains, a ratio of ω/ω_0 = 0.5 is selected in the design of the advanced scaled-down TCSC prototype. Additionally, a high inductance, L_T=10mH, is selected in order to reduce harmonics [20]. The capacitance C_T is derived using equation 4.6 and Figure 4.2, employing the following design factor *DF* and ω/ω_0 ratio:

$$L_T = \frac{DF}{C_T}$$

$$DF = 2.533e^{-6} \qquad ;\frac{\omega}{\omega_o} = \frac{1}{2}$$

$$L_T = 10\text{mH}$$

Hence,

$$C_T = 253.3\mu\text{F}$$

4.5 CONSTRUCTION OF THE ADVANCED SCALED-DOWN TCSC PROTOTYPE

4.5.1 Thyristor Modules, Capacitor Banks and Inductor ratings

The thyristor module is a major component of the TCSC. In full-scale TCSCs the cost of this component is quite high because of the large amount of power that it would need to handle. The maximum line current and the maximum voltage across the capacitor are the two main parameters to bear in mind when selecting the thyristors. The former relates to the load current, whereas a repetitive reverse voltage for the thyristors establishes the latter.

The current rating of the TCSC capacitor bank can be determined using similar principles to those used in actual capacitor bank installations, which are [21]:

I_{rated} = Maximum continuous line current at fundamental frequency

I_{temp} = Temporary line current (typically $1.35I_{rated}$)

I_{tran} = Maximum line current for which the thyristor is not inhibited by protective considerations (typically $2I_{rated}$).

I_{peak} = Maximum line current which the TCSC might experience during a major power system disturbance. I_{peak} is at least as large as I_{tran} but currents higher than I_{tran} will be subjected to protective overrides in the thyristor control.

Additionally, the voltage rating for the capacitor bank and thyristor can be established in terms of steady state and transient performance requirements:

V_{rated} = Maximum continuous voltage. This must be at least equal to the value given by the relationship $Xc \times I_{rated}$. To allow some continuous modulation in vernier mode, a greater margin should be selected. In the Slatt project a 15% margin has been used [22].

V_{temp} = Maximum temporary voltage. This should be at least equal to the value given by the relationship $Xc \times I_{temp}$.

V_{tran} = Maximum voltage required during transient swings. This should at least be equal to the value given by the relationship $Xc \times I_{tran}$. If the main TCSC application purpose is power transient stabilisation then a higher margin should be used.

Taking account of the requirements imposed by the real-time environment and the above guidelines, the voltage and current ratings for the thyristor module are:

I_{rated} = 5 A

I_{temp} = 1.35×5 A = 6.75 A

I_{tran} = 2×5A = 10 A

I_{peak} = 2.2×5A = 11 A

V_{rated} = $12.58\ \Omega \times 5\text{A} \times 1.15$ = 72.3 V

V_{temp} = $12.58\ \Omega \times 6.75$ A = 84.5 V

V_{tran} = $84.5\text{ V} \times 1.1$ = 92.95 V

The TCSC capacitor bank was constructed by connecting in parallel a block of four 50μF ±10%-250 V capacitors and one 3μF ±10% -250 V capacitor per phase. This configuration fulfils the rating requirement. The power inductors for each phase have been robustly constructed in the laboratory, each rated at 15A for continuous operation.

When the thyristors are blocked, the voltage at its terminals is equal to the capacitor voltage. Thus, each thyristor must have a repetitive reverse voltage above V_{tran}. The thyristor module SKKT 27B08 from Semikron fulfils well such a rating requirement.

A three-phase power interrupter and two additional parallel-connected 50 μF capacitor banks, external to TCSC prototype main module, are inserted in each phase, providing the equipment with selectable series compensation.

4.5.2 Operation Support System.

The operational flexibility and functionality of the scaled-down TCSC prototype resides in the operation support system (OSS), which comprises electronic hardware modules expressly developed to provide the controller prototype with suitable reference waveforms (magnitude, frequency and phase) for the precise triggering angle of each thyristor. The OSS input can be either the TCSC capacitor voltage or the line current of

the system under test. The hardware tools included are: the reference generation module, the sensors interface module, the automatic magnitude stabiliser module, the signal conditioning and step-up voltage module, and the phase-angle triggering control module.

The OSS is a three-phase system, with each phase capable of operating independently from the other two. Figure 4.3 presents the per phase schematic block diagram for the OSS.

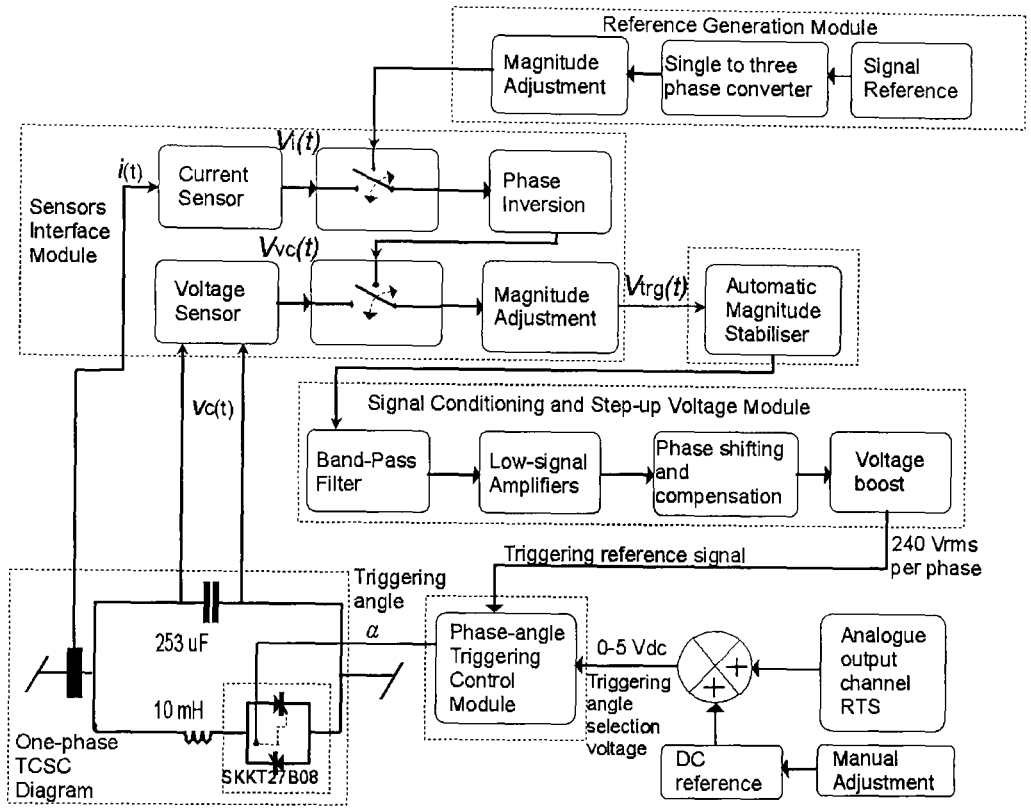


Figure 4.3. Operating Support System. Single-phase schematic block diagram

4.5.2.1 Reference Generation Module

The reference generation module subsystem provides balanced three-phase sinusoidal waveforms used as reference for open loop operation of the TCSC prototype. This reference serves the purpose of calibrating and verifying the voltage and current sensors operation, to check the correct operation of OSS internal modules, and to test other TCSC prototype features such as its off-line line modulation capability. The reference generation module comprises three blocks: a) initial one-phase signal reference; 2) single-to-three phase small-signal converter; and 3) magnitude adjustment.

4.5.2.2 Sensors Interface Module

The capacitor voltage and the line current are used as references to trigger the TCSC thyristors. The Sensors Interface Module (SIM) continuouslly monitors the waveforms,

conditioning the small-signals just sensed, and feeds the selected output to the Automatic Magnitude Stabiliser (AMS) for further processing. The operation of the SIM contains two blocks; the current processing block and the voltage processing block. Their structure share a similar design philosophy: a sensing stage, an amplitude-conditioning stage and a dc power supply. The current processing block also incorporates a phase inversion stage to synchronise the current line zero-crossing points, providing the correct phase reference to trigger the TCSC.

4.5.2.3 Automatic Magnitude Stabiliser Module

In order to minimise spurious triggerings, the magnitude, frequency, and phase of the reference waveform used to trigger the TCSC must be kept constant under a large range of changing steady-state operating conditions. The Automatic Magnitude Stabiliser (AMS) is designed to keep the output small-signal voltage within pre-fixed magnitude limits even though the input signal is varying, providing the signal conditioning and step-up voltage module with a reliable internal long-term steady state reference. This capability enhances the overall dynamic performance of the TCSC prototype.

4.5.2.4 Signal Conditioning and Step-Up Voltage Module

The signal conditioning and step-up voltage module (SUVM) has three main functions: filtering and low signal amplification, phase shifting and voltage output step-up. The filtering block is a band-pass Butterworth function centred at 50Hz, which limits the frequency spectrum of the input signal and adjusting its amplitude at the same time. The zero-crossing points of the ac signal feeding the phase-angle triggering control module is synchronised with its respective input reference, the TCSC capacitor voltage or the line current. If synchronisation is not properly achieved, a phase difference will occur provoking a non-controlled triggering angle error. The phase shifting block provides such a function. At the final stage, the small-signal voltage is boosted up to 240 V at 10 VA per phase, to feed the phase-angle triggering control module.

4.5.2.5 Phase-Angle Triggering Control Module

The nucleus of the Phase Angle Triggering Control Module (PATCM) are three SKPC200-240 modules from Semikron. Each module provides the gate triggering signal impulses, at the required voltage level, necessary to turn the one-phase thyristor

pair on at the angle specified by an external dc reference that acts as a phase-angle control signal. In addition to the dc reference the PATCM includes an ac input for the following purposes: to supply power to the internal circuitry and to provide the reference zero-crossing point for the triggering angle α. The relationship between the dc reference and the actual triggering angle is linear but the relating factor strongly depends on the voltage rms value fed at ac input. For this case, a 240 V regulated voltage signal is provided by the output of the SUVM. The protection snubber circuit for each thyristor is already included in the SKPC200-240 triggering module model.

4.6 ADVANCED SCALED-DOWN TCSC PROTOTYPE: FINAL IMPLEMENTATION

The final characteristics, established for the newly developed scaled-down TCSC prototype in sections 4.3 to 4.5, are summarised in Table 4.4. The significance of each parameter has been detailed in such sections.

Table 4.4. Final characteristics for the advanced scaled-down TCSC prototype

General Features	
Active resonance mode angle (n=1)	135°
Natural resonance angular frequency ω_0	628.31 rad/s
Capacitive reactance (thyristor blocked)	12.58Ω
Angle margin to the closest pasive resonance mode	15°
Inductance of the reactor L_T per phase	10mH
Capacitance of the capacitor bank C_T per phase	253μF
Capability for SSR mitigation (operating in capacitive region)	Yes
Capability for fast modulation of power	Yes
Capability for damping of power oscillation (only capacitive and inductive-capacitive regions)	Yes
Three-phase operation	Yes
Capability of independent operation per phase	Yes
Capacitive reactance compensation range	12.53Ω to 90 Ω
Electrical Operating Characteristics	
Maximum nominal line current at fundamental frequency per phase	5 A
Maximum nominal voltage current at fundamental frequency phase to earth	220V
Power safety margin per phase	100 VA
Maximum absolute apparent power	3.3kVA

The schematic diagram of the overall TCSC design is illustrated in Figure 4.4, which also includes two additional sections, the testing environment and the TCSC control triggering signal. The TCSC characteristics and each OSS block has been previously detailed in section 4.3. The TCSC control triggering signal and testing environment are detailed in Chapter 5 and Chapter 6, respectively.

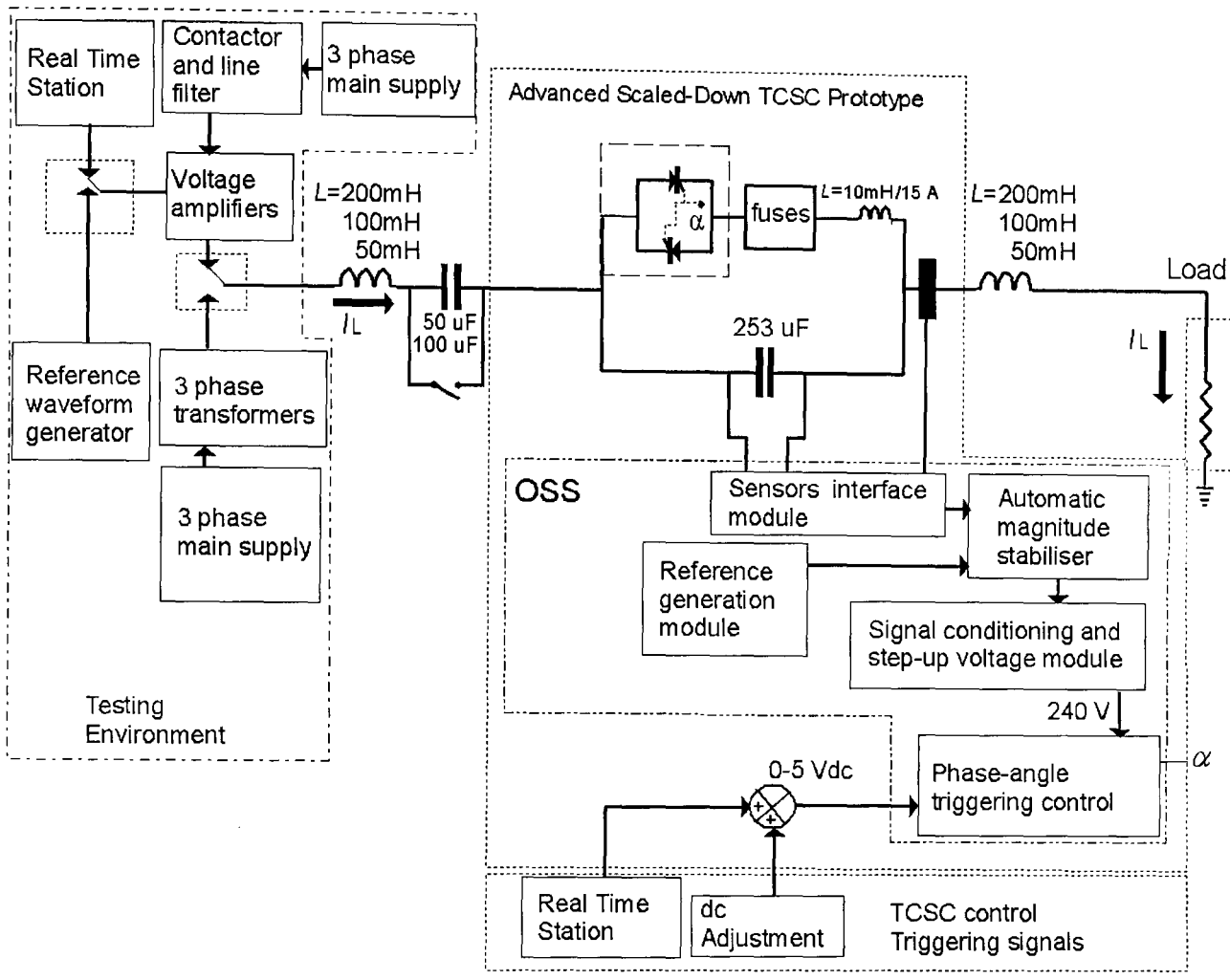
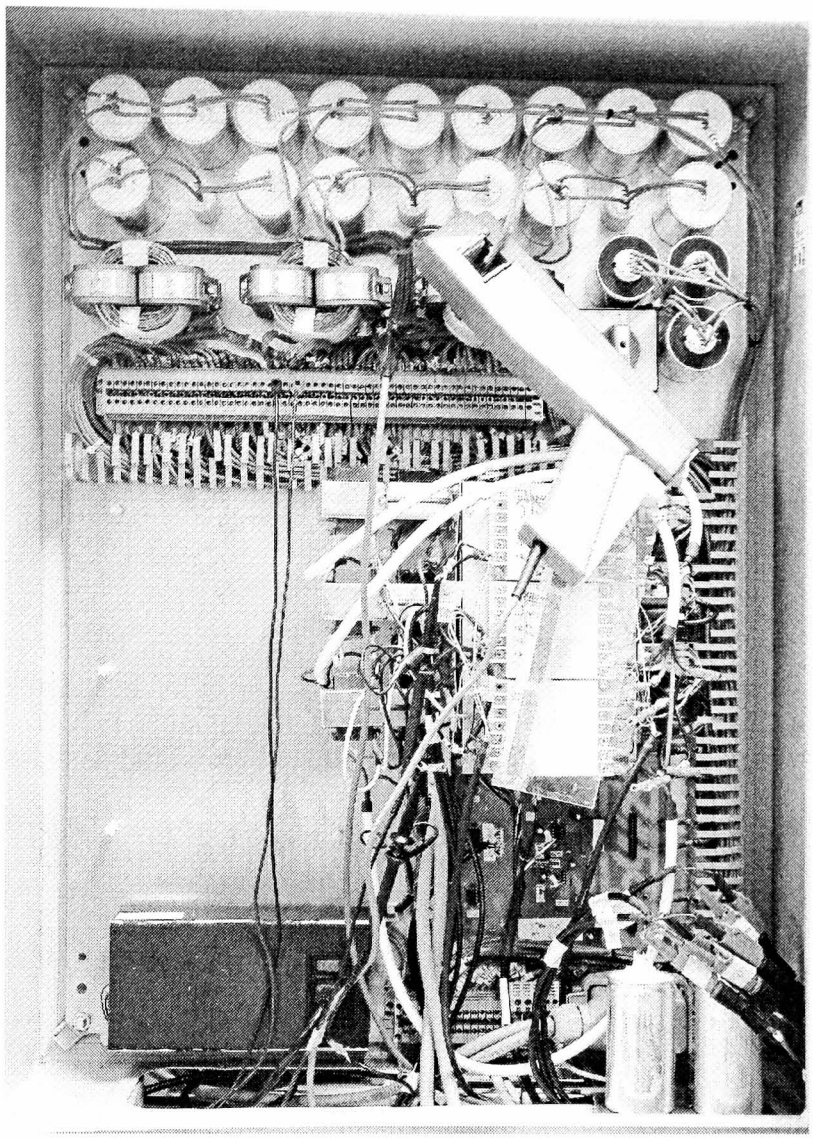


Figure 4.4. Advanced scaled-down TCSC prototype. Block diagram at final stage

The scaled-down prototype has been constructed complying with safety regulations for electrical equipment operating at up to 600 V. Two photographs in of the working scaled-down TCSC are shown in Figure 4.5 including measurement probes and ancilliary testing equipment, which is detailed in Chapter 6.

The TCSC prototype has been extensively simulaed using PSCAD™. The simulation results, which confirms the scaled down prototype as a well-designed TCSC, are presented in Appendix A

a)



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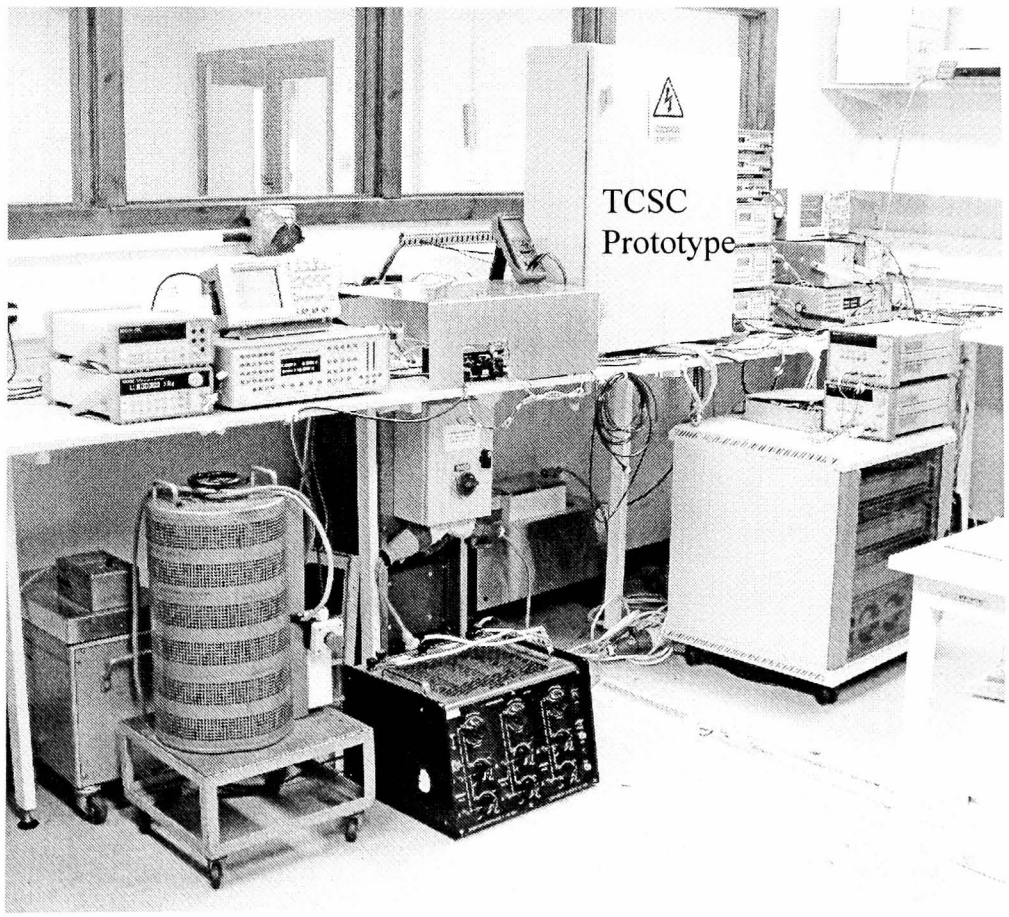

Figure 4.5. Scaled-down TCSC prototype in-situ: a) TCSC internal hardware; b) TCSC at laboratory

4.7 CONCLUSIONS

The design and construction of the advanced scaled-down TCSC prototype has been presented in this chapter.

The combination of the recently introduced design parameters, resonance mode and transition boundary, is useful in determining the electrical characteristics of a well-designed TCSC. The number of potential active resonance modes is in theory mathematically infinite, making the selection of the most suitable parameter for the TCSC a time consuming task.

The newly developed synchronised resonance mode technique is proposed in this research work as a method to reduce the universe of possibilities for the ω/ω_0 ratios and so the L and C values for a specific design. This strategy will minimise the design stage time influencing also the selection of the best components and characteristics for TCSCs for a given application.

A simplified L-C relation is derived based on ω/ω_0 ratios for synchronised resonance modes and the fundamental system frequency in order to facilitate the calculation of values for the LC circuit. The need for an ample triggering angle margin is clearly explained and the application oriented TCSC concept is envisaged. It has been demonstrated in this Chapter that the characteristics of a well-designed TCSC should includes only one active resonance mode, appart from the intrinsic mode, a suitable angle margin concordant with the TCSC application, and a ω/ω_0 ratio into the 0.6666 to 0.3333 range.

The operation support system (OSS) augments the flexibility and capacity of the TCSC prototype. The hardware tools included focus on the monitoring, processing and control of the magnitude, phase and frequency spectrum of the input waveforms used as reference to trigger the TCSC thyristor modules at the specified triggering angle α. The robust construction of the controller TCSC prototype and its support system potentially allows its functionality under diverse steady state and transitory operating conditions.

Digital simulations presented in Appendix A corroborate the smoother, non-oscillatory characteristic performance of the TCSC step modulated in the capacitive region, while

strongly recommends the controller as a well-suited equipment for controlling voltage fluctuation mitigations and transitory oscillations. Further computer simulations results, together with a comparative analysis involving data pertaining to the TCSC module in Kayenta, confirms the newly developed advanced three-phase scaled-down TCSC as a well-designed FACTS controller.

4.8 REFERENCES

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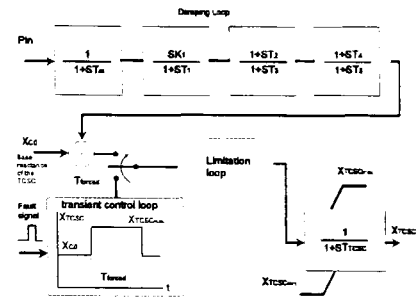
CHAPTER

5



VOLTAGE FLUCTUATION MITIGATION WITH A SERIES FACTS COMPENSATOR: A CONTROL STRATEGY FOR THE TCSC

5.1 INTRODUCTION

The steady state and transient state of transmission and distribution networks are normally analysed using digital simulation. Digital simulators are powerful tools that yield useful information for the better understanding of the control of electrical system. The real-time simulation provides a valuable resource to study the electric network complexities. In Section 5.2 some insights into the software tools used for the development of real-time control strategies are presented.

The FACTS technology is used to improve the operation and control of electrical power systems. The TCSC controller, in particular, has found application in areas such as enhancement of transient stability; mitigation of adverse oscillatory conditions, increment of stability margins, power flow scheduling and loss reduction in transmission corridors. The power system is continuously exposed to abnormal situations. Power system oscillations and subsynchronous resonance are among the unwanted oscillatory operating conditions that electrical systems must overcome for successful operation.

Although the TCSC control strategies found in the open literature for such applications is ample, including a wide variety of mathematical-based tools, the use of physical prototypes have been scarcely reported. Furthermore, very few works are reported using real-time testing environment. Section 5.2 presents a survey on power oscillations, subsynchronous oscillations, and current flow regulation basic concepts. In addition, their associated conventional control schemes are briefly reviewed and three open-loop schemes, developed using EASY5, are presented.

With the ever increasing complexity of modern electrical networks; the incorporation of advanced equipment and controllers; and imminent widespread incorporation of embedded generation units, there is a need to understand better the behaviour and interactions which may arise between the various components in the voltage fluctuations environment. A real-time digital simulator together with testing equipment provides an ideal real-time environment for close-loop experimentation with FACTS and their control strategy. In Section 5.3 presents a new real-time TCSC control strategy, named RT-DIMR, developed for voltage fluctuation mitigation. In Section 5.4 a comprehensive number of simulations have been carried out, using EASY5, in order to test the RT-DIMR capabilities. The simulation results confirm the RT-DIMR as a well-suitable control for voltage fluctuations mitigation.

5.2 DIGITAL SIMULATION SOFTWARE FOR REAL TIME APPLICATION DEVELOPMENT

Conventional power system simulators are powerful tools, which help to understand and to assess the operation of electrical power networks. Arguably, the main drawback is their inability to operate in real-time, which prevents their use in real-time hardware-in-the-loop experimentation. In the all-important area of power systems engineering, all-digital real-time simulators are the modern alternative because they are capable of performing simulations of fast transient electrical phenomena in real-time. They are now commercially available.

The design and implementation of digital models for real time simulation, involves a variety of software tools. The main software tools used in this research work are EASY5 [1], Advantage-IDE [2] and COSIM-Interact [2]. EASY5 is a set of software tools initially developed by Boeing Co. Advantage-IDE and COSIM-Interact are members of the SIMsystem tools developed by ADI to exploit fully the architecture and powerful real-time capabilities of its Real Time Station.

5.2.1 EASY5

EASY5 is a set of graphic-based (GUI) software tools used to design, model, analyse and simulate complex dynamic systems of various kinds, such as electrical, automotive, and hydraulic. The application libraries include primitive functional blocks, such as generic transfer functions, and special systems characterised by differential, difference and algebraic equations. The analysis tool options are a key feature of EASY5, including steady-state analysis, linear and non-linear simulation, data analysis and plotting.

The flexibility of EASY5 permits the direct inclusion of tailor-made user code written in FORTRAN and C. This feature is well suited to many real-time applications, including, but not restricted to, transmission and distribution equipment and systems. This feature is used for the RT-DIRM control strategy, in sections of the implemented virtual IEC-flickermeter and the statistical calculation of P_{st}.

The application design stage is accomplished using either the host workstation connected to the RTS or a PC platform. Once the different blocks for the application have been interconnected, and the component parameters set, the EASY5 code generator translates all the system models into FORTRAN or C source code, building executable code that runs when the analysis tool is launched. If the application is built using EASY5 for real-time running in the RTS, the Advantage-IDE and COSIM-Interact software are required. A number of off-line interactive simulations are carried out in order to debug, optimise, and evaluate the performance of the newly developed models.

5.2.2 Advantage-IDE

The Advantage-IDE tool is an easy-to-use graphic interface that enables the user significant time reduction in the design and construction of real-time hardware-in-the-loop simulations. This tool facilitates the hardware I/O configuration, the system model integration from EASY5, the incorporation of additional FORTRAN source code, the multi-processor architecture configuration, and preparation of the RTS configuration to run real-time simulations. The Advantage-IDE modular structure allows model variables to be easily connected to device channels, and to select the processor and I/O internal data scheduling. The system model source code and configuration settings options are linked together into an executable machine code, using the OASYS code assembler, which is downloaded into the RTS ready for real-time simulation running.

5.2.3 COSIM-Interact

The run-time development environment provided by COSIM-Interact allows the user to download the real-time machine code onto the RTS and to control the code execution during run time, which greatly facilitates the analysis, debugging and testing of application system models. The main features of COSIM Interact includes: run-time statistics, status flags for every device on the VME bus, a set of debugging commands as breakpoints and trace-backs, variables manipulation with schedules and triggers. Included in the tool is the Actual Frame Time (AFT) statistic parameter, which indicates the actual time that the RTS platform uses to compute every time step of simulation. If AFT exceeds the set time step, the simulation does not run in real time. The solution to make the simulation run in real-time can be as laborious as to require code reduction and optimisation; or as simple as to only increase the time step. Simulations running on COSIM-Interact can be visualised using the SIMplotter tool, also provided by ADI [2]. COSIM Interact is the cornerstone for run-time development with the ADI's RTS.

5.3 TCSC CONTROL STRATEGIES FOR POWER SYSTEMS

Today's electric power systems are large, complex structures that are not able to operate without state-of-the-art controllers, posing great many challenges to ensure their secure and economic operation. Besides its normal operation, the power system is continuously exposed to a multitude of perturbations or abnormal situations, which can lead to disastrous results if no proper control action is taken. Power system oscillations and SSR are among the unwanted oscillatory operating conditions the system must overcome for successful operation.

The FACTS technology has been designed to play a role in the operation and control of electrical power systems, including both the steady state and small signal and transient stability problems. In particular, the TCSC controller has so far been used for the following purposes: enhancement of transient stability; damping power oscillations, damping of SSR, increasing stability margins, power flow scheduling and loss reduction in transmission corridors. The TCSC control strategies found in the open literature for such applications are abundant in both breath and depth, including an ample variety of mathematical-based tools [3]. However, physical prototypes have been used scarcely. Furthermore very little work reports on the use of real-time experimentation [4-12,13].

The TCSC fundamental impedance control loop at steady state is represented by the lagging transfer function shown in Figure 5.1 [3,14,15].

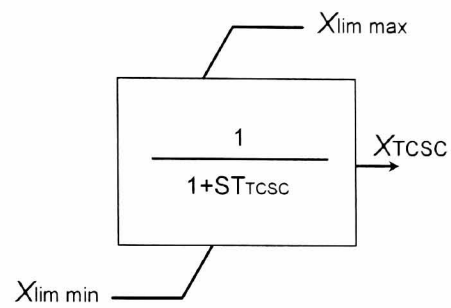


Figure 5.1. First-order lag function for the TCSC

This first-order lag is directly related to a non-time varying triggering angle and the natural response of the TCSC, which is represented by T_{TCSC}. The model's maximum and minimum limits are imposed by the TCSC's capability curve, pictured in Figure 5.2 [14]. The T_{TCSC} ranges from 15 to 30 ms [15], in particular, one of the TCSC modules of the Slatt installation is T_{TCSC} = 15 ms [14].

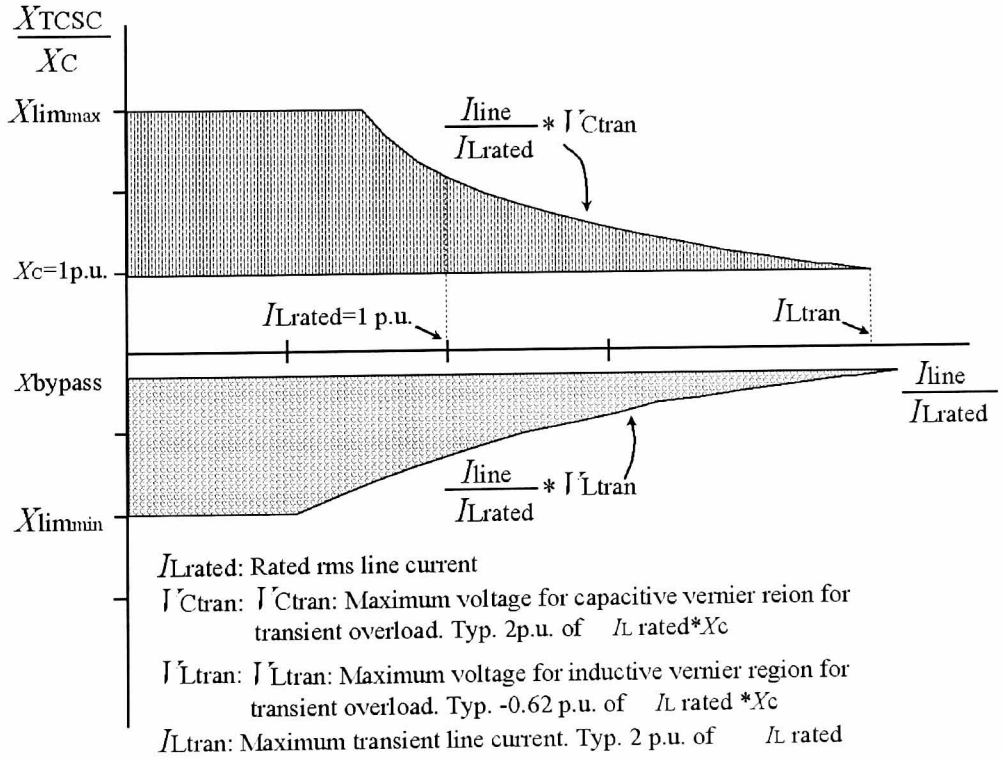


Figure 5.2. Operating ranges of the TCSC

A generic, conventional block diagram of the TCSC control, which is well suited for stability studies, is illustrated in Figure 5.3 [3,14,16].

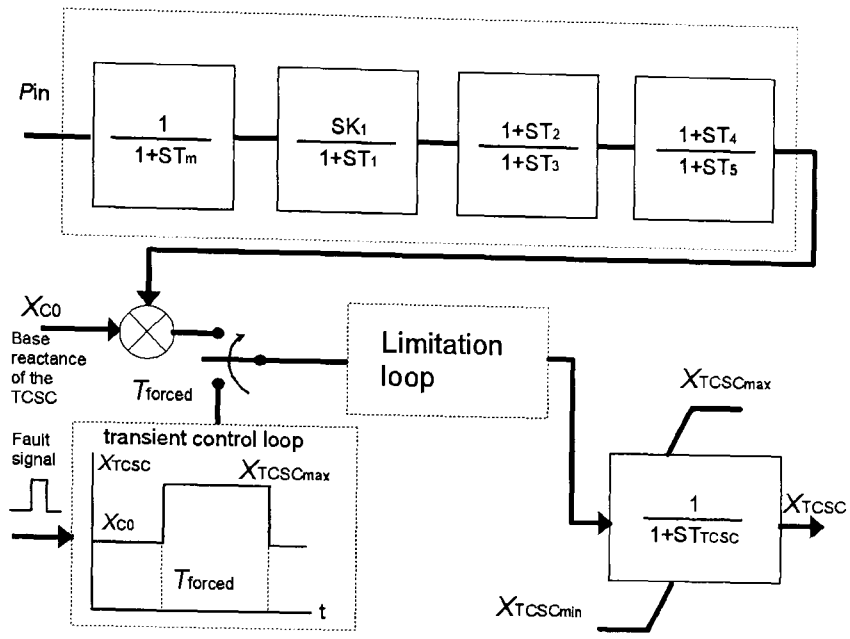


Figure 5.3. Representative stability control scheme.

This conventional control scheme includes three main branches: transient loop, damping loop and model loop. The model loop includes the transfer function that simulates the steady-state TCSC output characteristics. The transient loop provides the control actions required for improved transient stability, by controlling, for instance, the initial swing after a fault condition. The power oscillations are mitigated by the control actions of the damping loop. A combination of transient and damping control actions is possible by following a well co-ordinated strategy.

Research on control strategies involving full or scaled-down TCSCs can be traced back to the early 1990s, when N. Christl et al [4,17,18], reported on schemes for steady state control, bang-bang control and SSR mitigation, all of them in connection with the Kayenta scheme. Subsequently, reports on the Slatt project started to appear; Urbanek J. et al [9] detailed the TCSC prototype, operation and test programme. In this project, the control module has three basic functions: reactance control, SSR voltage modulations and thyristor module bypass. Hauer J. F. et al [10] focuses manly on SSR and swing damping tests performed with the plant off-line, detailing the network configuration and instrumentation used. Field-tests and contributions of the TCSC to SSR mitigation are the main aspects of the work reported in [11]. In spite of the quantity and quality of the available references, little explanation of the control scheme has so far been provided.

Building on conventional TCSC control schemes, a voltage fluctuation mitigation control strategy is developed in this research, termed Real-Time Dynamic Instantaneous Mitigation Response, RT-DIMR. This is presented in this chapter with reference to the three-phase scaled-down TCSC prototype.

5.3.1 Power Oscillations

Fundamental electromechanical oscillations are inherent to interconnected power systems where, nevertheless the configuration, the generator tendency is to remain in synchronism. In fact, oscillations in the power system were observed in the early electric power networks. Even in the presence of minor disturbances in an under-damped transmission system, machines tend to deviate little from their synchronous speed. In such cases, the angle oscillates around its steady-state value at the natural frequency of the total electromechanical system, resulting in a power oscillation around the steady state of the power transmitted. From the operating point of view, these oscillations are acceptable, as long as they decay. These oscillations are intrinsic in the system; they can also be initiated by the normal, small changes in load. In any case, if the system damping is insufficient, the transmission systems may undergo a major problem, such as growing oscillations and even system collapse, as demonstrated in the major blackout that occurred in the US/Canada interconnected system in 1996 [19].

Starting in the 1960's, the damping of power oscillations has been solved with the use of supplementary excitation signals, provided by control systems commonly known as Power System Stabilisers (PSS) [20]. The PSS is located next to the elements generating the oscillations, not requiring the installation of bulky power apparatus [21]. However, with increasing transmission line loading over long distances, the damping of inter-area oscillations could not be damped satisfactorily using conventional PSS [16]. Problems with the design and placement of power system stabilisers arise when attempting to co-ordinate multiple power system stabilisers in multi-machine systems [20, 22].

As utilities increase power exchanges over inflexible networks, inter-area oscillations are more likely to happen, even under nominal operating conditions. While power systems stabilisers remain the main damping tool, FACTS equipment such as the TCSC and the SVC are gaining growing attention as tools to be used as countermeasures to damp small signal oscillations [4,16,20,23-27]. In particular, the usefulness of the TCSC for damping power oscillations has been demonstrated through the application of real-life, full scale TCSCs [4,25] and a number of studies based on digital simulations [3,4,8,23,26,28].

The low-frequency bang-bang method used in the TCSC is a well-known method to damp power oscillations [4,27]. The key steps for the scheme consists in effectively controlling the electric power transmitted into the system as follows [27]: a) to compensate for the excess of mechanical input when the generator accelerates, the electrical power transmitted must be increased; b) when the generator decelerates, then the electric power transmitted is decreased to complement the mechanical input power.

Figure 5.4 illustrates case of damped and undamped waveforms; including the generator angle, power transmitted and series compensation contributed the TCSC [27].

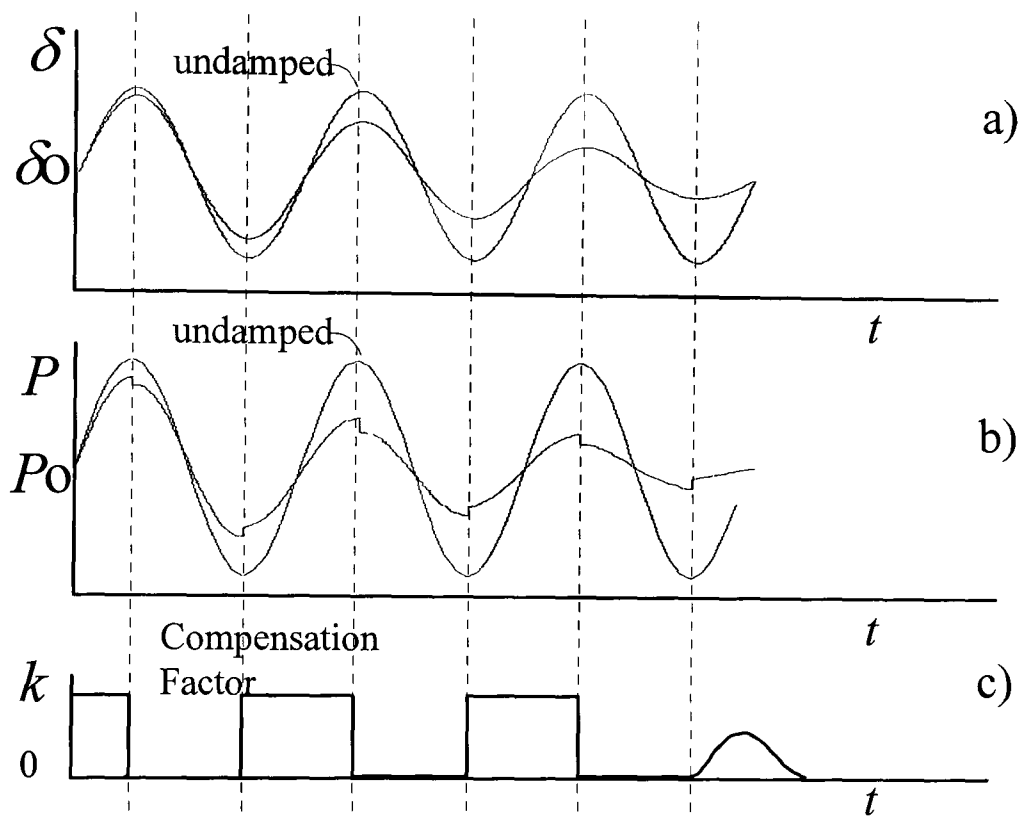


Figure 5.4. Power oscillation-damping profiles: a) generator angle, b) transmitted power, c) degree of compensation.

Complementary to this section, Figures 5.5 and 5.6 show the control loop and the waveforms resulting from digital simulations carried out in open loop, and using the bang-bang strategy developed using EASY5. The power oscillations are taken to be in the 0.5 – 10 Hz range where most of the oscillations fall. In this case, the damping control is based on a conventional transfer function-based control open loop consisting of two lead-lag stages, a first-order lag and the output [3]. An additional lead-lag is included for amplification and phase-shift compensation purposes. The control was tuned following an iterative simulation process. The final parameters used are also shown in Figure 5.5.

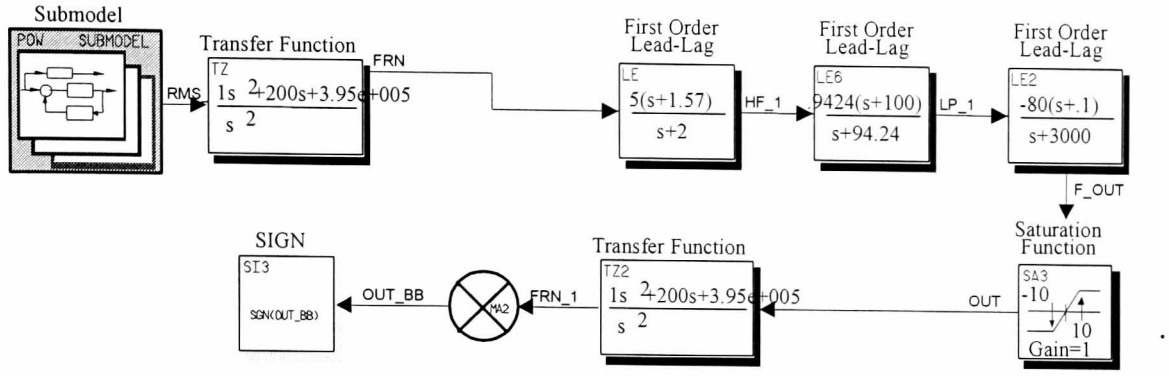


Figure 5.5. Power oscillations control loop

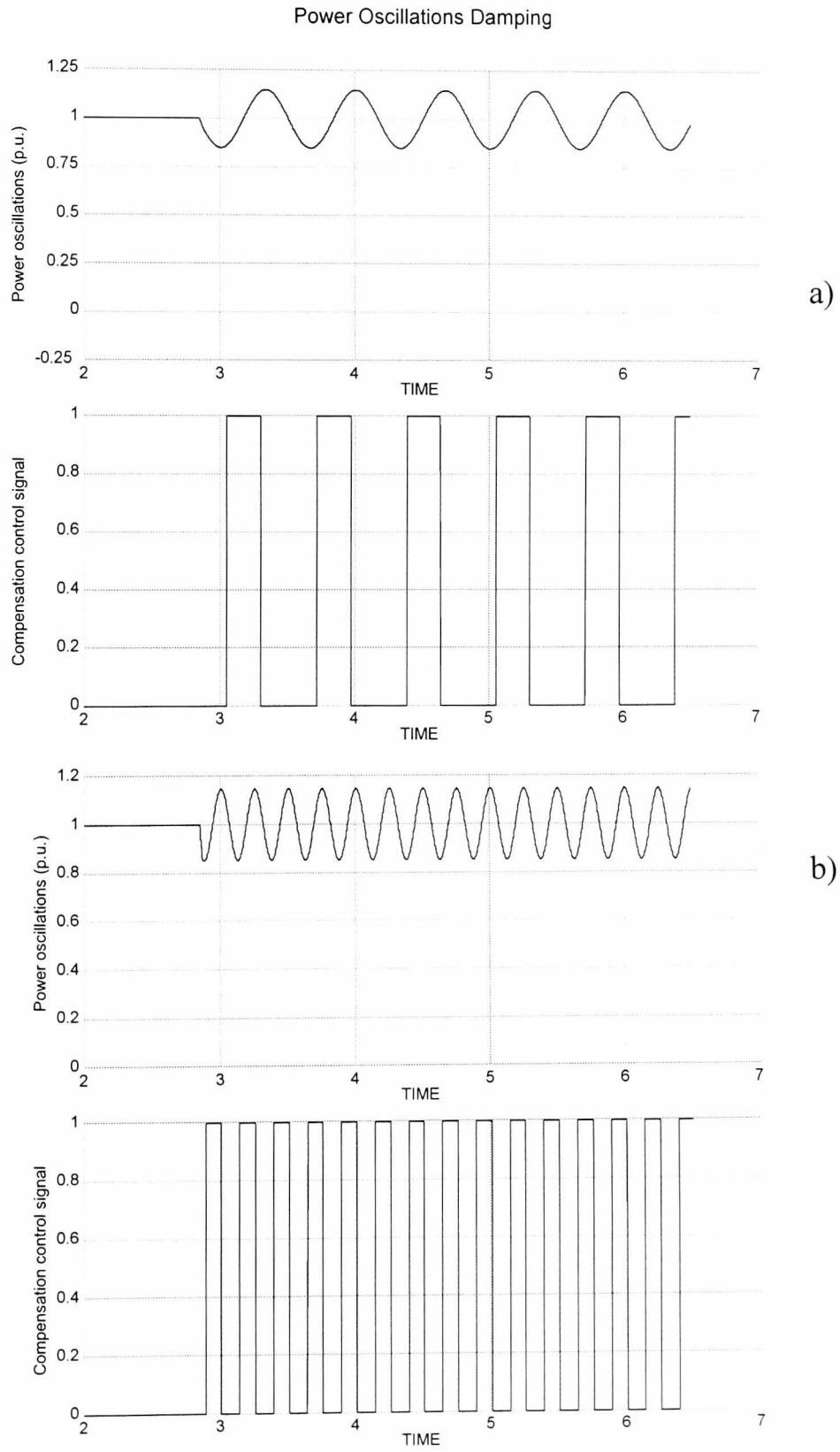


Figure 5.6. Open loop simulation. a) control response to 1.5 Hz oscillations; b) control response to 4 Hz oscillations.

5.3.2 Subsynchronous Resonance

The transmission system is designed to operate at nominal frequency, 50 Hz or 60 Hz. As a result of the integration of large multi-machine systems, an ample range of resonant oscillatory modes co-exist with the nominal frequency. Most of these oscillations are mitigated because of the positive damping of the network. However, sustained oscillations below the power frequency may appear, a phenomenon arising because the total inductive series reactance is compensated using series capacitive reactance. This phenomenon is commonly referred to as subsynchronous resonance (SSR) [19,15,29].

The first SSR phenomenon was observed in 1937. Nevertheless, its importance was only realised after a major destructive failure occurred in the 1970s at the Mojave generation station in Nevada, USA. The IEEE has formally defined the subsynchronous resonance as follows [29]:

Subsynchronous resonance is an electric power system condition where the electric network exchanges energy with a turbine generator at one or more of the natural frequencies of the combined system below the synchronous frequency of the system.

The definition includes any system condition which leads to an energy exchange at some subsynchronous frequency. This means that several SSR modes exist in the network, some modes of oscillation are due to the inherent system characteristics but other modes of oscillation are driven by a particular device or control system. The most common natural mode of SSR is related to series compensated transmission lines.

The subsynchronous oscillations exist when the interactions between a compensating series capacitor, oscillating at the natural frequency, and the mechanical generator system are set in torsional mechanical oscillations, resulting in negative damping and boosting the electrical and mechanical oscillations. The range of frequencies for such torsional oscillation modes is in the range of 10 to 50 Hz [4,11,15,19,27,29,30]. Large generators with multi-stage turbines are most susceptible to subsynchronous resonance when series capacitor transmission lines are used.

An analytical method for SSR damping consists in the computation of the eigenvalues of the linear model of the system. In this case, the main interest is not a detailed representation of the power network. Instead, the models for the turbine and generator together with their primary controls, the speed governor and the excitation system, are of importance.

The eigenvalues that have negative real parts are damped, but those with positive real parts represent resonant conditions that can lead to catastrophic results. The computation of eigenvalues and eigenvectors is an excellent method that gives crucial information on the SSR nature of the power system [15,19, 29, 31].

A relatively new control strategy, using FACTS-type devices for the mitigation of SSR is the so-called NGH-SSR scheme [27]. This is a thyristor-based controller. The idea behind the scheme is to trigger the thyristors at a fixed delay angle α, considering the zero-crossing point of the capacitor voltage, and discharge the capacitor at the end of each half cycle, preventing any subsynchronous oscillation from building up.

The eigenvalues calculation and the NGH-SSR scheme are not the only techniques or supporting measures to alleviate SSR problems. Over the years, a number of methods have been proposed in the open literature [21]:

- Static Filter: This is a blocking filter (parallel-resonance type) in series with the generator, or a damping circuit in parallel with the series capacitors.
- Dynamic Filter: This is an active device placed in series with the generator. It collects a signal derived from rotor motion and produces a voltage in phase opposition so as to compensate for, or even exceed, the subsynchronous voltage generated in the armature.
- Dynamic Stabiliser: This scheme uses thyristor modulated reactors connected to the generator terminal. The SSR control is achieved by modulating the thyristor-triggering angle, using signals derived from the generator shaft speed.
- Excitation system damper: Generator excitation control is modulated using a shaft speed derived signal providing increased torsional oscillations damping.
- Protective Relays: The SSR condition is detected by a relay, tripping the affected units. The relay may take several forms: detection of excessive torsional motion by sensing rotor speed or detection of SSR condition by sensing the armature current.

The TCSC controller has been advantageously used to improve the power system under SSR conditions. The TCSC mitigation capabilities have been proven in full-scale installation [4,8,11,13] and using single-phase physical prototypes in controlled laboratory environments [30]. The TCSC operation does not contribute adversely to SSR [11,15]. The smooth controllability of the TCSC capacitive reactance and its ability to vary the transmission system reactance at subsynchronous frequency [4.8] are

important advantages brought about by this controller. In fixed capacitor-TCSC configurations, such as the Kayenta scheme, the equivalent impedance varies from an inductive to a capacitive reactance, as the triggering angle increases towards 180° changing the SSR torsional interactions conditions [4]. For SSR mitigation, a smooth modulation of the TCSC capacitive impedance in the vicinity of the nominal line voltage and current is commonly applied. This technique varies the TCSC's triggering angle within a delimited region following the variation of the line voltage [4].

Figure 5.7 illustrates the open loop scheme, developed in EASY5, which generates the TCSC control modulation signal used to mitigate SSR conditions. The SSR loop output in the control is designed to modulate the TCSC triggering angle smoothly. The modulation varies, tracking the frequency differences between the disturbed and non-disturbed input signals. In the scheme, a second-order all-pass stage is used to induce a phase delay to the input voltage when frequencies different from 50Hz are present. The non-delayed input signal and the delayed processed signal are compared and the difference is processed to trigger the TCSC thyristors. The control does not include the processing stage, based on eigenvalues, used to discriminate between the normal and abnormal system operation.

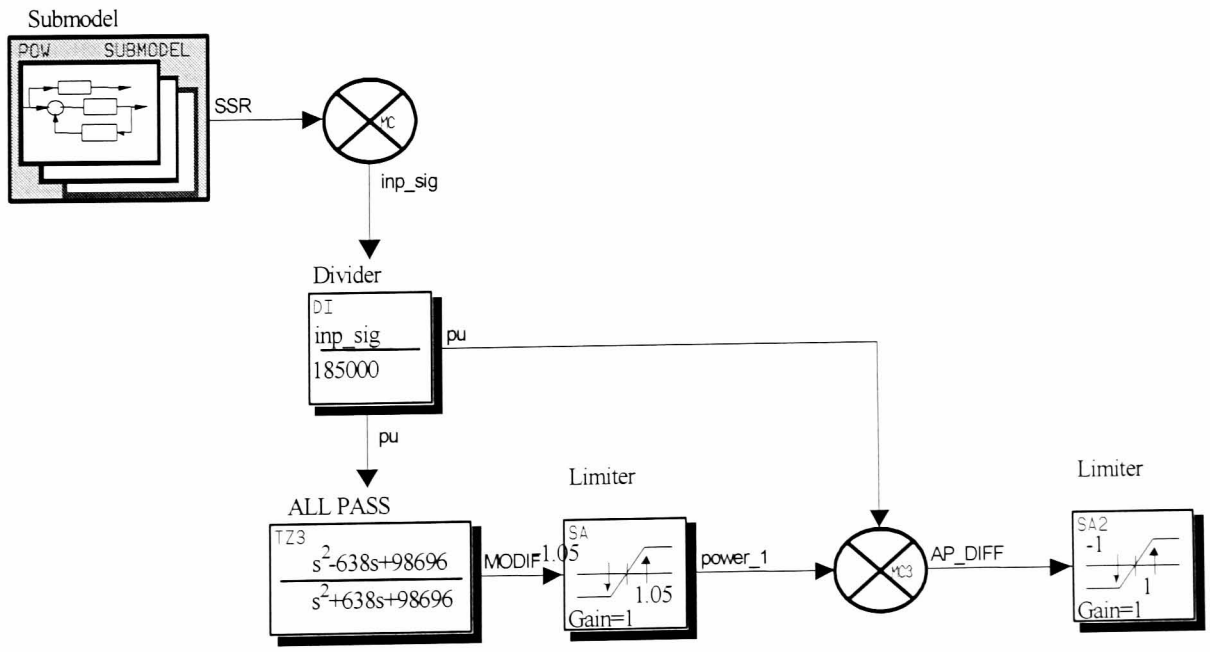


Figure 5.7. SSR open loop TCSC control scheme

5.3.3 Close-Loop Control Scheme for Current Flow Regulation

Under normal steady-state conditions the TCSC operates by regulating the fundamental component of the line current. The variable reactive impedance of the TCSC controller is adjusted by controlling the triggering angle, which is in proportional correspondence with the measured line current with respect to a reference. The TCSC capacitor voltage can be included as a system variable to derive additional operating references. The control law governing the TCSC–line current relationship is normally a PI-type controller, as in the Kayenta scheme [4], as depicted in Figure 5.8, which includes a 4^{th} order transfer function model representing the TCSC. Figure 5.9 shows two different close-control loop representations. In scheme a) the regulator output provides the final trigger angle to the thyristor block [16] whereas in scheme b) the output from the PI controller is post-processed by an internal control in order to calculate the final triggering angle [8,16,27]. This angle results from the difference between a reference angle and an estimated angle using the actual zero crossing of the capacitor voltage. As a result of controlling the final triggering angle, the conduction of the thyristor branch tends to be symmetrical.

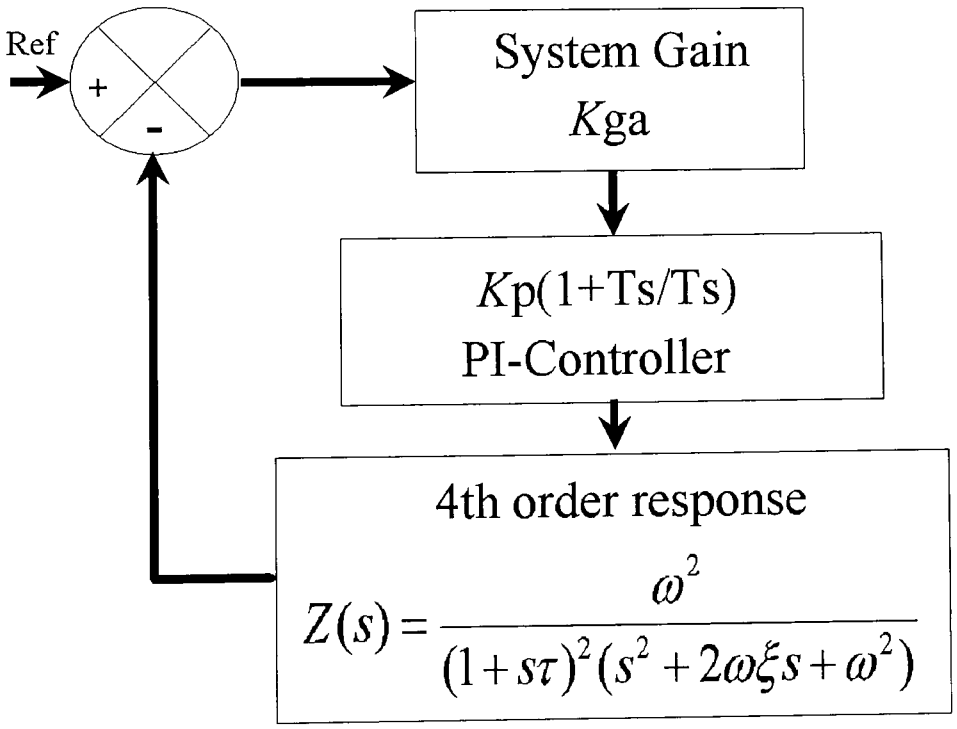
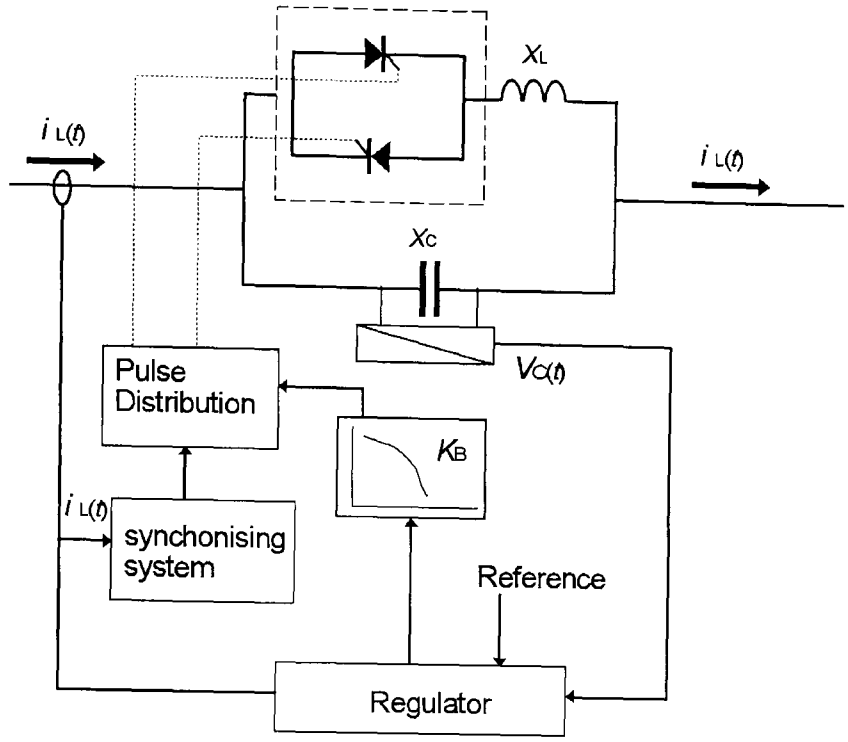


Figure 5.8. Conventional close-loop control block diagram.



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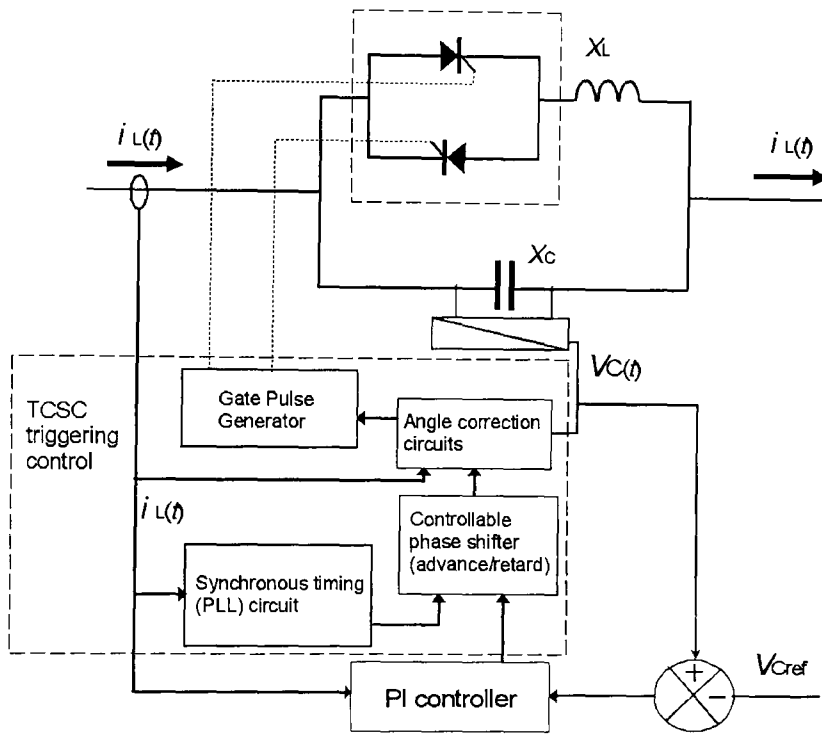


b)

Figure 5.9. Close loop control schemes. a) PI scheme with direct firing angle. b) PI-scheme based on estimation of capacitor zero-crossing occurrences.

A proposed generic control block diagram for the TCSC is presented in Figure 5.10. The control structure is a conventional scheme but incorporating a non-linear pre-distortion block in order to present a quasi-linear TCSC to the PI-controller. The relation between the TCSC triggering angle and its reactive impedance is not linear in nature. This is particularly evident as the triggering angle approximates to the resonance point of the TCSC.

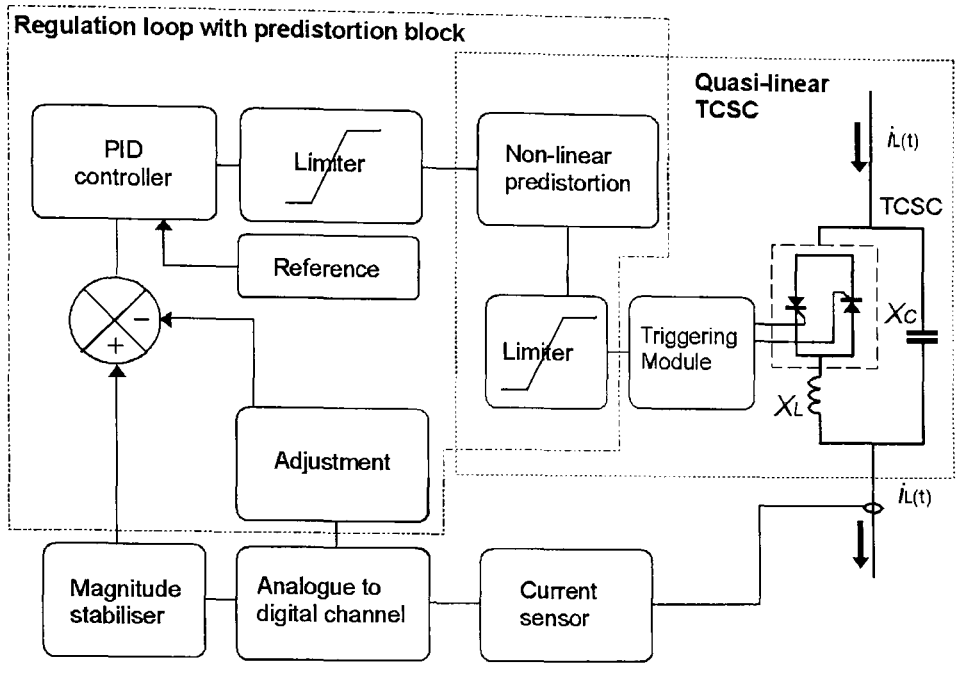


Figure 5.10. Generic regulation loop with pre-distortion block

The combined operation of the pre-distortion block and the TCSC capacitive reactance region presents a quasi-linear behaviour to the control system. Figure 5.11 shows the TCSC fundamental impedance with and without the pre-distortion block. It can be noticed that using the quasi-linear TCSC behaviour a smoother control is possible in the proximity to resonance. Figure 5.12 shows the regulation loop with pre-distortion block and Figure 5.13 shows the waveforms resulting from digital simulation of the control scheme using EASY5. It should be pointed out that the regulation scheme has been developed based on the block diagram presented in Figure 5.10.

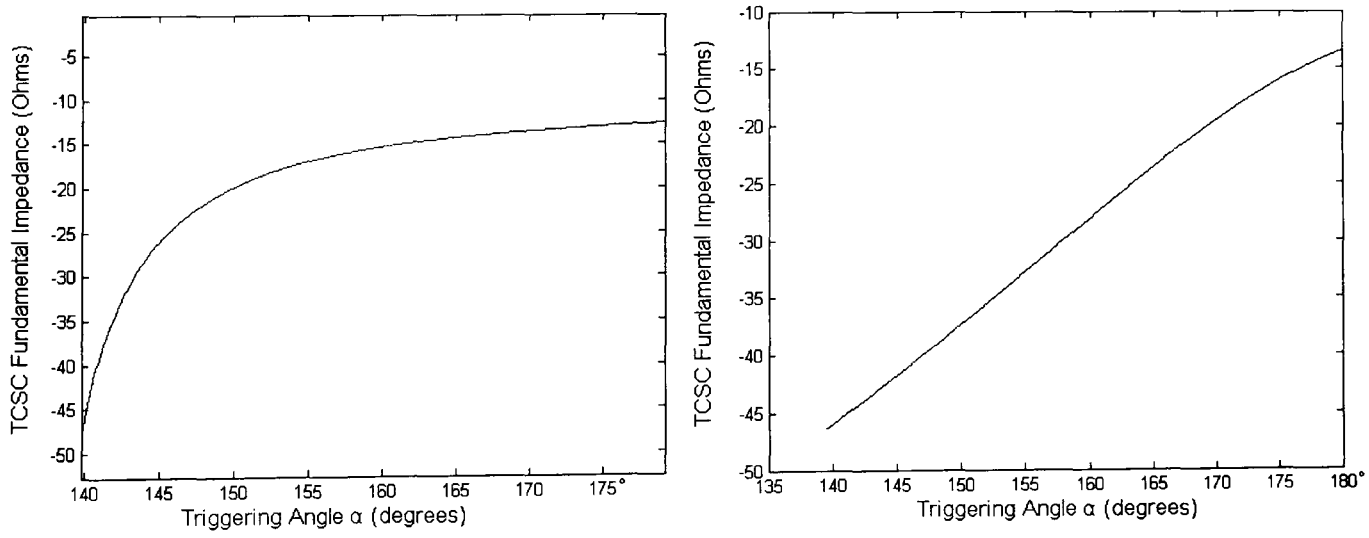


Figure 5.11. TCSC fundamental impedance: a) no- liner behaviour; b) quasi-linear behaviour.

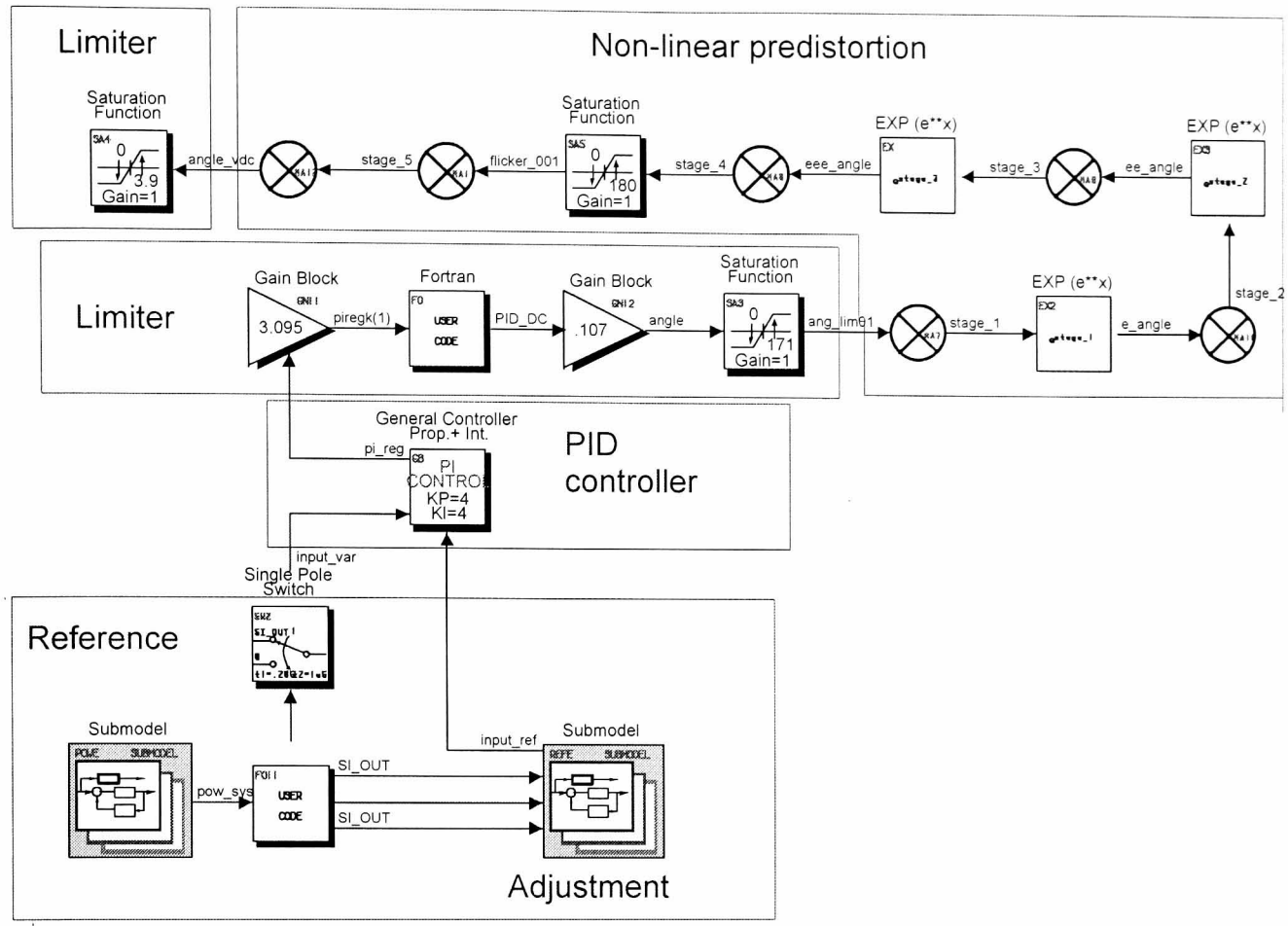


Figure 5.12. Regulation Loop Model

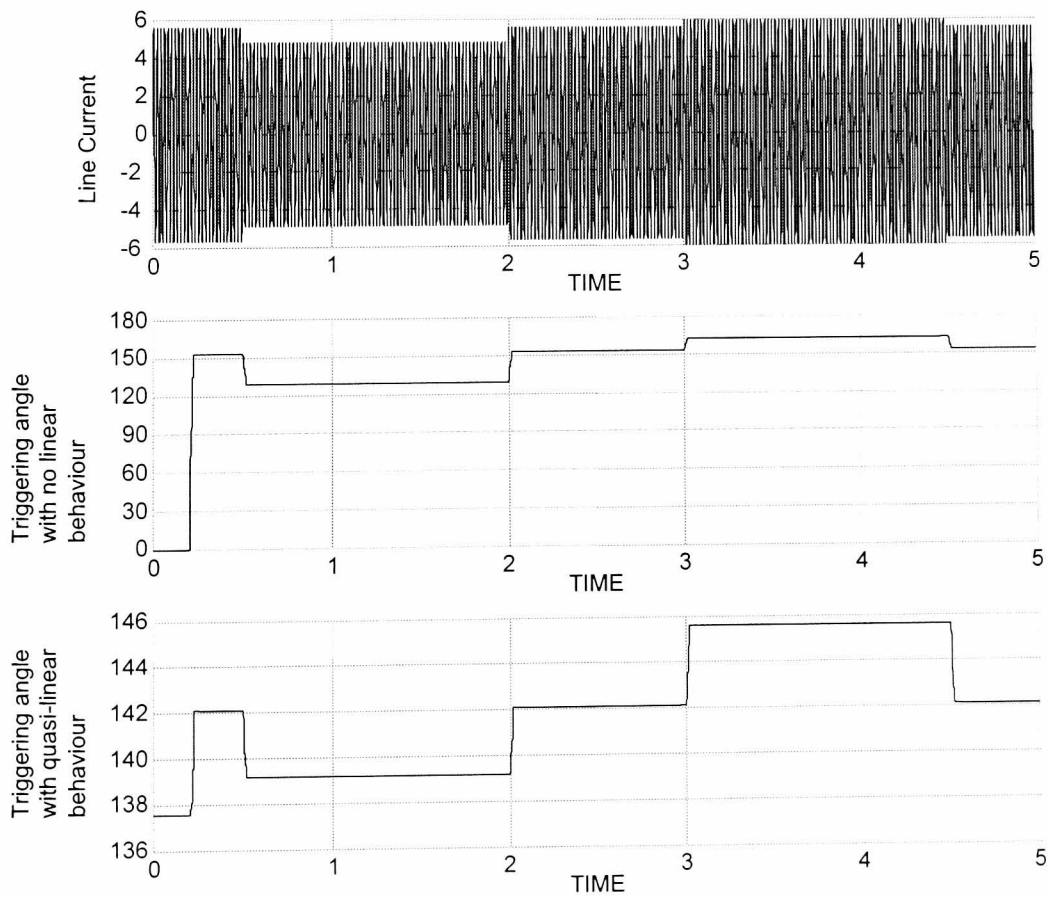


Figure 5.13. Regulation loop digital simulation waveforms

Figure 5.13 show the control output response to changes in the current flow magnitude. The three waveforms correspond to the line current; the triggering angles changes when the linear pre-distortion block is not used and when it is used. Between t=0 and t=0.5 s, the line current is at nominal value. At t=0.5 s, a load change is introduced, lowering the line current. In response, the control tends to increment the triggering angle in order to lower the TCSC impedance and augment the line current.

At t=2 s and t=3 s, the line current is incremented. In response, the control loop decrements the triggering angle, which provokes an increment of the apparent TCSC capacitive reactance and tends to lower the line current.

It should be noticed in Figure 5.13 that the triggering angle changes are larger, and nonlinear, if the pre-distortion block is not used. However, when this block is used, the α changes are not abrupt and occur only in the vicinity of the triggering angle used for nominal line current (α=142° for this case). The use of the pre-distortion block facilitates the line current regulation using a TCSC due to the reduction of the control sensitivity to line current changes. As a consequence, a smoother regulation is possible.

It should be mentioned that the control is operating in open loop for the case presented in Figure 5.13.

5.4 THE REAL-TIME DYNAMIC INSTANTANEOUS MITIGATION RESPONSE (RT-DIMR): CONTROL STRATEGY STRUCTURE

The set of rules governing the controller behaviour plays an important role in determining the effectiveness and versatility of the TCSC application. The following section gives a detailed description of the Real-Time Dynamic Instantaneous Mitigation Response control strategy. A real-time HIL testing environment, where the RT-DIMR is developed and evaluated, is illustrated in Figure 5.14. Further details about the testing environment are presented in Chapter 6.

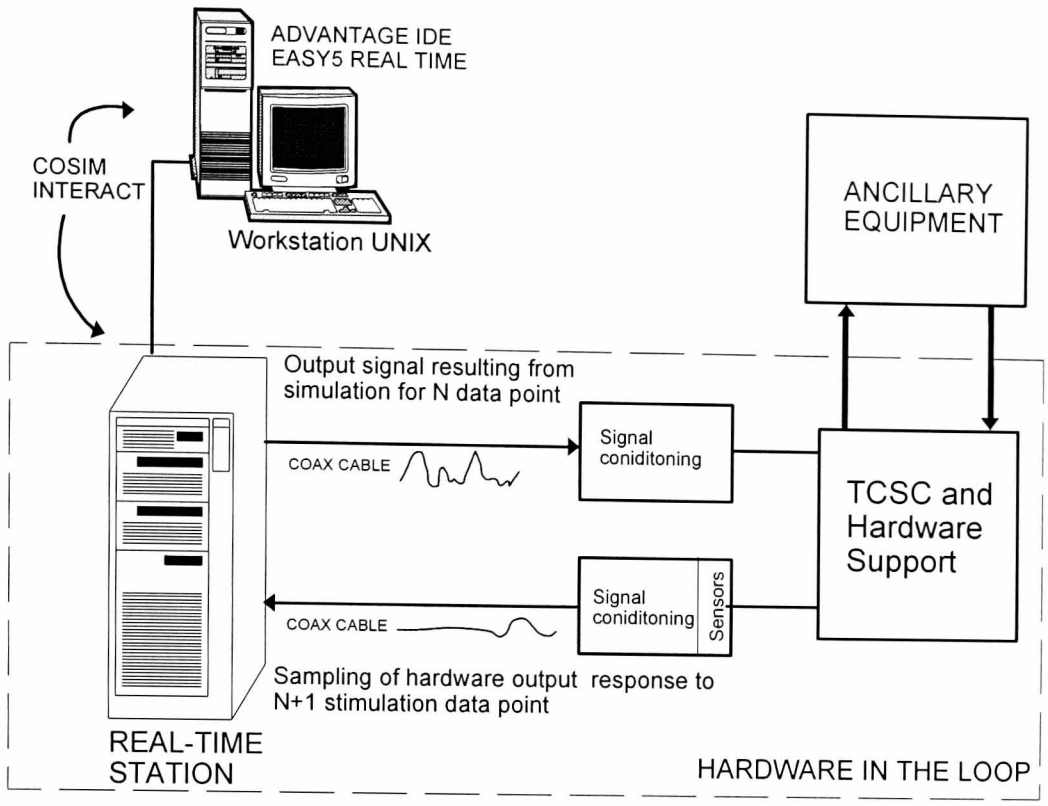


Figure 5.14. Real-time HIL testing simulation scheme.

5.4.1 RT-DIMR General Structure

The general characteristics of the TCSC control strategy required for voltage fluctuation mitigation are given below:

- Real-Time closed loop operation in HIL environment
- Dynamic interactivity with the system under test
- Dynamic adaptation to time-varying sinusoidal and non-sinusoidal voltage fluctuations with wide operating bandwidths, including the range of voltage fluctuation frequencies from sources such as EAF, DC-EAF, wind farms, large induction motors and other sources of voltage fluctuation
- Flexibility to adjust the compensation step triggering angle commanded to the TCSC
- Fast signal processing time to minimise input-output delay time
- Three independent phase operation
- Selectable error margin and fixed delay time adjustment

After careful analysis, the TCSC control options best fitting the application requirements of voltage fluctuation mitigation, have been identified and evaluated. These are presented in Table 5.1.

Table 5.1 Control strategy design options

Control law
1. PID regulator
2. PID + branch loop for instantaneous compensation
3. Direct dynamic instantaneous compensation
Control reference
1. Short-term severity index, P_{st} or Instantaneous flicker level, IFS
2. Instantaneous fluctuations of voltage
3. Instantaneous active power or reactive power
4. p-q decomposition
TCSC impedance operating region
1. Inductive reactance only
2. Capacitive reactance only
3. Combined capacitive – inductive reactances
Control input variable
1. Instantaneous line voltage
2. Instantaneous line current

The new real-time HIL TCSC-based control strategy has been termed Real-Time Dynamic Instantaneous Mitigation Response (RT-DIMR). The selected options from Table 5.1 for this control strategy are: a) direct dynamic instantaneous compensation; b) instantaneous fluctuations of voltage; c) TCSC capacitive region only; and d) selectable instantaneous line voltage or current.

The main characteristics of the new RT-DIMR control strategy are highlighted below:

1 Real-time HIL operation
2 Maximum computing time step: 500 μs
3 Voltage fluctuation bandwidth for immediate response: 0 – 25hz for 50hz fundamental frequency systems
4 Instantaneous mitigation of the voltage fluctuation using dynamic adjustment of the output response frequency by instantaneously tracking down the dynamic varying input signal fluctuation
5 TCSC mitigation response by selecting the appropriate apparent impedance between two pre-set minimum and maximum capacitive reactance values in agreement with the polarity of the extracted fluctuating input waveform.

6 Phase-independent instantaneous RMS calculation

7 Selectable input variable between line voltage and line current.

8 Three independent phase operation.

9 Selectable output triggering level.

10 Adjustable input-output response time

The development of the RT-DIMR control strategy and the initial off-line simulations were carried out using EASY5. The real-time, open-loop tests are carried out using a Real Time Station. Figure 5.15 shows the EASY5 block diagram for the RT-DIMR. The FORTRAN routines for the RT-DIMR control strategy are enlisted in Appendix B.

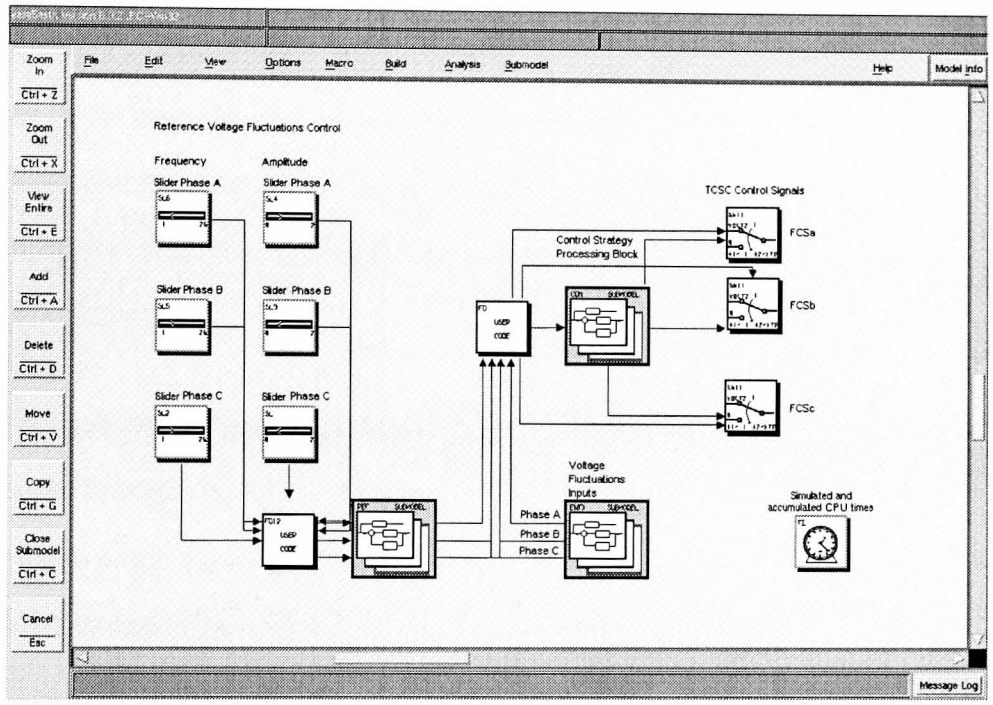


Figure 5.15a. RT-DIMR generic blocks

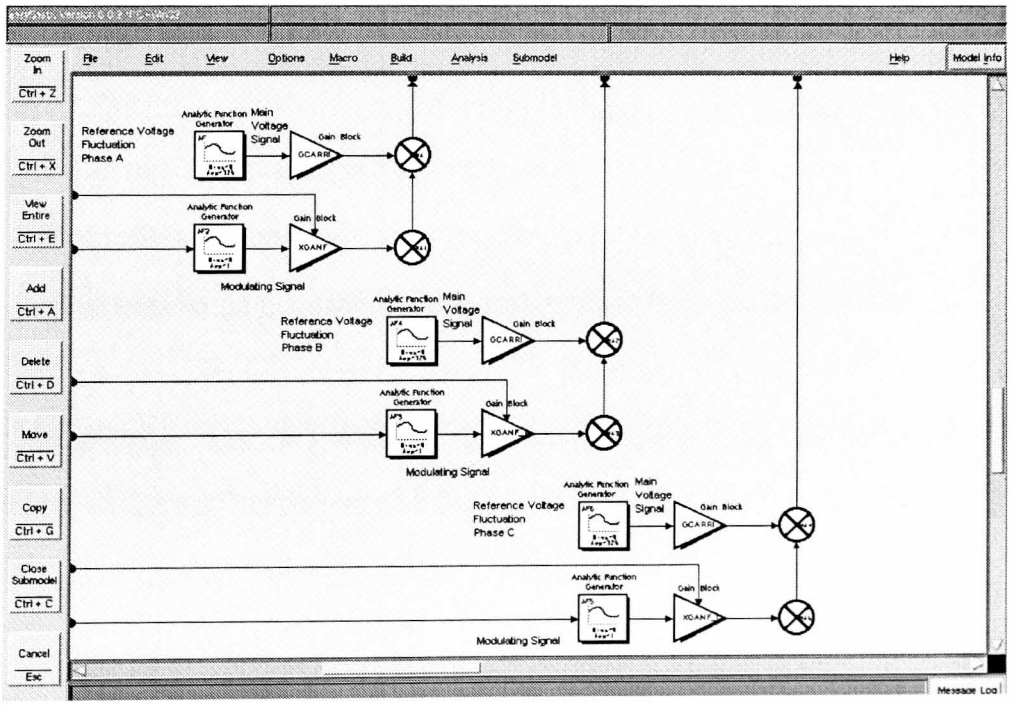


Figure 5.15b. Reference voltage fluctuations models.

Figure 5.15. EASY5 models of the RT-DIMR control strategy

5.5 RT-DIMR IMPLEMENTATION: A DESCRIPTION

The control scheme has been initially developed focusing on single-phase, non-real-time operation. This was then extended to encompass the three-phase scheme and suitably transformed to operate on a real-time basis. The modular structure of the RT-DIMR greatly facilitates the integration of models, adjustments in configuration, modifications in the source code, debugging of the application, and dynamic interactions between the Real Time Station and the user.

RT-DIMR dynamically boosts the TCSC using synchronised step-shaped triggering angle output pulses. This procedure effectively compensates a significant portion of the inductive reactance of the transmission line at a frequency equal to the frequency of the rms fluctuating line voltage or current. One immediate effect of the partial cancellation of the total inductive reactance is the dynamically controlled increment of short-circuit level, which ameliorates the voltage fluctuations and consequently, reduces measured flicker severity index.

The RT-DIMR control philosophy has three fundamental objectives: 1) the wide-band instantaneous detection of the varying fluctuating waveform modulation that governs the voltage fluctuation phenomenon; 2) the instantaneous generation of the analogue control response to such input stimulus on a real-time HIL basis; and 3) a flat time delay response.

The RT-DIMR design is divided into three main stages

- Stage I: Filtering and phase delay adjustment
- Stage II: Detection of dynamic varying waveform fluctuations
- Stage III: Generation of control output signals for mitigation.

Figure 5.16 illustrates the RT-DIMR block diagram for one-phase. A detailed description of the different blocks of the three-phase RT-DIMR control strategy is given below.

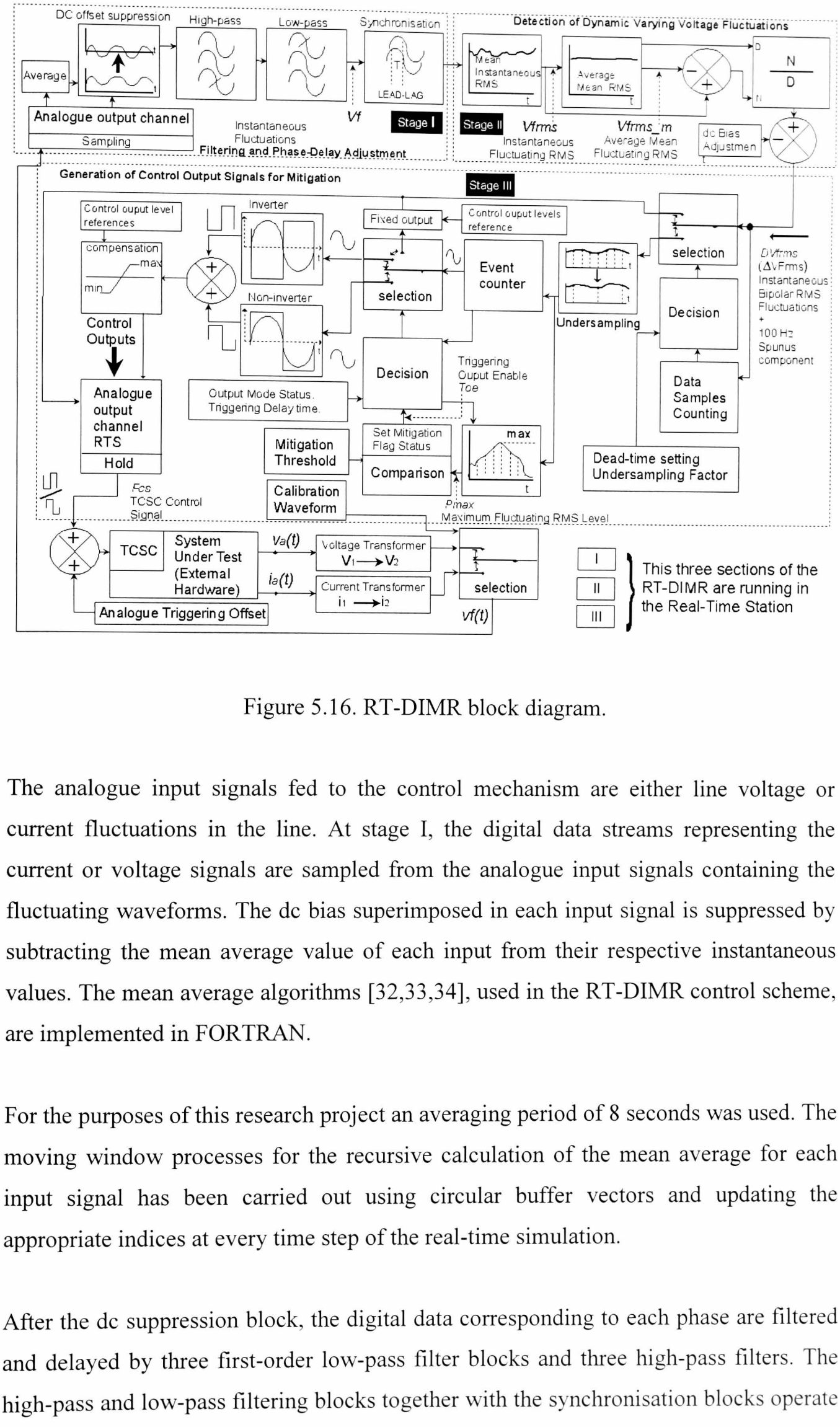


Figure 5.16. RT-DIMR block diagram.

The analogue input signals fed to the control mechanism are either line voltage or current fluctuations in the line. At stage I, the digital data streams representing the current or voltage signals are sampled from the analogue input signals containing the fluctuating waveforms. The dc bias superimposed in each input signal is suppressed by subtracting the mean average value of each input from their respective instantaneous values. The mean average algorithms [32,33,34], used in the RT-DIMR control scheme, are implemented in FORTRAN.

For the purposes of this research project an averaging period of 8 seconds was used. The moving window processes for the recursive calculation of the mean average for each input signal has been carried out using circular buffer vectors and updating the appropriate indices at every time step of the real-time simulation.

After the dc suppression block, the digital data corresponding to each phase are filtered and delayed by three first-order low-pass filter blocks and three high-pass filters. The high-pass and low-pass filtering blocks together with the synchronisation blocks operate

as band-pass filters and as a lead-lag function at the same time. The last block in the stage as lead-lag function at the same time. These blocks were implemented with conventional transfer functions provided by the EASY5 software.

At stage II, the mean rms fluctuating waveforms are profiled from the filtering block output processing the digital data, using an instantaneous rms algorithm. For this control strategy, the sample and first-derivative method [35], a sinusoidal-wave-based algorithm, was used as the best option to calculate the mean rms fluctuations instantaneously. Equations 5.1 to 5.8 detail the calculation procedure of the instantaneous rms fluctuations using the method.

The peak value of a sinusoidal-shaped waveform using the sample and first derivative is given by the following expression

$$F_{\text{peak}} = \sqrt{f(t)^2 + \frac{f'(t)^2}{\omega_0}} \qquad 5.1$$

The sampled function is

$$F_{\text{peak\_}n} = \sqrt{f(n\Delta T)^2 + \frac{f'(n\Delta T)^2}{\omega_0}} \qquad 5.2$$

and the first derivative is estimated from

$$f_k' = \frac{1}{\Delta T}\left(\nabla + \frac{1}{2}\nabla^2 + \frac{1}{3}\nabla^3 + ...\right) f_k; \quad f_k = f(n\Delta T)\big|_{n=k} \qquad 5.3$$

using only the first two terms of the series

$$f_k' \approx \frac{1}{\Delta T}\left(\nabla + \frac{1}{2}\nabla^2\right) f_k \qquad 5.4$$

where

$$\nabla f_k = f_k - f_{k-1} \qquad 5.5$$

$$\nabla^2 f_k = \nabla f_k - \nabla f_{k-1} \qquad 5.6$$

the approximate f_k derivative for this case is

$$f_k = \frac{1}{2\Delta T}(3f_k - 4f_{k-1} + f_{k-2}) \qquad 5.7$$

as a final step, the instantaneous rms is derived using equation 5.8

$$F_{\text{rms}} = \frac{F_{\text{peak\_}n}}{\sqrt{2}} \qquad 5.8$$

where

$f(t)$	sinusoidal waveform in time domain
f_k, f_{k-1}, f_{k-2}	values of $f(t)$ sampled at $n = k$, k-1, k-2 respectively. Notice that *k, k-1, and k-2* are consecutive samples with k being the current sample
$f_k^{'}$	first derivative of f_k
N	sample number
k	sample instant
ω_o	fundamental angular frequency of $f(t)$
ΔT	sampling time interval

The base algorithm to obtain $F_{\text{peak\_n}}$ is slightly modified by adding two cofactors in equation 5.1 in order to calibrate the final rms value and to further reduce the spurious ripple introduced in the rms during the ac-rms conversion action. The optimal cofactor values are finally determined after an iterative simulation-debugging procedure. In this stage $Vf_{\text{rms}} = F_{\text{peak\_n}}$ in Figure 5.16.

The rms can also be calculated using the well-known integral method given by equations 5.9 and 5.10, for continuous and discrete cases respectively [36,37,38].

$$F_{\text{RMS}} = \sqrt{\frac{1}{T}\int_T f^2(t)dt} \qquad 5.9$$

$T=2\pi/\omega_o$, where ω_o is the fundamental angular frequency

$$F_{\text{RMS}} = \sqrt{\frac{1}{N}\sum_{k=1}^{N} f(k\Delta T)} \qquad 5.10$$

where N is the window data length set in a cycle

ΔT is the sampling time interval

Although calculation of the mean rms fluctuations using the integration method is robust, accurate, and less sensitive to noise, it introduces two major disadvantages for the RT-DIMR. The first one is a frequency-dependent input-output time delay, lagging the fluctuating waveform. The second one is that an implicit averaging process is carried out producing an effective, but not desired, low-pass filtering action. These two disadvantages make the integration method unsuitable to capture the fast-changing rms fluctuations taking place in the system under test. The integration method is not used in this stage.

Further processing is required since the instantaneous mean fluctuating rms, Vf_{rms}, does not alternate in polarity, and are not normalised. Subsequently, Vf_{rms_m} is obtained by means of averaging Vf_{rms} using an 8 seconds window. In order to extract the ac fluctuating rms Vf_{rms_m} is compared with Vf_{rms}, and to normalise, the resulting signal is then divided by Vf_{rms_m}. As this resulting signal is dc biased, for adjustment purposes a correcting dc bias should be applied. At the end of this stage, the bipolar (ac) fluctuating rms waveform named DVf_{rms}, mixed with a spurious 100Hz ripple, is obtained.

At stage III, the 100Hz spurious ripple is removed using an under-sampling technique, with no additional delay time aggregated. For the purposes of the RT-DIMR, an under-sampling factor of 20 was selected. As the processing continues, the maximum instantaneous positive peak value of the fluctuating waveform is determined using a three sample algorithm.

The current maximum peak level is then compared against a pre-selected reference. When exceeded, the mitigation flag status is set active. A decision tree selects the appropriate control output based on the status of the mitigation flag, the pre-selected status of the output mode configuration, the triggering delay time, the reference to the control output levels and the polarity of the fluctuating waveform.

The output mode configuration, the triggering delay time and the output level reference settings indicate the control output whether or not a polarity inversion is to be applied, the minimum fixed delay time, and the maximum or minimum control output levels, respectively.

The generated digital three-phase control outputs are sent to the analogue output channels and from there to the system under test, closing the control loop and performing the hardware-in-the-loop-testing programme. The windowing vectors for rms and average algorithms are updated at the end of every simulation step.

The flow diagram shown in Figure 5.17 summarise the RT-DIMR operation previously described.

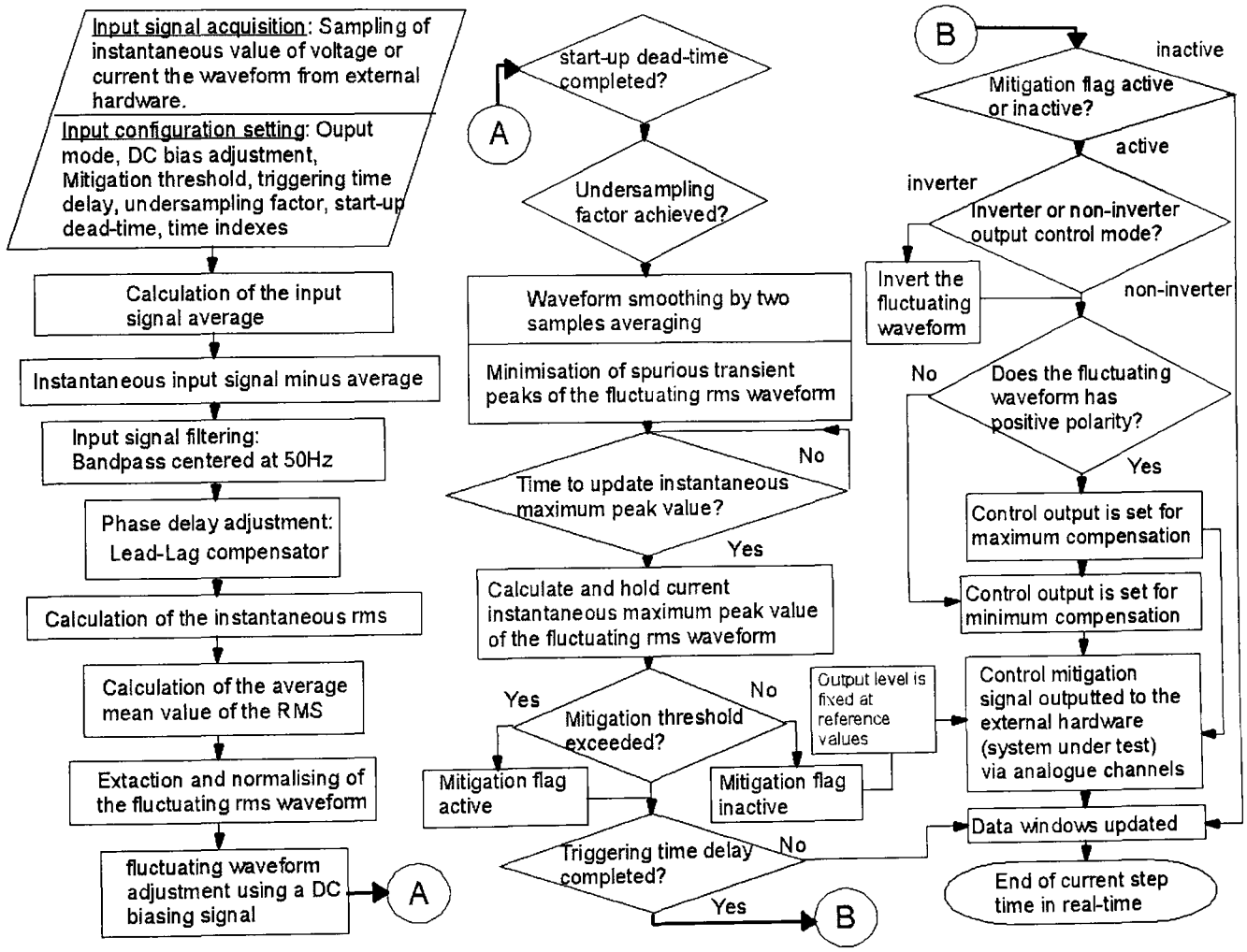


Figure 5.17. RT-DIMR Flow Diagram.

The real-time processing of the RT-DIMR control strategy is carried out at every single step time of the simulation. The Actual Frame Time (AFT) COSIM variable indicates the time the RTS used to complete one frame of calculations while the application is running. If the AFT is less than the pre-established time step, the simulation is running in real-time. The RT-DIMR control strategy was designed for a 500 μs step time. The average AFT in the simulation was 260 μs, fully confirming that the RT-DIMR operates in real-time.

The practical aspects of the physical implementation of realistic real-time hardware-in-the-loop testing imposes many challenges, which need solving for the real-time simulations to perform successfully, such as electrical noise interference, test system-RTS ground loops, three-phase system interconnection, operational range variations of the electronic systems due to temperature, a slight non-linear behaviour of the power inductors matching up the transmission lines, electrical safety, and the complex system interconnection reliability.

5.6 DIGITAL SIMULATIONS

The simulation results of the newly developed RT-DIMR control strategy are presented in this section. They are carried out in open-loop, non-real time using EASY5 software facilities. The dynamic capabilities of the control scheme are tested under different changing operating conditions. This enables the control strategy to be extensively tested prior to the RT-DIMR model is ready to drive the TCSC prototype as voltage fluctuation mitigation equipment.

In a three-phase system, the fluctuations of one phase voltage can be either synchronised or non-synchronised to the fluctuations of the other phases. The shape of the voltage fluctuations variations may not be exactly the same in each phase; the RT-DIMR can control each phase independently. As the voltage fluctuation in each phase might not be synchronised, the relative phase of each fluctuating rms may constantly change. The RT-DIMR control can manage this case by tracking down the rms fluctuations and sending the correspondent stream of triggering angle steps to the TCSC in response.

The RT-DIMR works with more than 20 internal parameters (variables and constant), three inputs from the electrical system and three outputs to the TCSC. Figures 5.18 to 5.27 present a selection of the most representative parameters. These are:

Instantaneous input fluctuating signals, $Vf(t)$: These are three input control signals connected, one per phase, to the electrical network. The signals can be either line voltages or currents.

Instantaneous fluctuating rms, $Vf_{rms}(t)$: This is set of three variables giving the rms values calculated from $Vf(t)$. These signals can be seen as dc signals with an ac ripple superimposed on them, where the ripple indicates the signal deviations.

Average mean fluctuation rms, $Vf_{rms\_m}(t)$: This set of internal variables is obtained by processing $Vf_{rms}(t)$ with an averaging algorithm. Ideally $Vf_{rms\_m}(t)$ should be a pure dc signal; however, some variations are usually noticed. The $Vf_{rms}(t)$ and $Vf_{rms\_m}(t)$ are used to calculate $DVf_{rms}(t)$.

Instantaneous bipolar rms fluctuations, $DVf_{rms}(t)$: These three variables represent the actual fluctuations of the line voltages or currents (the ripple of $Vf_{rms}(t)$).

TCSC control signals, $FCS(t)$: These are the output signals connected to the TCSC triggering modules. The $FCS(t)$ signals keep track of the variations of the $DVf_{rms}(t)$ signals. Each phase of TCSC is controlled individually by a single $FCS(t)$ signal.

Maximum fluctuating rms levels $P_{max}(t)$: These three variables indicate to the control the maximum fluctuating rms levels obtained from processing the instantaneous peak values of $DVf_{rms}(t)$.

Triggering output enabler $TOE(t)$: These internal control signals are used as reference to enable or disable the output of $FCS(t)$; if $TOE(t)$=1(0) then $FCS(t)$ is enabled (disabled). $TOE(t)$ results from comparing a reference against $P_{max}(t)$, if $P_{max}(t)$ exceed a limit then $TOE(t)$ =1.

Figures 5.18a, 5.18b and 5.19 present the RT-DIMR response to non-synchronised voltage fluctuations with different fluctuating frequency per phase. Figure 5.20 presents the RT-DIMR response to synchronised 10Hz voltage fluctuations but with different modulation in each phase.

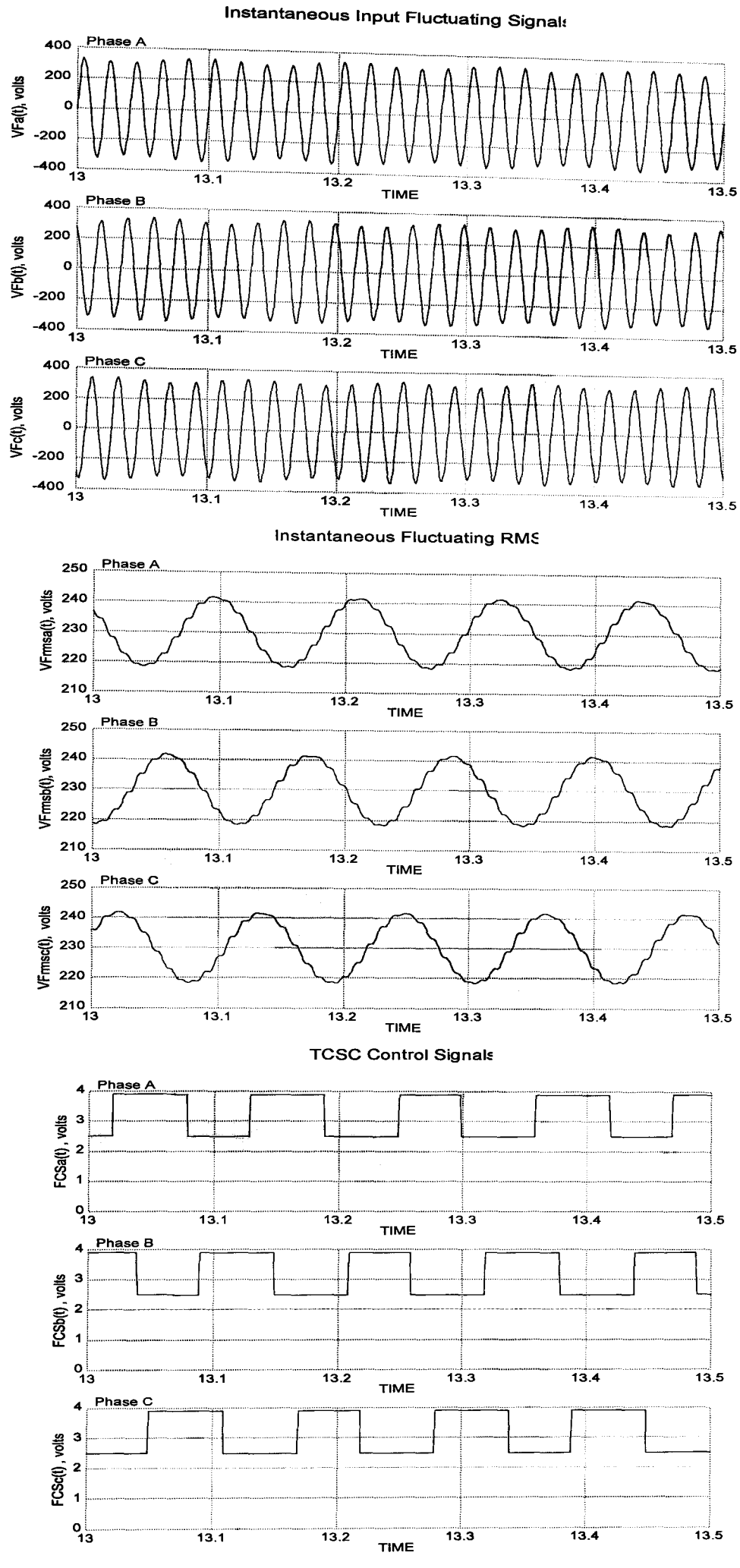


Figure 5.18a. RT-DIMR control response for non-synchronised sinusoidal voltage fluctuation fixed at 8.8 Hz and 5% modulation in each phase: i) instantaneous input; ii) instantaneous fluctuating rms; iii) TCSC control signals

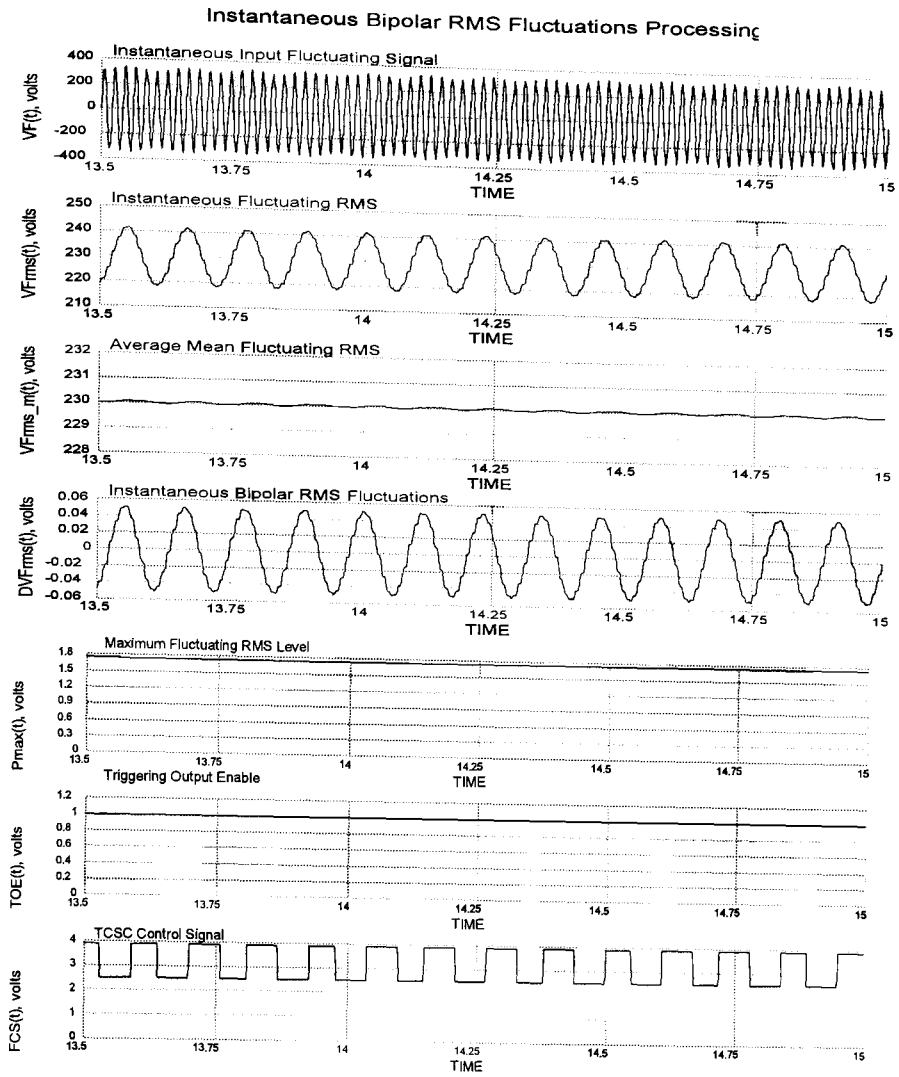
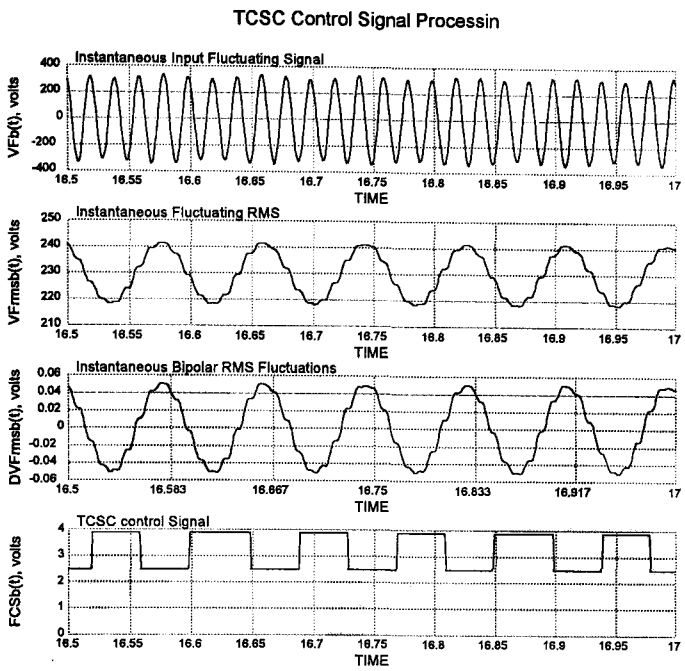
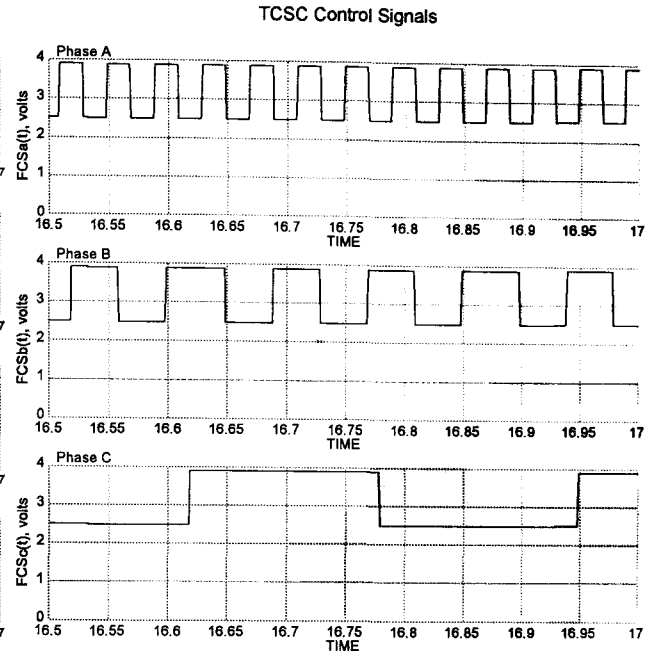


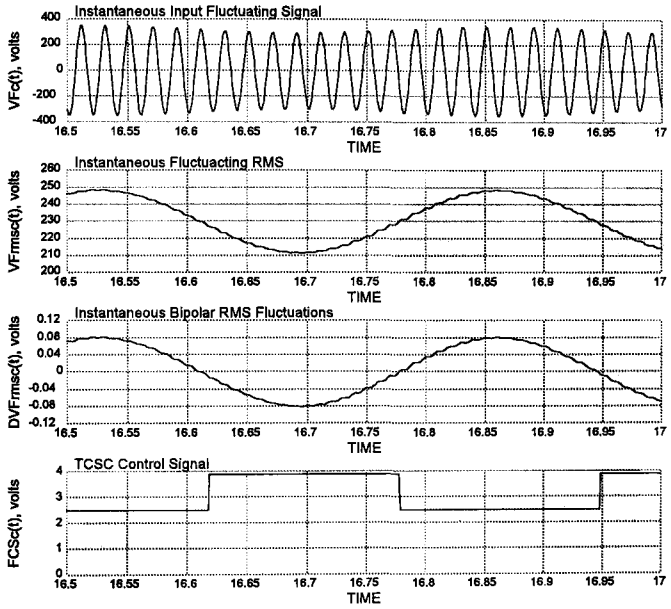
Figure 5.18b. RT-DIMR control response for non-synchronised sinusoidal voltage fluctuation fixed at 8.8 Hz and 5% amplitude modulation in each phase. Case of instantaneous rms fluctuations processing for phase A

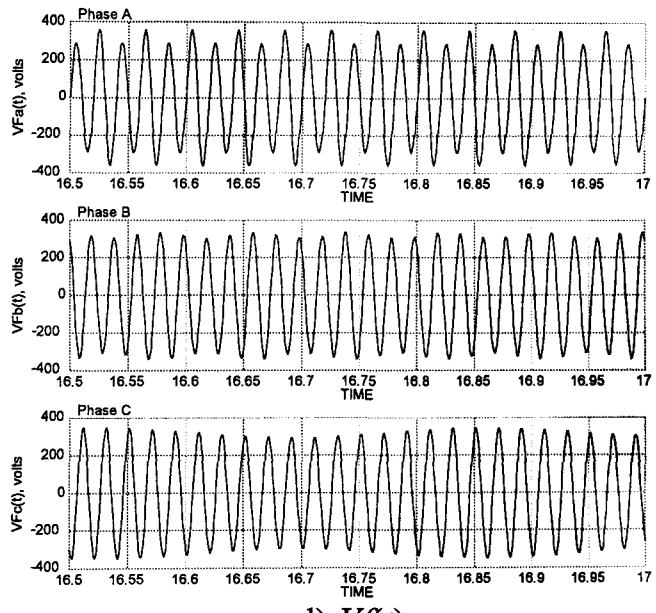
The waveforms in Figure 5.18a represent the three-phase inputs, outputs and internal variables. It should be noted that the zero-crossing of each phase in $FCS(t)$ is synchronised with the respective $Vf_{rms\_m}(t)$, and at the same time, the peak values of $Vf_{rms\_m}(t)$ are synchronised with the peak of $Vf(t)$. This is an indication of the fast response of the control strategy. The voltage fluctuations in $Vf(t)$, between phases, are not synchronised, as it is clearly indicated by the zero-crossing of $Vf_{rmsa}(t)$, $Vf_{rmsb}(t)$, and $Vf_{rmsc}(t)$. This shows the ability of the RT-DIMR to operate each phase independently. Figure 5.18b gives a closer look of the input-output processing of one phase. A key part of the control processing is to obtain $DVf_{rms}(t)$ from inputs $VF(t)$, which is carried out comparing $Vf_{rms}(t)$ against $Vf_{rms\_m}(t)$. The repetitive maximum peak level of $DVf_{rms}(t)$ is expressed in $P_{max}(t)$. At the final stage, $TOE(t)$ signals are enabled if $P_{max}(t)$ exceeds pre-selected maximum limits. When enabled, $FCS(t)$ switches between pre-selected maximum and minimum levels following the polarity of $DVf_{rms}(t)$. The $TOE(t)$ levels are normally set to trigger the TCSC prototype at maximum and minimum compensation with $TOE(t)$ at maximum and minimum levels, respectively. These results confirm the correct basic operation of the RT-DIMR control strategy.





a) phase B

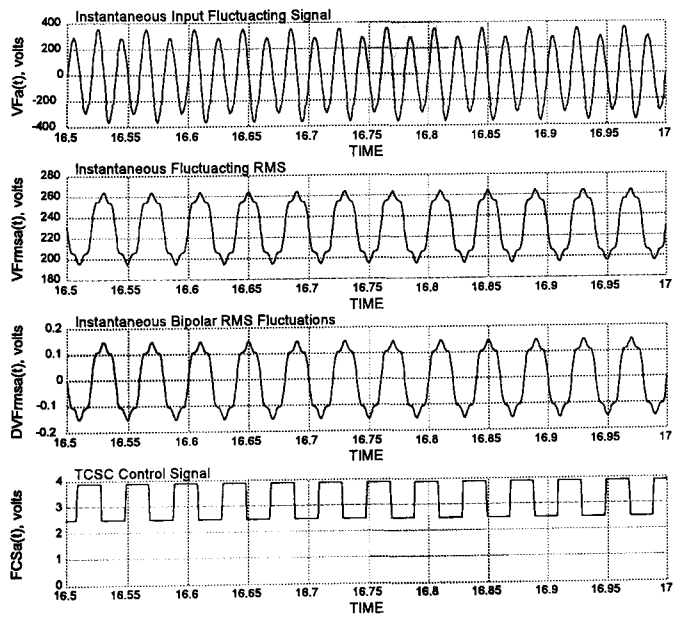


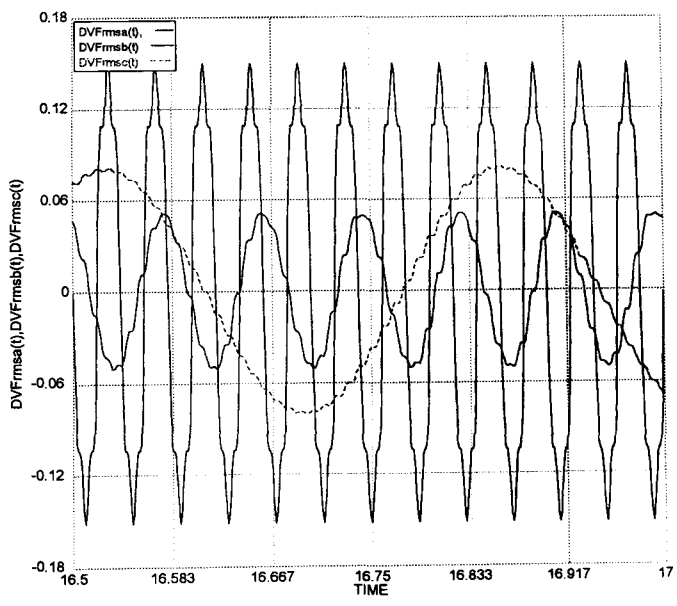


b) *FCS*(*t*)

c) phase C

d) *Vf*(*t*)

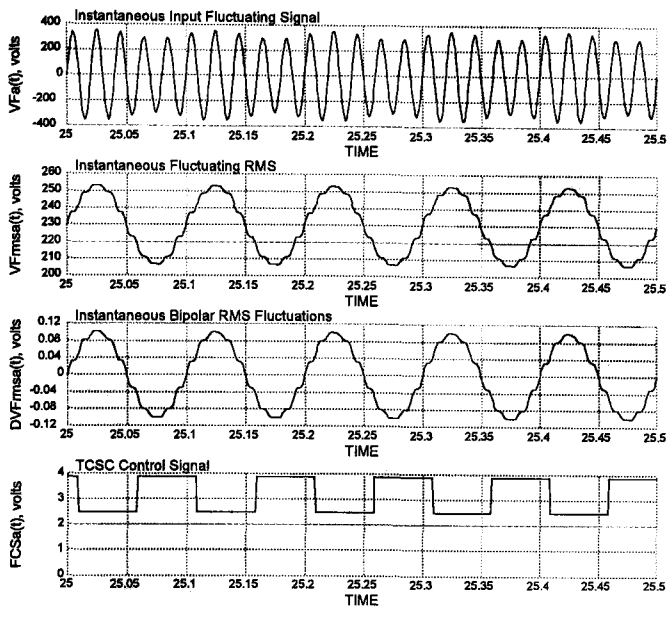




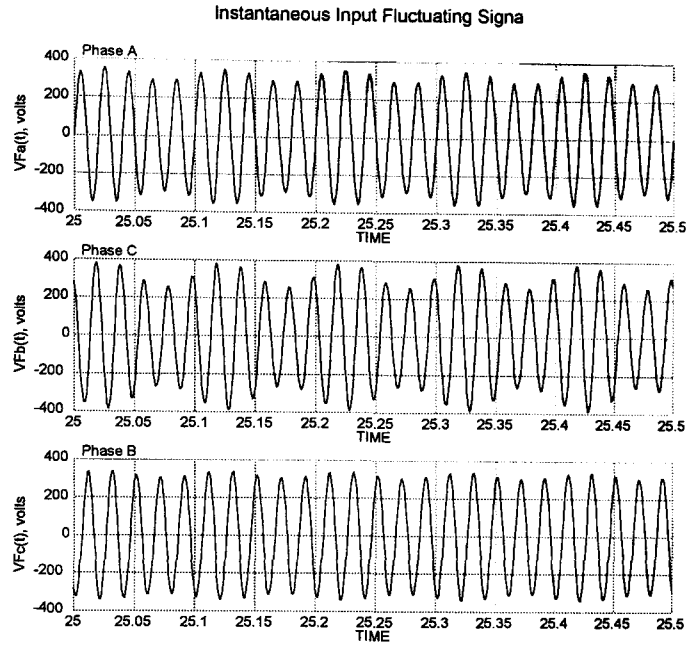
e) phase A

f) $DVf_{\text{rms}}(t)$

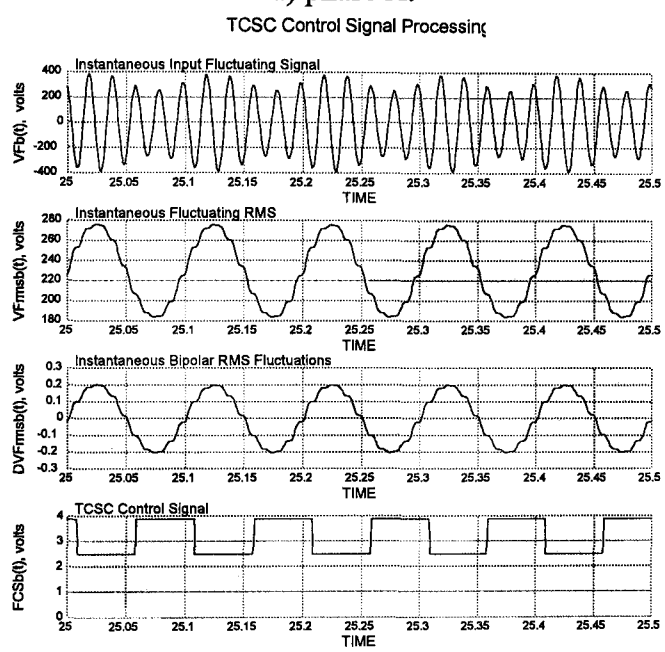
Figure 5.19. RT-DIMR control processing for non-synchronised sinusoidal input fluctuations. phase A: 25Hz and 15% modulation; phase B: 12Hz and 5% modulation; and phase c: 3Hz and 8% modulation



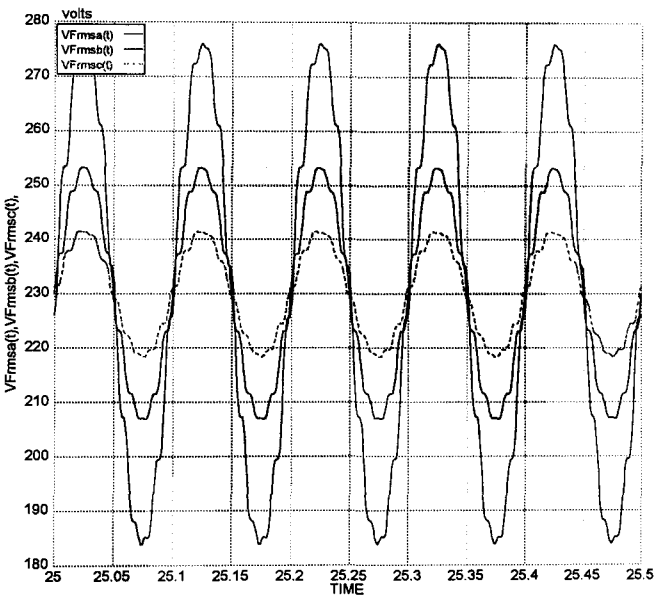
a) phase A.



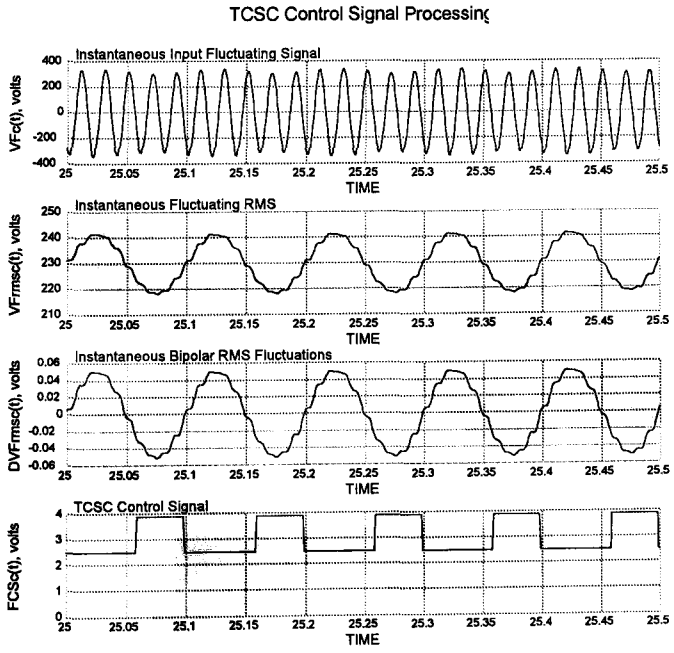
b) $Vf(t)$



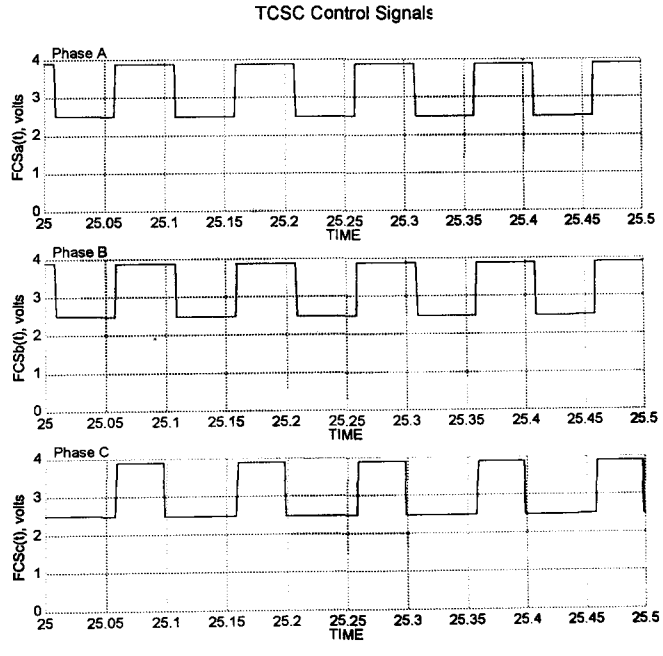
c) phase B



d) $Vf_{\text{rms}}(t)$



e) phase C



f) $FCS(t)$

Figure 5.20. RT-DIMR response to synchronised sinusoidal input fluctuations at 10Hz per phase for different modulation percentage

Figure 5.19 shows the input range of frequencies for the RT-DIMR control. $Vfa(t)$, $Vfb(t)$, and $Vfc(t)$ are independently processed, each having different fluctuating frequencies, 25 Hz, 12 Hz and 3 Hz, respectively.

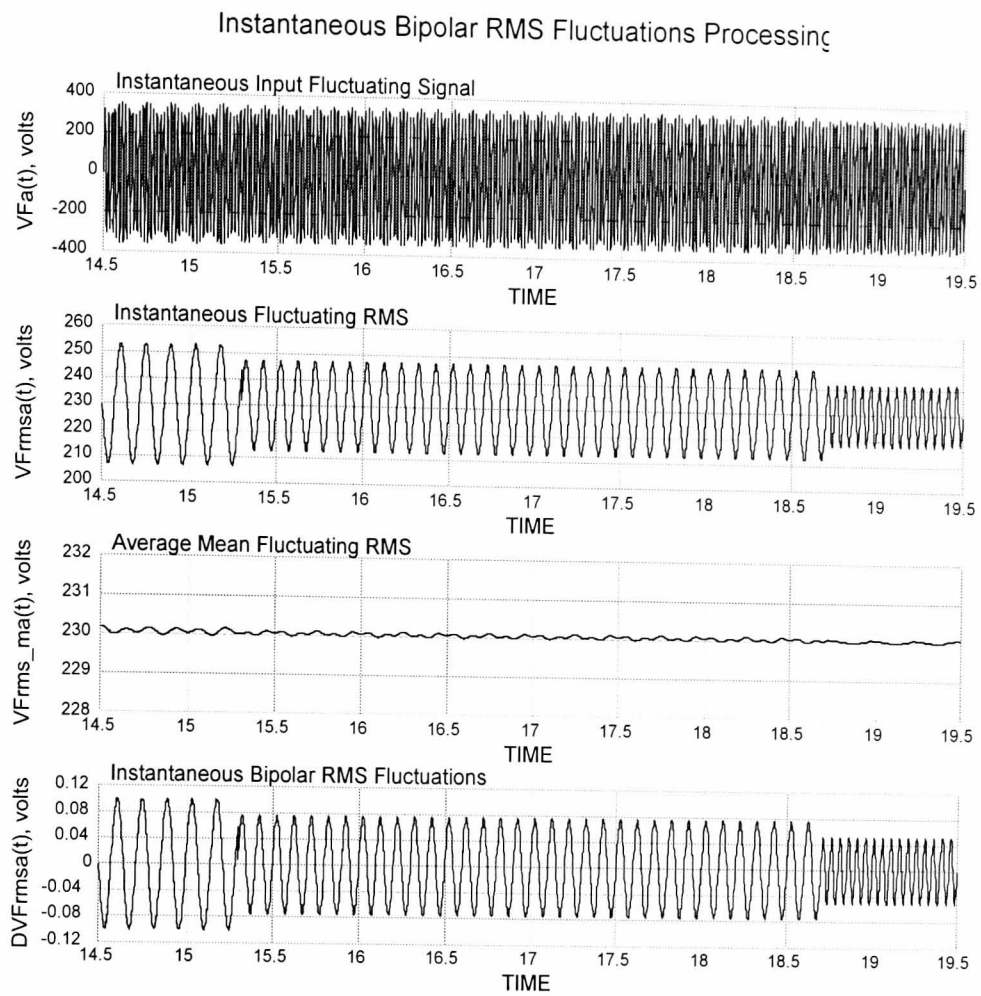
The input-output control processing per phase is illustrated in Figures 5.19a, 5.19c and 5.19e, which shows similarities with those in Figure 5.18b, indicating the repeatability of the control process. Figure 5.19f show waveforms of instantaneous bipolar rms fluctuations calculated from $Vf(t)$ inputs.

It is important to mention that the waveform distortion observed in Figures 5.19a, 5.19e and 5.19f is not due to control signals processing but to the lack of a signal reconstruction conditioning filter to pre-process the variables before visualisation.

The simulations in Figure 5.20 are similar to those presented in Figure 5.19. However, in the latter case the main purpose is to observe the control response to synchronised $Vf(t)$ inputs, at fixed frequency of the voltage fluctuations frequency. It should be noted that the change from synchronised to non-synchronised voltage fluctuations, or vice versa, is likely to occur in real networks, particularly if wind turbines are present. The waveforms in Figure 5.20d show the synchronisation between $Vf_{rmsa}(t)$, $Vf_{rmsb}(t)$, and $Vf_{rmsc}(t)$.

The RT-DIMR control strategy has been developed to enable the TCSC to mitigate voltage fluctuations in environments where the fluctuating signals continuously change in frequency and amplitude. Figure 5.21 illustrates the controller's response to voltage input signals with fluctuations varying in frequency and amplitude. The performance of the RT-DIMR for this case has been as good as expected to be.

Figures 5.22 and 5.23 show the RT-DIMR capability to act rapidly and independently with each phase, of the three-phase system, when operating under dynamic conditions. Additionally, other voltage fluctuation conditions are analysed. Figures 5.24 and 5.25 illustrate the RT-DIMR control performance when subjected to non-sinusoidal voltage fluctuations.



a)

b)

Figure 5.21a,b. RT-DIMR control response to sinusoidal input fluctuations varying between 7 Hz to 20Hz, with 5% to 10% amplitude modulation: a) instantaneous bipolar rms fluctuations processing; b) TCSC control signals processing

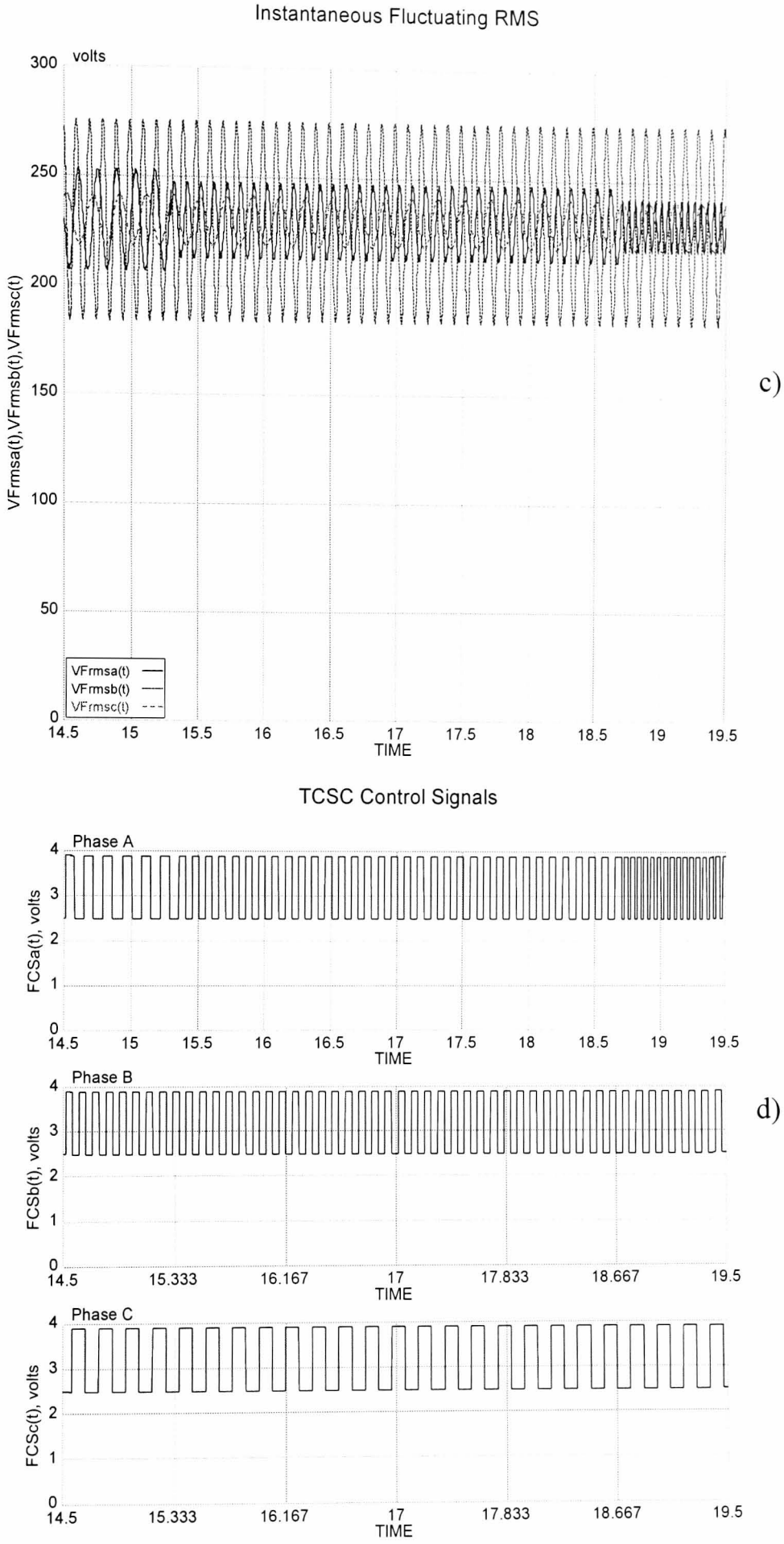
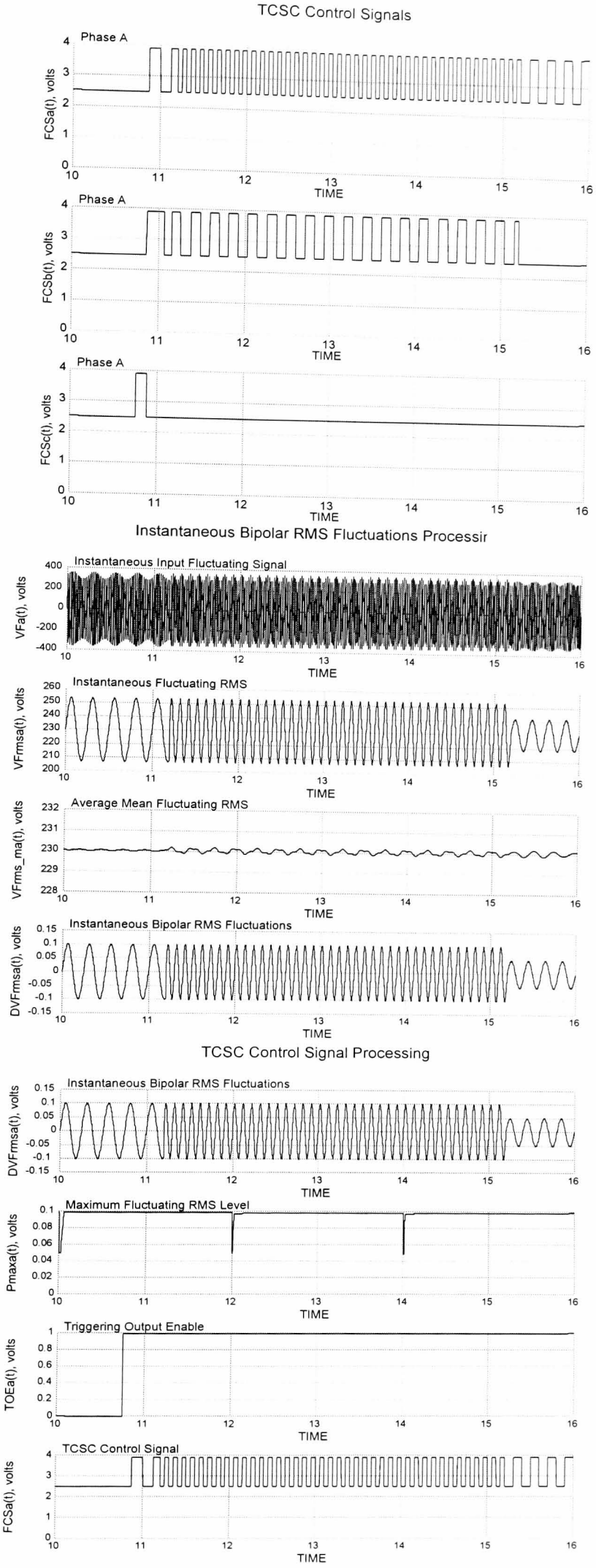


Figure 5.21c,d. RT-DIMR control response to sinusoidal input fluctuations varying between 7 Hz to 20Hz, with 5% to 10% amplitude modulation: c) instantaneous fluctuating rms; d) TCSC control signals



a)

b)

c)

Figure 5.22. RT-DIMR dynamic response to sinusoidal input fluctuation varying at different frequency in each phase: a) TCSC control signals; b) instantaneous bipolar rms fluctuations; c) TCSC control signal processing.

The set of waveforms shown in Figures 5.21 and 5.22 demonstrate the flexibility and fast response of dynamic adaptation of the output signals, $FCS(t)$, to the instantaneous fluctuating rms, $Vf_{rms}(t)$, varying in amplitude and frequency. The inter-relation between $FCS(t)$ and $Vf_{rms}(t)$ is shown in Figures 5.21c and 5.21d. In this case, the output signals $FCS_b(t)$, and $FCS_c(t)$ respond to input signals fluctuating at fixed frequencies (10 Hz and 5 Hz, respectively), and $FCS_a(t)$ responds to a varying fluctuating input.

The processing of $Vf_a(t)$ is shown in Figures 5.21a, 5.21b, and 5.22c. The amplitude and frequency of $Vf_a(t)$ are varied simultaneously, which show the capability of the RT-DIMR to rapidly process both changes together. In Figures 5.21a and 5.21b the range of changes are 7 Hz, 10 Hz and 20 Hz with 10%, 7% and 5% amplitude modulation, respectively. $FCS_a(t)$ effectively follows the fluctuations in all the three frequency changes, with no significant delay. $P_{maxa}(t)$ keeps track of the maximum peak level of $DVf_{rmsa}(t)$, updating its value every two seconds. The spikes at 16 s and 18 s in the waveform of $P_{max}(t)$, see Figure 5.21b, and those at 12 s and 14 s, see Figure 5.22c, indicate the updating points. $FCS(t)$ signals in Figure 5.22a keeps close track of the polarity of $DVf(t)$ variables, shown in Figure 5.22b, at all the fluctuating frequencies in the 0.5 – 25 range The RT-DIMR performance is quite satisfactory.

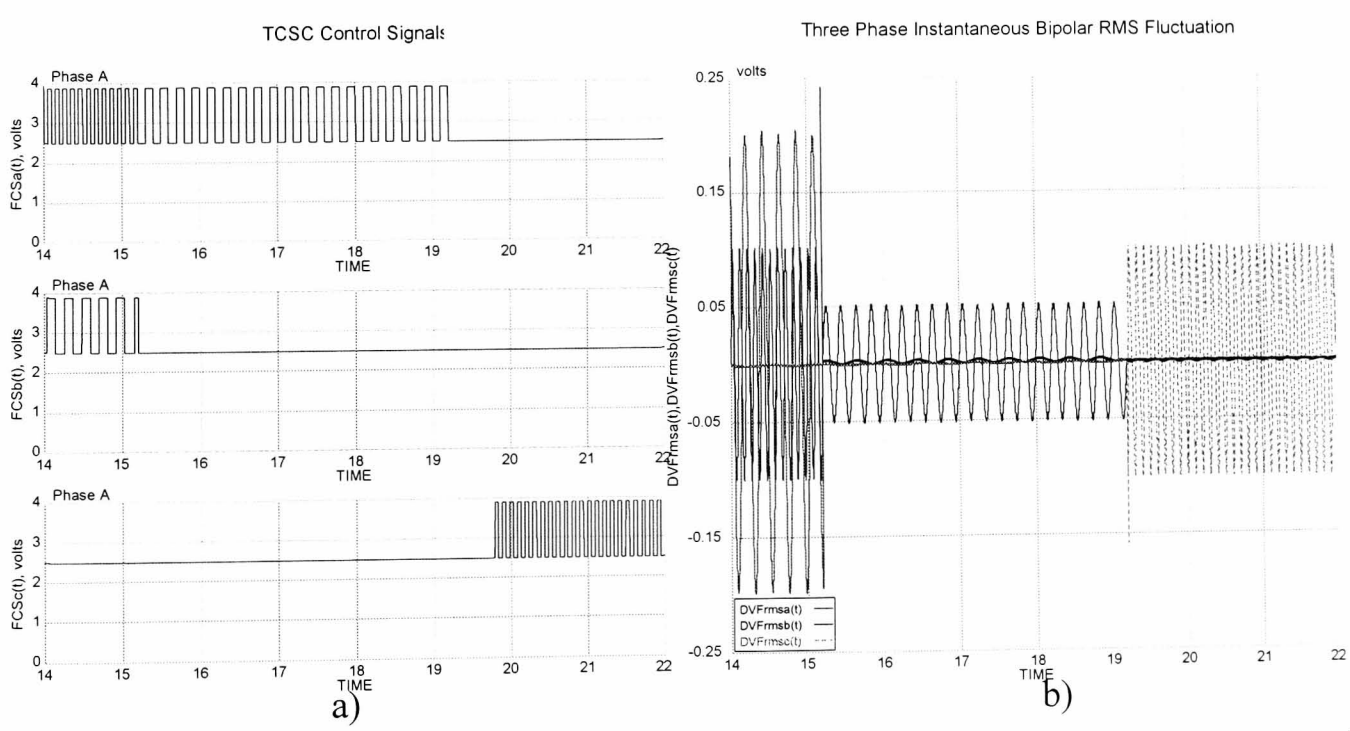


Figure 5.23. RT-DIMR response to fluctuations varying at different frequencies: a) TCSC control signals; b) instantaneous bipolar rms fluctuations

Figure 5.23 shows the case for input signal fluctuation, with each phase varying at different frequency. The RT-DIMR stop and resume mechanisms sent the controlling the signals to the TCSC with very little delay, no matter what the changes to the input are, it is evident by comparing the time scales of Figures 5.23a and 5.23b.

RT-DIMR control performance when subjected to non-sinusoidal voltage fluctuations is illustrated in Figures 5.24 and 5.25

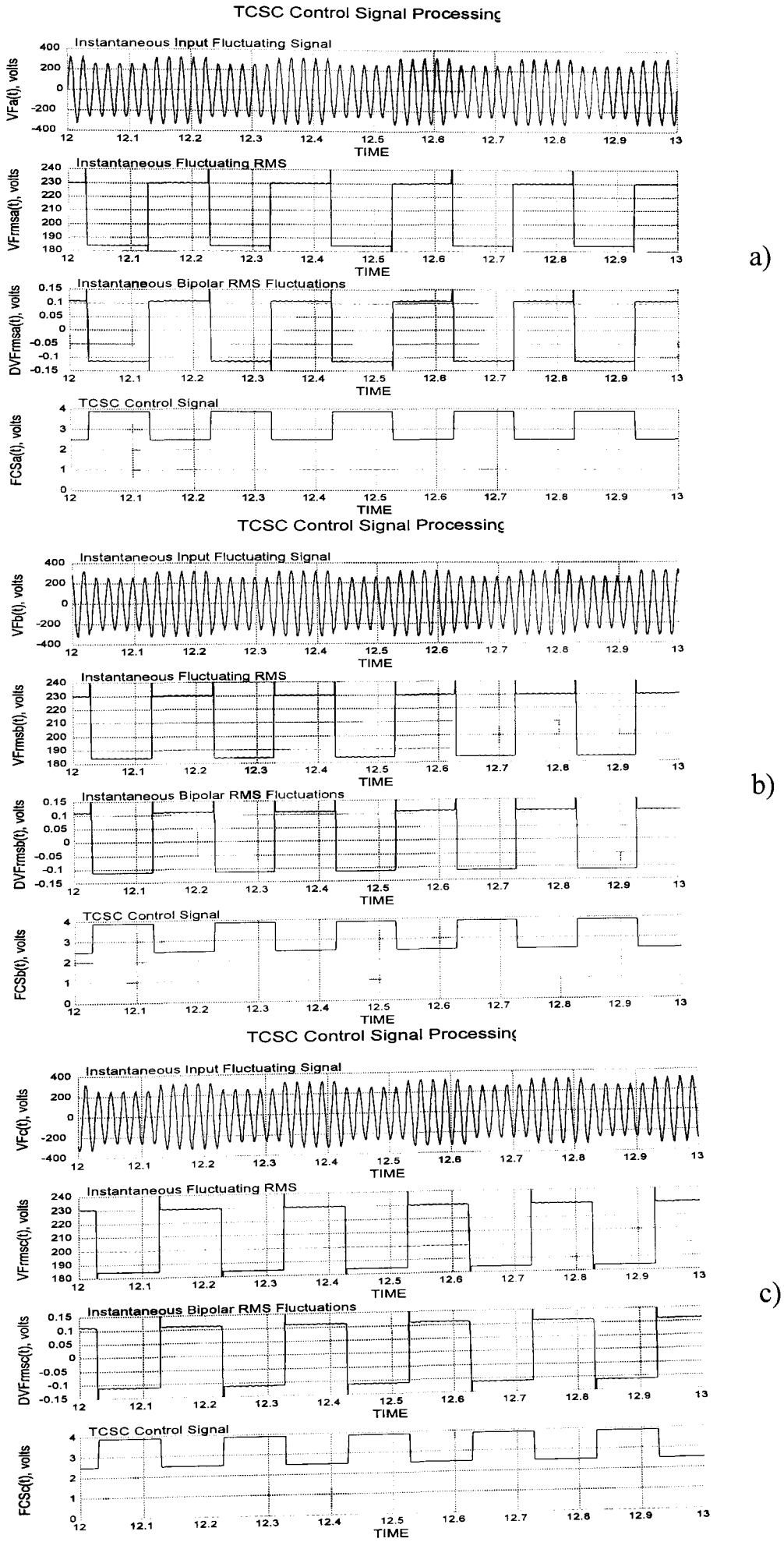


Figure 5.24. RT-DIMR response to fixed synchronised non-sinusoidal fluctuations at 10Hz with 10% amplitude modulation each phase: a) phase A processing; b) phase B processing; c) phase C processing.

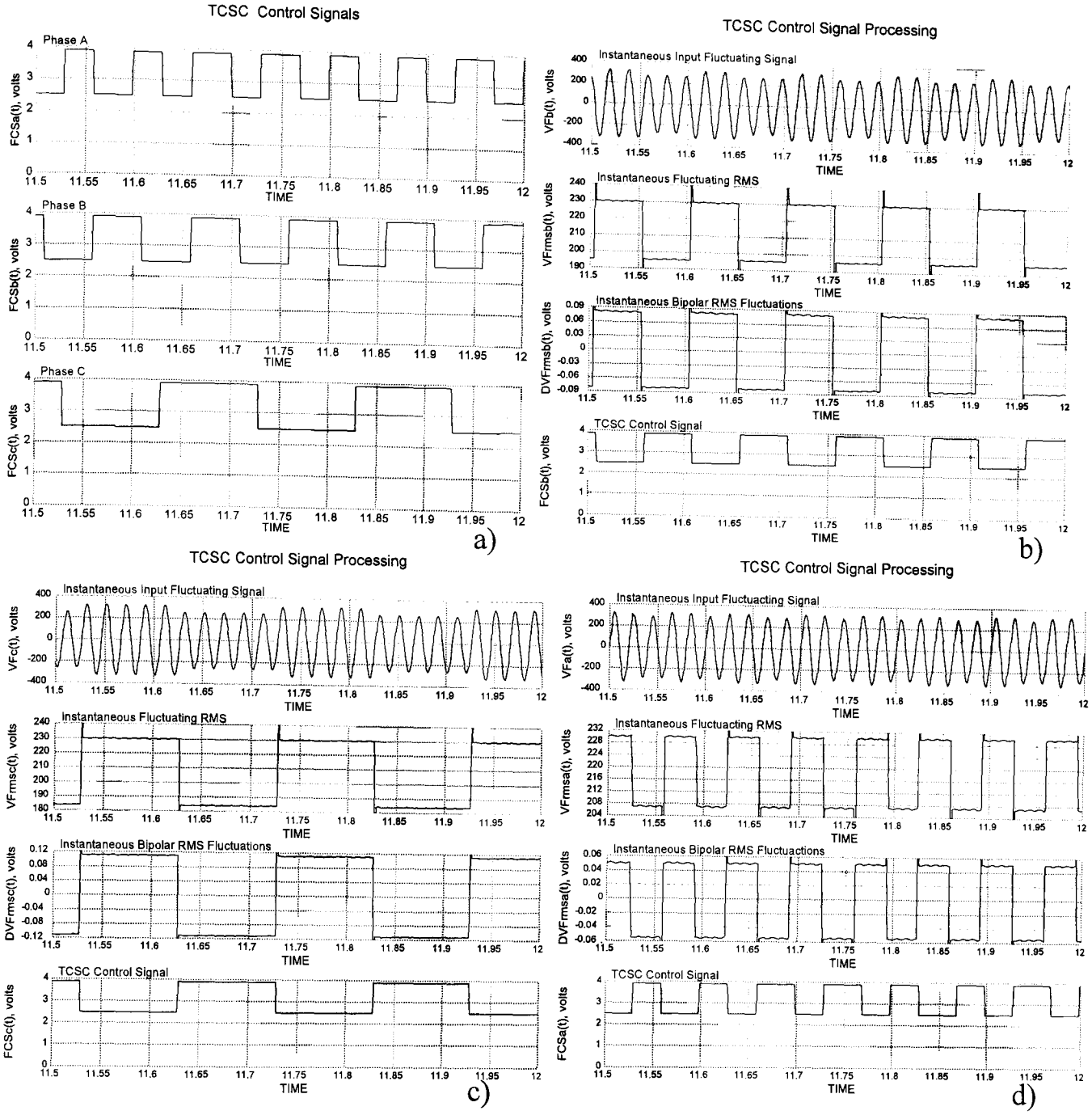


Figure 5.25. RT-DIMR control response to non-sinusoidal input fluctuations: a) TCSC control signals; b) phase A at 5Hz and 10% modulation; c) phase B at 10Hz and 7.5% modulation; d) phase C at 15Hz and 5% modulation.

The non-sinusoidal fluctuations are likely to occur in electrical networks and they are also the ones that challenge more the RT-DIMR control strategy. This is particularly true for rectangular fluctuations due to their wide harmonic spectra and usually sharp magnitude transitions, which can introduce some small deviations in calculating $DVf(t)$. Figure 5.24 presents the three-phase RT-DIMR input to output processing response to 10 Hz synchronised rectangular input fluctuations. As can be noticed in figures 5.24a 5.24b and 5.24c; $Vf_{rms}(t)$, $DVf(t)$, and $FCS(t)$ signals are fully-synchronised with the minimum and maximum instantaneous rms fluctuations of the input. The overshoots in

the waveforms of $Vf_{rms}(t)$ and $DVf(t)$ are due to the fact that the algorithm calculates rms quantities using numerical derivatives.

Figure 5.25 shows the RT-DIMR response to rectangular input fluctuations but considering different fluctuating frequency in each phase. Figure 5.25a details the output control signals and Figures 5.25b, 5.25c, and 5.25d give a closer look of the input-output control processing for phase a, b and c, respectively. This is a quite steep test for the RT-DIMR control, and it has been re-assuring to verify that also under this harsh test, the RT-DIMR performed very well.

The comprehensive simulations performed to evaluate the characteristics of the control strategy over a range of different conditions, fully shows that the RT-DIMR is well-suited to control the TCSC when mitigating voltage fluctuations is in practice. The RT-DIMR complies with the main characteristics detailed in Section 5.3.1.

5.7 CONCLUSIONS

This chapter has presented the design and implementation of the newly developed Real-Time Dynamic Instantaneous Mitigation Response (RT-DIMR) control strategy, which serves the purposes of mitigating the voltage fluctuation propagating in electrical systems. The core of the RT-DIMR is the instantaneous voltage fluctuation-tracking algorithm, which follows the fluctuating rms variations of an abnormal voltage waveform. The design aspects and implementation of the control strategy structure is fully described and detailed throughout this chapter. Extensive digital simulations show the dynamic flexibility of the RT-DIMR operating under several varying voltage fluctuating conditions, responding very well in the 0 – 25 frequency range with both sinusoidal and rectangular fluctuations.

The RT-DIMR has been designed to be an important element of the TCSC mitigation strategy to counteract voltage fluctuations with success.

This chapter also addresses traditional aspects of power system dynamics such as power oscillations and subsynchronous resonance phenomena, with emphasis on control strategies for the TCSC. The basic concepts, theory and models of the damping of power oscillations, the mitigation of subsynchronous resonance and the current flow

regulation in steady state, is addressed in some detail. The control philosophy and basic models for the TCSC are reviewed and three control schemes are presented to counteract these network conditions.

A good control background leads to a better understanding of voltage fluctuations mitigation using the TCSC. This chapter includes a brief description of the software tools used to develop the real-time control application for this research work.

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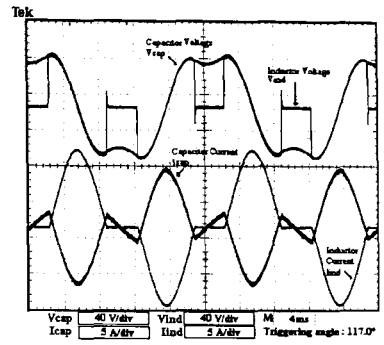
CHAPTER

6



SCALED-DOWN TCSC PROTOTYPE AND TESTING ENVIRONMENT: EXPERIMENTAL PERFORMANCE EVALUATION UNDER STEADY-STATE, DYNAMIC AND NON-CHARACTERIC CONDITIONS

6.1 INTRODUCTION

Experimental investigations on TCSC current and voltage waveforms for conditions other than steady-state are not commonly found in the open literature. Accordingly, an intimate experimental knowledge of TCSC behaviour under small signal, abnormal and non-characteristic conditions is a most after sought development.

The design and construction of a scaled-down TCSC prototype and electrical network, together with its testing environment, is a challenging and costly enterprise, requiring highly developed technical abilities in order to solve the many problems that arise even before the system is ready to operate. Nevertheless, a closer understanding of the TCSC particularities should bring new technological concepts and great many benefits to the power engineering community.

This chapter presents the experimental results of the TCSC prototype operating under steady-state, dynamic, transitory and non-characteristic system conditions in order further understand key characteristics of the controller's response. In all these cases, the TCSC has been tested in open-loop conditions.

The TCSC and the scaled-down electrical system are fully protected. In particular the TCSC thyristor modules are protected with fuses and the triggering module (which includes snubber circuits). It is also important to mention that the TCSC prototype has been over-designed, in terms of current ratings. As example, the TCSC thyristor modules were selected for 50 A, more than 30 times higher than the nominal current used in the experiments. On purpose, the controller has not been provided with overvoltage protection (MOV and breakers) and the overcurrent protection has been modified to allow the TCSC operation even when high surge currents are present.

The lack of overvoltage protections would allow investigations of the TCSC behaviour under conditions that cannot be easily observed in a full-scale TCSC, mainly because of operation of its protection system, the actual current and voltage ratings of its power devices (which could be damaged while testing) and potential problems in the network if overcompensation or resonance occurs.

6.2 EXPERIMENTAL REAL-TIME TESTING ENVIRONMENT

A real-time testing environment, which includes a scaled-down transmission system and accurate measurement equipments, has been developed in this research project to provide an advanced tool for realistic hardware-in-the-loop experimentation. The implementation of this environment requires the application of stringent electrical safety regulations.

For the purpose of this research project, the testing environment is divided into five main areas namely power signal conditioning, electrical system under test, electronic instrumentation system, protection system and real-time computing platform. The instrumentation and protection systems are transparent to the electrical system under test. Figure 6.1 shows the one-line real-time testing environment, in block diagram form. A brief description of the main blocks is given blow:

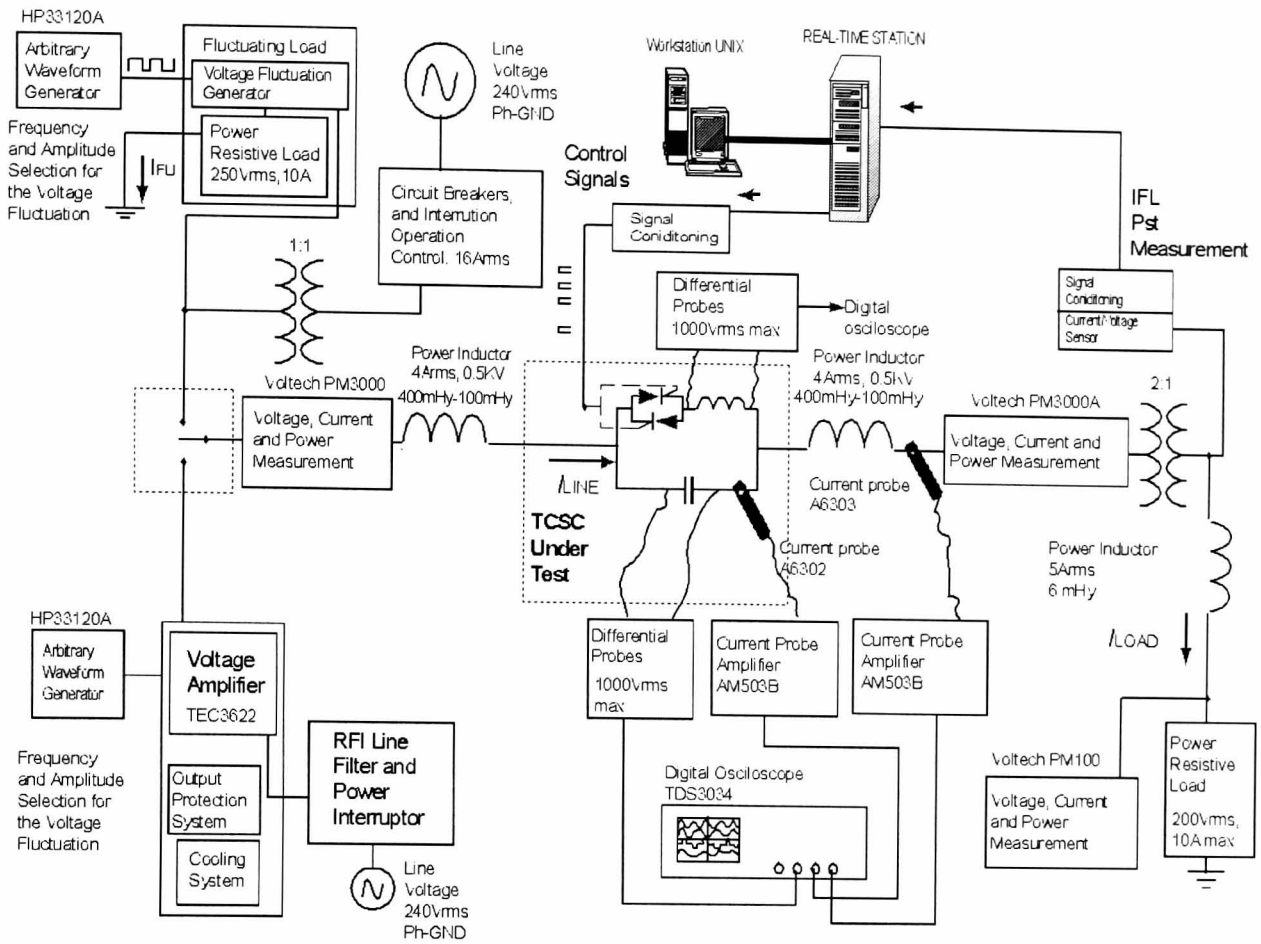


Figure 6.1. Experimental real-time testing environment: block diagram

Power Signal Conditioning: This system generates controlled electrical conditions to mimic realistic abnormal phenomena occurring in full-scale electrical networks. The sinusoidal voltage fluctuation fed to the electrical system under test is a small-signal output boosted by a set of three voltage amplifiers at varying amplitudes (maximum 20%) and fluctuation frequencies (maximum 25Hz) in order to re-create the sinusoidal voltage fluctuation phenomenon. On the other hand, a tailor-made non-sinusoidal current fluctuation conditioner, a power resistive load, and a set of transformers are capable of mimicking a non-sinusoidal fluctuating load and perturbing the electrical system under test with step voltage fluctuation at frequencies of up to 25Hz. In both cases the P_{st} level can be dynamically changed at any moment of the experiment run-time to observe the equipment's control and measurement responses.

The voltage amplifiers set consist of three single-phase TECHRON TEC3622 voltage amplification units with a maximum power rating of 125V@5A over a frequency bandwidth from dc to 50 kHz. These amplifiers are mounted into a 19" industrial

enclosure where a 4 cubic meter per minute cooling system is installed. The non-sinusoidal current fluctuation conditioner is a triac-based module developed to operate as a fast current interrupter.

The power signal conditioning system includes a manually controlled short-circuit generator module, based on fast relays, to produce three-phase, phase-to-phase and phase-to-ground fault conditions, although this was primarily intended to test the transformer's regulation margin.

Electrical System under Test: This system comprises two main components, the TCSC controller and support system, and the external passive power components, respectively. Two sets of three-phase 100/200/400mH power inductors rated at 3.5 A at 50 Hz play the role of three-phase power lines. The external passive power components comprise also three sets, 5kVA, 1kVA and 750kV, of three-phase transformer and a power resistive load. The scaled-down TCSC prototype is series connected with the power inductors. The TCSC controller and its support circuitry have already been explained in previous chapters.

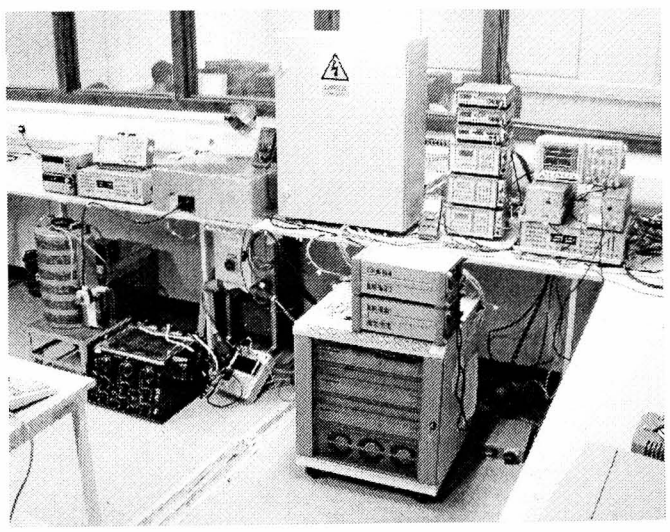
Instrumentation System: A multi-point measurement system for measuring currents and voltages, with each system node being monitored, provides a rich source of very useful information. For this research work, the multi-point measurement is made up of six PM100 single-phase and two three-phase PM3000/PM3000A power analysers, and six digital multi-meters. Two differential voltage and two high-precision current probes are used to measure voltages and currents at different points of the electrical system. The output signals from the probes are sent to the Tektronix TDS3034 digital oscilloscope (300 MHz Bandwidth-2.5GS/s) for visualisation, post-processing and storage.

Protection System: This system comprises a circuit breaker and a RFI line filter with power interrupter. The three-phase circuit breaker is series connected to safely interrupt the energy flow if an overcurrent occurs or the emergency stop button is pressed. A set of fuses and a contactor are the main elements of this module. An additional overcurrent protection and a set of fuses have also been installed in the TCSC-LC circuit, connected in series with the inductor.

Electromagnetic interference can be harmful to both the equipment that produces it and to other equipments used in the experiment. To minimise such a threat a three-phase RFI line filter with a power interrupter module has been developed with two main

purposes in mind: a) to prevent an overloading condition when the amplifiers are turned-on; b) to suppress the amplifiers RFI emission to the supplying 420 V electrical system, particularly those circulating in the voltage amplifiers inputs to RTS analogue channels ground-loop. The former avoids a destructive overvoltage situation damaging the RTS when the amplifiers are turned-off. Additional protection is required for the amplifiers power outputs as destructive overvoltages in the turned-on/turned-off process can occur.

Real time Computing Platform: An industry standard RTS is used to carry out the digital real-time simulations and to interact with the external equipment. The RTS characteristics will be explained in detail in Chapter 7. Figures 6.2 and 6.3 show the real-time testing environment.



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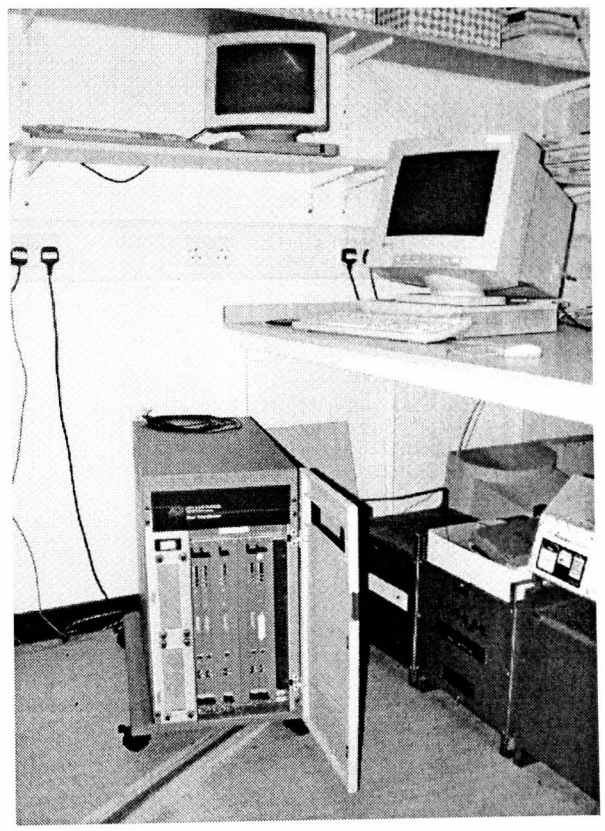

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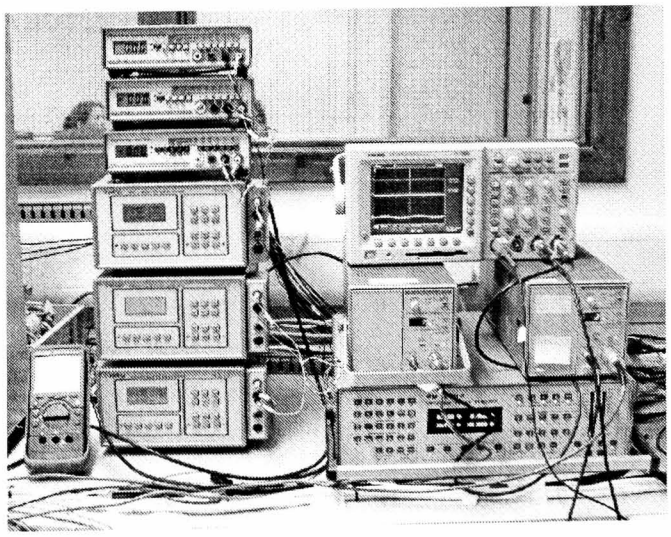

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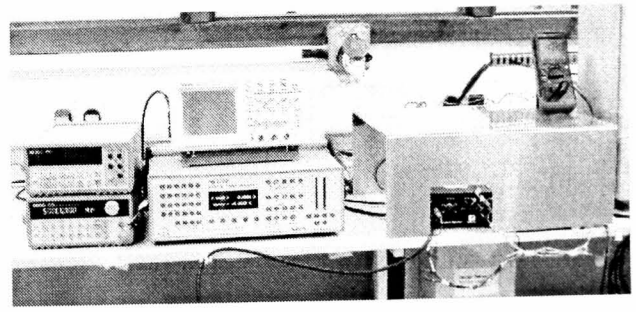
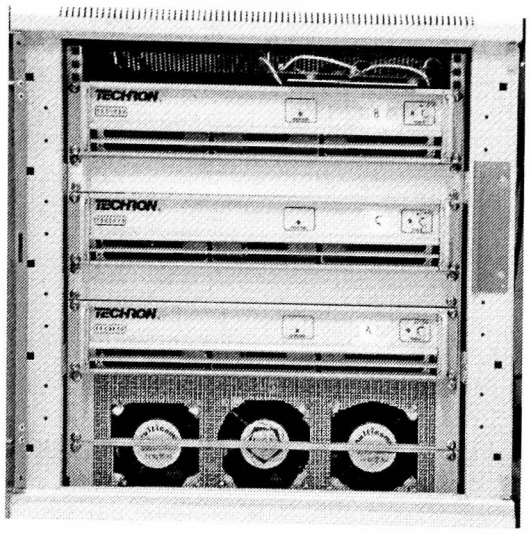


d)

Figure 6.2. Real-time testing environment: a) general overview; b) RTS and display; c) instrumentation system part 1; d) instrumentation system part 2



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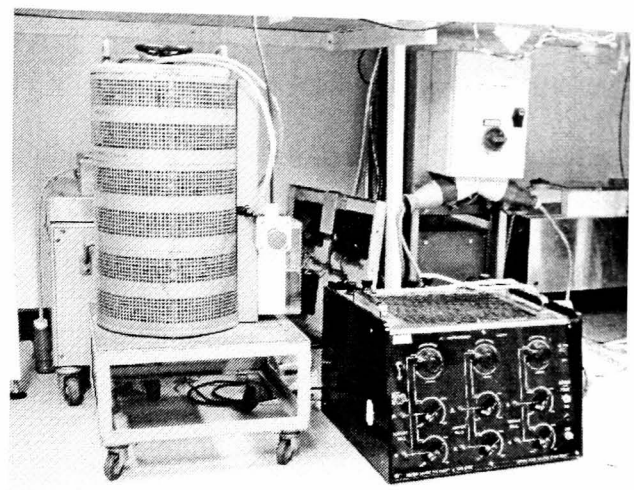

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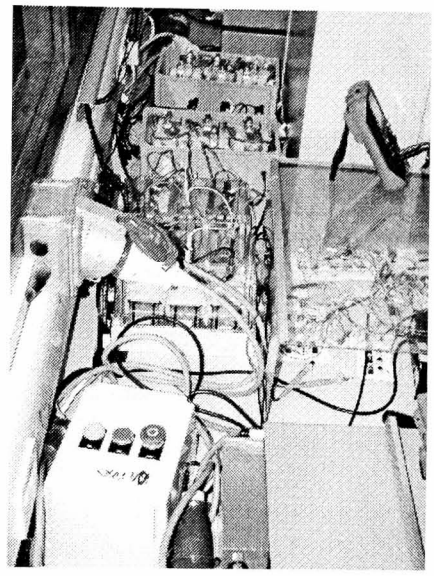


c)

Figure 6.3. Real-time testing environment: a) voltage amplifiers set; b) autotransformer, transformer set and power resistive load; c) power inductors and protective circuit breaker

6.3 EXPERIMENTAL CHARACTERISATION OF THE SCALED-DOWN TCSC PROTOTYPE

6.3.1 Steady-State Conditions

The TCSC is triggered at the time when the voltage and current through its capacitor are opposite in polarity, hence, there are two common triggering waveform references which can be used to operate the controller. For the purposes of the present research work these reference signals have been termed voltage triggering reference (VTR) and current triggering reference (CTR), respectively.

The triggering angle can be determined by using either the CTR or VTR or, alternatively, by using a combination of both. The TCSC prototype can be reconfigured, before the experiment starts, to make use of the CTR or VTR, depending on the type of experiment. As a common practice, the line current and the capacitor voltage of the TCSC-LC are used as CTR and VTR, respectively.

The fundamental resonance mode divides quite naturally the TCSC inductive and capacitive reactance operating regions. For steady-state purposes, the capacitive operating region is by far the main TCSC region employed.

The VTR or the CTR can be used for the entire capacitive region, with the TCSC showing no discernable difference in performance. Conversely, if the TCSC inductive region is used, which actually offers a very restrictive operating band, the use of VRT appears to be the only option. In fact, the TCSC prototype cannot operate in an apparent inductive reactance mode when the CTR is used. Two main reasons emerges to explain such anomaly: i) contrary to the capacitor voltage polarity, the line current has not polarity inversion when changing between operating regions, capacitive to inductive or vice-versa; ii) in the 90° to 180° and 270° to 360° zones, the capacitor voltage and the line current have the same polarity when the TCSC operates in the inductive region. To be able to operate, it would be necessitate a forced change of the triggering sequence of the thyristor pair if the line current were to be selected. Furthermore, if the CTR option is selected to use the TCSC capacitive region, the phase of the current line should be delayed by 180° in order to synchronise the triggering of the forward-looking thyristor of the controller with the 0 – 90° region of the current, preserving also the thyristor triggering sequence required when the VTR is used.

Figures 6.4 presents experimental voltage and current waveforms for the case when the TCSC operates in its capacitive region, at three different triggering angles. It should be noticed that the capacitor voltage waveforms and line current magnitudes in Figures 6.4a and 6.4b show no significant difference between them, which is in contrast to the signals shown in Figure 6.4c, even though the triggering angle difference of the waveform shown in Figures 6.4b and 6.4c is only 2.1°, as opposed to 7.7°. Figures 6.4a, 6.4b and 6.4c show the smooth operating behaviour of the TCSC, with Figure 6.4c also indicating that the operation of the controllers is moving towards the fundamental resonance mode, which takes place at α=135°.

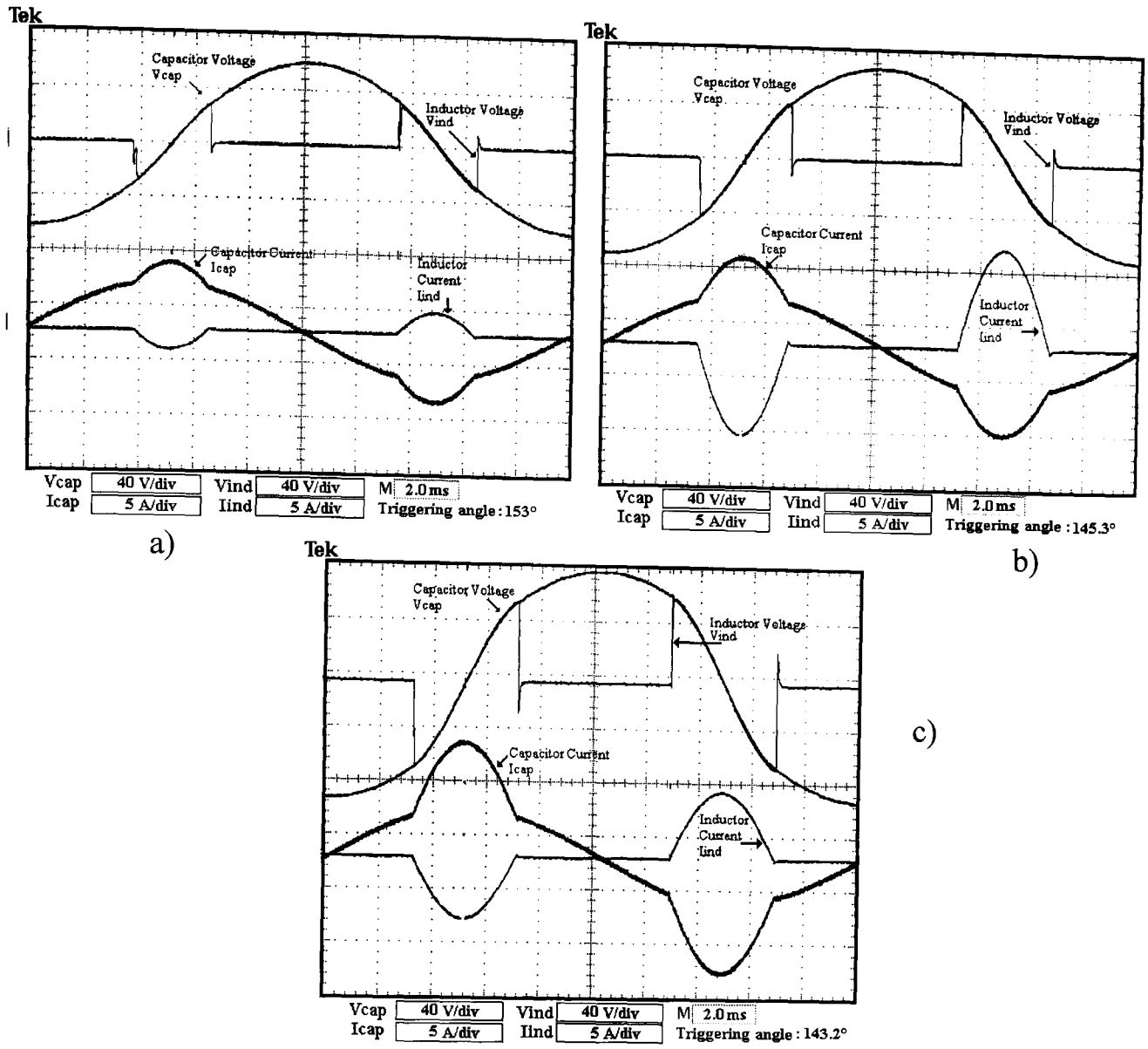
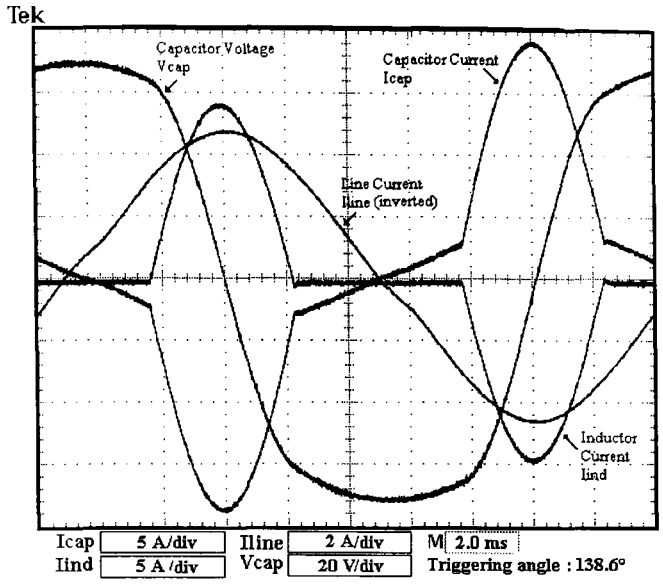


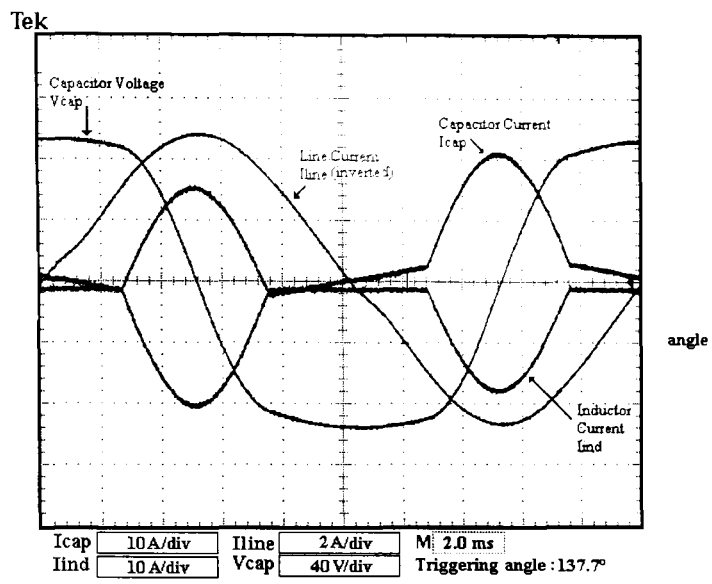
Figure 6.4. TCSC capacitive region waveforms at steady-state: a) α=153°; b) α=145.3°; c) α=143.2°

Figures 6.5 shows the TCSC behaviour when the triggering angle approaches the fundamental resonance mode. It can be noticed that the shorter the triggering angle the greater the distortion of the inductor and capacitor currents at the capacitor voltage zero-crossing point.

The inductive steady state response of the TCSC is presented in Figure 6.6. Similarly, Figure 6.7 shows the voltages and currents for triggering angles closely approaching the fundamental resonance mode. The triggering angle difference between Figure 6.6a (close to the intrinsic hidden resonance mode) and Figure 6.7b (close to the fundamental resonance mode) is very narrow (8°), showing the limited operational margin of the TCSC's inductive region and the difficulties incurring in operating the controller, in a swapping fashion, between the its capacitive and inductive regions. The reader should also appreciate the similarities between the inductor currents in Figures 6.5d and 6.7b, which give an indication of TCSC operation approaching to the fundamental resonance.



a)



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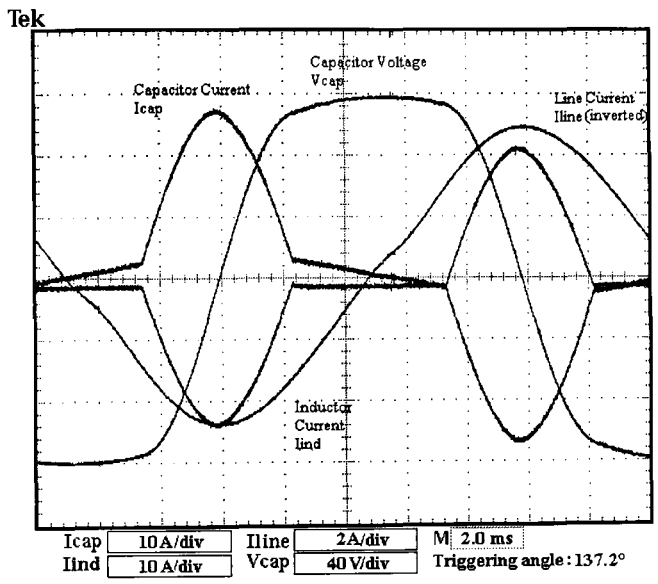

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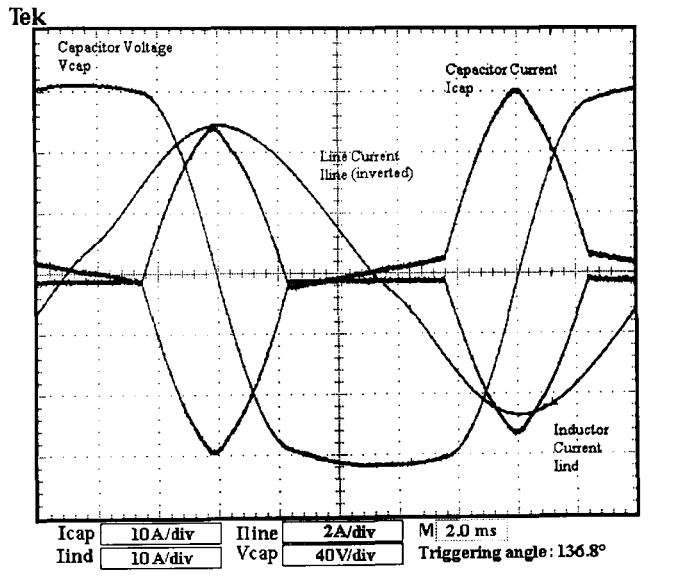
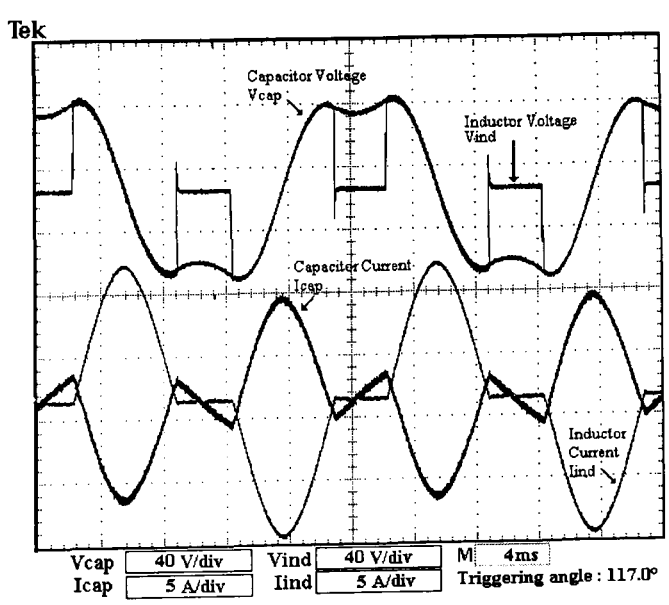
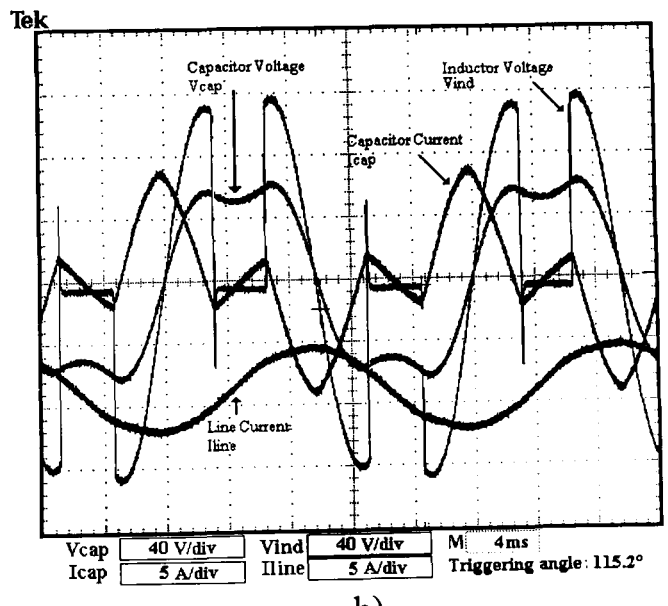


d)

Figure 6.5. TCSC voltage and current waveforms close to the fundamental resonance mode: a) α=138.6°; b) α=137.7°; c) α=137.2°; d) α=136.8°



a)



b)

Figure 6.6. TCSC waveforms in the inductive region I: a) α=117°; b) α=115.2°

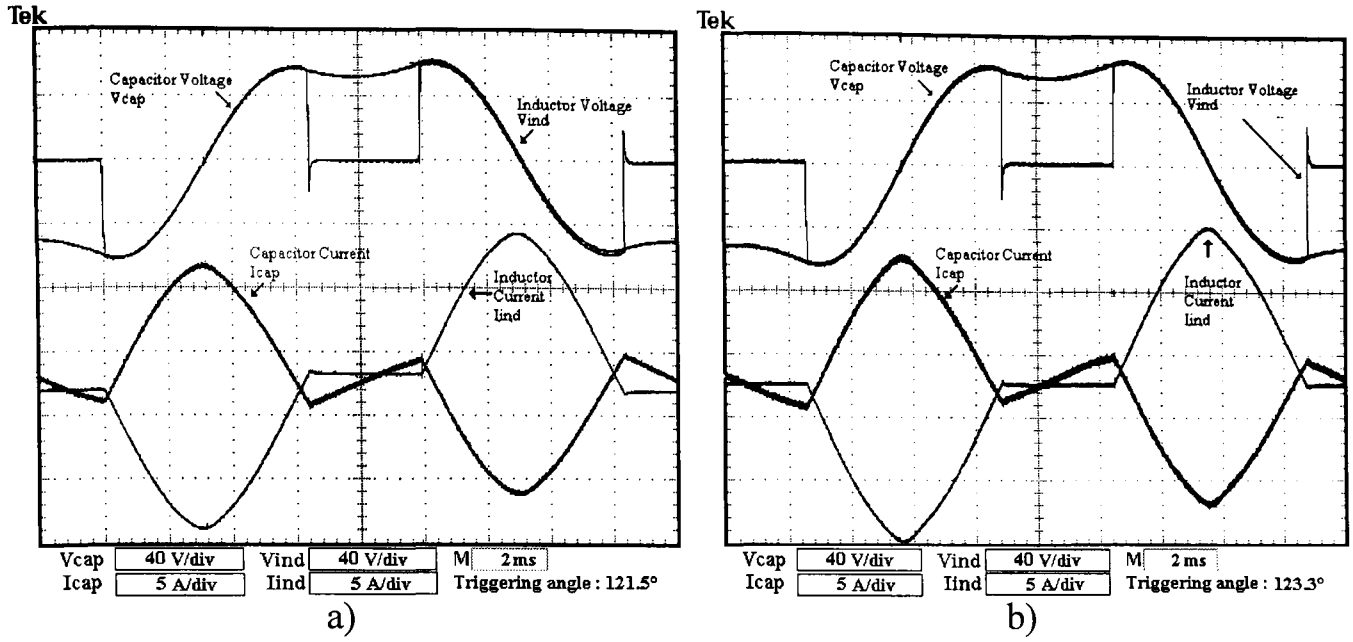


Figure 6.7. TCSC waveforms in the inductive region II: a) α=121.5°; b) α=123.3°

For completeness, Figure 6.8 shows the capacitor voltage profile of the three-phase TCSC prototype operation. In order to show the TCSC capacity to independently operate each phase, the capacitor voltages are forced to be unequal.

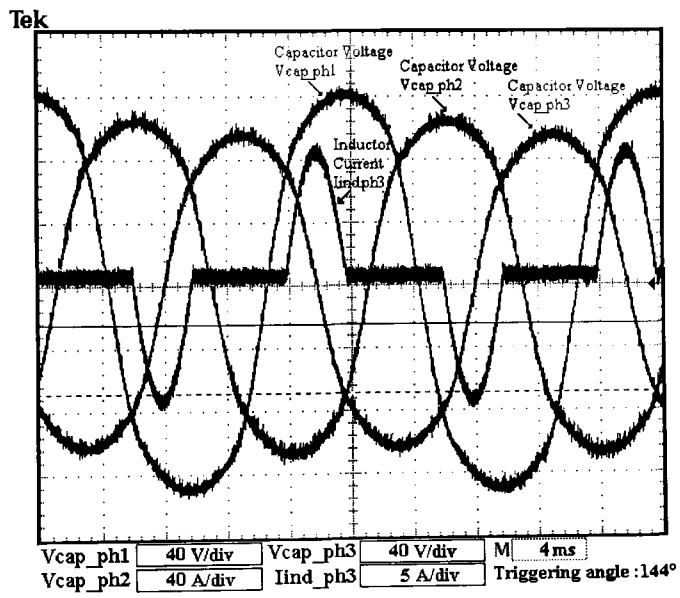


Figure 6.8. Steady-state three-phase TCSC operation at α=144°

6.3.2 TCSC Modulation as a Network Dynamic Operation Condition

Use of the TCSC to counteract some of the abnormal conditions present in today's transmission systems has been amply discussed in previous chapters. For such cases, the TCSC operation is adapted to response to frequency and amplitude changes in the network. The TCSC modulation is a dynamic operation condition. The three possible TCSC modulations modes are capacitive-capacitive region (CCR), capacitive-inductive region (CIR) and inductive-inductive region (IIR). The former is the most widely used and the latter has not even yet been reported. Figure 6.9 depicts the TCSC waveforms for CCR mode using two different modulation frequencies, 1.25Hz and 2.5Hz.

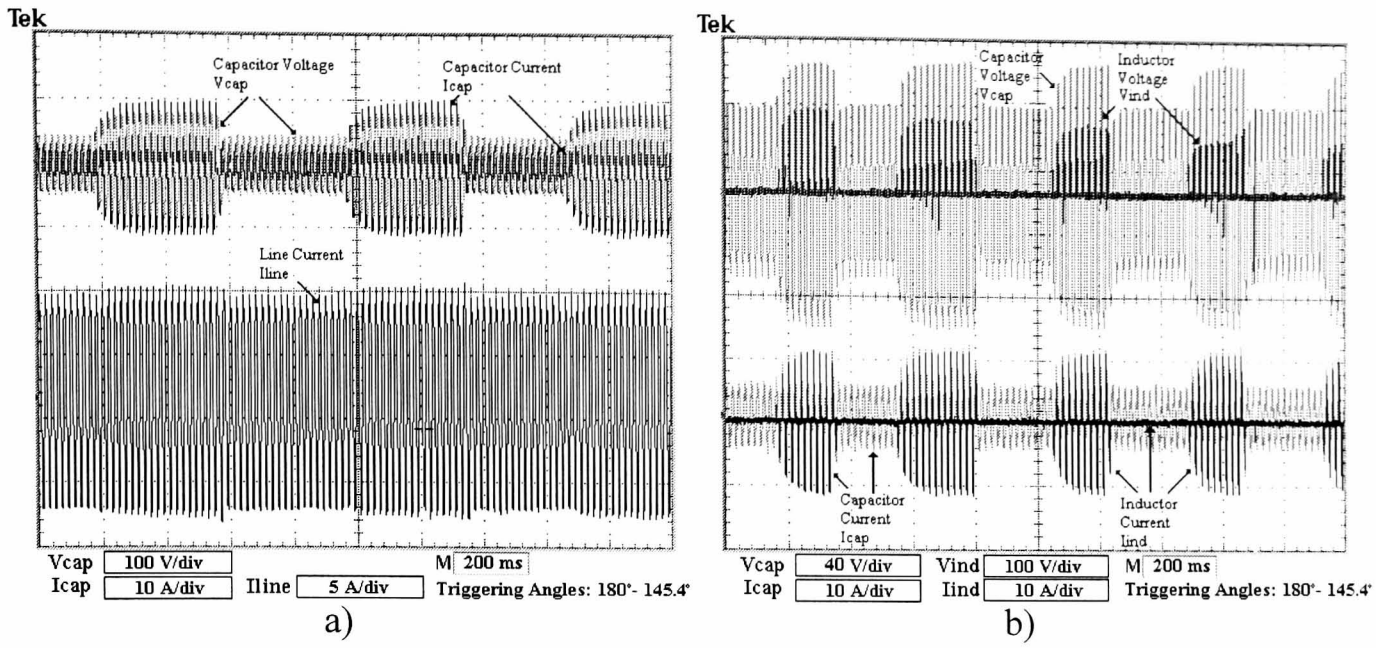


Figure 6.9. TCSC modulation with CCR mode: a) 1.25 Hz; b) 2.5 Hz

The CCR mode can be performed using either VTR or CTR. In Figure 6.9, VTR was used. The results in Figure 6.10 show waveforms resulting from TCSC modulation at 5 Hz using the CTR option.

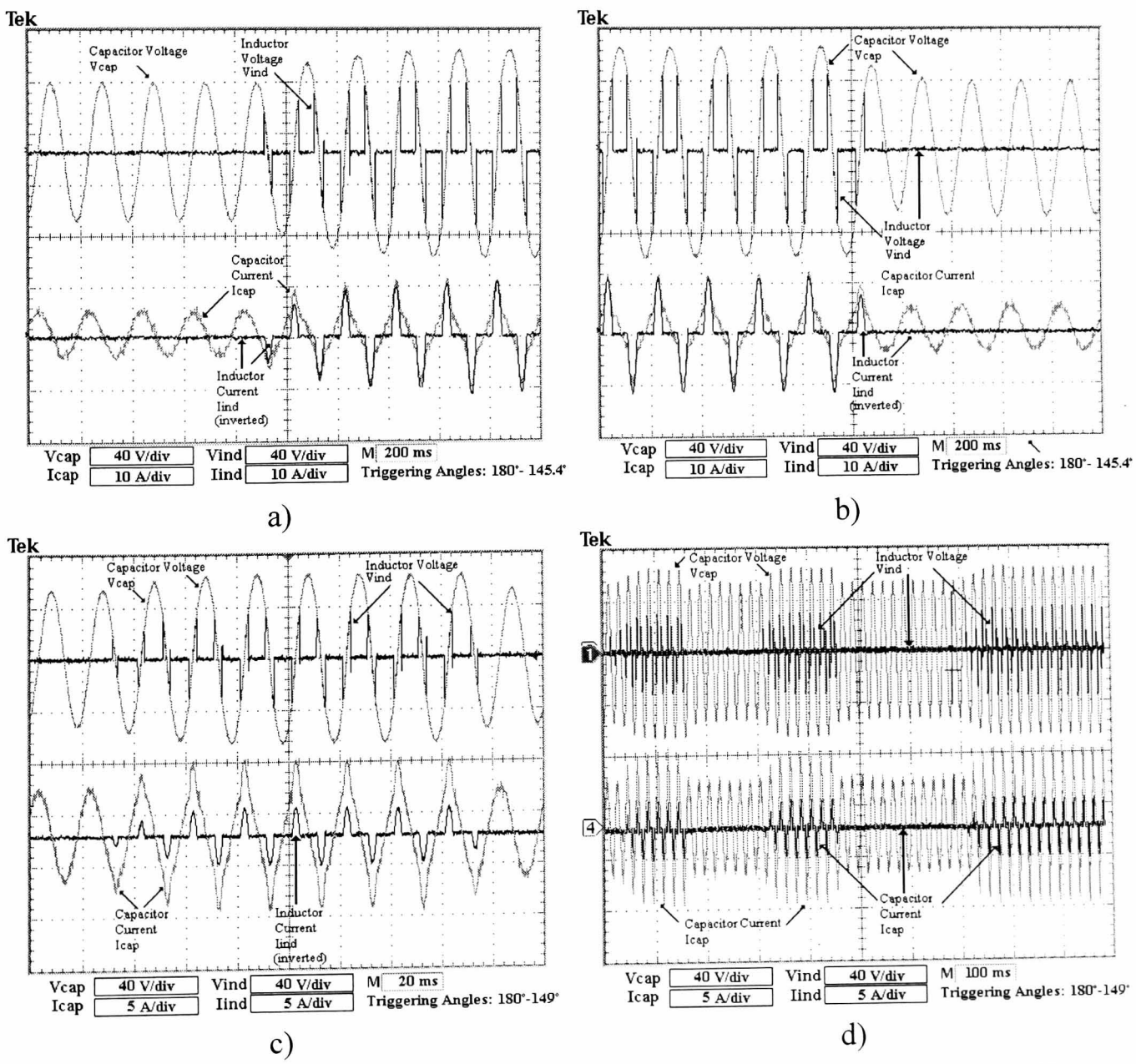


Figure 6.10. TCSC modulation with CCR mode and CTR: a) α=180° to 145.4°; b) α=145.4 to 180°; c) α=149°, closer view; d) modulation at 5 Hz

It is particularly noticeable that the voltage and current variations provoked by the step triggering angle changes in the CCR mode are smoother compared to those when the VTR option is used.

The CIR mode can be closely identified with the bang-bang strategy utilised to damp power oscillations phenomena, a condition that has been fully detailed in the previous chapters. In this case the TCSC reactance alternates from one operating region to another in order to cause a current modulation which promptly damps the abnormal condition. Figure 6.11 shows the TCSC modulating the power line at 2 Hz using the CIR mode.

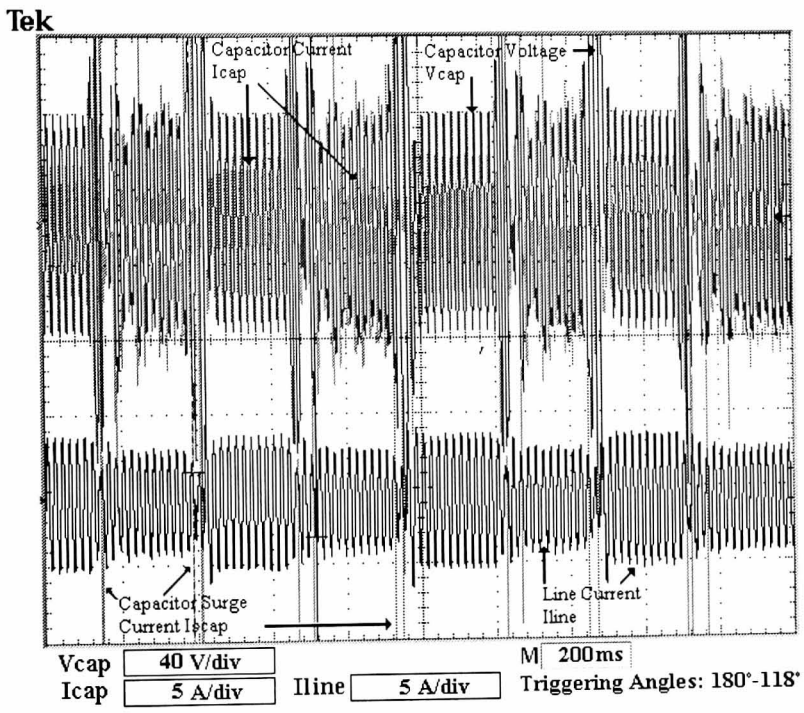


Figure 6.11. TCSC modulation with CIR mode at 2 Hz

The current modulation is, apparently, more effective in CIR mode than in CCR mode. However, the use of CIR brings many problems due to short instabilities, which cause very large inductor and capacitor current surges in the TCSC, highly stressing the thyristors, inductors and capacitors. This event can be understood as momentary instantaneous resonant points arising while crossing the fundamental resonance zone from the TCSC capacitive region to the inductive region or vice-versa. The region between the apparent TCSC inductive and capacitive region is termed transition zone. When the TCSC goes from the inductive to the capacitive region, the capacitor voltage inversion and the fundamental resonance mode delays the stabilisation of the TCSC. Similarly, when the TCSC operation crosses the transition zone into the inductive region, there is a further delay to settle the controller since in addition to the previous

factors, there is also the presence of the intrinsic resonance mode, even when the triggering angle α=90° is not used. As a consequence of these combining factors, the capacitive to inductive transition is less stable than the transition in the opposite direction. Figure 6.12 presents a more detailed view of the transition TCSC waveforms. Two points should be noticed around the transition zone; a) the controller presents irregular, highly distorted waveforms and b) the width of the zone is not restricted to a particular duration.

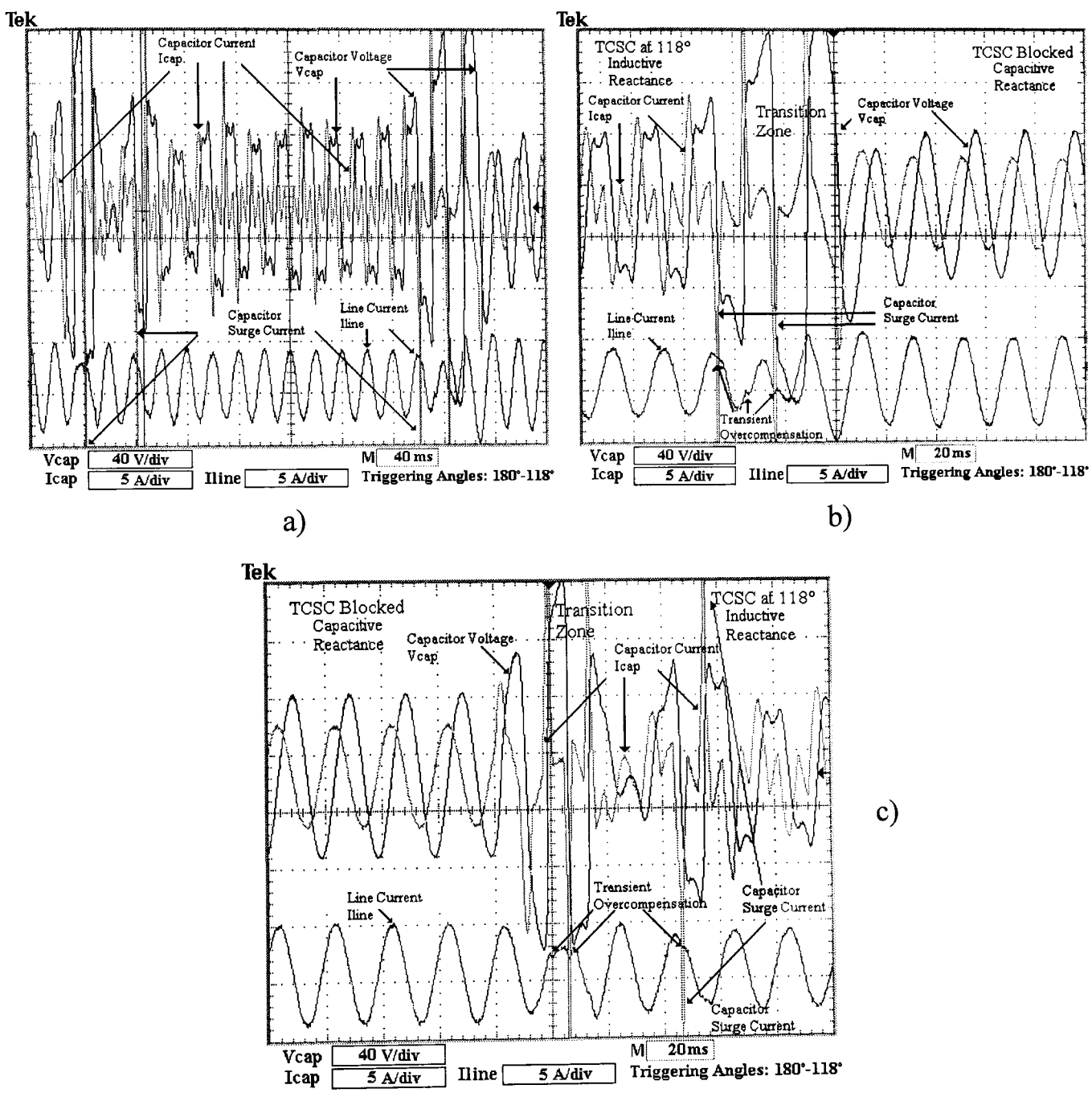


Figure 6.12. TCSC transition zone: a) overvoltages peaks produced by the TCSC modulation between inductive and capacitive regions; b) inductive to capacitive transition; c) capacitive to inductive transition

Since the TCSC undergoes inter-region commutations at higher frequencies there are two additional effects arising; a) the surge current peaks increase in number and magnitude, and b) the positive and negative dc polarisation of the controlled capacitor is noticeable. The voltage and current stabilisation in both regions deteriorate with

increased distortion, as shown in figure 6.13. It is important to notice that the large surge peaks of the inductor current occur at the capacitor voltage zero-crossing point indicating that the total instantaneous cancellation of the capacitive and inductive effects in the TCSC occurs at that precise instant.

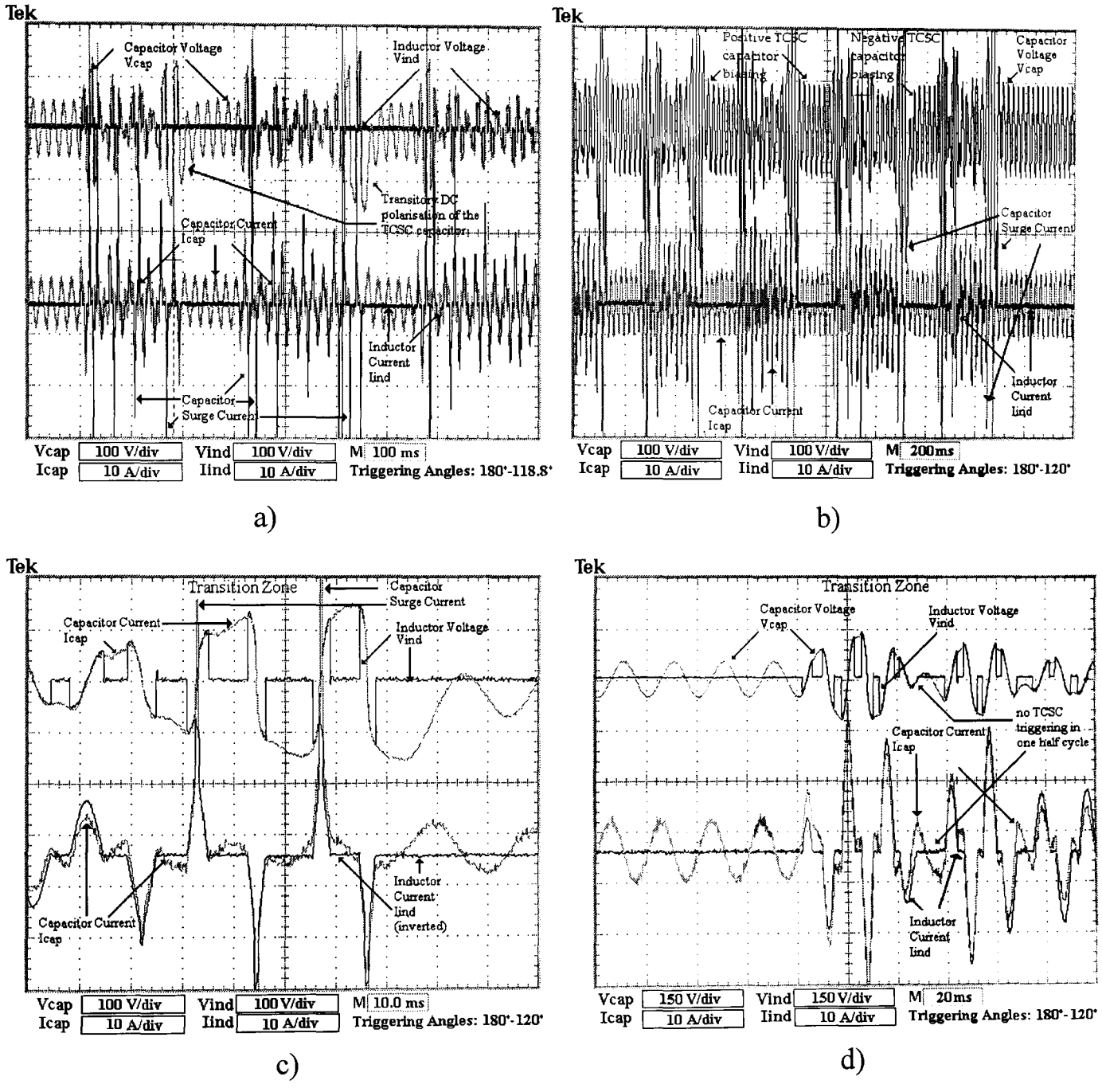
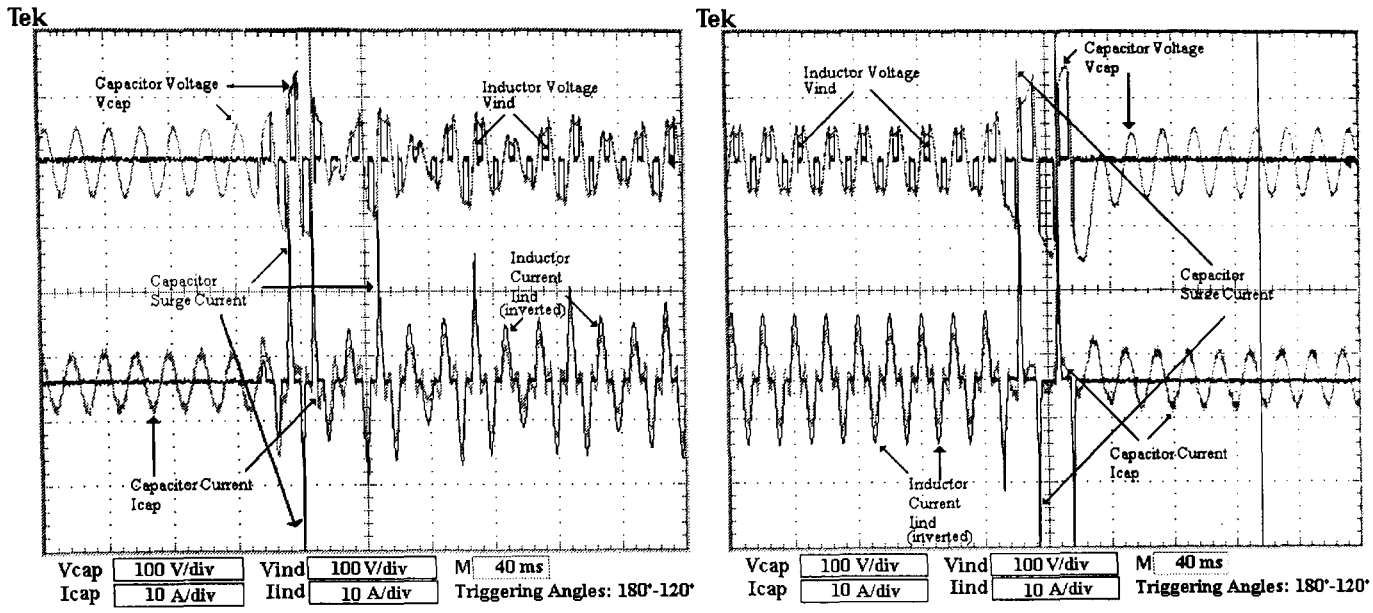


Figure 6.13. TCSC short instabilities: a) modulation at 3 Hz; b) modulation at 4.5 Hz; c) current surge peaks and dc polarization in the inductive to capacitive transition; d) current surge peaks in the capacitive to inductive transition

It can be observed that the higher the commutation frequency the larger the surges peaks are and the longer it takes the controller to become stable, this limiting the TCSC modulation to very low frequencies. A smoother capacitive-inductive-capacitive transition at frequency commutation lower that 1 Hz can be visualised in Figure 6.14.



a) b)

Figure 6.14. Smooth TCSC modulation at very low frequency: a) capacitive to inductive transition; b) inductive to capacitive transition

The TCSC strongly interacts with the transmission system when modulating the line current. This is particularly true if the CIR is used but the modulation is limited to slow varying events. An author's proposal is to use the CIR mode at the lower end frequency spectrum, preferably below 1Hz, of power oscillations and voltage fluctuations phenomena and the CCR mode for all the other cases.

It should be remarked that, in all the above cases the TCSC prototype is operating in open loop, with no external stimulus being contributed by the network undergoing abnormal conditions

6.3.3 Fundamental Resonance Mode Condition

The TCSC has one fundamental resonance mode, one intrinsic hidden resonance mode and the risk of *n* other resonance modes. The total apparent reactance taken by the controller in any resonance condition is unpredictable in nature and it may be argued that it is mathematically undefined. Figures 6.15 and 6.16 present the cases for the inductive and capacitive resonance TCSC behaviour, respectively.

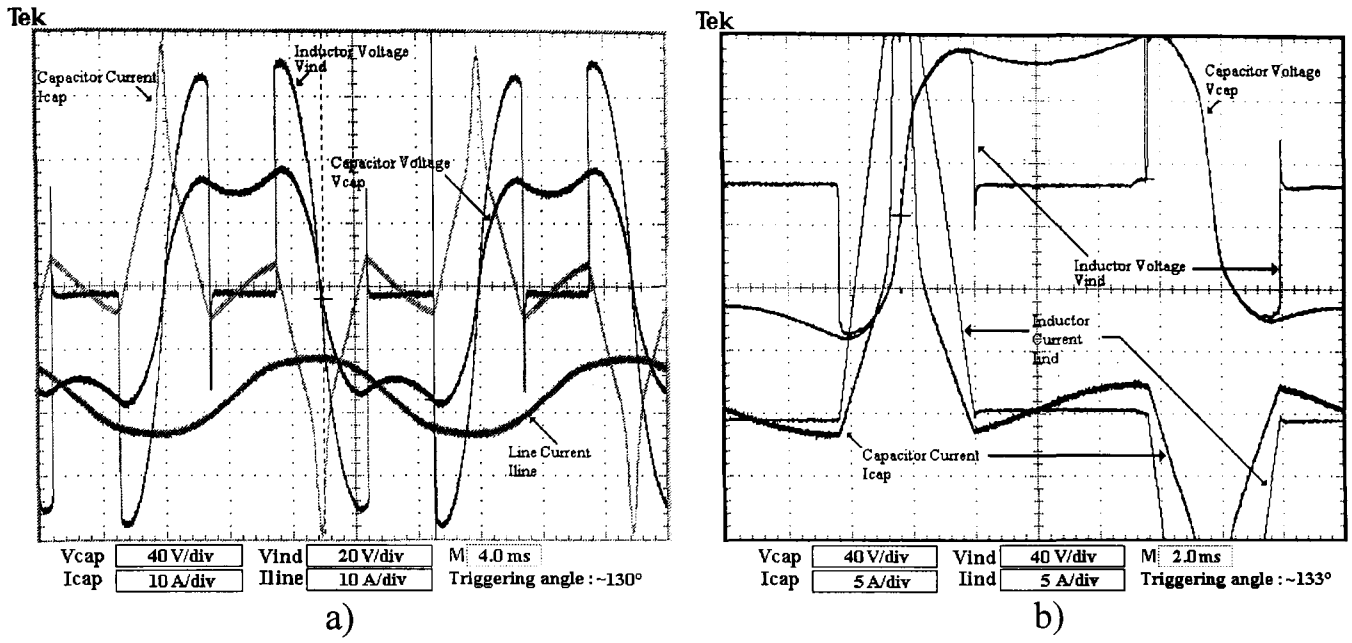


Figure 6.15. TCSC inductive behavior at resonance: a) $\alpha \approx 130°$; $\alpha \approx 133°$.

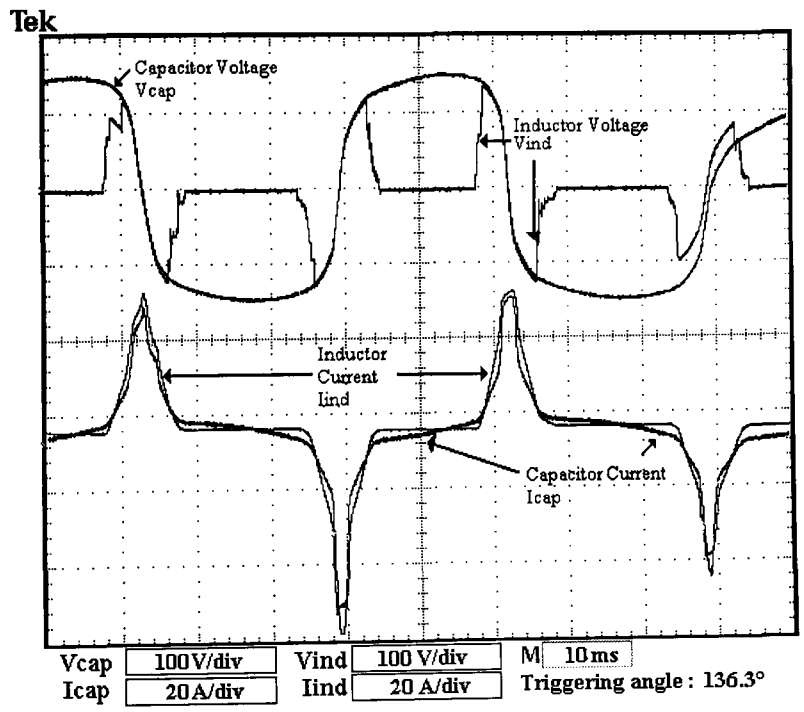


Figure 6.16. TCSC capacitive behaviour at resonance, $\alpha \approx 136°$

Under certain conditions, the TCSC prototype can significantly distort the line current. Figure 6.17 shows the case when the controller operation distorts the line current by instantaneously overcompensating the scaled-down electrical system (with no transformers). Likewise, Figure 6.18 presents the case when the TCSC resonance continuously overcompensates the compensated transmission line and ancillary devices, including transformers.

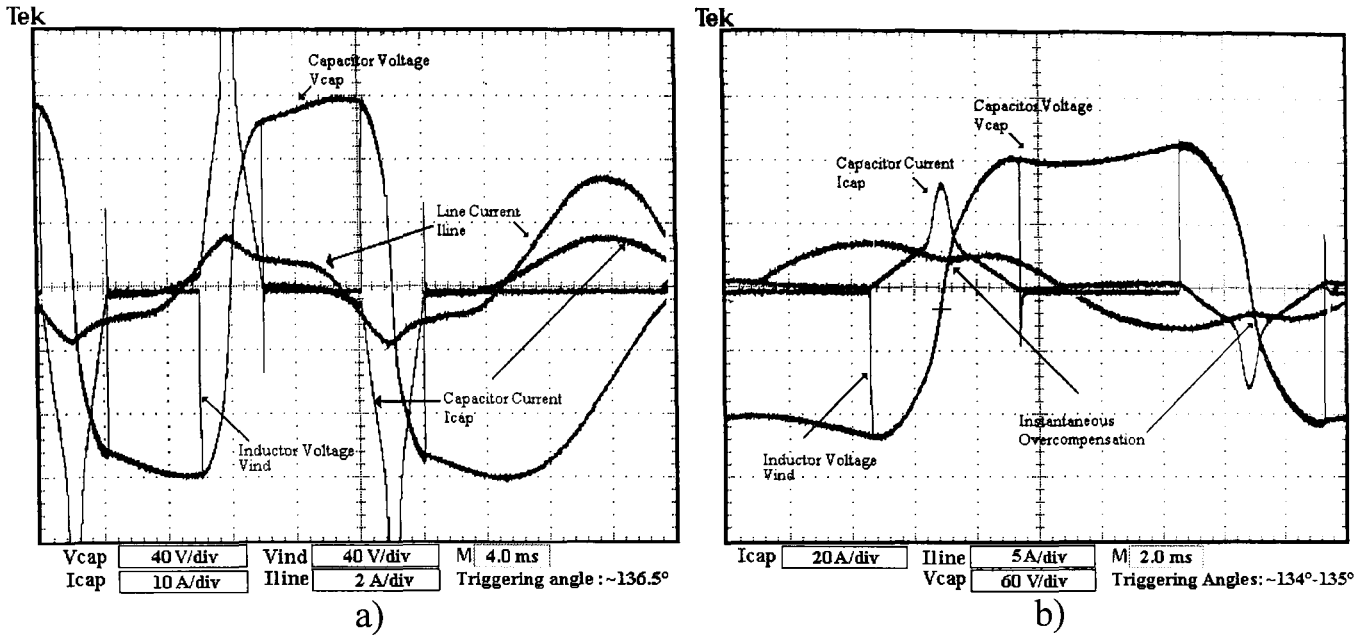


Figure 6.17. Instantaneous line overcompensation at voltage zero-crossing due to TCSC resonance: a) high instantaneous inductive behaviour; b) high instantaneous capacitive behaviour

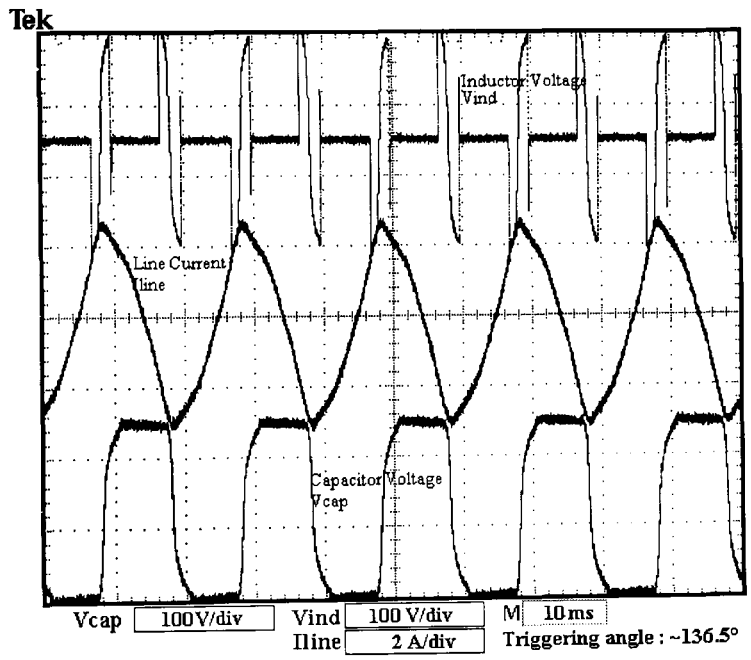


Figure 6.18. High line current distortion due to TCSC overcompensating the line-transformer system

An interesting observation is that the overcompensation can cause a dip in the current line, as shown in Figure 6.17b, or a small peak, as shown in Figure 6.17a. A possible explanation of the very different results when the TCSC is, apparently, working under similar operating conditions is that the TCSC is operating in the vicinity of the fundamental resonance mode but in different region in each case. In particular, the inductive-type appearance of the capacitor voltage profile in figure 6.17b mixed with a capacitive-type capacitor current profile can be understood as the transition turning-point between capacitive overcompensation to inductive overcompensation. Figure 6.18 shows the highly distorted line current provoked by the TCSC resonance. This case can

be explained considering that the scaled-down transmission system includes three sets of transformers. If the TCSC resonates, its capacitive reactance can be so high that the transmission line can result fully compensated, and the reactance of the transformers, at both ends of the line, can also be affected, degrading the linearity of the system. The condition shown in Figure 6.19 can also be linked to system operation close to series resonance. To the best of this Author's knowledge, measurements of a TCSC undergoing resonance have not yet been presented in the open literature.

6.3.4 Non-Characteristic Conditions

Turning the TCSC prototype on has a non-zero response time. At triggering angles close to 180°, the controller may not have sufficient energy to reach the activation state since the current injected to the TCSC inductor branch may not be enough to switch the thyristor on. Furthermore, the TCSC "turning-off" and "turning-on" triggering angles, are not the same. As a general rule, the higher the line current, the closer the "turning-on" angle to 180°, and the lesser the angular difference between the TCSC activation and de-activation angles. Figure 6.19 presents the voltage and current waveforms in the TCSC prototype at two different stages close to the "turning-on" triggering angles. After the "turning-on" angle has been reached, the TCSC presents its characteristics current and voltage waveforms.

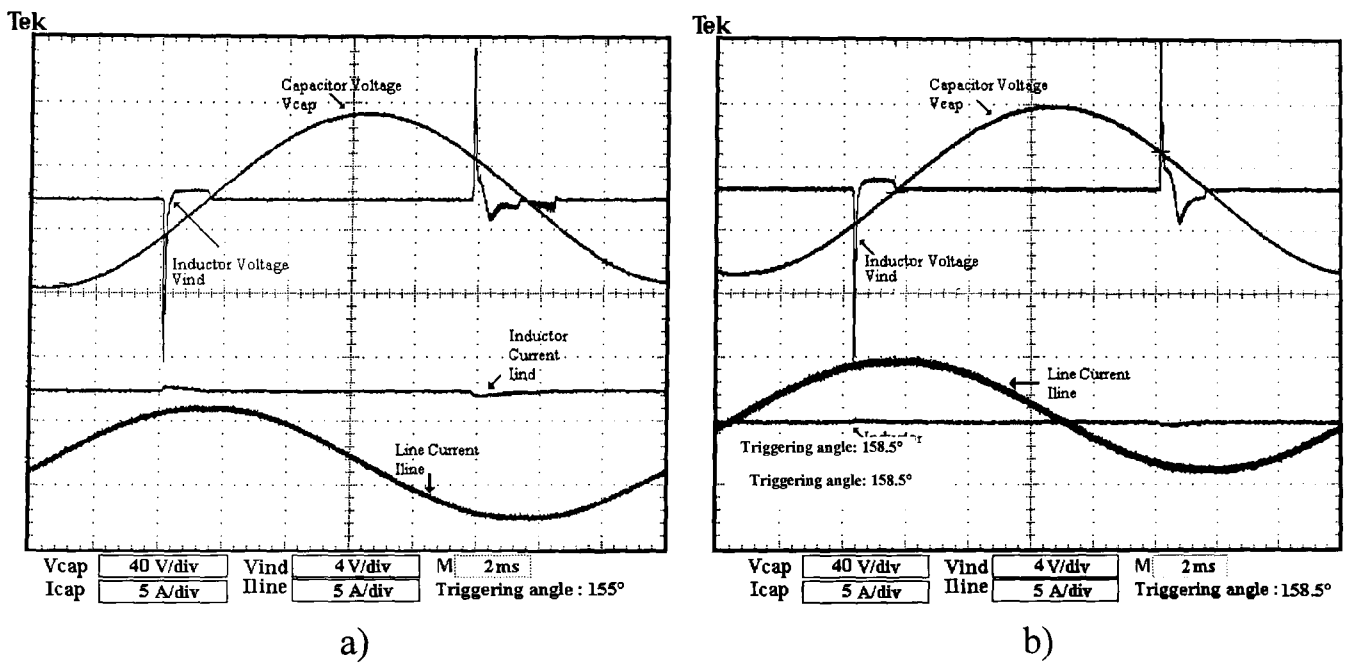


Figure 6.19. TCSC current and voltage waveforms before the thyristors are activated: a) α=158°; b) α=155°, closer to "turning-on" angle

Another non-typical behaviour is the unbalanced TCSC triggering caused by abnormal network conditions, and irregular current and voltage zero-crossing points. Figures 6.20a and 6.20b show cases of TCSC prototype unbalanced behaviour in the capacitive region, and Figures 6.20c and 6.20d show instances of unbalanced behaviour in the inductive region.

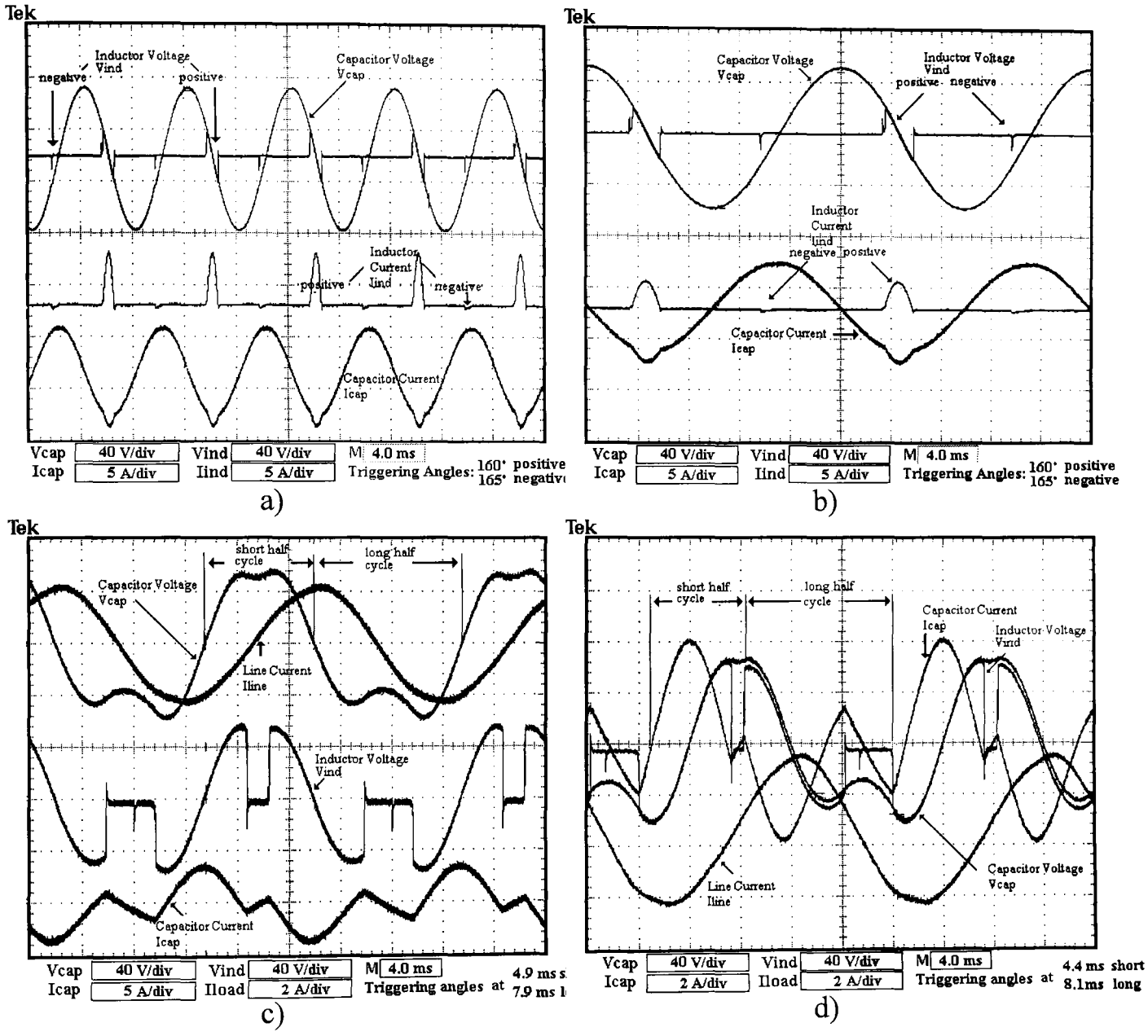


Figure 6.20. Unbalanced TCSC operation due to unbalanced triggering: a) α=160° positive cycle, α=165° negative cycle; b) closer look into a); c) α=118.5° long semi-cycle, α=110.5° short semi-cycle; d) α=121° long semi-cycle, α=99° short-cycle

6.3.5 Voltage distortion

The TCSC currents and voltages become increasingly distorted as the triggering angle approaches to resonance. At least in theory, the harmonics produced by the TCSC might pollute the network at the transmission system voltage level. However, such a threat is not so significant owing to three main factors: a) the TCSC's capacitor acts as a shunt filter trapping most of the harmonic current produced by the inductor-thyristor branch;

b) the current escaping the LC circuit is small compared to the line current; c) in compensated transmission lines where combined fixed and controlled capacitors are used, most of the compensation is provided by the former rather then the latter. Hence, the fixed capacitor, which produces no voltage distortion, overrides the voltage distortion of the smaller capacitor controlled by the TCR. The fixed capacitor, from the point of view of the network, can also be seen as a second filtering stage. Figure 6.21 shows the voltage capacitor distortion of the TCSC at various triggering angles.

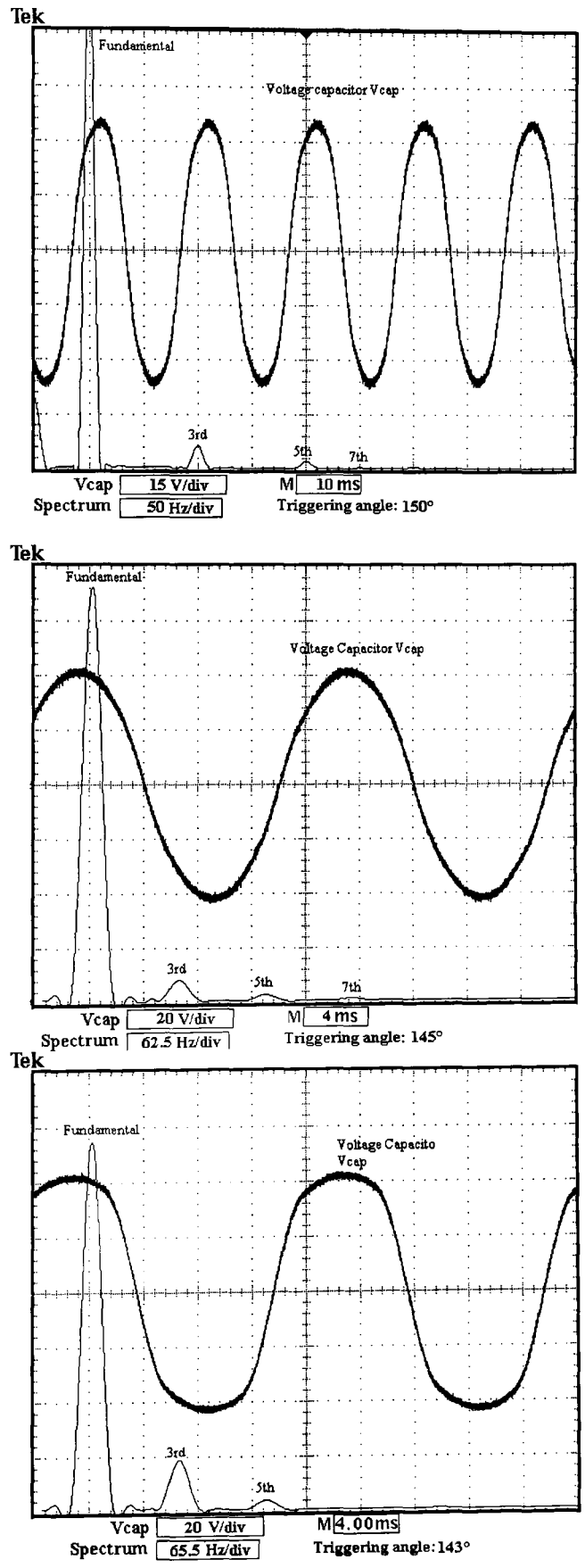


Figure 6.21. TCSC voltage capacitor distortion increment with increment of α: a) α=150°; b) α=145°; c) α=143°

It can be depicted in Figure 6.21, the voltage distortion, in particular the 3rd harmonic, goes higher as the triggering angle approaches the fundamental resonance mode.

TCSC schemes with a series fixed capacitor connected to it, may not inject significant voltage and current harmonics to the network. However, compensation schemes where various TCSC modules are series connected, but without a series fixed capacitor, the harmonic distortion might be higher because the distortion provoked by each TCSC module may eventually summate and, as the filtering effect of the fixed capacitor no longer exist, the line current and voltage may deteriorate more evidently. The harmonic distortion produced by the TCSC requires more experimental investigation.

6.4 DISCUSSION

Gaining further insight into the transitory and dynamic behaviour of TCSCs, for a wide range of both normal and abnormal system conditions, should support the development of improved control strategies, relaying protections in compensated environments and equipment protection. So far, most of the research work in the open literature has focused in assessing a narrow range of TCSC steady-state behaviour. This can be partially explained by the preoccupation to solve power flow related problems owing to the great attention that energy transactions in de-regulated electrical systems have generated over the last decade. As it is widely known, power flow studies are a steady-state problem, and the TCSC models intended for power flow analysis have to conform to this requirement.

Experimental investigation with FACTS and Custom Power are mainly oriented to understanding and elucidating the dynamic, transitory and non-characteristic behaviour of the equipment, emphasising aspects which are not easy to replicate in actual industrial installations. The characterisation of all power controllers is useful to improve the current design, and the emergence of new applications and ideas.

The use of CIR modulation to damp high-energy, very-low frequency (1 Hz and below), power oscillatory phenomena, such as power swings damping and power oscillations, as well as to mitigate voltage fluctuations at frequencies in the lower end band of the spectrum, 4 Hz and lower, is a realistic option. For SSR conditions, this TCSC

operation mode does not look suitable. For such an application the CCR mode appears to be a better option to use.

The use of VTR and CTR has each their advantages and drawbacks. When using VTR, the TCSC triggering system loop requires a voltage level stabiliser with a better regulation capability than that required if the CTR is used because in most system conditions the transmission line current varies smoothly except for cases of resonance, faults and voltage fluctuations conditions if the system is weak. As expected, CTR is a good option if the CCIR mode is used. A guideline for the selection of the CCRS, CIRS and their respective triggering modes, depending on the TCSC application, is presented in Table 6.1.

Table 6.1. Guidelines for the selection of TCSC operating and triggering references

Phenomena	Very low frequency	low frequency	Wide spectrum modulation
Power oscillations	CIR/VTR	CCR/VTR-CTR	
SSR			CCR/CTR
Voltage fluctuation mitigation	CIR/VTR		CCR/CTR
Fault current limiting	CIR/VTR		
Flow regulation	CCR/ VTR-CTR	CCR/ VTR-CTR	

6.5 CONCLUSIONS

In this chapter selected voltage and current measurements have been presented giving a realistic account of the TCSC behaviour under a range of both normal and abnormal network operating conditions. The TCSC prototype built by the author has shown its flexibility and functionality, throughout the extensive number of successful experiments, recommending itself as a well-designed and constructed experimental FACTS research tool. The experience gained with the characterisation of the TCSC should prove invaluable in designing better control strategies, TCSC overcurrent and overvoltage protection, specification for power devices ratings, protective relaying algorithms for FACTS compensated lines, and proposals for new FACTS designs and topologies.

As established, the voltage fluctuation frequency range is quite wide, and the SSR phenomenon has frequencies above the power oscillations but below the fundamental frequency. To counteract these undesirable effects, the use of the capacitive-capacitive TCSC operation is highly recommended. On the other hand, in the case of power oscillations below 1 Hz and power swings, the capacitive-inductive operation can be recommended for some cases. Based on the basic proposed terminology, the operating modes and triggering references for the TCSC have been described and related to specific applications oriented to damp and mitigate abnormal network conditions, such as power oscillatory phenomena and voltage fluctuations.

Besides the steady-state operation, the TCSC behaviour investigated in this chapter includes the singularities of the CCR and CIR modulation modes, fundamental resonance and unbalanced operation. The results presented in this chapter are not easily found in the open literature.

The exact total apparent reactance taken by the controller in the fundamental resonance mode condition is unpredictable in nature and arguably mathematically undefined. The high current surge peaks occurs at capacitors voltage zero-crossing points. To ensure the well-being of the TCSC and electrical network, such operating condition should be prevented, defining an angular safety margin of say 4° to 3°. Large surge signals are also present in the TCSC when the CIR modulation is used. The high surge overvoltage and overcurrents can be damaging to the thyristors and capacitors, either instantaneously or in the long-term. Hence, preventive action should be taken at the design level.

CHAPTER

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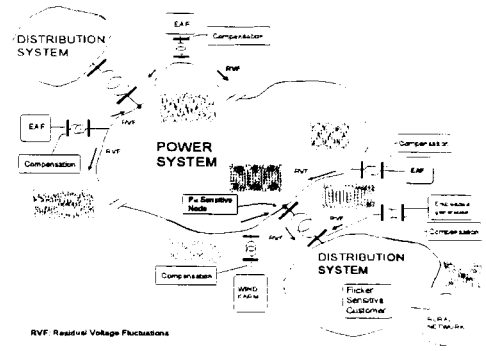


TCSC AS A VOLTAGE FLUCTUATION MITIGATION EQUIPMENT: PERFORMANCE EVALUATION ON A REAL-TIME TESTING ENVIRONMENT

7.1 INTRODUCTION

Digital simulations have been of great assistance in assessing the steady state and transient operation of transmission and distribution systems. Application programs and tools such as power flow studies; short-circuit analysis; harmonic propagation analysis; and transient stability state-estimation have been used very effectively to this end. Moreover, PSCAD/EMTDC [1] and EMTP [2] are two well-known general purpose time domain simulation tools for studying the transient behaviour of electrical networks. In contrast, far less work and application tools and methods exist for assessing power system phenomena in real-time.

Open-loop real-time testing is commonly known as playback testing. Such a scheme is shown in Figure 7.1a. Closed-loop, real-time simulations can be performed by feeding back, to the host computer, output signals resulting from previous stimulus to the electric system under test. This situation is illustrated in Figure 7.1b, where the scheme is known as real-time Hardware-in-the-Loop (HIL) simulation and testing.

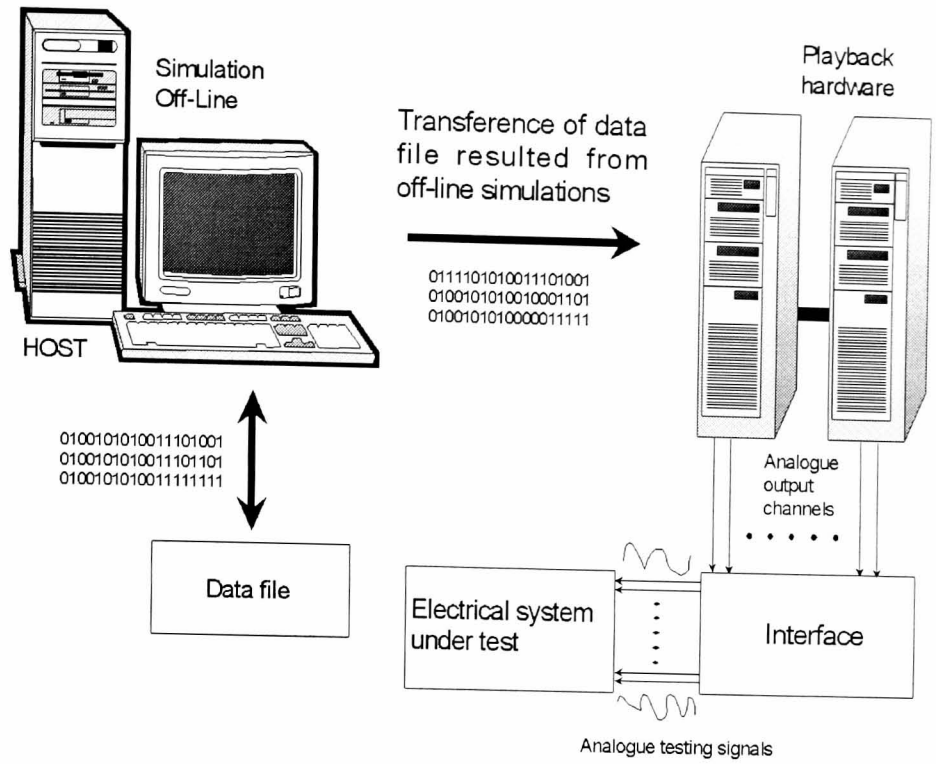


Figure 7.1a. Playback Testing

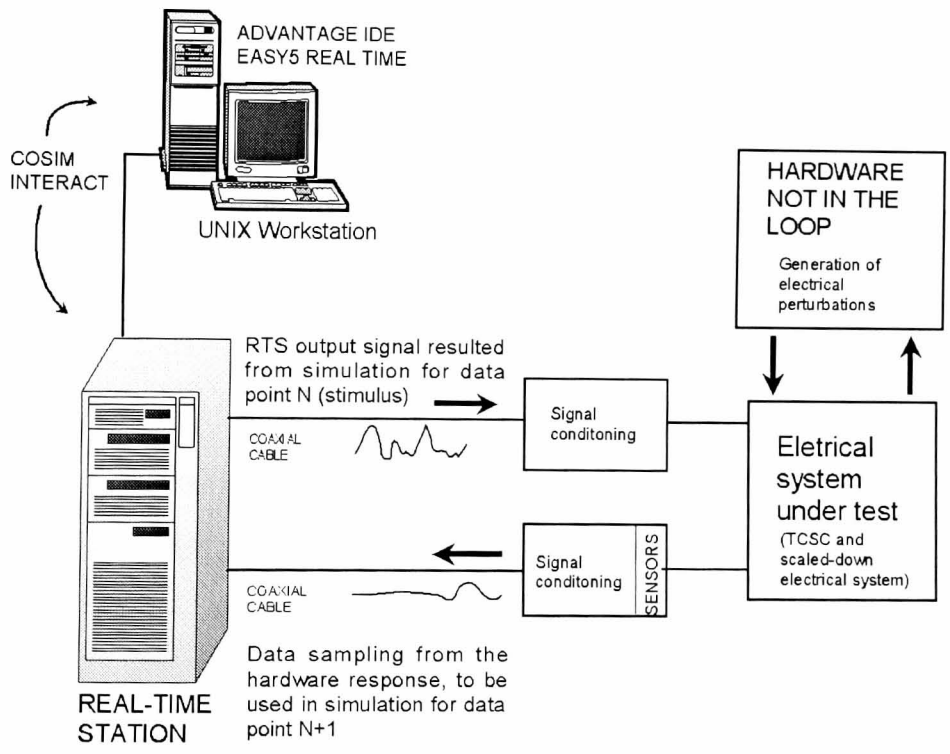


Figure 7.1b. Real-time HIL testing

The Real Time Digital Simulator (RTDS) from RTDS Technologies and the AD Real Time Station (ADI RTS) from Applied Dynamics International are examples of commercially available, high-performance real-time computing platform for closed-loop HIL simulation and testing. The latter has been used in this research project because of its availability and flexibility of use in a wide range of engineering applications.

7.2 A COMPUTATIONAL PLATFORM FOR A REAL-TIME HARDWARE-IN-THE-LOOP TESTING ENVIRONMENT

A real-time digital simulator together with supporting electronic systems provides an ideal real-time testing environment for closed-loop experimentation of FACTS and Custom Power controllers, and associated control strategies. The real-time experimentation, as used in the present work, requires that the digital simulation of the modelled system be executed in real-world time. This implies that at any given instant, the computational process of a previous input data point terminates before a new sample is taken from the incoming analogue response of the prototype under test. In this way, a physical phenomenon, or the response of a control scheme or an electric system element can be simulated as it occurs in the real world, and, when combined with appropriate hardware, the operation of the overall system is replicated. This covers both normal and abnormal operation.

7.2.1 Digital Computing Platform for Real-Time HIL

A Real Time Station (RTS) is used in this research work for the development of the control strategy; the virtual IEC-Flickermeter; and the closed-loop hardware-in-the-loop testing. The RTS is a specialised computing platform developed by Applied Dynamic International (ADI) to perform digital simulation and interactive hardware-in-the loop solutions on a real-time basis. The development of the RTS has been primarily for aerospace and automotive industries, however, applications to simulate transmission and distribution electrical systems are growing rapidly. The software tools supported by the RTS comprise a wide range of general analogue and digital control transfer functions blocks; mathematical functions blocks; and extensive pre-defined component blocks such as switches and special purpose blocks. This software also permits the inclusion of tailored user-defined FORTRAN and C routines, in which many transmission and distribution systems and phenomena can be modelled.

The RTS computing platform is a true multi-processor platform with an extensive array of I/O interfaces capable of parallel processing and I/O interactions in real-time. The system is relatively open architecture allowing selection of the computational power and I/O channels to suit a specific application, facilitating also the system upgrading for future computing and other hardware needs. The core of the RTS software management

is the real-time operating system (RTOS), which enables effortless use of the complete suite of special tools. In this research project, the RTS is coupled to a host Sun SPARCstation, serving as administrator of the software simulation tools, in which the application models are developed and simulated on a non-real-time basis. The host workstation is also used to kick start the real-time simulations and to provide an interactive interface with the RTS at run-time.

7.2.2 Real-Time Station Hardware

The RTS architecture is based on the VMEbus backplane, where different types of processors are coupled and synchronously working together. The fundamental RTS operation relies on four-task specific processors namely: Simulation (SP), Communication (COP), Compute Engine (CE) processors and User Interface Processor (UIP), together with the VMEbus Interact Manager (VIM). The generic configuration of the RTS is depicted in Figure 7.2

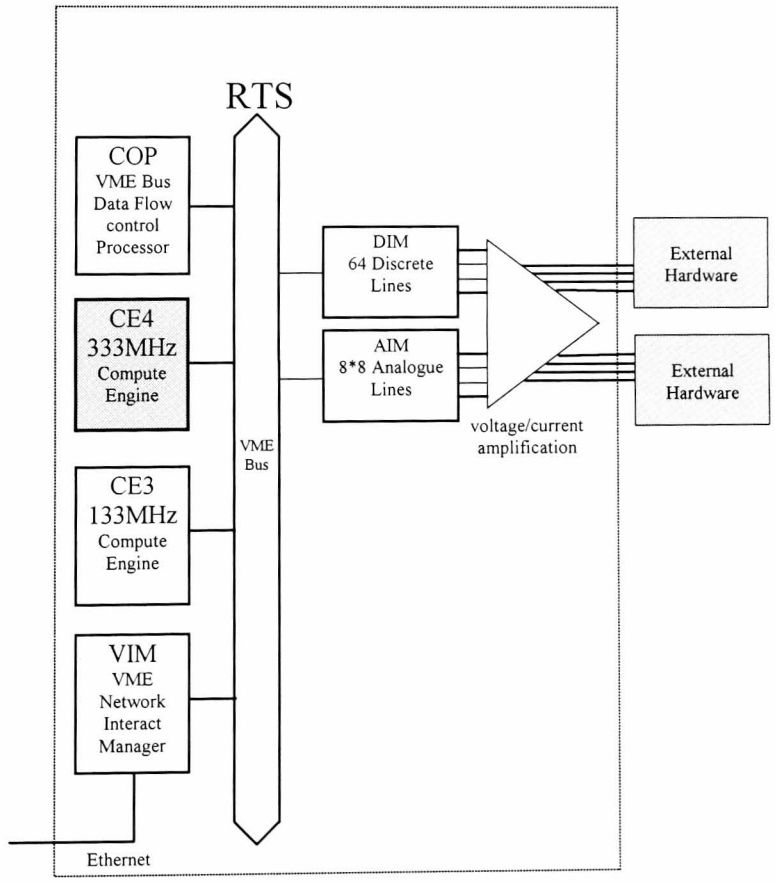


Figure 7.2. Real-Time Station (RTS) Generic Configuration

7.2.3 Simulation Processor

The simulation processor is used for general analogue-to-digital and digital-to-analogue interfacing between the system under test and the computing platform. The SP is embedded within a Parallel Intelligent Resource (PIR) hardware structure. The PIR is designed to allow the I/O data exchange to operate in parallel with model execution. As a consequence, VMEbus data traffic can be significantly reduced, and by implication, the processing load on the compute engines as well. The PIR also incorporates two interfaces: The Analogue (AIM) and the Digital (DIM) Interface Modules. Using the appropriate external analogue interface, protection and analogue signal processing, these modules are used to interface the control and electric system components modelled on the RTS to external hardware.

7.2.4 Analogue Interface Module

This module contains the circuitry necessary to perform the analogue-to-digital conversion of incoming signals (±10V maximum input), from the external electric system under test. Once converted the digital data is transferred to other processor into the RTS. In the opposite data flow direction, the AIM is also responsible for the digital-to-analogue conversion, outputting the data flow stream from the RTS into analogue signals (±10V maximum output). The RTS used in this project has one AIM containing 8 A/D channels and 8 D/A channels with a 12-bit resolution. The sampling period of the digital-to-analogue and analogue-to-digital converters is in the order of 8.6 μs per conversion per channel.

7.2.5 Digital Interface Module

The module provides the direct digital-digital output-input interface with external data. This interface is designed for 64-bit bi-directional digital I/O and has the capability to control each data line. The number of AIM and DIM modules may be included in the RTS to expand the PIR. The combination of up to six AIMs and DIMs using the VME Subsystem Bus is possible. This expanded processing power capacity enables a single SP to be applied to many interface tasks, without diminishing data transfer velocity of the primary system bus.

7.2.6 Communication Processor

The primary function of this Communication Processor is the data traffic control within the RTS and the link between the RTS and the host computational platform. The synchronisation of the multi-processor architecture is also part of the tasks assigned to the Communication Processor.

7.2.7 Compute Engine

The Compute Engine (CE) provides the core computing power to the RTS. In this processor, or array of processors, all the computations required for the real-time simulation are carried out. The current standard CEs include several versions of the Motorola PowerPC family. The Real-Time Station configuration used in this research project comprises two compute engines, a 133 MHz CE3 and a more powerful 333 MHz CE4. The RTS flexible open architecture, based on the VMEbus, permits the expansion of the computational power without the retirement of the earlier CE already installed. By using the ADvantage IDE software tool, before performing a simulation, the various models can be distributed across multiple compute engines through highly efficient shared memory exchanges.

7.2.8 User Interface Processor

This specialised processor provides the data link between the RTS and the workstation host. All data required for communication and interaction between the real-time platform and the workstation is transferred through the UIP. This architecture is designed to ensure real-time determinism, which is important to warrant that all real-time computation is accurate and repeatable.

7.2.9 VMEbus Interact Manager

The VIM communicates the RTS with the host computer workstation, or workstations on the LAN, with the purpose of program loading and run-time interaction between the user and the machine. Through the VIM, the user is provided with the ability to interactively communicate to the real-time simulation during run-time, selecting

variables for display, data logging, or parameter adjustment. This interaction is a non-intrusive operation, which ensures that the real-time characteristic of the simulation is retained while the data transfer occurs. This is a highly valuable tool when the real-time HIL experiments are running.

7.3 FLICKER SENSITIVE CUSTOMER

Voltage fluctuations propagating in the electrical network can adversely affect circuits, loads and customers in distribution systems. The potential sources of voltage fluctuations are many some examples are an induction motor connected at the far end of a long feeder, an EAF in the neighbourhood of a mostly residential circuit, and embedded generation system installed in a rural substation.

In voltage fluctuation analysis it is common practice to evaluate P_{st} at various distribution system interconnecting nodes [3,4]. Severity index evaluations are determined by identifying nodes exceeding the maximum permitted P_{st} level, bearing in mind local or international standards such as the IEC-614000-21 and IEC-61000-3-7. Identifying nodes with high P_{st} helps to identify loads and customers worst hit by voltage fluctuations.

The number of nodes, circuits, customers and loads potentially subjected to high voltage fluctuation and flicker levels are enormous, hence, a set of definitions is needed in order to localise each potential problem. Taking into account the concept of sensitive load used in harmonic analysis, a set of three P_{st}-flicker related definitions are proposed in this research work to apply to voltage fluctuation environments, in order to identify nodes, loads, and customer subjected to high flicker dosages.

The proposed definitions are given below:

1. P_{st} Sensitive Node: This is a node in the distribution network, including the point of common coupling with the transmission system, in which the evaluated P_{st} resulted from a single source or combination of voltage fluctuation sources, exceeds a pre-established maximum limit for that particular network. The assessment of P_{st} can be performed by simulation, for an early identification of the problem, or by direct measurements at the node if flicker is already a problem.

Voltage fluctuation sources can be internal or external to the distribution system. If external, the source can be located in the neighbouring electrical system, close to the P_{st} sensitive node and loads, as illustrated in Figure 7.3, or far away from the P_{st} sensitive node, as shown in Figure 7.4.

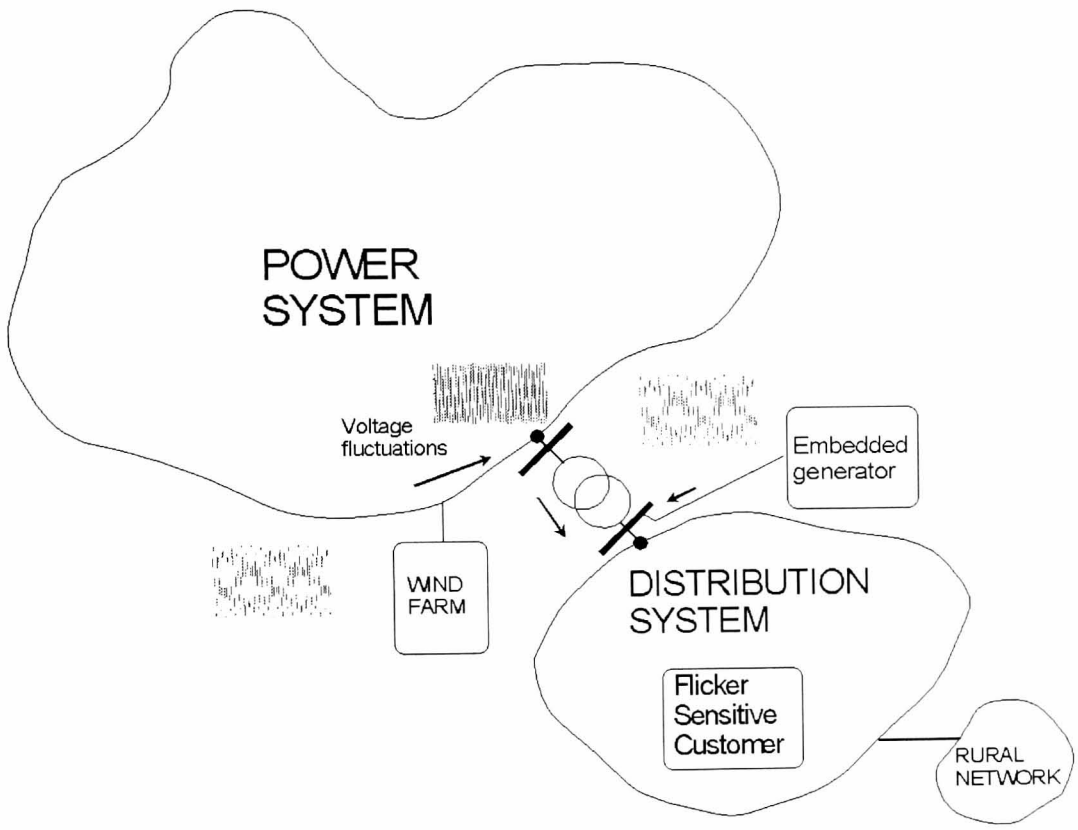


Figure 7.3. Near voltage fluctuation source

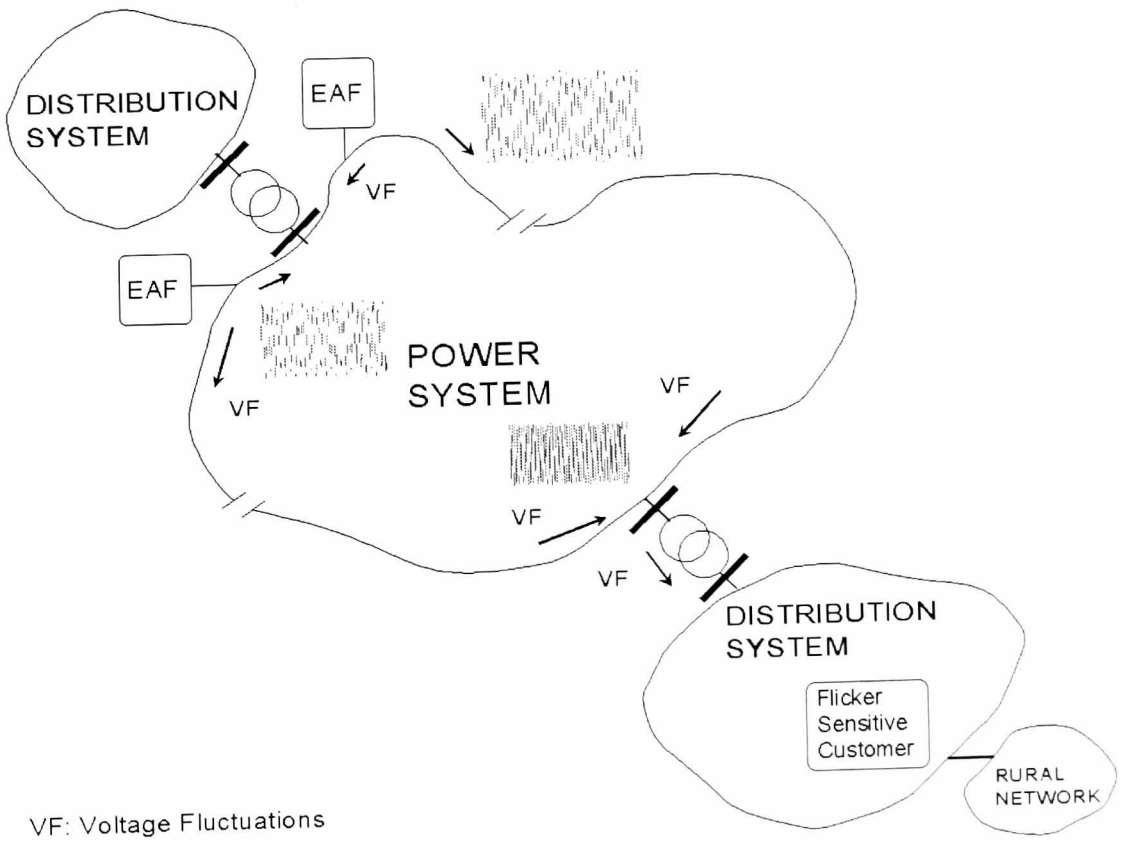


Figure 7.4. Far away voltage fluctuation source

2. P_{st} Sensitive Load: This concept refers to a load which under given voltage fluctuation conditions, applied to its input deviates from its normal operation, exhibiting a deteriorating performance. Incandescent and fluorescent lamps are archetypal P_{st} sensitive loads. Little information exists on domestic appliances such as fridges, TVs, and small pumps.

3. Flicker Sensitive Customer (FSC): This concept applies to individuals, or group of individuals, subjected to high flicker dosages (P_{st} close to one and greater) for long time periods. This condition eventually leads to customer complain. As a general rule, a P_{st} sensitive node supplies a P_{st} sensitive load (a residential, public, industrial or commercial circuit), which illuminates a FSC. Potential P_{st} sensitive nodes, P_{st} sensitive loads and FSCs can be identified by measurements or by customer complaints. However, simulation tools may be helpful in identifying problems well in advance.

The propagation analyses described in the open literature [3,4] normally make use of only a few nodes and a single voltage fluctuation source. Nevertheless, the analysis techniques reported can be developed further, including larger electrical systems, multiple voltage fluctuation sources, multiple IEC-Flickermeter, and mitigation apparatus. Alternatively, suitable models implemented in EMTP or PSCAD™ can be used instead. A tailor-made analysis tool may be helpful in evaluating the dynamic behaviour of distribution systems under complex voltage fluctuation variations, in order to identify circuits, loads and customers affected by high P_{st} levels. The influence of grid connection on mitigation effectiveness; the voltage fluctuation penetration in transmission and distribution system with embedded generation; the optimal placement of voltage fluctuation sources to minimise their impact in the network, are all important aspects which deserve more research attention. The development of a voltage fluctuation analysis tool, which includes the cases just described, would contribute to better understand electrical systems.

7.4 THE TCSC CONTROLLER AS A VOLTAGE FLUCTUATIONS MITIGATION APPARATUS

Shunt FACTS controllers such as the STATCOM; the SVC-light©; and the SVC, together with shunt Custom Power controllers such as the D-STATCOM, are equipment

already in use to mitigate voltage fluctuations in EAF; wind farms; and large induction motors. The key operative aspect of these controllers is their capability to provide voltage stabilisation, compensating reactive power, some of them also active, at the point of common coupling. The control actions involved are intended for power factor improvement, to minimise power consumption, and above all, to improve the overall plant performance. All these measures also contribute to voltage fluctuation mitigation. Even though field experience has demonstrated the effectiveness of shunt-connected controllers, the mitigation process is not perfect and voltage fluctuations are allowed to propagate in the electrical network. These post-mitigation remaining voltage fluctuations are termed Residual Voltage Fluctuations (RVF), which have a residual P_{st} that can provoke a residual flicker sensation. Figure 7.5 illustrates the residual voltage fluctuation concept.

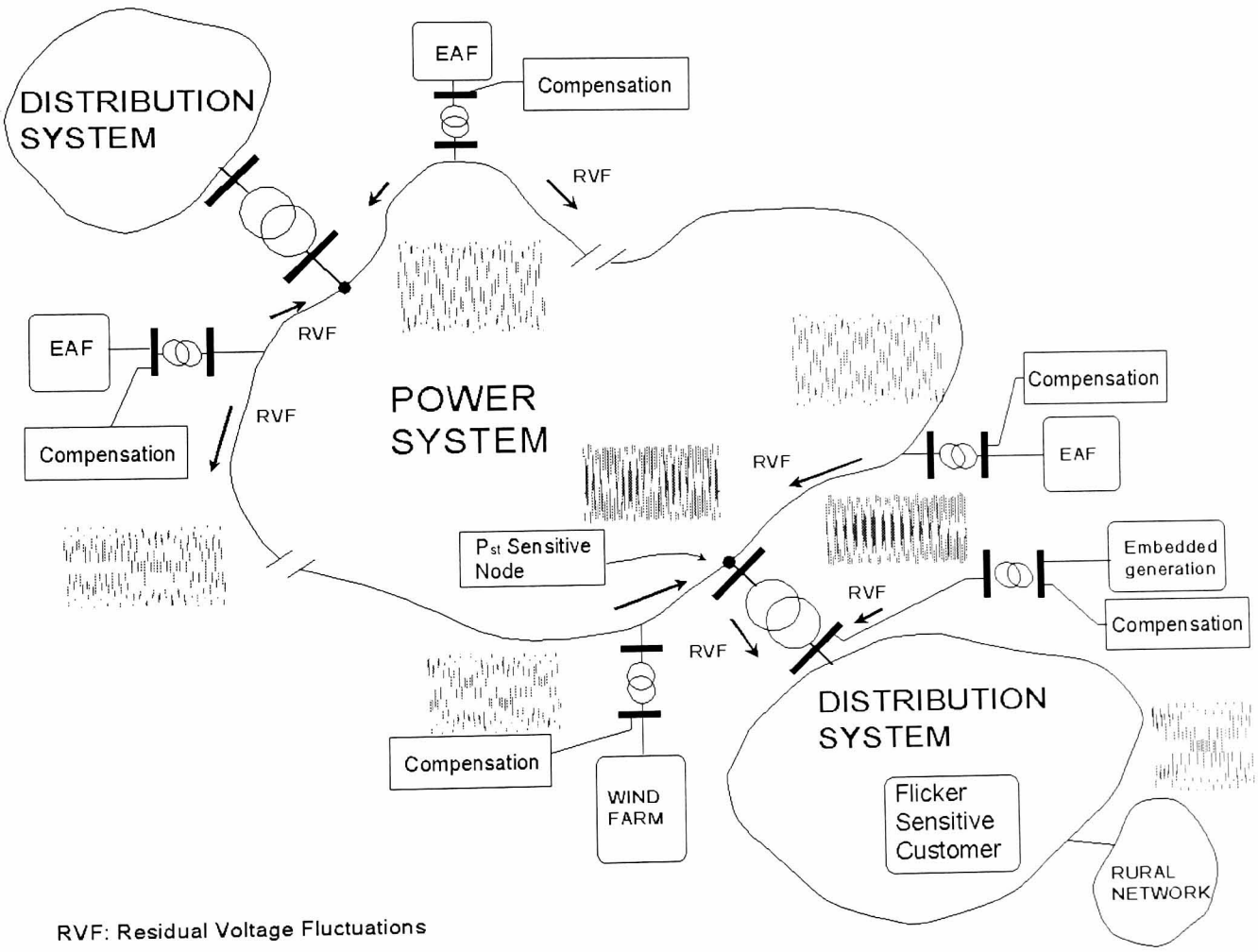


Figure 7.5. Residual voltage fluctuation propagation

RVF injected to the network by various not-perfectly mitigated sources may eventually summate and propagate in the network, increasing the actual P_{st} at certain nodes of the network and, as a consequence, the flicker severity. Such events may lead to increased complaints from sensitive customers. A RVF propagating scenario requires more

research attention. Some shortcomings of shunt mitigation equipment operating in a voltage fluctuation environment are identified below:

- Mitigation of voltage fluctuations is confined to the connecting node.

- The short-circuit ratio between the network-voltage fluctuation source at the connecting point is not incremented in practical terms.

- Negligible capacity to counteract the effective inductive reactance of the power lines where the voltage fluctuations propagate.

- The shunt mitigation equipment is dedicated to a specific voltage fluctuation source, which in cases of many voltage fluctuation sources implies the use of many mitigation equipments. To the best of this author's knowledge, series mitigation schemes to counteract multi-voltage fluctuation sources have not yet been considered in the open literature.

- Information concerning P_{st} reduction in real system, going from pre-mitigation to post-mitigation operating stages, is scarce.

An alternative solution to shunt mitigation equipment and fixed series capacitor banks is the series-connected mitigation controllers. Among the series FACTS controllers, the TCSC has been chosen in this research project as a suitable option to mitigate voltage fluctuations travelling in the network.

TCSC capability to change its apparent reactance has been primarily used to improve transmission systems. Here-to-fore, quite little evidence exists in the open literature in favour or against the use of the TCSC concept in distribution networks applications, including industrial and rural grids. This is an open area of research. The benefits the TCSC controller can bring to the voltage fluctuation mitigation arena are given below:

- Capability to minimise RVF propagating throughout the transmission and distribution network.

- Increase of the short-circuit ratio of the electrical network where the TCSC is series connected. This condition is helpful to alleviate voltage fluctuations mitigation.

- Capability to dynamically modify its effective capacitive compensation in the full range of voltage fluctuations frequencies (25 Hz and 30 Hz for 50 Hz and 60 Hz systems, respectively).

- Capability to minimise P_{st} provoked by multiple voltage fluctuation sources, including embedded generation and DC-EAF. In this environment, a single series mitigation equipment is a potential substitute for various shunt mitigating equipments and, at the same time, it can be used to suppress high levels of residual P_{st}.

- It enables the reduction of the voltage fluctuation amplifying effects, taking place while voltage fluctuations propagates in the network, by means of an effective cancellation of the inductive reactance of the line where the TCSC is connected.

- Capability to operate each phase independently, enabling the controller to mitigate a different P_{st} level in each phase.

- The TCSC characteristics can be planned bearing in mind future expansion of the network to include new fluctuating bulky loads and embedded generation units for instance.

- The TCSC mitigation capabilities can be extended to encompass peculiarities found in distribution systems. It can be used to "isolate" either a local voltage fluctuation source from the rest of grid, or a distribution network from residual P_{st} propagating in the transmission system, or a flicker sensitive customer from a distribution substation having a P_{st} sensitive node directly connected to it.

- Capability for dynamic, smooth or abrupt, line reactance control, by means of tracking down the voltage fluctuation variations.

The TCSC mitigation controller placement in transmission and distribution systems is still an area of research opportunities. Figure 7.6 illustrates three author's proposals for TCSC placement in the network.

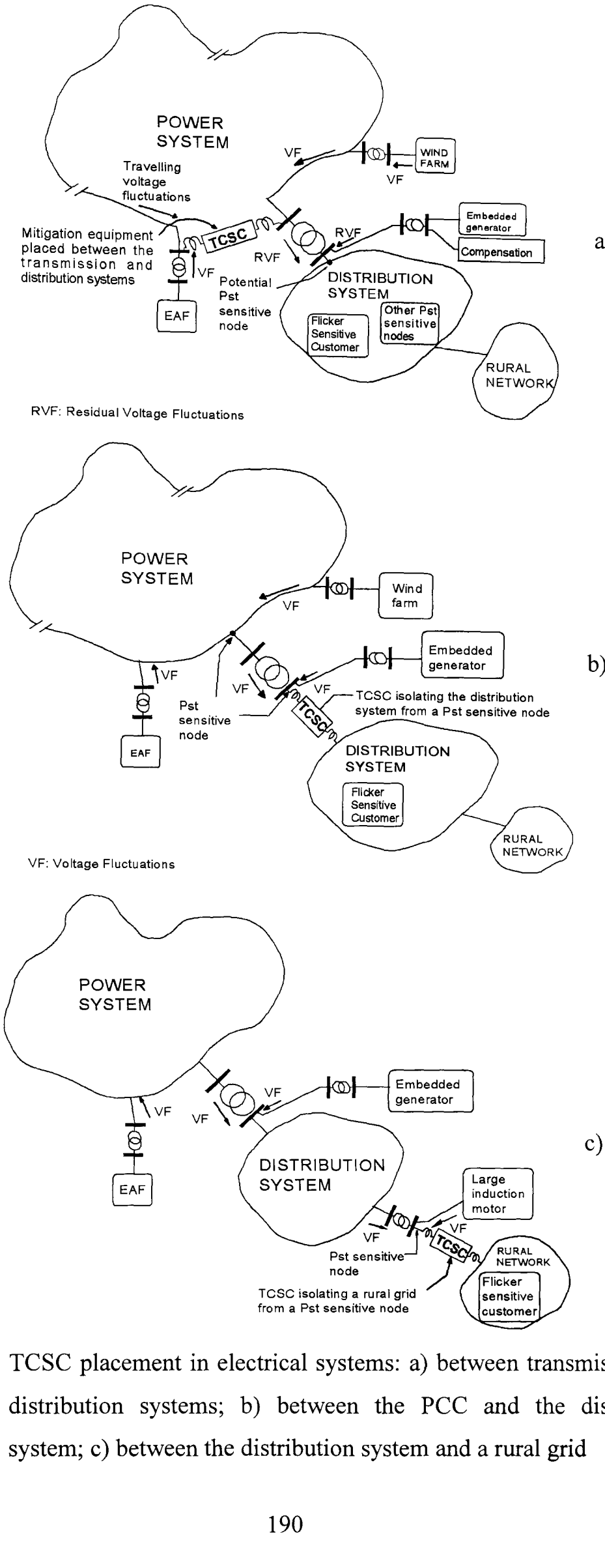


Figure 7.6. TCSC placement in electrical systems: a) between transmission and distribution systems; b) between the PCC and the distribution system; c) between the distribution system and a rural grid

Figure 7.6a shows the TCSC in the transmission system between a heavy voltage fluctuation source and a neighbouring distribution system with high P_{st} in its PCC. In this case the controllers mitigate only the voltage fluctuations travelling to the distribution network.

Figure 7.6b presents the TCSC located between the PCC with P_{st} sensitive node and the distribution system connected to it. In this case, the controller mitigation process "isolates" the distribution feeders from the incoming voltage fluctuations. Similarly, Figure 7.6c shows the TCSC lowering high P_{st} levels from a P_{st} sensitive node in the distribution main feeders in order to ameliorate a rural network.

The TCSC has proven its capacity to modulate the line current. This experience backs up further the application of the controller as voltage fluctuations mitigation equipment.

Additional applicability of the TCSC, or similar series compensation equipment, can be considered for future research projects, such as novel series-shunt VSC-based apparatus, which can use a multi-objective control with two strategies, one of them dedicated to the shunt branch improving the voltage stabilisation performance at the point of common coupling, and the second dedicated to the series branch mitigating residual voltage fluctuations

7.5 REAL TIME MODEL IMPLEMENTATION AND HIL TESTING

The development of real-time system models goes through a series of steps before the final application solution is fully acceptable. Real-time applications development in this research work have involved three main stages: a) design, implementation and initial model simulation on a non-real-time basis; b) open loop, real-time simulations performed in the RTS; c) closed-loop (hardware-in-the-loop) real-time simulations and hardware testing.

A good understanding of ADI and EASY5 simulation software tools and RTS operation characteristics greatly facilitate the design and implementation of the control strategies, reducing also the application development time. Figures 7.7 and 7.8 show the off-line application development and the real-time models and HIL testing procedures as used in this research project.

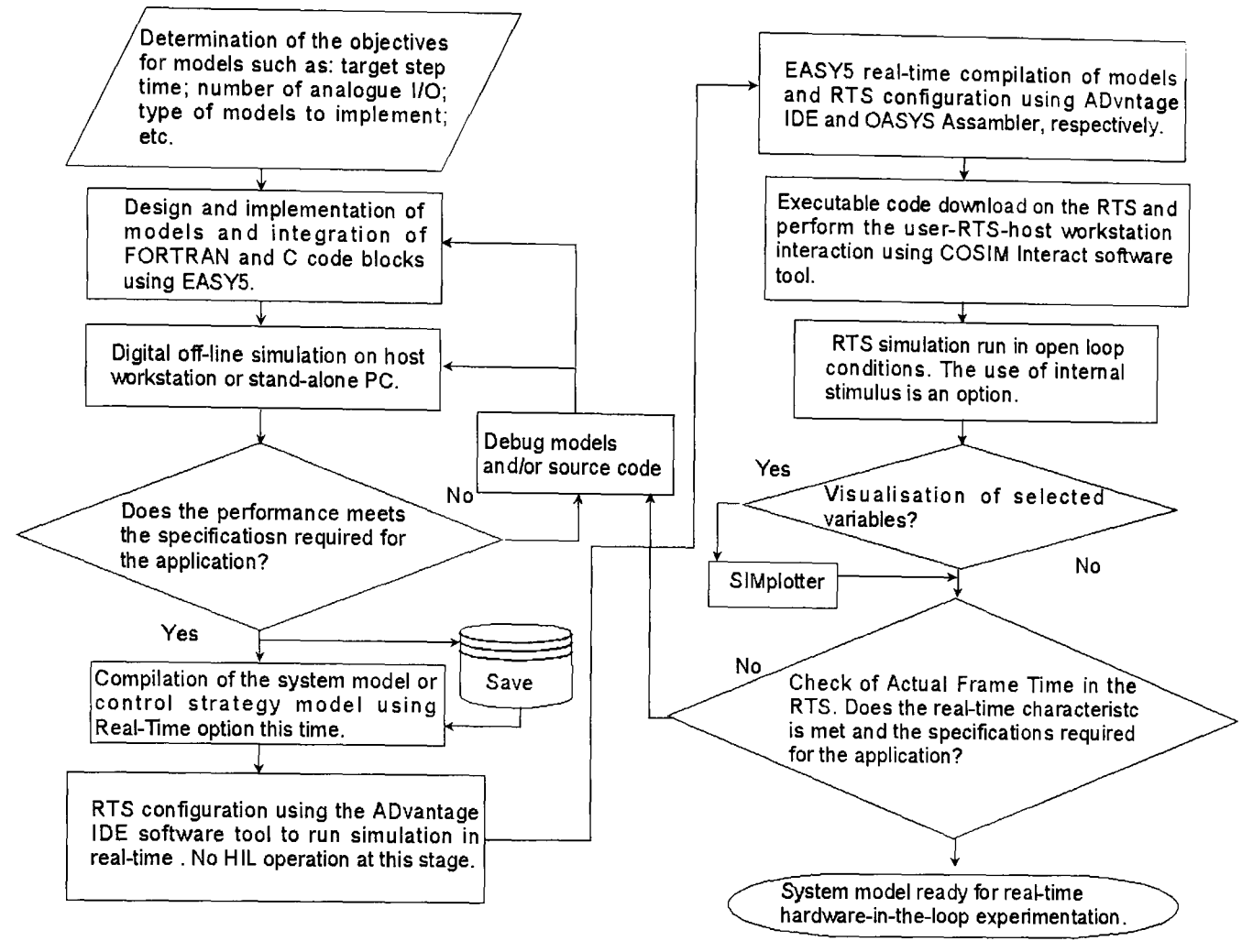


Figure 7.7. Off-line open-loop application development procedure

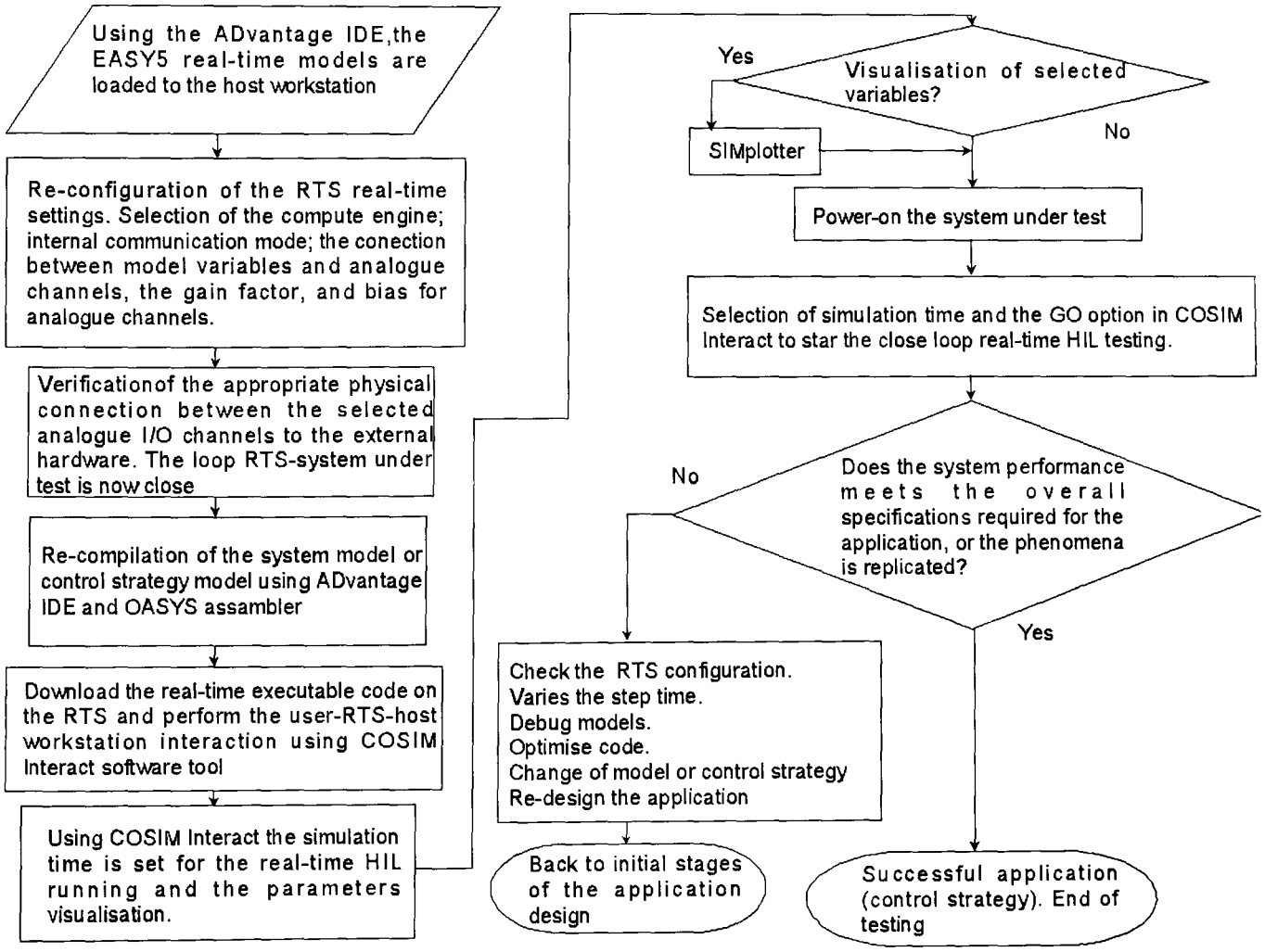


Figure 7.8. Real-time models development and HIL testing

The development of real-time controls may present many difficulties. The first one is the design of the control strategy. The off-line implementation and testing of models using EASY5 is useful to determine if the general open loop control strategy performance is satisfactory. At this stage, the main problems are associated with the implementation and assessment of FORTRAN and C user source code.

In real-time application, a major challenge is to meet the processing step time required for the application. If the value of the AFT parameter is higher than expected, the application should be debugged to comply with real-time

The compiler for real-time execution code is different from the one used for off-line application, the compatibility of the application variables names and types of the tailor-made FORTRAN and C routines, should be double checked to avoid collision in the RTS memory at run time. A general solution for most cases is to clearly declare all variables, and use the EASY5 'force explicit typing' option when compiling. This procedure compels the compiler to verify all variables, by converting local variables to global ones, and checking for repeated names.

The RTS should be configured, linking models with analogue input and output channels, before the real-time HIL start. The number of internal parameter options of the RTS is very large, which make the RTS configuration a time consuming task at application debugging stage.

7.6 REAL-TIME VIRTUAL IEC-FLICKERMETER AND SEVERITY INDICES EVALUATION

7.6.1 General Structure

The mitigation strategy and equipment performance evaluation requires the measurement of the instantaneous flicker sensation and P_{st}. In this research project, a real-time virtual IEC-Flickermeter instrument has been implemented based on the standard IEC-61000-4-15. The main virtual flickermeter functional blocks are shown in Figure 7.9 and Figure 7.10 shows the IEC-Flickermeter made up with EASY5 models.

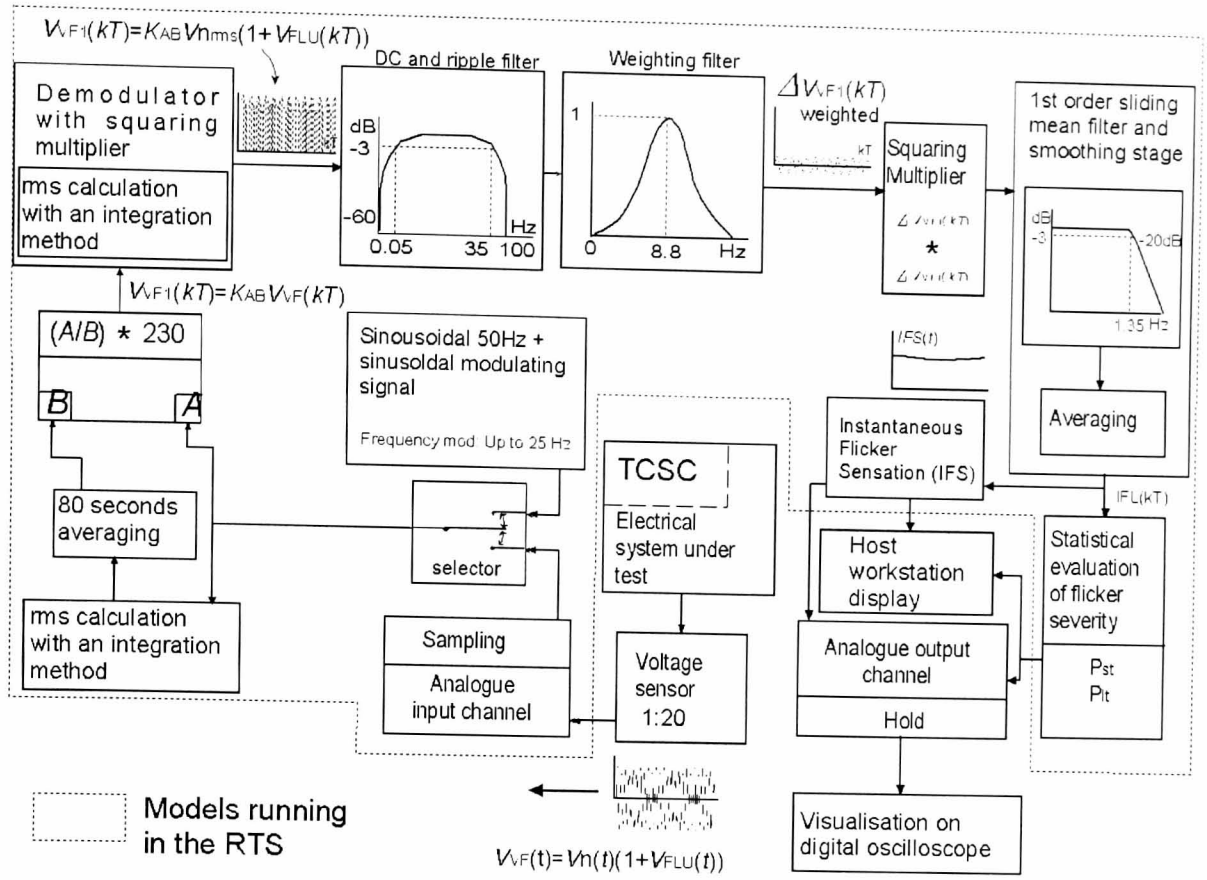


Figure 7.9. Virtual IEC- Flickermeter functional blocks

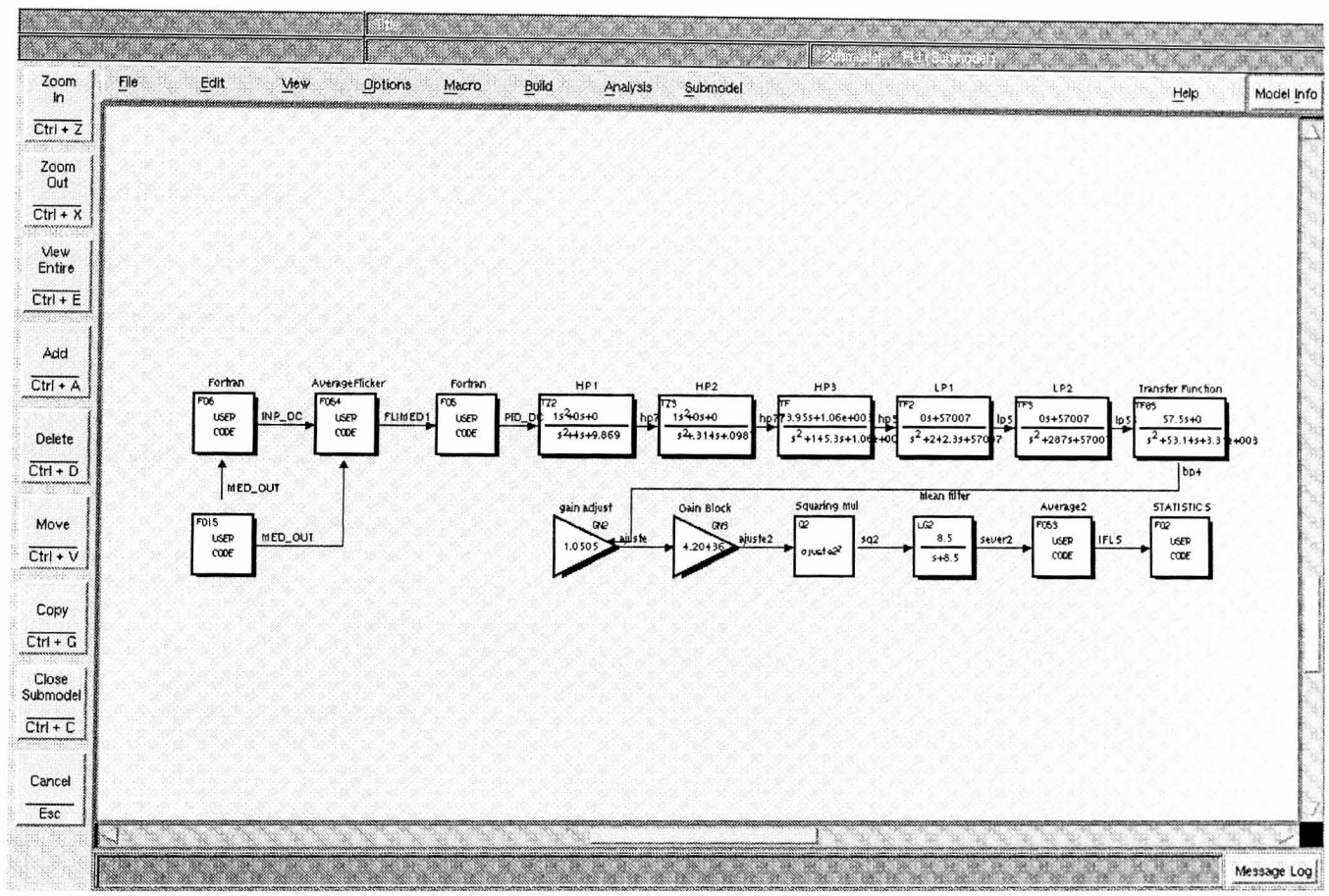


Figure 7.10. Virtual IEC-Flickermeter EASY5 models

Most models have been constructed using EASY5 built-in blocks, with three exceptions: a) the input interface and control gain block; b) the rms calculation of the input; and c) the P_{st} and P_{lt} calculation block. The FORTRAN routine for calculating the severity index measured by the virtual instrument is included in Appendix C.

7.6.2 Real Time Virtual IEC-Flickermeter: Structure Description.

The real-time virtual IEC-Flickermeter comprises two major stages: a) measurement of IFS; b) evaluation of flicker severity indices for both the short-term severity, P_{st}, and the long-severity index, P_{lt}. As mentioned before, the virtual instrument implementation is fully based on the functional block diagram and the principal guidelines stated in standard IEC-61000-4-15, but with four minor variants, which are explained below:

- A signal average block is inserted before the flicker level statistical evaluation block. The signal averaging smoothes further the IFS output, acting as a low-pass filter. It should be remarked that this block does not deteriorate the overall performance of the instrument.
- The range selector is not included.
- The IFS and P_{st} are the only two outputs implemented.
- As the Flickermeter is not physically constructed, the tests specified in Section 6 of the standard have not been carried out.

7.6.3 Measurement of the Instantaneous Flicker Sensation

Three main stages are involved in IFS measurements: 1) calibrating waveform generation; 2) signal adaptation to an internal reference, 3) DC-ripple filtering and weighting filter. The flow diagram describing IFS processing is presented in Figure 7.11

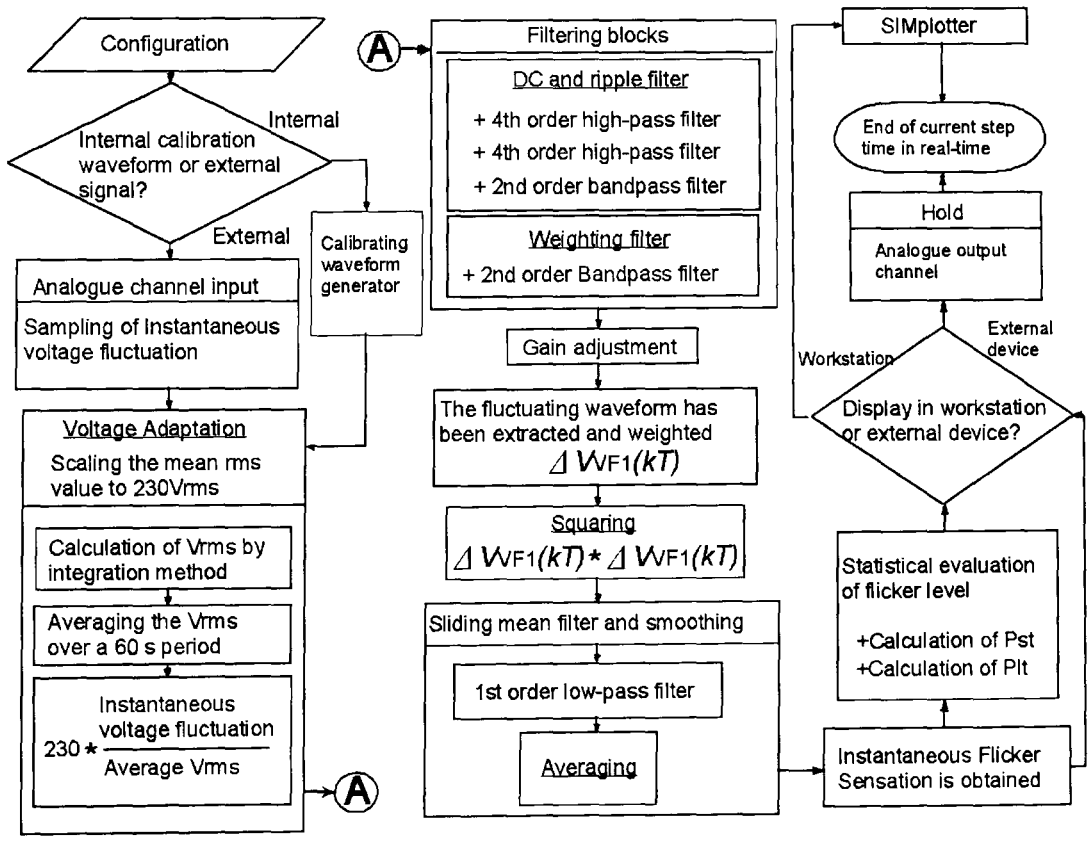


Figure 7.11. IFS flow diagram

A built-in signal generator block produces a fluctuating waveform which is used to adjust the precise instrument operation. In a typical calibration procedure, a number of tests are performed, which consist of injecting a reference waveform to the input block and observe the IFS measured by the IEC-Flickermeter. The instrument output is then compared with the normalised flickermeter response provided by the IEC-61000-4-15 standard. A flickermeter complies with the calibration requirements if the tested IFS and the normalised values have an average error not greater than 5%. This is the case for the virtual IEC-Flickermeter implemented in this research work.

The IFS calculation process, showed in Figure 7.11, initiates by sampling the input voltage fluctuation at 2 k samples/s. The signal magnitude conditioning to 230 V rms is carried out in four steps: a) calculation the rms using an integration method; b) averaging the rms calculated in a) over on 80 seconds period; c) dividing the instantaneous input values by the actual averaged rms, d) multiplying the previous result by 230.

The resulting signal is a normalised waveform, which preserves the ratio between the mean rms value of the input signal and the peak-to-peak fluctuations magnitude. Additional processing of the signal continues in the DC and ripple filtering and weighting filter blocks. The combination of a 4^{th} order high-pass filter, a 4^{th} order low-pass filter, and a 2^{nd} order bandpass Butterworth filter are used to suppress the dc component and the spurious 100 Hz ripple deviations. The implemented DC-ripple filtering block transfer blocks, which are not provided by the standard, are given below:

$$F_{HP}(s) = \left[\frac{S^2}{S^2 + 4S + 9.869}\right]\left[\frac{S^2}{S^2 + 0.314S + 0.987}\right] \quad \text{High-pass filter block} \qquad (7.1)$$

$$F_{LP}(s) = \left[\frac{57007}{S^2 + 242.3S + 9.869}\right]\left[\frac{57007}{S^2 + 287S + 0.987}\right] \quad \text{Low-pass filter block} \qquad (7.2)$$

$$F_{BP}(s) = \left[\frac{73.95S + 1.06e3}{S^2 + 145.3S + 1.06e3}\right] \quad \text{Bandpass filter block} \qquad (7.3)$$

At the end of the filtering stage, the signal is processed by a weighting filter, which is used to simulate the frequency response to sinusoidal voltage fluctuations of a coiled filament 60W-230V gas-filled lamp, combined with the human visual system.

A suitable transfer function is provided by the IEC-61000-4-15 standard. Nevertheless, as the DC-ripple filtering block slightly influences the frequency bandwidth and amplitude response, the transfer function stipulated in the standard is slightly modified for the purposes of the virtual IEC-Flickermeter. Equation 7.4 shows the final weighting transfer function implemented.

$$F_{BP}(s) = \left[\frac{57.5S}{S^2 + 53.14S + 3.31e3} \right] \qquad \text{Weighting Filter} \qquad (7.4)$$

The tuning process for the DC-ripple filtering transfer functions has been carried out following by an iterative simulation-debugging procedure. The weighting filter output represents the ac fluctuating waveform which modulates the system line voltage. The instantaneous flicker sensation is obtained at the end of three more processing blocks: a) a squaring signal; b) a first order low-pass filtering; and c) a mean signal averaging. The first two blocks simulate the non-linear eye-brain perception and the storage effect in the brain, respectively. The last block limits the bandwidth of the IFS to low frequencies. The actual IFS measurement can be displayed in the host workstation or sent to an RTS analogue output channel.

7.6.4 Statistical Evaluation of the Flicker Level

The statistical evaluation of flicker focuses in the determination of the short-term severity index, P_{st}, and the long-term severity index, P_{lt}. These two indices are calculated taking samples of IFS over a period of 10 minutes. The calculation comprises various statistical computations. The key blocks are the probability density function classifier-tree and the percentiles estimator needed for the P_{st} evaluation. Statistical operations, such as the classifier-tree for instance, are not clearly explained in the IEC-61000-4-15 standard. On the contrary, equations for P_{st}; P_{lt}; smoothing percentiles; and percentiles interpolation all fully detailed. The statistical evaluation process is detailed in the flow diagram shown in Figure 7.12.

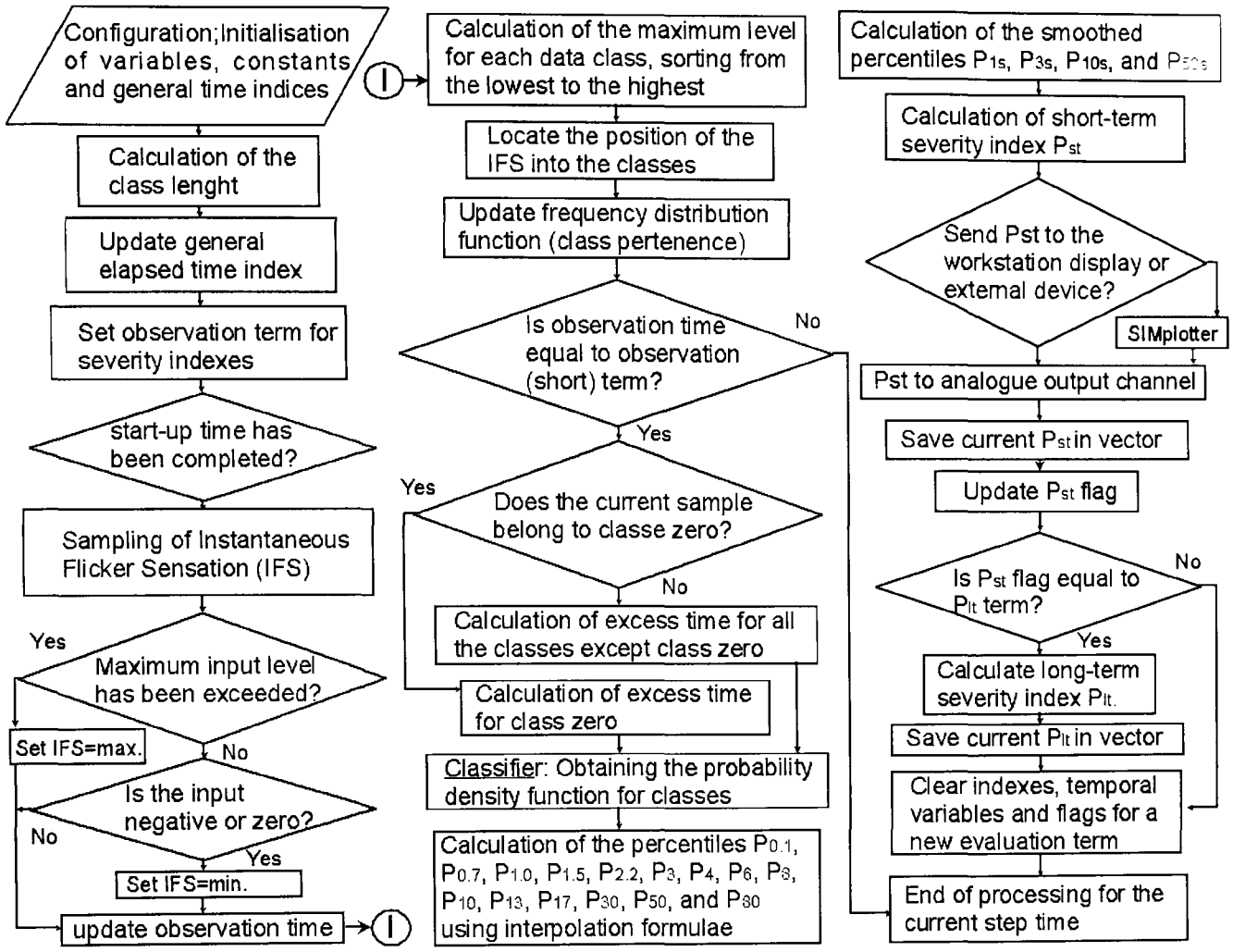


Figure 7.12. Flow Severity indexes statistical evaluation flow diagram

7.7 REAL-TIME EXPERIMENTAL EVALUATION OF VOLTAGE FLUCTUATION MITIGATION AND REDUCTION OF P_{ST}

A comprehensive number of real-time experiments have been carried out in order to assess the TCSC dynamic performance in a voltage fluctuations environment and the capacity of this controller to mitigate voltage fluctuations suppression.

The scaled-down, real-time test-bed has been implemented bearing in mind the following two cases:

a) Voltage fluctuations in the transmission system affecting a distribution system

b) Voltage fluctuations in distribution network feeders affecting a circuit node in that network

In a pre-mitigation scenario, both cases assume that travelling residual voltage fluctuations with P_{st} higher than one, created by a fluctuating bulky load in the vicinity, produce a P_{st} sensitive node. It is also assumed that this node has a P_{st} sensitive load connected to it, resulting in a flicker sensitive customers. Under such conditions, the TCSC mitigates voltage fluctuations, lowering P_{st}.

In a post-mitigation scenario, the P_{st} is low enough to relieve the P_{st} sensitive node. The TCSC is tested over the full range of sinusoidal and rectangular voltage fluctuations (0-25Hz), covering low frequency voltage fluctuations sources, such as wind farms, and full-range voltage fluctuations sources, such as EAFs.

Figure 7.13 shows the one-line diagram of the electric system implemented in laboratory and the real-time testing environment for cases a) and b). Figures 7.14 and 7.15 illustrate the real-time test-bed one-line diagram to recreate rectangular and sinusoidal voltage fluctuation environments, respectively.

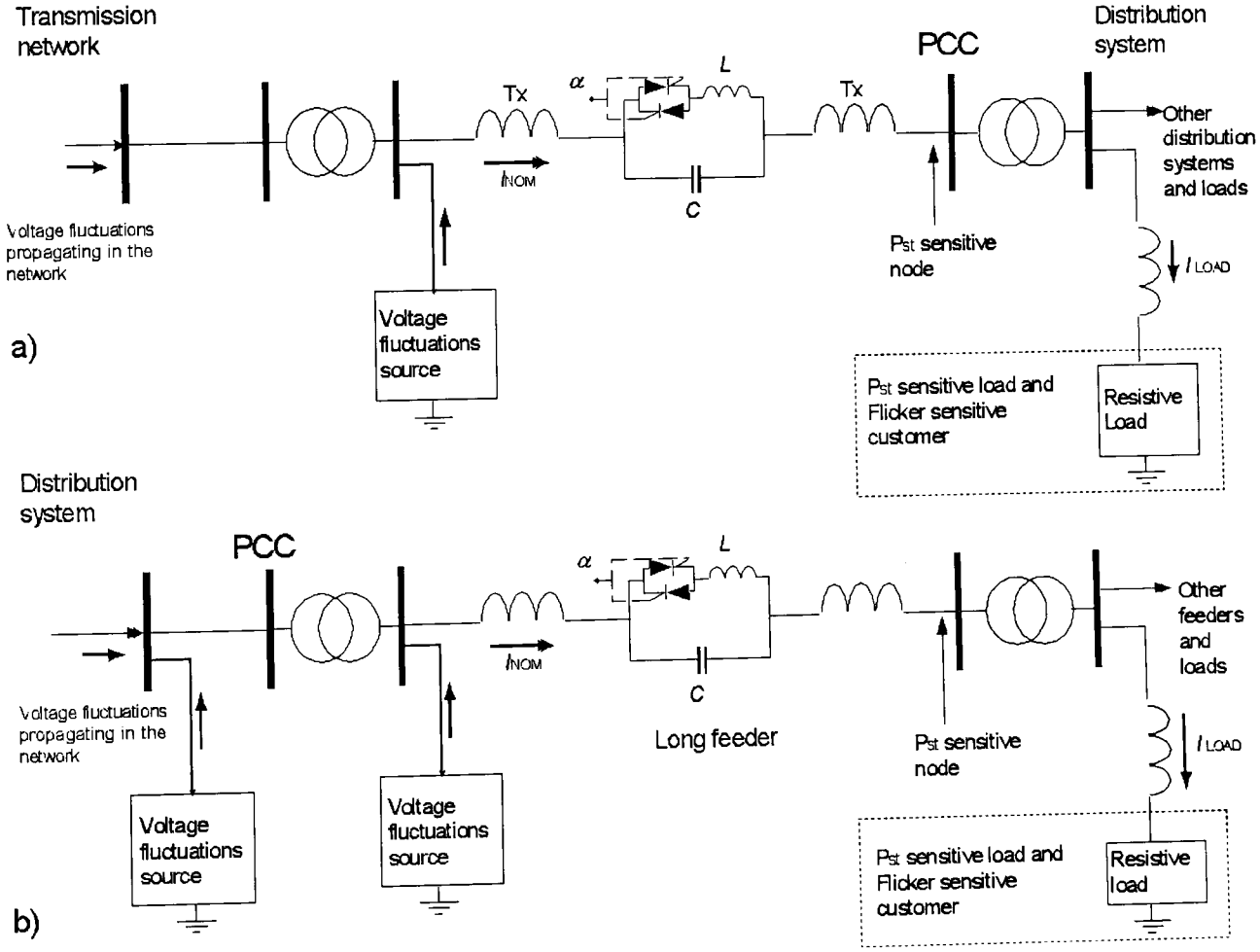


Figure 7.13. Electrical system under test, one-line diagram: a) residual voltage fluctuations travelling to a distribution system; b) residual voltage fluctuations injected to a P_{st} sensitive load located in the same distribution system

Figure 7.13a illustrates the case of voltage fluctuations, provoked by a bulky fluctuating load, travelling in a transmission system. The phenomena produce a P_{st} sensitive node in the neighbouring distribution system, affecting a P_{st} sensitive load and customer, as has been indicated in Figure 7.13 a. As the visual phenomenon of voltage fluctuation is not part of this research, the P_{st} sensitive load is represented only by a power resistor. The TCSC is located between the voltage fluctuation source and the distribution system. The most suitable voltage fluctuation source for this case is the EAF.

Voltage fluctuations originated and affecting the same distribution system are shown in Figure 7.13b. In this case the TCSC is placed between the voltage fluctuating source and the P_{st} sensitive node. Residual voltage fluctuations may also affect the distribution system; this is indicated in the diagram with an additional voltage fluctuation source block. Similar to Figure 7.13a, the P_{st} sensitive load is represented with resistive load block.

The real-time experimental environment at laboratory used for all the mitigation cases carried out in this research has been fully detailed in Chapter 6. Figures 7.14 and 7.15 illustrate two main set-ups for HIL testing.

Figure 7.14 shows the scaled-down electrical and TCSC prototype; the RTS in HIL with the TCSC; the power resistive fluctuating load and waveform generator, which represent a voltage fluctuations source; the P_{st} sensitive load; and the measurement equipment blocks. The testing environment is fed by 440 V main line using a set of transformers. The voltage fluctuation source is connected in the secondary winding, in order to inject high fluctuations in the electrical system under test and produce a P_{st} sensitive node. The voltage fluctuation source blocks are not in hardware-in-the-loop with the RTS, so it does not have any control over the source behaviour. Using this scheme, the electrical system shown in Figure 7.13 is subjected to non-sinusoidal voltage fluctuations.

The scheme showed in Figure 7.15 shares the same functional blocks than Figure 7.14, except for blocks of the voltage fluctuation source. In this case, the voltage amplifiers and a waveform generator are used to inject sinusoidal voltage fluctuation to the electrical system under test shown in Figure 7.13.

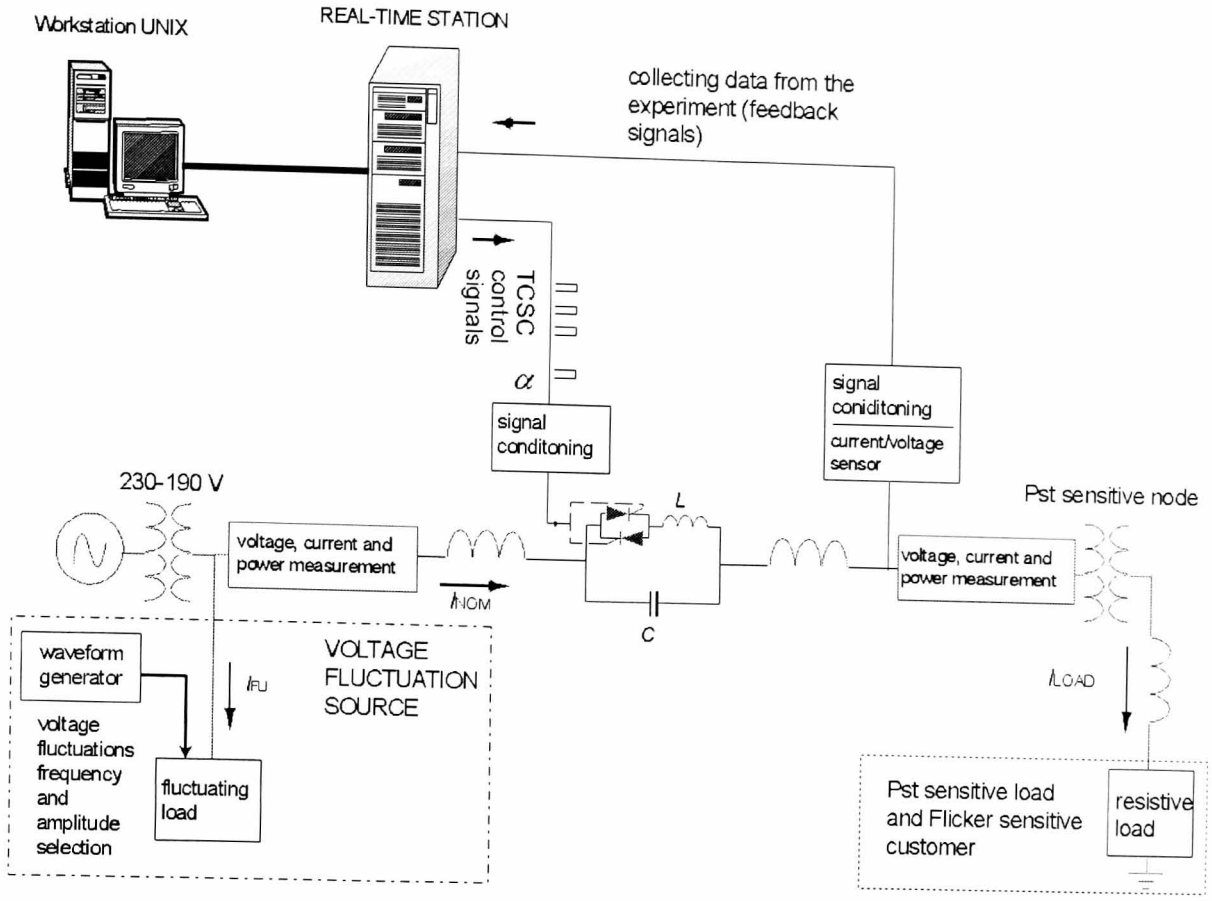


Figure 7.14. Real-time experimental-bed setup at laboratory for non-sinusoidal voltage fluctuations testing

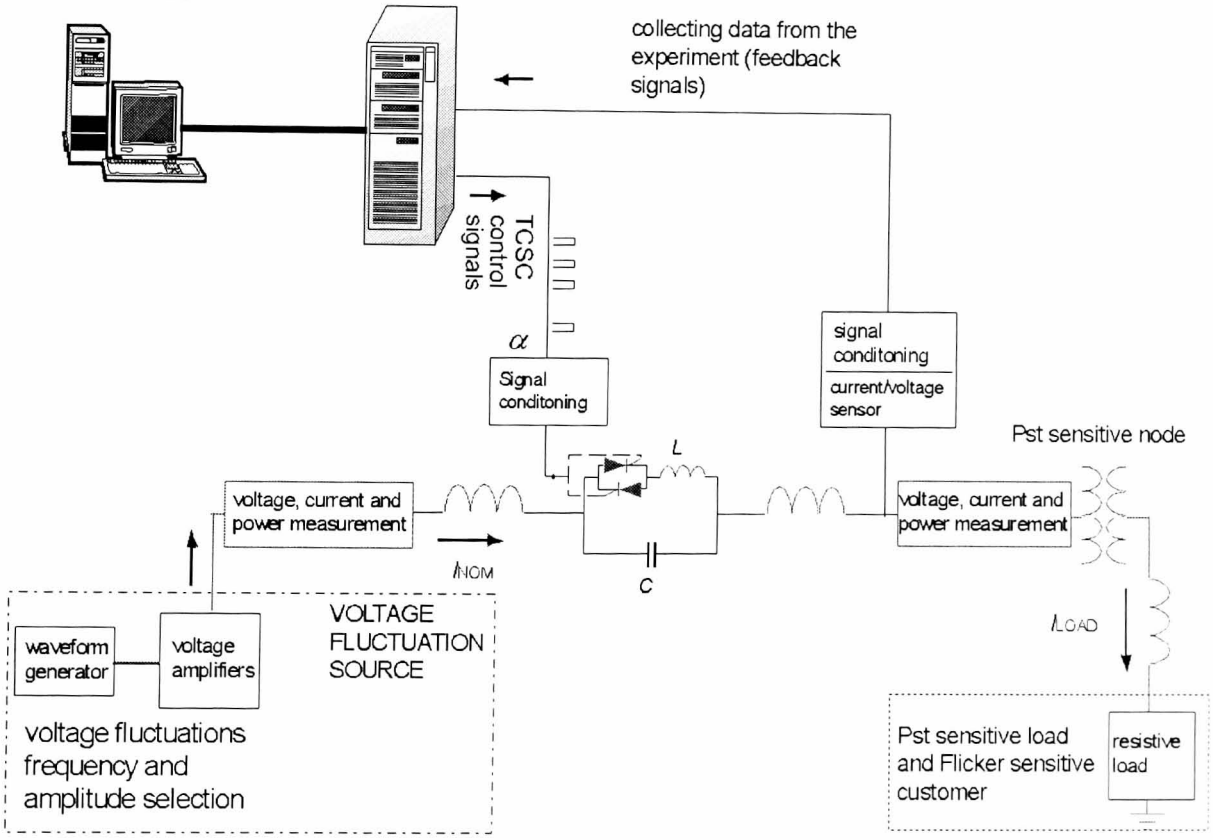


Figure 7.15. Real-time experimental-bed setup at laboratory for sinusoidal voltage fluctuations testing

Table 7.1 gives representative experimental results illustrating the TCSC mitigating capacity. On the other hand, Table 7.2 shows the mitigation factors for non-sinusoidal

voltage fluctuations. For completeness, selected mitigation factors achieved with a series non-controlled capacitor given in Table 7.3.

Table 7.1 TCSC mitigation factor for sinusoidal voltage fluctuations

Voltage fluctuations frequency (sinusoidal)	Pre-mitigation P_{st}	Post-mitigation P_{st}	Voltage fluctuations mitigation factor (*VFMF*)	Inverse VFM (1/*VFMF*)
1	1.2	0.960	0.800	1.248
2	1.1	0.955	0.868	1.151
3	1.2	0.933	0.777	1.285
4	1.35	0.932	0.690	1.447
5	1.25	0.782	0.625	1.597
6	1.45	0.896	0.618	1.617
7	1.65	0.925	0.561	1.782
8	1.2	0.800	0.667	1.498
8.8	1.75	0.976	0.558	1.792
10	1.3	0.784	0.603	1.657
11	1.3	0.745	0.573	1.743
12.5	1.8	0.903	0.502	1.991
15	1.45	0.874	0.603	1.658
20	1.6	0.922	0.576	1.734
24	1.4	0.928	0.663	1.507
25	1.1	0.929	0.844	1.183

Table 7.2 TCSC mitigation factor for non-sinusoidal voltage fluctuations

Voltage fluctuations frequency (rectangular)	VFMF
1	0.854
15	0.763

A number of carefully conducted real-time experiments have been useful to assess the TCSC's voltage fluctuations mitigation capabilities. Table 7.1 presents pre-mitigation and post-mitigation P_{st} values together with the named Voltage Fluctuation Mitigation Factor (*VFMF*), which is given by the post-mitigation P_{st}/pre-mitigation P_{st} ratio equation.

$$VFMF = \frac{\text{Post-mitigation factor}}{\text{Pre-mitigation factor}} \qquad 7.1$$

Although the TCSC mitigation is good enough all over the voltage fluctuations frequency range, it should be noticed that the network improvement is more effective in the 4 to 20 Hz frequency range. This effect can be explained by considering that a great

deal of the TCSC capacitive compensating capacity take place close to the triggering control signal zero-crossing instants, where the controller rapidly transits from one triggering angle to another, and the intrinsic underdamped transitory overshoot effects of the controller appears (the TCSC behaves as a second order system, as has been explained in chapter 5).

Figure 7.16a indicates the point where the TCSC overshoots occurs. This overshoot fits well in the temporal regions where the fluctuating rms is more depressed, helping to even the line voltage and current and maximising the TCSC mitigation. The overall TCSC effect is a significant reduction of P_{st}. However, at voltage fluctuations frequencies below 4 Hz, the TCSC transitory overshoot is not longer sufficient to cover the region of fluctuating rms voltage, which is more depressed. Hence, its effects are less significant than at higher frequencies. In this case, the P_{st} is also significantly reduced but with lower *VFMF*.

At voltage fluctuation frequencies higher than 20 Hz, the TCSC mitigation capacity is not as high as in the 4 to 20 Hz range. Two main reasons can be found to explain this condition: a) the rapidly changing nature of the TCSC modulation prevents it from taking full advantage of the controller's transitory overshoot; and b) the TCSC is not triggered at some line voltage zero-crossings, and so, some rms deviations are not fully compensated, which for implies lower *VFMF*.

EAF produces voltage fluctuations in the 0-25 Hz frequency range, whereas wind farms produce the more significant fluctuations at frequencies lower than 5 Hz, as it has been explained in Chapter 2. In both cases the TCSC is a realistic solution to mitigate voltage fluctuations resulting from the combined effect of the two sources. It should be mentioned that the TCSC dynamic operation can be improved to further reduce low frequency voltage fluctuations.

The best mitigation performance achieved by the fixed capacitor is at frequencies lower than 10 Hz, as can been seen in Table 7.3. It is important to mention that, at any voltage fluctuations frequency, the TCSC mitigation capacity clearly surpassed the best performance of the fixed capacitor. However, the fixed capacitor is a far less costly piece of equipment than the TCSC, and it can be an option in installations mainly affected by frequencies lower than 10 Hz with a P_{st} sensitive node having a P_{st} value higher than one.

Table 7.3 Fixed capacitor mitigation factor for sinusoidal voltage fluctuations

Voltage fluctuations frequency (rectangular)	VFMF
1	0.893
2	0.885
4.54	0.931
5	0.914
8.8	0.900
10	0.960
17	0.962
20	0.886

In general the three main TCSC capabilities which are most significant in voltage fluctuations mitigation process are:

a) The effect of the TCSC dynamic modulation

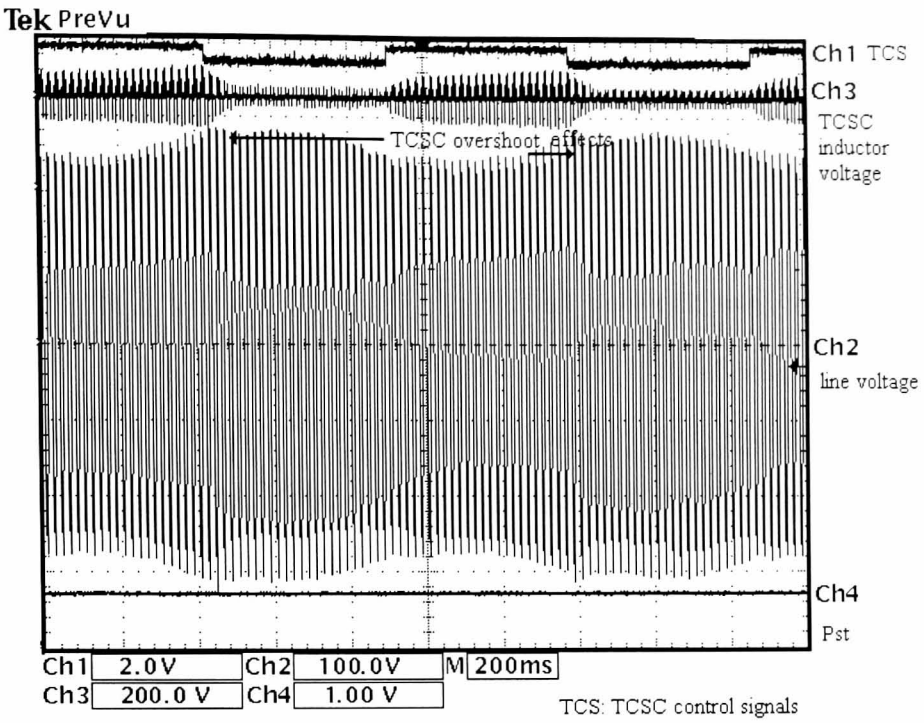
b) The effect of the TCSC series fixed capacitor

c) The TCSC apparent capacitive behaviour

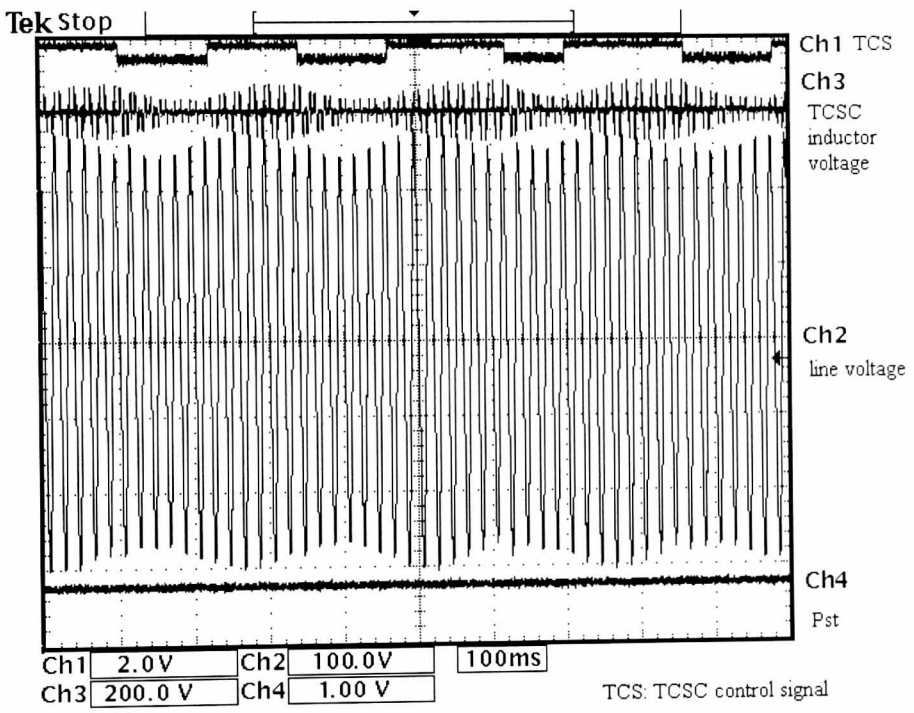
In the open literature, abundant reference to voltage fluctuation mitigation equipment may be found. However, only very few sources include actual P_{st} measurements and these are associated with shunt mitigation equipment. In particular, Grünbaum et al [5,6] reports a mitigation factor close to 3 using a SVC-light©. In this case the equipment is installed to deal with a single voltage fluctuations source, a single P_{st} reduction factor is provided, and the mitigation capacity of the equipment at various voltage fluctuations frequency ranges is not given. The mitigation factor obtained using the SVC-light© is higher than the one obtained using a TCSC. The reason for this is due to both the SVC-light© higher modulation flexibility, making use of IGBT, and its capability to compensate active and reactive power [7].

On the other hand, the very great advantage of TCSC as series mitigation equipment is that it can be used to mitigate residual voltage fluctuations propagating in the network at broader voltage fluctuation frequency range and it could be used in a wide area voltage fluctuations mitigation scheme. However, as have been previously mentioned, the TCSC mitigation performance should be improved at frequencies below 4 Hz and above 20 Hz in order to raise the *VFMF*.

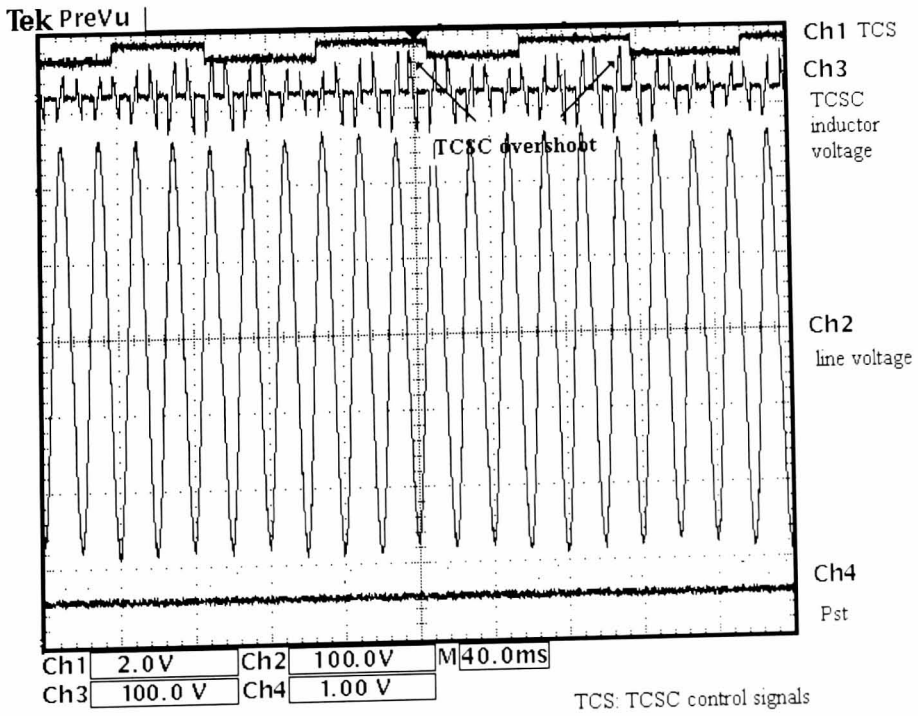
a)



b)



c)



Figures 7.16. Post-mitigation voltage fluctuation scenario for various frequencies: a) 2 Hz; b) 8.8 Hz; c) 20 Hz

Figures 7.16 illustrate the voltage fluctuations waveforms observed in a post-mitigation scenario. The explanation for the set of figures is as follows:

Figure 7.16 shows the voltage line fluctuating at 2 Hz, 8.8 Hz, and 20 Hz; the TCSC control signal from the RT-DIMR; the TCSC inductor voltage; and the P_{st}. The highest compensation period occurs in the vicinity of the TCSC transition, in particular when the triggering angle is changed from a point closer to fundamental resonance mode to 180°. Figures 7.16a and Figure 7.16c shows the TCSC overshoot points, where the transitions occur.

As can be depicted in TCSC inductor waveforms of Figure 7.16, the TCSC is triggered close to the resonance to achieve high compensation, in order to allow higher line current levels where the voltage is more depressed. As a consequence, the voltage fluctuation is smoothed and the P_{st} lowered. The TCSC high to low compensation transitions, or vice versa, follows the frequency of the line voltage fluctuations, which is a relevant characteristic of the RT-DIMR control, as has been fully detailed in Chapter 5. Figure 7.16 also illustrates the TCSC inductor voltage following the line voltage fluctuations.

The experimental results presented in Tables 7.1, 7.2 and 7.3, and the waveforms in Figure 7.16 confirm the effectiveness of the TCSC and RT-DIRM control strategy to perform well as voltage fluctuations mitigation equipment. It should be mentioned that more than 200 real-time experiments have been carried out in this section in order to repeatedly verify the TCSC performance.

7.8 FUTURE APPLICATIONS

The research contributions presented in this chapter may be used as basis for further developments, aiming at providing continuous improvements needed by modern electrical power systems. They can also be used as the starting point for establishing new research objectives.

The set of control and hardware tools developed in this research work have permitted the TCSC to operate as voltage fluctuations mitigation equipment, opening new research opportunities in distribution systems with embedded generation, in particular systems with a significant contribution from wind energy sources.

As demonstrated in this chapter, the basic TCSC mitigates well the voltage fluctuations, but it is clear that many benefits can be obtaining from additional operational flexibility, enabling also the implementation of more sophisticated abnormal phenomena countermeasures.

The following are some of the author's proposals developing further more advanced controllers to be used in tomorrow's distribution and industrial electrical systems:

- Development of a Flexible Custom Series Controller (FCSC) based on high-speed power electronic devices. Among the various characteristics which should be presented in the new equipment is the dual inductive-capacitive impedance behaviour of the TCSC. A schematic design of the proposal is shown in Figure 7.17.

  Figure 7.18 illustrates a possible placement site for the equipment, linking a transmission and a distribution network.

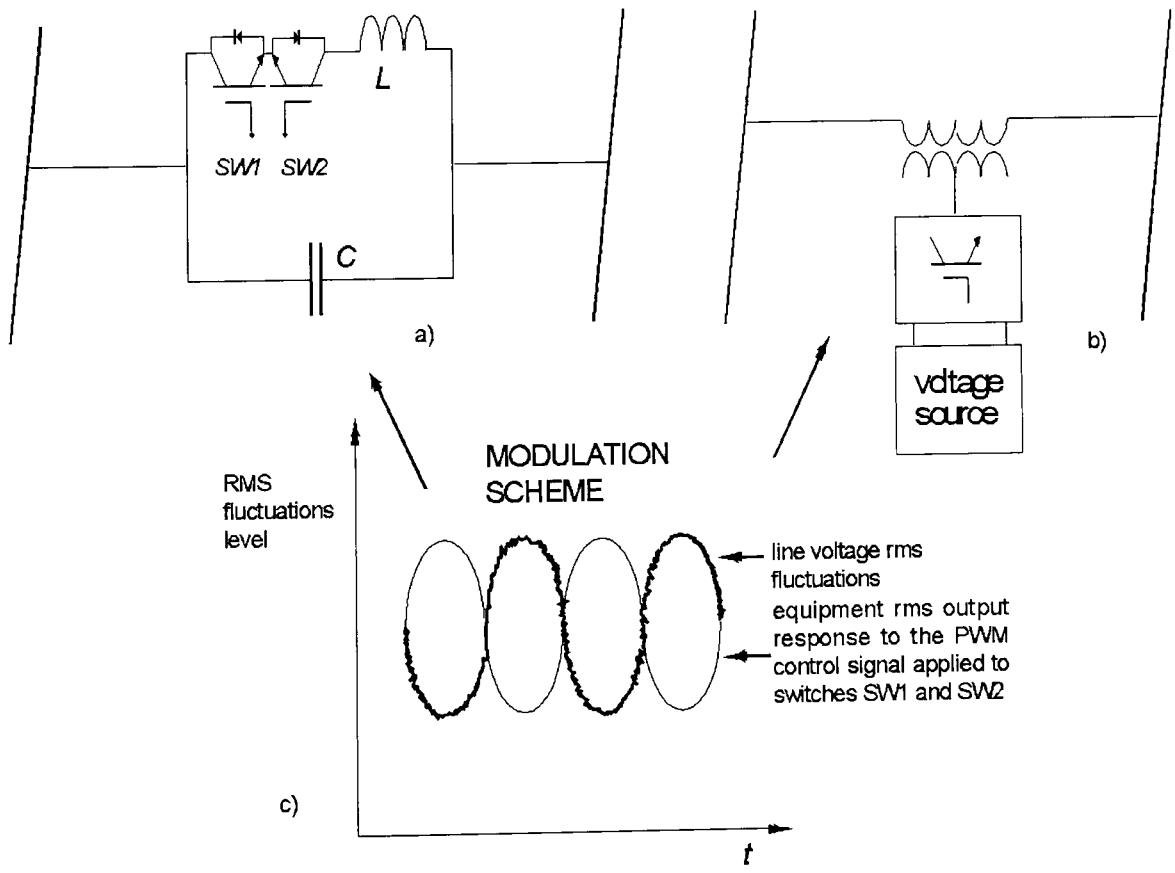


Figure 7.17. Flexible Custom Series Controllers (FCSC): a) FCSC controller for reactive compensation only; b) DVR-type controller for compensating active and reactive power

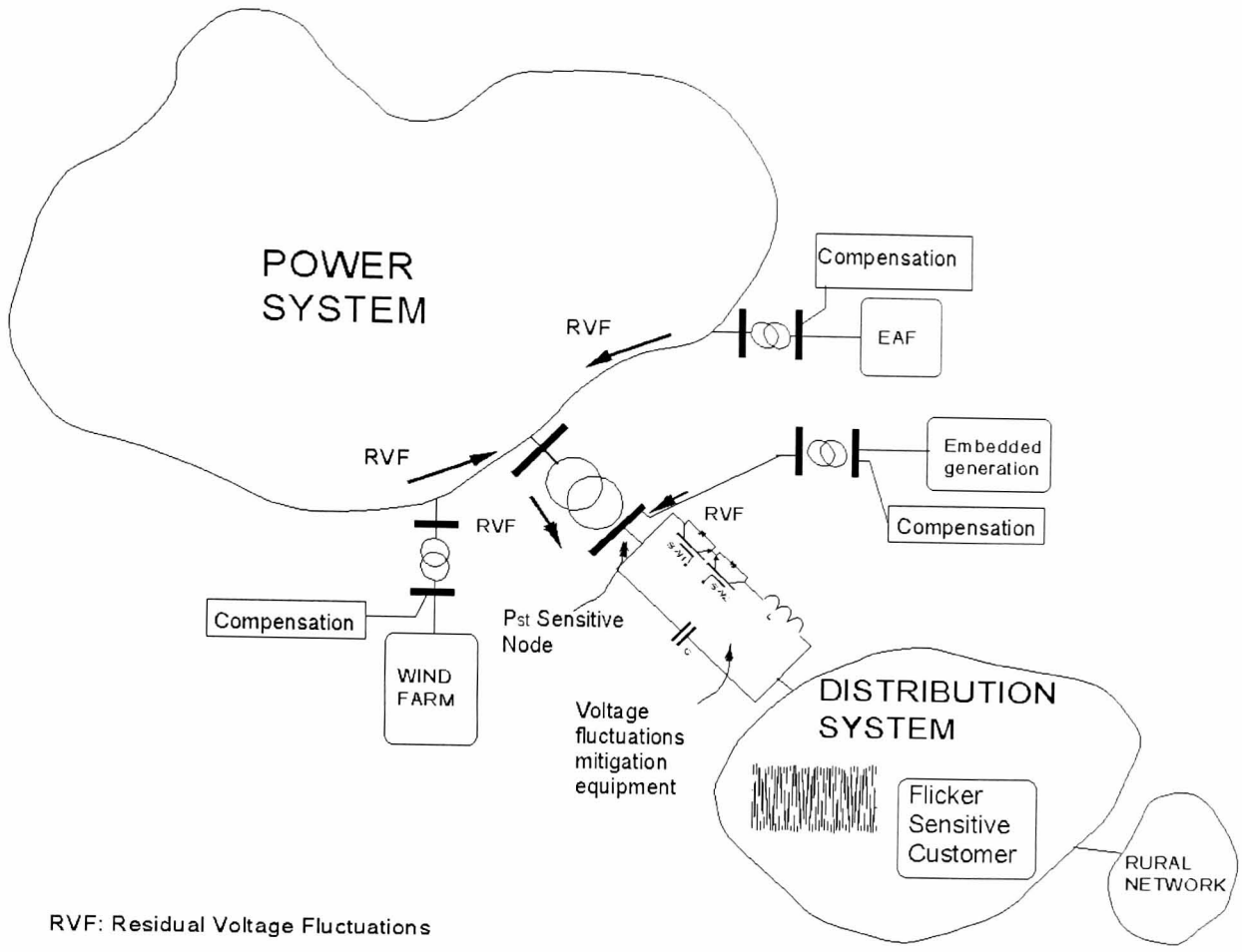


Figure 7.18. Suitable location for the FCSC

Figure 7.17a shows a controller proposed to behave as the TCSC does, but with an additional capability to change its impedance at points different from the zero-crossing, making the compensation more flexible. As thyristors, in particular the SCR cannot be realistically forced to turn-off, and they cannot be switched on and off at high speed, the original TCSC thyristors should be replaced by IGBTs, which present a better performance for the controller intended application.

A TCSC-type controller should be more capable of mitigating voltage fluctuations in all the 0 to 25 Hz range, in particular at those frequencies where the mitigation capacity of the original TCSC is lower (0-4 Hz and 20-25 Hz), as has been detailed in Section 7.7. The use of IGBT also can allow also the implementation of more complex multi-switching modulation scheme, intended to smooth further the line voltage fluctuations. Figure 7.17c illustrates a modulation scheme for FCSC. In this case the modulation inversely follows rms fluctuations in order to average the line voltage around its nominal value.

Figure 7.17b shows a DVR-type controller, which can be used if absorption and injection of active and reactive power is required. The selection between controllers for a given application should be investigated further.

- Development of a dual shunt–series flexible controller for distribution system applications, including its digital protection and multi-objective control strategy, committed to both residual P_{st} suppression and voltage stabilisation at PCC. Figure 7.19 shows the schematic design of the proposal using the controller's configuration previously detailed.

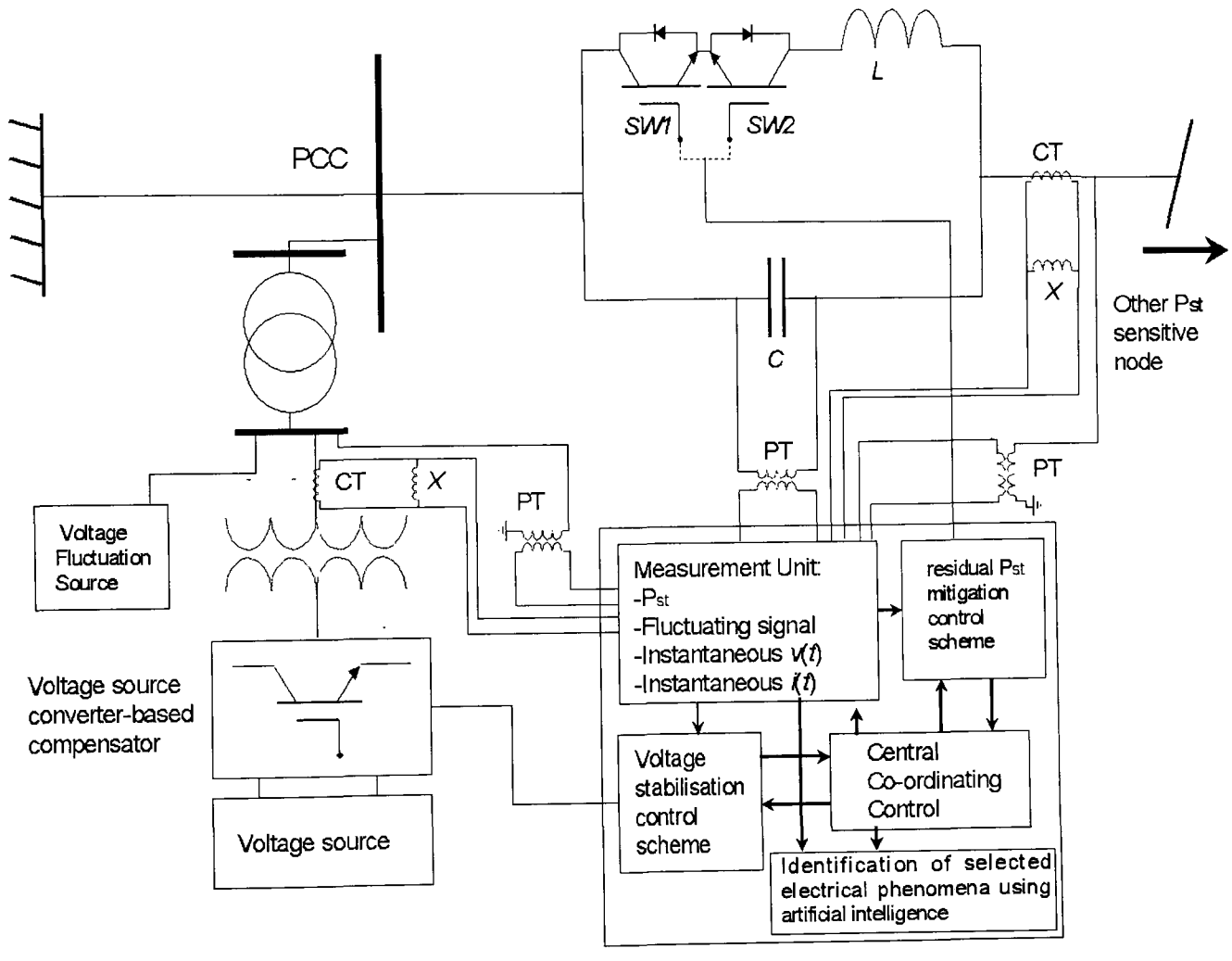


Figure 7.19. Shunt-series flexible controller

The double controller scheme is intended for weak electrical network with stiff voltage fluctuations source and very high P_{st} (more than 10). The shunt connected controller is placed close to the voltage fluctuation source, and it is mainly dedicated to compensate active and reactive power series-connected. The series-connected controller is committed to both mitigation of travelling residual voltage fluctuations from far and close sources, and to increment the network's short-circuit capacity.

The central co-ordination control unit is dedicated to administrate the control requirements of both controllers, and the measurement unit. The artificial intelligence unit is intended to identify magnitude and frequency of the voltage fluctuations and send that information to the central control unit.

The measurement unit quantify voltage and current, and continuously evaluate P_{st}. The results are send to the central control unit in order to facilitate their use by the voltage stabilisation and residual P_{st} mitigation schemes.

- Development of a real-time adaptable control strategies tool-box for multiple or single series controllers, such as DVR and TCSC. The control strategies would utilise a combination of vector control techniques; advanced time-domain multivariable strategies; and PWM and square wave multi-pulse modulation schemes. A special square modulation strategy for series controllers to mitigate voltage fluctuation at low frequency, below 4 Hz, is shown in Figures 7.20. It is assumed that the modulation is for a FCSC equipment.

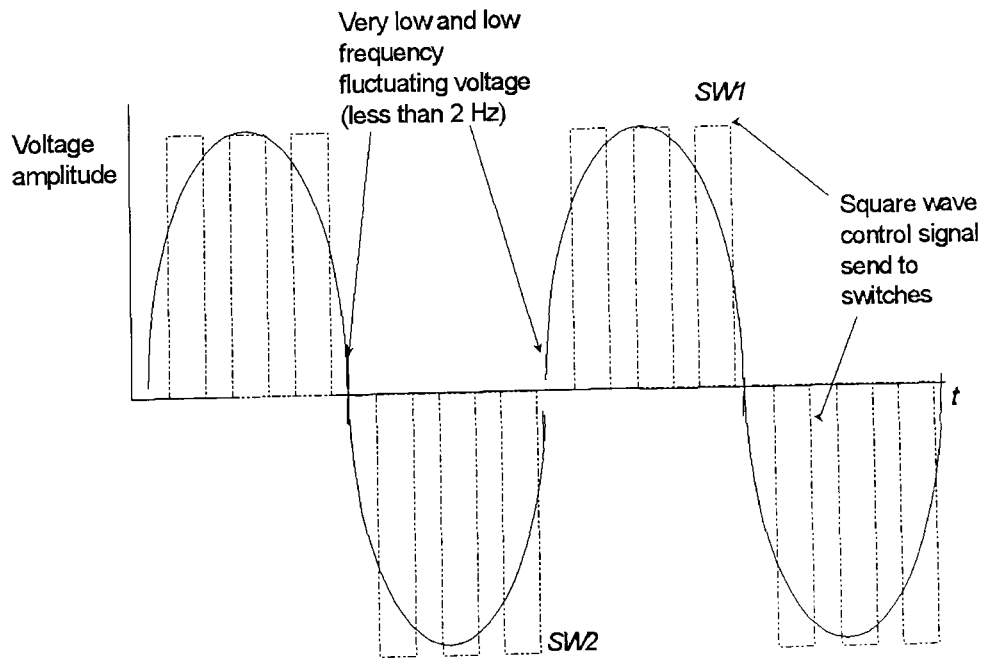


Figure 7.20. Square modulation for mitigation of low frequency voltage fluctuations

- Development of a time domain voltage fluctuations penetration analysis and evaluation tool, for transmission and distribution systems. The tool is intended to evaluate the voltage fluctuation propagations and locate P_{st} sensitive nodes, potential P_{st} sensitive loads; and flicker sensitive customers. In addition, the evaluation tool should be able to find the location and characteristics of series mitigation equipments to optimally mitigate voltage fluctuations. The analysis tool should include many types of voltage sources, such as embedded generation units for instance.

- Development of a TCSC adaptive control strategy to enable the controller to select its compensation scheme depending on actual IFS and P_{st} levels in a particular P_{st} sensitive node, and the frequency and amplitude of the fluctuations.

7.9 INTRODUCTION OF A GUIDELINE FOR LOCALISATION OF P_{ST} SENSITIVE NODE AND FLICKER SENSITIVE CUSTOMER AND MITIGATION EQUIPMENT ALLOCATION

The optimal location of series mitigation equipment in actual transmission and distribution systems is still an open area of research. The impact of the incorporation of new voltage fluctuation sources on the electrical system, and the mitigation performance of new shunt and series mitigation equipment should be assessed, well in advance of the scheduled time of installation. Of course, this would be only possible if the adequate software and hardware tools are on hand. An analysis tool which covers the evaluation of P_{st} nodes; series mitigation equipment placement, and voltage fluctuations mitigations assessment in a multi-source environment are not part of the original research objectives of this work. Nevertheless, a preliminary effort is offered in this direction by the author and a guideline for the placement of mitigation equipment and the identification of P_{st} sensitive nodes is proposed below:

1 Collection of distribution systems data
2 Collection of transmission and sub-transmission system data
3 A survey of the characteristics of voltage fluctuations sources connected to transmission and sub-transmission systems, such as EAF, DC-EAF and off-shore and in-shore wind farms.

4 Time domain modelling of the power grid considering all voltage fluctuations sources.

5 Evaluation of voltage fluctuations penetration in the electrical network for each individual source, using superposition.

6 Estimation of the total voltage fluctuations magnitude and frequency in every transmission network node, summing on injected, correlated and uncorrelated, voltage fluctuations.

7 P_{st} estimation in every node connecting the transmission network with every distribution system (power substation). The evaluation should be based on the IEC-Flickermeter using data results corresponding to actual 10 minutes time of system operation.

8 Categorisation, in decreasing order, of P_{st} levels resulting from the previous evaluation. The node exceeding P_{st} unity values, or in the vicinity, or close, are classified as P_{st} sensitive node. The exceptions to this rule are nodes inter-connecting voltage fluctuation sources with the transmission or distribution system, which are classified as P_{st} generating nodes. If no P_{st} sensitive node exists, the analysis terminates at this step.

9 Placing of mitigation equipment between the distribution system's PCC (classified as P_{st} sensitive node) with the highest P_{st} and the neighbouring P_{st} generating node where the voltage fluctuations source with the highest P_{st} exist.

10 Nodal P_{st} levels re-evaluation, repeating Steps 6 to 8 and 10.

11 If the targeted P_{st} sensitive node is eliminated, the evaluation for that node terminates at this point, moving the procedure on to Step 12 to address nodes. Otherwise, additional voltage fluctuations source affecting the targeted node exist, hence, the allocation of extra mitigation equipment should be evaluated. If the source is in the transmission or sub-transmission system, Steps 6 to 10 should be repeated. If the source is in the local distribution network, move to Step 13.

12 Repeat Steps 5 to 11 for the next P_{st} sensitive node. If no P_{st} sensitive nodes left, the evaluation terminates.

13 Time domain modelling of the distribution system under study considering all the internal voltage fluctuation sources. The P_{st} calculated for the PCC in previous steps should be included as a separate voltage fluctuations source having fixed frequency and amplitude.

14 Time domain simulation. Calculation of the voltage fluctuations frequency and magnitude in every distribution network node.

15 New P_{st} estimation in every node, as that carried out in Step 7. The calculation of P_{st} should consider actual 10 minutes time, and also 10 minutes of the simulation results previously obtained in Step 7.

16 Categorisation of P_{st} similar to that in Step 8. Lighting circuits connected to a P_{st} sensitive node are considered as P_{st} sensitive loads with a potential flicker sensitive customer in the neighbourhood.

17 Placement rules for custom series mitigation equipment are given below:

- If there are a number of P_{st} sensitive nodes (provoked by high P_{st} at PCC), and they are dispersed in a radial distribution network, the mitigation equipment can be connected between the low voltage side of the substation and the distribution feeder with the largest number of sources. If the distribution system is supplied by more than one substation via a sub-transmission ring, the options for connecting the mitigation equipment can be: a) between the transmission system and the substation with the highest P_{st}; b) between two neighbouring substations with the highest P_{st}.

- If a P_{st} sensitive node in the distribution system has higher P_{st} than the one injected from the substation (or substations) at PCC, the installation options are: a) between the feeder connecting the P_{st} sensitive load and the voltage fluctuation source; b) if many sources exist, the mitigation equipment can be installed in series with the feeder having the lowest short-circuit level, considering a flow trajectory to the P_{st} sensitive load.

18 Re-evaluation of nodal P_{st} values in the distribution systems repeating Steps 13 to 15.

19 If the P_{st} injected into the P_{st} sensitive load and flicker sensitive customer is not low enough, the incorporation of extra mitigation equipment is considered.

20 The analysis is terminated when the target P_{st} goal is achieved.

A fault level analysis and evaluation of the short-circuit capacity of the distribution system, particularly on those nodes surrounding voltage fluctuation sources, would be helpful to identifying, in advance, all the weak lines and the location of potential P_{st} sensitive nodes. The overall procedure of may be termed P_{st} sensitivity analysis.

Such specialised digital tools do not exist at present but initial studies may be assisted by the use of general time-domain application such as PSCAD© or ATP-EMTP.

7.10 CONCLUSIONS

This chapter has shown the TCSC to be an effective mean of voltage fluctuations mitigation. The controller has been extensively tested in a real-time HIL environment. The testing stage needed various hardware and software tools, which have also been successfully developed. Effective and encouraging research has been completed, producing valuable experiences and new research ideas. The main conclusion reached in this Chapter are summarised below:

The TCSC and RT-DIMR control effectiveness on lowering P_{st} levels has been fully demonstrated throughout a series of comprehensive and successful experiments carried out using a real-time HIL voltage fluctuations testing environment. The TCSC has been tested with a wide range of fluctuating frequencies, covering the spectrum range of voltage fluctuation sources such as EAF, DC-EAF, wind generators and induction motors. These experiments have launched the TCSC as a potential voltage fluctuations mitigation equipment in distribution system with embedded generation units.

A new real-time HIL control strategy, termed RT-DIMR, has been designed and implemented using both commercially available software and hardware computing tools; and tailor-made FORTRAN routines. The flexibility of the strategy to instantaneously track fluctuations for a wide range of frequencies, is among its strengths. The RT-DIMR is potentially applicable to other series or shunt controllers.

The success in lowering P_{st} opens many application and research opportunities for the TCSC technology. With this in mind, a number of future research ideas, proposed by the author, are fully detailed. The main research objectives in these projects are the

application and capabilities expansion of series mitigation equipment and the development of new control strategies.

The concepts of P_{st} sensitive node, P_{st} sensitive load; flicker sensitive customer; and residual voltage fluctuation are all defined in this chapter in order to facilitate the understanding of voltage fluctuation phenomena. Based on this philosophy, guidelines for their identification within an electrical system are also proposed, establishing an initial procedure to place series voltage fluctuation mitigation equipment in transmission, sub-transmission and distribution systems. The need to install new mitigating equipment in real-world electric systems should eventually lead to the implementation of new specialised tailor-made software and hardware tools for such a purpose.

7.11 REFERENCES

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CHAPTER

8

CONCLUSION AND SUGGESTIONS FOR FUTURE RESEARCH PROJECTS

8.1 GENERAL CONCLUSIONS

Power electronic-based controllers such as FACTS and Custom Power have come to revolutionise conventional power networks. Namely, the groundbreaking feature is their capability to ameliorate the steady and transient state, and dynamic behaviour of transmission and distribution systems. The TCSC capacity to improve electrical networks adversely affected by voltage fluctuations, has been experimentally demonstrated. The general conclusions for this research are the following:

- The TCSC effectively mitigates voltage fluctuations in the full range of frequencies (0 – 25Hz). The newly developed control strategy, RT-DIMR, demonstrates its capability and flexibility to modulate rapidly the TCSC capacitive region responding very well with both sinusoidal and non-sinusoidal fluctuations.
- The TCSC performance suggests that the controller is capable of mitigating residual voltage fluctuations emitted by multiple sources. Furthermore, this also suggests that under certain circumstances various shunt-connected mitigating equipments (local mitigation) could be substituted with a single TCSC (wide area mitigation).

- The various aspects of designing and constructing a scaled-down prototype and real-time environment are a laborious and time-consuming task. This knowledge allows a better perspective of planning and design of prototypes in the future.
- A well-designed TCSC involves a single resonance mode in the operation of the controller at fundamental frequency. The synchronisation of resonance modes facilitates the calculation and selection of the LC elements of the TCSC.
- The simultaneous use of real-time computing platform, simulation software, and ancillary electronics equipment provide an ideal real-time environment for hardware-in-the-loop experimentation with scaled-down prototypes and their control strategy.
- The use of the virtual IEC-Flickermeter based on the IEC-61000-4-15 avoids subjective interpretations of the flicker severity. The P_{st} is a useful index to assess the TCSC effectiveness as voltage fluctuation mitigation equipment.

The research and technical experience gained at each step of the project (hardware, software development and real time testing) has been plentiful and gratifying. Every difficulty overcome was fruitful, enabling the required solution to be found. Further ideas resulted from such challenging endeavours. The many and different experiments realised and hundreds of hours spent in laboratory have provided the author with a high degree of expertise useful for the next generation of research work and a vivid testimony of the meaning of physical human endurance. Accomplishing the final objectives of the research work and its respective documentation also marks the end of this PhD thesis but not the end of the road.

8.2 FUTURE RESEARCH PROJECTS

This section presents an assortment of future research projects and ideas.

Real-Time Time-Domain Voltage Fluctuation Propagation Simulator

There are few voltage fluctuations propagation analysis tools proposed in the open literature. They are based mostly on a harmonics propagation-like analysis, where each component of the very well-known frequency spectrum of the voltage fluctuations is evaluated separately. This technique is inflexible as the voltage fluctuations have only

constant frequency and amplitude and are injected by one type of source which only provides poor information on flicker severity. Furthermore, this analysis is limited to a few system nodes, it does not take into account mitigation equipment, and consideration of distribution systems and real-time simulation is not an option. This project proposes to develop a set of tools, to be run on a high-performance DSP platform, having the following capabilities:

- Development of models using time-domain techniques
- Estimate individual voltage fluctuation injections and their penetration in the network.
- Inclusion of several types of voltage fluctuations sources operating all at the same time
- Capability to evaluate varying voltage fluctuations
- Assessment of transmission and distribution systems with embedded generation
- Evaluate the performance of mitigation techniques and equipments
- Continuous calculation of flicker severity indices
- Capability to operate in real-time

Optimal Allocation of Series-Connected Power Customer Controllers for Voltage Fluctuations Mitigation in Distribution Systems.

The voltage fluctuations can propagate throughout the distribution system. The main objective of this project is the development of a procedure to optimally allocate series-connected Custom Power controllers into a distribution system, with embedded generation units. Artificial intelligence and the PSCAD™ will provide the tools too achieve the goal. A second objective of the research focuses on comparing the series against shunt mitigation equipment in a scenario where multiple sources of voltage fluctuation are installed. The challenge is to demonstrate the advantages of the former over the latter.

Optimal Design of a Compensating Scheme with Multiple Series-Connected TCSC Modules for Control of Power Oscillations and SSR phenomena

The TCSC capabilities to damp power oscillations and SSR have been widely reported in the open literature. However, a TCSC scheme is normally designed to control the power flow, and so select the inductive and capacitive elements and the thyristors. The

project proposes to research on the modulation efficiency of various series-connected TCSC modules and to propose a design procedure for power oscillations damping and SSR mitigation. One aim is to reduce the time response of the controller and to increase the modulation frequency when the capacitive – inductive regions are used. In addition, the modulation of multiple TCSC modules using its inductive region can be tested but avoiding the inherent hidden resonance mode of each module. The associated multi-module control strategy should also be developed in this project. The strategy should select between reactive mitigation technique to apply (capacitive-capacitive, capacitive-inductive and inductive-inductive) depending on the frequency and amplitude of the power oscillations or the presence of power swing. In order to evaluate the proposal, a scaled-down prototype should be constructed and experimentally tested. The damping performance of the optimised multiple TCSC modules scheme are compared with the characteristics of full-scale TCSC already in operation.

Wide Area Distributed Power Quality Monitoring Station for Distribution System with Embedded Generation System.

The bulk incorporation of multiple power-electronics based converter in distribution networks, electric arc furnaces and other non-linear loads, together with those distortion events caused by faults and line disruptions, have adversely affected the quality of power of the grid. In addition, the increasing inclusion of embedded generation units, particularly wind generators, has brought about benefits but also further concerns about power quality deterioration.

Although remedies such as application of custom power controllers and active filters are satisfactory solutions for specific-customers, the quality problems still persist, from the point of view of the network, affecting other customers and perturbing also the correct operation of sensitive loads. The planned characteristics for the monitoring station are given below:

- Wide area multi-point distributed measurements to analyse power quality events propagation phenomena
- Measurement of events such as voltage fluctuations, voltage sags and swells, voltage interruption, notches, and harmonics
- Capability to statistically process the data results

- Compatibility with up to date IEC and IEEE standards. Special attention should be put on the implementation of the IEC-Flickermeter as it should not be adversely affected by power quality events
- Wide bandwidth to evaluate fast events

Experimental Investigation of Power Electronics-Based Controllers and it Application in Embedded Generation Systems.

This is an extensive long-term research programme directed at developing and testing advanced Custom Power controllers, particularly for distribution system with embedded generation units. The main objectives of the program are:

- Development and testing of novel power electronics-based controller exploring or creating new configurations with enhanced capabilities to operate in distribution generation environments
- Investigation on novel modulation techniques and control strategies
- Development of easy-to-use controller design techniques and testing procedures
- Proposing recommendation for Custom Power applications, in particular for the improvement of the power quality

A specialised laboratory, named Advanced Power Controllers Research Centre, can be created pursuing the different individual projects to achieve the former objectives

Wide Area Multi-Objective Distributed Control Strategy for Distribution System with Embedded Generation Units and Custom Power Controllers

In the near future the operational complexity of large modern distribution systems (integrating multiple embedded generation units, Custom Power controllers and other controllable power electronic drives) should be comparable with some transmission systems, which require more research attention. Many are the challenges to overcome such as the coordinated operation of a distributed control system of Custom Power controllers, the incorporation of new generation units, effects of weather change, the behaviour of the relaying system, among other. This specialised research tool is proposed as a long-term research project. The hybrid characteristic planned for the project should provide the flexibility to incorporate digital and analogue models in the same real-time environment. The stages proposed to achieve the objectives are given below:

Stage 1: Implementation of a distribution system with Custom Power controllers and embedded generation units models (mainly wind and combined heat and power generation) using PSCAD©

Implementation of a differential wind variation model

Development of the set of Custom Power control strategies

Development of the master control strategy

Simulation of the wide area control in non real-time basis

Stage 2: Implementation of the wide area control in a high-performance DSP environment

Non-interactive simulation of the wide area control in real-time

Stage 3: Development and testing of three scaled-down wind turbines modules

Implementation of three scaled-down combined heat and power generators

Implementation and testing of a wide area measurement unit

Development of a dynamic interactive platform which can be used to provoke various fault types, load variations, connection/disconnection of an embedded generation units, wind flow variations among other. Single or multiple events should be possible to be applied at any moment.

Stage 4: Implementation and testing of a master communication system and distributed slave network based on Ethernet protocol

Implementation of a scaled-down distribution network

Development of a Distribution Relay Unit (DRU) to simulate fuses, sectionalisers, and interrupters

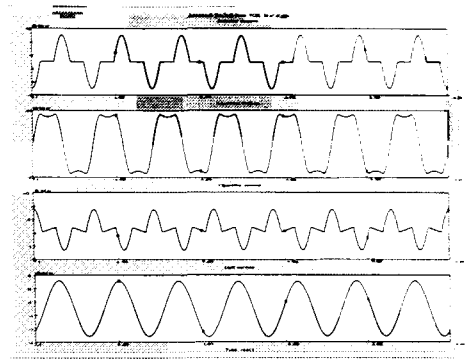
Stage 5: Incorporation of scaled-down Custom Power controllers

Integration of the full experimental environment

Long-tem, real-time experimentation

APPENDIX

A



TCSC SIMULATIONS

A.1 INTRODUCCION

Digital simulation is a powerful tool helping to better understand the TCSC capabilities. At the simulation stage the controller can be subjected to different operating conditions; in order to observe and analyse its behaviour; and to determine whether or not the TCSC performance is acceptable. Once confidence has been gained with the operation of the controller, the design stage is completed and the TCSC is ready to go into the construction stage. In this appendix simulations of the TCSC prototype are presented for cases of modulation and triggering at $\alpha = 90°$. In order to compare the TCSC prototype performance with that of a full-scale, well-designed TCSC, the modulation of the Kayenta scheme is simulated under similar circumstances. The simulations confirm the TCSC prototype as a well-designed equipment.

A.2 TCSC PROTOTYPE SIMULATIONS

The normal operation and modulation of the TCSC prototype is assessed using the PSCAD© software. The 230 kV power lines used in these simulations are based on the Glen Canyon –Shiprock transmission line [1,2,3]. It is a radial system, which includes two 160km transmission lines sections. The system is 50% series compensated with 41.2 % being fix, non-controllable capacitive compensation, and 8.2% contributed by the base TCSC controlled capacitor. Figure A.1 shows the electrical system and the TCSC prototype implemented in PSCAD©.

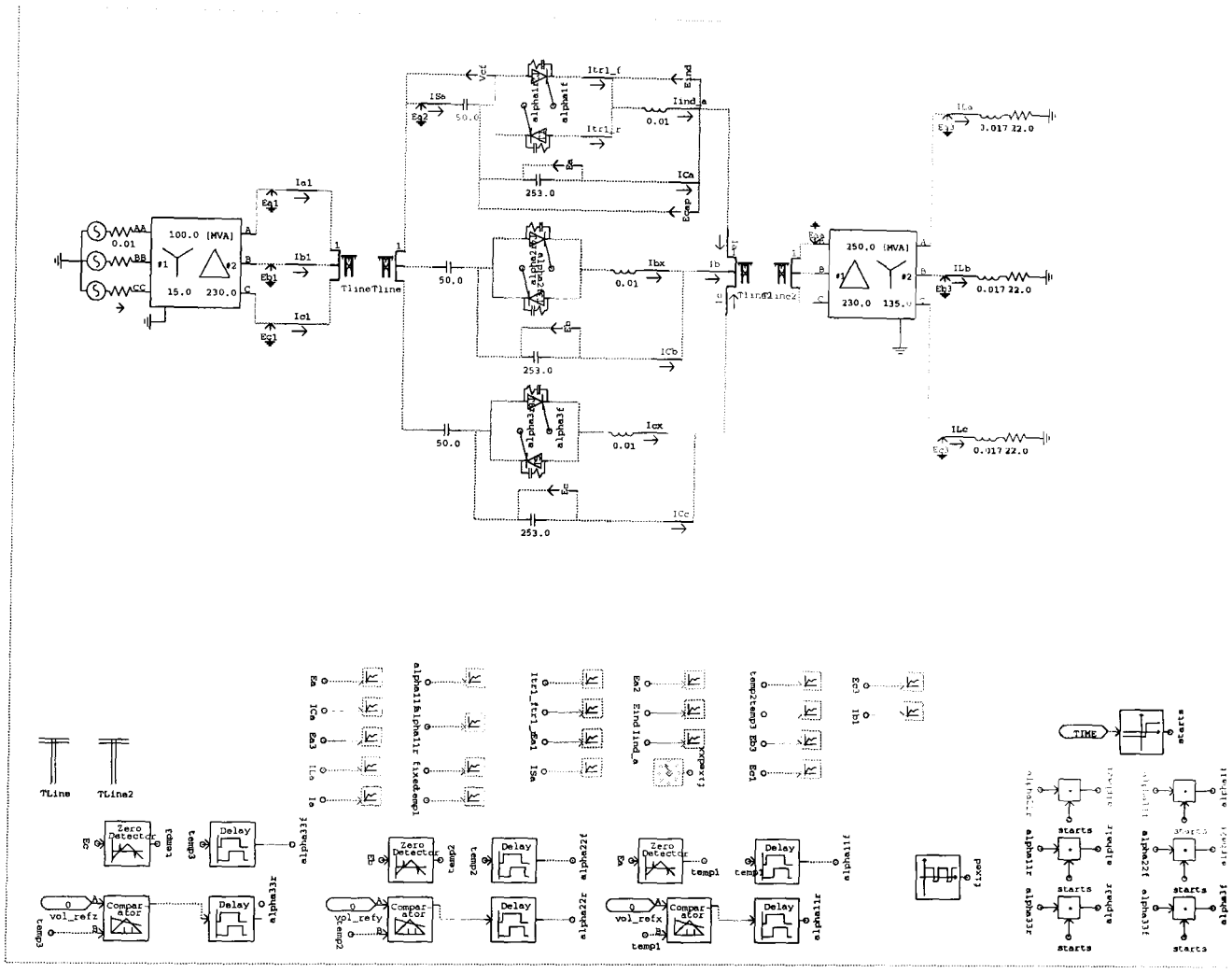


Figure A.1. PSCAD© schematic diagram of the TCSC prototype and electrical system

Figure A.2 shows the fundamental capacitor voltage and current waveforms together with the inductor current waveforms. The TCSC operates in the capacitive region with the triggering angle set at α=143°. The voltage and current capacitor profiles of the TCSC operating in the inductive region at α=130°are presented in Figure A.3. The basic TCSC operation details and the description of the fundamental waveforms has been presented in Chapter 3

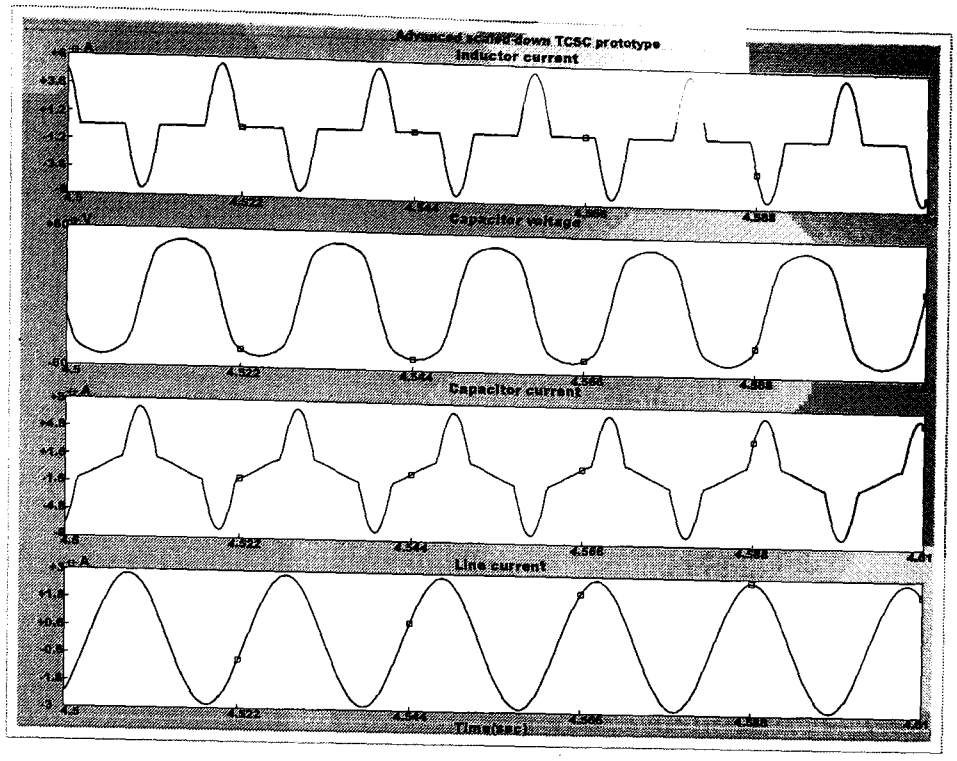


Figure A.2. Voltage and current waveforms characterising the TCSC in the capacitive region under steady-state operation at α=143°

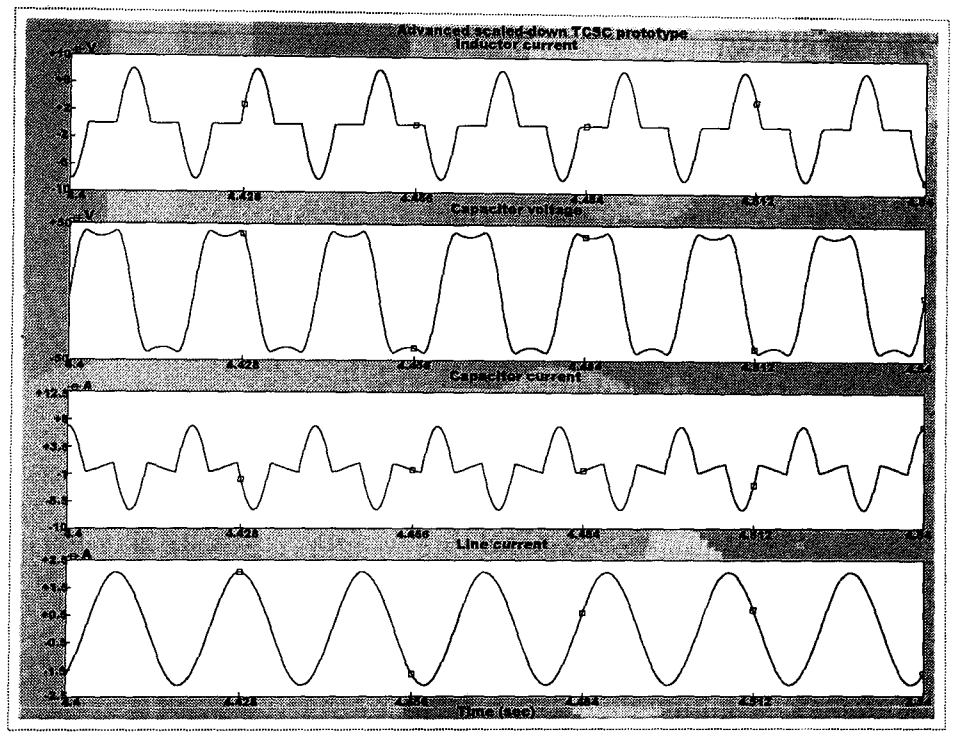
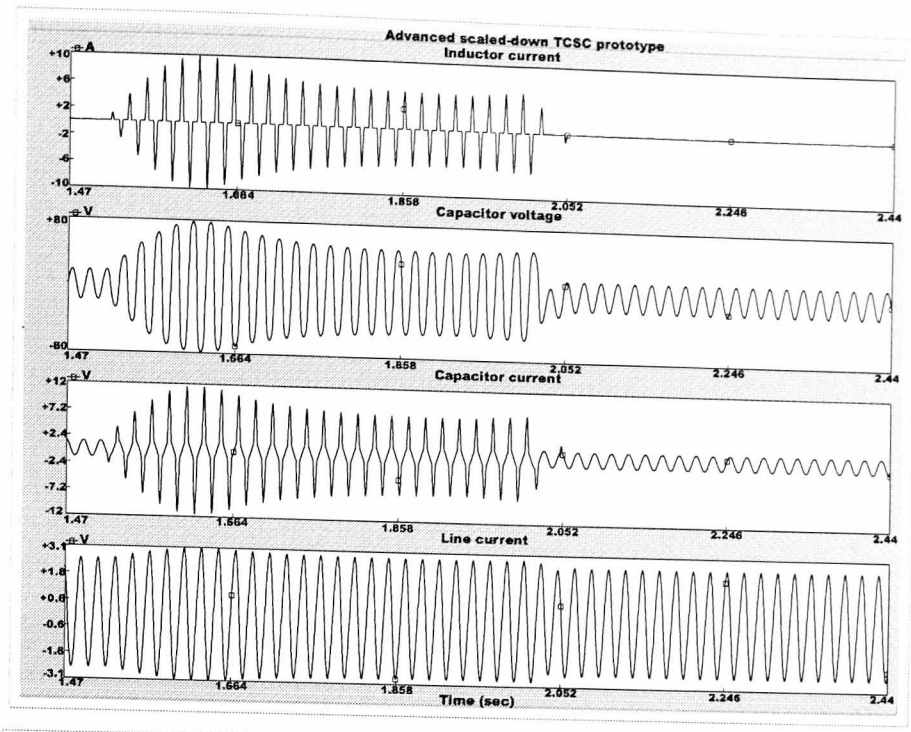
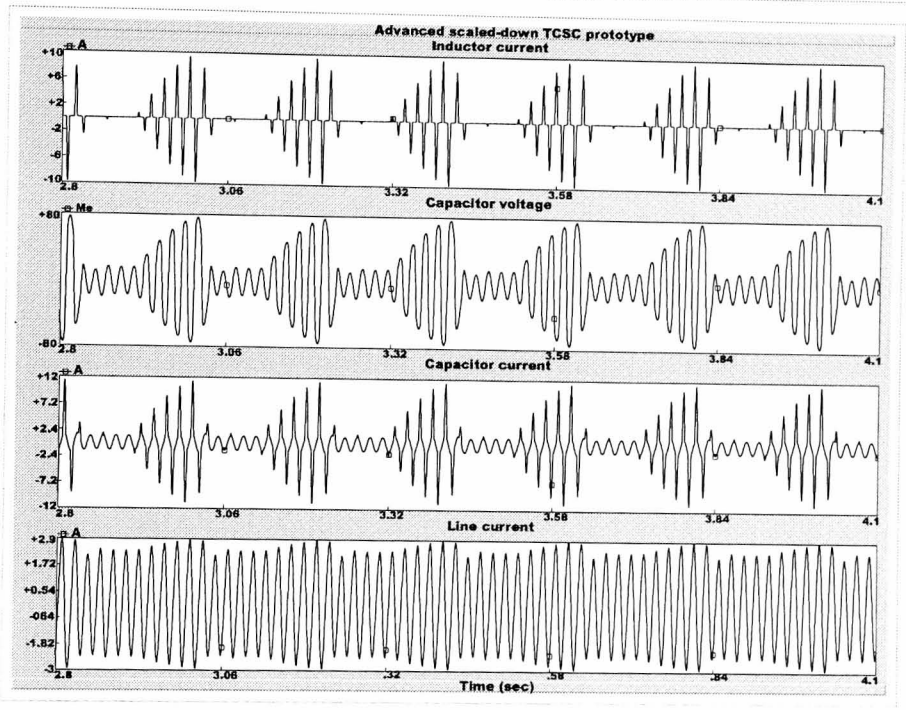


Figure A.3. Voltage and current waveforms characterising the TCSC in the inductive region under steady-state operation at α=130°

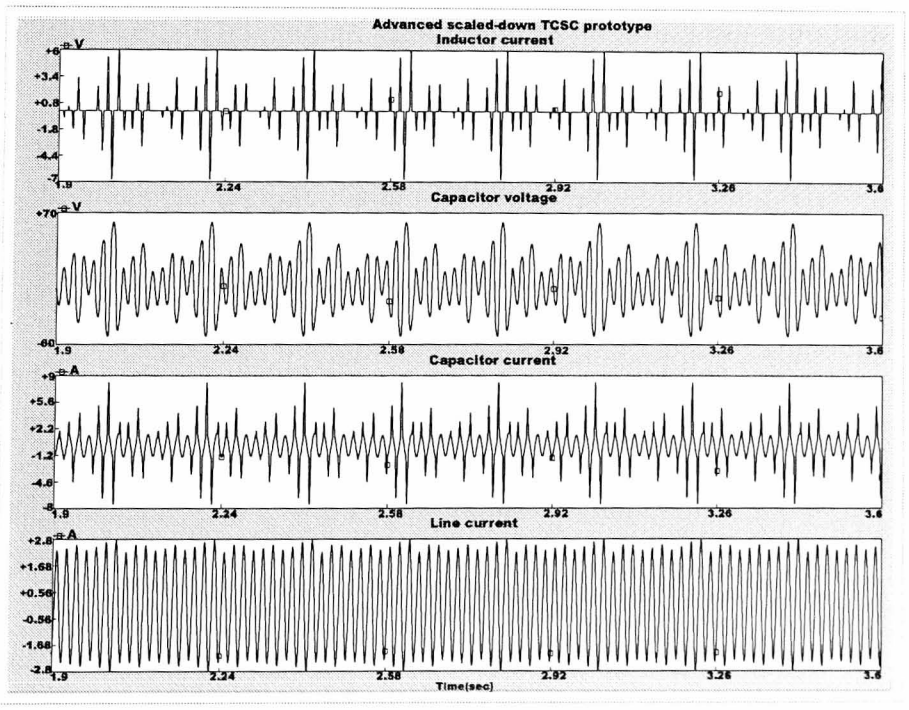
The transmission line current modulation is a technique widely used to control transitory oscillatory phenomena in actual electrical systems with FACTS equipment [4,5,6-9]. A typical example is the mitigation of subsynchronous resonance at low modulating frequencies [6-8]. Figure A.4 illustrates the TCSC operation in the capacitive region at different step modulating frequencies. Figure A.5 presents cases for TCSC operation in the capacitive-inductive region, with step modulation at different frequencies.



a)

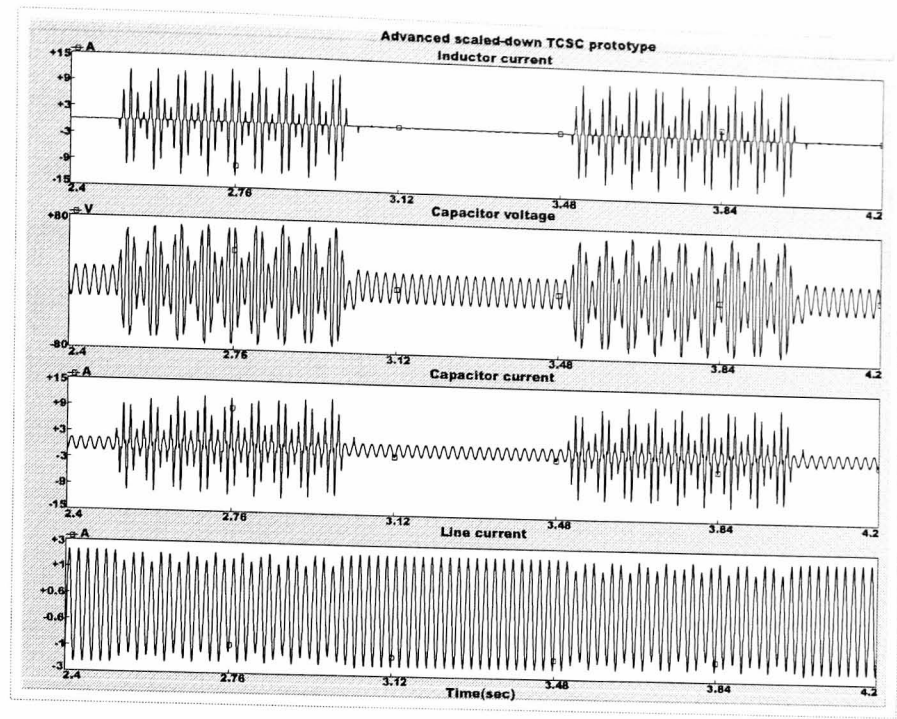


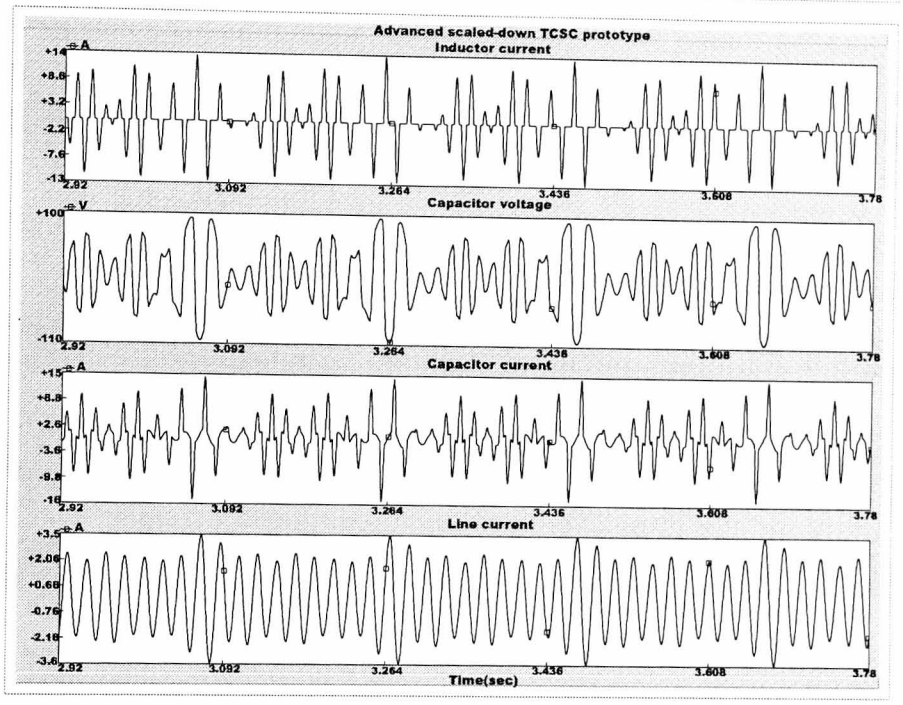
b)



c)

Figure A.4. TCSC voltage and current waveforms for operation in the capacitive region with step changes between α=180° and α=140° in open loop conditions at different modulating frequencies: a) 1 Hz; b) 5 Hz; c) 15 Hz





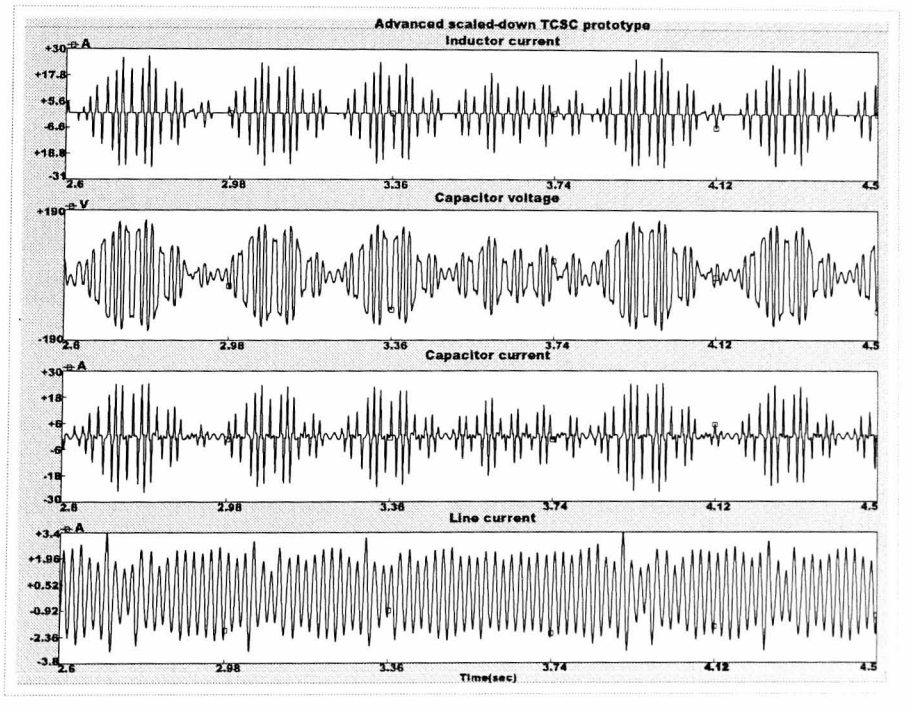


Figure A.5. TCSC voltage and current waveforms for the operation in the inductive-capacitive region with step changes between α=180° and α=90° in open loop conditions at different modulating frequencies: a) 1 Hz; b) 5Hz; c) 15 Hz

A comparative analysis of the two previous cases presented in Figures A.4 and A.5 clearly evidences the smoother current line modulation resulting from step changes using only the capacitive region. Operation in the capacitive-inductive inter-regions presents unwanted oscillations which eventually can lead the TCSC into instable operation. The grounds for this condition to happen can be explained when considering that the TCSC partially operates in the vicinity of intrinsic hidden resonance modes, in which the inception of resonances and instabilities are a continuous threat. Single or repetitive step changes modulating the apparent TCSC inductive reactance also produces undesirable oscillations and line current variations, particularly if triggering at α=90° is involved, as show in Figures A.6 and A.7.

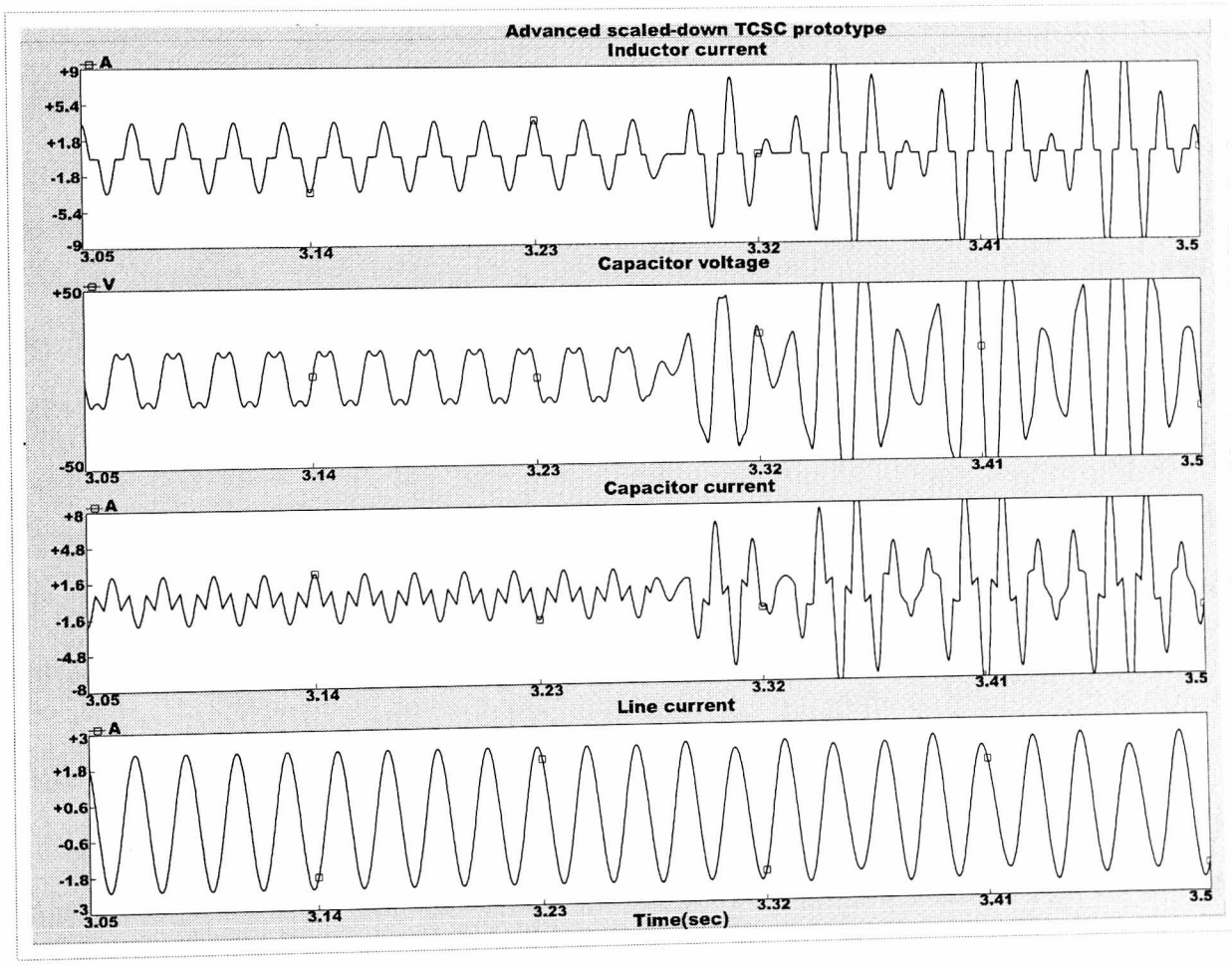


Figure A.6. TCSC voltage and current waveforms for operation in the inductive region with a single step angle change between α=120° and α=90°

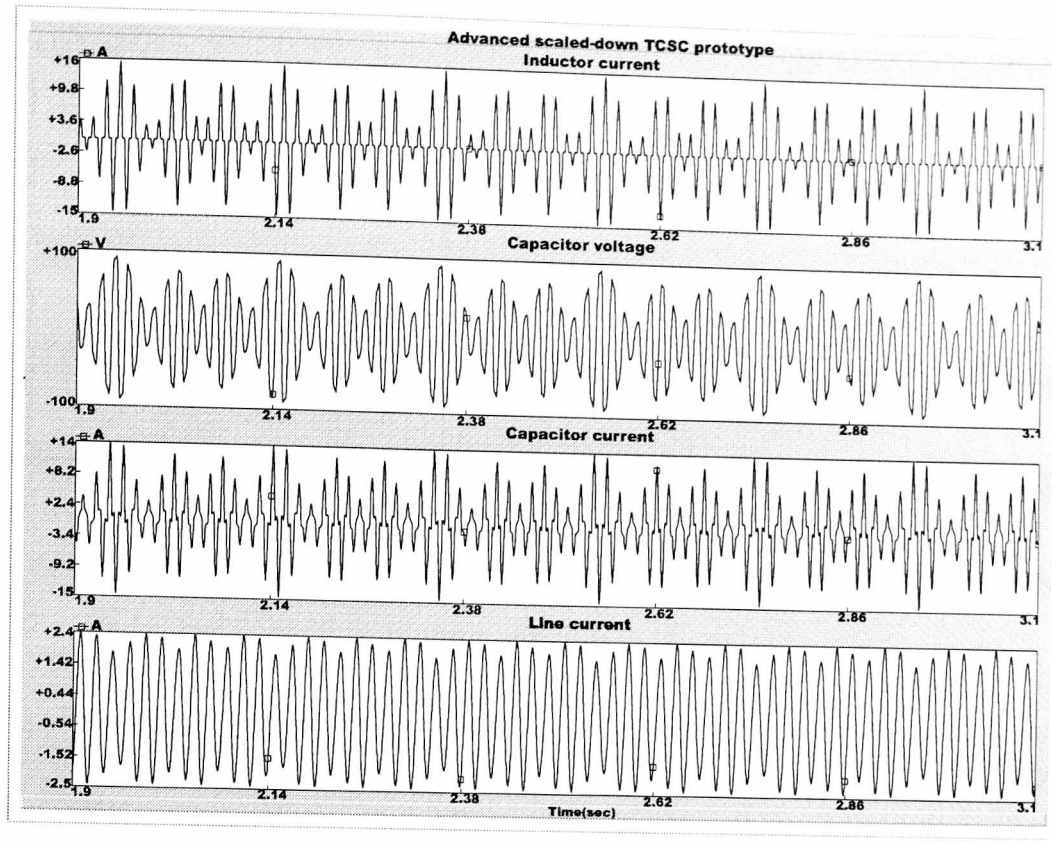


Figure A.7. TCSC voltage and current waveforms for operation in the inductive region with step changes between α=90° and α=100° at a modulating frequency of 5Hz

The TCSC tendency to resonate is notorious particularly when abrupt step triggering angles occur, as it is clearly illustrated by the previous simulations. The waveforms in Figures A.6 and A.7 show that the TCSC internal oscillations, rather than the step α changes, predominate over the modulation of the line current flow. The results bring into question the utilisation of the bang-bang modulation, involving triggering TCSC at α=90°, as a contingency control measure when repetitive, fast, undesirable oscillatory phenomena occurs in electrical networks.

The use of the TCSC inductive region in such conditions, seems to be possible but with triggering angles between α=95° and the fundamental resonant mode, especially for oscillations lower than 1 Hz. However, this requires further investigation. In Chapter 6, several experiments are carried out with the TCSC prototype which confirms the poor expectatives of the bang-bang, using α=90° - α=180° strategy.

A.3 KAYENTA SCHEME SIMULATIONS

In order to compare the TCSC prototype characteristics and behaviour with those of full-scale controllers, the TCSC module and transmission line of the Kayenta installation are simulated [1,2,3]. Figure A.8 presents the waveform profiles resulting from the modulation of the TCSC.

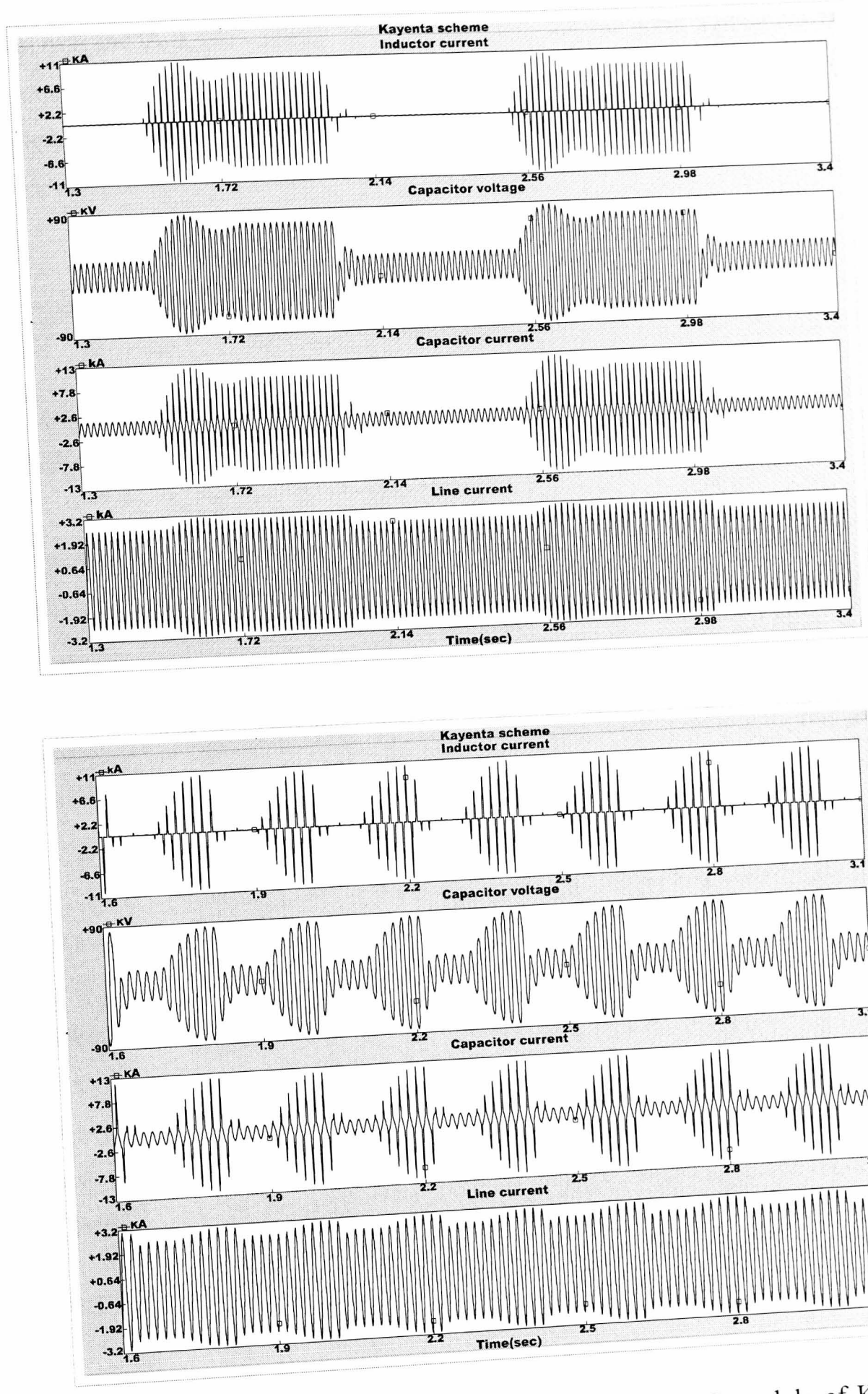


Figure A.8. Voltage and current waveforms of the TCSC module of Kayenta installation simulated using step changes between α=180° and α=147°: a) 1 Hz modulating frequency; b) 5 Hz modulating frequency

Figures A.4 and A.8 show many similarities. These reveal good agreement between behaviours of the TCSC prototype and the Kayenta scheme. Both controllers have been simulated considering very similar operating conditions. The results confirm that the newly developed three-phase scaled-down TCSC as a very well-designed prototype.

A.4 CONCLUSIONS

A representative number of advanced scaled-down TCSC prototype simulation under different conditions have been presented in this Appendix.

The repetitive TCSC operation in α=90° to α=180° is a risky strategy due to the inestabilities provoked by the intrinsic resonance mode. The use of the TCSC inductive region is not recommended for triggering angles at α=90° and close to it. If TCSC inductive region is to be used, then a safety angle margin is required in order to minimise potential unstable TCSC operation and avoid the its tendecy to resonate. If a single inductive to capacitive region transition occurs, using a safety angle margin, the TCSC may stabilise in a short period of time

Digital simulations corroborate the smoother, non-oscillatory characteristic performance of the TCSC step modulated in the capacitive region, while strongly recommends the controller as well-suited equipment for controlling voltage fluctuation mitigations and transitory oscillations. Further computer simulations results, together with a comparative analysis involving the TCSC module of the Kayenta scheme confirms the newly developed advanced three-phase scaled-down TCSC as a well-designed FACTS controller.

A.5 REFERENCES

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APPENDIX

B

RT-DIMR FORTRAN ROUTINES

The RT-DIMR control strategy presented in Chapter 5 has included the following three main routines: a) reference; b) input signal processing; and c) TCSC control signals processing. The FORTRAN source code for such routines is detailed below.

```
C*****************************************************************
C*****************************************************************
C     REAL TIME DYNAMIC INSTANTANEOUS MODULATION RESPONSE
C                          RT-DIMR
C                       CONTROL STRATEGY
C*****************************************************************
C
C*****************************************************************
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C************************VARIABLES*********************************
C++++++++++++TCSC CONTROL SIGNALS ROUTINE
      DECLARATIONS, INTEGER ikk, ipx, iz, km, j
      DECLARATIONS, REAL*8 xdp1(2),xdp2(2),xdp3(2),zeit1,zeit2,zeit3,prox1a,
     +prox2a,prox3a,tempo2,tempo1,t_topx,errn,damp1,damp2,damp3,xdamp1,
     + xdamp2,xdamp3,prox1,prox2,prox3,amax,bmax,cmax,sal_a,sal_b,sal_c,
     +xcambio,xmax1(2),xmax2(2),xmax3(2),top_mar,bot_mar,sq_peak(5),dx(5),
     +cxs(5,3),ave(999,16),smooth(3),crms1(5),wo,n,n1,smooth1,xlimit,ninput,
     +ave_mul,rms1a,rms2a,rms3a,rms4a,rms5a,smth(3),sli(999,16), nim, nim1,xlm1,
     +smth1, slimul, mean(3),avx(999,16),nz,nz1,avemul,xlmt,mean1
C++++++++++INPUT SIGNAL PROCESSING ROUTINE
      DECLARATIONS, integer iiy1, iiy3, iiy2
      DECLARATIONS, real*8 avg1(999,16),mnx1(3),na1,na11,almt,amul1,mnx11,
     +exis21,xtim1,xtim2,exism1,alag,alead,ag_ll,aleadz,avg2(999,16),mnx2(3), na2,
     +na12,amul2,almt2,mnx12,exis22,ytim1,ytim2,exism2,avg3(999,16), mnx3(3),
```

```
     +na13,na23,almt3,amul3,mnx13,exis23, ztim1,ztim2,exism3
C*****************************CONSTANTS*************************
C++++++++++++TCSC CONTROL SIGNALS ROUTINE
      wo=2*3.141596*50
      km=1
      ipx=1.0d0
       iz=1
      n=16.0d0
      nim=16.0d0
       nz=16.0d0
      n1=2.0d0
      nim1=2.0d0
       nz1=2.0d0
      xlimit=999.0d0
      xlm1=999.0d0
       xlmt=999.0d0
      ninput=5.0
C++++++++++INPUT SIGNAL PROCESSING ROUTINE
      iiy1=1.0d0
      iiy2=1.0d0
      iiy3=1.0d0
C       columns in arrays
      na1=16.0d0
      na11=2.0d0
      na2=16.0d0
      na12=2.0d0
      na13=16.0d0
      na23=2.0d0
C       vector size
      almt=999.0d0
      almt2=999.0d0
      almt3=999.0d0
C*****************************************************************
C**********************REFERENCE ROUTINE**************************
C*****************************************************************
C                THIS ROUTINE FACILITATE THE INTERFACE
C          BETWEEN EXTERNAL SIGNALS AND INTERNAL PARAMETERS
C                              DURING RUN TIME
C          PROVIDING ALSO THE PARAMETER TO PRODUCE AN
C                       INTERNAL CALIBRATING REFERENCE
C          INPUTS: FMODU (FREQUENCY OF FLICKER)
C          GANA (PERCENTAGE OF MODULATION - MODULATION INDEX)
C          GCARRI (GAIN OF THE POWER SIGNAL)
C*****************************************************************
C*****************************************************************
     fmodu=(agmodu*6.283185307)
     xganf=agnaf
     gcarri=carri
     fmodu_b=(agmodub*6.283185307)
     xganf_b=agnaf_b
     fmodu_c=(agmoduc*6.283185307)
     xganf_c=agnaf_c
```

```
C*****************************************************************
C                 USER SELECTION BETWEEN INTERNAL REFERENCE
C                          OR EXTERNAL SIGNALS
C
C*****************************************************************
      if (cambio.le.0) then
        ext_a=xpha
        ext_b=xphb
        ext_c=xphc
      else
        ext_a=ypha
        ext_b=yphb
        ext_c=yphc
      endif
C*****************************************************************
C         TIME OF THE  OUTPUT SWITCH FOR PHASE A,B AND C
C*****************************************************************
      xtempoa=xadjx
C++++++++++++++++++++END OF REFERENCE ++++++++++++++++++++++++
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C
C*****************************************************************
C*****************INPUT SIGNAL PROCESSING************************
C              THIS ROUTINE AVERAGES THE INPUT SIGNAL AND
C           AND REDUCE THE EFFECTS OF THE TCSC PROTOTYPE
C                 TRANSITORY ENERGISATION PERIOD.
C           THE PARAMETERS OF THE EASY5 BUILT-IN FILTER BLOCKS
C                ARE INCLUDED AT THE END OF THE ROUTINE
C*****************************************************************
C++++GENERAL TIME COUNTERS UPDATING++
      xtim1=xtim1+1.0d0
      ytim1=ytim1+1.0d0
      ztim1=ztim1+1.0d0
C+++++++++++++++++++++++++++++++++++++++
C+++++SAMPLING EXTERNAL INPUT++++++++
      avg1(m11,m21)=entx1
      avg2(m12,m22)=entx2
      avg3(m13,m23)=entx3
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C++++++AVERAGE INPUTTED EXTERNAL SIGNAL ++++++++++++
C+++*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*
C++++++++++++++++++++++PHASE A++++++++++++++++++++++
      amul1=1/(na1*almt)
      if (m11.eq.almt) then
        if (m21.eq.na1) then
          mnx11=mnx1(na11-1)+amul1*(avg1(almt,m21)-avg1(iiy1,iiy1))
          m21=0
        else
          mnx11=mnx1(na11-1)+amul1*(avg1(almt,m21)-avg1(iiy1,m21+1))
        endif
        m11=1
        m21=m21+1
```

```
      else
        mnx11=mnx1(na11-1)+amul1*(avg1(m11,m21)-avg1(m11+1,m21))
        m11=m11+1
      endif
C++++++++++++++++++++++++++++PHASE B++++++++++++++++++++++
      amul2=1/(na2*almt2)
      if (m12.eq.almt2) then
        if (m22.eq.na2) then
          mnx12=mnx2(na12-1)+amul2*(avg2(almt2,m22)-avg2(iiy2,iiy2))
          m22=0
        else
          mnx12=mnx2(na12-1)+amul2*(avg2(almt2,m22)-avg2(iiy2,m22+1))
        endif
        m12=1
        m22=m22+1
      else
        mnx12=mnx2(na12-1)+amul2*(avg2(m12,m22)-avg2(m12+1,m22))
        m12=m12+1
      endif
C++++++++++++++++++++++++++++PHASE C++++++++++++++++++++++
      amul3=1/(na13*almt3)
      if (m13.eq.almt3) then
        if (m23.eq.na13) then
          mnx13=mnx3(na23-1)+amul3*(avg3(almt3,m23)-avg3(iiy3,iiy3))
          m23=0
        else
          mnx13=mnx3(na23-1)+amul3*(avg3(almt3,m23)-avg3(iiy3,m23+1))
        endif
        m13=1
        m23=m23+1
      else
        mnx13=mnx3(na23-1)+amul3*(avg3(m13,m23)-avg3(m13+1,m23))
        m13=m13+1
      endif
C++++++++++++++++++END OF AVERAGING PROCESS++++++++++
C
C++++++++DATA WINDOWING
      mnx1(na11-1)=mnx11
      mnx2(na12-1)=mnx12
      mnx3(na23-1)=mnx13
C
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C+++SLOW START-UP TO AVOID A TRANSITORY STATE OF THE ++++
C++TCSC PROTOTYPE AND SCALED DOWN ELECTRIAL SYSTEM++
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C+++++++++++++++PHASE A+++++++++++++++
      exism1=(entx1-mnx11)
      exismx=exism1
      xtim2=xtim1*xinc2
      if (xtim2.gt.5) then
       exis11=(exism1*mult1)
       exis21=exism1
```

```
      else
        exis11=((exism1*mult1)*xtim2*0.2)
        exis21=(exism1*xtim2*0.2)
      endif
C+++++++++++++++PHASE B+++++++++++++++
      exism2=(entx2-mnx12)
      ytim2=ytim1*yinc1
      if (ytim2.gt.5) then
        exis12=(exism2*mult2)
        exis22=exism2
      else
        exis12=((exism2*mult2)*ytim2*0.2)
        exis22=(exism2*ytim2*0.2)
      endif
C+++++++++++++++PHASE C+++++++++++++++
      exism3=(entx3-mnx13)
      ztim2=ztim1*zinc1
      if (ztim2.gt.5) then
        exis13=(exism3*mult3)
        exis23=exism3
      else
        exis13=((exism3*mult3)*ztim2*0.2)
        exis23=(exism3*ztim2*0.2)
      endif
C**********PARAMETER FOR BUILT-INPUT FILTERS BLOCK********
      alag=aaf_lag
      alead=aa_lead
      ag_ll=aag_ll
      aleadz=0.0
      zzlag=alag*1.0
      zzlead=alead*1.0
      zzg_ll=ag_ll*1.0
      zzleadz=aleadz*1.0
C
C+++++++++++++++END OF INPUT SIGNAL PROCESSING+++++++ ++++++++
C*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*+*
C
C**************************************************************
C**************************************************************
C                    TCSC CONTROL SIGNAL PROCESSING
C          THIS ROUINE PRODUCES THE TCSC MODULATION SIGNAL
C            TRACKING DOWN THE VARYING RMS FLUCTUATIONS
C**************************************************************
C**************************************************************
C
C***************THREE PHASE PHASE-INDEPENDENT ***************
C********************RMS CALCULATION*****************************
C*******USING THE SAMPLE AND FIRST DERIVATIVE METHOD*********
C**************************************************************
C
C
C
```

```
C*************************************************************************
C++++SAMPLING THREE-PHASE INPUT SIGNALS
C++++AND TWO AUXILIAR INPUTS
      cxs(km,km)=cff1
      cxs(km+1,km)=cff2
      cxs(km+2,km)=cff3
      cxs(km+3,km)=cff4
      cxs(km+4,km)=cff5

C+++++++FIRST DERIVATIVE (SFD)
      do j=1,ninput
       dx(j)=(1/(2*cat))*(3*cxs(j,km)-4*cxs(j,km+1)+cxs(j,km+2))
      end do
C+++++++SAMPLE, PEAK VALUE AND RMS CALCULATION
      do j=1,ninput
      sq_peak(j)=(kf1*cxs(j,km)*cxs(j,km))+(kf2*(dx(j)/wo)*(dx(j)/wo))
      crms1(j)=sqrt(sq_peak(j))*adj_rms
      end do
C++++SET RMS MAXIMUM LIMIT
      if(rms1.gt.285) then
        rms1=285
      endif
      if(rms2.gt.285) then
        rms2=285
      endif
      if(rms3.gt.285) then
        rms3=285
      endif
      if(rms4.gt.285) then
        rms4=285
      endif
C+++++++RMS ADJUSTMENT
      rms1a=crms1(km)*1.0
      rms2a=crms1(km+1)*1.0
      rms3a=crms1(km+2)*1.0
      rms4a=crms1(km+3)*1.0
      rms5a=crms1(km+4)*1.0
C**************SLIDING WINDOW
C++++RMS
      do j=1,ninput
      cxs(j,km+2)=cxs(j,km+1)
      cxs(j,km+1)=cxs(j,km)
      end do
C
C******************END OF RMS CALCULATION***************
C*************************************************************************
C
C
C
C
C
C
```

```
C*************************************************************
C*************************************************************
C                        AVERAGING RMS
C                   USING CIRCULAR BUFFER-QUEUES
C*************************************************************
C*************************************************************
C
C+++++++++++++++++SAMPLING RMS++++++++++++++++++++++++
     ave(m1,m2)=rms1a
     sli(my1,my2)=rms1b
     avx(m1a,m2a)=rms1c
C++++++++++++++++++++++PHASE 1++++++++++++++++++++++++
      ave_mul=1/(n*xlimit)
      if (m1.eq.xlimit) then
        if (m2.eq.n) then
          smooth1=smooth(n1-1)+ave_mul*(ave(xlimit,m2)-ave(km,km))
          m2=0
        else
          smooth1=smooth(n1-1)+ave_mul*(ave(xlimit,m2)-ave(km,m2+1))
        endif
        m1=1
        m2=m2+1
      else
        smooth1=smooth(n1-1)+ave_mul*(ave(m1,m2)-ave(m1+1,m2))
        m1=m1+1
      endif
C++++++++++++++++++++++PHASE 2++++++++++++++++++++++++
     slimul=1/(nim*xlm1)
     if (my1.eq.xlm1) then
       if (my2.eq.nim) then
         smth1=smth(nim1-1)+slimul*(sli(xlm1,my2)-sli(ipx,ipx))
         my2=0
       else
         smth1=smth(nim1-1)+slimul*(sli(xlm1,my2)-sli(ipx,my2+1))
       endif
       my1=1
       my2=my2+1
     else
       smth1=smth(nim1-1)+slimul*(sli(my1,my2)-sli(my1+1,my2))
       my1=my1+1
     endif
C++++++++++++++++++++++PHASE 3++++++++++++++++++++++++
     avemul=1/(nz*xlmt)
     if (m1a.eq.xlmt) then
       if (m2a.eq.nz) then
         mean1=mean(nz1-1)+avemul*(avx(xlmt,m2a)-avx(iz,iz))
         m2a=0
       else
         mean1=mean(nz1-1)+avemul*(avx(xlmt,m2a)-avx(iz,m2a+1))
       endif
       m1a=1
       m2a=m2a+1
```

```
      else
        mean1=mean(nz1-1)+avemul*(avx(m1a,m2a)-avx(m1a+1,m2a))
        m1a=m1a+1
      endif
C+++++++++SLIDING WINDOW
      smooth(n1-1)=smooth1
      smth(nim1-1)=smth1
      mean(nz1-1)=mean1
C*************************************************************
C**********************END OF AVERAGING************************
C
C*************************************************************
C*********************TCSC CONTROL SIGNALS*********************
C*************************************************************
C++++++ERROR MARGIN FOR CONTROL START UP
      top_mar=0.1
      bot_mar=-0.1
C++++++++++ERROR MARGIN FOR INPUT
      errp=0.001
      errn=(-1)*errp
C++++++++++TIME EVENT COUNTERS
      tempo1=tempo1+1
      zeit1=zeit1+1.0
      zeit2=zeit2+1.0
      zeit3=zeit3+1.0
      t_topx=t_topx+1.0
      ikk=1
C+++++++++NORMALISE THE INPUT SIGNALS +++++++++++++++++
C**********PHASE A
      if (bn1.gt.0) then
      damp1=((an1-bn1)/bn1)
      endif
C**********PHASE B
      if (bn2.gt.0) then
      damp2=((an2-bn2)/bn2)
      endif
C**********PHASE C
      if (bn3.gt.0) then
      damp3=((an3-bn3)/bn3)
      endif
C++++++++ADJUST NORMALISED INPUT SIGNAL
      xdamp1=(damp1-bia_a)
      xdamp2=(damp2-bia_a)
      xdamp3=(damp3-bia_a)
C+++IF TIMEX IS LESS THAN 2.2 SECONDS THEN OUTPUT IS MINIMUM
      tempo2=tempo1*xinc1
      if ((tempo2.gt.8.5).and.(zeit3.ge.ftor)) then
       zeit3=0.0
C+++++MINIMISE INSTANTANEOUS PEAKS AND NOISE
      prox1=(prox1a+((xdp1(ikk)-xdp1(ikk+1))*0.5)*100)
      prox2=(prox2a+((xdp2(ikk)-xdp2(ikk+1))*0.5)*100)
      prox3=(prox3a+((xdp3(ikk)-xdp3(ikk+1))*0.5)*100)
```

```
C*************************************************************
C*******CALCULATE MAXIMUM INSTANTANEOUS INPUT**********
C++++++++++++++++++++PHASE 1++++++++++++++++++
      if ((xmax1(ikk).gt.xmax1(ikk+1)).and.(damp1.gt.0)) then
       if (amax.gt.xmax1(ikk)) then
         amax=amax
          else
         amax=xmax1(ikk)
        endif
      elseif (amax.gt.xmax1(ikk+1)) then
          amax=amax
        else
         amax=xmax1(ikk+1)
      endif
C++++++++++++++++++++PHASE 2++++++++++++++++++
      if ((xmax2(ikk).gt.xmax2(ikk+1)).and.(damp2.gt.0)) then
           if (bmax.gt.xmax2(ikk)) then
         bmax=bmax
          else
         bmax=xmax2(ikk)
        endif
      elseif (bmax.gt.xmax2(ikk+1)) then
         bmax=bmax
        else
            bmax=xmax2(ikk+1)
      endif
C++++++++++++++++++++PHASE 3++++++++++++++++++
      if ((xmax3(ikk).gt.xmax3(ikk+1)).and.(damp3.gt.0)) then
           if (cmax.gt.xmax3(ikk)) then
         cmax=cmax
          else
         cmax=xmax3(ikk)
        endif
      elseif (cmax.gt.xmax3(ikk+1)) then
         cmax=cmax
      else
        cmax=xdp3(ikk+1)
      endif
C*********MAXIMUM INPUT LEVEL (MIL) HAS BEEN OBTAINED*****
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C
C***********DATA MIRRORING FOR SAFE PROCESSING *
C     TRIGGERING
      xdp1(ikk)=xdamp1
      xdp2(ikk)=xdamp2
      xdp3(ikk)=xdamp3
C     MAXIMUM
      xmax1(ikk)=xdamp1
      xmax2(ikk)=xdamp2
      xmax3(ikk)=xdamp3
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C
```

```
C++++++++++++FIND IF MIL HAS EXCEEDED THE REFERENCE++++++++
      if (zeit1.gt.4500) then
C+++++PHASE 1
       if(amax.gt.errp) then
         sal_a=1.0
       else
         sal_a=0.0
       endif
C+++++PHASE 2
       if(bmax.gt.errp) then
         sal_b=1.0
       else
         sal_b=0.0
       endif
C+++++PHASE 3
       if(cmax.gt.errp) then
         sal_c=1.0
       else
         sal_c=0.0
       endif
       zeit1=0.0
      endif
C++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
C**********IF THE CONDITION TO TRIGGER THE TCSC ARE SET*********
C***************THEN SEND MODULATION SIGNAL********************
C**********+++++++++*********+++++++++********+++++++++*******
C+++++++++VERIFY IF USER INPUT COMMAND SET REFERENCE = 0+++++
C+++++++++(CURRENT AS REFERENCE FOR TCSC MODULATION)+++++++
C
     if ((refe.eq.0).and.(zeit2.gt.trigg)) then
      if(sal_a.gt.0) then
       if ((prox1.gt.top_mar).and.(sal_a.ge.1.0))then
          vdct1=minc

       elseif ((prox1.le.bot_mar).and.(sal_a.ge.1.0)) then
          vdct1=maxc
       else
         vdct1=minc
       endif
      else
        vdct1=nominal
      endif

      if(sal_b.gt.0) then
       if ((prox2.gt.top_mar).and.(sal_b.ge.1.0)) then
          vdct2=minc

       elseif ((prox2.le.bot_mar).and.(sal_b.ge.1.0)) then
          vdct2=maxc
       else
          vdct2=minc
       endif
```

```
      else
        vdct2=nominal
      endif

     if(sal_c.gt.0) then
      if ((prox3.gt.top_mar).and.(sal_c.ge.1.0))  then
         vdct3=minc

      elseif ((prox3.le.bot_mar).and.(sal_c.ge.1.0))  then
         vdct3=maxc
      else
         vdct3=minc
      endif
     else
       vdct3=nominal
     endif

    zeit2=0.0
    endif
C+++++++++++++++THE CONDITION HAS BEEN VERIFIED++++++++++++
C
C+++++++++VERIFY IF USER INPUT COMMAND SET REFERENCE = 1+++++
C+++++++++(CURRENT AS REFERENCE FOR TCSC MODULATION)++++++
C
    if ((refe.eq.1).and.(zeit2.gt.trigg)) then
     if(sal_a.gt.0) then
      if ((prox1.gt.top_mar).and.(sal_a.ge.1.0)) then
         vdct1=maxc

     elseif ((prox1.le.bot_mar).and.(sal_a.ge.1.0)) then
         vdct1=minc

     endif
   else
     vdct1=nominal
   endif

   if(sal_b.gt.0) then
    if ((prox2.gt.top_mar).and.(sal_b.ge.1.0)) then
       vdct2=maxc

    elseif ((prox2.le.bot_mar).and.(sal_b.ge.1.0)) then
       vdct2=minc
    endif
   else
     vdct2=nominal
   endif
   if(sal_c.gt.0) then
    if ((prox3.gt.top_mar).and.(sal_c.ge.1.0)) then
       vdct3=maxc

    elseif ((prox3.le.bot_mar).and.(sal_c.ge.1.0)) then
```

```
            vdct3=minc

          endif
         else
           vdct3=nominal
         endif
       zeit2=0.0
       endif

C+++MODULATION CONTROL SIGNAL HAVE BEEN SENT TO TCSC+++
C*************************************************************
C++++++++++++DATA WINDOWING
      xdp1(ikk+1)=xdp1(ikk)
      xdp2(ikk+1)=xdp2(ikk)
      xdp3(ikk+1)=xdp3(ikk)
      xmax1(ikk+1)=xmax1(ikk)
      xmax2(ikk+1)=xmax2(ikk)
      xmax3(ikk+1)=xmax3(ikk)
      prox1a=prox1
      prox2a=prox2
      prox3a=prox3
      endif
C
C*******CLEAR MIL REGISTERS AND OBTAIN A NEW MAXIMUM
C*******UPDATE EVERY 2 SECONDS
       if(t_maxi.gt.4000) then
         amax=amax/2.0e0
         bmax=bmax/2.0e0
         cmax=cmax/2.0e0
         t_topx=0.0e0
       endif
C
C*************************************************************
C*********END OF TCSC CONTROL SIGNALS PROCESSING************
C*************************************************************
C
C*************************************************************
C*************************************************************
C*****************END OF RT-DIRM CONTROL STRATEGY************
C*************************************************************
C*************************************************************
```

The easy5 built-in block interfacing with the reference and input processing routines are shown in Figures A.1 and A.2, respectively. The TCSC control processing routine makes no use of additional built-in blocks.

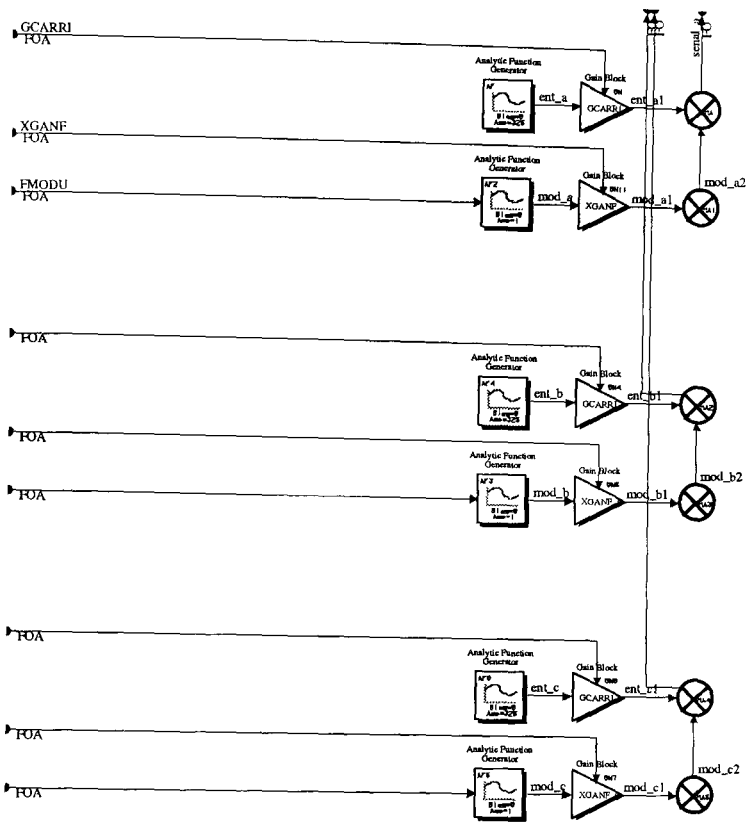

Figure B.1. EASY5 built-in blocks interfacing with the reference routine

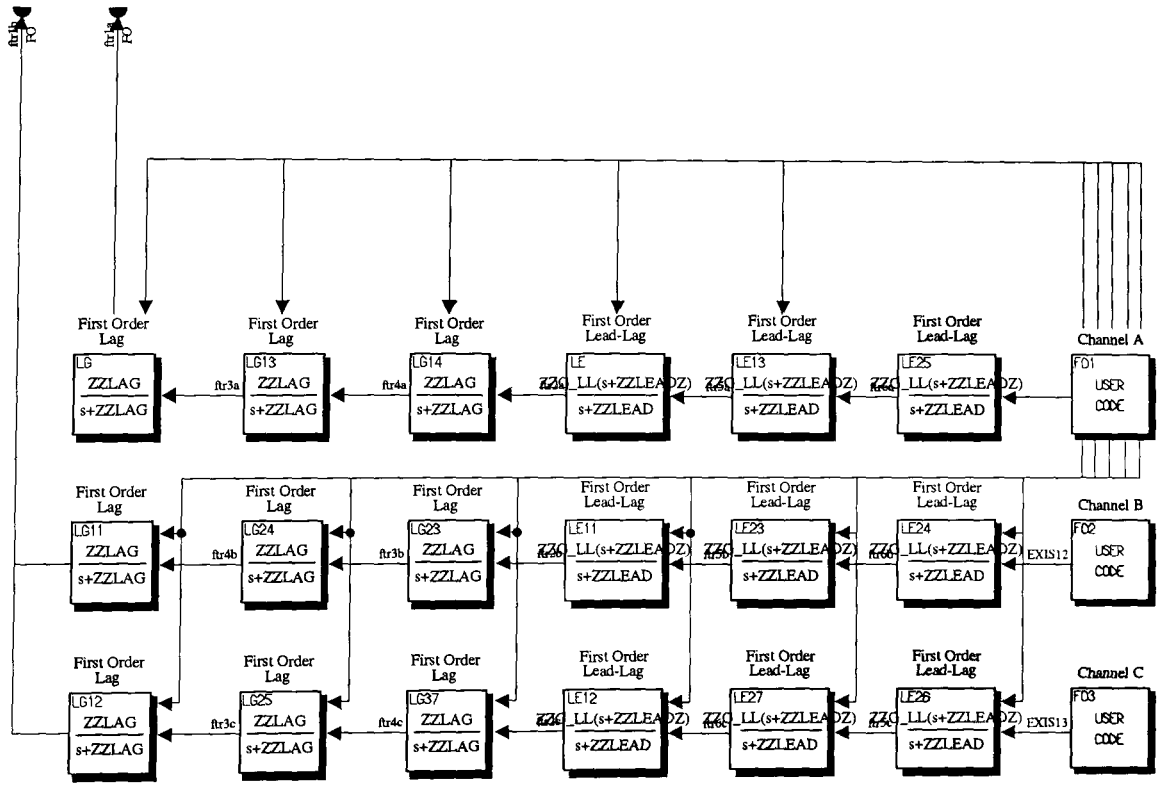

Figure B.2. EASY5 built-in blocks interfacing with the input signal processing routine

APPENDIX

C

SHORT AND LONG-TERM EVALUATION OF THE FLICKER SEVERITY: FORTRAN SOURCE CODE

A real-time virtual IEC-Flickermeter, measuring IFS and P_{st}, has been extensively used in this research work to evaluate the TCSC mitigation performance in real-time. The design characteristics and construction has been detailed in Chapter 7. The FORTRAN source code used to statically evaluate the P_{st} and P_{lt} flicker severity is given below. To the best this Author's knowledge, no equivalent source code is available in the open literature.

```
C*****************************************************************
C*****************************************************************
C       STATICAL EVALUATION OF THE FLICKER SEVERITY
C       BASED ON THE IEC-61000-4-15
C*****************************************************************
C*****************************************************************
C                                                                **
C                          -----CONSTANTS-----                   **
C       TINCR          =STEP INCREMENT (1/TIME OF PROCESSING)    **
C       NCLASSE        = NUMBER OF CLASSES                       **
C       RANGE          =RANGE FOR THE MEASUREMENT                **
C       XFLI           =MAXIMUM LIMIT FOR THE IFS INPUT          **
C       XTST           =MINIMUM PROCESSING STEP                  **
C       CLA()          =MAXIMUM VALUE FOR EACH CLASS             **
C       TST            =CALCULATION LOOP COUNTER                 **
C       TSP            =MONITORING TIME FOR PST CALCULATION      **
C       XSIZE          =LENGHT OF EACH CLASS (STEP)              **
C       INC    =  TIMES THAT THE PST HAS BEEN CALCULATED         **
C       I2     =  INDEX FOR PLT CALCULATIONS                     **
C+++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++
```

```
C       REFERENCE PERCENTILES FOR PST CALCULATION      **
     yref(i)= 0.001                                    **
     yref(i+1)= 0.007                                  **
     yref(i+2)= 0.01                                   **
     yref(i+3)= 0.015                                  **
     yref(i+4)= 0.022                                  **
     yref(i+5)= 0.03                                   **
     yref(i+6)= 0.04                                   **
     yref(i+7)= 0.06                                   **
     yref(i+8)= 0.08                                   **
     yref(i+9)= 0.1                                    **
     yref(i+10)= 0.13                                  **
     yref(i+11)= 0.17                                  **
     yref(i+12)= 0.3                                   **
     yref(i+13)= 0.5                                   **
     yref(i+14)= 0.8                                   **
C************************************************************
C************************************************************
c---------------------------------VARIABLE-------------------------------**
C  XILF        =INSTANTANEOUS FLICKER LEVEL INPUTTED  **
C  PK()        =INTERPOLATED PERCENTILES              **
C  PX()        =PERCENTILES FOR TO EACH CLASS         **
C  TP()        =FREQUENCY DISTRIBUTION FUNCTION       **
C  YN()        =PORCENTUAL PROBABILITY TO EACH CLASS  **
C  PST()       =SHORT TERM FLICKER SEVERITY INDEX     **
C  PLT()       =LONG TERM FLICKER SEVERITY INDEX      **
C************************************************************
C---------------------VARIABLES DECLARATIONS--------------------**
     DECLARATIONS, integer kk,i,i2,nn,l,m,mln1,inn
     DECLARATIONS, real*8 clax(6),cla(64),pk(15),tespe1,tespe2
     DECLARATIONS, real*8 tp(64),pst(999),plt(16),tme1
     DECLARATIONS, real*8 tte(64),yyn(64)
     DECLARATIONS, real*8 xsize,annn,xnn,aa,bb,cc,dd,ee,ff,ae,ai
C************************************************************
C++++++++++++SETTLING TIME COUNTER++++++++++++++++
C+++++(PHYSICAL PROTOTYPE ENERGISATION STAGE)+++++++
     tespe1=tespe1+1.0d0
C***************GENERAL TIME COUNTER*****************
     tsp=(10.0d0*60.0d0)*tincr
C************************************************************
C************************************************************
C       IF THE PROTOTYPE ENERGISATION TIME IS NOT OVER    *
C       GO TO END (110 SECONDS)                           *
     tespe2=(tespe1/tincr)
     if (tespe2.lt.tmed) then
      go to 500
     endif
C*************** INICIALISATION ROUTINE ****************
C************************************************************
C++++++++++++++GENERAL INDICES+++++++++++++++++++++
     kk=1
     i=1
```

```
      i2=1
C++++input under and over-range flags+++++++
      overag=0.0
      undrag=0.0
C++++update monitoring time counter ++++++++
      tst=tst+1.0d0
C*******************initialisation is over*********************
C*****************************************************************
C*BEGINNING OF SEVERITY INDICES CALCULATION PROCESS**
C*****************************************************************
C--------calculate class maximum length----------
      xsize=(1.0d0/nclasse)*xfli
C
C*********IF THE INPUT EXCEEDES THE MAXIMUM INPUT******
C****************** THEN INPUT=MAX************************
      if(xilf.gt.xfli) then
        xilf=(xfli*0.9999)
        overag=1.0
      endif
C*****IF THE INPUT IS ZERO OR NEGATIVE THEN SET INPUT****
C*****EQUAL TO 1E-5                                      ****
      if(xilf.le.0.0) then
        xilf=1.0e-5
        undrag=0.0
      endif
C
C**********MAXIMUM LEVEL FOR EACH CLASS**************
C*****************************************************************
      do i=nclasse,1,-1
        cla(i)=(0.015625)*xfli*(i*1.0d0)
      end do
C----------------------SAMPLE IFL AT THE INPUT-------------------------
      xilf=xilf
C-------------------------------------------------------------------------------
C     CALCULATE CLASS POSITION USING MOD(XILF/XSIZE) + 1
C-------------------------------------------------------------------------------
      annn=(xilf/xsize)
      inn=annn
      nn=inn+1
C---------------------THE UPPER LIMIT IS NCLASS--------------------------
      if (nn.gt.nclasse) then
        nn=nclasse
      endif
      xnn=nn
C-------------------------------------------------------------------------------
C                    CALCULATION OF CLASS PERTENENCE
C                 (OR FREQUENCY DISTRIBUTION FUNCTION)
c-------------------------------------------------------------------------------
      tp(nn)=tp(nn)+1
      tpx(nn)=tp(nn)
C-------------------------------------------------------------------------------
```

```
C*************************************************************
C   THE CALCULATION OF PERCENTILES REQUIRED FOR PST  **
C   CALCULATION IF TST IS EQUAL OR GREATER THEN THE   **
C   REFERENCE OBSERVATION TIME TSO                    **
C*************************************************************
    if (tst.ge.tsp) then
C********SEARCH FOR YK'S WHICH CORRESPONDE TO*********
C**THE PERCENTILESNEDEED FOR THE CALCULATION OF PST**
C*************************************************************
C-------------------------------------------------------------------------
C       CALCULATION OF EXCESS TIME TE() AND
C       PORCENTUAL PROBABILITY FOR EACH CLASS
C-------------------------------------------------------------------------
C       SPECIAL CASE FOR MAX CLASS
C       FIRST CALCULATION BEGINS WITH NCLASSE-1
C-------------------------------------------------------------------------
     te(nclasse)=0.0
     yn(nclasse)=0.0
     do i=nclasse-1,1,-1
        tte(i)=tte(i+1)+tp(i+1)
        te(i)=tte(i)
        yyn(i)=tte(i)*xtst
        yn(i)=yyn(i)
      enddo

C-------------------------------------------------------------------------
C       CALCULATION Y0 BY INTERPOLATION
C-------------------------------------------------------------------------
     y0 = 3*yn(kk)-3*yn(kk+1)+yn(kk+2)
C-------------------------------------------------------------------------
C------IF THE INSTANTANEOUS FLICKER BELONGS ONLY TO
C------THE FIRST CLASSE Y0 IS ZERO-------------------------------

     if ((y0.le.0).and.(yn(kk).le.0)) then
       y0=tp(kk)*xtst
     endif
C-------------------------------------------------------------------------------------
C       CLASIFICATION OF PORCENTUAL PROBABILITY;
C       CALCULATION OF PERCENTILES; AND DIRECT
C       CALCULATION OF SHORT AND LONG TERM SEVERITY
C       INDEX
C-------------------------------------------------------------------------------------
     i=1
     do l=1 ,15
      if (yref(l).lt.yn(i+31)) then
C*******FIRST PART OF THE SEARCH TREE. YN VALUES *********
C*******ABOVE 32ND PERCENTILE*****************************
        if (yref(l).lt.yn(i+47)) then
          if (yref(l).lt.yn(i+55)) then
            if (yref(l).lt.yn(i+59)) then
              if (yref(l).lt.yn(i+61)) then
                if (yref(l).lt.yn(i+62)) then
```

```
            m=64
    go to 100
    else
            m=63
    go to 100
    endif
  elseif (yref(l).lt.yn(i+60)) then
            m=62
  go to 100
  else
            m=61
  go to 100
  endif
elseif (yref(l).lt.yn(i+57)) then
          if (yref(l).lt.yn(i+58)) then
               m=60
     go to 100
          else
               m=59
     go to 100
          endif
elseif (yref(l).lt.yn(i+56)) then
          m=58
go to 100
else
          m=57
go to 100
  endif
elseif (yref(l).lt.yn(i+51)) then
     if (yref(l).lt.yn(i+53)) then
      if (yref(l).lt.yn(i+54)) then
       m=56
      go to 100
      else
       m=55
      go to 100
      endif
     elseif (yref(l).lt.yn(i+52)) then
         m=54
     go to 100
        else
         m=53
     go to 100
     endif
elseif (yref(l).lt.yn(i+49)) then
         if (yref(l).lt.yn(i+50)) then
           m=52
         go to 100
         else
           m=51
         go to 100
         endif
```

```
 elseif (yref(l).lt.yn(i+48)) then
            m=50
 go to 100
 else
            m=49
 go to 100

 endif
elseif (yref(l).lt.yn(i+39)) then
     if (yref(l).lt.yn(i+43)) then
      if (yref(l).lt.yn(i+45)) then
       if (yref(l).lt.yn(i+46)) then
         m=48
       go to 100
       else
         m=47
       go to 100
       endif
      elseif (yref(l).lt.yn(i+44)) then
          m=46
      go to 100
      else
          m=45
      go to 100
      endif
     elseif (yref(l).lt.yn(i+41)) then
         if (yref(l).lt.yn(i+42)) then
           m=44
         go to 100
         else
           m=43
         go to 100
         endif
      elseif (yref(l).lt.yn(i+40)) then
           m=42
      go to 100
      else
           m=41
      go to 100
      endif
elseif (yref(l).lt.yn(i+35)) then
       if (yref(l).lt.yn(i+37)) then
        if (yref(l).lt.yn(i+38)) then
          m=40
        go to 100
        else
          m=39
        go to 100
        endif
       elseif (yref(l).lt.yn(i+36)) then
           m=38
       go to 100
```

```
                else
                    m=37
                go to 100
                endif
            elseif (yref(l).lt.yn(i+33)) then
                    if (yref(l).lt.yn(i+34)) then
                      m=36
                    go to 100
                    else
                      m=35
                    go to 100
                    endif
             elseif (yref(l).lt.yn(i+32)) then
                        m=34
             go to 100
             else
                        m=33
             go to 100
             endif
C***** SECOND PART OF THE SEARCH TREE *******
           elseif (yref(l).lt.yn(i+15)) then
              if (yref(l).lt.yn(i+23)) then
               if (yref(l).lt.yn(i+27)) then
                if (yref(l).lt.yn(i+29)) then
                  if (yref(l).lt.yn(i+30)) then
                        m=32
                  go to 100
                  else
                   m=31
                  go to 100
                  endif
                elseif (yref(l).lt.yn(i+28)) then
                        m=30
                go to 100
                else
                        m=29
                go to 100
                endif
              elseif (yref(l).lt.yn(i+25)) then
                      if (yref(l).lt.yn(i+26)) then
                            m=28
                  go to 100
                      else
                            m=27
                  go to 100
                      endif
              elseif (yref(l).lt.yn(i+24)) then
                            m=26
              go to 100
              else
                            m=25
              go to 100
```

```
  endif
elseif (yref(l).lt.yn(i+19)) then
    if (yref(l).lt.yn(i+21)) then
     if (yref(l).lt.yn(i+22)) then
      m=24
     go to 100
     else
      m=23
     go to 100
     endif
    elseif (yref(l).lt.yn(i+20)) then
        m=22
    go to 100
    else
        m=21
    go to 100
    endif
elseif (yref(l).lt.yn(i+17)) then
        if (yref(l).lt.yn(i+18)) then
          m=20
        go to 100
        else
          m=19
        go to 100
        endif
elseif (yref(l).lt.yn(i+16)) then
          m=18
    go to 100
    else
            m=17
    go to 100
    endif
elseif (yref(l).lt.yn(i+7)) then
       if (yref(l).lt.yn(i+11)) then
        if (yref(l).lt.yn(i+13)) then
         if (yref(l).lt.yn(i+14)) then
           m=16
         go to 100
         else
           m=15
         go to 100
         endif
        elseif (yref(l).lt.yn(i+12)) then
           m=14
        go to 100
        else
           m=13
        go to 100
        endif
       elseif (yref(l).lt.yn(i+9)) then
          if (yref(l).lt.yn(i+10)) then
           m=12
```

```
                go to 100
                else
                  m=11
                go to 100
                endif
          elseif (yref(l).lt.yn(i+8)) then
                  m=10
          go to 100
          else
                  m=9
          go to 100
          endif
elseif (yref(l).lt.yn(i+3)) then
          if (yref(l).lt.yn(i+5)) then
           if (yref(l).lt.yn(i+6)) then
             m=8
           go to 100
           else
             m=7
           go to 100
           endif
          elseif (yref(l).lt.yn(i+4)) then
              m=6
          go to 100
          else
              m=5
          go to 100
                endif
        elseif (yref(l).lt.yn(i+1)) then
                  if (yref(l).lt.yn(i+2)) then
                    m=4
                  go to 100
                  else
                    m=3
                  go to 100
                  endif
        elseif (yref(l).lt.yn(i)) then
                    m=2
        go to 100
        else
                    m=1
        go to 100

C-----------------------------END OF SECOND PART-----------------------------*
      endif
C**********************END OF SEARCH TREE**********************
C
C************CALCULATION OF PK. M1= IS EXCLUDED*************
100   if (m.gt.1) then
        pk(l)=xsize*(m-((yref(l)-yn(m))/(yn(m-1)-yn(m))))
      else
        pk(l)=xsize*(1-((yref(l)-yn(m))/(y0-yn(m))))
```

```
      endif
      ppk(l)=pk(l)
c      im=m
     enddo
C------END OF SEARCH AND CALCULATION OF-------------------
C------PERCENTILES 0.1,0.7,1,1.5,2.2,3,4,6,8,10,13,17,30,50,80
C-------------------------------------------------------------------------
      inc=inc+1
C
C---------+++CALCULATION OF SHORT TERM SEVERITY INDEX+++-----
C      PST=SQRT(0.0314P0.1+0.0525P1S+0.0657P3S+0.28P10S+0.08P50S)----
C      P0.1,P1,P3,P10  AND P50 ARE THE IFS LEVELS EXCEDED FOR---
C      0.1,1,3,10 AND 50% OF THE TIME DURING THE OBSERVATION-
C      PERIOD
C
C      THE SMOOTHEST VALUES S ARE OBTAINED USING EQUATIONS  *
C        P50S= (P30+P50+P80)/3
C        P10S= (P6+P8+P10+P13+P17)/5
C        P3S = (P2.2+P3+P4)/3
C        P1S = (P0.7+P1+P1.5)/3
C*************************************************************
         p50s=(pk(kk+12)+pk(kk+13)+pk(kk+14))*0.333333
         p10s=(pk(kk+7)+pk(kk+8)+pk(kk+9)+pk(kk+10)+pk(kk+11))*0.2
         p3s= (pk(kk+4)+pk(kk+5)+pk(kk+6))*0.333333
         p1s= (pk(kk+1)+pk(kk+2)+pk(kk+3))*0.333333
         aa=0.0314*pk(kk)
         bb=0.0525*p1s
         cc=0.0657*p3s
         dd=0.28*p10s
         ee=0.08*p50s
         ff=aa+bb+cc+dd+ee
         pst1=sqrt(ff)
         pst(inc)=pst1
C***************END OF CALCULATION OF PST**********************
C*************************************************************
C******************CALCULATION OF PLT*************************
C
         if (inc.ge.12) then
        do i=1, 12
            ae=ae+(pst(i)*pst(i)*pst(i))
          enddo
        ae=ae*0.083333
C*******CUBIC ROOT FROM FORTRAN 77 , G.J. BORSE PAG. 357***
        ai=ae-1.0d0
        plt1=1+(0.3333*ai)-(0.11111*ai*ai)+(0.061728*ai*ai*ai)
        plt(i2)=plt1
           inc=1
        i2=i2+1
         endif
C******END OF PLT CALCULATION
C
C******ZEROING VECTORS
```

```
      do i=nclasse,1,-1
        tp(i)=0.0
        tpx(i)=0.0
        yyn(i)=0.0
        tte(i)=0.0
        yn(i)=0.0
        te(i)=0.0
      enddo
      do i=15,1,-1
        pk(i)=0.0
        ppk(i)=0.0
      enddo

C*******CLEAN MONITORING TIME COUNTER *******
      tst=0
c*******ENDIF BELONGING TO IF(TST.GT.TSP)
      endif
500   tme1=tme1+1.0d0
C***************************************************************
C***************************************************************
C************END OF EVALUATION OF SHORT AND LONG***************
C******************FLICKER SEVERITY INDICES**********************
C***************************************************************
C***************************************************************
```