Gold free ohmic contacts for III-V MOSFET devices

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Wout A. T. Jansen

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Abstract

Over the past forty years the development of CMOS has been able to follow Moore's law using planar silicon technology. However, this technology is reaching its limits as the density of transistors has a significant impact on the power dissipation in an integrated circuit. Alternative channel materials and device architectures will then be required in the future to reduce the power consumption of transistors. The development of CMOS technology with high mobility channel materials, specifically Ge for pMOS and III-V materials for nMOS, was the aim of the European Union FP7 funded Duallogic consortium, of which this project was part.

The experimental work at the University of Glasgow was the III-V compound semiconductor MOSFET, in particular the study of Si processing compatible source/drain contacts to III-V MOSFET devices with $In_xGa_{1-x}As$ channel materials, which was an important aspect of this thesis. Another area investigated in this thesis is the impact of current crowding effects on source/drain contact resistance by aggressive scaling of devices.

During this thesis, optimisation of a PdGe-based ohmic contact to buried channel device material with a $In_{0.75}GaAs$ channel led to a contact resistance of 0.15Ω.mm compared to 1Ω.mm in previous work by R. Hill. The PdGe-based contact also proved to be scalable in both vertical and lateral dimensions. This scaled structure was then integrated in a surface channel MOSFET device with 1µm access regions and gate lengths varying from 100nm to 20µm. The performance of the devices with 20µm gate lengths was then compared to devices with a NiGeAu based ohmic contact. An increase in R_C, 1.82Ω.mm vs. 0.94Ω.mm, and R_{on}, 11.1Ω.mm vs. 8.55Ω.mm, was observed in the PdGe-based contact, which resulted in a decrease in g_m, 92.3mS/mm vs. 103mS/mm, and $I_{d,sat}$, 103mA/mm vs. 122mA/mm. However, further optimisation of the PdGe-based ohmic contact showed promising results with a contact resistance of 0.45Ω.mm.

The novel test structure is the first test structure, which makes direct contact to III-V material, with critical dimensions below the transfer length. This structure is able to experimentally observe the current crowding effects and allows for the extraction of the sheet resistance underneath the contact and a more accurate extraction of the specific contact resistivity. This offers a significant insight into the impact of the sheet resistance underneath the contact and the role it plays.

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List of Abbreviations

2DEG	Two-Dimensional Electron Gas
AC	Alternating Current
ADF	Annular Dark Field
ALD	Atomic Layer Deposition
CAD	Computer Aided Design
CBKR	Cross Bridge Kelvin Resistor
CET	Capacitive Effective Thickness
CMOS	Complementary Metal Oxide Semiconductor
CTLM	Circular Transmission Line Model
CVD	Chemical Vapour Deposition
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DUT	Device Under Test
EACPE	Energy to Activate Chemical Plasma Etching
E-BEAM	Electron-Beam
EELS	Electron Energy Loss Spectroscopy
EOT	Equivalent Oxide Thickness
FCTLM	Floating-Contact Transmission Line Model
FE	Field Emission
FFT	Fast Fourier Transform
FINFET	Fin Field Effect Transistor
GF	Gate First

GGO	GaGdO (oxide)
GL	Gate Last
GPIB	General Purpose Interface Bus
HEMT	High Electron Mobility Transistor
ICP	Inductively Coupled Plasma
IMEC	Semiconductor research facility in Leuven, Belgium
IPA	Isopropyl Alcohol
ITRS	International Technology Roadmap for Semiconductors
JWNC	James Watt Nanofabrication Center
MBE	Molecular Beam Epitaxy
MEK	Methyl Ethyl Ketone
MIBK	Methyl Isobutyl Ketone
MIGS	Metal Induced Gap States
MLLS	Multiple Linear Least Square
MOCVD	Metal-Organic Chemical Vapour Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
nMOS	n-type Metal Oxide Semiconductor
PECVD	Plasma Enhanced Chemical Vapour Deposition
PMMA	Poly-Methyl Methacrylate
pMOS	p-type Metal Oxide Semiconductor

RF	Radio-Frequency
RHEED	Reflection High Electron Energy Diffraction
RIE	Reactive Ion Etching
SCE	Short Channel Effects
SEM	Scanning Electron Microscopy
SOI	Silicon on Insulator
SS	Subthreshold Swing
STEM	Scanning Transmission Electron Microscopy
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TFE	Thermionic-Field Emission
TLM	Transmission Line Model
TMA	Trimethyl Aluminium
TTL	Transistor-Transistor Logic
UHV	Ultra High Vacuum
UV	Ultra-Violet
VLSI	Very Large Scale Integration
XRD	X-Ray Diffraction

1. Associated publications

Jansen, W., Li, X. and Thayne, I. G. (2010) "Investigation of sub-micrometer ohmic contacts for III-V applications", *Hetech presentation*

Thayne, I.G., Bentley, S., Holland, M., Jansen, W., Li, X., Macintyre, D.S., Thoms, S., Shin, B., Ahn, J. and Mcintyre, P. (2011) "III-V nMOSFETs – Some issues associated with roadmap worthiness (invited)", *Microelectronic Engineering*, vol. 88, pp. 1070-1075.

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Jansen, W., Li, X., Thoms, S., Macintyre, D., and Thayne, I.G., "Novel test structure to investigate the behaviour of current crowding effects on ohmic contacts for III-V applications", *Electronics Device Letters*

Jansen, W., Li, X., Thoms, S., Macintyre, D., and Thayne, I.G.,"Impact of nanoscale metal deposition on the semiconductor sheet resistance underneath the contact metal", *Applied Physics Letters*

Jansen, W., Li, X., Thoms, S., Macintyre, D., and Thayne, I.G.,"Investigation of the sheet resistance underneath a source/drain ohmic contact using a scaled Transmission Line Model Characterisation method", *Transactions on Electron Devices*

2. Introduction

Over the past forty years, the development of CMOS has been able to follow Moore's law due to ever-shrinking transistor dimensions. This trend is set to continue in the future and is laid out by the International Technology Roadmap for Semiconductors [1]. This roadmap outlines the performance metrics and device dimensions, which need to be met by future technology nodes and are shown in Table 2.1. In recent years, density scaling has been the main driver in the mainstream semiconductor industry and has had significant ramifications for power dissipation in integrated circuits. Reducing the power dissipation of individual MOSFETs has led to innovative solutions such as high-k gate dielectrics and metal gate solutions, strained Si and Tri-gate field effect transistors [2].

The reduction of supply voltages will be one of the key aspects in the future to reduce power dissipation, as shown in Table 2.1. The density of scaling will be driven by scaling the source/drain contact length, physical gate length and the separation between the contacts and the gate, as shown in Table 2.1. As a consequence of scaling the device dimensions, regardless of novel high-k dielectrics, the ITRS [1] predicts a reduction in gate capacitance as shown in Table 2.1. In order to compensate the reduced supply voltage and the reduced gate capacitance, the effective carrier velocity will have to increase over time to compensate a loss in channel sheet carrier density.

Year	2015	2018	2020	2024
Physical gate length (nm)	17	13	11	7
Source and drain contact length (nm)	13	9	7	4
Total source drain resistance (Ω.mm)	0.14	0.13	0.12	0.11
Supply voltage (V)	0.81	0.73	0.68	0.6
Threshold voltage (V)	0.21	0.21	0.22	0.23
Effective carrier velocity (m/s)	$2.6x10^5$	$2.3x10^5$	$2.6x10^5$	$3.5x10^5$
Channel sheet carrier density (cm^{-2})	$7.3x10^{12}$	$7.1x10^{12}$	$6.4x10^{12}$	$5.1x10^{12}$
Gate capacitance (fF/µm)	0.5	0.42	0.37	0.28

Table 2.1: Various derived parameters and ITRS metrics taken from the 2009/2010 ITRS roadmap [1].

High carrier velocities in non-equilibrium conditions will then play a key role in future MOSFETs. The effective carrier velocity mainly depends on scattering mechanisms and the low-effective mass, which can be addressed by using a device architecture featuring reduced ionised impurity scattering and carefully chosen material compositions.

In order to research CMOS using high effective carrier velocity channel materials, the "Duallogic project" was founded and sponsored by the European Commission 7th framework program (FP7) in information and communication technologies. The objective of the Duallogic project was to develop a dual channel CMOS technology comprising MOSFETs with high channel mobility semiconductor materials co-integrated on a Si platform using a silicon-compatible process in a 65nm/200mm pilot line. The respective semiconductor materials are Ge for pMOS and III-V compounds for nMOS. The device dimensions were chosen to offer a competitive alternative for the state of the art Si CMOS. At the start of the project, the proposed gate length was 65nm, however at the point of writing, a 22nm technology is already commercially available by Intel [2]. The original structure is shown in Figure 2.1 and illustrates an III-V nMOS and Ge pMOS co-integrated on a Si platform.

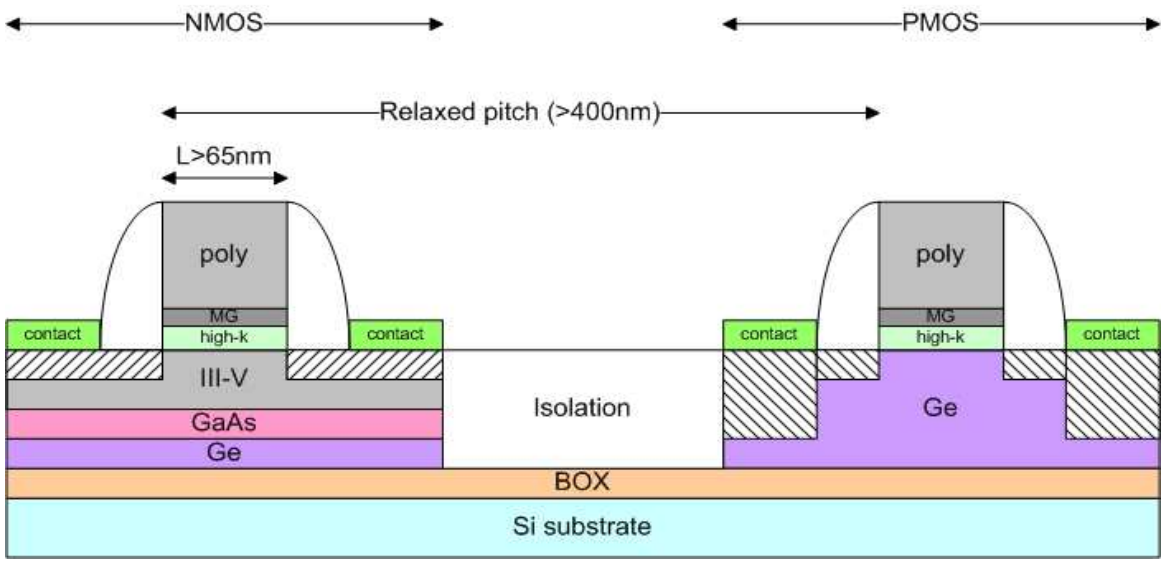


Figure 2.1: Duallogic 65nm layout

The consortium of the Duallogic project consists of research centres, equipment manufacturers, chip manufacturers and universities, including Aixtron, CEA-LETI, IBM, IMEC, Katholieke Universiteit Leuven, National Centre for Scientific Research Demokritos, NXP Semiconductors, ST Microelectronics and the University of Glasgow. The University of Glasgow was involved in two different areas: device simulation and device fabrication. The focus of the work of this thesis is the n-type III-V transistor with

particular emphasis on developing low resistance, silicon processing compatible source/drain ohmic contacts. This requires the development of gold free ohmic contacts because gold is an amphoteric material in silicon, which means that the behaviour of gold is unpredictable in silicon and can act as both donor and acceptor. The gold free ohmic contact results will be compared to the current best ohmic contact to III-V material, which are usually based on alloys of gold, germanium and nickel [3] with specific contact resistivities as low as $4x10^{-7}\Omega.cm^2$.

At the start of this work, there was much debate over which device architecture to use within the DualLogic consortium. Previous work at the University of Glasgow [4] using a flatband architecture [5] showed promising results and therefore this device structure was used in this work as well. In comparison to the more traditional inversion mode MOSFET, this structure does not need any implantation, which makes it easier to scale and reduces ionised scattering by making use of a heterojunction. In terms of scaling, flatband MOSFETs have an advantage over inversion mode MOSFETs as they have no p-n junctions. The p-n junctions are formed in the channel region between the ohmic contacts and the gate, also known as the access regions. Future technology nodes, with gate lengths of 15nm or smaller, are predicted to have access regions below 10nm [1]. In order to achieve p-n junction widths in silicon below 10nm, the doping levels will have to surpass $3x10^{19}cm^{-3}$ and keep increasing with each technology node. Obviating the need of a p-n junction will therefore aid the scaling of the access regions. Therefore, the flatband structure should be a serious competitor in terms of scalability and effective carrier velocity compared to the current silicon device technology.

The requirement to compete with Si technology regarding device dimensions will limit the sizes of the gates, access regions and contact areas. High electron mobility transistors (HEMT) have been built at the University of Glasgow on III-V materials with 10nm gate lengths [6], which show small gate III-V devices are possible to build. However, the source/drain contact areas on HEMT's are a lot bigger than the contact areas needed for a sub 22nm digital technology. In order to understand the effects of aggressively scaled ohmic contacts, simulations have been undertaken and test structures have been built to validate the simulations.

There are therefore two issues to consider in undertaking any research into source/drain contacts for III-V MOSFETs:

i) The contact geometries are scalable,

ii) The materials solutions are silicon manufacturing compatible.

The scalability issue is well captured in Figure 2.2, which shows theoretically how the resistance of a source or drain contact varies with the size of the structure according to the H.H. Berger model [7]. Basically, this is a reflection of current crowding effects, which increase the effective resistance of the contact as its size is reduced. To some extent, the current crowding issue can be mitigated if the specific contact resistivity (ρ_c) can be reduced. The contact resistance is governed by two factors:

i) The sheet resistance of the material beneath the source or drain metallisation, which may be modified from the underlying semiconductor sheet resistance if contact formation is facilitated by diffusion,

ii) The "transfer length" – a measure of the length scale over which current is injected into the underlying semiconductor from the edge of the source or drain contact.

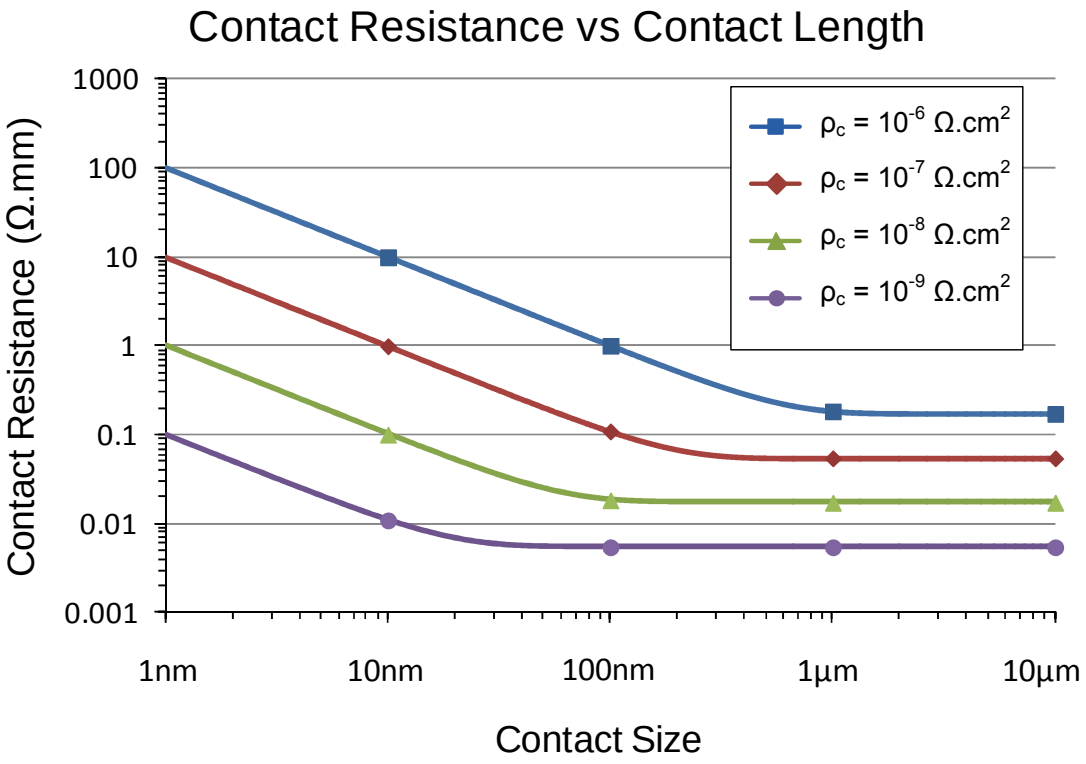


Figure 2.2: Simulated impact of source and drain contact size on contact resistance due to current crowding effects with specific contact resistivities in the range of 10^{-6} to $10^{-9}\Omega cm^2$.

The simulation, shown in Figure 2.2, demonstrates the current crowding effects, on the contact resistance values, taking place on a substrate with a sheet resistance of 300Ω/sq with specific contact resistivity values in the range $10^{-6}\Omega cm^2$ to $10^{-9}\Omega cm^2$. These specific contact resistivity values are achievable for low bandgap III-V semiconductors, though the former is much more prevalent than the latter. As shown in Table 2.1, the total source/drain access resistance should be below 0.14Ω.mm in future technology nodes. This results in a contact resistance value below 0.07Ω.mm which can only be achieved if the specific contact resistivity is below $1x10^{-8}\Omega.cm^2$ for a contact length of 13nm. Further scaling of the source and drain contact lengths will then have significant impact on the maximum specific contact resistivity value due to the current crowding effects.

One of the aims of this work is to validate, or otherwise, this prediction by assessing the dependence of contact resistance on contact length down to 100nm critical geometries. A further aspect of this work is to screen various contact metallisation options with regard to scalability, silicon manufacturing compatibility and of course, basic electrical performance where the key metric is the specific contact resistivity.

This thesis will first describe the theory of MOSFET device operation, the fabrication processes and tools and the characterisation methods used. Then a study of various ohmic contact structures on GaAs based semiconductor is undertaken and is used to determine the optimal ohmic contact strategy. This is followed by an experimental section, which verifies the electrical and chemical properties of different Si-processing compatible ohmic contact strategies including device results. The final part describes a novel measurement method in order to determine the contact resistance when the ohmic contacts are scaled. This includes the theory, concept, processes and techniques developed for reliable sub-micrometer scaled ohmic contacts and the experimental results. The experimental results are then compared to the most common contact resistance extraction methods.

3. MOSFET theory

3.1 Introduction

The ideal operation of the classic bulk silicon MOSFET is first described, which will later act as a benchmark to compare the III-V MOSFET technology against. Then the advantages of density scaling are discussed together with different scaling methodologies and the key parameters, which are impacted by the reduction of the device dimensions. The figures of merit for a scaled n-type MOSFET are shown with Intel 45nm technology as a benchmark.

A more in depth study of the metal/oxide/ semiconductor interface, channel transport properties and metal semiconductor contacts, is then undertaken to get a better understanding of the potential benefits of III-V channel material. Finally, MOSFET devices with advanced architectures will be discussed and compared to the classic bulk silicon MOSFET.

3.2 MOSFET principles

The classic bulk silicon MOSFET is illustrated in Figure 2.1 for the case of an n-type enhancement mode MOSFET. The silicon substrate material is p-type doped whereas the source/drain regions are n-type doped, achieved by diffusion, regrowth or implantation. Two p-n junctions in opposite direction are then formed between the source and the drain. The gate electrode is isolated from the channel by an insulator, which reduces the current flow from the gate into the source.

The operation of an ideal classic bulk MOSFET will be described using an inversion mode device with a long channel. This means that the influence of the electric field imposed by the gate (ξ_y), in the channel region, is far greater than the impact of the electrical field from the source/drain p-n junctions (ξ_x) when biased. The channel of an n-type inversion mode MOSFET device is p-type doped and therefore needs a positive voltage applied to the gate to accumulate an inversion channel of electrons. The areas underneath the source and drain ohmic contacts are n-type doped hence forming a p-n junction between the channel and contact region when no gate voltage is applied. When a small bias is applied between the source and drain, no current flows until the source/gate voltage (V_g) becomes higher than the threshold voltage (V_t). Once V_g is larger than V_t, an inversion layer of electrons forms at the semiconductor oxide interface, which supports a source/drain current (I_d).

In the linear regime, where $V_d < (V_g - V_t)$ and $(V_g - V_t) > 0$, I_d is dependent on the modulation of V_g and on the source/drain bias V_d as stated by Equation 3.1 [8].

$$I_d = \frac{W}{L_g} \mu C_{ox} \left[(V_g - V_t) V_d - \frac{V_d^2}{2} \right] \quad (3.1)$$

W and L_g are the gate width and gate length, as shown in Figure 3.1, μ is the mobility of the semiconductor material in the channel and C_{ox} is the capacitance of the oxide. In the saturation regime, $V_d > (V_g - V_t)$, threshold is barely maintained at the drain end. This threshold region is also known as pinch-off to indicate the lack of channel region near the drain. The pinch-off point in the channel will consequently move towards the source when V_g is further increased. The high longitudinal electric field will then allow the electrons to travel at saturation drift velocity from the drain towards the pinch-off region. The drain current, at this point ($I_{d,sat}$), does not increase significantly with V_g and therefore it is said to be in saturation regime. The value of $I_{d,sat}$ is given in Equation 3.2 [8].

$$I_{d,sat} = \frac{W}{2L_g} \mu C_{ox} (V_g - V_t)^2 \quad (3.2)$$

When devices are scaled, the long channel approximation above is no longer valid. The saturation current for a short channel device is given in Equation 3.3 [8] and is dependent on the velocity saturation (υ_{sat}) rather than the mobility.

$$I_{d,sat} = W \upsilon_{sat} C_{ox} (V_g - V_t) \quad (3.3)$$

Velocity saturation is one of the side effects when MOSFET devices are being scaled. The beneficial and detrimental effects of scaling MOSFET devices are discussed in following section.

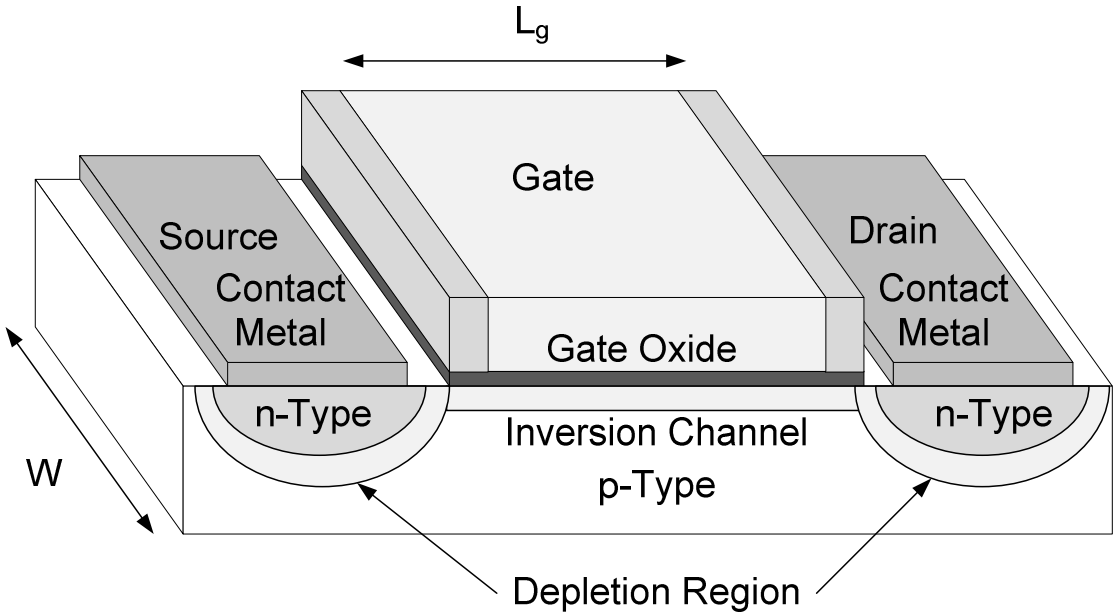


Figure 3.1: Schematic representation of inversion mode nMOSFET

3.3 Scaling

One of the advantages of scaling devices is that the density of devices increases on a chip, however there are also benefits to the performance of a single device. One major advantage is the reduction of intrinsic gate delay (τ_i). The reduction in gate delay allows for faster switching of the device, hence improving the performance of the device and the overall circuit.

$$\tau_i = \frac{C_g V_d}{I_{d,sat}} \tag{3.4}$$

As shown in Equation 3.4 [8], the intrinsic gate τ_i delay is determined by the supply voltage V_d, saturation current $I_{d,sat}$ and the total gate capacitance C_g. The total gate capacitance comprises the intrinsic gate capacitance (C_{ox}) and additional parasitic capacitive elements. Reducing the area ($W.L_g$) of the gate will then result in a proportionally reduced gate capacitance. Scaling of the gate will then directly result in a reduced gate delay τ_i as stated in Equation 3.4. To maintain the ideal characteristics of a long channel MOSFET, other parameters have to be scaled together with the gate length L_g. One of the key attributes, which needs scaling is the oxide thickness. When scaling the gate oxide C_{ox}, the saturation current $I_{d,sat}$ reduces as stated in Equation 3.2.

When simplifying the gate capacitance to a parallel plate capacitor, the oxide capacitance is then given by [8]:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{d} \quad (3.5)$$

The oxide capacitance is determined by the dielectric constant of the oxide (ε_{ox}), the capacitor area (A) and the oxide thickness (d). Decreasing the oxide thickness will result in a larger value for C_{ox}, which increases $I_{d,sat}$. The intrinsic gate delay reduces as $I_{d,sat}$ increases and scaling the oxide thickness has therefore a beneficial impact on the device performance.

When reducing the gate length of a MOSFET device, without altering other key parameters, the ideal long channel behaviour is no longer valid. In particular the depletion layer width of the p-n junctions at the source and the drain has to be larger than the gate length. When the gate length becomes comparable to the depletion region width, the distribution of carriers in the channel is then a function of both ξ_x and ξ_y and the long channel behaviour is lost. The detrimental effects of a loss in long channel behaviour are: reduced gate control; threshold voltage variations; increased off-state current and drain induced barrier lowering (DIBL). These effects are called short channel effects [204] and are caused by: source/drain depletion regions merging in the channel (also known as punch through); surface scattering; velocity saturation; impact ionisation and hot electrons and will be discussed more extensively further in this chapter. These effects will have to be taken into account when designing scaled device structures.

3.3.1 Key parameters to scale

The channel charge control has to be maintained when reducing the gate length to keep the long channel ideal characteristics. There are four main parameters, which need to be scaled together with the gate length: junction depth, supply voltage, oxide thickness and doping concentration.

Each of the parameters and their scaling advantages and limits will be discussed briefly in this section. Alternative technologies, used to scale devices without short channel effects, are analysed further in the chapter.

1) Junction depth: If the junction depth is too large, punch through can take place below the channel [9]. However, a sufficient junction depth is needed in an inversion mode device to reduce the parasitic series resistance of the ohmic regions. Increased series resistance limits the transistor performance and can play a

dominant role. Regrown source/drain regions are currently being used in Si 45nm technology [10] to mitigate this issue. Regrowing allows for high doping concentrations resulting in reduced ohmic contact resistances. The shape of the regrown area can also be manipulated so that the distance between the source and the drain gradually becomes bigger when moving from the oxide/semiconductor interface towards the substrate. This would reduce the punch through below the channel.

2) Channel doping concentration: The depletion region width of a source/drain p-n junction is important in inversion mode devices as the gate control is lost when the depletion region protrudes underneath the gate. This limits the size of the access regions, increasing the distance between the source and the drain contact resulting in overall larger device dimensions. The depletion region width of a p-n junction between the source and the channel (x_{ds}) and drain and channel (x_{dd}) is defined by [8]:

$$x_{ds} = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)(V_{bi})} \tag{3.6}$$

$$x_{dd} = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A+N_D}{N_A N_D}\right)(V_d + V_{bi})} \tag{3.7}$$

The depletion region width is dependent on the potential difference under equilibrium between the p-type channel and the n-type source/drain regions, also known the built in potential (V_{bi}), the channel acceptor concentration and the permittivity (ε_s) of the semiconductor material. In order to minimise the depletion region width, the channel acceptor concentration has to be as high as possible. Higher channel doping concentrations are then necessary to avoid punch through and loss in gate control, when scaling down MOSFET devices.

Although increased doping densities are beneficial to reduce short channel effects, the mobility of the channel material decreases due to increased ionised impurity scattering. A reduction in mobility has a detrimental effect on the saturation current $I_{d,sat}$ as stated in Equation 3.2. The solution to counter for a loss in mobility in current 45nm technology is to introduce strain in the channel region [10].

3) Dielectric thickness: The two-dimensional field distribution in the channel of the device is dependent on the thickness of the gate insulator and influences the threshold voltage (V_t) and the current flowing from the gate to the source, also known as gate leakage. The critical thickness of a gate oxide is then determined by the limit where electron tunnelling starts taking place, resulting in excessive leakage currents. This limit has been reached and one solution is to move from a standard SiO_2 film to a film material with a greater dielectric constant, also known as high-k dielectrics. The advantage of the high-k dielectrics is that larger capacitance values with greater film thickness can be achieved, resulting in lower gate leakage. The high-k dielectric material used in current 45nm technology is HfO deposited on a layer of SiO_2, which has a low interface state density when deposited on Si, and has a total oxide thickness of 0.8nm [10].

4) Supply voltage: If a large lateral field is applied to a scaled device punch through can occur. Therefore, the supply voltage has to be adjusted to the device dimensions to maintain an acceptable level of electric field strength. The mobility of the holes and electrons is also dependent on the vertical electrical field and follows a universal mobility curve [11]. At a low vertical electrical field the transport is limited by phonon scattering. When the field increases roughness scattering becomes more important as the carriers are pulled towards the oxide/semiconductor interface [12].

   Adjusting the supply voltage to reduce short channel effects is not a straight-forward process as a number of parameters are affected by a change in V_{dd}. The overdrive voltage is decreased ($V_{dd} - V_t$) as the threshold voltage is predicted to remain around 0.21V in future technology nodes, as shown in Table 2.1. This affects the saturation current and a compromise has to be made between short channel effects and $I_{d,sat}$.

3.3.2 How to scale

There exist a number of different scaling methodologies. Constant field scaling was first introduced by Dennard et al. [13] and is based on reducing the device dimensions without altering the electrical field. The oxide thickness, channel length, junction depth, channel width and supply voltage are then reduced by a factor k. The doping density has to increase with a factor k as well to maintain a similar electrical field. The device density can then be increased by a factor of k^2 and the power consumed by each cell is reduced by a factor of

k^2, resulting in a similar power-per-unit area. A potential detrimental effect is that the threshold voltage reduces by a factor k as well, which could potentially increase the off-state leakage current as it is inversely exponentially dependent on the threshold voltage [14].

Scaling a device while keeping the field constant is useful as the power delay product of a single device reduces. However, a reduction in power also means a reduction in supply voltage as the device dimensions decrease. Aggressively scaling devices increases the gate leakage as the oxide becomes critically thin. This has as a side effect that the threshold voltage does not scale with the device dimensions due to the leakage current. The supply voltage cannot be scaled with a factor of k as the relative difference between V_t and V_{dd} becomes greater, resulting in a reduced drive current.

When the devices are scaled while maintaining the supply voltage, the scaling methodology is known as constant voltage scaling [227]. This scaling methodology was preferred over many years as it ensures the compatibility with various technologies such as 5V TTL [15]. Scaling devices while maintaining the supply voltage results in an increased electrical field, which has a number of detrimental effects: increased leakage currents, mobility degradation and lower breakdown voltages. The power reduction is also minimal and this methodology is no longer used as, in recent years [1], the main driver has been the reduction of the supply voltage in order to mitigate the power consumption.

A more sophisticated scaling methodology is the generalised scaling, which combines elements from constant voltage and constant field scaling [13]. The main principle is to scale the physical dimensions more rapidly than the supply voltage. The shape of the two dimensional electrical field is then retained while the increased supply voltage increases the field strength.

3.3.3 Bulk silicon benchmark

CMOS technology is ever evolving and the benchmark at the start of this work was the Intel 45nm technology [10]. The 45nm technology is no longer the most aggressively scaled MOSFET device technology. The 22nm technology [2] developed during this work makes use of a FINFET structure to improve the gate control and is therefore not ideal for direct comparison. The most aggressively scaled planar MOSFET device structure in mass production is the Intel 32nm technology [51]. However, few device performance parameters could be obtained from the Intel 32nm technology, and as a result, the Intel

45nm technology is used as a benchmark. The figures of merit and critical dimensions of an nMOS device of the Intel 45nm technology are summarised in Table 3.1:

Figure of Merit	Intel 45nm (2007) [10]
Physical gate length (L_g)	35nm
Equivalent oxide thickness (EOT)	1nm
Nominal power supply voltage (V_{dd})	1V
Parasitic source/drain resistance (R_{SD})	150Ω.μm
Threshold voltage ($V_{t,sat}$)	0.3V
Subthreshold slope (SS)	110mV/dec
drain induced barrier lowering (DIBL)	130mV/V
On current (I_{on})	1360μA/μm
Off-state leakage current (I_{off})	100nA/μm

Table 3.1: Intel 45nm (2007) bulk silicon performance benchmark

The definitions of the figures of merit are defined as follows:

1) L_g: Physical gate length measured at the oxide/metal gate interface.
2) EOT: Equivalent oxide thickness is composed of the relative dielectric constant (k), the actual gate dielectric thickness (T_d) and is relative to the dielectric constant of thermally deposited SiO_2 and is given in Equation 3.22.
3) V_{dd}: The supply voltage.
4) I_{off}: Off-state leakage current, also known as sub-threshold leakage current ($I_{sd,leak}$), is defined as the residual current when $V_d = V_{dd}$ and $V_g = V_s = 0V$ measured at a temperature of 25°C.
5) $I_{d,sat}$: On-state current, also known as saturation drain current ($I_{d,sat}$), is defined as the drain current when $V_d = V_g = V_{dd}$ and $V_s = 0V$.
6) R_{SD}: Is the normalised value of the parasitic source and drain series resistance.
7) $V_{t,sat}$: The threshold voltage measured at saturation regime where the drain bias $V_d = V_{dd}$.

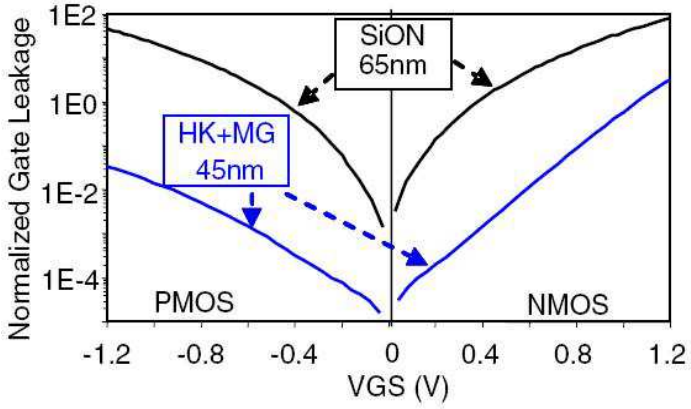


Figure 3.2: Normalised gate leakage of Intel 45nm compared to 65nm technology [16]

8) J_g: This is the gate leakage current density measured at 25°C. It is measured with $V_g = V_{dd}$ and $V_d = V_s = 0V$. The gate leakage density for the nMOS and pMOS devices of the Intel 45nm technology compared to 65nm technology is shown in Figure 3.2:

9) SS: The sub-threshold slope is the value of difference in V_g in order to reduce I_d by one order and is measured at voltages below V_t.

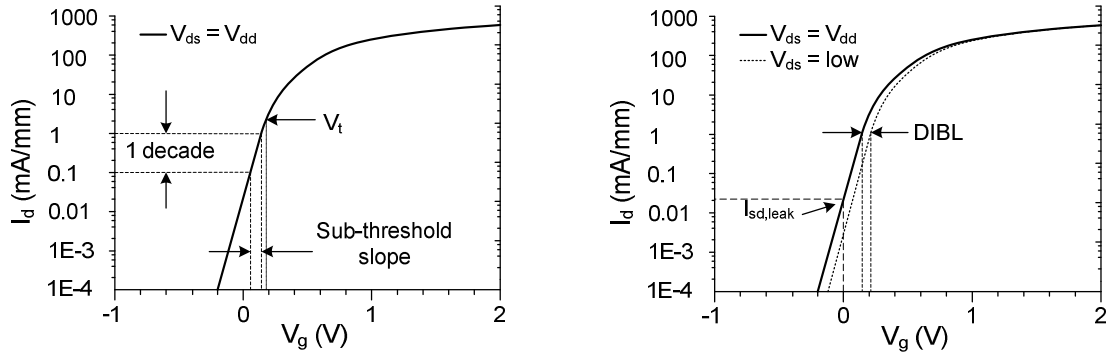
10) DIBL: drain induced barrier lowering is defined as a shift in V_t when V_d is altered. Larger V_d generally results in a reduced V_t.

11) g_m: The transconductance is the rate of change of I_d corresponding to the applied V_g with a fixed V_d as stated by Equation 3.8 [8]:

$$g_m = \frac{\delta I_d}{\delta V_g} \tag{3.8}$$

Unfortunately, the transconductance value of the Intel 45nm nMOS [10] could not be obtained and is therefore missing from the Table 3.1.

The typical I_dV_g responses together with a number of Figures of merit are illustrated in Figure 3.3.



a) V_t and Sub-threshold slope **b) DIBL**

Figure 3.3: Example of I_d/V_g plot

3.3.4 Advanced design

Another way of improving the device performance rather than straightforward scaling is the use of new materials and technologies. Different device structures such as buried channel devices, allow for further scaling of the access region as there is no p-n junction present. Also high-k dielectrics and metal gate stacks have already been introduced in current device technology [10]. This has been achieved by the optimisation of deposition tools resulting in high quality thin oxide layers, which outperform the poly-Si/SiO_2 system dramatically. The deposition of conformal oxide films has allowed an adaptation of the planar device structure into a FINFET structure for the 22nm technology [2]. Altering the channel material with high mobility and low band gap material may have the potential to improve the performance of the scaled devices and is further discussed in section 3.7.

3.4 MOS Contacts

The metal/oxide/semiconductor interface of a MOSFET device offers two main advantages over a metal/semiconductor interface; when reverse biased there is a lower leakage current and when forward biased a current barrier is maintained. These advantages help to reduce the overall power consumption of the MOSFET device and contribute to the success of MOSFET devices in digital electronics. Although this work is mainly focussed on ohmic contacts, the basic physics of an ideal MOS system are required for a full understanding of a MOSFET device and are described in this section.

3.4.1 The ideal MOS capacitor

An ideal MOS capacitor has the following characteristics:

a) The difference between the metal work function (φ_m) and the semiconductor work function (φ_s) is zero.
b) At any bias condition, the charges in the device are located in the semiconductor with an equal opposite charge at the metal/oxide interface.
c) The oxide is a perfect DC insulator without any leakage current taking place.

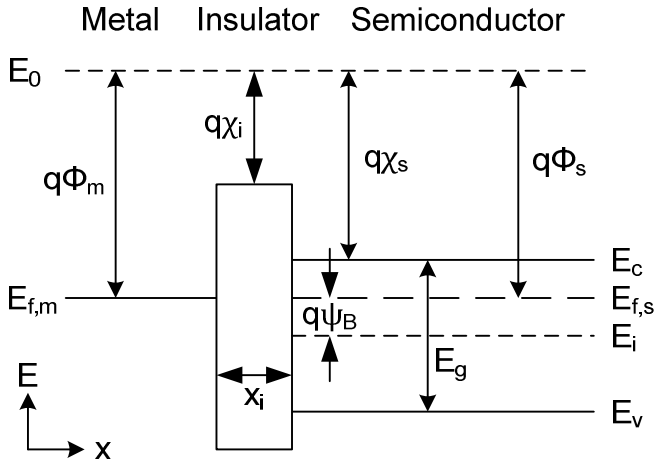
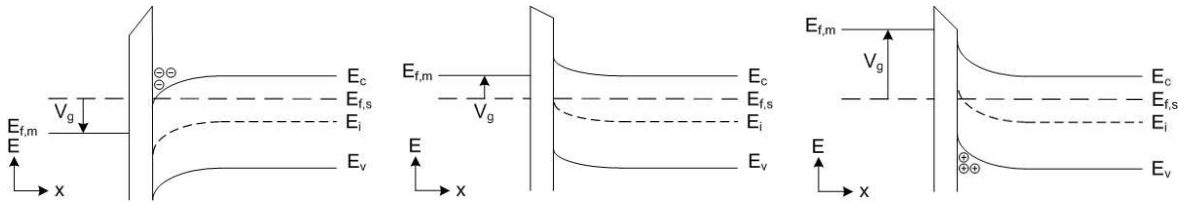


Figure 3.4: Ideal MOS capacitor band structure

The energy band diagram for an ideal MOS structure is shown in Figure 3.4. The semiconductor work function (φ_s) is equal to the metal work function (φ_m) and is determined by the band gap (E_g), the semiconductor electron affinity (χ_s) and the potential difference (ψ_b) between the Fermi level (E_f) and the intrinsic Fermi level (E_i), as shown in Equation 3.9 [8].

$$\phi_s = \chi_s + \frac{E_g}{2q} - \psi_b \qquad (3.9)$$

This work consists of MOS contacts on n-type III-V MOSFET material and therefore the behaviour of the ideal MOS contact will only be discussed for n-type semiconductor material. When applying a voltage bias to the metal (gate) of an ideal MOS contact, the carrier concentration in the semiconductor will alter as the energy bands are affected. There are three main regimes depending on the voltage bias: accumulation, depletion and inversion. The energy band diagrams are shown for each regime in Figure 3.5.



(a) Accumulation (b) Depletion (c) Inversion

Figure 3.5: Band structures of accumulation, depletion and inversion regimes.

a) Accumulation: The voltage applied to the gate is positive, resulting in the conduction band (E_c) of the semiconductor bending downwards. Once the conduction band becomes lower than the Fermi level (E_f), an accumulation of electrons at the insulator/semiconductor interface takes place. The carrier density (n) then depends on the effective density of states (N_c) and exponentially of the difference between E_f and E_c, as shown in Equation 3.10 [8].

$$n = N_c e^{\left(-\frac{E_c - E_f}{kT}\right)} \tag{3.10}$$

b) Depletion: The applied voltage to the gate is negative, resulting in the bands of the semiconductor bending upwards. The carrier concentration is then reduced to the intrinsic level when the intrinsic Fermi level becomes equal to the Fermi level. The insulator semiconductor interface is then depleted.

c) Inversion: Making the gate voltage more negative, results in an intrinsic Fermi Level with a higher energy level than the Fermi level. This causes an accumulation of holes at the insulator/semiconductor interface.

3.4.2 Capacitance Voltage characteristics

In order to get a good understanding of the capacitance voltage characteristics of the ideal MOS structure, a basic review of the parallel plate capacitor is given. The simplified model of the parallel plate capacitor forms the basis of the capacitive behaviour of an ideal MOS structure.

3.4.2.1 Parallel plate capacitor

The capacitance (C) is defined to be the amount of charge (Q) for a given potential difference (V) over two plates, as shown in Equation 3.11 [8]. Therefore, capacitance is used as a measure of the ability to store charge.

$$Q = CV \tag{3.11}$$

Using a parallel plate analogy, the C-V characteristics of an ideal MOS system can be analysed. A parallel plate model consists of two plates with a surface (A) separated by a vacuum with a distance (d) and are populated by an equal but opposite charge (Q). Gauss's law states that the electric field (ξ) is equal to the net charge enclosed in the surface (Q) divided by the permittivity of the vacuum (ε_0) and the surface area (A) as shown by Equation 3.12 [8].

$$\xi = \frac{Q}{\varepsilon_0 A} \tag{3.12}$$

The potential difference (V) over a uniform field is [8]:

$$V = \xi d \tag{3.13}$$

When combining Equation 3.11, 3.12 and 3.13, the capacitance of a parallel plate capacitor can be found and is given in Equation 3.14 [8].

$$C = \frac{\varepsilon_0 A}{d} \tag{3.14}$$

3.4.2.2 The MOS capacitor

Applying a voltage (V_g) to the gate metal of the ideal MOS contact causes the potential to drop across the oxide and the semiconductor, resulting in band bending. The semiconductor work function (φ_s) is equal to metal work function (φ_m) in an ideal MOS contact, leading to a semiconductor surface potential (ψ_s) of zero when the gate is unbiased.

$$V_g = V_o + \psi_s \tag{3.15}$$

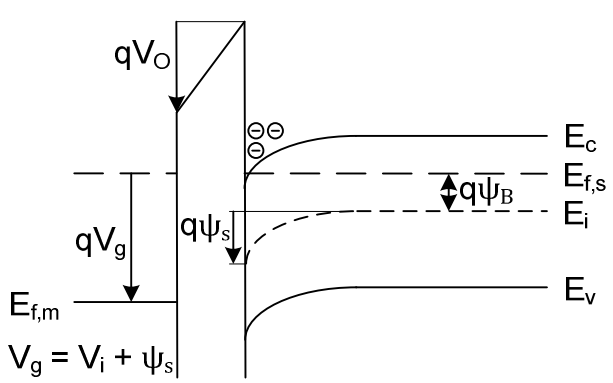
The potential across the oxide (V_o) is determined by the field (ξ_o) across the oxide and the oxide thickness (d). The field across the oxide (ξ_o) is then equal to the charge in the semiconductor (Q_s) divided by the product of the permittivity (ε_{ox}) and surface area (A) of the oxide [8].

$$V_o = \xi_o d = \frac{Q_s d}{A\varepsilon_{ox}} \tag{3.16}$$

Using Equation 3.13 the oxide capacitance (C_o) can be found, as shown in Equation 3.17 [8].

$$C_o = \frac{Q_s}{V_o} \tag{3.17}$$

A detailed band diagram of an ideal MOS contact in the accumulation regime can be seen in Figure 3.6 and shows V_o and ψ_s. The symbol ψ indicates a measure of band bending and is usually taken relative to the intrinsic Fermi level (E_i). The potential difference between E_i and E_f is expressed as ψ_B. The different regimes: accumulation, depletion and inversion can then be expressed using ψ. Also three other regimes are defined: intrinsic, flat band and strong inversion including non ideal behaviour, which will be discussed in the following section.



Accumulation: $\psi_s > 0$

Flat Band: $\psi_s = 0$

Depletion: $\psi_B < \psi_s < 0$

Intrinsic: $\psi_s = \psi_B$

Inversion: $\psi_s < \psi_B$

Figure 3.6: Detailed Accumulation regime

Accumulation

Accumulation occurs when a positive voltage is applied to the gate, which is greater than the flatband voltage V_{FB}. The ideal flatband voltage is 0V. The electrons then accumulate near the semiconductor/oxide interface due to the conduction band in the semiconductor bending downwards. Because of the proximity of the electrons close to the oxide, the capacitance reaches its maximum value (C_{max}). The maximum capacitance is approximately the same as the capacitance of the insulator, which can be modelled by using Equation 3.14 from the parallel plate capacitor.

Depletion

When the gate voltage bias is below the flat-band voltage, the conduction band bends upwards to the point where the Fermi level meets the intrinsic Fermi level. This will deplete the semiconductor/oxides interface, which will add an additional depletion capacitance in series with the capacitance of the oxide layer. The depletion region width is described as follows [8]:

$$x_d = \sqrt{\frac{2\varepsilon_s \psi_s}{q\, N_D}} \tag{3.18}$$

Where (ε_s) is the dielectric constant of the semiconductor and (ψ_s) is the semiconductor surface potential. Given the thickness and dielectric constant of the depleted region, the depletion capacitance (C_d) can be calculated [8]:

$$C_d = \frac{\varepsilon_s}{x_d} \tag{3.19}$$

The total capacitance extracted from the CV measurement given a certain voltage bias in the depletion region can then be expressed as [8]:

$$C = \frac{C_{ox} C_d}{C_{ox} + C_d} \tag{3.20}$$

Inversion

Further decreasing the gate voltage bias below the level where the intrinsic Fermi level and Fermi level meet, will allow for holes to start accumulating at the semiconductor/oxide interface. Once the surface hole concentration is greater than the bulk electron concentration, the surface will become strongly inverted and the depletion layer will no longer increase in width. The maximum depletion width ($x_{d(max)}$) for strong inversion is shown as [8]:

$$x_{d(max)} = \sqrt{\frac{4\, \varepsilon_s k\, T \ln(\frac{N_D}{n_i})}{q^2 N_D}} \tag{3.21}$$

Non ideal capacitor behaviour

So far, the ideal case of the MOS capacitor has been studied. However, in practice some non-idealities are present. The non-idealities are mainly due to work function difference and oxide charges. The oxide used on the most common Si MOSFET devices is SiO_2 and has properties, which closely approximate the ideal MOS capacitor structure. The physical mechanisms causing the non-ideal behaviour will therefore be discussed using a SiO_2/Si interface in this section. There are four main non-ideal oxide charges, which will be briefly discussed. Their relative position along the oxide/semiconductor interface is illustrated in Figure 3.7.

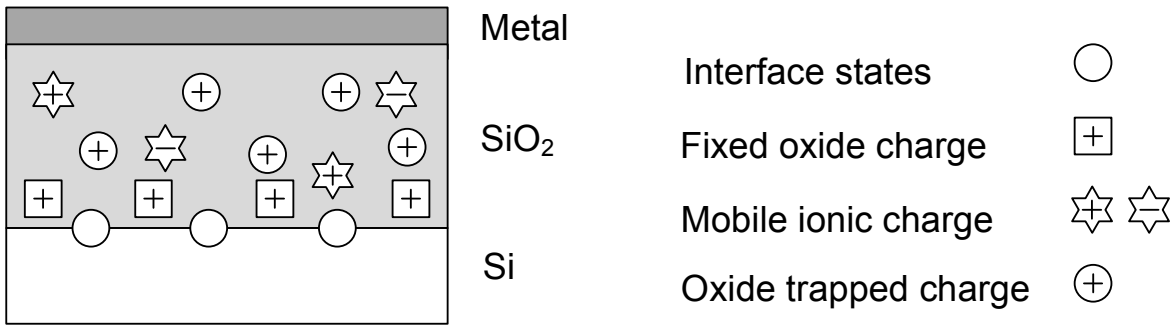


Figure 3.7: Si/SiO_2 MOS Charges [228]

Interface states

Interface traps (Q_{it}) are caused by a sudden termination of the semiconductor crystal lattice at the oxide/semiconductor interface. These sudden terminations are generally induced by an excess of Si, O or impurities. Due to the location of traps, interface traps have energy states in the Si bandgap. When applying a gate voltage the energy states can cross the Fermi level, which results in an exchange of charge with the semiconductor. The exchange of charge can be modelled by including the interface trap capacitance (C_{it}) and resistance (R_{it}) into the simple equivalent circuit diagram of the ideal system, as shown in Figure 3.8.

The interface trap lifetime (τ_{it}) can then be associated with the time constant of C_{it} and R_{it}. The interface traps are then able to respond to low frequency AC signals. This property is used to measure the interface trap (D_{it}) density using CV measurements (chapter 5.5).

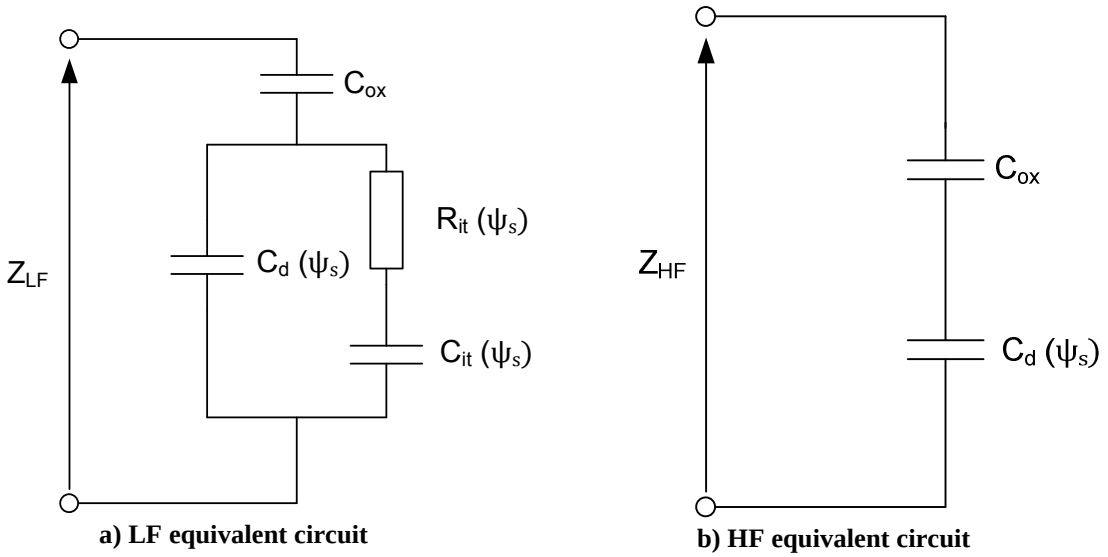


Figure 3.8: Equivalent circuit of oxide/semiconductor interface charge

Oxide charge

Oxide charge is a general term, which includes all charges and traps that are situated in the bulk of the oxide. The different charges involved in a Si/SiO_2 system are well understood and can be used as an example. There are three main types of oxide charge: fixed oxide charge, mobile ionic charge and trapped oxide charge. The origin of the charge together with their corresponding effects on CV-measurements, are discussed in the following section.

Fixed oxide charge (Q_f)

Historically the charges have been considered to be located within a region of 3nm thick near the semiconductor interface in a Si/SiO_2 system. However, modern MOSFET device technology [17] features SiO_2 dielectrics with a thickness below 2nm rendering the previous definition meaningless. The fixed charge is generally positive in a Si/SiO_2 system [8] and is unaffected by standard operating voltages and surface potentials. The polarity of the fixed charge varies with different oxides [18]. The fixed charge causes a voltage shift (V_f) when measuring high frequency CV measurements, as the interface trap lifetime (τ_{it}) prevents the traps from responding to the high frequency signal, as shown in Figure 3.9. The magnitude of the voltage shift depends on the fixed oxide charge and the oxide capacitance:

$$\Delta V_f = \frac{Q_f}{C_{ox}} \tag{3.22}$$

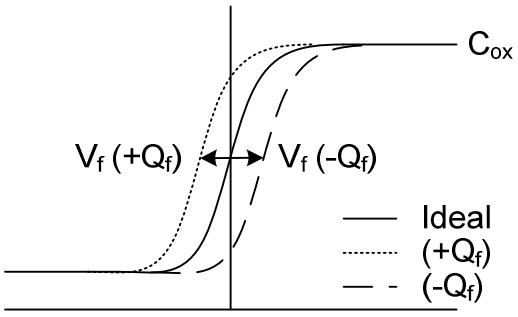


Figure 3.9: Effect of Q_f on V_t shift on C-V plot

Mobile ionic charge (Q_m)

The mobile ionic charges, most commonly Na^+ in SiO_2, are mobile under the influence of an electric field and can therefore move in the gate dielectric, resulting in fluctuations in the threshold voltage V_t [8].

Oxide trapped charge (Q_{ot})

The charges are caused by defects or impurities forming traps and are spread over the entire area of the gate dielectric. These traps are usually uncharged until the bias voltage is altered, resulting in threshold voltage shifts, which can create a hysteresis.

High-k dielectrics

As previously mentioned, CMOS performance improves when scaling the physical dimensions of MOSFET devices, which resulted in thinner gate dielectric layers. However, there is a crossover point where the advantages of a scaled gate dielectric are outweighed by an increase in leakage current. Therefore, alternative gate dielectric materials with a larger dielectric constant than SiO_2, known as high-k dielectrics, have been researched and introduced on large scale production [17]. From the parallel plate capacitor, we know that an increase in permittivity also allows for an equal increase in layer thickness while maintaining the same capacitance value. As a result, the increased layer thickness reduces leakage current, by reducing the probability of electrons tunnelling through the oxide, while maintaining long channel behaviour and charge control. The thickness of the high-k dielectric layer (d) is usually compared to the thickness of SiO_2 for a given capacitance and is known as the equivalent oxide thickness (EOT), expressed as:

$$\mathrm{EOT} = \mathrm{d}\ \frac{3.9}{\mathrm{k}} \tag{3.23}$$

where k is the relative permittivity of the dielectric [8]. A suitable high-k dielectric needs to have basic properties such as thermal stability, chemical stability and compositional stability. Also more complex properties are required such as low interface state density, low oxide trap density and reduced channel mobility degradation in order to approach the ideal MOS capacitor model. Various suitable high k- dielectrics on Si are shown in Figure 3.10 [19]. A minimum acceptable band offset, indicated by the dashed line in Figure 3.11, is required to keep the leakage current to a minimum when using a 1V supply bias: this excludes oxides such as Ta_2O_5 as a suitable dielectric on Si. A high band offset will also reduce the detrimental effects of hot electrons. The high electric fields ($>10^4$V/cm) present in scaled MOSFETs cause an increase in the energy of electrons. Non-equilibrium transport takes place as the electrons have greater energy than the thermal energy of the lattice. Some electrons are then able to leave the silicon and tunnel into the gate oxide if the kinetic energy band of the oxide conduction band is overcome (SiO_2 ~ 3.2eV). This gives rise to oxide charging, which can accumulate with time and degrade the device performance by increasing the threshold voltage. This short channel effect can adversely

affect the gate control on the drain current and can be mitigated by opting for higher band offset oxides such as SiO_2 and Al_2O_3. However, this work focuses on III-V materials and the suitable dielectrics are shown in Figure 3.11. Three different dielectric materials were used in this work: Ga_2O_3, GaGdO (GGO) and Al_2O_3. The choice of gate dielectric is determined by quality of the interface when deposited on the III-V material.

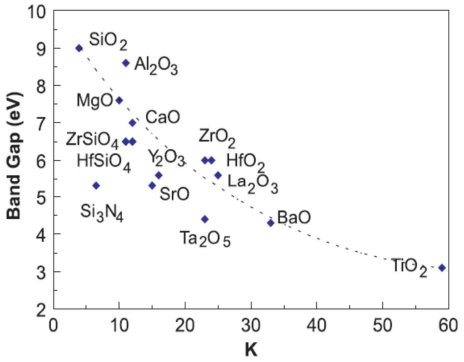


Figure 3.10: Band offsets of various high-k dielectrics [20]

Figure 3.11: Band offsets of various high-k dielectrics compatible with GaAs

Metal gates

The gate work function becomes increasingly important as devices scale, as the work function has a larger influence on V_t than substrate doping, oxide charge and oxide thickness on scaled MOSFET devices. The V_t has to be tightly controlled as devices are further optimised for low power consumption and therefore have smaller supply voltages. To obtain the correct V_t, the gate work function should be close to the conduction band edge in planar n-type MOSFET devices ($\Phi_m \approx$ 5.0eV to 5.2eV). The work function of various metals is illustrated in Figure 3.12.

The work function can be tuned by using alloys of metals with different work functions. The ease of work function tuning, patterning and resistance to boron penetration, have lead to the introduction of metal gates on large production volume devices [17].

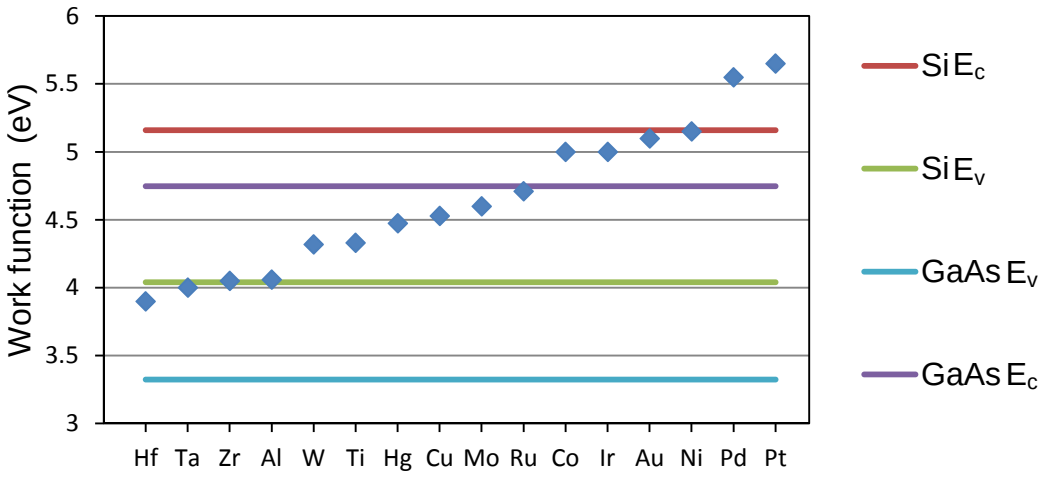


Figure 3.12: Work function of various metals under vacuum [229]

3.5 Channel Engineering

The introduction of new technologies such as high-k dielectrics, strain [17] and advanced architectures [2] has been necessary to keep scaling the size of the devices. Stress- or strain-induced improvement of the device performance is based on enhancing the mobility in the channel region and therefore improving the current density in the channel and the operation speed of the device. However, mobility enhancement by strain is limited [21]. Further improvement in mobility will then require materials with superior transport properties over strained Si, such as various III-V compositions, Ge and SiGe. This section will describe the basic transport concepts of velocity saturation and mobility in more detail and then compare the potential performance improvements of III-V channel materials.

3.5.1 Transport basics

Since III-V materials possess superior electron transport properties to both Si and strained-Si, they have been recognised as alternative channel materials. The transport properties of these materials can be simply compared by examining bulk low field mobility, which is the proportionality constant between carrier velocity (υ) and field strength (ξ).

$$\upsilon = \mu\xi \tag{3.24}$$

Mobility in non-polar semiconductors such as Si and Ge is determined by scattering from acoustic phonons and ionised impurities. On the contrary, optical phonon scattering is more significant in polar III-V materials [8]. The room temperature electron and hole mobility of alternative channel materials, compared to Si, is illustrated in Table 3.2 [8].

	Ge	Si	GaAs	InAs	InSb	InP
Electron mobility (cm^2/Vs)	3900	1500	8500	23000	80000	4600
Hole mobility (cm^2/Vs)	1900	450	400	100	1250	150

Table 3.2: Low field mobility of alternative channel materials (cm^2/Vs)

As shown in Table 3.2, the electron mobility of GaAs reaches a value of more than five times that of silicon and over double that of Ge. As drive current is directly proportional to mobility, in the case of the long channel model (Equation 3.2), an ideal GaAs MOSFET would then reach a fivefold increase in $I_{d,sat}$ over a Si MOSFET. Alternative materials, such as InAs and InSb, feature elevated values for electron mobility and could potentially provide large gains in drive current. Ternary materials, such as $In_xGa_{1-x}As$, can also be used to increase the mobility while the lattice structure can be determined by the In concentration. However, the lattice structure of these materials makes integration on a Si platform complex. The electron mobility value of a weakly doped $In_xGa_{1-x}As$ compound can be calculated using following equation:

$$\mu_n = (40 - 80.7x + 49.2x^2)(10^3)(cm^2/Vs), \quad (3.25)$$

where x represents the indium concentration [22].

However, when due to scaling the long channel operation is no longer valid, the semiconductor material in the channel is then subjected to high electric fields. When high fields are applied, usually in the order of 10-100kV/cm, the linear relationship between the average carrier velocity and the applied field is no longer valid, as shown in Figure 3.14. The velocity of the carriers then tends to saturate and both saturation field and the saturation velocity of a semiconductor material are typically dependent on impurities, crystal defects and temperature [230].

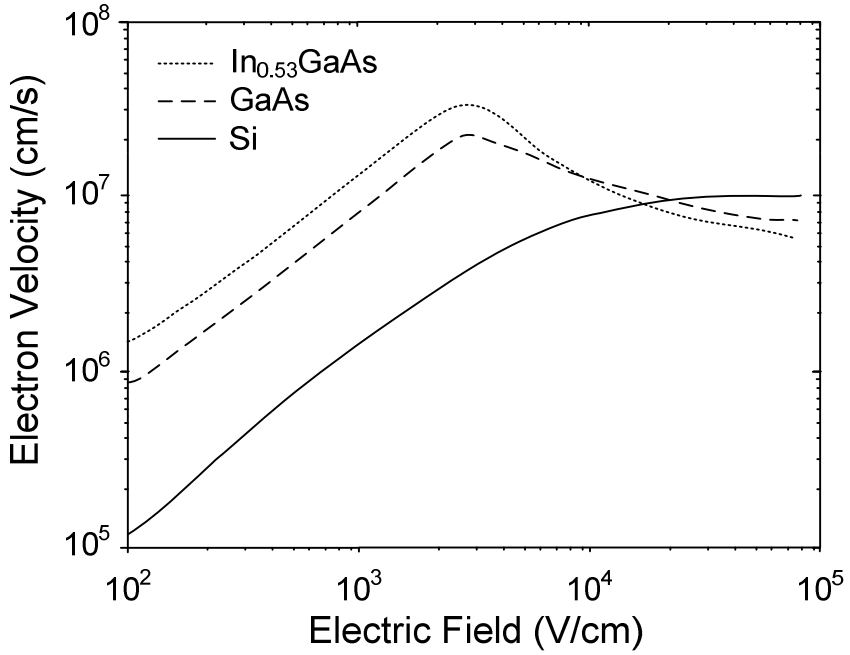
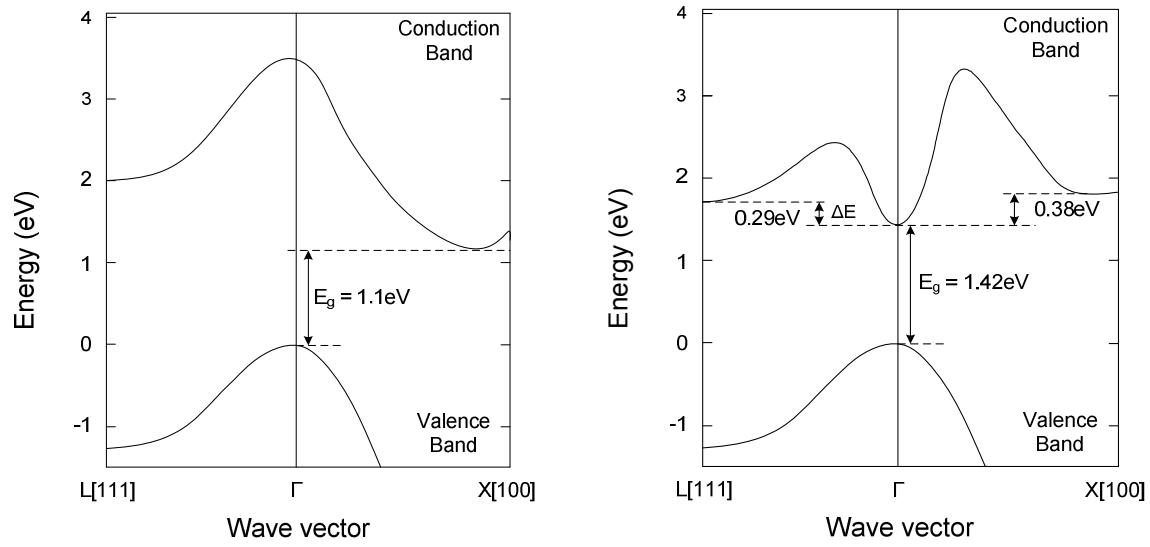


Figure 3.13: Velocity field characteristics of Si and GaAs

The differences between the velocity-field characteristics of polar III-V semiconductors and covalent group IV semiconductors can be illustrated by the differences in the band structure of the respective materials. The general principles of velocity saturation are demonstrated with Si and GaAs as these are the most widely used group IV and III-V semiconductors. The corresponding simplified band diagrams are shown in Figure 3.14 [23].



a) Si **b) GaAs**

Figure 3.14: Energy band structure

In multi-valley semiconductors such as InGaAs and GaAs, the majority of conduction band electrons remain in the high mobility Γ valley at low fields [231, 22]. Increasing the electric field causes the carriers to transfer to the higher energy (+0.29eV), lower mobility L valley. These higher valleys feature relatively higher effective masses resulting in reduced drift velocities. The ratio of carriers occupying the L valley is then increased rapidly at the intermediate field strength, which leads to a peak in velocity. Finally, at higher fields, the majority of carriers are present in the L valley and are subject to increased scattering mechanisms, resulting in velocity saturation.

Velocity saturation, as opposed to mobility, determines the drive current ($I_{d,sat}$), in MOSFET devices with short channels (Equation 3.3). In addition, Figure 3.13 suggests that since the saturation velocity of III-V channels is similar to that of Si, there will be no drive current advantage of GaAs compared to standard Si technology in short channel devices. Strained Si features increased velocity saturation values compared to GaAs and Si and improvements in mobility and drive current have been demonstrated on nMOS devices [31, 32, 33].

However, III-V channels can still offer an advantage in drive current over Si technology as the bulk transport is only a first order approximation of device performance. Other factors such as, 2 dimensional carrier confinement, transverse electric fields and non-equilibrium high field transport such as velocity overshoot and hot electrons can play a role in the physical processes of carrier transport in practical MOSFET devices.

3.5.1.1 2DEG

When an nMOS transistor is operating in inversion, the electrons are confined close to the gate oxide/semiconductor interface. This is due to the gate-induced band bending at the gate oxide/semiconductor interface, which causes a potential well. The potential well confines inversion electrons parallel to the interface, also known as quantum confinement, which allows them to move free in either direction parallel to the interface, but the motion of the electrons perpendicular to the interface is restricted. This sheet of electrons is also known as a Two – Dimensional Electron Gas (2DEG).

The electrons in the 2DEG are then separated from the donor impurities. The mobility is then greatly increased as there is a reduction of ionised impurity scattering [232]. Separating the channel from the ionised donors can then be used to increase mobility and the drive current and is most commonly used in HEMT devices.

The carrier distribution in the channel, caused by the potential well, is dependent on the density of states and effective mass. The electron distribution at the oxide/semiconductor interface, under forward bias, is given for Si and GaAs in Figure 3.15.

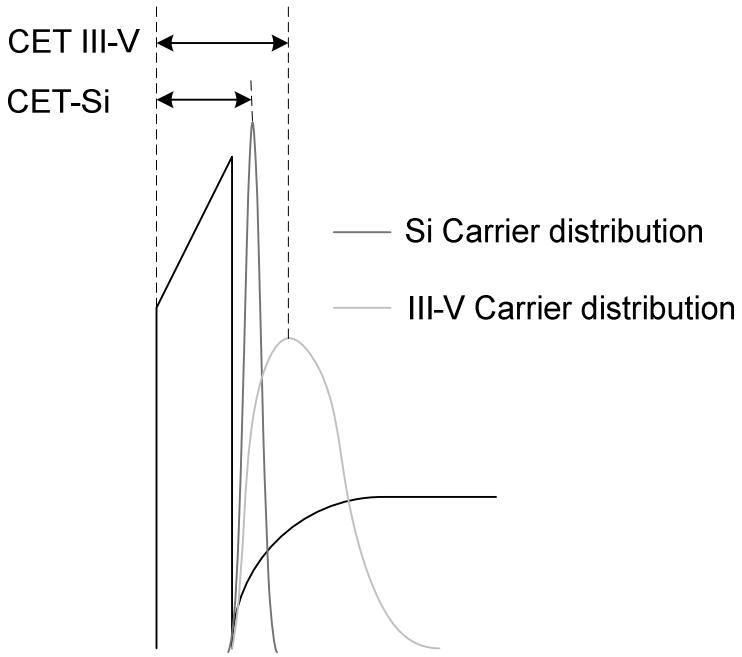


Figure 3.15: Impact of density of states on electron distribution at the oxide/semiconductor interface for Si and GaAs

The charge density can be calculated from the oxide capacitance and the drive voltage of the gate. The distance between the peak of the charge distribution and the oxide/semiconductor should be taken into account in order to calculate the charge density. This distance adds to the total thickness of the gate capacitance also known as the Capacitive Effective Thickness (CET) and is larger in III-V materials compared to Si. This is due to the lower density of states of III-V materials, which limits the spatial charge concentration and forces the electrons to accumulate in a wider distribution. As a consequence, the larger CET value in III-V materials leads to a reduced gate capacitance in surface channel devices. However, a larger gate voltage will then be required, compared to Si, which results in a reduced transconductance.

The reduction in current from the density of states is offset by the increase in velocity, with theoretical drive current improvements of 200% over Si [25].

3.5.1.2 Effective transverse electrical field vs. mobility

The elastic properties between the semiconductor and oxide are often not identical and therefore the phonon deformation potentials are modified [233]. This leads to an increase of phonon scattering and results in a reduction of the inversion mobility compared to the bulk Si value. The relationship between inversion mobility and transverse electric field has been investigated by Takagi et al. [11]. The research has shown that the mobility can be represented by a universal curve, which is unaffected by the doping density in the semiconductor material. At fields below 0.5MV/cm, the scattering mechanisms are mainly determined by acoustic phonon scattering and to a lesser extent to Coulomb scattering.

Coulomb scattering takes place at a lower field where the inversion charge density is low and collisions with impurities, such as doping are more likely to take place. At higher fields, the scattering mechanisms are a combination of acoustic phonon scattering and interface roughness scattering. At any inversion density or effective transverse electric field, the mobility consists of a contribution of all three main scattering mechanisms, as shown in Figure 3.16. The universal curve of mobility versus effective transverse electric field can then be used as a benchmark.

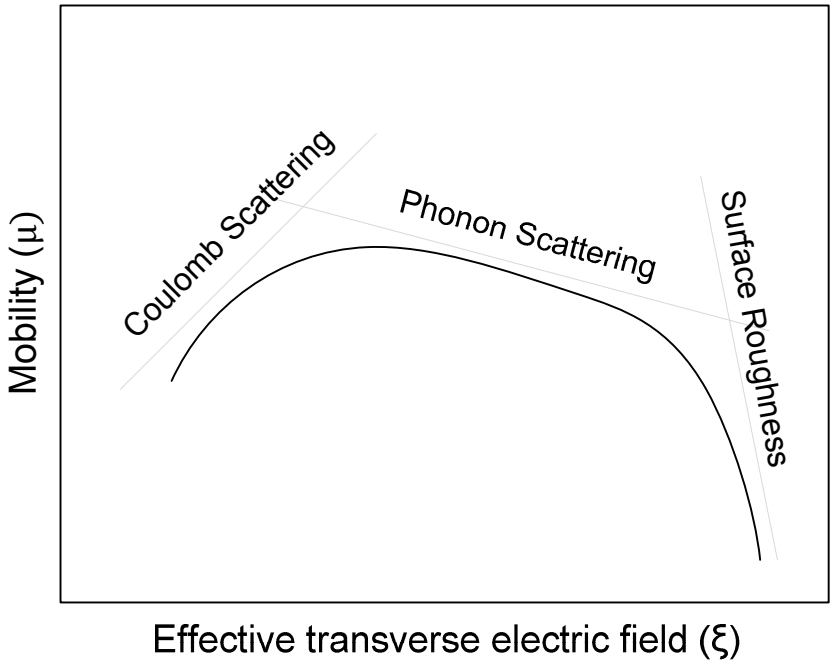


Figure 3.16: Dependence of mobility on transverse electric fields

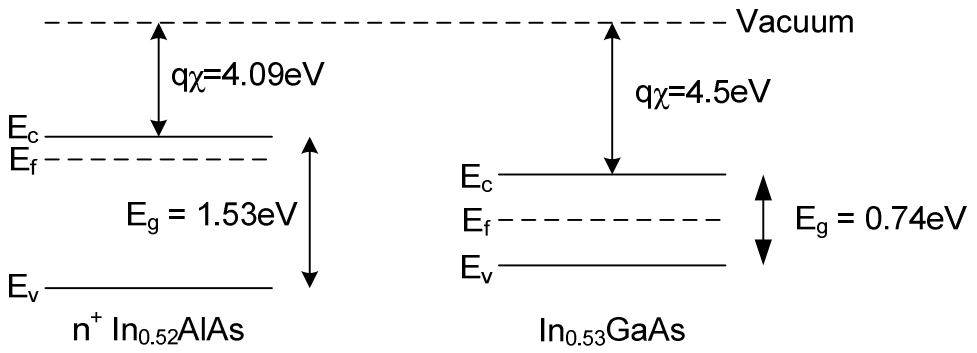
3.5.1.3 Velocity overshoot

As previously stated, optical phonon scattering is more significant in polar III-V materials [8]. However, the optical phonon scattering can be reduced by shrinking the gate length. This allows the electron to travel from source to drain in a time smaller than the time required to emit an optical phonon. This is also known as velocity overshoot and the electron velocity can then surpass the saturation velocity. The velocity overshoot was demonstrated experimentally on a Si MOSFET device, which was cooled down to 4.2K [24]. The average carrier velocity in this work was extracted from the intrinsic conductance and was found to be over 1.8 times higher than the equilibrium velocity saturation value even though the devices displayed short channel effects. Carrier velocity overshoot was also demonstrated at room temperature in devices with gate lengths around 100nm, resulting in a 20% to 35% improvement over the saturation velocity [25, 26, 27]. Device modelling, using Monte Carlo Simulations, confirmed the experimental findings, indicating that the velocity overshoot has beneficial effects on $I_{d,sat}$ and CMOS switching time [28].

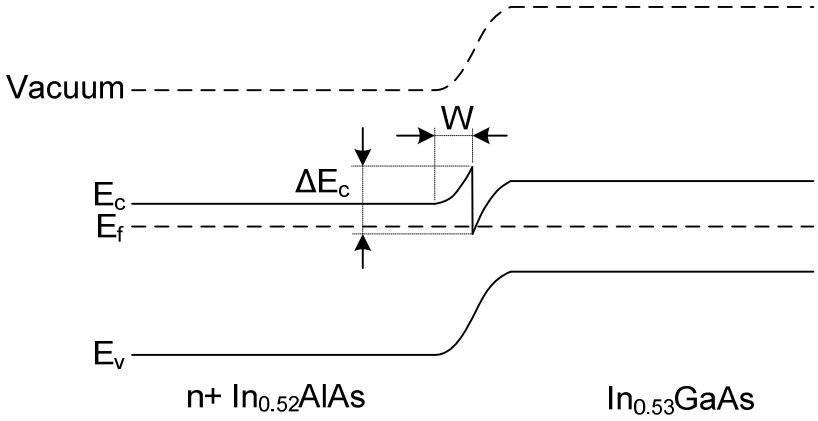
3.5.1.4 III-V heterostructure

Figure 3.14 shows that the saturation velocity of Si is greater than GaAs at high fields. This is a potential disadvantage for scaled bulk GaAs MOSFET devices. Deposition technologies such as molecular beam epitaxy (MBE) and chemical vapour deposition

(CVD) allow for well defined interfaces between different III-V material layers. This can be used to create heterostructure devices containing heterojunctions to improve the transport properties.



(a) n+ $In_{0.52}AlAs$ and $In_{0.53}GaAs$ before contact



(b) n+ $In_{0.52}AlAs/In_{0.53}GaAs$ heterojunction

Figure 3.17: Energy band diagram of a heterojunction formation

The standard simplified energy band diagram of a heterostructure is given in Figure 3.17a, where E_c is the conduction band, E_f the Fermi level, E_v the valence band, χ the electron affinity and E_g the bandgap or forbidden energy. A heterojunction is formed at the interface of a narrow bandgap semiconductor when it is brought into contact with a wider bandgap semiconductor, as shown in Figure 3.17b. As the layers are brought together, the Fermi levels align. Consequently the higher energy electrons diffuse into the undoped lower bandgap material. This causes a depletion region, with a width (W), at the wider bandgap material at the interface. The electrons accumulated in the narrow bandgap material eventually reach equilibrium and have a net negative charge. The electric field

across the heterojunction then causes band bending to occur with a magnitude of ΔE_c, forming a quasi-triangular potential well [235]. The quantum confinement creates a 2DEG sheet of electrons, which are spatially separated from the donors, as previously discussed in section 3.5.1.1, resulting in increased mobility.

High indium concentration materials such as $In_{0.53}GaAs$, InAs and InSb [22] feature a narrow (<1 eV) bandgap and also offer an increase in mobility, as shown in Table 3.2, due to reduced inter-valley scattering [38]. The indium concentration in the channel, in this work, varies from low $In_{0.3}GaAs$ to $In_{0.75}GaAs$ in order to obtain higher mobility values compared to Si and strained Si.

However, to form a heterojunction, two materials have to be grown on top of each other with minimal lattice mismatch in order not to create dislocations in the material. The dislocations will then cause defect scattering [41], reducing the mobility of the material. An overview of lattice constants and corresponding bandgap for some III-V materials and group IV materials is given in Figure 3.18.

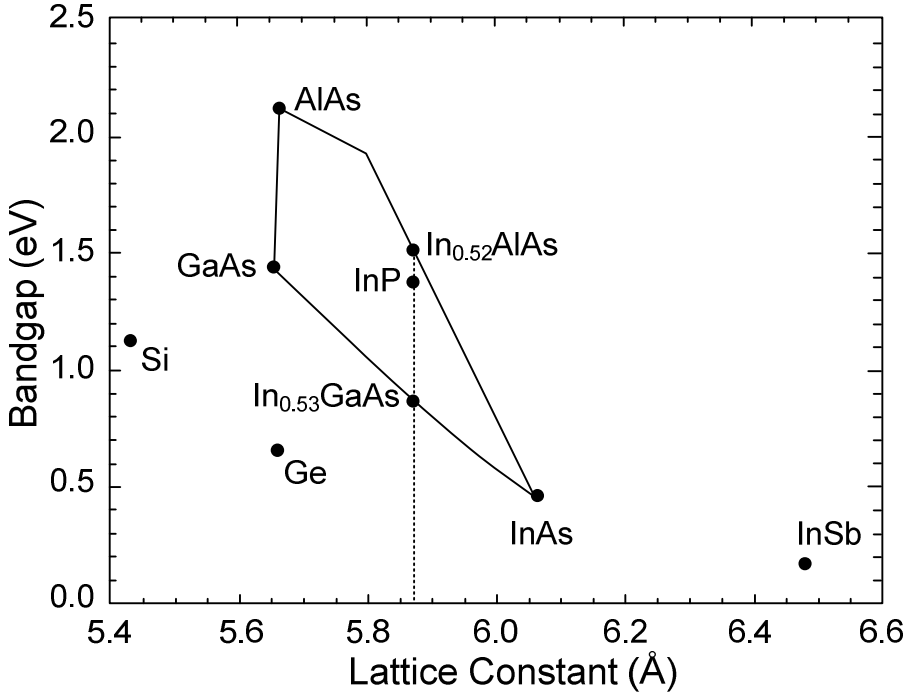


Figure 3.18: Lattice constants of common III-V and IV materials including the band gap

As shown in Figure 3.18, the arsenide materials system is one of the most versatile covering lattice constants of $In_xGa_{1-x}As$ from 0.567nm (x = 0%) to 0.608nm (x = 100%). III-V compounds with similar lattice constants are then needed to create a dislocation free

channel. A slight lattice mismatch between GaAs, AlGaAs, InAlAs and InGaAs can be accommodated when the layers are below a critical layer thickness [36, 37]. Therefore, the heterostructures formed in this work feature different wide bandgap materials and are grown on different substrates. The low indium concentration channel material (In = 30%) uses $Al_xGa_{1-x}As$ as a wide bandgap material and is grown on a GaAs substrate. The high indium concentration material (In >50%) uses $In_xAl_{1-x}As$ as a wide bandgap material and is grown on InP. The lattice constant of InP is matched to the lattice constant of $In_{0.53}GaAs$ and $In_{0.52}AlAs$ and will then form a dislocation free heterostructure, as shown in Figure 3.17. However, the lattice constant of InP is significantly larger than the lattice constant of Si. This can cause problems when integrating III-V MOSFET on a Si platform. This has been mitigated by growing InP in a trench on top of a Ge buffer layer, resulting in a defect free top InP layer [234]. Other III-V compounds, for example, InAs and InSb also offer high mobility values, but integration issues with Si processing such as lattice mismatch and contamination prevent these materials to be used on a 200mm Si pilot line. Therefore, only GaAs and InGaAs based MOSFET devices are studied in this work.

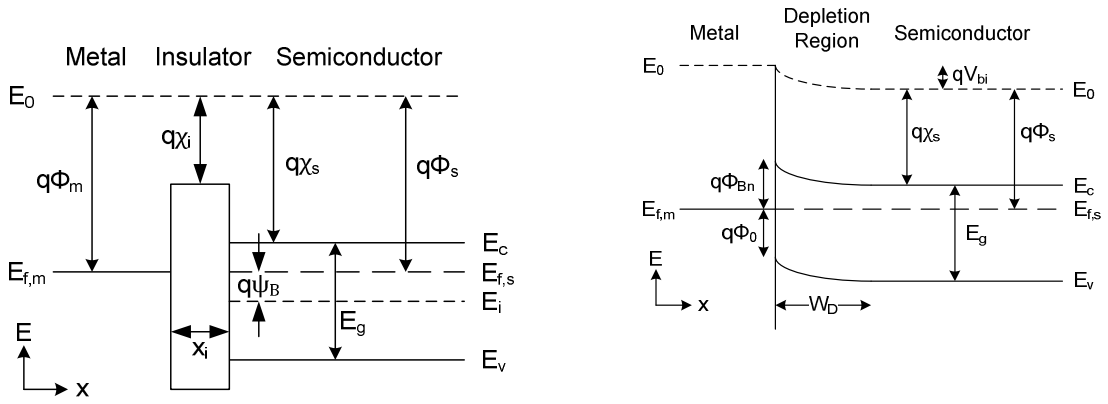
3.6 Metal- Semiconductor Contacts

3.6.1 Introduction

As this work focuses on forming ohmic contacts on III-V MOSFET material, the basic theory of metal-semiconductor contacts is explained in more detail. Both the ideal and practical energy band diagram of a metal/semiconductor interface will be discussed, leading to the conduction properties of the metal/semiconductor contacts, which are determined by the current transport processes.

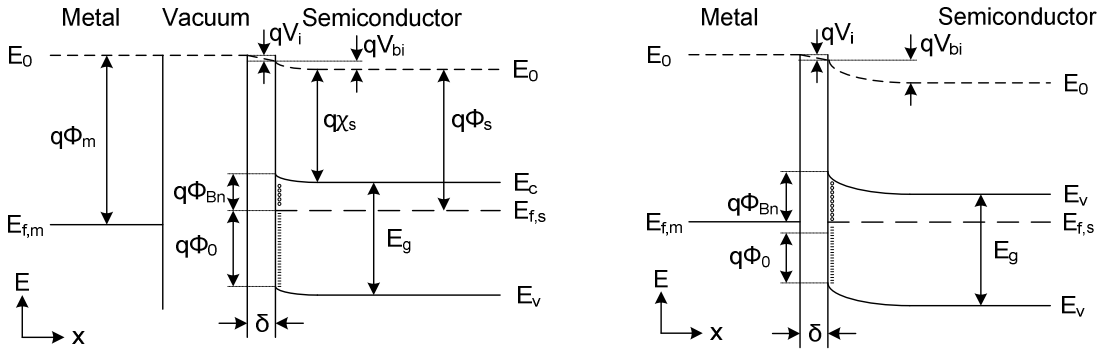
3.6.2 Energy band diagrams

The ideal energy band diagram for a metal semiconductor interface has two main limiting cases. Firstly, the ideal contact does not take the surface states into account between a metal and semiconductor. Secondly, when a practical metal/semiconductor interface is made, a thin interfacial layer is present on the semiconductor surface. The interfacial layer is assumed to have a theoretical infinite amount of surface states in order to simplify the model. The energy band diagram for each case is given in Figure 3.19 and 3.20, where (a) is before and (b) is after contact under equilibrium.



a) Before contact **b) After contact and under thermal equilibrium**

Figure 3.19: Energy band diagram of an ideal metal/semiconductor contact



a) Before contact **b) After contact and under thermal equilibrium**

Figure 3.20: Energy band diagram of a metal/semiconductor contact with a thin interfacial layer and an infinitely large density of states

The energy band diagram of n-type semiconductor without an interfacial surface layer and without surface states is shown in Figure 3.19. When a metal is placed in contact with a semiconductor, the Fermi levels align and the conduction (E_c) and valence (E_v) energy bands bend in order to reach thermal equilibrium. The process is similar to the formation of a heterojunction, where electrons diffuse from the (high band gap) semiconductor material to the metal, which has low or no band gap. An electric field is then generated as donors are exposed in the semiconductor, limiting the diffusion process and resulting in a thermal equilibrium. The energy band diagram of an n-type semiconductor with a thin surface layer is shown in Figure 3.20. The thin layer could potentially be a native oxide or processing residue, which contains a large density of surface states (D_{it}), many with energies distributed within the bandgap of the semiconductor. The physics of the junction are then

no longer governed by the properties of the metal and semiconductor material. Instead the physics of the junction are governed by the properties of the semiconductor surface [40]. In the case that the semiconductor surface is electrically neutral, it is possible to define a neutral level Φ_0, which represents the position of the Fermi level. Depending on the position of the surface states relative to $\Phi_{0,}$ the semiconductor surface will either be positive or negatively charged. When the Fermi Level differs from the neutral level Φ_0 a net charge (Q_{it}) will be present at the surface.

$$Q_{it} = q\, D_{it}(E_f - E_0) = q\, D_{it}\left(E_g - \Phi_{Bn} - \Phi_0\right) \tag{3.30}$$

The charge at the surface causes an electric field in the semiconductor, which leads to energy band bending. For an n-type semiconductor, a negative charge will make the energy band bend upwards, towards the surface, and a positive charge will make the energy band bend downwards, towards the surface. When bringing the metal in contact with the semiconductor, the charge at the surface is then a combination of the charge of the depletion region and the charge caused by the surface states:

$$Q_s = Q_{it} + Q_D = Q_{it} + (q\, N_D W_D) \tag{3.31}$$

where

$$W_D = \sqrt{\frac{2\varepsilon_{r,s}\varepsilon_0 V_{bi}}{q\, N_D}} \tag{3.32}$$

The height of the potential barrier (Φ_{Bn}) is in the ideal case the difference between the metal work function (Φ_m) and the semiconductor affinity (χ). A thin insulator at the metal/semiconductor interface causes an additional voltage drop (V_i) over the metal/semiconductor interface, which is determined by the charge (Q_s) at the surface and the capacitance at the interface layer (C_i).

$$\Phi_{Bn} = \Phi_m - \chi - V_i = \Phi_m - \chi - \left(\frac{Q_s}{C_i}\right) \tag{3.33}$$

Taking into account the density of states at the surface, the equation for the potential barrier height (Φ_{Bn}) then becomes:

$$\Phi_{Bn} = \Phi_m - \chi - \left(\frac{1}{C_i}\right)\left(Q_D + qD_{it}\left(E_g - \Phi_{Bn} - \Phi_0\right)\right) \tag{3.34}$$

Extracting for (Φ_{Bn}) gives:

$$\Phi_{Bn} = \gamma\,(\Phi_m - \chi) + (1 - \gamma)\left(E_g - \Phi_0\right) - \frac{\gamma Q_D}{C_i} \tag{3.35}$$

with

$$\gamma = \frac{1}{1+\frac{q D_{it}}{C_i}} = \frac{1}{1+\frac{q\,D_{it}\delta}{\varepsilon_{r,s}\varepsilon_0}} \tag{3.36}$$

For an infinitely large density of states (D_{it}), the potential barrier height is only dependent on the band gap of the semiconductor and the neutral level of the semiconductor. Fermi level pinning takes place at the interface making the potential barrier height independent from the metal work function. The infinitely large D_{it} then causes the potential barrier height to pin at 2/3 E_g, which is also known as Bardeen's limit [203]. The formation of surface states is dependent on the bonding type of the semiconductor material [40]. Covalent semiconductors such as Si, Ge and diamond, give rise to a large density of states at the surface due to the unsaturated bonds at the surface. For ionic semiconductors, the potential barrier height depends on the metal work function and a correlation between the interface behaviour and electronegativity exists [8]. The interface behaviour can be quantified by the dependence of potential barrier height to the electronegativity of the applied metal:

$$S \equiv \frac{d\Phi_{Bn}}{d\chi_m} \tag{3.37}$$

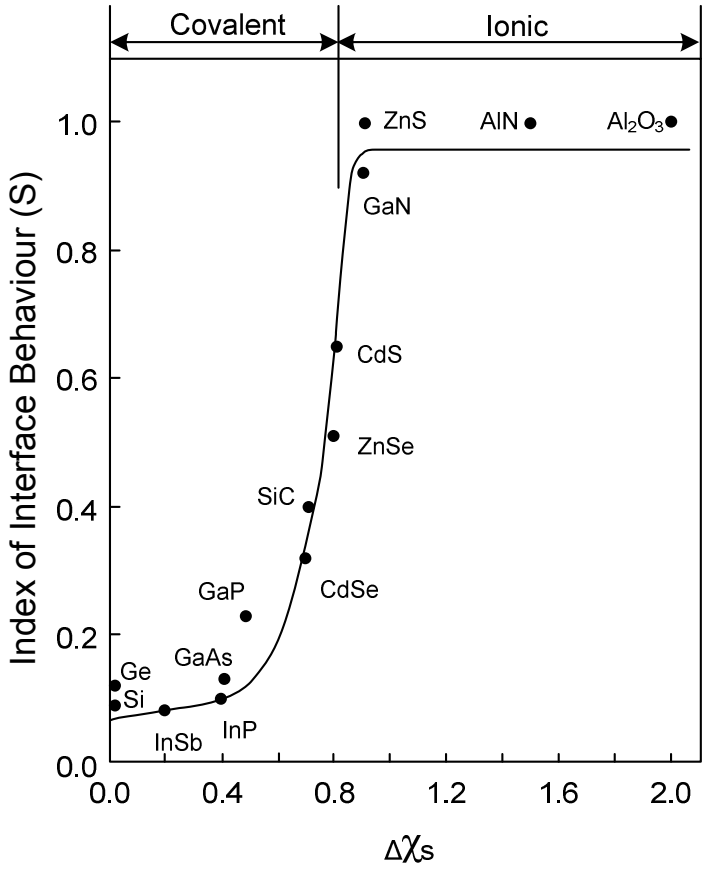


Figure 3.21: The index of interface behaviour (S) as a function of the electronegativity difference of various semiconductor materials [236].

The electronegativity (χ_m) of the metal is defined as the capability of an atom to attract an electron to itself. The index of interface behaviour (S), is plotted in Figure 3.21 as a function of the electronegativity difference of various semiconductor materials. The semiconductor material used in this work: GaAs, InGaAs, InAs, AlGaAs and InAlAs have low barrier heights, resulting in a low index of interface behaviour. As a consequence, the potential barrier height is highly likely to suffer from Fermi level pinning.

3.6.3 Current transport mechanisms

The current transport across a metal/semiconductor interface is mainly due to majority carriers. There are four basic transport mechanisms under forward bias for a metal to n-type semiconductor contact illustrated in Figure 3.22. The mechanisms remain the same under forward or reverse bias. The basic transport mechanisms are [40]:

1) Emission of electrons from the semiconductor over the top of the barrier into the metal.

2) Quantum mechanical tunnelling of electrons from the semiconductor through the barrier into the metal.

3) Recombination of electrons and holes in the depletion region.

4) Recombination of electrons and holes in the neutral region ("hole injection").

The four transport mechanisms will be discussed in the following sections.

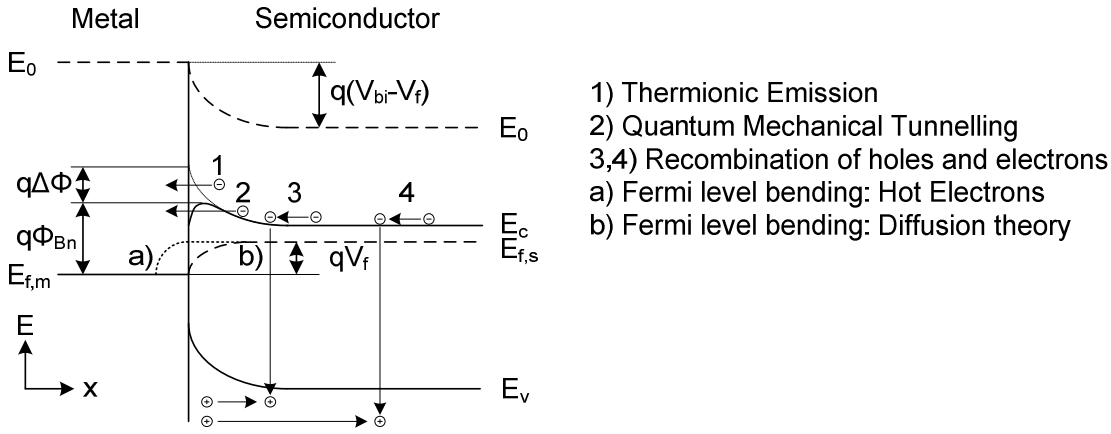


Figure 3.22: Energy band diagram displaying the four basic transport processes in a metal/ n-type semiconductor contact under forward bias.

3.6.3.1 Emission over the barrier

The emission of electrons over the top of the potential barrier can be described by two mechanisms: thermionic emission (TE) and diffusion. The mechanisms are dependent on the properties of the semiconductor material, where the semiconductor material can be described by either thermionic emission theory or diffusion theory. In practice, the transport process will be a combination of both, which has led to the development of a combined thermionic emission/diffusion theory. The assumptions made and the corresponding current density equations for are given in the following subsections.

The thermionic emission theory

The thermionic emission theory is based on a heat-induced flow of charge carriers from a surface over a potential energy barrier and is derived from the following assumptions [8, 41]:

1) The potential barrier height ($q\Phi_{Bn}$) is greater than the thermal energy of the electrons determined by kT, where k is the Boltzmann factor and T is the absolute temperature.

2) Thermal equilibrium is achieved at the plane that determines emission.

3) The thermal equilibrium is not affected by the existence of a current flow. The two current fluxes, from the semiconductor to the metal and vice versa, can be superimposed.

4) The actual transfer of electrons across the interface of the metal and the semiconductor is the current limiting factor.

5) The electron mean free path should be bigger than the width of the region over, which a drop in potential energy, with a value of (kT), occurs at the barrier.

According to these assumptions, the potential barrier height is the sole contributing factor to the current flow regardless of the barrier profile. Hence the thermal energy of an electron has to be sufficiently high to surpass the potential barrier in order for thermionic emission to take place. At thermal equilibrium, the electron flow is equal in both directions over a metal/semiconductor interface with, as a consequence, that the current density (J) across the interface is zero. Applying a forward bias voltage (V_f) will cause the Fermi level of the semiconductor to shift to a higher energetic level by an amount of qV_f compared to the Fermi level of the metal. The barrier height for the electron flow is then reduced, resulting in an increase in current density. The current density becomes greater as there is less thermal energy required to surpass the potential barrier. In case of a reverse bias voltage (V_r), the Fermi level of the semiconductor is reduced to a lower energetic level, by an amount of qV_r, compared to the Fermi level in the metal. The barrier height is then increased and the current density from semiconductor to metal reduces below the reverse current density, resulting in a reverse current. The current density in the reverse direction remains the same as the potential barrier Φ_{Bn} from the metal into the semiconductor is determined by the band gap of the semiconductor and either the metal work function or Fermi level pinning and therefore remains unchanged. The total current density for thermionic emission is given by [8,9]:

$$J = J_{ST}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.38}$$

where

$$J_{ST} = A^{*}T^{2}\exp\left(\frac{-q\,\Phi_{Bn}}{kT}\right) \tag{3.39}$$

and

$$A^* = \frac{4\,\pi\,q\,m_n^* k^2}{h^3} \tag{3.40}$$

The total current density is determined by the barrier height (Φ_{Bn}), voltage across the barrier (V) and the temperature (T) where A^* is the Richardson constant, q the electron charge, k Boltzmann's constant, m^*_n the electron effective mass, h Planck's constant. The saturation current density (J_{ST}) is defined by the temperature and barrier height and is therefore independent of the applied voltage.

The diffusion theory

The diffusion theory is based on the transport of charge carriers in a depletion region and is derived from following assumptions [8]:

1) The potential barrier height ($q\Phi_{Bn}$) is greater than the thermal energy of the electrons determined by kT.

2) The effect of electron collisions taking place in the depletion region is included;

3) The current flow does not affect the carrier concentrations at the interface and in the semiconductor.

4) The impurity concentration of the semiconductor does not degenerate.

The current – voltage characteristics can be derived from the current density in the depletion region:

$$J = J_x = q\mu_n n(x)E(x) + q\,D_n\frac{\delta n}{\delta x} \tag{3.41}$$

The current density in the x-direction consists of the electron charge (q), the electron mobility (μ_n), the electron concentration (n(x)), the electric field in the barrier (E(x)) and the diffusion coefficient for electrons (D_n). The current density in the x- direction can only be expressed under this form if the mobility and diffusion coefficient are independent from the electric field [40]. Taking into account this assumption, neglecting the image force induced lowering of the barrier height and the current density, after applying Einstein's relationship ($D_n/\mu_n = kT/q$), can be re-written as:

$$J = J_{SD}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.42}$$

where

$$J_{SD} \equiv \left\{ \frac{q^2 D_n N_C}{kT} \left[\frac{q(V_{bi}-V)2\, N_D}{\varepsilon_{r,s}\varepsilon_0} \right]^{1/2} \exp\left(\frac{-q\,\Phi_{Bn}}{kT} \right) \right\} \tag{3.43}$$

The total current density (J) is determined by the saturation current density (J_{SD}), the applied voltage across the barrier (V) and the temperature (T). The saturation current itself, is determined by the effective density of states in the conduction band (N_c), the built in potential (V_{bi}), the donor concentration (N_D), the permittivity of free space (ε_0) and the relative permittivity of the semiconductor material ($\varepsilon_{r,s}$). The expressions for the current density are similar for the thermionic emission and diffusion theory and are based on the saturation current density. However, the saturation current density for the thermionic emission theory (J_{ST}) is more sensitive to the temperature while the saturation current density of the diffusion theory (J_{SD}) is more sensitive to the applied voltage [9].

The combined thermionic emission / diffusion theory

The diffusion theory is based on the assumption that the electron concentration at the metal/semiconductor is not susceptible to the applied bias. The quasi-Fermi level of the semiconductor, describing the population of the carriers under non-equilibrium conditions, should be equal to the Fermi level of the metal at the interface, in order for the previous assumption to be valid. This would require the quasi-Fermi level to drop off from the bulk semiconductor towards the interface, through the depletion region, which is in sharp contrast to the Fermi level in a p-n junction, where the Fermi level remains flat across the semiconductor material for both types of carriers [40].

The electrons crossing over the potential barrier from the semiconductor into the metal have a higher energy than the conduction electrons in the metal and are therefore not in a thermal equilibrium. Relative to the conduction electrons in the metal, these electrons can then be regarded as “hot” electrons. Due to the difference in energy, the hot electrons have a different quasi-Fermi level compared to the conduction electrons in the metal. This energy is lost as the hot electrons penetrate the metal and collide with the lattice atoms and conduction electrons. Eventually a thermal equilibrium is reached with the conduction electrons in the metal, resulting in a quasi-Fermi level equal to the Fermi level of the metal [40]. This process is similar to the recombination of electrons in a semiconductor and implies that the quasi-Fermi level at the interface does not have to be equal to the Fermi level of the metal. The quasi-Fermi level across the depletion region can now be assumed to be flat as in a p-n junction [40] and is one of the assumptions made in the thermionic

emission theory. The limiting factor to the current flow is different for the diffusion and thermionic emission theory. The current flow is limited by the combined effects of diffusion and drift in the depletion region for the diffusion theory. The limiting factor for the thermionic emission theory lies in the process of emission of electrons into the metal [40]. The transport behaviour in practical cases is a combination between the two extremes of the diffusion theory and the thermionic emission theory and is brought together in a combined thermionic emission/ diffusion theory.

The most complete combined theory is that of Crowell and Sze, which consists of a concept including a recombination velocity (ν_r) at the top of the barrier [40]. The recombination velocity is determined by the electron current into the metal, which consists of the electron flux from the semiconductor to the metal for, which the electron flux from the metal to the semiconductor is subtracted. The effects of quantum mechanical tunnelling, reflection processes and backscattering of electrons have not been taken into account. The total current density is then given in Equation 3.43 and 3.44.

$$J = \frac{qN_C\nu_r}{1+\frac{\nu_r}{\nu_d}} \exp\left(\frac{-q\Phi_{Bn}}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.44}$$

with

$$\nu_d \equiv \left[\int \frac{q}{\mu kT}\left[\frac{-q(\Phi_{Bn}+\psi)}{kT}\right] dx\right] \tag{3.45}$$

The total current density according to the combined theory is then determined by the effective density of states function in the conduction band (N_c), the recombination velocity at the top of the barrier (ν_r), the potential barrier height (Φ_{bn}), Boltzmann's constant (k), the absolute temperature (T), the applied voltage across the barrier (V) and the electron potential energy ($q\psi$). The effective diffusion velocity (ν_d) is associated with the transport of electrons from the edge of the depletion layer to the potential energy maximum and not starting from the interface because of the image force induced barrier height lowering.

When ν_d is greater than ν_r, the transport process will tend towards thermionic emission and in the opposite case the transport process will tend towards diffusion. When the electron mobility (μ_n) is assumed to be independent from the electric field (E) and the image force effects are neglected, then ν_d should be equal to μ_n.E. The Equation 3.46 according to the standard diffusion theory can then be obtained. The complete characteristics for the current

density, including backscattering, reflection processes and quantum mechanical tunnelling, are given by [8]:

$$J = J_{SC}\left[\exp(\frac{qV}{kT}) - 1\right] \quad (3.46)$$

with

$$J_{SC} = A^{**}T^2 \exp(\frac{-q\,\Phi_{Bn}}{kT}) \quad (3.47)$$

where

$$A^{**} = \frac{f_p f_Q A^*}{1+\frac{f_p f_Q \nu_r}{\nu_d}} \quad (3.48)$$

The basic term for the current density (J) remains the same, however the saturation current density now depends on the effective Richardson constant (A^{**}), the temperature (T) and the potential barrier height Φ_{bn}. The effective Richardson constant is determined by the recombination velocity at the top of the barrier (ν_r), the effective diffusion velocity (ν_d), the probability of electron emission over the maximum potential of the barrier height (f_p) and the ratio of the total current flow (f_Q), taking into account quantum mechanical tunnelling and reflection, relative to the current flow neglecting these effects. The probability of emission over the maximum potential of the barrier height can be calculated with Equation 3.49 and the ratio of the total current flow strongly depends on the electrical field and the electron energy at the potential maximum.

$$f_p = \exp\left(-\frac{x_m}{\lambda_{mean}}\right) \quad (3.49)$$

where (x_m) is the position of the maximum potential of the barrier height measured from the interface and (λ_{mean}) is the carrier mean free path at this position.

The effect of the image force on the current – voltage relationship

The current voltage relationship can be expressed in all previous cases in the form of the ideal rectifier characteristic, where J_0 represents the saturation current density:

$$J = J_0\left[\exp(\frac{qV}{kT}) - 1\right] \quad (3.50)$$

In the case of the thermionic emission theory, the saturation current density is dependent on the potential barrier height (Φ_{Bn}).

$$J_0 = A^* T^2 \exp\left(\frac{-q\Phi_{Bn}}{kT}\right) \tag{3.51}$$

The potential barrier height is then supposed to be independent from variations in the electric field at the interface, however there are several reasons why this is not the case. In particular, the image force can reduce the barrier height in an ideal contact without an interface layer. The amount of barrier height reduction ($\Delta\Phi$) depends on the voltage bias [40]. Increasing the forward bias will result in a larger barrier height, reversing the bias voltage will then result in a reduced barrier height [8]. The resulting effective barrier height (Φ_e) is then given by:

$$\Phi_e = \Phi_{Bn} - \Delta\Phi \tag{3.52}$$

When an interface layer is in place, an applied voltage bias will cause an image force induced lowering of the barrier height, also known as the Schottky effect. The Schottky barrier height reduction is in this case given by [8]:

$$\Delta\Phi = \sqrt{\frac{qE}{4\pi\varepsilon_{r,s}\varepsilon_0}} \tag{3.53}$$

The maximum electric field at the interface (E) will then cause the effective barrier height (Φ_e) to be dependent on the applied bias. The electrical field at the interface is not only susceptible to the applied bias, but also to the penetration of the wave functions of electrons from the metal into the semiconductor. The wave functions of electrons contain energies in the metal corresponding to the forbidden gap of the semiconductor material and after penetration decay exponentially. This creates an additional charge from the metal into the semiconductor and can be represented by states, which are often referred to as Metal Induced Gap States (MIGS) [40]. The bias dependence of the effective barrier height can then alter the current voltage characteristics and, when assuming Φ_e/V is constant, is expressed as:

$$\Phi_e = (\Phi_{Bn})_0 - (\Delta\Phi)_0 + \beta V \tag{3.54}$$

The effective barrier height is then determined by the uncorrected barrier height ($(\Phi_{Bn})_0$), image force barrier height ($(\Delta\Phi)_0$) and the voltage variation βV due to MIGS. Adjusting the equation for the ideal rectifier characteristics for the thermionic emission theory then gives:

$$J = A^* T^2 \exp\left(-\frac{q((\Phi_{Bn})_0 - (\Delta\Phi)_0 + \beta V)}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.55}$$

$$J = J_s \exp\left(-\frac{q\beta V}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (3.56)$$

where

$$J \equiv A^* T^2 \exp\left(-\frac{q((\Phi_{Bn})_0 - (\Delta\Phi)_0)}{kT}\right) \quad (3.57)$$

Rewriting Equation 3.55 gives:

$$J = J_s \exp\left(\frac{qV}{nkT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (3.58)$$

where

$$\frac{1}{n} = 1 - \beta = 1 - \left(\frac{\delta\Phi_e}{\delta V}\right) \quad (3.59)$$

The factor n is called the ideality factor and is constant when Φ_e/V is constant. The current density including the ideality factor can be simplified when V is larger than 3kT/q:

$$J = J_s \exp\left(\frac{qV}{nkT}\right) \quad (3.60)$$

for V > 3kT/q

In practice, the ideality factor is not a constant as Φ_e/V is not constant but can be determined experimentally by extraction from the current voltage characteristics:

$$\frac{1}{n} = \frac{kT}{q}\frac{d}{dV}\ln\left[\frac{J}{1-\exp\left(-\frac{qV}{kT}\right)}\right] \quad (3.61)$$

or if (V> 3kT/q)

$$\frac{1}{n} = \frac{kT}{q}\frac{d}{dV}\ln(J) \quad (3.62)$$

In this case, the ideality factor depends on the bias (V) and can only be specified for a particular point on a current voltage characteristic. The current voltage characteristics of a metal/ semiconductor contact under reverse and forward bias, forming a Schottky diode, can be seen in Figure 3.23. The dependence of the ideality factor on the applied bias can be observed as the Schottky diode becomes leakier as n increases. As a result, the Schottky diode shows higher conduction in the reverse bias compared to forward bias.

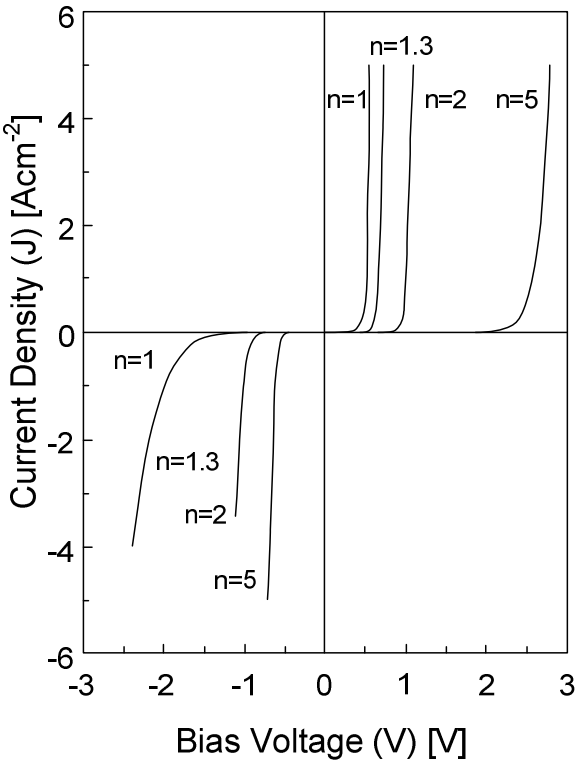


Figure 3.23: Schottky diode characteristics and the dependence on the ideality factor (n) [11]

3.6.3.2 Tunnelling through the barrier

The second basic transport process, quantum mechanical tunnelling, will be described using a metal to n-type semiconductor contact under forward bias. The transport process is based on the principle that electrons, with energies below the potential barrier maximum, can penetrate the barrier under certain circumstances by quantum mechanical tunnelling. Two cases of quantum mechanical tunnelling can be observed, field emission (FE) and thermionic field emission (TFE). The corresponding energy band diagrams are shown in Figure 3.22 (1 and 2).

In the case of highly doped semiconductor material ($N_D > 10^{18}cm^{-3}$) at the metal/semiconductor interface, field emission (FE) takes place as the depletion region width (W_D) of the Schottky barrier, close to the Fermi level energy, is narrow enough to allow for quantum mechanical tunnelling. The depletion width also depends upon the semiconductor material, as shown in Equation 3.31, and therefore field emission takes place at different doping densities for different semiconductor materials. Ohmic contacts usually consist of Schottky barriers on highly doped n-type semiconductor material and are predominantly driven by field emission. At intermediate levels of doping ($10^{17}cm^{-3} < N_D < 10^{18}cm^{-3}$), the depletion region width close to the Fermi level is too large for quantum

mechanical tunnelling to take place. When the temperature is raised, the electrons are excited to a higher energy level and the probability of quantum mechanical tunnelling increases. The electrons then encounter a thinner potential barrier and can tunnel through the barrier. This transport process is known as thermally assisted quantum mechanical tunnelling or thermionic field emission. Decreasing the doping to lower levels will require the electrons to travel over the top of the barrier height, resulting in thermionic emission [40,8]. Using the ideality factor [43], a universal expression for the current density for the different transport mechanisms (FE, TFE and TE) can be found, stated by equation:

$$J = J_s \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{3.63}$$

The saturation current density (J_S) is given by Equation 3.63, and the ideality factor (n) is used as a fitting parameter in order to fit the practical current voltage characteristics to the universal equation rather than a parameter indicating the dependence of Φ_e/V. It is assumed that when the ideality factor equals to 1, the transport mechanism is purely thermionic emission. When the ideality factor is between 1 and 2 it is assumed that thermionic field emission takes place. And in the case of the ideality factor being greater than 2, it is assumed that field emission takes place. Hence there is a relationship between the ideality factor and the transport mechanism. The more dominant field emission becomes as a transport mechanism, the higher the ideality factor [43].

3.6.3.3 Recombination in the depletion region

The transport mechanism based on the recombination of carriers in the depletion is caused by localised energy states within the band gap. These localised energy states exist in the vicinity of the metal/semiconductor junction and result from stresses and crystal lattice deformations. As a result, electrons may be captured by these states and can be re-emitted into the same energy bands. The states are traps and occur in the forbidden energy zone or band gap (E_g). When a state is occupied by an electron or a hole and returns to a neutral level, due to the capture of an opposite carrier, the states are called recombination centres [40]. The current density in Schottky diodes due to the recombination centres is based on the theory of Shockley, Read and Hall [237] and can be expressed as:

$$J_r = J_{r0} \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{3.64}$$

where

$$J_{r0} = \frac{qn_iW}{2\tau_r} \tag{3.65}$$

and $n = 2$

The current density induced by recombination in the depletion region is then determined by the electron charge (q), the intrinsic electron concentration (n_i), the depletion region width (W_D) and the life time within the depletion region (τ_r). However, three assumptions have to be made in order for this equation to be valid [40]:

1) The energy levels of the recombination centres coincide with the intrinsic Fermi level.
2) The capture cross sections are equal for electrons and holes.
3) The centres are distributed in a uniform manner across the interface.

These assumptions are very likely to be untrue in practice, as the hole and electron capture cross sections, can differ up to three orders of magnitude. The ideality factor value (n) for the recombination current density is between 1 and 2 and depends on the ratio of the capture cross sections for electrons and holes [40]. Assuming the three assumptions are valid the total current density is then given by:

$$J_{total} = J_{TE} + J_r \tag{3.66}$$

where

$$J_{total} = \left[J_{ST}\exp\left(\frac{qV}{nkT}\right) + J_{r0}\exp\left(\frac{qV}{2kT}\right)\right]\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{3.67}$$

This is the total current density combining thermionic emission theory (J_{TE}) and recombination theory (J_r) and has a ratio of thermionic emission current density to recombination current density proportional to:

$$T^2\,\tau_r\exp\left(\frac{q(E_g + V - 2\Phi_{Bn})}{2kT}\right) \tag{3.68}$$

The ratio then depends on the properties of the semiconductor, temperature and applied voltage. When the lifetime, applied voltage and band gap increase the thermionic emission becomes the main transport mechanism. The recombination transport mechanism is then more prominent in material with low lifetime, with a high barrier, biased at low voltage and under a low temperature. The temperature variation of the forward current then

consists of two activation energies [40]. At a high temperature, the thermionic emission component is more prominent and the activation energy tends towards the value $\Phi_{Bn} - V$, and at low temperatures the temperature approaches the value of $(E_g - V)/2$, which is a characteristic of the recombination component.

3.6.3.4 Hole injection

The hole injection transport process is based on the fact that if Φ_{Bn} is greater than $E_g/2$, the semiconductor material at the interface can become p-type, containing a high density of holes. Some of these holes are capable of diffusing into the neutral region of the semiconductor under forward bias, hence creating the injection of holes.

The transport mechanism of hole injection through the depletion region is identical to the transport mechanism for holes in a p-n junction. The current density can then be given by [40]:

$$J_h = J_{0h}\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3.69}$$

where

$$J_{0h} = \left[\frac{qN_v\,\nu}{(3r_h)^{1/2}}\right]\exp\left(-\frac{q\Phi_h}{kT}\right) \tag{3.70}$$

The current density for hole injection is then determined by the effective density of states function in the valence band (N_v), the mean thermal velocity of the holes (ν) and the barrier for holes (Φ_h). The term (r_h) consists of the recombination time for holes (τ_{rh}) and the mean time between collisions for holes (τ_{ch}) and is defined by [40, 42]:

$$r_h = \frac{\tau_{rh}}{\tau_{ch}} \tag{3.71}$$

The ratio between hole injection (γ_h) and the electron transport mechanism is given by [8]:

$$\gamma_h = \frac{J_h}{J_e + J_h} \cong \frac{J_h}{J_e} = \frac{4\,N_v}{(3r_h)^{1/2}N_C}\exp\left(-\frac{q(\Phi_h - \Phi_{Bn})}{kT}\right) \tag{3.72}$$

In the case of thermionic emission, the electron current density (J_e) is equal to J_{te} and given by Equation 3.37. Equation 3.72 indicates that an increase of the Schottky barrier height (Φ_{bn}) leads to an increase of (γ_h) as an increased barrier height reduces the electron current density.

In practice, the hole injection ratio (γ_h) is generally negligible, hence a Schottky diode is described as a "majority carrier" device [40, 8]. The hole injection ratio is susceptible to the interface between the metal and the semiconductor as a thin interfacial layer can increase the hole injection [40] and can become appreciable at high forward current densities. This effect is only noticeable on Schottky contacts with large barrier heights on weakly doped semiconductor material [40].

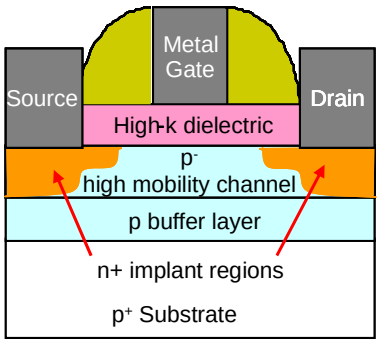
3.7 Advanced architectures

In order to control the short channel effects in scaled inversion mode devices, the channel doping has to be increased. The increased doping levels in the channel result in a decrease in channel mobility, which has a detrimental effect on the device performance. The detrimental effects of scaling will eventually outweigh the benefits of scaling and alternative MOSFET device architectures should be considered. At the start of this work, four device architectures, shown in Figure 3.24, were being actively explored as the test bed for assessing the potential of III-V MOSFETs.

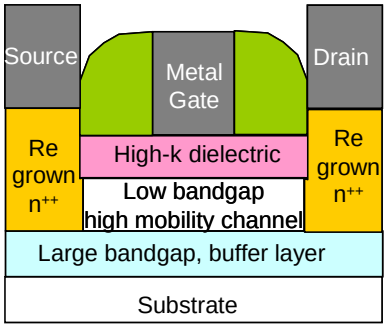
The inversion mode architecture, shown in Figure 3.24a, pursued by teams at the University of Purdue [44], National Tsing Hua University (NTSU) [45], Intel [46] and University of Texas [47], is a III-V embodiment of a traditional bulk silicon MOSFET. An inversion channel is formed at the interface between the high mobility semiconductor layer and the gate dielectric. The source and drain regions are formed by ion implantation. In terms of the source and drain formation, limitations on the maximum activation efficiency of ion implantation in III-V materials, given the restricted thermal budget (the III-V layers are usually grown at less than 600°C, implant activation annealing at any higher temperature will result in significant As out diffusion, degrading the properties of the high mobility channel material, may unacceptably increase the contact resistances. Even in close to ideal situations, in-situ Si doping during the epitaxial growth of $In_{0.53}Ga_{0.47}As$ yields maximum densities of 5-6x$10^{19}cm^{-3}$ [48], which is significantly below the values, which are likely to be required to form sufficiently low access resistances in channels of no more than 10nm thickness. So, whilst the inversion mode architecture is perhaps a good candidate in terms of electrostatic scalability, to fully control short channel effects via implantation strategies, as used extensively in scaling silicon devices, may have severe limitations on attainable access resistance.

The re-grown source/drain architecture of Figure 3.24b, pursued by the SRC Non-Classical CMOS Research Centre led by University of California Santa Barbara [49, 246], is essentially a variant on the inversion mode MOSFET, where the highly doped, re-grown source and drain regions are designed to address the access resistance issue arising from the limitations of ion implantation in III-V materials mentioned above. In addition, to further reduce the access resistance, source and drain contact metals are deposited in-situ following the raised source and drain re-growth. Thin sidewall spacers are required in this architecture to prevent the source/drain re-grown regions from shorting to the gate.

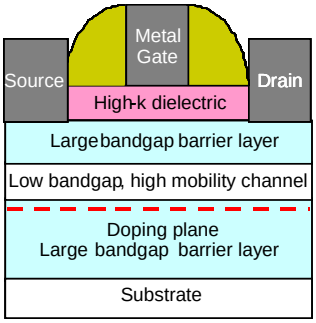
The flat-band architecture of Figure 3.24c, initially developed by Motorola/Freescale [5] and subsequently carried forward in collaboration with the University of Glasgow [4], takes its origins from a classic III-V HEMT structure, in that the channel is formed in a high mobility, low band gap, buried channel layer embedded within larger band gap materials. The carriers are thus well confined, providing charge control within the channel comparable to that achieved in ultra-thin body SOI MOSFETs. Further, the channel is spatially separated from the gate dielectric therefore interface roughness scattering is likely to be reduced, and larger capacitive effective thickness can be expected. The doping arrangement ensures that the access regions on either side of the gate have low resistance and the channel is depleted by the work-function of a metal gate, however for highly scaled devices, defining the source/drain contacts directly on the large band gap material above, the channel may compromise the achievable access resistance.



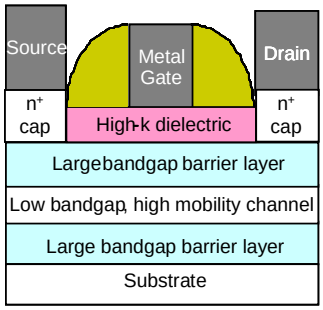
(a) – Inversion mode architecture



(b) – Regrown source/drain architecture



(c) – Flatband mode architecture



(d) – Recess gate architecture

Figure 3.24: Various III-V MOSFET architectures currently being investigated

The recessed gate architecture of Figure 3.24d, pursued by IBM [50, 241, 242, 244, 245], is also a buried channel solution, which should benefit from higher mobility due to reduced dielectric-semiconductor interface roughness scattering. In some ways, this architecture is similar to the raised source/drain structure of Figure 3.24b, in that the access resistance is reduced by having a heavily doped cap layer between the source/drain contacts and the gate. The gate is formed in a recess etched through the heavily doped cap. This structure has many of the other electrostatic and confinement advantages of the flat-band architecture of Figure 3.24c. From a manufacturing perspective, this architecture may have issues with threshold voltage uniformity due to variations in recess etch depth experienced by III-V HEMTs.

Current device architecture is moving away from the typical planar device structure towards a multi gate device structure [2]. The purpose of a multi gate structure is to increase the surface of the gate in regard to the channel and hence improving the gate control on the channel. The improved gate control enables the devices to operate at a lower voltage, with less leakage current and therefore the power consumption of a chip is

significantly reduced. The most common non-planar multi gate structure is a FinFET, which comes in three main variations; double gate, tri-gate and omega gate, as shown in Figure 3.25. The distinguishing characteristic of the FinFET is that the channel is a thin "fin", which is wrapped by a gate metal. The effective channel length of a FinFET is determined by the distance between the source and the drain. All FinFET structures are affected by the same basic issues. The fabrication of quality fins with a uniformly grown oxide requires more complex device processing. These issues were overcome, as experimental III-V FinFETs [238, 243] and large volume production compatible Tri-gate SI FinFETs [2], were demonstrated.

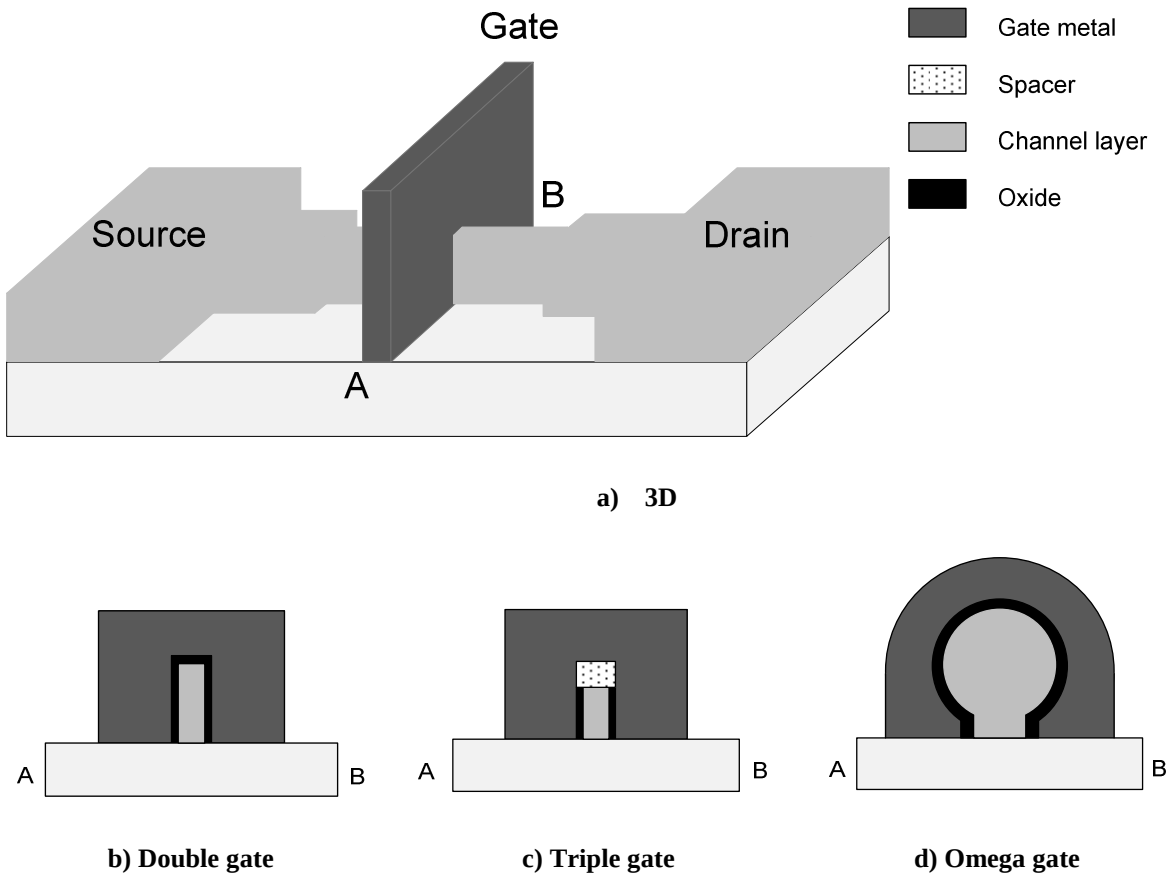


Figure 3.25: Representation of a generic FinFET and cross section of three fin variations

3.8 Summary

This chapter has explored how III-V MOSFETs can become an alternative to Si technology in the future. First, the ideal operation of the classic bulk silicon MOSFET is described. As future technology will require a density scaling of transistors in order to keep up with Moore's law, the different scaling methodologies and the key parameters, which are impacted by the reduction of the device dimensions, are discussed. The figures of merit of future scaled n-type MOSFETs are shown together with the Intel 45nm technology as a benchmark.

In order to better understand the potential benefits of III-V channel material, a study of the metal/oxide/semiconductor interface, channel transport properties and metal semiconductor contacts, is then undertaken. This covers the benefits of high-k gate dielectrics, metal gates and alternative channel materials featuring heterostructures. As this work focuses on ohmic contacts, a more in depth study of the different transport mechanisms present in metal and semiconductor contacts, such as emission over and through the barrier, recombination and hole injection.

Finally, MOSFET devices with advanced architectures will be discussed and compared to the classic bulk silicon MOSFET. The combination of advanced architectures and compound semiconductor materials with high channel mobility channels then allow scaling beyond that offered by Silicon technology. Therefore, the device material in this work features either a buried channel or surface channel device architecture with high-mobility $In_xGa_{1-x}As$ channel material, which eventually could be co-integrated on a Si 200mm platform.

4 Fabrication techniques

4.1 Introduction

Device performance, uniformity, reliability and repeatability can only be achieved by developing and integrating stable, low damage process modules. It is then key to have a fundamental understanding of the fabrication techniques used when expanding existing procedures or developing new processes. The principle techniques involved in device fabrication are described and analysed in this chapter. The fabrication techniques used in this project are semiconductor wafer growth, lithography, dielectric deposition, metal deposition and metal- and semiconductor etching. The principles of each individual process are discussed, together with an analysis of their benefits, limitations and effects on device performance.

4.2 Semiconductor wafer growth

4.2.1 Molecular beam epitaxy [74,75]

High quality semiconductor material is the base of the work performed in this project and will therefore be discussed first. As previously described in chapter 3.7, it is now generally accepted that III-V MOSFET devices require heterojunctions with abrupt atomic layer definition for optimal electrostatic control. The quality of the devices then depends upon the precision of the fabrication technique used to realise the heterostructure. The semiconductor growth technique used in this work is Molecular Beam Epitaxy (MBE), which grows the III-V layers with atomic layer precision. The dual chamber MBE system used at the University of Glasgow is shown schematically in Figure 4.1 and will be explained in the following paragraphs.

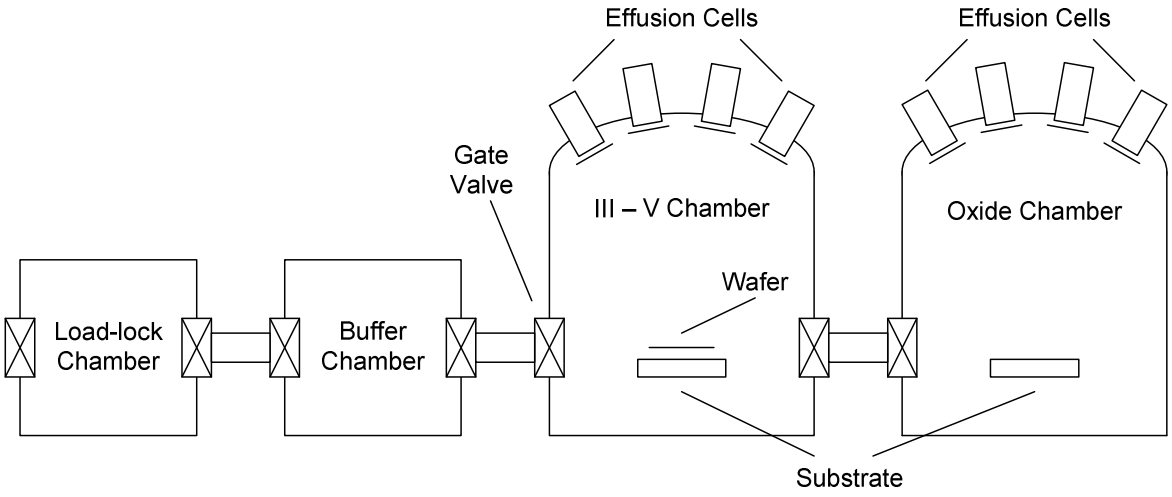


Figure 4.1: Schematic representation of dual chamber Molecular Beam Epitaxy growth system

The source material (e.g. Ga, Gd, In, As, Al, Si) is heated up in effusion cells to the point it starts evaporating. The atomic flux from the cells is dependent on the temperature of the cells and is then used to control the growth rate. Each effusion cell has a shutter to isolate it from the substrate, to control if the flux impinges on the substrate or not. The temperature of the substrates, used in this work, varies from 400°C to 640°C for material growth. To minimise the contamination of the wafers, the growth chamber needs an ultra high vacuum (UHV) with a pressure of $1x10^{-8}$mTorr and the source material needs to have a purity of at least 99.99999%. The contamination can manifest itself as inconsistent doping levels or as increased trap density. The requirement of a UHV limits the size of the growth chamber. One of the main drawbacks of the MBE tool is the processing of multiple large diameter wafers. This requires a higher complexity of the system resulting in a higher cost. This limits the use of a MBE tool for industrial requirements, but it is still very useful in a research environment. In industry, semiconductor growth tools with a higher throughput, such as metal organic chemical vapour deposition (MOCVD), are used.

The III-V heterostructure layers are grown in one chamber to form the III-V MOSFET device heterostructure. The oxide on the heterostructure is grown in a different chamber linked to the III-V chamber via a transfer tube, which is also under UHV. The effusion cells in the oxide chamber are equipped with individual cooling and are capable to run up to temperatures of 2000°C.

The oxide chamber in Glasgow has been used for the growth of a Ga_2O/GaGdO (GGO) dielectric stack. The sources used to form the GGO stack are polycrystalline Ga_2O_3, Gd

and O_2. The gallium oxide source sublimes at a temperature of 1990°C resulting in a flux of O_2 and Ga_2O molecules [52]. The Ga_2O molecules have a higher sticking coefficient on GaAs than O_2 and passivate the GaAs surface. Additional flows of atomic Gd and O_2 are used to grow a $Gd_xGa_{0.4-x}O_{0.6}$ (GGO) layer on top of the passivated GaAs/Ga_2O_3 to increase the dielectric constant of the gate oxide stack and to reduce gate leakage as the conduction band offset between Ga_2O_3 and GaAs is insufficient as seen in figure 3.11.

The quality of the growth is verified via an in-situ reflection high electron energy diffraction (RHEED) diagnostic tool. A beam of electrons is directed towards the wafer surface under a small angle of 1 – 2° and is reflected by the crystal surface. The reflected beam then strikes a fluorescent screen, which shows the diffraction pattern of the electrons. When the surface of the crystal is perfect, a set of lines separated by distances proportional to the atomic spaces is observed. A spotted diffraction pattern indicates a rough crystal surface suggesting poor growth conditions. The growth rate of III-V material and the surface quality can then be determined using the RHEED surface diagnostic tool.

The growth rate of the III-V material can be observed as the RHEED intensity changes as the surface goes through a cycle of becoming rougher and smoothing back out as each monolayer is completed. The interaction between the Ga_2O and GaAs can also be monitored via RHEED as it is important to have a passivation layer between semiconductor and oxide to limit defect density. After the deposition of the first monolayer of Ga_2O the crystal structure goes from crystalline to amorphous over multiple monolayers, which can be monitored using the RHEED diagnostic tool. The pattern on the RHEED diagnostic tool will then have a transition from a crystalline pattern to a ring pattern, which is characteristic for amorphous materials. The growth rate of the Ga_2O_3 layer is then determined from the time it takes for the amorphous ring structures to appear.

4.2.2 Atomic Layer Deposition [76]

Atomic layer deposition (ALD) is based on a gas phase chemical process, which is repeated until the required thickness of the film is reached. The ALD technique was used in this work to deposit a Al_2O_3 oxide layer on $In_{0.53}GaAs$ MOSFET device material and was grown at Stanford. Most commonly, the ALD deposition technique uses two separate chemical reactants called precursors. The precursors react in a sequential manner and every exposure to a single precursor will build up a mono layer of atoms on top of the underlying surface. Since a single layer is deposited with every exposure, the amount of material deposited in each reaction cycle is constant, resulting in uniform and thin conformal films.

The growth of materials by ALD is broken up into two half-reactions. The substrate is exposed to the first precursor, which is often an organo-metallic compound. Then the chamber is purged with either nitrogen or argon gas to remove excess non-reacted precursor material and the by-products. The sample is then exposed to the second precursor and is purged afterwards. This process is repeated until the desired film thickness is reached. The amount of material deposited during each reaction cycle is known as the growth per cycle. As an example, the growth of a thin film of Al_2O_3 on GaAs is described:

1. In air, most surfaces form a hydroxyl group and the sample is then put into the ALD chamber.
2. The first precursor is then pumped into the chamber, which is trimethyl aluminium (TMA). This reacts with the hydroxyl group producing methane as a by product:

$$\mathrm{Al\,(CH_3)_3 + \ GaAs - O - H \ \rightarrow GaAs - O - Al(CH_3)_2 + \ CH_4}$$

3. The chamber is then purged removing the excess trimethyl aluminium and methane.
4. The second precursor is then introduced, which is H_2O. The dangling methyl groups then react with the H_2O forming aluminium-oxide bridges and hydroxyl groups. Again, the by-product is methane.

$$\mathrm{GaAs - O - Al(CH_3)_2 + \ 2H_2O \ \rightarrow GaAs - O - Al(OH)_2 + \ 2CH_4}$$

5. The chamber is purged again and prepared for another trimethyl aluminium precursor reaction.

Repeating the cycle then forms a thin layer of Al_2O_3 on a GaAs substrate. Since the film thickness depends on the number of reaction cycles, the control of the layer thickness is simple and accurate. A single cycle layer thickness roughly takes 0.5s. The chemical nature of the process means there is little need for reactant flux homogeneity and parameters other than substrate material, precursors and processing temperatures have insignificant influence on the process. Another advantage is that there is no need for a plasma resulting in limited damage in the substrate [77] and high density and low impurity films, as shown in section 4.4.5. The temperature of the process can be below 200°C [221] in order not to affect sensitive substrates with epitaxially grown layers.

The sequential nature of purging gases means that the ALD technique is slow when thicker films are needed. Also, the residues from the precursors form a risk for the amount of impurities in the film.

4.3 Lithography

The cornerstone of electronic device fabrication is the use of masking layers to selectively pattern a surface. The pattern can then be used to selectively remove or deposit material. The term for the masking process is lithography and it encompasses many techniques. The lithography techniques can be divided up in two main categories: stamping or printing based lithography [53, 54, 55, 56] and an irradiation exposure based lithography. Although the nano-imprint technique is becoming increasingly more popular, only irradiation exposure based lithography has been used in this project.

The irradiation exposure based lithography is based on depositing a radiation-sensitive mask, which is usually a polymer. This resist layer can be uniformly applied to the surface of the sample by either spin coating or spraying. When the resist is exposed to either UV or electron radiation the physical properties of the resist change. The irradiated regions then become either more or less soluble in a developing solution.

When the irradiated region becomes more soluble, the resist is called positive tone. In case of electron radiation, the irradiation causes the polymer chains to break up by chain scission [57]. The depolymerised regions can then be dissolved by making use of an appropriate developer given sufficient time. The irradiated regions become unmasked when using positive resist.

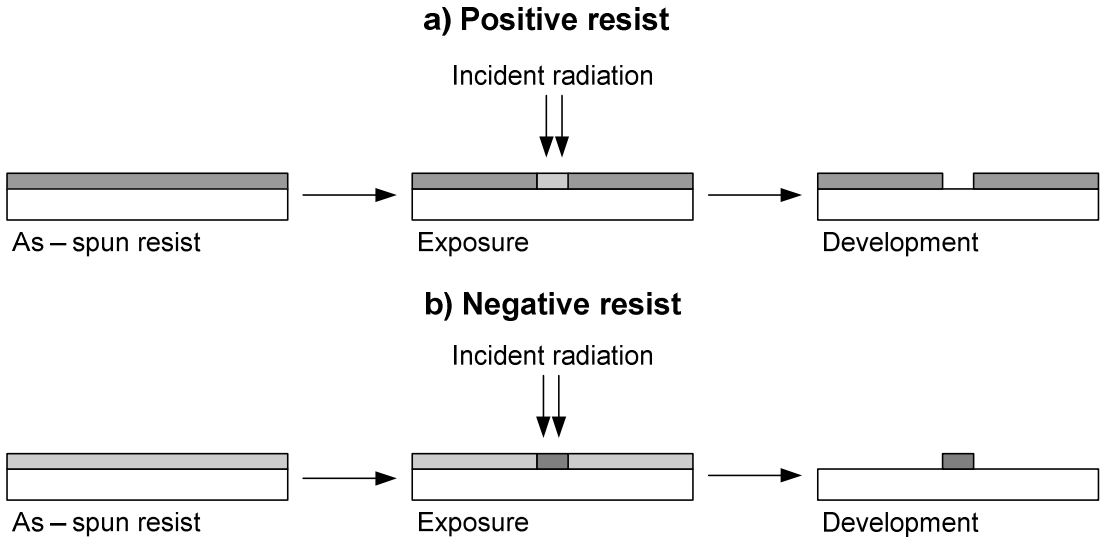


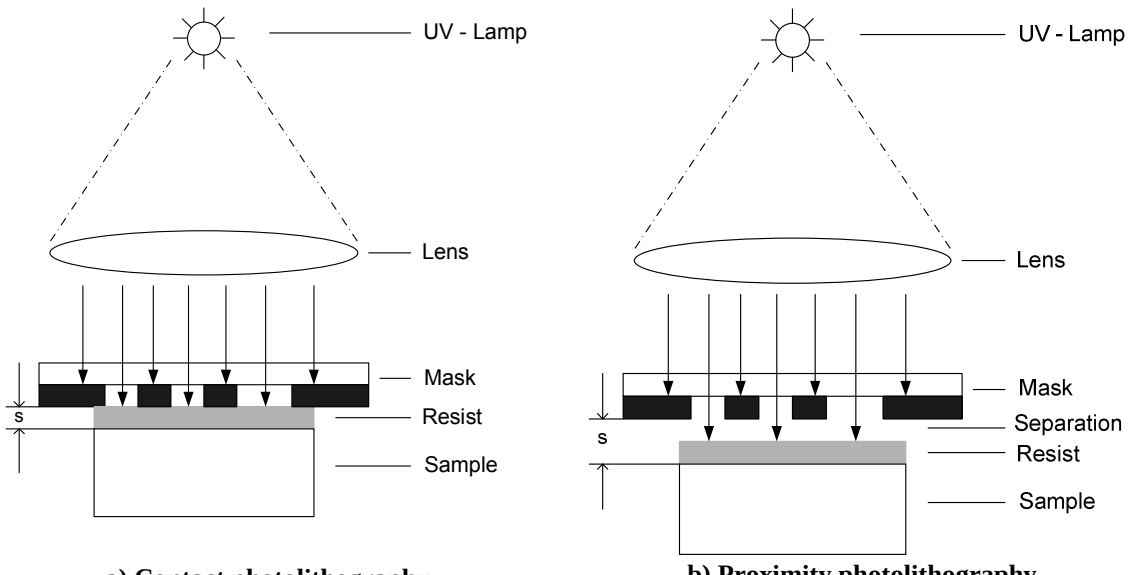
Figure 4.2: Development of positive and negative resist

If the irradiated region becomes less soluble, the resist is negative tone. In the case of electron radiation, the irradiation results in a linking of the polymer chains increasing the

average chain length. The exposed regions then become less soluble in comparison to the unexposed regions. The unexposed regions then become unmasked by the development process. The positive and negative resist processing is shown in Figure 4.2. The resolution of a resist based lithographic process is limited by several factors: the type of radiation, the incidence of radiation and the chemistry of the resists. The most commonly used lithography in this project is e-beam lithography using resist with positive tone.

4.3.1 Photo lithography

The lithography technique used in CMOS fabrication has to provide a high throughput, scaled feature sizes and low unit processing costs. The high throughputs compared to e-beam lithography makes photolithography the dominant lithography technique used by industry. The basic principle of photolithography consists of using a hard mask to block UV-light onto resist coated substrates. There are three main photolithograpy techniques: contact, proximity and projection. The proximity and contact process are very simple and comprise a light source, lens, hard mask and a resist coated sample. The difference between the two is that the hard mask either contacts or is in close proximity (>10µm) to the resist coated sample shown in Figure 4.3.



a) Contact photolithography **b) Proximity photolithography**

Figure 4.3: Schematic representation of basic photolithography techniques

Contacting the resist layer can introduce cross contamination between wafers and cause damage and is not suitable for modern device processing requirements. The gap between the hard mask and resist coated sample prevents the cross contamination, but potentially allows for diffraction of the UV light. The minimal theoretical resolution for proximity

lithography, l_{min}, is determined by the separation between mask and substrate (s) and illumination wavelength (λ).

$$l_{min} = \sqrt{\lambda s} \quad (4.1)$$

The wavelength of deep ultra violet is 193nm, which can be achieved by making use of a ArF excimer laser. Theoretically, a resolution of around 300nm can be achieved using a 500nm thick resist. The flatness of the wafer will limit the minimum separation distance, which will consequently reduce the resolution in practice.

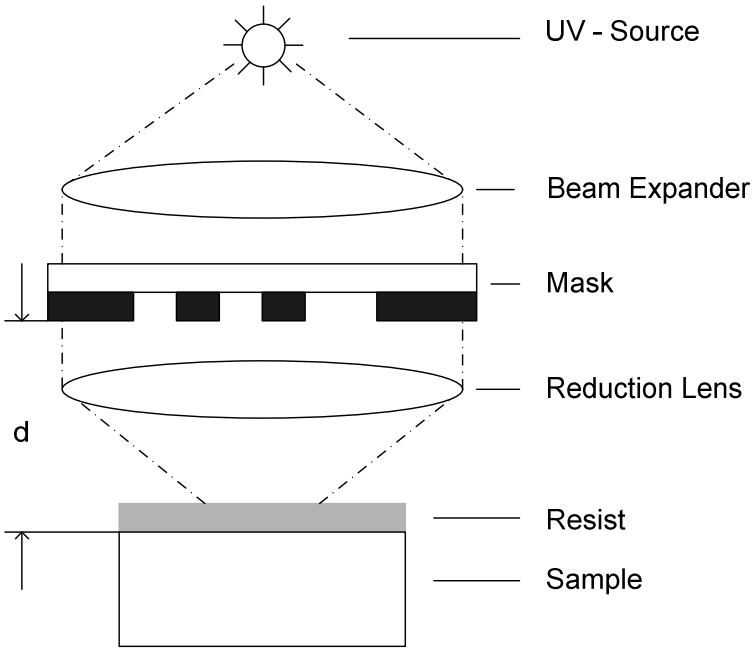


Figure 4.4: Schematic representation of projection lithography

The projection photolithography technique is based on focussing the beam of UV light by making use of a lens. The lens is positioned between the hard mask and the substrate and a simplified schematic is shown in Figure 4.4. Focussing the beam allows for a better resolution compared to the proximity photolithography without the detrimental effects from contact photolithography. The resolution limit for a projection system is defined as [8]:

$$l_{min} = \frac{k_{res}\lambda}{NA} \quad (4.2)$$

where k_{res} is a constant describing the ideality factor of a resist, wave length (λ) and the numerical aperture of the lens NA. The numerical aperture specifies the refractive properties of the lens and is a number between 0 and 1, characterising the angular extent of the lens. Modern low-k_{res} value resist and high-NA lenses have allowed for resolutions as

small as 30nm [17]. Other photolithography improvements, such as multiple exposures [58], phase shifting techniques [59] and resist etchback [60], have contributed to cost effective processing of critical geometries required by the silicon industry. The use of automatic registration schemes is another advantage of projection lithography enabling a high throughput with accurate alignment. These advantages makes the projection photolithography the most commonly used lithography techniques, however the systems are extremely expensive and can only be found in a handful of companies around the world.

4.3.2 Electron beam lithography

The resolution of photolithography is limited by the wavelength of the source due to diffraction, as shown in Equations 4.1 and 4.2. Electron beam Lithography (e-beam) uses a focussed beam of electrons instead of a hard mask. The pattern can then be generated by software and is written directly onto the resist with the help of a computer controlled exposure system. The diffraction of e-beam systems is limited by the de Broglie wavelength of the electron beam rather than the diffraction of light when using a hard mask. At a typical operating energy of 100keV, the diffraction of an e-beam is around 0.004nm, which is smaller than the spacing between atoms on any substrate material [61, 62]. Diffraction is therefore not an issue on e-beam systems, however the minimal resolution is dependent on the spot size and electron scattering. The quality of the electron optics determines the spot size but is limited by the mutual repulsion of electrons when being forced into a focussed beam. The detrimental effects of electron scattering come from two different electron components. First, when the e-beam hits the resist surface, it causes additional lateral exposure. Secondly, electrons can scatter backwards from the substrate increasing the secondary exposure, which results in line widening. The pattern dependent exposure is called the proximity effect.

A typical electron beam lithography system consist of three major parts: an electron source, an electronic lens system and the sample chamber, as shown in Figure 4.5, which is a schematic of the Vistec VB6 e-beam lithography tool used in this work. The electron source is a thermal field emitter using a zirconium oxide-coated tungsten cathode, which after heating emits electrons, which are then accelerated with voltages up to 100kV improving emission collimation. The higher accelerating voltages provide a smaller spot size at the expense of lower beam current densities, resulting in increased writing times.

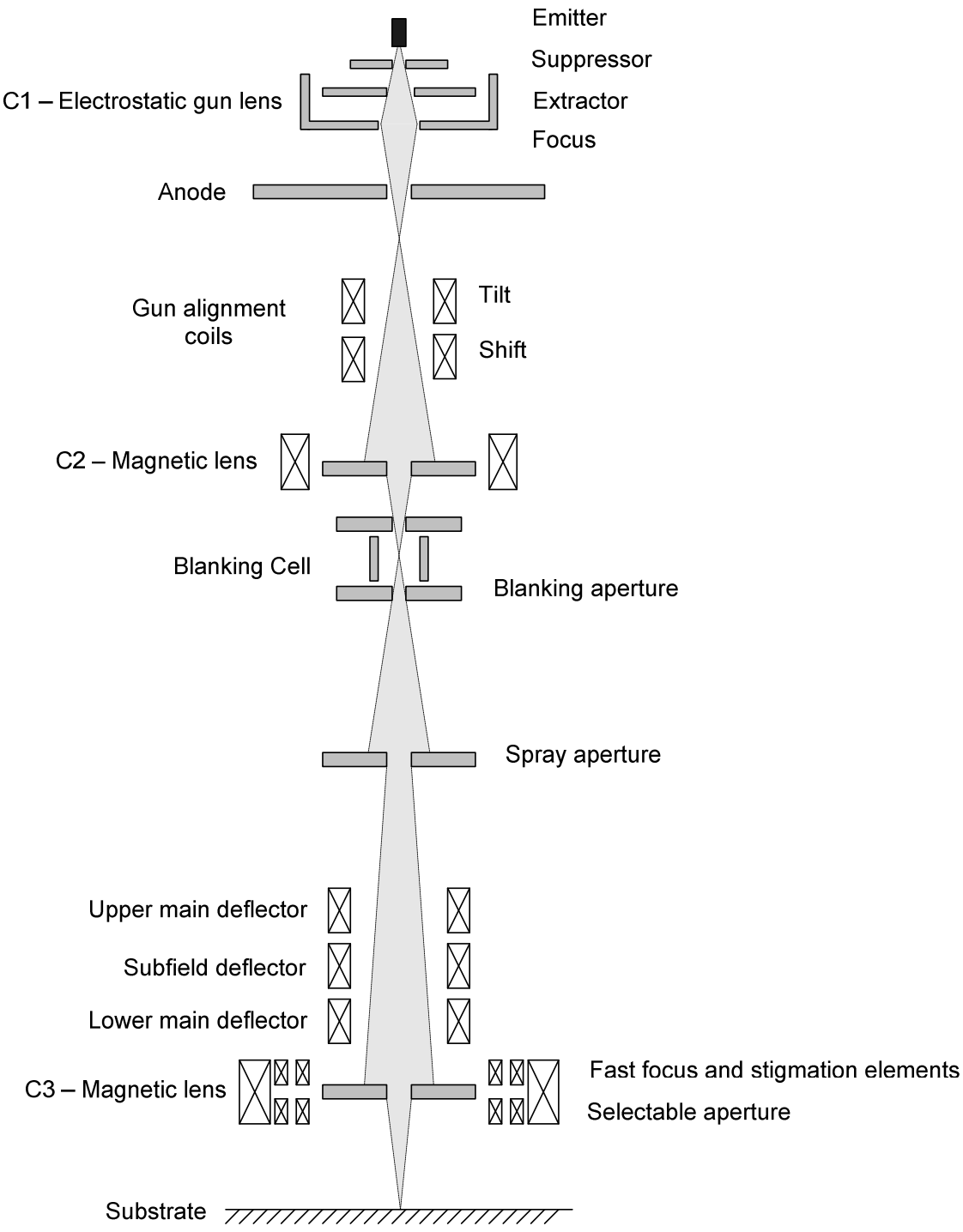


Figure 4.5: Schematic representation of a Vistec VB6 e-beam lithography tool [78]

The suppressor and extractor create a flow of electrons from a cathode, present in the emitter, through an electrostatic gun lens focusing the beam towards the anode. The electron beam then passes through gun alignment coils, which align the electron beam to the central 2D axis for optimal spot formation. A magnetic lens then focuses the beam and the blanking cell is used to deflect the beam away from the sample. The patterns are

generated by different deflectors before a final magnetic lens, which has to be adjusted for a given working distance. This system allows for a selective exposure within a limited region without having to move the substrate. The final beam focus determines the spot geometry and therefore also the minimum resolution, which can be calculated from:

$$d = k_{spot} C_s^{\left(\frac{1}{4}\right)} \lambda^{\left(\frac{3}{4}\right)} \quad (4.3)$$

Where k_{spot} is an ideality constant, which defines the sharpness of the spot and C_s is the spherical aberration of the final lens. The minimum ideal spot size has been calculated by Broers et al. [61] and was found to be 0.37nm at 100kV. Due to imperfect electron optics, the modern e-beam lithography tools have minimum spot sizes varying from 1 – 5nm. The Vistec VB6 tool used at the University of Glasgow has a digital pattern resolution 1.25nm, however the minimum spot size is 4nm.

The sample chamber contains a precision translational stage, a Faraday cup and detectors to measure the x, y and z position, beam current and electron backscattering. The stage is usually driven piezoelectrically and is controlled using feedback from laser interferometers, which measure the x and y travel. The offset in the vertical or z direction is measured, using a second laser with a photodiode detector. The measurement of the vertical direction is critical as it will determine the focus of the e-beam. The mechanical precision of the stage movements is usually a lot lower than the precision of the beam deflectors and will predominantly determine the field stitching accuracy. The Faraday cup is used to measure the electron current density of the e-beam, which is a feedback to calculate the exposure time. The visual representation of the samples is provided by a backscatter detector, which is similar to the operation of a scanning electron microscope. The visual representation can also be used for automatic sensing and alignment markers registration, which is all software controlled.

The patterns are first designed in the CAD package L-edit by Tanner EDA resulting in a GDS layout file. The pattern then has to be fractured up into smaller area structures (1.2mm x 1.2mm) as the lithography tool can only write within fields of this size. The fracturing software used is a CATS package by Synopsis. The fractured patterns can then be positioned on a virtual sample in Belle, which is in-house software created at the University of Glasgow. The Belle software also allows selection of the beam size, beam current and the dose. When saving, the exposure times are then calculated and this command file can then be used by the control computer of the VB6 system.

4.3.2.1 Proximity effects and scattering

The minimum feature size is dependent on the electron beam interaction between the resist and the substrate. Electrons are scattered once the beam penetrates the resist, altering their velocities and direction of travel. This results in an increased lateral exposure of the resist and consequently the minimum feature size will be larger than the minimum spot size. Scattered electrons can produce secondary electrons provided they have enough energy, which then travel in random directions with low energies. The scattering process is shown in Figure 4.6.

Electrons, which keep travelling towards the substrate after scattering are defined as forward scattering electrons. The forward scattering is inversely proportional to the energy of the electrons, and broadens the Gaussian profile of the beam energy [61].

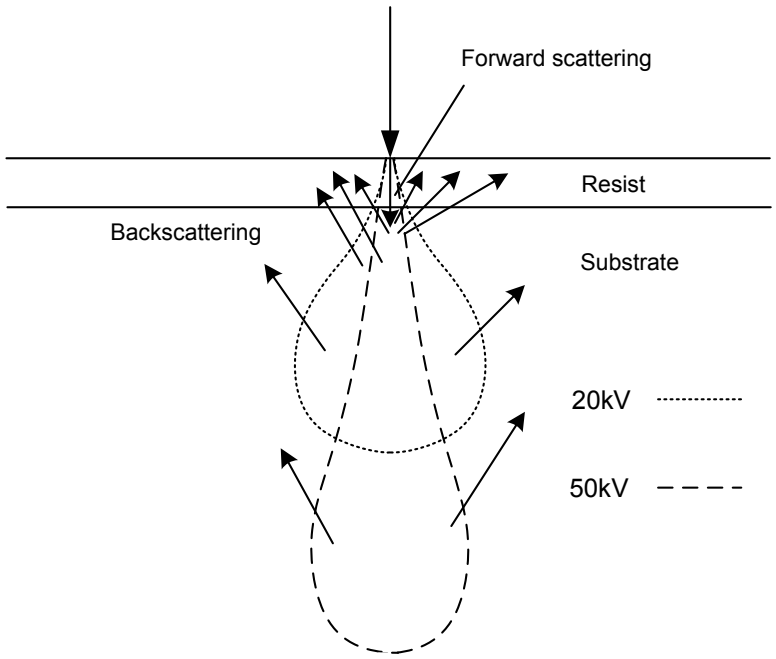


Figure 4.6: Schematic representation of the interaction between incident electrons and the resist and the substrate [61].

The substrate can also be penetrated by electrons given sufficiently high accelerating voltages during exposure. The electrons with high velocity can scatter from the substrate surface and re-enter the resist, known as backscattering. The backscattering effect produces a second, wide spread, Gaussian energy distribution into the resist. A small distribution of electrons with high enough energy scatters back from the sample and is picked up by the backscatter detector, forming the electron image. The backscattering

effect is dependent on the substrate material, which means that dose tests will be required across different samples. The combination of the forward beam energy and the backscattering results in a double Gaussian exposure profile, which is accelerating voltage dependent. Higher voltages reduce the forward scattering effect and therefore the accelerating voltages can be used to broaden the backscatter curve to get a broad and relatively uniform distribution of the backscattered electrons compared to the forward distribution [61, 62].

The proximity effect is caused by the increase of exposure in the resist by electron backscattering [63]. The effective exposure becomes higher in densely patterned regions as the distribution of the backscattered electrons starts accumulating. The proximity effect is shown in Figure 4.7 and shows that features written in the centre of a pattern receive a higher effective exposure. This will have detrimental effects when trying to write small features close to big exposed areas. This problem can be solved by taking into account the backscattering effects and altering the required exposure dose according to pattern size and density. Specialist software by Proxecco [64] is built into the CATS fracture suite and allows for proximity effect corrections according to resist thickness and substrate material.

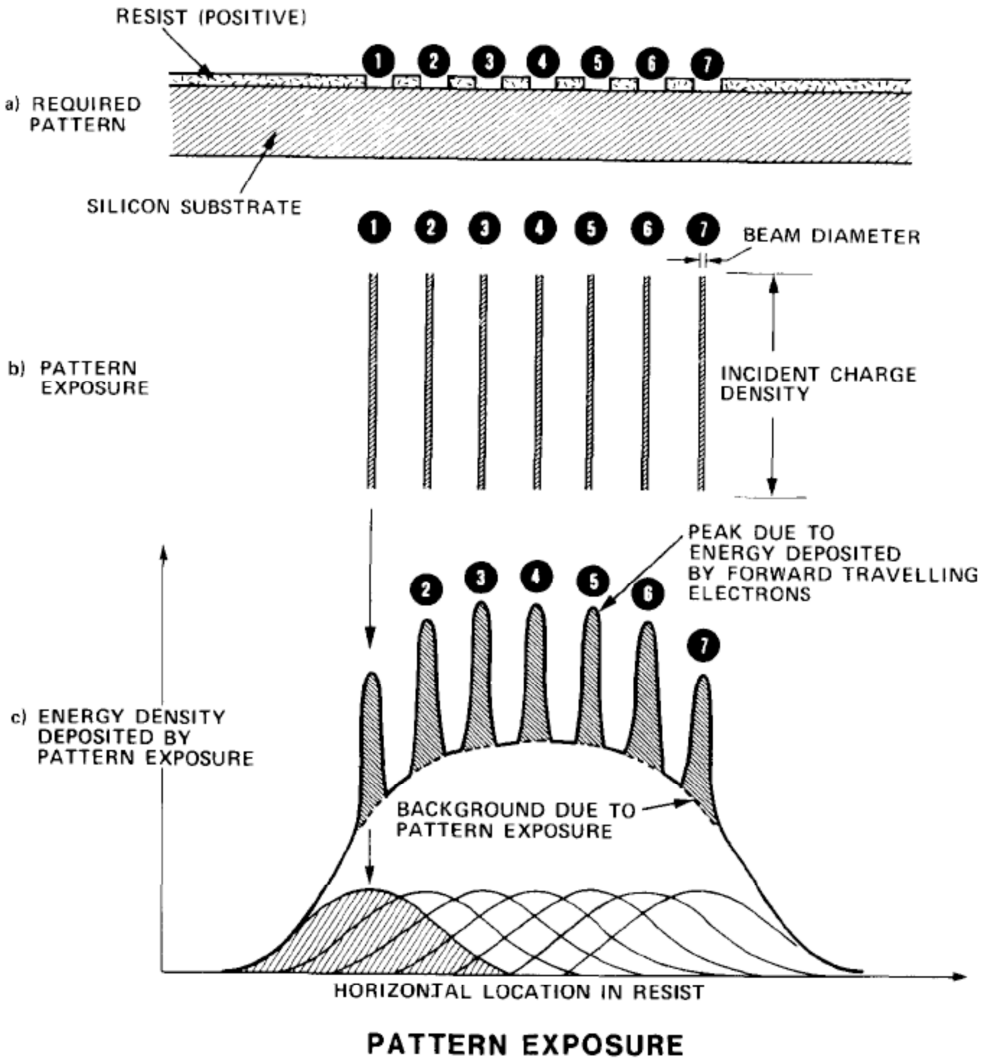


Figure 4.7: Schematic representation of the proximity effects [73].

4.3.2.2 Comparison between photolithography and Electron Beam Lithography

The photolithography tool used at the University of Glasgow is a Suss MicroTec MA6 mask aligner with a UV light source with a wavelength of 400nm. It uses contact lithography, which for an experimental research environment is adequate and masks can be made in house using E-beam lithography. The minimum feature sizes in this work are below 100nm and critical marker alignment will also be required for some process modules. Photolithography has an advantage over e-beam lithography in terms of time needed for processing, as e-beam lithography samples have to be written overnight. Therefore, it seems that it would be beneficial to use the photolithography for less critical lithography features and e-beam lithography for critical feature sizes (<1µm). However, it was chosen to write all the samples using e-beam lithography to obtain a maximum of

processing consistency. The versatility of the e-beam tool also allows making quick changes to the layout.

4.3.2.3 Resist

The pattern definition and minimum feature size strongly depends on the resist used. Different resists have different developer requirements, exposure characteristics and etch resistances. There will always be a trade off between resolution, adhesion, solubility, etch resistance and yield.

The solubility of the resist depends on the developer, development time and the temperature. The exposure dose is dependent on the resist sensitivity and thickness and to a lesser extent to the actual development process. The etch resistance and resist sensitivity is determined by the polymer density or molecular weight of the resist [65]. The resist will be less sensitive to an exposure dose when there is an increased molecular weight. This is due to the increased number of scission events needed for total exposure. The resolution of the resist is also determined by the molecular weight [66].

The resist used throughout this work is poly-methyl methacrylate (PMMA). The advantage of this resist is that it is easy to process, it is available with various molecular weights and has excellent resolution (<100nm) [66]. The developer used is a methyl isobutyl ketone (MIBK) or methyl ethyl ketone (MEK) [67] and isopropyl alcohol (IPA) solution.

4.3.2.4 Pattern transfer

There are two different kinds of pattern transfer: additive and subtractive. Additive patterning is used to deposit material onto lithographically exposed areas in the resist. Subtractive patterning is based on the removal of material of lithographically exposed areas. Either pattern transfer process can potentially affect the underlying semiconductor material. In the case of additive patterning, there could be a thin layer of resist present between the deposited material and the substrate and in the case of subtractive patterning, the etch process can damage the substrate material. These changes can affect the electrical properties and have to be taken into account when developing new process modules.

An example of an additive patterning process is the lift-off technique. The lift-off patterning relies on an overhung resist profile using a double layer of positive resist, as shown in figure 4.8. The profile creates a discontinuity in a uniformly deposited metal film. The bottom layer of the resist bi-layer is more sensitive with a lower molecular weight. Both layers are exposed to an identical dose, resulting in a larger development area

for the low molecular weight resist. This creates an undercut profile resulting in the discontinuity in the deposited metal. The exposed resist sidewall can then be dissolved using a solvent, in most cases acetone, and the metal layer on top of the resist lifts off. The metal pattern on the substrate defined by the exposed windows is then left behind on the substrate. To obtain a large enough exposed resist area, the bottom layer thickness has to be at least as large as the metal thickness.

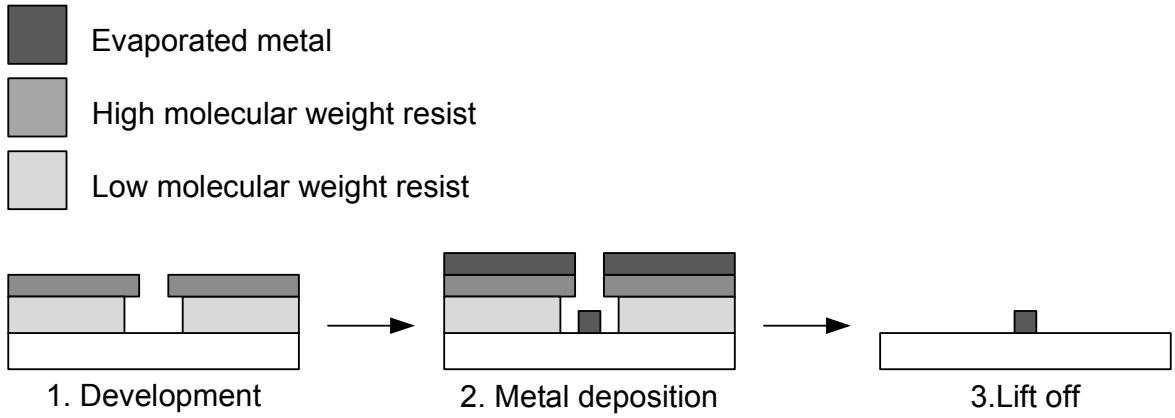


Figure 4.8: Schematic representation of lift-off technique

Subtractive patterning uses either a dry or a wet etch to remove uniformly deposited material from the substrate. A wet etch technique is attractive for large area feature sizes, but ineffective for small feature sizes described in section 4.5. Subtractive patterning is most commonly used after the deposition of refractory metal films such as tungsten and molybdenum, as the metals are uniformly deposited. The metal layer then covers the sidewalls of the resist undercut profile preventing the developer to dissolve the resist and metal lift-off to take place.

4.4 Plasma processing

Plasma processes can be used for either etching or dielectric deposition. The processes are dominant in a great number of device fabrication flows and the different techniques used will be reviewed in the following section. A number of factors have to be considered when comparing different etch processes of dielectric, metal or semiconductor material.

- Profile: There are two different types of etches resulting in more sloped or vertical etch edge profiles. An isotropic etch removes the material at the same rate in any direction while an anisotropic etch has a preferential etch direction.
- Selectivity: The removal of one material while not affecting another is called

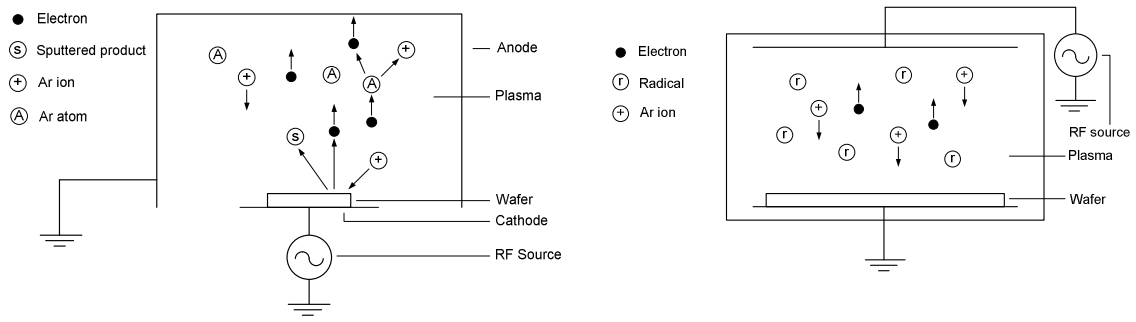
selective etching. This allows for etch stops to be incorporated into the device processing.

- Damage: The detrimental effects of altering inadvertently the underlying semiconductor material due to the plasma exposure. This affects the electrical properties of the semiconductor material.
- Etch speed: Time required to complete an etch process.
- Repeatability: Processing consistency over a large number of samples is required.

Plasma based etching techniques are also referred to as dry etch material removal, as there are no liquids involved in the process. The dry etch process most commonly involves physical sputtering, a gaseous chemical reaction or a combination of both.

4.4.1 Physical sputtering

The physical sputtering process is based on a non reactive process, where atom species bombard the surface of the substrate. The atom species are usually energetic ions from a plasma. To prevent chemical reactions between the substrate and the plasma, inert gases such as Ar are used. An example of physical sputtering is described using an RF-source and Ar ambient plasma, as shown in Figure 4.9a.The plasma is formed by electron initiated avalanche multiplication induced by the RF source in an Ar ambient. The negative period of the RF bias will then accelerate the charged Ar ions towards the substrate. When an Ar ion collides with the surface, the momentum of the ion is big enough to break bonds and material is ejected from the surface. The etch rate of a physical sputtering process is dependent on the voltage bias of the RF source, the substrate material and the ion density. Physical sputtering results in an anisotropic etch due to the low chamber pressure and the corresponding long mean free path. The process is non-selective and produces near vertical profiles. The disadvantage of the physical nature of the process is that the electrical damage can be problematic in the substrate. The relatively large energies required can cause the ions to penetrate into the substrate, hence altering its electrical properties. The material ejected from the surface is not absorbed by the process and this can lead to non ideal etch profiles with hourglass, trenched or redeposition effects. For this reason, the physical sputtering process is not suitable for a well controlled processing environment.



a) Physical sputtering **b) Plasma etching**

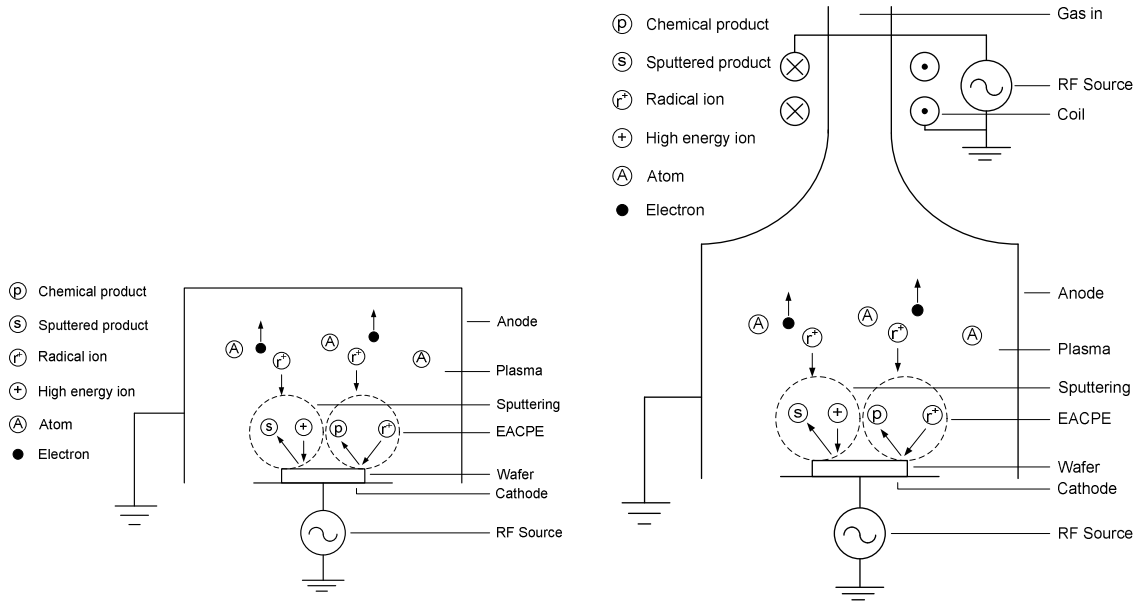
Figure 4.9: Schematic representation of basic dry etch techniques

4.4.2 Plasma etching

Where sputtering is driven by physical removal of the surface of the substrate, plasma etching in contrast, is a chemical process. The plasma supplies neutral radical species, which diffuse to the surface of the substrate with random velocities and cause a chemical reaction. For example, a reactive plasma etch can be used to remove a polymer resist. In this case, ozone plasma reacts with the hydrocarbon resist producing volatile products, which are removed from the etch chamber by pumping. There are different tool configurations, such as a barrel asher and a parallel plate ashing system, shown in Figure 4.9b.The barrel asher features a perforated earthed shield to protect the substrate from high energy positive charged species, which are potentially damage inducing. The chemical nature of the plasma etch and relatively high pressures results in an isotropic etch profile.

4.4.3 Reactive ion etching

Reactive ion etching (RIE) combines physical sputtering and plasma etching by replacing the neutral gas in a sputtering system by a reactive gas. The ions formed by the plasma then contribute to the etch in two forms. The high energy ions collide with the sample surface and bombard the surface causing a sputter product to eject. The reactive radical ions diffuse to the surface with sufficient energy to activate chemical plasma etching (EACPE) and hence react with the substrate. The chemical product after reaction is often volatile and can be extracted limiting redeposition. Figure 4.10a shows a schematic of the RIE process and equipment.



a) Reactive ion etching **b) Inductively coupled plasma etching**

Figure 4.10: Schematic representation of RIE and ICP dry etch techniques

Etching small critical dimensions requires anisotropic etches as the minimum feature size will be degraded by the undercutting. The mean free path of the ionised species increases the anisotropic etch profile and therefore low pressure plasma is required. The etch rate is controlled by high energy and reactive radical ion concentration and RF bias. Low plasma pressure will then result in increased etch times. Increasing the RF bias is unattractive, as the high energy ions cause too much damage in many applications. The inductively coupled plasma (ICP) technique was developed to allow independent control of the density of the plasma and the pressure in the processing chamber, as shown in Figure 4.10b. The technique uses one RF source to control the built in potential to accelerate the high energy ions and a second RF source to control the density of the plasma. The independent control of the plasma density and ion energy allows for fast anisotropic etches in a low pressure environment. However, the RIE etch induces damage due to the exposure to plasma even in a low pressure environment [77].

4.4.4 Ion gun etching

Ion gun etching is a form of physical sputtering. The difference between plasma and ion gun etching is that the ion gun uses an external source to accelerate the high energy ions towards the surface of the substrate. This allows for a large bias source to be applied, which results in very aggressive etching. The operation of a D.C. Kaufman-type ion gun is described in Figure 4.11. As the ion gun process is non reactive an inert gas is used in the

sample chamber, which in this case is Ar. The operation pressure is relatively low (0.4 to $4x10^{-2}$mTorr), resulting in an anisotropic etch profile. The principle of operation is to generate electrons by thermal emission. This is done by running a current through a cathode with a tungsten filament. The electrons are then accelerated towards an anode (V_{dis}), which is in an Ar environment. The Ar plasma is then ignited by electron initiated avalanche multiplication releasing Ar ions. The beam voltage (V_{beam}) accelerates the Ar ions towards the substrate through the screen grid. The Ar ions are further accelerated through the negatively biased (V_{acc}) accelerator grid. This stops neutraliser electrons from returning into the positive screen grid. The neutraliser, consisting of another tungsten filament, emits electrons to the positively charged Ar ion beam to stop the substrate from charging.

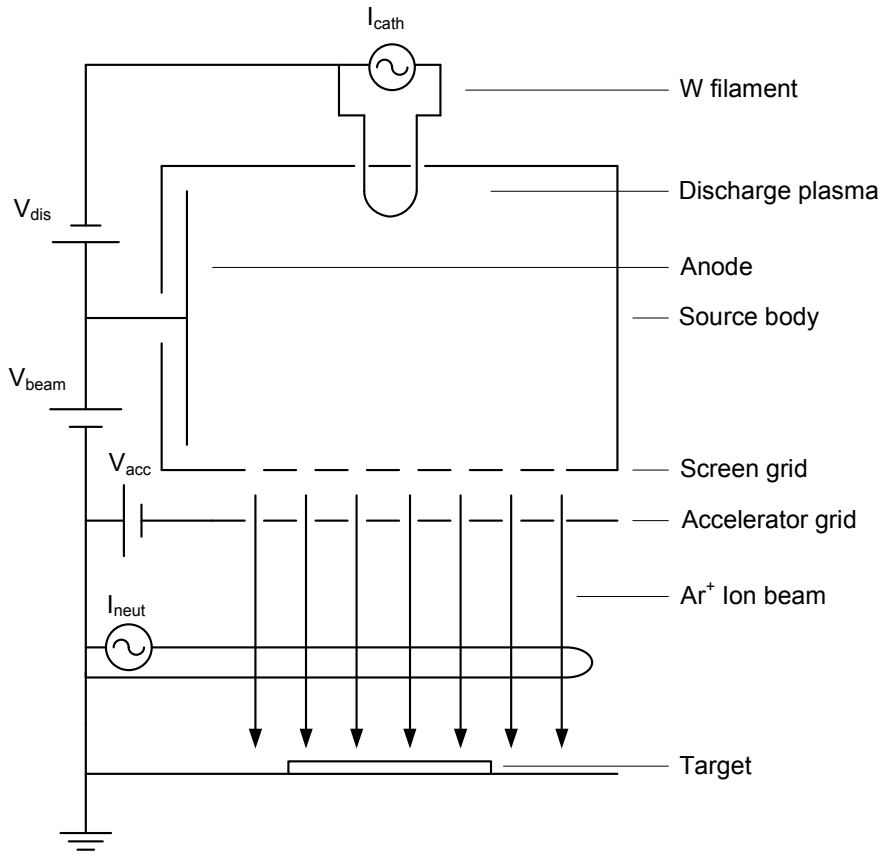


Figure 4.11: Schematic representation of an ion gun dry etch system

The density and the energy of the ion beam determines the etch rate. The beam current (I_{beam}) controls the density of the ion beam, which is dependent on the plasma density. The plasma density is dependent on the pressure of the Ar gas and can be controlled by the cathode current (I_{cath}). The energy of the individual ions in the ion beam is predominantly determined by the beam voltage (V_{beam}). Higher beam voltages will then result in higher

etch rates but will also increase the levels of damage in the semiconductor substrate. The ion gun is therefore not a suitable technique when limited levels of processing damage are required. Similar to the plasma sputtering technique, the ion gun technique also suffers from redeposition. A significant proportion of the ejected substrate material is then redeposited on the surface of the substrate. Some redeposited material is then re-sputtered, but since the etch profile is anisotropic there is a build-up of redeposited layers on both the etch sidewalls and the mask leading to non-ideal effects [68,69]. One of the e-beam evaporator metal deposition tools, discussed in section 4.5, features an in-situ ion gun, which allows for etching prior to metal deposition without having to break the vacuum.

4.4.5 Dielectric plasma deposition

Plasma processes can also be used for the deposition of thin films, in particular dielectrics, on substrate material. The MOSFET device process incorporates thin deposited dielectric films as spacers to separate contacts, insulating layers to form barriers or capacitors or as protective layers to protect the devices from further processing damage.

Chemical Vapour Deposition can deposit dielectrics, but it requires elevated temperatures comparable to the original material growth [70]. The elevated temperatures can cause damage to the underlying epitaxially grown semiconductor layers and to the quality of the oxides grown by MBE. The solution is to deposit the dielectrics using a plasma, known as plasma-enhanced chemical vapour deposition (PECVD).

The fundamental principles of PECVD are similar to plasma etching by exposing a gaseous mixture with reactants to an energetic plasma. The energy of the plasma provides the necessary activation energy, rather than the increased substrate temperature. Controlled deposition conditions can then be developed to deposit dielectrics on a sample surface with fewer damaging effects compared to CVD. A number of dielectrics can be deposited using PECVD, but only a Si_3N_4 dielectric is used in this work. In this case, silane (SiH_4) gas and either gaseous nitrogen or ammonia provide the Si and N components resulting in following reaction:

$$3SiH_4 + 2N_2 \rightarrow Si_3N_4 + 6H_2$$

The hydrogen by-product is likely to be present in the Si_3N_4 film and together with other possible contaminants the physical properties such as dielectric constant, refractive index, permeability and stress might change as a result [70]. The impurity of the PECVD deposited dielectric films potentially poses a problem when ideal properties of the dielectric films are required. The large energies involved to form a plasma in a PECVD

technique can damage the substrate making this technique unsuitable when a minimum amount of processing damage is required.

The PECVD technique can be improved by using a separate coil, with an RF source, to generate and control the plasma. This technique is known as inductively coupled plasma chemical vapour deposition. In case of Si_3N_4 deposition, a high density nitrogen plasma in the upper portion of the chamber is ignited by the inductively coupled coil. The silane is then introduced below the coil and reacts with the nitrogen plasma forming a high density of both species. These are consequently deposited on the surface of the substrate with low power. The low power reduces the energy of the ions compared to PECVD reducing potential damage to the substrate. The high density plasma allows a more efficient generation of highly reactive radicals, which allows a lower processing temperature. As a result, the concentration of reactive elements is relatively higher than the residual or secondary contributions. Higher quality and purity films can then be achieved using ICP-CVD, which are compatible with III-V MOSFET processing without damaging the underlying epitaxially grown layer structure. The tool used in this work for Si_3N_4 deposition is a Plasmalab System-100 ICP-CVD tool by Oxford Instruments.

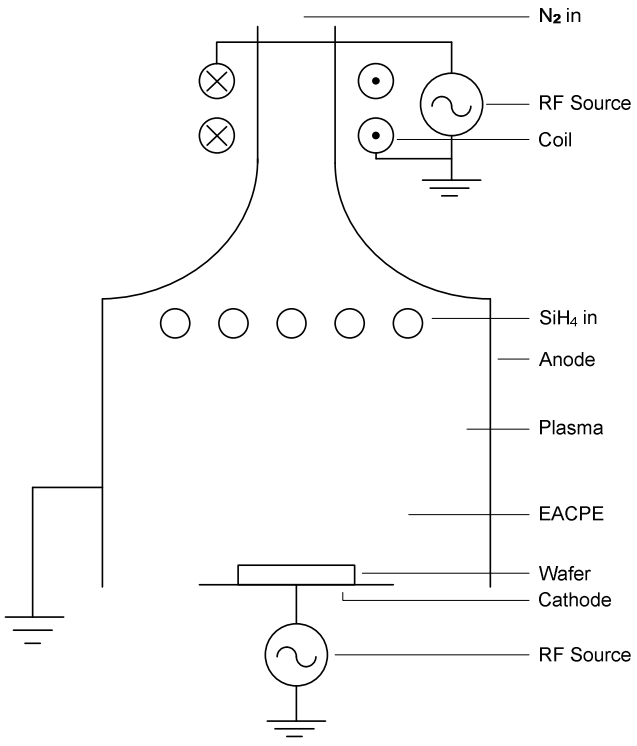


Figure 4.12: Schematic representation of an ICP-CVD deposition tool

4.4.6 Wet etching

The simplest method of removing material in a semiconductor device process is to use a liquid chemical etchant. There are wet etches for numerous materials and applications and are often used in a III-V MOSFET device process as oxide etches, isolation etches or gate recess etching when a HEMT like device structure is used chapter 3.7.

Wet etching is a chemical process, which can be split in three steps: a reactant is transported to the surface of the substrate, then a chemical reaction takes place between the reactant and the substrate and finally the product is transported away from the substrate [71]. The transport is driven by diffusion and if the transport is the etch rate limiting factor, then the process is diffusion limited due to the small diffusion coefficient in liquids. The etching process can in this case be quickened by agitating the sample or etch solvent. When the reaction is the etch rate limiting factor, then the process is reaction rate dependent. Increasing the temperature or concentration levels can then speed up the etching process.

The chemical process only affects the surface of the substrate and causes little or no damage in the substrate itself. The wet etch generally proceeds in all directions at the same rate and has therefore strong isotropic tendencies. The etch direction can then not be governed by process control as is the case in dry etch. In addition, the etchant solution can undercut the mask and etch the underlying material, resulting in an increased feature size. However, the etch direction can be dependent on the crystal orientation of the semiconductor substrate [71]. The morphology of a wet etched surface depends on the reaction rate. A slow reaction rate produces a smoother surface while a fast reaction rate causes gas bubbles to form at the surface of the substrate. These bubbles are the product of rapid gas production from the chemical reaction and affect the surface morphology and uniformity [72]. The by-products formed by the etching process can potentially re-deposit on the etched surface. This could lead to potential contamination or increased defect densities.

The III-V MOSFET device process can benefit from selective wet etching in different areas: semiconductor material etches with an etch stop, metal etching and oxide etching. An example of a wet etch with an etch stop is the gate recess etch process used with HEMT like structure processing. The process involves a succinic or citric acid and hydrogen peroxide mixture, which reacts with gallium containing layers but not with aluminium containing layers. The level of selectivity then depends on the aluminium

concentration. A layer structure with a sufficient amount of aluminium can then be used as an etch stop. Metals such as titanium can be etched using hydrofluoric acid and oxides can be etched using hydrochloric acid.

The III-V MOSFET device fabrication process also requires non-selective etching for the mesa isolation of devices. A wet etch process for III-V semiconductor material is more complex due to the zinc-blende crystalline structure. The principle of the wet etch is to first oxidise the semiconductor surface and then etch the oxide [71]. The surface can be oxidised with diluted hydrogen peroxide forming an oxide on the surface and can be etched using an acid, which is compatible with hydrogen peroxide such as orthophosphoric acid or sulphuric acid. The dilution ratio between the reactants and water will determine the etch rate. The etch process is electrochemical and the presence of metals can alter the etch rate. This has a detrimental effect on the uniformity of the etch across the wafer.

Advantages of wet etch over dry etch:

- Damage: Low or very little damage is introduced in the substrate.
- Speed: High etch rates can be achieved dependent on the material and etchant.
- Cost: Low running costs as wet etch equipment is inexpensive compared to dry etch. Most wet etches can take place in either a glass or plastic beaker.

Disadvantages of wet etch:

- Capillary action: Penetration of resist underneath the mask, which can lead to different feature sizes and increased edge roughness.
- Poor process control: Etch temperatures, sample solutions and agitation are difficult to reproduce in an experimental environment leading to poor repeatability.
- Contamination: Potential re-deposition of by products on the surface of the substrate.
- Waste: The by-product of a wet etch is often a hazardous liquid.
- Bubble formation: Gaseous reactions form bubbles, which lead to non-uniformity.

A wet etch process is preferred over a dry etch process when low cost, high throughput and low damage are paramount. However, when a vertical etch profile with good reproducibility is required, then dry etch is the preferred etch method.

4.5 Metallisation

There are principally three different methods of depositing metal on a substrate: plating, sputtering and metal evaporation. Metal plating is generally used to deposit thick layers and with relaxed process tolerances. In III-V device processes the most common metal used is gold to form interconnects, bond-pads or is used in backside processes. The resolution of plating is poor and has not been used in this work however it is a cost effective method for depositing thick layers of metal.

4.5.1 Metal Evaporation

Evaporation techniques are based on heating up a source to a temperature where the material starts vaporising. The vaporised material is then deposited on the sample and cools down forming a thin film. Thermal evaporation can either be achieved by heating the source with a resistive element or by using an electron beam. Resistive heating takes place by passing a current through a heating element, often made out of tungsten, which heats up a crucible containing the source material. Resistive evaporation has the disadvantage of potential contamination from the crucible if the melting temperature of the crucible is close to the melting temperature of the source material, resulting in a poor film quality. Electron beam evaporation uses an electron beam generated from a cathode to heat up the source material locally. The crucibles are water cooled to minimise contamination. The electron beam is generated by a thermionic emission filament and is accelerated towards the crucible using a high accelerating voltage. The beam is then focussed into a spot on the surface of the source material and the interaction between the accelerated electrons and the source material will cause the material to start heating up and vaporise. The combination of local heating and water cooled sources prevents crucible metal contamination, resulting in a high purity film deposited on the substrate.

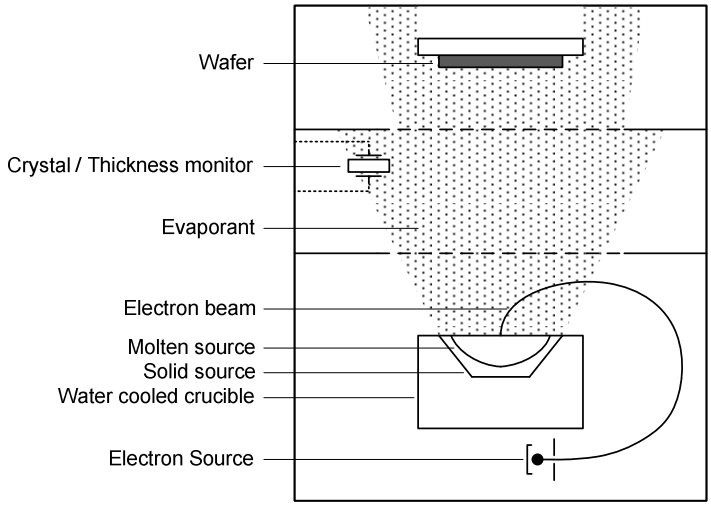


Figure 4.13: Schematic representation of e-beam evaporator

A generic schematic representation of an e-beam evaporator can be seen in Figure 4.13. Most commonly there are two shutters, illustrated by the dashed lines, between the source and the substrate target. The shutter separates the target from the source to allow for the source material to heat up. During the initial stages of the heating process, the flux rate fluctuates and the bottom shutter is opened once the evaporation rate is sufficiently stable. The evaporation rate is monitored, using a quartz crystal whose oscillation frequency reduces as additional layers of source material are deposited. This allows for rate control in a closed loop feedback with the e-beam source power control. Once a predetermined evaporation rate is reached, the top shutter opens and exposes the substrate to the evaporant flux until the desired film thickness is reached.

The evaporation processes take place under high vacuum ($1x10^{-3}$ to $1x10^{-4}$mTorr) in order to create a mean free path of the evaporating flux, which is greater than the distance between the source and the sample. As a result, there is low particle scattering, which leads to a highly directional, non-conformal coating on the sample. A Plassys MEB450 and a Plassys MEB550 were used in this work as evaporation tools. The Plassys MEB 450 features an in situ ion gun, which can be used for dry etching. The source materials present in the evaporation tools are described below:

1. Plassys MEB450: titanium, nickel, nickel/chromium, germanium, gold, palladium, aluminium
2. Plassys MEB550: titanium, nickel, nickel/chromium, germanium, gold, platinum, molybdenum, aluminium

4.5.2 Sputtering

While evaporation requires a source to be heated to produce a flux of gas, sputtering targets make use of a physical plasma process rather than heat. The sputtering process is then similar to a dry etch process, where the plasma bombards the surface of a target containing a source metal. The plasma is formed using an inert gas (normally Argon) and is excited by either a DC or RF source. The target source is negatively biased and the plasma sputters neutral atoms of source material away from the target towards an anode, where the neutral atoms are deposited on the sample. Since a plasma is required, the working pressures of sputtering systems are relatively high (around $1x10^{-1}$mTorr). Consequently, most atoms collide before reaching the sample resulting in a large spread of incident angles. The deposited metallic coating is therefore more conformal and as a consequence lift off techniques cannot be used. Sputtering of metallic films usually requires a subtractive process. The advantage of a sputtering tool is that materials with a relatively high melting point such as tungsten can be deposited. Also, alloys and compounds such as titanium-tungsten can be deposited in a single step. The sputtering tool used in this work is a Plassys MP900S.

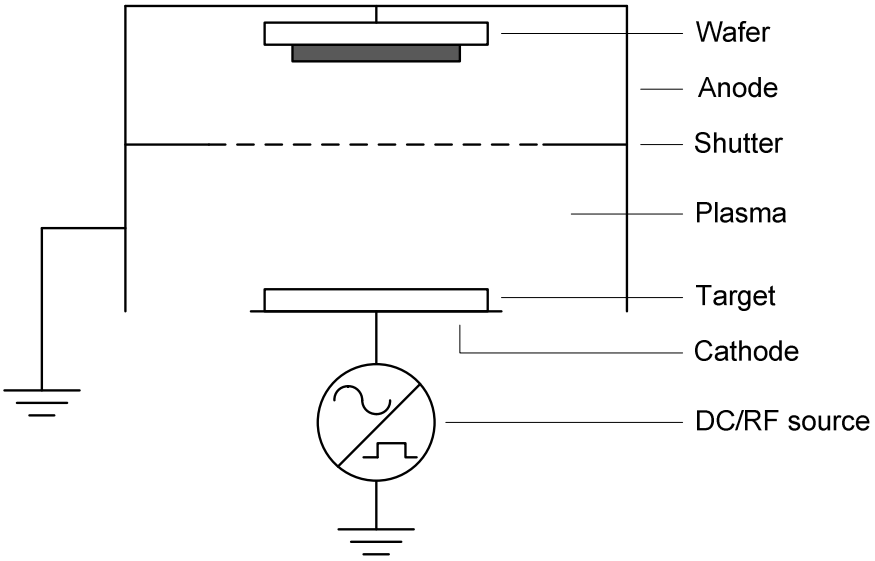


Figure 4.14: Schematic representation of a sputter system

4.5.3 Metal deposition technique comparison

The choice between sputtering and evaporation techniques is sometimes limited because of processing constraints. But when either sputtering or evaporation techniques can be used the relative advantages of both and their patterning technique must be evaluated.

Advantages of electron beam evaporation and lift-off:

- Reduced damage: The dry etch and plasma of the sputtering both introduce damage into the substrate.
- Cost: Dry etch and sputter tools are relatively expensive to purchase and to run compared to the evaporation tool.

Advantages of sputter deposition and subtractive dry etch:

- Material choice: Materials with high melting points, often refractory with good dry etch properties, cannot be used in e-beam evaporation tools.
- Scaling: The uniformity of the metal film over a large area is superior when using sputter deposition.
- Adhesion: Sputtered films have better adhesion compared to e-beam deposited films.
- Control of film properties: More parameters can be adjusted when sputtering a film, which controls the stress, grain, resistivity and step coverage of the metal.
- Compound deposition: Stoichiometric films that would dissociate during evaporation can still be deposited using sputter deposition.
- Yield: Due to the better adhesion and controllability, plasma processes have a better reproducibility and yield over e-beam evaporation.

Sputtering and dry etch has a number of advantages over e-beam evaporation and lift off. However, the low cost and the ease of processing makes the latter a more suitable solution in an experimental environment. Ohmic contact formation also requires a low damaging process as any out-diffusion of doping leads to an increased resistance. This is the most important factor why e-beam evaporation and lift-off have been preferred over sputtering/dry etch. Also an e-beam evaporator can still blanket deposit a metal, which can be dry etched afterwards if resist residue is an issue.

4.6 Summary

The fundamental technologies required to build MOSFET devices have been discussed in this chapter. This included the semiconductor growth techniques, lithography techniques, etch techniques and dielectric and metal deposition techniques. The semiconductor growth technique described the formation of a MBE grown GaGdO dielectric and an ALD grown Al_2O_3 dielectric, which are two types of gate dielectrics used in this work. The merits and disadvantages of the various technologies have been discussed. In particular the different etch techniques and metal deposition techniques, which will be crucial in forming low resistance ohmic contact, which will become clear in later chapters.

5 Characterisation and metrology

5.1 Introduction

The development of MOSFET devices relies on accurate characterisation and metrology in order to understand the operational behaviour of the various parameters and underlying phenomena involved. The device performance has to be able to be benchmarked against existing MOSFET devices of various technologies. Therefore, it is crucial that the characterisation and metrology used corresponds to what is commonly found in the literature.

The main physical parameters defining the performance of a MOSFET device are: the metal semiconductor interface for source/drain contacts, the channel material and the quality of the oxide. This chapter will show some basic measurement techniques for the channel material, the oxide quality and overall device performance. It will show some more in depth detail of the characterisation of the metal semiconductor interface, as this thesis focuses on the ohmic contacts to III-V MOSFETs.

5.2 Ohmic contacts theory

To be able to measure the physical properties of the ohmic contacts to semiconductors, a clear definition of the term 'contact resistance' and how it can be measured, needs to be established. Over the years, different terminologies have been used in the literature to describe the properties of an ohmic contact: contact, resistivity, contact resistance, specific contact resistivity, specific contact resistance, and specific interface resistance. Because of the different terms used, there exists some confusion on the definition of these ohmic contact properties, which will be explained in more detail.

There are several methods to determine the contact resistance, which are based on various models and use different simplifications. The measurement methods will be divided up in two-, three- and four-terminal resistor methods. Each of the different measurement methods has certain drawbacks and limits, which will be described in more detail.

5.2.1 Specific interface resistivity

The main goal of an ohmic contact measurement is to obtain information on the metal to semiconductor interface, called the interface resistance. As seen in the chapter 3.6, a metal semiconductor interface forms a Schottky barrier. Given the theoretical physical parameters for a certain semiconductor material, the Schottky barrier height and width can

be simulated [97,98]. However, this is an ideal theoretical approach where parasitic contributions from the semiconductor material are not taken into account. The specific interface resistivity (ρ_i) can therefore be determined theoretically, but is not equal to a particular measured quantity. This is due to the fact that a metal semiconductor interface is never perfect, there is always a small amount of damage and residue from processing on the interface layer. The specific interface resistivity (ρ_i) is found by the current density (J) flowing through a metal semiconductor interface for a certain voltage drop across the barrier (V) (Equation 5.1).

$$\rho_i \cong \left(\frac{\delta J}{\delta V}\right)^{-1}_{V=0} \tag{5.1}$$

The main mechanisms of current transport have been previously described in chapter 3.6.3: thermionic emission (TE), thermionic field emission (TFE) and field emission (FE). The expression for the specific interface resistivity depends on the current transport mechanism [3] and can be shown for each case as:

(TE)

$$\rho_i \propto \exp\left(q.\frac{\phi_{Bn}}{k.T}\right) \tag{5.2}$$

(TFE)

$$\rho_i \propto \exp\left\{\frac{4\pi\sqrt{m^*\varepsilon_0\varepsilon_{r,s}}}{h}\left(\frac{\phi_{Bn}}{\sqrt{N_D}}\right)\tanh\left[\frac{qh}{4\pi kT}\sqrt{\frac{N_D}{m^*\varepsilon_0\varepsilon_{r,s}}}\right]\right\} \tag{5.3}$$

(FE)

$$\rho_i \propto \exp\left\{\frac{4\pi\sqrt{m^*\varepsilon_0\varepsilon_{r,s}}}{h}\left(\frac{\phi_{Bn}}{\sqrt{N_D}}\right)\right\} \tag{5.4}$$

The value of the specific interface resistivity is then determined by the potential barrier height (Φ_{Bn}), doping concentration (N_d), temperature (T) and the semiconductor material properties (m^*).

The equations show that thermionic emission is temperature dependent, field emission has no temperature dependency and the thermionic field emission does not have a linear variation with either temperature or doping concentration.

The specific interface resistivity is mainly used when ohmic contacts are simulated, in practice the specific contact resistivity is the most frequently used term for the ohmic behaviour of a metal semiconductor interface.

5.2.2 Specific contact resistivity

The specific contact resistivity (ρ_c) is also a parameter to indicate the resistance of a metal semiconductor interface similar to the specific interface resistivity. Where the two differ, is that the specific interface resistivity is a theoretical value and the specific contact resistivity is an extracted value from an ohmic contact measurement. The specific contact resistivity includes the various parasitic contributions coming from processing such as: foreign contaminants and structural defects on the semiconductor surface. The non ideal characteristics of a Schottky diode can be simulated using a 'ideality factor' (n) [79, 80], as explained in section 3.6, and thus bringing the simulated value of specific interface resistivity in line with the measured specific contact resistivity. The specific contact resistivity is most commonly expressed in $\Omega.cm^2$ and is used as a benchmark to indicate the quality of an ohmic contact. The key figure of merit varies over the years and is technology dependent. The tendency is to achieve a value below $10^{-8}\Omega.cm^2$ according to the ITRS [1] roadmap for future CMOS devices.

The specific contact resistivity is often referred to as specific contact resistance. A resistivity value is expressed per unit area and is a physical property of a substance, in this case the metal semiconductor interface. Resistance is a property of an object given certain dimensions and is therefore the incorrect term when describing the potential drop over a metal semiconductor interface.

5.2.3 Contact Resistance

The definition of contact resistance originally proposed by Berger [7] was the difference between the measured value of the actual contact and the value of the ideal contact. The contact resistance was a series resistance to the ideal contact resistance. However, for measurement purposes it was more convenient to combine these.

The contact resistance is found by measuring the total resistance over two separate ohmic contacts and excluding the sheet resistance of the semiconductor substrate. This results in the contact resistance of two ohmic contacts. The contact resistance is the value for a single ohmic contact and is then found by dividing the previous result by two and commonly expressed in Ω.mm. Because of the fact that the contact resistance is a direct result from a measurement, there is no direct relation to the physical aspects of the ohmic contact unlike the specific contact resistivity. This limits the use of the contact resistance as a quick and easy guideline for some basic ohmic contact characteristics. There exist various models to extract the specific contact resistivity from the contact resistance, which are used by

different ohmic contact measurement methods.

5.2.3.1 Berger model (simple)

The simplest model [7] assumes there is a perfect vertical current flow in the interface layer and therefore has a uniform current distribution. The only parameters used in this model are the contact resistance, the specific contact resistivity and the contact area. The extraction of the specific contact resistivity is straightforward because of the uniform current distribution:

$$\rho_c = R_C.A \qquad (5.5)$$

The assumption of vertical current flow is only valid when the resistance of the metal semiconductor interface is significantly larger than the semiconductor bulk resistance. Progress through ohmic contact research has made this model redundant. The specific interface resistivity cannot be determined accurately from the specific contact resistivity using measurement methods based on this model.

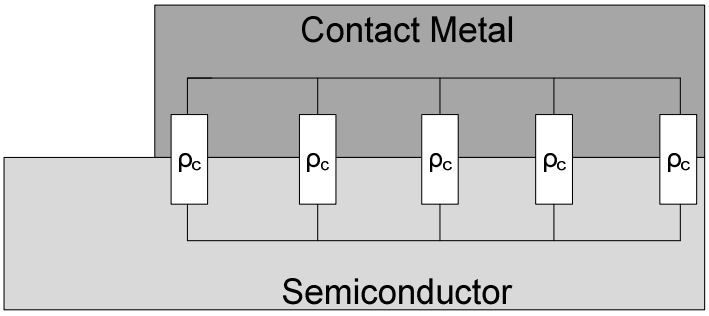


Figure 5.1: One dimensional ohmic contact model proposed by Berger [7]

5.2.3.2 Berger model (extended) [7]

Incorporating the semiconductor bulk sheet resistance recognises that the main part of the current flows parallel to the metal semiconductor interface. The current flow in the interface layer has no longer a uniform current distribution and causes current crowding effects to take place. Current crowding effects are caused by two main mechanisms:

1. The sheet resistance of the semiconductor substrate underneath the contact is higher than the sheet resistance of the metal layer.
2. The specific interface resistance is comparable to or larger than the sheet resistance of the semiconductor substrate underneath the contact.

The Berger model however does not take the sheet resistance of the metal into account and assumes that the sheet resistance of the diffusion area underneath the contact is equal to the

sheet resistance of the bulk semiconductor. The equivalent electrical circuit representing the model used is shown in Figure 5.2.

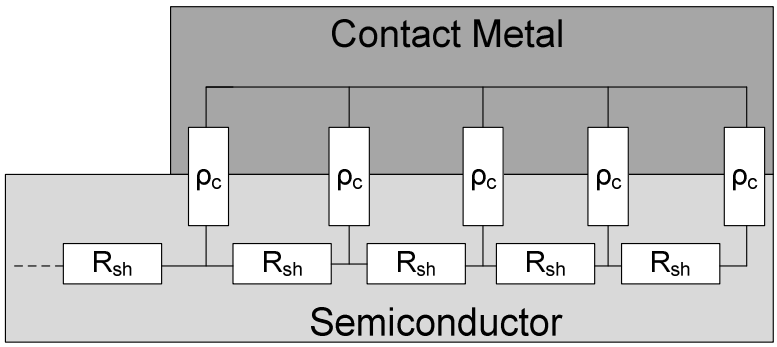


Figure 5.2: Two dimensional ohmic contact model proposed by Berger [7]

The mathematical analysis [7, 88] shows the dependency of the contact resistance on the current crowding effects and this limiting factor should be taken into account when measuring ohmic contacts. The current crowding effects start to take place when the contact length is smaller than two times the transfer length L_T. The transfer length is based on the distribution of current along the metal semiconductor interface. The distribution of the current density is not linear with distance and most of the current flows near the edge of the contact with an exponential decrease away from the edge Figure 5.3.

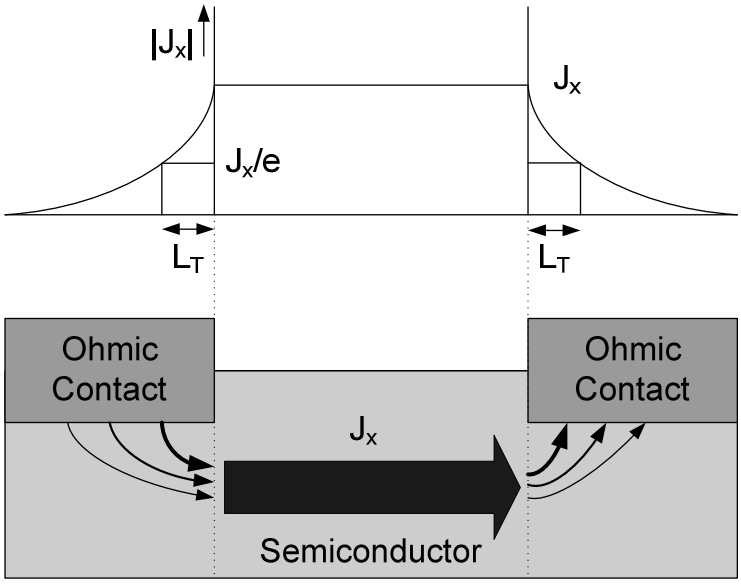


Figure 5.3: Current flow density in semiconductor using planar ohmic contacts

The equation for the transfer length shows that the current crowding effects are depending of the sheet resistance R_{sh} and specific contact resistivity ρ_c.

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{5.6}$$

$$R_C = \frac{R_{sh}.L_T}{W} . \coth\left(\frac{d}{L_T}\right) \tag{5.7}$$

d: Contact Length

W: Contact width

The specific contact resistivity can then be extracted by combining equation 5.6 and 5.7 using the sheet resistance and contact resistance values.

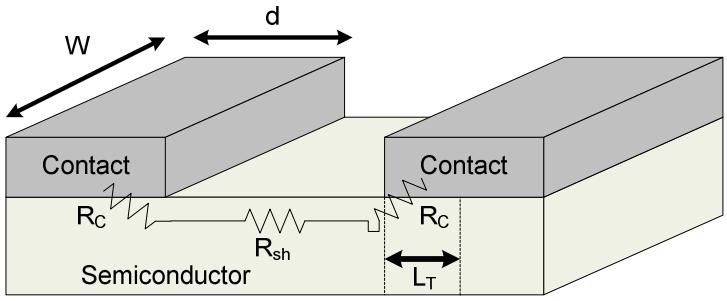


Figure 5.4: Schematic impression of a planar ohmic contact

5.2.3.3 Reeves and Harrison [81]

The bulk semiconductor sheet resistance does not necessarily correspond to the sheet resistance underneath the ohmic contact. The modification in sheet resistance beneath the ohmic contact can have multiple causes: alloying/sintering, polysilicide like ohmic contacts, processing induced damage and the thickness of the active semiconductor layer. Hence a more detailed model for ohmic contacts is required.

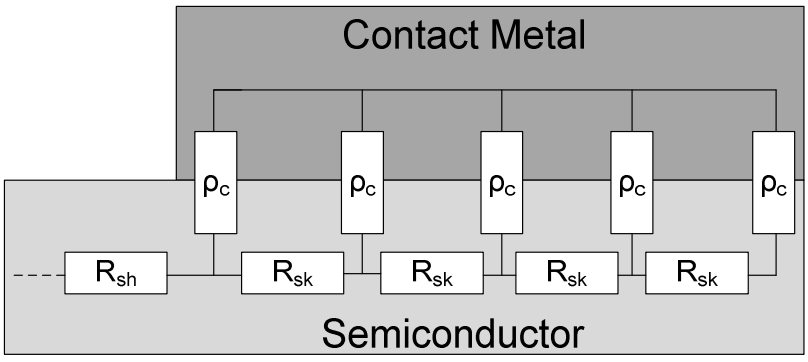


Figure 5.5: Two dimensional ohmic contact model proposed by Reeves and Harrison [81]

The sheet resistance underneath an ohmic contact has the symbol R_{sk} and has a similar expression as the sheet resistance in Ohm/sq. The equivalent electrical model is represented in Figure 5.5 and the corresponding mathematical equations are shown in equations 5.8 and 5.9.

$$L_T = \sqrt{\frac{\rho_c}{R_{sk}}} \tag{5.8}$$

$$R_C = \frac{R_{sk}.L_T}{W} . \coth\left(\frac{d}{L_T}\right) \tag{5.9}$$

The specific contact resistivity can be found by combining equations 5.8 and 5.9. However, the sheet resistance value underneath the contact has to be known in order to extract the specific contact resistivity according to this model.

5.2.3.4 Scott model

The model proposed by Scott et al. [82] was originally used to predict the effect of silicided diffusions on the performance of ohmic contacts. This is the most complete model and takes the sheet resistance of the silicide on top of a diffusion layer into account. However, the electrical equivalent model for an ohmic contact used in this thesis, is slightly different. So far, in previous models the sheet resistance of the metal of the ohmic contact was not taken into account. The metal sheet resistance is far smaller than the sheet resistance underneath the contact and should only play a minor role. Novel technologies allowing to scale the metal layers further and increasing doping concentration might alter the balance and a model that incorporates the metal sheet resistance will allow for more accurate measurements and simulations of ohmic contacts.

Using the mathematical analysis performed by Scott et al. and adjusting two parameters the electrical equivalent model looks as follows:

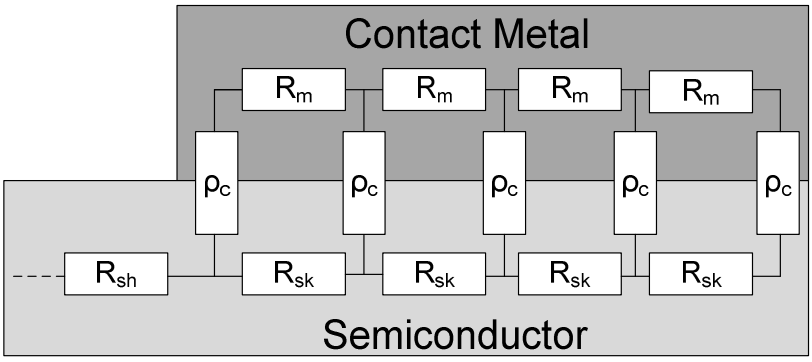


Figure 5.6: Two dimensional ohmic contact model proposed by Scott et al. [82]

The silicide sheet resistance has been replaced by the metal sheet resistance and the diffusion sheet resistance has been replaced by the sheet resistance underneath a contact. The mathematical equations for the transfer length and contact resistance are described as follows:

$$L_T = \sqrt{\frac{\rho_c}{R_{sk}+R_m}} \tag{5.10}$$

$$R_C = \frac{\left(R_{sk}.R_m+\left(R_{sk}^2+R_m^2\right)\right).\cosh\left(\frac{d}{L_T}\right)}{\left(\frac{W}{L_T}\right)(R_{sk}+R_m).\sinh\left(\frac{d}{L_T}\right)} \tag{5.11}$$

In order to extract the specific contact resistivity according to this model, the sheet resistance under the contact and the metal sheet resistance need to be known.

5.2.4 Summary

The extraction of the specific contact resistivity is critical to be able to determine the quality of the ohmic contact accurately. This is critical, as the result of the specific contact resistivity can be compared to a simulated specific interface resistivity and hence extracts the Schottky barrier height. To emphasize the limitations of the different models, due to the assumptions made, a comparison is shown in Table 5.1.

	Assumptions	Limitations
Berger (simple)	- Vertical current flow	- Sheet resistance not taken into account - Current crowding effects cannot be measured
Berger (extended)	- $R_{sk} = R_{sh}$ - $R_{sh} >> R_m$	- Specific contact resistivity will be extracted incorrectly when R_{sk} is different from R_{sh}
Reeves	- $R_{sk}>>R_m$	- Invalid when using highly doped semiconductor material and very thin metal contact layers.
Scott	- 2D model	- Voltage distribution across contact is assumed to be uniform

Table 5.1: Comparison between the different ohmic contact models

The models used in this thesis are the extended Berger model for normal contact measurements and Reeves and Scott model for scaled ohmic contacts. The simple Berger model has not been used, as the extracted data would be too inaccurate and would not allow for a direct comparison with the results found in literature.

5.3 Ohmic contact characterisation

5.3.1 Two terminal resistor

The two terminal resistor structure was originally proposed by Sullivan and Eigler [83] to be able to determine the semiconductor contact resistance. The structure consists of two contacts with a surface area on the top and bottom of a homogeneous semiconductor material (Figure 5.7).

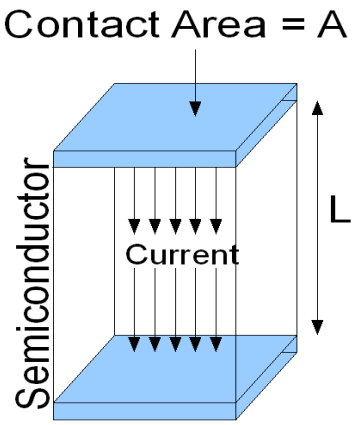


Figure 5.7: Two terminal resistor

The current is assumed to be uniform and vertical when passing through this structure. The model used for this particular measurement method is thus the Berger model (simple). The voltage drop measured over the top and bottom contact will give the total resistance R_T for this specific structure. The total resistance consists of the contact resistance of the ohmic contacts and the resistance of the bulk semiconductor:

$$R_C = \frac{1}{2}.\left(R_T - \frac{R_{sh}.L}{A}\right) \tag{5.12}$$

In order to extract the contact resistance the sheet resistance of the bulk semiconductor would have to be known, because it cannot be extracted from measuring the structure. A different two terminal resistor structure was suggested by Cox and Strack [84] to overcome this issue.

However, in both cases the measurement method can only be used on uniformly doped semiconductors. The semiconductor material used in this thesis has in nearly all cases a non uniform doping profile and layer structure. Together with the assumptions made by the Berger model (simple), this measurement method would be far too inaccurate to study the properties of ohmic contacts.

5.3.2 Three terminal resistor method

The three terminal resistor method is made up of two or more planar resistors, originally proposed by Shockley [85]. Two versions of this method exist: the transfer length method or transmission line model (TLM) and the contact end resistance extraction method. The contact end resistance method allows for a mathematical model to extract the sheet resistance underneath a contact whereas the TLM method is limited to the more simple model, where the sheet resistance underneath the contact is assumed to be the same as the bulk semiconductor sheet resistance.

5.3.2.1 TLM method,

The transmission line model (TLM) test structure is made of many planar contacts with constant widths (W) on non-insulating semiconductor material. The various contacts are separated by spacings, which progressively increase in size. The total resistance of the planar contacts is measured for each spacing and is plotted as a function of spacing size (l1, l2).

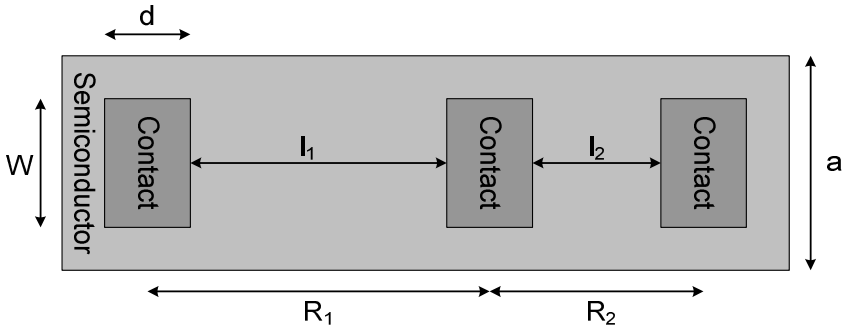


Figure 5.8: Resistor test structure for TLM measurements

The increase in resistance between a larger spacing and a smaller spacing gives an indication of the semiconductor sheet resistance R_{sh}. The sheet resistance is a normalised value expressed in Ω/square. This means that the gap size and contact width have to be normalised when calculating the sheet resistance. When extrapolating the data for a spacing length of zero, the semiconductor sheet resistance is nonexistent and only the resistance of two planar contacts remains. The resistance for one planar contact is called the contact resistance (R_C). The contact resistance is usually normalised for a contact width of 1mm resulting unit expressed in Ω.mm. Further extrapolation of the data, where R_C = 0Ω.mm, allows to find the value of the transfer length L_T, which is used to extract the specific contact resistivity ρ_c, as shown in Figure 5.9.

$$L_x = 2.L_T \tag{5.13}$$

$$R_C = \frac{R_{sh}.L_T}{W} \text{ for } (d \gg L_x) \quad (5.14)$$

$$R_T = 2R_C.\frac{R_{sh}.L_x}{W} \quad (5.15)$$

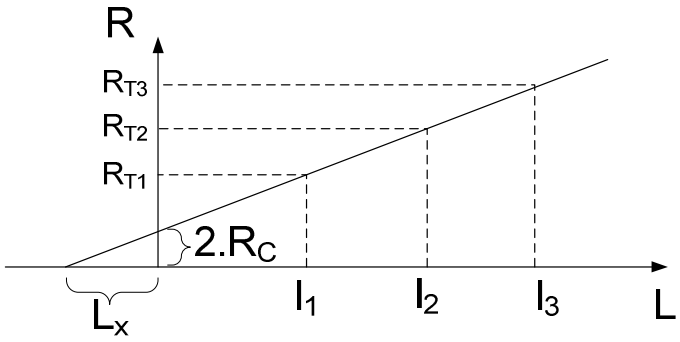


Figure 5.9: TLM extraction method

This measurement method has its limitations. Due to current crowding effects the contact length (d) has to be at least two times bigger than the transfer length of the contact. The resistance underneath the contact should be the same as the semiconductor sheet resistance, however this is not always the case as described by Chang [86]. The resistances of the contacts have to be identical, which in reality might not be true. This has to be taken into account when measuring the correlation between the data and the gap size. The correlation has to be as high as possible and preferably over 99.9%. The last limiting factor is the lateral spreading of the current and the possibility of the edge currents along the contact. This would make the contact width larger electrically and could affect the result. There are two ways to counter these effects: Circular TLM structures or a mesa etch. The TLM measurement method is a quick and easy way to determine contact resistance (R_C), semiconductor sheet resistance (R_{sh}) and specific contact resistivity ρ_c. The simplicity of this measurement method makes it a popular way of determining the ohmic contact quality in literature.

5.3.2.2 CTLM

The Circular TLM structure [87] is based on the TLM principle of planar contacts with various gap spacings (S). From this structure, the different ohmic contact parameters can be determined through the linear relationship between the gap spacings and the planar contacts. Where the circular TLM method differs from the ordinary TLM method, is that there is no mesa etch required to limit the current spreading between contacts. The typical CTLM structure consists of a round centre contact, a ring-shaped gap as a spacing and another larger contact.

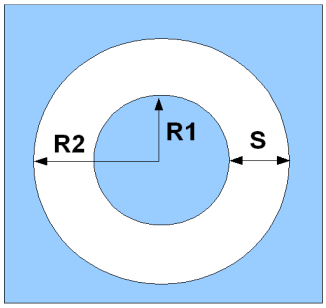


Figure 5.10: CTLM structure

When measuring CTLM contacts, the results of the total resistance over different gap spacings will not be linear. This non linear relationship is due to the changing circular geometry of the contact structures. It can be made linear by using correction factors [87] out of which the contact resistance, semiconductor sheet resistance, transfer length and specific contact resistivity can be determined.

$$R_C = \frac{R_{sh}}{2.\pi.R_1}.(s + 2L_T).c \qquad (5.16)$$

With c being the correction factor:

$$c = \frac{R_1}{s}.\ln\left(\frac{(R_1+s)}{R_1}\right) \qquad (5.17)$$

Although the Circular TLM does not require a mesa etch, it still has most of the same limitations in common with the normal TLM. When implementing the CTLM as a test structure on a sample, the size of the test structure has to be taken into account as it is considerably larger than a normal TLM structure.

5.3.2.3 End resistance

The contact end resistance is defined as a difference between the measurement of the contact resistance R_C for a loaded and unloaded contact [7]. This implies that there is a voltage drop between the outer edges of the ohmic contact when a current is applied to the contact. This is due to current crowding effects [88], which make the current density drop exponentially along the contact. The contact end resistance R_e can be derived from following measurement set-up:

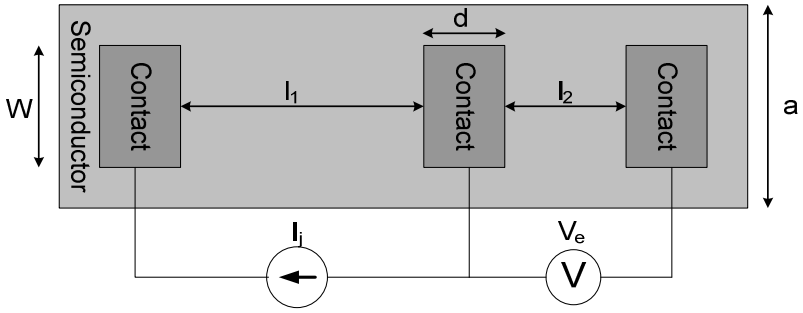


Figure 5.11: Contact end resistance measurement

$$R_e = \frac{V_e}{I_j} = \frac{Z}{\sinh(\alpha d)} \tag{5.18}$$

The parameter Z can be determined from R_C as long as the contact length (d) is longer than two times the transfer length ($\alpha d > 2$). The attenuation constant is described as following [89]:

$$\alpha = \frac{R_s}{W.Z} \tag{5.19}$$

With

$$R_{sh} = (R_1 - R_2).\frac{W}{l_1 - l_2} \tag{5.20}$$

And

$$R_C = \frac{R_2.l_1 - R_1.l_2}{2.(l_1 - l_2)} \tag{5.21}$$

The values of R_1, R_2, l_1 and l_2 can be measured from the structure shown in Figure 5.8. This extraction method is not capable of determining the sheet resistance underneath the contact. However, a new measurement method on similar contact structures as in Figure 5.8 proposed by Reeves [81] allowed the extraction of the contact resistance. By extracting the contact end resistance R_e and contact resistance R_C directly from the measurements, we can find the transfer length L_T. From the transfer length the sheet resistance underneath the contact can be determined, as shown in Equation 5.22.

$$L_x = \frac{2.R_{sk}.L_T}{R_{sh}} \tag{5.22}$$

Since this measurement method also uses a TLM structure, the same problems of current crowding and edge currents along the contact exist. Therefore, a Circular TLM structure could also be used to extract the sheet resistance underneath the contact (R_{sk}) in a similar fashion [90].

5.3.3 Four terminal resistor

The main issue with the TLM method is that the extraction of the contact resistance is based on extrapolation of data and therefore measurement errors are more critical. Measuring small values for the specific contact resistivity ($\rho_c < 10^{-7}\Omega.cm^2$) becomes more inaccurate. The inaccuracy comes from the errors made inadvertently during the measurements. These measurement errors have significant error propagation when extracting the contact resistance and specifically the specific contact resistivity resulting in large measurement uncertainty. It would therefore be beneficial to have a measurement method that extracts an absolute value for V/I straight away. The four terminal resistor also know as a Kelvin resistor [91], uses only one single contact area between metal and semiconductor material. The structure consists of four contact pads: two pads are connected to the doped bulk semiconductor material and two pads contact to the metal used to form the ohmic contact. The metal level and semiconductor material level are separated by an insulating material such as SiO_2 with a window for the ohmic contact area shown in Figure 5.13.

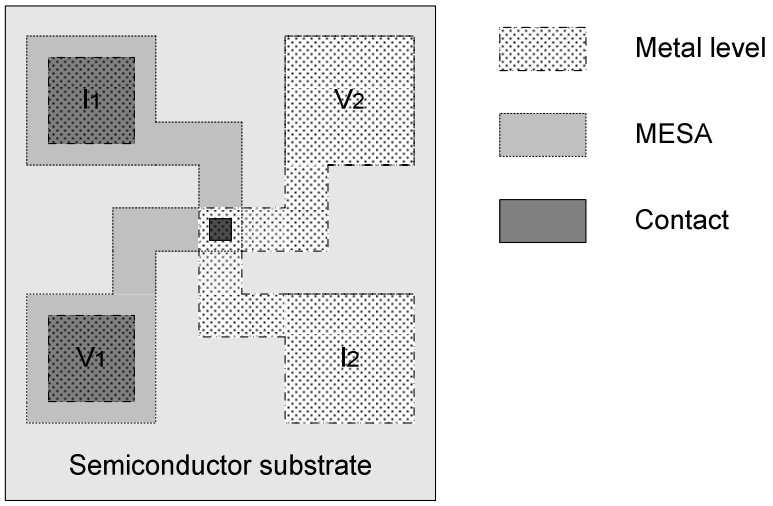


Figure 5.12: Four terminal resistor structure

Current is then forced into terminal I_1 and I_2 and a corresponding voltage drop over the ohmic contact is measured on terminal $V_1$and V_2. Since there is no current flow through terminal V_1 and V_2, the voltage drop is sensed and the resistances of the probes, metal layer and diffusion layer will not be measured. The value of the contact resistance R_C is measured directly, however for comparison purposes the value has to be adjusted to get a normalised value in Ω.mm. The big advantage of this measurement method is that small contact areas can be measured, corresponding to the same size of source/drain contact area used in current VLSI technology. The specific contact resistivity ρ_c is then extracted from

the contact resistance R_C value and the contact area A ($R_C = \rho_c/A$). This is based on a simple vertical current flow model and the sheet resistance of the semiconductor material is not taken into account. This means that current crowding effects cannot be taken into account when extracting the specific contact resistivity as described by W.M. Loh [92]. Substantial research has been done on the effect of lateral current spreading [93 - 96], which limits the size of the diffused semiconductor area. The measured value of V/I is no longer described as R_C but as R_k, which is a combination of R_C and an additional resistance R_{geom} due to current flow around the contact in the overlap region.

$$R_k = R_C + R_{geom} \tag{5.23}$$

$$R_k = \frac{\rho_c}{A} + \frac{4R_{sh}\delta^2}{3W_xW_y}\left[1 + \frac{\delta}{2(W_x-\delta)}\right] \tag{5.24}$$

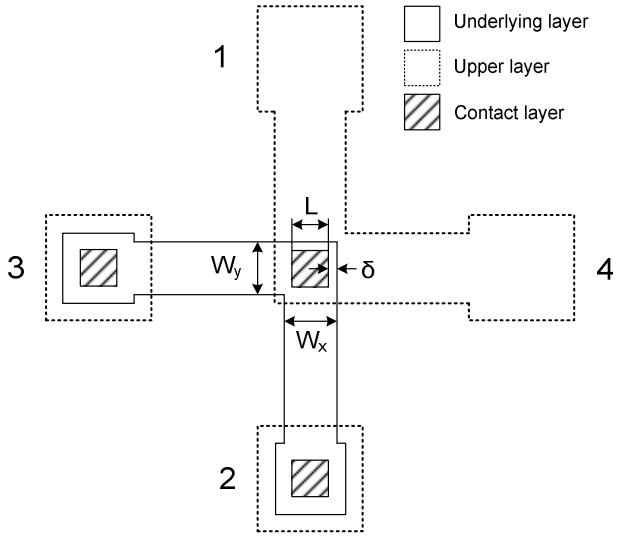


Figure 5.13: Contact area geometries for four terminal resistor structure [96]

This allows a more accurate extraction for R_C, but the specific contact resistivity is still extracted without taking into account the metal sheet resistance and the sheet resistance underneath the contact. The contact length should then be at least two times bigger than the transfer length in order to extract values for the specific contact resistivity ρ_c. Also the bulk semiconductor sheet resistance R_{sh} will have to be measured using a separate measurement method such as TLM or Hall measurement.

5.3.4 Summary

The measurement method used will determine, which parameters can be measured and how accurate they can be measured. The properties of each measurement method has been summarised in Table 5.2.

	Parameters extracted	Processing limitations	Measurement limitations
Two contact	R_C and ρ_c	- Uniformly doped, single layer bulk semiconductor only.	- Simple vertical model flow model. - Does not measure R_{sh}
TLM	R_C, R_{sh} and ρ_c	- Mesa etch	- Needs identical contacts - Extrapolation of data increases measurement inaccuracies
TLM Reeves	R_C, R_{sh}, R_{sk} and ρ_c	- Mesa etch	- Needs sufficient voltage drop over the contact length
CTLM	R_C, R_{sh} and ρ_c	- Lift off or etching of circular structures - Structure requires more space	- Needs identical contacts - Needs a correction factor to fit the curve
CTLM Reeves	R_C, R_{sh}, R_{sk} and ρ_c	- Lift off or etching of circular structures - Structure requires more space	- Needs sufficient voltage drop over the contact length
Kelvin Resistor	R_C and ρ_c	- Mesa etch	- Simple vertical model flow model. - Does not measure R_{sh}

Table 5.2: Comparison of the different ohmic contact measurement methods.

5.4 Channel material characterisation

The performance of III-V MOSFET devices strongly depends on the quality of the epitaxial layers grown by molecular beam epitaxy. The electron density and mobility of the active layers will define the drain current of the device, which determines factors such as sheet resistance, transconductance, subthreshold swing, I_{on}/I_{off} and $I_{d,sat}$ chapter 3.3.1. These parameters are key figures of merit for device performance and extracting the numbers for the electron density and mobility will allow for a more in depth study of the device behaviour.

The most frequently used method for semiconductor material characterisation is a technique based on the principles of the Hall effect [99]. The Hall effect describes the

influence of a force F and a magnetic field B on the current density J in a semiconductor. The charged carriers in the semiconductor material can thus be deflected by an electric field and a magnetic field.

$$F = J.B \tag{5.25}$$

If the magnetic field and the current flow through the semiconductor are perpendicular, then a Lorentz force is applied to the charged carriers. The electrons will accumulate on one side of the semiconductor whereas the holes will deplete the opposite side of the semiconductor. A voltage difference will then occur across the semiconductor expressed as V_H.

$$V_H = \frac{B.I.R_H}{t} \tag{5.26}$$

Where t is the thickness of the sample and R_H is the Hall coefficient, which is material dependent.

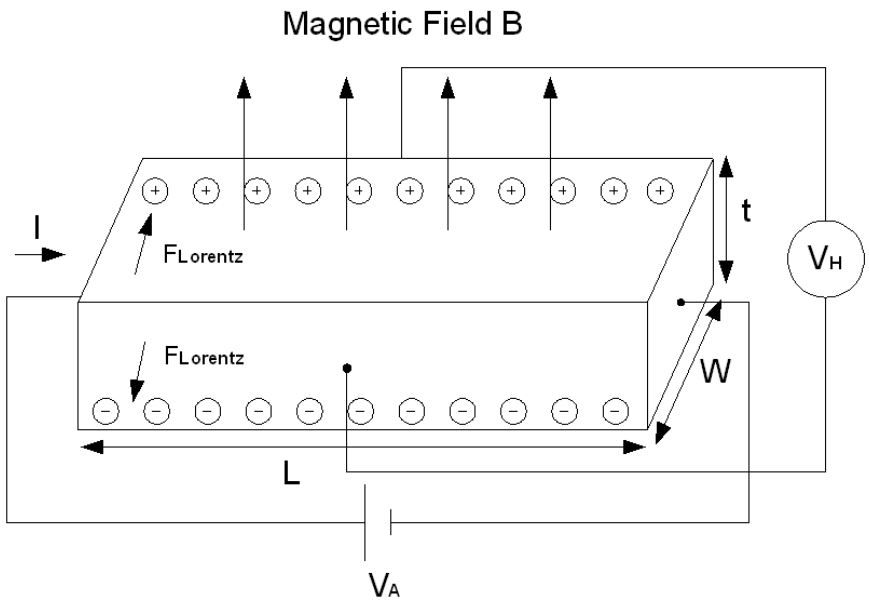


Figure 5.14: Hall effect principles

The conductivity of the semiconductor material σ is given by:

$$\sigma = \frac{I.L}{V_A.W.t} = n.q.\mu \tag{5.27}$$

Where L is the semiconductor length and W is the semiconductor width. The Hall coefficient R_H is equal to 1/n.q, the mobility is then defined as:

$$\mu = \sigma.R_H = \frac{1}{n.q.\rho} \tag{5.28}$$

The thickness of the material has to be known and the sample geometries have to be precise to be able to extract the mobility data. However, determining the layer thickness of a multi layer III-V semiconductor structure is not straightforward. A measurement method proposed by Van der Pauw [100] allowed for the extraction of the mobility without knowing the thickness of the material.

The Van der Pauw technique is based on the extraction of the Hall coefficient and resistivity value from a sample with an arbitrary geometry. The contacts are positioned at each corner of the sample resulting in a symmetrical design. The symmetry has as a result that the resistance values (R) are then equal across any given edge along the sample. Simplifying the equation for the resistivity value gives:

$$\rho_{sh} = \frac{\pi t R}{\ln(2)} \tag{5.29}$$

$$R_{sh} = \frac{\rho_{sh}}{t} = \frac{\pi R}{\ln(2)} \tag{5.30}$$

The sheet resistance can then be found by dividing the sheet resistivity by the thickness of the layer and can be directly extracted from the measurement, as the thickness of the material does not have to be known.

The resistance value (R) measured across the edge of the sample changes when a perpendicular magnetic field is applied to the sample. Since the magnetic field drives a change in the resistance, the Hall coefficient can then be extracted by measuring the changes in resistance, corresponding to a known perpendicular magnetic field.

$$R_H = \frac{t}{B}\Delta R \tag{5.31}$$

The mobility is a product of the conductivity and Hall coefficient and can in this case be extracted without requiring the sample thickness.

$$\mu = \frac{\ln(2)}{\pi . B} . \frac{\Delta R}{R} \tag{5.32}$$

With the majority carrier density being:

$$n_s = \frac{B}{\Delta R . q} \tag{5.33}$$

The structure used is shown in Figure 5.15 and shows that the contacts are positioned around a central square. The square, attached wires and contact areas is a mesa layer, which allows the current to flow from the contacts into the square while isolating the

square from any leakage currents. Ohmic contact metal is then deposited on the contact areas and has to be low in resistance to allow for an accurate measurement.

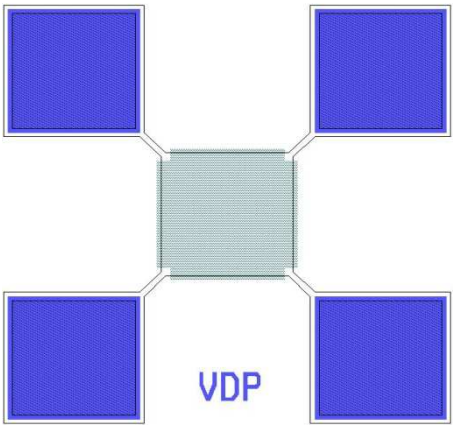


Figure 5.15: Van der Pauw test structure

The Van der Pauw measurement method is assumed to be accurate as the impact of the hole concentration is below the ionisation field thresholds. This is only valid in material where the hole concentration is sufficiently low compared to the electron concentration, which is the case for the highly doped $In_{0.53}GaAs$ and device materials used in this work.

5.5 Oxide characterisation

The oxide quality can be measured by making use of a capacitance voltage measurement or simply CV measurement. The basic principle of the CV-measurement is to apply an AC signal to the structure with a certain frequency and amplitude superimposed on a DC voltage. The DC voltage is swept to explore the inversion, depletion and accumulation regions. This will result in a curve, which shows the capacitance for one particular frequency. However, there is a frequency dependence of the CV measurement, because there is a certain amount of time needed to obtain thermal equilibrium. This does not allow for generation of minority carriers in the inversion layer and therefore a low and high frequency CV-measurement are necessary.

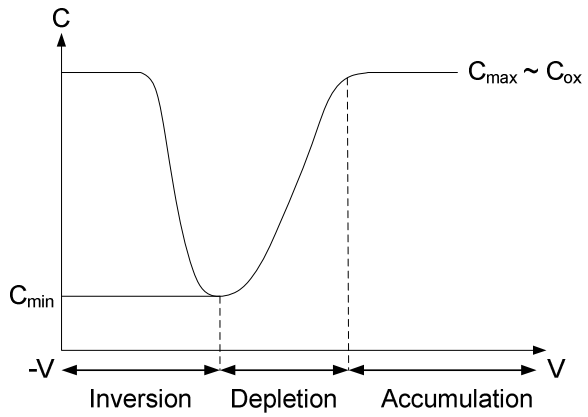


Figure 5.16: Low frequency capacitance - voltage plot

Quasi static or a low frequency measurement stays within the time boundaries for thermal equilibrium to take place. The capacitance measured over the voltage range is then directly related to the capacitance of the oxide. By sweeping the voltage, different capacitance values are measured for the different potential distribution modes for n-type semiconductor material. The different potential modes; accumulation, depletion and inversion are explained in chapter (3.3).

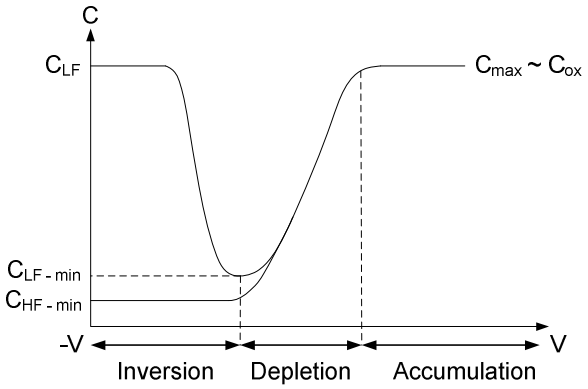


Figure 5.17: High frequency capacitance voltage plot

High frequency measurement does not allow for the thermal recombination/generation of the minority carrier. This limits the response of the inversion layer to the applied AC signal and renders the minority carriers invisible to the CV measurement. The depletion region will therefore stay constant and the capacitance stays constant at $C_{d(max)}$. The series combination of C_{ox} and C_d will then give $C_{HF\ -\ min}$ as a result. The high frequency CV measurement can also be used to show the effects of interface defects. The charges can then be extracted by calculating the charge difference between $C_{LF\ -\ min}$ and $C_{HF\ -\ min}$. However, this has not been used in this work as the focus is on the study of ohmic contact behaviour rather than oxide/semiconductor interface quality.

5.6 Device performance characterisation

The various MOSFET device parameters are extracted from two different measurements. In both cases the gate is connected to a voltage source and the source and drain are connected to a different voltage source. The first measurement sweeps the drain voltage and measures the source/drain current for a given gate voltage. The gate voltage is then raised in steps and the process is then repeated, which results in a I_d/V_d plot Figure 5.19. The source/drain voltage sweep ranges from 0V past the saturation point. Further increasing the drain voltage can damage the device due to avalanche effects. The second measurement keeps the drain voltage constant and sweeps the gate voltage from a negative voltage (between inversion and depletion) to a positive voltage (accumulation) resulting in a I_d/V_g plot Figure 5.20 and 5.21. The I_d/V_g plot is measured in the linear regime of the MOSFET and in the saturation regime, which can be found from the I_d/V_d characteristic.

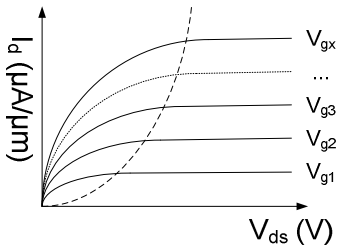


Figure 5.18: I_d/V_d plot

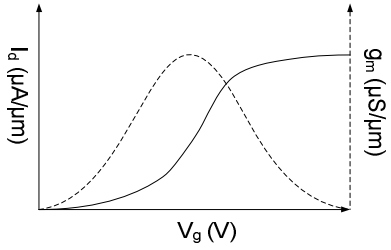


Figure 5.19: I_d/V_g plot

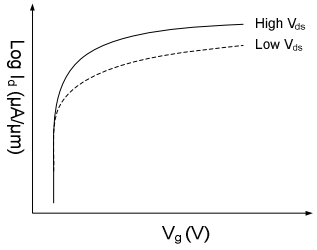


Figure 5.20: Logarithmic I_d/V_g plot

The I_d/V_d plot mainly extracts information about the maximum drain current and gives an indication for the linear and saturation regime of the MOSFET device. The data directly extracted from the measurement setup for the I_d/V_g curve are:

Symbol	Unit	Device parameters
g_m	S/μm	Normalised: $\delta I_d/\delta V_g$
Swing	mV/decade	Subthreshold swing
Swingmin	mV/decade	Lowest value for the subthreshold swing
$g_{m,max}$	S/μm	Maximum value for g_m
$I_{d,sat}$	A/μm	Saturation current maximum (normalised)
V_{thcon}	V	Gate voltage measured when I_d = 1 μA.μm
$I_{g,max}$	A	Maximum gate leakage
R_{on}	Ω.μm	source/drain resistance at highest gate voltage (normalised)
V_{on}	V	Voltage measured at maximum g_m
V_{thlin}	V	Threshold Voltage extracted from V_{on} - (V_d/2)

Table 5.3: Device parameters extracted from I_d/V_g plot.

The DIBL value is not directly extracted from the measurement set-up, but is calculated afterwards when the data is processed. The data is processed by using a template in a Origin 8 software package, allowing for faster analysis of the measured data.

5.7 Metrology

The equipment used to measure the various measurement setups are semiconductor analysers, which need to be able to perform accurate DC and AC measurements up to 1MHz. Only the CV characterisation uses an AC measurement, the ohmic contact and device measurement is DC only. The majority of the ohmic contacts have been measured on an Agilent 4155C semiconductor parameter analyser using a four probe measurement set-up to compensate for any series resistance of the cables, probes and connectors. The schematic representation of a four probe measurement is shown in Figure 5.22, where two probes are used on each side of the device under test (DUT). One pair of probes is used to pass current (I) through the device under test and the other pair of probes measures the voltage drop (V) over the device under test. The impedance of the voltage measurement tool has to be significantly higher than the resistance of the device under test, to keep the maximum amount of current flowing through the device under test. This will result in a negligible current through the voltage sensing probes, which minimises the voltage drop over the probe and cable resistances (R_{p2}, R_{p3}). The voltage V will then be equal to the

voltage drop over the device under test, resulting in a highly accurate measurement. The voltage drop over the current feeding probes (R_{p1}, R_{p4}) is unimportant as the current source provides a known constant current (I). The values of current and voltage over the device under test are then measured independently from each other cancelling out the resistances by probes, cables, switches and connectors between the semiconductor parameter analyser and the measured sample. This measurement set-up can be calibrated to obtain higher accuracy and sensitivity. However, there is currently no calibration kit available for the DC measurement set-up.

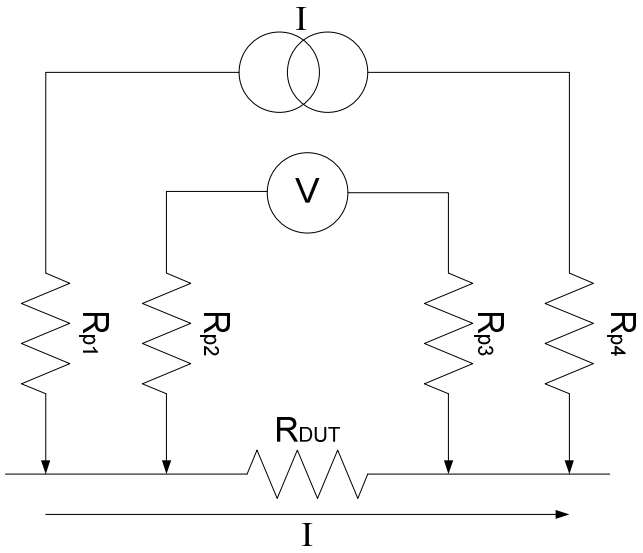


Figure 5.21: Schematic representation of a four probe measurement set-up

The CV, device and some ohmic contact measurements were performed on a Agilent B1500 semiconductor parameter analyser. The analyser is connected to a semi-automatic Cascade Microtech Summit 12000 probe station allowing for rapid measurements of multiple devices using Agilent Easy Expert and Cascade Microtech Nucleus software packages running on a Windows XP control computer. The control computer, semiconductor parameter analyser and probe station are connected via a General Purpose Interface Bus (GPIB).The control computer is able to control the stage of the probe station and extract the data from the semiconductor parameter analyser allowing for automatic measurements of multiple test structures. The probes have to be positioned manually prior to the automated measurement. The source and drain pads are connected to a double probe set-up allowing for a four probe measurement set-up and the gate is connected via a single probe, as shown in Figure 5.23. The single probe set-up on the gate should not suffer from voltage drops over the probes, cables and connectors, as the resistance of the oxide of a MOSFET device is high, reducing the current flowing through the gate probe.

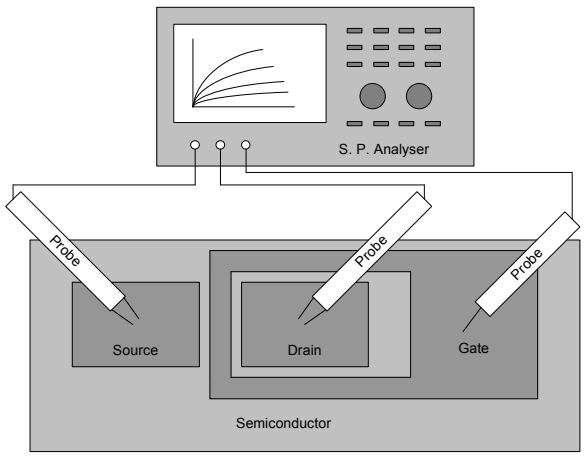


Figure 5.22: MOSFET Device measurement set-up

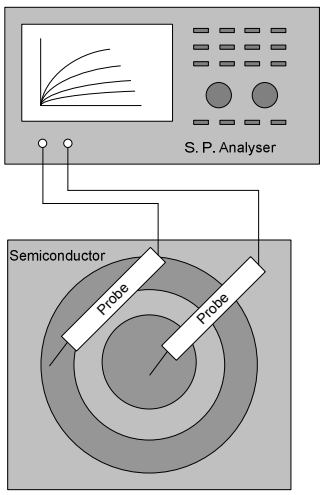


Figure 5.23: Capacitance - Voltage measurement set-up

The CV measurement uses two single probes as the series resistance of the probes is not critical to extract capacitance values. Ideally, the capacitance of the cables and connectors should be calibrated out by making use of a calibration kit. There is currently no capacitance calibration kit available, which leads to reduced sensitivity and accuracy of the measurement set-up. The CV measurements in this work have been used to verify the overall quality of the oxide rather than a detailed study of the metal/oxide/semiconductor interface removing the need for a highly accurate measurement set-up.

5.8 Summary

The first part of this chapter presented the different terminology and models used to describe the physical properties of an ohmic contact. The second part of this chapter described the different characterisation techniques used to measure ohmic contacts, devices, gate dielectrics and semiconductor properties. Emphasis has been put into the various ohmic contact characterisation techniques and a comparison has been made between them. The importance of correctly interpreting and extracting the physical ohmic contact properties will become clear in a later chapter. Also, the measurement equipment used during this work is described in this chapter and is a contributing factor to the accuracy of the measurements.

6 Ohmic contact development

6.1 Introduction

A metal/semiconductor interface is described as ohmic when the applied voltage and the resulting current flow have a linear relation, however good ohmic contacts need to have several additional properties. First of all they need to have a very low specific contact resistivity ρ_c $<10^{-8}\Omega.cm^2$ to meet MOSFET device requirements [1]. Secondly, the ohmic contacts have to be thermally stable, reproducible, uniform, non corrosive and have to be Si-processing compatible in an industrial environment. Finally, the ohmic contacts have to be scalable in order to keep up with the ever decreasing size of the transistors used in CMOS technology.

A generic ideal contact characteristic is first described and different contact strategies from previous work are then discussed regardless of any process flow constraints. This allows for a global overview of the different ohmic contact strategies on n-type $In_xGa_{1-x}As$ and GaAs. The ohmic contact strategies are divided up in different categories: alloyed contacts increasing doping; bandgap reducing ohmic contacts; non alloyed contacts on doped substrates; and various surface treatments and cleaning techniques to reduce the gap states formed at the metal/semiconductor interface. Regrowth and implantation techniques are also discussed as a mean of selectively increasing doping concentration underneath the metal/semiconductor interface.

This work has constraints on the materials used as the aim of this project is to develop Si-processing compatible ohmic contacts. This is not the only constraint as the MOSFET material has some limitations regarding the temperature budget, choice of oxide etching techniques and the potential scalability of the ohmic contact. Taking into account the various constraints a suitable ohmic contact strategy has been chosen from the previous work to correspond with specific MOSFET device material used in this work.

Finally, the experimental work will be discussed. The experimental ohmic contact work is divided up in two parts: ohmic contacts and MOSFET devices. The ohmic contact aspects are further subdivided as alloyed and non-alloyed contacts sections. This is because the alloyed part mainly focuses on forming ohmic contacts on MOSFET device material while the non-alloyed part focuses on highly doped $In_{0.53}GaAs$ material to investigate the possible gains if doping can be introduced in the device structure. The MOSFET device material has a gate dielectric layer in place, which has to be removed prior to contact

deposition and therefore wet etch and dry etch strategies are required. The alloyed contacts are analysed using transmission electron microscopy (TEM) and electron energy loss spectroscopy (EELS) to get a better understanding of the reactions taking place during annealing. The MOSFET device section features two different types of device: surface channel and buried channel MOSFET devices. These are discussed separately and benchmarked against previous work performed at the University of Glasgow using material with identical layer structures to assess the impact of the differences in the ohmic contact strategies.

6.2 Theory/Ideal Ohmic Contact Properties

Many factors contribute to the overall quality and feasibility of an ohmic contact scheme such as: specific contact resistivity, contact stability, surface and edge definition, radiation damage resistance, low cost, reproducibility and robustness against corrosion. In reality there will always be a trade-off between the different criteria. For example, a gold based ohmic contact scheme has a low specific contact resistivity, but imposes a low thermal budget for following processes and may have poor morphology. It is then important to understand all the criteria in order to choose the optimal ohmic contact scheme for a given device structure.

Specific Contact Resistivity: This will contribute to the total on resistance of the MOSFET device and has to be significantly small in order to allow for large ON-state current at a low supply voltage. Also when the devices are scaled and the ohmic contact area becomes very small, current crowding effects start to take place. The ITRS road map for sub 45nm technology requires a specific contact resistivity value in the low $10^{-9}\Omega cm^2$ range.

Contact stability: Ohmic contacts have to withstand elevated processing temperatures after the ohmic contact formation. The ohmic contact strategy has to be compatible with these elevated temperatures and is potentially a problem when using alloyed ohmic contact strategies. When the alloying temperatures are close or below the maximum processing temperature, additional reaction between the contact and semiconductor will take place. This may deteriorate the optimized ohmic contact structure causing additional lateral and vertical diffusion. The diffusion area has to be reduced to a minimum when working with shallow active layers and scaled device feature sizes.

Surface smoothness and edge definition: The separation between electrodes has been reduced over the years to a nanometer scale. A good edge definition is then needed to aid the processing of the devices and preventing short circuits. This property is less critical

when using self-aligned device structures. The contact surface morphology has to allow for easy interconnect wiring. Both properties are essential for devices with high yield requirements.

Corrosion resistance: Oxidation or corrosion during processing will deteriorate contact properties and will hamper interconnectivity bonding and its long term reliability. Metals such as Au and Pt are generally inert and do not have corrosion issues, however other corrosive metals might provide a better overall solution for an ohmic contact scheme and will require a protection layer.

Radiation damage resistance: The metals with a relatively low atomic number generally have a better resistance to radiation environment. However, CMOS technology is generally not used in high radiation environments and it's thus a minor issue.

Low residual stress: Stress can induce dislocations in the semiconductor device leading to device degradation. It can also limit the adhesion between the metal and the semiconductor resulting in metal layers peeling off.

Good thermal and electrical conductivities: VLSI applications generate a significant amount of heat within the devices, which has to be able to be dissipated. High thermal conductivity of the ohmic contact scheme used will aid the dissipation of heat. The metal also has to have good electrical conductivity as the current is passed through the metal into the wire bond or interconnect.

6.2.1 Recent developments

The III-V semiconductors suffer from high concentration of surface states at the surface of the semiconductor. These states are located in the bandgap, which causes Fermi level pinning at the Bardeen [203] limit. This results in a Schottky barrier that will cause high specific contact resistivity or in the worst case non ohmic behaviour. There are three ways to reduce the Schottky barrier:

a) Reduce the density of states, unpinning the Fermi level leads to a lower Schottky barrier height.

b) Reduce the barrier height by choosing a lower bandgap semiconductor material.

c) Increase the doping concentration to reduce the Schottky barrier width and increase the tunnelling probability of electrons.

The ideal case is a highly doped low bandgap material such as n-InAs to make low resistivity ohmic contacts. This allows for non alloyed contacts with good edge definition and generally good contact stability. To apply this strategy to an actual MOSFET a highly doped contact region with low bandgap semiconductor material will have to be regrown [119] as the device layer structure is MBE grown with a gate dielectric in place. Even though the University of Glasgow has an onsite MBE chamber, which potentially allows for regrowth, introducing processed wafers would potentially contaminate the chamber. This limits the best suitable ohmic contact strategy to an alloyed ohmic contact for the MOSFET work of this project. A HEMT-like layer structure with highly doped contact regions could potentially solve this problem, however it complicates the gate dielectric formation process as the highly doped layer has to be etched away. The gate dielectric deposition requires a very smooth surface to feature a low density of states and it is therefore undesirable to deposit a gate dielectric on an etched surface.

There are two main groups of alloyed ohmic contact strategies, increasing doping by inserting a n-type dopant in III-V material such as Si or Ge and reducing the barrier height by reducing the bandgap by increasing the indium concentration. Inserting a n-type dopant or indium into III-V material can be done by solid phase regrowth. The most common used ohmic contact strategies for III-V devices are a NiGeAu and PdGe based contact, which will be described in more detailed followed by a summary of various alloyed, bandgap reducing and non alloyed contact schemes.

6.2.1.1 Alloyed

Increasing doping into substrate:

NiGeAu [118, 120, 129]

This is the most commonly used ohmic contact to n-type III-V materials, resulting in an increased n-type surface doping provided by the Ge layer. The composition is generally 12% Ge and 88% Au and the mixture has a melting temperature of 361ºC on GaAs [3]. The Au and Ge forms a AuGe alloy, which is prone to “balling up” once temperatures exceed the eutectic temperature, which leads to poor morphology. Ni reacts with GaAs at lower temperatures to form binary and ternary compounds (Ni_3Ge, Ni_2GaAs, Ni_3GaAs) and facilitates the incorporation of Ge as an n-type dopant. Further increasing the temperature to 420ºC forms a AuGa compound and is responsible for spiking behaviour, which leads to lateral alloying of the contact. The Ni then forms a conductive NiAs(Ge)

compound. Specific contact resistivity of $2x10^{-6}\Omega cm^2$ has been reported on $7.5x10^{18}cm^{-3}$ doped GaAs [127].

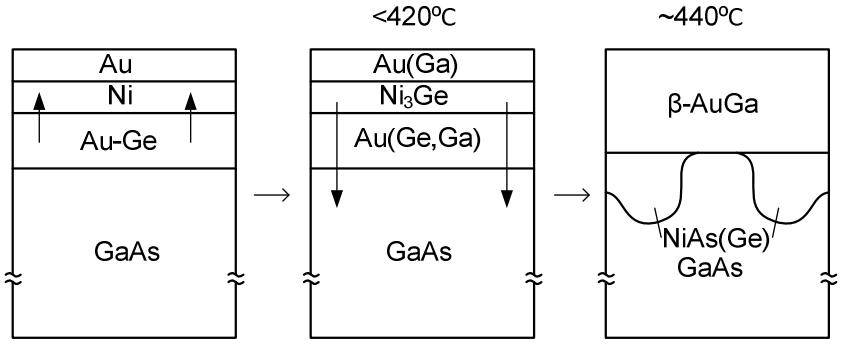


Figure 6.1: Schematic illustration of an alloying sequence Au/Ni/AuGe metallization on GaAs [3]

Table 6.1 shows a summary of Ni/Ge based ohmic contacts to n-GaAs/n-InGaAs and the metal layer at the left hand side makes contact to the semiconductor surface layer for all the following tables.

Metallisation	Anneal (optimal temperature)	Doping (cm^{-3})	Substrate	ρ_c ($\Omega.cm^2$)	R_C (Ω.mm)	Ref.
Ni/Ge/Au	450°C 5s	$2.00x10^{+18}$	GaAs		0.2	[142]
Ni/Ge/Ag	550°C -650°C	$2.00x10^{+18}$	GaAs		0.26	[143]
Ge/Ni	600°C	$1.00x10^{+18}$	GaAs		0.8	[147]
Al/Ni/Ge	500°C	$1.00x10^{+18}$	GaAs	$1.40x10^{-6}$		[148]
Au/W0.6N0.4/ Ge/Ni	500°C	$1.00x10^{+18}$	GaAs	$1.00x10^{-6}$		[160]
Ni/Ge/W	650°C 5s	$1.00x10^{+18}$	GaAs		0.16	[163]
Au/Ge/Ni/Au	400°C	$4.00x10^{+17}$	GaAs	$5.60x10^{-6}$		[173]
Ni/Ge/Au			GaAs			[176]
Ni/Ge/Au	420°C	$7.50x10^{+18}$	GaAs	$2.00x10^{-6}$		[127]
Ni/Ge/ (..,Au,Ag,Pd,In)			GaAs	Low 10^{-6}		[129]
Au/Ni/Au/Ge/Pd	400°C		GaAs-			[192]
Au/Ni/Au/Ge/Pd	400°C	$2.00x10^{+17}$	InGaAs	$1.00x10^{-6}$		[192]
Au/Ge/Ni/Au	440°C	$3.00x10^{+18}$	$In_{0.53}GaAs$		0.9	[118]
Ge/Ag/Ni	425°C 60s	n/a	$In_{0.53}GaAs$	$2.62x10^{-7}$	0.06	[120]

Table 6.1: Summary of Ni/Ge based ohmic contacts to n-GaAs/n-InGaAs

PdGe/PdSi [102, 103, 112, 114, 115, 116, 117, 118, 121, 130, 134, 138]

The two elements have different functions: the Ge or Si provides a n+ doping in GaAs , the Pd reacts with the GaAs allowing for solid phase regrowth. Annealing the Pd/Ge contact to a temperature of 100°C triggers a reaction between the Pd/Ge and the GaAs forming a Pd_4GaAs phase. The contact at this point is not ohmic. At 300°C the Pd_4GaAs decomposes reacting with the Ge layer and forming PdGe. This causes a migration of Ge across the PdGe layer resulting in a n+ GaAs (Ge) doped layer and a Ge layer on the GaAs substrate. An optimal Pd/Ge metallization thickness needs an excess of Ge to form the PdGe layer and Ge regrown layer. Most commonly the Pd/Ge thickness is a ratio of 5/12. Specific contact resistivities of $5x10^{-7}\Omega cm^2$ and $2x10^{-8}\Omega cm^2$ have be reported on $5x10^{18}cm^{-3}$ doped GaAs [187] and on $4x10^{19}cm^{-3}$ doped $In_{0.53}GaAs$ respectively.

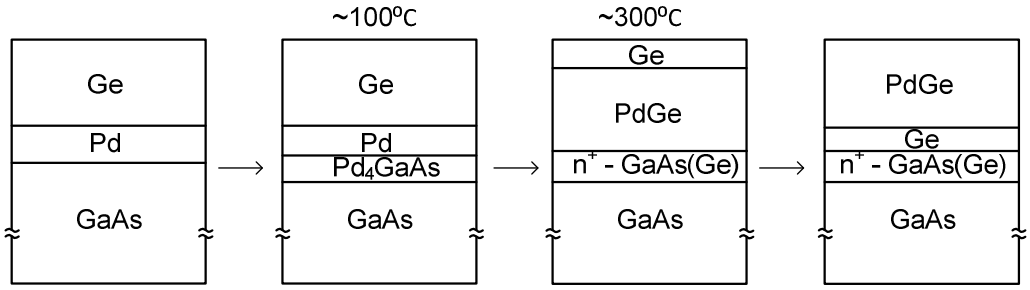


Figure 6.2: Schematic illustration of an alloying sequence Pd/Ge metallization on GaAs [3]

Table 6.2 shows a summary of Pd/Ge based ohmic contacts to n-GaAs/n-InGaAs:

Metallisation	Anneal (optimal temperature)	Doping (cm^{-3})	Substrate	ρ_c ($\Omega.cm^2$)	R_C ($\Omega.mm$)	Ref.
Pd/Ge	325°C	$1.00x10^{+18}$	GaAs	$1\text{-}3x10^{-6}$		[144]
Pd/Si	375°C	$1.00x10^{+18}$	GaAs	$2\text{-}6x10^{-6}$		[145]
Au/Ge/Pd	175°C 1h	$1.00x10^{+18}$	GaAs	$1.00x10^{-6}$		[153]
Au/W/Pd/Ge	800°C 5s	$1.00x10^{+17}$	GaAs	$5.00x10^{-6}$		[161]
Pd/Ge/Ti/Au	380°C	$5.00x10^{+17}$	GaAs		0.43	[168]
Pd/Ge			GaAs	$4.00x10^{-7}$		[179]
Pd/Ge/Ti/Au	340°C	$5.00x10^{+17}$	GaAs	$2.80x10^{-6}$		[182]
Pd/Ge/Ti/Pt	400°C		GaAs	$2.40x10^{-6}$		[183]
Pd/Ge/Ti/Pt	380°C-450°C	$6.00x10^{+17}$	GaAs	$2.40x10^{-6}$ – $5.30x10^{-6}$		[184]
Pd/Ge/Au/Pd/Au	400°C	$6.00x10^{+17}$	GaAs	$2.00x10^{-6}$		[185]
Pd/Ge/Au/Pd/Au	400°C		GaAs	$2.10x10^{-6}$		[186]
Pt/Ti/Ge/Pd	400°C	$5.00x10^{+18}$	GaAs	$5.00x10^{-7}$		[187]
Pd/Ge	320°C 60s	$3.70x10^{+18}$	GaAs	$1.00x10^{-5}$		[189]
Pd/Ge	317C	$7.00x10^{+16}$	GaAs			[138]
Pd/Ge	550°C	$1.00x10^{+16}$	GaAs	$3.50x10^{-4}$		[102]
Pd/Ge	325°C 30min	$4.00x10^{+18}$	GaAs	$9.00x10^{-7}$		[103]
Pd/Si	375°C 30min	$4.00x10^{+18}$	GaAs	$2.00x10^{-6}$		[103]
Ge/Pd/Ti	380°C	$2.00x10^{+18}$	GaAs	$8.50x10^{-7}$		[114]
Pd/Ge	400°C	n/a	GaAs	$9.80x10^{-6}$	0.29	[116]
Ge/Pd	400°C	$1.00x10^{+18}$	GaAs	$2.00x10^{-4}$		[130]
Pd/Ge/Cu	250°C	$4.00x10^{+18}$	GaAs	$5.73x10^{-7}$		[134]
Pd/Ge	400°C		InGaAs	$1.00x10^{-6}$ – $2.00x10^{-6}$		[194]
Pd/Si/Ti/Pt	425°C		InGaAs	$2.00x10^{-6}$		[121]
Pd/Ge/Ti/Pt	400°C		InGaAs	$3.70x10^{-6}$		[117]
Pd/Si/Pd/Ti/Au	300°C-400°C		InGaAs	$4.30x10^{-7}$		[196]
Pd/Ge/Pd/Ti/Au	425°C		InGaAs	$1.00x10^{-6}$		[197]
Pd/Ge/Pd/Ti/Au	400°C 10s	$1.00x10^{+19}$	$In_{0.50}GaAs$	$1.10x10^{-6}$		[112]
Pd/Ge/Ti/Pt	400°C 10s	$1.00x10^{+19}$	$In_{0.50}GaAs$	$3.70x10^{-6}$		[112]
Pd/Ge		$4.00x10^{+19}$	$In_{0.70}GaAs$	$2.00x10^{-8}$	0.01	[218]
Pd/Ge/Au	440°C	$3.00x10^{+18}$	$In_{0.53}GaAs$		0.3	[118]

Table 6.2: Summary of Pd/Ge based ohmic contacts to n-GaAs/n-InGaAs

Various

Other metallization strategies are based on reducing the Schottky barrier width by doping the substrate such as: MoGeW, PdSn and CuGe. CuGe shows specific contact resistivity value of $6.5x10^{-7}\Omega cm^2$ for $1\text{-}3x10^{17}cm^{-3}$ doped GaAs, as shown in Table 6.3 [132].

Towards the end of the project, a novel Ni-based salicide-like metallization contact strategy to $In_xGa_{1-x}As$ MOSFET devices was demonstrated [216, 217] showing some promising results. The main objective of this technique is to reduce the Schottky barrier height to almost zero by increasing the doping and the indium content in the underlying semiconductor material. The Ni-salicide layer is created by depositing Ni on a $In_xGa_{1-x}As$ substrate and then subjecting the sample to an annealing temperature of at least 250°C. This forms a Ni-InGaAs layer with good morphology and is uniform across the source/drain region with a composition ratio of Ni (51%), In (12%), Ga (14%) and As (23%) [216]. However, the specific contact resistivity value in the range of $10^{-3}\Omega cm^2$ to $10^{-4}\Omega cm^2$ is quite poor.

Metallisation	Anneal (optimal temperature)	Doping (cm^{-3})	Substrate	ρ_c ($\Omega.cm^2$)	R_C (Ω.mm)	Ref.
Ni	250°C 60s	Si Implant	$In_{0.7}GaAs$	10^{-3} ~ 10^{-4}	8.9 ~ 7.6	[216]
Ni	250°C 60s	Si Implant	$In_{0.8}GaAs$		2.73	[217]
Cu/Ge	400°C 30min	$1\text{-}3x10^{+17}$	GaAs	$6.50x10^{-7}$		[132]
Cu/Ge	200°C – 400°C	$3.00x10^{+17}$	GaAs	$6.50x10^{-7}$		[111]
Au/TaSiN/ Au/Ge/Pt	450°C- 550°C	$1.00x10^{+18}$	GaAs	$3.70x10^{-6}$		[151]
Mo/Ge/W	800°C	$1.00x10^{+18}$	GaAs		0.3	[154]
Au/WSi/Ge	600°C	$1.00x10^{+16}$	GaAs	$5.00x10^{-5}$		[159]
Pd/Sn	360°C	$2.00x10^{+18}$	GaAs	$3.00x10^{-5}$		[180]
Pd/Sn, Pd/Sn/Au	360°C-430°C		GaAs	$8.00x10^{-6}$ – $3.00x10^{-5}$		[181]
Pd/Ga/Ti/Au	380°C -460°C	$7.00x10^{-16}$	$Al_{0.23}GaAs$	$2.30x10^{-6}$ – $9.50x10^{-5}$		[195]

Table 6.3: Summary of various alloying ohmic contact strategies to n-GaAs/n-InGaAs

Bandgap reduction

Replacing Ga with In reduces the bandgap of GaAs, which reduces the specific contact resistivity. Some metallization strategies combine In with Ge to dope the substrate as well as lowering the bandgap. This results for the Pd/Ge/In case in a specific contact resistivity of $6x10^{-7}\Omega cm^2$ for $1x10^{18}cm^{-3}$ doped GaAs, as shown in Table 6.4 [165].

Metallisation	Anneal (optimal temperature)	Doping (cm^{-3})	ρ_c ($\Omega.cm^2$)	R_C ($\Omega.mm$)	Ref.
Pd/In/Pd	600°C - 650°C	$1.00x10^{+18}$	$1.00x10^{-6}$		[146]
W/In	700°C - 800°C	$1.00x10^{+18}$		<0.2	[150]
Mo/Ge/In/W	675°C	$3.50x10^{+13}$		0.3	[156]
Ge/In/W	900°C - 980°C	$3.50x10^{+13}$		0.5	[157]
Ni/In/W	800°C - 1000°C	$3.50x10^{+13}$		0.3	[157]
W/In/Te	500°C	$6.00x10^{+13}$	$5.00x10^{-6}$		[162]
W/Ni/InAs	750°C - 850°C	$3.50x10^{+13}$		0.4	[119]
W/Ni/InAs/Ni	750°C - 850°C	$3.50x10^{+13}$		0.4	[119]
Pd/In/Ge	400°C	$1.00x10^{+18}$	$6.00x10^{-7}$		[165]
Ni/In/WN	750°C 5s	$6.60x10^{+13}$		0.3	[166]
Ni/In/Ge	650°C			0.18	[175]
In	375°C	$2.00x10^{+16}$	$3.00x10^{-6}$		[177]
Pd/In	600°C	$1.70x10^{+18}$	$1.00x10^{-6}$		[178]

Table 6.4: Summary of In based bandgap reducing ohmic contact strategies to n-GaAs

6.2.1.2 Non alloyed [108, 113, 122, 135, 136, 137, 139]

Non alloyed ohmic contacts are ideal for applications where good morphology and edge definition are required. Non alloyed does not necessarily mean non annealed, but the contact metal does not react with the substrate after heating. The quality of the ohmic contact is nearly entirely dependent on the substrate material. Most non alloyed ohmic contacts strategies are applied to highly doped, high indium concentration material as they do not introduce additional doping or reduction of the bandgap. Native oxides are a critical issue as there is no possibility to aggressively alloy through the oxide layer. This makes substrate surface treatment prior to metal deposition vital for ohmic contacts with low specific contact resistivity values. Different surface treatments can be used: cleaning of the surface oxides, depinning of the surface and regrown InGaAs/InAs regions with in-situ metal deposition. An overview of various non alloyed contacts is shown in Table 6.5:

Metallisation	Doping (cm^{-3})	Substrate	ρ_c ($\Omega.cm^2$)	Ref.
Au/Pt/Ti	$1.50x10^{+19}$	GaAs	$1.10x10^{-6}$	[149]
Au/Ti	$5.00x10^{+18}$	GaAs	$2.00x10^{-6}$	[169]
Au/Al/Ti	$2.00x10^{+18}$	GaAs	$3.70x10^{-3}$	[170]
Cr/Au	$6.10x10^{+19}$	$In_{0.53}GaAs$	$1.70x10^{-8}$	[199]
Mo	$5.00x10^{+19}$	$In_{0.53}GaAs$	$1.00x10^{-8}$	[137]
Mo	$3.60x10^{+19}$	n/a	$1.30x10^{-8}$	[200]
Ti/Pd/Au	$3.50x10^{+19}$	$In_{0.53}GaAs$	$7.30x10^{-7}$	[108]
TiW/Ti/Ni	$3.50x10^{+19}$	$In_{0.53}GaAs$	$8.40x10^{-7}$	[108]
ErAs	$3.50x10^{+19}$	InAs	$1.50x10^{-8}$	[113]
Mo	$3.50x10^{+19}$	InAs	$5.00x10^{-9}$	[113]
TiW	$3.50x10^{+19}$	$In_{0.53}GaAs$	$7.00x10^{-9}$	[113]
Al	$3.00x10^{+19}$	$In_{0.50}GaAs$	$4.80x10^{-7}$	[135]
Au/Pt/Ti/WSiN	$1.00x10^{+19}$	n/a	$2.00x10^{-7}$	[122]

Table 6.5: Summary of non alloyed ohmic contact strategies to n-GaAs/n-InGaAs

Surface treatment

The surface of a GaAs, InGaAs and InAs substrate has a thin native oxide layer, which contains defects of sufficient density to pin the Fermi level. Even though the Fermi level pins in the conduction band in high indium concentration (>80%) material, the oxide causes an increased resistance as electrons have to tunnel through the thin oxide layer. It is therefore important to remove surface native oxides, which can be done via cleaning procedures. After the substrate cleaning there are also techniques using sulphur to passivate the substrate, reducing the number of states at the semiconductor surface. Alternatively the Fermi level can be unpinned by introducing an insulating layer between the metal and semiconductor to reduce gap states, which will lower the Schottky barrier height and lower the specific contact resistivity. But as a consequence the electrons will have to tunnel through a thin insulator rather than a Schottky barrier.

The ideal case is where the ohmic contact structure can be deposited in-situ on top of the semiconductor layer to overcome any surface oxide formation. This is another advantage of using regrowth techniques, as the sample can be metallised in the same tool without breaking the vacuum.

Cleaning

The native oxide can be removed by either wet or dry etch. The wet etch is the most common technique used and is based on wet etches of acids, ammonia based solutions or solutions containing sulphur. The H component of the acids bonds to the native oxide

forming H_2O, the sulphur based solution helps to passivate the surface by leaving a thin layer of sulphur behind. The various native oxide cleaning solutions are usually diluted in H_2O solutions:

HF [107, 140, 141]

HCl [105, 107, 116, 131, 137, 140]

NH_4OH [105, 108, 113, 116, 131, 140]

$(NH_4)_2S$ [105, 116, 131]

H_2SO_4:H_2O_2 [104]

Na_2S: C_3H_7OH [104]

A dry etch technique to remove the native oxide from the substrate is by exposing the sample to atomic H [137] leaving clean GaAs surfaces. However, extended exposure of atomic H might lead to reduction of the overall doping as the H passivates the Si donors in the n-type III-V material [223].

The substrate surface does not only contain a native oxide but it is also contaminated by various processing steps. These contaminants might not necessarily be affected by a wet etch clean. A UV/ozone surface cleaning technique can be used to deliberately oxidise the surface layer. This forms an oxide layer on top of the substrate and can be cleaned using conventional wet etch techniques [108, 113, 137, 140].

Depinning of surface

Fermi level pinning can be described by the theory of Metal Induced Gap States or MIGS [40] as explained in chapter 3.6.3. In a metal/semiconductor junction the free electron wave function can penetrate into the semiconductor bandgap. This generates gap states, which consist of donor and acceptor like states. There is a charge neutrality level in the bandgap where the gap-state charges are balanced. The metal Fermi level is pinned close to the charge neutrality level because of dipole formation. To prevent the Fermi level pinning the free electron wave function penetration has to be reduced. This can be done by introducing a thin dielectric layer. Si_3N_4 [105, 107, 131] has low dielectric constant and moderately high band gap to prevent the free electron wave function from penetrating into the semiconductor bandgap and hence releasing the Fermi level. Al_2O_3 [131] has also been reported to reduce the Fermi level pinning effects. Adding an additional layer of insulating

material will require the electrons to travel through the thin dielectric layer. This potentially causes additional resistance, increasing the specific contact resistivity value.

Regrown [119, 135, 137, 153]

When a semiconductor material is grown in an oxygen free environment, no native oxides can form. This is then the cleanest surface on which ohmic contacts can be deposited. However, processing requires lithography steps and source/drain contact definitions. The source/drain ohmic contact area will always be contaminated. A solution is to clean the surface and regrow semiconductor material in the source/drain area and in-situ deposition of a metal to form the ohmic contact. This will not only result in a very clean surface, also the doping concentration and In level can be altered, effectively reducing the bandgap and improving tunnelling probability.

Implantation [110, 123, 124, 125, 127, 128]

Implanting n- type species helps to reduce the Schottky barrier width by introducing local doping. The implantation of dopants into semiconductor material has two major disadvantages. One is the high activation temperature (> 800°C) of the Si atoms in III-V semiconductor materials. The other disadvantage is the large distribution of implanted atoms into the semiconductor material. The large distribution of atoms makes this an impractical technique when designing scaled CMOS devices.

6.2.2 Critical Issues

Apart from the standard factors that determine a good ohmic contact scheme, there are a number of factors that are specific to this project. Firstly the material used for III-V MOSFET has an oxide layer grown by MBE, MOCVD or ALD. The oxide has a certain temperature budget and will have to be removed in order to make ohmic contacts to the underlying GaAs/InGaAs semiconductor material. Since the technology for the ohmic contacts should be transferable to a 200mm processing environment using VLSI, there are some constraints on the metals and processes used. Ultimately, small contact geometries (<100nm) would be required for gate pitch scaling

6.2.2.1 Temperature budget

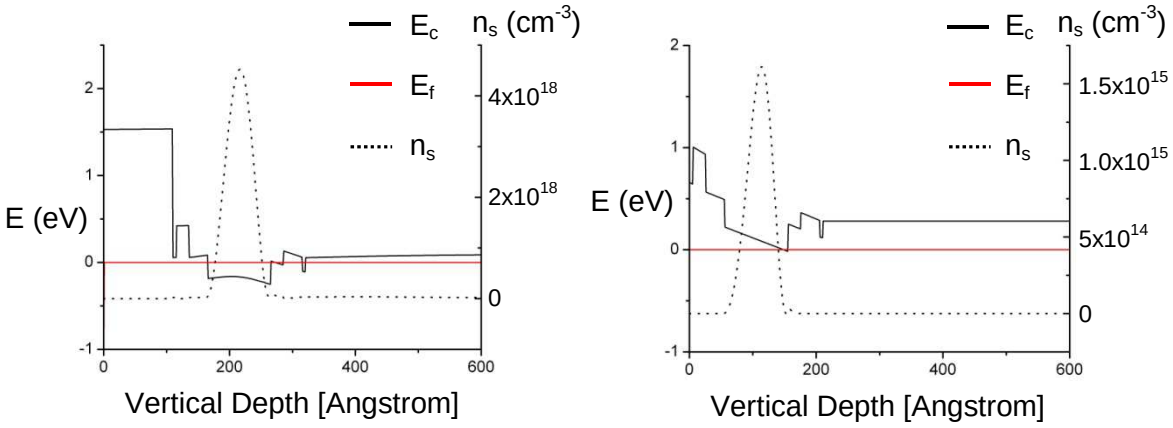
The III-V MOSFET device structure grown at the University of Glasgow uses a Ga_2O_3/GaGdO dielectric stack. This oxide dielectric stack has shown low interface state density and low gate leakage to GaAs and was therefore chosen as the oxide for GaAs-based III-V buried channel MOSFETs. The oxide stack is grown in a III-V MBE chamber

at around 460°C– 510°C for an amorphous deposition [101]. It is critical the dielectric oxide stack remains amorphous as the gate leakage increases and the permeability drops when the oxide stack becomes crystalline. This limits the annealing temperatures for any ohmic contacts to around a maximum 450°C.

The current tendency is to move away from the buried channel MOSFET device towards a high indium concentration surface channel device. The characteristics of a GaGdO stack on InGaAs are inferior to GaAs and alternative dielectric oxide stacks are used such as ALD grown Al_2O_3. The ALD gate dielectrics supplied by Stanford University have not been subjected to thermal budget tests and their maximum processing temperature is therefore unknown.

6.2.2.2 Oxide etching

The dielectric stack is grown uniformly on the wafer and has to be etched away in the source/drain region in order to make ohmic contacts. The etch of the gate dielectric needs to be well defined because the ohmic contact structure should not have any gap between the oxide or overlap the oxide. When there is a gap in the oxide the surface gets pinned mid gap in case of GaAs, which raises the conduction band from the channel. This moves the conduction band closer or above the Fermi level and limits the number of free electrons. The number of free electrons determines the maximum current and corresponding on-state device performance. In case of this band structure without the oxide the maximum electron concentration is $1.5x10^{15}$ cm^{-3}. From Figure 6.3 we can see that the electron concentration is a lot higher when there is an oxide ($>10^{17}cm^{-3}$), giving a lower sheet resistance for the access region in a buried channel device architecture.



a) Carrier concentration with GaO/GaGdO gate dielectric at V_g = 1.2V

b) Carrier concentration after removal of GaO/GaGdO gate dielectric

Figure 6.3: Carrier concentration distribution in GaO/GaGdO gate dielectric stack device material using Poison - Schrodinger simulation

When the contact structure overlaps the oxide the model becomes a bit more difficult. It's believed that there is a voltage difference between the channel and the contact metal. The electron concentration at the drain region can therefore increase and have essentially the same effect as the gate metal, which uses high metal work function metals to increase the carrier concentration. The detrimental effect is then more likely to take place at the source contact metal. The voltage difference between the contact metal and channel can then potentially reduce the electron carrier concentration or form a depletion region. The overlapping part may act as a negatively biased gate metal reducing the electron concentration in the channel and effectively increasing the sheet resistance in this region. Therefore, the gate dielectric has to be etched accurately to avoid increased sheet resistance in the access regions.

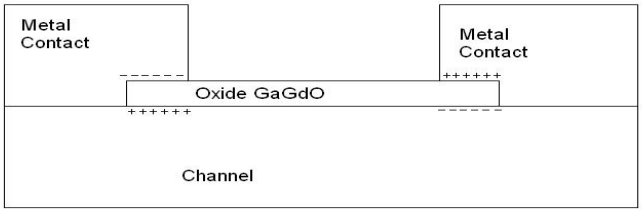


Figure 6.4: Charge effects due to ohmic contact overlap

6.2.2.3 Si Compatibility

The focus of the DualLogic activity in Glasgow is the n-type III-V transistor with particular emphasis on developing new gold free, low contact resistivity, ohmic contacts,

which are compatible with a silicon CMOS process flow. This requires the development of gold free ohmic contacts because gold is an amphoteric material in silicon, (the behaviour of gold is unpredictable in silicon and can act as both donor and acceptor). Also Ag and Cu are not Si-processing compatible metals however Cu is used in back end processing as interconnect wiring. The source/drain ohmic contact formation is a front end process and it's therefore impractical to use Cu as a possible source/drain ohmic contact metal. The MOSFET device structure was not finalized at this stage in the project and therefore corresponding processing including resists, masks, solvents and temperature budgets are not necessarily Si-processing compatible.

6.2.2.4 Scalability

When scaling MOSFET devices to sub 22nm technology generation, the ohmic contacts require good edge definition and little vertical and lateral alloying into the semiconductor material. Lateral alloying will result in poor yield and reproducibility, increased short channel effects and potentially a short circuit between source and drain. The ohmic contact structure thickness also has to be scaled as self aligned processing [202] requires thin source/drain regions in the region of 100nm or smaller. This is for a gate length of 40nm and further reducing of the gate will require thinner source/drain contact metals.

6.2.3 Comparison/Contact strategy

The choice of the best suitable ohmic contact is based on the III-V MOSFET device structure. The original device structure developed at the University of Glasgow in cooperation with Freescale Semiconductors is a flatband, buried channel device architecture. The oxide layer is a GaO/GaGdO layer, which will require etching prior to source/drain ohmic contact formation. Underneath the oxide there is a wide band gap undoped AlGaAs layer. Unless the ohmic contact strategy features significant alloying, the ohmic contact will form a Schottky barrier on the metal/semiconductor interface of the wide bandgap layer. Since the wide bandgap layer is undoped, tunnelling effects are going to be minimal and the Schottky barrier height will dominate the quality of the ohmic contact. It would thus be beneficial to use an ohmic contact strategy that increases doping levels and/or reduces the band gap. There are two different buried channel device structures used, which are both listed in the materials section in the appendix. One structure is GaAs-based with a wide bandgap structure ($Al_xGa_{1-x}As$) and a $In_{0.3}GaAs$ channel and the second structure is InP-based with a wide bandgap structure ($In_xAl_{1-x}As$) and a higher indium concentration $In_xGa_{1-x}As$ ($x \geq 0.53$) channel.

The ohmic contact strategy previously used at the University of Glasgow is NiGeAu based, which allows for lateral alloying due to the spiking behaviour. This has the advantage that the metal/semiconductor interface is positioned in the channel, taking advantage of the lower band gap of $In_{0.3}GaAs$. However, the purpose of this project is to develop an ohmic contact strategy, which is compatible with Si processing. Metals such as Au, Ag and Cu cannot be used as an ohmic contact, which significantly reduces the numbers of suitable candidates such as NiGeAu, CuGe, and NiGeAg.

The second limitation is the temperature budget with a maximum limit at 450°C. This limits the use of indium base contacts as In starts forming $In_xGa_{1-x}As$ at temperatures around 600°C. The high melting points of refractory metals prevent alloying below 450°C. This limits the possible ohmic contacts from the literature to the following metallisation, as shown in Table 6.6 [6] for GaAs.

Metallisation	Anneal (optimal temperature)	Doping (cm^{-3})	ρ_c ($\Omega.cm^2$)	R_C (Ω.mm)	Ref.
Pd/Ge	325°C 30min	$1.00x10^{+18}$	$1\text{-}3x10^{-6}$		[144]
Pd/Si	375°C 30min	$1.00x10^{+18}$	$2\text{-}6x10^{-6}$		[145]
Pd/In/Ge	400°C	$1.00x10^{+18}$	$6.00x10^{-7}$		[165]
In	375°C	$2.00x10^{+16}$	$3.00x10^{-6}$		[177]
Pd/Ge			$4.00x10^{-7}$		[179]
Pd/Sn	360°C	$2.00x10^{+18}$	$3.00x10^{-5}$		[180]
Pd/Sn,			$8.00x10^{-6}$ –		
Pd/Sn/Au	360°C-430°C		$3.00x10^{-5}$		[181]
Pd/Ge/Ti/Pt	400°C		$2.40x10^{-6}$		[183]
			$2.40x10^{-6}$ –		
Pd/Ge/Ti/Pt	380°C-450°C	$6.00x10^{+17}$	$5.30x10^{-6}$		[184]
Pt/Ti/Ge/Pd	400°C	$5.00x10^{+18}$	$5.00x10^{-7}$		[187]
Pd/Ge	320°C 60s	$3.70x10^{+18}$	$1.00x10^{-5}$		[189]
Pd/Ge	317C	$7.00x10^{+16}$			[138]
Pd/Ge	325°C 30min	$4.00x10^{+18}$	$9.00x10^{-7}$		[103]
Pd/Si	375°C 30min	$4.00x10^{+18}$	$2.00x10^{-6}$		[103]
Ge/Pd/Ti	380°C	$2.00x10^{+18}$	$8.50x10^{-7}$		[114]
Pd/Ge	400°C	n/a	$9.80x10^{-6}$	0.29	[116]
Al	Non Alloyed	$5.00x10^{+15}$	$5.00x10^{-6}$		[125]
Ge/Pd	400°C	$1.00x10^{+18}$	$2.00x10^{-4}$		[130]

Table 6.6: Summary of Si-processing and III-V MOSFET processing compatible ohmic contact strategies

The PdGe based ohmic contact seems to have low specific contact resistivity [179], ideal temperature window and is compatible with Si processing. This ohmic contact strategy has then been used experimentally to form source/drain ohmic contacts to a III-V MOSFET

During the project, new developments such as regrowth allowed the device structure to change to a surface channel device structure. This reduced a number of constraints. When regrowing is possible, doping can be increased to $1x10^{20}cm^{-3}$in source/drain regions and the indium content in the InGaAs compound can be gradually increased. Because of the increased doping, there is no longer a need for alloyed contacts, which usually have bad surface morphology and temperature budget. Since regrowing is not possible at the University of Glasgow, wafers with highly doped $1x10^{19}cm^{-3}$ Si $In_{0.53}GaAs$ surface material have been used instead. High doping and material with low bandgap should allow for ohmic contacts with low specific contact resistivity values. Potential suitable ohmic contacts for a Si compatible process using regrowth ohmic contacts are shown in Table 6.7.

Metallisation	Anneal (optimal temperature)	Doping (cm^{-3})	Substrate	ρ_c ($\Omega.cm^2$)	Ref.
Pd/Si/Ti/Pt	425°C		InGaAs	$1x10^{-6}$ – $2x10^{-6}$	[121]
Pd/Ge/Ti/Pt	400°C		InGaAs	$3.70x10^{-6}$	[117]
Wnx/WN0.5x/W	400°C		InGaAs	$2.00x10^{-7}$	[139]
Mo	n/a	$5.00x10^{+19}$	$In_{0.53}GaAs$	$1.00x10^{-8}$	[137]
Mo	n/a	$3.60x10^{+19}$	InGaAs	$1.30x10^{-8}$	[200]
TiW/Ti/Ni	Non Alloyed	$3.50x10^{+19}$	$In_{0.53}GaAs$	$8.40x10^{-7}$	[108]
Pd/Ge/Ti/Pt	400°C 10s	$1.00x10^{+19}$	$In_{0.50}GaAs$	$3.70x10^{-6}$	[112]
ErAs	n/a	n/a	InAs	$1.50x10^{-8}$	[113]
Mo	n/a	n/a	InAs	$5.00x10^{-9}$	[113]
TiW	n/a	n/a	$In_{0.53}GaAs$	$7.00x10^{-9}$	[113]
Al	Non Alloyed	$3.00x10^{+19}$	$In_{0.50}GaAs$	$4.80x10^{-7}$	[135]
ErAs	350°C	$9.00x10^{+18}$	InGaAlAs	$1.50x10^{-7}$	[219]

Table 6.7: Summary of Si-processing and source/drain regrowth compatible ohmic contact strategies

6.3 Experimental

This section is split up in three main parts, which covers alloyed and non alloyed ohmic contacts and MOSFET device results. The alloyed ohmic contact section is split up in two parts where the first part studies the chemical and electrical properties of a PdGe-based ohmic contact using a wet etch surface clean technique whereas the second part studies the use of alternative dry etch gate dielectric removal techniques in order to build scalable source/drain ohmic contacts to III-V MOSFET devices. The non-alloyed ohmic contact

section investigates the electrical properties of both e-beam evaporated and sputtered metals on $1x10^{19}cm^{-3}$ Si doped $In_{0.53}GaAs$. The MOSFET device section features the results of both buried channel and surface channel device architectures.

Previous to this work the foundations of GaAs-based buried channel MOSFETs with Ga_2O_3 or GaGdO gate dielectrics were developed by R. Hill and D. Moran. The work included the design of the buried channel, quantum well, layer structure, the choice of the oxide and its thickness, source/drain ohmic contacts including an oxide etch process, gate metal and various processing steps to build a device. The optimal way to deposit a semiconductor/oxide interface with a low density of states was found to be in-situ growth of AlGaAs/InGaAs/GaAs layer structures and GaGdO layer by MBE epitaxy without breaking vacuum. This means that the gate dielectric is present on the wafers with a buried channel architecture and therefore the insulating oxide layer has to be removed in order to make source/drain ohmic contacts to the underlying semiconductor material.

The process used to remove the oxide layer should not influence the underlying semiconductor material, resulting in a clean metal/semiconductor interface. There are two approaches that can be used to etch the oxide layer: a wet etch process and a dry etch process. The wet etch has been previously optimised by comparing different solutions of HF and HCl. The optimal wet etch found for a GaGdO gate dielectric is an $HCl:H_2O$ 1:100 solution. A 30s etch time results in a 10nm oxide etch with minimal (<100nm) lateral etch. The dry etch techniques previously tested are a methane:hydrogen/oxygen etch, an Ar plasma etch and an Ar ion gun. These had their disadvantages; residual layers for the methane: hydrogen/oxygen and re-deposition and damaging effects for the Ar plasma and ion gun. The current dry etch strategy uses a RIE etch with an ionised $SiCl_4$ gas as described in the fabrication chapter.

As source/drain ohmic contacts, NiGeAu and PdGe metal stacks have been researched by R. Hill. The measurements were all taken by making use of TLM structures. It was found that the Pd/Ge (50nm/50nm) contact was inferior to the AuGeNi contact and has thus been dropped. The optimal contact strategy was found to dependent on the gate dielectric removal technique, as shown in Table 6.8.

	Layer Structure	Optimal Anneal
NiGeAu (wet etch)	Ni/Ge/Au 20/20/200nm	360ºC 60s
AuGeNi (dry etch)	Au/Ge/Au/Ge/Au/Ni/Au 10/10/10/10/20/11/80nm	420ºC 60s

Table 6.8: Optimised Ni/Ge/Au based ohmic contacts for GaO/GaGdO gate dielectric stack device material use dry or wet etch

The MOSFET device material is not grown as a part of Duallogic, but borrowed from EPSRC funded work. This means there is a limited supply of actual MOSFET device material for this project. The various device layer structures are indicated by the first character as follows; "x" is a Glasgow grown structure with a GaGdO gate dielectric stack, "c" is a Glasgow grown structure, which may or may not have a gate dielectric and "6-" is a Freescale grown structure with a GaGdO gate dielectric stack. If a gate dielectric has been deposited on a c-wafer, it will have been deposited at Stanford University by ALD. The wafers grown at IMEC under the Duallogic project are indicated with "IM" followed by the material type. The full material layer structures can be found in the materials section in the appendix

In order to cover for HEMT-like device structures and MOSFETs with regrown source/drain areas, specific highly doped wafers were grown. This also allows for a comparison between results from literature, which use highly doped surface layers. Four types of wafers were grown: one wafer with highly doped GaAs surface (IM-GaAs), one wafer with a 500nm thick $1x10^{19}cm^{-3}$ Si doped $In_{0.53}GaAs$ layer at the surface (IM-InGaAs500), several wafers with a 20nm thick $1x10^{19}cm^{-3}$ Si doped $In_{0.53}GaAs$ at the surface (IM-InGaAs20) and two wafers with a 2.5nm thick $1x10^{19}cm^{-3}$ Si doped InAs layer at the surface (c760,c783). The IM-InGaAs20 wafer has an $In_{0.52}AlAs$ layer, which acts as a barrier and allows for isolation and mesa etching, which is not possible with the other wafers.

Over the period of this project, an InP-based structure with $In_{0.53}GaAs$ channel and ALD (Chapter 4.2.2) deposited Al_2O_3 from Stanford University was developed. The advantage of this structure is the high indium concentration of the channel material resulting in high mobility. The ALD Al_2O_3 oxide etch has been optimised by S. Bentley using dilute KOH and the ohmic contacts used are Ni/Ge/Au-based. The annealing cycle used is 280°C 60s, this limits the lateral alloying of Ni/Ge/Au-based ohmic contacts by keeping the alloy

under its eutectic temperature. This allowed for the study of scaled MOSFET devices, but it potentially has a detrimental effect on the contact resistance as there will be little additional doping into the semiconductor as the eutectic temperature has not been reached (chapter 6.2.2). The full material layer structures can be found in the materials section in the appendix.

TLM structures (chapter 5.3.2) were used as a test structure with gap sizes of 2,4,6,8 and 10µm and do not feature an isolation etch. On average 4-8 TLM structures were measured and the results were then analysed using excel. The excel file extrapolates the results for the R_C and L_x value, as shown in figure 5.9, using the "LINEST" function. The excel file also returns the correlation, R_{sh}, ρ_c and L_T values and the respective averages and standard deviation.

6.3.1 Alloyed Contacts

6.3.1.1 Wet Etch

Pd/Ge/Pd/Ti/Au on x238 device material

After making a comparison of the various ohmic contact strategies, a metallisation based on the work by I.H. Kim [112] was explored. The Pd/Ge/Pd/Ti/Au (50/120/50/35/35nm) metallisation was chosen because it featured a specific contact resistivity of $1.0x10^{-6}\Omega.cm^2$ and the Pd, Ge, Ti, Au metals were available in the Plassys 1 metal deposition tool chapter 4.5.1. Optimal anneal temperature range was chosen based on literature review [112]. In parallel an XRD study was carried out at IMEC, which indicated low resistivity phases are formed starting from 300ºC annealing temperatures.

A Pd/Ge/Pd/Ti/Au contact was then made using an e-beam evaporator and lift-off to x238 device material and the annealing temperature was based on the best temperature of 400°C in literature [112]. The annealing time was varied from 10s to 60s. An $HCl:H_2O$ oxide etch of 15s was used based on previous work. To determine the optimal oxide etch time a separate oxide etch test was carried out using a NiGeAu contact structure and the optimal etch time was then found to be 30s.

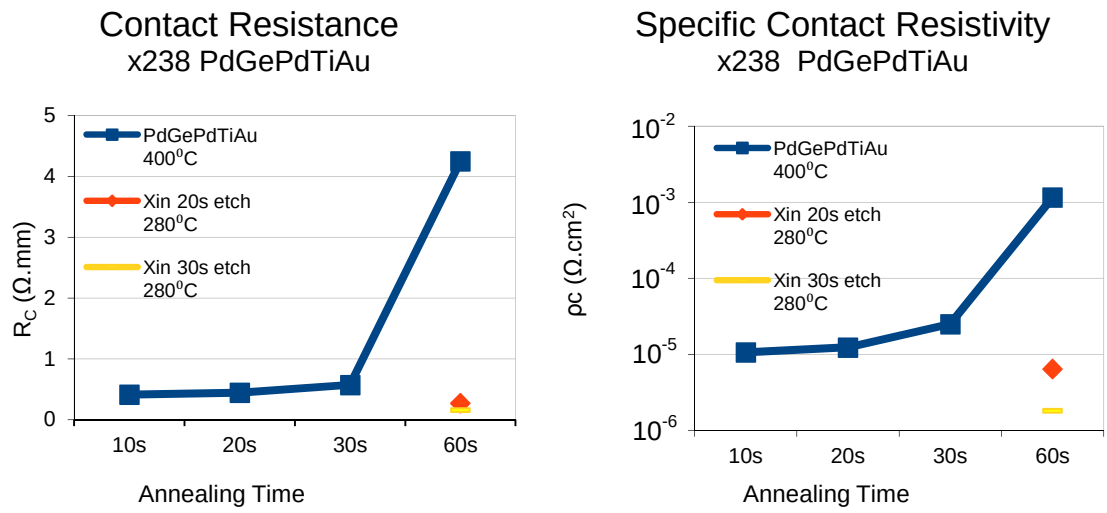


Figure 6.5: Comparison between a Pd/Ge/Pd/Ti/Au annealed at 360°C for 10s, 20s, 30s and 60s and AuGeNi ohmic contact structure on x238 device material.

The lowest contact resistance and specific contact resistivity values are found for an annealing time of 10s, which agrees with previously published data [112]. However, the specific contact resistivity is one order larger than the values found in [112]. The main reason for the higher specific contact resistivity values is the difference in semiconductor material used in comparison to previous work [112]. The Pd/Ge/Pd/Ti/Au is deposited on a narrow bandgap $1x10^{19}cm^{-3}$ doped $In_{0.5}GaAs$ wafer [112] in comparison to the MOSFET device layer structure, which features an oxide and a wider, undoped bandgap material underneath the oxide. A non-optimised oxide etch is one potential cause of a higher specific contact resistivity as explained in chapter (6.2.1). A second potential cause is the actual metal/semiconductor interface. This depends on the vertical alloying properties of PdGe on the device material. The top layer is an undoped wide bandgap material, whereas the channel is an $In_{0.75}GaAs$ narrow bandgap material in the case of the x238 layer structure. If there is little vertical alloying the metal/semiconductor interface will take place on wider bandgap GaAs or InAlAs material resulting in an increased specific contact resistivity compared to the narrow bandgap material in the channel. The lower specific contact resistivity for the NiGeAu is then largely due to the fact that because of significant alloying, the metal/semiconductor barrier actually forms in the channel. This suggests that there is little alloying in the semiconductor material from the PdGe contact. In this case, the contact performance should be compared to similar undoped material and the closest semiconductor material found in literature featuring a PdGe based ohmic contact is $1x10^{16}cm^{-3}$ doped GaAs [102]. The PdGe contact is annealed at 550°C giving a specific

contact resistivity of $3.5x10^{-4}\Omega.cm^2$. This is one order higher than the Pd/Ge/Pd/Ti/Au contact, indicating that the contact potentially alloys through the 2 monolayers of GaAs and forms an ohmic contact on narrower bandgap material.

So far, only the annealing time has been adjusted, while the XRD study performed at IMEC by A. Firrincielli suggests that ohmic contacts can be made at temperatures above 300°C. The time is still kept to 10s for direct comparison to previous results and the annealing temperatures have a very coarse scale of starting from a non annealed contact to an annealing temperature of 420°C, as shown in Figure 6.6. This temperature range was also based on results from [112] as an optimal window to show the relation between temperature and ohmic contact formation. The HCl:H_2O oxide etch time was adjusted to the best result for NiGeAu etch to 30s.

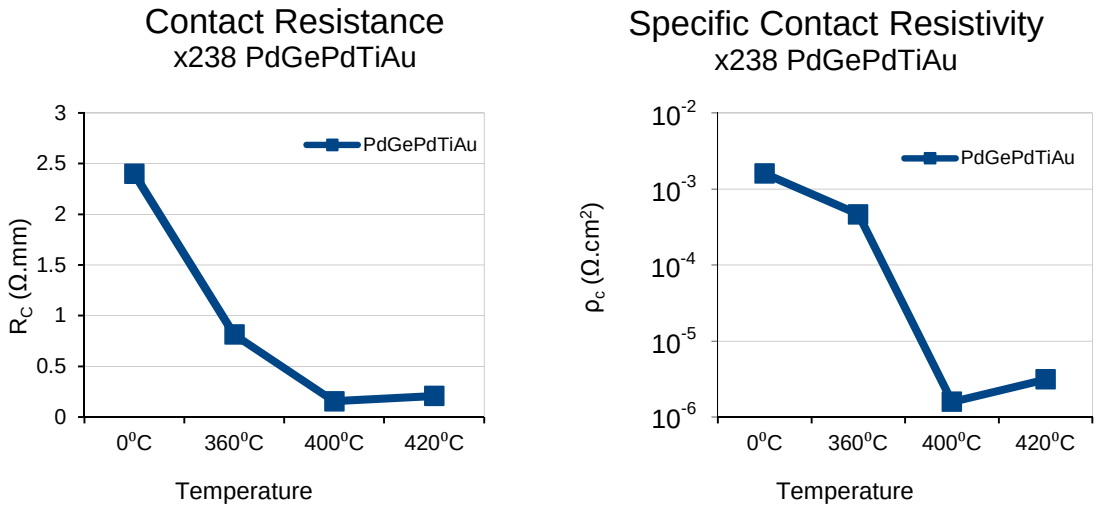


Figure 6.6: TLM results of a Pd/Ge/Pd/Ti/Au ohmic contact structure on x238 device material annealed for 10s at 0°C, 360°C, 400°C and 420°C.

The annealing temperature of 400°C confirms the lowest specific contact resistivity and the non annealed contact showed non ohmic behaviour. Changing the etch time resulted in a specific contact resistivity of $1.58x10^{-6}\Omega.cm^2$. This is better than the NiGeAu contact that had been optimised before and the PdGe work previously done before and comes very close to the work done in [112].

Pd/Ge/Pd/Ti/Au vs. Pd/Ge/Ti/Pt on highly doped IM-InGaAs500

Checking the effect of highly ($>1x10^{18}cm^{-3}$) doped low bandgap material used in the literature, a $1x10^{19}cm^{-3}$ Si doped $In_{0.53}GaAs$ layer of 500nm thick on InP substrate was

used. The optimal anneal (400°C 10s) was based on previous work on x238 device material. The sample had no oxide grown and thus no etch/clean was used. The Pd/Ge/Pd/Ti/Au structure previously used, yielded the result shown in Table 6.9:

Substrate	Metallisation	R_C (Ω.mm)	R_{sh} (Ω.sq)	ρ_c (Ω.cm^2)	Correlation
IM-InGaAs500	Pd/Ge/Pd/Ti/Au	0.01	0.31	2.77x10^{-6}	0.98

Table 6.9: TLM result of a Pd/Ge/Pd/Ti/Au ohmic contact structure on highly doped GaAs.

The sheet resistance of the material is very low making it hard to extract a precise result for the specific contact resistivity because of the poor correlation between different data points. A specific contact resistivity of 2.77x10^{-6}Ω.cm^2 is higher than previously recorded on x238. This might be due to the TLM measurement, but could also be due to the fact that there has not been a native oxide clean.

So far, the ohmic contact structure featured a layer of Au, which makes this contact scheme incompatible with Si processing. The choice was then made to investigate a Pd/Ge/Ti/Pt (50nm/120nm/35nm/35nm) structure also described in [112]. Slightly elevated specific contact resistivity values are to be expected as the lowest specific contact resistivity in the paper [112] was reported to be 3.7x10^{-6}Ω.cm^2 compared to the 1.1x10^{-6}Ω.cm^2 from Pd/Ge/Pd/Ti/Au. To make the Pd/Ge/Ti/Pt contact the sample had to be transferred from one deposition tool to the other after depositing the PdGe layers as the Plassys 1 deposition tool does not contain Pt. The exposure to air could have detrimental effects on ohmic contact behaviour as the Ge layer can oxidise.

The Pd/Ge/Ti/Pt was first tested on was the highly doped $In_{0.53}GaAs$ material. This formed ohmic contacts with similar values as Pd/Ge/Pd/Ti/Au. But the variability between contact measurements was far greater than the increase in sheet resistance of TLM's with 2,4,6 and 8µm gap sizes. The measurements of the total resistance between contact pads are in the same order as the Pd/Ge/Pd/Ti/Au contact but exact numbers for the sheet resistance and specific contact resistivity cannot be extracted due to poor correlation (<0.9) between the measured data.

EELS analysis on Pd/Ge/Ti/Pt on IM-InGaAs500

In order to understand the Pd/Ge/Ti/Pt contact formation on doped $In_{0.53}GaAs$, a scanning transmission electron microscopy ((S)TEM) and electron energy loss spectroscopy (EELS) investigation was carried out at the physics department at the University of Glasgow. The PdGe ohmic contact is based on a solid state reaction where Ge diffuses through the Pd layer into the $In_{0.53}GaAs$ layer occupying preferentially Ga sites n-type doping the substrate. The thickness of Pd and Ge are chosen in a way that there is an excess of Ge to provide for the Pd_2Ge formation and Ge penetration into the InGaAs. The Ti/Pt layer acts as a barrier for outdiffusion. The TEM micrographs give an insight into the morphology and layer structures, but chemical analysis is required to find the profile of the various elements in the contact structure. The chemical analysis has been done using EELS [201]. This is a powerful characterisation technique where a mono-energetic beam of electrons is directed at the sample and the composition of the material is obtained by the loss in energy of the electrons after the beam interacts with the sample.

Before EELS and TEM can be used, small samples have to be extracted from the processed substrate. For this reason, the substrates containing the TLM structures also feature small gratings, which are 2μm wide and 2μm apart. This allows for multiple samples to be taken from a single grating structure. The samples go through a specimen preparation that involves: cutting, grinding, dimpling and ion milling the sample. The sample preparation is a corrosive process and the substrate and contacts have to be covered with a 100nm layer of Si_3N_4 to give protection from sample preparation damage.

The recipe for the metals is Pd 50nm Ge 120nm Ti 35nm Pt 35nm, analysing the TEM micrograph Figure 6.7a of the unannealed contact showing the as-deposited metal layers, the actual thickness for the metals are: Pd 70nm, Ge 100nm, Ti 30nm, Pt 40nm. The unannealed sample does not show any signs of major reactions between the substrate and the whole contact region with amorphous Pd and Ge layers. The ohmic contact results showed non ohmic behaviour when the contact is not annealed suggesting an ohmic contact can only be formed after a solid state reaction has taken place.

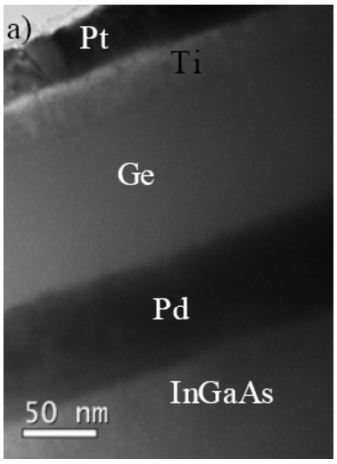


Figure 6.7: TEM micrograph of the ohmic contact stack: a) unannealed sample; b) annealed sample (400°C 10s)

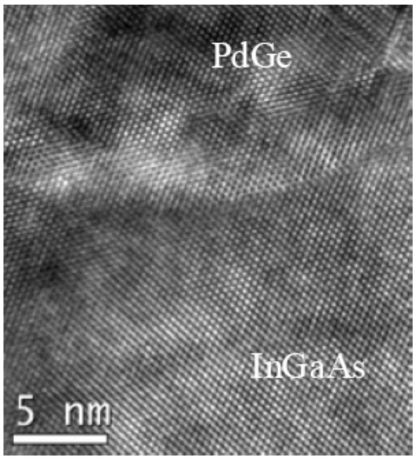


Figure 6.8: High-resolution TEM image of the interface region in the annealed sample (400°C 10s)

The contact after annealing, Figure 6.7b, still has clearly distinguishable Ti and Pt layers, but the Pd and Ge layers have reacted to form a Pd_2Ge granular structure. Some amorphous Ge remains at the Ti interface, and there is an indication of a reaction between Ge and Ti at the interface forming a slightly darker region underneath the Ti layer on the TEM micrograph. The interface layer between the substrate and the contact is no longer smooth. To look into the roughness of the sample a high magnification image was taken of the interface Figure 6.8. By making use of image masking and applying a FFT based filter a crystallised area has been detected at the interface region with the same orientation as the $In_{0.53}GaAs$ material. The crystalline material is most likely Ge that has been regrown on the substrate by solid phase regrowth as suggested by the theory. To examine if solid phase regrowth has taken place, a chemical analysis has been performed on the $In_{0.53}GaAs$/Pd/Ge interface using EELS Figure 6.10.

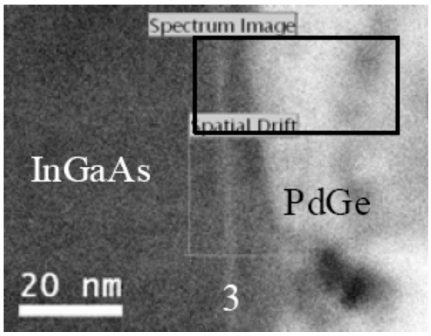


Figure 6.9: ADF STEM survey image of the annealed InGaAs sample with Pd/Ge/Ti/Pt ohmic contact structure.

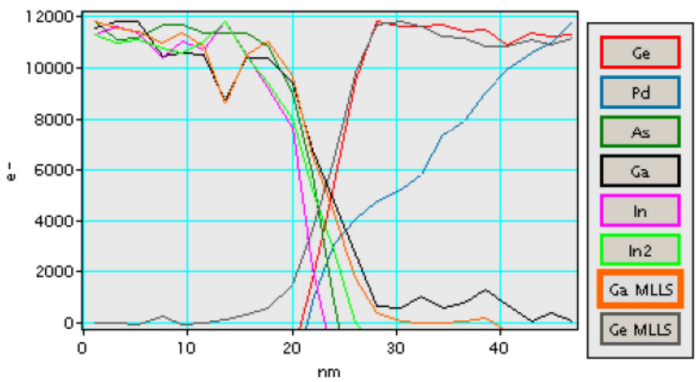


Figure 6.10: Normalised EELS edge intensity profiles, extracted from the region in the black box.

The edge intensity profile of Ge, Pd, As, Ga and In have been extracted for a given area, obtained by annular dark field scanning electron microscopy (ADF STEM), as shown in Figure 6.9 by a black box. A multiple linear least square (MLLS) fit method has also been applied to Ga and Ge to reduce background noise. The normalised spectrum shows that Ge has either directly penetrated the Pd layer or propagated along grain boundaries and diffused into the $In_{0.53}GaAs$ more strongly than the Pd. Ga, In and As have diffused into the contact region with Ga propagating further. Also a 2nm In rich and Ga deficient layer, indicated with "3" on Figure 6.9, has been detected. This is possibly due to Ga diffusing into the PdGe contact creating vacancies of Ga in the $In_{0.53}GaAs$ layer. The diffusion of Ge into the $In_{0.53}GaAs$ substrate potentially n-type dopes the substrate, however the Ga diffusion into the contact might create a PdGa compound, which is a p-type dopant in Pd_2Ge. The excess of Ge over Pd at the interface also indicates that the crystalline material is effectively regrown Ge.

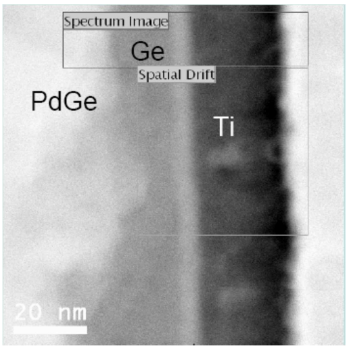


Figure 6.11: ADF STEM survey image of Ti/Ge interface. Black box is the area for acquisition of the EELS intensity edge profiles

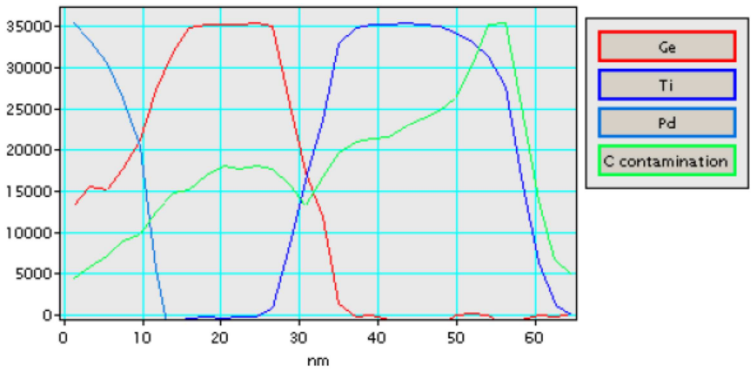


Figure 6.12: Normalised EELS edge intensity profiles, extracted from the region in the black box

The TEM micrograph Figure 6.7b and 6.11 indicate that the Pt and Ti layers have not diffused and can be used as capping material. However, there seemed to be a transition zone between the Ti and Ge layer that needed some further exploring. A high magnification image was taken and EELS analysis was performed to monitor the Ge levels in the Ti barrier layer, as shown in Figure 6.12. The normalised edge intensities have been extracted and it effectively shows the Ge has penetrated into the Ti layer. However, there is little diffusion throughout the Ti layer indicating the Ti layer is a good barrier from Ge out diffusion. Low Pd concentration near the interface layer confirms a residual amorphous layer, which has not reacted with the Pd.

In order to gain more understanding of how the alloy aids the formation of an ohmic contact two separate samples were made. The Pd and Ge layer, which form the solid phase

reaction were split and were deposited individually on the $In_{0.53}GaAs$ substrate. A TiPt layer was kept to protect the two samples from the TEM sample preparation. The sample with the 120nm deposited Ge layer had a respective TEM measured metal stack of: Ge 100nm, Ti 30nm, Pt 40nm. The other sample with the 50nm deposited Pd layer had a respective TEM measured metal stack of: Pd 70nm, Ti 30nm, Pt 40nm. Both metal stacks had one unannealed sample and one 400 C 10s annealed sample to compare the results with the Pd/Ge/Ti/Pt ohmic contact. Both samples were then investigated using TEM

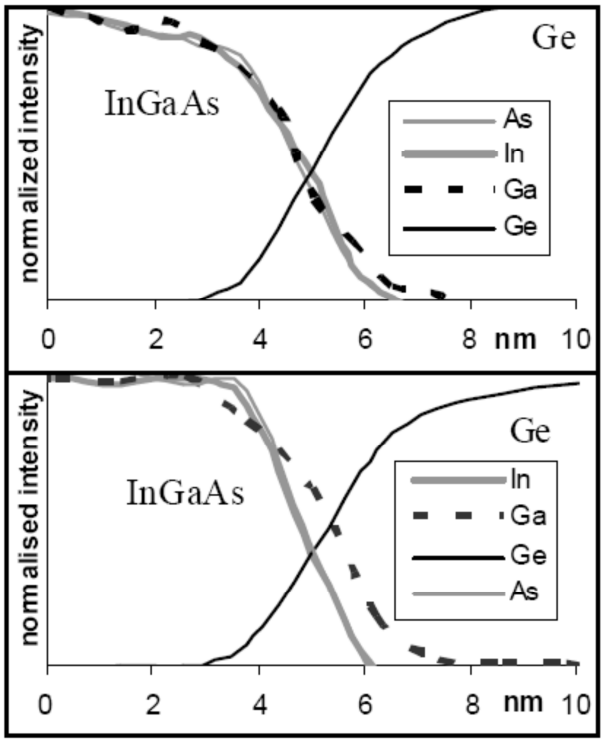


Figure 6.13: EELS edge intensity profiles extracted from the interface region in the Ge only sample: (a) top, unannealed; (b) bottom, annealed.

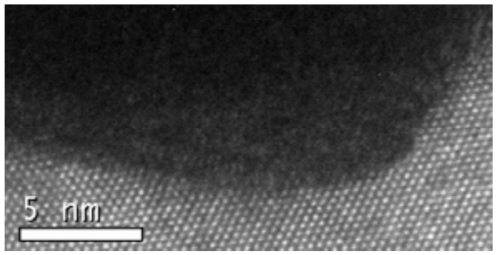


Figure 6.14: 7 High-resolution TEM image of the interface with the substrate in the annealed Pd only sample.

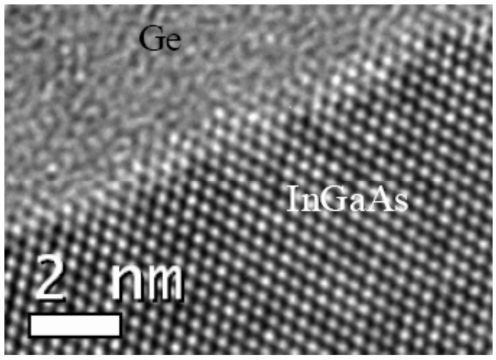


Figure 6.15: High-resolution TEM image of the interface region in the Ge only annealed sample.

micrographs and EELS analysis.

The interface between the substrate and Ge, as shown in Figure 6.15, appears to be smooth in both annealed and unannealed case. The In, Ga, Ge, and As edge intensity profile, as shown in Figure 6.13, indicates that the annealing process has not caused any major variations in morphology or chemistry. The In, Ga and As profile lines in the unannealed sample (Figure 6.13a) drop off together and symmetrically in respect to the Ge profile line. There seems to be little or no interpenetration from Ge into $In_{0.53}GaAs$. The Ga profile in the annealed sample (Figure 6.13b) appears to diffuse further into the Ge layer, potentially causing p-type doping. However, it's not clear if Ge has diffused into the $In_{0.53}GaAs$ layer.

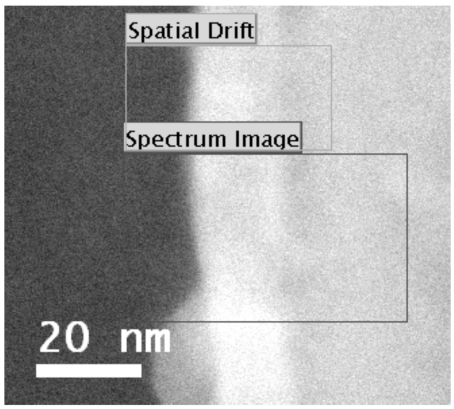


Figure 6.17: ADF STEM survey image used for the acquisition of the EELS edge intensity profiles in the annealed Pd only sample.

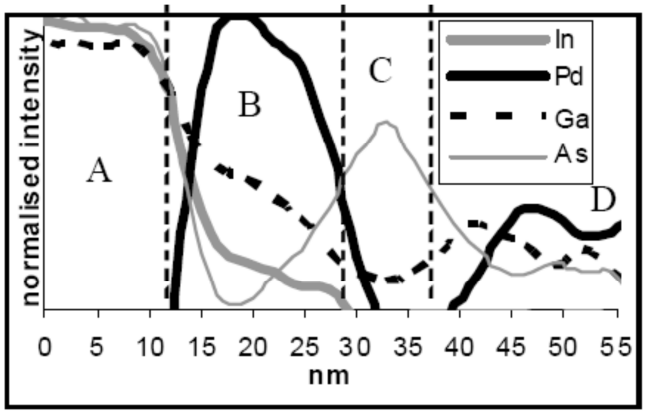


Figure 6.16: Edge intensity profiles extracted from the selected region in Figure 6.17.

The interface between the InGaAs substrate and Pd layer, as shown in Figure 6.17, is fairly sharp but rough with granular structures, which are most likely Pd. The In, Pd, Ga and As edge intensity profiles are presented in Figure 6.16 and show the penetration of In, Ga and As into the Pd layer. The As and Ga layer have penetrated throughout the Pd where the In layer only penetrates through region B. The regions are divided up as follows:

A) $In_{0.53}GaAs$ Substrate

B) High Pd concentration layer with significant Ga and little In

C) As rich layer

D) Mainly Pd with only Ga and As extending up to the Ti layer

The reaction between Pd and $In_{0.53}GaAs$ is relatively complex, but it seems to aid the diffusion of various elements. This is possibly due to the Pd_4GaAs phases that are formed during annealing as described in the theory. The Pd layer may then act as a metallic transport medium for Ge, which was previously suggested by T. Sands et al. [224].

The TEM and EELS analysis confirms the solid state reactions, which are described in the theory. There will be a competition between the interaction of Ge and $In_{0.53}GaAs$ with Pd. There is proof of Ge diffusing into the $In_{0.53}GaAs$ layer effectively n-type doping the substrate. There also seems to be Ga out diffusion into the contact, which could p-type dope the ohmic contact. This would be detrimental for the performance and might explain the inferior performance compared to the NiGeAu ohmic contact. Also Ti proves to be an excellent barrier layer to prevent Pt reacting with the underlying metals and substrate.

Pd/Ge/Ti/Pt on x266 device material

Given the fact that the Pd/Ge/Ti/Pt had ohmic contact behaviour, a study of the Pd/Ge/Ti/Pt contact stack was undertaken on MOSFET device material. Since the x238 material had been used up, a new wafer was used: x266. Although both have a buried channel layer structure, the In concentration in the channel is lower for x266 material and therefore the material underneath the oxide is wider bandgap $Al_{0.45}GaAs$ instead of $In_{0.52}AlAs$. The oxide etch characteristics of this wafer were first verified with the standard NiGeAu recipe annealed at 360°C 60s and the results are shown in Figure 6.18.

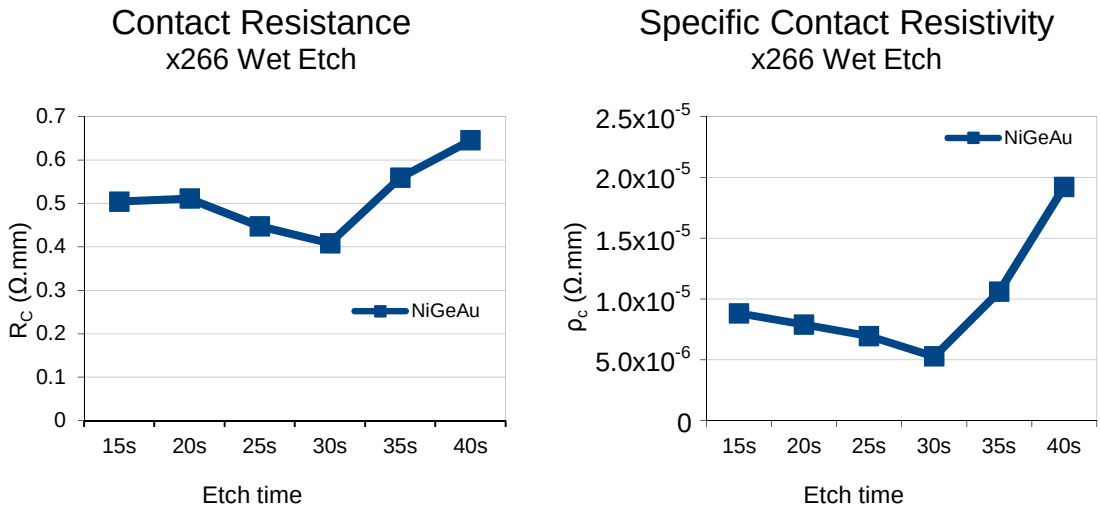


Figure 6.18: Wet etch test on x266 device material using standard NiGeAu ohmic contact

Optimal oxide etch for a HCl:H_2O 1:100 solution was found to be 30s. A Pd/Ge/Ti/Pt ohmic contact structure using a 30s oxide etch and lift off was then subjected to a temperature test and compared to a NiGeAu ohmic contact structure on the same x266 substrate material. The NiGeAu contact parameters were measured as a part of the characterisation of MOSFET devices. The processing of these devices featured a process where the gate was deposited prior to the ohmic contacts (GF) and a process where the gate was deposited after the ohmic contacts (GL). The temperature range of the Pd/Ge/Ti/Pt was varied from 360°C to 420°C based on previous results, as shown in Figure 6.19.

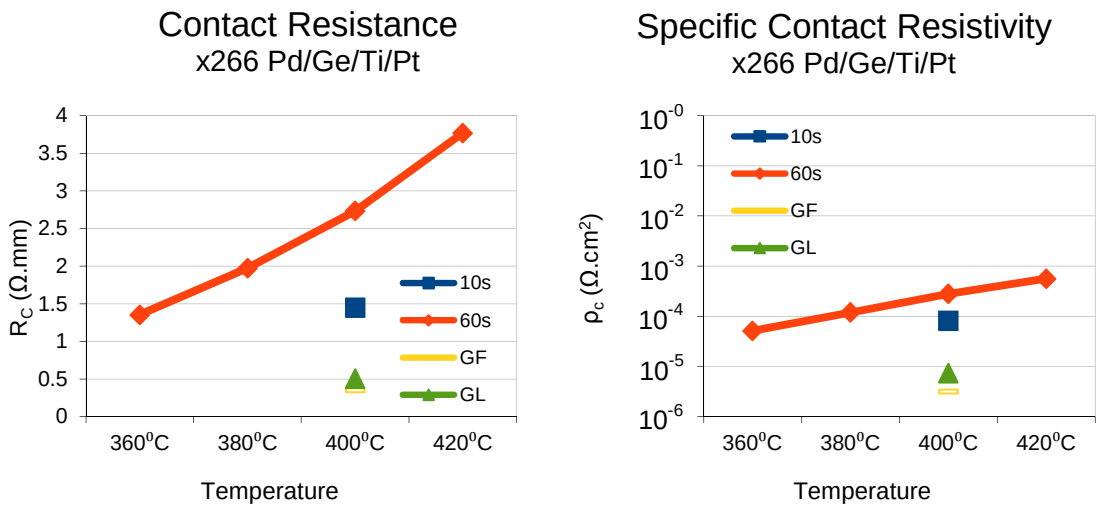


Figure 6.19: TLM results of a Pd/Ge/Ti/Pt ohmic contact structure on x266 device material annealed for 60s at 360°C, 380°C, 400°C and 420°C and for 10s at 400°C.

The 360°C 60s anneal shows slightly better results than the previous best anneal established at 400°C 10s. It was then chosen to do a time test for 360°C, as shown in Figure 6.20. However, looking at the temperature window, the contacts resistance is still on a descending trend at 360°C and potentially better ohmic contacts can be made at lower annealing temperatures.

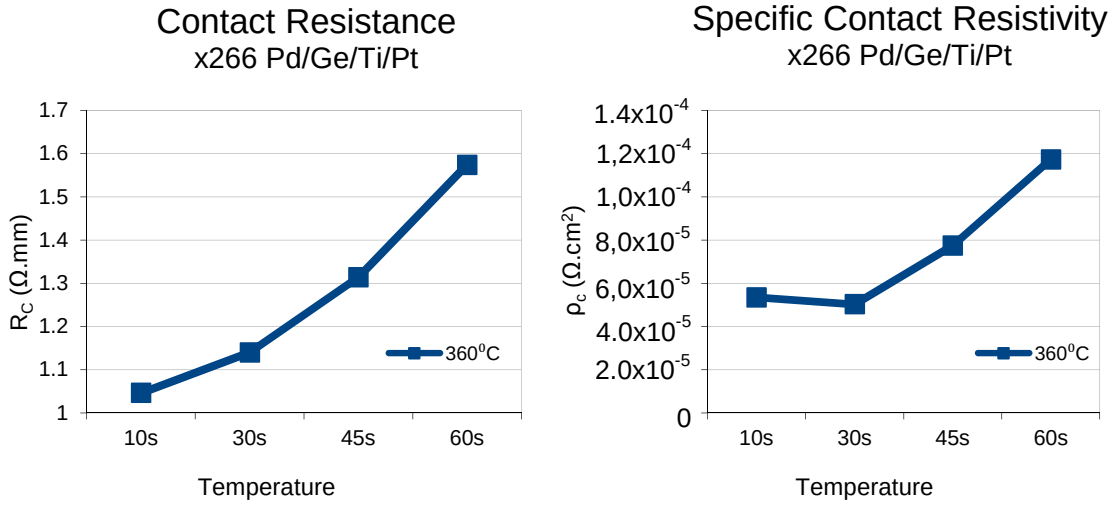


Figure 6.20: TLM results of a Pd/Ge/Ti/Pt ohmic contact structure on x266 device material annealed at 360°C for 10s, 30s, 45s and 60s

The R_C value would indicate that the 10s anneal is the best result. But the specific contact resistivity is the actual parameter indicating the quality of the metal/semiconductor barrier and the 30s anneal features the lowest specific contact resistivity. The results are

effectively one order of magnitude higher than the NiGeAu results and over one order of magnitude lower than the x238 Pd/Ge/Pd/Ti/Au results. However, the layer structure varies greatly between x238 and x266 and the results cannot be compared directly as the x266 features larger bandgap $Al_{0.45}GaAs$ material compared to $In_{0.52}AlAs$ underneath the oxide and throughout the whole layer structure.

EELS analysis Pd/Ge/Ti/Pt on x266 device material

Since the NiGeAu results were similar on x266 and x238, a TEM investigation was carried out to observe on which material the PdGe layer makes the better ohmic contact. Since the NiGeAu alloys in the channel it will take advantage of the lower bandgap material. The increased specific contact resistance of the Pd/Ge/Ti/Pt sample is then probably due to the fact that the PdGe-based ohmic contacts do not alloy into the channel. In order to investigate the alloying behaviour of a PdGe-based ohmic contact a TEM and EELS analysis was carried out on x266 material.

Figure 6.21 shows a TEM micrograph of a cross section of a non annealed Pd/Ge/Ti/Pt contact to x266 device material. The picture is tilted 90 degrees to the right. Moving from left to the right the x266 substrate can be seen on the left, the first lighter grey area is the $In_{0.3}GaAs$ channel, followed by wider bandgap GaAs and AlGaAs. The Pd (60nm), Ge (100nm), Ti (30nm) and Pt (<20nm) layers are clearly defined, with some reaction between the Pd and Ge layer.

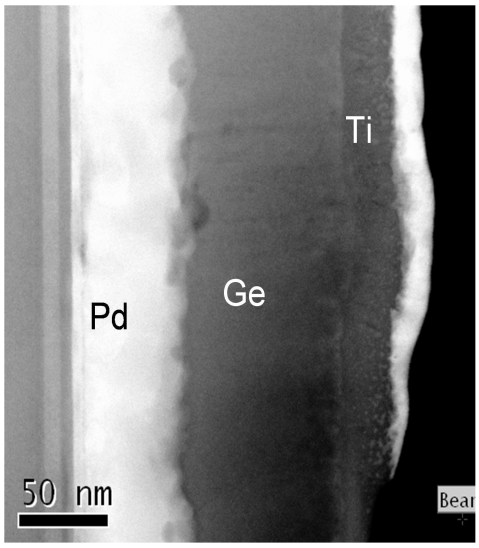


Figure 6.21: TEM micrograph of as deposited Pd/Ge/Ti/Pt contact on x266 device material

The samples used for EELS analysis are annealed at 380 C, 400 C and 420 C for 60s Figure 6.23. The specific contact resistivity increases with annealing temperature. According to literature [112] and previous TEM and EELS research on $In_{0.53}GaAs$, the

following behaviour is expected at annealing above 350^0C:

- Ge diffuses into Pd and reaches the semiconductor surface
- Ti layer acts as barrier layer maintaining the layer structure of Ti/Pt
- Non spiking interface, little alloying (<5nm)
- A layer deficient in Ga in the substrate

The TEM micrographs confirm the relatively smooth interface between contact and substrate and the annealing temperatures have not affected the $In_{0.3}GaAs$ channel layer. There also does not seem to be an extra In rich layer, which is deficient in Ga. The top Ti and Pt layers are still clearly defined separate layers and thus have not diffused into the Pd_2Ge region.

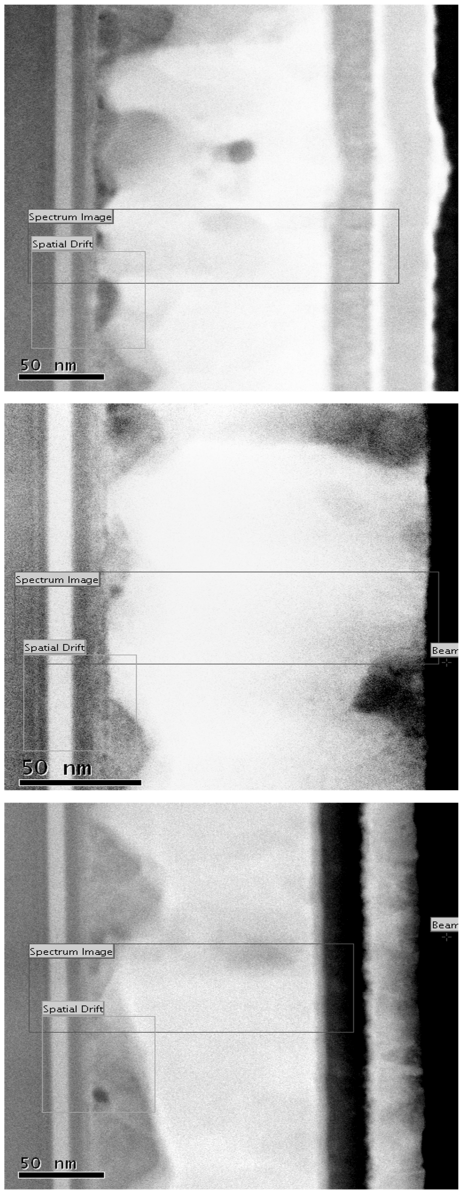


Figure 6.22: TEM micrograph of Pd/Ge/Ti/Pt contacts on x266 device material annealed at 380^{0}C, 400^{0}C and 420^{0}C

Figure 6.23: EELS analysis of Pd/Ge/Ti/Pt contacts on x266 device material annealed at 380^{0}C, 400^{0}C and 420^{0}C

The results of the EELS analysis are shown in Figure 6.23, as an edge intensity profile. There are six elements monitored: As, Ga, Ge, In, Pd, Ti. In every case there seems to be a Pd- rich layer at the semiconductor interface, which penetrates the GaAs and AlGaAs layers. The Ge layer, expected to reach the semiconductor surface, does not seem to diffuse into the GaAs/AlGaAs layer. In this case, the GaAs/AlGaAs layer would not receive additional n+ doping, which is critical to reduce the Schottky barrier width. The diffused Pd could potentially form a PdGa compound, which is a p-type layer causing an n-p barrier between the channel layer and ohmic contact. This could be the reason for the drop in

performance compared to the best annealing temperature for Pd/Ge/Ti/Pt ohmic contacts. The lack of an n+ interface layer could then be due to the elevated/non ideal annealing temperature, which is also mentioned in literature [112]. The ideal ohmic contact should still have a small residual layer of amorphous Ge near the Ti edge. Further optimisation of the contacts can then be achieved by altering Pd and Ge ratios and annealing temperatures.

The EELS analysis also measured the oxygen level but was found to be significantly low and there was no increased level between Ge and Ti layer. Suggesting the exposure of the sample during the processing step will have minimal contributions to the quality of the ohmic contact.

Pd/Ge/Ti/Pt vertical scaling study

IM-GaAs

The Pd/Ge/Ti/Pt is a rather large vertical structure of about 240nm. When the contacts are used on actual MOSFETs the contacts will have to become thinner (<100nm) as larger contacts pose lithography and processing problems. The thickness of the contact layers was then reduced, keeping the same ratio of Pd/Ge to have an excess of Ge. The structure was investigated without a cap, with a Ti/Au cap and a Ti/Pt cap, as work by [114] proved that scaled PdGe contacts are possible without a Pt or Au cap with specific contact resistivity as low as $8.5x10^{-7}$ $\Omega.cm^2$ on highly doped GaAs. The sample without a cap was difficult to measure as the probes damaged the thin PdGe layer. The PdGeTiAu structure showed poor contact resistance due to severe alloying of Au through the Ti barrier layer. The Ti/Pt cap proved the best results and also featured reduced Ti/Pt layer thickness. The material used is the highly doped GaAs wafer (IM-GaAs) supplied by IMEC. The temperature window has been expanded, given the results on x266. Pd and Ge layers thickness of are 10nm/25nm, 25nm/60nm, 50nm/120nm were studied and the results are shown in Figure 6.24.

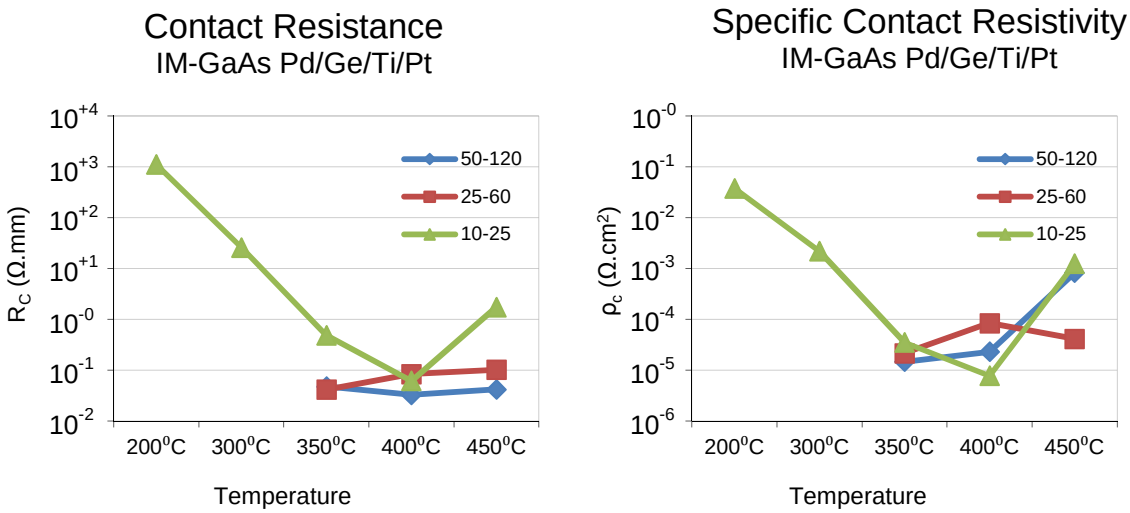


Figure 6.24: PdGe thickness scaling study on n-GaAs material annealed for 60s at 200^{0}C, 300^{0}C, 350^{0}C, 400^{0}C and 450^{0}C

The lowest specific contact resistivity was achieved with the thinnest layer structure at an annealing temperature of 400^{0}C. This clearly indicates that the PdGe structure is scalable. The specific contact resistivity is still rather large given the highly doped nature of the semiconductor material. This is potentially due to the Ga outdiffusion into the Pd_2Ge layer effectively p-type doping the layer and creating a p-n junction.

IM-InGaAs20

In order to compare the scaled Pd/Ge/Ti/Pt (10nm/25nm/30nm/30nm) contact with non-alloyed ohmic contacts, the scaled Pd/Ge/Ti/Pt contact was tested on 20nm 1x10^{19}cm^{-3} Si doped InGaAs (IM-InGaAs20). These results can then be used as a direct comparison with the Pd/Ge/Ti/Pt contact.

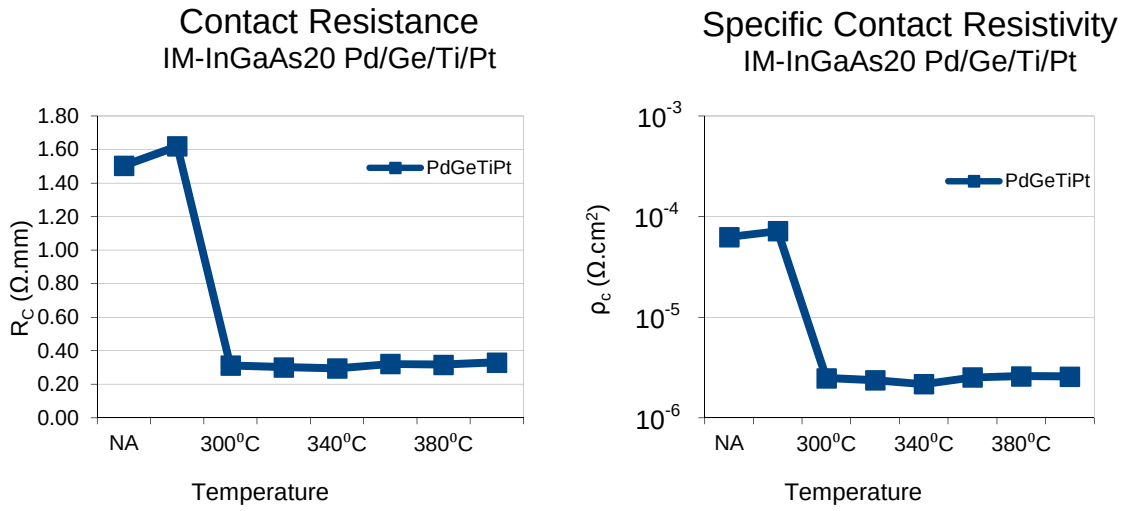


Figure 6.25: TLM results of scaled Pd/Ge/Ti/Pt ohmic contact structure on n-$In_{0.53}GaAs$ annealed at 0^0C, 200^0C, 300^0C, 320^0C, 340^0C, 360^0C, 380^0C and 400^0C

The results in Figure 6.25 show encouraging specific contact resistivity values. These are not as good as the non-alloyed contacts of chapter 6.3.2, suggesting a reduction of doping/increased barrier. This is similar to the Pd/Ge/Ti/Pt contact to highly doped GaAs and is possibly due to an outdiffusion of Ga, which potentially p-type dopes the Pd_2Ge layer as previously discussed in the EELS section.

NiGe on InGaAs20

Alternatively to the PdGe-based work a NiGe layer structure was tested based on the work by K. Tanahashi [147]. From literature this contact strategy gets the best results if annealed over 500^0C. Given the fact that in this work the temperature ranges are adjusted to the maximum temperature determined by the oxide, the annealing temperatures are kept in a window between 300^0C and 440^0C. The semiconductor material used in this test is IM-InGaAs20, which features a narrow bandgap, highly doped surface material.

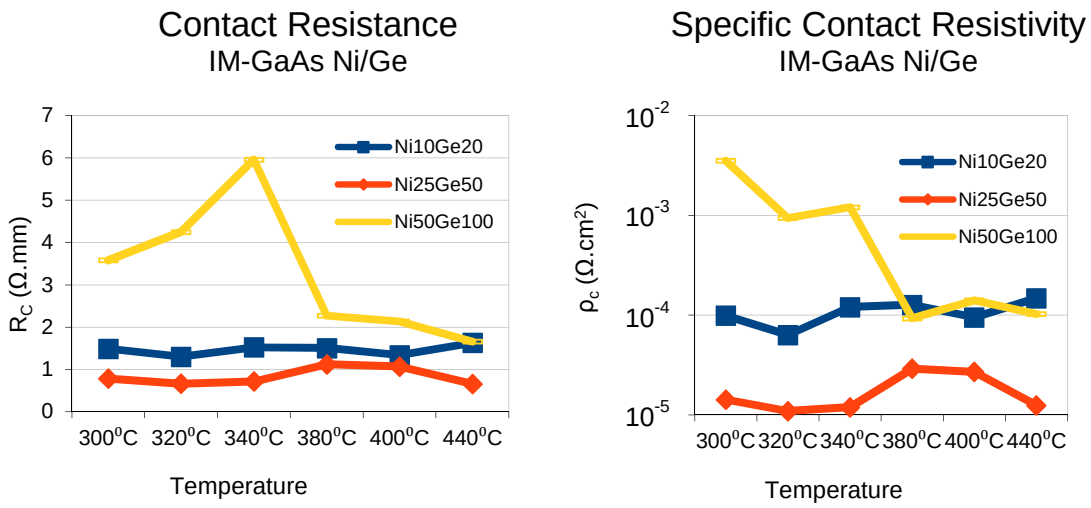


Figure 6.26: NiGe thickness scaling study on n-GaAs material annealed for 60s at 300°C, 320°C, 340°C, 380°C, 400°C and 440°C

As shown in Figure 6.26, The samples have poor ohmic contact performance, certainly given the highly doped and low barrier nature of the material. A drop off in specific contact resistivity after 450°C was detected at IMEC but for the purpose of developing an ohmic contact suitable for GaGdO based MOSFET devices, the NiGe contact layers are not considered viable.

Conclusion

The electrical performance of the ohmic contact is predominately determined by the bandgap and the doping of the semiconductor material underneath the contact metal. The chemical analysis revealed little alloying (5 to 10nm) into the semiconductor material, which results in specific contact resistivity ranges varying between $5x10^{-5}\Omega cm^2$ for x266 material to $3x10^{-6}\Omega cm^2$ for IM-InGaAs20. Therefore, the PdGe-based contact could potentially be used as a self-aligned ohmic contact but suffers from an increased contact resistance compared to the NiGeAu contact as the semiconductor material in the channel material has a lower bandgap than the semiconductor material underneath the oxide, which is due to the buried channel layer structure. Removing the wider bandgap material prior to metal deposition could potentially improve the specific contact resistivity, which is described in the following section.

6.3.1.2 Dry Etch

The chemical process of a wet oxide etch is isotropic for amorphous materials, which leads to lateral etching of the oxide underneath the mask. For small scaled devices the etch profile has to be vertical to limit access region pinning and depletion as discussed in chapter 6.2. Dry etching can form anisotropic features by making use of physical processes. Physical dry etch processes also feature detrimental aspects such as re-deposition, mask erosion, surface contamination and material damage. Previous work by R. Hill and X. Li established a process for dry etching GaGdO on device material with a Ni/Ge/Au based ohmic contact [225].

Combining dry etch with the small lateral alloying from the Pd/Ge contact, opens the route to devices with sub-100nm gate length. This is of a particular interest for self-aligned devices, which feature small sidewall spacers and require little lateral diffusion of the source/drain ohmic contacts. It also offers possibilities to remove the wider bandgap material between the dielectric and the channel prior to metal deposition.

Plasma etching of 6-1073 device material

As a benchmark, devices were built on device material provided by Freescale Semiconductors. The contacts used, are the standard Au/Ge/Ni metal stack annealed at 420^0C for 60s. The dry etch was performed in an Oxford Instruments Ltd. Plasmalab System 100 RIE at room temperature. The etching end point was monitored by using an interferometer with a laser wavelength of 670nm. The etch process featured following conditions: SiCl4 flow rate 20sccm, RF power 60W and chamber pressure 4mTorr with a self bias of 260V. The etch rate is then roughly 4nm/minute with an rms surface roughness around 0.3 to 0.7nm [225].

Metallisation	R_C (Ω.mm)	R_{sh} (Ω.sq)	ρ_c (Ω.cm^2)
Au/Ge/Ni	0.72	385	1.39×10^{-5}
Au/Ge/Ni	0.93	368.75	2.44×10^{-5}

Table 6.10: TLM results on 6-1073-6 Freescale Semiconductor material using dry etch and a AuGeNi ohmic contact annealed at 360^0C for 60s.

As shown in table 6.1, the contacts have relatively high specific contact resistivity values, but are ohmic and can be used as a benchmark.

Device material x319 was then used to test the dry etch process with PdGe based ohmic contacts. The same dry etch strategy with ionised $SiCl_4$ gas was used for the PdGe-based

ohmic contacts. Since the purpose of the research was to make the contacts scaled, a Pd/Ge layer thickness of 25nm/60nm was chosen to reduce the vertical height of the ohmic contact. This contact strategy didn't have the lowest specific contact resistivity when tested on highly doped GaAs but it was ohmic nonetheless. A temperature test between 300°C and 420°C was carried out using dry etched Pd/Ge contacts on x319 and the results are shown in Table 6.11.

	Metallisation	R_C (Ω.mm)
300^0C	Pd/Ge 25/60nm	8317.5
340^0C	Pd/Ge 25/60nm	6097.88
380^0C	Pd/Ge 25/60nm	Not measurable
420^0C	Pd/Ge 25/60nm	Not measurable
420^0C 300s	Pd/Ge 25/60nm	3906.38

Table 6.11: Dry etch test using a Pd/Ge ohmic contact on GaO/GaGdO gate dielectric MOSFET device material

The measurements showed non-ohmic behaviour to the point where some data could not be extracted. This means that either there is a residual layer or that the dry etch process induces damage into the material. The residual layer is potentially an effect of the dry etch as higher concentrations of C, O, Cl, GaO, GaH, GaCl, Al and Si were found on the surface just after RIE etching in previous work by X. Li et al. [226]. In order to clarify whether the Pd/Ge ohmic contact stack was causing the non-ohmic behaviour, the same experiment was repeated on x319 device material using the original Pd/Ge/Ti/Pt stack (50/120/30/30nm) since this had been tried and tested with device material (x266). Similar non-ohmic behaviour was observed excluding the contact stack as a potential fault.

Ion Gun etch on IM-InGaAs20

There are two potentially damage inducing processes, which could lead to non ohmic behaviour. One is the actual dry etch process, which leaves a thin layer of etch residue behind, which needs to be cleared prior to the metal deposition. This is done by making use of an in-situ ion gun in the Plassys 1 metallisation tool. To determine whether the damage is induced by the ion gun process, Pd/Ge/Ti/Pt contacts were made on 20nm $1x10^{19}cm^{-3}$ $In_{0.53}GaAs$ (IM-InGaAs20). The ohmic contact stack and semiconductor material are the same as the Pd/Ge/Ti/Pt test on IM-InGaAs20 material using a wet etch clean, which then allows for a direct comparison between dry etch and wet etch.

Two samples were made; one had a surface clean using the ion gun (Figure 6.27), the other one had a wet etch clean and no exposure to the ion gun (Figure 6.28).

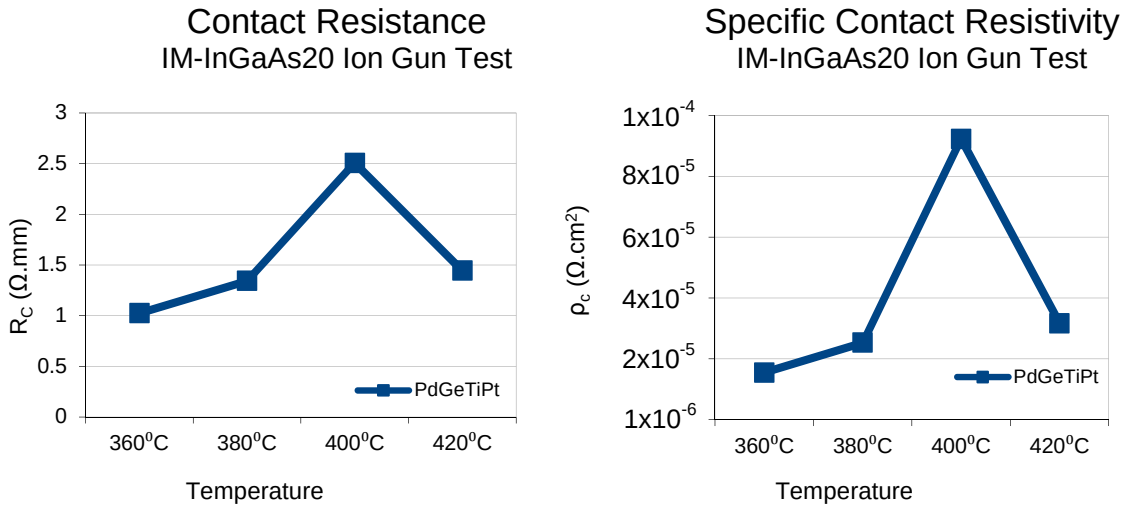


Figure 6.27: TLM result of Pd/Ge/Ti/Pt ohmic contact structure using ion gun sample cleaning on n-$In_{0.53}GaAs$ annealed for 60s at 360°C, 380°C, 400°C and 420°C

S11056 normal wet etch sample clean:

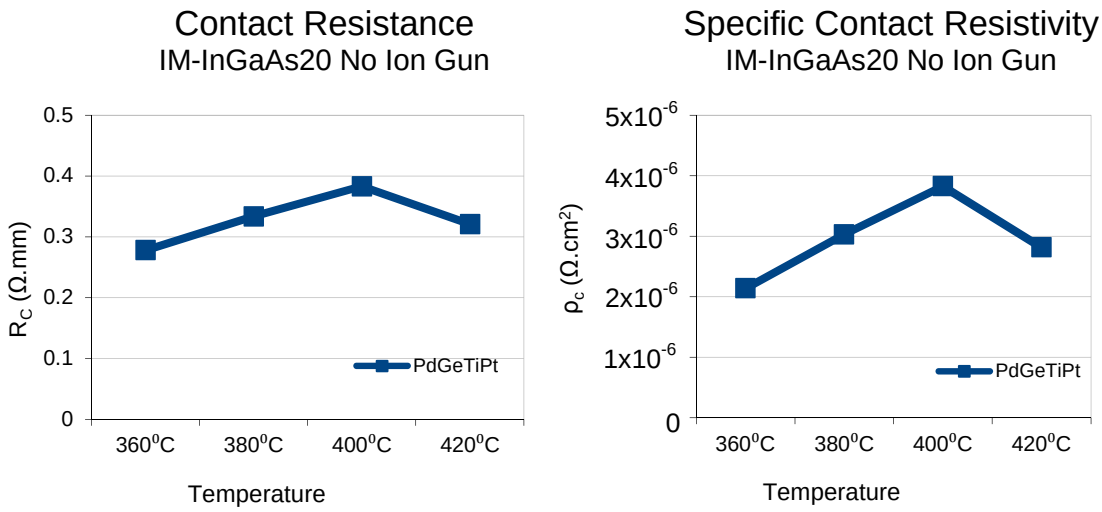


Figure 6.28: TLM result of Pd/Ge/Ti/Pt ohmic contact structure using wet etch sample cleaning on n-$In_{0.53}GaAs$ annealed for 60s at 360°C, 380°C, 400°C and 420°C

Comparing Figures 6.27 and 6.28, the values for the contact resistance and specific contact resistivity are clearly higher when using the ion gun. This shows the ion gun is doing significant damage to the surface of the semiconductor. However, the contacts still show ohmic behaviour, which means the actual RIE dry etch must have some damaging effects.

Comparison of wet etch, dry etch and ion gun etch on x266 device material

To investigate the effects of dry etch of GaGdO stopping on AlGaAs, x266 device material was used. Three samples were prepared: a full dry etch process, a wet oxide etch, a wet oxide etch and ion gun treatment. The full dry etch featured non-ohmic contact behaviour and is therefore not shown. The wet oxide etch and wet oxide etch with ion gun treatment are shown in Figures 6.29 and 6.30 respectively.

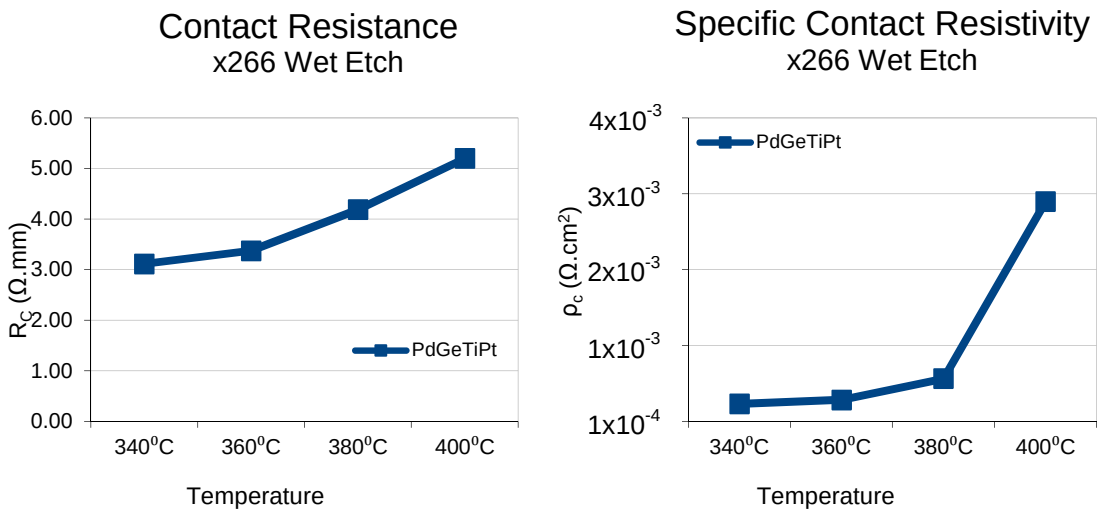


Figure 6.29: TLM results of Pd/Ge/Ti/Pt ohmic contact structure on x266 device material used as a benchmark for Ion gun and dry etch damage tests

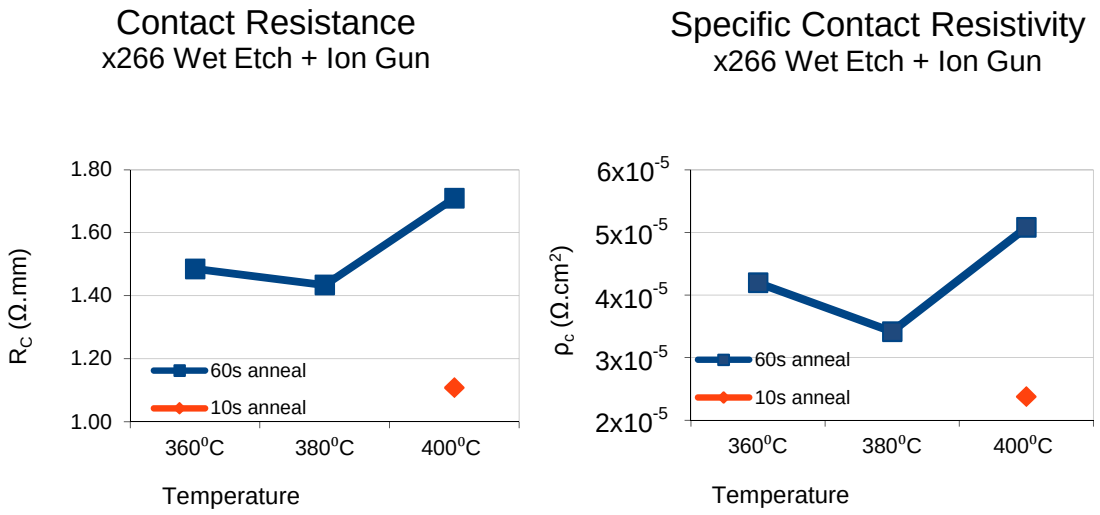


Figure 6.30: TLM results of a Pd/Ge/Ti/Pt ohmic contact structure on x266 device material using a wet etch and ion gun surface clean.

The results for the wet etch (Figure 6.29) are comparable to the results previously found on x266 material (Figure 6.19). Remarkably there is an improvement of about one order of magnitude in specific contact resistivity when the ion gun is used. This potentially does some further cleaning of the sample or removes some wide bandgap material. The Pd/Ge contact would benefit from having low bandgap material as the specific contact resistivity on highly doped $In_{0.53}GaAs$ (Figure 6.28) is over one order better compared to wide bandgap device material. However, the dry etch strategy works for a Au/Ge/Ni ohmic contact. This is possibly due to the large alloying into the channel material and effectively by-passing the residual layer or the damage induced by the dry etch. Forming contacts on self-aligned devices on GaGdO device material will then be challenging and future work should focus on reducing the damage from a dry etch.

Conclusion

Two different anisotropic etches were used: a RIE etch technique and an ion gun etch technique. The RIE etch resulted in non-ohmic contact behaviour but the ion gun etch improved the specific contact resistivity about one order. The ion gun etch was performed after a wet etch of gate dielectric and therefore more research is needed in order to perform a dry etch only gate dielectric removal. Dry etch techniques featuring optimized low damage etch processes could reduce the specific contact resistivity of buried channel devices even further, however the tendency is to move away from the buried channel device architecture towards a surface channel device architecture, which has the lower bandgap channel directly under the dielectric layer. The PdGe-based ohmic contact can therefore be implemented in the current GaGdO MOSFET device structures but only when a wet etch of the gate dielectric is used.

6.3.2 Non Alloyed Contacts

The non alloyed ohmic contacts feature no additional doping or reduction of bandgap barrier lowering and are therefore not suited for wide bandgap material. However, the non alloyed contacts form ohmic contacts on doped, low bandgap material (IM-InGaAs20).

Five main non alloyed contact structures have been tried on this material: Au, Ti/Pt, TiW, Al and Ni. The choice of metals used, was dominated by the availability of metals in the metal deposition tools at the JWNC cleanroom. The non alloyed contacts featuring Au were mainly used to build and test scaled ohmic contact structures chapter 7. The material has not been used for full optimisation of the ohmic contacts, it is mainly used as a proof of concept. The Au ohmic contact structure was used as a benchmark while the Ti/Pt, Ni and

Al were used as Si processing compatible ohmic contact structures using e-beam metal deposition featuring different work functions. The TiW contact structure was used to test a Si compatible sputtered ohmic contact.

6.3.2.1 E-Beam evaporated metals

Table 6.12 shows the results for the Si compatible ohmic contact structures of Ti/Pt, Al and Ni. The Ti layer helps the removal of remaining native oxides and helps the Pt to bond to the semiconductor material. The Ni contact has been measured twice both unannealed and annealed at 250^0C for 60s. This is based on previous work using "nickelide" ohmic contact structures [216, 217]. A HCl:H_2O 1:100 30s clean was used for the samples to remove the native oxides and the metals where then e-beam evaporated. Patterns were formed using lift off. Only the best results are discussed in this chapter as a more detailed study is performed in the scaled ohmic contact chapter 7.

Metallisation	R_C (Ω.mm)	R_{sh} (Ω.sq)	ρ_c (Ω.cm^2)
Ti/Pt 10/80nm	0.17	401.37	$7.76x10^{-7}$
Al 100nm	0.65	242.08	$1.76x10^{-5}$
Ni 100nm	0.42	222.83	$8.02x10^{-6}$
Ni 100nm (annealed)	0.68	189.31	$2.56x10^{-5}$

Table 6.12: Overview of Si-compatible non alloyed ohmic contacts to highly doped $In_{0.53}GaAs$ material

The result shows a promising specific contact resistivity for the Ti/Pt contact structure, making this a potential candidate for further optimisation. The Al and Ni ohmic contact structures show increased values for the specific contact resistivity compared to the Ti/Pt contact structure. Alloying the Ni ohmic contact structure didn't improve the performance and even seemed to affect the sheet resistance. A potential cause is that a Ni-As forms a low resistivity alloy, which laterally alloys hence reducing the sheet resistance.

The Au contacts were predominantly used to verify scaled structures and allow for proof of concepts. The same HCl:H_2O 1:100 30s surface cleaning was used.

Metallisation	R_C (Ω.mm)	R_{sh} (Ω.sq)	ρ_c (Ω.cm^2)
Au 100nm	0.15	307.2	$7.19x10^{-7}$

Table 6.13: Overview of Au contacts to highly doped $In_{0.53}GaAs$ material

The contacts show reduced specific contact resistivity for ordinary TLM's in all cases. However, there is a difference between non-isolated and isolated (mesa) TLM structures. If there would be no lateral current flowing along the contact edges the sheet resistance for a normal TLM should be the same as the isolated TLM structures. The sheet resistance increases when measuring isolated contacts. This is an indication that contacts measured with normal TLMs have a certain error, which has to be compensated, which is explained further in chapter 7.

The Au contact structure was also used to test c760 material with a 2.5nm InAs top layer. The lower bandgap should pin in the conduction band resulting in decreased specific contact resistivity values. A Au contact of 100nm thickness was e-beam evaporated after a surface clean experiment of varying HCl:H_2O 1:100 etch times, as shown in Figure 6.31.

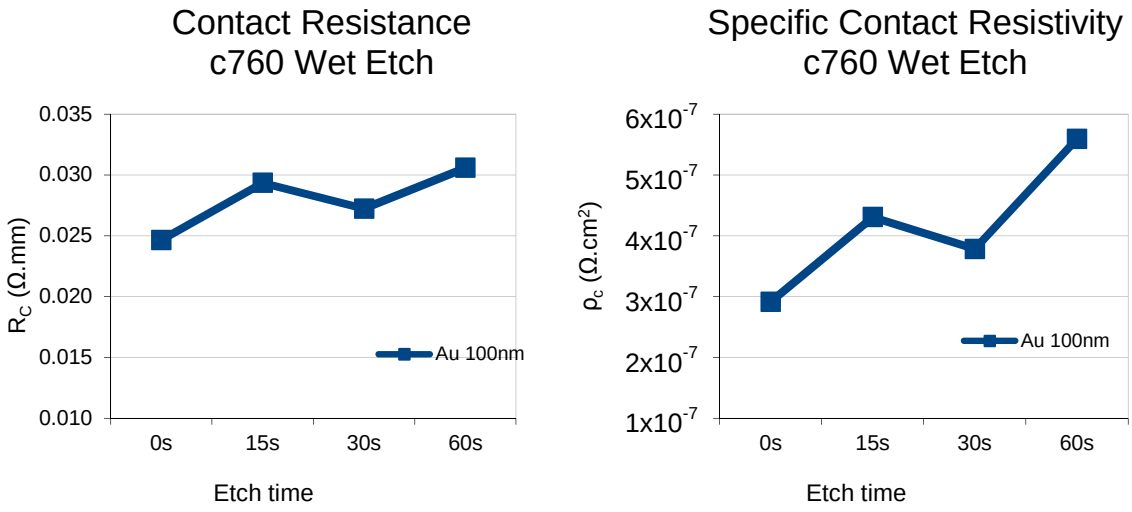


Figure 6.31: Surface cleaning study on n-InAs material using HCl:H_2O wet etch and 100nm Au ohmic contact structure.

A specific contact resistivity of $3x10^{-7}\Omega cm^2$ is observed on a sample, which didn't receive any native oxide etch. The specific contact resistance depends on the oxide etch time, which indicates that the oxide etch might actually remove or at least damage the thin 2.5nm InAs layer. Growing a thicker layer of InAs might solve this problem and the reduced specific contact resistivity values suggest that this material is promising to reach the ITRS [1] requirements.

6.3.2.2 Sputtered metals

The contact using a TiW metal structure was chosen based on the work by U. Singisetti et al. [113], which showed very low specific contact resistivities. The work features mainly two different metals: Mo and TiW. These metals have a work function close to the electron affinity of $In_{0.53}GaAs$ (4.5 eV), which should reduce the Schottky barrier when the Fermi level of the semiconductor is unpinned. Since at the time of the experiment Mo was not available in the metal deposition tools, TiW was chosen to investigate the quality of sputter deposition based ohmic contacts. Sputtering has the disadvantage of depositing a uniform layer across the sample. This prevents the use of a lift off technique and subtractive patterning techniques have to be used. First, the $In_{0.53}GaAs$ goes through a substrate cleaning cycle including a native oxide etch using $HCl:H_2O$ 1:100, secondly a 100nm TiW layer is deposited, thirdly a PMMA mask is spun, e-beam exposed and developed and finally the TiW layer is etched in a dry etch tool. The TLM structures on the sample were measured without annealing the sample first, and were measured again after a 400^0C for 60s anneal. The first run showed poor edge definition on the TLMs Figure 6.32, the cause of this problem was the PMMA being damaged by the dry etch. The solution was to do a post bake of 1h 180^0C after the sample has been developed.

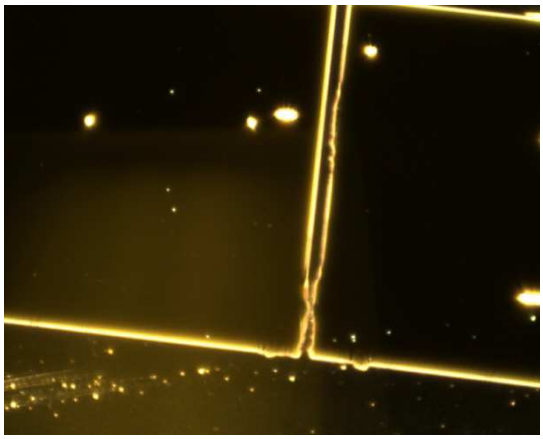


Figure 6.32: Dark field image of poor edge definition after dry etching TiW using a PMMA mask

The anneal of 400^0C 60s was based on previous work done at the University of Glasgow by X. Cao.[136] The work investigates the sputter-induced damage caused by direct current magnetron sputter coating of W on GaAs based HEMT's. Post sputter annealing was found to significantly reduce the damage, therefore the sample also received a 400^0C 60s anneal. There should be no alloying as the melting points of refractory metals or compounds such as TiW are generally above 800^0C. The results are shown in Table 6.14.

	Metallisation	R_C (Ω.mm)	R_{sh} (Ω.sq)	ρ_c (Ω.cm^2)
Non Annealed	TiW 100nm	2.95	1020.34	8.53x10^{-5}
400^{0}C 60s	TiW 100nm	1.08	2215.67	5.42x10^{-6}

Table 6.14: TLM results of samples s11082 with non-annealed and annealed TiW ohmic contacts on highly doped $In_{0.53}GaAs$

According to the contact resistance and specific contact resistivity values, the damage gets annealed out to a certain degree. However, lower specific contact resistivity values are shown using Au and Ti/Pt ohmic contact structures on the same material. The sheet resistance measured is significantly higher indicating damage in the semiconductor material after dry etch. Also annealing the sample seems to damage the substrate substantially. Due to the lack of a damage free metal etch, the sputtering technique was not further researched or optimised. However, further optimisation of a damage free metal etch could potentially allow a sputtered metal to be investigated in the future.

6.3.2.3 Conclusion

Future different MOSFET device structures featuring highly doped, narrow band source/drain regions will allow for non alloyed contact deposition as additional doping or band gap lowering is no longer required. Four different ohmic contact structures were deposited using e-beam evaporated metals with different work functions and one ohmic contact structure was deposited using sputtering. The e-beam evaporated metal structures were; Ti/Pt 10nm/80nm, Al 100nm, Ni, 100nm and Au 100nm and the sputtered metal structure was TiW 100nm. The best ohmic contacts were formed using the Au and Ti/Pt ohmic contact, which had a specific contact resistance in the region of 7.5x10^{-7}Ωcm^2. The Ni contact, which theoretically has a work function similar to Au had a specific contact resistivity, which was one order higher than the Au contact and deteriorated in contradiction to the results found in literature. The poor results of the annealed Ni sample are probably due to migration of Ni, which led to a decreased semiconductor sheet resistance. The Al contact with the lowest theoretical work function featured the highest specific contact resistivity. Therefore, the influence of the work function of the metal is not conclusive and is therefore probably not the crucial factor, which determines the quality of the ohmic contact on highly doped $In_{0.53}GaAs$.

The results of the sputtered contacts were subject to the quality of the metal etch and before any conclusive results can be drawn the metal etch should be optimised. However, the contacts showed promising specific contact resistivity values and the sputtered contacts should be considered in future work.

6.3.3 Device Results

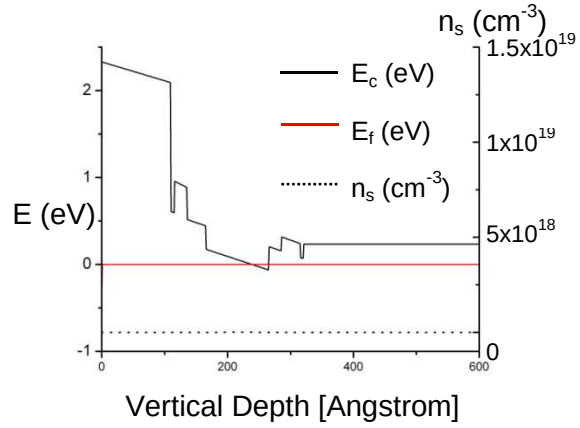
6.3.3.1 Scaling of Flatband Mode III-V MOSFETs with a GaO/GaGdO gate dielectric stack and an $In_{0.3}GaAs$ channel

Introduction

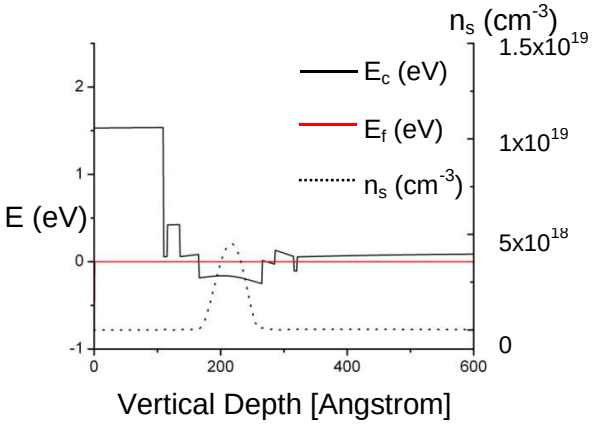
The purpose of this study is to determine whether the flatband III-V MOSFET device structure can be scaled along both the gate length and source/drain separation. This is an important step towards a device that has the dimensions required by the ITRS [1] for sub 22nm technology generations. Scaling down the access regions could result in significant short channel effects. It is believed that the short channel effects arise from the 2-dimensional nature of the channel charge control associated with the proximity of the source and drain alloyed contact regions to the gate of the device. Devices with gate lengths of 90nm, 180nm, 270nm and 1 µm each with a range of source/gate and drain/gate separation have been designed, fabricated and tested. The dimensions of the source/gate and drain/gate separations are explained in Table 6.16. Originally both Si-compatible and Au/Ge/Ni source/drain ohmic contacts were planned to be tested on 6-1073 material using the Au/Ge/Ni contacts as a benchmark. However, the Pd/Ge/Ti/Pt contacts are not compatible with the dry etch process (chapter 4.4.3 and section 6.3.1.2) and therefore have not been tested as the reduced feature size impedes the use of a wet etch for gate dielectric removal.

The motivation for utilizing a GaO/GaGdO gate dielectric stack and an $In_{0.3}GaAs$ channel is that the GaGdO dielectric stack [105] has a proven low interface state density when deposited on a GaAs surface layer. This constrains the channel composition to $In_{0.3}Ga_{0.7}As$ for the flatband mode architecture, and therefore lower drive current. Higher In concentration causes lattice mismatches to occur between the channel and the GaAs/AlGaAs buffer layer. This introduces defects in the channel reducing the performance of the device. However, this choice of gate dielectric enables a decoupling of device short channel effects (SCE) from gate oxide trap issues, which both adversely affect key performance metrics such as subthreshold swing (SS).

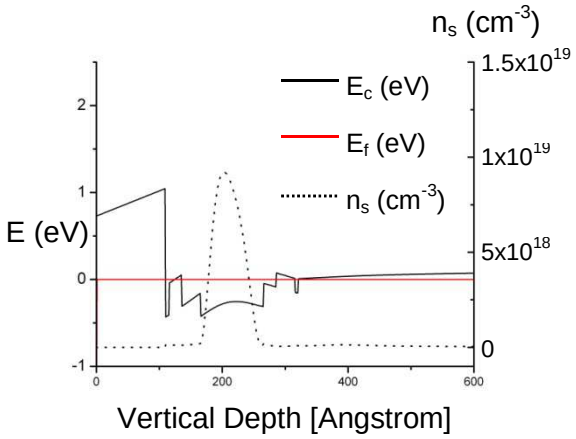
The materials used for all device fabrication have the layer structure using a $Al_{0.45}GaAs$ wide bandgap layer and $In_{0.3}GaAs$ channel. The 10nm GaGdO stack with dielectric constant of ~20, together with the underlying semiconductor layers, which spatially separate the device channel from the gate dielectric, result in an equivalent oxide thickness of 3.4nm. The full layer structure can be seen in the appendix under the materials section.



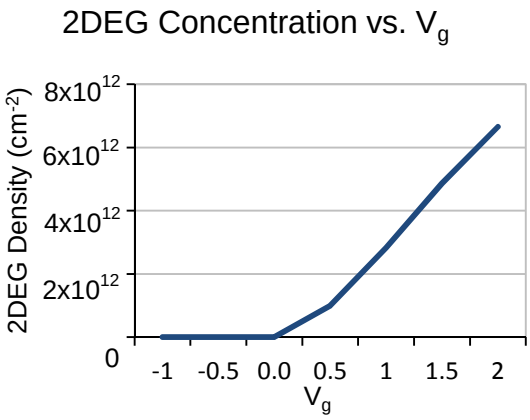
a) E_c, E_f and ns profiles for V_g = 0.4V



b) E_c, E_f and ns profiles for V_g = 1.2V



c) E_c, E_f and ns profiles for V_g = 2V



d) Channel carrier concentration against V_g

Figure 6.33: Poisson - Schrodinger simulation of a 5nm GaGdO gate dielectric device material

Based on Poisson-Schrodinger simulations, a positive V_t is expected for this layer structure as is shown in Figure 6.33d. This means that the channel features little charge population at 0V and the device is then pinched off, resulting in an enhancement mode MOSFET device. Increasing the V_g above the V_t level Figure 6.33a results in the conduction band at the bottom of the channel bending below the Fermi level aided by the lower δ-doping layer. The carrier concentration distribution is then mainly situated near the bottom of the channel away from the oxide/semiconductor interface. The carrier concentration distribution shifts towards the oxide/semiconductor interface as V_g increases towards the

saturation voltage V_g = 2V Figure 6.33c with a flatband voltage predicted to occur at V_g = 1.2V Figure 6.33b. The bulk of the carrier concentration, as observed in Figure 6.33 a,b,c, is in the channel at V_g below 2V, which reduces the influence of surface states at the semiconductor/oxide interface. This is an advantage of the buried channel architecture compared to an inversion mode device and as a result larger mobility values in the channel can be achieved.

The process flow comprises the formation of ohmic contacts of varying separations, between, which Pt/Au gates are subsequently aligned. A RIE dry etch process using ionised $SiCl_4$ gas, as previously discussed in section 6.3.1.2, was used for gate dielectric etch in the source/drain regions prior to electron beam evaporation of NiGeAu-based contact metallization, which was annealed at 360°C [106]. A "wrap-around" device design, shown in the micrograph of Figure 6.34 is utilized to obviate the need for an isolation level. Figure 6.34 also shows the relaxed 1 µm gate length/ 1µm gate/source and gate/drain devices. In all cases the gate is lithographically aligned centrally between the source and drain contacts, with equal source/gate and gate/drain spacings. Low contrast of PMMA does not allow for a separation between source and drain smaller than 500nm and therefore the source and drain have been written and processed independently over 2 different lithography steps. Table 6.15 summarises the gate length (L_G) and source/gate (L_{SG}) separations of the III-V MOSFETs investigated in this work.

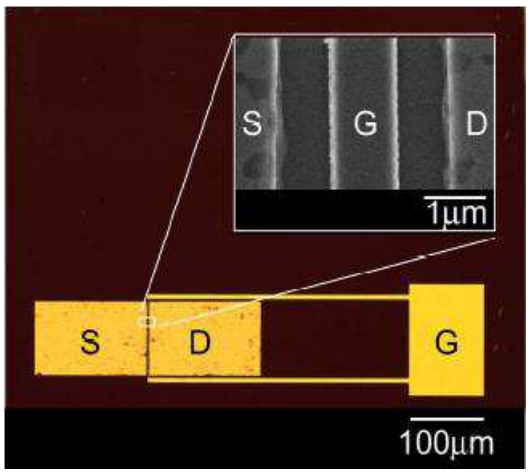


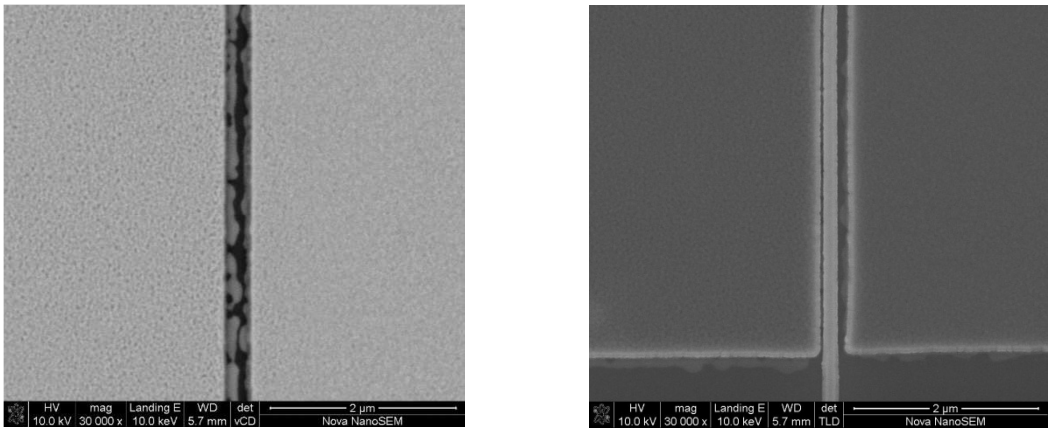
Figure 6.34: wrap around device design and relaxed device geometry

L_g	L_{sg}		
90nm	90nm	190nm	1µm
180nm	180nm	280nm	1µm
1µm	1µm	1µm	1µm

Table 6.15: Summary of L_g and L_{sg} sizes used for scaled flatband mode III-V MOSFETs with GaO/GaGdO gate dielectric stack

Device results

The main device characteristics will be discussed using the devices with 1μm access regions in order to eliminate potential short channel effects. This data can also be directly compared against the work performed by R. Hill et al. [4] using an identical layer structure and to the devices using a Al_2O_3 gate dielectric, as shown in section 6.3.3.2. The devices with a scaled access region below 1μm will be discussed separately. The motivation for choosing the source/gate and gate/drain spacings of the gate length+100nm were in an attempt to mitigate against the lateral alloying of the ohmic contact metal, which can be seen in Figure 6.35. This contact metal alloying compromises the performance of the most aggressively scaled devices due to poor alignment (+/- 30nm) and large lateral alloying of the NiGeAu contacts.



(a) **(b)**

Figure 6.35: Effects of laterally alloyed NiGeAu on source/drain 270nm gap (a), including a 90nm overlapping gate (b)

The benchmark data used is previous Glasgow work [4], which features low subthreshold swing, high transconductance, low R_{on} and a high peak mobility of 5230cm^2/V.s. The main difference between this work and the work in [4] is the oxide etch. This work uses a dry etch to remove the oxide to obtain little lateral removal of the oxide in the access regions allowing for more aggressively scaled devices. However, a dry etch technique can potentially increase contact resistance, due to contamination of the surface prior to contact deposition [226], resulting in larger R_{on} and lower g_m values compared to wet etched devices.

90nm, 180nm and 1µm gate length III-V MOSFETs with source/gate and source/drain separations equal to 1µm.

Figure 6.36 shows the $I_{ds}(V_{ds},V_{gs})$ characteristics of typical 1µm, 180nm and 90nm gate length devices, each with 1µm source/gate separations.

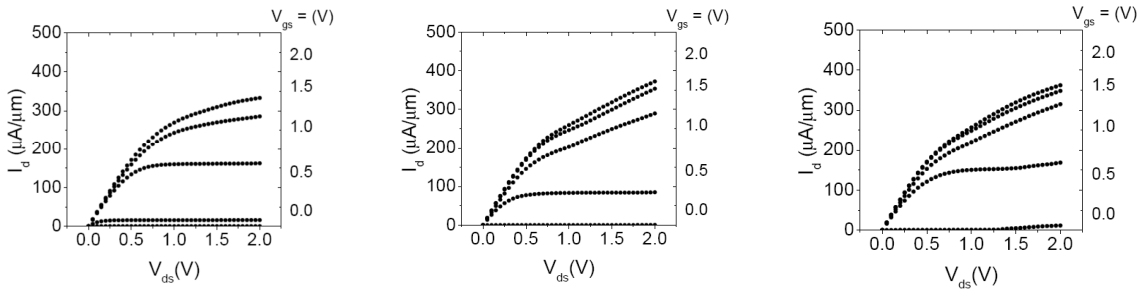


Figure 6.36: $I_{ds}(V_{ds},V_{gs})$ characteristics of typical III-V MOSFETs with 1µm source/gate separations for gate lengths of (a) 1µm; (b) 180nm; (c) 90nm

Figure 6.37 shows the log I_{ds},$(V_g - V_t)$ curves for these devices with 1.2V drain bias. The threshold voltage was determined to be the gate bias required to reduce the drain current (measured at V_{ds} = 1.2V) to 1µA/µm.

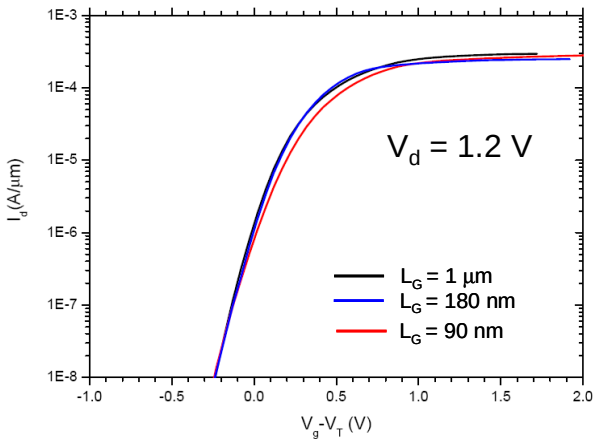


Figure 6.37: logI_d/$(V_g$-$V_t)$ curves for 1µm, 180nm and 90nm gate length devices with 1µm source/gate separations

Table 6.16 summarizes the on-state and off-state performance of the dry etch scaled devices compared to the work of [4].

	90nm	180nm	1µm	1µm [4]
V_t (V)	-0.29	-0.01	+0.31	+0.26
$I_{d,sat}$ (mA/mm)	288	260	286	407
SS (mV/dec)	78	76	68	102
g_m (mS/mm)	346	384.6	357	477
R_{on} (Ω.µm)	2503	2387	2703	1920
I_{on}/I_{off}	$2.54x10^1$	$3.0x10^4$	$1.2x10^6$	$6.3x10^4$

Table 6.16: Summary of device metrics for flatband mode III-V MOSFETs with GaO/GaGdO gate dielectric stack with L_{sg} = 1µm

The detailed performance of the dry etched device with 1µm access regions is discussed below.

V_t: The V_t is comparable between dry etch and wet etched contacts for a device with a 1µm L_g. This indicates that the oxide quality and underlying semiconductor material is not affected by the source/drain oxide etch. Scaling the L_g from 1µm to 90nm results in a voltage drop by 0.6V for V_t. The voltage drop is possibly due to a loss in electrostatic control. The loss in electrostatic control could be due to a loss of metal work function or from the buried channel layer structure. The barrier layer between the channel and the oxide helps to decouple the channel from gate oxide traps, but has the drawback that the channel is further away from the gate metal increasing potential electrostatic control issues. The layer structure should ideally be optimised with the smallest barrier layer between the channel and oxide as possible and care has to be taken to avoid residue forming on the oxide, which can decrease the impact of the metal work function.

$I_{d,sat}$: The $I_{d,sat}$ is comparable between the different gate lengths, suggesting the limiting factor for $I_{d,sat}$ is the maximum carrier concentration in the access regions. The larger $I_{d,sat}$ values in [4] can be explained by the lower total on resistance and the lower contact resistance value of 0.41Ω.mm [4] compared to 0.79Ω.mm.

Subthreshold performance: The flatband mode III-V MOSFET architecture using a dry etch technique delivers excellent off-state performance for gate lengths down to 90nm, with no appreciable degradation of subthreshold swing (SS), measured at both low and high drain bias with reducing gate length. These are some of the lowest subthreshold swing data ever obtained for III-V MOSFET devices. The channel is capable of switching off suggesting the gate oxide traps have little influence on the channel. Even with lower $I_{d,sat}$ and higher R_{on} values the I_{on}/I_{off} ratio of these devices is superior to [4] for a 1µm gate length device with 3µm source/drain pitch. The I_{on}/I_{off} ratio was determined with following parameters; I_{off}, V_{gs} = 0V and V_d = 2V; I_{on}, V_{gs} = 1.2V and V_d = 2V.

I_g: Low gate leakage current in the order of 30pA was recorded, which suggests a high quality oxide with a high-k value for the GaO/GaGdO dielectric stack. The low gate leakage is confirmed by the low subthreshold swing values with good uniformity across the sample.

R_{SD}: Increased R_{on} and R_C values compared to wet etch devices confirm the detrimental effects of a dry etch technique compared to a wet etch technique. The contact resistance measured by TLM measurements is relatively high at 0.79Ω.mm with a corresponding specific contact resistivity of $1.81 \times 10^{-5} \Omega.cm^{-2}$. This value is rather high compared to the specific contact resistivity calculated from [4], which is $3.74 \times 10^{-6} \Omega.cm^{-2}$. However, aggressively scaled devices using wet etch would not be feasible due to the lateral etching and therefore dry etch has been used.

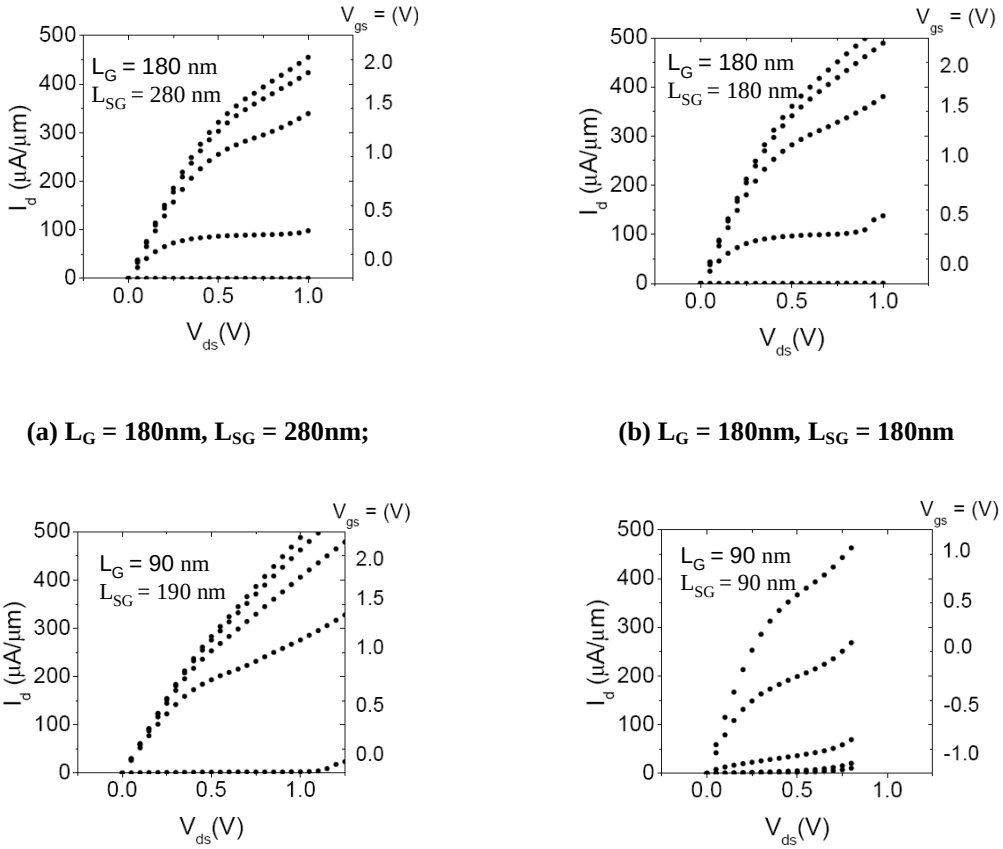
The devices show comparable performance to [4] with excellent off-state performance but with slightly increased contact resistance. In order to analyse the potential short channel effects the devices with scaled access regions will be discussed.

90nm and 180nm gate length III-V MOSFETs with source/gate and source/drain separations equal to the gate length and the gate length + 100nm.

The advantage of the scaled access regions is an increase of g_m and $I_{d,sat}$ as the overall contribution of the access region resistance becomes smaller but this could result in short channel effects. An inversion mode MOSFET device is considered to be short, when the channel length is the same order of a magnitude as the width of the source/drain depletion-layer. Flatband MOSFET devices do not have the conventional depletion-layers as there is no p-n junction and should then be less susceptible to short-channel effects. The short-channel effects can still occur from the depletion region caused by the ohmic

contact/semiconductor interface, which will become more prevalent when access regions are being scaled. The short-channel effects manifest themselves as a limitation on electron drift characteristics in the channel and a shift of V_t [204]. The main different short-channel effects are: DIBL and punchthrough, surface scattering, velocity saturation, impact ionization and hot electrons.

Figure 6.38 shows the $I_{ds}(V_{ds},V_{gs})$ characteristics of typical 180nm and 90nm gate length devices with source/gate (L_{SG}) separation equal to the gate length (L_G) and equal to the gate length + 100nm.



(a) L_G = 180nm, L_{SG} = 280nm; **(b) L_G = 180nm, L_{SG} = 180nm**

(c) L_G = 90nm, L_{SG} = 190nm **(d) L_G = 90nm, L_{SG} = 90nm**

Figure 6.38: $I_{ds}(V_{ds},V_{gs})$ characteristics for various III-V MOSFETs

Figure 6.39 shows the $\log I_{ds},(V_g-V_t)$ curves for these devices with 0.7V drain bias. The threshold voltage, V_t, was determined as above, for a drain voltage, V_{ds} = 0.7V.

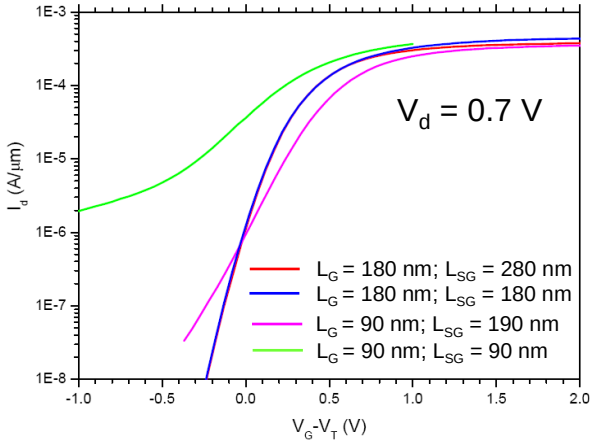


Figure 6.39: logI_d/(V_g-V_t) curves for 180nm and 90nm gate length devices with source/gate spacings of L_g and L_g+100nm. The data was obtained for drain bias of 0.7V.

Table 6.17 summarises the on-state and off-state performance of these devices.

L_G (nm)	L_{SG} (nm)	$I_{d,sat}$ (µA/µm)	$g_{m,max}$ (µS/µm)	V_t (V)	SS @ V_{ds} = 0.7V (mV/dec)
180	280	364	494	+0.01	84 (-0.41V)
180	180	415	477	-0.01	80 (-0.39V)
90	190	408	446	-0.35	202 (+0.15V)
90	90	305	288	-	-

Table 6.17: Summary of on-state and off-state characteristics of 180nm and 90nm gate length devices with aggressively scaled source/gate separations. The gate voltage relative to the threshold voltage (V_g-V_t) at which the sub-threshold swing was determined is shown in brackets for each data point.

The data shows a number of trends. Firstly, reducing the source/gate separation results in increased output conductance, and more pronounced on-state breakdown. Nevertheless, the 180nm gate length devices with 180nm source/gate separation still retain good off-state performance as indicated by the sub-threshold swing.

Both aggressively scaled 90nm gate length devices suffer significant on-state and off-state issues, with a negative shift in threshold voltage and increased sub-threshold swing in the devices with 190nm source/gate separation, and an inability to control the current in the 90nm source/gate separation device.

Even though there is a negative voltage shift, the V_t numbers stay similar for a 90nm L_g device with L_{sg} = 190nm and 1µm. This suggests that there are little short-channel effects taking place from reducing the source/gate and drain/gate gap size. On-state breakdown and shift in V_t of scaled devices suggests however that there are potentially some short-channel effects from scaling the gate length.

Conclusion

A number of conclusions can be drawn from this study. First, the utilization of a gate dielectric and device architecture with known low interface state density is vital when exploring device scaling issues, in particular where off-state performance metrics such as sub-threshold swing are important. The 1 µm source/gate separation devices show that the flatband mode architecture appears to be robust to scaling at least to 90nm, with the layer design and doping strategy adopted in this work. In addition, whilst the more aggressively scaled 180nm devices have encouraging off-state performance, on-state breakdown is a significant issue, which will have to be mitigated by device re-engineering, with particular emphasis on minimizing the lateral diffusion of the ohmic contacts. The 90nm aggressively scaled devices appear to be suffering significantly from this issue and in the most extreme case, to the extent that the devices cannot be turned off.

6.3.3.2 Surface Channel Al_2O_3 gate dielectric stack MOSFET devices

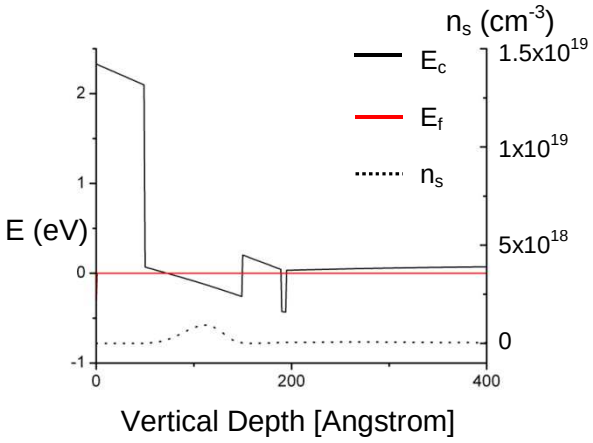
Introduction

The advantage of a GaO/GaGdO gate dielectric stack is that it forms an interface with low density of states on GaAs [101]. The quality of the oxide deteriorates when moving from a GaAs to an $In_xGa_{1-x}As$ interface. To counter this problem the GaO/GaGdO gate dielectric stack MOSFET devices have a buried-channel quantum-well structure with a thin GaAs layer underneath the oxide. The buried-channel structure allows increasing the indium concentration to a maximum of 30% in the channel region while maintaining a GaAs/oxide interface. The drive current of the device is determined by the drift velocity and the number of carriers. The drift velocity is dependent on the mobility and applied field. Therefore, the indium concentration should be as high as possible in the channel region to benefit from the higher mobility values. The buried channel device structure has the drawback of having a relatively large distance between the channel and the metal/oxide interface. This limits the potential to scale the devices as the electrostatic control of the gate reduces as the distance between the channel and the metal/oxide interface increases. This distance will adversely affect the CET value, which will also limit the maximum

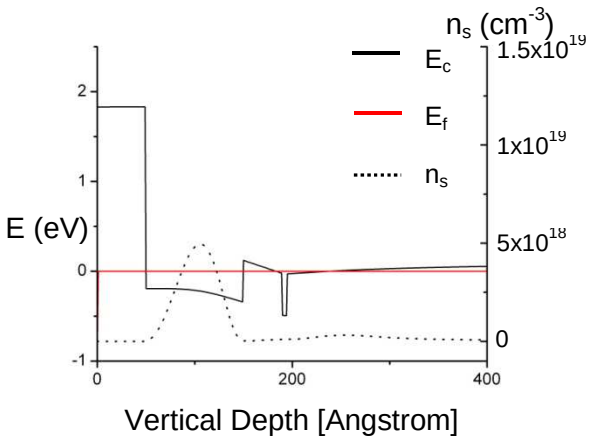
channel thickness for scaled devices with L_g values under 100nm. Further disadvantages of the GGO device structure are a relatively high access resistance. The wide bandgap GaAs/AlGaAs layer underneath the oxide makes ohmic contact formation more difficult because of the larger Schottky barrier. The ohmic contact issue was overcome by using a NiGeAu alloy, which alloys into both the channel and access region. This ohmic contact structure is not Si-processing compatible and the compatible alloying metals have far less vertical and lateral alloying resulting in increased contact resistance values.

To solve the scaling problems of a buried-channel structure the buffer layer between the oxide and the channel is removed, resulting in a surface channel device improving the electrostatic control. The indium concentration of the channel is increased from 30% to 53% for extra drive current. However, the GGO gate dielectric is not suitable for this device structure and an alternative Al_2O_3 gate dielectric is used. The Al_2O_3 grown by atomic layer deposition (ALD) has better gate dielectric properties than MBE grown GGO on $In_{0.53}GaAs$ and features a relatively low interface state density [205]. Also the lattice of the layer structures corresponds with the lattice of InP, which makes integration of this structure on a 200mm Si-platform possible [234]. The heterostructure, delta doping layer and the channel thickness have been optimised with the aid of 1D Poisson – Schrodinger simulations [207] resulting in the c707 and c764 layer structures, which are described in the list of materials in the appendix.

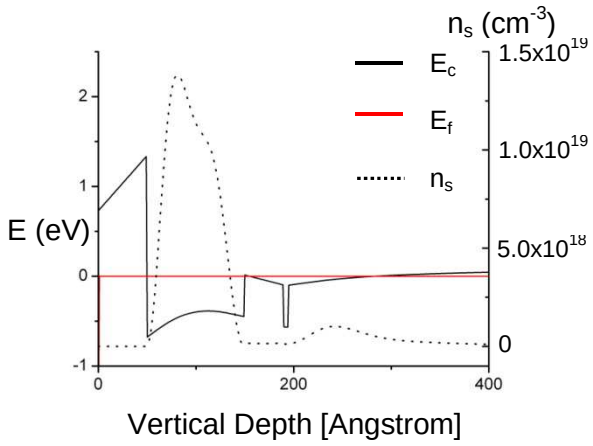
The layer structure is optimised to obtain a positive V_t as shown by the 2D carrier concentration of the channel and is plotted as a function of V_g in Figure 6.40d. The oxide/semiconductor interface states can trap electrons and the corresponding charge population can have detrimental effects on the performance of the gate oxide. These effects can be observed in a CV measurement by a stretch out and frequency dispersion of the CV data, which was discussed in more detail in chapter 5.5. At $V_g = 0V$ there is no significant charge population in the channel and the device is then fully pinched off. Increasing the V_g above the V_t level (Figure 6.40a) results in the conduction band at the bottom of the channel bending below the Fermi level aided by the δ-doping layer. The carrier concentration distribution is then mainly situated near the bottom of the channel away from the oxide/semiconductor interface. This will potentially help to reduce the detrimental effects of the interface scattering. The carrier concentration distribution shifts towards the oxide/semiconductor interface as V_g increases as shown at flatband and at $V_g = 2V$ (Figure 6.40b,c).



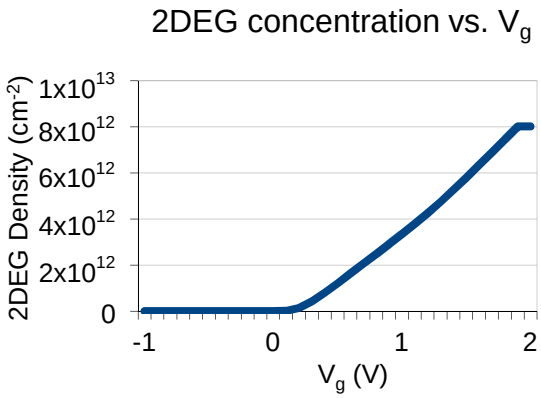
a) E_c, E_f and n_s profiles for V_g = 0.4V



b) E_c, E_f and n_s profiles for V_g = 0.9V



c) E_c, E_f and n_s profiles for V_g = 2V



d) Channel carrier concentration against V_g

Figure 6.40: Poisson - Schrodinger simulation of Al_2O_3 device material

The advantage of this structure is that the ohmic contacts are directly deposited on narrow band-gap material reducing the Schottky barrier height. The higher mobility also results in a lower access region resistance, which should aid reducing the total on resistance. The disadvantage of this structure is that any defects coming from the oxide/semiconductor interface will directly affect the channel resulting in a reduction of the drive current and an increased sub-threshold slope value (SS). The sub-threshold swing is mainly determined by the interface state density (D_{it}) in the oxide, preventing the device from switching off. A good quality oxide interface is then key as the flatband devices have no p-n junctions to aid the sub-threshold performance.

The device fabrication consists of two lithography steps using a wrap around gate. First, a combined gate/marker level using a e-beam evaporated Platinum/Gold gate stack using E-beam lithography and lift-off. The second step consist of source/drain ohmic contacts,

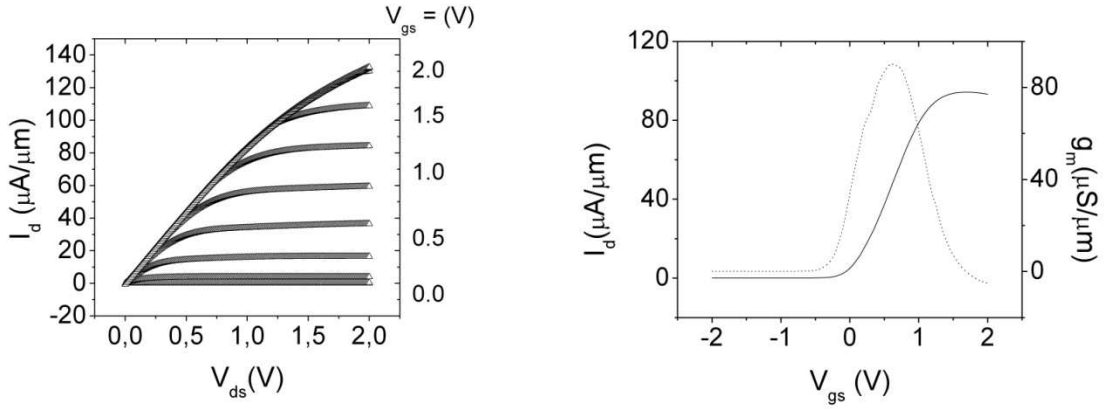
which are patterned by E-beam lithography and are lithographically aligned by making use of Penrose [208] patterns to aid marker alignment accuracy. Prior to metal deposition the Al_2O_3 layer is etched using a selective wet etch in dilute KOH. A Pd/Ge/Ti/Pt (10nm/25nm/30nm/30nm) ohmic contact is then deposited by e-beam evaporation and annealed in a RTA at 400°C for 10s under nitrogen atmosphere.

The impact of scaling the gate lengths has been investigated by using following gate lengths: 100nm, 300nm, 500nm, 1µm, 2µm and 20µm. The access regions have been kept at 1µm to allow for rapid turnaround and stable processing. The design also includes TLM and capacitor structures to measure the ohmic contacts and oxide quality.

Device results

The devices in this work use a similar device layer structure (c707) and processing as in the work presented by S. Bentley et al. [206]. The main difference is the source/drain ohmic contact, which in this case is a Si-processing compatible Pd/Ge/Ti/Pt alloy. TLM measurements indicate that $I_{d,sat}$ should be approximately 280 mA/mm using Pd/Ge/Ti/Pt ohmic contacts on c764 material. To compare the Pd/Ge/Ti/Pt device results to the Ni/Ge/Au device results, device data measured by S. Bentley on c764 material are used, which varies from the results from the c707 device results [206].

The output and transfer characteristics of a MOSFET device with L_g = 20µm can be seen in Figure 6.41.



a) Output characteristics **b) Transfer characteristics (V_d= 1V)**

Figure 6.41: I-V Characteristics of a c764 L_g=20µm device using Pd/Ge/Ti/Pt contacts

On first inspection of Figure 6.41, it is clear that the devices show reduced g_m, $I_{d,sat}$ and I_dV_g response compared to the Ni/Ge/Au [206] devices. This indicates that the source/drain ohmic contacts are worse than the Ni/Ge/Au contacts on c707 material. However, on

resistance (R_{on}) on c707 is significantly lower at 3030Ω.µm than on both c764 devices for L_g = 20µm hence limiting the comparison between the two wafers. The main device parameters are shown in Table 6.18 and show a relatively high contact resistance value for the source/drain ohmic contacts. The contact resistance of the Pd/Ge/Ti/Pt is high compared to the Ni/Ge/Au resulting in a decrease of g_m and $I_{d,sat}$. The sub-threshold slope should not be affected by the ohmic contacts but is predominantly dictated by off state leakage current.

c764	Ni/Ge/Au	Pd/Ge/Ti/Pt
g_m (mS/mm)	103	92.3
$I_{d,sat}$ (mA/mm)	122	103
SS (mV/dec)	169	244.5
R_{on} (Ω.mm)	8.54642	11.0744
R_{SD} (Ω.mm)	0.94	1.82
R_{sh} (Ω/sq.)	333.38	369.42

Table 6.18: Comparison of device parameters between Ni/Ge/Au [206] and Pd/Ge/Ti/Pt source/drain contacts on c764 L_g = 20µm devices

The detailed performance will be discussed by making use of the device data over different gate lengths. Table 6.19 shows a summary of the device parameters over different gate lengths.

L_g	100nm	300nm	500nm	1µm	2µm	20µm
g_m (mS/mm)	112.6	180	188	192.2	188.85	92.3
$I_{d,sat}$ (mA/mm)	155.7	182	188.9	210	188.2	103.1
SS (mV/dec)	566.7	269.4	236.3	250.4	234.2	244.5
R_{on} (Ω.mm)	4.1451	4.295	3.4387	3.6004	4.1166	11.0744
V_{th} (V)	-1.34	-0.22	-0.22	-0.19	-0.16	-0.11

Table 6.19: Overview of detailed device performance of MOSFET devices with variable gate lengths on Al_2O_3 gate dielectric stack device material. Access regions are 1µm.

a) V_t: The device results show a dependence between L_g and V_t. Reducing the size of the gate from 20µm down to 300nm shows a steady decrease in the value of V_t. This is possibly due to a loss in electrostatic control from reducing the gate length. The layer structure has been optimised for an ideal large scale device and this will have to be taken

into account when scaling down MOSFETs to sub 100nm gate pitches. There is a sudden drop in V_t when the gate is scaled to L_g = 100nm due to an over etch of the gate oxide. This can possibly be addressed by moving from a wet etch to a dry etch.

b) $I_{d,sat}$: The $I_{d,sat}$ measured from the TLM's is considerably higher than the $I_{d,sat}$ extracted from the L_g = 20μm devices. The MOSFET devices have been built and measured on the same sample as the TLM's and therefore the access region of the devices should be identical to the gaps between the TLM's in terms of carrier concentration and sheet resistance. The reduction in $I_{d,sat}$ is then the effect of the gate region on the channels performance, reducing the maximum current. The most likely explanation is that there is an increase in trapped charges when depositing a gate metal onto an oxide/semiconductor interface. The trapped charge then limits the maximum carrier concentration, resulting in a reduced $I_{d,sat}$ in the gate region. $I_{d,sat}$ is improved when scaling down the devices as the area underneath the contact becomes relatively smaller compared to the access region Table 6.19. The $I_{d,sat}$ value is then determined by the quality of the ohmic contacts.

c) Sub-threshold performance: The values for the sub-threshold swing are consistently around the 200mV/dec mark even for the scaled devices. These values are large compared to the values extracted from the buried-channel devices indicating a worse oxide/semiconductor interface. This is potentially due to a leaky oxide or increased trapped charges. Slightly lower values were found in the work done by S. Bentley indicating that the quality of the oxide/semiconductor interface will be critical to improve sub-threshold performance. The results for the 100nm device indicate that the oxide is poor and confirm the wet etch issues.

d) I_g: Typically the number for $I_{g,max}$ on buried channel devices is in the order of $1x10^{-9}A/cm^{-2}$ or smaller. The values measured on the devices are in the range of $2x10^{-4}A/cm^{-2}$ in saturation regime and do not scale with L_g. These increased values explain the poor sub-threshold performance. There is a reasonably large non-uniformity between individual devices of over 2 or 3 orders of magnitude suggesting that the uniformity of the oxide needs to be improved. The high leakage current also prevented from performing C-V measurements on this sample.

g) R_{SD}: The contact resistance using a Pd/Ge/Ti/Pt contact structure on identical c764 substrate material is nearly twice as high as the NiGeAu contacts. The contact resistance values are 0,94Ω.mm and 1.82Ω.mm for the NiGeAu and Pd/Ge/Ti/Pt respectively. This is

possibly due to the non optimised etch for Pd/Ge/Ti/Pt contacts, which feature very little lateral alloying into the channel unlike the NiGeAu contact structure. The lack of available substrate material meant that the annealing time and temperature was based on previous results on doped $In_{0.53}GaAs$ material and the wet etch was based on previous work using NiGeAu contact structures. The contact still needs to be further optimised to achieve lower contact resistance values. A Pd/Ge/Ti/Pt annealing temperature test was then performed on c707 material and compared to the NiGeAu results [206] using a AZ400K developer [239], for 2min45s, as a wet oxide etch. The contact resistance using NiGeAu contact structures is 0,57Ω.mm and this corresponds to a specific contact resistivity of $3.9x10^{-6}\Omega.cm^2$ for a sheet resistance of 768.9Ω/sq. The optimal annealing temperature for the Pd/Ge/Ti/Pt contact is around 350°C for 60s, which results in a contact resistance of 0.46Ω.mm and a specific contact resistivity of $6.1x10^{-6}\Omega.cm^2$ for a sheet resistance of 460Ω/sq as seen in Figure 6.42.

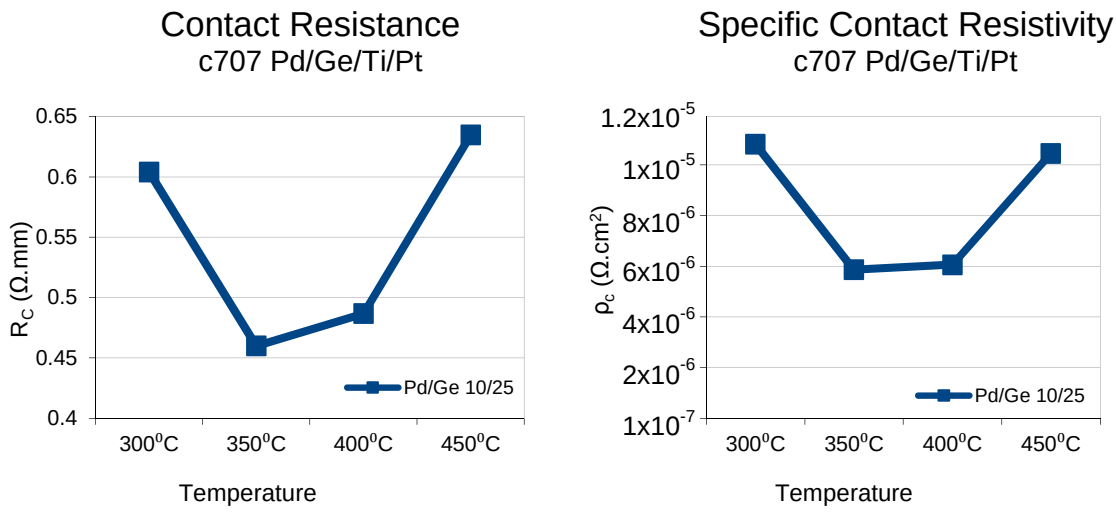


Figure 6.42: TLM results of a scaled Pd/Ge/Ti/Pt ohmic contact structure on Al_2O_3 device material annealed for 60s at 300°C, 350°C, 400°C and 450°C

The difference in sheet resistance can have various causes: the lateral alloying reduces the actual gap size and increases the contact width, which has to be compensated for, making TLM measurements less reliable. The c764 didn't suffer from the sheet resistance variation over temperature and it's then assumed that this is a wafer dependent issue.

Regardless of the sheet resistance variation, the ohmic contact parameters for a Pd/Ge/Ti/Pt structure are in line with the Ni/Ge/Au contact results. The Pd/Ge/Ti/Pt contacts can therefore be used as an alternative Si-compatible contact to the Ni/Ge/Au for

rapid turnaround MOSFET devices. Further optimisation of the oxide etch and annealing times and temperatures is needed to reduce the contact resistance.

Comparing the ohmic contact results to MOSFET devices, with high concentration Indium channel materials and Pd/Ge ohmic contacts, the results are similar to the work done by X. Gong [240] and H.-C. Chin [238], on Si-implanted $In_{0.7}GaAs$, with respective $R_{S/D}$ values of 2.25Ω.mm [240] and 1Ω.mm [238]. The work done by T. D. Lin [45] shows that specific contact resistivity values as low as $1.86.10^{-6}$Ω.mm can be obtained, resulting in high gm (700ms/mm) and $I_{d,sat}$ (960mA/mm) values, for self aligned inversion mode MOSFET devices. Other Si-compatible ohmic contact strategies such as nickelide source/drain regions have shown reasonably high contact resistances, on Si-implanted $In_{0.7}GaAs$, of 7.6Ω.mm [216]. So far the values required by the ITRS have only been approached with contacts with regrown source drain regions [49, 246] or recess gate device structures [50, 241, 242, 243, 244, 245] and should be the main focus in future work.

Conclusion

The surface-channel flatband architecture has shown promising mobility values with corresponding high carrier concentrations. Well behaved surface channel MOSFET devices were made with both NiGeAu and Pd/Ge/Ti/Pt based ohmic contacts. The performance of the Pd/Ge/Ti/Pt contacts is inferior to the NiGeAu but can be improved after optimising various parameters such as annealing temperature, oxide etch and the ratio of Pd/Ge layer thickness, however the stringent ITRS requirements are unlikely to be met and alternative contact strategies such as regrowth should be considered. The Al_2O_3 gate stack also requires an improvement to challenge the GaO/GaGdO gate dielectric stack in terms of leakage and density of states. Future work should focus on reducing ohmic contact resistance and improving the Al_2O_3 gate dielectric stack.

7 Scaled ohmic contacts

7.1 Introduction

As the size of MOSFETs decreases following the ITRS [1] technology generations, the resistance of source/drain contacts is critical as their dimensions scale down as well. The most common method of determining the ohmic contact resistance (TLM [85]) generally uses structures, which are at least two times larger in dimension than the transfer length in order to eliminate current crowding effects [88]. Another issue is that nearly all the current measurement methods such as TLM, CTLM and CBKR (chapter 5) utilise an approximation in the calculations, where it is assumed that the sheet resistance underneath the contact (R_{sk}) is the same as the bulk semiconductor sheet resistance between the contacts (R_{sh}). This approximation impedes the use of an accurate simulation showing the behaviour of the contact resistance below the transfer length as the sheet resistance underneath the contact can vary from the bulk semiconductor sheet resistance. There are, however measurement methods, which include the sheet resistance underneath the contact such as: FCTLM [209], 6 – terminal CBKR [210], end resistance measurement [220] and CTLM using a curve fitting based technique [42]. Apart from the FCTLM structure, these measurement structures have dimensions well above two times the transfer length of the ohmic contact and the behaviour of scaled contacts below the transfer length has to be modelled. This work focuses on the actual ohmic contact resistance of a scaled sub-micrometer contact and is then compared to the results obtained from ordinary 150μm x 150μm pad sized TLMs. The results from the ordinary TLMs are then used in a simulation to predict the impact of current crowding effects and then compare them to the measured results from the scaled contacts. If the two deviate the resistance underneath the contact is likely to be different from the bulk semiconductor sheet resistance. The difference between predicted and measured transfer length can then be used to extract the sheet resistance underneath the contact. This experimental investigation necessitated the realisation of a new type of test structure based around physically small ohmic contacts. A new TLM test structure was therefore designed and tested and is described in the following sections.

7.2 Theory

7.2.1 Extraction of sheet resistance underneath a contact (R_{sk})

As discussed in chapter 5.3.2, one way of determining the sheet resistance underneath the contact is the contact end resistance extraction method. Another way is scaling the contacts

below the transfer length, where the transfer length can be determined experimentally from the point where the current crowding effects start to take place. The sheet resistance underneath the contact can then be found in a similar way as used in the contact end resistance method. The total resistance for contacts with a length greater than two times L_T is given in Equation 5.15 and can be split up using a standard linear function:

$$R(x) = A + Bx \quad (7.1),$$

where R is the total resistance (R_T), x is the gap size between the TLM contacts, B is determined by the normalised bulk semiconductor sheet resistance (R_{sh}/W) and A is equal to the contact resistance of two contacts ($2.R_C$). Solving the total resistance equation for $R_T = 0$ Ω.mm gives an absolute value (L_x);

$$L_x = \frac{2.R_{sk}.L_T/W}{R_{sh}/W} = \frac{2.R_{sk}.L_T}{R_{sh}} \quad (7.2)$$

The ratio between L_T and L_x will then directly determine the ratio between R_{sh} and R_{sk}. The value of R_{sk} can then be found by combining the results from ordinary contacts and the scaled ohmic contacts. Equation 7.2 does not take the metal sheet resistance (R_m) into account. In order to incorporate the metal sheet resistance, the R_C factor in Equation 5.15 has to be adjusted according to the model presented by Scott et al. [82] using Equation 5.10. This includes the contact length (d), which will determine whether current crowding effects take place. The complete equation for the total resistance including the metal sheet resistance and current crowding effects then becomes:

$$R_C = \frac{(R_{sk}.R_m)+(R_m{}^2+R_{sk}{}^2).\cosh(\frac{d}{L_T})}{W.L_T{}^{-1}.(R_m+R_{sk}).\sinh(\frac{d}{L_T})} = \frac{R_{sk}.R_m}{W.L_T{}^{-1}.(R_m+R_{sk}).\sinh(\frac{d}{L_T})} + \frac{(R_m{}^2+R_{sk}{}^2).\cosh(\frac{d}{L_T})}{W.L_T{}^{-1}.(R_m+R_{sk}).\sinh(\frac{d}{L_T})} \quad (7.3)$$

This equation can be simplified when $d>>10.L_T$; the $\sinh(d/L_T)$ factor becomes large and the first term then becomes small and can be ignored leaving:

$$R_C = \frac{(R_m{}^2+R_{sk}{}^2).\cosh(\frac{d}{L_T})}{W.L_T{}^{-1}.(R_m+R_{sk}).\sinh(\frac{d}{L_T})} = \frac{(R_m{}^2+R_{sk}{}^2).L_T}{W.(R_m+R_{sk})}.\coth(\frac{d}{L_T}) \quad (7.4)$$

With the condition $d>>10.L_T$, the $\coth(d/L_T)$ factor becomes 1 and so (7.4) reduces to:

$$R_C = \frac{(R_m{}^2+R_{sk}{}^2).L_T}{W.(R_m+R_{sk})} \quad (7.5)$$

Substituting (7.3) into (7.2) gives:

$$L_x = \frac{2.R_C}{R_{sh}/W} = \frac{2.\frac{(R_m{}^2+R_{sk}{}^2).L_T}{W.(R_m+R_{sk})}}{\frac{R_{sh}}{W}} = \frac{2.(R_m{}^2+R_{sk}{}^2).L_T}{R_{sh}.(R_m+R_{sk})} \quad (7.6)$$

All the parameters apart from R_{sk} can be extracted from the ordinary TLM structure and the scaled structure. The absolute value L_x is the extrapolated value from the ordinary TLM's where R_T = 0Ω.mm. R_{sh} can measured using a Van der Pauw structure or alternatively can be extracted from the TLM result.

R_m can be found by measuring the metal sheet resistance and L_T is found by the transfer length extracted from the scaled TLM structures. The R_{sk} value is extracted from Equation 7.6 by solving the following quadratic equation:

$$\frac{L_x.R_{sh}}{2.L_T} = \frac{R_m{}^2+R_{sk}{}^2}{R_m+R_{sk}} \tag{7.7}$$

The value for R_{sk} will then be a positive value, ignoring the negative term of the quadratic equation:

$$R_{sk} = \frac{\left(\frac{L_x.R_{sh}}{2.L_T}\right)+\sqrt{\left(\frac{L_x.R_{sh}}{2.L_T}\right)^2 + 4.R_m.\left(\frac{L_x.R_{sh}}{2.L_T}\right)-4.R_m^2}}{2} \tag{7.8}$$

The specific contact resistivity value can then be extracted from L_T given in Equation 5.10

7.2.2 Random Error analysis on a TLM measurement including R_{sk}

When using the TLM method to extract the specific contact resistivity and sheet resistance an error analysis should be taken into account [211]. The work by H-J. Ueng et al. [211] considers the Berger model only and has to be expanded to take the sheet resistance underneath the contact into account from the Reeves model. As described in equation 5.22, the R_{sk} value can be found by comparing the measured L_T with L_x. The random error is then found by extrapolating a straight line with correlated errors for the L_x value. Solving the linear Equation 7.1 for L_x, we can find:

$$A = 2.R_C \tag{7.10}$$

$$B = R_{sh}/W \tag{7.11}$$

$$L_x = -A/B \tag{7.12}$$

This is a negative value, however when calculating the R_{sk} value we use the absolute value.

By differentiating equation 7.12 the uncertainty in L_x can be derived:

$$\Delta L_x = \left(\frac{\delta L_x}{\delta A}\right)\Delta A + \left(\frac{\delta L_x}{\delta B}\right)\Delta B + \left(\frac{\delta L_x}{\delta W}\right)\Delta W \tag{7.13}$$

$$\Delta L_x = \left(\frac{\delta(\frac{A}{B})}{\delta A}\right)\Delta A + \left(\frac{\delta(\frac{A}{B})}{\delta B}\right)\Delta B + \left(\frac{\delta(\frac{A}{B})}{\delta W}\right)\Delta W$$

After derivation:

$$\Delta L_x = \left(\frac{1}{B}\right)\Delta A + \left(\frac{A}{B^2}\right)\Delta B + \left(\frac{A}{WB}\right)\Delta W \tag{7.14}$$

Finding relative error:

$$\frac{\Delta L_x}{L_x} = \frac{\left(\frac{1}{B}\right)\Delta A + \left(\frac{A}{B^2}\right)\Delta B + \left(\frac{A}{WB}\right)\Delta W}{\left(\frac{A}{B}\right)}$$

$$\frac{\Delta L_x}{L_x} = \left(\frac{\Delta A}{A}\right) + \left(\frac{\Delta B}{B}\right) + \left(\frac{\Delta W}{W}\right) \tag{7.15}$$

The total random error is then given by:

$$\Delta A = (\sigma_{A|\sigma_d,\sigma_R} + \sigma_{A|\sigma_W}) \tag{7.16}$$

$$\Delta B = (\sigma_{B|\sigma_d,\sigma_R} + \sigma_{B|\sigma_W}) \tag{7.17}$$

From [211]:

$$\sigma_{B|\sigma_d,\sigma_R} = \left(\frac{2\sqrt{3}}{\sqrt{N}\, d_{max}}\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2} \tag{7.18}$$

$$\sigma_{A|\sigma_d,\sigma_R} = \left(\frac{2}{\sqrt{N}}\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2} \tag{7.19}$$

$$\sigma_{B|\sigma_W} = \left(\frac{1}{\sqrt{N}}\right)\left(\frac{B}{W}\right)\sigma_W \tag{7.20}$$

$$\sigma_{A|\sigma_W} = \left(\frac{1}{\sqrt{N}}\right)\left(\frac{A}{W}\right)\sigma_W \tag{7.21}$$

The relative error for L_x can now be found by using Equation 7.15 and substituting ΔA and ΔB by (7.16) and (7.17) using Equations 7.18, 7.19, 7.20, 7.21.

$$\frac{\Delta L_x}{L_x} = \frac{\left(\left(\frac{2}{\sqrt{N}}\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2}\right) + \left(\left(\frac{1}{\sqrt{N}}\right)\left(\frac{A}{W}\right)\sigma_W\right)}{A} + \frac{\left(\left(\frac{2\sqrt{3}}{\sqrt{N}\, d_{max}}\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2}\right) + \left(\left(\frac{1}{\sqrt{N}}\right)\left(\frac{B}{W}\right)\sigma_W\right)}{B} + \frac{\left(\left(\frac{1}{\sqrt{N}}\right)\sigma_W\right)}{W} \tag{7.22}$$

$$\frac{\Delta L_x}{L_x} = \left(\frac{1}{\sqrt{N}}\right)\left(\left(\left(\frac{2}{A}\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2}\right) + \left(\left(\frac{1}{W}\right)\sigma_W\right) + \left(\left(\frac{2\sqrt{3}}{B\, d_{max}}\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2}\right) + \left(\left(\frac{1}{W}\right)\sigma_W\right) + \left(\left(\frac{1}{W}\right)\sigma_W\right)\right) \quad (7.23)$$

$$\frac{\Delta L_x}{L_x} = \left(\frac{1}{\sqrt{N}}\right)\left(\left(\left(\left(\frac{2}{A}\right) + \left(\frac{2\sqrt{3}}{B\, d_{max}}\right)\right)\sqrt{B^2\sigma_d^2 + \sigma_R^2}\right) + \left(\left(\frac{3}{W}\right)\sigma_W\right)\right) \quad (7.24)$$

Working out (7.16) using (7.2) and (7.3) we find the relative error for L_x:

$$\frac{\Delta L_x}{L_x} = \left(\frac{1}{\sqrt{N}}\right)\left(\left(\left(\left(\frac{W}{\sqrt{\rho_c R_{sh}}}\right) + \left(\frac{2\sqrt{3}W}{R_{sh}\, d_{max}}\right)\right)\sqrt{\left(\frac{R_{sh}}{W}\right)^2\sigma_d^2 + \sigma_R^2}\right) + \left(\left(\frac{3}{W}\right)\sigma_W\right)\right) \quad (7.25)$$

Variables used:

N: Number of measurements of different gap spacings

W: TLM width

ρ_c: Specific contact resistivity found by using Berger model

R_{sh}: Sheet resistance of the semiconductor layer

d_{max}: Maximum gap size of TLM

σ_d: Absolute error of the gap size between TLM's. (standard deviation)

$$\sigma_d^2 = \frac{\Sigma(\Delta d_i)^2}{N-1} \quad (7.26)$$

σ_W: Absolute error of the contact width of the TLM (standard deviation)

$$\sigma_W^2 = \frac{\Sigma(\Delta W_i)^2}{N-1} \quad (7.27)$$

σ_R: Absolute error of the measurement of the resistance of the TLM (standard deviation)

$$\sigma_R^2 = \frac{\Sigma(\Delta R_i)^2}{N-1} \quad (7.28)$$

To find the random error for R_{sk} we can use the principles of error propagation using Equation 2:

$$R_{sk} \pm \frac{\Delta R_{sk}}{R_{sk}} = \frac{1}{2} \frac{\left(L_x \pm \frac{\Delta L_x}{L_x}\right)\left(R_{sh} \pm \frac{\Delta R_{sh}}{R_{sh}}\right)}{\left(L_T \pm \frac{\Delta L_T}{L_T}\right)} \tag{7.29}$$

When adding or dividing, the relative errors have to be added up.

$$\frac{\Delta R_{sk}}{R_{sk}} = \frac{1}{2}\left(\frac{\Delta L_x}{L_x} + \frac{\Delta R_{sh}}{R_{sh}} + \frac{\Delta L_T}{L_T}\right) \tag{7.30}$$

The unknown factor here is the relative random error from the transfer length extraction method. The transfer length is found by matching simulated data to measured data of scaled contacts, which makes it hard to define the right error. First, there is the random error by measuring the scaled ohmic contacts and secondly, there is the error of matching the curves. The relative error for L_T can be determined by finding the error related to the scaled ohmic contacts. However, the error of the curve fit is more difficult to determine and in this case the relative errors of the L_T and L_x extraction are added. This error will be significantly larger than the relative error of R_{sh}. Hence it is crucial to have excellent lithography and repeatability of the scaled ohmic contacts. Increasing the number of measurements for different scaled contact lengths will help to diminish the random error of the R_{sk} extraction method.

7.3 Experimental

To be able to investigate the current crowding effects, ohmic contacts have to be built with contact lengths smaller than the transfer length. The transfer length varies with the quality of the ohmic contact but is generally between 2µm and 0.5µm. Therefore, physically small ohmic contacts with contact lengths starting from 100nm have been designed and manufactured and were then compared to simulated data extracted from ordinary TLMs with contact lengths of 150µm. To enable a comparison between each, ohmic contact metals were chosen, which do not diffuse into the underlying semiconductor material. In this way lateral alloying is addressed and the properties of the semiconductor material underneath the contacts should be identical for both scaled and ordinary TLM test structures, allowing for a direct comparison between ordinary and scaled ohmic contacts. The ohmic contacts on both test structures can be affected by the processing, resulting in ohmic contacts, which are most probably not going to be optimal in terms of specific contact resistivity. As the aim of the experiment was primarily to investigate the current

crowding effects, it was not felt that this was a significant impediment, at least in the first instance.

Two types of designs were used in this work. The main difference between the two designs is how the large measurement pads connect to the scaled ohmic contacts. Both have their advantages and disadvantages and are described in following sections. The ohmic contacts were measured using an Agilent B1500 series semiconductor parameter analyser with a four probe configuration to account for the series resistance of the cables, probes and connectors.

7.3.1 Scaled structure first version

7.3.1.1 Design

The scaled TLM's in this design make contact via a big pad through a narrow line onto a mesa, as shown in Figure 7.1. The narrow lines are the ohmic contact structures and have contact lengths of 100nm, 200nm, 500nm and 1µm. This frame should allow the current crowding effects to be monitored together with the contact resistance R_C. The mesas are varied with different widths: 5µm, 4µm, 3µm, 2µm, 1µm and 0.5µm. The gap sizes between the TLM pads are identical to the ordinary TLMs, which are present on the same cell and therefore are subjected to the same processing steps. The ordinary TLMs are then used to determine the specific contact resistance, sheet resistance and contact resistance. The IM-InGaAs20 material is used, which enables the formation of well isolated mesas. The full layer structure can be found in the list of materials.

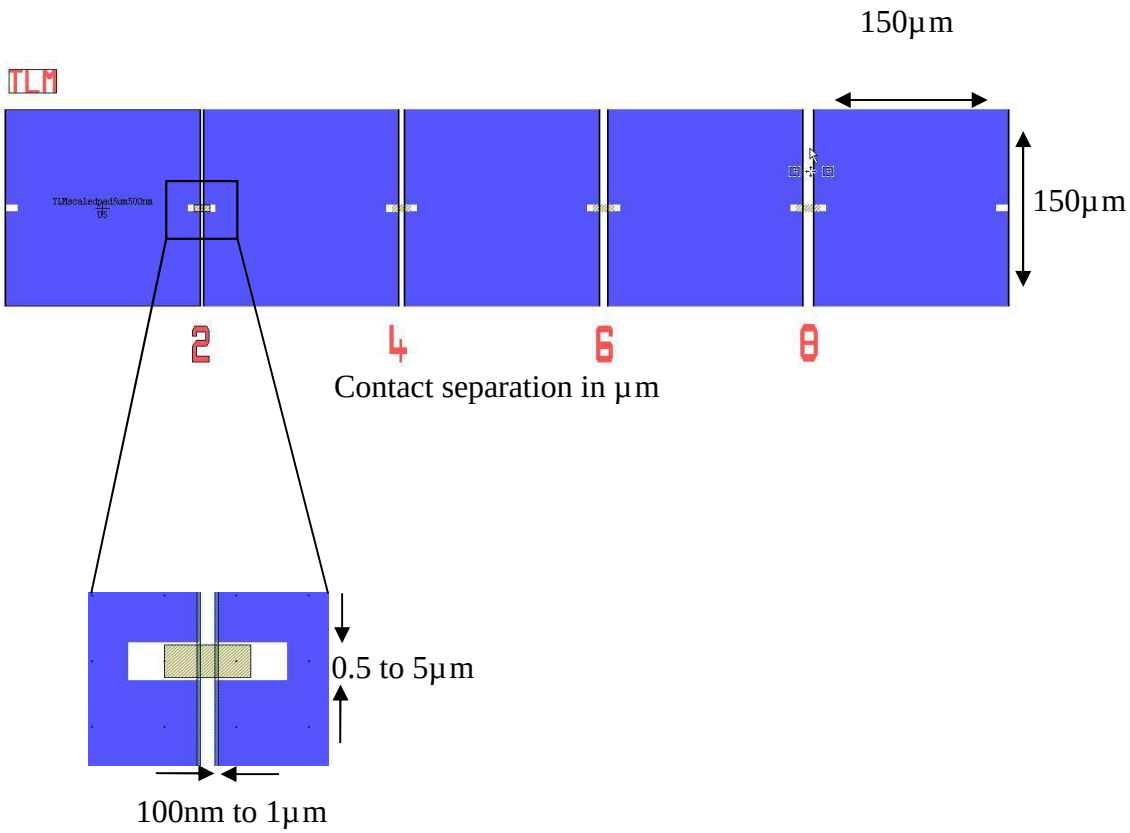


Figure 7.1: Design of first aggressively scaled TLM structure

7.3.1.2 Fabrication

The fabrication process consists of four main steps: marker definition and deposition, mesa isolation, ohmic contact definition and metallisation and measurement contact pad definition and metallisation. The marker layer is used to align subsequent levels. The markers are formed by depositing a bi-layer of PMMA on the substrate, E-beam patterning, resist development and metal deposition and lift off of a 100nm thick layer of gold. The choice of metals and its thickness is key for the automatic alignment of the Vistec VB6 E-beam tool as thinner layers provide insufficient contrast for automatic image processing using SEM images from the E-beam tool. The mesa etch level includes the deposition of a bi-layer PMMA resist, E-beam patterning using marker alignment, resist development and a mesa etch. The mesa etch is an optimised wet etch using a 1:1:100 H_2O_2: orthophosphoric acid: H_2O solution for 45s. This removes the $In_{0.53}GaAs$ and $In_{0,52}AlAs$ layer providing an electrical isolation between scaled ohmic contact lines. After the etch the resist mask is removed using acetone and IPA before the next processing step. The metal deposition was originally intended to form ohmic contacts and contact pads at the same time. However, processing issues, explained in the section below, prevented this. Therefore, the ohmic contact step involves the deposition of a bi-layer of PMMA resist, E-

beam patterning using marker alignment, resist development and lift-off based metal deposition. The last step is identical to the previous step, however different windows are opened in the resist allowing for the deposition of contact pad metal. The advantage of the extra step is that the ohmic contact metal can be different than the pad metal.

- Dose test

In order to create sub-micrometer features, dose tests were carried out alongside the work published by O. Ignatova [212]. Two resist thicknesses of 150nm and 280nm were used in this work, however for the scaled ohmic contacts a layer thickness of 280nm was used to obtain a large enough undercut for the lift-off of a 100nm thick layer of ohmic contact metal. Dose tests were performed to achieve contact lengths of 100nm, 200nm, 500nm and 1μm. The feature sizes were examined using a Hitachi S4700 SEM and analysed using automatic image processing using a macro on ImageJ software.

- Backscattering effects

The close proximity of relatively large contact pads resulted in a greater exposure dose of the scaled ohmic contact area due to backscattering effects. This led to larger ohmic contact lengths and made the process unreliable and therefore it was decided to write the ohmic contacts and the pads in different steps. The effects of the backscattering can be observed in Figure 7.2 and manifest themselves as rounded edges and a non perfectly rectangular shape of the gap between the metal contact pads.

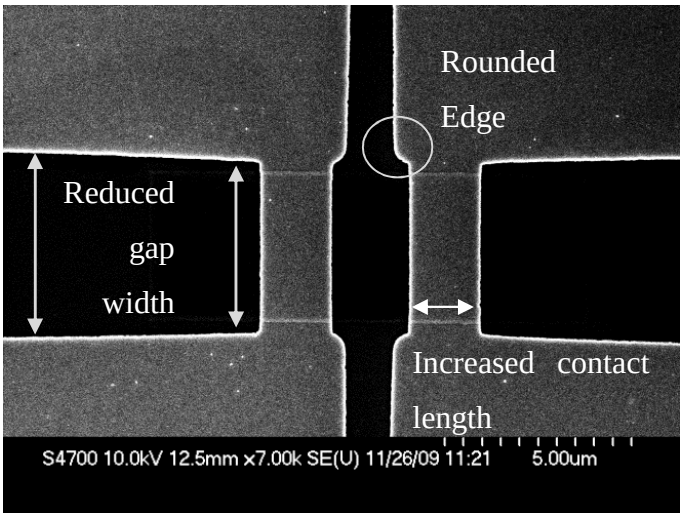
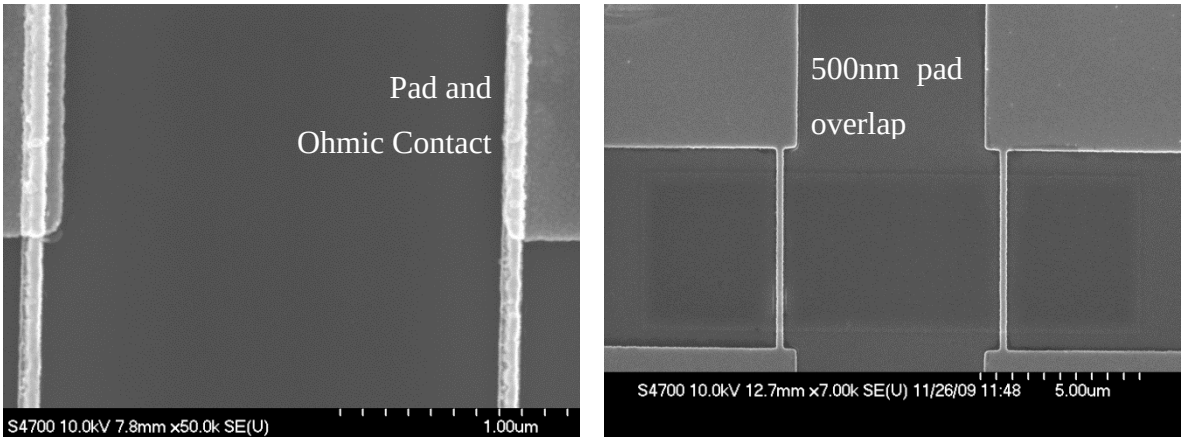


Figure 7.2: SEM micrograph of scaled ohmic contact with overexposed area's due to backscattering effects

- Alignment

The markers used in this work allow for a lithography alignment accuracy of +/- 100nm. This resulted in ohmic contacts sometimes being on the edge or not touching the contact pads, as shown in Figure 7.3a. This problem was solved by moving the ohmic contact wires back by 500nm, as shown in Figure 7.3b resulting in a higher yield. The different gap sizes between the contacts then have to be taken into account when analysing the data.



(a) **(b)**

Figure 7.3: SEM micrograph of alignment issues on scaled ohmic contacts

- Access resistance

A potential additional series resistance could arise where the scaled ohmic contact is connected to the contact pad. This resistance would be in series with the R_C value and therefore has to be kept to a minimum. This can be done by minimising the distance between the contact pad and the mesa structure.

- Mesa etch variability

The mesa etch is a wet etch process, as described in chapter 4.5, which can laterally etch material underneath the resist profile. Variability in processing can cause the mesa to become wider or smaller than originally intended by over 1 μm. As the contact width plays a crucial role in the accurate extraction of R_C, it is important that relative errors are minimised. Having an absolute error of over 1μm will then cause unreliable measurement data and therefore a second design was made with contact widths of 150μm, which reduces the relative error of the contact width significantly.

7.3.2 Scaled structure second version

7.3.2.1 Design

The purpose of designing a new scaled ohmic test structure is to reduce the mesa etch variability and eliminate series resistances between the ohmic contact and the measurement pad. The high resolution ohmic contact will be made in the same metal run as the pad metal hence assuring there will be little resistance between the ohmic contact and pad layer. One approach is to use Si_3N_4 as a mask and use the insulating properties of Si_3N_4 to isolate the pad from the active $In_{0.53}GaAs$ material. This strategy has the advantage of not needing a mesa etch either and passivates the semiconductor material at the same time. However, there is still an isolation etch present, which is necessary to prevent the current to flow through the scaled ohmic contact on the opposite side of the TLM pad as shown on Figure 7.4. The opposite high resolution ohmic contact could become a parallel resistance and therefore influencing the measurement in a detrimental way. This design has one great disadvantage over the previous: ohmic contacts that require alloying and, which react with the $In_{0.53}GaAs$ layer underneath are unsuitable. This means the current NiGeAu and PdGe contact strategies cannot be tested using this structure, which is still possible with the previous one. But it should provide a reliable test bed to show the effects of scaling contacts.

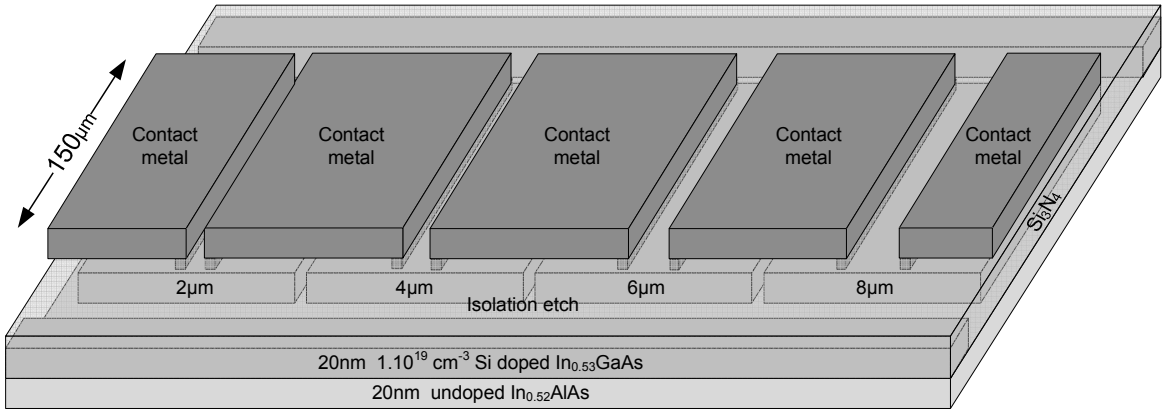


Figure 7.4: Design of second aggressively scaled TLM structure

7.3.2.2 Fabrication

The process consists of four E-beam runs similar to the previous design: markers, isolation etch, ohmic contacts and contact pads. However, there is an additional Si_3N_4 run and Si_3N_4 etching is required. The Si_3N_4 is deposited, using ICP-CVD, after the isolation etch and a clean of the sample. With the Si_3N_4 in place the PMMA layer, which will be used to write

the ohmic contact lines is deposited. After E-beam patterning and development, the sample will undergo a low damage RIE dry etch using SF_6 [222] to remove the Si_3N_4 in the corresponding areas. This up to date is still a slightly damaging process (chapter 4.4.3), so the ohmic contacts will probably be slightly worse because of this processing step. However, this is not necessarily a bad thing, the worse the contact is, the clearer the scaling effects become, as long as the contact still has ohmic contact behaviour. The last step is applying a new layer of PMMA in which the big pad areas will be written. Similar to the previous step the ohmic contact wires are moved 500nm back to compensate for any alignment issues. After developing and ashing the sample the pad and ohmic contact areas are exposed and the contact metal contact gets deposited. The full process can be found in appendix A.2 and is shown in Figure 7.5. The different processing steps also allowed for the integration of different test structures such as CTLM and CBKR. These could then be measured alongside the ordinary and scaled TLMs.

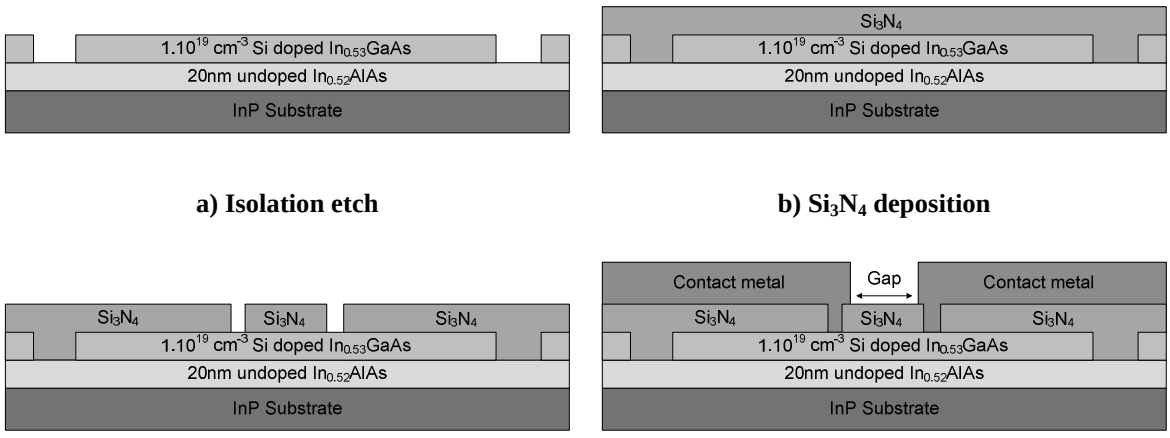
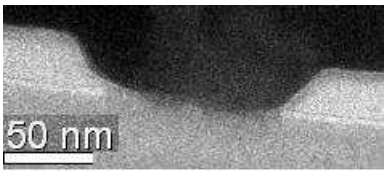


Figure 7.5: Scaled ohmic contact structure processing steps on IM-InGaAs20 substrate

Contact length verification

The contact length dimensions used in this design cannot be measured using ordinary top down SEM images as used in the first design. This is due to the fact that theoretically the Si_3N_4 etch is anisotropic and should feature a vertical etch profile, however in practice the etch profile is not perfectly vertical. The contact length observed from the top will therefore be bigger than the actual contact length at the metal/semiconductor interface. This problem was addressed by preparing small samples, using Focussed Ion Beam milling, in order to measure the contact lengths at the interface between the metal and the semiconductor using cross section TEM. The respective contact lengths and cross section

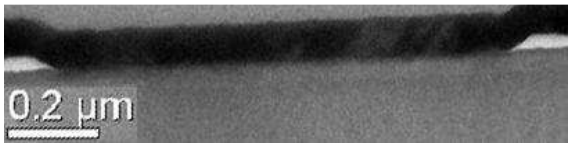
TEM images are shown in Figure 7.6, which also show the non-vertical Si_3N_4 etched profile. Nearly all the contact lengths correspond to the original design apart from the 200nm contact and therefore a 250nm contact length will be used in the simulations.



a) Measured contact length between 90nm and 100nm

b) Measured contact length between 240nm and 260nm

c) Measured contact length between 475nm and 490nm



d) Measured contact length between 990nm and 1000nm

Figure 7.6: Detailed micrograph of TEM cross section scaled contact lengths of 100nm, 200nm, 500nm and 1000nm

Fabrication issues

The initial test samples, using a Ti/Pt (10nm/80nm) contact metal, went through a full cycle of processing however the last layer failed, as shown in Figure 7.7. The Ti/Pt peeled off the Si_3N_4 and actually seemed to have ruptured the Si_3N_4 as well. The cause of this problem could be either metal stress related or unclean surface prior to Si_3N_4 deposition. To mitigate these problems, the metal contact was changed to gold (100nm) and an extra ash and surface clean was introduced prior to Si_3N_4 deposition. The ohmic contact was no longer Si processing compatible but it was used as a proof of concept. After this, the metal peeling issue reduced dramatically resulting in far better yield.

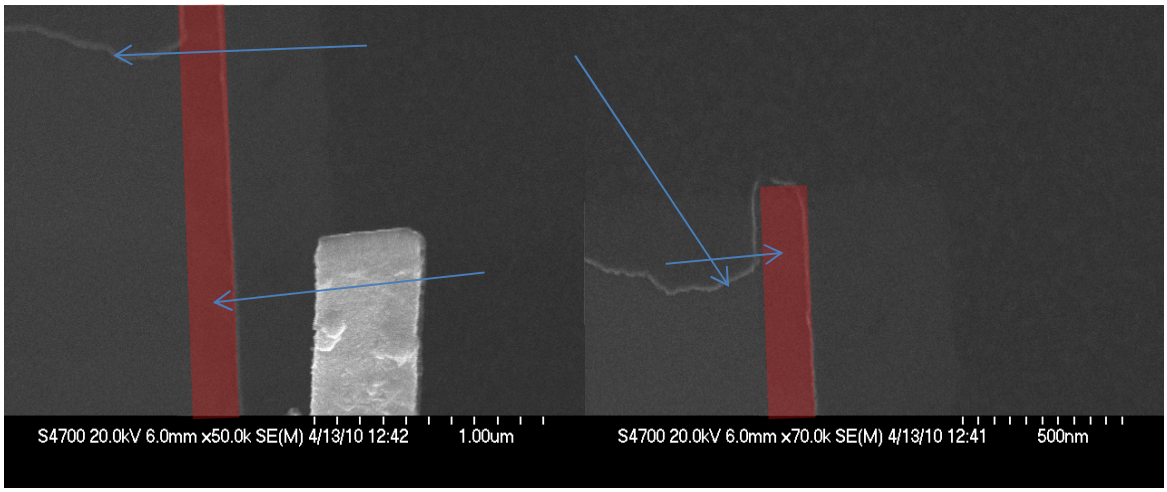


Figure 7.7: SEM micrographs of the scaled ohmic contact structure showing the missing Ti/Pt metal and damage to the Si_3N_4 layer.

7.3.3 Summary

Both designs have their advantages and disadvantages. The main disadvantage of the second design is the added complexity of the Si_3N_4 layer and etch. This led to processing issues at the initial stages, which were resolved by changing the process and metal. As previously stated the second design should feature a smaller variability in measurement due to the wider contact width. However, the first design could be further optimised if possible using dry etch of to obtain an anisotropic mesa etch with reduced lateral etching, hence reducing the variability between the contacts as well.

7.4 Experimental results

The results are split up in three sections, which cover the data from the two designs and a comparison between the different contact resistance extraction methods. The different sections relate to the individual samples with their respective sample numbers. The first section covers the results from the first design, the second section (Design 2a) features a comparison between the second design and the end resistance extraction method and the final section (Design 2b) compares the scaled devices using the second design to the results obtained from a CTLM structure. The CBKR structure was tested but featured very poor yield and unrealistic contact resistance values. This is possibly due to the fact a wet etch is used, which does not comply with the exact dimension required by a CBKR structure [96]. Both test structures feature twelve scaled TLM structures for each contact length and each result shown for the scaled structures has been measured using a minimum of eight structures. Given the larger size of the CTLM structure only two structures were measured.

7.4.1 First design results

The metallisation used on this sample is a Ti/Pt bi-layer with a thickness of 90nm (Ti:10nm/Pt:80nm). The results of the different measurements are shown in Table 7.1 with the standard deviation included to the measured results. The simulated data does not include the standard deviation and can therefore be recognised more easily. The average ρ_c and L_T values are not given for the Scaled TLM data because of the fact that the current crowding effects will affect these values and produce an erroneous outcome. Also the extracted values for standard deviation do not take into account any variability of the contact dimensions or position.

The results from the ordinary TLM data are poor with relatively high sheet resistance and specific contact resistivity, as shown in Table 7.1, compared to results obtained in chapter 6.3.2 on the same material. The minimum correlation between the data points of various gap sizes is 0.99 for the ordinary TLM data and 0.9 for the scaled data set. The transfer length measured from the ordinary TLM measurements indicates that the contact lengths for the scaled TLMs are well below the transfer length ($d < 2\mu m$). If the sheet resistance underneath the contact is then equal to the bulk sheet resistance, the current crowding effects should become very clear on the scaled contacts. However, observing the behaviour of the scaled contacts in Figure 7.8, it appears that the transfer length derived from the ordinary TLM measurement does not correspond with the actual scaled contact measurement. The transfer length estimated from the scaled contact structures is more in the region of 200nm. This would mean the actual transfer length is one order of magnitude smaller than measured from the TLM data. Since the transfer length is in direct relationship with R_{sk} and R_{sh}, as shown in Equation 5.22, the resistance underneath the contact would be around $5k\Omega$. However, the contact resistance values extracted from the scaled structures are well below the contact resistance obtained from the ordinary TLM measurement. This is possibly due to the fact that the actual mesa width differs from the design and is indicated by the larger value and great variability in sheet resistance when measuring scaled contacts, which also explains the lower correlation value compared to the ordinary TLM measurement. An accurate transfer length and resulting R_{sk} and ρ_c values can therefore not be extracted as curve fitting needs to take place. The choice was then made to abandon this design and focus on the second design, which should feature less variability between scaled contact measurements.

	Ordinary TLM	Scaled TLM
R_C (Ω.mm)	1.11 ± 0.19	-
R_{sh} (Ω/sq)	525.31 ± 62.49	739.19 ± 150
ρ_c ($\Omega.cm^2$)	$2.52x10^{-5} \pm 1.46x10^{-5}$	-
L_T (µm)	2.17 ± 0.66	-

Table 7.1: Summary results of scaled ohmic contacts sample s4126

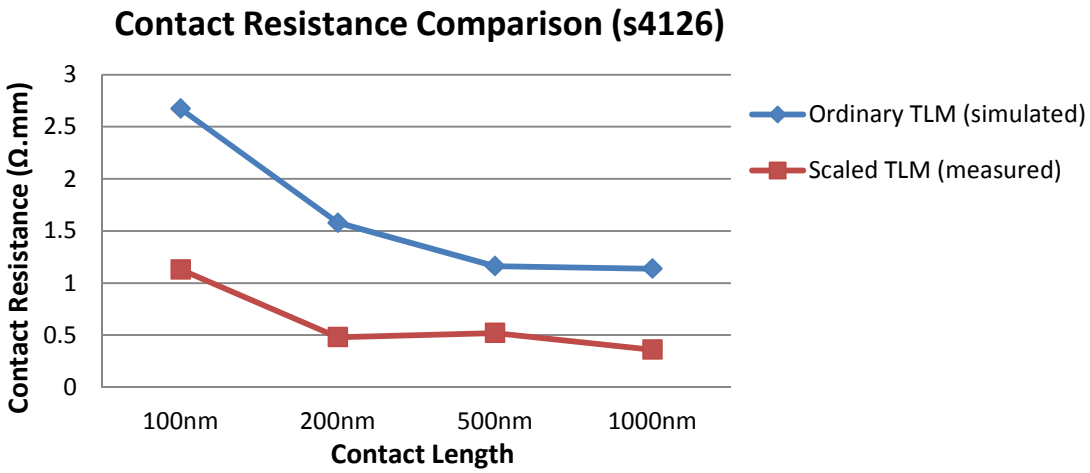


Figure 7.8: Contact Resistance comparison between scaled TLM structures and simulated data based on the ordinary TLM measurements on sample s4126

7.4.2 Second design results

7.4.2.1 Design 2a

The aim of this experiment is to compare the results from the ordinary TLM measurement method to the end resistance measurement method. Two different measurement methods using the end resistance to extract the contact resistance were used; one proposed by Reeves et al. [81] and one proposed by Berger et al. [89]. The measured data from the scaled structure results were then compared to the contact resistance extracted with ordinary TLM structure and the end resistance measurement on the same material. In order to make a direct comparison the contact resistance below, the transfer length has to be simulated. The simulation makes use of the Berger Model [89] and uses the specific contact resistivity and sheet resistance to calculate the normalised contact resistance when scaled below the transfer length.

The metallisation used on this sample is gold with a layer thickness of 100nm. The correlation between the data points of various gap sizes of the ordinary TLM data and the scaled data set is at least 0.99. The sheet resistance was extracted with a Van der Pauw [100] measurement and had a value of 211Ω/sq., which corresponded to the sheet resistance extracted by the TLMs and the end resistance measurements. Therefore, the different measurement methods can be directly compared.

The results from the scaled data, illustrated in Table 7.2, show that the measured contact resistance was consistently lower than the simulation suggests. In case of the Berger [89] and Reeves [81] measurement method, it was found that the contact resistance results were not at all corresponding to the data of the scaled structure and the transfer length for these measurements were unrealistically high. This is due to an incorrect end resistance measurement when the specific contact resistivity is low [213]. As seen in previous design, the actual transfer length differs from the scaled data, which is more in the region of 200nm instead of 751nm. The actual transfer length is then extracted using the solver function in excel (2007), which is found by matching the simulated data for the smallest contact length to the measured data. The error of the ρ_c, R_{sk} and L_T values, in this case, is found using error propagation based on the standard deviation of the contact resistance value for the smallest contact and is therefore not a direct result from a measurement.

The actual transfer length was then found to be 188nm and this has consequences for the sheet resistance underneath the contact and the specific contact resistivity. The specific contact resistivity value drops to $3x10^{-7}\Omega.cm^2$ and the sheet resistance value increases to 856Ω/sq. The reduced specific contact resistivity indicates that the metal/semiconductor interface features a lower barrier height than previously indicated by the ordinary TLM measurement. The increased sheet resistance underneath the contact could be caused by either damage induced by the dry etch and metal deposition, reduced mobility of the material due to impurities at the surface compared to the Si_3N_4 passivated surface between the contacts and potentially the depletion layer under the metal could also contribute to an increased sheet resistance. In order to assess the damage induced by the dry etch a Van der Pauw measurement [100] of Si_3N_4 deposited and Si_3N_4 etched samples should be taken, which is addressed in the next sample.

	Ordinary TLM (Ω.mm)	R_e [81] (Ω.mm)	R_e [89] (Ω.mm)	Scaled TLM (Ω.mm)	R_{sk} adjusted (Ω.mm)
R_C (Ω.mm)	0.16 ± 0.006	0.16 ± 0.005	0.16 ± 0.004		0.16 ± 0.006
ρ_c ($\Omega.cm^2$)	$1.21x10^{-6}$ ± $8x10^{-8}$	$8.08x10^{-5}$ ± $5.0x10^{-6}$	$9.97x10^{-5}$ ± $4.5x10^{-5}$		$3.03x10^{-7}$ ± 1.10^{-7}
R_{sh} (Ω/sq)	214.43 ±1.79	213.47 ± 2.42	210.9 ± 1.19	253.48 ± 11.41	214.43 ±1.79
R_{sk} (Ω/sq)	214.43 ±1.79	3.18 ± 0.18	2.50 ± 0.50		856 ± 342
L_T (µm)	0.751 ± 0.029	50.5 ± 5	63.3 ± 4.0		0.188 ± 0.060

Table 7.2: Summary results of scaled ohmic contacts sample s10294

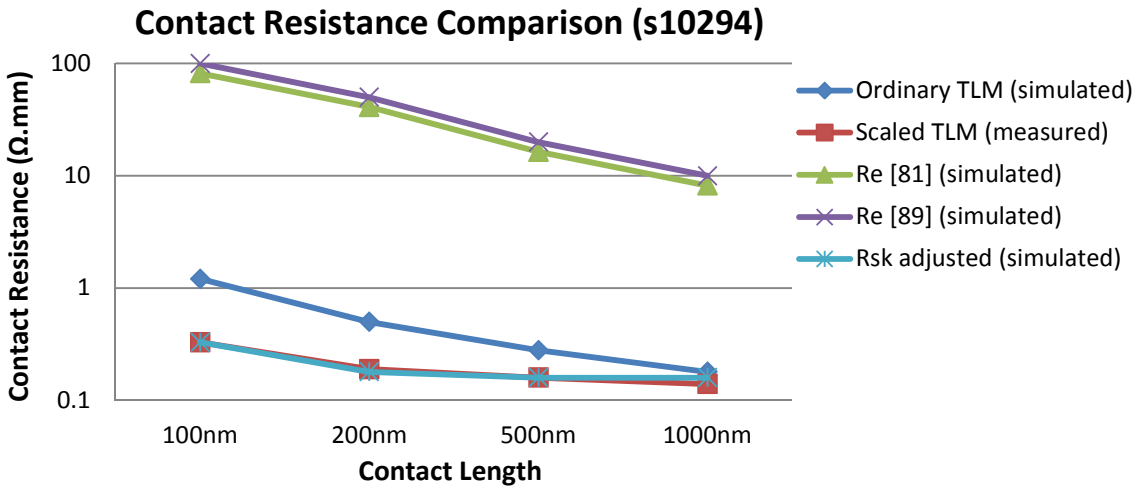


Figure 7.9: Contact resistance comparison between the simulated data of ordinary TLM and end resistance (Reeves and Berger) and measured scaled data on sample s10294.

7.4.2.2 Design 2b

The main objective of this sample is to compare the results from a CTLM measurement method to the scaled TLM measurements. The CTLM method is based on the TLM principle and should therefore, in theory, have similar results to the ordinary TLM

measurement. However, the CTLM method requires a correction factor because of the non linearity between measurements featuring different gap spacings. In most cases the results for R_C, R_{sh}, L_T and ρ_c are obtained by applying the correction factor to the measured total resistance values (R_T) for different gap spacings and then extrapolating the data. The value for R_{sh} is then found by the slope and the value of L_T is found by the intersection of the extrapolated data and the x-axis. The R_C and ρ_c are then calculated using R_{sh} and L_T and are given in Table 7.3. Also the R_T values have been recalculated and are compared to the original measured, which gives the correlation value.

There is an alternative method to extract the contact resistance proposed by Marlow and Das [214]. It is based on a circular centre contact with radius R_1, a gap spacing s and an infinitely large contact area. The equation for the total resistance is then shown in Equation 7.31 and includes the sheet resistance underneath the contact (R_{sk}) and the modified Bessel functions I_0, I_1, K_0 and K_1.

$$R_T = \frac{R_{sh}}{2\pi}\ln\left(\frac{R_1+s}{R_1}\right) + \frac{R_{sk}.L_T}{2\pi R_1}\frac{I_0\left(\frac{R_1}{L_T}\right)}{I_1\left(\frac{R_1}{L_T}\right)} + \frac{R_{sk}.L_T}{2\pi(R_1+s)}\frac{K_0\left(\frac{R_1}{L_T}\right)}{K_1\left(\frac{R_1}{L_T}\right)} \tag{7.31}$$

When R_1 and (R_1+s) are greater than L_T by a factor of at least four, the Bessel functions approximate unity [215] and become 1. The simplified Equation 7.32 can then be used to perform a least square fit to the experimental data. In this case, the fit is performed in Matlab using a "lsqcurvefit" function and the results are shown in Table 7.3 together with the original data. The results are then compared to the original data by calculating the correlation between the measured data and the recalculated R_T values based on the results from the least square fit.

$$R_T = \frac{R_{sh}}{2\pi}\left[\ln\left(\frac{R_1+s}{R_1}\right) + L_T\left(\left(\frac{1}{R_1}\right) + \left(\frac{1}{(R_1+s)}\right)\right)\right] \tag{7.32}$$

The R_C, R_{sh}, L_T and ρ_c values can also be directly calculated from the R_T values by reworking Equation 7.7 using two different measurements with respective gap spacings (s_a, s_b). Solving the equation for L_T gives:

$$L_T = \frac{\left(\left(\frac{\log\left(\frac{(R_1+s_a)}{R_1}\right)}{2\pi R_{Ta}}\right)-\left(\frac{\log\left(\frac{(R_1+s_b)}{R_1}\right)}{2\pi R_{Tb}}\right)\right)}{\left(\left(\frac{\left(\frac{1}{(R_1+s_a)}+\frac{1}{R_1}\right)}{2\pi R_{Ta}}\right)-\left(\frac{\left(\frac{1}{(R_1+s_b)}+\frac{1}{R_1}\right)}{2\pi R_{Tb}}\right)\right)} \quad (7.33)$$

And the sheet resistance can be found by:

$$R_{sh} = \frac{2\pi R_{Ta}}{\log\left(\frac{(R_1+s_a)}{R_1}\right)+\left(L_T\left(\left(\frac{1}{R_1}\right)+\left(\frac{1}{(R_1+s_a)}\right)\right)\right)} \quad (7.34)$$

The results of the direct calculation are included in Table 7.3 and to extrapolated data using excel LINEST function and a MATLAB least square curve fit. The difference between the extraction methods is minimal and stays within the standard deviation margin of the various extraction methods. The results of directly calculated extraction method feature the highest correlation compared to the measured data and are therefore retained as a comparison to the scaled and ordinary TLM method in Table 7.4.

CTLM gap	Extrapolated	Calculated	Matlab fitted
Correlation	99.998923%	99.998928%	99.998926%
R_C (Ω.mm)	0.103± 0.02	0.110 ± 0.02	0.108 ± 0.017
ρ_c (Ω.cm^2)	3.39x10^{-7} ± 1.15x10^{-7}	4.33x10^{-7} ± 1.39x10^{-7}	3.69x10^{-7} ± 1.12x10^{-7}
R_{sh} (Ω/sq)	320.01 ± 1.57	316.87 ± 1.42	319.70 ± 1.53
L_T (µm)	0.322 ± 0.068	0.369 ± 0.064	0.337 ± 0.053

Table 7.3: Summary CTLM results of sample s12829

The contact resistance value measured by CTLM is then compared to the result from the ordinary and scaled TLM, where the ordinary TLM without the isolation etch features the highest R_C value and the CTLM features the lowest R_C value. These two measurements also feature the lowest and highest sheet resistance values. The sheet resistance value with a Si_3N_4 layer has been measured using a Van der Pauw structure and was found to be 286Ω/sq. The further the sheet resistance deviates from this value, the more inaccurate the extraction for the R_C becomes. Therefore, the CTLM and non-isolation ordinary TLM are less reliable even though the standard deviation of the measurements is low. The reason of

the decreased sheet resistance for a non –isolated TLM is obvious: the current can travel with a wider path through the semiconductor material than the contact width due to lateral current spreading [92]. The increased sheet resistance for the CTLM measurement is probably due to differences in gap spacing or contact pad dimensions. The error caused by the differences in these dimensions is further amplified by the need for a correction factor (chapter 5.3.2.2). The correction factor includes the dimensions of both the gap spacing and the radius of the inner contact pad. Slight differences due to misalignment or overexposure of the resist then cause a bigger error compared to the ordinary TLM measurement.

Contact Length	Ordinary TLM No mesa	Ordinary TLM mesa	CTLM	Scaled TLM	TLM (1µm)	TLM corrected (1µm) (R_{sk})	TLM corrected (1µm) ($R_{sk}+R_m$)
R_C (Ω.mm)	0.268 ± 0.02	0.215 ± 0.02	0.111 ± 0.02		0.1829	0.1816	0.1815
ρ_c ($\Omega.cm^2$)	$3.30x10^{-6}$ ± $0.54x10^{-6}$	$1.56x10^{-6}$ ± $0.26x10^{-6}$	$4.33x10^{-7}$ ± $1.39x10^{-7}$		$1.32x10^{-6}$ ± $0.59x10^{-6}$	$3.14x10^{-7}$ ± $0.70x10^{-7}$	$3.42x10^{-7}$ ± $0.43x10^{-7}$
R_{sh} (Ω/sq)	218.75 ± 3.77	299.13 ± 4.66	316.87 ± 1.42	262.07 ± 11.41	260.91 ± 9.32	260.91 ± 9.32	260.91 ± 9.32
R_{sk} (Ω/sq)	218.75 ± 3.77	299.13 ± 4.66	316.88 ± 1.42		260.91 ± 9.32	1049.67 ± 191.86	1141.26 ± 282.77
L_T (µm)	1.230 ± 0.224	0.720 ± 0.060	0.370 ± 0.064		0.701 ± 0.157	0.173 ± 0.039	0.173 ± 0.039

Table 7.4: Summary results of scaled ohmic contacts sample s12829

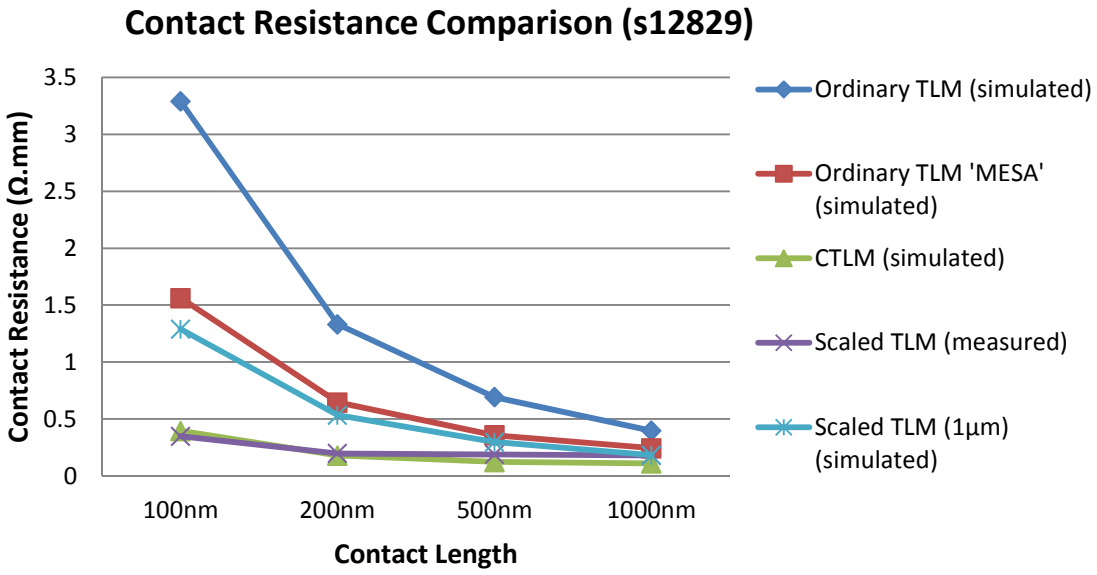


Figure 7.10: Contact resistance comparison between the simulated data of ordinary TLM, isolated ordinary TLM, and CTLM and measured scaled data on sample s12829

In order to investigate the current crowding effects, it was then decided to use the TLM results, however the contact resistance results differ slightly between the ordinary and scaled TLMs. It was chosen to use the results from 1µm scaled contact as any error in R_C will influence the extraction of the actual transfer length. As explained in previous sample, the transfer length was found by fitting the simulated data of a 100nm contact to the actual measured value of the 100nm contact. The actual transfer length was then found to be 173nm instead of the predicted ~700nm. This confirms the findings of the previous sample, where the actual transfer length was considerably shorter than the predicted transfer length by the ordinary TLM measurement even though the actual transfer length is in the range of 180nm for both samples. In order to investigate where the error can possibly come from, Hall measurements were taken to investigate the effect of depositing and etching Si_3N_4 on a n-type doped $In_{0.53}GaAs$ layer, as shown in Table 7.8. However the data recorded for the No Si_3N_4 sample proved to be unreliable for the carrier concentration and mobility measurement and have therefore been left out of Table 7.5.

	No Si_3N_4	Si_3N_4	Si_3N_4 etched
R_{sh} (Ω/sq)	451	286	588
Symmetry	1.13	1.17	1.12
p-n carrier concentration (cm^{-2})		$1.07x10^{13}$	$4.34x10^{12}$
μ (cm^2/Vs)		2050	2450

Table 7.5: Summary of hall measurement results of sample s12829

The sheet resistance decreases after Si_3N_4 deposition and increases beyond its original value after a Si_3N_4 etch, indicating that there is some degree of processing damage. Looking further into detail after a Si_3N_4 etch the mobility only slightly decreases and the carrier concentration reduces by a factor of 2.5. Previous research by S. Bentley on highly doped $In_{0.53}GaAs$ material has shown that a RIE SF6 dry etch causes a carrier reduction over etch time, as shown in Figure 7.11, which can potentially cause an increased sheet resistance underneath the contact. However, the sheet resistance of the Si_3N_4 etched sample (588Ω/sq) is then still significantly smaller than the predicted R_{sk} value of about 1kΩ/sq. The following reasons can potentially induce an increased sheet resistance underneath the contact: Additional processing damage, increased surface trap density and a large depletion region width compared to the active semiconductor layer thickness. Also, the measurement error due to changed scaled contact dimensions should be investigated.

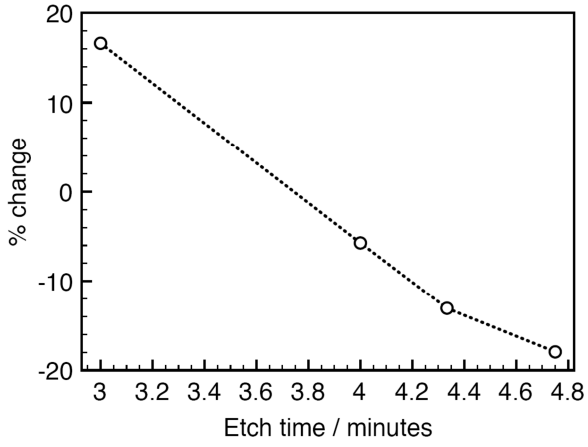


Figure 7.11: Percentage of carrier concentration variation over time for a RIE SF6 Si_3N_4 dry etch

Additional processing damage could be caused by the metal deposition technique used and will be hard to quantify. The damage could manifest itself as either out-diffusion of

semiconductor material or a reduced active layer thickness due to metal intrusion into the semiconductor layer, even when the sample is non alloyed. Both will result in a higher sheet resistance underneath the contact and could be investigated to a certain degree by using STEM and EELS. A grating structure with an area of 10 mm x10mm is required for sample preparation in order to use EELS and this structure was not present on the sample as the sample size is only 12mm x 12mm. Therefore, no STEM micrographs have been taken and no layer analysis using EELS was performed.

Increased surface trap density could be caused by lattice mismatches between the metal and the semiconductor leading to a reduced carrier concentration. Also metal induced gap states can cause a reduction of carrier concentration at the metal/semiconductor surface leading to increased sheet resistance near the interface. The reduction of carrier concentration underneath a metal layer is hard to quantify as a Hall measurement cannot be taken. The impact of metal deposition on the sheet resistance is therefore unknown, however the sheet resistance underneath the contact should be influenced by a smaller amount on thicker doped semiconductor layers. In this work the doped layer is 20nm and an increase in sheet resistance of 400% is observed while in the work by M. Lijadi et al. [209], the doped layer thickness is 100nm and only an increase in sheet resistance of 20% is observed. This implies that there is a possibility that the deposited metal causes an increase in sheet resistance, however this is an assumption and an extensive research with different layer thicknesses should be performed.

The depletion region underneath the metal may result in a lower carrier concentration and have a larger sheet resistance compared to the doped semiconductor region. On material with thin highly doped layers the depletion region could take up a significant thickness of the doped semiconductor layer. For example, the sample used has a 20nm $1x10^{19}cm^{-3}$ Si doped $In_{0.53}GaAs$ surface layer. The depletion width formed by a contact, assuming Bardeen's limit [203] for the built in potential, is 7nm. In the ideal theoretical case, this would mean that 35% of the total doped layer is a depletion region with reduced carrier concentration. Assuming the depletion region has an infinitely large sheet resistance compared to the bulk semiconductor sheet resistance this would mean the sheet resistance underneath the contact should become 904Ω/sq based on the bulk sheet resistance of the Si_3N_4 etched sample. This is close to the number obtained by the R_{sk} measurement, however this is a theoretical approach and in reality the depletion region is not equally distributed over the full depletion width. Therefore, this result should be compared to

different findings in literature: in the first case [209] the material used is p-type $3.5x10^{19}cm^{-3}$ $GaAs_{0.5}Sb_{0.5}$ with a layer thickness of 100nm. The calculated depletion region is 5nm compared to 100nm bulk semiconductor material. There should therefore, according to this theory, an increase of 5% in sheet resistance while there is a 20% increase in sheet resistance. In the second case [42], the top material is a 10nm $1x10^{19}cm^{-3}$ doped $Al_{0.25}Ga_{0.75}N$ layer, with a calculated depletion width of 16.9nm. This is a HEMT layer structure and therefore has extra doping in a 2DEG layer 3nm under the doped layer. Nonetheless the sheet resistance should be significantly large if the depletion region would cause the increase in sheet resistance. However, there is a 269% increase in sheet resistance, which is a similar number to that observed in this work. Therefore, it is unlikely that the depletion region contributes to an increased sheet resistance but it cannot be ruled out completely either. The effect could be investigated by making samples with various layer thicknesses, but could potentially be misinterpreted for damage induced by metal deposition.

As previously shown in section (7.2.1), the measurement error can be extracted for the sheet resistance underneath the contact for contacts with variable dimensions. As curve fitting is used, finding the measurement error for the extracted transfer length will be critical. Unfortunately, the transfer length is extracted by the measurement of scaled contacts, which have a non-linear relationship to contact resistance due to current crowding effects. The random error analysis can therefore not be used to extract the error of the transfer length when the contact length of the scaled contacts is variable. Therefore, the error of the transfer length is calculated using the standard deviation of the 100nm contact length and combining this with 10% variability in contact length. The variability of the contact width and gap size has not been taken into account in this case since these should play a minor role compared to the contact length variability. As a result, the relative error of the transfer length is then determined to be 32.65%, which can be used in Equation 7.30 giving a relative error for R_{sk} of 27.81%. The minimum R_{sk} value is then 757.73Ω/sq, which is still larger than the measured sheet resistance value of the etched Si_3N_4 sample. In order to achieve a value of 588Ω/sq, the extracted transfer length should have a relative error of at least 60%, which means the contact has to be 90% larger. Even though there will be a variability in contact length due to processing a relative error of 90% was not observed and the variability of a deposited metal measured top down with a SEM was around 2.5%. Therefore, it is concluded that there is an actual increase in sheet resistance

due to metal deposition. This is confirmed by multiple different samples with R_{sk} values, which are significantly higher than the R_{sh} value.

This sample features a similar sheet resistance underneath the contact as extracted by previous sample. Even though the relative error of the sheet resistance is quite large, there is a strong indication that the metal deposition introduces an increased sheet resistance underneath the contact. The most likely explanation for the increase in sheet resistance is potential intrusion of the metal into the semiconductor and a potential loss of carrier concentration due to increased surface states. This impedes the use of a TLM or CTLM structures as a correct measurement method to extract the specific contact resistivity and transfer length values. The CTLM structure also seems to be relatively more inaccurate compared to the TLM structure given the same processing. Misalignment and overexposure are therefore critical parameters when extracting the contact resistance with a CTLM measurement.

7.5 Conclusion

Two different designs were designed, fabricated and tested. The first design was dismissed due to large variability issues due to a mesa wet etch with inaccurate dimensions. Multiple samples were produced using the second design and featured lower transfer lengths than predicted by the TLM measurement. This means that the assumption that the sheet resistance below the contact is equal to the bulk sheet resistance is not valid. As a result, the specific contact resistivity and transfer length values extracted using an ordinary TLM or CTLM are inaccurate due to the approximations made in the model. Even though CBKR was not measured, it also uses the same model and will extract the specific contact resistivity and transfer length values with a similar inaccuracy. It is therefore critical to measure the sheet resistance underneath the contact in order to be able to predict the behaviour of the ohmic contact when the device is scaled following the ITRS node [1]. Also the metal sheet resistance could play a key role, however in this work the metal sheet resistance was very low compared to the sheet resistance and had little influence on the overall result.

8 Conclusion

As discussed in the introduction, the aim of this thesis was to develop a Au-free ohmic contact to a n-type III-V MOSFET, which could be integrated in a 200mm Si pilot line. A literature study was performed to find suitable candidates for Si processing compatible and low resistance source/drain ohmic contacts. From this study, it was apparent that the device architecture would determine the most suitable ohmic contact: an alloyed Ge based ohmic contact for low doping and low In concentration device material and a non-alloyed ohmic contact for highly doped ($>10^{19}cm^{-3}$) high In concentration device material using source/drain regrowth.

Both Pd/Ge and Ni/Ge based alloyed ohmic contacts have been investigated in this work. The Ni/Ge contact featured relatively high optimal annealing temperatures, which are in excess of the maximum annealing temperature of the GaGdO gate dielectric of 450°C. Therefore, the contact is less suitable for the MOSFET device structure with a GaGdO gate dielectric but could be further investigated on material with different gate dielectrics in the future. The optimal annealing temperature for a Pd/Ge ohmic contact was shown to be 360°C and 400°C depending on the annealing time and semiconductor material. More extensive research was then carried out on different substrates with different layer structures, which are described in the appendix: x238, x266, IM-GaAs, IM-InGaAs500 and IM-InGaAs20, which included a vertical scaling study. The study showed that the thickness of the overall contact can be scaled when a ratio of 10/25 of Pd/Ge is maintained. The performance of the ohmic contact is predominately determined by the bandgap and the doping of the semiconductor material underneath the contact metal. The specific contact resistivity ranges between $5x10^{-5}\Omega cm^2$ for x266 material to $1.58x10^{-6}\Omega cm^2$ for x238 material, which were measured using TLM structures. The specific contact resistivity value on the IM-InGaAs20 sample is relatively high compared to the results of the non-alloyed ohmic contacts on identical material. A chemical analysis revealed that Ge diffuses into the semiconductor material, which should improve the doping levels and consequently reduce the barrier width and specific contact resistivity. However, the specific contact resistivity is worse than the non-alloyed ohmic contacts and this is possibly due to an outdiffusion of Ga into the PdGe contact rendering this area p-type doped increasing the specific contact resistivity. The chemical analysis also revealed little alloying, between 5nm and 10nm, into the semiconductor material, which is an advantage over a NiGeAu contact. Therefore, the PdGe contact could potentially be used as a self-aligned ohmic contact but suffers from an

increased contact resistance compared to the NiGeAu contact as the semiconductor material in the channel material has a lower bandgap than the semiconductor material underneath the oxide, which is due to the buried channel layer structure. Removing the wider bandgap material prior to metal deposition could potentially improve the specific contact resistivity. An anisotropic dry etch is needed in order to prevent an undercut forming underneath the oxide. Two different anisotropic etches were used: a RIE etch technique and an ion gun etch technique. The RIE etch resulted in non-ohmic contact behaviour but the ion gun etch improved the specific contact resistivity by about one order of magnitude. The ion gun etch was performed after a wet etch of gate dielectric and therefore more research is needed in order to perform a dry etch only gate dielectric removal. The PdGe based ohmic contact can therefore be implemented in the current MOSFET device structures when a wet etch of the gate dielectric is used.

Future different MOSFET device structures featuring highly doped, narrow band source/drain regions will allow for non alloyed contact deposition as additional doping or band gap lowering is no longer required. Four different ohmic contact structures were deposited using e-beam evaporated metals with different work functions and one ohmic contact structure was deposited using sputtering. The e-beam evaporated metal structures were; Ti/Pt 10nm/80nm, Al 100nm, Ni, 100nm and Au 100nm and the sputtered metal structure was TiW 100nm. The best ohmic contacts were formed using the Au and Ti/Pt ohmic contact, which had a specific contact resistance in the region of $7.5x10^{-7}\Omega cm^2$. The Ni contact, which theoretically has a work function similar to Au had a specific contact resistivity, which was one order of magnitude higher than the Au contact and deteriorated on annealing in contradiction to the results found in literature. The poor results of the annealed Ni sample are probably due to migration of Ni, which led to a decreased semiconductor sheet resistance. The Al contact with the lowest theoretical work function featured the highest specific contact resistivity. Therefore, the influence of the work function of the metal is not conclusive and is therefore probably not the crucial factor, which determines the quality of the ohmic contact on highly doped $In_{0.53}GaAs$.

The results of the sputtered contacts were subject to the quality of the metal etch and before any conclusive results can be drawn, the metal etch should be optimised. However, the contacts showed promising specific contact resistivity values and the sputtered contacts should be considered in future work.

Also devices were built on two different types of III-V MOSFET device structures: a buried channel flatband device structure and a surface channel device structure. The buried channel flatband MOSFET device structure featuring a GaGdO gate dielectric was used in a study to determine whether the devices could be scaled along both the gate length and source/drain separation. The surface channel device structure was used to investigate the benefits of lower bandgap material in the channel combined with a PdGe ohmic contact structure and a different gate dielectric using Al_2O_3.

In order to build ohmic contacts to the source/drain scaled devices, the gate dielectric needed to be removed using a dry etch and therefore a NiGeAu contact is used in this study. From this study a number of conclusions can be drawn. First, the utilization of a gate dielectric and device architecture with known low interface state density is vital when exploring device scaling issues, in particular where off-state performance metrics such as sub-threshold swing are important. The 1 µm source/gate separation devices show that the flatband mode architecture appears to be robust to scaling at least to 90nm, with the layer design and doping strategy adopted in this work. In addition, whilst the more aggressively scaled 180nm devices have encouraging off-state performance, on-state breakdown is a significant issue, which will have to be mitigated by device re-engineering, with particular emphasis on minimising the lateral diffusion of the ohmic contacts. The 90nm aggressively scaled devices appear to be suffering significantly from this issue and in the most extreme case, to the extent that the devices cannot be turned off. In future work these drawbacks can be mitigated when a dry etch compatible with a PdGe contact structure can be realised.

The surface-channel MOSFET device architecture, which can potentially be integrated on a 200mm Si platform, has shown promising mobility values with corresponding high carrier concentrations. Well behaved surface channel MOSFET devices were made with both NiGeAu and Pd/Ge/Ti/Pt based ohmic contacts. The performance of the Pd/Ge/Ti/Pt contacts is low compared to the NiGeAu but can be improved after optimisation of various parameters such as annealing temperature, oxide etch and the ratio of Pd/Ge layer thickness, however the stringent ITRS requirements are unlikely to be met and alternative contact strategies such as regrowth should be considered. The Al_2O_3 gate stack also requires an improvement to challenge the GaO/GaGdO gate dielectric stack in terms of leakage and density of states. Future work should focus on reducing ohmic contact resistance and improving the Al_2O_3 gate dielectric stack.

The research described above was performed with contact dimensions well above the transfer length. However, the ohmic contacts have to be integrated in a scaled CMOS technology and therefore two different TLM-based designs with contact lengths scaled below the transfer length were designed, fabricated and tested. Once the contacts are scaled below two times the transfer length, current crowding effects start to dominate. The use of the scaled contact measurement method proved to have several advantages: the sheet resistance underneath the contact can be extracted and therefore the contact resistance can be calculated more accurately when ohmic contact regions are scaled even further. The results were then compared to the measurement results from TLM, CTLM and the end resistance measurement method.

The first design was dismissed due to large variability issues due to a mesa wet etch with inaccurate dimensions. Multiple samples were produced using the second design and featured lower transfer lengths than predicted by the TLM measurement. This means that the assumption that the sheet resistance below the contact is equal to the bulk sheet resistance is not valid. There is a strong indication that the metal deposition introduces an increased sheet resistance underneath the contact. The most likely explanation for the increase in sheet resistance is potential intrusion of the metal into the semiconductor and a potential loss of carrier concentration due to increased surface states. This impedes the use of a TLM or CTLM structures as a correct measurement method to extract the specific contact resistivity and transfer length values. The end resistance measurement was found to have great measurement errors when the specific contact resistivity is low and therefore cannot be used to extract the sheet resistance underneath the contact. The CTLM structure also seems to be relatively inaccurate compared to the TLM structure given the same processing. Misalignment and overexposure are therefore critical parameters when extracting the contact resistance with a CTLM measurement.

It is therefore critical to measure the sheet resistance underneath the contact in order to be able to predict the behaviour of the ohmic contact, when the device is scaled following the ITRS node [1]. Also, the metal sheet resistance could play a key role, however in this work the metal sheet resistance was very low compared to the sheet resistance and had little influence on the overall result. The increase in sheet resistance underneath the contact changes could not be explained conclusively in this work and should therefore be the main focus in future work.

The future work would then involve the measurement of ohmic contacts on materials with a different active layer thickness. The increase in sheet resistance underneath the contact could then be explained by comparing the experimental results to the results from a 1D Poisson-Schrodinger solver which takes the depletion region underneath the contact into account. Also TEM and EELs analysis could more accurately determine the layer thickness of the active material which can be fed back into the solver.

The future work to develop a Si processing compatible ohmic contact has two possible fields of research. One field is the development of nickelide contacts to high Indium concentration InGaAs or InAs. Nickelide ohmic contact feature relatively high contact resistances on $In_{0.53}GaAs$ however moving to high indium concentrations could potentially result in very low specific contact resistivities in the range required by the ITRS standards. Also the addition of Ge to nickelide recipe could be explored to increase the doping in a surface channel device. The other field is to move away from tradiditional planar MOSFET devices to FinFETs. The wet etch required to etch the fin structures would mean that the structure of the device can be changed as there will no longer be an oxide layer grown on top of the layer structure. This would allow a HEMT like quantum well structure with a recessed gate, which features highly doped, high indium concentration source/drain ohmic contact areas. In situ deposition of metals, such as Mo and TiW, has already shown that the requirements for the ITRS can be met and this deposition technique should therefore be considered in future work.

9 Appendices

9.1 References

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9.2 Fabrication processes

9.2.1 Standard clean

- Clean sample 5 minutes Acetone in ultrasonic bath
- Clean sample 5 minutes IPA in ultrasonic bath
- Clean sample 2 minutes H_2O

9.2.2 Standard TLM (metal layer thickness > 150nm)

- Standard clean
- Spin 12% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0001 belle file
    - Dose 450
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect

- Ash sample
    - New asher 1 minute, 40 Watt
- Wet etch 1:100 HCl:H_2O duration dependant of material
- Metallisation
- Lift off after 1h in 50°C Acetone
- Annealing
- 50nm Si_3N_4 deposition
- Measurement on probe station

9.2.3 Standard TLM (metal layer thickness < 150nm)

- Standard clean
- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0002 belle file
    - Dose 330
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 45s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Wet etch 1:100 HCl:H_2O duration dependant of material
- Metallisation
- Lift off after 1h in 50°C Acetone
- Annealing
- 50nm Si_3N_4 deposition
- Measurement on probe station

9.2.4 Sputtered metal TLM

- Standard clean
- Wet etch 1:100 HCl:H_2O duration dependant of material

- Metallisation
- Spin 12% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0003 belle file
    - Dose 450
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- 1h post bake 180°C
- Dry etch
- 1h in 50°C Acetone
- Annealing
- 50nm Si_3N_4 deposition
- Measurement on probe station

9.2.5 6-1073 MOSFET device

- Standard clean
- Spin 12% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - RHI0088 belle file
    - Dose dependent on feature size
- Develop sample
    - 1:2 developer 60s at 23°C

    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - Old asher 2 minutes, 110 Watt
- Metallisation Au/Ge/Au/Ge/Au/Ni/Au (10/10/10/10/20/11/80nm)
- Lift off after 1h in 50°C Acetone
- IPA clean
- Standard clean
- Spin 12% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - RHI0089 belle file
    - Dose dependent on feature size
- Develop sample
    - 1:2 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - Old asher 2 minutes, 110 Watt
- Metallisation Au/Ge/Au/Ge/Au/Ni/Au (10/10/10/10/20/11/80nm)
- Lift off after 1h in 50°C Acetone
- IPA clean
- Standard clean
- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - RHI0090 belle file
    - Dose dependent on feature size
- Develop sample
    - 1:2,5 developer 45s at 23°C

  - IPA 30s
  - Blow dry + inspect
- Ash sample
  - Old asher 2 minutes, 110 Watt
- Wet etch HCl:H_2O 1:100 (15s-30s depending on oxide thickness) + 30s water rinse
- Metallisation 20nm Pt + 200nm Au
- Lift off after 1h in 50°C Acetone
- Annealing 400°C 10s
- 50nm Si_3N_4 deposition
- Measurement on probe station

9.2.6 c707 MOSFET device

- Standard clean
- Spin 12% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
  - SB7001 belle file
  - Dose dependent on feature size
- Develop sample
  - 1:2.5 developer 30s at 23°C
  - IPA 30s
  - Blow dry + inspect
- Ash sample
  - Old asher 2 minutes, 110 Watt
- Metallisation 20nm Pt + 200nm Au
- Lift off after 1h in 50°C Acetone
- IPA clean
- Standard clean
- Spin 12% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven

- VB6 patterning
    - SB7003 belle file
    - Dose dependent on feature size
- Develop sample
    - 1:1 developer 30s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Wet etch AZ400k 2m45s + 30s water rinse
- Metallisation 10nm Pd 25nm Ge 35nm Ti 35nm Pt
- Lift off after 1h in 50°C Acetone
- Annealing 400°C 10s
- 50nm Si_3N_4 deposition
- Measurement on probe station

9.2.7 Scaled design (1)

- Standard clean

Markers:

- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0100 belle file
    - Dose 330
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Metallisation 100nm Au

- Lift off after 1h in 50°C Acetone
- IPA clean

Mesa etch:

- Standard clean
- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning (Markers)
    - WOJ0101 belle file
    - Dose 330
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Wet etch
    - 1:4 HCl:H_2O 30s
    - 1:1:100 H_2O_2:Orthophosphoric Acid:H_2O 45s
    - H_2O rinse 60s
- Strip PMMA 1h in 50°C Acetone
- IPA clean

High resolution Contacts:

- Standard clean
- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 2.5% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0102 belle file
    - Dose dependant of feature size
- Develop sample

    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Metallisation
- Lift off after 1h in 50°C Acetone
- IPA clean

Contact Pads:

- Standard clean
- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0103 belle file
    - Dose 330
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Metallisation
- Lift off after 1h in 50°C Acetone
- IPA clean

Probe station TLM measurement

9.2.8 Scaled design (2)

- Standard clean

Markers:

- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0200 belle file
    - Dose 330
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Metallisation 100nm Au
- Lift off after 1h in 50°C Acetone
- IPA clean

Isolation etch:

- Standard clean
- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning (Markers)
    - WOJ0201 belle file
    - Dose 330
    - Beam current 64nA
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s

    - Blow dry + inspect
- Ash sample
    - New asher 1 minute, 40 Watt
- Wet etch
    - 1:4 HCl:H_2O 30s
    - 1:1:100 H_2O_2:Orthophosphoric Acid:H_2O 45s
    - H_2O rinse 60s
- Strip PMMA 1h in 50°C Acetone
- IPA clean + H_2O clean 2 min
- Ash sample
    - New asher 1 minute, 40 Watt
- Standard clean
- 30nm Si_3N_4 deposition

High resolution Contacts:

- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning
    - WOJ0202 belle file
    - Dose dependant of feature size
- Develop sample
    - 1:2.5 developer 60s at 23°C
    - IPA 30s
    - Blow dry + inspect
- Dry etch Si_3N_4
- PMMA strip 1h in 50°C Acetone
- IPA clean

Contact Pads:

- Spin 8% 2010 at 5000rpm. (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- Spin 4% 2041 at 5000rpm (Recipe 2 spinner)
- 1 hour bake in 180°C oven
- VB6 patterning

  - WOJ0203 belle file
  - Dose 330
  - Beam current 64nA
- Develop sample
  - 1:2.5 developer 60s at 23°C
  - IPA 30s
  - Blow dry + inspect
- Ash sample
  - New asher 1 minute, 40 Watt
- Metallisation
- Lift off after 1h in 50°C Acetone
- IPA clean

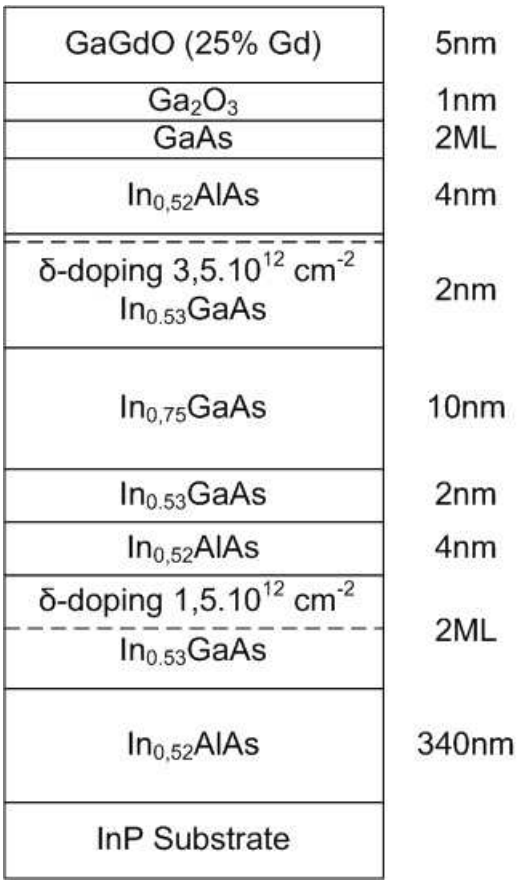
Probe station TLM measurement

9.3 List of materials

9.3.1 University of Glasgow grown material

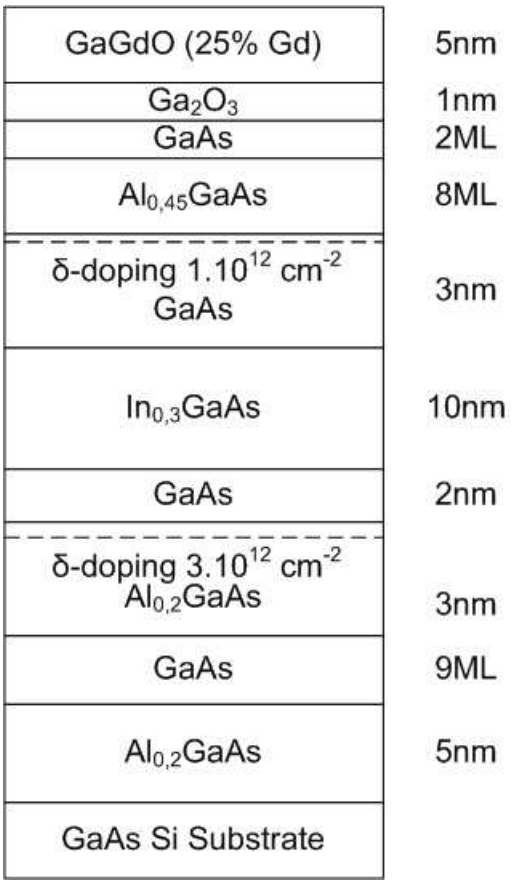
9.3.1.1 x238

- Buried channel architecture
- Increased In content in channel
- Layer structure:



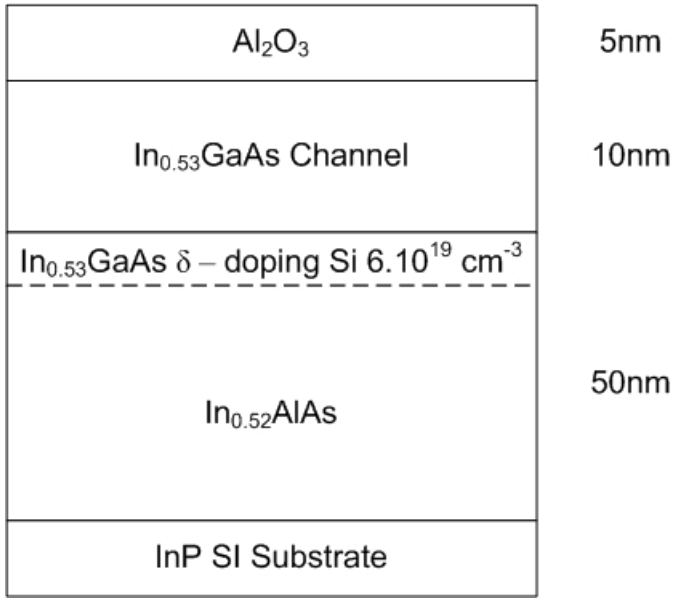
9.3.1.2 x266, x319

- Buried channel architecture
- Reduced GaGdO gate dielectric
- Layer structure:



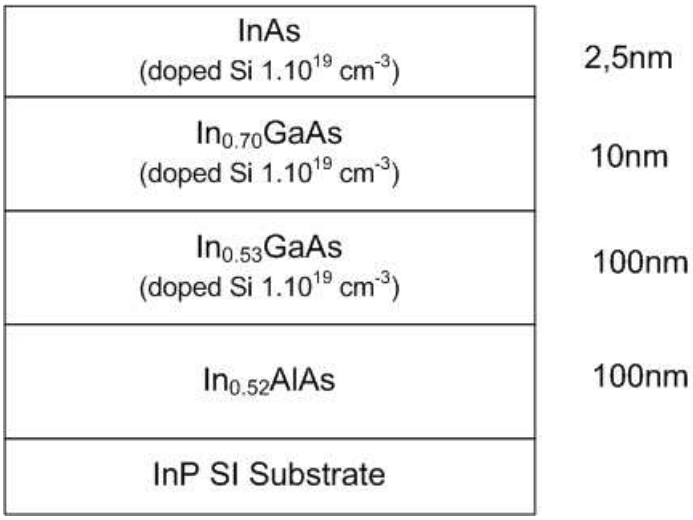
9.3.1.3 c707, c764

- Surface channel architecture
- Al_2O_3 gate dielectric
- Layer structure:



9.3.1.4 c760,c783

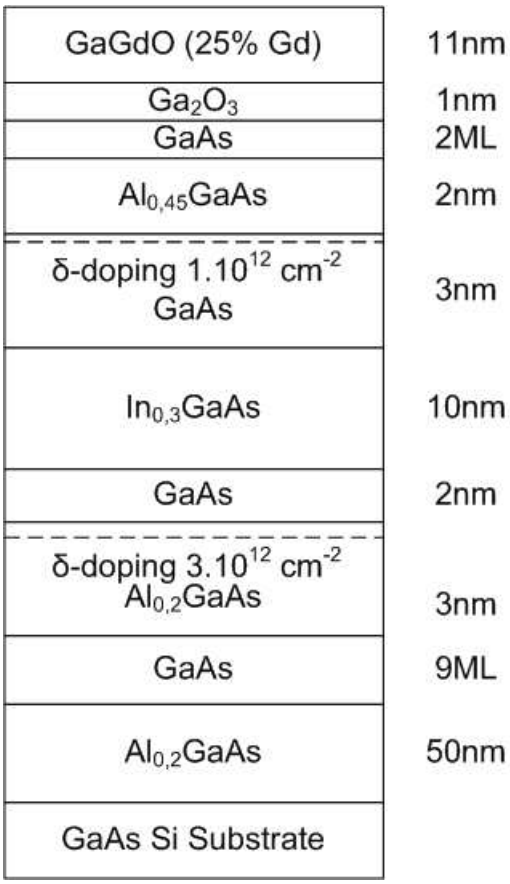
- Thin InAs surface layer
- Layer structure



9.3.2 Freescale grown material

9.3.2.1 6-1073

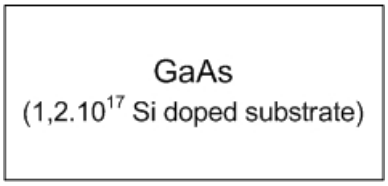
- Layer structure:



9.3.3 IMEC grown material

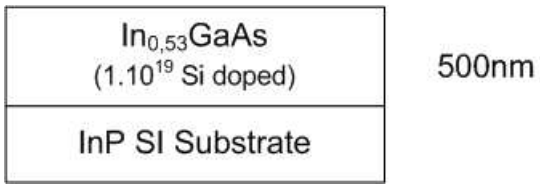
9.3.3.1 IM-GaAs:

- Low R_{sh} value
- Layer structure:



9.3.3.2 IM-InGaAs500:

- Low R_{sh} value
- Layer structure:



9.3.3.3 IM-InGaAs20:

- Barrier layer: 20nm undoped $In_{0.52}AlAs$
- Isolation possible
- R_{sh} around 300 $\Omega.cm^2$ with Si_3N_4 passivation
- Layer structure: