Ultra-Thin Silicon Technology for Tactile Sensors

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Abstract

In order to meet the requirements of high performance flexible electronics in fast growing portable consumer electronics, robotics and new fields such as Internet of Things (IoT), new techniques such as electronics based on nanostructures, molecular electronics and quantum electronics have emerged recently. The importance given to the silicon chips with thickness below 50 μm is particularly interesting as this will advance the 3D IC technology as well as open new directions for high-performance flexible electronics. This doctoral thesis focusses on the development of silicon–based ultra-thin chip (UTC) for the next generation flexible electronics. UTCs, on one hand can provide processing speed at par with state-of-the-art CMOS technology, and on the other provide the mechanical flexibility to allow smooth integration on flexible substrates. These development form the motivation behind the work presented in this thesis.

As the thickness of any silicon piece decreases, the flexural rigidity decreases. The flexural rigidity is defined as the force couple required to bend a non-rigid structure to a unit curvature, and therefore the flexibility increases. The new approach presented in this thesis for achieving thin silicon exploits existing and well-established silicon infrastructure, process, and design modules. The thin chips of thicknesses ranging between 15 μm – 30 μm, were obtained from processed bulk wafer using anisotropic chemical etching. The thesis also presents thin wafer transfer using two-step transfer printing approach, packaging by lamination or encapsulation between two flexible layerand methods to get the electrical connections out of the chip. The devices realised on the wafer as part of front-end processing, consisted capacitors and transistors, have been tested to analyse the effect of bending on the electrical characteristics. The capacitance of metal-oxide-semiconductor (MOS) capacitors increases by ~5% during bending and similar shift is observed in flatband and threshold voltages. Similarly, the carrier mobility in the channel region of metal-oxide-semiconductor field effect transistor (MOSFET) increases by 9% in tensile bending and decreases by ~5% in compressive bending. The analytical model developed to capture the effect of banding on device performance showed close matching with the experimental results.

In order to employ these devices as tactile sensors, two types of piezoelectric materials are investigated, and used in extended gate configuration with the MOSFET. Firstly, a nanocomposite of Poly(vinylidene fluoride-co-trifluoroethylene), P(VDF-TrFE) and barium titanate (BT) was developed. The composite, due to opposite piezo and pyroelectric coefficients of constituents, was able to suppress the sensitivity towards temperature when

force and temperature varied together, The sensitivity to force in extended gate configuration was measured to be 630 mV/N, and sensitivity to temperature was 6.57 mV/^{o}C, when it was varied during force application.

The process optimisation for sputtering piezoelectric Aluminium Nitride (AlN) was also carried out with many parametric variation. AlN does not require poling to exhibit piezoelectricity and therefore offers an attractive alternative for the piezoelectric layer used in devices such as POSFET (where piezoelectric material is directly deposited over the gate area of MOSFET). The optimised process gave highly orientated columnar structure AlN with piezoelectric coefficient of 5.9 pC/N and when connected in extended gate configuration, a sensitivity (normalised change in drain current per unit force) of 2.65 N^{-1} was obtained.

List of Publication

The work presented in this thesis has culminated in the following journal publications and conference proceedings:

Journal Articles (published)

1) **S. Gupta**, W. T. Navaraj, L. Lorenzelli, and R. Dahiya, "Ultra-thin chips for high-performance flexible electronics," *Nature Flexible Electronics*, vol. 2, p. 8, 2018.

2) **S. Gupta**, D. Shakthivel, L. Lorenzelli, R. Dahiya "Temperature Compensated Tactile Sensing using MOSFET with P(VDF-TrFE)/$BaTiO_3$ Capacitor as Extended Gate" *IEEE Sensor J*ournal, vol.9, issue.2, pp. 435-442, 2018.

3) W. T. Navaraj, **S. Gupta**, L. Lorenzelli, and R. Dahiya, "Wafer Scale Transfer of Ultrathin Silicon Chips on Flexible Substrates for High Performance Bendable Systems" *Advanced Electronic Materials*, vol. 4, issue.4, pp. 1700277, 2018.

4) N. Yogeswaran, W. T. Navaraj, **S. Gupta**, F. Liu, V. Vinciguerra, L. Lorenzelli, and R. Dahiya, "Piezoelectric Graphene Field Effect Transistor Pressure Sensors for Tactile Sensing," *Applied Physics Letters*, 2018.

5) A.Vilouras, H. Heidari, **S.Gupta**, R. Dahiya "Modelling of CMOS Devices and Circuits on Flexible Ultra-Thin Chips" *IEEE Transactions on Electronic Devices* , vol.64, pp: 2038 - 2046, 2017.

6) **S. Gupta**, H. Heidari, L. Lorenzelli, R. Dahiya, "Device modelling for bendable piezoelectric FET-based touch sensing system" *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, pp: 2200-2208, 2016.

7) N. Yogeswaran, W. Dang, W. T. Navaraj, D. Shakthivel, S. Khan, E. O. Polat, **S. Gupta**, H. Heidari, M. Kaboli,L. Lorenzelli, G. Cheng, and R. Dahiya, "New

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8) **S. Gupta**, N. Yogeswaran, R. Dahiya “Fabrication of c-axis Oriented Aluminium Nitride Films by RF Magnetron Sputtering for Tactile Sensing”

9) A. Vilouras, **S. Gupta**, R. Dahiya “Flexible Ion-Sensitive Field-Effect Transistors on Ultra-Thin Chips”

10) **S. Gupta**, A.Vilouras, and R. Dahiya “Polydimethylsiloxane as polymeric protective coating for anisotropic silicon etching”

Conferences Papers

1) **S. Gupta**, N. Yogeswaran, F.Giacomozzi, , L. Lorenzelli and R. Dahiya, "Flexible AlN coupled MOSFET Device for Touch Sensing," *IEEE Sensors 2018*, New Delhi, India.

2) N. Yogeswaran, **S. Gupta**, and R. Dahiya, “Low Voltage Graphene FET Based Touch Sensor” *IEEE Sensors 2018*, New Delhi, India.

3) A. Paul, **S. Gupta**, and R. Dahiya, “Corrugated Graphene Network based Pressure Sensor” *IEEE Sensors 2018*, New Delhi, India, 2018.

4) **S. Gupta**, L. Lorenzelli, and R. Dahiya, "Multifunctional flexible P(VDF-TrFE)/$BaTiO_3$ based tactile sensor for touch and temperature monitoring," *IEEE Sensors 2017*, Glasgow, UK.

5) **S.Gupta**, A.Vilouras, H.Heidari, R.Dahiya “Device Modelling of Silicon based High Performance Flexible Electronic” *IEEE ISIE 2017*, Edinburgh, UK.

6) **S. Gupta**, F. Giacomozzi, H. Heidari, L. Lorenzelli, and R. Dahiya, "Ultra-Thin Silicon based Piezoelectric Capacitive Tactile Sensor," *EuroSensors 2016,* Budapest, Hungary.

7) **S. Gupta**, H. Heidari, L.Lorenzelli, R.Dahiya "Towards Bendable Piezoelectric Oxide Semiconductor Field Effect Transistor based Touch Sensor", *IEEE ISCAS 2016,* Montreal, Canada.

Poster Presentations

1) **S. Gupta**, F.Giacomozzi, L.Lorenzelli, R.Dahiya "Towards Fabrication of Ultra-Thin Piezoelectric capacitor For Tactile Sensing" *Terzo Convegno Nazionale Sensori (CNS) 2016,* Rome, Italy.

2) **S. Gupta**, H.Heidari, L.Lorenzelli, R.Dahiya, "Analytical Modelling of Piezoelectric Oxide Semiconductor Field Effect Transistor" *innoLAE 2016,* Cambridge, UK.

3) H.Heidari**, S. Gupta**, W.T.Navaraj, L.Lorenzelli, R.Dahiya "Simulation Scenarios for Ultra-Thin Chips in Smart Large-Area Flexible Electronics", *innoLAE 2016,* Cambridge, UK.

4) **S. Gupta**, L.Lorenzelli, R.Dahiya, "Device Modelling of Piezoelectric Oxide Semiconductor Field Effect Transistor" *NanotechItaly 2015,* Bologna, Italy.

Book

A. Paul, **S. Gupta**, R. Dahiya, *Solid-State Sensors (in progress)*
Publisher: IEEE+ Wiley

कर्मण्येवाधिकारस्ते मा फलेषु कदाचन।
मा कर्मफलहेतुर्भूर्मा ते सङ्गोऽस्त्वकर्मणि॥

\- *Bhagavad Gita 2-47*

Karmanye vadhikaraste Ma Phaleshu Kadachana
Ma Karmaphalaheturbhurma Te Sangostvakarmani

"You are entitled to do your duty and action, but never to the results of your actions. Let not the results be your motivation, and do not be attached to laziness and inaction."

This dissertation is lovingly dedicated to my mother, Mrs. Sandhya Gupta. Her support, encouragement, and constant love have sustained me throughout my life.

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Author's Declaration

I, Shoubhik Gupta, hereby declare that except where explicitly reference is made to the contribution of others, this thesis is the result of the work of the named and has not been submitted for any other degree at the University of Glasgow or any other institution.

In particular, William Ringal Taube Navaraj and Anastasios Vilouras have been involved in characterisation of thin silicon based devices and implementation of Verilog-A code in Cadence, respectively.

Definitions/Abbreviations

2D	2 Dimensional
3D	3 Dimensional
AFM	Atomic Force Microscopy
AlN	Aluminium Nitride
APS	Active Pixel Sensor
BAW	Bulk Acoustic Wave
BT/BaTiO3	Barium Titanate
C_4F_8	Octafluorocyclobutane
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance-Voltage
CVD	Chemical Vapour Deposition
DBG	Dicing Before Grinding
DC	Direct Current
DI	De-Ionised
DRC	Design Rule Check
DRIE	Deep Reactive Ion Etching
FOX	Field Oxide
FTIR	Fourier-Transform Infrared Spectroscopy
HF	Hydrofluoric acid
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IoE	Internet of Everything
IoT	Internet of Things
IPA	Isopropyl alcohol
KOH	Potassium Hydroxide
LCP	Liquid Crystal Polymer
LED	Light Emitting Diode
LPCVD	Low Pressure Chemical Vapour Deposition
MEMS	Microelectromechanical System
MEOL	Middle End Of Line

MIM	Metal Insulator Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OFET	Organic Field Effect Transistor
P(VDF-TrFE)	Poly(vinylidene fluoride-co-trifluoroethylene)
PDMS	Polydimethylsiloxane
PECVD	Plasma Enhanced Chemical Vapour Deposition
PET	Polyethylene Terephthalate
PI	Polyimide
POSFET	Piezoelectric Oxide Semiconductor Field Effect Transistor
PVA	Polyvinyl Alcohol
PVC	Polyvinyl Chloride
PZT	Lead Zirconate Titanate
RF	Radio Frequency
rpm	Rotation per minute
sccm	standard cubic centimetres per minute
SEM	Scanning Electron Microscope
SF_6	Sulphur hexafluoride
Si	Silicon
Si_3N_4	Silicon Nitride
SiO_2	Silicon dioxide
SoC	Silicon on Carbide
SOI	Silicon Over Insulator
TBAF	Tetra Butyl Ammonium Fluoride
TEOS	Tetraethyl Orthosilicate
TMAH	Tetramethylammonium hydroxide
UTC	Ultra-Thin Chip
UTSi	Ultra-Thin Silicon
UV	Ultra Violet
VTC	Voltage Transfer \Characteristics
XRD	X-Ray Diffractometer
ZnO	Zinc Oxide

Chapter 1. Introduction

1.1 Background and motivation

The ever-increasing consumer demand for more powerful and multifunctional portable devices has driven the ultra-fast technology growth in electronics that we observe nowadays. Flexible electronics, as the emerging technology, has shifted the paradigm in electronics due to its wide range of applications, such as healthcare monitoring, display, energy harvesting, e-skin for robotics and prosthesis, consumer electronics and telecommunications [1]. It also provides a pathway for multi-layer integration of electronics, which is termed as 3D stacked electronics[2]. Current technologies for flexible electronics are mainly focused on organic electronics, which is limited by low-performance when compared to high-performance silicon-based CMOS technology[3]. However, the standard CMOS process is developed around rigid silicon wafer, which tends to fracture during any bending. To resolve this issue and realise the silicon-based flexible electronics, the development of silicon thinning technology is essential. As such, when silicon is thinned up to the ultra-thin regime (<50 μm), it becomes bendable and can conform to curvilinear surfaces. Such motivation has also been highlighted by the ITRS, which stated the need for thin chips almost 15 years ago in context with 3D IC staking for system-in-package. The ITRS report in 2005 has also emphasised on UTCs which are thinner than 20 μm including the wafer thinning and handling, small and thin die assembly and packaging of thin chips technologies. Until a few years ago the demand for UTCs was primarily for 3D system integration, where multiple active silicon dies having active and lateral interconnects are vertically connected through silicon vias. However, with emerging applications such as m-Health, wearable systems, smart cities, and IoT, the high-performance and flexibility requirements for electronics are primarily pushing the interest in UTCs and making it move ahead from just 3D ICs.

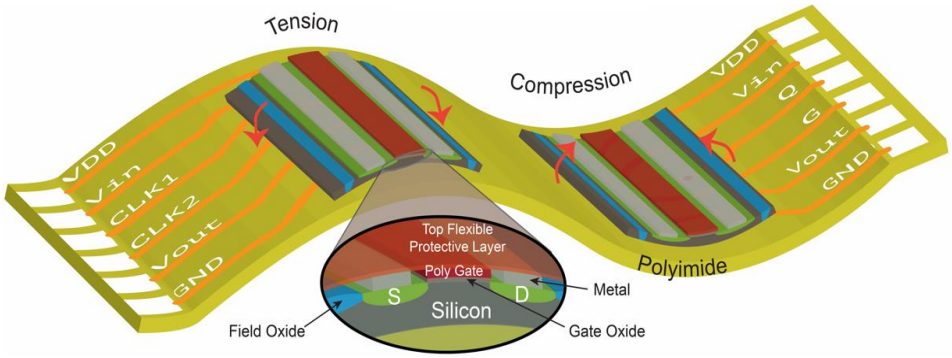


Figure 1.1: Illustration of seamless integration of thin chip over the flexible substrate.

In this direction, Prof. Rogers group at NorthWestern University, USA works on thin silicon ribbon and island structure, derived from SOI wafer with a view of stretchability in the envisaged system[4]. Prof. Hussain group at King Abdullah University of Science and Technology, Saudi Arabia, also explore thin silicon at large scale using innovative dry etching techniques[5]. On the industrial side, IMEC and IMS Chips are investigating thin silicon for sensor application and, ABB and Infineon are interested in using thin semiconductor for better power device applications. With a range of work being carried out across industry and academia for exploring thin silicon as next platform for flexible electronics, the objective of this thesis is to develop the process and strategies to effectively fabricate mechanically bendable devices and sensors, which could empower electronic systems for a variety of novel applications. The goal is directed towards fabricating bendable tactile sensors that use the piezoelectric material as a transducer layer in combination with MOSFET. Thus, three main elements make up this work. Firstly, process design, mask layout, and fabrication of chips consisting MOSFETs and test structure were carried out. Secondly, two types of piezoelectric materials (nanocomposite of P(VDF-TrFE)/BT and AlN) were developed to address the issues associated with P(VDF-TrFE) i.e. unwanted sensitivity to temperature and requirement of poling. Thirdly, post-processing methods were developed to transform the silicon from rigid to bendable regime and models were developed to capture the effect of bending on device performance.

1.2 Objectives of the Ph.D. research

The primary objectives of this thesis are:

- To design the process and simulate key steps, mask layout, and fabricate the MOSFETs and test structures.

- To investigate other piezoelectric materials for resolving the challenges associated with P(VDF-TrFE).

- To develop the process and optimisation techniques for thinning silicon to sub-50 μm regime.

- To package the thinned chips and model the effect of mechanical bending stress on device performance.

- To characterise the devices and sensing structures for tactile sensing applications.

1.3 Structure of the thesis

This thesis is arranged in 8 chapters, which are summarised here as follows:

Chapter 2 introduces the state-of-the-art of ultra-thin silicon. The chapter discusses the market share of thin wafers, its growth and future opportunities arising in this field. In particular, more discussion concerns the post-processing techniques, and their evaluation. The new research avenues which need more attention in the area of ultra-thin wafer such as thin wafer handling and dicing are also discussed. A brief discussion on the applications of the ultra-thin chips and how they are pushing the advancements concludes the chapter.

Chapter 3 presents the process design, layout and process steps carried out to fabricate transistors and test structures. The fabrication run consisted 135 steps and the chapter includes 55 key steps. The illustration showcasing the cross-sectional view of device after every lithography and optical images captured after some important steps are also included. The fabricated devices were used as active devices for tactile sensing.

Chapter 4 discusses the work done for investigating the piezoelectric materials that has to be used as transducer layer for tactile sensing devices. It presents the development of two different class of piezoelectric materials, first one is nanocomposite of P(VDF-TrFE) and BT, and second one is thin film of AlN. The nanocomposite shows suppression of sensitivity towards

temperature due to opposite piezo and pyroelectric properties of the constituents. The thin film of AlN deposited by RF magnetron sputtering, possesses piezoelectric properties without any poling, making it a good candidate, when it comes to direct deposition on the gate area of MOSFET. The chapter also includes a range of tests, such as EDX, SEM, AFM, Raman, and FTIR to evaluate the material properties.

Chapter 5 presents the post-processing steps followed to thin the silicon from bulk state to ultra-thin regime. The anisotropic wet etching with Tetra methyl ammonium hydroxide (TMAH) was chosen as the method to remove the substrate from backside, due to the etchant IC compatibility. The chapter also presents the chip separation technique, encapsulation and transfer of thinned sample on flexible substrate. Some preliminary work done using dry etching and grinding are also included towards the end of chapter.

Chapter 6 presents the development of analytical models to study the effect of mechanical bending on device performance and its implementation in Verilog-A. It also discusses the model of devices such as POSFET which employs piezoelectric material as transducer layer for converting mechanical stimuli into electrical signal. The model includes force attenuation due to the protective layer attached to the sensor, and shows close matching with the experimental data.

Chapter 7 includes the electrical and electromechanical tests carried out to characterise the devices and performance of the sensors. The MOSFET devices were characterised and parameters such as transconductance, threshold voltage and mobility were calculated. The capacitance related measurements were carried out on the sensing layer to evaluate the dielectric properties. The sensing parts were characterised individually as well as in extended gate configuration with the MOSFET to evaluate their sensing properties. The devices were also tested in bent condition to analyse the effect of bending on device performance, and these results are summarised towards the end of the chapter.

The thesis is concluded in Chapter 8 and also highlights the areas which require more attention and outline the possible future works.

1.4 Key contributions of this thesis

The four important key contributions of this thesis can be summarised as follows:

- The fabrication of thin silicon based devices using modified etching process with reduced number of mask plates and processing steps.

- Development of the piezoelectric nanocomposite P(VDF-TrFE)/BT nanocomposite which suppresses the sensitivity to temperature.

- Process optimisation for the RF sputtering of piezoelectric AlN that do not require poling.

- Modelling the effect of bending on device behaviour using analytical equations and their implementation in the circuit design tool.

Chapter 2. State-of-the-Art in Ultra-Thin Silicon Technology

In this chapter, state-of-the art relating to various processes which have been used to obtain ultra-thin silicon are presented. The comprehensive study presented in this chapter includes important topics such as thin wafer handling, thin wafer dicing, thin chip packaging, deviation in major physical properties from bulk, and potential application of UTCs in 3D IC, robotics and medical health. As a case study, thin-silicon based tactile sensor is included towards the end of the chapter, which sets up the direction for the variety of work presented in this thesis.

2.1. Ultra-thin silicon

The electronics on flexible substrates and enabling technologies for the same are being pursued by researchers around the globe due to the huge scope of this fast-emerging field in a wide range of applications summarised in Figure 2.2**.** These include radio frequency identification (RFID) tags, flexible displays, flexible solar cells, and futuristic areas such as electronic textiles/skin in wearables, robotics, prosthetics, and healthcare, which are considered as driving applications for the advancement of flexible electronics [6-9]. Several initiatives from governments and industry have also contributed to the progress and it is estimated that the market for flexible electronics is to reach $300 billion by 2028 [10]. Many of the current applications of flexible electronics require high-performances (e.g. large drive currents (in mA range) and higher transistor switching frequency (MHz-GHz).) at par with today's CMOS electronics - ideally with cost-effective fabrication. For example, the wireless communication in applications such as *m*-health, where wearable/conformable skin-like sensors patches are being proposed for real-time health monitoring, will require data handling in frequency bands up to ultra-high frequencies (0.3 – 3 GHz) [11]. Likewise, the faster communication, higher bandwidth, and efficient distributed computation will make the high-performance requirement inevitable in connected objects in emerging and futuristic concepts such as Internet of Things (IoT) or Internet of Everything (IoE) [12]. At the same time, promoting their widespread use will make the low cost of electronics a critical requirement.

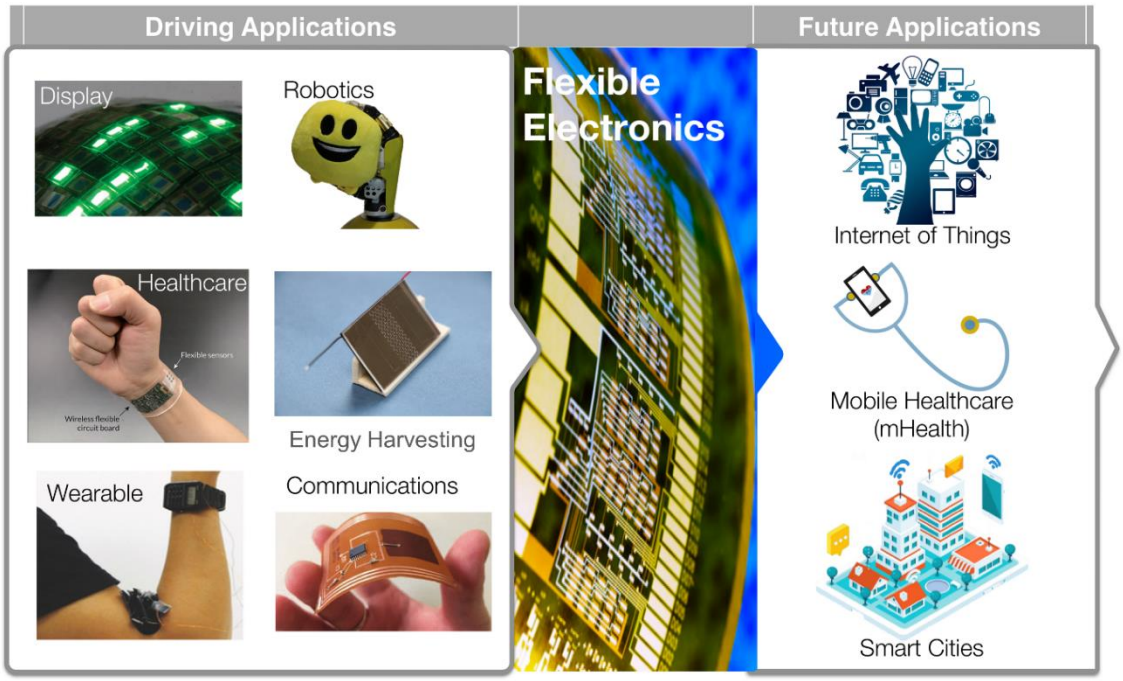


Figure 2.2: Various application areas for UTC in the flexible electronics landscape. The left side shows the already demonstrated applications and the right side represents the future applications which will be enabled by these applications.

The high speed and reliable operation of electronic devices and circuits is currently possible with conventional rigid and planar inorganic semiconductor-based technology. However, with the advancement in electronics and need for application-specific requirements, many semiconducting materials are investigated. However, the lack of flexibility and conformability often puts hurdles in their effective utilisation in many applications such as conformable electronic skin, wearable and implantable electronics.

In order to compare the suitability of various materials for realising high performance electronics, a comparison is presented in Table 2.1, between carrier mobility (μ), channel length (L) and normalised cut-off frequency ($f_{T_{norm}}$) of transistor fabricated using different semiconducting materials as channel material. While mobility is a material property, channel length is decided by the available technology. The cut-off frequency is also a very important measure of device performance as this decides the speed of the transistor. Assuming the FET parameters such as channel width, oxide capacitance etc. to be fixed, cut-off frequency dependency boils down to mobility and channel length and can be written as:

Table 2.1: Comparison between mobility, channel length and normalised cut-off frequency of transistors fabricated using different semiconducting materials.

Material	Mobility [cm^2/V-s]	Channel length reported [nm]	Normalised Transit Frequency [GHz]	I_{on}/I_{off}	Ref.
Mono-crystalline silicon	300-1200	14	4250	10^9	[13, 14]
Amorphous silicon	5-32	12500	0.00115	10^5	[15, 16]
III-V semiconductors	400-12000	75	165	10^4	[17-20]
MoS_2	700	300	42	10^8	[21-24]
WS_2	234	6000	3.8	10^8	[25, 26]
Pentacene	1.5	2000	0.0114	10^2	[27-29]
CVD Graphene	24000	40	100	10^2	[30-32]

$$f_T = k\frac{\mu}{L^2} \tag{2.1}$$

where k is proportionality constant arising from the above stated assumptions. Considering devices which have same parameters except mobility and channel length, cut-off frequency

can be normalised w.r.t. the proportionality constant and can be written as:

$$f_{T_{norm}} = \frac{f_T}{k} \tag{2.2}$$

Comparing these three parameters, it can be clearly observed that the devices based on mono-crystalline silicon outperform most of the semiconductor materials. Although graphene, carbon nanotubes and some 2D materials have been reported to show higher mobility than silicon, they are still in the nascent stage of development and far from commercialisation. Moreover, the

cost of compound semiconductor wafers is much higher ($1900 for a 2-inch. bulk gallium nitride substrate, vs. $10-$50 for a 6-inch silicon wafer), making it an unfavourable choice at industrial scale.

In terms of flexibility of devices, organic semiconductors, thin -film semiconductors such as a-Si:H and 2D materials dominate the area of flexible electronics due to their ability to be processed over large area at a relatively low temperature (< 250^{o}C) and low cost. However, the issues such as low mobility, lack of bandgap, scalability, reliability, yield and through-put have limited their usage in applications requiring high performance. In this scenario, silicon-based microelectronics industry with the ability to bring device dimensions down to nanoscale and exponentially scale the device densities up to billions of devices per mm^2, makes it an obvious choice as a potential and leading candidate for flexible electronics.

Nonetheless, Si chips are traditionally fabricated on wafers up to a thickness of one millimetre. In this rigid form, the wafers are stiff and stable enough to survive the fabrication process but lack flexibility. Upon thinning down to thicknesses below 300 µm, they are termed as thin wafers (in the case of 6" or above) but remain stiff and require careful handling. Going further below 100 µm thickness, the wafer may break or warp by its own weight. Remarkably, under 50 µm regime, they become flexible and mechanically more stable [33]. The wafers ranging between these limits are termed as ultra-thin silicon wafers and the chips realised

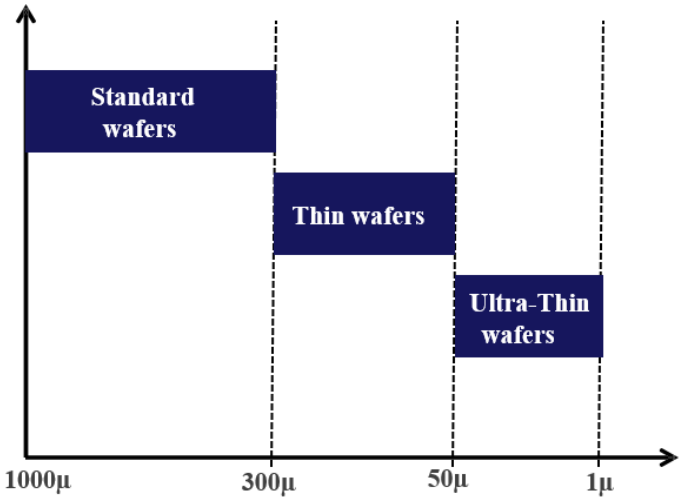


Figure 2.3: Wafer thickness based terminology classification. For thickness above 300, wafers are termed as standard wafers whereas when their thickness falls below 50, they are termed as ultra-thin wafers.

with this thickness are termed as ultra-thin silicon chips or UTC (Figure 2.3), which are ideal for the futuristic high-performance thin-film and flexible electronics. Due to the excellent form factor of UTCs, their integration on flexible substrates is better than the conventional thick chips.

Furthermore, they retain the high-performance of electronics on conventional thick chips, which is another critical requirement of numerous applications previously highlighted. Using UTC also reduces the volume of package and gives reduction in parasitic capacitance and leakage currents, thus allowing better high-frequency performances and lower power consumption when compared to devices on bulk counterpart. The seamless integration of UTCs on flexible substrates will also bring noticeable improvements in applications such as implantable electronics, where conformability and closeness with biological cells and tissues improve the signal capture. Therefore, attempts are continuously being made to realise and implement flexible chips by either pre-processing (i.e. before fabrication of devices) or post-processing (i.e. after fabrication of devices).

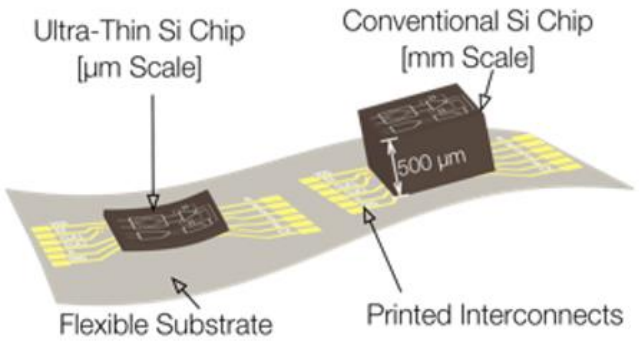


Figure 2.4: Illustration showing the package volume when an UTC is used in comparison to a conventional chip.

2.2. Historical Perspective

Interest in ultra-thin silicon and based devices is not very sudden and new. It is the result of gradual development in technology and demand. The market study of major players in the area of thin silicon has been included as Appendix 1, which clearly highlights the important industrial fields which are pushing the growth of thin wafers. On the academic research side, Figure 2.5 plots the trend in the growth of ultra-thin semiconductor and the related technologies where the cumulative total number of publications and publications related to specific areas are plotted against the years from 1965 onwards, based on data obtained from

Web-Of-Knowledge. The trends are plotted only for articles having the phrase "thin silicon" or "thin chip" in their titles. As can be seen, the use of thin semiconductors towards flexible electronics dates back to the 1960s. Initially, thin silicon (Si) was explored as an active material to realise a large flexible array of solar cells for space applications [34]. From there on, a progressive trend in the area of thin silicon solar cell and ultra-thin silicon solar cell can be observed. Another area where significant works on thinning of silicon has been pursued was for realising Silicon-on-Insulator (SOI) wafer, by bonding a silicon wafer over another oxidised silicon wafer and followed by grinding/thinning one of the wafer commonly known as the bond and-etch-back SOI (BESOI) process [35]. The gradual growth of thin-SOI, followed by ultra-thin SOI and the emerging progressive trend in extremely-thin-SOI technologies, is evident from Figure 2.5. A significant number of articles related to SOI technology, but not having "thin-silicon" as a part of their title, may have been excluded in our analysis. The SOI wafers have also been used to fabricate UTCs[36]. However, the high cost of SOI wafers

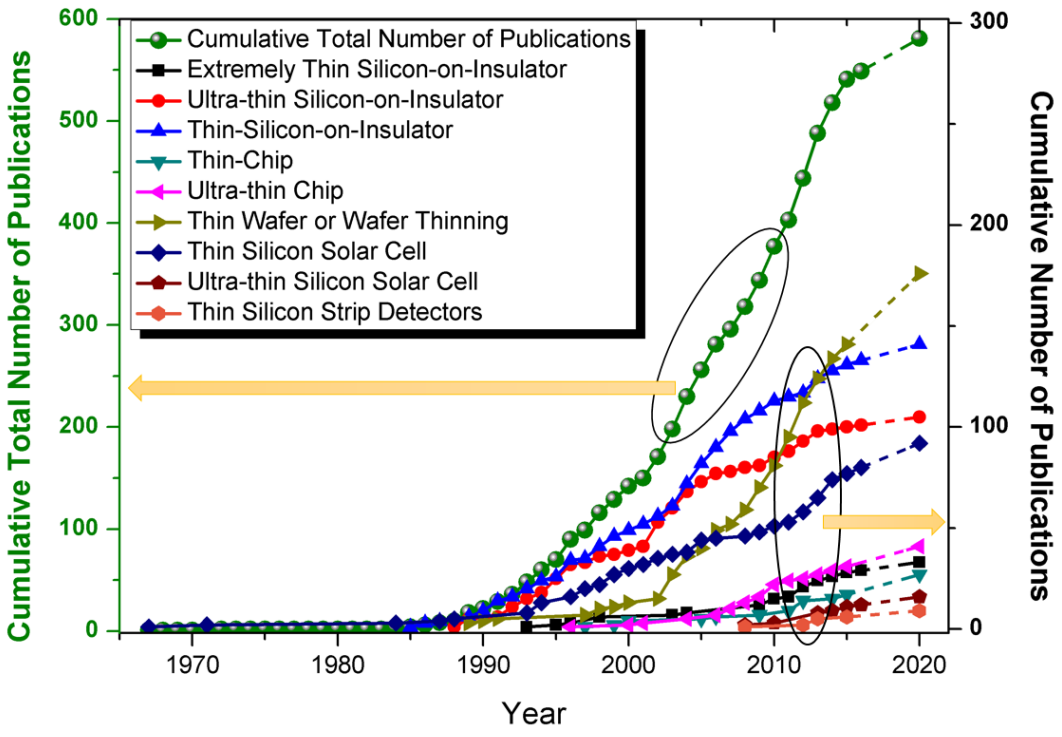


Figure 2.5: Plot of cumulative number of publication in major area and cumulative total number of publication vs year showing the progress in area of ultra-thin silicon. [Source: Web of Science]

(approximately an order of magnitude higher than bulk wafers) is driving researchers around the globe to find innovative low cost techniques to obtain UTCs. The increased interest in the area of thin wafer or wafer thinning could also be attributed to increased demands for 3D ICs, and flexi-chips. Overall, since the early 80's there has been significant progress in the field of thin silicon based flexible electronics and the trend indicates that this will continue to grow due to huge potentials and industrial need.

2.3. Ultra-thin silicon properties

The physical dimension could significantly influence the material properties and therefore could have implications for electronics devices. In the case of UTCs, the properties of electronics substrates may differ from their bulk counterparts in terms of mechanical flexibility, carrier mobility, thermal coefficients and optical transmittance. These variations open multiple new windows of opportunities, which are otherwise difficult with bulk silicon.

2.3.1. Mechanical properties

The thinning process, irrespective of the methodology, has a direct impact on the mechanical properties of the thinned electronic substrate. For example, the sub-surface damage (SSD) and deep cracks in the silicon during thinning by wafer grinding results in poor bending and eventually leads to early breakage of UTCs. Likewise, the etch pits and hillocks formed during thinning by wet etching result in stress localisation, which in turn decreases the breaking strength of silicon. The Young's modulus (E), a constant number and a measure of strength of bulk silicon, becomes thickness dependent, especially when the thickness hits the nanometre regime. After a certain thickness, h_b, the dependence of Young's modulus on the thickness [37] is described as:

$$E = 54.872 * h_b^{0.226} \tag{2.3}$$

For silicon, h_b is approximately 80 nm and this value depends on parameters such as in-plain strain, Poisson's ratio and the bulk value of Young's modulus. The nanometre range is hard to achieve with mechanical grinding or wet etching of bulk silicon wafer, nonetheless with SOI wafers it is possible to obtain nanoscale thick UTCs. The stress generated during bending also depends on the mechanical strength of UTCs as:

$$\sigma_{st} = \frac{E * h}{2R} \tag{2.4}$$

where *h* is thickness of UTC and *R* is the bending radius. This means for the same stress; the thinner chip will have a lower radius of curvatures or can be bent to a higher degree. This is clearly indicated in Figure 2.6(a), where the estimated values of bending strain (calculated using MATLAB code based on equations in [39]) are plotted against the radius of curvature

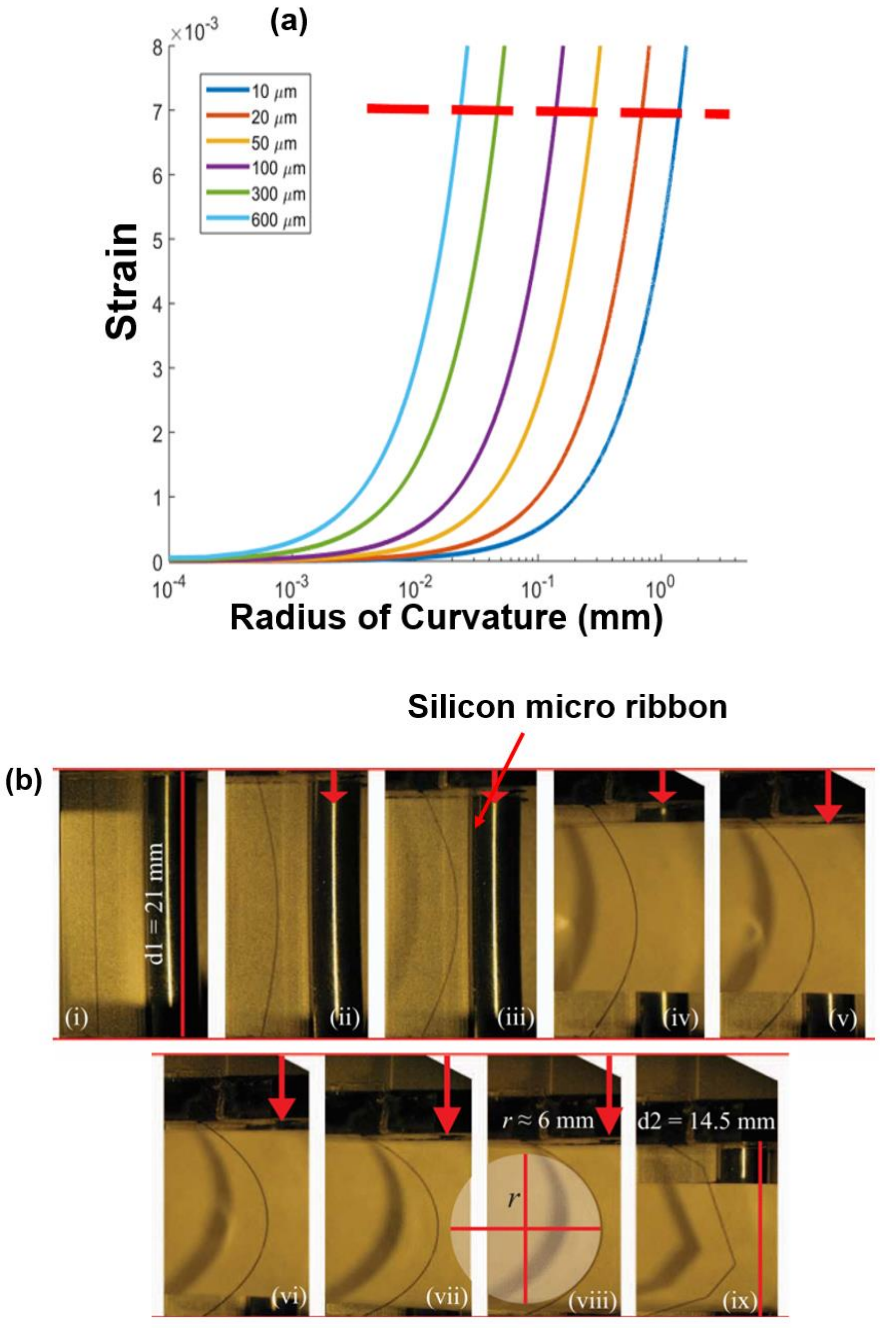


Figure 2.6: (a) Plot showing the calculated bending strain vs. radius of curvature for various thicknesses of Si wafer. This plot of shows that at a constant strain level, thinner chip can undergo higher bending i.e. lower radius of curvature. (b) (i-ix) Optical pictures of silicon membrane of length 21 mm encapsulated between PDMS layers, under sequential bending. It can observed that the sample achieved the bending radius of 6 mm before breaking. [38]

for silicon wafers with different thicknesses. The dashed line at 0.007 parallel to x-axis indicates the typical breaking strain for UTC.

2.3.2. Electrical properties

Ovbdofvb The stress experienced by the top surface of UTCs is directly proportional to Young's modulus of substrate and its thickness. For this reason, polydimethylsiloxane (PDMS) (E = 360-870 kPa) could be a better substrate than polyimide (PI) (E= 2.5 GPa). This is also reflected in Figure 2.6(b), which shows UTC over PDMS substrate bending up to 6 mm without breaking[40]. The neutral plane concept has been proposed often, to reduce the stresses experienced by electronics on UTCs. This can be achieved by laminating or encapsulating the UTCs between two layers of suitable thicknesses. However, in practical terms it is difficult to fabricate or integrate UTCs in the neutral plane.

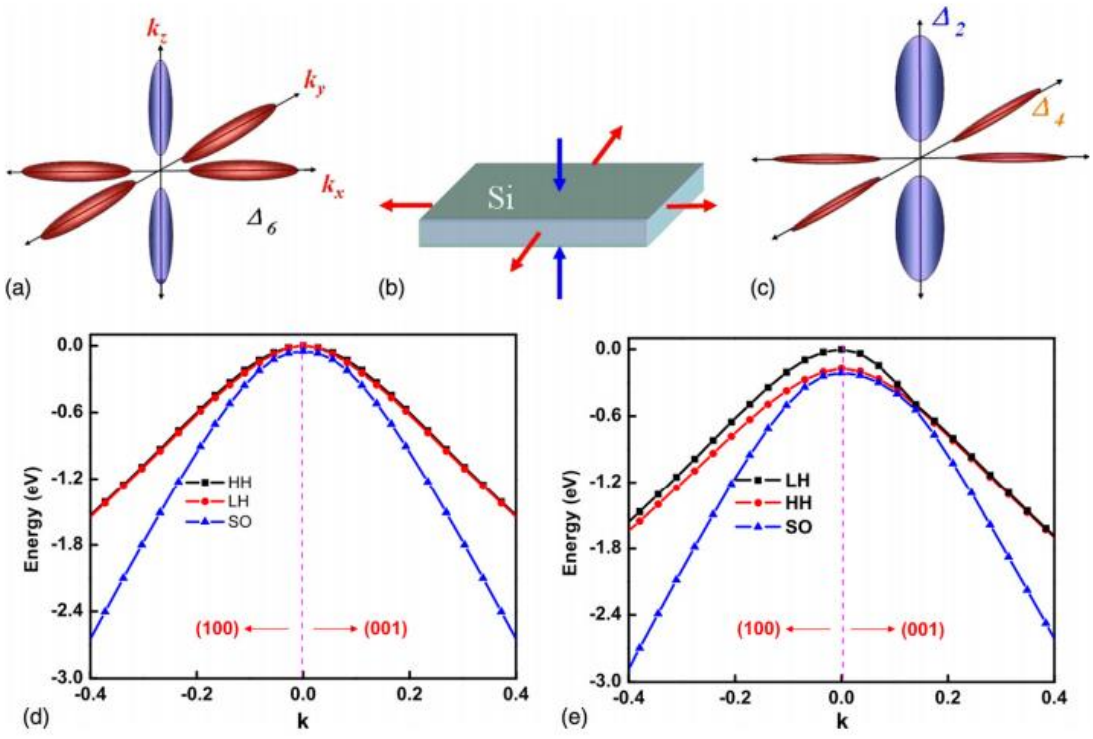


Figure 2.7: Si conduction and valence bands as a function of biaxial strain. (a) The six Si conduction band valleys along three different directions are equally populated without strain; (b) schematics of bulk Si under biaxial tensile strain; (c) under tensile strain, the valleys are split into two groups. Electrons tend to populate the lower Δ_2 valleys rather than the higher Δ_4 valley; (d) and (e) show the three-top valence band near the Γ point for the strain-free and 1.5% biaxial tensile-strained Si, respectively. [41]

The strain generated during thinning or bending, causes variations in the crystal structure of electronic substrate, which could lead to changes in the electrical properties of semiconducting

material and eventually the electrical output of devices on them. This internally generated or externally applied strain leads to splitting of bands into sub-bands, lifting the band degeneracy and changes in effective mass of carriers, as shown in Figure 2.7 [42]. At transistor level, this change in the effective mass results in the variations in the charge career mobility. The strain in UTCs also changes the semiconductor to metal work function, and shifts the flatband voltage. These changes are reflected in devices through shifts in their threshold voltage[43]. In the case of SOI wafers, the charge carrier mobility depends on the thickness of the active layer. The hole and electron mobility are reported to decreases monotonically when the thickness of the Si layer is reduced from 60 nm to 2.7 nm due to additional confinement caused by Si/SiO_2 interface[44]. For easing complex circuit design and precisely predicting their response under different bending conditions, it is necessary to understand these variations and implement them in design tools.

2.3.3. Thermal properties

Thermal properties of UTCs are important, as temperature has a significant impact on the performance and reliable operation of electronics. The thermal behaviour of UTCs is significantly different from thick chips.

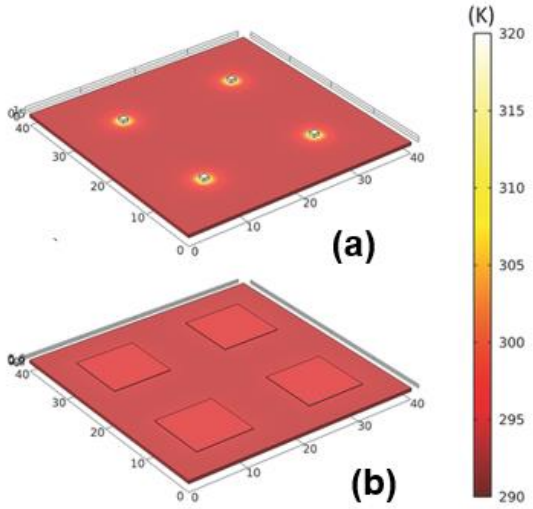


Figure 2.8: COMSOL simulation of heat distribution in (a) 500 µm thick chip with area 1 mm² showing creation of hot spots – up to 45°C for a low input power density of 1 W/cm² (b) 100 µm thick with area 100 mm², showing temperature rise of only 2°C above ambient at same power density. [45]

The effect is more visible in the case of UTCs as the thermal conductivity is known to decrease with thickness. For example, the thermal conductivity of less than 100 nm thick UTCs is half

the value of intrinsic bulk silicon (~148 $Wm^{-1}K^{-1}$) [46]. Low thermal conductivity means the heat generated is not easily transferred to the package and therefore there is a price to be paid when we think of UTCs as the solution for high-performance flexible electronics. The thermal issues can be overcome by incorporating on-chip cooling architecture. However, this is a cumbersome process and will typically lead to power-hungry UTCs. A potential alternative to overcome the challenges related to thermal issue is to use large size UTCs [45]. As an example, COMSOL simulation (Figure 2.8) reported elsewhere[45] show that a 1mm x 1mm conventional chip (0.5 mm thick) on a 0.5 mm thick polyimide, can heat up the substrate to 40^{o}C, even with a small power density of 1 Wcm^{-2}. However, with a larger chip the heat can be distributed over a larger area and therefore local heating can be reduced. Applying the same argument to thin chips (~100 µm thick) with bigger area (10 mm x 10mm) and applying the same power, the simulation results show only 2^{o}C higher temperature than ambient on polyimide substrates. This much raise in local temperature is acceptable in terms of minimal thermal effects on performance, as well as biomedical (e.g. implants) and wearable applications where higher temperatures can damage living tissues or skin, hence maintaining lower temperatures is critical. Keeping this in mind, the chips fabricated in this project have the dimension of 1 cm x 1 cm, which makes sure that the thermal dissipation do not create any mismatch with the flexible substrate.

2.3.4. Optical properties

Silicon becomes optically transparent at very low thickness starting with the red region and progresses towards the blue region as the thickness is gradually reduced. This is owing to varying absorption coefficients of silicon at different wavelengths. For relatively thicker silicon (>10 µm) this behaviour could be studied with Fresnel Equation of Reflectance (equation (2.5)) and Beer-Lambert's law (equation (2.6)), given the optical parameters [47]:

$$R\ (\%) = 100\ \left|\frac{n_{Air} - n_{Si}(\lambda)}{n_{Air} + n_{Si}(\lambda)}\right|^2 \tag{2.5}$$

$$A\ (\%) = 100\left(1 - e^{-\alpha_{Si}(\lambda)x}\right) \tag{2.6}$$

where, n_{Air} is the refractive index of the air (~1.00), n_{Si} is the refractive index of silicon, and λ is the optical wavelength, α_{Si} is the absorption coefficient of silicon at a given wavelength and x is the optical path length. Figure 2.9(a) shows the optical transmittance versus wavelength for silicon of various thicknesses. The transmittance spectrum

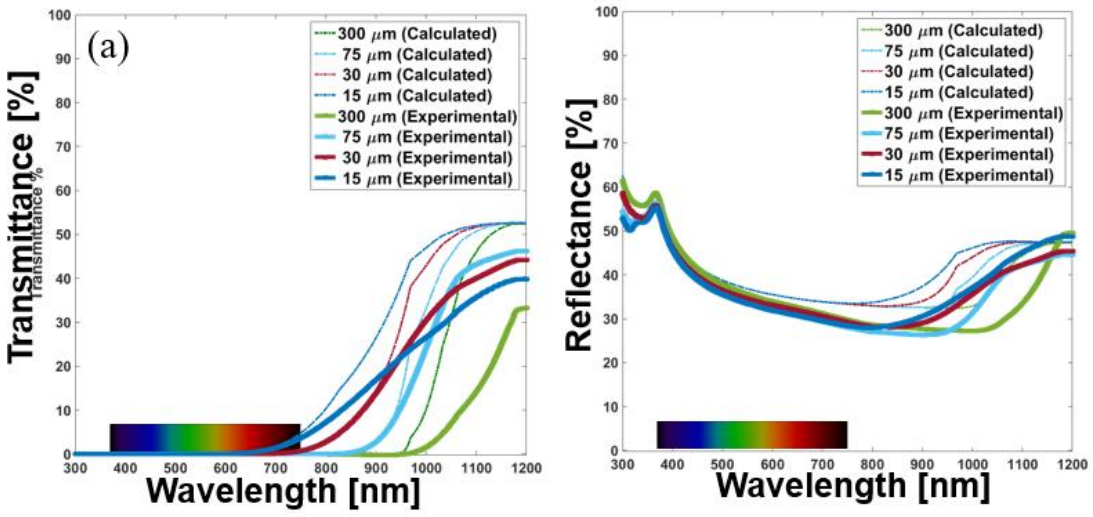


Figure 2.9: (a) Trasnmittance percentage of light plotted against wavelength for different thickness of silicon (b) Reflectance percentage of light plotted against wavelength for different thickness of silicon. [38]

indicates that silicon is more transmittive in the red end. Figure 2.9(b) shows the spectral reflectance for silicon at various thicknesses. For applications such as photodetectors or solar cells, where higher absorptance is required along with flexibility, the optical path length in thin silicon can be improved by using special optical trapping techniques such as Lambertian trapping[48, 49], texturing[50], antireflection coatings[51]. This property of varying optical transmittance with thickness could be exploited to monitor and control the etching of silicon as the thickness becomes a function of transmitted light. Back thinning also contributes to achieving higher quantum efficiency in both Charge-Coupled Device (CCD) and Active Pixel Sensor (APS) image sensors. However, their red and infrared response is decreased due to thinning. Nonetheless, this could be addressed with special optical trapping techniques as described above. The changes in optical transparency with thickness means the UTCs could also find use in applications other than those requiring flexible electronics.

2.4. Ultra-Thin Chip Methodologies

There are several ways for thinning the bulk silicon in order to obtain UTC. These methods can be broadly divided into three categories: (A) Physical Thinning (B) Chemical Thinning (C) Physico-Chemical Thinning as shown in Figure 2.10. Many of these methods are also applicable for thinning other inorganic semiconductor wafers. Some of these thinning methods involve pre-processing or post-processing, or both processes.

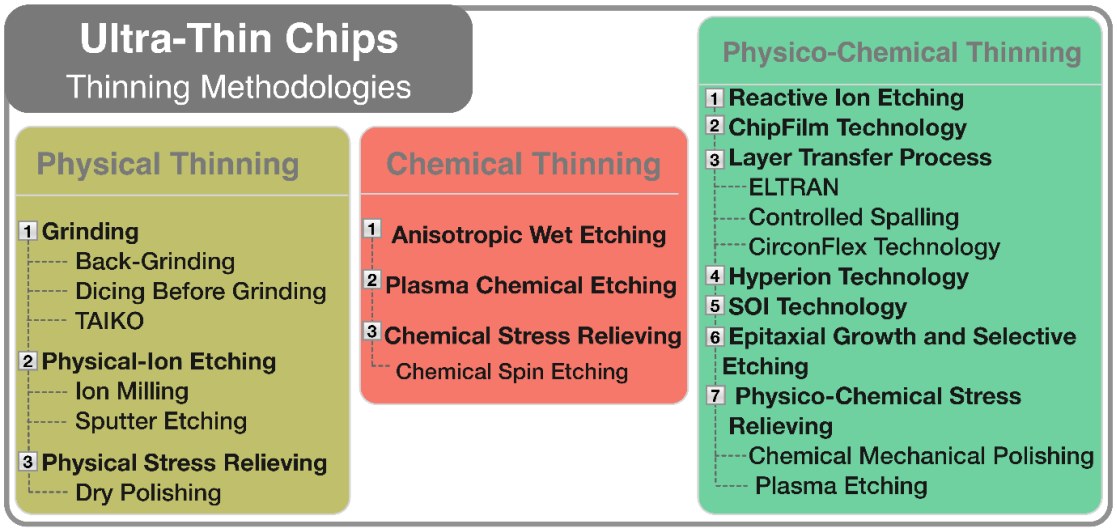


Figure 2.10: Classification of thinning methodologies

2.4.1. Physical Thinning

In processes which come under physical thinning, bulk silicon is removed by mechanical action. The material removal rate in physical thinning is quite high compared with other processes. The various physical thinning processes are:

2.4.1.1. Grinding

2.4.1.1.1. Back Grinding

Back grinding is the most popular, convenient, and well-established method for thinning down wafers to the required thickness. In the back grinding approach, the removal rate is large compared with other methods such as wet etching. Normally, it is carried out in two steps: coarse grinding and fine grinding. Coarse grinding uses a grinding wheel with large diamond abrasives (1.40 mm – 0.40 mm) embedded in a ceramic pad, to remove the majority of the silicon and to give a fast feed rate to achieve high throughput [52]. However, it does have the disadvantages of applying mechanical stress and heat that causes deep scratches on the

backside of the wafer. A second step of fine grinding is carried out where a fine grinding wheel with smaller diamond abrasives (0.18 mm—0.012 mm) and a slower feed rate are used to achieve a smoother finish. This results in a lesser stress and sub-surface damage (SSD). Following the back grinding, some steps are recommended to be followed to release the stress and damages generated during the back grinding. This can be done by slowly removing the micro-cracks on the wafer surface by using any of the stress-relieving techniques.

One of the major problems associated with grinding is damage during delamination of the thin wafer from the protection tape. Thin wafer can break or warp during delamination, due to lack of support. DISCO has proposed a technique, called TAIKO, for back grinding in which the thin wafer is supported by the outer rim of the wafer, thus reducing the chances of wafer breakage. X.Zhang *et.al*. [53] reported piezo resistive stress sensors realised by backgrindng a 400 μm to 100 μm thickness.

2.4.1.1.2. TAIKO® Process

TAIKO is a Japanese word for drum and the process is named TAIKO because the processing results in a wafer with this shape. This process is a variation of grinding where back-grinding is done only on the inner area from the rear side, leaving a boundary at the outermost area of the wafer in the form of a ring[54]. The ring section works as a support for the thinned wafer, resulting in better strength and less warpage as can be observed from Figure 2.11(b). However, this method is not suitable for some wafer processes during which vacuum tables are used [55]. Using this technique, K.Shinsho *et.al*. [56]demonstrated monolithic pixel devices with thickness of 100 μm utilizing a 0.2 μm Fully Depleted Silicon-on-Insulator (FD-SOI) process technology. With small increase in leakage current the devices exhibited excellent performance to infrared and red laser lights.

2.4.1.1.3. Dicing Before Grinding (DBG)

DBG is one of a variant of a grinding technique proposed to solve the problem of breakage of the thinned wafers (obtained through grinding) during transport and the backside chipping that occurs during dicing [59]. DBG is performed as a post-processing step, as indicated in Figure 2.11(c). In contrast to other grinding techniques, in case of DBG, during post-processing the wafers are first partially-grooved and then grinded. Die singulation occurs when the wafer is

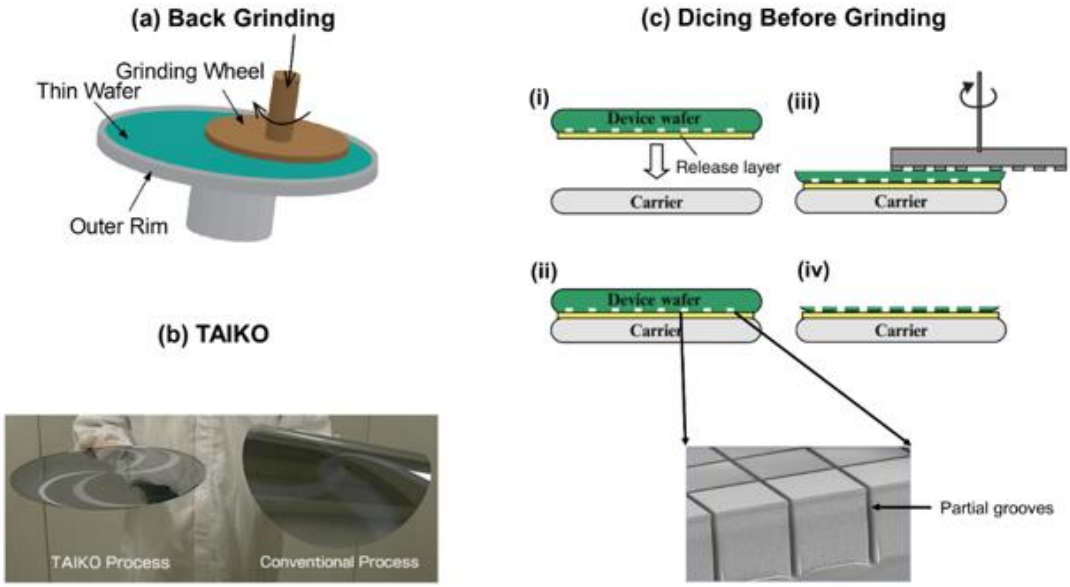


Figure 2.11: (a) Illustration of Back Grinding. (b) Thin Wafer obtained by the TAIKO process in comparison to warped wafer obtained by conventional back grinding. [57] (c) Illustration of Dicing Before Grinding technique. [58]

thinned below the level of this cut[60]. Using this technique, the wafer can be grinded to an ultra-thin final thickness. The risk of fracture is avoided, as there will not be any edge chipping [61]. R.Zhang et.al.[62] thinned and sigulated wafers consisting memory cell upto the thickness of 25 μ

2.4.1.2. Physical Ion Etching

It is a physical process to remove the atoms from the substrate surface by bombardment with energetic ions. Therefore, etching occurs by physically knocking atoms off the surface. The major disadvantage associated with the ion etching is the re-deposition of the product. The re-deposition can be minimised by etching at low pressure (< 1 mTorr).

Ion etching can be done using two different approaches: (1) ion milling and (2) sputter etching.

2.4.1.2.1. Ion milling

The ion beam is generated by ionising neutral gas atom in a discharge chamber which is then accelerated towards the substrate. By focusing the beam over a substrate, as shown in Figure 2.12, any arbitrary shape can be etched, but there is always some re-deposition in this process which may reduce the effective etch rate. Sometimes, gas-assisted etching is used, in which a gas is flown into the work chamber to increase the speed and selectivity, in that case this can be considered as a physico-chemical etching.

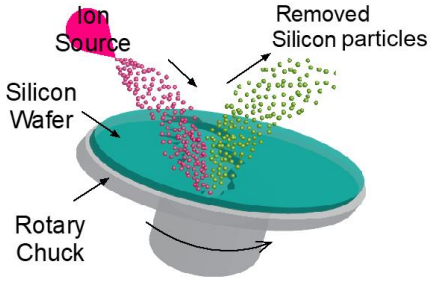


Figure 2.12: Illustration of Physical Ion Etching.

2.4.1.2.2. Sputter Etching

This process is based on the physical bombardment of high-energy ions of noble gas such as Argon (Ar^+) on the target substrate. High velocity is imparted to inert molecules using plasma energy. When the ions pass through the plasma region, they gain a high momentum. When the projectile energy of moving ions exceeds the bonding energy of silicon, atoms are dislodged, leading to material removal. Thus, sputter etching depends on the momentum transfer between etchant ions and substrate atoms. It gives an anisotropic profile with low etch rate and poor selectivity.

2.4.2. Chemical Thinning

In chemical thinning processes, silicon is removed using chemical reactions. The chemicals react with silicon to form products, which disassociate themselves from the bulk. These reactants can be either in liquid or gaseous phases. Although the material removal rate is low when compared to some of the physical removal processes, it gives a smooth surface with less SSD. Chemical thinning is mainly done by anisotropic etching of silicon using potassium hydroxide (KOH), and TMAH. The major chemical thinning processes are:

2.4.2.1. Anisotropic Wet-Chemical Etching

Anisotropy is a composition of Greek words meaning “not the same way in all directions” referring to the etch rate. Any wet etching process is composed of mainly five steps: Reactant is transported from solution to substrate surface, followed by its absorption on the surface. A chemical reaction occurs on the surface and the product of the reaction get desorbed from the surface. Finally, the etch products are transported back to the solution.

Wet anisotropic silicon etching is a well-established, easy to implement and cost-effective technology used to realise micromechanical structures in the fabrication of different kinds of miniaturised sensors. A similar process with some modifications can be adapted to obtain ultra-thin silicon [63].

CMOS compatibility of etchant is a very important requirement for the fabrication of UTC-based sensors and micromechanical structures. Other things which need to be considered are etch rate, the ability to modulate etching with dopants or electrical bias, surface roughness, the availability of suitable masking films, health hazards and disposal issues [64].

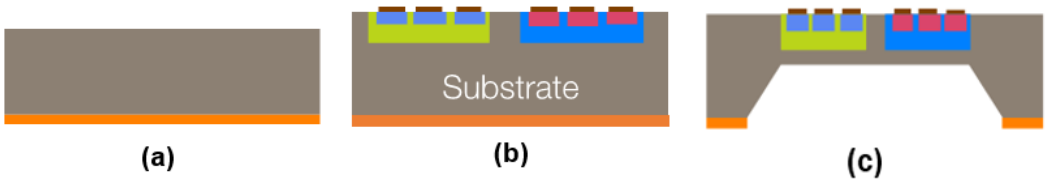


Figure 2.13: Illustration of pre-processing and post-processing modules in Wet Etching.

The most commonly used etchants are hydrazine, EDP (ethylene-diamine-pyrocatechol),, TMAH and KOH water solutions. However, handling of hydrazine and EDP is dangerous due to their high toxicity and instability. Aqueous KOH solutions are the most widely used, due to lower toxicity as well as yield good etched surfaces, but compatibility with CMOS processes is not good enough due to mobile ion (K+) contamination and poor selectivity towards aluminium.

In this scenario, TMAH shows very good results. TMAH is IC-compatible, nontoxic, has very good anisotropic etching characteristics and does not decompose below 130ºC. However, undercutting ratios for TMAH solutions are higher than those for KOH-based solutions. In order to reduce the undercutting ratio, isopropyl alcohol (IPA) is generally added to TMAH solutions [65]. As illustrated in Figure 2.13, wet etching needs a pre-processing or mid-processing stage where a hard mask is defined, which is mostly Si_3N_4 or SiO_2. The protection of front-side of the wafer from etchant is critical for this route to obtain UTCs as otherwise the

etchant may render the devices on the front side useless. To provide front-side protection, a custom-made wafer holder made from etchant resistant material or

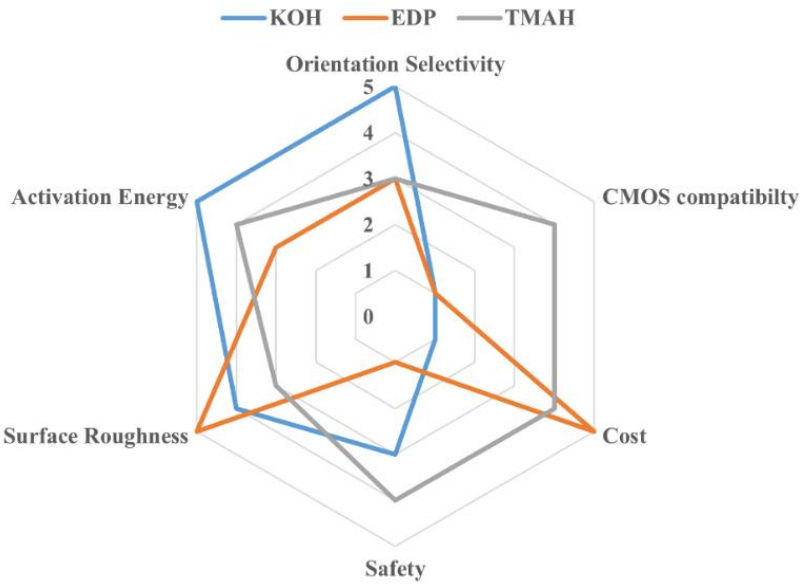


Figure 2.14: Radar chart showing comparison between KOH, EDP and TMAH on major etching related parameters.

polymeric protection layer is used. The concentration of etchant is maintained regularly during this process, in order to have better control over the total etch time. A potential solution for monitoring the etch process is to exploit the change in optical transmittance with thickness. Dahiya el.al. [63] demonstrated ultra-thin silicon ribbons and chips using wet etching methods.

2.4.2.2. Plasma Chemical etching

Plasma etching is the process of using plasma to generate active species (such as atoms and radicals) from a relatively inert molecular gas. The active species then react with the substrate to produce volatile products. For thinning the wafers via plasma etching, they are placed in vacuum chamber and RF excitation is used to ionise a variety of source gases being purged into the vacuum system. Usually the plasma contains fluorine or chlorine ions to etch silicon [66]. The halogen ions react with silicon to form gaseous products. Since the process is a chemical etching it results in good selectivity, with etch rate higher than normal chemical etching. However, the disadvantage of purely chemical etching techniques, specifically plasma chemical etching processes, is that they do not have high anisotropy. This is because of the fact

that reacting species can react in any direction. Moreover, the plasma etch environment is highly reactive with so many reactions going on, that create contamination and can interfere with the etching process.

2.4.3. Physico-Chemical Thinning

This way of thinning is more versatile than pure physical or chemical thinning, as it presents unique combination between both. It provides advantages of both processes, namely; higher etching rate by physical etching and at the same time giving a better surface finish.

2.4.3.1. Reactive ion etching

RIE etching process is typically carried out as a post-processing process, as illustrated in **Error! Reference source not found.**Figure 2.15 (a). Firstly, ions impact on the substrate and physically remove atoms, opening up the area for reaction. This is followed up by ions reacting with substrate and chemical removal of material. Therefore, it is considered as a combination of the sputter etching/ion milling processes and chemical etching. The anisotropicity of the RIE process can be tuned by varying the power and etchant composition. Although RIE gives high anisotropic behaviour, it comes with a low level of selectivity (in absence of any additive) and surface damage.

A special modification of RIE which is gaining interest nowadays is DRIE (Deep Reactive Ion Etching) due to its capabilities to give high etch rate and aspect ratio, better profile control and good uniformity[67]. This process can give etch depth of hundreds of microns with almost vertical sidewalls. In DRIE, subsequent etch and passivation cycles are employed after each other (popularly known as Bosch process). A. Schander *et al*. [68] reported two step DRIE is used to realise highly flexible silicon probes of thickness 20 µm for floating chronic implantation in the cortex.

2.4.3.2. ChipFilm™ Technology

This technology was developed in Institute for Microelectronics, Stuttgart, Germany under the trade name, ChipFilm™. It involves growing epitaxial silicon, layer by layer on a foundation with cavities ensuring the foundation remains strong enough to support the chip during the processing steps but weak enough to let the user snap the finished chip from the wafer [69].

Once the front-end processing has been completed in the post-processing stage, trenches are created along the side-lines of the chip. This leaves the chip in weak attachment to the substrate on the support of pillars only, as illustrated in Figure 2.15 (b). The pick-and-place tool is used to detach the chip from the pillars with mechanical force and place it on a flexible substrate [70]. This technology gives precise control over the thickness and also the original wafer can be used multiple times. S.Ferwana et.al. [71] fabricated flexible sensor based on a stack of two ultra-thin IC-chips using ChipFilm technology. The sensor consists of an almost stress-compensated bottom chip and a stress-sensitive top chip that are in good mechanical and thermal contact

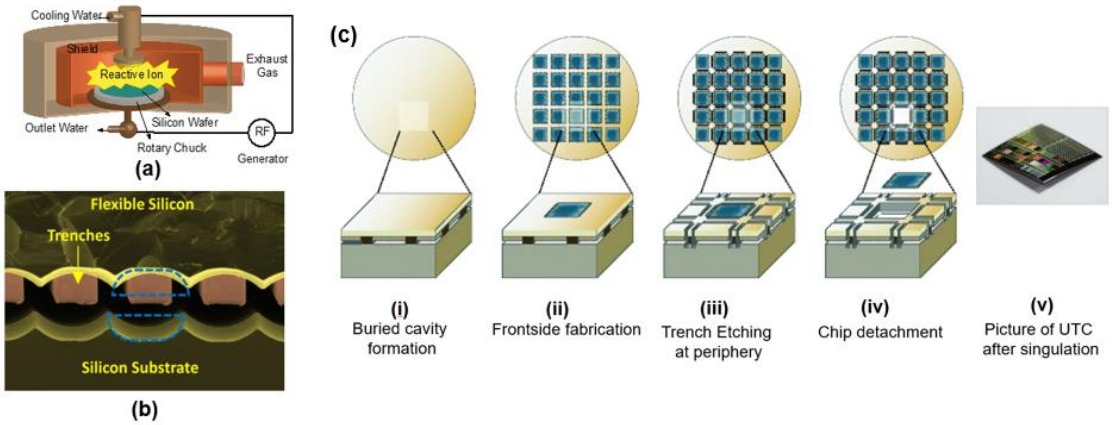


Figure 2.15: (a) Illustration of RIE and (b) SEM image of trenches etched between released top layer and bulk substrate. [72] (c) Illustration of pre-processing and post-processing modules of ChipFilm. [73]

2.4.3.3. Layer Transfer Processes

Layer transfer is another method for the realisation of high quality monocrystalline thin silicon. The layer transfer process starts with the surface conditioning of a silicon substrate followed by epitaxial layer growth on it and device fabrication is followed afterwards. Following device fabrication, a carrier structure is attached to the top epitaxial device layer to provide sufficient mechanical strength during the layer transfer. In some cases, the device layer either detaches due to surface conditioning, whereas in others, the bulk is mechanically removed. Depending upon the method adopted to detach the processed layer, the layer transfer process can be one of three types:

2.4.3.3.1. Epitaxial Layer Transfer (ELTRAN®)

This process is developed by Canon, but in 1994 Yonehara *et al*. [74] successfully demonstrated the transfer of monocrystalline silicon using ELTRAN. The process starts by transforming the top 10 µm of a planar monocrystalline Si wafer porous by anodic etching in aqueous hydrofluoric acid. The porous Si is then oxidised in order to stop the re-organisation during high temperature processing. The wafer is then dipped in HF and annealed in hydrogen atmosphere to close the pores at sample surface[75]. The device layer is deposited by a CVD epitaxy process, followed by device fabrication. The processed wafer is then bonded to an oxidised carrier wafer and the substrate wafer is removed by grinding it down to the porous Si layer [76]. Although developed for flexible solar cells, no report has been made about fabrication of solar cell using the ELTRAN process, but SOI wafers manufactured using this process are commercially available.

2.4.3.3.2. Controlled Spalling Technique

This method, introduced by Bedell *et al.* [77], is a simple, versatile and low cost method for removing surface layers of brittle substrate such as Si, GaAs etc. A tensile strained film is deposited on the top of the substrate during post-processing, as shown in Figure 2.16. The basic principle behind this technique is that under some specific conditions of the tensile strained film, any fracture on the edge of a brittle substrate can propagate downwards to a certain depth below the film-substrate interface and, then, travel parallel to the interface. This results in the removal of upper surface from the brittle substrate in the form of thin film. The entire process being carried out at room temperature, makes this technique suitable for kerf-free ingot dicing, removal of pre-formed p-n junctions or epitaxial layers, or even completed devices. Shahrjrdi *et al*. [78] fabricated nanoscale flexible circuits on 60 Å thick ultrathin body silicon comprising functional ring oscillators and memory cells.

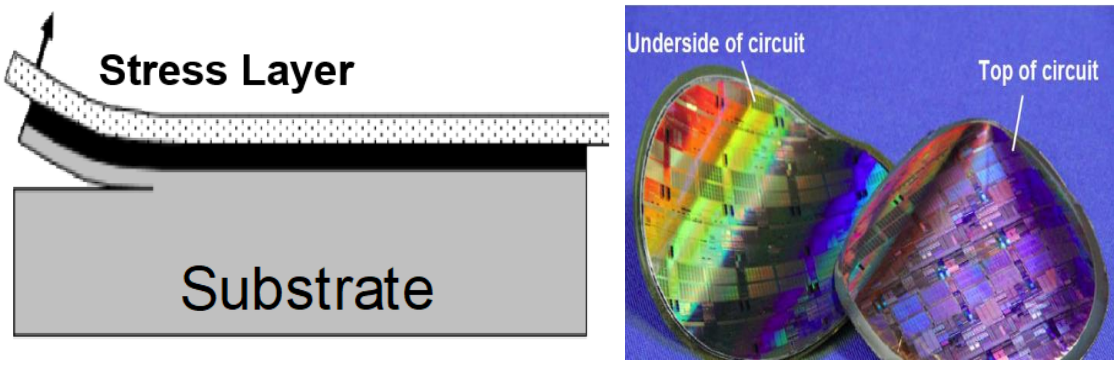


Figure 2.16: (a) Illustration of controlled spalling process (b) Thin processed wafer obtained via controlled spalling technique. [79]

2.4.3.3.3. Proton Induced Exfoliation

Twin Creeks Technologies demonstrated this process with the ability to produce ultra-thin crystalline silicon wafers, for use in solar cells application [80]. The basic principle behind this process is proton-induced exfoliation. Following fabrication, wafers of crystalline silicon are placed in a vacuum chamber, and then they are bombarded with a beam of hydrogen ions, as shown in Figure 2.17(a). By controlling the voltage of hydrogen beam, a layer of ions is precisely deposited. These ions penetrate the silicon and gets embedded just beneath its surface. The wafers are then transferred to a furnace and heated. This causes the ions to combine and expand into microscopic bubbles of hydrogen gas, which in turn causes a few micrometres thick layer of silicon to peel off from the surface of the disk, as can be observed from Figure 2.17(b). The disks can be reused many times, each time exfoliating another layer of ultra-thin silicon [81]. The major limitation of this process is the necessity of using an expensive ion accelerator for energising hydrogen ions. Recently, H-S Lee et.al. [82] fabricated 50 μm thick kerfless silicon wafers using proton induced exfoliation for the purpose of solar cell.

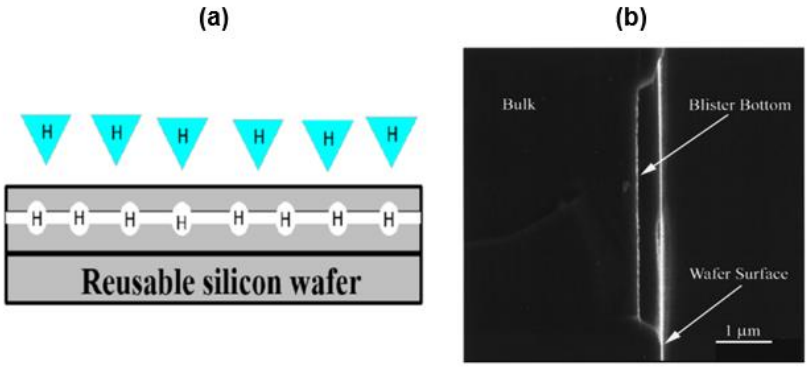


Figure 2.17: (a) Illustration of proton induced exfoliation (b) Image of blister created after heating hydrogen implanted wafer. [83]

2.4.3.4. Using SOI wafer

Using silicon-on-insulator (SOI) wafer is one of the attractive methods of obtaining UTC. SOI wafers provide a range of benefits relative to conventional wafers, such as lower parasitic capacitance, resistance to latch up, lower leakage current and immunity to radiation induced soft errors. While these features of SOI wafers enable high-performance electronics, their higher cost (~$1000 vs. ~$25 for a 6-inch bulk Si wafer) is a barrier. Nonetheless, despite this cost-performance trade-off, the SOI wafers are used in many niche applications, such as low power high performance RF chips [84] and commercial devices such as IBM's PowerPC [85], Global Foundry's 22FDX [86], AMD's dual core module [87]. SOI wafer could also be used for UTCs with precise thickness. This is achieved by fabricating electronic devices on the top active layer of SOI wafer, followed either by: (a) etching the buried oxide layer (i.e. BOX removal), or (b) thinning the backside of the wafer up to the required thickness or buried oxide (i.e. bulk removal), in which case the oxide acts as the etch stop layer.

A commonly-followed approach for handling UTC realised with SOI technology is transfer of the UTC using PDMS or similar intermediate stamp substrate. This process is generally termed as transfer printing. This process has been used by various researchers to transfer transistors, logic gates, RF components [88-90]. This is a simple and low-temperature process for fabricating silicon micro and nano-structures. High temperature steps such as doping and annealing can be carried out before the silicon layer release from the SOI substrate. Hwang *et al*.[91] demonstrated flexible RFICs for in-vivo medical application, using this approach.

2.4.3.4.1. CirconFlex™ Technology

Circonflex™ technology which is a variant of layer transfer, developed by Philips, is illustrated in Figure 2.18(a), where the role of carrier and substrate is performed by the same layer. It allows the transfer of the functional devices to a polyimide layer. It is based on substrate transfer technology, which enables the transfer of the top functional layer of a SOI wafer to practically any flexible substrate. The main advantage is the ability to fabricate the electronic devices in a conventional manner on SOI silicon wafers and then to transfer the devices to a flexible medium as a post-processing step [92]. R.Dekker *et.al*. [93]demonstrated a contact-less RF-ID tag on 10 μm thick demonstrator IC. The chip with dimension 3 mm ×3 mm, has a maximum working distance to the base station of 15 mm.

2.4.3.5. Epitaxial growth and selective etching technique

This technique was developed by Angelopoulos *et al*. [95]. The complete fabrication process is divided into pre-processing and post-processing parts as shown in Figure 2.18(b). In the pre-processing part, highly doped (p^{++} type) film is formed on the front side of the wafer, followed by a lightly doped epitaxial layer which act as an active layer for device fabrication. In post-

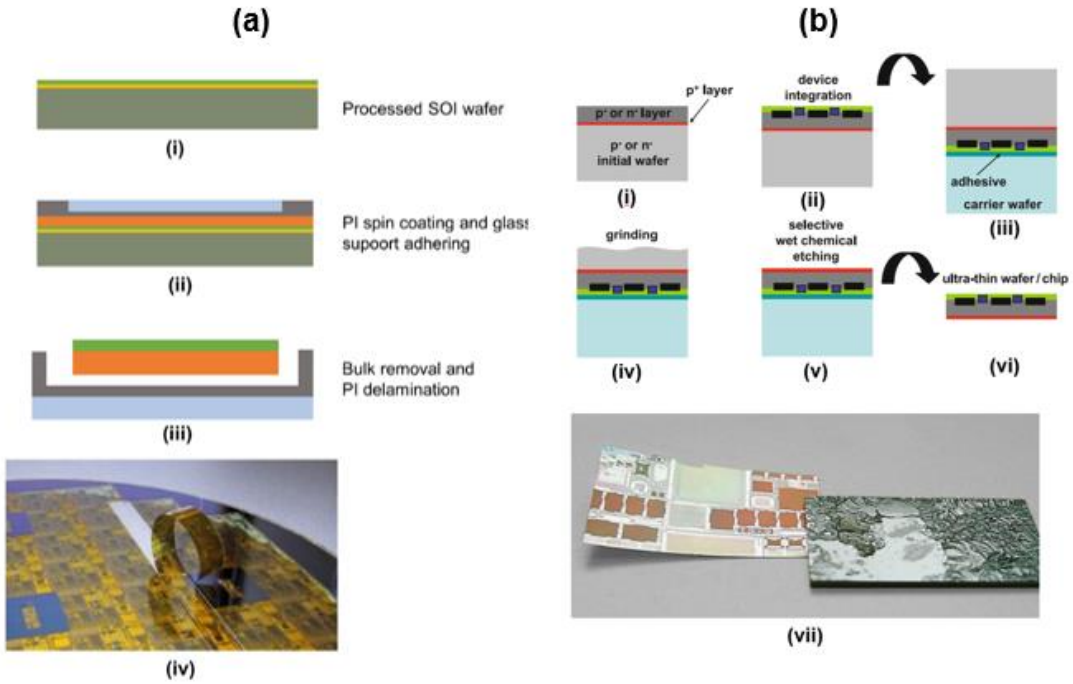


Figure 2.18: (a) Illustration of CirconFlex technique using SOI wafer[94] (b) Various steps in epitaxial growth and selective etching approach. [95]

processing, the wafer is bonded in backside up manner to the carrier substrate and coarsely ground to reduce the thickness. Finally, it undergoes chemical wet etching with p^{++} layer as the etch stop. The final thickness of the UTC is the sum equivalent of the thicknesses of the epitaxial and highly doped layer. This method on the one hand gives an alternative to costly SOI wafer based process and on the other gives precise control over final thickness and uniformity.

Table 2.2: Summary and comparison of various thinning techniques.

Process	Need for pre-processing	Material Removal rate (µm/min)	Typical thickness of semiconductor layer (µm)	Challenges	Ref.
Back Grinding	No	0.1-10	5-10	Deep Scratches on backside Chipping at the edges	[96-98]
TAIKO	No	0.1-10	50-100	Dicing of membrane supported on ring can lead to breakage	[99]
Dicing Before Grinding	No	0.1-10	10-25	>15µm sawlane is required No metal line over sawlanes	[59, 100]
RIE/DRIE	No	0.05 - 10	5-30	Non-uniform surface Chances of frontside contami-nation due to reactive ions	[101]
Proton Induced Exfoliation	No	-	20-30	Need of specifically designed proton accelerator	[102]
Controlled Spalling	No	-	0.006-10	Stress continuity across the lateral dimension is tough to maintain	[78],[103]

Anisotropic Wet Etching	Yes	0.5-2	10-100	Sensitive to temperature and etchant concentration Micro-masking led hillocks formation	[63, 104]
Epitaxial Silicon over Porous Silicon	Yes	-	10-25	Stacking faults due to sintering Warpage on thin chip during detachment from supporting pillars	[105]
Epitaxial Growth and Selective Etching	Yes	0.17-0.2	20-50	Low thermal budget in post-processing step due to high temperature sensitivity of etch stop layer. Extreme control over defects in p+ layer	[95]
SOI BOX/Bulk Removal	No	-	12-20	Fixing and supporting the thin chip during transfer	[94, 106]

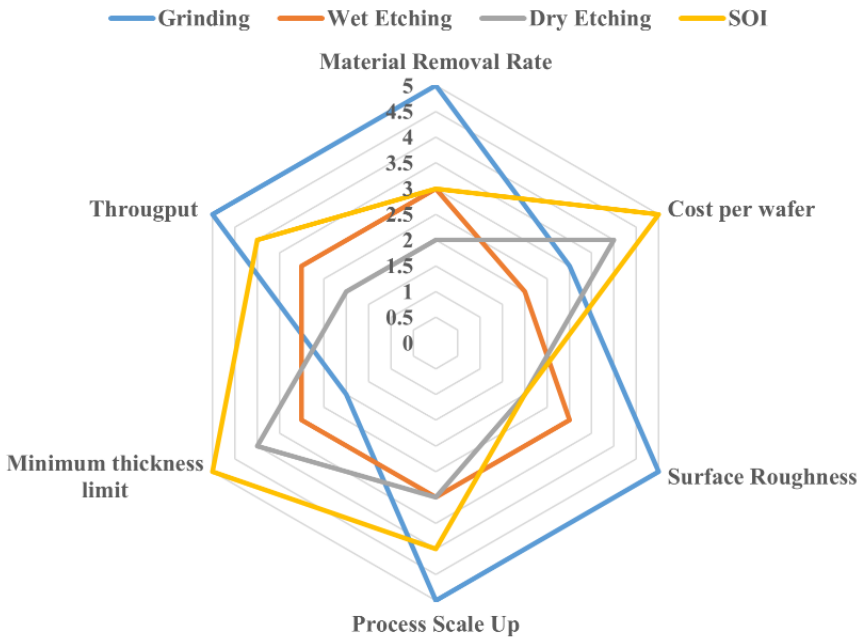


Figure 2.19: Radar chart showing comparison between main four techniques of realizing UTCs.

2.5. Thin Wafer Handling

While significant developments have been made in thinning wafer, a critical manufacturing challenge, i.e. handling of thin wafers, remains a pressing issue. Furthermore, technological

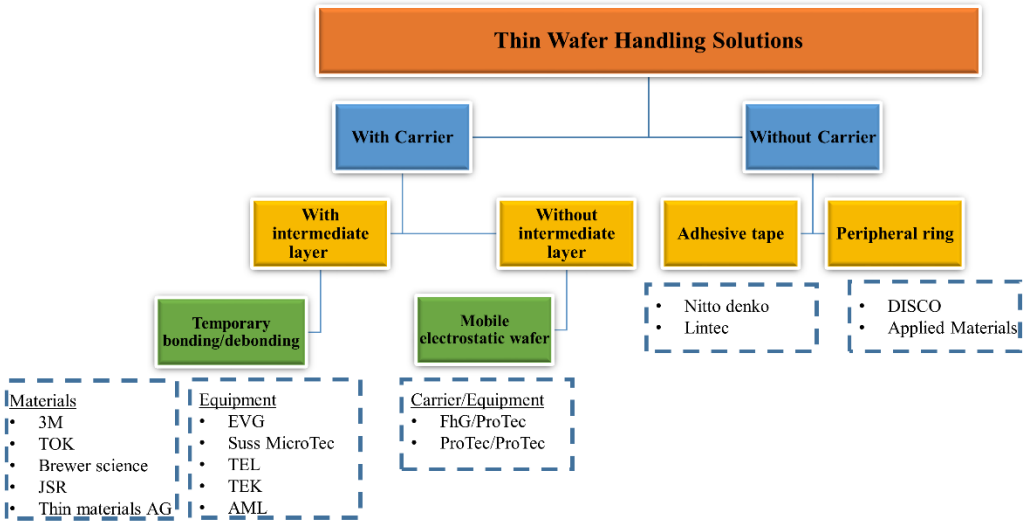


Figure 2.20: Classification of major thin wafer handling practices.

developments in vertical system integration and stacked-die assemblies for MEMS devices,

require new handling techniques for processes that must be performed on the backside of thin or fragile substrates. The techniques which are used for handling thin wafers can be classified as shown in Figure 2.20.

2.5.1. With carrier wafer

2.5.1.1. Using adhesive

In most of the middle end of the line process (MEOL), the thin processed wafer is supported by a carrier wafer. The supporting wafer can be of silicon, glass or quartz and the stack can be handled in most semiconductor tooling with little or no modification. This kind of arrangement allows the usage of existing tooling. In this process, a carrier wafer is attached to the backside of the wafer using a temporary adhesive. This adhesive must hold the wafer securely during the process steps, but easily separate (debonding) when processing is completed. The debonding of the wafer from the carrier is the most challenging step of handling, as a slight mistake or mishandling may break the wafer.

There are three type of debonding techniques:

Chemical release: processes use solvent to dissolve the adhesive between the wafers and carrier. In order to allow the solvent to reach the adhesive layer, perforated carriers are used. This requires specific design consideration while choosing the perforated carrier, since the holes which take the solvent from the bulk to the interface, can also provide a path to adhesive to move down the perforation and contaminate the tools.

Thermal release: involves heating the stack above the glass transition temperature of the adhesive. Above this temperature, the adhesive loses its adhesion capability and the wafer can be separated by applying a sheer load. The carrier wafer does not have specific requirement but temperature constraints place a limitation over the maximum process temperature. The deboning temperature is usually the highest temperature of the whole process and sheer force needs to be as gentle as possible.

UV release: involves illumination of stack from the back side of a carrier to debond the wafers. Since silicon blocks the UV, the carrier wafer needs to be made of special glass in order that UV light can easily pass through. Adhesives with higher temperature stability can be used for this process.

2.5.1.2. Using electrostatic force

The technology of keeping two object intact using electrostatic force was developed long ago, but researchers from Fraunhofer EMFT, for the first time used the electrostatic force to handle thin wafer. The thin wafer was placed onto a mobile electrostatic carrier prepared on a silicon wafer and charged using a hand-held unit, which provides 200V DC voltage to initiate the electrostatic fixation [107]. The biggest advantage of this method is its ability to hold the thin wafer even at an elevated temperature (~400°C), which is not possible with most of the adhesive-based processes. Moreover, in the absence of any polymeric material, tools contamination is minimal and de-bonding can be achieved quickly by reversing the charging polarity.

2.5.2. Without carrier wafer

2.5.2.1. Using tape

Instead of using adhesive glue on a carrier wafer, adhesive tape stretched on a frame, alone can provide the provide mechanical to thin wafer. This technique is usually used by companies for shipment of thin and separated dies. For releasing the wafer from the tape, UV exposure, thermal treatment or appropriate solvent can be used.

2.5.2.2. Periphery ring

In cases where some process steps such as backside metallisation for electrode patterning, are needed, it becomes necessary to transport the thin wafer from one machine to another. The TAIKO process explained above is a better technique for the processes involving manual handling or clamp handling of thin wafer to perform intermediate steps.

2.6. Thin Wafer Dicing

In order to singulate the chips from the wafer, a diamond saw blade has traditionally been used. However, as the thickness of the wafer decreases, this technique poses serious challenges such as chipping of edges, die damage and delamination of adhesive layer. Due to low thickness and flexibility, even small force can cause the wafer to break, so to avoid disastrous damage, a non-contact dicing tools are preferred for singulating thin chip. Moreover, the techniques that allow for round corners on individual dies are desirable, in order to enhance the mechanical strength of dies. With so many rigorous requirements and challenges, several new thin wafer-dicing techniques have been developed.

2.6.1. Laser Dicing

This is a non-contact way of dicing using laser and can be modified to dice thin wafer using two types: (a) thermal stress generation-led dicing (b) stealth dicing. In the former, the laser is used as a volume heat source that generates a stress field which causes the wafer to crack. Whereas later, a defect is generated inside the volume of thin wafer by focusing the laser accurately below the surface. In the second step, the tape on which the wafer rests is expanded, and the chips are separated by propagating the stress layer created inside the wafer [108]. Nevertheless, the backside roughness and scratches originating during the thinning process, may change the direction of the stress propagation. This is the reason why full cut is considered better than stress induced dicing. The short pulsed laser beam can perform the full cut and are less complex and reliable than stealth dicing. The beam usually has pulse duration in the range of 10-100 ns and wavelength in the range of ~355 nm.

2.6.2. Dry Etching

This is also a non-contact method in which reactive species of plasma removes the material from the dicing line. This requires the remainder of the chip to be protected using the etch mask, preferably a resist which can be easily cleaned. Deep reactive ion etching could be used to separate the chips from the thin wafer, as it can provide very narrow and deep vertical trenches [109].

2.6.3. Blade Dicing

This is the least preferable technique, due to the high chances of chipping. However, if performed carefully, the thin wafer can be diced precisely using a blade dicing machine. It is generally advisable to dice thin wafers with an extremely fine-grit blade. Due to lower cutting power, they can be affected by deposited films, test element groups, and other elements present on the frontside of the wafer. DISCO has developed a system with a #4800 blade (much finer grit) which can dice wafers of thickness 25 μm.

2.7. Integration of ultra-thin chips

Like the conventional ICs, UTCs also need to be packaged to increase their reliability and lifespan. Although UTCs can be packaged on traditional rigid packages for preliminary electrical characterisation, flexible packages and substrates are required for their application in flexible electronics. The choice of substrate is critical and depends on the inherent material properties and the intended application. The materials which have been used as flexible

substrate can be broadly divided into two categories, i.e. polymeric and metallic. An insulation coating is generally needed on the backside of metallic substrate for electrical isolation of UTCs. However, there are some exceptions, such as solar cells where the required common back contact is achieved by transferring UTSi on flexible metallic or conductive-material-coated polymeric substrates [110]. The metallic substrates for flexible electronics have an added advantage as they can serve as a heat sink or means for thermal reliefs. Further, they can be useful in applications such as electrical waveguide or where electromagnetic shielding is required. This can also be achieved with polymeric substrates coated with a thin conductive material, including metals [111]. However, metallic substrates have inherent tendency towards retaining the shape on deformation, which may not be desirable. In this regard, thin polymeric substrates are advantageous, as they are inherently

Table 2.3: Comparison between various flexible substrates used for packaging UTCs

Material	**Max. process temperature [^{o}C]**	**Coeff. of thermal expansion [1/^{o}C]**	**Thermal Conductivity [W/m-K]**	**Young's Modulus [GPa]**	**RMS surface roughness [nm]**	**Ref.**
Stainless Steel [304]	1023	16	14	190-203	33.8	[112]
Molybdenum	760	5	140	315-343	85	[113]
Polyethylene terephthalate	140	39	0.15-0.4	2.0-2.7	1000-1500	[114]
Polyimide	360	30-40	0.46	2.5	2	[115]
PDMS	150	310	0.15	360-870 x 10^{-6}	0.88	[116, 117]
Parylene C	109	38	0.08	3.2	13 – 25	[118, 119]

Polyethylene naphthalate	155	20	0.15	5	0.64-0.68	[120, 121]
Collagen	70	--	0.60	5.0-11.5	100	[122, 123]
Silk Fibroin	100	-1060	--	2.8	11.92	[124-127]

elastic and flexible, with the ability to regain their normal shape. An alternative approach is to use a stack of both polymeric and metallic substrates and engineer the structure to realise smart substrates with desired properties. Thermal properties of substrates such as coefficient of thermal expansion and thermal conductivity should also be considered as they influence the integration and thermal management of UTCs. As the stress level in UTCs is influenced by the elastic properties of the substrate, generally a material with lower Young's Modulus is preferred. With the increasing interest in health or bio-related applications, such as implantable systems, bio-compatibility of substrate is also an important parameter to consider. Bacterial cellulose membrane, collagen, silicone gel, and silk fibroin have been used in such applications, as they also offer better integration with tissues [123, 128, 129]. A comparison of various flexible substrate used for UTCs is given in **Table 2.3**.The Integration of UTCs on flexible substrate has mainly been achieved by the following four techniques, examples of some of which are shown in Figure 2.21.

2.7.1. Flip Chip Assembly on Flexible Substrate

Bonding chip on flexible substrate, also called Chip-on-Flex, has been reported in [130] where thin silicon chips are obtained by back grinding and then assembled on polyimide or liquid crystal polymer (LCP) through flip chip assembly. In the case of polyimide substrate, the solder bumped die are reflow soldered to the patterned flex. In the case of LCP, vias are etched through to expose the underside of contact pads. Xao *et al*. [131] assembled a pressure sensor and an actuator on a flexible substrate using Flip Chip technology. Flip chip assembly allows reducing the substrate area, the package size and its weight. However, the reliability of these bumps is debated, as they show the typical coarsening of the solder during ageing and the

growth of the intermetallic compound, which results in a changing shear mode and increase in resistance [132].

2.7.2. Laminating UTC between two polymer layers

In this way of packaging, the thin chip lies at the neutral plane created between two layers of polymer. Thus, the major advantage of this technique is that it reduces the stress experienced by the thin chip to negligible level, compared with the Chip-On-Flex technique. A PI-based embedding technology for integrating very thin silicon chips in between two spin-on PI layers was developed by IMEC, and was termed as Ultra-Thin Chip Package (UTCP) [133].

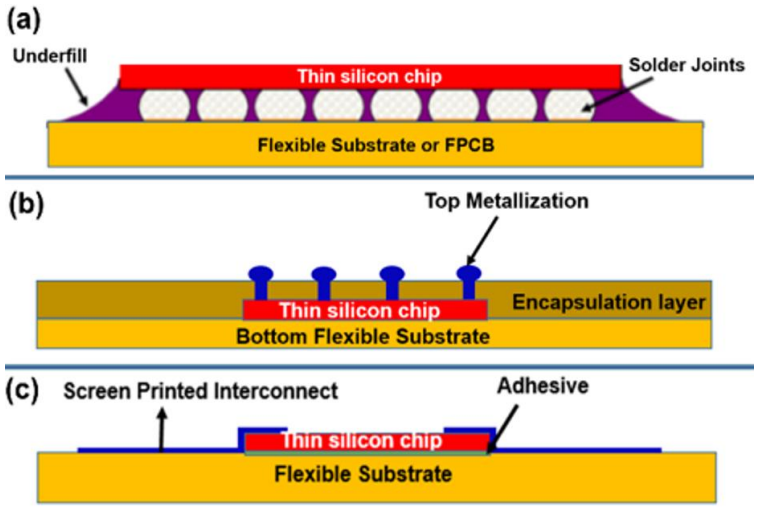


Figure 2.21: Major schemes of packaging UTC: (a) Flip-Chip packaging of UTC (b) UTC lamination between two flexible layers (c) UTC on flexible substrate with screen-printed connection. [134]

Sterken *et al.*[135] reported a conformable and wearable wireless ECG monitoring system using UTCP. However, once laminated between two layers, the heat produced in the device cannot escape to the atmosphere through direct conduction, resulting in spatial temperature increase. Higher temperature degrades the device performance and also reduces the package reliability. Under the localised area of high temperature, the adhesion between the polyimide and the silicon increases, resulting in uneven adhesion of package within the chip. Therefore, on-chip cooling and thermal management on flexible chip will be required in the near future when the complexity of the chip will match the current miniaturisation level. In this direction, Chowdhery *et al.*[136] proposed on-chip cooling by nanostructured super lattice-based thin-film thermoelectric and achieved ~14.9^{o}C decrease in temperature using Be_2Te_3 material. Similar advances can be made in UTC and its heterogeneous integration with nanomaterials to provide on-site cooling, thus increasing the package reliability.

2.7.3. Chip on Foil with printed connections

In this approach, UTCs are fixed in face-up configuration on the flexible substrate using epoxy-based adhesive. Thin wires are printed on the top of the flexible substrate with conductive ink in order to realise the electrical connection between the chip and the substrate. Screen printing or ink-jet printing is used to connect the contact pads on the chip to the connecting wires on the substrate. Although this technique is simple, the problem lies in the height levelling step and resolution of printing. The contact pads and wires realised through printing usually have lower resolution compared with that of the chip, so the connections on the substrate takes much greater area than the real chip. Silver-based conductive ink and polymer-based conductive material such as PEDOT:PSS has widely been used for printing the connections. California *et al*. [137], reported a highly durable connection system by combining screen printed silver grid with PEDOT:PSS, which can find good application in UTC packaging.

2.7.4. Heterogeneous Integration

For realising a thin film flexible electronics system through additive processes, materials other than crystalline silicon are also used, typically for large area flexible electronic devices where high speed performance is not a concern. Some examples are a-Si/Poly-Si, inkjet or transfer printed nanowires [138], PQT, solution processed organic/inorganic materials such as peri-xanthenoxanthene (PXX)[139], LISICON [140], pentacene [141], DNTT [142], copper hexadecafluorophthalocyanine (F16CuPc)[143], Poly (3,4-ethylenedioxythiophene) (PEDOT) [144] and thixotropy materials [145]. Some of the these materials are used as piezoresistive material for pressure or strain sensing and to realise various other sensors such as tactile sensors, light sensors [146]. In addition, the above materials can be heterogeneously integrated with UTC to implement a number of advanced microsystems. This kind of integration, where UTCs perform the high speed computing and other materials help in realising flexible system, will enhance the overall usability of the system.

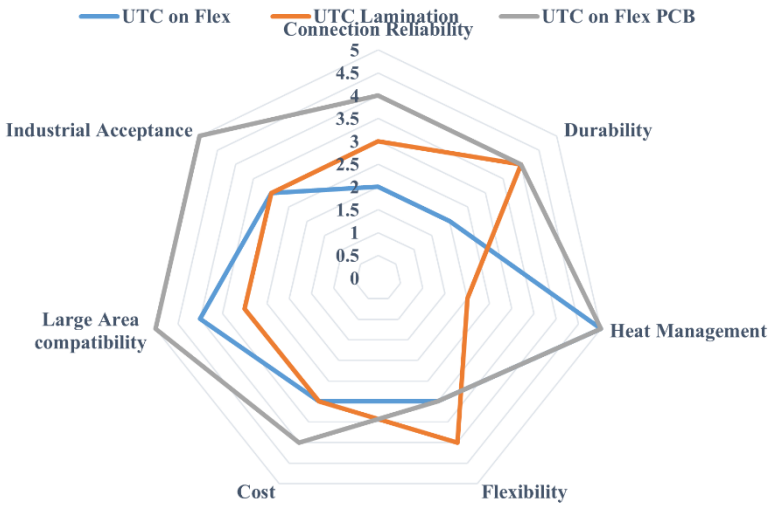


Figure 2.22: Radar chart showing comparison between major packaging schemes for UTCs.

2.8. Application of Ultra-Thin Chips

Various applications of flexible electronics where UTC technology could be utilised are shown in Figure 2.2. In addition to performance enhancement, such thinned chips find application in flexible electronics and could be useful in realising a number of applications such as flexible displays, flexible mobile phones, flexible FETs [147] and circuits, photovoltaics, E-skin for robotics, inventory scanners, energy harvesting, RF-ID antennas, smart food wrappers, health monitoring sensors/systems [148] and many more. Three important application areas of UTCs which are attracting significant attention, are presented:

2.8.1. 3D Integrated Circuits

With a vision of connecting every single object in the world to form one network, IoT is a fast-emerging area. Considering the huge number of objects, with different size, shape and rigidity, which are going to be connected, high performance and mechanical flexibility of these devices is inevitable. As discussed before, the wireless communication in IoT will require data handling in frequency bands up to ultra-high frequencies (0.3 – 3 GHz). The UTCs will be useful in this scenario, as they could support faster communication, high bandwidth, and efficient distributed computation with very high clock speed. Further, with interconnecting schemes such as through-silicon-vias, low power consumption and excellent

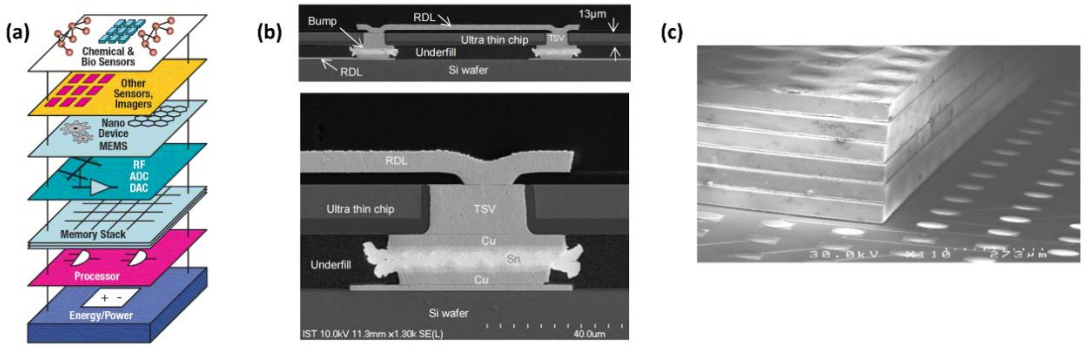


Figure 2.23: (a) Conceptual structure of UTC based 3D super-chip. [149] (b) Cross-sectioned microstructure of (top) a pair of TSV joints and (bottom) one TSV joint. [150] (c) Six ultra-thin silicon layers with TSV and thin silicon interconnections. [151]

performance, the UTCs have potential usage in 3D ICs to handle large amounts of data and processing in the IoT concept[152, 153]. 3D ICs is seen as the next generation semiconductor technology. It has many advantages such as low form factor (three to four times less than 2D System-on-Chip), low power consumption due to inter-chip routing, high-density integration by stacking UTCs over each other with billions of devices on one chip, and excellent performance due to innovative interconnection schemes [153] (some examples being shown in Figure 2.23). The International Technology Roadmap for Semiconductors (ITRS) for more-Moore concept of 3D ICs demands very thin chips in order to facilitate vertical integration [154]. For application of UTC in 3D ICs, ChipFilm technique is a very viable method as thin chips can be directly picked using a pick-n-place tool and stacked vertically. Likewise, the Ferroelectric Random Access Memory (FeRAM) based on flexible silicon shows superior performance and can be an ideal choice for flexible memory applications in IoT [155].

2.8.2. Medical/Life Healthcare

There have been outstanding progresses in the field of medical diagnoses and treatments, but care delivery had not changed much until the arrival of medical healthcare-based consumer electronics. Availability of gadgets having integrated sensors, processing and communication units is enabling patient-centric healthcare. High-performance and compact electronics with UTCs is needed to make many such gadgets wearable. UTC finds vast application in biological and medical arenas such as video endoscopy, smart catheters, diagnostic pills, sub-retinal implants, neural prosthetics and tactile functional prosthetics. A combination of flexible electronics, mechanised prosthetics and flexible tactile skin may create fully functional

prosthetics for amputees. The convergence of flexible electronics, and biology has huge potential for many exciting futuristic applications, such as brain-machine interfaces (BMI) to study or excite neurons, neuromorphic implantable biomedical system, swallowable smart pill [156].

Flexible RFICs using SOI wafers encapsulated with biocompatible liquid crystal polymers have been successfully implanted and tested *in vivo* in a mouse by Hwang *et al.* [91]. Zrenner *et al.* [157] have shown that sub-retinal micro photodiodes array can successfully replace degenerated photoreceptors. There are several reports of implantable devices in literature where thin silicon-based devices on flexible substrate are implanted on tissues (some examples being shown in Figure 2.24) for health monitoring. The above reports of products and prototypes clearly substantiate the role of UTC in the area of medical science, which, on further advancement and integration, may lead to a fully flexible human health care monitoring system.

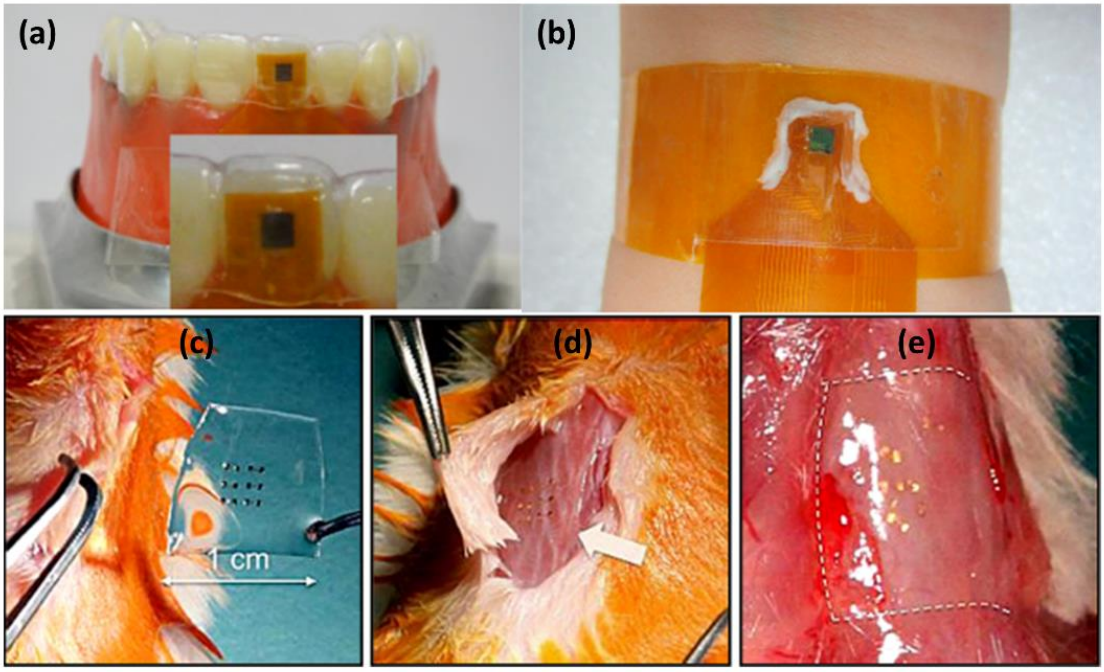


Figure 2.24: Ultra-thin silicon chip (a) for orthodontic force measurement of invisible aligners (b) for measuring pulse on wrist. [158] Image of procedure and result of the animal toxicity test (c) before, (d) shortly after, and (e) two weeks after implantation silicon electronics on silk. [159]

2.8.3. Robotics

Robotic devices, which were earlier limited to the industrial environments, are now entering human's daily life in many ways. With a new generation robots designed to physically interact with humans and real-world objects, there is a need of covering these robots with touch sensory skin, in order to enable safe interaction. Sensors and electronics distributed on flexible and conformable substrates are essential for this purpose and as the number of sensory components increases, there is demand to handle large data. The on-site processing and signal conditioning of the raw data can be fulfilled by integrating these sensors with UTC. Likewise, for faster reaction, robots need faster sensory feedback and UTCs could serve the purpose. Several solid-state touch sensory schemes reported in literature could benefit from the UTC technology. Many large area tactile skin based on planar off-the-shelf electronics integrated on flexible printed circuit boards have been reported [160], where a lack of bendability in electronics has been highlighted as the common reason for their limited use. UTCs will address these issues and advance existing solutions for robotic tactile sensing. The energy requirement of skin can also be met by integration of flexible photovoltaics over the e-skin [161, 162].

2.8.4. Large Area Electronics

The essence of large area electronics lies in its application in displays, lightings, energy harvesting and sensor networks. Displays and lightings are available in a wide range of sizes, from a 1-inch smart watch screen to a 100-inch LCD displays. Currently, there are reports of success in terms of flexible display and back panel drive electronics, while the high performance computing parts is still rigid. For introducing high density computing/electronic driving nodes on these large area electronic systems, UTC technology is promising and can be used to make these systems fully flexible. Further, for special display applications, the drive electronics could be made using UTC which will result in a highly power-efficient display system. Flexible large area electronics also finds its application in the area of electronic skin for prosthetics. A conformable electronic tactile skin with high speed feedback system, on a robot's body, enabled by the ultra-thin silicon-based sensor and circuit, will allow safe interaction of the robot with various objects and humans.

Photovoltaics is another important application area of large area electronics where thin inorganic semiconductors have a significant advantage and could be used effectively to

minimise the material usage and at the same time achieve higher efficiency by using approaches such as lambertian trapping and tandem structures [103, 163].

2.9. Case Study: Ultra-thin silicon based tactile sensors

One of the essential features which allow humans to interact with surroundings is “sense of touch” which allows assessing object properties, such as shape, size, texture, and temperature. This sense of touch, also termed as tactile sensing, fills the gap between what is sensed and what is perceived. These sensors are of specific interest, and in fact, an integral part of envisaged electronic-skin for robotics and prosthesis. To mimic the sense of touch in humans, e-skin is required to have flexible and conformable tactile sensors with density and spatial distribution depending on the targeted body site. Notably, the tactile sensors for fingertips require a large number of taxels (tactile elements) in a small region (~ 1 mm spatial resolution) and fast response [164].

In the last three decades, the need to improve the touch sensing capability of sensors has resulted in many types of touch sensors based on a different kind of transduction mechanism such as capacitive, piezoelectric, piezoresistive, and optical.

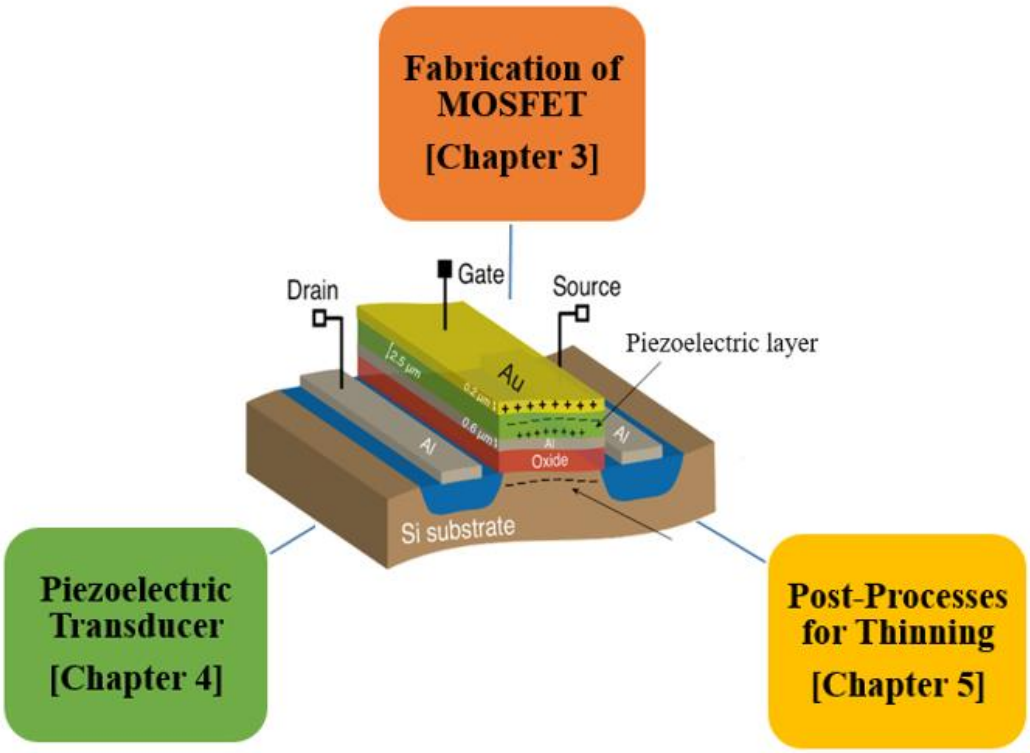


Figure 2.25: Radial cluster showing the major areas of work presented in the thesis.

One interesting approach to realise tactile sensor is the integration of the transistor with any transducer material. This kind of approach allows integration of the sensing layer and active devices on the same substrate and therefore opens up possibilities of performing the signal processing very close to the sensors. The piezoelectric transducer layer can either be connected in an extended gate configuration away from the FET or coupled directly over the gate area of FET. Both of these approaches have their advantages and disadvantages, and depending upon the conditions, either of these is used. Organic semiconductor-based FETs and their circuits have attracted considerable attention, as they can be manufactured on plastic films at low temperature, which make them inherently flexible and potentially low in cost. The major drawback in using OFETs in tactile sensing is their low spatial resolution and low carrier mobility ranging between 1-2 cm^2/V-s, which leads to slow response [165]. On the other hand, silicon-based FETs provides high-speed response and high spatial resolution due to the matured technology. However, due to the rigid nature of the silicon, they cannot be used on the curved surface. Nevertheless, with the advent of thin silicon, if the sensing chip thickness is reduced to the ultra-thin domain, this limitation can be lifted. The bendable silicon based tactile sensors can be integrated conformably to the flexible substrate of e-skin. Therefore, this thesis focusses on the development of sensing devices where the MOSFET is used as an active device and the piezoelectric layer is transducer layer. Since, MOSFET has been fabricated using standard technology over rigid 6 inch wafer, the methods to thin the silicon are also developed.
The subsequent chapters, which are 3, 4, and 5 presents the work done to fabricate MOSFET, piezoelectric transducer and thinning processes respectively, as illustrated in Figure 2.25.
Although, the presented work emphasis on tactile sensors, the developed technology can be used for realising any bendable silicon-based system such as driving and processing units of fully-flexible display.

2.10. Conclusion

This chapter has presented and compared the ways to make bendable Si and variations in the response of devices on UTCs due to changes in electrical, optical and mechanical behaviour. Tremendous progress has been made for obtaining UTCs and a range of thinning methods used for this purpose has been compared in this chapter.

The major hurdles for UTCs will be in the areas related to packaging, modelling and dealing with the effect of stress and strain on electrical response of UTCs. The handling of thin fragile wafers and packaging of UTCs needs more attention. Unlike conventional chips, UTCs cannot

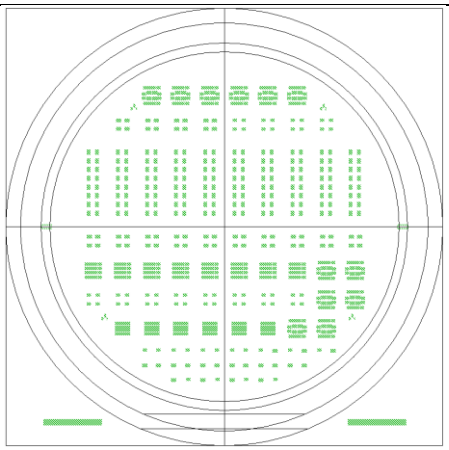
be diced and bonded easily with blade dicing and wire-bonder respectively. Reliable and durable connection from chip to the substrate is a challenging task due to the bumps coarsening (in the case of flip-chip bonding) and the possibility of electrical discontinuity (in the case of screen-printing). With suitable thermal management and embedding the chip between two layers of pre-patterned electrical connection, it is possible to overcome the bonding related issues. The cost of fabrication of UTCs is also argued as an area that requires attention, especially when they are realised from a SOI wafer. However, with mass manufacturing of UTCs the costs will further come down and this is likely to be a non-issue. In conclusion, despite many challenges, the UTCs holds a great promise for advances in many areas where high-performance flexible or conformable electronics are needed.

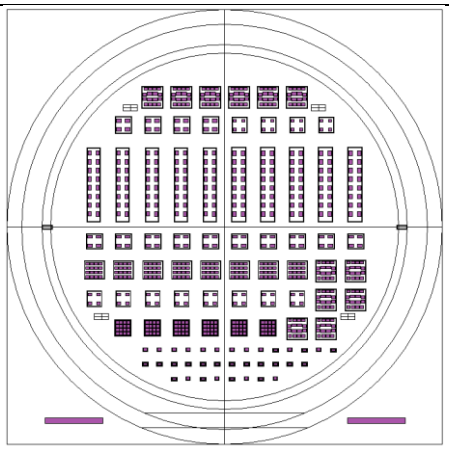
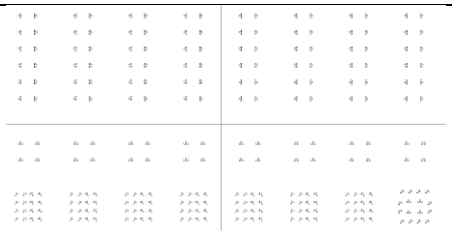
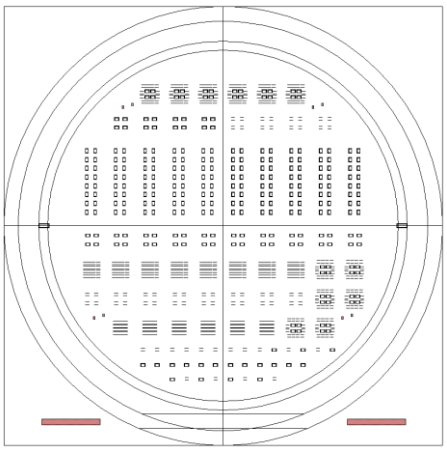
Chapter 3. Fabrication of MOSFET as an Active Device of Tactile Sensor

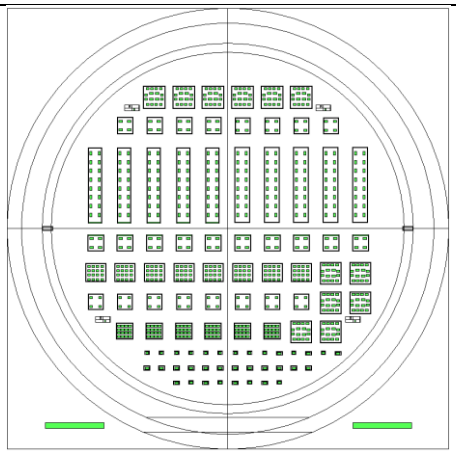
In this chapter, the step-by-step process followed for the fabrication of the MOSFET devices has been presented, which was later used as active device for tactile sensor in combination with piezoelectric transducer material. The fabrication run was carried out at Fondazione Bruno Kessler, Italy. Prior to the fabrication, full design rules set was implemented and the process was designed to comply with the installed change from 4 inch wafer to 6 inch wafer. The masks were designed in L-Edit and fabricated at Photronics Inc. The chapter first presents the designed mask set and then the key fabrication step. Wherever required, the cross-sectional illustration and doping profile simulation is also provided.

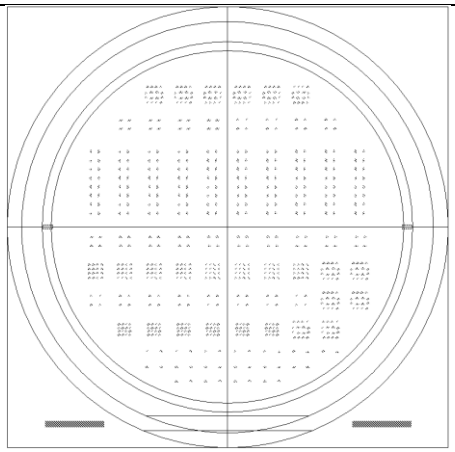
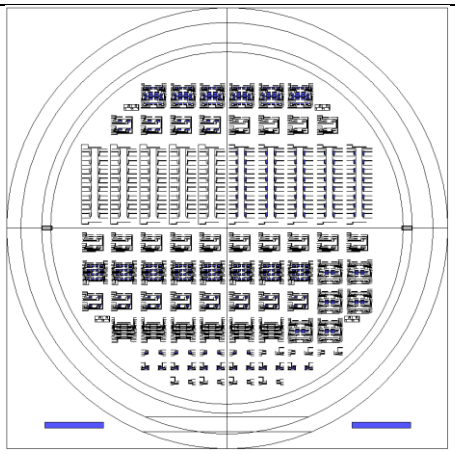
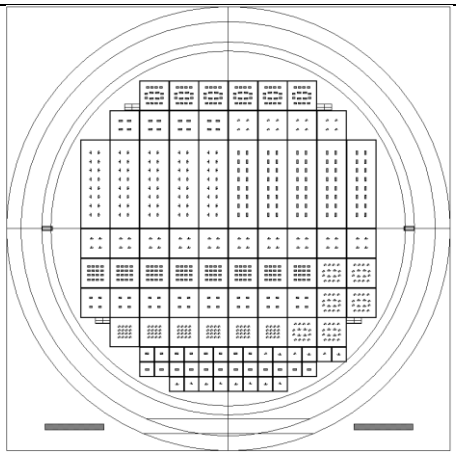
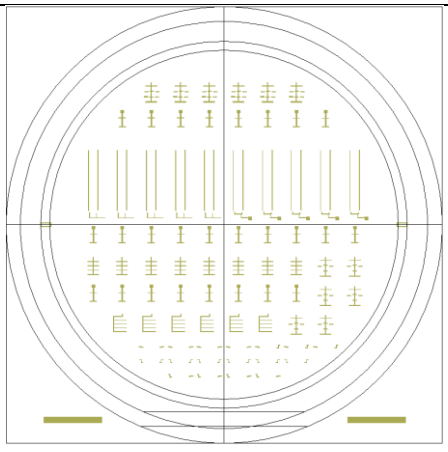
3.1.1. Mask Design

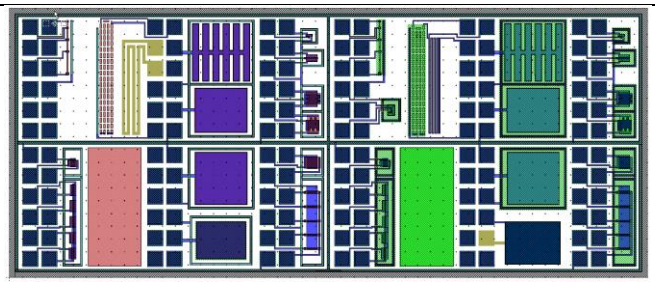
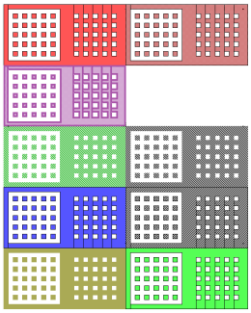
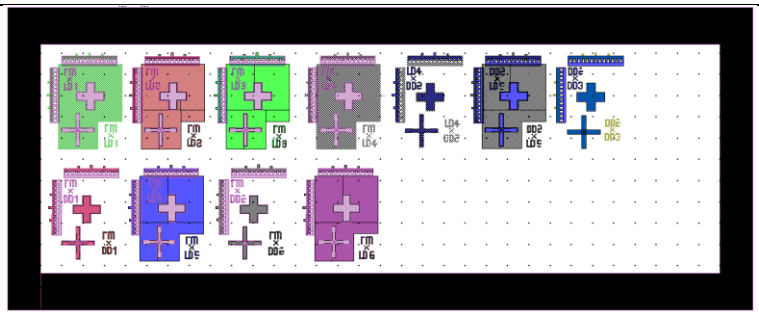
Masks for lithography were designed in L-Edit using IRST ISFET/CMOS4 technology. A total of 9 masks were designed out of which 6 were dark field (light data) and 3 were light field (dark data). The critical dimension was kept at 4 μm and a set of alignment markers was developed to meet the requirements of fabrication. The mask set and other important parts of the design are summarised below:

No	Mask	Layout	Type	Process
1	P-Well		Dark field Aligned over Mask 0	Implantation

2	Active Area		Dark field Aligned over Mask 0	Implantation
3	Poly		Light field Aligned over Mask 0	Deposition
4	P-Plus		Dark field Aligned over Mask 0	Implantation

5	N-Plus		Dark field Aligned over Mask 0	Implantation

6	Contact hole		Dark field Aligned over Mask 0	Etching
7	Metal1		Light field Aligned over Contact Hole	Deposition
8	Glass		Dark field Aligned over Metal1	Deposition
9	Gold		Light field Aligned over Metal1	Deposition

10	Test Strip	
11	CDs	
12	Alignment Markers	

3.1.1.1. Critical Dimension Check

When fabricating a device, the smallest dimension on a lithography level that must be accurately controlled to optimise electrical performance is called critical dimension. In the designed process, it was 4 μm and so a special design consisting of etching and deposition window of dimension 4 μm x 4 μm in every mask layer was placed at the edges of the wafer.

3.1.1.2. Alignment markers

In order to make working devices, the patterns for different lithography steps that belong to a single mask/layer must be aligned to one another. The first pattern transferred to a wafer usually includes a set of alignment marks which are etched in the wafer. These are high precision features that are used as the reference when positioning subsequent patterns, and usually remain the same for most of the fabrication run. Since these first markers may be obliterated as processing progresses, the next masks have their markers which can be used as reference for other mask plate.

3.1.1.3. Test Strip

Two test strips are included at the edges of each wafer. These were designed to monitor the process variation and sheet resistivity measurement.

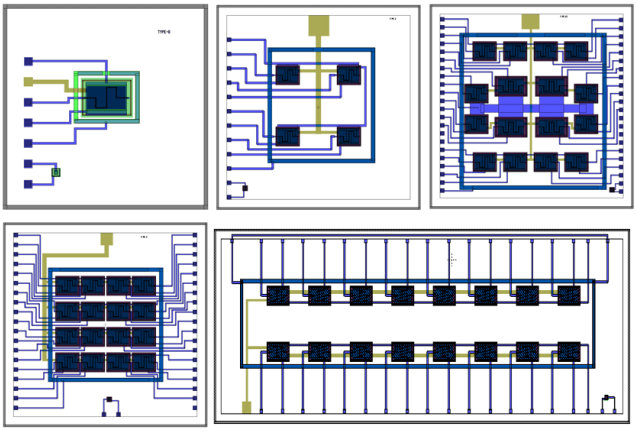


Figure 3.26: Layout design of different arrangements of POSFET devices. These chips are designed for specific target areas, such as the 4x4 array is for fingertip where high resolution is needed, whereas, 8x2 array is designed for palm area where the large area covering with low resolution is needed.

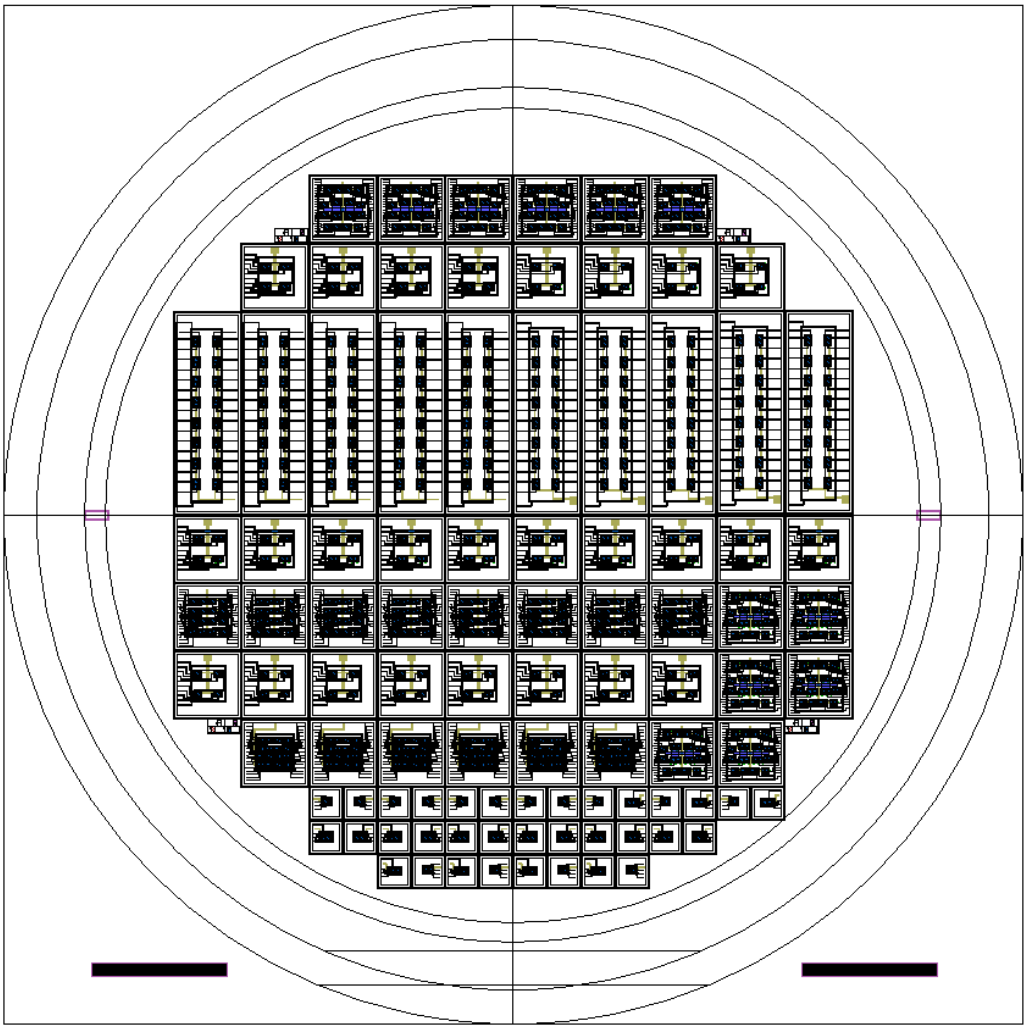


Figure 3.27: Final layout of wafer consisting various arrangements. Total 96 chips are included in the wafer layout and extra area was left for defining the backside etching window. Two teststrips were also included in the design to monitor the key steps.

3.2. Fabrication Steps

15 n-type, (100), double-sided polished, prime grade wafers with resistivity of 1-20 Ω-cm were procured from University Wafers. In total, 125 steps were carried out to fabricate the MOSFETs. The whole process has been summarised in 76 key steps by merging common or repetitive steps. The cross-sectional illustration is also provided for steps involving the additive, subtractive or lithography process. The doping profile was simulated in SILVACO using the process parameters and the dopant profiles are included wherever required.

Step-1: RCA cleaning

RCA cleaning is named after Radio Corporation of America, where, in 1965, Werner Kwern developed the procedure, which has now become an industry standard for removing the contaminant from the wafer. The RCA clean is a must when the wafer has to go through high temperature processing in a shared furnace, since any kind of contamination may affect the next batch.

The cleaning was divided into two parts: RCA-I and RCA-II. In RCA-I, wafers were cleaned by sequential desorption and complexing with H_2O_2-NH_4OH-H_2O, and this removed organic residues. RCA –II was developed for removing metal ions and achieved using H_2O_2-HCl-H_2O. During this process, a thin layer of oxide was produced on the surface, which needs to be removed if a pure silicon surface is required. This process was repeated before any step involving tube furnace.

Figure 3.28: Cross-sectional illustration of n-type double-sided polished wafer.

Step-2: SiO_2 deposition

Silicon dioxide (SiO_2) was deposited using Tetraethyl orthosilicate (TEOS). TEOS is a chemical compound with the formula $Si(OC_2H_5)_4$ and has a tetrahedral structure. It was used as precursor since it easily converts to SiO_2 upon the addition of water and produces ethanol as by-product:

$$Si(OC_2H_5)_4 + 2\ H_2O \rightarrow SiO_2 + 4\ C_2H_5OH \qquad (3.1)$$

It can also be converted in SiO_2 by heating at an elevated temperature, where the molecule breaks into SiO_2 and volatile diethyl ether.

$$Si(OC_2H_5)_4 \rightarrow SiO_2 + 2\,(C_2H_5)_2O \quad (3.2)$$

The TEOS molecule was transported to the hot surface of the wafer using carrier gas, where it results in deposition of SiO_2 after a series of complex pyro electric reactions. In the process, 1200 nm thick SiO_2 was deposited on both sides of the wafer using a CENTROTHERM tube furnace.

Step-3: SiO_2 etching

The SiO_2 deposited on the frontside in the previous step was removed using the dry etching technique. The equipment used for this purpose was Tegal 903 and the CF_4 etch chemistry was employed. This led to a clean front surface but oxide-covered back surface, which was later used as one of the layers for the wet etching mask.

Step-5: Screen oxide growth

Screen oxide is an example of one of the many sacrificial layers used in device fabrication. It does not have any direct role to play and is discarded after use. It is basically a thin layer of SiO_2 whose function is to screen, i.e. protect, the silicon. Screen oxide stops the low energy debris, such as metal ions, stray ions, carbon ions, coming with the high energy ion beam during implantation. It also helps in scattering of the ion beam, to some extent, and prevents channelling of ions deep into the crystal. Dry thermal oxidation at 975^{o}C for 36 minutes was carried out to grow 20 nm thick screen oxide on the front surface of the wafer.

Step-6: Lithography 1

Wafers were cleaned sequentially in acetone, IPA and DI water. HDMS was spin coated as primer, with a speed of 4800 rpm for 20 seconds, and baked at 150^{o}C for 35 seconds. HiPR612, a positive photoresist, was spin coated with a speed of 4800 rpm and baked at 90^{o}C for 60 seconds. Lithography was performed using Mask 0, which was standard mask for the first alignment markers. An exposure of 6.5 seconds using KARL SUSS MA150 was performed and developed in OPD 4262 for 50 seconds. This was followed by hard bake at 150^{o}C for 1 minute on a hot plate and at 120^{o}C for 1 hour in a convection oven. After development, the silicon below the patterned area was exposed for etching.

Figure 3.29: Cross-sectional illustration of lithography performed to do first marker etching.

Step-7: Markers etching

The first alignment markers were necessary to align the subsequent mask plate. Following the lithography step, the exposed silicon was etched using Deep Reactive Ion Etching using SF_6 chemistry.

Step-8: Plasma ashing

Plasma ashing of photoresist following etching and ion implantation is one of the important and frequently performed steps in semiconductor fabrication. The ashing process uses ions and radicals generated by a plasma to remove the resist. While the ions physically remove the photoresist, radicals chemically react with the photoresist surface to create volatile molecules such as H_2O and CO_2. The combination of these two mechanisms is the key behind plasma ashing. Tepla asher with oxygen plasma for 30 minutes was used for this purpose.

Step-9: Screen oxide removal

The screen oxide deposited in step 5 and patterned in step 6 was removed using the dry etching technique with CF_4 +SF_6+He chemistry at 1800 mtorr, 500W in Tegal 903.

Step-10: Screen oxide growth

20 nm thick screen oxide was grown on the frontside of wafer at 975^{o}C in 36 minutes using a Centrotherm tube furnace.

Step-11: Lithography 2

Standard lithography steps were executed, as explained previously using HiPR612 resist. Lithography was performed using Mask P-Well, which was designed for defining the p-well area. After development, the silicon below the patterned resist was exposed for implantation.

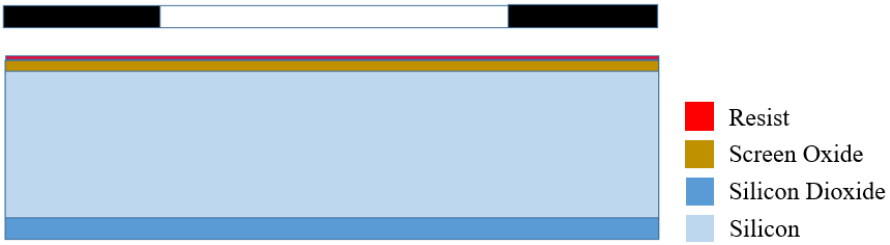


Figure 3.30: Cross-sectional illustration of lithography performed to do p-well implant.

Step-12: Implant Boron

In order to create p-well, i.e. a region in the substrate with an excess of holes, the wafer was implanted with a p-type dopant, boron. BF_3 (boron triflouride) source was used to generate B11 ions with energy 100 keV, dose of $6.5x10^{12}$ atoms/cm^2 and tilt of 7 degrees. The implantation was performed using Varian Extrion 200. The SILVACO simulation for doping concentration immediately after implantation shows the typical Gaussian distribution and can be seen in Figure 3.31.

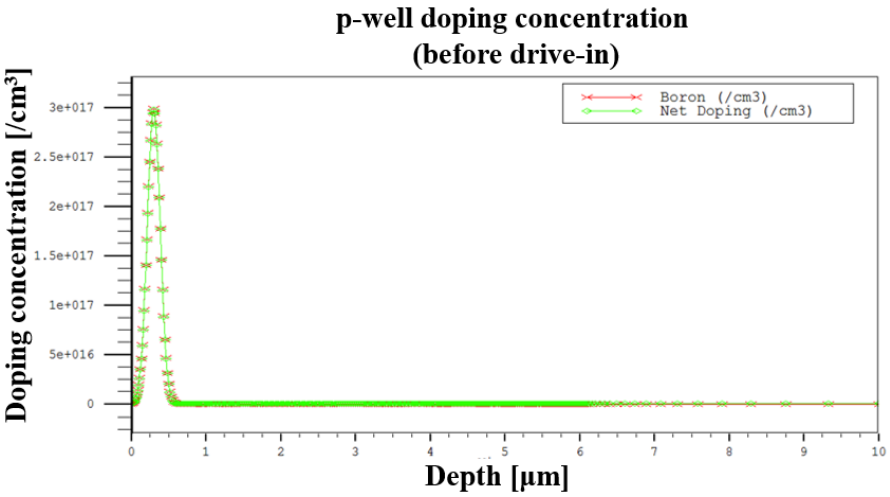


Figure 3.31: Simulated profile of doping concentration immediately after boron implant. Simulation has been done using SILVACO and the plot shows the depth in silicon at which the concentration is highest, which is also characterised as junction depth immediately after implant.

Step-13: Well drive-in

Immediately after the implantation, dopants are concentrated in the top few hundred nanometres of silicon. In order to conduct profile control, decide junction depth and dopant concentration, a drive-in was performed. Well drive-in is a process in which the wafer was heated in a nitrogen atmosphere, during which the dopants move further down the substrate in Gaussian distribution. The concentration at the surface also plays a role in deciding the threshold voltage of the devices. Well drive-in was carried

in furnace's Tube 3 with 1 hour soak time in N_2 ambient at 975 °C, then 15 hours in dry oxygen ambient at 1050°C and finally in nitrogen ambient for 8 hours at 1050°C. The simulated dopant profile after the drive-in is shown in **Figure 3.32**

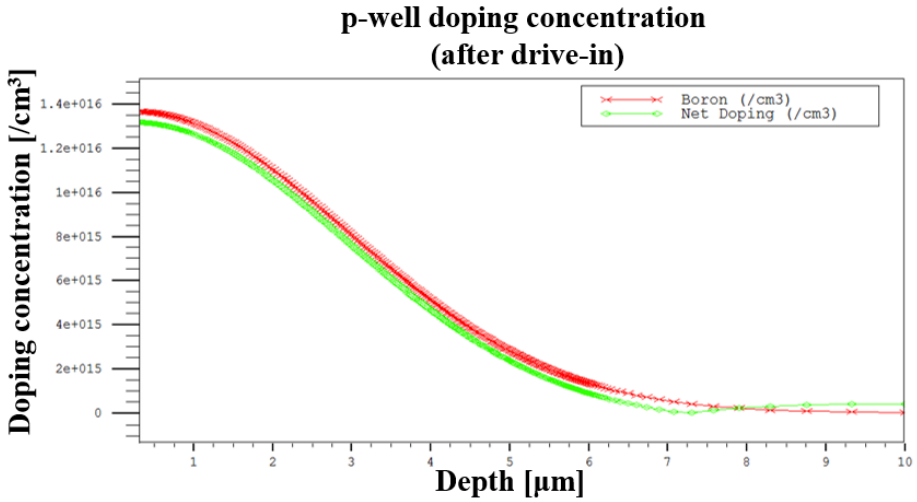


Figure 3.32: Simulated profile of doping concentration after well drive-in. Simulation has been done using SILVACO and the plot shows the depth how the dopant concentration adopts Gaussian distribution form after the drive-in step.

Step-14: Screen oxide removal

The screen oxide used for boron implantation and drive-in was dry etched using CF_4 +SF_6+He chemistry at 1800 mtorr, 500W in Tegal 903.

Step-15: Screen oxide growth

20 nm thick screen oxide was grown on the frontside of wafer at 975°C in 36 minutes.

Step-16: Lithography 3

Wafers were cleaned sequentially in acetone, IPA and DI water. Primer was spin coated at 3000 rpm for 30 seconds and baked at 150°C for MaN-1420 (negative resist) was spin coated with speed of 1500 rpm and baked at 1150°C for 2 minutes. Lithography was performed using Mask P-Well which was designed for defining the p-well area, but due to negative resist, it was used for defining well-stop region. An exposure of 6 seconds in development for 2 minutes in developer was done before the hard bake at 150°C. After development, the silicon below the patterned resist was exposed for implantation.

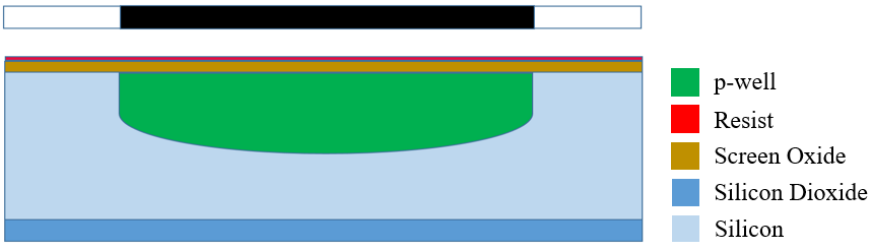


Figure 3.33: Cross-sectional illustration of lithography performed to do well stop implant.

Step-17: Phosphorus implantation

In order to control the lateral diffusion of p-well during subsequent heating steps, a p-well stop implant was performed using phosphorus with dose $5x10^{15}$ atoms/cm^2 and energy 80 keV with tilt of 7 degrees. This n-type implant also acts as well isolation and prevents any cross-talk between nearby wells.

Step-18: Screen oxide removal

The screen oxide used for phosphorus implantation was dry etched using CF_4 chemistry in Tegal 903.

Step-19: Pad oxide growth

50 nm thick pad or buffer oxide was thermally grown on the front side of the wafer in dry oxygen ambient at 975^{o}C in 110 minutes using Tube 3. Pad oxide acts as a stress-relief layer between the silicon beneath and the nitride layer above the pad oxide.

Step-20: LPCVD Nitride deposition

100 nm thick silicon nitride was deposited by Low Pressure Chemical Vapour Deposition (LPCVD) in Tube 6. Since thermally grown SiO_2 layers are under compressive stress and Si_3N_4 layers are under tensile stress, they partially compensate for each other reducing stress on the substrate. PECVD is a chemical reactive taking place at the surface of the surface without any involvement from the substrate atoms. The reactants which are widely used for nitride deposition are dichlorosilane and ammonia as a source for silicon and nitrogen respectively. These two react at high temperature (700^{o}C-850^{o}C) to form silicon nitride with hydrogen chloride and hydrogen as by-product gases.

$$3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2 \qquad (3.3)$$

Step-21: SiO_2 deposition

600 nm thick SiO_2 was deposited using TEOS on both sides of the wafer in Tube 5. At this stage the backside had stack of oxide-nitride-oxide which was used as etch mask for bulk etching of silicon from the backside.

Step-22: Frontside oxide etching

The SiO_2 on the backside was protected using 2.1 μm thick resist and the oxide on the frontside was etched using buffered oxide etchant.

Step-23: Lithography 4

Standard lithography steps were executed, as explained previously, using HiPR612 resist. Lithography was performed using Mask Active Area, which was designed for defining the area of interest, which was p-well and n+ region. After development, the stack of pad oxide and nitride was exposed for etching.

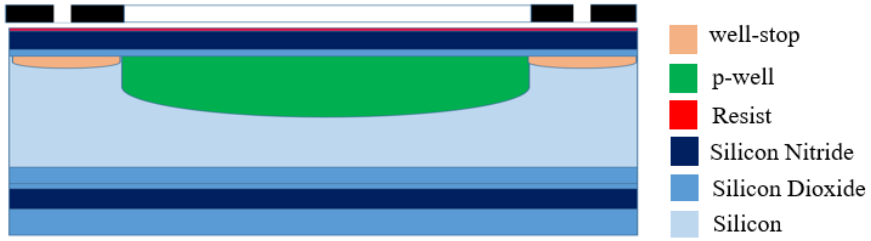


Figure 3.34: Cross-sectional illustration of lithography performed to define active area.

Step-24: Pad oxide and nitride etch

The stack was patterned by dry etching in Tegal 903, to define area of field oxide growth.

Step-25: Field oxide (FOX) growth

FOX is much thicker than the gate oxide and acts as a shield for protecting the underlying substrate from impurities when other processes are being carried out on the wafer. Besides, it also aids in isolation by preventing conduction between unrelated transistor source/drains. Since FOX was relatively thicker (1000 nm) and the electrical and chemical properties of the film are not critical, it was grown using wet oxidation of silicon in Tube 3 and it took 9 hours at 975°C. During wet oxidation, the following reaction takes place between silicon and pressurised water vapour:

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \qquad (3.4)$$

Step-26: Nitride etching

The silicon nitride was stripped in hot phosphoric acid using the wet etching technique.

Step-27: Backside protection and pad oxide stripping

Before etching the pad oxide, it was important to protect the oxide on the backside, so 2.1 μm thick resist was coated and hard baked. Thereafter, buffered oxide etchant was used to remove the pad oxide from the front.

Step-28: Screen oxide growth

40 nm thick screen oxide was grown on the frontside of the wafer at 975^{o}C in 80 minutes.

Step-29: Threshold adjustment implantation

Threshold adjustment is performed implanting a fixed, but relatively small and precisely controlled number of charges to shift the threshold voltage. Implantation of boron causes a positive shift in threshold voltage, whereas implantation of phosphorus causes a negative shift. From the study of previous runs, it was found out that when gate oxide is 50 nm thick, in presence of oxide charges, threshold voltage always remains below 0.7 and in order to increase the voltage, boron was implanted in the channel region. Wafers were separated into three lots and received three different doses of boron (B11). S1-S3 received $3x10^{11}$ atoms/cm^2, S4-S7 received $5x10^{11}$ atoms/cm^2 and S8-S11 received $6x10^{11}$ atoms/cm^2, all with energy 30 keV and tilt of 7^{o}.

Step-30: Backside protection and screen oxide stripping

Before etching the pad oxide, it was important to protect the oxide on the backside, so 2.1 μm thick resist was coated and hard baked. Thereafter, buffered oxide etchant was used to remove the screen oxide from front.

Step-31: Gate oxide growth

High quality 50 nm thick gate oxide was grown over the silicon surface in dry oxygen ambient at 950^{o}C in Tube 3. The thickness and quality of this oxide film has a major effect on transistor performance and reliability, and thus it must be a thin, high-density, defect-free film with a uniform distribution. The oxide capacitance per unit area, which is defined as ε_{ox}/t_{ox}, not only

directly affects the drain current but also decides various parasitic capacitances of any transistor.

Step-32: Polysilicon deposition

Polysilicon deposition was achieved by thermally decomposing silane, SiH_4, inside a low-pressure reactor at a temperature of 580 to 650^oC. This pyrolysis process involves the following basic reaction:

$$SiH_4 \rightarrow Si + 2H_2 \quad (3.5)$$

In this process, 450 nm thick polysilicon was deposited on both side of the wafer at 620 ^oC in Tube 7, and used as gate electrode material for MOS devices.

Step-33: Polysilicon removal from backside

The unwanted polysilicon on backside was dry etched in Tegal 6510 using fluorine based chemistry.

Step-34: Lithography 5

Standard lithography steps were executed, as explained previously, using HiPR612 resist. Lithography was performed using Mask Poly, which was designed for defining the MOSFET gate area, i.e. channel length and width. After development, the stack of unmasked area of polysilicon and gate oxide was exposed for etching.

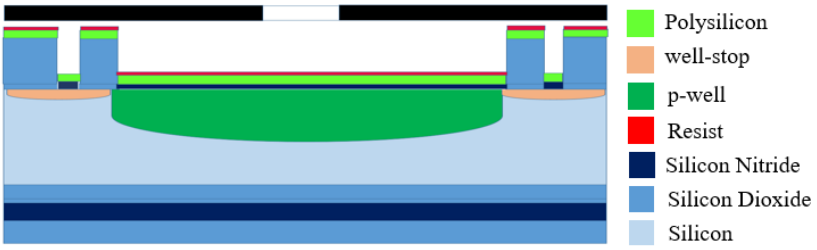


Figure 3.35: Cross-sectional illustration of lithography performed to define the gate area of MOSFET.

Step-35: Polysilicon etching

The patterned polysilicon was dry etched in Tegal 6510 using fluorine based chemistry, leaving it just above the gate oxide.

Step-36: Lithography 6

Standard lithography steps were executed, as explained previously, using HiPR612 resist. Lithography was performed using Mask P-Plus, which was designed for defining the highly

doped area in p-well for creating well contact. After development, screen oxide was exposed for the implantation.

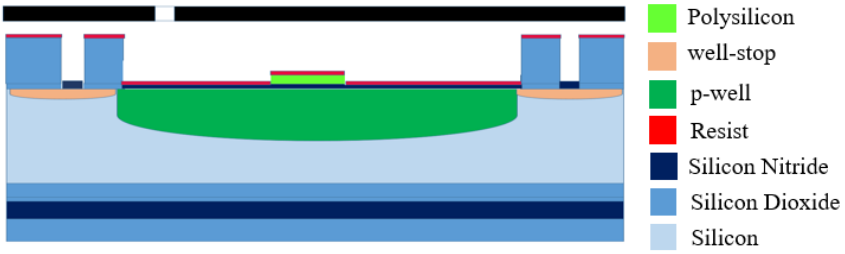


Figure 3.36: Cross-sectional illustration of lithography performed to define the well contact region.

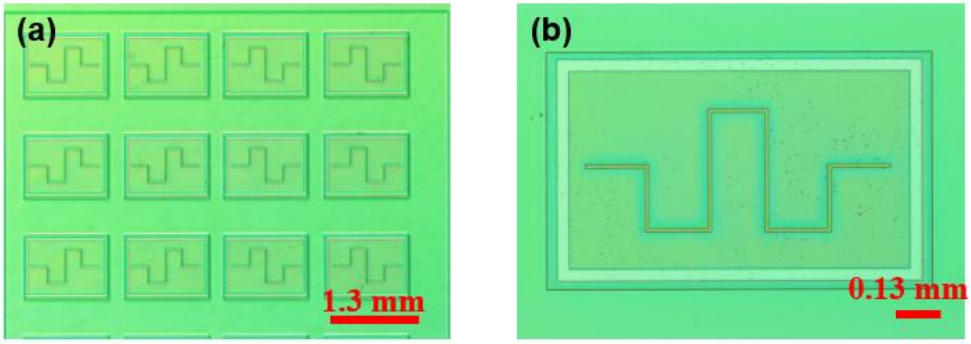


Figure 3.37: Optical image of device after P-plus lithography. The image on left shows part of chip consisting an array of 3x4 and the image on right shows a single device with serpentine shape gate.

Step-37: Boron implantation

BF_2 was chosen as boron source for p+ ions for realising body connection to p-well. The heavy BF_2 dopant gives a shallow but highly conductive profile. The dose of $5x10^{15}$ atoms/cm^2 was given with energy of 80 keV and tilt of 7 degrees in Varian Extrion 200.

Step-38: Lithography 7

Standard lithography steps were executed, as explained previously, using HiPR612 resist. Lithography was performed using Mask N-Plus, which was designed for defining the source/drain and substrate contact region. After development, screen oxide was exposed for the implantation.

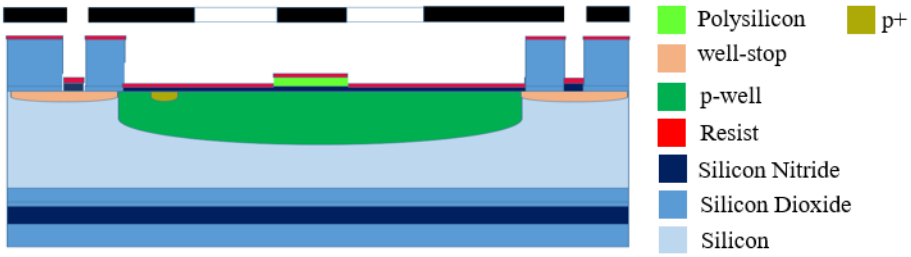


Figure 3.38: Cross-sectional illustration of lithography performed to define source, drain and substrate contact region.

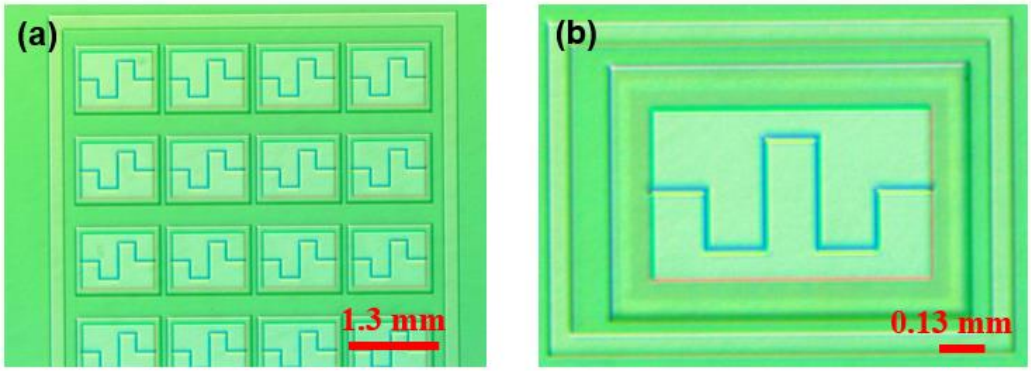


Figure 3.39: Optical image of device after N-plus lithography. (a) shows the image of a 4x4 array and (b) shows a single cell.

Step-39: Phosphorus and arsenic implantation

Source and drain of NMOS was implanted in two steps: firstly, phosphorus was implanted with dose $5x10^{15}$ atoms/cm^2 and energy 80 keV, followed by arsenic with dose $2x10^{15}$ atoms/cm^2 and energy 120 keV. The arsenic, with its lower diffusion coefficient, tends to concentrate near the top surface of the n-wells, with the phosphorus penetrating sufficiently to define the n-wells at the desired depth. Since the implantation was performed after the gate realisation, it was a self-aligned process.

Step-40: Back side protection and gate oxide etching

Before etching the gate oxide from unwanted area, it was important to protect the oxide on the backside, so 2.1 µm thick resist was coated and hard baked. Thereafter, buffered oxide etchant was used to remove the oxide from front, with polysilicon acting as a masking agent.

Step-41: SiO_2 deposition

300 nm thick SiO_2 was deposited on both sides of the wafer using TEOS in Tube 5. This was done before the diode drive-in process in order that the dopant profile did not disturb in case

of any possible thermal oxidation. The already present oxide on the silicon surface prohibits any surface oxidation and thus during the drive-in process, the dopant moves down in the substrate.

Step-42: Diode drive-in

After the implantation, the doping species remained near the surface with high density. A drive-in was performed in nitrogen ambient for 2 hours at 975^{o}C. The simulated doping profile after this drive-in is shown in Figure 3.40.

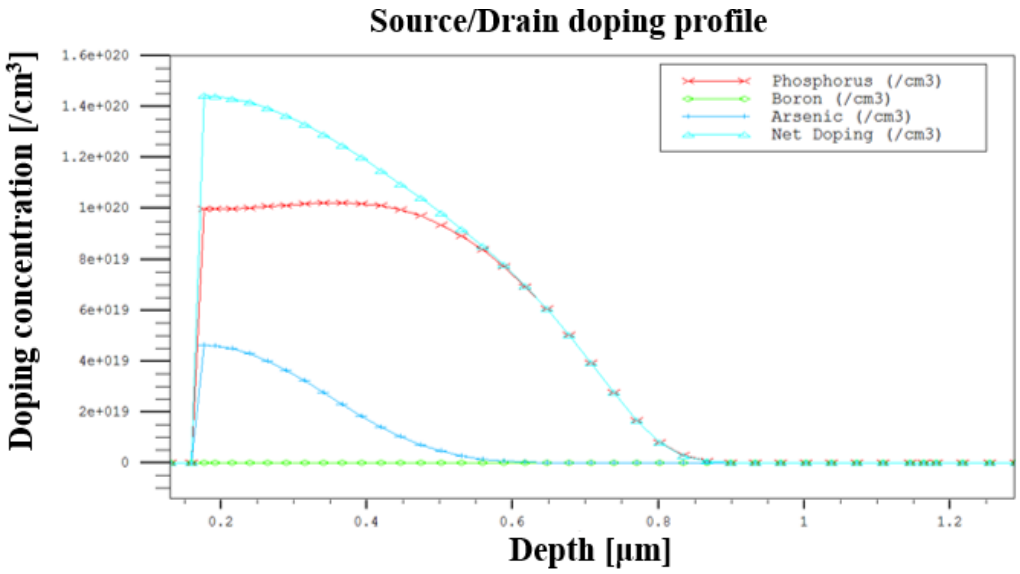


Figure 3.40: Simulated profile of doping concentration after dopant drive-in. Simulation has been done using SILVACO and the plots shows the depth in silicon at which the doping concentration of phosphorus, arsenic and net doping becomes equal to the intrinsic doping concentration. This depth is called the junction depth of source/drain implant after drive-in and that is around 0.9 µm.

Step-43: Lithography 8

Standard lithography steps were executed, as explained previously, using HiPR612 resist. Lithography was performed using a circular-shaped aluminium foil acting as the backside mask, which was designed for defining the etching window. After development, the oxide-nitride-oxide stack was exposed for the implantation.

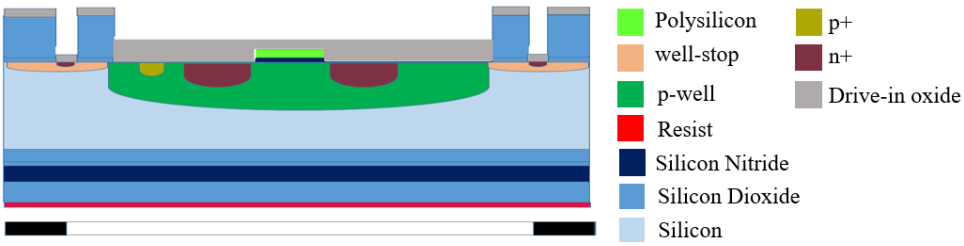


Figure 3.41: Cross-sectional illustration of lithography performed to define backside etching window.

Step-44: Oxide-Nitride-Oxide etching

The stack on the backside was deposited as etch mask for alkaline etching, was removed in Tegal 903 using appropriate dry etch chemistry.

Step-45: Lithography 9

Standard lithography steps were executed, as explained previously, using HiPR612 resist. Lithography was performed using Mask Con Hole, which was designed for defining the contact holes in the passivation layer deposited in step-58. After development, the patterned oxide was exposed for the etching of contact holes.

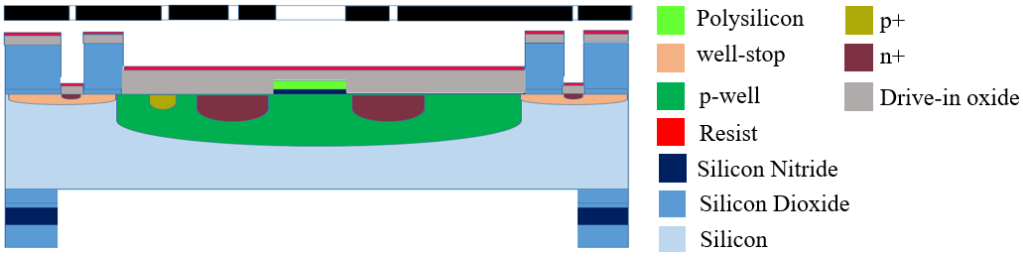


Figure 3.42:Cross-sectional illustration of lithography performed to define contact holes in passivation layer.

Step-46: Contact hole opening and oxide etch dip

The contact holes are etched into the 300 nm SiO_2 layer in Tegal 903, from the top surface down to the level of silicon. Immediately after this, the wafers were dipped in buffered oxide etchant for 10 seconds in order to remove any oxide residue on the side walls of the contact holes. The wafers were thoroughly cleaned to prevent any attack on the passivation layer.

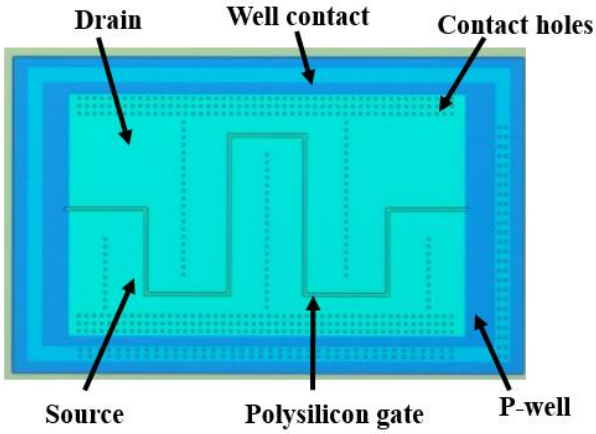


Figure 3.43: Optical image of device after opening of contact holes, showing the different regions of the FET.

Step-47: Pre-metal deposition clean

The wafers were soaked in DI water for 5 minutes and dipped in buffered oxide etchant for 5 seconds, just before the metal deposition. This step ensured that there was no oxide in the contact holes.

Step-48: Metal deposition

50 nm thick titanium and 600 nm thick Al-Si% was sputtered over the wafers in ULVAC metal depositor.

Step-49: Lithography 10

The wafers were just rinsed in DI water to avoid damage to the metal layer in ultrasonic agitation. Primer and MaN-1420 (negative resist) were spin coated with a speed of 3000 rpm and baked at 1150^{o}C for 2 minutes. Lithography was performed using Mask Metal1, which was designed for defining the metal layer and interconnection scheme on the wafer. An exposure of 6 seconds in development for 2 minutes in developer was conducted before the hard bake at 150^{o}C. After development, the patterned metal was exposed for the etching of aluminium.

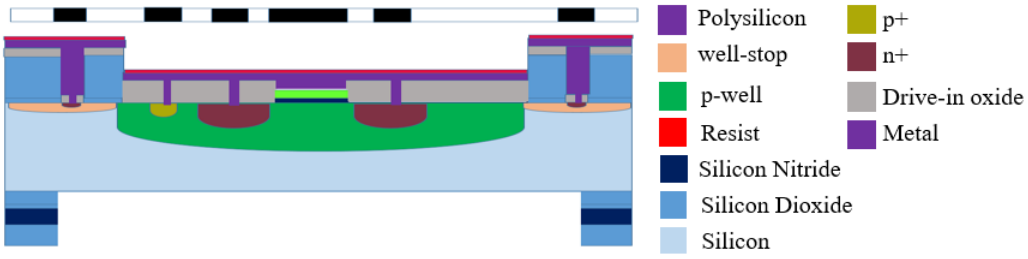


Figure 3.44: Cross-sectional illustration of lithography performed to define metal layer.

Step-50: Metal etching

The unmasked metal was etched in Tegal 6510 using chlorine-based chemistry.

Step-51: Contact sintering

This step was required for improving the electrical contacts between the metal and the silicon substrate. The wafers are sintered at 400°C for 30 minutes in forming gas in Tube 8.

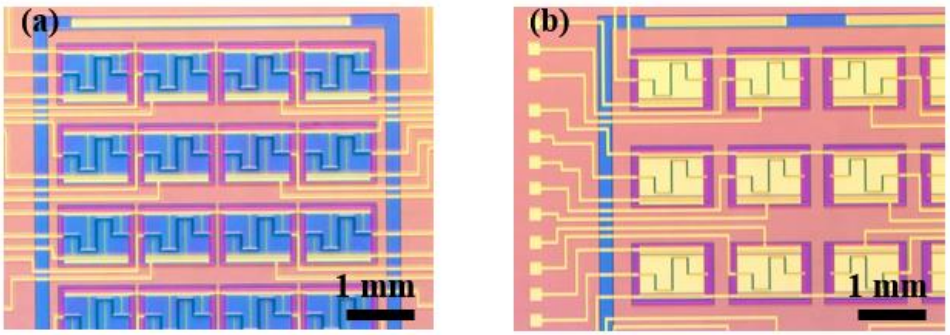


Figure 3.45: Optical images of devices after (a) patterning the resist for lift-off, and (b) deposited metal after contact sintering.

Step-52: SiO_2 deposition

200 nm thick SiO_2 was deposited over the wafer frontside using low frequency PECVD method. This layer, also called overglass, was deposited to protect the metal from the normal wear and tear.

Step-53: Lithography 11

The wafers were rinsed in DI water and lithography was performed following the steps mentioned in step-69 using MaN-1420. The exposure was done using Mask Overglass, which was designed for opening the protection layer in order to gain access to the contact pads and interconnection scheme on the wafer. After development, the patterned overglass was exposed for the etching of SiO_2.

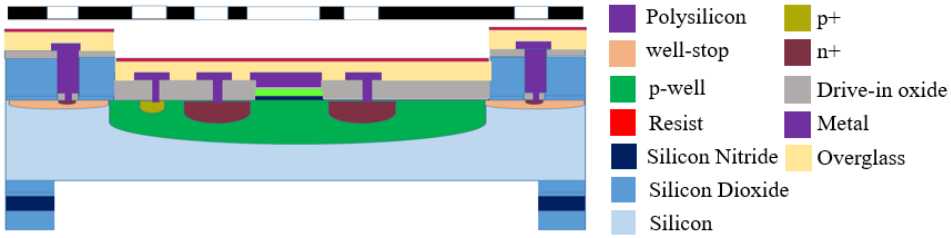


Figure 3.46: Cross-sectional illustration of lithography performed to define opening area in passivation layer.

Step-54: Overglass etching

The unmasked area of overglass was etched in Tegal 903 using CF_4 chemistry, giving access to the contact pads at the chip edges and the gate area for deposition of piezoelectric material.

Step-55: Plasma ashing and final rinse

The resist on the frontside was removed in oxygen plasma for 30 minutes and the final rinse was performed.

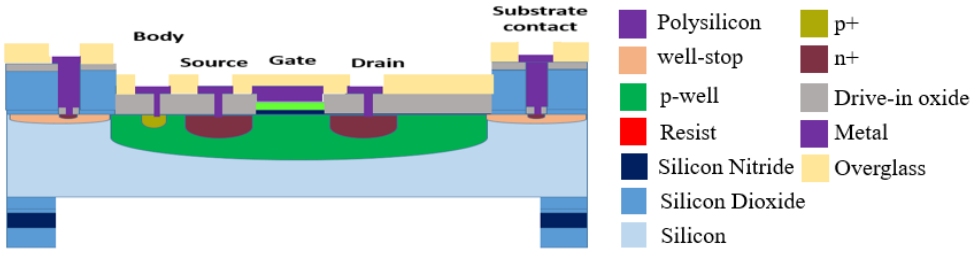


Figure 3.47: Cross-sectional image of wafer after protection layer patterning.

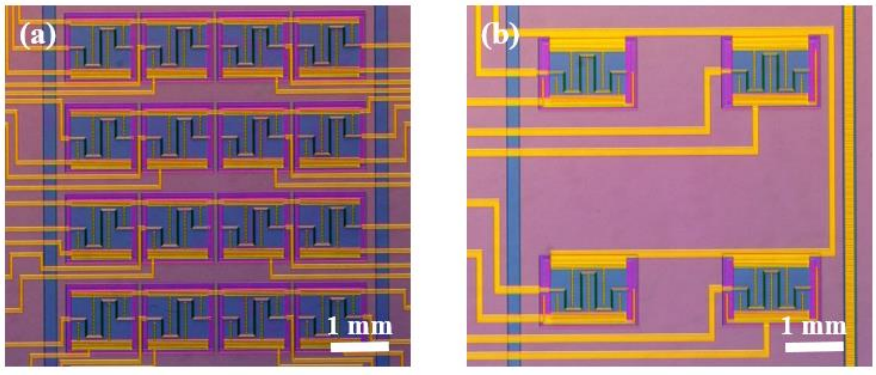


Figure 3.48: Optical images of devices at final stage after overglass deposition and patterning.

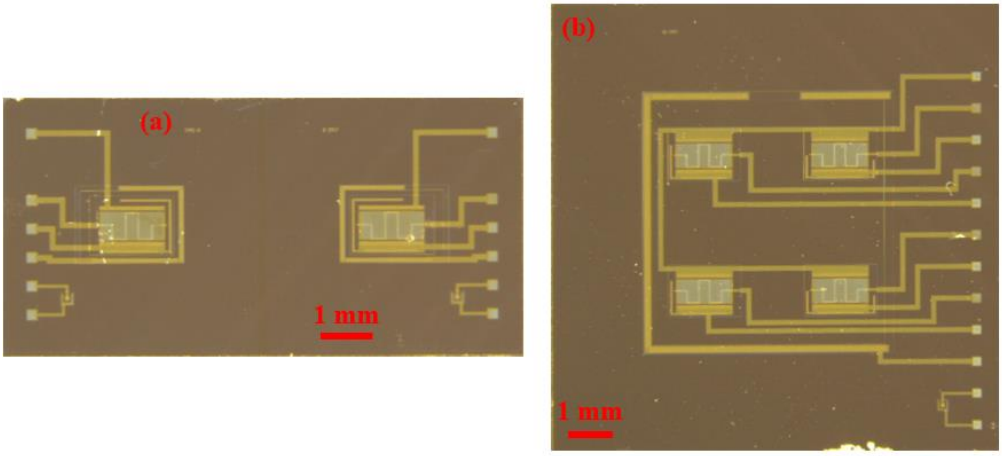


Figure 3.49: Micrograph of the fabricated chips. The left image consist two individual MOSFETs, and the right image consists an array of 2x2.

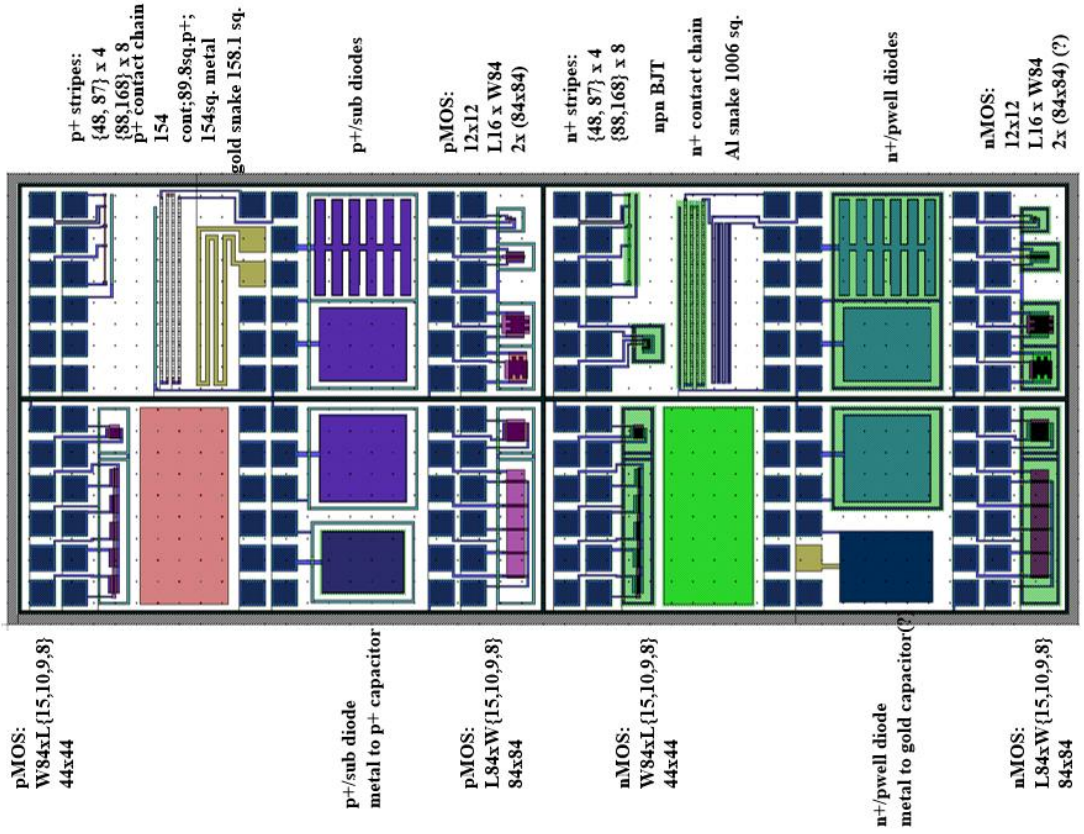


Figure 3.50: Layout of test strip which was designed to monitor the processing steps. It consisted of nmos, pmos, bjt, capacitors, resistors, implant areas, and oxidation areas. The devices on this test strips were characterised during the fabrication stage to confirm the success of important steps and extract device parameters.

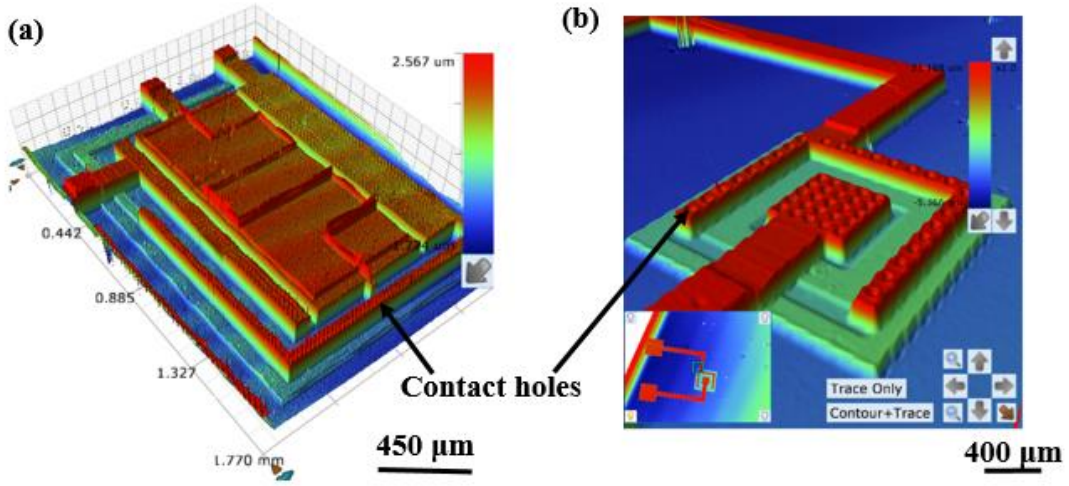


Figure 3.51: Optical profilometer scan of (left) MOSFET (right) diode, showing the height contour of different layers. The scan also shows the contact holes etching over the implant and well-contact area. The optical profiling gives high precision measure of surface roughness quickly as compared to stylus profiling.

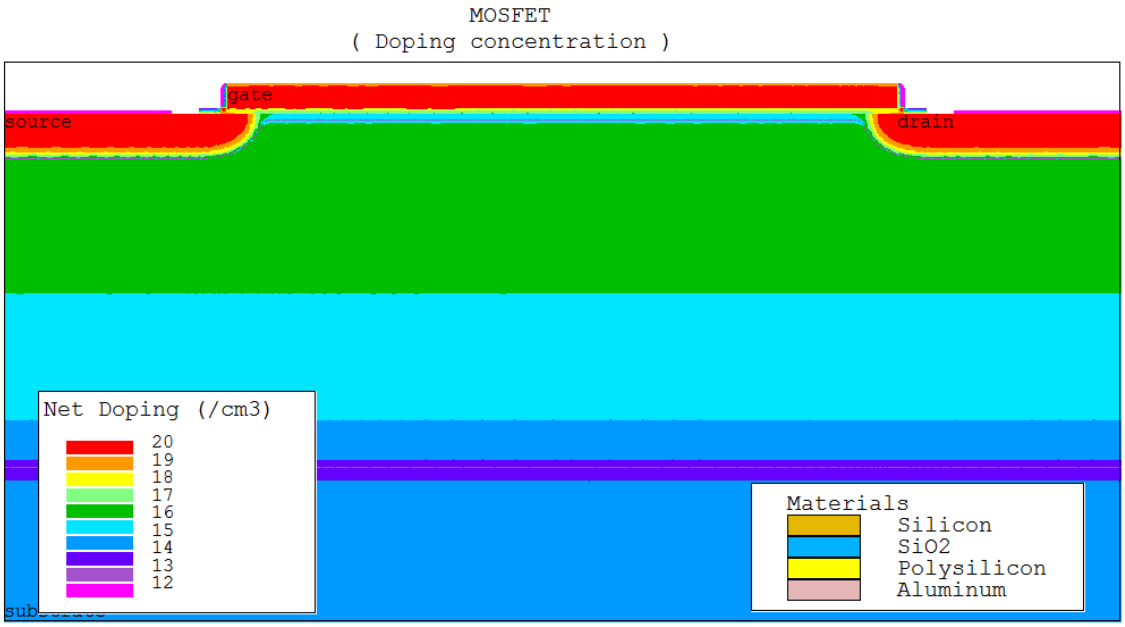


Figure 3.52: Simulated doping profile of fabricated MOSFET. Simulation has been done using SILVACO and the colour plot shows the doping densities in the different region of MOSFET. The source and drain region surface has the highest dopant concentration (~10^{20} /cm^3) and decreases till the p-well junction (~10^{17} /cm^3).

3.3. Conclusion

This chapter presents the research work carried out to fabricate MOSFETs for the purpose of realising bendable silicon-based tactile sensor. The fabrication process was tailored to become compatible with the change in wafer size from 4 inch to 6 inch. The mask set was designed with improved design tolerance and implemented updated design rules. The stack of silicon nitride and silicon dioxide which was used as gate oxide in previous process was replaced with high quality silicon dioxide, which resulted in fewer trapped charges and better control on threshold voltage. The number of masks was also reduced from 13 mask to 9 mask by excluding implant stop steps. These modifications resulted in an overall decrease in number of steps from ~200 steps to ~125 steps. In summary, the process was implemented with 12 lithographies, 5 implantations, 5 dry oxidations, 1 wet oxidation and 7 depositions steps. The gate oxide was composed of 50 nm thick SiO_2, instead of stack of Si_3N_4/SiO_2, which resulted in lower concentration of trapped charges and better control over threshold voltage. All of these changes with respect to previous runs ensued in high performance transistors whose electrical characterisations are presented in Chapter 7.

Chapter 4. Piezoelectric Materials as Transducer for Tactile Sensor

The material selection is an important part of a "smart material" integrated sensors. P(VDF-TrFE) has been a common choice for piezoelectric tactile sensors due to its easy proccessability and inherent flexibility. However, the challenges associated with P(VDF-TrFE) which are sensitivity to temperature and requirement of poling, leaves room for the research of other piezoelectric materials. Therefore, this chapter presents the work done in the area of investigating other piezoelectric materials. In the first part, a composite of P(VDF-TrFE) and BT nanoparticles has been used, which due to opposite piezoelectric and pyroelectric, reduces the sensitivity to temperature. In the second part, a structurally piezoelectric material, Aluminium Nitride was investigated, as it does not need any poling procedure.

4.1. Piezoelectricity

The word piezoelectricity means electricity by pressure and is derived from a Greek word, In 1880, Pierre Curie and Jacques Curie observed that positive and negative charges appeared on parts of a crystal surface when subjected to stress[166], which Hankel in 1881 termed as piezoelectricity [167]. The material becomes polarised and the charges, which finally appear on the surface, are called polarisation charges. This polarisation charge set up an electric field across the material that can be harnessed as electrical energy by depositing electrodes at two surfaces of the material [168]. This conversion of mechanical energy to electrical energy was termed as "direct piezoelectric effect" by Lippmann who also predicted the presence of reverse piezoelectric effect[169]. The Curie brothers then verified this prediction of Lippmann, in 1882, when they showed that on application of an electric field, deformation is observed in material structure, causing strain in those materials.

4.2. Piezoelectric Constitutive Equations

The IEEE Standard on Piezoelectricity has documented the constitutive equations for linear piezoelectric material in a detailed manner [170]. Both the direct and converse piezoelectric effects can be expressed mathematically as a relationship between four field variables i.e. stress, strain, electric field and electric displacement. Considering any two field variables as independent variables, four forms of the constitutive equations can be written, however, the most common representation of these relations is expressed in tensor notation as:

$$S_{ij} = s^{E}_{ijkl} T_{kl} + d_{kij} E_k \quad (4.6)$$

$$D_i = d_{ikl} T_{kl} + \varepsilon^{T}_{ik} E_k \quad (4.7)$$

where $S_{ij}$is the mechanical strain, $D_i$is the electric displacement, T_{kl} is the mechanical stress, E_k is the electric field, s^{E}_{ijkl} is the mechanical compliance measured at constant electric field, d_{ikl} is the piezoelectric strain coefficient, and ε^{T}_{ik} is the dielectric permittivity measured at zero mechanical stress.

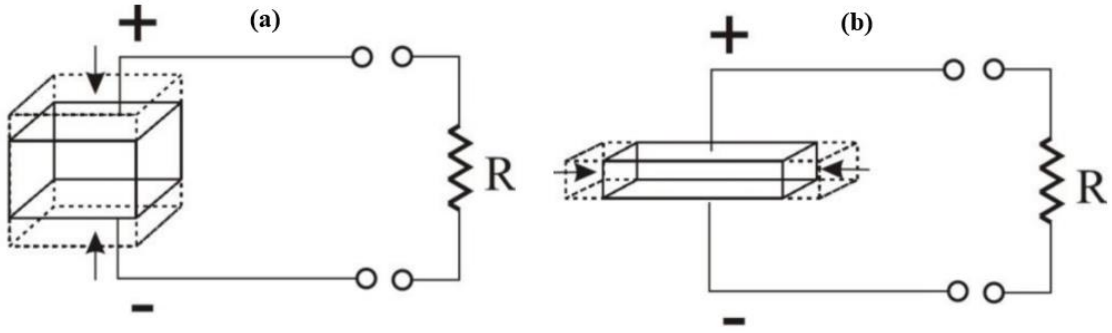


Figure 4.53: Piezoelectric material in (a) 33 mode and (b) 31 mode. In 33 mode, direction of stress application are in same direction, whereas in 31 mode, they are in perpendicular direction.

The piezoelectric material is generally used in two corresponding modes, 33 and 31, and are shown in Figure 4.53. In 33 mode, the stress acts in the same direction as the voltage appears and in 31 mode, it acts in a direction perpendicular to the direction where voltage appears. For 33 mode, which is used in pressure sensing, the constitutive can be simplified to:

$$S_3 = s^{E}_{33} T_3 + d_{33} E_3 \quad (4.8)$$

$$D_3 = d_{33} T_3 + \varepsilon^{T}_{33} E_3 \quad (4.9)$$

Here, in absence of any electric field, which is the case in most of times during sensor characterisation, equation 4.4 can be written as: $D_3 = d_{33} T_3$ which means charge is directly proportional to force and piezoelectric coefficient. That is why, for a better sensor, materials with high piezoelectric coefficients are preferred.

For 31 mode, which is commonly used for strain sensor and energy harvesters, the constitutive can be simplified to:

$$S_1 = s_{11}^{E} T_1 + d_{31} E_3 \quad (4.10)$$

$$D_1 = d_{31} T_1 + \varepsilon_{31}^{T} E_3 \quad (4.11)$$

Similarly, in this mode, the material need to have higher d_{31}, if one need to have a high performance strain sensor.

These constitutive equations are widely used for finite element modelling. However, there are a number of limitations of the linear constitutive equations. The piezoelectric effect is actually non-linear in nature due to hysteresis and creep and piezoelectric coefficients are temperature dependant and show a strong electric field dependency.

4.3. Piezoelectric Materials

One of the important areas of research in the area of piezoelectric sensor is discovering the phenomenon of piezoelectricity in new materials. Piezoelectric materials can be natural or man-made. The natural materials are crystals such as quartz (SiO_2), Rochelle salt, Topaz, Tourmaline-group minerals and some organic substances such as silk, wood, enamel, dentin, and bone. However, it is the man-made piezoelectric materials including ceramics, polymers and composites which fuelled the piezoelectric sensor industry, due to their better properties when compared to natural piezoelectric material. In this section, four piezoelectric materials, which possess some very unique properties leading to their widespread use in sensors, have been discussed briefly. The first is PZT which has very high piezoelectric coefficient and is used for applications where mechanical stimuli are limited by low values. The second is BT, which due to its lead-free nature, finds application in the bio-medical area. The third piezoelectric material is AlN, which has the interesting advantage that it does not need poling to exhibit piezo properties. The fourth material is PVDF, which due to its flexibility, is very useful in flexible electronics-related applications.

4.3.1. Lead zirconate titanate

Lead zirconate titanate ($Pb[Zr(x)Ti(1-x)]O_3$), often referred to as PZT, is one of the most widely used piezoelectric ceramic materials. PZT has a perovskite crystal structure, as can be seen from Figure 4.54(a), with each unit consisting of a small tetravalent metal ion in a lattice of large divalent metal ions. It has many uses, most commonly as a piezoelectric ceramic. Piezoelectric thin films of PZT are widely used in the field of sensors and actuators, due to

their ability to generate large displacements, the higher sensitivity and higher energy densities with a wide dynamic range and low power requirements [171].

4.3.2. Barium Titanate

Barium Titanate (BT) is a member of a large family of compounds with the general formula ABO_3 that has a perovskite structure, as shown in Figure 4.54(b). It was found during World War II as a high dielectric constant material. Later on, the discovery of electrostriction effect for the unpoled BT together with the piezoelectricity for the poled samples was found, leading to many applications in the area of sensors [172]. Due to its high dielectric constant and low loss characteristics, BT has been used in applications, such as capacitors and multilayer capacitors (MLCs) [173]. Whereas, doped BT has found wide application in semiconducting devices, PTC thermistors [174] and piezoelectric devices [175], and has become one of the most important ferroelectric ceramics.

4.3.3. PVDF

In 1969, Kawai found that when a semi-crystalline polymer, PVDF, a chain of CH_2CF_2 is subjected to the effect of both mechanical stretching and the application of an electric field, it transforms from α phase to β phase and becomes strongly piezoelectric [45]. Until now, researchers have identified at least four different crystals structures for PVDF polymers, commonly termed as α, β, γ, and δ. Nevertheless, α and β are always in the majority as the β phase actually has more intermolecular stability, while α phase is favoured on an intramolecular basis. PVDF's α phase, which is a combination of helical and planar zigzag, occurs in a trans-gauche-trans-gauche (TGTG) formation. The β phase of PVDF is a planar zigzag, or trans-trans (TT) configuration. Numerous studies has been dedicated and can be found in literature relating to various processing steps optimisation which could potentially enhance the β phase [47-49]. Its strong piezoelectric properties, chemical resistance, and mechanical durability make it a valuable transducer material for use as sensors and actuators. However, the need of stretching for inducing piezoelectric properties in the film becomes a hurdle in micro fabrication steps while fabricating the sensors. This challenge has been overcome either by altering the polymer structure or by mixing it with other piezoelectric materials, such as carbon nanotubes, graphene and ceramic nanoparticles.

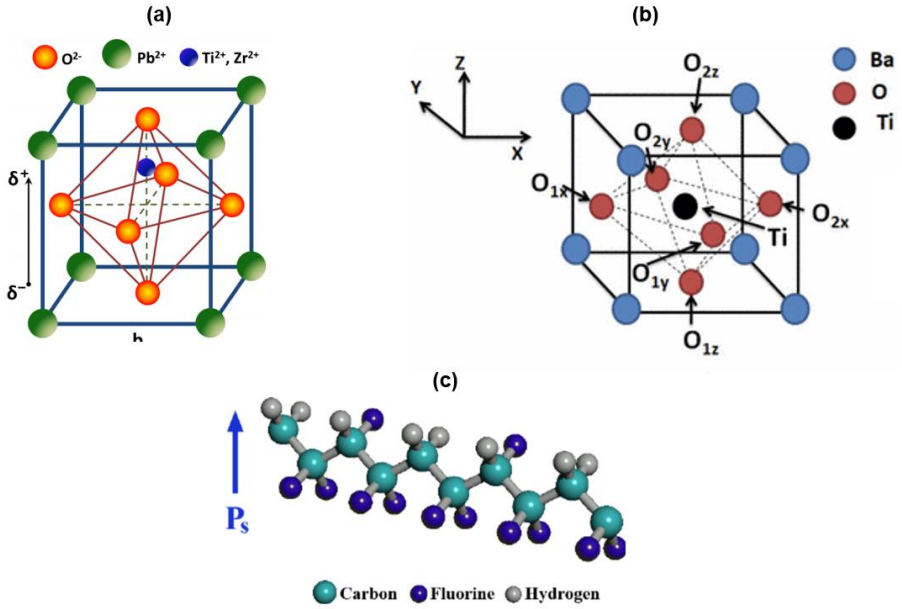


Figure 4.54: Structure of (a) PZT (b) BT (c) P(VDF-TrFE) [176] [177] [178]

4.3.3.1. PVDF copolymers

When two different types of monomers are joined in the same polymer chain, the polymer is called a copolymer. In the case of PVDF, when the CH_2-CH_2 chains are joined with trifluoroethylens, as shown in Figure 4.54(c), it gives P(VDF-TrFE). Due to the addition of extra electronegative fluorine, the polymer chain is forced to all-trans configuration, which is the polar phase, and thus eliminates the need for stretching. In fact, the extent of crystallisation in P(VDF-TrFE) is much more than PVDF. It exhibits strong piezoelectric, pyroelectric and ferroelectric behaviour. Although the piezoelectric coefficient of PVDF is higher than its copolymers, the ease in processing, enhanced crystallisation to polar phase, and higher temperature range, makes the copolymer favourable for sensor fabrication.

4.3.4. Piezoelectric composite

Piezoelectric ceramics are generally less expensive and can be fabricated at a large scale easily than polymers or single crystals. With their relatively high dielectric constant and good electromechanical coupling coefficient, they are preferred for mechanical power sources. However, they are stiff and brittle, which means that the monolithic ceramics cannot be formed onto curved surfaces, limiting design flexibility in the transducer. They also have a high degree of noise associated with their resonant modes. On the contrary, piezoelectric polymers are mechanically flexible and can be made in multiple shapes and sizes. However, applications for

these polymers are limited, due to their low electromechanical coupling, low dielectric constant, and high cost of fabrication. One well-accepted way to achieve the beneficial properties of both ceramic and polymer is to combine them together to make composite. Piezoelectric composite is a system that consists of a polymer phase (active or inactive) in combination with piezoelectric ceramic fillers. Piezoelectric ceramic/polymer composites combine high coupling coefficient and dielectric coefficient of ceramic with flexibility and low impedance of polymer.

To obtain a better and uniform dispersion of ceramic in polymer, nanoparticles of filler is desired as filler material. Once mixed with the polymer, the field patterns within the composite which is decided by the arrangement of the two phases comprising the composite, dictates its electromechanical properties. Out of many connectivity patterns, (0-3) is of specific interest, since in this type of pattern a three dimensionally connected polymer phase is loaded with zero dimensional ceramic powder. Since the polymer is base material in (0-3) composite, it can be easily fabricated in a variety of shapes and sizes including large flexible sheets. Moreover, it can be produced at a mass level and is suitable for applications involving conformal surfaces. The properties of (0-3) composites are very sensitive to the choice of filler and base material, as well as the used fabrication method.

Initial attempts of producing (0-3) composites can be traced back to 1972, when Kitayama and Sugawara from Japan used PZT as a filler in polyurethane. Several types of composite with PZT dispersed in chloroprene rubber or Eccogel are also reported. Later on, the piezoelectric polymer PVDF was also used as a matrix, which provided a greater degree of freedom and provided more control on tuning the piezoelectric property of composite. The toxic nature of lead has led to other piezoelectric nanofillers such as BT, bismuth sodium titanate (BNT) and sodium potassium niobate (KNN) to be used as fillers.

4.4. Multi sensing using piezoelectric composite

Suitable selection of filler, polymer and their volume ratio could allow the fabrication of a new class of material having tailored properties with considerable potential in sensor applications. For example, composites with inclusions of inorganic fillers such as nanoparticles, nanowires embedded in polymer matrix have been used for various applications such as sensors, actuators, energy storage and harvesters [179], some of which are tabulated in Table 4.4.

These composites are an attractive choice for many niche applications as they combine two or more properties of the constituent materials. The polymer of choice could be a simple elastomer such as PDMS, which aims to provide the mechanical flexibility, but depending upon the

Table 4.4: Various works reported in literature using PVDF and BT based composite.				
Polymer	**Filler**	**Application**	**Figure of Merit**	**Ref**
PVDF	BT	Energy harvesting	Output power: 25 µW	[182]
PVDF	BT	Energy storage	Energy density: 18.8 J cm^{-3}	[183]
PVDF-HFP	BT	Nano generator	Output voltage: 75 V @0.23 MPa	[184]
PVDF	BT, Ag	EMI shielding	Shielding effectiveness: 26 dB	[185]
PVDF	BT	Flow Sensor	15.8 nW at 125.7 m/s.	[186]
Epoxy	BT/PMN-PT	Capacitor	Capacitance density: 50 nF/cm^2	[187]

application requirements, active polymer such as PVDF, PVC etc. have also been used [138, 180, 181].

With ferroelectric ceramics (e.g. BT, lead titanate (PT) etc.) as inclusions, the composites can offer promising solutions for multifunctional touch sensing, as they combine the high pyroelectric and piezoelectric coefficients of the ceramic with the good mechanical properties (e.g. flexibility) of the polymer. Furthermore, if ,in addition to the inclusions, the polymer matrix is also ferroelectric (e.g. matrix of PVDF or P(VDF-TrFE)), then the poling state of the composite could be tailored to obtain an additional degree of freedom. For example, by polarising only the polymer matrix (Figure 4.55(a)) or only the inclusions (i.e. BT in P(VDF-

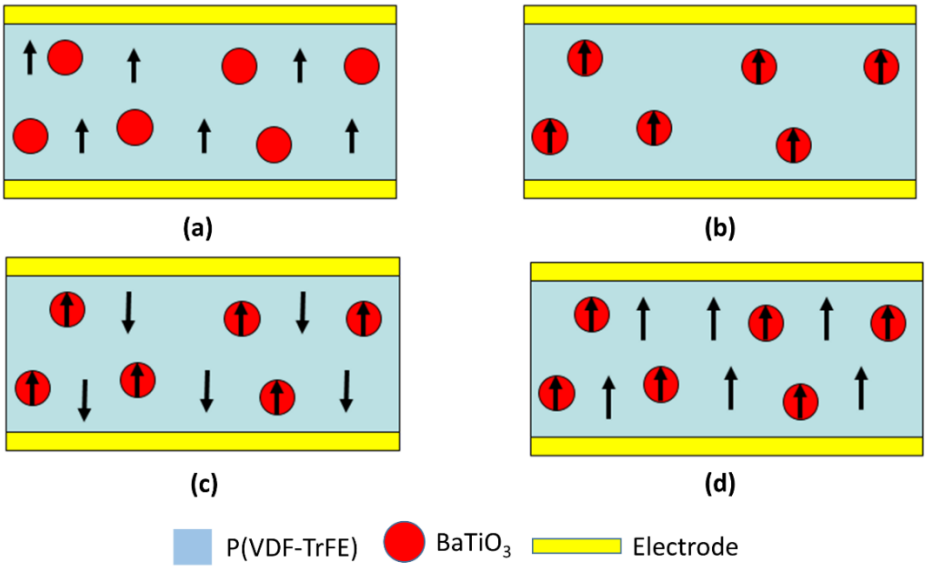


Figure 4.55: The polarisation state in (a) poled P(VDF-TrFE); (b) poled BT; (c) P(VDF-TrFE) and BT poled in opposite direction leading to strengthening of piezoelectric effect; (d) P(VDF-TrFE) and BT poled in the same direction to lead to strengthening of pyroelectric effect. [188]

TrFE)-BT nanocomposite) (Figure 4.55(b)) it is possible to tailor the effective pyroelectric and piezoelectric properties of the composite.

4.4.1. P(VDF-TrFE)/ BT composite based tactile sensor

In the case of tactile sensor for electronic skin application, piezoelectric composites are a good choice due to their virtue of converting mechanical stimuli into electrical signals. BT/PVDF nanocomposites are emerging as the smart choice for sensor applications due to their biocompatibility, convenient fabrication process, low cost, and tuneable properties [189-191]. BT has remarkable ferroelectric properties, high dielectric constant, and amiability towards the environment, compared with other useful ceramics such as PZT. It is gaining significant interest in those applications, which include proximity to biological living beings.

One interesting ability of PVDF/BT composites which can be harnessed to separate the piezoelectric effect from pyroelectric effect, is poling them separately in the composite, thus opening a way for the fabrication of piezoelectric materials in which pyroelectricity is internally compensated, or vice versa [192]. This is due to the fact that the piezoelectric coefficients of BT and P(VDF-TrFE) have opposite polarity, whereas their pyroelectric coefficients have the same polarity, and are summarised in Table 4.5.

Table 4.5: Piezoelectric and Pyroelectric coefficient of BT and P(VDF-TrFE)

Properties	BT	P(VDF-TrFE)	Ref
Piezoelectric coefficient d_{33} (pC/N)	193	-20 $\pm$2	[193, 194]
Pyroelectric coefficient [$\mu C/m^2K$]	-16900	-20 $\pm$4	[193, 195]

It allows the preparation of nanocomposites with enhanced piezoelectric activity but reduced pyroelectric activity if the matrices and inclusions are polarised in opposite direction and vice-versa if polarised in the same direction, as shown in Figure 4.55.

Therefore, taking into consideration the above-stated advantages and possible way to distinguish between the piezo and pyro effects, nanocomposite of P(VDF-TrFE) and BT became the preferred choice for multimodal tactile sensing.

4.4.2. Nanocomposite fabrication

The BT nanoparticle, with an average size of about 100 nm nanoparticle and Methyl Ethyl Ketone (MEK), was purchased from Sigma Aldrich. The P(VDF-TrFE) copolymer pellets

,with a VDF/TrFE molar ratio of 70/30, were acquired from Piezotech. In the first step, BT nanoparticles were dispersed in MEK solvent using a probe sonicator, followed by dissolution of pellets, as illustrated in Figure 4.56. This was done to ensure that the nanoparticles were not agglomerated in the viscous PVDF solution.

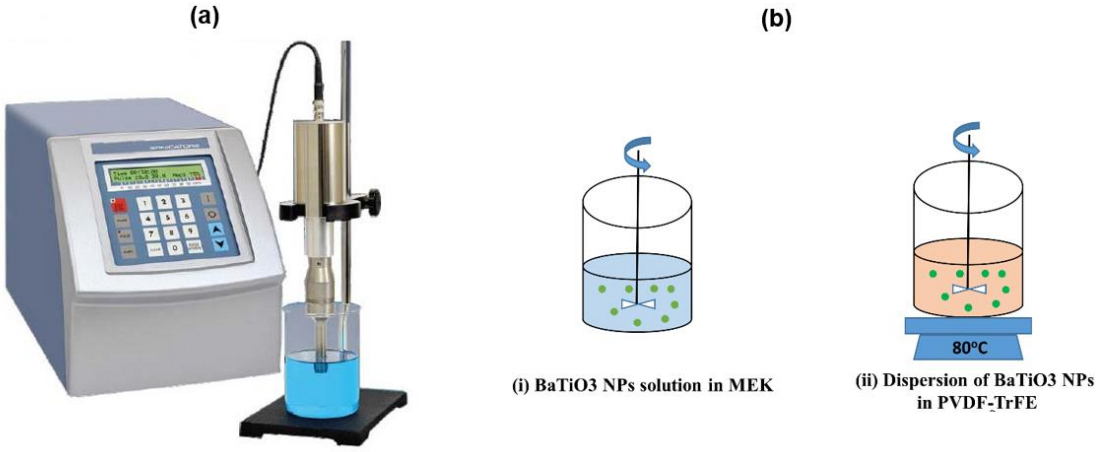


Figure 4.56: (a) Image of probe-sonicator used for making the composite (b) Illustration of the two-step process adopted to achieve uniform dispersion of NPs in matrix. [196]

The nanocomposite was then again bath sonicated for 1 hour before spin coating.

4.4.3. Nanocomposite characterisation

In order to analyse the effect of BT, various structural characterisation was carried out using various techniques. These methods aided the study related to structural property correlation. Importantly, the results show that the presence of a nucleation site and the space charge effect of BT favours the formation of β-phase in P(VDF-TrFE).

4.4.3.1. FTIR Spectroscopy

Fourier-transform infrared spectroscopy (FTIR) is a non-destructive, high precision used to obtain an infrared spectrum of absorption or emission of a solid, liquid or gas.

The molecular structure of pure P(VDF-TrFE) films was characterised using the Fourier-transform infrared spectroscopy (FTIR) technique and is presented in Figure 4.57. As depicted in the spectrum (blue line), the peak observed at 1,288 cm^{-1} is associated with CF_2 asymmetric stretching, C--C symmetric stretching, and C--C scissoring vibration. The vibrations associated with –C--F asymmetric stretch at 1288 cm^{-1} are sensitive to ferroelectric crystallinity, which can be observed in the spectrum. The peaks at 850 and 885 cm^{-1} associate with the –C--F

symmetric stretch and $–CH_2$ in plane rocking deformations, respectively. All these bonds are highly sensitive to dipole orientation towards the applied electric field [197].

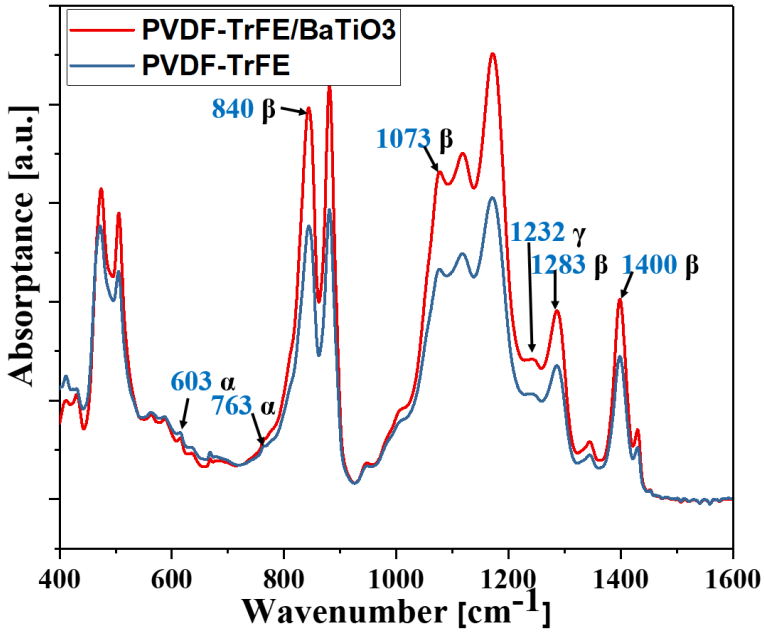


Figure 4.57: FTIR spectra of P(VDF-TrFE) and P(VDF-TrFE)-BT nanocomposite showing the characteristic peaks of polar β phases, which are at 840 cm^{-1} and 1283 cm^{-1}. The increase in peak intensity observed is attributed to bonding between fluorine of polymer and barium titanate nanoparticles. [188]

The vibration band at 840cm^{-1} is assigned to β-phase and the vibration band at 763cm^{-1} is assigned to α-phase. As can be seen from Figure 4.57, the intensity at 840 cm^{-1} is much higher compared with 763cm^{-1}. This confirms that pure P(VDF-TrFE) is dominated by β-phase. The FTIR spectra of nanocomposite was obtained for the same scan range (red line). The increase in intensity corresponding to β- phase increases shows the enhancement effect upon adding BT. The enhancement effect is attributed to the chemical bonding which occurs between P(VDF-TrFE) and BT. The underlying mechanism of interface bonding is explained elsewhere [198]. To be precise, fluorine of P(VDF-TrFE) being negatively charged can readily be combined with positively charged BT. Due to this tendency of fluorine, the effective mass increases and frequency of vibration decreases. The introduction of fluorine in the octahedron structure of BT, helps to decrease the interface and space charge. This results in the increment of dielectric constant of nanocomposite as electric dipoles can move more freely, without much hindrance from the space and interface charge.

4.4.3.2. Raman Analysis

Raman spectroscopy analysis was carried out for P(VDF-TrFE) and P(VDF-TrFE)-BT nanocomposite films, which are shown in Figure 4.58. Raman spectra provides insights regarding the conformation and chain skeleton of polymer over a large range of wave numbers. Thus, Raman data provides more spectroscopic information than that provided by FTIR analysis alone. The spectrum of pure P(VDF-TrFE) shows that the polymer alone was dominant in β phase, which is confirmed by peak intensity at 836 cm^{-1}. Furthermore, it is noteworthy to record that Raman bands at 836 cm^{-1} and 1430 cm^{-1} that corresponds to the presence of ferroelectric β phase shows higher intensity in the case of nanocomposite than pure P(VDF-TrFE). Thus, it is indicated that the addition of BT nanoparticles (NPs) increases the ferroelectric property of the material. Moreover, the inset in Figure 4.58 shows the Raman spectrum for a short range of 500 cm^{-1} to 600 cm^{-1}. The peaks of the Raman spectrum positioned at 513 cm^{-1} [E, A_1(TO)], which is subjective to a tetragonal phase, revealed that the BT NPs have a tetragonal phase and there was no degradation in the structure of NPs during the nanocomposite preparation [184].

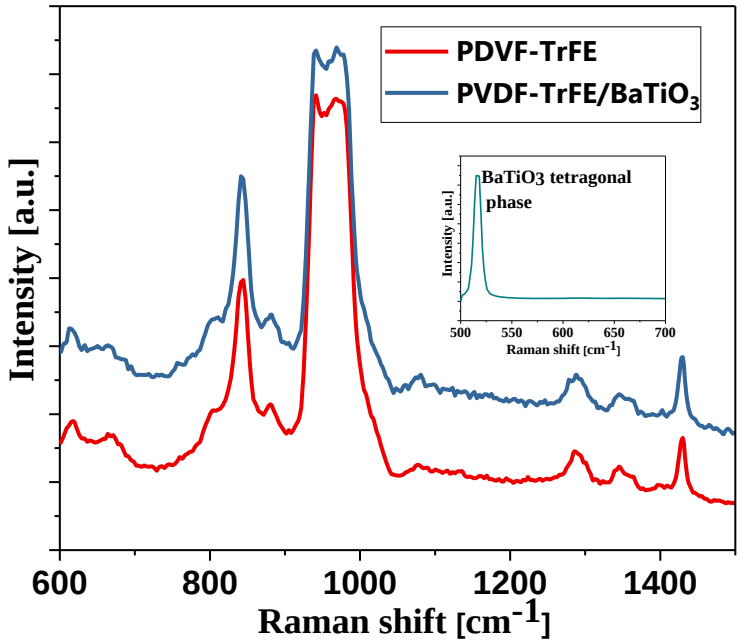


Figure 4.58: Raman spectra of P(VDF-TrFE) and P(VDF-TrFE)-BT nanocomposite showing the β peak enhancement. Inset shows the tetragonal phase of BT. [188]

4.4.3.3. Surface morphology characterisation

The surface morphology of nanocomposite was studied using the AFM technique and the scan images of P(VDF-TrFE) and its composite are shown in Figure 4.59 (a-b). The images predominantly show two types of structures in both pure PVDF–TrFE and nanocomposite. In the case of pure P(VDF-TrFE), the darker region in the image corresponds to amorphous copolymer state, which belongs to nonpolar α phase. The lamellar structures in the surface are crystalline fraction of the copolymer. These structures have an average length of 1.2 μm and diameter of 0.3 μm shows the presence of polar

β-phase. On further investigating the composite, it can be observed that the addition of ceramic nanoparticles leads to formation of interconnected lamellar structure in the film.

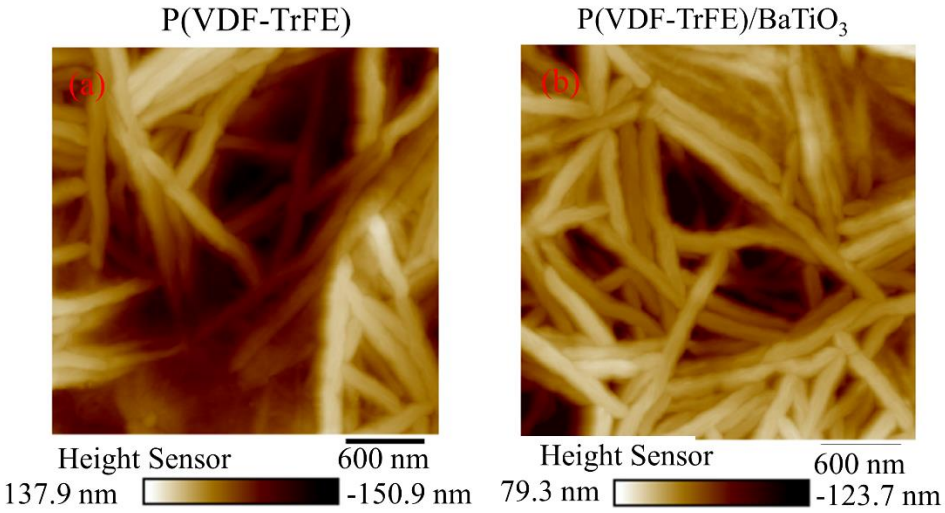


Figure 4.59: AFM images of P(VDF-TrFE) and P(VDF-TrFE)-BT indicating the emergence of interconnected lamellae upon adding nanoparticles. [188]

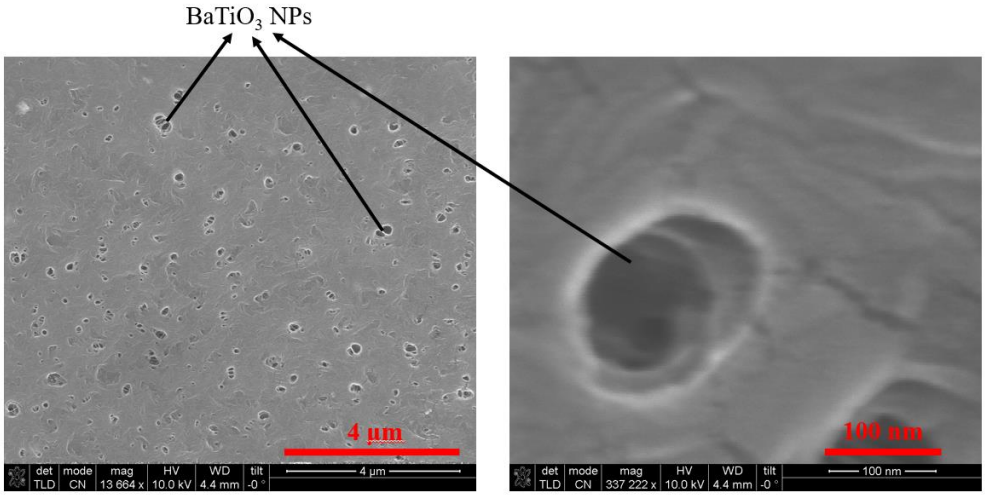


Figure 4.60: SEM images of nanocomposite showing dispersion of BT nanoparticles in P(VDF-TrFE) matrix. [188] There are observed agglomerations of particles as well as individual nanoparticles are also observed.

These structures were observed to improve the β phase [199]. The ratio of brighter to darker area, which corresponds to the ratio between polar and nonpolar phase, has significantly improved. Moreover, the lamellae average length increased to 1.5 µm and with decrement of diameter to 0.2 µm. The increase in β-phase is due to the spatial confinement of the polymer chains imposed by the nanoparticles and amplified by charge-dipole interfacial interactions [200].

The dispersion state of BT in PVDF matrix was determined from the morphology of top surfaces of PVDF-BT nanocomposite. As shown in Figure 4.60, the agglomerates of BT appeared to be dispersed within the polymer matrix, with the high contrast area showing the presence of NPs. There are evidences of single nanoparticles too when investigated at high magnification.

4.4.3.4. Energy-dispersive X-ray (EDX) spectroscopy

Elemental composition of the nanocomposite has been analysed using SEM-EDX technique (SEM-SU8240). The presence of various elements was confirmed from EDX spectra, as shown in Figure 4.61. The signal counts were reasonably high to confirm the presence of heavy elements. The observed ratio between Ba and Ti could be a good indication of the compound with possible defects. These results distinctly show that BT NPs were incorporated in PVDF matrix during spin coating.

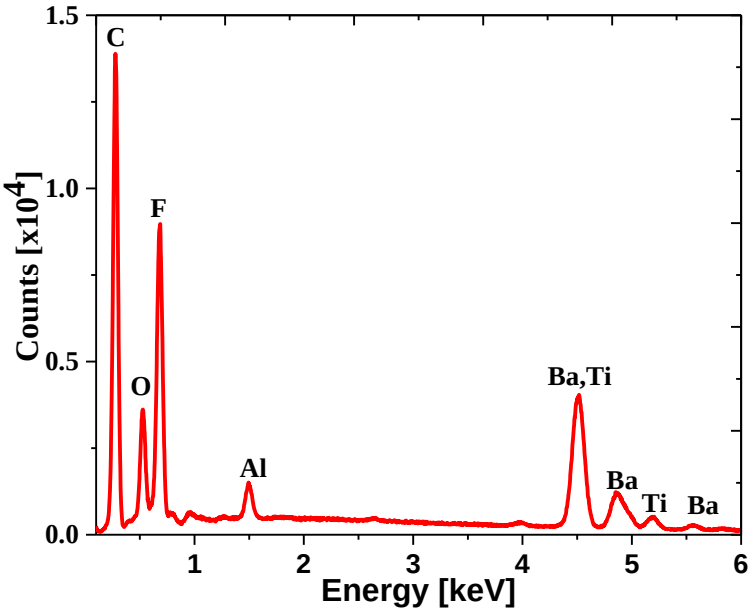


Figure 4.61: EDX spectra of the nanocomposite highlighting the peaks related to its constituents. The peaks of carbon and fluorine are associated with P(VDF-TrFE) and peaks of Ba, Ti and O are due to the nanoparticles. [188]

4.4.4. Sensor fabrication

Polyimide film from Dupont was used as a flexible substrate for the sensing layer. The PI film was thoroughly cleaned and fixed on a carrier wafer. 100 nm thick aluminium was evaporated for the bottom electrode, using MEB550S. The nanocomposite was spin coated at a rate of 500 rpm for 10 seconds, followed by 1000 rpm for 30 seconds, to ensure uniform spread and thickness over the sample. The film was then annealed in nitrogen ambient for 1 hour at 140°C. At this temperature, the viscosity of nanocomposite decreases and becomes low enough to allow the motion of conformers without deformation of the crystal structure. Since 140°C is more than α relaxation temperature, the tendency of crystallisation to β phase is considerably greater. The thickness of film was measured to be 4 µm after annealing. 10 nm/150 nm of nichrome and gold was then evaporated through a hard mask to realize top electrode. PI substrate was then gently released from the carrier wafer. In order to make the electrical connection, thin conductive wire was attached on the top and bottom electrodes using silver paste and secured with epoxy glue. The fabrication process is schematically shown in Figure 4.62.

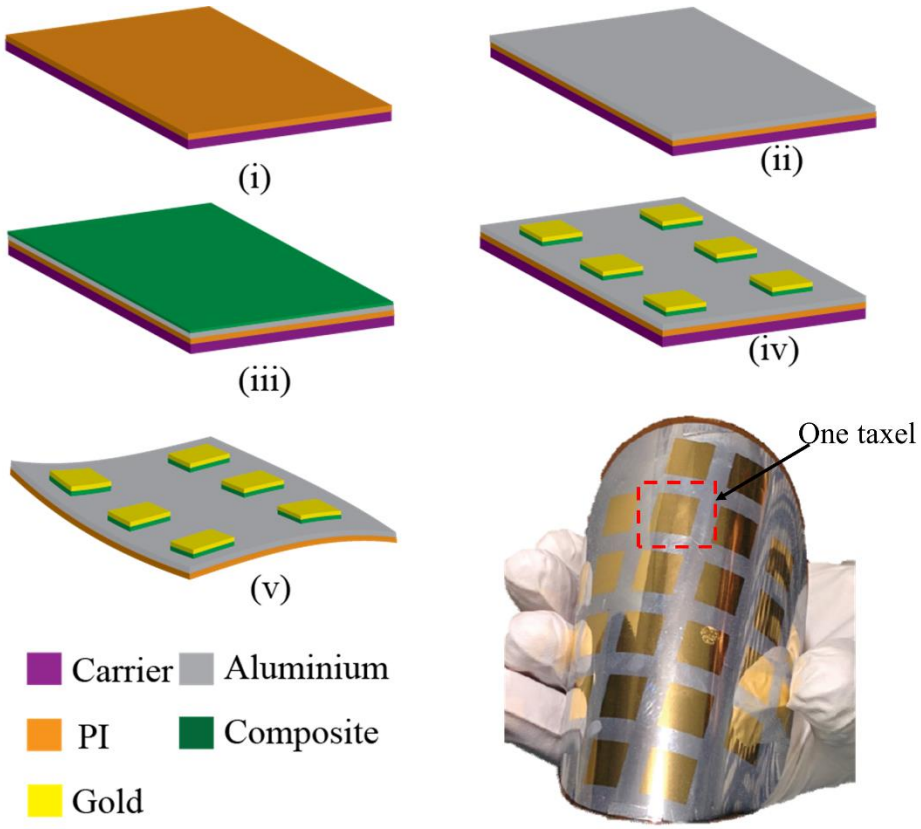


Figure 4.62: Fabrication steps adopted for realising the P(VDF-TrFE)/BT based sensing structure and image of final flexible sensor. [188]

4.5. Aluminium Nitride

One of the major challenges associated with materials such as PZT and PVDF, especially when they are integrated with FETs, is associated with the poling, i.e. the high-voltage needed to orient the dipoles in a particular direction to introduce piezoelectric behaviour. As an example, approximately 80V is needed to orient dipoles in a 1 μm thick P(VDF-TrFE) sample. Such high voltage poses a severe risk to the reliable operation of the transistor part in devices such as POSFETs, where P(VDF-TrFE) is coated on the gate area to obtain a dynamic response to contact force. The issue could be addressed either by taking extra measures to protect the transistor (e.g. grounding everything underneath the piezoelectric layer) or by using an alternative piezoelectric material which does not require any poling step. The additional steps to protect the transistor make the fabrication complex and the high voltage could still lead to local sparking, which could damage the chip. For this reason, Aluminium Nitride (AlN) was investigated as an alternative piezoelectric material. Due to its non-centrosymmetric wurtzite crystal structure, the AlN is structurally piezoelectric and does not need poling. This feature is

very attractive in cases such as the above where the piezoelectric material is used with MOSFETs. AlN fabrication is also compatible with standard IC-fabrication technology. Indeed, due to this compatibility, AlN has been one of the most commonly-used piezoelectric materials for the fabrication of electroacoustic devices and sensors such as thin film BAW band-pass filters.

Although the piezoelectric properties of AlN are inferior in comparison to other ferroelectric material such as PZT, zinc oxide (ZnO), BT and PVDF, it is still preferred in many MEMS applications due to its high signal to noise ratio, low dielectric loss tangent and hysteresis-free behaviour. It also has a range of unique structural (Table 4.3), optical (Table 4.4), electrical (Table 4.5), thermal (Table 4.6), and piezoelectric (Table 4.7), properties, such as wide bandgap (6.2 eV), high thermal conductivity (170W/m-K), high breakdown voltage (4 MV/cm), and high electrical resistivity ($1x10^{16}$ Ω.cm), which prevent electrical failure and charge leakage from AlN thin films. It also has high Curie temperature (1150 °C) and melting point (~2200 °C), which makes AlN attractive for high temperature applications. Due to its high quality factor (~3000), acoustic velocity (11300 m/s), moderate coupling coefficient (~6.5%) and low propagation loss, AlN is also suitable for bulk acoustic wave devices [14]. Moreover, it is thermally and chemically stable, especially in an inert environment and oxidation starts at its surface in air at a temperature above 800 °C. Unlike PZT, AlN does not pose any contamination risk during CMOS fabrication. Further, like piezoelectric polymers AlN can be suitable for emerging fields such as flexible electronics, as thin layers of AlN can be deposited at room temperature on flexible substrates.

Table 4.3: Structural properties of AlN [201-203]

Properties	Value
Density (g/cm^{-3})	3.257
Modulus of Elasticity (GPa)	331
Elastic Constant (GPa) C_{11}	410±10
Elastic Constant (GPa) C_{12}	149±10
Elastic Constant (GPa) C_{13}	99±4
Elastic Constant (GPa) C_{33}	389±10
Elastic Constant (GPa) C_{44}	125±5
Common Crystal Structure	Wurtzite
Poisson's Ratio	0.22

Lattice constant (Å)	a = 3.112 c = 4.982
Hardness (Kg/mm^2)	1100
Water Absorption	None

Table 4.4: Optical properties of AlN [201-204]	
Properties	Value
Density of States Conduction Band (cm^{-3})	4.1×10^{18}
Density of states Valence band(cm^{-3})	4.8×10^{20}
Effective hole mass	mhz = 3.53 m0 mhx =10.42 m0
Optical phonon energy (meV)	113
Refractive index (vis-ir)	~2.15

Table 4.5: Electrical properties of AlN [201-203, 205]	
Properties	Value
Breakdown field (V/cm)	$1.2\text{-}1.8\times10^6$
Mobility electrons holes (cm^2/V-s)	135 /14
Dielectric constant (static/high frequency)	8.5-9.14 / 4.6-4.84
Energy Band Gap (eV)	6.13-6.23
Resistivity (Ohm-cm)	1013

Table 4.6: Thermal properties of AlN [201-204]	
Properties	Value
Thermal conductivity (W/mK)	175
Thermal expansion (20-400°C)	$(4.2\text{-}4.3)\times10^{-6}$
Debye temperature (K)	980
Melting Point (°C)	2200

Table 4.7: Piezoelectric properties of AlN [201-204]	
Properties	Value
Piezoelectric coefficient (pC/N) d_{33}	1-6
Coupling Coefficient (C/m2) e_{15}	-0.33~-0.48
Coupling Coefficient (C/m2) e_{31}	-0.38~-0.82
Coupling Coefficient (C/m2) e_{33}	1.26-2.1
Relativity Permittivity Coefficient ε_{11}	9
Relativity Permittivity Coefficient ε_{22}	9
Relativity Permittivity Coefficient ε_{33}	11

Despite the many advantageous properties discussed above, AlN is scarcely used as a transducer in piezoelectric sensors due to the challenges associated with growing it in a specific orientation. AlN film needs to be deposited in such a way that it grows with wurtzite (002) or c-axis orientation, which is vital for obtaining higher values of electromechanical coupling factor. The existence of orientations other than preferred orientations, such as (100) and (101) has been shown to significantly deteriorate the desired properties of AlN and hence the response of devices and sensors such as electroacoustic and pressure sensors. To harness the full potential of AlN, it is necessary to control the crystallographic orientation of the film by optimising the deposition process parameters. The process parameters, such as power, pressure, gaseous concentration and temperature, strongly affect the microstructure of AlN and consequently its piezoelectric property. The temperature is particularly important in thin film deposition, since the deposited films and the substrate materials usually possess different thermal expansion coefficients.

This section presents the effect of such parametric variations on the film quality of AlN deposited using a RF magnetron sputtering tool available in the James Watt Nanofabrication Centre, University of Glasgow. The sputtering was preferred in this work as it also allows direct deposition of AlN at temperatures compatible with flexible and plastic substrates such as polyimide. In sputtering, the substrate temperature can be controlled externally. Other tools, such as molecular beam epitaxy (MBE) and chemical vapour deposition (CVD), require high deposition temperatures, which is incompatible for flexible electronics. Moreover, considering that the final goal was to sputter AlN directly on the gate area of MOSFET, the deposition temperature has to be low enough to leave the CMOS unharmed. 400^{o}C is generally considered to be the highest temperature that can be tolerated by unpackaged CMOS processed wafers.

4.5.1. Deposition Technique

Radio Frequency (RF) sputtering was chosen for deposition of AlN. RF sputtering is a type of Plasma Vapour Deposition (PVD) process in which the plasma is generated using a RF power source. The plasma consists of positively charged ions, which are accelerated towards the negatively charged target, with an acceleration potential ranging from a few hundred to thousands of electron volts. These positive ions then strike the target with sufficient force to dislodge and eject atoms, in a line-of-sight cosine distribution and condense on the receiver substrate, that are placed in close proximity to the target, as illustrated in Figure 4.63. In order to enhance the film quality and decrease the damage due to the direct impact of atoms, a strong magnetic field is utilised near the receiving substrate area, which is why it is called magnetron sputtering. The advantage of any magnetron sputtering is that it minimises the amount of impurities and stray ions entering the film.

For the deposition of AlN, the target can be made of pure Al or AlN itself. While with the AlN target, just argon plasma is used, with the pure Al target, argon plasma in combination with nitrogen is used. The plasma cracks the nitrogen gas into nitrogen atoms which reacts with the dislodged Al atom and deposit on the substrate. In the sputtering system, there are many parameters such as chamber pressure, gas composition, power, target to substrate distance and temperature. Each of these parameter affects the film crystallographic orientation and deposition in different ways. Therefore, the sputtering process provides a greater number of process control parameters and so a variety of film quality can be achieved using sputtering. One of the most important advantages of sputtering is its temperature tailorability, which can be ranged from room temperature to 500^{o}C, which means material with a low thermal budget such as PET, PVC can also be used for depositing AlN.

For the work presented here, AlN thin films were deposited by magnetron sputtering tool, an image of which is shown in Figure 4.64. It has a primary load-lock chamber and a main chamber. The base pressure in the main chamber was about 5×10^{-8} mbar.

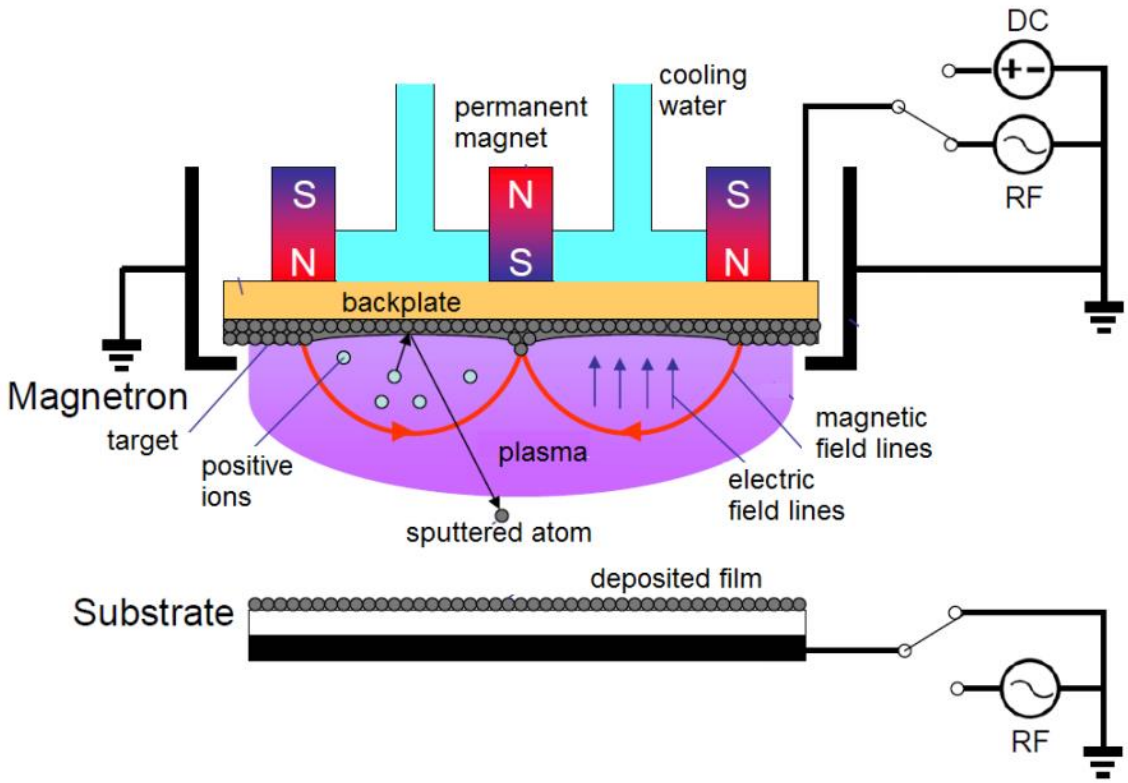


Figure 4.63: Illustration of RF sputtering system used for AlN film deposition..[206]

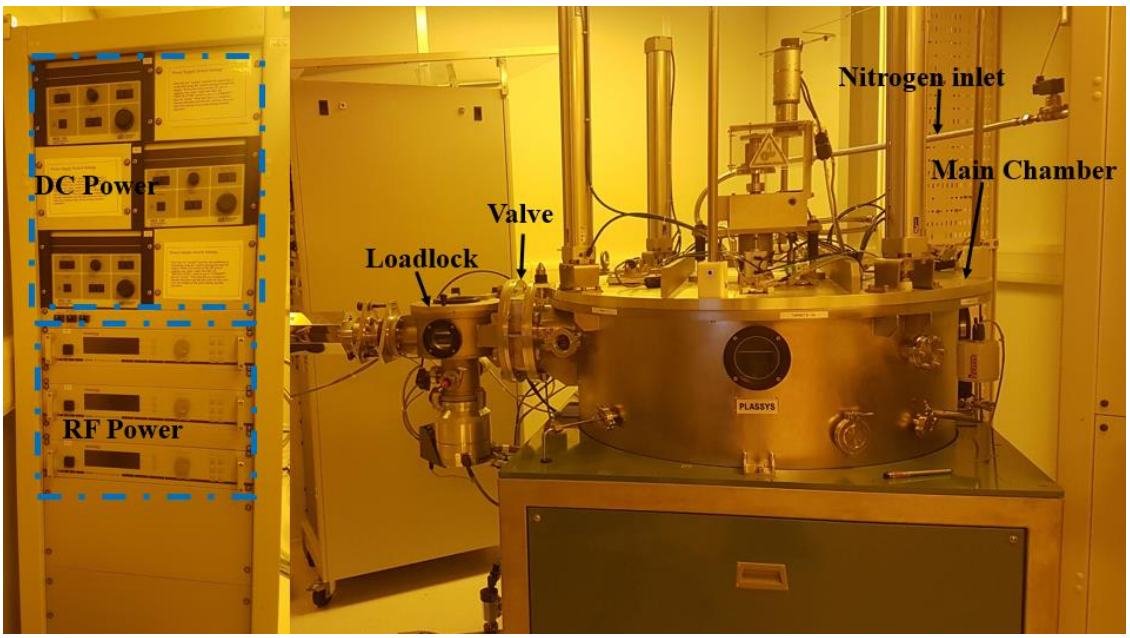


Figure 4.64: Plassys 900s tool used for AlN deposition.

The aluminium target was 6.35 mm thick and 150 mm in diameter, with a purity of 99.999%. The power was controlled using Caser RF Power Supplies.

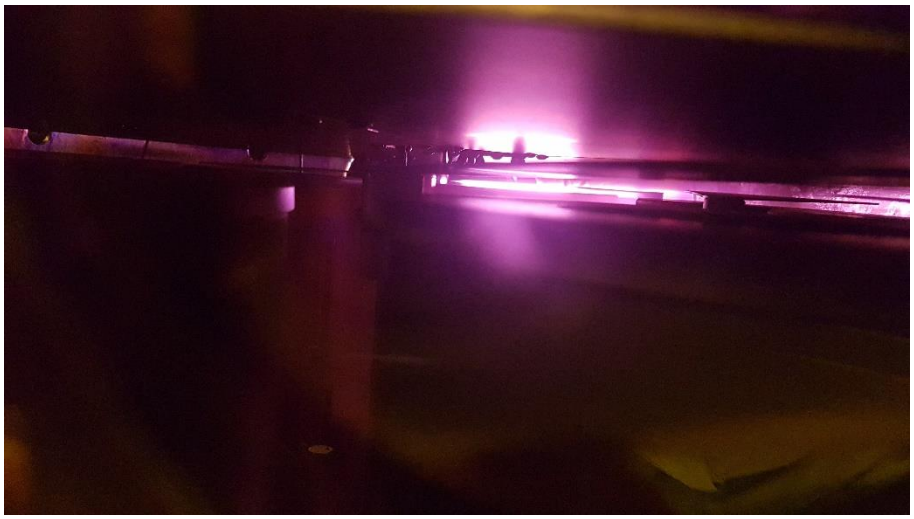


Figure 4.65: Image of plasma generated during sputtering of AlN.

The reactive and sputtering gases were high-purity Nitrogen (N_2) and Argon (Ar), respectively. The prime grade silicon wafer with (100) orientation was used as substrate and the native oxide was removed by HF dip. The substrate was then degreased using ultrasonic cleaning in acetone, isopropanol and RO water and dried in an oven at 110^{o}C to remove any moisture trace. Then, 20 nm titanium and 100 nm aluminium were deposited using a metal evaporator. For sputtering, the distance between the target and the substrate was kept constant at 59 mm and no external heating was supplied to the substrate. The sputtering was carried out for 2 hours, during which the temperature was below 80^{o}C, thus also making the process suitable for flexible substrates. Table 4.8 outlines the steps performed during the sputtering process, and which was loaded as the recipe in the tool's controlling software.

Table 4.8: Process steps for sputtering AlN

Step Type	Parameter 1	Parameter 2	Comment
Gas	Ar	100 sccm	Ramp Gas
Pressure Control	3/4/5 mtorr	1:00	Pressure Control
Wait	2:00		Wait for a fixed time
RF Plasma	RF2	300	Ramp RF generator
Wait	1:00		Wait for a fixed time
RF Plasma	RF2	500/600/700 W	Ramp RF generator
Ramp Wait	All		Wait for ramp(s) to finish
Wait	1:00		Wait for a fixed time

Pressure Control	3/4/5 mtorr	10:00	Pressure Control
Wait	2:00		Wait for a fixed time
Gas	Ar	20/30/50 sccm	Ramp gas
Wait	2:00		Wait for a fixed time
Gas	N_2	50 sccm	Ramp gas
Pressure Control	3/4/5 mtorr	10:00	Pressure control
Ramp Wait	All		Wait for ramp(s) to finish
Wait	2:00		Wait for a fixed time
Position Table	T2 RF2	0.0	Move substrate table
Wait	1:00		Wait for a fixed time
Shutter	T2 RF2	Open	Shutter Open
Wait Subproc Time			Wait for recipe time
Shutter	T2 RF2	Closed	Shutter Closed
RF Plasma	RF2	0 W	Ramp RF generator

The parameters which were varied keeping the other constants are sputtering pressure, RF power and gaseous ratio. The chamber was evacuated below the base vacuum pressure of less than 7.5 $x10^{-5}$ mtorr and the Al target was pre-sputtered in the argon atmosphere for 10 minutes to clean it from atmospheric gases impurities and to remove any target surface contamination. The recipe, with pressure 3 mtorr, 700W power, 50 sccm N_2 (sccm denotes cubic centimetres per minute at standard temperature and pressure) and 20 sccm Ar as base recipe, was chosen

Table 4.9: List of samples with various sputtering parameters

	Pressure (mtorr)	Power (Watt)	Gas ratio [%]	Thickness [nm]	Time, Distance
S1	3	700	71.4	468.7	2 hours, 59 millimetres
S2	4	700	71.4	526.4	
S3	5	700	71.4	600.9	
S4	3	500	71.4	286.1	
S5	3	600	71.4	418.6	
S6	3	700	62.5	524.2	
S7	3	700	50	588.3	

and then one parameter was varied keeping the remaining three constant. This resulted in seven samples, namely S1-S7, tabulated in Table 4.9.

The crystal structure and orientation of the deposited film was characterised by X-Ray diffraction using Panalytical X'Pert PRO MPD (A3-26) and a Bruker D8 (A4-37) diffractometer, both equipped with Cu sealed tube X-ray source λ=0.154 nm. XRD measurements were conducted at X-ray tube voltage of 40 kV and a current of 40 mA. The scan was performed for the range between 32 to 38 degrees with step size of 0.05 during theta-omega scan. The small scan size was chosen to obtain finer data points in the area of interest. The Full Width Half Maximum (FWHM) was calculated from the XRD data and then used for estimating the grain size using Scherer's equation:

$$d = \frac{0.9\lambda}{\omega\cos(\theta)} \tag{4.12}$$

Here λ is the wavelength of the X-rays, θ is the diffraction angle (in radians), d is the crystallite size, k is a constant (0.9 for AlN), and ω is the corrected full width at half maximum of the peak (in radians) [207]. The observed XRD peak at 2θ ~36.01° is assigned to (002) orientation of wurtzite AlN phase [208]. The surface morphology and roughness of the film was analysed using Atomic Force Microscopy in scanasyst mode and carried out on an area of 2 µm x 2 µm. The thickness of the film was measured using a Bruker Dektak XT height profiler by scanning the area between the masked and exposed regions. The cross-sectional images, revealing the columnar growth of film, were obtained by a scanning electron microscope (SU8240). The elemental composition of the film was analysed using an Energy-dispersive X-ray spectroscopy equipped with X-Flash Detector.

4.5.2. Effect of sputtering pressure

The XRD spectrum and rocking curves of the AlN thin films deposited under different pressures is shown in Figure 4.66(a) and Figure 4.66(b). The relative peak intensity of (002) peak was comparable to that of (100) under the pressure of 3 mtorr. Upon increasing the pressure to 4 mtorr, (100) peak decreases, which almost disappears when pressure was increased to 5 mtorr, indicating that film has better crystallinity and fine c-axis orientation. As can be observed from the spectrum, the sputtering pressure influences the preferred orientation of the film by controlling the mean free path of particle. The lower the sputtering pressure, the longer the mean free path, the higher energy the particles have and vice-versa. When particles have a longer free mean path, the chances of collision between them decreases, which results in high particle energy and gives film with high nucleation density and roughness. On the other

hand, on increasing the power reduces the mean free path of particles, which makes the particles drastically lose energy by the time they reach the substrate. Therefore, roughness and nucleation density decreases. In the pressure range, studied in this work, 3 mtorr was on the lower pressure side when the particles with higher energy arrive at substrate and introduce defects and residual stress, thus degrading (002) orientation. As pressure increases to 5 mtorr, particles lose energy while reaching the substrate and promote the growth of (002) oriented

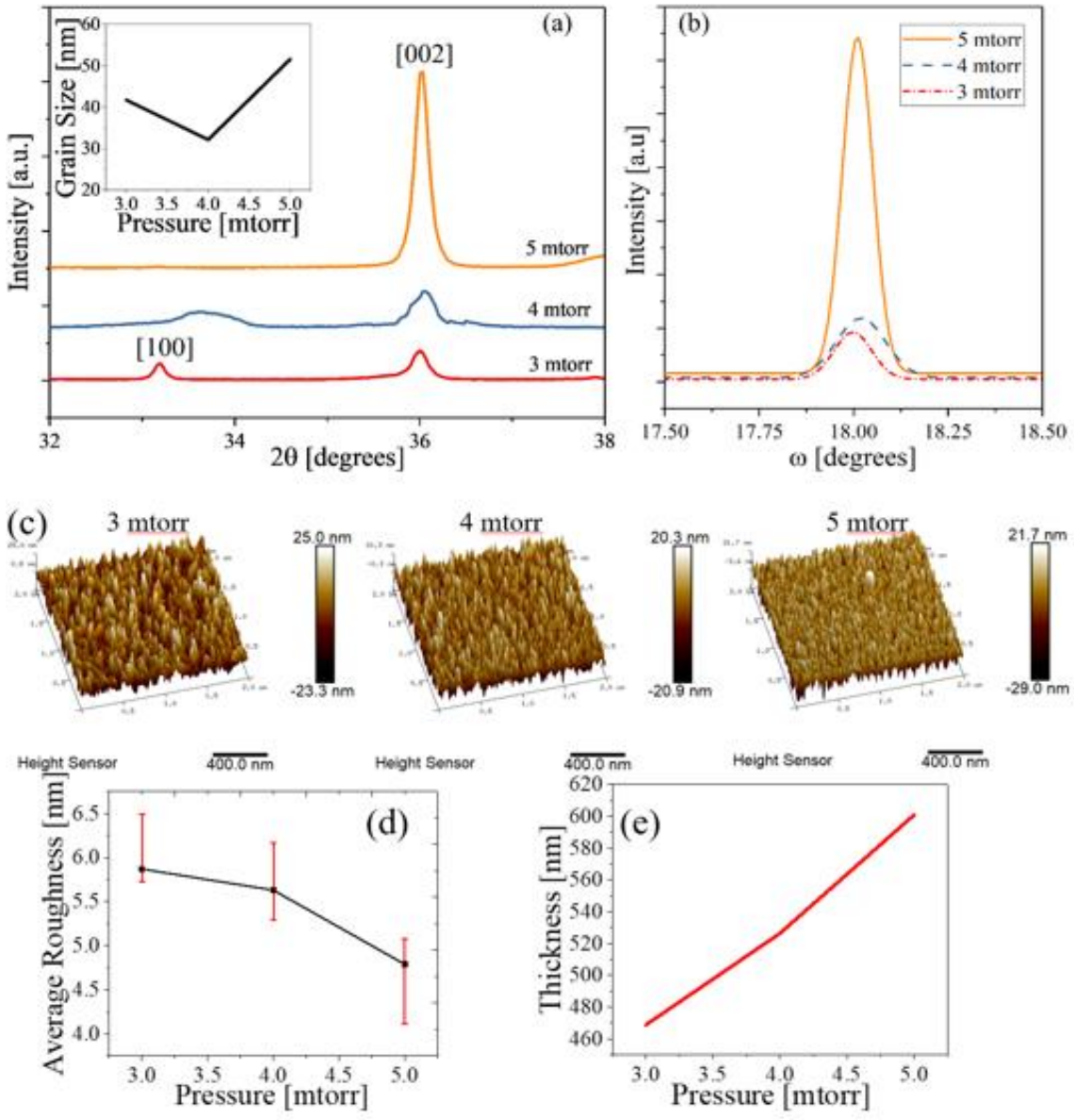


Figure 4.66: (a) XRD spectrum (b) Rocking curves (c) AFM scan (d) Roughness with statistical variation between scanned sample and (e) Thickness of AlN film deposited at various pressures.

AlN. Furthermore, the surface roughness decreases from 4.87 nm to 4.79 nm with the increasing pressure, as can be seen from the AFM scans of the samples and shown in Figure 4.66 (c) and Figure 4.66 (d).

4.5.3. Effect of sputtering power

The XRD spectrum and rocking curves of the AlN thin films deposited under different sputtering power is shown in Figure 4.67(a) and Figure 4.67(b). As can be seen, increasing the power leads to degradation of (002) peak and emergence of (100) peak. Therefore, it can be said that (002) was the preferred orientation at low power in the studied power range. The higher power degrades the film quality, since it damages the orienting film due to bombardment of high-energy particle. During the sputtering process, the Ar ions not only bombard the target, but also the growing thin films. Thus, when the sputtering power is high, Ar ions hold greater

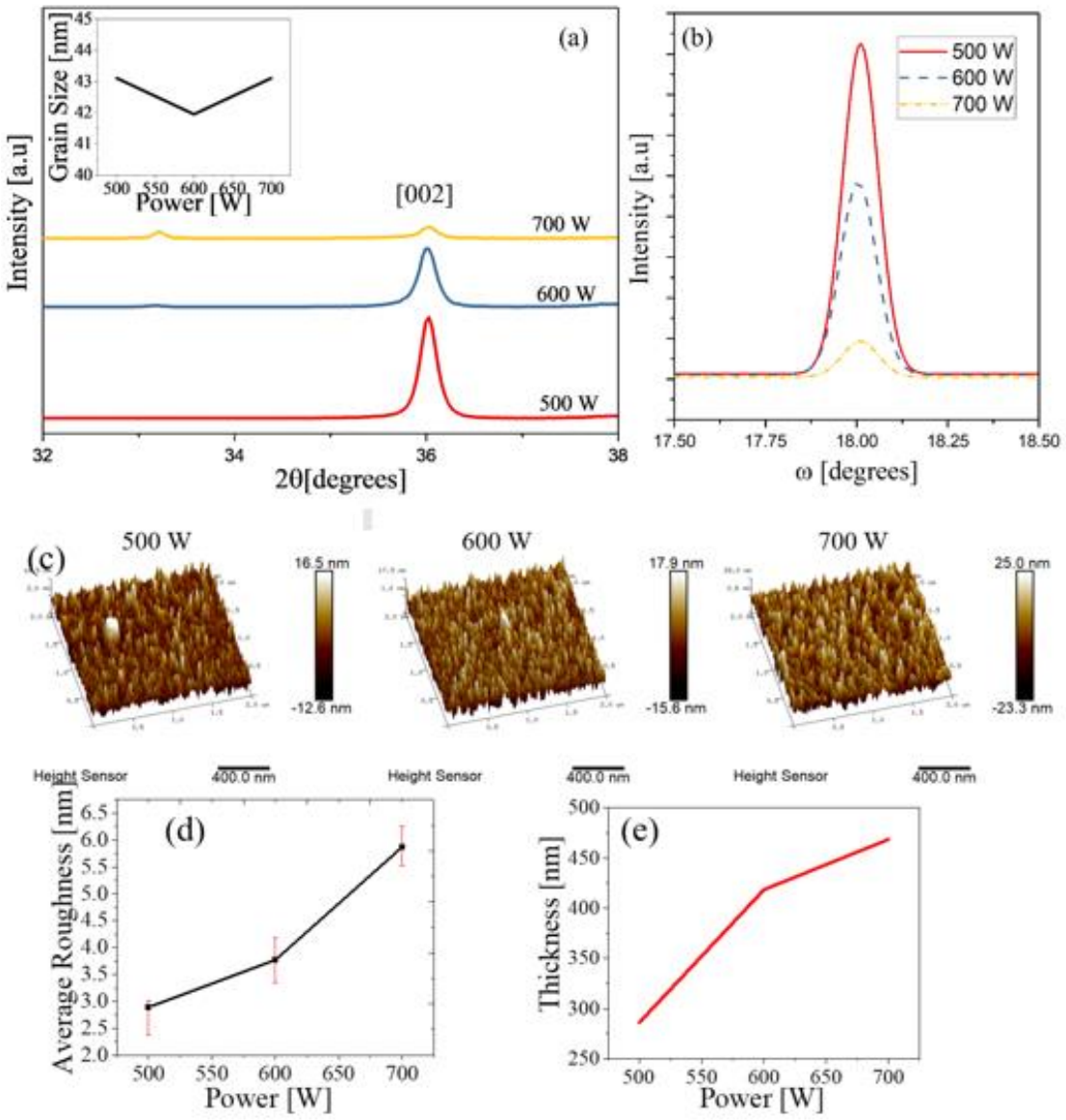


Figure 4.67: (a) XRD spectrum (b) Rocking curves (c) AFM scan (d) Roughness with statistical variation between scanned sample and (e) Thickness of AlN film deposited at various power.

energy, which leads to the rougher surface of the growing thin film, as can be observed from Figure 4.67(d) where roughness increases from 2.89 nm @500W to 4.87 nm @700W. Moreover, the large contribution to the surface migration and surface reaction from the high-energy particles' incident energy leads to the increase of the average surface roughness with increasing the RF power. The growth rate of AlN films increases almost linearly with an increase in sputtering power, since higher plasma power results in a higher number of ejected Al particles from the target, which leads to an increase in film thickness, as shown in Figure 4.67(e).

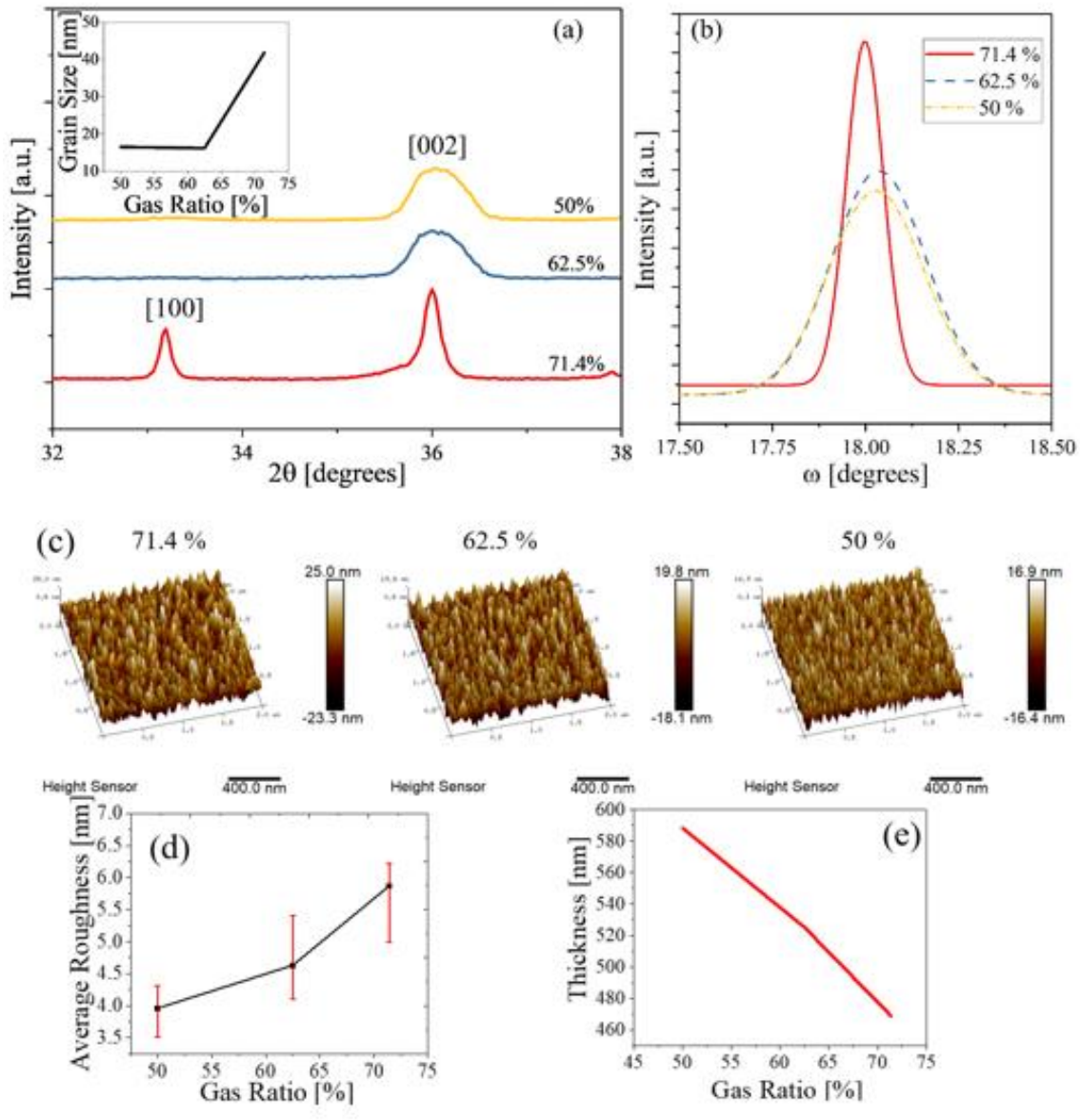


Figure 4.68:(a) XRD spectrum (b) Rocking curves (c) AFM scan (d) Roughness with statistical variation between scanned sample and (e) Thickness of AlN film deposited at various gas ratio.

4.5.4. Effect of gaseous composition

During any compound sputtering process, there are two types of gases, inert and reactive. Argon is the preferred choice for inert gas and its role is to ionise and bombard the target material. Nitrogen is the reactive gas when the nitride of the target material is needed, which is the case here with AlN. The Al particles that came out of the target reacts with the reactive gas, while migrating towards the substrate and get deposited. Since reactive gas is chemically consumed to form the desired product compound, it is beneficial to have an excess of reactive gas in the sputtering chamber. Therefore, against the traditional approach of varying nitrogen, it was kept constant at 50 sccm and the argon flow rate was varied, and the gas ratio is defined

as $\frac{N_2}{N_2+Ar_2}$. To study the effect of gas flux on AlN film quality, the argon flow rate was increased from 20 sccm to 50 sccm, thus reducing the gas ratio. Figure 4.68 (a) and Figure 4.68 (b) shows the XRD spectrum and rocking curves obtained at three ratios, 71.4%, 62.5% and 50% respectively. It can be observed that a higher value of the gaseous ratio is favourable for (002) oriented film growth, since a lesser number of argon ions will eject a lesser number of aluminium particles, and most of them will react with the nitrogen, and so aluminium particles can be considered as a rate limiting reactant. The lesser number of product species prefers more ordeal deposition, leading to (002) oriented film. Moreover, on increasing the argon content (i.e. decrease of gas ratio), the thickness of film increases as shown in Figure 4.68 (e), as more argon produces a larger number of reacting species. The surface roughness decreases as the gas ratio decreases, as shown in Figure 4.68 (d) where roughness decreases from 4.87 nm @71.4% to 3.96 nm @50%, due to the fact that a lesser number of energetic particles of aluminium can reach the depositing film to damage it by impingement.

4.5.5. Sensor fabrication

With the optimised parameters (500W, 5 mtorr, 50 sccm N_2 and 20 sccm Ar), a piezoelectric capacitor was fabricated over silicon as carrier substrate. A silicon wafer was cleaned with acetone, isopropanol and DI water before loading for bottom metal deposition. Then, 20 nm titanium and 100 nm aluminium were evaporated using an electron beam evaporator, followed by RF reactive sputtering of AlN. The cross-sectional picture showing the columnar growth is displayed in Figure 4.69 (a). EDX and XRD analyses were also carried out to confirm the film composition and orientation and, as can be seen from Figure 4.69 (b), the film was composed mainly of aluminium and nitrogen with high (002) orientation. Finally, the top electrode was realised by evaporating 20 nm nichrome and 100 nm gold and Figure 4.69 (c) shows the picture of the fabricated sensor.

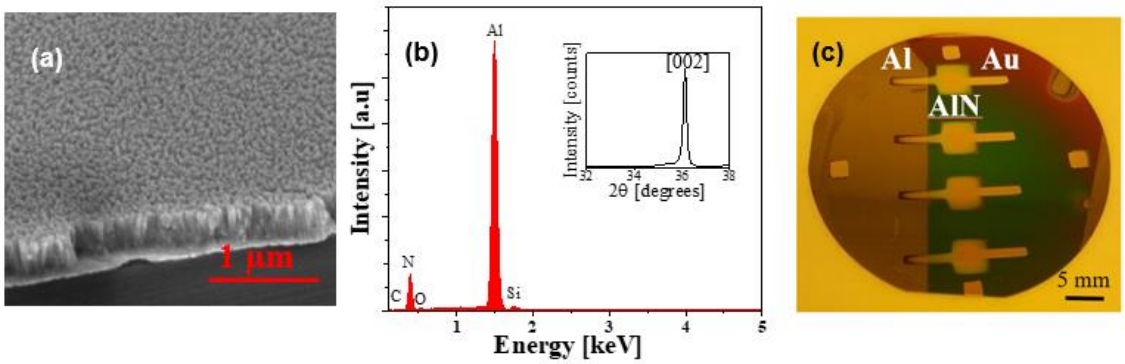


Figure 4.69: (a) Cross-sectional SEM image of AlN showing the columnar structure of grains. (b) EDX and XRD (inset) spectrum of AlN sputtered using optimised recipe (c) Picture of fabricated AlN piezocapacitor on silicon wafer.

4.6. Direct Deposition of AlN on MOSFET

After optimising the recipe for AlN sputtering, the next step was to deposit it directly on the gate metal of MOSFET. The top electrode mask was designed as dark data and to be used with positive resist, it would require the etching of metal to pattern it. However, this was not possible with AlN, since the etching chemistry of AlN is similar to aluminium and thus can very well adversely affect the aluminium, which was gate metal, So, a new process has to be established for the successful deposition of AlN on gate area of MOSFET and the subsequent top metallisation layer.

Since the mask was already fabricated, it was decided to use the same mask but with negative resist. This process generated a pattern in the resist which could be used as lift-off pattern for the AlN and Au. MaN-1420 was spin coated at 3000 rpm for 30 seconds and exposed for 16 seconds to develop the slope profile needed for lift-off. The exposed sample was developed in ma-D 533S for 90 seconds. The optical images taken after development are shown in Figure 4.70 (a-b), where light turquoise colour represents the developed area where AlN gets deposit.

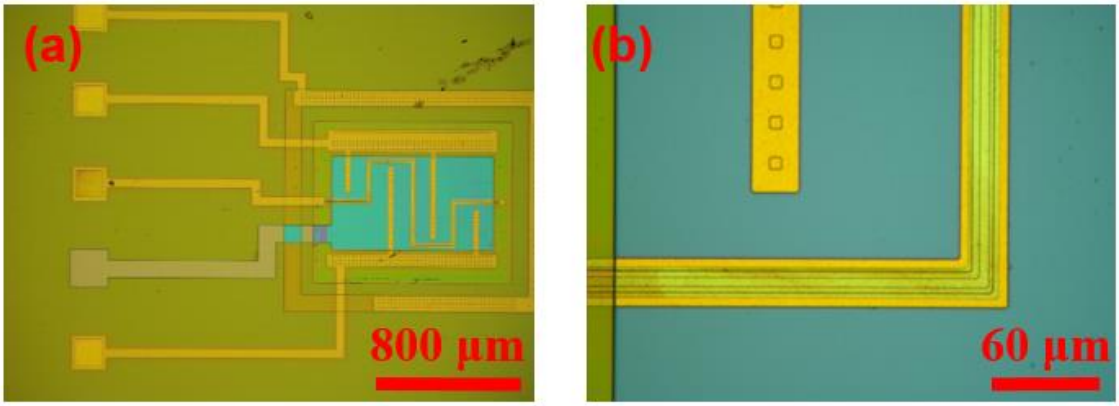


Figure 4.70: Optical image of chip showing the patterned resist before AlN sputtering at different magnification level. The blue area in (a) is the top gate area which receive the sputtered AlN.

Using this recipe, a lift-off pattern was realised on the chip having just bottom metal i.e. a structure which resulted in a MIM capacitor upon sputtering of AlN and top metal deposition. This was done to optimise the sputtering and lift-off conditions. AlN was sputtered using various sputtering parameters, and then NiCr/Au of thickness 20nm/150 nm was evaporated using Plassys 2. Figure 4.71 shows the SEM picture of the sample after sputtering.

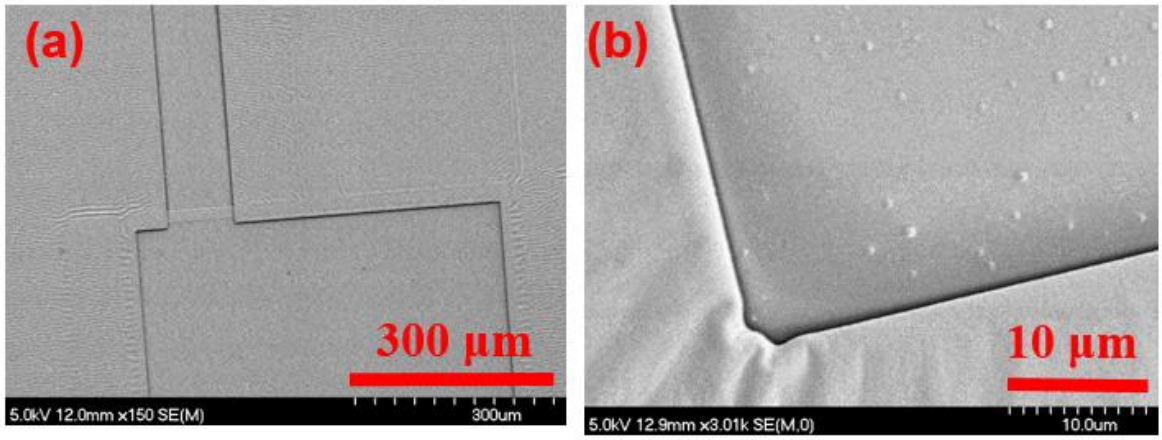


Figure 4.71: SEM images of the resist pattern after AlN sputtering. Due to the sputtering power, ripples and re-flow of resist can be observed at the edges.

The sputtered sample was soaked in SVC-14 (which contains DMSO) overnight for lift-off. However, it was observed that plasma produced during sputtering is affecting the resist and making it hard to lift-off. As can be seen from Figure 4.72(a-b) which shows the SEM image of resist after sputtering, a clear wavy pattern was observed, showing the plasma effect on resist. Also, the optical picture shows that even after overnight soaking, no lift-off occurred.

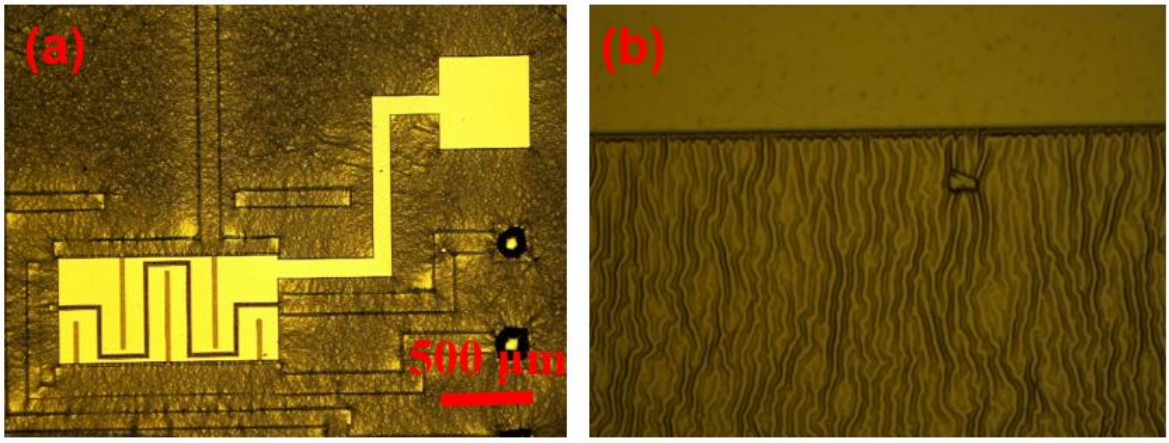


Figure 4.72: Optical images of chip after sputtering at 700W and overnight soaking in SVC-14. No lift-off of the AlN happened, as can be observed from the pictures.

In the second run, power was reduced from 700W to 500W. This reduction, on the one hand gave better (002) orientation of AlN, as discussed above, and led to a lesser damaging impact on resist. Nevertheless, manual scrubbing using a micro-swab had to be used after a short sonication, to remove resist from the contact pads. Figure 4.73(a-b) shows the image of the chip after cleaning and, as can be seen, there was still a considerable amount of residues remaining on the chip. In the third test, before the sputtering, a blank flood exposure and hard-bake was given to the sample, which helped to increase the crosslinking degree and the thermal stability of resist patterns. The sputtering was performed at reduced power of 500W and soaked in Microposit Remover 1165 and SVC-14. After a quick sonication and some swabbing, a considerable amount of residue was removed.

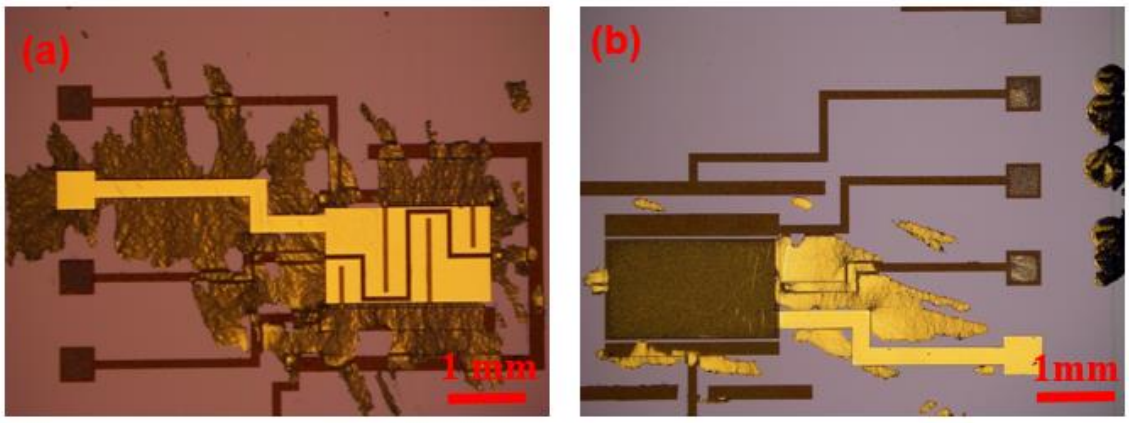


Figure 4.73: Optical image of chip after (a) sputtering at 500 W (b) UV exposure, hard bake and sputtering at 500 W. The chip had significant amount of residues attached near the active area of MOSFET.

In the final test, after the hard bake, a thin layer of aluminium was evaporated at a slow rate (~0.03 nm/min). The metal layer was beneficial for the lift-off as it acted as a buffer and heat dissipation layer, thus protecting the resist to a certain extent from getting damaged. This step resulted in a much better degree of lift-off with sharp patterns and minimum residue, as can be seen from the optical image shown in Figure 4.74.

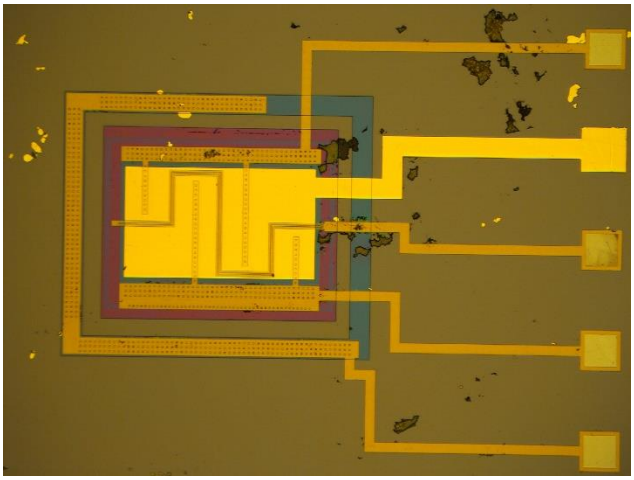


Figure 4.74: Optical image chip after sputtering over pre-deposited thin Al film followed by lift-off. The chip was clean with some minor residues attached at the edges.

4.7. Conclusion

Piezoelectric materials are an attractive choice as the transducer layer for tactile sensors, and this chapter presented the work done to develop two piezoelectric materials. The focus was on such piezoelectric materials which can resolve the challenges associated with P(VDF-TrFE) i.e. unwanted sensitivity to temperature and requirement of poling. In this direction, firstly, a piezoelectric composite which comprised the advantages of both, polymer and filler, was developed using P(VDF-TrFE) and BT. Since, the polymer and filler exhibits opposite piezo and pyroelectric properties, it was possible to suppress the sensitivity to temperature arising due to pyroelectric behaviour, by using appropriate poling condition. The variety of tests conducted on the composite showed enhancement in dielectric properties and β-phase due to addition of BT nanoparticles. The composite was then used as sensing layer in capacitive structure on flexible polyimide foil.

In the second part, AlN, which is a structurally piezoelectric material, and does not require any poling, has been presented. The extensive parametric variation during the sputtering process

resulted in highly c-axis oriented piezoelectric film. The XRD analysis carried out on the samples, showed strong peak of (002) orientation for majority of samples. The optimised recipe was used to fabricate a capacitive structure and the film exhibited piezoelectric coefficient of 5.9 pC/N. Following this, the direct deposition of AlN on the processed chip was carried out, and the challenges and their solution concludes this chapter.

Chapter 5. Post-Processing Techniques for Thinning Silicon

This chapter presents various thinning methodologies and improvement techniques employed to realise ultra-thin silicon. With the main focus on alkaline wet etching, some preliminary work done using dry etching and grinding is also presented. The optimised process was employed to for wafer-scale and chip-scale etching, in order to achieve devices over thin silicon so that they can conform over flexible substrate. The two-step transfer process adopted for transferring thin silicon on to flexible substrate ensured the mechanical stability of the chip during the transfer. The encapsulation between the two layers of PDMS or PVC, kept the sample in neutral plane, which is critical to get lower bending radius.

5.1. Wet etching of silicon in tetra methyl ammonium hydroxide

Compared to grinding and dry etching, wet etching of silicon is relatively economical and free from the issues of micro-cracks. Moreover, it provides a higher degree of selectivity, and is often faster. TMAH, as the etchant for silicon, has many advantages, such as high selectivity to thermal oxide, very smooth etched surface, IC compatibility and batch scale reproducibility. Establishing the process of wet etching of silicon with TMAH was thus the first goal.

Nevertheless, it is important to discuss the various research areas and challenges associated with silicon etching using TMAH.

5.1.1. Mechanism of Si etching in TMAH

The mechanism of anisotropic etching of Si is as follows: Two hydroxide ions from etchant solution bind with two dangling bonds of Si atom on an exposed surface, thus injecting two electrons into the conduction band.

$$Si + 2OH^- \rightarrow Si(OH)_2^{++} + 2e^- \quad (5.13)$$

Following this, the Si-Si bond between the two neighbouring lattices is broken to obtain a positively charged and soluble Si complex.

$$= SiHOH + OH^- + H_2O \rightarrow = Si(OH)_2 + H_2 + OH^- \quad (5.14)$$

The complex formed between silicon and hydroxide further reacts with two more hydroxide ions to give orthosilicic acid, which leaves the solid surface by diffusion.

$$(\equiv Si)_2 = Si(OH)_2 + 2OH^- \rightarrow 2(= Si - H) + Si(OH)_4 \quad (5.15)$$

However, due to the high pH of the solution it forms a soluble complex and water molecule.

$$Si(OH)_4 + 2OH^- \rightarrow SiO_2(OH)_2^- + 2H_2O \quad (5.16)$$

The excess electrons which were produced in the first step now attack the water molecule to produce more hydroxide ions and hydrogen gas.

$$4H_2O + 2e^- \rightarrow 4H_2O^- \rightarrow 2OH^- + 2H_2 \quad (5.17)$$

The overall reaction is represented in Equation (5.6) as:

$$Si + 2OH^- + 2H_2O \leftrightarrow SiO_2(OH)_2^- + 2H_2 \quad (5.18)$$

5.1.2. Anisotropy in etching

In anisotropic etching, the etch rate is dependent on direction and in the case of silicon it is the plane directionality associated with the crystal structure of silicon which has different rates of etching. Etch rates vary with different crystallographic orientations due to the atomic bonds formed at the surface silicon atoms. Wafers with a (100) orientation present superficial atoms with two backbonds, linking to two underlying silicon atoms, and two dangling bonds. These dangling bonds are capable of being attacked by nucleophilic species of etchant, i.e. hydroxyl ions. The energy required to break these bonds to release silicon-hydroxide compound is different for different planes and is summarised in Table 5.6.

Table 5.6: Experimental data for binding energy of silicon planes

Crystal plane	Interplaner distance (A^o)	Binding energy (eV)
(100)	5.43	1.13
(110)	3.84	2.25
(111)	2.35	6.02

The lower the energy requirement, the higher the etch rate of that specific plane. Anisotropic etching of (100) silicon wafer can produce either vertical (100) walls or sloping

(110) or (111) walls, inclined at 45^o or 54^o respectively. The level of anisotropy also depends on the concentration of etchant and the presence of any additive in it[65]. For checking the extent of anisotropic behaviour, a (100) Si was etched with SiO_2 as mask, for 1 hour in 25% TMAH solution. The SEM images shown in Figure 5.75 clearly show the sidewalls due to (111) plane creating an almost 54^o edge with the (100) bottom surface.

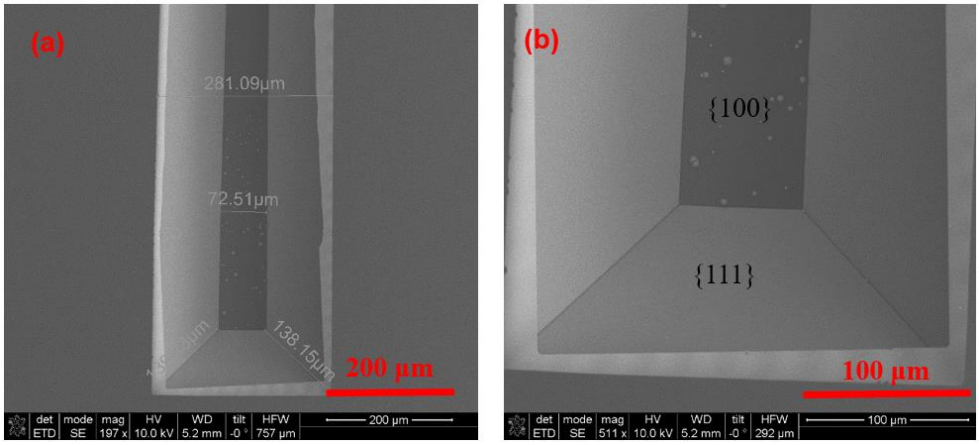


Figure 5.75: SEM images after etching of silicon showing the anisotropic behaviour of process.

5.1.3. Effect of TMAH concentration on etch rate

The concentration of solution plays an important role in deciding the etch rate of silicon. It is well accepted that etch rate of silicon increases as TMAH concentration decreases [209]. When the TMAH is doped with Si, the pH value of the bulk solution decreases, i.e. the number of hydroxyl ions decreases. This could happen through dissociation of weak acid formed during the intermediate stage. However, it is observed that etch rate increases for TMAH doped with Si, signifying that hydroxyl ions from bulk the solution probably do not contribute to the etching mechanism. Therefore, the hydroxyl ions necessary to dissolve silicon must be produced on the Si surfaces, and it has been proposed that water dissociates to form the etching ions, thus also strengthening the fact why etch rate increases with decrease in TMAH solution concentration. The lower concentration of TMAH (~5 wt%) can give an etch rate of upto 60 µm/hr at 80^{o}C, but due to the vigorous nature of the reaction, surface roughness is very high. Therefore there is a trade-off between etch rate and surface roughness. An ideal concentration which is used in most of the cases for bulk micromachining is 25% solution, which can give etch rate upto 40 µm/hr at 80^{o}C. This can

be seen from the scan profile in Figure 5.76 where Si(100) was etched in 25% TMAH for 2.5 hour at 85°C, giving a step 142 µm, thus etch rate of 58.8 µm/hr.

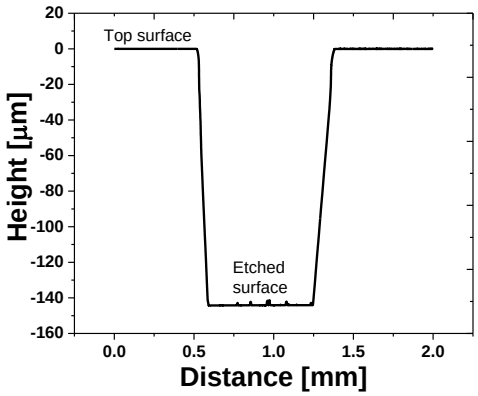


Figure 5.76: Scan profile of etched pattern in 25% TMAH.

5.1.4. Hillock formation and surface roughness

Hillocks are small pyramidal structures which are observed during anisotropic etching of silicon. Their formation during Si (100) etching is a consequence of the high anisotropic dissolution ratios, with (100) and (110) surfaces dissolving much more rapidly than the (111) plane. This leads to exposing of the slower etching (111) planes that constitute the sides of pyramidal features. At low magnification, the hillocks appear as regular pentahedrons composed of four lateral (111) crystallographic planes resting on the (001) base plane, as can be seen in Figure 5.77

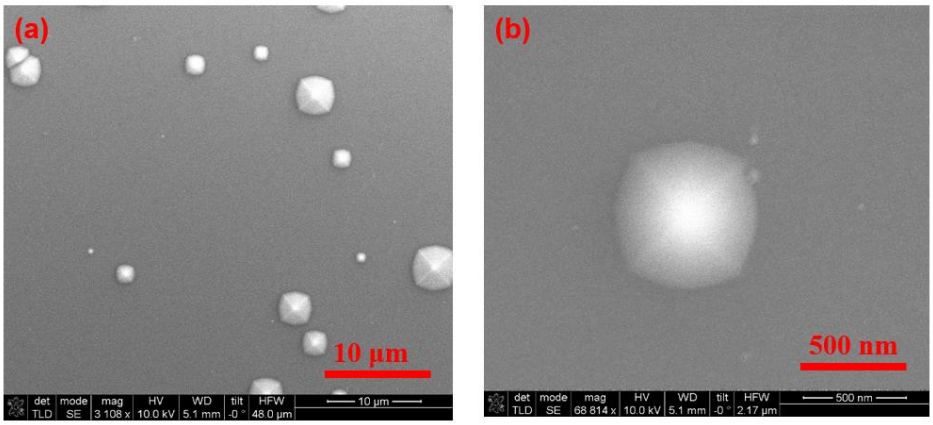


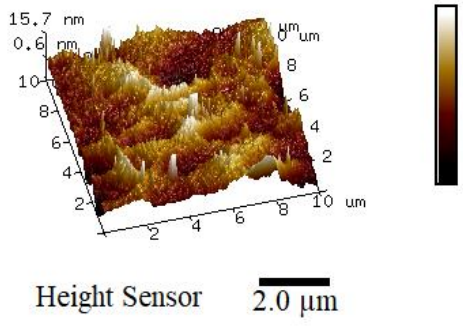
Figure 5.77: SEM images of hillocks formed during etching.

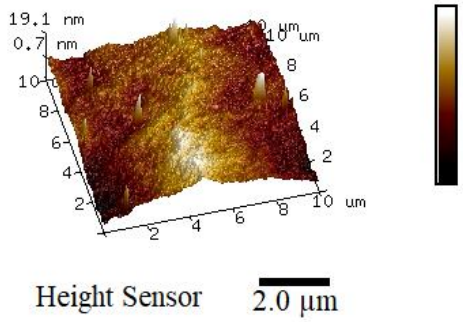
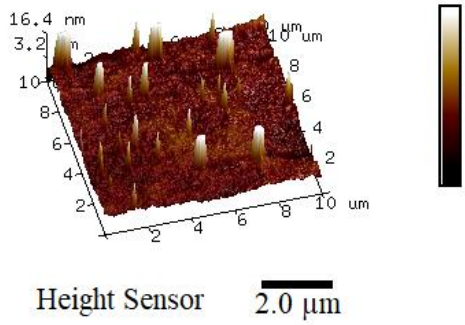
The formation of hillocks can be affected by many factors, such as etchant composition, concentration, temperature, agitation and dopants. The presence of hillocks leads to stress localisation and can cause breakage during thinning, so it is beneficial to reduce the hillock density. One simple way is to agitate the solution, which leads to dispersion of unpolymerised reaction products into the etchant, which could otherwise mask the reaction at random sites. Moreover, looking at the equation (5.6) which is reversible reaction, i.e., the forward reaction is the etching process and the reverse reaction results in re-deposition of silicon on the substrate. This redeposited particle can nucleate the hillock formation.

Another way to reduce the hillock formation is by using high concentration TMAH (above 22%) [210]. This is due to the fact that the anisotropic etching is quite sensitive to the dissolved Si content. The lower the TMAH concentration, the higher the Si content and at a high level of dissolved Si content, the (101) plane is etched much more slowly than (100) plane. [211].

The hydrogen bubble formed during reaction is also one of the reasons which can produce the micro-masking effect and leads to preferential formation of pyramidal structure. There are reports of solving this issue by adding isopropanol in varying concentration ratios [212]. In order to analyse these effects, some tests were carried out using a double-sided polished silicon sample. In the first case, the sample was etched for 1 hour in pure 25% TMAH without any agitation and in the second case with mechanical stirring.

Table 5.7: AFM scan images and surface roughness values of etched samples.

	AFM scan	Roughness values
Case I: 25% TMAH No agitation		Rq = 4.29 nm Ra = 3.35 nm

Case II: 25% TMAH With agitation		Rq = 4.93 nm Ra = 3.83 nm
Case III: 25% TMAH With agitaion IPA doped		Rq = 3.14 nm Ra = 1.48 nm

For the third case, the same etchant was used and 10% IPA was added and the new sample was immersed for one hour with stirring. The etching was carried out at 80^{o}C, and as can be observed from the AFM scan tabulated in Table 5.7, the surface roughness follows the discussion.

5.1.5. Aluminium protection

Aluminium is one of the most important metals used for metallisation and interconnection on a chip. TMAH is corrosive to aluminium and any leakage on frontside during back etching could destroy the metal layer, leaving the chip useless. Thus, it becomes important to prevent aluminium from coming into contact of the etchant for a longer duration and even if it does, the etchant can be chemically modified to prevent it from attacking the aluminium. This can be achieved by doping TMAH with silicon or silicic acid. This addition passivates the exposed aluminium layers and makes it resistant to the action of the etchant. The process is occur to happen in two steps: First, the silicates in the solution will contribute to the formation of aluminosilicates on the exposed aluminium layer, which are less soluble at moderate pH levels. Second, the pH level of the doped solution is decreased,

increasing the lifetime of the aluminosilicate passivation layer. This could be solved by adding oxidising agents such as ammonium persulfate, which decreases the extent of hillock formation.

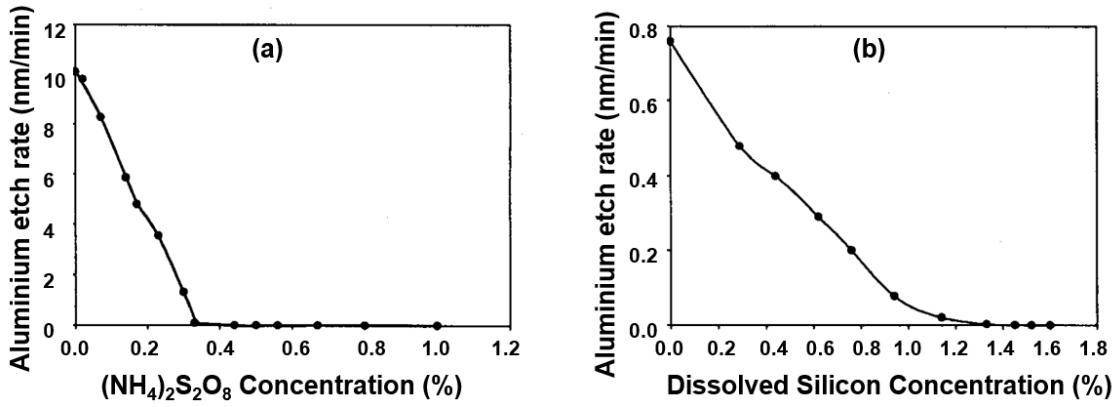


Figure 5.78: The aluminium etching rate as a function of (a) $(NH_4)_2S_2O_8$ concentration (b) dissolved silicon concentration. [213]

5.2. Ultra-thin silicon based piezocapacitor

5.2.1. Piezocapacitor fabrication

In order to optimise the etching setup, a 6 inch mask was designed, consisting of capacitor's electrode of different shapes and sizes, as shown in Figure 5.79(a). The same mask was used to pattern both the bottom and top electrode. The capacitors were fabricated on a (100) double-sided polished 6 inch p-type silicon wafer with resistivity 10-20 ohm-cm and initial thickness 636 µm.

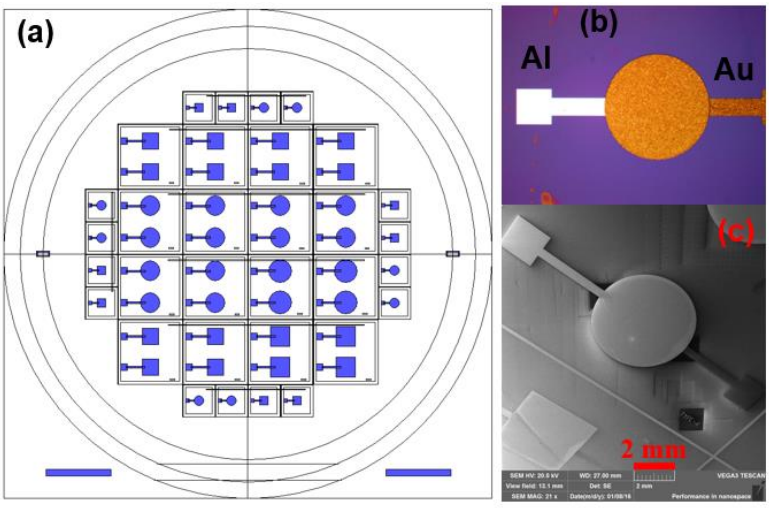


Figure 5.79: (a) Mask layout for piezocapacitor fabrication. (b) Optical (c) SEM image of fabricated device.

As shown in Figure 5.80, the process starts with depositing silicon oxide-silicon nitride-silicon oxide stack by Low Plasma Chemical Vapour Deposition (LPCVD) method. The stack is composed of 1200 nm SiO_2, 80 nm Si_3N_4 and 800 nm SiO_2. This stack acts as an etch mask during wet etching and the etching window was patterned using fluorine chemistry in Tegal 903. On the frontside, 600 nm thick aluminium was deposited via sputtering and patterned to make the bottom electrode of the capacitor. Commercially available P(VDF-TrFE) pellets were dissolved in RER 500 solvent using a magnetic stirrer at 80^0C to obtain 10 wt% solution. The solution was spin coated over the patterned wafer and the thickness measured with an optical interferometer, was found to be 2µm. Since the piezoelectric property of polymer depends on its crystal structure, the crystallinity of PVDF-TrFE was improved by annealing the polymer film in nitrogen atmosphere. 150 nm thick gold was evaporated and patterned to realise the top electrode of capacitor. Following this, the P(VDF-TrFE) was etched using oxygen plasma in Tegal 903. The metal covered with resist acted as the protection mask for PVDF-TrFE etching. The optical and SEM image of the piezoelectric capacitive structure over bulk silicon is shown in Figure 5.79(b-c).

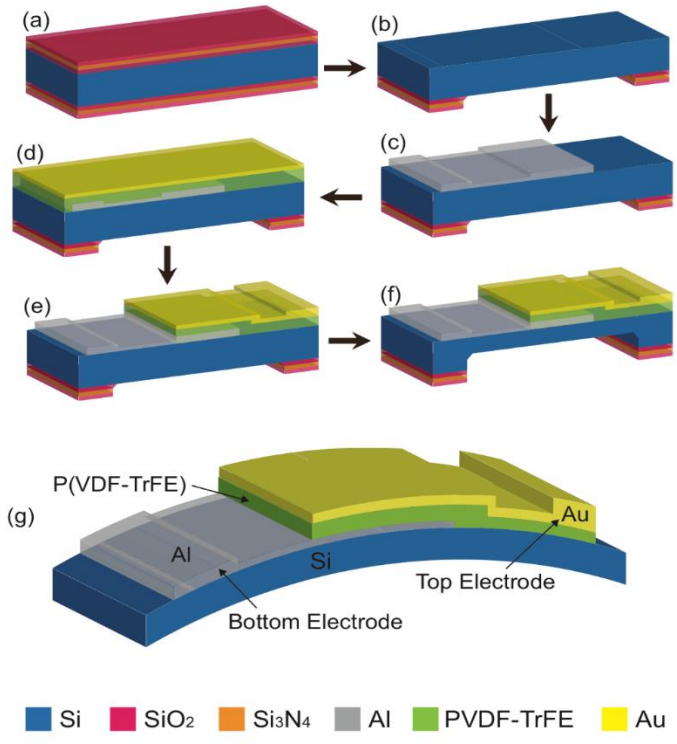


Figure 5.80:Illustration of process steps followed for realising ultra-thin silicon based piezocapacitor.

5.2.2. Post-processing

Once the front end fabrication had been conducted, post processing was carried out to realise ultra-thin capacitive structure. Then wafer was carefully loaded in the AMMT GmBH wafer holder (shown in Figure 5.81(a). 3 O-rings and 8 nuts arrangement was used to avoid any etchant sipping to the front side. The etching bath was made from a double-walled glass vessel, and the space in between was filled with a mixture of glycol and water, so the etchant was heated by convection of the circulating solution. The heating was controlled using an external controller and the temperature of the etchant was controlled through closed loop feedback. Figure 5.81(b) shows the etching setup used in this process. The sample was immersed in 25% TMAH solution at 80^0C and etching was carried out in two turns, with timse of 8 hours and 7.5 hours respectively.

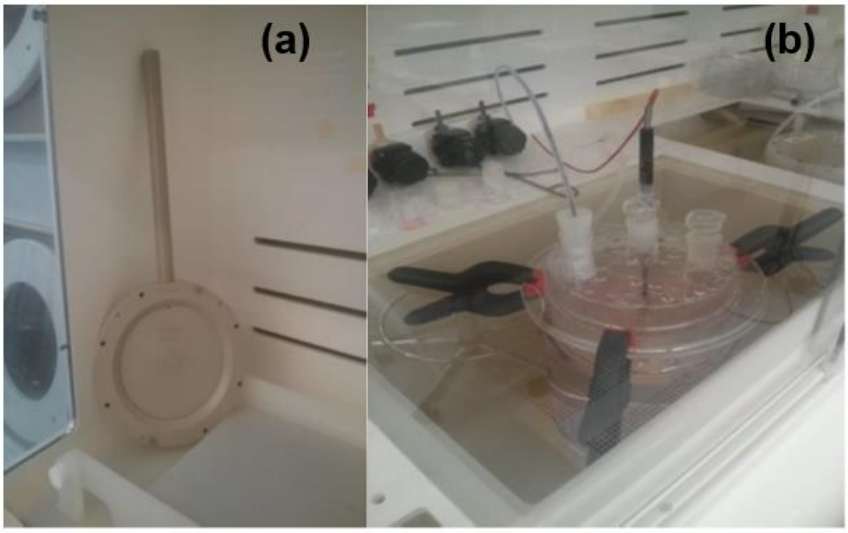


Figure 5.81: (a) AMMT holder (b) Wet etch setup used for chemical etching of 6 inch wafer.

Following the thinning, the holder was carefully taken out and placed in a warm water bath to avoid any thermal shock. Once the wafer had cooled down to room temperature, it was thoroughly cleaned and dried. Figure 5.82(a) shows the wafer's backside after the etching and Figure 5.82(b) shows the optical picture of the backside, where etch pits can be clearly observed. The next challenge was to separate the thin chips. Here, two techniques were investigated, which resulted in a good yield of thin chips: (i) Polyethylene terephthalate (PET) supported dicing (ii) Dicing before wet etching.

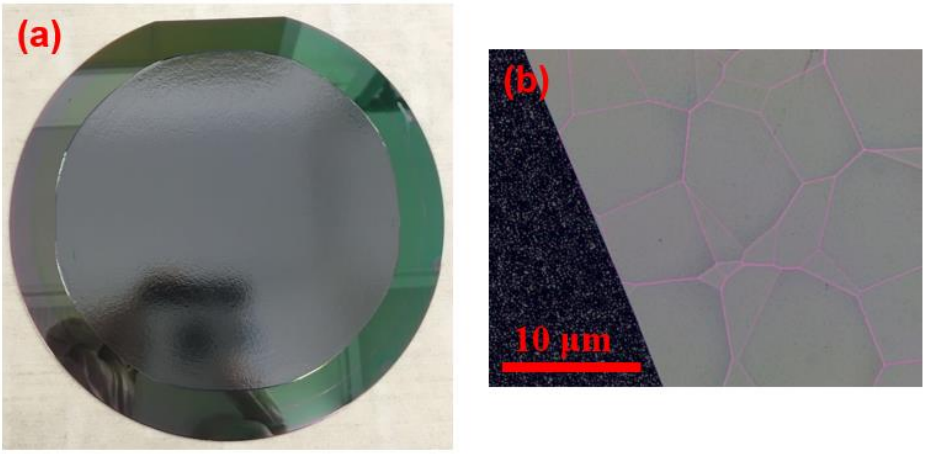


Figure 5.82: (a) Backside image of thinned wafer (b) Optical image of backside showing the etch pits.

5.2.2.1. PET supported dicing

During dicing, the sample to be diced underwent extreme conditions due to blade pressure and coolant stream flow, which is why the thin silicon membrane supported on the bulk ring achieved after post-processing cannot be diced conventionally. In order to tackle this issue, a PET sheet was used to provide mechanical support to the thin wafer. A 3D printer was used to cut a circular disc shape PET, with thickness the same as the etch depth.

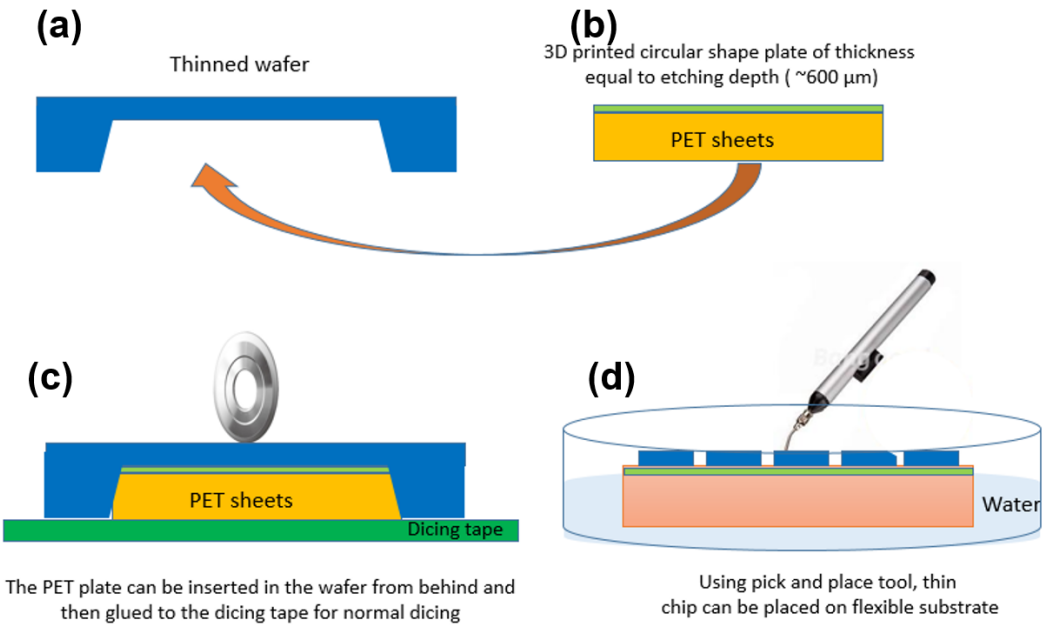


Figure 5.83: Illustration of PET supported dicing.

For attaching this disc to the wafer, a water soluble binder, polyvinyl alcohol (PVA) was chosen, in order that the thinned separated thin chip could be easily released after dicing. PVA pellets were dissolved in water at an elevated temperature (70^{o}C) and the PET disc was plasma treated for one minute to decrease the surface hydrophobicity.

The thinned wafer was carefully placed over the disc in such a manner that the etched part aligned well with the disc, and was then left for drying in an ambient atmosphere. Once glued well, the combination of the thin wafer and the PET disc was attached to the dicing tape and frame. The dicing was carried out using a fine grit size saw blade and PVA glue ensured that the chip did not detach during dicing. Afterwards, the diced sample was immersed in warm water to dissolve the glue, and as can be seen from Figure 5.84 (a-b), the thin chip detached automatically after some time and floated up to the surface.

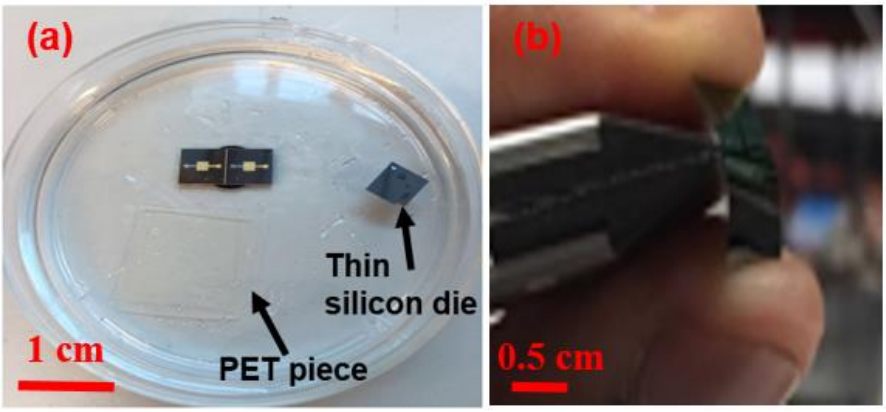


Figure 5.84: Image of (a) thin chips in water after dicing (b) Bendable chip.

5.2.2.2. Dicing before Wet etching

In this technique, instead of dicing after etching, it was performed before the wafer was loaded in the holder for etching. This gave two advantages: (i) no need of PET and PVA, (ii) thickness of chip can be pre-decided. Following the front end fabrication, the wafer was partially diced after fixing it to the dicing frame. The dicing depth decided the final thickness of the thin chips. When the etching depth reached the cut depth, die separation occurred automatically. Due to the capillary action, the chip remained stuck to holder and did not fall into the solution. The holder with separated chips was immediately taken out of the TMAH bath, and rinsed and dried.

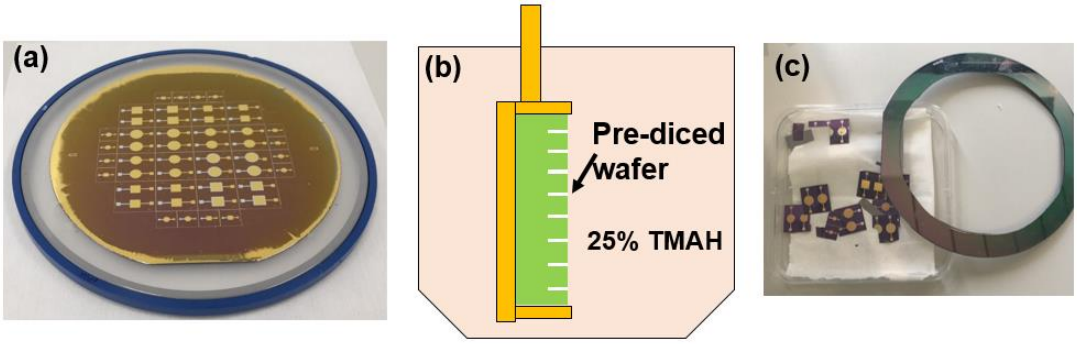


Figure 5.85: (a) Pre-diced wafer (b) Illustration of dicing before etching process (c) Image of separated chips and outer ring.

5.2.2.3. Laser Dicing

Laser dicing of the thin silicon wafer, as discussed in Chapter 2, provides kerfless and chipping free diced samples. Before exposing the thinned wafer to the laser machine, a polyimide foil was attached to the back of the thinned wafer. This provided the mechanical support during the dicing and also reduced the warpage immediately after dicing. A focused beam laser was then used to dice the wafer, and images following dicing are provided in Figure 5.86(a-c).

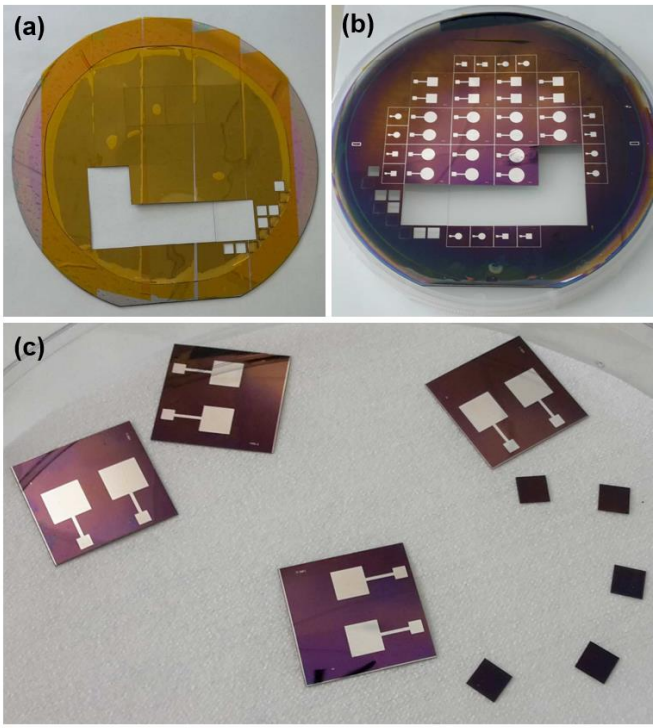


Figure 5.86: Images of (a) Thinned wafer backside showing polyimide support (b) Front side of diced wafer showing the accuracy of the dicing (c) Separated thinned chips.

5.2.3. Thin chip encapsulation

Encapsulation of thin chip is necessary to reduce the stress level of the chip by putting it in a neutral plane. Even if packaged on a flexible PCB, it is beneficial to encapsulate the package with an extra layer. Two types of encapsulation technique have been used in this work:

5.2.3.1. PDMS encapsulation

Due to low Young's modulus of PDMS, it generate minimum stress on the encapsulated chip. PDMS was mixed with a curing agent in the ratio of 10:1 and degassed to remove any bubble. A 4 inch wafer was salinised prior to spin coating, in order that PDMS could be easily peeled off from the carrier. Following this, PDMS was spin coated at 500 rpm for one minute and thin chip was placed during the curing stage. Once the chip was fixed, a second layer of PDMS was coated and cured. The whole stack was peeled off carefully, as shown in Figure 5.87(a) and Figure 5.87(b-c) shows the package bendability and placement over a human arm. This method is good for cases such as wireless chip, where the chip can be powered and the data can be transmitted wirelessly, as PDMS etching over the contact pads requires cumbersome processing steps.

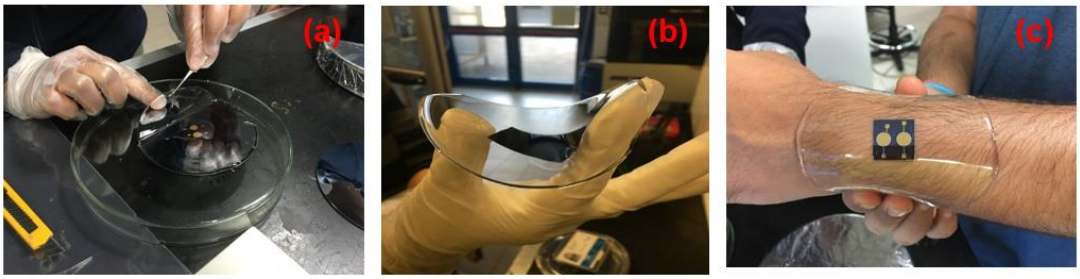


Figure 5.87: (a) Release of the thin encapsulated chip from carrier wafer (b) Thin encapsulated chip in bent condition (c) Thin encapsulated chip placed on forearm, showing its conformability.

5.2.3.2. Hot lamination using PVC sheet and laser cutting

To surpass the challenge related to accessing the contact pad after encapsulation, hot lamination was performed, using PVC foil. The lamination was done by placing a thin chip between two PVC sheets and laminated using a roller laminator at 80˚C. After lamination, a laser cutter (Trotec Speedy 300 Laser Engraver/cutter) was used to etch PVC over the contact pad to obtain the electrical connection. Many tests were performed on dummy

silicon samples laminated in PVC, to optimise the equipment parameters, in order that the laser only etches the PVC over the contact pads, but not the contact pad itself. Table 5.8 lists all the recipes with the etch depth achieved and Figure 5.88 shows the optical image of the first 6 recipes, and, as can be seen recipe 4 was the most successful in etching the PVC till the metal layer.

Table 5.8: List of laser etching recipes tested for removing the encapsulation

Recipe	Power [%]	Speed [%]	Frequency [kHz]	Etch depth [µm]
1	30	5	1	160
2	10	5	1	160
3	10	5	0.5	160
4	10	20	0.5	0
5	20	20	0.5	160
6	20	70	1	20.2
7	40	70	1	65.6
8	50	70	1	12.6
9	80	90	1	16.5
10	40	90	1	60.3

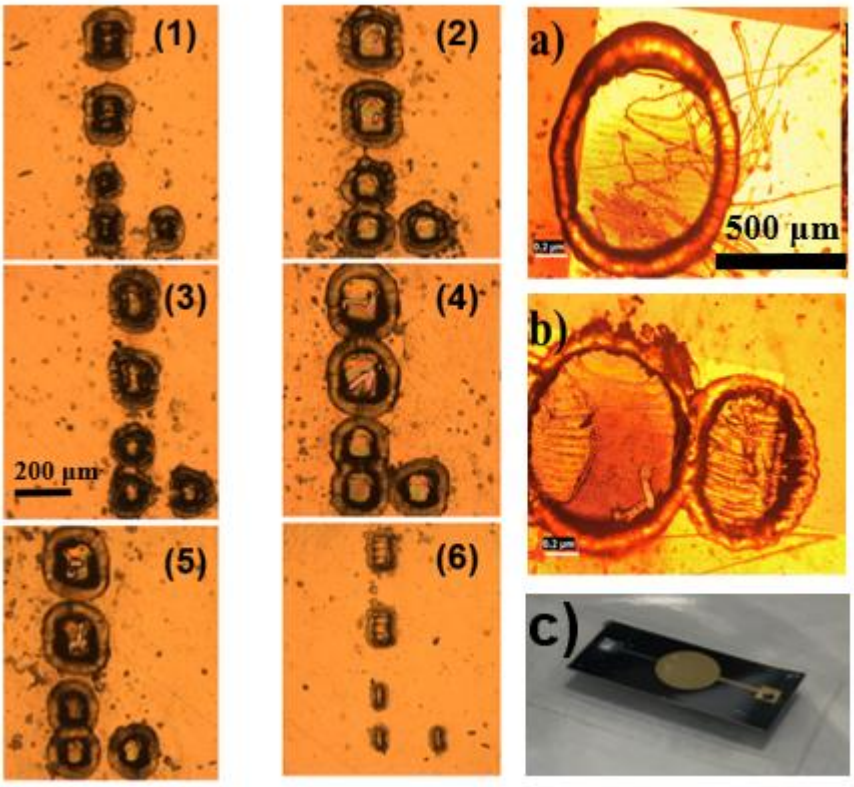


Figure 5.88. (1-6) Optical images of vias etched in PET by carbon dioxide laser using the recipes tabulated in Table 5.8. Optical image of laser etched via over the (a) bottom and (b) top electrode of capacitor (c) Thin silicon-based capacitor laminated between two PET sheets.

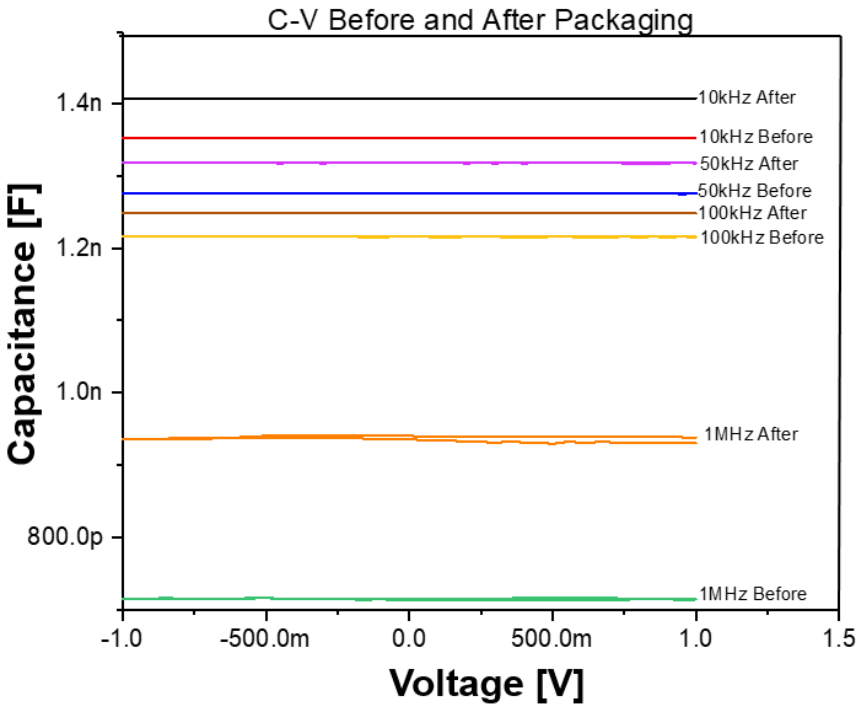


Figure 5.89: Capacitance vs Voltage plots of thin silicon based capacitor before and after lamination.

Since the capacitor has two different metals, Al and Au as pad metal, recipe 4 and recipe 7 were used to etch the PET over Al and Au and Figure 5.88 (a-b) shows the etched PET over Al and Au respectively.

For checking the success of packaging, C-V measurements were done before and after packaging. The plots in Figure 5.89 show the C-V test under four different frequencies before and after packaging.

5.3. Wafer Scale Etching

After optimising the TMAH etching recipe, a process was carried out to realise wafer scale thinning and the transfer of thin silicon-based devices on flexible substrate.

5.3.1. Device Fabrication

Two basic structures of any electronics i.e. MOSCAPs and MOSFETs were fabricated on 2" p-type (100) Si wafers of (100) orientation and 1-10 Ω-cm resistivity. For MOSCAP, 100 nm thick high quality silicon dioxide was grown via dry oxidation at 1000^{o}C. Nickel (10 nm) and gold (100 nm) were evaporated by electron beam evaporation system and patterned to define the top electrode. A single MOSCAP has an area of 0.48 cm^{2}. For MOSFETs fabrication, 5 mask process was used and the key process steps are shown in Figure 5.90. A field oxide of thickness ~500 nm was grown on the top of the wafer which was later used to isolate diodes of adjacent MOSFET as well as the mask on the rear side. Lithography was carried out to the patterned oxide layer in the front side and the exposed area was etched. Phosphorus was then diffused at 970˚C for 30 minutes through the opened window for creating the source and drain region of the transistor. After defining the active region, a high quality gate oxide of thickness ~100 nm was grown. The contacts holes for diodes were opened through gate oxide itself and metal stack of Ni/Au (10 nm/100 nm) was evaporated. In the last stage of fabrication, metal was patterned to define the contact pads and interconnection, and sintered in forming gas at 450^{o}C to obtain better ohmic contact. The gate length was of 10 µm (with further 5 µm overlap on each diode regions) and channel width of 100 µm.

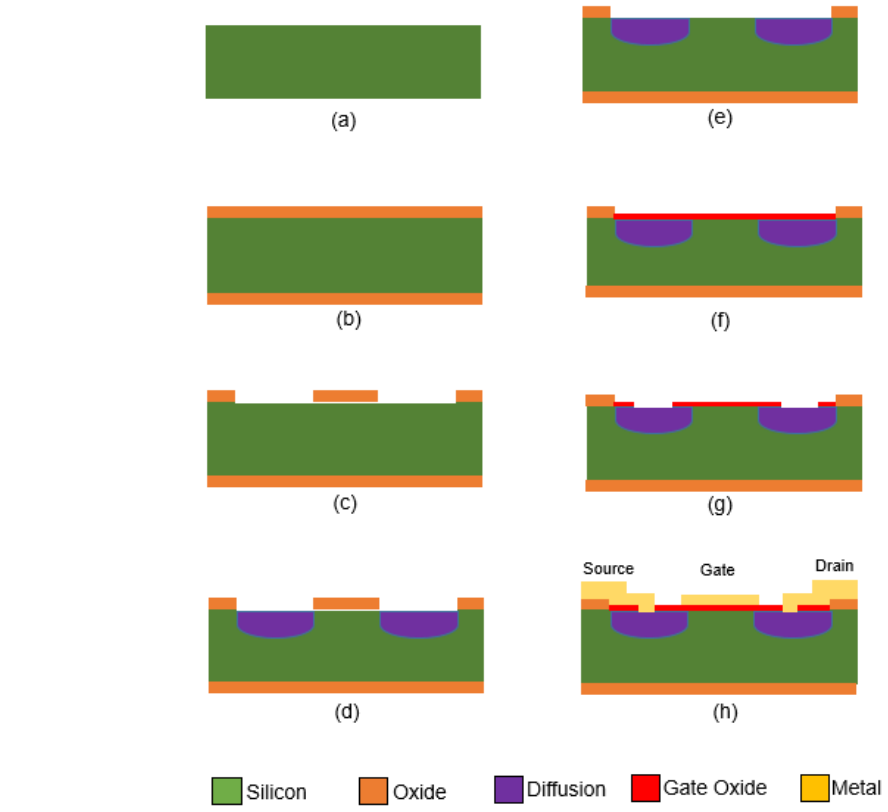


Figure 5.90: Key process steps carried out to fabricate MOSFETs on bulk silicon wafer.

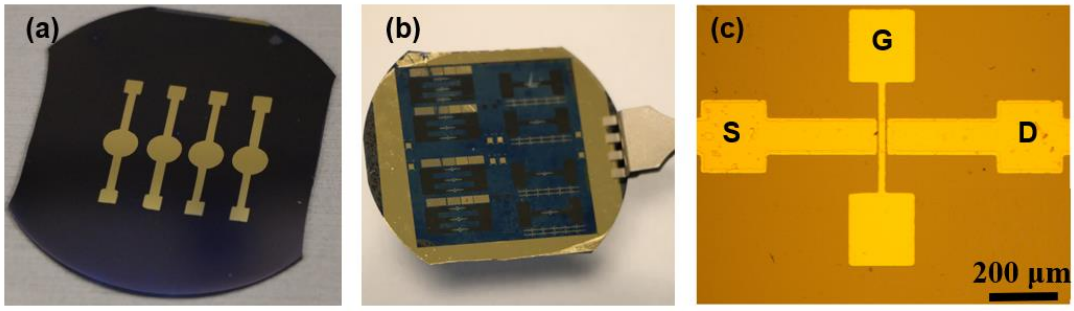


Figure 5.91: Image of fabricated (a) MOSCAP (b) MOSFET (c) Optical image of single MOSFET.

5.3.2. Post processing

The front side of the wafer was protected from TMAH by ProTEK B3 protective coating from Brewer Science and a custom wafer holder with double O-ring. Follwing fabrication of the devices, ProTEK B3 primer was spin-coated over the devices at 1500 rpm for 30 seconds with an acceleration of 10000 rpm/second. Then the wafers were baked on a hotplate at 140˚C for 120 seconds, and then at 205˚C for 5 minutes in a convection heating

oven. Following this step, the ProTEK B3 protective coating was spin-coated on the front side at 1500 rpm for 60 seconds with an acceleration of 10000 rpm/s. The wafers were then baked on a hotplate at 140˚C for 120 seconds and at 205˚C for 30 minutes in a convection heating oven. After chemical thinning from the backside, the front ProTEK protection mask was cleaned by repeatedly rinsing it with fresh acetone and methanol until the solution became clear. Then, the wafer-scale transfer method was followed to transfer the thin wafer on polyimide foil.

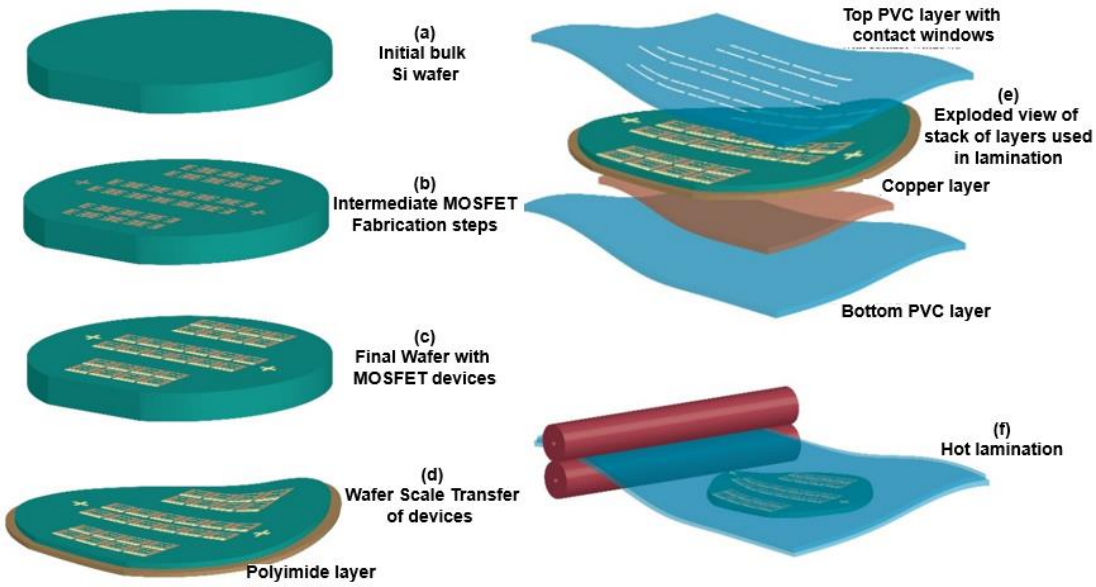


Figure 5.92: Illustration of wafer-scale MOSFET fabrication, thinning and packaging.

5.3.3. Thin wafer transfer

Following chemical etching, the wafer-scale transfer of the ultra-thin wafer to flexible polyimide substrate was carried out. The thinned wafer was adhered to a carrier substrate, which had PDMS of thickness ~200 µm spin coated on it. A low power plasma was used to control the adhesion of membranes with PDMS. The bulk part present on the periphery of wafer was removed using laser dicing wafer, leaving behind only the thinned silicon on PDMS. This first transfer resulted in the front-side of wafer attached to PDMS. In order to gain access to the front side, the membrane was transferred once again, to the final the polyimide film, which was the final receiving substrate. The filmwas obtained by spin coating of polyimide on a carrier substrate with the adhesion promoter at the edges. The layer was cured for 30 minutes at 350°C and another thin layer of PI was spin coated as an adhesive layer just before the transfer of the thinned wafer from PDMS. Before transferring the thinned wafer to polyimide, a small central part was removed to get the back contacts

from the wafer. The wafer on PDMS was then placed on PI film, and soft-baked in a vacuum at 110°C for one minute. Following this, the PDMS was removed using a dilute solution of Tetra Butyl Ammonium Fluoride (TBAF) in a hydrophobic non-hydroxylic aprotic solvent Propylene Glycol Methyl Ether Acetate (PGMEA). This completed the wafer-scale transfer of membranes on PI film. After transferring to polyimide, copper tape (50 μm thick) was used as back contact of devices. The tape also served as the thermal dissipation layer, which is required for high performance computing. Instead of using another spin coated PI for encapsulation, the hot lamination of PVC was used to encapsulate the MOSFETs and the final image of bendable wafer is shown in Figure 5.93. To gain access to contact pads the openings were cut on the top of the PVC using a Silhouette cutter before laminating the devices.

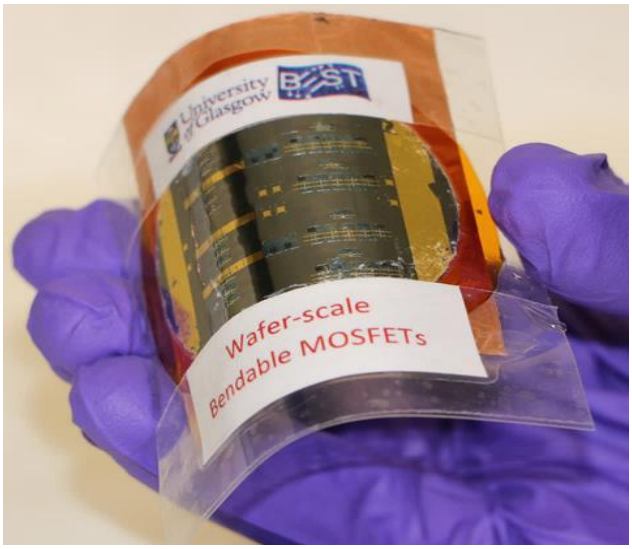


Figure 5.93: Image of bendable devices realised after wafer scale thinning and transfer.

5.4. Chip Scale Thinning

The pre-fabricated chip was provided by researchers at University of Toronto, Canada and thinning at chip level and transfer on flexible substrate was carried out as a collaborative project. The chip has dimensions of 5 mm x 5 mm, thickness of 250 µm and fabricated with standard 130 nm CMOS technology. Due to the small size of the sample, a glass slide was used as the carrier, instead of conventional holder. Before the thinning, the front side of the chip was protected by using ProTEK B3 protective coating as discussed above. The

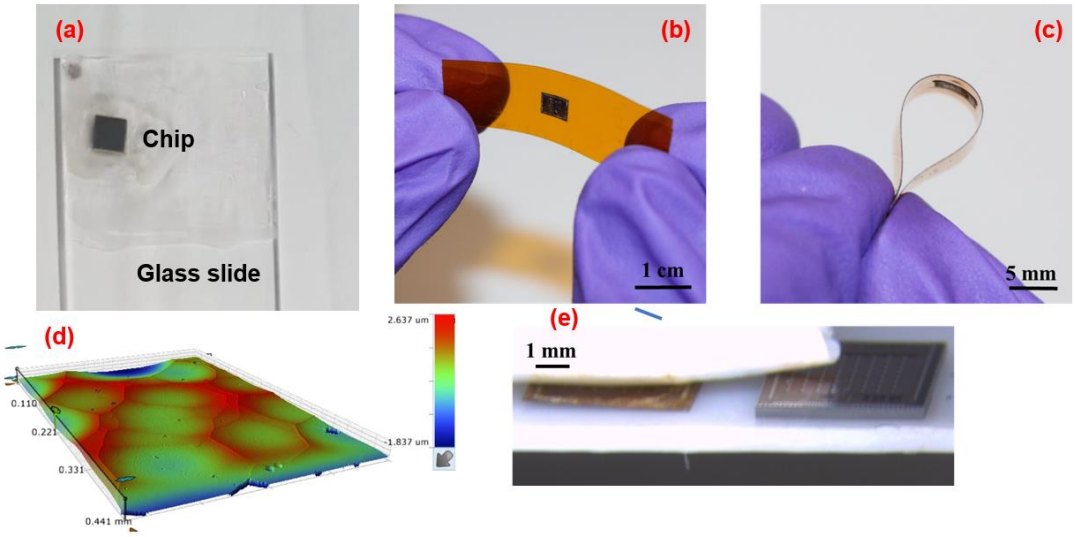


Figure 5.94: (a) Image of thick chip adhered to glass slide in face down approach before thinning (b)-(c) Thin chip attached to polyimide using thin PDMS layer (d) Optical profilometer scan of etched surface showing etch pits (e) Image showing thickness comparison of chip before and after thinning. *(submitted in ISSCC 2019)*

chip was treated in an oxygen plasma asher system at 150 W for 2 minutes. The adhesion promoter (ProTEK B3 primer) was first coated and the sample was baked on a hot plate at 140°C for 120 seconds, followed by 205°C for 5 minutes in a convection heating oven. Following this step, the ProTEK B3 protective coating was coated on the front side. The chip was then baked on a hotplate at 140°C for 120 seconds followed by 205°C for 30 minutes in a convection heating oven. The chip was then chemically etched in (25% TMAH + 10% isopropanol) solution at 83ºC to achieve a thickness of around 15±6 µm. At the centre of the wafer. After thinning, the polymeric protection was cleaned using warm acetone and methanol, and the thin chip was transferred on polyimide foil with PDMS as adhesion layer. Figure 5.94(b-c) shows the thinned chip on PI and Figure 5.94(d) shows the surface profile of the etched side of the thinned chip. A variation in the height of 2.24

µm is observed in the local area arising from the etch pits, as can be seen in the optical profilometer image of Figure 5.94(d).

5.5. Dry etching

Many types of reactive gases have been used in different kinds of plasma for etching range of materials. For silicon, halide based reactive gases such as SF_6, $CBrF_3$, Cl_2/Ar and HBr have been used, due to their reactive nature and ability to make volatile components (SiF_4, $SiCl_4$, or $SiBr_4$) on reacting with silicon.

Bosch process is one of the variants of dry etching processes that uses fluorine-based plasmas operated in an inductively coupled plasma (ICP) reactor. This process is especially used in the applications requiring very deep and vertical trenches. Two alternating pulses are frequently used to ensure the silicon deep etching through the mask. SF_6 plasma pulse is the first of the alternatives used for etching, while C_4F_8 plasma is the second pulse which is used for protecting the sidewalls by polymer deposition.

In this work, Estrelas installed by Oxford Instrument (shown in Figure 5.95(a) was used for bulk etching of silicon).

5.5.1. Effect of ICP power

In the BOSCH process, the bias power of ICP reactor contributes to the momentum of ion bombarding toward the substrate and is thought to determine the intensity of the ions hitting the silicon wafer. So higher power means a high number of energetic particles, thus resulting in an enhanced etch rate.

5.5.2. Effect of chamber pressure

The chamber pressure during the etching mainly influences the profile of the etching structure. Generally, the chamber pressure during the BOSCH process controls two basic features in silicon etching: the energy of the reactive ion flux and its density, i.e. the density of the fluorine ions. For example, at low pressure the ions receive very little resistance, thus when bombarded with high intensity, gives a high etch rate but is limited by the number of reactive ions. As the chamber pressure increases, the energy of the ions decreases and the number of fluorine radicals increases, which leads to many uncertain collisions and gives a rough and non-uniform surface.

5.5.3. Effect of SF_6 flow rate

In an ICP etching system, SF_6 gas is the source of the chemically reactive species and so its flow rate plays a very important role in the etching. It is obvious that the etch rate is directly proportional to the flow rate of SF_6, as more gas will give more reactive species. Howver, this is true only up to a certain limit, after which the radicals start obstructing themselves, thus reducing the etch rate.

5.5.4. Effects of the C_4F_8 flow rate

C_4F_8, a cyclic fluorocarbon disintegrates to produce CF_2 and longer chain radicals in the high-density plasma. These readily deposit as fluorocarbon polymer on the samples being etched. The polymer materials serve as a passivation layer to protect the silicon sidewalls from being etched by SF_6 gas during the BOSCH process. The flow rate plays an important role in maintaining the anisotropy of the etching, as less gas will forma thin layer and can increase the side etching, whereas more gas will form a thicker passivation layer, decreasing the etch rate. In this work, the C_4F_8 flow rate was kept to a minimum, just to initiate the process, because the task was to etch silicon completely from the back, not the formation of trenches.

5.5.5. Role of Helium

As the process is cryogenic, it is extremely necessary to keep the carrier wafer cool and this is achieved by using liquid nitrogen. The wafer is mechanically clamped to a stage and helium pressure of 10 torr was applied on the back, since helium has high thermal conductivity, it improves the heat transfer.

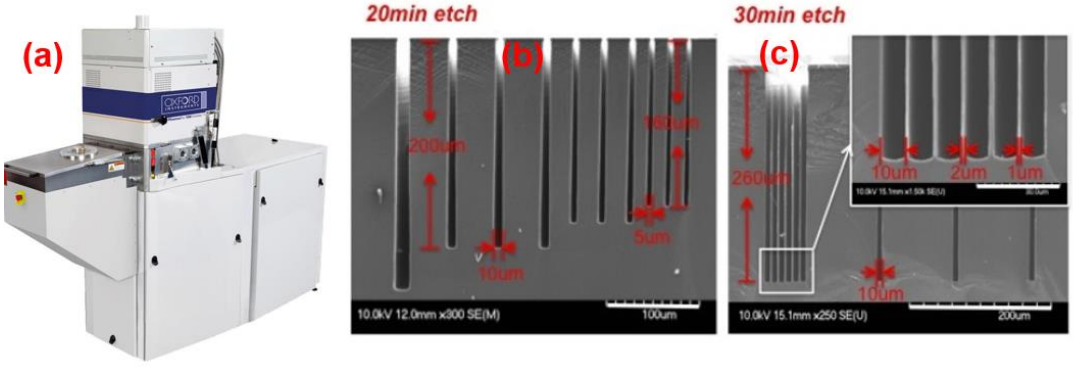


Figure 5.95: (a) Image of Estrelas used for bulk Si etching (b)-(c) SEM images of deep trenches etched using high etch rate recipes.

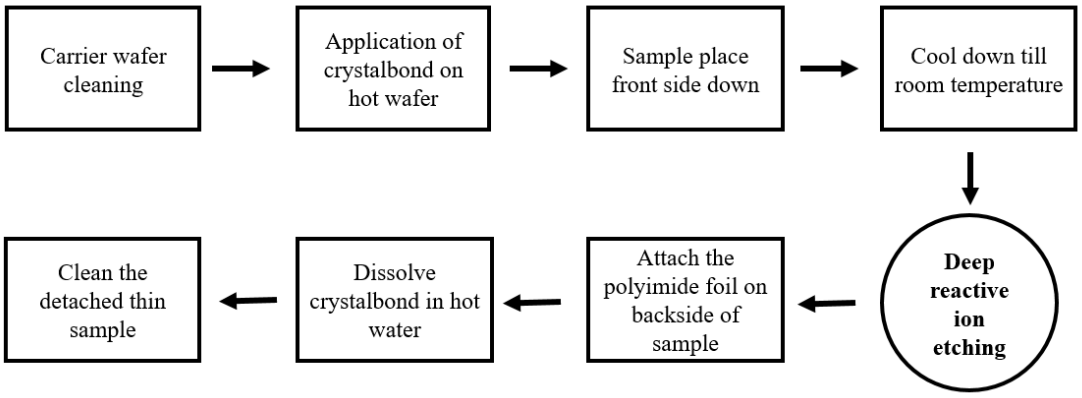


Figure 5.96: Process flow of DRIE performed to obtain thin silicon

5.5.6. Sample preparation

A 2 inch silicon wafer of (100) orientation was used as substrate material for fabricating aluminium nitride (AlN) capacitive structure. The wafer was cleaned using the standard cleaning procedure, i.e. acetone, IPA and DI water. Ti/Al of thickness 20nm/100 nm as bottom electrode was deposited using Plassys 2. AlN was sputtered in Plassys 3 using RF power source for 2 hours at the following parameters:

Table 5.9: Sputtering parameters for AlN deposition

Parameter	Value
Power	500 W
Nitrogen	50 sccm
Argon	20 sccm
Pressure	3 mtorr
Distance	59 mm

Top electrode composed of 20nm/100 nm thick NiCr/Au was deposited through hard mask in Plassys 4.

5.5.7. Post-processing

The sample was mounted on carrier wafer (a 6 inch silicon wafer with 2.5 µm thick oxide) using Crystalond 555. The crystalbond, which as the heat transfer layer between sample and carrier, was evenly spread on the carrier wafer before fixing the sample. After cooling down, the mounted sample was loaded in the chamber and cleaning of the chamber was carried out with following parameters:

Table 5.10: Process parameters used for cleaning step before the etching	
Parameter	**Value**
Time	20 minutes
Pressure	15 mtorr
ICP Power	2500 W
Helium backing	10 torr
Oxygen flow rate	200 sccm
Backing temperature	25^{o}C

This was followed with the etching step with the following parameters:

Table 5.11: Process parameters used for bulk etching of silicon	
Parameter	**Value**
Process time	12 minutes
SF_6	800 sccm
C_4F_8	10 sccm
Pressure	120 mT
ICP	3500 W
Helium pressure	10 T
Backing temperature	5^{o}C

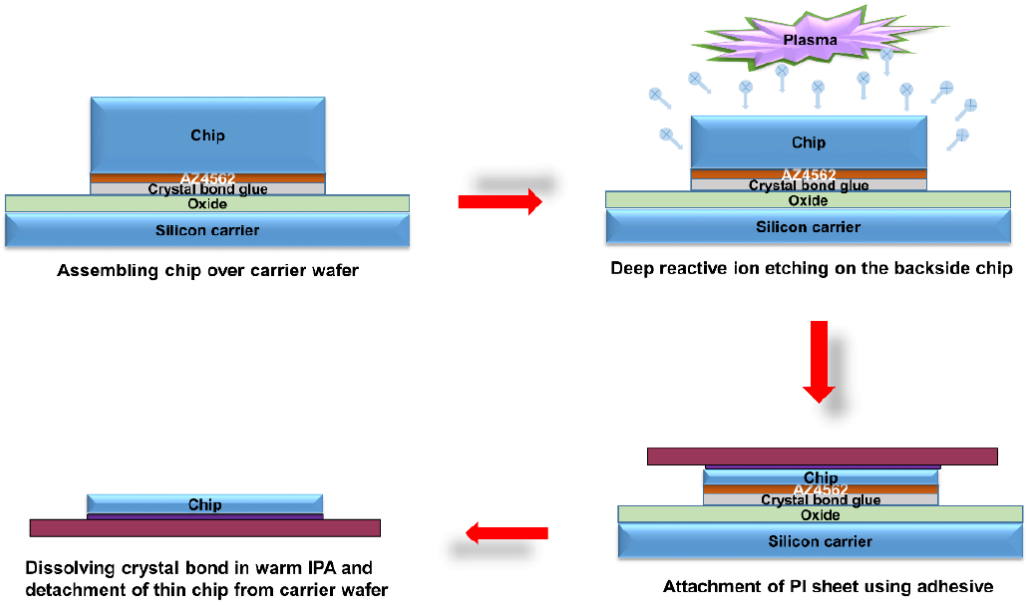


Figure 5.97: Illustration of DRIE of sample and its transfer on flexible substrate.

The etching was carried out for 12 minutes with etch rate ~20 µm/minutes. Once the etching finished, a thin layer of low-stress epoxy glue was applied on the etched side of the sample and a polyimide foil was attached to it. The stack was baked at 80°C for 3 hours to cure the glue and then placed in hot water overnight. The crystalbond is dissolvable in hot water, so the thin chip detached from the carrier wafer but remained attached to the polyimide foil. Thereafter, it was rinsed in IPA to remove any residues and dried. This process is shown in

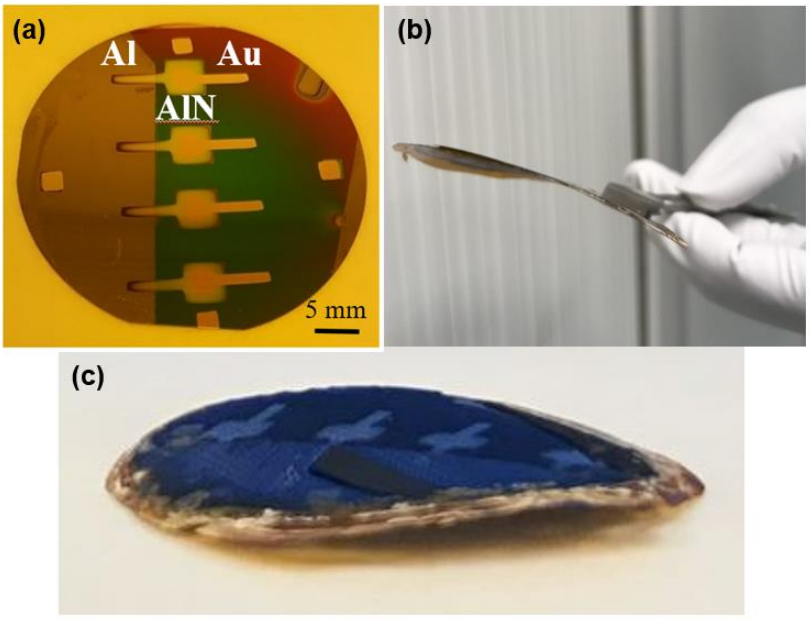


Figure 5.98: Image of AlN piezocapacitor (a) before thinning (b-c) after thinning.

the form of a flow chart in Figure 5.96 and illustrated in Figure 5.97. The images of the fabricated sample before and after thinning are shown in Figure 5.98(a-c).

5.6. Mechanical Grinding

The chips used for the grinding process were fabricated using standard 180 nm CMOS technology. The chip had a CMOS inverter that was composed of NMOS and PMOS of different channel length and width, as shown in Figure 5.99(a-c). The sample was mounted on grinding tape in facedown approach. Coarse and fine grinding was performed till the thickness reached 20 µm, as depicted in Figure 5.99(d). The thin chips were picked up using vacuum tweezer and bonded on flexible PCB. A thin layer of PDMS was spin coated on the top of the package that kept the chip in neutral plane. These samples were used to analyse the effect of bending on inverter characteristics by fixing the chip on 3D printed jigs, as shown in Figure 5.100(b-c).

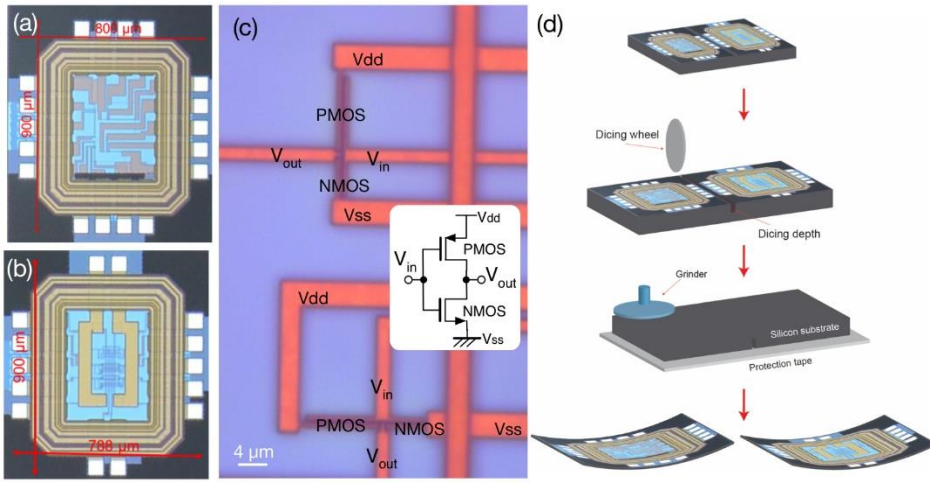


Figure 5.99: (a) Microphotograph of the fabricated chip (d) Optical image of inverter (d) Dicing before grinding approach adopted for thinning the chip.

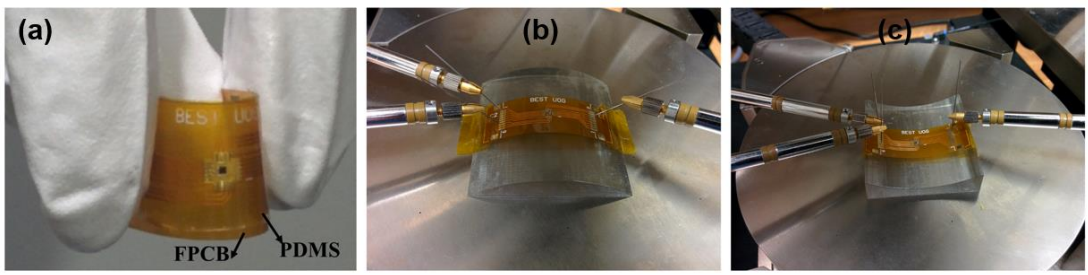


Figure 5.100: Image of (a) Thin chip packaged on FPCB (b) Testing under tensile stress (c) Testing under compressive stress.

5.7. Conclusion

There are different types of thinning techniques available that can be adopted depending on the pre-processing steps and the limitations. In this work, three major types of thinning methodologies were adopted, namely wet etching, dry etching and grinding. In the wet etching, 25% TMAH solution was used due to its IC compatibility, and extra protection was ensured by using a polymeric layer on the processed side. The techniques such as dicing before etching, and PET supported dicing developed during the process, showed a promising increase in the yield of thinned chips. The encapsulation methods used for keeping the thinned chips in neutral planes could be used for increasing the mechanical reliability. Moreover, the issue of contact pads access was solved by developing recipes in the laser cutter, which resulted in PVC etching just over the metal pads. Once the processed wafer was thinned, its transfer on to the flexible substrate was achieved by a two-step transfer process using PDMS and polyimide coated wafer. Using the optimised wet etching process, thinning was performed on chip scale as well using custom made wet etching setup. These processes resulted in wafer and chips with thickness ranging between 15 μm to 25 μm.

For the dry etching process, a capacitive structure composed of AlN was fabricated as a sample. The BOSCH process was modified in the available equipment (Estrelas) to achieve a high etch rate using SF_6 as etchant. The etch rate of ~ 20 μm/min was reached which resulted in final thickness of ~25 μm, and the transfer from the carrier wafer was carried out using a one-step transfer process.

The mechanical grinding of the processed die was performed using the Dicing-Before-Grinding technique and a final thickness of ~ 20 μm was achieved. The thinned chips were packaged on FPCB and wire-bonded to study the effect of bending on inverter characteristics.

The various types of test conducted to study the effect of thinning on silicon properties and effects of bending on device characteristics are discussed in Chapter 7.

Chapter 6: Flexible Electronics Device Modelling

As the device responses are known to change with the stress induced by bending, it is important and necessary to develop analytical models which can capture this effect. This will not only facilitate the defining of the boundary conditions, but can also help circuit designers to design a circuit which can work reliably during bending. This chapter presents the work done in the direction of analytical modelling of silicon-based device and the circuit's response to mechanical bending. Firstly, a model tactile sensor which uses piezoelectric material with transistor, was developed using piezoelectric and standard semiconductor device equations. The model equations are also implemented in Verilog-A, which makes it compatible for a standard circuit designing tool like Cadence and ultimately the sensor response was simulated, which showed close matching with experimental. Furthermore, the bending stress and the shift in device response has been modelled using the piezoresistance theory of silicon. Based on this stress-dependent model, devices including MOSFET, POSFET and inverters are modelled. The discussion also includes strategies for compensating or minimising these bending-induced variations, and simple readout architecture for POSFET has been proposed. These advances will enable the next generation of computer-aided-design tools to meet the future design needs in flexible electronics.

6.1. Analysis of Stress Effects on Ultra-Thin Chips

As the interest in the field of flexible electronic is increasing, many technologies, such as printed electronics or sensor over organic semiconductors have been investigated. However, for such technologies, the low carrier mobility is becoming the main disadvantage for the applications which require high speed. Si as the conventional high-performance material, has been investigated in flexible electronics by using devices such as silicon nanowires (NWs) and ultra-thin chips (UTCs). Nevertheless, simulation of changes in the performance due to bending stress is still a challenge, as there is a lack of suitable models which can predict the behaviour of devices and circuits under compressive and tensile bending stress.

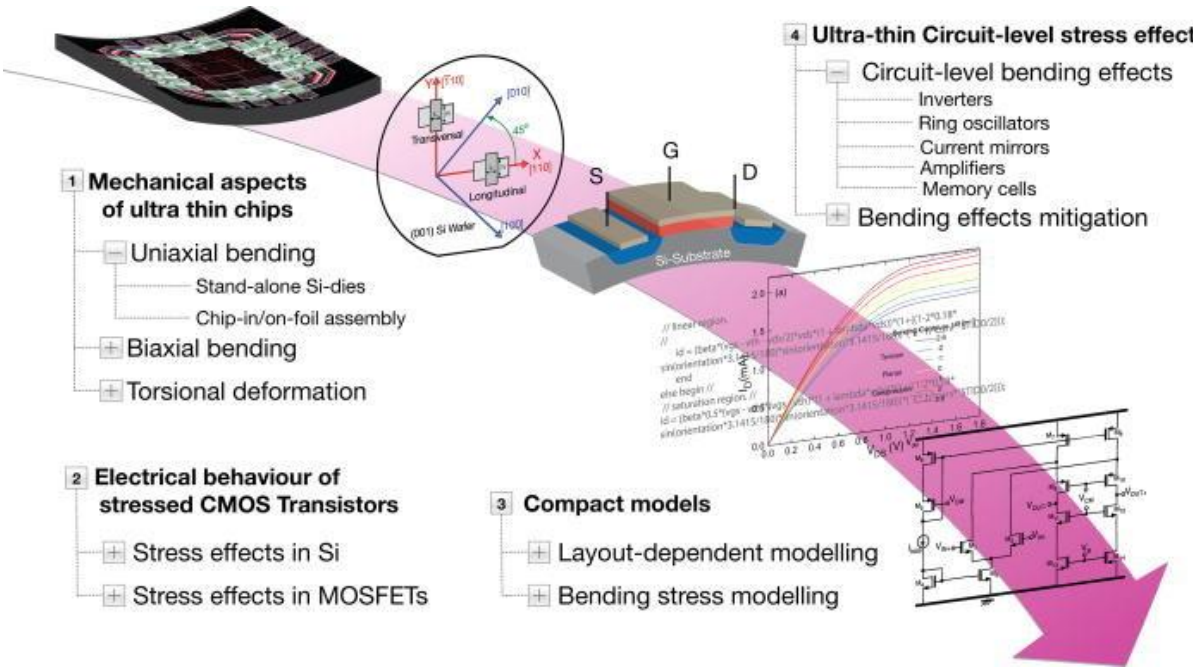


Figure 6.101: Illustrative figure showing different techniques for modelling the effect of bending stress on devices and circuits. [214]

This case is of specific interest in the case of UTC, as when UTC is packaged on a flexible substrate and placed over a curved surface, the UTC experiences mechanical stress. Even if the UTCs are not bent or externally loaded, residual stress is developed during the fabrication processes, which may affect the electronics properties of devices, as discussed in Chapter 2. This results in deviation from the expected electrical behaviour of the devices [215]. Therefore, it is necessary to study the stress effect on thin chips right from the device and up to circuit level ,as illustrated in Figure 6.101, as this study not only helps in analysing the piezoresistive effect in stressed devices, but also in maintaining the electrical reliability of electronics. This has been done mainly in three ways, which are illustrated in Figure 6.102 and discussed briefly below**.**

6.1.1. Analytical Modelling

Analytical models are important to attain physical insight and predict the behaviour of UTC under non-stressed and stressed conditions. It may need intelligent approximations/assumptions to formulate the analytical relations which model and describe the relationships between the parameters of interest observed in empirical results. The model should include various physical parameters which are influenced by stress. For example, considering chip on flex system, where the substrate and thin silicon are modelled on the basis of beam theory. During the bending of such a system, when the tensile strain exceeds critical

strain, the substrate starts bending. [216]. Under these assumptions, the maximum tensile stress in thin silicon chip at which it may fracture, occurs at the centre of the silicon, and is given by:

$$\sigma_{crack} = \left\{ G_a h_s \left[\beta \left(\frac{2\chi^4}{\lambda^3} + \frac{\lambda}{2} \right) - \frac{2h_f \chi^4}{2\lambda^2} \right] + E'_a \right\} * \frac{3\pi}{\chi^4 {h_f}^2 h_a L} \sqrt{\frac{dL}{L} - \frac{\pi^2 {h_s}^2}{12L^2}} \qquad (6.19)$$

where G_a is the shear modulus of the adhesive layer, h_s, h_s, h_a are thickness of substrate, thin silicon and adhesive respectively and E'_a is shear modulus of adhesive. Details about λ and χ can be found in [217-219].

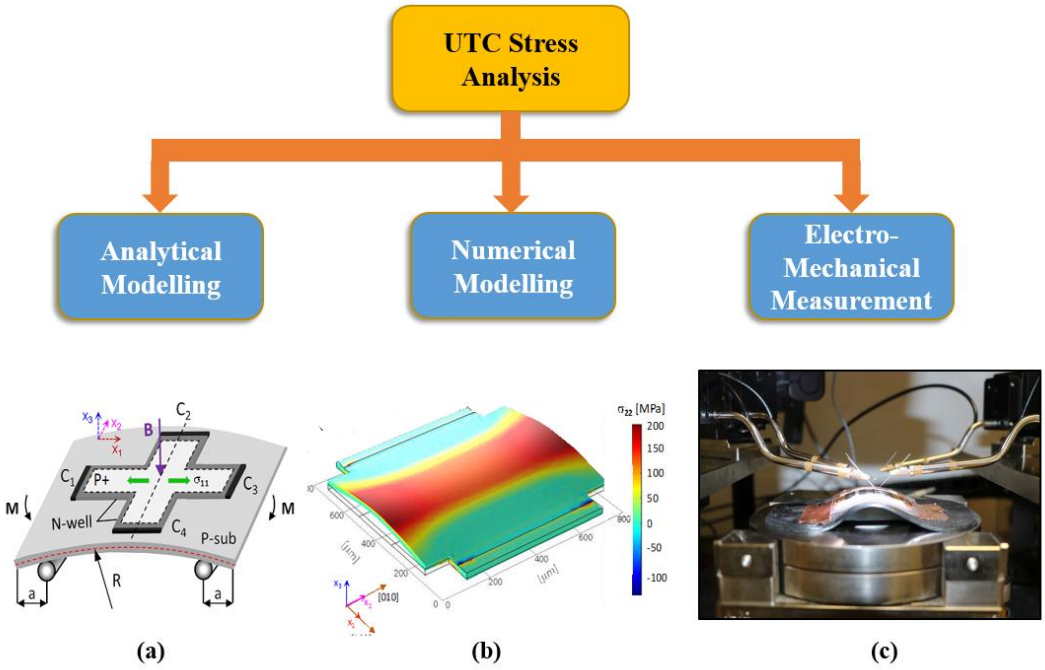


Figure 6.102: Various techniques i.e. analytical modelling, numerical modelling and electro-mechanical measurements used for studying and analysing the effect of bending on device response. While the first two are used for the making predictive models, the actual measurements are necessary to fit those models.[214]

6.1.2. Numerical Modelling

Analytical solutions may not be sufficient or possible to explain complex behaviour and coupled behaviour/interaction between mechanical, electronic or other physical parameters of interest. In this regard, multi-scale multi-physics numerical simulations are promising to describe the physical behaviour. As such for the case with thin silicon, the magnitude of stress and its distribution in the system at different bending radius can be determined by numerical analysis such as the Finite Element Method. Wacker *et al.* [220] used a structural mechanics

module available in COMSOL Multiphysics® in combination with contact modelling with friction for the contacts between the support struts and chip surface to study the bending effect of chip-on-foil configuration.

Such theoretical studies then need to be validated by either one or more of the following experimental methods:

6.1.3. Electro-mechanical measurements

Electromechanical measurements are performed on UTCs comprising basic devices such as PMOS and NMOS to validate the model. In these experiments, a thin chip is placed over a 3D surface to introduce stress in the chip and electrical characterisation is performed. Wacker *et al.* [220] have carried out bending tests and electrical measurements on specially designed ultra-thin CMOS chips with PMOS and NMOS test devices to quantify the change in different electrical parameters.

6.2. Analytical Model of POSFET

POSFET device is composed of MOSFET and piezoelectric material, coupled together at gate terminal. POSFET exhibits characteristics similar to MOSFET characteristics, i.e. transfer and output characteristics, just with the difference that oxide capacitance role in traditional current equation is played by effective oxide capacitance. However the change which is not apparent at first look, is the slight shift in threshold voltage of MOSFET after poling. One of the most important process during fabrication of P(VDF-TrFE) based POSFET is poling i.e. the process of aligning the dipoles present in the P(VDF-TrFE), by applying high electric field across it.

In order to theoretically study the effect of poling on the electrical characteristics of POSFET, a mathematical model was proposed. The model combines the hysteresis property of piezoelectric polymer with standard MOSFET characteristics equation. To calculate the amount of polarisation charges on application of an electric field, Miller *et al.* [221], proposed a simple equation which relates the polarisation charges to the electric field.

$$P^{+}(E) = P_s \tanh\left(\frac{E - Ec}{2\delta}\right) + \varepsilon_F \varepsilon_o E \tag{6.20}$$

where $\delta = E_c \left(\ln\left(\frac{1+\frac{P_r}{P_s}}{1-\frac{P_r}{P_s}}\right)\right)^{-1}$

and

$$P^{-}(E) = -P^{+}(-E) \tag{6.21}$$

P_s: saturation polarization, i.e. the maximum polarisation charge achieved during poling and after which the hysteresis loop saturates.

P_r: remnant polarization, i.e. the electrical charge left when the electric field reaches zero.

E_c: the coercive field at which the polarisation charges changes their polarity.

$P^+(E)$ and $P^-(E)$ denotes positive going (lower) branch and negative-going (upper) branch of hysteresis curve, respectively. The values of P_r and P_s are obtained by the experimental measurement and the full hysteresis loop is plotted using equations as presented in Figure 6.103.

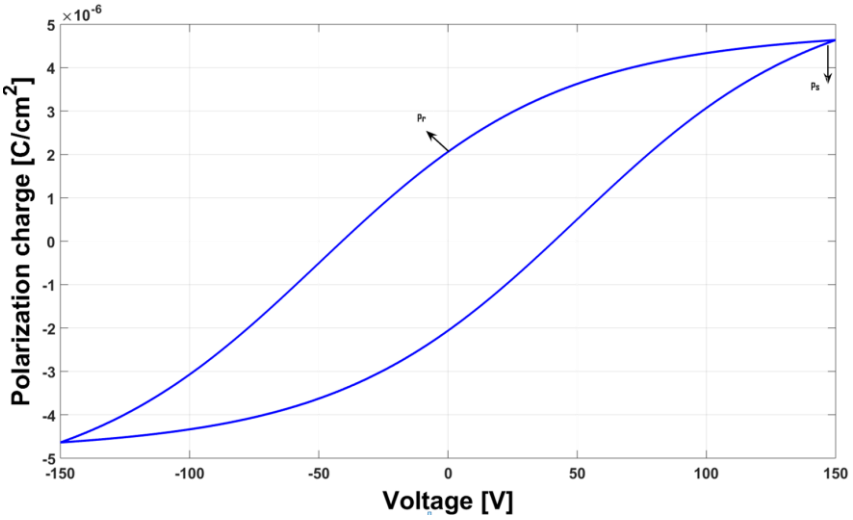


Figure 6.103: Simulated Hysteresis curve of P(VDF-TrFE). The saturation polarisation state is the maximum charge which is attained at 150V and upon removing the electric field, the charge drops down to remnant polarisation state. [222]

During poling, the switching polarisation charge developed in polymer, P_{sw}, is defined as the charge switched from one remnant polarisation state to the maximum polarisation state of the opposite polarity. In the presence of a transistor below the piezoelectric layer, as was the case with POSFET, this switching polarisation charges, leads to the creation of an extra layer of charge in the semiconductor channel region to maintain charge neutrality. These extra charges can be termed as compensation charges and can be written as

$$P_{comp} = P_{sw} = P_r + P_s \tag{6.22}$$

Therefore, after poling there was a fixed amount of charges present at the oxide-semiconductor interface, which results in a change of flatband voltage. Flatband voltage of the transistor, which is defined as the difference between the gate metal workfunction, $\emptyset_M$, and the semiconductor workfunction, $\emptyset_s$ is written as:

$$V_{FB} = \emptyset_M - \emptyset_s \tag{6.23}$$

This change can lead to either an increase or decrease of flatband voltage, depending upon the poling direction. In the case of POSFET, poling was done by applying positive voltage on the top metal and keeping the gate metal at ground. This condition creates a layer of negative charges at the oxide-semiconductor interface and so the flatband band voltage for N-MOSFET decreases and can be written as:

$$V_{FB\_eff} = V_{FB} - \left(\frac{P_s + P_r}{C_{ox}}\right) \tag{6.24}$$

Threshold voltage of transistor which is defined as the level of gate voltage, needs to be applied to the gate voltage to create the inversion charge layer and onset of current. Threshold voltage is directly proportional to flatband voltage and can be written as :

$$V_{th} = V_{FB} + 2\emptyset_F + \frac{\sqrt{2\epsilon_s N_a(2\emptyset_F + V_{SB}}}{C_{ox}} \tag{6.25}$$

As the flatband voltage changes so do the threshold voltage with the same amount and can be written as:

$$V_{th\_eff} = V_{th} - \left(\frac{P_s + P_r}{C_{ox}}\right) \tag{6.26}$$

After quantifying the change in threshold voltage after poling, and taking into account the overall device capacitance, which is series combination of polymer capacitance and oxide capacitance, the characteristic current equation of POSFET can be written in linear and saturation region as:

$$I_{DS}\begin{cases}\mu_n C_{stack}\left(\frac{W}{L}\right)\left\{(V_{gs}-V_{th_{eff}})V_{ds}-\left(\frac{1}{2}\right){V_{ds}}^2\right\} & \text{Linear}\\ \mu_n C_{stack}\left(\frac{W}{2L}\right)\left\{(V_{gs}-V_{th_{eff}})^2\right\}\ ) & \text{Saturation}\end{cases} \quad (6.27)$$

Where $\frac{1}{C_{stack}}=\frac{1}{C_{ox}}+\frac{1}{C_{PVDF}}$

The equations are simulated using MATLAB at different gate and drain voltages and plotted against the experimental measurement (Table 6.12), as shown in Figure 6.104 (a-b). Reasonable matching was achieved under the range of experimental error and thus validates the proposed analytical model.

Table 6.12: Experimental values used for model validation

Parameter	Value
Width, W	3276 µm
Length, L	12 µm
Mobility, μ_n	850 cm^2/V-s
Oxide thickness, t_{ox}	45 nm
P(VDF-TrFE) thickness, t_{PVDF}	2.5 µm
Relative permittivity of P(VDF-TrFE), ε_{PVDF}	12

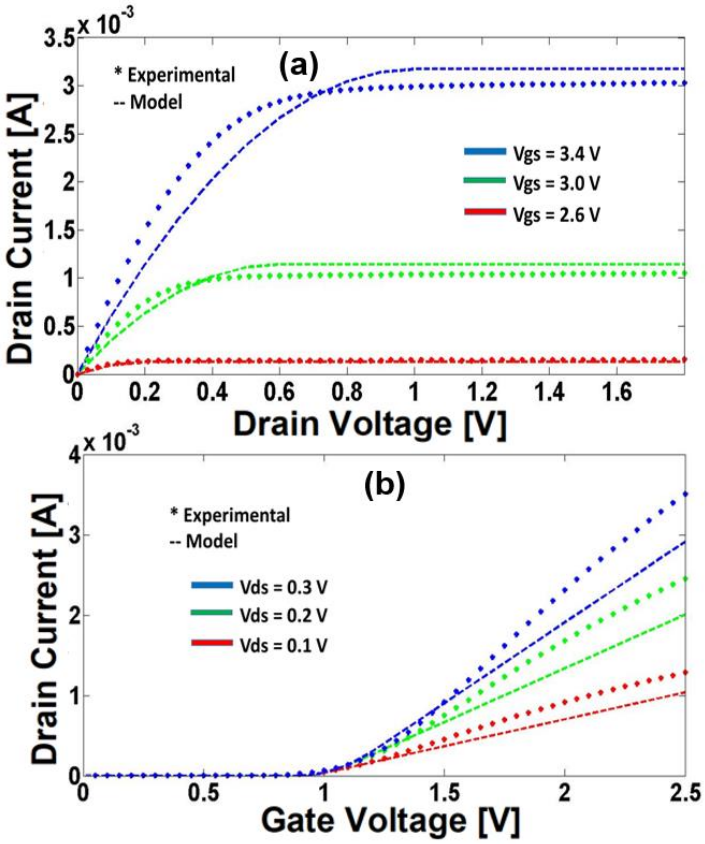


Figure 6.104: Experimental vs model data plot of (a) output (b) transfer characteristics of POSFET. [222]

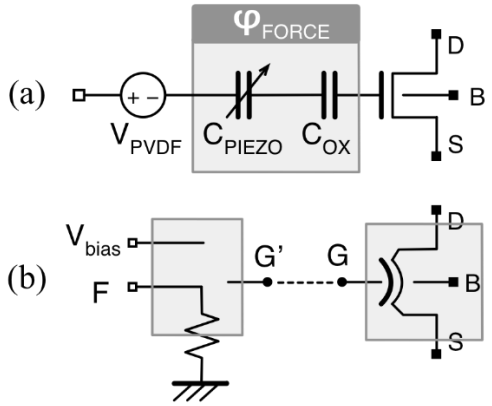


Figure 6.105: (a) POSFET macro-model structure consisting the piezoelectric part and MOSFET, (b) Bendable POSFET Verilog-A sub-circuit blocks and external connections. [223]

6.2.1. Implementation of POSFET model in Verilog-A

Although analytical models of devices give physical insights into working principle, they are not very useful when it comes to using those devices as components in a complex circuit. As

the device response then becomes dependent on other surrounding devices, circuit simulators such as PSpice, PartSim, Multisim and Cadence Virtuso are employed to study the circuital level behaviour. These software have pre-defined but tunable different level device models, which include the different parameters and their relationships with each other. These models are usually written in Verilog-A, which is an industry standard modelling language for analogue circuits. Verilog-A is a DSL for modelling circuit components. The advantage over SPICE based circuit design tools, is the descriptions are "user defined" rather than built-in. One can develop model at the device level with the better accuracy as SPICE, or use rougher models that are faster to compute for blocks in a design. Once the definitions of the working principle are written in Verilog-A, they can be easily run in Cadence. It also provide many other variables like temperature, humidity, band-gap, which provide more freedom in modelling. Specially, in the case flexible device modelling, Verilog-A based models are easier to compile and optimize than using built-in models. In order to design any circuit which utilises POSFET sensing properties, it was necessary to implement the analytical equations in Verilog-A.

The physico-mechanical model described in the analytical modelling section could be adapted to fully model the POSFET devices in a circuit simulator environment using Verilog-A. For the implementation, 0.18-µm CMOS technology was used, since it is currently industry standard for circuit design. POSFET was considered as two fully uncoupled stages: an electro-mechanical stage, i.e piezoelectric capacitor where the effects due to small stress have been neglected, and an electronic stage, i.e. the MOSFET. However, this assumption does not follow the condition of charge neutrality of the POSFET structure, which is:

$$\sigma_I + \sigma_P + \sigma_s = 0 \tag{6.28}$$

where σ_I, σ_P, and σ_S are the charge densities at the interface of gate electrode - piezoelectric polymer, in the bulk of the piezoelectric polymer, and in the semiconductor, respectively. Usually σ_S is much smaller than σ_I and σ_P, and constant with respect to the applied force, and therefore Eq. (6.10) reduces to:

$$\sigma_I + \sigma_P = 0 \tag{6.29}$$

With this assumption, the electronic stage can be considered as fully decoupled from the electro-mechanical stage.

Now, when force is applied over the POSFET (i.e. touch event), the piezoelectric layer produces the charge according to direct piezoelectric effect, and can be written as:

$$Q = d_{33}F \tag{6.30}$$

Similarly, the capacitance of POSFET can be written as the equivalent capacitor C_{stack}, defined as:

$$C_{Stack} = \frac{C_{PVDF}C_{OX}}{C_{PVDF} + C_{OX}} \tag{6.31}$$

The formulated approach discussed in previous sections leads to the POSFET equivalent macro-model shown in Figure 6.105(a).

The piezoelectric dipoles generated during touch event aligns them according to the bias voltage polarity, and results in an extra potential beneath the top electrode and thus changes the effective gate voltage of the MOSFET. This extra voltage produced during touch event can be written as:

$$\varphi_{Force} = \frac{d_{33}F}{C_{PVDF}} \tag{6.32}$$

Based on equation (6.14), φ_{Force} was modelled as a linear voltage-controlled voltage source, with its value depending both on the applied force and the capacitance C_{PVDF}.

The macro-model needed in Verilog was defined as two sub-circuit blocks presented in Figure 6.105(b), showing the outer connections, where V_{bias}, G', G, D, B, S stand for the bias voltage applied to the top electrode, the connection towards the gate of the MOSFET, the gate, the drain, the bulk, and the source of the strained MOSFET, respectively.

The terminal F accounts for the independent applied force, modelled by a voltage source connected to a dummy resistor. This voltage was used to model the piezo- potential φ_{Force} of the macro-model.

Now, assuming that piezo-potential is of same polarity as top electrode voltage, the effective voltage at gate can be written as:

$$V_{gs_{eff}} = V_{gs} + \frac{d_{33}F}{C_{pvdf}} \tag{6.33}$$

In the source-follower configuration which was adopted for POSFET biasing, the device remains in saturation region as $V_{DS} > V_{GT}$, so when force was applied, the change in current can be written as:

$$\Delta I_{ds} = \mu_n C_{stack} \left(\frac{W}{2L}\right) \left(V_{gs_{eff}} - V_{th_{eff}}\right)^2 - \mu_n C_{stack} \left(\frac{W}{2L}\right) \left(V_{gs} - V_{th_{eff}}\right)^2 \quad (6.34)$$

Due to the change in the current, the output voltage of the device changes proportionally with the applied force, and can be written as function of load resistance, R, as:

$$V_{out} = \Delta I_{ds} R \quad (6.35)$$

However, these equations are valid when force is directly applied over sensing device and complete force is considered to be experienced by piezoelectric material, without any attenuation. However, in order to protect the device from damage, a thin layer of PDMS with thickness ~300 um, is attached over the chip during characterisation. This was done to protect the device from any possible damage from the shaker tip.

This protective layer is approximated to be rigid and incompressible with Poisson's ratio = 0.5. When a force is applied on the protective layer, the force is spread through the material with an angle of 45° and therefore the force structure becomes pyramidal with a flat top, as shown in Figure 6.106:

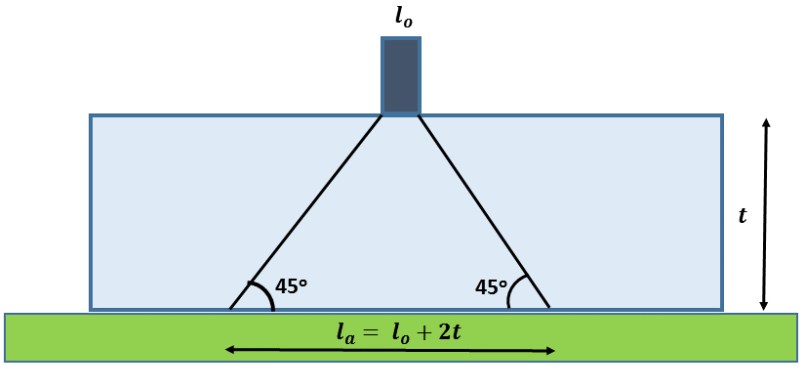


Figure *6.106:* Illustration of force distribution through PDMS. The tip has dimension of l_o which during force application creates a cone of action and the base of that cone decides how much force is being experienced by the sensor.

Here t (=0.3 mm) is the thickness of the PDMS layer, l_0 (=1.3 mm) is the length contact area, l_p (=1.3 mm) is the dimension of the sensing structure and since the angle is 45°, $l=l_0+2t=1.9$mm. The cone base is the circle with diameter of *l*, which is the area under the pressure of force, and the area of cone base is given by:

$$A_{conebase} = 0.25\pi l^2 = 0.25\pi * (l_0 + 2t)^2 = 2.835\text{mm}^2 \tag{6.36}$$

and area of piezoelectric sensing area was [7]:

$$A_{PVDF} = 0.6\text{mm} * 0.9\text{mm} = 0.54\text{mm}^2 \tag{6.37}$$

The stress on the PVDF surface can be estimated as:

$$T_{PVDF} = \frac{A_c}{A_{conebase}} * T = \frac{A_c}{A_{conebase}} * \left(\frac{F_c}{A_C}\right) = \frac{F_C}{A_{conebase}} \tag{6.38}$$

From equation (6.20), the force experienced by the piezoelectric layer get attenuated and can be written as:

$$F_{PVDF} = T_{PVDF} * A_{PVDF} = \frac{A_{PVDF}}{A_{conebase}} * F_c \tag{6.39}$$

Putting the values mentioned above, we get:

$$F_{PVDF} = \frac{A_{contact}}{A_l} * F_c = \frac{1.3^2\text{mm}^2}{1.9^2\text{mm}^2} * F_c = 0.468 * F_c \tag{6.40}$$

From equation (6.22), it can be seen that by adding a PDMS protective layer, the force through the PDMS get attenuated by a factor of 0.468 (for the experimental values) which will decrease the output since now when 1 N of force is applied to the contact area, only 0.468 N of force will be experienced by the piezoelectric layer.

Using equations (6.14)-(6.22) with the experimental values reported in [224], a good match was achieved, as can be seen from Figure 6.107, demonstrating the validity of the model.

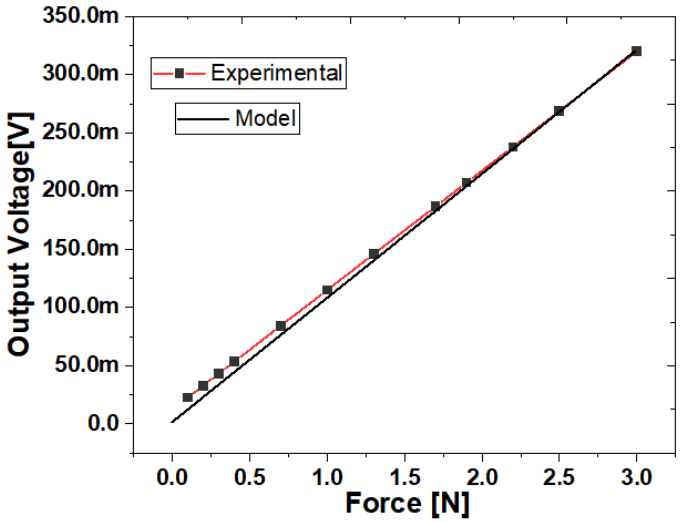


Figure 6.107: Plot of POSFET response vs Force (experimental and model).

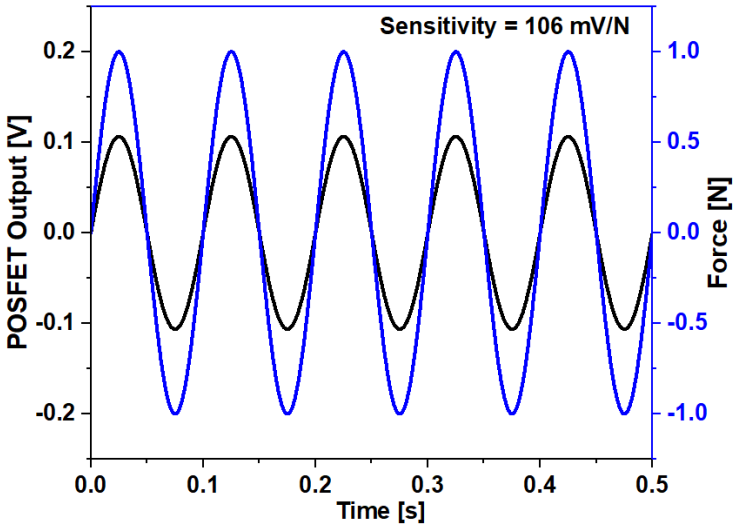


Figure 6.108: Modelled dynamic response of POSFET to 1N force.

The advantage of Verilog-A modelling lies in its ability to include the effect more variables when compared to SPICE based modelling tools. To demonstrate this ability, effect of temperature has been modelled. Since carrier mobility is inversely proportional to the temperature, so when temperature increases, the mobility decreases and thus the drain current decreases too. Assuming everything else constant, the increase in the temperature leads to decrease in POSFET output voltage as shown in

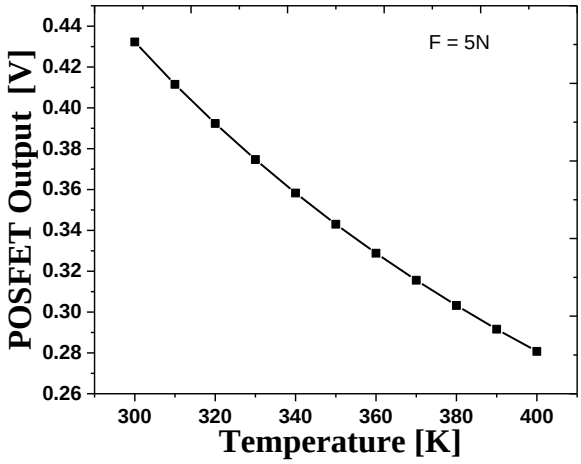


Figure 6.109: Effect of temperature on POSFET output voltage. The temperature was varied from room temperature (300K) to the higher range, and due to decrease in carrier mobility, the output decreases under the application of a constant force of 5N.

6.2.2. Bendable POSFET model

Analytical modelling and Verilog implementation of bendable POSFET was based on the modelling of piezo resistance led effect on the underlying MOSFET. In this study, it was assumed that the contact force and piezoelectric layer do not undergo any change during bending. Thus, when the sensing device was under bent condition, piezoresistive behavior of silicon came in to play. Piezoresistive behaviour means the change of electrical resistance for

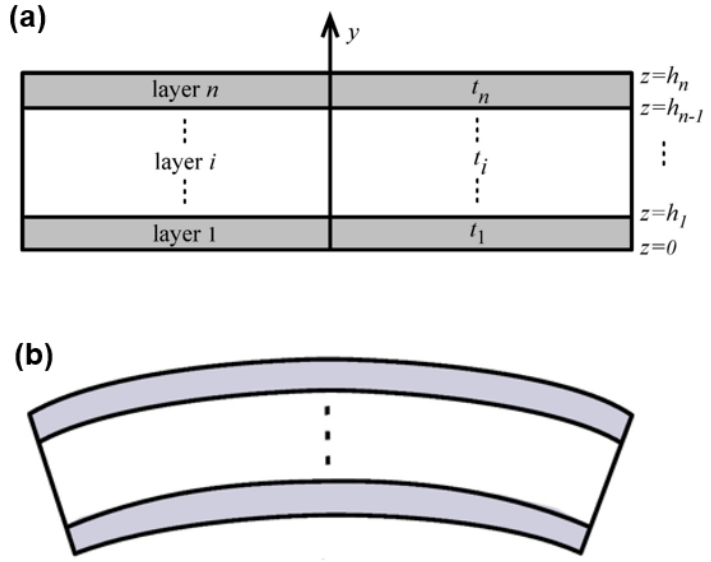


Figure 6.110: An elastic multilayer strip considered (a) without and (b) with external bending external bending.

a semiconductor device when mechanical strain/stress is applied. This effect of mechanical stress on field-effect transistors is of particular importance because it changes the carriers' mobility, threshold voltage and therefore changes the output characteristics of the device. Since these changes are directly dependent on the stress level experienced by the device, it was important to devise an equation set with which to formulate stress from the bending radius. Stoney's formula is generally used to calculate the stress in thin film over a flexible substrate, but it is applied only under the condition when the film is much thinner compared with the substrate. However, in the case of bendable POSFET, it was assumed that both the top layer (i.e. silicon) and the flexible substrate were of comparable thicknesses. So, instead of Stoney's formula, semi-analytical equations were formulated to calculate the strain and then multiplied by Young's modulus to get stress.

For an elastic multilayer strip with *n* layers, with individual thicknesses t_i, bonded sequentially, as shown in Figure 6.110, the strain at a location y in the stack is given by:

$$\varepsilon = c + \frac{y - t_b}{R_c} \tag{6.41}$$

Where ε is strain, c is the uniform strain component due to the thermal expansion which was assumed to be zero here, y is the location at which strain needs to be calculated, t_b is the bending axis location, R_c is the radius of curvature.

The bending axis location depends on the type of materials and their thicknesses, and can be written as:

$$t_b = \frac{\sum_{i=1}^{n} E_i * t_i * (2 * h_{i-1} + t_i)}{2 * \sum_{i=1}^{n} E_i * t_i} \tag{6.42}$$

Where E_i is the Young's modulus of i^{th} material, ti is the thickness of the i^{th} layer and h_i is the height at which the layer *i* is located, which is the sum of the layer thickness from layer 0 to layer i^{th}.

Assuming that 20 μm thick silicon is packaged on 50 μm thick polyimide substrate, the bending axis location is at 56.8 μm from the bottom, and the Young's modulus of silicon being 179 GPa, stress can be calculated over the top surface of silicon using equation (6.23), and values of which for some bending curvature is tabulated in Table 6.13.

Table 6.13: Stress value at different bending curvatures for 20 µm thick silicon on 50 µm thick polyimide.	
Rc [mm^{-1}]	Stress [MPa]
10	200.48
30	66.82
50	40.09
70	26.64
90	22.27

Once the stress has been calculated, it was required to model how this stress changes the current of MOSFET. The current equations of a n-channel MOSFET in different regions are:

Cut off $I_{ds}=0$ (6.43)

Linear
$$I_{ds} = \mu_n * C_{ox} * \frac{W}{L}\left[(V_{gs} - V_{th}) * V_{ds} - \frac{V_{ds}^2}{2}\right] * (1 + \lambda * V_{ds}) \quad (6.44)$$

Saturation
$$I_{ds} = \frac{1}{2} * \mu_n * C_{ox} * \frac{W}{L} * (V_{gs} - V_{th})^2 (1 + \lambda * V_{ds}) \quad (6.45)$$

The drain current depends on the carrier mobility, threshold voltage and structural dimensions for a given set of bias voltages and for small variations in saturation region, the normalised change in output drain current can be written as:

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta \mu}{\mu} - 2 * \frac{\Delta V_{TN}}{V_{TN}} * \left(\frac{V_{TN}}{V_{GS} - V_{TN}}\right) \quad (6.46)$$

It was also demonstrated that the variation of threshold voltage only has a very weak relationship with the applied stress and it is essentially independent of the applied stress and the reported variation of threshold voltage is caused by the contact resistance [225]. This observation can be proven by the experimental results from AT Bradley et al.[226], which also satisfies the theory from Mikoshiba [227]. Therefore, here the variation of threshold voltage is assumed to be negligible as a result, the Equation (25) can be simplified as:

$$\frac{\Delta I_D}{I_D} \cong \frac{\Delta \mu}{\mu} \tag{6.47}$$

Nevertheless, unlike bulk Si, the carrier mobility changes in the channel region of MOSFETs is much more complex due to two reasons [61]. Firstly, apart from the scattering on photons and impurities, the carriers' mobility is also affected by the scattering at the t_{ox} interface of a MOS transistor by Coulomb force [62]. Due to this, the carriers' mobility of surface is much lower than in the bulk Si [61]. In addition, in a NMOS, $\Delta 4$ and $\Delta 2$ valleys are nondegenerate even at the planner condition, the energy splitting between $\Delta 4$ and $\Delta 2$ valleys depending on the magnitude of the electric field [63]. In the presence of stress, this degeneracy further widens up.

In the strong inversion operation region, for either linear or saturation region, MOSFET current is controlled by the resistive behaviour of the channel. Since the change in resistance can be written as the product of stress and piezoresistive coefficients, the variation of the drain current of 0°and 90° oriented channel under stress can be written as:

$$\left.\frac{\Delta I_D}{I_D}\right|_0 = \frac{Л_S}{2} * (\sigma'_{11} + \sigma'_{22}) + \frac{Л_{44}}{2} * (\sigma'_{11} + \sigma'_{22}) + Л_{12} * \sigma'_{33} \tag{6.48}$$

$$\left.\frac{\Delta I_D}{I_D}\right|_{90} = \frac{Л_S}{2} * (\sigma'_{11} + \sigma'_{22}) - \frac{Л_{44}}{2} * (\sigma'_{11} + \sigma'_{22}) + Л_{12} * \sigma'_{33} \tag{6.49}$$

where $\sigma'_{11}, \sigma'_{22}, \sigma'_{33}$ are the three normal stress resolved in the primed coordinate system and $Л_{ij}$ represents the piezoresistive coefficient of the MOSFET. In this work, 0° channel orientation and uniaxial stress are considered, therefore, $\sigma'_{22}, \sigma'_{33}$ can be ignored. Comparing equation (6.29) and (6.30), it can be reduced as:

$$\left.\frac{\Delta \mu}{\mu}\right|_0 = \left(\frac{Л_S + Л_{44}}{2}\right) * \sigma \tag{6.50}$$

Furthermore, the parameter $\left(\frac{Л_S + Л_{44}}{2}\right)$ is referred to as effective piezoresistive coefficient $Л_{eff}$. From equations (6.29) and (6.32), it can be seen that with effective piezoresistive coefficients

value and stress, the theoretical variation of drain current could be evaluated. AT Bradley *et al.* [226], calculated the piezoresistive coefficients for n-type and p-tpe MOSFET fabricated in three independent foundaries (IBM, Texas Instruments and Lucent Technologies), which are listed in Table 6.14.

Table 6.14: Piezoresistive coefficients for MOSFETs on (100) silicon ($* \mathbf{10^{-12}Pa^{-1}}$) [226]

Piezoresistive Coefficient	IBM	Texas Instruments	Lucent Technologies
$Л_s^n$	800	570	850
$Л_{44}^n$	100	70	150
$(Л_s^n+Л_{44}^n)/2$	450	320	500
$Л_s^p$	-50	-30	-200
$Л_{44}^p$	-950	-800	-100
$(Л_s^p+Л_{44}^p)/2$	-500	-415	-150

Multiplying the effective piezoresistive coefficient with the maximum value of the stress (when bending radius=10 mm), the percentage variation in drain current was calculated for each set of piezoresistive coefficient and tabulated in Table 6.15.

Table 6.15: Product of effective piezoresistive coefficient and stress (~200 MPa) and current variation.

Piezoresistive Coefficient	IBM	Texas Instruments	Lucent Technologies
$(Л_s^n+Л_{44}^n)\frac{1}{2} * 10^{-12}\text{Pa}^{-1}$	450	320	500
Variation in current (%)	9	6.4	10
$(Л_s^p+Л_{44}^p)\frac{1}{2} * 10^{-12}\text{Pa}^{-1}$	-500	-415	-150
Variation in current (%)	-10	-6.32	3

From the table above, it can be observed that the variations between the three sets of data for drain current have no significant difference (due to $x10^{-12}$ factor) and so the IBM data was chosen for the following calculations. Based on these, the final equation used to model the piezoresistive behaviour effect on drain current is written as:

$$I_d = I_{d0} * (1 \pm \text{effective piezoresistive coefficient} * \text{stress}) \quad (6.51)$$

Where I_{d0} is the drain current in planar condition when no bending occurs. From equation (30), it can be seen that in NMOS for tensile stress (positive bending curvature), the drain current will be increased and for compressive stress (negative bending curvature), the drain current will be decreased. Moreover, since the piezoresistive coefficient for PMOS device is negative value, the effect of piezoresistive behaviour is opposite with NMOS where tensile stress gives a lower drain current and compressive stress gives a higher drain current.

For establishing the model, first level BSIM4 model parameters were used along with the above derived equations, to plot the effect of bending on drain current of MOSFET. As can be observed from Figure 6.111, drain current increases for tensile stress (positive R_c), whereas it decreases for compressive stress (negative R_c). This model is further validated with experimental results in Chapter 7.

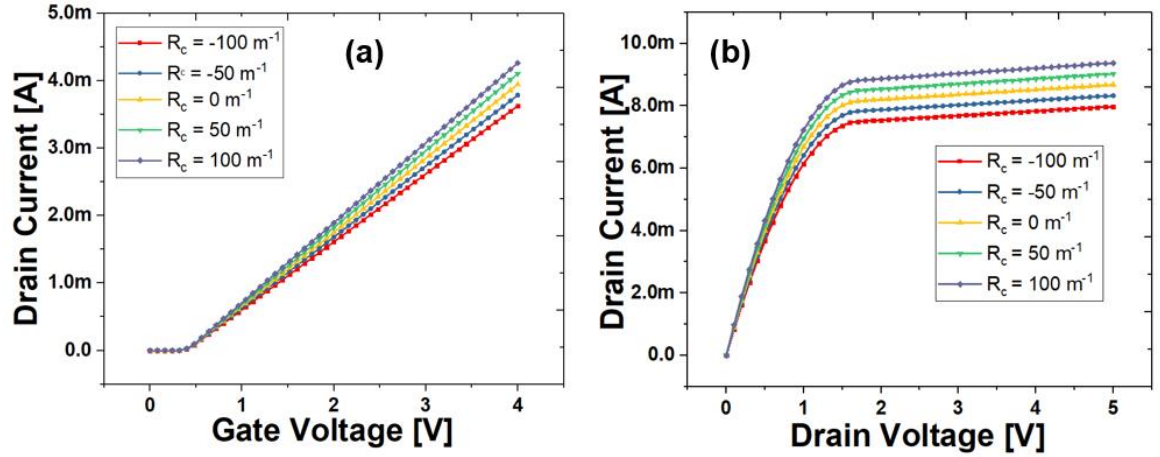


Figure 6.111: (a) Transfer (b) Output characteristics of MOSFET under different bending conditions. As the bending move from tensile state to the compressive state, decrease in the current can be observed.

Finally, these equations, along with the experimentally derived parameters, were written in Verilog-A to simulate the POSFET behaviour to dynamic force at different bending curvature, and plotted as Figure 6.112.

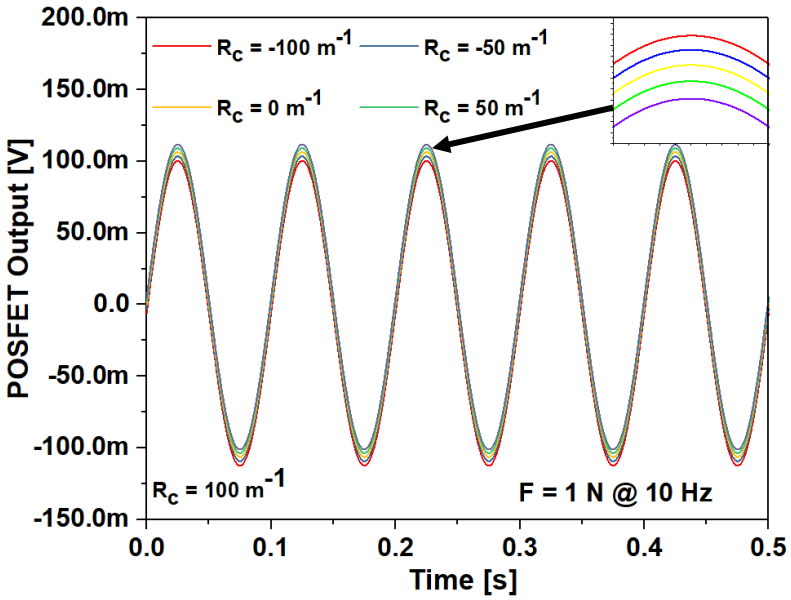


Figure 6.112: POSEFT output with sinusoidal force applied under different bending conditions. Under tensile stress, increase in drain current can be observed and opposite for compressive stress.

6.2.3. Stress compensated circuit design using POSFET

The bending stress affects the transistor's performance and consequently varies the output signals of the analogue and digital circuit building blocks. Furthermore, in CMOS based sensors, such as POSFET and ISFET, stress may introduce offsets that affect the sensitivity and detection of static and low frequency signals. The bending induced stresses and strains brings variations in electrical parameters such as charge carrier mobility and threshold voltage. The bending induced effects can bring significant deviation in the response of flexible electronics from their designed values and may influence their effective use in the target application. Therefore, it is critical to understand the behaviour of devices and circuits under different bending conditions by understanding the dependence between mechanics, solid-state physics, and electrical and electronic inputs.

In order to fabricate ICs that function within specifications, both planar as well as during mechanical deformation, the effects of stress must be considered in the design process. Sometimes it is also required to nullify the bending effect on the devices, to ensure the accuracy of circuit behaviour. The strategies to mitigate stress effects in flexible electronics is likely to gain more importance as the flexible electronics research makes it way to the market. There have been few attempts to minimize or compensate the effects of bending-induced stress on devices and circuit level. The three main approaches which have been reported so far include (1) placing or embedding the device and circuits in the neutral plane so that they experience

zero or minimum stress, (2) distributed islands of rigid and stiff electronic components on flexible and stretchable substrates which can take major part of the stress by stretching or contracting themselves and keeping the functional devices under no stress, and (3) optimal layout orientation for the circuits, and considering the expected bendability during use [214].

Since different applications have different sets of requirements which lead to varied specifications. For example, in case of force sensors, if the range of force to be experienced by the sensor is not pre-defined, then the sensor needs to maintain reliable functionality in a wide range of applied contact force. For this reason, the POSFET device was biased in common drain mode, popularly known as source follower configuration [228, 229]. The major advantages of this configuration was it's less than unity gain, which makes wide range force detection possible. On the other hand, when the sensor output is limited by the available voltage line, the range of applied force becomes limited. For example, in e-skin for robots the preferred range is based on human daily sensing range (0.1-1 N) [230]. The output voltage produced for this range of force should be within the maximum voltage available at the supply. Considering these, a new operational amplifier circuit configuration was proposed, where one of the transistors in a differential pair has been replaced with a bendable POSFET model. The differential amplifier configuration nullifies the noise which was common to both the inputs and amplifies the difference created by touch event. Furthermore, the amplifier was designed with techniques including chopper stabilisation and correlated double sampling. Chopper stabilisation constantly corrects low-frequency errors across the inputs of the amplifier. This compensates for low-frequency errors such as input offset voltage, input bias current, temperature drift, or pink (1/f) noise. Similarly, correlated double sampling allows the removal of any undesired offset due to bending during measurements.

Figure 6.113 (a) shows the simplified block diagram of the proposed microsystem. This scheme employs the bendable MOS transistors implemented by Verilog-A description using the parameters extracted from a standard 0.18-µm CMOS technology.

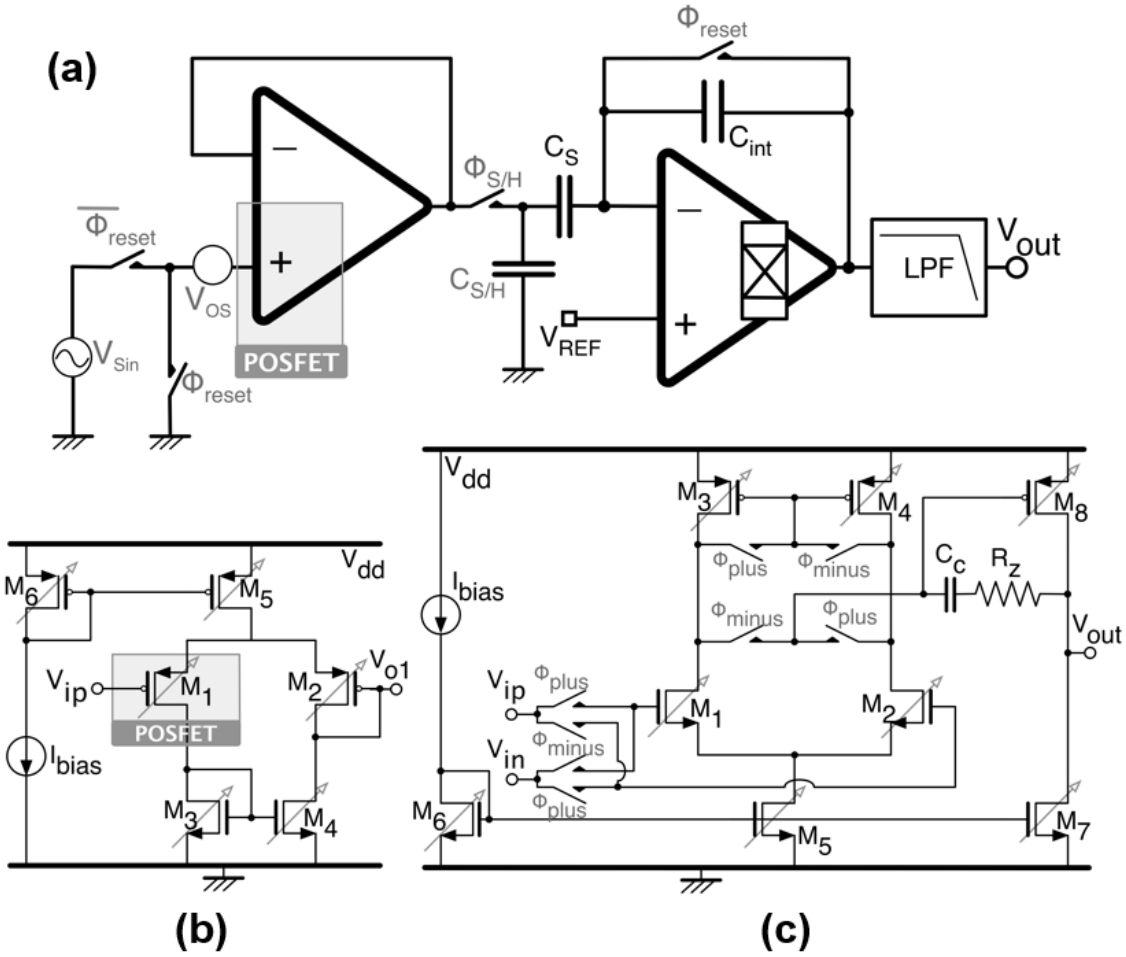


Figure 6.113: (a) Block diagram of the proposed readout circuit for POSFET microsystem. (b) Schematic diagram of the POSFET biasing as voltage follower, and (c) Schematic circuit diagram of two stage single-ended amplifier. [223]

The proposed scheme utilises the POSFET in a differential pair as a positive input transistor to configure a voltage follower, as shown in Figure 6.113(b) and Figure 6.113(c) shows the two stage chopper amplifier with chopping frequency of 40 kHz, which was employed in the integrator. In order to avoid output buffers, a switched-capacitor, used as a low pass filter (LPF), was used to drive the output pins [231]. 0.18-µm CMOS technology was used for designing the circuit and biasing was simulated using a current source of value 1µA. The chopper amplifier was biased with current of 10 µA and voltage 1.8 V. Resetting frequency and chopping clock frequency was set to 1.25 kHz and 40 kHz, respectively. A sinusoid input signal with amplitude of 2mV corresponding to the piezopotential produced by applied force was used on the top electrode of the piezoelectric layer. The proposed circuit function as follows: When the POSFET based op-amp is configured as voltage follower, any difference in

the input stage generated due to contact event gets amplified at the output terminal. This amplification can be tuned so that the output remains below the maximum voltage value.

Figure 6.114 shows the timing diagram and waveforms of the input and output of the POSFET readout circuit. The proposed circuit was also simulated under compressive and tensile bending states with bending curvatures of 1.5 m^{-1} in both conditions. Simulation of the POSFET with readout circuit shows 12.5% increase in peak-to-peak voltage for compression and 9% reduce in peak-to- peak voltage for tension.

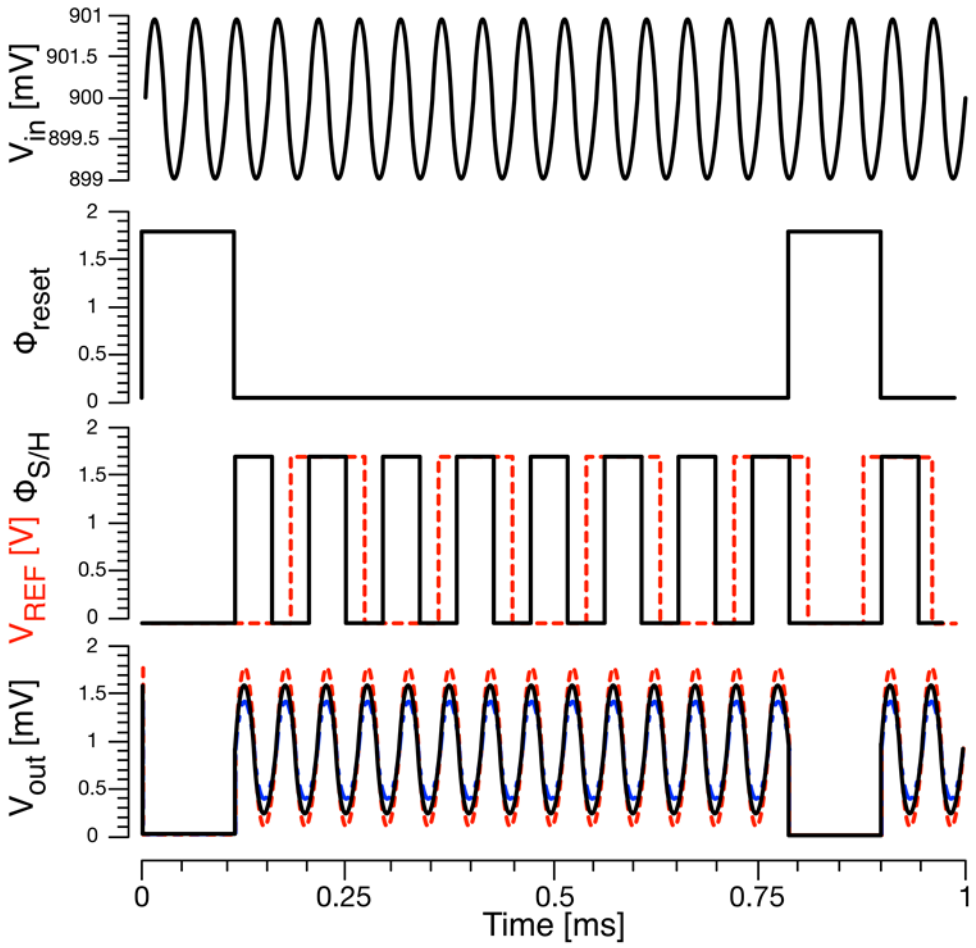


Figure 6.114: Simplified timing diagram of a complete readout operation with transient response of output voltage. Black line shows the output voltage in planar state, where the red and blue dotted lines show the transient response under compression and tension, respectively. [223]

6.3. Modelling the effect of bending on CMOS inverter

After modelling the bending effect in n-MOSFET, similar steps were taken to model p-MOSFET, and both models were combined to model the behaviour of CMOS inverter under different bending conditions. For the inverter, NMOS with aspect ratio of 1/0.6 and PMOS with aspect ratio of 1/0.18 was implemented in Cadence Virtuoso. The DC voltage sweep of 1.8V was applied for sets of both tensile stress and compressive stress with different bending radius, and the DC characteristics can be seen in Figure 6.115:

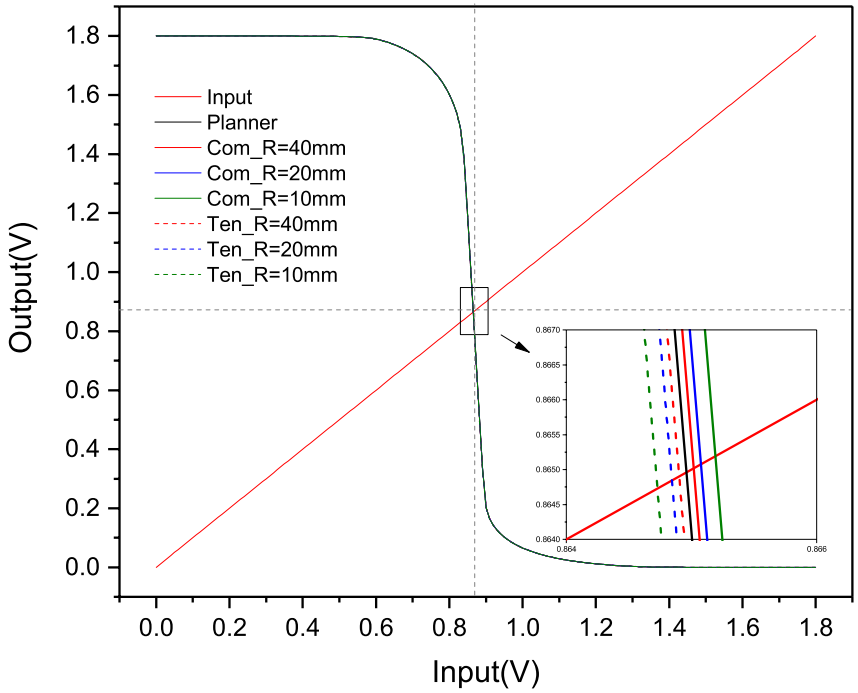


Figure 6.115: DC characteristics of inverter with different bending radius in both tensile (dashed lines) and compressive stress (solid lines). The middle voltage point decreases under tensile and increases under compressive

The middle voltage V_M, the input-high voltage V_{IH} and input-low voltage V_{OH} under different bending conditions are tabulated in Table 6.16.

Table 6.16:Characteristic parameters of inverter under different bending condition

Inverter	V_M(V)	A_V	$V_{IH}(V)$	$V_{IL}(V)$
Planner	0.8649	5.685	1.023	0.706

Tension 40 mm	0.8648	5.60	1.025	0.704
Tension 10 mm	0.8646	5.567	1.026	0.703
Compression 40 mm	0.8650	5.70	1.022	0.707
Compression 10 mm	0.8652	5.786	1.021	0.709

The middle voltage point V_M shifts slightly due to bending. The main reason behind the shift of V_M could be its high dependence on the $\frac{\beta_p}{\beta_n}$ ratio. As the hole mobility increases and electron mobility decreases under compressive stress, the V_M increase under compressive stress and vice-versa occurs in tensile stress. As the V_M changes slightly, the gain, V_{IH} and V_{IL} also change. These simulated trend is in line with the experiments reported in [232] and further experimentally verified in Chapter 7.

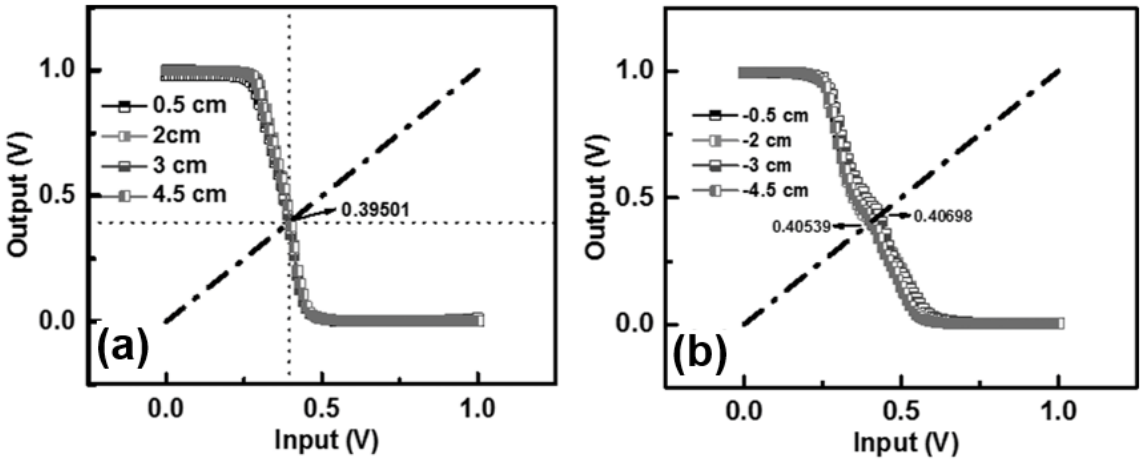


Figure 6.116: VTC characteristics of flexible inverters at (a) Tensile stress (b) Compressive stress. [232]

6.4. Conclusion

The analysis of bending stress on the device performance is an important area of area in thin-silicon technology. Since the bending generated stress affect the mobility and other parameters of device, it is required to predict the shift so that the design and the system can be tuned to ensure the proper operation and behaviour. This chapter presented the work done in analytical modelling of the bending effect, which is compared with the experimental results in Chapter 7. The model of POSFET was developed using standard semiconductor and ferroelectric physics and on combining with the force attenuation due to protective layer, the model showed close

matching with the experimental data. Using this model, POSFET was incorporated in two-stage single-stage amplifier and with some stress-compensation blocks, the circuit was simulated to analyse the effect of bending. During this work, model for change in the drain current of MOSFET was developed using piezoresistance theory. The change in mobility was considered to be major contributor towards the shift in current, and have been studied using concept of band-splitting under stress. The model was implemented in Verilog-A for NMOS and PMOS, and combined to analyse simple circuit like inverters. The work presented in this chapter emphasis on the importance of modelling required for development of models which can capture the effect of bending, and facilitate the circuit designers to design robust system in flexible electronics. Moreover, due to advantageous properties offered by Verilog-A, the developed model can be extended to included the effect of variation in temperature and humidity of environment around sensor. Since temperature and environmental condition has major effect on drain current of transistor, it is important to include these effect on sensor performance. This kind of full model will all kind of variations may lead to more complete model for flexible devices. In addition, some tactile sensors are able to detect to more than one variation, such as pressure and temperature simultaneously without any interference from other. These sensors are called multi-modal sensors and can be modelled in Verilog-A as the effect of individual cause can be modelled separately and then integrated together. These kind of works where more than one effect are modelled together can be an important addition to the current state of flexible electronics device modelling.

Chapter 7. Results and Discussion

This chapter presents the electrical and electro-mechanical characterisation performed for establishing the working nature of devices and sensors. The results are presented in the same sequence as they are discussed in the previous chapters. Firstly, characteristic curves of MOSFETs fabricated with modified process and mask set, discussed in Chapter 4, is presented. Following which, the electrical test conducted with P(VDF-TrFE)/BT nanocomposite and AlN thin film fabricated in Chapter 4 is presented, along with their feasibility as piezoelectric layer for tactile sensors, is being demonstrated. Finally, the effect of thinning and bending on the optical and electrical properties of ultra-thin silicon based devices realised in Chapter 6, is discussed.

7.1. MOSFET characterisation

The characteristic curves of MOSFET were obtained using a Summit 12k Autoprober and a semiconductor parameter analyser. The obtained output characteristics, transfer characteristics, channel conductance and transconductance show the functioning of the devices.

7.1.1. Single MOSFET characterisation

The output, transfer, channel conductance and transconductance plots of MOSFET fabricated using the steps discussed in Chapter 3 are plotted as Figure 7.117(a-d) and the extracted parameters are tabulated in Table 7.17.

Table 7.17: Measured and extracted parameters of fabricated MOSFET

Parameters	Value
Channel length	12 μm
Channel width	2000 μm, 2500 μm
Oxide thickness	50 nm
Mobility	695 cm^2/V-S
Threshold voltage	0.68 V
Maximum transconductance	0.44 mS

The channel length was decided by the available technology at the fabrication facility and was fixed at 12 μm to make sure the proper lithography pattern development. Since the device was designed to be used as sensor with high sensitivity, so it was decided to have a high aspect ratio, since sensitivity is directly proportional to the aspect ratio of transistor. Keeping in mind,

the area of one taxel (~1 mm x 1 mm), the channel shape was designed in serpentine manner with two different widths, 2000 µm and 2500 µm.

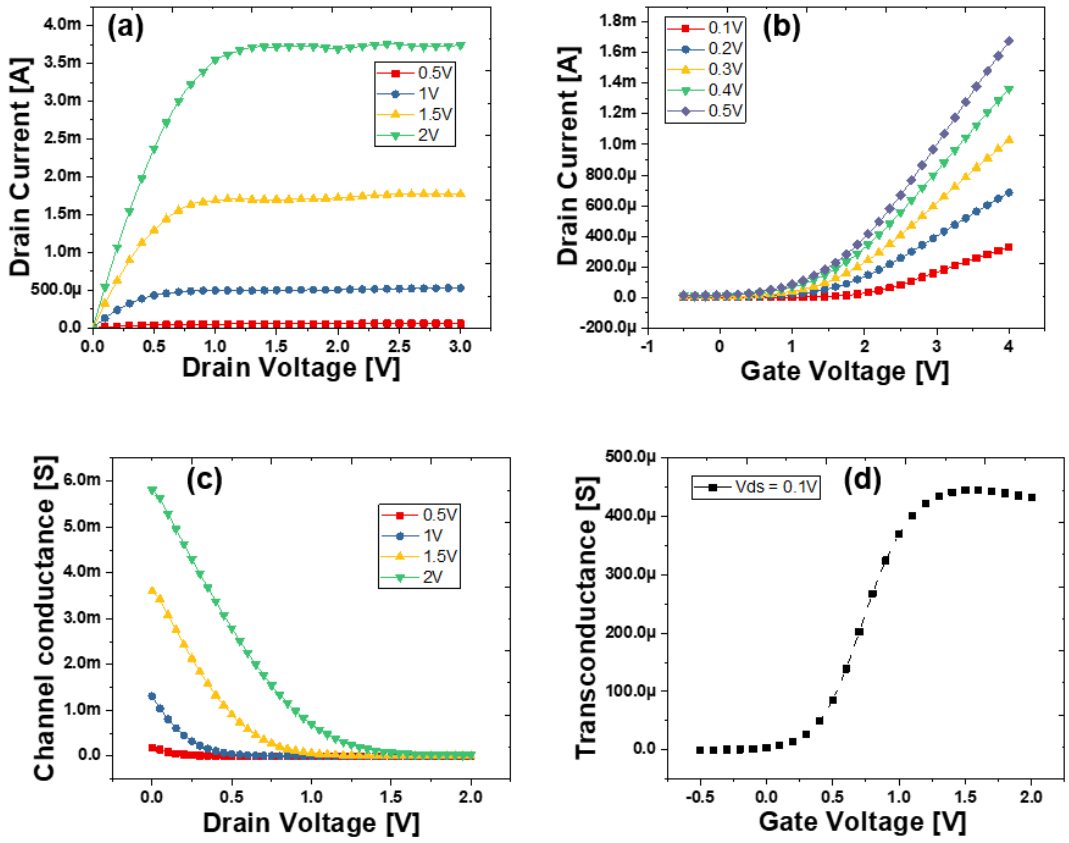


Figure 7.117: (a) Output characteristics of MOSFET at different gate voltages (b) Transfer characteristics of MOSFET at different drain voltages (c) Channel conductance of MOSFET at different gate voltages (d) Transconductance plot of MOSFET at drain voltage of 100 mV.

7.1.2. 2x2 array MOSFET characterisation

The chip of size 1 cm x 1 cm, has 2x2 MOSFET with shared top electrode. Each MOSFETs were characterised separately to check their functioning and have been plotted in Figure 7.118-Figure 7.121.

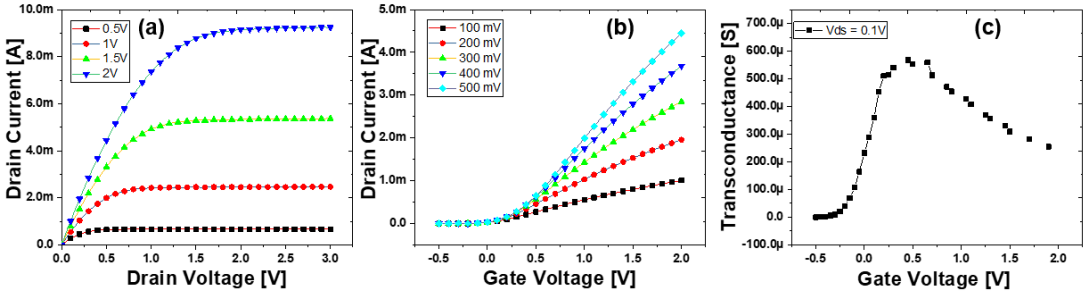


Figure 7.118: (a) Output (b) Transfer characteristics (c) Transconductance plot of 1st element of 2x2 array.

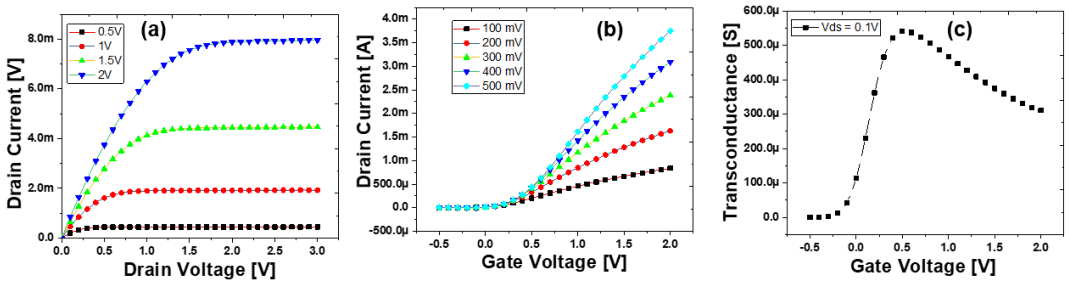


Figure 7.119: (a) Output (b) Transfer characteristics (c) Transconductance plot of 2nd element of 2x2 array.

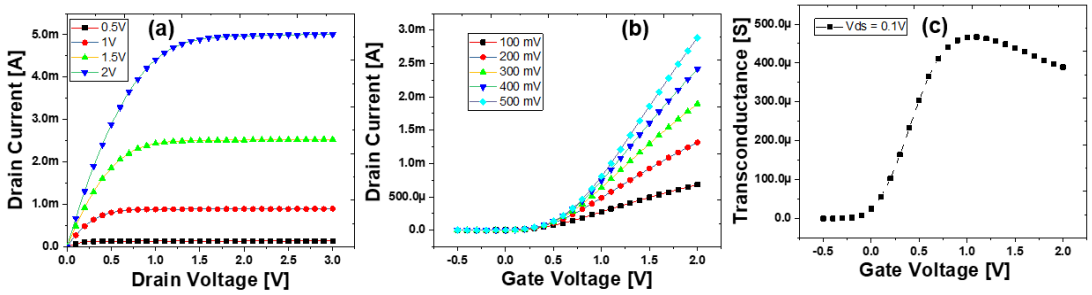


Figure 7.120: (a) Output (b) Transfer characteristics (c) Transconductance plot of 3rd element of 2x2 array.

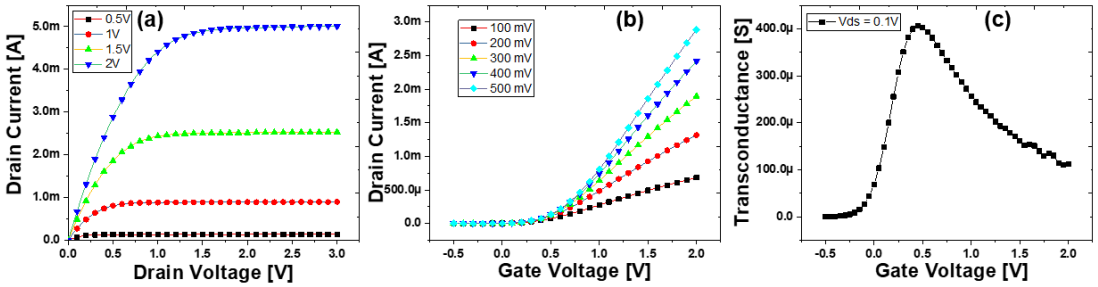


Figure 7.121: (a) Output (b) Transfer characteristics (c) Transconductance plot of 4th element of 2x2 array.

As can be observed from the plots, the drain current for the first and second device is higher as compared to third and fourth devices. This change in the threshold voltage could be attributed to the variation in the threshold adjustment implant received during the implantation step. Nevertheless, it is noteworthy to mention that even after the variation on two devices, all of them demonstrated the functionality of device.

7.2. Electrical characterisation of ultra-thin piezo capacitor

7.2.1. Electrical Impedance Spectroscopy

Electrical impedance spectroscopy (EIS) involves the measurement of the output electrical potential (V_{out}), and the phase shift (φ) of a system when an alternating current of small amplitude (I_{out}) and known frequency ω is applied. An impedance analyser (HP LF 41928) was used to measure the impedance of the piezocapacitor over a frequency range of 5 Hz–10MHz. As shown in Figure 7.122(a), capacitive behaviour was observed over a wide frequency range. The capacitance value can be calculated by fixing a frequency. The value of capacitance was also confirmed by Cascade MircoTech PM5 probe station. The measured value was 1.14 nF and knowing the electrode area (0.197 cm^2) and polymer thickness (2 µm), the relative permittivity was calculated to be 13.1.

7.2.2. Sensor characterisation

The sensor electro-mechanical characterisation was performed using TIRA shaker setup, shown in Figure 7.123©. The shaker tip applied the force with frequency 70 Hz and the magnitude of force was controlled using power amplifier. The sensor exploited the basic piezoelectric property of P(VDF-TrFE) of converting force into charge. To explain briefly, when the piezoelectric sensing structure experience force, the charges on the polymeric chain become out of balance. This effect of charges does not cancel each other, so net charges appears on both side of material. A charge amplifier circuit with amplification factor of 10, was designed to read this charge and convert into voltage. The force applied by shaker was recorded by the force sensor and the output produced across the terminals of capacitive sensor was collected by a programmed Data Acquisition (DAQ) board, the characteristic curve with sensitivity ~120 mV/N can be seen in Figure 7.123(a).

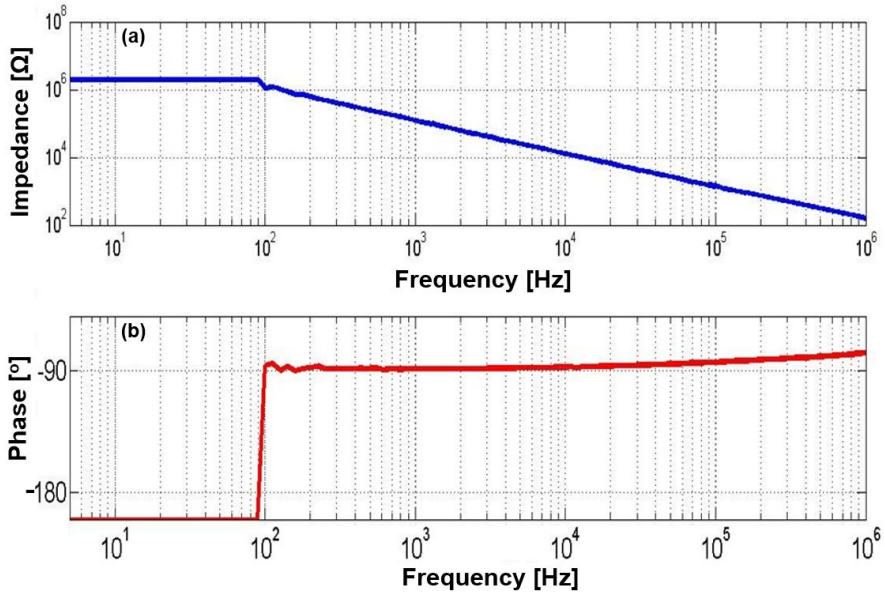


Figure 7.122: (a) Magnitude and (b) Phase plot of ultra-thin silicon-based piezocapacitor. These plots confirms the capacitive behaviour of fabricated device and the obtained data was used to calculate the dielectric constant of material.[233]

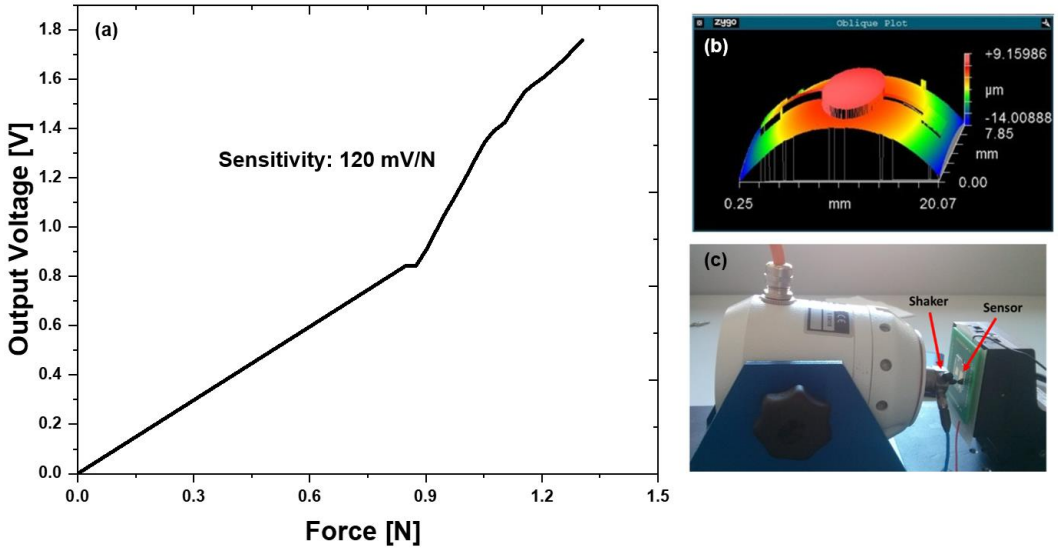


Figure 7.123: (a) Sensor characteristic curve obtained by varying the force level over the sensing structure. The sensitivity of 120 mV/N was obtained during characterisation. (b) Optical profilometer scan of one sensing device where the warping effect due to low thickness can be observed. (c) The image of measurement setup consisting of a TIRA shaker, a piezotronic force monitor and the sample holder. [233]

7.3. P(VDF-TrFE)/BT nanocomposite for tactile sensing application

7.3.1. Electrical characterisation of nanocomposite

The dielectric properties such as impedance, loss tangent and permittivity of the nanocomposite were measured with impedance analyser, summit 12k Autoprober and Keysight B1500A semiconductor parameter analyser. The capacitance-voltage curves shown in Figure 7.124(a), obtained at different frequencies (10 kHz, 50 kHz, 100 kHz, 1 MHz), confirm the capacitive behaviour of the structure. The dielectric permittivity was calculated over 1 kHz to 3 MHz frequency range (Figure 7.124(b),) using

$$\varepsilon = \frac{Cd}{A\varepsilon_o} \tag{7.52}$$

and it shows the permittivity enhancement of around 30%, which is credited to space charge confinement. The permittivity enhancement has been used extensively for applications such as energy harvesters and energy storage [182, 183]. The impedances measured over 1-100 kHz do not change much w.r.t. each other at high frequency, as can be noted from Figure 7.124(c). At higher frequencies, the merging of impedance suggests that there is a release of space charges which is a responsible factor for the enhancement of AC conductivity [234].

The loss tangent was calculated for the frequency up to 3 MHz using

$$tan\delta = \frac{1}{2\pi f R_p C_p} \tag{7.53}$$

where R_p and C_p are the parallel mode resistance and capacitance of sample. The loss tangent decreases in the P(VDF-TrFE)/BT composites, particularly at higher frequencies, as shown in Figure 7.124(d). This can be attributed to the glass transition relaxation of the P(VDF-TrFE) polymer matrix [235].

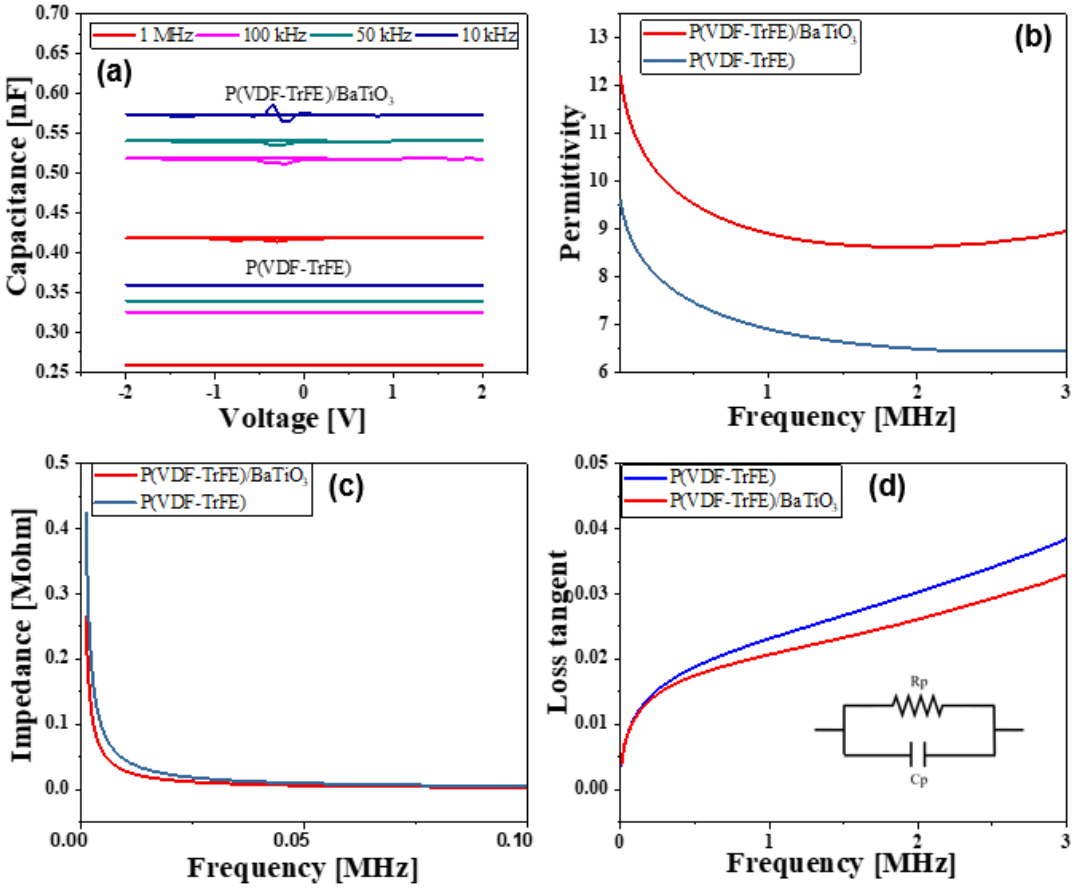


Figure 7.124: Electrical characteristics plot of P(VDF-TrFE)–BT nanocomposite. (a) Capacitance vs Voltage, (b) Dielectric Permittivity vs Frequency (c) Impedance vs Frequency, (d) Loss tangent vs Frequency. [188]

7.3.2. Sensor characterisation

Firstly, the sensor was characterised as it is by connecting the top and bottom electrode of sensor to LCR meter. The change in capacitance on application of force was monitored using the LabView programme. The zero force capacitance value was measured to be 5.6 nF and a constant force of 45 mN was applied and released at regular intervals of 2 seconds to simulate a tapping form of touch. A custom made pressing setup, as shown in Figure 7.125 was used to apply the tapping force and the magnitude was measured by a load cell situated beneath the sensor.

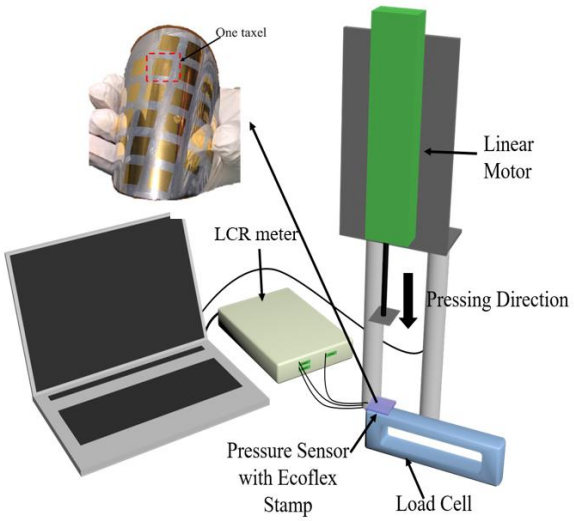


Figure 7.125: The schematic of setup used for characterising the nanocomposite sensor. It consisted of a LabView controlled pressing setup and a load cell for monitoring the magnitude of applied force,

With every event of touch, ~10 pF increase in capacitance was observed, which returns to steady state value upon release, as can be seen from Figure 7.126(a). The stimulus can be approximated as a pulse wave with period of 1.6 seconds and have also been plotted alongwith the sensor response. Since P(VDF-TrFE) is a semi-crystalline polymer, change in thickness can be neglected and it can be said that the change in capacitance is due to the piezoelectric effect of the composite. Due to piezoelectric effect of material, on the application of force, charges appeared in the dielectric of capacitor, and since due to more charges in capacitor, capacitance value increases. Secondly, the sample was placed on a hotplate and the temperature was gradually increased to characterise its sensitivity towards temperature. The room temperature was 27^{o}C and the initial capacitance at room temperature was measured to be 5.6 nF. With increase in temperature, the capacitance increases, as shown in Figure 7.126(b). The measurement was done up to 60^{o}C, which is encountered as high temperature in daily life activities and the sensor shows a linear response with sensitivity up to 54pF/^{o}C. The increase in capacitance with temperature is attributed to the increase in composite permittivity, since dielectric permittivity of any material depends on electronics, ionic, dipolar and interfacial polarisations. Among these, the effect of temperature on ionic and electronic polarisation is very small, so increase in permittivity is directly related to increase in interfacial polarisation of BT due to the creation of crystal defects and decrease in dipolar polarisation due to increase in randomness of dipoles.

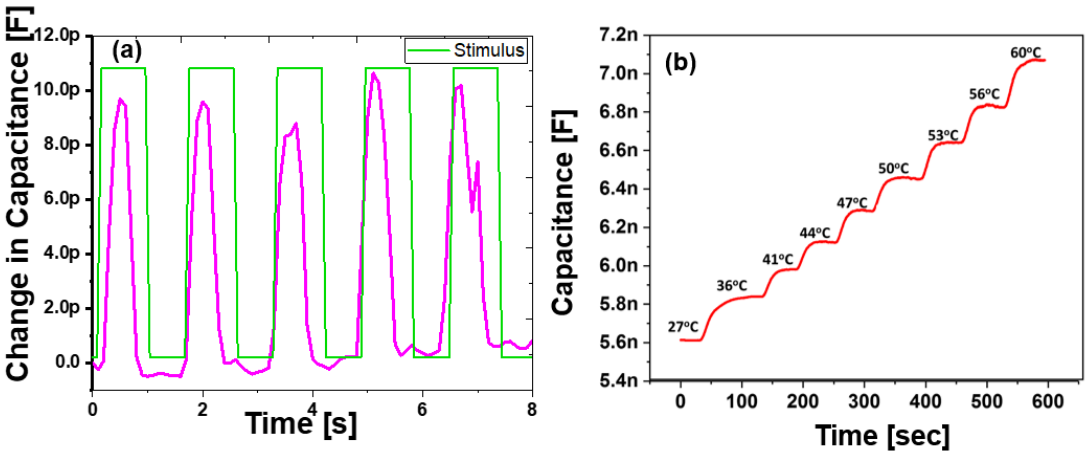


Figure 7.126: Response of sensor to (a) periodic force of magnitude 45 mN (b) *stepwise increase in temperature.* [196]

7.3.3. Characterisation in extended gate configuration

The sensing structure composed of P(VDF-TrFE)/BT nanocomposite was coupled to MOSFET in extended gate configuration, as shown in Figure 7.127(a). The extended gate configuration allows faster detection due to high switching speed of transistor and quick conversion from charge to voltage. The experimental setup for mechanical stimulation is shown schematically in Figure 7.127(b). It consisted of a rigid frame for mounting the sensor and an electro-mechanical shaker (TIRA model). The sensing structure was placed over the frame and covered with 100 μm thick layer of polydimethylsiloxane (PDMS) for protection during the contact event. The shaker was controlled via a closed loop feedback programme to ensure the precise value of force. The tip of the shaker was mounted with a piezoelectric force transducer (ICP Force sensor). The tip with the contact area of 0.011 m^2, resulted in force to pressure conversion of 1N → 91 Pa. The sensor was characterised using common-drain or source follower topology, in which the FET's drain terminal and top electrode of sensing layer was biased at 3V. The source of FET was connected to 1MΩ pull-down resistor. The output voltage was recorded across the resistor at varying force magnitude. When a human body comes into contact with the surface of an object the amount of force produced is typically less than 2.0 N and this force can be taken as a centre of ballpark

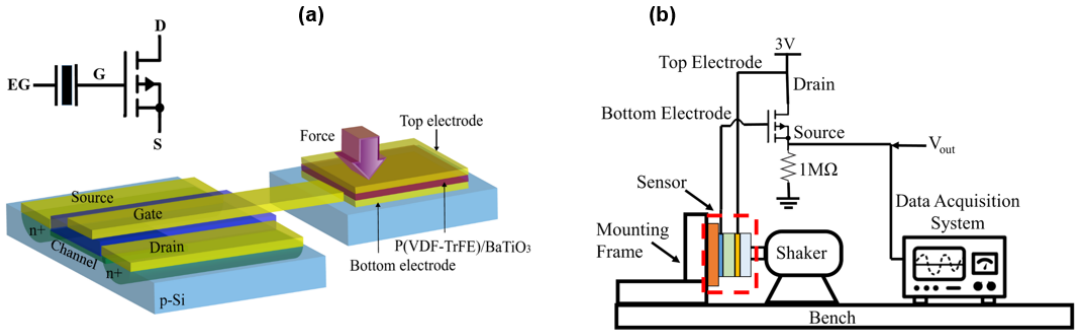


Figure 7.127: (a) Illustration of P(VDF-TrFE)-BT nanocomposite coupled to a MOSFET in extended gate configuration and its symbolic representation.(b) Schematic of characterisation setup. [188]

area reference for the mechanical stimuli without causing any pain. Moreover, the response time in which a human completes all processing of tactile stimuli from contact detection to response output is 100–200 ms [236]. Therefore, force with magnitude from 1N-4N and frequency 5 Hz was applied. Similarly, for its characterisation as temperature sensor, temperature range was varied from ambient temperature to 70^{o}C, which is the temperature range that is required for most tactile applications [237]. During the sensitivity to temperature measurement, the temperature was ramped in steps of 1^{o}C from room temperature, in order that the difference between the two subsequent temperature levels was 1^{o}C.

The sensing mechanism can be briefly explained as follow: Upon application of force/temperature, the charges are produced in composite due to virtue of piezo/pyroelectricity of composite. Since the composite is capacitively coupled to the gate of MOSFET, any extra charge appearing in the composite. modulates the gate voltage of the transistor to maintain the charge neutrality condition, as discussed in Chapter 6. The modulated gate voltage in turn changes the drain current, as the drain current is directly proportional to the square of gate overdrive voltage. The change is drain current was measured as change in voltage across the resistor connected at the source terminal. The force level was increased in steps from 1N to 4N, keeping the frequency constant at 5 Hz using TIRA shaker. The sensor response to applied force/pressure is shown in Figure 7.128 (a). The sensitivity measured with this configuration is calculated as 630 mV/N (6.92 mV/Pa) without any extra amplification. The sensitivity was calculated from the linear fit of the plot using Origin. It shows good linear behaviour to force and without any noticeable hysteresis, as shown in Figure 7.128(b).

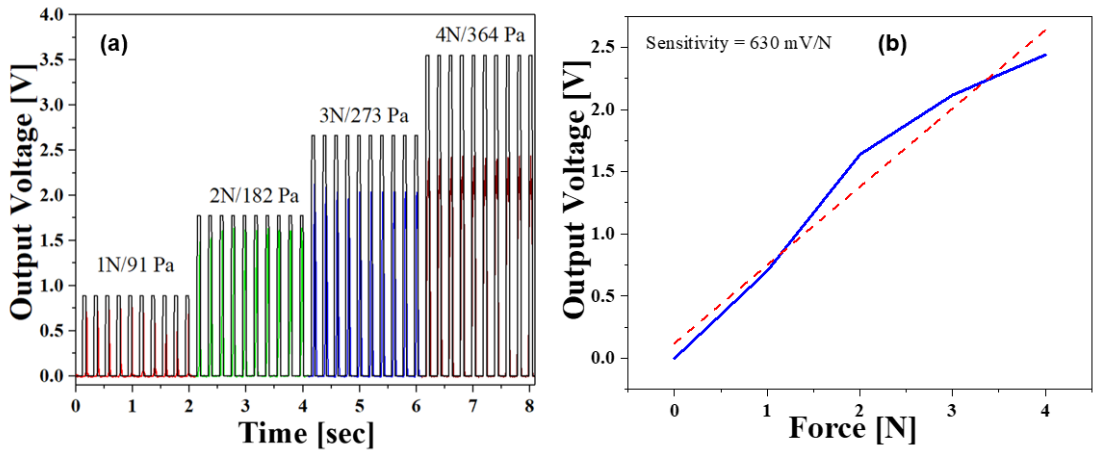


Figure 7.128: (a) Variation of output voltage at different force levels, and (b) Calibration curves of P(VDF-TrFE)/BT nanocomposite for change in force. [188]

The same configuration was used to sense the change in temperature. For this, the sensing structure was heated gradually with increasing temperature steps (2^{o}C-9^{o}C) using a hotplate, without any mechanical force and the output was recorded as explained previously and shown in Figure 7.128(a) . This kind of stimulus is similar to the common stimulus pattern which occurs when a region of one's skin get exposed to a radiant source of heat, causing a linear temperature ramp. Due to pyroelectric component of composite, since it was in as-mixed condition, without any poling, it showed the sensitivity towards temperature. The sensitivity, which was calculated using linear fit of the plot shown in Figure 7.128 (b) is 19.3 mV/^{o}C, and also shows linear behaviour.

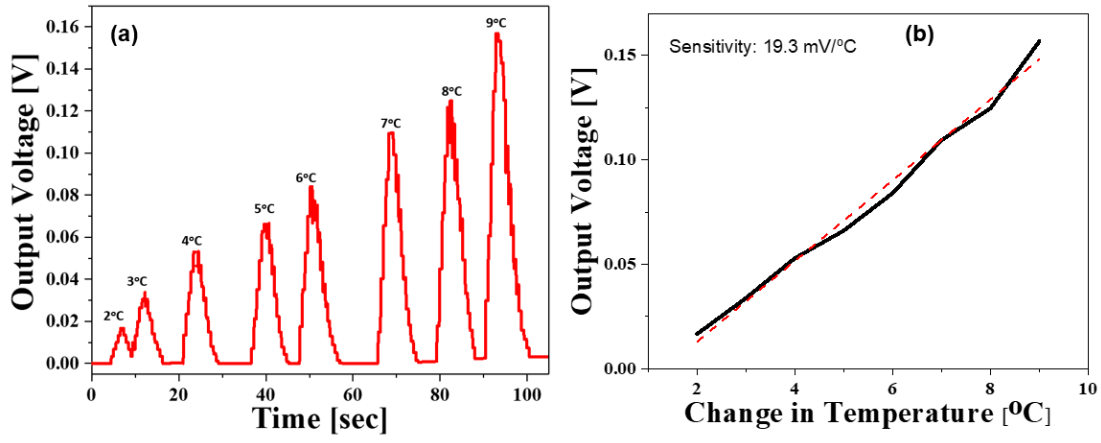


Figure 7.129: (a) Output voltage of sensor with temperature increment, and (b) Calibration curves of P(VDF-TrFE)/BT nanocomposite for change in temperature. [188]

To characterise the sensor when force and temperature act together, the sensing structure

was poled in a way that pyroelectric coefficient of filler and matrix cancel out each other, as explained in Chapter 4. It was then placed in a closed chamber. The ambient temperature of the enclosure was increased from 25°C to 50°C in steps of 5°C using a heater. Once the temperature gets stabilised, a constant force of 1N with frequency 5Hz was applied.

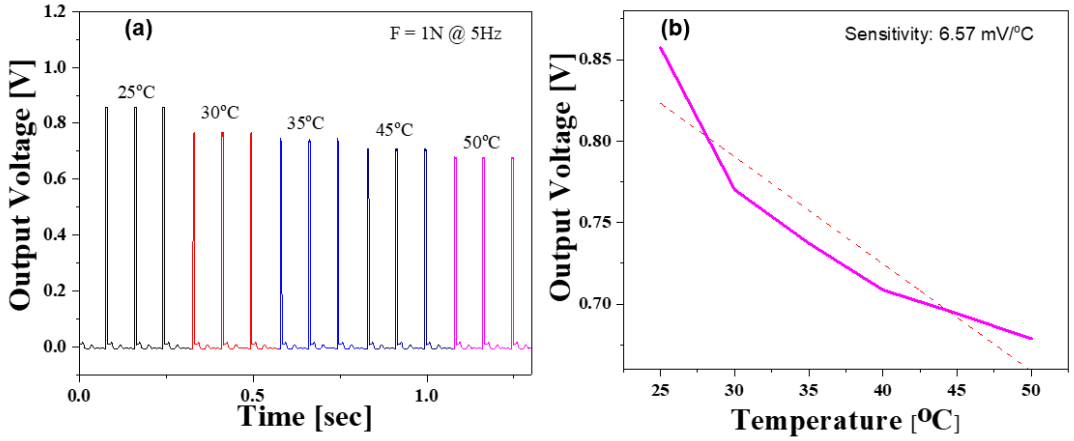


Figure 7.130: (a) Output voltage of sensor at constant force amplitude of 1N and frequency 5 Hz at different temperatures. (b) Calibration curve of sensor when both force and temperature vary simultaneously. [188]

The temperature of the sensing layer was recorded from the area which was not covered with a protection layer, using an infrared thermometer. As can be observed from Figure 7.130 (a), the output voltage slightly decreases as the temperature increase, and the decrement was calculated from the liner fit of calibration curve shown in from Figure 7.130 (b) and is around 6.57 mV/°C. This observation shows that charges originating due to pyroelectric effect is in opposite direction to that of due to piezoelectric effect. Comparing the temperature related shift with the force/pressure sensitivity of 630 mV/N (6.92 mV/Pa), the temperature effect was negligible while using the presented device as force sensors.

The performance of presented touch sensing devices in compared in Table 7.18 with previously reported works based on similar configuration i.e. piezoelectric touch sensing part tightly coupled with FET. In particular, the output is compared with Piezoelectric Oxide Semiconductor Field Effect Transistor (POSFET) and P(VDF-TrFE) coupled with organic FET (OFET). The comparison in Table III clearly shows that the P(VDF-TrFE)-BT nanocomposite-based sensors has better performance.

Table 7.18: Comparison of P(VDF-TrFE)/BT sensor with other P(VDF-TrFE) based sensors

	Force Sensitivity (mV/N)	Temp. Sensitivity (mV/ºC)	Ref.
POSFET	102	12.5	[238]
EG-OFET	65	3.8	[165]
This work	630	19.30	--

7.4. Piezoelectric AlN thin film

7.4.1. d_{33} measurement

For the d_{33} measurement, aluminium was deposited on the backside of the carrier substrate and the bottom electrode of AlN capacitor was electrically shorted to the backside metal. A d_{33} meter which operates on Berlincourt method [239], was used to measure the piezoelectric coefficient value of 5.9 pC/N (image during the measurement shown in Figure 7.131(c). The high value of d_{33} shows the success of the process optimisation carried out in Chapter 5, for the deposition of piezoelectric AlN.

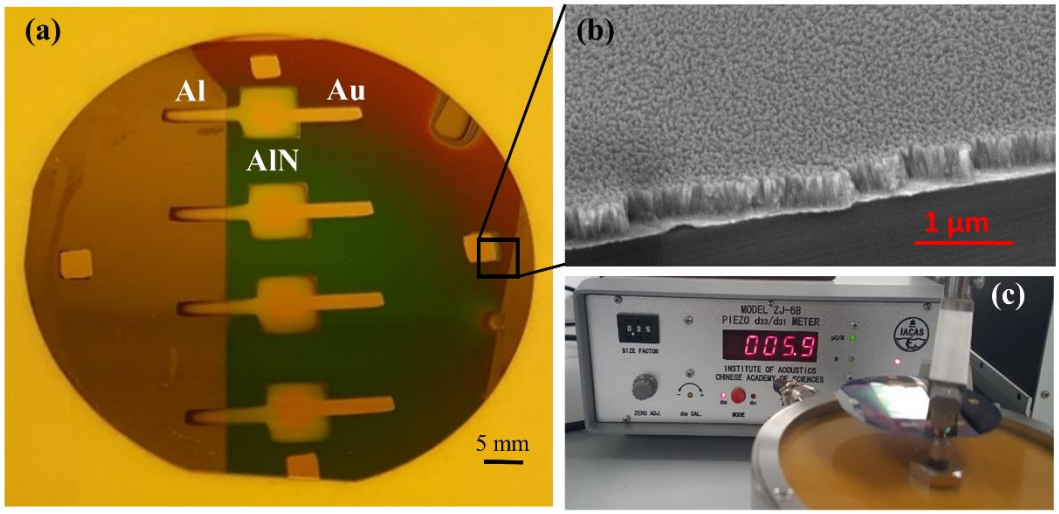


Figure 7.131:(a) Picture of fabricated AlN piezocapacitor on silicon wafer (b) SEM picture of cross-section showing columnar growth (c) Piezoelectric coefficient, d33 (= 5.9 pC/N) of AlN measured using d33 meter.

7.4.2. C-V measurement

The capacitance vs. voltage and capacitance vs. frequency measurements were performed using a summit 12k autoprober and shown in Figure 7.132(a-b), establishes the capacitive nature of the fabricated structure. As it is MIM structure, the capacitance value remained constant during the voltage range. Also, since the permittivity decreases with increase in frequency, the capacitance value decreases with increase in frequency.

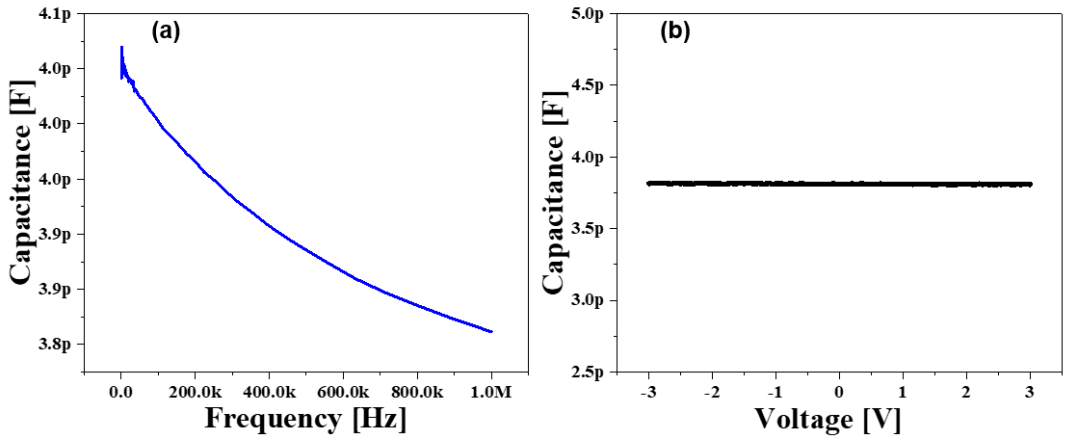


Figure 7.132: Plot of (a) capacitance vs frequency and (b) capacitance vs voltage of AlN sensor realised on silicon substrate.

7.4.2.1. Characterisation of thin silicon based AlN capacitor

The fabricated sample was etched using SF_6, as discussed in Chapter 6. After thinning, the capacitance vs voltage and capacitance vs frequency measurements were performed to check the effect of thinning on capacitive behaviour.

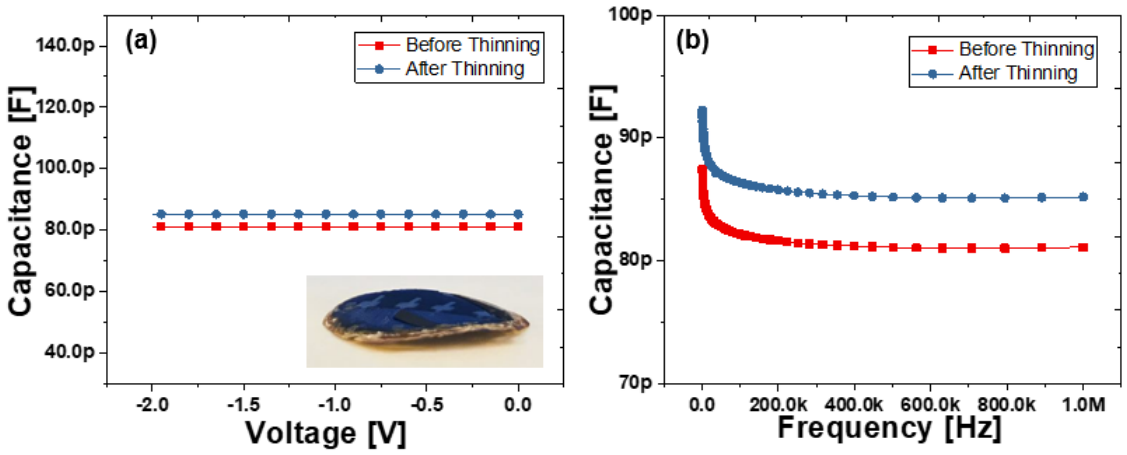


Figure 7.133: Plot of (a) of (a) capacitance vs voltage and inset shows the AlN sensor after thinning the silicon by dry etching technique (b) capacitance vs frequency of AlN capacitor before and after the thinning of silicon.

As can be seen from Figure 7.133, the capacitance value increases from 7.11 pF to 7.52 pF after thinning, which was about 5% change due to mechanical anomaly and under acceptable deviation limits. Although, ideally a MIM capacitor value is independent of the substrate thickness, however, the parasitic capacitance arising due to metal pads with the substrate comes in series with the MIM capacitance. Thus the substrate thickness starts playing a role when the thickness decreases, as with decreasing substrate thickness, the parasitic capacitance associated

between metal pads and substrate increases. There are some mechanical anomalies associated too, making this dependence a case for further study.

7.4.3. Sensor characterisation

The experimental setup for mechanical stimulation consisted of a rigid frame for mounting the sensor and an electro-mechanical shaker (TIRA model). The sensing structure was placed over the frame and covered with a thin layer of PDMS for protection during the contact event. The shaker was controlled via a closed loop feedback program meto ensure the precise value of force. The tip of the shaker was mounted with a piezoelectric force transducer (ICP Force sensor). The force level was applied in tapping mode, increasing from 1N to 3N with frequency 2 Hz. The output voltage was recorded using a digital multimeter and the LabView programme. The sensor response to applied force is shown in Figure 7.134(a) and a linear sensitivity calculated from the calibration curve shown in Figure 7.134(b) was around 5.70 mV/N. Extending this study to the domain of flexible electronics, where flexible tactile sensors are required for applications such as electronic skin [38, 134, 240], AlN capacitors were also fabricated on polyimide substrate. The polyimide foil was cleaned ultrasonically and AlN was sputtered directly over it. The top and bottom electrodes were deposited, and the final structure is shown in inset of Figure 7.135(b). The characterisation was performed as explained before and the response is shown in Figure 7.135(a), and the sensitivity of 7.36 mV/N was achieved. Due to the inherent flexibility of the substrate, the fabricated sensor could be attached on the curvilinear surface of an object such as a prosthetic hand.

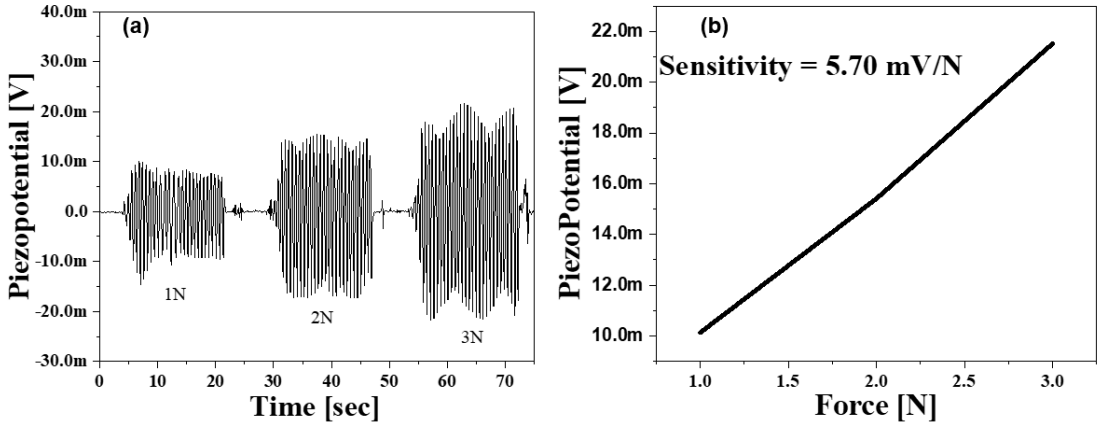


Figure 7.134: (a) Response of AlN based sensor on silicon to increasing magnitude of force (b) Calibration curve for sensor

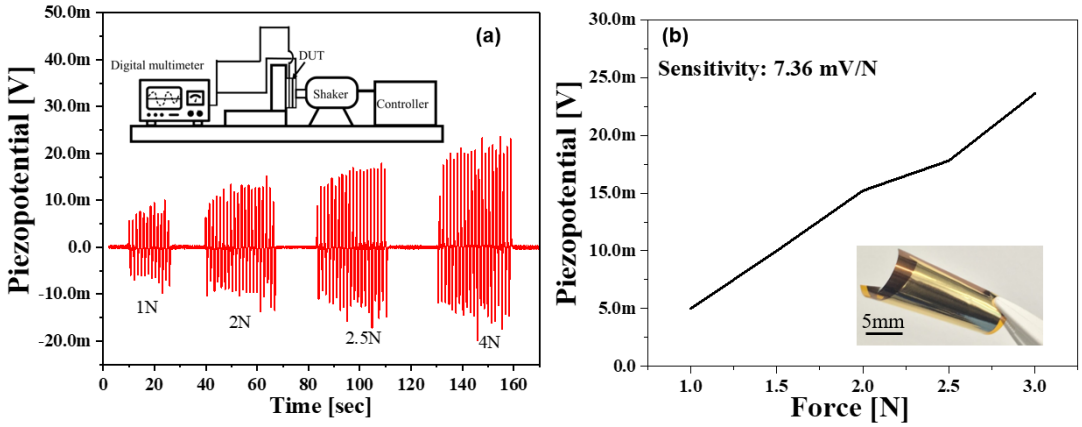


Figure 7.135: (a) Response of AlN based sensor on polyimide to increasing magnitude of force and inset illustrates the schematic of characterisation setup. (b) Calibration curve for sensor and inset shows the picture of sensing structure fabricated on flexible polyimide foil.

7.4.4. Characterisation in extended gate configuration

To validate the sensor performance in extended gate configuration, the bottom electrode of sensor was connected to the gate of MOSFET and the top electrode is connected to its drain. This configuration is chosen for the reasons already discussed above in Section 7.3.3. The device was mounted over a fixture having a motor-controlled setup to apply force of varying magnitude, as shown in Figure 7.136(b). A load cell underneath measures the applied force, while the transistor output voltage gives a measure of sensor output. The MOSFET was biased at 1V and the drain terminal was grounded together with the top electrode of the AlN capacitor, as shown in Figure 7.136(a). The drain current was recorded in response to tapping force. Figure 7.137(a) shows the periodic nature of normalised

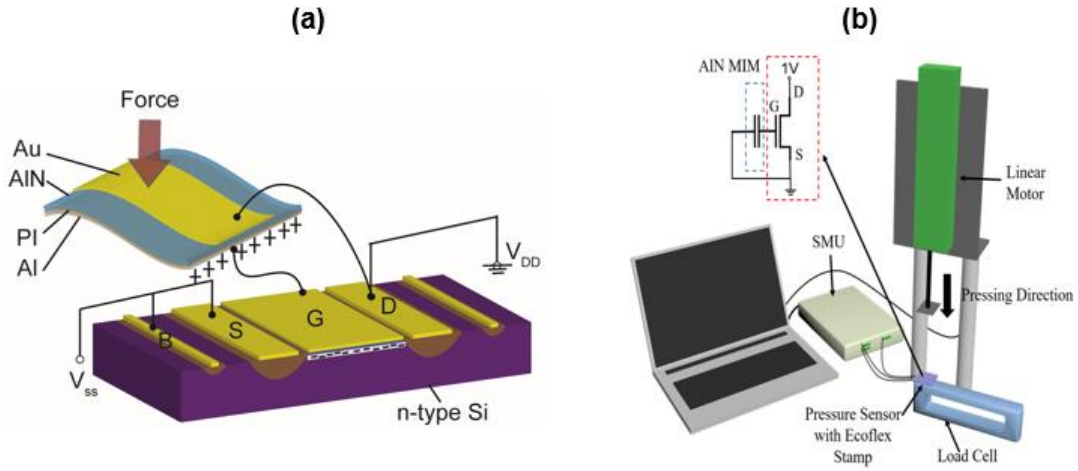


Figure 7.136: Illustration of the (a) piezoelectric AlN capacitor connected to MOSFET in extended gate configuration. (b) experimental setup for pressure sensor characterisation with biasing conditions.

change in current on application of 3.5N and Figure 7.137(b) shows the calibration curve and

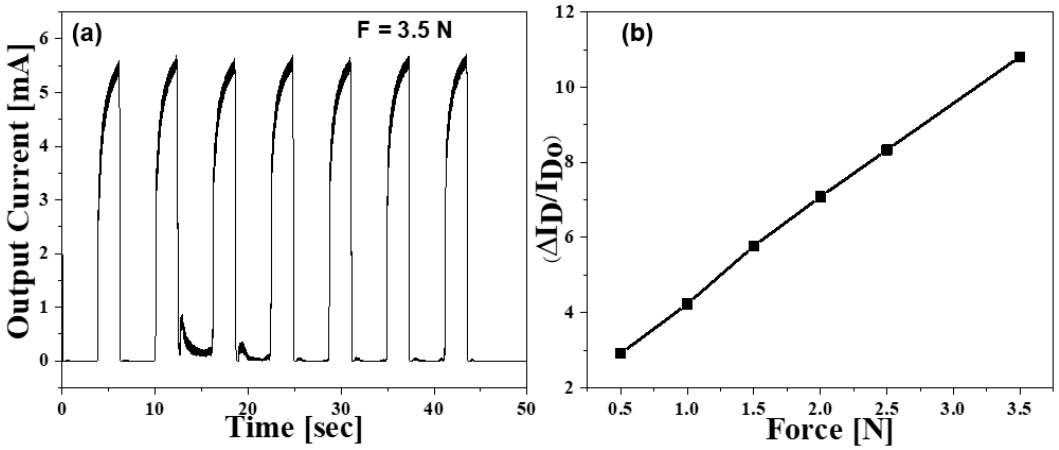


Figure 7.137: (a) Sensor response to periodic force of magnitude 3.5N. (b) Calibration curve of AlN based tactile sensor. [241]

sensitivity which is defined as normalised change in drain current per unit applied force, is calculated to be 2.65 N^{-1}.

7.5. Characterisation of devices after wafer scale thinning and transfer

7.5.1. Optical characterisation of thin chip

As discussed in Chapter 2, as the thickness decreases, silicon starts to become optically transparent, starting in the red region and progressing towards the blue region. This shift in transparency is due to different absorption coefficient of silicon at different wavelengths. When a light falls on silicon, the percentage of reflected and absorbed portion of light can be estimated using Fresnel equation and Beer-Lambert law. In order to use these equations, the thickness of silicon has to be more than 10 μm, which is more than the wavelength of light spectrum, which is 300 nm to 1100 nm, where interference effects are negligible. The optical properties of silicon are characterised using UV-Visible-NIR spectroscopy with Shimadzu UV2600 spectrophotometer having a 60 mm integrating sphere. The net spectral transmittance and spectral reflectance of four samples with thicknesses 15 μm, 30 μm, 75 μm and 300 μm are plotted in Figure 7.138 (a) and Figure 7.138 (c) respectively. It can be observed that the absorption coefficient of silicon becomes lower towards the infrared and the near-infrared region, which results in an increase in both transmittance and reflectance

towards the red end of the spectrum. The calculated spectral transmittance and spectral reflectance are also plotted and as such during calculation only spectral reflectance was considered. That is why there was a difference observed between measured and calculated spectrum, especially in the near- infrared region. Out of the light passing through the silicon, the portion belonging to blue and green region get completely absorbed within 10 μm. As the thickness goes below 10 μm, the absorptance decreases and touches the minimum at ~1150 nm wavelength, which is also the bandgap of silicon. Since photons passing through the silicon gets reflected both at the front and rear sides, the red and infrared photons gets scattered more in the initial phase of etching, due to the highly-textured and rough surface. However, as the etching progresses and thickness decreases, the surface becomes smoother and shallow etch pits appear. Due to the smoother surface, the higher portion of red and IR photons are transmitted. The normalised net transmittance of the four samples are tabulated in Table 7.19.

Table 7.19: Normalised net transmittance at different thicknesses of silicon.

Thickness	Normalised net transmittance
15 μm	7.694%,
30 μm	7.380%,
75 μm	6.09%
300 μm	0.927%

In the visible range spectrum, no transmittance was observed for sample with thickness 300 μm and 75 μm, and when thickness decreases to 15 μm, the transmittance increases to 0.170%. To experimentally verify this, the samples were illuminated from front and back to capture reflection and transmission respectively, and the picture was captured from the front side. In Figure 7.138 (b2-b6), the top yellow strip in the case of the front illumination and the black strip in the case of the back illumination relates to the metal of capacitor fabricated over the silicon. It can be well observed that for the sample with thickness 300 μm, complete opaqueness was detected and when thickness reaches sub 20 μm, it started becoming transparent in the red region. Although the sample looked similar in the front illumination, red light transmitting through etch pits and edges can be clearly observed. Figure 7.138 (d) shows the thinned MOSCAP wafer under rear illumination by a white LED light, in which red light transmission can be observed.

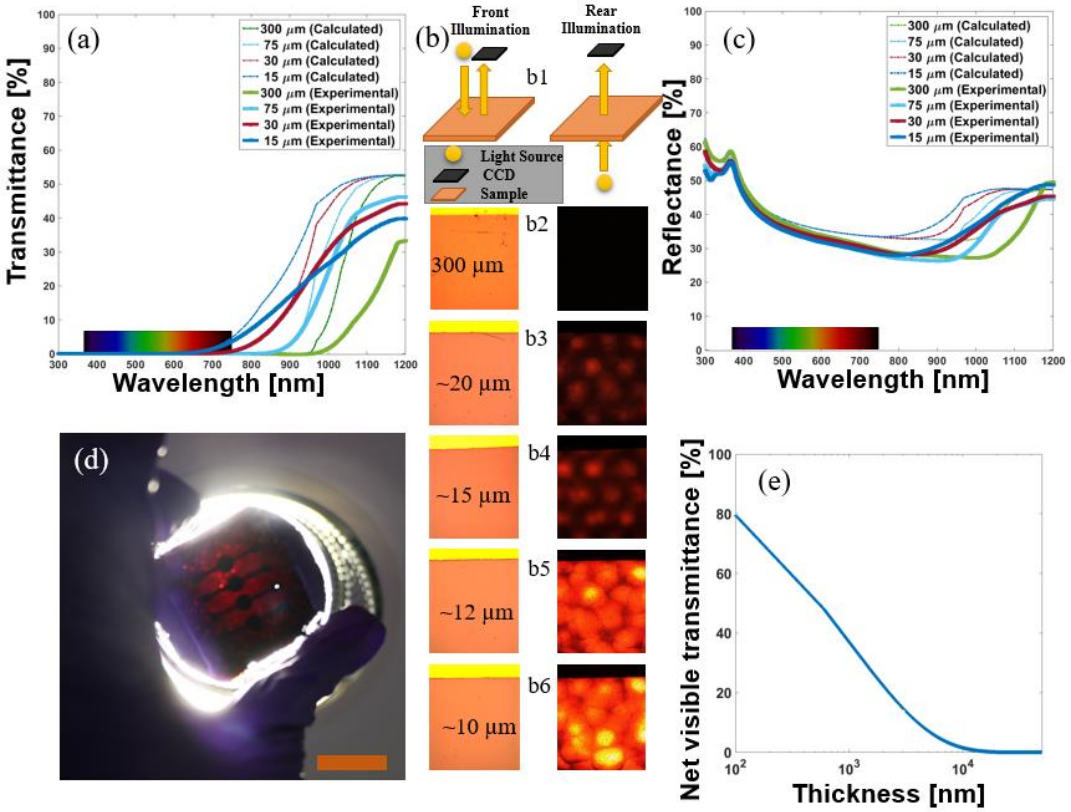


Figure 7.138: UV–vis–NIR (a) transmittance and (c) reflectance spectrum compared to the calculated spectrum for various thicknesses of Si chips (b) (b1) schematic and (b2–b6) optical microscopic images of samples of different thickness imaged from front-side under front-side illumination and rear-side illumination (d) Thin silicon MOS capacitor structure transmitting red light under a white LED light illumination (e) Net visible transmittance versus thickness of wafer. [38] ***Courtesy: William Taube for conducting this optical test.***

Figure 7.138 (e) shows normalised weighted transmittance in the visible region for various thicknesses and 80% weighted visible transmittance can be achieved for around 100 nm thick silicon membrane. These optical studies could be beneficial in deciding etch stop time during a wet etch process. Since etch time is very crucial and hard to control, due to variation with the passage of time, if the sample is not taken out at proper time, the etchant may damage the devices on the front side. To solve this issue, a red-light source could be placed at one end of the etching setup and the transmittance can then be observed from the other side. When the transmittance crosses the limit, which corresponds to a particular thickness, etching can be stopped. This will assist in large- scale manufacturing of ultrathin chips.

7.5.2. Effect of bending on MOSCAP

The MOSCAP were fabricated and thinned, as discussed in Chapter 6. After thinning, the effect of bending on MOSCAP were characterised using a Nordson Dage 3-point bending

set-up as shown in inset of Figure 7.139 . Before the test, thin sample was laminated in between PVC sheets using the hot lamination technique. The sample was placed facing down in order that the moving bar did not touched the capacitor directly, due to which when the sample was loaded with force, it experienced tensile strain. The connections were taken out using copper tape and various loading force and the corresponding vertical displacement of sample was measured. The vertical displacement was used to calculate the bending radius of the sample, using sample width as arc length and displacement as chord of a circle, as illustrated in Figure 7.140(a). The C-V measurements were carried out during loading using a semiconductor parameter analyser at 1MHz frequency. The voltage sweep was carried out with DC voltage from -4V to 4V superimposed with AC voltage of 50 mV. During the bending, it was observed that capacitance increases with increase in loading force and up to 5% increase in capacitance was observed at bending radius of 42 mm as can be observed from Figure 7.139.

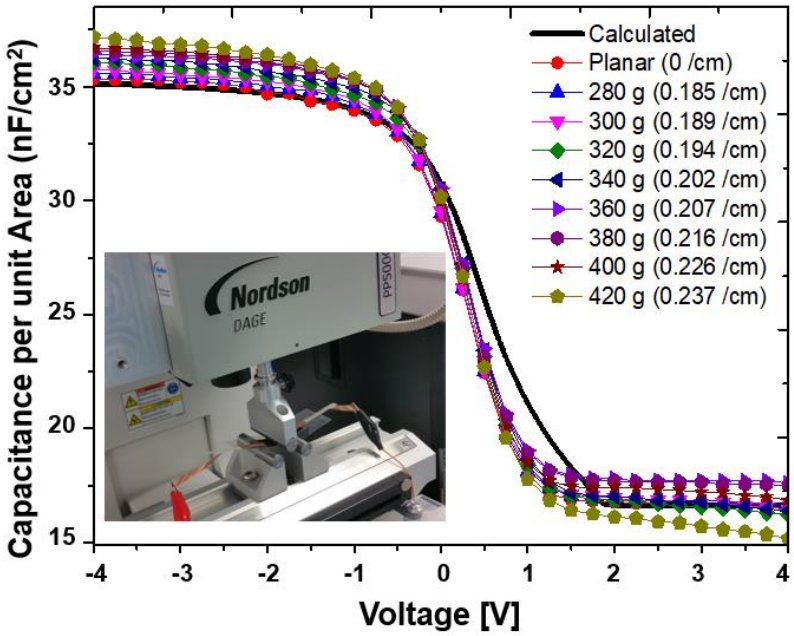


Figure 7.139: C–V characteristics under ideal and various bending conditions. Insets shows the Device under test (DUT) using three-point bending setup. [38]

The experimental data was compared with ideal C-V characteristics calculated using MATLAB code. The ideal conditions did not include the presence of various oxide charges such as fixed oxide charges, mobile ionic charges, interface trapped charges, leading to a difference between calculated and measured values. However, the code was used to extract these tapped and interface charge density and plotted as a function of bending radius. It can

be noted from Figure 7.140(b) that interface trap density increases and threshold voltage, Vth decreases as the bending curvature increases. Moreover, with the increase in tensile strain, the accumulation capacitance increases, but effective oxide charge remained almost constant, as depicted in Figure 7.140(c). The flatband voltage and flatband capacitance also change with increase in bending curvature and have been plotted in Figure 7.140(d). Various device and interface parameters extracted by comparing the measured and ideal C-V characteristics are summarised in Table 7.20.

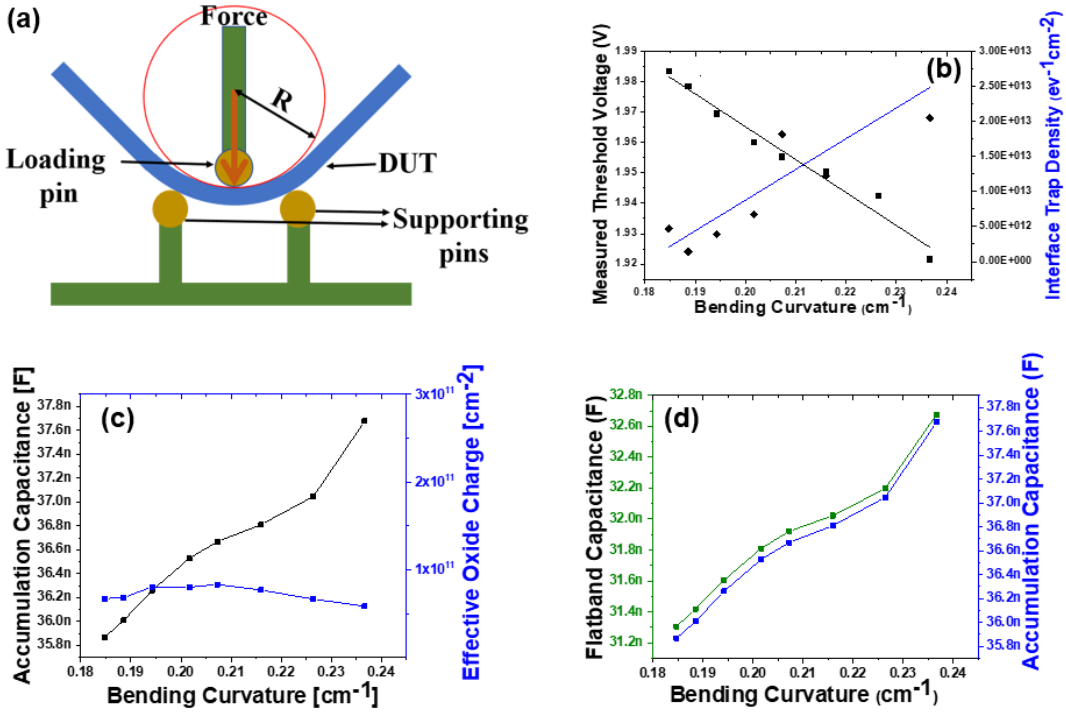


Figure 7.140: (a) Illustration of bending condition used for estimating bending curvature (b) Bending curvature versus threshold voltage and interface trap density (b) Bending curvature versus accumulation capacitance and effective oxide charge (d) Bending curvature versus flatband capacitance and accumulation capacitance. [38]

Due to these bending related anomalies, the operating point of any device or circuit can change, which places the requirement of having the compensation circuit to be included as an important part of design.

Table 7.20: MOSCAP parameters in planar condition

Parameters	Value
Threshold voltage	1.99319 V
Effective oxide charge	6.88×10^{10} /cm^2
Interface trap density	7.65×10^{11} /cm^2-eV
Depletion width	327 nm

Flatband capacitance	31.1 nF
Flatband voltage	-0.189 V
Accumulation capacitance	35.6 nF/cm^2

7.5.3. Bending Effect on MOSFET

Following the thinning and transfer of the thin wafer, as described in Chapter 6, the MOSFET devices were tested under tensile and compressive bending conditions. The laminated thinned wafer was placed on a 3D printed convex and concave jig. On a convex jig of radius 40 mm, the devices come under tensile stress whereas on a concave jig, they come under compressive stress. The strain generated due to the bending affects the band structure of silicon by splitting the six degenerate conduction bands into two groups, Δ_4 and Δ_2. For tensile strain, the energy of Δ_4 gets lowered down with respect to Δ_2 and vice-versa for compressive strain. For the valence bands, tensile strain increases the energy of all three-valence band and compressive strain increases their energy level. These changes in the energy levels lead to change in carrier mobility, since it is obtained using E-k model either at the bottom of the conduction band or at the top of the valence band. So, due to energy lowering in case of tensile strain, the carrier mobility increases and for compressive strain, mobility decreases. As discussed in Chapter 6, the analytical equations relating the stress with the mobility and drain current are:

$$\mu_{(\text{stress})} = \mu_o\left(1 \pm \Pi_\mu \sigma_\mu\right) \tag{7.54}$$

$$I_{D(\text{stress})} = I_{D_0}\left(1 \pm \Pi_{I_D} \sigma_{I_D}\right) \tag{7.55}$$

where μ_0, I_{D0}, μ_{stress} and $I_{Dstress}$ are mobility and drain current under normal and stressed conditions respectively. The piezo-resistive coefficients Π_μ and Π_{ID} account for sensitivity towards stress and σ is magnitude of stress.

In the case of n-MOSFET, carrier mobility and the oxide capacitance increase with the increase in tensile strain. Since the drain current is directly proportional to mobility and capacitance value, it increases with the increase in drain current, and opposite behaviour is observed for compressive strain. This behaviour can be clearly observed in Figure 7.141 from output and transfer characteristics of MOSFET during tensile and compressive bending

The threshold voltage was then extracted using the linear extrapolation method from the transfer characteristic data under planar, tensile and compressive conditions. Similarly,

transconductance (g_m) and channel conductance (g_d) of the MOSFET was calculated by numerical differentiating the drain current with reference to the gate-source and drain-source voltage respectively.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} | V_{DS} = Constant \tag{7.56}$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} | V_{GS} = Constant \tag{7.57}$$

Using these extracted parameters, the effective surface mobility μ_{eff} was calculated by the equation:

$$\mu_{eff} = \frac{L}{W} \frac{g_d}{C_{ox}(V_{GS} - V_{th})} \tag{7.58}$$

where W and L are the MOSFET channel width and length, g_d is the channel conductance, C_{ox} is the oxide capacitance and V_{th} is the threshold voltage.

The saturation mobility (μ_{sat}) was obtained from output characteristics and in planar condition, the mobility was calculated to be 341 cm^2/V-s. Similarly, mobility for tensile and compressive conditions was calculated to be 355 cm^2/V-s and 320 cm^2/V-s respectively. Using Equation (3), the semi-empirically (in relation to planar saturation mobility) estimated value of motilities under tensile (convex) and compressive (concave) bending are 353 cm^2/V-s and 327 cm^2/V-s. These calculated values closely matches with the experimental data and deviate only by 0.5% and 2.5% for tensile and compressive case respectively.

Since current is directly proportional to capacitance and mobility, and both change during bending, therefore for small change, the normalised change in current can be written as the sum equivalent of change in mobility and change in capacitance:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta C_{ox}}{C_{ox}} + \frac{\Delta \mu}{\mu} \tag{7.59}$$

At R = 40 mm, the estimated change in mobility and capacitance were around 3.82% and 5% respectively, which led to about 7.5% change in the current. This also matched with experimental measurements, which show a maximum of ~10% change in the current.

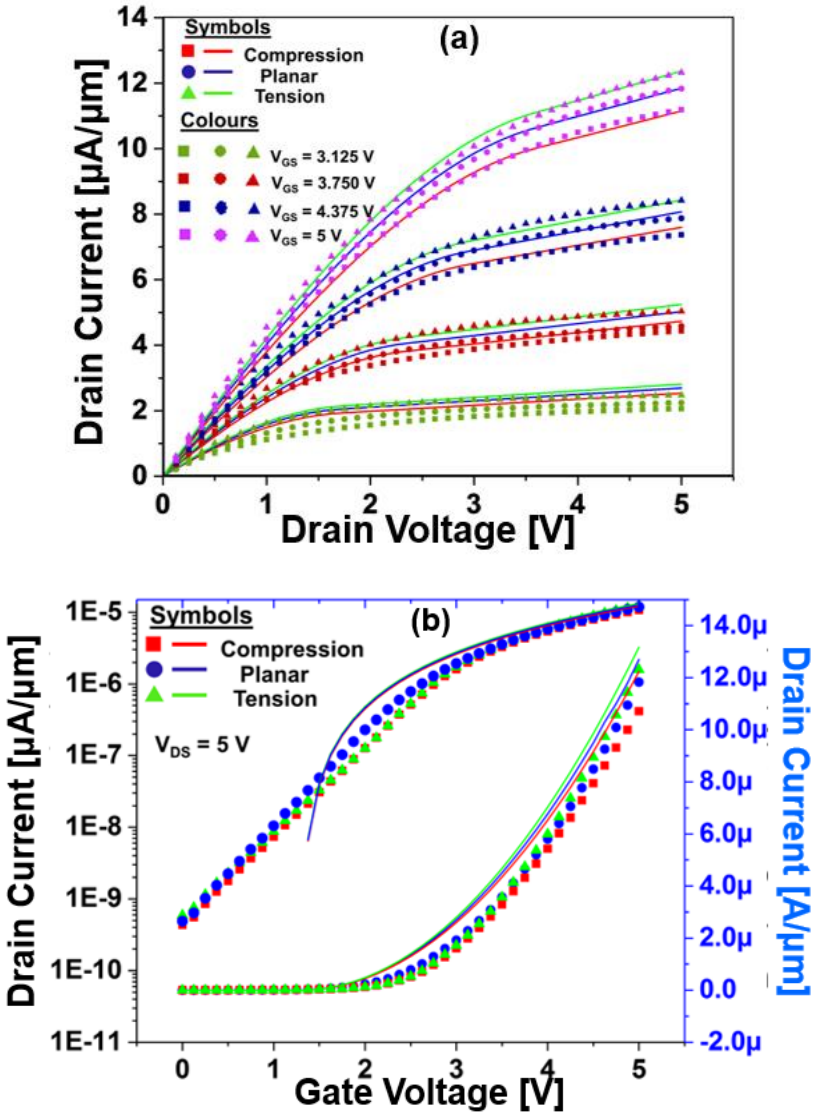


Figure 7.141: (a) Output characteristics of MOSFET [experimental (dots) versus simulation (line)] under planar (blue line), compressive (red line) and tensile (green line) bending conditions. e) Transfer characteristics of MOSFET [experimental (dots) versus simulation (line)] under planar (blue line), compressive (red line), and tensile (green line). [38] *Courtesy: These measurements were done with assistance of William Taube.*

The saturation current (at V_{DS}=5V and V_{GS}=5V) were 12.3, 11.8, 10.7 µA/µm for tensile, planar and compressive conditions respectively.

The on-to-off current ratios for the three cases were 4.32, 4.38 and 4.39 decades. The sub-threshold swing (SS) was estimated from the logarithmic transfer characteristics in sub-threshold regime by numerical differentiation and is given by the equation:

$$SS = \frac{1}{\partial \log(I_D) / \partial V_{GS}} \tag{7.60}$$

The sub-threshold slope for tensile, planar and compressive conditions were 1.06, 0.98 and 1.04 V/decade. Various parameters extracted from the electrical characterisation of the MOSFET under planar and bending conditions are summarised in Table 7.21.

Table 7.21: Various parameters related to MOSFET characteristics

Parameters	Tensile Strain	Planar	Compressive Strain
Bending Radius of Curvature R_C	40 mm (Convex)	-	40 mm (Concave)
Effective Mobility (Experimental) μ_{eff}	384 cm^2/V-s	350 cm^2/V-s	333 cm^2/V-s
Saturation Mobility (Experimental) μ_{sat}	355 cm^2/V-s	341 cm^2/V-s	320 cm^2/V-s
Saturation Mobility (Semi-empirical) $\mu_{sat-Cal}$	353 cm^2/V-s	341 cm^2/V-s (Ref.)	327 cm^2/V-s
Threshold voltage (V_{th})	1.305 V	1.425 V	1.55 V
Channel-length Modulation Factor (λ)	0.094	0.115	0.122
Saturation Current (I_{D-sat}) at V_{DS}=5 and V_{GS}=5V	12.3 µA/µm	11.8 µA/µm	10.7 µA/µm
Drain Conductance (g_d)	4.94 µS/µm	4.58 µS/µm	4.06 µS/µm
I_{ON}/I_{OFF}	4.32 decades (2.08×10^4)	4.38 decades (2.42×10^4)	4.39 decades (2.46×10^4)
SS	1.06 V/decade	0.98 V/decade	1.04 V/decade
Transconductance (g_m)	6.67 µS/µm	6.62 µS/µm	6.21 µS/µm

7.5.4. Effect of cyclic bending on device performance

In order to evaluate the effect of cyclic bending on device performance, thinned MOSFET underwent 100 bending cycles. The devices were characterised in planar condition after every 10 cycles of compressive and tensile bending over 3D printed zig of R_C 80 mm. Furthermore, gate leakage current density (J_G) characteristics were also obtained during the initial planar condition and after the 50^{th} and 100^{th} cycle, to check if there was any deterioration in gate dielectric due to bending. The plots of MOSFET leakage current

densities and transfer characteristics are shown in Figure 7.142(a) and Figure 7.142(b) respectively, and it can be observed that statistically the device performance in terms of transfer characteristics remains unaffected, even after 100 bending and negligible variation in the leakage current density when the gate voltage is positive.

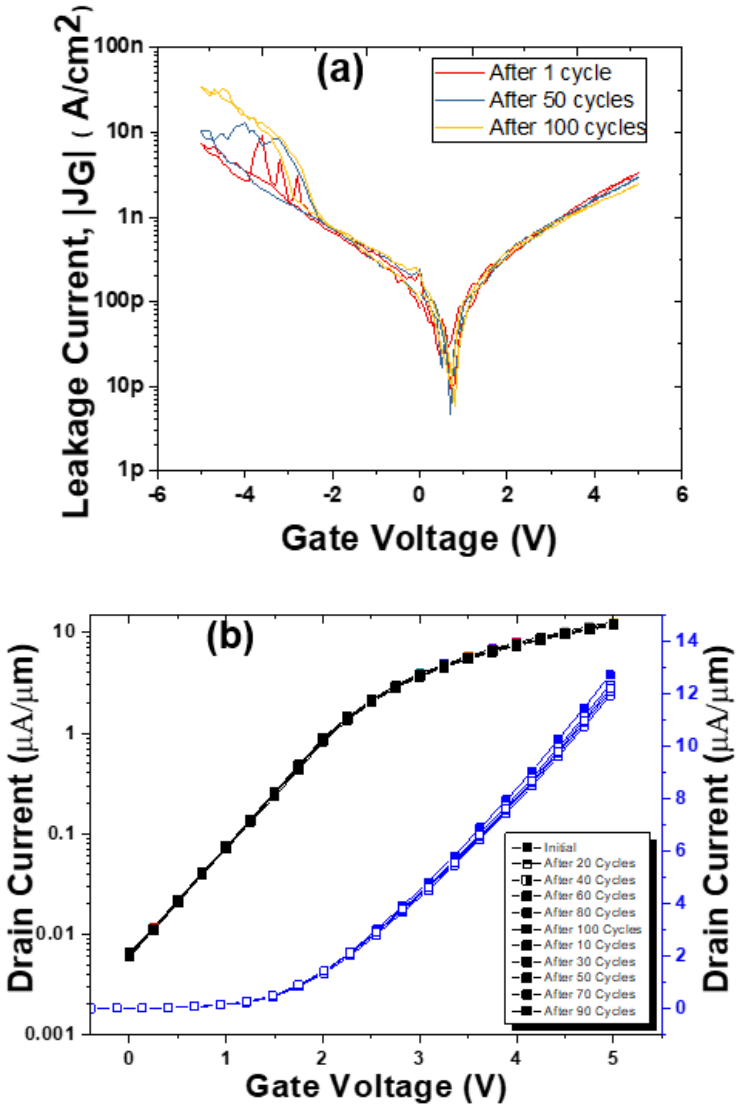


Figure 7.142: (a) Leakage current density of MOSFET at initial condition, mid, and end of cyclic bending test. (b) Transfer characteristic of MOSFET under cyclic bending test. [38]
Courtesy: These measurements were done with assistance of William Taube

7.6. Effect of bending on inverter transfer characteristic (VTC)

The ultra-thin CMOS inverter realised in Chapter 6, was fixed on 3D printed jig of bending radius 40 mm and 20 mm in both way i.e. concave and concave, to put the chip in tensile and compressive bending condition. The voltage was swept on the input terminal of inverter from 0 to 1.8V and voltage signal was recorded at the output terminal. The VTC i.e. output

voltage vs input voltage is the figure of merit for the static behaviour of inverter. The device parameters including noise tolerance, gain, and operating logic-levels can be obtained from the inverter's VTC and are summarised in Table 7.22.

As can be observed from Figure 7.143, midpoint voltage (V_M) of inverter decreases from compressive and increases for tensile bending. A similar trend was observed for input high (V_{IH}) and input low (V_{IL}) voltage levels, and the behaviour is similar to the discussion provided in Chapter 7.

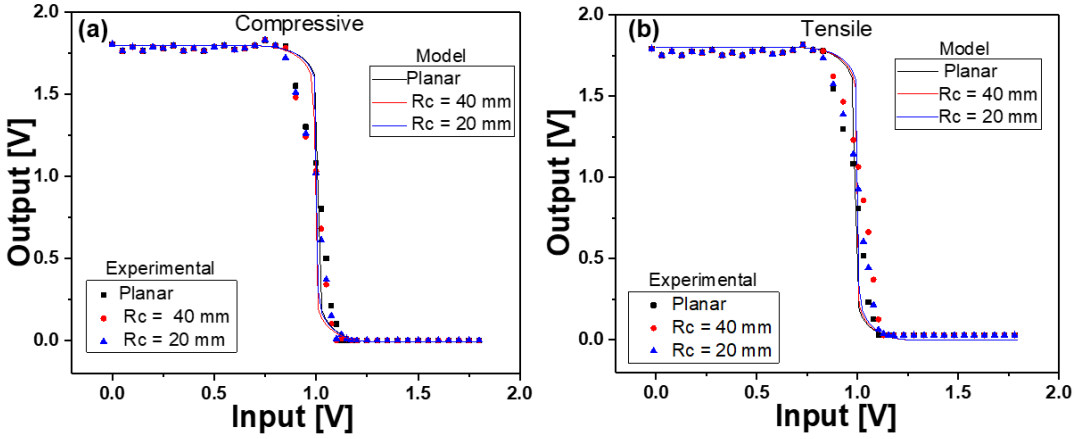


Figure 7.143: Experimental and simulation data inverter VTC under (a) Planar (black)/Compression 40mm (red)/Compression 20mm (blue), and (b) Planar (black)/Tension 40mm (red)/Tension 20mm (blue). [242] *Courtesy: Anastasios Vilouras implemented the Verilog-A code in Cadence.*

Table 7.22: Values of midpoint voltage, gain and operating points of inverter under planar and bent conditions.

Inverter	V_M (V)	A_V	V_{IH} (V)	V_{IL} (V)
Planar	1	6.09	1.148	0.852
Tension 40mm	1.03	5.92	1.182	0.878
Tension 20mm	1.04	5.97	1.191	0.889
Compression 40 mm	0.99	6.01	1.139	0.840
Compression 20mm	0.98	5.98	1.131	0.829

7.7. Conclusion

This chapter presents the electrical, electro-mechanical and optical characterisation of the devices and sensing structures fabricated during the course of this doctoral work and discussed in Chapter 2 – Chapter 5. The electrical characteristics of fabricated MOSFETs demonstrated the successful conduct of the designed process. The current characteristics were used to extract the associated device parameters. The MOSCAP, MOSFET and inverter were tested under

planar and bend conditions to study the shift in electrical response, and close matching with the models developed in Chapter 6 was achieved. Moreover, the optical transmission studies carried out during wafer-scale thinning and transfer can lead to an important application of using red-light source as etch monitor during wet etching of silicon.

In addition, the range of characterisations were performed on the transducer materials namely, P(VDF-TrFE), composite of P(VDF-TrFE)/BT and AlN, individually and in extended gate configuration. The nanocomposite of P(VDF-TrFE) and BT was able to suppress the sensitivity to temperature, which was an issue for the POSFET, and at the same time, it also enhanced the sensitivity to pressure. Whereas, the extensive process optimisation carried out for obtaining (002) oriented AlN film, resulted in piezoelectric film, which does not require any poling, thus resolving another potential challenge associated with P(VDF-TrFE).

Chapter 8. Conclusion and Future Perspective

This chapter concludes all the work contained within this thesis in Section 8.1. Opportunities for types of future work, which can be done and the candidate's perspective on how the field of high performance flexible electronics, may benefit from this thesis, is presented in Section 8.2.

8.1. Conclusion

Flexible electronics is envisaged to be one of the next generation technologies with wide range of applications from 3D-ICs to advanced bio-electronic technologies. Currently, there are many electronic products already in the market which are flexible and bendable but almost all of them are based on low mobility, low resolution and less durable organic semiconductors, therefore, are not suitable for the areas of application which demands for high-speed, reliability and durability. On the contrary, most of the high-speed and compact application, ICs based on silicon has been used from long time, however, the rigid nature of these ICs pose a limitation for their usage in the emerging area of flexible electronics. Nevertheless, the thinner any material becomes, the flexible it gets, silicon being no exception. Moreover, the market dominance of matured mono-crystalline silicon based technology makes it a natural choice for integration in the emerging area of flexible electronics. However, the challenges associated with UTC in the area of fabrication, packaging and performance modelling has motivated the researchers to push the limit and introduce new processes and techniques, so that the goal of flexible electronics can be fulfilled without compromising the performance. Until now, researchers have explored the way to realise silicon nanostructures like nanowires, nano-rods, and serpentine shape nanomebranes to investigate its potential in the realm of flexible electronics. However, the nanostructures need sophisticated processing steps and devices realised using these suffer from immature technology and low yield percentage of devices.

The presented work demonstrated the potential of transforming traditional high performance silicon based devices into flexible form, opening its applicability in the domain of flexible electronics, especially for tactile sensors as highlighted in Chapter 2. The necessary elements for building a sensor have been separately demonstrated and their characteristics has been assessed. The major novel contributions of this thesis can be summarised as:

1) The thinning processes developed during this work, resulted in devices with substrate thickness ranging between 20 μm – 30 μm. With the major attention on wet etching, some work in the direction of dry etching is also presented. The techniques related to

thin silicon dicing and handling resulted in yield improvement. Moreover, the two-step transfer process carried out to transfer the thin sample on flexible substrate, and further encapsulation in PVC sheets resulted in ability to conform over the surfaces having bending radius up to 20 mm.

2) The analytical model of POSFET was developed using standard semiconductor and ferroelectric equations. The model showed close matching with the experimental results and then further implemented in circuit design tool to facilitate the complex design.
3) The semi-analytical set of equations were developed for modelling the effect of bending on the device parameters, behaviour and circuit response. The model was further validated using electrical measurement of devices in bent condition and close matching was achieved. In tensile condition, the drain current increased by 4.2%, whereas in compressive condition, it decreased by 9%. Similar trend was observed in the capacitance value of MOSCAPs where the accumulation capacitance increased by 5% under during bending. In the case of inverter, slight shift in the mid –point voltage was also observed in bent state.
4) In the direction of alternate piezoelectric material for POSFET, the development of PVDF-TrFE/BT nanocomposite was carried out. The uniform dispersion of filler in polymer was achieved using probe sonicator and the poling was performed in such a way that pyroelectric contribution cancels out each other. This process step resulted in decreased sensitivity towards it was varied during force application. Moreover, the addition of BT nanoparticles enhanced the β-phase formation in the PVDF-TrFE and better dielectric properties of the composite. The sensing structure was fabricated over polyimide foil and characterised in extended-gate configuration with MOSFET. The experimental results demonstrated the enhanced sensitivity towards force (690 mV/N) and supressed sensitivity towards temperature (6.57 mV/^{o}C).
5) The RF sputtering process optimisation for AlN deposition was carried out with three variable parameters namely, gas ratio, chamber pressure and RF power. The (002) crystalline orientation of the film, which is required for piezoelectric response was determined by XRD analysis and an optimised recipe was developed, which gave the piezoelectric coefficient value of 5.9 pC/N. The sensing structure was fabricated over silicon and polyimide as carrier substrate, and the characterised individually and in extended gate configuration. While individually, the sensitivity of 5.70 mV/N and 7.36 mV/N were obtained for silicon and polyimide based sensor respectively, in extended

gate configuration, sensitivity (normalised change in drain current per unit force) of 2.65 N^{-1} was achieved.

8.2. Future Work and Perspectives

With the development of thinning and packaging techniques for silicon, UTC can now be employed for high-performance flexible electronics more reliably than before. However, as this technology is still in development stage, there are quite a few challenges which require specific attention. The future work will aim to resolve these challenges, some of which are summarised below:

1) Thin chips are usually encapsulated between two layers to keep it in neutral plane. Therefore, getting the electrical connection out to the top layer of package is still a pressing issue, which will need some investigation. As a preliminary step, laser cutting was used to remove the plastic from the top of contact pad, and more work is needed to done in this area.
2) In this work, wire bonding has been used for connecting thin chip to the PCB. However, as discussed in Chapter 2, wire bonding can damage the chip. For this reason, inkjet printing will be investigated for this purpose. This kind of connection will also address the issue of edge hardening which comes when wire bonds are protected using epoxy glue.
3) More work is required in the area of thin wafer dicing as it has direct impact on chip strength. The dicing before etching is a viable option, which has been explored in this thesis, however, there is always a probability of etchant led damage to the front side. The laser dicing approach which is also used, will be further optimised to achieve more fine dicing.
4) The analytical model developed for studying the effect of bending on device performance took into account the band-splitting led change in the carrier mobility. However, this also produce a slight change in the threshold voltage as observed during bending test on the MOS capacitor. That's why the model will be further tuned to include the effect of bending on the threshold voltage of the MOSFET. Also, study of the stress using micro-Raman spectroscopy could be exploited to calculate the strain generated in the thin silicon.

In the case of tactile sensing, following are the areas which need more attention:

5) The further work will aim to characterise the sensor with the piezoelectric material directly deposited over the gate area in the bending condition to study the effect of bending on the sensor response. In this direction, some work has already been presented showcasing the sputtering of AlN on the resist-patterned gate area of MOSFET and its lift-off, and extra work will be focussed in this direction.
6) The sputtering process optimisation carried out to deposit AlN gave highly c-axis oriented film. Nevertheless, the spatial variation of the film quality is something which need to be further studied.
7) In the fabrication of P(VDF-TrFE)/BT composite, the DC poling was performed which suppressed the pyroelectric effects of the constituents. Further work will study the effect of poling condition variation, so that complete decoupling of piezoelectric and pyroelectric properties can be achieved.

To summarise, with the range of research work reported in this thesis, a strong case for the role of ultra-thin silicon chips for the high performance flexible electronics has been established. The major application areas of flexible electronics such as e-skin, display, and wearables, will be the biggest beneficiary from this technology as they can meet the requirement of high speed processing using thin chips without restricting the overall flexibility of system. The thinning experiments can be performed at batch-level are thus can be scaled up to industrial level. Although, with more focus on flexible electronics, developed technologies is not only limited to that but can be extended to other application areas such as 3D ICs.

Appendix 1: Market Analysis

The key drivers behind growth of any new product or technology is its demand in market which either opens new application areas or brings easiness in the existing technology. In the case of thin wafers, these drivers are growth in the consumer electronics market, and reduction in size of devices which is complemented with growth in the semiconductor industry. For example, SiP (system in package), IC cards and RFID (radio frequency identification) tags commonly used in digital and mobile devices employ 30–50 μm thick product die. The thinning of wafers to enhance performance is also in strong demand in power devices used for power conversion, such as IGBTs (insulated gate bipolar transistors) used in solar power generation and hybrid vehicles, which have attracted attention for energy conservation and global environmental protection.

According to a new market research report *"Thin Wafer Market by Wafer Size (125mm, 200mm, 300mm), Process (Temporary Bonding & Debonding, Carrier-less/Taiko Process), Application (MEMS, CMOS Image Sensor, Memory, RF Devices, LED, Interposer, Logic), and Region - Global Trend and Forecast to 2022"*, the thin wafer market was valued at USD 6.76 billion in 2015 and is estimated to reach USD 9.17 billion by 2022, at a compound annual growth rate of 3.7% between 2016 and 2022. Moreover, the annual shipment of thin wafer which was a little over 15 million unit in 2015, will exceed 30 million units by 2022.

Wafers of size 150 mm and larger are widely used in the manufacturing plants, as the large size allows companies to fabricate a large number of devices in a single batch. Therefore, this preferred size is expected to show the highest growth and thus it is essential to develop techniques for realising thin wafers at a scalable level. In terms of application area, it is the thin wafer based LED market which is expected to benefit most, since a thin wafer offers high conductivity and electrical benefits for LED chips. This will be followed by microelectromechanical system (MEMS) and 3D IC technology as bulk micromachining and wafer thinning are integral parts of these technologies. The largest share of this developing market will be accounted for by countries in the Asia Pacific Region such as China, Taiwan and South Korea, due to increasing industrialisation and urbanisation in these regions along

with increasing semiconductor manufacturing capacity. European countries are expected to lead the research frontier in the thin wafer field, followed by North American countries. Although the thin wafer market is still at an early stage, there are many companies and research institutions which could become major players by 2022, some of which are provided in Table A.1 and their qualitative market share is shown in Figure A.1 as a pie chart.

Table A.1: List of major companies involved in thin wafer market and their area of expertise/product.

Company	Location	Product
Siltronic Inc	Germany	Wafer
Shin-Etsu	Japan	Chemical
Sun Edision	USA	Wafer
SUSS MicroTec AG	Germany	Equipment
3M	USA	Accessories
Nissan Chemical Corporation	Japan	Chemical
Synova SA	Switzerland	Equipment
EV Group	USA	Equipment
UlVac Gmbh	Germany	Material, Components
Applied Materials	USA	Equipment, Software
TSMC	Taiwan	Wafer
IMEC	Belgium	R&D
Infineon Technologies	Germany	Sensors and Systems
Brewer Science Inc	USA	Coating Materials
Beijing Sinopoly Technology Co. Ltd.	China	Wafer

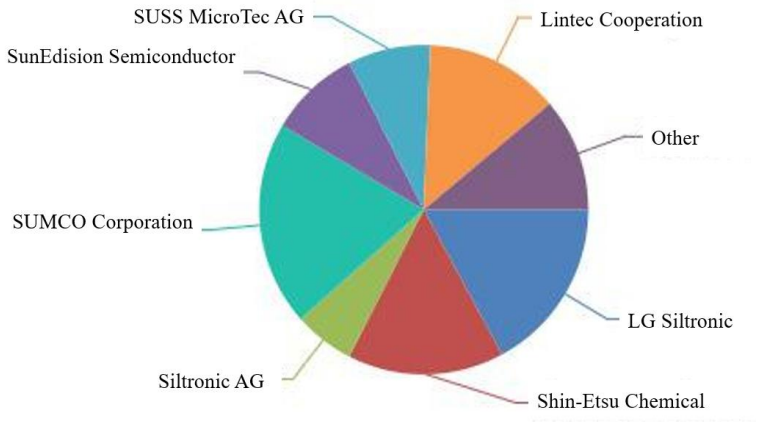


Figure A.1: Market shares of major companies in Thin Wafer industry. [243]

Appendix 2: Design Rule Check list

The design rules were modified to suit the available equipment capability. This is based n IRST CF10 process run at Fondazione Bruno Kessler and has been prepared with the help of Dr. Andrea Adami and Dr. Christian Collini. The DRC checks implemented in the design software are summarised in Table A.2.

Table A.2: DRC rules followed for designing the mask

Rule	Rule Distance
PWell minimum width	8 µm
PWell minimum spacing	26 µm
PWell to N Plus minimum distance	20 µm
PWell to P Plus minimum distance	20 µm
N Plus on PWell minimum overlap	8 µm
P Plus on PWell minimum overlap	8 µm
Diffusion minimum width	4 µm
Minimum diffusion spacing	16 µm
Minimum gate length	8 µm
Poly on gate minimum overhang	4 µm
Minimum gate spacing	6 µm
Gate to P diffusion minimum distance	10 µm
Gate to N diffusion minimum distance	10 µm
Minimum polysilicon width	6 µm
Minimum polysilicon spacing	6 µm
Polysilicon to diffusion minimum distance	6 µm
Minimum contact width	4 µm
Minimum contact spacing	4 µm
Diff contact on P Plus overlap	4 µm
Diff contact on N Plus overlap	4 µm
Diff contact to gate edge minimum distance	8 µm
Poly contact on Poly minimum overlap	4 µm
Metal1 minimum width	6 µm

Minimum metal-1 spacing	6 µm
Minimum metal-1 spacing to diffusion outside	6 µm
Metal1 on contact minimum overlap	4 µm
Glass minimum spacing	120 µm
Gold minimum width	20 µm
Gold minimum spacing	20 µm
Gold to metal-1 minimum distance	10 µm

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