INTEGRATION OF PLANAR GUNN DIODES AND HEMTS FOR HIGH-POWER MMIC OSCILLATORS

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By

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To the memory of my beloved father

Abstract

This work has as main objective the integration of planar Gunn diodes and high electron mobility transistors (HEMTs) on the same chip for the realisation of high-power oscillators in the millimeter-wave regime. By integrating the two devices, we can reinforce the high frequency oscillations generated by the diode using a transistor-based amplifier.

The integration of the planar Gunn diode and the pseudomorphic HEMT was initially attempted on a combined gallium arsenide (GaAs) wafer. In this approach, the active layers of the two devices were separated by a thick buffer layer. A second technique was examined afterwards where both devices were fabricated on the same wafer that included AlGaAs/InGaAs/GaAs heterostructures optimised for the fabrication of pHEMTs. The second approach demonstrated the successful implementation of both devices on the same substrate. Planar Gunn diodes with 1.3 μm anode-to-cathode separation (L_{ac}) presented oscillations up to 87.6 GHz with a maximum power equal to -40 dBm. A new technique was developed for the fabrication of 70 nm long T-gates, improving the gain and the high frequency performance of the transistor. The pHEMT presented cut-off frequency (f_T) equal to 90 GHz and 200 GHz maximum frequency of oscillation (f_{max}).

The same side-by-side approach was applied afterwards for the implementation of both devices on an indium phosphide (InP) HEMT wafer for the first time. Planar Gunn diodes with L_{ac} equal to 1 μm generated oscillations up to 204 GHz with -7.1 dBm maximum power. The developed 70 nm T-gate technology was applied for the fabrication of HEMTs with f_T equal to 220 GHz and f_{max} equal to 330 GHz.

In the end of this work, the two devices were combined in the same monolithic microwave integrated circuit (MMIC), where the diode was connected to the transistor based amplifier. The amplifier demonstrated a very promising performance with 10 dB of stable gain at 43 GHz. However, imperfections of the material caused large variations at the current density of the devices. As a consequence, no signals were detected at the output of the complete MMIC oscillators.

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Associated Publications

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- V. Papageorgiou, A. Khalid, C. Li, and D. R. S. Cumming, "Cofabrication of Planar Gunn Diode and HEMT on InP substrate," *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2779-2784, 2014.

- V. Papageorgiou, A. Khalid, C. Li, and D. R. S. Cumming, "The Development of Planar Gunn Diodes for the realisation of MMIC oscillators," *Proceeding of the 1st Annual Active and Passive RF Devices Seminar*, Glasgow, UK, Oct. 2013.

- V. Papageorgiou, A. Khalid, M. J. Steer, C. Li, and D. R. S. Cumming, "Monolithic Fabrication of a Planar Gunn Diode and a pHEMT side-by-side," *Proc.43rd European Solid-State Device Research Conference,* pp. 111-114, Bucharest, Romania, Sep. 2013.

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- V. Papageorgiou, A. Khalid, C. Li, and D. R. S. Cumming, "Simulation and fabrication of InGaAs Planar Gunn Diode on InP Substrate," *Proceedings of the 25th International Conference on Indium Phosphide and Related Materials*, pp. 1-2, Kobe, Japan, May 2013.

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1. Introduction

The first Gunn diode oscillators were demonstrated in 1963 by J. B. Gunn, on gallium arsenide (GaAs) and indium phosphide (InP) substrates [1]. Significant development of the Gunn diode technology was conducted in the subsequent years, making Gunn oscillators widely used for millimeter-wave (mm-wave, 30 - 300 GHz) applications. Currently, there is a growing interest for the mm-wave and terahertz (THz, 300 GHz - 30 THz) range of the electromagnetic spectrum. Numerous mm-wave and THz applications have been presented, such as security systems [2], anti-collision radars [3, 4], telecommunication systems [5] and astronomy instrumentation [6]. Modern Gunn diodes are required to present high output power and high frequency oscillations in the upper mm-wave (above 100 GHz) and the THz regime, in order to meet the requirements for the above applications.

The oscillation frequency of Gunn diodes is strongly dependent on the separation between the anode and the cathode electrodes. Conventional Gunn oscillators are implemented in vertical configuration where the channel layer is sandwiched between the two contact layers. The active layer structure is typically separated from the substrate and mounted in a rectangular waveguide. Vertical devices have presented oscillations up to 77 GHz and 150 GHz for GaAs and InP based systems, respectively [3, 7]. Advanced vertical Gunn diodes compatible with coplanar waveguides (CPWs) were recently demonstrated [8], presenting reduced complexity and implementation cost. However, the maximum oscillation frequency of the vertical devices is limited by the epitaxial thickness of the channel layer.

The frequency performance of the Gunn diode was significantly improved after the introduction of the first planar Gunn diodes operating above 100 GHz by Khalid et al [9]. The anode and the cathode of the planar devices are placed on the top of the structure, similarly to the electrodes of field effect transistors (FETs). Thus, the oscillation frequency can be easily determined by the adjustment of the anode-to-cathode separation (L_{ac}) through the lithographic design, and oscillations at various frequencies can be generated from the same chip. State of the art planar Gunn diodes based on InP reached the THz regime, were devices with L_{ac} as small as 0.6 μm presented oscillations up to 307.5 GHz [10].

Despite the high frequency performance, planar Gunn diodes present oscillations with limited generated power. The maximum output power reported was equal to -4 dBm for operation in fundamental mode at 109 GHz, resulted from devices with 7 channel layers [11]. However, the number of the channels that contributed to current conduction was equal to 5. Therefore, there is limited number of channel layers that can be included in the layer structure and additional layers cannot further improve the power performance.

The main objective of this project is the integration of planar Gunn diodes and high electron mobility transistors (HEMTs) on the same substrate. HEMTs are well known amplifying elements with low noise characteristics that recently demonstrated power gain for frequencies above 1 THz [12]. The Gunn oscillator can benefit from a transistor based amplifier for the reinforcement of the signal power, while the low phase noise characteristics of the diode can be retained. The successful implementation of the two devices on the same chip can also lead to the implementation of more sophisticated monolithic microwave integrated circuits (MMICs).

In this work, the integration of the two devices was investigated by following two different approaches. In the first technique the individual layers of the two devices were combined in a single wafer, separated by a thick buffer layer. In the second technique, the implementation of both devices was examined using the same layer structure that was optimised for the realisation of HEMTs. Following the successful realisation of both devices on the same substrate, complete MMIC oscillators were designed and fabricated. The signals generated by planar Gunn diodes were delivered to HEMT amplifiers for the enhancement of the power characteristics.

Following this brief introduction, Chapter 2 presents the basic physical principles and the properties of the materials used in this work, such as GaAs, InP and the $In_xGa_{1-x}As$ ternaries. The operation of HEMTs and Gunn diodes is also described in the same chapter, based on the formation of semiconductor/semiconductor and metal/semiconductor interfaces. Chapter 3 focuses on the passive elements used in modern MMICs, such as CPWs, capacitors and inductors. In the end of the chapter, the general methodology for the design of transmission line matching networks is described. Chapter 4 presents the fabrication and characterisation techniques used in this project and Chapter 5 conducts an overview of the technology development related to Gunn diodes, HEMTs and MMIC amplifiers. The first experimental

results resulted from GaAs based substrates, are presented in Chapter 6 where both the combined wafer and the single wafer approaches are described in detail. The results from the devices fabricated on InP substrates are given in Chapter 7. In the same chapter we present details of the design procedure of the HEMT amplifier and the complete MMIC oscillator. Finally, Chapter 8 gives a conclusion of this work with the discussion of the results and the proposal of future developments.

2. Physics & devices

2.1 Introduction

III-V semiconductor compounds have been the main choice for the implementation of devices for high frequency applications due to their superior electron mobility over silicon (Si). Heterojunction bipolar transistors (HBTs), metal-semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), Gunn diodes and resonant tunnelling diodes (RTDs), are some examples of devices based on III-V compounds. The above components have demonstrated operation at the frequency range between several tens of GHz and THz. GaAs and InP are the most studied materials for the fabrication of Gunn diodes while GaAs and InP based HEMTs demonstrate excellent characteristics at high frequencies.

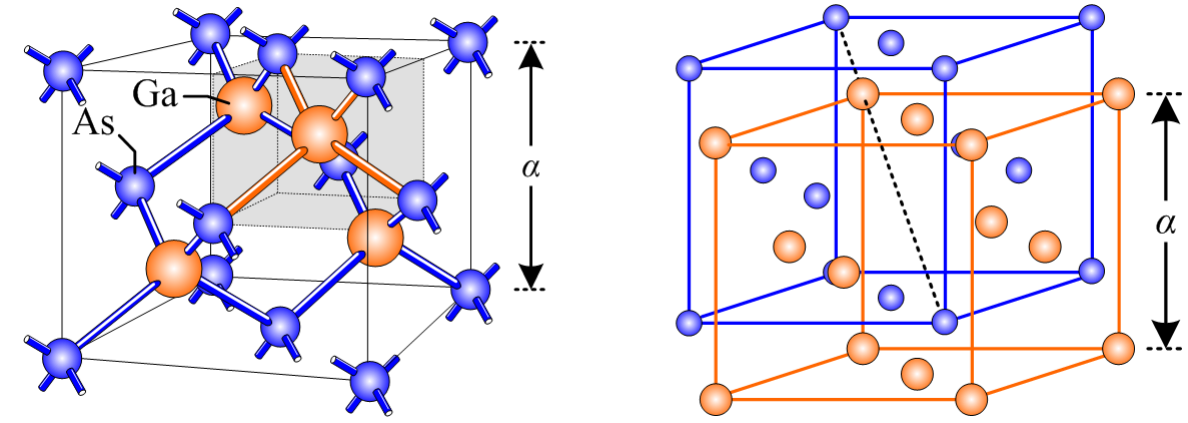
In the next sections, the structure and the basic physical properties of III-V compounds is presented, with the main focus on GaAs and InP. The interfaces between semiconductors with different band gaps, known as heterojunctions, and metal - semiconductor interfaces are also described as the fundamental structures for the realisation of the active devices. The current transport properties are described afterwards. Based on the above principles, the operation of the HEMT and the Gunn diode are described in the last sections of this chapter.

2.2 Materials and properties

III-V compounds consist of one element from group III of the periodic table (i.e. gallium, indium) and one element from group IV (i.e. arsenic, phosphorus) in 1:1 stoichiometry. GaAs and InP are structured with the zinc-blende lattice which is shown in Figure 2.1(a). The zinc-blende structure is formed by two face-centred cubic (fcc) structures where the second one is shifted by one quarter of the cubic diagonal, placed along the diagonal of the first element (Figure 2.1(b)). The zinc-blende structure can also be considered as an fcc lattice, where two atoms (one of each group) are placed at each point of the lattice. The edge distance of the cubic unit cell determines the lattice constant α of the crystal.

It is important to note that some crystallographic planes in the zinc-blende lattice structure can be viewed as pure monolayers consisting of single elements placed periodically. For

example, the Ga atoms are alternated with the As atoms along the [100] and the [111] directions. On the contrary, equal Ga and As atoms form monolayers along the [110] direction. The geometric characteristics of the structure are taken into account during the epitaxial process for the growth of the compound at a specific crystallographic direction. The effect of etching is also dependent on the direction of the crystal as described later in Chapter 4.



(a) (b)

Figure 2.1 The zinc-blende lattice (a) [13] and the relative positioning of the two fcc structures (b) [14].

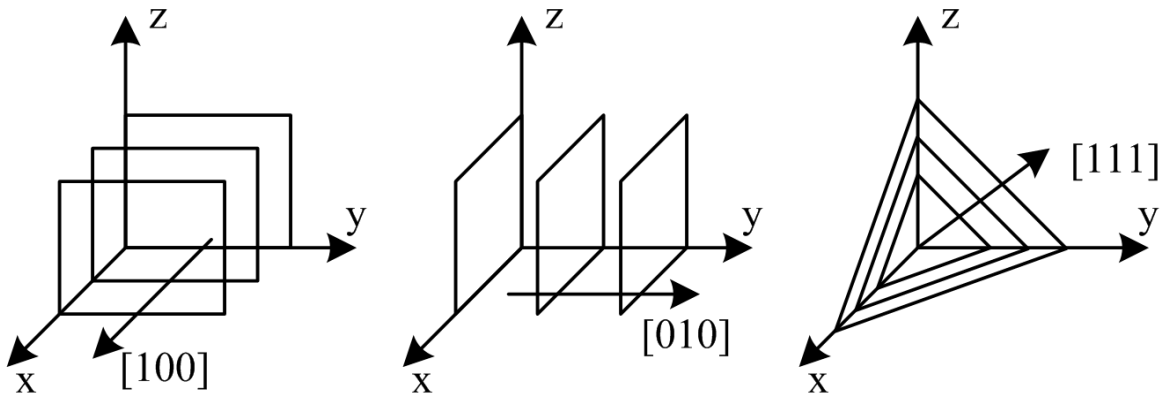


Figure 2.2 Some crystallographic directions.

The main bonding force for the formation of the III-V compound materials is provided by the so-called covalent bond. The bond results from the outer electrons of the atoms which lie in

the valence band at 0 K. As an example, each atom of Ga and As provides three and five electrons respectively (Figure 2.3(a)). These eight electrons create four covalent bonds where each one is formed by two electrons with opposite spins due to the Pauli principle. When the electrons get enough thermal energy they can be excited to the conduction band and they are no longer bond electrons and instead contribute to the intrinsic carrier concentration. Practically, the number of the conducting electrons is very small in comparison with the bond electrons [15].

Doping is the effective method to significantly increase the carrier concentration in the material. Si, which belongs to group IV of the periodic table, is commonly used as an n-type dopant to increase the amount of conducting electrons. When Si replaces an atom of Ga at the crystal lattice, four electrons are introduced to the material instead of three. The three electrons are used to form the covalent bonds and the additional electron can move in the crystal (Figure 2.3(b)).

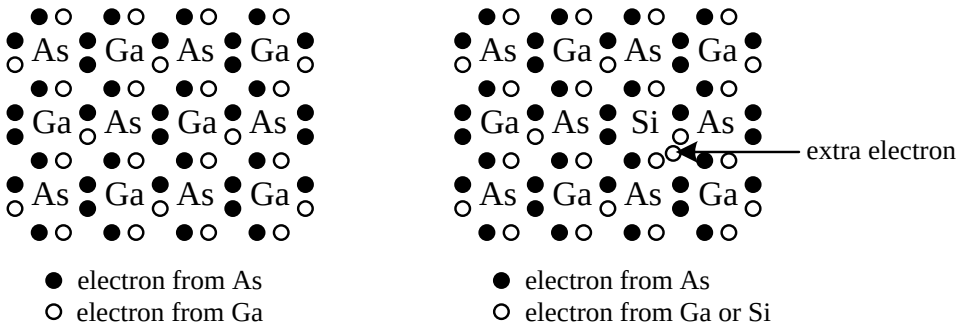


Figure 2.3 The atomic bonding in GaAs (a) and in n-type GaAs (b) [15].

As a result of doping the material, additional energy states E_d are introduced in the forbidden energy gap. The energy difference between the E_d level and the conduction band is a few kT. Thus, at room temperature the electrons introduced by the donor have sufficient energy to transfer to the conduction band. When the level of the doping concentration is comparable to the effective density of states of the semiconductor, the interactions between the closely spaced doping atoms are increased. The discrete E_d energy state turns to a continuous band which reaches and overlaps with the minimum of the conduction band. Therefore, the gap between the valence and the conduction band effectively decreases. The decrement of the band gap is proportional to the donor concentration, while the Fermi level moves closer to the minimum of the conduction band, as illustrated in Figure 2.4 [13, 15].

The Fermi level results from the Fermi-Dirac distribution function, which provides the probability that an electron occupies an energy state at specific temperature *T*. The Fermi level represents the energy level that has 50% probability to be occupied and it is usually placed in the middle of the band gap for undoped materials. As mentioned above, the Fermi level moves towards the lower edge of the conduction band, for n-type doping and the energy gap between the two bands is given by:

$$E_C - E_F = kT \ln\left(\frac{N_C}{N_D}\right) \tag{2.1}$$

were k is the Boltzmann constant, T is the absolute temperature, N_C is the effective density of states in the conduction band and N_D is the donor concentration.

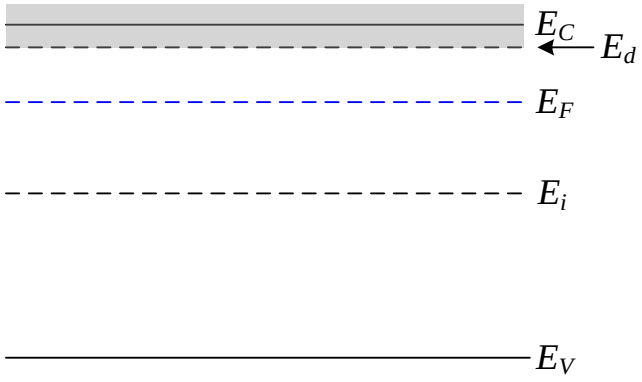


Figure 2.4 The continuous E_d energy states, the Fermi level E_F and the intrinsic Fermi level E_i [13, 15].

The general energy diagram illustrated in Figure 2.4 represents the energy levels when the wave vector **k** of the electron wave function is <000>. A more informative band diagram is presented in Figure 2.5 where the conduction and the valence bands of GaAs are plotted as a function of the wave vector **k**. It can be seen from the band diagram that GaAs is a direct band gap material, as the maximum of the valence band is aligned with the minimum of the conduction band in the <000> direction of the wave vector. Apart from the centre conduction valley, which is called the Γ valley, two more conduction valleys appear in the <111> and the <100> directions. These are the satellite L and X conduction valleys. The existence of the

satellite valleys is fundamental for the generation of the Gunn oscillations, as explained in Section 2.6 where the operation of the Gunn diode is analysed.

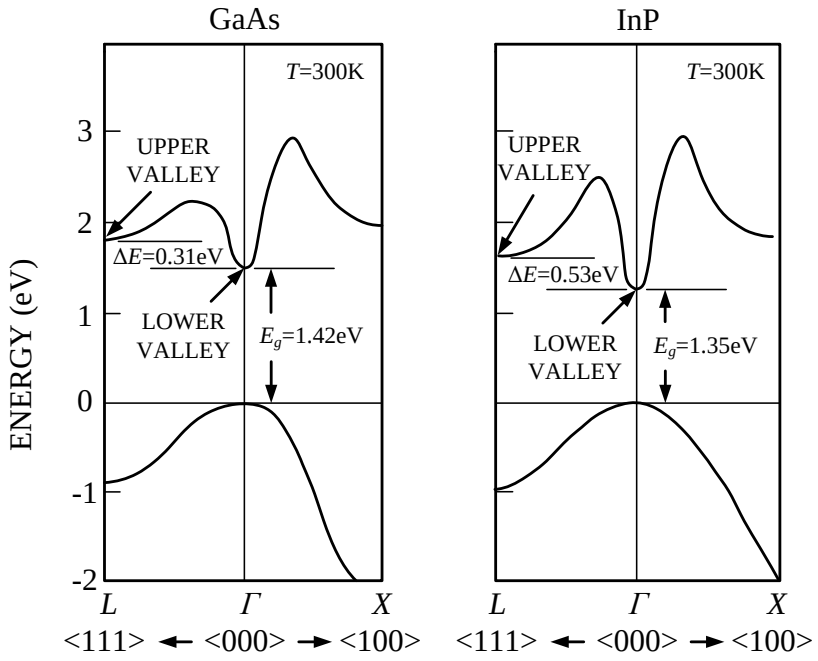


Figure 2.5 The simplified energy diagram of GaAs and InP [16].

The energy diagram of the material also provides information of the effective mass of the electrons. When electrons travel in free space they only experience the effect of the applied fields. However, electrons travelling inside crystals are affected additionally by the periodic potential caused by the atoms in the lattice. Effectively, the mass of these electrons, which is called the effective mass m_e^*, is a smaller fraction of the mass for electrons travelling in free space. Taking the assumption that the conduction valleys have a parabolic shape, the effective mass can be calculated by:

$$m_e^* = \hbar^2 \left(\frac{d^2 E}{dk^2} \right)^{-1} \tag{2.2}$$

Thus, the curvature of the conduction valley is inversely proportional to the effective mass. As an example, the L and X valleys are more flat than the Γ valley and the electrons lying there have higher effective masses than the ones in the centre conduction valley.

The energy diagrams are characteristic of the materials, depending on the periodic potentials in the crystal. Due to these potentials the effective mass of electrons in the centre conduction valley of GaAs is equal to 0.063 times the electron mass in free space [17]. As the effective mass strongly determines the mobility of the carriers, GaAs has a high electron mobility equal to approximately 9200 $cm^2/V{\cdot}s$ and for this reason it is selected for high-frequency applications. For comparison purposes, it is noted that the effective mass of electrons in Si is equal to 0.26 times the free space electron mass and the electron mobility is equal to 1450 $cm^2/V{\cdot}s$.

Table 2.1 summarises some of the basic parameters for GaAs and InP. Gallium nitride (GaN) is also presented here as the material which currently attracts lot of attention for high-power applications. The ability of GaN devices to deliver high amounts of power results from the high break down field due to the large band gap of the material. The parameter values of GaN presented in Table 2.1 correspond to the zinc-blende version of the crystal which is more suitable for high frequency applications over the wurtzite crystal structure [18]. The basic parameters of Si are also presented as a reference to a more conventional technology. All the parameters are referred to room temperature conditions.

Parameter	GaAs	InP	GaN	Si
Crystal structure	zinc-blende	zinc-blende	zinc-blende	diamond
Lattice constant (Å)	5.65	5.86	4.52	5.43
Band gap (eV)	1.42	1.34	3.2	1.12
Effective mass m_e^*/m_0 at central valley	0.063	0.079	0.13	0.26
Low field mobility ($cm^2/V{\cdot}s$)	9200	5900	1000	1450
Breakdown field (V/cm)	$\sim 4{\cdot}10^5$	$\sim 5{\cdot}10^5$	$\sim 5{\cdot}10^6$	$\sim 3{\cdot}10^5$
Effective density of states in conduction band (cm^{-3})	$4.7{\cdot}10^{17}$	$5.8{\cdot}10^{17}$	$1.2{\cdot}10^{18}$	$2.8{\cdot}10^{19}$

Table 2.1 Basic parameters of GaAs [19, 20], InP [20, 21], GaN [22, 23] and Si [17].

2.3 Current transport

When no external electric field is applied to the semiconductor, conducting electrons move randomly in every direction due to their thermal energy. The kinetic energy of the electrons is equal to their thermal energy as:

$$\frac{1}{2} m_e^* u_{th}^2 = \frac{3}{2} kT \tag{2.3}$$

where u_{th} is the average thermal velocity [24]. If the crystal structure is uniform, there is an equal possibility for the electron to move in every direction. Therefore, the total shift of the electron inside the material is zero. During the random thermal movement, electrons undergo various kinds of scattering interactions inside the crystal. The collisions mainly occur with the atoms of the crystal and the dopants. The former is known as lattice scattering and the latter as impurity scattering.

Lattice scattering is generally referred to collisions between the electrons and the lattice. At finite temperatures, the molecules of the crystal vibrate around their central positions. As the temperature of the material increases, the vibrations become more intense affecting the periodicity of the crystal potential. As a result, lattice scattering becomes more important at high temperatures where carrier mobility degrades significantly. The out-of-phase vibrations of the atoms, which are known as optical phonon modes, result in high frequency oscillations and have relatively high associated energy. The in-phase vibrations of the atoms, known as acoustic phonon modes, occur at low frequencies over a wide spectrum. Both modes of vibration increase the interaction with the electrons in the crystal, which is known as phonon scattering. Since optical phonons have relatively high energy, optical phonon scattering can cause significant changes in the momentum of the electrons. Due to the large change of momentum, electrons can scatter to different energy valleys and the phenomenon is known as inter-valley scattering [25].

Impurity scattering is caused by the ionised donors (for the n-type example) where the impurities cause perturbations to the travelling electrons, due to the additional Coulomb interactions. Consequently, the impurity scattering effect becomes dominant at high doping concentrations. The correlation between the impurity concentration and the mobility in GaAs at room temperature in depicted in Figure 2.6 [24]. For impurity concentrations up to 10^{16} cm^{-3} the material can be considered as lightly-doped and the mobility does not degrade

significantly. In this region, the mobility is limited by lattice scattering. When doping exceeds the value of 10^{18} cm^{-3} the mobility decreases by one order of magnitude. The hole mobility appears lower than the electron mobility, because of the higher effective mass of the holes. One significant difference between lattice and impurity scattering is that the latter is less effective at high temperatures. In that case, the carriers gain higher thermal velocity and they are less affected by the Coulomb forces as they travel faster through the lattice.

The mean free time τ_c shows how often a carrier is expected to scatter and is equal to the average time between the occurring collisions. The total probability of a possible collision is equal to the sum of the probabilities for collisions due to the individual scattering mechanisms. Thus:

$$\frac{1}{\tau_c} = \frac{1}{\tau_{c,lattice}} + \frac{1}{\tau_{c,impurity}} \tag{2.4}$$

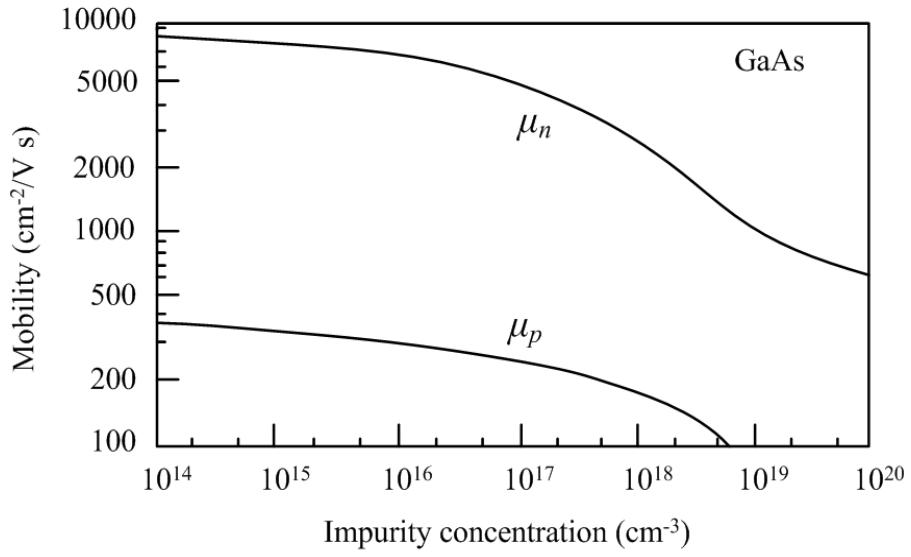


Figure 2.6 Mobility of GaAs at 300 K as a function of impurity concentration [24].

As described above, the average velocity, caused by the random thermal movement of the electrons, is zero. When an external electric field is applied to the material, electrons gain an additional velocity which is called drift velocity u_{drift}. Then, a force equal to $-q\mathscr{E}$ causes the acceleration of the electrons to the opposite direction of the electric field $\mathscr{E}$. Therefore, the momentum of the electrons is given by [24]:

$$m_e^* u_{drift} = -q\mathscr{E}\tau_c \tag{2.5}$$

After solving with respect to the drift velocity:

$$u_{drift} = -\mu_n \mathscr{E} \tag{2.6}$$

where μ_n is the electron mobility equal to:

$$\mu_n = \frac{q\tau_c}{m_e^*} \tag{2.7}$$

The drift current density is given by:

$$J_{drift} = qnu_{drift} \tag{2.8}$$

As described in Section 2.2, mobility is a characteristic property of the material which is determined by the periodic potentials in the crystal. Here, mobility shows how strongly the electron transport is affected when an external electric field is applied to the semiconductor.

Charge transport occurs even if no external electric field is applied, when the electron concentration inside the semiconductor is not uniform. Electrons flow from the areas with high concentration towards the areas with low concentration until the non-uniformity is compensated. The so-called diffusion current, can also result from the placement of two different materials together. The existence of the diffusion current can be explained as a result of the non-uniform thermal movement of the electrons. Examining the cross section of a uniform material, the electrons arriving from the left and from the right side are equal. Consequently, the individual currents cancel each other and the total current is zero. Assuming that the electron concentration is higher at the right side of a semiconductor, the carriers arriving at the cross section from the left side are less than the ones arriving from the right side. Thus, the diffusion current is created while electrons are moving towards the side of the semiconductor with lower concentration. The diffusion current density J_n is proportional to the gradient of the carrier concentration as [24]:

$$J_n = qD_n \frac{dn}{dx} \tag{2.9}$$

where D_n is the diffusivity of the material which is related to the mobility through the

Einstein relation [24]:

$$D_n = \frac{kT}{q}\mu_n \tag{2.10}$$

High field phenomena

Equation 2.6 indicates that the drift velocity is proportional to the external electric field. However, this assumption is valid only for a relatively low electric field, where the drift velocity is significantly lower than the thermal velocity ($1 \cdot 10^7$ V/cm at room temperature for semiconductors [15]). Under these conditions, the drift velocity and the thermal velocity can be considered as independent. When $\mathscr{E}$ increases and u_{drift} approaches the value of u_{th}, the relation between u_{drift} and $\mathscr{E}$ diverges from the linear Equation 2.6. Figure 2.7 presents the drift velocity versus the electric field for a heavily doped sample of GaAs with $5 \cdot 10^{18}$ cm^{-3} n-type doping concentration. As $\mathscr{E}$ increases and u_{drift} becomes comparable to u_{th}, the scattering effects play a significant role to the electron transport. The energy given by the field is no longer transformed to an additional kinetic energy of the carriers but is consumed through the various scattering mechanisms. For highly doped materials, impurity scattering becomes dominant and the drift velocity reaches a saturation value u_{sat} as depicted in Figure 2.7 [15].

For lightly doped materials, the drift velocity also increases in a linear fashion at low electric fields but the slope and the u_{sat} are higher due to the reduced impurity scattering. However, when exceeding a critical electric field the behaviour of the drift velocity is different for materials like GaAs and InP in comparison with Si. As described in Section 2.2, the energy diagrams of GaAs and InP present more than one conduction valley in contrast with Si which is a single-conduction valley material. The curvatures of the conduction valley determines the effective mass and as a consequence the mobility of the electrons lying there.

When a small electric field is applied to the semiconductor, electrons gain sufficient energy and transfer from the valence band to the centre conduction valley Γ, as depicted in Figure 2.8(a). Therefore, u_{drift} increases monotonically with $\mathscr{E}$. If $\mathscr{E}$ is higher than a critical value, electrons have enough energy to overcome the energy gap between the centre conduction valley Γ and the satellite valley L transferring to the latter. The threshold field is equal to 3.5 kV/cm and 10.5 kV/cm and the energy separation between the two valleys is 0.31 eV and 0.53 eV for GaAs and InP, respectively [16].

The overall mobility of the system is equal to the average mobility of the carriers as [24]:

$$\overline{\mu} = \frac{\mu_{\Gamma} n_{\Gamma} + \mu_L n_L}{n_{\Gamma} + n_L} \tag{2.11}$$

The drift velocity is given by:

$$u_{drift} = -\overline{\mu}\mathscr{E} \tag{2.12}$$

where μ_{Γ} and μ_L represent the mobilities and n_{Γ} and n_L are the number of carriers at the two conduction valleys. For both GaAs and InP, electrons transferred to the *L* valley have a lower mobility as the new valley has a smaller curvature (Figure 2.8). As a result, the overall mobility of the carriers decreases and so does the drift velocity. Under these conditions, the material shows a negative differential resistance (NDR). The phenomenon is also known as the Gunn effect and it is fundamental for the formation of Gunn oscillations as presented in Section 2.6. The NDR appears only when the material is lightly doped otherwise the drift velocity degradation starts from lower electric fields due to the impurity scattering as depicted in Figure 2.7. Figure 2.9 illustrates the drift velocity versus the electric field for GaAs, InP and Si [26]. GaAs and InP show an NDR after the critical electric field which is higher for InP which presents a higher energy difference between the Γ and the *L* valley. As Si is a single-conduction valley material, the Gunn effect does not exist.

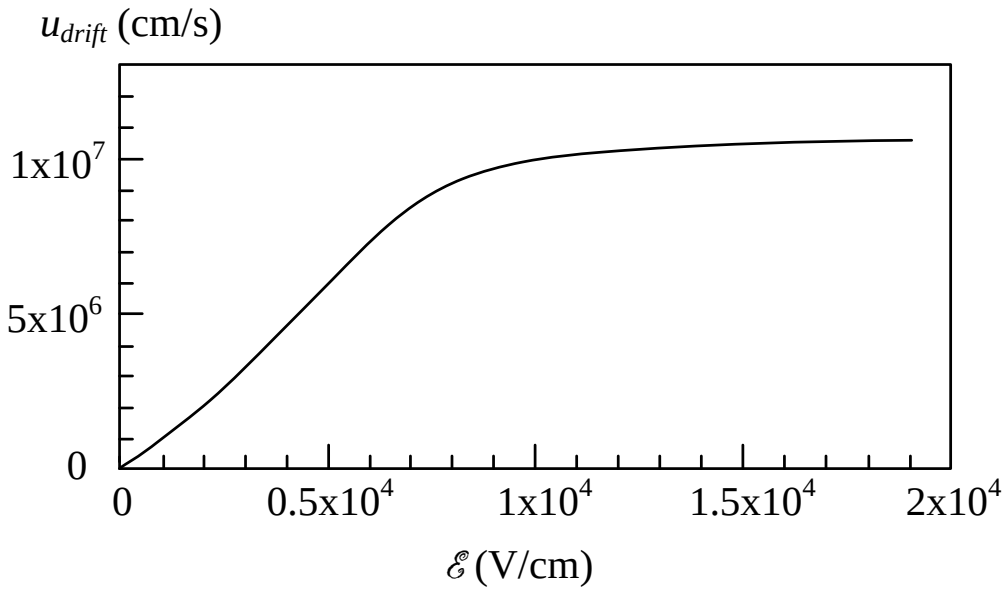


Figure 2.7 Electron drift velocity as a function of the external applied field for heavily doped ($5 \cdot 10^{18}$ cm-3) GaAs [15].

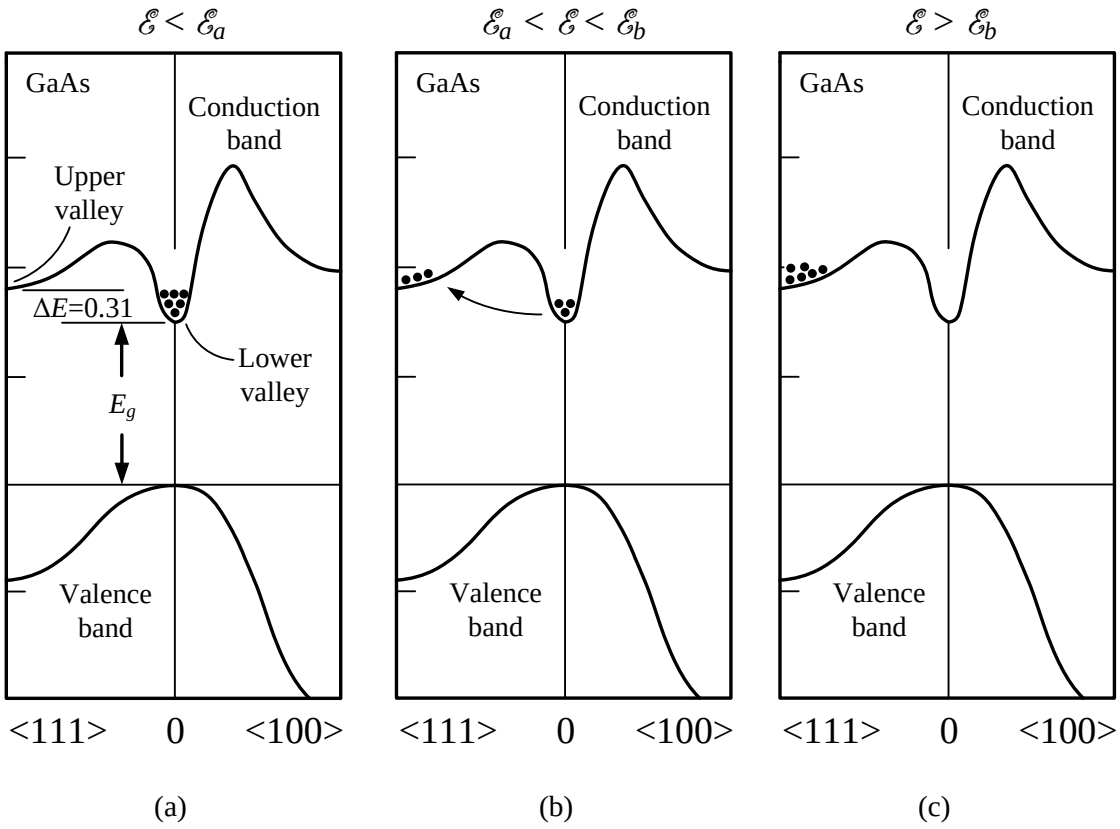


Figure 2.8 Electron distributions at the conduction valleys under various applied electric fields for multi-valley semiconductors [24].

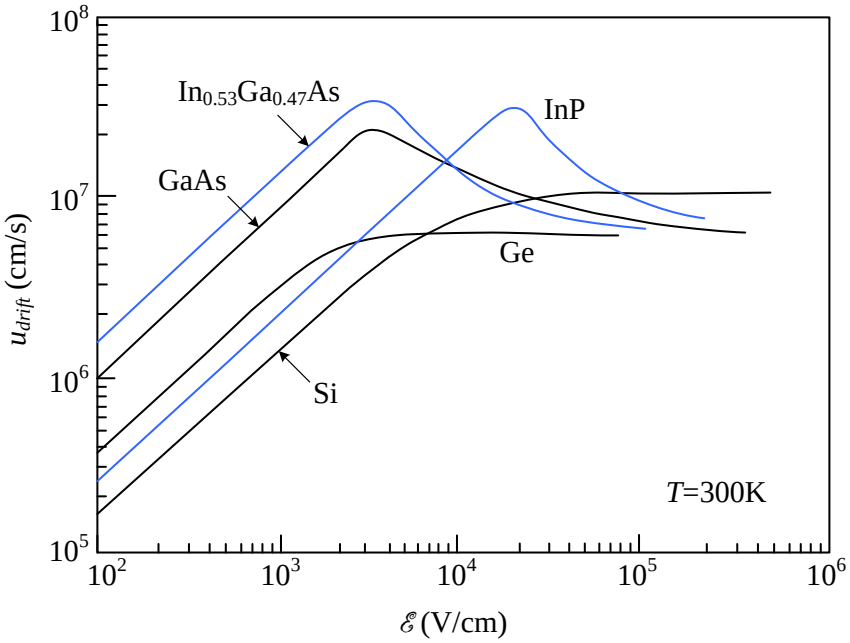


Figure 2.9 Drift velocity as a function of the external applied field for various semiconductors [26].

For very high electric fields, exceeding the NDR region, the current starts increasing again as a result of the impact ionisation effect which is also known as the avalanche process. This is caused by the electron-hole pairs that are generated after the interaction of high-energy carriers with the lattice. If the accelerated electrons get enough energy from the applied field, they can break valence bonds after colliding with the lattice. In this way, an electron-hole pair is produced as the bond electron is ionised to the conduction valley leaving an empty space behind. The ionised electron gets highly accelerated before the next collision where a new electron-hole pair is generated. As a consequence, the current of the semiconductor starts rising again as more electrons transfer to the conduction valley.

2.4 Heterojunctions

Heterojunctions are formed when two materials with similar lattice constants and different band gaps are brought together to form a contact which is also known as heterostructure. The deployment of modern epitaxial growth techniques as metal organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE) was essential for the realisation of heterojunctions. Modern optoelectronic and microwave active devices resulted from the development of band gap engineering.

Limitations arise during the design of heterostructures as the individual layers need to form a high quality material. Ideally, the stack of the various layers and the substrate should have the same lattice constant and the total structure should be lattice-matched. Any mismatch between the different layers can degrade the quality of the material and the performance of the devices. The defects generated can cause poor carrier mobility, increased current leakage and poor surface morphology [26].

Figure 2.10 presents the lattice constants and the band gaps for some binary and ternary compounds that are important for the purposes of this work. The difference between the lattice constants of GaAs and AlAs is only 0.14% and the difference between their band gaps is 0.73 eV [15]. Therefore, every composition of $Al_xGa_{1-x}As$ can be grown on GaAs and the two materials are used to form the commonly used AlGaAs/GaAs heterojunction. However, it is often desired to introduce layers with dissimilar lattice constants to the structure. As an example, $In_{0.53}Ga_{0.47}As$ provides superior current transport characteristics but it cannot be grown directly on GaAs.

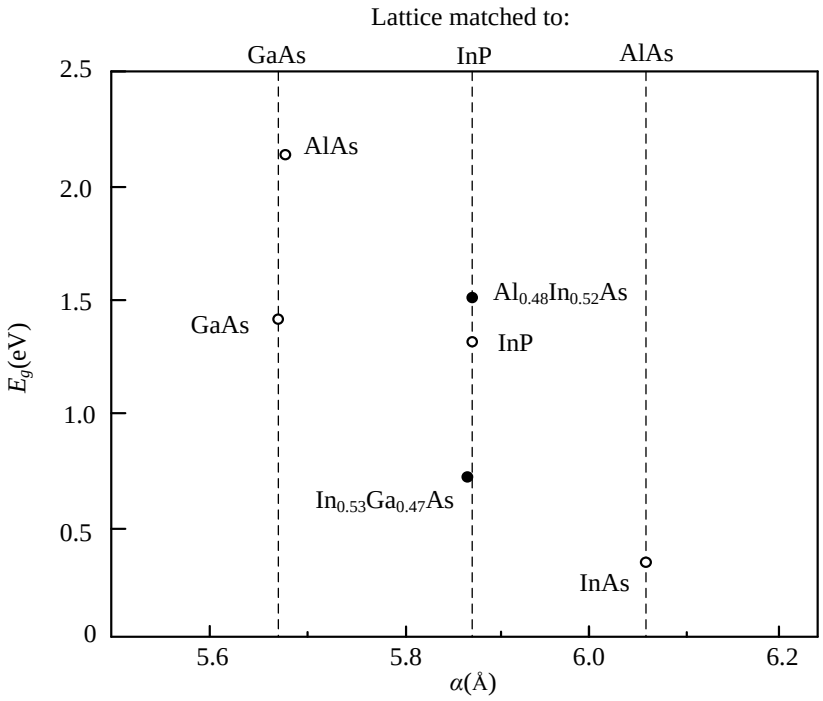


Figure 2.10 The lattice constant and the band gap for some III-V compounds.

A commonly used technique, to overcome the mismatch of the lattice, is the growth of the desired layers on the substrate in a metamorphic way. A buffer layer is grown on the top of the substrate, and the lattice constant is changed gradually until the desired lattice constant is achieved. This method makes feasible the growth of InGaAs with high indium content equal to 53% even if the lattice constants of the two materials are significantly different.

Pseudomorphic growth is an alternative technique to form layer structures with slightly different lattice constants. If the thickness of the epitaxial layer is below a critical value, the thin layer can be strained under the effect of elastic forces and matches with the surrounding layers. As an example, the critical thickness for growing a layer of $In_{0.23}Ga_{0.77}As$ on GaAs is approximately 12 nm [26]. The introduction of $In_{0.23}Ga_{0.77}As$ as a channel layer can enhance significantly the performance of GaAs-based HEMTs and Gunn diodes, as described in the next chapters.

In the next section, the formation of the AlGaAs/GaAs heterojunction is described as an example. The energy diagrams of the two compounds are illustrated in Figure 2.11(a) when they are separated. The electron affinity $q\chi_i$ represents the energy required for an electron

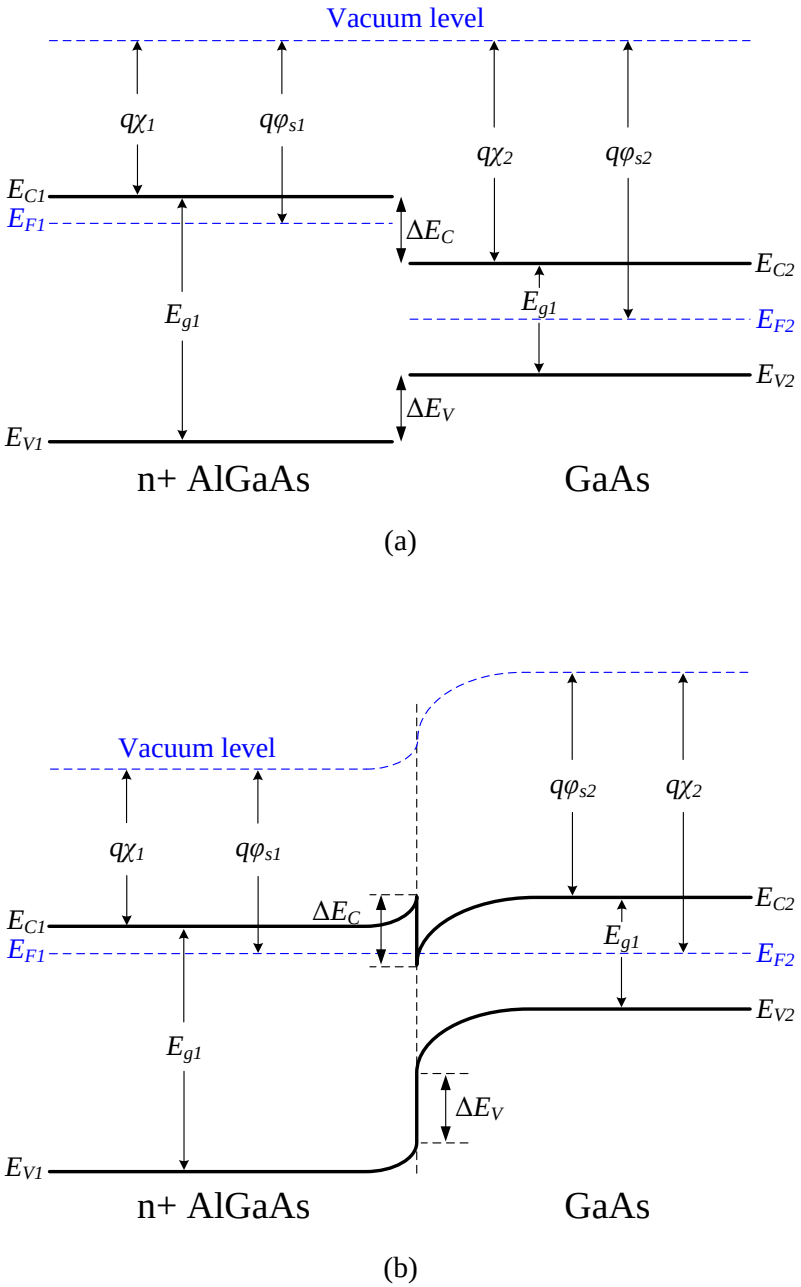


Figure 2.11 The individual energy diagrams of the isolated n+ AlGaAs and GaAs (a) and the resulted band diagram after the formation of the AlGaAs / GaAs heterojunction (b).

to transfer from the bottom of the conduction valley to vacuum. The energy required for an electron to transfer from the Fermi level to free space is represented by the work function $q\varphi_{si}$. The two materials have different band gaps and since AlGaAs is doped with additional electrons, the Fermi level has moved closer to the bottom of the conduction valley.

When the two materials are brought in contact, the AlGaAs / GaAs heterojunction is formed and the energy diagram of the system is formed according to the following mechanism. The

Fermi level at the side of the doped AlGaAs is higher and electrons start flowing to the side of the undoped GaAs where the Fermi level is lower. This electron transfer is in agreement with the principle of the electrons diffusing from high to low concentration regions. The electrons accumulating at the GaAs side leave behind them the positively charged donors. Therefore, an electric field is formed, pointing to the direction of the electron flow. As more electrons flow to the right side of the heterojunction, the electric field grows opposing further electron diffusion. This negative feedback mechanism leads to the establishment of an equilibrium state where the Fermi levels of the two materials are eventually aligned and no more electron diffusion takes place. As a result, the conduction bands across the heterojunction bend in a way that an "N" shape discontinuity is created, as illustrated in Figure 2.11(b). Since the properties of the materials do not change, the conduction bands will remain parallel with the vacuum level. As the vacuum level of the system has to be continuous, the energy difference between the conduction bands at the interface is equal to the difference of the electron affinities of the two materials:

$$\Delta E_C = q\chi_1 - q\chi_2 \tag{2.13}$$

The areas across the heterojunctions are known as space-charge regions or depletion regions. Away from the heterojunction interface, no electron transport occurs and the energy diagrams are the same as the energy diagrams of the separated semiconductors. These regions are known as the neutral regions.

The formation of the triangular shaped potential well at the side of GaAs is crucial for the operation of high speed electronics. As described in Section 2.3, lattice and impurity scattering are the two dominant mechanisms that degrade the mobility of the carriers. As lattice scattering depends on the temperature, the carrier mobility can be increased only by reducing the impurity scattering. This could be achieved by decreasing the doping concentration. However, the reduction of the doping concentration would reduce the available conduction electrons and the current level would be insufficient. The solution is given by the triangular potential well where the carriers accumulate at the side of GaAs, away from the parental AlGaAs atoms. By this method, which is known as modulation doping, the channel is formed at the side of undoped material where the impurity scattering is significantly lower.

Electrons accumulating in the triangular well are limited to move in the *xz* plane as the transport in the *y* direction is prohibited by the potential barriers (Figure 2.12). The thickness

of the channel is in the order of 100 Å which is narrower than the de Broglie wavelength of an electron at room temperature (260 Å). Thus, the energy levels in the triangular well are discrete and the momentum of the electrons moving in the *xz* plane is quantized. The channel of electrons lying in the triangular well is referred as a two-dimensional electron gas (2-DEG) [27, 28]. The advantage of using modulation doping over a simply doped bulk material for the channel of the device, is demonstrated in Figure 2.13. The reduced impurity scattering that occurs in the 2-DEG channel is demonstrated by the enhanced current characteristics of the AlGaAs/GaAs heterojunctions versus an n-type GaAs sample [29].

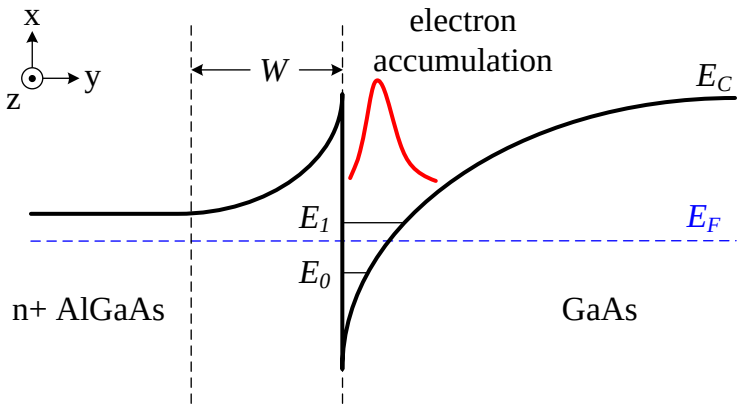


Figure 2.12 Band diagram at the AlGaAs/GaAs interface [30].

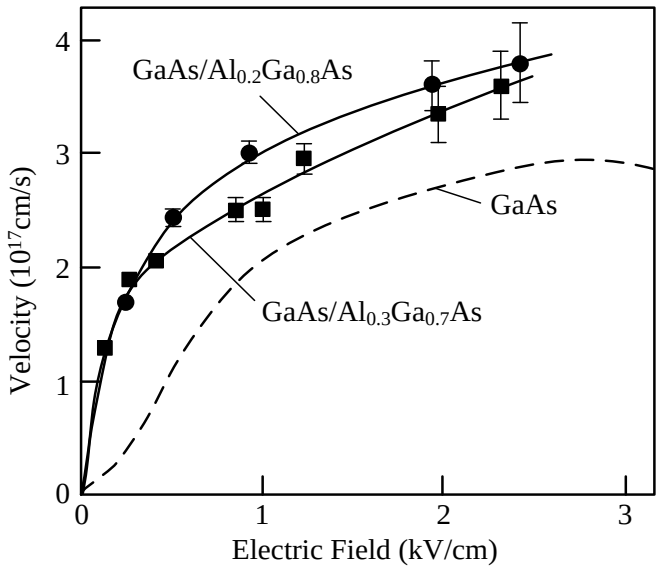


Figure 2.13 Velocity versus electric field dependences for electrons in the 2-DEGs and for n-type GaAs at 4.2 K [29].

2.5 Metal-semiconductor contacts

The advantages introduced by the modulation doping for the formation of a high-mobility channel were described in the previous section. In addition to the enhanced current transport in the channel, the appropriate interface needs to be developed for the external control of the devices. For the example of a field effect transistor, the current needs to be driven in and pulled out of the channel through the drain and the source electrodes. In addition, the bias at the gate should modulate efficiently the channel of the device. The next sections present the interfaces developed between semiconductors and metals, ensuring the functionality of the devices.

2.5.1 The Schottky contact

The basic interface for the control of the device is created when a semiconductor is simply brought in contact with a metal. The mechanism for the establishment of the electron equilibrium state is very similar to the one that takes place between two semiconductors. The energy diagrams of the two individual materials are shown in Figure 2.14(a). The Fermi level of the metal concurs with the bottom of the conduction valley, as all the electrons are free to transfer in the crystal. After bringing the two materials in contact, electrons start diffusing from the semiconductor to the metal as the Fermi level of the former is higher than the one of the latter. A potential barrier starts growing at the side of the semiconductor leading to the bending of the conduction band close to the interface. The barrier grows until no more electron transfer occurs between the two materials. The height of the resulted barrier, which is known as Schottky barrier, is given by the difference between the electron affinities of the two materials [26]:

$$q\varphi_{Bn} = q(\varphi_m - \chi) \tag{2.14}$$

The potential barrier V_{bi}, which is also known as built-in potential, opposes to the transfer of the electrons from the side of the semiconductor to the metal. The built-in potential is given by the difference between the work functions of the two materials and also by:

$$V_{bi} = \varphi_{Bn} - V_n \tag{2.15}$$

where qV_n is the difference between the bottom of the conduction band and the Fermi level of the semiconductor.

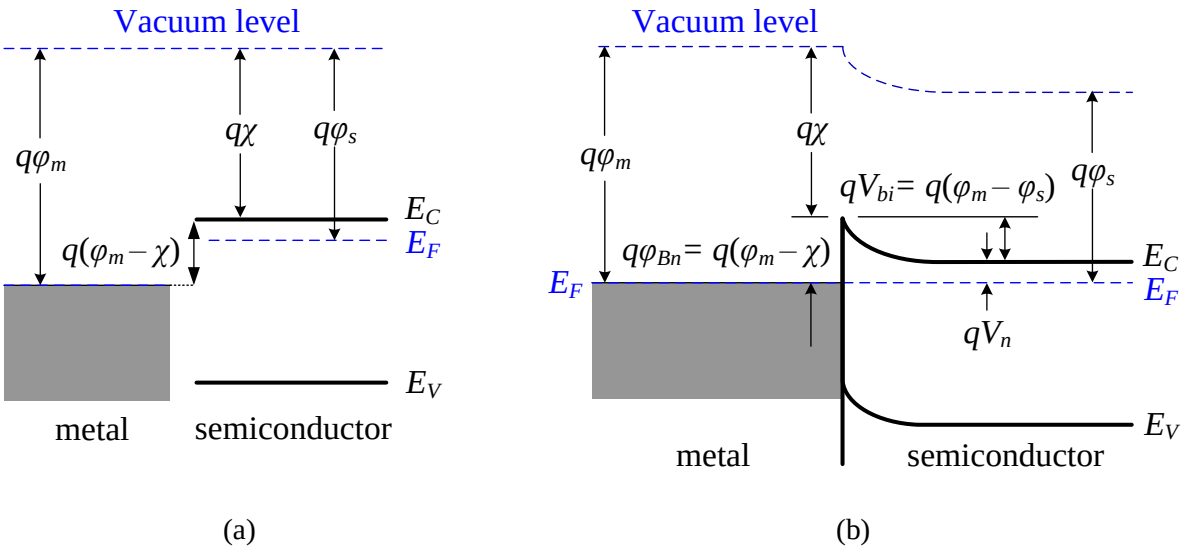


Figure 2.14 The energy diagrams of the isolated metal and the n-type semiconductor (a) and the energy diagram of a metal-semiconductor contact (b).

The presence of midgap states at the interface between the metal and the semiconductor can significantly affect the position of the Fermi level relatively to the conduction and valence bands. In the case that the surface states are located below the Fermi level, electrons from the conduction band will fill these states. Effectively, a depletion region will be created at the surface region with positive space-charge. The space-charge will be equal to approximately $+e\,N_D\,d_{sc}$, where d_{sc} is the width of the space-charge region. Thus, the electric field created prevents further electron transfer towards the surface states and the Fermi level in the semiconductor will be aligned with the top of the filled surface states. Since III-V compounds have large surface state density, the Fermi level is effectively pinned at the energy of the midgap states. As a consequence, the barrier height is no longer dependent on the metal work function, but is determined by the surface state density. Ideally, the new surface states should be moved out of the forbidden gap of the semiconductor, and the Fermi level should become unpinned. The unpinning of the Fermi level can be performed with the passivation of the surface that changes the chemical composition of the surface and the energy of the dominant surface states.

If a positive external bias V_F is applied to the metal, the energy bands of the semiconductor will rise by a factor of qV. Under the forward biasing, the built-in potential will be reduced to V_{bi} - V_F. Therefore, electrons will flow more easily from the semiconductor to the metal. When a negative bias V_R is applied to the metal, the barrier will increase to q (V_{bi} + V_R). In

contrast with the forward bias, electron transfer from the semiconductor to the metal is more difficult to occur under reverse biasing conditions. The effects of the two biasing conditions at the energy diagram of the contact are illustrated in figures 2.15(a) and 2.15(b). The width W of the potential barrier, also known as the depletion width, is also affected by the applied voltage V as given by Equation 2.16 [26].

$$W = \sqrt{\frac{2\varepsilon_s (V_{bi} - V)}{qN_D}} \tag{2.16}$$

where ε_s is the permittivity of the semiconductor. It comes from Equation 2.16 that the width of the barrier depends on the bias voltage at the metal and the doping concentration of the semiconductor. The dependence of the barrier shape according to these factors determines strongly the current transport across the Schottky contact, as described in the next section.

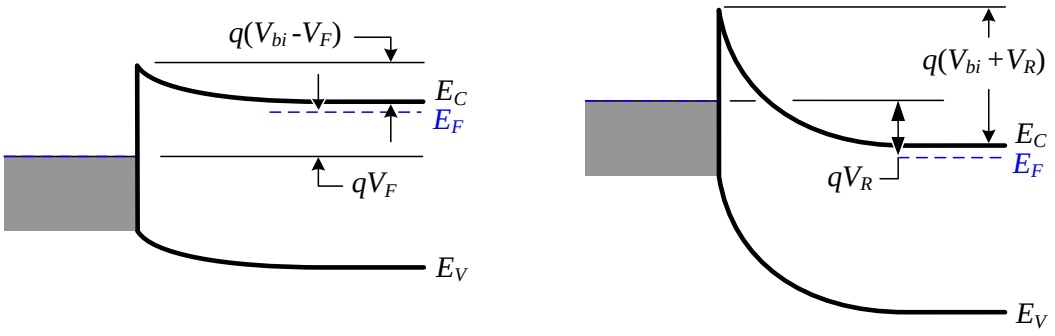


Figure 2.15 The energy diagrams of the metal-semiconductor interface under forward (a) and reverse (b) biasing conditions.

2.5.2 Current transport across barriers

The main mechanisms for current transport across the metal-semiconductor interfaces are thermionic emission (TE), field emission (FE) and a combination of them, the thermionic field emission (TFE). The dominant mechanism is determined by the height and the width of the potential barrier. As discussed in the previous section, the shape of the barrier is strongly dependent on the biasing conditions at the metal. The current transport mechanisms and their dependence on the applied bias are described in this section.

TE is the dominant current transport mechanism at room temperature. As the name indicates, TE is strongly dependent on the temperature of the system. This mechanism represents the

classic current transport where electrons can transfer across the metal-semiconductor interface only after gaining enough energy to overcome the height of the barrier. According to the Fermi-Dirac statistics, the number of electrons that have sufficient energy to overcome the barrier is given by [26]:

$$n_{th} = N_C \exp\left(-\frac{q(\varphi_{Bn} - V)}{kT}\right) \tag{2.17}$$

Equation 2.17 indicates that as temperature increases more electrons obtain enough energy to transfer across the barrier. The population of the electrons transferring due to TE is also affected by the applied bias. As described in the previous section, the built-in potential decreases under forward biasing and electrons flow from the semiconductor to the metal accelerated by the externally applied field. TE is less important in highly doped semiconductors where the barrier is narrower and the majority of the current transport occurs due to FE.

Field emission occurs due to the quantum tunnelling effect where electron transfer is forbidden by the classic theory. If the barrier is narrow enough, there is a finite probability that electrons will transfer through the barrier even if their energy is lower than the energy required for the TE. FE becomes the dominant mechanism at high doping concentrations for electrons at the bottom of the conduction band as the barrier width becomes thinner when N_D increases (Equation 1.16). Equation 2.18 gives an estimated relation for the current-voltage characteristic of the junction due to FE [16].

$$I_{FE} \propto \exp\left(-\frac{q\varphi_{Bn}}{E_{00}}\right) \tag{2.18}$$

where E_{00} is the characteristic tunnelling energy given by:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\varepsilon_s m_e^*}} \tag{2.19}$$

Thermionic field emission occurs as a combination of thermionic and field emission. Current transport can occur due to TFE if electrons do not have sufficient energy to transfer

exclusively through TE or if the barrier shape forbids any FE. Thus, as the barrier width decreases for higher energy states, tunnelling is possible for electrons that have energy higher than the minimum of the conduction band. As TFE is a combination of the two individual transport mechanisms, it is affected by the temperature, the doping concentration and the barrier shape. The various transport mechanisms described above are shown in Figure 2.16.

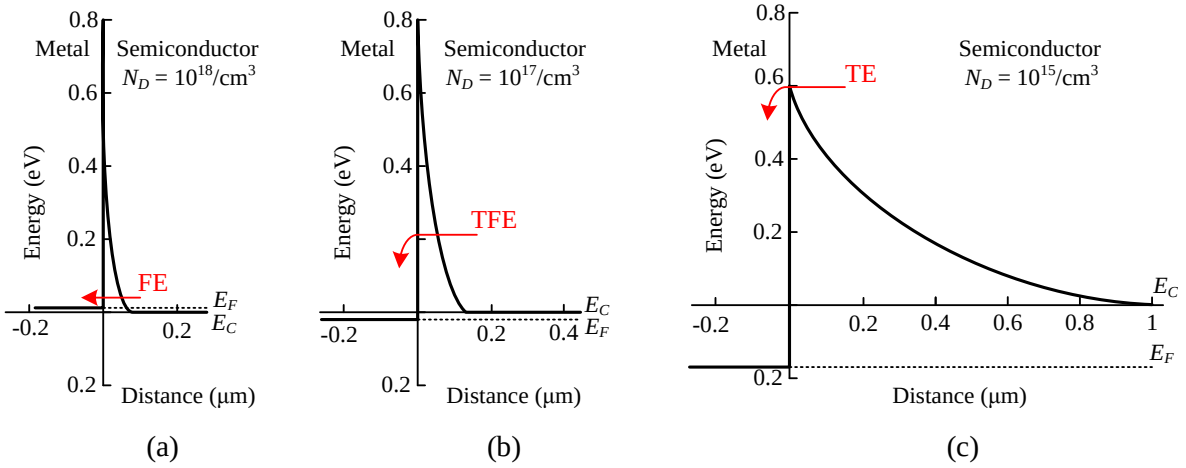


Figure 2.16 The main mechanisms for current transport across a metal-semiconductor junction. The junctions are forward biased with $N_{D1} > N_{D2} > N_{D3}$. The arrows indicate the electron transfer mechanism [31].

2.5.3 The Ohmic contact

Ohmic contacts are basically formed by a metal-semiconductor interface where FE is the dominant current transport mechanism. High quality Ohmic contacts are expected to show very small contact resistance in order to cause minimum degradation to the device performance. Current also needs to be transferred across the interface in a linear way with minimum losses.

When the doping concentration of the semiconductor is very high, the width of the barrier becomes very narrow and current transport across the contact occurs due to the tunnelling effect. The barrier height, which is determined by the difference between the electron affinities of the semiconductor and the metal, can be lowered with the appropriate material selection. The contact resistance of electrodes on highly doped semiconductors is given by Equation (2.20) [26].

$$R_C = \exp\left(\frac{4\varphi_{Bn}\sqrt{m_n \varepsilon_s}}{N_D \hbar}\right) \tag{2.20}$$

where the doping concentration, the barrier height and the electron mobility are the critical parameters for the formation of high quality metal-semiconductor interfaces.

2.6 The high electron mobility transistor (HEMT)

The invention of the 2-DEG by Dingle et al. [32] in 1978 lead to the generation of a new series of devices with exceptional characteristics for high frequency applications. The innovative method of modulation doping reduces the ionized and impurity scattering of the carriers by separating them from their parent donors, as described in Section 2.4. The realisation of the HEMT by Mimura in 1979 [33] was a direct consequence of Dingle's invention and has become one of the most important devices composing modern MMICs. The next section presents the main structure of the HEMT based on the heterojunctions and the metal-semiconductor interfaces. The DC and small-signal operation characteristics are described in Section 2.6.2.

2.6.1 Device structure

Figure 2.17 illustrates the basic HEMT structure where the GaAs channel layer is grown between the two AlGaAs layers. As described in Section 2.4, the heterojunctions between the two materials with different band gaps are used to form a quantum well confining the electrons inside the channel. In this example, the channel is grown on the top of the AlGaAs buffer layer. Apart from the confinement of the electrons, the buffer layer is also used to isolate the active device from the substrate. The epitaxial layers of the buffer consist of high quality crystal, minimising any possible transfer of defects emanating from the substrate. In this approach, the AlGaAs layer on the top of the channel is undoped and a δ-doping layer is used to supply the channel with electrons. Delta doping layers are very thin layers that usually consist of silicon with very high doping concentration in the order of 10^{12} cm^{-2}. The undoped AlGaAs layer between the channel and the δ-doping layer is known as spacer that separates the channel electrons from the parent donors. The 2-DEG resides in the channel, close to the interface with the spacer. The barrier is grown after the δ-doping using another layer of undoped AlGaAs. Finally, a highly doped GaAs layer is grown on the top of the barrier, to

form a low-resistive metal-semiconductor interface. The so-called cap layer is removed in the middle area and the three electrodes are deposited to control the device.

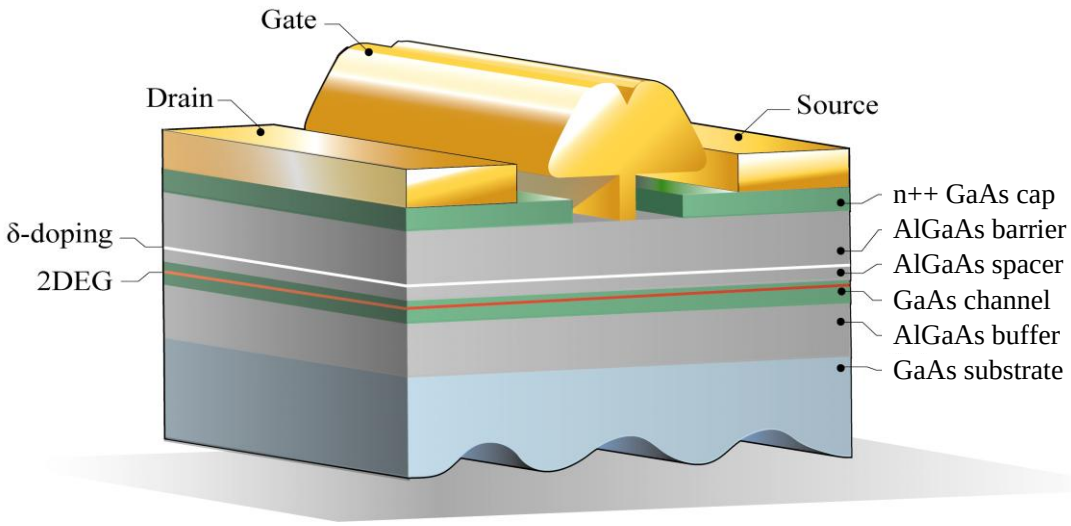


Figure 2.17 The basic structure of the HEMT.

The two electrodes on the top of the cap layer are the drain and the source which provide access to the current in the device. As the degradation of the current has to be as small as possible, quality Ohmic contacts are required at this metal-semiconductor interface. As described in Section 2.5.3, electron transport across Ohmic contacts depends on the width and the height of the barrier. The width of the barrier is significantly decreased because of the heavy doping of the cap layer. For the further reduction of the barrier height, a metamorphically grown lattice-matched material with a lower band gap, such as $In_{0.53}Ga_{0.47}As$, can be used to favour the field effect mechanism.

The middle electrode with the “mushroom” shape is the gate of the device which modulates the current that flows from the drain to the source. In contrast with the Ohmic electrodes, the gate is placed on the undoped AlGaAs layer to form a Schottky contact. The strip of the cap layer is removed before the deposition of the gate metal. The interface between the undoped semiconductor and the metal creates a wide barrier ensuring that minimal current transport occurs between the gate and the channel. The successful etching of the cap strip and the realisation of the mushroom gate are the most critical steps of fabrication. As presented in the next chapters, the geometries of the etched area and the gate play a significant role in the performance of the device.

2.6.2 Device operation

In the case that no voltage is applied at the gate of the transistor, the majority of the electrons accumulate in the 2-DEG region of the channel. Therefore, the current is dependent on the external field given by the potential difference between the drain and the source. A positive voltage applied at the drain causes the current transport. The source terminal is usually connected to ground, achieving a low noise operation of the transistor at high frequencies [34]. At low biasing voltages, the current increases in a linear way with the voltage where the slope is determined by the overall resistance between the electrodes (Figure 2.18). As the drain to source voltage increases, the scattering phenomena between the carriers and the material become more intense. Under these conditions the current reaches the saturation region and further increment of the drain voltage has minor effect. When the biasing voltage exceeds a critical value, the device enters the breakdown region and the current increases dramatically (Figure 2.18). Due to the very high field, electrons attain enough energy to release bond electrons when scattering with them and the device can be damaged permanently. The breakdown voltage depends on the geometry of the device as higher electric fields occur when the distance between the electrodes is smaller.

The current transport characteristics are strongly dependent on the properties of the semiconductor, particularly the mobility, the velocity saturation and the energy band diagram. The breakdown voltage depends also on the band gap of the material. GaN which has a very large band gap equal to 3.44 eV [23] is currently the most studied material for high power applications where a very high biasing voltage can be applied (~ $5 \cdot 10^6$ V/cm [22]) without breaking down the device.

Since the biasing of the drain and the source is established, a voltage change at the gate will modulate the charge in the channel. By applying a negative voltage to the gate, the barrier width increases and consequently the electron concentration in the channel reduces. Effectively, the electrons at the gate metal push the electrons accumulating in the channel deeper into the buffer layer, the area under the gate is depleted and the device presents extremely high resistance. Consequently, the current flowing from the drain to the source will be reduced after applying a negative voltage as a result of the lower carrier concentration in the channel. When the device is biased at the saturation region, the channel current is given by Equation (2.21) [30].

$$I_{DS} = q\, n_s\, u\, W = 0.8\, I_F \tag{2.21}$$

Where n_s is the sheet electron density per cm^2 in an undepleted 2-DEG, u is the average electron drift velocity and W is the width of the device. I_F represents the maximum current going through the channel when the gate is forward biased. The sheet concentration is given as a function of the gate to drain voltage by [30]:

$$n_s = \frac{(V_{GS} - V_T)\,\varepsilon_s}{qd} \tag{2.22}$$

where d is the distance between the gate and the 2-DEG and $-V_T$ is the threshold voltage of the gate that depletes completely the channel. The transconductance of the device gives the modulation efficiency, i.e. how much is the current affected by changes of the gate voltage for fixed drain and source biasing. Thus, the intrinsic transconductance is by definition given by:

$$g_{m0} \equiv \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \tag{2.23}$$

After replacing equations 2.21 and 2.22 and solving Equation 2.23, the intrinsic transconductance is given by:

$$g_{m0} = \frac{u\varepsilon_s W}{d} \tag{2.24}$$

Therefore, the intrinsic transconductance is improved for materials with higher average electron velocity and for wider devices. On the contrary, g_{m0} decreases for longer d as the channel is placed further away from the gate and the modulation is less effective.

When the gate voltage becomes lower than the threshold voltage, the channel becomes completely depleted. Then the device is so-called pinched off and little current transport occurs between the two Ohmic electrodes. The modulation of the channel current by applying different gate voltages is presented in Figure 2.18.

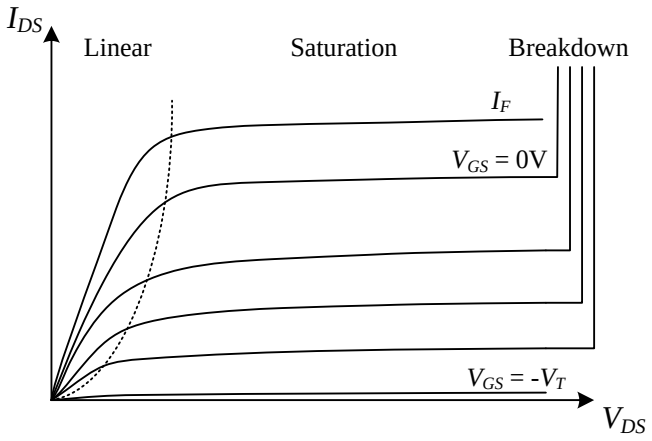


Figure 2.18 Typical I_{DS} - V_{DS} characteristics as a function of the gate voltage V_{GS} .

The above transconductance calculations are referred to the intrinsic model of the device which represents the area near the channel. However, the actual performance of the device is strongly affected by the parasitic resistances appearing at the access areas in the device. Figure 2.19 presents the voltage drop due to the parasitic access resistance R_S and the depletion layer. The latter shows a non-uniformity at the side closer to the drain as high electric fields appear between the positively biased drain and the gate. As the gate is biased with voltages well below zero, the depletion region extends further in the channel limiting the available travelling space for the electrons. Thus, the scattering effects with the material increase and the current saturates at lower V_{DS} biasing, as illustrated in Figure 2.18.

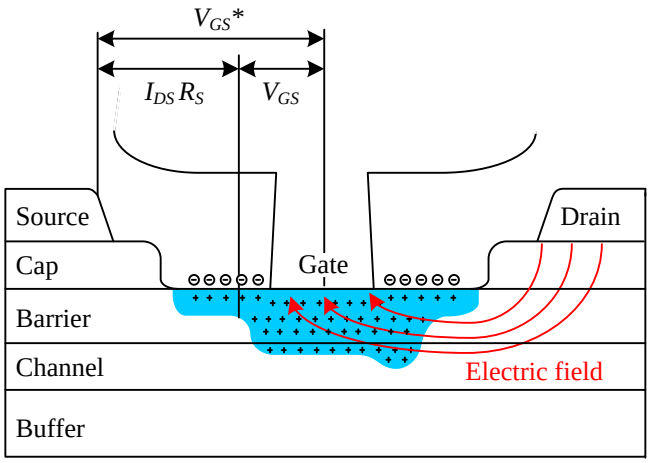


Figure 2.19 The voltage drops and the depletion layer in the device [35].

After considering the voltage drop on the source parasitic resistance, the extrinsic V_{GS}* is equal to:

$$V_{GS}* = V_{GS} + I_{DS} R_S \tag{2.25}$$

For the calculation of the extrinsic transconductance g_m the simplified equivalent of the FET is constructed as depicted in Figure 2.20. The circuit can be considered as an intrinsic transducer included inside the extrinsic transducer. As the current is the same for both transducers, it can be written:

$$V_{GS} = \frac{I_{DS}}{g_{m0}} \tag{2.26}$$

$$V_{GS}* = \frac{I_{DS}}{g_m} \tag{2.27}$$

After replacing equations 2.26 and 2.27 to Equation 2.25 the extrinsic transconductance g_m is equal to:

$$g_m = \frac{g_{m0}}{1 + g_{m0} R_S} \tag{2.28}$$

Equation 2.28 demonstrates the significance of eliminating the parasitic resistance R_S.

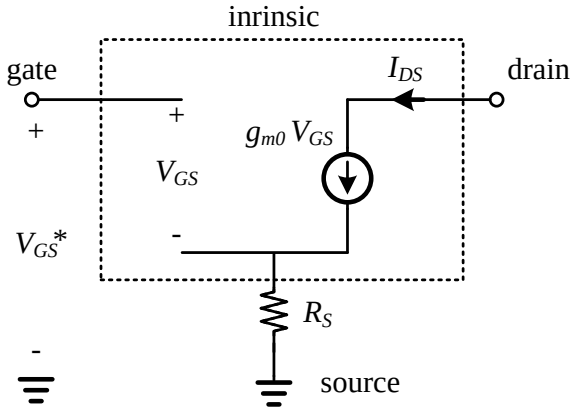


Figure 2.20 The simplified equivalent circuit representing the FET for the calculation of the extrinsic transconductance.

Apart from the channel/spacer interface, a smaller quantum well is formed at the region of the δ-doping where electrons accumulate as well. In the case that the placement of the gate metal does not deplete this area, electrons accumulate in the well creating a parallel channel to the 2-DEG. Thus, an additional negative voltage is required at the gate to deplete the total channel area. This operation is known as the depletion mode where the maximum modulation efficiency is presented when negative voltages are applied to the gate. On the contrary, the channel operates at the so-called enhancement mode when positive biasing at the gate is required to attract sufficient amount of electrons in the channel [36]. In general, a small negative offset from zero biasing is required to maximise the concentration in the channel. However, devices operating in strong depletion or enhancement mode present limited performance and the fabrication procedure or the layer structure needs to be reconsidered. The modulation efficiency of the channel and the pinch off as described above, are extremely sensitive to the process followed for the fabrication of the gate. Experimental results of devices operating at different modes are presented in detail in Chapter 6.

Previously, the degradation of the transconductance caused by the parasitic access resistance R_S was presented. However, the detailed equivalent small-signal circuit becomes more complicated as more parasitic components have to be considered for high frequency operation. The intrinsic and extrinsic elements that compose the high-frequency model are presented in Figure 2.21 [17, 37, 38] .

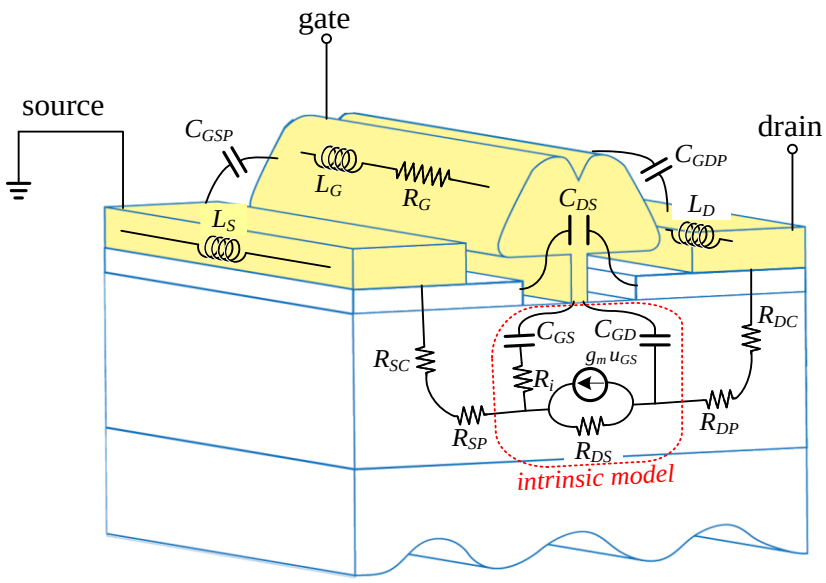


Figure 2.21 The detailed equivalent circuit for high frequency operation.

The intrinsic transconductance is represented by a voltage-controlled current source and R_{DS} stands for the channel resistance. The gate-to-channel capacitance is represented by two individual capacitors C_{GS} and C_{GD} emulating the non-uniform depletion layer presented in Figure 2.19. It arises from the geometry that the above capacitances are proportional to the Schottky contact area. The finite resistance in the path between the gate and the source is represented by R_i. The elements R_S and R_D display the total resistances between the metal electrodes and the channel. These consist of the contact resistances R_{SC} and R_{DC} that appear at the metal/semiconductor interface and the access resistances R_{SP} and R_{DP} that appear between the cap layer and the channel. The parasitic capacitances between the metal electrodes are represented by C_{GSP} and C_{GDP}. C_{DS} is the capacitance appearing between the drain and source Ohmic contacts. As will be presented in the next chapters, the drain and the source pads are extended in a large area in order to present the minimum possible contact resistance. Thus, no parasitic resistance is considered to be introduced by the metallic pads. However, metal sections with finite dimensions introduce inductance in high frequencies which is displayed by L_S and L_D for the electrode metals. As the gate terminal has a finite width, comparable with the signal wavelength in high frequencies, a parasitic inductance L_G appears at the electrode. In contrast with the Ohmic contacts, the gate metallisation unit has a small length and a resistance R_G has to be considered. R_G attenuates the signal travelling from the wide access pad along the gate metal.

The equivalent circuit of the parasitic model is illustrated in Figure 2.22 for the calculation of some significant figures of merit of the transistor. The frequency where the current gain falls to unity is represented by the cut-off frequency f_T :

$$f_T \equiv \frac{i_{OUT}}{i_{IN}} = \frac{i_D}{i_G} \tag{2.29}$$

The cut-off frequency arising from the analysis of the equivalent intrinsic circuit presented in Figure 2.22 is given by [38]:

$$f_T = \frac{g_{m0}}{2\pi\left(C_{GS} + C_{GD}\right)} \tag{2.30}$$

After including the extrinsic parasitic elements in the circuit analysis, the effective cut-off frequency for the complete circuit is given by [38]:

$$f_T^{*} = \frac{g_{m0}}{2\pi\left[\left(C_{GS}+C_{GD}\right)\left(1+\left(R_S+R_D/R_{DS}\right)+g_{m0}C_{GD}\left(R_S+R_D\right)\right)\right]} \tag{2.31}$$

The power amplification of the device is given by the maximum available gain (MAG) which results after the simultaneous impedance matching of the input and the output [38].

$$MAG = \frac{\left(f_T/f\right)^2}{4\left(R_G+R_i+R_S/R_{DS}\right)+4\pi f_T C_{GD}\left(2R_G+R_i+R_S\right)} \tag{2.32}$$

The frequency where the maximum available gain becomes equal to one is given by the maximum frequency of oscillation f_{max} [38]:

$$f_{max} = \frac{f_T}{2\sqrt{(R_G+R_i+R_S)/R_{DS}+2\pi f_T R_G C_{GD}}} \tag{2.33}$$

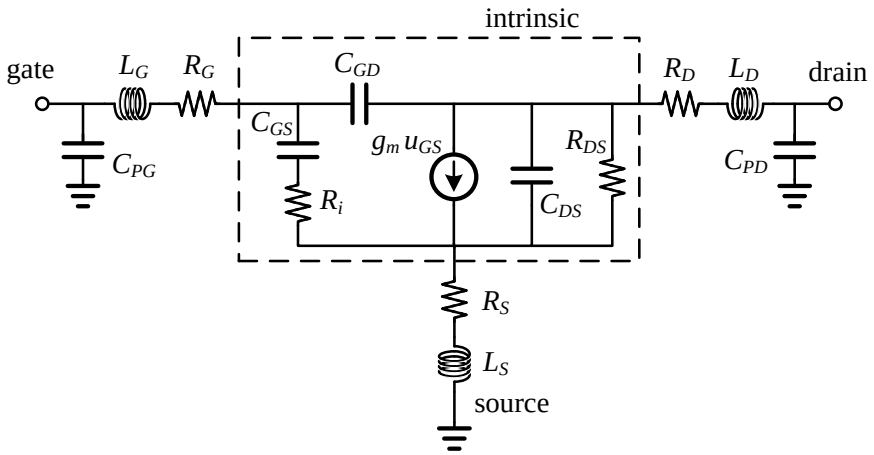


Figure 2.22 Lumped-element equivalent circuit of the transistor [38].

The significance of the elimination of the parasitic elements becomes clear after examining equations 2.28, 2.31, 2.32 and 2.33. The various resistances and capacitances cause serious degradation to the performance of the device and the layout of the transistor has to be designed carefully for their elimination. Thus, the drain and source pads are designed large

enough to minimize the contact resistances at the interface with the semiconductor. The parasitic elements C_{GS}, C_{GD} and R_G, introduced by the gate terminal play a dominant role for the device performance in high frequencies. A smaller length of the gate metallisation could reduce the parasitic capacitance. However, the reduced cross section area of the metal wire would present high resistance between the access pad and the edge of the electrode. These problems are eliminated by using a "mushroom gate", also known as "T-gate". This configuration minimises the parasitic capacitances C_{GS} and C_{GD} due to the narrow "foot". A low R_G is also achieved due to the large cross section area provided by the "head".

2.7 The Gunn diode

It was 1963 when J. B. Gunn discovered microwave frequency oscillations on GaAs and InP [1, 39]. The discovery came while Gunn was examining the current-voltage characteristics of the materials after applying high biasing voltages. When the electric field exceeds a critical value, which is characteristic for each material, a high field domain is generated at the cathode and travels towards the anode electrode of the semiconductor. Previous to this discovery, the study of Ridley and Watkins [40] and Hilsum [41] had shown that some materials can present an NDR. These studies were referred to semiconductors with multiple conduction valleys, like GaAs and InP, where electrons have higher effective masses at the satellite valleys. Ridley also predicted that domains were expected to appear in materials that show an NDR [42]. Finally in 1964, Kroemer interpreted that the Gunn oscillations occur due to the transferred electron effect [43] according to the studies of Ridley, Watkins and Hilsum.

2.7.1 Material requirements

The transferred electron effect was described in Section 2.3, where the semiconductor shows an NDR under a high applied electric field. Gunn diodes, which are also known as transferred electron devices (TEDs), present microwave instabilities if the semiconductor material meets a set of requirements. These criteria proposed by Ridley-Watkins-Hilsum are [40, 41]:

- The semiconductor must have at least two conduction valleys.
- The minimum of the satellite conduction valley needs to be higher from the minimum of the central conduction valley by a factor of several times the thermal energy of the

electrons ($\Delta E > kT$). This criterion ensures that electrons excited from the valence band will transfer first to the centre conduction valley.

- The effective masses of the electrons lying at the satellite valleys have to be higher than those in the centre valley so that the semiconductor presents an NDR after a critical electric field.

- The energy difference between the bottom of the satellite conduction valley and the bottom of the central conduction valley needs to be lower than the band gap of the semiconductor. Thus, no impact ionisation is caused before the presence of the NDR.

- The time required for the electrons to transfer between the conduction valleys has to be considerably shorter than the desired period of oscillation.

Of the materials satisfying the above criteria, GaAs and InP are the only ones that have been used extensively for the implementation of Gunn diodes.

2.7.2 Operation principles

The semiconductor becomes unstable when biased in the NDR region and a small charge perturbation can grow to form a Gunn domain. The mechanism of the domain formation is explained in Figure 2.23 and Figure 2.24. A small charge non-uniformity near the cathode at the time t_0 will cause the rise of the electric field between the accumulation and the depletion region. The electric field in Figure 2.23 is divided in three regions and matched to the corresponding drift velocities for convenience. Electrons in region *a* experience a relatively low electric field and transfer with high velocity towards the anode. Electrons in region *b* experience a higher electric field and as a consequence they transfer to the satellite conduction valley. Therefore, the current electrons travel with lower drift velocity. This allows to the electrons of the region *a* to close the distance with those of region *b*. Similarly with electrons in region *a*, electrons in region *c* have high velocity and draw away from the electrons in region *b*. Therefore, the accumulation and the depletion region are reinforced as the domain travels towards the anode ($t+t_0$). Then the domain disappears, a new domain is generated close to the cathode and the mechanism is repeated presenting the Gunn oscillations.

A small inhomogeneity in a semiconductor that shows an NDR will grow exponentially with time, as presented in the next lines. The current density equation is given by the sum of the drift and the diffusion current densities as explained in Section 2.3:

$$J = qn_0\bar{\mu}\mathscr{E} + qD\frac{\partial n}{\partial x} \tag{2.34}$$

where n_0 is the uniform charge density of the semiconductor. Here $\bar{\mu}$ is the average mobility of the electrons at the two conduction valleys as presented in Equation 2.11. For a small inhomogeneity of the charge density n-n_0, the Poisson and the one-dimensional continuity equations are given by [44]:

$$\frac{\partial \mathscr{E}}{\partial x} = \frac{-q(n-n_0)}{\varepsilon_s} \tag{2.35}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J}{\partial x} \tag{2.36}$$

After the differentiation of Equation 2.35 with respect to x and replacing with the right term of Equation 2.36, we get:

$$\frac{1}{q}\frac{\partial J}{\partial x} = -\frac{n-n_0}{\varepsilon_s / qn_0\bar{\mu}} + D\frac{\partial^2 n}{\partial x^2} \tag{2.37}$$

After replacing Equation 2.37 to Equation 2.36 the latter becomes:

$$\frac{\partial n}{\partial t} = -\frac{n-n_0}{\varepsilon_s / qn_0\bar{\mu}} + D\frac{\partial^2 n}{\partial x^2} \tag{2.38}$$

Using the method of the separated values with $n(x,t) = n_1(x)\ n_2(t)$, the solution of the differential equation is:

$$n - n_0 = (n-n_0)_{t=0}\exp\left(\frac{-t}{\tau_R}\right) \tag{2.39}$$

where τ_R is the dielectric relaxation time which represents the time constant for the neutralisation of the charge density when the average mobility is possible. In the case of a negative differential average mobility μ_- the dielectric relaxation time corresponds to the time constant for the growth of the domain and is given by Equation 2.40.

$$|\tau_R| = \frac{\varepsilon_s}{q n_0 |\mu_-|} \tag{2.40}$$

If the conditions remain the same so that Equation 2.39 is valid for the entire period of the domain travel, the maximum growth factor is equal to $\exp(L_{ac} / u_T \tau_R)$. Here, L_{ac} is the length between the cathode and the anode of the device and u_T is the effective transit velocity. The domain will grow significantly before reaching the anode only if the growth factor is high enough, which is translated to $L_{ac} / u_T \tau_R > 1$, or:

$$n_0 L_{ac} > \frac{\varepsilon_s u_T}{q|\mu_-|} \approx 10^{12}\,\mathrm{cm}^{-2} \tag{2.41}$$

for GaAs and InP. The velocity of the travelling domain is given by $u_T = u(\mathscr{E}_l) = u_D(\mathscr{E}_h)$ which results from the equal-area rule presented in Figure 2.24 [16]:

$$\int_{\mathscr{E}_l}^{\mathscr{E}_h} [u(\mathscr{E}) - u_D]\, d\mathscr{E} = 0 \tag{2.42}$$

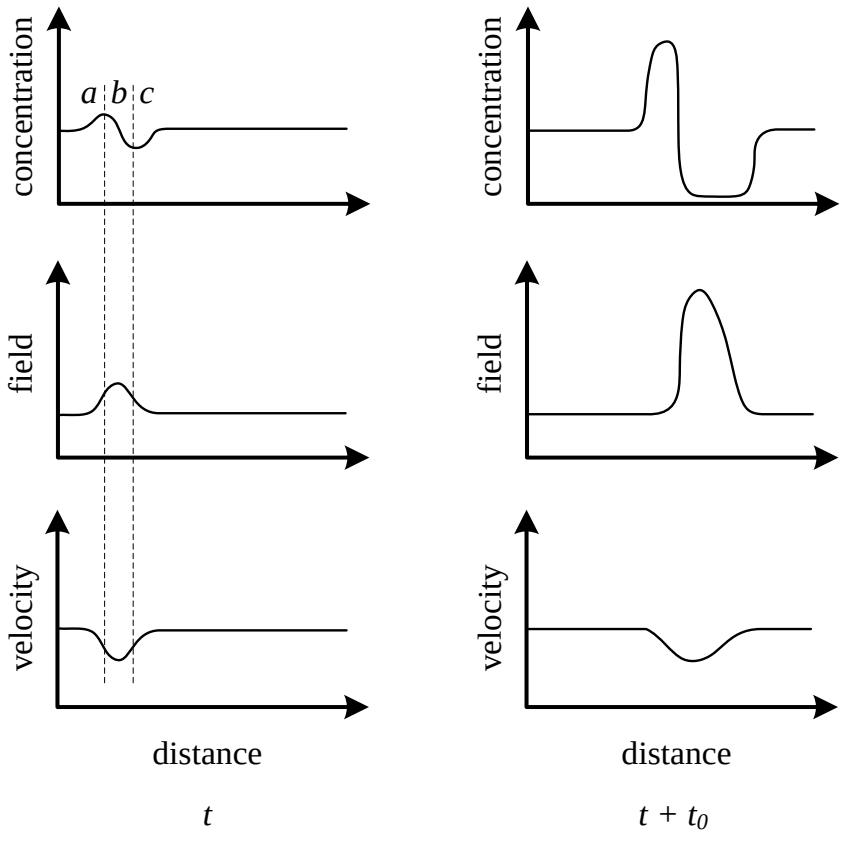


Figure 2.23 The formation of the Gunn domain.

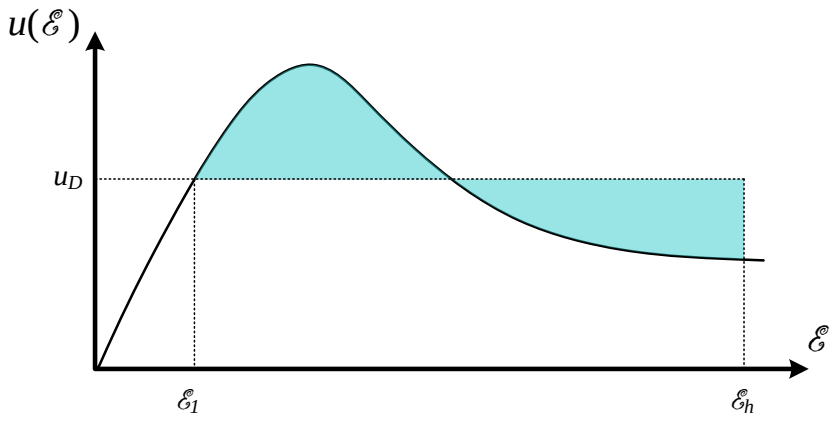


Figure 2.24 The equal-area rule for transferred electron devices.

According to the transit time domain mechanism described above, the time period where the domain is generated and reaches the anode is equal to $T = L_{ac} / u_T$, where L is the device length. Thus, the frequency of oscillation is expected to be equal to $f_{osc} = u_T / L_{ac}$. However the active length is reduced by a small factor due to the so-called dead zone that appears at the beginning of the transit region [45, 46]. This part of the channel can be considered as an additional series resistance where the electric field is not big enough, limiting the available space for the Gunn domain to grow. Therefore, the oscillation frequency is expected to be equal to:

$$f_{osc} = \frac{u_T}{L_{ac} - L_{dead}} \tag{2.43}$$

Since the effective transit velocity decreases for higher electric fields, the oscillation frequency is expected to decrease after increasing the biasing voltage. It comes from Equation 2.43 that f_{osc} can be strongly determined by the geometry of the device after choosing the length between the anode and the cathode.

The maximum oscillation frequency of the Gunn diodes is limited by the finite time that the electrons need to gain and lose energy or to transfer between the conduction valleys. Table 2.2 [16] presents some important properties of GaAs and InP that determine the oscillation characteristics. The acceleration-deceleration and energy relaxation times are 0.4-1.5 ps and 0.2-0.75 ps for GaAs and InP, respectively. Thefore, InP presents superior properties over GaAs for high frequency operation. Short-channel InP diodes have a theoretical limit of 200 GHz which is approximately double than the one for GaAs [16]. Another advantage of InP over GaAs is the reduced sensitivity to temperature fluctuations.

InP presents higher intervalley energy separation, thus less electron transfer occurs between the conduction valleys due to temperature variations.

Property	GaAs	InP
Energy gap (eV)	1.42	1.34
Low-field mobility (at 500K) ($cm^2/V \cdot s$)	5000	3000
Thermal conductivity ($W/cm \cdot K$)	0.46	0.68
Velocity peak-to-valley ratio	2.2	3.5
Threshold field E_{th} (V/cm)	3.5	10.5
Breakdown field (at $N_D = 10^{16}/cm^3$) (kV/cm)	400	500
Effective transit velocity u_T (cm/s)	$0.7 \cdot 10^7$	$1.2 \cdot 10^7$
Temperature dependence of u_T (K^{-1})	0.0015	0.001
Diffusion coefficient-mobility ratio at $2E_{th}$ (cm^2/s)	72	142
Energy relaxation time due to collisions (ps)	0.4-0.6	0.2-0.3
Intervalley relaxation time (ps)	-	0.25
Acceleration-deceleration time (ps)	1.5	0.75

Table 2.2 Semiconductor material characteristics of GaAs and InP for TEDs (at 300 K temperature unless noted) [16].

2.7.3 Devices

There are two main approaches for the implementation of the Gunn diode; vertical and planar. The characterisation of "vertical" or "planar" is determined by the placement of the electrodes that direct the current flow through the active layers. The next section presents the main configurations that have been used for the implementation of Gunn diodes. The purpose of this section is to point out the advantages and the disadvantages of each approach, as more details about the fabrication techniques can be found in chapters 4, 6 and 7.

The Gunn diode has been traditionally fabricated as a vertical device where the current flows perpendicular to the active layers. The general layer structure of the vertical Gunn diode is presented in Figure 2.25 where the channel layer is grown between the highly doped contact

layers. The conventional configuration of a Gunn diode oscillator incorporates the placement of the diode in a rectangular waveguide cavity, as illustrated in Figure 2.26 [47]. Thus, the part of the wafer that participates to the formation of the device needs to be removed from the wafer so that the lower contact layer becomes accessible. After removing the wafer under the active layers, the chip is mounted in the waveguide cavity to form the complete oscillator. The bottom cathode contact is placed on the heat sink that removes a significant amount of heat that is generated by the enormous current (~1A [3]). A back power short is used as a tuning medium for improving the impedance matching or for the fine adjustment of the oscillation frequency. The latter is mainly determined by the resonant cap which is placed on the top of the diode. The device is biased through the bias post which is usually a bias T that isolates the DC from the RF signal for the protection of the bias source. The generated signal is finally driven in the waveguide which delivers the signal to the antenna or to the next circuit component.

The above configuration provides high levels of generated power and very good thermal stability as a significant amount of heat is dissipated in the heat sink. In addition, the rectangular waveguide cavity transmits the signal with very low power losses. Despite these advantages, the realisation of the oscillator is very complicated, mainly due to the required isolation of the active device from the wafer. In addition, the Gunn diode cannot be integrated with other components on a MMIC. Since the complete oscillator is bulky, this solution is mainly used in automotive and radar applications.

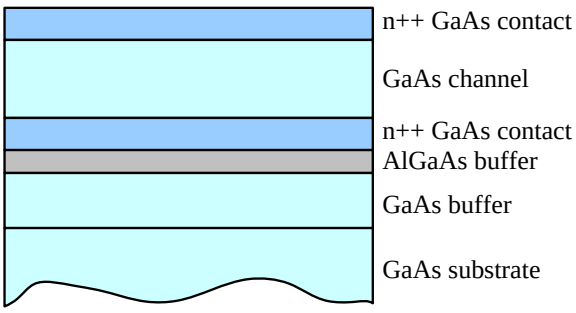


Figure 2.25 Layer structure of the conventional vertical Gunn diode.

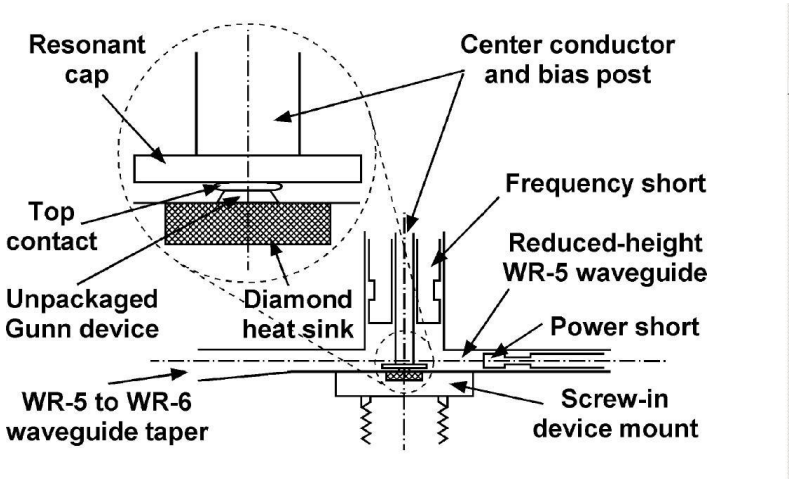
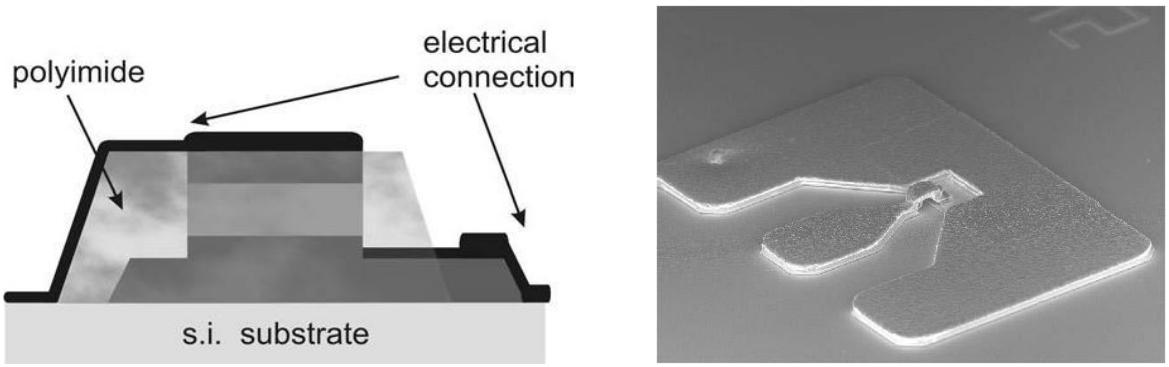


Figure 2.26 Schematic of oscillator with a vertical Gunn diode placed in a rectangular waveguide cavity [3].

A significant development of the vertical Gunn diode has been recently presented, where a similar layer structure has been used for the fabrication of MMIC-compatible oscillators [3, 8]. The general structure of the device is illustrated in Figure 2.27(a) where the bottom highly doped layer is accessed from the top surface of the chip. This configuration allows the deposition of coplanar waveguide (CPW) pads as illustrated in Figure 2.27(b), allowing the integration with other mm-wave components [3]. The main disadvantage of the current solution is the reduced flexibility regarding the choice of the oscillation frequency. Since the material growth is complete, the distance between the anode and the cathode is fixed and the oscillation frequency is characteristic for each wafer. Another drawback of this approach



(a) (b)

Figure 2.27 Schematic view of the MMIC-compatible vertical Gunn diode (a) [8] and SEM picture of the CPW configuration [3].

arises from the need for an air bridge interconnection which makes the fabrication procedure more complicated. A more detailed comparison between the various versions of the Gunn diode can be found in Chapter 5.

The first planar Gunn diodes oscillating at frequencies above 100 GHz were demonstrated by Khalid et al. [9] in 2007. In this version of the Gunn diode, current flows laterally, in the epitaxial layers. The basic layer structure of the device is illustrated in Figure 2.28 where an obvious similarity with the HEMT layer structure can be observed. Indeed, the design of the planar Gunn diode was inspired from the layer structure of the HEMT as Gunn instabilities had been previously reported on HEMT substrates [48, 49]. An additional feature of the Gunn diode structure is the extra GaAs/AlGaAs interface at the bottom side of the channel where the second δ-doping layer provides additional electrons in the channel. Thus, the charge density in the channel is sufficient for the formation of the Gunn domains. The formation of parallel channels has been used for the enhancement of the generated power of planar Gunn diodes, as described in Chapter 5.

The major novelty of the planar Gunn diode structure is the ability to determine the oscillation frequency through a lithographic process. The distance between the anode and the cathode can be defined with high accuracy through the deposition of the metallic electrodes. Thus, the same wafer can be used for the realisation of devices oscillating at various frequencies. Additionally, the fabrication procedure is significantly simplified in comparison with the fabrication of the vertical Gunn diodes. Initial results presented oscillations at 108 GHz [9]. The development of the vertical device in the subsequent years has been mainly focused on maximising the generated power.

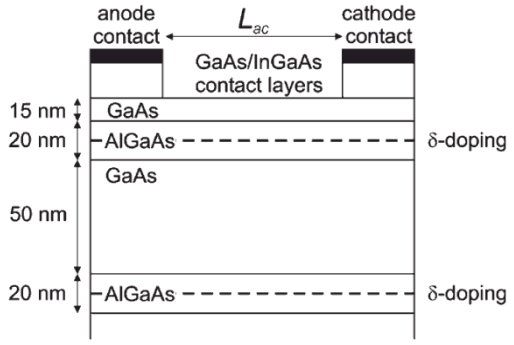


Figure 2.28 The layer structure of the first planar Gunn diode oscillating above 100 GHz [9].

2.7.4 Applications

Presenting excellent phase noise characteristics, the diodes are ideal for use as local oscillators for point-to-point telecommunications, motion detectors and telemetry systems. The compact size and the low voltage requirements, make the Gunn diode compatible for integration in mobile electronic devices. The growing interest for terahertz sources sets new targets for the performance of the device. Terahertz technology demonstrates important applications in security imaging, chemical and biological sensing and high-speed high-bandwidth telecommunications [2]. Thus, new challenges arise for the Gunn diode demanding oscillations in the terahertz frequency range (300 GHz - 3 THz) with high output power and improved DC-to-RF conversion efficiency.

2.8 Chapter summary

This chapter has presented the main principles of the semiconductor physics leading to the implementation of devices for mm-wave frequencies, such as the HEMT and the planar Gunn diode. The presentation of the physical properties and the high field phenomena of various materials aim to give a clear understanding of the requirements for the design of the material systems. Heterojunctions, which lead to the formation of energy barriers and quantum wells, have also been described in detail for the different interfaces between semiconductors and metals. In conclusion, a large number of factors that affect the performance of the devices at high frequencies has been presented in this chapter. Factors such as the carrier mobility, the contact resistance and the parasitic elements, strongly affect the performance of the devices as will be better demonstrated in the experimental chapters 6 and 7.

3. Passive components

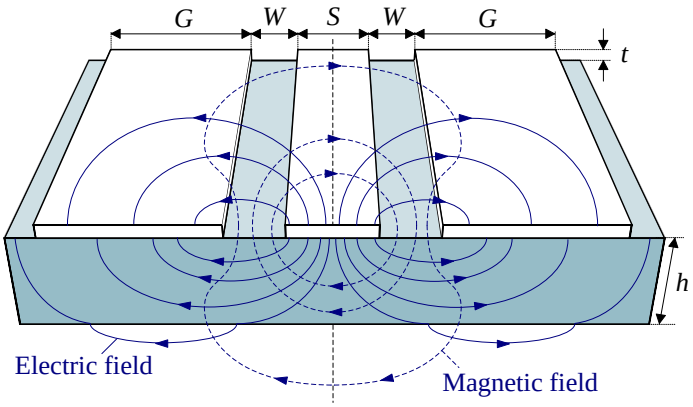
3.1 Introduction

In the previous chapter, the physical principles and the basic structures of the active components used in this project were presented. Passive components are equally significant elements for the realisation of complete MMICs. The low-loss signal delivery between the components and the biasing of the devices are some important requirements of the passive elements. It is critical that the fabrication technology used is compatible with the technology used for the active devices so that the complexity and the costs are kept relatively low. In this chapter, the MMIC-compatible passive elements used in this work are presented. Transmission lines in the CPW configuration have been used as connecting lines and for matching the different impedances of the individual elements. The biasing circuits consist of metal-insulator-metal capacitors and spiral inductors for DC and RF decoupling, respectively. Complementary components such as air bridges were used for the minimisation of the transmission losses through the coplanar waveguides. Air bridges also serve as interconnections between the centre and the outside area of the spiral inductors.

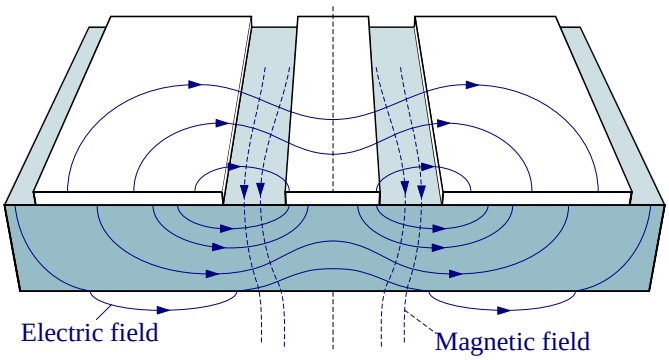
3.2 Coplanar waveguides

At low frequencies where the signal wavelength is significantly larger than the circuit dimensions, the connection between the various elements can be realised by using simple lumped elements. However, at microwave frequencies the signal wavelength becomes comparable to the length of the wire connections and the propagation effects can degrade the signal quality significantly. Some of the most important effects are the excessive increase of the wire impedance and the undesired radiation caused by circulating currents. Thus, the need for signal transferring in MMICs with relatively low losses led to the introduction of waveguide transmission lines. In addition, the structures need to be planar for the simplification of the fabrication procedure. The planar waveguides shall be implemented by simple lithographic procedures combined with the fabrication steps of the active devices. Thus, CPW lines were employed in this work, meeting the requirements described above.

The first CPWs were introduced by Wen in 1963 [50]. The waveguide structure consists of a centre signal strip and two parallel ground electrodes on a dielectric substrate. Figure 3.1 illustrates the basic structure of CPWs with finite dielectric thickness and metal planes with finite width *G*. The even and odd modes of propagation are presented in Figure 3.1(a) and Figure 3.1(b), respectively. In the even mode the electric field is symmetric to the centre of the structure and the magnetic field encloses the centre strip. The electric field lines start from the centre strip ending to the ground electrodes. In the odd propagation mode, the electric field lines start from the one ground plane ending to other, such that the two ground strips have opposite potentials. The even mode shows a very small variation of the effective dielectric constant and the characteristic line impedance over a wide frequency range [51]. The even mode also presents low dispersion characteristics and is preferred for the design of broadband MMICs.



(a)



(b)

Figure 3.1 The coplanar waveguide configuration with finite substrate thickness and finite width of the ground strips. The even mode of propagation is presented in (a) and the odd mode in (b).

For the calculation of the transmission parameters in closed form, the conformal mapping technique is applied where the structure is mapped to the equivalent parallel plate capacitors. Thus, the effective dielectric constant ε_{eff} and the characteristic line impedance Z_0 are given by [52]:

$$\varepsilon_{eff} = \frac{C_{CPW}}{C_{AIR}} \tag{3.1}$$

$$Z_0 = \frac{1}{c_0 C_{AIR} \sqrt{\varepsilon_{eff}}} \tag{3.2}$$

where C_{AIR} is the capacitance of the line after the replacement of the whole dielectric with air, c_0 the speed of light in free space and C_{CPW} the total capacitance of the line:

$$C_{CPW} = C_D + C_{AIR} \tag{3.3}$$

with C_D representing the capacitance caused by the dielectric substrate. The solutions given by using the conformal mapping technique are [3]:

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k_1)}{K(k_1')} \frac{K(k_0')}{K(k_0)} \tag{3.4}$$

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{eff}}} \frac{K(k_0')}{K(k_0)} \tag{3.5}$$

where ε_r is the dielectric constant of the substrate. The solutions of the complete elliptic integrals $K(k_n)$ are given in Appendix A by [51]. The extraction of the above equations is outside the scope of this work and more information can be found elsewhere [53].

CPW lines present significant advantages over the alternative configurations (mictrostrips, slotlines, coplanar strips). CPWs are very easy to realise by using one lithographic step, providing compatibility for integration with other planar structures. Due to their planar configuration, CPWs implement easily shunt or series connections with other components. Another advantage over microstrip lines is that no via-holes are needed for connecting with the ground, thereby simplifying the fabrication procedure significantly. In addition, a wide range of available characteristic impedances can be achieved by adjusting the geometry of the strips.

However, there are several drawbacks in the use of CPWs. In addition to the fundamental even mode of propagation, the fundamental odd mode can propagate at the same time if the two ground planes do not have the same potential. This disadvantage can be eliminated by using air-bridges that interconnect the ground planes periodically to equalise their potentials. Consequently, additional fabrication steps are required and the realisation of the complete structure becomes more complicated. More information about the air-bridges is given in the next section. In some applications, the large area that CPW lines cover can be an extra disadvantage. Even if the ground planes have finite width, the overall area is much larger in comparison with microstrip lines and this could be less cost effective when expensive substrates are used.

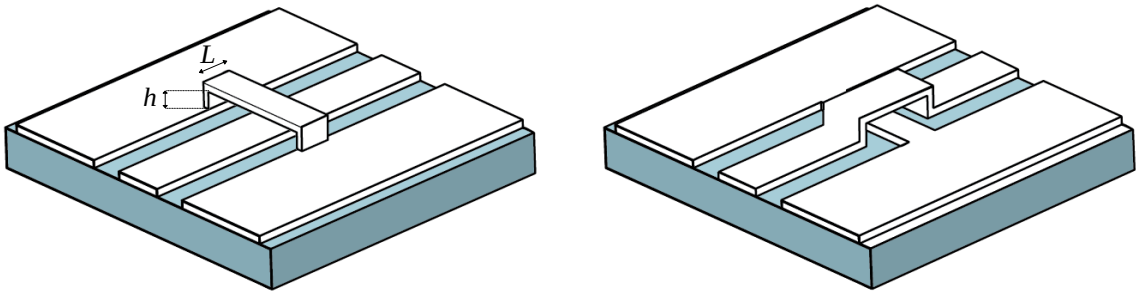
3.3 Air bridges

As described in the previous section, the two ground planes of CPWs need to be connected over the signal strip, so that their voltage is equalized. Therefore, the use of air bridges is critical for the elimination of transmission losses where the parasitic odd, or slot-line, mode of propagation needs to be suppressed [54]. Air bridges are extensively used in the fabrication of MMICs. Passive components like Wilkinson dividers have presented low return loss by using cross-overs [55]. Metal interconnections are also needed for the implementation of multi-finger transistors and inductors. Air bridges are also used for the connection of the top electrode in vertical active devices, such as the vertical version of the Gunn diode presented in Section 2.7.4. The air bridge technology is also used for the realisation of elevated CPWs that present low-loss passive elements for the frequency range 100 - 300 GHz [56].

There are two basic types of air bridges. In type A, the metal interconnection is realised by an overpass connecting the ground planes as shown in Figure 3.2(a). In type B, the overpass is used to connect the two edges of the centre signal strip while the ground planes are connected under the air bride (Figure 3.2(b)).

The characteristic impedance of the CPW line is strongly determined by the S and W dimensions of the structure as presented in Figure 3.1. It comes from the geometry of type B air bridges that the distance W varies significantly near the crossover section, causing a variation of Z_0. Air bridges of type A present a smaller non-uniformity of W near the crossover section. Therefore, air bridges of type A were used in this work, presenting less variation of Z_0 [54]. One significant drawback of the interconnections is caused by the introduction of additional capacitance between the signal strip and the ground. This will also

lead to a variation of the characteristic impedance of the line. Therefore, the length *L* of the air bridge needs to be kept small and the structure needs to be sufficiently high. Also, the total number of the air bridges should be kept as small as possible [54, 57].



(a) (b)

Figure 3.2 Type A (a) and type B (b) air bridge configurations.

Another significant requirement that the incorporated air bridge fabrication technology should meet, is the ability to accurately place the posts. Figure 3.3 [51] illustrates the current density distribution in the cross section of a CPW, where the majority of the charge is concentrated at the edges of the strips. Thus, it is more efficient to place the air bridges as close as possible to the edges of the ground planes for the equalisation of their potential.

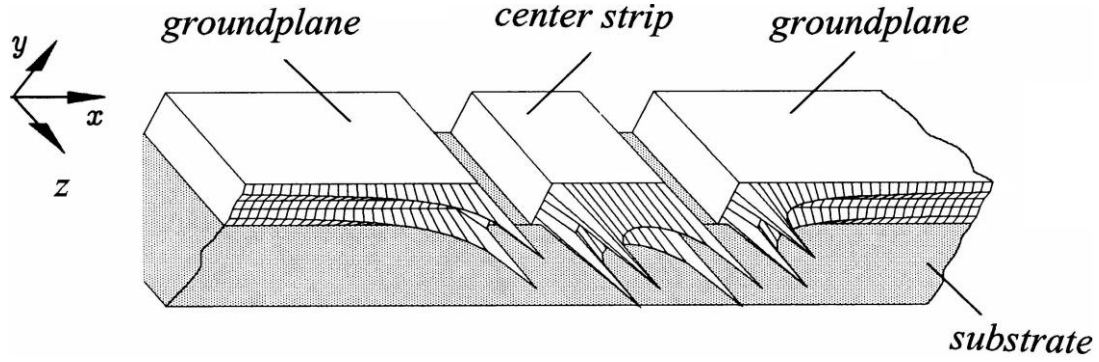


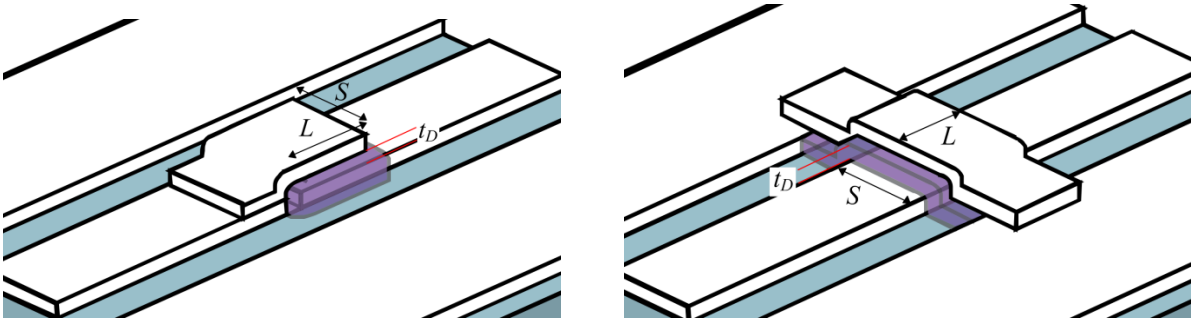
Figure 3.3 The surface current density distribution in the cross section of a symmetrical coplanar waveguide with finite metallization thickness [51].

3.4 Metal-insulator-metal capacitors

Capacitors are fundamental circuit elements used for the realisation of impedance matching and for RF coupling. The basic structure of a metal-insulator-metal (MIM) capacitor consists of a dielectric layer sandwiched between the two electrodes. This configuration can be implemented easily by the CPW transmission lines, either in series or in shunt connection as depicted in figures 3.4(a) and 3.4(b), respectively. In the series connection, the two parallel metal plates usually have the same width so that the characteristic impedance is not affected. The dielectric film is slightly wider in order to prevent short circuit connections between the two electrodes. The thickness of the dielectric layer is usually low for the production of high capacitance using a small area on the substrate. Therefore, no air bridge components are needed for the connection of the top electrode as the metallic strips are significantly thicker then the dielectric layer. The well known equation for the calculation of the capacitance, ignoring the fringe effects, is:

$$C = \frac{\varepsilon_0 \varepsilon_D S\ L}{t_D} \tag{3.6}$$

where ε_D the relative dielectric constant and S, L, t_D the geometric characteristics of the capacitor as depicted in Figure 3.4. Silicon nitride (Si_3N_4), silicon dioxide (SiO_2) and polyimide are some of the dielectrics used for the realisation of MIM capacitors. Si_3N_4 provides high values of capacitance due to the high relative dielectric constant (6-8 depending on the stoichiometry) The deposition of the dielectric film can be used at the same time for the protection of the active devices since Si_3N_4 forms an excellent passivation layer.



(a) (b)

Figure 3.4 The MIM capacitor in series (a) and shunt (b) configurations.

The general equivalent circuit of the MIM capacitor is presented in Figure 3.5 [58]. The series element *C* represents the capacitance of the parallel plates and the components C_1 and C_2 stand for the parasitic capacitance with the ground plane. For the elimination of the shunt capacitances the extension of the dielectric film with respect to the parallel electrodes has to be kept as small as possible. The parasitic *L* and *R* elements represent the mutual inductance between the plates and the dielectric losses, respectively. Both increase proportionally with the thickness of the dielectric.

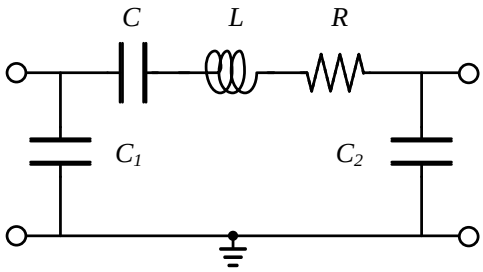


Figure 3.5 The equivalent circuit of the MIM capacitor [58].

Interdigital capacitors are an alternative solution for the implementation of MMIC-compatible couplers. The fabrication of interdigital capacitors can be considerably simpler than the MIM capacitors, as only one lithographic step is required. However, only very small capacitance values can be achieved (hundreds of fF) for relatively large elements with increased parasitic effects. Compact MIM capacitors present tens of pF with smaller parasitic elements [59] and are therefore more desirable for use in this work. More information about monolithic capacitors can be found in [58].

The capacitors and inductors used in this project served as biasing elements, thus no detailed modelling of the fabricated components was performed in this work. The basic requirement of the biasing components is to provide a sufficient ability of RF coupling and decoupling using small integration areas. Considering all the above, Si_3N_4 MIM capacitors were used in this project for the RF connection of the individual elements.

3.5 Spiral inductors

Spiral inductors present high inductivity in small integration areas in comparison with alternative solutions like meander or loop inductors. In contrast with meander inductors, the current flows towards the same direction increasing the mutual inductance of the parallel lines presenting up to few nH. The fabrication technology requires the implementation of air

bridges for the interconnection of the centre of the spiral to the outside access pad. The configuration of a 2.5 turn spiral inductor is presented in Figure 3.6 where the component is mounted on CPW feed lines.

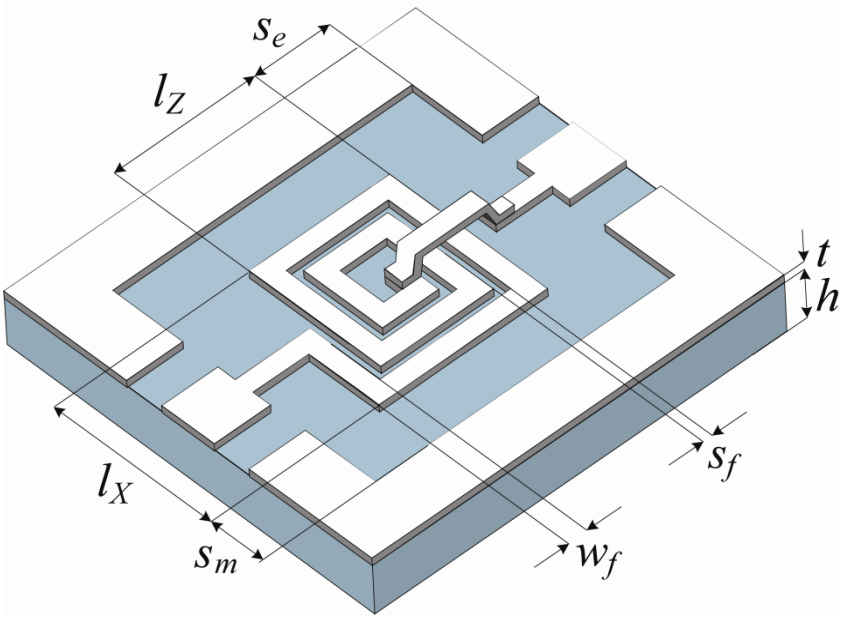


Figure 3.6 Spiral inductor connected with CPW feed lines.

The generalised equivalent circuit of the spiral inductor is depicted in Figure 3.7 [60]. The inductance of the coil is represented by L the series resistance of the line is represented by R_S. The parallel capacitance C_3 is caused by the parasitic coupling between the parallel lines. The shunt elements C_1 and C_2 represent the capacitance between the coil and the ground planes. The maximum feasible inductance is limited by several factors. For the achievement of high inductivity, more turns are required resulting the increase of the total line length. As a consequence, the series resistance R_S increases simultaneously with the line length as well as the parasitic coupling between the lines. In addition, the inductor is limited to operate at frequencies where the total length is smaller than the quarter of the signal wavelength where the line acts as a resonator. The tradeoffs between different design approaches on a GaAs substrate are summarized in Table 3.1 [59]. A general formula for the calculation of the inductance is given by [60]:

$$L(\text{nH}) = 0.03937 \frac{a^2 n^2}{8a + 11c} \left[1 + 0.333 \left(1 + \frac{s_f}{w_f} \right) \right] \tag{3.7}$$

$$a = \frac{D_o + D_i}{4} \tag{3.8}$$

$$c = \frac{D_o - D_i}{2} \tag{3.9}$$

where D_o and D_i are the outer and the inner dimensions of the spiral, respectively.

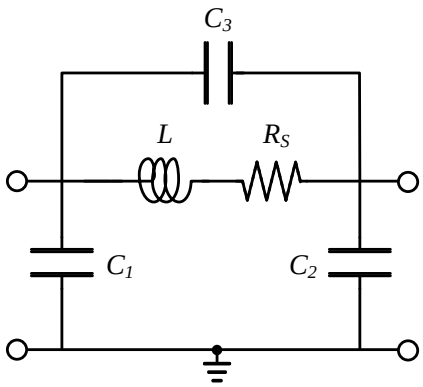


Figure 3.7 The equivalent circuit of the spiral inductor [60].

	Inductor No.		
Parameter	1	2	3
Turn number, N	2.5	3.5	4.5
Turn width, w_f (μm)	25	25	25
Gap width, s_f (μm)	5	5	5
Size length, $l_X = l_Z$ (μm)	185	240	300
Distance to ground, s_m (μm)	50	50	50
Distance to ground, s_c (μm)	50	50	50
Length of winding, l_{strip} (μm)	1.245	2.055	3.155
Self-inductance, L (nH)	0.701	1.455	2.813
Parallel capacitance C_1 (fF)	41.97	60.72	81.34
Parallel capacitance C_2 (fF)	19.03	23.36	29.65
Coupling capacitance C_3 (fF)	21.38	22.16	32.67
Ohmic resistor, R_f (1 GHz) (Ω)	0.334	0.563	0.838
dc resistor, R_{dc} (Ω)	0.434	0.716	1.10
λ/4-frequency, f(λ/4) (GHz)	30	18	11

Table 3.1 Different design approaches for the implementation of spiral inductors on a GaAs substrate (ε_r = 12.9, t = 3 μm, h = 400 μm) [59].

3.6 Matching networks

Matching networks are fundamental circuits in RF system design for the maximisation of the power transfer between nodes with different impedances. For the design of microwave matching networks, the use of transmission lines is much more convenient than using lumped elements such as capacitors and inductors. The modelling of lumped elements becomes a very challenging task at high frequencies. The design of transmission line matching networks using the Smith chart is described in this section.

Figure 3.8 presents a lossless CPW with characteristic impedance Z_0, terminated with a load Z_L. The ratio of the reflected to the incident voltage amplitude is given by the reflection coefficient Γ:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} = \frac{z-1}{z+1} \tag{3.10}$$

where z is the normalised impedance:

$$z = \frac{Z_L}{Z_0} = \frac{R + jX}{Z_0} = r + jx \tag{3.11}$$

The Smith chart performs the mapping of the x-r orthogonal system of coordinates to the U-V system as presented in Figure 3.9 The analytical expressions for the transformation from the r-x to the U-V system are given in Appendix A. It should be noted that the following calculations are valid under the assumption that the transmission lines are lossless. The input impedance of the circuit presented in Figure 3.8 is given by Equation 3.12 [61].

$$Z_{IN} = Z_0 \frac{Z_L + jZ_0 tan\beta l}{Z_0 + jZ_L tan\beta l} \tag{3.12}$$

Here, l is the length of the transmission line and β the propagation constant given by:

$$\beta = \frac{2\pi}{\lambda} \tag{3.13}$$

The wavelength λ of a complete sinusoidal wave for a frequency f is easily calculated by:

$$\lambda = \frac{v_P}{f} \tag{3.14}$$

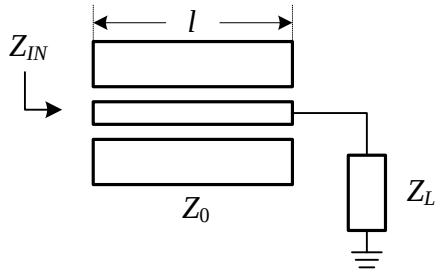


Figure 3.8 A CPW line terminated with load Z_L.

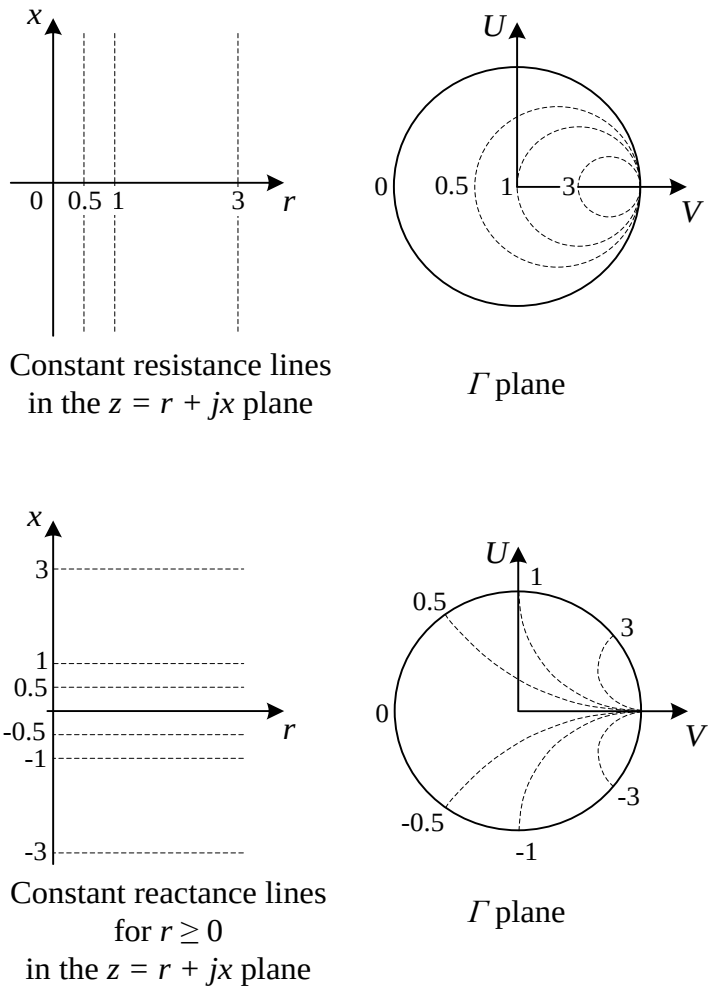


Figure 3.9 The development of the Smith chart [62].

The phase velocity v_p represents the velocity of propagation of the signal which depends on the effective dielectric constant as given in the following equation [52]:

$$v_P = \frac{c_0}{\sqrt{\varepsilon_{eff}}} \tag{3.15}$$

As presented in Section 3.2 the effective dielectric constant for CPW lines depends on properties of the dielectric substrate and the geometric characteristics of the strips. The above equations are universal and can be applied in any version of transmission line after calculating the respective ε_{eff} .

For the analysis of the matching procedure, the impedance and the admittance of some basic configurations are calculated in the next lines. Figure 3.10 demonstrates three basic termination solutions of transmission lines. For the short circuit and the open circuit termination of the transmission line, Equation 3.12 gives:

$$Z_{SC} = jZ_0 \tan\beta l \tag{3.16}$$

$$Z_{OC} = -jZ_0 \cot\beta l \tag{3.17}$$

In the case that the length of the transmission line is equal to the quarter of the wavelength and the line is terminated with Z_L, the input impedance resulting from Equation 3.9 is:

$$Z_{IN(\lambda/4)} = \frac{Z_0^{\,2}}{Z_L} \tag{3.18}$$

Equation 3.18 demonstrates a commonly used matching method, where the characteristic line impedance Z_0 is mainly chosen in order to match real impedances.

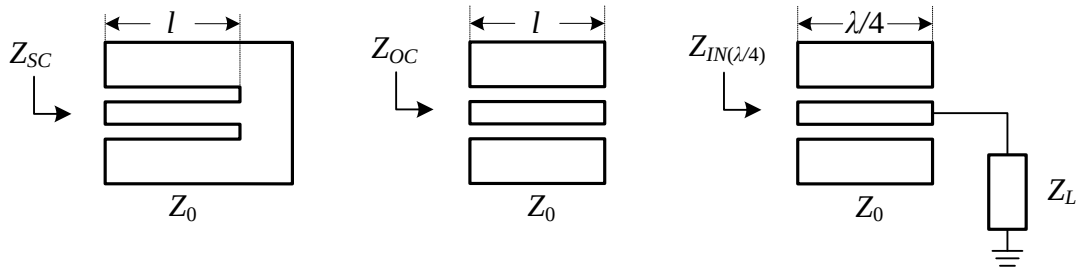


Figure 3.10 Basic termination configurations of the transmission line.

In the next section, two different approaches are presented for impedance matching, demonstrating the combination of series and shunt transmission lines. Both of them perform the matching between a theoretical impedance with $Z = (100 + j50)\ \Omega$ and a 50 Ω load. In this example, the normalised admittance Smith chart is used which results from the normalised impedance chart after a 180^o clockwise turn.

The L matching approach is illustrated in Figure 3.11(a). A short circuited line with length l_1 is connected in parallel with the 50 Ω load. The normalised admittance added to the load is $y_1 = 1 / (Z_{SC1} / Z_0)$. After replacing Z_{SC1} with Equation 3.16 for $l = l_1$ the added admittance becomes: $y_1 = -j\cot\beta l_1$. Since no real part is added to the load, the admittance is transformed as presented in the Smith chart of Figure 3.11(a). Thus, a shift is performed from the point A to the point B along the circle with the equal normalised real admittance $y = -1$. The line l_1 can be found from the readings of the Smith chart which provide the length as a fraction of the wavelength (green lines). Thus, the length of l_1 is equal to 0.125 λ. As a reminder, the wavelength in the transmission line can be calculated from Equation 3.14. At

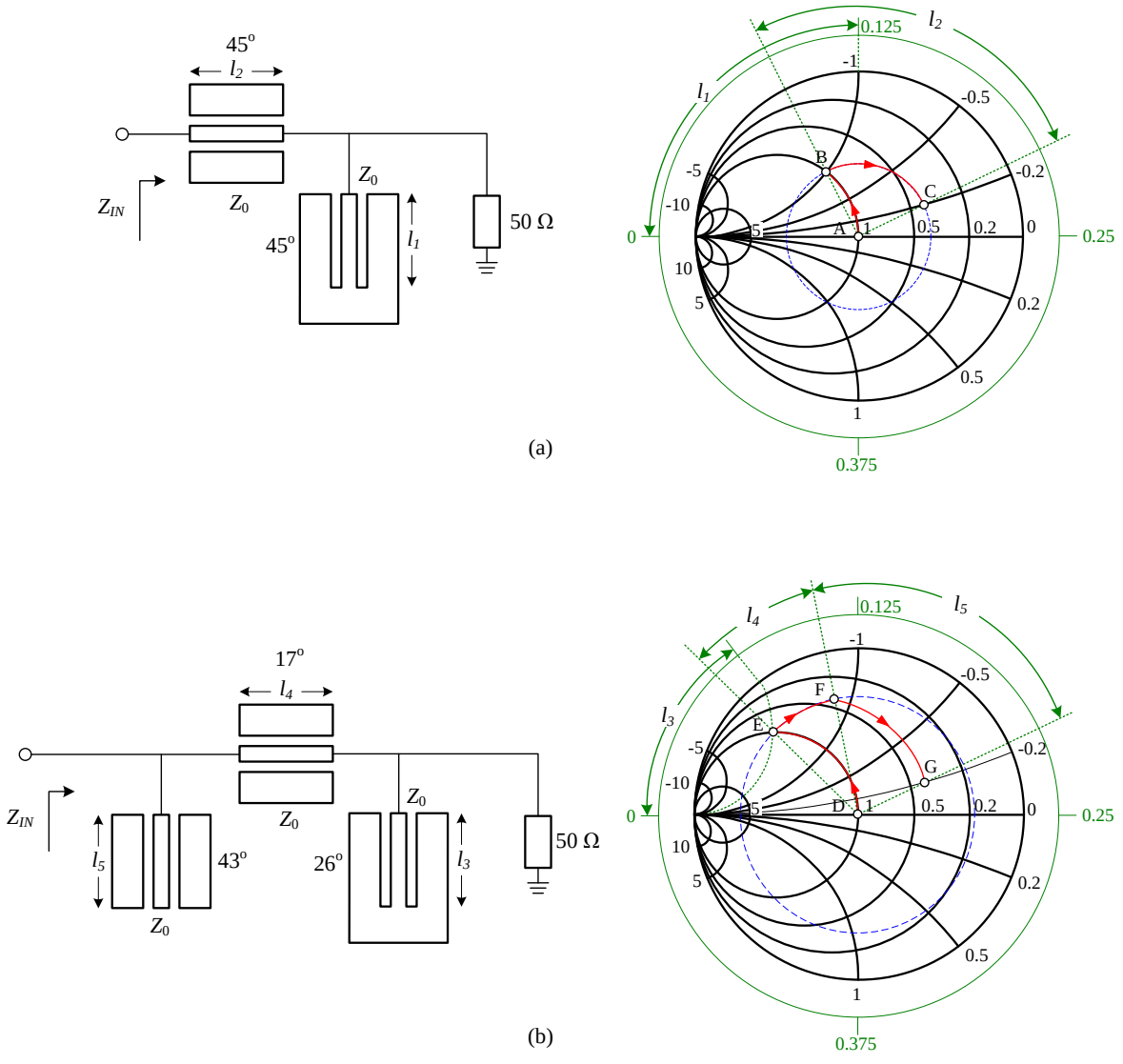


Figure 3.11 The L (a) and the Pi (b) matching network approaches.

the point B the admittance has transformed to 1-*j*. After the shunt short-circuited line, a series line with length l_2 is added to the circuit. The admittance shift is performed along the equal-Γ circle (blue dashed line) which is concentric with the Smith chart, from the point B to the point C. After reading the length generator of the admittance chart, the length l_2 is also equal to $0.125\,\lambda$ which corresponds to a phase shift equal to $\theta_2 = 45^{o}$. With the placement of the series line the matching from the point A (50 Ω) to the point C ($Z = 100 + j50$ Ω) is complete.

The matching between the same impedances after transforming the L to a Pi matching network is analysed in the following lines. For the realisation of the Pi matching network, an extra open circuited shunt line has been added as presented in Figure 3.11(b). In this example, the length l_3 of the short-circuited stub gives a shift of 26^{o} from point D to point E. The series stub with length l_4 gives a shift of 17^{o} along the equal-Γ circle from point E to point F. Finally, the additional open circuited line which is connected in parallel, adds a positive imaginary admittance equal to $j\tan\beta l_5$ (from Equation 3.17 with $y = Z_0 / Z_{OC}$). The open circuited line introduces a shift of 43^{o} to match point F with point G.

The above examples demonstrate that more than one solution exists for the realisation of the impedance matching. The matching procedure can be summarized as:

- Lines connected in series perform a clockwise turn along the equal-Γ circles.
- Short circuited lines connected in parallel perform an anti-clockwise turn, keep the real parts constant and add negative imaginary parts to the admittance.
- Open circuited lines connected in parallel perform a clockwise turn, keep the real parts constant and add positive imaginary parts to the admittance.

This method provides sufficient accuracy for the majority of the applications, assuming that the transmission lines are lossless. Since the signal wavelength varies for different frequencies, the calculations for the dimensions of the lines are valid for a specific frequency. Therefore, a matching network presents a frequency response similar to a resonant circuit. The loaded quality factor Q_L of a resonator is given by [62]:

$$Q_L = \frac{f_0}{BW} \tag{3.19}$$

where f_0 is the central frequency and BW the -3dB frequency pass-band. For L matching networks, the quality factor for an equivalent series input impedance $R_S + jX_S$, is given by the circuit node Q_n [62]:

$$Q_n = \frac{|Xs|}{Rs} \tag{3.20}$$

For the equivalent parallel admittance $G_P + jB_P$ the circuit node is equal to [62]:

$$Q_n = \frac{|B_P|}{G_P} \tag{3.21}$$

It arises that the relation between the loaded Q_L and the circuit node Q_n for an L matching network, is given by [62]:

$$Q_L = \frac{Q_n}{2} \tag{3.22}$$

For the example of the Pi matching network, the calculation of the the loaded Q_L becomes more complicated. In general the quality factor of Pi matching networks is proportional to the highest circuit node Q_n. The highest Q_n of the L network coming from the node B of Figure 3.11 is equal to 1 where for the Pi network the F node gives a Q_n of 2.84. Figure 3.12 presents the frequency response of the matching networks analysed above. The higher node of the Pi network is translated to a narrower bandwidth in comparison with the broad band response of the L network. In conclusion, simple or more complicated matching networks are chosen depending on the requirements of the application, such as the desirable bandwidth, the integration area, the fabrication tolerances etc.

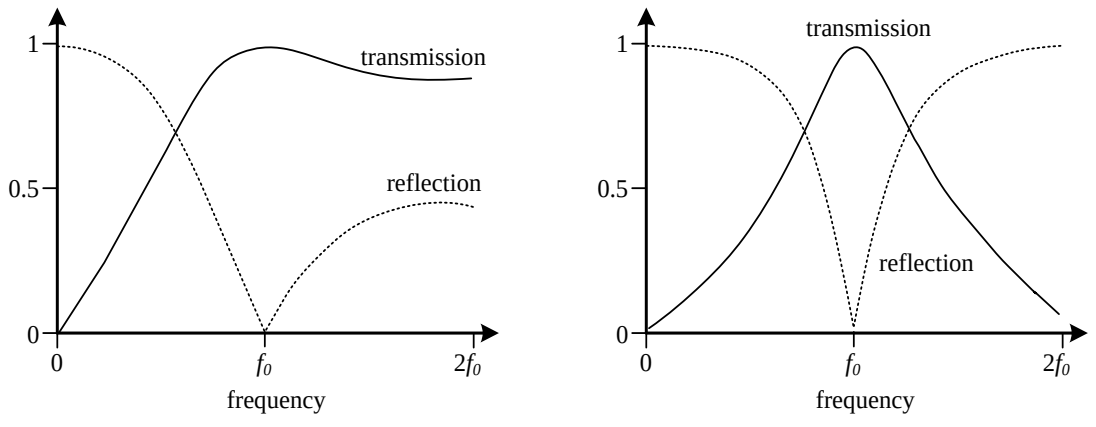


Figure 3.12 The frequency response of the L (a) and the Pi (b) matching networks of Figure 3.11.

The transmission line matching networks are often implemented using symmetrical balanced stubs on both sides. The pair of lines must present the same admittance as the single line that they replace. Thus, the individual admittance is the half of the initial one. It should be noted that the length of the stubs is not equal to half of the single lines. The length of the balanced lines has to be calculated from equations 3.16 and 3.17 in order to present the half values of the initial admittances. The balanced version of the Pi matching network of Figure 3.11(b) is presented in Figure 3.13.

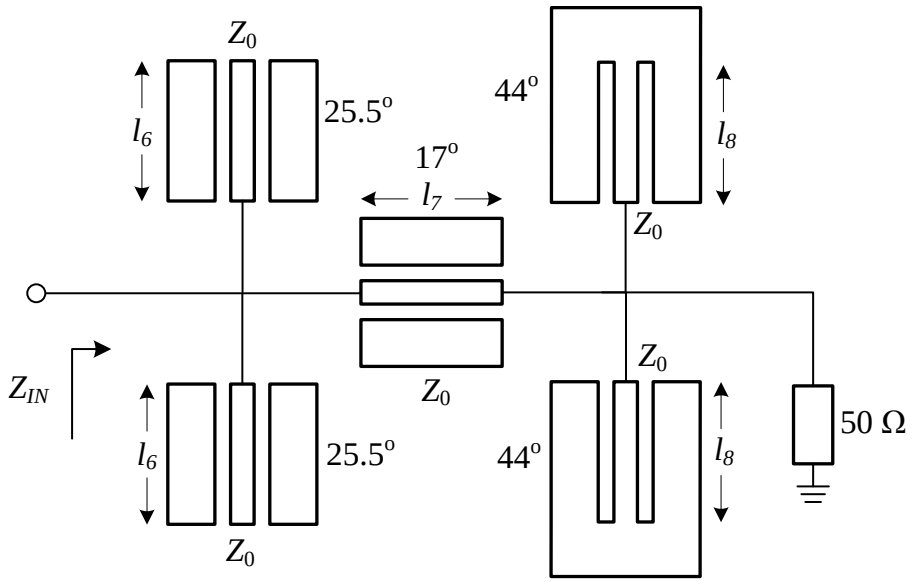


Figure 3.13 The balanced version of the Pi matching network of Figure 3.11(b).

3.7 Chapter summary

This chapter has presented the individual passive elements that were used for the realisation of the MMICs in this project. Transmission lines in CPW configuration present a low-loss interface between the different elements of the circuits. The CPW lines are also used for the performance of the impedance matching between the different nodes of the circuits. The design aspects of the lumped elements implemented in this work, such as the MIM capacitors and the spiral inductors, have also been presented in the relative sections. The design of spiral inductors arises very challenging as frequency increases, thus inductors shall only be used as compact RF blocks for biasing purposes. Air bridges are required for the suppression of the parasitic modes of propagation in the CPW lines, as well as the interconnections required for

the spiral inductors. The design procedure and the fabrication techniques for the implementation of the complete MMICs are presented in detail in the next chapters.

4. Fabrication & characterisation

4.1 Fabrication

The fabrication process is one of the most significant factors affecting the performance of the devices. The techniques that are followed need to be reliable and repeatable, providing high-performance and high-yield components. The fabrication techniques used in this work are presented in the next sections. Following the bulk substrate material growth, the active semiconductor layers were grown using molecular beam epitaxy (MBE). Regarding the pattern definition, Electron Beam Lithography (EBL) has been used for the definition of the very small features of the diodes and the HEMTs as well as for the larger patterns. The metallization and the lift-off procedures for the formation of the metallic pads are shown afterwards. The dry and the wet etch processes are also presented in this chapter, describing the advantages and the disadvantages of each approach.

4.1.1 Material growth

The substrate material that is the base for the active layers is grown following the Liquid Encapsulated Czochralski method (LEC). A heated crucible contains melted GaAs where the temperature is controlled to be close to the liquid-solid transition and a crystal "seed" is placed on top of the melt as a starting material. The GaAs crystal grows at the melt-crystal interface and an ingot is created as the crystal is pulled away from the melt under rotation. When growth is completed, the ingot gets sliced to wafers which are polished and prepared for the next step which is the epitaxy of the active layers [63].

The active layers are formed afterwards on top of the substrate, which plays the role of the seed for the crystal structure. The dislocation density of these layers is much smaller than that of the substrate. Therefore, a relatively thick buffer has to be grown initially to prevent the propagation of the substrate defects to the active layers. One of the most common epitaxial methods is molecular beam epitaxy (MBE), which provides high flexibility in the placement of the semiconductor layers and the dopants. MBE involves equipment that directs beams of atoms or molecules to the heated substrate inside an ultra-high vacuum (~10^{-8} Pa) chamber. This technique ensures a very high control of the growth process regarding the composition

of the compounds, the doping levels and the precision of the layer thickness. Layers in the order of the atomic scale are feasible by MBE [64]. For the above reasons, this technique was used in this work. All the wafers used in this work were grown using MBE.

4.1.2 Lithography

After the growth of the material, the process of lithography is involved in the majority of the fabrication steps. Lithography is the technique for transferring the designed patterns on the sample material, so that only particular areas undergo further process like metallisation, dielectric deposition, etching etc. A liquid material is used for the coating of the sample surface which turns to solid after baking. The material is called resist because it is sensitive to radiation exposure that changes its properties. The exposed areas of positive resists become more soluble to developing solutions (wet etching of desirable area) and vice versa for negative resists. The two most commonly used techniques are photolithography and electron-beam lithography (EBL).

Several factors determine the choice of the suitable procedure for a fabrication process. Resolution is one of the most significant, referred to the minimum feature size that can be achieved by lithography. The registration capability of the technique is also very important, giving a measure of the alignment accuracy between different lithographic layers. The productivity of the technique is represented by throughput which is considered more in industrial fabrication than in research. The thickness of the resists and their resistance to the etching processing should also be taken into account when choosing the most suitable lithographic technique. It is worth mentioning that more than one technique can be combined during a complete fabrication procedure, taking the advantages that each technique can provide.

The process of photolithography involves resists (photoresists) that are sensitive when exposed to ultraviolet (UV) light with wavelength equal to few hundreds of nanometres ($\lambda \approx$ 200-400 nm). Initially, a replica of the designed pattern is transferred to a chrome layer on a quartz plate, known as mask. Then, the mask is placed between the light source and the sample and the transparent windows allow the exposure of the photoresist in the same fashion with the designed features. This exposure causes the change of the chemical structure of the positive photoresists, and the areas that absorb radiation become soluble to the developing solution. The negative photoresists are mainly polymers with a photosensitive ingredient. The absorption of the radiation energy form the photosensitive ingredient causes the creation of

cross linking to the molecules of the polymer. Thus, the exposed areas have a higher molecular weight, being insoluble by the developer.

Photolithography achieves pattern definition with low cost, high throughput and simplicity. For the above reasons, it is the most widely used technique in the semiconductor industry. The major disadvantage of the basic photolithographic process is the relatively low resolution which is determined by the wavelength of light. Radiation with wavelength smaller than 200 nm gets significantly absorbed by the quartz plate and the air. Additionally, the diffraction effects caused by the mask windows lead to the distortion of the pattern that is transferred to the photoresist plane. For the minimisation of these effects, the mask should be in contact with the sample. In this case, any dust particles will be transferred to the photoresist causing, at the same time, physical damage to the mask after contacting the sample. For the elimination of these problems, the mask can be kept in a sufficient distance above the wafer. However, this method magnifies the distortion at the transferred pattern as the diffracted light travels a longer distance between the mask window and the photoresist plane.

Modern photolithography introduces new techniques for shrinking the size of the components. Resolution enhancement techniques (RETs) involve optical proximity correction, phase-shifting masks and modified illumination, achieving minimum features of less than 25 nm for the commonly used 193 nm light source [65]. Immersion lithography reduces the effective wavelength that reaches the photoresist, by introducing a liquid of high refractive index which replaces the air over the wafer [66]. Another technique of high-interest is the extreme ultraviolet (EUV) photolithography which uses light with 13.4 nm wavelength, providing feature sizes in the order of tens of nanometres. The very small wavelength requires the replacement of the transmitting optics by reflecting optics in a vacuum environment [67]. Although the above methods of optimisation have boosted the available resolution, photolithography is no longer a simple and cheap technique. The advanced equipment is by far more expensive and more complicated. Nevertheless, most of the above developments are applied in industry, because of the very high throughput that photolithography can provide. A simpler solution has also been presented, which does not require the modification of the traditional equipment. This fabrication process includes the reflow of the photoresist after development for the formation of narrower gaps. This technique has recently demonstrated the fabrication of 350 nm T-gates where the opened window has an initial length of 1 μm [68].

Regarding the fabrication of MMICs, photolithography is an ideal solution for the definition of the large patterns. The CPW lines, the mesa areas and the contact areas of the devices that do not require high resolution lithography, can be fabricated quickly using photolithography. Unfortunately, photolithography requires a well-established fabrication process where the same masks are used many times for the various samples. This was not possible in this work, as new techniques had to be explored demanding the continuous modification of the pattern layout.

During the EBL process a beam of electrons is sent directly to the substrate, scanning the areas that the patterns are to be written. The orientation of the beam is controlled by the software which is responsible for the translation of the designed layout to the appropriate signals in the machine. Thus, the minimum feature size that can be achieved is mostly dependent on the quality of the resist and the scattering effects, as explained latter. State of the art results have demonstrated the fabrication of sub-10 nm nanowires on silicon [69] and 3 nm-gap nanoelectrodes [70]. However, EBL is a time-consuming technique, as all the areas are not exposed in one run like in photolithography. The scanning that reproduces the designed shapes can take many hours or even days for a large wafer.

Nevertheless, the samples used in this work were relatively small as well as the areas of the various patterns. In addition, the most important requirements in this work were the ability of defining sub-100 nm T-gates and the flexibility of frequently changing the designed patterns. For these reasons, EBL was chosen exclusively for the pattern definition.

Electron beam lithography

The optical system of the EBL tool ensures that a beam with the right energy and spot size reproduces precisely the designed layout. Figure 4.1 illustrates the general structure of the column optics inside the vectorbeam by Vistec Microsystems [71]. The source providing the electrons for the formation of the electron beam is a heated tungsten cathode, coated with zirconium oxide. The electrons are emitted only by the cathode tip, limited by the suppressor electrode. A high electric field is created between the cathode and the extractor exciting the cathode electrons to higher energy levels. The accelerated electrons finally exit the gun, where a last electrode focuses the beam below the anode.

Two sets of deflection coils perform the tilting and shifting for the alignment of the electron beam with the optical axis of the system. The electrostatic lens C1 and the magnetic lens C2,

form a lens system ensuring that the focus point and the current density are kept constant when the beam exits the lens C2. The blanking cell controls the “on” and “off” state of the beam. Thus, when the “off” state is desired, the beam diverges from the optical axis and does not reach the substrate. The dose that the resist is exposed is determined by the current density and the exposure time. In this way, the blanking cell adjusts the correct dose that is assigned to the resist. The final lens of the column is the magnetic lens C3 which is responsible for the focus of the beam on the substrate.

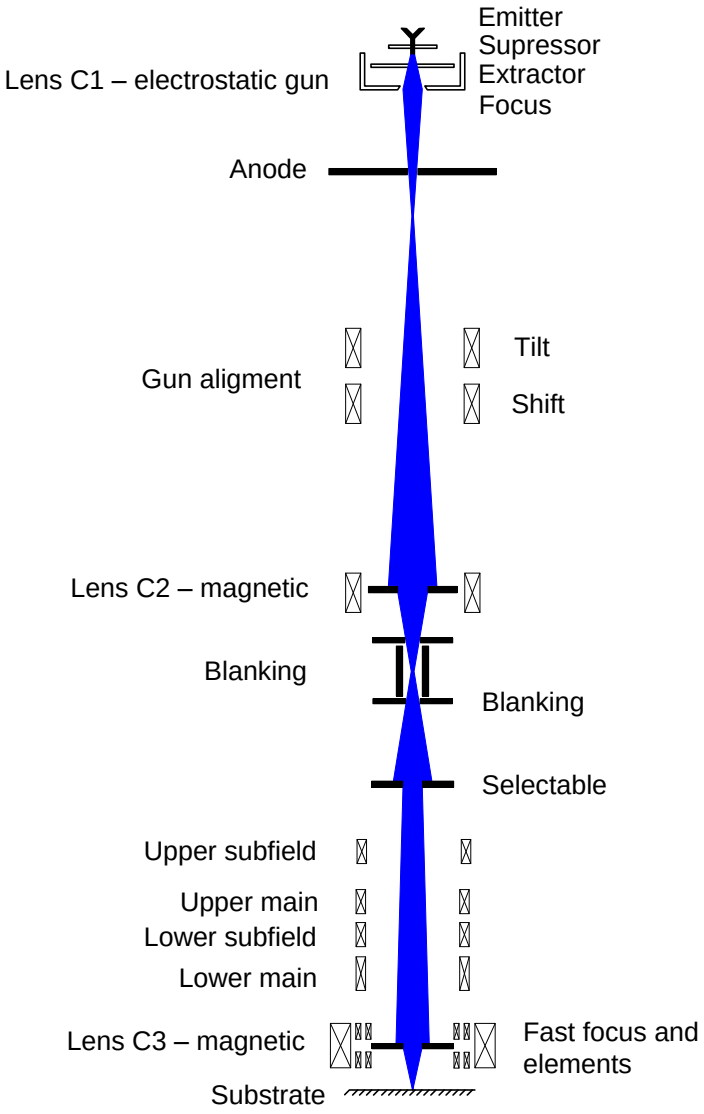


Figure 4.1 Ultra high resolution (UHR) column optics [71].

The EBL technique uses two general addressing methods for moving the beam over the substrate and locating the areas that are to be exposed. The size of the substrate is bigger than the distance between this and the final lens. Therefore, the electron beam has to be steered in very big angles to scan the total area. However, this would result a large spot without uniformity. For this reason, the layout pattern is initially split in main fields. The beam is placed at the centre of each field by movements of the stage that holds the substrate. This general addressing cannot be used for the definition of the patterns because the control of the stage is limited by the mechanical errors of the stage. Thus, the fracturing software divides the main fields to 64x64 subfields and the beam is located at the centre of each subfield, steered by the main deflector coils. Finally, the subfield deflector coils direct the beam scanning the total area of the subfield. Similarly, the main deflectors steer the beam to the centre of the next subfield to be written.

The electron beam is steered to scan the area where the pattern needs to be transferred as depicted in Figure 4.2. After the exposure of one area by a certain electron dose, the beam moves to the next area. The distance between the centres of the two areas is given by the product of the variable resolution unit (VRU) and the resolution. This distance is usually kept smaller than the spot size to ensure a continuous exposure of the total area.

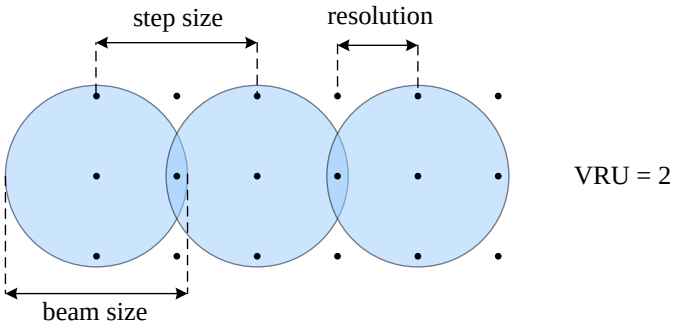


Figure 4.2 Pattern writing by stepping the spot. The beam step size is equal to VRU x resolution.

Scattering

The electron beam after inserting the resist layer undergoes various scattering effects that degrade the resolution limit. Initially, electrons diverge from their initial direction as a result of their interactions with the resist molecules. This effect, which is known as forward scattering, causes the randomisation of the electron velocities. As a result, the beam size of the penetrating electrons gets wider following a Gaussian profile [72].

A secondary scattering effect occurs when the electrons reach the substrate. Most of them penetrate it in various depths and some electrons are scattered back to the resist re-exposing it. Thus, the effect is known as backscattering and the Gaussian profile of the current exposure is much broader than the one caused by forward scattering. Finally, the profile of the exposed resist is formed by the two accumulating mechanisms.

The effect of the above effects to the resist profile is strongly dependent on the acceleration voltage that is applied by the vectorbeam. High energy electrons are subject to less scattering and the beam is narrower. The penetration profiles of electrons accelerated at 50 kV and 500 kV are illustrated in Figure 4.3 [72]. For 50 kV the exposure profile is significantly wider and a considerable amount of electrons are backscattered to the resist (yellow layer). The importance of the resist thickness is also pointed in this figure. Electrons lose less energy while penetrating a thinner resist layer and the beam size is expected to get less affected by the scattering effects.

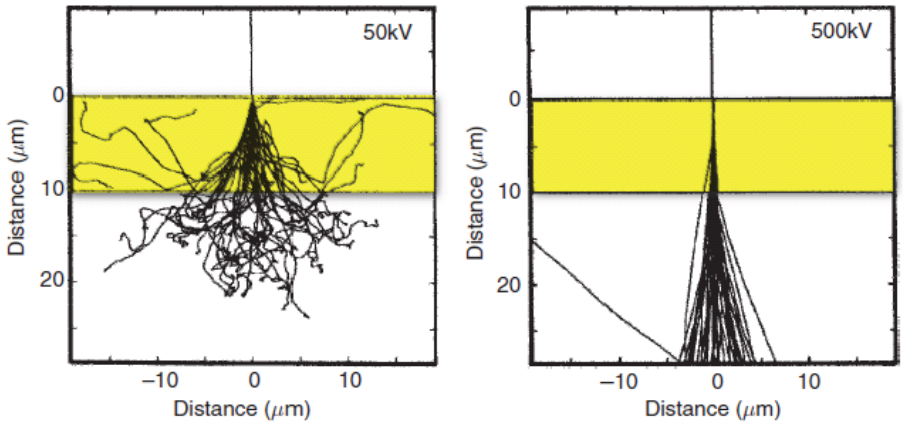


Figure 4.3 Electron trajectories for different acceleration voltages [72]. The yellow area indicates the resist layer and the white area bellow indicates the substrate.

The Gaussian profile of the electron beam introduces an additional effect which is known as the proximity effect. Figure 4.4 presents the accumulation mechanism of the electron dose after scanning a pattern area with 6 spot steps. Since the individual exposures form a Gaussian profile, the resulted dose accumulation results from the contribution of every spot around the exposed region. Thus, higher electron doses are assigned to the middle of the pattern from the contribution of the surrounding exposures. On the contrary, the total dose is

reduced around the edge areas. The distortion caused by the proximity effect is depicted in Figure 4.5 which illustrates the top view of some exposed patterns.

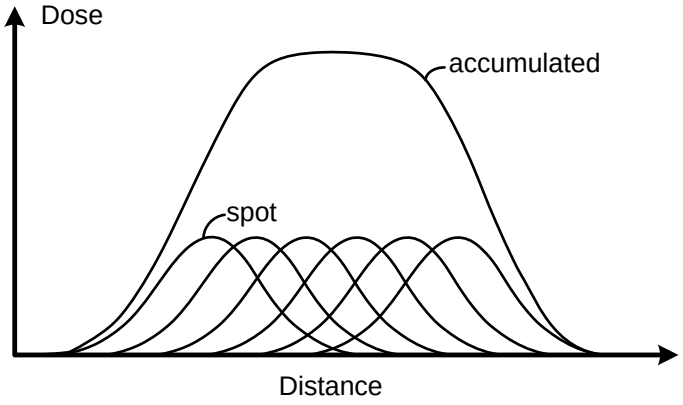


Figure 4.4 The electron dose accumulation mechanism.

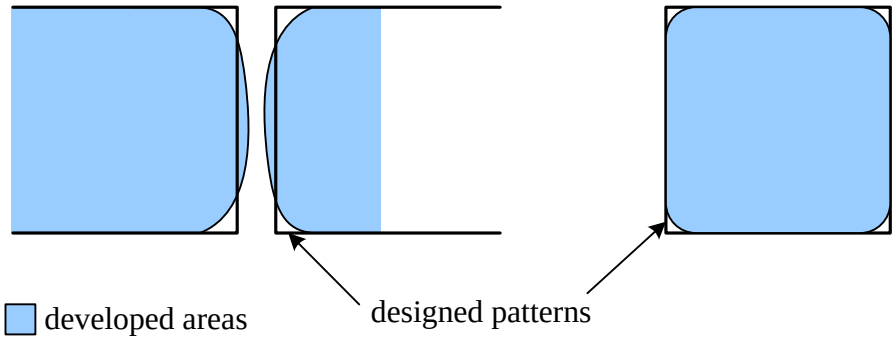


Figure 4.5 Distortion caused by the proximity error effect.

The distortion appearing between closely-placed rectangles causes problems during the fabrication of the Ohmic contacts. The problem can be eliminated after the modulation of the electron dose according to the area exposed, as described in Section 6.2.2. Since the acceleration voltage of the vectorbeam is fixed, the designer is called to find the optimum resolution, VRU and spot size according to the resist layers and the geometry of the patterns.

One advantageous consequence of the forward scattering effect is the partial exposure of the resist from electrons that do not have sufficient energy. This is fundamental for the implementation of 3-dimensional EBL where the depth of the exposed resist is adjusted by

the electron dose. The fabrication of T-gates and air bridges using 3D EBL is presented in chapters 6 and 8.

4.1.3 Metallisation

After the definition of the patterns the resist is developed which means that the exposed areas that are soluble to the developing solution are removed. Afterwards, the sample is placed in the metal evaporator and the total surface is covered by the desirable metal stack in a high vacuum environment (~10^{-7} torr). The final procedure is the lift-off where the sample is placed in pre-warmed acetone (~50^{o} C) and the remaining resist, with the unwanted metal on top, is dissolved away. It is very important that a double resist layer is used to ensure a precise definition of the patterns. The bottom resist layer has lower molecular weight in comparison with the top layer, presenting higher sensitivity when exposed to the electron beam. Thus, the undercut that results after the development provides the required discontinuity between the metal that needs to be deposited and the metal that is to be removed. The three steps of the process are depicted in Figure 4.6.

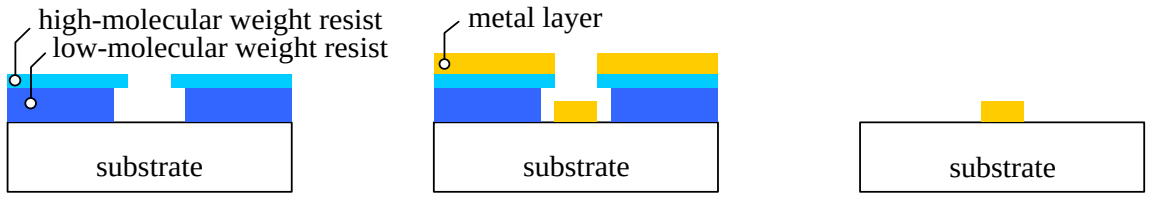


Figure 4.6 The conventional process of development, metallisation and lift-off.

4.1.4 Etching techniques

The process of etching is one the most important fabrication steps for the implementation of the active components. The removal of the epitaxial layers between the Ohmic contacts in a controlled way is very critical for the performance of the devices. Etching is also very important for the isolation of the devices from the surrounding elements, preventing any undesirable short circuiting. The dry and wet etching techniques incorporated in this work are described in the next sections.

Dry etching

One of the most common dry etching techniques is reactive ion etching (RIE). In the planar configuration illustrated in Figure 4.7 the sample is placed on the powered electrode and the second electrode is grounded. An RF source is used to create a plasma environment between the two electrodes. As electrons have a high mobility their response to the RF signal is high and they are finally separated from the parental atoms. As the remaining ions present a lower mobility, they respond only to the average applied potential. Thus, the RF source presents a double functionality by separating the more energetic radicals from the heavy ions and accelerating the ions towards the sample surface. Finally, the etching mechanism is a combination of chemical reactions and physical sputtering between the gas and the substrate.

Since dry etching presents limited selectivity over different materials due to the sputtering mechanism, the process in the chamber can be monitored incorporating an interferometer. A laser beam is directed to the substrate and the reflected beam presents intensity oscillations due to the superposition of beams with different phases. These oscillations are characteristic for materials with different refractive indices and the process can be terminated when the etch stop material is detected by following the interferometer [73].

The resulting profile of the sidewalls is mainly dependent on the etching conditions. Using high acceleration voltages the ions gain more energy and physical sputtering is the main etching mechanism causing diagonal crystallographic etching profiles. Chemical reactions are dominant for low ion energies, resulting in isotropic sidewall profiles. The etching characteristics such as the sidewall profile, the etch rate and the surface smoothness are dependent on the applied conditions such as the acceleration voltage, the RF power, the chamber pressure and the gas flow rate [74].

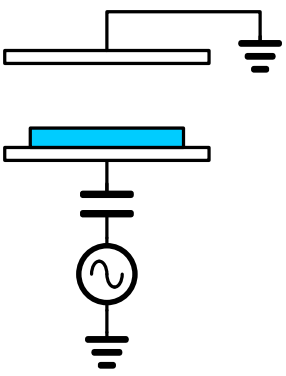


Figure 4.7 Basic structure of RIE etcher with the sample placed on the powered electrode [75].

The most significant advantage of the dry etching technique is the ability to control sidewall profiles by choosing the appropriate processing conditions. Isotropic, diagonal or vertical profiles can be achieved by tuning the contribution of the physical and the chemical mechanisms. Dry etching also presents advanced uniformity across the substrate regarding the etched depth which is very critical for the removal of thick layers of materials. However, the sputtering mechanism causes a significant damage to the substrate. The violent reactions between the high-energetic ions and the surface of the lattice can cause dislocations to the latter that can propagate deeper in the substrate. In addition, due to the sputtering of the sample surface, the resist mask often vanishes prior to the end of the process. Thus, undesired etching may occur at the areas that should be protected and the sample gets permanently damaged. Dry etching also demands advanced equipment for the control of the gasses and the maintenance of the vacuum, which increases dramatically the cost of the technology.

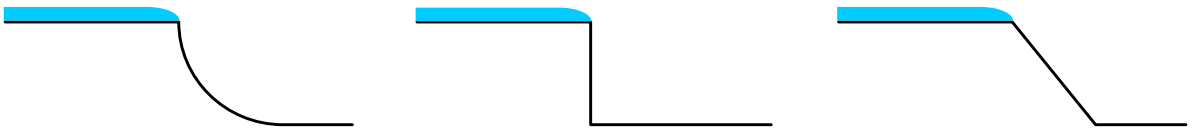


Figure 4.8 Cross-sectional profiles depending on the contribution of chemical and physical etching.

Wet etching

Wet etching is a simpler and more inexpensive solution, in comparison with dry etching, for the removal of the epitaxial layers requiring simple glassware. In addition, the chemical solutions have a reasonable cost and they can be mixed in different stoichiometries depending on the required etch rate and selectivity. One of the main advantages of wet etching is that, in contrast with dry etching, it does not cause damage to the deeper layers of the material degrading the performance of the devices. Thus, wet etching can also be performed after dry etching in order to remove the damaged layers on the surface.

The mechanism of wet etching is based on the oxidisation of the surface layers which are then etched by the by the acidic ingredient of the mixture. When the first surface layer is removed, the layer underneath undergoes the same process, and so on. Hydrogen peroxide (H_2O_2) is

commonly used as the oxidisation agent and the surface oxides are removed by the acidic elements of the solution. The etch rate and the selectivity of the etching are strongly dependent on the stoichiometry of the solution and the composition of the materials. An example is given by the citric acid/hydrogen peroxide solution ($C_6H_8O_7$ / H_2O_2), which is used for the selective removal of GaAs over AlGaAs. At a stoichiometry of 3:1 - $C_6H_8O_7$:H_2O_2 the etch rate for GaAs is 100 higher than the one for $Al_{0.3}Ga_{0.7}As$, while for 10:1 dilution both materials are etched with the same rate [76]. For an increased concentration of Aluminium, the etch rate of $Al_{0.4}Ga_{0.6}As$ remains approximately 30 times lower than GaAs even for a 15:1 - $C_6H_8O_7$:H_2O_2 stoichiometry [77].

Unfortunately, the procedure of wet etching is also very sensitive to variations of the process conditions. The temperature, the pH of the solution and the agitation of the sample need to be controlled in order toachieve reproducible etching rates. As an example, the etch rate of $Al_{0.4}Ga_{0.6}As$ by the succinic acid solution is 8 times higher for a temperature rise from 20^o C to 30^o C [78]. The same solution at 20^o C doubles in etch rate for an increase of the pH from 4.4 to 5.4.

Unlike dry etching, the wet etching process occurs at both vertical and lateral directions, creating an undercut to the resist mask. Thus, there is less control to the dimensions of the processed features. The sidewall profiles are strongly determined by the crystallographic directions in the crystal. The various crystallographic etch profiles in GaAs are presented in Figure 4.9. In the case that the sidewall profile presents a negative undercut, as presented in Figure 4.9(a), connection discontinuities can arise after the deposition of the metal. There is also an additional degree of freedom depending by the stoichiometry of the etching solution [79]. Undesired open-circuits result when the metal layer is thinner than the step in the substrate. Thus, the correct orientation of the substrate with respect to the positive slope profiles needs to be taken into account during the design and the fabrication process.

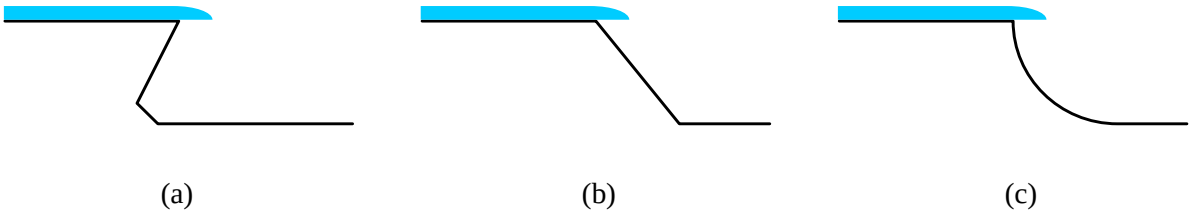


Figure 4.9 Cross-sectional profiles for various crystallographic orientations of GaAs.

The limited control of the lateral etching is one of the most significant disadvantages of the wet etching technique, affecting the performance of the transistors. The horizontal extension of etching during the removal of the cap layer is decisive for the operation of the devices, as presented in Section 6.3.6. In addition, due to the limited uniformity, wet etching is not recommended for the removal of thick epitaxial layers as various etch depths can arise across the substrate.

4.1.5 Cleaning and passivation

The cleaning of the sample is a fundamental procedure which is performed before and after the execution of every single fabrication step. Cleaning is essential for the removal of the organic compounds and the native oxide from the surface of the sample prior to the deposition of the resist layers. A typical procedure for degreasing involves the treatment of the sample with Acetone which is followed by Isopropanol (IPA) and deionized (DI) water.

The atmospheric oxygen causes oxidisation to the surface of every III-V compound semiconductor which degrades significantly the electronic performance of the devices. Typically, a layer of 2-3 nm of oxide is formed at the surface of the samples after a long term exposure to the atmospheric air [80]. The removal of the surface oxides before the deposition of the Ohmic contacts is of high importance for the fabrication of low resistive electrodes. Similarly with the wet etching techniques, an acidic solution can be used to dissolve the oxidised layers of the semiconductor. A 4:1 - H_2O:HCl deoxidising solution is commonly used for GaAs and InP based semiconductors. A monolayer of oxide can grow within a few milliseconds after the treatment which is unavoidable. After etching using the acidic solution, a treatment with high pressure nitrogen gas can limit the amount of the residual oxide by 2-3 times.

The passivation of the surface using a permanent protection layer is recommended after the deoxidisation process. This is normally performed using a Si_3N_4 layer which covers the active devices and can also serve as the dielectric layer for the implementation of the MIM capacitors.

4.2 Characterisation techniques

The reliability of the characterisation techniques is essential for the successful implementation of both active and passive components. Accurate measurements provide the required feedback for the improvement of the design and the fabrication processes. This section presents the main characterisation techniques that have been incorporated in this work.

The transmission line method (TLM) is a relatively simple technique which can be executed inside the clean room area, providing some initial indications about the material and the device characteristics. The vector network analyser (VNA) instrumentation is used for the small-signal characterisation of both the passive circuits and the active devices. The spectrum analyser tool has also been used extensively in this work for the identification of Gunn oscillations in various areas of the frequency domain.

4.2.1 Contact resistivity characterisation

The realisation of high-quality Ohmic contacts with low resistivity is essential for the implementation of high-performance HEMTs and Gunn diodes. A possible high resistance of the electrodes can cause the suppression of the growing domains of the Gunn diodes. The significance of low-resistive contacts for the transistor operation has been demonstrated in Section 2.6.2 were high values of R_S and R_D cause a significant degradation to the small-signal performance of the device (equations 2.28, 2.31 - 2.33).

The transmission line method (TLM) [81] provides a simple method for the determination of the contact resistivity at the metal-semiconductor interface as well as the sheet resistance of the semiconductor. The TLM structure is depicted in Figure 4.10 consisting of equal-area square pads with variable distances separating them. The measured contact resistance between the various pairs of pads is expected to increase in a linear relationship with the gap length, as a result of the increasing resistance introduced by the semiconductor. For the extraction of the total resistance, a four-probe approach is followed where the current is driven by one probe on each pad and the voltage is monitored by the other two probes. The resulted resistance is equal to the combined resistance of the two metal-semiconductor interfaces and the resistance introduced by the semiconductor. A typical resistance over distance (R-d) plot is illustrated in Figure 4.11.Under the hypothesis that the length of the semiconductor between the pads is zero, the resulting resistance would have been caused only

by the two metal-semiconductor interfaces. Thus, the intersection of the *R-d* characteristic with the *R*-axis provides twice the value of the contact resistance for each pad. In this work, the contact resistivity is expressed after multiplying R_C by the width of the pads W (i.e. 2 Ω * 150 µm = 0.3 Ω.mm). The sheet resistance R_{sh} of the material results from the slope of the *R-d* characteristic divided by the width W of the pads. The voltage under the contact follows an exponential distribution as the distance increases. The transfer length L_T, which can be found from *R-d* characteristic, represents the distance where the voltage curve drops to 1/e.

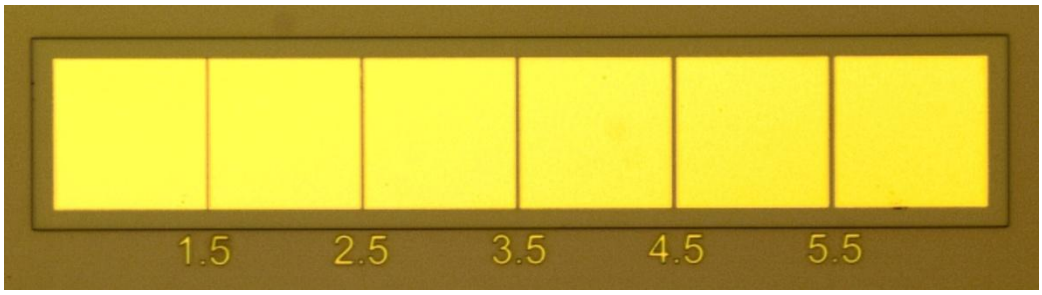


Figure 4.10 Fabricated TLM pattern with 1.5 - 5.5 μm pad distance.

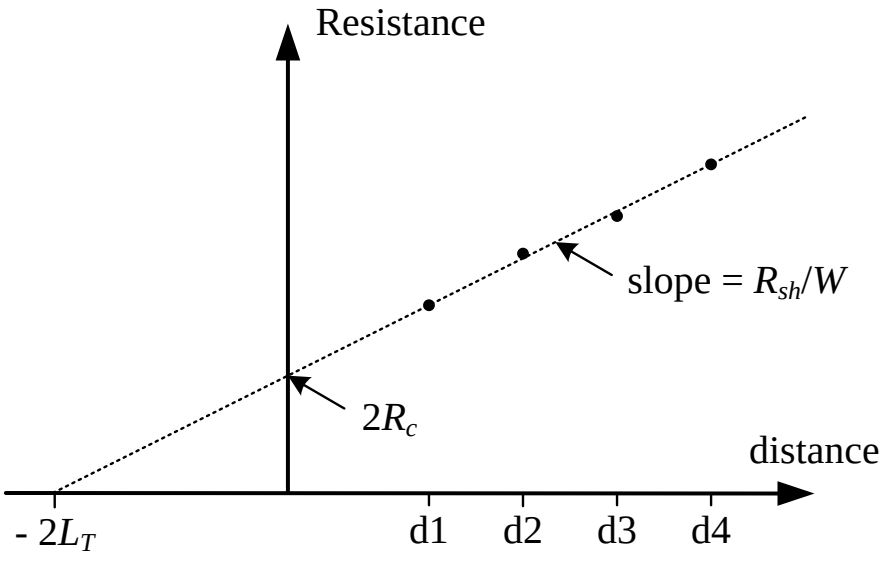


Figure 4.11 Resistance over distance characteristic for the extraction of the contact and the sheet resistance by the TLM method.

4.2.2 Vector network analyser characterisation

Small-signal measurements are required for the characterisation of every component used in a MMIC. A VNA has been used extensively in this work for the characterisation of the passive components, the HEMTs and the Gunn diodes. The VNA operation is based on the determination of the scattering parameters from the incident and the reflected voltage waves in the network. The scattering parameters are calculated according to the microwave network theory, as described in the next section.

A hypothetical two-port network, like a matching network or a HEMT, is illustrated in Figure 4.12. The voltage vector at the port *i* is equal to [82]:

$$V_i = V_i^{\text{in}} + V_i^{\text{ref}} \tag{4.1}$$

where V_i^{in} is the incident to the network and V_i^{ref} the reflected wave due to impedance mismatches. The factors a_i and b_i of each port are defined as:

$$a_i = \frac{V_i^{in}}{\sqrt{2Z_{0i}}} \tag{4.2.a}$$

$$b_i = \frac{V_i^{ref}}{\sqrt{2Z_{0i}}} \tag{4.2.b}$$

where Z_{0i} is the characteristic impedance of the port *i*. Finally, the scattering parameters are defined as:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2 = 0} \tag{4.3.a}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2 = 0} \tag{4.3.b}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1 = 0} \tag{4.3.c}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1 = 0} \tag{4.3.d}$$

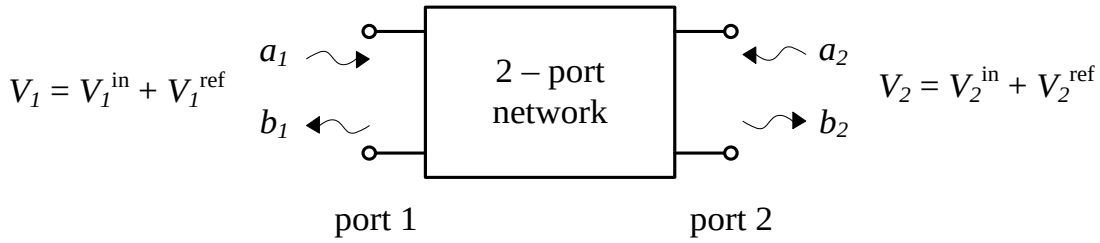


Figure 4.12 Calculation of the scattering parameters from a two-port network.

The condition of $a_i = 0$ is satisfied by terminating the port i to a matched load. Assuming that port 2 is terminated and the wave a_1 is driven to the network, a fraction of a_1 will be reflected as b_1 and the wave b_2 will exit the network. The two waves will be $b_1 = S_{11}\, a_1$ and $b_2 = S_{21}\, a_1$. Similarly, when port 1 is terminated, the two waves will be $b_1 = S_{12}\, a_{12}$ and $b_2 = S_{22}\, a_2$. With both ports active:

$$b_1 = S_{11}\, a_{11} + S_{12}\, a_{12} \tag{4.4.a}$$

$$b_2 = S_{21}\, a_{11} + S_{22}\, a_{22} \tag{4.4.b}$$

where the matrix representation is:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{4.5}$$

The scattering matrix is characteristic for each network, indicating the allowance or the blocking behaviour of the network between the two ports. An active device like a transistor is expected to present an S_{21} parameter greater than one within the frequency range of interest.

In the case of two cascade connected networks, it is more convenient to express the voltage waves using the scattering transfer parameters T. These are given by [83]:

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \tag{4.6}$$

Figure 4.13 illustrates the voltage waves and the T parameters of the two cascade networks N_x and N_y. The voltage waves of the total network are given by Equation 4.7.

$$\begin{bmatrix} a_{1x} \\ b_{1x} \end{bmatrix} = \begin{bmatrix} T_{11}^{\,x} & T_{12}^{\,x} \\ T_{21}^{\,x} & T_{22}^{\,x} \end{bmatrix} \begin{bmatrix} T_{11}^{\,y} & T_{12}^{\,y} \\ T_{21}^{\,y} & T_{22}^{\,y} \end{bmatrix} \begin{bmatrix} b_{2y} \\ a_{2y} \end{bmatrix} \tag{4.7}$$

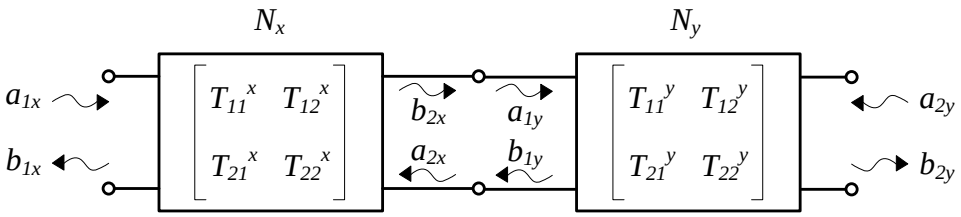


Figure 4.13 Cascade connection of the two networks.

If the *T* matrix of the total network is known as well as the *T* matrix of one of the two networks, the *T* matrix of the other network can be easily found from Equation 4.7. Thus, the *T* parameters provide as easy method of de-embedding for cascade networks, which is used for the subtraction of the effects introduced by the transition pads of the HEMTs (Section 7.2.2). The transformation formulas between the *S* and the *T* parameters are presented in Appendix A.

The wave vectors are used by the VNA for the extraction of the *S* parameters of the measured components. A general block diagram of a VNA is illustrated in Figure 4.14 [84]. The signal generator produces the RF signal which is divided by the power splitter to the reference signal and the measurement signal. An attenuator is used for the adjustment of the power level of the measurement signal. Thus, a power sweep at a certain frequency can be used for the characterisation of non-linear circuits, like power amplifiers, for the extraction of the P_{OUT} / P_{IN} characteristic. The attenuated measurement signal is driven to a directional coupler which is able to isolate the incident and the reflected signal of the device under test (DUT). A local oscillator (LO) generates a signal which is similar to the RF signal for the down-conversion of the reference and the measurement signals (reflected and inserted) to the frequency IF. The difference between the RF and the LO signals is externally set by adjusting the IF bandwidth. Finally, the reflected and the inserted signals are compared to the reference signal by the phase sensitive detectors (PSDs) which detect the magnitude and the phase differences between the channels. The two switches are set alternately to the left and to the right position for the extraction of the S_{11}, S_{12} and the S_{21}, S_{22} parameters, respectively.

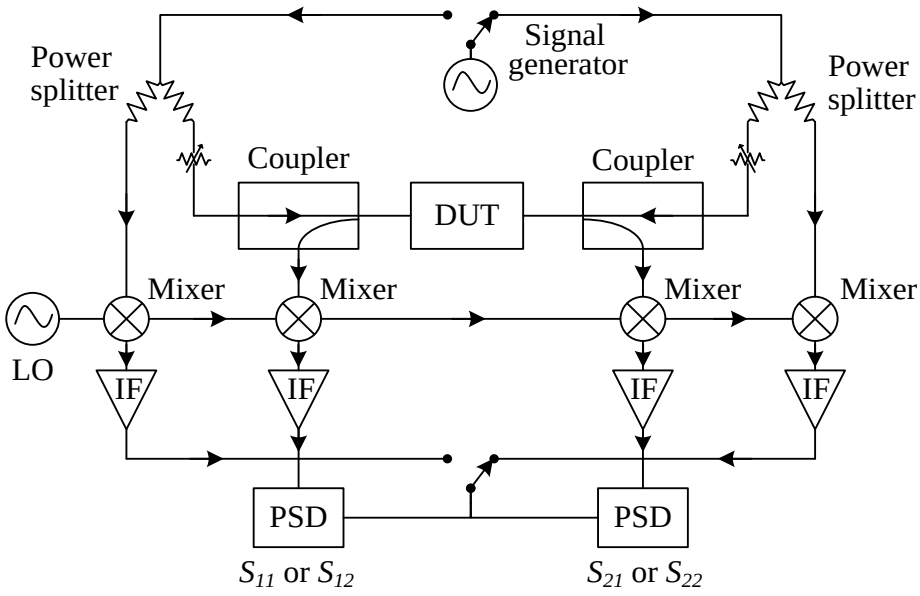


Figure 4.14 General block diagram of a vector network analyser [84].

A calibration procedure of the test set-up is required before the characterisation of the DUT, for the elimination of the systematic errors that are introduced by system imperfections. These can be mismatches between the equipment components, insertion losses of the cables, crosstalk etc, affecting the measured *S* parameters [85]. Assuming that the PSD detectors of the VNA are ideal, the calibration process subtracts the measurement errors up to the point of the probe tip after the measurement of some on-wafer calibration standards. In this work, two calibration techniques were followed, the SOLT (short, open, line, through) and the LRRM (line, reflect, reflect, match). The LRRM calibration procedure was executed for measurements above the V-band (75-110 GHz) presenting smaller calibration errors [86, 87].

In addition to the characterisation of the passive components and the HEMTs, VNA measurements also provide an easy way for an initial identification of oscillations produced by one-port devices. While measuring an active oscillator using a VNA, the oscillator signal is added to the VNA RF signal that is reflected from the device. Thus, under certain circumstances, the S_{11} parameter resulting from a one-port oscillator can be greater than one (0 dB) near the frequency of oscillation, as presented in [3]. In general, the detection of sharp peaks or valleys in the S_{11} parameter, depending on the phase offset between the VNA and the device signals, can indicate generated oscillations [88].

The spectrum analyser used in this work, had the ability of detecting signals itself up to 50 GHz. Measurements of frequencies above that limit were performed using down-conversion incorporating external mixers. Thus, measurements had to be performed separately for the frequency ranges 3 Hz-50 GHz, 50-65 GHz and 75-110 GHz requiring three different experimental setups. In contrast, the VNA set-up, connected with the appropriate frequency extenders, can perform a one-step frequency sweep from 10 MHz to 110 GHz. For this reason, an initial characterisation of the Gunn diodes using the VNA was performed in this work, saving some time from setting up the spectrum analyser instrumentation.

4.2.3 Oscillation detection using the spectrum analyser

As described above, an initial test of the Gunn diodes can be performed using the VNA. Further measurements are required afterwards using the spectrum analyser for the accurate identification of the oscillating characteristics such as the centre frequency of oscillation and the generated power.

A general block diagram of the spectrum analyser is illustrated in Figure 4.15 [89]. The signal is initially attenuated for the protection of the instrument in the case of a high-power input, before getting down-converted from the mixer to the IF frequency. The noise of the IF signal is filtered by the resolution bandwidth filter and the signal is amplified or suppressed afterwards to the appropriate power level for the envelope detector. The video bandwidth filter minimises the noise inserted by the instrument, and the peak power values are identified by the relevant detector. Finally, the signal is digitised by the analogue-to-digital converter (ADC), for display [90].

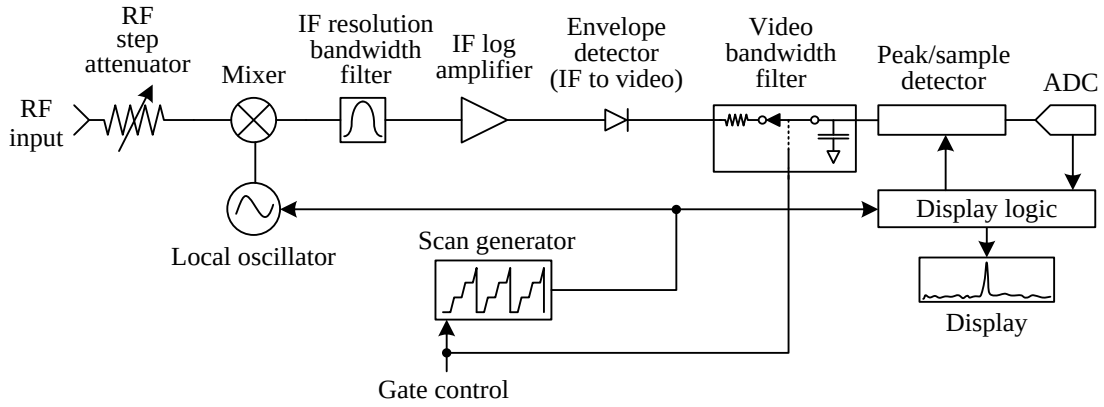


Figure 4.15 General block diagram of the spectrum analyser with gate control [89].

An E4448A spectrum analyser from Agilent Technologies was used in this work, with gated LO timing. In this concept, a gate control is used for the control of the instrument by disabling the LO sweep and the video bandwidth filter when measurements are paused [89]. The current instrument presents the ability of measuring within the 3 Hz - 50 GHz frequency range. For measurements above 50 GHz, an externally connected set-up is required as presented in Figure 4.16. An external mixer, operating within the frequency range of interest, is used for the down-conversion of the high-frequency signal. The LO signal, which is generated by the spectrum analyser, is separated by the down-converted IF signal using a diplexer.

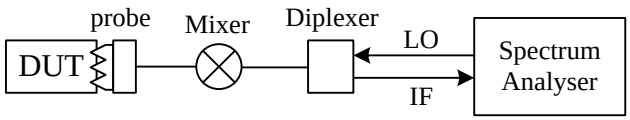


Figure 4.16 Simplified block diagram for measurements above the limit of the spectrum analyser.

4.3 Chapter summary

This chapter has initially presented an overview of the main fabrication techniques incorporated in this work. The concepts of e-beam lithography were described in addition with the scattering effects that electrons experience after entering the resist layer. The scattering effects can be used beneficially for the formation of 3D resist profiles, aiming the implementation of T-gates and air bridges as presented in chapters 6 and 7. The various etching techniques, such as dry etching and wet etching were compared for the needs of the different fabrication steps. The appropriate cleaning and passivation of the wafer surface is also required, preventing from the degradation of the device performance.

The characterisations techniques used in this work were presented afterwards. The TLM technique provides the feedback for the evaluation of the quality of the Ohmic contacts. The small-signal measurements using the VNA, has also been described for the characterisation of both the passive and the active components. Finally, the operation of the spectrum analyser and the related set-up were described for the identification of oscillations in the mm-wave regime.

5. Technology review

Today's MMIC technology demonstrates a great variety of applications, such as ultra-fast telecommunication systems, biomedical systems, remote sensing, radar and security systems. Thus, there is a growing demand for more advanced active and passive components with improved power efficiency, maximum frequency of operation and minimum integration area.

This chapter presents a brief review of the latest developments for the implementation of Gunn diodes, HEMTs and MMIC amplifiers. These developments incorporate the design of advanced layer structures and the introduction of new fabrication techniques.

5.1 Gunn diodes

Gunn devices have been used for the implementation of millimetre and sub-millimetre wave sources, mainly based on GaAs and InP material systems, presenting up to hundreds of milliwatts of generated power [47]. A significant development of vertical GaAs devices for automotive applications has been presented recently, generating oscillations at 77 GHz with 83.2 mW output power [91, 3]. The layer structure includes a hot electron injector layer which consists of graded $Al_xGa_{1-x}As$ layers between the emitter and the transit region. Thus, the dead zone and the positive resistance that appear at the beginning of the transit region are practically eliminated. Fully packaged commercialised vertical Gunn oscillators have been presented, based on the principle of the hot electron injector. The devices are embedded in waveguide circuits delivering 121.5 GHz frequency of oscillation with 40 mW generated power after the extraction of the second harmonic [92].

Similar implementation approaches have been presented using InP-based vertical Gunn devices, demonstrating oscillations beyond 150 GHz in the fundamental-mode of operation [7]. The devices were mounted on diamond heat sinks to reduce thermal dissipation and deliver approximately 130 mW output power. The combination of two devices in a dual-cavity waveguide led to the enhancement of the performance of the oscillator circuit, generating up to 305 mW combined power at 106 GHz [93]. The same devices have been used for the realisation of oscillators exceeding frequencies of 400 GHz after the suppression of the fundamental-mode and the second harmonic [94, 95]. Thus, generated signals in the

range of 400-480 GHz with maximum output power of 85 μW have been demonstrated from the extraction of the third harmonic of oscillation.

Although oscillators based on the vertical version of the Gunn diode present remarkable results in terms of generated power, their implementation demands increased complexity, size and cost. The bottom contact layer of the structure needs to be exposed for the fabrication of the Ohmic contact. In addition, the active part of the layer structure is required to be separated from the substrate in order to be embedded inside the waveguide circuit. The general process for the implementation of vertical Gunn diodes is described in the next paragraph.

Initially, a metallic alloy layer is deposited on the top of the highly doped layer in order to form an Ohmic contact. Afterwards, a thick layer of gold is deposited to act as a heat sink as the device conducts an enormous DC current, which is in the order of Amperes [3]. After the deposition of gold the substrate is removed. A fast wet etching solution is used to etch away the biggest part of the substrate which is followed by a slower selective solution for stopping at the etch-stop layer (citric acid for GaAs/AlGaAs). The etch stop layer of AlGaAs is removed later by a hydrofluoric acid solution. A very thick layer of metal (usually nickel) is plated afterwards to stabilise the layer structure. Since the bottom highly doped layer is exposed, the chip is flipped and a metal alloy is deposited to form the second electrode of the device. After the removal of the nickel, the chip is packaged and mounted in the waveguide cavity for the realisation of the complete oscillator. A similar fabrication procedure is followed for the implementation of the InP devices [93, 94, 95] where the devices are mounted on metallised diamond heat sinks.

As presented in Section 2.7.4, the latest development of the vertical structures presents a MMIC-compatible device with a significantly simplified fabrication procedure [8]. The fabrication process incorporates dry etching using electron cyclotron resonance-reactive ion etching (ECR-RIE), monitoring the etched depth with a profilometer for reaching the bottom highly-doped layer. Since vertical sidewalls of the mesa result from the dry etch process, a self-aligned technique is applied for the simultaneous evaporation of the top and bottom metal electrodes. The final fabrication step is the realisation of the air bridges which increases the complexity of the technology, requiring the spin coating and subsequent dry etching of polyimide using RIE. The devices present a maximum generated power of 2.5 mW at 37.2 GHz. Although the power performance is very promising, the maximum oscillation frequency is limited by the fixed thickness of the channel layer.

The maximum oscillation frequency in fundamental-mode of the MMIC-compatible devices was boosted beyond 100 GHz with the introduction of the planar Gunn diodes [9]. Both electrodes are placed on the top highly-doped layer where the anode to cathode separation can be determined accurately by the lithographic process. The only demanding step of the fabrication process is the selective recess etching of the cap layer between the electrodes which needs to be performed accurately. The first planar Gunn diode demonstrated oscillations of 45 nW generated power at 108 GHz fundamental-tone frequency.

The main research in the subsequent years was focused on the maximisation of the generated power of the planar Gunn diode by modifying the design of the epitaxial layers. The introduction of double δ-doping layers on each side of the channel led to the enhancement of the device current by a factor of 2 with a proportional increment of the generated power [96]. Better phase noise characteristics were also achieved as a result of the increased electron concentration in the channel. A significant development of the power characteristics has been presented after using a lattice-strained channel layer of $In_{0.23}Ga_{0.77}As$ on a GaAs material system [46][97]. Due to the superior characteristics of the $In_{0.23}Ga_{0.77}As$ channel layer, the devices generate power equal to 4 μW at 116 GHz oscillation frequency. The latest development of GaAs-based planar Gunn diodes incorporates 7 channel layers of strained $In_{0.23}Ga_{0.77}As$ demonstrating an exceptional improvement of the generated power which is equal to 400 μW [11]. The fundamental-mode frequency is equal to 109 GHz while the extraction of the second harmonic at 218 GHz delivers 2.2 μW output power.

The reliability of the devices described above has been significantly improved after the introduction of composite anode contacts, where the anode pad is designed in order to overlap with the active area by 0.3 μm [98]. Thus, the current inserting the anode is spread at the Schottky contact and the Ohmic contact, decreasing the high electric field at the edge of the electrode. Thus, the breakdown of the device occurs at biasing voltages sufficiently beyond the NDR region.

A further increment of the indium content above 23% can cause the lattice mismatch with the GaAs system, resulting in increased defects in the crystal. The growth of $In_{0.53}Ga_{0.47}As$ layers is feasible using an InP substrate since the two materials are lattice matched. The first planar Gunn diodes using a $In_{0.53}Ga_{0.47}As$ channel layer have been recently demonstrated presenting a fundamental-mode oscillation at 164 GHz [99]. The maximum generated power is 100 μW from devices with 1.3 μm anode to cathode separation and 120 μm width.

Gunn diodes, apart from being used as signal sources, have found various applications in mm-wave circuits. Vertical devices combined with varactors embedded in waveguide circuits have been used to compose voltage controlled oscillators (VCOs) [100] and complete modules of tranceivers at 94 GHz [101]. The combination of the diode with the varactor provides oscillations with 1365 MHz available tuning of the centre frequency which is significantly extended in comparison with the tuning ability of the diode itself [94, 95]. Reflection amplifiers based on Gunn diodes have been presented based on the principle of reflection with $S_{11} > 0$ dB [102, 103, 104]. This results from the calculation of the reflection coefficient given by Equation 3.7 for a negative real part of impedance which is provided from the NDR of the Gunn diode. The same principle can be applied in future by combining planar devices with CPW hybrid couplers for the composition of MMIC sources and amplifiers based on Gunn diodes. Based on the nonlinearity of the diode impedance, two-port planar Gunn diodes have also demonstrated operation as mixers [105]. The diode, operating also as a local oscillator, provides excellent mixing linearity within a power range of 30 dBm, presenting though a relatively high conversion loss of approximately 20 dB.

5.2 HEMTs and MMIC amplifiers

The development of MMICs is strongly dependent on the improvement of the characteristics of the active devices, which are mainly transistors for the basic circuit modules. The efforts for the enhancement of the HEMT performance had been initially focused on the realisation of T-gates for the elimination of the parasitic effects. After reaching the sub-50 nm limit for the gate length, advanced layer structure designs and more complex fabrication techniques were presented for reaching the sub-mmwave regime. The evolution of the technology over the last years that led to the recent realisation of HEMT-based THz amplifiers is described in the next section.

The first fabrication method for the implementation of T-gates was demonstrated using a PMMA / MPR (Matsuhita positive resist) stack [106]. The PMMA / MPR bi-layer presented low and high sensitivity to e-beam, respectively, for the realisation of the required resist profile. The addition of a third low-sensitivity layer on the top of a bi-layer provided the required undercut profile for the lift-off process [107]. A PMMA / P(MMA MAA) / PMMA tri-layer resist stack was used in a single-step process demonstrating a 250 nm T-gate technology for HEMTs with 50 GHz cut-off frequency.

A new generation of devices resulted after using a PMMA-LOR-UVIII tri-layer resist system, demonstrating the fabrication of T-gates with 30 nm length [108]. UVIII is a photoresist which also serves as a low-resolution e-beam resist with high sensitivity. Thus, the deposition of UVIII on the top presents a wide window after the exposure for the formation of the "head" of the T-gate. The LOR layer serves as separator, preventing the dilution between the PMMA and the UVIII. Pseudomorphically grown HEMTs on GaAs substrates with 50 nm gate length presented an f_T of 200 GHz, while metamorphic devices with increased Indium content in the channel reached the frequency of 350 GHz. Using the same T-gate fabrication technology, the performance of mHEMTs was reinforced after increasing the Indium content in the channel up to 70% [109, 110]. The benefits of using a self-aligned technique for the deposition of the Ohmic contacts were demonstrated in [109]. The devices with self-aligned evaporated drain and source electrodes delivered 1.9 mS/mm g_m and 490 GHz f_T over 1.6 mS/mm g_m and 465 GHz f_T of the conventional technique. A new recess etching procedure was also introduced following three etching steps before the deposition of the gate. The succinic acid-orthophosphoric acid-succinic acid treatment was used to bring the gate closer to the channel for a more efficient current modulation. Similar devices with an f_T of 550 GHz were used for the implementation of a single-stage amplifier, presenting more than 10 dB gain at 90 GHz operation frequency [110].

A multiple-step technique for the realisation of the recess etching was also performed on $In_{0.7}Ga_{0.3}As$ pseudomorphic devices, bringing the gate close to the channel layer by 4 nm [111]. The fabrication of 25 nm long T-gates was realised after using a ZEP/PMGI/ZEP resist stack and the devices presented an f_T of 562 GHz.

A problem that usually arises during the implementation of T-gates is the reduced mechanical stability of the structure due to the short length of the gate "foot". An alternative technique for the achievement of high-yield fabricated devices has been presented demonstrating a zigzag layout for the design of the gate "foot" [112]. A tri-layer system of PMMA/PMGI/P(MMA-MAA) was used for the fabrication of 35 nm long T-gates with enhanced yield. An $In_{0.53}Ga_{0.47}As$ channel layer was grown metamorphically on GaAs and the devices presented a record, for that time, f_{max} equal to 520 GHz.

Ultra-short T-gates with 15 nm length have been presented with a cut-off frequency of 610 GHz [113]. A layer of Si_3N_4 is deposited prior to the recess etching step and a ZEP resist layer serves as a mask with high lithographic resolution and with high resistivity to dry

etching. A layer of conformal polymer is deposited and the etching of the Si_3N_4 is performed afterwards using a double RIE process. The high f_T achieved from devices with ultra-short gates results from the enhanced average electron velocity under the gate. However, the fabrication of ultra-short gates requires the use of Si_3N_4 which increases the parasitic capacitance in the area around the base of the T-gate. As a result, the devices present an f_{max} equal to 330 GHz which is significantly lower than the f_T.

The technology of the amplifiers is strongly dependent on the development of the transistors. Multi-stage amplifiers combine more than one devices in series for the generation of higher gain values. As an alternative to the series configuration, cascade devices present approximately double available gain for the same integration area. Based on the cascade connection of two HEMTs with 120 nm long T-gates, low noise amplifiers (LNAs) have demonstrated 8 dB of gain per cascade pair for the 105 - 115 GHz frequency range [114]. The current configuration presents very good noise characteristics with less than 4 dB noise figure at 105 GHz. The researchers were able to use the cascade pair in a 3-stage amplifier presenting 22 dB small signal gain over the 100-115 GHz frequency range. Metamorphic technology was used for the growth of the InGaAs channel layer with high Indium content on a GaAs substrate, as a less expensive solution over InP substrates. The combination of the biasing circuits with the matching networks led to the realisation of compact circuits with 0.725 mm^2 integration area for single stage amplifiers.

The same cascade approach using metamorphic GaAs wafers was followed in [115], where the reduction of the gate length led to the enhancement of the cut-off frequency to 220 GHz. The devices were used in a four-stage cascade amplifier demonstrating 20 dB of gain in the frequency range of 210 - 220 GHz. The devices were further developed with the increment of the Indium content in the channel to 80% and the reduction of the gate length to 50 nm. The latter mHEMTs presented improved small signal characteristics with 380 GHz f_T and 380 GHz f_{max}, over 220 GHz and 300 GHz, respectively, for the 100 nm devices.

The majority of the work presented in the subsequent years adopted the solution of channel layers with high Indium content which provides superior small-signal characteristics and high current levels. An $In_{0.75}GaAs$ channel layer was used in [116] incorporating a 70 nm T-gate technology, demonstrating 250 GHz f_T and 400 GHz f_{max}. Eight devices were used for the realisation of a two-stage amplifier chip. Each stage consists of two amplifiers with two sub-stages where the signal is initially divided and re-combined in the end using branch line

couplers [117]. Two cascaded chips were mounted in a WR-5 fixture, presenting 20-40 dB small-signal gain from 160 GHz to 195 GHz.

Two different approaches using $In_{1-x}Ga_xAs$ channel layers have been followed in [118] and [119], highlighting the tradeoffs that appear during the selection of the Indium fraction for different applications. For the implementation of power amplifiers, the Indium content was selected to be 65% and a 100 nm gate technology was incorporated, providing higher breakdown voltages [118]. The power amplifier presented 9.5 dB of gain at 105 GHz with 19 dBm of output power at the 1 dB compression point. The Indium content was increased to 80% and the gate length reduced to 50 nm for the realisation of high-frequency LNAs presenting an average gain of 16 dB between 180-220 GHz [118, 119].

In addition to the development of the active components, the performance of MMIC LNAs can be reinforced by using advanced transmission lines with lower insertion loss. Elevated CPW and grounded elevated CPW transmission lines have demonstrated advantageous performance over conventional CPW structures at the upper limit of the mm-wave regime, eliminating the dielectric loss effect [120, 56]. The use of air bridge-type transmission lines (ABTL) for the implementation of H-Band LNAs has been demonstrated in [121]. The ABTLs were combined with a 70 nm GaAs mHEMT technology for the demonstration of 4-stage LNAs with gain higher than 18 dB between 216 GHz and 238 GHz.

Further reduction of the gate length to 35 nm in combination with an $In_{0.75}GaAs$ channel layer, was applied for the realisation of devices with a maximum transconductance equal to 1.6 mS/mm [122]. The transistors were used in 3-stage amplifiers presenting 11.6 dB of maximum gain at 270 GHz, setting a new record frequency of operation at that time. The same HEMT technology was also used for the implementation of a 245 GHz amplifier with 12 dB of gain [123]. For the implementation of the 3-stage amplifier, 1:2 power dividers were used between the stages and a 4:1 power combiner was used for adding the signals in the output.

The same HEMT technology [122, 123] demonstrated the first submillimeter-wave amplifier, presenting 4.4 dB of gain at 308 GHz [124]. The common gate configuration used in the current amplifier, presented conditional stability which could be turned to unconditional stability after lowering the biasing voltages at the expense of the available gain. A modified HEMT layout was applied for the improvement of the high-frequency performance. Two finger transistors with 30 μm width presented a cut-off frequency exceeding 300 GHz with

the maximum frequency of oscillation exceeding 600 GHz. However, no further information was reported for the modified HEMT layout. A new record-breaking LNA based on the same technology, was presented by the same research group, after reducing the HEMT width from 30 μm to 10 μm [123]. Due to the reduced parasitics introduced by the gate, the cut-off frequency was increased to 400 GHz. The 3-stage LNA presents 16 dB of gain at 340 GHz with an impressive bandwidth of 100 GHz (240-340 GHz) and gain higher than 10 dB.

A new generation of S-MMICs has been introduced after the realisation of the first HEMT with f_{max} greater than 1 THz [12] adopting the same 35 nm T-gate technology as in [40-43]. The key-development of the InP-based material system was the increment of the doping level for the cap layer. As a result, the contact resistivity was reduced to 0.05 Ohm.mm and the devices presented exceptional small-signal characteristics with 2300 mS/mm of maximum transconductance. However, no further information regarding the fabrication of the T-gate and the detailed layer structure has been revealed. The devices were improved as presented in [125] after reducing further the gate length and applying an appropriate epitaxial scaling according to the new geometry. Thus, the cut-off frequency was increased from 385 GHz to 586 GHz and 3-stage amplifiers were implemented producing 7 dB of gain at 390 GHz. The same technology was used later for the demonstration of a 0.48 THz amplifier [126]. The circuit consists of 5 amplifying stages, demonstrating a gain higher than 10 dB between 465-482 GHz. The width of each gate finger was reduced to 7 μm for operation at higher frequencies.

At the same time, the less expensive mHEMT GaAs-based technology demonstrated devices with comparable performance to the THz technology described above. T-gates with 35 nm length were fabricated following a two-step process [127]. A Si_3N_4 layer was initially spun and dry etched in order to form the window for the gate "foot". The T-gate was formed afterwards using a three layer PMMA resist stack. Devices with 2 x 10 μm finger width presented excellent small-signal performance with 515 GHz f_T and > 900 GHz f_{max}. The finger width was reduced to 5 μm for the realisation of a 4-stage amplifier delivering 16.1 dB of gain at 460 GHz. Several modifications were applied afterwards for the development of the mHEMT technology. The $In_{0.8}GaAs$ channel layer was enclosed by double-side doped $In_{0.52}AlAs$ barriers, the "foot" window on Si_3N_4 was reduced to 20 nm and the drain was brought close to the source terminal by 500 nm [128]. As a result, the cut-off frequency of 2 x 10 μm finger devices was extended to 660 GHz. Transistors with 2 x 4 μm fingers were

used for the composition of a 4-stage amplifier, presenting an average gain of 10 dB between 470-500 GHz.

A state-of-the-art amplifier has been recently implemented using 30 nm InP HEMT transistors [129]. A composite InGaAs/InAs/InGaAs channel layer was introduced presenting superior electron transport properties and the 14 μm wide transistors presented f_{max} > 1 THz. The 10-stage amplifier delivers a maximum gain of 30 dB at 670 GHz, setting a new benchmark for the THz technology.

6. Individual fabrication of planar Gunn diodes and HEMTs

6.1 Introduction

The physical principles, fabrication techniques and characterisation methods were described in the previous chapters. In this chapter, these shall be combined for the realisation of the Gunn diodes and the HEMTs. The layer structures, the existing and developed fabrication techniques and the measurements conducted for the characterisation of the devices are presented in detail in the next paragraphs. Section 6.2 presents the fabrication of planar Gunn diodes and section 6.3 presents the implementation of pHEMTs. The GaAs wafers incorporated in this work have been designed separately for the two devices.

6.2 Fabrication of planar Gunn diodes on single GaAs wafers

6.2.1 Layer structure of the Gunn diode wafers

Initially, two different GaAs wafers were used as test materials for the implementation of planar Gunn diodes using existing or developed, when required, fabrication techniques. Figure 6.1(a) illustrates the detailed layer structure of the first wafer with name C341, as presented in [96]. An un-doped buffer layer of GaAs with 0.5 μm thickness was first grown on the 620 μm thick semi insulating substrate using MBE. This buffer layer is used to increase the crystal quality before the growth of the active layers on the top, preventing the transfer of defects caused by the substrate. The un-doped GaAs channel is sandwiched between the two $Al_{0.23}Ga_{0.77}As$ barrier layers that confine the electrons in the GaAs quantum well. The double silicon δ-doping layers used for each barrier layer present a higher electron concentration in the channel, in comparison with the single δ-doped layer structure. A highly doped $Al_{0.8}Ga_{0.2}As$ layer was grown afterwards, serving as an etching-stop layer for the recess process. Finally, a compositionally graded GaAs / $In_xGa_{1-x}As$ cap layer ending with $In_{0.53}Ga_{0.47}As$ was grown on the top of the layer structure. $In_{0.53}Ga_{0.47}As$ presents a significantly lower band gap in comparison with GaAs (0.7 eV and 1.4 eV, respectively). High-quality Ohmic contacts are feasible when using InGaAs cap layers with high Indium content, by lowering the Schottky barrier between the semiconductor and the metal of the

electrodes [130]. The $In_{0.53}Ga_{0.47}As$ is grown on GaAs using a metamorphic process to maintain the lattice matching.

The layer structure of the second wafer with name C230 is presented in Figure 5.1(b). In this wafer the multi-channel approach was followed, where a second group of AlGaAs/GaAs/ AlGaAs layers is placed below the top group to formation a second quantum well. Two δ-doping layers were used for the electron supply of each channel, with a total number of four δ-doping layers as in C341. Simulation results have presented enhanced performance of the two-channel wafer over the single-channel, where the current of the devices was increased by a factor of approximately two [46][131].

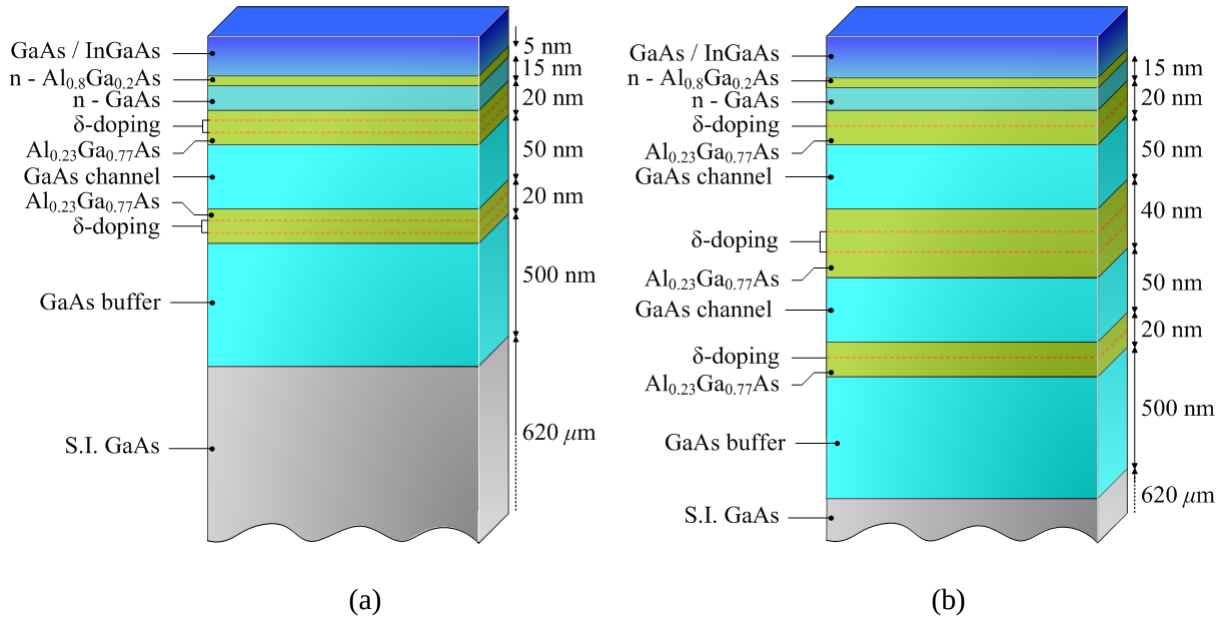


Figure 6.1 The layer structure of the single-channel wafer with 4 δ-doping layers per channel (a) and the double-channel wafer with 2 δ-doping layers per channel (b) (not to scale).

6.2.2 Fabrication of Ohmic contacts

The first step for the implementation of the planar Gunn diodes is the fabrication of the Ohmic contacts which serve as anodes and cathodes for the devices. This lithographic step is usually combined with the definition of the alignment markers, saving some fabrication time. The designed L_{ac} varies from 1.3 μm to 4 μm, determining the oscillation frequency within the range of approximately 40 - 120 GHz [46].

The patterns are defined on a bi-layer resist stack of poly-methyl methacrylate (PMMA). The bottom layer is a 12% PMMA layer with low-molecular weight and a 2.5% PMMA layer with high molecular weight is deposited on top. The bottom resist layer presents higher sensitivity when exposed to e-beam, to form the required under-cut profile for the lift-off process. For the L_{ac} dimensions described above, the distance between the two pattern areas is small enough for the appearance of the proximity error, as illustrated in Figure 4.5. Thus, the gap between the electrodes is not constant and the proximity error becomes more intense for narrow L_{ac} geometries. A conventional solution is given by the alternate fabrication of the two patterns individually. This minimises the variance at the distance of the electrodes, however an additional exposure and metallisation step are required.

In this work, a proximity error correction software tool was used as a part of the Layout beamer software (by GenISys GmbH). The software takes as an input the material and the thickness of the resist layer, generating variable multiplying factors for the different areas of the patterns. The basic dose set by the user is multiplied by the correction factors. These are calculated according to the relative position of the area to be written with the edges of the pattern. Higher gradient doses are assigned to the areas close to the corners of the patterns thereby ensuring square edges. In contrast, the central areas of the patterns are exposed to lower electron doses. Thus, wider areas are exposed due to the increased scattering effects and the patterns are written faster. Figure 6.2 illustrates the generated pattern with the proximity error correction factors for the anode and cathode electrodes of the diode. An additional dose test is required for the identification of the optimum basic dose. Figure 6.3 depicts three fabricated set of electrodes using different basic electron doses, where 200 μC/cm^2, 350 μC/cm^2 and 800 μC/cm^2 have been assigned for the samples a, b and c respectively. The 12 - 2.5% PMMA bi-layer resist stack has a thickness of approximately 700 nm (12% 650 nm, 2.5% 50nm).

Prior to the metalisation of the patterns, a hydrocloric acid (HCl) de-oxidising treatment is applied for the removal of the surface native oxide. A Paladium-Germanium-Gold based metal alloy is used for the formation of the Ohmic contacts. The use of the Pd/Ge/Au/Pd/Au alloy on highly doped GaAs cap layers has demonstrated the formation of Ohmic contacts with contact resistivity equal to ~$2\cdot10^{-6}$ Ωcm^2 [132]. The thicknesses of the Pd/Ge/Au/Pd/Au layers were 20, 50, 10, 50 and 100 nm, respectively.

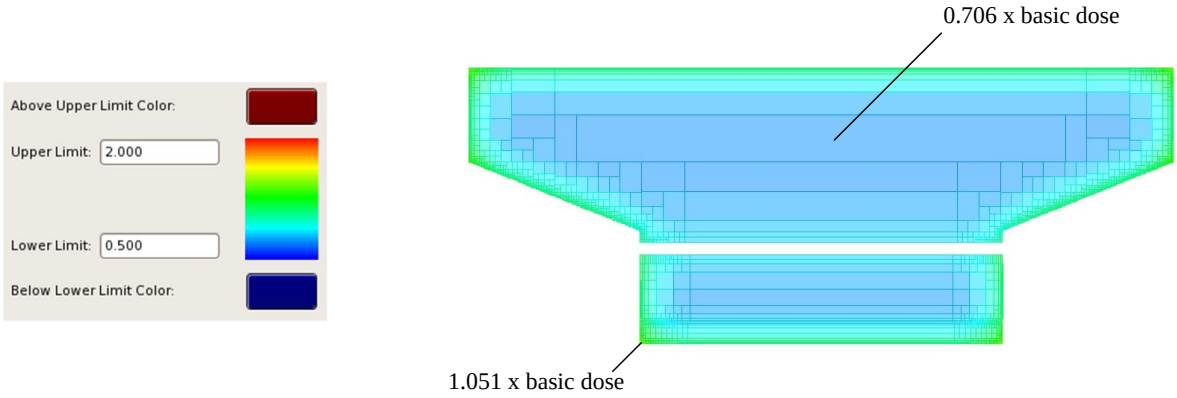


Figure 6.2 Generated areas with variable factors for the proximity error correction.

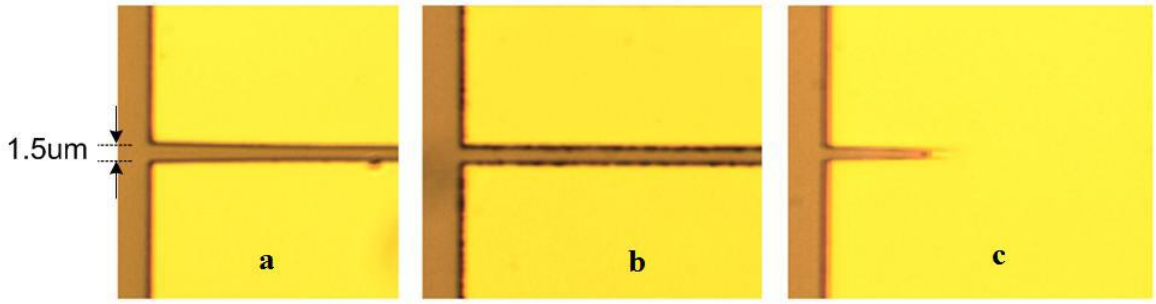


Figure 6.3 Metalised patterns using the proximity error correction and variable basic doses (a : 200 μC/cm^2, b : 350 μC/cm^2, c : 800 μC/cm^2) for a 1.5 μm designed separation.

The Pd content reacts with GaAs and Pd_x-GaAs complexes are created. The perturbation of the GaAs lattice favours the insertion of Ge in the semiconductor, acting as an n-type dopant. As a ramped temperature increment is applied to the material, Pd-Ge compounds are formed, GaAs is regrown including the Ge dopant and Pd is removed from GaAs. A disadvantage of the Pd-Ge contact is the high resistivity presented, which is eliminated by the insertion of Au between the matel layers. The above mechanism, which is known as solid-phase regrowth, provides stable Ohmic contacts up to temperatures near 600^{o}C [133].

A rapid thermal anealling tool was used for the metal diffusion and the formation of the Ohmic contacts as described above. The sample was initially heated linearly up to 320^{o}C and remained at this temperature for 20 s. A second ramped increment, applied for 60 s, brought the temperature to 400^{o}C which is the optimum point for minimum contact resistivity [132].

6.2.3 Mesa isolation

The next step in the fabrication procedure of planar Gunn diodes is the isolation of the active layers from the surrounding areas on the semiconductor. Thus, short-circuit connections between different nodes of the same device or between different devices, are prevented. A layer of UVIII is used as an e-beam resist for the protection of the mesa areas during the removal of the active layers from the surrounding areas.

The etching solution used for the mesa isolation, constists of a citric acid / hydrogen peroxide mixture ($C_6H_8O_7/H_2O_2$). In this solution, H_2O_2 acts as the oxidising agent creating surface oxides and the acidic ingredient attacks and dissolves these oxides. The $C_6H_8O_7$:H_2O_2 solution is mixed in 10:1 stoichiometry, providing sufficient etch rates for the removal of InGaAs, GaAs and AlGaAs [76].

The complete removal of the active layers is checked between the etching steps by electrical measurements on the areas to be etched. A breakdown voltage of approximately 30 V, and a current lower than 100 nA, are some typical targets after placing the probes on the semiconductor separated by ~5 μm. A profilometer is also used to ensure that the etched depth is higher than the total thickness of the active layers.

6.2.4 CPW pads and composite contacts

CPW pads

The evaporation of the CPW pads is perfomed after the mesa isolation, providing an interface between the Gunn diodes and the test equipment for the DC and the RF characterisation of the devices. The geometry of the pads is selected in a way that the coplanar waveguides present a characteristic impedance of 50 Ω according to the formulas of Section 3.2. The access pads of every component in this work adopt a configuration with a 40 μm ground-signal gap W and a 60 μm signal pad width S. This geometry provides compatibility with the 50 Ω / 100 μm-pitch RF probes of the laboratory.

Figures 6.4 and 6.5 present the fabrication development of the planar Gunn diode after the implementation of the Ohmic contacts, the isolation of the mesa island and the evaporation of the CPW pads.

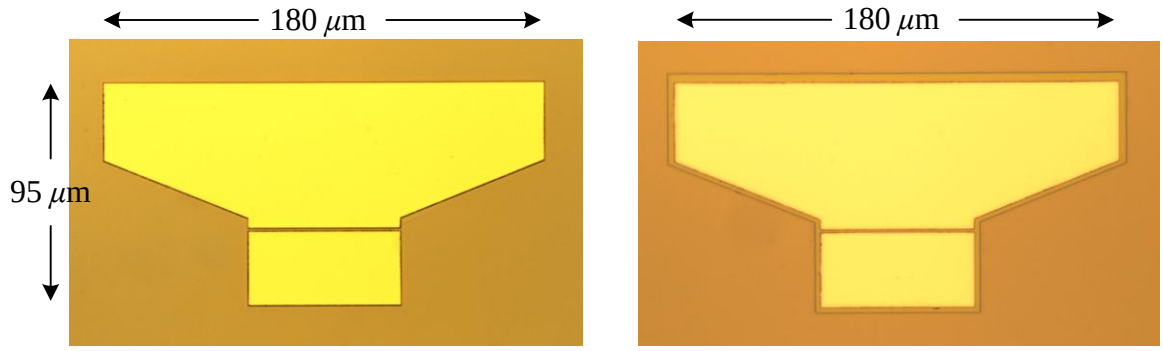


Figure 6.4 Fabricated Ohmic contacts (a) and mesa isolation (b) for a device with 1.3 μm L_{ac} and 60 μm width.

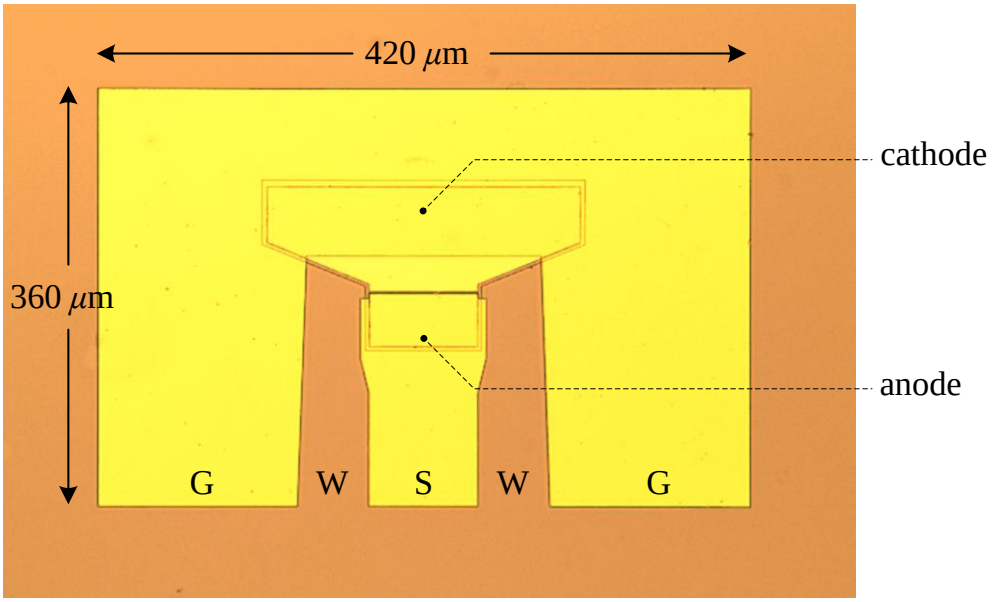


Figure 6.5 Optical picture of the 1.3 μm / 60 μm device after the evaporation of the CPW pads.

Composite contacts

During the ealy-stages of the planar Gunn diode developement, the devices presented limited reliability. This was caused by breakdown failures appearing close to the biasing point where the diodes generate oscillations. This problem is caused by the high electric field appearing at the edge of the anode contact. The Gunn domain approaching the anode electrode follows the path with the lowest total resistance, entering the metal within a very narrow area where

electric field spikes appear. This phenomenon does not exist in vertical configurations where the current is spread out across the whole contact area.

The reliability of the planar Gunn diodes was significantly increased after the introduction of the composite contact design [98]. This solution adopts a hybrid contact design, where the conventional Ohmic contact is combined with a Schottky extension as illustrated in Figure 6.6(b). In this approach a fraction of the high energy dipole is dissipated in the high-resistive Schottky area and the rest enters the Ohmic contact. The current is therefore spread across a larger area and the electric field is reduced at the edge of the contact. The extension of the Ohmic contact is 0.3 μm, combining a low contact resistance with a high breakdown voltage. Experimental results showed that the breakdown voltage was increased by 1 V for 1.3 μm devices after the introduction of the composite anode contact. The extension of the maximum bias voltage by 1 V is signifficant considering that devices with 1.3 μm L_{ac} start oscillating at voltages as small as 3.5 V [98].

The Schottky extension of the composite contact can be implemented by a Ti / Au metal alloy. Thus, the same metal layer stack of Ti 20 nm / Au 500 nm is used for the fabrication of both the Schottky contact and the CPW pads. The Ti layer is also required for the implementation of the CPW pads, providing an adhesion interface between Au and the semiconductor. The layout pattern is simply modified with the signal pad overlapping the active area by 0.3 μm.

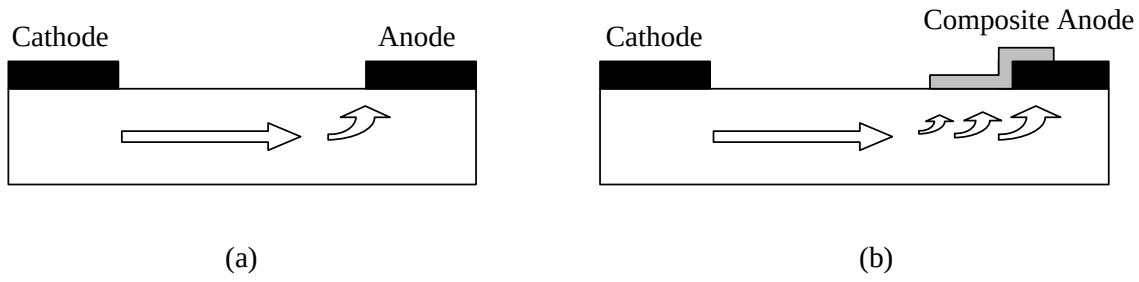


Figure 6.6 Schematic representation of the conventional Ohmic contacts (a) and the composite Schottky anode contact (b) [98].

6.2.5 Recess etching processing

The final and most important step in the fabrication procedure of planar Gunn diodes is the recess etching where the GaAs/InGaAs cap layer between the electrodes is removed. This is a

very delicate process which strongly affects the device performance. The etching of an insufficient portion of the cap layer will cause the current to flow through the surface of the material without entering the channel layer and no oscillations will occur. At the other extreme, a possible over-etching of the material can cause the creation of a depletion region that extends bellow the channel. In such cases, the current level is very low and the Gunn domain has not enough strength to grow.

Recess etching tests using a citric acid solution

Initial fabrication tests were undertaken using a C341 wafer for the experimental examination of the challenges that may appear during the process of planar Gunn diodes. The implementation of the electrodes, the mesa isolation and the CPW pads were performed according to the techniques described previously. No resist mask is required for the etching of the cap layers where the anode and cathode pads determine the area that is exposed to the etching solution. A citric acid solution ($C_6H_8O_7$:H_2O_2) with 3:1 stoichiometry was applied for the removal of the unwanted layers. This mixture presents high selectivity for the removal of GaAs/InGaAs over the $Al_{0.8}Ga_{0.2}As$ etch-stop layer [76, 77]. The test sample was cleaved into two pieces and the etching treatment was applied to each one for different time periods.

Figure 6.7 presents the reduction process of the Gunn diode current for the first test piece of the C341 wafer, during a stepped etching process. The device has 4 μm L_{ac} and 60 μm width. A compliance current of 100 mA was set to protect the test equipment from burning out. A HCl:H_2O solution with 1:4 stoichiometry was initially applied for 30 s for the deoxidation of the surface. The sample was then treated with the citric acid solution progressively for 5 s during each step. After 20 s of acidic treatment, a considerable volume of the cap layer had been removed and the current presented a significant reduction for each additional step. After 25 s the device presented a peak current equal to 55 mA and approximately 38 mA after 30 s. Smaller steps were applied afterwards, having ~25 mA as a target current level according to the reported results for the C341 wafer [96]. The devices however were damaged after the application of the etching solution for an extra time as small as 1 s. Further measurements across the first test wafer indicated that the devices were over-etched regardless of their position on the wafer.

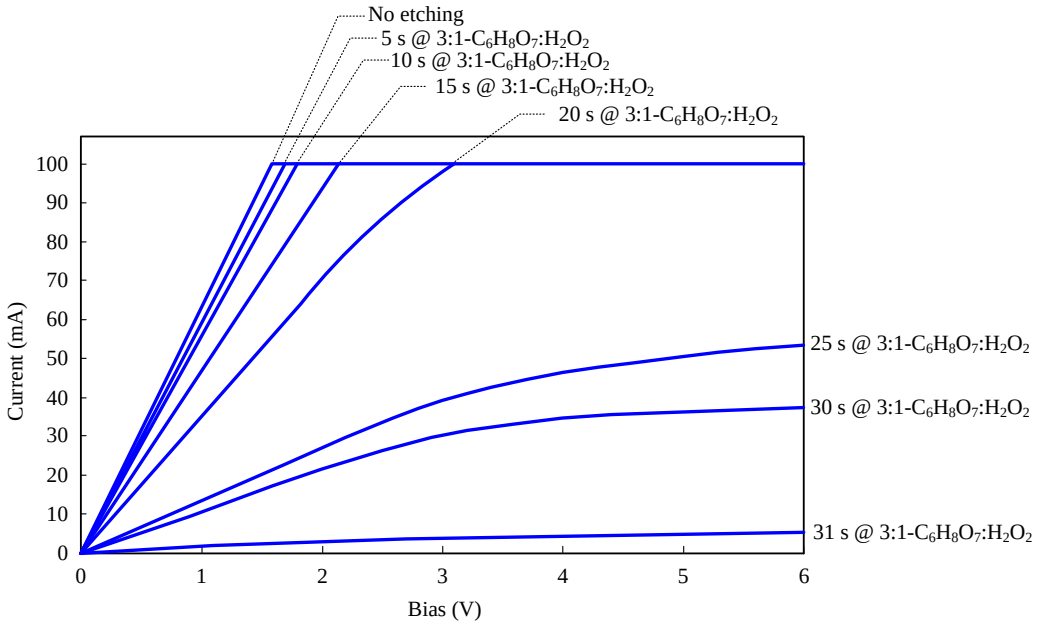


Figure 6.7 Results of the first test wafer showing the reduction of the device current for a 4 μm / 60 μm diode after applying a stepped recess etching treatment.

A second test was conducted afterwards using the second test sample, following a similar stepped etching procedure as described above for the first sample, using the same etching mixture. The results of the second test are illustrated in Figure 6.8 for a 4 μm / 60 μm device. In this test, the current reduced below the compliance level rapidly, after just 10 s of treatment with the same solution. In the same figure, the current level of a second diode with the same geometry is depicted for comparison. The devices were over-etched after only 15 s of citric acid treatment.

There are several conclusions resulting from the recess etching tests. During the first test, the devices were over-etched after just 1 s of extra exposure to the etching solution. Therefore, the citric acid mixture appears to be an aggressive solution for the current material system, presenting limited accuracy in the control of the etching depth. The current level of the devices processed in the second test was reduced by a significantly higher rate in comparison with the first test, even though the same etching solution was applied in both cases. In addition, as presented in Figure 6.8 different devices with the same geometry presented dramatically different current levels for the same etching time.

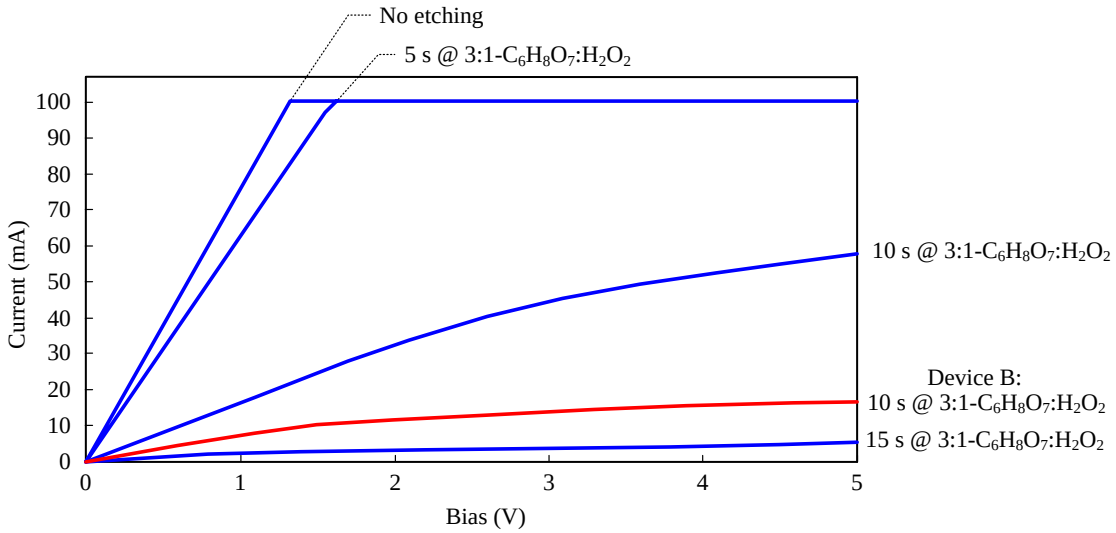


Figure 6.8 Results of the second test wafer presenting the reduction of the device current for two different 4 μm / 60 μm diodes.

There is a number of reasons reported in the literature that could explain the large variations in the etch-rates. The etch rate of citric acid solutions for GaAs, AlGaAs and InGaAs increases exponentially as temperature rises [134, 135]. However, it is expected that temperature reaches a peak value immediately after the preparation of the solution due to the interaction of citric acid with hydrogen peroxide. The temperature of the solution decreases as time passes, reaching an equilibrium value after several minutes. This hypothesis was proved experimentally by measuring the temperature after preparng the solution. Thus, the etch-rate is expected to decrease instead of increasing as observed in the tests performed. It is recommended that the mixture is prepared 15 minutes before the etching so that there is sufficient time for the solution to return to room temperature [136]. In addition, the selectivity of the etching solutions is usually determined by the comparison of the etch rates that have been measured individually for relatively thick layers of each material. In the case of thin etch-stop layers, such as the 5 nm $Al_{0.8}Ga_{0.2}As$ layer of this example, carriers can diffuse easily through the material. Thus, the etch-stop layer can be dissolved at significantly higher rates than measured for the thick test samples.

A possible solution for the reduction of the etch-rate is the dilution of the etching solution with water to reduce the $C_6H_8O_7$:H_2O_2 concentration. However, this could cause

unpredictable variations to the pH which strongly influences the selectivity of the mixture [136].

An additional effect that could potentially damage the devices during the etching procedure is the presence of the trench profile close to the mask edges. This phenomenon is depicted in Figure 6.9 where the vertical profile increases around the area of the mask edge. The effect is strongly dependent on the age of the solution, where the trench can be 50% deeper near the mask edge 20 minutes after the preparation of the mixture. The trench-prone etch is expected to cause the non-progressive reduction of the Gunn diode current, as the reduction rate was increased rapidly during the etching process.

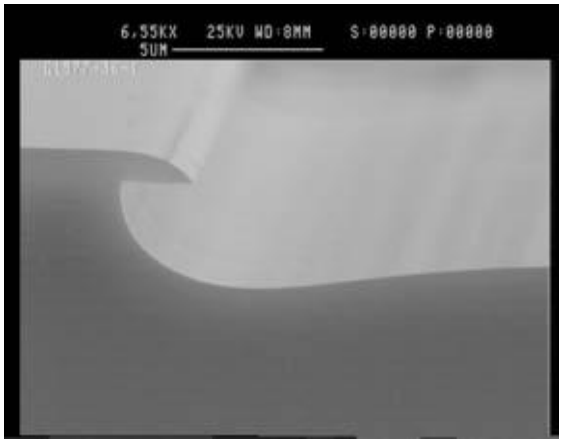


Figure 6.9 Trench profile appearing close to mask edges [136].

A more reliable etching technique is required where a lower etch rate would provide greater control of the etched depth. The new technique should also present uniformity across the etched areas and very small variations of the etch rate over time.

Recess etching tests using a succinic acid solution

The succinic acid-based solution presents a high selectivity of etching GaAs over $Al_xGa_{1-x}As$ etch-stop layers. The selectivity increases monotonically with the pH of the solution [78] and practically zero etch rates have been reported for $Al_xGa_{1-x}As$ etch-stop layers with aluminium mole fraction x greater than 0.8 [78, 137]. The etch rates for GaAs and InGaAs are in the order of 150 nm/min and 40 nm/min, respectively [137, 138] where negligible variation in the etch rate of InGaAs have been reported for a wide temperature range between 22-30^{o}C [138].

The use of succinic acid has also demonstrated exeptional results for the selective removal of GaAs/InGaAs cap layers for the implementation of T-gate pHEMTs [139]. According to these specifications, succinic acid is expected to remove the GaAs/InGaAs cap layer with high selectivity over the AlGaAs etch-stop layer within aproximately 120 s.

A new set of devices was fabricated on the C230 wafer following the same fabrication steps as described previously, but replacing the final step with recess etching using a succinic acid solution. The Pd/Ge/Au/Pd/Au Ohmic contacts were annealed as described in Section 6.2.2 presenting a contact resistivity of 0.19 Ω.mm. For the purposes of the new recess etching test the succinic acid powder was initially mixed with hydrogen peroxide and diluted in water. Ammonium hydroxide was added afterwards in small steps to adjust the pH to 5.9. Within a few minutes the solution was stabilised to an equilibrium room temperature of ~22.5^{o}C. The conventional HCl acid solution was applied prior to the recess etching for the deoxidation of the surface. The sample was treated afterwards with the succinic acid solution in short steps having ~40 mA as a target current level according to the simulations for the C230 wafer [131].

Figure 6.10 illustrates the procedure of etching the cap layer, monitored by the reduction of the device current for a 1.3 μm / 60 μm Gunn diode. The current level falls below the compliance limit of 100 mA after etching for 95 s. Additional treatment in steps of 5-15 s resulted a relatively small reduction to the current, which is finally set at 37 mA after 126 s of etching.

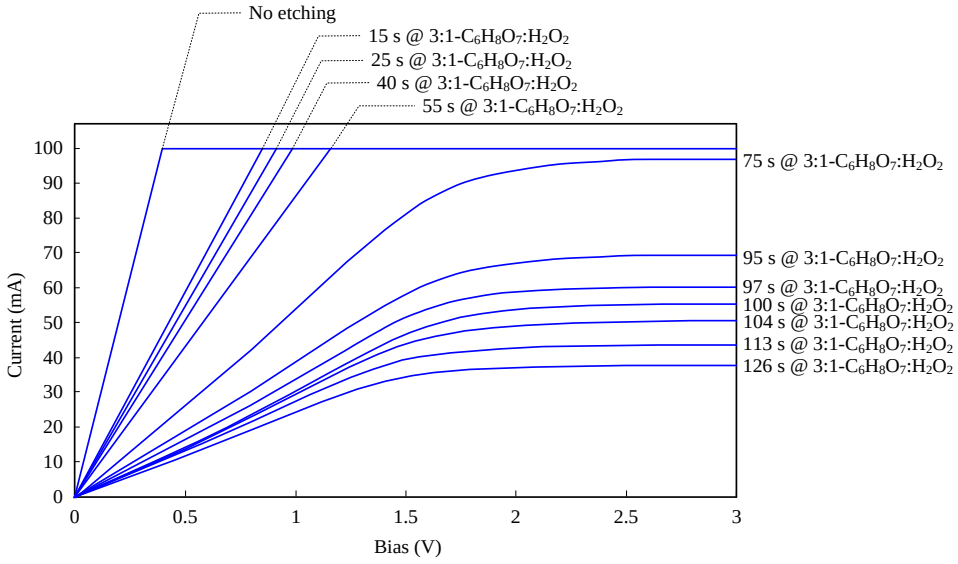


Figure 6.10 Reduction of device current for a 1.3 µm / 60 µm diode after applying a stepped recess etching treatment using succinic acid.

Figure 6.11 depicts the final current level for 8 devices fabricated across the wafer with the same 1.3 μm / 60 μm geometry. The reults indicate very good uniformity of the etching process using the succinic acid solution, considering the variations caused by the imperfections of the semiconductor. The devices present a median current of 43 mA with ± 6 mA variation.

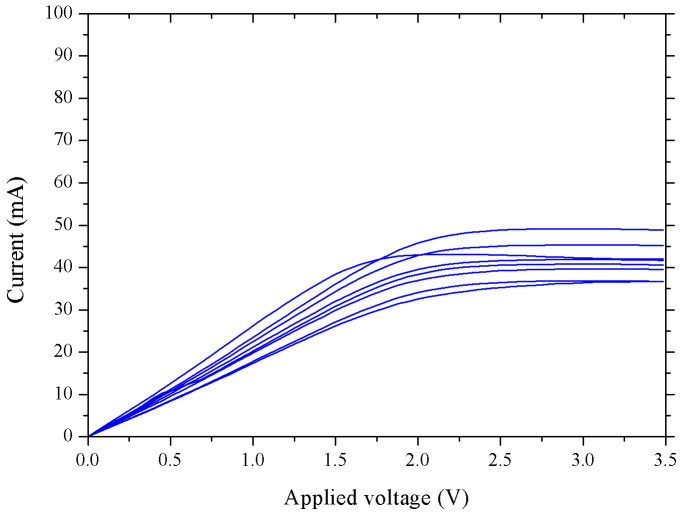


Figure 6.11 Current - voltage characteristics for a group of eight devices with the same geometry (1.3 μm / 60 μm).

6.2.6 Results

A set of operating Gunn diodes with 60 μm width and variable L_{ac} from 1.3 μm to 4 μm was fabricated using the succinic acid solution on the C230 wafer. VNA characterisation was performed for the initial detection of oscillations. Figure 6.12 presents the oscillation frequency as a function of L_{ac} for the devices fabricated using succinic acid. The oscillation frequency presents a large variation between devices with the same geometry, decreasing monotonically with the L_{ac}, as expected. Although a maximum frequency of oscillation above 100 GHz is expected for 1.3 μm L_{ac} [9], such high frequencies resulted from the devices with a slightly shorter channel and 1 μm L_{ac}.

Figure 6.13 illustrates the current-voltage characteristic for a 1.3 μm / 60 μm planar Gunn diode. The device presents an NDR for an applied voltage between ~2.0-3.5 V. For biasing above 3.5 V the majority of the electron population lies in the *L*-valley and the device presents again a positive differential resistance. The $|S_{11}|$ response for the same device is

presented in Figure 6.14 for various biasing voltages. In agreement with the theory of the Gunn effect, the oscillation frequency decreases for an increasing biasing voltage.

In conclusion, oscillating planar Gunn diodes were successfully fabricated using the succinic acid solution for the execution of the recess etching. The mixture presents advanced uniformity in comparison with the citric acid solution. The lower etch-rate provides better control during the removal of the cap layer and the reduction of the device current where no over-etched devices resulted from this process. The oscillation frequency of the diodes increases for shorter devices, presenting however a relatively high variation.

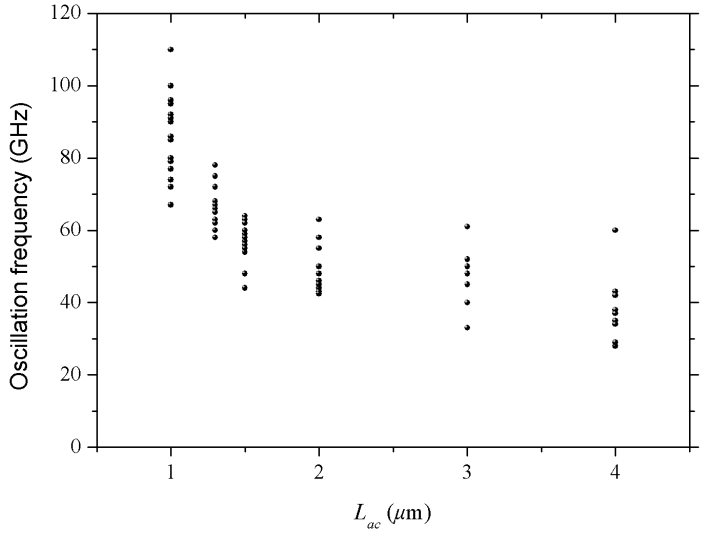


Figure 6.12 Oscillation frequency as a function of L_{ac} for devices fabricated using succinic acid on the C230 wafer.

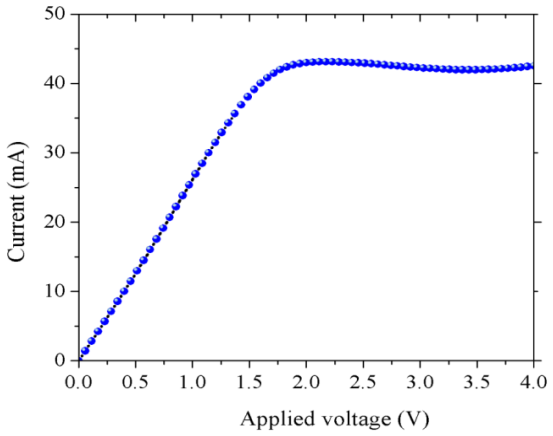


Figure 6.13 Current-voltage characteristic for planar Gunn diode with 1.3 μm L_{ac} and 60 μm width.

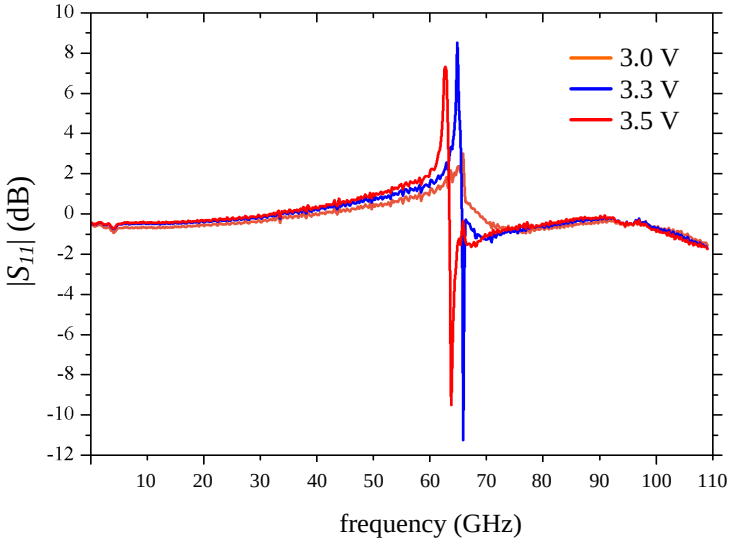


Figure 6.14 $|S_{11}|$ response for a planar Gunn diode with 1.3 μm L_{ac} and 60 μm width, under various biasing conditions.

6.3 Fabrication of pseudomorphic HEMTs on GaAs

6.3.1 Layer structure of the pHEMT wafer

Following the fabrication of oscillating planar Gunn diodes, the implementation of HEMTs was examined using conventional or developed fabrication techniques. The layer structure of the wafer used for this purpose is illustrated in Figure 6.15. The layer structure is similar to the one presented in Section 2.6.1, with the introduction of some additional features. A surface buffer layer of GaAs beneath the etch-stop layer prevents a possible extensive depletion of the channel, caused by the oxidised exposed AlGaAs etch-stop layer. GaAs mono-layers are grown between the barrier and the spacer layers, sandwiching the Si δ-doping layer. Hence the Ga atomic surface favours the migration of Si atoms and higher carrier concentrations are feasible in the δ-doping area [140]. The channel consists of an $In_{0.2}Ga_{0.8}As$ strained layer, since $In_xGa_{1-x}As$ compounds present higher mobility and saturation velocity compared to GaAs [19, 20, 26]. An additional development of the conventional HEMT structure incorporates the introduction of super lattice buffers under the channel layer. The super lattices are formed by repeated AlAs/GaAs mono-layers that provide advanced confinement of electrons in the channel [141]. The current wafer has been used for the implementation of 120 nm T-gate pHEMTs with 450 mS/mm maximum transconductance and an f_{max} of 182 GHz [142].

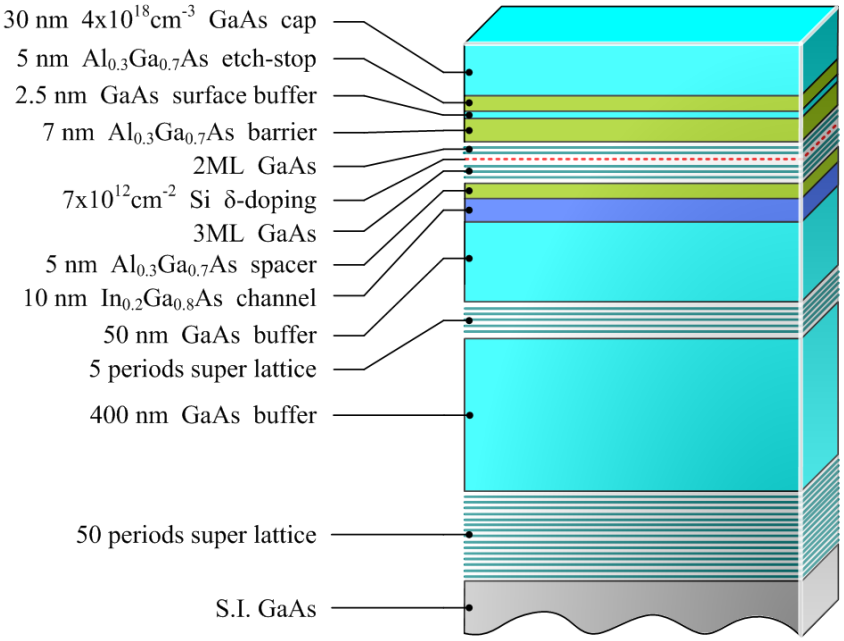


Figure 6.15 Layer structure of the GaAs-based pHEMT wafer.

6.3.2 Ohmic contacts

Initial TLM tests indicated that the Pd/Ge/Au/Pd/Au contact alloy used on the C230 wafer presents high values of contact resistivity, of the order 0.8 Ω.mm. This is probably caused by the absence of the graded InGaAs cap layer which presents a low bandgap surface. Instead the Ni/Ge/Au - based alloy was selected for the current wafer as it is a commonly used solution for highly-doped GaAs layers. Ni is the key element for the formation of low-restive Ohmic contacts on GaAs. Nickel initially reacts with the native oxide of the surface, creating complexes with GaAs afterwards, disturbing the lattice. The Ni_xGaAs complexes allow Germanium to penetrate the semiconductor at temperatures between 100 - 400^{o}C increasing the doping level. A more thermal stable alloy of Au-Ga is created for temperatures above 250^{o}C. The final step of the Ohmic contact formation is the rejection of As to the surface of the contact [133]. At high annealing temperatures bad surface morphology can result due to the transfer of As. This however can be eliminated by using a similar alloy consisting of Au/Ge/Au/Ni/Au [142].

TLM structures with a Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm alloy were evaporated and annealed at various temperatures for the identification of the minimum contact resistivity. The results of the TLM tests are presented in Table 6.1, where the

minimum value is equal to 0.32 Ω.mm. The temperature applied to the current contacts was ramped to 320°C for 20 s and finally set to 400°C for 60 s.

Pd/Ge/Au/Pd/Au		Au/Ge/Au/Ni/Au	
		No An.	No Ohmic
400°C	0.8 Ω.mm	360°C	0.49 Ω.mm
		380°C	0.33 Ω.mm
		400°C	0.32 Ω.mm

Table 6.1 Contact resistance values obtained from TLM measurements.

6.3.3 Mesa etching

The mesa etching of the HEMTs is performed in the same way as described for the planar Gunn diodes. The $C_6H_8O_7$:H_2O_2 solution mixed in 10:1 stoichiometry was used for the removal of InGaAs, GaAs and AlGaAs. However, the UVIII mask presented a degraded resolution for relatively old prepared solutions. As presented in Figure 6.16, rounded corners at the mesa pattern are caused by the limited resolution of the resist. As a result, the gate terminal does not cut effectively the path between the drain and the source and short circuit effects are observed. Thus, a 12% PMMA mask was used instead of UVIII for the protection of the active layers. The resist was hard baked in a conventional oven at 180°C for two hours, getting sufficient resistivity to remain undamaged by the etching solution.

During the mesa etching, a relatively thick layer of semiconductor is removed which is compared to the thickness of the gate metal. The citric acid solution creates a crystallographic profile during GaAs etching, which depends on the orientation of the sample as presented in Figures 6.16 and 6.17. Thus, a discontinuity can be created after depositing the gate metal and the sample has to be orientated correctly before the execution of any processing.

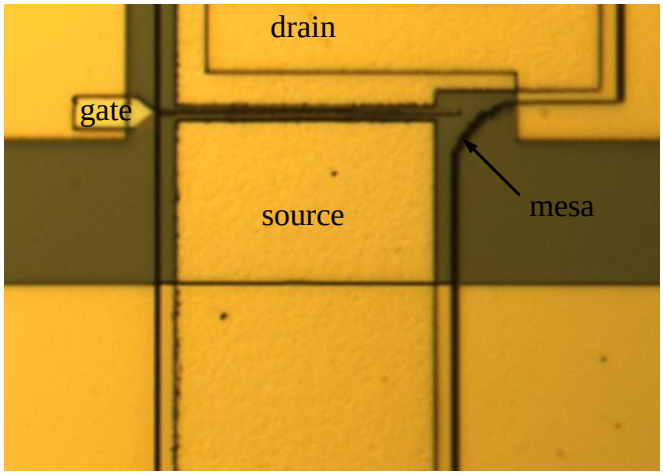


Figure 6.16 Drain-source short circuit caused by degraded UVIII resist.

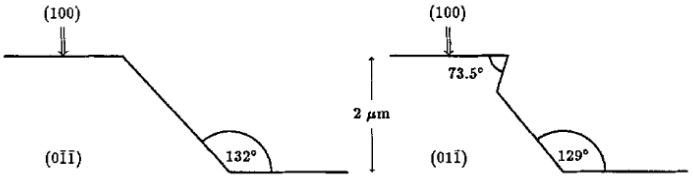


Figure 6.17 Etching profiles of GaAs after etching with 5 : 1 - Citric Acid : H_2O_2 [76].

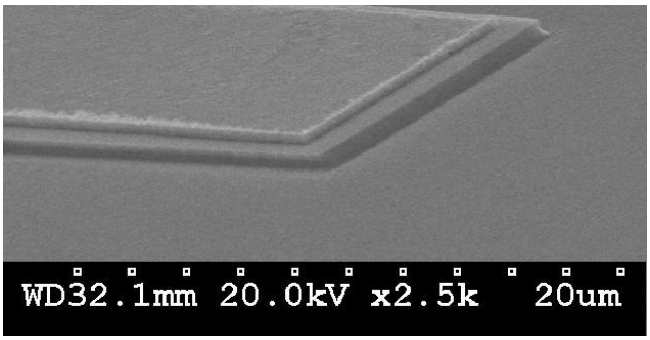


Figure 6.18 The resulting mesa island after etching with 10 : 1 - Citric Acid : H_2O_2.

6.3.4 Fabrication of conventional 250 nm gate devices

The first step for the fabrication of the gate terminal before the metallisation is the recess etching of the cap layer up to the AlGaAs etch-stop layer. This process is similar to the recess etching of the planar Gunn diodes, using the same succinic acid solution with controlled pH at 5.9. A thin metal layer (20 nm Ti/100 nm Au) is deposited prior to the fabrication of the gates to form the required test pads for monitoring the etching process.

Several test devices were measured during the process where the reduction of the I_{DS} current was used to monitor the progress of the etching. After few etching steps of approximately 5 s, the test devices presented ~40 mA of I_{DS} and no further reduction of the current was observed with additional etching. This was caused by the collapse of the narrow PMMA gate window during the measurements. As the devices conduct current, the temperature increment causes the PMMA mask to melt and no further etching occurs for the test transistors. At the same time, the actual devices that are not monitored have been over-etched and damaged. Figure 6.19 presents the gate area of a test transistor after the metallisation process. The gate line does not exist and only the gate feed has been metallised properly.

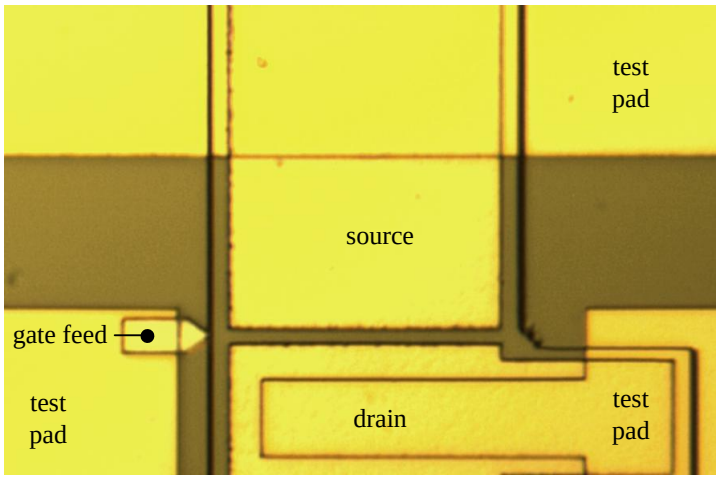


Figure 6.19 Closing of the gate window during the recess etching.

A second fabrication cycle was performed for the implementation of the gate terminals. For the purposes of the new test, the sample was cleaved into two pieces after the development of the gate windows. The first sample included an array of test devices that were sacrificed during the etching test. After each etching step a new group of devices is measured, avoiding the misleading monitoring that is caused by the closed gate windows. The reduction of the drain current after the stepped etching process is illustrated in Figure 6.20. After 30 s of etching treatment, the devices were over-etched presenting very low current.

According to previous results for the current wafer [143] 400 mA/mm is a target current level when 0 V bias is applied at the gate. Thus, for the one-finger 50 μm-wide devices of this test, the resulting 20 mA target current corresponds to approximately 15 s of etching treatment.

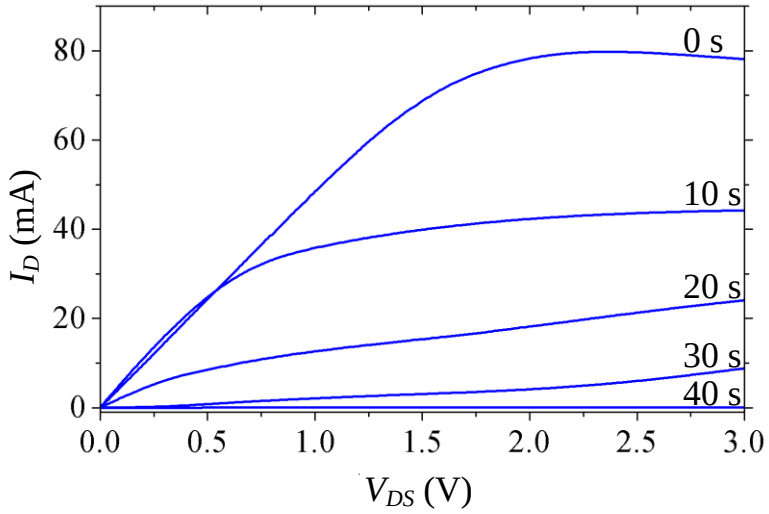


Figure 6.20 Reduction of the drain current for the 50 μm wide test transistors with 250 nm gate length.

After the test etching, the second piece of the wafer was etched for 15 s continuously. The gate metallisation was performed afterwards, consisting of a commonly used Titanium / Platinum / Gold alloy (Ti 15 nm / Pt 15 nm / Au 400 nm). The Ti layer provides a good adhesion interface between the metal and the semiconductor, presenting at the same time a good Schottky contact. The intermediate Pt layer prevents the diffusion of the top Au layer into the semiconductor, which would increase the contact conductance. Finally, a thick layer of Au is deposited on the top of the stack providing a low-resistive access to the Schottky contact [144]. After the metallisation of the gate a Ti 20 nm / Au 500 nm layer was deposited to form the CPW test pads. Figure 6.21 presents the SEM image of a complete fabricated pHEMT with 50 μm width, 250 nm gate length and 0.8 μm drain-to-source separation.

Figure 6.22 presents the current-voltage characteristics (I_D - V_{DS}) for a 25 μm wide pHEMT, with 250 nm gate length and 0.8 μm drain-to-source separation, for different voltages applied at the gate. The device presents a maximum current of approximately 480 mS/mm for 900 mV gate bias. The transistor is pinched-off for gate biasing below -100 mV. The transconductance performance of the same device is presented in Figure 6.23. A maximum value of 450 mS/mm results for V_{DS} equal to 1.5 V and V_{GS} of 450 mV. A relatively high positive voltage is required for increasing the channel current density and maximising the device transconductance. This indicates that the gate is slightly over-etched and the device

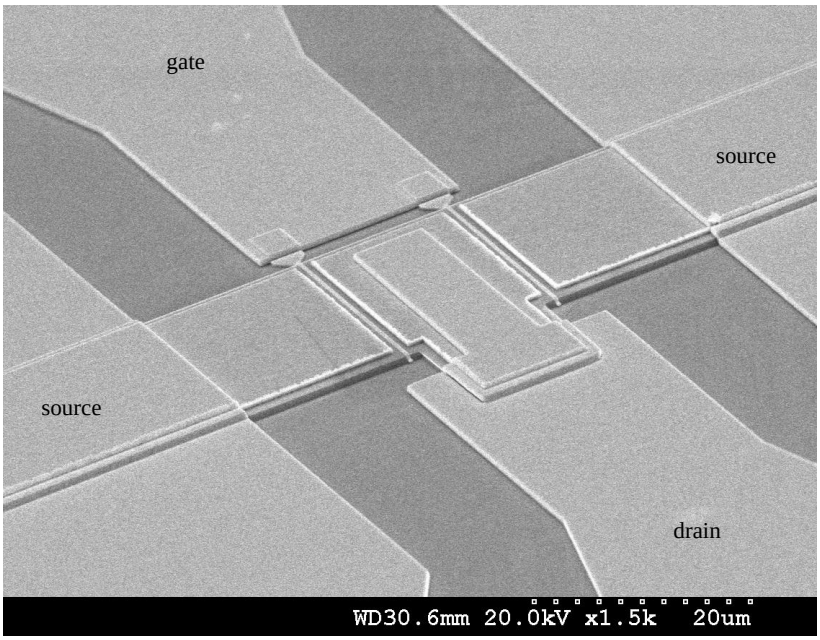


Figure 6.21 SEM image of a complete pHEMT with 50 µm width, 250 nm gate length and 0.8 µm drain-to-source separation.

operates in enhancement mode. In this case, the AlGaAs etch-stop layer is over exposed causing the increased depletion of electrons under the channel layer. The enhancement of the transistor performance is feasible by applying the recess etching treatment for a shorter period. The results however are very encouraging as the DC performance characteristics are similar to the results presented by devices with significantly shorter gates of 120 nm [143].

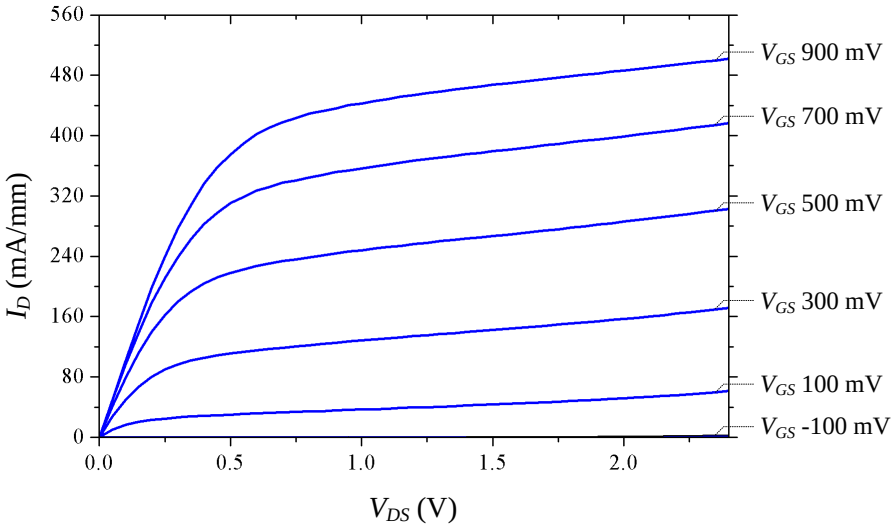


Figure 6.22 I_D - V_{DS} characteristics under variable gate biasing for a pHEMT with 25 μm width, 250 nm gate length and 0.8 μm drain-to-source separation.

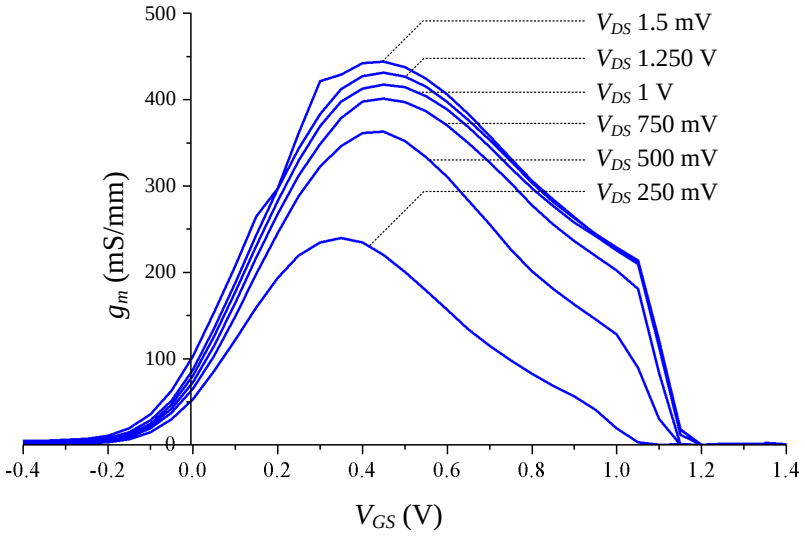


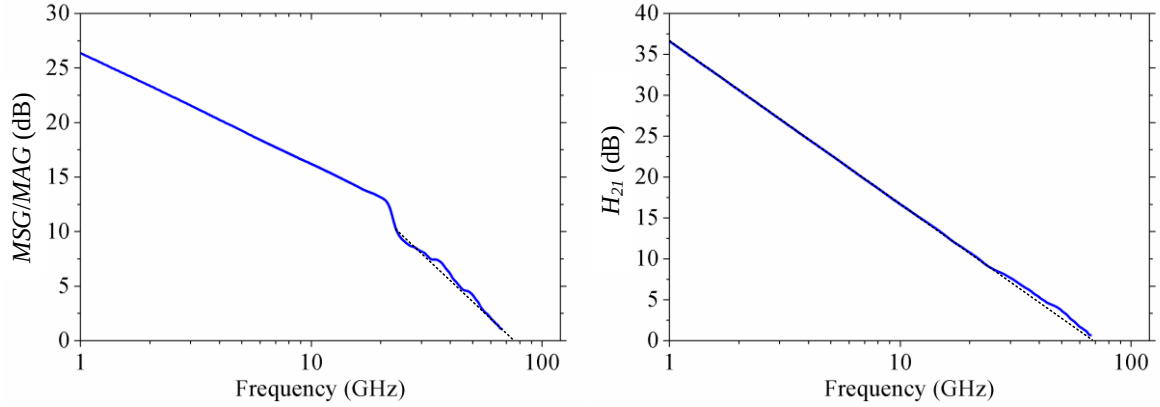
Figure 6.23 Transconductance performance over V_{GS} for variable drain biasing. The dimensions of the pHEMT are the same as in Figure 6.21.

The high-frequency characterisation of the devices was performed using the VNA in the frequency range of 10 MHz - 67 GHz. Figure 6.24(a) presents the maximum stable and the maximum available power gain (*MSG* / *MAG*) as a function of frequency. The operation of the transistor is defined by the stability factor *K* as given by Equation 6.1. For *K* smaller than 1 the device is potentially unstable and can be used for the design of oscillating circuits. In the case of an unstable circuit the value of the gain can reach infinity. For the implementation of amplifiers the transistor has to be connected with the appropriate input-output matching networks, maintaining *K* greater than 1 for the total circuit. In this case, the power gain is given by Equation 6.2 for *K* equal to 1, i.e. $MSG = S_{21} / S_{12}$. For *K* greater than 1 the transistor is unconditionally stable, as desired for the implementation of amplifying circuits, and the power gain is given by Equation 6.2 [145]. The unconditionally stable region of Figure 6.24(a) occurs up to 22 GHz, where the device presents the characteristic "knee" of transition to the unconditionally stable region.

$$MAG = \frac{S_{21}}{S_{12}} \left(K + \sqrt{K^2 - 1}\right) \tag{6.1}$$

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|} \tag{6.2}$$

By following the -20dB/decade rule, as indicated by the dashed line, the device presents f_{max} equal to ~ 75 GHz. The same rule is used for the identification of f_T, which is equal to ~ 68 GHz as presented in Figure 6.24(b). The high-frequency performance of the transistor is limited due to the increased parasitics introduced by the 250 nm gate. However, the current results are very encouraging considering the reported performance of devices with similar geometries [107].



(a) (b)

Figure 6.24 *MAG* / *MSG* (a) and current gain (b) as a function of frequency for 250 nm-gate HEMTs.

6.3.5 Development of 70 nm T-gate technology

Following the successful implementation of 250 nm gate pHEMTs, the next challenge arises in the fabrication of sub-100 nm T-gates. Considering the design aspects of the HEMT as described in Section 2.6, the shorter gate length is expected to enhance significantly both the DC and RF characteristics of the devices. The T-shaped gate presents reduced capacitance due to the narrow foot print and lower parasitic resistance is inserted by the semiconductor due to the shorter geometry. At the same time, the access resistance to the gate Schottky contact is kept in low levels by using a wide gate "head". The use of T-gate technology is of high importance for the implementation of transistors with sufficient gain in the operation range of planar Gunn diodes, i.e. up to ~100 GHz.

For the implementation of the T-shaped gates the creation of a stepped profile in the resist is required. This has been traditionally created by 3D EBL techniques, where different doses are assigned on a stack that consists of resist layers with different sensitivities. A typical example is the UVIII/LOR/PMMA system [108, 109, 110]. The top UVIII layer is exposed to a very

low dose of electrons and a high electron dose is used to expose the stack up to the semiconductor. In this way, a sharp profile between the "foot" and the "head" areas is created due to the high contrast between the sensitivities of the two layers. The intermediate LOR layer is used to prevent the two layers from intermixing. Due to the increased degradation of the UVIII resist that was observed during the mesa etching, as described in Section 6.3.3, alternative solutions were explored for the formation of the stepped profile.

In this work a new method was developed for the fabrication of T-gates, using an all-PMMA resist stack. Similar to the traditional techniques, the "foot" and the "head" areas are exposed to high and low electron doses respectively. Thus, the low dose in not enough to expose the total resist stack and PMMA is removed partially after the development. However, the required contrast does not exist between the PMMA layers and the depth of the "head" area varies dependent on time and temperature variations during the development procedure [146]. The solution comes from the introduction of a thin intermediate layer of Aluminium with 10 nm thickness which increases the back-scattering of the electron beam. In this way, a threshold is created by the Al layer and the lower PMMA layers are under exposed from relatively low doses. On the other hand, a high dose is needed in the middle of the pattern in order to penetrate the Al layer and expose the bottom layers down to the substrate.

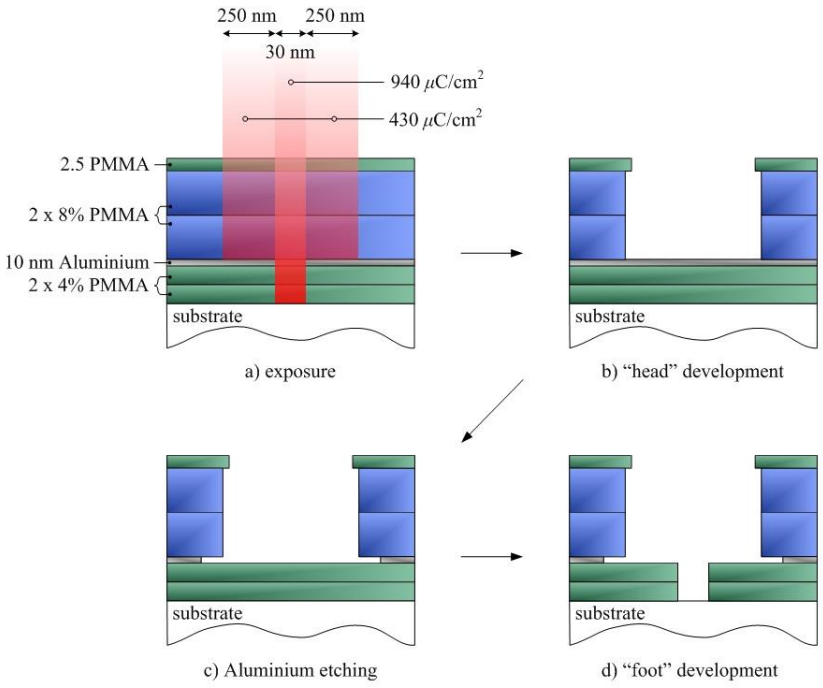


Figure 6.25 Schematic diagram of the PMMA/Al based T-gate technique.

The complete PMMA/Al stack is illustrated in Figure 6.25(a). Two layers of low-sensitivity 4% PMMA resist are deposited initially, composing a bi-layer with ~200 nm total thickness. The 10 nm Al layer is evaporated afterwards. A bi-layer of 8% PMMA with ~400 nm thickness is spun for the formation of the "head" area. The top 2.5% PMMA resist layer is used for the creation of the under-cut profile required for the lift-off procedure. In principle, this technique is expected to present relatively wide "foot" windows due to the increased forward scattering introduced by the multiple PMMA layers and Al. However, this method is simple to implement as only one registration job is required for the e-beam tool and the resist stack consists exclusively of PMMA.

The opening of the T-gate window is performed in 3 steps. An MIBK (info) solution diluted with IPA in 2.5 : 1 - MIBK : IPA stoichiometry is applied for 40 s for the removal of the top three PMMA layers. The Al layer which stops the further development of the bottom PMMA is etched afterwards using a CD-26 solution. This step is the most critical part of the process. The Al layers need to be etched sufficiently in order to open the window for the development of the "foot" area. However, Al is also etched laterally as shown in Figure 6.25(c) and a possible over-etching could cause the complete removal of the top resist stack. Etching tests indicated ~100 s as the optimum etching duration for the removal of Al. Figure 6.26 presents the optical image obtained after the etching of the Al layer where the Al window is extended under the top PMMA window. The ~900 nm-long test structures present excellent uniformity of Al etching along the complete line, ensuring a high fabrication yield. Finally, the bottom PMMA layers are developed after a second treatment with 2.5 MIBK at 23^{o}C for 40 s.

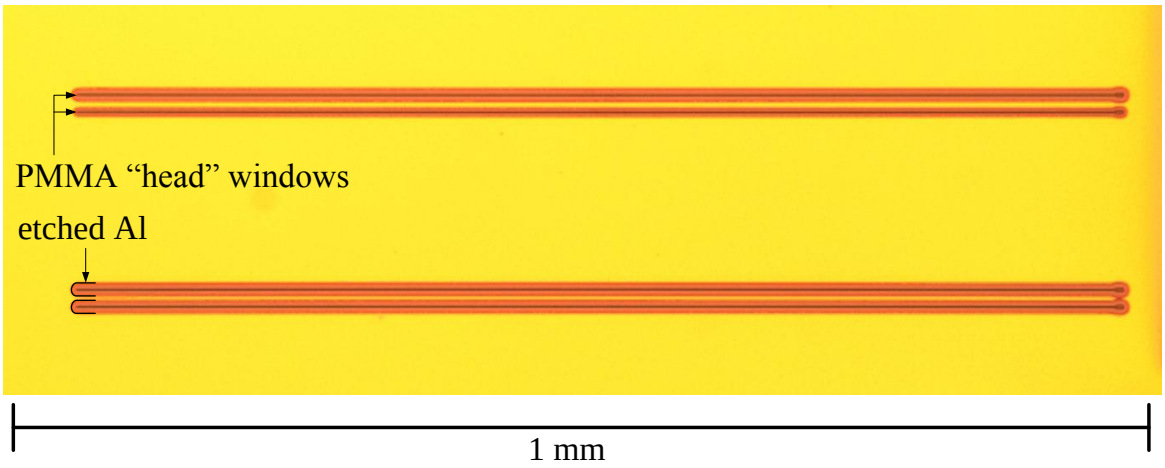


Figure 6.26 Optical image after etching the Al layer.

A set of dose tests were executed for the identification of the optimum balance between the "head" and "foot" dose. The width of the designed "foot" line was also varied to identify the optimum geometry that presents both narrow patterns and high yield. The two side patterns that form the "head" areas were designed with a constant width of 250 nm. For the exposure of the "foot" area, the beam current was 4nA and the VRU was 4. The equivalent values for the exposure of the "head" area were 8nA and 10. Figure 6.27 presents the resulted yield for the various designs of the test. The dose of 430 μC/cm^2 presents the highest reliability for the exposure of the "head" area, while the optimum "foot" dose depends on the foot-line design.

A second dose test was performed with foot-line designs equal to 10, 20, 30, 40 and 50 nm and the developed patterns were inspected in the SEM tool before the metallisation of the T-gate. As expected, the wider designs presented well-defined "foot" windows along the lines. On the other hand, the 10-20 nm line designs present narrow patterns but with limited yield. The foot-lines designed with 30 nm width presented a very good compromise of narrow windows with adequate yield. Figure 6.28(a) presents the SEM image of the resist profile for a 30 nm designed "foot" line. The substrate is exposed clearly for the whole pattern and the "foot" window is ~70 nm wide due to the scattering effects. Figure 6.28(b) illustrates the fabricated T-gate after metallisation. The final geometry and dose design is given in Figure 6.25.

An additional metal layer with 100 nm thickness was deposited on the top of the fabricated T-gates to investigate the capability of the structure to support a self-aligned technique.

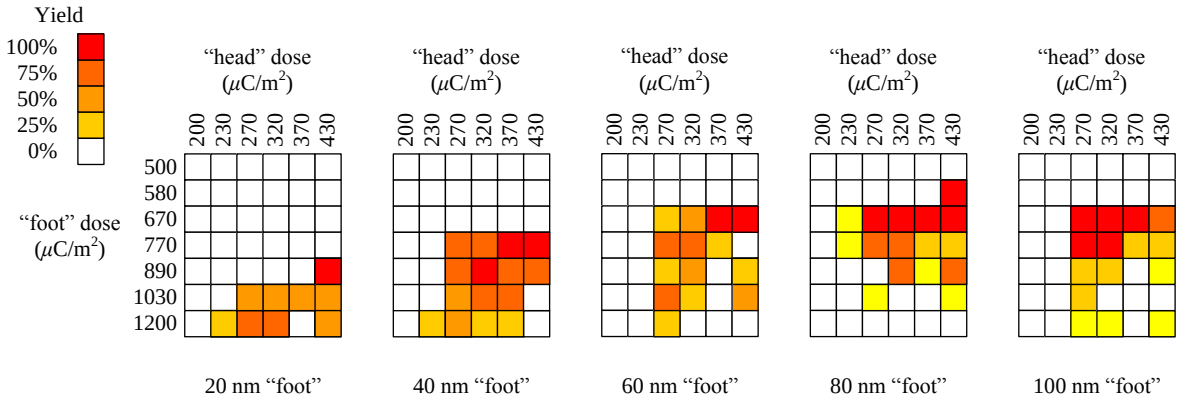
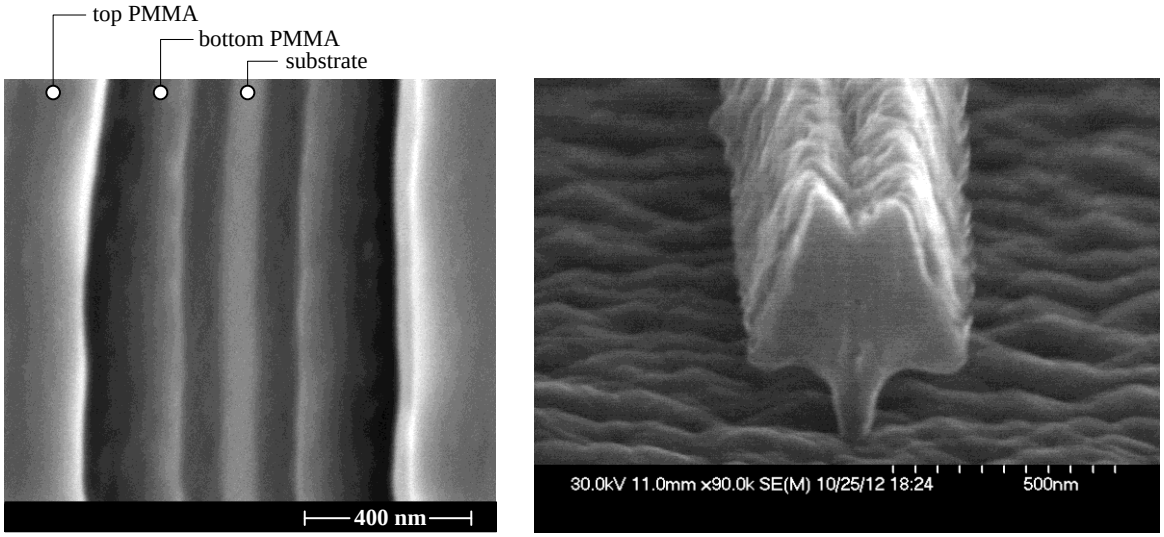


Figure 6.27 Measured yield of the T-gates for various doses and designs.



(a) (b)

Figure 6.28 Resist profile (a) and metallised T-gate (b).

Figure 6.29 illustrates the fabricated test structure, where a sufficient gap is maintained between the T-gate and the contact extension. The isolation of the gate with the contact extension was confirmed after the execution of electrical measurements. Although the above test demonstrates the compatibility of the current T-gate technology with a self-aligned technique, the latter was not applied in this work due to a possible reduction in the fabrication yield [147]. The resistance of the current T-gates was measured equal to 640 Ω/mm.

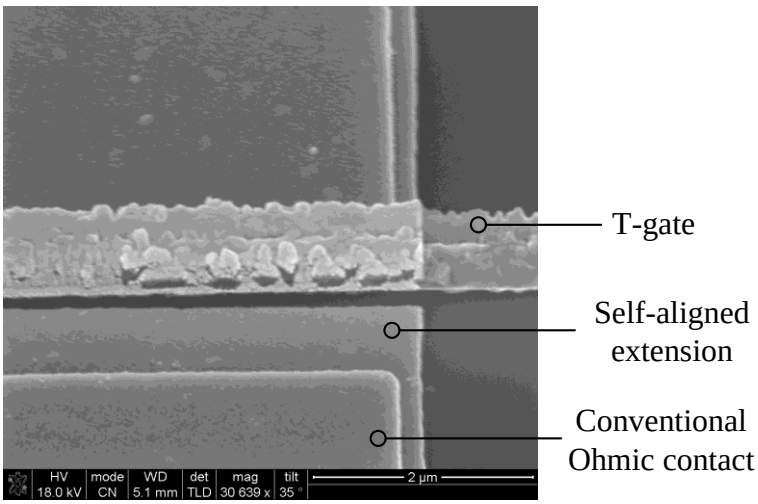


Figure 6.29 Fabricated T-gate with self-aligned extensions of the Ohmic contacts.

6.3.6 Fabrication of 70 nm T-gate pHEMTs

After the development of the 70 nm T-gate technology, a set of pHEMTs was fabricated to evaluate the benefits of the new gate structure. The implementation of the Ohmic contacts and the mesa isolation were performed in the same way as in the conventional 250 nm pHEMTs. An initial test was performed for the identification of the approximate etching time, similarly to the tests presented in Section 6.3.4. The etching tests indicated that approximately 20 s were needed for the removal of the cap layer using the same succinic acid solution with adjusted pH at 5.9.

A second wafer used for the fabrication of the actual devices was cleaved in two pieces after the opening of the T-gate windows. The first piece was etched continuously for 20 s while a shorter treatment of 17 s was applied for the second piece of the wafer. A comparison of the performance for the two different treatments is presented in this paragraph. Figure 6.30 presents the I_D - V_{DS} characteristics under different gate voltages for devices etched for 17 s (blue curves) and 20 s (red curves). Devices etched for 17 s present a small advantage, with ~605 mA/mm maximum drain current at 1.5 V_{DS} and 800 mV V_{GS}, over ~595 mA/mm for the devices etched for 20 s.

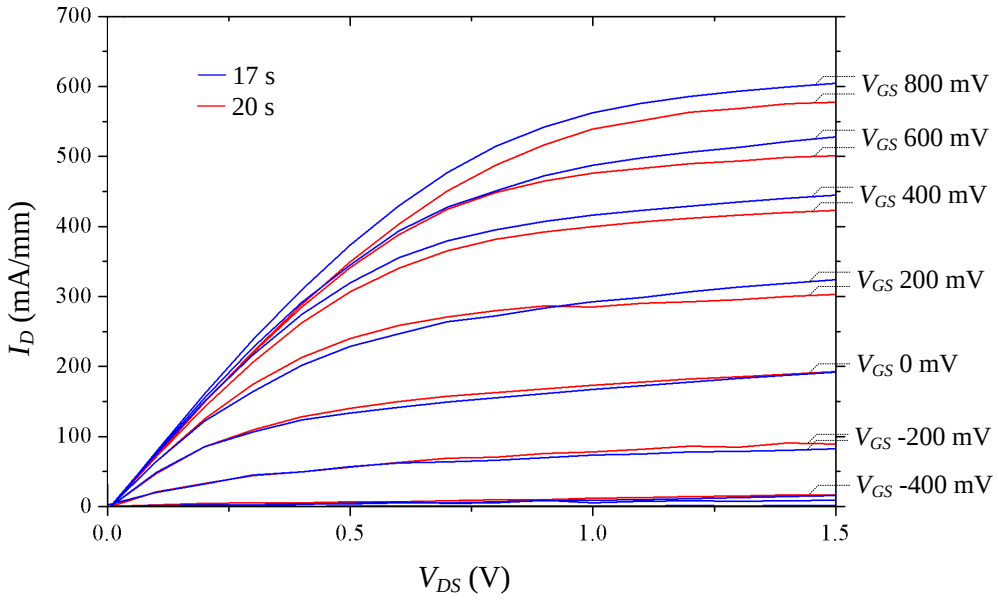


Figure 6.30 Comparison of I_D - V_{DS} characteristics for the 17 s (blue curves) and the 20 s treatment (red curves) for different gate biasing. The 70 nm T-gate devices are 25 μm - wide with 1.5 μm drain-to-source separation.

The transconductance of the same devices is presented in Figure 6.31 as a function of the applied gate voltage V_{GS} for various biasing of the drain V_{DS}. These results highlight the importance of the etching process period. The devices etched for 17 s present a maximum transconductance of 660 mS/mm for V_{DS} equal to 1.4 V. In this case, a gate voltage of 140 mV is required for the maximisation of the transconductance. For the devices etched for 20 s, the depleted region extends deeper in the semiconductor. Thus, a higher voltage equal to 230 mV is required for the attraction of the electrons in the channel. This has an impact on the maximum transconductance which is reduced to 580 mS/mm.

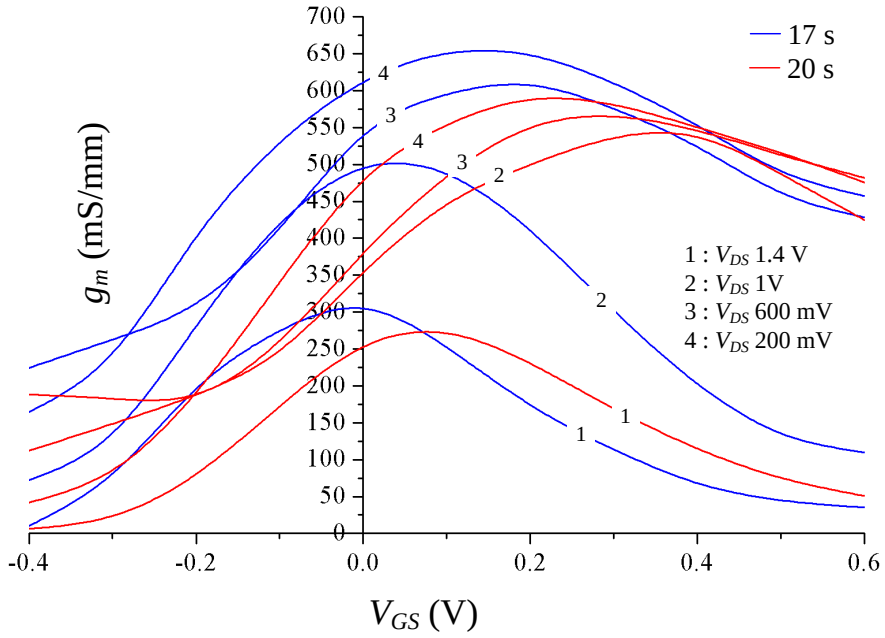
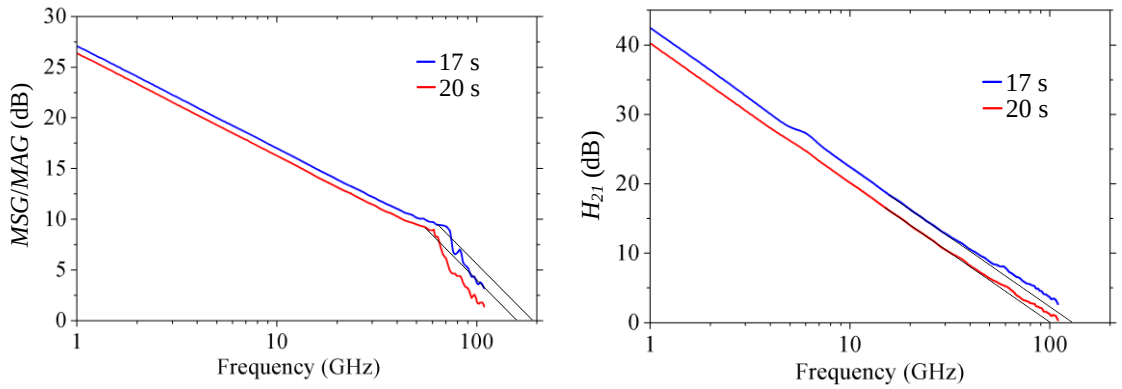


Figure 6.31 Comparison of g_m - V_{GS} characteristics for various drain biasing of the devices etched for 17 s and 20 s. The geometry of the devices is the same as in Figure 6.30.

The comparison of the RF performance for the two solutions is presented in this section. Figure 6.32(a) illustrates the *MAG* / *MSG* as a function of frequency. The higher transconductance of the devices etched for 17 s is transformed to a small gain advantage of ~1 dB. The effect of the longer etching treatment is monitored at the f_{max} of the transistors which is equal to ~190 GHz and ~160 GHz for devices etched for 17 s and 20 s, respectively. Since the solution reaches the etch-stop layer, the lateral etching of the cap layer occurs at a higher rate than the horizontal etching of the etch-stop layer. Figure 6.33 illustrates a schematic diagram of the two scenarios. For the longer etching treatment (dashed lines) a bigger part the etch stop layer has been removed, bringing the gate closer to the channel. In

this way an extended depletion is caused as monitored by the transconductance results. At the same time, the extended lateral etching of the cap layer creates a longer path for the current out of the highly-doped cap layer. The increased parasitic resistance introduced by the channel causes a small degradation in the small signal performance of the devices etched for a longer period. The current gain of the devices is presented in Figure 6.32(b), where a higher gain of ~2.5 dB results for the devices etched for 17 s. Thus, the latter present a higher f_T equal to ~130 GHz over 100 GHz for the devices etched for 20 s.



(a) (b)

Figure 6.32 Device performance; *MAG* / *MSG* (a) and current gain (b) as a function of frequency for devices etched for different periods.

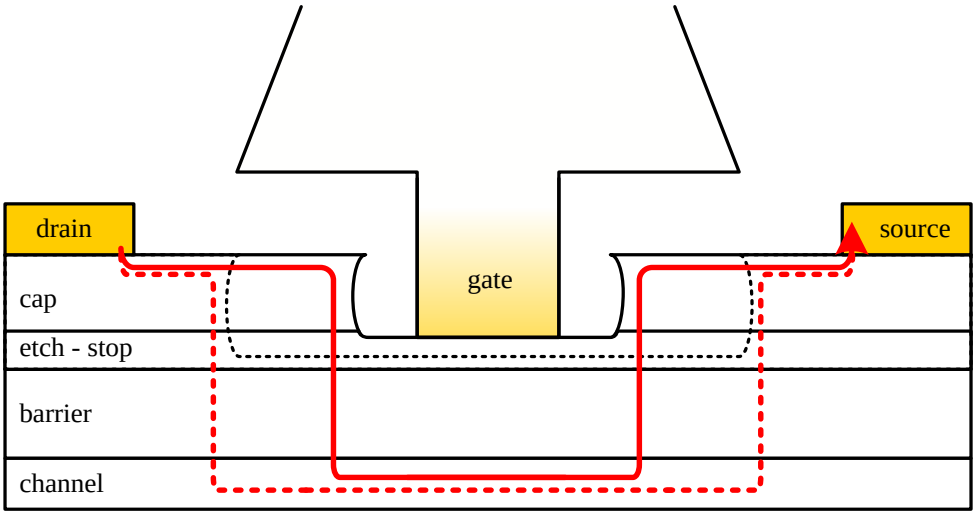


Figure 6.33 The extended etched profile and the different current path for devices etched for a longer period (dashed lines).

6.3.7 Geometry aspects of transistor design

To identify the pHEMT structures with the maximum amplifying capabilities and fabrication yield, a set of experiments was performed using transistors with various geometries. All the devices were fabricated with the 70 nm T-gate technology, etched for 17 s using the succinic acid solution.

Variable drain-to-source separation

The first test incorporates the variation of the separation between the drain and the source (L_{DS}). The fabricated devices have the same width equal to 12.5 μm with 0.8 μm, 1.5 μm and 3.0 μm L_{DS}. Figure 6.34 presents the I_D - V_{DS} characteristics for various gate voltages for the three different geometries. As expected, the maximum drain current is inversely proportional to the L_{DS} with 780, 670 and 600 mA/mm for 0.8, 1.5 and 3.0 μm L_{DS} respectively. The transconductance performance of the same devices is presented in Figure 6.35. A small difference occurs for the two shorter geometries with 760 mS/mm for 0.8 μm and 750 mS/mm for 1.5 μm L_{DS}. Devices with 3.0 μm L_{DS} present limited performance with 650 mS/mm.

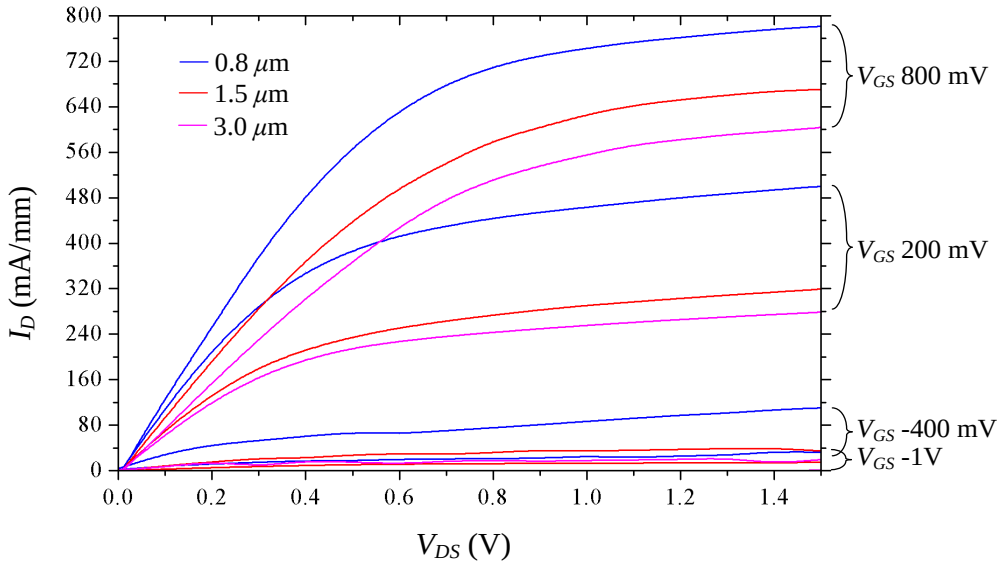


Figure 6.34 Comparison of I_D - V_{DS} characteristics for 0.8 μm (blue curves), 1.5 μm (red curves) and 3.0 μm (pink curves) drain-source separation. The 70 nm T-gate devices are 12.5 μm - wide.

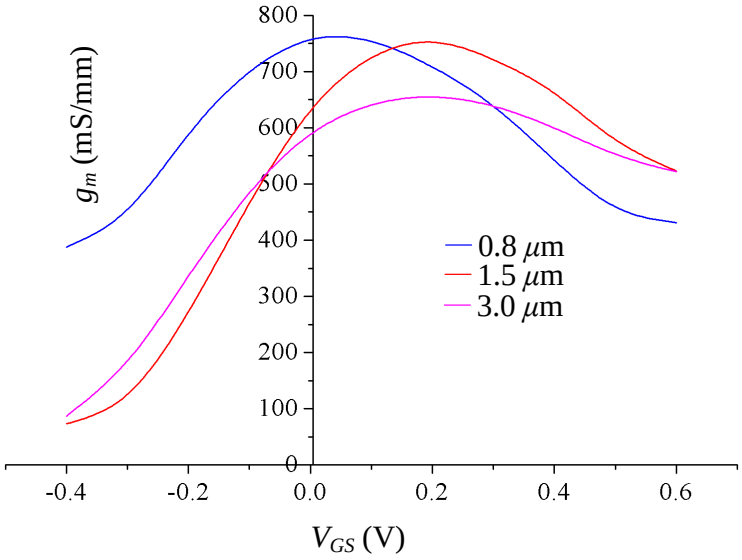
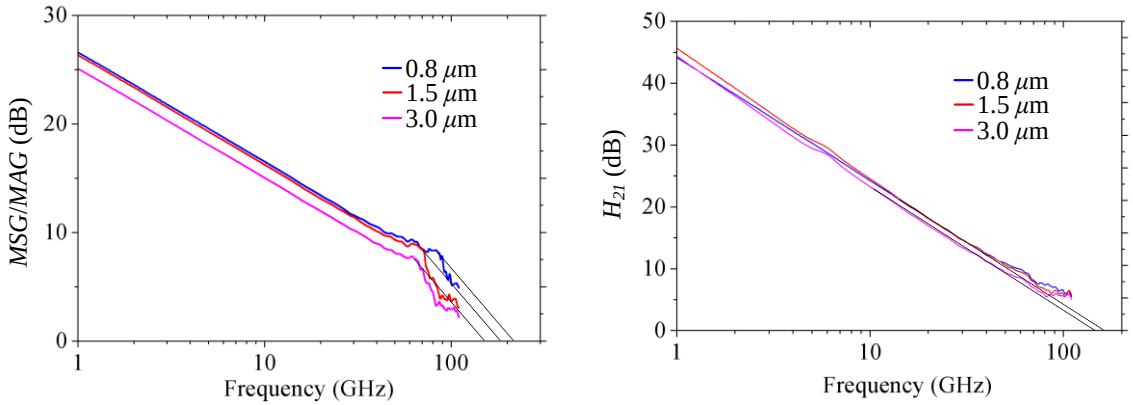


Figure 6.35 Comparison of g_m performance for devices with L_{DS}. The devices are biased at 1.2 V V_{DS}.



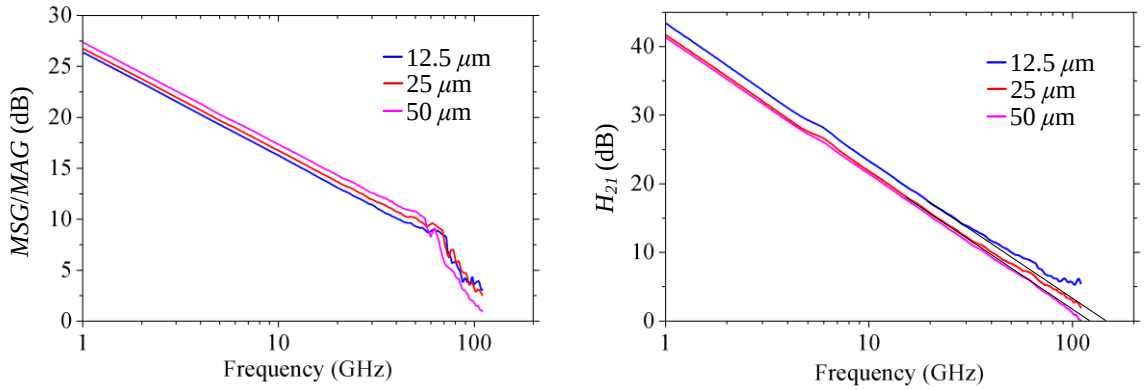
(a) (b)

Figure 6.36 Device performance; *MAG* / *MSG* (a) and current gain (b) as a function of frequency for devices different L_{DS}.

Similarly to the DC results, the devices with shorter L_{DS} present superior RF performance, as illustrated in Figure 6.36. The similar g_m characteristics of the 0.8 μm and the 1.5 μm geometries are translated to the equal *MSG* of the devices as presented in Figure 6.36(a). The maximum frequency of oscillation is equal to 230, 190 and 160 GHz while the cut-off frequency is equal to 170, 170 and 150 GHz for 0.8, 1.5 and 3.0 μm L_{DS} respectively.

Variable width

For the second test, a set of devices with variable width was fabricated where the L_{DS} was constant at 1.5 μm. As expected, the maximum transconductance increases proportionally to the device width with 19, 35 and 61 mS/mm for 12.5, 25 and 50 μm wide devices, respectively. Nevertheless, the main interest is focused on the comparison of the RF performance for the different geometries. As presented in Figure 6.37(a), a similar f_{max} of ~180-190 GHz results for the three devices. The *MSG* increases proportionally to the width of the transistor. However, the parasitic elements C_{GS}, C_{GD} and R_G present higher values as the width of the device increases, degrading the f_{max} and f_T figures of the transistor (Section 2.6.2). This is depicted in Figure 6.37(a) where the "knee" frequency increases as the width of the transistor decreases. The maximum f_T of 150 GHz results from devices with 12.5 μm width and the f_T is ~120 GHz for 25 μm and 50 μm geometries.

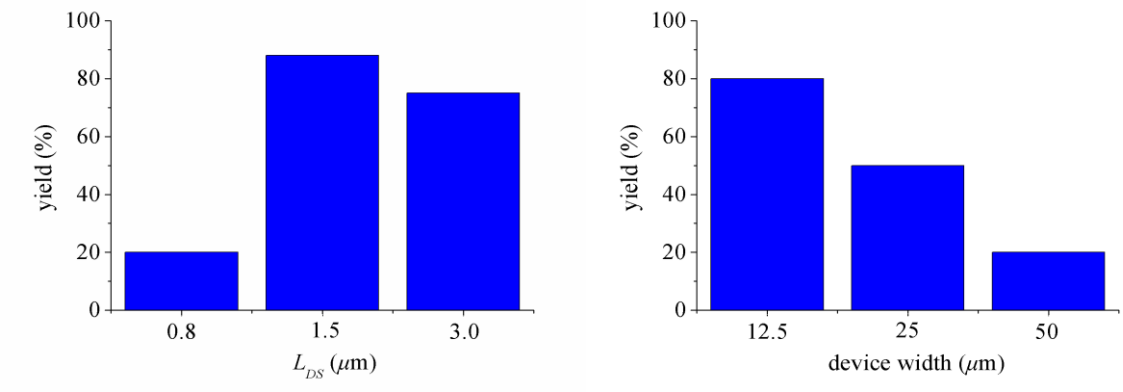


(a) (b)

Figure 6.37 Device performance; *MAG* / *MSG* (a) and current gain (b) as a function of frequency for devices different width.

The fabrication yield for the different geometries presented above is depicted in Figure 6.38. The short L_{DS} possibly causes reduced flatness of the resist layers that are spun on top for the creation of the T-gates. This is depicted in the limited yield that results for devices with 0.8 μm L_{DS}. The wide T-gates are more unstable, accepting larger forces during the lift-off process. This assumption was confirmed by the yield results and optical inspection where a large amount of the 25 μm and the 50 μm T-gates presented bending along the structures.

Since no significant difference results for the *MSG* / *MAG* between the 0.8 μm and the 1.5 μm L_{DS} devices, the 1.5 μm geometry is preferred for the implementation of high-yield MMICs. Regarding the width of the transistor, 12.5 μm devices present a competitive *MSG* / *MAG* over the wider geometries providing advanced fabrication yield.



(a) (b)

Figure 6.38 Fabrication yield as a function of the L_{DS} (a) and the device width (b).

6.4 Chapter summary

This chapter described in detail the existing and developed techniques for the implementation of planar Gunn diodes and pHEMTs. It has been demonstrated that the repeatability of the fabrication procedure for the diodes has been improved significantly after the replacement of the citric acid with a succinic acid solution with controlled pH. Thus, the recess etching of the highly doped cap layer can be performed with slower rates and better uniformity across the wafer. The same etching solution has been used for the recess etching of the pHEMTs, demonstrating the first operating transistors in this work. The high-frequency performance of the transistors has been reinforced after the introduction of a novel 70 nm T-gate technology. The tradeoffs arising for different geometries were also examined in the search for a compromise between sufficient fabrication yield and high performance. Devices with 1.5 μm L_{DS} and 12.5 μm width, presented the highest yield of 80% and maximum frequency of oscillation equal to 190 GHz. After the successful implementation of planar Gunn diodes and pHEMTs on separate wafers, the developed techniques for the co-fabrication of the two devices are presented in the following chapter.

7. Co-fabrication of planar Gunn diodes and HEMTs

7.1 Introduction

This chapter presents the developed techniques for the co-fabrication of planar Gunn diodes and HEMTs on the same substrate. Initially, two different approaches are presented for the implementation of both devices on the same GaAs substrate. The first technique incorporates the combined wafer approach where two groups of layers, optimised for the individual implementation of the devices, are grown on the same substrate. The two layer groups are isolated by a buffer layer grown between them. In the second approach, a single wafer is used for both devices. The single wafer was designed for the realisation of pHEMTs where a compromise has been conducted as there is no optimisation of the layer structure for the Gunn diodes. In the research of alternative ways for the enhancement of the diode performance, a HEMT material system based on InP was also used for the joint realisation of the diode and the transistor. The fabrication procedures followed for each wafer are extensively described in the following sections.

7.2 Co-fabrication on a GaAs combined wafer

The fabrication techniques of planar Gunn diodes and pHEMTs were described individually in the previous paragraphs. In the next section, a combined wafer approach is presented for the implementation of both devices on the same wafer for the first time. A possible integration of the two devices would lead to the significant reinforcement of the oscillator performance. The generated power of the diode would benefit from the use of transistor-based MMIC amplifiers [114, 148], while pHEMT-mixers could be used for the extraction of harmonics at higher frequencies [149]. The successful monolithic implementation of both devices could also be used for the realisation of more sophisticated hybrid circuits, such as MMIC transceivers [150]. The wafer structure of the combined wafer and the fabrication techniques followed are described in detail in the next paragraphs.

7.2.1 Layer structure

The concept of the combined wafer incorporates the growth of two layer groups separated by a thick buffer layer. The two layer groups are optimized individually for the implementation of pHEMTs and planar Gunn diodes. The buffer layer provides the required electrical isolation between the two devices. Figure 7.1 illustrates the combined wafer approach [151]. The pHEMT layers are grown on the top of the structure, whereas the Gunn layers are grown under the GaAs buffer layer. Thus, an accurate etching process is required to access the top of the Gunn layers.

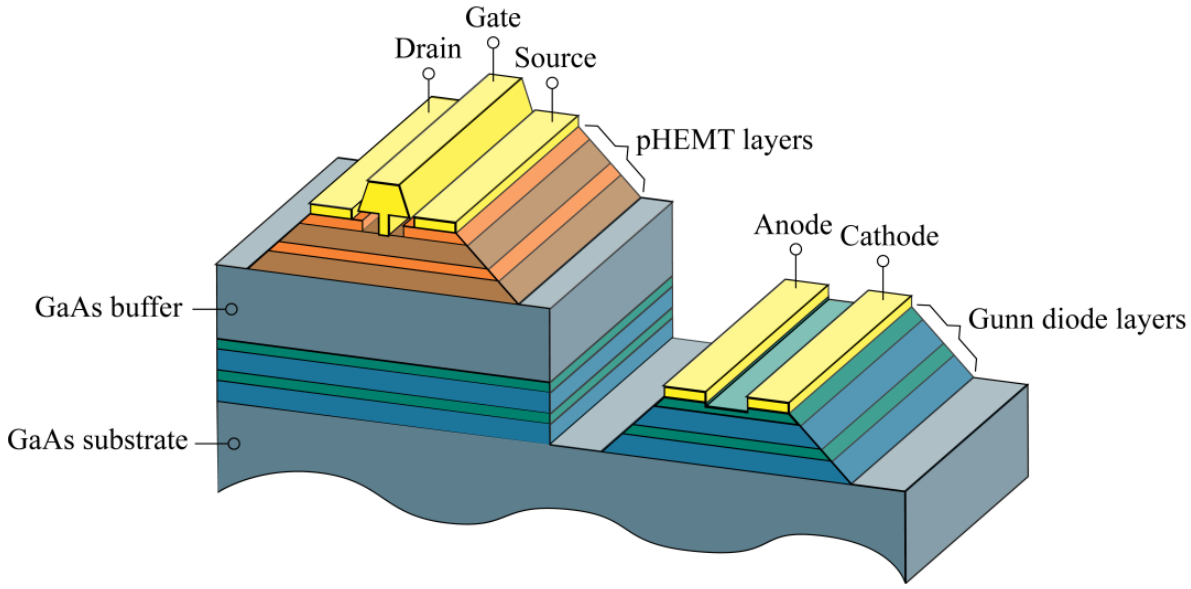


Figure 7.1 The general layer structure of the combined wafer approach (not to scale) [151].

The detailed layer structure of the wafer is depicted in Figure 7.2. The transistor layers placed on top are identical to the pHEMT structure with an $In_{0.2}Ga_{0.8}As$ channel layer, as presented in Section 6.3.1. A GaAs buffer with thickness of 1.1 μm is placed between the active layers of the two devices. Additionally, a thin layer of 5 nm AlGaAs is placed underneath the buffer serving as an etch-stop layer for the removal of the pHEMT and the buffer from the top. The high aluminium content of AlGaAs, equal to 80%, provides a high selectivity for etching over GaAs using citric acid and succinic acid solutions [77, 78, 137]. The bottom Gunn diode layers are similar to the C230 wafer, with each of the two channel layers sandwiched between two δ-doping layers. The cap layer is the only layer modified, where the graded InGaAs has been replaced with highly-doped GaAs. Thus, the lattice mismatch between the Gunn cap layer and the GaAs buffer is avoided, with obvious drawbacks expected for the Ohmic

contacts of the diode. Finally, the thickness of the Gunn cap layer has been increased to 150 nm, providing an error margin for the etching process when reaching the Gunn diode.

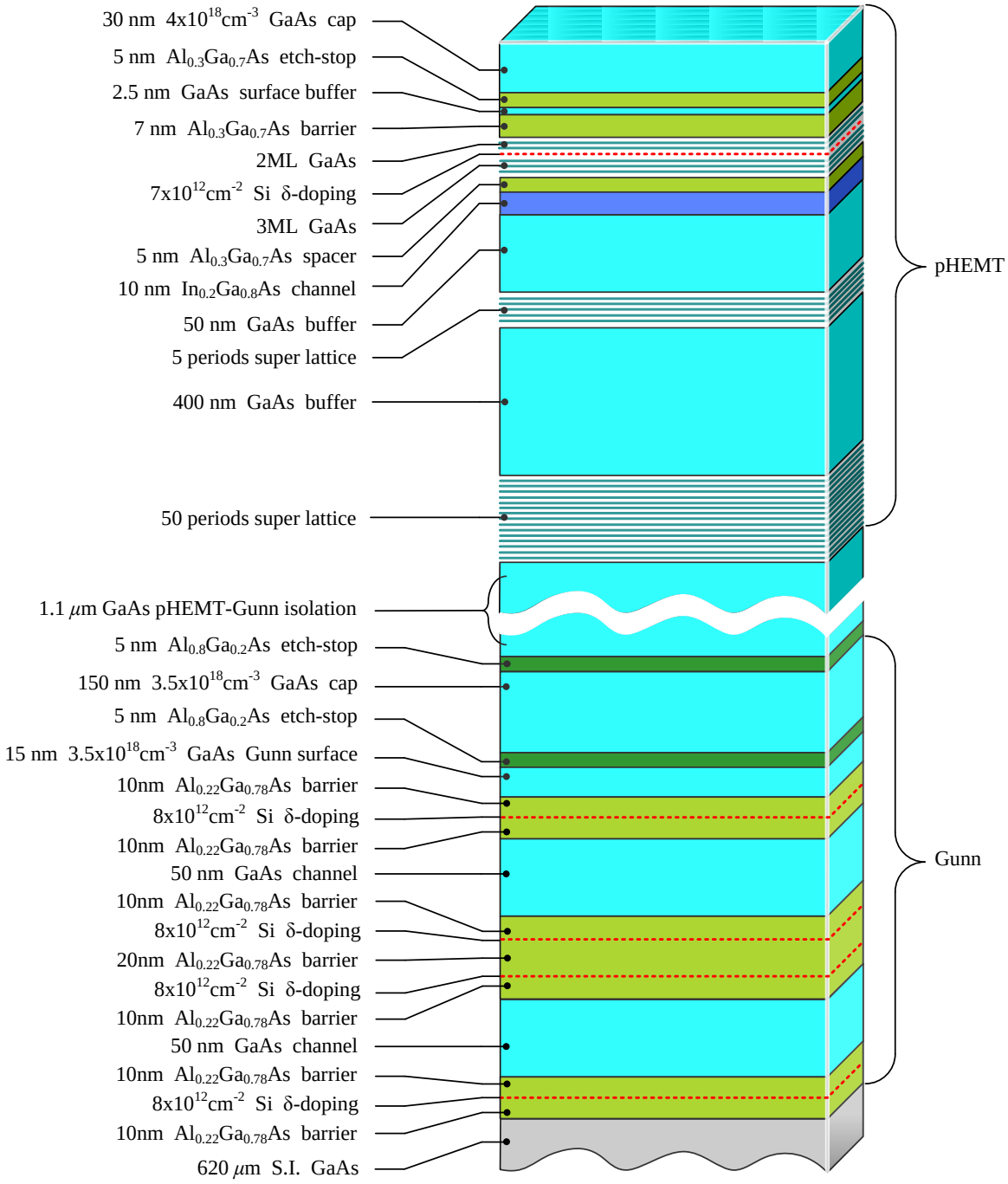


Figure 7.2 The detailed layer structure of the combined wafer (not to scale).

7.2.2 Fabrication process

The fabrication process flow for the combined wafer technique is illustrated in Figure 7.3. The removal of the pHEMT and the buffer layers is initially required to reach the surface of the Gunn cap layer. This process needs to be executed with high uniformity across the wafer, while at the same time minimising the possible damage to the Gunn diode layers. Thus, the removal of the top layers is performed using a hybrid procedure. After cleaning the surface for the removal of native oxides, a dry etching process is applied for the removal of the pHEMT layers and a large amount of the GaAs buffer layer (figures 7.3(a) & (b)). The dry etch process presents higher uniformity over wet etch. A stepped wet etching treatment is applied afterwards for the removal of the remaining buffer, reaching the Gunn cap layer (Figure 7.3(c)). The wet etch treatment limits the damage caused to the layers underneath [136, 75].

An RIE process has been selected for the dry etch process using a silicon-tetrachloride $SiCl_4$ gas environment. Experimental tests have demonstrated the etching of GaAs, $Al_{0.3}Ga_{0.7}As$ and $Al_{0.8}Ga_{0.2}As$ occurs at similar rates using $SiCl_4$ [152]. The $In_{0.2}Ga_{0.8}As$ pHEMT channel is expected to perform as an etch-stop layer when using the current chemistry. The etch rate of $In_{0.2}Ga_{0.8}As$ can be increased by using a higher RF power in the RIE chamber, which causes higher energy bombardment of the semiconductor. The detailed RIE conditions used are presented in Appendix B.

A set of test runs was conducted, where the total layer structure of the combined wafer was etched down to the semi-insulating substrate. The etching process was monitored using a laser interferometer at 630 nm. The interferometer response was matched to the layer structure for the identification of the end point of the etching before reaching the Gunn layers. The response of the interferometer results from the superposition of two signals. The first signal is reflected at the surface of the etched material, whereas the second one penetrates until reaching a hetero-junction. The incident signal is then reflected due to the different refractive indices at the semiconductor interface. The magnitude of the secondary signal is attenuated proportionally to the penetration depth. Finally, the interferometer response consists of oscillations created from the alternate constructive and destructive interference between the two signals [153]. Since the epitaxial layers are removed from the top, the secondary signal experiences lower absorption and the oscillation extremes increase when

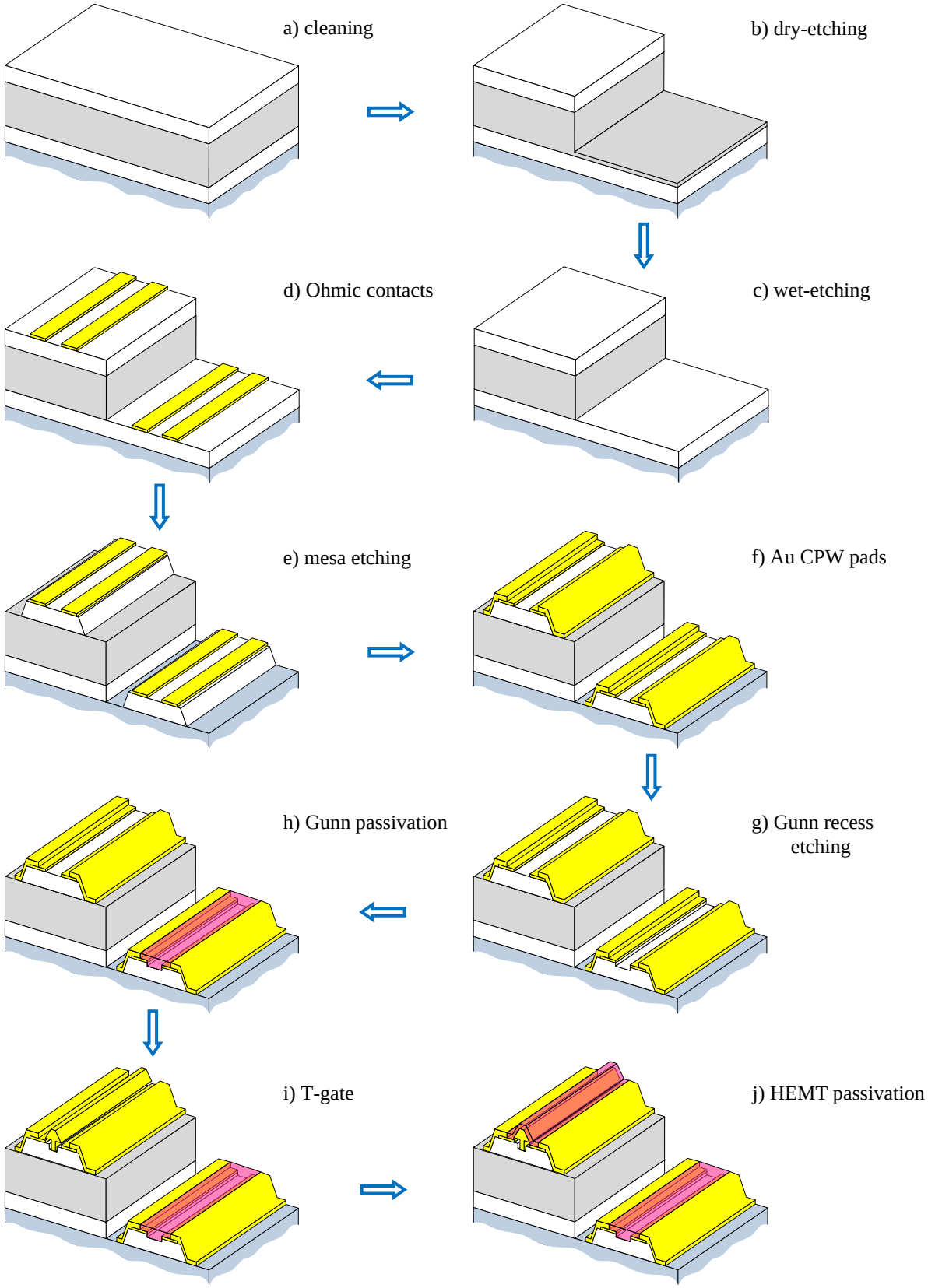


Figure 7.3 The fabrication process flow for the combined wafer.

reaching the hetero-junction. The intensity of the reflected signals also depends on the refractive indices of the materials.

The resolution of the interferometer is determined by the etched thickness between two consecutive extremes of the reflectance, i.e. ~ 82 nm for GaAs [154]. Thus the monitoring capability of the technique is limited when etching thin epitaxial layers. On the other hand, due to the significant attenuation of the incident signal by relatively thick layers, variations in the reflectance are distinguishable only for relatively thin layers (less than 500 nm for GaAs [154]).

Considering the above specifications of the interferometer technique, the response resulting from the etch test is analysed in this section. Figure 7.4 depicts the interferometer response after removing the complete layer structure of the combined wafer. The removal of the pHEMT layers is complete after the characteristic "W" of the response. Then the negligible amplitude of oscillations indicates the exposure of the thick GaAs buffer as the secondary signal is significantly absorbed. The oscillations become distinguishable again after the point "A", which is approximately 600 nm away from the next GaAs / AlGaAs hetero-junction. After this point, the intensity of the secondary signal rises as the GaAs buffer is progressively removed. After four periods with increasing amplitudes a relative decrement due to the lower refractive index of the material indicates the presence of the $Al_{0.8}Ga_{0.2}As$ etch-stop layer. This hypothesis was later confirmed after the execution of electrical measurements. Three additional test samples were etched up to three different points with -1, 0 and +1 peak offset relative to the $Al_{0.8}Ga_{0.2}As$ point. The sample etched up to the point of one peak to the right of the $Al_{0.8}Ga_{0.2}As$ point presented the highest conductivity, lying at the beginning of the highly doped Gunn cap layer. Additionally the etched depth was measured using a profilometer, confirming the above results. After the removal of the Gunn layers, the reflectance becomes negligible again with the incident signal absorbed by the thick substrate.

The same procedure was performed three more times, where the layer structure of the complete wafer was removed completely. Although the etching period was varied from run to run due to the different conditions of the RIE chamber, the same sequence of extremes was observed for every test. Thus, the process presents the required repeatability to enable stopping at the same point every time.

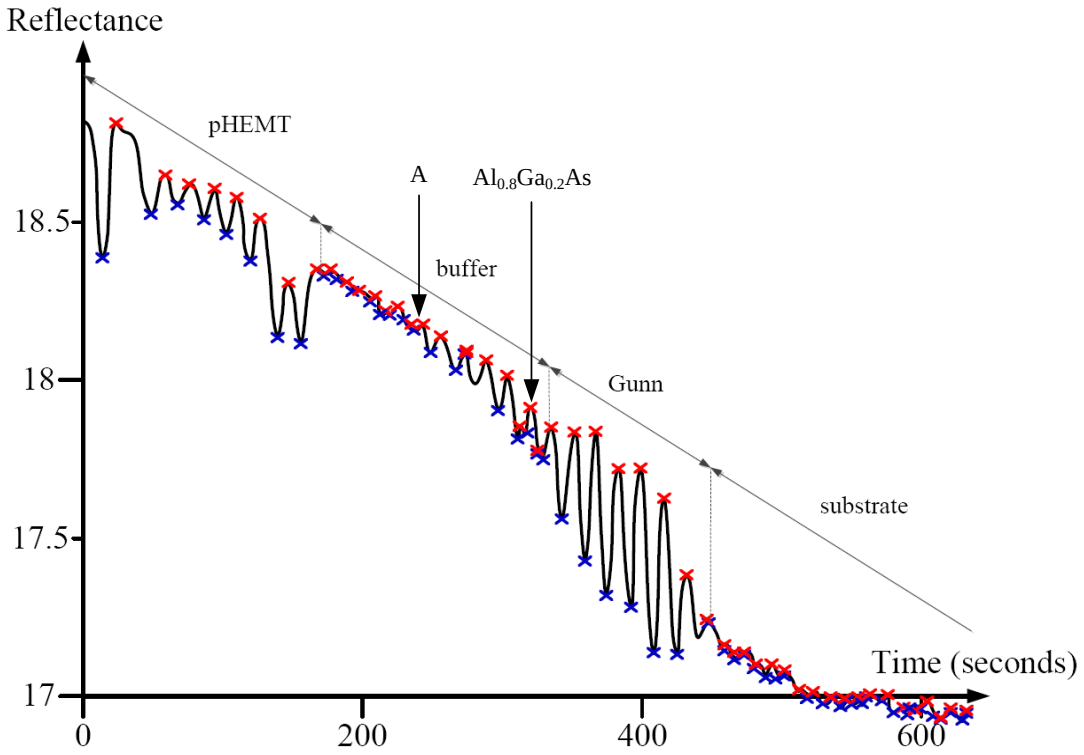


Figure 7.4 The interferometer response for the test run where the layer structure is completely etched.

During the fabrication of the actual Gunn diodes, the dry-etching process was interrupted before reaching the $Al_{0.8}Ga_{0.2}As$ layer, avoiding any damage caused to the Gunn layers by the high-energetic reactants. The remaining GaAs buffer was removed by using the succinic acid solution which stops at the $Al_{0.8}Ga_{0.2}As$ layer. The etched depth was monitored between the etching steps using a profilometer. Finally, the etch-stop layer was removed selectively over GaAs using a 10:1 buffered hydrofluoric acid solution for 30 s [155].

Following the complete removal of the pHEMT and the buffer layers, planar Gunn diodes were fabricated with 1, 1.3, 1.5, 2, 3 and 4 μm L_{ac}. The diodes were implemented following the same techniques as described in Sections 6.2.2 - 6.2.5 for the steps d-g of Figure 7.3. Due to the absence of the graded GaAs/InGaAs cap layer, the Pd/Ge/Au/Pd/Au alloy was replaced by a Au/Ge/Au/Ni/Au alloy for the formation of the Ohmic contacts. After annealing at 400^{o}C the resulting contact resistivity was equal to 0.23 Ω.mm, but bad surface morphology was observed as presented in Figure 7.5. This is due to the transfer of the As compound to the surface during the final phase of formation of the Ohmic contact [133, 142]. Thus, the actual devices were annealed at 360^{o}C maintaining a good surface morphology with a small

increment in the contact resistivity to 0.25 Ω.mm. The recess etching was performed using the same succinic acid solution with adjusted pH 5.9 and the devices were finally passivated with a 250 nm thick layer of Si_3N_4.

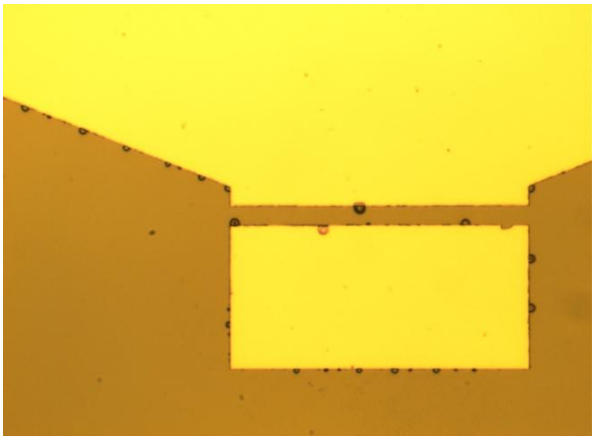


Figure 7.5 Bad surface morphology caused by the transfer of As at the surface after annealing at 400°C.

7.2.3 Gunn diode results

The devices were initially characterised in terms of DC performance. Figure 7.6 presents the *I* - *V* characteristic of a 60 μm wide device with 2 μm L_{ac}, showing a promising NDR for biasing voltages above 2.5 V. The RF characterisation was performed afterwards using the VNA for the initial signal detection. Figure 7.7 presents the $|S_{11}|$ response of the same 2 μm device biased at 2.5 V. The device presents a maximum value of approximately 1 dB around the centre frequency of 60 GHz. This is the highest $|S_{11}|$ response obtained from all the fabricated devices. The spectrum analyser set up was then used for the detection of any occurring oscillations. Although various biasing conditions were applied to all the diodes, no device presented any oscillations.

It could be initially assumed that the limited performance of the devices is caused by the replacement of the graded GaAs/InGaAs cap layer of the C230 design with the highly doped GaAs. The increment of the contact resistance in comparison with the C230 wafer, from 0.19 to 0.25 Ω.mm, could confirm this assumption. A new set of tests was executed for the identification of possible reasons that could cause the lack of oscillations of the diodes.

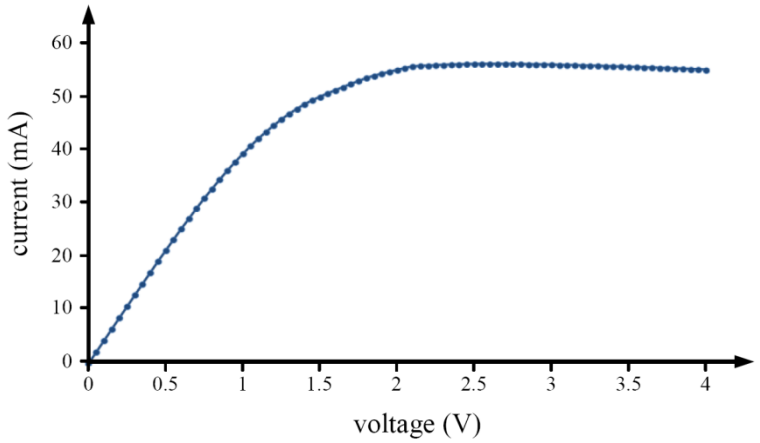


Figure 7.6 Current-voltage characteristic for a planar Gunn diode with 2 μm L_{ac} and 60 μm width [151].

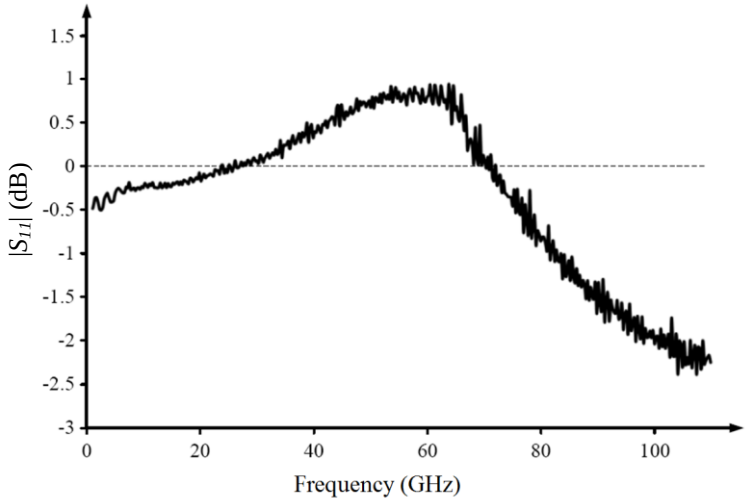


Figure 7.7 The $|S_{11}|$ response versus frequency for the diode of Figure 7.6 [151].

TLM structures were fabricated on both the pHEMT and the Gunn levels of the combined wafer, where the Au/Ge/Au/Ni/Au alloy was annealed at 360^{o}C. A small difference in the contact resistance was observed between the two levels, where 0.29 Ω.mm resulted for the pHEMTs. The thickness of the Gunn cap layer was measured afterwards using the profilometer. This was found to be ~140 nm. Thus, no significant over-etching occurred during the removal of the etch-stop $Al_{0.8}Ga_{0.2}As$ layer with HF and the cap layer maintains a relatively high thickness. The thicker Gunn cap layer would be expected to present lower sheet resistance, due to the larger cross section of the channel occurring for the electron transport. This was confirmed by the measurements where 65 Ω/□ and 215 Ω/□ resulted for the Gunn and the pHEMT level, respectively.

Additional tests were performed by removing the highly doped cap layer between the TLM pads using the succinic acid solution. The resistance between two pads with 150×150 μm^2 geometry and 2.5 μm separation was measured for both levels. An average value of 16 Ω resulted for the pHEMT level, whereas the resistance for the Gunn level presented a variation with values between 50-60 Ω. The overall results of the above tests are presented in table 7.1.

	cap thickness (nm)	contact resistance (Ω.mm)	sheet resistance (Ω/□)	recessed pads resistance (Ω)
pHEMT	30	0.29	215	16
Gunn	130	0.25	65	50-60

Table 7.1 Results obtained from the TLM tests. The recessed resistance is referred to the resistance between two TLM pads with 150×150 μm^2 geometry and 2.5 μm separation.

The above results indicate that the increased thickness of the cap layer for the Gunn level causes the performance degradation of the diodes. The higher thickness of the Gunn cap layer, in comparison with the HEMT cap layer, is monitored at the lower values of the sheet resistance resistivity. The contact resistivity is also lower for the Gunn level, as a result of the majority of the current flowing through the highly doped surface cap layer rather than travelling through the lower channel layer. The effective contact resistance for the current travelling through the channel is extracted after etching the highly doped semiconductor between the pads, as demonstrated in [142]. The very high resistance of the recessed pads for the Gunn level indicates the insufficient diffusion of the metal alloy down to the channel layer, causing the degradation of the diode performance. The limited diffusion of the Ohmic contacts in relatively thick layers of semiconductors has been demonstrated through the multi-quantum well wafers, where the deeper channels do not contribute to electron conduction [11].

For the successful future integration of the two devices following the combined wafer approach, the modification of the Gunn cap layer is required. The reduction of the layer thickness to 50 nm would provide a sufficient margin for over-etching during the removal of the $Al_{0.8}Ga_{0.2}As$ etch-stop layer. Thinning the cap layer in the current wafer could potentially

eliminate the problem of the limited diffusion of the Ohmic contacts. However, the final thickness would present large variations across the wafer due to fluctuations occurring during the wet etching. Since no oscillating diodes were detected during the current experiments, no transistors were fabricated on the top of the structure and the steps i and j of Figure 7.3 were not executed.

7.3 Side-by-side implementation on a GaAs pHEMT wafer

In parallel with the processing of the combined wafer, the operation of planar Gunn diodes on the pHEMT wafer of Section 6.3.1 was examined. The transferred electron effect in AlGaAs/GaAs multi-quantum well devices was observed for the first time in [49] and simulation results presented the high possibility of Gunn oscillations on HEMT structures [48]. According to these results, there is a high possibility for a joint implementation of diodes and transistors on the same pHEMT substrate.

The implementation principle is illustrated in the schematic representation in Figure 7.8. Because both devices share the same layers, the fabrication procedure is significantly simplified in comparison with the combined wafer approach. The fabrication process flow is illustrated in Figure 7.9. Ohmic contacts are initially fabricated for both devices as presented in Section 6.3.2 for the pHEMTs. Similarly, the same process was followed as in Section 6.3.3 for the mesa isolation of the transistor and the diode (Figure 7.9(b)). The 70 nm T-gate technique was applied afterwards for the transistor and the 50 Ω CPW pads were then evaporated then for both the Gunn diode and the pHEMT (Figure 7.9(d)). In the next step of the fabrication procedure, the cap layer between the Gunn electrodes was partially etched using the succinic acid solution with adjusted pH at 5.9. The surface of the wafer was cover with a PMMA layer for the protection of the transistors and the diodes were exposed for the performance of the recess etching. The target current for the diodes was set by the performance of the transistors, as presented in Figure 6.30. Finally, both devices were protected after the deposition of a 250 nm thick passivation layer (Figure 7.9(f)).

The pHEMTs with 1.5 μm L_{DS} present a maximum current of approximately 600 mA/mm, i.e. ~ 36 mA for a 60 μm wide device. Figure 7.10 illustrates the current-voltage characteristic for a complete planar Gunn diode with 1.3 μm L_{ac} and 60 μm width, presenting a maximum current equal to 35 mA. An NDR arises for biasing voltages between 2.5-2.7 V, which is hardly visible due to the impact ionisation effect.

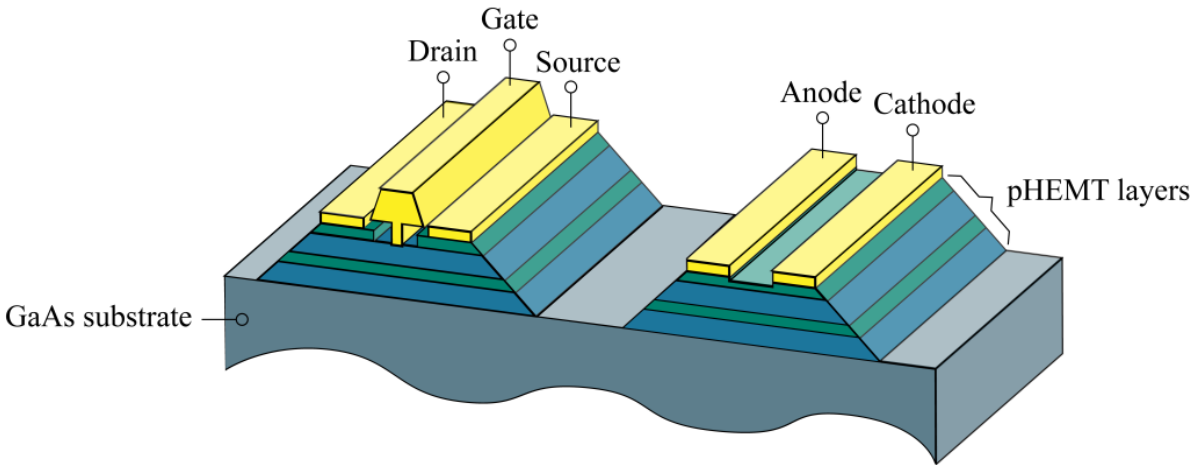


Figure 7.8 The side-by-side implementation of the transistor and the diode on the pHEMT substrate.

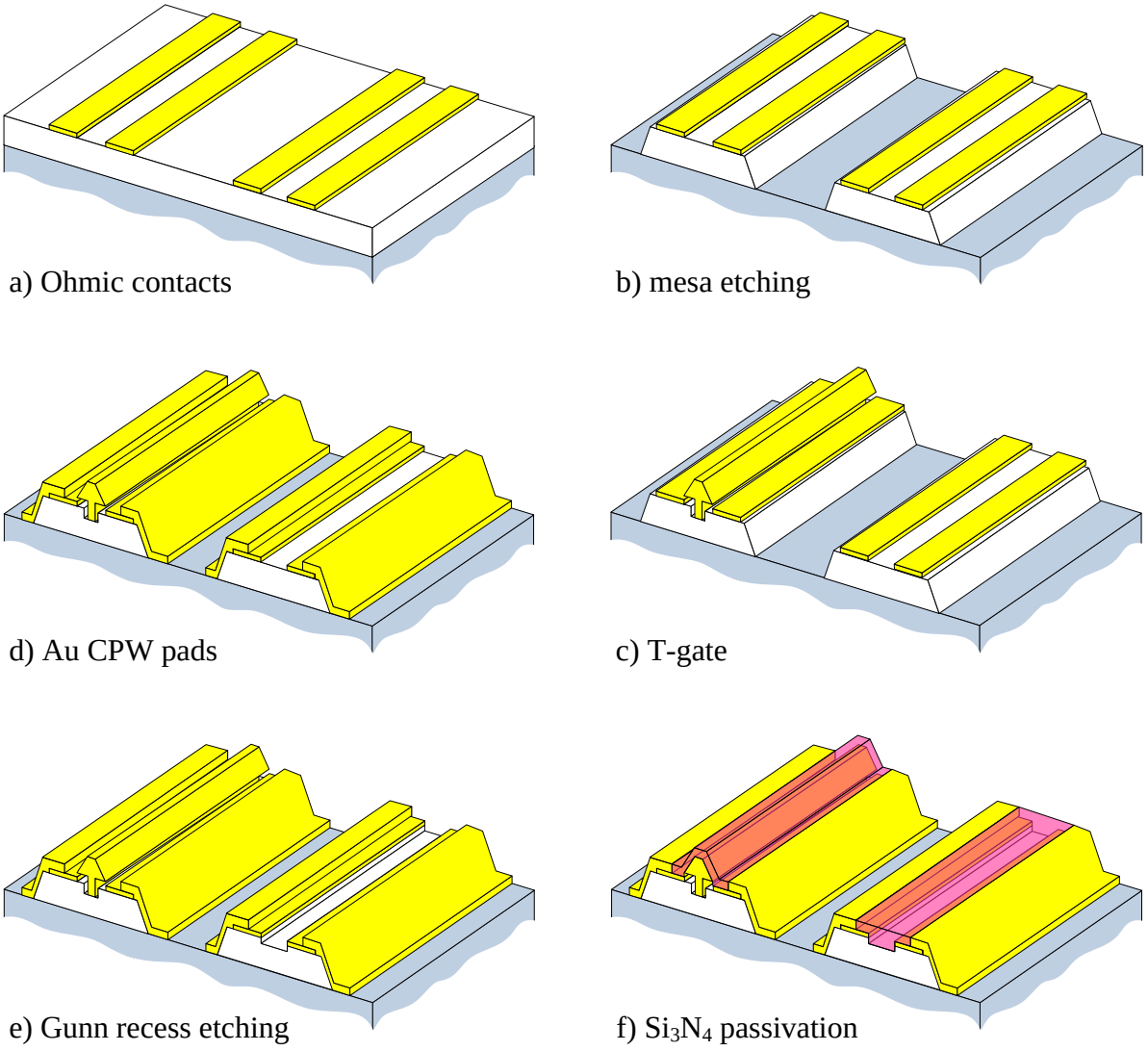


Figure 7.9 The fabrication process flow for the side-by-side approach.

Figure 7.11 illustrates the first ever reported oscillation generated by a planar Gunn diode implemented monolithically with a pHEMT side-by-side [156]. The device with 1.3 μm L_{ac} and 60 μm width presents oscillations at 87.6 GHz in the fundamental mode of operation. The device presents a maximum generated power of -40 dBm for an applied voltage equal to 3.42 V. Due to the limited available material, only two more operating devices were detected, generating oscillations at 55 and 27.5 GHz with 1.5 and 3 μm L_{ac}, respectively.

The above results demonstrate a great potential for the future implementation of high-power, high-frequency MMIC oscillators based on planar Gunn diodes and pHEMTs. However, there are several improvements that need to be conducted for the enhancement of the oscillator performance. The generated power of -40 dBm, i.e. 0.1 μW is extremely low for any attempt of amplification. On the other hand, the power performance of the diode is similar to the one reported for the first high-frequency planar Gunn diodes [9]. Thus, the current results are very promising and a number of modifications could lead to the enhancement of the performance of both the transistor and the diode. The replacement of the GaAs cap layer with the graded GaAs/InGaAs is expected to reduce significantly the contact resistance, with obvious benefits for the performance of both devices. In addition, the current level of the devices would be increased after the introduction of a second channel layer [157]. This development would

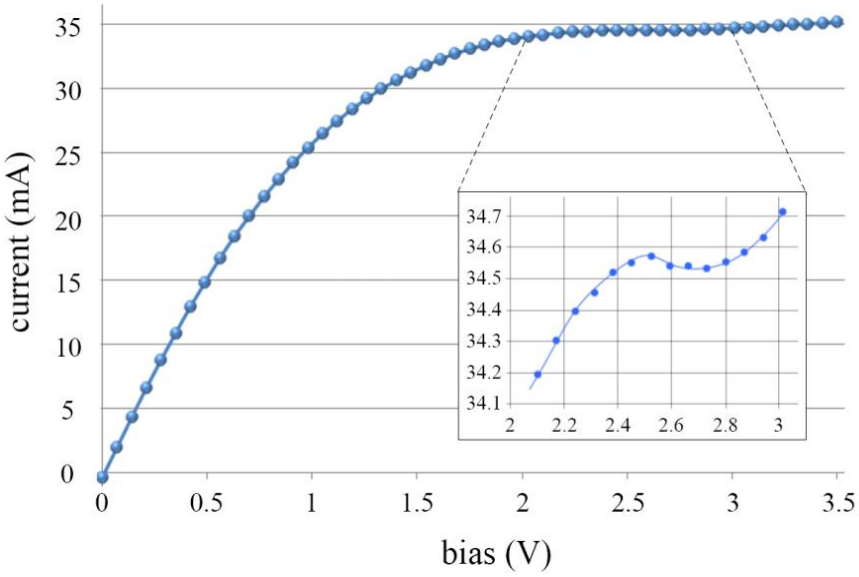


Figure 7.10 Current - voltage characteristic for planar Gunn diode with 1.3 μm L_{ac} implemented on the pHEMT wafer [156].

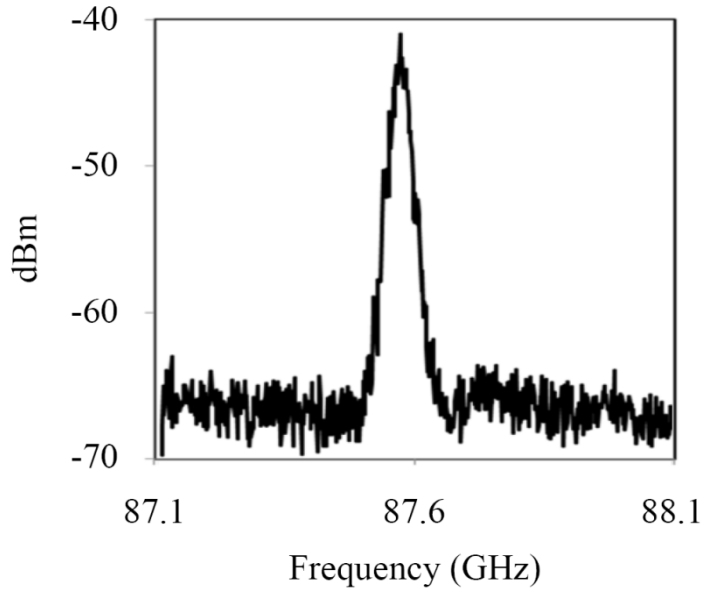


Figure 7.11 Measured spectrum of a planar Gunn diode with 1.3 μm L_{ac} implemented on the pHEMT substrate [156].

have a significant impact on the transconductance of the transistor and the generated power of the diode. However, the total number of the channel layers cannot be more than two. Although the generated power of the diode is boosted after the introduction of many channel layers [11] this cannot be implemented for the transistor. The transconductance would present multiple maximum values due to the parallel current paths and the gate would have limited control of modulating the lower channels [157, 158]. A significant development could also be realised with the introduction of extra δ-doping layers, where the carrier concentration in the channel is expected to increase significantly [96, 159].

7.4 Side-by-side implementation on the InP HEMT wafer

7.4.1 Layer structure and fabrication process

The layer structure of the InP HEMT wafer is presented in Figure 7.12. The InP substrate allows the growth of lattice matched $In_{0.53}Ga_{0.47}As$ for the formation of the cap and the channel layers. The barrier and the buffer layers consist of $In_{0.52}Al_{0.48}As$ which is also lattice matched to the rest of the materials. $In_{0.52}Al_{0.48}As$ provides the high band gap required for the formation of the channel quantum well.

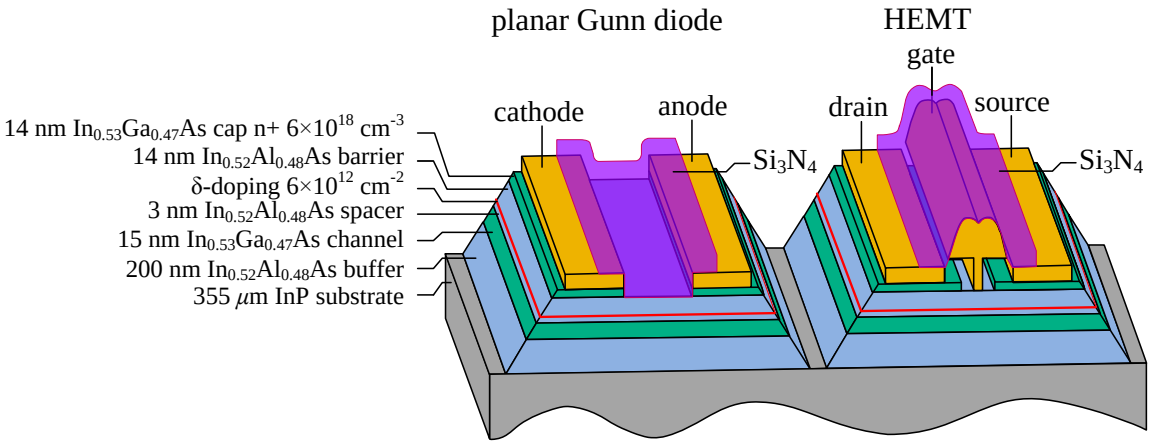


Figure 7.12 Cross-section illustration of the integrated planar Gunn diode and the HEMT.

The side by side approach is similar to the procedure presented in Section 6.5 for the GaAs layer system where the two devices share the majority of the fabrication steps. However, some minor alternations have been applied in the current process due to the different material properties. The same Ohmic contact alloy used in the pHEMT substrate is also suitable for the creation of high quality contacts on the $In_{0.53}Ga_{0.47}As$ cap layer without need for annealing. Additionally, the characterisation of the Ohmic contacts using the standard TLM method, resulted a contact resistance equal to 0.11 Ω.mm. The complete fabrication process is presented in detail in Appendix B VI.

Following the fabrication of the Ohmic contacts, the mesa isolation was performed for both devices. Similarly to the GaAs wafer, a PMMA mask was hard baked for two hours before getting exposed to the electron beam, obtaining the required resistance to the wet etching solution. The latter consists of an orthophosphoric acid (H_3PO_4) solution in 1:1:100-H_3PO_4:H_2O_2:H_2O mixture, applied for 120 s. The current etchant has been used for the fabrication of sub-100 nm HEMTs on similar layer systems [147].

The next step was the recess etching of the planar Gunn diode. The sample was covered with a 12 % PMMA resist layer for the protection of the HEMTs and windows were opened for the exposure of the mesa areas of the diodes. The succinic acid solution was applied for 5 s for the reduction of the current to approximately 60 mA for diodes with 120 μm width. This target current level is indicated from the results reported for $In_{0.53}Ga_{0.47}As$ devices with similar geometry [99]. The current density was equal to 500 mA/mm, which is approximately equal to the maximum HEMT current density as presented in the results section.

The same 70 nm T-gate technology presented in Section 6.3.5 was used for the realisation of the 3D profile for the gate terminals. Similarly to the etching tests presented in Section 6.3.6, four different etching treatments were applied for the identification of the optimum duration of etching. Thus, the test sample was cleaved in four pieces that were treated afterwards with the 5.9 pH succinic acid solution for 9, 11, 13 and 16 s. Prior to the metal evaporation, an ammonia based solution was applied for the de-oxidation of the InAlAs etch stop layer. The ammonia solution (10:1 - H_2O:NH_3OH) causes a relatively low reduction to the device current in comparison with sulphuric, phosphoric, HCl and HF mixtures [160]. The fabrication of the T-gates was complete after the evaporation of the Ti/Pt/Au metal alloy.

Finally, a Si_3N_4 passivation layer was deposited using a lift-off process for the protection of both the diode and the HEMT from oxidisation. The dielectric layer was formed using an inductively coupled plasma - chemical vapour deposition (ICP-CVD) process in room temperature [161]. Thus, a possible diffusion of the gates that can occur at high temperatures was avoided. Moreover, the low temperature environment is needed for the PMMA mask in order to maintain the required sharp profile for the lift-off process. Figure 7.13 illustrates the SEM image of the planar Gunn diode and the HEMT implemented on the InP HEMT substrate. A detailed image of the transistor, before the deposition of the Si_3N_4 passivation layer, is presented in Figure 7.14 showing the mesa island and the T-gate cross-section.

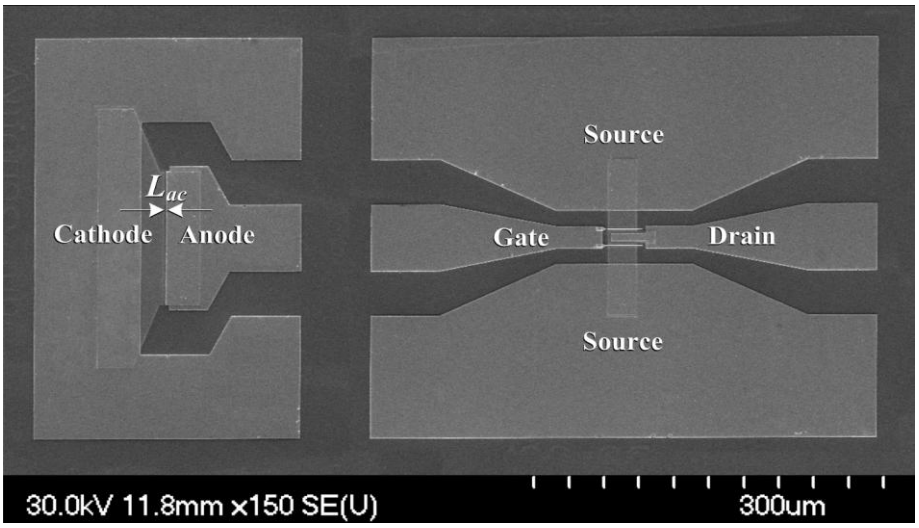


Figure 7.13 SEM picture of the two devices fabricated side by side on the InP HEMT substrate. The L_{ac} of the planar Gunn diode is equal to 1.3 μm and the width is 120 μm. The 70 nm T-gate HEMT is 12.5 μm wide with 1.5 μm drain to source separation.

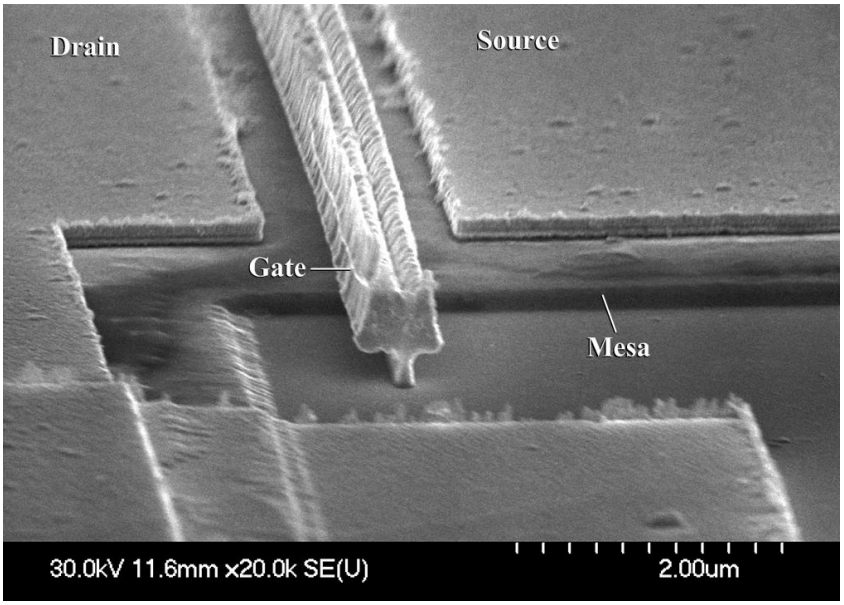


Figure 7.14 Detailed image of the 70 nm T-gate HEMT with 1.5 μm drain to source separation.

7.4.2 Results

The DC performance of the HEMTs is presented first. The devices treated for 16 s showed the best performance, where the devices etched for 9, 11 and 13 s presented insufficient control of the current due to a remaining portion of the cap layer. All the results presented in the next sections refer to HEMTs etched for 16 s, with 12.5 μm width and 1.5 μm drain to source separation.

Figure 7.15 presents the drain current as a function of the V_{DS} bias for various V_{GS} voltages. The maximum current density is equal to approximately 600 mA/mm for a 0.8 V V_{GS} bias. After the saturation region the device presents a small increment of the drain current for V_{DS} higher than ~ 0.8 V, due to the impact ionisation effect. The pinch-off is achieved for gate biasing lower than -0.8 V. The transconductance performance is depicted in Figure 7.16. The devices present a maximum transconductance equal to 525 mS/mm for -0.1 V gate bias.

The transistors present high current density in comparison to the similar structure presented in [159] where a self-aligned technique was applied for the definition of the Ohmic contacts. On the contrary, the transconductance performance is significantly lower than the equivalent reported maximum transconductance of 1500 mS/mm. However, the current results are very promising considering that the layer structure in [147, 159] includes two δ-doping layers.

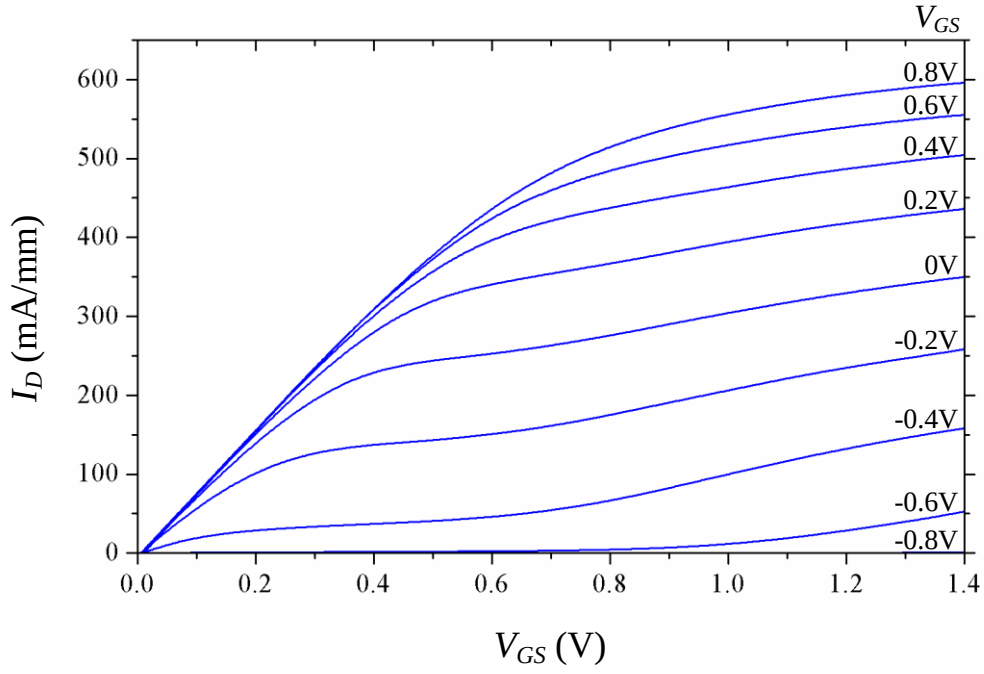


Figure 7.15 I_D-V_{DS} characteristics for a 70 nm T-gate device with 12.5 μm width and 1.5 μm drain-to-source separation.

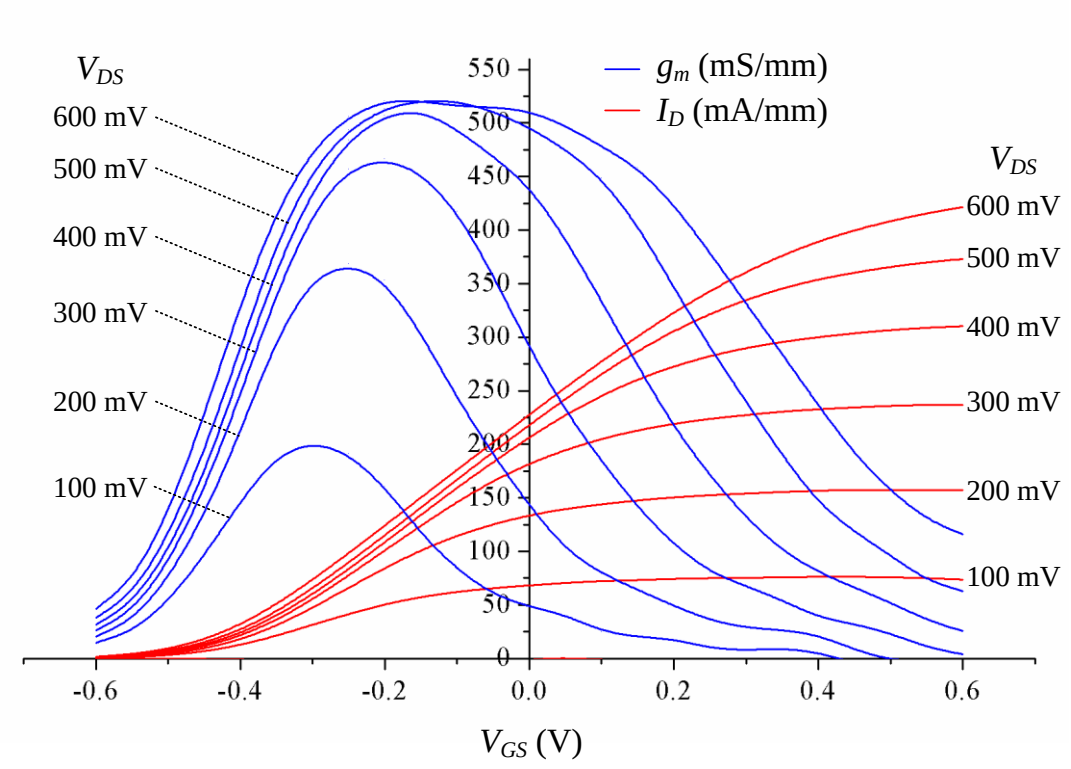


Figure 7.16 Resulted g_m-V_{GS} and I_D-V_{GS} characteristics for various drain biasing. The geometry of the device is the same as in Figure 8.4.

In addition, a double recess etching has been performed in the self-aligned approach, bringing the gate closer to the channel for a more effective current modulation.

The RF characterisation of the devices followed the DC measurements. The devices were measured using the 10 MHz - 110 GHz and 140 - 220 GHz VNA set ups available in the mm-wave lab of the University of Glasgow. The pads performing the transition from 40/60/40 μm W/G/W geometry to 15/20/15 μm were de-embedded from the measured results. Thus, the effect of the transition pads which introduces additional poles in high frequencies has been subtracted. Two probes with 100 μm and 50 μm signal-to-ground pitch were used for the characterisation of the transition pads as illustrated in Figure 7.17.

The high-frequency performance of the 70 nm T-gate HEMT is illustrated in Figure 7.18. The device presents excellent characteristics with 220 GHz f_T and 330 GHz f_{max}. The equivalent reported values for the self-aligned devices with double δ-doping layers are 270 GHz f_T and 300 GHz f_{max} [147, 159]. A significant enhancement of the high-frequency performance is also observed in comparison with the pHEMTs presented in section 7.3, as a result of the reduced contact resistance and the superior characteristics of the $In_{0.53}Ga_{0.47}As$ channel layer.

The performance of the planar Gunn diodes is presented in the next lines. An array of diodes with different geometries has been fabricated where the L_{ac} distance was varied from 1.0 to 4.0 μm. Figure 7.19 illustrates the current-voltage characteristic of a 120 μm wide diode with 1.0 μm L_{ac}. The device presents excellent current density with 62 mA maximum current. In addition, an NDR is clearly observed for biasing voltages above 1.25 V.

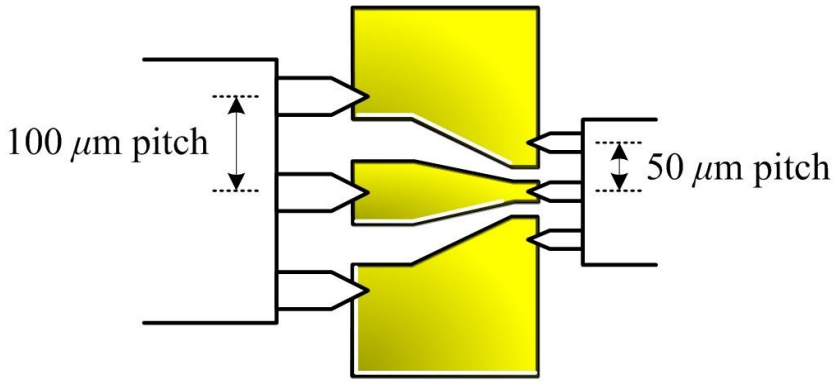


Figure 7.17 Characterisation of the transition pads for post-processing de-embedding.

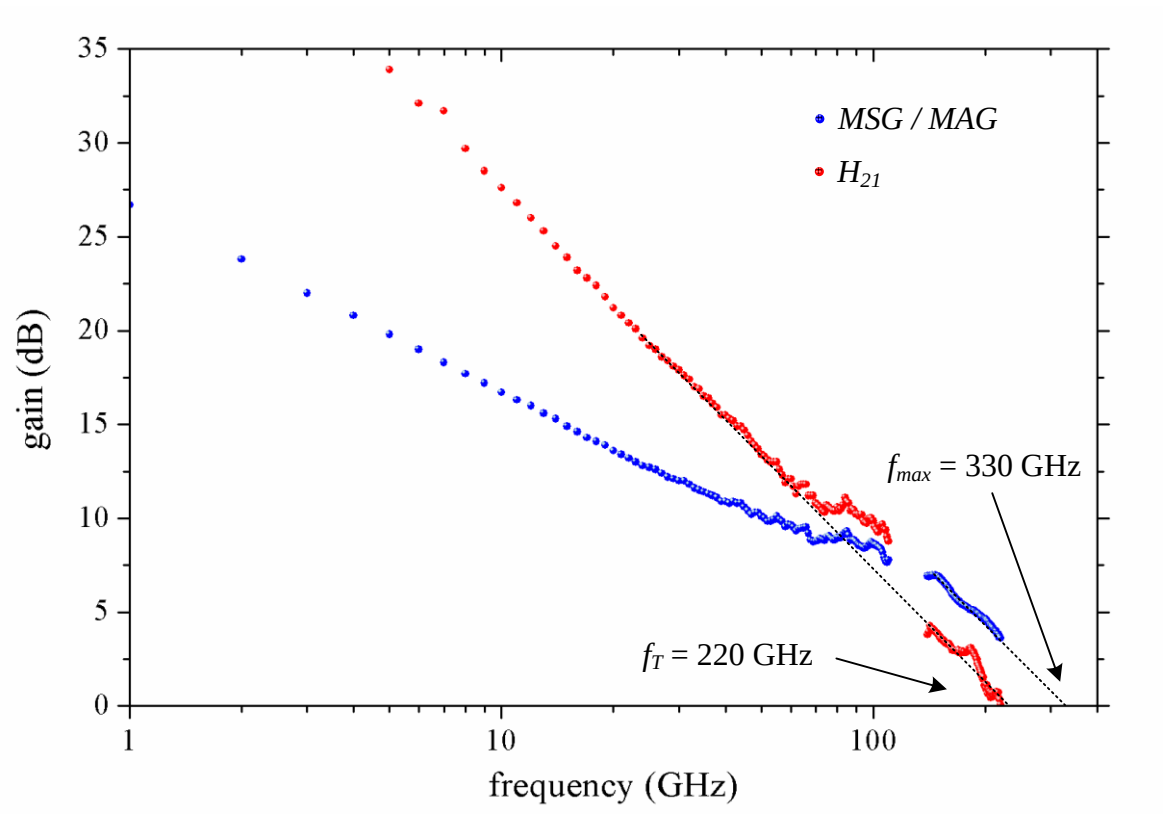


Figure 7.18 *MSG/MAG* and H_{21} gain after de-embedding the transition pads.

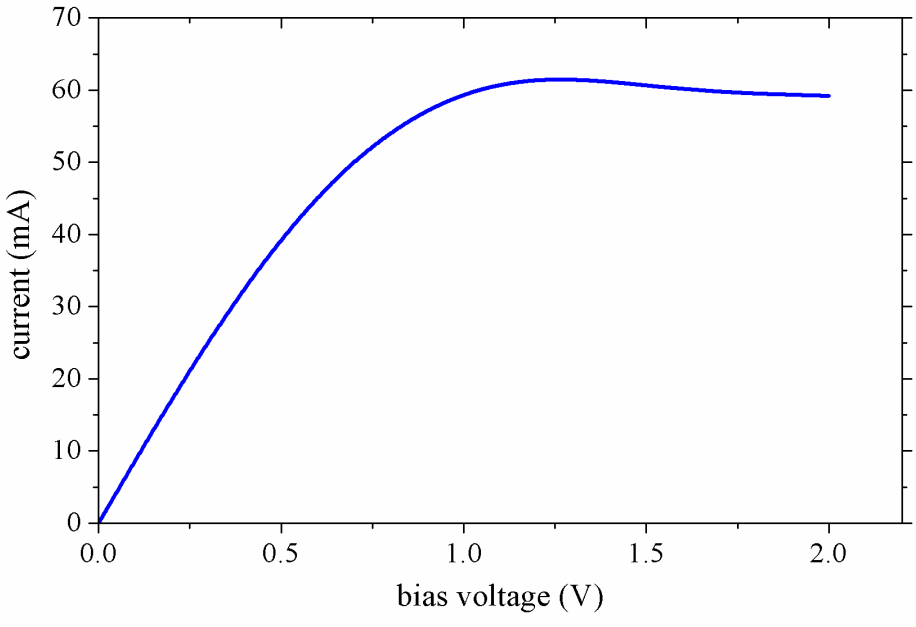


Figure 7.19 Current-voltage characteristic for planar Gunn diode with 1.0 μm L_{ac} and 120 μm width.

Figure 7.20 presents the measured spectrum of the 1.0 μm device. The diode presents excellent oscillating characteristics with 204 GHz frequency of oscillation and -7.3 dBm generated power. The diode also presents a high quality signal with very low phase noise. Figure 7.21(a) and (b) present the measured spectrum for devices with L_{ac} equal to 1.3 μm and 2.0 μm, respectively. Due to the lack of appropriate equipment, an exact value for the phase noise could not be measured. However, a significant reinforcement of the performance can be observed in comparison with the GaAs pHEMT layer structure presented in Section 7.3. For the same L_{ac} equal to 1.3 μm, the $In_{0.53}Ga_{0.47}As$ diodes present approximately double frequency of oscillation with significantly improved power performance and phase noise characteristics. The oscillation frequency and the generated power are presented as a function of L_{ac} in Figure 7.22. The power level is in the order of hundreds of microwatts for all the

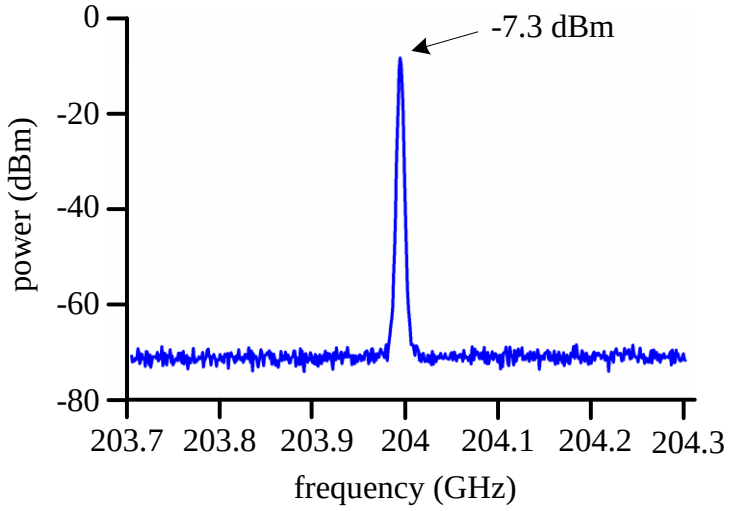


Figure 7.20 The measured spectrum of a planar Gunn diode with 1.0 μm L_{ac} and 120 μm width.

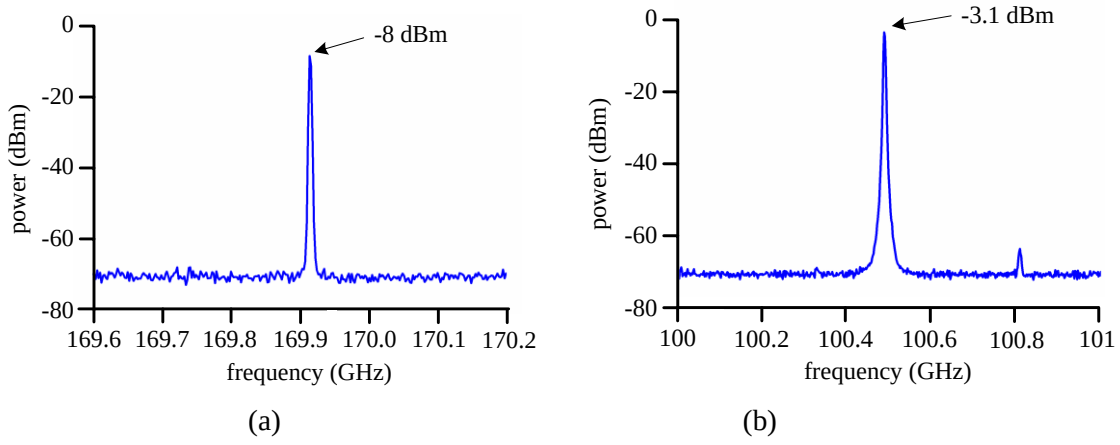


Figure 7.21 The measured spectrum of planar Gunn diodes with 1.3 μm (a) and 2.0 μm (b) L_{ac}.

devices and the oscillation frequency depends on the L_{ac} following the same rule as reported for the first $In_{0.53}Ga_{0.47}As$ devices [99]. No oscillations were detected for devices with L_{ac} greater than 2 μm due to imperfections of the material presented across the wafer.

The tuning ability of the oscillation frequency for the 1.3 μm device is presented in Figure 7.23. In agreement with the theory of Gunn oscillators, the frequency decreases for increasing biasing voltage. The tuning range is relatively low, equal to 100 MHz for a 300 mV biasing range.

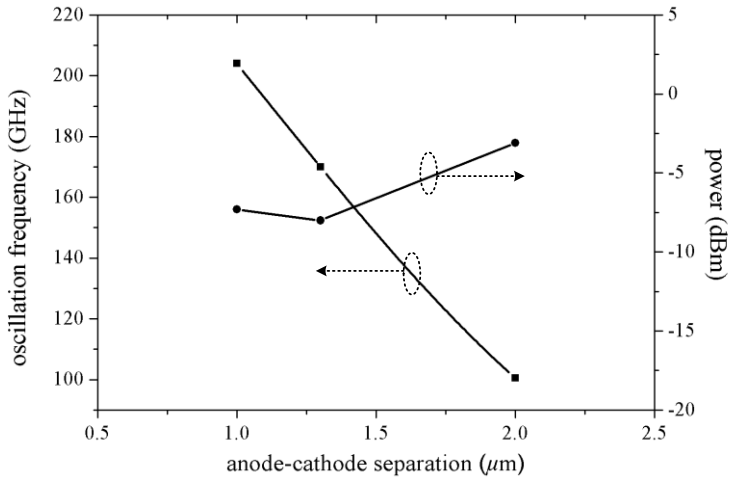


Figure 7.22 The oscillation frequency and the generated power as a function of L_{ac}.

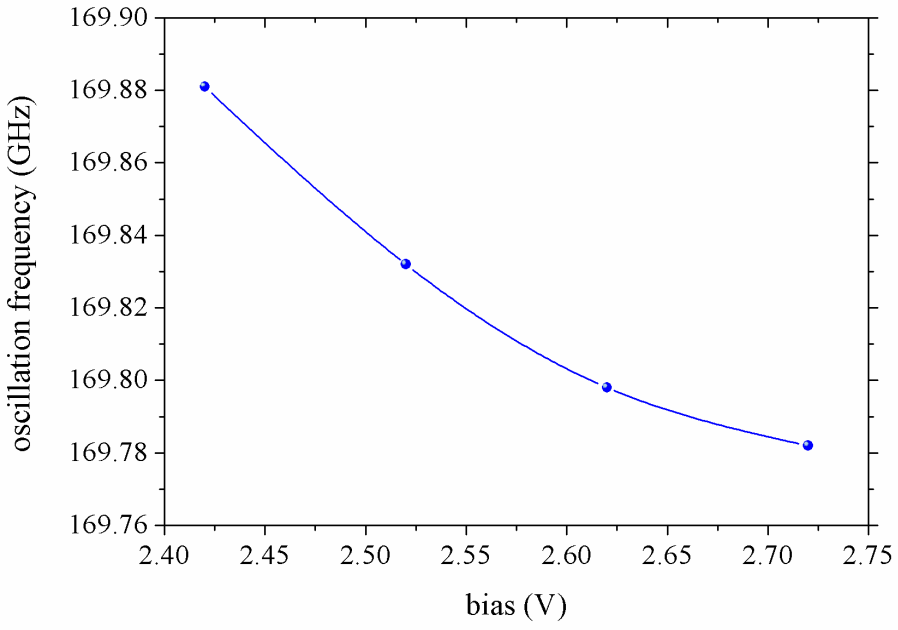


Figure 7.23 Tuning of the oscillation frequency of the 1.3 μm diode for variable bias voltages.

In conclusion, the planar Gunn diodes fabricated on the $In_{0.53}Ga_{0.47}As$ HEMT wafer prove the concept of fabricating the two devices on the same InP substrate. In addition, the diode itself presents exceptional characteristics of oscillation, in agreement with the reported results for the $In_{0.53}Ga_{0.47}As$ wafer designed exclusively for planar Gunn diodes [99]. At the same time, the transistors demonstrate advanced high frequency performance in comparison with the GaAs pHEMTs, providing a sufficient gain greater than 9 dB for frequencies up to 110 GHz. These results demonstrate the potential of amplifying the diode signal using a HEMT amplifier on the same MMIC for the extraction of oscillations with generated power greater than 1 mW.

7.5 Chapter summary

Two different techniques were presented for the implementation of planar Gunn diodes and HEMTs on the same substrate. Regarding the GaAs wafers, the combined wafer approach presents relatively high complexity, since the top pHEMT and the buffer layers need to be removed in a uniform and controlled way. This was achieved by the combination of dry and wet etching processes. However, the relatively thick cap layer of the Gunn diode limits the diffusion of the Ohmic contact metal up to channel layer. Thus, the devices presented a limited performance where no oscillations were detected. The successful implementation of both devices on the same substrate has been demonstrated for the first time by using a single pHEMT wafer. Although the generated power of the diode is very low equal to -40 dBm, the future development of the pHEMT layer structure is expected to enhance significantly the performance of both devices.

A significant development towards the implementation of high power MMIC oscillators has been conducted after the co-fabrication of the diode and the transistor on the InP HEMT wafer. The superior characteristics of the $In_{0.53}Ga_{0.47}As$ channel and cap layers led to the improvement of the high frequency performance of both the planar Gunn diode and the HEMT. Diodes with 1 μm L_{ac} presented oscillations at 204 GHz in fundamental mode, where the maximum generated power was boosted to -7.3 dBm for devices with 120 μm width. The f_{max} of the 70 nm T-gate HEMTs was equal to 330 GHz, demonstrating that the transistor can provide sufficient gain for the implementation of amplifiers operating up to the W-band. The operation of the two devices side-by-side demonstrates a significant achievement towards the implementation of high-power, high-frequency MMIC oscillators using integrated planar

Gunn diodes and HEMTs. The design, fabrication and characterisation of the MMIC oscillator based on the InP HEMT wafer is presented in the following chapter.

8. Design and fabrication of MMIC oscillator

8.1 Introduction

A new technology was presented in the previous chapter for the implementation of the two devices on the same chip. The co-fabrication on the InP HEMT wafer presents very promising results regarding the performance of both devices. Therefore, the next challenge undertaken is the realisation of the transistor amplifier connected to the diode for the reinforcement of the Gunn oscillations. The design procedure of the complete MMIC oscillator is described in detail in the next section. The fabrication of the individual components such as the MIM capacitors, the resistors and the air bridges is also extensively presented in the following sections. The fabrication of the complete MMIC and the characterisation results are finally described in the end of the chapter.

8.2 Circuit design

In order to design the circuit, the first step is to analyse the performance of the transistor itself where the device is examined as a basic amplifying element. The transistor operation shall be improved afterwards with the addition of peripheral circuits, composing the complete amplifier. From the results of Figure 7.18, the transistor can provide a *MSG* of approximately 11 dB at 45 GHz. The S parameters of the $In_{0.53}Ga_{0.47}As$ HEMT for the frequency range between 10 MHz - 110 GHz are illustrated in Figure 8.1. The transistor presents a gain equal to 3.5 dB at 45 GHz, due to the mismatch with the 50 Ω - impedance testing ports. This means that appropriate matching networks need to be connected in the input and the output of the HEMT. Thus, the overall 2-port network, including the matching networks, should provide approximately 11 dB gain with sufficient stability.

Stability is very important for the avoidance of undesirable oscillations at different frequencies. The S_{11} parameter is greater than 1 (0 dB) for frequencies between 7-19 GHz which means that the transistor presents an NDR that can potentially generate oscillations.

The stability factor *K* (Equation 6.2) of the transistor is presented in Figure 8.2. With *K* lower than 1, the transistor is potentially unstable for the total frequency range.

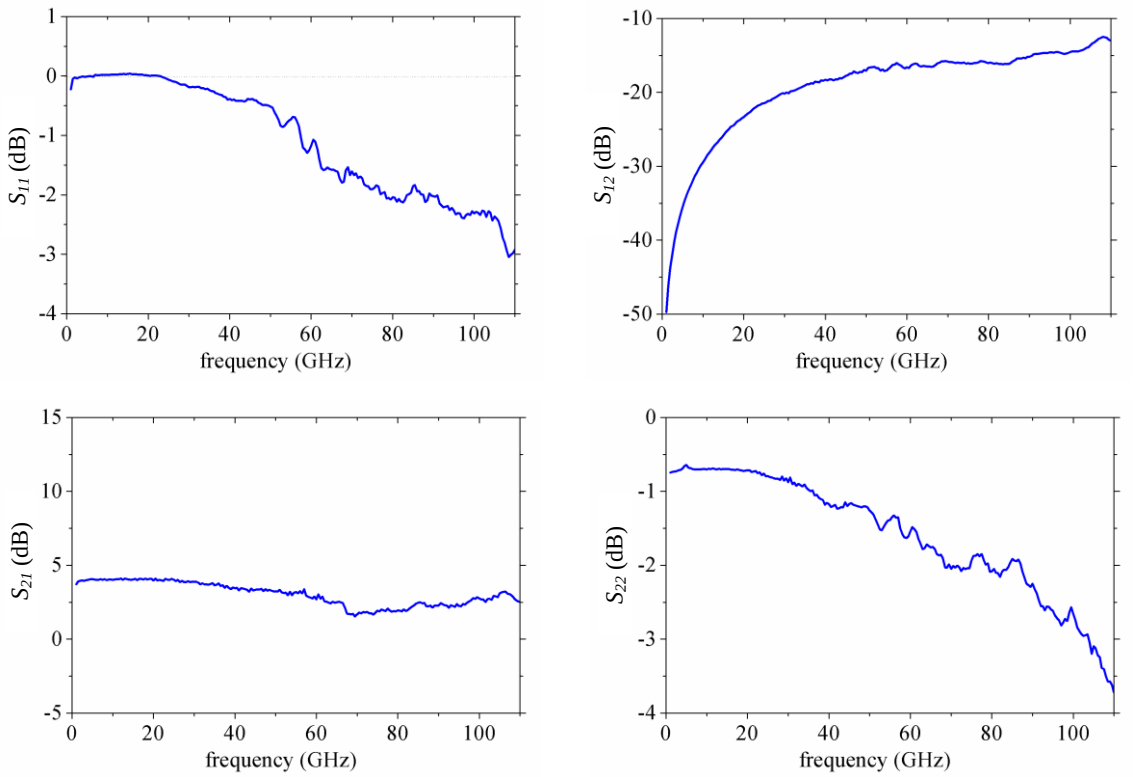


Figure 8.1 S-parameters of the $In_{0.53}Ga_{0.47}As$ HEMT.

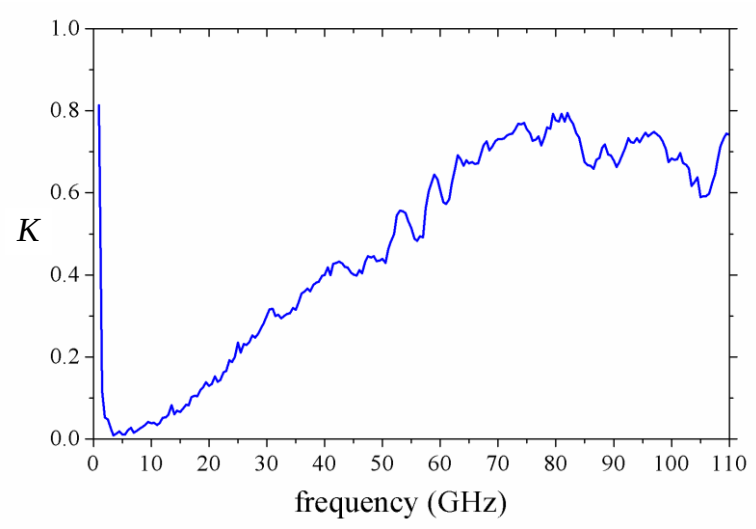


Figure 8.2 Stability factor of the $In_{0.53}Ga_{0.47}As$ HEMT as a function of frequency.

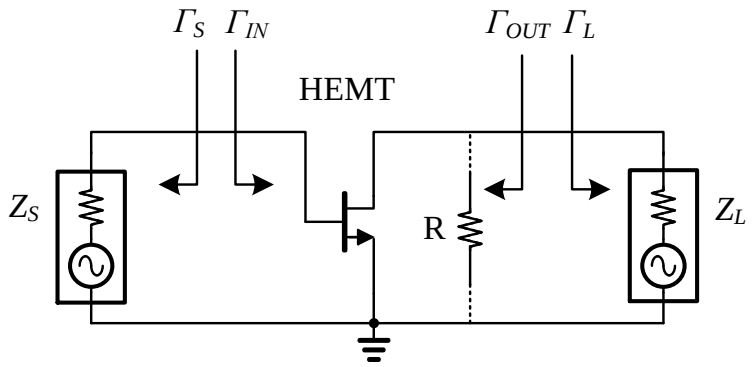


Figure 8.3 The transistor as a two-port network and the addition of a parallel transistor for increased stability.

An additional characteristic of the transistor which is also very important for the amplifier design is the directivity of the device. In the case of a bilateral transistor, the input characteristics of the HEMT will be affected after the connection of a matching network at the output. On the contrary, no effect will occur in the case of a unilateral transistor. A figure of merit for the characterisation of the transistor directivity is given by the ratio of the transducer gains when the device is considered as bilateral and unilateral. The power gain of the transducer, which is defined as the ratio of the power delivered to the load to the power available from the source, is equal to [62]:

$$G_T = \frac{|S_{21}|^2\left(1-|\Gamma_S|^2\right)\left(1-|\Gamma_L|^2\right)}{\left|\left(1-S_{11}\Gamma_S\right)\left(1-S_{22}\Gamma_L\right)-S_{21}S_{12}\Gamma_L\Gamma_S\right|^2} \tag{8.1}$$

Assuming a unilateral transistor, S_{12} equals zero and the transducer power gain is:

$$G_{TU} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \tag{8.2}$$

The ratio of the bilateral to the unilateral gain is bounded by equation 8.3.

$$\frac{1}{\left(1+|X|\right)^2} < \frac{G_T}{G_{TU}} < \frac{1}{\left(1-|X|\right)^2} \tag{8.3}$$

$$X = \frac{S_{12}S_{21}\Gamma_S\Gamma_L}{\left(1-S_{11}\Gamma_S\right)\left(1-S_{22}\Gamma_L\right)} \tag{8.4}$$

The G_T / G_{TU} figure of merit is equal to ± 0.8 dB at 45 GHz and ± 0.95 dB at 60 GHz, increasing with frequency. This is also expected from a quality evaluation of the S_{12} parameter of Figure 8.1. These variations are relatively high and the transistor cannot be considered as unilateral.

The MMIC oscillator was designed for signal generation at 45 GHz. As described in the previous section, no oscillating diodes were detected during the experiments due to the limited material uniformity. Thus, following the f_{osc} - L_{ac} rule reported in [99], two designs were implemented where the L_{ac} of the diodes was selected to be equal to 6 and 8 μm. The complete circuit consists of two general modules; the HEMT amplifier and the Gunn diode with the biasing network. Initially, the design of the HEMT amplifier is described. One of the requirements for the amplifier of the current application is the maximum gain with sufficient stability. A broadband performance is also desired from the circuit for the amplification of oscillations in a wide frequency range. Considering a bilateral and potentially unstable transistor, the design procedure of the amplifier is presented in the next paragraphs.

The desirable stable power gain of the amplifier at 45 GHz is selected to be equal to the maximum capability of the transistor, i.e. 11 dB. The constant operating power gain circle G_p is designed in the Smith chart of the output of the transistor for G_p equal to 11 dB, as presented in Figure 8.4 (a). In the same chart, the output stability circle determines the unstable region. For the simplicity of this short description, the calculation of the constant power gain circles and the stability circles is presented in Appendix A. As shown in Figure 8.4 (a), the whole G_P circle lies in the unstable region of the Smith chart. Thus, there is no possible matching of the output with sufficient stability in the region where the transducer provides 11 dB of power gain. The stability of the transistor can be significantly improved after connecting a parallel resistor at the output [145], as depicted in Figure 8.3. Therefore, the output unstable circle is shifted to the upper side of the Smith chart as presented in Figure 8.4 (b) after the connection of a 250 Ω parallel resistor. The impedance of the load connected to the output is chosen at the point Γ_L of the G_P circle that has the higher distance from the unstable region. Thus, Γ_L was chosen equal to 0.186 - j0.387 which gives Z_L equal to 45.1 - j44.6 Ω.

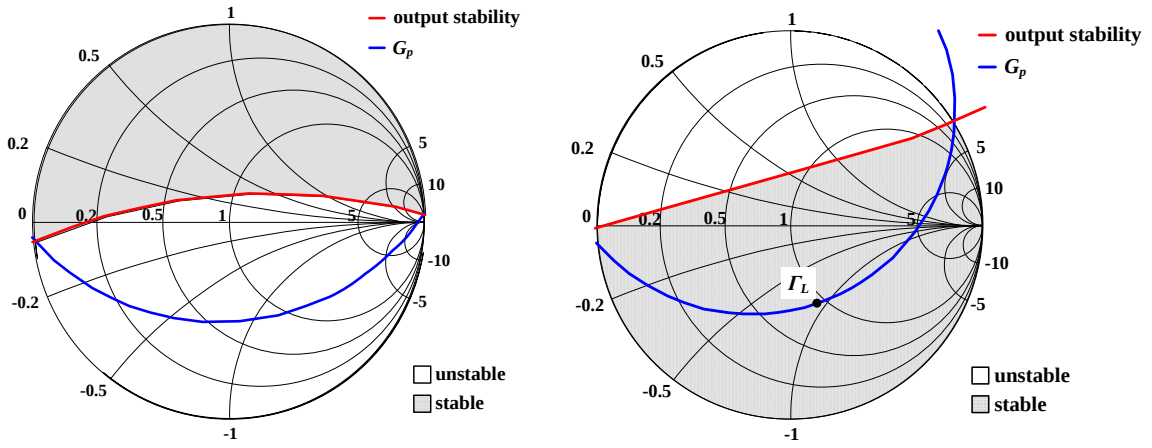


Figure 8.4 Normalised impedance Smith charts of the output of the transistor before (a) and after (b) the connection of the parallel resistor.

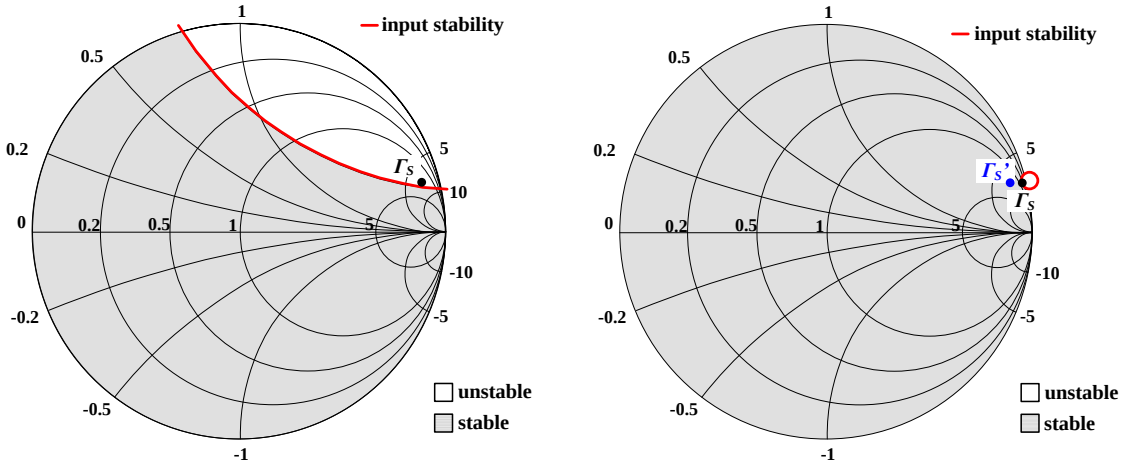


Figure 8.5 Normalized impedance Smith charts of the input of the transistor before (a) and after (b) the connection of the parallel resistor.

Consequently, the output matching network needs to perform an impedance transformation from the load Z_L to the $50\,\Omega$ - standard of the test equipment (Figure 8.6). The source impedance is calculated as follows. Since the transistor in not unilateral, Γ_{IN} is given by Equation 8.5 and the input of the transistor is connected to a network with conjugate load (Equation 8.6) [145].

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{8.5}$$

$$\Gamma_S = \Gamma_{IN}^* \tag{8.6}$$

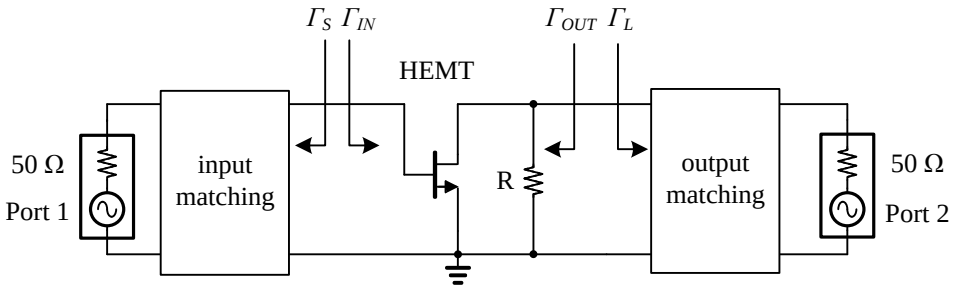


Figure 8.6 The two-port network after the addition of the input and the output matching networks.

The Γ_S load and the input stability circles are depicted in Figure 8.5 before (a) and after the connection of the parallel 250 Ω resistor (b). In both occasions, Γ_S lies on the edge of the stability limit. However, the area of the Smith Chart that is available for stable matching is significantly increased after the introduction of the resistor. This gives a higher flexibility for the design of the input matching network. In this example, the selected load is shifted to the point Γ_S' keeping a small distance away from the unstable region, sacrificing a part of the available gain.

The schematic diagram of the complete MMIC oscillator is illustrated in Figure 8.7. The CPW_4 line with the symmetrical CPW_2 and CPW_3 lines compose an L-matching network which performs an impedance transformation similarly to Figure 3.11 (a). The symmetrical lines are short circuited, from the RF perspective, through the C_3 and C_4 capacitors. In the same way, the output L-matching network consists of the CPW_5, CPW_6 and CPW_7 lines. The two matching networks are connected to the gate and the drain nodes of the HEMT. The L_2 and L_3 inductors are used for decoupling the RF signal that could damage the biasing equipment. The C1 and C7 capacitors perform as RF short circuit connections, isolating the DC biasing of the HEMT from the input/output ports of the amplifier. The design of the MMIC oscillator is complete after the connection of the Gunn diode and the relative biasing circuit. The CPW_1 line feeds the diode with the bias voltage of the pad through the RF-decoupling L_1 inductor. The electrical length of the CPW_1 line is equal to 90^o introducing a 360^o shift in the Smith chart which does not affect the impedance. This also results from Equation 3.13 for a short-circuited line with length equal to λ/4.

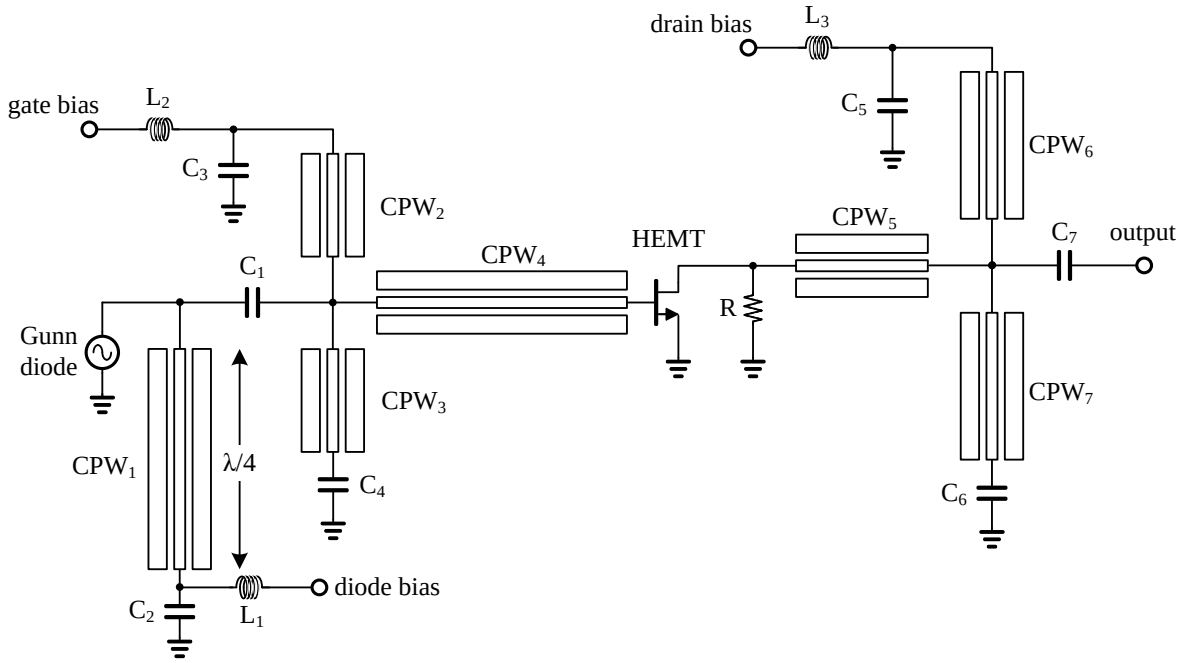


Figure 8.7 Schematic representation of the complete oscillator circuit.

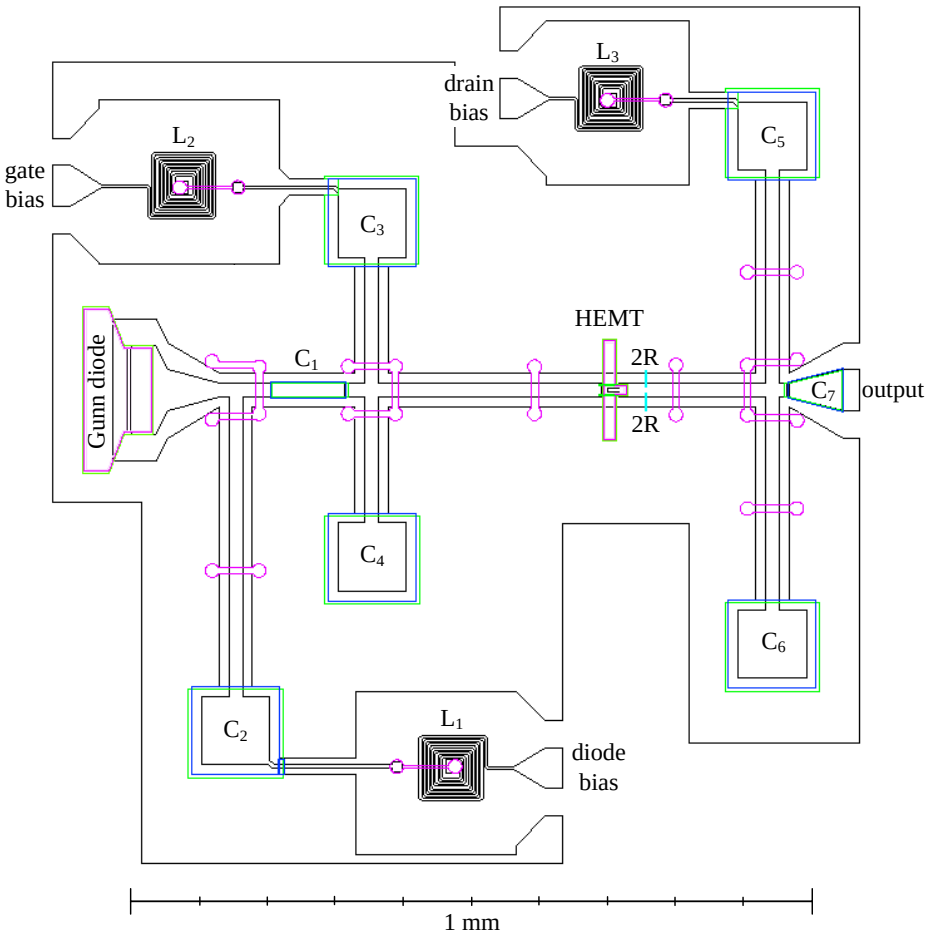
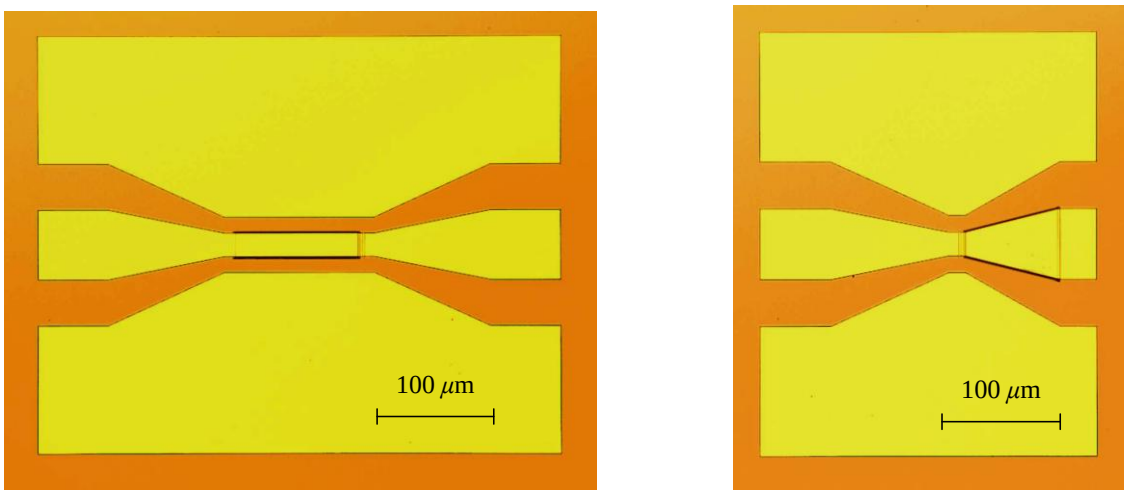


Figure 8.8 Layout design of the complete oscillator circuit.

8.3 Implementation of MIM capacitors

MIM capacitors are simply composed by a Si_3N_4 dielectric layer sandwiched between the two metal electrodes for both series and shunt configurations, as presented in Figure 3.4. The Si_3N_4 film can be formed by following two different techniques. During the conventional method, the dielectric film is deposited after the evaporation of the first metal electrode, covering the entire sample. In this work, a very thin dielectric film equal to 50 nm was selected for the achievement of high values of capacitance. In the second step, a PMMA mask is patterned in order to expose the areas where Si_3N_4 is to be etched. Finally, the undesired film is etched by using an RIE process. On the other hand, the second technique incorporates a simpler approach without the need of the dry etching process. The patterns are initially created on a PMMA bi-layer and the Si_3N_4 film is deposited afterwards. Following a lift-off process, the surrounding dielectric film and the PMMA mask are simply removed after treating the sample with pre-warmed acetone, similarly to the fabrication of the metallic sections. For both techniques, the implementation of the MIM capacitors is completed after the evaporation of the top electrode. The top electrode is considerably thicker than the dielectric film, ensuring continuity with the CPW line. As a result, no use of air bridges is needed.

The Si_3N_4 insulating layer was deposited using the same ICP-CVD room temperature technique applied for the passivation of the active devices. The current technology has demonstrated excellent results for the fabrication of MIM capacitors with very low leakage



(a) (b)

Figure 8.9 Optical image of the fabricated C_1 capacitor (a) and C_7 capacitor (b) in a CPW configuration.

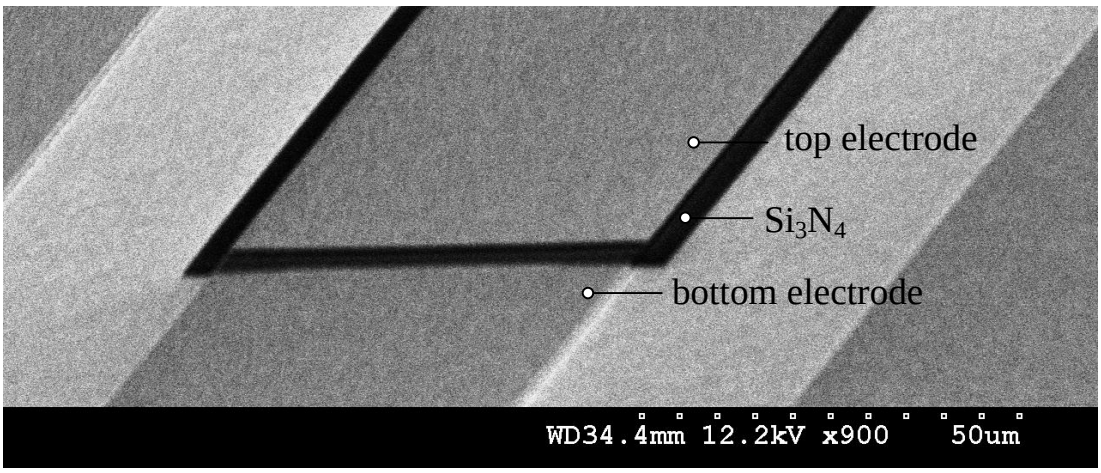


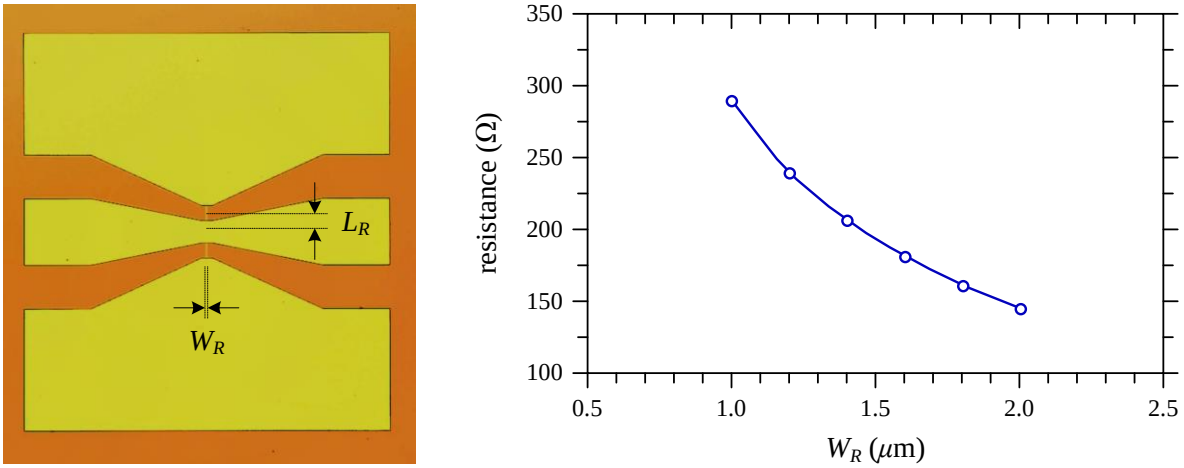
Figure 8.10 Detailed SEM image of the fabricated MIM capacitor.

current, even for Si_3N_4 layers as thin as 5 nm [162]. Figure 8.9(a) presents the fabricated MIM capacitor in a CPW configuration that implements the C_1 capacitor of MMIC oscillator. The capacitor consists of parallel plates covering a total area of 1000 μm^2. The detailed SEM picture of the MIM capacitor is presented in Figure 8.10.In addition, Figure 8.9(b) presents the optical image of the fabricated capacitor that realises C_7 at the oscillator circuit. The parallel plates of the capacitor cover an area equal to 2400 μm^2. The current element also performs the transition from 15/20/15 μm W/G/W geometry to 40/60/45 μm.

8.4 NiCr resistors

The resistors required for the stability of the amplifier are simply implemented by a thin film of nickel – chromium (NiCr). Figure 8.11(a) presents the implemented 250 Ohm resistor in shunt connection, where two shunt resistors of 500 Ohm are connected in parallel. A 33 nm thick layer of NiCr is expected to present 50 Ohm/sq DC resistance [163]. Therefore, an area of 15×1.5 μm^2 is required for the implementation of a 500 Ohm resistor. However, the effect of the parasitic elements that appear at high frequencies causes significant variations to the resulted resistance. A detailed presentation of the high frequency equivalent circuit of thin film resistors can be found in [164].

A set of NiCr resistors with 15 μm length L_R and variable width W_R was fabricated for the identification of the optimum geometry that presents 250 Ohm resistance at 45 GHz. Figure 8.11(b) presents the measured resistance for the various resistors with 1.0-2.0 um W_R, after de-embedding the transition pads. The results indicate a W_R of 1.15 μm for the realisation of 250 Ohm resistors operating at 45 GHz.



(a) (b)

Figure 8.11 Test shunt resistor in CPW configuration (a) and measured resistance at 45 GHz as a function of W_R for L_R equal to 15 μm.

8.5 Air bridge technology

Air bridges are extensively used for the realisation of MMICs. As described in Section 3.3 the interconnections are required for the suppression of the parasitic modes of propagation in CPWs. The air bridges are also needed for the implementation of spiral inductors that block the RF signal in biasing networks.

The creation of air bridges requires the production of a 3D profile on the resist stack that provides a continuous step from the base to the top of the structure. Several techniques have been presented in the past using EBL for the creation of 3D profiles on the resist. Metallic air bridges have been fabricated by exposing the different areas of PMMA using various doses. As presented in [165], an intermediate dose was assigned to the span area so that the required undercut profile for the lift-off was created. The pillar-areas were exposed to higher electron doses for the complete penetration of the resist and the metallisation of the bases on the substrate. A similar approach has been presented in [166] where the acceleration voltage of the beam was varied to create the stepped profiles on the resist. The structures fabricated by these techniques were not higher than 0.5 μm with maximum length of 4 μm. A more sophisticated work has explored the effect of using more than two electron doses for the creation of higher features [167]. The penetration depth was examined extensively as a function of the electron dose and smooth posts with gradient slopes where produced. The penetration of a single layer of PMMA resist was found very sensitive to small dose

variations since a 6 kV acceleration voltage was used. Therefore, AR-U4040 photoresist was preferred for the fabrication of 1.5 μm high and 12 μm long structures.

The main drawback of the techniques described above, is the limited dimensions of the fabricated air bridges. Since a part of the resist needs to be sacrificed for the formation of the lift-off undercut profile, the maximum height of the structure is limited. Relatively low air bridges can degrade significantly the performance of MMICs. The introduced capacitance changes the characteristic impedance of CPWs causing shifts in the resonant frequency [57]. The technology that is applied for the fabrication of the elevated CPWs has illustrated excellent structures with 13 μm height and 200 μm length [168]. However, this technique requires a more complicated fabrication process including a combination of EBL and photolithography for the pattern definition and evaporation, sputtering and electroplating for the metallisation. The air bridge technology used in this work incorporates a two-step EBL technique using polyimide, UVIII and PMMA resists as presented in [169].

The polyimide/UVIII/PMMA technique

The process flow of the current technology is presented in Figure 8.12. Two layers of polyimide are initially spun to form the base layer for the creation of the sloped profile. A layer of UVIII resist is deposited on top where the windows for the creation of the air bridge pillars are developed afterwards. During the development of the UVIII windows, the CD-26 developer also dissolves the polyimide underneath, giving to the structure the required sloped shaping as illustrated in Figure 8.12(d). A PMMA resist mask is spun and exposed in the next steps and the Ti 20 nm/Au 800 nm metal layers are deposited to form the air bridge (steps e-h). In the end of the process, the polyimide under the air bridge is removed using a dry-etch technique with O_2 plasma resulting a high yield over 90 %.

Figure 8.13(a) presents a fabricated air bridge, connecting the two ground planes of a CPW transmission line. The structure is approximately 60 μm long with 2.7 μm height. One main drawback of the current technique is the difficulty of placing the air bridge pillars accurately on the sample. This is caused by the lateral dissolve of the polyimide by the CD-26 developer which is hard to control. As presented in Section 3.3 the air bridge pillar needs to be placed as close as possible to the ground strip edge where electron charge presents the maximum density. Furthermore, the accurate construction of the pillar is also important for the fabrication of spiral inductors for the interconnection of the centre with the access pad. The

same air bridge technology was used for the implementation of the 4.5 turn - turn spiral inductor presented in Figure 8.13(b).

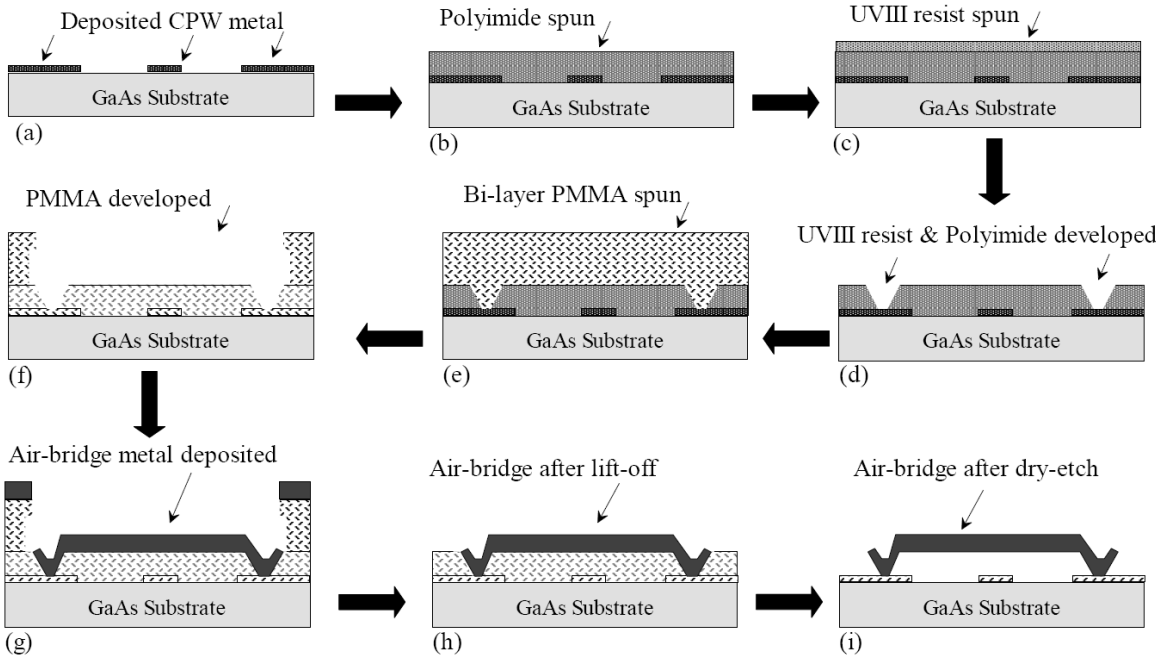
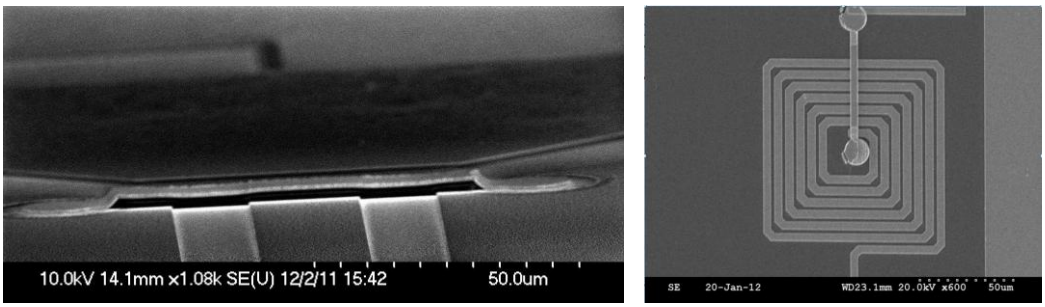


Figure 8.12 Process flow of the polyimide/UVIII/PMMA technique [169].



(a) (b)

Figure 8.13 Fabricated air bridges interconnecting the ground planes of the CPW transmission line (a) and the center with the second terminal of the spiral inductor (b).

The 3D EBL technique

An alternative technique for the fabrication of air bridges was developed in this work using 3D EBL. The main objective of the new method is the accurate placement of the air bridge pillars and the simplification of the fabrication process. The current resist stack consists exclusively of PMMA, where four layers of 15 % PMMA resist were spun to create a layer

with 5 μm thickness. Moreover, a new design was introduced for the lift-off process where the span area was not exposed. In addition, a gradient exposure was initially applied for the creation of the trapezoid profile needed for the air bridge. The desirable profile created on the PMMA is presented in figures 8.14 and 8.15. A second gradient exposure was applied at the sides of the air bridge trapezoid, creating the required discontinuity with the surrounding area for the lift-off process. In contrast with the exposure along the air bridge body, the PMMA at the side patterns should not be exposed down to the substrate. In that case, undesirable metal would be deposited at the sides of the air bridge. One of the main advantages of this concept is that the height of the air bridge is equal to the total resist thickness.

The creation of sloped profiles using 3D EBL has been demonstrated, using the accumulation process occurring at adjacent beam patterns [170]. Therefore, sloped profiles can be created when the resist is exposed to line-patterns with gradient dose after the identification of the optimum width of the lines. Wide lines could cause the formation of low gradient and narrow lines are expected to create very steep profiles. In this work, test patterns were fabricated for the identification of the optimum design where the line width was varied from 50 nm to 1 μm. The structures exposed to 200 nm wide lines presented smooth profiles with slope equal to approximately 45^{o}.

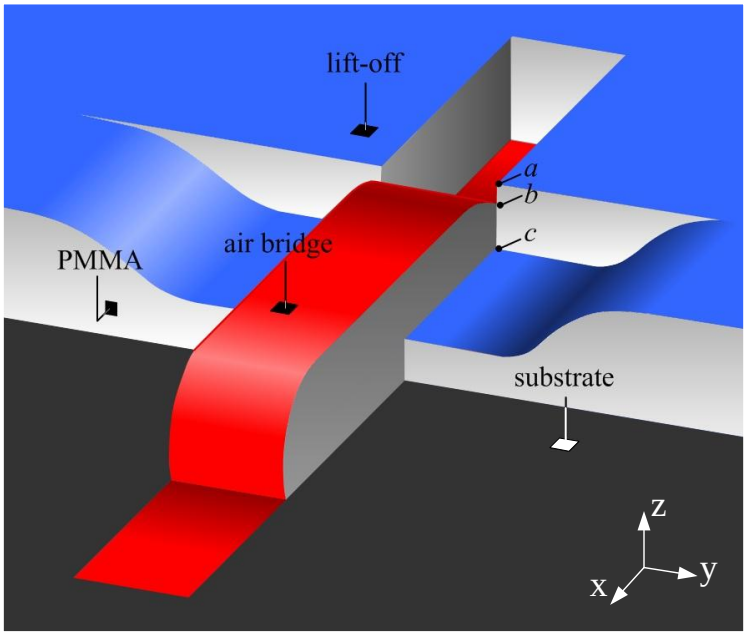


Figure 8.14 The desirable 3D profile created on PMMA. Levels *a*, *b* and *c* indicate the level of the metal to be lifted-off, the level of the air bridge and the intermediate level, respectively [171].

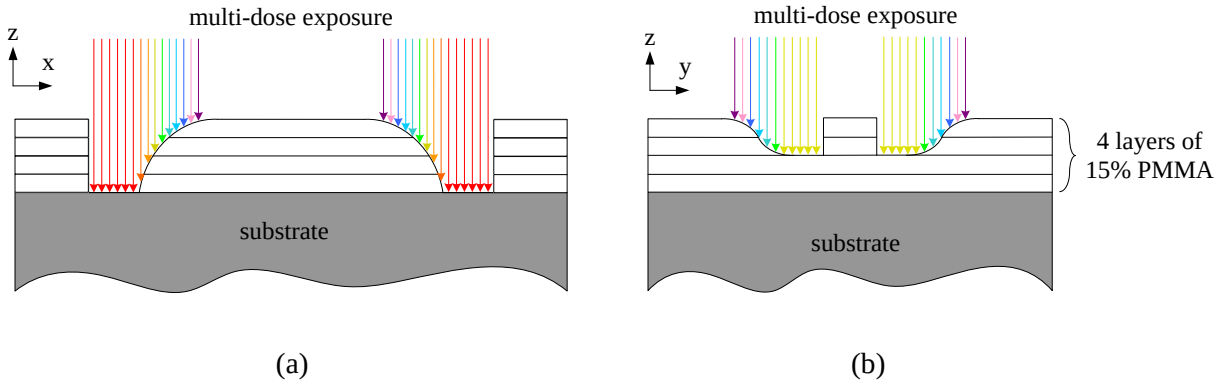


Figure 8.15 The multi-dose exposure of the 4-layer resist stack with respect to the x-axis (a) and the y-axis (b).

In addition to the geometry tests, dose tests were also conducted indicating that the total resist stack is sufficiently exposed to electron doses higher than 520 μC/cm^2. A design example of an air bridge with 10 μm and the corresponding dose map are depicted in Figure 8.16. The side patterns of the structure are exposed to 400 μC/cm^2 electron dose which is sufficient for the removal of approximately 2 μm of the resist stack.

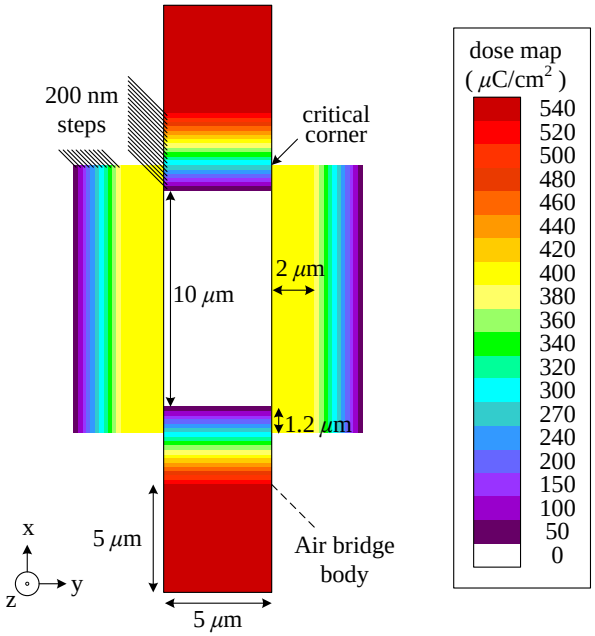
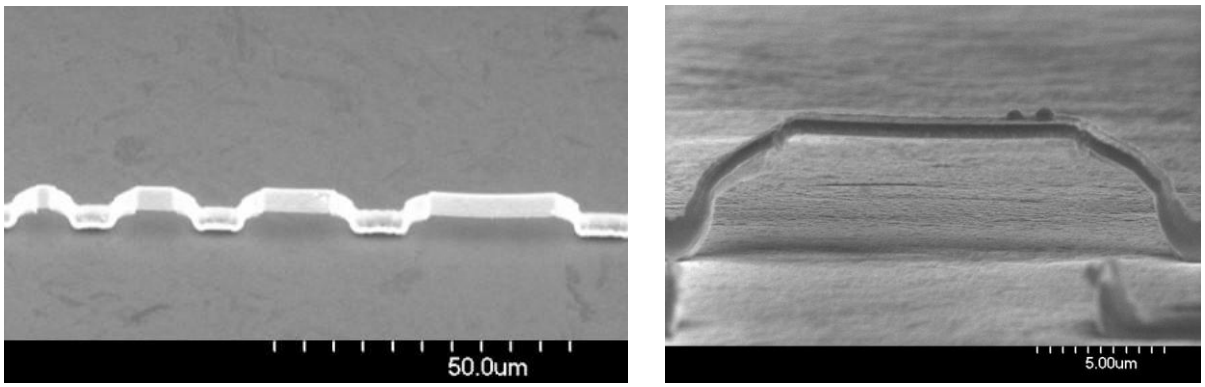


Figure 8.16 Design example of air bridge. The doses corresponding to the colours of the design are illustrated at the dose map.

A set of air bridges with 20 μm width and various lengths was fabricated for the evaluation of the new technique. Figure 8.17(a) presents a group of structures where the maximum length of air bridges with sufficient mechanical stability was equal to 30 μm. Figure 8.17(b) illustrates a side image of the interconnection, where the height of the structure is equal to 5 μm.

The current technique presents excellent placement control with ± 200 nm maximum offset of the pillar in comparison with the designed pattern. Thus, the method is ideal for the implementation of relatively short interconnections where high accuracy is needed, such as the fabrication of multi-finger transistors. However, due to the required wet-etching process, high forces are applied to the air bridges and the fabrication yield of long structures is limited. For these reasons, the polyimide/UVIII/PMMA technique was used for implementation of the interconnections in this work.



(a) (b)

Figure 8.17 Fabricated air bridges with 20 μm width and various lengths [171].

8.6 Fabrication process of the complete MMIC

The individual fabrication techniques described in the previous sections are finally combined for the realization of the complete MMIC, as presented in Figure 8.18. The first step incorporates the evaporation of the Ohmic contacts for the active devices. This step was combined with the evaporation of the alignment markers for the following registration jobs. The isolation of the active devices from the surrounding areas was performed afterwards as illustrated in Figure 8.18(b). The bottom plate of the MIM capacitor was deposited at the third step. The same metal layer was used for the formation of the test pads for the Gunn diode that

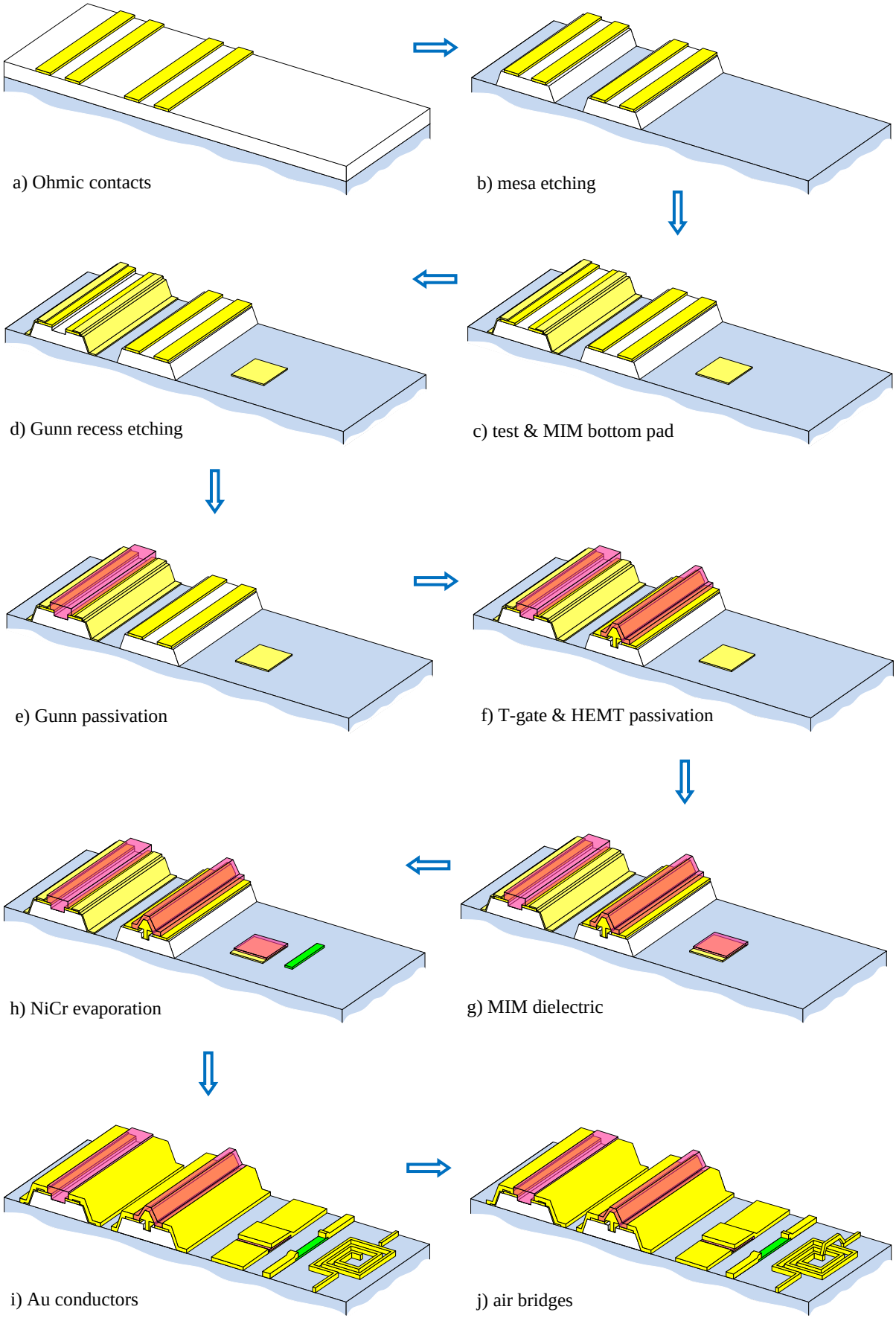


Figure 8.18 Process flow for the fabrication of the complete MMIC (not to scale).

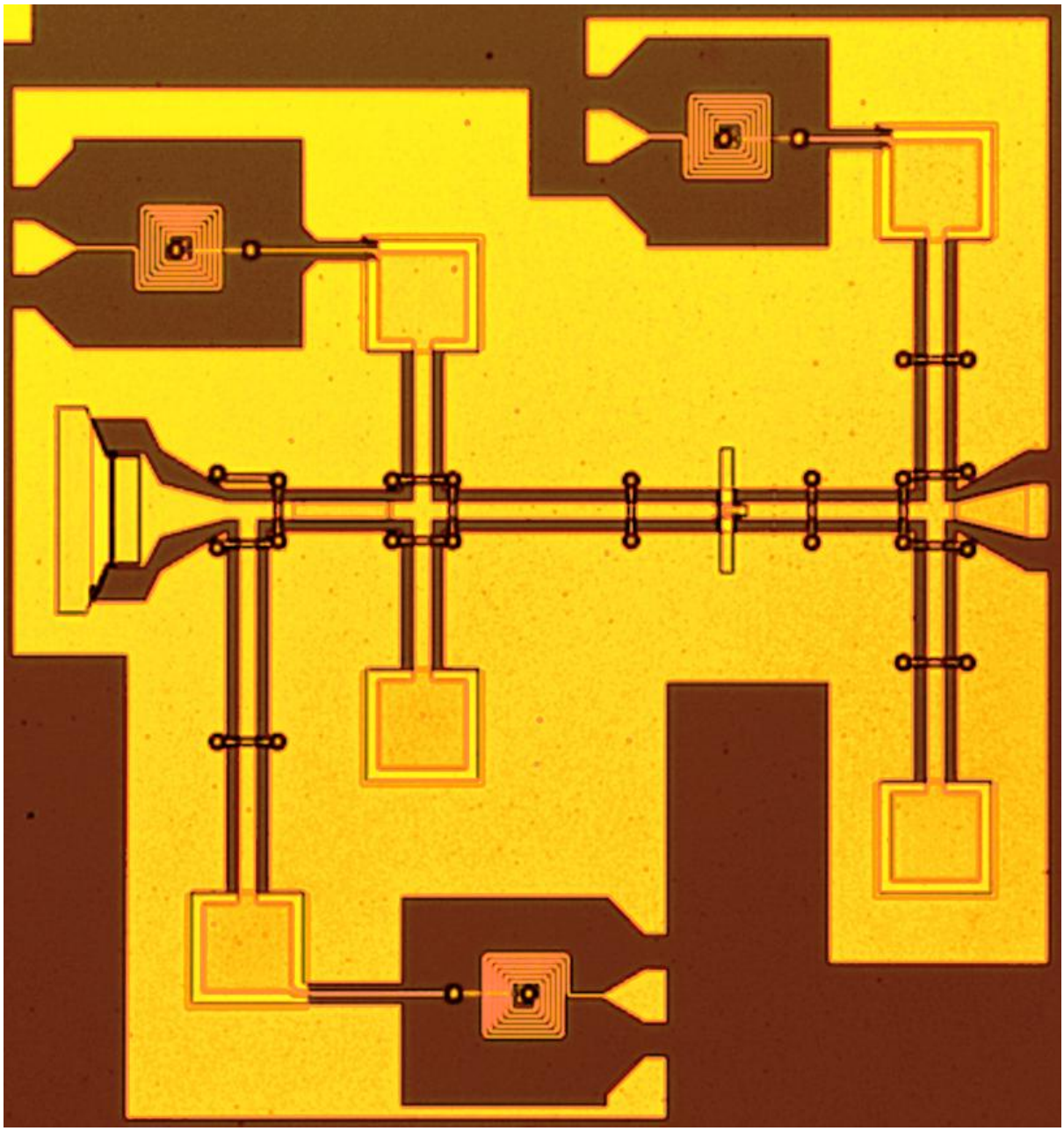


Figure 8.19 Optical image of the fabricated MMIC oscillator.

were used in the next step. The recess etching of the Gunn diode was executed afterwards, as presented in Figure 8.18(d). During this step, the highly doped area between the electrodes of the diode was progressively removed until reaching the target current, as described previously in Section 7.4.1. The area between the electrodes of the diode was passivated with Si_3N_4 immediately after a short de-oxidation treatment. The recess etching of the transistor was performed afterwards, followed by the implementation of the T-gate. The transistor was immediately passivated after the fabrication of the T-gate with a Si_3N_4 layer, as depicted in Figure 8.18(f). The passivation layer needs to be relatively thick, in order to cover sufficiently

the active layers around the area of the T-gate. The thick passivation layer is also vital for the protection of the active devices during the dry etching process needed for the fabrication of the air bridges.

The rest of the procedure is mainly related with the implementation of the passive components. A thin layer of Si_3N_4 was deposited afterwards for the formation of the MIM capacitor. The nichrome (NiCr) layer was deposited in the next step, realising the stabilisation resistor. A thick layer of Au (500 nm) was deposited afterwards to realise the waveguides for both the active and the passive components. Likewise, the CPW access pads of the active devices, the transmission lines, the top plate of the capacitor and the spiral of the inductor were all implemented in this step (Figure 8.18(i)). The fabrication of the MMIC was complete after the implementation of the air bridges, following the polyimide/UVIII/PMMA process presented in Section 7.3.3. The detailed fabrication process of the oscillator circuit is presented in Appendix B VIII. Figure 8.19 demonstrates the complete oscillator circuit after following the fabrication procedure described in this section.

8.7 Results

This section presents the performance of the individual components of the circuit, as well as the performance of the complete MMICs. The RF performance of the C_1 capacitor, after de-embedding the CPW transition pads, is presented in Figure 8.20. The capacitor operates as an excellent RF short - circuit, where the insertion loss is lower than 0.5 dB in the frequency range between 5 - 67 GHz. The return loss is kept below -20 dB in the frequency range between 7 - 67 GHz. The RF performance of the capacitor C_7, after de-embedding the left transition pad, is illustrated in Figure 8.21. Similarly to capacitor C_1, capacitor C_7 presents very low insertion loss and very high return loss. Capacitor C_7 operates as a sort-circuit starting from lower frequencies due to the higher capacitance produced by the larger area of the parallel plates. The measured capacitances at 10 GHz are 2.04 pF and 3.15 pF for C_1 and C_7, respectively. It should be noted that as frequency increases, the series inductance introduced by the dielectric increases as well affecting the overall impedance. As a result, the measured capacitances at 45 GHz are 1.02 pF and 1.12 pF for C_1 and C_7, respectively. The above results indicate that the losses introduced by the transistors are very low for a wide frequency range. In addition, the impedances added by the capacitors can be neglected at 45 GHz.

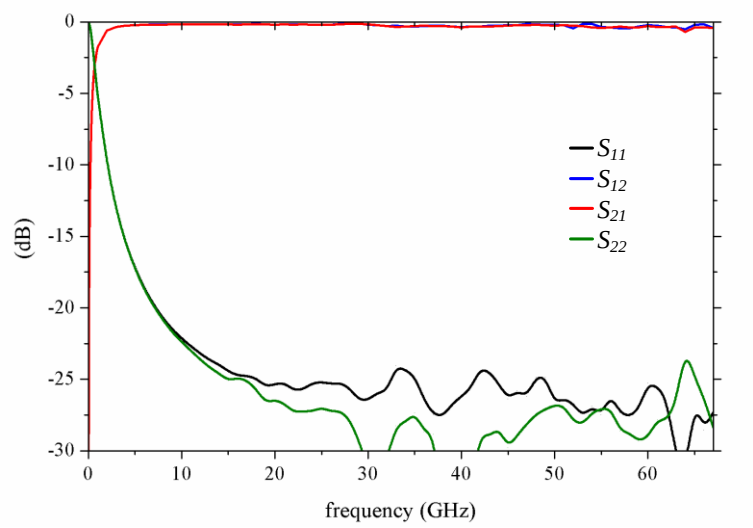


Figure 8.20 Measured *S*-parameters for the C_1 series capacitor.

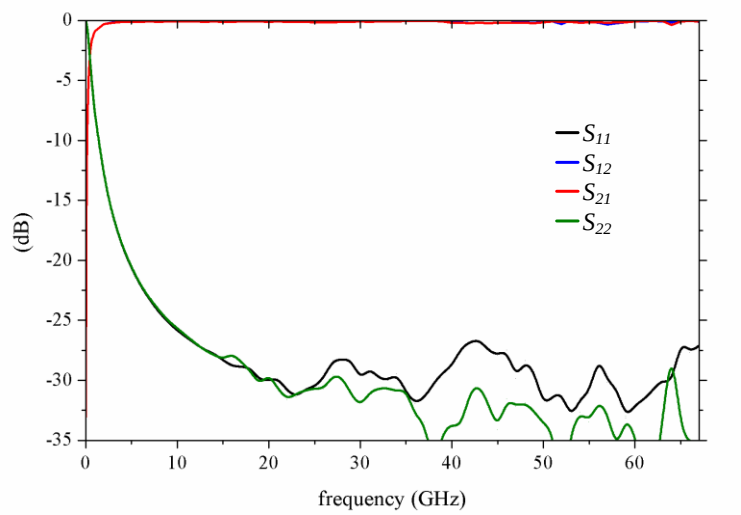


Figure 8.21 Measured *S*-parameters for the C_7 series capacitor.

The isolation between the various ports of the oscillator is presented in Figure 8.22. Figure 8.22(a) presents the *S*-parameters measured between the bias pad of the diode (port 1) and the bias pad of the transistor gate (port 2). The isolation of the two ports remains below -20 dB for the entire frequency range of measurements. The isolation between the bias pad of the transistor drain (port 1) and the output (port 2) is presented in Figure 8.22(b). The insertion loss presents a peak value of -18 dB at 84 GHz, remaining however below -20 dB for a very wide frequency range. The results presented in Figure 8.22(b) indicate the successful small signal decoupling between the output of the amplifier and the DC bias pad of the transistor drain.

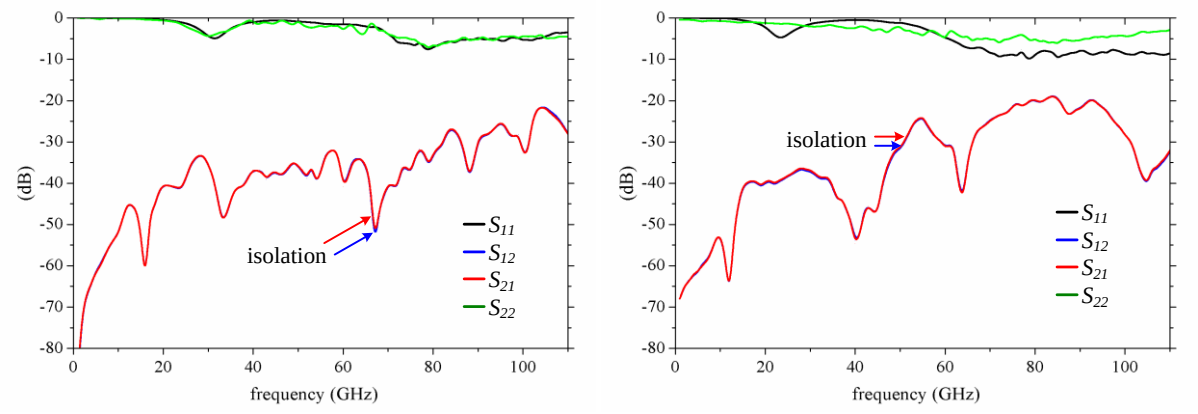


Figure 8.22 Isolation between diode bias pad - gate bias pad (a) and drain bias pad - output pad (b).

The characterisation of the amplifier was performed afterwards, which examined the ability of the circuit next to the Gunn diode to enhance a possible generated signal. For this reason, an amplifier circuit was fabricated next to the complete oscillator on the same chip. The two circuits are almost identical where the only difference between them is the absence of the Gunn diode from the amplifier. Figure 8.23 presents the fabricated amplifier during the characterisation process. The GSG RF probes connected to the VNA are placed at the input and the output of the amplifier, left and right respectively as shown in the picture. At the same time, the DC probes are placed before the RF coils to bias the HEMT. Although the biasing of the diode was not needed in this measurement, the third DC probe is also shown in this picture. Figure 8.24 presents the measured S-parameters of the amplifier. Initially a frequency shift is observed, where the centre frequency of operation is equal to 43 GHz instead of 45 GHz according to the design. However, the amplifier presents high gain equal to 10 dB where the return loss is -6 and -9.5 dB for the input and the output, respectively. The amplifier gain is reduced only by 1 dB in comparison with the *MSG* of the HEMT. The small reduction of the gain is possibly caused by the various loss mechanisms, such as dielectric or radiation losses, or due to the small impedance mismatches between the components.

The -3 dB bandwidth of the amplifier was equal to 2.4 GHz. The relatively narrow bandwidth indicates that the amplifier is not suitable for broadband applications. However, the selective operation of the circuit around the centre frequency is to be expected, considering that the amplifier was designed to extract the maximum stable gain from a single transistor. The successful implementation of the single-stage amplifier that presents sufficient gain,

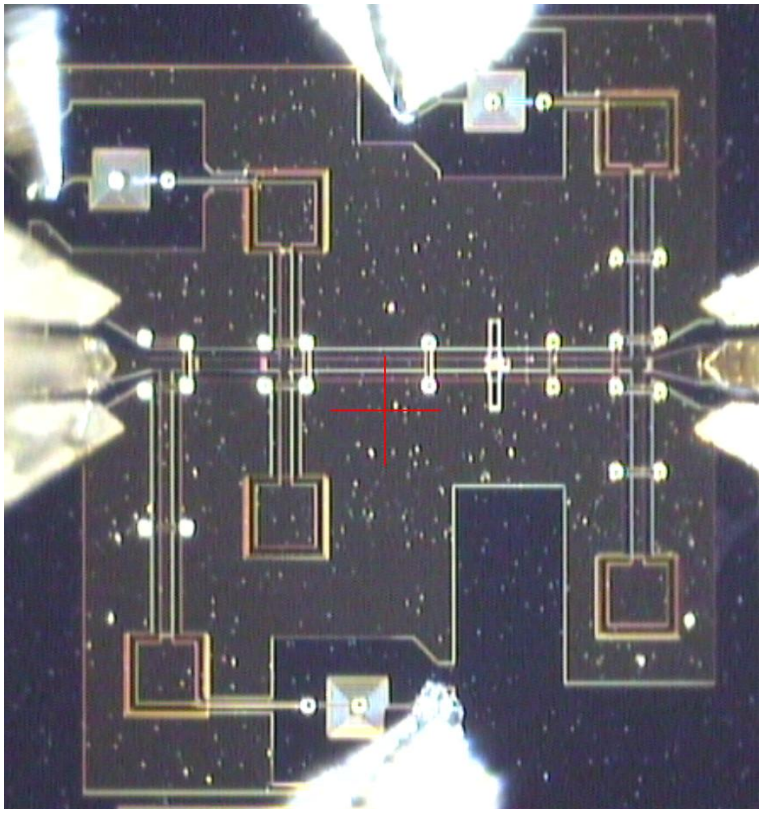


Figure 8.23 The amplifier circuit during the on-chip characterisation process.

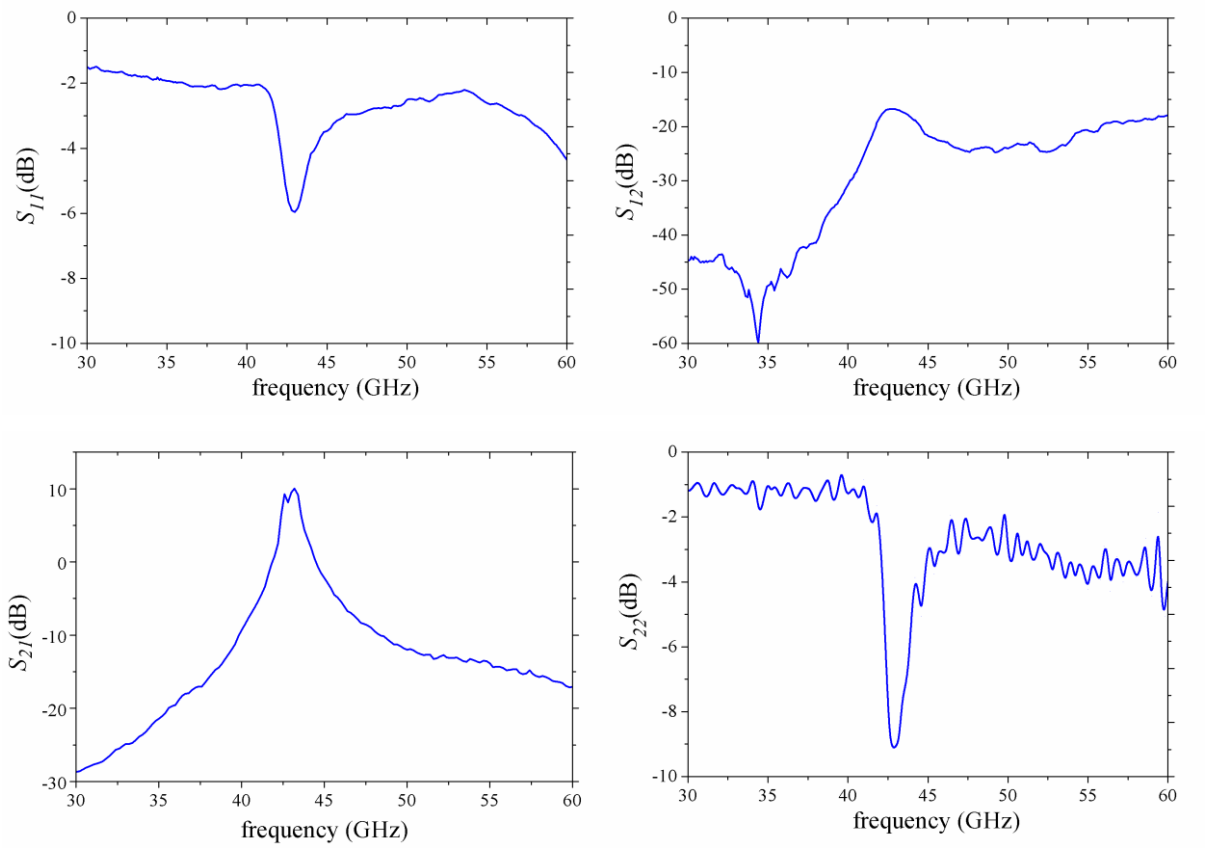


Figure 8.24 S-parameter performance of the amplifier designed at 45 GHz.

demonstrates the potential for a future realisation of circuits with multiple stages. The multi-stage amplifier is expected to present significantly enhanced performance in terms of high gain and broad bandwidth.

The repeatability of the performance presented by the amplifier was also examined during the characterisation of the chip. Figure 8.25 illustrates the measured gain for two identical amplifiers fabricated side by side following the same process. A large variation of the performance can be observed as the second amplifier presents a significantly reduced gain, equal to 3 dB. The two circuits operate at the same centre frequency which is determined by the matching CPW lines. Thus, the degradation of the second amplifier is expected to be caused by the limited performance of the transistor.

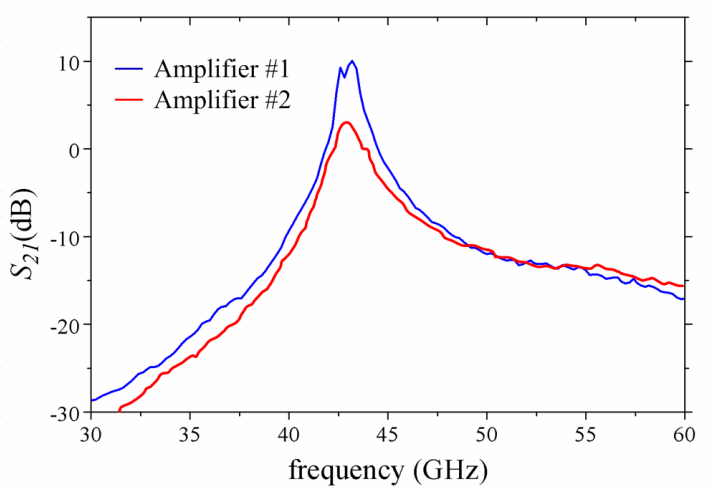


Figure 8.25 Comparison of performance for two identical amplifiers fabricated on the same chip.

Individual transistors were also fabricated across the wafer for testing purposes, such as the examination of the wafer uniformity. Figure 8.26 presents the I_D - V_{DS} characteristics of two HEMTs implemented next to each other. The difference of the performance between the two transistors is enormous, considering that the two devices are located very closely on the wafer. Transistor #1 presents a significantly higher current density of 710 mA/mm when biased at 1.4 V V_{DS} and 0.8 V V_{GS}, where transistor #2 presents 390 mA/mm under the same biasing conditions. The variation of the current density between the two transistors is reflected at the transconductance presented by the two devices, as demonstrated in Figure 8.27. Transistor #1 presents a maximum g_m of 690 mS/mm where the equivalent value for transistor #2 is only 320 mS/mm. It should be noted that transistor #1 also presents a superior

performance over the transistor presented in section 7.4, although the same fabrication process was applied in both cases.

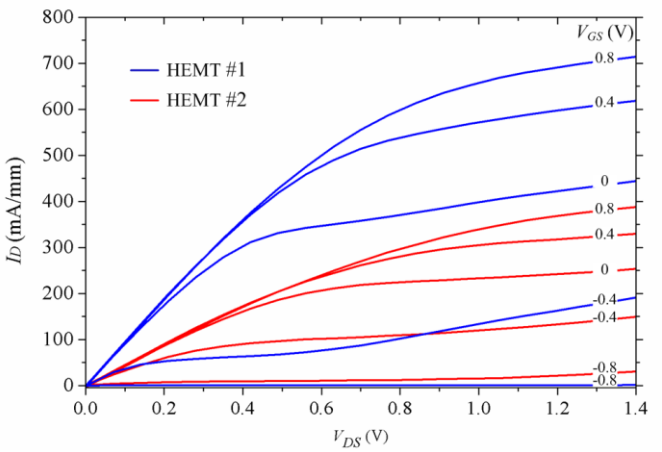


Figure 8.26 Comparison of current density for two identical HEMTs fabricated on the same chip.

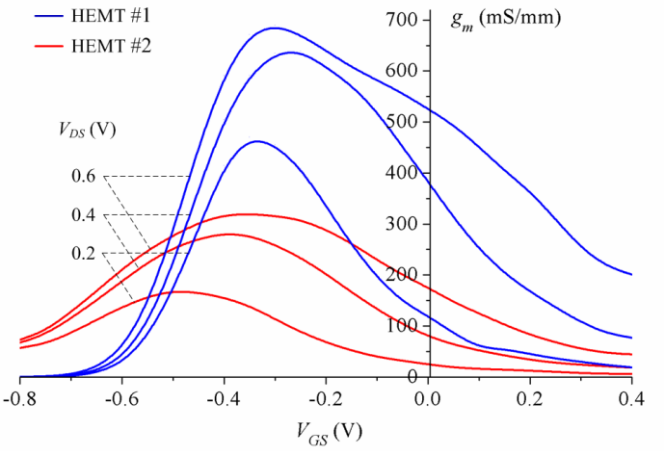


Figure 8.27 Comparison of transconductance performance for two identical HEMTs fabricated on the same chip.

In addition to the test transistors, individual Gunn diodes were fabricated across the wafer. Figure 8.28 presents the *I-V* characteristics of two identical planar Gunn diodes with 8 μm L_{ac} and 120 μm width, fabricated next to each other. Similarly to the variations observed at the transistor performance, the two diodes present current levels that vary by approximately two orders of magnitude.

The large variations presented above, indicate the lack of uniformity observed for the current InP HEMT wafer. This non-uniformity can be misleading while etching the cap layer

between the Gunn diode electrodes, as explained in the following scenario. The Gunn diode #1 of Figure 8.28 was used as a test device to monitor the current reduction during the recess etching process. Thus, Gunn diode #2 was etched for a longer than needed period, presenting a limited current density. It was found that the majority of the Gunn diodes implemented in this fabrication circle presented limited current density, similarly to the device #2.

Prior to the characterisation of the complete MMIC oscillators, the individual Gunn diodes where tested to detect any occurring oscillations. Figure 8.29 illustrates the best obtained diode response after using the VNA characterisation technique. The planar Gunn diode with 8 μm L_{ac} and 120 μm width, presents a peak value of $|S_{11}|$ equal to 3.3 dB centred at 45 GHz. The relatively low $|S_{11}|$ response indicates a small possibility of generated oscillations. The above hypothesis was confirmed after the characterisation of the devices with the spectrum analyser where no oscillations were detected from any device. Similarly to the individual Gunn diodes, no oscillations were detected at the output of the MMIC oscillators.

In conclusion, a significant improvement of the wafer uniformity needs to be conducted for the successful integration of the diode and the HEMT in a MMIC oscillator. The individual results demonstrate the potential of reinforcing the Gunn oscillations through a HEMT based amplifier on the same chip. However, it was not possible so far to fabricate both devices operating in the same circuit. The limited uniformity observed at the current density of the devices is possibly caused by variations of the doping level assigned to the cap layer during the growing process. The Van Der Pauw characterisation technique [172] shall be used in a future investigation of the sheet concentration, before and after removing the cap layer.

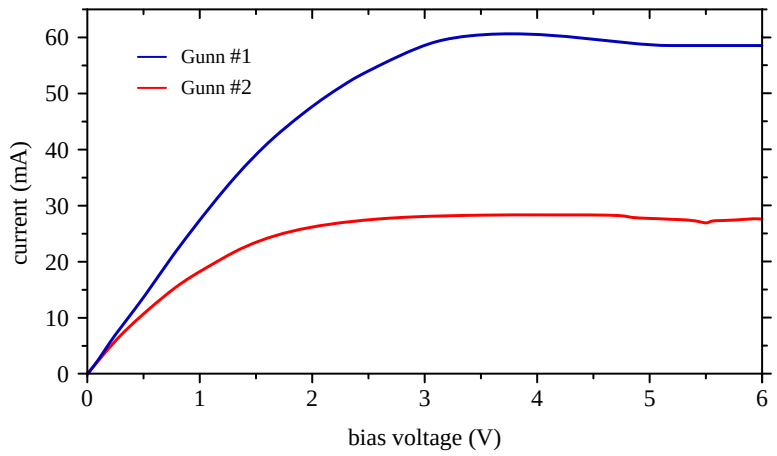


Figure 8.28 Comparison of current level for two identical Gunn diodes with 8 μm L_{ac} and 120 μm width, fabricated on the same chip.

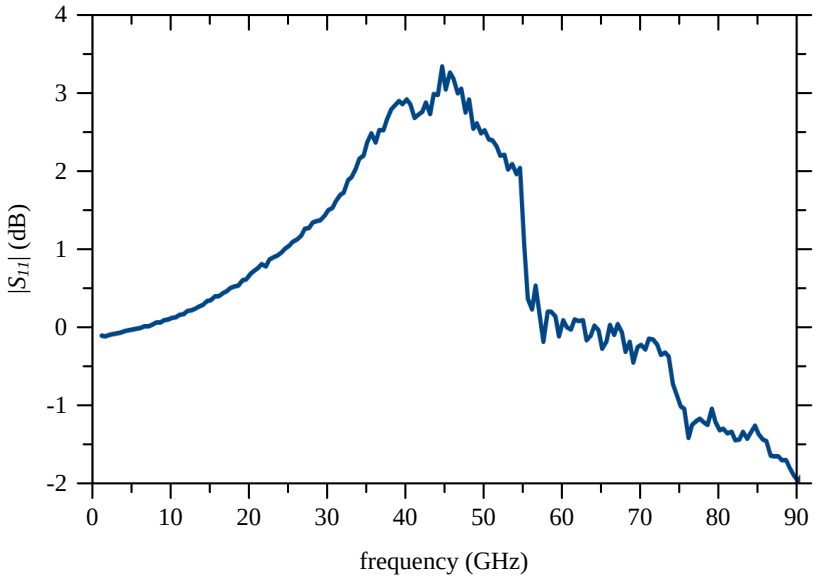


Figure 8.29 The $|S_{11}|$ response versus frequency for a planar Gunn diode with 8 μm L_{ac} and 120 μm width.

8.8 Chapter summary

Following the side-by-side implementation of the two devices, the design procedure of the 45 GHz MMIC oscillator was described in detail. This chapter also examined the design considerations, such as the trade-off between the stability and the gain of the amplifier.

The design, fabrication and characterisation of the individual components, such as the MIM capacitors, the NiCr resistors and the air bridges, were presented before the description of the complete MMIC process flow. The MIM capacitors proved ideal for the required RF coupling between the different circuit nodes, presenting very limited insertion loss over a wide frequency range. In addition to the conventional polyimide/UVIII/PMMA technique, a new technology was presented for the implementation of air bridges. The new technique is based on 3D EBL providing high accuracy of placing the air bridge posts. However, the new technique presents limited fabrication yield and the conventional polyimide/UVIII/PMMA process was followed during the implementation of the MMIC. The single stage amplifier was characterised prior to the complete oscillator, demonstrating very promising results were a maximum gain of 10 dB was measured at 43 GHz. The future connection of multiple amplifying stages is expected to significantly enhance not only the available gain but also the bandwidth of the amplifier.

Despite the successful implementation of the individual elements, the realisation of the complete MMIC oscillator was hindered by the limited uniformity of the wafer. The latter decreases dramatically the possibility of a simultaneous operation of the two devices. Thus, no functional complete circuits were detected and no oscillations were detected at the outputs of the MMICs. The limited uniformity observed between the different devices is probably caused by variations at the doping level of the cap layer. The material quality shall be evaluated after the performance of Van Der Pauw measurements. The future growth of a uniform wafer is a task of high importance for the fabrication of the complete MMIC oscillators.

9. Conclusions and future work

The growing interest on mm-wave and THz applications introduces new challenges for the development of the active and the passive elements, as discussed in the introduction. Oscillators and transistors are fundamental active components required for the implementation of complete systems. Planar Gunn diodes generate oscillations demonstrating excellent high frequency performance that has entered the THz regime. HEMTs are key circuit elements for mm-wave and THz applications, presenting low noise and high gain characteristics.

This work was focused on the enhancement of the signal generated from the diode through a transistor based amplifier. Prior to the final implementation of the complete MMIC, a large number of tests was conducted and new techniques were explored, focused on the fabrication of the active elements.

The fabrication of the two devices was initially explored using separate GaAs based wafers that were optimised individually for the diode and the transistor. Following the conventional fabrication process of planar Gunn diodes, it was found that the citric acid solution etches rapidly the cap layer between the electrodes. In addition, the results could not be repeated since large variations of the etching rate were observed between the individual tests. The wet etching solution was then replaced by a succinic acid mixture with adjusted pH which has been traditionally used for the recess etching process of HEMTs. The succinic acid solution presented better control and repeatability over the citric acid solution, leading to the implantation of the first functional planar Gunn diodes of this work.

Etching tests were also performed for the fabrication of transistors on a GaAs pHEMT wafer, using the same succinic acid solution that was used for the diodes. A conventional gate terminal with 250 nm width was initially used for the modulation of the channel. The first operational devices presented a maximum g_m equal to 450 mS/mm. The f_{max} and the f_T of the devices were equal to 75 GHz and 68 GHz, respectively. These results were very encouraging considering the increased parasitics introduced by the wide gate area.

A new sub-100 nm T-gate technology was developed afterwards, for the enhancement of the small-signal and the high frequency performance of the pHMETs. A multi-dose EBL technique was applied on a PMMA/Al/PMMA stack for the formation of the required stepped profile. The new technique demonstrated T-gates with 70 nm length and excellent fabrication yield. Various fabrication and geometry aspects were examined in following tests. An optimum compromise between high performance and fabrication yield was found for devices with 1.5 μm L_{DS} and 12.5 μm width. The current pHEMTs presented a g_m equal to 750 mS/mm, and enhanced high frequency performance with f_{max} and f_T equal to 190 GHz and 170 GHz, respectively.

Two different approaches were followed afterwards for the implementation of both the planar Gunn diode and the HEMT on the same substrate. A combined wafer was initially designed, including the active layers of both devices on a GaAs substrate. The bottom Gunn diode layers and the top pHEMT layers were separated by a thick buffer layer. The pHEMT and the buffer layers were removed at the desirable areas for the fabrication of the diodes by following a hybrid fabrication process. An RIE and a wet etching process were combined for the uniform and controlled removal of the top layers. An interferometer was used during the RIE process monitoring the depth of the etched material in real time, thus indicating the end of the process. Low quality Ohmic contacts resulted from the relatively thick cap layer of the diode that limited the diffusion of the metal alloy in the semiconductor. Thus, the high access resistance to the channel hindered the generation of any oscillation.

The two devices were successfully implemented on the same substrate for the first time, after using a pHEMT GaAs wafer. The side-by-side approach presented advanced simplicity over the combined wafer, since the two devices shared the majority of the fabrication steps. Planar Gunn diodes fabricated on the pHEMT wafer demonstrated oscillations at 87.6 GHz with -40 dBm generated power. Despite the encouraging results, the power level of the diode was very low for any attempt of amplification.

The same side-by-side approach was applied afterwards on an InP based HEMT wafer with lattice matched $In_{0.53}Ga_{0.47}As$ channel and cap layers. The superior properties of the channel layer and the high-quality Ohmic contacts, led to a significant reinforcement of the high frequency performance of both devices compared to the GaAs substrate. Transistors with 70 nm T-gates demonstrated f_{max} and f_T equal to 330 GHz and 220 GHz, respectively. At the

same time, fundamental oscillations at 204 GHz were detected from planar Gunn diodes with 1 μm L_{ac} generating -7.3 dBm maximum power.

The design and the fabrication procedure of a MMIC oscillator operating at 45 GHz were presented afterwards. The MMIC oscillator was realised after the combination of the planar Gunn diode and the HEMT based amplifier. A number of passive elements was used to compose the matching and the biasing networks of the complete circuit. MIM capacitors were used for the DC isolation between the various nodes, introducing very small insertion losses around 0.5 dB in a wide frequency range. A new technique was developed for the implementation of air bridges, using a single step 3D EBL process on a PMMA multi-layer stack. The new technique presented excellent placement control of the posts within a range of ±200 nm. However, the structures presented limited mechanical stability during the final wet etch process and the implementation of interconnections longer than 30 μm was not feasible. Thus, the polyimide/UVIII/PMMA technique was selected for the fabrication of the air bridges in this work.

Following the fabrication of the complete MMICs, the circuits were finally characterised. The single stage amplifier presented excellent characteristics, providing 10 dB of fain at 43 GHz. However, limited repeatability of the results was observed after the characterisation of similar circuits on the same chip. Large variations were also detected at the performance of single transistors fabricated next to each other. Thus, no oscillations were detected from any circuit fabricated on the final chip. The future growth of a uniform InP HEMT wafer is fundamental for the successful integration of the two devices in the same MMIC.

A large number of developments could further improve the performance of both devices in the future. Starting from the transistor gate terminal, the reduction of the gate length bellow 70 nm is expected to reinforce the gain and the high frequency performance of the device. Although the current single-step 70 nm T-gate technology presents simplicity and reliability, the minimum gate length is limited by the increased forward scattering of the electron beam. This effect can be significantly decreased with the introduction of a two-step exposure. In the first step, the “head” area could be exposed to the low-dose beam and get developed afterwards. During the second step, the high-dose beam used for the “foot area” would be subject to less scattering, penetrating a resist layer with reduced thickness.

Since no annealing treatment is required for the formation of the Ohmic contacts, the implementation of self-aligned electrodes could additionally improve the transistor performance. Relevant tests were presented in Section 6.3.5 demonstrating the compatibility of the current technology with the self-aligned process.

The development of the InP HEMT layer structure could benefit both the transistor and the diode. The introduction of a second layer of δ-doping is expected to increase significantly the current density of the two devices. The introduction of additional channel layers could also reinforce the current level of the devices. Although this solution is recommended for the diode, the large distance between the bottom channels and the transistor gate is expected to cause reduced control of the current. Thus, the deeper channel layers would not be completely depleted and the devices could present multiple peaks at the g_m-V_{GS} characteristic. However, one additional channel can be used, reinforcing the transconductance of the transistor [173] and the current density of the diode.

Further improvement of the HEMT layer structure can be conducted with the increment of the indium content in the channel which leads to higher electron mobility. Strained $In_xGa_{1-x}As$ channel layers with $x \geq 0.7$ can be grown on a metamorphic structure based on InP. The increased indium element can also improve the electron confinement in the channel due to the increased band discontinuity between the channel and the barriers. The higher electron mobility presented in the strained channel could also lead to the extraction of oscillations at higher frequencies.

In conclusion, the side-by-side implementation of the planar Gunn diode and the HEMT on the same chip has undoubtedly proved the potential for the integration of the two devices on the same MMIC. However, the growth of a uniform InP HEMT wafer is vital for the future integration of the two devices. A large number of developments is also expected to further improve the performance of both devices, as described in the previous paragraphs.

Appendix A

The complete elliptic integrals are given by [51]:

$$K(k_n) / K(k_n') = \pi / \ln[2(1+\sqrt{k'}) / (1-\sqrt{k'})] \qquad \text{for } 0 \le k_n \le 0.707$$

$$K(k_n) / K(k_n') = (1/\pi)\ \ln[2(1+\sqrt{k}) / (1-\sqrt{k})] \qquad \text{for } 0.707 \le k_n \le 1$$

$$k_0 = S / S + 2W$$

$$k_1 = \sinh(\pi S / 4h) / \sinh\{[(\pi(S + 2W)]/4h\}$$

$$k_n' = \sqrt{(1 - k_n^2)}$$

where *S*, *W* and *h* the geometric parameters of the structure as presented in Figure 3.1.a.

Transformation from *x*-*r* to *U*-*V* coordinates for impedance mapping at the Smith chart [62] :

$$\Gamma = U + jV = (r - 1) + jx / (r + 1) + jx$$

$$U = r^2 - 1 + x^2 / (r + 1)^2 + x^2$$

$$V = 2x / (r + 1)^2 + x^2$$

Transformation formulas between the *S* and the *T* parameters [83]:

$$\begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} = \begin{bmatrix} \frac{1}{S_{21}} & -\frac{S_{22}}{S_{21}} \\ \frac{S_{11}}{S_{21}} & S_{12} - \frac{S_{11}S_{22}}{S_{21}} \end{bmatrix}$$

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{T_{21}}{T_{11}} & T_{22} - \frac{T_{21}T_{12}}{T_{11}} \\ \frac{1}{T_{11}} & -\frac{T_{12}}{T_{11}} \end{bmatrix}$$

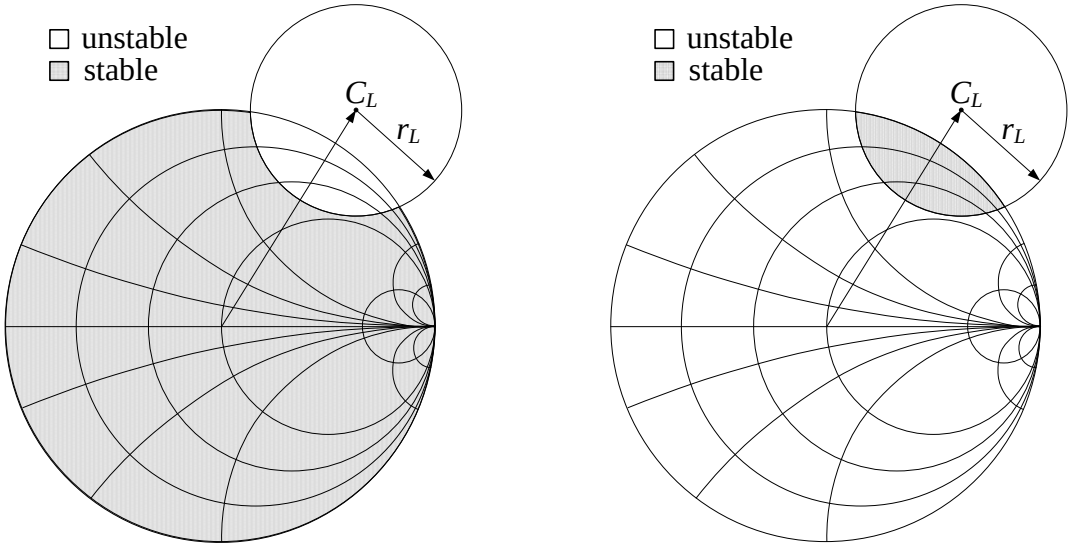
Calculation of stability circles [145]:

Output stability circle:

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

$$r_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \qquad \text{(radius)}$$

$$C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)^*}{|S_{22}|^2 - |\Delta|^2} \qquad \text{(centre)}$$

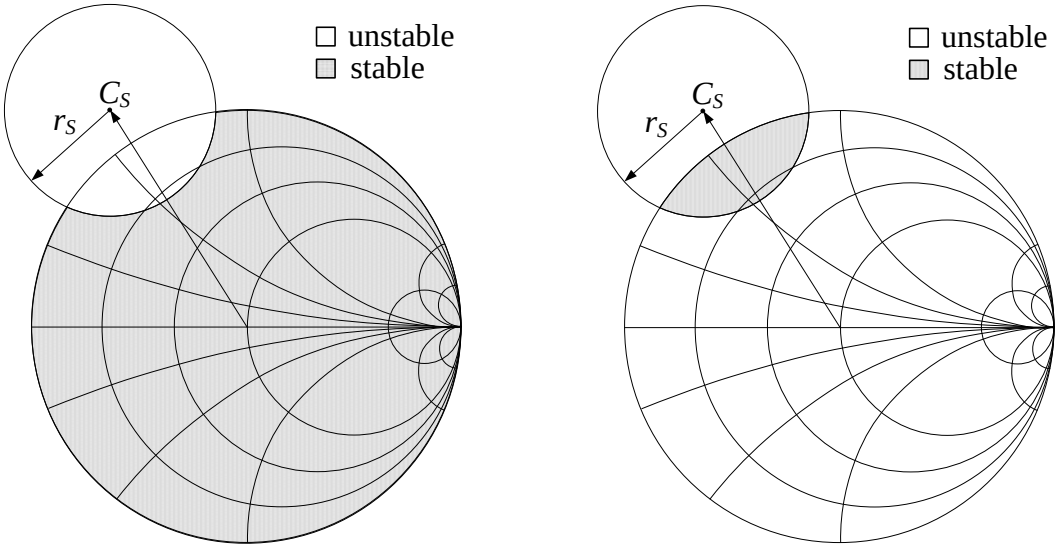


$|S_{11}| < 1$ $\qquad$ $|S_{11}| > 1$

Input stability circle:

$$r_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \qquad \text{(radius)}$$

$$C_S = \frac{\left(S_{11} - \Delta S_{22}^*\right)^*}{|S_{11}|^2 - |\Delta|^2} \qquad \text{(centre)}$$



$|S_{22}| < 1$ $|S_{22}| > 1$

Operating power gain circles [145]:

$$g_P = \frac{1-\left|\Gamma_L\right|^2}{\left|1-S_{22}\Gamma_L\right|^2-\left|S_{11}-\Delta\Gamma_L\right|^2}$$

$$C_2 = S_{22}-\Delta S_{11}^*$$

$$C_P = \frac{g_P C_2^*}{1+g_P\left(\left|S_{22}\right|^2-\left|\Delta\right|^2\right)} \qquad \text{(centre)}$$

$$r_P = \frac{\sqrt{1-2K\left|S_{12}S_{21}\right|g_P+\left|S_{12}S_{21}\right|^2 g_P^2}}{\left|1+g_P\left(\left|S_{22}\right|^2-\left|\Delta\right|^2\right)\right|} \qquad \text{(radius)}$$

Appendix B

B I. Planar Gunn diode on C230 GaAs substrate

1. Markers & ohmic contacts

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ Pd 20 nm/Ge 50 nm/Au 10 nm/Pd 50 nm/Au 100 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse
Annealing	20 s 320 ^{o}C → 60 s 400 ^{o}C

2. Mesa isolation

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water
Spin resist	80 % UVIII @ 4 krpm 60 s → 90 s hotplate baking @ 138^{o}C
Exposure	Dose 60 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	H_2O rinse → 15 s CD-26 @ room T → H_2O rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 3 min 10:1 $C_6H_8O_7$:H_2O_2 → electrical test → additional etching if required

3. CPW pads & composite contacts

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s

Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

4. Recess etching

Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse → ~ 120 s 5.9 pH succinic acid @ 22.5 ^oC → electrical test → etching until reaching the target current of 40 mA for 60 μm wide devices

B II. pHEMT on GaAs with conventional 250 nm gates

1. Markers & ohmic contacts

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse
Annealing	20 s 320 ^{o}C → 60 s 400 ^{o}C

2. Mesa isolation

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 2 hr oven @ 180^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	IPA rinse → 30 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 3 min 10:1 $C_6H_8O_7$:H_2O_2 → electrical test → additional etching if required

3. 250 nm gate fabrication

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 900 μC/cm^2 , resolution 1.25 nm, VRU 4, Spot 4nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Recess etching	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 15 s 5.9 pH succinic acid @ 22.5 ^{o}C

Metallise	10 s 10:1 H_2O:HF de-ox → 60 s H_2O rinse
	→ Ti 15 nm/ Pt 15 nm/Au 400 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

4. CPW pads

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^oC
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^oC
Exposure	Dose 350 $\mu C/cm^2$, resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^oC → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

B III. pHEMT on GaAs with 70 nm T-gates

1. Markers & ohmic contacts

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse
Annealing	20 s 320 ^{o}C → 60 s 400 ^{o}C

2. Mesa isolation

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 2 hr oven @ 180^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	IPA rinse → 30 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 3 min 10:1 $C_6H_8O_7$:H_2O_2 → electrical test → additional etching if required

3. 70 nm T-gate fabrication

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Metallisation	10 nm Al
Spin resist	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	“Head” : Dose 430 μC/cm^2 , resolution 1.25 nm, VRU 10, Spot 8nA

	"Foot" : Dose 940 μC/cm^2 , resolution 1.25 nm, VRU 4, Spot 4nA
Develop	IPA rinse → 45 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
	H_2O rinse → 100 s CD-26 @ room T → H_2O rinse 15 s
	IPA rinse → 40 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Recess etching	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 17 s 5.9 pH succinic acid @ 22.5 ^{o}C
Metallise	10 s 10:1 H_2O:HF de-ox → 60 s H_2O rinse
	→ Ti 15 nm/ Pt 15 nm/Au 400 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

4. CPW pads

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

B IV. Planar Gunn diode on GaAs combined wafer

1. Removal of pHEMT & buffer layers

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	HSQ @ 2 krpm 60 s → 15 m hotplate baking @ 90^{o}C
Exposure	Dose 400 μC/cm^{2} , resolution 1.25 nm, VRU 8, Spot 8nA
Develop	30 s TMAH @ 21 ^{o}C → H_2O rinse 30 s → H_2O rinse 30 s → IPA rinse 15 s
Dry etching	RIE $SiCl_4$: 18 sccm, 100 W, 9 mTorr, following interferometer
Wet etching	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse → 5 min 5.9 pH succinic acid @ 22.5 ^{o}C → profilometer inspection → additional etching if required → 30 s 10:1 H_2O:HF → 60 s H_2O rinse

2. Markers & ohmic contacts

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C 2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^{2} , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse → Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse
Annealing	20 s 280 ^{o}C → 60 s 360 ^{o}C

3. Mesa isolation

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 2 hr oven @ 180^{o}C
Exposure	Dose 350 μC/cm^{2} , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	IPA rinse → 30 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse

→ 3 min 10:1 $C_6H_8O_7$:H_2O_2 → electrical test → additional etching if required

4. CPW pads & composite contacts

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

5. Recess etching

Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ ~ 360 s 5.9 pH succinic acid @ 22.5 ^{o}C → electrical test → etching until reaching the target current of 40 mA for 60 μm wide devices

B V. Side by side implementation on GaAs pHEMT wafer

1. Markers & ohmic contacts for pHEMTs & Gunn diodes

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse
Annealing	20 s 320 ^{o}C → 60 s 400 ^{o}C

2. Mesa isolation for pHEMTs & Gunn diodes

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 2 hr oven @ 180^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	IPA rinse → 30 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 3 min 10:1 $C_6H_8O_7$:H_2O_2 → electrical test → additional etching if required

3. 70 nm T-gate fabrication

Clean substrate	5 min ultrasonic acetone → 5 min ultrasonic IPA → 3 min DI water rinse
Spin resist	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Metallisation	10 nm Al
Spin resist	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	“Head” : Dose 430 μC/cm^2 , resolution 1.25 nm, VRU 10, Spot 8nA

	"Foot" : Dose 940 μC/cm^2 , resolution 1.25 nm, VRU 4, Spot 4nA
Develop	IPA rinse → 45 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
	H_2O rinse → 100 s CD-26 @ room T → H_2O rinse 15 s
	IPA rinse → 40 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Recess etching	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 17 s 5.9 pH succinic acid @ 22.5 ^{o}C
Metallise	10 s 10:1 H_2O:HF de-ox → 60 s H_2O rinse
	→ Ti 15 nm/ Pt 15 nm/Au 400 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

4. Protection of pHEMTs & Gunn diode recess etching

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ ~ 7 s 5.9 pH succinic acid @ 22.5 ^{o}C → electrical test → etching until reaching the target current of 35 mA for 60 μm wide devices

5. CPW pads

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

B VI. Side by side implementation on InP HEMT wafer

1. Markers & ohmic contacts for pHEMTs & Gunn diodes

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

2. Mesa isolation for pHEMTs & Gunn diodes

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 2 hr oven @ 180^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	IPA rinse → 30 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 2 min 1:1:100 H_3PO_4:H_2O_2:H_2O → electrical test → additional etching if required

3. Protection of HEMTs & Gunn diode recess etching

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ ~ 5 s 5.9 pH succinic acid @ 22.5 ^{o}C → electrical test → etching until reaching the target current of 60 mA for 120 μm wide devices

4. 70 nm T-gate fabrication

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C

Metallisation	10 nm Al
Spin resist	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	"Head" : Dose 430 μC/cm^2 , resolution 1.25 nm, VRU 10, Spot 8nA
	"Foot" : Dose 940 μC/cm^2 , resolution 1.25 nm, VRU 4, Spot 4nA
Develop	IPA rinse → 45 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
	H_2O rinse → 100 s CD-26 @ room T → H_2O rinse 15 s
	IPA rinse → 40 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Recess etching	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 16 s 5.9 pH succinic acid @ 22.5 ^{o}C
Metallise	20 s 10:1 H_2O:NH_3OH de-ox → 30 s H_2O rinse
	→ Ti 15 nm/ Pt 15 nm/Au 400 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

5. Si_3N_4 passivation

Spin resist	15 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	15 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 600 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Si_3N_4 deposition	250 nm ICP-CVD deposition in room T
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

6. CPW pads

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

B VII. 3D EBL air bridge technology

Spin resist	4 x (15 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C)		
Exposure	resolution 1.25 nm		
	200 nm lines: Dose (μC/cm^2)	VRU	Spot (nA)
	50	30	32
	100	15	16
	150	13	16
	200	8	8
	240	8	7
	270	8	7
	300	8	7
	320	8	7
	340	8	7
	360	8	7
	380	8	7
	400	8	7
	420	8	7
	440	8	7
	460	8	7
	480	8	7
	500	8	7
	520	8	7
Develop	IPA rinse → 90 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s		
Metallise	Ti 20 nm/Au 500 nm		
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse		

B VIII. MMIC oscillator

1. Markers & Ohmic contacts for pHEMTs & Gunn diodes

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ Au 14 nm/Ge 14 nm/Au 14 nm/Ni 11 nm/Au 70 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

2. Mesa isolation for pHEMTs & Gunn diodes

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 2 hr oven @ 180^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	IPA rinse → 30 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 2 min 1:1:100 H_3PO_4:H_2O_2:H_2O → electrical test → additional etching if required

3. Test pads for Gunn diodes & bottom plate of capacitor

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 200 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

4. Protection of HEMTs & Gunn diode recess etching

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA

Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Wet etch	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ ~ 5 s 5.9 pH succinic acid @ 22.5 ^{o}C → electrical test → etching until reaching the target current of 60 mA for 120 μm wide devices

5. 70 nm T-gate fabrication

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Metallisation	10 nm Al
Spin resist	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	8 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	"Head" : Dose 430 μC/cm^2 , resolution 1.25 nm, VRU 10, Spot 8nA
	"Foot" : Dose 940 μC/cm^2 , resolution 1.25 nm, VRU 4, Spot 4nA
Develop	IPA rinse → 45 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
	H_2O rinse → 100 s CD-26 @ room T → H_2O rinse 15 s
	IPA rinse → 40 s 2.5:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Recess etching	30 s 4:1 H_2O:HCl de-ox → 30 s H_2O rinse
	→ 16 s 5.9 pH succinic acid @ 22.5 ^{o}C
Metallise	20 s 10:1 H_2O:NH_3OH de-ox → 30 s H_2O rinse
	→ Ti 15 nm/ Pt 15 nm/Au 400 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

6. Si_3N_4 passivation

Spin resist	15 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	15 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	4 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 600 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 1:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Si_3N_4 deposition	250 nm ICP-CVD deposition in room T
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

7. Si_3N_4 for MIM capacitors

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155°C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155°C
Exposure	Dose 400 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 1:1 IPA:MIBK @ 23 °C → IPA rinse 15 s
Si_3N_4 deposition	50 nm ICP-CVD deposition in room T
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

8. NiCr resistors

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155°C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155°C
Exposure	Dose 600 μC/cm^2 , resolution 1.25 nm, VRU 15, Spot 16nA
Develop	IPA rinse → 80 s 2:1 IPA:MIBK @ 23 °C → IPA rinse 15 s
Metallise	NiCr 33 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

9. CPW pads

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155°C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155°C
Exposure	Dose 350 μC/cm^2 , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 °C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse

10. Air bridges

Clean substrate	5 min acetone rinse → 5 min IPA rinse → 3 min DI water rinse
Spin polyimide	2 x (2545 polyimide @ 100 rpm 10 s → 500 rpm 10 s → 5 krpm 60 s → 90 s hotplate baking @ 138°C)
Spin resist	80 % UVIII @ 4 krpm 60 s → 90 s hotplate baking @ 138°C
Exposure	Dose 60 μC/cm^2 , resolution 1.25 nm, VRU 50, Spot 64nA
Develop	H_2O rinse → 5 s CD-26 @ room T → H_2O rinse 15 s

Spin resist	12 % 2010 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
	2.5 % 2041 PMMA @ 5 krpm 60 s → 90 s hotplate baking @ 155^{o}C
Exposure	Dose 400 μC/cm^{2} , resolution 1.25 nm, VRU 30, Spot 32nA
Develop	IPA rinse → 60 s 2:1 IPA:MIBK @ 23 ^{o}C → IPA rinse 15 s
Metallise	Ti 20 nm/Au 500 nm
Lift-off	Pre-warmed acetone 2 hr → pipette clean → IPA rinse → H_2O rinse
Dry etch	20 min, RIE O_2 : 20 sccm, 100 W, 20 mTorr

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