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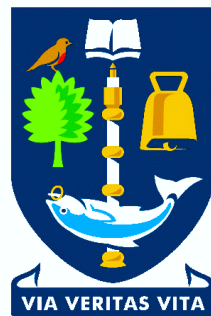
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# Nanofabrication of Silicon Nanowires and Nanoelectronic Transistors

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A Thesis Submitted in Fulfilment of the Requirements for the  
Degree of Doctor of Philosophy (Ph.D.)  
In Division of Electronics & Nanoscale Engineering



University of Glasgow

## Abstract

This project developed a robust and reliable process to pattern  $< 5$  nm features in negative tone Hydrogen silsesquioxane (HSQ) resist using high resolution electron beam lithography and developed a low damage reactive ion etch (RIE) process to fabricate silicon nanowires on degenerately doped n-type silicon-on-insulator (SOI) substrates. A process to thermally grow high quality silicon dioxide ( $\text{SiO}_2$ ) (between 5-15 nm) is also developed to passivate onto the etched silicon nanowire devices to serve the purposes of gate dielectric and a diffusion barrier to minimize the donor deactivation. The measured interface state trap density ( $D_{it}$ ) of the 10 nm thermally grown oxide is  $1.3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  with a breakdown voltage of  $\sim 7$  V.

Using optimized processes for lithography, dry etch and thermal oxidation, Hall bar and Greek cross devices are fabricated with mean widths from 45 to 4 nm on SOI substrates with a doping density  $\sim 2 \times 10^{19}$ ,  $4 \times 10^{19}$ ,  $8 \times 10^{19}$  and  $2 \times 10^{20}$  atoms/ $\text{cm}^3$  and electronically characterized at room and cryogenic temperatures (from 1.4 to 300 K) to allow resistivity, mobility and carrier density to be extracted directly as a function of temperature. This allowed to probe electron transport and scattering mechanisms in degenerately doped silicon nanowires. The mean free path is theoretically calculated and directly compared with the widths of the nanowires by which it can be approximated that the electron transport is 3 dimensional (3D) for the 12 nm wide nanowire which has likely to be changed to 2D and 1D for the 7 nm and 4 nm wide nanowires respectively. Moreover the experimental mobility is directly compared with a number of theoretically calculated mobilities using Matthiessen's rule, where it has been determined that the neutral impurity scattering is the dominant scattering mechanism limiting the performance of silicon nanowires.

Using silicon nanowires, junctionless transistors are fabricated on SOI substrate with a doping density  $\sim 4 \times 10^{19}$  atoms/ $\text{cm}^3$  and electronically characterized at room and cryogenic temperatures (from 1.4 to 300 K). It was observed that reducing the width of channel from 24 to 8 nm, the transistor changed their operation from depletion to enhancement mode due to increase in the surface depletion at smaller length scales. Since the drain current in a junctionless transistor is proportional to the doping density, a high on-state drive current  $\sim 1.28 \text{ mA}/\mu\text{m}$

has been observed with sub-threshold slope (SS)  $\sim 66$  mV/decade at 300 K. Moreover temperature dependent measurements revealed a low SS  $\sim 39$  mV/decade at 70 K and single electron oscillations at 1.4 K.

Finally, independent arrays of 2 terminal nanowires devices with mean widths from 45 to 4 nm are fabricated on SOI substrate with a doping density  $\sim 8 \times 10^{19}$  atoms/cm<sup>3</sup> to detect polyoxometalate (POM) molecules  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$ . A change in resistivity has been observed  $\sim 3.6$  m ohm-cm (corresponds to  $\sim 13$  % increase) when POM molecules are coated around the nanowires, shown n-type behaviour of molecules. POM molecules exhibit highly redox properties, therefore side-gated FETs with mean width  $\sim 4$  nm were fabricated on SOI substrate with a doping density  $\sim 4 \times 10^{19}$  atoms/cm<sup>3</sup> where side-gate was used to apply alternative  $\pm$  pulses of 20 V to charge and discharge the POM molecules to demonstrate flash memory operation. The average change in the threshold voltage was  $\sim 1.2$  V between the charging (program) and the discharging (erase) cycles. The program/erase time is currently limited to 100 ms for a reasonable single-to-noise ratio. Moreover no significant decay in the stored charge has yet been measured over a period of 2 weeks (336 hours).



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## Symbols

$A^{**}$	Richardson constant
$B$	Magnetic field
$C$	Capacitance
$c_L$	Averaged longitudinal elastic modulus
$D$	Diffusion constant
$D_0$	Initial dose
$D_1$	Dose at which resist is fully exposed
$E$	Energy
$E_D$	Donor activation energy
$E_F$	Fermi energy
$E_H$	Hall electric field
$F$	Electric field
$F_e$	Lorentz force on holes
$F_y$	Lorentz force on electrons
$g_D$	Donor's degeneracy
$g_s$	Spin degeneracy
$g_v$	Valley degeneracy
$h$	Plank's constant
$\hbar$	$h / 2\pi$
$I$	Current
$I_x$	Longitudinal current
$I_y$	Transverse current
$k_B$	Boltzman constant
$k_F$	Fermi wavenumber
$L$	Length of the channel
$L_D$	Debye length
$L_G$	Gate length

$l$	Mean free path
$l_B$	Magnetic length
$l_e$	Elastic scattering length
$l_F$	Electric length
$l_{in}$	Inelastic scattering length
$l_t$	Thermal length
$l_\varphi$	Phase coherence length
$m^*$	Effective electron mass
$m_0$	Free electron mass
$m_l$	Longitudinal electron mass
$m_t$	Transverse electron mass
$m_c^*$	Conductivity effective mass
$m_{de}^*$	Density of states effective mass
$N_D$	Doping density
$N_S$	Sheet density
$n$	Carrier density
$V_H$	Hall voltage
$Q_S$	Sheet charge
$q$	Electron charge
$R_H$	Halls coefficient
$T$	Temperature
$T_{ox}$	Thickness of oxide
$T_{Con}$	Thickness of control oxide
$T_{Tun}$	Thickness of tunnelling oxide
$t$	Thickness of the channel
$V_F$	Forward bias voltage
$V_{Fb}$	Flatband voltage
$V_H$	Hall voltage
$V_T$	Thermal voltage
$V_{Th}$	Threshold voltage

$V_x$	Drift velocity
$v_F$	Fermi velocity
$w$	Width of the channel
$\Delta V_{Th}$	Change in threshold voltage
$\phi_{Bn}$	Schottky barrier height
$\Gamma$	Scattering rate
$\sigma$	Conductivity
$\mu$	Mobility
$\mu_{ac}$	Mobility due to acoustic phonon scattering
$\mu_I$	Mobility due to ionized impurity scattering
$\mu_{IRS}$	Mobility due to interface roughness scattering
$\mu_{NI}$	Mobility due to neutral impurity scattering
$\mu_{op}$	Mobility due to optical phonon scattering
$\tau$	Elastic scattering time
$\tau_\varphi$	Inelastic scattering time
$\lambda_F$	Fermi wavelength
$\epsilon_0$	Permittivity of a vacuum
$\epsilon_{oxide}$	Permittivity of gate oxide
$\epsilon_r$	Relative permittivity of a material
$\Xi_{ac}$	Acoustic deformation potential

# I. Introduction

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Over the last few decades, advancements in silicon nanowire technology have shown promising potential in future-generation electronics, opto-electronics and chemical/biological sensing applications. Silicon nanowires have been used to demonstrate nanoelectronic transistors [1], memories [2], quantum information processing [3], sensors [4], thermoelectric energy harvesting [5], solar cells [6] and electrometers [7]. Silicon is an ideal material for these applications as it is considerably cheaper compared with other materials and many semiconductor foundries use it for mass manufacturing of devices.

In particular, scaling the dimensions of the silicon metal-oxide-semiconductor field-effect-transistors (MOSFETs) has remarkably achieved over 2.5 billion transistors in present day microprocessor chips with continued scaling evolution of silicon nanowire (fin) - based multi-gate transistors, which emerged as successors to ultra-scaled planar gate silicon MOSFETs due to intimidating short-channel effects (SCE) in nanometer regime, such as drain-induced barrier lowering (DIBL), channel length modulation and hot-carrier effects, which deteriorates the controllability of the gate over the channel and result in degradation of sub-threshold slope and increase in off-state current. However the multi-gate transistors such as FinFETs [8], double-gate FETs [9] and tri-gate FETs [10] has not only downsized the technology node to present day 14 nm, but also demonstrated better electrostatic control of the channel due to proximity of multiple gates, which has remarkably suppressed the short-channel effects (SCE) even at shorter gate lengths and delivered near ideal sub-threshold slopes with reduced threshold voltage roll-off [11]. The advancements and innovations such as process-induced strain in silicon channels enhances the mobility without additional process complexity [12], addition of high-k dielectric stacks which delivers desired threshold voltage by tuning the work-function and provides better electrostatic control over the channel while preserving low gate leakage and replacement of the poly silicon with metal gate to eliminate the poly-depletion effects [8] are some of improvements being made to the planar gate silicon MOSFETs along with the scaling to improve transistor characteristics.



Apart from the transistors, silicon nanowires are predominantly used for a range of biochemical sensors, where the dimensions required is below 10 nm to achieve higher sensitivity through large surface-to-volume ratio. The operation of a silicon nanowire is based on the electric field effect where the charge on surface of the nanowire modulates the free carrier concentration in the channel region which modulates the conductivity. Hence the silicon nanowire becomes a resistive sensor, ideal to sense gases such as NO<sub>2</sub> & NH<sub>3</sub> [13], hydrogen [14] and diagnose a wide range of diseases for the point-of-care healthcare applications including proteins [15], DNA [16], cancer biomarkers [4,17] and viruses [18]. Similarly quantum information processing also requires devices below 10 nm in order to reduce the capacitance of the channel region for potentially high temperature operation.

Over the years, many fabrication techniques have been developed to fabricate silicon nanowires, which are based on top-down and bottom-up approaches or hybrid top-down/bottom-up approaches. The nanowires fabricated with bottom-up approaches use catalyst-assisted growth mechanisms such as vapour-liquid-solid (VLS) mechanism, which involves three main stages for the nanowire growth, i.e. metal alloying, crystal nucleation and axial growth [19]. However VLS mechanism exhibits Gibbs-Thomson effect, which relates surface curvature to vapour pressure and chemical potential to describe the diameter-dependent growth rate of a highly curved particle [20]. The growth rate controlled by the growth conditions can be varied to obtain the desired length of nanowire. Generally the nanowires with smaller diameter grows slower than larger ones and the diameter of the nanowire is limited by the radius of the metallic particle. Bottom-up nanowires can be grown on any substrate with extremely small diameter down to ~1 nm with very high aspect ratio, however yield is too low to be economical for mass manufacturing in semiconductor foundries, because the nanowires are not directionally aligned when grown on a non-silicon substrates and subject to complex integration problems such as mechanically transfer nanowires to the substrate, position individual nanowires and add ohmic contacts.

On the contrary, top-down approach provides better lithographic control to fabricate nanowires and still results in industry yields of over 99 %, which is required to sell products in the market. It involves deposition of resist material on the substrate and exposure using various energy sources, which after resist development result in a mask for pattern transfer via dry or wet etch techniques. The energy sources used in top-down lithographic processes consists of

photons (visible to ultraviolet radiation and x-rays), particle beams (electrons and ions), physical contact printing (nano-imprint), edge based techniques (shadow evaporation). Other methods of lithography include the uses scanning probe microscopy (SPM) to modify and manipulate the deposited material on the surface at atomic scale but patterning a large area using a single tip would take an enormous time. The considerations for any lithographic technique are resolution (minimum achievable feature size), process stability, registration (layer-to-layer alignment), yield and throughput. Electron beam lithography uses a beam of electrons (with minimum spot size  $\sim 3$  nm) and exposes the pattern in resist either pixel-by-pixel or shape-by-shape, hence provides the minimum feature size of  $\sim 3$  nm with highest pattern fidelity in terms of shape, accuracy, precision of features and overlay, over all the existing top-down approaches. Whilst electron beam lithography is commercially only used for writing masks and templates because of very low throughput, however it is useful for limited large scale integration and R&D to develop the technological nodes ahead of mass production. For high volume manufacturing, throughput is the prime criterion for choosing any lithographic technique. Therefore over the years, multi-beam lithography tools has been developed, which can decrease the exposure time of electron beam lithography by several orders of magnitude. Mapper has developed such a multi-beam lithography tool [21] where 13,000 electron beams are generated by splitting up a single electron beam, originating from a single electron source. Each of the beam has its own optical column to avoid cross-over during the wafer exposure. The beams are switched on/off by 13,000 light signals (each for a beam directed by the pattern generator), which are streamed to the electron beams at 1-10 GHz. This technique result in a throughput of over 10 wafers (300 mm) per hour at a resolution of  $< 45$  nm half pitch.

Despite substantial progress towards multi-beam lithography tools, industry however still relies on various photolithographic techniques, which provides the highest throughput with lowest manufacturing cost. The resolution of photolithography is limited by the wavelength of the light and numerical aperture (NA). Typically feature sizes below 500 nm are extremely difficult to realize with 365 nm ultraviolet (UV) photolithographic techniques, because of the diffraction of light at the mask openings, however advance photolithographic techniques such as immersion lithography enhances resolution by 30–40 % by replacing the air gap between final lens and substrate with various fluids such as water, aluminium chloride, hydrogen phosphate and sodium sulphate [22], which increases the numerical aperture (NA) above 1.

Currently deep ultraviolet (DUV) lithography uses argon fluoride (ArF) 193 nm wavelength excimer lasers to deliver a throughput of  $\geq 130$  wafers (300 mm) per hour with a resolution of  $\leq 45$  nm [Nikon NSR-S610C]. Currently Intel is using 193 nm wavelength DUV lithography along with double patterning techniques for the production of Xeon, Core and Atom processors based on 14 nm technology node.

So far, both top-down and bottom-up approaches have produced high performance silicon nanowire transistors. Intel's 14 nm technology node which is currently in high-volume manufacturing, is based on 2<sup>nd</sup> generation 20 nm gate length bulk FinFETs with 8 nm wide and 42 nm tall rectangular fins. For NMOS, at 0.7 V supply voltage,  $I_{ON} = 1.04$  mA/ $\mu$ m has been reported which is more than 15% improvement on that reported for 1<sup>st</sup> generation 26 nm gate length bulk FinFETs (22 nm technology node). About  $\sim 6$  orders of  $I_{ON}/I_{OFF}$  has been observed with a sub-threshold slope of  $\sim 65$  mV/decade and DIBL of 50 mV/V [23]. The silicon nanowire transistors fabricated on SOI substrate using electron beam lithography are reported in [11]. Here the gate length is 1  $\mu$ m whereas the fin width and height is 30 and 10 nm respectively, whereas  $\sim 10$  nm SiO<sub>2</sub> is thermally grown and used as a gate dielectric. Measurements shown that at 1.0 V supply voltage,  $I_{ON} = 2$   $\mu$ A/ $\mu$ m has been observed with ratio between  $I_{ON}/I_{OFF} \sim 8$  orders and sub-threshold slope of  $\sim 64$  mV/decade. Silicon nanowire transistors with channel width down to 4 nm has been realized using atomic force microscopy (AFM) lithography [24]. Whilst the channel is oxidized with  $\sim 2.5$  nm SiO<sub>2</sub> but a back gate is used to modulate the channel. Here at 1.0 V supply voltage,  $I_{ON} = 0.5$   $\mu$ A/ $\mu$ m has been observed with a sub-threshold slope of over a V/decade. Silicon nanowire transistors fabricated using a bottom-up approach is reported in [25]. Here the grown nanowire has a diameter below 5 nm after thermal oxidization and a channel length range from 1.0 – 1.5  $\mu$ m. Results from 300 nm gate length devices shown that at 1.25 V supply voltage,  $I_{ON} = 0.2$  mA/ $\mu$ m has been observed with ratio between  $I_{ON}/I_{OFF} \sim 5$  orders and sub-threshold slope of  $\sim 120$  mV/decade.

There are quite a few demonstrations electronically characterizing 10 nm silicon nanowires to understand the transport mechanisms at smaller length-scales. Bottom-up approach has been used to fabricate silicon nanowires from 60 – 5 nm in diameter [26]. An increase in ionization energy with decreasing nanowire diameter has been observed due to lack of surface passivation, which may have profound implications for the design of scaled devices such as FETs for bio-sensing, where a change in dielectric properties could modify the

conductance of nanowires. A number of top-down approaches are employed to fabricate silicon nanowires for transport studies [27,28,29,30], the majority of which show either no or hopping conductivity for nanowires below 10 nm. The main reason for poor electrical characteristics in top-down nanowires is the need of developing etch processes for pattern transfer with minimized plasma-induced sidewall damage [31,32].

The term damage refers to any effect of the etch process which disrupts the lattice structure, creates dangling bonds on the etched interface, contaminate the etched surface with polymer passivation layer or heavy metals, which result in deep traps for charge carriers, and deteriorates the electrical characteristics of the nanowire. Such damage has become more critical with continued scaling evolution of CMOS technology with modified transistor designs, such as FinFETs where the active channel region is formed either through inversion or accumulation layer near the Si-SiO<sub>2</sub> interface on the multiple sidewalls of the etched Si. The plasma-induced sidewall damage introduces defect states and can potentially pin the Fermi level at the middle of the energy gap and trap electrons at the sidewall surfaces which can reduce the number of charge carriers in the channel region since the electrons on the sidewalls would not gain sufficient energy to reach the conduction band. These defects and trapped charges also becomes the scattering sites for the charge carriers which deteriorates the mobility of the channel region. Therefore the sidewall carrier depletion results in poor or no electrical conductivity if the channel width is comparable to the depletion width. The mechanisms result in sidewall damages often correlates with the etch process parameters such as bias voltage, this can't be independently controlled in an RIE system but typically low RF power result in smaller bias voltage, which reduces the ion bombardment energy and ion flux to the substrate, and hence helps to minimize the plasma induced sidewall damage. The work in this thesis is based on developing a low damage etch process for high quality pattern transfer to fabricate a number of different types of nanowire devices discussed in subsequent chapters.

### 1.1. Project Overview

For this project, 200 mm diameter (100) crystal orientated silicon-on-insulator (SOI) wafers purchased from SOITEC with a top silicon layer of 55 nm and buried oxide of 150 nm on 735  $\mu\text{m}$  thick silicon substrate. The cross-section of SOI substrate is shown in figure 1-1. Initially the top silicon layer was doped with boron ( $\sim 1.5 \times 10^{15}$  atoms/cm<sup>3</sup>) and later heavily

implanted with phosphorus to dope above metal-insulator transition. However the bottom silicon substrate was doped with boron ( $\sim 9 \times 10^{14}$  atoms/cm<sup>3</sup>). The quarters of SOI wafers were implanted from ion beam services (IBS) at France, detail of which is shown in table I-1.

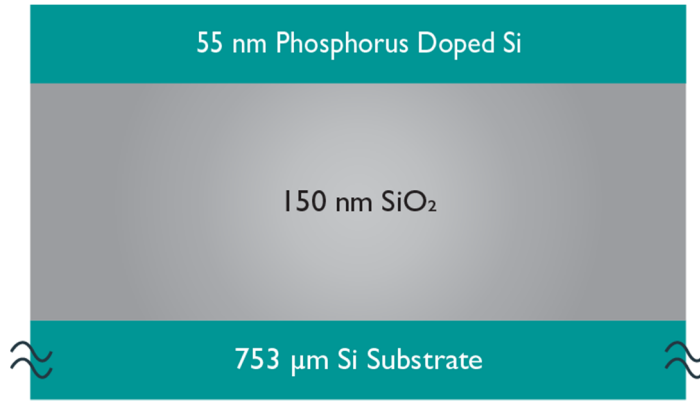


Figure I-1: Cross-sectional illustration of silicon-on-insulator (SOI) substrate.

After implantation, dopant is activated in rapid thermal annealing (RTA) furnace under nitrogen gas environment at 1000 °C for 75 seconds. Transmission line measurement (TLM) structures were made with nickel silicide contacts to optimize the dopant's activation time and temperature to make sure that the metal contacts made to SOI substrate are ohmic and the dopant is fully activated.

Implantation Dose (cm <sup>-2</sup> )	Implantation Energy (KeV)	Activated Doping Density (cm <sup>-3</sup> )
$2 \times 10^{13}$	10	$3 \times 10^{18}$
$5 \times 10^{13}$	10	$6 \times 10^{18}$
$2 \times 10^{14}$	10	$2 \times 10^{19}$
$4 \times 10^{14}$	15	$4 \times 10^{19}$
$1 \times 10^{15}$	15	$8 \times 10^{19}$
$5 \times 10^{15}$	15	$2 \times 10^{20}$

Table I-1: Implantation dose and energy used to implant quarters of 8 inch SOI wafers with phosphorus.

This project has been divided into three main parts. In first part, processes for nanolithography, reactive ion etch and thermal oxidation ( $\text{SiO}_2$ ) are developed and well optimized so that they can be repeatedly used to deliver consistent HSQ linewidths, silicon etch profile and thin oxide film for the fabrication of a number of different types of silicon nanowire devices. To begin with, a robust, reliable and reproducible process is developed to pattern  $< 5$  nm isolated lines on SOI substrate using hydrogen silsesquioxane (HSQ) resist by high resolution electron beam lithography tool. This process is optimized in terms of investigating the resist cleaning procedures, patterning strategies, resist prebake time/temperature and resist post-exposure development. By varying the exposure dose, resist developer dilution, developing time and developing temperature are the key parameters predominantly examined to determine the optimum conditions that can deliver consistent HSQ linewidths with very smooth line edge roughness, these results are discussed in chapter 2.

HSQ linewidths are fabricated typically from 100 – 5 nm to optimize silicon nanowire etch process using reactive ion etching (RIE). Initially tetrafluoromethane ( $\text{CF}_4$ ) based etch chemistries are explored to etch silicon but it was found that the selectivity (i.e. ratio of the resist: etch) can't be improved any further (3:1), Therefore sulphur hexafluoride ( $\text{SF}_6$ ) and octafluorocyclobutane ( $\text{C}_4\text{F}_8$ ) based etch chemistries are investigated and a low damage RIE process is optimized to transfer  $< 5$  nm features onto SOI substrate with a relatively good selectivity (1:2.5). These results are discussed in detail in chapter 3. Another process is optimized to thermally grow  $\sim (5\text{-}15\text{ nm})$  silicon dioxide ( $\text{SiO}_2$ ) in a dedicated high temperature oxidation furnace in order to passivate the silicon surface with oxygen to remove any dangling bonds and trap charges present at the silicon interface. The oxide quality has been determined from circular metal-oxide-semiconductor (MOS) capacitors fabricated on silicon substrate, which revealed a low  $D_{it} = 1.3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  (determined from 10 nm  $\text{SiO}_2$  using conductance method) after capacitors annealed in forming gas.

In second part, silicon nanowire devices are fabricated using optimized processes for lithography, dry etch and thermal oxidation. The device fabrication techniques are discussed in chapter 4. Hall bar and Greek cross devices are fabricated on SOI substrates with a doping density  $\sim 2 \times 10^{19}, 4 \times 10^{19}, 8 \times 10^{19}$  and  $2 \times 10^{20} \text{ cm}^{-3}$  with mean widths from 45 to 4 nm to determine the resistivity, mobility and carrier density as a function of temperature to identify major scattering mechanisms dominating the electron transport. By directly comparing the

theoretically calculated mean free path of an electron with the widths of the nanowires, it has been approximated that the electron transport is 3 dimensional (3D) for the 12 nm wide nanowire which has likely to be changed to 2D and 1D for the 7 nm and 4 nm wide nanowires respectively. Furthermore different scattering mechanisms are modelled to estimate the total mobility using Matthiessen's rule, which has been directly compared with experimental mobility to determine the dominant scattering mechanism limiting the performance of the nanowires. These results are discussed in chapter 5.

Using silicon nanowires, Junctionless transistors with widths from 24 to 8 nm are fabricated on SOI substrate with a doping density  $\sim 4 \times 10^{19}$  atoms/cm<sup>3</sup> and electronically characterized at room and cryogenic temperature. Such high doping density is normally required to maintain an electrostatic integrity in the channel especially with smaller length scales. The 24 and 16 nm wide transistors were found to be operating in depletion mode whereas for the 8 nm wide transistor, a transition has been observed where the transistor changed their operation from depletion to enhancement mode possibly due to an increase in the surface depletion. For an 8 nm wide transistor, a high on-state drive current  $\sim 1.28$  mA/ $\mu$ m has been observed with sub-threshold slope (SS)  $\sim 66$  mV/decade, attributed to the high doping density and potentially 1D transport, established from determining electron transport at 4 nm wide nanowires. The absence of junctions provides immunity to short channel effects, hence a low DIBL  $\sim 106$  mV/V has been observed. Moreover temperature dependent measurements were performed onto 8 nm wide transistor which revealed a low SS  $\sim 39$  mV/decade at 70 K and single electron oscillations at 1.4 K.

Finally, polyoxometalate based CMOS compatible non-volatile flash memory devices are fabricated. This work has been done in collaboration with several groups across the school of engineering who have been involved with synthesis, characterization, electrochemical analysis, electron paramagnetic resonance (EPR) studies, crystallography, density flow theory (DFT) calculations and industrial level device modelling of the polyoxometalate (POM) based clusters after which electronic devices are fabricated such as side-gated FETs to realize the flash memory operation as predicted. These FETs with mean width  $\sim 4$  nm were fabricated on SOI substrate with a doping density  $\sim 4 \times 10^{19}$  atoms/cm<sup>3</sup> by adding a side gate to the Hall bar geometry and tested before and after deposition of POM molecules around the channel. There are different versions of POM molecules but in this work selenium-based polyoxotungstates

are used. A shift in the sub-threshold slope of the transistor has been observed after the deposition of POM molecules indicated an n-type behaviour. Furthermore, side-gate is used to apply  $\pm$  pulses to charge (–) and discharge (+) the POM molecules, hence demonstrated the flash memory operation. These results are discussed in chapter 7.



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## 2. Electron Beam Lithography in HSQ Resist

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This chapter begins with an introduction to electron beam lithography (EBL) which is being extensively used throughout this project for patterning micro- and nano-scale features in positive tone polymethyl methacrylate (PMMA) and negative tone hydrogen silsesquioxane (HSQ) EBL resists. PMMA is primarily used for metal lift-off purposes whereas HSQ is the key resist used for pattern transfer in silicon via reactive ion etch (RIE) process. A robust and reliable process has been optimized to pattern 10 nm isolated lines in HSQ resist is discussed in detail which enabled to fabricate a diverse range of nano-scale devices discussed in next chapters.

### 2.1. Electron Beam Lithography

Vistec vector beam (VB) 6 ultra-high resolution (UHR) extra wide field (EWF) electron beam lithography tool is installed in James watt nanofabrication centre (JWNC). It is classified as a Gaussian-beam lithography tool where each shape is formed as a series of exposures with a focused electron beam. The schematic representation of Vistec VB6 is shown in figure 2-1, mainly comprises of an electron gun, column, chamber, stage and loadlock all of which are mounted over the vibration isolated 'plinth' where all the vacuum systems are installed. A beam of electrons is generated by an electron gun using a cathode emission process with a thermally assisted field emitter (TFE) source. In Vistec VB6, Schottky emitter is installed which is equipped with a heated zirconium oxide ( $ZrO_2$ ) coated tungsten (W) tip surrounded by the suppressor and extractor electrodes to control the electron emission process. The suppressor electrode prevents the electron emission from the cathode shank except from the tip region. The potential is applied between the tip and the extractor electrode which creates a large electric field allows the electrons to tunnel through the tip and form a beam of electrons also referred as spot size of orders of few nm in diameter. These electrons then passed through another electrode for focusing the beam and then accelerated towards the anode in the column where they are further accelerated at fixed 100 keV potential. The suppressor, extractor and focusing electrodes are characterized as electrostatic lens and forms lens I assembly of the electron gun by which the electrons trajectory can be controlled (focused and deflected) due to the Lorentz force produced by the electromagnetic field onto the beam of electrons.

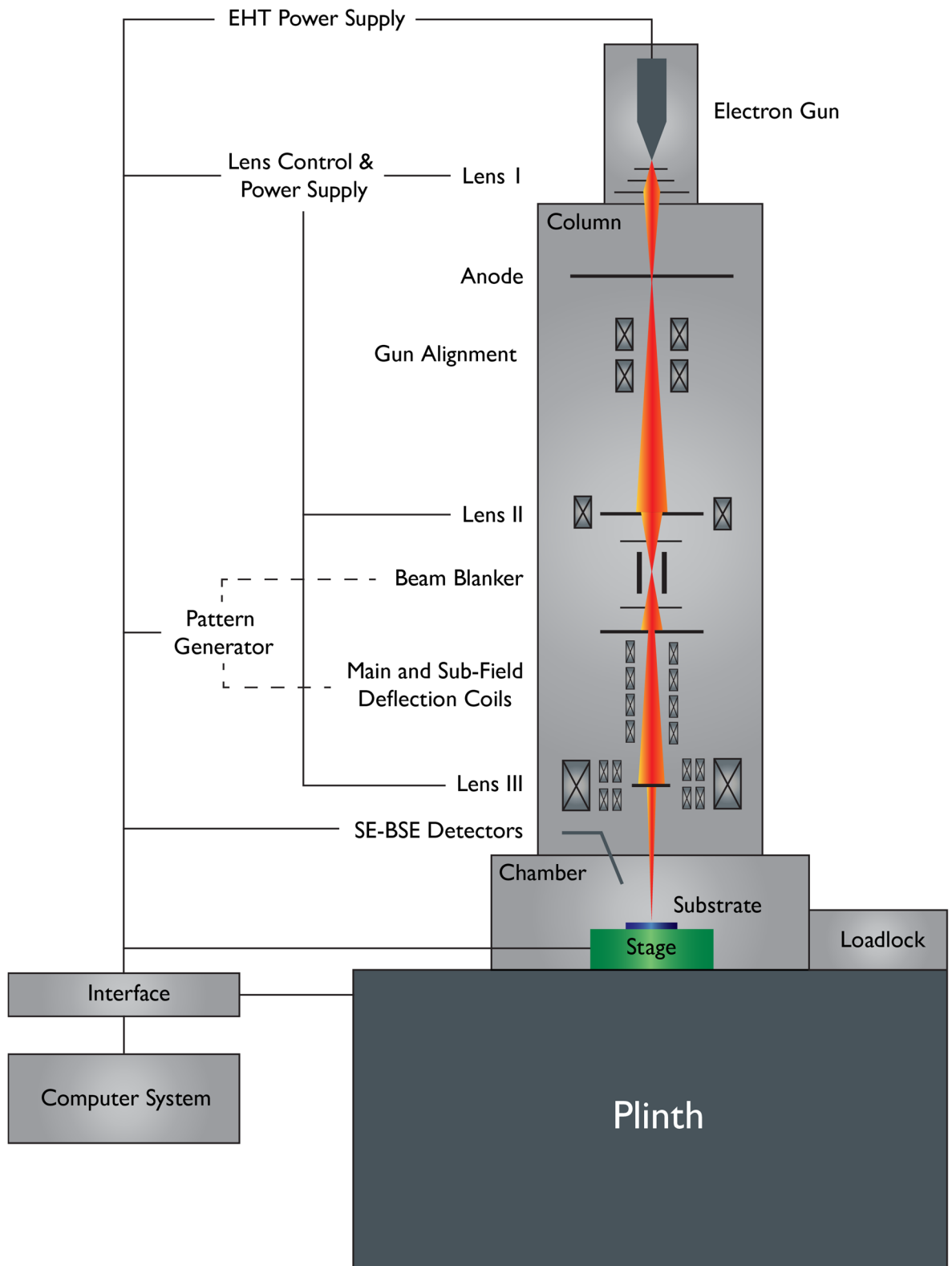


Figure 2-1: Schematic representation of the key components of Vistec VB6 electron beam lithography tool.

The column consists of gun aligner, magnetic lens II, electrostatic beam blanker, main & sub-field deflection coils and magnetic lens III, all through which the electron beam is kept aligned down to the substrate. The gun aligner consists of two pairs of magnetic deflection coils to shift and tilt the electron beam in the optical axis. There are 6 different sized apertures used at different places throughout the column so that any required beam diameter can be produced by varying the current density. A combination of lens I and lens II work as a zoom lens where the focus point of lens II is fixed such that the beam diameter can be varied onto substrate while holding the focus and current density constant [1]. This feature is useful for electrostatic beam blanker which is positioned in the middle of the focal point known as beam crossover created by the lens placed above beam blanker plates. While the beam blanker is in switched on state, the electron beam is not deflected and substrate is being exposed whereas in switched off state, the electron beam is electrostatically deflected from optical axis at a large angle onto a limiting aperture and substrate is not exposed.

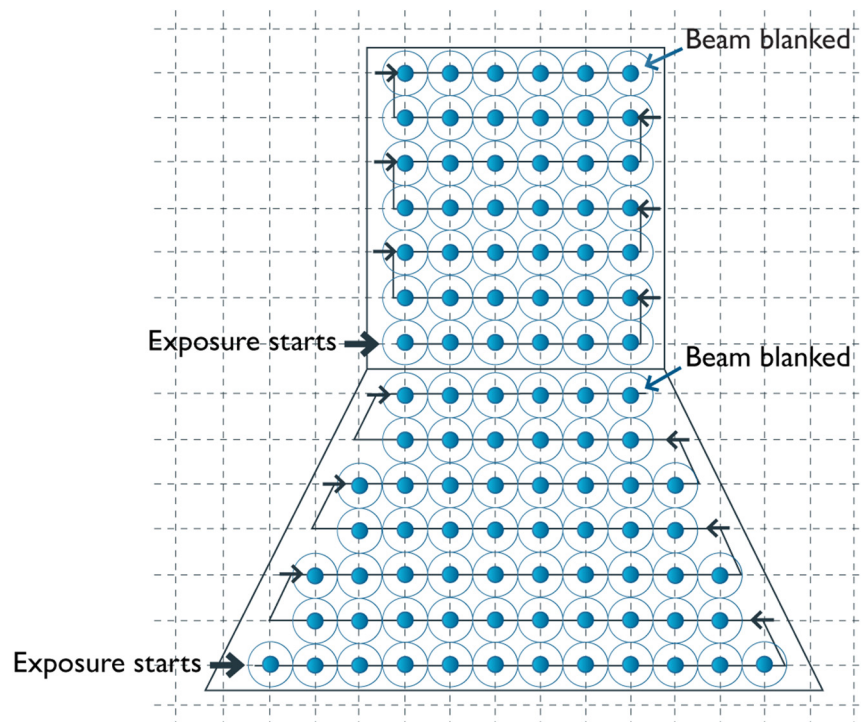


Figure 2-2: Vector scan of Vistec VB6.

Vistec VB6 uses vector scan exposure technique to write onto the substrate which employs the electrostatic beam blanker and main & sub-field deflection coils synchronized by the pattern generator. Unlike the beam blanker which is electrostatically deflecting the electron

beam, main & sub-field deflection coils creates electromagnetic field perpendicular to the optical axis to deflect the electron beam while not affecting its focus. This mechanism keeps the electron beam independent of the voltage applied to beam blanker plates until the beam is switched off, known as conjugate plane blanking. Pattern generator reads the digital pattern from the central computer and generates analogue signals to the beam blanker and main & sub-field deflection coils to rapidly switch on/off the beam and deflect the beam onto the substrate respectively. Lens III is the ultra-high resolution (UHR) final lens installed at the end of the column which accurately focus the final spot size generated onto the substrate for writing.

Figure 2-2 shows vector scan of Vistec VB6 exposure onto a designed pattern where the electron beam only scanned and exposed the designed pattern fractured into different shapes. The exposure start from the bottom left of the shape and once fully exposed through moving (deflecting) the beam onto the substrate by main & sub-field deflection coils, the beam is blanked and immediately moved to the bottom left of another shape to start the exposure. In conventional raster scan lithography tools the entire subfield is scanned back and forth and exposed accordingly, thus making vector scan tools not only more efficient in writing but also more expensive. Pattern generator equipped with a 20 bit digital to analogue converter (DACs) that defines the maximum deflection limit of the electron beam which is given by,

$$\text{Maximum field size} = \text{Resolution grid} \times 2^{20}$$

$$\text{Maximum field size} = 1.25 \text{ nm} \times 1048576 = 1310.72 \text{ } \mu\text{m}$$

Where resolution grid is the minimum deflection limit of the electron beam that defines that accuracy of the Vistec VB6 tool to place and expose a pattern. Thus there are 1048576 points which can be addressed in x and y direction on 1.25 nm resolution grid in a maximum field size of 1310.72  $\mu\text{m}$  without stage being moved. There are two other resolution grids that can be used with Vistec VB6 are 0.5 and 1.0 nm which gives a maximum field size of 524.288 and 1048.576  $\mu\text{m}$  respectively. Often the desired pattern is larger than the maximum field size for which the stage can be moved with linear motors in x and y direction but it could potentially result in possible drift or misalignment of few microns comes with each stage movement. A beam error feedback (BEF) correction unit employs  $\lambda/1024$  interferometer to measure the actual stage position with a resolution of 0.62 nm. The difference between the desired and the

actual stage position is reimbursed by an offset to the beam by deflecting it to its correct position and eradicate the misalignment caused by stage movement.

The substrates from 5 mm up to 6 inch can be mounted onto different sized holders and are loaded onto the stage with kinematic mounts to allow the substrates to be repeatedly loaded at the same position onto the stage. The separation between the principle plane of the lens III and the substrate is approximately  $\sim 35.4$  mm and retaining this distance for each substrate is very critical since the substrates comes with different thicknesses and also spun with diverse range of resists with different thicknesses. A height meter is used to confront this issue where the infrared laser is spotted onto each substrate and further detected by a charge coupled device (CCD) array sensor to accurately measure the separation between the principle plane of lens III and the substrate, so that any correction can be applied to the electron optics to finely focus the electron beam onto the substrate. The Vistec VB6 is also equipped with secondary electron (SE) and backscattered electron (BSE) detectors in the column to turn the tool into scanning electron microscopy (SEM), used to scan over the substrates to find markers for layer-to-layer alignment.

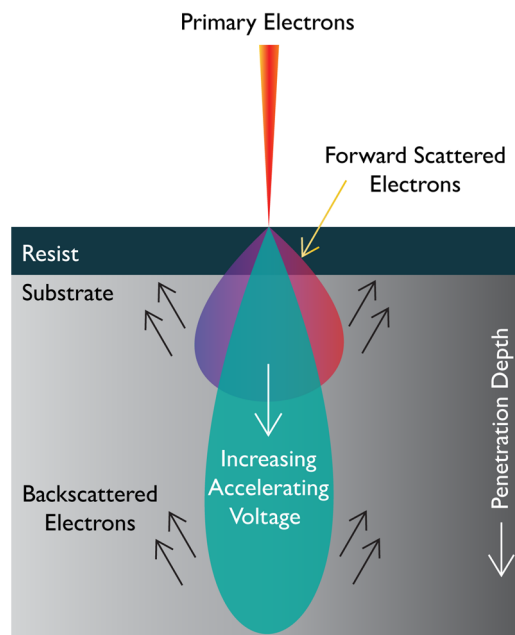


Figure 2-3: Interaction volume of electron beam exposure.

In principle the resolution of the electron beam exposure should be limited by the wavelength of an electron, for example for 100 KeV accelerating voltage the wavelength is



0.003 nm but fact of the matter is that such high resolution is actually limited by the scattering mechanisms and proximity effects. The electrons generated by the electron gun are normally referred as “primary electrons” which penetrates in the resist and do exposure. An exposure is a combination of several scattering take place due to the electron-solid interactions and mainly dominated by the forward scattering and backscattering of electrons. The interaction volume of such exposure is shown in figure 2-3, at 100 keV accelerating voltage the electrons can penetrate a few orders of 10  $\mu\text{m}$  deep into silicon substrate. The energy of an electron influences the scattering angle. In forward scattering, the primary electrons collides with the orbital electron of an atom from resist and substrate to either excite or ionize the atom and result in an inelastic scattering event, the lower energy electrons scatter to a larger angle whereas higher energy electrons scatter to a smaller angle. Thus, the penetration depth of an exposure depends on the accelerating voltage, larger the accelerating voltage, larger is the penetration depth and lower forward scattering. The primary electrons are the source of secondary electrons generated through the ionization process are mainly responsible for most part of the exposure throughout the resist. However the backscattering electrons are due to the collision of an electron with the nucleus of an atom from substrate result in an elastic scattering event, whilst with increasing accelerating voltage there will be less backscattering events but with a larger angle that could potentially bring in proximity effects.

Proximity effects deteriorates the performance limitations of the electron beam lithography tool. It is an undesired exposure in addition to the designed pattern often causes broadening of the resist, initially the forward scattering broaden the spot size into the resist and later due to the backscattering elections which return back to the surface cause further exposures. Normally the resist thickness is only a few percent of the total electron penetration depth. Therefore, the forward scattering can be controlled by using a higher accelerating voltage to narrower the beam penetration into the resist. Whereas backscattering can be controlled by approximating the backscattered electron intensity distribution which is often the sum of two Gaussian functions (one for forward scattering and other for backscattering) by simulating the designed pattern using Monte Carlo simulations with respect to the resist thickness and substrate to determine the optimum dose for the different shapes within a pattern, This allows to generate a point spread function (PSF) that modulates the dose and do the proximity correction accordingly.

Some of the common spot sizes corresponds to the beam current available in Vistec VB6 are shown in table 2-1. The beam current is measured using Faraday's cup where the electron beam is directed into a large conductive bucket through a very small aperture so that the majority of the incident and scattered electrons are captured within the bucket and their current flow is measured accurately by an ammeter. However to measure the spot size for a given beam current, the most accurate method in practice is known as a knife-edge measurement [2]. Here a transmission detector is positioned under the beam (on the stage) with a sharp edges or wire positioned above the detector. The electron beam is scanned over the edge and a plot of intensity against beam position over the edge gives a direct measure of the beam width. This method is a complicated process to do routinely, so it is generally done once across a range of beam currents and controlling the beam current allows a simple method to keep the beam size consistent.

Beam current	Spot size
1 nA	~3 - 4 nm
2 nA	6 nm
4 nA	9 nm
8 nA	12 nm
16 nA	19 nm
32 nA	24 nm
64 nA	33 nm
100 nA	45 nm

**Table 2-1: Spot size corresponds to the beam current.**

The number of electrons required to do an exposure is expressed in terms of 'area dose' if the spot size is larger than the pattern, and 'line dose' if the spot size equals the width of the pattern. Area dose is a function of beam current which corresponds to a spot size and the frequency of the exposure shots between two points defined by beam step size (BSS) on a exposure grid is given by,

$$\text{Area dose} = \frac{\text{Beam current (I)}}{\text{Frequency (f)} \times (\text{BSS})^2} \text{ (}\mu\text{C/cm}^2\text{)}$$

$$\text{BSS} = \text{Variable resolution unit (VRU)} \times \text{Resolution grid (1.25 nm)}$$

The area dose is limited by the frequency of the pattern generator which is fixed, so either beam current has to be adjusted or the BSS in order to optimize the area dose. Some of the basic rules to select appropriate BSS are,

$$\text{BSS} \approx \frac{\text{Minimum feature size}}{5}$$

$$\text{Spot Size} > 2 \times \text{BSS}$$

VRU can be any integer from 1 to 512. Since the resolution grid is very small, BSS offers a secondary grid used during the exposure and it should always be integer multiple of resolution grid. The spot size should be at least twice or more than BSS, so that all the pattern get full exposure. The width and height of the every shape of the designed pattern should be in round numbers and also the multiple of BSS as shown in figure 2-2, else Vistec VB6 will round the shapes into the multiple of BSS and resulting exposure may slightly shorter than expected which may introduce small gaps between different shapes. 10 nm designed linewidths with exposure shots shown in figure 2-4, where the BSS is 2.5, 5 and 10 nm as a result of VRU 2, 4 and 8 respectively and a spot size of ~3 - 4 nm. Whilst 10 nm lithography can be achieved with different BSS as illustrated but the line edge roughness can be significantly improved by using a smaller BSS.

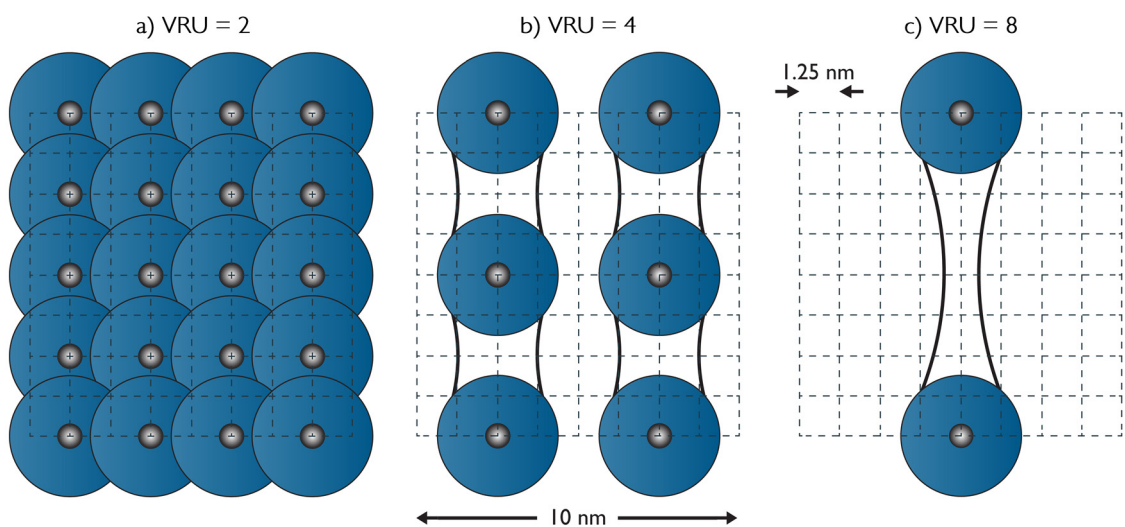


Figure 2-4: 10 nm linewidth exposure with different VRU's.

The patterns with multiple layers are designed in Tanner EDA L-Edit software on 1.25 nm resolution grid, they are exported as GDSII format. Layout beamer is the fracturing software which converts the designed patterns into trapezium shapes and defines the field & sub-fields for the electron beam exposure compatible with Vistec VB6. The GDSII file is imported in layout beamer where initially all the designed layers are extracted together to keep the overall field size identical for all the different layers, after that each individual layer is extracted and healed to remove any overlaps and join adjacent polygons, overlaps may result in double exposure. After healing, proximity effect correction (PEC) is applied onto the layer if needed, whilst layout beamer offers verity of PEC's but for this work conventional PEC method is used. The value of isodose grid should be multiple of BSS and should not be less than the spot size. For example for 10 nm linewidths, isodose grid value been set to 5 nm and a short range correction is being applied. The layer is then fractured and exported as VEP format. All the subsequent layers are fractured and exported in the similar way. The VEP files are then imported onto the Belle which is a java based tool to draw a schematic of substrate and then apply the dose, spot size and VRU to the each layer for the exposure in a sequential order along with the cross & marker positions and search parameters for the layer-to-layer alignment if required. A 'layout file' is then exported to the EBL server which is loaded by the Vistec VB6 software to run the job. The hierarchical flow of all this job submission process is shown in figure 2-5.

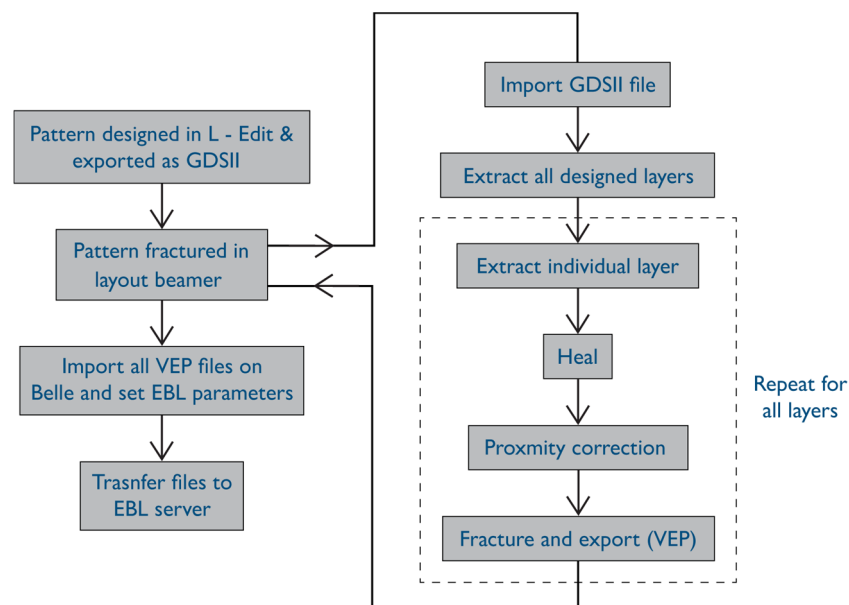


Figure 2-5: Flow of electron beam lithography job submission process.

The total writing time for any pattern using electron beam lithography tool is predominantly made up of four major things i.e. dwell time, calibration time, stage time and shape time. Dwell time is the time that the beam incident on the substrate and start exposing the resist. It is dependent on the area of the pattern to be written, the dose required and the beam current. Calibration time is the fixed time required at the start of the job to setup the height map and run a full calibration to select the resolution setting and to restore a given beam current. It is roughly 10 minutes at the start of a job. Stage time is the total time required for moving the stage around so the whole pattern gets exposed. There is some movement time and an associated dwell time after every move. A typical move time will be of order of 250 ms but depends on the distance the stage is being moved and the dwell time, which is typically 10 ms, but again is dependent on the length of the preceding move. Shape time is the time associated with processing a shape element within the data. Settling time required when deflecting the beam to the start of a new shape, it is generally between 2-10  $\mu$ s depending on the distance of the deflection from the previous shape. There are a few more short delays such as sub-field settling delays (normally  $\sim$  1 ms), which is the dwell time after moving the beam to a new sub-field before writing commences. The time to transfer the pattern across the network from the control computer to the pattern generator, shape synchronisation time, layer to layer alignment time are other overheads which accounts in overall writing time.

The dwell time for one 10 nm wide (1  $\mu$ m long) nanowire is  $\sim$  0.156  $\mu$ s when exposed with a dose of 2500  $\mu$ C/cm<sup>2</sup>, beam current of 1 nA and BSS of 2.5 nm. However the overall writing time to complete the exposure is 10.02 minutes, which is mainly dominated by the calibration time. With similar parameters writing 1000 nanowires would take 21.36 minutes in total where the calibration time is 10.02 minutes and stage time of 11.34 minutes.

## 2.2. Electron Beam Lithography Resists

The resists used for electron beam lithography are classified as either positive tone or negative tone resist. Resists are polymers which dissolves in various solvents (developer). An electron beam exposure substantially modifies a resist. For a positive tone resist, the exposed area becomes soluble in the developer as a result of bond scission process of breaking the long polymer chains into small fragments during an electron beam exposure. On the contrary for a negative tone resist, the exposed area becomes insoluble in the developer as a result of cross-

linking process of joining polymer chains which generates a cross-linked 3D network after an electron beam exposure. Hence positive and negative resist profile can be obtained.

A brief comparison of high resolution electron beam lithography resists is shown in table 2-2. These resists are trade-off between sensitivity, contrast and resolution but these parameters ultimately depends on pattern density, accelerating energy, resist pre bake temperature, developer and developing conditions. In high resolution electron beam lithography, resist with a lower sensitivity is preferred for better reproducibility and throughput. In context of this work, both positive and negative resists were required for metal lift-off and dry etch mask purposes respectively. PMMA (see section 2.3) and ZEP-520 are both positive resists which can be used to develop process for metal lift-off. ZEP-520 consists of a copolymer of -chloromethyl acrylate and methyl styrene in anisole (solvent). It can be developed with amyl-acetate and xylene but xylene is preferred. Whilst ZEP-520 provides higher contrast and over 3 times dry etch resistance over PMMA, but requires low acceleration voltages  $\sim 10$  KeV to deliver re-entrant profiles suitable for metal lift-off purposes. Moreover it often requires hexamethyl-di-silazane (HDMS) primer layer to achieve good adhesion between the resist and the substrate which is not required with PMMA. Since the electron beam lithography tool at Glasgow operates at fixed 100 KeV, therefore PMMA was used to develop process for metal lift-off. Whereas for dry etch mask purposes, NEB-31 and HSQ are most commonly used negative tone resists for high resolution electron beam lithography. NEB-31 is a chemically amplified resist and has higher dry etch resistance, comparable to most of the photo resists but in terms of resolution and contrast, HSQ (see section 2.4) was preferred which also has smaller linewidth fluctuations for features below 10 nm. Both NEB-31 and HSQ are generally developed with TMAH based developer.

Resist	Tone	Sensitivity	Contrast	Etch Resistance	Developer	Resolution
PMMA	Positive	High	Low	Poor	MIBK : IPA	$\sim 4$ nm [3]
ZEP- 520	Positive	High	High	High	Xylenes	$\sim 12$ nm [4]
NEB - 31	Negative	Low	High	High	TMAH	$\sim 25$ nm [5]
HSQ	Negative	Low	High	High	TMAH	$\sim 2.5$ nm [6]

Table 2-2: Comparison of high resolution electron beam lithography resists.

### 2.3. Polymethyl Methacrylate (PMMA) Resist

Polymethyl methacrylate (PMMA) is one of the most widely used positive tone electron beam lithography resist which is still prevailing since reported over 4 decades ago [7]. Whilst it has low contrast and poor dry etch resistance but provides extremely high resolution features close to the fundamental limits of lithography and also has a wider process latitude. PMMA comes with different molecular weights. In this work, PMMA 2010 (lower molecular weight) and 2041 (higher molecular weight) are used, which are diluted from 15% to 2.5% with anisole to achieve various resist thicknesses. The average molecular weight of PMMA 2010 and PMMA 2041 is 150,000 MW and 500,000 MW which allows maximum resist thickness of 2  $\mu\text{m}$  and 1  $\mu\text{m}$  respectively. After electron beam exposure, PMMA is developed in a solution of methyl isobutyl ketone (MIBK) diluted with isopropyl alcohol (IPA) to clear the exposed areas. Diluted developers tends to give high resolution but with low contrast and selectivity, also the cold development is reported to enhance the resolution [3] and improve feature quality.

In this work, PMMA is used to selectively deposit metal bond pads to the devices by developing a simple metal lift-off process, by spinning a lower molecular weight PMMA layer underneath a heavier molecular weight PMMA layer. After electron beam exposure, the exposed lower molecular weight PMMA develops much quicker than heavier since it requires low dose for dissolution, which allows a large undercut after development, hence aids the lift-off process illustrated in figure 2-6. The minimum feature lifted off is  $\sim 1\ \mu\text{m}$  (wide) that connects the etched semiconductor to a 200  $\mu\text{m}$  bond pad to allow electronic characterization. Prior to resist spinning, substrates cleaned ultrasonically in successive baths of acetone/ isopropyl alcohol/ de-ionized (DI) water and dehydrated bake on vacuum hotplate for 2 minutes at 140  $^{\circ}\text{C}$  to remove any residues. A bi-layer of 15% 2010 PMMA and 4% 2041 PMMA spun onto the substrate at 5000 rpm, which roughly gave a resist thickness of 1.2  $\mu\text{m}$  and 0.125  $\mu\text{m}$  respectively and then baked on vacuum hotplate for 2 minutes at 140  $^{\circ}\text{C}$  each. The substrates were then exposed with a dose of 450  $\mu\text{C}/\text{cm}^2$ , BSS of 25 nm and spot size  $\sim 45$  nm. After exposure, the substrate developed in a solution of 1:3 (MIBK:IPA) for 60 seconds and rinsed in IPA for 10 seconds before blown dry with nitrogen ( $\text{N}_2$ ). Substrate is then ashed in oxygen ( $\text{O}_2$ ) plasma at 10 SCCM, 50 mTorr and 10 W for 30 seconds in a reactive ion etch (RIE) tool to remove any remaining resist residues and immersed in a diluted 30:1 HF for 45 seconds as a final step to de-oxidize the semiconductor surface before metallization. The metal

is then evaporated  $\sim 400$  nm by using Plassys electron beam evaporator tool and after which the substrate is left in acetone which is kept in a hot water bath at  $50^\circ\text{C}$  for approximately two hours to lift-off the undesired metal leaving behind the bond pads. In ideal case the metal should not be evaporated more than  $1/3^{\text{rd}}$  of the thickness of bottom layer of PMMA to allow smoother lift-off without using ultrasonic agitation.

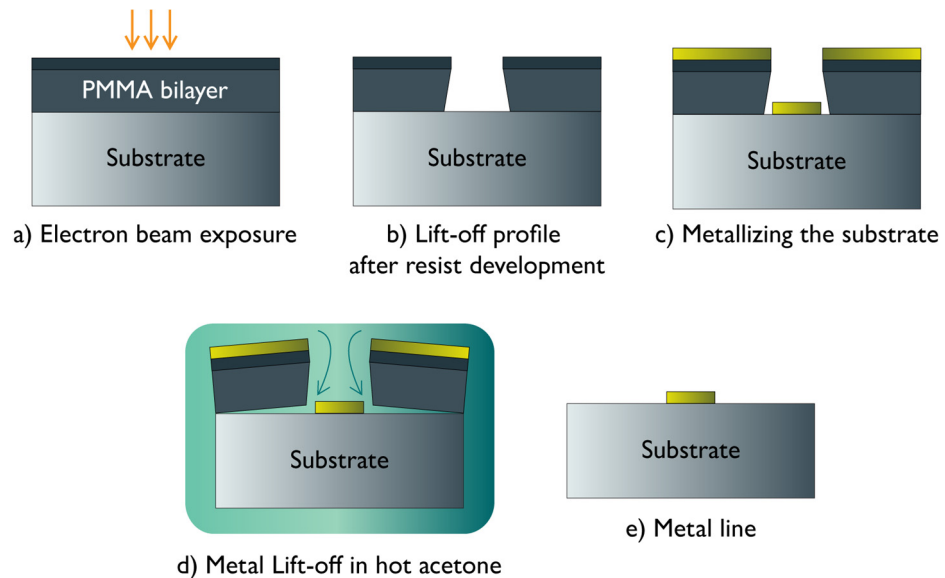


Figure 2-6: Lift-off steps using PMMA resist.

## 2.4. Hydrogen Silsesquioxane (HSQ) Resist

HSQ is most predominantly explored negative tone inorganic resist and has a capability to get a resolution down to  $2.5$  nm [5]. It was originally used in semiconductor industry as interconnect insulating layer for gap filling and planarization and has low dielectric constant which helps to minimize the capacitance. Namatsu et al. [8] being first to use HSQ as resist for electron beam lithography and demonstrated the linewidths with line edge roughness (LER) below  $2$  nm. HSQ is a cage like structure shown in figure 2-7, where each silicon atom is bonded to 3 oxygen and 1 hydrogen atom. During an electron beam exposure the caged structure turned into a linear networked structure through cross-linking process, initially Si-H bonds which are weaker than Si-O bonds broke up as a result of exposure and turned into the silanols (Si-OH) due to presence of absorbed moisture in the HSQ resist, these silanols are unstable and condensed to form a linear network of Si-O-Si bonds which is similar to silica insoluble in developer [7-9]. After exposure when developed with a hydroxide ( $\text{OH}^-$ ) based developer,



$\text{OH}^-$  reacts with unexposed HSQ molecules to form significant number of ionized silanols ( $\text{Si-O}^-$ ) to make the molecules soluble in developer [10].

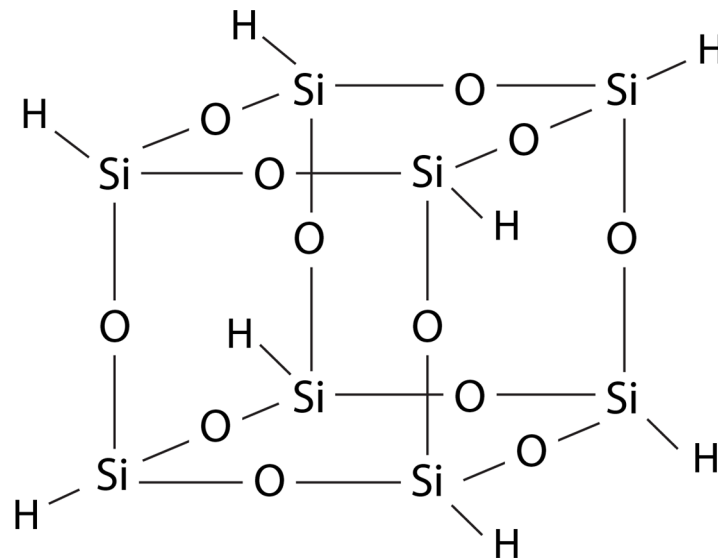


Figure 2-7: Caged structure of HSQ molecule.

There are a number of hydroxide based solutions can be used to develop HSQ patterns, Tetramethylammonium hydroxide (TMAH) [11] is the most widely used developer, a competitive contrast and sensitivity can be achieved by simply increasing the developer strength and temperature, but recently potassium hydroxide (KOH) [12], sodium hydroxide (NaOH) and lithium hydroxide (LiOH) based salty [potassium chloride/ sodium chloride (KCL/ NaCl)] developers [13] are also being used to develop HSQ patterns results in better contrast compared to conventional TMAH developer [14]. This is due to the fact that the neat hydroxide developers covers the HSQ pattern with an insoluble layer which stops the further development and limits the contrast [15] whereas by adding salt to the hydroxide further allows to etch the insoluble scum and helps to improve the contrast and also reduce the linewidth. Generally with a thicker HSQ resist, 10 nm lines mostly collapse during development stage due to increase in the surface tension while agitating the sample, whilst supercritical resist drying allows fabrication of very high aspect ratio 18 nm HSQ lines in 770 nm thick resist [16] but most of the 10 nm lithography in HSQ has been demonstrated using a thin resist layer ~ 30 nm. Therefore, this work specifically investigates and optimizes processes to pattern 10 nm HSQ lines in thicker resist, adequate for pattern transfer.

### 2.4.1. Experiment

All the experiments were performed on 100 mm diameter silicon (100) wafers ( $\sim 525$   $\mu\text{m}$  thick) cleaved into  $10 \times 10$  mm substrates. These wafers has 100  $\Omega\text{-cm}$  resistivity purchased from university wafers. Initially each substrate was cleaned with successive solutions of acetone, isopropyl alcohol (IPA) and de-ionized (DI) water for 5 minutes each in ultrasonic bath. The substrate then blown dry with  $\text{N}_2$  and baked on vacuum hotplate for at 140  $^\circ\text{C}$  for at least 10 minutes. It was observed that cleaning the substrate with DI water followed by a dehydration bake not only removes the remaining residues of acetone and IPA but also promotes strong adhesion between HSQ and silicon due to the formation of native oxide. It has been tested and verified that without DI water cleaning and dehydration baking, the thicker HSQ lines always collapsed. The HSQ used in this work supplied from Dow Corning FOX 16 which was further diluted with MIBK at a volume of 1:1, 1:2 and 1:3 and spin coated at 2000, 2000 and 5000 rpm resulting a desired thickness of 250, 150 and 50 nm HSQ resist. The resist was then pre-baked on vacuum hotplate at 90  $^\circ\text{C}$  for 2 minutes before loaded onto the Vistec VB6 by the trained operators.

On average the time between resist spinning and exposure is  $\sim 6$  -20 hours. The sensitivity of HSQ resist increases with the development delay [5], so most of the substrates are developed within 24 hours. The linewidths from 100 – 10 nm are designed with a period of 1  $\mu\text{m}$  to prevent any proximity effects using Tanner L-Edit software on a resolution grid of 1.25 nm and fractured using layout beamer software without any proximity correction. The lines were written with a dose ranging from 500 – 5000  $\mu\text{C}/\text{cm}^2$ , using a  $\sim 3$  nm spot size with a beam step size of 2.5, 5 and 10 nm at 100 keV accelerating energy. After exposure the substrates developed in 25% TMAH developer further diluted with DI water to make 12.5% to 1.19% TMAH dilutions and developed between 30 and 120 seconds, the temperature of the developer is also varied between 10  $^\circ\text{C}$  to 75  $^\circ\text{C}$  to fully understand the effect of changing developer concentration, time and temperature to optimize a reproducible process for 10 nm linewidths. All the substrates are examined using secondary electron detector without any sputter coating on FEI Nano Nova SEM 930 and Hitachi S-900 for top view and cross sectional view respectively. With these SEMs it has been investigated that the standard error between secondary electron and backscattered electron detector is  $\sim 1$  nm for 5 and 10 nm lithography [5]. The thickness of resist is measured on Veeco atomic force microscopy (AFM).

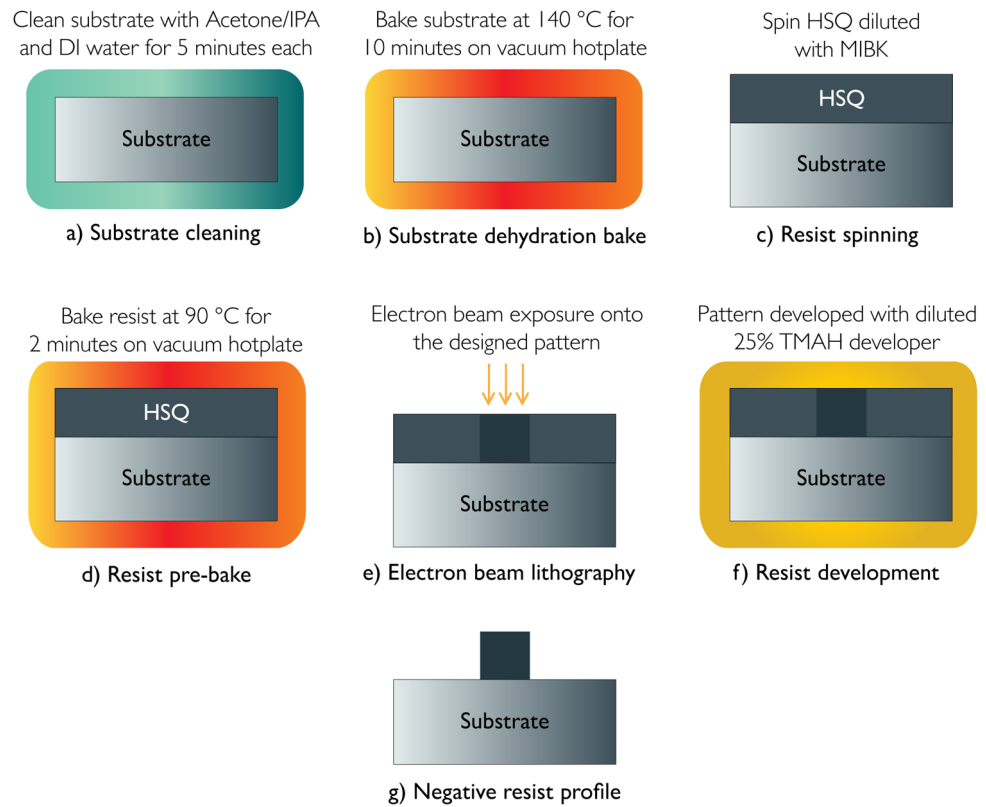


Figure 2-8: Sample preparation stages for HSQ resist.

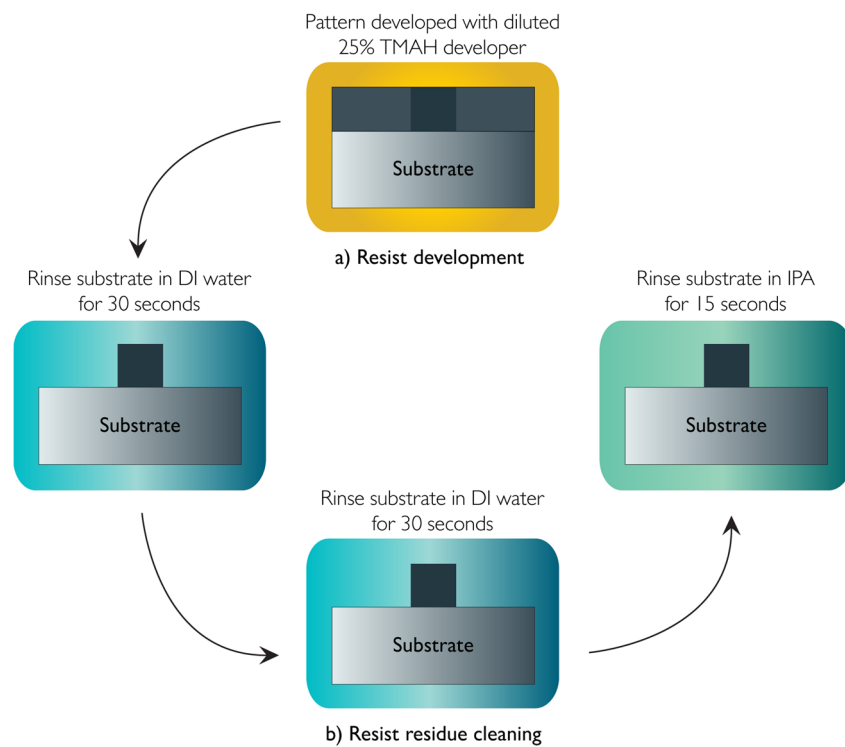


Figure 2-9: Resist development stages of HSQ resist.

### 2.4.2. Results & Discussions

To understand the patterning and resist development mechanisms, initially 150 nm thick HSQ is used for the experiments and once the process is optimized, it has been applied to different thickness. Line edge roughness (LER) limits the performance of the nanoscale devices and increases the overall resistivity of the channel especially when widths are below 50 nm. It should be as small as possible to reduce the fluctuations in linewidth. In HSQ, LER depends on number of factors including resist pre-bake temperature, exposure dose and developer concentration but pre-bake temperature has a greater influence on LER. It has been reported that rise in pre-bake temperature from 90 °C to 220 °C increases an overall surface roughness of 0.75 nm prior to exposure whereas the contrast decreases substantially with increase in sensitivity after exposure [17]. This is due to the fact that during the curing process, the bond scission and recombination takes place and reduces the ratio between cage to network with increasing pre-bake temperature and as a result there is significant reduction of hydrogen concentration and increase in silicon dangling bonds. The pre-bake temperature influences the LER more than the developer concentration since it distorts the overall HSQ film and its granularity, under these considerations the resist was pre-baked at 90 °C for 2 minutes which is believed to not effectively disrupt the cage to network ratio.

There are different strategies to pattern 10 nm lines, single (pass) pixel exposure is the most common but could potentially result in larger LER, therefore we first investigated the effect of LER as a function of beam step size (BSS). Figure 2-4 illustrates the exposure shots of 10 nm lines with a BSS of 2.5, 5 and 10 nm corresponds to 4, 2 and 1 electron beam exposure passes through the designed line with a  $\sim 3$  nm spot size. The substrate developed with 6.25% TMAH for 60 seconds and rinse in DI water and IPA for 60 and 15 seconds respectively and below dry with N<sub>2</sub>. I found that exposure dose reduced linearly from 2700  $\mu\text{C}/\text{cm}^2$ , 2500  $\mu\text{C}/\text{cm}^2$  and 2300  $\mu\text{C}/\text{cm}^2$  for HSQ lines exposed with 2.5, 5 and 10 nm BSS. Figure 2-10 shows the fabricated where the LER increases with increase in the BSS, whilst the linewidth is reduced to  $\sim 8$  nm with a 10 nm BSS but the LER is  $> 2$  nm corresponds to 20% of the linewidth. The HSQ lines written with 5 nm BSS has  $> 1$  nm LER, whereas with 2.5 nm BSS there is almost no visible LER. Therefore for the rest of the experiments, the substrates are written with a BSS of 5 nm whereas for the devices where LER is very critical a smaller BSS is used.

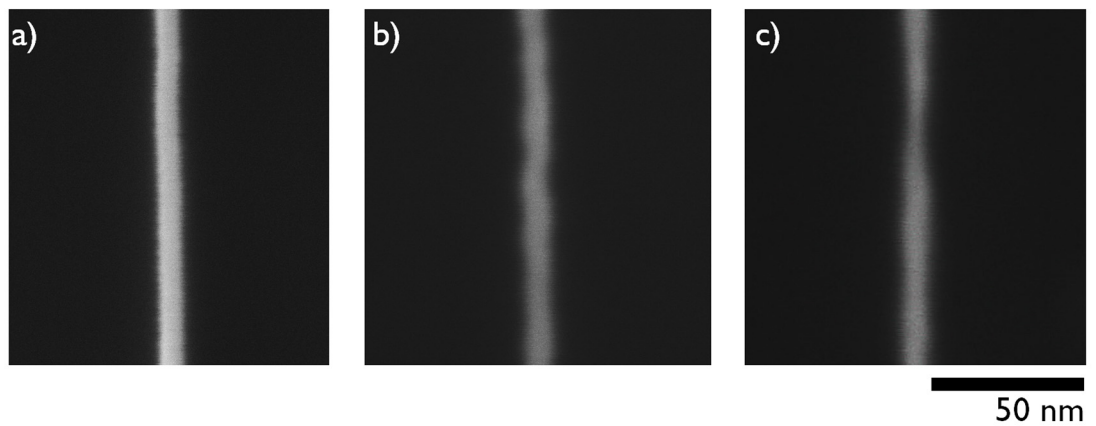


Figure 2-10: Top view SEM images of HSQ lines written with a) BSS = 2.5 nm, b) BSS = 5 nm and c) BSS = 10 nm.

Several demonstrations suggests low resist pre-bake temperature, higher exposure dose and stronger developer concentration result in better throughput [16] but in this work since we used thicker (~150 nm) HSQ resist with a strategy to achieve 10 nm linewidths, we observed and came out with a slightly different conclusion explained shortly. For a better comparison and understanding, I investigated each development parameter one at a time.

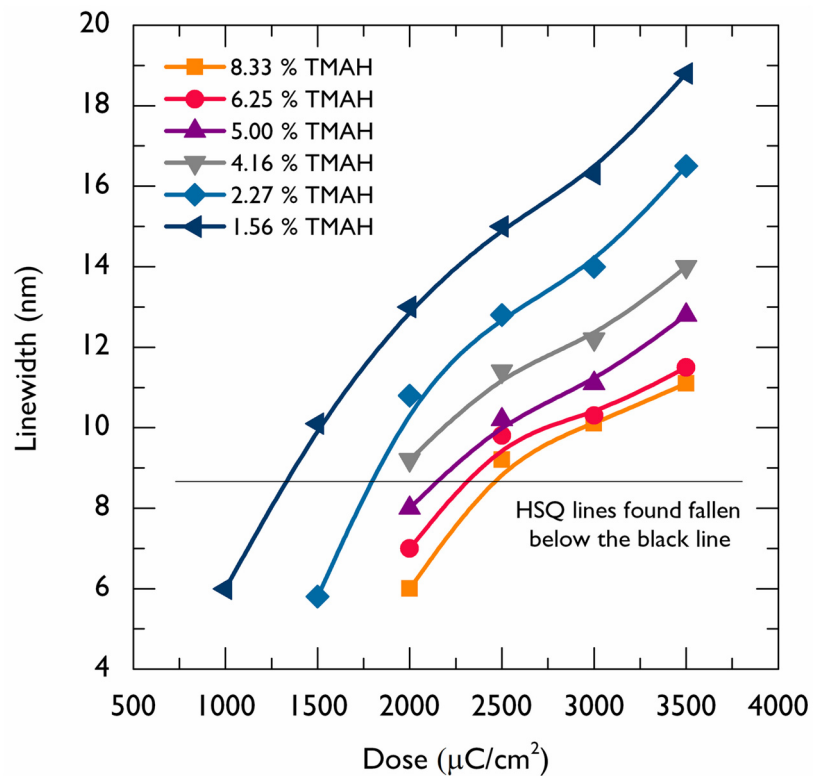


Figure 2-11: The HSQ linewidths as a function of exposure doses.

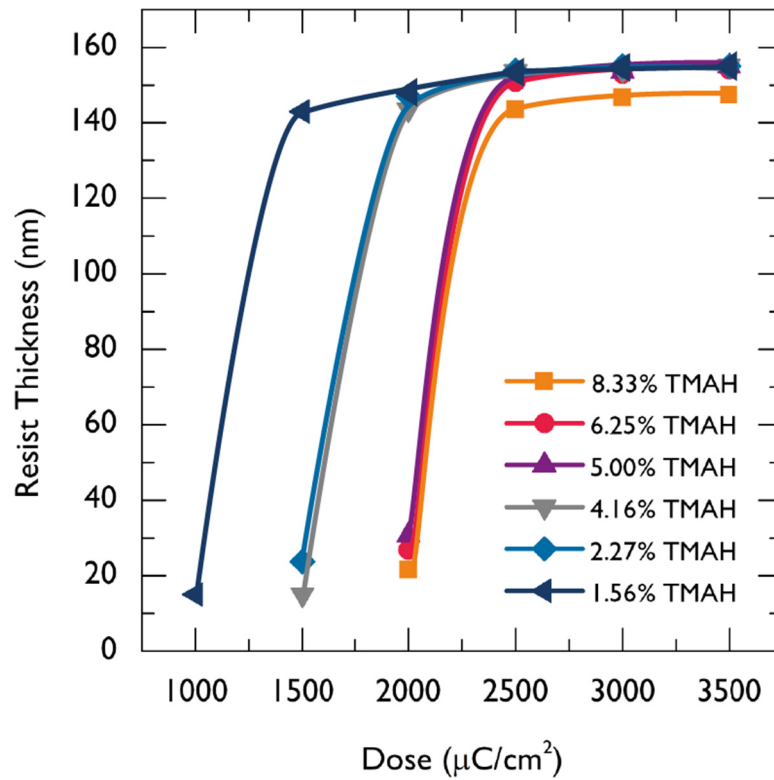


Figure 2-12: The contrast curve of HSQ resist for 10 nm linewidths.

To investigate the effect of developer dilution onto 10 nm linewidths, the substrates exposed with a dose ranging from 500 to 5000  $\mu\text{C}/\text{cm}^2$  and developed for 60 seconds at 23 °C in 25% TMAH developer diluted with DI water to make dilutions from 12.5% to 1.56% TMAH. All the substrates are further rinsed in DI water for 60 seconds and in IPA for 15 seconds before blown dry with  $\text{N}_2$ . The substrates then investigated under SEM and AFM to determine the linewidths and resist thickness without been coated/sputtered with any metal. Figure 2-11 and figure 2-12 shows the change in the linewidths and resist thickness as a function of exposure dose by varying TMAH developer dilution from 8.33% to 1.56%. I found that 10 nm lines completely washed out with 25% TMAH whereas ~15 nm faded linewidths appeared with 12.5% TMAH show in figure 2-12a where the resist is mostly collapsed, whilst the exposure dose is increased to allow lines to stand firmly but the overall linewidths increased with increasing dose. This is probably happen due to increase in the surface tension during resist development where strong developer tends to remove the unexposed resist more aggressively and result in wispy and faded HSQ lines below 15 nm.

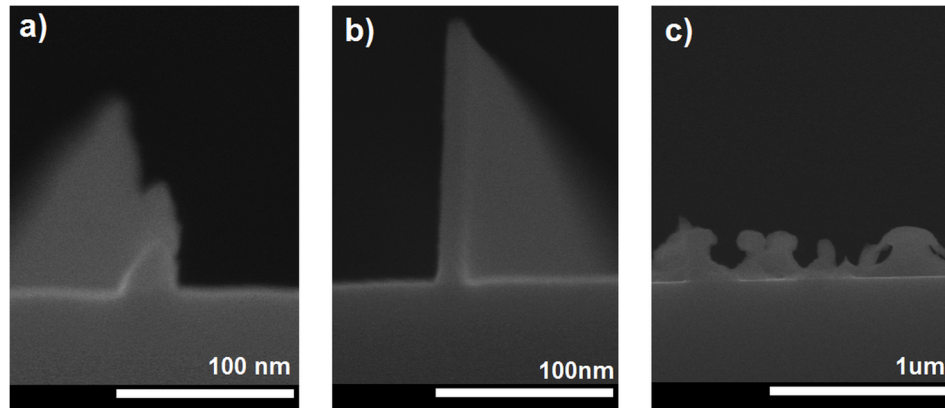


Figure 2-13: Cross sectional SEM images of HSQ lines with a) 12.5% TMAH, b) 2.27% TMAH and c) 1.19% TMAH.

The contrast of the negative tone resist is given by,

$$\text{Contrast } (\gamma) = \frac{1}{\text{Log } D_1 - \text{Log } D_0}$$

Where sensitivity is inversely proportional to the contrast,  $D_0$  is the initial dose at which the exposure starts and  $D_1$  is the dose at which the resist is fully exposed. The resist development curve is shown in figure 2-12, the developer concentrations from 8.33% to 1.56% TMAH result in much stable linewidths from  $\sim 9$  nm to 15 nm respectively, whereas the development completely stopped at 1.19% TMAH show in figure 2-13c. The numbers extracted from development curve for contrast and sensitivity are high because the pitch of the designed pattern is  $1 \mu\text{m}$  but the overall trend is equitable i.e. contrast is decreased from 10.31 to 5.68 and sensitivity is increased from  $0.097$  to  $0.176 \mu\text{C}/\text{cm}^2$  at 100 keV when HSQ lines are developed from 8.33% to 1.56% TMAH. Hence the area dose is significantly reduced for 10 nm lines from  $2500$  to  $1500 \mu\text{C}/\text{cm}^2$  due to increase in sensitivity by lowering the developer concentration. It is observed that at a dose of  $2500 \mu\text{C}/\text{cm}^2$  and above almost all the HSQ lines were stable with all developer concentrations and the linewidth varied only by  $\sim 1$  nm from 8.33% to 5% TMAH. The dose values in our case are much lower than the 10 nm HSQ lines produced in 40 nm thin resist and developed in 25% TMAH where the exposure dose is  $\sim 28,000 \mu\text{C}/\text{cm}^2$  on the same lithography system [18].

So it can be concluded that 6.25% TMAH provides the optimum balance between the minimum linewidth and the reproducibility. So, the next parameter which was investigated was resist developing temperature. The substrate exposed with a fixed dose of  $2500 \mu\text{C}/\text{cm}^2$  and developed in 6.25% TMAH for 60 seconds at different temperatures between  $10^\circ\text{C}$  to  $75^\circ\text{C}$ . High temperature TMAH development is known to rapidly remove lower molecular weight partially cross-linked HSQ molecules more vigorously while maintaining the mechanical integrity of exposed regions [19]. Hence the contrast increases with increasing temperature whereas the sensitivity decreases. The exposed substrates were developed at different temperatures and it was found that the linewidth decreases as expected by  $\sim 3.5 \text{ nm}$  from development between  $10^\circ\text{C}$  to  $45^\circ\text{C}$  but the overall uniformity of HSQ lines also decreased along with the resist thickness. At  $75^\circ\text{C}$  the HSQ lines effectively reflowed as shown in figure 2-14c. This suggests that the development around  $23^\circ\text{C}$  is ideal since there is no significant change in the linewidth and the HSQ lines are much smoother at room temperature.

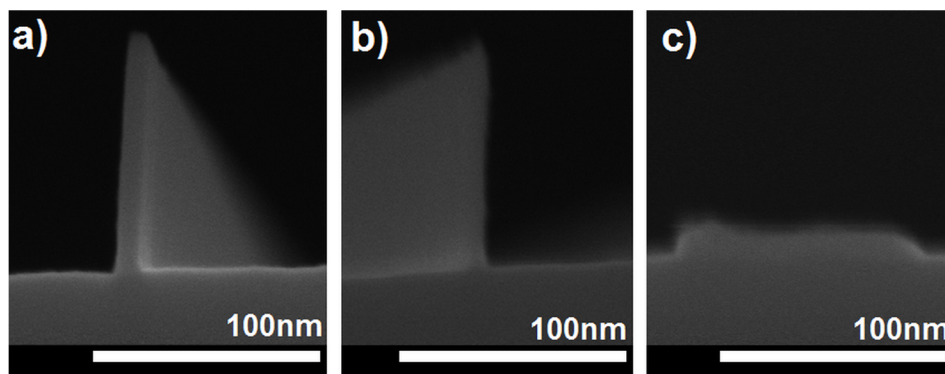


Figure 2-14: Cross sectional SEM images of HSQ lines developed at a)  $10^\circ\text{C}$ , b)  $45^\circ\text{C}$  and c)  $75^\circ\text{C}$ .

The final parameter which was investigated is resist developing time. The substrate exposed with a fixed dose of  $2500 \mu\text{C}/\text{cm}^2$  and developed in 6.25% TMAH between 30 and 120 seconds at  $23^\circ\text{C}$ . Figure 2-15b shows the resist developing time as function of linewidth and resist thickness, it was observed that the resist is not fully developed below 30 seconds and there is no major change in linewidth when resist developed between 60 and 120 seconds apart from the fact that the resist thickness is reducing with increasing development time. Hence it is clear that 60 seconds is the optimum time for development while preserving the maximum resist thickness.



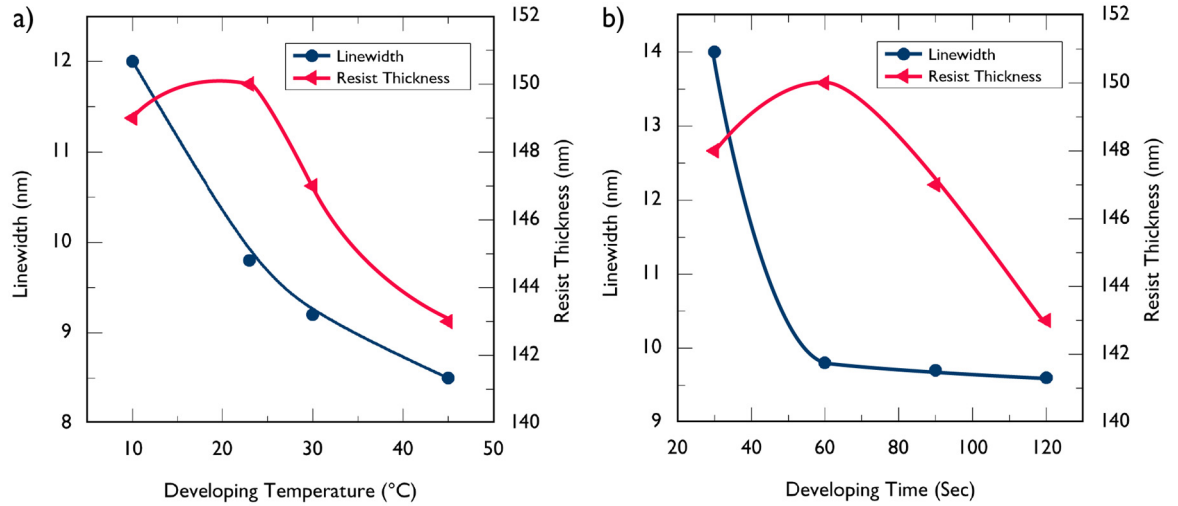


Figure 2-15: The resist developing temperature (a) and developing time (b) as a function of HSQ linewidth and resist thickness.

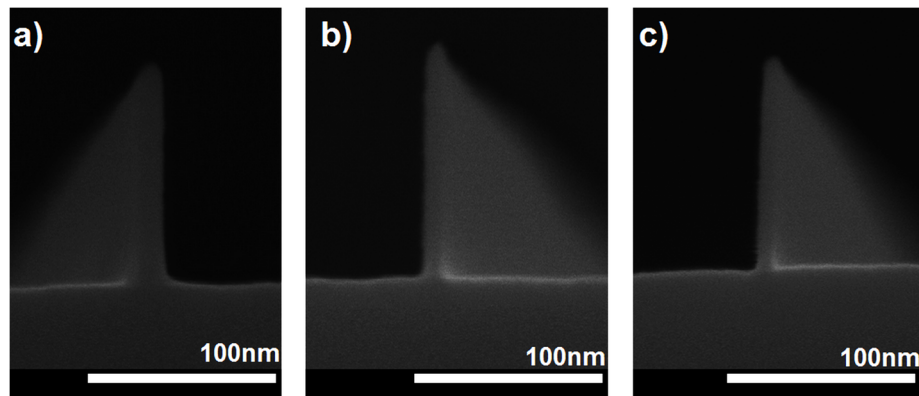


Figure 2-16: Cross sectional SEM images of HSQ lines developed for a) 30 seconds b) 90 seconds and c) 120 seconds

### 2.4.3. Summary

A process for patterning 10 nm features in negative tone HSQ resist has been developed by investigating a wide range of TMAH developer dilutions from 12.5% to 1.56%. Based on the optimized developer strength and dose, developing time and temperature are also investigated with view to pattern high aspect ratio 10 nm HSQ lines. From results it can be concluded that to produce high aspect ratio 10 nm HSQ lines, the optimum development parameters are 6.25 % TMAH developer concentration, 60 seconds development time at 23 °C with an exposure dose of 2500  $\mu\text{C}/\text{cm}^2$  using 5 nm BSS and  $\sim 3$  nm spot size. Similar process parameters are

applied to 50 and 250 nm thick resist and which repeatedly produced similar results. Figure 2-17 shows a) 5:1, b) 15:1 and c) 25:1 aspect ratio 10 nm linewidths. These results are best in our knowledge are the first demonstration of ultra-high aspect ratio 10 nm HSQ linewidths and have potential to realize many new types of devices where deep etches are required at smaller linewidths. In chapter 3, these HSQ lines are extensively used as a dry etch mask to optimize processes for high resolution pattern transfer in silicon substrate with great reproducibility and reliability.

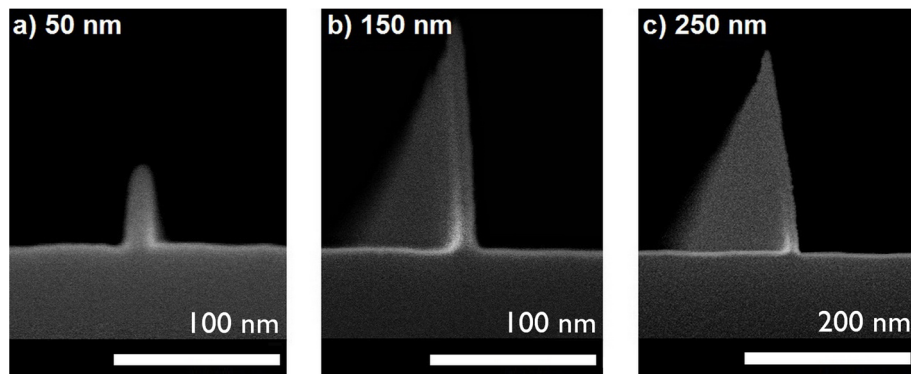


Figure 2-17: Cross sectional SEM images of 10 nm HSQ linewidths using a) 50 nm, b) 150 nm and c) 250 nm thick resist.

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### 3. Reactive Ion Etching Silicon Nanowires

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This chapter explains the different processes developed for the nanofabrication of highly anisotropic (vertical), smooth and uniform silicon nanowires using reactive ion etching (RIE). A particular effort has been made to enhance the quality and flexibility of the pattern transfer process using  $\text{SF}_6/\text{C}_4\text{F}_8$  based plasma chemistry to fabricate high aspect ratio silicon nanowires using an optimized HSQ resist process that repeatedly deliver 10 nm linewidths. The key strategy in here is to start with a thicker HSQ resist and then improve and optimize the etch process in terms of investigating the combination of different etchant and passivation gases, their flow rates, chamber pressure, chamber temperature and the platen/coil power to achieve higher etch rate and selectivity while reducing the linewidth and preserving a highly anisotropic etch profile to allow thinner resist to be used to etch silicon nanowires with very close proximity in order to realize a number of different types of silicon nanowire devices.

#### 3.1. Reactive Ion Etching

Reactive ion etching is the most widely used pattern transfer technique for top-down fabrication of micro and nano-scale features by etching the substrate with reactive ions comes from the plasma. Plasma is a partially or fully ionized gas which is almost neutral and consists of energetic molecules, electrons and ions. Figure 3-1 shows conventional RIE system where plasma is generated in presence of reactive gases under high vacuum of orders of few millitorr (mTorr) by applying a radio frequency (RF) power between the capacitively coupled cathode, which carries the substrate to be etched and the anode which is grounded. The free electrons accelerated from the electric field collides with the gas molecules result in more electrons and ions through a dissociative process, which continues until the plasma is generated. The mobility of electrons are higher than ions, hence during first few cycles the electrons collides with the walls of the chamber to build a negative charge and once that's established, it repels further electrons, meanwhile the substrate electrode acquires a negative potential (DC bias voltage) onto the coupling capacitor, ultimately creates a dark space above the substrate electrode which penetrate the electrons and accelerate ions perpendicular to the substrate result in physical and chemical etching. There is only a small proportion of ions can be generated from the reactive

gas, typically  $10^8 - 10^{10} \text{ cm}^{-3}$  which can be increased by increasing the RF power and lowering the chamber pressure [1]. In order to etch anisotropically, the physical and chemical etching mechanisms has to be balanced by optimizing RIE parameters i.e. RF power, gas flow ratio, chamber pressure and chamber temperature.

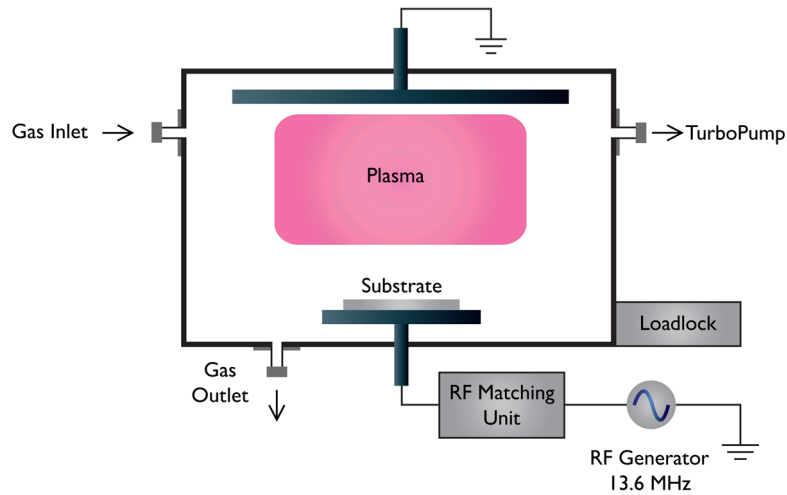


Figure 3-1: Schematic diagram of the conventional RIE system.

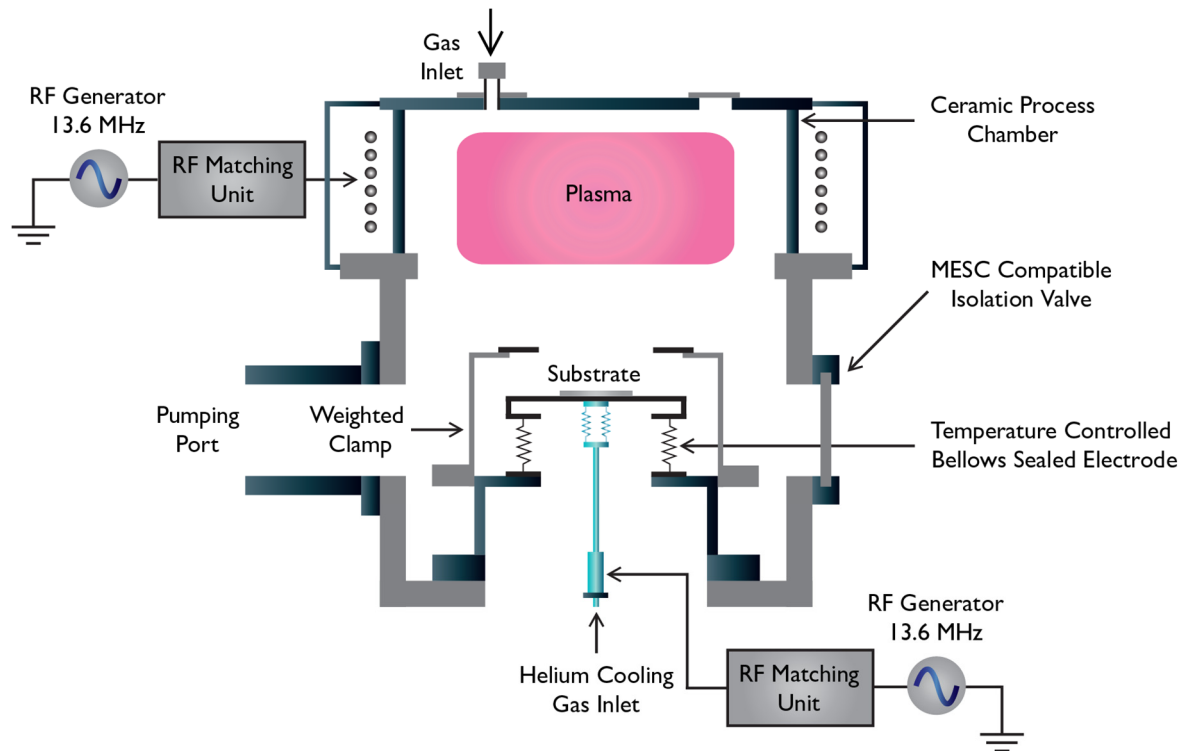


Figure 3-2: Schematic diagram of the STS ICP-RIE system.

Figure 3-3 [1] illustrates different etching mechanisms that take place simultaneously during ion bombardment in a typical RIE process which are as follow,

1. Ions sputter onto the surface of the substrate and transfer their momentum to knockout the surface atoms, attributed to physical etching. Initially this is helpful to remove any hydrocarbon contaminations and native oxide to prepare a clean surface to promote gas molecules to get absorb onto the surface [2]
2. Some ions are extremely reactive and they directly react chemically with surface atoms and form volatile products, attributed to reactive etching
3. Most of the ions releases energy on the surface of the substrate results in formation of radicals, which reacts chemically with the surface atoms to form volatile products, attributed to radical etching. It is these radicals which predominantly contribute towards the etching
4. The radicals move around through surface migration and reacts with the surface atoms to form volatile products
5. All the volatile products are frequently pumped away from the chamber to avoid any re-deposition during RIE process

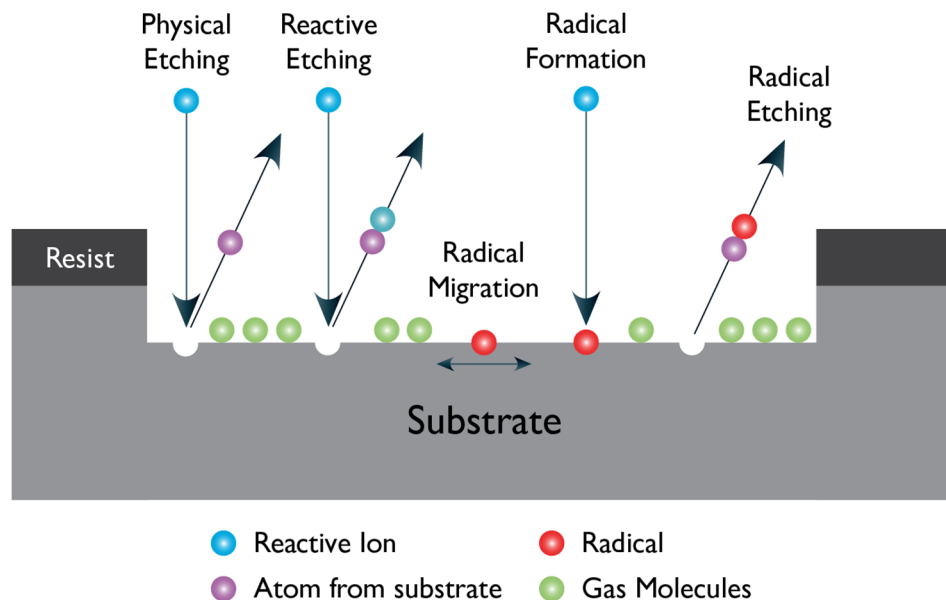


Figure 3-3: Etching mechanisms during RIE process.

Nano-scale device fabrication heavily depends on the quality of the pattern transfer to achieve high reliability, moderate etch rates and selectivity, smooth and anisotropic etch profiles and most importantly low plasma-induced sidewall damages. Whilst high density plasma allows to achieve high etch rates but requires higher RF power which increases the bias voltage and effectively accelerates the high energy ions from the plasma towards the substrate to etch, but it may introduce trap states on the surface of substrate which is the major cause of plasma-induced sidewall damages, termed as 'sidewall depletion' in nanowires, limits the performance of the devices. In general, these damages increases with higher RF power.

In a typical RIE system as shown in figure 3-1, the density of the plasma is proportional to the RF power which in turn increases the bias voltage. The etch rates are associated with the density of the plasma whereas the substrate damages are due to higher bias voltages. In order to keep them separate, inductively coupled plasma (ICP) RIE systems are used where the coil is wrapped around the chamber and provided with a RF power (coil) to generate the high density plasma, whereas to extract the ions, another RF power (platen) is provided to the substrate electrode to allows the generation of high density plasma at expense of low bias voltages. Silicon can be etched with any halogen containing gas including  $\text{CF}_4$ ,  $\text{SF}_6$ ,  $\text{NF}_3$ ,  $\text{SiCl}_4$ ,  $\text{BCl}_3$  and  $\text{HBr}$ . These gases are chemically reactive and produce enormous amount of radicals which are the primary source etching and often mixed with a passivation gas to improve the etch profile. Fluorine (F) based gases result in isotropic etching whereas chlorine (Cl) based are known to etch anisotropically since etching is dominated by ions, Therefore the etch rate and selectivity is higher with F comparing Cl based gases [3].

High aspect ratio silicon etching is widely realized with ICP-RIE system using a Bosch process with  $\text{SF}_6/\text{C}_4\text{F}_8$  based plasma [4] with particular applications in microelectromechanical (MEMS) systems, but the Bosch process comes with a fundamental problem of sidewall scalloping where the alternating etch steps i.e. etching and passivation create undulations in sidewall profile deteriorate the surface roughness down to  $\sim 100$  nm [5], whilst such roughness is negligible for etching micro-scale features in MEMS but become comparable while etching nano-scale features, because the size of scallops can be more than the width of the nanowire. Minimizing the etching-passivation cycle duration can possibly average out the scallops but at an expanse of reducing the etch rate and selectivity which is distinctive feature of Bosch process. The  $\text{SF}_6/\text{O}_2$  based plasma can anisotropically etch nano-scale features in silicon with smooth



sidewalls by cryogenic cooling of the wafer [6], but it may result in thermal stress, shrinkage and cracking issues comes from the different layers of resist/metal/semiconductor due to difference in their thermal expansion coefficients. Therefore, in this particular work, realizing the silicon nanowires requires very smooth and vertical sidewalls with good etch rate and selectivity, the main focus is on etching 10 nm silicon nanowires using a continuous – mixed mode  $\text{SF}_6/\text{C}_4\text{F}_8$  based ICP etch process at 20 °C.

### 3.2. Sample Preparation for Etching Experiments

HSQ resist has proven to be the best candidate for high resolution 10 nm electron beam lithography, it has low line edge roughness, high dry etch resistance and good mechanical strength make it suitable to be used for pattern transfer. Therefore we used HSQ resist not only for patterning nano-scale features but also used it as a hard mask for direct pattern transfer. Most of the demonstrations such as [7] used thinner HSQ resist layers to achieve high resolution lithography, since it's difficult to maintain the strength of the high aspect ratio resists at smaller linewidths due to increase in the surface tension during resist development stage results in adhesion problems but such thin HSQ resist layers restricts the etch depths. To overcome this, we developed processes to pattern 10 nm HSQ lines in thicker resists to be able to achieve high aspect ratio etching.

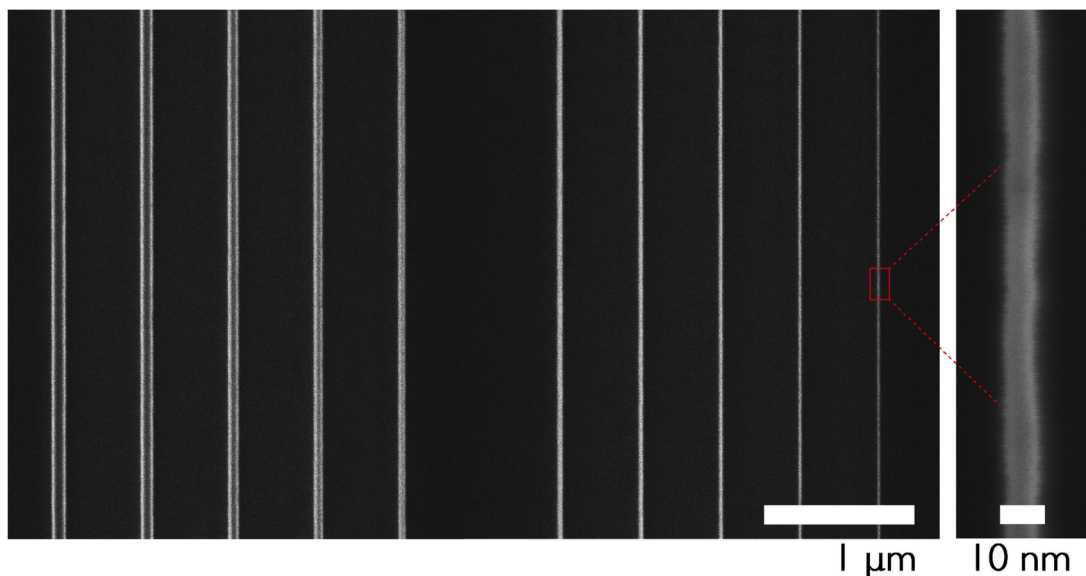


Figure 3-4: Top view SEM image of designed pattern for etching trials showing HSQ linewidths from 80 – 40 nm and 30 – 10 nm (left to right).

HSQ resist is patterned on 100 mm diameter silicon (100) wafers with 100  $\Omega$ -cm resistivity cleaved into  $10 \times 10$  mm substrates. The detail of processing is briefly as follow which has already been discussed in detail in section 2.4. Each substrate is cleaned successively with acetone, IPA and DI water for 5 minutes each in ultrasonic bath before blown dry with N<sub>2</sub>, substrates are then dehydrated baked on vacuum hotplate at 140 °C for 10 minutes after which the neat HSQ resist diluted 1:1, 1:2 and 1:3 with MIBK is spun onto the substrates at 2000, 2000 and 5000 rpm to get a thickness of 250, 150 and 50 nm respectively, the resist is pre-baked on vacuum hotplate at 90 °C for 2 minutes before electron beam exposure. Three sets of different linewidths are designed with 0.75  $\mu$ m period in L-Edit on 1.25 nm grid resolution, first from 1000 – 100 nm, second from 80 – 40 nm and third from 30 – 10 nm, and fractured using layout beamer software. Vistec VB6 is used to do exposure, first pattern written with a dose of 1500  $\mu$ C/cm<sup>2</sup>, BSS of 25 nm and spot size of  $\sim$  33 nm whereas second and third pattern written with a dose of 2700  $\mu$ C/cm<sup>2</sup>, BSS of 5 nm and spot size of  $\sim$  3-4 nm. After exposure the substrates developed in 6.25% TMAH solution for 60 seconds, rinsed in DI water twice for 30 seconds each and finally rinsed in IPA for 15 seconds before blown dry with N<sub>2</sub>. Finally the substrates are baked at 120 °C for 2 minutes in oven to dry it properly to remove any moisture. Figure 3-3 shows top-view SEM image of sample prepared for etch trails.

### 3.3. RIE Silicon Nanowires Using CF<sub>4</sub> Based Chemistry

Mechanisms of etching silicon with fluorocarbons such as CF<sub>4</sub> has been extensively explored [8] along with effects of addition of O<sub>2</sub> to the CF<sub>4</sub> plasma [9,10] to compensate the isotropic etching by the passivation of silicon oxyfluorides (SiO<sub>x</sub>F<sub>y</sub>) polymers onto the sidewalls. The F radicals reacts with the silicon surface to form SiF<sub>x</sub> species as a volatile product, whereas the addition of O<sub>2</sub> to the CF<sub>4</sub> plasma forms volatile carbon oxyfluorides (CO<sub>x</sub>F<sub>y</sub>) from CF<sub>x</sub><sup>+</sup> molecules, reduces the recombination of F radicals with CF<sub>x</sub><sup>+</sup>, hence rises the concentration of F radicals that increases the overall etch rate [11,12], however excessive increase of O<sub>2</sub> result in decrease in etch rate due to the thick passivation and reduction of F radicals as a result of recombination of F radicals with O<sub>2</sub>.

In this particular work, oxford instruments 80 plus RIE system is used to etch HSQ lines (in 150 nm thick resist) shown in figure 3-4. Initially the sample is etched in CF<sub>4</sub> at 25 sccm gas flow, 25 W platen power and 25 mTorr chamber pressure at 20 °C. With these conditions,

silicon was etched at 15 nm/minute but with an undercut of  $\sim 30$  nm result in highly isotropic 80 nm silicon nanowires with selectivity below  $\sim 0.5$ . That was expected since  $\text{CF}_4$  is a highly reactive gas, therefore  $\text{O}_2$  at 2 sccm fed into the chamber with same etch parameters to passivate the sidewalls with polymer, whilst the undercut reduced down to  $\sim 10$  nm for 30 nm silicon nanowires (figure 3-5a) but the etch rate is also reduced to 6 nm/minute and so the selectivity  $\sim 0.45$ . The flow of  $\text{O}_2$  is further increased to 3 sccm, which aided the passivation but etched 10 nm silicon nanowires with  $\sim 4$  nm undercut (figure 3-6c), increasing further the concentration of  $\text{O}_2$  result in tapered sidewalls due to excessive passivation. Due to the low etch rate and high bias voltage, platen power has not been changed throughout but only the chamber pressure which was reduced down to 9 mTorr but vertical sidewalls has never been achieved. The bias voltage was carefully monitored throughout the etching trials which was increased from  $-77$  V to  $-128$  V when  $\text{O}_2$  was added to  $\text{CF}_4$ .

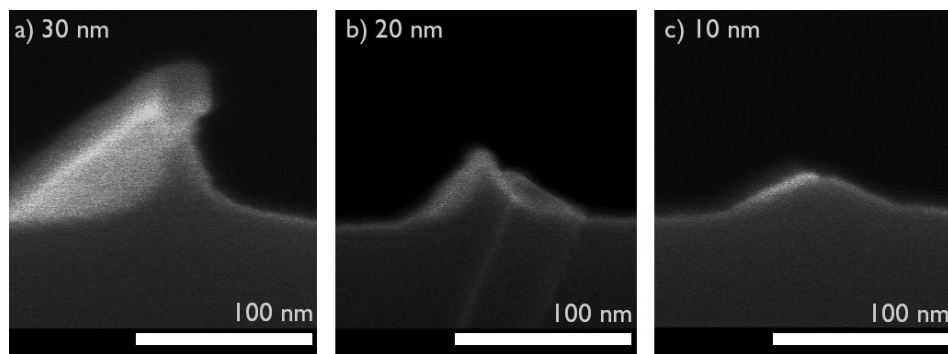


Figure 3-5: SEM images of silicon nanowires a) 30 nm, b) 20 nm and c) 10 nm etched using  $\text{CF}_4/\text{O}_2 = 25/2$  sccm, 25 W platen power and 15 mTorr chamber pressure.

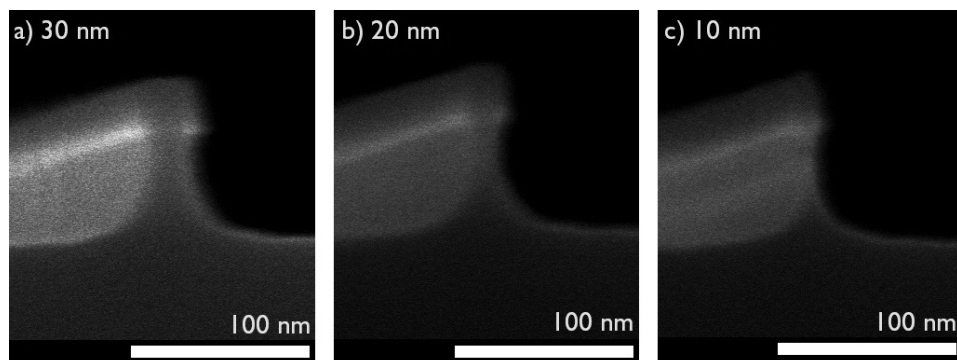


Figure 3-6: SEM images of silicon nanowires a) 30 nm, b) 20 nm and c) 10 nm etched using  $\text{CF}_4/\text{O}_2 = 25/3$  sccm, 25 W platen power and 15 mTorr chamber pressure.

The similar efforts been made to etch silicon nanowires using  $\text{CF}_4/\text{CHF}_3$  plasma, and after optimizing the gas flow ratios and chamber pressure, a process is optimized to etch 10 nm silicon nanowires with smooth and vertical sidewalls shown in figure 3-7 using  $\text{CF}_4/\text{CHF}_3 = 25/10$  sccm, 25 W platen power and 15 mTorr chamber pressure. This process etch silicon  $\sim 4$  nm/minute with a selectivity of  $\sim 0.7$  at a bias voltage of  $-180$  V. Such low etch rate and selectivity requires a very thin mask for pattern transfer and can only be useful to fabricate isolated nanowires. Since the proximity effect starts dominating in thicker resists, doesn't allow to make pattern with close pitch, hence the contrast will be low with thicker resists, also the etching can be trivial and can potentially dominated by resist lag effect. The other issue associated that process is the high bias voltage that could bring in high plasma induced sidewall damages which can limit the performance of nano-scale devices.

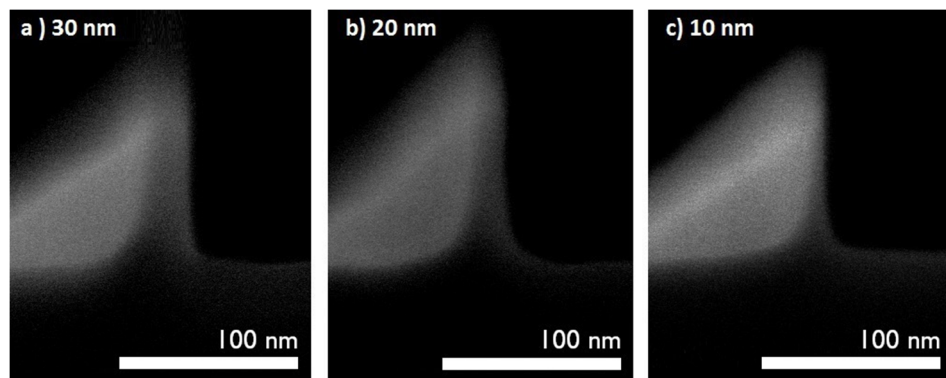


Figure 3-7: SEM images of silicon nanowires a) 30 nm, b) 20 nm and c) 10 nm etched using  $\text{CF}_4/\text{CHF}_3 = 25/10$  sccm, 25 W platen power and 15 mTorr chamber pressure.

### 3.4. ICP – RIE Silicon Nanowires Using $\text{SF}_6/\text{C}_4\text{F}_8$ Based Chemistry

Bosch process is widely acclaimed for high aspect ratio silicon etching, but for etching nanowires with widths down to 10 nm, a continuous mixed mode  $\text{SF}_6/\text{C}_4\text{F}_8$  based ICP etching is a preferred to avoid scallops and achieve highly vertical nanowires with smooth sidewalls [13,14,15]. Mixed mode allows etch and passivation at the same time, F radicals from  $\text{SF}_6$  reacts the silicon surface and form volatile  $\text{SiF}_x$  species to initiate the etching, meanwhile  $\text{C}_4\text{F}_8$  is used for passivation, deposits a very thin layer of fluorocarbon polymer  $(\text{C}_x\text{F}_y)_n$  similar to Teflon onto the substrate which is being etched horizontally by the directional bombardment of energetic ions ( $\text{SF}_x^+$ ) whereas sidewalls remains protected from being etched further [16].

In this work we aimed to optimize the etch process by balancing the etch and passivation through changing the gas flow ratios of  $\text{SF}_6$  and  $\text{C}_4\text{F}_8$  gases, coil/platen power and chamber pressure with approach to achieve moderate etch rate and selectivity with minimum possible platen power to minimize plasma induced damages.  $\text{SF}_6$  is the main etchant gas used with a flow rate between 20 – 40 SCCM whereas  $\text{C}_4\text{F}_8$  is used for passivation whose flow rate kept fixed at 90 SCCM for all the experiments, whereas the chamber pressure varied between 15 – 8.5 mTorr. All the etching experiments performed onto surface technology systems (STS) ICP-RIE system, schematic diagram of this system is shown in figure 3-2 [17]. This system consists of a 1000 W, 13.56 MHz coil source, inductively coupled to the chamber to generate high density plasma and another 30 W, 13.56 MHz platen source attached to the wafer electrode to allow independent control of bias voltage to extract ions from plasma. We selected a nominal coil power i.e. 600 W to generate a moderate ion density and selected a relatively low platen power i.e. 12 W to optimize a highly anisotropic RIE process by changing gas flow ratios and chamber pressure, and once the process is optimized the platen power is reduced down to 1 W to examine if the platen power can be reduced with minimum disruption to the optimized process.

The substrate is mounted over the carrier wafer which is normally coated with any photoresist to allow only the patterned substrate be etched, it also helps in reducing the loading effect. The wafer is mechanically clamped onto the wafer electrode and supplied with helium gas coolant to consistently maintain 20 °C temperature during the run. This system is equipped with automatic pressure controller (APC) value to automatically adjust the position of valve in accordance with the chamber pressure at a predetermined value.

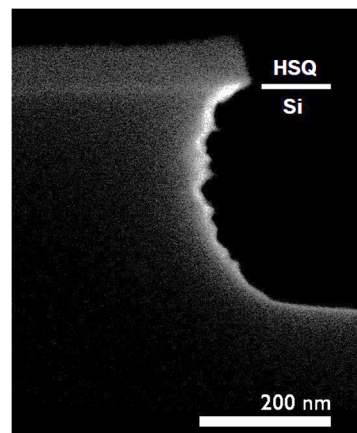


Figure 3-8: SEM cross-sectional image of Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 40:90$  sccm, 12/600 W platen/coil power and 15 mTorr chamber pressure (1 min).

### 3.4.1. Effect of Gas Flow Ratio

The effect of gas flow ratios of  $\text{SF}_6/\text{C}_4\text{F}_8$  are investigated in detail to determine the optimum balance between the etchant and the passivation gases. The etching and passivation processes simultaneously takes place, passivation is a complicated process involves ion induced reactions and sputtering of chemical components takes place in the chamber, this works in a way that the  $\text{SF}_6$  produce fluorine radicals to initiate spontaneous isotropic etching, whereas  $\text{C}_4\text{F}_8$  deposits a layer of  $(\text{C}_x\text{F}_y)_n$  polymer everywhere onto the substrate, especially on sidewalls to protect them from being etched. So, in order to achieve highly anisotropic etching, the etching and passivation has to be carefully adjusted by optimizing gas flow ratios.

Figure 3-4 shows the HSQ lines (in 150 nm thick resist) prepared for etching trails. All the samples simply placed in the middle of the carrier wafer without the use of any cool grease or wax, normally used in DRIE to increase thermal conductivity between the wafer and the sample. Initially the first sample etched for 1 minute with  $\text{SF}_6/\text{C}_4\text{F}_8 = 40:90$  sccm, 12/600 W platen/coil power at 15 mtorr chamber pressure, resulted in a large concave shaped undercut of  $\sim 70$  nm. It implies from figure 3-8 that only larger Si features managed to survive after 1 minute of etch duration due to significant flow of etchant over passivation gas.

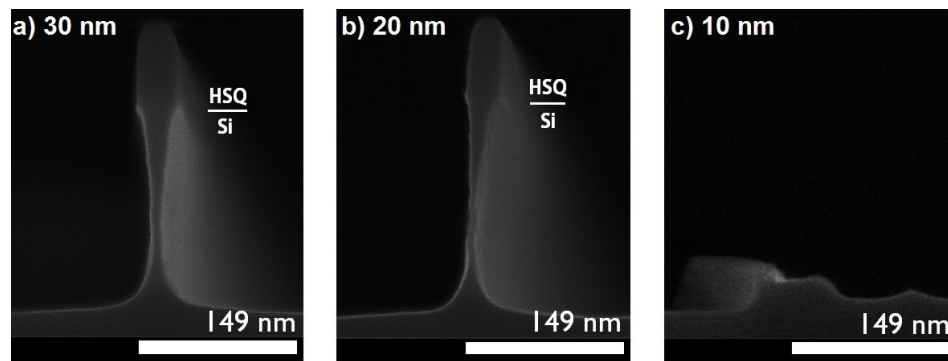


Figure 3-9: SEM cross-sectional image of Si nanowires etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 30:90$  SCCM, 12/600 W platen/coil power and 15 mTorr chamber pressure (1 min).

Whilst these etch conditions allowed to etch Si nanowires with widths above 500 nm but provided a start point to optimize the gas flow ratios, Three samples then etched with decreasing the flow of  $\text{SF}_6$  from 40 to 20 SCCM whereas the flow of  $\text{C}_4\text{F}_8$  kept fixed at 90 SCCM along with other etch parameters previously used. It is observed that the sidewall profile



changed dramatically from undercut to slightly tapered (positive) profile with decrease in the flow of  $\text{SF}_6$ . Figure 3-9 shows the etch results where the flow of  $\text{SF}_6$  reduced from 40 to 30 sccm, Whilst the undercut reduced and allow to etch 20 nm Si nanowires but the flow of  $\text{SF}_6$  was still slightly higher for 10 nm Si nanowires which are mostly found collapsed. All the Si nanowires with widths down to 10 nm etched at  $\text{SF}_6 = 25$  and 20 sccm able to completely survive shown in figure 3-10 and 3-11 respectively. A slight undercut has been observed with  $\text{SF}_6 = 25$  sccm which was compensated when  $\text{SF}_6$  decreased to 20 sccm result in slightly over passivated etch profile. Thus from these results it is clear that the gas flow ratios has larger impact onto the etch profile and has to be carefully adjusted in order to accurately control between etching and passivation onto the sidewalls to achieve 10 nm Si nanowires.

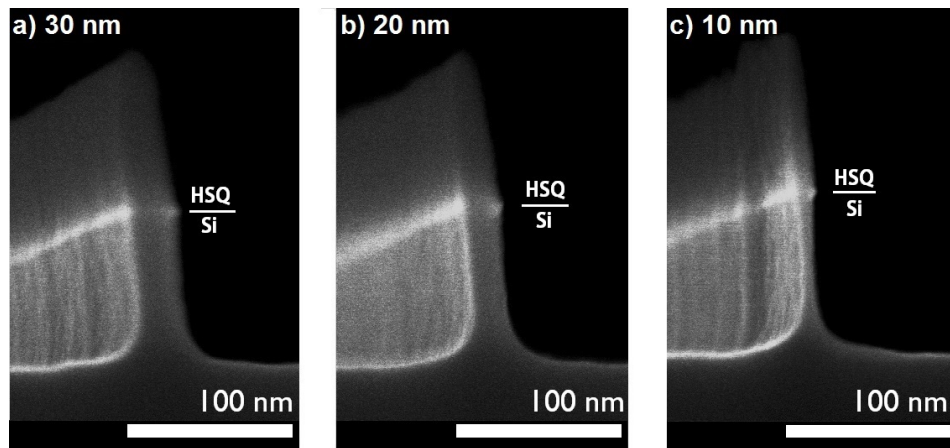


Figure 3-10: SEM cross-sectional image of Si nanowires etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 25:90$  sccm, 12/600 W platen/coil power and 15 mTorr chamber pressure (1 min).

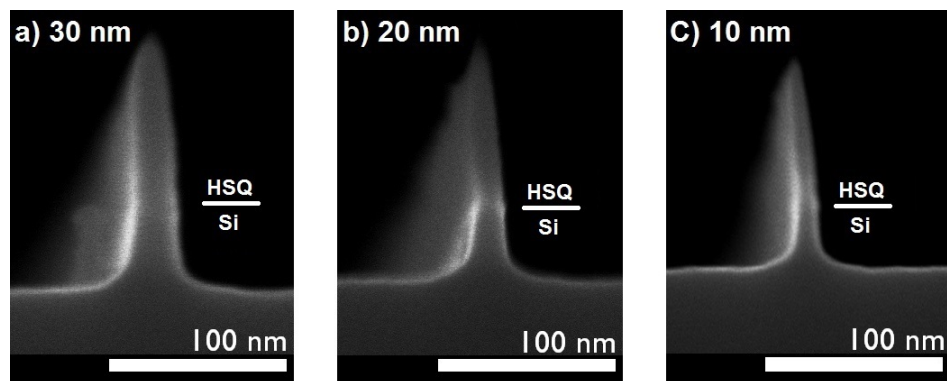


Figure 3-11: SEM cross-sectional image of Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 20:90$  sccm, 12/600 W platen/coil power and 15 mTorr chamber pressure (1 min).

Figure 3-12 shows the vertical and lateral etch rates as a function of gas flow ratios, whereas selectivity as a function of gas flow ratios is shown in figure 3-13. These data values are extracted from the SEM images, where the lateral etch determined from the middle of the nanowire at which it was concaved. Here the selectivity is defined as the ratio of the Si etched over the remaining HSQ resist. It is observed that the etch rate reduced from 360 nm/min down to 40 nm/minute when the flow of  $\text{SF}_6$  reduced from 40 to 20 sccm, meanwhile the selectivity is reduced from 4.65 to 0.72, this is due to the reduction of fluorine radicals in the  $\text{SF}_6$  /  $\text{C}_4\text{F}_8$  plasma. On the other side, lateral etch rate significantly reduced from 85 nm/minute to 8 nm/minute when the flow of  $\text{SF}_6$  reduced by 25% i.e. from 40 to 30 sccm, this is a dramatic 90.5% decrease in overall lateral etch rate, which means that there is more passivation then etching onto the sidewalls as a result of reduction of F radicals which were provoking spontaneous isotropic etching at higher flow of  $\text{SF}_6$ . Reducing the flow of  $\text{SF}_6$  further down to 20 sccm completely stopped the lateral etching which is attributed as the optimum balance between etching and passivation through adjusting gas flow ratios. The passivation on the bottom of the nanowire is more preferentially removed as compared to sidewalls, forcing Si nanowire to etch anisotropically.

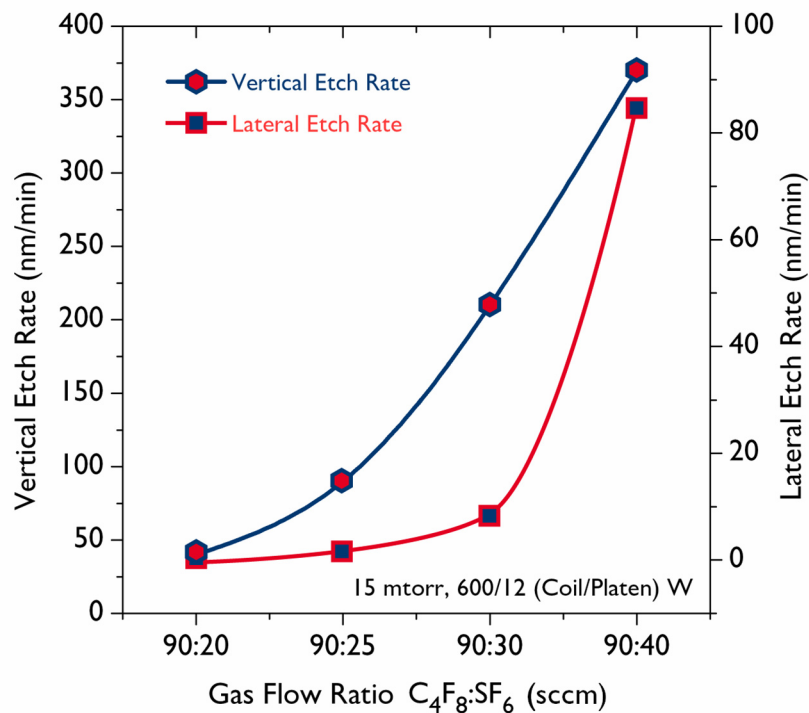


Figure 3-12: Vertical and lateral etch rates as a function of gas flow ratios.



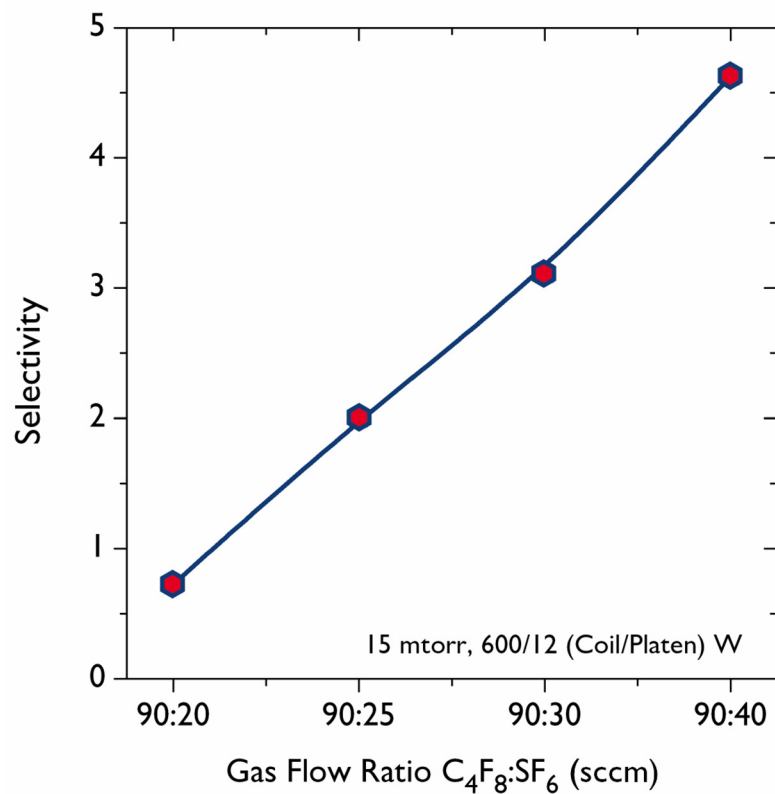


Figure 3-13: Selectivity as a function of gas flow ratios.

### 3.4.2. Effect of Chamber Pressure

The effect of chamber pressure on etch rate, selectivity and etch profile is investigated after optimizing the gas flow ratio to  $SF_6 / C_4F_8 = 25:90$  sccm in previous section. Whilst we are able to etch 10 nm Si nanowire with  $SF_6 = 20$  sccm, but the etch profile was slightly over passivated resulting in a low etch rate, therefore we used a slightly higher flow of  $SF_6$  (25 sccm) which although has a lateral etch rate of 1.5 nm/minute (i.e. 30% of the width of 10 nm Si nanowire), but we are aiming to improve the etch profile through optimizing the chamber pressure without compromising over the etch rate and the selectivity.

We etched the samples with  $SF_6 / C_4F_8 = 25:90$  sccm, 12/600 W platen/coil power and varied the chamber pressure between 15 – 8.5 mTorr. As mentioned before, 8.5 mTorr is the minimum achievable pressure with STS ICP-RIE system. Reducing the chamber pressure is known to make the plasma more electronegative that aids to etch sidewalls smoother and vertical, because the residence time of plasma species reduces by lowering the chamber pressure and as a result there will be fewer interactions of F radicals with the sidewalls which

helps to minimize lateral etching [18]. Figure 3-14 shows Si nanowires etched with 10 mTorr for 1 minute, comparing this with figure 3-10 in previous section, it is clear that by decreasing the chamber pressure from 15 mTorr to 10 mTorr, the etch profile changed from the concaved to highly vertical sidewall. Moreover we etched another sample by decreasing the chamber pressure further down to 8.5 mTorr and etched it for 1 minute and 45 seconds, these conditions allowed to etch 10 nm Si nanowire with  $\sim 20:1$  aspect ratio shown in figure 3-15c.

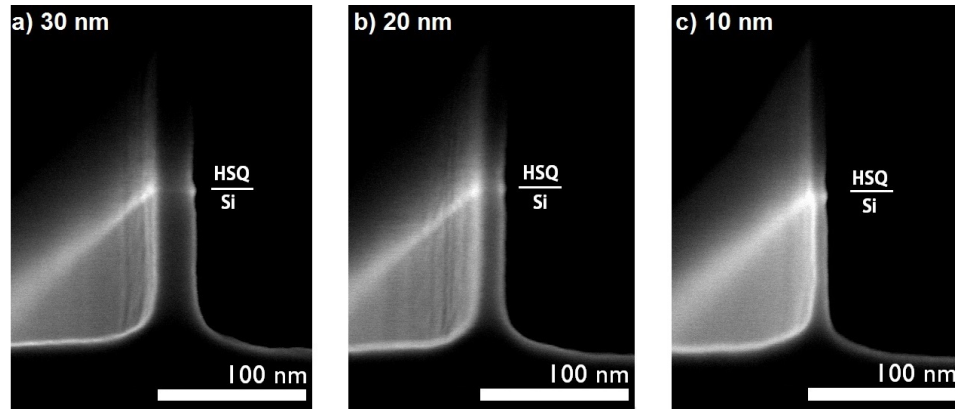


Figure 3-14: SEM cross-sectional image of Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 25:90$  sccm, 12/600 W platen/coil power and 10 mTorr chamber pressure (1 min).

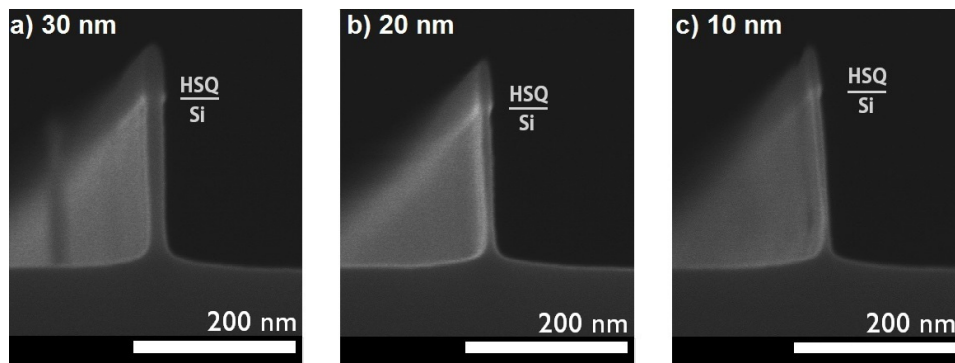


Figure 3-15: SEM cross-sectional image of Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 25:90$  sccm, 12/600 W platen/coil power and 8.5 mTorr chamber pressure (1 min 45 sec).

Figure 3-16 shows the vertical etch rate and selectivity as a function of chamber pressure, the data points are extracted from the SEM images. Since there is no measurable lateral etch rate, hence not included in analysis. The etch rate is increased from 90 nm/minute to 126 nm/minute when chamber pressure is reduced from 1 to 8.5 mTorr. Whereas the selectivity

is also increased from 2 to 2.4 as chamber pressure is reduced. This is obvious because the chamber pressure controls the amount of gas for ionization and the mean free path of the particles decreases with increasing chamber pressure which result in more electron-ion interactions, hence reducing the plasma density. In other terms the concentration of F radicals decreases as chamber pressure increases and as a result etch rate decreases which is evident from the plot.

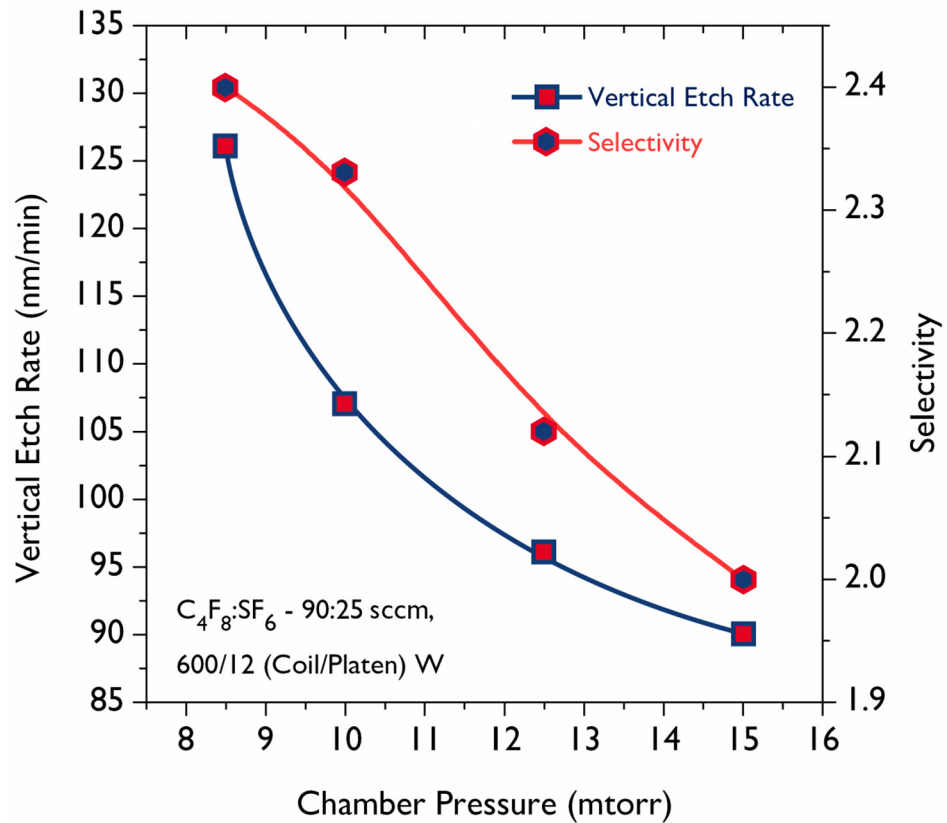


Figure 3-16: Chamber pressure as function of vertical etch rate and selectivity.

### 3.4.3. Process Optimization for High Aspect Ratio Etching

Optimizing the gas flow ratio and chamber pressure adequately controls the etch profile. The etch processes are optimized according to the resist thickness and required etch depths because the etch rate and selectivity changes as etching is initiated and normally increased as a function of etch duration. A gas flow ratio to  $SF_6 / C_4F_8 = 25:90$  sccm, 12/600 W platen/coil power and 8.5 mTorr of chamber pressure allowed to etch 10 nm Si nanowires with more than 200 nm etch depth (figure 3-15c), where  $\sim 60$  nm HSQ resist is still remaining over the

nanowire. To etch even deeper, the process need a bit of further optimization, since the pressure can't be reduced below 8.5 mTorr, the flow of  $\text{SF}_6$  is reduced down to 22 sccm. Figure 3-17b shows the 10 nm Si nanowires etched with  $\text{SF}_6/\text{C}_4\text{F}_8 = 22:90$  sccm, 12/600 W platen/coil power and 8.5 mTorr of chamber pressure, etched for 2 minutes and 30 seconds. Almost all of the 150 nm thick HSQ resist is consumed to be able to etch  $\sim 350$  nm deep in silicon, corresponds to  $\sim 30:1$  aspect ratio etching. We used a  $\sim 250$  nm thicker HSQ lines as hard mask and reduced the flow of  $\text{SF}_6$  to 20 SCCM in the recipe and able to etch 10 nm Si nanowire  $\sim 500$  nm deep in silicon ( $\sim 50:1$  aspect ratio) shown in figure 3-18b. Thus, by carefully optimizing the etch parameters, we able to demonstrate highly vertical and smooth ultra-high aspect ratio 10 nm Si nanowires. These processes provides very controlled etch depths with great reproducibility.

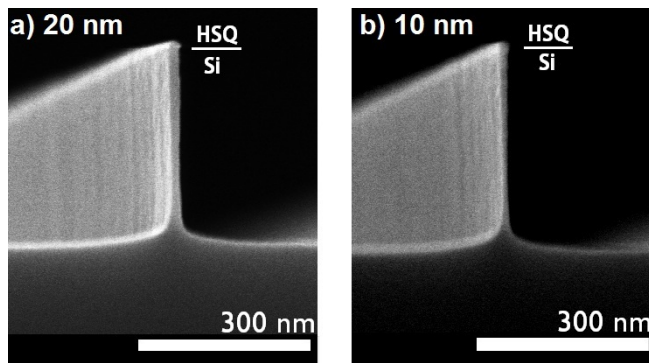


Figure 3-17: SEM cross-sectional image of Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 22:90$  sccm, 12/600 W platen/coil power and 8.5 mTorr chamber pressure (2 min 30 sec).

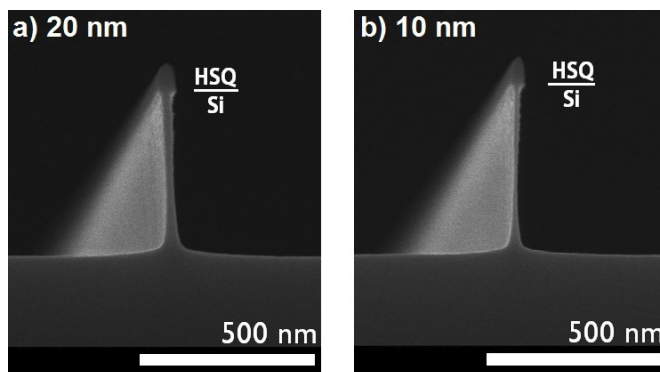


Figure 3-18: SEM cross-sectional image of Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8 = 20:90$  sccm, 12/600 W platen/coil power and 8.5 mTorr chamber pressure (3 min 30 sec).

### 3.4.4. Effect of Platen Power

The effect of platen power is investigated to minimize the plasma-induced sidewall damages. The dc bias voltage builds up as a result of applied platen power which controls the directionality of the ion bombardment perpendicular to the etching surface result in anisotropic etching. Ion bombardment helps to remove the passivation from the etching surface while retaining the passivation onto the sidewalls. The dc bias voltage is calculated as an average over the total etch duration. To investigate and understand the effect of platen power, we started with an optimized recipe, i.e.  $\text{SF}_6/\text{C}_4\text{F}_8 = 22:90$  sccm, 12/600 W platen/coil power and 10 mTorr of chamber pressure, results of which are shown in figure 3-14.

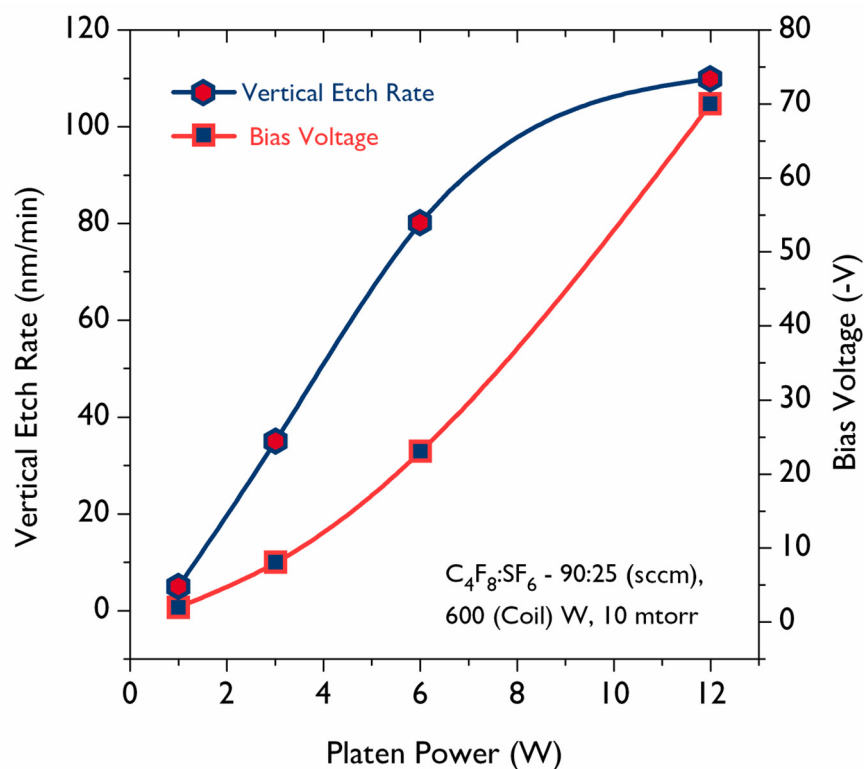


Figure 3-19: Platen power as a function of vertical etch rate and bias voltage.

We swept the platen power in that recipe from 12 to 1 W and observed the etch rate, selectivity and the etch profile. Figure 3-19 shows the platen power as function of vertical etch rate and bias voltage, the overall etch rate is reduced from 110 down to 5 nm/minute when platen power is reduced from 12 to 1 W, whereas the corresponding bias voltage is decreased from -70 to -2 V. The etch rate dropped by 27% between 12 and 6 W platen power whereas

the bias voltage is reduced by  $\sim 67\%$ , which is the optimum balance between a moderate etch rate and a low bias voltage. The profile remained very anisotropic even with a 6 W platen power whereas the samples etched with platen power below 6W has some lateral etching due to dominance of chemical etching over ion enhanced etching. A higher bias voltage causes intense ion sputtering onto the etching substrate enhances the efficiency of bond breaking and formation of etch products, thus increases the overall etch rate. Typically higher bias voltage results in significant percentage of plasma induced sidewall damages, so the etch processes should be optimized with a view to keep the bias voltage as low as possible.

Therefore, a low damage etch process is also optimized to minimize plasma-induced sidewall damages, an example of which is shown in figure 3-20 where a 5 nm HSQ line is patterned in thin HSQ resist  $\sim 30$  nm, which is used as a mask to etch highly anisotropic 5 nm Si nanowire at an etch rate of 80 nm/minute with a selectivity over 2. The average bias voltage for this process is  $-23$  V, which allows high quality pattern transfer for nanoscale devices

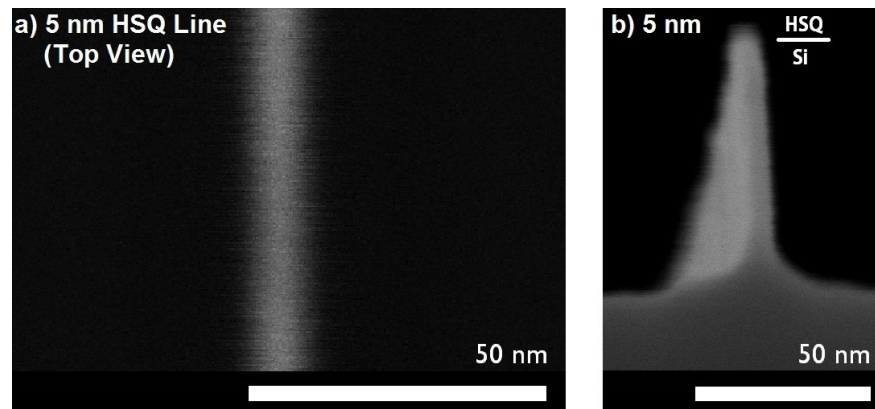


Figure 3-20: SEM images of a) 5 nm HSQ line, b) 5 nm Si nanowire etched using  $\text{SF}_6/\text{C}_4\text{F}_8$  = 25:90 sccm, 6/600 W platen/coil power and 10 mTorr chamber pressure.

### 3.4.5. Summary

Results are presented for the fabrication of Si nanowires with widths below 5 nm. Initially different etch chemistries have been investigated, where the effects of RF power, gas flow ratio and chamber pressure are studied in detail using  $\text{CF}_4$ ,  $\text{CF}_4/\text{O}_2$ ,  $\text{CF}_4/\text{CHF}_3$  based RIE and  $\text{SF}_6/\text{C}_4\text{F}_8$  based ICP-RIE plasma. Results indicated a large undercut  $\sim 30$  nm, when Si nanowires are etched with  $\text{CF}_4$  plasma, therefore  $\text{O}_2$  was added as a functional gas to  $\text{CF}_4$  plasma to reduce

the chemical reactivity of F radicals, which increased the sidewall protection but reduced the etch rate and lowered the selectivity, the process able to etch 10 nm Si nanowires with a  $\sim 4$  nm undercut. Later  $O_2$  was replaced with  $CHF_3$  to investigate if sidewalls can be further improved, whilst smooth and vertical 10 nm Si nanowires are etched with  $CF_4/CHF_3$  based plasma but at an etch rate of 4 nm/minute with a poor selectivity of  $\sim 0.7$ . Such etch selectivity requires thicker resists for etching and can only be useful to pattern simple geometries due to increase in the proximity effects, where pattern is designed with a smaller pitch. Moreover the bias voltage, which corresponds to the plasma induced sidewall damages was carefully monitored throughout the etching experiments, which has been varied between  $-77$  V to  $-180$  V. The term damage refers to any effect of the etch process, which includes disruption of the lattice structure, creation of dangling bonds on the interface, contamination of etched surface with polymer passivation layer and heavy metals, which result in deep traps for charge carriers, deteriorates the electrical characteristics of the nanowires. These damages can be reduced by optimizing the process parameters to etch the substrate with low bias voltages, detail of which can be found in [19,20,21,22].

Gases	$CF_4$	$CF_4/O_2$	$CF_4/CHF_3$	$SF_6/C_4F_8$
Etch rate	15 nm/min	5 nm /min	4 nm/ min	80 nm/min
Undercut	30 nm	4 nm	-	$< 1$ nm
Selectivity	0.5	0.4	0.7	2
Bias Voltage	$-77$ V	$-128$ V	$-180$ V	$-23$ V

**Table 3-1: A comparison of the etch processes optimized for 10 nm Si nanowire etching**

With a view to develop a process to etch faster with good selectivity and low bias voltage,  $SF_6/C_4F_8$  based ICP-RIE plasma has also been investigated. A process is optimized to deliver smooth and vertical high aspect ratio (50:1) 10 nm Si nanowires at an etch rate of 110 nm/minute with a selectivity over 2.4. The averaged bias voltage of the process was  $-70$  V. To ensure low damage etching, the platen power was lowered, which although reduced the etch rate to 80 nm/minute but significantly lowered the bias voltage to  $-23$  V to ensure high quality pattern transfer.

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## 4. Device Fabrication and Characterization Tools

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This chapter explains the nanofabrication of integrated silicon nanowire devices based upon the processes developed for lithography in HSQ resist and low damage reactive ion etching of silicon nanowires, explained in detail in chapter 2 and 3 respectively. The instruments and tools used for the electronic characterisation are the part of discussion along with the cryogenic systems to allow low temperature measurements.

### 4.1. Device Fabrication

The main steps involved in nanofabrication of 2 terminal nanowire devices, Hall-bar & Greek-cross devices, wrap-around gate field-effect transistors and side-gated field-effect transistors are discussed in detail in the following section.

#### 4.1.1. Layer-to-Layer Alignment

Figure 1-1 shows the cross-sectional illustration of silicon-on-insulator (SOI) substrate used in this work to fabricate silicon nanowire devices. Since the fabrication involves in multiple steps of lithography, etching and metallization, the square alignment marks are used to allow layer-to-layer alignment to precisely pattern the layers with respect to the existing patterns. Whilst metal alignment marks are preferred for high precision alignment on Vistec VB6 and Penrose marks are developed to achieve alignment accuracy down to  $\sim 1$  nm [1], but the devices are subject to anneal at high temperatures  $\sim 950$  °C and any metal in furnace can contaminate not only the furnace tubes but also the grown oxide, therefore etched marks are used throughout this work.

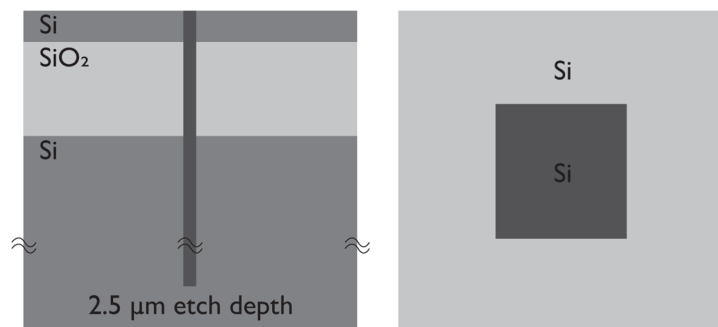


Figure 4-1: Illustration of etched marks, cross-sectional (left) and top-view (right).

The SOI wafer diced into 12 mm<sup>2</sup> chips where each chip initially patterned with a set of 50 μm<sup>2</sup> marks separated by 200 μm on each corner of the chip to allow global alignment. A tri-layer of PMMA is used for patterning where 15% 2041, 15% 2041 and 4% 2010 spun at 5K and baked at 140 °C for 2 minutes each. The pattern is exposed with a dose of 750 μC/cm<sup>2</sup>, BSS of 25 nm and spot size of ~ 33 nm. The exposed pattern developed in a solution of 1:2 (MIBK:IPA) for 60 seconds followed by a rinse in IPA for 10 seconds before blown dry with N<sub>2</sub>. After patterning, the different layers of SOI substrate are etched as follow:

Si (top): CF<sub>4</sub> = 25 SCCM, 25 W, 25 mTorr for 9.5 minutes

SiO<sub>2</sub> (middle): CHF<sub>3</sub>/Ar = 25/18 SCCM, 200 W, 30 mTorr for 8 minutes

Si (bottom): SF<sub>6</sub>/C<sub>4</sub>F<sub>8</sub> = 90:30 SCCM, 12/600 (platen/coil) W, 12 mTorr for 7 minutes

Figure 4-1 shows the illustration of etched marks, all the layers are etched down to 2.5 μm to able to get enough contrast for VB6's backscattered detector to locate marks. These etched alignment marks yields to ~ 50 nm layer-to-layer accuracy using global alignment and ~ 10 nm with cell alignment where the size of cell is less than the maximum field size of VB6.

#### 4.1.2. Lithography & Pattern Transfer

After the alignment marks transferred into SOI substrate, the chips are first cleaned ultrasonically in successive baths of acetone and isopropyl alcohol to remove remaining PMMA resist and later cleaned in a solution of de-ionized water, sulphuric acid (H<sub>2</sub>SO<sub>4</sub>) and hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>) at a concentration of 20:1:1 for 5 minutes to remove any organic residues from the surface of the substrate. Lithography for pattern transfer in silicon is proceeded using HSQ resist which is discussed in section 2.8. Figure 2-8 and 2-9 shows the illustration of steps followed after cleaning the chips with concentrated piranha solution. For all the device fabrication, ~30 nm thick HSQ resist is used for pattern transfer which is obtained by diluting HSQ with MIBK at a proportion of 1:5 and spinning the substrate at 5 K rpm. The thinner resist allows to pattern designs with close proximity and using an optimized silicon nanowire etch process [SF<sub>6</sub>/C<sub>4</sub>F<sub>8</sub> = 25:90 SCCM, 6/600 W platen/coil power and 10 mTorr] the pattern is transferred with a good selectivity (>2) in SOI substrate. Laser interferometer is used to monitor the etching through different layers. Each of the chip is individually etched in STS-RIE system with ~ 20% over-etch time to completely remove the unexposed silicon areas.

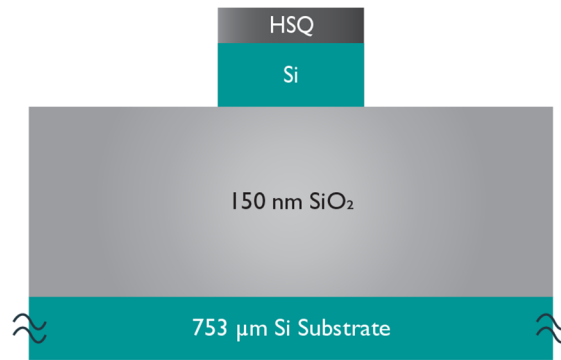


Figure 4-2: Cross-sectional illustration of etched silicon pattern.

### 4.1.3. Thermal Oxidation

The thermal oxidation is a process to grow a thin layer of oxide ( $\text{SiO}_2$ ) by the reaction of oxygen with silicon typically at high temperatures (850–1100 °C). It is performed onto the etched silicon nanowire devices to serve different purposes, primarily to passivate any dangling bonds and trap charges present at the silicon interface with oxygen atoms to remove electrical defects which result in current leakage along the interface through electron tunnelling, secondly to use  $\text{SiO}_2$  as gate oxide to fabricate devices with wrap around gates and thirdly to use  $\text{SiO}_2$  as a barrier to prevent dopant diffusion from the silicon. The growth of  $\text{SiO}_2$  result in low Si- $\text{SiO}_2$  interface state density [2]. In order to grow high quality oxide, the silicon surface should be perfectly cleaned, therefore piranha and RCA cleaning procedures [3] are followed prior to oxidation which are as follow,

1. Piranha cleaning: Agitate the substrate in a solution of de-ionized water, sulphuric acid ( $\text{H}_2\text{SO}_4$ ) and hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) at a concentration of 5:1:1 for 30 seconds and rinse in DI water for 1 minute and blown dry with  $\text{N}_2$
2. RCA 1 cleaning: Agitate the substrate in a solution of de-ionized water, ammonium hydroxide ( $\text{NH}_4\text{OH}$ ) and hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) at a concentration of 5:1:1 for 30 seconds and rinse in DI water for 1 minute and blown dry with  $\text{N}_2$
3. RCA 2 cleaning: Agitate the substrate in a solution of de-ionized water, hydrochloric acid ( $\text{HCL}$ ) and hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) at a concentration of 6:1:1 for 30 seconds and rinse in DI water for 1 minute and blown dry with  $\text{N}_2$
4. HF dip: Agitate the substrate in buffered hydrofluoric (HF) acid (10:1) diluted 1:3 with DI water for 45 sec and rinse in DI water for 1 minute and blown dry with  $\text{N}_2$

The piranha and RCA 1 solution removes any traces of organic residues whereas RCA 2 solution removes any metallic contaminations by oxidizing the silicon surface (Hydrogen peroxide is an oxidizing agent which promotes  $\sim 1\text{--}2\text{ nm}$  of oxide with the silicon surface). HF dip removes this oxide and prepares a neat surface for oxidation. A thin layer of polymer is deposited onto the sidewalls during silicon pattern transfer which is also being stripped off during these cleaning procedures.

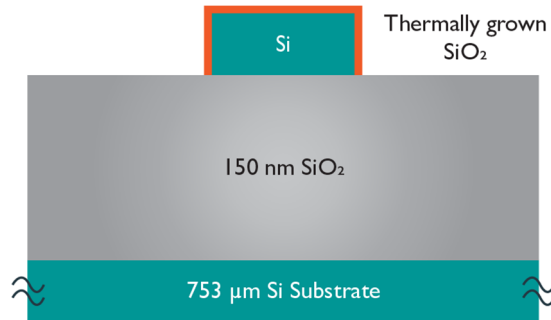


Figure 4-3: Cross-sectional illustration of etched silicon being thermally oxidized.

ATV PEO 145 furnace was used for thermal oxidation, the substrates were loaded for oxidation right after the HF dip. Initially, nitrogen was used at a flow of 350 litre/hour to ramp up the furnace to a temperature of  $950\text{ }^{\circ}\text{C}$  in 30 minutes after which substrates were exposed to oxygen at a flow of 400 litre/hour between 1–5 minutes to grow  $\sim 5\text{--}10\text{ nm}$   $\text{SiO}_2$ . After oxidation, the gas was switched back to nitrogen under which the furnace was slowly ramped down in another 30 minutes to room temperature. The high temperature annealing recrystallize the silicon atoms with dopant and remove the damage caused by the ion implantation, whereas the slow ramp down of temperature under nitrogen helps to lowers the fixed and interface trap charges present at the  $\text{Si-SiO}_2$  interface [4].

#### 4.1.4. Device Metallization and Annealing

A nickel silicide process was optimized to make ohmic contacts with the etched silicon nanowire devices. Nickel silicide is formed by migration of nickel into silicon to initially form  $\text{Ni}_2\text{Si}$  and after annealing the contact between  $400\text{--}600\text{ }^{\circ}\text{C}$  it forms  $\text{NiSi}$ . It has low sheet resistivity and low silicon consumption that makes it suitable to use in CMOS applications [5,6]. The platinum is often used along with nickel as a diffusion barrier which also aids to improve the thermal stability of the  $\text{NiSi}$  contact [7]. In this work,  $\text{Ni-Pt}$ : 20-50 nm is deposited using

Plassys-4 electron beam evaporator tool. The lithography for lift-off has been discussed in section 2.3 in detail. Prior to metal evaporation, the thermal oxide is stripped from the silicon pads opened for metallization using a HF dip by agitating the substrate in buffered hydrofluoric (HF) acid (10:1) diluted 1:3 with DI water for 45 sec and rinse in DI water for 1 minute and blown dry with  $N_2$ .

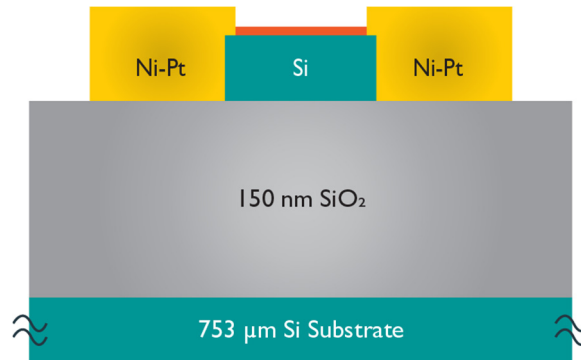


Figure 4-4: Illustration of depositing metal contacts to the etched silicon nanowire device.

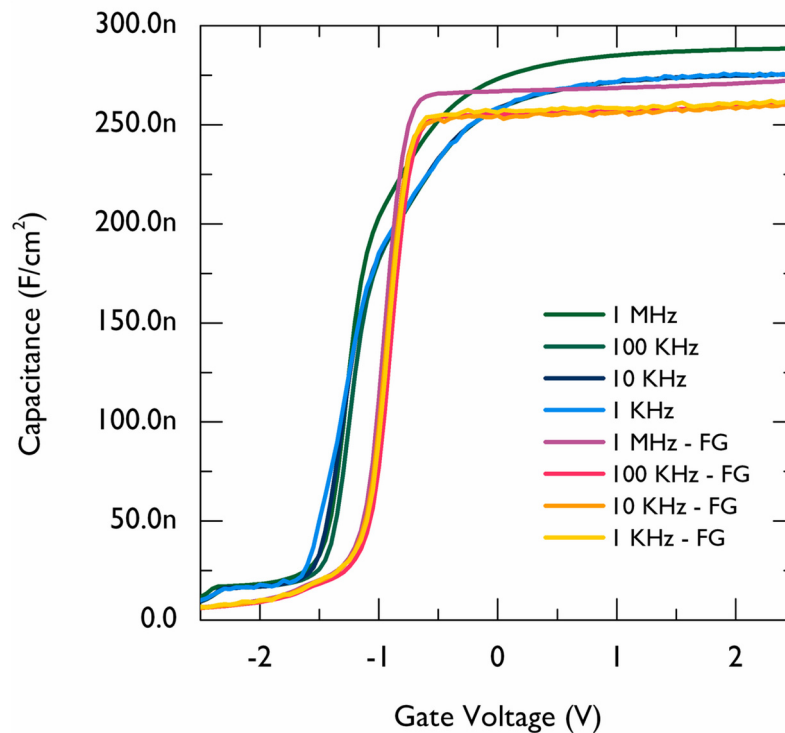


Figure 4-5: High frequency CV characteristics of a 100  $\mu m$  circular n-MOS capacitor measured between 1 MHz – 1 KHz before and after forming gas (FG) annealing.

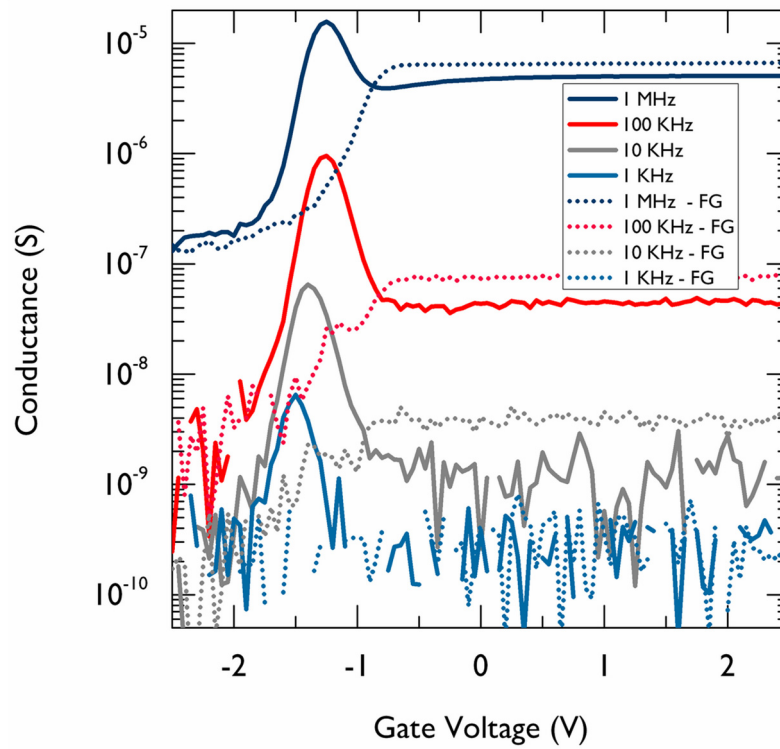


Figure 4-6: Conductance measurements performed before and after forming gas (FG) annealing on a 100  $\mu\text{m}$  circular n-MOS capacitor.

The contacts are annealed in forming gas (5%  $\text{H}_2$ , 95%  $\text{N}_2$ ) using a tube furnace pre-heated to a temperature of 360  $^\circ\text{C}$  for 15 minutes. Annealing alloys the Ni to form NiSi ohmic contact with a specific contact resistivity of  $1.5 \times 10^{-9} \Omega\text{-m}^2$ , which is determined from TLMs made on SOI substrate doped  $\sim 8 \times 10^9 \text{ atoms/cm}^3$  (TLM data in appendix 9.1). The quality of the oxide film and the effect of forming gas annealing has been determined from capacitance-voltage (CV) measurements performed on 100  $\mu\text{m}$  circular MOS capacitors fabricated on (100) crystal oriented n-type silicon substrate ( $N_D = 3.5 \times 10^{15} \text{ cm}^{-3}$ ) with  $\sim 10 \text{ nm}$  thermally grown  $\text{SiO}_2$ . Forming gas passivates the dangling bonds and trap charges with hydrogen atoms and lowers the interface state trap density ( $D_{it}$ ) [8]. The high frequency CV measurements performed between 1 MHz – 1 KHz are presented in figure 4-5 and 4-6. The results revealed the presence of mid-gap states in the thermally grown oxide with a large  $D_{it} = 2.3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  measured at 1 MHz (see figure 4-7). Here the  $D_{it}$  was extracted by using conductance method [9]. It was observed that after the forming gas annealing, the conductance peak at 1 MHz was smeared out, whereas small conductance peaks appeared between 100 KHz to 1 KHz. Since the conductance method is no longer valid in absence of a conductance peak,

therefore the  $D_{it}$  after the forming gas annealing was extracted at 100 KHz. The forming gas annealing reduced the  $D_{it}$  by over an order down to  $1.3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ . Moreover the oxide breakdown voltage was determined from ramped voltage technique which was  $\sim 7 \text{ V}$  (or  $7 \text{ MV/cm}$ ).

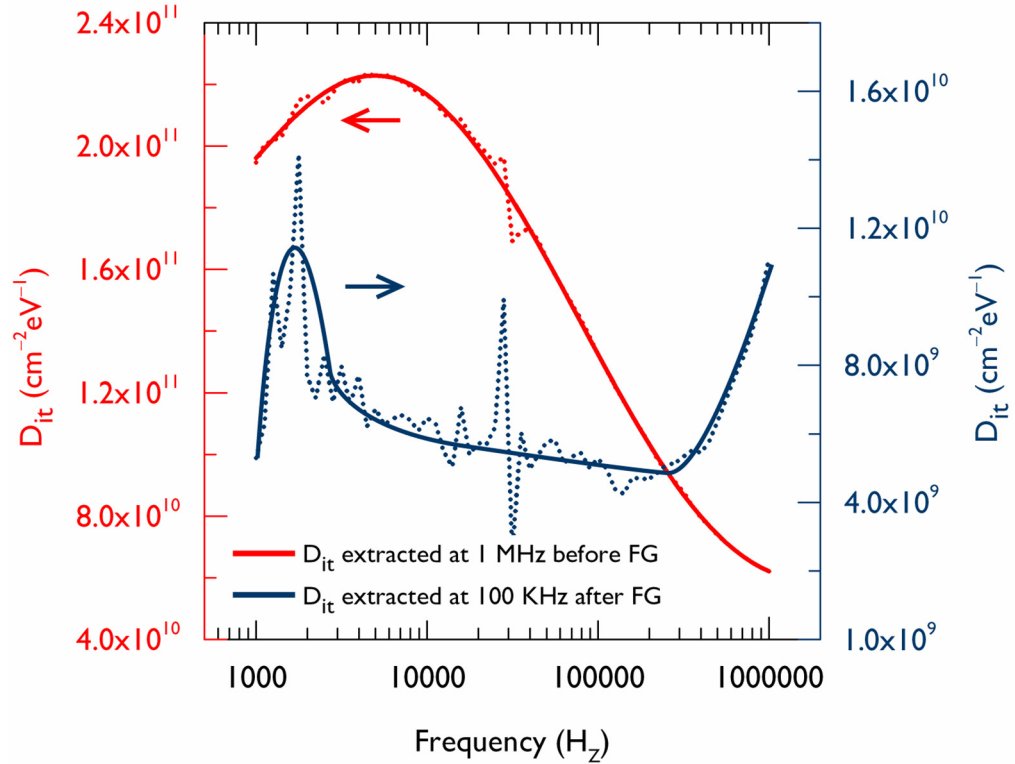


Figure 4-7: The  $D_{it}$  extracted using conductance method before and after FG annealing.

#### 4.1.5. Top Gate Metallization

A thick layer of aluminium  $\sim 400 \text{ nm}$  was deposited for both bond pads and wrap around gate using a lift-off process in two lithography steps. The lift-off process was optimized using PMMA resist discussed in section 2-3. The first lithography allows to deposit aluminium on Ni-Pt after the contacts are de-oxidized in solution of HCL diluted 1:4 with DI water for 30 seconds followed by rinsing in DI water for 1 minute. Similarly second lithography step allows to deposit aluminium over the grown thermal oxide to realize wrap around gate to modulate the silicon nanowire channel. Another layer of aluminium was also deposited on the back of the substrate to realize back gate operation. The Plassys-4 electron beam evaporator was used to deposit aluminium at  $4 \text{ nm/sec}$ .



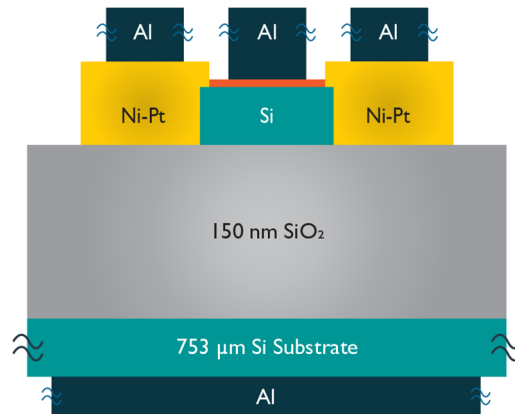


Figure 4-8: Illustration of depositing bond pads and wrap around gate.

## 4.2. Tools for Electronic Characterization

### 4.2.1. Semiconductor Parameter Analyser (DC Measurements)

The Agilent B1500 semiconductor parameter analyser allows to electronically characterize the devices using source monitor units (SMU's). The SMU's can either force the voltage or current to simultaneously measure the current or voltage and are capable of measuring the current down to  $\sim 10$  fA. SMU's are characterized into high power, medium power and high resolution and should be selected based on the required measurement. The Agilent B1500 is equipped with Cascade Microtech probe station to allow on-wafer measurements using micromanipulators having either single tip or kelvin probes.

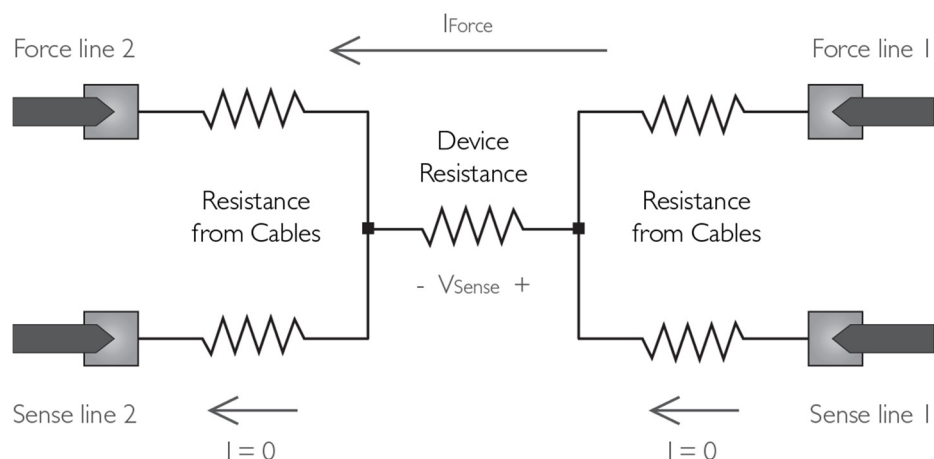


Figure 4-9: Illustration of kelvin probes for 4 terminal measurements.

The kelvin probes (shown in figure 4-9 [10]) are especially designed to eliminate the series resistance comes from the cables by separating the lines carrying the force and the sense, hence accurately measures the resistance across the device. The Agilent B1500 is also equipped with capacitance monitor units (CMU), high voltage pulse generator and waveform generator units to facilitate a diverse range of device characterization.

#### 4.2.2. Lock-in-Amplifiers (AC Measurements)

The major source of noise comes from the power lines operating at 50 Hz which can possibly superimpose noise through electromagnetic fields into the measurements. Whilst increasing the integration time may help to remove the noise but at the same time it can smear out the quantum effects of interest. For this work, Stanford research SR-830 DSP lock-in-amplifiers are used to take measurements onto the SETs and the Hall bar devices. Lock-in-amplifiers uses phase-sensitive-detection technique to accurately measures voltage or current. An AC signal excited at 77 Hz is superimposed onto the DC signal to apply either constant current or voltage to the device to measures voltage or current at that frequency within a bandwidth of a few hundred of millihertz. The time constant should be selected  $3 \times T$  (i.e. 30 ms for 77 Hz AC signal) to average the data value. A virtual instrument (VI) is programmed in LabView to record the data value from lock-in-amplifier to the computer, a delay of  $3 \times$  time constant (i.e. 90 ms) is applied in the VI to allow the data value to have adjusted to represent the actual value. In order to break any possible ground loops between different instruments connected together, the Stanford research SIM910 JFET voltage and SIM918 precision current pre-amplifiers are also used.

#### 4.2.3. Cryogenic Systems

Low temperature measurements allows to reduce the thermal energy ( $k_B T$ ) in order to probe the energy levels defined by the device physics. Most of the low temperature measurements in this work are taken on to the Oxford Instruments Teslatron, based on pulse tube refrigerator (PTR) which is a closed-cycle regenerative mechanical cryofree cooler. The block diagram of the Teslatron is shown in figure 4-10. It is integrated with a superconducting magnet and a variable temperature insert (VTI) to sweep the magnetic field up to 10 Tesla and temperature over a wide range from 1.4 to 300 K.

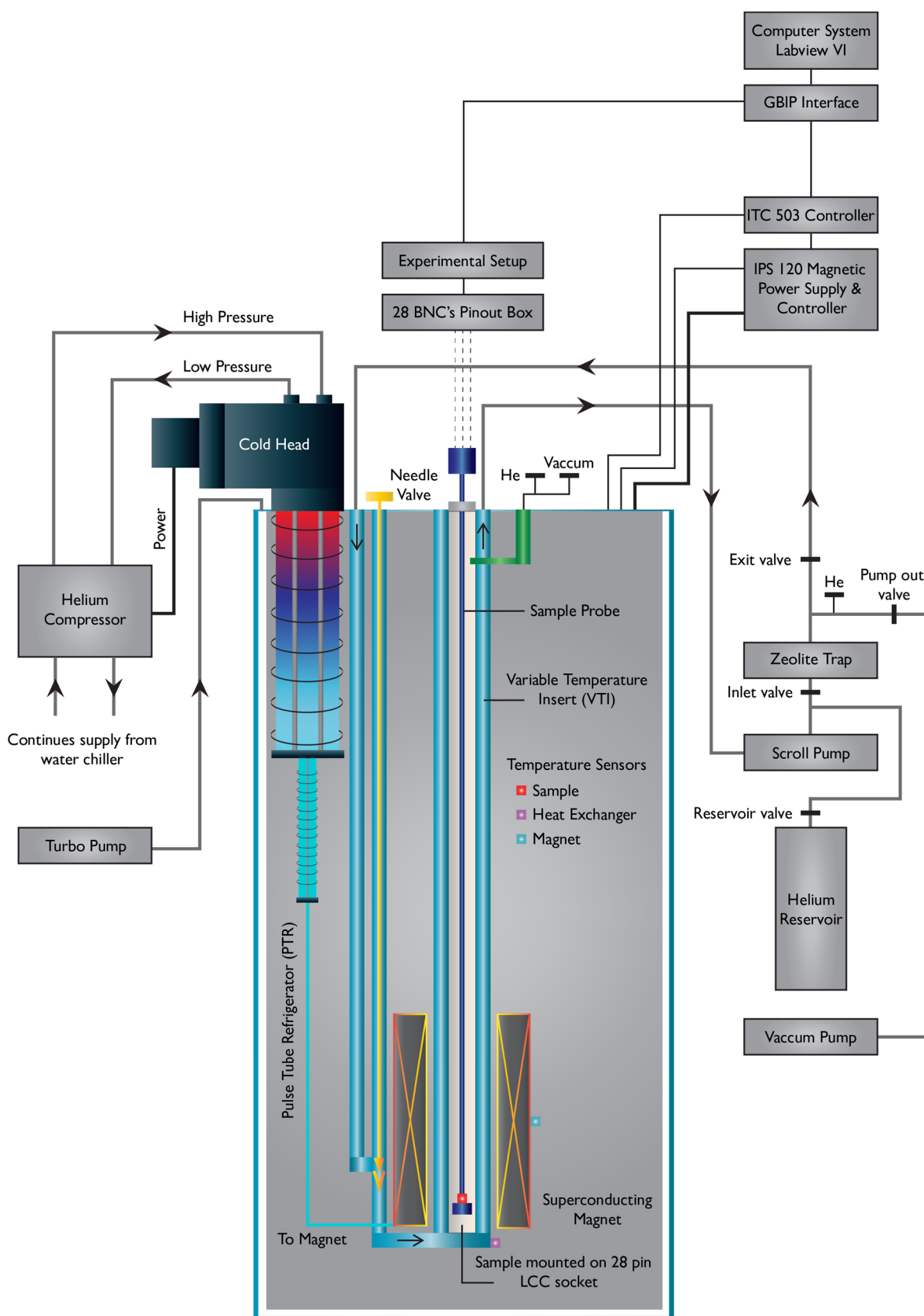


Figure 4-10: Schematic diagram of oxford instruments Teslatron.

The main components are PTR, VTI and superconducting magnet. The intelligent temperature controller (ITC) 503 monitors and controls the temperature of sample, heat exchanger and superconducting magnet whereas intelligent power supply (IPS) 120 is used to sweep on the magnet. These controllers can either be programmed through GBIP/ RS232 interfaces or used manually using Maglab measurement software. The Teslatron is cooled down to cryogenic temperatures by expansion of helium in a closed-cycle using PTR, consists of helium compressor, rotary valves, regenerator and cold head. The compressor uses 99.99% pure helium refrigerant and produces continuous high and low pressures, whereas rotary valves generates pressure oscillations to pump-in high pressure helium into the cold head where the regenerator takes out the further heat from the compressed helium and allows it to pass through the pulse tube which has cold and hot heat exchangers on its ends, after which the low pressure helium is pump-out of the system.

The compressor is connected to a closed-cycle water chiller and has a room temperature heat exchanger to remove heat from the low pressure helium and returns back high pressure helium to the cold head [11]. Assuming the complete system is pumped-out, the turbomolecular pump is turned on to achieve an ultimate low pressure  $\sim 7 \times 10^{-6}$  mbar, required to evacuate the empty space of the Teslatron. The gas handling components for the VTI consists of helium reservoir, circulation (scroll) pump, zeolite trap and a vacuum pump. A couple of purges of helium are required to push the air out of the gas lines meanwhile the scroll pump kept isolated and turned off. The helium from the main bottle is fed into the gas line through the zeolite trap to fill the helium reservoir up to  $\sim 1400$  mbar, the scroll pump is then turned on to circulate the helium in the VTI loop, this will eventually reduce the pressure of helium reservoir down to 1280 mbar. The helium is circulated for about 2 hours to scrub out all the moisture in the zeolite trap. Later, the zeolite trap is isolated from the loop and scroll pump is turned off to put the helium back into the helium reservoir. The zeolite trap is pumped out and baked for 24 hours in order to remove the moisture. At that point the helium compressor and the scroll pump is turned on to circulate helium in PTR and VTI loops respectively. The pressure of needle valve in VTI normally set to 20 mbar before Teslatron being set to cool down. The magnet is independently cooled down to 4 K via PTR and should not be operated above 6 K.

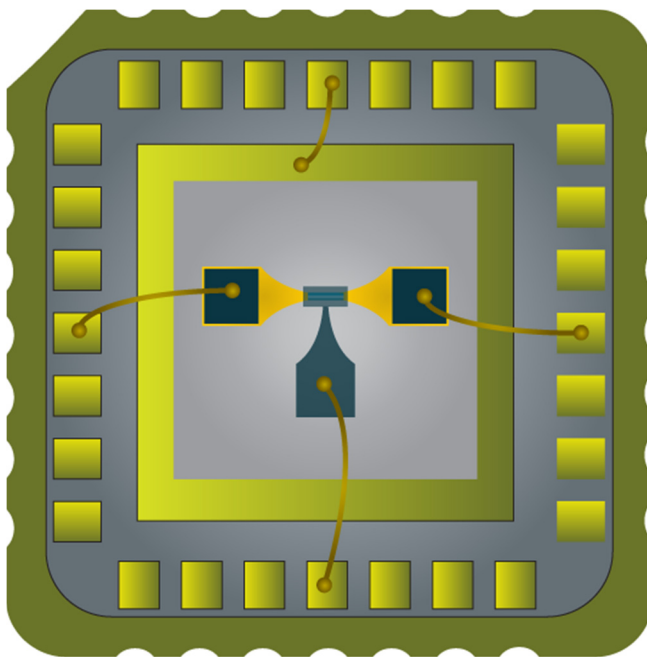


Figure 4-11: Illustration of device being bonded in 28 pin LCC header package.

The sample probe of the Teslatron has a 28 pin LCC live bug loading socket soldered to lemo connectors using cooper wires on the other end of the probe. The devices were bonded using gold wire wedge bonder on 28 pin LCC header packages shown in figure 4-11. These header packages were loaded onto the socket of sample probe and accessed using BNC pinout box (which has lemo-BNC connectors). The sample space in Teslatron was completely isolated from the VTI heat exchanger which allows to load the sample probe at any temperature. While loading or unloading the sample probe, the sample area should be supplied with a continuous helium just above 1000 mbar to keep a good thermal contact between the sample and the VTI heat exchanger [12].

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## 5. Electron Transport in Silicon Nanowires

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Understanding the electron transport properties of silicon nanowires is essential, since the recent development in nanowire technology has gained interest in potential applications in transistors [1], qubits [2], biosensors [3], thermoelectric generators [4] and color selective photodetectors [5], where majority of the applications are based on silicon material. A number of studies have investigated the effects of donor deactivation, surface roughness scattering [6] and noise [7] in silicon nanowires but being able to determine the carrier density directly rather than extracting it from the electrical conductivity which has been more of a challenge. Recently Hall effects measurements onto the InP nanowires are reported [8] but only carrier densities and mobilities have been extracted, whereas determining the performance limiting scattering mechanisms of nanowires are requisite to allow the high performance devices to be optimized for the wide range of applications. In this work, electron beam lithography and dry etch is used to fabricate silicon nanowires typically from 45 to 4 nm (mean widths) using top-down fabrication techniques in a Hall bar and Greek cross configuration with low LER, minimized plasma induced sidewall damages and high quality surface passivation ( $\text{SiO}_2$ ). Both of these devices allowed to directly extract resistivity, mobility and carrier density as function of temperature and enabled to identify major scattering mechanisms limiting the performance of silicon nanowires. The critical length scales are theoretically calculated and directly compared with widths of the nanowires, which demonstrates that the electron transport is likely to be changed from 3D for the 12 nm to 2D for 7 nm and 1D for 4 nm wide nanowires.

### 5.1. Device Physics

#### 5.1.1. Hall's Effect

Hall's effect was discovered by Edwin Hall in 1879, it describes the behaviour of the free charge carriers and accurately determines the resistivity, mobility and carrier density of any conducting material [9]. The whole idea is to apply a constant current ( $I_x$ ) to the conductor and measure the hall voltage ( $V_H$ ) across the conductor which is transverse to the current in the presence of magnetic field ( $B_z$ ) which perpendicular to the current. Figure 5-1 shows a 6 terminal Hall bar configuration. Assuming the conducting material is n-type semiconductor

where the electrons are in majority carrier, when current  $I_x$  flows through the material in  $x$  direction, the charge particles i.e. electrons (with charge  $-q$ ) moves towards  $-x$  direction with drift velocity ( $V_x$ ) which is on opposite side of the conventional current. In presence of magnetic field in  $z$  direction, there will be Lorentz force acting upon the electrons in  $y$  direction given by,

$$F_y = -q (V_{-x} \times B_z)$$

The electrons start deflecting towards the top side whereas the holes towards the bottom side of the semiconductor, thus separating the charge particles. The piling up of electrons give rise to the potential difference and as a result electric field ( $F_e$ ) increases which is given by,

$$F_e = -q E_{-y}$$

Where  $E_{-y}$  is given by,

$$E_H = \frac{V_H}{w}$$

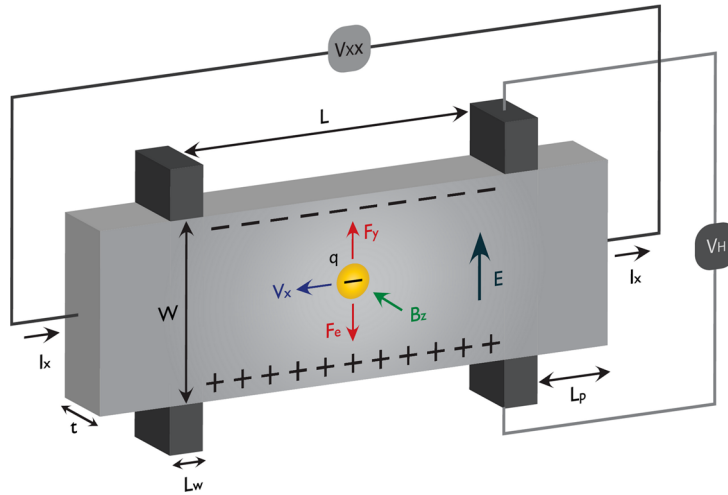


Figure 5-1: Illustration of 6 terminal Hall bar device configuration.

At some point the electric field reaches the magnitude of the magnetic field, thus both forces  $F_y$  and  $F_e$  balances out each other and the semiconductor will reach in a steady state equilibrium state where there will be no net force on to the carriers. This is given by,



$$V_x B = \frac{V_H}{w}$$

The drift velocity,  $V_x$  can be written in form of total current ( $I_x = -qnV_xwt$ ) to workout Hall voltage ( $V_H$ ) from the above equation,

$$V_H = - \frac{I_x B_z}{q n t}$$

Where  $t$  is the thickness of the semiconductor. The Halls coefficient ( $R_H$ ) is given by,

$$R_H = \frac{V_H t}{I_x B_z} = - \frac{1}{q n} \quad (\text{Eq. 5.1})$$

From the Halls coefficient, the carrier density ( $n$ ) of the semiconductor can be calculated. Whereas in order to determine the mobility, the conductivity can be written in terms of mobility as,

$$\sigma = - nq\mu$$

By rearranging this, the mobility ( $\mu$ ) is given by,

$$\mu = R_H \sigma \quad (\text{Eq. 5.2})$$

Where the conductivity ( $\sigma$ ) is,

$$\sigma = \frac{1}{\rho} = \frac{I_x L}{V_{xx} w t} \quad (\text{Eq. 5.3})$$

Some geometrical considerations must be accounted before designing the Hall bar devices to minimize the error percentage in determining the mobility and carrier density. These considerations minimizes the Hall voltage shorting effects to determine the true Hall voltage [10,11].

$$\frac{L_s}{w} \geq 3, \quad L_w \leq \frac{w}{3}, \quad \frac{L_p}{w} > 1 \text{ or } L_p > \frac{1}{4} \frac{L_s}{w} \text{ and } L \geq 4w$$

$$\text{Where } L_s = 2L_p + L$$

### 5.1.2. Characteristic Length Scales and Transport Regimes

The electronic transport mechanisms in semiconductors/metals are defined in terms of transport regimes, various characteristic length scales and scattering mechanisms. Some of the length scales are given below [12] which defines the different transport regimes,

**Inelastic scattering length ( $l_{in}$ ):** The length an electron travels without any change in its kinetic energy. The collisions such as electron-electron and electron-phonon are as a result of inelastic scattering events. It is defined as,

$$l_{in} = v_F \tau_\varphi$$

Where  $v_F$  is the Fermi velocity and  $\tau_\varphi$  is inelastic scattering time.

**Elastic scattering length ( $l_e$ ):** The length an electron travels without change in its wave vector. The collisions between electrons and fixed Coulombic impurities are an example of elastic scattering events. It is defined as,

$$l_e = v_F \tau$$

**Phase coherence length ( $l_\varphi$ ):** The length an electron travels before initial phase of the wave function is disrupted by some scattering event. The scattering length ( $l_\varphi$ ) associated with scattering time ( $\tau_\varphi$ ) is linked through the diffusion constant  $D$  given by,

$$l_\varphi = \sqrt{D \tau_\varphi}$$

**Electric length ( $l_F$ ):** The length scale due to electric field ( $F$ ) is

$$l_F = \left( \frac{D\hbar}{qF} \right)^{1/3}$$

**Magnetic length ( $l_B$ ):** The length scale due to magnetic field ( $B$ ) is

$$l_B = \sqrt{\frac{\hbar}{qB}}$$

**Thermal length ( $l_t$ ):** The length scale due to thermal motion of carriers is

$$l_t = \sqrt{\frac{\hbar D}{k_B T}}$$

**Mean free path ( $l$ ):** The minimum length an electron travels between successive scattering events. Elastic scattering length is the shortest of all other lengths scales, hence defines the mean free path as [13]

$$l = v_F \tau = \frac{\hbar k_F}{m^*} \tau$$

Where  $k_F$  is a Fermi wavenumber. For specific 3D, 2D and 1D transport, the mean free path is defined as,

$$l_{3D} = \frac{\hbar \mu}{q} k_{F\ 3D} = \frac{\hbar \mu}{q} \left( 3\pi^2 \frac{n}{g_v} \right)^{1/3} \quad (\text{Eq. 5.4})$$

$$l_{2D} = \frac{\hbar \mu}{q} k_{F\ 2D} = \frac{\hbar \mu}{q} \sqrt{2\pi \frac{n}{g_v}} \quad (\text{Eq. 5.5})$$

$$l_{1D} = \frac{\hbar \mu}{q} k_{F\ 1D} = \frac{\hbar \mu}{q} \pi \frac{n}{g_v} \quad (\text{Eq. 5.6})$$

Where  $g_v = 2$  is the valley degeneracy and  $g_s = 2$  is the spin degeneracy of the semiconductor material.

**3D Fermi wavelength ( $\lambda_F$ ):** The majority of the electron transport is due to the electrons near the Fermi level, so the appropriate length scale to consider these electrons is 3D Fermi wavelength which is given by [13]

$$\lambda_F = \frac{2\pi}{k_F} = 2\pi \left( \frac{g_v}{3\pi^2 n} \right)^{2/3} \quad (\text{Eq. 5.7})$$

**Debye length ( $L_D$ ):** The length scale over which the charge separation can occur. Debye length limits the electrostatic interaction between charged particles. It is defined as,

$$L_D = \sqrt{\frac{\epsilon_r \epsilon_0 V_T}{q N_D}} = \sqrt{\frac{\epsilon_r \epsilon_0 k_B T}{q^2 N_D}} \quad (\text{Eq. 5.8})$$

Where  $\epsilon_r$  is the relative permittivity of a material,  $\epsilon_0$  is the permittivity of a vacuum,  $V_T$  is the thermal voltage,  $k_B$  is the Boltzman constant,  $T$  is the temperature,  $q$  is an electron charge and  $N_D$  is the carrier density.

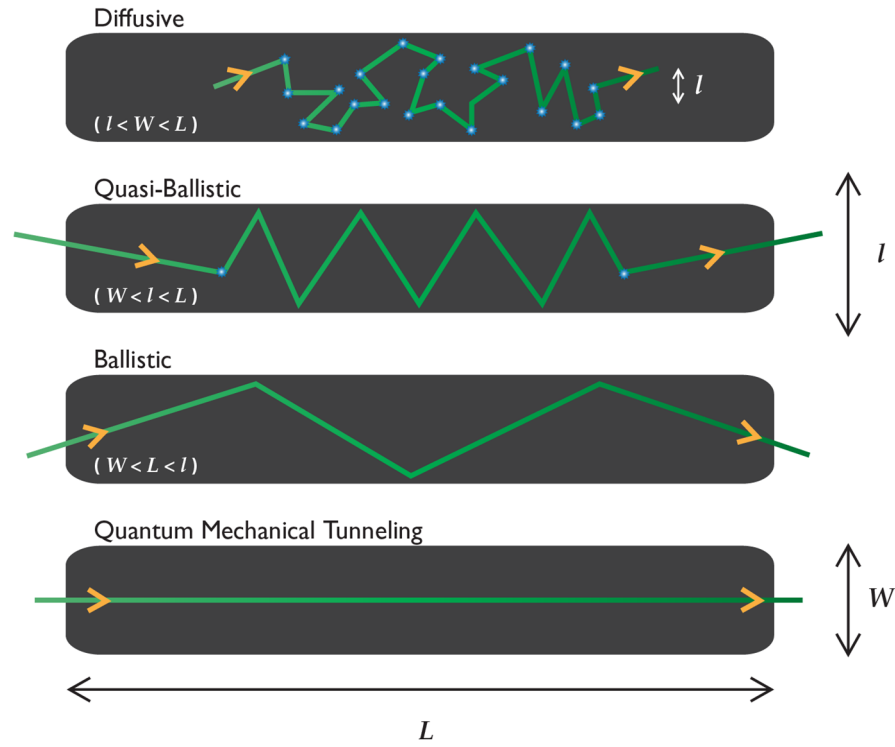


Figure 5-2: Illustration of transport regimes in nanostructures.

**Transport Regimes:** Based on some of these length scales, if we consider an active channel with dimensions length ( $L$ ) and width ( $W$ ), then electrons can have four distant transport regimes. These are illustrated in figure 5-2 [14] and defined on the basis of mean free path ( $l$ ) and dimensionality. The transport regime is diffusive where the length and width of the channel is larger than the mean free path ( $l$ ) of electrons and is dominated by scattering events (shown by blue asterisks). In quasi-ballistic regime the mean free path is larger than the width

of the active channel but smaller than the length, in this case only a few scattering events takes place and the transport is mostly quantized in one whereas diffusive in other dimensions. In ballistic regime the mean free path is larger than both length and width and electrons are not scattered within the channel.

### 5.1.3. Scattering Mechanisms

The electrons/holes travelling through a channel undergo a variety of interactions with the semiconductor material and the nature of those interactions can be determined from the mobility of the channel. Whilst mobility for any absolute temperature  $T$  can be calculated from Einstein relation (5.9) but it does not provide any further information to determine any specific scattering mechanism, limiting the performance of the channel.

$$\mu = \frac{qD}{k_B T} \quad (\text{Eq. 5.9})$$

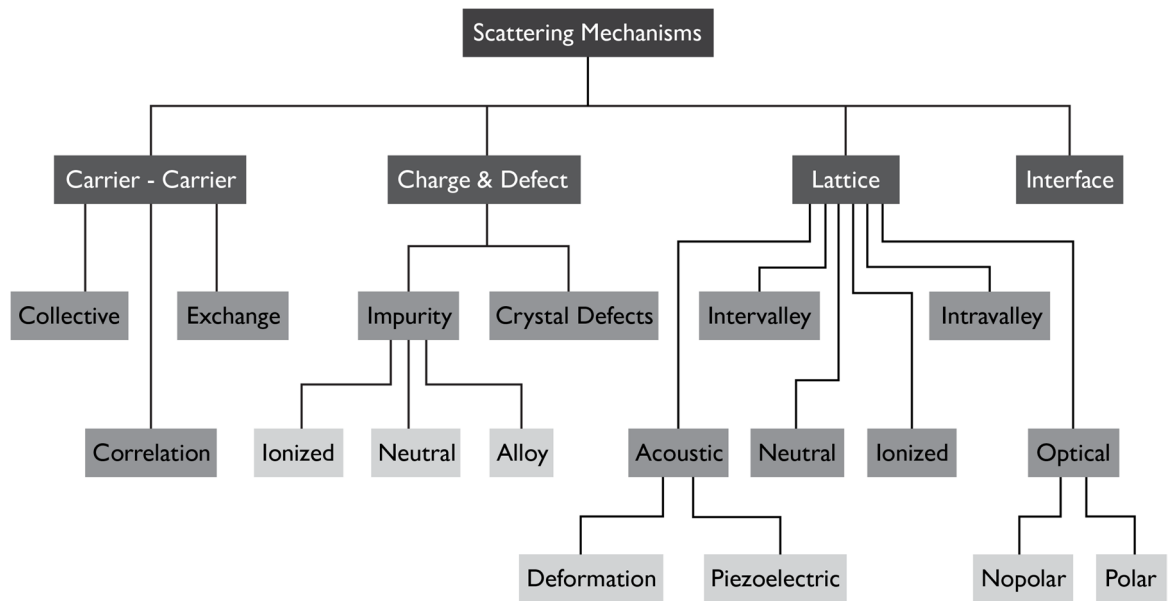


Figure 5-3: Scattering mechanisms in semiconductors.

Some of the scattering mechanisms in semiconductors are listed in figure 5-3 [18]. In degenerately doped semiconductors, Fermi level will be inside the conduction band of the channel and to account this into the calculations, the effective mass ( $m^*$ ) defined to include a non-parabolicity factor as,

$$m^* = m_c^* \left[ 1 + 2C \frac{\hbar^2}{m_c^*} \left( \frac{3\pi^2 n}{g_v} \right)^{2/3} \right] \quad (\text{Eq. 5.10})$$

Where  $m_c^*$  is the conductivity effective mass defined as,

$$m_c^* = 3 \left( \frac{1}{m_l} + \frac{2}{m_t} \right)^{-1}$$

The values of longitudinal electron mass is  $m_l = 0.98m_0$  and transverse electron mass is  $m_t = 0.198m_0$ , where  $m_0$  is the free electron mass,  $n$  is the carrier density,  $g_v = 2$  is the valley degeneracy of conduction band and  $C = 0.5 \text{ eV}^{-1}$  is nonparabolicity parameter [15].

### 5.1.3.1. Acoustic Phonon Scattering

The acoustic phonon scattering mechanism based on lattice vibrations as a result of a potential shift known as deformation potential. The deformation potential is due to phonon induced strain in the material which disrupts the band structure as a result of change in the crystal potential which in turn changes the lattice spacing, hence varies the lattice constant. This scattering mechanism is due to the collective vibration of the atoms in the lattice about their equilibrium positions [16]. For degenerative semiconductors, the acoustic phonon scattering has quasi-elastic characteristics and has a small acoustic phonon energy which result in a small wave vector change and due to reservation of momentum, the scattering mechanism limits the acoustic phonon to long wavelength range [17]. The mobility due to acoustic phonon scattering defined in terms of deformation potential which depends on temperature and electron density is defined as [18]

$$\mu_{ac} = \frac{16\sqrt{2}\pi c_L \hbar^4 q}{3\Xi_{ac}^2 m^{*5/2}} (k_B T)^{-2/3} \quad (\text{Eq. 5.11})$$

$$c_L = c_{12} + 2c_{44} + \frac{1}{3} (c_{11} - c_{12} - 2c_{44}) \quad [19]$$

Where  $c_L$  is averaged longitudinal elastic modulus and values of elastic constants are  $c_{11} = 165.77 \text{ GPa}$ ,  $c_{12} = 63.93 \text{ GPa}$  and  $c_{44} = 79.62 \text{ GPa}$  and acoustic deformation potential  $\Xi_{ac} = 8.6 \text{ eV}$  [20]

### 5.1.3.2. Optical Phonon Scattering

The optical phonon scattering is generally due to the relative displacement of atoms within a unit cell caused by deformation potential [17]. Optical phonon energy is higher than thermal energy of electron at room temperature, so after a collision electron losses most of its energy and result in an inelastic scattering process. Whereas at low temperatures typically below 100 K, the electrons do not emit optical phonons due to low thermal energy. So, optical phonon scattering is dominant at room and negligible at low temperature.

In this particular work optical phonon scattering model of Hamaguchi [18,21] is used since it allows all temperature to be considered. The mobility due to optical phonon scattering calculated using,

$$\mu_{op} = \frac{4\sqrt{2\pi} q\hbar^4 \sqrt{\hbar\omega_{LO}}}{3\Xi_{op}^2 m^{*5/2}} f(z_0) \quad (\text{Eq. 5.12})$$

Where LO optical deformation potential between  $\Delta$ -valleys defined as  $\Xi = 11.0 \times 10^{10} \text{ eV/m}$  [15] and LO optical phonon energy,  $\hbar\omega_{LO} = 63 \text{ meV}$  and  $\rho = 2329 \text{ kg m}^{-3}$  is density of silicon. Also  $f(z_0)$  is given by,

$$f(z_0) = z_0^{5/2} (e^{z_0} - 1) \int_0^\infty z e^{-z} \frac{1}{\left(1 + \frac{z_0}{z}\right)^{1/2} + e^z \left(1 - \frac{z_0}{z}\right)^{1/2}} dz$$

$$z_0 = \frac{\hbar\omega_{LO}}{k_B T} \text{ and } z = \frac{E}{k_B T}$$

Where  $E$  is the energy under consideration for phonons.

### 5.1.3.3. Ionized Impurity Scattering

The ionized impurity scattering is due to the presence of charged impurity atoms in the semiconductors after being doped. The scattering is as a result of coulomb potential produced by the ionized impurity atoms. In degenerately doped semiconductors, the probability of carriers being scattered by ionized impurity atoms increases as increase in the doping density and becomes a dominant scattering mechanisms limiting the mobility. At low temperatures, the

carriers slows down due to low thermal velocity and are subject to spend longer time in the vicinity of ionized impurities, hence increases the probability of being scattered more strongly by Coulombic interaction forces as compared at high temperatures.

The expression for mobility due to ionized impurity scattering is given by [18],

$$\mu_I = \frac{24\pi^3 \epsilon_0^2 \epsilon_r^2 \hbar^3 n}{N_I Z^2 q^3 m^{*2} \left[ \ln(1 + \gamma_F) - \frac{\gamma_F}{1 + \gamma_F} \right]} \quad (\text{Eq. 5.13})$$

Where  $\epsilon_0$  is the permittivity of vacuum,  $\epsilon_r = 11.9$  is the relative dielectric constant of silicon and  $Z = 1$  is the charge on the donor and  $\gamma_F$  is given by,

$$\gamma_F = \frac{4\sqrt[3]{3} \epsilon_0 \epsilon_r \pi^{8/3} \hbar^2 n^{1/3}}{q^2 m^*}$$

The ionized donor concentration is defined as,

$$N_I = \frac{N_D}{1 + g_D \exp\left[\frac{E_F - E_D}{k_B T}\right]}$$

Where  $g_D = 2$  for the phosphorus donor,  $N_D$  is the doping density and  $E_D$  is the donor activation energy.

#### 5.1.3.4. Neutral Impurity Scattering

The neutral impurity scattering is generally accompanied by other impurity and lattice scattering mechanisms. It becomes a dominant scattering mechanism especially at low temperatures where ionized impurities become neutral due to carrier freeze out and conduction electrons no longer emit photons due to low thermal energy [22].

The mobility due to neutral impurity scattering is given by [23],

$$\mu_{NI} = \frac{m^* q^3}{20 \epsilon_0 \epsilon_r (N_D - n) \hbar^3} \quad (\text{Eq. 5.14})$$

Where  $N_D - n$  determines the density of neutral impurities in the semiconductor.



### 5.1.3.5. Interface Roughness Scattering

The interface roughness scattering due to the scattering of carriers by the roughness of the semiconductor interfaces. If the surface roughness is comparable to the de Broglie wavelength, then this scattering mechanism becomes significant [18]. The interface is modelled to determine the mobility due to interface roughness scattering [24] is based on Gaussian-type autocorrelation for an interface roughness height of  $\Delta$  and lateral correlation length of  $\Lambda$ . A Gaussian model was chosen as it has demonstrated better fits to the experimental mobility in quantum well devices without a vertical electrical field, whilst the exponential model used in MOSFETs has demonstrated superior descriptions of mobility under large vertical electrical fields [25]. The mobility due to interface roughness scattering is defined as

$$\mu_{IRS} = \frac{q\hbar^3 k_F}{2m^2 \sqrt{\pi} \Lambda \Delta^2 |\Gamma|^2} \exp k_F^2 \Lambda^2 \quad (\text{Eq. 5.15})$$

Where the confinement assumed to be a potential well of width  $w$ , producing a scattering rate  $\Gamma$  given by,

$$\Gamma = \frac{\hbar^2 \pi^2}{mw^3}$$

## 5.2. Device Fabrication and Experimental Setup

In order to investigate the electron transport properties of silicon nanowires, Hall bar and Greek cross devices are fabricated with mean widths from 45 – 4 nm. The device fabrication techniques are discussed in detail in section 4.1. Patterning nanowire devices are more challenging than patterning isolated nanowires, because the bond pads accessing the nanowire can bring in proximity effects which often result in widening of the nanowire channel. For both kind of devices, the layout for the pattern transfer is designed to get three different electron beam exposures, i.e. the nanowire channel (layer 1), nanowire connecting smaller bond pads  $\sim 2.25 \mu\text{m}^2$  (layer 2) which ultimately joins larger bond pads  $\sim 400 \mu\text{m}^2$  (layer 3) to add ohmic contacts to the devices. This allows to write nanowire channel with smallest beam diameter and beam step size (BSS) to minimize line edge roughness (LER) and the bond pads to a relatively larger beam diameter with low doses to minimize proximity effects. The electron beam

exposure parameters used for the pattern transfer of the Hall bar and Greek cross devices are shown in table 5-1. Following the lithography, the devices are etched, oxidized and metalized as discussed in section 4.1.

	Dose ( $\mu\text{C cm}^{-2}$ )		Beam step size (nm)	Spot size (nm)
	HBD	GCD	HB & GC Devices	HB & GC Devices
Layer 1	2500	4700	2.5	3
Layer 2	2000	2500	5	3
Layer 3	1800	1800	25	33

**Table 5-1: Electron beam exposure parameters used for pattern transfer of the Hall bar and Greek cross devices.**

The SEM images of fabricated Hall bar and Greek cross devices are shown in figure 5-4. In this work, Hall bar devices are used to extract mobility whereas Greek cross devices for carrier density. These devices are made on the samples from four different SOI wafers. The activated dopant density of four wafers were  $2 \times 10^{19}$ ,  $4 \times 10^{19}$ ,  $8 \times 10^{19}$  and  $20 \times 10^{19} \text{ cm}^{-3}$  measured from large area Hall bar devices. Figure 5-5 shows cross sectional transmission electron microscopy (TEM) images of final devices with lithographic widths 10, 15, 20 and 25 nm (from left to right).

The thickness of  $\text{SiO}_2$  oxide is  $\sim 4 \text{ nm}$  determined from the capacitance-voltage measurements (shown in figure 4-5) which is also confirmed from the TEM images. There is clear footing revealed from the TEM images due to RIE and enhanced oxidation rates at the top edges of the nanowire, figure 5-5a shows the smallest made nanowire with top section as small as 1.9 nm whilst the bottom is 10.7 nm, whereas similar effects are observed with other nanowires as well. Therefore widths quoted throughout the thesis are the mean widths determined from ten cross sectional measurements of the physical width of silicon over ten equally spaced positions in height of the nanowire. Whilst it defines the width of the smallest nanowire  $\sim 4 \text{ nm}$  but it's believed that the majority of the transport will be dominated by the wider 10.7 nm bottom foot.

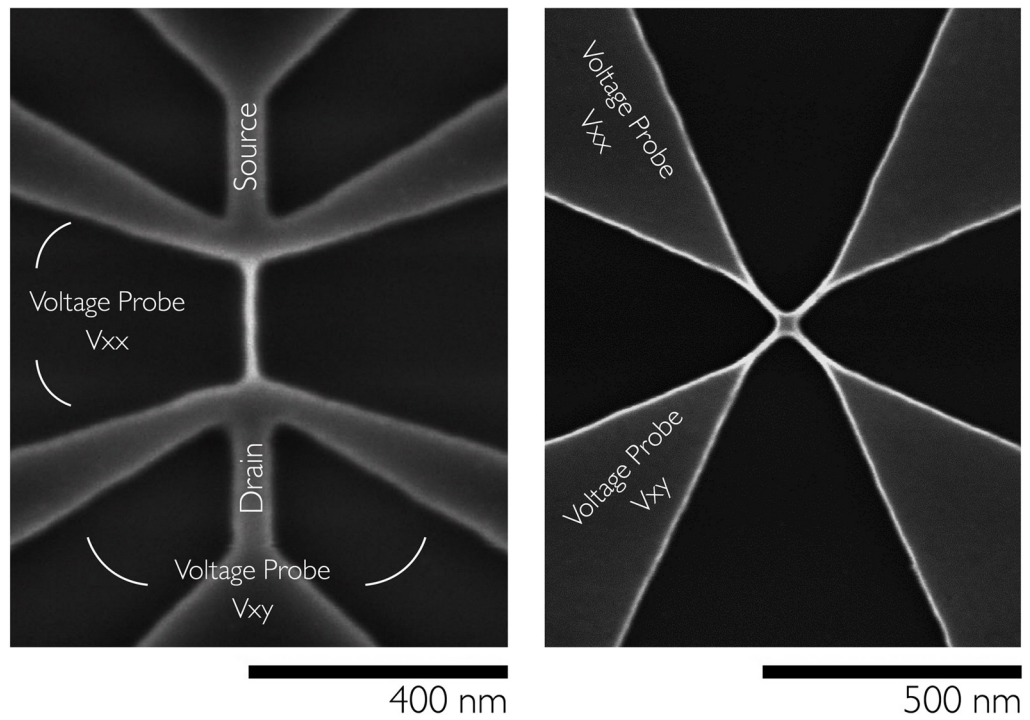


Figure 5-4: SEM images of 4 nm (mean width) Hall bar (left) and Greek cross (right) devices etched on SOI substrate.

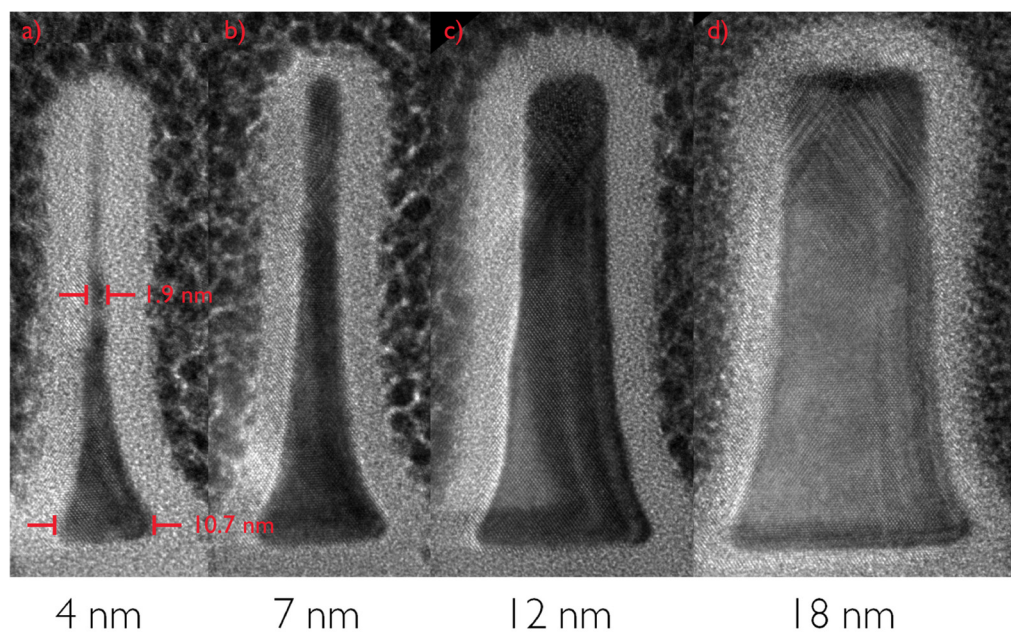


Figure 5-5: Cross-sectional TEM images of thermally oxidized silicon nanowires fabricated on SOI substrated labelled with mean widths.

The experimental setup used to probe Hall bar and Greek cross devices is shown in figure 5-6. AC (alternating current) constant current measurement technique is used to minimize electron heating in the nanowire channel for which Agilent 33521A arbitrary waveform generator source and Stanford Research SR-830 lock-in amplifiers are used. 1 V at 77 Hz is generated across a 10 M $\Omega$  resistor to provide  $\sim 100$  nA constant current to the nanowire channel, whereas a calibrated 1 K $\Omega$  resistor at the output is used to determine the constant current during the measurements. Separate lock-in-amplifiers are used to record  $V_{xx}$ ,  $V_{xy}$  and  $V_{out}$  simultaneously. Temperature dependent characteristics of nanowires are measured using Oxford Instruments Teslatron cryostat with variable temperature insert (VTI) and 12 T magnet. All these instruments were accessed and controlled using a LabView's virtual instrument (VI) program connected to the computer via GBIP interfaces.

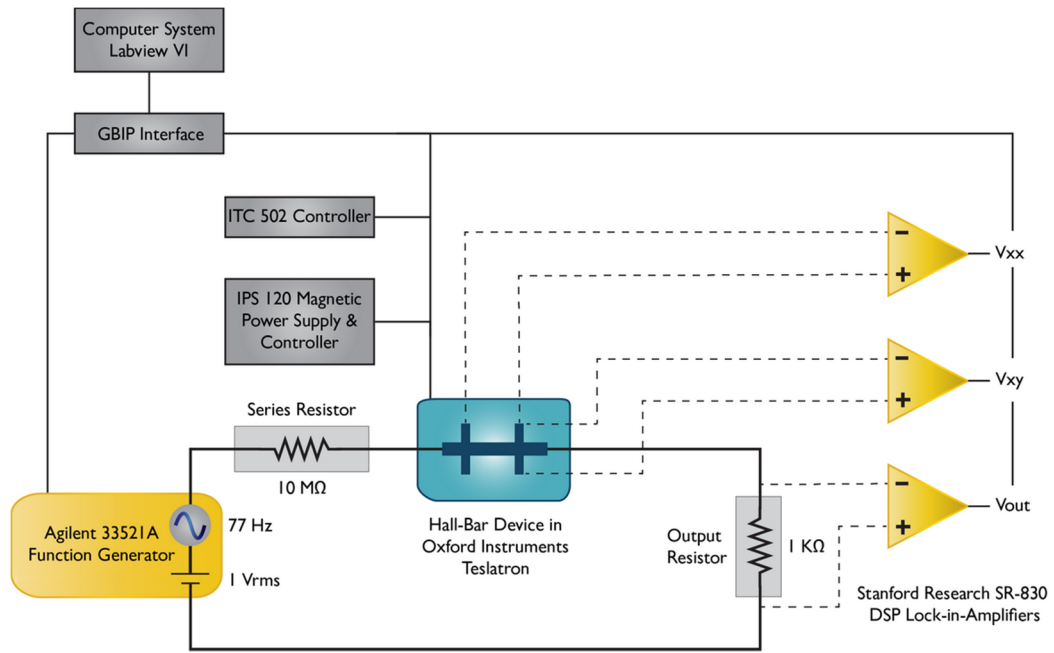


Figure 5-6: Experimental setup to probe Hall bar and Greek cross devices.

### 5.3. Results & Discussions

The DC measurements are performed onto the both types of fabricated devices using Agilent B1500 parameter analyser before temperature dependent AC measurements are performed under cryostat. For clarity, results for the nanowires fabricated on SOI substrate with a doping density below  $2 \times 10^{19} \text{ cm}^{-3}$  are not included for the analysis, because of poor or no conductivity for the nanowires with widths below  $\sim 30$  nm. Results from the  $N_D = 2 \times 10^{19}$

$\text{cm}^{-3}$  indicated that the doping was still not sufficient for the nanowires below  $\sim 12$  nm. Even for 12 nm wide nanowires, non-linear I-V characteristics are observed with a large energy gap of  $\pm 0.4$  V shown in figure 5-7 (red). These non-linear I-V characteristics are similar to those reported for Coulomb blockade and single electron tunnelling at lower temperatures [26], whilst this has not been probed further but there is significant possibility that the combination of depletion and sidewall roughness reduced the nanowire channel into number of small islands of charge through which electrons might have been tunnelling, however further work is required to exactly determine if the device has a Coulomb gap or a non-linear behaviour as a result of Schottky barriers at the source/drain end of the channel. Ohmic conduction has been observed for the nanowires with widths down to 7 nm and non-linear conduction for the smallest 4 nm nanowire fabricated on  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$ , but to significantly enhance the reproducibility and reliability, the doping density is further increased.

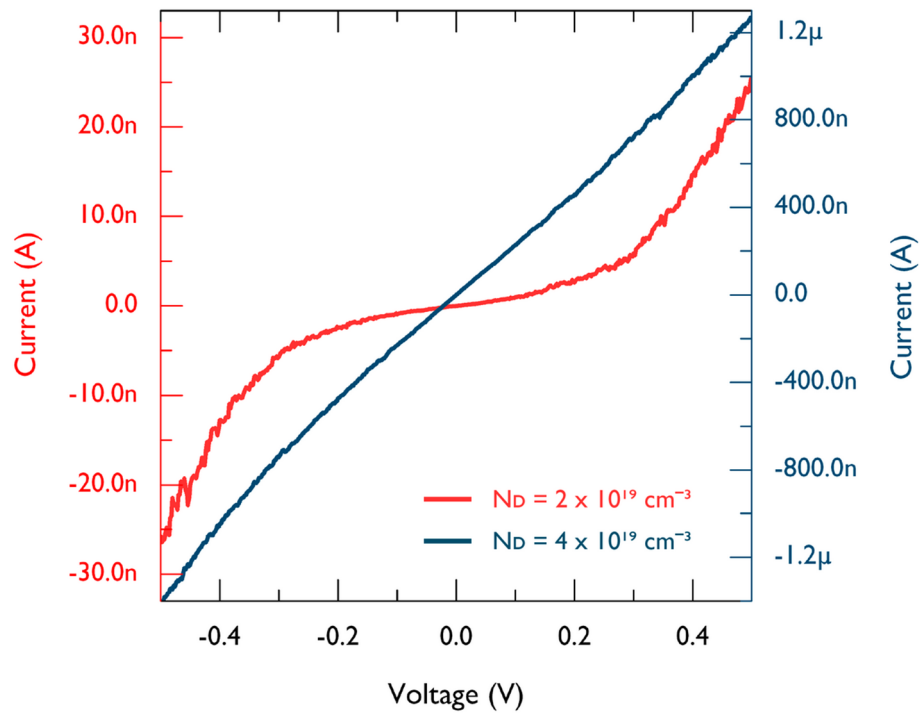


Figure 5-7: I-V characteristics of 12 nm (red) and 7 nm (blue) silicon nanowires with different doping densities.

The electrical resistivity as function of nanowire width for different doping densities is shown in figure 5-8. Here the resistivity has been measured from the two terminals of the Hall bar devices. The geometry of the Hall bar devices are designed in a way to lower the contact and access resistances which are negligible as compared to the resistance of the nanowires.

Hence there is only a small difference observed between the two and four terminal resistance measurements, this has been shown in appendix 9.1. From resistivity plot it's clear that for  $N_D = 2 \times 10^{19} \text{ cm}^{-3}$  all the nanowires tends to have significant depletion effects and the resistance of nanowires below 12 nm is as high as 100 M $\Omega$ , indicating the insulating behaviour demonstrating that the nanowire channel is completely depleted out of carriers. Whereas for  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$  the depletion effects became significant in nanowires below 18 nm and the smallest 4 nm nanowire have similar insulating properties. Only the nanowires fabricated on  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$  and above, haven't demonstrated any depletion effects and could potentially be used to examine electrical properties of the nanowires.

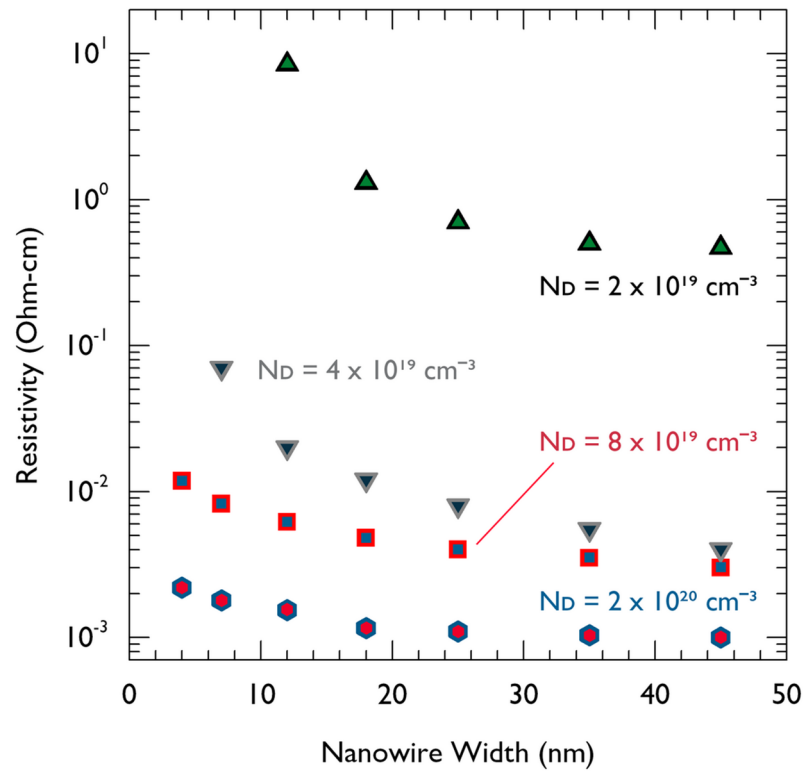


Figure 5-8: Resistivity as function of nanowire width for different doping densities.

Figure 5-9 shows the electrical resistivity as function of temperature extracted from four terminals of the Hall bar devices. It is observed that the wider nanowires had strong metallic connectivity which was expected since the doping densities is significantly above the Mott criterion [27] for Si:P of  $3.5 \times 10^{18} \text{ cm}^{-3}$  whereas the 4 nm nanowire behaved differently at high temperatures suggesting that the depletion of the conducting part of the channel may have reduced the dimensionality for the electron transport to 1D.

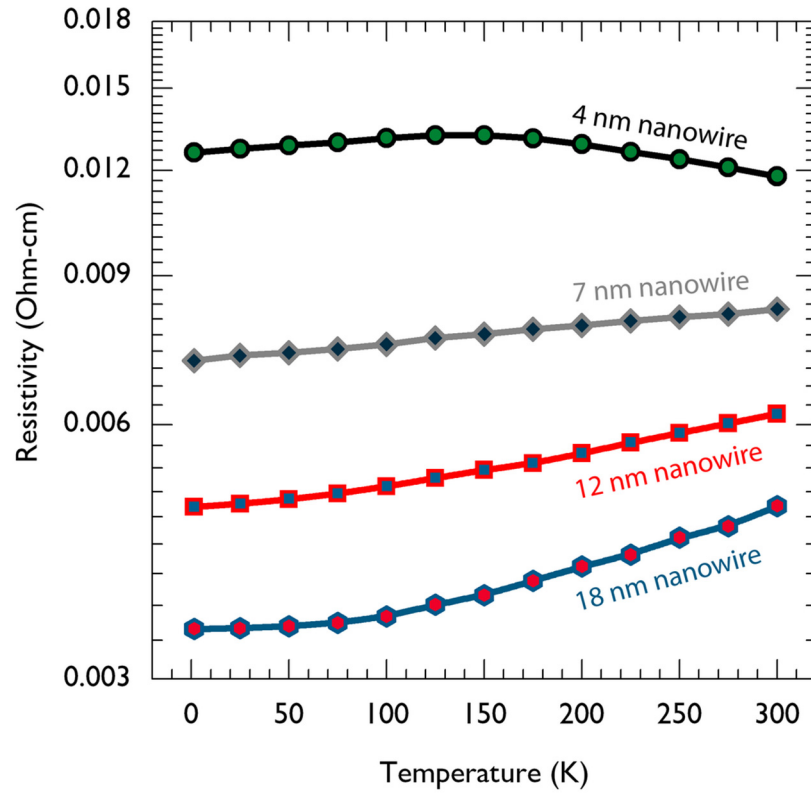


Figure 5-9: Four terminal resistivity measured for the devices fabricated on  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$  as a function of temperature.

The extraction of carrier density and mobility requires to measure the Halls voltage generated in the nanowires which is independent of the cross sectional geometry of the nanowire. The accuracy of the Halls measurements relies on the width the voltage probes rather than the width of the nanowire channel, for the nanowires with widths below 20 nm, the proximity effects result in widening of the nanowire, voltage probes and their junctions, hence limits the accuracy of any extracted Hall voltage. Whilst smaller voltage probes are desirable to determine true Hall voltage but wider voltage probes allows to minimize the access resistance to prevent any electron heating. Since the doping densities of the nanowires devices is considerably very high, the resulting Hall voltage is extremely small and orders of few  $\mu\text{V}$ . The geometrical uncertainty from [10] in measuring the carrier density from the Halls effect in fabricated Hall bar devices with widths below 20 nm provides a value accurate within a factor of 2 of the true Hall voltage. For these reasons the Greek cross devices are fabricated which allowed to measure the carrier density by the Hall's effect with geometrical uncertainty below 1% even for the 7 nm nanowire. Whereas due to larger uncertainty in 4 nm nanowire, the results are only be estimated to be accurate within a factor of 2.

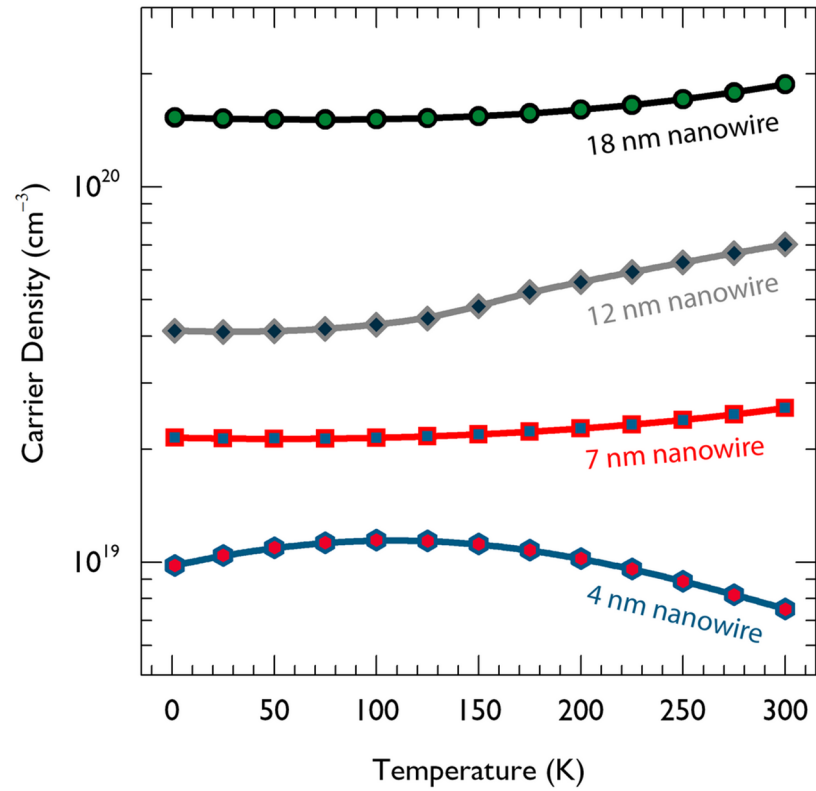


Figure 5-10: Extracted carrier density of nanowires as function of temperature.

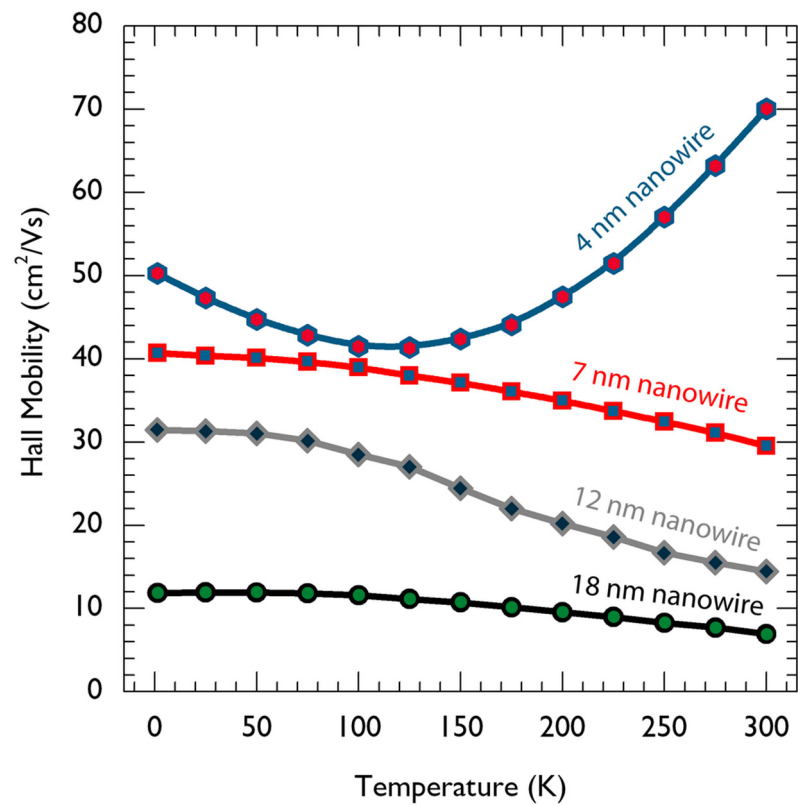


Figure 5-11: Extracted Hall mobility of nanowires as function of temperature.



In this work, Hall voltage was extracted by applying a linear fit to the data obtained by sweeping the magnet from  $-1$  T to  $1$  T which can potentially remove any stray field effects. The results from both Hall bar and Greek cross devices found to be identical, so for the results presented in here are from Hall bar devices. Figure 5-10 shows the extracted carrier density as function of temperature for the nanowires with widths of 4, 7, 12 and 18 nm, fabricated on  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ . Results from widest nanowires indicated the difficulty in extracting accurate carrier density which is measured to be  $1.5 \times 10^{20} \text{ cm}^{-3}$  whereas all the nanowires demonstrates the expected trend when the widths, carrier density and temperature are varied i.e. the carrier density reduced as the width of the nanowire is reduced through surface depletion. Also for the nanowires between 7 – 18 nm, the carrier density is reduced as the temperature is reduced, shows the activated behaviour. For 12 nm nanowire which is nominally doped at  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ , the measured carrier density at 300 K is  $7 \times 10^{19} \text{ cm}^{-3}$  which is reduced to  $4.1 \times 10^{19} \text{ cm}^{-3}$  when temperature is reduced down to 1.4 K. In case of 4 nm nanowire, an anomalous behaviour is observed which is probably due to large geometrical uncertainty in extracting the carrier density which might have been related to change in the dimension of the transport. Figure 5-11 shows the hall mobility as function of temperature for the nanowires fabricated on  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ . The hall mobility of nanowires with widths between 7–18 nm tends to decrease as the temperature goes higher due to increase in scattering events. However the 4 nm nanowire has initially shown reduction in mobility from 1.4 to 150 K after which mobility increased from 150 to 300 K, indicated multiple scattering mechanisms. Also mobility at 300 K increased from 7 to 70  $\text{cm}^2/\text{Vs}$  as the width of the nanowires reduced from 18 to 4 nm. These results have not completely understood and attributed to the large geometrical uncertainty of the Hall bar devices. For these reasons Greek cross devices were fabricated which also has shown the same trend of an increase in mobility as with width of the nanowires reduced.

It is very unlikely that the electrical width can be similar to the physical width of the nanowire. In case of non-degenerately doped semiconductors, the depletion approximation allows to determine the sidewall depletion width which enables to determine the electrical width, where in degenerately doped semiconductors, the depletion approximation is no longer valid and the correct screening length is Debye length which is being true from the theoretical analysis of electron-electron, electron-impurity [28] and p-n junction potentials [29] in degenerately doped semiconductors. Therefore to determine the electrical width from the

physical width, the simplest approach is to subtract the physical width from twice the Debye screening length. From this approach the minimum and maximum electrical widths and heights are determined of the nanowires. The mean free path ( $l$ ), 3D Fermi wavelength ( $\lambda_D$ ) and Debye length ( $L_D$ ) are theoretically calculated from Eq. 5.4 to 5.8 and their values are presented in table 5-2. By directly comparing the mean free path with the physical width of the nanowire, it has been approximated that the dimensionality of the electron transport in 18 nm and 12 nm nanowire is likely to be 3D, whereas for 7 nm the transport is predominantly 2D but as the bottom foot of the nanowire is wider, some of the transport can be 3D. Similarly for 4 nm nanowire, the transport is likely to be 1D but can have 2D transport as some extent. This all shows that even at such smaller scales the transport is 1D only for the smallest 4 nm nanowire.

Mean nanowire width (nm)	Max. electrical width (nm)	Min. electrical width (nm)	Electrical height (nm)	$L_D$ (nm)	$\lambda_F$ (nm)	$l$ (nm)	Dim.
4	9.2	0.1	18.1	1.5	13	20.4	1D
7	11.1	1.4	42.3	0.81	8.7	6.7	2D / 3D
12	18.5	6.0	51.0	0.49	6.2	6.2	3D
18	25.6	12.4	51.9	0.30	4.5	4.5	3D

Table 5-2: The main characteristics length scales at 300 K for the nanowires doped at  $8 \times 10^{19} \text{ cm}^{-3}$ .

The donor activation energy can be determined from the slope of the carrier density plotted versus temperature on a log-log scale. Figure 5-12 shows the extracted activation energy for the 7 nm, 12 nm and 18 nm nanowires determined from the activated function for the carrier density,

$$n \propto \exp\left(\frac{E_D}{2k_B T}\right)$$

Where  $E_D$  is the donor activation energy. It is observed that the extracted activation energies for nanowires are significantly lower than demonstrated from bottom-up grown

nanowires without any surface passivation [30]. The lower value of donor activation energy for 7 nm nanowire as compared to 12 nm nanowire is possibly because of the change in the dimensionality of transport from 3D to 2D. The donor activation energy for the 4 nm nanowire is not extractable due to high geometrical uncertainty in determining the carrier density but could also be as a result of change in transport dimension.

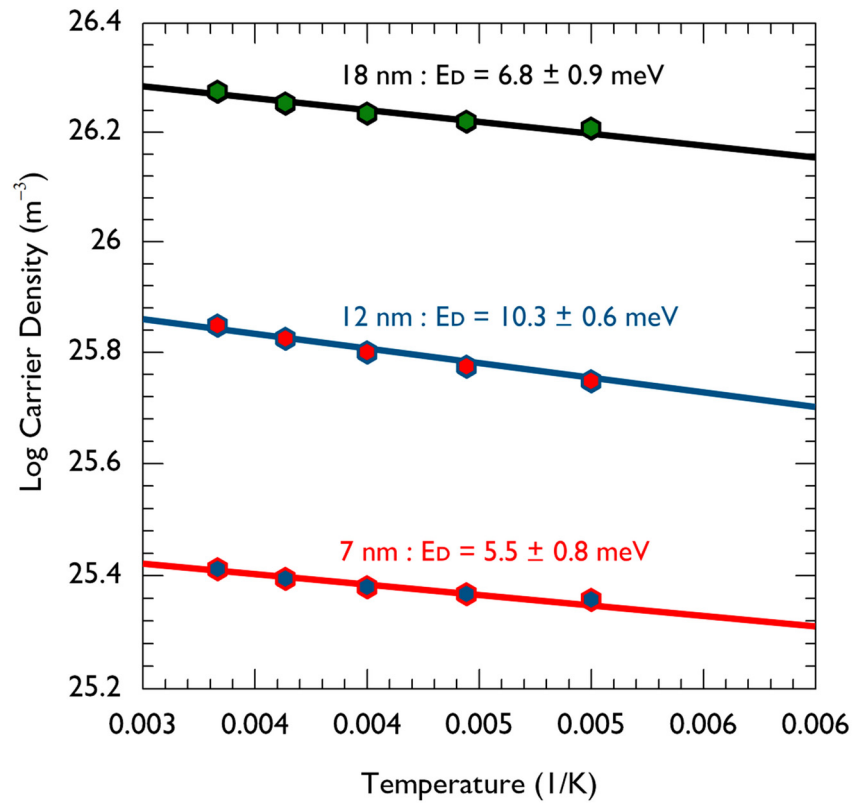


Figure 5-12: Extracted dopant activation energy from nanowires fabricated on  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ .

The donor deactivation is addressed to be primarily issue in unpassivated nanowires grown from bottom-up technique [30]. Here the donor activation energy for 12 nm nanowire is  $10.3 \pm 0.6 \text{ meV}$  which is significantly lower than demonstrated in [30] for 15 nm nanowire unpassivated nanowire where the activation energy is 46 meV. The reason behind this is that the  $\text{SiO}_2$  has a dielectric constant of 3.9 compared to air which has 1, which will significantly reduce the donor deactivation [31]. Other reason is that the grown thermal oxide in this work has a low surface trapped charge density of  $1.1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  which helps to improve the Si- $\text{SiO}_2$  interface. Whilst the etched nanowires would have higher surface state densities than

normally determined from MOS capacitors but it will still be lower than any surface without any oxidation and forming gas treatment.

In order to extract the drift mobility from the Hall mobility, it requires the knowledge of the Hall factor which is dependent onto the dominant scattering mechanism in the nanowires. The scattering mechanisms which are limiting the mobility of these nanowires are determined from the direct comparison of the experimental Hall mobility with a number of different theoretical calculated mobilities corresponds to the scattering mechanisms discussed in section 5.1.3. The total mobility was estimated by using the Matthiessen's rule defined as,

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_{oc}} + \frac{1}{\mu_I} + \frac{1}{\mu_{NI}} + \frac{1}{\mu_{IRS}}$$

Whilst the Matthiessen's rule has a significant uncertainty as the weighting of the scattering mechanism is not taken into account but still has sufficient accuracy to allow to determine the dominant scattering mechanism without going into details of Monte Carlo modelling approaches. Figure 5-13 shows the experimental Hall mobility compared with different scattering mechanism for 7 nm nanowire doped at  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ .

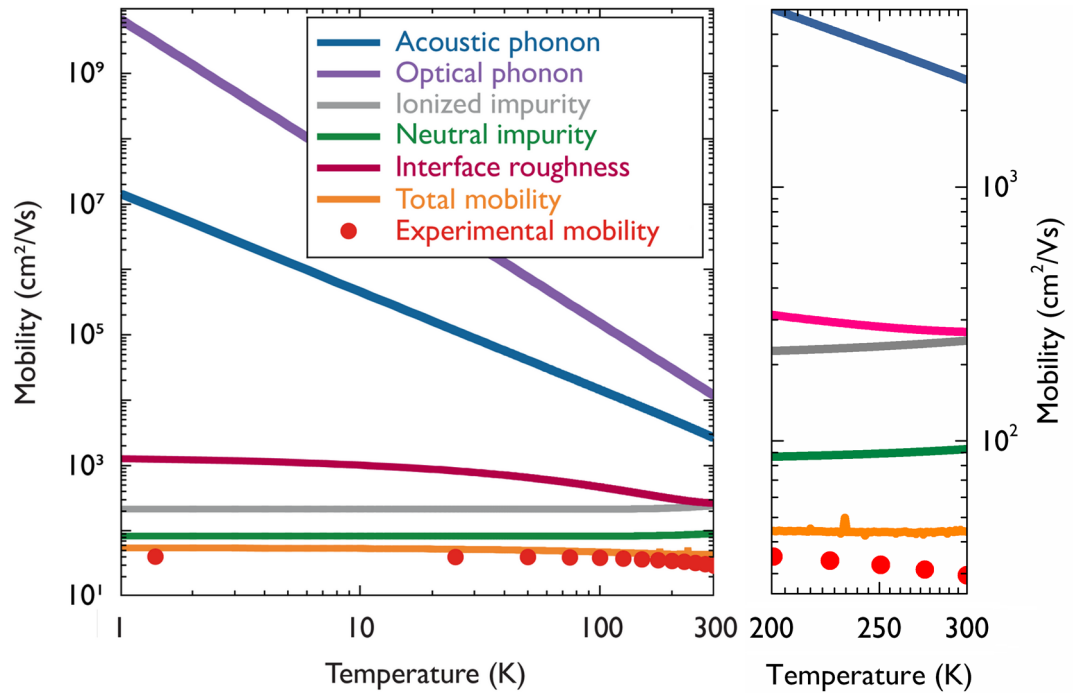


Figure 5-13: Comparison of experimental Hall mobility with different scattering mechanisms for the 7 nm nanowire doped at  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ .

It is determined from the modelling that neutral impurity scattering is the dominant scattering mechanism limiting the mobility in these nanowires. The interface roughness scattering is not found to be significant as compared to the neutral impurity scattering, even for  $\Delta = 2$  nm and  $\Lambda = 1$  nm, the interface roughness scattering is still insignificant for compared to other scattering mechanisms. As neutral impurity scattering is dominant scattering mechanisms, therefore Hall factor is 1 for these degenerately doped nanowires and so the drift mobility equals to the Hall mobility.

### 5.4. Summary

Silicon nanowires are fabricated using top-down fabrication approach down to 4 nm, the transport properties are studied for degenerately doped silicon nanowires and determined that neutral impurity scattering is the performance limiting scattering mechanism in these nanowires. The characteristic length scales are theoretically calculated and directly compared with the physical width of the nanowires to approximate that the electron transport is likely to be 3D in 12 nm nanowire and 2D and 1D in 7 nm and 4 nm nanowires respectively. The Hall factor is determined from experiments to be 1, indicating that the Hall mobility equals the drift mobility for these nanowires. Moreover, the donor deactivation and surface roughness are the major challenges in bottom up grown nanowires, which are not determined to be significant in top-down fabricated nanowires, indicating the importance of high quality surface passivation for all the nanowires at these length scales.

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## 6. Silicon Nanowire Junctionless Transistors

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Over a few decades, scaling the dimensions of the silicon based metal-oxide-semiconductor field-effect-transistors (MOSFETs) has remarkably achieved over 2.5 billion transistor in present day microprocessor chip. Whilst scaling allows to achieve higher packing density, but downsizing the transistor with gate length ( $L_G$ ) below  $\sim 100$  nm has not been brought up significant improvements in the device performance, hence strained silicon [1] been introduced to enhance velocity saturation [2]. Moreover the gate dielectric ( $\text{SiO}_2$ ) has also been scaled down to its physical limit  $\sim 1.2$  nm and scaling further has markedly affected by quantum mechanical tunnelling effect, result in significant static current leakage from gate to channel, which increased the off current and the power consumption [3]. The switching operation of the transistors below  $L_G \sim 50$  nm is predominantly affected because it is quite challenging to control the on/off current at smaller length scales due to poor electrostatic control of the gate over the channel. Whilst high-k gate dielectric materials such as hafnium oxide ( $\text{HfO}_2$ ) has also been preferred over conventional gate dielectric ( $\text{SiO}_2$ ) to gain better electrostatic control [4] and metal gates are replaced with poly-silicon to avoid depletion effects [5] but despite of all these sustained efforts, scaling has further increased the short channel effects and high off current made that extremely difficult to exponentially shrink the planar-gate MOSFETs any further by using conventional approaches.

Therefore, the conventional planar-gate is being replaced with wrap-around-gate to realize transistors with better electrostatic control over the channel to allow further downsizing without trading-off the performance of the transistors. Figure 6-1 [6] illustrates a number ways in which wrap-around-gate can be modified to realize different types of FETs, such as FinFETs [7], Tri-gate FinFETs [8,9],  $\pi$ -gate FETs [10,11],  $\Omega$ -gate FETs [12], gate-all-around FETs [13,14] and bulk tri-gate FinFETs [15]. These all structures are termed as multigate transistors since the channel is being wrapped around by the gate from the multiple sides. The electrostatic control which is the capacitive coupling between the gate and the channel (achieved through the gate oxide) tends to improve as the wrap-around-gate is modified from figure 6-1a to 6.1e, hence the gate-all-around provides the maximum electrostatic control over the channel. Multigate transistors has reduced short channel effects and has low off-state and high on-state current

drive which allows faster switching operation. Low drain voltage ( $V_{DS}$ ), reduced swing in threshold voltage ( $V_{Th}$ ) and minimized random dopant fluctuations (RDF) made multigate transistors suitable candidate for future CMOS technologies.

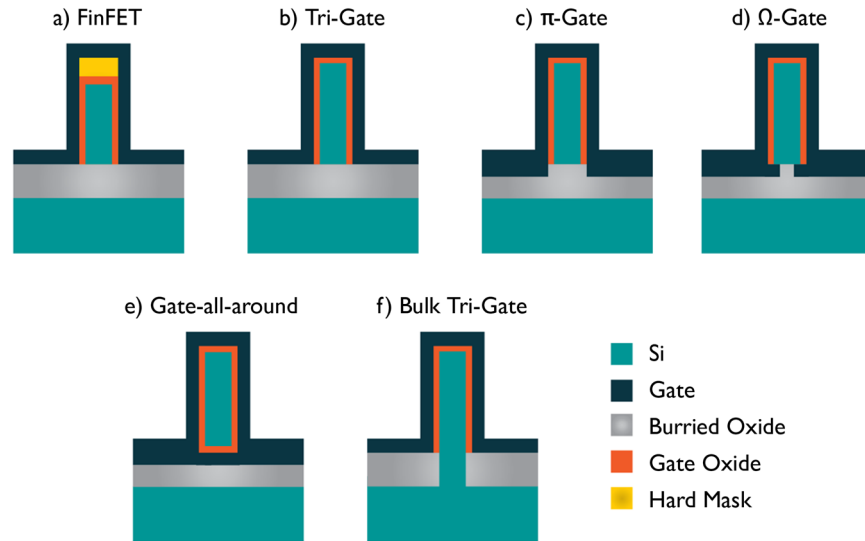


Figure 6-1: Illustration of different types of wrap-around-gate (multigate) FETs.

This chapter demonstrates 150 nm gate length junctionless transistors fabricated with widths from 24 – 8 nm on  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$ . It was observed that the electric field from the gate unable to modulate the drive current of the widest channel (24 nm) due to screening effects from the high electron concentration which prevents carrier depletion in the channel. However as the channel width was reduced from 16 nm to 8 nm, the drive current been modulated by the applied gate voltage and a high drive current  $\sim 1.28 \text{ mA}/\mu\text{m}$  has been observed for 8 nm wide transistor where the ratio between on/off was over  $\sim 10^8$  orders with a low SS of 66 mV/decade and  $V_{Th} \sim 0.18 \text{ V}$  at  $V_D = 1.5 \text{ V}$ . Moreover, the 8 nm wide transistor behaved like an insulator at low temperatures and revealed single electron oscillations at 1.4 K.

## 6.1. Conduction Mechanisms in Junctionless Transistors

The multigate transistors as figure 6-1 depicts are further characterized based on the doping of the source, drain and channel regions. Generally there are three main conduction mechanisms in multigate FETs from the doping prospective, i.e. inversion, accumulation and partial depletion mode, where the source, drain and channel regions are doped as  $N^+P N^+$ ,  $N^+N N^+$  and  $N^+N^+N^+$  respectively. The inversion and accumulation mode transistors [16,17] are the standard MOSFETs based on the formation of PN or Schottky junctions where the

drain is initially reverse biased to restrict any current flow in the channel region unless a sufficient gate voltage is being applied to create an inversion layer to provide a way for the carriers to flow between the source and drain regions. Hence these transistors are normally off and after the inversion layer being created, the current flows and transistor turned on. This is further illustrated in figure 6-2 [18] where the gate voltage is plotted as a function of Log of drain current to demonstrate these conduction mechanisms in more detail.

For the inversion mode transistors, the channel region is depleted for the gate voltage ( $V_G$ ) below the threshold voltage ( $V_{Th}$ ) and the flatband voltage ( $V_{Fb}$ ) lies well below the  $V_{Th}$  where the transistor is switched off and channel region is predominantly neutral below the  $V_{Fb}$ . Above the  $V_{Fb}$ , depletion starts and an inversion layer is formed for the  $V_G > V_{Th}$  to turn on the transistor. Whereas for the accumulation mode transistors, the channel region is depleted below the  $V_{Th}$  and partially depleted above the  $V_{Th}$  until the  $V_G = V_{Fb}$  where the channel region becomes neutral. Above  $V_G > V_{Fb}$  accumulation layer being formed to keep the transistor on.

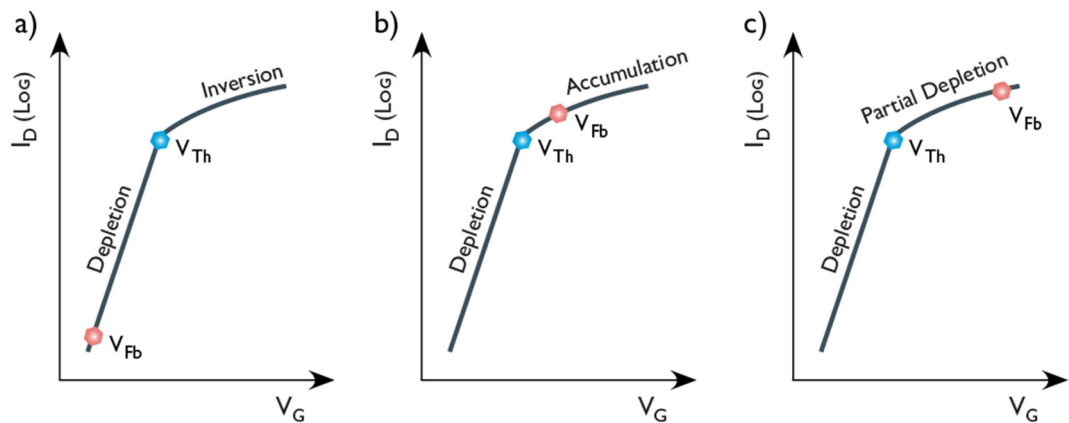


Figure 6-2: Illustration of conduction mechanisms in multigate FETs from doping prospective a) inversion b) accumulation and c) partial depletion mode.

On the contrary, the transistors which operates in partial depletion mode are normally on, they are referred as junction-less transistors or gated resistors [18, 19, 20] since all the transistor regions are degenerately doped with either  $N^+$  or  $P^+$ , hence no doping density gradients are required to form any PN junctions which is a pre-requisite for inversion and accumulation mode transistors. The junctionless transistor works quite similar to an accumulation mode transistor, the channel region is fully depleted in sub-threshold regime ( $V_G < V_{Th}$ ) and becomes partially depleted as the  $V_G$  increases which causes degradation of the

depletion width, allows the current to flow from the neutral path. At  $V_G = V_{Th}$  the electron concentration reaches the doping density of the channel, increasing  $V_G$  beyond  $V_{Th}$  reaches the  $V_{Fb}$  where the channel region becomes fully neutral. Applying  $V_G > V_{Fb}$  makes the channel behaves like a resistor because of the formation of accumulation layer near the interface which is not desirable since a high current drive has already been achieved through the higher doping density in the partial depletion regime with a lower electric field as compared to an accumulation mode transistor [18]. This is due to the work function difference between the gate and the channel which shifts both the  $V_{Th}$  and  $V_{Fb}$  to the positive values [21]. The conduction mechanisms in a junctionless transistor are illustrated in figure 6-3.

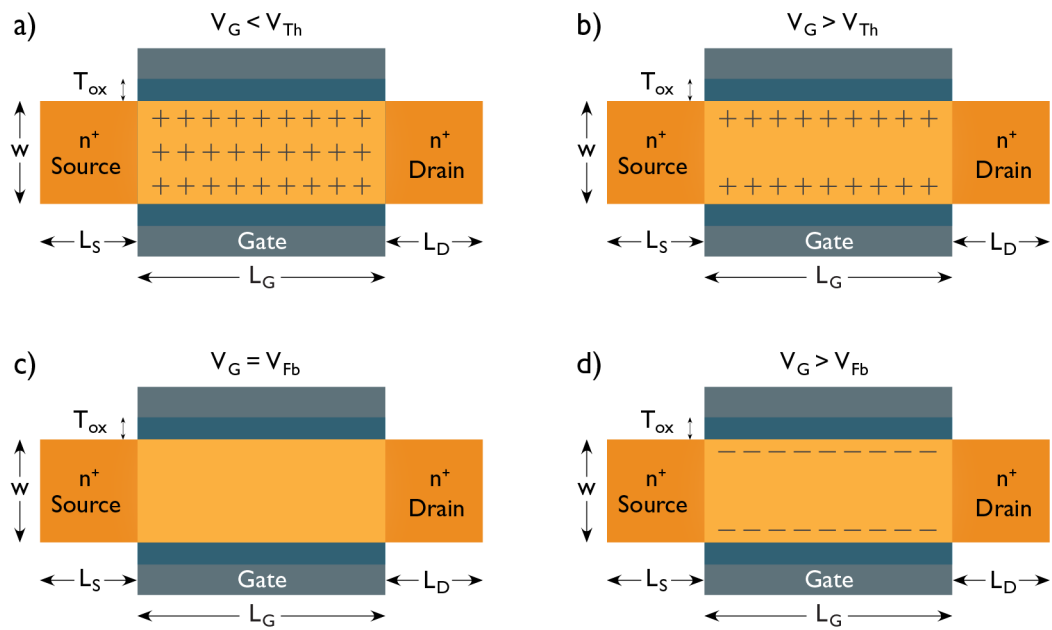


Figure 6-3: Illustration of top view of n-type junctionless transistor in a) depleted b) partially-depleted c) flat-band and d) accumulation mode.

It is worth mentioning that in inversion mode transistors, for  $V_G > V_{Th}$  the most of the conduction is through the formation of inversion layer on the interface, where the majority of the carriers are confined on the top surface and sidewalls with peaks of the carrier concentration lies on the corners of the channel, as illustrated in figure 6-4a [21]. The same holds true for an accumulation mode transistor where the carrier concentration of the middle part equals the doping density of the channel for the  $V_G > V_{Th}$  and only a small current is being added before the flatband is reached. Hence in both cases the conduction is mainly through the

surface inversion/accumulation. However in the case of junctionless transistor, the conduction is through the bulk or centre of the channel (figure 6-4c [21]) for both the off-state and the on-state current, thus requires significantly lower electric field to direct the carriers which doesn't deteriorate the mobility at higher gate voltages [22].

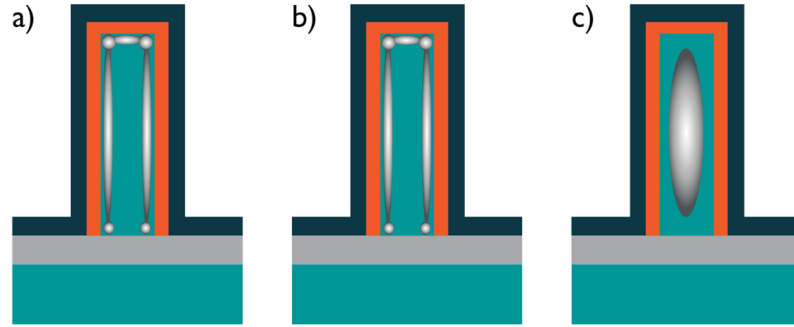


Figure 6-4: The conduction path in an a) inversion mode b) accumulation mode and c) partial depletion mode (junctionless transistor) for the  $V_G > V_{Th}$ .

The on-state current drive of the junctionless transistor is given by [19],

$$I_{DSat} \approx q\mu N_D \frac{T_{ch} W_{ch}}{L} V_D$$

$$V_{DSat} = V_G - V_{Fb} - \left( \frac{qN_D T_{ch}}{2\epsilon_{ch}} + \frac{qN_D T_{ch}}{C_{ox}} \right)$$

Where  $N_D$  is the doping density,  $T_{ch}$  and  $W_{ch}$  are the thickness and width of the channel,  $V_D$  is the drain voltage,  $L$  is the gate length,  $\epsilon_{ch}$  is the relative permittivity of the channel material and  $C_{ox}$  is the gate oxide capacitance. Clearly, the drain current is proportional to the doping density and doesn't directly related to the gate oxide capacitance unlike the inversion mode transistors. Hence the drain current increases with increasing the doping density [19]. The effective channel length is the distance between the source and the drain region and becomes critically important if the dimensions of the source, drain and channel are comparable. The source and the drain creates a depletion region due to the formation of PN junction which penetrates the into the channel region and take control of the part of the channel from the gate. Thus the effective channel length if equals the gate length shortens (figure 6-5a [21]) and result in short channel effects (SCE). The primarily cause of SCE is drain-induced barrier lowering (DIBL) which is due to a further increase in the depletion region from the drain side

as the  $V_D$  is increased. DIBL lowers the  $V_{Th}$  with increasing  $V_D$  which directly influences the sub-threshold slope as leakage current increases which in turn increases the off-state current of the inversion/accumulation mode transistors. Thus lowers the switching speed of the transistor by [19],

$$\frac{\Delta f}{f} = - \frac{2 \text{ DIBL}}{V_D - V_{Th}}$$

However in a junctionless transistor, the source and the drain regions are rather squeezed as shown in figure 6-5b which result in an increases in the effective channel length, typically larger than the gate length, hence significantly reduces the unnecessary SCE which are limiting the junction based transistors to be further scaled down.

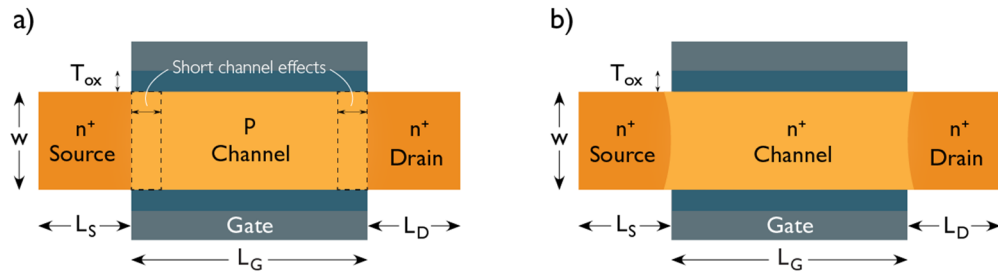


Figure 6-5: Effective channel length as a result of short channel effects in an  
a) inversion mode and b) junctionless transistor.

The sub-threshold slope  $SS$  determines the efficiency of a transistor to switch from its off-state to its on-state. It is  $SS$  defined as,

$$SS = \frac{\delta V_g}{\delta(\log I_D)} = \frac{k_B T}{q} \ln(10) n$$

Where  $n$  is the body effect and set to unity if the gate is effectively controlling the channel, at  $T = 300 \text{ K}$  the ideal  $SS$  a transistor could have is  $\sim 59.52 \text{ mV/decade}$  [19]. The threshold voltage is the gate voltage at which the magnitude of diffusion current equals drift current and transistor turns on. Whilst several analytical models have been proposed to determine  $V_{Th}$  but given below also accounts fully depleted channel at threshold [23],

$$V_{Th} = \phi_{MS} - qN_D \left[ \frac{WH}{C_{ox}} + \frac{1}{\epsilon_{ch}} \left( \frac{WH}{2H + W} \right)^2 \right] + \frac{\pi^2 \hbar^2}{2qm^*} \left[ \frac{1}{H^2} + \frac{1}{W^2} \right]$$

Where  $\phi_{MS}$  is the metal-semiconductor work function,  $N_D$  is the carrier density,  $W$  and  $H$  are the width and height of the channel,  $\epsilon_{ch}$  is the relative permittivity of the channel material,  $C_{ox}$  is the gate oxide capacitance,  $m^*$  is the effective mass and  $\hbar$  is the Planck's constant divided by  $2\pi$ . There are number of ways to extract  $V_{Th}$  but the most profound method used in multigate transistors is transconductance to drain current ratio to determine the point where magnitude of the drift current equals diffusion current, which is satisfied at the half of the maximum value of the ratio.

$$\frac{g_m}{I_D} = \frac{1}{2} \left( \frac{g_m}{I_D} \right)_{max}$$

## 6.2. Device Fabrication and Experimental Setup

Junctionless transistors are fabricated using SOI substrate on  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$ . These are fabricated with channel widths from 24 – 8 nm where the channel length is 150 nm. The top silicon layer is initially etched before any pattern transfer from 55 to 10 nm to minimise unnecessary corner effects which becomes more visible as the channel width of hall bar devices reduced from 24 – 4 nm (figure 5-5). Similar device fabrication techniques are used for the fabrication of junctionless transistors as discussed in section 4.1, except that Al is deposited for source-drain metallization instead of two stage metallization i.e. Ni-Pd for make ohmic contacts and Al for bond pads.

Description		Dose ( $\mu\text{C cm}^{-2}$ )	Beam step size (nm)	Spot size (nm)
Pattern Transfer	Layer 1	4700	2.5	3
	Layer 2	2800	5	3
	Layer 3	2500	25	33
Metallization		2200	25	33

**Table 6-1: Electron beam exposure parameters used for pattern transfer and source-drain & top-gate metallization of the junctionless transistors.**

Moreover to avoid leakage current from the gate, a thicker  $\text{SiO}_2$  ( $\sim 18 \text{ nm}$ ) is grown at an oxygen flow of 525 litre/hour at  $950^\circ\text{C}$  for 1 minute and 40 seconds. The layout for the pattern transfer is designed in similar way the Hall bar layouts are designed. The electron beam

exposure parameters are shown in table 6-1. The SEM image of the fabricated  $\sim 8$  nm wide junctionless transistor is shown in figure 6-6 whereas it's cross-sectional TEM image is shown in figure 6-7. The TEM image confirms the top-gate deposited resembles to a tri-gate as depicted in figure 6-1.

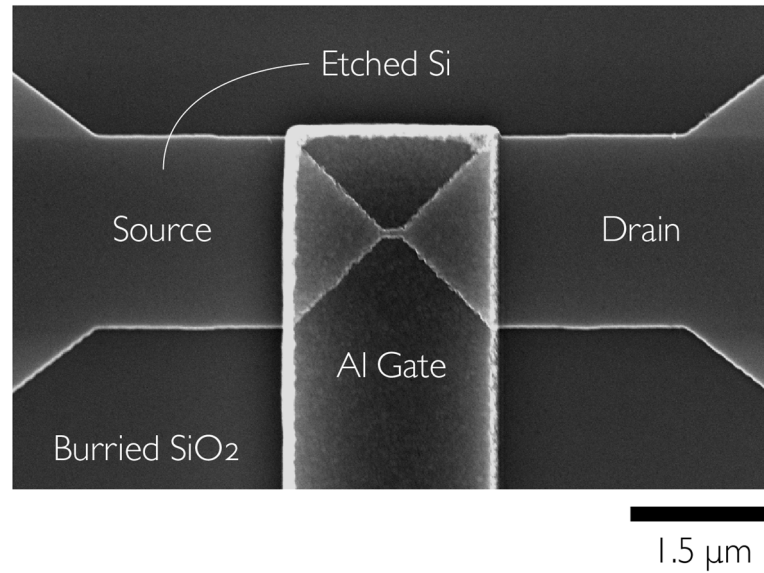


Figure 6-6: a) SEM image of junctionless transistor with channel width = 8 nm and effective channel length = 150 nm.

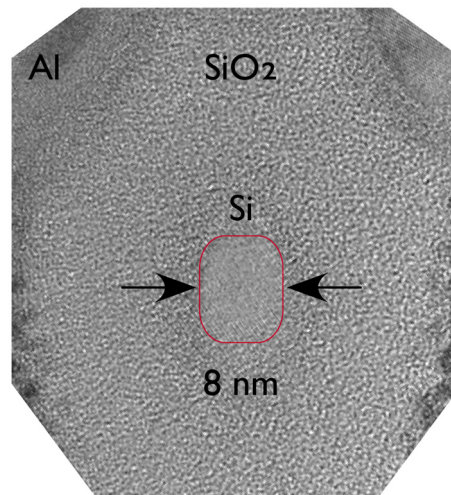


Figure 6-7: Cross-sectional TEM image of the 8 nm channel width.

The experimental setup used to perform DC and AC measurements onto the junctionless transistor is shown in figure 6-8. For DC measurements, Agilent B1500



semiconductor parameter analyser was used which was connected to probe of Oxford Instruments Teslatron via a BNC pin-out box to access the bonded device inside the cryostat. This allowed to perform temperature dependent DC measurements ranging from 300 to 1.4K. Similarly low noise/ low current AC measurements are performed to probe Coulomb blockade and single electron tunnelling in a junctionless transistor typically at cryogenic temperatures. An Agilent 33521A arbitrary waveform generator source was used with a voltage divider to apply low voltage to the source of orders of few mV whereas Stanford Research SR-830 lock-in amplifiers were used to record  $V_{in}$  at the source input and  $I_{out}$  drain output simultaneously while  $V_G$  being applied from Agilent 3631A power supply. All these instruments were accessed and controlled using a LabView's virtual instrument (VI) program connected to the computer via GBIP interfaces.

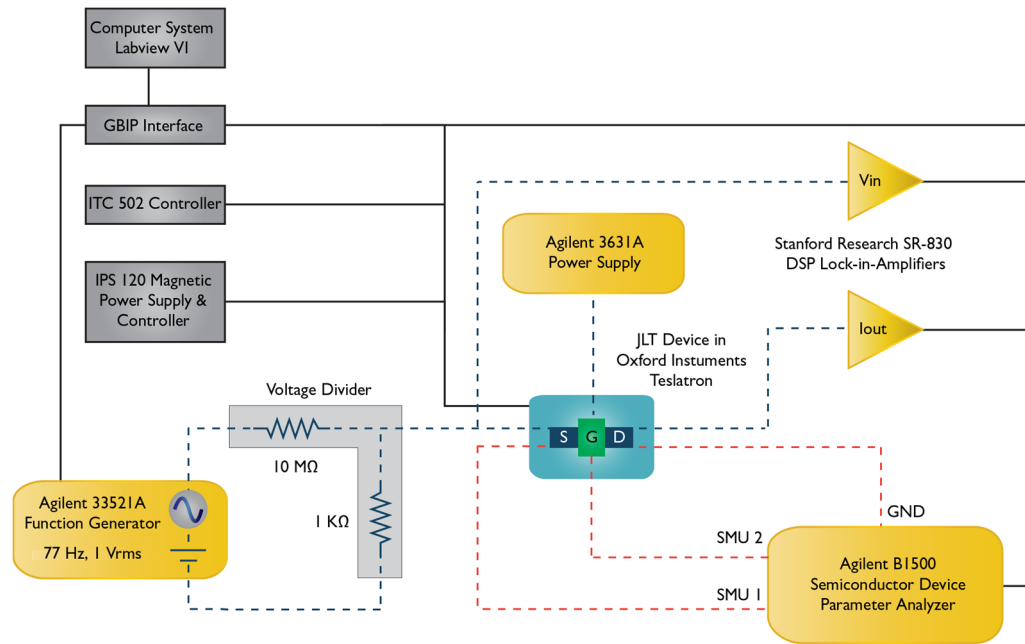


Figure 6-8: Experimental setup for DC and AC measurements taken at room and cryogenic temperatures using Oxford instruments Teslatron.

### 6.3. Results & Discussions

Degenerately doped junctionless transistors are fabricated on SOI substrate with channel width = 24, 16 and 8 nm, channel height = 10 nm and channel length = 150 nm, where  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$ . A 2  $\mu\text{m}$  wide wrap-around-gate (resembles to a tri-gate, figure 6-1) is deposited over the channel covering the effective channel length. Initially DC measurements were

performed with BI 500 semiconductor parameter analyser at room temperature in a Cascade microtech probe station. The drive current in a planar gate transistor is generally normalized by the width but in a tri-gate configuration, since the channel is being electrostatically controlled by the 3 sides, the effective width becomes  $2H + W$ , where  $H$  is the height and  $W$  is the width of the channel. The variation in the drive current as a function of channel width measured at  $V_D = 1.5$  V is shown in figure 6–9. Results indicated an increase in drive current from 1.28 mA/ $\mu\text{m}$  to 1.75 mA/ $\mu\text{m}$  as the width of the channel increases from 8 to 24 nm for the fixed channel length. Clearly this is attributed to the doping density, since the drain current in a junctionless transistor is proportional to the doping density. Also the carrier density tends to increase with the increasing width (figure 5-10), so the drive current increases proportionally. In previous discussion while determining the resistivity of the nanowires (figure 5-8) fabricated on SOI substrate with a doping density  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$ , a significant degradation in resistivity has been observed due to depletion effects and as the nanowire widths reduced from 24 to 7 nm, the resistivity increased from 8 to 70 m-ohm-cm respectively. Hence it can be anticipated that the doping in the wider channels is  $N^+$  which becomes predominantly  $N$  as the channel width is reduced due to increase in the depletion effects.

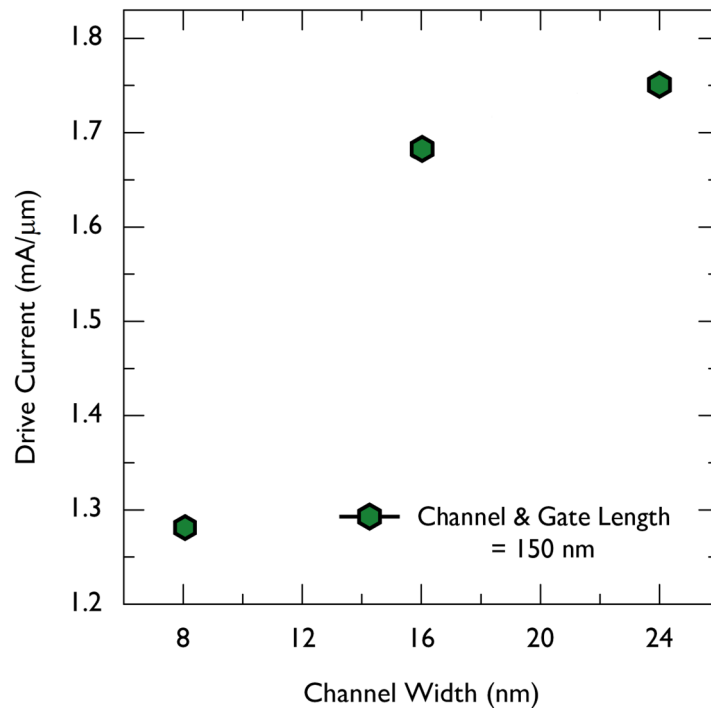


Figure 6-9: Drive current in a junctionless transistor as a function of different channel widths.

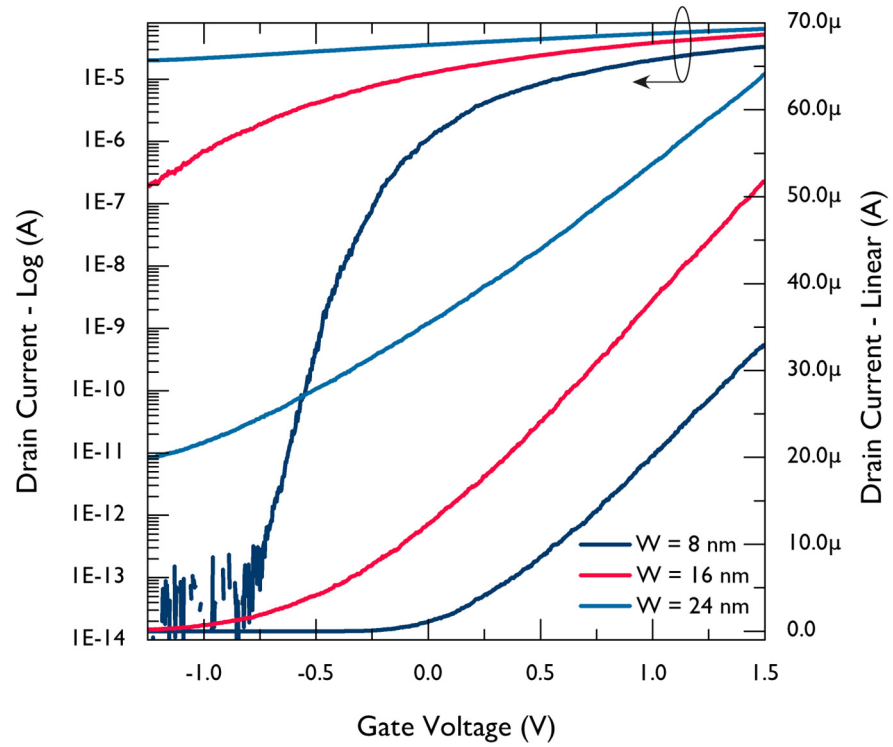


Figure 6-10: Transfer characteristics ( $I_D$ – $V_G$ ) of junctionless transistor with widths 8, 16 and 14 nm measured at  $V_D = 1.5$  V.

For 8 nm wide transistor, the measured off-state current  $\sim 1 \times 10^{-14}$  A (or 0.35 pA/ $\mu\text{m}$ ) is below the minimum current detection level of the B1500 semiconductor parameter analyser whereas the on-state drive current is  $\sim 3.6 \times 10^{-5}$  A (or 1.28 mA/ $\mu\text{m}$ ) at  $V_G = 1.5$  V, hence an enormous enhancement in the current has been observed where the ratio between on/off current is over  $\sim 10^8$  orders. With similar doping density, the drive current is over an order higher than previously demonstrated [19], but this could potentially be due to shorter channel length in our transistors, since most of the demonstrations typically has a channel length over 1  $\mu\text{m}$  [19–21] and drive current is known to increase as the channel length is reduced [24]. The peak transconductance lies at  $V_D = 1.2$  V which is  $\sim 26.5$   $\mu\text{S}$ . The threshold voltage is extracted from transconductance to drain current ratio method. For 8 nm wide transistor,  $V_{Th}$  is  $\sim 0.18$  V measured at  $V_D = 1.5$  V, whereas for 16 and 24 nm wide transistors,  $V_{Th}$  is  $-0.37$  V and  $-1.75$  V respectively. Hence wider transistors are predominantly depletion mode devices whereas the 8 nm wide transistor is on the edge of depletion and enhancement mode, since  $V_{Th}$  is close to zero for higher drain voltages whereas in minus for lower drain voltages.

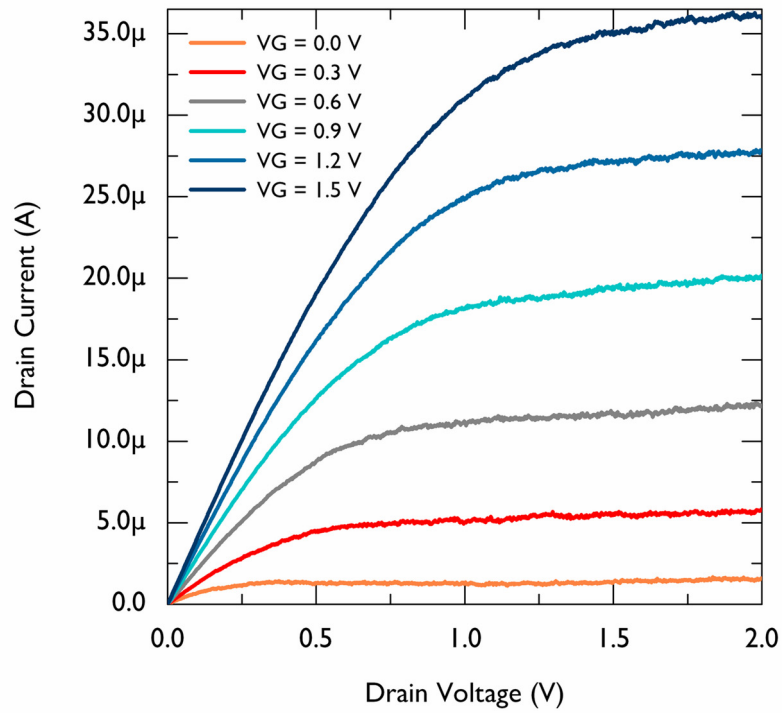


Figure 6-11: Output characteristics ( $I_D$ – $V_D$ ) of an 8 nm wide junctionless transistor at  $V_G$  ranging from 0 to 1.5 V in steps of 300 mV.

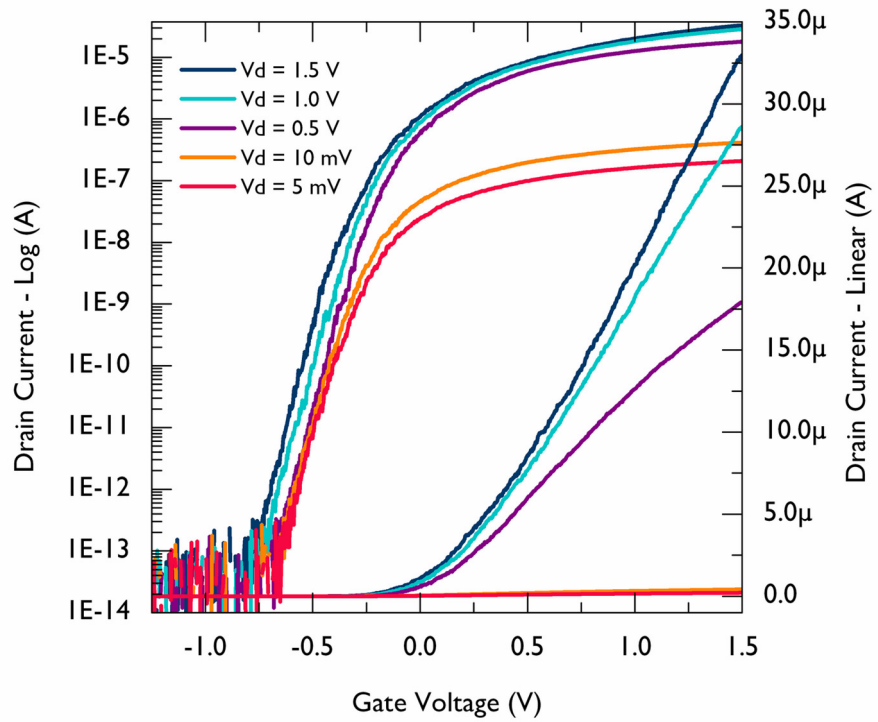


Figure 6-12: Transfer characteristics ( $I_D$ – $V_G$ ) of an 8 nm wide junctionless transistor at  $V_D$  ranging from 5 mV to 1.5 V.

Analysing the sub-threshold slopes of different channel widths measured at  $V_D = 1.5$  V, the 8 nm wide transistor has a minimum sub-threshold slope of 66 mV/decade (measured between  $1 \times 10^{-12}$  to  $1 \times 10^{-11}$  A). Such low sub-threshold slope is close to the ideal theoretical limit of  $\sim 59.52$  mV/decade and reveals body effect  $n = 1.11$ , which means that the gate is controlling the channel with over  $\sim 89\%$  efficiency. In contrast for 16 nm wide transistor, sub-threshold slope increased dramatically to 580 mV/decade where the ratio between on/off current fallen to less than  $\sim 10^3$  orders as compared with  $\sim 10^8$  orders with 8 nm wide transistor, moreover the off-state current increased to  $4.89 \times 10^{-7}$  A. For 24 nm wide transistor, the sub-threshold becomes nearly flat as the drain current increased linearly from  $2.55 \times 10^{-5}$  to  $6.41 \times 10^{-5}$  A for the gate voltages between  $V_G = -1.5$  to 1.5 V. So the wider channels has metallic conductivity and behaving more like a resistor but as the channel width is reduced and surface depletion increases, the gate has got effective control over the channel. A 2 nm surface depletion for an 8 nm wide transistor accounts 50% of the channel, hence provides room to be operated in a junctionless mode. To evaluate the short channel effects, DIBL is determined from the following relation,

$$DIBL = - \frac{V_{Th}^{high} - V_{Th}^{low}}{V_D^{high} - V_D^{low}}$$

Where  $V_{Th}^{high}$  and  $V_{Th}^{low}$  is the threshold voltage extracted at a higher ( $V_D^{high}$ ) and a lower ( $V_D^{low}$ ) drain voltage respectively. For an 8 nm wide transistor, change in the threshold voltage extracted at 1.5 and 10 mV drain voltages is  $\sim 159$  mV, hence the DIBL is  $\sim 106$  mV/V. For such low DIBL the loss in switching operation is  $\sim 16\%$ . Moreover an enormous increase in DIBL ( $\sim 1340$  mV/V) has observed for 16 nm wide transistor which corresponds to further deterioration of switching operation by  $\sim 237\%$ . Hence with fixed channel width  $\sim 150$  nm, increasing the channel width incorporates severe short channel effects. The junctionless transistors has slightly higher threshold voltage dependence on temperature than its rivals, therefore transfer characteristics of an 8 nm wide transistor are measured at different temperatures. Earlier the resistivity of the nanowires as function of temperature (figure 5-9) is discussed in section 5.3. It was observed that for wider widths the resistivity decreases as temperature goes down from 300 – 1.4 K due to metallic conductivity, however for the nanowire with the smallest width, resistivity increased as the temperature goes down from 300 to 150 K after which resistivity decreased as the temperature is further reduced to 1.4 K.

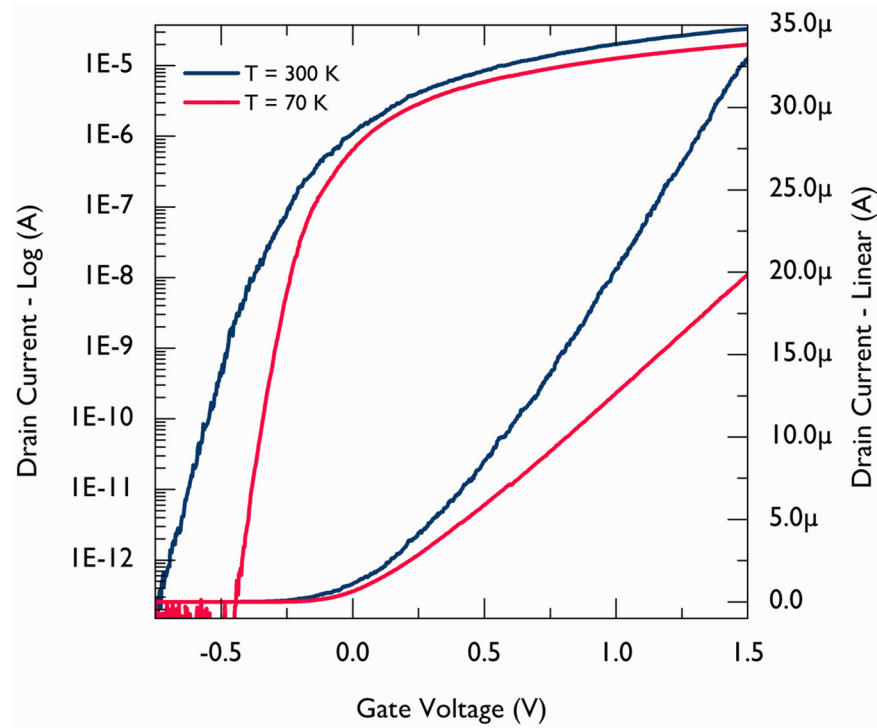


Figure 6-13: Transfer characteristics ( $I_D$ - $V_G$ ) of an 8 nm wide junctionless transistor for  $V_D = 1.5$  V measured at 300 K and 70 K.

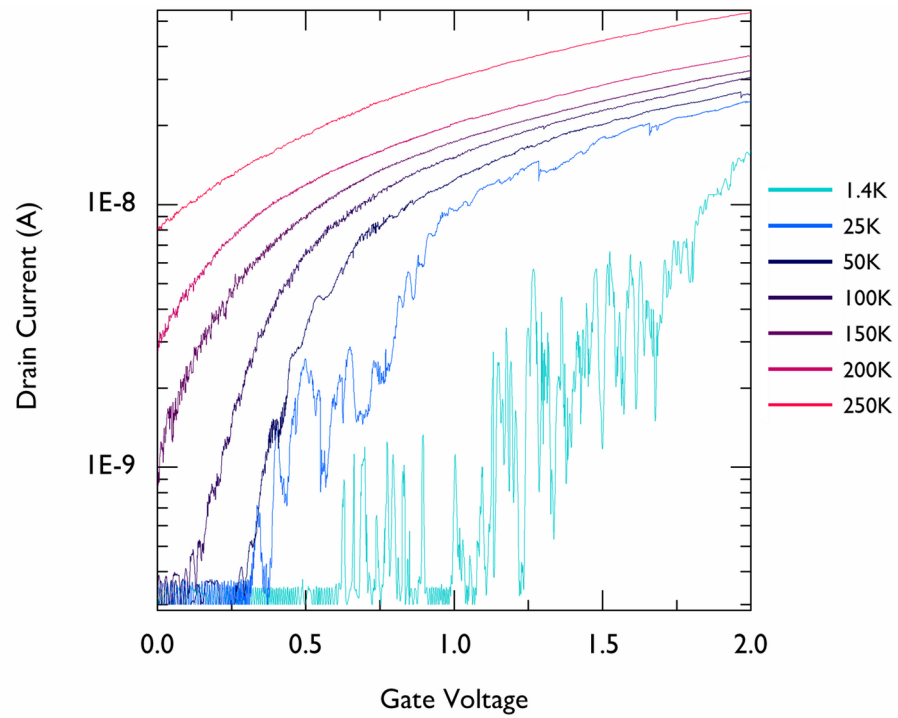


Figure 6-14: Temperature dependent transfer characteristics of an 8 nm wide junctionless transistor measured at  $V_D = 10$   $\mu$ V using AC techniques.

This is due to swap over in the transport mechanism observed in partially depleted nanowires. Similar characteristics has been observed while measuring the transfer characteristics of 8 nm wide junctionless transistor. The threshold voltage is moved towards more +ive values as the temperature goes down but below 150 K a swap over has been observed and threshold voltage started moving the other way. Figure 6-13 depicts the threshold voltage measured at  $V_D = 1.5$  V at 70 K, revealed a decrease in threshold voltage to  $\sim 0.06$  V as compared to  $\sim 0.18$  V measured at 300 K. The sub-threshold slope however decreased as function of temperature since it's predominantly depends on the diffusion current. The minimum sub-threshold measured at 70 K is  $\sim 39$  mV/decade (between  $1 \times 10^{-12}$  to  $1 \times 10^{-11}$  A). However due to fewer measurements, the discrepancy between sub-threshold slope and temperature can't be established. The sub-threshold slope at 300 K is 66 mV/decade which revealed body effect  $n = 1.1$ . Considering the similar body effect, theoretically the sub-threshold slope at 70 K would be 15.4 mV/decade, whereas experimentally 39 mV/decade has been observed at 70 K. This could be due to the argument established from the measurements and theoretical calculations in chapter 5 that only half of the donors has been activated and the mobility is vastly affected by the neutral impurity scattering mechanism. Hence the sub-threshold slope has not been linearly decreased as function of temperature due to degradation of mobility.

Further it was observed that the current in sub-threshold regime is suppressed for small applied voltages  $\sim 10$  mV below 70 K, indicated the evidence of Coulomb blockade and single-electron tunnelling effects. This has been further explored with another 8 nm wide transistor using low noise/ low current AC technique, where a constant  $V_D = 10$   $\mu$ V is applied to the source and current is measured at drain terminal using lock-in-amplifiers while the  $V_G$  is swept from 0–2V. Assuming an 8 nm wide transistor has a surface/line-edge roughness of a nm, corresponds to 25% of the channel total width of the channel. There is a fair possibility that the channel has formed into a number of islands of charge through which the electrons are tunnelling. Results are presented in figure 6-14, shows a non-linear sub-threshold current below 50 K which turned into a number of periodic single-electron oscillations at 1.4 K for the  $V_G$  between 0.6 – 1.75 V. The average width of the oscillation is  $\sim 12$  meV which corresponds to an island size of  $\sim 7$  aF. However when the temperature is increased to 25 K, most of the oscillations are smeared out because the thermal energy exceeded the charging energy of the corresponding islands.

## 6.4. Summary

Results are presented for the short-channel junctionless transistors fabricated with widths from 24 – 8 nm where the channel length is fixed to  $\sim 150$  nm. It was observed that wider channels has metallic conductivity but as the width is reduced to 8 nm, an increase in surface depletion makes the channel partially depleted to be operated in junctionless mode. A high drive current  $\sim 1.28$  mA/ $\mu$ m has observed for 8 nm wide transistor where the ratio between on/off was over  $\sim 10^8$  orders with a low SS of 66 mV/decade and  $V_{Th} \sim 0.18$  V at  $V_D = 1.5$  V. Moreover a low DIBL  $\sim 106.6$  mV/V has also been observed indicated reduced SCE. However the threshold voltage extracted for the lower drain voltages found to be predominately in negative. At  $V_G = 0$ , there is significant drive current in the channel of orders of  $10^{-6}$  A, whereas the off-state current ( $1 \times 10^{-14}$  A) is measured at  $V_G = -0.75$  V. These issues can be addressed by replacing the aluminium with another metal, which has a higher work function. For example, molybdenum and tungsten (has a work function varies between 4.36 – 4.95 and 4.32 – 5.22 respectively) can be used to shift the off-state current and sub-threshold characteristics towards the positive values by a volt. Moreover, etch process has to be optimized for any of these metals using  $SF_6/C_4F_8$  based ICP plasma to downsize the present gate length from 2  $\mu$ m down to a few nm.



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## 7. Molecular Metal Oxide Nanoelectronics

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The molecular electronics has gained substantial interest in potential application in non-volatile flash memory devices due to the requirement of the low operational power for the electronic devices. The molecular reduction-oxidation (redox) states allows to reversibly charge and discharge the molecules by applying alternative  $\pm$  voltage pulses if they being used as a floating gate (FG) in a typical metal oxide semiconductor (MOS) transistor [1]. The charge stored in the floating node changes the surface potential and so the conductivity of the channel which controls the sub-threshold slope (SS) of the MOS transistor. Encapsulating the molecular charge in the FG provides strong charge confinement and has advantages over conventional poly-silicon FG memory devices where the interference due to FG result in a shift of 0.2 V in a multilevel cell operation due to capacitive coupling between the cells [2]. Whilst this issue can be addressed by introducing the charge trapping dielectrics [3] or metallic nano clusters [4] in the FG but can potentially result in large variability in charge trap density.

The redox active molecules produced as a result of chemical synthesis have better self-assembly and yields to linear spatially distribution in the charge storing centres [5] allows to realize FG down to a few nm. Efforts has been made in pursuit of molecule based flash memory devices, such as organic redox active molecules based on ferrocene [6], porphyrin [5] and fullerenes [7] are used to demonstrate memory devices but these are subject to low retention time (due to lower redox potential) and high thermal budget. Also these demonstrations suffers from low electrical conductivity, high access resistance and difficulty to produce in high yield. There are other practical issues associated such as requirement to chemically attach the molecules to the substrate [8], complicated molecule in-device assembly steps [9], electrode materials incompatible with MOS [10], complex write processes using optical input [11] and most importantly the molecules are not compatible with high temperatures to properly integrate them into the current MOS technologies. On the contrary, the inorganic redox active molecules are not been predominately explored in the quest for memory devices. Therefore this work in particular explores Wells-Dawson's class of polyoxometalate (POM) molecules, which are inorganic metal-oxide-nano clusters formed from early transition of metal ions and

oxo ligands, These molecules are extensively studied in [12]. The work presented in this chapter has been done in a collaboration with several groups across the school of engineering as part of the EPSRC Molecular MOS project. Lee Cronin's group was involved with synthesis, characterization, electrochemical analysis, electron paramagnetic resonance (EPR) studies, crystallography, density flow theory (DFT) calculations whereas Asen Asenov's group was responsible for industrial level device modelling of the POM clusters by encapsulating them in the FG of a single transistor flash memory cell. However the practical devices i.e. 2 terminal nanowires for sensing POM molecules and side-gated FETs to realize flash memory operation using POM molecules were fabricated, tested and analysed by myself.

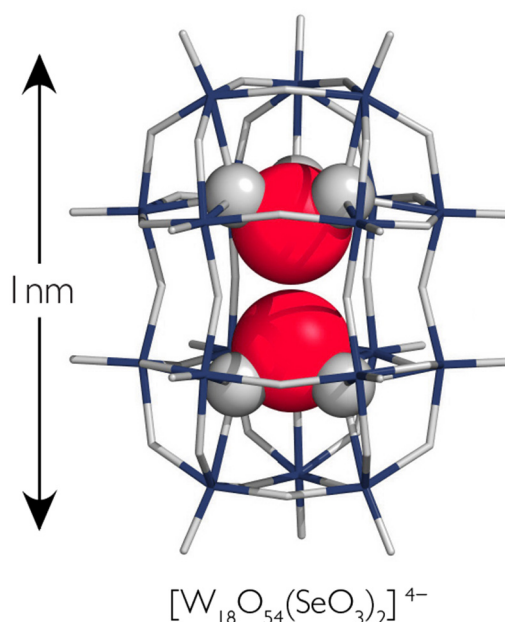


Figure 7-1: A selenium-based polyoxotungstate inorganic redox active (parent) molecule.

### 7.1. Polyoxometalate (POM) Molecules

POM molecules are nano-scale sized (*ca.* 1.2 × 1 × 1 nm) molecules having highly charged poly-anions, electronically (redox) active metal-oxygen clusters and have exceptional thermal stability (*ca.* 600 °C), moreover the multiple redox states of POM molecules can allow to realize multi-bit storage cells. Thus POM molecules are potential candidate to be used for the integration in molecular flash memory devices with current MOS technologies. The POM molecules are Dawson-like archetype with general formula  $\{\text{M}_{18}\text{O}_{54}(\text{XO}_3)_2\}^{m-}$  where M = Mo

or W, X = P, S or Se, n = 3 or 4 and m = 2 to 8. Thus the core-shell nature of POM molecules allows dopants to be included to control the electronic behaviour at the molecular level [13]. The doping of metallic cage by various materials allows to modulate the electronic properties of the molecular capsule especially if electronically active templates are embedded [14].

The thermal stability of tungsten based clusters are better than molybdenum, also density functional theory (DFT) calculations allowed to understand the reactivity and electronic structures of the clusters to choose appropriate heteroatom [15]. After careful considerations it is been found that  $\{\text{Se}^{\text{IV}}\text{O}_3\}$  would provide optimum balance in terms of structural stability and electronic reactivity, concluded that the cluster anion  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  would be most suitable candidate to explore molecular flash memory devices. Figure 7-1 shows ball-and-stick illustration of the atomic structure of  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  where two core Se dopants (shown by red balls) bonded with three O atoms (shown by grey balls) each and encapsulated in a cluster cage of W and O atoms (shown by blue and grey sticks respectively). These molecules are synthesized via dehydration of two selenite containing clusters  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2(\text{H}_2\text{O})_2]^{8-}$  by a cation exchange reaction in which the cluster undergoes dehydration and rearrangement of the tungsten scaffolding.

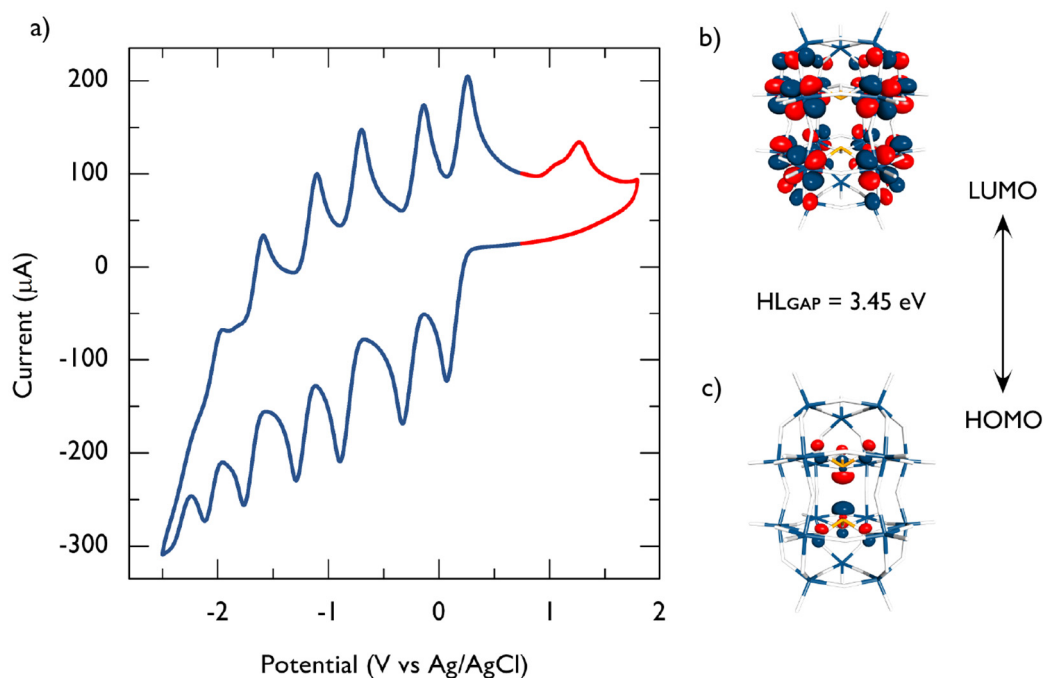


Figure 7-2: a) Cyclic voltammetry plot of the  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  molecules and illustration of atomic structure of molecules in b) LUMO and c) HOMO states.

The core elliptical shell of the  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  molecules is  $\sim 1$  nm in length and accommodates two anions in their intermediate oxidation state  $[\text{Se}^{\text{IV}}\text{O}_3]^{2-}$  and demonstrates exceptionally rich redox behaviour associated with the reduction and oxidation of the  $\{\text{W}_{18}\text{O}_{54}\}$  cluster cage. Figure 7-2a [22] shows the cyclic voltammetry of the  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  molecules, which is obtained from the microcrystals adhered to a glass carbon electrode (GCE) of diameter 1.5 mm in a 0.1M tert-butyl alcohol (TBA)  $\text{PF}_6$  acetonitrile solution at a scan rate of  $200 \text{ mV s}^{-1}$  and scanning range of -2.5 V to 1.8 V against Ag/AgCl electrodes. Figure 7-2a shows that the  $\{\text{W}_{18}\text{O}_{54}\}$  cluster cage can be reduced up-to six times by trapping an electron into the cluster (shown by top-blue peaks), whereas by reversing the sweep, the trapped electrons can be released from the cluster (shown by the bottom-blue peaks). Thus the cluster can undergo a series of reversible electronic states in addition to the oxidation of Se (shown by red peak) which result in a transition of  $\text{Se}^{\text{IV}} \rightarrow \text{V}$  and formation of a  $\text{Se} \cdots \text{Se}$  bond in an  $\text{O}_3\text{Se}-\text{SeO}_3$  moiety containing two  $\text{Se}^{\text{V}}$  within the cluster shell, (illustrated in figure 7-3d) feasibility of which was determined from DFT calculations. On the contrary reduction does not change the internal heteroatom and additional goes to the symmetry adapted orbitals [16]. The HOMO-LOMO gap ( $\text{HL}_{\text{GAP}}$ ) is the difference between the highest occupied molecular orbital (HOMO) and lowest un-occupied molecular orbital (LUMO). The  $\text{HL}_{\text{GAP}}$  of the parent molecules is 3.45 eV determined from the DFT calculations whereas upon oxidation the  $\text{HL}_{\text{GAP}}$  reduced to 2.01 eV. Figure 7.2b and 7.2c shows the illustration of atomic structure of the  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  molecule in LUMO (in reduced form) and HOMO (in its parent form) respectively. The LUMO are d-like and are generally delocalized over the metal centres connecting W-O-W by relatively large angles whereas HOMO are p-like and are primarily delocalized over the oxygen atoms [17,18]. It is worth mentioning that these orbitals don't form any bands because they are separated by discrete energy levels [19].

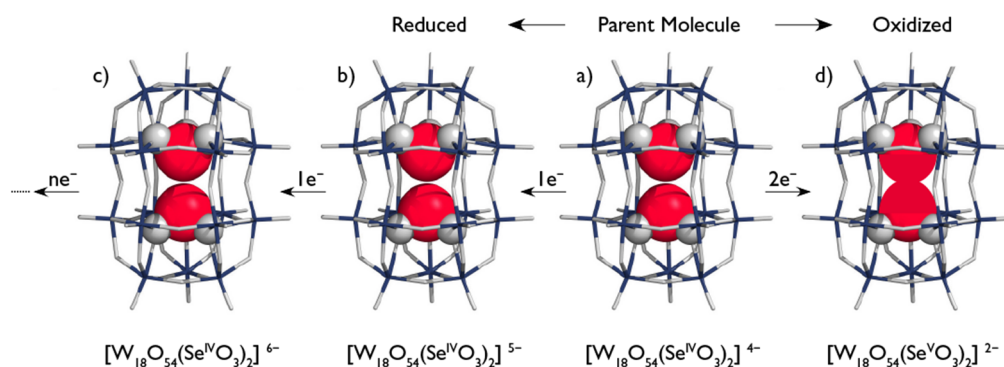


Figure 7-3: A summary of the redox behaviour of  $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$  molecule.

The  $[W_{18}O_{54}(SeO_3)_2]^{4-}$  molecule will now be referred as POM molecule for the rest of the text. The POM molecules are stable in both the solid state or in the dilute solution [20]. For example, acetonitrile solution is used as solvent to prepare a solution of POM molecules. The parent POM molecule has a charge of  $-4$ , which is balanced by  $+4$  counter-cations from the acetonitrile solution, so the parent POM molecule would be in its stable state with no net charge. When an electron is pumped-in to the POM molecule, the net charge becomes  $-1$ , so the molecule behaves like n-type. Similarly if 2 electrons are pumped-out from the POM molecule the net charge becomes  $+2$  and molecule behaves like p-type. So these POM molecules are highly redox-active and exhibit multiple and stable oxidation and reduction states which are reversible as evident from the cyclic voltammetry of the POM molecules shown in figure 7.2a.

## 7.2. Device Modelling

A multi-scale and multi-level computational framework is designed by the 'Device Modelling Group' in school of engineering to evaluate the possibility and perform realistic modelling and simulations of the POM molecules to replace them with the conventional polysilicon in a floating gate (FG) to realize a non-volatile molecular flash memory device, details of which can be found in [21,22] but some of the results are summarized in here for the clarity to link between the modelled and practical devices. Figure 7-4 [21] shows the illustration of a non-volatile flash memory cell designed with shallow trench insulation (STI) using 18 nm gate length n-type single transistor to deliver accurate results.

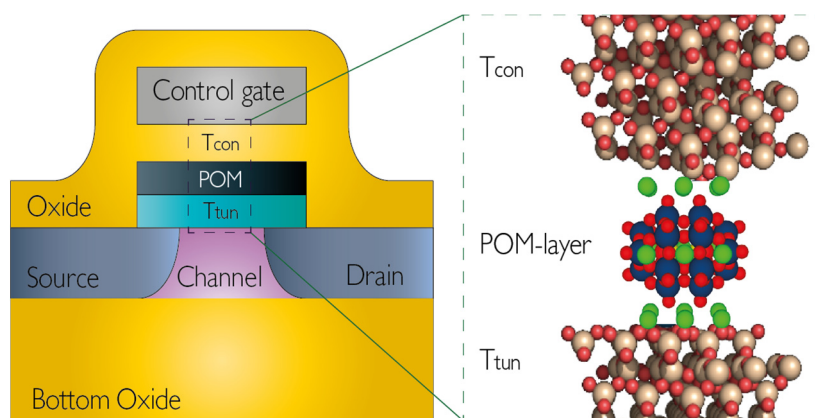


Figure 7-4: Illustration of a non-volatile flash memory cell based on POM molecules.



Figure 7-5 [21] shows the block diagram representation of the simulation methodology used to perform modelling of a flash memory cell. At first instance, density functional theory (DFT) simulations are done onto the POM molecules to determine the atomic charges and obtain the spatial charge distribution for the POM molecules at different redox states which are later transferred to the commercial three-dimensional (3D) numerical device simulator (GARAND) [23] via a custom build 'Simulation Domain Bridge' connecting two very distinct simulation softwares. This hierarchy allows to accurately analyse the POM molecules involving  $\sim 100$  atoms at molecular level and links it to the GARAND simulator which determines the current flow through the flash memory cell requires continues modelling at mesoscopic level involving millions of atoms [21].

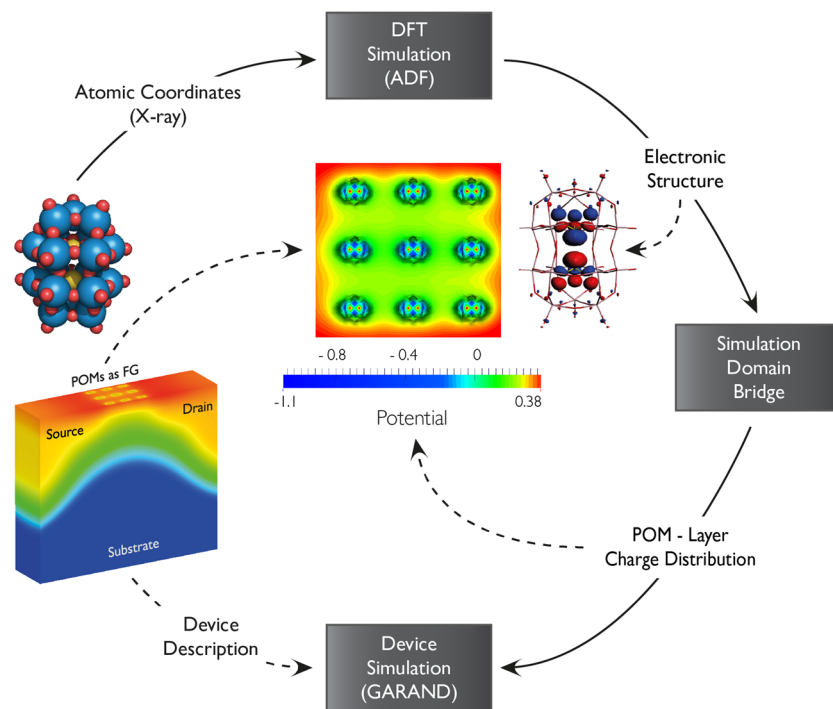


Figure 7-5: Illustration of the simulation methodology.

The DFT calculations gives insight into the POM molecules and helps to understand and analyse the structural, electronic and magnetic properties. Here the purpose of DFT was to extract the atomic and electronic structure of the POM molecules in a given redox state, but it is worth mentioning that these calculations can only be liable for individual molecules. The POM molecules are deposited in the FG either randomly or in a matrix of  $3 \times 3$  and a minimum number of 10 molecules were required to realize sufficient storage in the FG. The purpose of

simulation domain bridge was to generate a spatial charge distribution of the POM molecule in a given redox state taking account the counter-cations (from solvent) balancing the net charge onto the POM molecule. This spatial charge distribution (shown in figure 7-5) is imported to the GARAND simulator as a fixed fractional charge in the gate-oxide of the flash memory cell. This allows to realize the charge stored in the FG for various spatial and redox configurations and 3D numerical simulations were performed considering drift-diffusion transport mechanisms and density gradient quantum corrections required for accurate modelling [21]. Thus, transfer characteristics are calculated in this way to extract the programming window (the threshold voltage change between the charged and discharged molecule) [21].

In flash memory cell, the doping of the channel was  $\sim 5 \times 10^{18} \text{ cm}^{-3}$  to allow sufficient carriers in the channel adequate enough to maintain an electrostatic integrity at smaller length scales. Such high doping is also necessary to able to get a clear response from the charge stored in the FG on the drain current of the transistor which changes the threshold voltage and so the sub-threshold slope. The ratio between W/L is considered 1 for all the simulations which means the gate area is 18 nm square. The total thickness of the gate oxide ( $\text{SiO}_2$ ) is  $\sim 4 \text{ nm}$  whereas the POM molecules are deposited 1.5 nm apart from the channel, the modelling is mainly focused on the  $\Delta V_{Th}$  and sheet charge approximation (SCA) which is related to the gate oxide as follow [21],

$$Q_S = -qnN_S$$

$$\Delta V_{Th} = \frac{Q_S T_{CON}}{\epsilon_{Oxide}}$$

Where  $q$  is the electron charge,  $n$  is the number of times the POM molecules are reduced,  $N_S$  is the sheet density,  $\epsilon_{Oxide}$  is the permittivity of the gate oxide,  $T_{Tun}$  is the thickness of the tunnelling oxide (between the channel and the FG) and  $T_{Con}$  is the thickness of the control oxide (between the FG and the control gate). Thus SCA allows to compute  $\Delta V_{Th}$  as function of total number of POM molecules and associated charges, where  $\Delta V_{Th}$  entirely depends on  $T_{Con}$  and is independent of  $T_{Tun}$ . Here  $N_S$  is assumed  $\sim 3 \times 10^{12} \text{ cm}^{-2}$  and  $5 \times 10^{12} \text{ cm}^{-2}$  which corresponds to the 9 and 12 POM molecules in an arrangement of a matrix of  $3 \times 3$  and  $4 \times 4$  respectively separated by  $\sim 3 \text{ nm}$ . Figure 7-6 [21] shows the charge density as function of  $\Delta V_{Th}$  when POM molecules are reduced 1x and 2x for various thickness of

control oxide. For 7.8 nm control oxide,  $\Delta V_{Th}$  of 1.2 V is observed when 1 electron is trapped into the POM molecule. Whilst increasing the thickness of control gate increases the  $\Delta V_{Th}$  but may result in degradation of the electrostatic integrity. Since the conduction and the valence band edges of the  $\text{SiO}_2$  are far larger than the LUMO and HOMO of the POM molecules, it can provide strong insulation barrier for the retention of charges in the FG [21, 22].

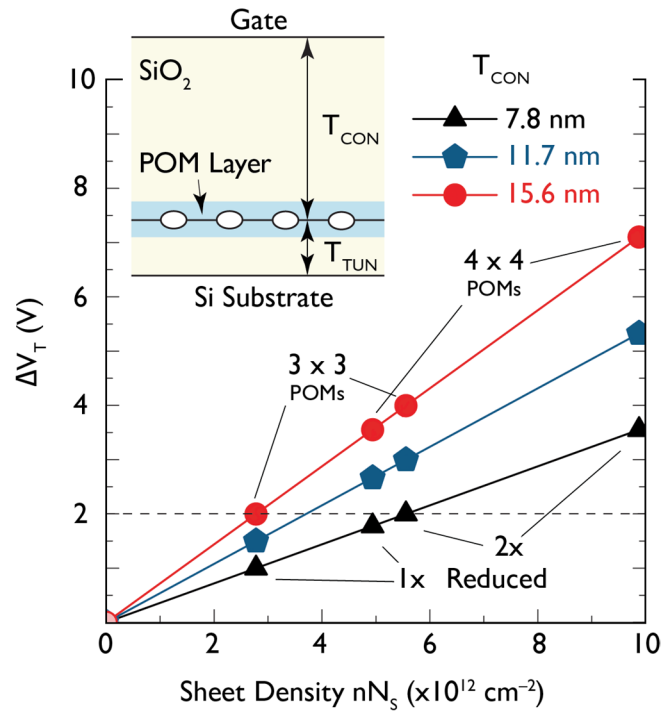


Figure 7-6: Sheet density as function of  $\Delta V_{Th}$  for various thickness of  $T_{CON}$ .

Figure 7-7 shows the current – voltage ( $I_D$ - $V_G$ ) characteristics of the flash memory cell measured at a drain voltage of 50 mV, here 9 POM molecules are placed in an arrangement of  $3 \times 3$  matrix. It clearly demonstrates that the while adding an electron to each parent POM molecule, the off current at  $V_G = 0$  is reduced by 3 orders, further when 2 electron been trapped in the POM molecule, the OFF current is reduced by 5 orders. Similarly when 2 electron are removed from the parent POM molecule, the OFF current is increased by more than 4 orders. This is due to the fact that the OFF currently is influenced by the electron density distribution of the channel and adding more negative charge in the FG will repel the electrons in the channel of the transistor. Change in the OFF current is evident from the change in the threshold voltage and for each time an electron is pumped into the POM molecule, the threshold voltage changes by  $\sim 1.2$  V at drain current =  $2 \times 10^{-6}$  A.

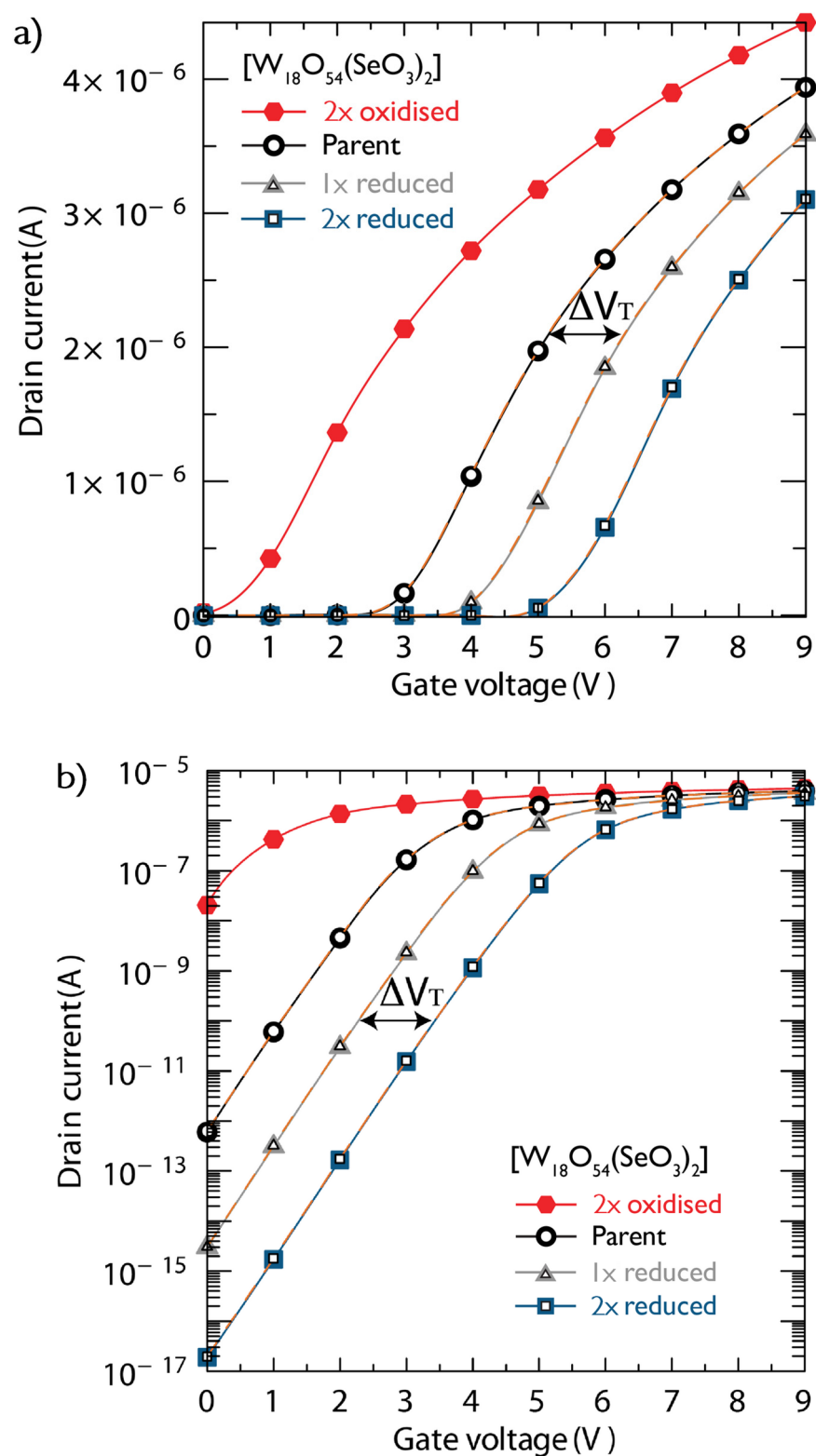


Figure 7-7: Transfer characteristics a) linear and b) logarithmic scale of the flash memory cell measured at drain voltage of 50 mV for POM molecules in the FG at various redox states.

### 7.3. Device Fabrication and Experimental Setup

In order to probe POM molecules and demonstrate molecule flash memory operation, initially 2 terminal nanowires were designed and fabricated with mean widths from 24 to 7 nm to be able to detect the presence of POM molecules on the nanowire surface. Furthermore side-gated FETs with mean width  $\sim 4$  nm are fabricated which is actually a Hall bar device with a side gate to able to demonstrate transistor characteristics. The purpose of side gate is to charge and discharge the POM molecules with alternative  $\pm$  pulses to determine any subsequent change in the threshold voltage and sub-threshold slope of the transistor. This configuration of side-gated FETs differs from the flash memory cell being modelled in section 7.2 but allows to deposit POM molecules at any stage and can provide sufficient evidence for the proof of concept. The device fabrication techniques used for the 2 terminal nanowire devices and the side gated-FETs are discussed in detail in section 4.1, the only exception is that the Al is replaced with Au for the bond pads deposited over Ni-Pd contacts to allow electrical characterization. Au is preferred because the POM molecules reacts with Al and overall surface being coated showed evidence of significant conduction between the bond pads. The layout for the pattern transfer is designed in similar way the Hall bar layouts are designed. The electron beam exposure parameters used for the pattern transfer of both kind of devices is shown in table 7-1.

	Dose ( $\mu\text{C cm}^{-2}$ )		Beam step size (nm)	Spot size (nm)
	2T-D	SGFET-D	2T & SGFET Devices	2T & SGFET Devices
Layer 1	3100	2500	2.5	3
Layer 2	2500	2000	5	3
Layer 3	2200	1800	25	33

**Table 7-1: Electron beam exposure parameters used for the pattern of the 2 terminal nanowire devices and side-gated FETs.**

Agilent B1500 semiconductor parameter analyser is used to perform all DC measurements onto the 2 terminal nanowires and side-gated FETs at 300 K. The POM molecules are delivered in a crystalline form the 'Cronin's Group – School of Chemistry' which

were dissolved in acetonitrile solution at a concentration of 2.5 mg/mL. The solution is then agitated in ultrasonic bath for ~ 5 minutes at 30 °C to ensure it is fully dissolved. The devices were then immersed in the solution for ~ 5 minutes and blown dry with the nitrogen gun.

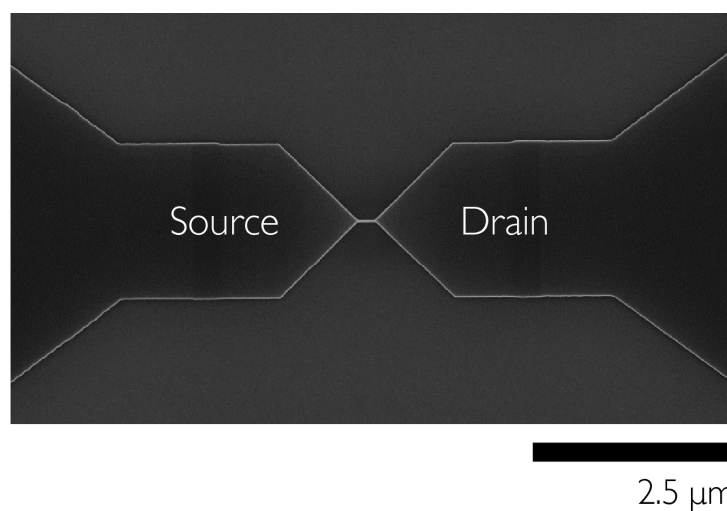


Figure 7-8: SEM image of a 2 terminal nanowire device with mean width ~ 7 nm used to detect POM molecules.

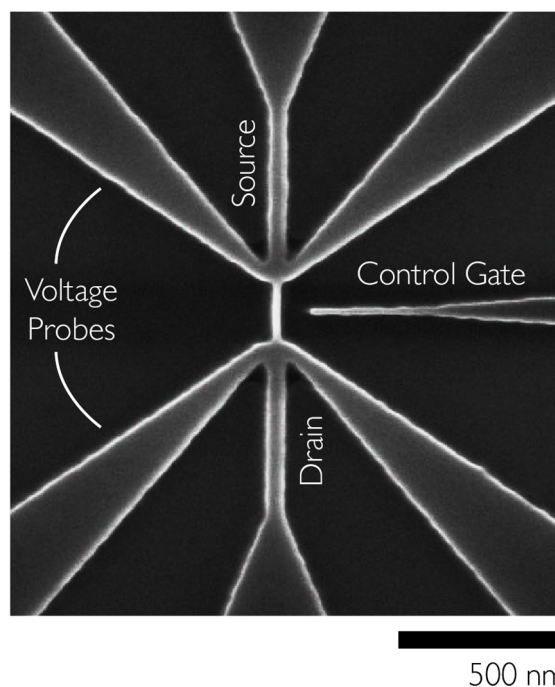


Figure 7-9: SEM image of a side-gated FET with mean width ~4 nm used to charge/discharge POMs to demonstrate flash memory operation.

## 7.4. Results & Discussions

The 2 terminal nanowires devices are fabricated on SOI substrate with a doping density  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$  in order to investigate any change in the resistivity of the nanowires due to the presence of POM molecules. Coating nanowires with any solvent result in some change in the surface potential due to change in the work function which certainly changes the resistivity of the nanowires. Since acetonitrile is the solvent used for the POM molecules, therefore at first instance, the resistivity of nanowires was being measured after devices been dipped in acetonitrile solution for few minutes and blow dry with the nitrogen to consider any effect from the solvent. Later, same devices were dipped in a solution of POM molecules and measured right after to determine any change in the resistivity.

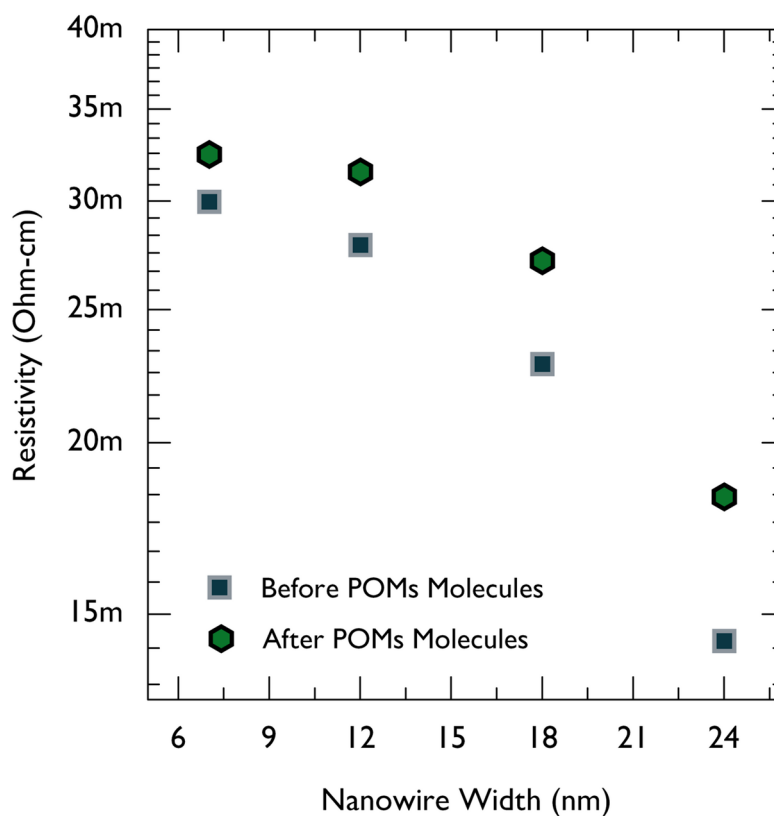


Figure 7-10: Change in the resistivity of nanowires coated with and without POM molecules.

The results from cyclic voltammetry and device modelling predicted that the parent POM anion has a net charge of  $-4$  but it will be balanced by  $+4$  counter-cautions from the acetonitrile solution, so the parent POM molecule would be in its stable state with no net charge. However

in reality that was not the case and a negative charge on the POM molecule has been observed. This could potentially be due the fact that not all the POM anions are being balanced by counter-cations and there are vast majority of clusters being unaffected or still has some negative charge. This is evident from the figure 7-10 that the resistivity of all the nanowires tend to increase after nanowires been coated with POM molecules, hence clearly indicates the negative (n-type) behaviour of POM molecules. The average change in the nanowire resistivity after nanowires been coated with POM molecules is  $\sim 3.6$  m ohm-cm which corresponds to  $\sim 13$  % increase in the resistivity. To confirm whether this change is due to negative charge associated with the POM molecules, not due to the electron heating expected in such thin nanowires, a voltage divider low noise / low current AC setup (similar to figure 6-8) is used to apply 0–5 mV across the nanowires, where the input voltage and output current is measured using lock-in-amplifiers. Similar results have been obtained with both DC and AC techniques which convinced that the change in nanowire resistivity is due to negative behaviour of the POM molecules and not all the clusters are in their stable state.

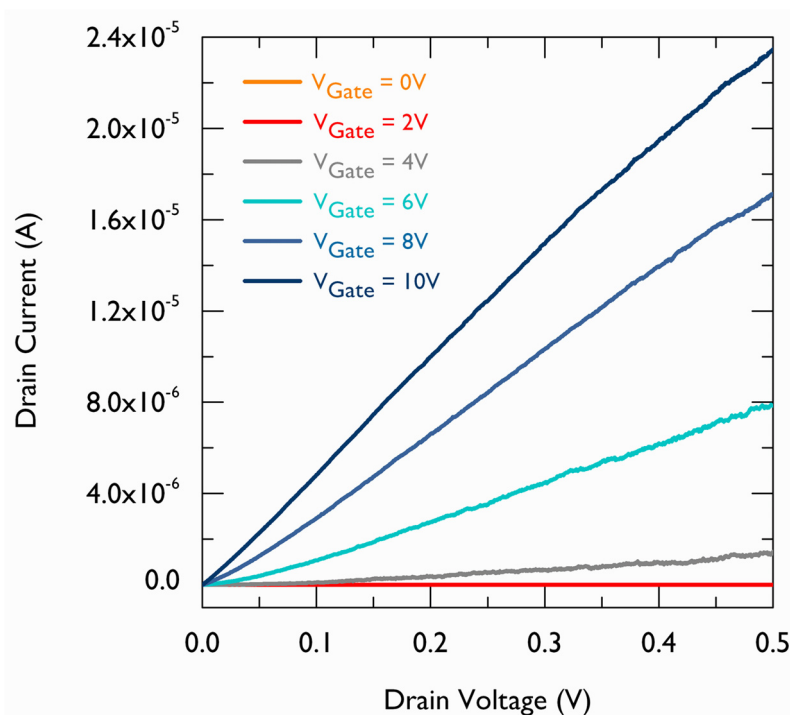


Figure 7-11: Output characteristics of the side-gated FET at different gate voltages in steps of 2 V.



To provide first demonstration of non-volatile flash memory device based upon POM molecules, side-gated FETs with mean channel width  $\sim 4$  nm were fabricated on SOI substrate with a doping density  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$  by introducing a side-gate to the Hall bar device. The side-gated FETs were designed and fabricated in an array of 9 independent devices where the distances from side-gate to channel was varied between 30 to 100 nm. From experiments a gap of 60 nm was found most suitable to deposit POM molecules between gate and channel and able to demonstrate reproducible results. Whilst the device was expected to a depletion mode FET but due to sufficient surface depletion, it turned out to be an enhancement mode FET. Figure 7-11 shows the output characteristics of the side-gated FET clearly demonstrates that high gate voltages are applied to turn on the transistor. The key advantage of this design over the modelled vertical flash memory cell is that the POM molecules can be deposited at any stage. Hence allows to measure the output and transfer characteristics of the transistor with/without POM molecules and charge/discharge the clusters by applying alternative  $\pm$  pulses from the side-gate and re-measure the transistor characteristics.

Figure 7-12 shows a) linear and b) logarithmic scale transfer characteristics of the side-gated FET measured at a drain voltage of 500 mV, demonstrates flash memory operation, measured at 300 K. Figure 7-12b shows the sub-threshold slope of the gated-FET without POM molecules been coated (blue), over 8 orders of enhancement in on-state drive current been observed where the ratio between the on and off-state current ( $V_G = 0\text{V}$ ) is more than 4 orders. A change in threshold voltage of  $1.1 \pm 0.1$  V has been observed from the bare nanowire to the nanowire been coated with POM molecules, indicates a sheet charge density stored in the POM molecules of  $\sim 2 \times 10^{15} \text{ cm}^{-2}$ . This is similar behaviour observed while determining the change in resistivity of nanowires with/without POM molecules being coated, that not all the clusters are in their stable state and there are significant number of POM molecules in their oxidation states. The OFF current at  $V_G = 0$  is reduced by more than 2 orders confirms the similar trend been observed in the modelled flash memory cell where the OFF current was reduced due to presence of POM molecules in their oxidation state. Later, side-gate has been used to apply large alternative  $\pm$  pulses to charge and discharge the POM molecules in order to exploit their redox nature.

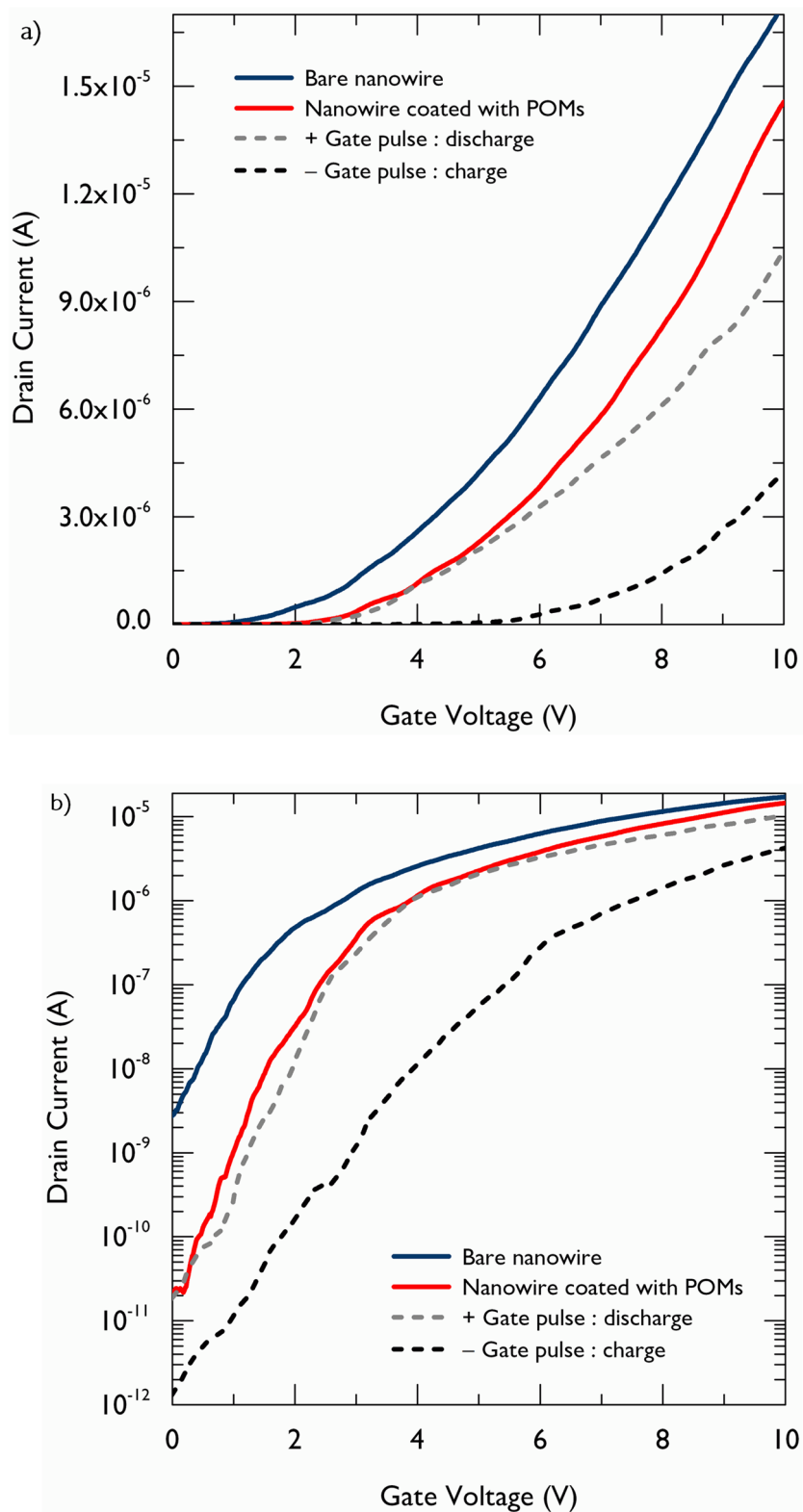


Figure 7-12: Transfer characteristics a) linear b) logarithmic scales of the side-gated FET measured at drain voltage of 500 mV with and without POM molecules and after alternative  $\pm$  pulses from side-gate to demonstrate flash memory operation.

Since a large gate voltage was applied to obtain transfer characteristics, so doubled the gate voltage is used (20 V) to apply the pulses, which is 40 MV/m between the side gate and the channel, well below the breakdown voltage of thermal oxide ( $\text{SiO}_2$ ) of  $10^9$  V/m, therefore it is very unlikely that thermal oxide around the nanowire is charging [24]. A gate voltage of  $-20$  V for 3 seconds is applied to inject the charge in the POM molecule above the LUMO energy state after which transfer characteristics were measured. A change in threshold voltage of  $1.2 \pm 0.1$  V (at  $10^{-10}$  A) has been observed demonstrating the POM molecules been charged with a negative potential, similarly a gate voltage of  $+20$  V for 3 seconds is applied to remove the stored charge from the POM molecules after which transfer characteristics measured again, demonstrating the POM molecules been discharged with a positive potential, hence the sub-threshold slope returned back to its original discharged state. There is more than an order of current varied in charging and discharging mechanism. This effect is highly repeatable and clearly demonstrates the programming window of  $\sim 1.2$  V at low gate voltages for charging and discharging the POM molecules. Whilst the current geometry of the side-gated FET is not optimized and high voltages are required to charge and discharge the POM molecules, figure 7-13 shows the logarithmic plot of program/erase time (pulse time) as function of change in the threshold voltage demonstrates that the present limit of program/erase time is limited by 100 ms. The charge retention time of POM molecules measured to be non-volatile for at least 2 weeks (336 hours). Whilst ultimate retention time is still not know but can be significantly longer, since no decay in the stored charge has been measured over the two 2 weeks.

The read time however is presently limited only by the RC time constant (i.e. product of resistance and capacitance:  $22.3 \text{ pF} \times 250 \text{ k}\Omega = 56 \text{ }\mu\text{s}$ ) of the channel and especially by the large bond pad capacitance. A radio-frequency (RF) design of the device and optimization of the capacitance and resistance should able to reduce this to sub-nanosecond read times. Moreover the write/erase time is also limited by the large density of POM molecules ( $\sim 2 \times 10^{15} \text{ cm}^{-2}$ ) and current compliance of the Agilent B1500 semiconductor parameter analyser. Preliminary calculations suggested that 100 POM molecules would have a sub-picosecond write time, subject to the device and characterization limits, but we expect the fundamental charging mechanisms of the POM molecules to dominate at such device dimensions. The above analysis clearly demonstrates that the ultimate performance of the POM molecules has not been reached and further work is required to determine the fundamental limits of the proposed

technology. The sub-threshold slope in charged state indicates additional charging mechanisms in the device in addition to the POM molecule charging and discharging mechanisms. This is because the POM molecules have been distributed over the entire device with high density, there are many potential charging mechanisms that could provide this type of non-optimal behaviour. The sub-threshold slope in discharged state also indicate that the return to the original state has not been completed, suggesting that optimization of the device geometry and POM molecule positioning is required to improve the performance. Nevertheless, these measurements demonstrate that it's possible to produce functional flash devices using POM molecules owing to their intrinsic n-type properties simply by drop-casting a solution of the POM directly onto the gate architecture in a one-step process.

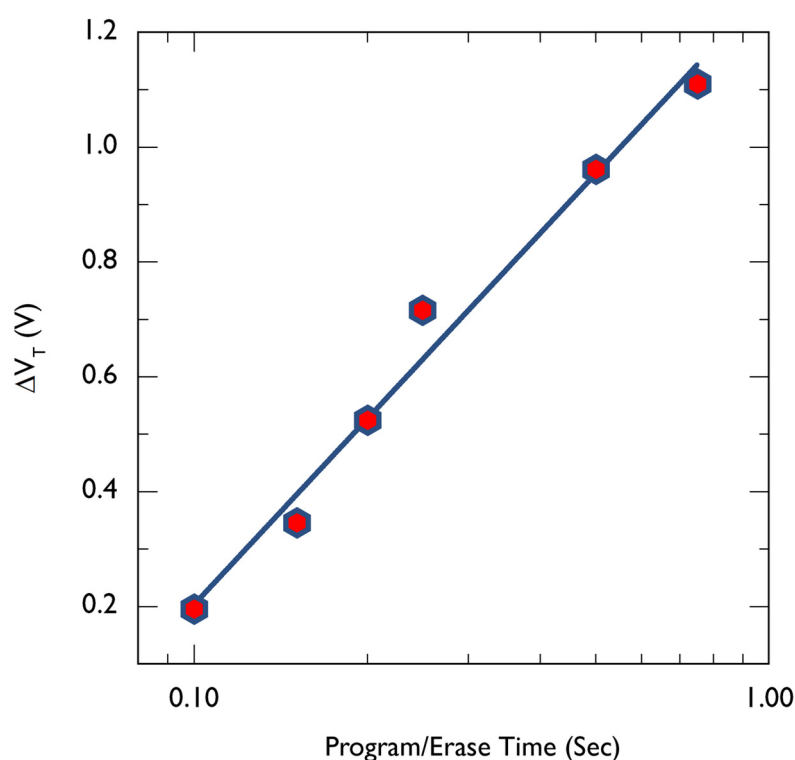


Figure 7-13: Change in  $V_T$  as function of pulse time applied from side-gate to charge and discharge (program and erase) the POM molecules.

## 7.5. Summary

Efforts has been made to demonstrate first ever POM molecules ( $[W_{18}O_{54}(SeO_3)_2]^{4-}$ ) based non-volatile flash memory devices. The POM molecules exhibit highly redox properties determined from the cyclic voltammetry indicated at least 6 reversible reduction states and an

oxidation state responsible for the transition of  $\text{Se}^{\text{IV} \rightarrow \text{V}}$ . DFT calculations are made to determine atomic charges and spatial charge distribution of POM molecules which are used for highly accurate modelling of molecular flash memory cell using GRAND simulator. These results are compared to the practical nano-scale fabricated devices. At first instance, 2 terminal n-type nanowires are used to probe the presence of POM molecules, results indicated that the resistivity of nanowires increased after POM molecules deposited around the nanowire, shown n-type behaviour of the POM molecules. Furthermore side-gated FETs are fabricated with mean widths  $\sim 4$  nm, where alternative  $\pm$  pulses ( $-$  for charge,  $+$  for discharge) from the side-gate were applied to charge and discharge POM molecules to demonstrate molecular flash memory operation. The average change in the threshold voltage was  $\sim 1.2$  V between the charging and the discharging cycles, which was predicted by the device been modelled. The program/erase time was limited by 100 ms for a reasonable single-to-noise ratio whereas the stored charge has been found to be non-volatile over the period of 2 weeks.

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## 8. Conclusions & Future Work

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Results are presented in previous chapters involves process optimization for patterning 10 nm features in negative tone HSQ resist using high resolution electron beam lithography, reactive ion etching 10 nm silicon nanowires for pattern transfer and thermal oxidation for high quality surface passivation for the fabrication of silicon nanowires devices on phosphorus doped silicon-on-insulator (SOI) substrate. The procedures and techniques developed to pattern 10 nm features in HSQ resist, are discussed in chapter 2. HSQ is widely acknowledged for producing high resolution features down to  $\sim 3$  nm but most of the demonstrations typically involved patterning in thin HSQ films  $\sim 30$  nm or below. One of the reason to use such thin films for patterning is the increase in surface tension as the feature size goes down and lines below 10 nm (with thicker resists) generally fell over. It's worth mentioning that HSQ is predominantly used as a dry etch mask for pattern transfer and thin HSQ layer is often inadequate for pattern transfer, especially if the etchant gas also etch resist and substrate at the same time.

Therefore, a process is optimized to produce high aspect ratio smaller linewidths with a view to etch deep in silicon. Initially, linewidths from 100 – 10 nm were designed and exposed with a dose ranging from 500 – 5000  $\mu\text{C}/\text{cm}^2$  with a spot size of  $\sim 3$  nm, beam step size of 2.5 nm at 100 keV accelerating energy. The linewidths were patterned in a thick HSQ resist  $\sim 150$  nm and developed after electron beam exposure with a range of 25% TMAH developer dilutions from 12.5% – 1.56%. That allowed to optimize the exposure dose and developer strength. Results indicated that an exposure dose of 2500  $\mu\text{C}/\text{cm}^2$  along with 6.25% TMAH provides the optimum balance to pattern 10 nm linewidths with great reproducibility. Moreover, with these optimized conditions, the effect of development time and temperature are also investigated. It has been observed that by weaken the developer strength, the development time between 60–120 seconds only varies the linewidths by  $\sim 1$  nm. However, the development temperature above 45 °C etches the exposed resist more vigorously and resist effectively reflowed when developed at 75 °C. Therefore we suggests that, 6.25% TMAH, 60 seconds development time and 23 °C development temperature are the ideal parameters at an exposure dose of 2500  $\mu\text{C}/\text{cm}^2$  to pattern 10 nm linewidths in thicker resist. Similar

process parameters were applied to 250 nm HSQ resist which allowed to produce 10 nm linewidths with 25:1 aspect ratio. This process has been extensively used throughout the course of research as it provided the optimum balance to pattern smaller linewidths with thicker resist. However this process is only be useful to pattern simple geometries with larger periods and gaps, because the resist contrast has been poorly affected when standard 25% TMAH developer strength weaken to 6.25%. When this process was used to pattern complex geometries, it was observed that the minimum achievable pitch was 50 nm with 30 nm resist thickness, which became even worst when thickness of resist was increased. Therefore, to achieve a higher contrast, the process is required to be optimized to a stronger developer strength and etch process should be optimized with a high selectivity, so thinner resists could be used to etch deep in substrate.

Chapter 3 describes the optimization of reactive ion etch process, where HSQ resist is used as a dry etch mask to fabricate of silicon nanowires with widths below 5 nm. Different etch chemistries have been investigated to etch silicon, such as  $\text{CF}_4$ ,  $\text{CF}_4/\text{O}_2$ ,  $\text{CF}_4/\text{CHF}_3$  and  $\text{SF}_6/\text{C}_4\text{F}_8$  where the effects of RF power, gas flow ratio and chamber pressure have been studied in detail. A large undercut  $\sim 30$  nm has been observed when silicon nanowires etched with  $\text{CF}_4$  based plasma because of excessive amount of F radicals, therefore  $\text{O}_2$  was introduced along with etchant gas to reduce the chemical reactivity of F radicals in the plasma, which although increased the sidewall protection but reduced the etch rate to 5 nm/minute and lowered the selectivity to 0.4. Also the 10 nm silicon nanowires were etched with a  $\sim 4$  nm undercut. We also attempted to etch silicon nanowires with  $\text{CF}_4/\text{CHF}_3$  based plasma, whilst vertical 10 nm silicon nanowires been able to etched but at an etch rate of 4 nm/minute with a poor selectivity of  $\sim 0.7$ . Such etch selectivity requires thicker resists to be used for patterning which limits the contract of the pattern due to the proximity effects. Moreover the bias voltage for the each process was monitored throughout the etching experiments, which varied between  $-77$  to  $-180$  V. Such high bias voltages are often associated with enormous plasma induced sidewall damages. In RIE tools, the bias voltage is directly related to the RF power, hence can't be independently controlled. However in ICP-RIE tools, the high density plasma is generated separately with a high coil power whereas a low platen power is generally used to etch the substrate. Thus allows to achieve higher etch rate at a low platen power. Therefore, with a view to develop a process to etch faster with a good selectivity and low bias voltage, I moved onto

the ICP-RIE tool where  $\text{SF}_6$  /  $\text{C}_4\text{F}_8$  based plasma was used to optimize a process to deliver smooth and vertical high aspect ratio (50:1) 10 nm Si nanowires at an etch rate of 110 nm/minute with a selectivity over 2.4. The averaged bias voltage of the process was  $-70$  V but to ensure low damage etching, the platen power was lowered from 12 to 6 W, which although reduced the etch rate to 80 nm/minute but significantly lowered the bias voltage to  $-23$  V to ensure high quality pattern transfer. That process is repeatedly used to fabricate a number of different types of silicon nanowire devices on SOI substrate.

After optimizing the processes for lithography and etching, another process is optimized to passivate the etched silicon nanowire devices with a high quality thermal oxide ( $\text{SiO}_2$ ) to remove dangling bonds and trap charges from the silicon interface. A dedicated furnace was used to thermally grow  $\sim 5$ -15 nm  $\text{SiO}_2$  oxide at  $950^\circ\text{C}$  for 80 seconds. The quality of oxide was determined from n-MOS capacitors made with  $\sim 10$  nm thermally grown oxide, where CV measurements made between 1 MHz – 10 KHz revealed the presence of mid-gap states in the thermally grown  $\text{SiO}_2$  with a large interface state trap density ( $D_{it}$ ) of  $2.3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ . Therefore, the capacitors were annealed in forming gas (5%  $\text{H}_2$ , 95%  $\text{N}_2$ ) at  $360^\circ\text{C}$  for 15 minutes, which significantly lowered the  $D_{it}$  down to  $1.3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  by passivating the remaining dangling bonds with  $\text{H}_2$ . The breakdown voltage of the thermally grown oxide is  $\sim 7$  V. Moreover, NiSi ohmic contact to n-type silicon also developed with a low specific contact resistivity of  $1.5 \times 10^{-9} \Omega\text{-m}^2$ , which has been determined from TLMs (shown in appendix).

Using above optimized processes for lithography, etch and thermal oxidation, a number of different types of silicon nanowire devices has been fabricated and tested on phosphorus doped 55 nm silicon on insulator (SOI) substrates. Initially silicon nanowires were fabricated with mean widths from 45 to 4 nm on SOI substrates with a doping density  $N_D = 2 \times 10^{19}$ ,  $4 \times 10^{19}$ ,  $8 \times 10^{19}$  and  $2 \times 10^{20} \text{ cm}^{-3}$  in a Hall bar and Greek cross configuration to determine resistivity as function of linewidths. A high depletion has been observed in the nanowires made on  $N_D = 2 \times 10^{19} \text{ cm}^{-3}$  but as the doping density was increased, the depletion effects significantly reduced and the conduction changed from non-linear to ohmic. Moreover, the transport properties were studied in silicon nanowires fabricated on substrate with a doping density  $N_D = 8 \times 10^{20} \text{ cm}^{-3}$ . The carrier density and mobility as a function of temperature for different widths was directly extracted from the Hall bar device. The carrier density has reduced whereas

the mobility increased as the width of nanowire has reduced, because of an increase in the surface depletion. The scattering mechanisms limiting the mobility in these nanowires has also been studied, where the experimental mobility was compared with a number of different theoretically calculated mobilities corresponds to various scattering mechanisms. It was determined that the neutral impurity scattering is the scattering mechanism limiting the mobility in fabricated nanowires. Moreover, various characteristic length scales such as mean free path for 3D, 2D and 1D transport are theoretically calculated and directly compared with the physical width of the nanowires. It has been approximated that the transport is likely to be 3D for nanowires with widths from 45 to 12 nm, whereas 2D and 1D for 7 nm and 4 nm nanowires respectively. It's worth mentioning that the depletion approximation no longer valid in these degenerately doped nanowires, so the correct screening length is Debye length which is theoretically calculated allows to determine the electrical width of these nanowires. Moreover, the donor deactivation and surface roughness, which are the major challenges in bottom up grown nanowires, have not been found to be significant in top down fabricated nanowires, indicates the importance of high quality surface passivation which confines the carriers in the channel.

To extract the carrier density and mobility, the Hall voltage is required to be measured accurately, which relies on the width of the voltage probes rather than the width of the channel. Here the Hall bar devices have been fabricated with  $\sim 50$  nm voltage probes for all the nanowire widths to reduce the access resistance and prevent any electron heating, but it came up a number of challenges. Measuring extremely small Hall voltage of orders of few  $\mu\text{V}$ , has been a challenge itself. Moreover, the geometrical uncertainty in measuring the carrier density increased as the width of nanowire was reduced. The Hall bar devices fabricated with channel width below 20 nm provided a value accurate to within a factor of 2 of the true value. For these reasons, the Greek cross devices were fabricated, which allowed to determine the carrier density with geometrical uncertainty below 1% even for the 7 nm wide nanowire. However both type of devices has produced almost similar results except for 4 nm wide nanowire which has shown an anomalous behaviour, probably due to a large geometrical uncertainty, which might have been related to change in the transport dimension, hence future work is required to fabricate devices according to the geometrical considerations mentioned in section 5.1.1.

Whilst the nanowires were etched very smooth and vertical, but the thermal oxidation has made them wider from the bottom and thinner because the oxidization is more towards the corners and sidewalls regions, whereas the foot is barely oxidized. This has not been a problem with wider nanowires, but as the lithographic width was reduced down to  $\sim 10$  nm, the oxidized nanowire has  $\sim 10.2$  nm foot and  $1.9$  nm top, hence turned out to be a tapered shape nanowire. The key disadvantage of such shape is that the transport also goes through the off-axis plane which is not desirable. Moreover the cornered nanowire is also not desirable, especially in a multigate architectures. Because the electric field at the corners is always amplified as compared with the sidewall of the nanowire, as a result the current density is generally higher at the corners than the sidewalls, which result in multiple threshold voltages operating in the channel due to premature inversion at the corners, hence lowers the overall sub-threshold slope of the transistor. Therefore, before the junctionless transistors were fabricated, the thickness of the top silicon layer of the SOI structure has been reduced from  $55$  nm to  $10$  nm, using a controlled reaction ion etching process. After patterning the junctionless transistors, the devices were  $20\%$  over etched to clear the foot, whereas before the oxidation step, the devices were dipped in the buffered hydrofluoric acid for a bit longer to remove the buried oxide under the channel region, which has allowed to thermally oxidize the channel equally from all the sides. Hence the channel has the round corners with minimized off-axis plane area, as compared with  $55$  nm etched nanowire. Thinning the silicon reduces the gate capacitance which in turn reduces the gate intrinsic delay, whereas rounding the corner eliminates electric field overlapping and allows a homogenous transition through all the three sides of the channel in a multigate transistor. I suggest that thinning the silicon using a reaction ion etch process is not a permanent solution and a process is required to be optimized to thin down the silicon using chemical mechanical polishing (CMP) tool.

Junctionless transistors with channel widths from  $24 - 8$  nm were fabricated on SOI substrate with a doping density  $N_D = 4 \times 10^{19} \text{ cm}^{-3}$ , where the channel length kept fixed to  $\sim 150$  nm. It has been observed that the transistors with wider channels has metallic conductivity but as the width is reduced to  $8$  nm, an increase in surface depletion makes the channel partially depleted to be operated in junctionless mode. A high drive current  $\sim 1.28 \text{ mA}/\mu\text{m}$  has observed for  $8$  nm wide transistor where the ratio between on/off was over  $\sim 10^8$  orders with a low SS of  $66 \text{ mV/decade}$  and  $V_{Th} \sim 0.18 \text{ V}$  at  $V_D = 1.5 \text{ V}$ . Moreover a low DIBL  $\sim 106.6 \text{ mV/V}$

has also been observed indicated reduced SCE as junctionless transistor has some immunity to SCE due to absence of PN junctions. However the threshold voltage extracted for the lower drain voltages was predominately negative. At  $V_G = 0$ , there is significant drive current in the channel of orders of  $10^{-6}$  A, whereas the off-state current ( $1 \times 10^{-14}$  A) is measured at  $V_G = -0.75$  V. The above issues can be easily addressed by using the multigate with a higher work function than aluminium (4.08 eV). We purpose that molybdenum or tungsten should be used, which has a work function varies between 4.36 – 4.95 eV and 4.32 – 5.22 eV respectively, can potentially shift the off-state current and threshold characteristics towards the positive values by more than a volt.

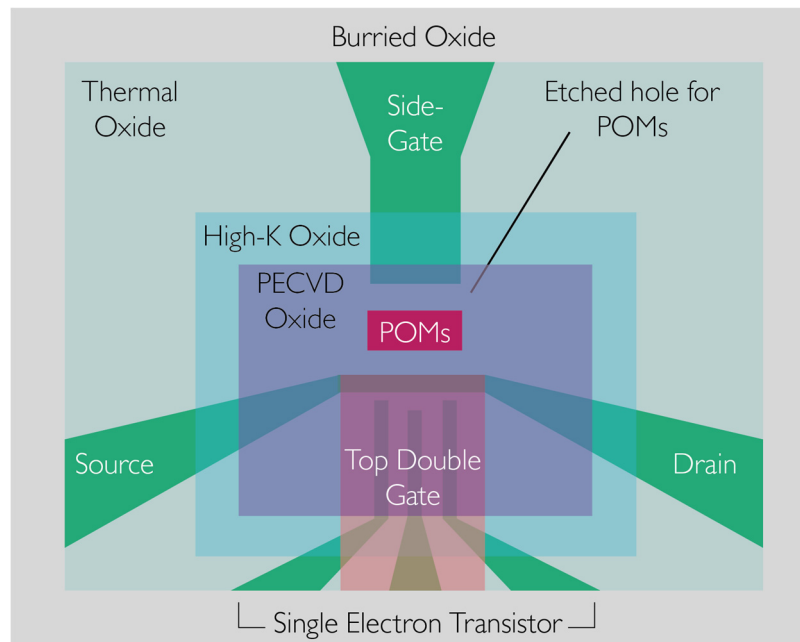
Moreover, the conformal deposition of tri-gate around the channel using standard electron beam evaporator tools has not really possible, especially if the surface is not clamped flat enough and fin is ultra-thin. We therefore purpose that tungsten should be sputtered as gate-all-around, which can provide enormous electrostatic control over the channel and can further improve the transistor characteristics. Moreover, after the thermal oxidation, high-k dielectrics such as hafnium oxide ( $\text{HfO}_2$ ) or aluminium oxide ( $\text{Al}_2\text{O}_3$ ) should be deposited over thermal oxide as a stop layer to etch tungsten gates using  $\text{SF}_6/\text{C}_4\text{F}_8$  based inductively coupled plasma. Since tungsten oxidizes in the air and the oxidized surface can provide a strong adhesion between the tungsten and the HSQ mask. Therefore patterning  $\sim 5$  nm HSQ lines over tungsten can scale down the fabricated  $2 \mu\text{m}$  gate down to a few nm. However, sputtering the tungsten film itself is quite a bit challenging. A process is required to be optimize to sputter a low stress tungsten film. Van der Pauw structures should be made on SOI substrate to measure the resistivity, carrier density and mobility before and after sputtering the tungsten film in order to investigate sputter induced damages caused by the direct current magnetron sputter coater. A few thoughts are to develop the recipe with low sputtering current, large source to substrate distance and high sputtering pressure to able to compromise between the density of the film and the sputter induced damages. Post-annealing tungsten could also help to reduce the damages. Moreover, the work function of the sputtered film should be determined from the MOS capacitors.

The polyoxometalates (POM) ( $[\text{W}_{18}\text{O}_{54}(\text{SeO}_3)_2]^{4-}$ ) are inorganic molecules, which exhibit highly redox properties with at least 6 reversible reduction states and an oxidation state

responsible for the transition of  $\text{Se}^{\text{IV} \rightarrow \text{V}}$ . DFT calculations made to determine atomic charges and spatial charge distribution of POM molecules which imported to the GARAND simulator to accurately model a non-volatile flash memory cell designed with shallow trench insulation (STI) using 18 nm gate length n-type single transistor. To experimentally evaluate the possibility of a molecular flash memory based upon POM molecules, initially 2 terminal nanowires were fabricated from mean widths from 45 – 7 nm on  $N_D = 8 \times 10^{19} \text{ cm}^{-2}$ . The change in the resistivity has been measured before and after devices been dip coated with a solution of POM molecules. Results indicated a consistent trend of an increase in the resistivity with presence of POM molecules around the nanowires. POM molecules changes the surface potential of the nanowire surface and from results we concluded that they are negatively charged. The POM molecule has a net charge of  $-4$ , after they are diluted with a solution of acetonitrile, ideally  $-4$  should be counter balanced by the  $+4$  of the acetonitrile, but we observed that not all the POM molecules went to their stable state and most of the clusters are still in oxidation state with negative charge.

I suggest that further work is required for a better understanding. For example, it's worth measuring the resistivity of nanowires after applying a positive bias of say 10 V from the back gate and measuring the resistivity after coating nanowires with POM molecules. Similarly, resistivity of nanowires should be measured after applying a negative bias of  $-10$  V from the back gate and measuring the resistivity afterwards. That would allow to understand that how surface potential of the nanowire device affecting the deposited POM molecules. Generally if the surface is pre-charged to +ive charges, the change in resistivity should be smaller after the deposition of POM molecules, similarly if the surface is pre-charged to -ive charges, the change in resistivity should be larger after the deposition of POM molecules. After detecting the presence of POM molecules on the nanowire surface. The side-gated FETs with mean channel width  $\sim 4$  nm were fabricated on SOI substrate with a doping density  $N_D = 4 \times 10^{19} \text{ cm}^{-2}$ . A change in the sub-threshold slope of the transistor has been observed after the deposition of POM molecules, which confirmed that clusters are negatively charged. Using a side gate, alternative  $\pm$  pulses ( $-$  for charge,  $+$  for discharge) were applied to charge and discharge POM molecules to demonstrate molecular flash memory operation. The average change in the threshold voltage was  $\sim 1.2$  V between the charging and the discharging cycles, which was predicted by the device been modelled. We observed that the program/erase time was limited

by 100 ms for a reasonable single-to-noise ratio whereas the stored charge has been found to be non-volatile over the period of 2 weeks. The read time however was presently limited only by the RC time constant ( $56\ \mu\text{s}$ ) of the channel and especially by the large bond pad capacitance. Therefore, RF design of the device and optimization of the capacitance and resistance should be able to reduce this to sub-nanosecond read times. Moreover the write/erase time is also limited by the large density of POM molecules ( $\sim 2 \times 10^{15}\ \text{cm}^{-2}$ ). Preliminary calculations suggested that 100 POM molecules would have a sub-picosecond write time, subject to the device and characterization limits, but we expect the fundamental charging mechanisms of the POM molecules to dominate at such device dimensions.



**Figure 8-1: Purposed design of a flash memory cell based on a double-gate junctionless transistor and a single electron transistor**

Generally the POM molecules are dissolved in acetonitrile solution at a concentration of 2.5 mg/mL. I suggest that the density of POM molecules should be reduced in order to lower the program/erase time to picosecond regime, one of the thoughts is to dilute the POM molecules in acetonitrile with different concentrations and embed them into a MOS capacitor between the gate and the oxide material. Ideally POM molecules are oxidized, hence they don't conduct and by embedding them in a MOS capacitor, we can determine the minimum change in the surface potential as a function of different concentration of POM molecules. That would



allow us to accurately determine the minimum density of POM molecules necessary to observe a clear change. Moreover, there are a number of drawbacks in the current geometry of side-gated FETs. For example the side gate was quite far from the channel  $\sim 50$  nm, which was mainly limited by the proximity effects, hence due to poor electrostatic control, normally high gate voltages were required to obtain the transfer characteristics. The same side-gate was used to charge and discharge the POM molecules and measuring the transfer characteristics, which could potentially charge and discharge the POM molecules at least twice, i.e. when pulses were applied to program/erase and when transfer characteristics measured again.

Therefore I propose a new design of a flash memory cell depicted in figure 8-1, which could explicitly able to program/erase the POM molecules and measure the transfer characteristics more efficiently by incorporating a side gate to charge and discharge the molecules and a double-gate junction less transistor to measure the transfer characteristics independently. The POM molecules should be embedded horizontally in the floating node between the channel and the side gate, by etching a deep trench in PECVD oxide. Instead of a tri-gate, a double gate architecture would allow to sense the presence of POM molecules on third side. Moreover, a single electron can be placed near the nanowire to probe the reduction and oxidation states predicted by cyclic voltammetry of the POM molecules (figure 7-2). Whilst the results for the single electron transistor has not been presented in the thesis but shown structure has successfully been tested, where two side (corner) gates were used to deplete the nanowire into a quantum dot and middle gate was used to observe single electron oscillations at 1.4 K with average charging energy  $\sim 100$  meV, the capacitance of the quantum dot measured to be  $\sim 0.8$  aF, suggests the quantum dot formed of orders of less than  $\sim 10$  nm.

The source and drain pads should be made as small as possible of orders of few  $\mu\text{m}$  and should be placed as close to the channel region. Moreover, via holes should be etched after deposition of thick PECVD oxide to access the source and drain contacts to evaporate large contact pads. Similarly, tungsten gate should be used to fabricate double gate over the channel and electroplated afterwards to copper using conventional T-gate techniques. These are some of RF design considerations, which should allow to optimize the flash cell to lower the read times.

## 9. Appendix

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### 9.1. Ohmic Contacts to the SOI Substrate

The nickel-silicide (NiSi) ohmic contacts are made onto SOI substrate doped with phosphorus to achieve doping density ( $N_D$ ) from  $2 \times 10^{19} \text{ cm}^{-3}$  to  $2 \times 10^{20} \text{ cm}^{-3}$ . There are a number of two and four terminal measurements undertaken throughout the project and both produced almost identical results. Each contact has a transfer resistance of  $0.3 \text{ } \Omega\text{-mm}$ , sheet resistivity of  $60 \text{ } \Omega/\text{sq}$  and specific contact resistivity of  $1.5 \times 10^{-9} \text{ } \Omega\text{-m}^2$ . Each contact is designed to have an area of  $5 \times 10^{-10} \text{ m}^2$  and by combining a square with a triangle narrowing to the nanowire allows to reduce the access resistance and resulting in each contact having an overall resistance of  $3 \text{ } \Omega$ . The resistance of the nanowires is typically above  $100 \text{ K}\Omega$  and the contact and access resistance is negligible in the measurements for  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$ . Hence, experimentally there is no differences found between two and four terminal measurements at any temperature.

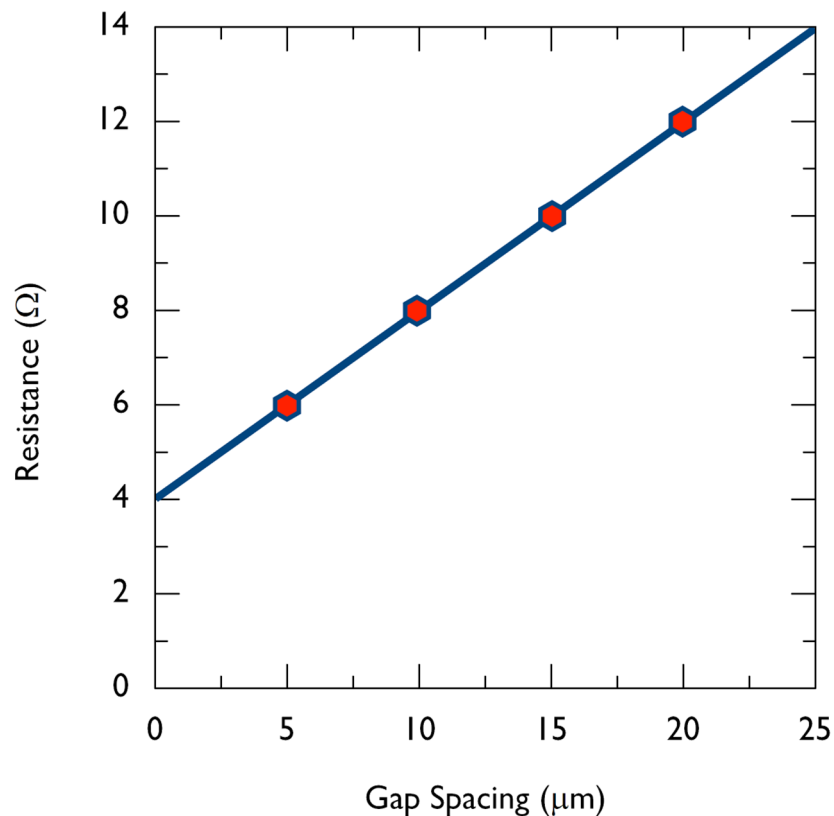


Figure 9-1: Data from a TLM device with an effective width of  $150 \text{ } \mu\text{m}$ .

The NiSi contact has a Schottky barrier height which has been measured to be 0.67 eV [1]. This contact is expected to be operating in the field emission regime provided that,

$$k_B T \ll E_{00}$$

Where  $E_{00}$  is given by,

$$E_{00} = \frac{q\hbar}{2} \sqrt{\frac{N_D}{m^* \epsilon_0 \epsilon_r}}$$

Where  $q$  is the electronic charge of an electron,  $\hbar$  is Plank's constant divided by  $2\pi$ ,  $\epsilon_0$  is the free space permittivity and  $\epsilon_r$  is the relative dielectric constant for silicon ( $=11.9$ ). This is true for the  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$  samples below 1077 K as the current density is dominated at all measured temperatures by the quantum mechanical tunnelling current through the Schottky barrier and the barrier width is kept small by the large doping density in the semiconductor resulting in a large current density and Ohmic behaviour. The specific constant resistance as a function of temperature can be calculated for this regime using [2,3]

$$\rho_c = \frac{k_B \sin(\pi c_1 k_B T)}{A^{**} \pi q T} \exp\left(\frac{q \phi_{Bn}}{E_{00}}\right) \quad \text{Eq. 9.1}$$

Where  $k_B$  is Boltzmann's constant,  $T$  is the temperature,  $A^{**}$  is the reduced Richardson constant ( $= 3.23 \times 10^5 \text{ A cm}^{-2} \text{ K}^{-2}$ ) and  $\phi_{Bn}$  is the Schottky barrier height (in V). The other undefined parameters are as follow,

$$c_1 = \frac{1}{E_{00}} \ln \left[ \frac{4\phi_{Bn} - V_F}{-\phi_n} \right]$$

$$\phi_n \simeq \frac{k_B T}{q} \left[ \ln \left( \frac{n}{N_c} \right) + 2^{-3/2} \left( \frac{n}{N_c} \right) \right]$$

$$\rho_c = g_s g_v \left( \frac{2\pi m_{de}^* k_B T}{\hbar^2} \right)^{3/2}$$

Where  $V_F$  is the forward bias voltage for the contact ( $=0.0196$  V for experiments),  $n$  is the measured carrier density as a function of temperature,  $g_s$  is the spin degeneracy ( $=2$ ),  $g_v$  is the valley degeneracy ( $=2$ ),  $m_{de}^*$  is the density of states effective mass and  $\hbar$  is Plank's constant divided by  $2\pi$ .

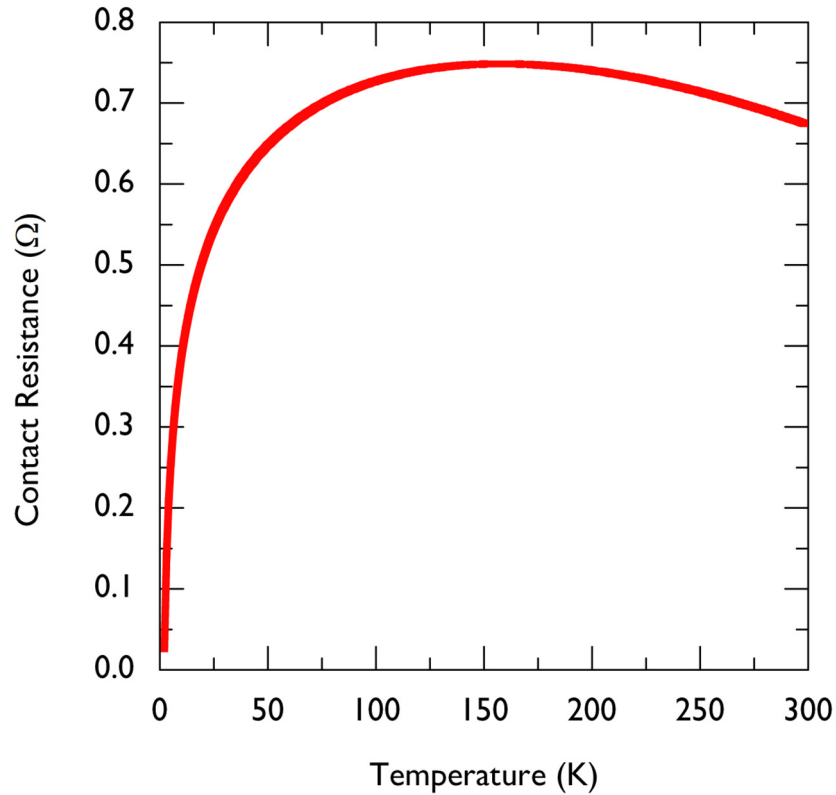


Figure 9-2: Temperature dependence of each Ohmic contact made the silicon nanowire doped at  $8 \times 10^{19} \text{ cm}^{-3}$ .

Figure 9-2 shows the calculated temperature dependence for a single Ohmic contact to the nanowire using equation 9.1 and area of the contact. Whilst there is a small increase, at the lowest temperatures the contact resistance decreases as the quantum mechanical tunnelling current density increases due to the reduction in thermal smearing. Figure 9-1 provides data from transmission line measurement (TLM) structure for the same doped sample which for a contact of area  $5 \times 10^{-10} \text{ m}^2$  provides a resistance of  $3 \text{ } \Omega$  which is the same order as the calculated value of  $0.7 \text{ } \Omega$  which excludes all other scattering mechanisms. Therefore for all the temperature for the  $N_D = 8 \times 10^{19} \text{ cm}^{-3}$  doped samples in this work, two and four terminal measurements produce nominally identical results.

## 9.2. Modelling of Scattering Mechanisms in Matlab

% Scattering processes as a function of Temperature for Si Nanowires

```

T = linspace(1,300,299); % Lattice temperature in K
rho = 2329; % Si mass density in kg/m^3
hbar = 1.054571726*10^-34; % Js
kB = 1.3806488*10^-23; % m^2kgs^-2K^-1
q = 1.602176463*10^-19; % C
epsilon0 = 8.854187817*10^-12; % permittivity of a vacuum F m^-1
mDOS = 0.328 * 9.10938215 * 10^-31; % Si DOS average electron mass in kg
mc = 0.269 * 9.10938215 * 10^-31; % Si conductivity average electron mass in kg
c11 = 165.77; % elastic constant in GPa
c12 = 63.93; % elastic constant in GPa
c44 = 79.62; % elastic constant in GPa
cL = (c12+ 2*c44 + (1/3)*(c11-c12-2*c44))*10^9; % in Pa
chiDelta = 8.6 * q; % Deformation potential for Delta-valleys in eV
N = 8*10^25; % ionized impurity density in nanowire in m^-3
epsilon = 11.9 * epsilon0; % relative dielectric constant
Z=1; % Number of charge units of the impurity centre
gD = 2; % donor degeneracy factor for doping;
omegaLO = (0.063*1.6*10^-19)/hbar; % LO phonon energy in rad/s
% NI = N./(1+gD.* exp((0.0096*q)/(kB.*T))) % ionised donor density -
% Jacoboni & Reggiani, Rev. Mod. Phys. 55(3), 645 (1983)%
% 12 nm nanowire n = (4.1906*10^25)-(T.*7.0065*10^22)+((T.^2).*9.6789*10^20)-
((T.^3).*1.3988*10^18); % cubic fit to measured carrier density in m^-3 for Si nanowire in
April 2014
n = (2.1465*10^25) - (5.6557*10^21).*T + (4.3998*10^19).*(T.^2) +
(7.1734*10^16).*(T.^3);
% NI = (4.0398*10^25)+(T.*3.409*10^21)+((T.^2).*3.3591*10^20); % quadratic fit to
measured carrier density in m^-3 for Si nanowire in April 2014
N0 = 1./(exp(hbar.*omegaLO/(kB.*T))-1); % Phonon occupation number

```

---

```

EF = ((hbar*(1.5*(pi^2).*n).^ (1/3)).^2)/(2*mDOS);
NI = (N)/(1+2*exp(EF-(0.00055*q)));
C = 0.5/q; %Non-parabolicity of the conduction band edge in eV-l
mstar = (mc*(1+2*C*((hbar^2)/mc).*(3*(pi^2).*n).^(2/3)));

%plot(T,N0);
DeltaE=0.063*1.6*10^-19; % Energy between initial and final valley for scattering process in J

% Acoustic Phonon Scattering - H. Morkoc "Nitride Semiconductor Devices" Wiley (2013)
muAP = (2*((2*pi)^0.5)*cL*(hbar^4)*q ./ (3 *(chiDelta^2) *(mstar.^2.5))) .* ((kB.*T).^(-
1.5))*10000; % mobility of acoustic phonon scattering in cm^2/Vs
%tauAP = (pi*(hbar^4)*cL)/((2^0.5)*(chiDelta^2)*(m^1.5));

% Ionised Impurity Scattering - H. Morkoc "Nitride Semiconductor Devices" Wiley (2013)
gamma = 24* epsilon * mstar .* ((kB.*T).^2)/(hbar*hbar*q*q*N); % for ionised impurity
scattering
gammaF = 4*(3^(1/3))*epsilon*(pi^(8/3))*(hbar^2).*(n.^(1/3))/((q^2)*mstar); % for
ionised impurity scattering in degenerate semiconductors
% mull = 10000*128 * ((2*pi)^0.5)*epsilon*epsilon .*((kB.*T).^1.5)
./(NI.*Z.*Z.*q.*q.*q.*(mDOS^0.5).*(log(1+gammaF) - (gammaF/(1+gammaF)))) ); % mobility
from ionised impurity scattering Brooks-Herring in cm2/Vs
mull = 10000*
((24*(pi^3)*(epsilon^2)*(hbar^3))./((Z^2)*(q^3).*(mstar.^2).*(log(1+gammaF) -
(gammaF/(1+gammaF)))).*(n./NI); % Degenerately doped ionised impurity scattering

%Optical Phonon Scattering - H. Morkoc "Nitride Semiconductor Devices" Wiley (2013)
chiDeltaLO = 11.0*10^10 * q; % J from Ferry "Semiconductors" Maxwell MacMillan (1991)
% chiDeltaLO =5.0 *10^10 * q; % from Ridley Quantum Processes in Semiconductors p113
%chiDeltaLO =5.6 * q; % J from Ferry "Semiconductors" Maxwell MacMillan (1991)
OpticalTemperature = hbar * omegaLO / kB % Temperature of change of scattering formula

```

```
muoptical =  
10000*(2^0.5)*pi*q*rho*(hbar^4)*((hbar*omegaLO)^0.5)/(((chiDeltaLO^2)*(mstar.^2.5)  
).*N0); % optical phonon scattering in cm2/Vs  
muoptical2 =  
10000*(2^1.5)*(pi^0.5)*q*rho*(hbar^2)*((hbar*omegaLO)^2)/(3*(chiDeltaLO^2)*(msta  
r.^2.5)*((kB.*T).^1.5)); % optical scattering in cm2/Vs above hbar omegaLO  
  
% Hamaguchi non-polar optical phonon scattering from C. Hamaguchi "Basic  
% Semiconductor Physics" Springer (2001)  
x0 = hbar.*omegaLO/(kB.*T);  
format long;  
fun = @(x) x.* exp(-x).*(1./(((1+(x0./x)).^0.5)+(exp(x0).*(1-(x./x0).^0.5))));  
gx = integral(fun,0,Inf,'ArrayValued',true,'RelTol',0,'AbsTol',1e-12);  
fx = (x0.^2.5).*(exp(x0)-1).* gx;  
muoptical3 =  
10000.*fx.*(4.*(2.^0.5)*q.*(hbar.^2).*rho.*((hbar.*omegaLO).^0.5))/(3.*(mstar.^2.5)*(chi  
DeltaLO.^2));  
semilogy(T,muoptical3,'k');  
  
% Intervalley phonon scattering  
omegaij = 0.063*q/hbar;  
gij = 4;  
Chij = 11*q;  
%a = hbar * omegaij/(kB.*T);  
%z = int(x*exp(-x).*(1./(((1+a/x)^0.5)+(exp(a).*(1-(a/x))^0.5))),x = 0..infinity);  
%g = (a.^2.5)*(exp(a)-1).*z  
%mulInterValley =  
(4*gij*(2^0.5)*q*(hbar^2).*rho*((hbar*omegaij)^0.5)/(3*(mDOS^2.5)*Chij^2)).*g;  
  
%Dislocation - H. Morkoc "Nitride Semiconductor Devices" Wiley (2013)  
Ndislocations = 10^5; % Dislocation density in m^-2  
space = 0.3*10^-9; % Spacing between donors
```

```

f = 1; % occupation of acceptor centres
Debye = (epsilon.*kB.*T./(q*q*n)).^0.5; % Debye screening length
% plot(T,Debye)
% muDislocations =
%
10000.*((8*(epsilon^2)*(2^1.5)).*(space.^2).*((kB.*T).^1.5))./(Ndislocations*(f^2)*(q^3)*
(mDOS^0.5)*Debye);
% % Mobility due to dislocations in cm2/VsMorkoc
muDislocations =
10000.*((30*(2^0.5)*(epsilon^2)*(space.^2)).*((kB.*T).^1.5))./(Ndislocations*(f^2)*(q^3)
*(mDOS^0.5)*Debye); % Mobility due to dislocations in cm2/Vs Seeger

% Interface roughness scattering - Motohisa, J.; Sakaki, H. Appl. Phys. Lett. 1992, 60,
1315-1317.
Delta = 2*10^-9; % Roughness height in m
Lambda = 1*10^-9; % Roughness correlation length in m
width = (7*10^-9)-2.*Debye; % width of Si nanowire in m
gammaRI = (hbar^2)*(pi^2)./(mstar.*(width.^3)); % Strength of scattering for quantum well
% kF = (n.^(1/3)); % Fermi wavelength in 1D
kF = (pi.*(n.*width)).^0.5; % 2D Fermi wavenumber
%kF = (1.5.*(pi^2).*n).^(1/3); % 3D Fermi wavenumber
EQ=epsilon.*(1+((q^2).*mstar)./(epsilon.*kF.*2.*pi.*(hbar^2)).*((hbar^2).*(kF.^2)./(2.*mst
ar))));
mulRS =
10000*(q*(hbar^3)./(2.*(mstar.^2)*(pi^0.5)*Lambda*(Delta^2).*(gammaRI.^2))).*kF.*exp
((kF.*Lambda).^2); % Interface roughness scattering from APL 60, 1315 (1992)
% mulRS =
10000*(((hbar^3).*(EQ.^2))./(pi*(mstar.^2).*(Lambda^2).*(Delta^2).*(q^3).*(n.^2))).*kF.
*exp(0.25.*((kF.*Lambda).^2)); % Interface roughness scattering from Hamaguchi
%plot(T,mulRS,'r');

% Potential well - H. Morkoc "Nitride Semiconductor Devices" Wiley (2013)

```



```

EB = 3.15*q; % Si/SiO2 barrier height in J;
muQW=10000.*(q*(mstar.^0.5).*EB./((2^1.5)*(pi^2.5)*(hbar^2)*n)).*((kB.*T).^(-0.5);

% plot(T,muQW,'r');

% Neutral impurity scattering - C. Erginsoy "Neutral Impurity Scattering in Semiconductors"
Phys. Rev. 79, 1013 (1950)
% and B.K. Ridley "Quantum Processes in Semiconductors" 2nd Ed OUP(1988)
% aB=(epsilon*4*pi*(hbar^2))./(mstar.*(q^2));
%muNI = 10000*q./(20.*aB.*hbar.*n);
muNI = 10000.*mstar.*(q^3)./(20*epsilon*(N-n)*(hbar^3));

% Mathesson's rule NB accuracy limited
mu = 1./((1./muAP)+(1./mull)+(1./muoptical3)+(2.*(1./mulRS))+(1./muNI));

%plot(T,mulRS,'k',T,mu,'r');
%semilogy(T,mulRS,'k');
semilogy(T,muAP,'b',T,mull,'r',T,muoptical3,'c',T,mu,'g',T,mulRS,'k',T,muNI,'m');
xlabel('Temperature (K)');
ylabel('Mobility (cm2/Vs)');

Tout=transpose(T);
muAPout=transpose(muAP);
muOpticalOut=transpose(muoptical3);
mullout=transpose(mull);
muNIout=transpose(muNI);
mulRSout=transpose(mulRS);
muOut=transpose(mu);
Output=[Tout,muAPout,muOpticalOut,mullout,muNIout,mulRSout,muOut];
dlmwrite('output',Output,'delimiter','\t','precision', '%.8f');

```

## References

- [1] J. P. Gambino, E. G. Colgan, "Silicides and ohmic contacts" *Materials chemistry and physics*, Vol. 52, No. 2, pp. 99 (1998).
- [2] C. R. Crowell, V. L. Rideout, "Normalized thermionic-field (T-F) emission in metal-semiconductor (Schottky) barriers" *Solid-state electronics*, Vol. 12, Issue 2, pp. 89 (1969).
- [3] S. M. Sze, K. N. Kwok, "Physics of semiconductor devices" 3<sup>rd</sup> edition, John Wiley and sons, New Jersey, USA (2007).