High Performance Terahertz Resonant Tunnelling Diode Sources and Broadband Antenna for Air-side Radiation

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Dedication

To my parents,

To my wife,

& to my children.

Acknowledgement

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Abstract

Resonant tunnelling diode (RTD) is known to be the fastest electronics device that can be fabricated in compact form and operate at room temperature with potential oscillation frequency up to 2.5 THz. The RTD device consists of a narrow band gap quantum well layer sandwiched between two thin wide band gap barriers layers. It exhibits negative differential resistance (NDR) region in its current-voltage (I-V) characteristics which is utilised in making oscillators. Up to date, the main challenge is producing high output power at high frequencies in particular. Although oscillation frequencies of ~ 2 THz have been already reported, the output power is in the range of micro-Watts. This thesis describes the systematic work on the design, fabrication, and characterisation of RTD-based oscillators in microwave/millimetre-wave monolithic integrated circuits (MMIC) form that can produce high output power and high oscillation frequency at the same time.

Different MMIC RTD oscillator topologies were designed, fabricated, and characterised in this project which include: single RTD oscillator which employs one RTD device, double RTDs oscillator which employs two RTD devices connected in parallel, and coupled RTD oscillators which combine the powers of two oscillators over a single load, based on mutual coupling and which can employ up to four RTD devices. All oscillators employed relatively large size RTD devices for high power operation. The main challenge was to realise high oscillation frequency (~ 300 GHz) in MMIC form with the employed large sized RTD devices. To achieve this aim, proper designs of passive structures that can provide small values of resonating inductances were essential. These resonating inductance structures included shorted coplanar wave guide (CPW) and shorted microstrip transmission lines of low characteristics impedances Z_o. Shorted transmission line of lower Z_o has lower inductance per unit length. Thus, the

geometrical dimensions would be relatively large and facilitate fabrication by low cost photolithography. A series of oscillators with oscillation frequencies in the J-band (220 – 325 GHz) range and output powers from 0.2 – 1.1 mW have been achieved in this project, and all were fabricated using photolithography. Theoretical estimation showed that higher oscillation frequencies (> 1 THz) can be achieved with the proposed MMIC RTD oscillators design in this project using photolithography with expected high power operation.

Besides MMIC RTD oscillators, reported planar antennas for RTD-based oscillators were critically reviewed and the main challenges in designing high performance integrated antennas on large dielectric constant substrates are discussed in this thesis. A novel antenna was designed, simulated, fabricated, and characterised in this project. It was a bow-tie antenna with a tuning stub that has very wide bandwidth across the J-band. The antenna was diced and mounted on a reflector ground plane to alleviate the effect of the large dielectric constant substrate (InP) and radiates upwards to the air-side direction. The antenna was also investigated for integration with the all types of oscillators realised in this project. One port and two port antennas were designed, simulated, fabricated, and characterised and showed the suitability of integration with the single/double oscillator layout and the coupled oscillator layout, respectively.

Publications

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[2] **K. Alharbi**, Ata Khalid, A. Ofiare, J. Wang, and E. Wasige, "Diced and grounded broadband bow-tie antenna with tuning stub for resonant tunnelling diode terahertz oscillators,'' Special Issue of the IET Microwaves, Antennas & Propagation journal (Re-submitted)

[3] **K. Alharbi**, Ata Khalid, A. Ofiare, J. Wang, and E. Wasige, "Diced and grounded broadband bow-tie antenna with tuning stub for resonant tunnelling diode terahertz oscillators," IET Colloquium on mm-wave and THz Engineering & Technology, London, 2016.

[4] **K. Alharbi**, Ata Khalid, A. Ofiare, J. Wang, and E. Wasige, "Broadband bow-tie slot antenna with tuning stub for resonant tunnelling diode oscillators with novel configuration for substrate effects suppression," European Microwave Week, London, 2016 (Accepted).

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List of Symbols and Acronyms

ADS: Advanced Design System

AlAs: Aluminium Arsenide

Au: Gold

BCB: benzocyclobutene

CPW: Coplanar Waveguide

DBQW: Double-Barrier Quantum-Well

DC: Direct Current

E-Beam: Electron-Beam

EBPVD: Electron Beam Physical Vapor Deposition

FIR: Far Infrared

GaAs: Gallium Arsenide

GSG: Ground Signal Ground

HBT: Heterojunction Bipolar Transistor

HCL: Hydrochloric Acid

HEMT: High Electron Mobility Transistor

HFSS: High Frequency Structure Simulator

H_2O: Water

H_2O_2: Hydrogen Peroxide

H_3PO_4: Phosphoric Acid

ICP-CVD: Inductively Coupled Plasma Chemical Vapour Deposition

IMPATT: Impact Avalanche Transit-Time

InAlAs: Indium Aluminium Arsenide

InGaAs: Indium Gallium Arsenide

InP: Indium Phosphide

IPA : Isopropyl Alcohol

LOR: Lift-off Resist

MBE: Molecular Beam Epitaxy

MMIC: Monolithic Microwave Integrated Circuit

N_2: Nitrogen

NDR: Negative Differential Resistance

NiCr: Nichrome

Pd: Palladium

PMMA: Polymethyl Methacrylate

PVCR: Peak to Valley Current Ratio

QCL: Quantum Cascade Laser

RF: Radio Frequency

RTD: Resonant Tunnelling Diode

SEM: Scanning Electron Microscope

S-parameters: Scattering Parameters

Si: Silicon

Si_3N_4: Silicon Nitride

SiGe: Silicon Germanium

TLM: Transmission Line Model

THz: Terahertz

Ti: Titanium

TD: Tunnel Diode

TUNNET: Tunnel Injection Transit-Time

UV: Ultraviolet

VNA: Vector Network Analyser

Symbols

ε_r :Dielectric Constant

J_p: Peak Current Density

ρ_C: Specific Contact Resistance

R_{sh}: Sheet Resistance

R_c: Contact Resistance

l_T : Transfer Length

ΔE_C: Conduction Band Offset

I_p: Peak Current

I_v: Valley Current

V_P: Peak Voltage

$V_{v:}$ Valley Voltage

Eg: Band gap

f_{max}: Maximum Oscillation Frequency

C_n : RTD Self-capacitance

Chapter 1 Terahertz Technologies: Sources

1.1 Introduction

Terahertz (THz) radiation usually refers to the frequency band which lies between millimetre-waves and infrared light in the electromagnetic spectrum. This is the frequency range between 300 GHz and 10 THz (free space wavelength (λ) between 1 mm and 30 μm) [1]. In other references, it also refers to the frequency band between 100 GHz and 10 THz [2]. This frequency band is located between microwaves and photonics bands in the electromagnetic spectrum as can be seen in the electromagnetic spectrum diagram in Figure 1.1.

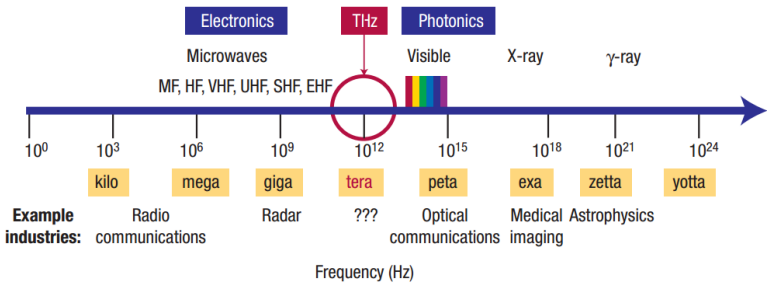


Figure 1.1: *Electromagnetic spectrum showing the terahertz location between radio frequency range and infrared spectrum* [1].

THz frequencies have many potential applications in different scientific fields such as medical diagnostic, security imaging, and wireless communication [3]–[6]. THz radiation is non-ionizing, and so it is safer than other ionizing radiation used for medical diagnostics, such as X-rays, which may produce physiological effects. In addition, THz radiation does not penetrate through metals or water but it does penetrate through many common materials such as leather, fabric,

cardboard, wood, clothing, plastic, ceramics, and paper, and so provides new sensing capabilities. Portable THz equipment would improve airport security where it can be used to identify dangerous materials. THz frequencies can offer very large bandwidths, in excess of tens of gigahertz (GHz). Thus, it has a potential for very high data rates of tens of gigabits per second (Gbps). However, THz technology suffers from the lack of efficient and practical radiation sources and sensitive detectors, and so part of the THz band is sometimes called the THz gap although, in the past few years, the improvement in photonic devices, microwave, and electronics devices has narrowed the THz gap as shown in Figure 1.2.

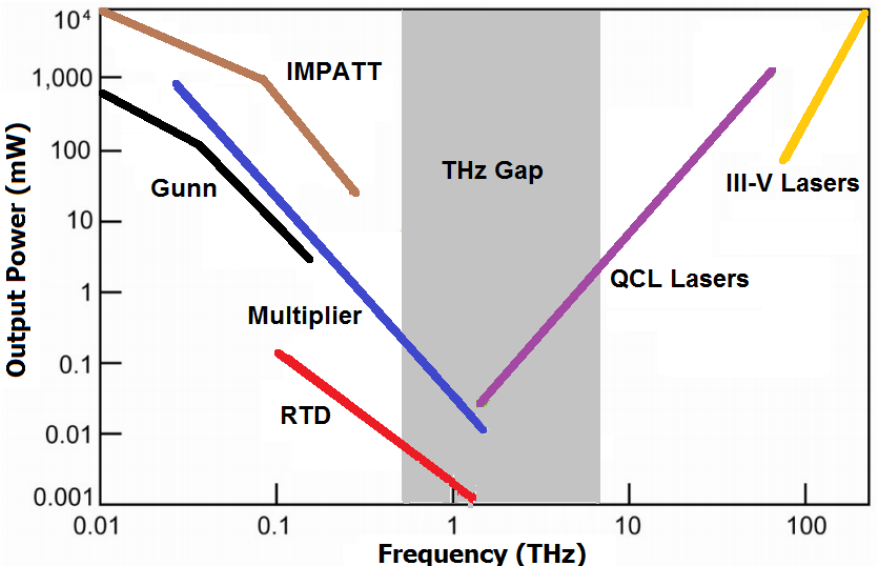


Figure 1.2: *Output power of different electronic and photonic sources around the THz gap. RTD: Resonant tunnelling diode. IMPATT: impact ionisation transit time diode. QCL: Quantum cascade lasers. (adapted from* [3]*).*

Since the THz band lies between microwaves and photonics bands in the electromagnetic spectrum, many efforts have been devoted to develop THz sources utilising devices commonly used in both neighbour bands. Quantum cascade lasers (QCLs) and far infrared (FIR) gas lasers can operate in the THz gap

[7], [8], and can emit tens/hundreds of milli-Watts power. However, both are bulky with QCLs requiring cryogenic cooling although QCL sources operating at room temperature but limited to >1 THz frequencies have been demonstrated recently [9]. In addition, they require high power to operate.

On the other hand, a variety of electronic solid-state oscillators have been studied for their potential in extending their output frequency toward THz region. Transistor-based sources, including high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are electronics devices that can operate at few hundred of GHz. The maximum oscillation frequency of the transistors (cut-off frequency$f_T = 1/(2\pi\tau)$) is limited by the carrier transit time (τ). For HEMTs, $\tau = L_g/v$ where L_g is the gate length and v is the drift velocity which is usually relatively low [10]. Therefore, to realise high oscillation frequency, the gate length L_g must be reduced. For example, HEMT devices with a cut-off frequency of over 1 THz was reported with sub 50 nm gate length [11]. For HBT, cut-off frequency of ~ 0.8 THz was reported with 12.5 nm base layer and 55 nm collector layer [12]. Both HEMTs and HBTs must be reduced in size (scaled) for realisation of higher frequencies and this introduces lithography challenges and increased contact resistance.

Diode-based sources such as Gunn diode, impact ionisation transit time (IMPATT) diodes, tunnel injection transit time (TUNNETT) diodes, and resonant tunnelling (RTD) diodes are common two terminal devices that have been considered as THz sources by exploiting the negative differential resistance (NDR) across the diode terminal. A Gunn diode (also known as transferred electron device (TED)), unlike usual $p - n$ junction diode, consists of N-doped semiconductor material. The Gunn device consists of three layers which are a thin layer of lightly n-doped material between two heavily N-doped on each terminal.

The NDR is formed due to electrons transfer from the high mobility lower valley (low effective mass) to the low mobility upper valley (high effective mass). As a result, the average electron velocity decreases causing a decrease in the current. Gunn diode oscillators with 85 μW at 480 GHz was reported [13], while higher power of 25 mW was demonstrated at 162 GHz with the device mounted on diamond heat sink [14]. The IMPATT diode is a p^+–p –n –n^+ junction diode which exhibits negative resistance attained from the avalanche breakdown and the carrier transit time across the diode. The TUNNETT diode is a variant of IMPATT diode that can generate higher oscillation frequencies due to the use of tunnelling mechanism instead of avalanche mechanism. Compared with IMPATT diodes, TUNNETT diodes can realise higher oscillation frequencies and lower noise but with lower output power. The highest reported oscillation frequency for the TUNNETT based source is 706 GHz with – 67 dBm output power [15], while IMPATT diode sources operating at 285 GHz and 115 GHz with output power of 8.8 dBm and 18.9 dBm, respectively, were reported [16]. However, the performance of the IMPATT diode is limited by the high noise levels produced during the avalanche multiplication process.

THz sources based on low frequency sources with multiplier chains to achieve the THz signal have been broadly used. Different results have been demonstrated with high frequency up to 2 THz [17]–[20]. In [19], 1.8 - 1.9 THz was reported with -30 dBm to -25.2 dBm output power, and 2.55 THz with -40 dBm was reported in [20]. However, the main disadvantage of multipliers chains is they require input signals that largely depend on the development of electronic solid-state sources. Also, they have low power efficiency.

The resonant tunnelling diode (RTD) is the fastest electronics device that can be fabricated in compact form and operate at room temperature with estimated

oscillation frequency up to 2.5 THz [21]. Fundamental oscillation frequency of 712 GHz was demonstrated in 1991 in waveguide technology [22]. Later in 2009, 831 GHz fundamental oscillation was demonstrated in planar integrated circuit technologies [23]. Frequencies above 1 THz were reported in the last few years [24]–[27]. Up to date, the highest reported oscillation frequency was 1.92 THz [28]. Theoretically, RTD-based oscillators can reach up to 50% DC-to-RF conversion efficiency [29]. However, the reported DC-to-RF efficiency for RTD oscillators is very low under 1%. Up to date, the main limitation of RTD-based oscillators is the low output power at THz frequencies in particular due to the use of small size RTD devices. Small device sizes are usually used in the oscillator circuits in order to reduce the device capacitance and realise higher oscillation frequencies as will be discussed throughout this PhD thesis. This project aims to raise the power level of RTD oscillators in the THz frequency range.

1.2 THz RTD-based Oscillators

In this section, historical perspective highlighting the state of the art of RTD-based oscillators is presented with emphasis on the approach toward achieving high frequency and high power operation. A description of the operational principle of a RTD device and an overview on the RTD material systems are given first.

A resonant tunnelling diode (RTD) device consists of a narrow band gap material (well) sandwiched between two thin wide band gap materials (barriers), making up the double barrier quantum well (DBQW) structure. The structure is completed by an un-doped or lightly doped spacer layer, an n-type emitter/collector layer and highly doped semiconductor material contact layer. Figure 1.3 shows a typical layer structure of a RTD device.

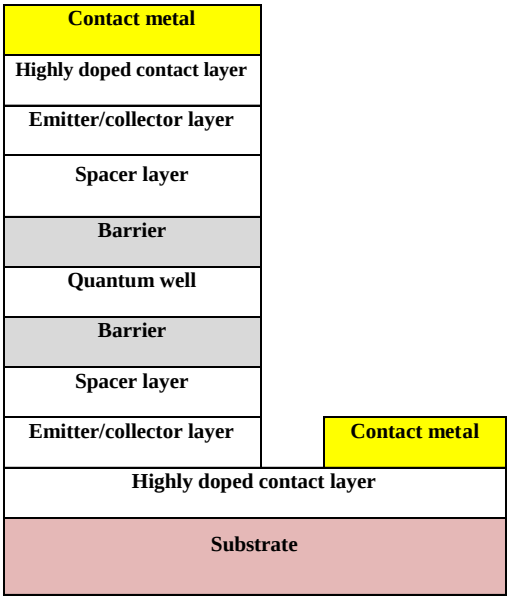


Figure 1.3: *Typical layer structure of the resonant tunnelling diode device.*

1.2.1 Operational Principle of RTD

The operational principle, and how the negative resistance is formed in the RTD structure, can be illustrated with the aid of the conduction band diagram of the double barrier structure at different applied bias voltages with the corresponding I-V characteristics as shown in Figure 1.4. By applying different bias voltages at the collector the following states occur:

- If no voltage is applied (**V_{bias} = 0 V)**, then the Fermi level of the emitter (E_{FE}) and the Fermi level of the collector (E_{FC}) are aligned below the resonant energy levels (E_{r1}) and (E_{r2}) as shown in Figure 1.4 (a). In this case, no current will flow due to thermal equilibrium.

- When small bias voltage is applied (**V_{bias} > 0 V)** at the collector, the energy levels in the well are moved down. When the first resonant energy level (E_{r1})

reaches the Fermi level of the emitter (E_{FE}), electrons can tunnel through the barrier structure leading to increased current. This case is illustrated in Figure 1.4 (b).

- With further increase in the bias, at some bias point (called peak voltage V_P), the first resonant energy level (E_{r1}) is moved down to the bottom of the conduction band of the emitter (E_{cE}) as shown in Figure 1.4 (c). At this bias point, the current reaches its maximum (I_p).

- When the applied voltage is increased further, the first resonant energy level (E_{r1}) is moved down below the conduction band of the emitter (E_{cE}) as shown in Figure 1.4 (d). The current then decreases and the negative differential resistance (NDR) region is formed.

- With further increase in the applied bias voltage, the second resonant energy level (E_{r2}) will further move down leading to another tunnelling process and increase in the thermal emissions of electrons causing rapid increase in the current over the barriers as depicted in Figure 1.4 (e). The bias voltage at which the current starts increasing is the valley voltage (V_v).

From the I-V characteristics of a RTD device, different key parameters can be calculated/extracted to estimate the performance when the device is employed in, for example, an oscillator circuit. Figure 1.5 shows the typical I-V characterises of a RTD device. The key parameters that can be extracted from Figure 1.5 include the peak-to-valley voltage difference ($\Delta V = V_P - V_V$), the peak-to-valley current difference ($\Delta I = I_P - I_V$), and the peak-to-valley current ratio$\left(PVCR = \frac{I_P}{I_V}\right)$. The two parameters ΔV and ΔI are used to estimate the maximum power (P_{max}) that a RTD-based oscillator can deliver to the load, which is given by $P_{max} = \frac{3}{16}\Delta V \Delta I$

[30]. They are also used to calculate the absolute value of the RTD negative conductance (G_n), which is calculated as $G_n = \frac{3\Delta I}{2\Delta V}$ [31], [32]. The value of G_n plays important role in impedance matching to the load and maximising the delivered power. More details will be given in Chapter 2.

The peak current density J_p can also be estimated from the I-V characteristics. It is usually expressed in kA/cm^2 or mA/μm^2 and estimated by $J_P = \frac{I_P}{A}$, where A is the RTD device area for which the I-V was measured. The value of J_p depends mainly on the layer structure of the device. High J_p device designs are usually used for THz RTDs since they require the use of submicron device sizes, with correspondingly small device self-capacitances.

The RTD self-capacitance C_n is also an important parameter when designing an oscillator circuit. It is used, with an external resonating inductor, to estimate the oscillation frequency in the oscillator circuit. The RTD capacitance is formed by the electron accumulation on the barrier in the emitter side, depletion in the collector region, and charging-discharging of quantum well region. Equation 1.1 gives a simple estimation of the RTD self-capacitance [33].

$$C_n = \frac{\varepsilon A}{d} \tag{1.1}$$

where ε is the permittivity, A is the RTD mesa size, and d is the thickness of the double barrier quantum well structure including the spacer layer.

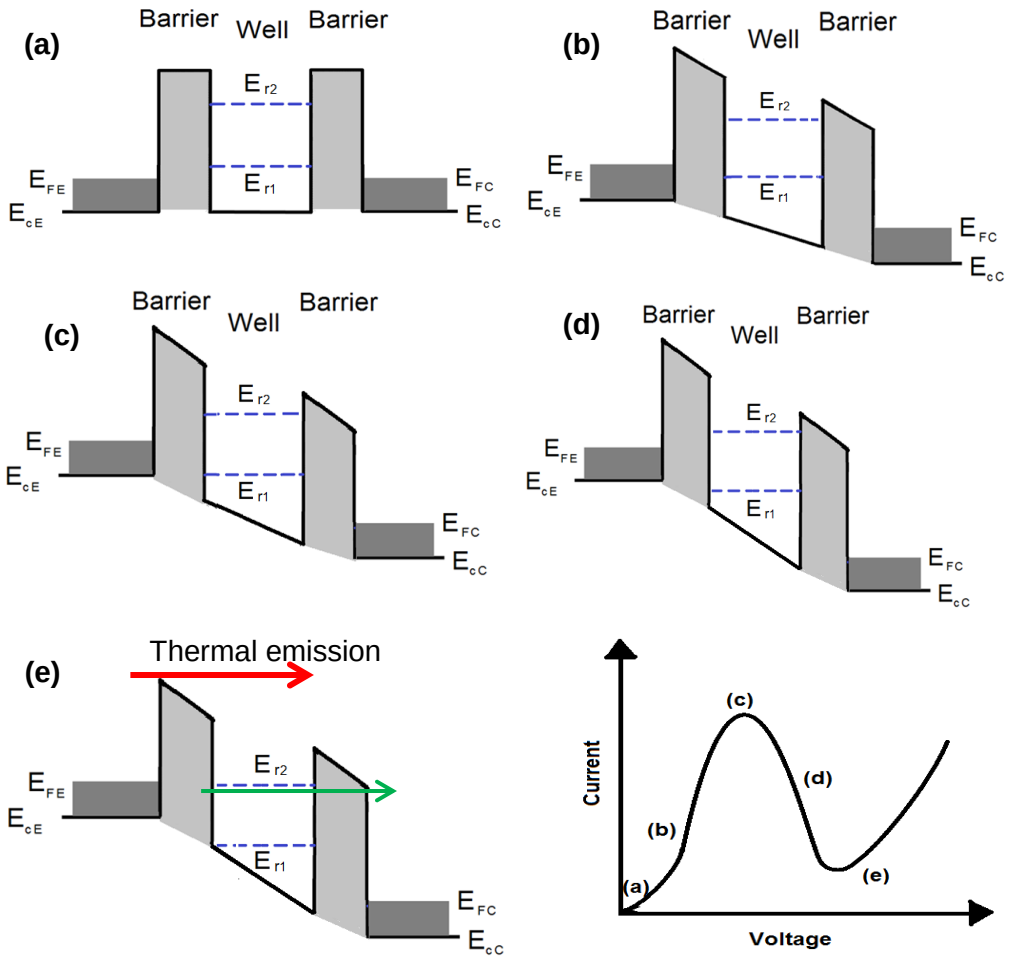


Figure 1.4: *Conduction band diagram of a double barrier quantum well structure and the corresponding I-V curve under different bias voltages. (a) No applied bias. (b) Small bias voltage (V_{bias} > 0). (c) Peak voltage (V_P) at which the current is maximum. (d) Negative differential resistance (NDR) region. (e) Valley voltage (V_v) at which the current increases.*

The bandwidth of an RTD is defined by the maximum frequency of oscillation f_{max} at which the RTD functions as an active device and can be estimated by [32], [34]

$$f_{max} \approx \frac{1}{2\pi C_n \sqrt{R_n R_s}} \tag{1.2}$$

where, $R_n = \frac{1}{G_n}$ and $R_s = \frac{\rho_C}{G_n}$, with ρ_C being the specific contact resistance. It can be noted from Equation 1.2 that, for a given RTD device size and layer structure, a large series resistance R_s (large ρ_C) will reduce f_{max} as will be shown throughout this thesis.

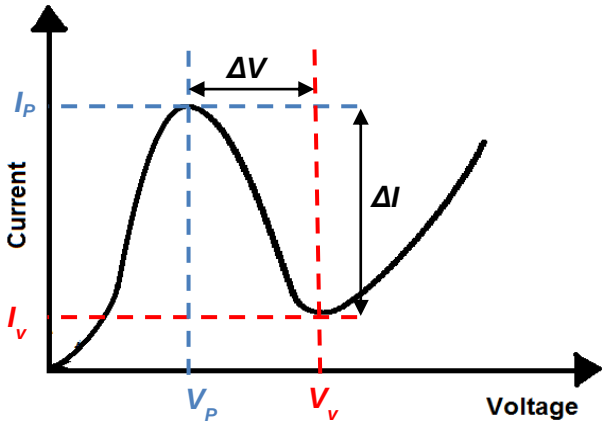


Figure 1.5: *Typical current-voltage (I-V) characteristic of a RTD device. V_P and I_P are the peak bias voltage and peak current, respectively. V_v and I_v are the valley voltage and valley current, respectively. ΔV denotes the peak-valley bias voltage difference while ΔI denotes the peak-valley bias current difference.*

1.2.2 RTD Device and Material Systems

Conventionally, RTD devices based on III-V semiconductor materials have been used due to the development in the epitaxial growth techniques which enable high quality nano-scale structures and, consequently, adjust the materials properties. The two main material properties include the electron effective mass (m^*) and the conduction band offset (ΔE_C). Small electron effective mass increases the electron mobility which leads to high current density (J_p), while high conduction band offset leads to high current density and improved peak-to-valley current ratio (PVCR) by suppressing the thermal current [35], [36]. RTDs are commonly realised in gallium arsenide (GaAs), indium phosphide (InP), and recently also in

antimonide based semiconductors. In addition, silicon-based RTDs are also being investigated with the potential of integration with silicon technologies.

Gallium Arsenide Based RTD ($GaAs/Al_xGa_{1-x}As$):

RTD devices based on $GaAs/Al_xGa_{1-x}As$ material system have been realised with different contents composition (mole fraction x) of Al and Ga. They employ gallium arsenide (GaAs) well sandwiched between aluminium gallium arsenide barriers ($Al_xGa_{1-x}As$). In 1974, a small negative differential resistance (NDR) region was demonstrated from a RTD device using $GaAs/Al_{0.7}Ga_{0.3}As$ at low temperature (77 K) by Chang et.al [37]. By changing the composition to $Al_{0.25}Ga_{0.75}As$, Sollner et.al in 1983 presented large PVCR of 6 at 25 K with theoretical frequency up to 2.5 THz [21]. Later in 1985, a PVCR of 1.5 at room temperature (300 K) was reported by Shewchuck et.al using $GaAs/Al_{0.25}Ga_{0.75}As$ [38]. In 1987, Huang et.al reported higher PVCR of 3.9 at room temperature with $GaAs/Al_{0.42}Ga_{0.58}As$ and a current density of ~7.7 kA/cm^2 [39]. A PVCR of 5.35 was reported from RTD devices using GaAs/AlAs by Forster et.al in 1994 [40]. The conduction band offset between GaAs and AlGaAs is around 0.23 eV [36]. The electron effective mass is $m^* = (0.067 + 0.083x)m_o$ for $Al_xGa_{1-x}As$ and $m^* = 0.067m_o$ for GaAs, while the specific contact resistance is around $10^{-6}\ \Omega.cm^2$ [41].

Indium Phosphide based RTD ($InGaAs/Al_xIn_{1-x}As$):

Indium gallium arsenide/aluminium indium arsenide ($InGaAs/Al_xIn_{1-x}As$) material systems have become more popular in RTD devices realisations. This is mainly because this material system offers better properties than what $GaAs/Al_xGa_{1-x}As$ systems do. For example, the conduction band offset in the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ is around 0.53 eV which is higher than that of the GaAs/AlGaAs system. Furthermore, the electron effective mass for $In_{0.52}Al_{0.48}As$

is $0.075m_o$ compared to $0.092m_o$ for $Al_{0.30}Ga_{0.70}As$, which leads to improved peak current density [36]. The $In_{0.53}Ga_{0.47}As$ can also be highly doped when used as the RTD device electrodes to reduce the Ohmic contact resistance [35]. Very high peak current density of 2800 kA/cm^2 with a PVCR of 2 was reported [42]. The highest reported RTD oscillator frequency was 1.92 THz [28] and was realised using InGaAs/AlAs material systems. The material system for the RTD device utilised in this project was InGaAs/AlAs. More details will be given in Chapter 3.

Indium Arsenide based RTD (InAs/AlSb):

Indium arsenide/aluminium antimonide (InAs/AlSb) material systems provide a number of advantages over GaAs/AlGaAs and InGaAs/AlAs systems such as the high conduction band offset (1.35 eV) and the low electron effective mass ($0.023m_o$ for InAs) [43]. It also provides lower specific contact resistance (10^{-9} $\Omega.cm^2$) than other material systems. A 712 GHz oscillation frequency was reported using this system in 1991 [22]. Large PVCR of 11 at room temperature and 28 at 77 K and peak current density of 100 kA/cm^2 were reported by Soderstrom et.al [44]. However, the low band gap of InAs (0.36 eV) leads to unwanted breakdown because of the impact ionization [45].

Silicon based RTD

RTD devices have the potential of integration with existing silicon (Si) technologies. They can be realised using silicon-based material systems such as silicon/germanium (Si/SiGe) [46], [47]. Memory and logic circuits employing RTDs would provide a number of advantages such as reducing circuit complexity, reducing power consumption, and enhancing high-speed operation [48]. RTDs fabricated using Si/SiGe system with peak current density of 282 kA/cm^2 and PVCR of 2.4 (which are comparable to the III-V RTDs performance) has been demonstrated at room temperature [47]. However, it was observed that peak

current density is inversely proportional to the device size due to the thermal limitations in the device structure.

1.2.3 State of the Art

1.2.3.1 Single RTD Oscillators

- As discussed above, RTD devices exhibit negative differential resistance (NDR) in their I-V characteristics and so have the potential to produce RF signals. The NDR exists from DC to THz frequencies. First reported RTD THz oscillators used quasi-optical resonator where the RTD device was mounted on a rectangular waveguide [29]–[31]. Figure 1.6 shows an example of this RTD oscillator technology. The resonator was realised by a metallic plate which acts as a semi-confocal resonator. A coaxial circuit was used as DC bias and the spurious oscillation was suppressed by a very lossy transmission line. The main limitation of this oscillator technology was the large inductance of the whisker contact and the series resistance which led to difficulties in stabilising the DC bias circuit.

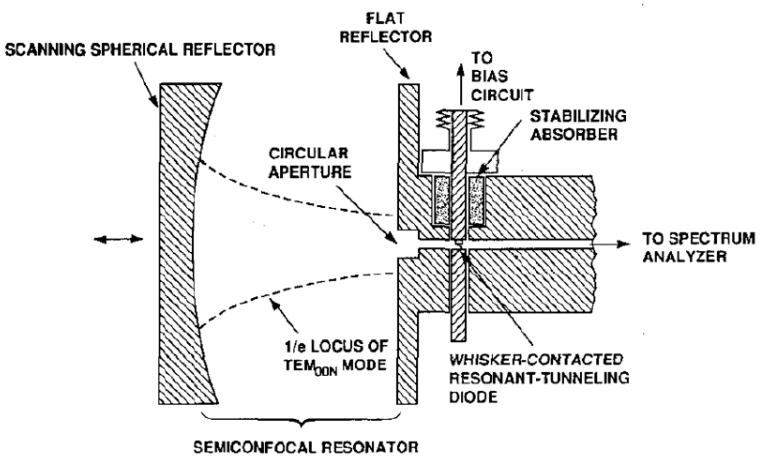


Figure 1.6: *Schematic cross-section of a quasi-optical RTD oscillator* [51].

- Planar RTD oscillators became more popular in the last few years where a single RTD device integrated with slot antenna was proposed and realised [27], [28], [52]–[57]. The slot antenna acts as a resonator and a radiator element at the same time. Figure 1.7 shows schematic structure of this oscillator circuit. The highest reported oscillation frequency was 1.92 THz with ~ 0.4 μW output power with 12 μm long slot antenna and ~ 0.1 μm^2 RTD device area [28]. The main challenge with this RTD-slot antenna integrated oscillator is the difficulty of impedance matching. The impedance of a slot antenna is infinity at the centre of the slot and zero at the edge of the slot. Thus, when the RTD device is located at the centre of the slot, the power will be extremely low due to the severe impedance mismatch. Relative increase in the power was observed by locating the RTD at different location in the slot to improve the impedance matching [54], [56], [58]. Since the slot antenna length is relatively short, and further reduces with increasing frequency, employing large RTD device would limit the impedance matching. For example, at 1.92 THz, a 12 μm long slot antenna was used [28]. This length is comparable to, for example, 4 μm^2 RTD device dimension. Thus, RTD devices with areas less than 1 μm^2 are usually employed at higher oscillation frequencies. In addition, small RTD device sizes (in the sub-micrometre range) are usually used in order to reduce RTD self-capacitance and, as a result, realise higher oscillation frequencies [59] since the resonating inductance is realised by the antenna and would be difficult to tune to the target oscillation frequency with a given device size. Furthermore, small devices in the sub-micrometre range require electron beam (e-beam) lithography which is more costly compared to fabrication of larger devices using photolithography.

High peak current density (J_P) (> 6 mA/μm^2) device designs have conventionally been used for THz RTDs since they require the use of submicron device sizes, e.g. 0.33 μm^2 for 1.31 THz [57] and ~ 0.1 μm^2 for 1.92 THz [28], with correspondingly small device self-capacitances [28], [57], [59], [60]. The main issues that may be attributed to high J_P RTDs include reduced thermal stability [59] and the need for ultra-low Ohmic specific contact resistances for the small-sized devices to keep the device contact resistance low [61], since high resistance limits the oscillator output power significantly [31].

The high J_P device designs typically employ ~1 nm aluminium arsenide (AlAs) barriers. The accurate growth of ultra-thin AlAs barriers is also difficult/challenging which limits the uniformity and so the manufacturability of the devices [62], [63]. Furthermore, such thin barrier thicknesses reduce the peak-to-valley current ratio (PVCR) to less than two (2) through the increased electron transmission probability through the DBQW. Therefore, the peak-to-valley current difference (ΔI) reduces and so also the potential output power of an oscillator using such a device reduces.

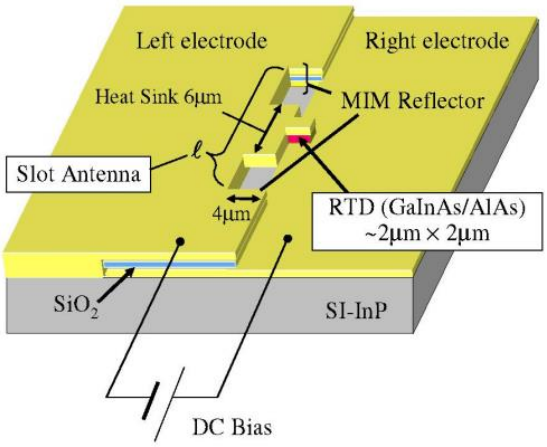


Figure 1.7: *Schematic structure of RTD-slot antenna oscillator* [54].

1.2.3.2 Power Combining Approaches

To increase the output power of the RTD-based oscillators, different power combining approaches have been reported. This sub-section discusses those approaches.

- An array of multiple oscillators placed close to each other has been proposed to increase the power of the RTD oscillator integrated with slot antenna [55], [64]. Here, each individual oscillator consists of a single RTD integrated with slot antenna. However, for each individual oscillator, the challenges with RTD-slot antenna integrated oscillator discussed above are still encountered. In addition, power combining occurs in some regions of space, and so inevitably there are regions at which the signals cancel each other out. This approach was pioneered by a group at the University of California, Santa Barbara (UCSB) in the 1990's [64] and recently revisited by Japanese researchers [55].

- A recent power combining technique developed by a group at Korea Advanced Institute of Science and Technology is based on triple-push oscillator topology has been reported [26]. In this oscillator topology, three sub-oscillators are connected to a single on-chip patch antenna. Each individual sub-oscillator employs a RTD device and an inductance realised by a coplanar waveguide (CPW) transmission line. The patch antenna radiates the signal generated from the three RTD sub-oscillators. Figure 1.8 shows the circuit schematic diagram of the triple-push oscillator. To achieve proper triple-push performance, the symmetry of the RTD sub-oscillators is essential and the three sub-oscillators have to operate at the same fundamental frequency oscillation f_o. The power combining occur only for the third

harmonic ($3 \times f_o$) signals, whereas the fundamental and the second harmonic signals cancel each other out [26].

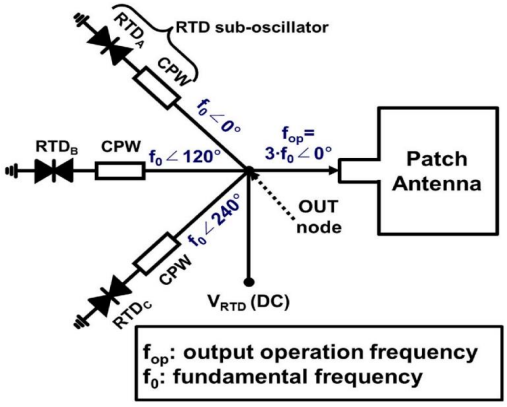
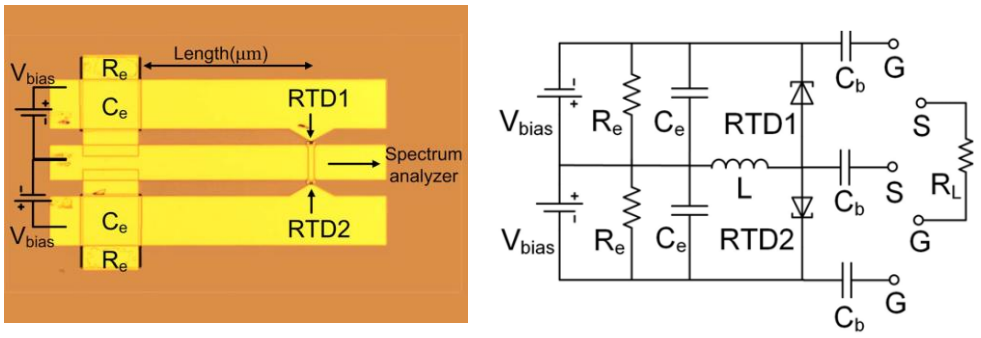


Figure 1.8: Circuit schematic diagram of the RTD oscillator integrated with an on-chip patch antenna [26].

- A power combining oscillator circuit topology that employs two relatively large RTD devices and deliver the output power to a single load has been reported and demonstrated by the group at the University of Glasgow. Figure 1.9 shows a photograph of a fabricated two RTDs oscillator in coplanar waveguide (CPW) technology with the corresponding schematic circuit. The elements in the schematic circuit are specified in the caption. In this circuit, there are two largest possible RTD devices A_{max} (according to the stabilisation criteria to supress the bias oscillations as will be described in Chapter 2) and each device is biased individually and connected to its own stabilising resistance, R_e. Therefore, limitations to the output power due to the bias oscillations are overcome. Alternatively, employing a single RTD device (with size equivalent to the two devices, i.e. $2 \times A_{max}$) would require a very small stabilising resistance ($R_e/2$) which would short circuit the DC supply/bias. Using this approach, 28 GHz and 76 GHz InP-based RTD oscillators with around 1 mW were realised [65], [66]. Thereafter, D-band

oscillators operating at 125GHz, 156GHz and 166 GHz, with output power of 0.34 mW, 0.24 mW, 0.17 mW, respectively, were also demonstrated [67].



(a) (b)

Figure 1.9: *The two RTDs power combining oscillator in CPW technology. (a) Fabricated oscillator. (b) Schematic circuit. Each RTD is biased individually with its own DC stabilization circuit R_e. C_e is the decoupling capacitor, R_L is the load resistance, L is the resonator inductance, and C_b is the DC-block capacitor to protect the spectrum analyser from DC bias voltage during on-wafer characterisation* [67].

The oscillator circuit employ large micro-sized RTD devices which do not suffer thermal stability issues and can provide high RF power in oscillator circuits due to the increased ΔI, and can be fabricated with low cost photolithography. Such circuits can employ low J_P designs, and so employ thicker barrier layers (~1.4 nm) as those used in Ref. [65]–[67]. Thus, the epitaxial growth requirements are therefore less demanding and more accurate benefiting a reproducible technology. High PVCR is achieved, and since for a given specific contact resistance, the larger size RTD devices exhibit low Ohmic contact resistance, these factors benefit higher output power in oscillator circuits.

In order to obtain high oscillation frequencies with the employed large RTD devices, the circuit employs shorted 50 Ω CPW line to realise the resonating inductance which can offer high accuracy of providing a required inductance

value. Therefore, the accuracy of estimating the oscillation frequency is high. However, the maximum attainable frequency (with employment of two large RTD devices for high power operation) is governed by the shortest CPW length. However, higher oscillation frequencies can be achieved with new structures that are able to provide very low resonating inductance values to compensate for the self-capacitance of the large RTD devices, as will be described later in this thesis.

From the discussions above, individual RTD oscillators exhibit low output power in the micro-Watt range in general, while high power in the milli-Watt range is desirable. To provide a perspective for this, practically relevant output powers of at least 10 mW at 90 GHz, 5 mW at 160 GHz and 1mW at 300 GHz are required [68].

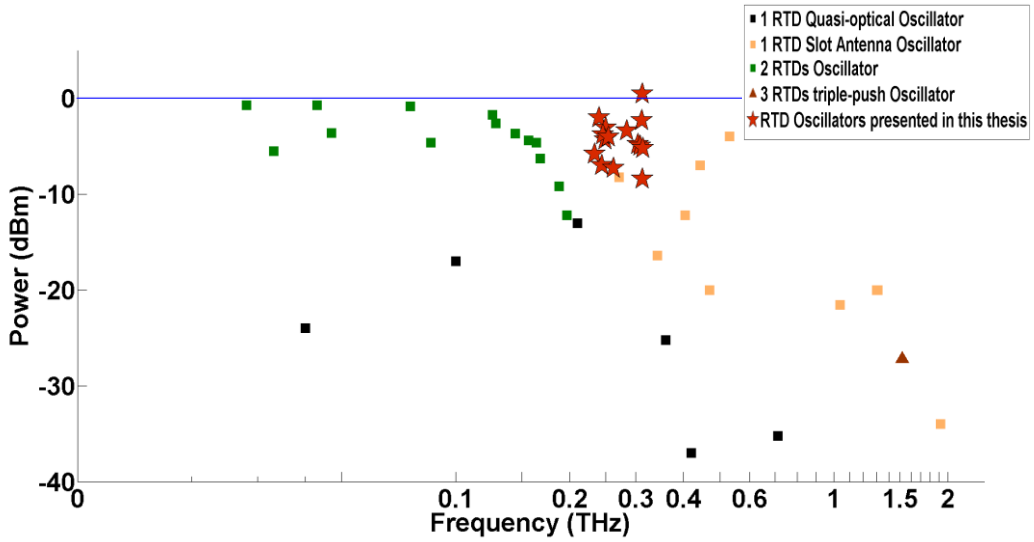


***Figure 1.10**: State of the art of RTD oscillator development* [22], [26]–[28], [49]–[51], [53], [56], [65]–[67], [69]–[72]. *Only oscillators employing a single (antenna) load are considered.*

The performance of different RTD-based oscillators having a single (antenna) load including RTD quasi optical oscillators, RTD-slot antenna oscillators, the triple-push oscillators, the two RTDs power combining oscillators, and the

oscillators realised in this project are compared in Figure 1.10 in terms of frequencies versus power. The red stars show the output power of the oscillators presented in this project in the J-band (220 GHz – 325 GHz) with record power above 0 dBm at ~ 312 GHz. The details of the RTD oscillators designed and realised on this project will be described in the following chapters.

1.3 Antennas for THz RTD-based Oscillators

Antennas fabricated on large dielectric constant (ε_r) substrates tend to radiate most of their energy into and through the substrate [73]. For example, an infinitesimal planar dipole radiates approximately $\varepsilon_r^{3/2}$ more power into the substrate than into free space. For InP (ε_r = 12.56) this ratio is around 45. In addition, any radiation into the substrate at angles greater than the critical angle ($\theta_c = \sin^{-1}(\varepsilon r^{-1/2})$) is totally internally reflected at the top and bottom surfaces and leading to confinement of the energy inside the substrate. For InP the critical angle is around 16.4º. This confined radiation propagates inside the substrate without getting radiated unless a discontinuity appears at the edges leading to degradation in the radiation pattern and in antenna performance in general.

RTD oscillators employing integrated (narrow band) slot antennas have been commonly used where the antenna performs as radiator and resonator element at the same time [27], [28], [52]–[57], [74]. Because the majority of the output power generated from this RTD-slot antenna oscillators radiate towards the substrate (InP) direction, a number of proposed solutions have been reported to overcome the substrate effects and extract the radiation from the RTD-slot antenna. The common solution has been to use a hemispherical lens on the backside to collect the power from the bottom side of the substrate [64], [71], [74]. Tapered slot (Vivaldi) antenna on a dielectric membrane was also proposed to extract the radiation where the signal radiates in the plane of the membrane

[60]. Patch antenna placed on top of benzocyclobutene (BCB) layer which is stacked on an RTD-slot antenna oscillator for upward radiation was also reported [75]. Recently, an on-chip patch antenna has been reported [26]. More details and discussions on the challenges when integrating antennas on large dielectric constant substrates will be given in Chapter 6 which also reviews a number of reported antennas for RTD-based oscillators.

1.4 Project Aim and Thesis Structure

The aim of this PhD project is to realise THz RTD oscillator circuit topologies in monolithic microwave/millimetre wave integrated circuit (MMIC) form for high power and high oscillation frequencies as well as the design, realisation and characterisation of broadband antennas that can radiate upwards toward the air side direction. The oscillators will be designed to operate in the J-band (220 – 325 GHz) with expected output powers in the milli-watt range using simple and low cost fabrication processes. Output power of 1 mW is required at 300 GHz oscillation frequency to realise different applications such as short range ultra-broadband wireless communications.

This thesis is organized as follows: Chapter 1 is the introduction, and has reviewed common THz sources and the progress of RTD THz oscillator research. Chapter 2 describes the design procedure of MMIC RTD oscillator employing one RTD device, two RTD devices connected in parallel, and the coupled oscillators topology which can employ up to four RTD devices and deliver the power to a single load. Chapter 3 explains the device and oscillator MMIC fabrication techniques including photolithography, dry and wet etching, metallization, lift-off, etc. Chapter 4 describes the passive components required to complete a RTD oscillator, such as coplanar waveguide (CPW), microstrip transmission line, metal-insulator-metal (MIM) capacitor, and thin-film resistor nichrome (NiCr).

Experimental characterisation results for the various components are given in this chapter as well. In Chapter 5, on-wafer frequency and output power measurement results of the RTD oscillators realised in CPW technology are described. It also presents the on-wafer frequency and output power measurement results of the RTD oscillators that employ resonating inductances realised by shorted microstrip lines. In Chapters 6, reported antennas for RTD-based oscillators are reviewed and the common issues when designing planar antennas on large dielectric constant substrate are discussed. A new broadband bow-tie antenna realised in this project is also described in this chapter. Finally, conclusions and future work are given in Chapter 7.

Chapter 2 RTD Oscillators: Design and Circuit Topologies

2.1 Introduction

As discussed in Chapter 1, RTD devices exhibit negative differential resistance (NDR) characteristics from DC to THz, and have the potential to realise compact THz oscillators that can operate at room temperature. The main limitation of the RTD oscillators is the low output power. To address this problem, a power combining oscillator topology employing two relatively large size RTD devices fabricated in MMIC form was reported [65]–[67]. In this project, the aim was to extend the previous work to realise higher frequencies (~ 300 GHz) and higher power at the same time. In addition, a novel power combining circuit that can employ up to four large size RTD devices and oscillate with higher frequencies was proposed and realised in this project. It is based on mutual coupling between two oscillators and delivers the combined power to a single load. Detailed analysis is given in this chapter.

2.2 DC Stability and Maximum Device Size

Large micro-sized RTD devices offer a number of advantages compared to smaller sized devices. They do not suffer thermal stability issues and can provide high RF power in oscillator circuits due to the increased ΔI, and can be fabricated with low cost photolithography. In addition, they allow for employment of low J_P designs, and so employ thicker barrier layers (~1.4nm) as those used in Ref. [65]–[67]. Thus, the epitaxial growth requirements are therefore less demanding and more accurate benefiting a reproducible technology. High PVCR is also

achievable, and since for a given specific contact resistance, the larger size RTD devices exhibit low Ohmic contact resistance, these factors benefit higher output power in oscillator circuits.

Figure 2.1 shows an example of a measured I-V characteristic of a RTD device (details on the used layer structure will be given in Chapter 3). The I-V curve exhibits a plateau-like distortion in the NDR region because of the low frequency bias oscillations created by the bias cable inductance [76], [77]. The low frequency bias oscillation leads to reduction in the RF power at the designed frequency.

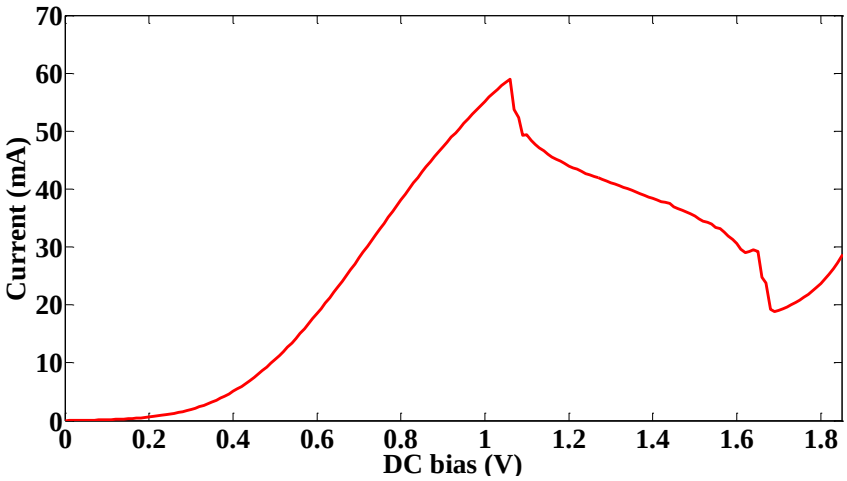


***Figure 2.1**: Measured typical I-V characteristics of a single 5 µm × 5 µm RTD device fabricated on this project.*

Figure 2.2 shows the large signal RF equivalent circuit of a RTD device where the current source of the RTD is represented by a cubic polynomial [30], [34]. By shifting the origin of the axis to the middle of the NDR region for convenience, the RTD I-V characteristics can be represented by a cubic polynomial [30], [34]:

$$I(V) = -aV + bV^3 \tag{2.1}$$

where a and b are positive constants related to the absolute value of the peak-valley voltage difference (ΔV) and the peak-valley current difference (ΔI) which represent the extent of the NDR region. By equating the slope of the I-V curve to zero at the peak and valley points, the constants a and b can be expressed as [30], [34]

$$a = \frac{3\Delta I}{2\Delta V} \tag{2.2}$$

$$b = \frac{(2\Delta I)}{(\Delta V^3)} \tag{2.3}$$

The maximum absolute value of small-signal negative conductance (G_n) is obtained at the origin of the cubic polynomial (middle of the NDR region) and it equals to the constant (a).

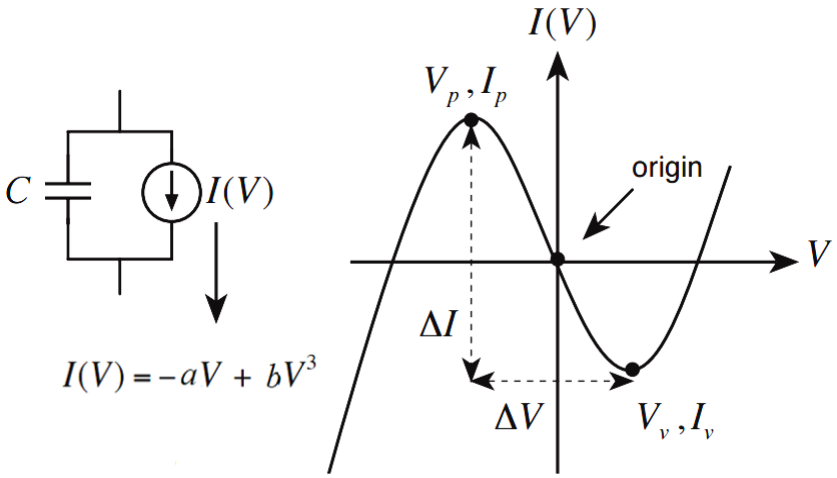


Figure 2.2: *RTD device large-signal model. The device is represented by self-capacitance C_n in parallel with voltage controlled current source I(V)* [34].

In this project, a stabilising resistor connected in parallel with the RTD device is employed in the RTD oscillator circuit to suppress the parasitic oscillation as shown in Figure 2.3. The admittance looking into the circuit is

$$Y_{in} = (Z_{in})^{-1} = \frac{1}{R_e} + [j\omega L_b + (-G_n + j\omega C_n)^{-1}]^{-1} \tag{2.4}$$

where L_b denotes the bias cable parasitic inductance, R_e is the stabilising resistor, C_n is the RTD device self-capacitance, and $-G_n$ is the RTD negative differential conductance.

The real part of $Y_{in}\ is$

$$Real(Y_{in}) = \frac{1}{R_e} + \frac{-\frac{G_n}{G_n^2 + \omega^2 C_n^2}}{\left(\frac{G_n}{G_n^2 + \omega^2 C_n^2}\right)^2 + \left(\omega L_b - \frac{\omega C_n}{G_n^2 + \omega^2 C_n^2}\right)^2} \tag{2.5}$$

$$= \frac{1}{R_e} - G_n \frac{1}{(1 - \omega^2 L_b C_n)^2 + (\omega L_b C_n)^2} \tag{2.6}$$

To suppress the low frequency oscillation, and obtain DC stability, the real part of the admittance in Equation 2.6 has to be positive [31], [77]. This means

$$Real(Y_{in}) = \frac{1}{R_e} - G_n > 0 \tag{2.7}$$

$$R_e < \frac{1}{G_n} \tag{2.8}$$

At high frequency, $Real(Y_{in})$ becomes negative and so high frequency oscillation occurs without low frequency parasitic oscillation.

For a given R_e, the maximum RTD device size with which DC stabilisation is satisfied can be estimated from the I-V characteristics as follows.

Since

$$G_n = \frac{3\Delta I}{2\Delta V} = \frac{3\Delta JA}{2\Delta V} \tag{2.9}$$

where A is the RTD device size and $\Delta J = J_p - J_v$ is the peak-valley current densities difference. Thus, Equation 2.8 becomes

$$R_e < \frac{2\Delta V}{3\Delta JA} \tag{2.10}$$

Therefore, for a given stabilising resistor R_e (usually in the 10 – 20 Ω range), the maximum device size that can be employed to obtain higher power but with DC stabilisation is

$$A_{max} = \frac{2\Delta V}{3\Delta JR_e} \tag{2.11}$$

A new approach/arrangement for using Equation 2.11 has been developed as follows. Since, for a given layer structure, ΔV and ΔJ are approximately constant, Equation 2.11 can be re-written as

$$A_{max}R_e = \frac{2\Delta V}{3\Delta J} = k \tag{2.12}$$

where k is a constant. For example, for a layer structure with ΔV = 0.75 V, and $\Delta J = 0.35\ \text{mA}/\mu\text{m}^2$ [32], the constant $k = 1.43 \times 10^3\ \Omega.\mu\text{m}^2$. Therefore, by using this unique constant value k, the value A_{max} can be calculated for any given stabilising resistor R_e. In the example given here, the maximum device size A_{max} using stabilising resistor $R_e = 20\ \Omega$ will be:

$$A_{max} = \frac{k}{R_e} = 71.4\ \mu\text{m}^2 \tag{2.13}$$

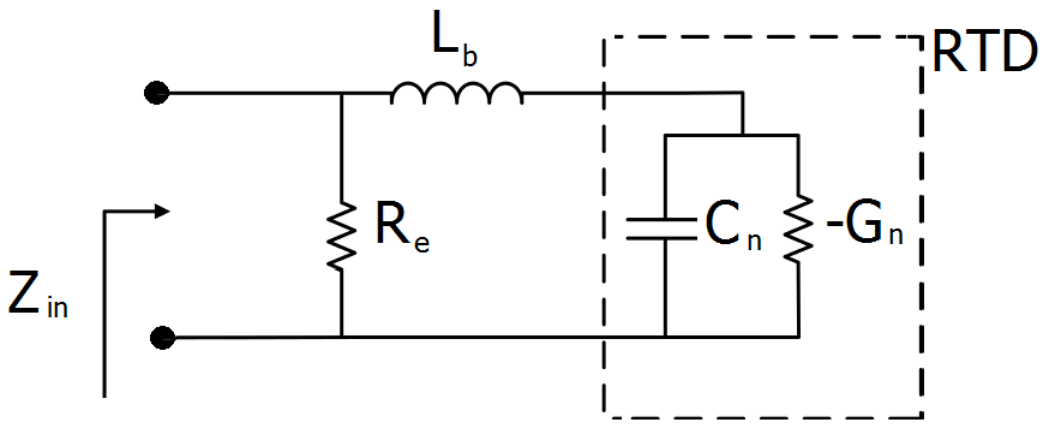


Figure 2.3: *DC stabilisation circuit with stabilising resistor (R_e) to suppress the bias oscillation. L_b is the bias cable parasitic inductance. C_n is the self-capacitance and -G_n is the negative differential conductance.*

From the discussion above, there is a limitation on the maximum RTD device size that can be employed in an oscillator circuit with DC stabilisation, where very large device size requires very small stabilising resistance R_e which is not preferable. Thus, the oscillator output power would be limited. Double RTD oscillator topology was proposed to increase the power by connecting two RTD devices in parallel and delivering their power to a single load where each device is

biased individually and connected to its own stabilising resistance R_e. More details are given next.

2.3 Single RTD Oscillator

The RTD oscillator circuit that employs one RTD device is shown in Figure 2.4 (a). The RTD device is connected to a stabilising resistor R_e to suppress the low frequency bias oscillations and a bypass capacitor C_e which is placed to short-circuit the RF signal to ground and avoid dissipating the RF power over R_e [65]. L_b denotes the bias cable inductance. Inductor L is designed to resonate with the RTD self-capacitance C_n to obtain the desired oscillation frequency. R_L is the load resistance. The capacitor (DC-Block) is introduced in the circuit to prevent any DC from reaching the spectrum analyser during on-wafer measurement. The capacitor C_e is designed to behave as a short circuit (i.e. very small impedance) at the designed frequency (f_o) which can be designed as:

$$\frac{1}{2\pi f_o C_e} < 0.1 \tag{2.14}$$

The RF equivalent circuit of the single RTD oscillator is shown in Figure 2.4 (b). The RTD is represented by its large signal model which are the device self-capacitance C_n and the voltage controlled current source $i = f(v) = -av + bv^3$. The total current in the circuit loop in Figure 2.4 (b), according to Kirchhoff's current law, is zero. Thus

$$i_1 + i_2 + i_3 - i = 0 \tag{2.15}$$

That is

$$\frac{1}{L}\int v dt + C_n \frac{dv}{dt} + vG_L - (-ab + bv^3) = 0 \tag{2.16}$$

where G_L is the load conductance ($G_L = 1/R_L$).

Equation 2.16 can be differentiated with respect to time and re-arranged to give

$$LC_n \frac{d^2v}{dt} + L(G_L - a + 3bv^2)\frac{dv}{dt} + v = 0 \tag{2.17}$$

Assuming v is sinusoidal $v = Vcos(\omega t)$, where V is the signal amplitude and ω is the angular frequency $\omega = \frac{1}{\sqrt{LC_n}}$. The instantaneous power dissipated by the load is given by

$$P_L = v^2 G_L = (Vcos(\omega t))^2 G_L \tag{2.18}$$

Thus, the average power dissipated by the load is

$$P_{Lavg} = G_L \frac{V^2}{2} \tag{2.19}$$

The instantaneous power over the RTD device is

$$P_{RTD} = -i \times v = av^2 - bv^4 \tag{2.20}$$

The average power which can be given by integrating Equation 2.20 over one period is

$$P_{RTDavg} = \frac{aV^2}{2} - \frac{3bV^4}{8} \tag{2.21}$$

The generated power by the RTD device is the power over the load which is given by

$$\frac{aV^2}{2} - \frac{3bV^4}{8} = G_L \frac{V^2}{2} \tag{2.22}$$

And *V* equals to

$$V = 2\sqrt{\frac{G_n - G_L}{3b}} \tag{2.23}$$

Then, the average power dissipated by the load is given by substituting Equation 2.23 into Equation 2.19

$$P_L = 2(G_n - G_L)\frac{G_L}{3b} \tag{2.24}$$

The maximum power delivered to the load is when $G_L = \frac{G_n}{2}$ and expressed as [49], [76]

$$P_{max} = \frac{G_n^2}{6b} = \frac{3}{16}\Delta I \Delta V \tag{2.25}$$

Figure 2.4 (c) shows the small signal RF equivalent circuit of the single RTD device oscillator where the RTD is represented by its self-capacitance C_n, and negative differential conductance $-G_n$. The frequency of oscillation f_o can be derived when the susceptance of the circuit is set to zero

$$2\pi f_o C_n - \frac{1}{2\pi f_o L} = 0 \tag{2.26}$$

or

$$f_o = \frac{1}{2\pi\sqrt{LC_n}} \tag{2.27}$$

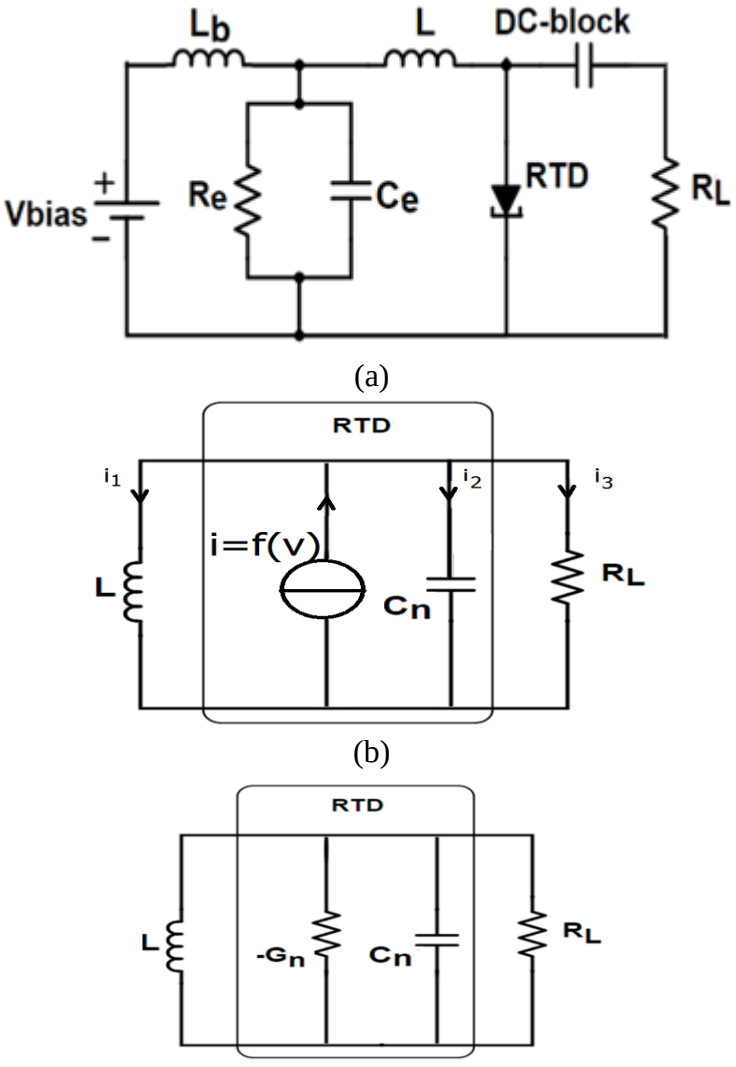


Figure 2.4: *Single RTD oscillator. (a) Oscillator circuit topology where R_e is the stabilising resistor and C_e is the decoupling capacitor. L_b is the bias cable inductance. R_L is the load resistance and L is the resonator inductance. (b) Large signal model where the RTD is represented by the self-capacitance C_n in parallel with voltage controlled current source I(V). (c) Small signal equivalent circuit. The RTD is represented by the self-capacitance C_n in parallel with the negative conductance $-G_n$.*

The RTD device self-capacitance is in general in the 2–4 $fF/\mu m^2$ range for the typical InP-based epitaxial structure (e.g. in Ref. [57], [59], [65]–[67]). Therefore, the required resonating inductance for 300 GHz would be in the 140–70 $pH.\mu m^2$

range. For an RTD device with A = 16 μm^2 and G_n = 62 *mS,* and assuming the self-capacitance of 3.56 $fF/\mu m^2$ and ρ_C = 6.3 $\Omega.\mu m^2$ [78], the calculated maximum frequency using Equation 1.2 is f_{max} = 1.1 THz.

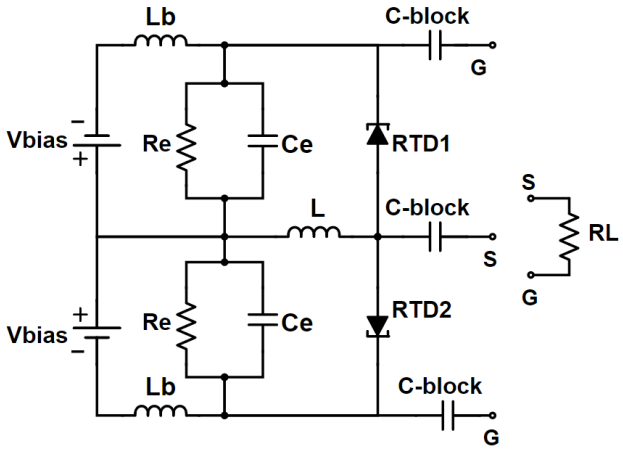
2.4 Double RTD Oscillator

Since the power of the single RTD oscillator is limited because the difficulty of employment of large RTD device without parasitic bias oscillation and the requirement of very small R_e, the double RTD oscillator topology was proposed to increase the power by connecting two RTD devices in parallel and delivering their power to a single load [79] as shown in Figure 2.5 (a). The stabilising resistors and the decoupling capacitors are calculated in similar way for the single RTD oscillator design described above. The two RTD devices are biased individually but share a single resonating inductance *L*. Thus, since the two RTDs are connected in parallel, the resultant self-capacitance will be doubled as shown in the RF equivalent circuit in Figure 2.5 (b) where each RTD is modelled by its lumped equivalent circuit model which comprises the negative differential conductance ($-G_{n1}$ and $-G_{n2}$) in parallel with the self-capacitance (C_{n1} and C_{n2}) of each device. The device contact resistance is neglected in this description for simplicity. The oscillation frequency for this parallel resonant circuit is

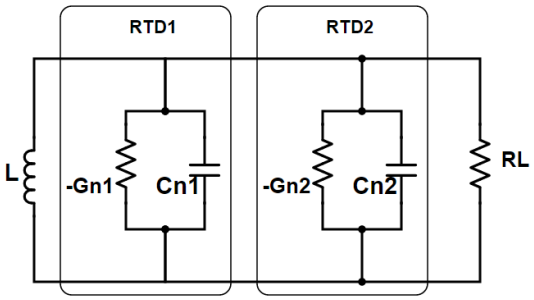
$$f_{osc} = \frac{1}{2\pi\sqrt{(C_{n1} + C_{n2})L}} \tag{2.28}$$

For C_{n1}=C_{n2}=C_n, Equation 2.28 reduces to:

$$f_{osc} = \frac{1}{2\pi\sqrt{2C_nL}} \tag{2.29}$$



(a)



(b)

Figure 2.5: *Double RTD oscillator. (a) Oscillator circuit topology where R_e is the stabilising resistor and C_e is the decoupling capacitor. L_b is the bias cable inductance. R_L is the load resistance and L is the resonator inductance. (b) Small signal equivalent circuit. Each RTD is represented by the self-capacitance (C_{n1} and C_{n2}) in parallel with the negative conductance ($-G_{n1}$ and $-G_{n2}$).*

2.5 Coupled RTD Oscillators

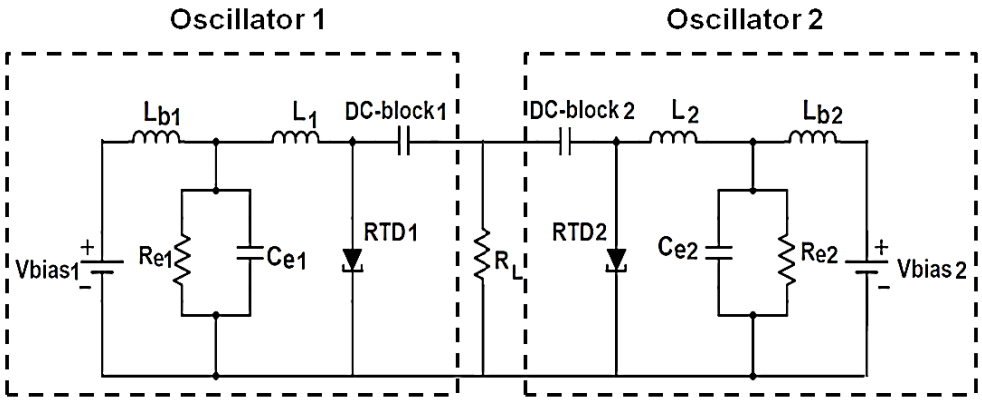
The power combining circuit described in section 2.4 uses two RTD devices in parallel. Since the equivalent device self-capacitance is twice of that of a single RTD device, smaller value for resonating inductance *L* need to be used to maintain the same oscillation frequency obtained from the single RTD oscillator. To increase the power by using two RTD devices in the circuit but without the need to reduce the inductance value *L*, a new power combining circuit topology

for MMIC RTD oscillators was realised in this project. It is based on the mutual coupling of two RTD oscillators (each oscillator can employ one or two RTD devices connected in parallel) and the output power from the two individual oscillators is combined in a single load to achieve higher power. Figure 2.6 shows the schematic circuit diagram of the power combining coupled oscillator. Two individual RTD oscillators are arranged in such a way that they share a single load. This concept was first realised for tunnelling diodes (TDs) oscillators where two individual TD oscillators are coupled and the output power is combined through synchronisation (or injection locking) [80]. Injection locking is the synchronisation in frequency and phase of a free running oscillator with another oscillator that operate at a similar frequency. The two synchronised TD oscillators were realised in microstrip hybrid technology with measured power of -6.72 dBm at 716.2 MHz, while that of the single tunnel diode oscillator was -9.09 dBm. Figure 2.6 (a) shows the proposed coupled RTD oscillator circuit topology. Each individual oscillator has one RTD device and designed as described in Section 2.3.

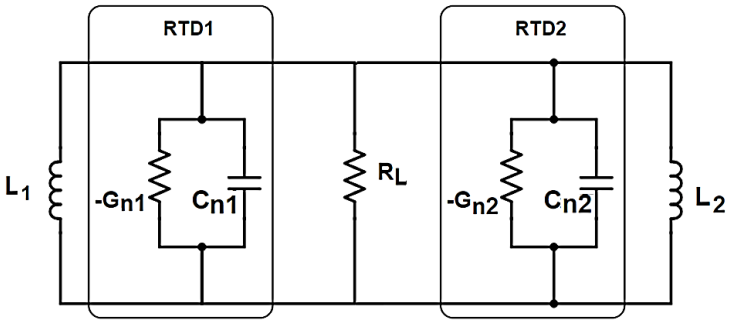
For each individual oscillator in the coupled/synchronised oscillator circuit in Figure 2.6 (a), the oscillation frequency is given by Equation 2.27. Alternatively, the synchronised oscillators could be considered as a single oscillator with the equivalent RF circuit shown in Figure 2.6 (b). The oscillation frequency can be expressed as

$$f_{osc} = \frac{1}{2\pi\sqrt{(C_{n1} + C_{n2})\left(\frac{1}{\frac{1}{L_1} + \frac{1}{L_2}}\right)}} \tag{2.30}$$

which could be reduced to Equation 2.27 for $C_{n1} = C_{n2} = C_n$ and L_1=L_2=L.



(a)



(b)

Figure 2.6: *Power combining of RTD oscillators based on mutual coupling with two RTD devices employed in the circuit. (a) Oscillator circuit topology where R_e is the stabilising resistor and C_e is the decoupling capacitor. L_b is the bias cable inductance. R_L is the load resistance and L is the resonator inductance. (b) Small signal equivalent circuit. Each RTD is represented by the self-capacitance (C_{n1} and C_{n2}) in parallel with the negative conductance ($-G_{n1}$ and $-G_{n2}$).*

To further increase the output power, each individual oscillator can use two RTD devices. Therefore, the total number of the RTD devices in the oscillator is four. This power combining oscillator was realised in this project. Figure 2.7 (a) shows the proposed coupled RTD oscillator circuit topology in which the total number of RTD devices is four. Each individual oscillator employs two RTD devices and designed as described in Section 2.4.

For each individual oscillator in the synchronised oscillator circuit in Figure 2.7 (a), the oscillation frequency is given by Equation 2.29. Alternatively, the synchronised oscillators could be considered as a single oscillator with the equivalent RF circuit shown in Figure 2.7 (b). The oscillation frequency can be expressed as

$$f_{osc} = \frac{1}{2\pi\sqrt{(C_{n1} + C_{n2} + C_{n3} + C_{n4})\left(\frac{1}{\frac{1}{L_1} + \frac{1}{L_2}}\right)}} \tag{2.31}$$

which could be reduced to Equation 2.29 for $C_{n1} = C_{n2} = C_{n3} = C_{n4} = C_n$ and L_1=L_2=L.

The new proposed power combining circuit topology which is based on mutual coupling can offer the following advantages:

- Up to four RTD devices can be employed and, therefore, 4 times the power obtained from a single RTD device oscillator can be generated.
- In this proposed circuit, there are four largest possible RTD devices (A_{max}) and each device is biased individually and connected to its own stabilising resistance, R_e. Therefore, limitations to the output power due to the bias oscillations are overcome. Alternatively, a single RTD device (with equivalent size to the four devices, 4×A_{max}) would require a very small stabilising resistance (R_e/4) which would essentially short circuit the DC supply/bias.
- Single load. Other power combining techniques [9], [10], where an array of multiple oscillators placed close to each other and each individual oscillator consists of a single RTD integrated with slot antenna (load). Therefore, power combining could occur in some regions of space and

there are regions at which the signals cancel each other out. In contrast, the proposed circuit in this project delivers the combined power to a single load which could be an antenna, and as such, it allows for a predictable radiation pattern.

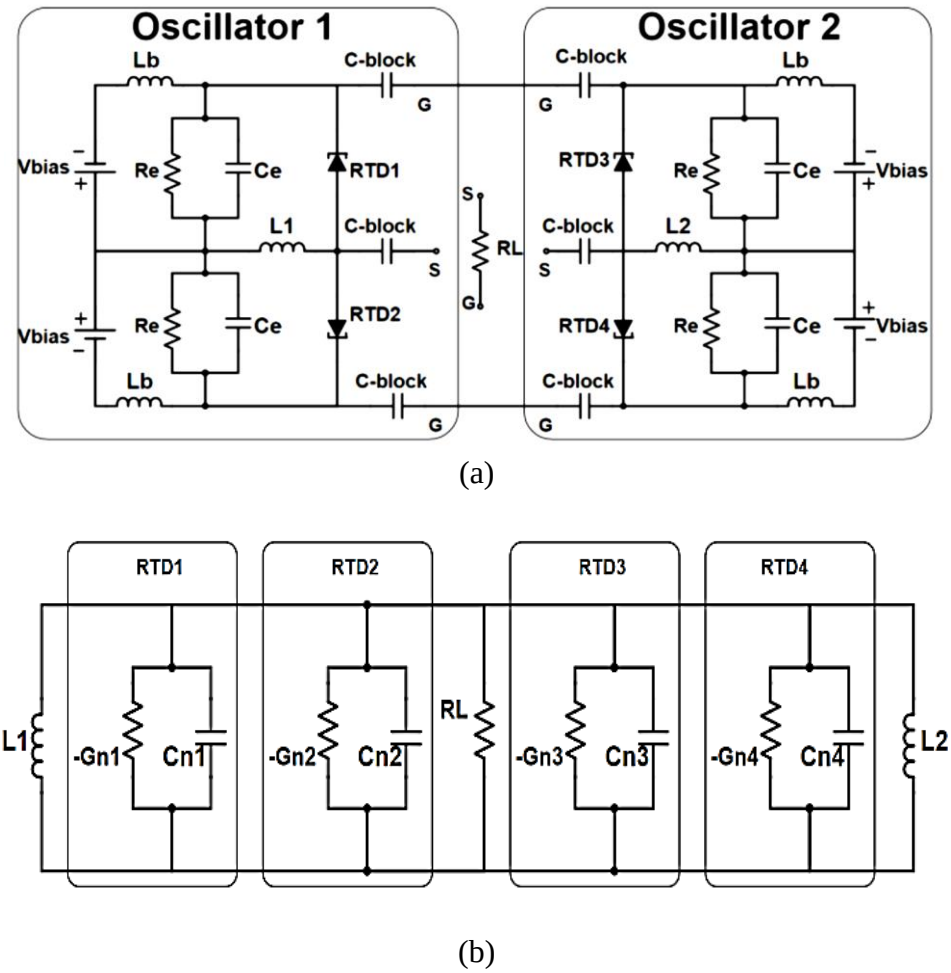


Figure 2.7: *Power combining of RTD oscillators based on mutual coupling with four RTD devices employed in the circuit. (a) Oscillator circuit topology where R_e is the stabilising resistor and C_e is the decoupling capacitor. L_b is the bias cable inductance. R_L is the load resistance and L is the resonator inductance. (b) Small signal equivalent circuit. Each RTD is represented by the self-capacitance (C_{n1}, C_{n2}, C_{n3}, and C_{n4}) in parallel with the negative conductance ($-G_{n1}$, $-G_{n2}$, $-G_{n3}$, and $-G_{n4}$).*

2.6 Resonating Inductors

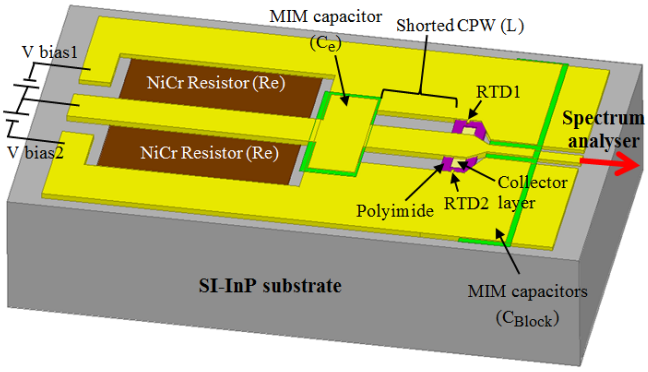


Figure 2.8: *Schematic structure for the RTD oscillator that employs two RTD devices with single inductance L realised by CPW shorted by the MIM capacitor* C_e.

As described in section 2.4, the power combing oscillator circuit with two RTD has a single resonating inductor L in the circuit. The resonating inductors L in previous work [65]–[67] were realised by using a shorted coplanar waveguide (CPW) lines of characteristic impedance (Z_o) of 50 Ω. Figure 2.8 shows an illustration of a schematic structure (of Figure 2.5 (a)) for the two RTDs oscillator with single inductor realised by CPW shorted by the capacitor C_e. In this structure, a single C_e is used unlike the structure in Figure 1.9 (a) which has two C_e capacitors connected in parallel. The single C_e is used to provide better estimation to the length of the shorted CPW line.

At very high frequencies the required length of the shorted 50 Ω CPW line becomes extremely short and so limits that maximum oscillation frequency [32]. To realise higher oscillation frequencies smaller RTD devices can be employed in the circuit in order to reduce the device self-capacitance. However, this will lead to reduction in the generated output power in addition to the requirement of electron-beam lithography which is expensive compared to photolithography. To

realise higher oscillation frequencies and achieve higher power (by employing relatively large RTD devices) at the same time with simple and low cost photolithography fabrication techniques, small resonating inductance values are required to compensate for the self-capacitance of the large device.

In this project small resonating inductance values were also realised by two large geometrical structures: shorted CPW lines with lower Z_o (32 Ω and 25 Ω) and shorted microstrip lines with Z_o 10.4 Ω. Shorted CPW/microstrip lines of lower Z_o have lower inductance values per unit length. Thus, for a given target inductance value, longer shorted CPW/microstrip line can be used when lower Z_o is used and, therefore, simple photolithography process can be utilised because the dimension limitation is largely eliminated. Results and more details will be given in the next chapters.

2.7 Summary

In this chapter, a criteria for stabilising the RTD device and suppress the low parasitic oscillations using stabilising resistor was described. Estimation of the maximum RTD device size that oscillator circuits can employ under stabilising condition was described as well. The design of different RTD oscillators that can employ single or double RTD device was described in this chapter, in addition to description of the power combining circuit which combines the powers from two oscillators over a single load based on mutual coupling and synchronisation of two individual oscillators.

Chapter 3 MMIC Technology and RTD Oscillators Fabrication

3.1 Introduction

In this chapter, the main fabrication processes required to realise RTD oscillators in monolithic microwave/millimetrewave integrated (MMIC) form will be described. The main fabrication processes include lithography, metal and dielectric deposition, and wet/dry etching. All the work in this project was undertaken in the James Watt Nanofabrication Centre (JWNC) at the University of Glasgow. The layer structure specification of the RTD device used in this project and the fabrication steps to fabricate a RTD device will be described first followed by explanation the different MMIC fabrication processes used in this project. These processes are detailed in Appendix A

3.2 RTD device

As discussed in Chapter 1, the material system for the RTD device utilised in this project was InGaAs/AlAs. This material system has been broadly used due to the capability of obtaining high peak-to-valley current ratio (PVCR) and high peak to valley current density ($\Delta J = J_P - J_V$) [35], [78]. The performance of a RTD device using this material system can be optimised through adjusting different structural design parameters. The main design parameters include: the quantum well thickness, the barrier thickness, and the spacer thickness (see Figure 1.3). A brief discussion is given here.

Reducing the thickness of the quantum well will shift the peak voltage (V_P) to a higher value. However, higher PVCR can be achieved. Reducing the barrier thickness results in increased peak current density (J_P) but the PVCR will reduce.

Spacer layers are introduced to prevent the diffusion of dopant impurities into the un-doped barrier region. They also reduce the RTD device self-capacitance to enable high frequency operation. Increasing the spacer thickness will also lead to higher PVCR but at the expense of lower current density [35].

3.2.1 Layer Structure

The layer structure specification for the RTD wafer used in this project is shown in Table 3.1. The wafer was grown by molecular beam epitaxy (MBE) by IQE Ltd on a semi-insulating InP substrate. The RTD device consists of (from the top layer to the bottom layer): highly n-type doped contact layer ($In_{0.53}Ga_{0.47}As$), collector/emitter layer ($In_{0.53}Ga_{0.47}As$) depending on the bias polarity, 25 nm lightly doped spacer layer ($In_{0.53}Ga_{0.47}As$), 1.4 nm un-doped wide band gap materials barrier layer (AlAs), 4.5 nm un-doped narrow band gap material quantum well layer ($In_{0.53}Ga_{0.47}As$), 1.4 nm un-doped barrier layer (AlAs), 25 nm spacer layer ($In_{0.53}Ga_{0.47}As$), emitter/collector layer ($In_{0.53}Ga_{0.47}As$), an etching stop layer ($In_{0.52}Al_{0.48}As$), highly n-doped contact layer, and buffer layer ($In_{0.53}Ga_{0.47}As$) which is lattice matched and grown on the InP substrate. The undoped spacer layers are used to reduce the diffusion of dopant impurities to the DBQW while the lightly doped spacer layers reduce the device capacitance and enhance the high frequency performance. The etching stop layer is included for controlling the etching depth when a dry etch recipe is used to form the device mesa. That is, a recipe that does not etch aluminium-contained materials should be used to etch down to the etching stop layer. After that the etching stop layer can be etched (e.g. wet etching) to expose the bottom contact layer. The 1.4 nm AlAs barrier, used in the RTD design for this project, has more advantages over thinner barriers (~ 1 nm) which have conventionally been used to realise THz RTD oscillators (e.g. in [57], [59]). The advantages of thicker barriers include: less

demanding and more accurate epitaxial growth requirements which therefore benefiting a reproducible technology [62], [63], higher peak-to-valley current ratio (PVCR) which has the potential for higher power performance, and expected lower J_P which could enhance the thermal stability [59]. In addition, Thinner barrier (~ 1 nm) results in high peak current density (J_P) devices and so sub-micron devices have to be realised. More details and analytical discussion will be given in Chapter 5.

Table 3.1: *The layer structure specification of the RTD device used in this project.*

Semiconductor Composition	**Mole Fraction (x)**	**Thickness (Å)**	**Doping (cm^{-3})**	**Description**
In(x)GaAs	53.2	400	3×10^{19} :Si	Contact layer
In(x)GaAs	53.2	1600	2×10^{18} :Si	Emitter/ Collector
In(x)GaAs	53.2	250	2×10^{16} :Si	Spacer
In(x)GaAs	53.2	15		Spacer
AlAs		14		Barrier
In(x)GaAs	53.2	45		Well
AlAs		14		Barrier
In(x)GaAs	53.2	15		Spacer
In(x)GaAs	53.2	250	2×10^{16} :Si	Spacer
In(x)GaAs	53.2	250	2×10^{18} :Si	Collector/ Emitter
In(x)AlAs	52.1	100	1×10^{19} :Si	Etch stop
In(x)GaAs	53.2	2000	3×10^{19} :Si	Contact layer
In(x)GaAs	53.2	2000	2×10^{19} :Si	Buffer
SI : InP				Substrate

3.2.2 RTD Device Fabrication Flow

The main fabrication steps required to fabricate a single RTD device are summarized in Figure 3.1. The first step in fabrication is to deposit a contact metal on the top of the emitter/collector layer as shown in Figure 3.1 (a). The contact

metal scheme used is in this project is Ti/Pd/Au (20/30/150 nm) which can provide very low specific contact resistance ($0.73 \pm 0.44\ \Omega.\mu m^2$) [81]. The next step, as illustrated in Figure 3.1 (b), is to etch the epitaxial layers down to the bottom collector/emitter layer. After etching, another contact metal is deposited as can be seen in Figure 3.1 (c). The next step is then to etch to the semi-insulating InP substrate and form the emitter mesa as shown in Figure 3.1 (d). Acid solvent (H_3PO_4:H_2O_2:H_2O=1:1:38) which has etching rate of ~ 100 nm / min was used to complete these two etching steps in this project. Thereafter, the next step is to deposit/spin the passivation layer (polyimide PI-2545), which is indicated by the green area in Figure 3.1 (e), and open a via in the polyimide using a dry etch recipe and a suitable resist mask. The via opening process was optimised and described in [32]. Accurate mask alignment, for small device sizes in particular, is crucial. Misalignment will lead to device failure. For 3 μm × 3 μm RTD device, the via size is 1.5 μm × 1.5 μm which means the alignment tolerance is only 0.75 μm. After the via opening, a metal pad (Ti/Au (20/400 nm)) is deposited as shown in Figure 3.1 (f). The RTD device fabrication is now completed. DC characterisation results will be given in Chapter 5. To complete a RTD oscillator circuit, additional passive components such as a thin-film resistor and Metal-Insulator-Metal (MIM) capacitor are also required and will be described the next chapter. The specific process details are provided in Appendix A.

3.3 General MMIC Fabrication Processes

3.3.1 Lithography

Lithography is the process of transferring patterns on top of a sample surface with the aid of suitable mask. The most common lithography techniques used in integrated circuits fabrications are electron beam lithography and photolithography.

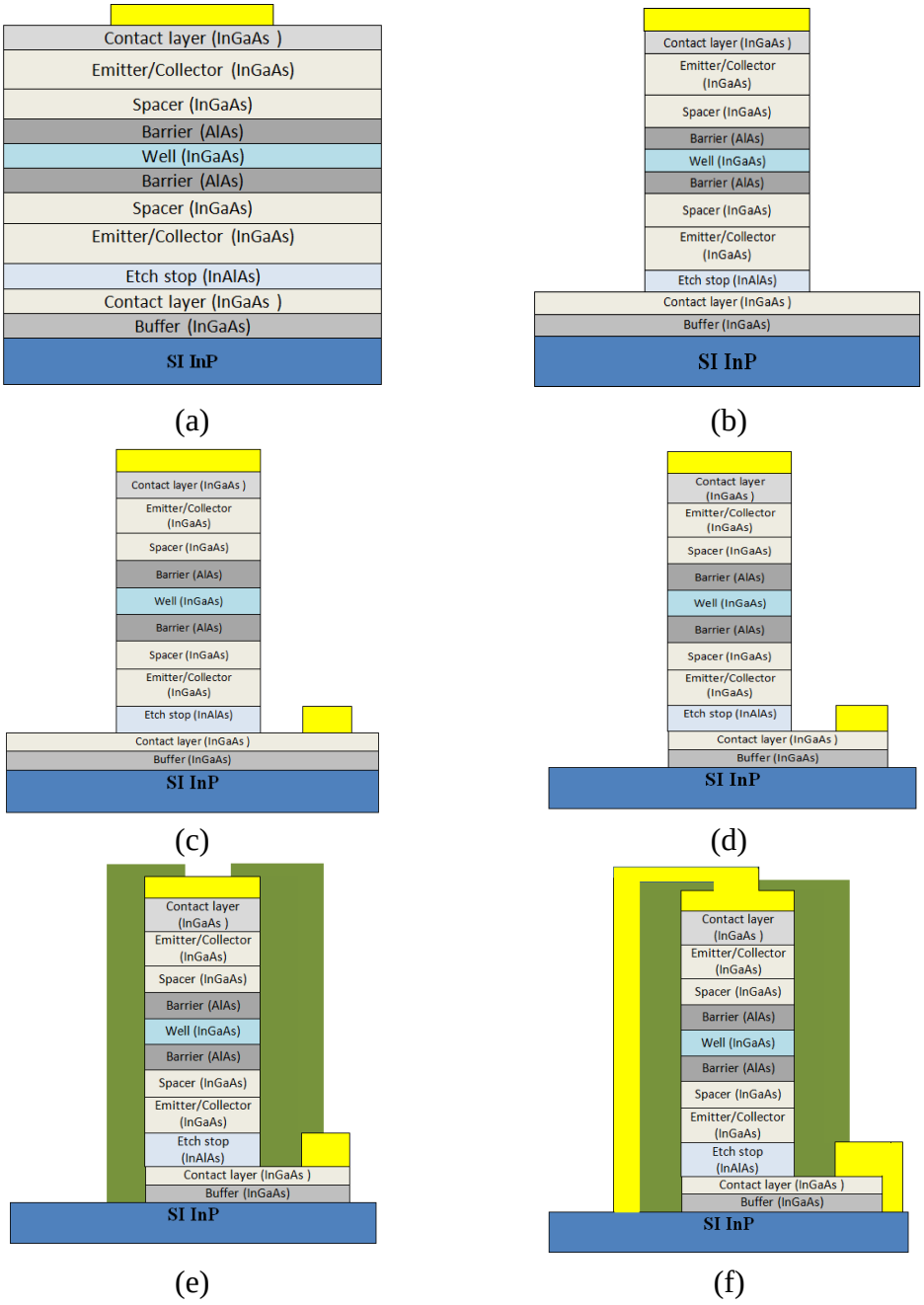


Figure 3.1: *RTD device fabrication steps: (a) Deposit contact metal. (b) Etch to the bottom emitter/collector layer. (c) Deposit contact metal. (d) Etch to the substrate. (e) Passivation and via opening. (f) Deposit bond metal pads.*

3.3.1.1 Electron-beam

Electron-beam (e-beam) lithography is a technique of defining patterns on a sample where a beam of electrons is scanned through a sample surface covered with suitable resist that is sensitive to the electron beam. It offers high resolution and less alignment errors compared to photolithography. It has the capability of defining small features of less than 100 nm. The e-beam lithography tool available at the JWNC is the Vistec VB6-UHR-EWF which has a minimum resolution of 0.5 nm and a minimum spot size of 4 nm. Compared to photolithography which requires a hard mask, e-beam requires a software mask which can be modified easily. However, e-beam lithography takes much longer time than photolithography which can be accomplished in few seconds. In this project, e-beam was used in the manufacturing of the optical masks for photolithography processes, and for single step lithography tasks such as antennas. All masks were designed by L-Edit software [82].

3.3.1.2 Photolithography

As the micron-sized RTDs are the smallest components in the oscillator circuits in this project, photolithography was used to define all features required to fabricate the RTD oscillator circuits[1]. Photolithography is low cost and provides high throughput, compared to e-beam lithography technique. However, the resolution is limited due to light wave diffraction. A Karl Suss MA6 mask aligner was used in this project for photolithography processes. It can offer resolution capability of 0.6 μm with an ultra-violet (UV) source of wavelength λ = 400 nm. The first step in photolithography process is to spin a suitable photoresist on the sample. After that, UV light is projected and the photoresist is exposed through optical windows

[1] The proposed THz oscillator circuits in this project employ large size RTD devices to generate high power and high oscillation frequencies using photolithography. Details will be given in Chapter 5.

in a hard mask. After exposure, a development step is carried out and various features defined on the mask are patterned to the photoresist on the sample surface. The transferred patterns define the required features which will be used in different fabrication steps such as metal/dielectric deposition and wet etching mask.

3.3.1.3 Photoresists

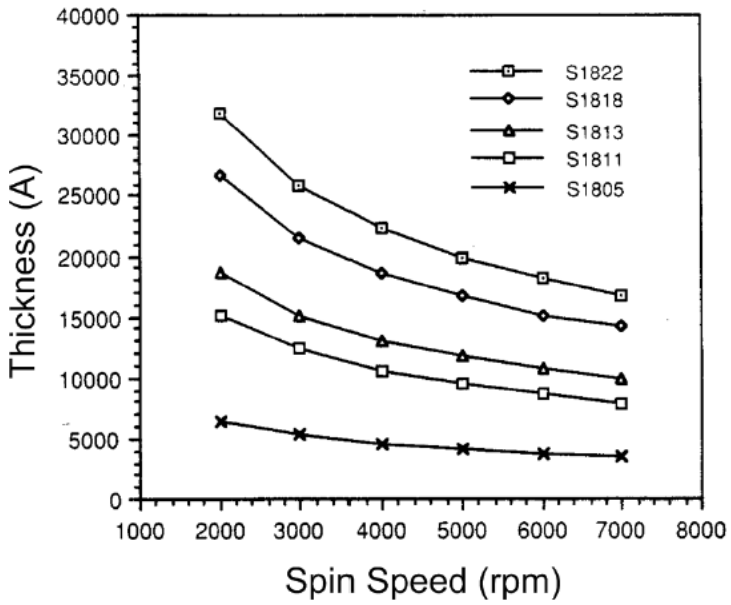


Figure 3.2: S1800 series photoresist thickness versus spin speed [84]

In photolithography processes, photoresists play an important role in successful fabrication. A photoresist is photosensitive material used to transfer a pattern from the mask to the wafer sample. There are two types of photoresists: negative and positive. With the negative photoresists, the unexposed region dissolves more quickly during the developing process while the exposed region remains unchanged on the sample. Positive photoresists react in the opposite way. Two photoresists have been used in this project: the S1805 and the S1818 from Shipley Europe Ltd. Both are positive photoresists. The difference between the two resists

is the spin-thickness as can be seen in Figure 3.2. With 4000 rpm speed, the thicknesses obtained are ~1.8 µm and ~0.5 µm for the S1818 and S1805, respectively.

Lift-off process is an important step in order to realise successful metal structures. After the required metal is deposited on exposed and developed photoresist on top of the sample, the next step is to lift-off the unwanted metal by dissolving the photoresist in an appropriate solvent (e.g. acetone). The thickness and the profile undercut of the resist have to be considered in lift-off process according to the thickness of the metal to be deposited. When thin layer of metal (~200 nm) is required, single layer of photoresist (S1805) would be sufficient. The undercut can be formed after dipping the spun S1805 in chlorobenzene (C_6H_5Cl) for ~ 5 minutes before UV exposure. Chlorobenzene penetrates and reduces the dissolving rate of the resist top surface. As a result, the profile of the soaked resist will be changed and an undercut will be formed making it suitable for successful lift-off [83]. Figure 3.3 illustrates this technique.

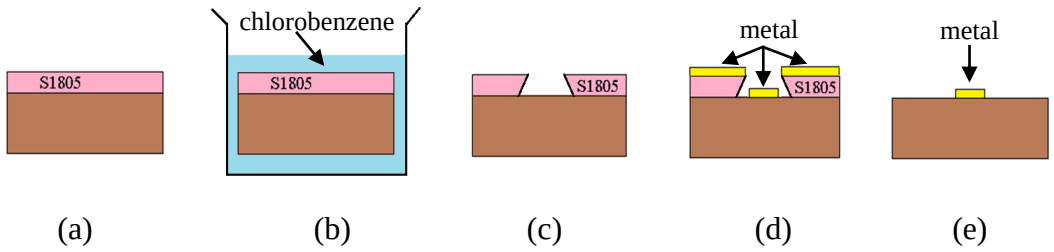


Figure 3.3: *Lift-off process using single layer of photoresist: (a) Spin and prebake photoresist on the sample, (b) Dip in chlorobenzene (C_6H_5Cl) for ~ 5 minutes, (c) UV Expose and develop the photoresist, (d) Metallisation, and (e) Lift-off.*

When thicker layers of metal are required (e.g. ~ 400 nm thick), bi-layer lift-off process is recommended. In this process the S1805 or S1818 photoresist is used with combination with another thick resist: Lift-Off Resist (LOR). Figure 3.4

illustrates this technique. The LOR resist is first spun on the sample followed by spinning S1805 photoresist. This technique provides an undercut due to the different dissolution rate in the developer, which makes it useful for the lift-off process when thick metal is deposited. The undercut formed in the bi-layer process (LOR and S1805) is larger than that formed in the single layer resist (S1805 soaked in chlorobenzene). This ensures more successful lift-off process when thin dielectric material layer is deposited as will be explained in sub-section 3.3.3.

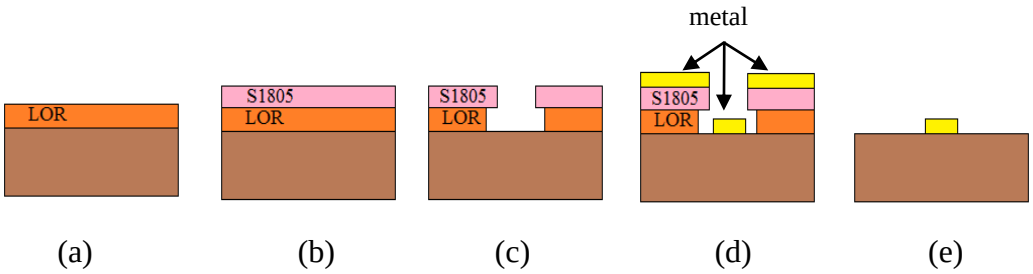


Figure 3.4: *Lift-off process using bi-layer process: (a) Spin and prebake LOR-10A, (b) Spin and prebake photoresist over LOR-10A, (c) UV Expose and develop both photoresist and LOR-10A, (d) Metallisation, and (e) Lift-off.*

3.3.2 Metallisation

The different metal scheme (e.g. contact and metal pads) were patterned by metallisation and lift-off. Electron beam physical vapor deposition (EBPVD) is the technique that was used in this project for metallisation. In this technique, atoms from target metal are evaporated by focused electron beam forming thin film layer of metal on the sample. The EBPVD tool used in this project is the Plassys MEB550S (Plassys IV) system. Plassys IV is an automated metallisation system that can deposit multi-layer of up to eight different materials. The available metals are Titanium (Ti), Nickel (Ni), Nickel-Chromium (NiCr), Germanium (Ge), Gold (Au), Molybdenum (Mo), Palladium (Pd), and Aluminium

(Al). At the start of the run, the sample is mounted on a suitable sample holder in the load lock. The load lock is then pumped into vacuum. After selecting the required metal scheme the process can be executed and the machine will commence automatic deposition. This involves checking the vacuum levels before opening the valve between the load lock and the chamber and rotating the sample assembly to face the electron gun. When the deposition run is complete the load lock automatically vents and the sample can be retrieved. The Plassys IV also provides another argon Gun treatment option before metal deposition. In this project, argon gun treatment for 20 seconds was used to clean the surface of the sample (de-oxidation step) prior to the contact metal deposition. This de-oxidation technique was found to be quick and can provide good Ohmic contact resistance. The specific contact resistance was measured by transmission line model (TLM) technique and the details will be given in Chapter 4.

3.3.3 Dielectric Layer Deposition

Chemical Vapor Deposition (CVD) is a chemical process that is used to deposit different dielectric materials (e.g. silicon dioxide (SiO_2) and silicon nitride (Si_3N_4)). Dielectric material (silicon nitride Si_3N_4) was used in this project as insulator layer to construct the required metal-insulator-metal (MIM) capacitors used in the RTD oscillator circuits (more details will be given in Chapter 4). Inductively Coupled plasma (ICP) chemical vapor deposition (CVD) is the process that was used to deposit 75 nm layer of Si_3N_4 in this project. The process is performed at room temperature which makes it suitable for deposition on samples with previously spun photoresist and, as so, no damage to the photoresist occurs. This also means that it can be patterned by using lift-off technique.

Although the thickness of the deposited Si_3N_4 is only 75 nm, bi-layer lift-off process provides better lift-off compared to single layer lift-off process. This

might be because the 75 nm Si_3N_4 is deposited on the side wall of the single layer photoresist (S1805) which makes the lift-off process difficult where the stripper solvent cannot access the photoresist. On the other hand, the undercut formed in the bi-layer photoresist process (LOR-10A and S1805) is larger compared to that obtained from the single layer photoresist.

3.3.4 Etching

Dry or wet etching can be used to define the RTD mesa. In this project, chemical wet etching (H_3PO_4:H_2O_2:H_2O = 1:1:38) was used. This recipe can etch InGaAs and InAlAs materials at a rate of around 100 nm/min but does not etch InP. Wet etching process is fast, low cost, and has low surface damage compared to dry etching. For wet etching process, the contact metal (Ti/Pd/Au) was also used as etching mask unlike dry etching which require the use of suitable mask to protect the contact metal. However, the main disadvantage is that wet etching creates an undercut because of the isotropic nature of the process. During the time at which the semiconductor is etched down, the chemical solvent will also etch part of the semiconductor material underneath the mask creating an undercut. The undercut becomes severe when the aspect ratio of the feature is high. The undercut will cause reduction in the designed device size and alter the expected performance. Dry etching, on the other hand, can provide vertical side wall depending on the used recipe. In this project, only wet etching was used in oscillators realisation since the mesa height is relatively low (~300 nm) and the device sizes ranges from 3 µm × 3 µm to 5 µm × 5 µm.

In this project, dry etching process was used to open up a via in polyimide (PI2545) and enable a connection between the top contact of the RTD device and the bond pads as shown in Figure 3.1 (e). The process was developed in previous work [32]. The dry etching recipe was CF_4:O_2 with 5:95 sccm flow rate.

Photoresist S1805 is the recommended etching mask in order to obtain a smooth slope profile of the PI-2545. The measured dry etching rate is about 240 nm/min for PI2545 and 170 nm/min for S1805 photoresist. To ensure etching down the PI2545 and opening the via successfully, “end point” detection technique using laser interferometer was used [85]. This technique is used to determine the end point and the depth that has been etched. In interferometer end point detection technique, a monochromatic light is emitted from a laser source. During the polyimide etching time, constructive and destructive interference of the radiation reflected from the vacuum-polyimide interface produces oscillation in the intensity which is displayed in the intensity curve. When the PI2545 is completely etched, the laser beam will penetrate the InP substrate leading to almost constant intensity. Figure 3.5 shows an interferogram example obtained during etching down the polyimide layer. When the polyimide is completely etched, a straight line (i.e. constant intensity) will be displayed indicating the etching endpoint.

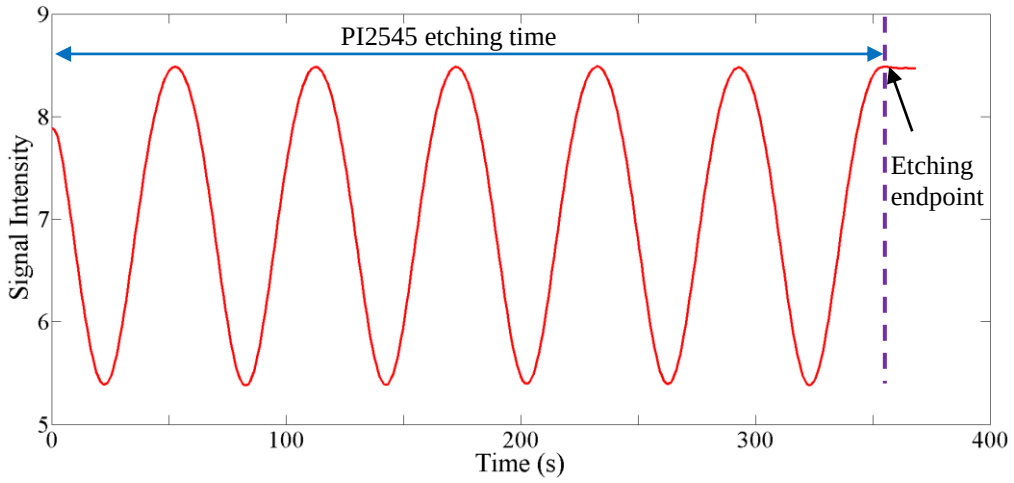


Figure 3.5: *Interferogram example obtained during etching down the polyimide layer.*

3.4 Summary

In this chapter, the main fabrication steps to fabricate RTD devices and the general fabrication processes to realise RTD oscillators were described. Photolithography was used to fabricate the RTD devices and oscillators in this project. e-beam lithography was used in the manufacture of masks and to fabricate the tested antennas which require only single lithography step. Single layer lift-off process was used when thin metal had to be deposited while the bi-layer lift-off process was used for thick metal deposition. It is also recommended when depositing 75 nm Si_3N_4 for MIM capacitor in order to get better lift-off. Wet etching was used for all required etching steps except for via opening. End point detection technique using laser interferometer proved to be an effective way to ensure successful via opening. The specific process details are provided in Appendix A. These processes were utilised to realise RTD devices and THz oscillators successfully.

Chapter 4 Passive Components

4.1 Introduction

As discussed in Chapter 2 and Chapter 3, RTD oscillators require additional passive components in the circuit according to the specific designs. They include metal-insulator-metal (MIM) capacitors, coplanar waveguide (CPW) transmission line, shorted CPW or shorted microstrip transmission line, and thin-film resistors. In MMIC technologies, metal-insulator-metal (MIM) capacitors, and thin-film resistors can be designed and realised to obtain the required values. In this chapter, the design procedures of these different passive components are described. Experimental characterisation results of these components will be given at the end of this chapter. Characterisation of Ohmic contact resistance is also included in this chapter since it plays an important role in the performance of the RTD device.

4.2 Design of Passive Components

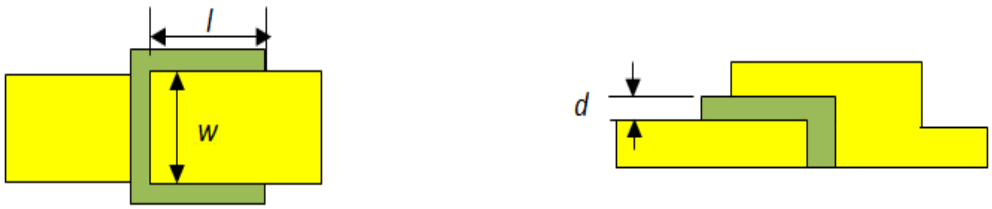
4.2.1 Metal–Insulator-Metal (MIM) Capacitor

Metal-Insulator-Metal (MIM) capacitor consists of two metal plates separated by a dielectric layer. In this project, silicon nitride (Si_3N_4) was used as the dielectric layer. The typical layout of the MIM capacitor is shown in Figure 4.1. The capacitance value can be calculated as

$$C = \varepsilon_o \varepsilon_r \frac{wl}{d} \tag{4.1}$$

where $\varepsilon_o = 8.854 \times 10^{12}\text{F/m}$ is the vacuum permittivity and $\varepsilon_r = 6.8$ is the dielectric constant of the Si_3N_4. *l*, *w*, and *d* are the dimensions of the MIM capacitor as shown in Figure 4.1. The thickness of the dielectric Si_3N_4 (*d*) used in this project is 75 nm, which corresponds to 0.8 fF/μm^2. Therefore, to design a MIM capacitor with specific value the dimensions *l* and *w* have to be calculated.

Two types of MIM capacitors (parallel and series) were designed and used in the oscillator circuit. The parallel capacitor (C_e) is used to short circuit the RF signal and prevent its power being dissipated by the stabilising resistor R_e and also used to short transmission line structures to realise the resonating inductors as will be described later. The series capacitor (DC-block) is used as a DC block to protect the spectrum analyser from DC bias voltage during on-wafer characterisation. It can be noticed from Figure 4.1 (b) that there is additional capacitance because of the Si_3N_4 is also deposited on the side wall of the bottom metal of the capacitor. This would also enhance the performance (depending on the dimensions of the extra capacitance on the sidewall of the bottom metal) of both C_e and DC-Block capacitors, because larger capacitance values will provide better short circuit for the RF signal.



(a) (b)

Figure 4.1: *MIM capacitor layout. (a) Top view. (b) Cross-section view.*

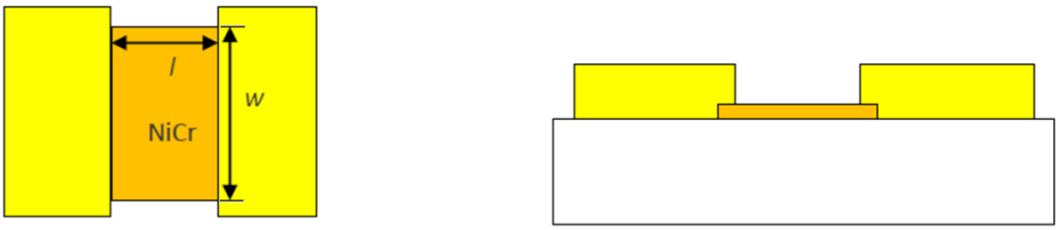
4.2.2 Thin-film Resistor

A thin-film resistor is used to realise the stabilising resistor R_e to supress the parasitic bias oscillation. In this project, 33 nm Nichrome (NiCr) was used as

resistors in the MMIC RTD oscillators. This thickness of NiCr provides sheet resistance (R_{sh}) of around 50 Ω/□ [86], [87]. The geometry of the resistor is shown in Figure 4.2. The resistance value can be calculated using the following equation

$$R = \rho \frac{l}{wd} = R_{sh} \frac{l}{w} \tag{4.2}$$

where ρ is the material bulk resistivity (1.65×10^{-6} Ω.m). The dimensions *l*, *w*, and *d* are the length, the width and the thickness of the resistor film, respectively.



(a) (b)

Figure 4.2: *Thin-film resistor. (a) Top view. (b) Cross section view.*

4.2.3 Coplanar Waveguide (CPW)

Coplanar waveguide (CPW) is used in the RTD oscillator circuits to connect different elements in the circuit and to provide a 50 Ω transmission line for RF pads on which RF probes are landed during on-wafer characterisations of the oscillators. It is also used to realise resonating inductors when it is short circuited. Figure 4.3 shows the general structure of a CPW line which consists of a thin strip conductor (signal line) and two ground planes all are deposited on the same level on the top of a substrate [88]. The different design parameters are *w*, *s*, *g*, *t*, and *h*, which are the width of the signal line, the gap distance between the signal line and

the ground plane, the width of the ground plane, the thickness of the metallic strip, and the substrate thickness, respectively.

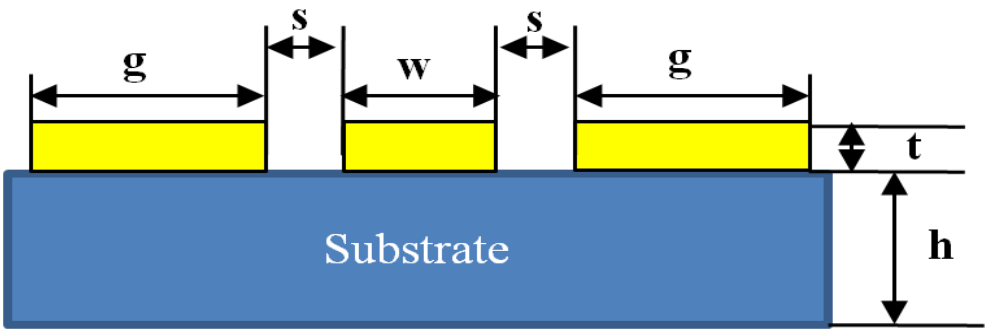


Figure 4.3: *Illustration of a CPW structure. The signal line width is w, the gap between the signal line and ground plane is s, the width of the ground planes is g, the thickness of the conductor metal is t, and the thickness of the substrate is h.*

In this project, the dimensions (*w* and *s*) of the CPW that gives a particular Z_o were calculated using the "LineCalc" tool within Agilent's Advanced Design System (ADS) software [89]. The width of the ground planes *g* should be at least two times the signal line width *w* in order to reduce the conductor loss and the attenuation introduced by a narrow ground plane [90]. Normally the thickness of the metalic conductor *t* is chosen to be three times the skin depth δ (to reduce the attenuation) which is given by $\delta = \sqrt{\frac{\rho}{\pi f \mu_o \mu_r}}$ [91], where ρ is the resistivity of the conductor in $\Omega.m$, f is the frequency, μ_o is the vacuum permeability ($\mu_o = 4\pi \times 10^{-8}\ H/m$), and μ_r is the relative permability of the conductor. For gold with resistivity ρ = 2.44 × 10^{-8} $\Omega.m$, and $\mu_r = 1$, the skin depth at 300 GHz is δ = 0.13 μm. Thus, 0.4 μm (400 nm) thick gold was used to realise the transmission lines conductors in this project.

Different CPW structures with different Z_o (50 Ω, 32 Ω, and 25 Ω) fabricated on InP substrate which has dielectric constant $\varepsilon_r = 12.56$ were also used to realise different resonating inductors in the oscillator circuits and the design methodology is described here. For a transmission line of length *l*, the input impedance Z_{in}, is expressed as [91]

$$Z_{in} = Z_o \frac{Z_L + jZ_o tan(\beta l)}{Z_o + jZ_L tan(\beta l)} \tag{4.3}$$

where Z_o is the characteristic impedance, Z_L is the load impedance, and $\beta = \frac{2\pi f_o \sqrt{\varepsilon_{eff}}}{c_o}$ is the phase constant. The effective dielectric constant of the CPW (ε_{eff}) can be approximated as $\varepsilon_{eff} = \frac{1}{2}(\varepsilon_r + 1)$ for finite-width ground CPW and relatively thick substrate [92]. c_o is the speed of light in free space. For a short circuited CPW line (i.e. $Z_L = 0$), Equation 4.3 becomes

$$Z_{in} = jZ_o tan(\beta l) \tag{4.4}$$

Therefore, the input impedance of the shorted transmission line is imaginary and acts as an inductive reactance when the electrical length of the line is less than 90º. Therefore Equation 4.4 becomes

$$j\omega L = jZ_o tan(\beta l) \tag{4.5}$$

where *L* is the line inductance and $\omega = 2\pi f_o$ is the angular frequency. For a desired inductance *L* the equivalent length of the shorted transmission line is

$$l = \frac{1}{\beta} tan^{-1}\left(\frac{2\pi f_o L}{Z_o}\right) \tag{4.6}$$

From Equation 4.6, for a given inductance value L and frequency, if the line characteristic impedance Z_o reduces, the required line length increases. A line with lower Z_o has lower inductance per unit length. At very high frequencies, for a RTD oscillator with a given device size, lower Z_o line will facilitate the fabrication process using photolithography because the dimension limitation is largely eliminated as will be discussed in Chapter 5. Table 4.1 lists the CPW dimensions with different Z_o used in this project. It can be seen these dimensions can be easily fabricated using photolithography. However, for lower Z_o values fabricating the CPW structure using photolithography will be challenging. For example, to construct a 10 Ω CPW line, the required the signal line width is w = 66.5 mm with gap dimension s = 2 μm. Therefore, an alternative transmission line structures of characteristic impedance values < 20 Ω was proposed and designed in this project. It was a microstrip line using the polyimide as a substrate. More details are in the following subsection.

Table 4.1: *CPW design dimensions for different characteristics impedances.*

Z_o (Ω)	W (μm)	S (μm)
50	*60* *20*	*40* *13.8*
32	*110*	*15*
25	*126*	*7*

4.2.4 Shorted Microstrip Transmission Line

Microstrip transmission line consists of a strip of conductor (signal line) deposited on top of a substrate with ground plane underneath [91]. Figure 4.4 shows a cross-sectional view of a general microstrip line. The design dimensions include: the

width of the signal line (*w*), the thickness of the strip (*t*), and the substrate thickness (*h*).

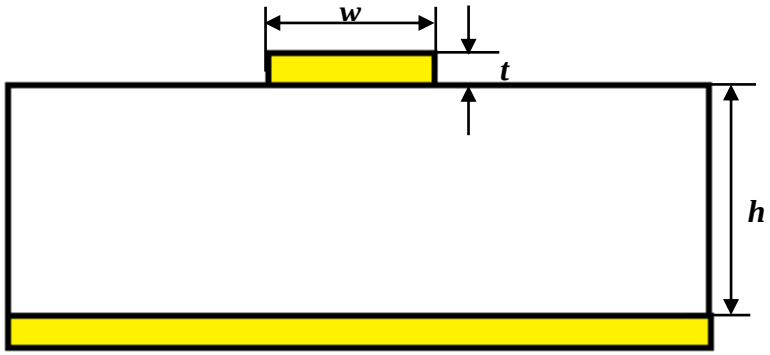


Figure 4.4: *General structure of a microstrip transmission line.*

Shorted microstrip transmission lines were used in this project to realise resonating inductors in the oscillator circuits. The polyimide PI2454 layer (ε_r = 3.5), which was mainly used for RTD device passivation, was also used as a substrate in the shorted microstrip line structure. Figure 4.5 shows cross-sectional view of the shorted microstrip line section in the RTD oscillator. The polyimide thickness is 1.2 µm and spun on top of ground plane depoistied on the InP substrate. The signal line is connected to the top electrode of the RTD device and terminated (short circuited) by the MIM capacitor (C_e) which uses Si_3N_4 as a dielectric layer. Using the "LineCalc" tool within Agilent's Advanced Design System (ADS) software, it was found that when the signal line width w = 20 µm (the same width of the signal line of the CPW RF pads used in the RTD oscillatiors for on-wafer characterisation) and the thickness t = 0.4 µm, this microstrip line has characteristic impedance Z_o = 10.4 Ω. This low Z_o will facilitate the realisation of low resonating inductance values using photolithography proccess (compaerd to the 50 Ω CPW line) because longer line can be used. To explain this, Figure 4.6 plots the required CPW/microstrip (50 Ω/10.4 Ω) line length that provides a given resonating inductance value up to 5 pH. It can be seen that, for exapmle, in order to realise 1.3 pH resonant

inductance, the 50 Ω CPW line is 3 µm long, while for the 10.4 Ω microstrip line the length is 20 µm. This microstrip design was used in this project to realise RTD oscillators using photolithography. Detalis will be given in Chapter 5.

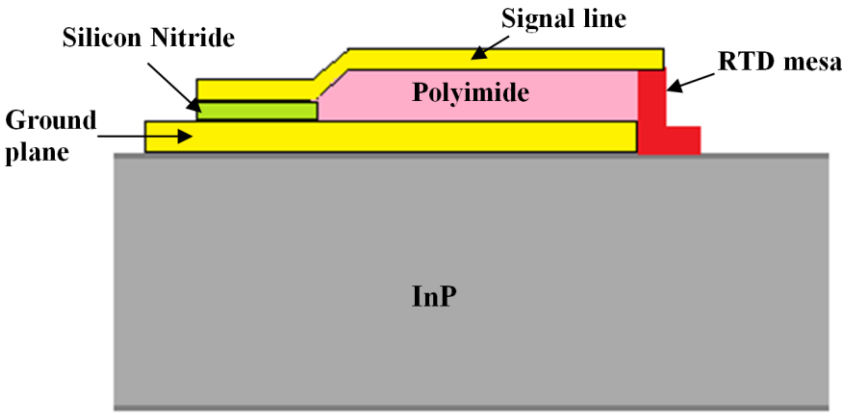


Figure 4.5: *Cross-sectional view of the shorted microstrip line structure with PI245 substrate to realise resonating inductances. The MIM capacitor with silicon nitride dielectric is used to short circuit the microstrip line.*

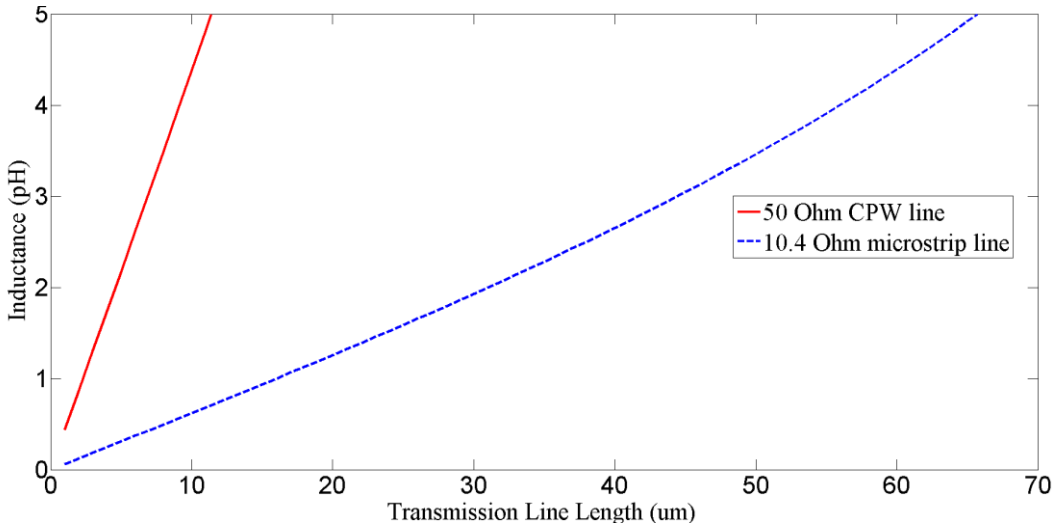


Figure 4.6: *Inductance versus transmission line (50 Ω CPW or 10.4 Ω microstrip) length.*

4.3 Characterisation of Passive Components

This section describes the characterisation results of some of the passive components which are used to realise the RTD oscillators. CPW and MIM capacitors were characterised with the scattering parameter (S-parameter) measurement using a calibrated vector network analyser (VNA) in the J-band (220 GHz – 325 GHz). A VNA characterisation is performed by measuring the reflection and transmission coefficients (S_{11}, S_{22}, S_{12}, and S_{21}) across the whole measured frequency band. Short-open-load-thru (SOLT) calibration technique using a standard calibration substrate was carried out before any measurement to correct for system errors and move the measurement reference plane to the tips of the ground-signal-ground (GSG) probes.

4.3.1 Coplanar Waveguide

To characterise the designed CPW lines, CPW test structures were fabricated and characterised by 2-port S-parameter measurements in the J-band (220 GHz to 325 GHz). The CPW structure designed for characteristic impedance Z_o = 50 Ω on a semi-insulating InP substrate of dielectric constant ε_r = 12.56. The calculated width of the signal line strip is w = 20 µm and the gap s = 13.8 µm. The ground plane width g is 80 µm and the line length is 400 µm. The return loss (S_{11} and S_{22}) are plotted in Figure 4.7 while the measured insertion loss (S_{12} and S_{21}) are plotted in Figure 4.8. The average value for S_{11} and S_{22} is about -15 dB, which means very low power of the transmitted signal has been reflected back to the same port. For S_{12} and S_{21}, the average insertion loss value is around 1.5 dB. This indicates that the CPW line perfectly transmit the signal from one port to the other, although the relatively long line of the structure (400 µm). It can be noted from Figure 4.7 and

Figure 4.8 that fluctuations are observed between 260 GHz and 270 GHz which could be due to error in the calibration, etc.

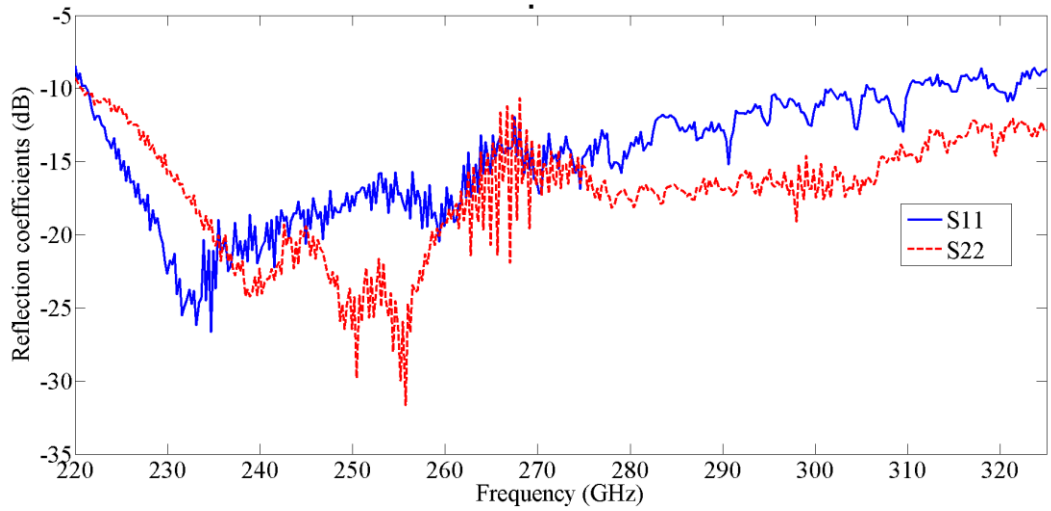


Figure 4.7: *Measured S-parameter (S_{11}, S_{22}) of the CPW with designed characteristic impedance Z_o = 50 Ω. The average value is about -15 dB, which means very low power of the transmitted signal has been reflected back to the same port.*

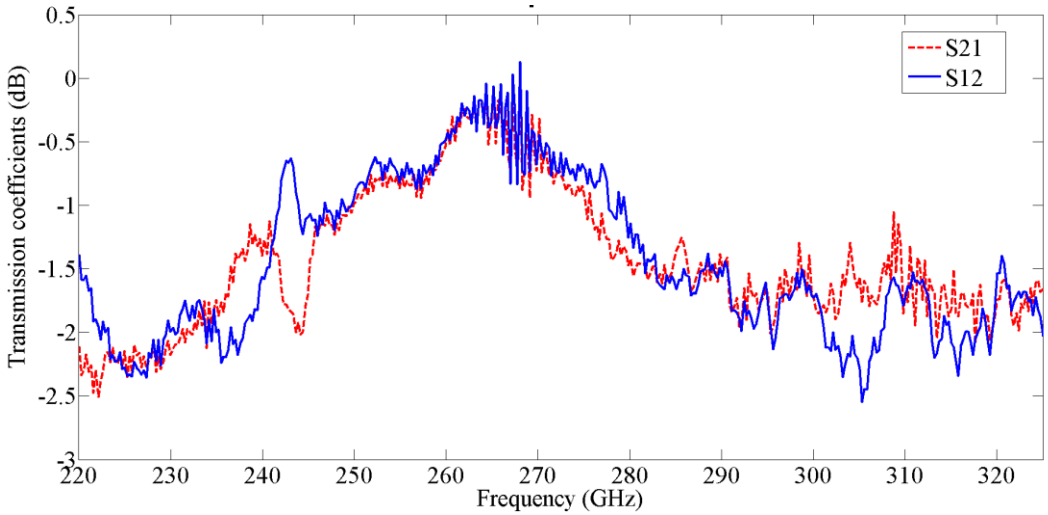
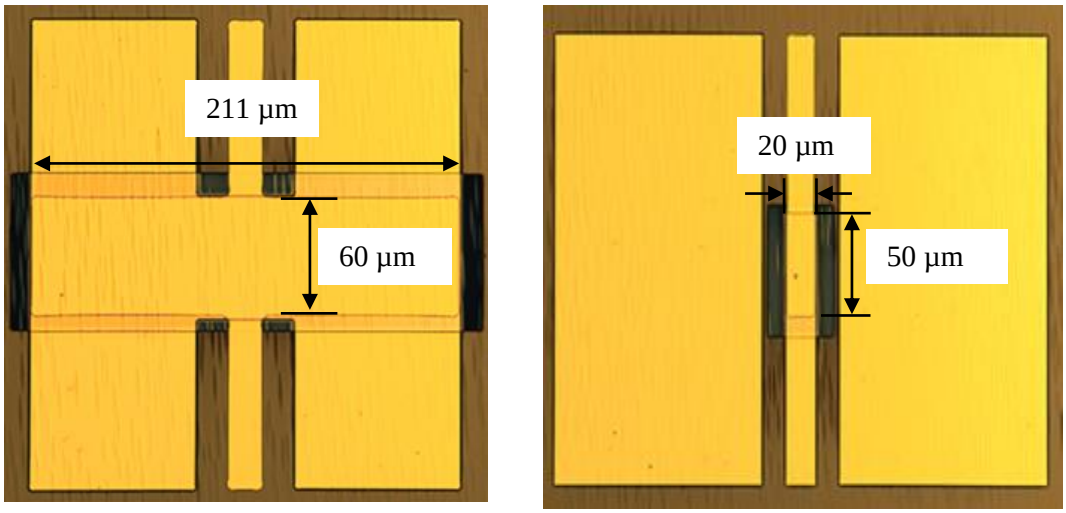


Figure 4.8: *Measured S-parameter (S_{21}, S_{12}) of the CPW with designed characteristic impedance Z_o = 50 Ω. The average value is around -1.5 dB which indicates that the CPW line perfectly transmit the signal from one port to the other.*

4.3.2 MIM Capacitors

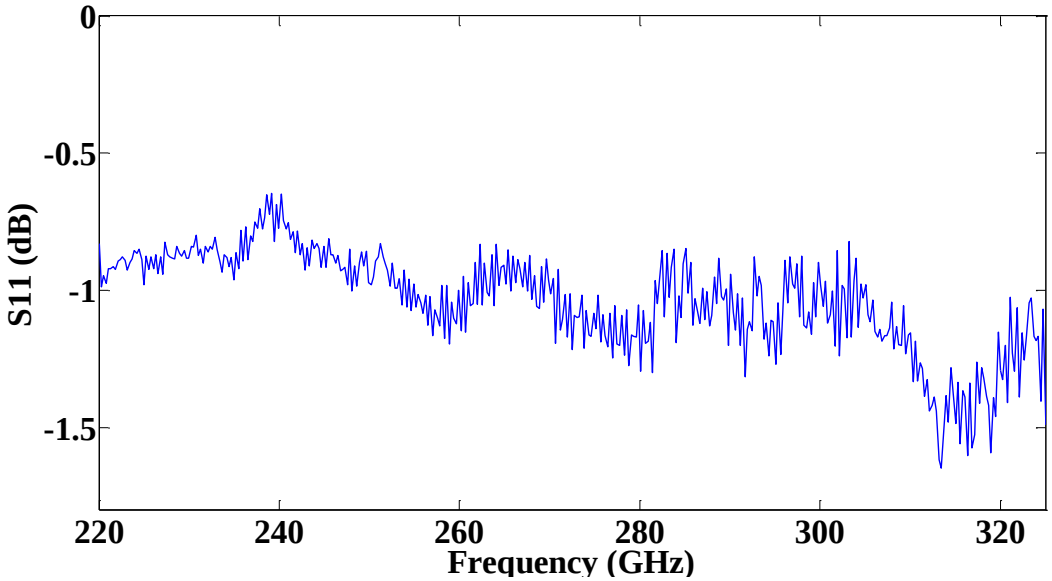


(a) (b)

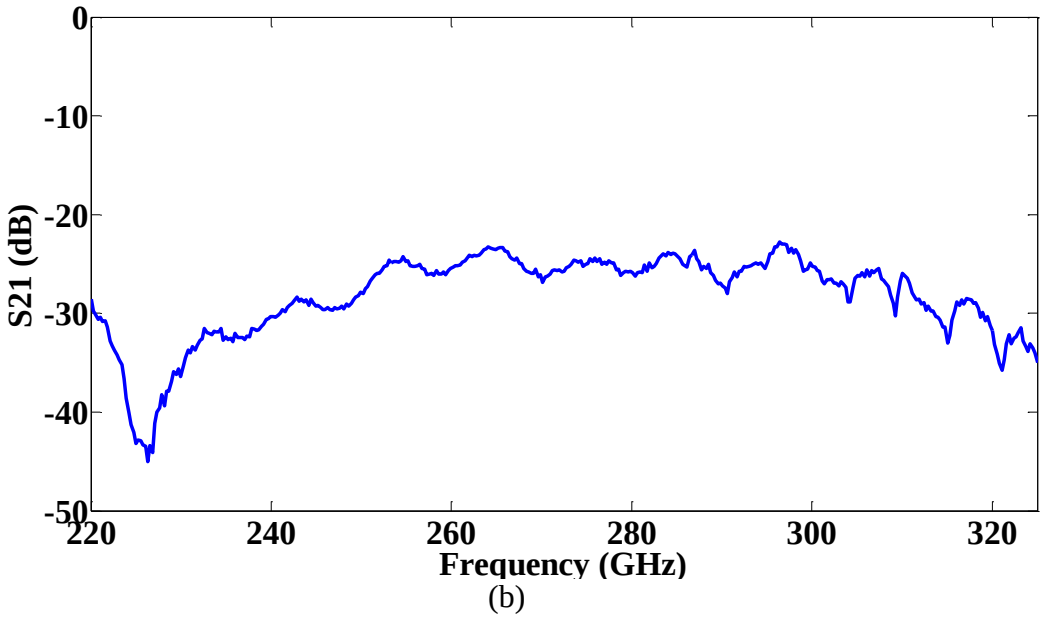
Figure 4.9: *Micrograph of fabricated MIM capacitor test structures. (a) Parallel capacitor (10 pF). (b) Series capacitor (800 fF).*

As described above, two types of MIM capacitors (parallel and series) were designed and used in the oscillator circuit. Test structures were designed and fabricated for capacitors characterisation. Figure 4.9 (a) shows a micrograph of fabricated MIM parallel capacitors, while the series one is shown in Figure 4.9 (b). The calculated capacitance values are 800 fF and 10 pF for the series and parallel capacitor, respectively. The measured return loss (S_{11}) and the insertion loss (S_{21}) for the parallel capacitor are shown in Figure 4.10 (a) and Figure 4.10 (b), respectively. The S-parameters of the parallel capacitor show the suitability of the design to act as a short circuit where the insertion loss, S_{21}, is below -20 dB for all frequencies in the J-band. The measured return loss (S_{11}) and the insertion loss (S_{21}) for the series capacitor are shown in Figure 4.11 (a) and Figure 4.11 (b), respectively. The series capacitor has acceptable performance in the measured band with average insertion loss of around 1dB although periodic feature (repeated every 10 GHz) was observed in Figure 4.11 (b). Future work is required

to investigate the reasons. The measured capacitance value for the parallel capacitor is 17 pF.

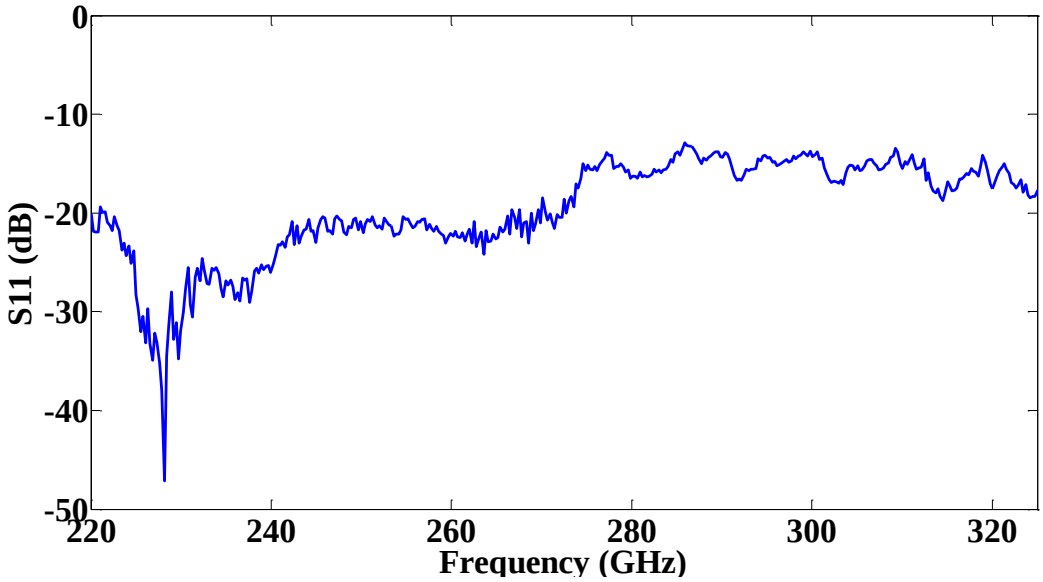


(a)

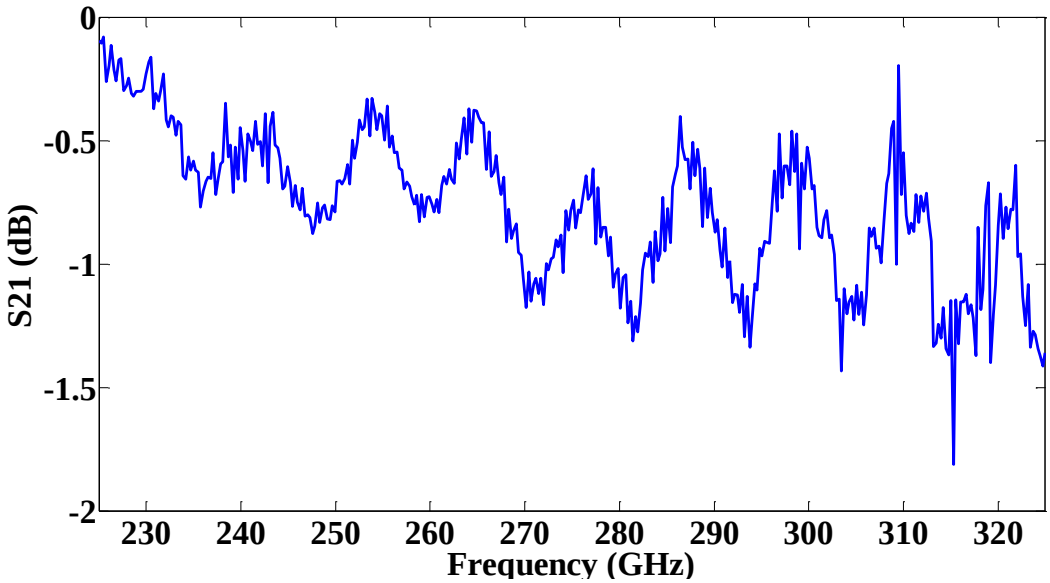


(b)

Figure 4.10: *Measured S-parameters of the parallel capacitor. (a) S_{11}. (b) S_{21}. The S-parameters show the suitability of the design to act as a short circuit where the insertion loss, S_{21}, is below -20 dB for all frequencies in the J-band.*



(a)



(b)

Figure 4.11: *Measured S-parameters of the series capacitor. (a) S_{11}. (b) S_{21}. The S-parameters show that the series capacitor has acceptable performance to block the DC and pass the RF signals in the J-band with average insertion loss of around 1dB.*

4.3.3 Thin-film Resistor

As described above, thin-film resistors were used in the RTD oscillators in this project. The thin-film used was 33 nm thick NiCr which has a sheet resistance, R_{sh} of 50 Ω/□. Different resistors values were designed and fabricated. Test structures were fabricated to measure the resistance and compare with the designed values. Figure 4.12 shows one of the fabricated NiCr resistor test structure with two identical resistors connected in parallel. The designed and measured values are compared in Table 4.2. The discrepancy between the theoretical and measured resistance values could be due to different reasons such as the non-uniform thickness due to variation in the deposition rate (measured variation is around ±10%) and contaminated interface between the NiCr and the contact pads. In addition, measured resistance of the same design but in different samples can also be different. However, large resistance values will not suppress bias oscillations and, thus, the oscillator output power of the desired signal will reduce.

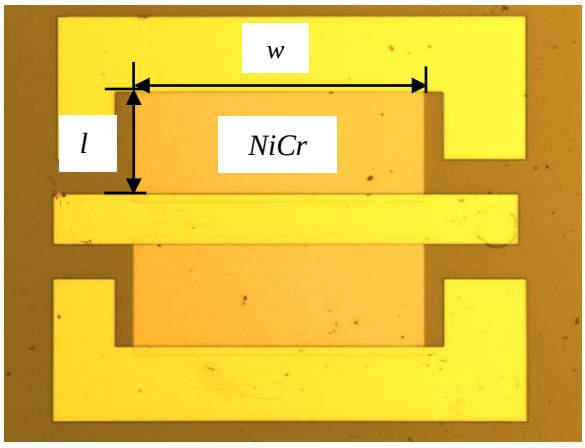


Figure 4.12: *Micrograph of fabricated NiCr film resistors.*

Table 4.2: *Designed and measured resistance of different NiCr film designs.*

Designed resistance (Ω)	***l (μm)***	***w (μm)***	***Measured resistance (Ω)***
21.7	*130*	*300*	*23.8*
22	*66*	*150*	*29*
10	*30*	*150*	*18*

4.4 Metal-Semiconductor Ohmic Contact and TLM Measurement

The metal-semiconductor contact resistance plays important role in the device performance. Low contact resistance is required in order to reduce the power consumption and obtain higher f_{max} [61], [93]. The Ohmic contact resistance of the RTD was investigated by transmission line model (TLM) test structures in this project. The TLM measurement structure consists of a series of identical metal-semiconductor contact pads separated by various distances as described in Figure 4.13. Mesa etching has to be performed in order to restrict the current direction between the two measured contact pads. For each pair of contact pads, the resistance between them are measured by applying four probes (two probes to apply voltage across the two contact pads and the other two probes to measure the current) as shown in Figure 4.14.

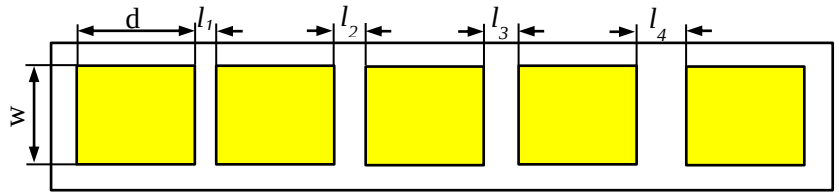


Figure 4.13*: Top view of the TLM test structure. A series of identical metal-semiconductor contact pads are separated by different distances l.*

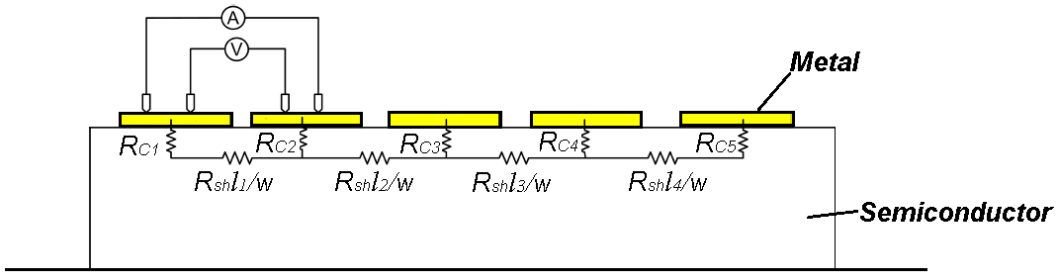


Figure 4.14: *Illustration of TLM measurement with four probes applied on a pair of metal-semiconductor contact pads.*

The measured resistance (R_t) is the sum of the contact resistance of the first contact (R_{C1}), the contact resistance of the second contact (R_{C2}), and the sheet resistance in-between the two contacts (R_{sh}). Assuming $R_C = R_{C1} = R_{C2}$, R_t can be written as

$$R_t = 2R_c + R_{sh}\frac{l}{w} \tag{4.7}$$

The total resistance (R_t) is measured between all pairs of contact pads which have different separation distances l. All measured R_t are plotted versus the corresponding distance l as shown in Figure 4.15. The intersection of the plotted line with the R-axis (at $l = 0$) equals to double the contact resistance, $2 \times R_C$. The intersection of the line with the l-axis (at $R_t = 0$) equals to double the transfer length, $2 \times l_T$, which is distance over which most of the current transfers from the semiconductor into the metal or vice versa [93]. The slope of the line equals to the semiconductor sheet resistance divided by the width of the contact pad, R_{sh}/w. The specific contact resistance ρ_C is calculated by [93]

$$\rho_C = l_T^2 R_{sh} \tag{4.8}$$

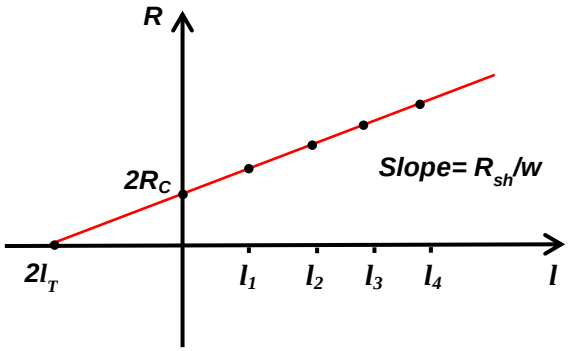


Figure 4.15: *Typical plot of measured resistances versus contact pads separation distances obtained from TLM technique.*

TLM test structures were fabricated with a series of nine contact pads with separation distances of 1 µm, 2 µm, 3 µm, 5 µm, 7 µm, 9 µm, 11 µm, 13 µm, and 15 µm. The fabrication process steps included the deposition of contact metal Ti/Pd/Au (20/30/150 nm) followed by wet etching around the TLM structure which is completely covered by etching mask (S1805). Two structures with the same design were fabricated to investigate the Ohmic contact at the emitter layer (the top highly n-type doped contact layer ($In_{0.53}Ga_{0.47}As$) of the RTD device) and collector layer (the bottom highly n-type doped contact layer ($In_{0.53}Ga_{0.47}As$) of the RTD device). Before the metal deposition in Plassys IV, argon gun treatment for 20 seconds was carried out under vacuum to remove the oxidation layer over InGaAs. The deposition started immediately after the argon gun treatment, and so, the sample will not be exposed to the atmosphere which prevents the formation of oxidation layer. Figure 4.16 shows micrograph of a fabricated TLM test structure. The measured resistance values are plotted in Figure 4.17 and tabulated in Table 4.3 .

***Figure 4.16**: Micrograph of fabricated TLM test structure.*

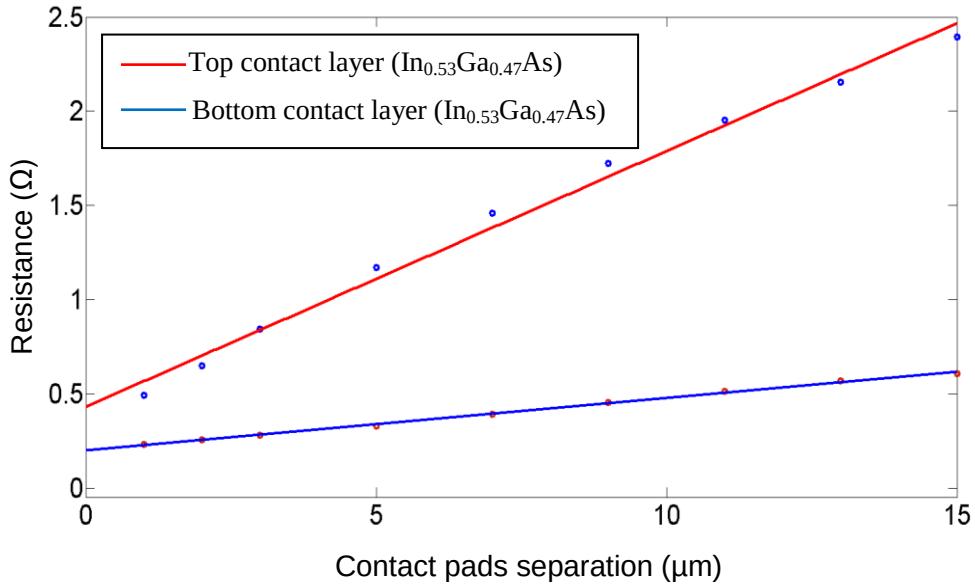


***Figure 4.17:** The measured total resistance R_t as a function of contacts pads separation distance l.*

The extracted contact resistance (R_c), the transfer length (l_T), the sheet resistance (R_{sh}), and the specific contact resistance (ρ_C) are listed in Table 4.4. The achieved specific contact resistance ρ_C = 51.6 to 55.38 ($\Omega\ \mu m^2$), which is worse by less than one order of magnitude compared with ($0.73 \pm 0.44\ \Omega.\mu m^2$) reported in [81]. However, this value is about 3.5 times better than the values reported in [32] which could be due to the use of argon gun treatment, and is sufficient to realise oscillation frequencies above 300 GHz as will be discussed in the next chapter.

Table 4.3: *Measured total resistance R_t as a function of contacts pads separation distance l.*

Gap (μm)	***Resistance (Ω)***	
	Emitter (Top contact)	***Collector (bottom contact)***
1	*0.49*	*0.23*
2	*0.65*	*0.26*
3	*0.84*	*0.28*
5	*1.17*	*0.33*
7	*1.46*	*0.39*
9	*1.72*	*0.45*
11	*1.95*	*0.51*
13	*2.15*	*0.57*
15	*2.39*	*0.6*

Table 4.4: *Extracted TLM data from test structures.*

	R_C (Ω)	l_T (μm)	R_{sh} (Ω/□)	ρ_C (Ω μm^2)
Emitter (Top contact)	*0.21*	*1.6*	*20.34*	*51.6*
Collector (bottom contact)	*0.1*	*3.6*	*4.14*	*53.7*

4.5 Summary

In this chapter, the main fabrication processes to fabricate RTD devices were described. Designs of passive components including MIM capacitors, coplanar waveguide, and thin-film resistors, that are used in RTD oscillator circuits were presented with characterisation results. Description of shorted polyimide-based microstrip line that can be employed in the RTD oscillators circuits and provides very low resonating inductances with relatively large dimensions were also given. In addition, characterisation of the Ti/Pd/Au-InGaAs contact resistance was characterised using linear TLM test structures.

Chapter 5 Characterisation of RTD Devices and Oscillators

5.1 Introduction

This chapter presents the characterisation of the RTD devices used to realise the RTD oscillators in this project. Characterisation of different oscillators that employed a different number and sizes of RTD devices are described as well. These oscillators employed either shorted coplanar waveguide (CPW) or shorted microstrip lines with different characteristic impedances (Z_o) to realise small values of resonating inductances that, along with relatively large sized RTD devices, can produce high power and high oscillation frequencies at the same time. All fabrication processes were carried out using photolithography.

5.2 RTD Device DC Measurement

Different RTD devices with different sizes (3 μm × 3 μm, 4 μm × 4 μm, and 5 μm × 5 μm) were used in the RTD oscillators in this project. To investigate the DC characteristics of these devices and extract important parameter before designing RTD oscillators, test structures were fabricated and measured. Figure 5.1 shows a scanning electron microscope (SEM) image of a fabricated RTD, while Figure 5.2 shows the measured I-V characteristics of the various RTD device sizes.

From Figure 5.2, the peak voltage V_p, the valley voltage V_V, the peak current I_p, the valley current I_V, the peak-valley voltage difference ΔV, the peak-valley current difference ΔI, the absolute value of negative conductance $G_n = \frac{3\Delta I}{2\Delta V}\ (mS)$, and the peak current density J_p are estimated and listed in Table 5.1.

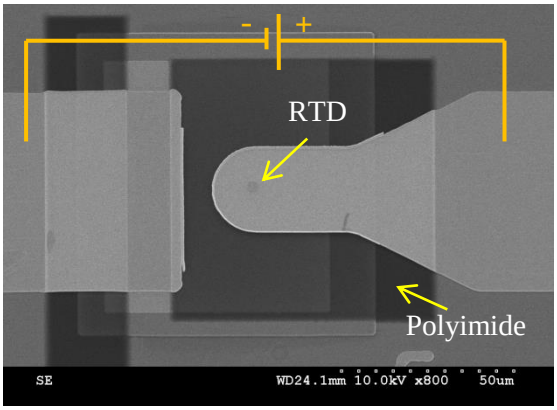


Figure 5.1: *A SEM image of a fabricated RTD for DC characterisation.*

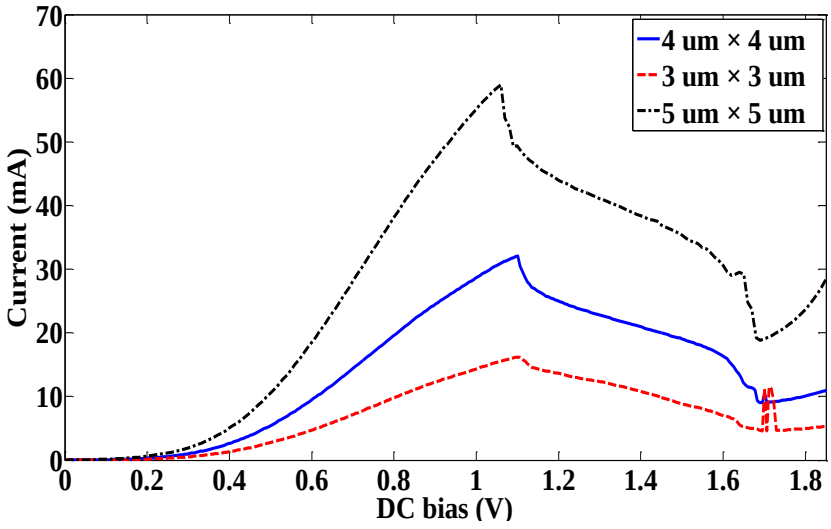


Figure 5.2: *Measured I-V characteristics of single 3 µm × 3 µm, 4 µm × 4 µm, and 5 µm × 5 µm RTD devices. The devices exhibit negative differential resistance (NDR) region when biased between ~1.13V and 1.7 V.*

Table 5.1: *Analysis of the measured I-V characteristcs of different RTD devices.*

RTD size (μm^2)	V_P (V)	V_V (V)	I_P (mA)	I_V (mA)	ΔV (V)	ΔI (mA)	G_n (mS)	J_P (mA/μm^2)
3 × 3	1.12	1.7	15	4.5	0.58	10.5	27.2	1.7
4 × 4	1.1	1.68	32	8	0.58	24	62	2
5 × 5	1.07	1.67	59	18	0.6	41	102.5	2.4

The estimated RF powers delivered to the load 20 *mS* (50 Ω spectrum analyser), P_L using Equation 2.24, and the estimated maximum RF power, P_{max} using Equation 2.25 for different device sizes in the oscillator circuits are listed in Table 5.2. The calculated maximum frequencies f_{max} (using Equation 1.2) are also listed in Table 5.2 assuming different specific contact resistance values (ρ_C) which are ρ_C = 51.6 Ω μm^2 that was achieved in this project, ρ_C = 6.3 Ω μm^2 which was reported in [78], and ρ_C = 0.73 Ω μm^2 which was reported in [81]. The calculated RTD self-capacitance (using Equation 1.1) is 3.56 fF/μm^2. Thus, the self-capacitances for 3 μm × 3 μm device, 4 μm × 4 μm device, and 5 μm × 5 μm device are 32 fF, 57 fF, and 89 fF, respectively.

Table 5.2: *Estimated RF power delivered to the 50 Ω load (P_L) and the maximum power P_{max} in addition to the calculated maximum frequency (f_{max}) for different device sizes. The maximum frequencies f_{max} are calculated for different specific contact resistance using Equation 1.2.*

RTD size (μm^2)	P_L **(mW)**	P_{max} **(mW)**	f_{max} **(THz)**		
			ρ_C **= 51.6 Ω μm^2 (Realised in this thesis)**	ρ_C **= 6.3 Ω μm^2** [78]	ρ_C **= 0.73 Ω μm^2** [81]
3 × 3	0.88	1.1	0.34	0.98	2.9
4 × 4	2.2	2.6	0.39	1.1	3.25
5 × 5	2.9	4.6	0.4	1.14	3.35

5.3 Frequency and Power Measurement Setup

The RTD oscillators in this project were designed for on-wafer characterisation. The spectrum analyser used in this project was the E4448A spectrum analyser from Agilent Technologies which has upper frequency limit of 50 GHz. For higher frequencies measurements (from 50 GHz and 325 GHz) an external mixer to down-convert the frequencies is required. Figure 5.3 shows the measurement setup. The spectrum analyser graphically plots the amplitude of the measured

signal as a function of frequency. However, as the characterisation of THz oscillators using a 50 GHz spectrum analyser with down conversion mixers is time consuming and non-trivial, a recently developed quicker technique which uses a vector network analyser (VNA) was used to identify the oscillation frequencies of the circuits [94]. The setup is shown in Figure 5.4. The VNA detection technique is also useful in detecting low power oscillation signals where using the spectrum analyser with mixer to identify the signal would be challenging especially when the mixer introduces high loss levels (typically 50 to 80 dB) and when the noise floor level is high. Therefore, by using the VNA detection technique, the oscillation signals were known prior to using the spectrum analyser for detailed characterisation. The VNA has to be calibrated for one port measurement. The oscillator is biased through a ground-signal-ground (GSG) probe and the return loss (S_{11}) is monitored to see any sharp gain which indicates the existence of an external oscillation frequency being sensed by the VNA.

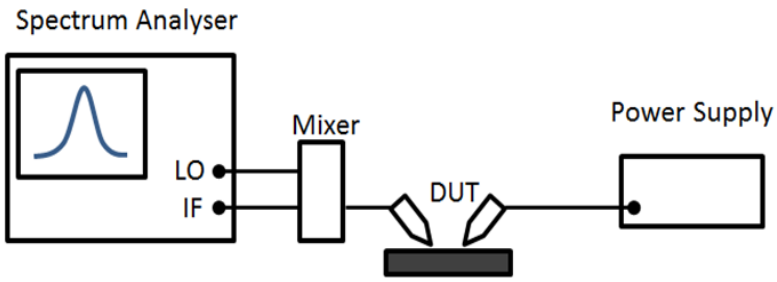


***Figure 5.3**: Schematic block diagram showing on-wafer frequency measurements setup using a spectrum analyser with mixer. The oscillator is biased through a ground-signal-ground (GSG) probe.*

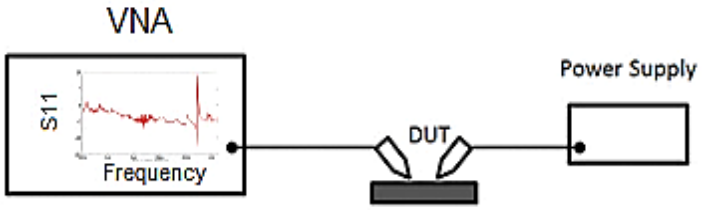


***Figure 5.4**: Schematic block diagram showing on-wafer frequency measurements setup using a vector network analyser. The oscillator is biased through a ground-signal-ground (GSG) probe and the return loss (S_{11}) is monitored to see any sharp gain which indicates the existence of an external oscillation frequency being sensed by the VNA.*

As the conversion loss of the mixer is not accurately specified, the actual output power was measured by power meter (Erikson PM4) with the setup illustration shown in Figure 5.5. The power sensor is used to pick up the related RF signal, and the power metre processes and displays the data. Since the input of power sensor head is WR-10 (W-band) waveguide, a WR-3 to WR-10 tapered waveguide was used as shown in Figure 5.5.

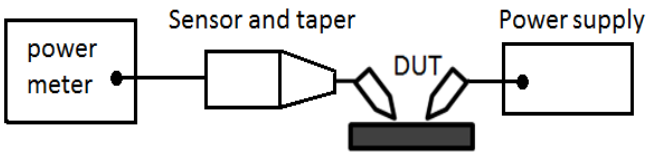


***Figure 5.5:** Schematic block diagram showing on-wafer power measurements setup using a power meter.*

5.4 Characterisation of RTD Oscillators in CPW Technology

5.4.1 Single RTD Oscillators

RTD oscillators employing one RTD device were designed and fabricated with shorted 50 Ω CPW line to realise the resonating inductance. Two device sizes, 4

μm × 4 μm and 5 μm × 5 μm were employed in two different oscillators with the same layout shown in Figure 5.6, but different CPW lengths. The 50 Ω CPW line structure consists of 20 μm wide signal line and 13.8 μm gap to the ground planes, and shorted by the capacitor C_e.

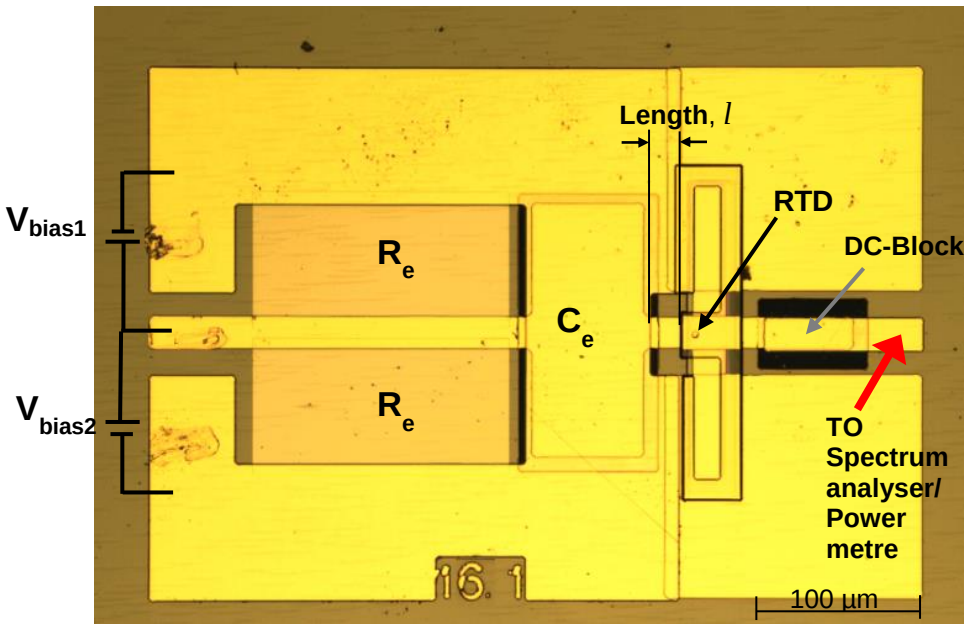


Figure 5.6: *Micrograph of the fabricated single RTD oscillators showing the circuit layout. Two device sizes were employed, 4 μm × 4 μm and 5 μm × 5 μm, with shorted 50 Ω CPW lines to realise the resonating inductances.*

For the single 4 μm × 4 μm oscillator, the measured oscillation frequency was 244 GHz with measured power of 0.2 mW (-7 dBm) when the bias voltage was $V_{bias} = 1.27$ V ($I_{bias} = 92$ mA). The output power has been compensated for the probe and taper insertion losses which is 3.5 dB as per manufacturer specifications. Figure 5.7 shows the measured spectrum. The theoretical designed frequency was 237 GHz (using Equation 2.27) with inductance realised by 18 μm long CPW shorted line. The DC-to-RF conversion efficiency is $\frac{0.2}{117} \times 100 = 0.17$ % considering the total DC power consumption in the circuit. The two

stabilising resistors R_e (R_e = 29 Ω) have a DC current flowing across them as $i_{Re} = \frac{V_{bias}}{R_e/2} = \frac{1.27}{14.5} = 87.6\,mA$. The current flowing through the diode was $I_{bias} - i_{Re} = 4.4\,mA$. Therefore, the DC power dissipated over the RTD was 5.6 mW. The DC-to-RF conversion efficiency, without considering the DC power dissipated by the stabilising resistors, was $\frac{0.2}{5.6} \times 100 = 3.6\,\%$.

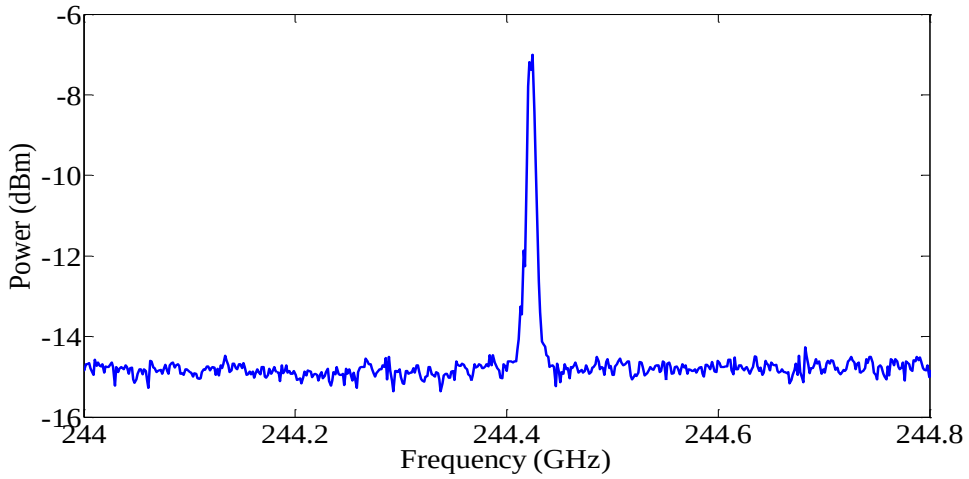


Figure 5.7: *Measured spectrum of the 4 μm × 4 μm RTD oscillator with 18 μm long shorted 50 Ω CPW line when V_{bias} = 1.27 V and I_{bias} = 99 mA.*

For the single 5 μm × 5 μm oscillator, 233 GHz oscillation frequency was observed with output power of 0.264 mW (-5.8 dBm) when the bias voltage was $V_{bias} = 1.29$ V ($I_{bias} = 105$ mA). Figure 5.8 shows the measured spectrum. The theoretical designed frequency was 269 GHz (using Equation 2.27) with inductance realised by 9 μm long CPW shorted line. The DC-to-RF conversion efficiency is $\frac{0.264}{135} \times 100 = 0.2\,\%$ considering the total DC power consumption in the circuit. The DC current flowing across the resistors was $i_{Re} = \frac{V_{bias}}{R_e/2} = \frac{1.29}{14.5} = 89\,mA$. The current flowing through the diode was $I_{bias} - i_{Re} = 10.3\,mA$.

Therefore, the DC power dissipated over the RTD was 16 mW. The DC-to-RF conversion efficiency, without considering the DC power dissipated by the stabilising resistors, was $\frac{0.2}{16} \times 100 = 1.25\ \%$. A summary of the measurement results is tabulated in Table 5.3.

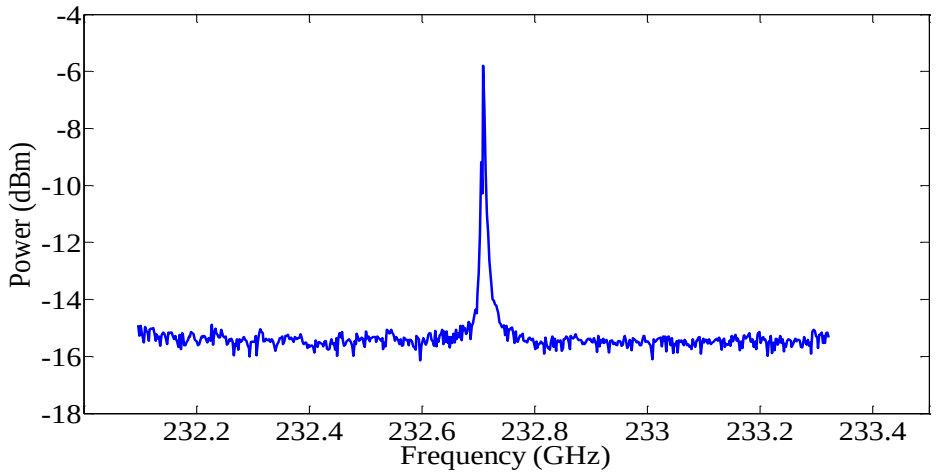


Figure 5.8: *Measured spectrum of the 5 μm × 5 μm RTD oscillator with 9 μm long shorted 50 Ω CPW line when V_{bias} = 1.29 V and I_{bias} = 105 mA.*

Table 5.3: *Measurement results of the single RTD oscillators.*

RTD size (μm^2)	***Shorted CPW length (μm)***	***Designed frequency (GHz)***	***Measured oscillation frequency (GHz)***	***Measured Power (mW/dBm)***	***DC-to-RF conversion efficiency (%)***
16	*18*	*237*	*244*	*0.2/-7*	*0.17*
25	*9*	*269*	*233*	*0.264/-5.8*	*0.2*

To increase the oscillation frequency using this layout, the length of the CPW needs to be reduced in order to realise lower inductance values. Figure 5.9 plots the 50 Ω CPW length versus frequency for oscillators employing single RTD device (4 μm × 4 μm and 5 μm × 5 μm). Plots for double RTD oscillator (with single inductance *L* and calculated using Equation 2.29) are also included in

Figure 5.9. The maximum calculated frequency from the four plots, assuming the extremely 2 µm short CPW lines, are listed in Table 5.4. It can be seen that achieving high frequencies (> 0.7 THz) is challenging when the oscillator circuit employs such large devices and resonating inductance realised by 50 Ω CPW line. This is mainly because the inductance value per unit length is relatively high in the 50 Ω CPW line (0.44 pH/µm for the line length up to 30 µm) and cannot compensate for the self-capacitance of the large size RTD devices. Other option is to reduce the device size but at the expense of lower power. In this project, new structures that have lower inductance value per unit length were designed and realised. They were based on shorted CPW lines but with lower characteristic impedance values. Details are given in the next sub-section.

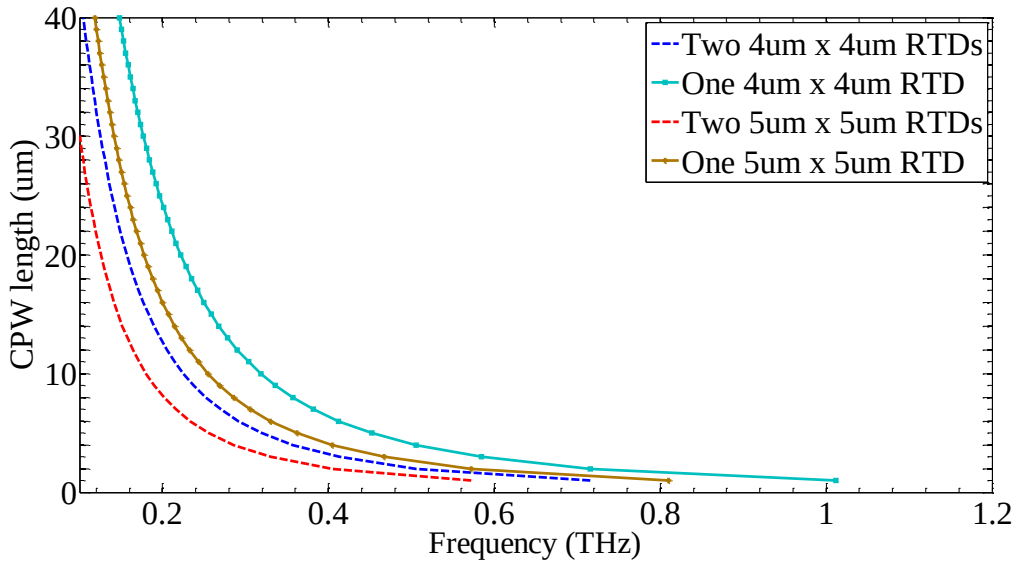


Figure 5.9: *Calculated oscillation frequency of different oscillators employing different RTD device sizes versus the length of the shorted 50 Ω CPW line.*

Table 5.4: *Calculated frequencies with 2 µm 50 Ω CPW lines. All frequencies are below the maximum frequencies assuming very low specific contact resistance reported in* [78] *or in* [81] *as specified in Table 5.2.*

Number and size of RTDs	***Calculated frequency (THz)***
One 4 µm × 4 µm	*0.72*
Two 4 µm × 4 µm	*0.5*
One 5 µm × 5 µm	*0.57*
Two 5 µm × 5 µm	*0.4*

5.4.2 Double RTD Oscillators

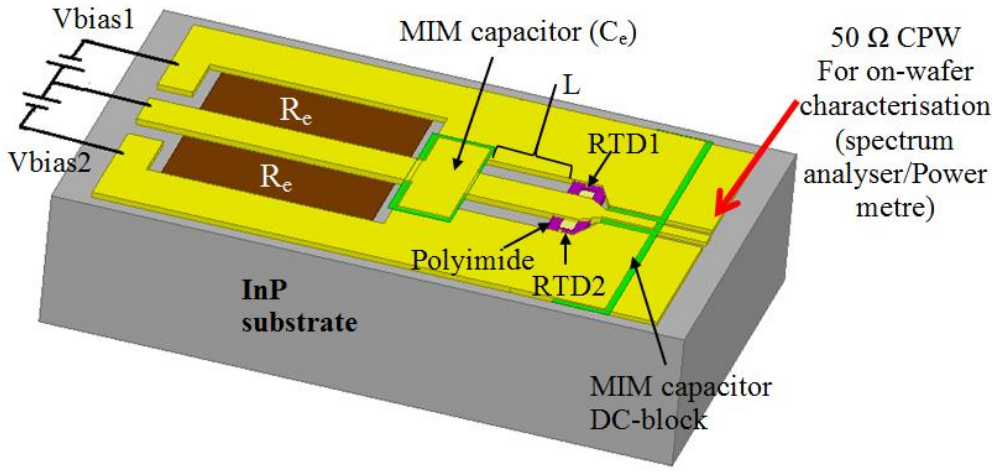


Figure 5.10: *Schematic structure for the double RTDs oscillator.*

The double RTD oscillator layout, which was described in Chapter 2, has two RTD devices connected in parallel (to increase the power) and one resonating inductor *L*. Figure 5.10 shows a schematic structure for the double RTDs oscillator in which the inductor *L* is realised by shorted CPW line. As discussed in the previous sub-section, realisation of very high frequency with large size RTD devices and 50 Ω CPW line for inductance is challenging. In this project new oscillator layout with large RTD devices and new structures that can offer low resonating inductance for high power and high oscillation frequencies was

designed and realised. The new inductance structures are shorted CPW lines with < 50 Ω characteristic impedance. As was described in Chapter 4 (Equation 4.6), a line with lower Z_o has lower inductance per unit length. Thus, at very high frequencies, for an oscillator employing a given RTD device size, lower Z_o line will facilitate the fabrication process using photolithography because the dimension limitation is largely eliminated.

A series of different oscillators each employs two RTD devices of same size (3 μm × 3 μm or 4 μm × 4 μm) and different CPW lines of different Z_o (50 Ω, 32 Ω, and 25 Ω) and lengths were designed, fabricated, and characterised in this project. Figures 5.11, 5.12, and 5.13 show micrographs of the fabricated double RTD oscillators with 50 Ω, 32 Ω, and 25 Ω CPW lines, respectively. A zoom in on each CPW line is shown on the right hand side of the figure with dimensions which give the corresponding characteristic impedance.

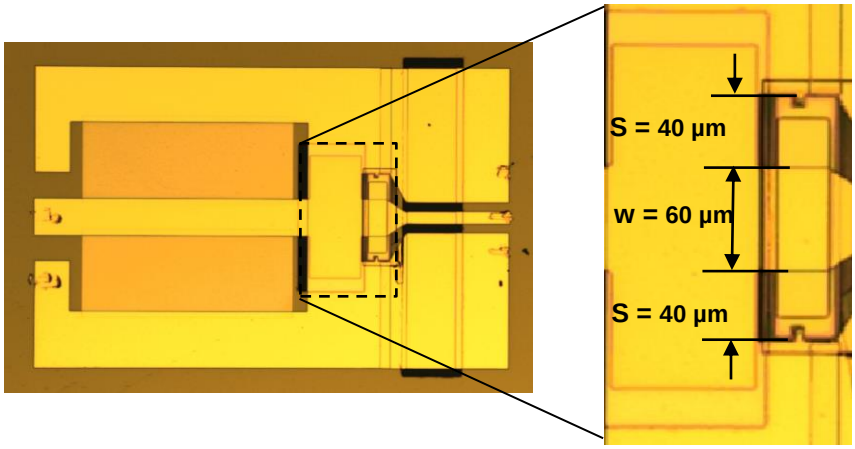


Figure 5.11: *Micrograph of the fabricated double RTD oscillators with shorted 50 Ω CPW lines to realise the resonating inductances. The CPW dimensions are shown in the zoomed area.*

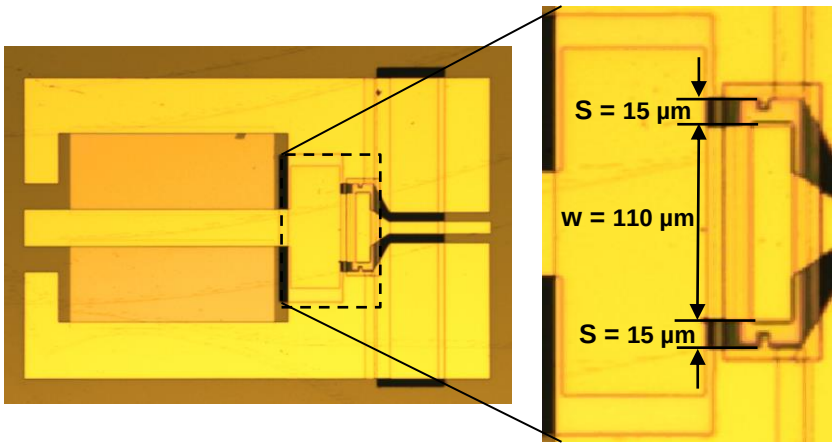


Figure 5.12: *Micrograph of the fabricated double RTD oscillators with shorted 32 Ω CPW lines to realise the resonating inductances. The CPW dimensions are shown in the zoomed area.*

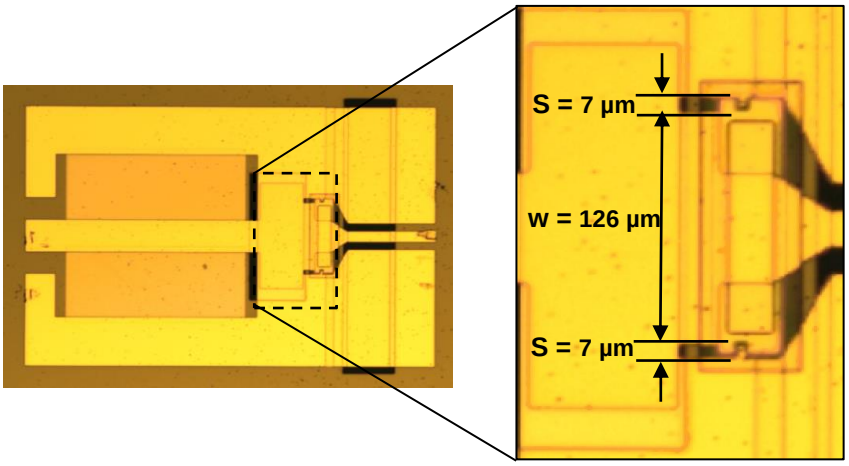


Figure 5.13: *Micrograph of the fabricated double RTD oscillators with shorted 25 Ω CPW lines to realise the resonating inductances. The CPW dimensions are shown in the zoomed area.*

Characterisation results of oscillators with two 4 µm × 4 µm RTD devices are presented here. An oscillation frequency of 308 GHz was observed for a 10 µm long shorted CPW with Z_o = 25 Ω, while similar frequency (304 GHz) was observed for 3 µm shorted CPW with Z_o = 50 Ω. For an oscillator with 7 µm long

50 Ω shorted CPW, the oscillation frequency was 245 GHz, while a higher oscillation frequency of 309 GHz was observed from oscillator with same CPW length but with Z_o = 25 Ω, as expected. Oscillation frequency of 254 GHz was observed with similar length (8 μm) of 32 Ω CPW, the frequency in between the measured 245 GHz (with 7 μm long 50 Ω CPW) and 309 GHz (with 7 μm long 25 Ω CPW). Finally, for an oscillator with two 3 μm × 3 μm RTD devices on the sample with 10 μm long shorted 50 Ω CPW, 284 GHz oscillation frequency was observed.

Table 5.5 summarizes the measured and designed (calculated) oscillation frequencies of the different oscillators with different device sizes and different shorted CPW designs (lengths and Z_o). The results in Table 5.5 show that higher oscillation frequencies are achievable with longer CPW lines of lower Z_o which proves the feasibility of generating high THz frequency even when large size RTD devices are used. It can also be seen that small deviations from the designed frequency can be achieved with around 3-5 % deviation although, at higher frequencies this percentage corresponds to deviation of few ten of GHz which could be due to additional parasitic inductances.

Table 5.5: *Designed and measured frequency of the double RTD oscillators.*

RTD devices		***Shorted CPW design***		***Oscillation frequency***		
Size (μm^2)	***Number***	***Length (μm^2)***	***Impedance (Ω)***	***Designed (GHz)***	***Measured (GHz)***	***Deviation (%)***
16	*2*	*7*	*50*	*272*	*245*	*10*
16	*2*	*7*	*25*	*356*	*309*	*13*
16	*2*	*3*	*50*	*413*	*304*	*26*
16	*2*	*10*	*25*	*319*	*308*	*3.4*
16	*2*	*8*	*32*	*317*	*254*	*19.8*
9	*2*	*10*	*50*	*300*	*284*	*5.3*

The maximum measured output power for various oscillators are tabulated in Table 5.6 together with the corresponding frequency. The table has measurement results from two (2) identical oscillators fabricated on the same epitaxial material in different runs, labelled sample1 and sample2, to investigate the performance repeatability and reproducibility of the process. It can be seen that consistently high output powers of around 0.2 – 0.5 mW was achieved across various oscillator designs in the 245 – 313 GHz range. The powers in the table have been compensated for the probe and taper insertion losses which is 3.5 dB as per manufacturer specifications.

It can be noted that the difference between the calculated and measured frequency is larger for shorter CPW lines. This could be to the errors in photolithography alignment. For example, if the misalignment was ± 1 µm, the change in the CPW lines lengths will be ± 33 % and ± 10 % in the 3 µm and the 10 µm CPW lines, respectively. Thus, the change in the frequency would be larger for very short CPW lines (See Figure 5.17 where sharp variation in the calculated frequency is observed when a small change occurs in the length of the very short CPW lines).

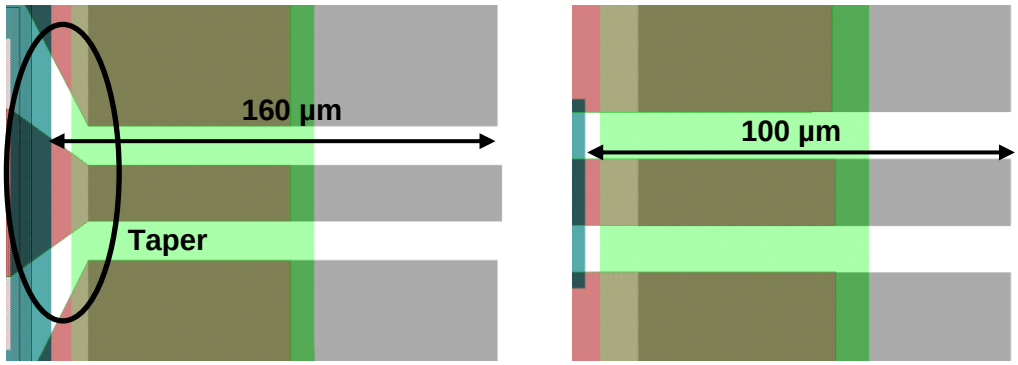
The typical DC power consumption of the RTD oscillators is ~ 250 mW, which results in a DC to RF conversion efficiency of ~ 0.2%. The measured output powers are only small fractions of the theoretical maximum given Table 5.2. This could be improved with optimised epitaxial designs to increase ΔV [29] and oscillator design/layout to omit or remove R_e and reducing the Ohmic contact resistance, in addition to improved impedance matching between the RTD negative differential conductance and the load conductance.

Table 5.6: *Measured frequency and power for different oscillator designs on sample1 and sample2.*

		Sample1		***Sample2***	
Oscillator design	***Calculated Frequency (GHz)***	***Frequency (GHz)***	***Power (mW)***	***Frequency (GHz)***	***Power (mW)***
3 µm long 50 Ω CPW Two 4 µm × 4 µm RTDs	*413*	*304*	*0.33*	*286*	*0.18*
10 µm long 25 Ω CPW Two 4 µm × 4 µm RTDs	*319*	*308*	*0.31*	*305*	*0.21*
7 µm long 25 Ω CPW Two 4 µm × 4 µm RTDs	*356*	*309*	*0.26*	*313*	*0.3*
7 µm long 50 Ω CPW Two 4×4 µm2 RTDs	*272*	*245*	*0.42*	*245*	*0.11*
10 µm long 50 Ω CPW Two 3 µm × 3 µm RTDs	*300*	*284*	*0.46*	*289*	*0.11*
8 µm long 32 Ω CPW Two 4 µm × 4 µm RTDs	*317*	*254*	*0.4*	*285*	*0.33*

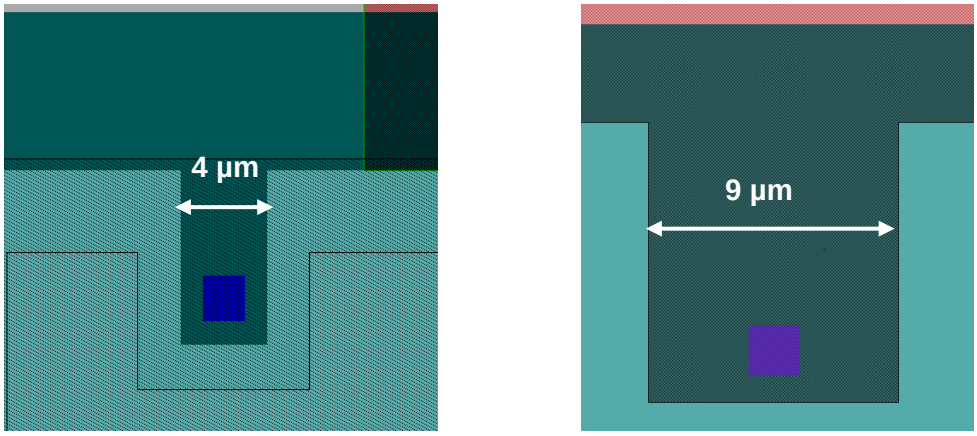
For these reasons, another fabrication run with optimised double RTD oscillator layout was realised and characterised in this project. The main change in the new optimised layout was in the RF pads on which the RF probes land to characterise the oscillators. Figure 5.14 illustrate the difference between the two pads. In the first layout, a taper was used to match the RF probes dimensions as can be seen in Figure 5.14 (a). This tapering would alter the line impedance and cause some

losses. In the optimised layout in Figure 5.14 (b) this tapering was eliminated. As such, the line has uniform impedance. In addition, the length of the pad in the optimised layout was shorter than that used in the first layout. At very high frequencies, the attenuation (in dB per unit length) would be high. Another optimisation was done in the interconnection between the top contact of the RTD and the pad metal. As can be seen in Figure 5.15 (a) the metal pad was narrow compared to that in the optimised layout shown in Figure 5.15 (b). This would reduce the line parasitic inductance and resistance, and dissipate less power. From the new optimised layout, higher power of 0.593 mW (-2.3 dBm) was measured at 312 GHz from the circuit that employs two 4 µm × 4 µm RTD devices and 13 µm long 50 Ω CPW line. The calculated frequency was 200 GHz which means 112 GHz higher compared to the measured one. A possible reason could be the reduced parasitic inductance in the circuit. Figure 5.16 shows all the spectrum measurement results for various double RTD oscillators.



(a) (b)

Figure 5.14: *The RF pads of the two double RTD oscillator layouts. (a) The first layout with CPW tapering to match the GSG probes size. The length of the pad is 160 µm. (b) The optimised layout with no tapering and shorter length of 100 µm.*



(a) (b)

Figure 5.15: *The interconnection between the top contact of the RTD and the pad metal in the two double RTD oscillator layouts. (a) The metal pad in the first layout is narrow. (b) The optimised layout employs wider metal pad which has reduced parasitic inductance.*

The experimental results presented above prove the feasibility of generating high THz frequency even when large size RTD devices are used. The oscillator configuration can employ two RTD devices to potentially produce higher power compared to a single RTD oscillator. Although the equivalent device capacitance of the two RTD devices is twice that of a single one, high oscillation frequencies can still be easily achieved with low inductance values realised by low Z_o shorted CPW lines. Figure 5.17 plots the calculated oscillation frequency versus shorted CPW lengths of different Z_o and different RTD device sizes in the oscillator circuits. They show that 10 µm CPW long lines can be used to realise oscillators up to about 600 GHz, and extremely 2 µm short lines, this can reach 1.4 THz. However, this requires high alignment to avoid/reduce changing in the length of the CPW lines.

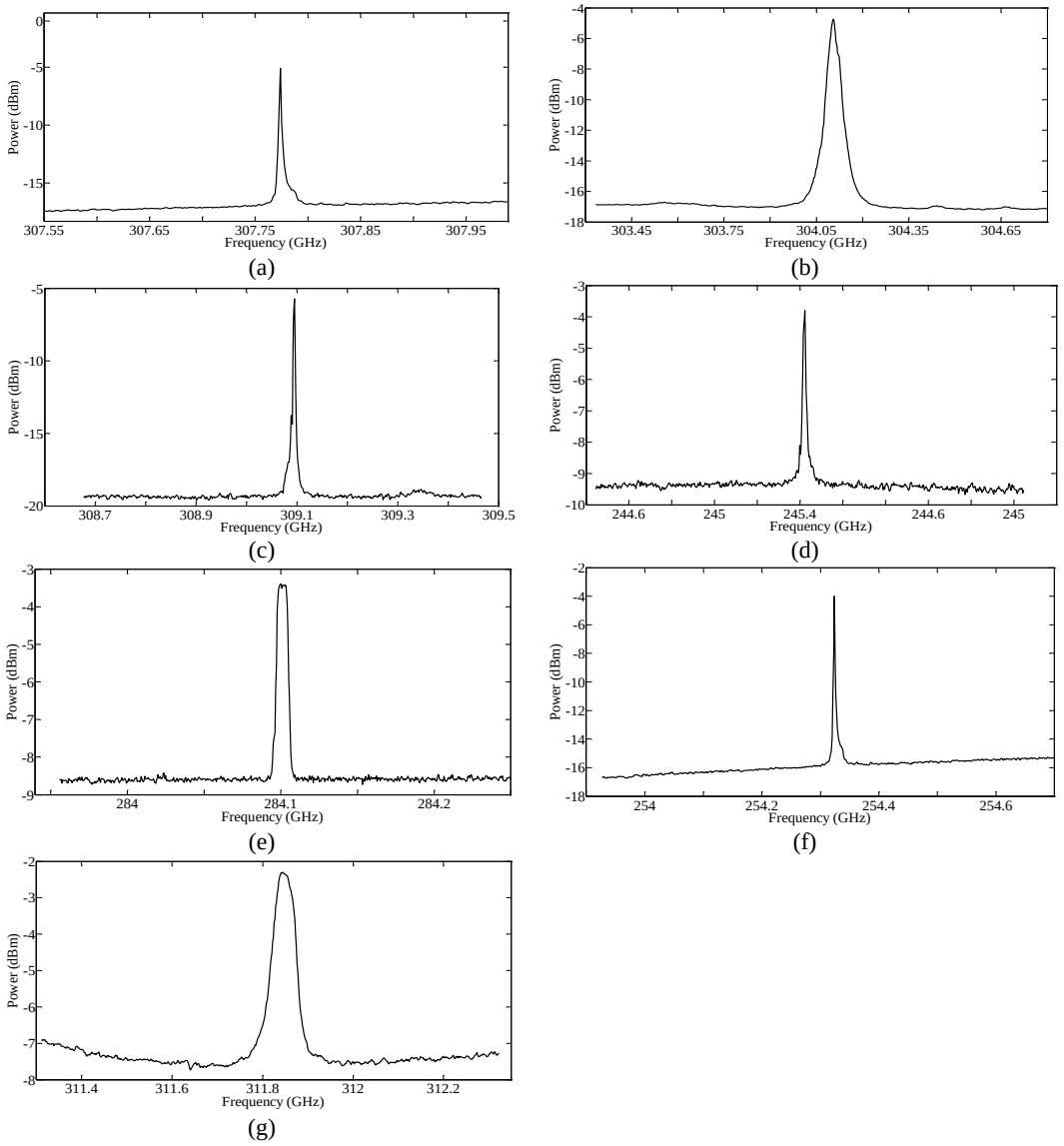


Figure 5.16: *Measured spectrum of the double oscillators with different designs (a) 10 μm long 25 Ω CPW and two 4 μm × 4 μm RTDs. (b) 3 μm long 50 Ω CPW and two 4 μm × 4 μm RTDs. (c) 7 μm long 25 Ω CPW and two 4 μm × 4 μm RTDs. (d) 7 μm long 50 Ω CPW and two 4 μm × 4 μm RTDs. (e) 10 μm long 50 Ω CPW and two 3 μm × 3 μm RTDs. (f) 8 μm long 32 Ω CPW and two 4 μm × 4 μm RTDs. (g) 13 μm long 50 Ω CPW and two 4 μm × 4 μm RTDs.*

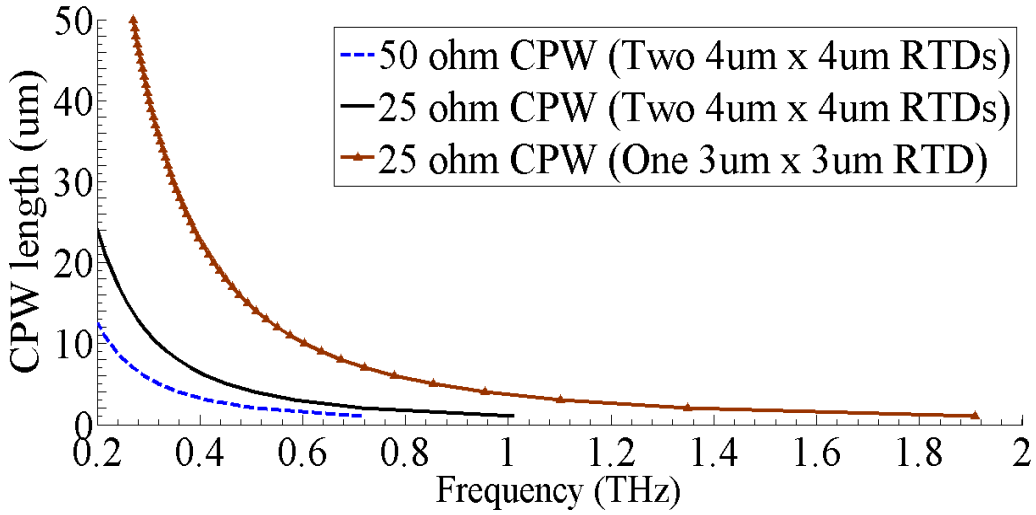


Figure 5.17: *Calculated oscillation frequency versus CPW length of different Z_o and different RTD device sizes employed in the oscillator circuits.*

5.4.3 Coupled RTD Oscillators

The power combining circuit which is based on mutual coupling between two individual oscillators were designed, realised, and characterised in this project. Figure 5.18 shows a schematic structure for the coupled oscillators that can employ up to four RTD devices. To facilitate the biasing and probing process, extra pads were added as shown in the micrograph on Figure 5.19. The double RTD oscillator with spectrum shown in Figure 5.16 (g) which produced 0.593 mW at 312 GHz was used in the coupled oscillator topology. Two of this oscillator circuit (each employs 13 μm long 50 Ω CPW and two 4 μm × 4 μm RTDs) were arranged in a coupled oscillator layout and sharing a single load (spectrum analyser or power metre) as shown in Figure 5.18, forming a single oscillator with four RTD devices and single load. When both biasing were V_{bias1} = 1.34 V (I_{bias1} = 193 mA) and V_{bias2} = 1.48 V (I_{bias2} = 190 mA), maximum power of 1.1 mW was achieved which is almost double the power of the double RTD oscillator (individual oscillator) in Figure 5.16 (g). Figure 5.20 plots the measured

power versus the bias conditions for the double oscillator (with only two RTD devices) and the coupled one (with four RTD devices).

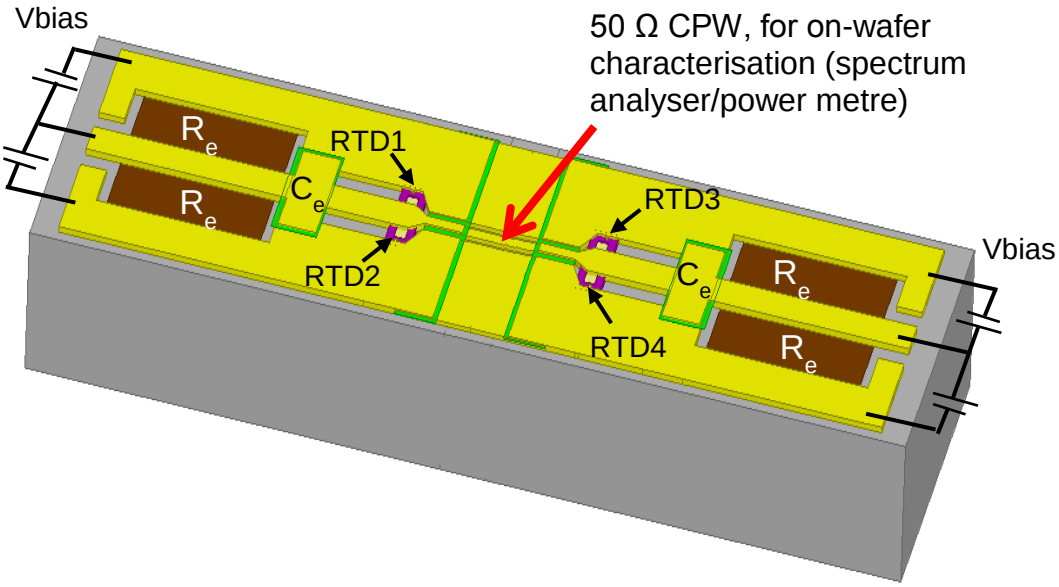


Figure 5.18: *Schematic structure for the coupled RTD oscillators which can employ up to four RTD devices. RF signal is extracted using RF probe landed in the middle of the circuit.*

The single RTD oscillators presented in sub-section 5.4.1 were also used in coupled RTD oscillator topology. Two of the oscillator which employed a single 4 μm × 4 μm RTD device and 18 μm long shorted 50 Ω CPW line, and produced 0.2 mW (-7 dBm) output power at 244 GHz were used and arranged in a coupled oscillator layout as shown in Figure 5.19. The maximum measured output power of the coupled oscillators which include two 4 μm × 4 μm RTD devices in total was 0.374mW (-4.3 dBm) when V_{bias1} = 1.24 V (I_{bias1} = 92 mA) and V_{bias2} = 1.3 V (I_{bias2} = 91 mA). That is, the coupled oscillators produced about 2.7 dB higher power than the single oscillator. Two of the oscillator which employed a single 5 μm × 5 μm RTD device and 9 μm long shorted 50 Ω CPW line, and produced 0.264 mW (-5.8 dBm) output power at 233 GHz were also used and arranged in a

coupled oscillator layout. The maximum measured output power of the coupled oscillators was 0.625 mW (-2 dBm), when V_{bias1} = 1.23 V (I_{bias1} = 107 mA) and V_{bias2} = 1.37 V (I_{bias2} = 110 mA). This power is 3.8 dB higher than that produced by the single 5 µm × 5 µm RTD oscillator. Table 5.7 summaries the measured power results of the different coupled RTD oscillators with the measured power of the individual oscillator used in the coupled layout for comparison. It was noted from the power measurement that the maximum power of the coupled oscillator occurs when $I_{bias1} \approx I_{bias1}$ although V_{bias1} and V_{bias2} are different.

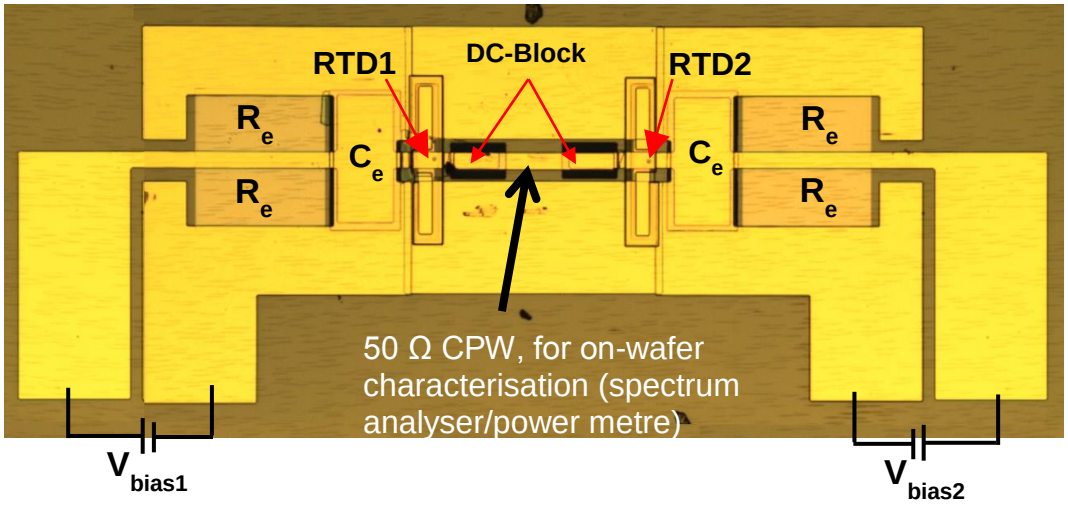


Figure 5.19: *Micrograph of the fabricated coupled RTD oscillators. Two individual oscillators (each with single RTD device) are coupled to deliver higher power where the coupled RF signal is extracted using RF probe landed in the middle of the circuit as indicated. Extra pads were added to facilitate probing and biasing.*

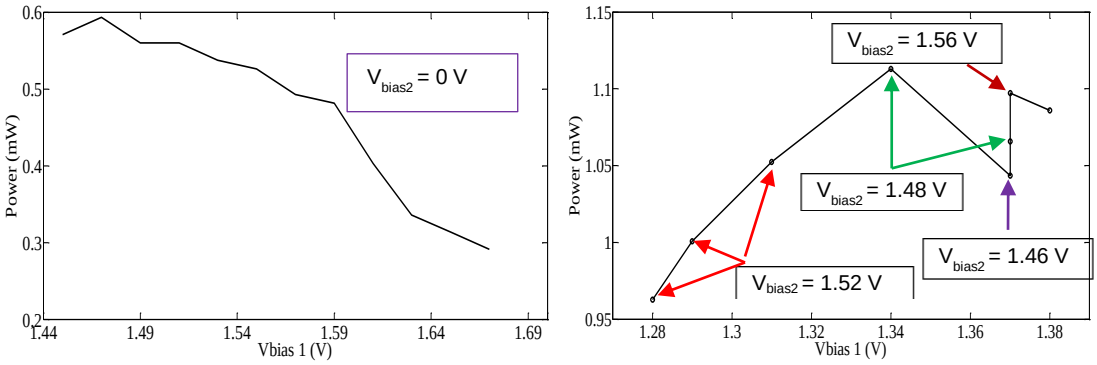


Figure 5.20: *Measured power versus the bias conditions for (a) the double oscillator (with only two RTD devices) and (b) the coupled one (with four RTD devices).*

Table 5.7: *Summary of power measurement results of the different coupled RTD oscillators. The measured power of the individual oscillator used in the coupled layout is also included for comparison.*

	Single RTD Oscillator			***Double RTD Oscillator***		
Device size (μm^2)	***Frequency (GHz)***	***Power from individual oscillator (mW)***	***Power from Coupled oscillator (two Single RTD oscillators) (mW)***	***Frequency (GHz)***	***Power from individual oscillator (mW)***	***Power from Coupled oscillator (two Single RTD oscillators) (mW)***
16	*244*	*0.2*	*0.374*	*312*	*0.593*	*1.11*
25	*233*	*0.264*	*0.625*	-	-	-

5.5 Characterisation of RTD Oscillators using Microstrip Resonating Inductances

As described above, any shorted transmission line can be used as a resonating inductor in the RTD oscillator when the electrical length is less than 90º. Shorted CPW lines were used in the RTD oscillator circuits to realise different oscillation frequencies as described in Section 5.4. It was shown that, for a given inductance value, the lower the characteristic impedance (Z_o) it is, the longer the line

becomes. Different oscillators were realised with shorted CPW lines with Z_o of 50 Ω, 32 Ω, and 25 Ω. However, the geometrical dimensions of the CPW line of lower Z_o become impractical. For example, to construct a 10 Ω CPW line on InP substrate, the required signal line width is w = 66.5 mm with gap dimension s = 2 μm. Therefore, a different transmission line that can provide lower Z_o values but with a geometry which is easy to realise, was proposed and realised in this project. It is a microstrip line which employs polyimide layer (ε_r = 3.5) as a substrate. The polyimide layer is mainly used for RTD device passivation and can be spun in one step for both functions. The polyimide thickness is 1.2 μm and spun on top of ground plane depoistied on the InP substrate. Using the "LineCalc" tool within Agilent's Advanced Design System (ADS) software, it was found that when the signal line width w = 20 μm (the same width of the signal line of the CPW RF pads used in RTD oscillatiors for on-wafer characterisation) and the thickness t = 0.4 μm, this microstrip line has characteristic impedance Z_o = 10.4 Ω. Measurement results of fabricated RTD oscillators employing different RTD device sizes and different lengths of 10.4 Ω shorted polyimide-based microstrip lines to realise the resonating inductance will be described in this section.

5.5.1 Single RTD Oscillator

The RTD oscillator topology that employs one RTD device and resonating inductor realised by shorted polyimide-based microstrip transmission line is shown in Figure 5.21 (a) while Figure 5.21 (b) shows a micrograph of one of the fabricated oscillators. The RTD device is connected to a stabilising resistor R_e (two connected in parallel) to suppress the low frequency bias oscillations and a bypass capacitor C_e which is placed to short-circuit the RF signal to ground and avoid dissipating the RF power over R_e. The capacitor C_e is also used to short the polyimide-based microstrip line.

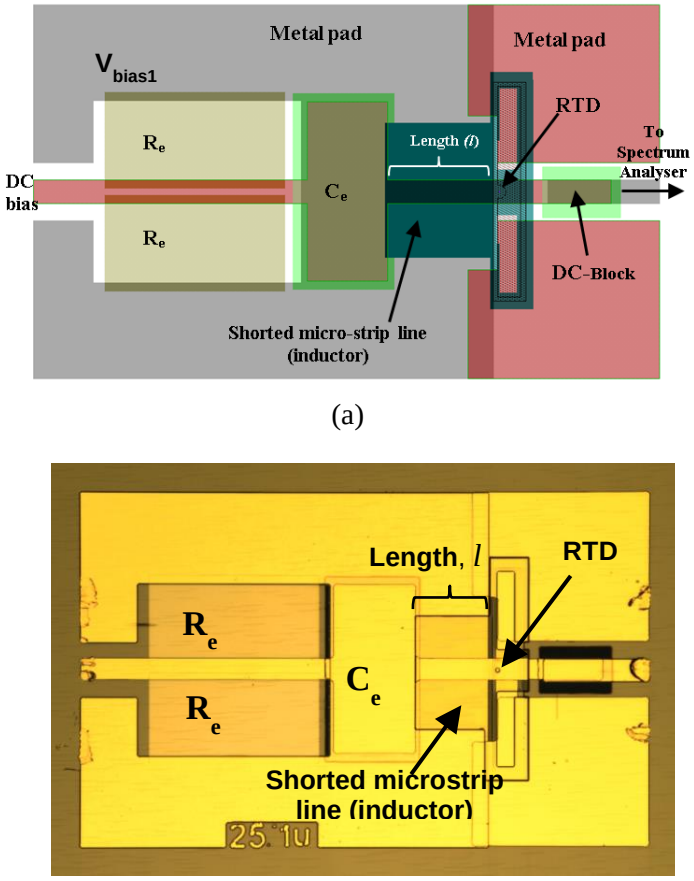


Figure 5.21: *RTD oscillator circuit topology employs one RTD device. Resonating inductance is realised by shorted microstrip transmission line. (a) Circuit layout. (b) Micrograph of a fabricated oscillator.*

Two oscillators with different RTD device size (4 μm × 4 μm and 5 μm × 5 μm) and different lengths of shorted 10.4 Ω microstrip line lengths were fabricated and measured. The setup for frequency detection (spectrum measurement) and power measurement were the same of that described above. When the bias voltage was 1.37 V and the bias current was 90 mA, oscillation frequency of 312 GHz was observed when 88 μm long shorted microstrip line was used in the oscillator circuit that employs one 4 μm × 4 μm RTD device. The measured output power (measured by power meter) was 0.146 mW (-8.4 dBm) after compensating for the

probe and taper insertion losses which is 3.5 dB as per manufacturer specifications. The measured spectrum is shown in Figure 5.22.

For the oscillator that employs one 5 μm × 5 μm RTD device and 65 μm long shorted microstrip line, the measured oscillation frequency was 262 GHz when the bias voltage was 1.41 V and the bias current was 106 mA. The measured output power was 0.186 mW (-7.3 dBm) after compensating for the probe and taper insertion losses which is 3.5 dB as per manufacturer specifications. The measured spectrum is shown in Figure 5.23.

The theoretical calculated frequency of both single oscillators is 250 GHz using Equation 2.27. Thus, the difference between measured and calculated frequency is 62 GHz and 12 GHz in the oscillator that employs 4 μm × 4 μm RTD, and 5 μm × 5 μm RTD, respectively. The discrepancy could be attributed to the reduced parasitic inductance.

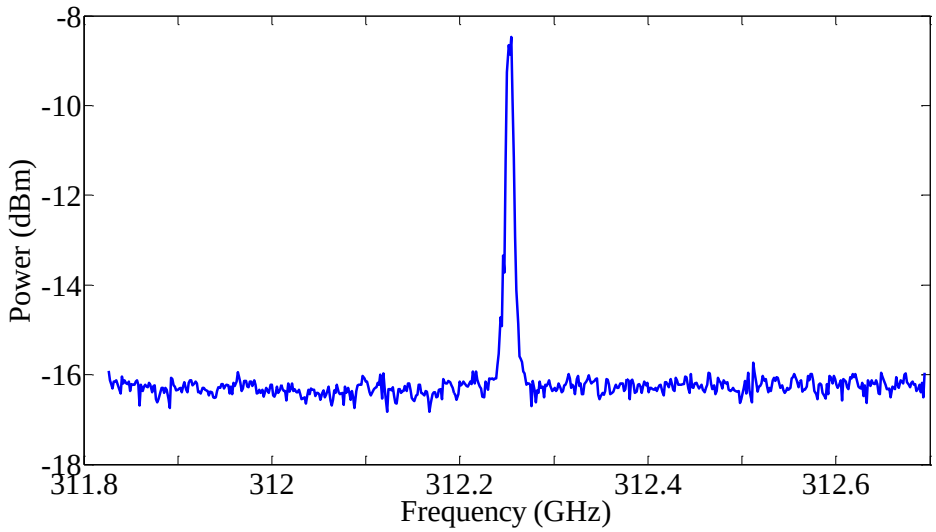


Figure 5.22: *Measured spectrum of the 4 μm × 4 μm RTD oscillator with 88 μm long shorted microstrip line when V_{bias} = 1.37 V and I_{bias} = 90 mA.*

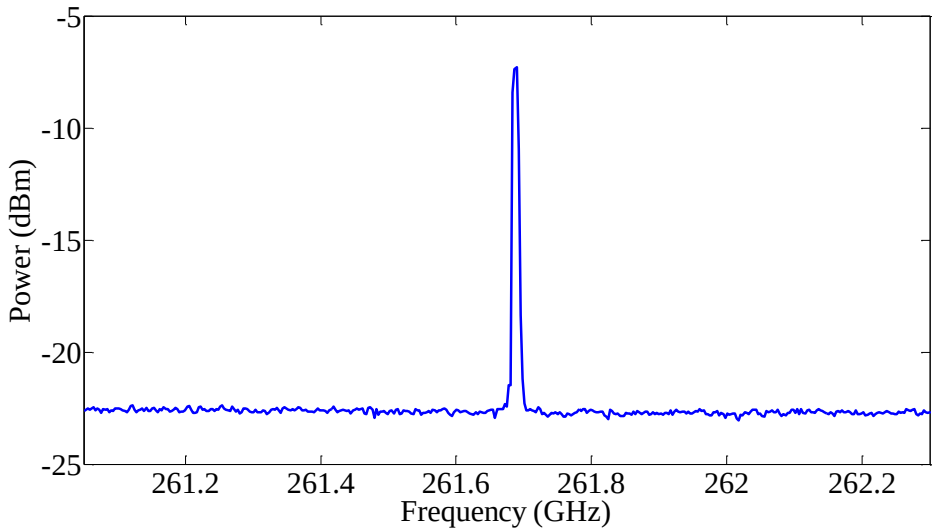


Figure 5.23: *Measured spectrum of the 5 μm × 5 μm RTD oscillator with 65 μm long shorted microstrip line when V_{bias} = 1.41 V and I_{bias} = 106 mA.*

The length *l* of the shorted polyimide-based microstrip line versus frequency f_o is plotted in Figure 5.24. The blue solid line represents the double RTD oscillator employing 4 μm × 4 μm RTD devices with 10.4 Ω shorted polyimide-based microstrip line in which the signal line width is 20 μm. It can be seen that 5 μm long microstrip lines can be used to realise 0.9 THz. If 60 μm wide signal line is used, the calculated Z_o will be 3.8 Ω which means longer lines can be used to realise a given inductance compared to the 10.4 Ω lines. The red dashed line in in Figure 5.24 represents the double RTD oscillator employing 4 μm × 4 μm RTD devices with 3.8 Ω lines. With 5 μm lines, 1.4 THz can be reached compared to the estimated 0.9 THz that can be reached from the oscillator with same RTD devices number and size but with 10.4 Ω line of same length. To further increase the power two double RTD oscillator employing 5 μm × 5 μm RTD devices can be used. The brown line in Figure 5.24 represents this oscillator with 3.8 Ω line. The estimated frequency of this oscillator with 5 μm lines is 1.1 THz, while 1.7 THz can be reached with extremely short 2 μm lines. However, more power can be achieved by employing four RTD devices of same size in coupled oscillator

layout without reduction in the oscillation frequency and without any change in the dimensions of the oscillator's elements.

5.5.2 Coupled RTD Oscillator

Coupled RTD oscillators circuit that combine the power from the two oscillators each employing one 5 µm × 5 µm RTD device and 65 µm long shorted microstrip line was fabricated and characterised in this project. The individual one 5 µm × 5 µm RTD oscillator that produced 0.186 mW (-7.3 dBm) at 262 GHz was employed in the coupled oscillators circuit. Figure 5.25 shows a micrograph of one of the fabricated oscillators. The output power was measured by a power meter and two power supplies were used to bias the two oscillators. It was found that the maximum power was 0.493 mW (-3.1 dBm) when the first oscillator was biased at V_{bias1} = 1.33 V (I_{bias1} = 112 mA) and the second oscillator was biased at V_{bias2} = 1.41 V (I_{bias1} = 110 mA). The measured power is about 2.7 times higher than that obtained from the single oscillator with the same design.

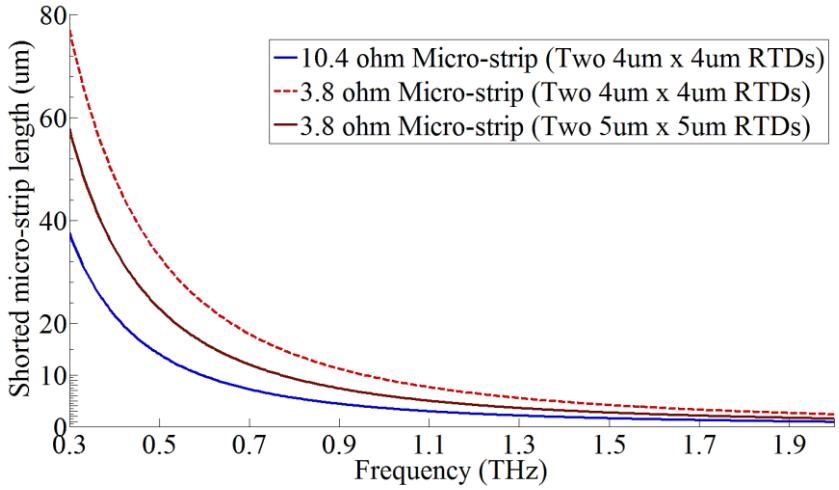


Figure 5.24: *Calculated oscillation frequency of different oscillators employing different RTD device sizes versus shorted microstrip length with different Z_o.*

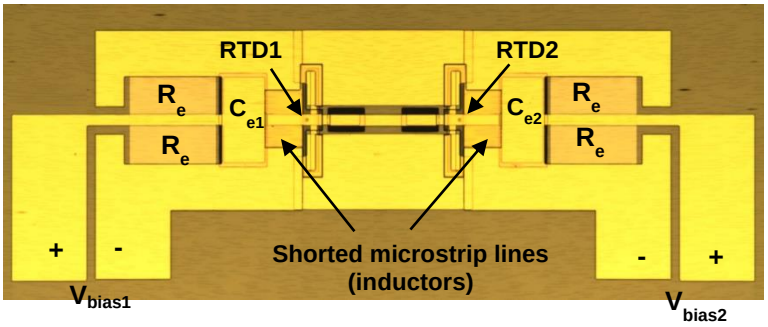


Figure 5.25: *Micrograph of the fabricated coupled RTD oscillators. Each oscillator employs one 5 μm × 5 μm RTD device with 65 μm long shorted microstrip line.*

5.6 Discussion

RTD oscillators with circuit topologies that can employ relatively large size RTD devices (~9 μm^2 to ~25 μm^2) to produce high power and high oscillation frequencies at the same time were described in this chapter. The oscillators were fabricated using photolithography processes and employed different CPW/microstrip structures to realise small inductance values that, with the self-capacitance of the large RTD devices, can reach up to 1.7 THz. A comparison between the oscillators and other published work is discussed here.

Conventional THz RTD oscillators usually use small RTD device sizes (in the sub-micrometre range) in order to reduce RTD self-capacitance and, as a result, realise higher oscillation frequencies [59]. Reducing the RTD device size however leads to lower output power which can be attributed to a number of reasons. One of the reasons is using narrow AlAs barriers (~1 nm) in order to achieve high peak current density (J_P) (> 6 mA/μm^2) and allow for the use submicron device sizes (e.g. 0.33 μm^2 in for 1.31 THz [57] and ~ 0.1 μm^2 for 1.92 THz [28]) with correspondingly small device self-capacitances [28], [57], [59], [60]. However,

such thin barrier thicknesses reduce the peak-to-valley current ratio (PVCR) to less than two (2) through the increased electron transmission probability through the DBQW. Therefore, the peak-to-valley current difference (ΔI) reduces and also the potential output power of an oscillator using such a device reduces. Other issues that may be attributed to high J_P RTDs include reduced thermal stability [59] and the need for ultra-low Ohmic specific contact resistances for the small-sized devices to keep the device contact resistance low [61], since high resistance limits the oscillator output power significantly [31]. The accurate growth of such ultra-thin AlAs barriers is difficulty/challenging which limits the uniformity and so the manufacturability of the devices [62], [63]. Last but not least, small devices in the sub-micrometre range require e-beam lithography which is more costly compared to fabrication of larger devices using photolithography.

In this project, large micro-sized RTD devices were used in the oscillator realisation. These devices have low J_P designs with thicker barrier layers (~1.4 nm). The epitaxial growth requirements are therefore less demanding and more accurate benefiting a reproducible technology. PVCR is also higher (>3), and since for a given specific contact resistance, the larger size RTD devices exhibit low Ohmic contact resistance and do not suffer thermal stability issues, these factors benefit higher output power in oscillator circuits. In addition, they can provide high RF power in oscillator circuits due to the increased ΔI, and can be fabricated using photolithography.

Oscillators topologies in this project allow for accurate on-wafer detection of the oscillation frequency and accurate power measurement. This is an important stage to know the oscillator performance before being integrated with an antenna. With on-wafer characterisation, the generated signal is guided by transmission lines to the measurement equipment; spectrum analyser or power meter for accurate

measurement. This can be considered as a first stage to design a high performance and well characterised RTD oscillator. Once the oscillator has been characterised on-wafer, the next design stage would be the integration of a high performance and well-characterised antenna to couple the generated RF power to the free space. For this configuration, the broadband load which does not influence the oscillation frequency allows for efficient RTD voltage controlled oscillators (VCOs). For an integrated antenna, one with a zero reactance component will be highly desirable in order to maintain the oscillation frequency determined by the first stage. With this design flow, high performance THz source with known radiation pattern would be achievable.

5.7 Summary

This chapter described RTD oscillators that can employ large RTD devices (up to four devices) to deliver high power to a single load with high oscillation frequencies. The high oscillation frequencies are achievable with the low resonating inductances that are realised by shorted CPW/microstrip lines with low characteristic impedance. Maximum power of 1.1 mW was achieved from oscillator that employs four 4 μm × 4 μm devices at ~ 312 GHz. The achieved power is 10% higher than the required power level (i.e. 1 mW at 300 GHz) which was the main target of this project. All oscillators were fabricated using photolithography.

Chapter 6 Antennas for THz RTD-based Oscillators

6.1 Introduction

Once the RTD oscillators have been characterised on-wafer for accurate frequency detection and power measurement, a high performance antenna is required to be integrated with the oscillator circuit and couple the generated THz radiation into free space. An antenna with high gain and directivity is preferable in order to radiate most of the RF power into a specific direction and offer larger distance coverage. Integrating a high performance antenna with a complete characterised oscillator circuit would lead to radiation of all/most of the generated RF power.

This chapter discusses the fundamental parameters used for describing antenna performance with an overview on the High Frequency Structure Simulator (HFSS) simulation software which was used to design and characterise the antennas in this project. It also discusses the challenges encountered when designing antennas on substrates of large dielectric constant materials such as InP and critically reviews a number of reported antennas for RTD-based oscillators in the literature. It also describes a proposed simple antenna configuration which requires simple fabrication and integration with the oscillator circuit. It is a broadband bow-tie slot antenna with a tuning stub which is diced and mounted on a ground plane to improve the antenna performance and radiates to the air-side direction instead of to the substrate side. One port and two port bow-tie antennas

were designed, fabricated and characterised in this project with bandwidth between 200 GHz and 350 GHz.

6.2 Antenna Fundamental Parameters

An antenna is a structure (metallic device) that converts electrical signal into electromagnetic radiation (in transmission mode) or vice versa (in reception more) [95]. It is a transducer between a system (transmitter or receiver) and free space. Antennas are reciprocal devices. That means the properties of an antenna are identical in both transmitting and receiving modes. For instance, if an antenna transmits most of the power in a specific direction, it receives the best through the same direction. The radiation pattern is defined as a graphical representation of the radiation properties of the antenna as a function of angle and position. It can be represented in 2D or 3D to describe the spatial distribution of parameters such as antenna gain or directivity. The radiation intensity in a given direction describes the radiated power per unit solid angle. The antenna overall or realised efficiency represents the ratio of the radiated power to the incident power [96]. The antenna radiation efficiency is the ratio of the radiated power to the accepted power at the antenna input terminal (i.e. radiated power and lost power). Antenna directivity is a term used to describe the antenna capability of focusing/directing the radiated power in a specific direction. Directivity in a given direction is the ratio of the radiation intensity to the radiation intensity of a theoretical reference antenna that radiates isotropically. Antenna gain is defined by multiplying the radiation efficiency and directivity.

6.3 High Frequency Structure Simulator (HFSS)

High Frequency Structure Simulator (HFSS) is the simulation software that used to design and characterise the different antennas in this project [97]. HFSS is

commercial simulation software for electromagnetic structures that can be used to model and design antennas, and other RF electronic components such as filters and transmission lines. HFSS uses Finite Element Method (FEM) by which the full problem domain is segmented into huge number of small regions and represents the field in each sub-region (element). In general, the basic design steps to run a simulation in HFSS include:

1- **Drawing Geometries:** HFSS offers a number of drawing tools that enables the user to draw different geometrical shapes such as boxes, cylinders, etc. The user can also import different layout (e.g. in GDS format) and create different structures based on the dimensions of the imported layout.

2- **Materials Assignment:** The material library in HFSS offers a wide range of common materials that can be assigned to the individual geometries. It also allows the user to define a new material and define its different parameters such as dielectric constant and conductivity.

3- **Boundaries Assignment:** Assigning boundaries is essential and has direct impact on the simulation results. When simulating an antenna, radiation boundary is used to simulate an open problem that allows waves to radiate infinitely far into space and prevent reflections. Usually an air box should be drawn around the antenna geometry and the radiation boundary is assigned to it.

4- **Excitations:** The main two excitation methods that HFSS provides are the wave-port and lumped-port. Wave-port represents the external surface through which a signal enters or exits the geometry. It is effectively a semi-infinite waveguide attached to the model. Lumped-port represents an

internal surface through which a signal enters or exits the device. Wave-ports are very useful for exciting different transmission lines such as microstrip, coaxial, coplanar waveguide. The results of wave-ports can be de-embedded while those of the limped-ports cannot. In this project wave-ports were employed to excite the antennas.

5- **Analysis Setup and Adaptive Meshing:** The user has to specify the solution frequency and the frequency sweep range over which the problem will be solved. HFSS will generate the mesh based on the specified solution frequency. One of the key features of HFSS is the automated adaptive mesh refinement technique which generates an accurate solution. HFSS applies a meshing refinement algorithm where it iteratively adds mesh elements in regions where a finer mesh is needed due to the localized electromagnetic field behaviour.

6.4 Reported Antennas for RTD-based Oscillators: Challenges and Solutions

6.4.1 Challenges

Antennas fabricated on large dielectric constant (ε_r) substrates tend to radiate most of their energy into and through the substrate [73]. For example, an infinitesimal planar dipole radiates approximately $\varepsilon_r^{3/2}$ more power into the substrate than into free space. For InP (ε_r = 12.56) this ratio is around 45. In addition, any radiation into the substrate at angles greater than the critical angle ($\theta_c = \sin^{-1}(\varepsilon r^{-1/2})$) is totally internally reflected at the top and bottom surfaces and leading to confinement of the energy inside the substrate as illustrated in Figure 6.1. For InP the critical angle is around 16.4º. This confined radiation propagates inside the substrate without getting radiated unless a discontinuity appears at the edges

leading to degradation in the radiation pattern and in antenna performance in general. To investigate these issues more, an antenna (bow-tie) placed on relatively large size InP substrate was simulated using HFSS simulation software to visualise the confined energy inside the substrate and the radiation pattern. Results will be presented in following sub-sections.

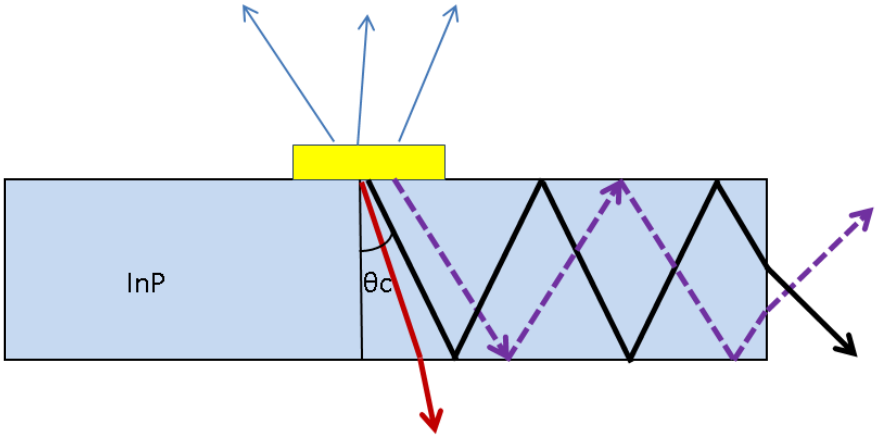


Figure 6.1: *Illustration of the critical angle and its effects. Only radiation from one half of the substrate is shown for simplicity.*

6.4.2 RTD-Slot Antenna Oscillators

RTD oscillators employing integrated slot antennas have been commonly used where the antenna performs as radiator and resonator element at the same time [27], [28], [52]–[57], [74]. Figure 6.2 shows the schematic structure for the RTD-slot antenna integration.

Because the majority of the output power generated from this RTD-slot antenna oscillators radiate towards the substrate (InP) direction, a number of proposed solutions have been reported to overcome the substrate effects and extract the radiation from the RTD-slot antenna as will be discussed here.

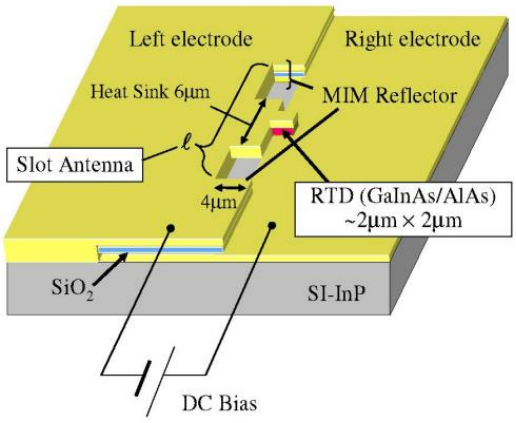


Figure 6.2: *Schematic structure of the RTD oscillator integrated with slot antenna which acts as resonator and radiator* [54].

- **Hemispherical Lens for Backside Radiation:**

  The common solution has been to use a hemispherical lens on the backside to collect the power from the bottom side of the substrate [64], [71], [74]. Figure 6.3 shows an example of a hemispherical lens with RTD-slot antenna oscillator which is placed on the top of the lens [74]. The figure also shows the radiation pattern. It can be seen that radiation is collimated with half power beam width of ~ 6º. This narrow beam width is advantageous for applications that require point-to-point link. However, the RF power reduces because of the reflection loss at surface of the lens due to the high refractive index of the lens [74].

- **Tapered Slot (Vivaldi) Emitter for Horizontal Radiation:**

  Instead of using the bulky lens, slot-antenna resonator integrated with planar tapered slot (Vivaldi) antenna on a dielectric membrane was proposed to extract the radiation [60]. In this configuration, the signal radiates in the plane of the membrane which bears the emitting antenna and the resonator as shown in Figure 6.4.

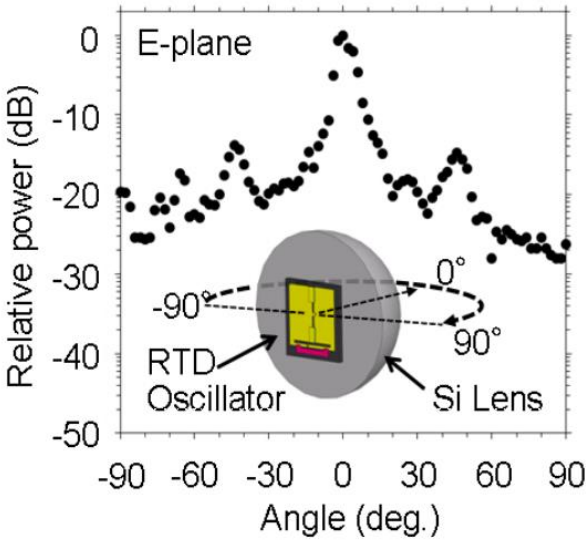


Figure 6.3: *Schematic structure of hemispherical lens used to extract the radiation from the RTD-slot antenna oscillator with the corresponding radiation pattern* [74].

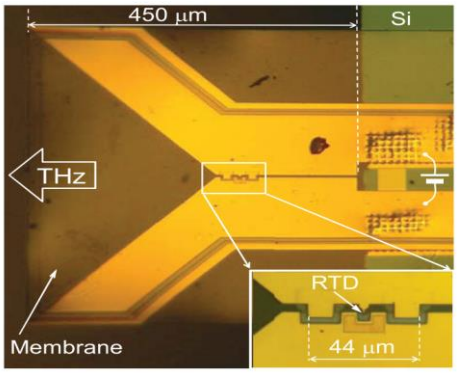


Figure 6.4: *Schematic structure of the RTD-slot antenna oscillator with tapered slot antenna. The radiation is emitted in the plane of the membrane* [60].

- **Patch Antenna on BCB for Upward Radiation**

  Since radiation perpendicular to the substrate would be more desirable, a technique of using patch antenna placed on top of 7 µm thick benzocyclobutene (BCB) layer which is stacked on an RTD-slot antenna

oscillator was reported for upward radiation without the need of lens as shown in Figure 6.5 [75]. With this configuration, a ratio of 4:1 between the power in the upward and substrate direction was reported.

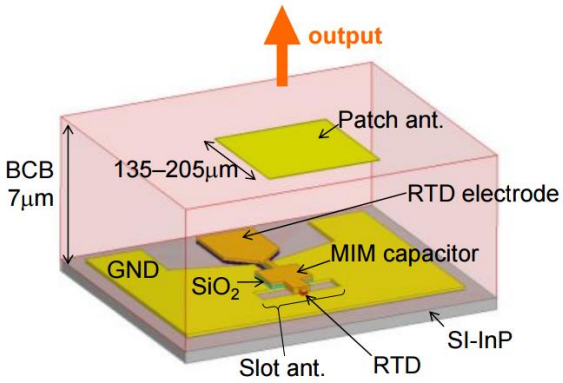


Figure 6.5: *Schematic structure of the RTD-slot antenna oscillator with patch antenna for upwards radiation* [75].

Despite the efforts to extract the radiation from the RTD-slot antenna oscillators, the slot antenna has its own design considerations. The impedance of a slot antenna is infinity at the centre of the slot and zero at the thin edges. Thus, when the RTD device is located at the centre of the slot, the power will be extremely low due to the severe impedance mismatch. Therefore, reported work have shown relative increase in the power when the RTD was placed at different location (shifted from the centre) to improve the impedance matching [54], [56], [58]. Since the slot antenna length is relatively short, and further reduces with increasing frequency, a large RTD device would limit the impedance matching. For example, at 1.92 THz, a 12 μm long slot antenna was used [28]. This length is comparable to, for example, 4 μm^2 RTD device dimension. Thus, RTD devices with areas less than 1 μm^2 are usually employed at higher oscillation frequencies. Furthermore, in order to increase the oscillation frequencies, reduction in the slot antenna inductance and/or the RTD self-capacitance is required. Reducing the RTD-self capacitance is usually more convenient and done through the RTD mesa size. As such, smaller RTD device sizes (in the sub-micrometre range) are usually

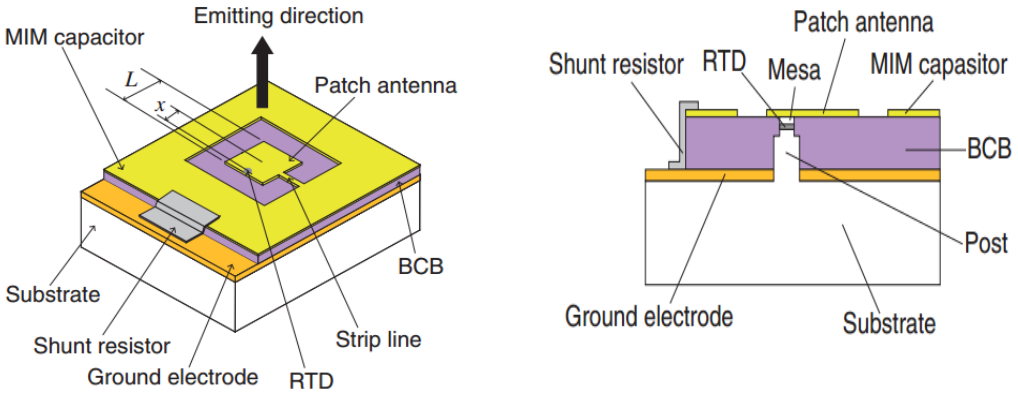
used to realise higher oscillation frequencies. Generally speaking, the slot antenna is narrowband and requires small RTD devices which could suffer thermal stability issues as was discussed in Chapter 5.

6.4.3 RTD Oscillators with Integrated Patch Antenna on BCB Substrate

RTD oscillators integrated with patch antennas, where the antenna performs as radiator and resonator element at the same time, have been reported [98], [99]. Figure 6.6 shows the schematic structure for the RTD-patch antenna integration. In this structure, the RTD post is buried within a layer of BCB and is sandwiched between the patch and the ground plane on top of an InP substrate, so emitting output power into the air side with the aid of the antenna's ground plane. In contrast to the RTD-slot antenna oscillator, this oscillator does not require additional component to extract the power. The oscillation frequency is determined by the resonant length l of the patch and the input resistance (for impedance matching with the RTD) can be tuned by locating the RTD post at a distance x away from the centre of the patch.

The performance of the patch antenna largely depends on the thickness of the BCB layer and the operating frequency. The efficiency and gain can be increased by using thicker BCB layer. However, this means thicker RTD mesa has to be used as well because the top and bottom RTD electrodes are connected to the patch and the ground plane, respectively, as illustrated in Figure 6.6 (b). There is a trade-off between the size and the thickness of the RTD mesa where thick mesa with small area (to realise higher oscillation frequencies) leads to non-negligible self-inductance (L_m) and series resistance [98], [99].

The effects of the BCB layer on the performance of the patch antenna were investigated in this project. Two patch antennas were designed and simulated in HFSS simulation software with two different designed frequencies; 180 GHz (relatively low) and 1 THz (relatively high). Details are given in Section 6.5.



(a) (b)

Figure 6.6: *Schematic structure of the RTD oscillator integrated with patch antenna which acts as resonator and radiator. The patch antenna is placed on grounded BCB layer and radiates to the air side. (a) Perspective view. (b) Cross-sectional view* [99].

6.4.3.1 RTD Oscillator with On-chip Patch Antenna

Instead of using integrated antenna with the RTD device to act as resonator and radiator element simultaneously, an on-chip patch antenna used as a radiation element only has been reported [26]. Figure 6.7 shows the circuit schematic diagram. Three identical RTD sub-oscillators were integrated with a single on-chip patch antenna. Each sub-oscillator contains one RTD and coplanar waveguide (CPW) transmission line to realise the resonating inductance. The patch antenna radiates the signal generated from the three RTD sub-oscillators. However, few details on the configuration and the performance of the antenna itself were given in the paper.

If the patch antenna was fabricated on large dielectric constant substrate (such as InP substrate with ε_r =12.56), then the antenna performance will be degraded [100]. To enhance the performance of the patch antenna on such large dielectric constant, different techniques have been proposed. Micromachining techniques including creating a cavity underneath the patch antenna [101], and elevated patch antenna [100] are common proposed techniques in which the effect of the large dielectric constant substrate is reduced. However, these techniques require additional fabrication steps though, and the bandwidth is still narrow.

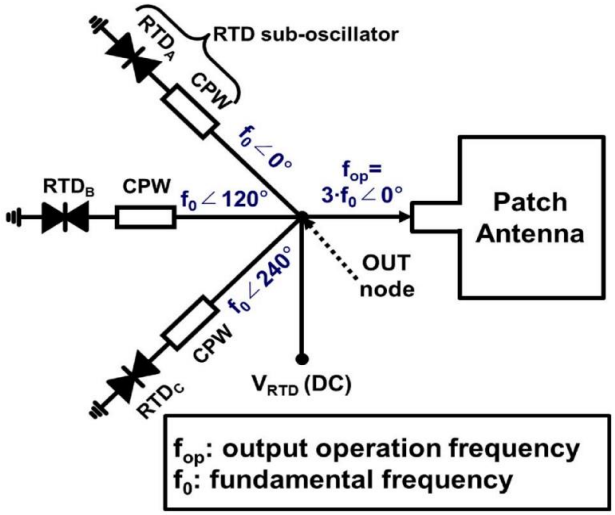


Figure 6.7: Circuit schematic diagram of the RTD oscillator integrated with an on-chip patch antenna [26].

6.5 Simulation of Patch Antennas on BCB Substrate

A microstrip patch antenna is one of the most commonly used planar antennas. It consists of a metal element mounted on a ground plane through a dielectric substrate [102]. Different shapes of metal for the patch such as circular and rectangular can be used. Rectangular patch is the most common due to the

simplicity of the design. Figure 6.8 shows the geometry of the rectangular patch antenna. To design a microstrip patch antenna, the following equations are used to determine the dimensions values of the patch (*W* and *L*) [95]

$$W = \frac{c_0}{2f_r}\sqrt{\frac{2}{\varepsilon_r + 1}} \tag{6.1}$$

where, c_0 is the speed of light, ε_r is the dielectric constant, and f_r is the designed frequency. The value of *L* can be calculated by

$$L = \frac{c_0}{2f_r\sqrt{\varepsilon_{reff}}} - 2\Delta L \tag{6.2}$$

where

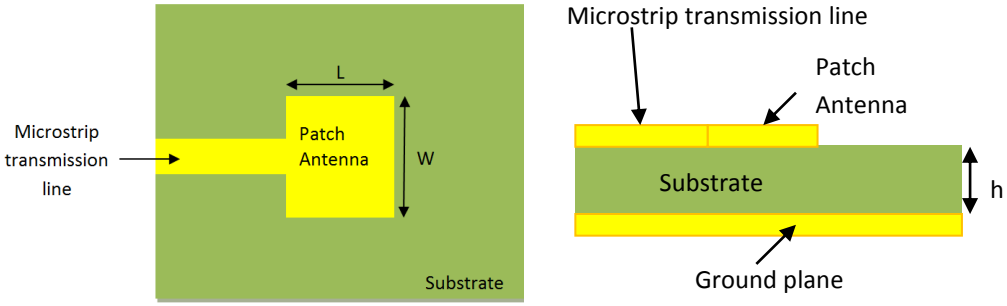
$$\varepsilon_{reff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right]^{-1/2} \tag{6.3}$$

and

$$\Delta L = 0.412\frac{h(\varepsilon_{reff} + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\varepsilon_{reff} - 0.258)\left(\frac{W}{h} + 0.8\right)} \tag{6.4}$$

As was described in sub-section 6.4.3, the thickness of the BCB layer (substrate) affects the performance of the patch antenna. Thicker BCB would improve the antenna gain and efficiency. However, thicker BCB layer means thicker RTD mesa because the top and bottom electrodes of the RTD device are connected to the patch and the ground plane, respectively, which is not preferable. The

optimum required BCB thickness that gives acceptable performance was investigated in this project using HFSS simulation software.



(a) (b)

Figure 6.8: *Rectangular patch antenna geometry. (a) Top view. (b) Cross-sectional view.*

The substrate material is BCB, which has a dielectric constant of 2.7. A series of simulations were carried out using HFSS to investigate the substrate effects on the antenna performance. Different thicknesses of BCB, ranging from 5 µm to 60 µm, were used. The operating frequency of all initial runs was 180 GHz. Following the design procedure explained above, and due to different substrate thicknesses, each antenna has its unique length and width. Figure 6.9 shows the simulated return loss (S_{11}) of the antenna designed on 5 µm thick BCB substrate. The antenna resonance is 177.4 GHz which means 1.4 % deviation from the designed frequency.

Figure 6.10 shows the antenna gain versus the BCB thickness while Figure 6.11 shows the antenna efficiency. It can be seen from Figure 6.10 that the antenna gain increases as the BCB thickness increases. Sharp increase was achieved in the gain (from 0.6 dB to 6.9 dB) when the thickness increases from 5 µm to 20 µm. However, small increase (less than 1 dB) was observed when the thickness further increases from around 20 µm to 60 µm. The antenna radiation efficiency (in

Figure 6.11) also increases with the increase in the substrate thickness. A large enhancement in the efficiency (from 19 % to 75 %) was achieved when the BCB substrate thickness increases from 5 µm to 20 µm. Efficiency of ~ 90 % was achieved for 40 µm to 60 µm thick BCB. Therefore, the 5 µm BCB is not an optimum thickness for the patch at this frequency. The 10 µm BCB would provide an acceptable performance (~ 5 dB gain and ~ 50 % efficiency). However, this means 10 µm thick RTD mesa is required with potential increase in the self-inductance and series resistance.

The patch antenna was also designed and simulated at much higher frequency; 1 THz. It was found that gain of ~ 5.8 dB and ~ 50 % radiation efficiency were achieved when 5 µm thick BCB was used.

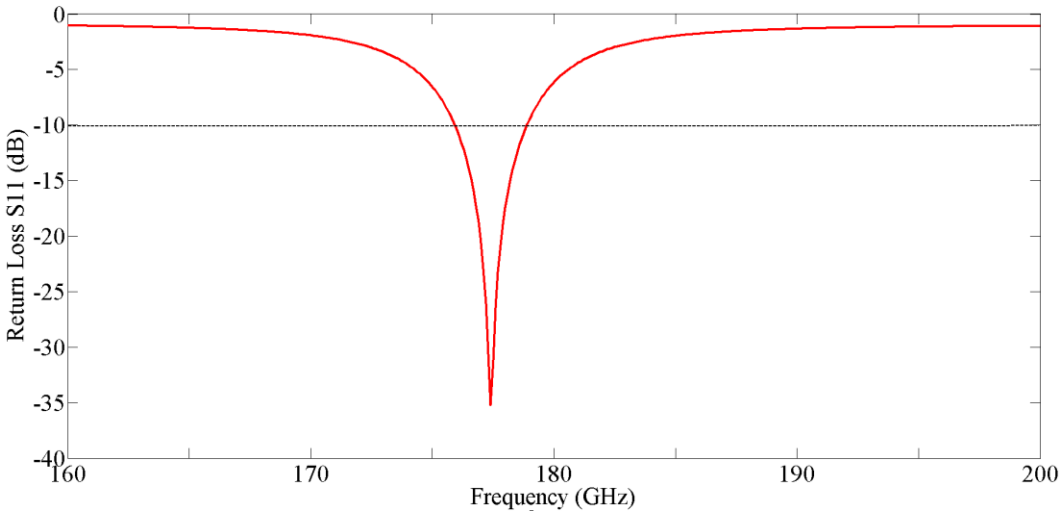


Figure 6.9: *Simulated return loss of the patch antenna designed at 180 GHz on5 µm thick BCB substrate. The antenna resonance is at 177.4 GHz which means 1.4 % deviation from the designed frequency.*

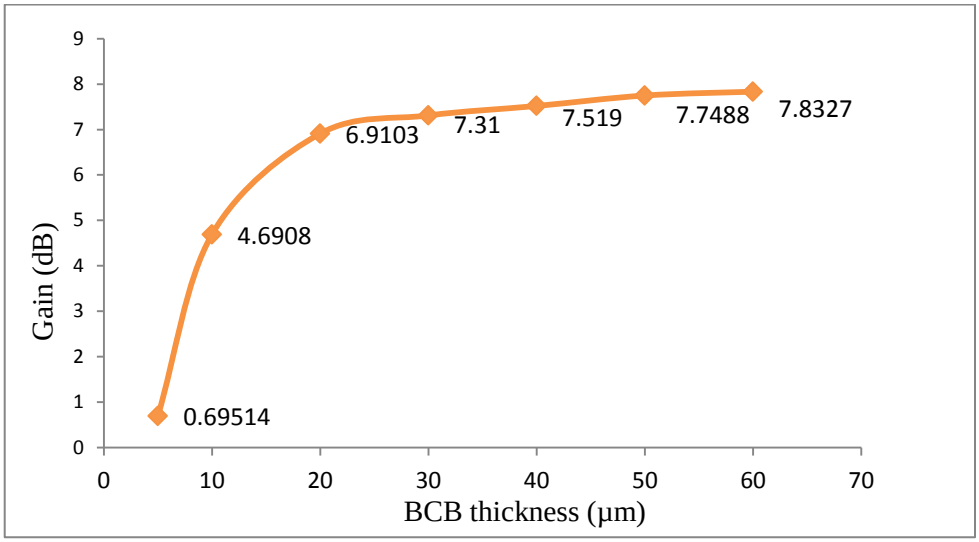


Figure 6.10: *Simulated antenna gain of the patch antenna as a function of the BCB substrate thickness. All designs were for 180 GHz.*

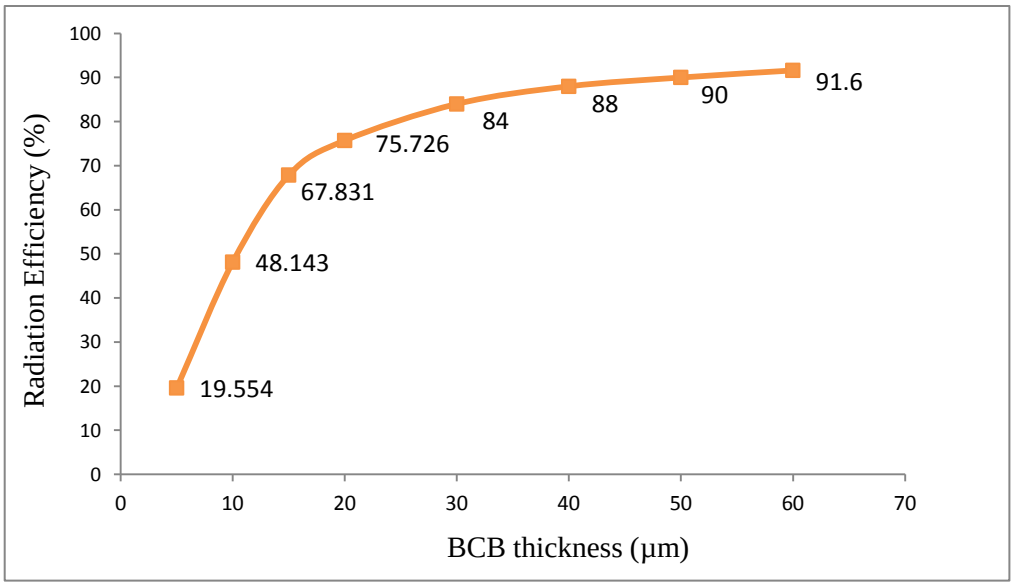


Figure 6.11*: Simulated antenna radiation efficiency of the patch antenna as a function of the BCB substrate thickness. All designs were for 180 GHz.*

6.6 Novel Bow-tie Antenna Realisation

From previous section, it can be concluded that broadband antenna that can also be easily integrated with large devices (for higher power) and realise high oscillation frequencies at the same time is more desirable. In this project, a bow-tie slot antenna with a tuning stub was designed, simulated, fabricated, and characterised with the aim of obtaining an antenna that has wide bandwidth, radiates to the air-side instead of to the substrate, and is suitable for integration with the oscillators presented in this project. To supress the effects of the large dielectric constant substrate the antenna was diced and mounted on a ground plane. Here, the large dielectric constant substrate around the antenna conductor is removed. The ground plane underneath the diced substrate acts as a reflector and, ultimately, the antenna radiates to air-side direction without employing additional component. More details are given next.

6.6.1 Antenna Design

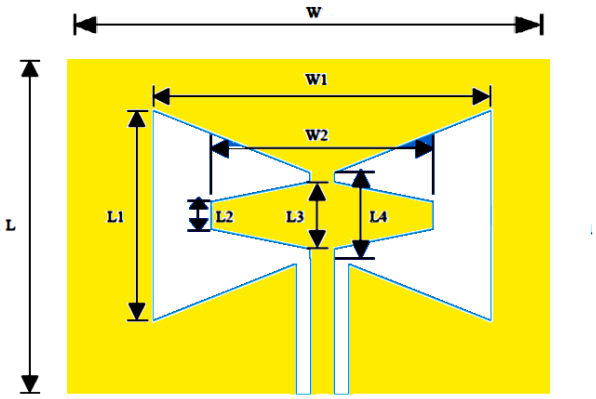


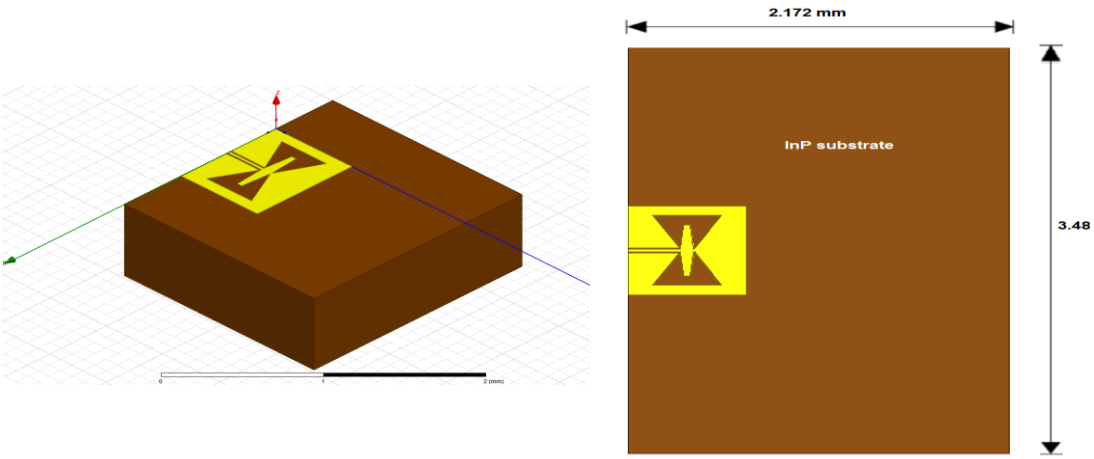
Figure 6.12: *The geometry of the proposed bow-tie antenna* [103].

A bow-tie antenna is a simple version of planar slot antennas which can offer large bandwidth. A simple CPW-fed bow-tie antenna with tuning stub for

increased bandwidth adopted in this work was proposed in [103]. Figure 6.12 shows the geometry of the antenna design. The stubs increase the input resistance, which results in better matching. Moreover, it shifts the main resonance to a lower frequency and creates a new resonance at a higher frequency. For a desired bandwidth, the antenna dimensions are calculated as a function of the free space wavelengths at the lower frequency (λ_L) and the higher frequency (λ_H), where $W_1 = 0.77\lambda_H$, $W_2 = 0.40\lambda_L$, $L_1 = 0.33\lambda_L$, $L_2 = 0.03\lambda_L$, $L_3 = 0.09\lambda_H$, $L_4 = 0.10\lambda_H$, $W = 1.3\times W_1$ and $L = 1.12\times L_1$. In this project the antenna was designed for bandwidth between 200 GHz and 350 GHz with the following antenna dimensions: $W_1 = 660$ µm, $W_2 = 600$ µm, $L_1 = 495$ µm, $L_2 = 45$ µm, $L_3 = 77$ µm, $L_4 = 96$ µm, $W = 840$ µm, and $L = 556.5$ µm. The CPW line with signal line width of 20 µm and gap of 13.8 µm to each of the two ground planes were calculated to give 50 Ω characteristic impedance. The metallisation was made of 0.4 µm thick gold and patterned on the top of the InP substrate. The antenna was simulated in HFSS with different sizes of the InP substrate to investigate the radiation pattern and the issues of the confined energy.

6.6.2 Bow-tie Antenna on Large Size InP Substrate

As discussed in sub-section 6.4.1, for InP ($\varepsilon_r = 12.56$) the critical angle is around 16.4º. Therefore, any radiation into the substrate at angles greater than this angle will be confined inside the substrate. To visualise this trapped energy, the bow-tie antenna was simulated on large area InP substrate compared to the bow-tie antenna area using HFSS simulator. Figure 6.13 shows an illustration of the bow-tie antenna on a large area InP substrate. Figure 6.14 and Figure 6.15 show the electric and magnetic fields inside the substrate, respectively. These trapped fields confirm the inevitable degradation of the antenna performance when it is fabricated on a large area substrate of large dielectric constant.



(a) (b)

Figure 6.13: *Antenna geometry on relatively big size substrate used to visualise the fields inside the substrate. (a) 3D view. (b) Top view (xy-plane) showing the InP substrate outer dimensions.*

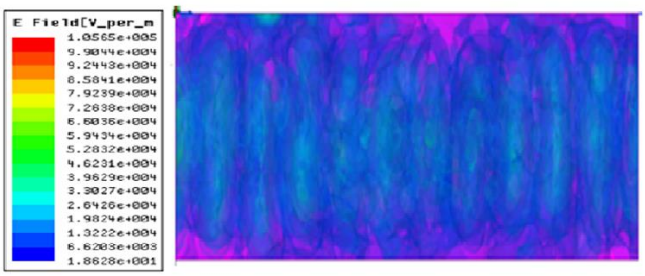


Figure 6.14*: E-field inside the large size substrate (side view, yz-plane).*

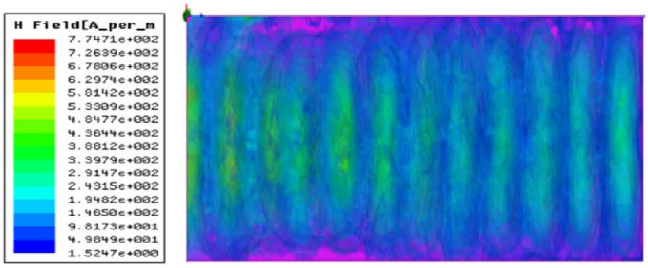


Figure 6.15: *H-field inside the large size substrate (side view, yz-plane).*

The radiation pattern of the antenna configuration shown in Figure 6.13 was plotted and shown in Figure 6.16. It can be seen that the radiation pattern is unpredictable with no clear lobe to indicate the antenna directivity.

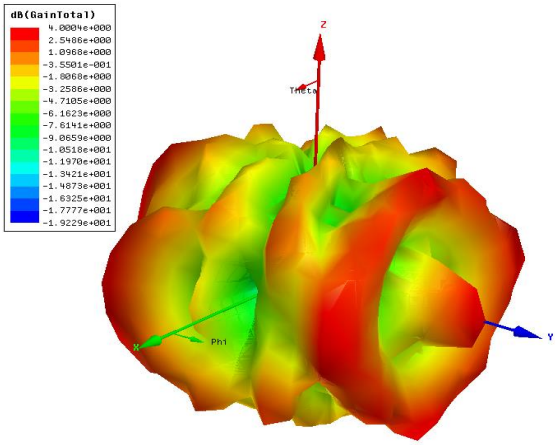


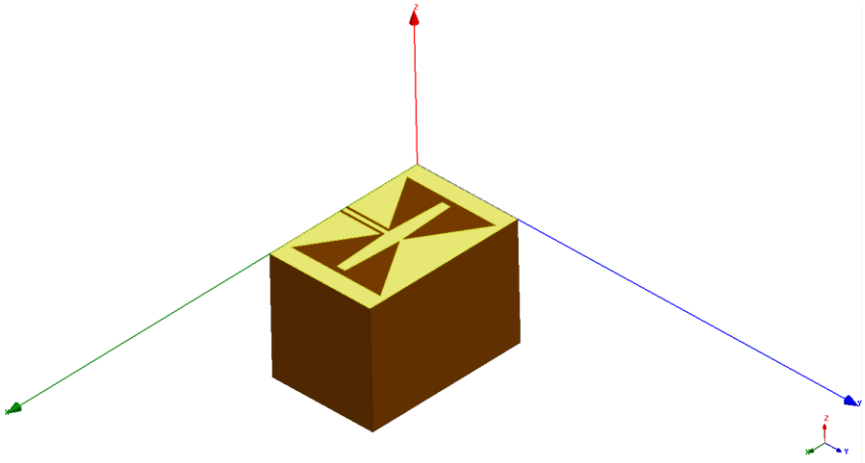
Figure 6.16: *Radiation pattern of the bow-tie slot antenna placed on large area InP substrate (Figure 6.13) at 280 GHz. Degradation in the radiation pattern is clear.*

6.6.3 Proposed Design: Diced and Grounded Antenna

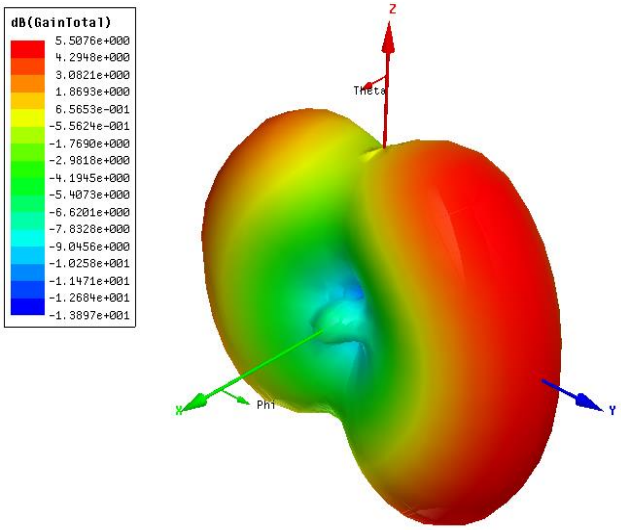
As discussed above, the large size InP substrate has large impact on the antenna performance. Instead of employing the solutions discussed above (e.g. employing bulky hemispherical lenses), the effects of the substrate could be alleviated (and the antenna performance improves) by the following hypothesis:

1- If the substrate material around the antenna conductors was removed (i.e. shrinking the size of the substrate to be the same as the outer dimension of the antenna), then the amount of the confined energy would be less due to the presence of air surrounding the antenna. In addition, the path of confined radiation (zigzag path) will be shorter which means lower decay to the signal. This step was investigated in HFSS simulator where the substrate around the antenna in Figure 6.13 was removed as shown in

Figure 6.17 (a). The simulated radiation pattern is shown in Figure 6.17 (b). Compared to the radiation pattern in Figure 6.16, there is improvement in the pattern due to the use of diced substrate.



(a)



(b)

Figure 6.17: *(a) Diced antenna geometry used in HFSS simulation to alleviate the effects of the large dielectric constant substrate. (b) Simulated radiation pattern.*

2- If the diced antenna in step 1 was then placed on a big size reflector ground plane, the radiation pattern would be enhanced by re-directing any radiation into the substrate side into air-side perpendicular to the reflector ground plane. Figure 6.18 illustrates these two steps and shows an example for potential radiations from this proposed diced and grounded configuration.

Simulation results of the proposed antenna configuration indicated air-side radiation and wide bandwidth, and so the antenna was fabricated and experimentally characterised. Details will be discussed next.

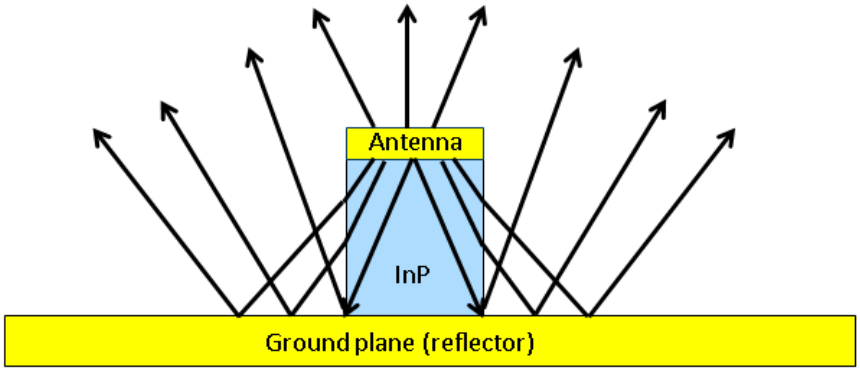


Figure 6.18: *Illustration of the proposed diced bow-tie antenna placed on reflector ground plane and potential radiation. The InP material is removed around the antenna which leads to less confined radiation. The ground plane reflects the radiation to the air-side.*

6.6.4 Antenna Fabrication

The bow-tie antenna with a tuning stub was designed using L-Edit software. An array that includes large number of this antenna was designed as shown in Figure 6.19. The gap between each neighbouring antennas was 100 µm to facilitate the cleaving (dicing) process which was carried out by Optocap Ltd.

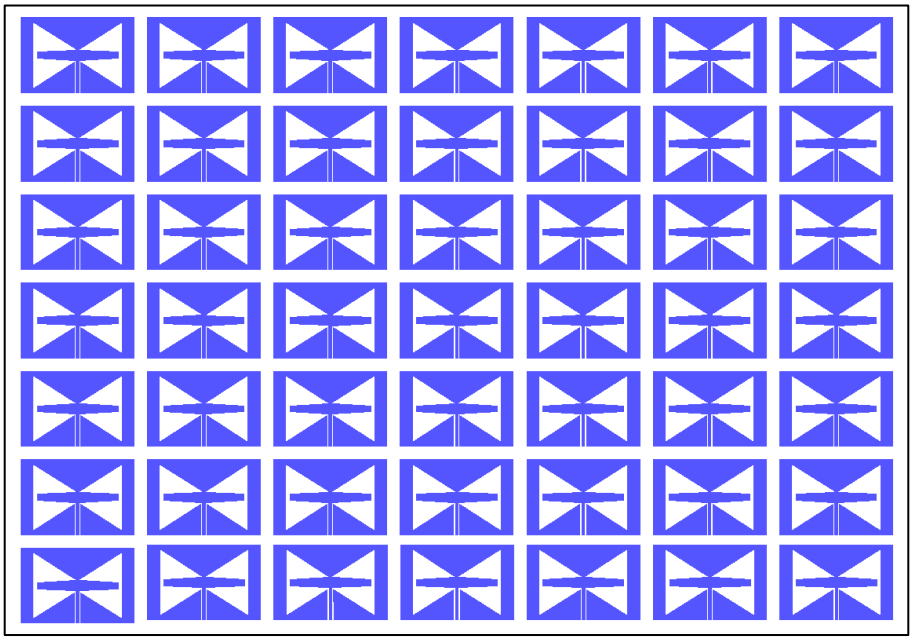


Figure 6.19: *Layout design of the bow-tie antenna in L-Edit with 100 µm gap between adjacent antennas to facilitate the dicing process.*

The bow-tie antenna with a tuning stub was then fabricated using electron beam (e-beam) lithography process. A bi-layer e-beam resist system using polymethyl methacrylate (PMMA) was used to form a suitable undercut to facilitate the lift-off process. The first 15% PMMA 2010 layer was spun at 5000 rpm on 600 µm thick InP substrate which was then baked at 143°C for two minutes. The thickness of the first layer was around 1200 nm. A second layer of 4% PMMA 2041 was then spun at 5000 rpm and baked at 143°C for two minutes. The thickness of the second (top) PMMA layer was 100 nm. The spun PMMA layers were then exposed by e-beam pattern writing using Vestec VB6 beam writer. The exposed PMMA was then developed in a 1:1 mixture of methyl isobutyl ketone (MIBK) and isopropyl alcohol (IPA). Since the lower layer is more sensitive to the e-beam dose than the top layer, an undercut profile will be formed. Finally, Ti/Au (20nm/400nm) metal scheme was deposited using an electron beam evaporator

followed by lift-off in acetone. The antenna was then diced and mounted on big size reflector ground plane. Figure 6.20 shows a picture of the fabricated antenna.

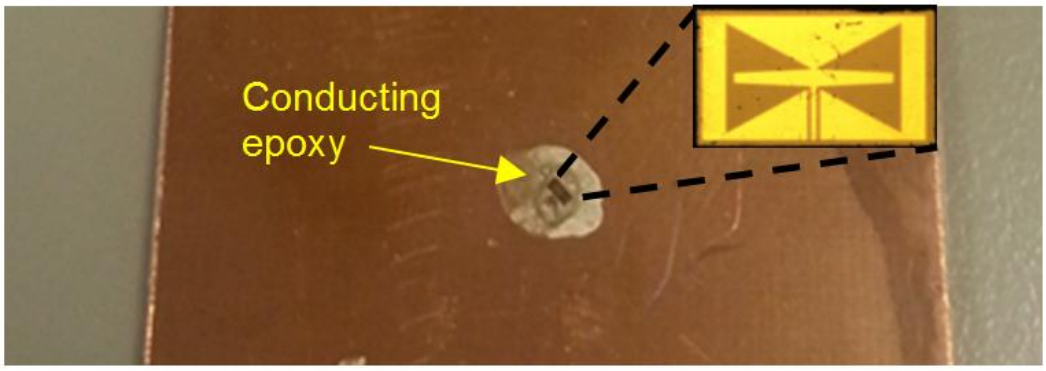


Figure 6.20: *Fabricated diced antenna placed on reflector ground plane.*

6.6.5 Antenna Return Loss and Equivalent Inductance

The return loss of the fabricated antenna shown in Figure 6.20 was measured using a J-band (220 GHz - 325 GHz) Cascade Microtech millimeter wave vector network analyser (VNA) with G-S-G infinity probes. The VNA was calibrated for 1-port S-parameter measurements using the short-open-load (SOL) one port calibration process on a Cascade impedance substrate. Figure 6.21 shows the measured and simulated return loss of the designed antenna with a 50 Ω characteristic impedance CPW feed line. The bandwidth (defined by return loss of less than -10 dB) is around 100 GHz and extends almost the entire frequency band from 220-325 GHz. The discrepancy between the measured and simulated results can be attributed to unwanted signal reflections from surrounding objects during measurements. However, since not all the accepted power will be radiated, radiation efficiency was investigated and results will be given in the next sub-section.

The simulated real part of the antenna impedance is plotted in Figure 6.22, while the simulated reactance part of the antenna is plotted in Figure 6.23 (a). The reactance part of the antenna is inductive across the frequency range from 220-310 GHz and the equivalent inductances are plotted in Figure 6.23 (b). It is zero at around 308 GHz making it suitable for integration with the oscillators developed in this project. At other frequencies, the antenna reactance is much higher than that of the resonating inductance and no significant modification in the oscillation frequency is expected. More details will be given in Section 6.7.

According to Equation 2.25, the maximum power delivered to the load (antenna here) is when $G_L = \frac{G_n}{2}$. In case of an antenna was used, $G_L = G_{ant.} = 1/R_{ant.}$. If $G_{ant.}$ was large (i.e. small R_L), G_n need to be large as will. Therefore, larger RTD device size can be employed according to Equation 2.9 and higher power would be achieved/radiated if the antenna performance was maintained. For this perspective, the return loss was simulated for the antenna fed by 30 Ω CPW line. Figure 6.24 compares the simulated return loss of the antenna when fed by 50 Ω and 30 Ω CPW lines. The bandwidths of the two antennas are comparable and almost extend the entire J-band. Therefore, the feed line can be chosen according to the RTD device negative differential conductance to improve the impedance matching and so deliver higher power.

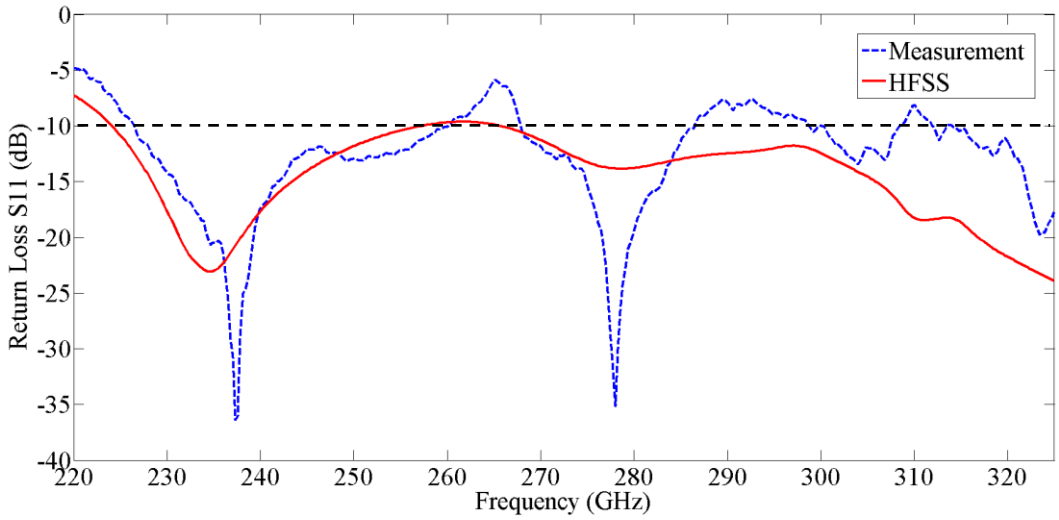


Figure 6.21: *Simulated and measured return loss of the bow-tie antenna with 50 Ω CPW feed line. The antenna demonstrates broadband performance across the entire J-band.*

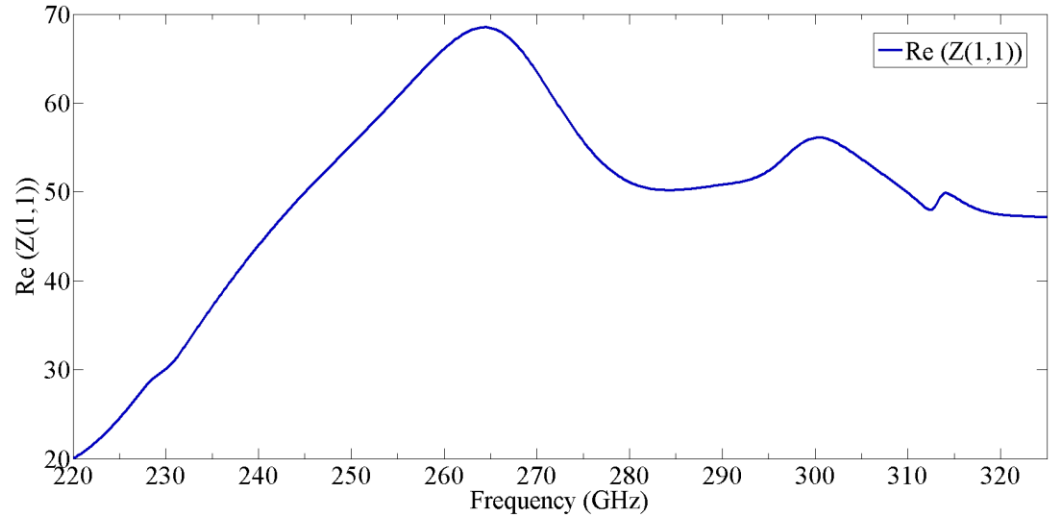
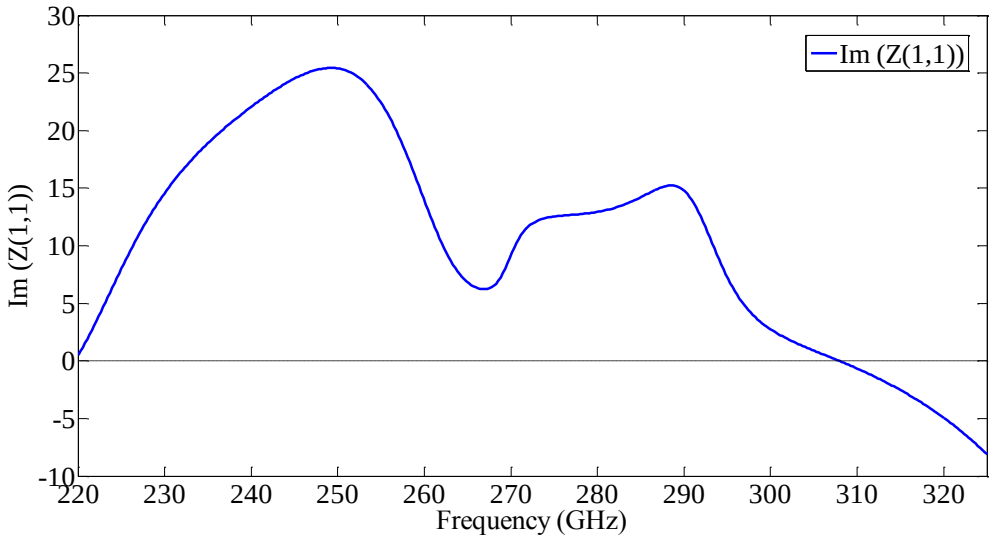
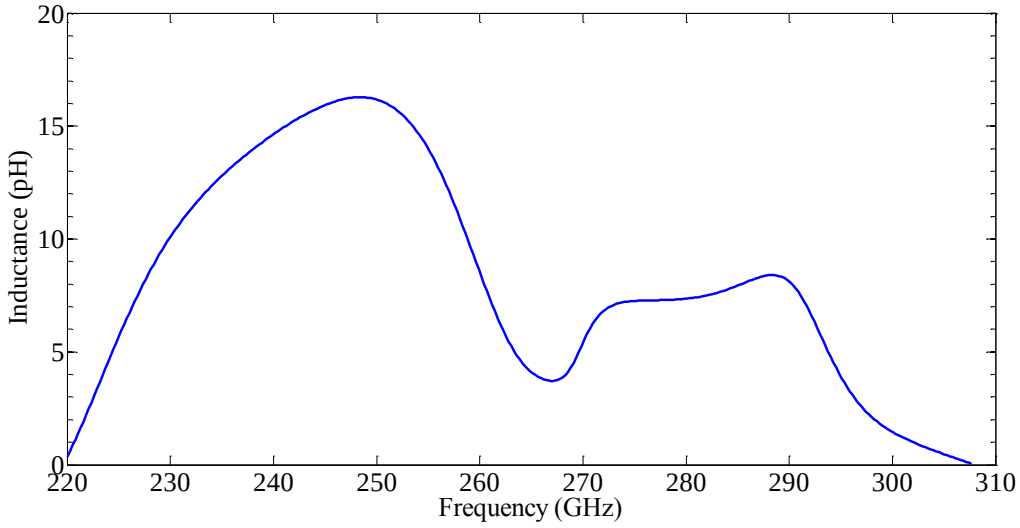


Figure 6.22: *Simulated real part of the of the bow-tie antenna impedance with 50 Ω CPW feed line.*



(a)



(b)

Figure 6.23: *(a) Simulated reactance of the of the bow-tie antenna impedance with 50 Ω CPW feed line.(b) Extracted equivalent inductances.*

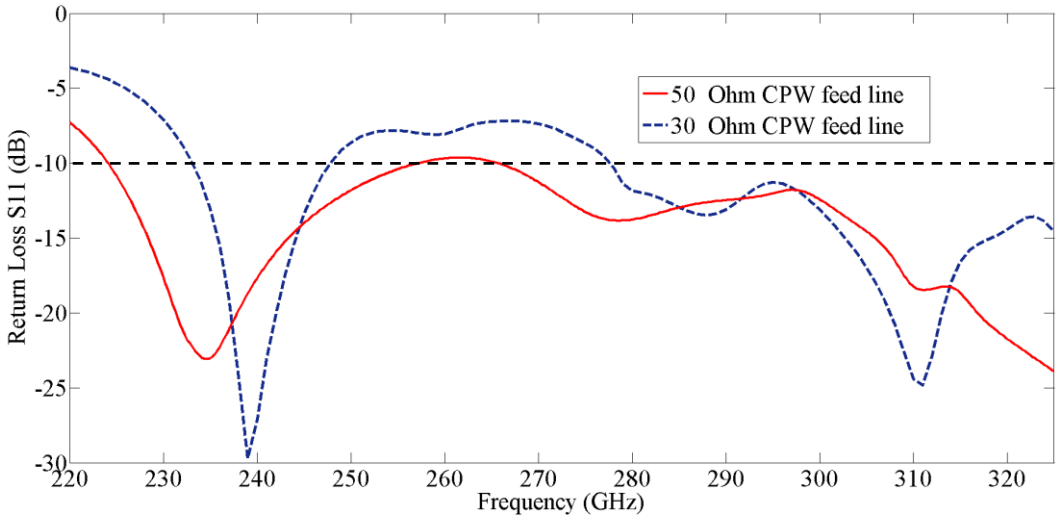


Figure 6.24: *Simulated return loss of the single port-fed antenna with 50 Ω and 30 Ω CPW feed lines. The bandwidths of the two antennas are comparable. Therefore, the feed line can be chosen according to the RTD device negative differential conductance to improve the impedance matching and so deliver higher power.*

6.6.6 Efficiency, Gain, and Radiation Pattern

Due to the lack of measurement facilities at these very high frequencies, the antenna radiation performance was only characterised through simulation using HFSS. The simulated antenna overall efficiency and the antenna radiation efficiency are plotted in Figure 6.25 and Figure 6.26, respectively. The antenna overall efficiency is 80% at the lowest frequency in the band (220 GHz) and increases to 95% at 320 GHz. The radiation efficiency (which describes the ratio of the radiated power to the accepted power) is around 92% in average across the entire simulated frequency band.

The antenna gain was also simulated and plotted in Figure 6.27. The gain values ranges from 4 dB (at 230 GHz) and 11 dB (at 280 GHz). The low gain value at a given frequency indicates that the antenna has broad beam-width. For instance,

Figure 6.28 shows the simulated 3D radiation pattern at 230 GHz which has a maximum gain of 4 dB. It can be seen that the antenna radiates almost the same power in a wide angular range (beam-width) above the antenna. On the other hand, the high gain indicates that the antenna has directional performance at a specific direction as shown in Figure 6.29 which plots the pattern at 280 GHz with maximum gain of 11 dB. That is, the radiation intensity is larger at the direction of the maximum gain compared to other directions. It is also important to note that the proposed antenna radiates upward toward the air side (perpendicular to the substrate) which proves the advantages of both the diced antenna and the reflector ground plane which is placed on the bottom side of the InP substrate.

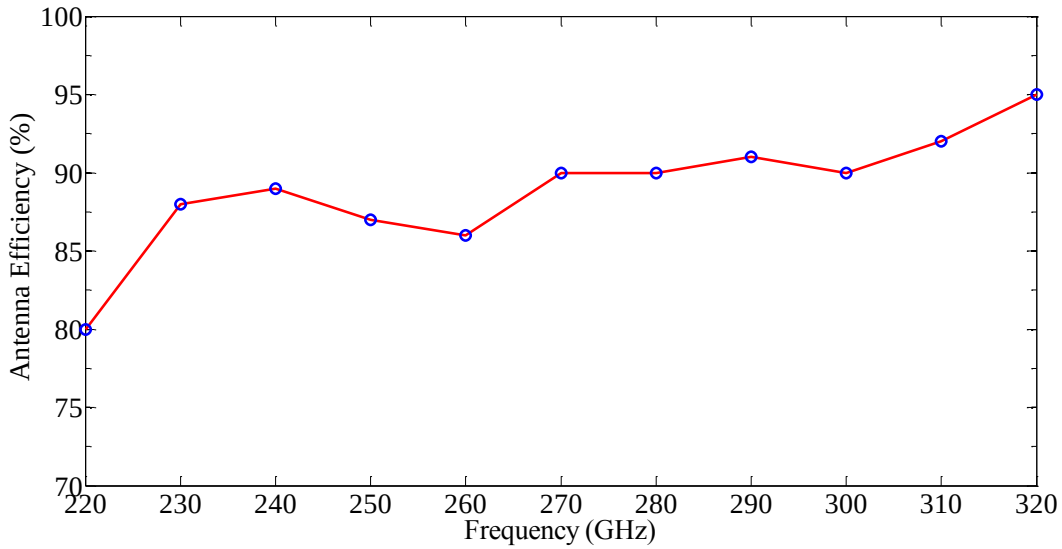


Figure 6.25: *Simulated overall efficiency of the one port bow-tie antenna which describes the ratio of the radiated power to the incident power.*

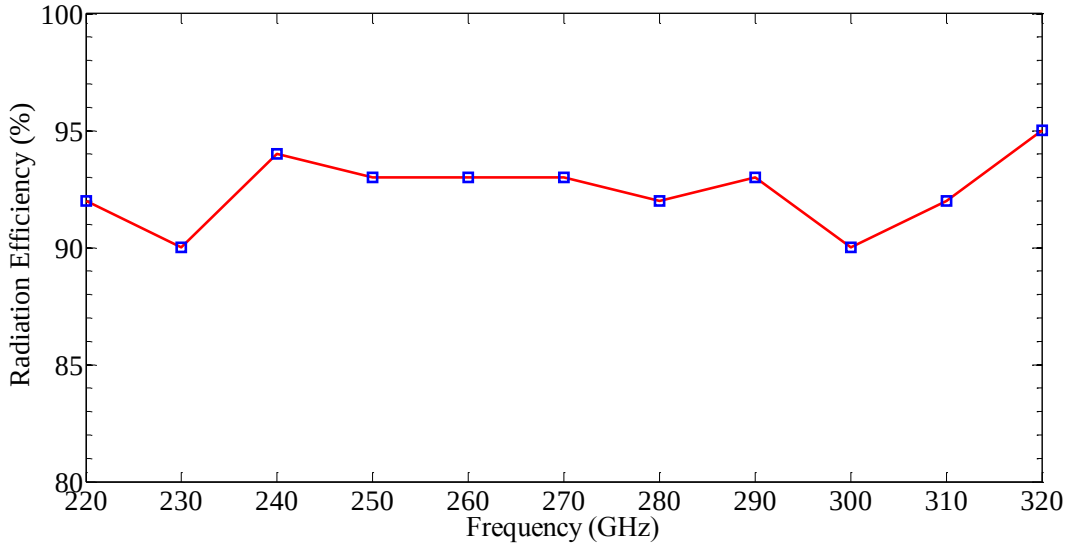


Figure 6.26: *Simulated radiation efficiency of the one port bow-tie antenna which describes the ratio of the radiated power to the accepted (delivered) power.*

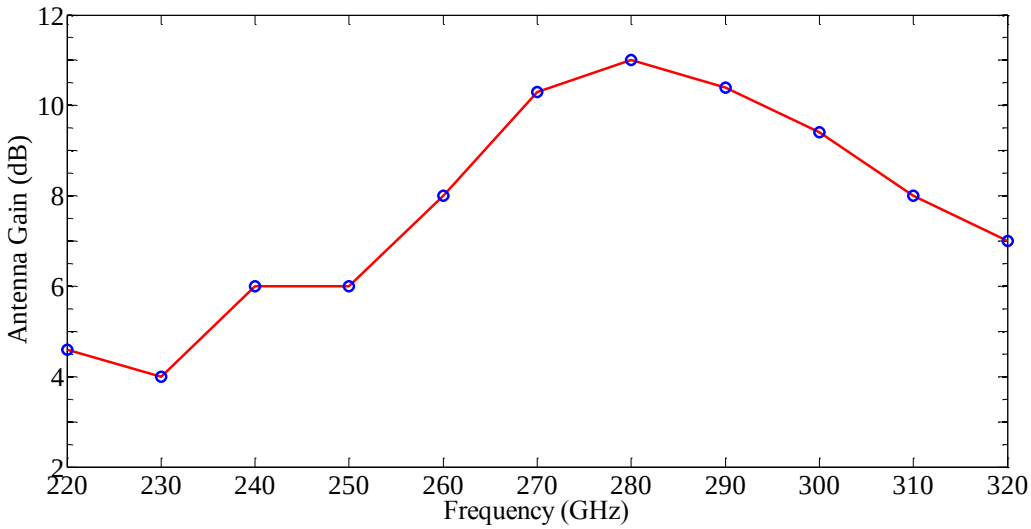


Figure 6.27: *Simulated gain of the one port bow-tie antenna. Higher gain values indicate more directivity.*

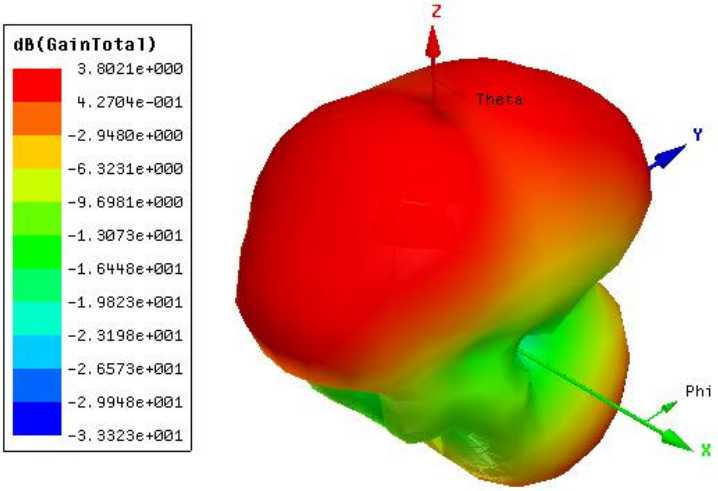


Figure 6.28: *Simulated 3-D radiation pattern of the one port bow-tie antenna at 230 GHz. The antenna has a maximum gain of 4 dB and wide beam-width.*

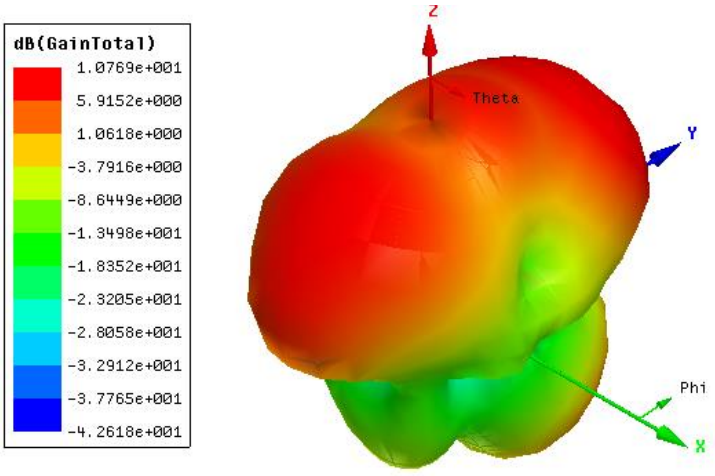


Figure 6.29: *Simulated 3-D radiation pattern of the one port bow-tie antenna at 280 GHz. The antenna has a maximum gain of 11 dB and directional performance with two major lobes.*

6.6.7 Two Port Bow-tie Antenna

The one port antenna described above can be integrated with the single and double RTD oscillators described in Chapter 5. For the integration with the coupled oscillators, which can employ up to four RTD devices, the bow-tie was further investigated with a two port design. The antenna was designed with the same dimensions presented above but with two 50 Ω CPW feed lines. Figure 6.30 shows a picture of the fabricated two port bow-tie antenna.

The measured return loss (S_{11} and S_{22}) of the fabricated two port antenna are shown in Figure 6.31, while Figure 6.32 shows the measured insertion loss (S_{21} and S_{12}). All the 4 S-parameters indicate that most of the signal send towards the antenna is accepted, and little is reflected back (S_{11} and S_{22} less than -10 dB) or transmitted through to the other port (S_{21} and S_{12} less than -10 dB) across the majority of the measured frequency band. Compared with the return loss obtained from one port antenna in Figure 6.21, the return loss from the two ports are similar in general with some discrepancy that might be due to the measurement environment, e.g. close proximity of the pair of probes and reflections. The simulated antenna overall efficiency and the antenna radiation efficiency of the two port bow-tie antenna are plotted in Figure 6.32 and Figure 6.33, respectively. The antenna overall efficiency is ~ 65 % on average. The radiation efficiency (which describes the ratio of the radiated power to the accepted power) is around 93% on average across the entire simulated frequency band. Thus, the two port bow-tie antenna is a good candidate to be integrated with the coupled oscillator circuit that can employs four RTD devices for high power operation.

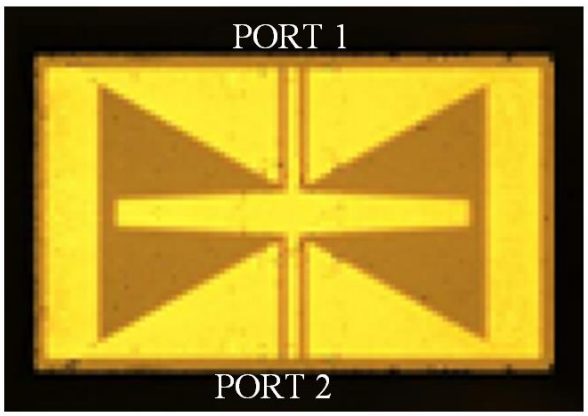


Figure 6.30: *Fabricated bow-tie antenna with two CPW feed lines. The antenna dimensions are the same as of the antenna shown in Figure 6.20.*

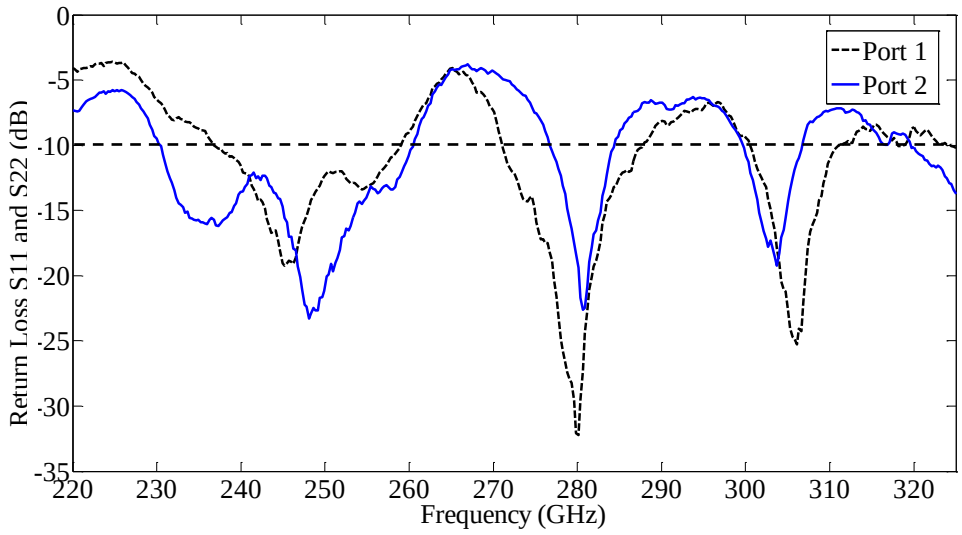


Figure 6.31: *Return loss (S_{11} and S_{22}) of the two port bow-tie antenna with tuning stub.*

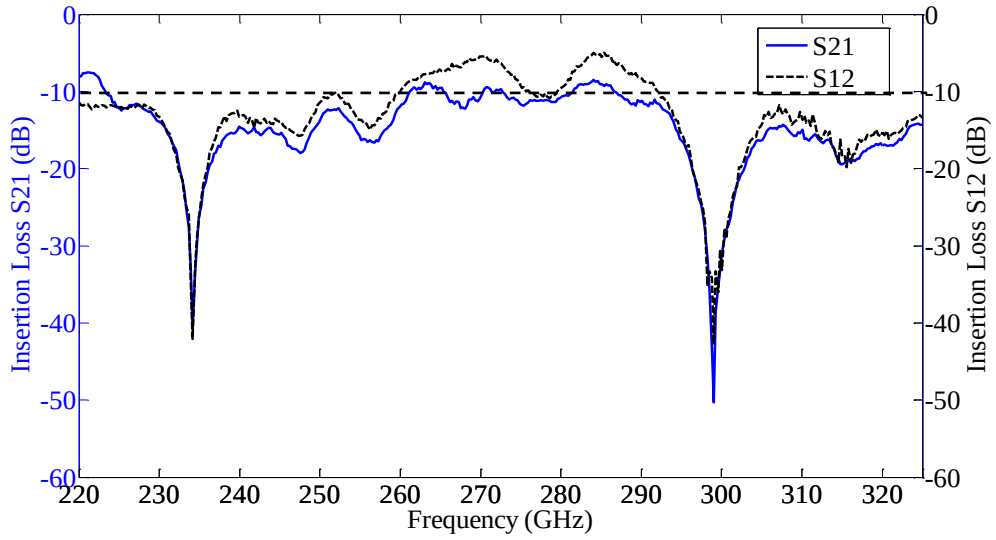


Figure 6.32: *Insertion loss (S_{21} and S_{12}) of the two port bow-tie antenna with tuning stub.*

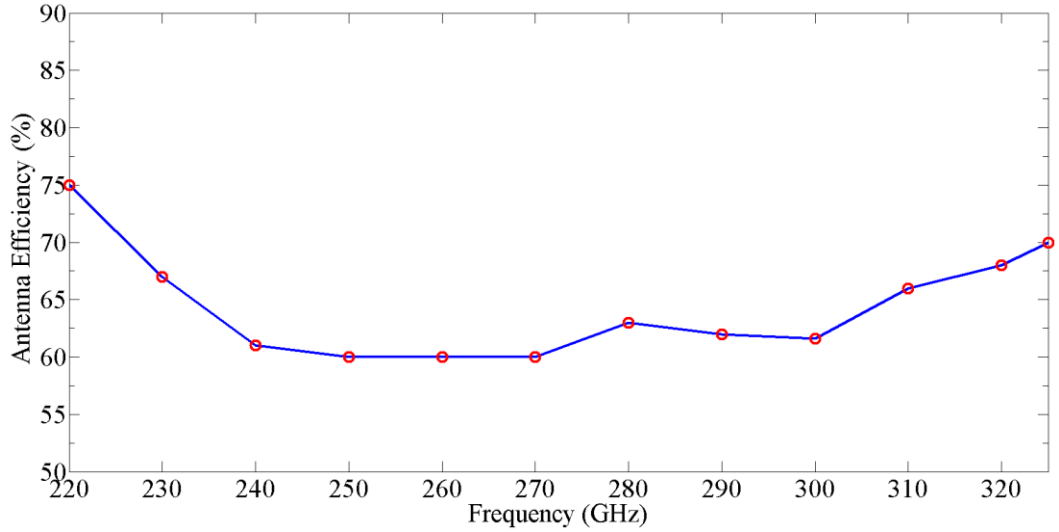


Figure 6.33: *Simulated overall efficiency of the two port bow-tie antenna which describes the ratio of the radiated power to the incident power.*

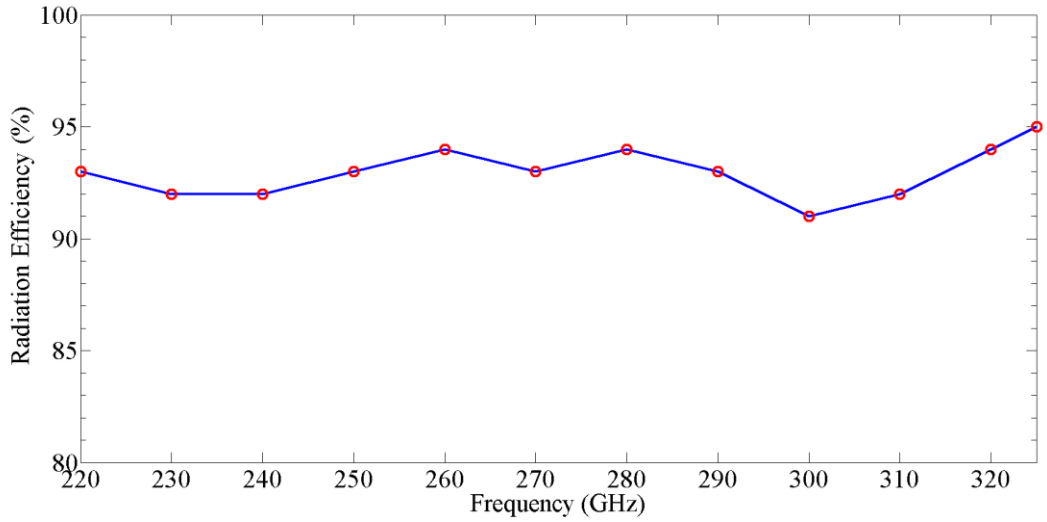


Figure 6.34: *Simulated radiation efficiency of the two port bow-tie antenna which describes the ratio of the radiated power to the accepted (delivered) power*

6.7 Discussion

The characterisation of the one port and two port bow-tie antennas presented in this chapter showed the possibility of integration with the different RTD oscillator types presented in this thesis. Possible schematic structures for integrating the bow-tie antenna with different RTD oscillators are shown in Figure 6.35. The integration of the antenna with the single oscillator (with two RTD devices) is shown in Figure 6.35 (a) while the integration with the coupled/synchronised oscillator (with four RTD devices) is shown in Figure 6.35 (b). In both schematics, MIM capacitors have to be designed to act as a short circuit at the oscillation frequency and isolate the DC electrodes (DC-Block).

It was shown in Figure 6.23 that the reactance part of the antenna is inductive across the majority of the measured frequency band. The effect of the antenna inductance on the designed oscillation frequency can be explained by the means of the equivalent circuit of the RTD-bow-tie antenna integration in Figure 6.36. The oscillation frequency is when the susceptance is equal to zero, i.e.

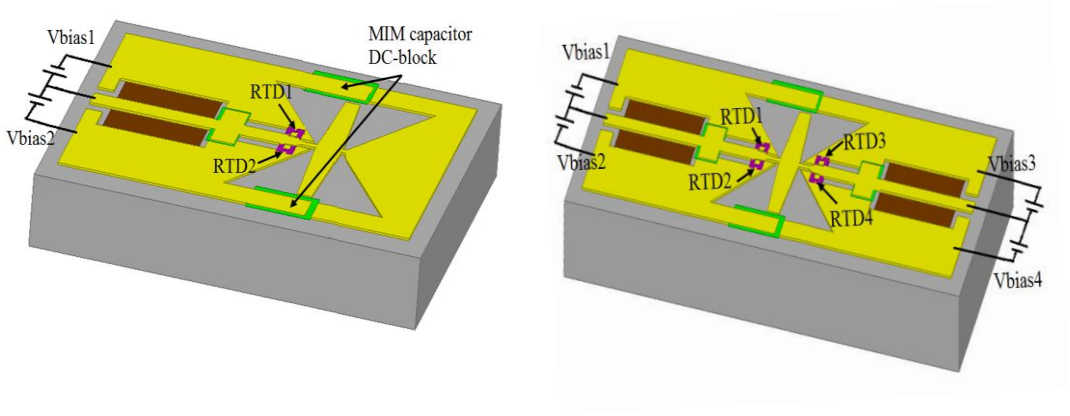
$$j\omega_o C_n + \frac{1}{j\omega_o L} + \frac{1}{j\omega_o L_{ant.}} = 0 \tag{6.5}$$

then,

$$\omega_o = \frac{1}{\sqrt{C_n L_{eq}}} \tag{6.6}$$

where $L_{eq} = \frac{L_{ant.}L}{L_{ant.}+L} \approx L$ when $L_{ant} \gg L$.

If the antenna inductance $L_{ant.}$is much larger than the resonating inductance L then the oscillation frequency will not change.



(a) (b)

Figure 6.35: *Schematic structure for integrating the bow-tie antenna presented in this project with: (a) the two RTD oscillator, and (b) the coupled/synchronised RTD oscillators.*

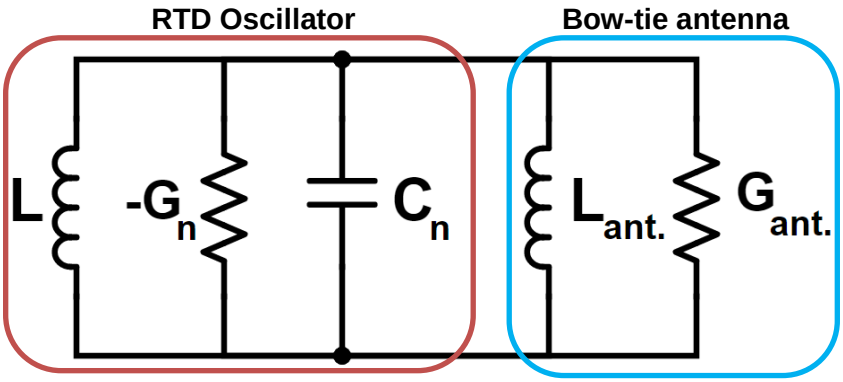


Figure 6.36: *Equivalent circuit of the RTD oscillator integrated with bow-tie antenna. L denotes the resonating inductance realised in the RTD oscillator circuit. $-G_n$ and C_n are the RTD device negative differential conductance and the self-capacitance, respectively. $L_{ant.}$ and $G_{ant.}$ are the inductance and the conductance of the integrated bow-tie antenna.*

6.8 Summary

This chapter discussed the main challenges when designing antennas on large dielectric constant substrates such as the InP. In addition, reported antennas for RTD and with different ideas to supress the substrate effects were reviewed. Broad band bow-tie antenna with air-side radiation in new design configuration was proposed, designed, and realised. The bandwidth extends almost the entire J-band (220 GHz to 325 GHz). One port and two ports bow-tie antennas were designed and characterised to investigate the suitability of the antennas to be integrated with the oscillators realised in this project. The one port antenna showed the suitability of integration with the single RTD oscillators while the two port antenna showed the suitability of integration with the coupled/synchronised oscillators.

Chapter 7 Conclusion and Future Work

7.1 Conclusion

Resonant tunnelling diodes (RTDs) are considered to be the fastest semiconductor-based electronics devices with the potential to generate up to 2.5 THz signals at room temperature [21]. Up to date, RTD oscillators at 1.92 GHz with 0.4 μW output power have been demonstrated [28]. Although high oscillation frequencies have been reported, the main limitation of RTD oscillators is the low output power. The purpose of this PhD thesis was to realise a microwave/millimetre-wave monolithic integrated circuits (MMIC) RTD oscillator with frequencies in the J-band (220 – 325 GHz) range with around a milli-Watt output power fabricated using photolithography.
The main results achieved in this project are:

I. Oscillators in coplanar waveguide (CPW) technology

- *Single RTD oscillator*:

A 244 GHz RTD oscillator with 0.2 mW (-7 dBm) output power and a 233 GHz with 0.264 mW (-5.8 dBm) power, where each oscillator employed one RTD device, were demonstrated. The 244 GHz oscillator employed one 4 μm × 4 μm RTD device, while the 233 GHz oscillator employed one 5 μm × 5 μm device.

- *Two RTD Oscillator:*

A series of different oscillators each employing two RTD devices of the same size (4 μm × 4 μm) connected in parallel, and different CPW lines of

different characteristic impedances Z_o (50 Ω, 32 Ω, and 25 Ω) and lengths producing different oscillation frequencies and power were demonstrated. A 308 GHz with 0.31 mW (-5 dBm) was demonstrated with a 10 μm long shorted 25 Ω CPW, while 304 GHz with 0.33 mW (-4.8 dBm) was demonstrated with 3 μm long shorted 50 Ω CPW. For an oscillator with 7 μm long 50 Ω shorted CPW, the oscillation frequency was 245 GHz with 0.42 mW (-3.8 dBm), while a higher oscillation frequency of 309 GHz with 0.26 mW (-5.6 dBm) was demonstrated from oscillator with same CPW length but with Z_o = 25 Ω. Oscillation frequency of 254 GHz with 0.4 mW (-4 dBm) was demonstrated with 8 μm long 32 Ω CPW. For an oscillator with two 3 μm × 3 μm RTD devices and with 10 μm long shorted 50 Ω CPW, 284 GHz with 0.46 mW (-3.37 dBm) was demonstrated. With an optimised layout, a power of 0.593 mW (-2.3 dBm) at 312 GHz was demonstrated from the circuit that employs two 4 μm × 4 μm RTD devices and 13 μm long 50 Ω CPW.

- *Coupled oscillators:*

RTD oscillators employing mutual coupling were also demonstrated. The maximum demonstrated output power of the coupled oscillators which included two 4 μm × 4 μm RTD devices in total was 0.374 mW (-4.3 dBm). The individual oscillator (with one RTD) produced 0.2 mW (-7 dBm). Another coupled oscillator included two 5 μm × 5 μm RTD devices in total demonstrated power of 0.625 mW (-2 dBm) while the individual oscillator produced 0.264 mW (-5.8 dBm) power at 233 GHz.

The highest power in this project was demonstrated from the coupled oscillators that included four 4 μm × 4 μm RTD devices in total. 1.1 mW (0.45 dBm) was demonstrated while the individual oscillator (with two devices) produced 0.593 mW (-2.3 dBm) power at 312 GHz.

II. Oscillators with shorted microstrip lines for inductance realisation

- *Single RTD oscillator*:

A 312 GHz RTD oscillator with 0.146 mW (-8.4 dBm) output power was demonstrated from the oscillator that employed one 4 μm × 4 μm RTD device and 88 μm long shorted 10.4 Ω microstrip line, and a 262 GHz with 0.186 mW (-7.3 dBm) was demonstrated from the oscillator that employed one 5 μm × 5 μm RTD device and 65 μm long shorted 10.4 Ω microstrip line.

- *Coupled oscillators:*

Output power of 0.493 mW (-3.1 dBm) was demonstrated from the coupled oscillator that included two 5 μm × 5 μm RTD devices in total. The individual oscillator (with one device) produced 0.186 mW (-7.3 dBm) power at 262 GHz.

The RTD device self-capacitance (C_n) was estimated using Equation 1.1, where accurate characterisation of the RTD when biased in the NDR region is non-trivial due to the effects of bias oscillations. Equation 1.1 has been considered as a good approximation for C_n which is important in estimating the oscillation frequency in the RTD oscillators [22], [33]. Nevertheless, there was a good agreement between calculated and measured frequencies in oscillators realised in this project.

III. Broadband Bow-tie Antenna

The main issues with different reported planar antennas for RTD-based oscillators were reviewed and discussed. The reported patch antenna on BCB layer requires relatively thick BCB to improve the radiation performance which means thick

RTD mesa is also required since the two electrodes of the RTD device are connected to the patch and the ground plane. Thick RTD mesa would increase the self-inductance and the series resistance. The challenges in designing high performance integrated antenna on large dielectric constant substrates were discussed as well. A novel antenna design was designed, simulated, fabricated, and characterised in this project. It was a bow-tie antenna with tuning stub that has very wide bandwidth in the J-band. The antenna was diced and mounted on a reflector ground plane to alleviate the effect of the large dielectric constant substrate (InP) and radiates upwards to the air-side. The antenna does not require additional component to extract the RF signal. The antenna was also designed in one port and two port configurations to investigate the suitability of integration with the different MMIC RTD oscillators realised in this project. Measured and simulated S-parameters proved the suitability of this antenna for integration with the RTD oscillators presented in this PhD thesis.

7.2 Future Work

7.2.1 High Power and High Oscillation Frequencies

As described in Chapter 5, large RTD devices can be employed in a RTD oscillator circuit to increase the output power. To further increase the power, power combining circuits presented in the project (up to four large RTD devices and a single load) can be employed. Higher oscillation frequency (> 1 THz) can be achieved by reducing the CPW/microstrip length and maintain the RTD device sizes. Microstrip line of 10.4 Ω (with 20 μm wide signal line) was designed in this project to realise very small inductance per unit length. The estimated oscillation frequency is ~ 0.9 THz when 5 μm long microstrip line and two 4 μm × 4 μm RTD devices are employed in the oscillator circuit. Future research should employ 60 μm wide signal line with which the characteristic impedance reduces

to 3.8 Ω and, therefore, realise lower inductance per unit length. With this configuration, the 5 μm long microstrip line in an oscillator circuit with two 5 μm × 5 μm RTD devices can generate higher power at similar oscillation frequency (~ 1.1 THz). A 1.7 THz can be also achieved with extremely short 2 μm lines. Future work should also optimise the fabrication process to reduce the series contact resistance to increase the output power. Revised device design that can provide lower V_P (as close as much to zero volts) will improve the oscillator efficiency. In addition, the efficiency can be further improved by optimised layout to omit or remove the resistor R_e.

7.2.2 Optimised Fabrication

Since the sizes of the RTD devices fabricated in this project were relatively large (3 μm × 3 μm to 5 μm × 5 μm), wet etching was used to define the mesa. Although wet etching is fast process, the device performance might be affected by the created undercut. Dry etching with vertical side wall should be used and compare the performance with the oscillators fabricated with wet etching.

In this project, polyimide was used for different purposes such as RTD device passivation and isolation between the emitter and collector metal pads. One of the main purposes was to prevent the break in the metal (used as a cushion) when it is deposited on two areas of two different levels (e.g. the InP substrate and high level RTD mesa). This polyimide cushion allows for the deposition of thin metal layer. Figure 7.1 shows a SEM picture of a RTD device with non-broken metal on top of polyimide cushion (the right hand side of the picture) and broken metal (on the left hand side of the picture). Figure 7.2 shows close-up SEM picture of both broken and non-broken metals. The metal thickness was 400 nm which is comparable to the step to the RTD mesa. The polyimide cushion is important when thin layer of metal is sufficient (e.g. in the DC circuits). However, at RF

frequencies in a RTD oscillator, this extra area of metal on top of polyimide will change the characteristics of the RF pads (e.g. 50 Ω CPW line) which is mainly designed considering the InP as a substrate. In addition, parasitic components will be created (e.g. inductance) and will change the oscillator performance. To avoid these issues, future research should eliminate the use of polyimide cushion and deposit thick metal to avoid any break and losses in the RF signals.

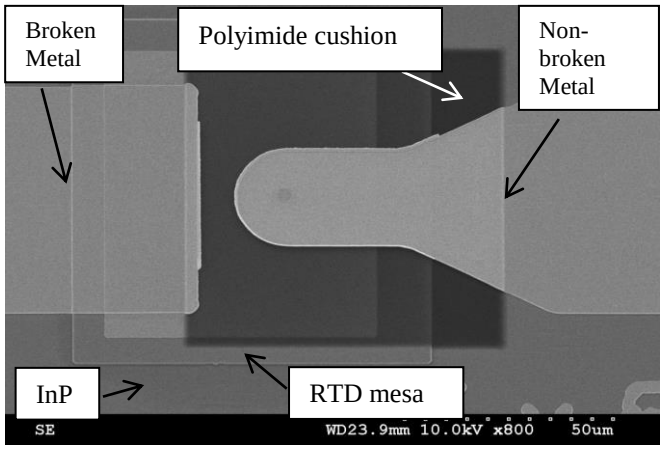
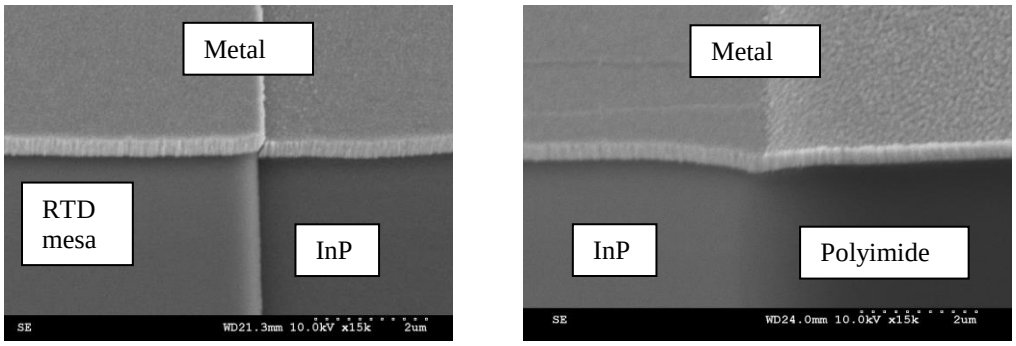


Figure 7.1*: SEM picture of RTD device showing the use of polyimide cushion to prevent metal break. The metal on the right hand side was not broken due to the use of the polyimide cushion while the metal on the lift hand side was broken because of the step between the InP substrate and the RTD mesa.*



(a) (b)

Figure 7.2: *(a) Close-up SEM picture of the broken metal. (b) Close-up SEM picture of the non-broken metal on top of polyimide cushion.*

7.2.3 Bow-tie Antennas

The bow-tie antenna described in this project was designed for J-band (220 – 325 GHz) operation. Future work should experimentally measure the radiation patterns to verify the simulated ones. In addition, future work also required to scale the design to higher frequency bands and characterise the performance for different InP substrate thicknesses to investigate the effect of the thickness. Future research should also fabricate and characterise the integrated bow-tie antenna presented in this project with all types of the RTD oscillators. The main observation should be focused on the frequency of the radiated signal and compare it with the on-wafer measured frequency from the same oscillator design but without antenna.

In summary, high performance RTD oscillators and antenna were demonstrated in this thesis. The oscillators could form compact basic building block for THz system and realise different applications such as short-range wireless communication and imaging radar.

Appendix A. Fabrication Process

I. RTD Oscillators in CPW technology:

a. Sample cleaning

Ultrasonic bath in acetone for 3 minutes

Ultrasonic bath in methanol for 3 minutes

Ultrasonic bath in IPA for 3 minutes

Rinse in de-ionised (DI) water for 3 minutes

Blow Dry with N_2

b. Top contact metal

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115^{o}C for 1 minute

Dip in Chlorobenzene for 5 minutes

Expose by MA6 for 2 seconds

Develop in 1:1 MDC:H_2O for 50 seconds

Rinse in DI water for 1 minute

Blow dry with N2

Ash at 60W for 2 minutes

Argon Gunn for 20 seconds (in Plassys 4)

Deposit Ohmic contact Ti/Pd/Au 20/30/150 nm

Lift-off in acetone at 50 ^{o}C for 20 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

c. Etch to the bottom contact layer

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115^{o}C for 1 minute

Expose by MA6 for 2 seconds

Develop in 1:1 MDC:H_2O for 50 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Ash at 60W for 2 minutes

Dip in H_3PO_4:H_2O_2:H_2O=1:1:38 for 4 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

d. Bottom contact metal

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115^oC for 1 minute

Dip in Chlorobenzene for 5 minutes

Expose by MA6 for 2 seconds

Develop in 1:1 MDC:H_2O for 50 seconds

Rinse in DI water for 1 minute

Blow dry with N2

Ash at 60W for 2 minutes

Argon Gunn for 20 seconds (in Plassys 4)

Deposit Ohmic contact Ti/Pd/Au 20/30/150 nm

Lift-off in acetone at 50 ^oC for 20 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

e. Etch to InP substrate

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115^oC for 1 minute

Expose by MA6 for 2 seconds

Develop in 1:1 MDC:H_2O for 50 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Ash at 60W for 2 minutes

Dip in H_3PO_4:H_2O_2:H_2O=1:1:38 for 4 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

f. Passivation and via openning

Spin polyimide PI2545 at 8000 rpm for 30 seconds

Put in 180^oC oven for 6 hrs.

Spin S1805 at 1500 rpm for 30 seconds

Bake on hotplate at 115^oC for 2 minutes

Expose by MA6 for 2.2 seconds

Develop in 1:1 MDC:H_2O for 50 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Bake on hotplate at 115^oC for 10 minutes

Etch by CF_4/O_2 5/95 sccm in 80 plus RIE for ~ 6 minutes

Strip S1805 in 1165 photoresist stripper at 50 ^oC for 60 minutes

g. Thin-film resistor

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115^oC for 1 minute

Dip in Chlorobenzene for 5 minutes

Expose by MA6 for 2 seconds

Develop in 1:1 MDC:H_2O for 50 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Ash at 60W for 2 minutes

Dip in HCL:H_2O=1:5 for 20 seconds

Deposit NiCr 33 nm

Lift off in acetone at 50 ^oC for 20 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

h. 1st bond pad

Spin LOR 10A at 6000 rpm for 30 seconds

Bake on hotplate at 150 ^oC for 3 minutes

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115 ^oC for 2 minutes

Expose by MA6 for 2 seconds

Develop in MF319 for 75 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Ash at 60W for 2 minutes

Deposit contact metal Ti/Au 20/400 nm

Lift off in 1165 photoresist stripper at 50 ^oC for 20 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

i. Si_3N_4 Insulator

Spin LOR 10A at 6000 rpm for 30 seconds

Bake on hotplate at 150 ^{o}C for 3 minutes

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115 ^{o}C for 2 minutes

Expose by MA6 for 2 seconds

Develop in MF319 for 75 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Ash at 60W for 2 minutes

Deposit SiNx 75 nm by ICP-CVD

Lift off in 1165 photoresist stripper at 50 ^{o}C for 20 minutes

Rinse in DI water for 3 minutes

Blow dry with N2

j. 2nd bond pad

Spin LOR 10A at 6000 rpm for 30 seconds

Bake on hotplate at 150 ^{o}C for 3 minutes

Spin S1805 at 4000 rpm for 30 seconds

Bake on hotplate at 115 ^{o}C for 2 minutes

Expose by MA6 for 2 seconds

Develop in MF319 for 75 seconds

Rinse in DI water for 1 minute

Blow dry with N_2

Ash at 60W for 2 minutes

Deposit contact metal Ti/Au 20/400 nm

Lift off in 1165 photoresist stripper at 50 ^{o}C for 20 minutes

Rinse in DI water for 3 minutes

Blow dry with N_2

II. RTD Oscillators in Microstrip technology:

Use the same processes described above but with the following steps order*:*

1. (a)

2. (b)

3. (c)

4. (d)

5. (e)

6. (g)

7. (h)

8. (f)

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