THE FABRICATION OF VERY SHORT GATE-LENGTH GaAs FIELD EFFECT TRANSISTOR DEVICES

A thesis submitted to
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by

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CONTENTS

Summary

The object of the work described in this thesis was to fabricate GaAs Metal-Semiconductor Field Effect Transistors with gate lengths comparable with the smallest structures fabricated previously in this Department using electron beam lithography. It was envisaged that MESFETs would be fabricated on both solid substrates and on thin active membranes of GaAs. It was then hoped to transfer the technology developed for the fabrication of MESFETs to the fabrication of High Electron Mobility Transistors (HEMTs).

A substantial part of the work was devoted to the development of a low temperature contact technology which could be used for the formation of ohmic contacts to GaAs. The low temperature was thought to be necessary to prevent undesired diffusion of the contact material during annealing, particularly on devices with closely spaced drain-source contacts. It was found that by varying the contact composition, a reduction in optimum annealing temperature of over 100 oC could be achieved without a reduction in specific contact resistance.

The MESFETs were designed to conform to a geometrical layout suggested by Plessey (Caswell) which would allow them to be bonded for rf testing. With this design, MESFETs with gate lengths down to 0.055 μm were fabricated and tested both at dc and at high frequency. Devices were fabricated on several different substrates and were optimised for maximum dc transconductance. The devices worked well at dc exhibiting transconductance values as high as had been reported for similar device structures, but the ac measurements (s-parameters) were disappointingly poor.

A new isolation technique was also developed - isolation using a boron ion implant - to replace mesa isolation. As this was only fully developed towards the end of the project only a specimen number of devices were fabricated using the technique. However, the process has subsequently been adopted by other workers in the electron-beam lithography group and has been shown to work satifactorily.

With the development of the boron isolation technique it was possible to consider fabricating FET type devices on thin GaAs membranes (<100 nm). Various new processing methods combined with those already available, were used to produce a device with ohmic contacts on an area of active GaAs membrane, which was isolated from the rest of the wafer. Unfortunately, the material parameters were not suitable for continuation of this work, but, since the conclusion of this project, another worker has shown that devices may yet be made on a GaAs membrane.

Finally high electron mobility transistors were studied. A design for such a device was compiled and the material grown in this Department. Devices were fabricated and tested at dc where errors originating with the initial design became obvious. It was however, established from these results, that the devices operated in good agreement with theoretical predictions.

0.1 Introduction

Photolithography is by far the most important tool in the semiconductor industry for defining the features which form solid state electronic circuits. The advancement in expertise in this field has, so far, enabled the industry to fabricate circuits of progressively increased complexity by the reduction of device dimensions. Unfortunately, the minimum feature size which can be defined optically is determined by the wavelength of the illuminating radiation. This sets a resolution limit for photolithography at approximately 0.3 μm (deep ultraviolet radiation). Future circuit requirements may demand smaller feature sizes, tending towards the sub 0.1 um or nanometer scale, in which case alternative lithographic techniques will have to be found. X-ray and ion beam lithography are possible alternatives but, to date, the highest resolution has been obtained using electron beam lithography (EBL) where 10 nm linewidths have been demonstrated [0.1,0.2]. Currently the principal use of EBL systems is in the fabrication of reticle masks for use in optical lithography. More importantly, from a research point of view, the mask can be disposed of completely and patterns can be exposed directly (Direct Write) onto wafers coated in electron sensitive resist. The Direct Write system is particularly useful for research applications because of the ease of which pattern information, stored in computer memory, can be modified as needs demand. The main disadvantage of direct write EBL systems is that the sequential manner in which the pattern is scanned imposes limitations on sample throughput. It is therefore unlikely that the technique will be adopted for mass production purposes.

The electron beam lithography group in this Department was set up about seven years ago to study the limitations of electron beam lithography as a tool for fabricating extremely small features, less than 0.1 μm in size. Much of the early work consisted of writing metallic gratings on thin, electron transparent substrates; initially carbon [0.3,0.4] but more recently on silicon nitride [0.5] and GaAs membranes [0.1,0.6].

The ultimate linewidth and pitch resolution obtained on these thin substrates (silicon nitride) was 10 nm and 40 nm respectively [0.1]. More recently the emphasis has been on transferring the lithographic technology to the fabrication of devices which might exhibit interesting characteristics because of their small dimensions. In particular Mackie [0.1] developed the techniques for fabricating very short gate-length GaAs MESFETs and Binnie [0.7] studied the fabrication of small geometry silicon MOSFETs.

0.2 Project Outline

The aim of the work done for this thesis was to develop the techniques for fabricating very short gate-length GaAs MESFETs and to attempt to fabricate a MESFET device on a thin active layer of GaAs. It has been predicted that devices with dimensions of the order a few tens of nanometers would have different characteristics from similar devices with larger dimensions [0.8,0.9]. In simple terms, the carriers in an extremely small device would have a reasonable chance of being transfered ballistically between contacts; without experiencing any scattering events in the substrate. If this happens, the electrons would not reach an equilibrium velocity meaning that classical device physics no longer apply. Using high resolution electron beam lithography it was envisaged that MESFETs with gate lengths down to 50 nm, or less, could be fabricated on solid substrates. This dimension is still too large to expect truly ballistic effects but it was hoped that novel device characteristics would be observed because of the very smallness of the device. The reason for attempting to fabricate devices on a thin GaAs membranes was to take advantage of the very high resolution pattern definition capabilities previously demonstrated in this Department [0.1,0.3-6]. It would then be possible to fabricate transistors with a gate length of the order of 10 nm and drain-source spacing about an order of magnitude higher.

The work was divided into the following main sections:-

(1) The development of a low temperature annealing process for

forming ohmic contacts to GaAs. It was envisioned that the low temperature anneal would enable closely spaced contacts to be formed without interdiffusion of the contact material between contacts.

(2) Qualitative analysis of the annealed contacts using x-ray microanalysis to study the lateral diffusion of contacts on a thin GaAs membrane and Auger analysis to examine contacts formed on solid substrates.

(3) Processing and testing of GaAs MESFETs fabricated on a number of different substrates. The MESFETs were optimised for maximum dc transconductance. When tested at dc the output characteristics were good even down to a gate-length of 55 nm. Unfortunately, the ac (s-parameter) measurements taken from a selection of these devices were unsatisfactory.

(4) Development of an isolation technique to replace the conventional mesa isolation method. A novel ion implantation process (metal on polymer mask) was developed using a positive on negative two layer resist system.

(5) Fabrication of devices on thin active GaAs membranes isolated using boron implantation. Although no working transistors were produced the results obtained indicated that the fabrication of such a device is still a distinct possibility.

(6) A brief study of High Electron Mobility Transistors (HEMTs) was made, from the material design through to the manufacture and testing of devices.

A short description of the lithographic processes used throughout this work is given in the following chapter. The ohmic contact processing and analysis are described in chapters 2 and 3. Chapter 4 is devoted to the fabrication of GaAs MESFETs on solid substrates. Included in this chapter is the dc characterisation of devices fabricated on different substrates as well as s-parameter measurements (up to 18 GHz) of a selection of these devices. A novel ion implantation masking technique is described in chapter 5. Chapter 6 deals with the processes

required in the fabrication of MESFET devices on thin GaAs membranes. The design, fabrication and testing of HEMT devices is given in Chapter 7. Finally, some overall conclusions and suggestions for future work are given in chapter 8.

Chapter 0 References

[0.1] WS Mackie, PhD Thesis, University of Glasgow (1984).

[0.2] HG Craighead, RE Howard, LD Jackel, PM Manckiewitch, "10-nm Linewidth Electron-Beam Lithography on GaAs," Appl. Phys. Lett **43** p38 (1983).

[0.3] SP Beaumont, T Tamamura, CDW Wilkinson, "Two Layer Resist System for Efficient Lift-Off in Very High Resolution Lithography," Proc. Microcircuit 80, Amsterdam, (1980)

[0.4] SP Beaumont, PG Bower, T Tamamura, CDW Wilkinson, "Sub-20-nm-wide Metal Lines by Electron Beam Exposure of thin Poly(methylmethacrylate) films and Lift-Off," App. Phys. Lett. **38** p436-438 (1981).

[0.5] SP Beaumont, B Singh, CDW Wilkinson, "Very High resolution Lithography-Thin Films or Solid Substrate?" Proc. 10th International Conf. on Electron and Ion Beam science and Technology, montreal, Canada (1982).

[0.6] WS Mackie, SP Beaumont, CDW Wilkinson, JS Roberts, "High Resolution Lithography on Active Semiconductor Membranes," Ref. 0.5.

[0.7] CE Binnie, PhD Thesis, University of Glasgow (1985).

[0.8] MS Shur, LF Eastman, "Ballistic Transport in Semiconductors at Low-temperatures for Low-Power, High Speed Logic," IEEE Trans. Elect. Dev. **ED-26**, 1677-1683 (1979).

[0.9] LF Eastman, R Stall, D Woodward, N Dandekar, CEC Wood, M Shur, K Board, "Ballistic Motion in GaAs at Room Temperature," El. Lett. **16**, p524-525 (1980).

1.1 Itroduction

Much has already been written about electron-beam litographic processing in the theses of Mackie [1.1], Binnie [1.2] and Rishton [1.3]. Therefore a detailed review of all the processing steps used in this work will not be presented here. However, for completeness, a brief description of the main processes is given in the following sections. A recently published article by Mackie and Beaumont provides a good overview of nanometer lithographic techniques [1.4].

1.2 Exposure System

The machine used in this project was a Philips PSEM 500 scanning electron microscope which was modified for lithography. The main modifications were:-

(a) The addition of a beam blanking system to prevent undesired exposure of the sample. When this feature is selected, control of the electron beam is switched from the internal raster scan generator to an external digital scan generator. Both the beam blanking and scan generator are controlled by a microcomputer. This was originally a KIM microprocesser with only a temporary memory which meant that pattern data had to be transfered from the GEC 4180 mainframe computer at every exposure session. The KIM has now been replaced with an Ithaca microcomputer which has the facility for storing all the pattern data on disc.

(b) A transmission detector was fitted in the specimen chamber for the exposure and examination of thin substrate specimens.

The Philips machine has a range of electron spot sizes from 8 nm up to 1 μm and an accelerating voltage which is continuously variable from 1.5 to 50 kV. The spot size selected for exposure purposes depended mainly on the frame size and area of the feature to be exposed but the accelerating voltage was invariably set at 50 kV for maximum resolution.

A schematic representation of the scanning electron-beam exposure system is shown in fig. 1.1. Each pattern file is generated on a GEC 4180 computer, using an interactive pattern editor (DESIGN) developed by Mackie [1.1]. The files are transfered to the microcomputer where they are stored on disc. A program (EBSS) is run on the microcomputer which sends pattern data sequentially to the scan generator which, in turn, generates the reversing raster scan that defines each rectangle. When the beam is scanned over the electron sensitive resist, the structure of the resist is modified in such a manner that either the exposed or the unexposed resist can be selectively removed in a suitable developer. The patterned resist layer can then be used as a stencil to transfer a metallic pattern onto the wafer or it can be used as a mask for etching.

1.3 DESIGN and SHAPES

DESIGN is the interactive pattern editor used for pattern development and is run on a GEC 4180 computer. Since describing DESIGN in his thesis, Mackie has modified the program to cater for multi-level pattern editing which has proved to be most useful in the design of complete mask sets for device manufacture. The basic concepts of the program however, are the same as described in ref. [1.1]. The data file generated using DESIGN contains the coordinates of the opposite corners of each rectangle in the pattern as well as the appropriate exposure information for each section of the pattern.

SHAPES is a simple program which was written for this thesis to generate triangular or trapezoidal patterns made up of a series of narrow rectangles. Although this program is not incorporated into DESIGN, the output of SHAPES is in a form which can be used directly in DESIGN for final pattern editing. Using SHAPES, it is assumed that two sides of the figure are parallel to the x-axis. However, by reducing one of the parallel sides to a point, it is possible to generate triangular patterns (fig. 1.2.). The y coordinates of the top and bottom sides of each pattern, the x coordinates of all of the corners (defined clockwise from the bottom left hand corner) and the number of rectangles per figure are specified for each separate pattern. The diamond shape shown

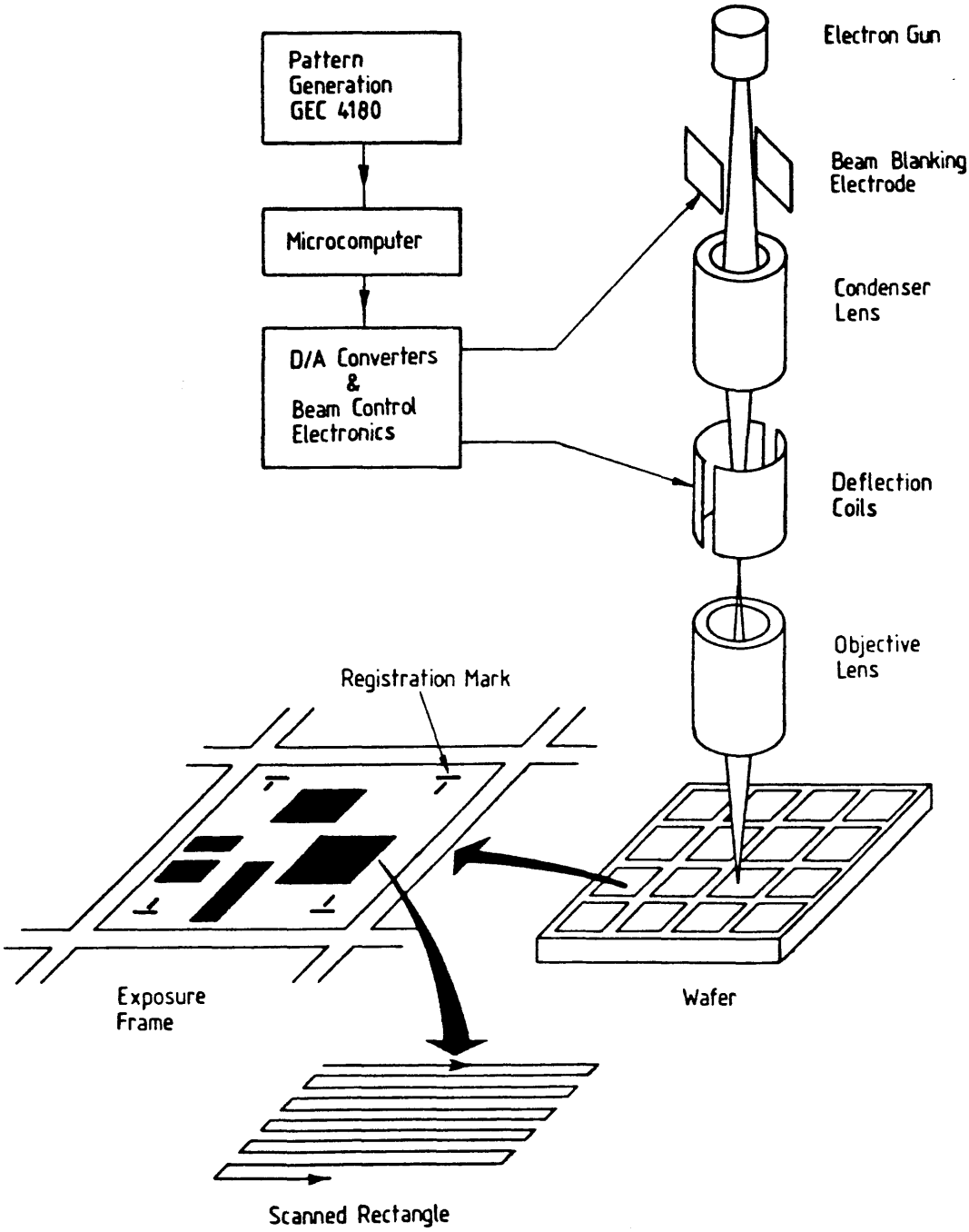


Fig.1.1 Schematic illustration of the electron-beam exposure system used throughout this project.

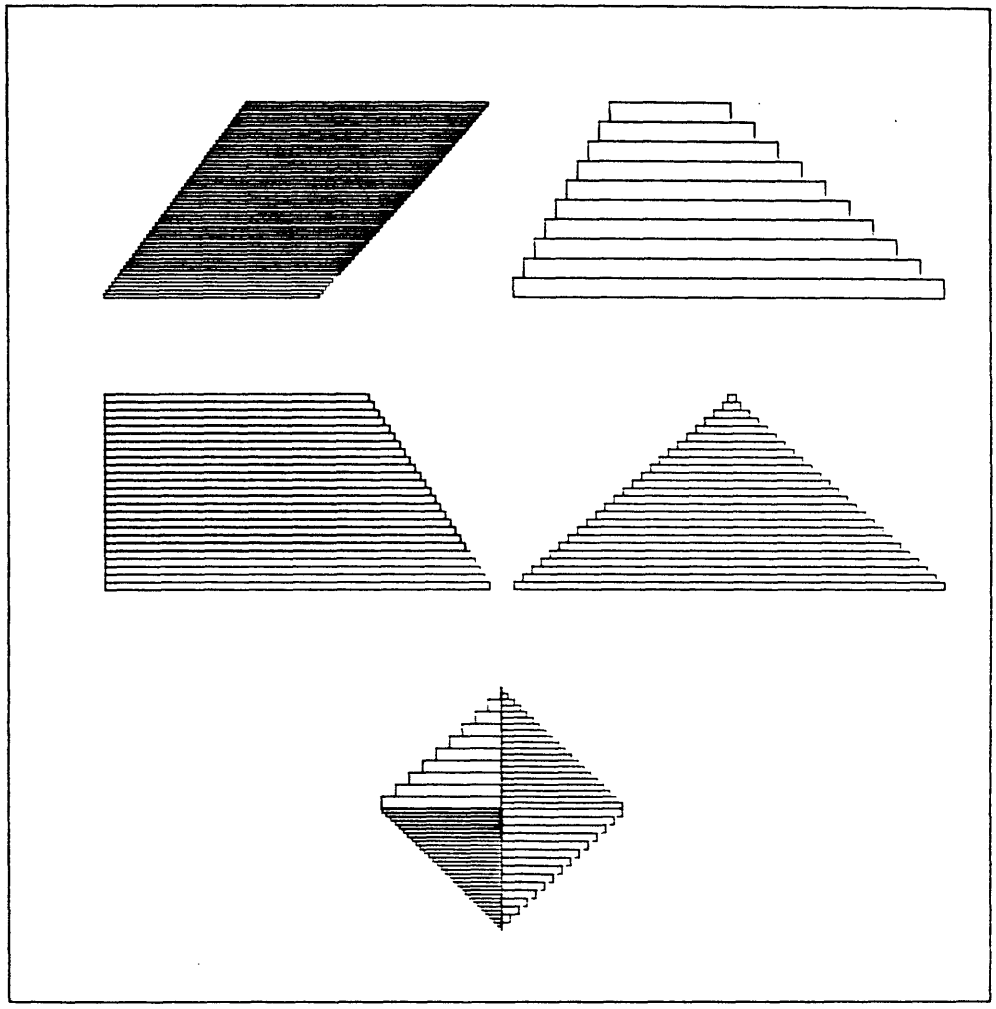


Fig. 1.2 Examples of the patterns which can be generated using the program "SHAPES".

in fig.1.2 was made up of four individual parts and each part was made up with a different number of rectangles. The choice of the number of rectangles per figure depends on how smooth the edges of the final exposed pattern needs to be. Clearly the more rectangles specified per figure the less apparent it will become that the pattern is, in fact, made up of a group of individual rectangles. It should be noted that the maximum number of rectangles which can be stored in a DESIGN file is 1000 so this has to be taken into consideration when creating a pattern using SHAPES. In this work the main pattern which utilised this program was the ohmic contact pattern of the GaAs MESFETs (Sect. 4.2.6) which contained 950 rectangles.

1.4 Pattern Replication

1.4.1 Resist

There are two types of resist; **positive** resist where the areas of resist exposed by the electron beam are subsequently dissolved in a developer and **negative** resist where it is the unexposed resist which is dissolved. Negative resist (in this case polyimide) was only used as part of a novel process for fabricating metal on polymer ion implantation masks and circuit crossover points. This is described in full in chapter 5 and so requires no further mention here. The bulk of the work was carried out using Poly (Methyl MethAcrylate) (PMMA) positive resist. When PMMA is illuminated by an electron beam the molecular structure of the exposed area of the resist is modified by the beam. Put simply, the long molecular chains are severed principally by the secondary electrons generated in the resist from inelastic scattering of the primary beam electrons [1.3,1.5,1.6]. The modified resist areas can be selectively dissolved in a suitable solvent such as Methyl IsoButyl Ketone (MIBK). Conventially, the developer solution consists of part MIBK and part Iso Propyl Alcohol (IPA) the latter of which dissolves neither the exposed or unexposed resist. The ratio of MIBK to IPA essentially determines the sensitivity, contrast and edge definition of the resist [1.4].

The main pattern replication techniques employed in the work

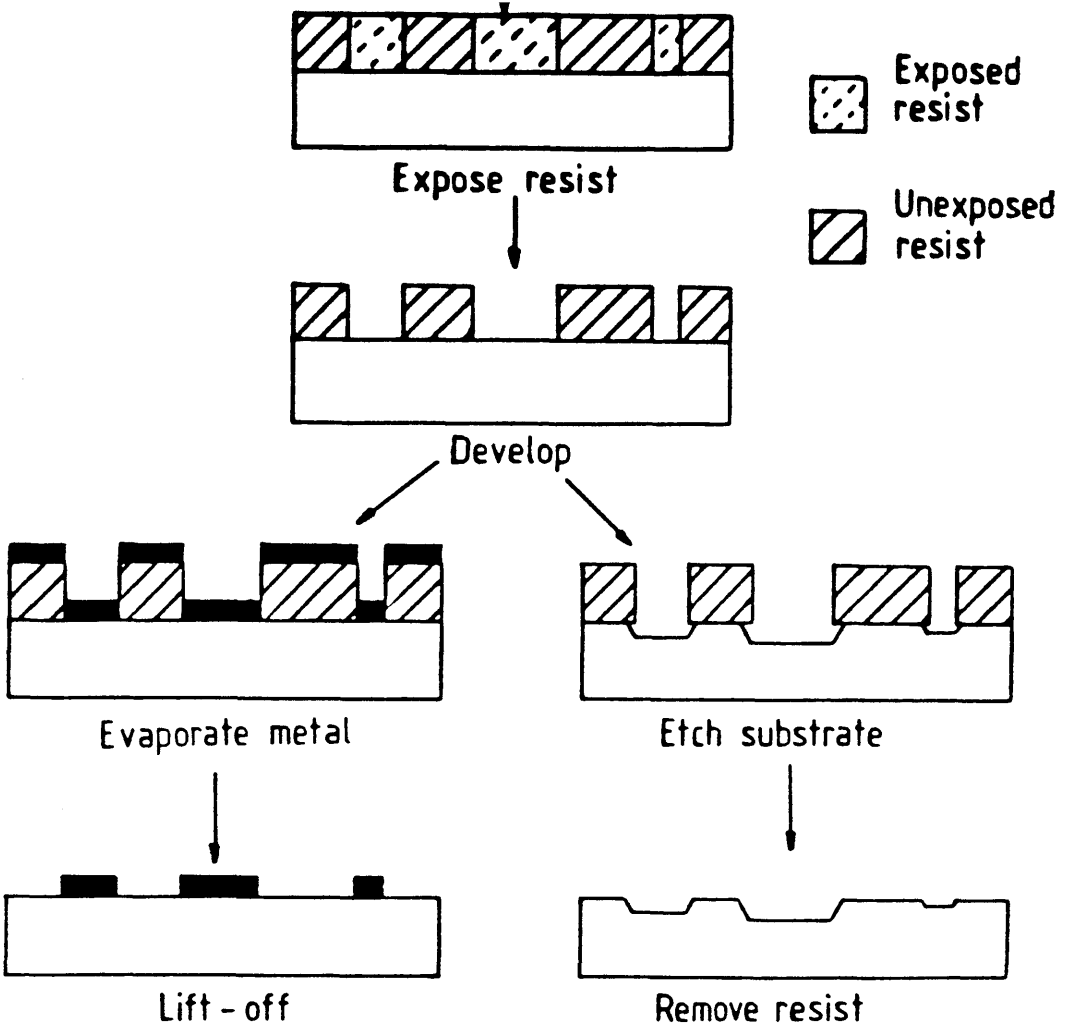


Fig. 1.3 Illustration showing the lift-off and etching techniques used in this work.

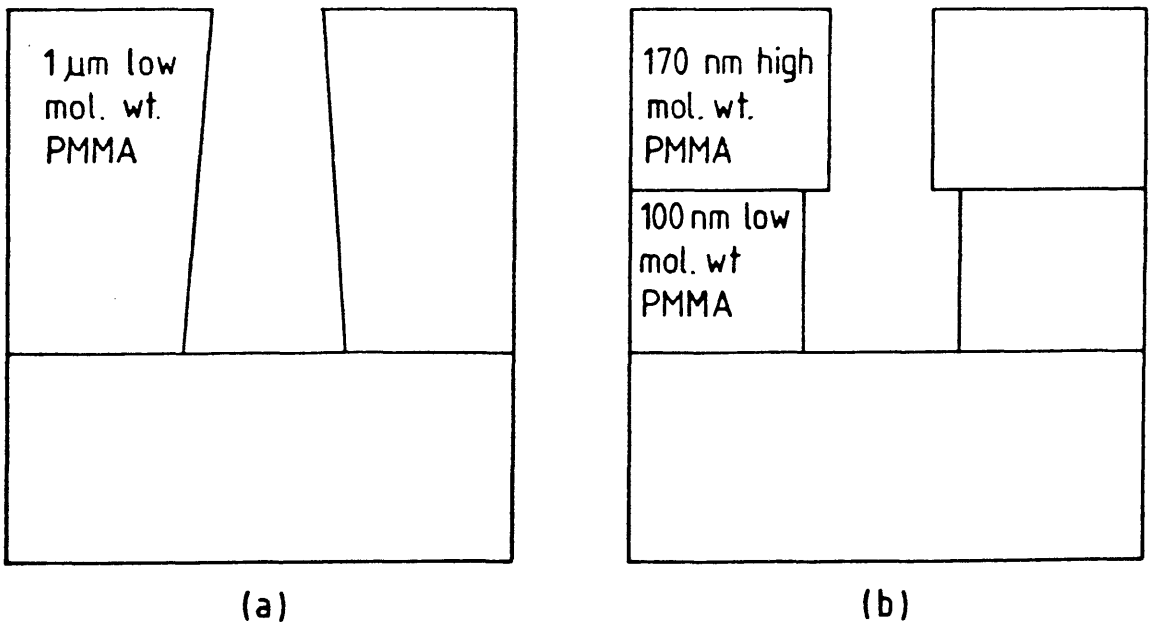


Fig.1.4 Developed profiles of the two main resists used for pattern definition. (a) Low resolution resist for all lift-off and etching steps other than those associated with gate definition. (b) Two layer, high resolution resist for defining very short gates.

of this thesis were lift off and etching. These processes are illustrated in fig 1.3. The lift-off process uses a patterned PMMA film as a stencil for transfering a metallic pattern to the specimen surface. After processing the resist, a metallic layer is deposited over the entire surface of the wafer (thermal evaporation was used throughout this project). The unwanted metal is then removed by dissolving the remaining PMMA in acetone, leaving the desired metal pattern on the wafer. Patterned resist films were also used as masks for etching the substrate material below the resist. Care had to be taken in the preparation of an etch mask to ensure good adhesion between the resist and substrate (Sect. 1.4.2).

Two resist sytems were used extensively throughout this project:-

(a) A thick (1 μm), single layer of low molecular weight PMMA (185 000) and

(b) A high resolution two layer resist consisting of a 170 nm layer of high molecular weight PMMA (350 000) on 100 nm of low molecular weight PMMA (185 000).

Resist (a) was used for defining thick metallic patterns (low resolution) by lift-off. The profile of this resist after development is shown in fig. 1.4 a). The undercut profile is a consequence of the divergence of the electron-beam as it passes through the resist film (due to elastic and inelastic scattering events). Fortunately, this profile is ideal for lift-off because the metal evaporated over the resist is completely separated from the metal on the specimen surface. This allows easy access of the solvent to the remaining resist and facilitates good, clean lift-off of the unwanted metal [1.1,1.2.1.4].

Resist (a) was also used successfully as a wet etch mask for various applications. This resist was chosen because of the small amount of pinhole defects associated with the thick resist and for its resistance to the etch solutions, provided it was properly prepared (see following section).

Resist (b) was used only for the definition of the very narrow lines used in the formation of Schottky gates on GaAs MESFETs. When developed, the two layer resist also exhibits a desireable undercut profile (fig. 1.4b)) which improves the reliability and quality of the lifted-off lines. The undercut, in this case, arises because the lower layer of resist is more sensitive than the upper layer. Thus, when the resist is developed, more material is dissolved from the bottom layer, leaving the undercut profile shown in the figure [1.1,1.2,1.4,1.7].

1.4.2 Choice of Casting Solvent

The PMMA, as received from the manufacturers, was in powder form and had to be dissolved in a suitable solvent before it could be spin coated onto wafers for processing. There were essentially four readily available solvents which could be used; MIBK, chlorobenzene, xylene and trichloroethylene. A short experiment was carried out to see if the casting solvent in any way affected the adhesion of the resist to a substrate. First of all, solutions of PMMA dissolved in each of the solvents were made up and characteristic plots of resist thickness (after baking) versus spin speed were obtained. Then, selecting spin speeds for each solution that would produce resist layers of similar thickness (200 nm), several clean GaAs wafers were coated with resist and baked for either 2 hours or overnight (12 h) at 180^{o}C. An arbitary pattern was then exposed in the resist and developed in 1:1 MIBK:IPA. Next, each wafer was immersed in a 10 % ammonia solution, chosen because previous experimental evidence had shown that PMMA (dissolved in xylene) had low resistance to ammonia containing solutions. After 1 minute in ammonia, the wafers were rinsed in deionised water, blown dry, and observed under an optical microscope. In the table 1.1 below the percentage of the PMMA mask remaining on each sample, after being subjected to the ammonia solution, is shown.

TABLE 1.1

CASTING SOLVENT	BAKE TIME	PERCENTAGE OF RESIST FILM REMAINING
MIBK	2 HOURS	100 %
	12 "	100 %
Chlorobenzene	2 "	60 %
	12 "	100 %
Xylene	2 "	0 %
	12 "	50 %
Trichloroethylene	2 "	0 %
	12 "	0 %

The obvious choice of casting solvent for PMMA is MIBK which adhered perfectly to the substrate in this experiment even with just a two hour bake. However, MIBK was not selected because the time taken to dissolve the large amounts of MIBK required to produce a PMMA layer of similar thickness to resist (a) above, was excessive. Consequently chlorobenzene was chosen as the casting solvent for the PMMA layers required for device processing. The 1 μm layer was obtained by dissolving 15 % PMMA by weight in the solvent and spin coating the solution onto GaAs wafers at 5000 rpm. When the resist was to be used as an etch mask it was always baked overnight beforehand. Similarly, the lower layer of the two layer resist (b) was obtained by spinning 4 % PMMA dissolved in chlorobenzene at 6000 rpm. Unfortunately, because the dissolution rate of PMMA in chlorobenzene is very high, this solvent could not be used as the casting solvent for the upper layer of the two layer system. This would have resulted in partial dissolution of the previously applied film as soon as the second solution was applied. Xylene, which is a relatively slow dissolver of PMMA, was therefore chosen as the casting solvent for the second layer resist.

Chapter 1 References

[1.1] WS Mackie, PhD Thesis, University of Glasgow (1984).

[1.2] CE Binnie, PhD Thesis, University of Glasgow (1985).

[1.3] SA Rishton, PhD Thesis, University of Glasgow (1984).

[1.4] WS Mackie, SP Beaumont, "Materials and Processes for Nanometer Lithography," Solid State Tech. Aug 1985, p117-123.

[1.5] AN Broers, "Resolution Limits of PMMA Resist for Exposure with 50 kV Electrons," J. Electrochem Soc. **128** p166-170 (1981).

[1.6] GR Brewer, "Electron-Beam Technology in Microelectronic Fabrication," Academic Press, New York, (1980).

[1.7] CE Binnie, SP Beaumont, CDW Wilkinson, JC White, "The Fabrication of Very Short Gate Length N-Channel MOSFETs by Direct Write Electron Beam Lithography," Proc Microcircuit 82, Grenoble, France (1982).

2.1 Introduction

In the fabrication of semiconductor devices good ohmic contacts need to be formed to transfer current into or out of each device. An ohmic contact is defined as a metal to semiconductor contact that has negligible contact resistance compared with the bulk or spreading resistance of the semiconductor. A good ohmic contact should supply the required current to a device with a voltage drop at the metal semiconductor interface that is sufficiently small compared with the drop across the active region of the device [2.1]. The specific contact resistance, ρ_c, is an important figure of merit for the contacts and is defined as [2.2].

$$\rho_c = \frac{V_c}{J_c} = \frac{\text{Voltage drop across the interface}}{\text{The interfacial current density}}$$

The energy band diagram of a metal-semiconductor barrier under equilibrium conditions is shown in fig. 2.1 ϕ_m is the work function of the metal, ϕ_b is the barrier height, $\Delta\phi$ is the barrier lowering due to image force and V_{bo} is the built in potential.

There are two main current transport mechanisms associated with metal semiconductor barriers. These are thermionic emission of carriers over the metal-semiconductor barriers and tunneling through the space charge region at the metal-semiconductor interface. For contacts to low doped semiconductors ($<10^{17}$ /cm^3), the thermionic emission dominates and lower contact resistances can be obtained using lower barrier heights [2.2]. On highly doped material on the other hand the tunneling process dominates since the width of the potential barrier decreases with increased doping. The best conditions for low resistivity metal-semiconductor contact formation is therefore a high doping concentration, a low barrier height or both. However on GaAs, since the barrier height is essentially independent of the metal used (approximately 0.8 eV) [2.1,2.3], it is necessary to use highly doped semiconductor contact layers for the fabrication of

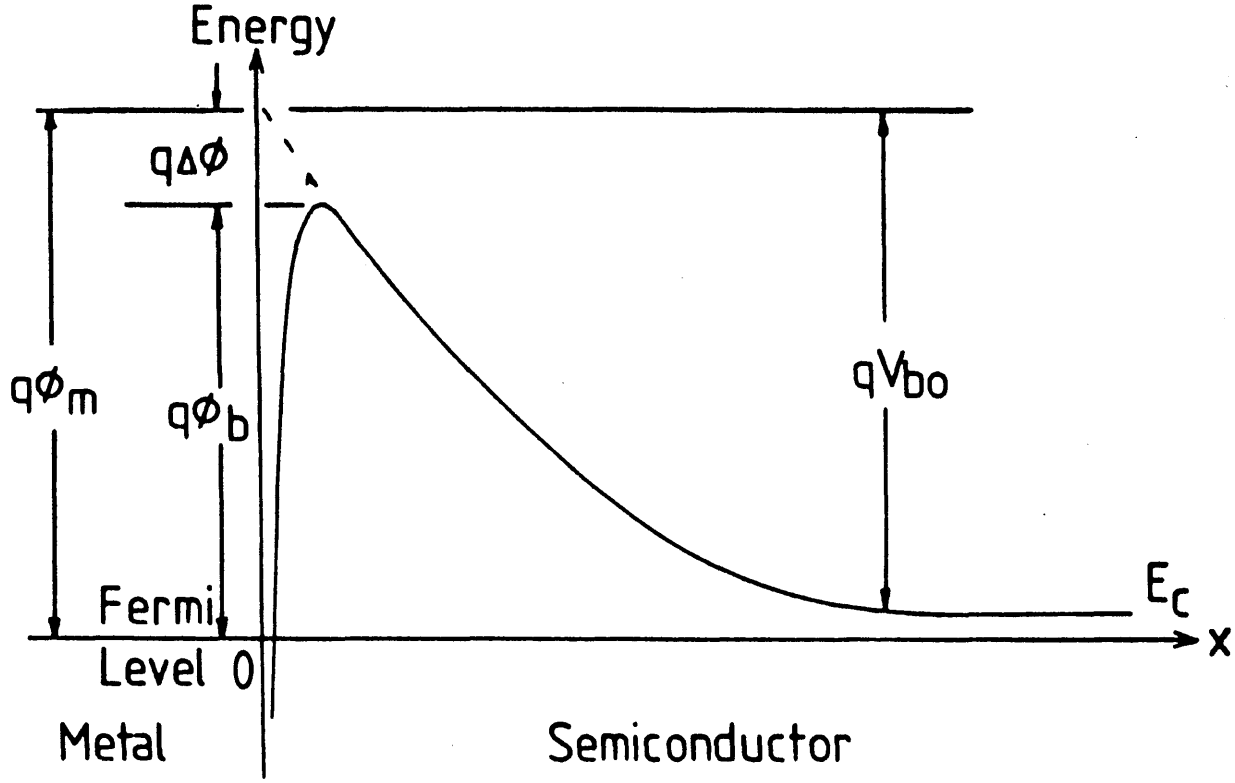


Fig. 2.1 Energy band diagram for a metal-semiconductor contact.

contacts with low resistivities. A paper by Pruniaux [2.4] claims that heating the substrate during contact evaporation will reduce the barrier height. However, since the temperatures required (>150 ^{o}C) are greater than the glass transition temperature of PMMA (100 ^{o}C), this method is not practical for use when lift-off is used for pattern definition.

The doping level of the GaAs epi-layers used for MESFET fabrication (Chap. 4) was typically 10^{18} /cm^{3}; about ten times lower than the doping level required for the potential barrier at the metal-semiconductor interface to appear almost transparent to carrier flow [2.2]. Higher doped material could not be used in MESFET fabrication because, although the ohmic contacts would improve, the Schottky characteristics of the gate, an important element in the devices, would deteriorate. Therefore, the commonly used AuGe/Ni/Au contact system was adopted for producing contacts to GaAs. When these contacts are annealed, complex metallurgical reactions take place and a degenerately doped semiconductor layer is formed beneath the contact. Many attempts have been made to describe these complex reactions; the work of Ogawa [2.5] gives a detailed analysis of annealed contacts.

Essentially the description given by Ogawa for annealed contacts is as follows. At 300 ^{o}C Ge diffuses towards the contact surface and is trapped in the Ni layer. Some of the Ni diffuses inward. At the metal-semiconductor interface GaAs is decomposed partly through the reaction between Ni and GaAs but mainly through the reaction of Au with GaAs where Ni plays the role of a catalyst. At higher temperature (400 ^{o}C) the Ge which was trapped at the surface diffuses inwards and is partly captured by NiAs. The rest of the Ge is considered to be doped into the GaAs.

In the work described here, specific contact resistances around 10^{-5} ohm.cm^{2} were obtained on material originally doped with silicon to 10^{18} /cm^{3}. Theoretically ρ_c on this material should have been about 10^{3} ohm.cm^{2} assuming a barrier height of 0.8 eV [2.2,2.6]. The doping level required to reduce ρ_c to 10^{-5} ohm.cm^{2} is around 3.10^{19} /cm^{3} for the same barrier height. Therefore, during the annealing of the AuGe/Ni/Au contacts the

doping of the semiconductor layer below the contact must have been increased by more than an order of magnitude.

2.1.2 Chapter Outline

In this chapter the experimental work done on the fabrication of ohmic contacts to n^+ GaAs is described. In particular, the development of a low temperature annealing process for contacts to thin epi-layers (<100nm) will be given. Low temperature annealing was desireable, particularly in devices with small source-drain gaps, to ensure that the lateral diffusion of the contact material during annealing does not adversly affect the GaAs in the vicinity of the gate. It was thought that if the annealing temperature could be reduced from the standard temperature for AuGe/Ni/Au of 420 ^{o}C to less than 300 ^{o}C (below the eutectic temperature of AuGe 365 ^{o}C), then the diffusion of the contact material during annealing would be significantly reduced.

Before describing the low temperature annealing process for contacts to thin n+ GaAs epi-layers a description of the transmission line model used in the analysis of contact parameters will be given. Then the initial experiments on AuGe contacts to epitaxial and bulk n^+ substrates, including the effects of anneal temperature and time, are described. Finally the optimisation of AuGe/Ni/Au contacts for low temperature annealing will be described. The following chapter contains the analysis of contacts on solid substrates using Auger Analysis and of contacts on thin substrates using Energy Dispersive X-ray microanalysis.

2.2 Transmission Line Model

2.2.1 Introduction

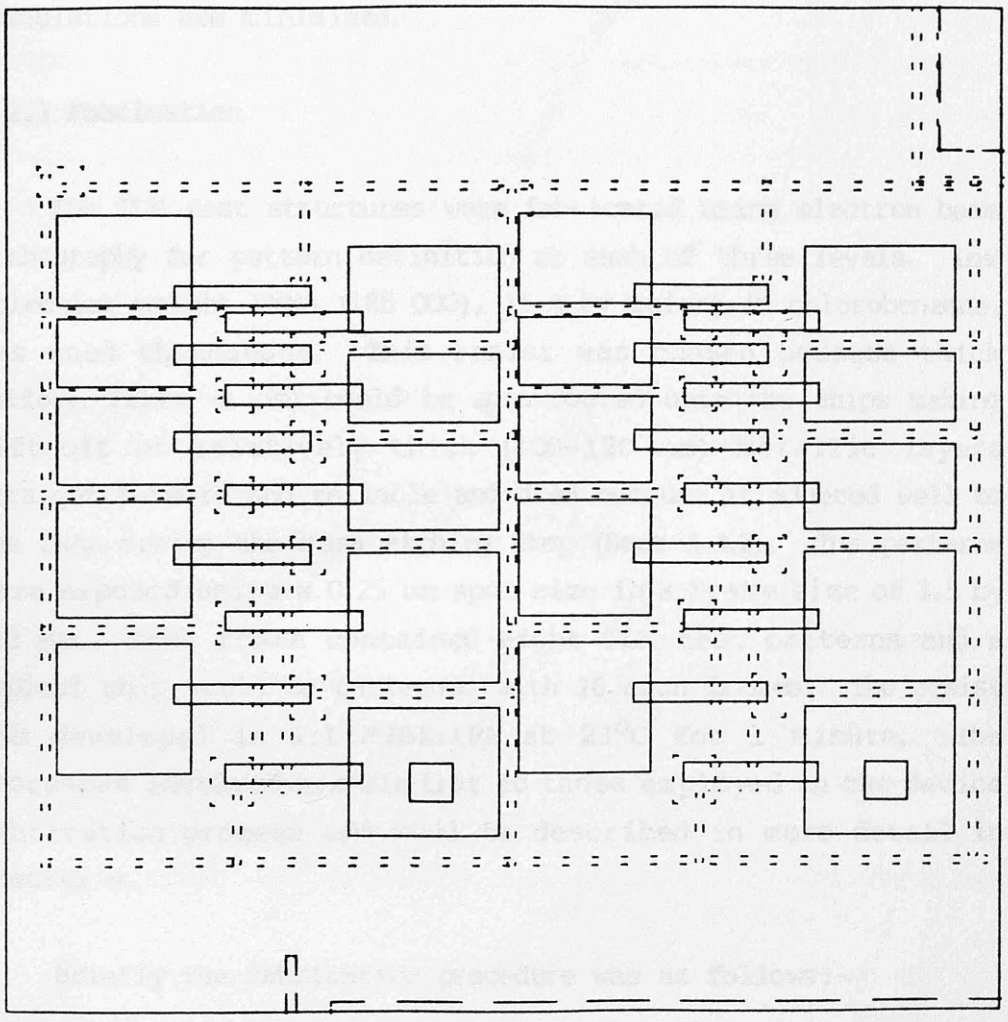
The tool used in the analysis of planar ohmic contacts is the transmission line model (TLM) developed by Murrmann and Widmann [2.7] and independently by Berger [2.8]. In this model the

contacts are modelled as a distributed circuit analogous to that of a transmission line. A detailed description of the TLM is given in appendix 2A.

In the original model, the sheet resistance of the semiconductor directly below the contact is assumed to be the same as the semiconductor layer outside the contact region. This assumption is not however realistic for the contacts studied here as it is likely that the diffusion depth of the annealed Au/Ge/Ni contacts will be greater than the n+ GaAs epi-layer thicknesses (<100 nm) [2.5]. Hence, it is reasonable to assume that the metallurgical reactions that take place during contact annealing will significantly change the sheet resistance of the semiconductor below the contact [2.6,2.9]. Therefore the modified TLM model described by Kellner [2.9] and Reeves and Harrison [2.10] was used in the analysis of all the contacts made to thin epi-layers. In this model, the difference in sheet resistance of the semiconductor layer outside the contact (R_{sh}) and that underneath the contact (R_{sk}) is taken into account. It should be noted that the resulting values of specific contact resistance obtained using the modified TLM were often more than an order of magnitude greater than those evaluated using the standard models of Berger and Murrmann and Widmann. This was consistent with the observations made by both Kellner and Reeves and Harrison.

2.2.2 TLM Test Structure

The final version of the transmission test structure consisted of a set of ten identical contact stripes patterned over 14 or 20μm wide mesas of n^+ GaAs (fig 2.2). These contacts extended from the mesa to larger pads approximately 100 μm square which were used for probing. The distance between the contacts (L) varied in increments of about 4 μm from 2 μm up to 38 μm. From the measured resistance values between contacts (R_T) a graph of R_T v L with 9 data points could be plotted. Also from the test pattern up to 8 values of the so called contact "end resistance" (R_e) [2.8-10] could be determined from groups of three contacts. R_e is defined as the potential at the end of a contact divided by the current flowing into that contact (see



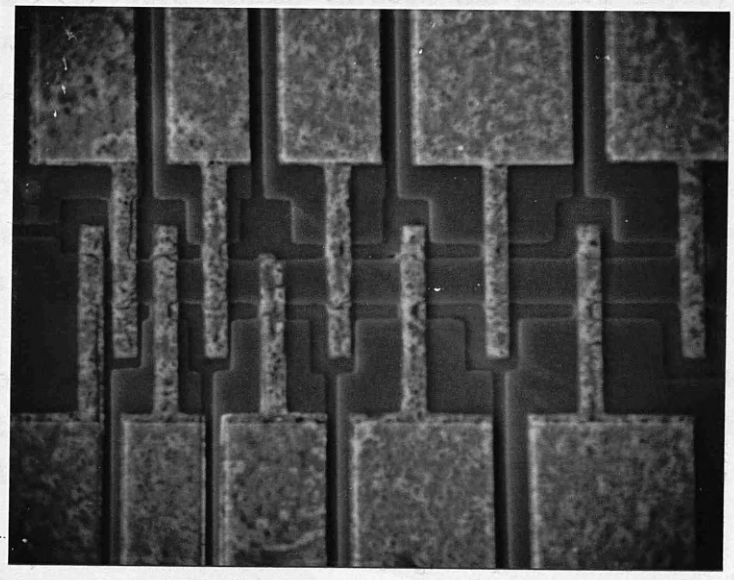


Fig. 2.2 (a) Mesa isolation and contact patterns for TLM test chips and (b) an SEM micrograph of a completed test structure.

App. 2A). The relatively large number of measurements taken from each TLM test structure means that errors involved in parameter calculations are minimised.

2.2.3 Fabrication

The TLM test structures were fabricated using electron beam lithography for pattern definition at each of three levels. Low molecular weight PMMA (185 000), 15 % by weight in chlorobenzene, was used throughout. This resist was chosen because thick uniform films (1 μm) could be spin coated onto the chips making lift-off of relatively thick (100-120 nm) metallic layers straight forward and reliable and also because it adhered well to the GaAs during the mesa etching step (Sect 1.4.2). The patterns were exposed using a 0.25 um spot size in a frame size of 1.5 by 1.2 mm. Each frame contained eight TLM test patterns and a typical chip would be patterned with 16 such frames. The resist was developed in 1:1 MIBK:IPA at 23^{o}C for 1 minute. The processes involved are similar to those employed in the device fabrication process and will be described in more detail in chapter 4.

Briefly the fabrication procedure was as follows:-

- Ohmic markers were patterned by lift-off, then annealed to produce low resistivity probing pads to be used in the mesa isolation step.

- Channels were etched through the active layer, using a resist mask, to isolate probing pads and to define the mesas between contacts.

- The ohmic contacts were defined using lift-off. The GaAs wafers were scribed and broken up into chips containing 4 TLM test structures - 2 wide and 2 narrow mesas.

- The chips were individually annealed and the measurements for contact analysis made using an HP 4145A semiconductor parameter analyser and probing system.

Some of the earlier work on ohmic contacts was done on less refined TLM structures consisiting of only 5 or even 3 contacts. However, all of the results for the final analysis of low temperature contacts to thin GaAs epi-layers were obtained from structures with 10 contacts per mesa and the final result obtained from each annealed chip was the averaged values obtained from the 4 test structures on that chip.

2.3 Annealing

All of the samples were annealed on a strip heater in a reducing atmosphere of 95:5 $Ar:H_2$. Figure 2.3 is a schematic of the annealing furnace. Before annealing the chamber was flushed out for at least 2 minutes with the reducing gas. During annealing however, the gas flow was reduced, but not cut-off altogether, so that a positive $Ar:H_2$ pressure was maintained in the chamber. This pressure was crudely monitored by observing the gas outlet through a bubbler. Annealing was carried out when the water level in the outlet tube was about 2 cm below the level of the water in the flask. The reduction in gas flow was essential to maintain a uniform temperature during the annealing.

The temperature of the strip heater, which consisted of a 2 cm wide strip of either iron or tungsten, was manually controlled using a variac to alter the current through the strip. A thermocouple, connected to a digital thermometer was used to measure the temperature of the strip. The samples, which were typically only 0.5 mm square were placed as close to the thermocouple as possible during the anneal as the temperature variation over the strip, particularly if it had been used for several weeks, was significant. If larger samples (e.g. 5 mm device chips) were being annealed the thermocouple was sometimes placed on the surface of the chip itself if a suitable position, such as a faulty exposure site, could be found.

When several samples were to be annealed at different temperatures it was often convenient to calibrate the temperature of the strip heater to the variac setting before annealing the samples. This was not a one-off procedure as the calibration varied from day to day depending on the metal and dimensions of

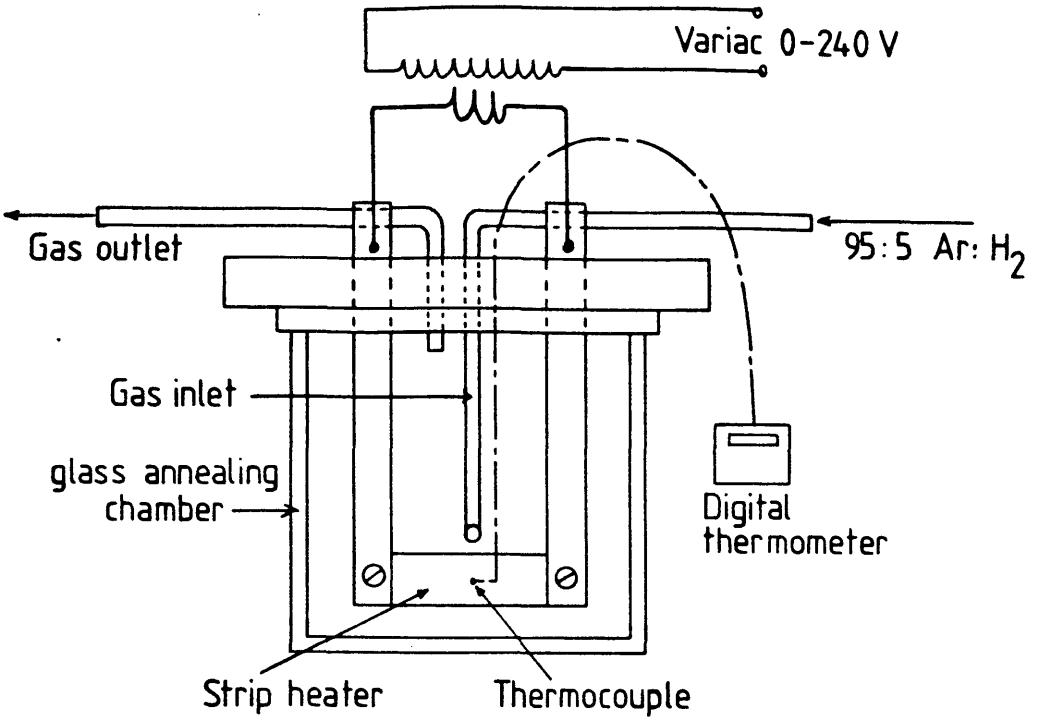


Fig. 2.3 Schematic representation of the furnace used for annealing ohmic contacts to GaAs.

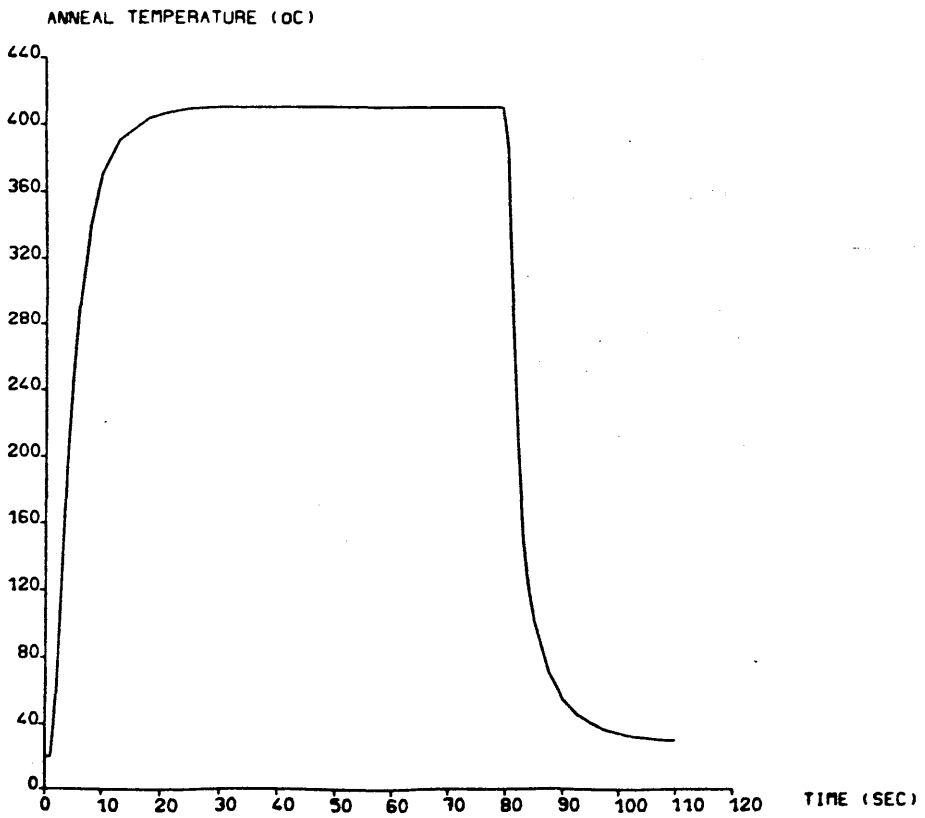


Fig. 2.4 Graph of temperature versus time for a typical 1 minute anneal cycle. The temperature rise and fall times are about 20 and 30 seconds respectively.

the strip heater as well as the positioning of the thermocouple and gas inlet pipe.

The annealing furnace has a very rapid temperature response cycle. The plot in figure 2.4 shows a typical temperature versus time curve obtained by connecting the thermocouple output to a chart recorder during a 60 second anneal. It can be seen that fast temperature rise and fall times (20 and 30 seconds respectively) could be achieved. This high heating and cooling rate is thought to be important in the production of contacts of low resistivity [2.5,2.11,2.12]. The temperature fluctuation at the peak annealing temperature could be held to +/- 5 ^{o}C without any difficulty when the gas flow was reduced as described above.

2.4 AuGe Contacts

2.4.1 Thin Epi-layer v Bulk Substrate

It was found early on in the work on ohmic contacts that the fabrication of ohmic contacts to very thin (< 100nm) n^+ GaAs epi-layers was significantly different to the fabrication of contacts to bulk GaAs substrates with similar doping levels. Initially arrays of gold germanium dots (12 % Ge by weight) 100nm thick were patterned on various substrates using photolithography and lift-off. The substrates were:-

a) 50nm MOCVD grown n^+ GaAs ($1.5.10^{18}$ /cm^3) on an AlGaAs heterostructure similar to those described in chapter 6 for membrane fabrication (grown at Sheffield University).

b) 80 nm n^+ GaAs ($2.3.10^{18}$ /cm^3) as above.

c) Bulk n^+ GaAs (10^{18} /cm^3).

After the AuGe dots were defined the samples were scribed then broken into smaller chips, each containing several dots. The chips were then annealed at temperatures in the range 200 to 400^{o}C and for durations of 0 to 18 minutes. The 0 minute anneal means that the time spent at the annealing temperature was as short as possible. In other words the sample was heated up to

annealing temperature then the current to the heater was immediately cut off.

The AuGe dots were probed and the I/V characteristics observed on a curve tracer. At this stage the contact was considered ohmic if, when a voltage was applied between two dots, the resulting I/V curve had linear characteristics in the voltage range -5 to +5 V. No attempts were made in these early experiments to analyse the contacts using TLM test srutuctures.

2.4.2 Results

The graph in figure 2.5 shows which anneal temperatures and times produced ohmic contacts to the various substrates. There is a distinct area on this graph within which all of the contacts on the epitaxial material exhibited linear I/V characteristics. This "ohmic" region extends right down to temperatures as low as 250^{o}C. It was interesting to observe that if the annealing times were too long the contacts no longer produced linear curves. For example at 320^{o}C a 1 minute anneal produced ohmic contacts to the epitaxial GaAs wafers whereas a 3 minute anneal did not. The curves obtained with longer anneal times were generally linear at the origin but there was a point of inflection at about 2 volts.

It was not understood at the time of this experiment why ohmic contacts could be obtained with a 1 minute anneal but not with a 3 minute anneal. On reflection however, it seems likely that as most of the measurements were made on GaAs/AlGaAs heterostructures, the contact material had penetrated through the active layer and into the underlying AlGaAs layer. It is therefore possibile that there was some parallel conduction through the AlGaAs layer which would lead to the inflections observed in the I/V characteristics [2.13,2.14] which resulted in the contacts being labelled non-ohmic.

This initial test did show that ohmic contacts could be formed to thin GaAs epi-layers at temperartures a lot lower than the 420 to 450 ^{o}C required for contact formation to bulk n^{+} material.

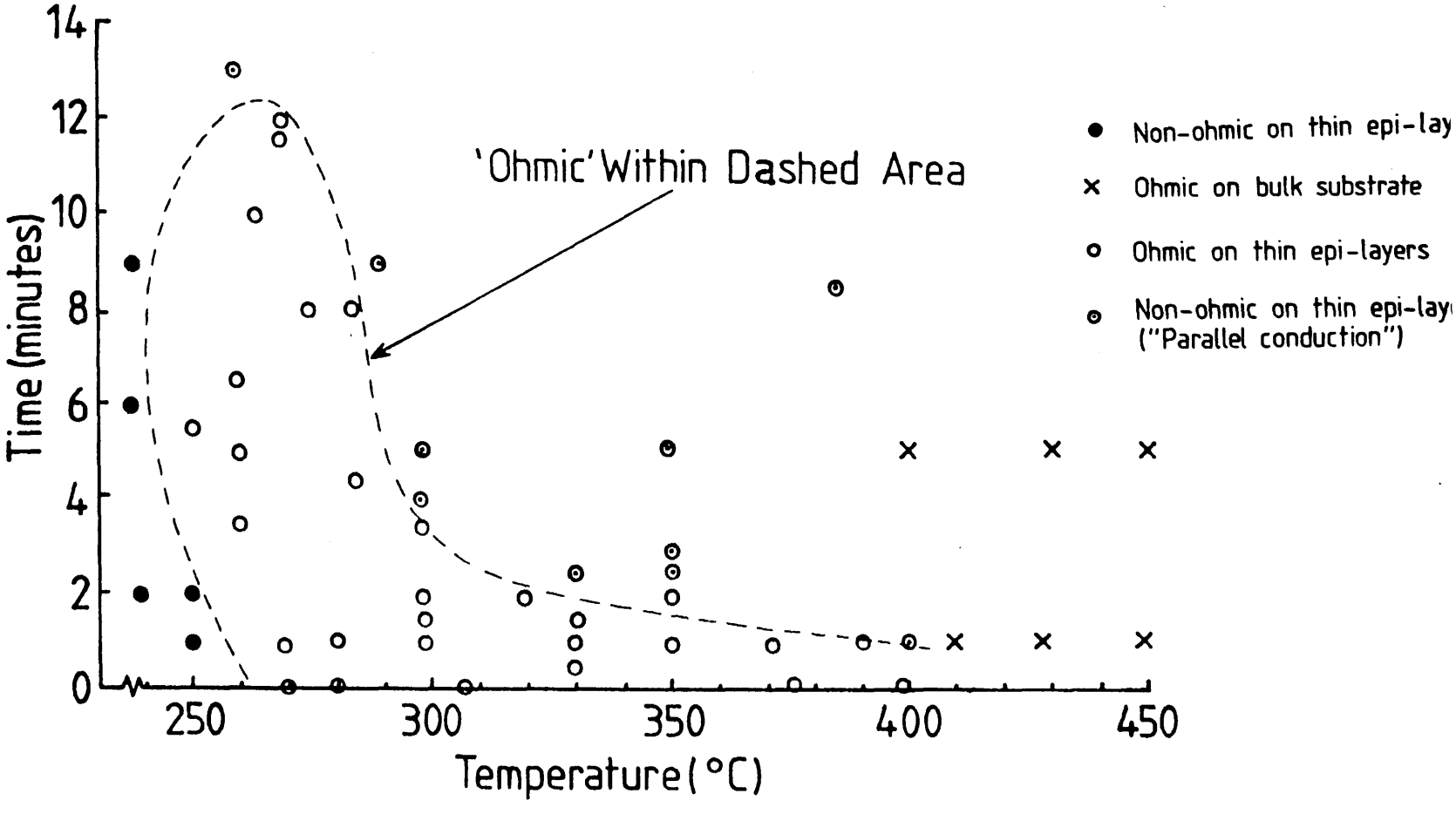


Fig 2.5 Graph showing the range of anneal times and anneal temperatures which could be used to form ohmic contacts to thin n^+ GaAs layers. In this case "ohmic" is defined as linear I/V characteristics.

2.4.3 First TLM Measurements

The first transmission line model test patterns were fabricated on 200 nm thick GaAs epi-layers ($n=1.5 \times 10^{18}$ /cm^3) with a nominally undoped buffer layer between the active layer and the semi-insulating substrate. The material was grown using vapour phase epitaxy (VPE) at Plessey (Caswell). The test pattern consisted of three identical 18 μm wide contacts patterned over a 75 μm wide mesa of active material (Fig. 2.6). The distances between the contacts were 15 and 150 μm. In this original structure, the active layer below the probing pads was removed during the mesa isolation step. The test structures were fabricated in a similar way to the ultimate TLM structure summarised in section 2.3.

The initial experiments involving the TLM were to determine how the specific contact resistance of AuGe contacts varied with anneal temperature and anneal time. Test structures were fabricated with AuGe contacts 120 nm thick. It should be noted that in the early experiments no special cleaning of the GaAs surface was carried out before contact metallisation and that no nickel was used to improve the contact resistivity [2.15].

Individual TLM test structures were annealed in the furnace described in section 2.3. After annealing the resistances between contacts were computed from the slope of the I/V curves. The contact end resistance R_e which is an essential parameter in the modified TLM was determined by both of the methods described in appendix 2A. The first of these methods was to measure the resistance between contacts 1 and 2, 2 and 3 and 1 and 3 (R_1, R_2 and R_3 respectively) then compute R_e from the equation

$$R_e = 0.5 \ (R_1 + R_2 - R_3 \ ).$$

The second method was to pass a current between contacts 1 and 2 and measure the voltage drop between contacts 2 and 3. The value of R_e was then determined by dividing the measured voltage by the input current.

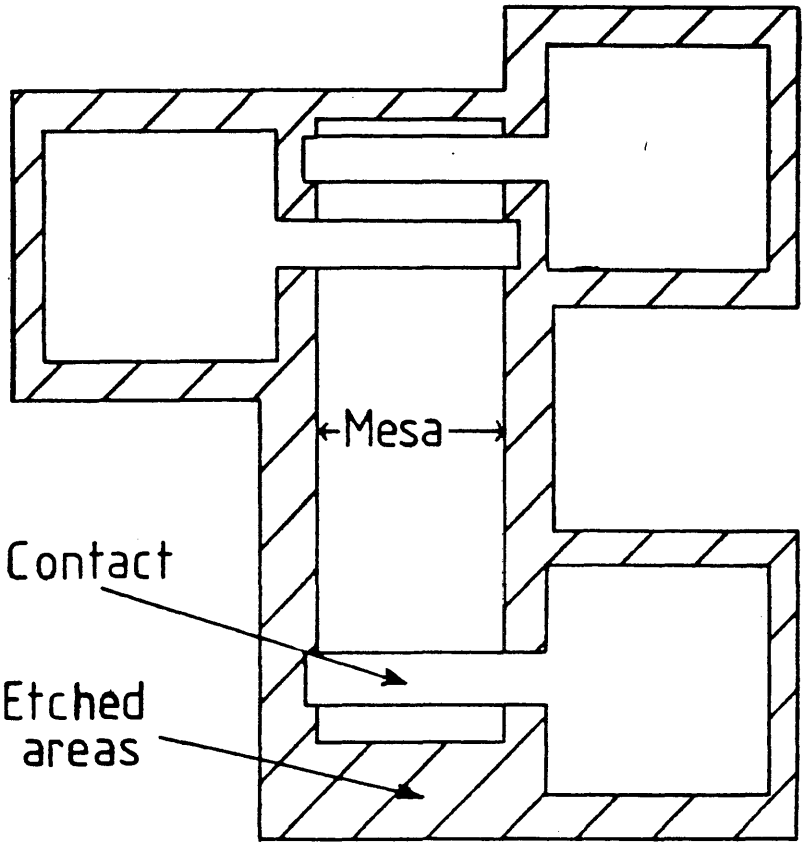


Fig 2.6 Initial TLM structure consisting of a 75 μm wide mesa with 18 μm contact stripes separated by 15 and 150 μm.

The sheet resistance of the semiconductor layer outside the contacts (R_{sh}) and the contact resistance (R_c) were determined directly from the measured resistance values and the physical dimensions of the test structure. Then, using the modified transmission line model [2.9,2.10], the specific contact resistance (ρ_c) and the sheet resistance of the semiconductor layer directly below the contact (R_{sk}) were computable using the determined values of R_e, R_c and R_{sh}. A program (RESCAL) was written to determine all the contact parameters from measured data. In this simplified test pattern only the measured resistance between contacts, the R_e value and the spacing between contacts were input to the program. With the more complex test structure described in Sect. 2.2.2, a graph of resistance between contacts v contact separation was first of all plotted. Then, after fitting the best curve to this data, two reference points could be taken from the curve and input to RESCAL along with an average value of R_e determined from up to eight measurements per sample.

2.4.4 Specific Contact Resistance v Anneal Temperature

Table 2.1 contains the measured and computed results from samples annealed at different temperatures (60 seconds). The R_e values were determined using both of the methods described above. It can be seen that the sheet resistance of the semiconductor layer outside the contact (R_{sh}) is constant over the entire temperature range studied. The sheet resistance under the contact (R_{sk}) does however vary with the anneal temperature. Broadly speaking, the lower the value of specific contact resistance obtained (ρ_c), the lower the value of R_{sk}. The fluctuations in R_{sk} are due to errors in the measured value of R_e. This is the main reason why the simple test structure of this experiment, where only one R_e measurement can be made, was subsequently replaced by the complex test structure (Sect. 2.2.2) where up to 8 measurements of R_e can be made.

In this experiment the lower values of ρ_c (10^{-4} ohm.cm^2) were obtained at higher annealing temperatures (Fig. 2.7). The reduction in sheet resistance below the contact is caused by the reactions which take place during annealing. It is likely that

Table 2.1

T	R_1	R_2	R_3	R_e	R_{sh}	R_c	ρ_c	R_{sk}
280	140	380	430	45.0	133	56.6	6.6	101.0
				*42.0			6.3	129.0
300	65	285	314	18.0	122	20.3	2.5	19.4
				*16.0			2.3	37.2
325	64	280	314	14.5	120	20.0	2.2	48.5
				*11.0			1.9	83.8
350	50	280	307	11.5	128	12.2	1.6	6.0
				*11.5			1.6	6.0
380	50	282	312	10.0	129	12.1	1.4	18.2
				* 9.5			1.4	22.7
400	46	265	291	10.0	121	10.8	1.4	7.0
				* 9.5			1.3	11.4
425	50	270	300	10.0	122	12.8	1.5	24.2
				*10.0			1.5	24.2

T is in ^{o}C, R_1, R_2, R_3, R_e and R_c are in ohms
R_{sh} and R_{sk} are in ohms/square ρ_c is in ohm.cm^2 $x10^{-4}$
* indicates R_e measured using V/I method.

at higher temperatures more Ge will have diffused from the contact into the underlying semiconductor increasing the doping level by more than an order of magnitude [2.9,2.10], hence, the reduction in sheet resistance.

This lowering in sheet resistance below the contact illustrates why the standard TLM model gives lower values for the specific contact resistance than the modified TLM. In order to get contact resistances of the order of 10^{-5} ohm.cm^2 the GaAs doping level should be around 5.10^{19} /cm^3 [2.6]. In the case of contacts to thin epi-layers, as already discussed, it is likely that the whole of the semiconductor layer will be modified during contact annealing (lower sheet resistance). If the layer below the contact is not assumed to be modified, then, in order to satisfy the measurements made on the TLM test structure, the calculated values of specific contact resistance would appear to be smaller than they actually were.

2.4.5 Specific Contact Resistance v Anneal Time

A second experiment was carried out to find out how the specific contact resistance of the AuGe contacts varied with anneal time. A set of TLM samples, fabricated in the same way as those in the previous test, were annealed for different times at 350 ^{o}C. The graph of fig. 2.8 shows that ρ_c is in fact more or less constant for anneal times from 0 (instantaneous anneal) up to 18 minutes. The inflections observed in the I/V curves of the samples fabricated on GaAs/AlGaAs heterostructures with longer anneal times were not present in this test on 200nm n^+ epi layers on undoped buffers. This confirmed that the inflections observed previously were due to parallel conduction through the AlGaAs layer and not to a deterioration in the contact quality.

In all subsequent experiments the anneal time was chosen to be 1 minute since there was no obvious advantage in annealing the samples for any longer. 1 minute was selected in preference to say 15 seconds to allow the completion of the reactions which take place during annealing. It was speculated by Ogawa [6.5] that contacts formed at low temperature would deteriorate with time because the reactions would be incomplete. However, the

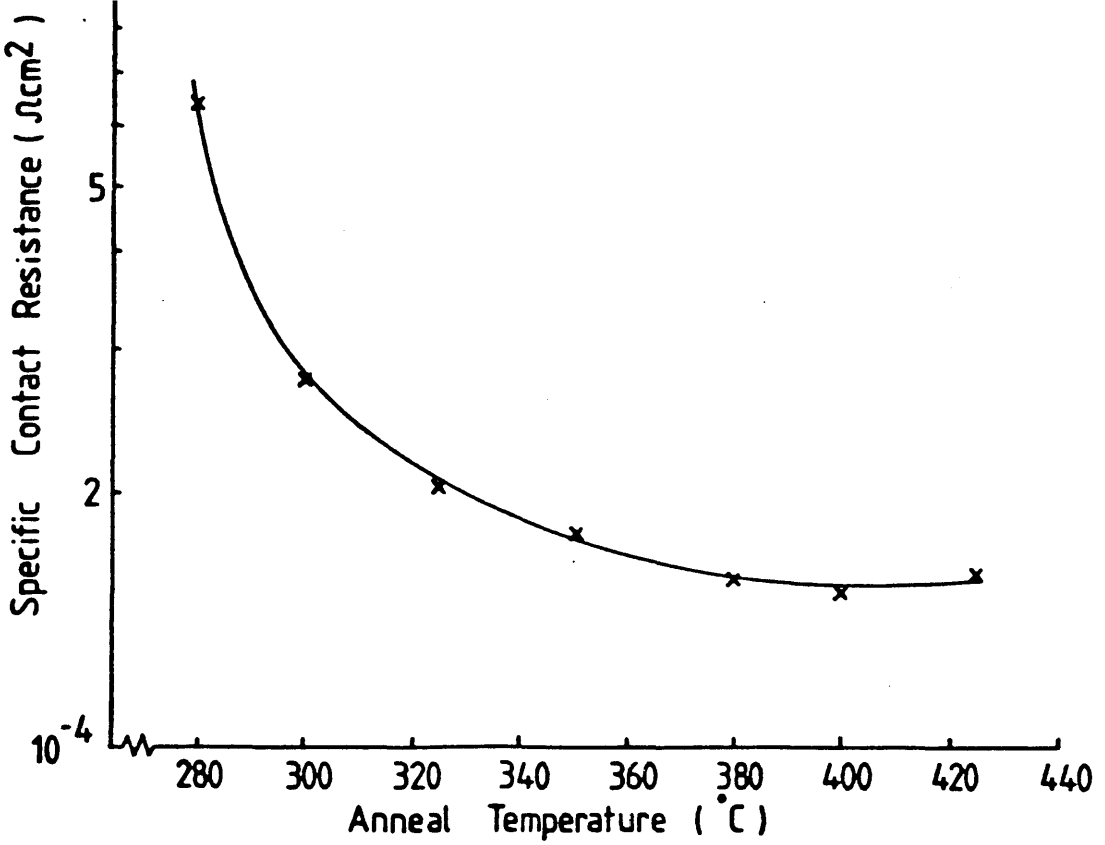


Fig 2.7 Specific contact resistance versus annealing temperature for AuGe contacts to 200 nm 10^{18} GaAs. The anneal time was 60 seconds for each sample.

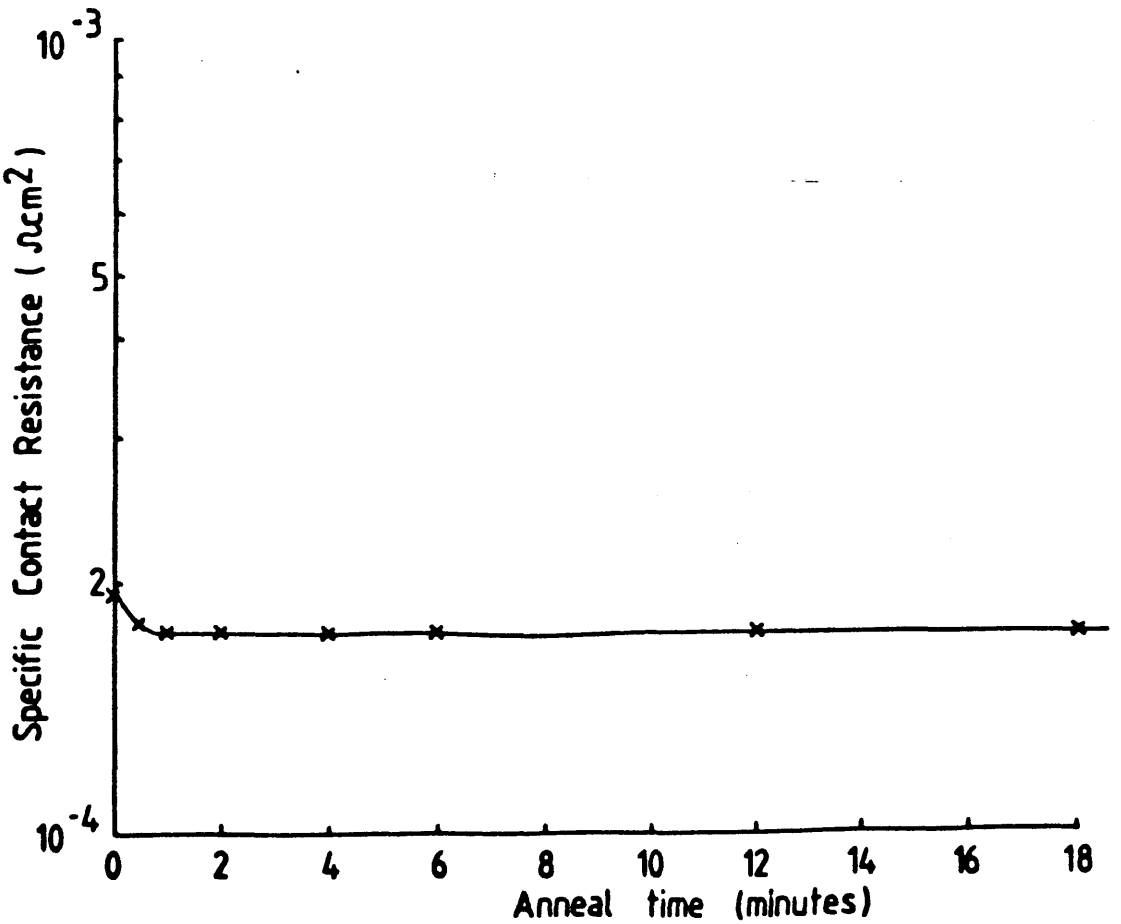


Fig 2.8 Specific contact resistance versus anneal time for AuGe contacts annealed at 350 °C.

results of this experiment indicate that the reactions are completed in a few seconds since there is no improvement in resistivity when longer anneal times are used. In later work on AuGe contacts with Ni and Au capping layers, low temperature contacts annealed for 1 minute were remeasured some 8 weeks after they were first tested and it was found that there had been no deterioration of the contacts in this time.

2.5 AuGe/Ni/Au Contacts

The minimum values of specific contact resistance (10^{-4} ohm.cm^2) obtained in these initial experiments was high compared with other reported values on similarly doped material measured using the modified TLM [2.9,2.10]. To improve the resistivity a nickel layer was incorporated into the contacts since the nickel improves wetting and enhances the solubility of the GaAs. Nickel does have the disadvantage that it is a fast diffuser and a compensating acceptor [2.15,2.16]. A gold capping layer typically 20 nm thick was also added to reduce the sheet resistance of the metal contact.

It was also found that cleaning the GaAs immediately before the contact metallisation improved the resistivity of the contacts. A 60 second clean in 5 % ammonia solution prior to metal evaporation reduced ρ_c by about a factor of five and also improved the adhesion of the contacts to the GaAs. It is believed that the ammonia solution etches away any surface oxide, thus improving the contact resistance.

2.5.1 Low Temperature Annealing

The initial results from contacts including nickel showed that low resistivity contacts could be formed with annealing temperatures in the range 300 - 320 ^{o}C (Sect. 2.5.3). Further experiments were therefore carried out to see if the composition of the AuGe/Ni/(Au) contacts could be optimised for low temperature annealing (Sect. 2.5.4,5). Ultimately contacts with ρ_c around 10^{-5} ohm.cm^2 were obtained with an anneal temperature of 300 ^{o}C.

2.5.2 Test Structures

Experiments were carried out to study what effect the nickel concentration had in AuGe/Ni/Au contacts to thin GaAs epi-layers and to determine if a suitable composition could be found for low temperature annealing. The TLM structures described in Sect. 2.2.2 (fig 2.2), consisting of 10 contacts on mesas 14 and 20 μm wide, were fabricated on material consisting of an 85nm n^+ GaAs ($n=10^{18}/cm^3$) active layer and a 1 μm nominally undoped buffer layer grown by VPE on a semi-insulating substrate. Initially a 4 X 5.2 mm chip was patterned with 9 exposures, each containing 8 TLM patterns. The frame size for each exposure was 1.2 X 1.5 mm. When the chip was completely processed, including mesa isolation and ohmic metallisation, the chip was scribed and broken into 1 X 0.5 mm samples, each with 4 test structures, for individual annealing.

Immediately before loading the samples into the vacuum system for contact metallisation, the GaAs surface was cleaned by immersing the samples in 5 % ammonia solution. The samples were then rinsed in de-ionised water and thoroughly blown dry in a stream of nitrogen.

2.5.3 Varying The Nickel Concentration

The first test was to determine what effect the nickel concentration in the composite metal contacts had on the annealed contacts. TLM structures were fabricated which were metallised with 92nm AuGe / X nm Ni / 20 nm Au, where X (the nickel thicknesses) were 12, 25 and 35 nm. The percentages of nickel to AuGe by weight were 6.4, 12.3 and 17.5 % respectively. A standard composition for annealing contacts at high temperatures consists of 100 nm AuGe (88:12) with approximately 5 % Ni by weight and an Au capping layer to reduce the sheet resistance of the contact metal [2.15]. The samples were annealed at temperatures in the range 250 - 425 ^oC. To limit the number of variables, and since the alloying process was shown to be almost independent of annealing time (sect 2.4.5), all the samples were annealed for 1 minute. After annealing resistance values were measured from the test chips and the average value of specific

contact resistance computed from the 4 test patterns on each of the samples.

Fig. 2.9 contains a graph of specific contact resistance versus anneal temperature for contacts with each of the three nickel concentrations. Curve 1 was plotted for contacts containing 6.4 % Ni (Ni to AuGe by weight) and shows a minimum value of 2.10^{-5} ohm.cm^2 when the annealing temperature was 420^{o}C. This is a standard temperature for contact formation to bulk GaAs [2.15] which is reasonable since the composition of the contacts of curve 1 was close to the standard.

Curve 2 however (12.3 % Ni), shows a minimum in specific contact resistance, similar in value to the minimum of curve 1 (2.10^{-5} ohm.cm^2) at an annealing temperature of 320 ^{o}C. Specific contact resistances in the order of 2.10^{-5}ohm.cm^2 were also obtained from some of the contacts containing 17.5 % Ni (curve 3) annealed at temperatures as low as 250 ^{o}C. Unfortunately, the number of low resistivity contacts formed at these very low temperatures was less than the number of contacts with extremely high resistivities.

The curves in fig. 2.9 show that the annealing temperature of AuGe/Ni/Au contacts can be reduced by over 100 ^{o}C by increasing the proportion of nickel in the composition. The specific contact resistances obtained in the contacts with a high proportion of nickel annealed at 300 - 320 ^{o}C were as low as were achieved using a contact of standard composition annealed at 420 ^{o}C. However, when the anneal temperatures are too low (250-300^{o}C), low resistivity contacts cannot be made reliably even if the nickel concentration is increased further. Therefore, an annealing temperature of 300 - 320 ^{o}C was considered to be the lowest practical temperature for contact formation.

2.5.4 Optimum AuGe Thickness

A second set of experiments was carried out to find out if there is an optimum AuGe thickness which would give low resistivity contacts when annealed at low temperatures. TLM test structures were fabricated on the same material as the previous

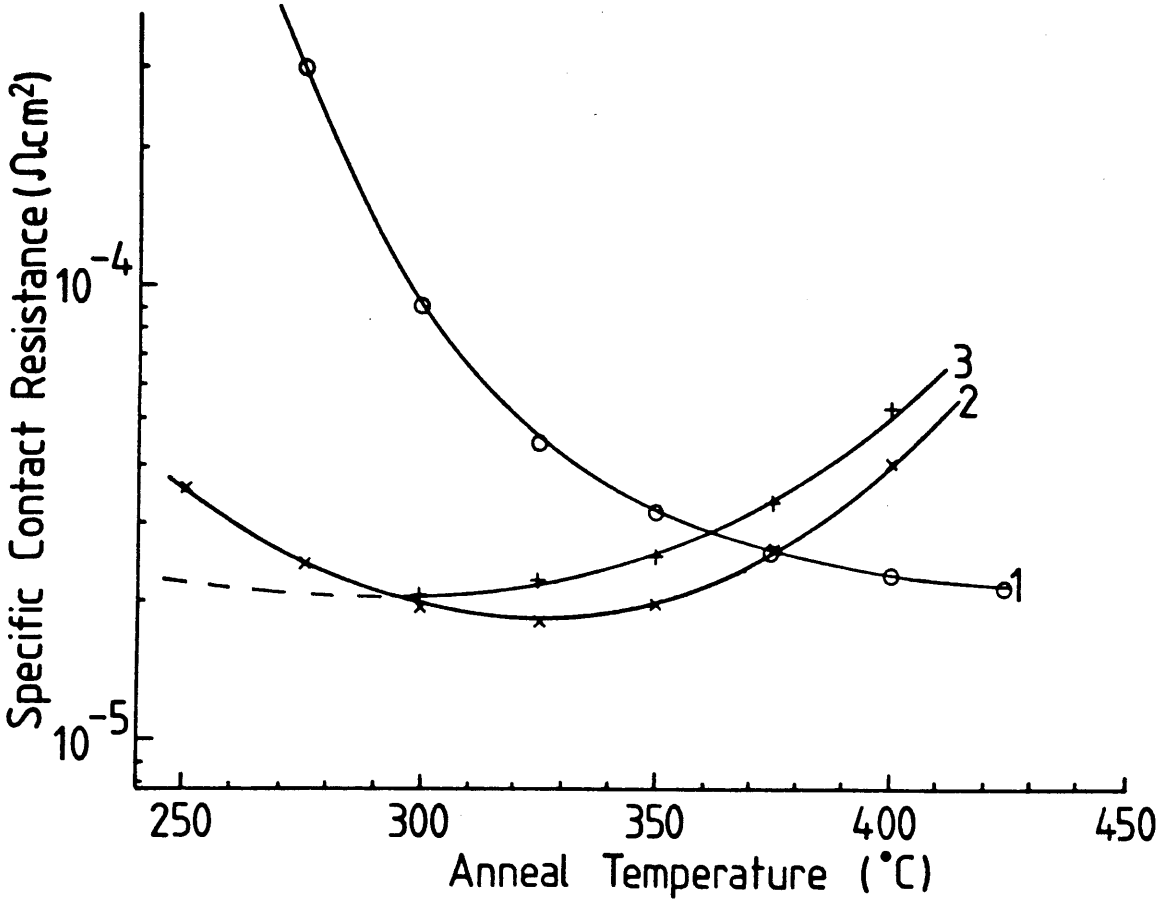


Fig 2.9 Specific contact resistance versus anneal temperature for contacts with the following compositions:-

Curve 1 92 nm AuGe (88:12), 12 nm Ni (6.4% by weight), 20 nm Au.

Curve 2 " " " 25 nm Ni 12.3% " " "

Curve 3 " " " 35 nm Ni 17.5% " " "

test chips. Four different AuGe thicknesses were used in the metallisation of the contacts: 30, 63 75 and 85 nm. To complete the metallisation, a nickel layer equivalent to 10 % of the AuGe thickness (4.5 % weight) and a gold capping layer 20 nm thick were evaporated. Annealing was once again carried out on individual 0.5 x 1 mm chips containing 4 TLM patterns.

The graph of fig. 2.10 shows the specific contact resistances obtained from each of these samples annealed at temperatures from 300 to 400 ^{o}C. From this graph it can be seen that curve 3 with 75 nm of AuGe has the lowest specific contact resistance (minimum 1.4 X 10^{-5} ohm.cm^{2}) over the temperature range studied. The minimum value of specific contact resistance was not significantly lower than any previously obtained values. Extrapolation of curve 4 (85 nm) suggests that this composition may produce lower contact resistances when annealed at temperature greater than 400 ^{o}C. Nevertheless, the optimum AuGe thickness for low temperature annealing of ohmic contacts to thin n^{+} GaAs epi-layers was taken to be 75 nm.

It was interesting to find that when the AuGe layer was thin, as was the case with the contacts of curve 1 in fig 2.9 (30 nm AuGe), the contact resistivity became very large when anneal temperatures greater than 370 ^{o}C were used. It is speculated that the reason for this is that most of the contact metal has diffused into the semiconductor leaving only a thin, uneven film on the surface. The thin metallic layer would have a very high sheet resistance which would result in the high resistance values measured on these samples. Perhaps if another gold layer was patterned over the contacts after annealing, to reduce the sheet resistance, lower resistivities might have been recorded. However, it seemed unlikely that such a procedure would produce contacts with lower resistivities than could be obtained with a thicker AuGe layer. The high resistance values observed in the thin contacts were not seen in the thicker contacts except for a few of the samples with 63 nm Au annealed at 400 ^{o}C. This was presumably because the sheet resistance associated with the metal layer in the thicker contacts was negligible. These observations are consistant with those reported by Dell et al [2.19] where 60 nm was determined to be the minimum total contact thickness for

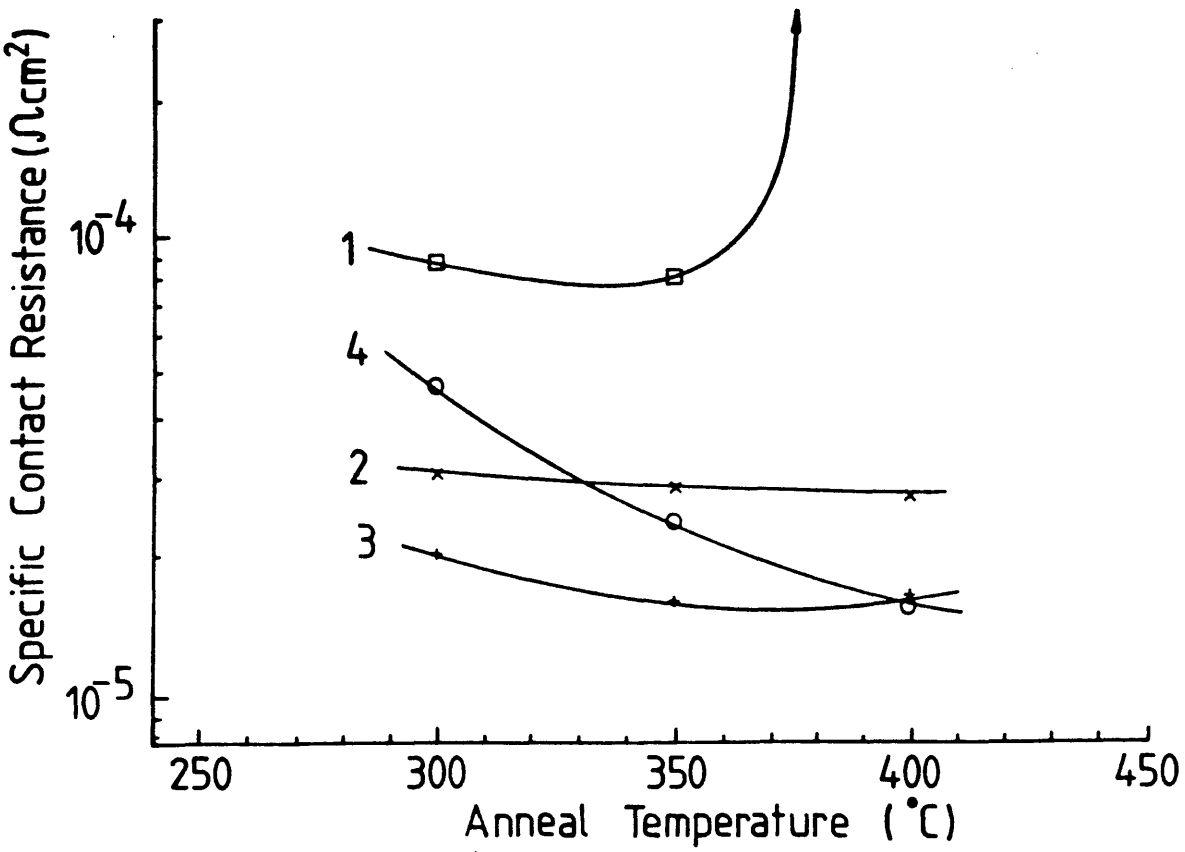


Fig 2.10 Specific contact resistance versus anneal temperature for contacts with different AuGe thicknesses:-

Curve 1 30 nm AuGe (88:12), 3 nm Ni (4.5% by weight), 20 nm Au.

Curve 2 63 nm " " 6.3 " " " " "

Curve 3 75 nm " " 7.5 " " " " "

Curve 4 85 nm " " 8.5 " " " " "

reasonable contact formation.

2.5.5 Varying Ni Concentration On Optimum AuGe Layer

A further experiment was carried out using the optimum thickness of AuGe (75 nm) and nickel thicknesses of 11 nm (6.8 % by weight) and 18 nm (11.2 % wt.). A 20 nm gold capping layer was included as in the previous studies.

Fig 2.11 is a graph of specific contact resistance versus annealing temperature for contacts of the above compositions. Also included are the results from the 75 nm AuGe contacts with 4.5 % Ni from the previous experiment. Minimum contact resistances (1.5×10^{-5} ohm.cm^2) were obtained either from the contacts containing 4.5 % Ni annealed at 400 ^{o}C or from those with 6.8 % Ni annealed at about 320 ^{o}C. It was also found that similar resistivity values were obtained from the 11.2 % Ni samples annealed at temperatures as low as 270 ^{o}C. However, as was found in the experiments described in section 2.5.3, the reliability of the contacts formed at this temperature was low.

The results from this experiment were similar to the results obtained from the initial experiment where nickel was included in the contact composition (sect. 2.5.3). The main difference between the two experiments was the AuGe thicknesses used - 75 nm in this case and 92 nm previously. When the optimum AuGe thickness (75 nm) was used the contacts containing 6.8 % Ni produced the lowest specific contact resistances when annealed at 320 ^{o}C. However, when a 92 nm AuGe layer was used, the percentage of nickel required to produce good contacts at this temperature was 12.3 %.

2.6 Discussion

From the results of the annealing experiments described above (Sect. 2.5.3 to 2.5.5) it is clear that the proportion of nickel required to produce low resistivity contacts when annealed at low temperatures, is dependent on the thickness of the AuGe layer. In a standard contact (about 100 nm AuGe) 5 % Ni is included in the contact for annealing at typically 450 ^{o}C. It

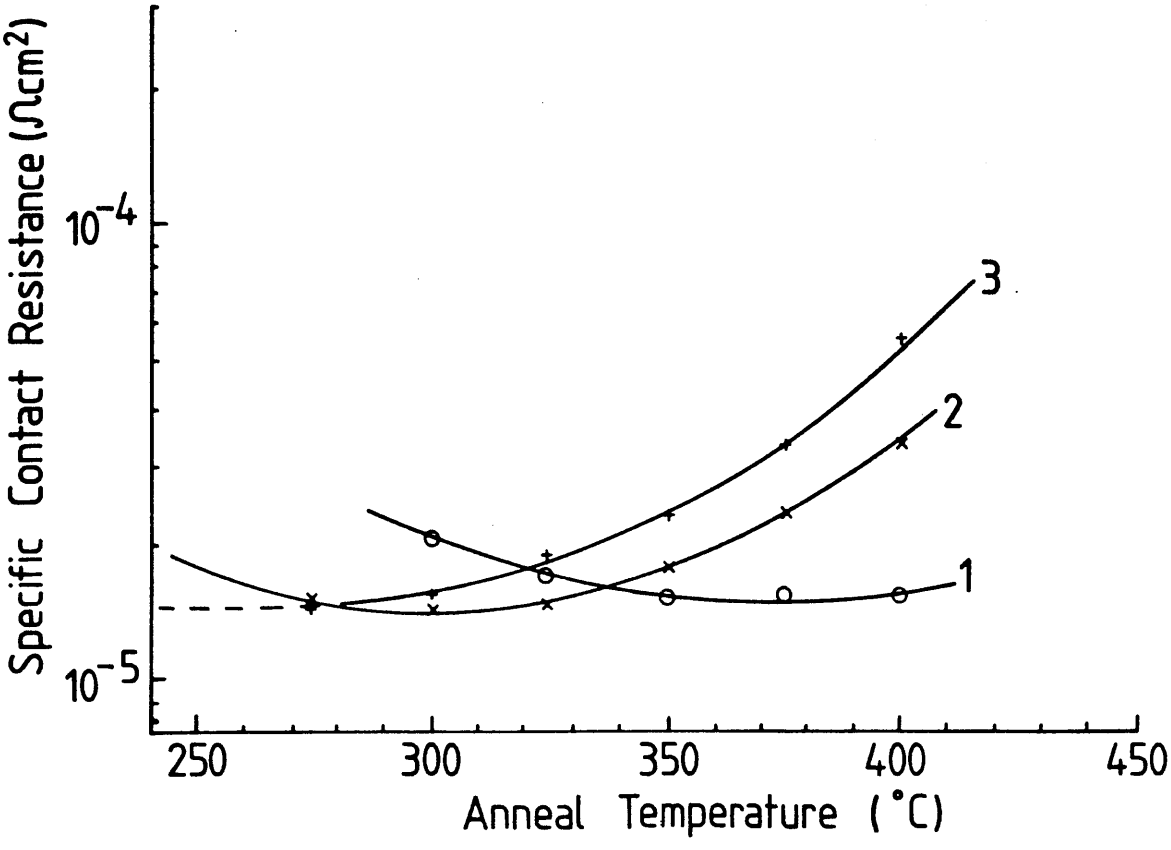


Fig 2.11 Specific contact resistance versus anneal temperature for contacts with the optimum AuGe thickness and 3 different percentages of Ni:-

Curve 1 75 nm AuGe (88:12), 7.5 nm Ni (4.5% by weight), 20 nm Au.
Curve 2 " " " 11 " 6.8% " " "
Curve 3 " " " 18 " 11.2% " " "

has been shown that contacts with approximately this composition are not suitable for low temperature annealing. If needs demand a thick low temperature annealed contact, then the percentage of nickel in the contact has to be increased (12.3 % for a 92 nm AuGe layer). However, if the optimised AuGe thickness is used (75 nm) the proportion of nickel required for low temperature annealing is reduced to 6.8 %.

The choice of which contact composition to use in device fabrication depends on many factors. In standard GaAs MESFETs with source-drain gaps of the order of 2 - 3 μm there was no particular need for low temperature annealing except that better contrast could be obtained in the SEM for alignment purposes. For this reason the typical device ohmic contact metallisation (source drain pads) consisted of about 85 nm AuGe with around 9 % (weight) of Ni and a gold capping layer 20 - 30 nm thick. An anneal temperature of 350 ^{o}C was found by experiment to produce the minimum specific contact resistance for this composition.

In devices with very short source-drain gaps (0.5 μm), and devices fabricated on thin (50nm) GaAs membranes however low temperature annealing is essential to prevent lateral spreading of the contact into the active drain source channels. It was shown by others working in this Department that a direct short is obtained across a 0.3 μm gap on solid substrates when a standard contact was annealed at 400 ^{o}C [2.20]. However, no visible short circuits were obtained when contacts with a composition suitable for low temperature formation, were annealed at 325 ^{o}C. In addition, the Auger Analysis of contacts formed on solid GaAs substrates and the Energy Dispersive Energy Microanalysis of contacts on thin GaAs membranes, described in the following chapter, both indicate that the diffusion of the contact material into the semiconductor is significantly reduced when the contacts are annealed at low temperature (300 ^{o}C).

Appendix 2A Contact Analysis Using The Transmission Line Model

In this appendix a description of the transmission line model of planar contacts, developed by Murrmann and Widmann [2.7] and Berger [2.8], is given. From this model the contact resistance R_c, specific contact resistance ρ_c and the sheet resistance of the semiconductor R_{sh} can be deduced from simple resistance measurements made between contacts on a TLM test structure. The modified TLM [2.9, 2.10] in which a different value is obtained for the semiconductor sheet resistance directly below the contact (R_{sk}) is also described.

In Fig. 2A.1 a cross section of a contact to a thin semiconductor layer is compared with a transmission line section. In this case R_{sh} is assumed to be the same as R_{sk}.

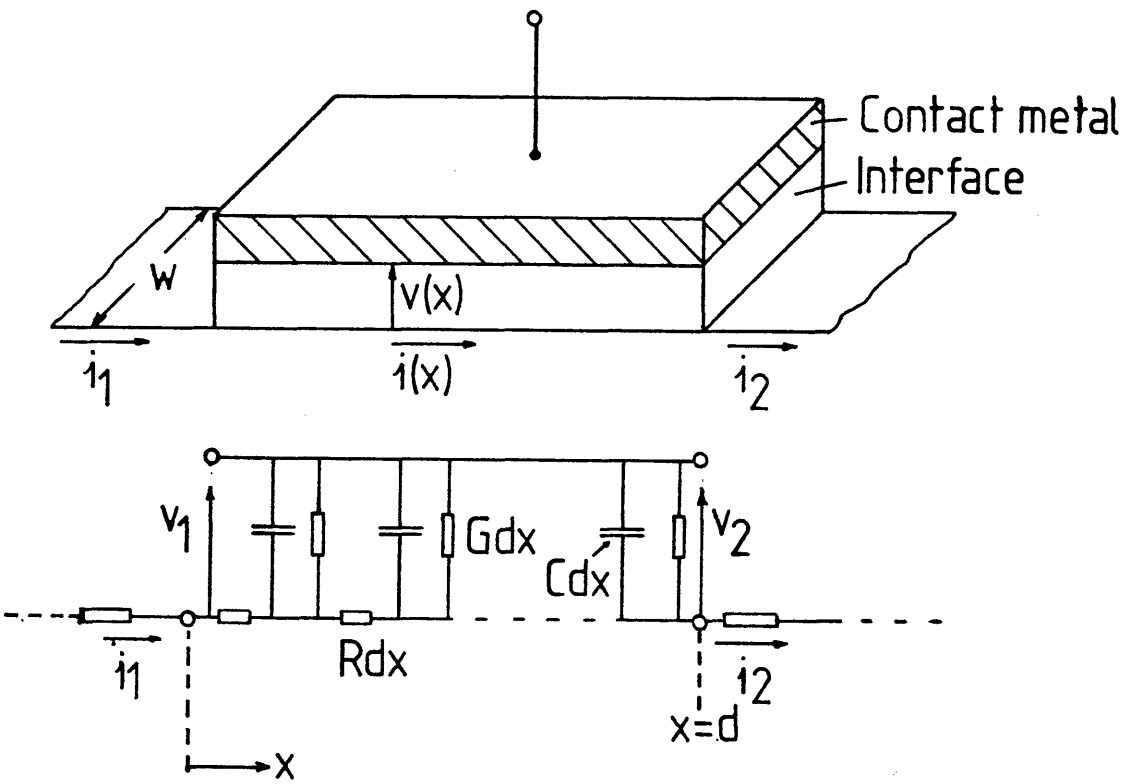


Fig. 2A.1 Comparison of the metal-semiconductor contact region with a transmission line section.

R - Line resistance per unit length corresponding to the semiconductor layer resistance.

G - Shunt line conductance per unit length corresponding to the interface resistance.

C - Shunt capacitance per unit length included for ac operation.

The return lead of the transmission line corresponds to the metal layer of the contact.

Comparing the transmission line with the contact cross section the following primary line parameters can be written:-

$$R = \frac{R_{sh}}{w} \tag{1}$$

$$G = \frac{w}{\rho_c} + j\omega w C^* \tag{2}$$

where C^* is the capacitance per unit area and ρ_c is the specific contact resistance defined as the voltage across the interface layer divided by the current density.

The secondary line parameters known as the characteristic impedence, Z, and the propagation constant, γ, are,

$$Z = \sqrt{\frac{R}{G}} = \frac{1}{w}\sqrt{(R_{sh}\rho_c)} \cdot \frac{1}{\sqrt{(1 + j\omega C^*\rho_c)}} \tag{3}$$

$$\gamma = \alpha + j\beta = \sqrt{(RG)} = \sqrt{\frac{R_{sh}}{\rho_c}}\sqrt{(1 + j\omega C^*\rho_c)} \tag{4}$$

The dc values are,

$$Z = \frac{\sqrt{(R_{sh}\rho_c)}}{w} \tag{5}$$

$$= \sqrt{\frac{R_{sh}}{\rho_c}} \tag{6}$$

The well known line equations then describe the current and voltage distribution along the contact. For the most important

dc case these equations are,

$$V(x) = V_1 \cosh(\alpha x) - I_1 . Z \sinh(\alpha x) \quad (7)$$

$$I(x) = I_1 \cosh(\alpha x) - (I_1/Z) \sinh(\alpha x) \quad (8)$$

where x is the distance from the leading contact edge.

TLM Test Pattern for Planar Contact Analysis.

The TLM test structure for contact analysis consists of three or more contacts of identical geometry patterned on a strip of active material (Fig. 2A.2a)). The resistance measurements are made between adjacent contacts and plotted as a function of L, the separation between contacts (fig. 2A.2b). The resistance measurement indicated by R_3 in the diagram is used to determine the contact end resistance described later.

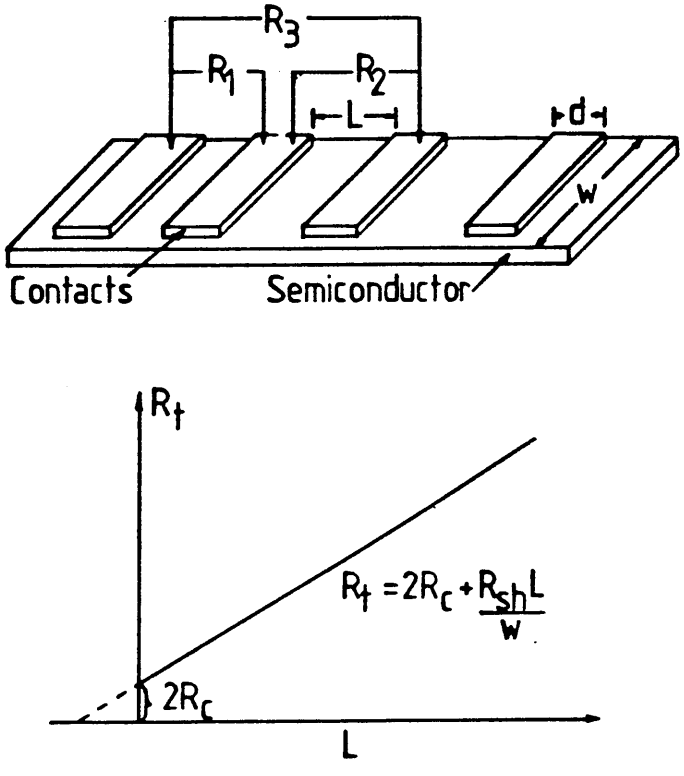


Fig. 2A.2 Schematic representation of the measurements made on a transmission line test structure. a) is the test structure itself while b) is a graph of R_t versus L obtained from the resistance measurements.

From the resulting R_t v L graph the sheet resistance of the semiconductor can be determined from the slope of the curve.

Also, extrapolation of the curve to L=0 gives a direct measurement of the contact resistance R_c since, at L=0, there is no contribution to the total resistance between contacts from the sheet resistance of the semiconductor.

In the transmission line model of the contact, R_c is equivalent to the input resistance of the two port network (fig. 2A.1). Therefore, with I2 = I(d) = 0 and using equation (8),

$$R_c = \left.\frac{V_1}{I_1}\right|_{I_2=0} = Z\coth(\propto d) \qquad (9)$$

Hence, with increasing contact length d, the contact resistance approaches asymptotically to Z and for $d > 2.0$, R_c can be taken to be equal to Z.

Before a complete analysis of the contacts can be made, the contact end resistance, defined as the voltage drop $V_2 = V(d)$ at the end of the contact divided by the input current I_1 with $I_2 = 0$, has to be determined. This can be achieved in two ways:

a) A current can be passed between two contacts (I_1) and then the potential between the semiconductor and contact metal (V(d)) measured, using an adjacent contact to probe the potential of the semiconductor.

b) The resistance between two adjacent pairs of contacts can be measured (R1 and R2 fig. 2A.2a)) and then the resistance between the two outer contacts can also be measured (R_3). The contact end resistance is given as [2.10],

$$R_e = 0.5(R_1 + R_2 - R_3) \qquad (10)$$

Using equations (7), (8) and (9) and the definition

$$R_e = \left.\frac{V_2}{I_1}\right|_{I_2=0}, \qquad (11)$$

$$R_e = \frac{Z}{\sinh(\alpha d)} \tag{12}$$

Therefore, once R_c and R_e have been determined experimentally, it is then possible to evaluate the specific contact resistance of the contacts. Using (9) and (12),

$$\frac{R_c}{R_e} = \cosh(\alpha d) \tag{13}$$

from which the value of ρ_c can be calculated. Equation (6) gives

$$\rho_c = \frac{R_{sh}}{\alpha^2} \tag{14}$$

Modification to the transmission Line Model.

The model described so far assumes that the sheet resitance of the semiconductor below the contact is the same as the sheet resistance outside the contact (R_{sh}). This assumption is not realistic for contacts to the very thin epi-layers analysed in the course of this work since the alloyed depth of the contacts is likely to exceed the active-layer thickness. Therefore the modified TLM is used [2.9, 2.10]. If the sheet resistance below the contact is denoted by R_{sk}, then Z and α become

$$Z = \frac{\sqrt{(R_{sk}\rho_c)}}{W} \tag{15}$$

$$\alpha = \sqrt{\frac{R_{sk}}{\rho_c}} \tag{16}$$

R_{sh}, R_c and R_e can be determined as before. Z is calculated from (9) or (12) and α is determined using (13). Then, using (15) and (16) ρ_c and R_{sk} can be evaluated.

Thus, the modified TLM gives a fuller analysis of the planar ohmic contacts since the actual sheet resistance below the contacts is calculated. Experimental results have shown that R_{sk} is often more than an order of magnitude less than R_{sh}.

Chapter 2 References

[2.1] V.L. Rideout, "A Review of the Theory and Technology for Ohmic Contacts to Group III-V Compound Semiconductors," Solid State Electronics **18**, 541-550 (1975).

[2.2] "Physics of Semiconductor Devices," 2nd Ed. S.M. Sze, Wiley, New York, 1981, Sect 5.7.

[2.3] Ref 2.2 p291.

[2.4] B.R. Pruniaux, "Transport Properties of the Gold Germanium Gallium Arsenide Metal Semiconductor System," J. App Phys **42**, 3575-3577 (1971).

[2.5] M. Ogawa, "Alloying Behaviour of Ni/AuGe Films on GaAs," J. Appl. Phys. **51**, 406-412 (1980).

[2.6] C.Y. Chang, Y.K. Fang, S.M. Sze, "Specific Contact Resistance of Metal-Semiconductor Barriers," Solid State Electronics **14**, 541-550 (1971).

[2.7] H. Murrmann, D. Widmann, "Messung des Ubergangswiderstandes zwischen Metall und Diffusionsschicht in Si-Planarelementen," Solid State Electronics **12**, 879-876 (1969).

[2.8] H.H. Berger, "Models for Contacts to Planar Devices," Solid State Electronics **15**, 145-158 (1972).

[2.9] W. Kellner, "Planar Ohmic Contacts to N-Type GaAs: Determination of Contact Parameters Using the Transmission Line Model," Siemens Forsch. -u. Entwickl-Ber, **4**, 137-140 (1975).

[2.10] G.K. Reeves, H.B. Harrison, "Obtaining the Specific Contact Resistance from Transmission Line Model Measurements," IEEE Electron Device Lett. **EDL-3**, 111-113 (1982).

[2.11] H.G. Henry, D.E. Dawson, Z.J. Lemnois, H. Kim, "Hot-Plate Alloying for Ohmic Contacts to GaAs," IEEE Trans. Electron Devices, **ED-31**, 1100-1103 (1984).

[2.12] M.I. Nathan, M. Heiblum, "Novel Ohmic Contacts to N-Type GaAs," IEEE Trans. Electron Devices **ED-29** 1691 (1982).

[2.13] M. Keever, T.J. Drummond, H. Morckoc, K. Hess, B.G. Streetman, "Hall Effect and Mobility in Heterojunction Layers," J. Appl. Phys. **53**, 1034-1036 (1982).

[2.14] EF Schubert, K Ploog, H Dambkes, K Heime, "Selectively Doped n-AlGaAs/GaAs Heterostructures with High-Mobility Two-Dimensional Electron Gas for Field Effect Transistors. Part 1 Effect of Parallel Conductance," App. Phys. A **33** p63-76 (1984)

[2.15] N. Braslau, "Ohmic Contacts to GaAs," Thin Solid Films, **104**, 803-807 (1981).

[2.16] N. Braslau, "Alloyed Ohmic Contacts to GaAs," J. Vac. Sci. Tech. **19**, 391-397 (1981).

[2.17] A. Iliadis, K.E. Singer, "The Role of Germanium in Evaporated Au-Ge Ohmic contacts to GaAs," Solid State Electronics **26**, 7-14 (1983).

[2.18] A. Iliadis, K.E. Singer, "Metallurgical Behaviour of Ni/Au-Ge Ohmic Contacts to GaAs," Solid State Comm. **49** 99-101 (1984).

[2.19] J. Dell, H.L. Hartnagel, A.G. Nassibian, "Ultrathin-film Ohmic Contacts for GaAs FET," J. Phys. D:Appl. Phys. **16**, L243-L245 (1983).

[2.20] C. Black, Private Communication (Summer Student 1985).

CHAPTER 3 AUGER AND ENERGY DISPERSIVE X-RAY MICROANALYSIS OF ANNEALED OHMIC CONTACTS

3.1 Introduction

Auger analysis and Energy Dispersive X-ray Microanalysis (EDX) were used to study annealed ohmic contacts on solid substrates and thin GaAs membranes respectively. This chapter contains the results of the contact analysis.

On solid substrates, TLM test structures were fabricated with AuGe/Ni/Au ohmic contacts where the Ni concentration had been modified for low temperature annealing (see previous chapter). After annealing the samples (250-430 ^{o}C) and measuring their contact parameters, they were sent to Plessey for Auger Analysis. The results of the analysis are given in section 3.2.

Contacts with standard composition (approximately 5% Ni) were fabricated on GaAs membranes. These were annealed at 300 and 400 ^{o}C, then taken to the Physics Department (Glasgow University) for EDX microanalysis. The purpose of this experiment was to determine how far the contact material diffuses from the contact edge during annealing. The experiments are described in full in section 3.3.

3.2 Auger Analysis of Contacts to Solid Substrates.

3.2.1 Introduction

When an atom which has been ionised by incident photons or electrons undergoes subsequent deexcitation, the transition of electrons from one shell to another can result in the emission of an x-ray (sect 3.3.3) or the ejection of an Auger electron [3.1,3.2]. Auger electrons occur when a vacancy in the inner shell is filled by an electron from a less tightly bound level with the subsequent ejection of a second lower energy electron to the vacuum. The ejected Auger electron has an energy which is characteristic of the atom from which it came due to the well defined energy levels of the atom. Energy analysis therefore allows identification of the surface of the material [3.2].

Auger spectroscopy is only suitable for analysing material to a depth of about 1nm because the interaction of the ejected electrons with other atoms means that the electrons lose their characteristic energy. However, when Auger spectroscopy is combined with ion-beam etching it is possible to obtain a depth profile of solid material. Ion-beam etching can be used to slowly but progressively remove atoms of the material being studied. If Auger spectroscopy is used to analyse the surface of the material as etching progresses, the variation of the chemical composition with depth can be derived. This method of analysis was used to study ohmic contacts to solid GaAs substrates.

3.2.2 Sample Description

The samples which were analysed consisted of TLM structures (sect 2.2.2) metallised with 85 nm AuGe (88:12), 19 nm Ni (10.2% by weight) and an Au capping layer 35 nm thick. This was a composition which would allow low temperature annealing of the contacts (the optimum temperature range turned out to be 320 - 350 ^{o}C). Six samples were sent to Plessey Research Centre (Caswell) for analysis: an unannealed sample and five annealed samples. The annealing temperatures were 250, 300, 350, 400 and 450 (^{o}C). The specific contact resistance of the five annealed samples were 7.69, 2.88, 2.57, 3.60 and 5.44 (all x 10^{-5} ohm.cm^{2}) respectively. These values were determined using the modified TLM described in chapter 2.

The samples prepared for this experiment all came from the same batch (ie they were fabricated on the same wafer, then the wafer was scribed and broken into individual test chips). The three metallic contact layers were evaporated in separate vacuum cycles. This allowed clean microscope slides to be placed near the sample during each evaporation. The thickness of the metallic layers deposited on the glass slides was then measured by talystep. As a double check, the combined thickness of the layers deposited on the slide holding the sample was also measured. The combined thickness was found to equal the sum of the individual layer thicknesses. After contact metallisation the samples were annealed and then despatched to Plessey for analysis immediately after making the TLM measurements.

3.2.3 Results

Fig 3.1 a)-d) contains the Auger depth profiles from the unannealed sample and the samples annealed at 250 ^{o}C, 350 ^{o}C and 400 ^{o}C. The profile from the 430 ^{o}C annealed sample was similar to that of the 400 ^{o}C sample although the Ge, Au and Ni had diffused slightly further into the GaAs (the 300 ^{o}C sample was lost in the system so no plot was obtained).

In the unannealed sample (fig. 3.1a)) the individual contact layers can be identified. It can be seen that even although the contact has not been annealed, there has been some diffusion of Ni into the AuGe layer. This observation is consistant with other reported results [3.3,3.4]. There has also been some separation of the Ge and Au during evaporation even though the metals were evaporated from the same source. Both the high mass and the large amount of Au in the evaporation boat combine to produce an Au-rich film at the GaAs surface due to the relative evaporation rates of the metals. It was estimated that the initial evaporation rate of of Au from the AuGe melt would be about 4 times the evaporation rate of Ni. [3.5 with data from 3.6].

Looking now at the profile from the 250 ^{o}C annealed sample (fig. 3.1b)), it is evident that some movement of the contact material has already taken place. The most striking result is that the Ge has diffused into the Ni layer, away from the GaAs surface. This is the observation Ogawa made in his study of annealed ohmic contacts [3.7]. The Ni layer has also diffused towards the GaAs surface and there has been some diffusion of Au into the GaAs.

The profile obtained from the 350 ^{o}C annealed sample (fig. 3.1c)) is completely different. Ni has now diffused a long way into the GaAs and Ge has also diffused inwards but not as far as the Ni. There is evidence of outdiffusion of both Ga and As but more Ga has actually pentrated to the surface. The Au profile is also of interest. In the previous plots there have been two Au peaks, one from the capping layer and the other from the AuGe layer. Now the peaks have merged together and whereas there was

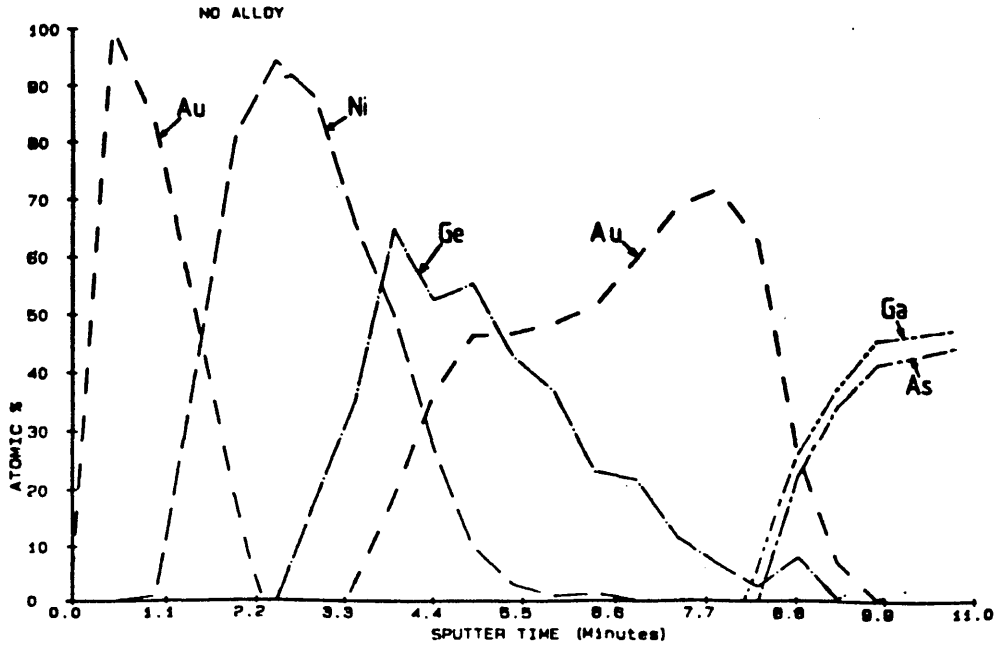


Fig. 3.1 a). Auger Profile of an as deposited AuGe/Ni/Au contact on n^+ GaAs.

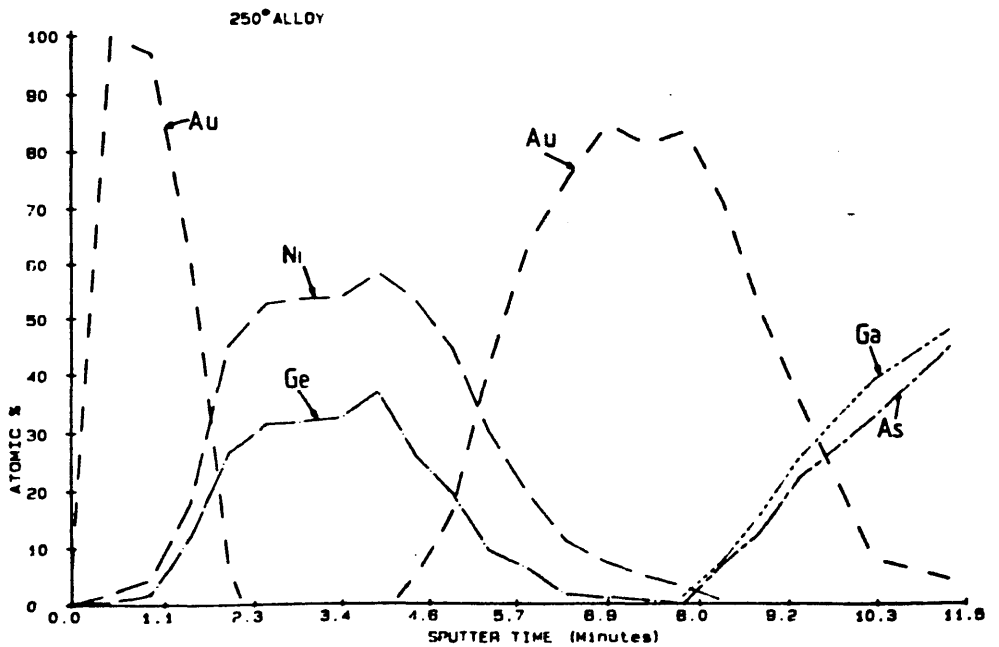


Fig. 3.1 b). Auger Profile of an AuGe/Ni/Au contact on n^+ GaAs after a 1 minute anneal at 250 ^{o}C.

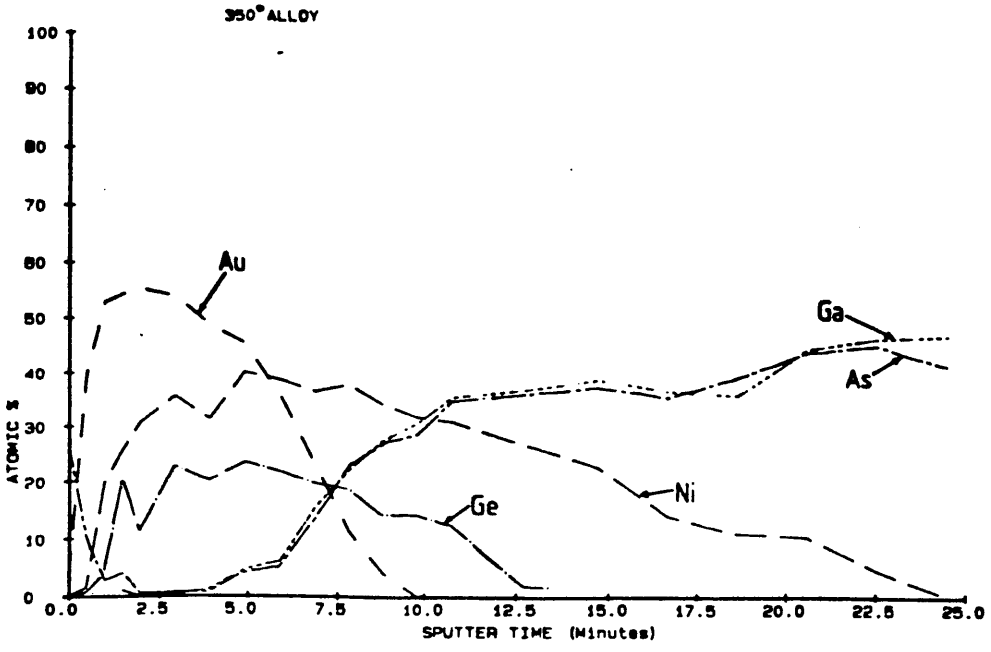


Fig. 3.1 c). Auger Profile of an AuGe/Ni/Au contact on n^+ GaAs after a 1 minute anneal at 350 ^{o}C. This was the optimum annealing temperature for this particular set of contacts.

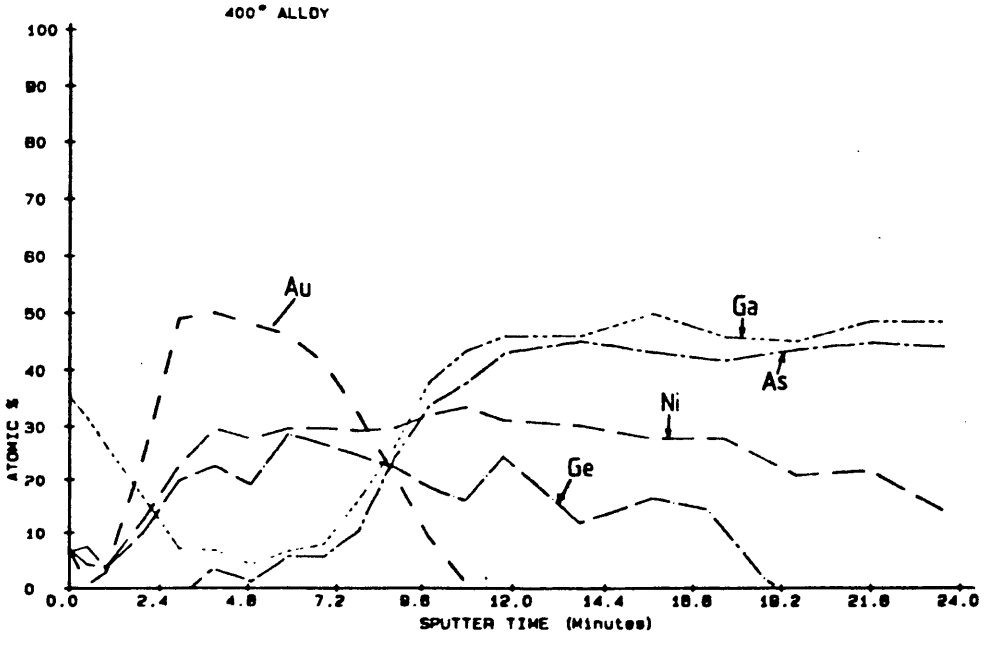


Fig. 3.1 d). Auger Profiles of an Auge/Ni/Au contact on n^+ GaAs after a 1 minute anneal at 400 ^{o}C.

evidence of Au diffusing into the GaAs at 250 ^{o}C it appears not to have diffused any further at this higher anneal temperature.

Of all the samples measured, it was the 350 ^{o}C annealed sample which produced the minimum specific contact resistance. In a previous experiment it was found that at the optimum annealing temperature for contacts with a composition similar to the contacts described here, more Ge than Ni was detected at any given depth into the semiconductor. This was a reasonable observation since Ge provides donors in GaAs, if it is incorporated into the Ga lattice sites, whereas Ni would add acceptors. The mechanism for producing good ohmic contacts, as discussed in chapter 2 [3.8], is to create a highly doped layer below the contact in order to reduce the metal-semiconductor barrier width, thus allowing tunneling of electrons through the barrier. Therefore, to minimise the contact resistivity, it is clear that the amount of Ge diffused into the GaAs should exceed the amount of Ni.

However, in the results presented here it is evident that a greater amount of Ni has diffused into the substrate. Other reported Auger profiles of annealed contacts also show similar effects [3.4,3.5]. This suggests that although large amounts of Ni have diffused into the substrate, the Ni is not becoming active as an acceptor in the GaAs.

The Auger profile of the 400 ^{o}C annealed sample shows that both the Ge and Ni have diffused further into the substrate. However, instead of producing a contact with a lower specific contact resistance, ρ_c has increased from the 350 ^{o}C annealed value of 2.57 x 10^{-5} ohm.cm^2 to 3.6 x 10^{-5} ohm.cm^2 (with a further increase to 5.44 x 10^{-5} ohm.cm^2 at 430 ^{o}C). Some possible explanations for the increase in specific contact resistance are given in the discussion below. It should be noted that in this particular sample (400 ^{o}C anneal), the annealed contact was highly irregular so an exact interpretation of the Auger profile cannot be made.

3.2.4 Discussion

In the above experiments Auger Analysis was used to study the diffusion of the various contact metals in GaAs. The problem is now to try and relate the Auger profiles with the measured specific contact resistances.

It was found that, at the optimum annealing temperature (350^{o}C) Ni had diffused further than the Ge. Since Ni is an acceptor in GaAs it would be expected that the large amount of Ni would have resulted in a deterioration of the contact resistivity. However, since a very low contact resistance was measured on this sample (2.57 x 10^{-5} ohm.cm^{2}) it would appear that the Ni must be electrically passive when annealed at 350 ^{o}C. The donor concentration below the contact, determined from the measured ρ_c value [3.9], is 3 x 10^{19} /cm^{3} which is more than an order of magnitude greater than the initial concentration. This indicates that Ge has moved into the lattice sites vacated by the out-diffusing Ga atoms.

Two questions arise from the work on low temperature annealed contacts. The first is what role does the nickel play in ohmic contact formation? The work done by Ogawa [3.7] reports that Ni acts as a catalyser for the reaction between Au and GaAs resulting in the formation of Au-Ga and leaving vacancies in the GaAs lattice. Since the diffusion coefficient of a substitutional diffuser such as Ge in GaAs is proportional to the number of lattice vacancies, the enhanced out diffusion of Ga to the contact metal would subsequently result in a higher concentration of Ge donors in the semiconductor. Other reports [3.7,3.10] suggest that it is the fast diffusing Ni which enhances the diffusivity of Ge in GaAs. Therefore, it could be that the catalysed reaction between Au and Ga, coupled with the Ni enhanced, Ge diffusion into the GaAs lattice, results in the formation of the degenerately doped layer essential for low resistivity contact formation [3.8].

The second question is, why does the specific contact resistance increase with anneal temperatures above the optimum? Auger analysis does not tell us anything since the profiles from

the 350 °C (optimum) and 400 °C (and 430°C) samples are similar, except for the slightly deeper diffusion of Ni and Ge at the higher temperatures.

In the paper by Yoder [3.10] it is stated that excess annealing (temperature or time) could lead to deeper Ni penetration into the substrate with a subsequent reduction in the Ge donor concentration below the contact. However, observation of the Auger profile at 400 °C shows that there is about 20 % (atomic) of Ge in the semiconductor just below the contact/GaAs interface. It is therefore likely that there are more Ge atoms present than Ga vacancies which implies that deep diffusion is not the origin of the increased contact resistivity.

However, it may be possible that when the contact are annealed at higher temperatures, Ni becomes incorporated into the GaAs lattice and becomes electrically active. This would have the effect of adding compensating acceptors to the semiconductor which, in turn, would lead to an increase in specific contact resistance due to the increase metal semiconductor barrier width. Another possibility is the higher annealing temperatures increase the amount As out-diffusion (although this is not evident from the Auger profiles). The vacated As sites could then be filled by Ge, which is an amphoteric dopant in GaAs. This would again have the effect of increasing the level of compensating acceptors in the semiconductor, with a corresponding increase in ρ_c.

Both the mechanisms described above would reduce the quality of the ohmic contact, however, it is impossible to tell from the Auger analysis which process, if either, actually occurs. What the Auger profiles do tell us is that the diffusion depth of the contact material when an annealing temperature of 400 °C is used is more than 400 nm. However, when a contact was annealed at 300 °C the diffusion depth was reduced to about 100 nm. These diffusion lengths were determined making the crude assumptions that the etch rate of the contact and semiconductor were the same and that the thichkness of the annealed contact was the same as the deposited metal thickness.

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3.3 Energy Dispersive X-ray Microanalysis of Contacts to Thin GaAs Membranes.

3.3.1 Introduction

In the previous experiments it was not possible to determine how far the contact material moved laterally during annealing. The reason for this is that the area required for producing an Auger plot (tens of microns) was far greater than the expected diffusion length of the material. This meant that it was impossible to analyse the composition of the GaAs (+ contact material) at short distances from the contact edge. Therefore, in order to determine how far the contact diffuses an alternative technique was used.

Ohmic contact patterns were defined (using lift-off) on thin GaAs membranes [3.12] and then annealed. Energy dispersive x-ray microanalysis was then used to study the diffusion of the contact material through the membrane. Since the probe diameter used for EDX analysis was between 2.5 and 5.0nm, it was possible to get a reasonable idea of how far the contact had diffused during annealing. Although the diffusion through the membrane would be different to that through bulk material, the results of this experiment confirm that low temperature annealing should be used when closely spaced, annealed contacts are required.

3.3.2 Sample Preparation.

The fabrication technique for GaAs membranes is given in full in chapter 6 therefore only a brief description is given here. The membrane material consists of (from the surface) alternate layers of GaAs (100 nm membrane layer), AlGaAs (330 nm), GaAs (340 nm), and AlGaAs (1.04 μm), grown by Metal Organic Chemical Vapour Deposition (MOCVD), at Plessey Research Centre (Caswell), on a GaAs substrate. The AlGaAs/GaAs (60 % Al) layers were used as etch stop layers - when a well was etched from the back of the wafer, these layers could be selectively removed until only the top GaAs layer remained. This was the layer which formed the GaAs membrane.

When several membrane samples had been fabricated, they were spin coated with a thick layer (1 μm) of PMMA (mol. wt 185,000) and then baked at 180 ^{o}C for about 12 hours. A pattern of transistor source-drain ohmic contacts (see fig 6.12) was then exposed using a 125 nm diameter electron beam on each membrane. After developing in 1:1 MIBK:IPA the surface of the GaAs exposed through the developed windows in the PMMA was cleaned in 5% ammonia solution then rinsed in deionised water and blown dry. The contact metallisation consisted of 90 nm AuGe, 13 nm Ni (6.5% of the AuGe layer by weight) and 20 nm Au. This was not an optimised composition for low temperature annealing since the percentage of Ni, relative to AuGe, was too low (see chapt 2). The transistor contact pattern was defined by lift-off.

Three membrane samples with contact patterns survived the fabrication processes. Two of these samples were then annealed, one at 300 ^{o}C and the other at 400 ^{o}C. Fig 3.2 contains STEM micrographs of the annealed contacts taken from the same position on the device patterns. It can be seen that when the contacts were annealed at 400 ^{o}C there had been a lot of movement of the contact material during annealing. The edges of the contact are no longer well defined. The contact metal appears to have coalesced forming islands of dense contact material within areas which seem to be virtually depleted of contact metal. When the annealing temperature was reduced to 300 ^{o}C the contacts appear to be more uniform. The edges are reasonably well defined, although when the sample was observed at higher magnification there appeared to be a layered structure at the contact edge. This will be discussed in more detail later.

One sample was left unannealed. The unannealed sample was on a membrane which consisted not only of the 100 nm GaAs layer but also had the underlying AlGaAs layer. This gave a total membrane thickness of 400nm.

3.3.3 Energy Dispersive X-ray Microanalysis

Chemical analysis in an STEM is performed by measuring the energy and intensity distribution of the x-ray signal generated by a focused electron beam [3.13]. X-rays are produced by the

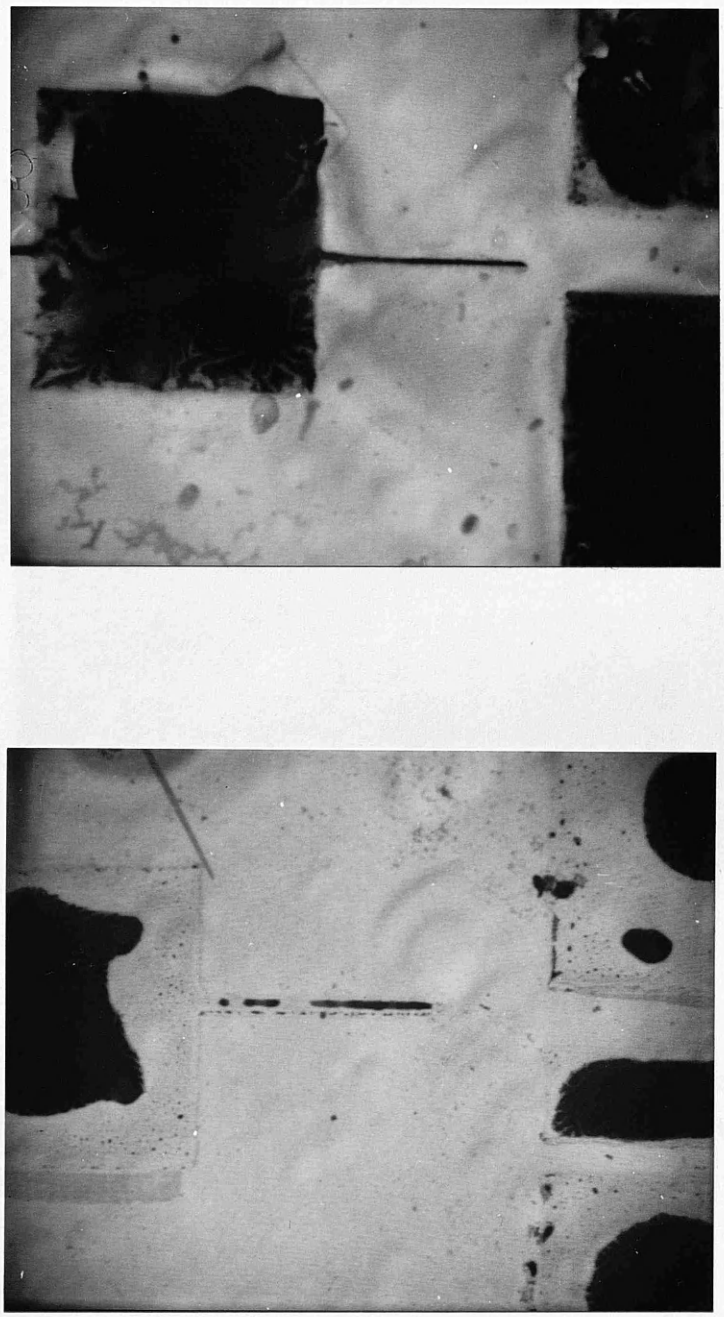


Fig. 3.2. SEM micrographs of AuGe/Ni/Au contacts deposited on 100 nm membranes of GaAs. The top micrograph shows a sample which was annealed for 1 minute at 300 ^{o}C and the bottom micrograph is of a sample annealed for 1 minute at 400 ^{o}C.

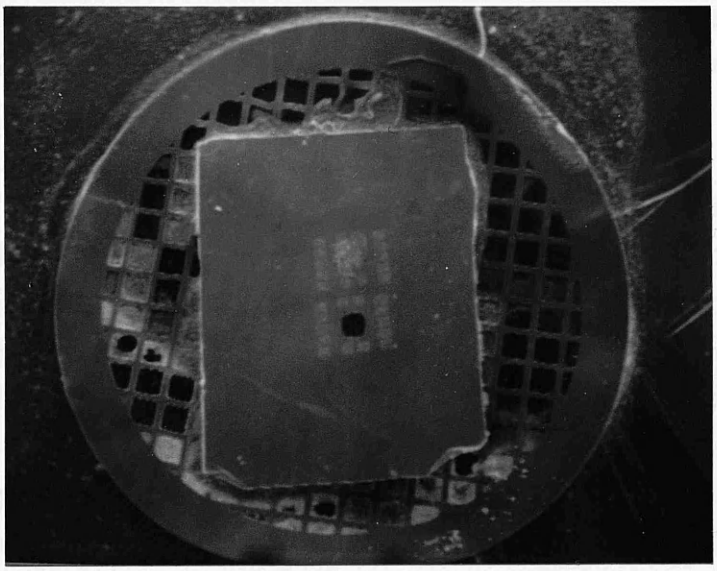


Fig. 3.3. SEM micrograph of a membrane chip, mounted on a copper TEM grid. This was suitable for loading into the HB 5 STEM for x-ray microanalysis.

following process. The interaction of a beam electron with an inner-shell electron can result in the ejection of the bound electron which leaves the atom in an excited state with a vacancy in the inner electron shell. During subsequent deexcitation, there is an electron transition from an outer shell to fill this vacancy. The energy released by this transition can manifest itself either in the form of an x-ray or an ejected (Auger) electron. The energy of the transmitted x-ray is related to the difference in energy between the sharply defined levels of the atom and is referred to as a characteristic x-ray.

EDX microanalysis of the annealed ohmic contacts on thin GaAs membranes was carried out in a VG HB 5 STEM. The membrane chips were "glued," using 10% polyimide, on to copper TEM specimen grids (fig. 3.3) which could then be placed in the standard specimen holder for the microscope. An electron probe diameter of 5 nm was used for microanalysis of the contacts. The sampling time at each measurement site was 200 seconds. The spectrum recorded at each sampling site was stored on disc for future analysis.

3.3.4 Characteristic X-ray Spectrum

The characteristic x-ray spectrum obtained from the centre of a contact on the unannealed sample is shown in fig. 3.4. The energy range 6 keV to 16 keV contains all the significant information for the elements contained in the ohmic contacts. The x-ray peaks detected in this range were the $K\alpha$ and $K\beta$ peaks for Ni, Cu, Ga, Ge and As as well as the $L\alpha$, $L\beta$ and $L\gamma$ peaks for Au. The Cu peak is background due to the relatively large amount of copper present in the TEM grid and the grid holder itself.

The EDX spectrum shown in fig. 3.4 reveals that some of the peaks are close enough in energy that peak overlapping occurs. At first sight this would appear to create problems in the quantitative analysis of the contacts. However, it was possible to extract the intensities of all of the peaks given that the proportion of $K\alpha$ to $K\beta$ peaks was known for each element [3.14]. This will be illustrated in the following section

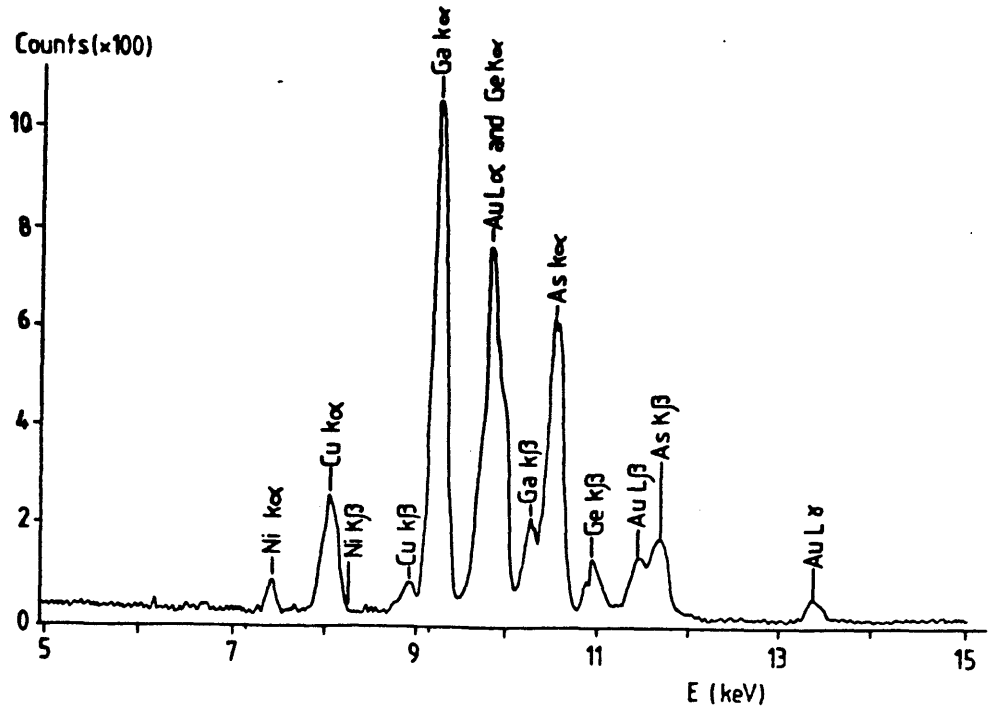


Fig. 3.4. X-Ray Spectrum obtained from the centre of an ohmic contact (unannealed). The characteristic x-ray peaks of interest are indicated on the diagram.

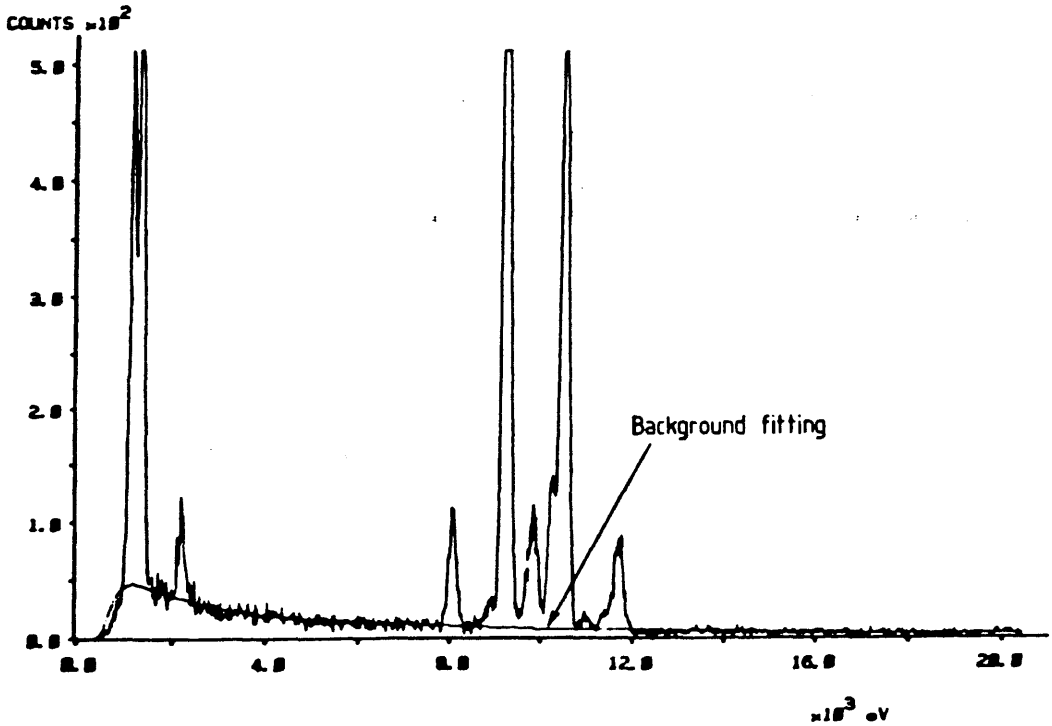


Fig. 3.5. X-ray spectrum showing the modelled background superimposed on the actual background level. The windows set for modelling the background were from 3-7 keV and 14-18 keV where there are no characteristic x-ray peaks.

3.3.5 Spectrum Analysis.

The first step in the analysis of the x-ray spectra was to model the background signal of the recorded spectra. A software routine was available in the Physics Department for this purpose. The background was modelled by setting two windows at energies where there were no peaks from the detected elements. In the case of the contacts on GaAs membranes the windows were set between 3 and 7 keV and 13 and 17 keV. The background is represented in the form $D(a/E + b + cE)$ where D is the x-ray detector efficiency, E is the energy and a, b and c are the fitting parameters. Fig. 3.5 shows an EDX spectrum from 0 to 20 keV with the background modelled using the technique described above. It can be seen that the modelled background fits the background of the spectrum over the entire energy range. The x-ray peaks below 3 keV are the low energy L peaks of Cu, Ni, Ga, Ge and As which, because they were all so closely spaced, were not used in the contact analysis.

Once the background had been modelled, it was then possible to integrate the total number of counts associated with each peak. This was done by setting energy windows around each peak then subtracting the background integral to give the net signal integral. For example the energy window 7.7 kev to 8.4 keV contains all of the Cu $K\alpha$ peak but no other peaks, except the Ni $K\beta$ peak which is small enough to be assumed negligible. In the case of overlapping peaks, the window was set from the minimum energy of the lower energy peak to the maximum energy of the higher energy peak (for example 8.8 keV to 9.6 keV contains the Cu $K\beta$ peak and the Ga $K\alpha$ peak). The net signal integral for the combined peak was then deduced as before.

To evaluate the net signal integral for each peak in an overlapping signal, a hand calculation had to be made. As an example, consider the net signal integrals obtained from the combined Cu $K\beta$ and Ga $K\alpha$ peaks and the isolated Cu $K\alpha$ peak mentioned above. The ratio of $K\alpha$:$K\beta$ intensities are well tabulated for the elements of interest in these experiments [3.14]. Therefore, it is a trivial task to extract the Cu $K\beta$ peak from the integral for the overlapping Cu $K\beta$ and Ga $K\alpha$ peaks

leaving the net signal integral for the Ga Kα peak. The relative intensities of the x-ray peaks could then be converted to relative number of atoms by a simple calculation [3.15,3.16].

Using this method it was possible to extract the net signal integral for each of the elements detected from the samples. The only problem arose with the Au Lα and Ge Kα peaks which occured at similar energies (9.711 keV and 9.876 keV respectively). In the bulk of the contact, where there was a lot of gold present, it was difficult to determine accurately the amount of Ge which was present. Fortunately however, the Ge Kβ peak was sufficiently separated in energy from any of the other elements that a net signal integral could be obtained for this peak on its own, therefore giving a reasonable indication of the amount of Ge in the contact.

3.3.6 Experimental Results

To determine how far the contact metal had diffused laterally during annealing, x-ray spectra were recorded at various positions away from the contact edge. The distance between sampling sites was 50 nm in the vicinity of the contact edge, increasing to half micron steps away from the contact edge.

In the unannealed sample there was a distinct boundary between the metal contact and the GaAs substrate. It was therefore straight forward to record spectra at specified distances from the contact edge. However, the boundary between the metal and the substrate was not so well defined on the sample annealed at 300 ^{o}C. As mentioned earlier, there was a layered structure at the contact edge. This is illustrated in fig. 3.6. The layered structure is likely to be caused by the different diffusion lengths of the contact materials. For the purposes of this experiment, the original contact edge was taken to be at the edge of the darkest layer, as indicated in the figure.

The definition of the original contact edge was made even more difficult in the case of the 400 ^{o}C annealed sample. Here, because the contact was no longer uniform, it was very difficult to predict where the contact edge had been before annealing.

300 °C

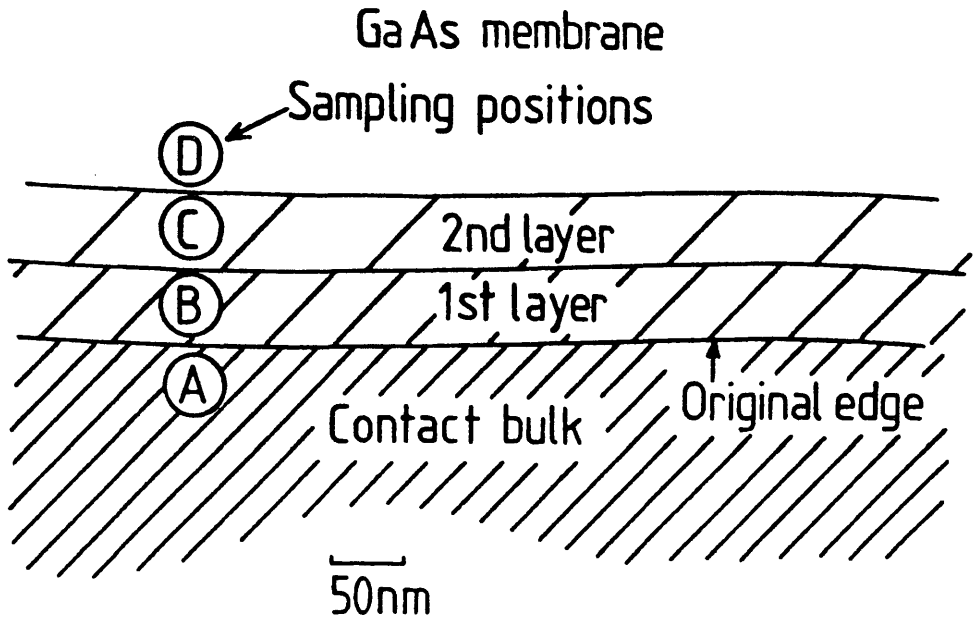


Fig. 3.6 Schematic representation of the layered structure found at the edge of a contact annealed at 300 °C. Typical locations for recording x-ray spectra are also shown.

400 °C

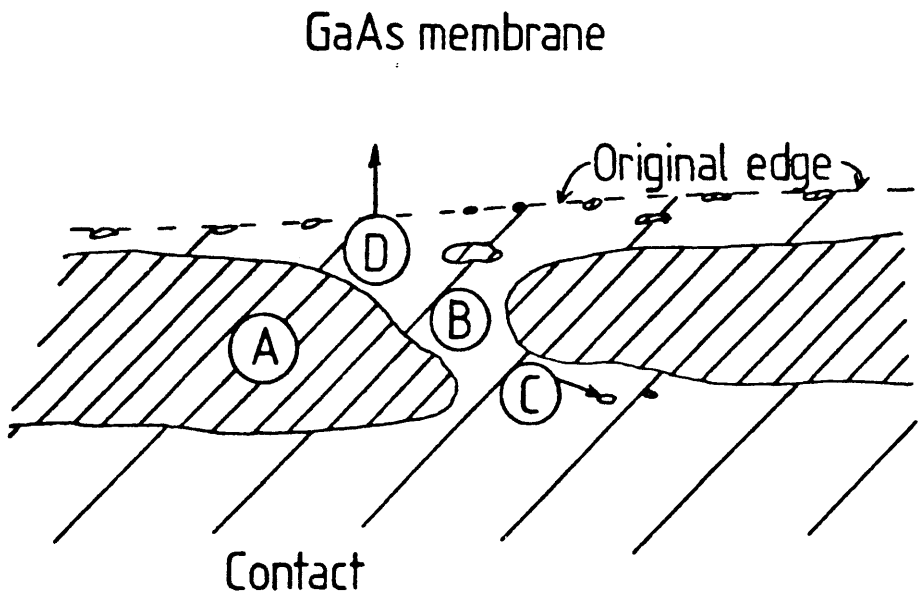


Fig. 3.7 Schematic representation of the edge of a contact annealed at 400 °C. X-ray spectra were recorded at locations similar to those indicated in the figure.

However, closer inspection of parts of the sample showed that there were rows of small (sub 0.1 micron) particles which corresponded (judging from their general position) to the outline of the original contacts. This is illustrated in fig. 3.7.

3.3.7 Unannealed Sample.

Two typical spectra from the unannealed sample are shown in fig 3.8. Spectrum a) was recorded 50 nm from the edge of the contact (into the metallic region) and spectrum b) was recorded 25 nm from the contact edge (off the metallised region). As expected, all the elements of the contact metallisation can be detected within spectrum a) whereas only Ga and As are detectable in b) (excluding the background Cu peak). This shows that there is no diffusion of the contact material as the metal is evaporated.

3.3.8 300 ^{o}C Annealed Sample

The edge of a typical contact annealed at 300 ^{o}C was shown in fig 3.6. The width of the different layers at the contact edge was approximately 50 nm at any particular location around the edge of the contacts. Typically four x-ray spectra were recorded at each measurement location on the sample. The spectra obtained (fig. 3.9 a)-d)) correspond to 25 nm into the thick contact region, the centre of the two layers, and 25 nm from the second layer respectively.

From these spectra the following deductions can be made:-

1 - Gold and Ge have diffused outwards from the contact into the first layer outside the contact. This was evident because both the Au Lγ and Ge Kβ peaks were detected whenever an x-ray spectrum was recorded from the first layer.

2 - Only Ge has diffused into the second layer. A relatively large peak was detected at the Au Lα-Ge Kα energy. Since there was no evidence of an Au Lγ peak but there was a distinct GeKβ peak it was concluded that only Ge had diffused into this layer.

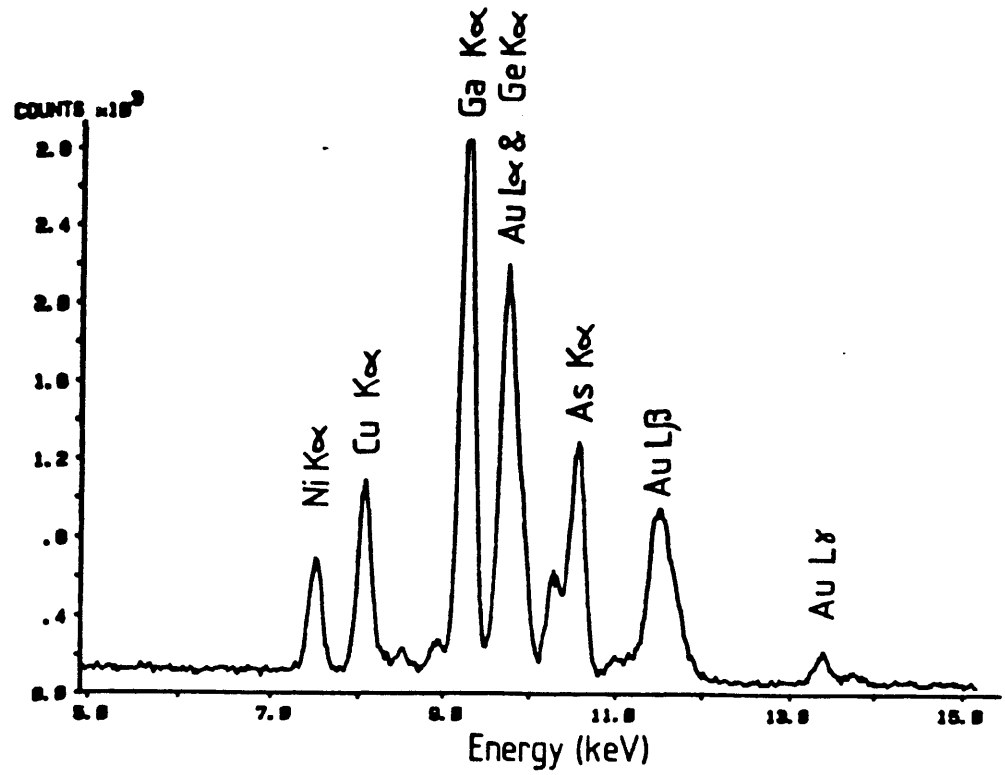


Fig. 3.8 a). X-ray spectrum obtained from a position 25 nm onto the contact on an unannealed sample. As expected all of the contact elements plus Ga and As can be detected.

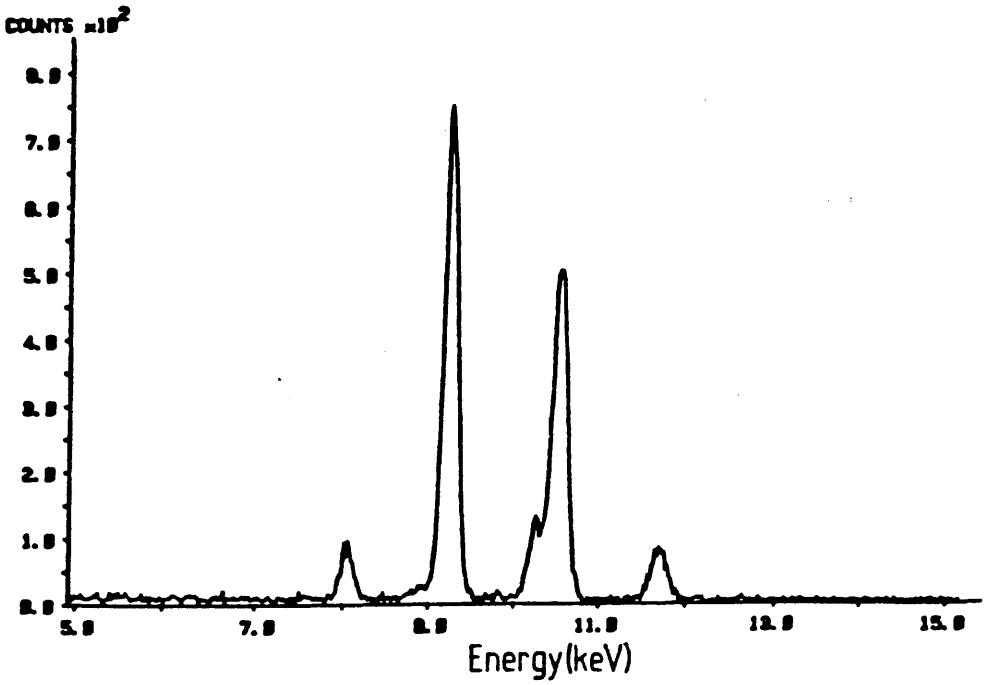


Fig. 3.8 b). X-ray spectrum obtained from a position 25 nm away from the contact on an unannealed sample. Only Ga and As (and background Cu) can be detected which indicates that there has been no diffusion of the contact material.

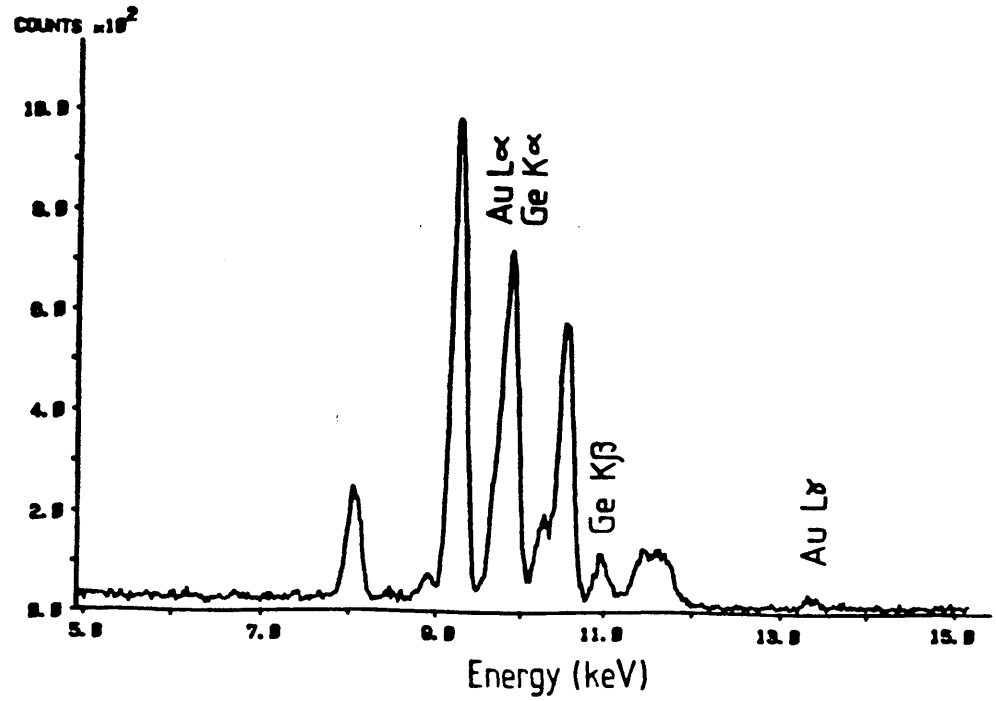


Fig. 3.9 a). X-ray spectrum obtained from the thick part of an ohmic contact (position A, fig. 3.6) annealed at 300 °C. All of the contact elements except Ni have been detected.

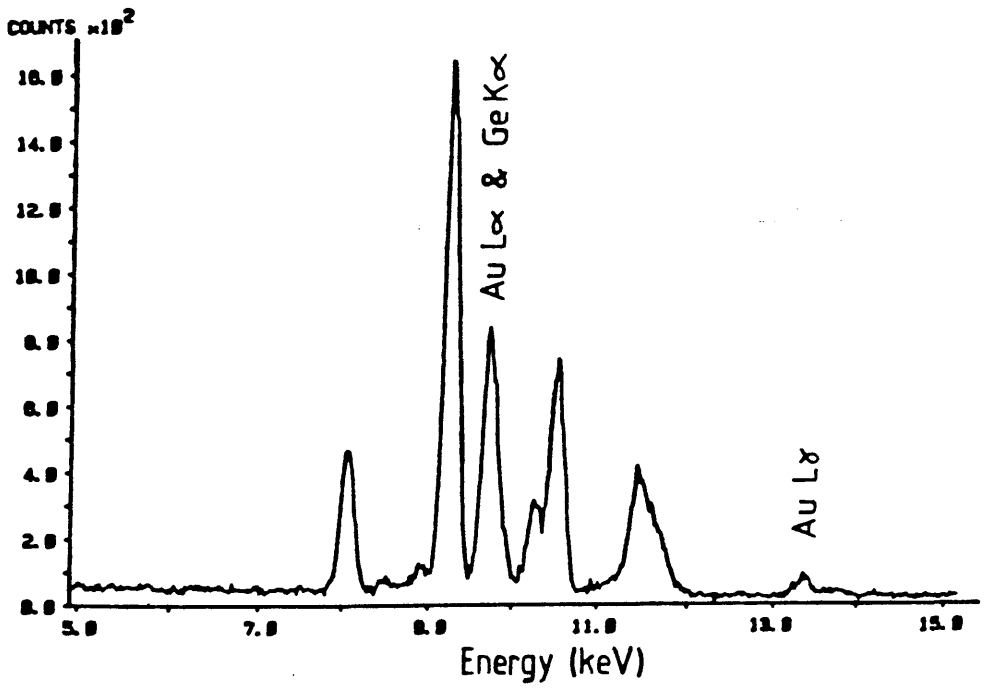


Fig. 3.9 b). X-ray spectrum obtained from the first layer around a contact annealed at 300 °C (position B, fig. 3.6). Large amounts of Au can be detected in this layer.

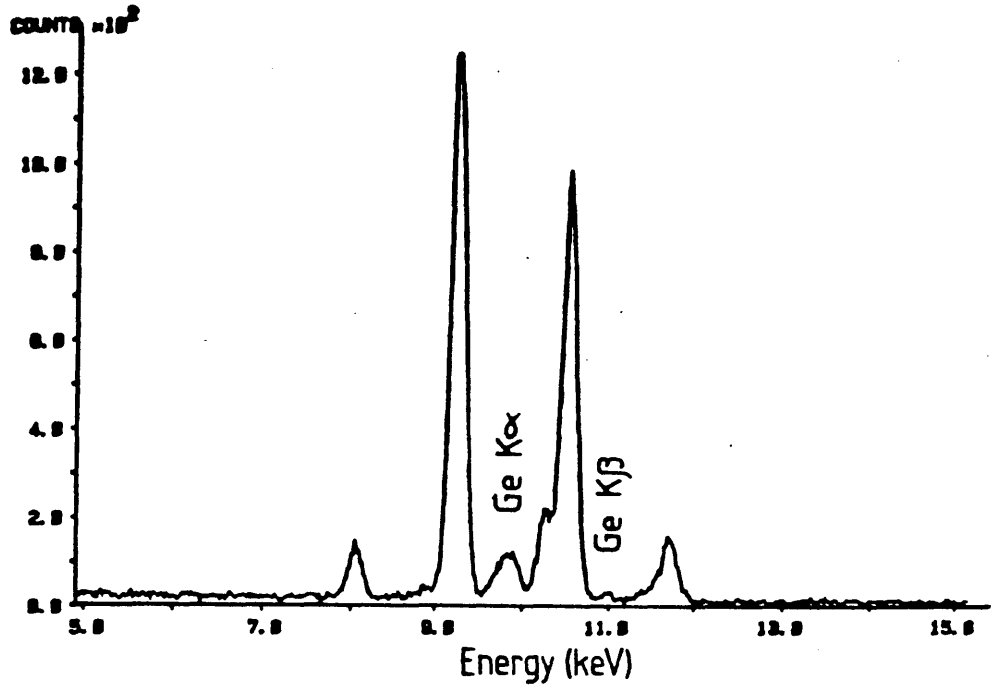


Fig. 3.9 c). X-ray spectrum obtained from the second layer around the 300 ^{o}C annealed sample (position C, fig. 3.6). There is no Au present in this layer but a relatively large amount of Ge can still be detected.

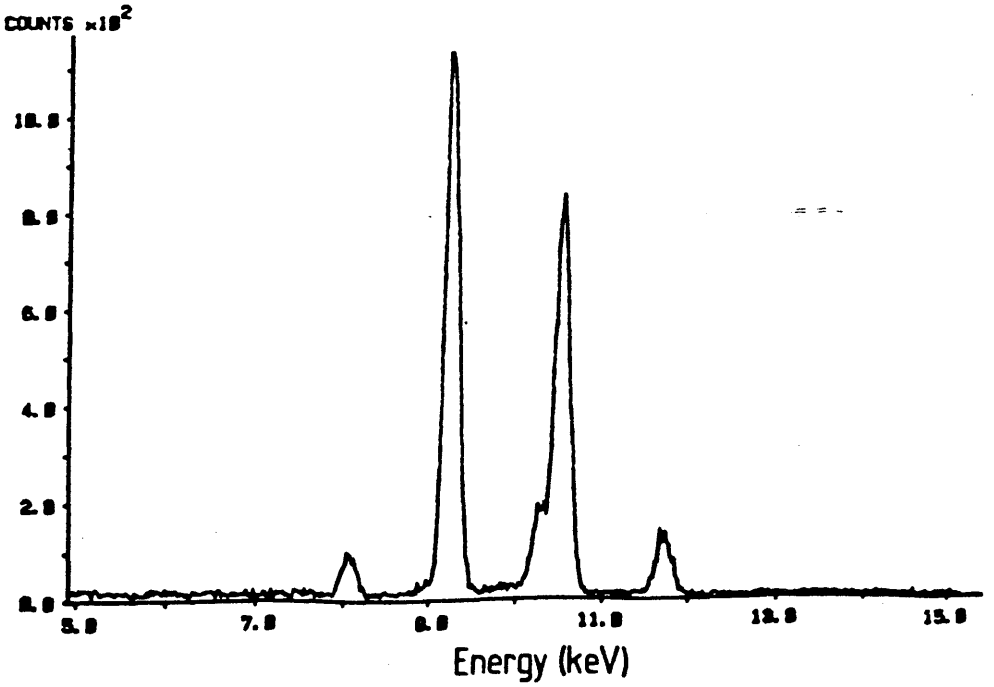


Fig. 3.9 d). X-ray spectrum recorded 25 mm away from the second layer around a 300 ^{o}C annealed contact (position D, fig 3.6). No detectable amounts of Au or Ge were found here.

3 - There were no Au or Ge peaks detected 25 nm from the edge of the second layer (125 nm from the original contact edge).

An interesting observation from these measurements was that no nickel was detected at any of the (25) sampling positions from this sample. This phenomenon will be discussed in sect. 3.10.

3.3.9 400 ^{o}C Annealed Sample

It was mentioned before that it was difficult to determine exactly where the original contact edge had been on the sample annealed at 400 ^{o}C. However, as a rough guide spectra were taken from the thick metallic regions within the contact, from the thin regions within the original contact area and in short increments away from the original contact edge.

The general observations from the spectra recorded from the 400 ^{o}C sample were:-

1 - The thick areas of the contact showed an abundance of gold, giving spectra similar to fig 3.9b).

2 - In the thin areas (but still within the area of the original contact) the spectra looked more like that of fig. 3.9c) with a relatively large amount of Ge present but no detectable Au.

3 - Outside the contact, the spectra were similar to "2" up to a maximum of 300 nm from the speculated contact edge indicating that relatively large amounts of Ge had diffused quite far from the contact edge.

4 - Further away from the contact, it was found that there was still detectable amounts of Ge well away from the contact edge. The spectrum shown in fig 3.10 was taken at a position on the membrane which was 5 μm from the nearest contact (the maximum distance from a contact on the membrane). It can be seen that there is still a distinct peak at the Ge Kα energy (9.876 keV). Care has to be taken in the interpretation of this result. Even though it appears as if the Ge has diffused a long way from the original contact, it cannot be determined from the x-ray spectrum

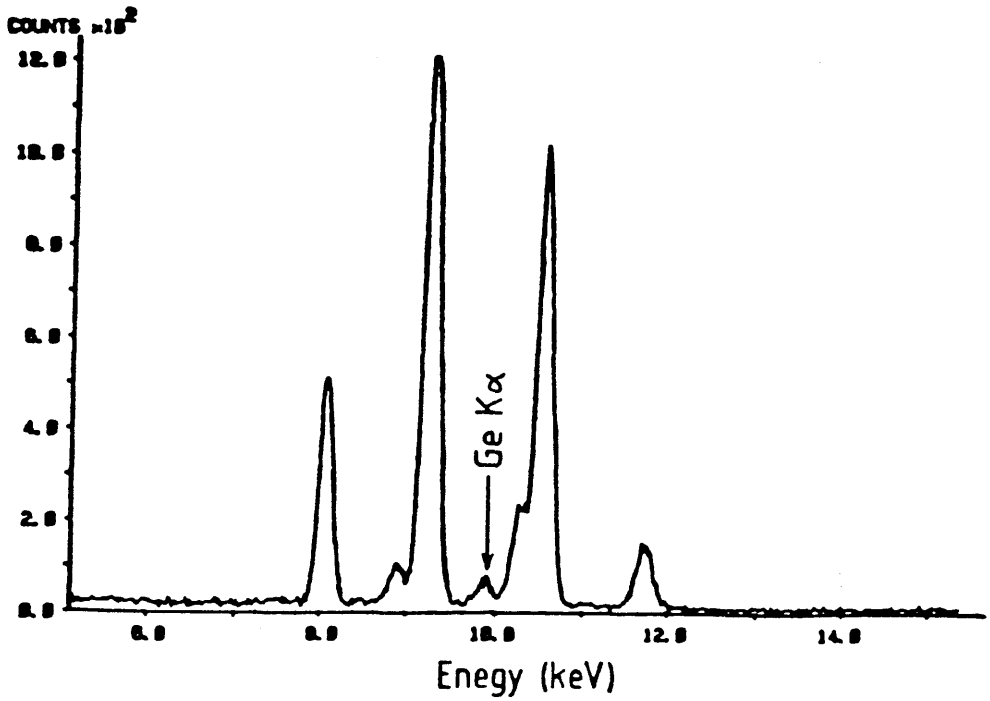


Fig. 3.10 This x-ray spectrum was recorded on the GaAs membrane at least 5 um away from the nearest contact, on the sample annealed at 400 ^{o}C. There is still a significant amount of Ge present in the spectrum indicating that the Ge has diffused a long way from the original contact edge.

whether it had diffused through the GaAs or if it had, in fact, only diffused over the surface of the membrane. Indeed, there is also the possibility that the detected Ge may be a result of contamination from the alloying furnace.

5 - As in the 300 ^{o}C sample, no nickel was detected anywhere on this sample either.

The qualitative observations described so far reveal two surprising results. Firstly, the distance the Ge moved from the contact edge during the high temperature anneal, assuming that it was diffusing through the GaAs, was far greater than the expected diffusion length of the material, even allowing for the fact that these contacts were fabricated on GaAs membranes, which would confine the diffusion to 2 dimensions.

Secondly, it was interesting to observe that on the two annealed samples there was no detectable amounts of Ni anywhere on the samples. It is possible that because the Ni diffuses so quickly (see Auger results) that even at low anneal temperatures, it spreads so far through the membrane that the level of nickel at any particular point is below the detection limit of the measurement technique.

3.3.10 Quantitive Analysis

Quantitive analysis of the two annealed contacts was carried out using the methods described in sect 3.3.5. In this analysis the intensity of the Ge and As peaks were normalised to the Ga peak. It was then possible to convert the relative number of counts into number of atoms [3.15,3.16].

Fig. 3.11 shows the number of atoms of Ge and As, normalised to the number of Ga atoms, as a function of distance from the original contact edge. As observed from the spectra when they were recorded, it can be seen that the Ge can be detected a long way from the contact edge (several microns) when the contacts are annealed at 400^{o}C. However, when the samples were annealed at 300 ^{o}C Ge can only be detected up to a maximum distance of 0.2μm from the contact edge. If, as was suggested above, the detected

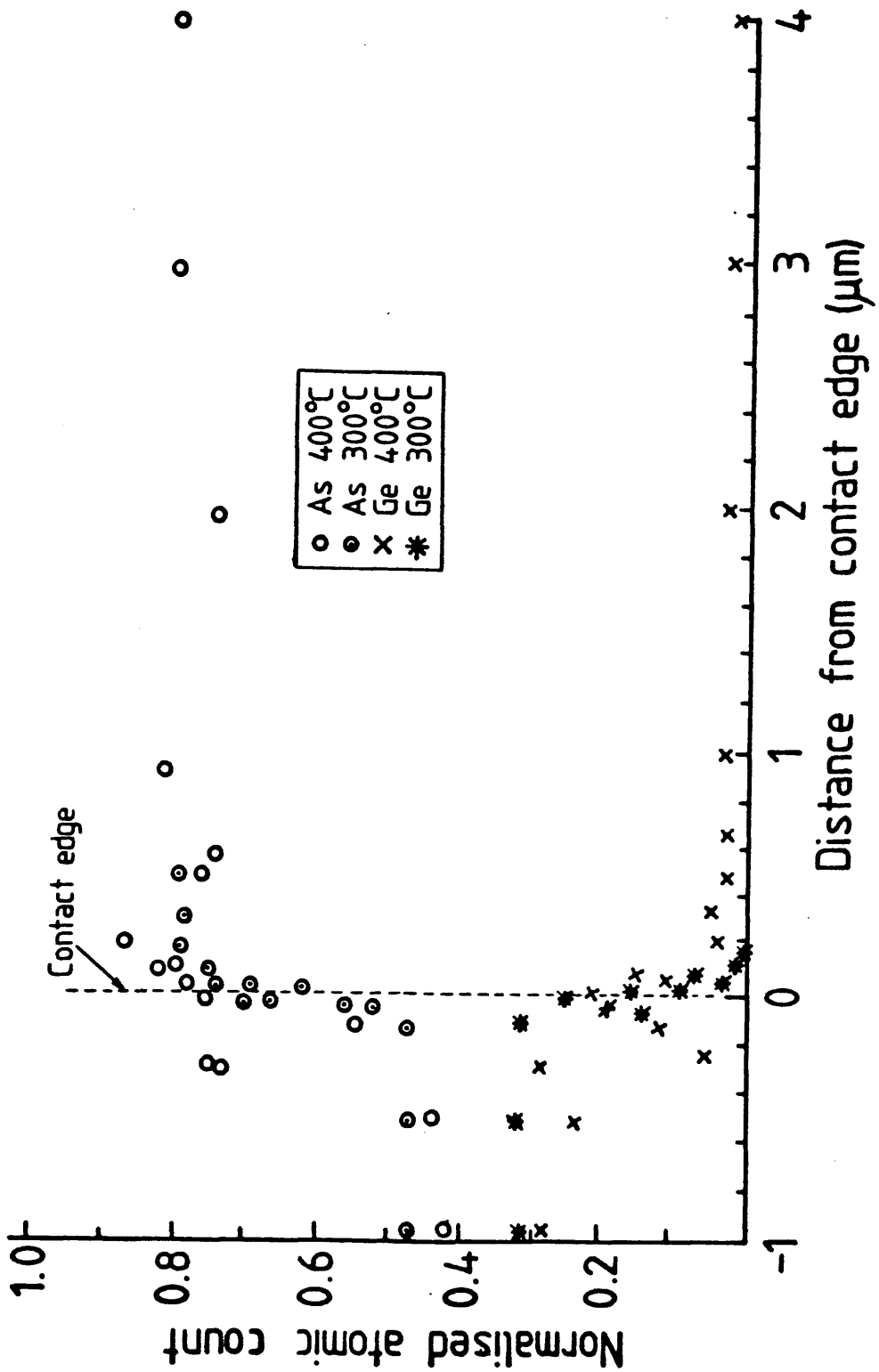


Fig 3.11 Graph showing the number of atoms of Ge and As normalised to the number of Ga atoms as a function of distance from the contact edge for samples annealed at 300 °C and 400 °C. Negative d denotes distance into the contact and positive d is distance away from the contact.

level of Ge far from the contact edge (4 μm) is due to contamination, then this level can be subtracted from the graph of fig. 3.11. If this is done, it is found that the maximum distance from the contact edge where Ge can still be detected is about 400 nm, which is about double the distance obtained when the sample is annealed at 300°C. It must be stated however, that this estimation is not very accurate considering the poorly defined edges of the contacts annealed at high temperature (fig. 2.2).

Another interesting observation from the graph in fig. 3.11 is that the As concentration below the contact was a lot lower than the concentration in the GaAs membrane away from the contact. To ensure that this effect was not due to absorption of the x-rays by the other elements in the contact, the absorption coefficient for As Kα Photons was calculated.

The absorption of Arsenic Kα was calculated for ohmic contacts of the composition described in sect. 3.3.2 deposited on a 100 nm GaAs membrane using the equation [3.15,3.17]

$$\frac{N_t}{N_o} = [1 - \exp(\mu/\rho)\rho t\,\mathrm{cosec}\phi)]/((u/\rho)\rho t.\mathrm{cosec}\phi)$$

where N_t is the number of transmitted x-rays, N_o is the number of x-rays generated in the specimen, (μ/ρ) is the mass apsorption coefficient, ρ is the specimen density, t is the specimen thickness and ϕ is the take-off angle which is the angle between the x-ray detector and the surface of the sample (30° in this case). The mass absorption coefficient for As Kα photons by the specimen was equivalent to

$$\left(\frac{\mu}{\rho}\right)_{\mathrm{Spec.}}^{\mathrm{As}} = \left[\left(\frac{\mu}{\rho}\right)_{i}^{\mathrm{As}} .C_i\right]$$

where $\left(\frac{\mu}{\rho}\right)_{i}^{\mathrm{As}}$

is the mass absorption coefficient of As Kα in material i and C_i is the mass fraction of material i. The mass absorption

coefficients were calculated from the theory in the paper by Thinh [3.18] and were confirmed by looking up the data base of ref [3.13].

The absorption of the As Kα x-rays by the specimen was calculated to be only 2.8 %. Even when the substrate thickness was increased to 400 nm (as was the case on the unannealed sample) the absorption was only increased to 5 %. This therefore indicates that the reduction in the As concentration below the ohmic contacts is not caused by the As x-rays being absorbed as they penetrate through the sample.

It is difficult to surmise where the As has gone during annealing. In fact a reduction in the As level was detected below the contacts even in the unannealed sample. This implies that the disappearance of As occurs as the metal contact layers are being evaporated. As no similar loss of As was detected from the Auger analysis of contact on solid substrates, it may be that the effect is peculiar to the evaporation of contacts onto membrane material. However without further experimental evidence, no precise conclusions can be drawn from this result. Similarly no definate explanation for the disappearance of Ni from the annealed contact can be given. It can only be speculated that the Ni has diffused so far in the membrane that the amount of Ni at any particular point is below the detection limit of the EDX system. This explanation may be viable since the original amount of Ni in the contact was small (only about 5 % of the total metallic layer weight) and it was shown in the Auger analysis of the contacts on solid substrate that Ni is a fast diffuser in GaAs.

3.4 Summary

In this chapter attempts have been made to analyse ohmic contacts fabricated on both solid substrates and on thin GaAs membranes. Both the Auger and EDX analysis have justified the neccessity for low temperature annealing when small contact separations are required, but the results from the membrane samples were particularly interesting. The fact that the Ge could be detected several microns from the nearest contact edge

in a specimen annealed at 400 ^{o}C but could only be detected 0.2 μm from the contact edge in a specimen annealed at 300 ^{o}C clearly indicates that, for short dimensions, low temperature contact annealing is desirable. It must be said however, that it was not established whether the Ge had diffused through the membrane or was only present on the surface of the membrane.

Chapter 3 References

[3.1] M. Prutton, "Surface Physics," 2nd ed. Claridon Press, Oxford (1983).

[3.2] J.C. Riviere, "Auger Electron Spectroscopy," Contemp. Phys. **14** p513-539 (1973).

[3.3] A. Iliadis, K.E. Singer, "Metallurgical behaviour of Ni/AuGe Ohmic Contacts to GaAs," Solid State Commun. **49**, 99-101 (1984).

[3.4] G.Y. Robinson, "Metallurgical and Electrical Properties of alloyed Ni/AuGe Films on N-Type GaAs," Solid State Eectronics, **18**, 331-342 (1975).

[3.5] R.W. Berry, P.M. Hall, M.T. Harris, "Thin Film Technology," p149-151, Van Nostrand Reinhold, New York (1968).

[3.6] C.J. Smithells, E.A. Brandes, "Metals Reference Book," 5th ed. Butterworts, London (1976).

[3.7] M. Ogawa, "Alloying Behaviour of Ni/AuGe films on GaAs," J Appl. Phys. **51**, 406-412 (1980).

[3.8] S.M. Sze, "Physics of semiconductor devices," 2nd ed. Sect. 5.7, Wiley, New York, (1981).

[3.9] C.Y. Chang, Y.K. Fang, S.M. Sze, "Specific Contact Resistance of Metal Semiconductor Barriers," Solid state Electronics, **14**, 541-550 (1971).

[3.10] MN Yoder, "Ohmic Contacts in GaAs," Solid State Electronics, **23**, p117-119 (1980).

[3.11] J.G. Werthern, D.R. Scifres, "Ohmic contacts to N-GaAs Using a Low Temperature Anneal," J. Appl. Phys. **52** 1127-1129 (1981).

[3.12] W.S. Mackie, S.P. Beaumont, C.D.W. Wilkinson, JS Roberts, "High Resolution Lithography on Active Semiconductor Membranes," Proc. 10th International Conference on Electron and Ion Beams Science and Technology, Montreal (1980).

[3.13] J.I. Goldstein, D.E. Newbury, P. Echlin, D.C. Joy, C. Fiori, E. Lifshin, "Scanning Electron Microscopy and X-Ray Microanalysis," Chapters 2 & 5, Plenum Press, New York (1981).

[3.14] K.F.J. Heinrich, C.E. Fiori, R.L. Myklebust, "Relative Transition Probabilities for the X-Ray Lines from the K Level," J. Appl. Phys, **50** 5589-5591 (1979).

[3.15] Useful discussions with Dr J.N. Chapman, Dept. Nat. Phil, Glasgow University, on x-ray spectra evaluation are gratefully aknowledged.

[3.16] J.N. Chapman, W.A.P. Nicholson, P.A. Crozier, "Understanding Thin Film X-Ray Spectra," J. Microscopy, **136**, 179-191 (1984).

[3.17] J.I. Goldstein, H. Yaowitz, D.E. Newbury, E. Lifshin, J.W. Colby, J.R. Coleman, "Practical Scanning Electron Microscopy," p330, Plenum Press, New York (1975).

[3.18] T.P. Thinh, J. Leroux, "New Basic Empirical Expression for Computing Tables of X-Ray Mass Attenuation Coefficients," X-Ray Spectrometry, **8** 85-91 (1979).

4.1 Introduction

4.1.1 Structure of a GaAs MESFET

The structure of a GaAs Metal on Semiconductor Field Effect Transistor (MESFET) is shown schematically in fig. 4.1. The device consists of two ohmic contacts, known as the source and drain, between which current can flow through a thin channel of conducting material. The current in the channel (I_d) is controlled by applying bias to the Schottky contact known as the gate. The drain-source channels are formed in n+ epitaxial layers grown on highly resistive substrates by Vapour Phase Epitaxy (VPE), Metal Organic Chemical Vapour Deposition (MOCVD), or Molecular Beam Epitaxy (MBE). Mesa isolation or boron isolation is used to define the drain-source channels. Alternatively the drain-source channel can be formed by local implantation into a semi-insulating substrate [4.1]. This technique is of particular interest for the fabrication of short channel n^+ self aligned (SAINT) GaAs MESFETs in which a "T" shaped gate is used as a mask during the implantation of high conductivity regions near the gate [4.2]. Using this method, exceedingly high switching speeds have been reported, the fastest of which is below 10 ps [4.3].

The MESFETs fabricated in this work were all depletion mode devices (normally on) which means that the built in potential of the gate-metal/semiconductor contact (V_b) does not fully deplete the active channel below the gate. A negative bias is applied to the gate to increase the depletion width below the gate, therefore reducing I_d. With sufficient bias, the depletion region will extend all the way through the active layer blocking the current flow between the contacts. The voltage required to turn the transistor off is known as the pinch-off voltage. If the depletion region of the unbiased gate extended all the way through the active layer, the device would be an enhancement mode MESFET (normally off). In such a device, a positive gate bias has to be applied to reduce the depletion width below the gate, allowing current to flow between source and drain. No attempts

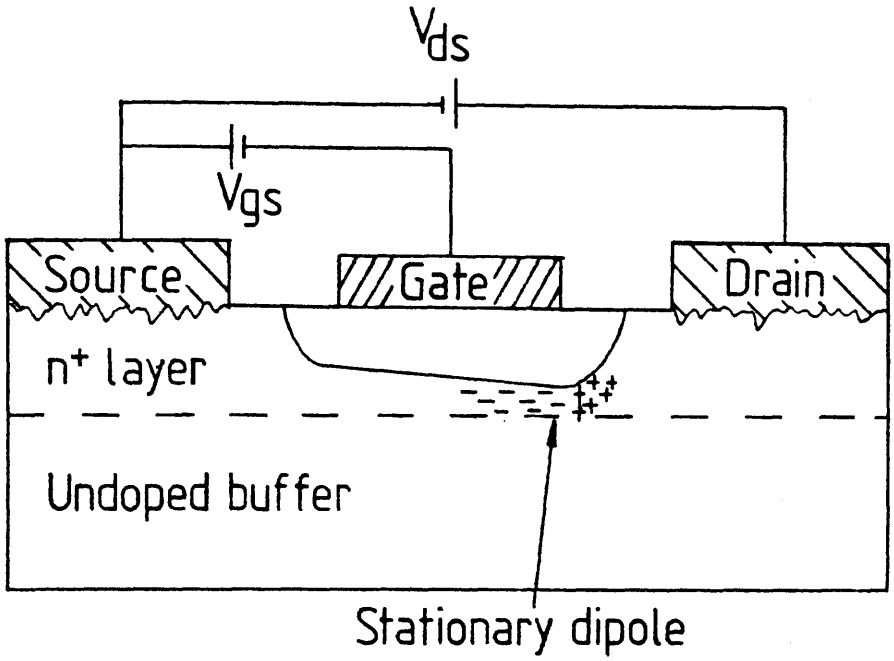


Fig. 4.1 Schematic cross section of a GaAs MESFET showing the depletion region under the gate and the position of the stationary dipole layer.

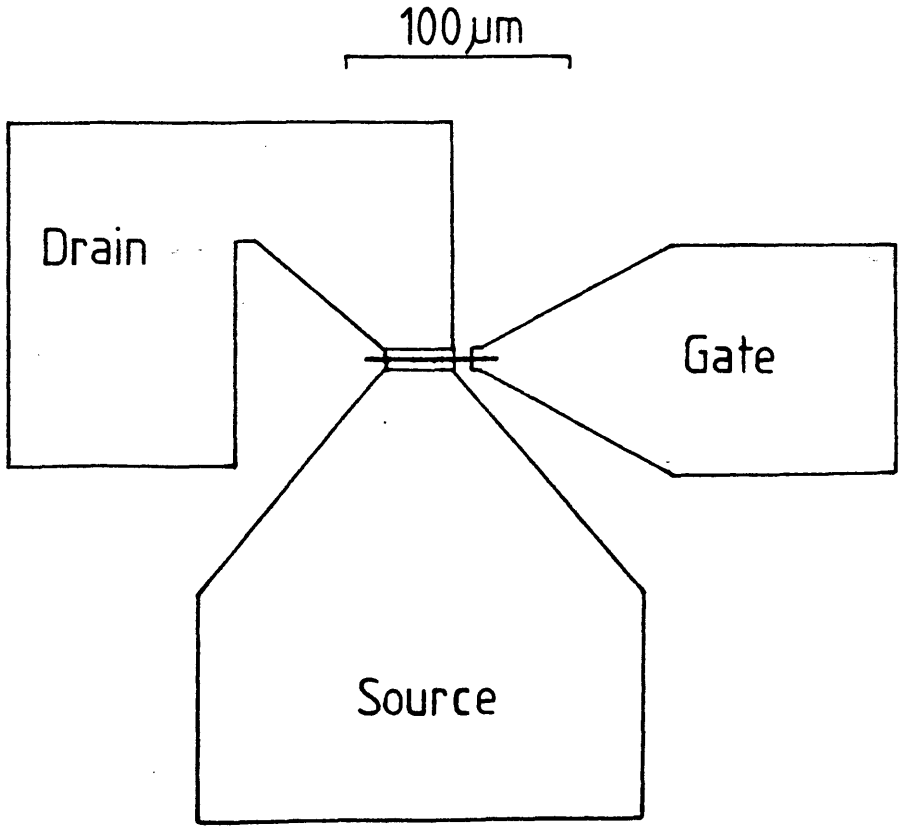


Fig. 4.2 Plan view of a device designed to be suitable for ac testing.

were made to fabricate this type of MESFET.

The geometry of the first sets of MESFETs was similar to the design created by WS Mackie [4.4]. However, these were not suitable for ac testing, due to the unsuitable layout of the devices. Therefore the MESFET design had to be completely restructured, along Plessey guidelines [4.5], to make them suitable for ac testing (fig 4.2). The drain and gate bonding pads of the ac devices were situated directly oppposite one another to allow the device to be bonded into an ac test fixture with the minimum length of bond wire (see sect 4.4). The source bonding pad was made sufficiently large to allow a double wire bond to be made to the source, thus reducing the inductance of the source bond. Parasitic source and drain inductances were reduced by using the tapered contacts shown in the figure.

4.1.2 Device Operation

Long-gate MESFETs (several microns) can be described using a model similar to that used to describe a J-FET [4.6]. In this 'two region' model, the complicated velocity-field curves for GaAs [4.7] are simplified into a region of constant mobility at low electric fields and a region of constant velocity above a certain critical field. In FETs with short gate lengths (< 2μm), a model where full current saturation is assumed below the gate has to be employed. The complicated velocity-field curves for GaAs also have to be taken into account [4.8]. When this model is used, it is found that the saturated velocity is modulated by the width of the conducting channel. Returning to fig. 4.1, the narrowest channel opening is located under the drain end of the gate. As electrons move along the channel, their velocity rises (due to the increased field), reaches a peak and then drops to the saturated velocity at the gate edge. In order to preserve current continuity, because of the narrowing channel and slower moving electrons, electron accumulation occurs in this region. However, as the channel width widens, the electron velocity increases, causing a strong depletion region. In other words, when a large enough voltage is applied to the drain of the device, a dipole layer is formed in the channel, extending beyond the end of the gate. Most of the drain voltage is dropped across

this stationary dipole layer [4.8]. For very short gate lengths, the electrons may not reach an equilibrium condition in the high field region of the device [4.8,4.9]. Electrons entering the high field region are accelerated to twice their peak equilibrium velocity and then after travelling a distance of approximately 1 μm relax to their equilibrium saturated velocity. This "velocity overshoot" effect shortens the transit time of carriers in the high-field region and is expected to improve the high frequency response of short gate length GaAs MESFETs.

When the gate length becomes extremely short (submicron) it is possible that electrons will experience few, if any, scattering events as they pass under the gate. Such a device would be said to be operating "ballistically" [4.10]. A truely ballistic transistor may be difficult to realise in practice since the gate length of the device would need to be shorter than the mean free path of electrons at the operating temperature of the device [4.11]. This implies that devices should be on lightly doped material and operated at low temperatures. In addition the device would have to be operated with low voltages to avoid interband, intervalley scattering of the carriers. Nevertheless, ballistic properties have been observed at room temperature in a vertical FET-type structure [4.12] and near ballistic transport is predicted in sub micron GaAs diodes [4.13]. It is envisioned that FETs with ballistic electron injection operating with switching of only 1ps will be fabricated in the near future [4.14].

The solid substrate MESFETs fabricated for this thesis were not expected to operate ballistically. However, very short gate length transistors are of particular interest for high frequency applications. Considerable effort has been made in minimising the noise figures of high frequency devices [4.15-17] and in fabricating FETs with very short switching speeds [4.2,4.3]. (The high electron mobility transistor (HEMT) has also been developed for very high speed logic [4.18]. More will be said about HEMTs in chap 7).

It was decided to fabricate GaAs MESFETs with gate lengths much shorter than any previously fabricated devices. The

resulting decrease in the gate-source capacitance, coupled with a low source resistance, should have produced very low noise figures and high cut-off frequencies [4.19]. Using the high resolution capabilities of electron-beam lithography it was possible to fabricate extremely short gate-length transistors (55 nm) on a variety of substrates. These devices were all found to operate well at dc, even at the shortest gate lengths. However, the ac measurements (s-parameter) made on a relatively small number of devices did not produce any consistent data which could be used to predict the high frequency performance of the devices.

4.2 MESFET Fabrication

4.2.1 General Description

The starting material for GaAs MESFETs was typically a 6mm by 5 mm wafer of undoped GaAs with an active layer of epitaxially grown n^+ GaAs 50 to 100 nm thick. The coarse patterning of the devices (isolation, contacts, bonding pads) was done using a large exposure frame size of 1.5 mm by 1.2 mm. Each exposure frame contains 9 transistors, and on each wafer there were typically 16 frame exposures. The location of each exposure site on the wafer was determined using the POSITION program [4.4], which calculates the exposing positions on the sample in terms of the goniometer coordinates. The orientation of the wafer, relative to the goniometer axes, is calculated in POSITION so that the exposed frames are parallel to the axes of the wafer. This enables scribe lines to be drawn parallel to the GaAs crystal axes for the eventual division of the wafer. The locations of the exposed frames on a wafer, determined using POSITION, are shown schematically in fig. 4.3. The offset between the goniometer and specimen axes was exaggerated in this figure to illustrate the positioning technique.

Before studying the GaAs MESFET fabrication process in detail, the techniques used for aligning one pattern level to another will be described.

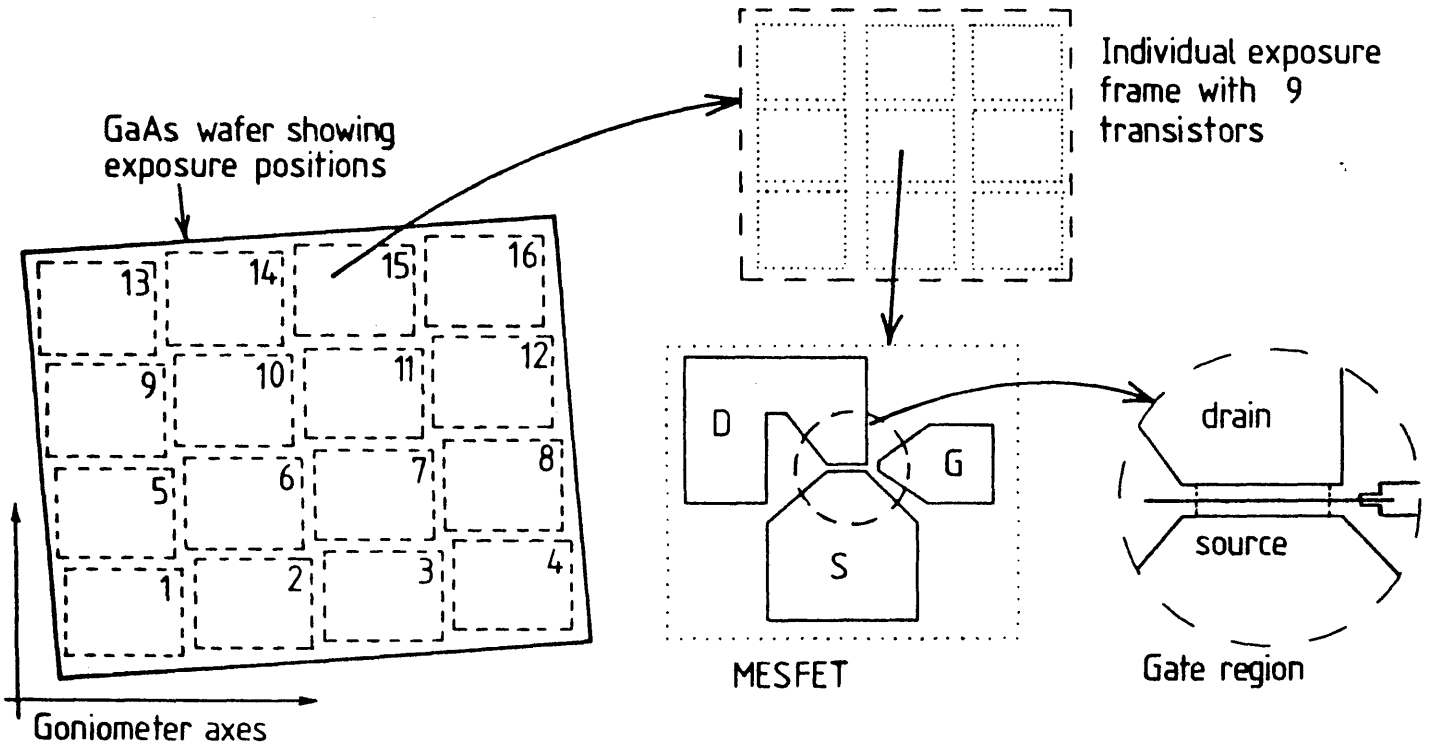


Fig. 4.3 Schematic diagram showing how the exposure frames are located on a wafer using the POSITION program. The insets show that each exposure frame contains nine devices.

4.2.2 Alignment Techniques

There are at least four pattern levels required for the fabrication of GaAs MESFETs; isolation, ohmic contacts, bonding pads and gates. A reliable technique was developed for aligning the coarse features (isolation, contacts and pads) relative to previously deposited registration marks, to within 0.5 μm over a 1.5 mm frame. A similar technique was used for alignment of the gate exposures relative to markers incorporated into the ohmic contact pattern.

4.2.2.1 Alignment Test

The following experiment was carried out to test the accuracy of the alignment technique. The pattern shown in fig. 4.4 was defined (by e-beam exposure and lift-off) at 4 locations (determined using POSITION) on a 3.5 by 3.0 mm GaAs wafer. The pattern consists of the standard registration marks for a device chip along with a set of crosses which were used in the alignment test. The object of this experiment was to see how accurately another set of crosses could be deposited over the existing crosses using the registration marks for alignment.

4.2.2.2 Coarse Alignment

After depositing the registration marks and the first set of crosses, the wafer was recoated with resist and then placed into the SEM for alignment and exposure of the second set of crosses. The rough coordinates of the exposure sites were determined using POSITION. When the sample had been moved to the first exposure site a coarse alignment pattern was scanned once to observe how the specimen was positioned relative to the scanned pattern. The alignment pattern consisted of a horizontal, 10 pixel pitch grating which was scanned with a dwell time of 2.0 μs per pixel (ie as fast as the DACs in the scan generator could be driven). The partial outline of the large blocks of the registration pattern were also scanned with a dwell time of 20 μs per pixel. This meant that the outline pattern appeared brighter than the scanned raster on the VDU screen.

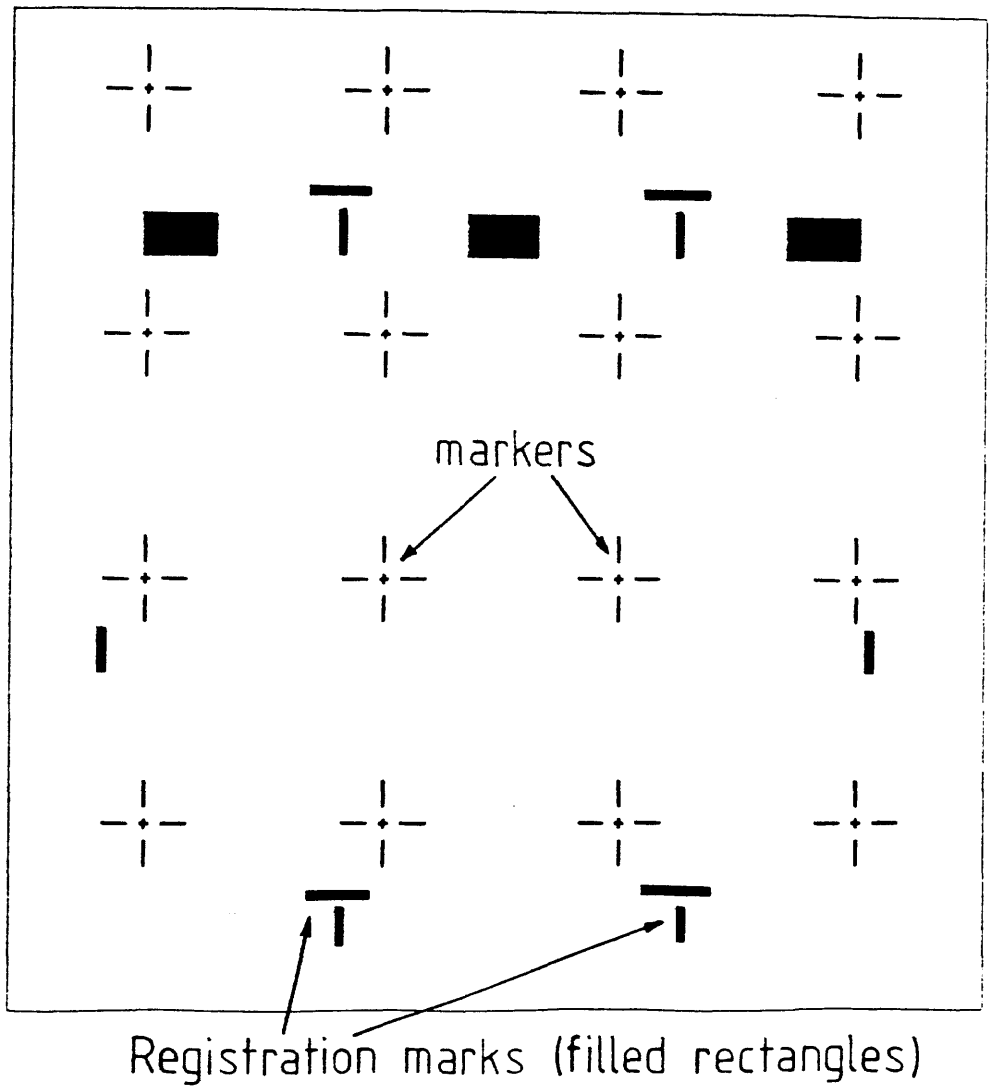


Fig. 4.4 Pattern used in the alignment experiment. The registration marks (solid pattern) are the standard marks for an ac device chip. The crosses were used to test the accuracy of the alignment technique.

The object of the coarse alignment scan was to ensure that the scanned outline pattern corresponded to the registration blocks. The first coarse alignment scan often showed significant offsets in x, y and rotation. These offsets were corrected by dead reckoning (ie with no image on the SEM VDU) and then checked by a second coarse alignment scan. It was not generally necessary to repeat the alignment scan a third time (the exposure of the resist began to be significant when 3 or more coarse alignment scans were used). At subsequent exposure sites only one coarse alignment scan was normally required as the rotation did not have change significantly and the x and y offsets, determined from the first alignment, could be added to the exposing coordinates calculated using POSITION. With practice, the coarse alignment scan could often be avoided in all but the initial exposing position. The patterns were then aligned by the fine alignment scan only.

4.2.2.3 Fine Alignment

The fine alignment marks are the "T" shapes in the registration pattern shown in fig 4.4. Fine alignment was achieved by scanning rectangles (2 us dwell time) around these "T" shapes as shown in fig 4.5. This means that the sample is correctly aligned when no part of the "T"s are visible. At the first exposure site on a wafer, several fine alignment scans were often required to adjust the x, y and rotation controls as well as the fine x and y "varimag" controls (see sect 4.2.4) to achieve proper alignment. However, at subsequent exposure positions alignment was achieved with as few as 2 scans of the fine alignment pattern. A low number of scans is desirable because it avoids unnecessary exposure of the resist which could obscure the registration marks for subsequent pattern levels.

4.2.2.4 Results

The micrograph shown in fig 4.6. shows the two sets of crosses patterned in the alignment test. The first set of crosses, which are the shorter of the two, were metallised with Au (100 nm). In order to obtain a high contrast in the SEM, the second set of crosses was metallised with NiCr (100 nm). It can

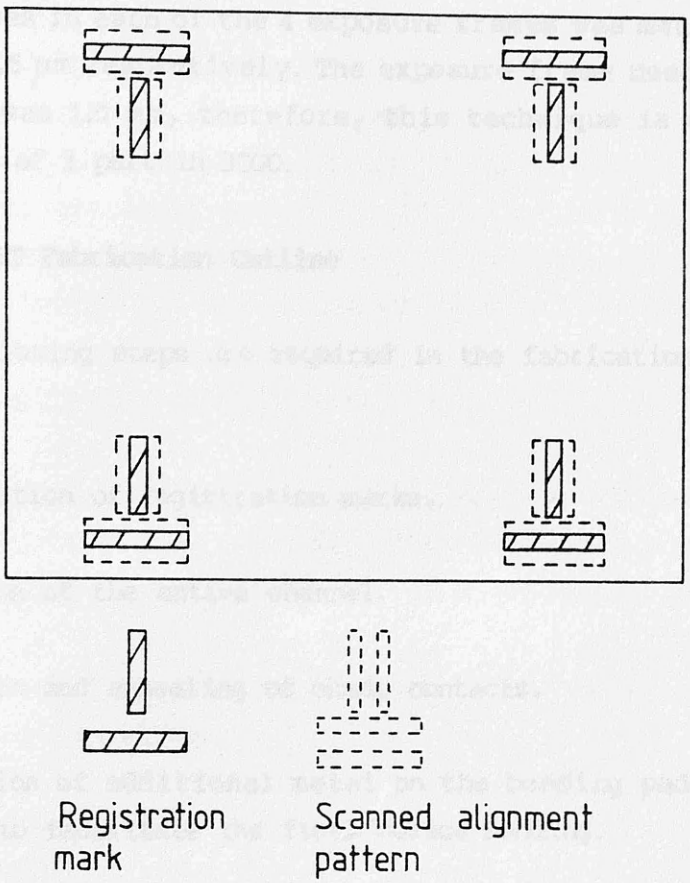


Fig. 4.5 Schematic of the fine alignment technique. The sample is correctly aligned when the markers disappear completely from the scanned alignment pattern.

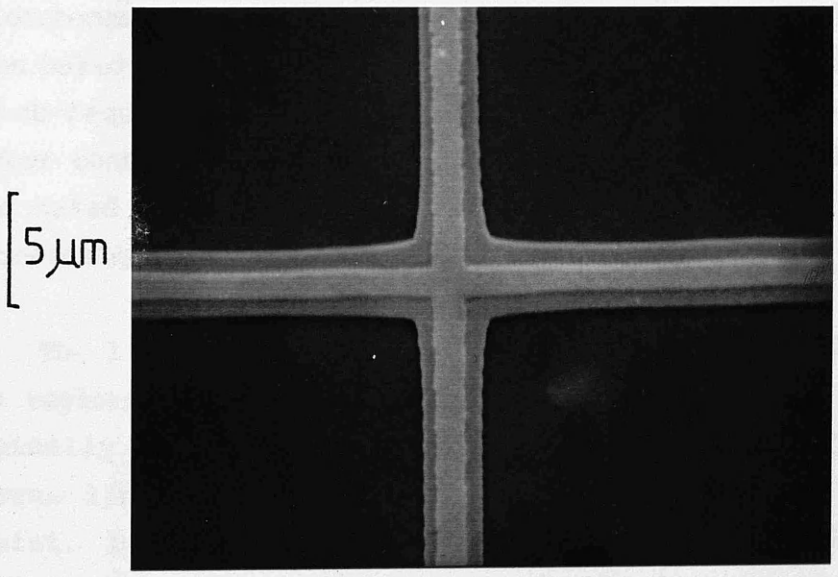


Fig. 4.6 SEM Micrograph of the two sets of crosses deposited in the alignment test.

be seen from fig 4.6. that the two sets of crosses are aligned almost perfectly. The average x and y offsets measured from all of the crosses in each of the 4 exposure frames was measured to be 0.6 and 0.5 μm respectively. The exposure frame used in this experiment was 1.5 mm, therefore, this technique is good for registration of 1 part in 3000.

4.2.3 MESFET Fabrication Outline

The following steps are required in the fabrication of GaAs MESFETs

a) The deposition of registration marks.

b) Definition of the active channel.

c) Deposition and annealing of ohmic contacts.

d) Deposition of additional metal on the bonding pads of the transistors to facilitate the final device bonding.

e) Gate patterning with appropriate recessing for optimised device transconductance.

The resist used for patterning levels a) to d) was 1 μm of low molecular weight PMMA (185 000). The PMMA (15% in chlorobenzezne) was spin coated onto the wafers at 5000 rpm and then baked for more than 2 hours at 180 ^{o}C. For pattern levels which required wet etching, for example the GaAs deoxidation before contact deposition or the mesa isolation step, the resist was baked overnight to ensure good adhesion during the wet processing (Sect.1.4.2).

The 1 μm film of PMMA was exposed by a 0.5 μm (0.25 μm for the registration pattern) electron beam. The exposure dose was typically 300 uC/cm^2 for large areas and 320-350 μC/cm^2 for narrow lines. 1:1 MIBK:IPA (23 ^{o}C) was used to develop the resist. Development times were all 60 seconds except for the ohmic contact pattern where a 45 sec development time was used to avoid excessive development of the narrow source-drain gaps. All

the metallic pattern levels (registration, contacts and bonding pads) were defined by lift-off.

A typical layout of a device wafer is shown in fig 4.7. A row of TLM chips (chap. 2) was generally included for finding the optimum annealing temperature for the ohmic contacts. When the wafer had been processed up to the ohmic contact metallisation step, this row of test chips could be removed from the wafer and divided into individual test chips containing 4 TLM structures. These were then annealed at different temperatures to find the optimum annealing temperature for the device wafer.

In the following sections a complete description of the device fabrication steps is given. The TLM test patterns were patterned simultaneously and required no additional processing steps.

4.2.4 Registration Marks

The registration marks used for alignment of one pattern level to another are shown in fig. 4.4. The registration marks normally consited of 85 nm AuGe/15nm Ni/20nm Au. This metallic system was chosen so that the samples could be annealed at low temperature and ohmic contacts formed between the markers and the semiconductor. These ohmic contacts could then be used in the mesa isolation step described in section 4.2.5.

It was already mentioned that the exposure coordinates of the wafer, in terms of goniometer coordinates, were determined using the POSITION program. The standard procedure for all the exposure levels, after loading the wafer into the SEM was:-

1) Focus at the exposing spot size on the edge of the Faraday cup (used for beam current measurement) on the specimen holder. Then, move the specimen until the Faraday cup is in the center of the VDU screen, increase the magnification to 80 000 and measure the beam current.

2) Reduce the spot size to 16 nm and magnification to X 20, and move to the left hand edge of the wafer. Find a piece of debris

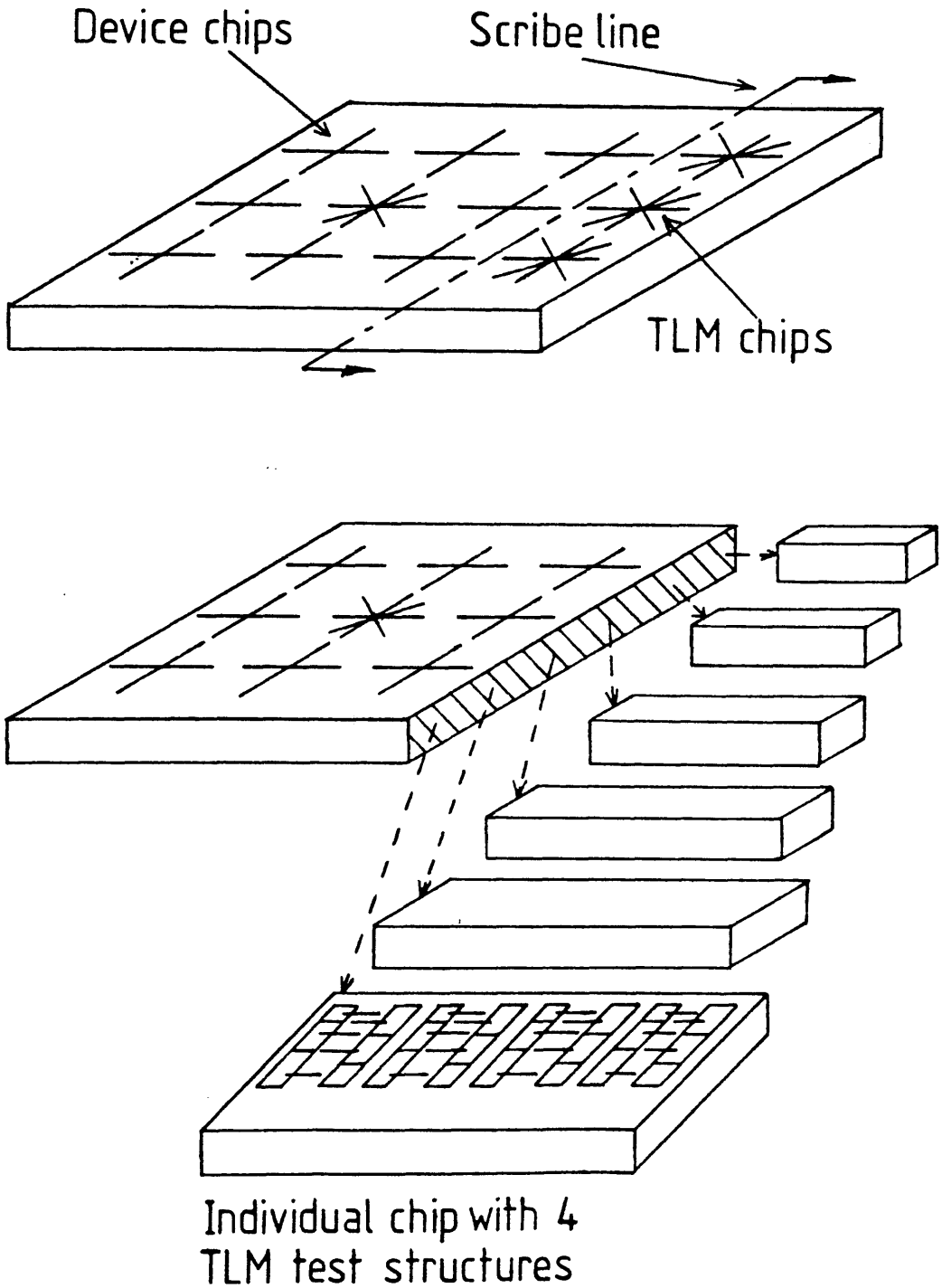


Fig. 4.7 Schematic representation of a typical device wafer with a row of TLM test patterns which can be removed and individually annealed (temperature optimisation) after the ohmic contact depositon step.

on the wafer. Increase the magnification to X 2500 and then increase the spot size to the diameter to be used for the exposure and refocus on the wafer.

3) Reduce the magnification and spot size to X 160 and 16 nm respectively and locate the top left hand corner of the wafer in the centre of the VDU screen and note the goniometer coordinates. Repeat with the bottom left hand corner of the wafer.

4) Use POSITION to determine the wafer exposure coordinates in terms of goniometer coordinates. The program takes the coordinates from the sample file and converts them into coordinates relative to the bottom left hand coordinate of the wafer taking into account the misalignment of the goniometer and specimen axes. The exposure coordinates can then be recorded from the output of the POSITION program.

5) Return magnification and spot size to correct settings and expose sample.

When the alignment marks were exposed the x and y "varimag" controls were both set to 2.0. The "varimag" control is used to adjust the frame size independently in the x and y directions. The reason for setting a nonzero value was to ensure that the frame size can be adjusted both above and below the set value. This means that if there is a drift in the frame size for subsequent exposure levels, the exposure frame size can be adjusted until it is exactly the same as previously patterned frames.

Before spinning the resist for the mesa isolation step, the registration marks were annealed for 1 minute at 320 ^{o}C. This ensured that ohmic contacts would be formed between the registration marks and the GaAs (for use in the isolation step). However, because a low temperature anneal was used, the alignment marks still had a high contrast when observed in the SEM.

4.2.5 Isolation Level

In order to define the active source-drain channel and to

isolate devices from one another either mesa isolation or isolation by boron implantation was used. The majority of the devices fabricated were isolated using the former technique. The channel widths of the devices varied between 4.1 and 34 μm. The wider channel devices were prefered for ac testing due to their lower channel resistances.

4.2.5.1 Mesa Isolation.

Mesa isolation involves etching away the conducting epi-layer, through a PMMA mask, leaving an island of active material on which the device is fabricated. The mesa isolation pattern used for the MESFETs is shown in fig 4.8. (the dashed pattern). It can be seen that, instead of removing all of the epi-layer except for the source-drain channel, in these devices the active mesa was defined by etching narrow grooves through the active layer. This has the desired effect of confining all of the current to the active island of material between the source and drain contacts. The reason for etching grooves rather than etching away all of the unwanted epi-layer was to save on e-beam exposure time. However, the active layer below the gate pads was removed. This was to make sure that the source-gate capacitance was kept to a minimum.

At selected exposure sites on the wafer, windows were exposed over the coarse alignment blocks of the registration pattern. This was to create openings in the resist so that the pads could be probed for monitoring the isolation etch.

Etching

Before commencing the etching, the current that flowed between registration blocks, at a given voltage (typically 2 V), was measured. The mesa etching was then carried out, using a slow etch to remove the GaAs not protected by the resist mask. Every 10 seconds the wafer was removed from the etch solution, rinsed in deionised water and blown dry. The current between pads was remeasured after each etch, for the same applied voltage (2V). Because each of the pads used for current monitoring was completely surrounded by an etched groove, (the blocks formed

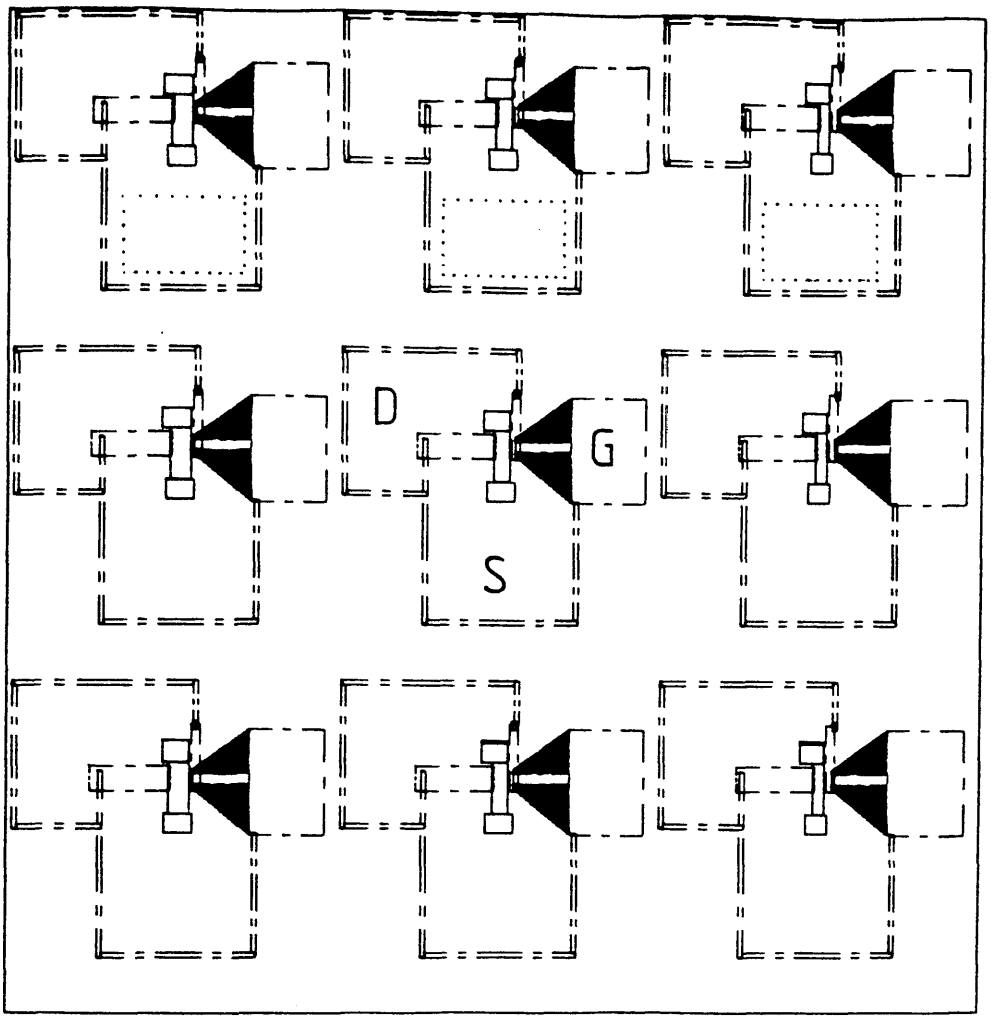


Fig. 4.8 Isolation Level. The dashed pattern is the mesa isolation level. Grooves are etched through the epi-layer around the source and drain contacts, but, all of the epi-layer is removed from beneath the gate. The positions of the registration blocks used for monitoring the mesa isolation are also shown. The solid lines represent the ion implantation mask pattern. Only the active drain-source channel region of the devices is protected during implantation.

part of the source pad of 3 of the divices) the current between pads diminishes as the etching progresses. When the depth of the etched grooves slightly exceeds the thickness of the active layer, the current between pads becomes negligible. Etching was stopped when less than 1 μA flowed between the pads.

The solution used for the mesa isolation etch was 1:8:100 H_2SO_4:H_2O_2:H_2O. Typical etch times for an 85 nm epi-layer were of the order of 30 seconds. Before each etch, the wafer was immersed in IPA then rinsed in deionised water before placing it in the etch solution. The reason for this was to wet the PMMA to ensure that the etch solution would get into the relatively narrow openings in the resist.

4.2.5.2 Boron Isolation

Boron isolation was used as an alternative method of confining the current to an active channel between the source and drain contacts of a device. The principal of this technique is to protect the active part of the device with a thick, removable mask and then to implant the wafer with boron ions. The implanted boron effectively renders the GaAs, not protected by the mask, semi-insulating. This is due to the formation of a large number of efficient, deep level traps within the GaAs (sect 5.4.)

A detailed description of the masking technique for boron implantation is given in chapter 5 (metal on polymer masks). Essentially these masks consist of a thick primary metallic mask on a polymer parting layer which can be dissolved in a solvent, allowing easy removal of the mask after implantation [4.20].

The pattern for the MOP masks used for MESFET fabrication is shown in fig. 4.8 (solid pattern). These masks were patterned using the novel MOP mask fabrication technique described in Sect. 5.4.5. [4.21]. The MOP masks were aligned to the registration marks deposited previously. The masks consisted of 0.8 μm of germanium on a 0.35 μm layer of polyimide. Once the masks had been fabricated, the wafers were sent to the SERC Microfabrication Facility at Edinburgh University for

implantation. The ion dose was 2 x 10^{13} ions/cm^2 and the implantation energies were 40 and 80 keV. This was sufficient to isolate the 85 nm epi-layers, however, for layers up to 100 nm thick an additional higher energy (120 keV) implant was required.

Boron isolation was the more suitable method to use for the very short gate length devices because it avoids the need to deposit the gates over a step onto the active channel region. The problem with patterning a gate over the mesa is that at the mesa edge the gate tends to be thinner than on the mesa itself. This is due to a thickening of the resist in the vicinity of the mesa edge which results in a narrower developed window in the resist at this point. The use of ion implantation is also advantageous because it reduces the effects of backgating [4.22] which will be discussed in sect. 4.3.4. However, as this isolation process was not fully developed until near the end of this project, only a few MESFET devices were actually made using boron isolation.

4.2.6 Ohmic Contact Level

Fig. 4.9 contains the pattern for the ohmic contacts level. In the region of the source-drain gap, the contacts were exposed with a reduced dose of 250 $\mu C/cm^2$. This was because the two contacts were patterned close to one another (of the order of 2 μm). If a higher exposure dose was given to the contacts, it would be difficult to maintain the small contact separation because of the proximity effect of the closely spaced patterns [4.23].

Care had to be taken to avoid exposing the resist during the alignment of the exposure frame to the registration marks on the wafer. This meant that, at most, 1 coarse alignment scan and 2 fine alignment scans could be used for locating and correctly positioning the sample. The reason for not wanting to expose the resist around the registration marks was to avoid obscuring the markers by the ohmic contact metallisation, hence causing problems with the final processing step at this scale (the bonding pads). However, all was not lost if the resist did become exposed. The coarse alignment scan could be used to

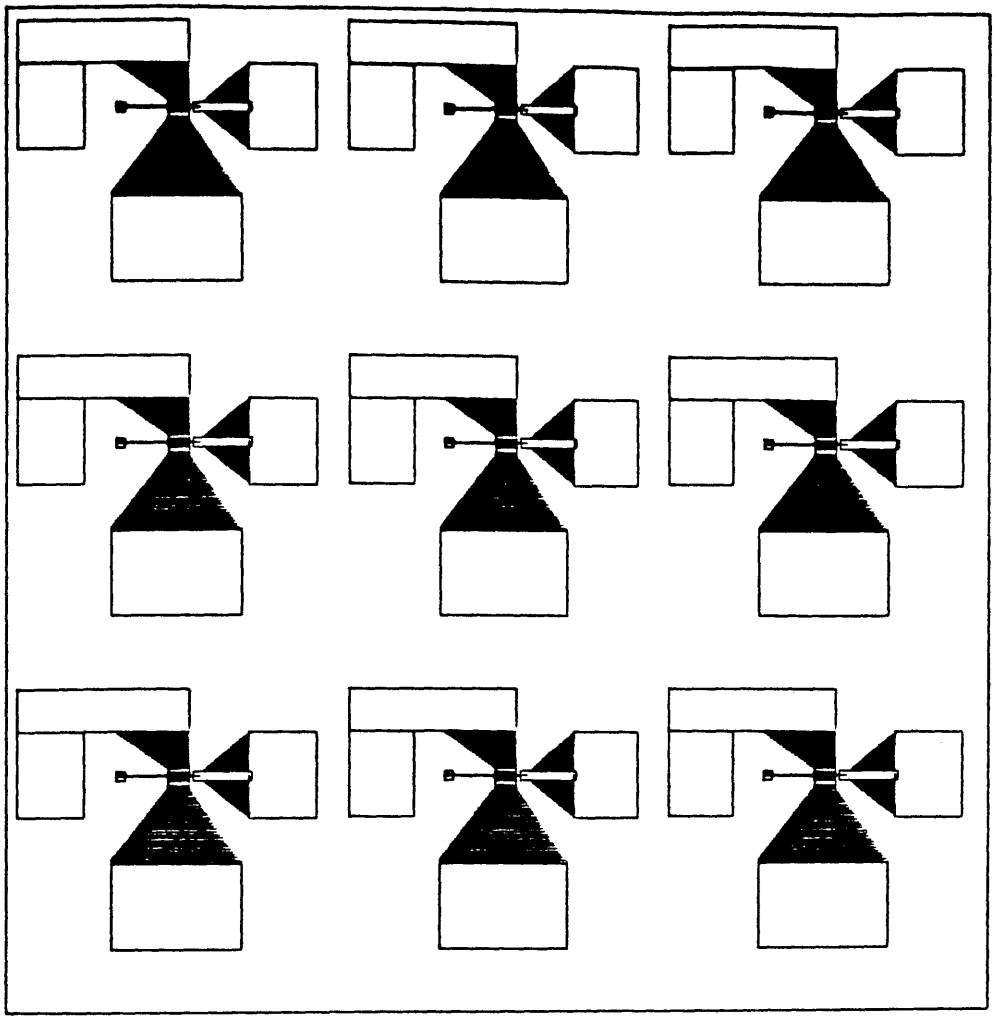


Fig. 4.9 Ohmic contact level. A detailed view of the drain-source region of these devices is given in fig. 4.13.

locate the original registration blocks, which were visible through the contact metallisation. The resolution obtained using the coarse alignment scan (approximately 3 μm) was sufficiently accurate for the bonding pad level.

The metallisation for the ohmic contacts was typically 85 nm AuGe (88:12) with a 150 nm Ni layer and a 20-40 nm Au capping layer. This composition was suitable for low temperature annealing (Chap. 2). Before placing the sample in the vacuum system for metallisation, the exposed areas of GaAs were cleaned for 1 minute in 5 % ammonia solution to remove any surface oxide from the wafer. The samples were then thoroughly blown dry in nitrogen and loaded into the evaporation system. It was found that this etch greatly greatly improved the adhesion of the contact metal to the GaAs.

At this stage the column of TLM test patterns at the right hand edge of the wafer was removed and divided into individual test chips. These were annealed at different temperatures to find the optimum annealing temperature for the contact system. The device chip was then annealed at the optimum temperature.

4.2.7 Bonding Pad Level

After the ohmic contacts had been annealed it was essential to deposit a further metallic layer on the bonding pads to ensure that reliable bonding of the devices could be carried out. The bonding pad pattern is shown in fig 4.10.

Initially the pads consisted of a 100 nm layer of NiCr and a 200 - 300 nm layer of Au. The NiCr ensured good adhesion to the ohmic contact and the thick Au layer was required to facilitate bonding of the devices. However, it was found that when these bonding pads were probed (ie contact was made to the top Au layer but not directly to all of the metal layers of the device) it was sometimes difficult to get current through a device. This implied the presence of an insulating layer deposited with the bonding pads. This could have arisen from the incorporation of residual oxygen from the evaporation chamber into the first layers of NiCr evaporated onto the samples. The conduction of

the bonding pads did not however improve even when a shutter was placed over the the NiCr evaporation evaporation source for the first few seconds of the evaporation.

To improve the conduction of the pads, the NiCr layer was replaced by a 100 nm layer of AuGe (proportions approximately 88:12 but not weighed out accurately). AuGe had been shown to have a better adhesion to GaAs then pure Au, so it was envisaged that it would also have better adhesion to annealed contacts. When the pads were fabricated it was found that the current which could be passed through a device with bonding pads was the same as the current through the device before the bonding pads were deposited. Therefore these pads were electrically superior to the NiCr/Au pads used previously. It also turned out that it was far easier to bond to the AuGe/Au bonds than to the NiCr/Au. All of the bonds on eight devices (32 bonds - sect 4.4) were successfully bonded at Plessey (Caswell) for ac testing. With the NiCr adhesion layer, an average of 1 out of every 10 bonds failed resulting in about 40 % of the actual devices being rendered unusable. Fig. 4.11 contains a schematic of an individual device fabricated up to this level and an SEM micrograph of a device fabricated up to the same level.

4.2.8 Gate Level

The final step in the fabrication of MESFETs was to pattern the Schottky gates between the source and drain contacts. To achieve the high resolution required for fabricating very short gate length devices, the gates were individually aligned and exposed using a frame size of 50 by 38 μm and a 16 nm diameter beam.

4.2.8.1 Gate Resist

A high resolution bi-layer resist system was used for patterning the gates. This was made up of a layer of high molecular weight PMMA (350 000) 170 nm thick, on a layer of low molecular PMMA (185 000) 100 nm thick. When the resist is developed, the bottom layer develops further laterally because it is more sensitive. This produces an undercut in the resist which

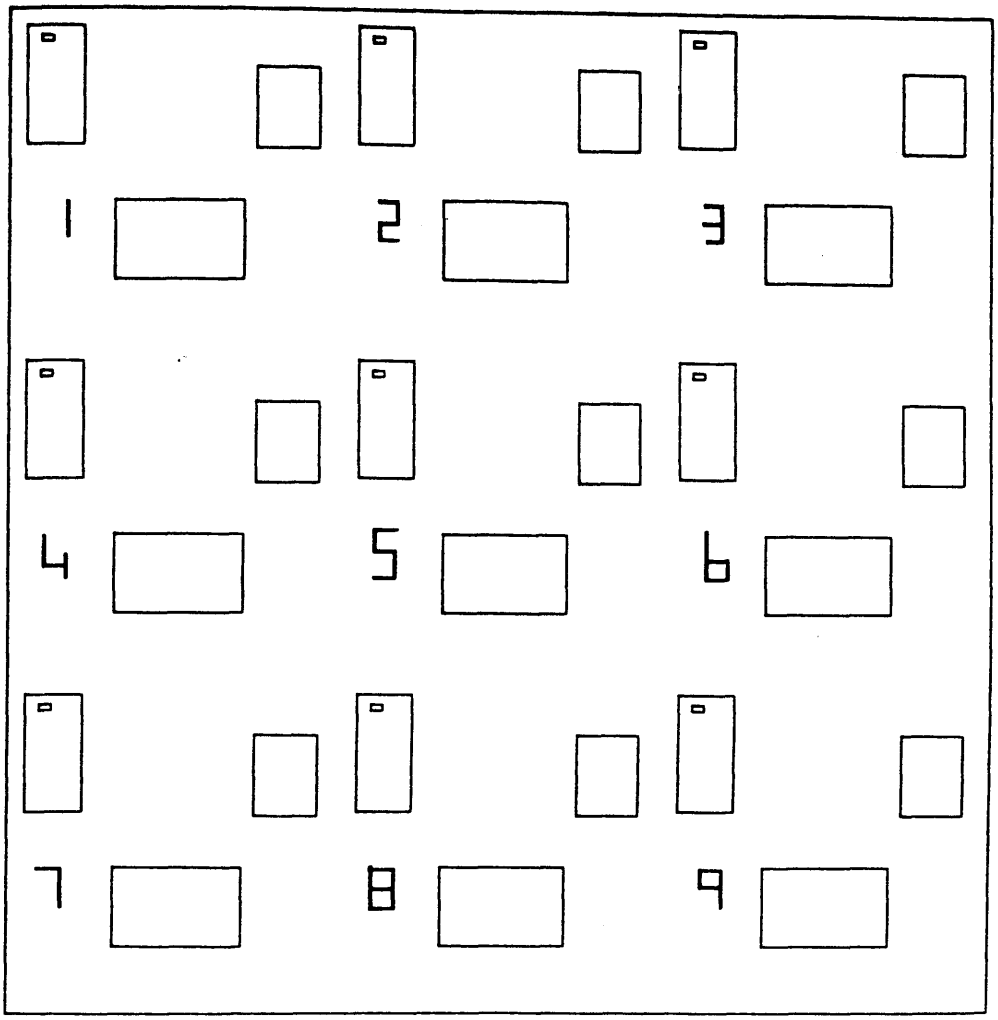
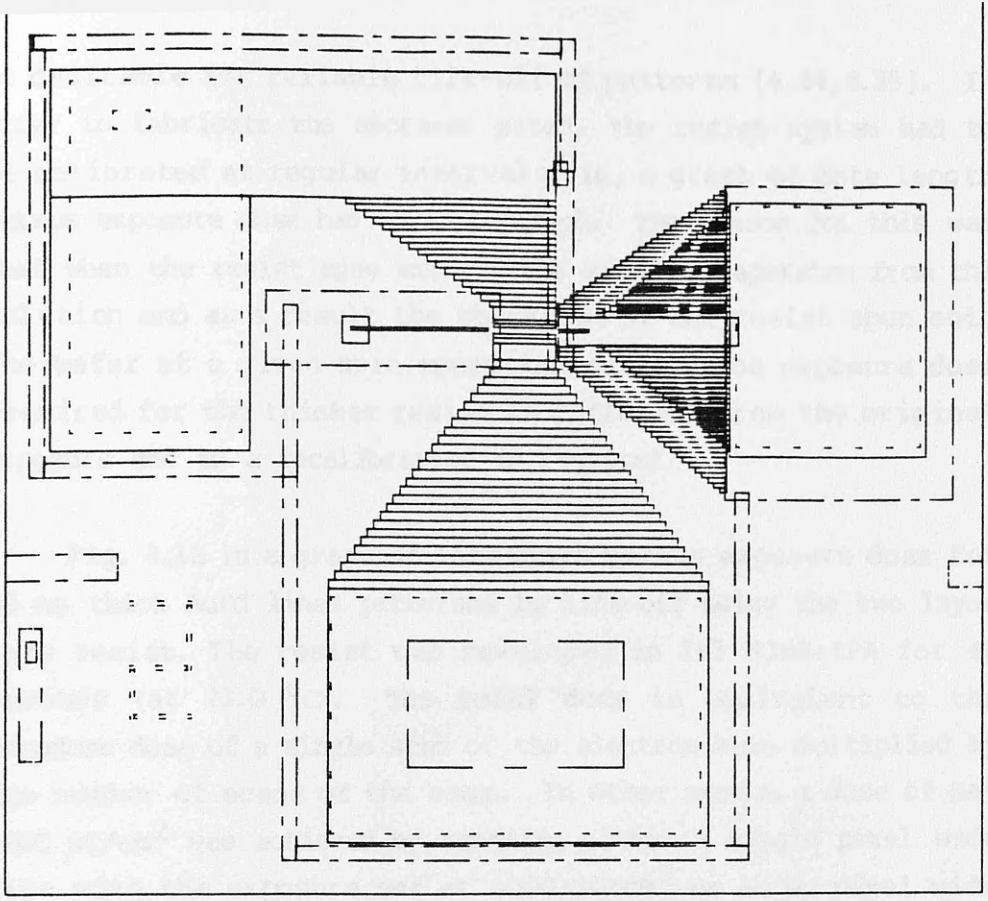


Fig. 4.10 Bonding pad level. A set of numbers is patterned at the same time as the bonding pads to facilitate device identification when the chip is eventually broken up into individual device chips.



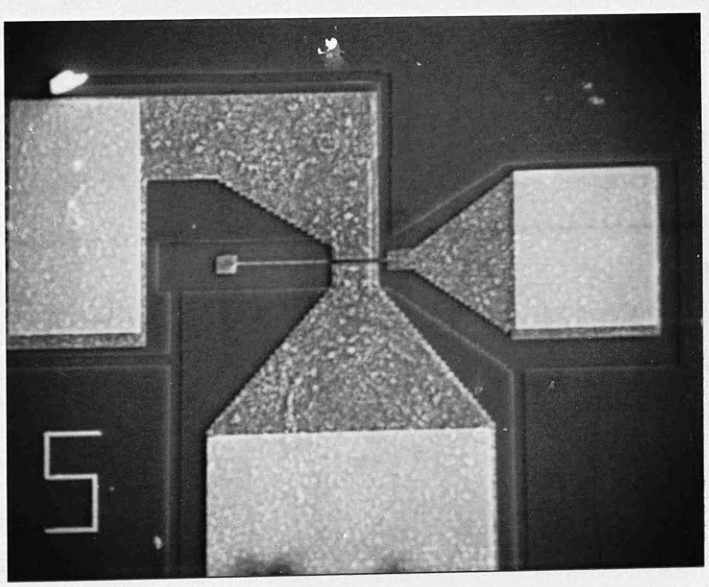
(a)

Registration marks

Mesa level

Ohmic contact level

Bonding pads & device numbers



(b)

Fig. 4.11 a) All the pattern levels up to the bonding pad level shown for an individual device. b) An SEM micrograph of a device fabricated to the bonding pad level.

is desirable for reliable lift-off of patterns [4.24,4.25]. In order to fabricate the shortest gates, the resist system had to be calibrated at regular intervals (ie, a graph of gate length versus exposure dose had to be plotted). The reason for this was that when the resist ages some of the solvent evaporates from the solution and as a result the thickness of the resist spun onto the wafer at a given spin speed increases. The exposure dose required for the thicker resist is different from the original exposure and so a recalibration is required.

Fig. 4.12 is a graph of linewidth versus exposure dose for 80 nm thick AuPd lines patterned by lift-off using the two layer gate resist. The resist was developed in 1:3 MIBK:IPA for 40 seconds (at 23.0 ^{o}C). The total dose is equivalent to the exposure dose of a single scan of the electron beam multiplied by the number of scans of the beam. In other words, a dose of say 4000 $\mu C/cm^2$ was achieved by scanning either a single pixel wide line with the exposure set at 4000 $\mu C/cm^2$ or a two pixel wide line with with the exposure set at 2000 $\mu C/cm^2$. It can be seen from the graph that the linewidth was independent of the number of electron scans (at a given total dose) for 1, 2 and 4 pixel wide lines but there was a slight increase when a 6 pixel wide line was scanned. The shortest gate lengths (55 nm in the actual device) were exposed by 2 scans of the beam with the exposure dose set at 1500 $\mu C/cm^2$.

When the gate resist had been baked, the wafer was scribed and divided into individual chips for gate patterning.

4.2.8.2 Gate Alignment

The MESFET gates were aligned to the markers contained within the ohmic contact level. Fig 4.13 contains an enlarged view of the contact pattern showing these alignment marks approximately as they appear on the SEM screen for gate alignment. The alignment procedure was as follows:-

1) The bottom of the source pad of each transistor was located at low magnification (X 160).

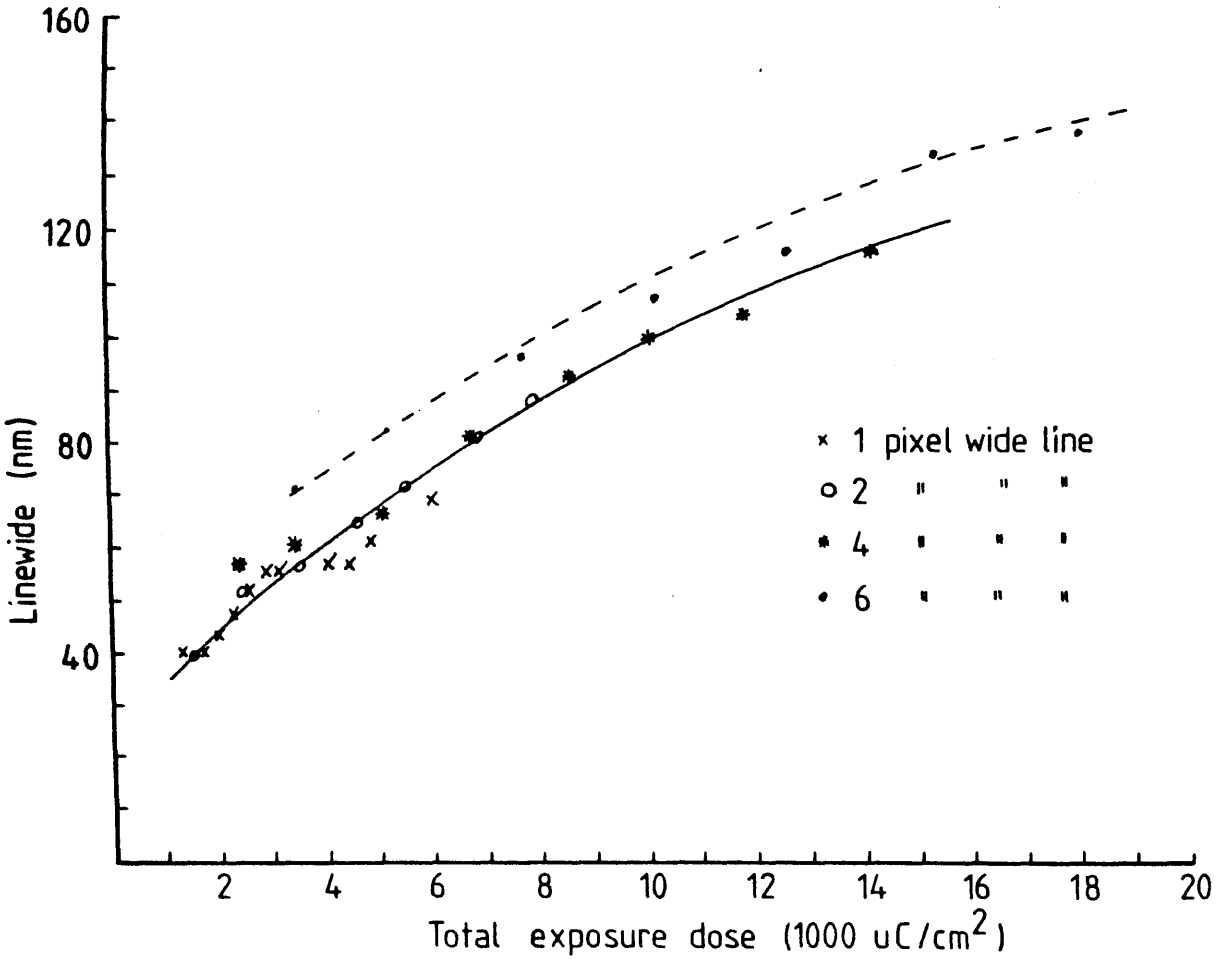


Fig. 4.12 Graph of gatewidth versus total exposure for 1, 2, 4 and 6 pixel wide gates patterned using a high resolution two-layer resist.

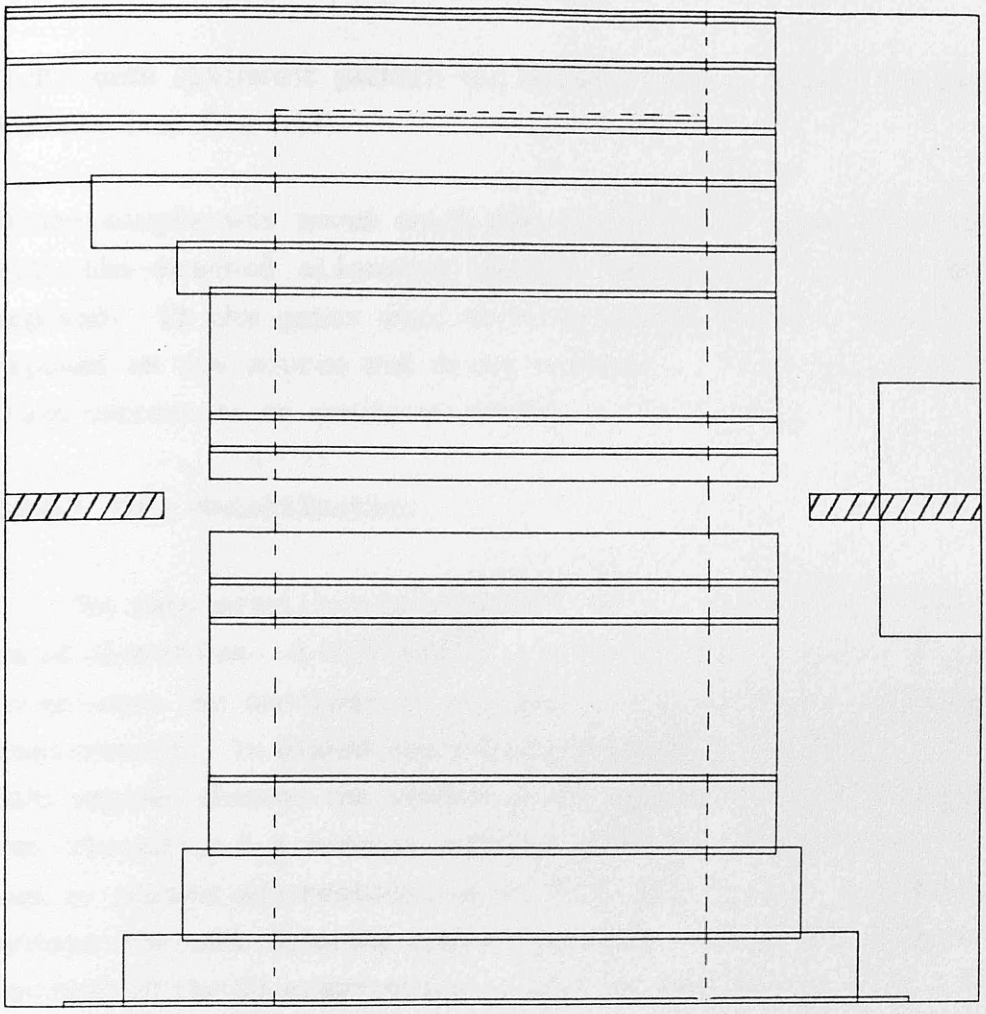


Fig. 4.13 Detailed view of the drain-source region of the ohmic contact level, showing the alignment marks used for positioning the gate.

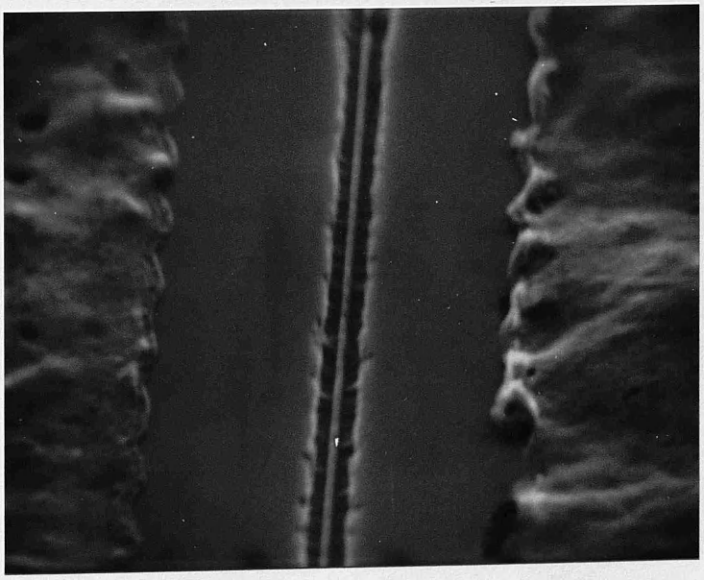


Fig. 4.14 SEM micrograph of a 0.1 um recessed gate MESFET.

2) With the beam blanked, the sample was moved down by a fixed amount (approximately 0.2 mm) equal to the distance between the bottom of the device and the gate region.

3) The gate alignment pattern was scanned once to locate the gate markers (see fig 4.13).

4) The sample was moved until the registration marks coincided with the scanned alignment pattern whereupon the gate was exposed. If the gates were to be recessed windows were also exposed on the source and drain contacts. These allowed the drain current to be monitored during the recess etch.

4.2.8.3 Gate Metallisation

The gate metallisation consisted of 30 nm of titanium and 40 nm of aluminium. A thin AuPd layer (20 nm) was also evaporated to enhance the contrast of the gates in the SEM for linewidth measurement. In planar devices (no recess), the surface of the GaAs exposed through the window in the resist for the gate stripe was cleaned in 5 % ammonia solution prior to evaporation. This was to remove any residual oxide from the surface in order to produce the best Schottky contact possible. During the first few seconds of the Ti evaporation, a shutter was used to shield the specimen from the incident metal. When Ti is evaporated, the first metal to be boiled off absorbs any residual oxygen within the vacuum chamber. Therefore, a shutter has to be used to prevent any of the oxidised Ti from reaching the sample.

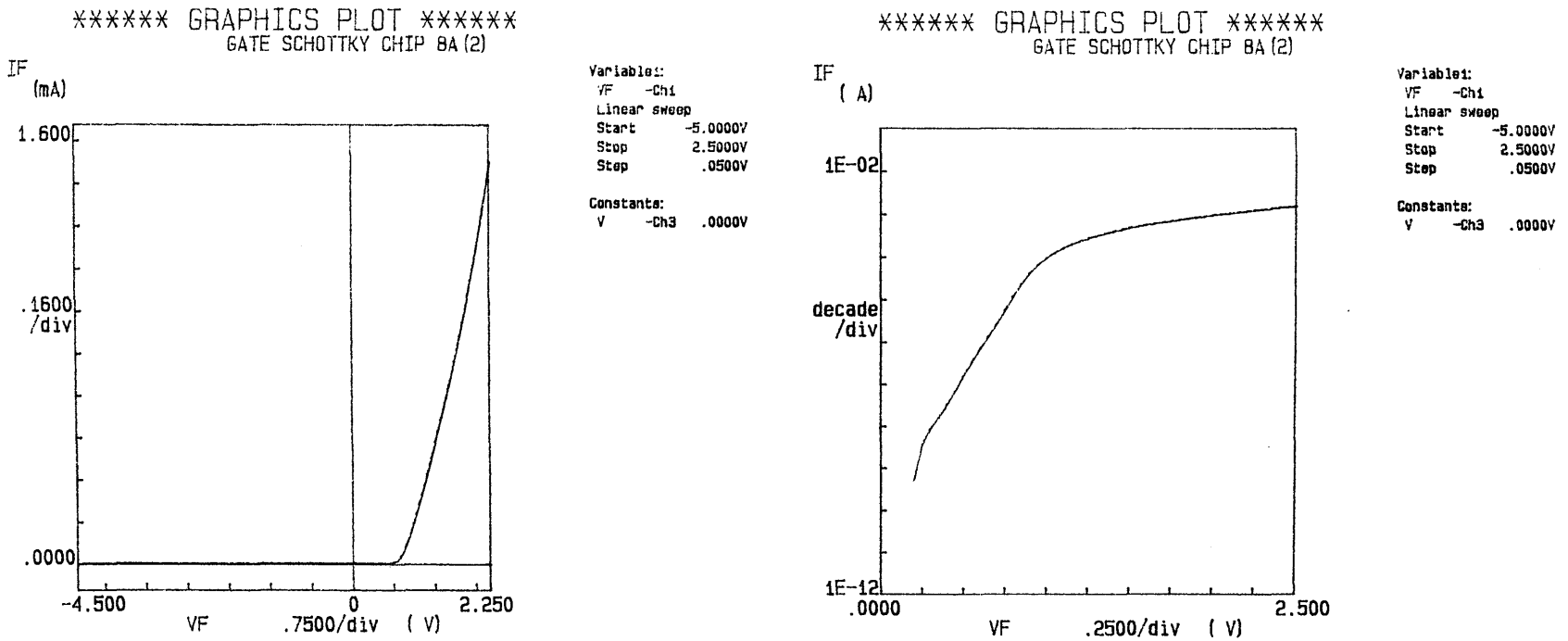
However, most of the gates in the devices fabricated for this thesis had to be recessed in order to pinch-off the channel completely. Recessing was carried out by etching the GaAs through the windows opened in the resist for defining the gates. After etching a recess in the GaAs the gate metal was deposited through the same resist mask, therefore, the gate recessing and the gate metallisation were self aligned. The etch used was a proprietry Plessey etch which, unlike many other GaAs etches, was designed to leave the surface of the etched material oxide-free. An SEM micrograph of a completed, recessed gate, device is shown in fig 4.14.

It was difficult to obtain consitently good Schottky characteristics for gates fabricated on highly doped material. However, when care was taken in their preparation reasonable results could be obtained. Fig. 4.15 shows the I/V characteristics of one of the better gates (both I_d and $Log(I_d)$). From these curves the ideality factor, n, was determined to be 2.60 and the barrier height 0.88 [4.26]. The value of n is rather high but the barrier height is in good agreement with the expected barrier height of Ti on GaAs [4.27]. The best gates had a reverse breakdown of 30 volts, but, the average was -5 to -10 volts.

4.2.8.4 Gate Recessing

The amount of recessing was monitored by measuring the saturated drain current after the sample had been etched for short periods of time. For different device material the optimum recess current for maximum transconductance was determined experimentally.

Fig 4.16 contains the dc output characteristics from MESFETs (0.1 μm gate length) fabricated on the same material (85 nm VPE wafer) but with different recess depths. The amount of recessing is expressed in terms of the reduction in the saturated drain current. DC output characteristics were obtained from a planar device (no recess), and devices where the drain current had been reduced to 0.94, 0.88 and 0.72 times the unrecessed current. The maximum transconductances obtained from these devices were 77, 109, 167 and 192 mS/mm respectively (transconductance is defined as Id/ Vg and is expressed per mm of gate width). It transpired that the optimum recess depth for this particular wafer occured when the drain current was reduced to 75 % of the unrecessed value. At this point g_m was of the order of 240 mS/mm. Below the optimum recess depth, the transconductance is low because the channel is too thick to be pinched of by the voltage applied to the gate. When the recess is too deep, the drain current is reduced and as a result the transconductance of the device is also reduced.



a)

b)

Fig.4.15 I/V Characteristics of a Ti/Al gate. a) Forward and reversed biased gate (linear IF) b) Forward biased gate (log IF) for barrier height and ideality factor calculations.

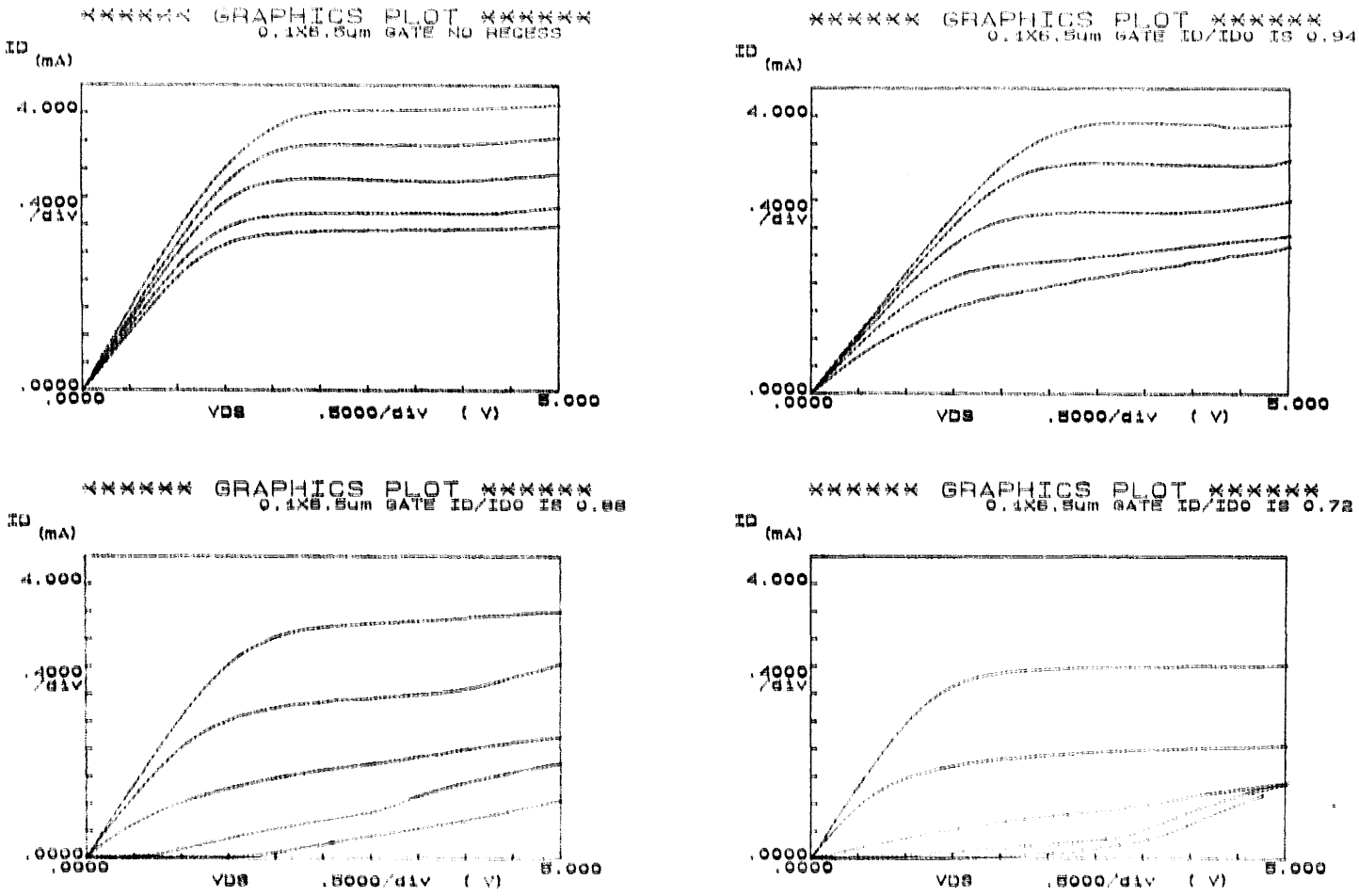


Fig 4.16 I/V Characteristics recorded during a recess optimisation experiment. The transconductance of devices a) to d) are 77, 109, 167 and 192 mS/mm respectively. Δ Vg is -1V/step in all cases.

4.3 DC Output Characteristics.

4.3.1 Material

Most of the GaAs MESFETs were fabricated on material grown by vapour phase epitaxy (VPE) at Plessey (Caswell). The material consisted of 85 nm of n^+ GaAs (1.5×10^{18}) grown on a nominally undoped buffer layer on a semi-insulating substrate. However, transistors were fabricated on various other substrates. These are summarised in the table below.

Table 4.1

	T	n	Buffer	Growth	Origin
1	85nm	$1.5.10^{18}$	1 um undoped	VPE	Plessey
2	100nm	10^{18}	1 um undoped	VPE	Plessey
3	100nm	unknown	300 nm undoped AlGaAs	MOCVD	Plessey
4	50nm	3.10^{18}	50nm undoped	MBE	Glasgow

T - active layer thicknes. n - active layer doping /cm^3.

The transitor dc characteristics were measured using an HP 4145A Semiconductor Parameter Analyser and an Omni-probe probing system. All the transistor characteristics were recorded with the prober microscope illumination turned off. If the illumination was turned on, there was an increase in the drain current of the devices due to the production of optically induced carriers in the active layer. This increase was particularly significant (approximately 10%) in the devices fabricated on the MOCVD and MBE grown layers. Owing to the relatively small amount of storage space on the HP operating discs, many of the transistor characteristics were not saved on disc. Therefore, the results presented here are a combination of the original HP plots (stored files), and reproduced curves from the original plots (unstored files).

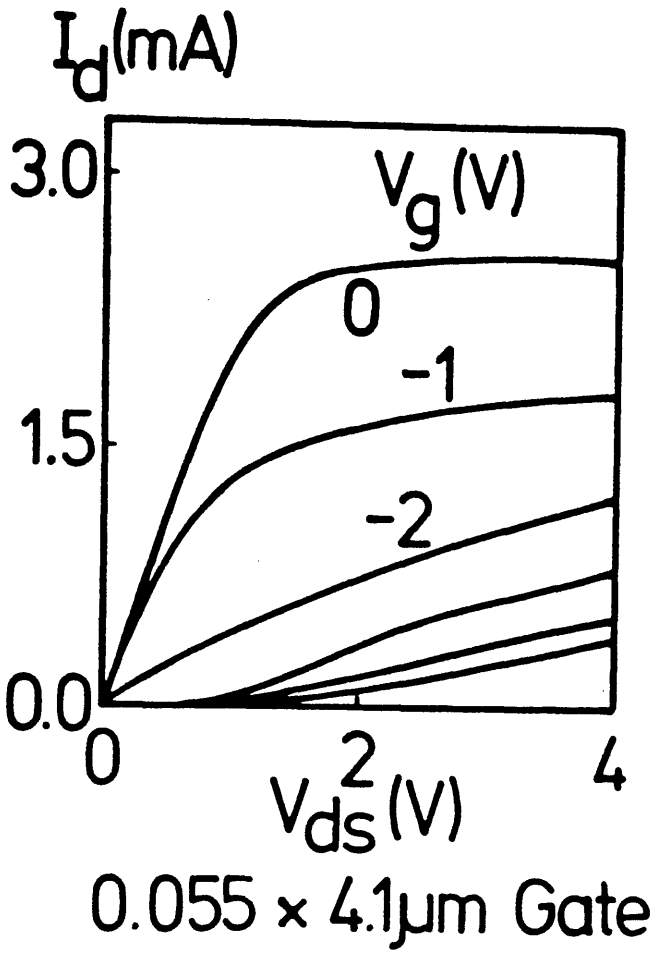
4.3.2 Devices on 85 nm VPE Layers.

GaAs MESFETs were fabricated using the methods described in the previous sections on the 85 nm VPE grown layers. The optimum

recess depth was determined experimentally using the method described in Sect. 4.2.8. In this case maximum g_m was achieved by recessing the gate until the drain current was reduced to 75 % of the drain current of the unrecessed device. No attempts were made to measure the recess depth by say, cleaving a sample and observing the recess profile in an SEM, as this would have been difficult due to the smallness of the samples. However, it was possible to calculate that the channel thickness under the gate was approximately 60 nm, from the pinch-off voltage of the devices [4.28]. Devices with gate lengths from 0.5 μm down to 0.055 μm were fabricated. The 0.055 μm devices are the shortest gate length devices reported anywhere, at this time [4.29].

From the dc characteristics of these devices it was found that there was no dramatic deterioration of the performance of the transistors. Even at the shortest gate lengths, the devices still showed good drain current saturation above 1.5 volts (V_{ds}). However, in the very short gate-length devices, the channel could only be pinched-off (at a given gate bias) for drain-source voltages less than a specific value which was defined as V_{ds} max. V_{ds} max was found to decrease with decreasing gate length. Fig 4.17 contains the output characteristics from a 0.055 μm device (4.1 μm width) and a 0.21 μm device (9.4 μm width). It can be seen that the short gate device only remains pinched-off (with a gate voltage of -4V) for drain-source voltages below 1.2V (V_{ds} max). However, the long gate device remains pinched-off until V_{ds} exceeds 2.4 volts. V_{ds} max was found to vary with the gate length of the transistors but was completely independent of the total gate width of the devices.

A set of devices with gate lengths ranging from 0.055 μm to 0.5 μm was fabricated on the 85 nm VPE wafer. Because, the etch rate of the recessing etch varies with the width of the opening in the resist, only devices with the same gate length were fabricated on individual chips. This meant that the recess depth could be kept reasonably constant for each particular gate length. V_{ds} max was measured on all of the devices. Fig 4.18 shows a graph of V_{ds} max versus gate length for devices which had been recessed by similar amounts (-4 volts applied to the gate). It can be seen that V_{ds} max varies exponentially from



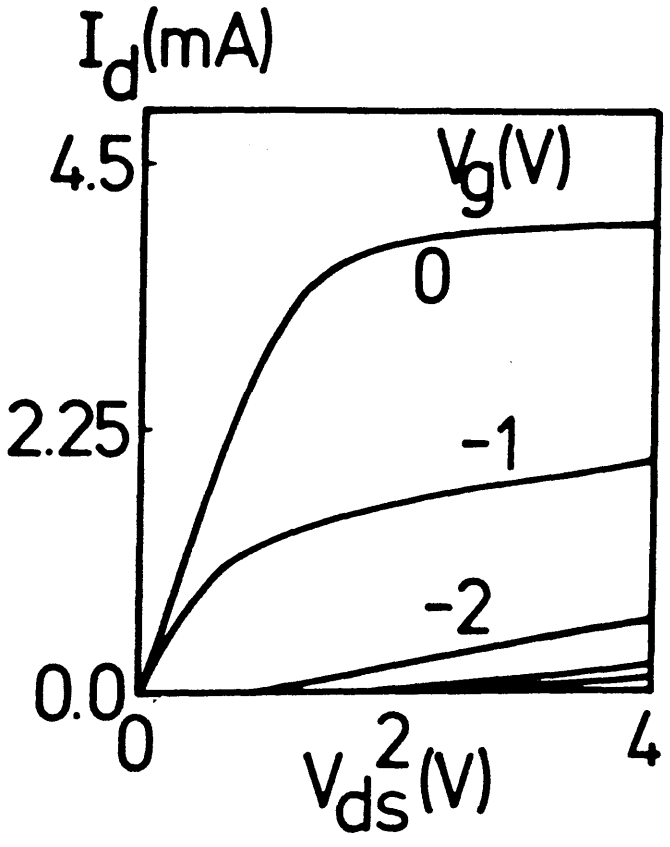


Fig. 4.17 DC output characteristics of a 55 nm gate-length and a 210 nm gate-length GaAs MESFET showing the poorer pinch-off of the short gate device.

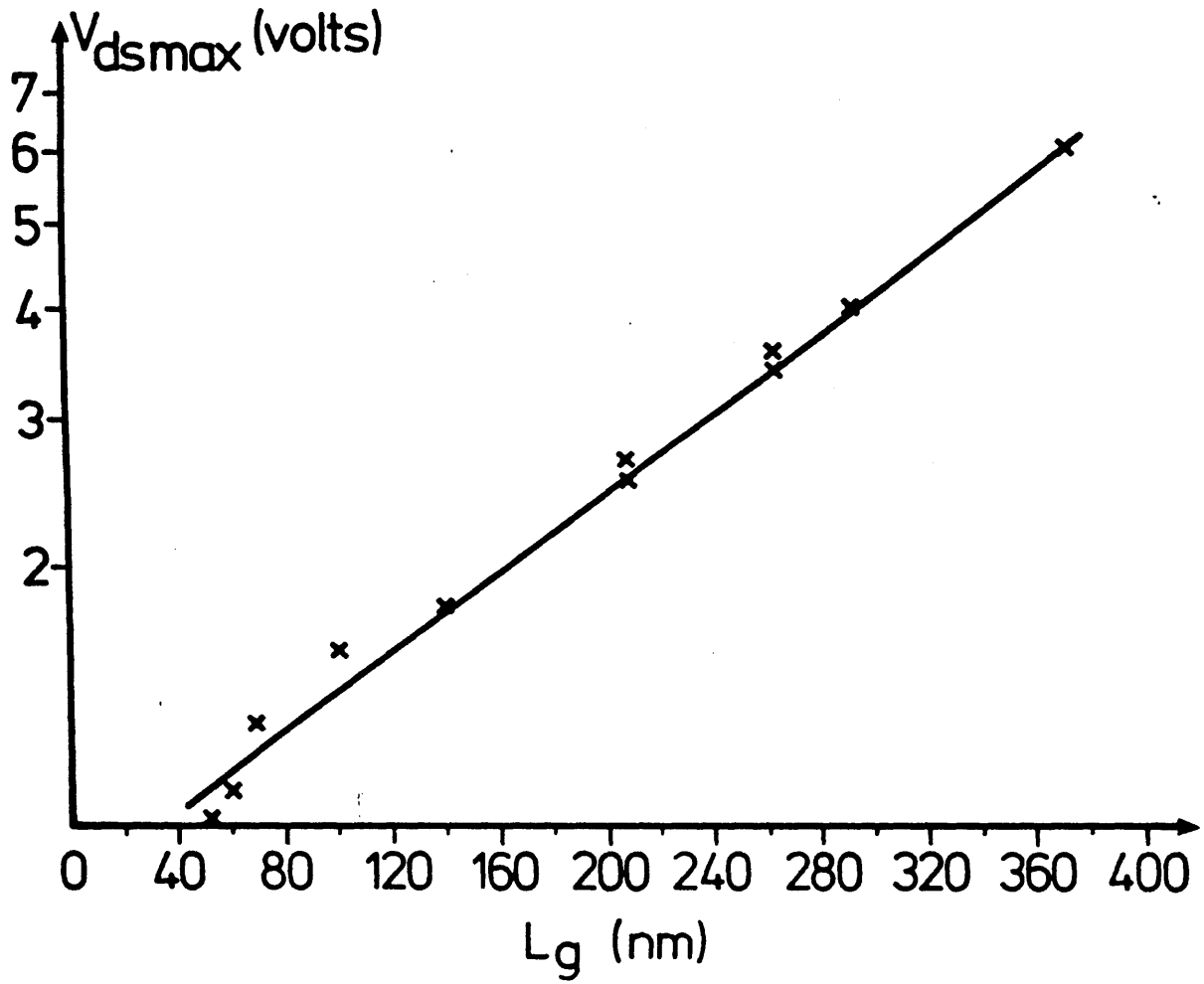


Fig. 4.18 Graph of the maximum drain-source voltage which can be pinched-off in a device (-4 V gate bias) versus the gate length of the device.

approximately 1 V with L_g = 55 nm up to 6 V when L_g = 360 nm.

In practice, V_{ds} max could be increased by recessing the gate further. However, this resulted in a reduction in the drain current caused by an increase in the parasitic resistance of the channel. Over-recessing the gate led to an unacceptably low transconductance.

It was speculated in ref. 4.29 that the failure of pinch-off in these short gate transistors was due to the poor interface between the n^+ epi-layer and the undoped buffer layer of the VPE grown material. Fig. 4.19 shows the doping concentration (N_d) versus depth profile for this material. It can be seen that N_d drops from $10^{18}/cm^3$ to $10^{16}/cm^3$ over a distance of approximately 150 nm. With such a graded interface, it seemed reasonable to assume that current injection into the interface region was likely cause of poor pinch-off at higher drain source voltages.

4.3.2.1 Monte-Carlo Simulation

Since the publication of these results the devices have been analysed using a Monte-Carlo simulation program [4.30]. The modelling was carried out for devices fabricated on material with the doping profile of fig. 4.19 and also for devices on material with an abrupt interface between the doped active layer and the undoped buffer.

First of all, the carrier concentration beneath the gate was evaluated. For this simulation the gate was assumed to be recessed until the channel thickness below the gate was 50 nm. The carrier concentration versus depth profiles for devices fabricated on material with both graded and abrupt active/buffer layer interfaces is shown in fig 4.20. It is evident that a higher percentage of carriers is present in the interface region of the graded material than in the abruptly doped material. This supports the speculation that current injection into the buffer layer may cause problems with extremely short gate devices.

Fig. 4.21 shows graphs of I_d versus gate bias for both sets of devices (gate length =0.055μm). It is clearly shown that,

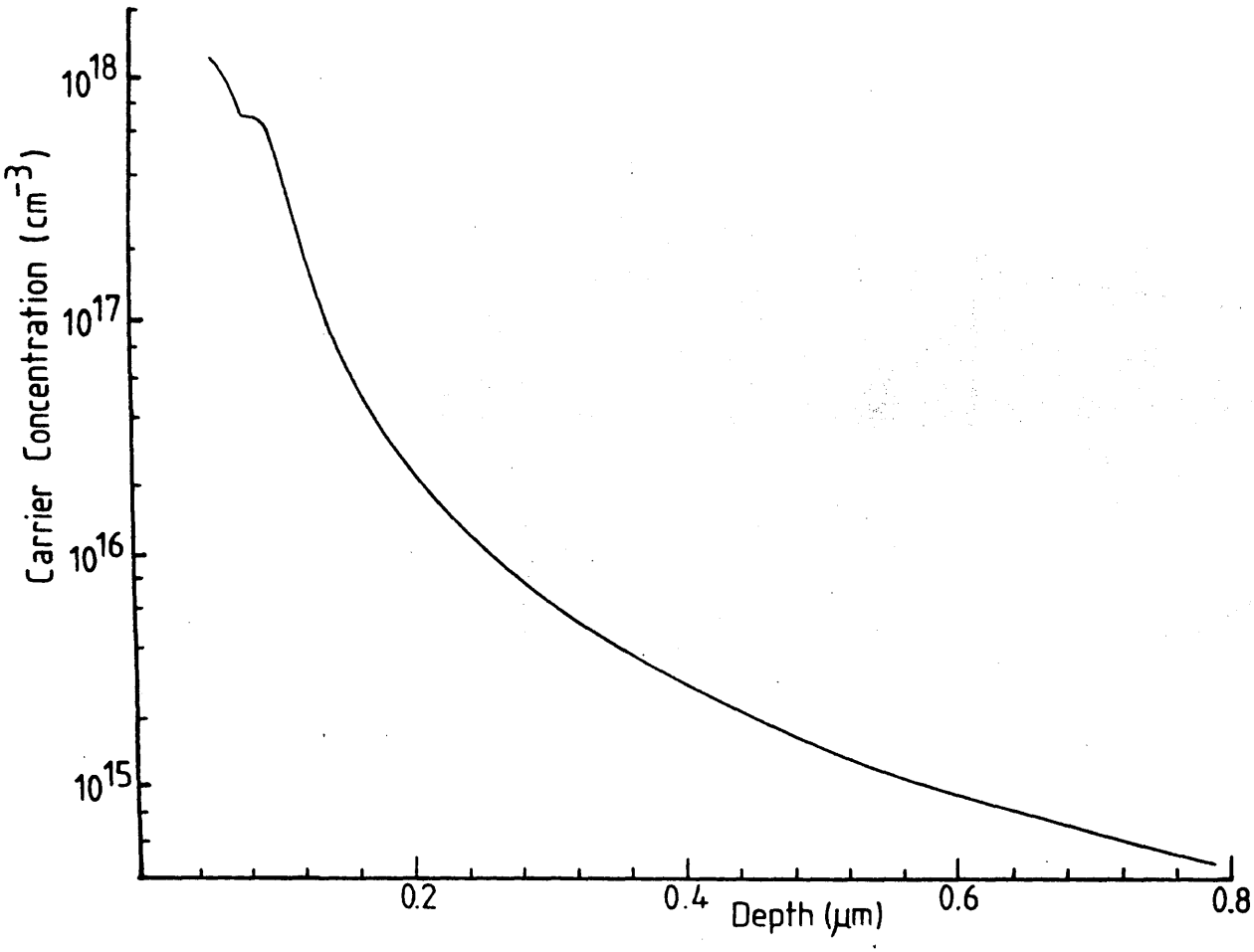
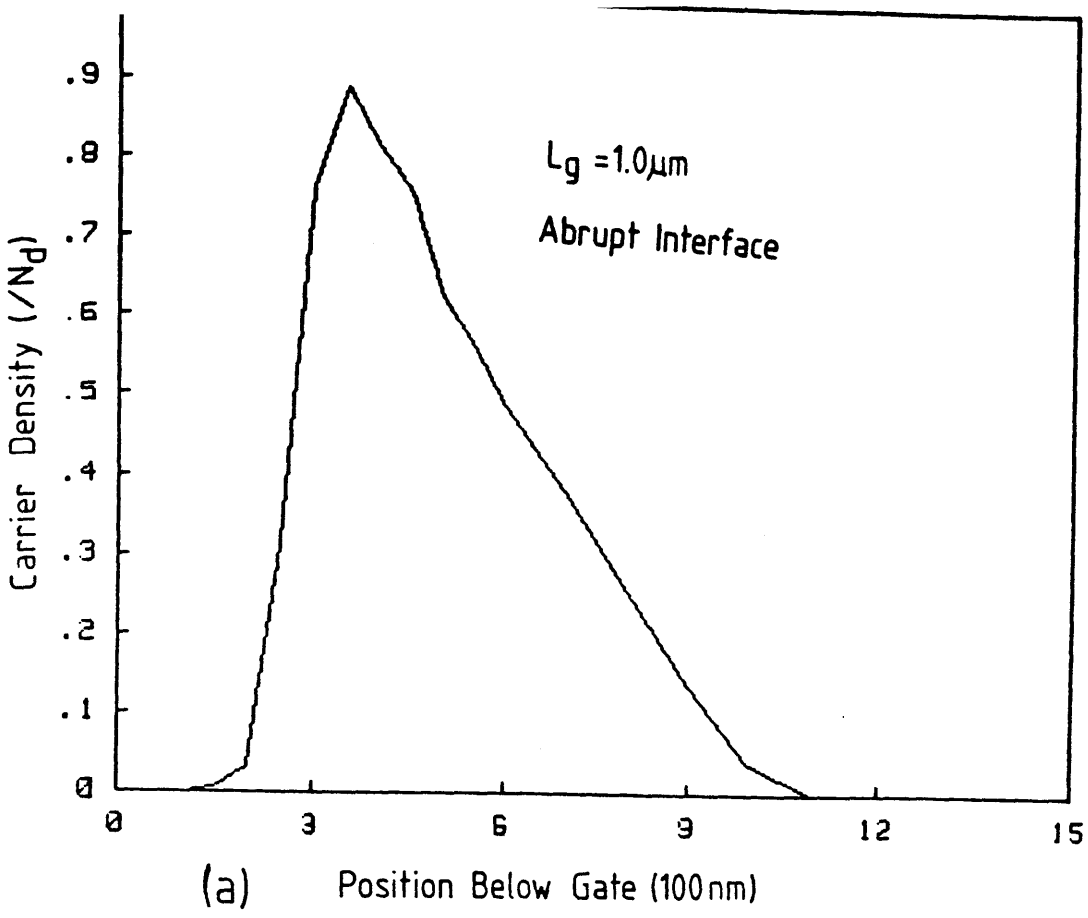


Fig. 4.19 Doping profile of the 85 nm VPE grown wafer used for MESFET fabrication.



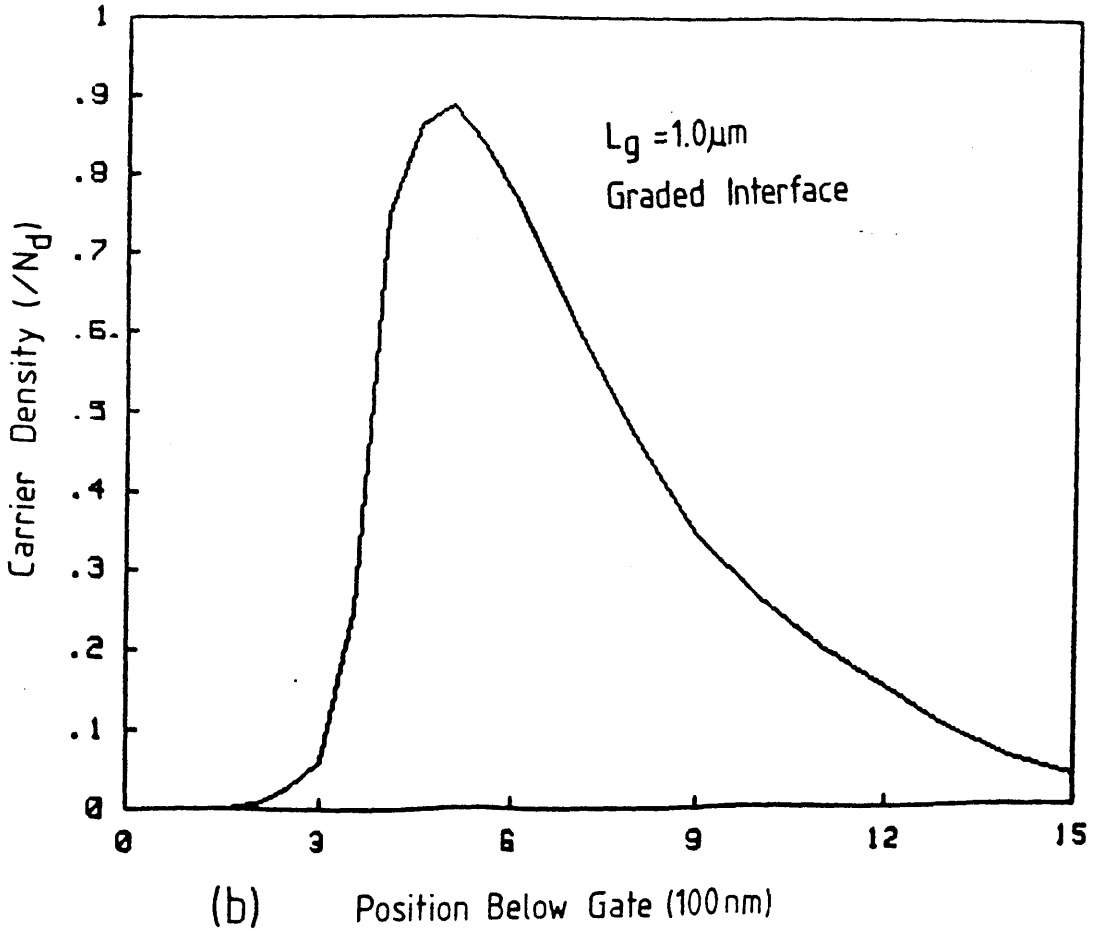
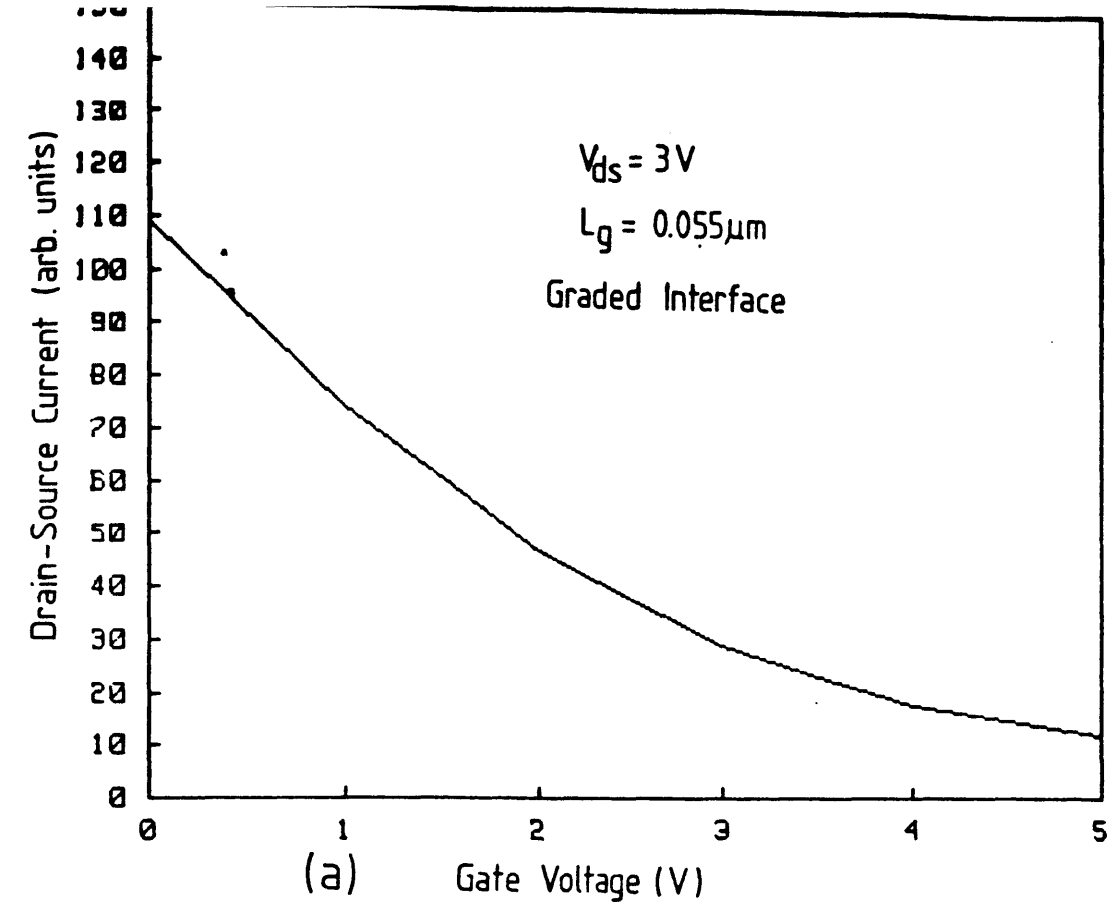


Fig. 4.2C Monte Carlo simulation of carrier density v depth below the gate for a 1 μm gate device on material with a) a graded interface and b) an abrupt interface.



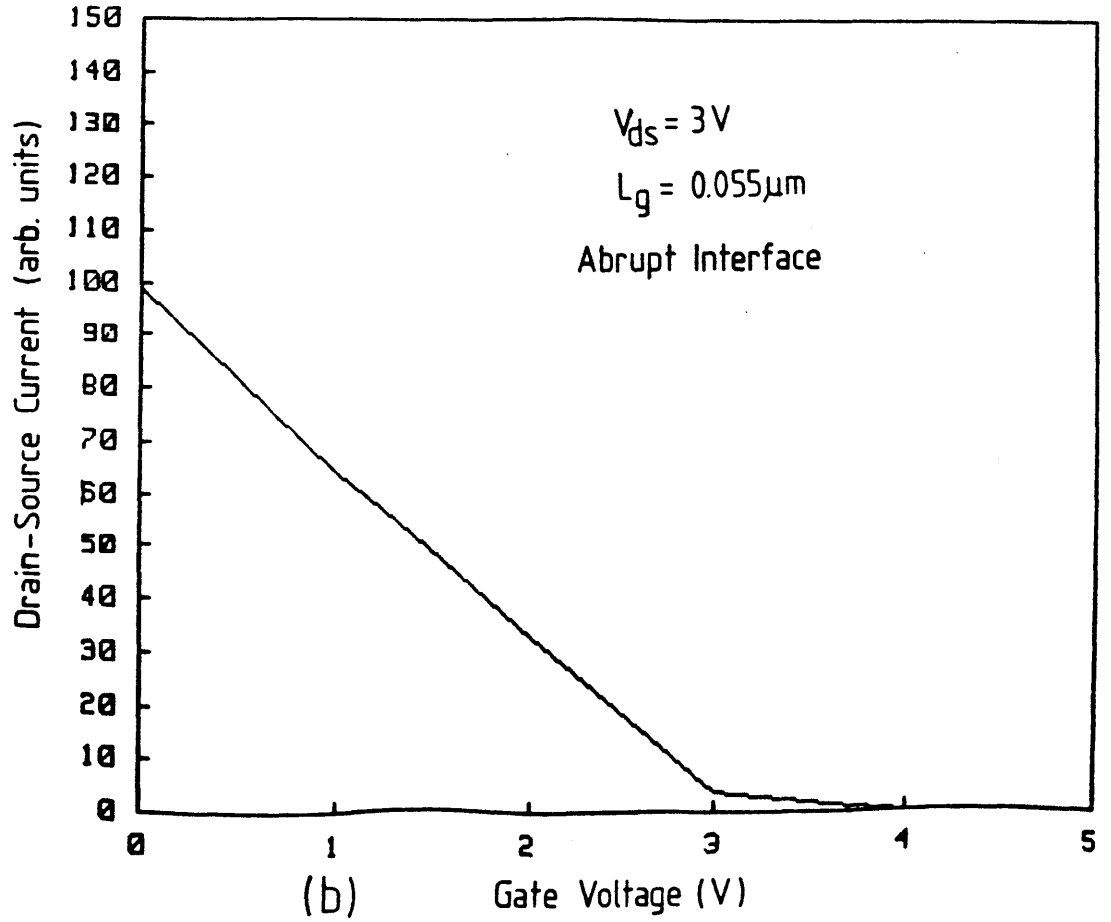
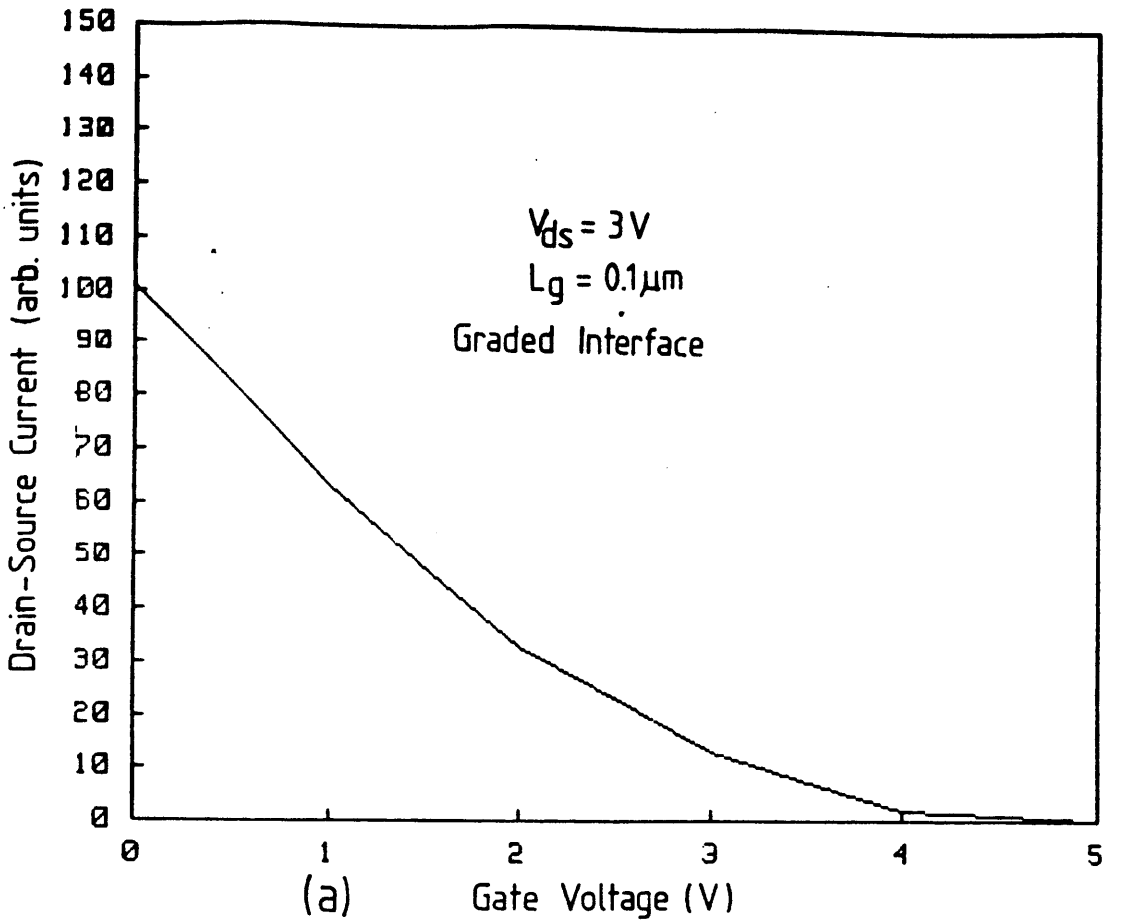


Fig. 4.21 Monte-Carlo simulation of the drain current versus gate voltage for 0.055 μm gate length devices fabricated on material with a) a graded interface and b) an abrupt interface.



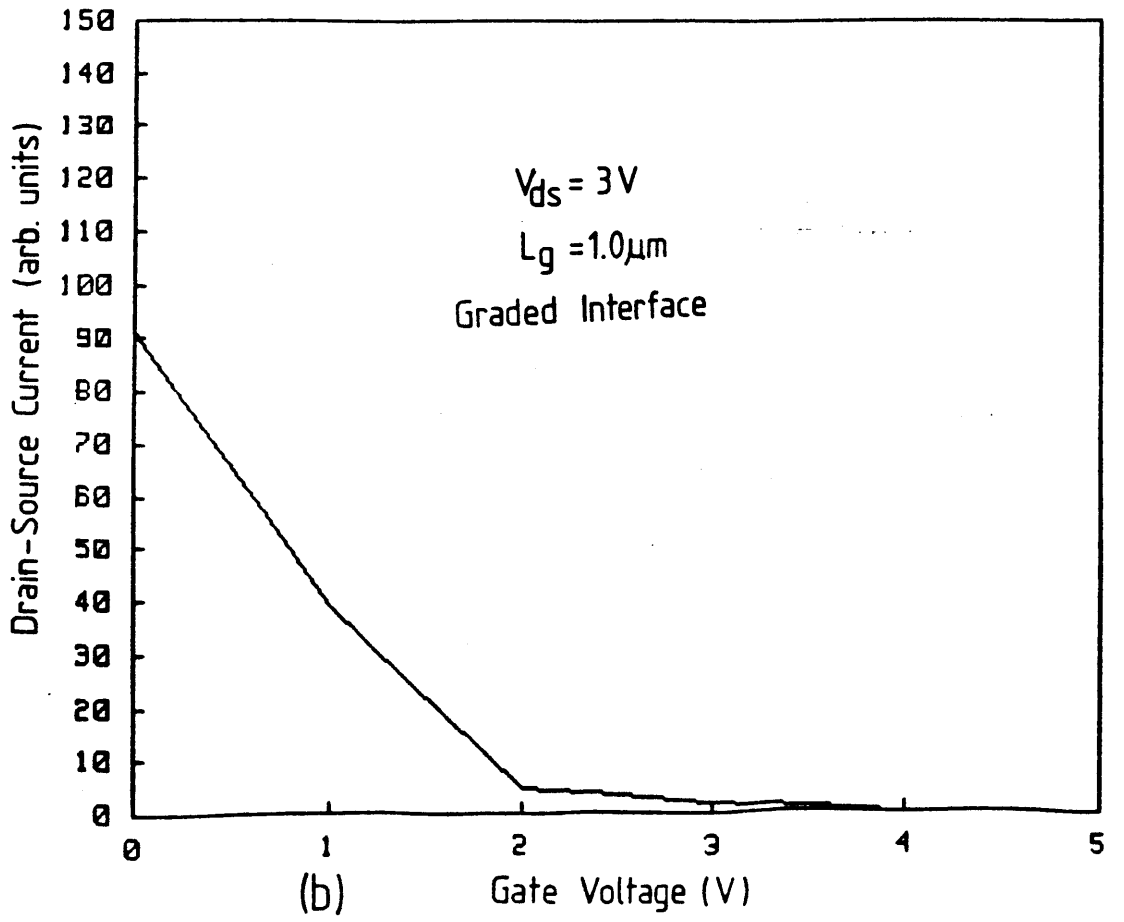


Fig. 4.22 Monte-Carlo simulation drain current versus gate voltage for devices fabricated on material with a graded interface for gate lengths of a) 0.1 μm and b) 1.0 μm.

with an abrupt interface, the transistor is almost pinched-off with an applied gate voltage of -3 V, whereas, with the graded interface there is still a significant current flow even with a gate bias of -5 V. The program was rerun for longer devices (0.1 and 1 μm) fabricated on the graded material. The drain current versus gate bias graphs for these devices are shown in fig. 4.22. These curves clearly show that as the gate length is increased, the current flowing in the interface region is reduced, which means that better pinch-off characteristics are obtained.

These simulated results agree well with the experimental observations made with short devices on the 85 nm VPE grown epi-layer. That is, the current injection into the buffer layer is confirmed to be the cause of the poor pinch-off characteristics of the short gate devices. They also show that the effect is significantly reduced when material with an abrupt interface is used for device fabrication. This result was confirmed when devices were fabricated on the MOCVD and MBE grown layers, the results of which are presented in sections 4.3.3 and 4.3.4.

4.3.2.2 Variation of transconductance with gate length.

The transconductance (g_m) of a MESFET is predicted to be proportional to $1/L_g$ [4.6]. Therefore extremely high transconductances should have been expected from the very short gate length MESFETs. However, the maximum transconductance was found to occur in devices with gate lengths of 0.08 μm and not at the shortest gate lengths of 0.055 μm. Fig 4.23 shows the dc output characteristic of a 0.08 μm gate length MESFET, where the gate had been recessed to the optimum depth for this material. The transconductance of this device is 320 mS/mm which is amongst the highest reported transconductances for GaAs MESFET devices. [4.31,4.32]. On average, however, g_m values of around 200 to 250 mS/mm were obtained for the range of gate lengths produced. It was surprising to find that the highest g_m values came from devices with very short channel widths (<10 um) since g_m should be independent of the channel width. It was not understood why higher g_m values were obtained in the narrow channel devices.

The sensitivity of the transconductance of these devices to

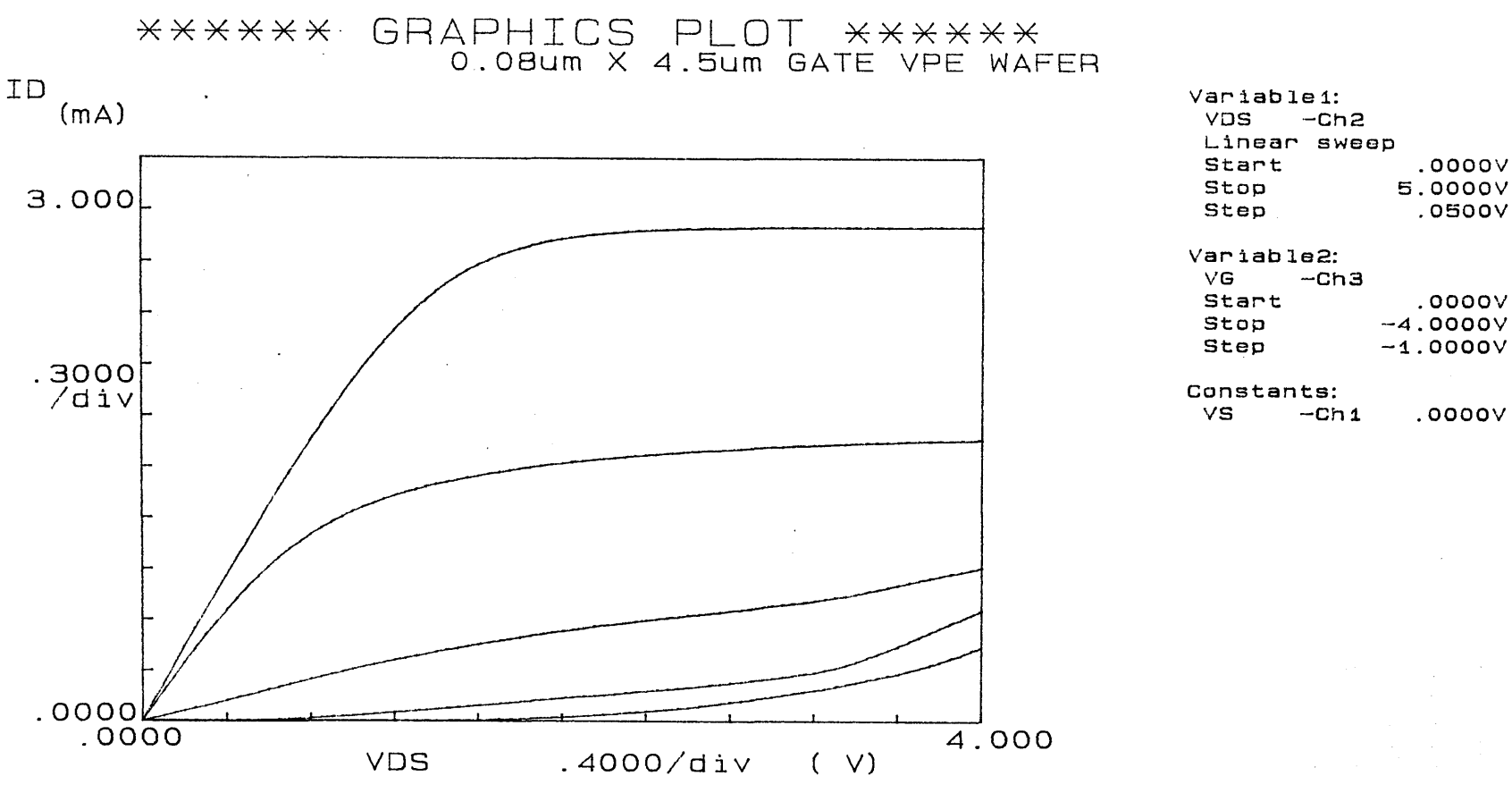


Fig. 4.23 DC Output characteristics of a 0.08 µm gate-length MESFET fabricated on the 85 nm VPE grown epi-layer. This device has a high transconductance of 320 mS/mm.

the recess depth of the gate meant that it was impossible to determine accurately how g_m varied with L_g. It was found by experiment that the transconductance was far more sensitive to small differences in the recess depth than to changes in the gate length. Therefore, any plots of g_m versus L_g would be meaningless. However, the maximum transconductances were almost invariably obtained from 0.08 - 0.12 μm gate length devices and never from the shortest gate length devices. This implies that the transconductance reaches a maximum value at a certain gate length and then decreases as the gate length is reduced. This effect could be due to the high series resitance of the recessed structure [4.28] and/or the transconductance compression due to free surface depletion [4.33]. In very short gate-length devices, the depletion width below the gate may be less than that under the free surface between the gate and drain. It is this free surface depletion which then limits the current in the channel.

4.3.3 Devices on 100 nm VPE grown layer

Transistors were fabricated on the VPE grown wafer with the 100 nm active layer. These devices were essentially fabricated for ac measurement because it was hoped that the thicker epi-layer would reduce the parasitic channel resistances of the devices. The optimum recess depth was determined to correspond to a saturated drain current reduction to 45 % of the unrecessed drain current (sect. 4.2.8). The channel thickness below the recessed gate was estimated [4.28] to be the same as for the devices on the 85 nm layer (60 nm), as expected. Because of the deeper recess required for these devices, they were more difficult to fabricate. However, the dc output characteristics obtained were slightly superior to those of the previous devices. The drain current saturation was improved and the saturation voltage was reduced, probably as a result of a reduction in the parasitic channel resistances. Fig 4.24 contains an example of the output characteristics of a device fabricated on this material. It can be seen that the drain current is much higher than on any of the previous devices due to the increased channel width (34 μm).

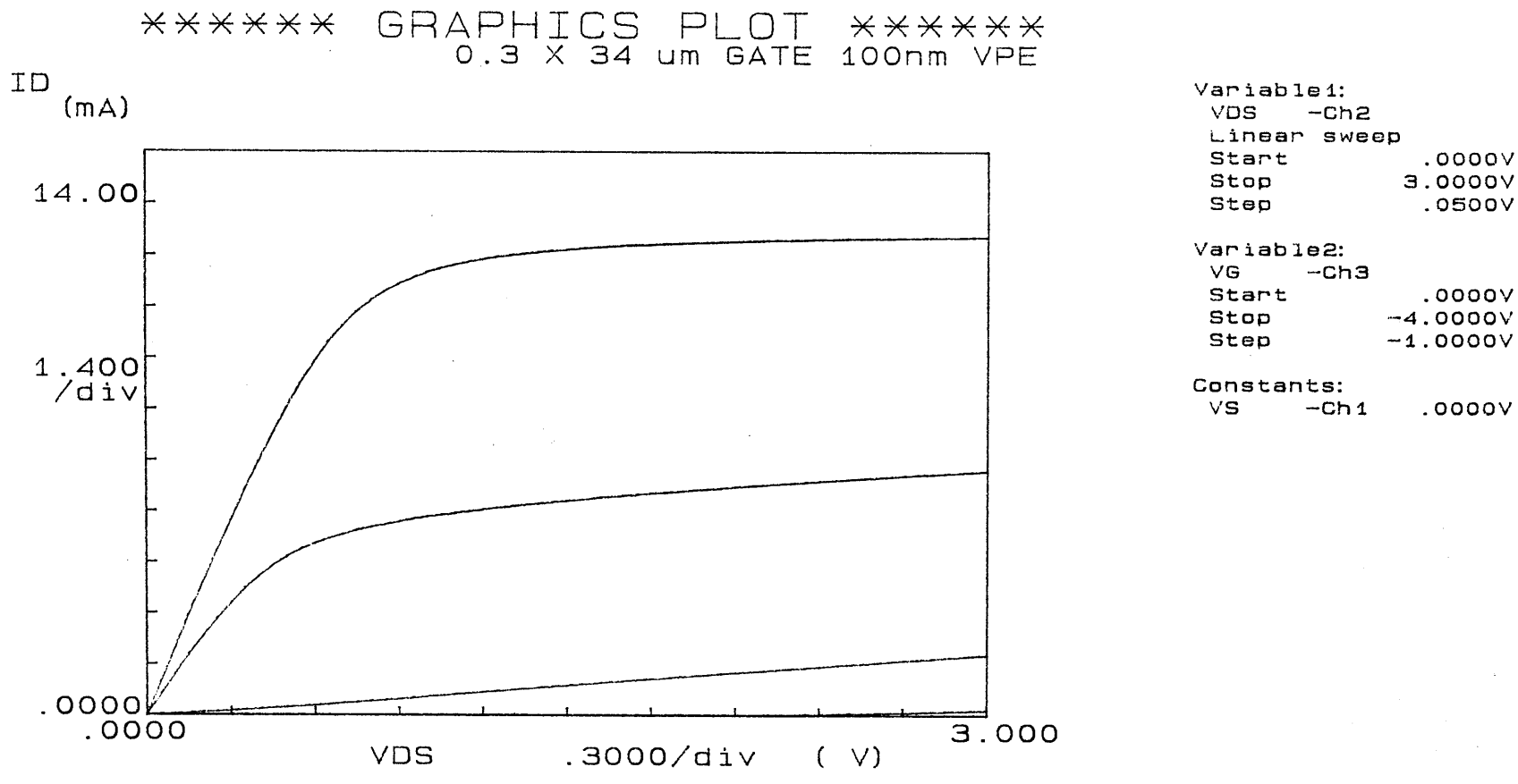


Fig. 4.24 DC Output characteristics of a 0.3 µm gate-length MESFET fabricated on the 100 nm VPE grown epi-layer. The channel width is 34 µm and the transconductance is 200 mS/mm

4.3.4 Devices on the 50 nm MBE Grown Wafer

GaAs MESFETs were fabricated on the wafer grown by MBE in this department (wafer 4 - table 1) [4.34], with a range of gate lengths down to 0.08 μm. The material was designed so that the channel below the gate of the devices could be pinched-off without the need for gate recessing. It was hoped that this would give a better indication of how the device performance varies with gate length. Unfortunately, it was discovered that the devices on this wafer were dominated by a backgating effect which meant that only a few MESFETs were fabricated.

4.3.4.1 Backgating

Backgating is an effect in which a change in the substrate bias results in a reduction in the drain current of the MESFET [4.35]. This is obviously a detremental effect in GaAs circuits, due to the interaction of closely spaced devices [4.36]. Backgating is normally associated with the accumulation of negative charge on deep traps at the interface between the active layer and substrate, resulting in the formation of a space charge region. The application of a bias to the substrate modulates the space charge region, which leads to a change in the active channel thickness and, therefore, a change in the drain current.

However, on the MBE wafer, the backgating was significantly worsened due to the fact that the undoped buffer layer of this material turned out to be lightly p-doped. This means that at interface between the active layer and the buffer layer, there is a p-n junction. Applying a negative voltage to the substrate, means that the depletion width of the junction increases and consequently the active channel layer is decreased.

4.3.4.2 "Gateless FET"

Fig. 4.25 contains the dc characteristics of a gateless FET, ie, a transistor was fabricated up to the point where it is ready for gate patterning, but was tested before depositing a gate. It can be seen that the device operates very much like a normal FET.

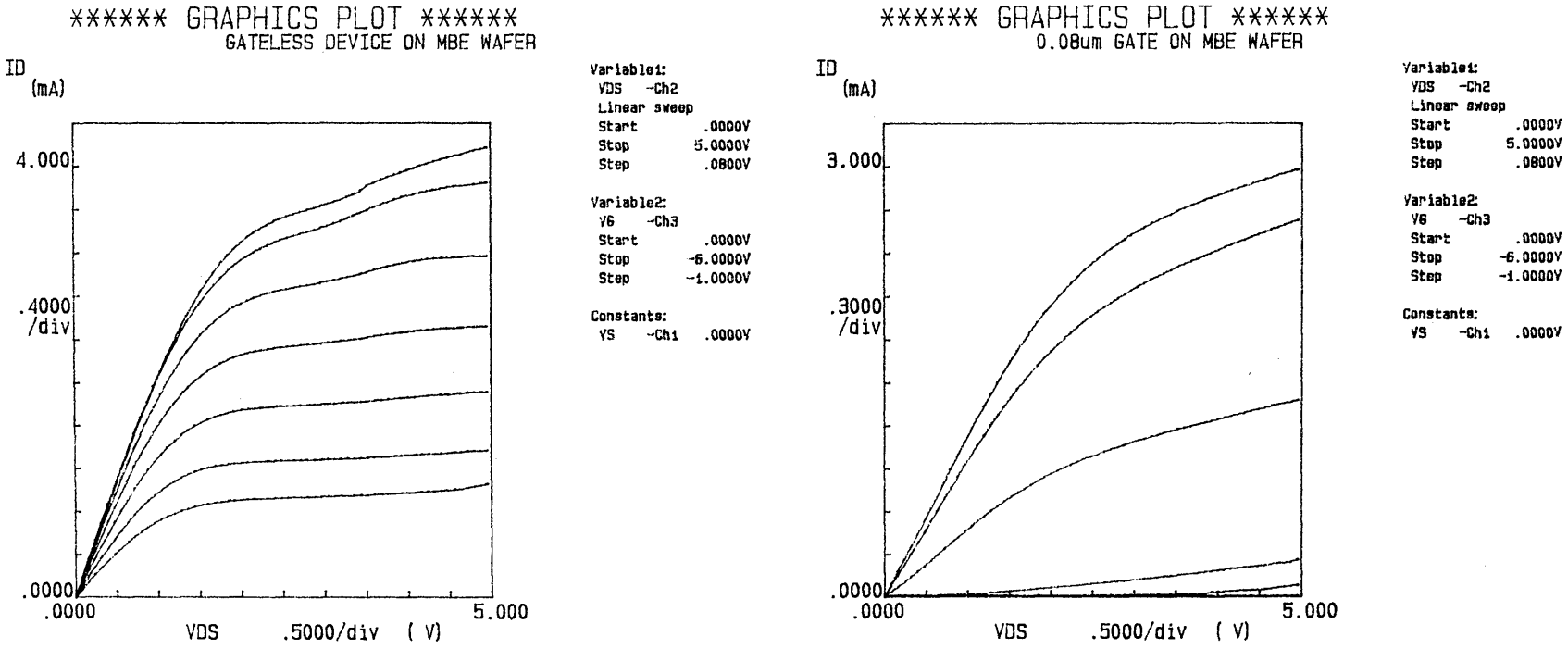


Fig 4.25. DC Output characteristics of a "gateless FET." The drain current of this device is modulated by the backgating effect.

Fig.4.26 DC Output characteristics of a 0.08 um gate-length MESFET fabricated on the MBE grown material.

With -7 V applied to the gate bonding pad, which was 5 μm from the source-drain channel, the device is almost pinched-off. This clearly illustrates the problems associated with backgating on this particular wafer.

Later MBE grown wafers with various buffer layer thicknesses showed that the backgating worsens with buffer layer thickness. This is probably a result of the mesa isolation processing. When the buffer layer is thin (50nm), it is likely that, under the gate pad, most of the buffer layer will have been removed, due to the faster etch rate of large areas compared with the isolation grooves (see fig 4.8). However, with the thicker layers (100 and 200nm), more of the buffer layer would be left under the gate pad, leading to a worsening of the backgating effect.

Serious backgating was only observed on the MBE wafer. On the other wafers the backgating transconductance was of the order of a few mS/mm which was negligible compared with the g_m of the actual devices (200-300 mS/mm). Backgating g_m is defined as the reduction in drain current, arising from the application of a potential to a contact remote from the drain-source channel, divided by that potential [4.37]. In these devices the potential was applied to the gate pad deposited on the buffer layer of the material.

Subsequently when MBE wafers have been requested, an n^- buffer layer has been specified. The reason for this is that the nominally undoped MBE layers are actually lightly p-doped. Therefore, to avoid backgating the buffer layer has to be deliberately grown with a lightly doped n-type buffer layer. However, no such wafers were received before the conclusion of this work so it still remains to be seen if improved device performance is achieved on MBE material.

4.3.4.3 MESFETs With Gates

Fig 4.26 shows the dc output characteristics of a 0.08 μm gate length MESFET fabricated on the MBE wafer. This device does not exhibit the poor pinch-off characteristics observed in the

devices on VPE grown material. It can be seen that with an applied voltage of -4 volts the channel is completely pinched-off for drain-source voltages up to 4 V (cf 1.2 V previously). The g_m of this device, is 192 mS/mm, half of which could probably be attributed to the backgating effect.

The improvement in the pinch-off properties of this device is probably due to the abrupt p-n junction at the active-layer /buffer-layer interface. The junction barrier will improve the carrier confinement to the active layer of the device. Therefore, at the pinch-off voltage, carrier injection into the buffer layer is less severe than on the VPE grown wafers with graded doping profiles at the interface. Unfortunately, the p^- buffer layer also leads to a very serious backgating problem so should not be used to improve the pinch-off of the devices.

4.3.5 Devices on the MOCVD Wafer (AlGaAs Buffer Layer)

It was reported by Ghosh and Layman [4.38] that device performance would improve if the undoped buffer layer is replaced by an AlGaAs buffer layer. The AlGaAs layer improves the carrier confinement to the active layer and, to a certain extent, prevents the injection of electrons into the buffer layer. It was determined in ref 4.38 that the Al concentration should be around 20 % for optimum device performance.

No material was available with this type of buffer layer. However, the material for fabricating GaAs membranes (MOCVD wafer) had an etch stop layer of $Al_{.6}Ga_{.4}As$ immediately below an n^+ GaAs layer (see sect 6.5). It was decided to fabricate devices on this material. Fig. 4.27 shows the dc output characteristics of a 0.1 gate length device fabricated on the MOCVD wafer. The difference obtained by measuring the output characteristics under illumination and in the dark are shown in this figure. Although this device is not pinched-off, the flatness of the I/V curve (dark) with a gate bias of -2.5 suggests that the pinch-off properties of this device would be superior to devices fabricated on the VPE grown wafers, given that the gate recessing was fully optimised. In the device of fig. 4.27 the gate was recessed etched until the drain current

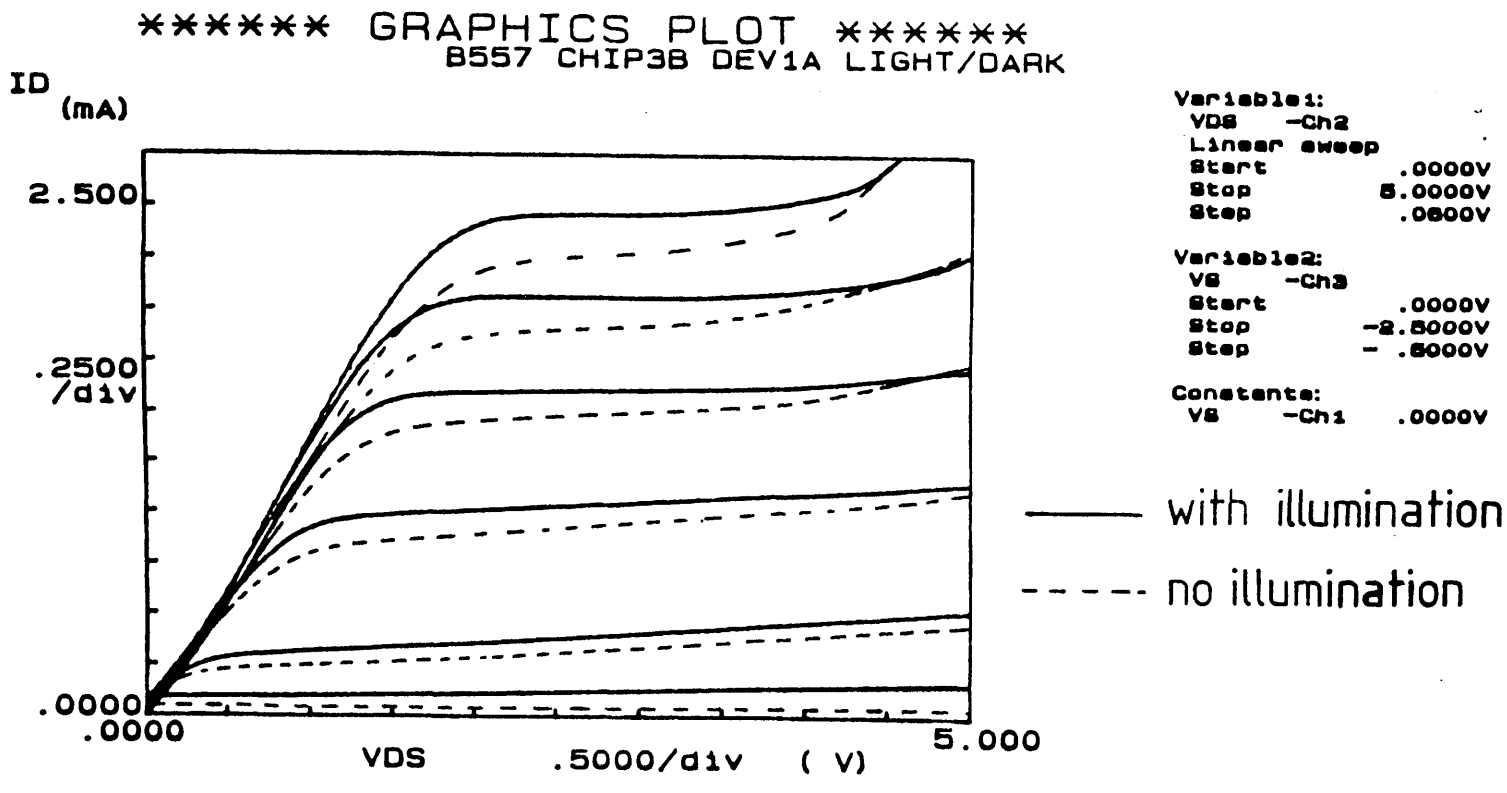


Fig. 4.27 DC Output characteristics of a 0.1 um gate-length MESFET fabricated on the MOCVD grown wafer (AlGaAs buffer). The two sets of curves show the difference obtained when the device was tested under microscope illumination and when it was tested in the dark.

was reduced to about 60 % of its unetched value. However, no experiments were done to find the optimum recess depth for this wafer. Of all the devices tested on this wafer, it was found that only about 10 % had reasonable characteristics. The poor quality of the GaAs layer grown on high aluminium concentration AlGaAs (due to large lattice mismatch) was the probable cause of the low number of working devices. The g_m of the device in fig 4.27 was calculated to be only 72 mS/mm (9.2 μm channel width). This is a lot lower than the values which were obtained on the VPE grown epi-layers. Again, the low transconductance was attributed to the fact that a high Al concentration was present in the buffer layer. This would cause a reduction in the mobility of the GaAs active layer and, as a result, a reduction in g_m.

4.3.6 Summary of dc Measurements

Very short gate length devices have been fabricated on several types of wafer. It was found that at very short gate lengths, current injection into the buffer layer results in poor pinch-off. The pinch-off of the devices was improved using MBE grown material and MOCVD material with an AlGaAs buffer layer. Unfortunately, severe backgating in the MBE wafer and the unsuitably high Al concentration of the buffer layer of the MOCVD wafer, means that more work has to be done to determine the most suitable type of material for extremely short gate length transistors.

4.4 AC Measurements (s-parameters)

Measurement of voltages and currents become increasingly difficult at very high frequencies, therefore, scattering or s-parameter measurements were used in the analysis of the MESFETs. [4.39]. S-parameters define the ratios of reflected and transmitted travelling waves at the ports of a two port network as shown schematically in fig 4.28a). When the two port network is a GaAs MESFET (fig 4.28b) it is possible to determine the lumped-element equivalent circuit for that device using the measured s-parameters. Fig. 4.29 shows the rf equivalent circuit of a GaAs MESFET and the location of the various elements in a

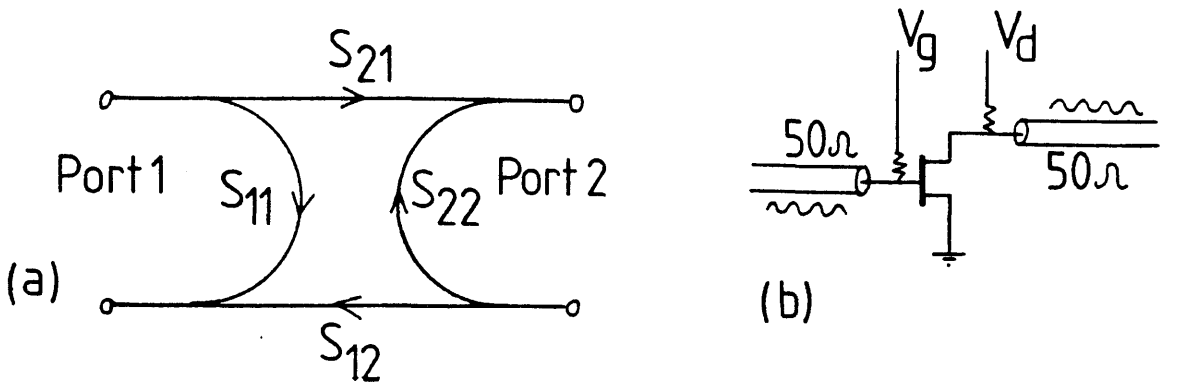


Fig. 4.28 a) s-parameter flow diagram. b) Conceptual representation of FET s-parameter measurements.

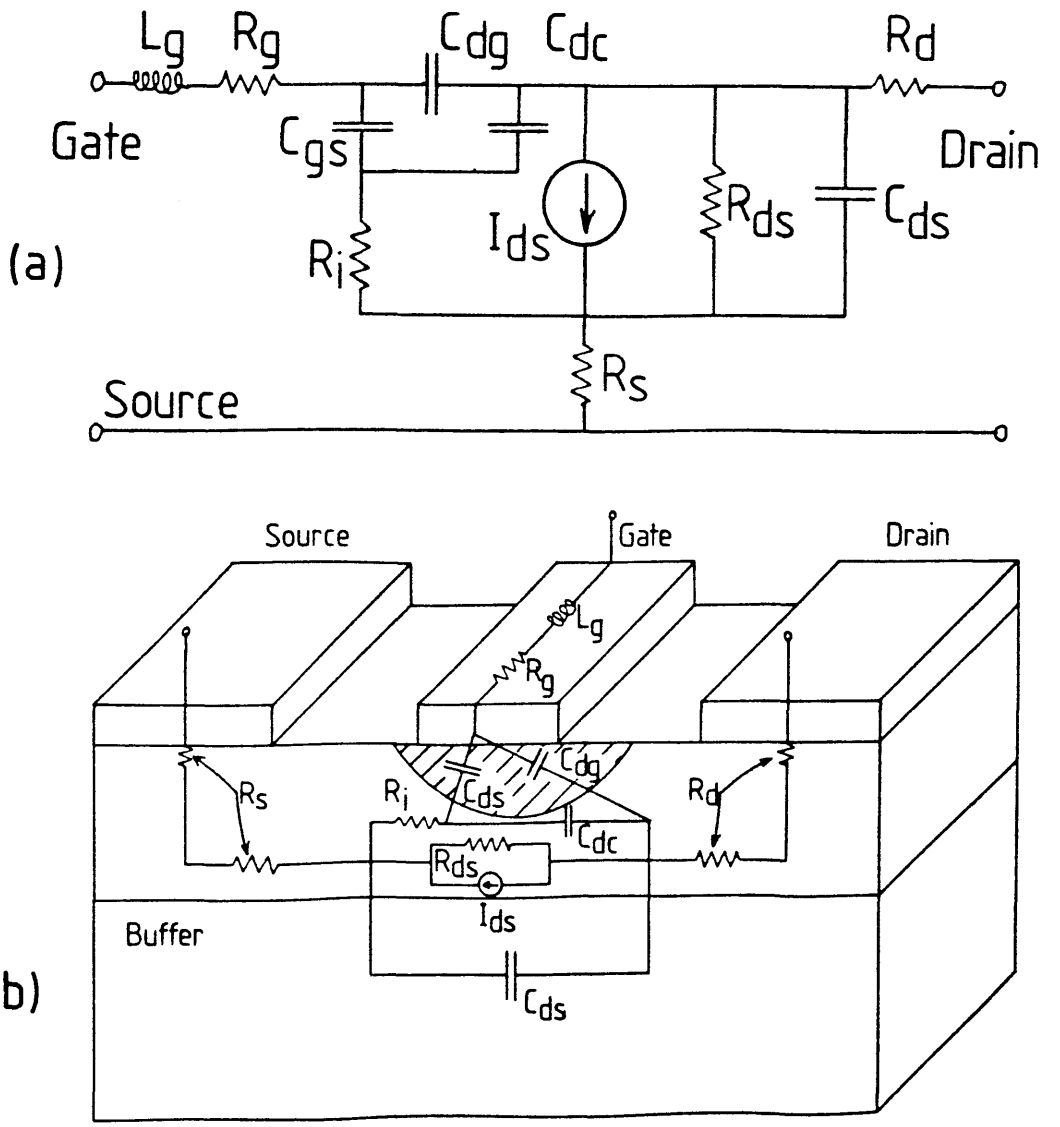


Fig. 4.29 a) Equivalent circuit diagram of a GaAs MESFET and b) the physical origins of the circuit parameters.

FET structure [4.8]. The input impedence of the circuit can be determined from the reflection parameter S_{11}. The real part of S_{11} is equal to the input resistance $R_g + R_s + R_i$ where R_g is the series gate resistance, R_s is the source resistance and R_i is an intrinsic resistance associated with the channel below the gate. The reactive part of S_{11} arises from C_{gs}, the gate-source capacitance, in series with L_g, the gate inductance. C_{gs} and L_g can be calculated from two simultaneous equations. Similarly S_{22} yields values for the output resistance, $R_s + R_d + R_{sd}$ where R_d is the drain resitance and R_{sd} is the source-drain channel resistance. Normally $R_{sd} >> R_s$ or R_d. The output capacitance, $C_{dc} + C_{ds}$ where C_{dc} is the capacitance associated with the dipole layer formation and C_{ds} is the substrate capacitance, can also be determined from S_{22}.

The first devices to be tested were narrow channel (6.8 μm) devices fabricated on the 85 nm VPE grown wafer. However, it was thought that the parasitic parameters (R_s, R_d, R_g and C_{ds}) were dominating these devices. Subsequently only devices fabricated on the 100 nm wafer (channel width 25 or 34 μm) were considered for ac testing. When taking dc measurements it was possible to test every device on a chip. However, for s-paramterer measurements only the best of the devices were selected for testing. Once selected (according to their dc performance), the chip was scribed and divided into individual devices for mounting into the ac test jigs. These test jigs consisted of a 1.5 x 0.5 inch ceramic holder with 50 ohm microstrip lines extending from either end of the holder to a 1 mm hole in the centre. The ceramic holders were mounted in a special test fixture for connection to the network analyser via coaxial cable. Fig 4.30 shows an idividual device bonded into a ceramic holder. The gate and drain of the device are connected to the microstrip by single 25 μm gold wire bonds, whereas, the source is double bonded to the base of the sample holder (ground). This was to reduce the inductance of the source bonds.

All the ac measurements were carried out at Plessey (Caswell). An HP8410 network analyser was used for measuring the s-parameters. Before proceeding with the measurements, the system was calibrated using a variety of sliding loads and open

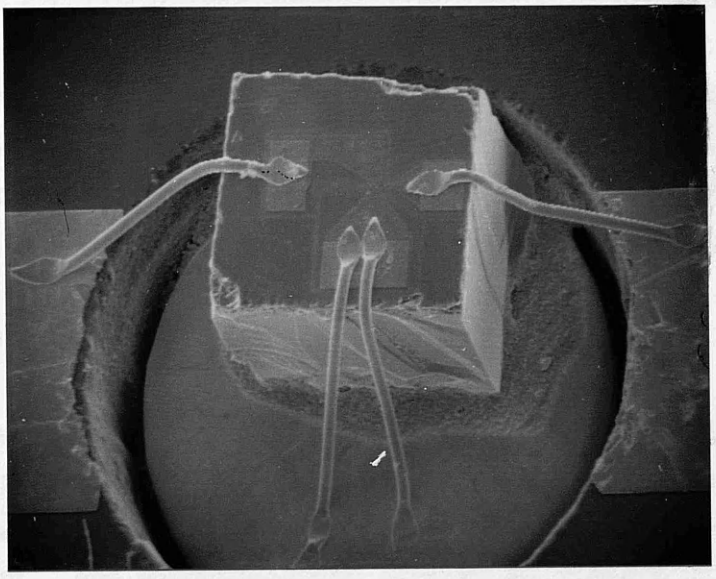


Fig. 4.30 SEM micrograph of an individual MESFET mounted and bonded into an ac test holder. The diameter of the hole is 1mm.

and short circuits according to the software instructions from the system. However, the calibration was only made up to the plane at the end of the coaxial cable. This meant that the measured s-parameters were a combination of the actual device parameters and the holder parameters (ie the connector, 50 ohm line, and bond wires). The parameters of the connector were known and the parameters of the 50 ohm line and bond wires could be calculated from their physical lengths allowing their contribution to the s-parameter measurements to be removed. This process is known as "stripping."

4.4.1 Results

The s-parameters of five wide channel (25 and 34 μm) MESFETs, fabricated on the 100 nm VPE grown epi-layer, were measured at Plessey. Unfortunately, the results obtained were inconsistent. For example, there was no correlation between the gate-source capacitance of the devices, determined from the s-parameters, and the physical dimensions of the gate. To illustrate this point, it was found that C_{gs} of narrow (0.1 μm) gates on 25 μm wide devices was determined to be more or less the same as a 0.3 μm gate on a 34 μm wide device. Furthermore, the C_{gs} obtained from the s-parameter measurements were always about a factor of 3 - 5 greater than the calculated capacitance values from the gate dimensions and material parameters [4.30]. This suggests either one of two things; 1) the fringing capacitance of the gates becomes important at very short gate lengths or 2) the measurement technique, as it stands, is not suitable for extracting the very small parameters expected from these devices. Although a combination of both the above effects may lead to the inconsistent results, it is likely that the latter effect is more dominant. The reason for this goes back to the stripping paramaters used to extract the device information from the measured reflection and transmission coefficients. One of the parameters, namely the capacitance of the 50 ohm microstrip line (0.03 pF) was greater than the calculated depletion capacitance (of the order of 0.01-0.02 pF) of most of the devices which were measured. It seems unlikely that the resolution of the measurement technique could be better than the value of the stipping paramters. The fact that the measured C_{gs} did not vary

with the gate dimensions further supports this statement.

Further inexplicable observations were made from the reflection coefficients of the output circuit. It was found that when the gate bias was 0 V the output resistance and capacitance of the devices were typically 100 ohms and 0.02 pF respectively. When the gate bias was increased to -1 V, however, these parameters became 700 ohms and 0.07 pF respectively. The increase in the output resistance is due to the narrowing of the conducting channel below the gate which would result in a higher R_{ds} value. However, it was not understood why the output capacitance value ($C_{dc} + C_{ds}$) should increase so dramatically, although the effect could be due to the poor interface of the doped/undoped material of these devices.

The final observation to be made from the s-parameters of the tested devices was that the maximum available gain of the devices was determined to be very low and the cut-off frequency was about 7 GHz at best. In addition, the best gain values were obtained when the devices were biased with approximately -1 V on the gate. This effect could be as a result of the relatively low output resistance obtained from these devices. Once again however, the observations were not understood.

4.4.2 Summary of ac results

It was difficult to obtain any useful information from the ac measurements carried out due to the inconsistancy of the results. Because of these inconsistencies, it was decided not to proceed with high frequency noise measurements on this particular set of devices. Therefore, there is no indication yet of how these devices will perform at very high speeds. Clearly more work needs to be done in the field of ac testing. First of all it has to be established what methods should be used to determine the device parameters. Measurement of s-parameters, where the network analyser is only calibrated to the plane of the sample holder, may not be adequate for ultra-small MESFETs since the parameters of the holder and connector themselves may be greater than the paramters to be measured. This problem may be solved by using a system with rf probes in which the calibration can be

made right to the tips of the probes. Therefore, only the actual device parameters are measured.

Secondly, the design of short gate-length MESFETs has to be completely reconsidered. For this work the strategy was to make a device and test its performance. From the few ac measurements that were made on some of these devices it is evident that more thought will have to go into the MESFET design in order to obtain the best performance which could possibly be obtained by reducing the device dimensions.

Chapter 4 References

[4.1] SI Long, BM Welch, R Zucca, PM Asbeck, CP Lee, CG Kirkpatrick, FS Lee, GR Kaelin, RC Eden, "High Speed GaAs Integrated Circuits," Proc. IEEE **70**, p35-45 (1982).

[4.2] N Kato, K Yamasaki, K Asai, K Ohwada, "Electron-beam Lithography in N^+ Self Aligned GaAs MESFET Fabrication," IEEE Trans. Elect. Dev. **ED-30**, p663-668 (1983).

[4.3] K Yamasaki, N Kato, M Hirayama, "Below 10ps/gate Operation With Buried Layer SAINT FETs," El. Lett. **20** p1029-1031 (1984).

[4.4] WS Mackie. PdD Thesis, Glasgow University, 1984.

[4.5] I would like to acknowledge CH Oxley (Plessey) for his assistance in the MESFET design of devices for ac testing.

[4.6] SM Sze, "Physics of Semiconductor Devices," 2nd Ed. Chapter 6, Wiley, New York, (1981).

[4.7] ref [4.6] p325.

[4.8] CA Liechti, "Microwave Field Effect Transistors-1976," IEEE Trans. Microwave Theory Tech. **MTT-24**, p279-300 (1976).

[4.9] A Yoshii, M Tomizawa, K Kakoyama, "Accurate Modelling for Submicron-Gate Si and GaAs MESFETs using 2-Dimensional Particle Simulation," IEEE Trans. Elect. Dev, **ED-30**, p1376-1380 (1983).

[4.10] K Hess, "Ballistic Electron Transport in Semiconductors," IEEE Trans. Elect. Dev, **ED-28**, p937-940 (1981).

[4.11] MS Shur, LF Eastman, "Ballistic Transport in Semiconductors at Low Temperatures for High-Speed Logic," IEEE Trans. Elect. Dev. **ED-26**, p1677-1683 (1979).

[4.12] LF Eastman, R Stall, D Woodward, N Dandekar, CEC Wood, M Shur, K Board, "Ballistic Motion in GaAs at Room Temperature," El. Lett. **16**, p524-525, (1980).

[4.13] K Tomizawa, Y Awano, N Hashizuma, "Simulation of Near Ballistic Electron Transport in a Submicron GaAs Diode with AlGaAs/GaAs Heterojunction Cathode," IEEE Proc.**132**, p37-41 (1985)

[4.14] P Alto, "Ballistic Transistors Fastest Yet," Electr. Week, Apr 1985 p22-23.

[4.15] K Ohata, H Hoh, F Hasegawa, "Super Low-Noise GaAs MESFETs with a Deep Recessed Structure," IEEE Trans. Elect. Dev. **ED-27** p1029-1034 (1980).

[4.16] H Fukui, JV Dilorenzo, BS Hewitt, JR Velebir, JR Herbert, HM Cox, LC Luther, JA Seman, "Optimisation of Low-Noise GaAs MESFETs," IEEE Trans. Elect. Dev, **ED-27**, p1034-1037, (1980).

[4.17] H Higashisaka, T Mizata, "20 GHz Monolithic GaAs FET Low Noise Amplifier," IEEE Trans. Microwave Theory Tech. **MTT-29** p1-6 (1981).

[4.18] R Dingle, "New High Speed III/V Devices for Integrated Circuits," IEEE Trans. Elect. Dev. **ED-31**, p1662-1667 (1984).

[4.19] H Fukui, "Optimal Noise Figure of Microwave GaAs MESFETs," IEEE Trans. Elect. Dev. **ED-26**, p1032-1037 (1979).

[4.20] DM Tennant, "Metal on Polymer Ion Implantation Mask," J. Vac Sci Tech. **B1** p494-496, (1983).

[4.21] W Patrick, WS Mackie, SP Beaumont, CDW Wilkinson,

"Polyimide as a Negative Electron Resist and its Application in Crossovers and Metal on Polymer Mask Fabrication," Proc. 29th International Symposium on Electron, Ion and Photon Beams, Portland, Oregon (May 1985). Proceedings to be published in J. Vac. Sci. Tech. B. (Jan-Feb 1986).

[4.22] RL Van Tuyl, V Kumar, DC D'Avanzo, TW Talor, VE Paterson, DP Hornbuckle, RA Fisher, DB Estreich, "A manufacturing Process for Analog and Digital GaAs Integrated Circuits," IEEE Trans. Elect. Dev. **ED-29**, p1031-1037 (1982).

[4.23] THP Chang, "Proximity Effect in Electron-Beam Lithography," J. Vac. Sci. Tech. **12** p1271-1275 (1975).

[4.24] CE Binnie, SP Beaumont, CDW Wilkinson, "The fabrication of Very Short Gate Length N-Channel MOSFETs by Direct Write Electron-Beam Exposure," Proc. Microcircuit Engineering 82, Grenoble, France p44-49 (1982).

[4.25] WS Mackie, SP Beaumont, "Materials and Processes for Nanometre Lithography," Solid State Tech. Aug 1985, p117-121.

[4.26] H Fukui, "Determination of Basic Device Parameters of a GaAs MESFET," Bell Syst. Tech. J. **58** p771-797 (1979).

[4.27] Ref [4.6], Chapter 5.

[4.28] H Daembkes, W Brockerhoff, K Heime, A Cappy, "Improved Short-Channel GaAs MESFETs by use of Higher Doping Concentration," IEEE Trans. Elect. Dev. **ED-31**, p1032-1037 (1984).

[4.29] W Patrick, WS Mackie, SP Beaumont, CDW Wilkinson, "Very Short Gate-Length GaAs MESFETs," IEEE El. Dev. Lett. **EDL-6**, p471-472, (1985).

[4.30] The Monte-Carlo Simulations were carried out by Dr Al Mudares who is gratefully acknowledged.

[4.31] H Onodera, H Kawata, N Yokoyama, H Nishi, H Yagati, "High-Transconductance Self Aligned MESFET Fabricated Through AlN

Implantation," IEEE Trans. Elect. Dev. **ED-31** p1808-1813, (1984).

[4.32] T Onuma, A Tamura, T Uenoyama, H Tsujir, K Nishii, H Yagati, "High Transconductance Enhancement Mode GaAs MESFET Fabrication Technique," IEEE Elect. Dev Lett. **EDL-4**, p409-411 (1983).

[4.33] CL Chen, KD Wise, Transconductance Compression in Submicron GaAs MESFETs," IEEE Elect. Dev. Lett. **EDL-4**, p341-343 (1983)

[4.34] The MBE wafer was grown by Mr J Frost who is gratefully acknowledged.

[4.35] C Kacot, CA Stolte, "Backgating in GaAs MESFETs," IEEE Trans. Elect. Dev, **ED-29**, p1059-1064 (1982)

[4.36] MS Birrittella, WC Seelbach, H Goronkin, "The Effect of Backgating on the Design of GaAs Digital Integrated Circuits," IEEE Trans. Elect. Dev. **ED-29** p1135-1142 (1982).

[4.37] D Arnold, R Fischer, J Klem, F Ponse, H Morkoc, "Reduction of Backgating in GaAs/AlGaAs MESFETs by Optimisation of the Active-Layer/Buffer-Layer Interface," Elect. Lett. **20**, p376-377 (1984).

[4.38] CL Ghosh, RL Layman, "GaAs MESFETs with GaAlAs Buffer Layers," IEEE Elect. Lett. **EDL-5** p3-5 (1984).

[4.39] Useful discussions with CH Oxley at Plessey Research Centre on s-paramter measurements are gratefully acknowledged.

[4.40] TH Chen, MS Shur, "A Capacitance Model for GaAs MESFETs," IEEE Trans. Elect. Dev **ED-32**, p883-891 (1985).

5 Masking techniques and Device Interconnections

5.1 Introduction

Two useful processes were developed which can be used in GaAs device and circuit fabrication.

The first was to establish a reliable method of isolating devices using ion bombardment. The main advantage this method has over mesa isolation is that the planar surface of the GaAs can be maintained. Both proton and boron implantations were considered as a means of isolating devices. Eventually boron isolation was adopted mainly because the implantation faciltity available for this process was better suited to the shallow implants required for GaAs MESFETs (100 nm). A suitable system was developed for masking areas of the chips during implantation using metal on polymer masks. A novel method is decribed (Sect 5.4.5) for the fabrication of these masks using a positive on negative resist system. These resists were PMMA positive electron resist and polyimide which was found to be a negative electron resist.

The fabrication of device interconnections using polyimide bridges to crossover active elements on a chip was developed as a consequence of discovering that polyimide was a negative electron resist. Although no direct applications were found for this technique in this project, it does have obvious applications in GaAs integrated circuits fabricated by electron beam lithography. It is therefore described in section 5.5. of this chapter.

5.2 Ion Implantation For Device Isolation

5.2.1 Introduction

The use of mesa isolation is not ideally suited to the fabrication of GaAs MESFETs with extremely short gate lengths. This is because the gates have to be deposited over a step from the undoped GaAs buffer material, on which the gate pad is patterned, onto the mesa of active material which forms the source-drain channel. In the MESFETs described in chapter 4, the

height of this step ranged from 50 to 100 nm depending on the epitaxial n+ active layer thickness. At the mesa edge there is a thinning of the gate (sect 4.2.5.2) which can lead to the destruction of the gate patterns when relatively large voltages (up to -4 V) are applied to pinch-off the channel.

This problem can be eliminated using isolation by proton or boron ion implantation which effectively renders the GaAs epitaxial layer semi-insulating. This occurs because the damage which is caused by high energy ions entering the semiconductor causes many efficient deep level traps [5.1-5.3]. As a result, the implanted regions become highly resistive (M-ohm.cm) and leakage currents between isolated devices are reduced to an acceptably low level (often much less than a microamp).

During the implantation the source-drain channels have to be protected by masks thick enough to prevent any ions from entering the underlying semiconductor layer. When the mask is removed after implantation only the protected source-drain channels remain active. Therefore, MESFETs can be fabricated without having to pattern the gates over a step onto the active source-drain channel, thus improving the reliability of the very short gate devices. In addition, this method of isolation is clearly the only practical way to insulate devices produced on thin (80nm) GaAs membranes (Sect. 6.8).

5.2.2 Masking Difficulties.

The deposition of a masking layer, typically a thick gold layer, directly on to a GaAs wafer leads to problems when the mask has to be subsequently removed. The reason for this being that most wet or dry etching processes which could be used to remove the mask would also damage the underlying semiconductor.

An alternative masking technique is to deposit the gold layer onto an intermediate parting layer. The parting layer should be of a material which can be dissolved in a solution which will not damage the semiconductor. With a suitable parting layer, the primary mask can be lifted-off by dissolving the parting layer.

5.2.3 Development of Masking Techniques

A summary of work done in this department by WS Mackie [5.4] on proton implantation masks with different parting layers is given in the following section [5.3.1]. For various reasons, no suitable implantation masks were fabricated.

The present author developed a gold on arsenic trisulphide masking system for proton implantation (sect. 5.3.2). Some positive results were obtained using this system and it is possible that the technique could be refined to produce a reliable masking process. However, as the penetration depth of the protons, even at the lowest available energy (150keV), was so great that it was difficult to produce masks which would absorb all of the implanted ions, boron implantation was investigated. An ion implantation facility was available which could be operated at much lower energies (40keV) and was therefore more suitable for the small penetration depths (100nm) required for both MESFET and membrane isolation. The first masking system to be tested was the metal on polymer (MOP) masks described by Tennant [5.5,5.6]. This masking system was found to be suitable for boron implantation (sect 5.4.6) and was therefore employed in all subsequent isolation tests. A useful modification was made to the MOP mask fabrication procedure [5.7] in which the process was simplified by eliminating the need to use Reactive Ion Etching (RIE). The modified process was developed as a consequence of discovering that polyimide is in fact a negative resist and is described in section 5.4.5.

5.3 Proton Isolation

5.3.1 Original Proton Implantation Masks

Some work was done in this department by WS Mackie [5.4] to find a masking system which would be suitable for proton implantation. The implantation was carried out at the SERC ion implantation facility at Surrey University. The minimum proton energy available was 150 keV. At this energy the protons have a penetration depth of around 1.2 microns in gold and 1.8 microns in GaAs. This was far greater than the thickness of any epi-

layers which were used for MESFET fabrication (100 nm).

Three different masking systems were tested, with both polymer and inorganic parting layers. The primary masks were either gold or aluminium.

It was found that gold on polymer masks were inadequate as the polymer layer became cross-linked during the implantation making it difficult to remove afterwards. It should be noted that the uncovered polymer layer was not removed in these experiments and that no attempts were made to fabricate MOP type masks at this stage. Even if the surrounding polymer was removed before the proton implantation it is likely that the H^+ ions would have penetrated the gold masking layer and the underlying polymer would still have become cross-linked.

The second masking system to be tested consisted of an aluminium primary mask with a sodium chloride parting layer. This was found to be unsuitable because the adhesion of the metal primary mask to the inorganic parting layer was poor. Water absorption from the atmosphere was the probable cause of this poor adhesion.

Attempts to use the process described by D'Avanzo [5.8] were also unsuccessful. It was found that the calcium fluoride parting layers, reported by D'Avanzo as being "easily removable" in weak HCl, could not in practice be removed in 30% HCl assisted by ultra-sonic agitation. This method of masking was also abandoned.

5.3.2 Gold Masks With Arsenic Trisulphide Parting Layers

Subsequently gold masks were patterned, using lift-off, on arsenic trisulphide parting layers (fig 5.1a). Arsenic trisulphide was chosen as a possible parting layer for three main reasons:-

- It is easily dissolved in neat AZ developer [5.9].

- Gold adheres well to it.

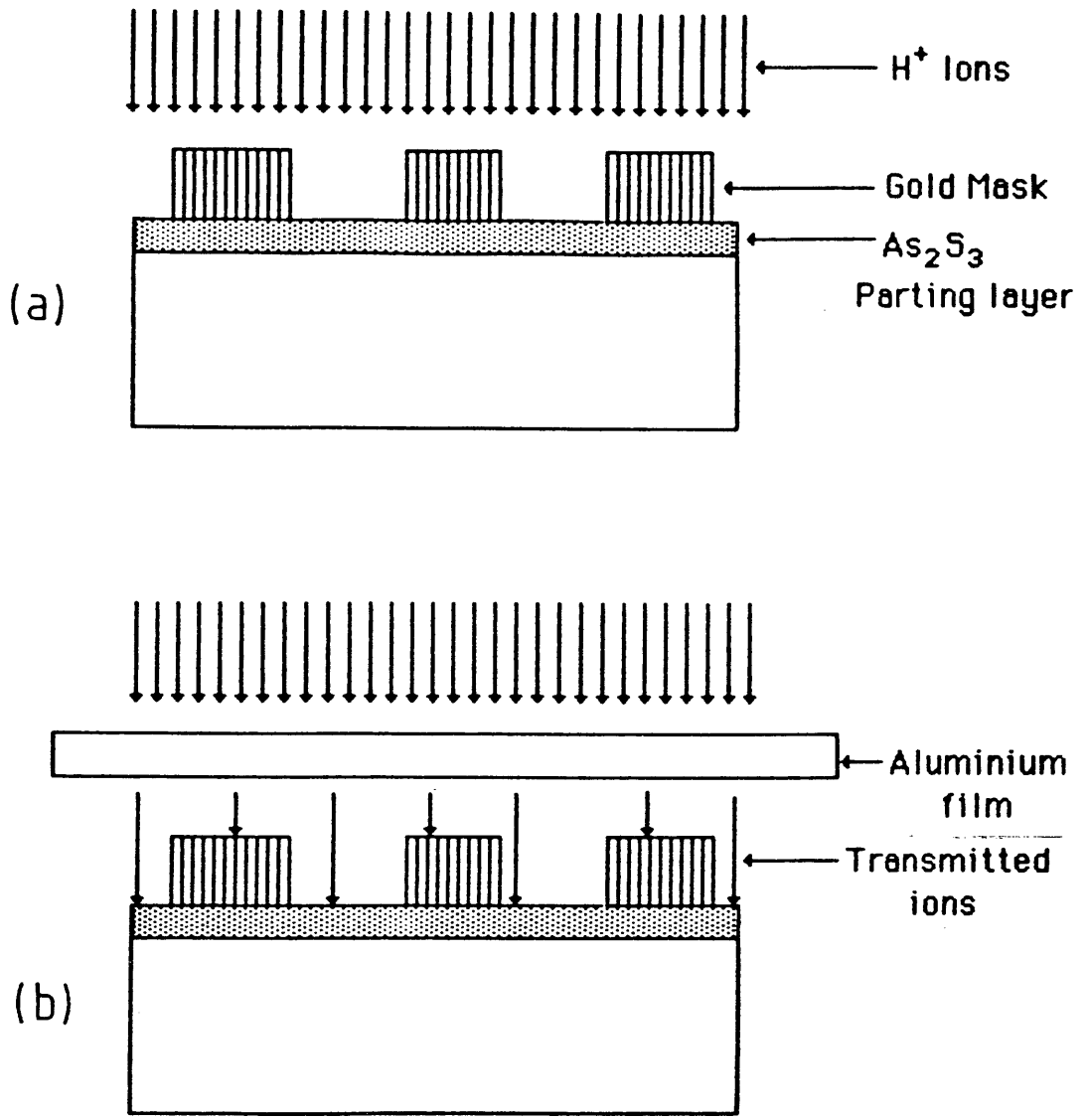


Fig. 5.1a) Arsenic-trisulphide/gold mask with no thin foil shielding.

Fig. 5.1b) Arsenic-trisulphide/gold mask with thin foil shielding.

- Thick layers (1 μm) can be evaporated.

Some gold on arsenic trisulphide masks were prepared on GaAs chips with an epitaxial active layer thickness of 85 nm. A 210 nm film of arsenic trisulphide was thermally evaporated on to the GaAs wafers. A layer of PMMA was then spin coated on to the As_2S_3 film, baked and then exposed using a 0.25 μm diameter electron beam. The PMMA was developed in 1:1 MIBK:IPA (23°C) and then a 500 nm gold layer was evaporated with a thin nichrome layer to enhance adhesion. The mask patterns, which would mask off areas suitable for TLM measurements (Sect. 2.2.2), were defined using lift-off. The masks were positioned relative to previously defined markers, to allow relocation of the masked areas when the implantation masks were removed.

Samples were sent to Surrey University for implantation. The proton dose was 4.10^{14} ions/cm^2 at an energy of 150 keV. After implantation the mask was easily removed by dissolving the arsenic trisulphide parting layer in neat AZ developer. AuGe/Ni/Au contacts were patterned on the TLM test strips using e-beam lithography These were than annealed to produce ohmic contacts (chap. 2). Unfortunately it was found that the gold mask layer, which was the thickest that could reasonably be evaporated and reliably lifted-off (about 500 nm), had not been thick enough to absorb all the implanted protons. Because the protons had penetrated the gold and arsenic trisulphide masking layers, the implanted samples were found to be completely insulating, even in the areas below the masks.

The above experiment was repeated only this time a thicker arsenic trisulphide layer (800 nm) was evaporated onto the wafer before the gold mask was patterned. The combined thickness of the gold and arsenic trisulphide layers (1.3 microns) was greater than the penetration of 150 keV protons through gold (1.2 microns). Again, after the implantation it was found that the protons had penetrated the masking layer and damaged the underlying semiconductor, rendering it highly resistive.

To reduce the range of the protons a thin aluminium film (18 um) was placed over the samples during further implants (fig

1b). The film was used to absorb some of the energy of the protons before they reached the masked wafer, thus reducing their penetration depth. The dose and energy of the protons were the same as before but it was not known what percentage of these protons actually passed through the aluminium film nor what energy they would have when the reached the specimen.

This method was found to be reasonable successful but the sheet resistance obtained from the masked GaAs, measured on TLM test strips patterned as before, was found to be twice the sheet resistance of the wafer before implantation (measured on a mesa structure). It was therefore likely that some protons still had sufficient energy to pass through the gold-arsenic trisulphide mask into the substrate below.

Although further improvements may have been made to this process using either a thicker layer of aluminium foil during the implant or by trying to produce thicker gold masks - in two lithographic steps for example - the technique on the whole did not seem to be very practical or efficient. The range of the protons through the gold masks, even when an aluminium film was employed to absorb some of their energy, was still greater than the thickness of gold which could be patterned easily.

5.4 Boron Implantation

5.4.1 Introduction

An alternative method of isolation is to use boron instead of proton implantation. In this case, because of their size, the boron ions have a much shorter range than protons of the same energy (approximately 30 %) [5.6]. An implantation facility was available at the SERC microfabrication facility at Edinburgh University but, as it was part of a silicon fabrication line, gold masks had to be avoided as the gold could have contaminated the system.

5.4.2 Metal on Polymer Ion implantation masks

Metal on polymer masks were fabricated using a thick germanium layer (0.8 μm), in place of gold, as the primary mask and polyimide as a parting layer. The initial masks were fabricated using Tennant's process [5.5,5.6] where the germanium mask was patterned by lift-off on a 350nm film of polyimide which was spin coated onto a GaAs wafer. A low power, oxygen plasma etch was used to remove the polymer not covered by the mask. The pressure was 100 mT and the etch time was 40 minutes to ensure that the germanium was sufficiently undercut to avoid cross-linking of the polyimide (sect 5.4.6).

The wafers were sent to Edinburgh University for implantation. A boron dose of 2×10^{13} cm^{-2} and energies up to 120 KeV were sufficient to isolate 200 nm of active material. The masks were removed by dissolving the polyimide layer in hot acetophenone. It was found that the masks had been effective during the implantation since the sheet resistance of the masked TLM stripes were the same as the unimplanted material. Therefore, boron implantation using metal on polymer masks was adopted as a means of isolating devices.

5.4.3 Modified MOP Mask

The modified MOP mask process, mentioned previously was developed as a result of discovering that polyimide is in fact a negative electron resist. The characterisation of polyimide as a negative resist is given in the next section. The modified MOP mask process is then described. An additional application for polyimide as a resist was found in the fabrication of circuit crossovers (sect.5.5).

5.4.4 Characterisation of Polyimide as a Negative Electron Resist

Polyimide, when cured at low temperature (<200°C), does not become cross-linked and can therefore be dissolved in an organic solvent such as acetophenone. However, it was discovered that when it is exposed by an electron beam the polyimide is cross-linked and becomes insoluble. Therefore polyimide is suitable for

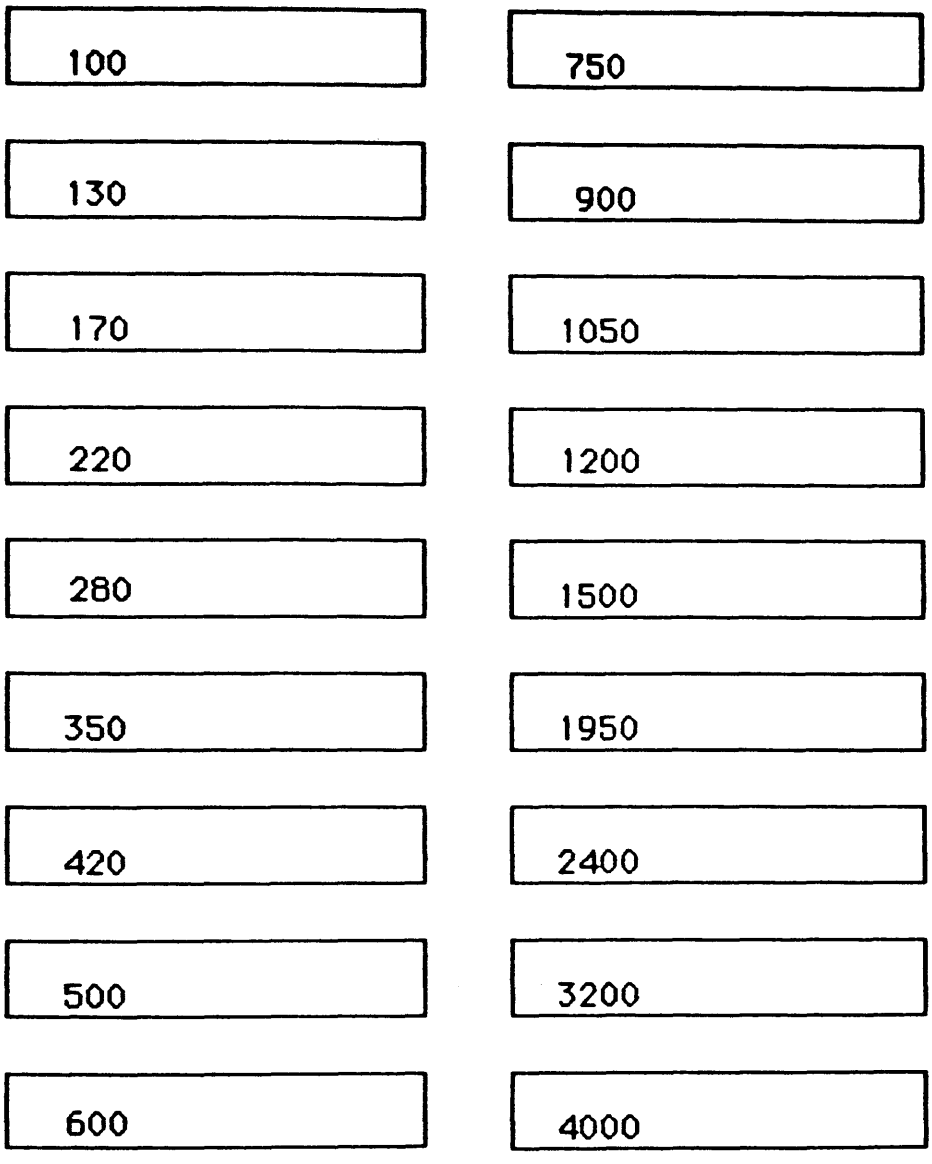


Fig. 5.2 Polyimide exposure test pattern.

use as a negative electron resist.

The polyimide used was preimidised Ciba-Geigy XU218 dissolved in 35:65 acetophenone:xylene. A 10% polyimide solution was spin coated on to clean GaAs wafers and then baked for 1 hour at 180°C. A spin speed of 5000 rpm was used to produce a uniform 350 nm thick film. An exposure test pattern consisting of a set of stripes 20μm wide and 30μm apart (fig 5.2) was exposed with a 500 nm diameter electron beam. The exposure dose ranged from 100 $\mu C/cm^2$ to 4000 $\mu C/cm^2$. After development the thickness of the resist was measured by talystep.

Figures 5.3 and 5.4 are typical developed thickness versus exposure curves for polyimide film thicknesses of 350 and 1400 nm respectively. A solution of 8:10 acetophenone:xylene at room temperature (21°C) was used as a developer. The development times were 2 and 8 minutes respectively. The contrast values obtained from the maximum slope of these curves were 2.14 and 2.15 which are high for a negative resist [5.10]. Also from these curves, the gel dose, which is the minimum exposure dose for the resist, is about 300$\mu C/cm^2$ in both cases. The significance of this particular number will be discussed in the MOP mask fabrication section (5.4.5.9).

The development rate can be increased by either heating the developer solution or, more practically, the acetophenone concentration can be increased. Stronger (or hotter) developer solutions not only reduce the development time but they dissolve all of the unexposed polymer; weaker solutions often leave deposits of resist on the substrate.

Figure 5.5 shows how the development rate of unexposed polyimide varies with the acetophenone:xylene ratio (at 21°C). It can be seen that the rate is constant for a ratio greater than 16:10. However, when stronger developers were used, the gel dose was increased from 300 $\mu C/cm^2$ in 8:10 solution to 550 $\mu C/cm^2$ in neat acetopenone. This is unlikely to be important when the resist is to be used as a negative resist since doses much higher than the gel dose would probably be used to ensure that the resist is completely cross-linked. Therefore, the best developer

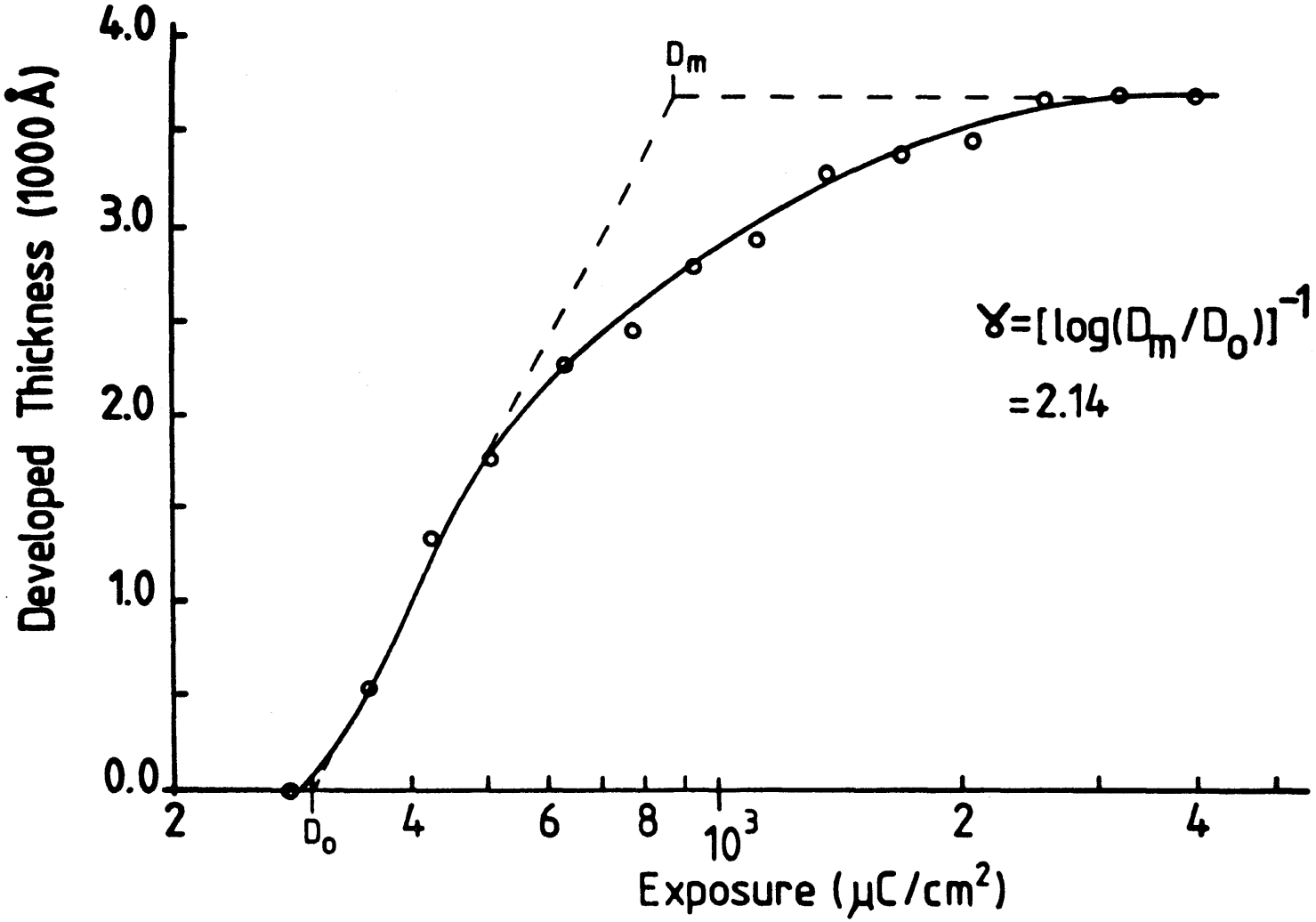


Fig. 5.3 Graph of developed polyimide thickness v exposure dose for a 350 nm polyimide layer.

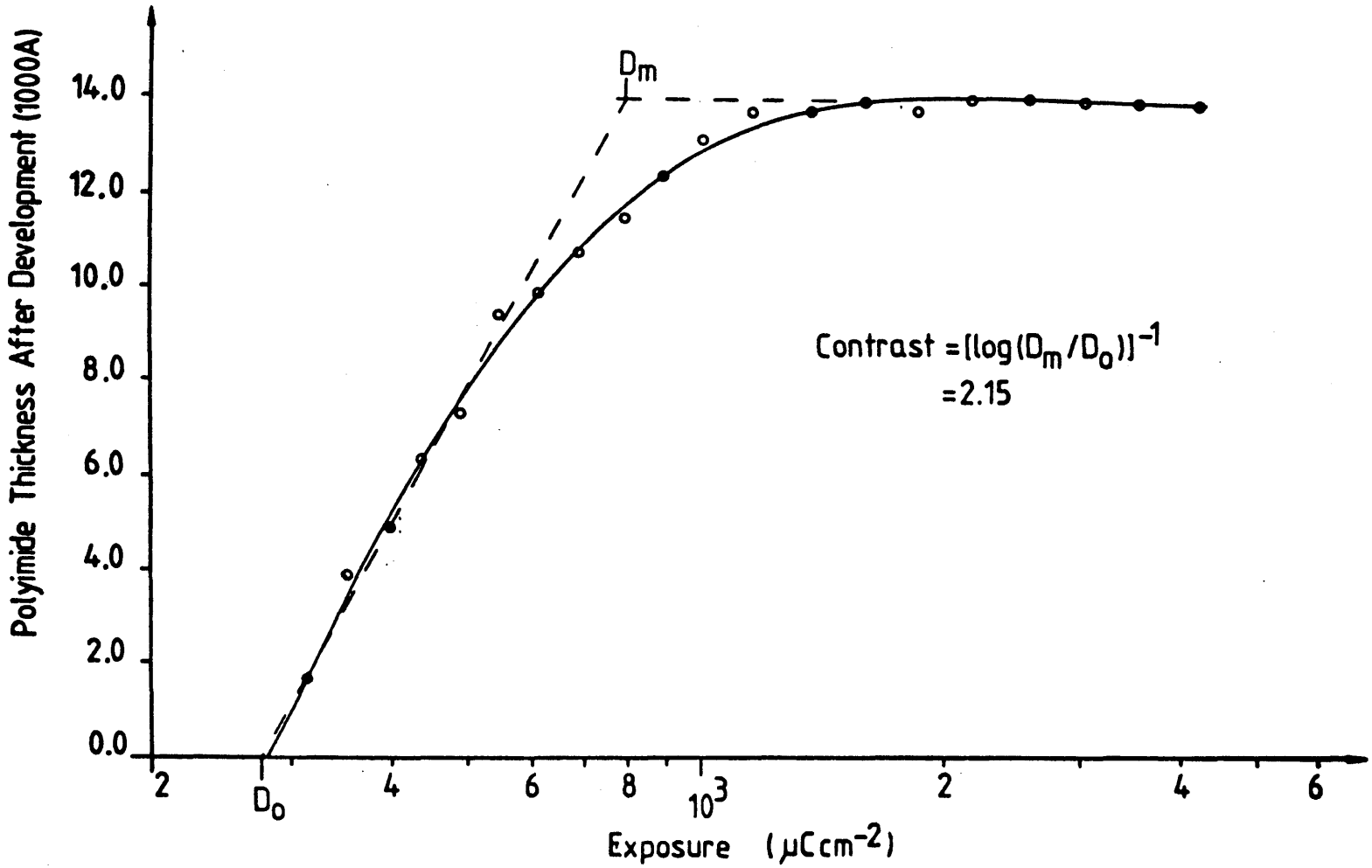


Fig. 5.4 Graph of developed polyimide thickness v exposure dose for a 1400 nm polyimide layer.

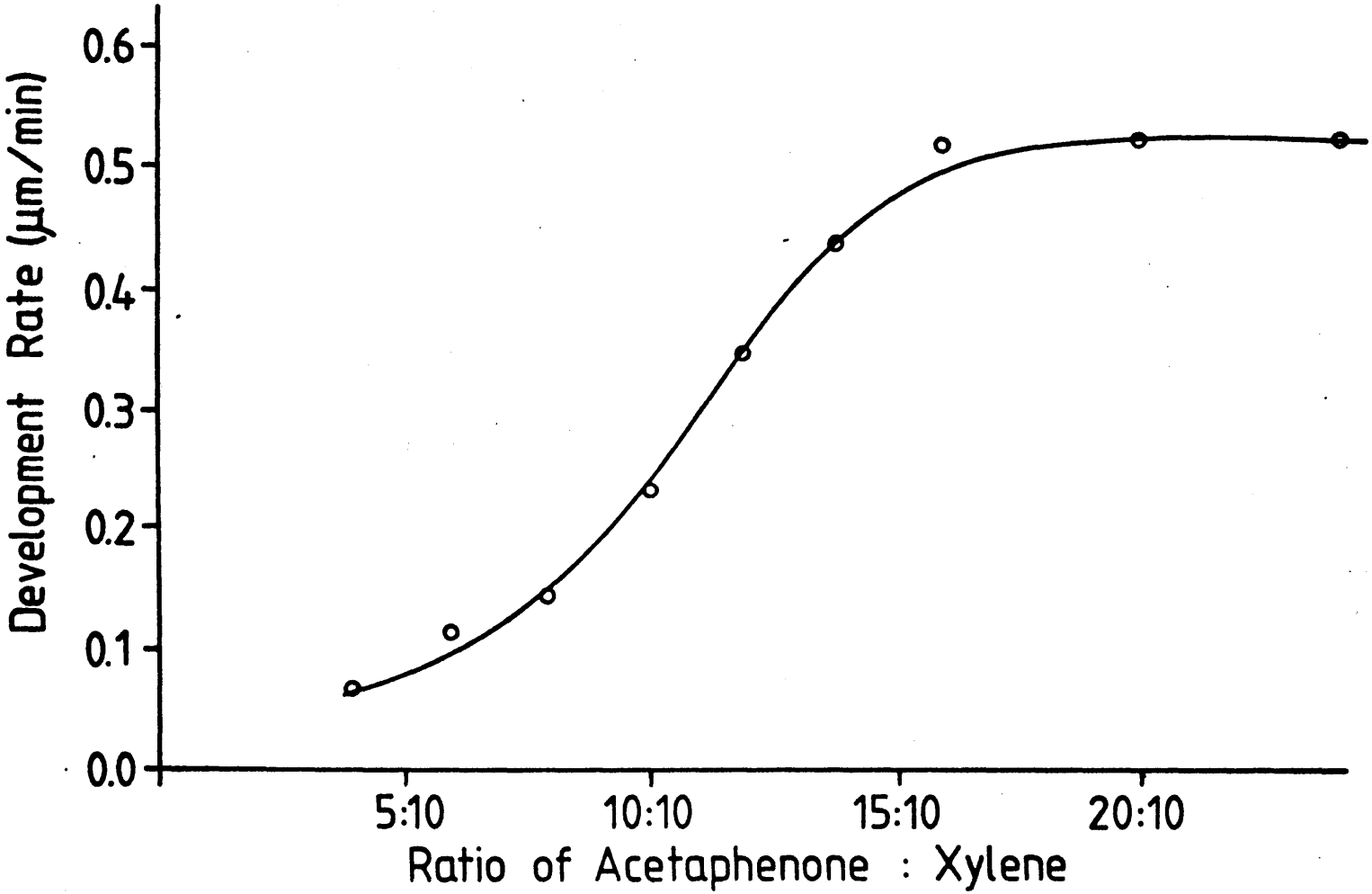


Fig.5.5 Graph showing the variation of development rate with the ratio of acetophenone:xylene.

for polyimide was chosen to be the 16:10 solution. This gives the maximum development rate (0.5 μm/min), a low gel dose (400 $\mu C/cm^2$) and completely dissolves the unexposed polyimide leaving the substrate clear of undeveloped particles.

The profile of the developed polyimide was found to be suitable for bridging circuitry due to its sloping rather than vertical side walls. These bridges will be described in section 5.5. Metal on Polymer masks were also fabricated making use of the negative electron resist properties of polyimide. In these masks a weaker developer solution had to be used as a low gel dose (300 $\mu C/cm^2$) is an essential feature of the process.

5.4.5 Modified MOP Mask fabrication Process

Metal on polymer masks were fabricated using a bi-layer, PMMA on polyimide resist system (positive on negative). A schematic of the fabrication process is given in figure 5.6. Polyimide was spin coated on a clean GaAs wafer at 5000 rpm for 1 minute then baked at 180^{o}C for 1 hour. A layer of low molecular weight PMMA (15% in chlorobenzene) was spun on top of the polyimide at 6000 rpm. The samples were then baked for a further 2 hours at 180^{o}C. The respective polymer thicknesses were 0.35 and 1 μm.

The mask patterns were exposed using a 0.25 um diameter electron beam. An exposure dose of 350 $\mu C/cm^2$ was used. This was previously determined to be the optimum dose for reliable lift-off of thick germanium films. It should also be noted that 350 $\mu C/cm^2$ is just greater than the gel dose for polyimide developed in 8:10 solution.

The PMMA was developed for 1 minute in 1:1 IPA:MIBK solution at 23^{o}C. A thick germanium film (0.8 μm) was then thermally evaporated and the mask patterns defined using lift-off. A thin nichrome film was deposited before the germanium to promote adhesion to the polymer layer. It was found that lift-off was more reliable when the samples were immersed in acetone as soon as they were removed from the vacuum system. At this point the germanium film was soft and easily scratched with tweezers.

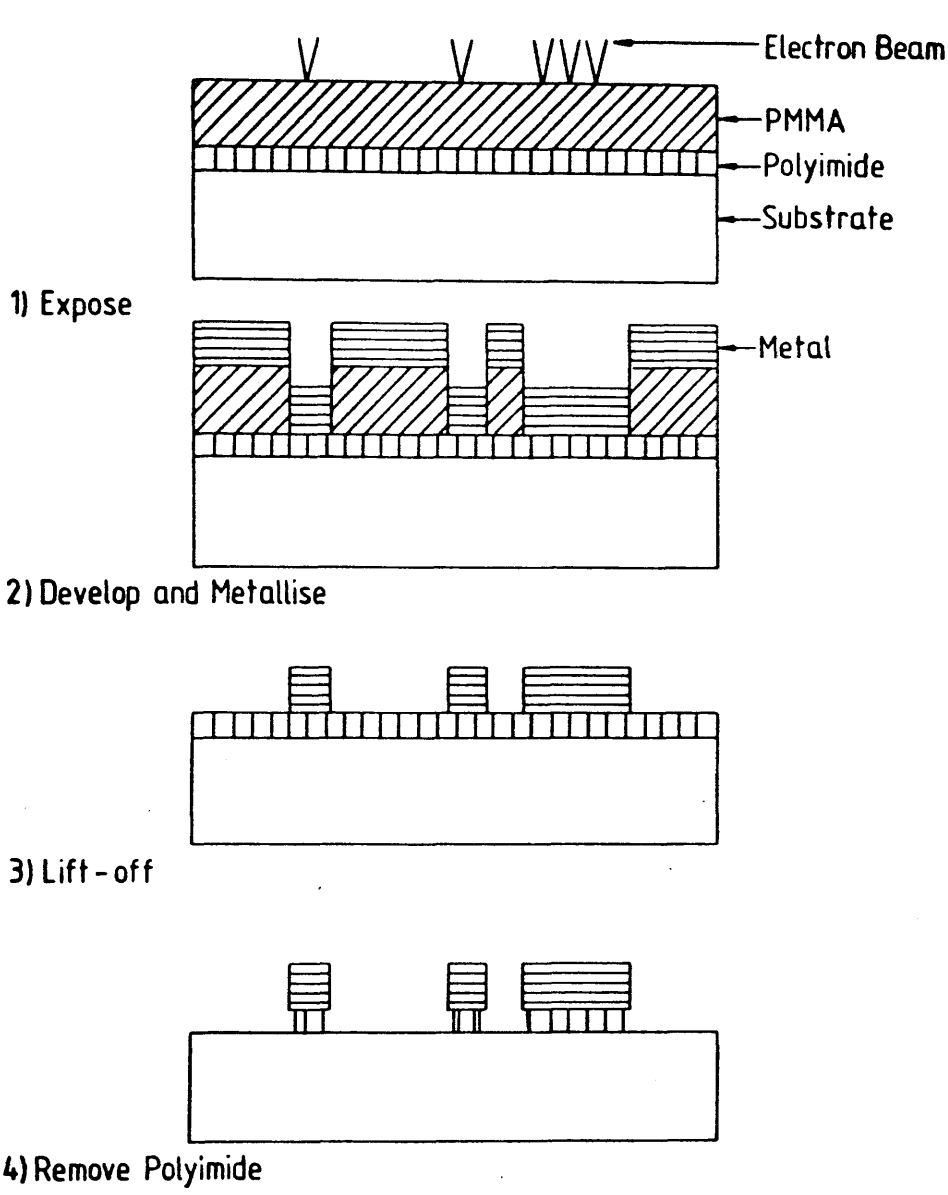


Fig. 5.6 Schematic diagram of the MOP mask fabrication process.

However, when the film was exposed to atmosphere for more than a few minutes it became extremely difficult to scratch. When this happened the time taken for the solvent to dissolve the PMMA increased and lift-off often had to be completed using ultrasonic agitation.

After lift-off the uncovered polyimide was removed by dissolving it in 8:10 acetophenone:xylene solution; effectively developing the polyimide resist. When the mask pattern was exposed, the polyimide under the mask was cross-linked but, because of the relatively low dose, was not completely insoluble in the polyimide developer (see fig. 5.3). Therefore, an undercut, particularly desireable in MOP ion implantation masks, was produced by dissolving the unexposed polyimide and partially dissolving the polyimide under the germanium mask. Varying the development time controlled the amount of undercutting obtained.

Figure 5.7 contains three scanning electron micrographs of the profiles obtained for three different development times. The top micrograph is of a sample developed for 2 minutes which was the time taken to clear the uncovered polyimide. There is no undercutting of the germanium. The development times for the centre and lower micrographs were 5 and 10 minutes respectively. These exhibit good undercut profiles. Both of these would be ideal for use as an ion implantation mask as there is no possibility of the polymer below either mask becoming cross-linked by the ion beam.

5.4.6 Chemically Produced MOP Masks versus Plasma Etched

A set of MOP masks were fabricated using oxygen plasma etching to remove the uncovered polyimide. The etching was carried out in a low power asher (10W rf power) at a pressure of 100 mTorr. Etch times were: 20 minutes (the time taken to clear the substrate) and 30 and 40 minutes. Figure 5.8 shows the profiles obtained for each of these etch times (top to bottom respectively). The 20 and 30 minute etches produced masks which do exhibit some undercutting but, in both samples there was a polyimide "tail" extending beyond the germanium edge. This tail would be exposed to the ion beam during implantation, becoming

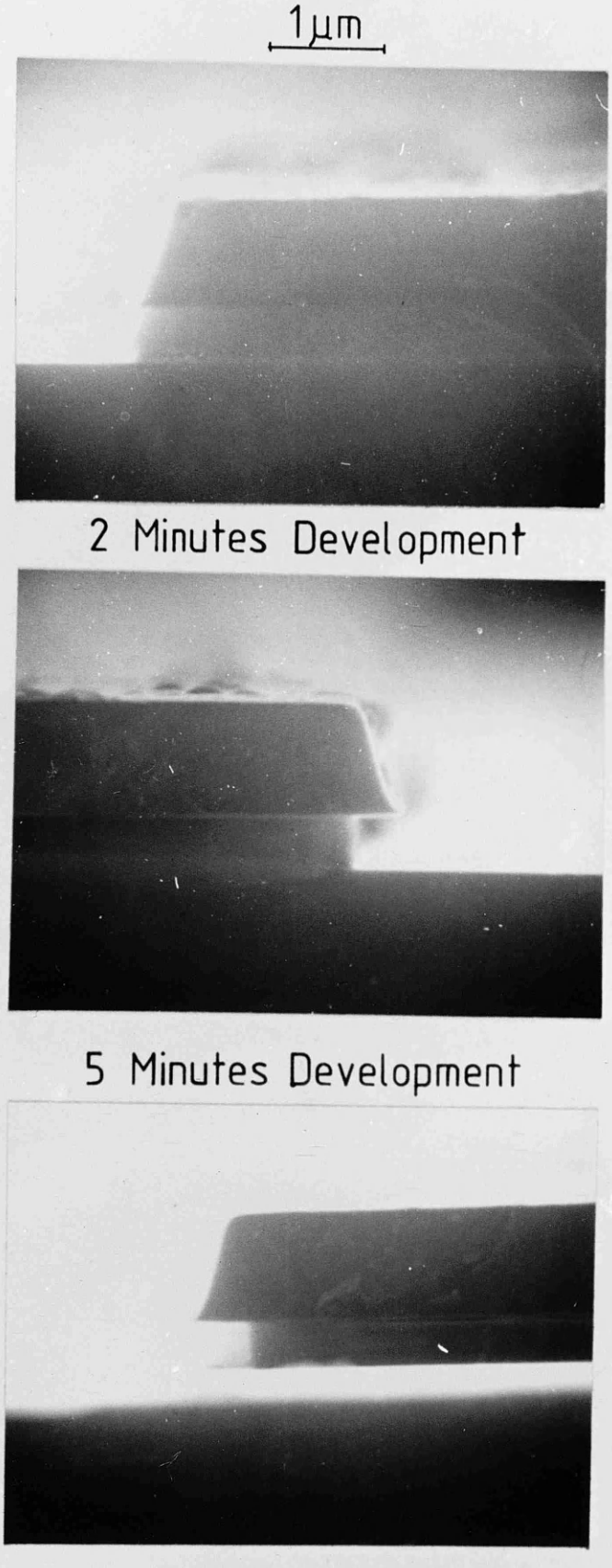


Fig. 5.7 SEM micrographs of MOP masks where the polyimide layer was developed for 2, 5 and 10 minutes in acetophenone:xylene.

Fig. 5.8 SEM micrographs of MOP masks where the polyimide layer was etched for 20, 30 and 40 minutes in an oxygen plasma.

cross-linked and subsequently difficult to remove. The sample which was etched for 40 minutes does not have this polymer "tail" and would therefore be suitable for use as an implantation mask.

MOP masks were fabricated on 85 nm n^+ GaAs epi-layers using both plasma etching (30 min) and chemical development (5 min). The wafers were implanted at Edinburgh University to isolate the masked regions (2.10^{13} ions/cm^2, 40 and 80 keV). After implantation the MOP masks were removed by dissolving the polyimide parting layer in boiling acetophenone. This was essential as the polyimide had become slightly cross-linked during the exposure of the mask patterns. On some occasions parts of the mask would remain after the parting layer was dissolved. However, this could readily be resolved by placing the wafer in an ultrasonic bath for a few seconds. If this also failed, as a last resort, the remainder of the mask could be removed by gently swabbing the wafer with a cotton bud.

When the masks had been removed, the surface of the wafer masked using the chemical fabrication technique was perfectly clean. However, on the wafer masked by the dry etched mask the outline of the mask was left on the substrate. This indicated that the sample had not been etched for long enough and that the polyimide tails had, as already predicted, become cross-linked during the implantation. The outline pattern was completely insoluble and could not be removed even by ultra-sonic agitation.

5.4.7 Discussion

This test showed that the modified MOP mask fabrication technique was more reliable in that the masks were more readily removed after implantation. The fabrication time was also much shorter using the new technique since the polyimide could be developed as soon as lift-off of the germanium pattern was completed. Even neglecting the pump-down time of the vacuum system, the time taken to dry etch the uncovered polyimide was eight times longer than the time taken to remove the polymer by solvent. The dry etching process would be much shorter, and better profiles might have been obtained, if high power RIE was used to remove the unwanted polymer layer. However, the pump-down

time of the system would still make this method longer than the modified method.

5.5 Circuit Crossovers Using Polyimide Bridges

5.5.1 Introduction.

A further application for negative polyimide resist was found in the fabrication of circuit crossovers.

Interconnections between devices on a chip often have to be made across previously defined patterns. This is normally achieved by depositing a dielectric layer over the entire chip and then interconnecting devices via holes etched through the dielectric layer [5.11]. This procedure requires a masking and dry etching step for the fabrication of the vias then another lithographic step to define the interconnections. In the following sections a process is defined in which parts of the circuit to be crossed are protected with a layer of polyimide, patterned by e-beam lithography. Although no direct application for circuit crossovers was used in the work of this thesis, it is likely that the process will be used in the fabrication of ring oscillators by others in the group.

5.5.2 Interconnecting Techniques

A comparison between conventional interconnections and the polyimide bridging technique is given in figure 5.9.

In figure 5.9a) the 1st and 2nd metal levels are separated by a dielectric layer, usually silicon dioxide. Interconnections are made via holes dry etched through the dielectric layer. The 2nd level metallisation has to be thick enough to fill the via holes to ensure that there is a continuous contact between the metal in the hole and the interconnection itself.

A more elaborate process, but similar to the previous one, is illustrated in fig 5.9b) [5.12]. At the point where a connection is to be made a hole is ion milled through the 2nd level metallic layer, through the dielectric layer and part way

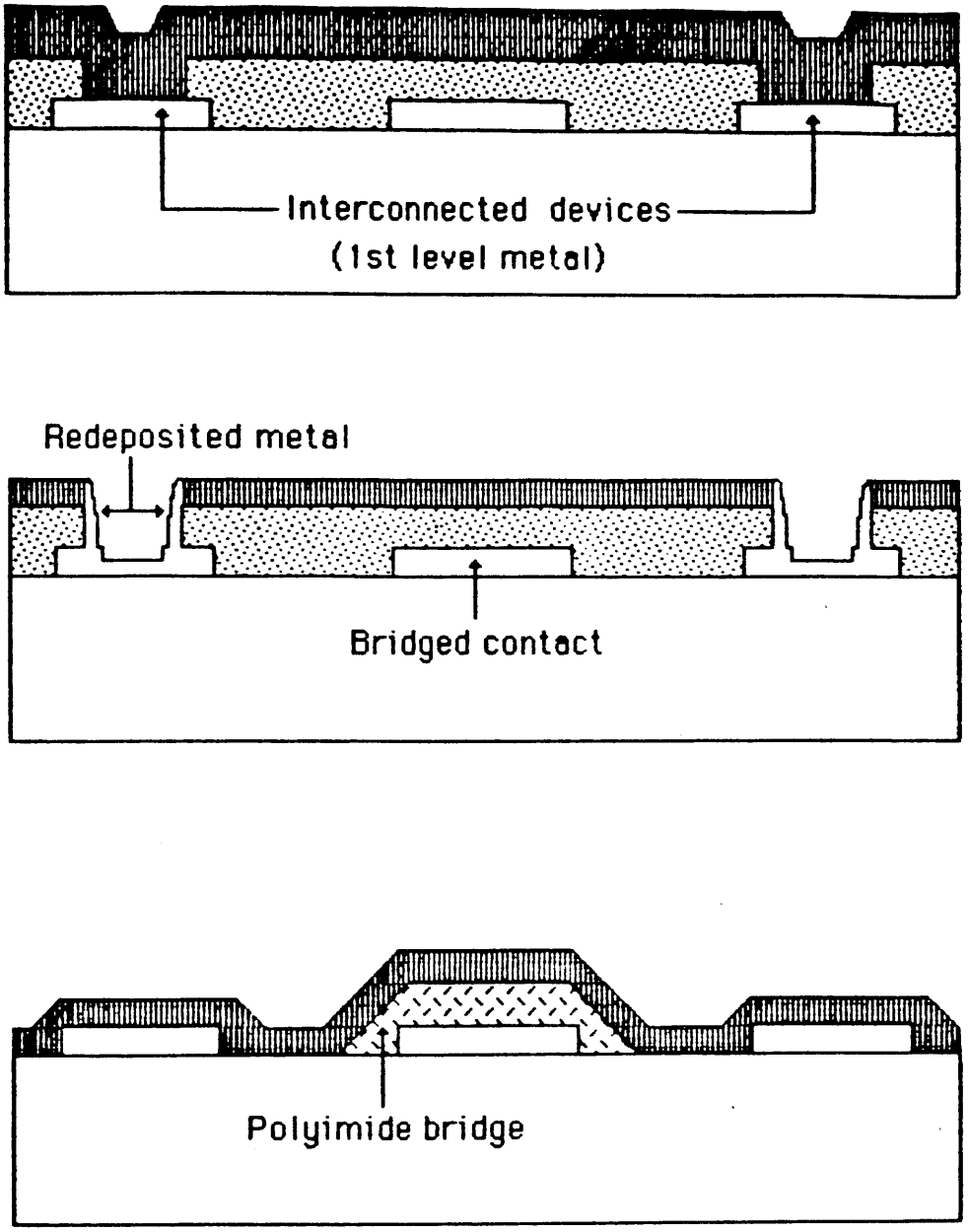


Fig. 5.9 Schematic diagram showing various techniques for interconnecting devices on an integrated circuit.

into the lower metallic layer using a focussed ion beam. The ion beam scan is then reduced to cover only the centre of the via. The first level metal is then sputtered and partly redeposited on the vertical walls forming a short circuit. Although efficient contacts were reported using this method the time taken to produce each short circuit was almost 4 minutes for 3 x 3 μm dimensions.

The polyimide bridging technique is shown in figure 5.9c). A polyimide stripe straddling the part of the circuit to be crossed is patterned by electron beam lithography. The interconnections can then be made by patterning the 2nd level metallic layer over the polyimide bridge in another lithographic step. Clearly this method is a lot simpler than the previous methods described, particularly when e-beam lithography is being used for all other pattern definition steps, as it only requires two straight forward lithographic steps. There is no need for dry etching or ion beam processing.

5.5.3 Fabrication of Crossovers

When polyimide is used as a negative resist, the developed lines have sloping walls angled from 45^{o} to 60^{o} depending on exposure and development conditions. Figure 5.10 shows the end profile of a polyimide stripe (1 μm wide and 0.7 μm thick) after development. The exposure dose was 1700 $\mu C/cm^2$ and the developer used was 16:10 acetaphenone:xylene. A development time of 90 seconds was required to clear the substrate of unexposed resist. This type of profile is ideal for the fabrication of crossovers because continuous metallic lines can readily be patterned over the polyimide edges using lift-off.

5.5.4 Test Circuit

To test the effectiveness of crossovers fabricated using polyimide bridges to insulate circuit levels the test pattern shown in figure 5.11a) was developed. Circuits were fabricated on silicon wafers coated with an insulating layer of silicon nitride. The first level metallisation was the horizontal bars connected to the two probing pads on the left hand side. The

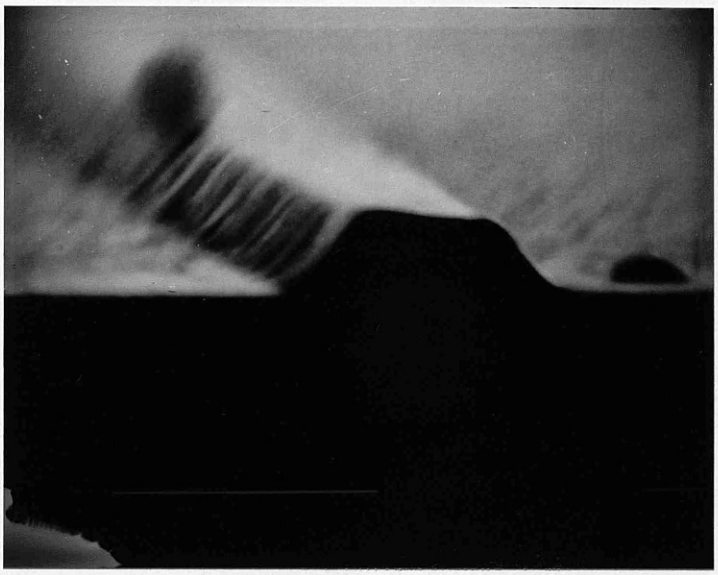


Fig. 5.10 SEM micrograph of a section taken through a developed polyimide line. The marker is 1 um.

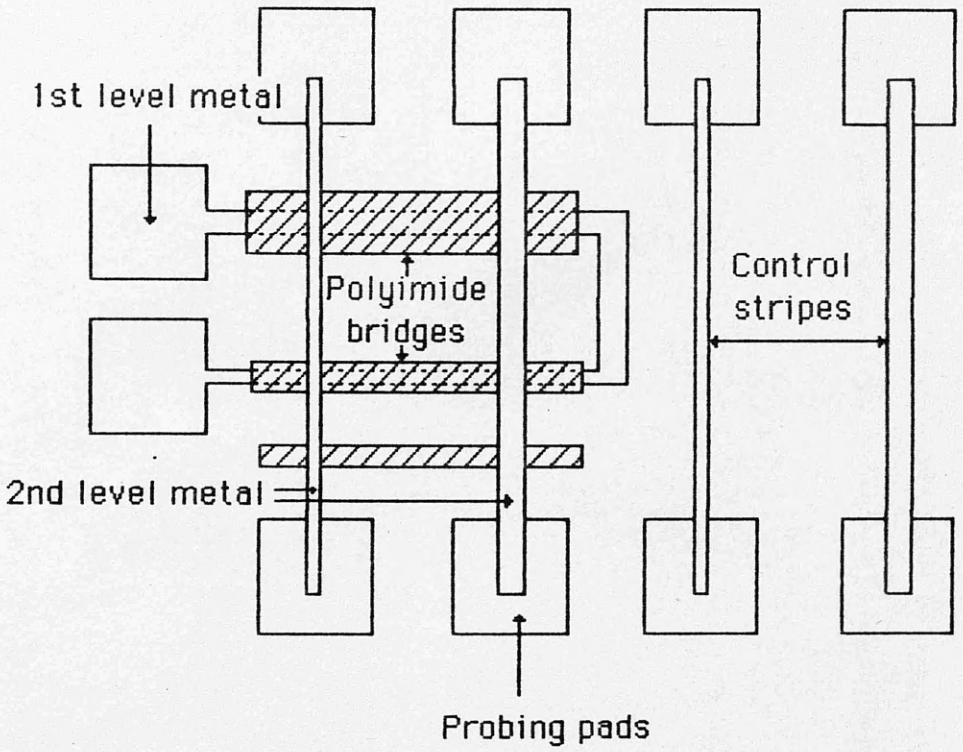


Fig. 5.11a) Circuit to test the reliability of polyimide bridges.

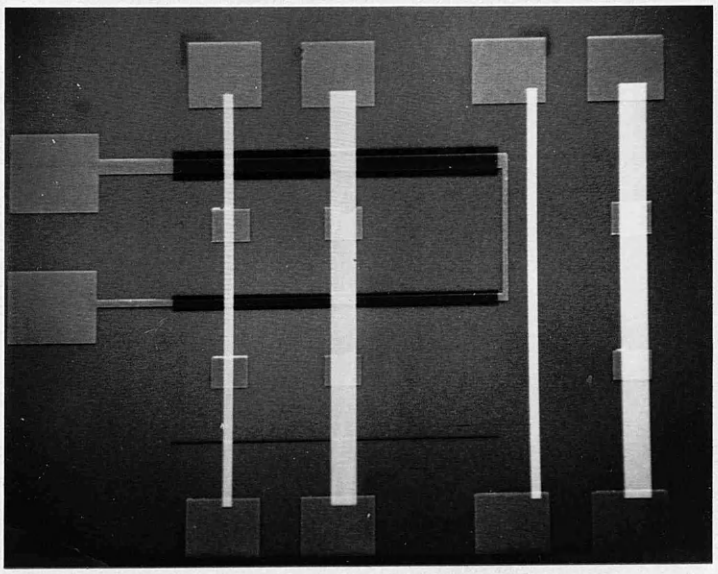


Fig.5.11b) Micrograph of the test circuit shown in a) fabricated on a silicon nitride coated silicon wafer.

bars were patterned by electron beam exposure of low molecular weight PMMA, followed by development in 1:1 IPA:MIBK and then metallisation (100nm Au) and lift-off. Polyimide (350nm) was then spin coated onto the wafer and baked for 1 hour at 180°C. Next three stripes were exposed, two of which straddled the previously patterned gold lines, using crude alignment to the corners of the probing pads (see section 4.2.2 for alignment techniques). The unexposed polyimide was removed by developing in 16:10 acetophenone:xylene for 1 minute. Two sets of gold stripes were then patterned as before, one set crossing the polyimide bridges while the other was deposited directly on to the substrate. The dimensions of the wide and narrow gold stripes were 15 and 8 microns respectively. The polyimide stripes were approximately twice the widths of the underlying gold stripes. An SEM micrograph of a completed test circuit is given in figure 5.11b).

5.5.5 Results

When these circuits were tested, using an HP 414A semiconductor parameter analyser, it was found that the resistance of a gold stripe passing over the three polyimide bridges was not significantly different to a stripe of the same dimension patterned directly on to the substrate. In fact the resistance of the crossover stripes was sometimes less than that of the lines patterned on the substrate. This indicates that the resistance variations observed were primarily due to slight variations in the stripe widths and were not associated with the polyimide bridge steps.

As a second test, a voltage was applied between the substrate and crossover stripes and the leakage current through the polyimide measured (HP 4145). It was found that a negligible current of less than 10 nA passed between the stripes for potential differences up to 50 volts (fig 5.12). No significant leakage current was observed until about 70V was applied across the bridge. Above 70 V the leakage current rose exponentially to approximately 1 mA with 100 V applied. Most of the bridges tested up to 100 V at the time of fabrication showed no physical signs of breakdown although when the samples were retested some

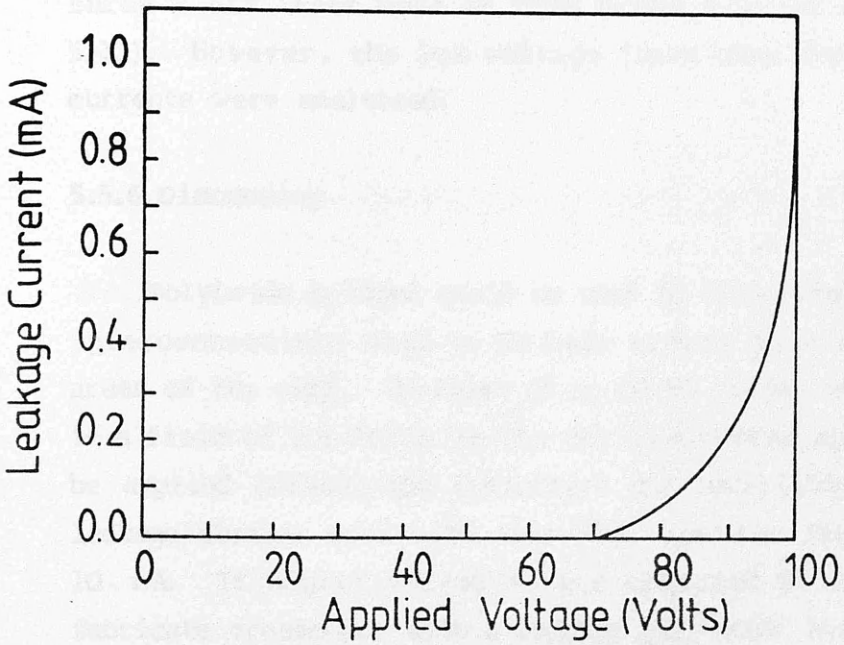


Fig.5.12 Graph of leakage current v applied voltage across a polyimide bridge. The polyimide thickness was 350 nm.

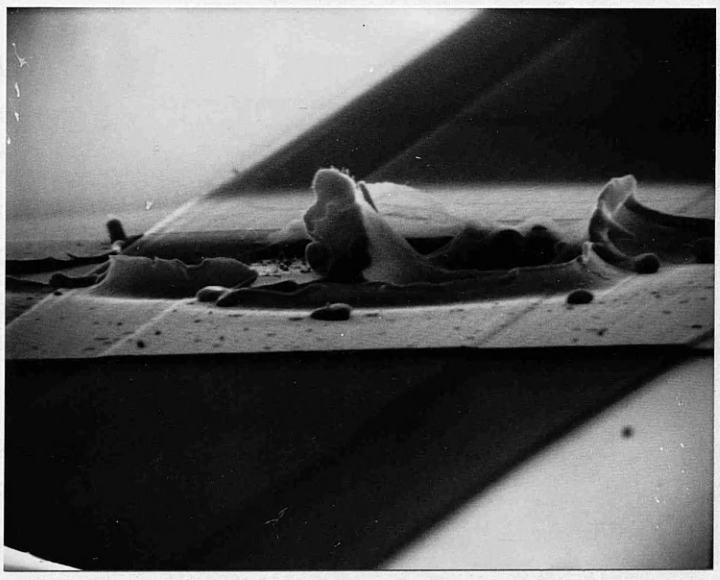


Fig.5.13 SEM micrograph of a device after 100 V was applied between the crossover connections and the substrate connections.

three weeks later most of them broke down at about 80 V (fig 5.13). However, the low voltage (less than about 50V) leakage currents were unaltered.

5.5.6 Discussion

Polyimide bridges could be used in integrated circuits where interconnections need to be made across previously patterned areas of the chip. Voltages of up to 50 volts, which corresponds to a field of 1.4 MV/cm in the devices tested above, can safely be applied between the crossovers and underlying circuits. The leakage current even with this high electric field is less than 10 nA. If higher voltages were required it would be easy to fabricate crossovers with a thicker polyimide insulating layer.

This method of device interconnection would be particularly applicable to processes in which electron beam lithography is used as the only pattern definition tool. Because of the relatively low sensitivity of polyimide, it is unlikely that the method would have commercial applications, but in a research environment it could be useful, particularly in the development stage.

Chapter 5 References

[5.1] J.P. Donnelly, F.J. Leonberger, "Multiple-Energy Proton Bombardment in n^+ GaAs," Solid State Electronics, **20**, 183-189 (1977).

[5.2] J.M. Zavada, H.A. Jenkinson, R.G. Wilson, D.K. Sadana, "Depth Distribution and Damage Characteristics of Protons Implanted in N-Type GaAs," J. Appl. Phys. 57, 2299-2301 (1985).

[5.3] J.C. Dyment, J.C. North, L.A. D'Asaro, "Optical and Electrical Properties of Proton-Bombarded P-Type GaAs," J. Appl. Phys. **44**, 207-213 (1973).

[5.4] W.S. Mackie, PhD Thesis, Glasgow University (1984).

[5.5] D.M. Tennant, "Metal on Polymer Ion Implantation Mask," J. Vac. Sci. Technol. B1, 494-496 (1983).

[5.6] P. Grabbe, R.E. Howard, E.L. Hu, D.M. Tennant, "Metal on Polymer Masks for Reactive Ion Etching," Proc. 10th International Conference on Electron and Ion Beam Technol. Montreal, Canada (Electrochemical Society, Pennington NJ 1983).

[5.7] W. Patrick, W.S. Mackie, S.P. Beaumont, C.D.W. Wilkinson, "Polyimide as a Negative Electron Resist and its Application in Crossovers and Metal on Polymer Mask Fabrication," Proc. 29th International Symposium on Electron, Ion and Photon Beams, Portland, Oregon (1985). Proceedings to be published in J. Vac. Sci. Technol B (Jan 1986).

[5.8] D.C. D'Avanszo, "Proton Isolation for GaAs Integrated Circuits," IEEE Trans. Electron Devices, **ED-29**, 1051-1059 (1982).

[5.9] Shipley AZ Photoresist developer.

[5.10] "E-Beam Techniques in Microelectronic Fabrication," G.R. Brewer p110, Academic Press (1980).

[5.11] S.I. Long, B.M. Welch, R. Zucca, P.M. Asbeck, C.P. Lee, C.G. Kirkpatrick, F.S. Lee, G.R. Kaelin, R.C. Eden, "High Speed GaAs Integrated Circuits," Proc. IEEE **70**, 35-45 (1982).

[5.12] J. Melngailis, C.R. Musil, E.H. Stevens, M. Utlaut, E.M. Kellog, R.T. Post, M.W. Geis, R.W. Mountain, "Focussed Ion Beams Applied to Integrated Circuit Restructuring," Ref. 5.7

6.1 Introduction

In this chapter, the fabrication processes required for producing devices (MESFETs in this case) on active membranes of GaAs, are described. Previously, WS Mackie had developed a process for fabricating GaAs membranes [6.1,6.2], but at that time it was not possible to consider making any devices because a reliable isolation technique had not been developed. However, with the development of metal on polymer ion implantation masks for boron isolation the fabrication of membrane devices was made possible.

Using thin substrates, the very high resolution capabilities of electron beam lithography can be used to fabricate devices with dimensions much smaller than can be achieved on solid substrates. Although the length of the gates will not necessarily be reduced by a significant amount, the source-drain separation can be decreased thus reducing the parasitic channel resistance. The reason small gaps cannot be reliably fabricated on solid substrates is that the exposure latitude for closely spaced patterns is small [6.3,6.4]. Ideally, a test exposure would have to be done every time gaps of less than say 1 μm were to be fabricated. This would not only be time consuming, but, even when the optimum exposure for the test pattern was found, it would be difficult to maintain exactly the same exposure, development, and pre-evaporation etching conditions for fabricating the actual devices.

On thin substrates on the other hand, the exposure latitudes are wider and closely spaced patterns are much more reliably produced [6.3]. This is because the number of electrons backscattered from the substrate is small, (compared with solid substrates), so proximity effects are greatly reduced. Therefore, MESFETs with source drain separations of say 100 nm and gate lengths down to 10 nm could be fabricated without too much difficulty. With these very small dimensions, electrons would have a reasonable chance of being transfered ballistically between contacts, even at room temperature [6.5]. It has been

shown, using Monte Carlo particle simulation, that such a device would exhibit high drain currents and transconductance values, typically 2-3 times greater than a long channel MESFET [6.6]. A high resolution alignment technique had already been developed in the department which could be used for positioning the gates in the centre of the source-drain gap to an accuracy of 5 nm [6.7].

6.2 Chapter Outline

If ion implantation is to be used to isolate devices on a membrane, for obvious reasons it would be far better to carry out the isolation step (and first level contact patterning) before the membranes are fabricated. If this is done however, the etch mask on the back of the wafer has to be aligned in such a way that, when the membranes are fabricated, they coincide with the isolated regions. To achieve this a back to front alignment technique was developed, first on silicon wafers and then on GaAs. This process is described in detail in the next section.

Modifications had to be made to the membrane fabrication process [6.1,6.2] because a different source of material was used. This material was different to the previous batch and as such different etching rates, etc. were obtained. The fabrication process, including the modifications is given in section 6.5.6. Tests were carried out on completed membranes to find out if they could withstand repeated lithographic steps (spinning, lift-off etc) and to ensure that ohmic contact annealing did not damage the membranes. It is shown that the membranes could withstand relatively harsh treatment and that actual device fabrication was viable (sect 6.6).

The processing steps for a real device are then given. Devices were fabricated up to the point where ohmic contacts were annealed and tested to find out if a current could be passed through the active regions of the membrane. The results of these tests unfortunately signified the end of these membrane devices, but it is shown that hope for future devices with different material specifications, is still high.

6.3 Back to front Alignment

The first back to front alignment experiments were made on silicon wafers coated on both sides with silicon nitride. The silicon nitride was deposited by Chemical Vapour Deposition (CVD) at the SERC Microfabrication Facility at Edinburgh University. The wafers were approximately 350 μm thick with 60 nm of nitride on both the polished (front) and the unpolished (back) surfaces. These wafers were readily available in the department where they were being used for silicon nitride membrane fabrication [6.8]. Essentially the alignment technique involved etching two (or more) wells all the way through the silicon wafer and then using these wells for positioning of the back etched wells. The procedure for back to front alignment is given in the following sections. A schematic diagram of the alignment technique is shown in fig. 6.1.

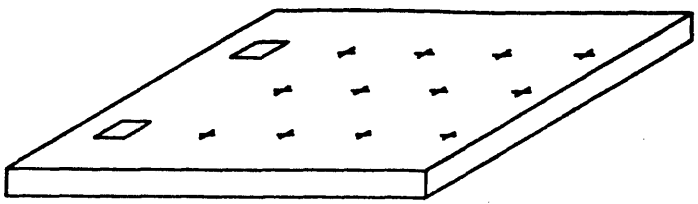
6.3.1 Alignment Test Pattern

The alignment test pattern used in these experiments is shown in fig. 6.2. The two large rectangles (620 μm square) are the windows for etching the alignment wells through to the back of the wafer. The markers in this case were crosses 220 μm long by 15 μm wide. It was thought that the markers would only etch shallow V-shaped grooves (stopping on the (111) planes) in the silicon during the etching of the alignment wells. However, because of the anisotropic nature of the silicon etch (sect 6.3.4), it was found that a relatively deep pyramidal well was etched at the centre of each marker. These wells were used to test the alignment of the back etched wells. The windows and markers were exposed using a frame size of 1.5 by 1.2 mm on wafers measuring 8 by 6 mm. The location of the exposure sites relative to the left hand corners of the wafer were determined using the POSITION program described previously (sect 4.2).

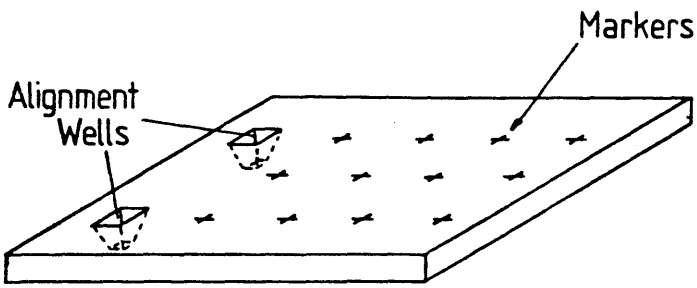
6.3.2 Resist Coating

A layer of Shipley AZ 1350J photoresist was spin coated on to the front surface (polished) of the nitride covered silicon

(1) Pattern resist.



(2) Etch alignment wells.



(3) Align. Expose and develop resist. Etch from the back of the wafer.

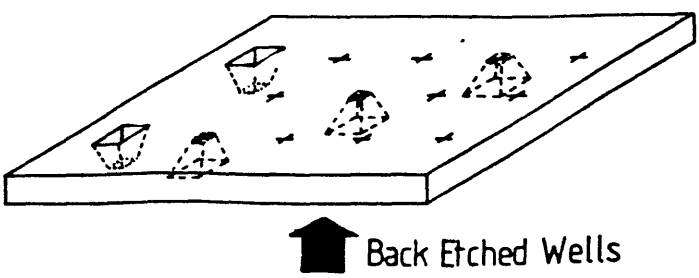


Fig. 6.1 Schematic representation of the back to front alignment technique. Two alignment wells are etched relative to the other exposure sites on the surface of the wafer. These wells are then used for posiioning the windows for the back etched wells.

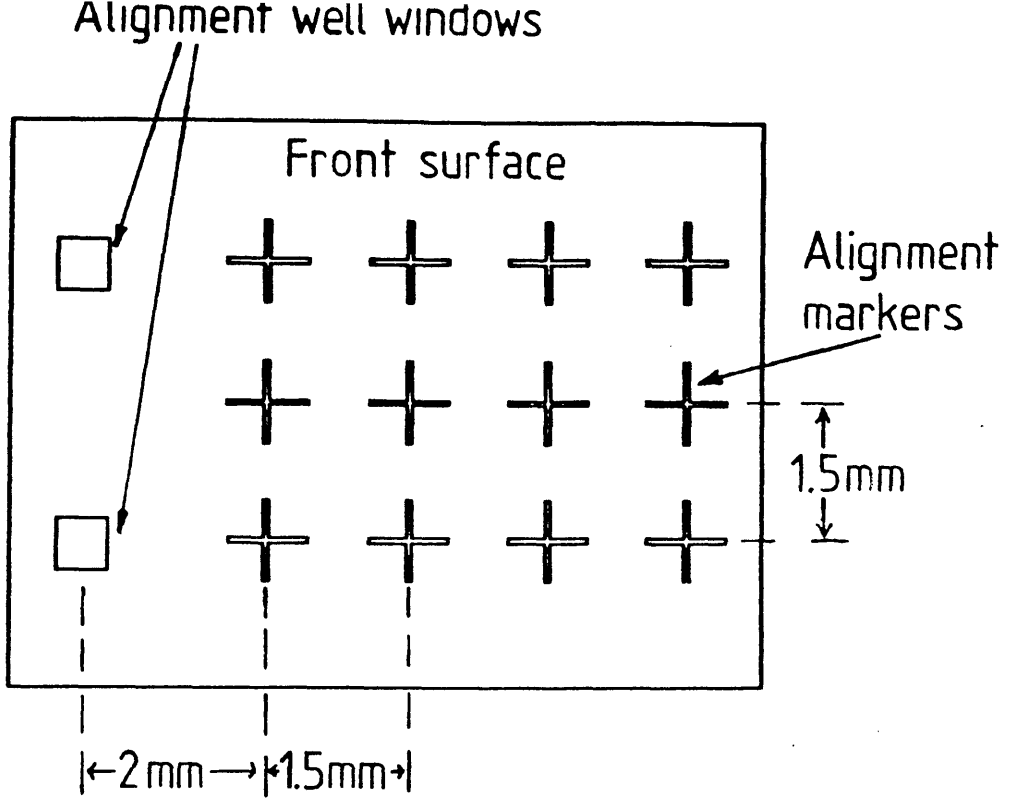


Fig 6.2 The test pattern used in the back to front alignment experiments. The two square windows are for etching the alignment wells and the crosses are the alignment marks.

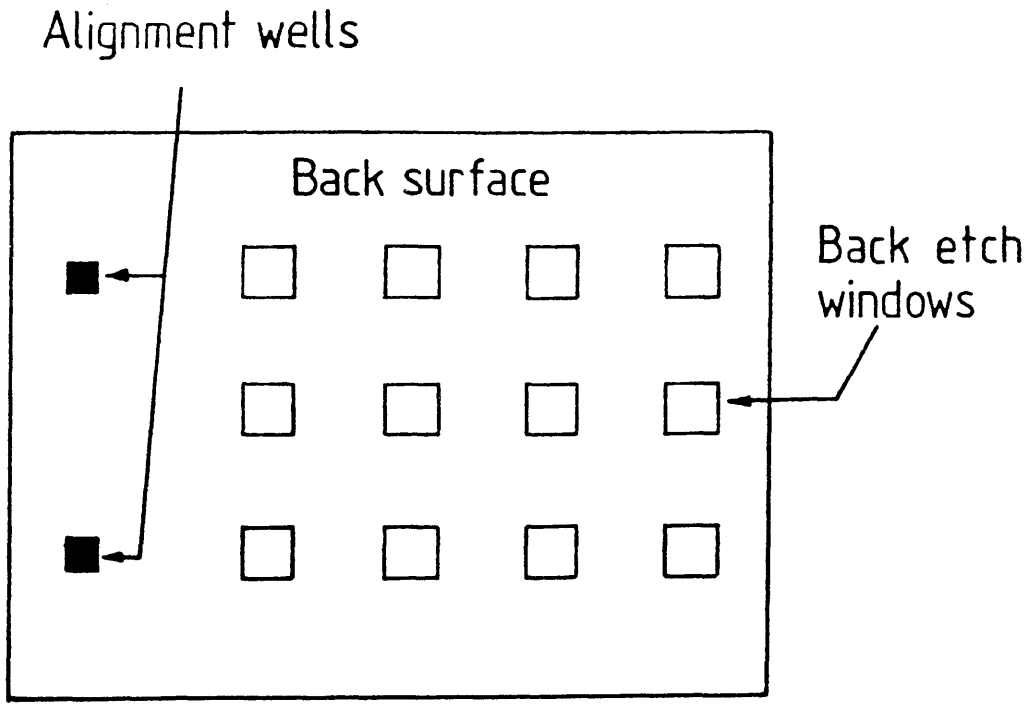


Fig. 6.3 The back etched wells were positioned relative to the two alignment wells, so that their position corresponds to the markers on the front of the wafer.

wafer. The resist was spun for more than 30 seconds at 4000 rpm to ensure that a uniform film was obtained. After spinning the wafer was baked at 80 ^{o}C for 20 minutes. A layer of resist also had to be applied to protect the back surface of the wafer during etching of the alignment wells. Spin coating could not be used because placing the sample resist side down on the vacuum chuck used for spinning, would have resulted in damage to the previously applied resist layer. Therefore, the resist was "painted" onto the back of the wafer using a small soft haired brush. The sample was then baked for a further 20 minutes.

The alignment test pattern was exposed with a dose of 85 $\mu C/cm^2$ using a 250 nm diameter electron beam and then developed for 60 seconds in neat AZ developer. After development the resist was baked for at least 30 minutes at 180 ^{o}C. This post development bake was to harden the resist making it completely insoluble in organic solvents and in the the silicon nitride etch which follows.

6.3.3 Silicon Nitride Etch

The silicon nitride layer was etched in boiling phosphoric acid using the patterned resist as a mask [6.8]. The concentration of the acid (originally 85 %) was altered by adding water until the boiling temperature was 146 ^{o}C. At this temperature the etch rate of the nitride was about 3.4 nm/min. The etching was carried out in a flask fitted with a reflux condenser which kept the concentration of the acid and hence the boiling temperature constant. The wafers were etched for about 20 minutes to ensure that all of the nitride was removed. After etching the wafers were rinsed in deionised water.

6.3.4 Silicon Etch

Wells were then etched through the silicon, using the nitride layer with the etched windows as a mask [6.8]. The silicon etch was boiling sodium hydroxide solution, with the concentration adjusted to give a boiling temperature of 121 ^{o}C (around 33 % by weight) at which the etch rate was about 10 μm/min. The sodium hydroxide solution etches the silicon (100)

planes about 7 times faster than the (111) planes, so the resulting etched pits are pyramidal with side walls almost parallel to the (111) planes. The samples were etched initially for 30 minutes, then at intervals of 2 minutes until the silicon had been etched through to the nitride layer on the back (rough) surface. The samples were inspected after each etch by holding them up to the light to see if the etched wells were visible through the nitride film on the back surface of the wafers. When etching was completed the samples were rinsed in deionised water and blown dry. In this particular experiment it was the positions of the etched wells which were important and not the formation of nitride membranes.

After the sodium hydroxide etch, the samples were cleaned in a mixture of concentrated sulphuric acid and hydrogen peroxide. The approximate ratio of acid to peroxide was about 20:7. This post etch clean was to remove any residual resist from the samples although most of the resist had already been removed during the sodium hydroxide etch. The samples were immersed in the cleaning solution for about 10 minutes and then rinsed in deionised water and blown dry.

6.3.5 Resist Coating For Back Etched Wells

After cleaning AZ 1350J resist was again coated on both sides of the wafer only this time the resist was spin coated on to the back surface and "painted" on the front surface. After each resist application the samples were baked for 20 minutes at 80 ^{o}C.

6.3.6 Alignment

The pattern for the back etched wells is shown in fig. 6.3 There are 12 square windows (620 μm) corresponding to the 12 markers on the front of the wafer. The alignment of the back etched wells to the markers is as follows:-

The samples were placed in the SEM, with the rough side of the wafer towards the electron beam. After focussing on the specimen with a 250 nm diameter beam, which would be used for

exposing the well pattern, a lower beam spot size (32 nm) was selected and the first alignment well was located and positioned roughly in the centre of the microscope VDU screen. A small spot size was used in the location of the wells to minimise the exposure of the resist. Once the wells had been located, the beam diameter was set to 250 nm and the exact coordinates of the well were determined by continuously scanning the raster pattern (1.5 x 1.2 mm frame size) shown in fig. 6.4. over the well. The sample was moved using the stage x and y shifts (and rotation) until the well was positioned centrally within the raster. The x and y coordinates were recorded. The second well was located, again at a small spot size, and the x and y coordinates determined using the scanned raster as before only no adjustments were made to the stage rotation for the second well.

The windows for the back etch wells were exposed using the POSITION program to calculate the exposure sites relative to the two alignment wells. The square window patterns were exposed with a frame size of 1.5 x 1.2 mm and a beam diameter of 250 nm. The resist was developed in neat AZ developer and then given a post development bake at 180 ^{o}C to harden the resist.

Using the same techniques as before windows were etched through the nitride layer. Then the silicon was etched using the patterned nitride layer as a mask. Etching was stopped in this case when the back etched wells reached the marker wells etched from the front of the wafer.

6.3.7 Results

Fig. 6.5a) is an SEM micrograph of a processed sample, viewing from the back of the wafer. It can be seen that the alignment markers (the small squares within the wells) are almost concentric with the back etched wells over the entire wafer. At a higher magnification (fig 6.5b) it can be seen that there is only a slight offset between back etched wells and the markers. When the offset was measured it was found that in the y direction (even in the worse case) the alignment was correct to less than 15 μm. In the x direction it was found that there was no measurable offset, at the magnification used for measurement

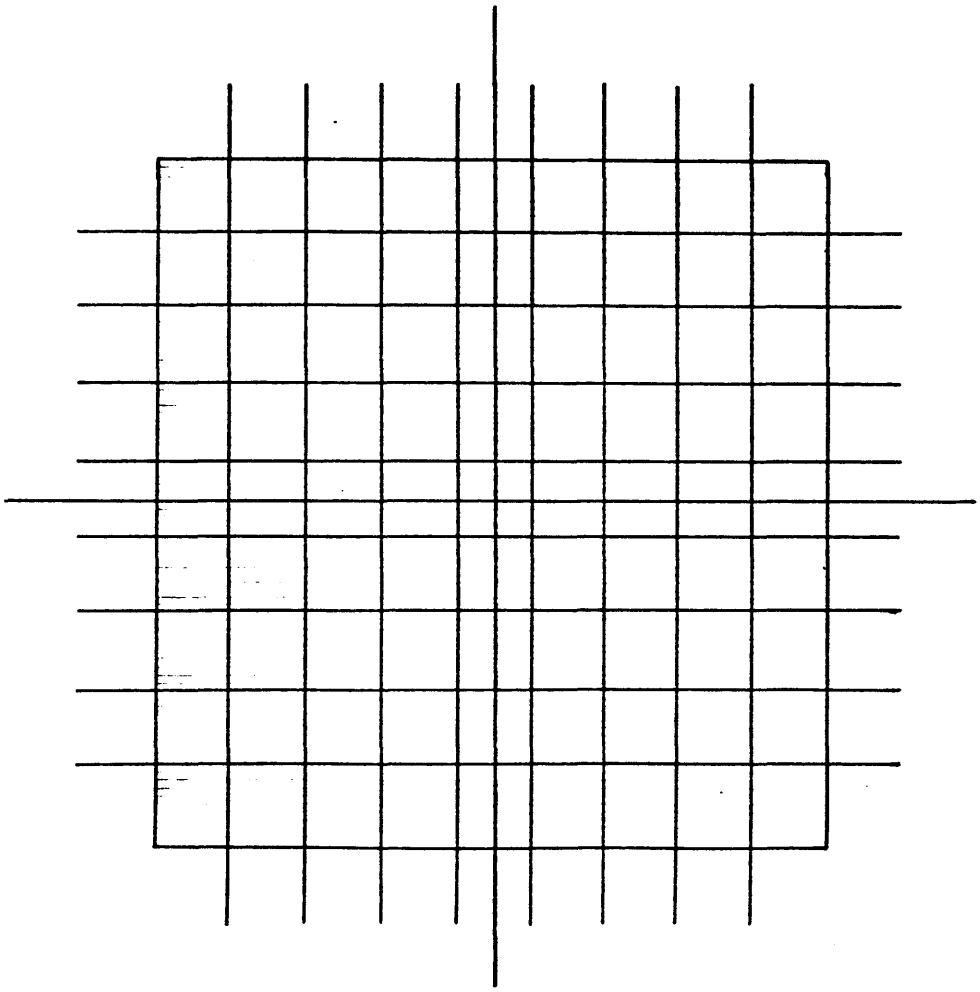


Fig. 6.4 Schematic of the raster pattern used for locating the alignment wells. The central region consists of a single pixel grating with 10 pixel pitch and the marker lines are symetrically positioned about the centre of this grating.

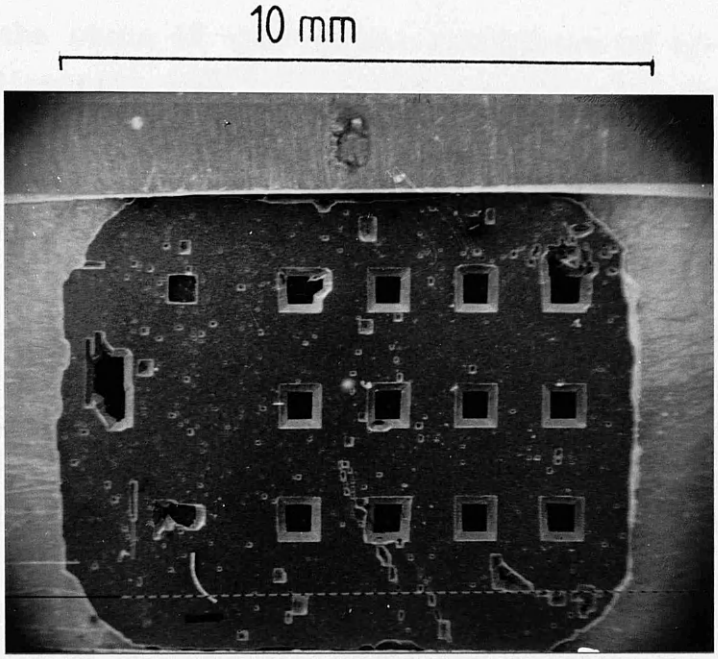


Fig. 6.5a) SEM micrograph of a test chip observed from the back surface of the wafer. The marker wells can be seen at the centre of each back-etched well.

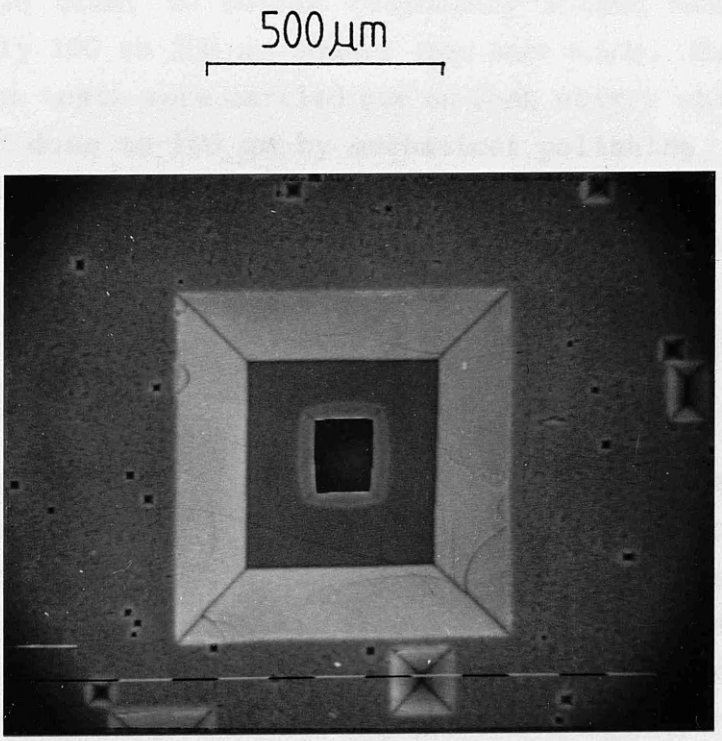


Fig. 6.5b) SEM micrograph of one of the back etched wells. The back-etched well is almost concentric with the marker well etched from the front of the wafer.

(X80), over the whole of the sample. Alignment of +/- 20 μm in either direction would be acceptable for the eventual fabrication of GaAs membrane devices.

6.4 Back To Front Alignment on GaAs Wafers

The principal of the back to front alignment procedure described in the previous section was applied to GaAs wafers, which were to be used in the fabrication of membrane devices. Various alterations were made to the alignment process because of the different nature of the GaAs etches. The principal changes were:-

- The patterning of gold markers instead of etched pits.

- Waxing the wafers to glass slides during etching to prevent uneccessary handling difficulties

- The use of PMMA as an etching mask.

6.4.1 Procedure

GaAs membranes have to be fabricated on thin (100 μm) substrates in order to obtain reasonably shaped membranes approximately 100 to 200 μm square (see sect 6.5.1). Therefore the alignment tests were carried out on GaAs wafers which had been thinned down to 100 μm by mechanical polishing. After thinning, the crystal directions were determined using the scratched cross technique described in sect. 6.5.3. It should be noted that if the [011] direction on the front surface of the wafer turned out to be horizontal say, the [01$\bar{1}$] direction on the back of the wafer would be vertical.

The alignment test pattern was basically the same as that used in the test described previously. However, the windows for the alignment wells were now 200 x 20 μm strips aligned parallel to the [011] crystal direction (the same as was used in membrane fabrication) and the marker crosses were replaced by dashed lines as shown in fig. 6.6.

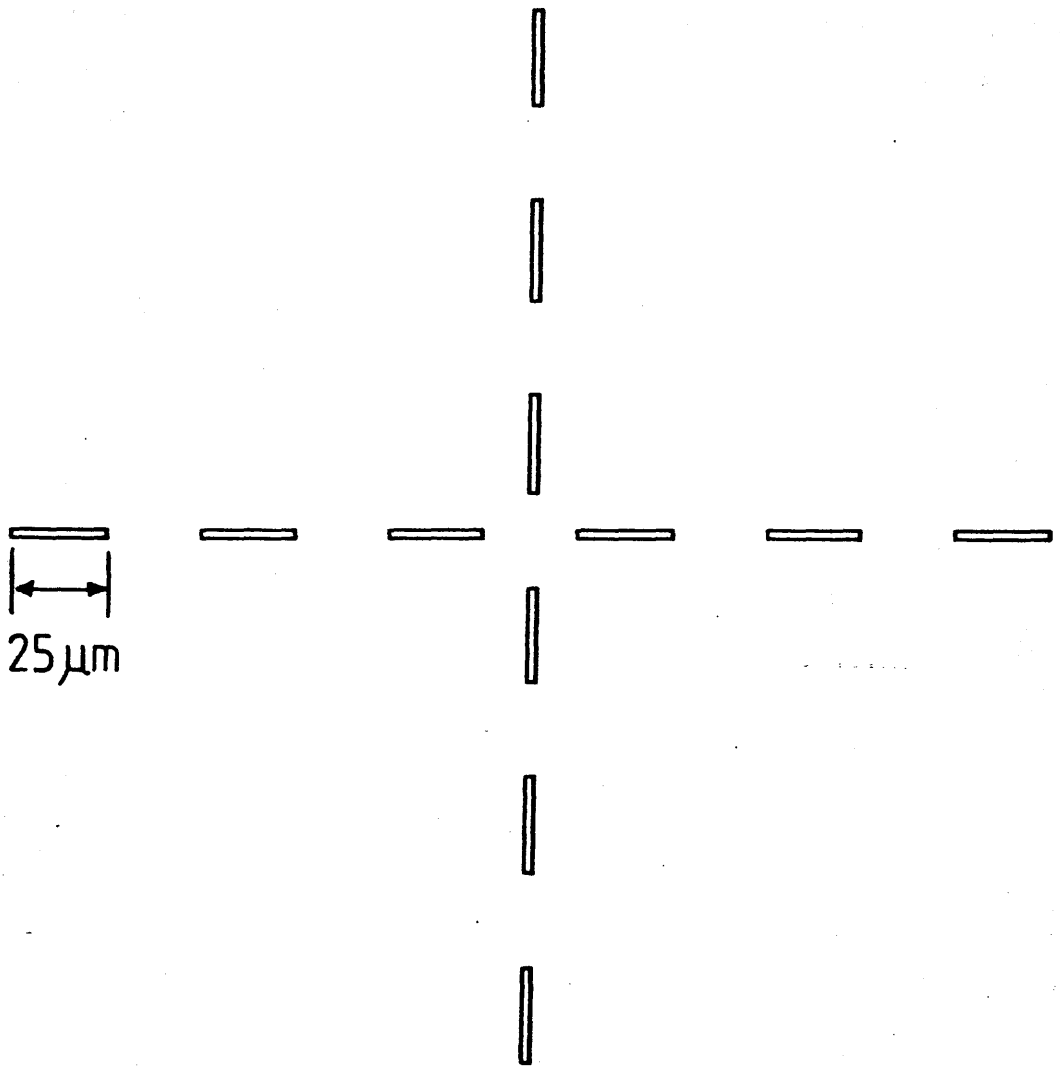


Fig. 6.6 Detailed view of one of the marker crosses used in the alignment test on GaAs wafers.

6.4.2 Alignment Pattern

The GaAs wafers were scribed and broken into 8 x 6 mm samples which were cleaned in trichloroethylene, acetone and then methanol. PMMA was spin coated on to the surface of the wafer at 4000 rpm for 1 minute and then baked overnight. The resist thickness was about 1 μm. The long bake was essential to ensure the resist adhered to the wafer during etching (Sect. 1.4.2).

The alignment pattern was exposed by e-beam using a 250 nm diameter beam. When the samples had been exposed they were waxed on to glass microscope cover slips using white wax. Not only was this useful for handling the fragile wafers, it meant that the back surface of the wafer did not need to be protected by resist during etching. The alignment pattern was developed in 1:1 MIBK:IPA (23 ^{o}C) for 60 seconds. When the pattern had been developed the wafers were metallised using a thin strip of aluminium foil to shield the alignment well windows from the metal evaporation source (fig. 6.7). The markers were metallised with 50 nm Au using a thin nichrome layer to promote adhesion to the GaAs. At this stage the pattern was not lifted-off, otherwise the windows for the alignment marks would have disappeared when the resist was dissolved. Instead, some white wax was melted over the part of the wafer covered in gold, to protect the markers during etching.

6.4.3 Alignment wells

The alignment wells were etched using 1:8:1 H_2SO_4:H_2O_2:H_2O. The samples were etched, initially for 5 minutes and then in 1 minute intervals until the wafer had been etched all the way through. When etching was complete the wells were clearly visible from the back of the wafer (through the cover slip and wax) when the sample was held up to the light.

At this stage the sample was immersed in trichloroethylene (trich) for about 2 minutes. This was long enough to dissolve the wax over the gold which had been evaporated onto the sample but not sufficiently long to dissolve the wax holding the sample

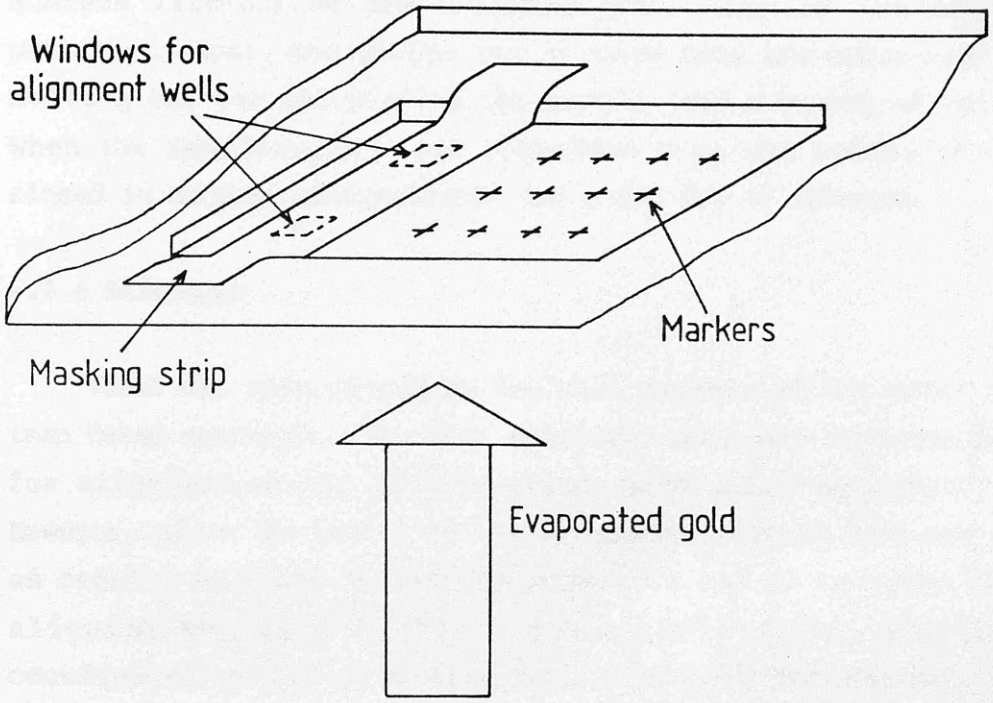


Fig. 6.7 Schematic showing how the alignment well windows are protected during the gold marker evaporation. Subsequently, the metallised part of the wafer is protected with white wax during the etching of the alignment wells.

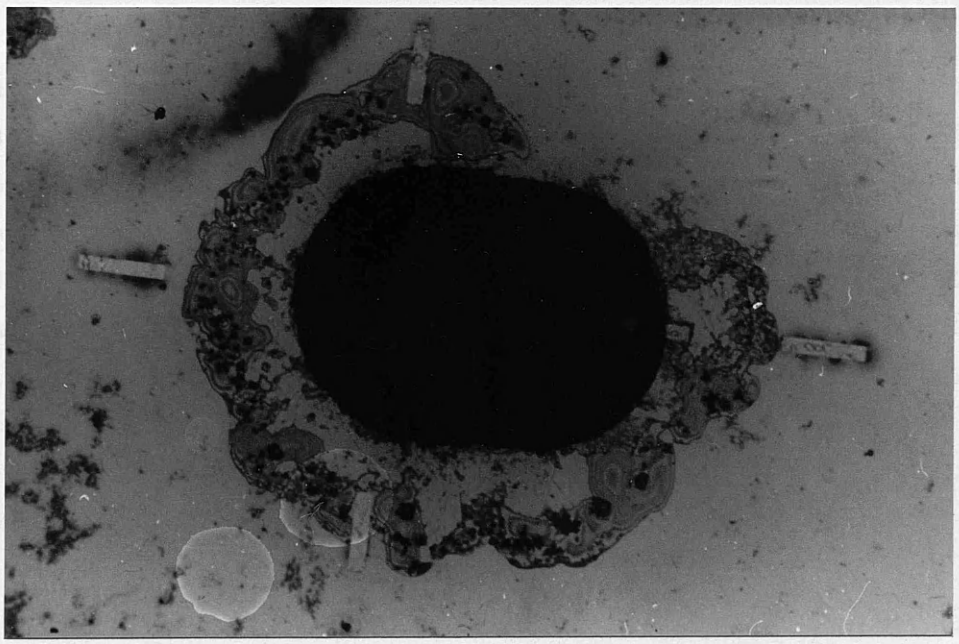


Fig. 6.8 Optical micrograph showing the position of a back-etched well relative to the gold marker pattern. The well is within the 20 um limit which was thought to be adequate for device fabriacation.

to the cover slip. The sample was removed from the trich and placed in a beaker of acetone to dissolve the PMMA and hence achieve lift-off of the unwanted gold, leaving the marker patterns. Next, the sample was removed from the cover slip by melting the wax and sliding the sample into a beaker of trich. When the remaining wax was dissolved from the wafer, it was rinsed in acetone then methanol and blown dry in nitrogen.

6.4.4 Alignment

PMMA was spin coated on the back surface of the wafer and then baked overnight. The same alignment procedure that was used for alignment on the silicon wafer (sect 6.3.6) was employed. However, since the bottom of the alignment wells in GaAs are not as regular as those in silicon more care had to be taken when aligning the well within the scanned raster. When the coordinates of the alignment wells had been determined, the windows for the back etched wells were exposed. The wafers were etched using the 1:8:1 etch as before, until the wells had gone all the way through to the wax. The samples were removed from the wax, cleaned as before and then observed under an optical microscope.

6.4.5 Results

It was found that the alignment of the back etched wells to the markers was not as good as had been obtained on the silicon wafers. An optical micrograph showing the typical location of a back etched well relative to the gold marker pattern is shown in fig 6.8. On average the x and y displacements were about 10 and 20 μm repectively. The reason for this can be attributed to the problems associated with determining the exact coordinates of the alignment wells. However, the errors were still within the acceptable limits for the fabrication of membrane devices.

6.5 GaAs Membrane Fabrication

6.5.1 Introduction

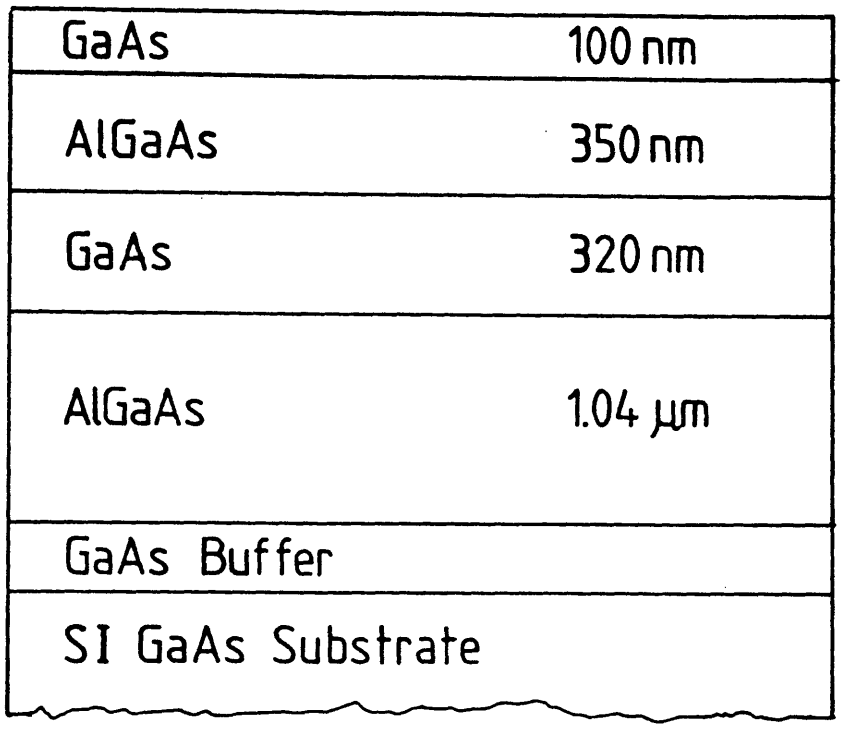
GaAs membranes were fabricated using a slightly modified

version of the process developed in the department by WS Mackie [6.1,6.2]. A schematic diagram of the material requirements for producing membranes is shown in fig. 6.9a). The alternate GaAs/AlGaAs (60% Al) layers were used as etch stop layers during the membrane fabrication. To produce the membranes, a well was etched from the back of the wafer to within 10 μm of the etch stop layers using a fast, non-selective etch. Then the remaining layers were removed using selective etches which either etched GaAs and not AlGaAs or vice-versa until only the top GaAs layer remained fig.6.9b).

The previous work done in the department by, WS Mackie, had shown that the properties of the first non-selective etch determines the shape of the final membrane. It was shown that a 20 x 200 μm etch window patterned on the back of the wafer, with the long axis parallel to the [011] crystal direction, resulted in a membrane with edges between 100 and 200 μm. Because of the rounding of the etch profile in the [011] direction it was also shown that the wafer thickness has to be between 100 and 120μm to prevent the membranes from becoming too large an so very fragile.

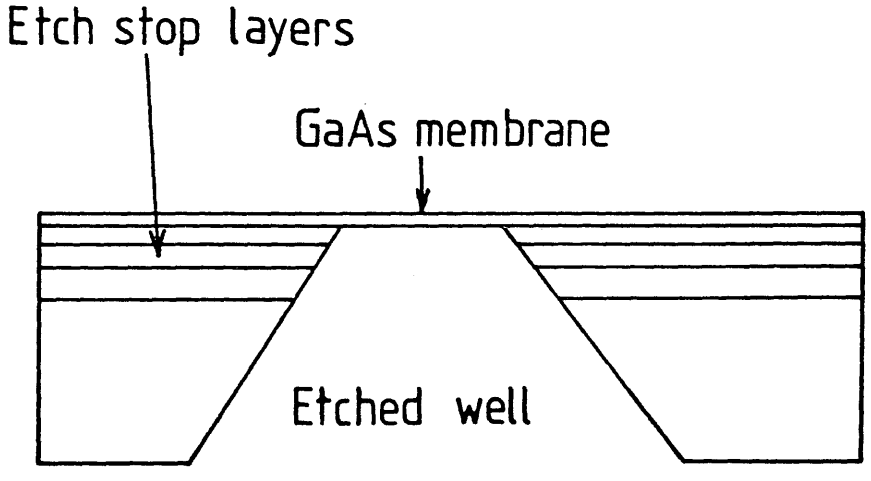
6.5.2 Material

The membrane material shown in fig 6.8a) was grown by Metal Organic Vapour Deposition (MOCVD) at Plessey Research (Caswell) Ltd. The thickness of the received wafer was about 450 μm so the first step towards producing membranes was to have the wafer thinned down to 100 um. The wafers were polished down to roughly 200 μm using coarse Aloxite 800 grit and then down to the desired 100 μm with 0.3 μm alumina [6.9]. It was easier to thin down the entire wafer (about 4 square centimeters) and then break it into individual chips (5 mm^2) than to break the sample into smaller pieces and then do the polishing. Therefore, the entire membrane stock existed as 100 μm thick wafers and had to be processed as such which meant that there were some handling difficulties with the fragile wafers.



a)

Fig 6.9a) Schematic of the material layers used for GaAs membrane fabrication. The layer thicknesses were determined from Talistep measurements of the selectively etched layers. The aluminium concentration in the AlGaAs layers was nominally 60 %.



b)

Fig. 6.9b) The membrane is formed by etching a well from the back of the wafer, then selectively etching the alternate AlGaAs and GaAs layers until only the top GaAs layer is left.

6.5.3 Crystal Orientation

Before the whole wafer was divided into individual chips the orientation of the GaAs crystal had to be determined to ensure that the etch windows would be patterned in the correct orientation. This was done by removing a small piece of the wafer and melting some white wax on to the back surface (the side from which the wells would be etched). A cross was then scratched through the wax using the point of a pair of tweezers The wafer was then immersed in the fast GaAs etch (1:8:1) given below. After etching for about 5 minutes the sample was removed from the etch, the wax was dissolved in trichloroethylene and the resulting etched cross observed under an optical microscope. In one direction the bottom of the etched groove would appear rounded. The direction of this groove corresponds to the [011] direction of the crystal. In the other direction [01$\bar{1}$] the bottom of the groove would be flat and an abrupt edge between the bottom of the groove and the wells of the groove would seen.

6.5.4.Masking System

The bottom surface of the wafers have to be protected with a mask which will be resistant to all of the etches used during membrane fabrication. Previously the mask was a gold layer patterned by lift-off, covered with a layer of Shipley AZ 1350J photoresist. However, another suitable masking system was found again using gold but this time PMMA was used instead of photoresist. A 40 nm layer of gold was thermally evaporated on to the back of the wafers using the standard thin layer of nichrome to enhance its adhesion with the GaAs. Then a thick layer (1 μm) of PMMA (15% in chlorobenzene) was spin coated, on to the gold and baked overnight at 180 ^{o}C. The 20 x 200 μm windows for etching the wells were exposed using a 250 nm electron beam and then developed in 1:1 MIBK:IPA. This opened up windows in the PMMA but, at this stage, the gold layer below the resist was still complete. In order to open a window through the gold layer, using the patterned PMMA as a mask, the uncovered gold was removed by etching in an argon plasma. However, since this step required a dry etching system and was therefore quite lengthy, this method of removing the gold was abandoned in favour

of chemical etching. It was found [6.10] that a 15 s etch in $KI:I_2$ was sufficient to remove the gold layer without any significant undercutting of the PMMA mask.

6.5.5 Etching

The etches used in the process are as follows.

1:8:1 $H_2SO_4:H_2O_2:H_2O$ - a nonselective anisotropic etch which etches GaAs at about 15 μm/min when the etch is freshly made up, decreasing to less than 10 μm/min as the etch solution cools [6.11].

95:5 $H_2O_2:NH_4OH$ - etches GaAs at a rate of approximately 2 μm/min but the etch rate of $Al_xGa_{1-x}As$ decreases exponentially with Al concentration and for x greater than 0.3 the etch rate is negligible [6.12, 6.13].

20% HF - etches $Al_xGa_{1-x}As$ at a reasonable rate for for x greater than 0.5 but not GaAs. The etch rate increases exponentially with Al concentration and for x=0.6 is about 0.8 μm/min [6.13, 6.14].

These are the etch solutions which were used in previous membrane experiments in the department which were carried out on MOCVD grown material from the SERC III/V growth facility at Sheffield University. However, it was found that on the Plessey MOCVD material, the selective etches had to be modified before reliable membranes could be produced. The differences were probably due to different aluminium concentrations in the different wafers. Using the material supplied by Plessey, it was found 38:3 $H_2O_2:NH_4OH$ and 50% HF were the best solutions to use.

6.5.6 Membrane fabrication

The size of the chips used for membrane fabrication were typically about 5 x 4 mm. 200 x 20 μm etch windows were patterned on the back of the wafers using the masking system described above. The long axis of the windows were patterned parallel to the [011] crystal direction. Two windows were

patterned in each exposure frame (1.5 x 1.2 mm) so each chip would have potentially up to 18 membranes.

After the electron beam exposure of the PMMA, the samples were waxed on to glass microscope cover slips to protect the side of the wafer where the membranes were eventually to be fabricated. Then the PMMA was developed and the underlying gold layer etched to produce the etch masks described previously. Before commencing the GaAs etching, the chips were immersed in IPA to wet the PMMA resist, rinsed in deionised water and then transferred immediately to the first etch solution.

When a sample had been etched for 5 minutes in the 1:8:1 etch, it was removed,rinsed in deionised water and blown dry. The depth of the etched wells were then measured using an optical microscope. By focusing first on the well bottom and then on the gold layer on the surface, the etched depth could be determined from the change in height of the microscope stage. Typically the well depths would be around 50 um after the first 5 minute etch. Before resuming with the etching, the overhanging part of the Au/PMMA mask (fig 6.10) was broken by immersing the sample, upside down in a beaker of IPA, in an ultra-sonic bath. This was to ensure that during further etching, the etch solution was not prevented from going into the etched wells by trapped air bubbles. Removing the overhang also facilitated the measurement of the well depths. Subsequent etches were for 2 minutes or less, until the depth of the etched wells was about 90 μm (10 μm from the etch-stop layers). Once again the overhanging mask material was removed as before.

At this stage the wafer was scribed into individual chips, 1.5 mm square, each containing 1 or 2 etched wells. The wafer was removed from the cover slip by melting the wax, and carefully lifting the sample with tweezers, ensuring that no wax got onto the masked side of the wafer. The wafers often broke up into individual chips as they were removed from the cover slips because the substrates were so thin. The individual chips were then waxed on plastic strips for further etching. These strips were resistant to the HF etches which follow.

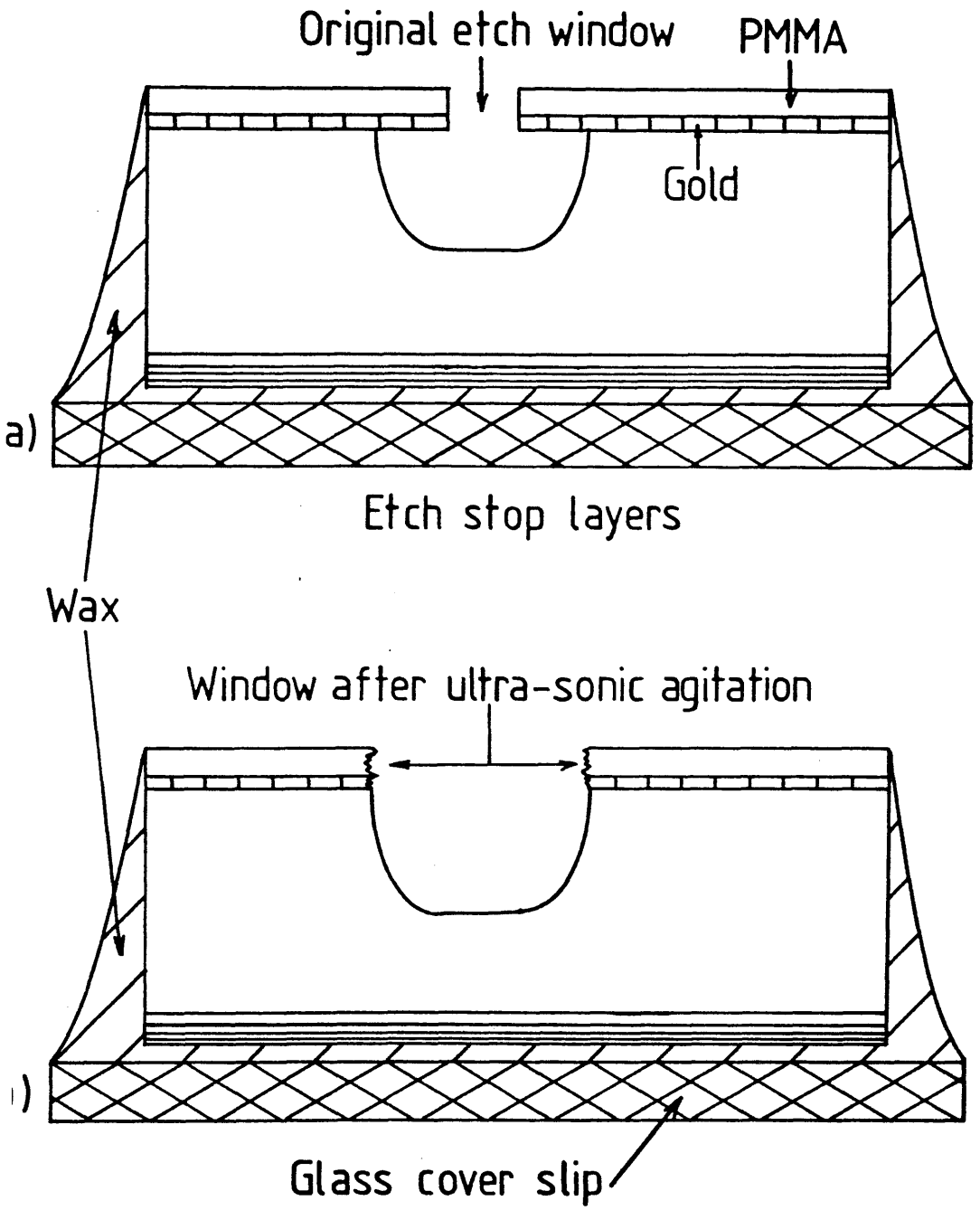


Fig. 6.10 The overhang caused by the undercutting of the GaAs etch needs to be removed to allow the etch solutions to flow into the partially etched wells. This is achieved by placing the wafer in an ultrasonic bath for a few seconds.

The first selective etch was the 95:5 etch. Each chip was etched initially for 5 minutes and then in 1 minute intervals until the well bottom appeared flat. This happens when all the GaAs has been removed and the first AlGaAs layer has been reached. Unfortunately, as mentioned earlier, the 95:5 solution did not produce the best results on the Plessey material; it was found that when the etch stopped on the GaAs/AlGaAs interface, the AlGaAs surface, instead of being clean and mirror like, was brown in colour. It was then virtually impossible to etch the following AlGaAs layer, even when 50% HF was used.

The reasons for the brown colour at the surface of the first etch stop layer was speculated to be that the interface between the GaAs and the AlGaAs was not as abrupt as in the Sheffield MOCVD material used previously. Therefore, the 95:5 etch would see a region of AlGaAs with low aluminium concentration and the etch rate would consequently slow down but not stop entirely. The brown colour could be a result of oxidation of the interface layer by the GaAs etch.

The problem was solved by using a peroxide / ammonia etch with a higher ammonia concentration. It was found that 38:3 solution gave cleaner surfaces at the interface, although the surface was still not perfectly mirror like. However, it was found that the following AlGaAs layer could be etched uniformly in HF when the 38:3 solution was used to etch the GaAs layer. It was also found that mirror like surfaces could be obtained when, after each 38:8 etch, the sample was placed in 30% HCl for a few seconds. This presumably removed the oxide which had been formed during the GaAs etch. The HCl etch between the GaAs and AlGaAs etches was employed as standard procedure for membrane fabrication.

The AlGaAs layers were etched in 50% HF since the etch rate using the previously used 20% HF was too slow. This indicated that Al concentration of the supplied material, instead of being the specified 60 %, was in fact significantly lower. From the etch rate of the 1 μm AlGaAs layer it was determined from avilable data [6.13], that the aluminium concentration must have been nearer 50 %.

The etch times for each of the etch stop layers is summarised below:-

Final 10 um of GaAs - 5 to 8 minutes in 38:3 solution.
1st AlGaAs layer - 2 1/4 min in 40% HF.
1st GaAs layer - 45 sec in 38:3. (Then 5 seconds HCl).
2nd AlGaAs layer - 30 sec in 50% HF.

The alternate GaAs/AlGaAs layers were etched until only the top GaAs layer remained. Then the samples had to be removed from the plastic strips. This could not be done by melting the wax and lifting the sample from the strip as the membranes were too delicate and would not survive such harsh treatment. Therefore, each sample was placed face down in trichloroethylene about 4 mm deep, which was sufficient to ensure that the plastic strips floated in the trich. When all the wax had been dissolved by the trich, the samples dropped to the bottom of the petri dish, membrane side upwards. They could then be transferred to an acteone bath for cleaning. After a few minutes the chips were removed from the acetone, briefly rised in methanol, then carefully blown dry in a gentle stream of nitrogen.

6.5.7 Yield

The success rate for removing the membranes from the plastic strips was probably about 60%. However, when it came to actually trying to fabricate devices on membranes it was found that the yield was improved when contacts were patterned on to the area of the membrane before fabricating the membrane (sect 6.8.6).

6.6 Lithography On GaAs Membranes

6.6.1 Introduction

Until now the only lithography which had been done on thin GaAs membranes was the high resolution work involving the patterning of thin metallic (usually AuPd) lines. In order to fabricate devices on a membrane however, completely new litographic processes had to be tested. For example, the ohmic source-drain contact pads need to be thicker than the metallic

patterns patterned previously. Therefore, thicker resist has to be spun over the membranes in order to achieve reliable lift-off. When the contacts are patterned, the contacts need to be annealed at at least 300 ^{o}C. It was not known what effect this would have on the membranes.

In the following sections it will be shown that the membranes could stand up to both thick contact metallisations and high temperature annealing. In fact, the membranes could stand up to the repeated resist spinning, metallisation and lift-off steps which would be required for the fabrication of an actual device.

6.6.2 Ohmic Contact Metallisation

In an actual device, it was likely that coarse source-drain contact patterns would be patterned on the active side of the wafer before fabricating the membranes themselves. Then once the membrane had been produced closely spaced source-drain contacts would be patterned on the membrane. However, to test the viability of patterning thick metallic layers on a membrane a psuedo device pattern was created on membranes fabricated as described above. No working devices could have been produced on this particular sample because no isolated regions had been defined on the membrane beforehand (see sect 6.8.3).

Sample Holder

The first step was to take a 1.5 mm membrane chip, with either one or two complete membranes, and mount it in a holder designed for handling these chips (fig 6.11). A thin layer of polyimide (10 % in 35:65 acetophenone:xylene) was applied to the recessed part of the holder using a piece of filter paper. This was to act as a glue for holding the chip into the holder. Polyimide was chosen because, when it is cured at 180 ^{o}C it is not readily dissolved in acetone. Therefore, even when the sample is immersed in acetone for several minutes to achieve lift-off, the membrane chip will stay in the holder. The holder was placed on a hot plate (100 ^{o}C), once the chip was inserted, to drive off most of the solvent from the polyimide.

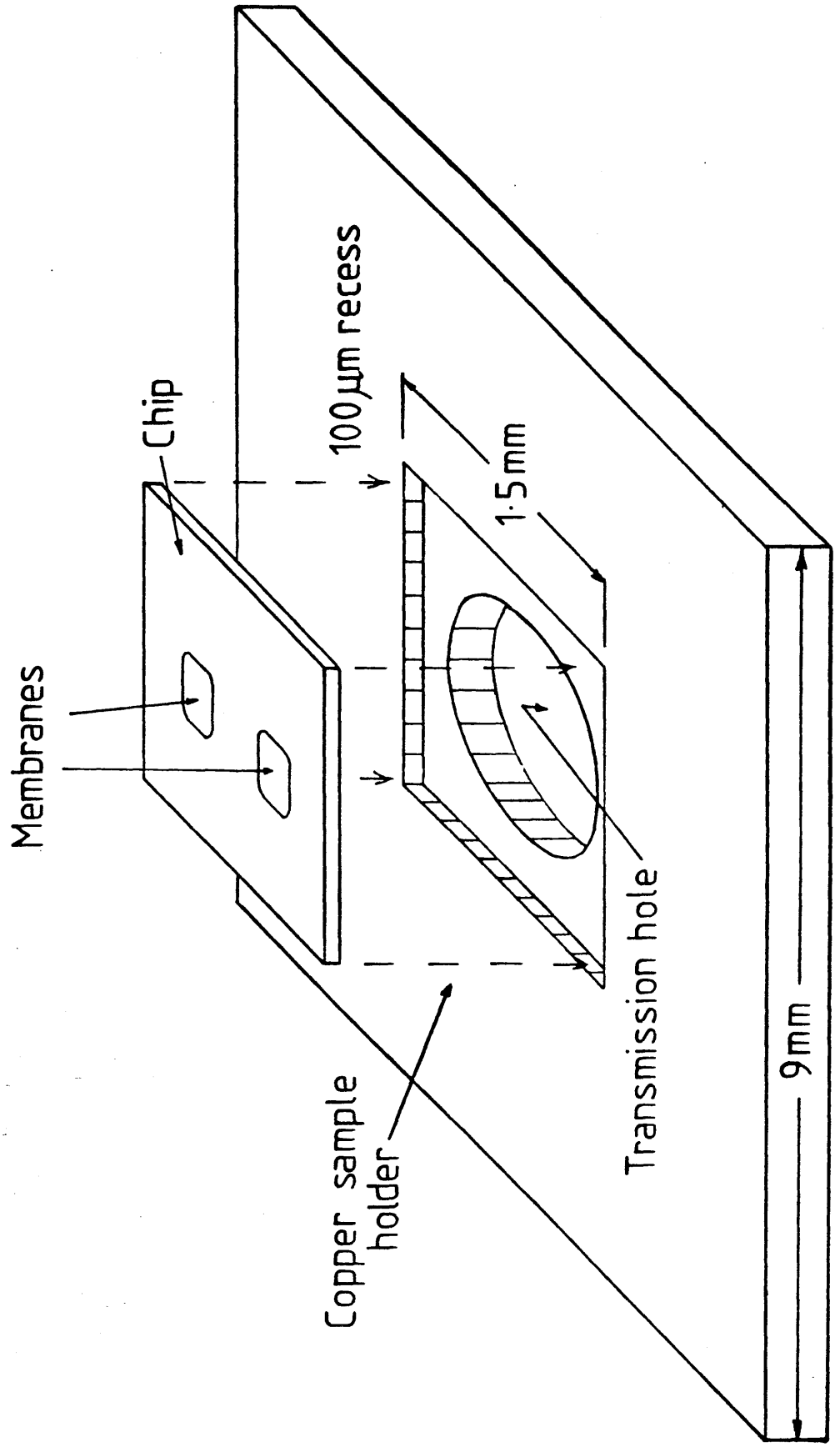


Fig. 6.11 Copper membrane chip holder with a 100 um recess and a 1mm diameter hole which allows the membranes to be examined in transmission mode.

Resist Spinning and Metallisation

A thick layer (1 μm) of low molecular weight PMMA (15% in chlorobenzene) was applied to the membrane using a spinner speed of 5000 rpm. The resist was baked for 2 hours at 180 ^{o}C. After baking, the pattern shown in fig. 6.12 was exposed using a frame size of approximately 0.4 x 0.3 mm and a beam diameter of 0.125 μm. The dose for the thin contacts to the membrane was 450 μC/cm^2 and for the pads 250 μC/cm^2. The resist was developed in 1:1 MIBK:IPA solution (23 ^{o}C) for 60 seconds. After development, the ohmic contacts were metallised with the AuGe/Ni/Au system described in chapter 2. The composition for the contacts was chosen so that low temperature annealing (325^{o}C) could be used for forming low resistivity contacts. The total contact thickness was 0.1 μm. After metallisation the sample was immersed in a beaker of acetone for 10 minutes to achieve lift-off of the unwanted metal.

Fig 6.13 is an SEM micrograph of the metallised membrane taken in transmission mode. The minimum gap between contacts which was obtained was 0.2 μm. This had been achieved without any exposure tests or optimisation procedures being carried out beforehand; the exposure dose was taken to be x1.5 of that of a similar pattern on solid substrates. This illustrates the potential of fabricating closely spaced devices on membranes although it should be remembered that the diffusion length of the Ge from the contacts is about 0.2 μm (Chap 3) when annealed on membranes at 300 ^{o}C.

6.6.3 Contact Annealing

It was possible to deposit thick metallic patterns on to a membrane, but what happens when the contacts are subsequently annealed? It was shown in the x-ray microanalysis experiments that membranes could withstand anneal temperatures up to 400^{o}C (sect 3.3.9). However, the edge definition of the contacts deteriorated with increased anneal temperature. Therefore, to maintain good pattern definition for gate alignment purposes, and to reduce the lateral spreading of the contact material, low temperature annealing (300-320 ^{o}C) was chosen for thin substrate

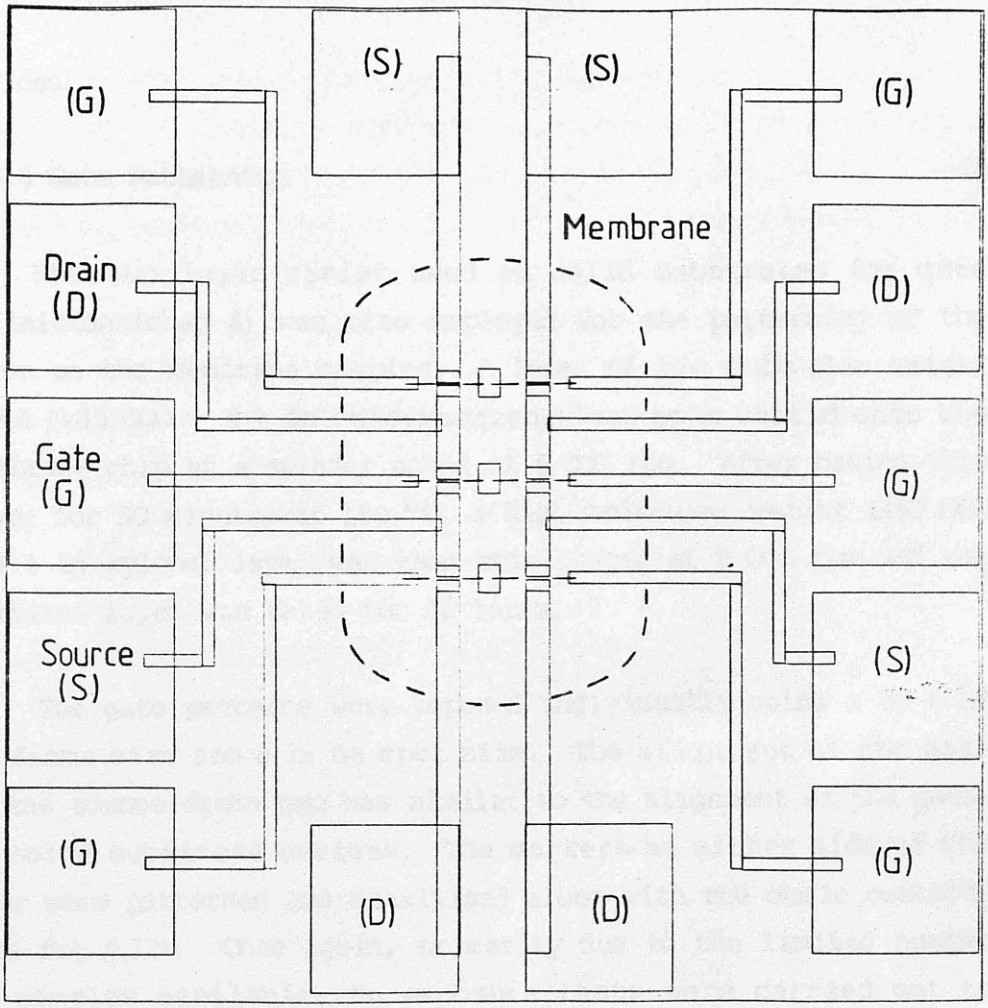


Fig. 6.12 The membrane device pattern (exposed directly onto the membrane). The distances between contacts on the membrane varies from 0.2 um up to 1 um.

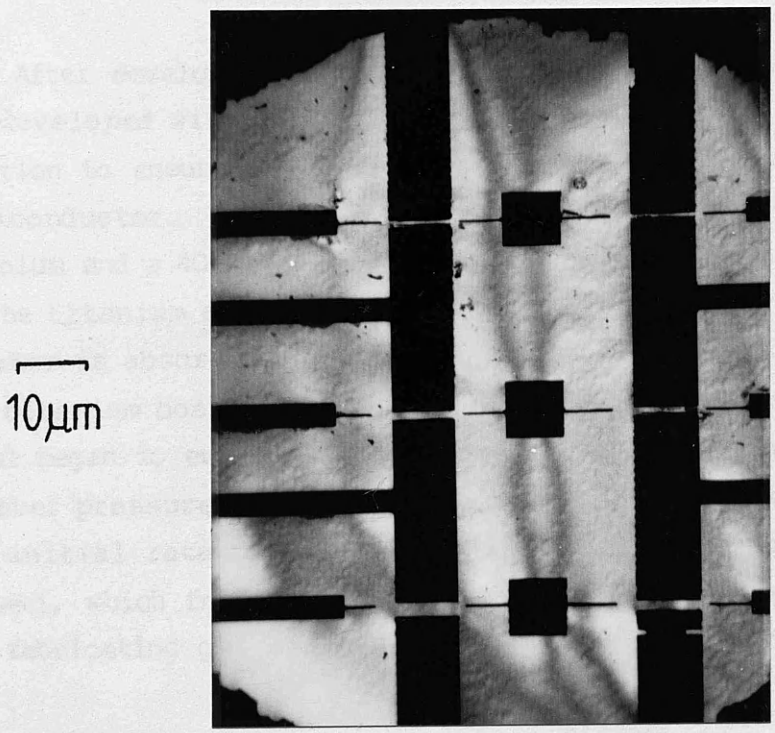


Fig. 6.13 SEM micrograph of a metallised membrane device.

devices.

6.6.4 Gate Patterning

The two layer resist used on solid substrates for gate definition (chap 4) was also employed for the patterning of the gates on the membrane samples. A layer of low molecular weight PMMA (185 000 - 4 % in chlorobenzene) was spin coated onto the membrane chip at a spinner speed of 6 000 rpm. After baking this layer for 30 minutes at 180 ^{o}C, a high molecular weight (350 000 - 4 % in xylene) layer was then spin coated at 8 000 rpm and the combined layer was baked for 12 hours.

The gate patterns were exposed individually using a 50 x 38 μm frame size and a 16 nm spot size. The alignment of the gate to the source-drain gap was similar to the alignment of the gates on solid substrate devices. The markers at either side of the gate were patterned and metallised along with the ohmic contacts (see fig 6.12). Once again, primarily due to the limited number of samples available, no exposure tests were carried out to determine optimum doses for narrow gate fabrication. Instead, the exposure dose required to fabricate gates on solid substrates was doubled to give an estimate of the required dose for thin substrates (3000 $\mu C/cm^2$ for a 1 pixel wide line). The two layer resist was developed for 40 seconds in 1:3 MIBK:IPA, at 23 ^{o}C.

After development, the surface of the GaAs exposed through the developed windows in the resist was cleaned in 5 % ammonia solution to ensure good adhesion between the gate metal and the semiconductor. The gate metallisation consisted of 30 nm of titanium and a 40 nm of aluminium. During the inital few seconds of the titanium evaporation, any residual oxygen in the vacuum chamber is absorbed by the evaporating metal. For this reason the titanium boat was shuttered for about 10 seconds after the metal began to evaporate (this was indicated by a sudden rise in chamber pressure). Shuttering the Ti filament also meant that the initial rate of evaporation was relatively high (about 3 nm/sec), which from previous experimental results was desireable for fabricating gates with good Schottky characteristics.

Following metallisation, the wafers were immersed in acetone for at least 10 minutes, to dissolve the PMMA and lift-off the unwanted metal. Lift-off was assisted by directing a stream of acetone, from the plastic acetone containers, at the wafer. The stream of acetone was angled at about 20 ^{o} to the plane of the wafer to avoid exerting unneccessary pressure on the fragile membranes. Using this technique it was possible to remove all of the unwanted metal from the membranes, leaving only the patterned Ti/Al gates.

Fig. 6.14 is an optical micrograph of the completed device. It was shown that the GaAs membranes could withstand: 4 resist spinning steps (2 spins for the two layer gate resist), 3 lift-off steps (1 failed) as well as an anneal of 300 ^{o}C. From this experiment, and from others on other membranes, it was clear that the possibilities of fabricating working devices was still fairly high. In fact once the membranes had been removed from the plastic strip (where the most fatalities occured), they were extremely robust. It was only careless handling and not routine processing which would damage the membranes.

6.7 Cracks Around Membranes

It was found that on some of the GaAs membrane samples fabricated, cracks appeared round the edges of the membranes after a few processing steps. These cracks appeared on the solid part of the wafer about 10 μm from the mesa edges. The origin of these cracks is not clear although it was established that only the top GaAs (membrane) layer is affected. This was discovered when a membrane which had been patterned with source-drain contacts (fig 6.12) was being tested. One of the probing pads was lifted from the surface of the GaAs when the probes were raised, taking with it part of the membrane and the GaAs active layer up to the crack. With the material from one side of the crack removed, observation of the sample under an optical microscope showed that the crack must have been confined to the top GaAs layer as the underlying layers were obviously still complete.

The origin of these cracks may be due to stress in the membranes, but, it is not clear why the cracks should appear 10μm

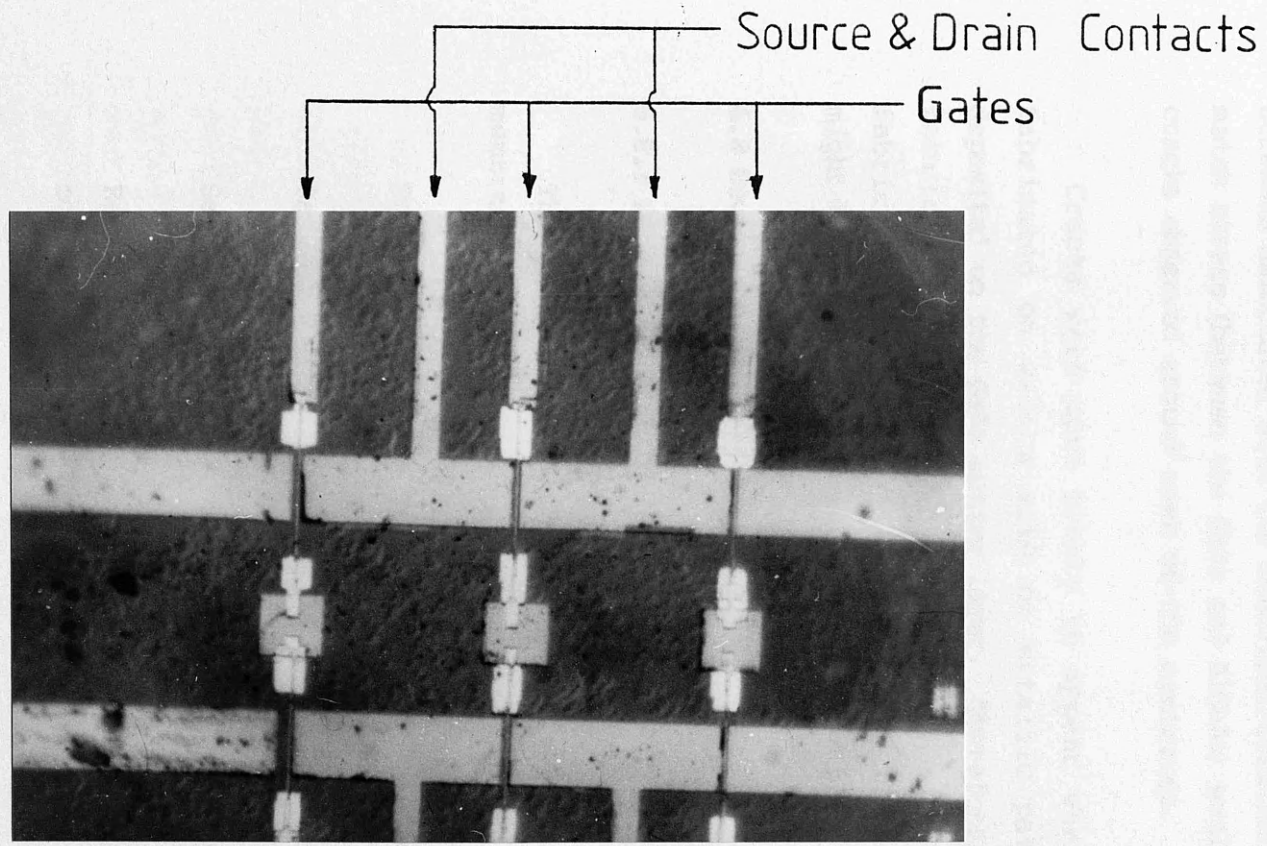


Fig 6.14 Optical micrograph of a membrane device complete with gate metallisation.

away from the membrane edges. Besides, during the TEM examination of the membranes prior to the x-ray microanalysis experiments it was observed that the stresses in the membranes were not excessive. Therefore membrane stress is unlikely to be the only origin of these cracks. It may be possible however, that the stresses associated with the membranes combined with crystal mismatch stress (between the GaAs and AlGaAs) would give rise to the cracks observed around some of the membranes.

Cracks were more likely to appear when membranes were fabricated on wafers with no metallic patterns previously deposited on the GaAs active layer. Therefore, in actual device fabrication (where contacts are pattened before membrane fabrication), the cracks did not present as big a problem as might have been expected.

6.8 Device Fabrication

6.8.1 Process Outline

The steps involved in fabricating actual devices on the membranes are as follows:-

Deposit markers on the active GaAs side of the wafer.

Pattern metal on polymer masks relative to the markers.

Send the sample for boron implantation (isolation).

Remove the mask and pattern the coarse source-drain contacts.

Back to front align then form the GaAs membranes.

Pattern the fine source drain-contacts and anneal.

Pattern the gates.

Test.

6.8.2 Markers.

The markers were patterned by electron beam exposure of low molecular weight PMMA and lift-off. A frame size of 400 X 300 μm was used because this would best accomodate the membrane with surrounding pads in the eventual device. The markers were metallised with a 50 nm layer of gold, with a thin nichrome layer to promote adhesion to the GaAs.

6.8.3 Metal on Polymer Mask

The pattern used for the metal on polymer (MOP) mask is shown in fig. 6.15. MOP masks consisting of 350 nm polyimide with 800 nm Ge were fabricated using the technique described in chapter 5. The wafers were then sent to Edinburgh University's Microfabrication Facility for boron implantation. The samples were implanted with a boron dose of 2.10^{13} ions/cm^2 at energies of 40 and 80 keV. This was sufficient to completely isolate the active GaAs layer of the samples.

When the wafers were returned the MOP masks were removed by dissolving the polyimide layer in boiling acetophenone. The metal mask then simply lifted-off the surface. Any parts of the mask which did not lift-off were given extra assistance using ultrasonic agitation (in cold acetophenone) or as a last resort the cotton bud treatment (sect 5.4.6) was used. Once the mask had been completely removed the surface of the wafers was perfectly clean. It was impossible to tell using an optical microscope where the mask had been (although the original markers were still present). However, when the wafers were placed in the SEM, the contrast between the implanted and unimplanted regions was very high. An SEM micrograph of a masked area of the wafer is shown in fig. 6.16. The contrast between implanted and unimplanted areas is sufficiently high that in future devices alignment to masked areas of the chip may be considered.

6.8.4 Coarse Contacts Pattern

The coarse ohmic contact pattern was patterned on the GaAs wafer, aligning to the markers so that the source-drain gaps

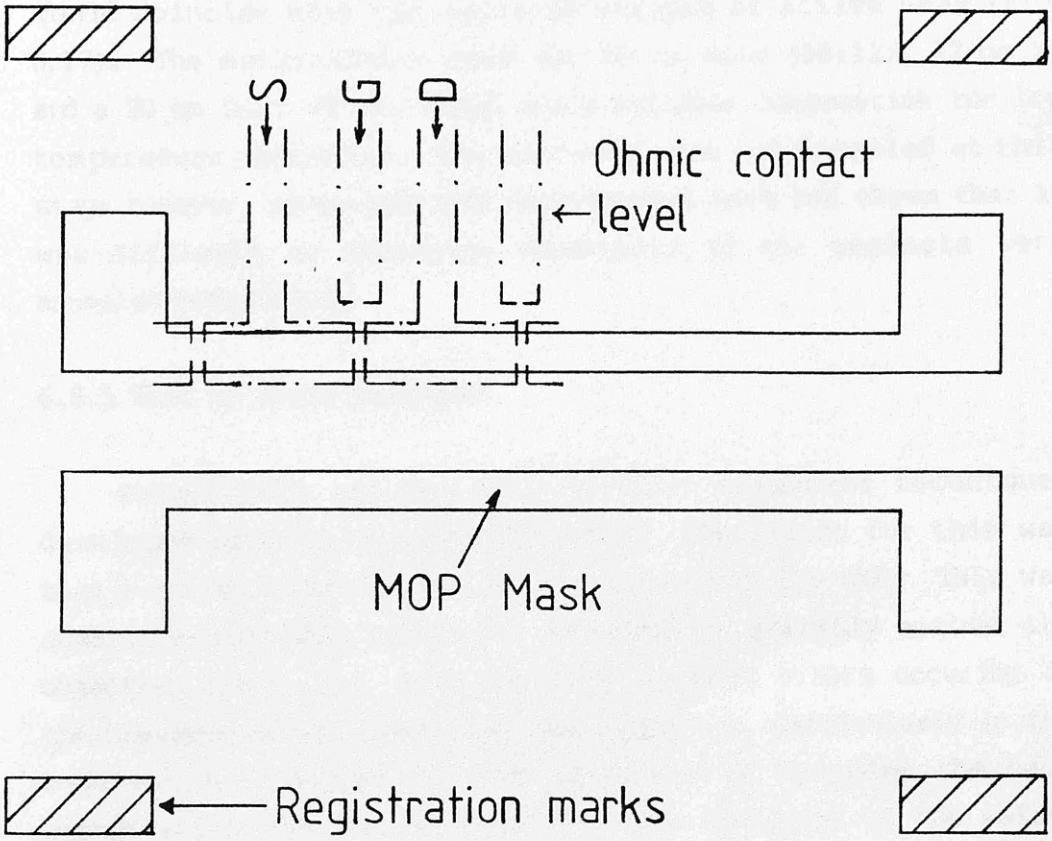


Fig 6.15 Metal on Polymer mask pattern for membrane isolation.

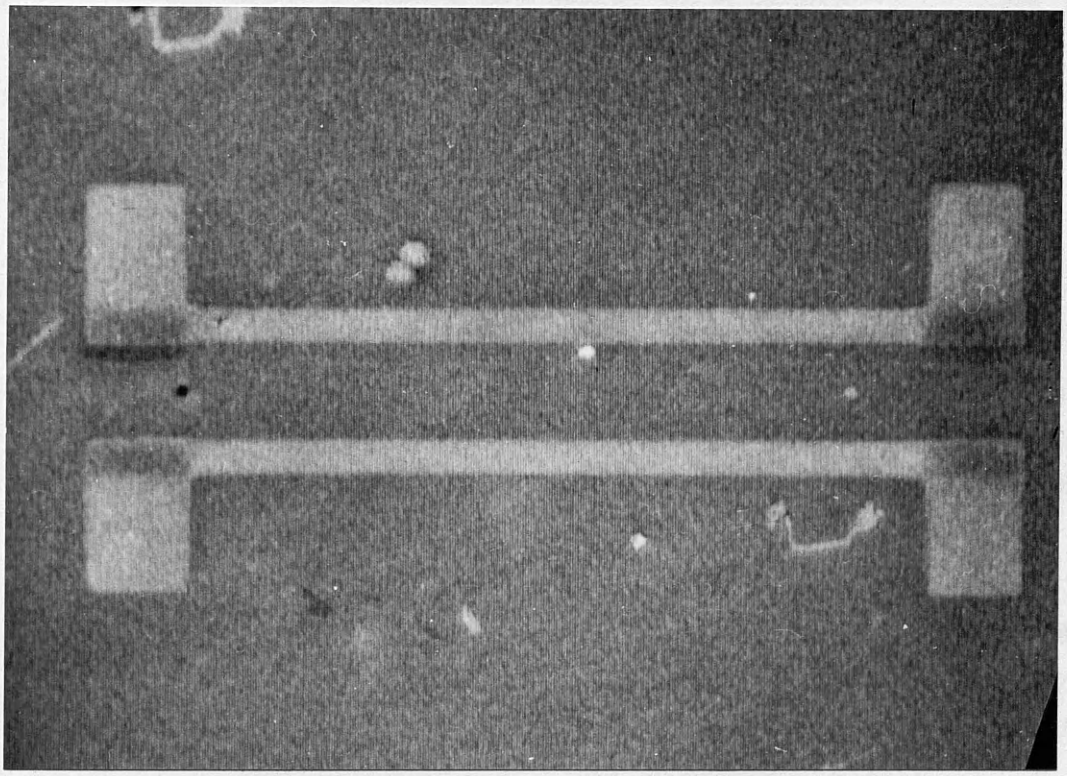


Fig 6.16 SEM micrograph showing the high contrast which is obtained between implanted and unimplanted GaAs.

would coincide with the isolated stripes of active GaAs (fig. 6.17). The metallistion used was 80 nm AuGe (88:12), 12 nm Ni and a 20 nm layer of Au, which was a suitable composition for low temperature annealing. The contacts were not annealed at this stage however, since previous experimental work had shown that it was difficult to fabricate membranes if the contacts were annealed beforehand.

6.8.5 Back to Front Alignment

Attempts to use the back to front alignment techniques developed earlier were unsuccessful. The reason for this was that a new specimen holder was being used in the SEM. This was obstructed partially inside the SEM chamber, possibly against the objective lense cap. This resulted in large errors occuring in the movement of the sample between exposures, particularly in the x-direction. Therefore, the technique of aligning the back etched wells with two wells etched from the front of the wafer, could not be used.

Consequently, the method used for aligning the back etched wells to the boron isolated areas was to calculate the distance from each exposure site to the nearest edges of the wafer and then turn the wafer over and expose the back etch windows accordingly. In order to achieve reasonable accuracy with this method, the wafers were first divided into smaller chips with say 2 x 3 eposure sites per chip. Using this technique it was possible to align the back etched wells to within the required 20 μm of the isolated regions.

6.8.6 Etching the Back Etched Wells

The same methods described earlier were used for etching the GaAs substrate and then the etch stop layers to produce the GaAs membranes. When the first fast etch had reached within 10 μm of te etch stop layers the sample was scribed and then broken into individual chips. These chips were then etched seperately. It was found that when these samples were removed from the plastic strips (see Sect. 6.5.6), the number of membranes which survived was significantly higher than was obtained before when no

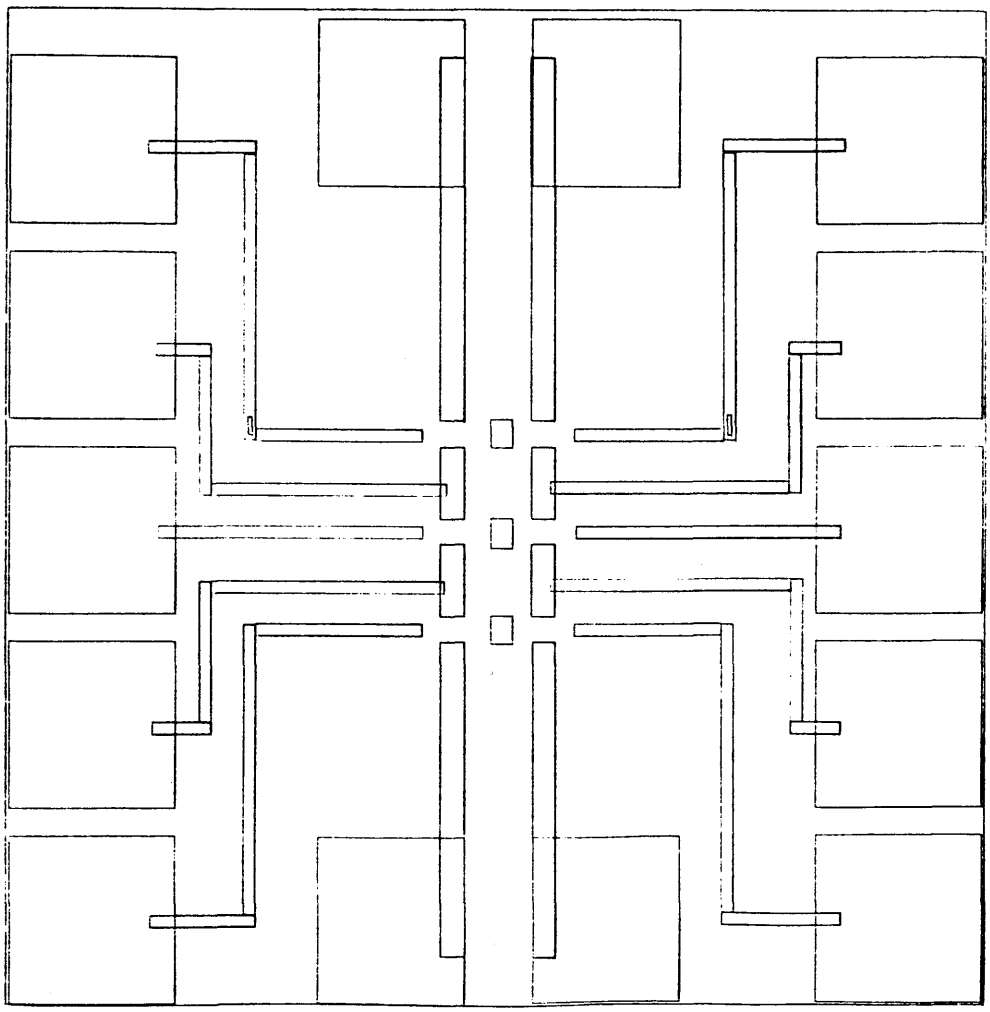


Fig. 6.17 Course device ohmic contact pattern for deposition before the fabrication of the membrane itself. It can be seen that the closely spaced contacts and alignment marks of fig 6.12 have been omitted.

contacts had been patterned on the front of the wafer before fabricating the membrane. It is likely that the contacts, which extend from pads on the solid part of the wafer on to the membrane itself, strengthen the membrane and hence, make it easier to remove them from their plastic strips.

6.8.7 Annealing

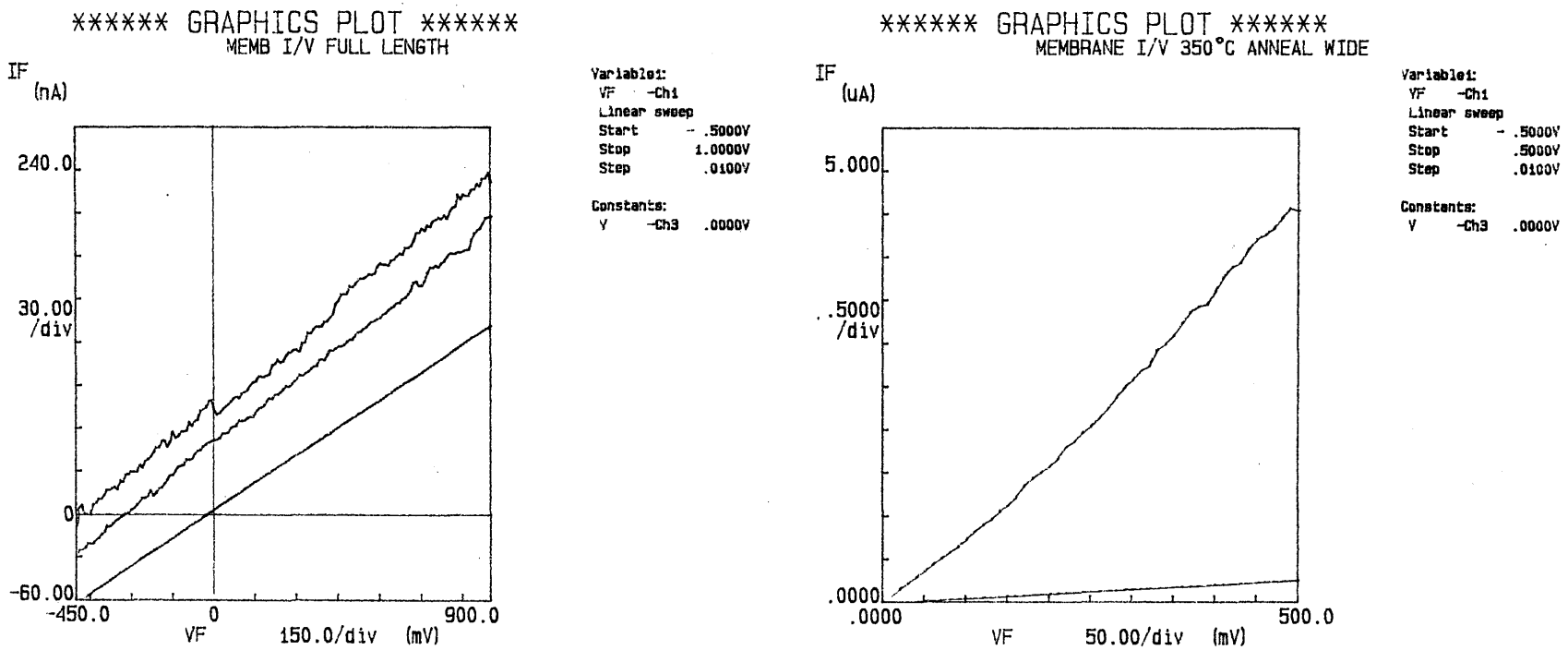
The completed membrane samples were mounted on to the copper sample holders (fig. 6.11) described previously. They were then annealed at 325 ^{o}C for 1 minute in 95:5 Ar:H_2.

6.8.8 Testing

When the samples had been annealed they were tested to see if any current could be passed through the active part of the membranes. The source drain pads on the solid substrate were carefully probed and the current between them measured. It was found that with an applied voltage of 1 volt the current between contacts was typically less than 1 μA although higher currents were obtained on some of the samples.

Fig. 6.18 is an output plot from the HP 4145A semiconductor ananlyser. It can be seen that the current through the membrane, at a given voltage, increases as the microscope illumination on the probing system increases. This indicates that there are optically induced carriers being generated on the wafer. However, the interesting point is that the current measured between the source-drain contacts is significantly higher (x10) than the leakage current between isolated pads. Therefore, the current, even though it is very small, must be flowing through through the active source drain channel on the membranes.

The reason the current was so small was originally thought to be due to poor electrical contact between the pads and the device caused by the cracks which sometimes appear at the membrane edges (see sect 6.7). It was in fact shown that on samples with no cracks (as observed under an optical microscope), currents of up to 10 μA could be passed between the source-drain contacts for 1 V applied (fig 6.18 up to 0.5 V).



a)

b)

Fig. 6.18 I/V curves obtained from membrane devices. a) The current increases for a given voltage as the microscope illumination is increase. b) Difference in current between pads connected by active material (top curve) and between isolated pads (bottom curve).

The width of the active channel between contacts on the membrane samples was 9 μm, the same width as the active channel on the solid substrate devices fabricated on this material (see sect 4.3.5). However, the maximum current measured between contacts on the membrane devices was 10 μA (with 1 V applied) but, for a similar voltage applied to the solid substrate devices, the current between contacts was over 100 μA. It is therefore reasonable to assume that the pinning of the Fermi level by the surface states, in the membrane, was almost sufficient to completely deplete the GaAs membrane of carriers. For a depletion width of 50 nm (half the thickness of the membrane), the doping concentration of the GaAs membrane was estimated to be 3.10^{17} /cm^3 [6.15]. Using this value of doping concentration the energy band diagram was evaluated [6.16] for n+ GaAs on undoped AlGaAs (60 % Al). As there was no information available on the AlGaAs layer, a background doping level of 10^{16} (both p and n type) was assumed.

Figure 6.19 contains the estimated band diagrams for GaAs (5.1017 /cm^3), on undoped AlGaAs (Al=60 %) for both n$^-$ and p$^-$ AlGaAs layers. The surface depletion (50 nm) was estimated for a surface barrier potential of 0.6 V [6.15]. It can be seen that with both a p$^-$ and an n$^-$ AlGaAs layer, the depletion width at the GaAs side of the GaAs/AlGaAs interface is relatively small compared with the depletion from the surface of the GaAs. In fact, at the interface of the GaAs/n$^-$AlGaAs structure the conduction bends down slightly which could lead to a weak electron accumulation layer at the interface. However, if the AlGaAs layer is removed, there will be surface depletion from both sides of the GaAs (see inset Fig. 6.19) which will drastically reduce the width of the conducting channel in the membrane. This is exactly the effect which was observed when the membrane devices were compared with the solid substrate devices fabricated previously.

Due to time and material limitations it was not possible to obtain different material with the correct doping and GaAs thickness. It was also decided to abandon the devices fabricated up to the stage of measuring source-drain currents, because these currents were so low.

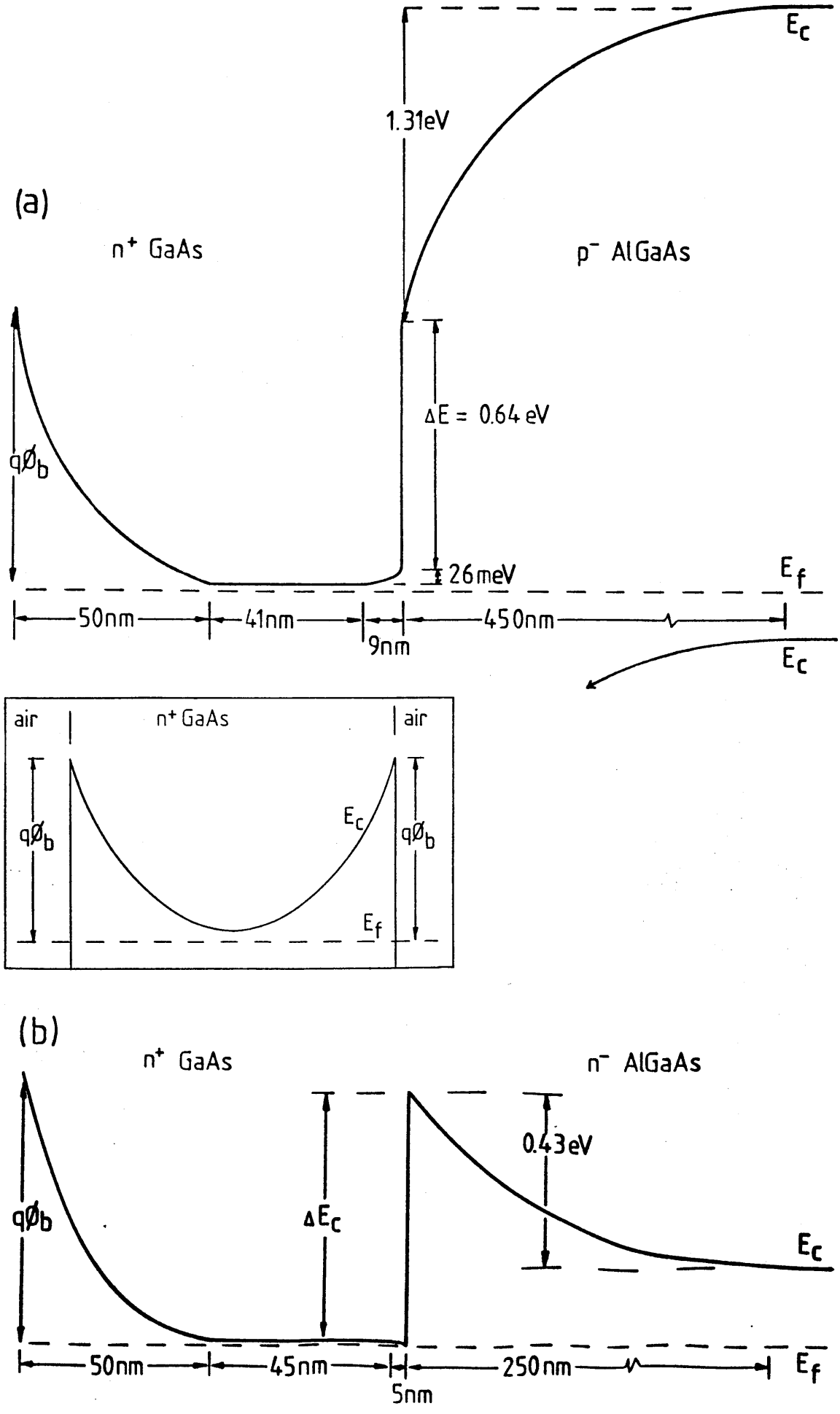


Fig 6.19. Energy band diagram of GaAs on a) a p^- AlGaAs substrate and b) an n^- AlGaAs substrate. The inset shows the effect of removing the substrate completely.

6.9 Future of GaAs Membrane Devices

Although no transistors were fabricated on GaAs membranes, the experiments carried out showed promising signs for the future. The fact that several lithographic steps, including annealing of contacts could be done on the same membrane, showed that there are no fabrication difficulties. Back to front alignment of the etched wells to previously defined markers was also shown to be satisfactory.

The only question to be answered is whether sufficient current will flow through the active channels when a GaAs membrane of sufficient thickness and doping is fabricated. If the current is similar to what would be expected on an epitaxial layer on a solid substrate then it should be possible to fabricate working devices.

Chapter 6 References.

[6.1] WS Mackie, SP Beaumont, CDW Wilkinson, JS Roberts, "High Resolution Lithography on Thin Active semiconductor Membranes," Proc. 10th Electron and Ion Beam Science and Technology Conference, Montreal, Canada (May 1982).

[6.2] WS Mackie, PhD Thesis, Glasgow University, 1984.

[6.3] SP Beaumont, B Singh, CDW Wilkinson, "Very High Resolution Electron-Beam Lithography - Thin Films or Solid substrates?" Proc. 10th Electron and Ion Beam Science and Technology Conference, Montreal, Canada, (May 1982).

[6.4] WS Mackie, SP Beaumont, "Materials and Processes for Nanometre Lithography," Solid State Tech, Aug 1985, p117-122.

[6.5] K Hess, "Ballistic Electron Transport in Semiconductors," IEEE Trans. Elect. Dev. **ED-28**, p937-940 (1981).

[6.6] Y Awano, K Tomizawa, N Hasizume, M Kawashima, "Monte Carlo Particle Simulation of a GaAs Short-Channel MESFET," Elect. Lett. **19** p20-21 (1983)

[6.7] WS Mackie, SP Beaumont, PG Bower, CDW Wilkinson, "Very High Resolution Alignment of Electron-Beam Written Patterns," Proc. Microcircuit Eng. 82, Grenoble, France.

[6.8] M Losco, "Fabrication of Silicon Nitride Membranes for Electron-Beam Lithography," Unpublished (1980)

[6.9] The wafers were polished by Mr K Piechowiak, who is gratefully acknowledged.

[6.10] KY Lee, Internal Communication.

[6.11] DW Shaw, "Localised GaAs Etching With Acidic Hydrogen Peroxide Solutions," J. Electrochem. Soc, **128**, p874 (1981).

[6.12] RJM Giffiths, ID Blenkinsop, DM Wright, "Preparation and Novel Properties of GaAs Layers for Novel FET Structures," Elect. Lett. 15 p629 (1979)

[6.13] CH Oxley, Plessey Research Centre (Caswell), Private Communication

[6.14] XS Zu, LA Coldrew, JL Mertz, "Selective, Etching Characteristics of HF for AlGaAs/GaAs," Elect. Lett, **22**, p558-559 (1985)

[6.15] A Chandra, CEC Wood, DW Woodward, LF Eastman, "Surface and Interface Depletion Corrections to Free Carrier-Density Determination by Hall Measurements," Solid State Elect. **22**, p645-650 (1979).

[6.16] SM Sze, "Physics of Semiconductor Devices," 2nd-Ed. Sect. 2.8, p122-129, Wiley, New York (1981).

7.1 Introduction

In this chapter a brief description is given of the design and fabrication of high electron mobility transistors, otherwise known as HEMTs, MODFETs (modulation doped FETs) or TEGFETs (2-D Electron gas FETs). It was originally intended to fabricate very small HEMTs on membrane structures taking full advantage of the high resolution capabilities of e-beam lithography, on thin substrates, to shrink the device dimensions to their limit. However, restrictions on time and material meant that it was only possible to begin to study HEMTs, the starting point of which was a solid substrate device.

7.1.1 Introduction to HEMTs

Interest in high electron mobility transistors originated about seven years ago when it was reported that the mobilities obtained in modulation doped GaAs/AlGaAs hetorojunction interfaces were more than an order of magnitude greater than in bulk material at low temperatures (2K) [7.1]. The high mobility arises because the carriers (electrons) in such a structure are separated from their parent donor atoms. This is illustrated in fig 7.1 which is a schematic representation of a modulation-doped heterojunction. The structure consists of a doped AlGaAs layer grown on a high purity undoped GaAs layer. Because the band gap of the GaAs layer is smaller than that of AlGaAs, electrons are transfered from the doped material into the smaller band-gap undoped material (fig 7.1b)). The mobility of electrons in the undoped layer is enhanced due to the relatively low number of ionised impurities scattering centres in the GaAs layer. Since the early pioneering experiments on heterojunctions, extremely high mobilities have been obtained. Recently in a review article by Dingle [7.2] it is reported that low temperature mobilities of over 2.10^6 cm^2/Vs have been achieved. To obtain this high mobility value, the design of the heterojunction has to be optimised. This will be discussed in sect 7.1.2. Interest in utilising the high mobility of modulation doped structures stimulated keen interest in fabricating very fast FET devices.

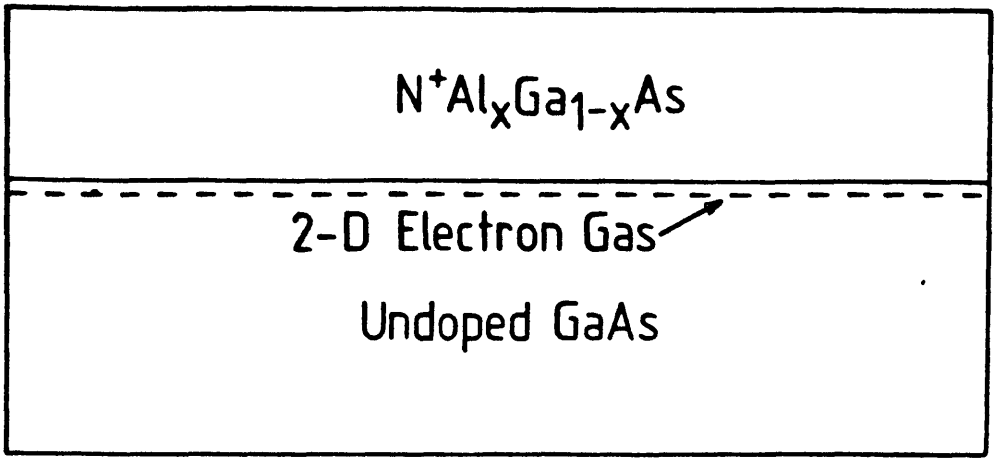


Fig. 7.1a) Modulation-doped n^+ AlGaAs / undoped-GaAs heterojunction

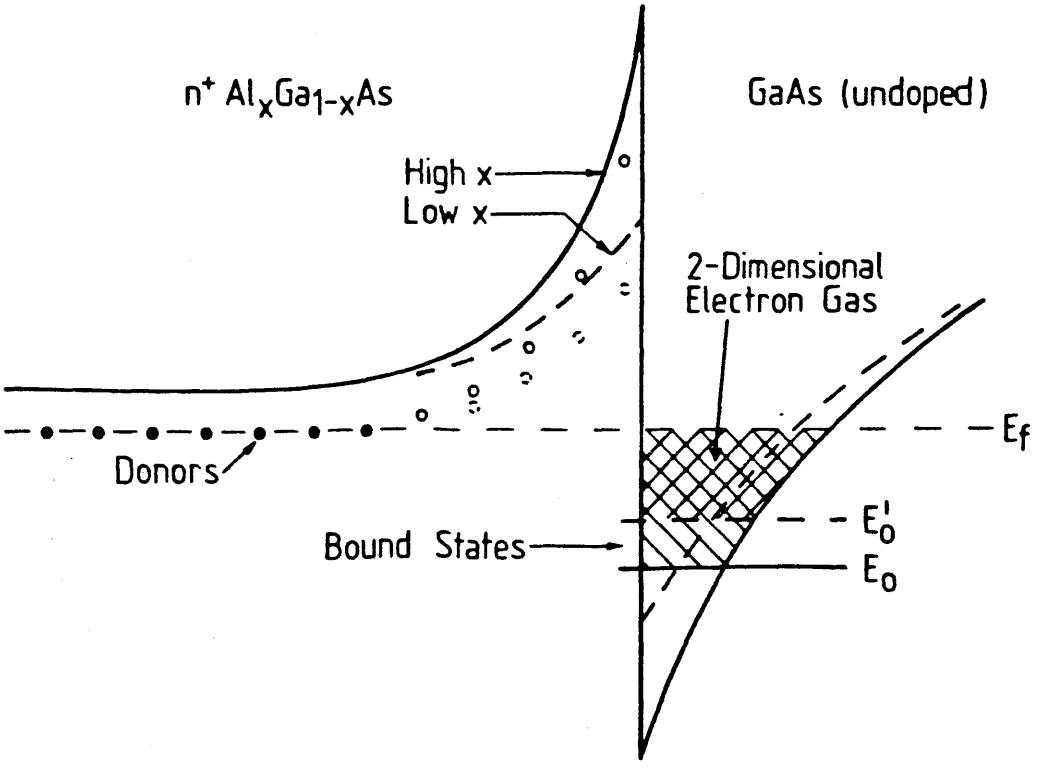


Fig 7.1b) Energy band diagram of a modulation doped heterojunction showing the location of the two dimensional electron gas.

After Dingle's first report [7.1] several research groups strived to produce such a device, but it was T Mimura of Fijitsu Labs who reported the first HEMT device [7.3]. Since then, there has been a lot of interest in HEMTs and currently the best ring oscillator results show switching speeds of 9.4 ps [7.4]. Surprisingly, the switching speed of this device is only marginally better than the best reported value for a GaAs MESFET (9.7 ps [7.5]).

7.1.2. Design Considerations

An indication of some of the design criteria for high electron mobility FETs is given in this section. Basically, the carrier concentration in the 2-DEG (2-dimensional electron gas) depends upon the composition of the AlGaAs layer (which determines the barrier height at the interface) and the doping of the AlGaAs layer [7.6,7.7]. It is generally accepted that an Al concentration of 30 to 35 % is used for HEMT fabrication [7.8]. The maximum mobility is reported to be obtained when the sheet carrier concentration is around 7-9 X 10^{11} [7.9,7.10]. At higher carrier concentrations there is a reduction in mobility due to inter-subband scattering; the second subband of the quasitriangular potential well (fig 7.1b)) becomes populated when the sheet carrier concentration exceeds 7 X 10^{11} cm^{-2} [7.6].

The incorporation of an undoped AlGaAs spacer layer, between the doped AlGaAs and the undoped GaAs layer, has also been shown to enhance the mobility of the 2-DEG [7.7,7.10]. As the spacer thickness increases the mobility rises because the Coulombic interaction between the electrons and their donor ions is reduced. However, beyond a certain thickness electron transfer becomes less efficient resulting in a lower sheet carrier concentration in the 2-DEG. A spacer thickness of 5 nm has been shown to be the optimum value for high mobility at the $Al_{.33}Ga_{.67}As$-GaAs interface [7.11]. The background doping of the GaAs layer also affects the electron mobility. Drummond et al [7.12] reported mobility values of 30 000 and 5400 cm^2/Vs (78K) with GaAs doping densities of 10^{16} and 10^{17} $/cm^3$ respectively.

7.2 HEMT Fabrication

7.2.1 Design of the HEMT Structure.

The structure of the proposed HEMT device is shown in fig. 7.2a) and the energy band diagram for this structure is shown in fig. 7.2b) [7.13]. A GaAs capping layer was included to facilitate the fabrication of the Schottky gate in the device. To avoid parallel conduction in the doped AlGaAs layer (which would have a detremental effect on the mobility [7.14,7.15]) the HEMT structure was designed in such a way that the distance W_p in fig. 7.2b)) was zero. The AlGaAs layer would then be fully depleted and no parallel conduction could occur. The theory given in the paper by Schubert et al [7.13] was used to estimate the depletion widths W_{ds} and W_d (fig 7.2b)) for a selected doping concentration of 10^{18}, an Al mole fraction of 35 %, a GaAs capping layer thickness of 15 nm and an undoped spacer thickness of 5 nm. These values were Wd = 15nm and Wds = 26 nm which is a total depletion width of 41 nm. A value of 40 nm was chosen for the thickness of the doped AlGaAs layer. With the layer dimensions and doping concentrations used in this design, the estimated sheet carrier concentration in the 2-DEG was 16.10^{11} cm^{-2}. This is higher than the concentration required for maximum mobility, but was chosen to give a higher drain current in the HEMT devices.

7.2.2 Material Growth

The HEMT material was grown by the MBE group in this Department [7.16] on an undoped substrate. No magnetoresistance measurements were made to verify the existance of a two-dimensional electron gas (2-DEG) [7.17], but the mobility of the wafer was measured to be 4000 cm^2/Vs at room temperature and 10000 cm^2/Vs at 77K. These mobilities were higher than typical mobilities (1000-2000 cm^2/Vs at room temperature) of GaAs layers with similar doping grown for MESFET and other applications. The existance of a 2-DEG was therefore assumed.

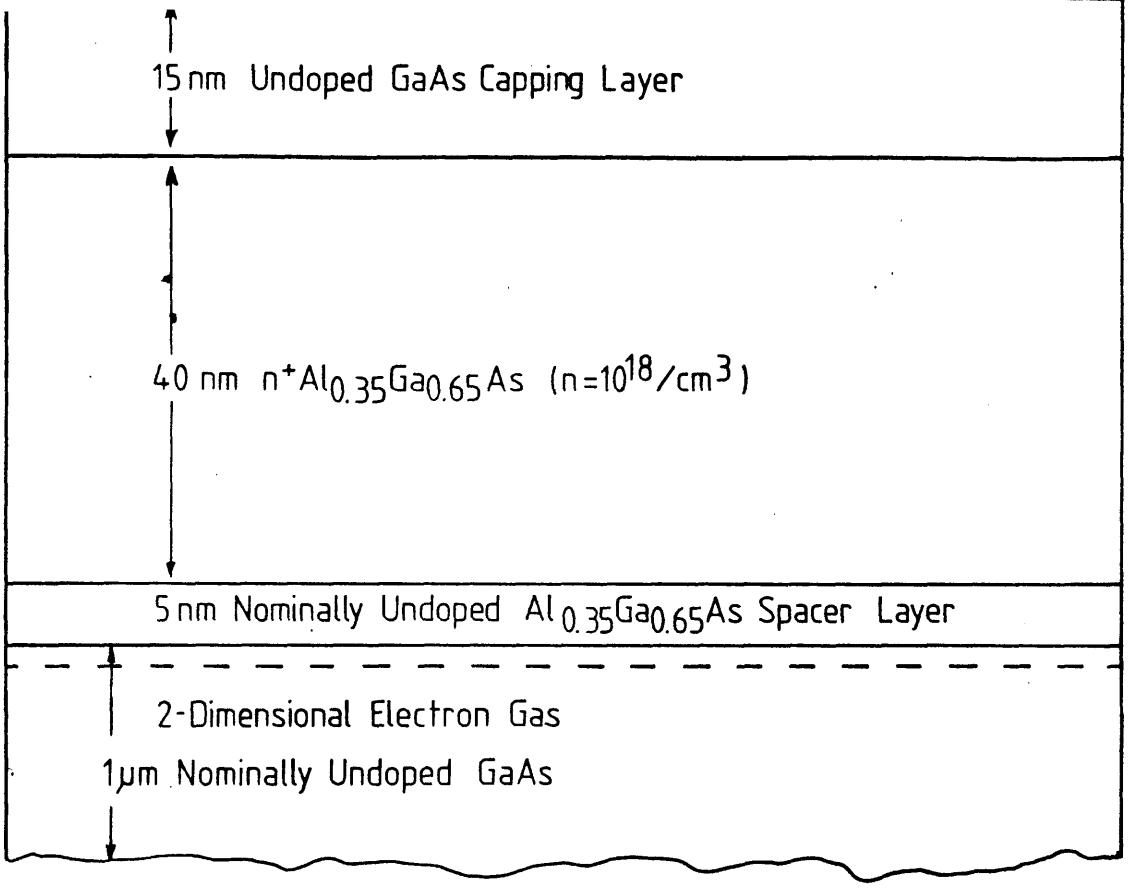


Fig. 7.2a) Structure of the proposed HEMT material.

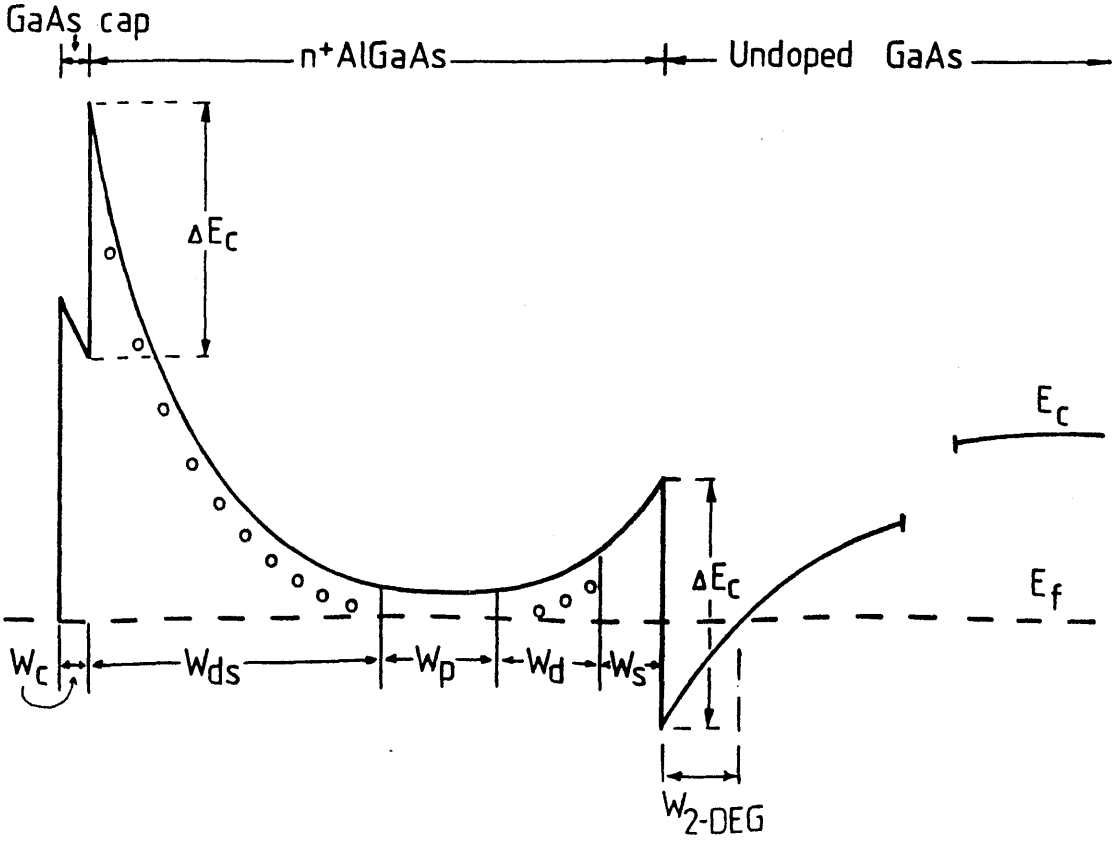


Fig. 7.2b) Energy band diagram of the HEMT structure shown in fig. a).

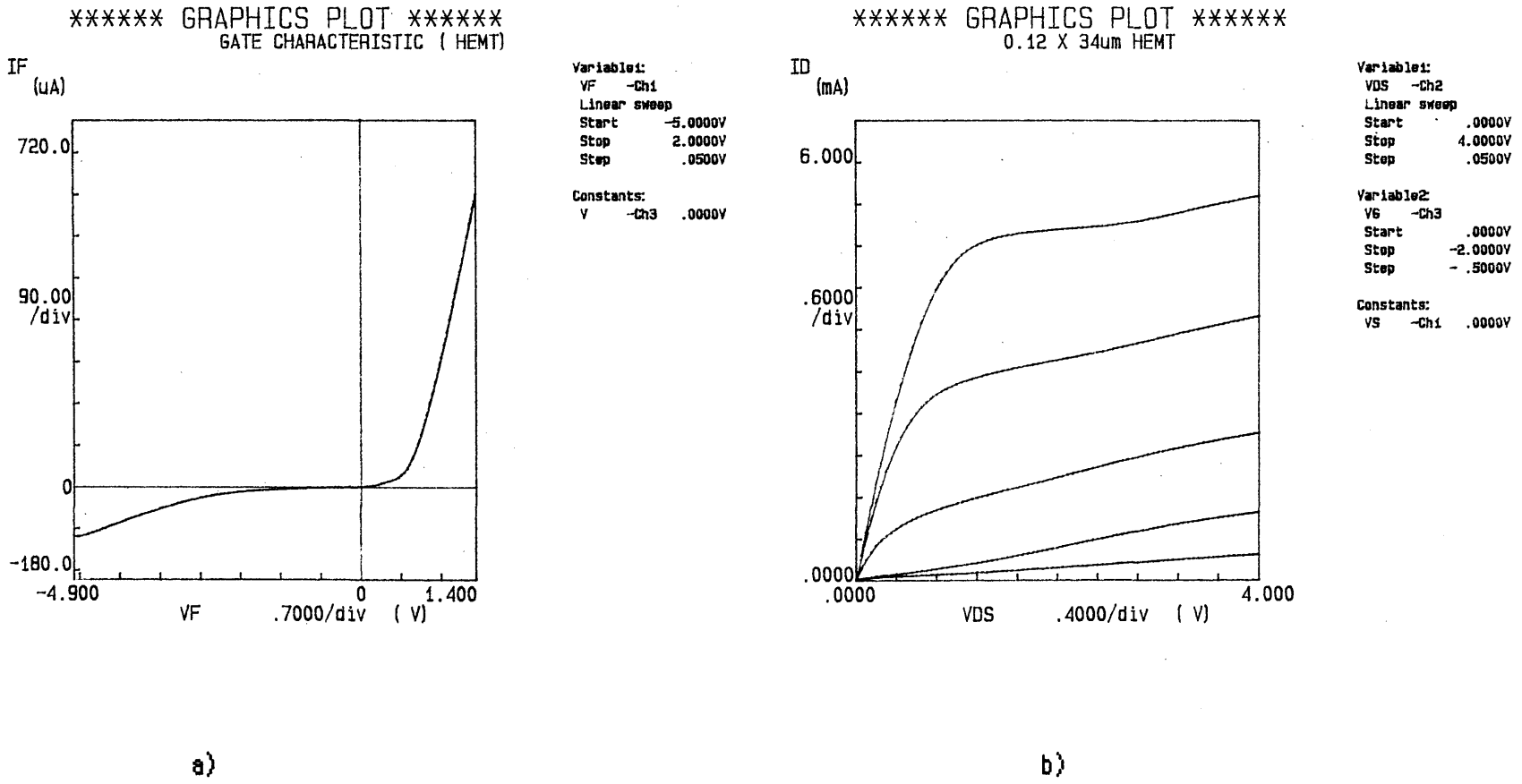
7.2.3 Fabrication

The HEMTs were fabricated using the processes and patterns developed for GaAs MESFETs (ac design, chap 4). The only difference was in the ohmic contact metallisation. A standard contact composition (100 nm AuGe and 5 % Ni) was deposited and the contacts were annealed at 400 ^{o}C. The reason for this was to ensure that during annealing the contact metal diffuses through the undoped capping layer and into the underlying AlGaAs layer. However, as the capping layer was only 15 nm thick, it is likely that the low temperature annealing process could have been used for the contact formation. The contact resistance measured on TLM structures on the device wafers was 10^{-4} ohm.cm^2 which is a relatively high value. This could be due to the high sheet resistance of 1400 ohm/square (c.f. 400 ohm/square on MESFET material) which was also determined from the TLM structures. Devices were fabricated initially without recessing the gates. However, it was found that the quality of the Schottky gate characteristics was poor, presumably due to oxide on the surface of the GaAs. In an attempt to improve the gate characteristics, a very shallow recess was etched using the proprietry Plessey etch which should have left the GaAs surface oxide-free. However, because the GaAs capping layer was so thin, it was not possible to etch too far or the gate would have been deposited on the AlGaAs layer which is known to oxidise rapidly in atmospheric conditions. Unfortunately, it turned out that the shallow recessed gates were no better than the unrecessed gates, so recessing was abandoned.

7.3 HEMT Characteristics

The I/V characteristics of a typical gate deposited on a HEMT structure is shown in fig. 7.3a). It can be seen that the reverse breakdown voltage for this gate is only about 2 volts. The log(I)/V curves of the forward bias gate was so erratic it was impossible to determine the barrier height and ideality factor of this, or any other, Schottky contacts on HEMT material.

The dc output I/V characteristics of a 0.12 μm gate-length HEMT (34 μm gate-width) is shown in fig. 7.3b). It can be seen



a)

b)

Fig. 7.3 a) Gate characteristics of a typical HEMT device. b) DC output characteristics of a 0.12 x 34 µm gate HEMT

that the device saturates reasonably well for drain-source voltages above 0.8 volts. This is lower than the saturation voltages (typically 1.5-2 V) observed on MESFET devices. The transconductance of this device is 140 mS/mm which was the highest value of g_m measured on any of the devices. Longer gate-length devices were fabricated (up to 0.4 µm), but, there was no significant correlation between the device gate length and the measured value of g_m.

The source resistance of the 34 µm device shown in fig. 7.3b) was determined to be 54 ohms, using a method described by Fukui for MESFET applications [7.18]. Using this value of R_s the intrinsic transconductance of the HEMT can be calculated to be 190 mS/mm. This is very close to the value for the maximum transconductance of 218 mS/mm calculated for this device using the theory presented by Lee and Shur [7.19]. Similarly, the maximum drain current for a 34 µm wide device was calculated to be 8.7 mA. From the I/V curves of fig 7.3b) for a 34 µm channel device, it can be seen that the drain current for 0 V gate-bias is around 6 mA. The difference in drain current could be due to a lower than expected carrier concentration in the 2-DEG. For a drain current of 6 mA the sheet carrier concentration was calculated to be 11.10^{11} /cm^2 which is about 30 % lower than the expected value of 16.10^{11} /cm^2. The lower carrier concentration could partly be due to a lower than specified doping in the AlGaAs layer or a slight variation between the spacer layer specification and the actual material parameters. This would also account for the slight differences in the intrinsic transconductance values.

7.4 Discussion

High Electron Mobility Transistors were fabricated, but, from the dc characteristics of these devices, no significant improvement in device performance was observed. However, the device transconductance and maximum drain current values agree reasonably well with the calculated values for this particular design. With hindsight, a different approach should have been adopted in the design of the HEMT material. Since the low field mobility does not strongly affect device performance, the HEMT

structure should have been designed to maximise the charge transfer across the heterojunction. This could have been achieved using a thinner undoped spacer layer and/or by increasing the doping of the AlGaAs layer. The higher carrier concentration in the 2-DEG would lead to higher drain currents which would improve the switching speed of the device because the charging time of the effective gate capacitance is dependent on the current [7.19]. The thickness of the undoped GaAs capping layer would also have to be modified. The formation of a good Schottky contact generally requires the removal of 20-30 nm of GaAs prior to the metal evaporation. This is effectively to remove the residual surface oxide and leave the GaAs surface free from contamination. If this amount of recessing is to be achieved on HEMT structures, the GaAs capping layer should be increased to approximately 50 nm.

Chapter 7 References

[7.1] R Dingle, HL Stormer, AC Gossard, W, Wiegman, "Electron Mobilities in Modulation Doped Semiconductor Heterojunction Superlattices," Appl. Phys. Lett, 33, p665-670 (1978).

[7.2] R Dingle, "New High Speed III-V Devices for Integrated Circuits," IEEE Trans. Elect. Dev, **ED-31**, p1662-1667 (1984).

[7.3] T. Mimura, S Hiyamizu, T Fujii, K Nanbu, "A New Field-Effect Transistor With Selectively Doped GaAS/n-AlGaAs Heterojunctions," Jpn. J. Appl. Phys. **19**, pL225-L227 (1980).

[7.4] SS Pei, NJ Shah, RH Hendel, CW Tu, R Dingle, Ref. 12 cited in [7.2].

[7.5] K Yamasaki, N Kato, M Hirayama, "Below 10 ps/Gate Operation With Buried P-Layer SAINT FETs," Elect. Lett, **20**, p1029-1031 (1984).

[7.6] HL Stormer, AC Gossard, W Wiegmann, K Baldwin, "Dependence of Electron Mobility in Modulation-Doped GaAs/AlGaAs Heterojunction Interfaces on Electron Density and Al Concentration," Appl. Phys. Lett, **39**, p912-914 (1981).

[7.7] P Delescue, M Laviron, J Chaplart, D Delagebeaudeuf, NT Linh, "Transport Properties in GaAs/AlGaAs Heterostructures and MESFET Application," Elect. Lett, **17**, p342-344 (1981).

[7.8] M Laviron, D Delagebeaudeuf, P Delescluse, P Etienne, J Chaplart, NT Linh, "Low Noise Normally Off Two-Dimensional Electron Gas Field-Effect Transistors," Appl. Phys. Lett, **40**, p530-532 (1982).

[7.9] S Mori, T Ando, "Electronic Properties of a Semiconductor Superlattice II. Low Temperature Mobility Perpendicular to the Superlattice," J. Phys. Soc. Japan, **48**, p865-873 (1980).

[7.10] S Hiyamizu, T Mimura, T Fujii, K Nanb, "High Mobility of Two-Dimensional Electrons at the GaAs/n-AlGaAs Heterojunction Interface," Appl. Phys. Lett. **37**, p805-807 (1980).

[7.11] LC Witkowski, TJ drummond, CM Stanchac, H Morkoc, "High Mobilities in AlGaAs-GaAs Heterojunctions," Appl. Phys. Lett. **37**, p1033-1035 (1980).

[7.12] TJ Drummond, W Kopp, H Morkoc, K Hess, AY Cho, BG Streetman, "Effect of Background Doping on the Electron Mobility of AlGaAs/GaAs heterostructures," J. Appl. Phys, **52**, p5689-5690 (1981).

[7.13] EF Schubert, K Ploog, H Dambkes, K Heime, "selectively Doped n-AlGaAs/GaAs Heterostructures With High Mobility Two-Dimensional Electron Gas for Field Effect Transistors. Part I Effect of parallel Conductance," Appl. Phys. A, **33**, p63-76 (1984)

[7.14] Ref [7.13] part II "Hot Electron Effects," p183-193

[7.15] M Keever, TJ Drummond, H Morkoc, K Hess, BG Streetman, M Ludowise, "Hall Effect and Mobility in Heterojunction Layers," J. Appl. Phys. **53**, p1034-1036 (1982).

[7.16] The HEMT layers were grown by J Frost who is gratefully acknowledged.

[7.17] R Dingle, HL Stormer, Ac Gossard, W Wiegman, "Electronic Properties of Modulation-Doped GaAs/AlGaAs Heterojunction Superlattices," GaAs And Related Compounds. Inst. Phys. conf. Ser. No 45, p249-255 (1978).

[7.18] H Fukui, "Determination of Basic Device Parameters of a GaAs MESFET," Bell System Tech. J. **58**, p771-797 (1979).

[7.19] K Lee, MS Shur, TJ Drummond, SL Su, WG Lyons, R Fischer, H Morkoc, "Design and Fabrication of High Transconductance Modulation-Doped AlGaAs/GaAs FETs," J. Vac. Sci. Tech. B, 1, p186-189 (1983).

A low temperature annealing process was developed for forming low resistivity ohmic contacts to GaAs. The composition of the commonly used AuGe/Ni/Au contact system was modified so that the optimum annealing temperature of these contacts was reduced from 420 ^{o}C to 300-320 ^{o}C with no apparent reduction in contact quality. A process was also developed for isolating devices using Boron ion implantation using a novel technique for fabricating Metal on Polymer ion implantation masks. Both of these processes have applications in the fabrication of extremely small devices; the low temperature annealing means that closely spaced contacts can be fabricated, reducing the risk of interdiffusion of the contact material during annealing and the boron isolation technique eliminates the need for mesa isolation which is not particularly suitable for very small devices.

GaAs MESFETs were fabricated with gate lengths down to 0.055 μm which are the smallest reported devices at this time. There was no significant deterioration of the dc output characteristics of these devices, even at the shortest gate lengths. However, as the gate length decreased, it was observed that the pinch-off properties of the devices gradually deteriorated. It was speculated that this effect was due to the poorly defined interface associated with the VPE material on which they were grown. Preliminary experiments on MBE wafers and MOCVD wafers with AlGaAs buffer layers resulted in devices with improved pinch-off properties but, for various reasons, exhibited inferior device performance. AC measurements of the short gate-length MESFETs were disappointingly poor. It was found that no correlation could be made between the s-parameter measurements and the physical dimensions of the devices tested.

Processing techniques were developed for the fabrication of Field Effect Transistor devices on thin GaAs substrates. All the steps for making such a device were carried out and shown to work satisfactorily. Unfortunately, when it came to producing an actual device, it was discovered that no current could be passed through the membrane; this signified the end of this work.

HEMT devices were fabricated on an MBE wafer grown in the Department. Although these devices did not produce particularly exciting dc output characteristics, they did perform close to the theoretical predictions for the particular structure grown.

Looking at the project as a whole, processes were developed which have particular applications in the production very small devices. Also, devices were fabricated close to the current lithographic limits on solid substrates. However, due to time limitations, it was not possible to combine both the processing and the lithography to produce small devices which take full advantage of the low temperature contact technology (to reduce the source-drain contact separation) and the boron isolation technique (to replace mesa isolation).

This means that future work can be pursued along several lines, the most obvious being the combination of the processes mentioned above with the lithographic technology to produce a device optimised for high frequency applications. In the work of this thesis it was particularly clear that, at very small dimensions, material parameters will play an important role in the performance of the device. Material specification should therefore be carefully considered for the fabrication of sub 0.1 μm gate-length MESFETs.

The HEMT design could be modified to produce devices with higher drain currents than the devices fabricated in this project. These devices should exhibit high transconductance values and improved rf performance, particularly at the short gate-lengths which can be defined by electron beam lithography.

Finally work could be continued on the fabrication of devices on thin active membranes. It has been shown by others in the Department, since the conclusion of this work, that current can be passed through a membrane. This means that the fabrication of a novel device is still possible. This should be of interest, not only because of the small dimensions at which such a device could be fabricated, but because the effects of the buffer layer of conventional devices would be removed competely.