Fabrication and Scaling Effects of Very Short Gate-Length GaAs MESFETs

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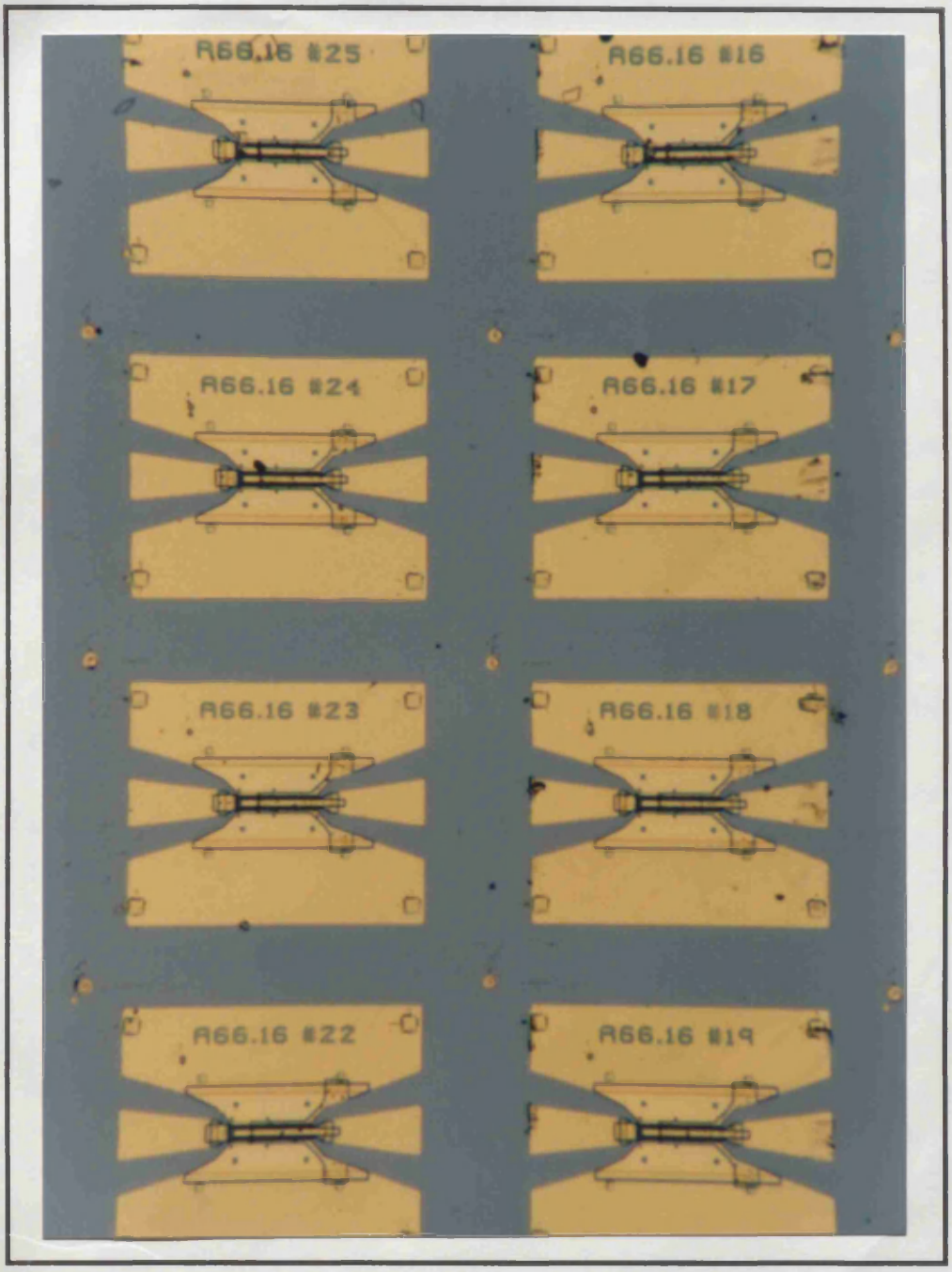

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For Julie

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Table of Contents

List of Figures

List of Tables

Summary

A process has been demonstrated[1] for the fabrication of scaled GaAs based metal-semiconductor field effect transistors (MESFETs) suitable for high frequency characterisation with gate-lengths down to 40nm. MESFETs were fabricated with gate-lengths in the range 40 to 300nm on molecular beam epitaxy (MBE) grown layers with GaAs and AlGaAs buffers. The MESFETs were characterised electrically at direct current (DC) and high frequency.

The MESFETs have very good DC and high frequency performance, even down to the shortest gate-lengths. The performance is characterised by figures of merit such as transconductance and unity current gain cut-off frequency. MESFETs with a DC extrinsic transconductance of 720mS/mm and unity gain cut-off frequency of 150GHz (for a 40nm gate-length) have been demonstrated[2].

However, the performance of the MESFETs is limited by scaling effects. Some of these effects are of a technological nature such as buffer layer current, a large gate resistance, surface depletion effects, and the high active layer doping. More importantly, the performance of the shortest gate-length MESFETs is restricted by the fundamental short-channel effects of punch-through and hot-electrons. The origin and function of many of these effects are introduced through a review of the operation and modelling of short-channel FETs.

The MESFET design included features to minimise the technological scaling effects. i.e.

1) AlGaAs buffer layers to suppress buffer layer current. Experimental comparison was made with the GaAs buffer case.

2) High active layer doping to reduce the effect of surface depletion and maintain the channel aspect ratio, at the cost of deteriorated carrier transport. Devices with three different doping concentrations were compared.

3) A reduced gate-width with shorter gate-length to compensate for the larger series gate resistance.

The experimental work described in this thesis investigates the scaling effects by electrical characterisation of the devices at DC and high frequency. The measurements presented and discussed include:

1) DC open channel and subthreshold transfer and output characteristics.

2) DC threshold voltage shift, equivalent to output conductance.

3) High frequency (up to 26.5GHz) S-parameters which yield the short-circuit current gain, maximum frequency of oscillation, and parasitic carrier transit delays through the channel.

The design strategy was successful to the extent of overcoming many of the detrimental scaling effects for MESFETs with gate-lengths down to 200nm. The buffer layer current was suppressed by the AlGaAs buffer, and it was shown that interrupted growth of the AlGaAs buffer can surmount the problem of degradation of active layer quality associated with MBE growth of GaAs on AlGaAs.

On the negative side, the technological problems of large gate resistance, surface depletion effects and very high active layer doping (which inhibits carrier transport) were found to significantly degrade the high frequency performance of the devices in this work. These are all issues which could be addressed by modifications to the device design. In addition, the parasitic carrier transit delays became more significant in degradation of high frequency performance as the gate-length was reduced.

As for the more fundamental effects, the main conclusion of this thesis is that the ultimate scaling limits of hot-electron and punch-through effects govern the behaviour of the MESFETs with very short gate-lengths (in this case, less than 100nm). The most severely affected parameters are output conductance and subthreshold current. For example, the benefits of AlGaAs buffer are greatly reduced for 40nm gate-length MESFETs. Reduction of gate-length can still give an improvement in high frequency performance, but less than predicted by simple scaling of the carrier transit time and the beneficial hot-electron effect of velocity overshoot. No evidence of velocity overshoot effects has been found in these MESFETs.

Chapter 1 - Introduction

1.1 GaAs Field Effects Transistors

GaAs Field Effect Transistor Applications

GaAs field-effect transistors (FETs) have many applications in high speed electronics. GaAs FETs are used as amplifiers, oscillators, mixers, switches, attenuators, modulators, and limiters. Two or more of these components can be integrated into monolithic microwave integrated circuits (MMICs). A major role of the GaAs FET in many of these MMICs is as an amplifier, and gain (voltage, current or power) at high frequency is a figure of merit. GaAs metal-semiconductor FETs (MESFETs) are also established as the dominant low noise active devices in the microwave and millimetre wave frequency range. Military applications of MMICs include very high frequency communication links and high definition electronically steerable phased array radars. Many very high speed instruments such as network analysers and sampling oscilloscopes benefit from GaAs MMICs. A large civil market for these circuits exists in ground receivers for direct broadcast satellites. Another potentially massive market is in high definition radars for collision avoidance in motor vehicles. Is it just coincidence that workers at Ford Microelectronics have demonstrated some of the best high speed GaAs MESFETs?

High speed digital circuits have been developed, using several different logic schemes. In these circuits, the GaAs FET is used as a switch, but gain is still a figure of merit because it is closely linked to the maximum switching speed and fanout capability of each logic gate. GaAs digital circuits have applications in high speed signal processing and computing (e.g. the latest generation of Cray supercomputers).

A promising application of GaAs FETs is integration with photodetectors and radiators (e.g. laser diodes) in optoelectronic circuits for communication applications. Here again the large gain and speed of GaAs FETs can be used to advantage.

GaAs MESFETs

Metal-semiconductor FETs (MESFETs) which use a Schottky diode as the gate electrode are superior to junction FETs (JFETs) which use a diffused p-n junction for high speed applications because of the reduced gate-source capacitance.

GaAs MESFETs have given better high frequency performance than bipolar transistors because they afford lower noise performance, high power gain and high output power.

GaAs is preferred to Si for microwave FET fabrication. The main advantages of GaAs are the higher electron mobility compared to Si and the higher average electron velocity, leading to lower transit times and thus superior high frequency response. In addition semi-insulating GaAs substrates allow simplified fabrication and reduced parasitic capacitances. GaAs has other advantages over Si, it is radiation hard and can operate over a wide range of temperatures from below 77K to above 525K.

The disadvantages of GaAs are a poor quality native oxide and a high surface state density both of which make fabrication of GaAs metal-oxide-semiconductor FETs (MOSFETs) difficult.

Most commercially available GaAs MESFETs are made using ion implantation into semi-insulating GaAs substrates

1.2 Aims of the Work

It was the primary aim of this work to produce GaAs FETs that have a large gain at high frequencies (tens of GHz). There are other performance parameters to consider, such as subthreshold current leakage for digital circuit applications.

The simplest way to improve high frequency performance in FETs is by reduction of the gate-length. Smaller carrier transit times and reduced capacitance under a short gate are the mechanisms of the performance improvement. However, there are other mechanisms of both a technological and fundamental nature which accompany the reduced gate-length and conspire to limit the performance increase so obtained.

Therefore, much of the work described in this thesis are investigations of the scaling effects and short-channel effects which have degraded the DC and high frequency performance of the MESFETs that have been fabricated. The term short-channel is used rather than short gate-length because many detrimental effects associated with a small ratio of length to height of the conducting channel in a FET can be overcome even for gate-lengths down to ~ 200nm as is demonstrated in this work. A short-channel can be regarded as having a channel length to height ratio of less than about 2.

The work involved design, fabrication and characterisation of discrete FET devices. The work also involved extensive development of automated electron-beam lithography. All aspects of device fabrication were undertaken from design of pattern sets to optimisation of wet etches for gate recessing. Characterisation of devices was by electrical measurements at DC and with high frequency S-parameter measurements.

1.3 Survey of the Following Chapters

Chapter 2 describes the terminology, physical layout and operation of scaled GaAs MESFETs and reviews the technological and fundamental scaling effects. Physical effects governing the electrical characteristics are introduced, leading to the definition of the figures of merit and important parameters of MESFET electrical performance. The effects of a short-channel on these parameters (both beneficial and detrimental) are discussed, and further insight is gained by reviewing the development of and results from FET models. The short-channel effects arising from the models are summarised, then the effects related to the technological aspects of scaling are reviewed. Finally, the best reported short gate-length FET performance at DC and high frequency are reviewed.

Chapter 3 describes the design and fabrication process of the MESFETs. The design of the semiconductor layers, device geometry and fabrication process are discussed. The methods of electron beam lithography (EBL) and alignment are described. Enhancements to the EBL system to facilitate the work are detailed. The complete sequence of fabrication of the MESFETs is presented, from wafer preparation to the steps specific to each pattern level.

Chapter 4 presents the results of DC and high-frequency electrical measurements of the GaAs MESFETs. First, characterisation some important material parameters of the as-grown layers are described. In the main experiment, GaAs and AlGaAs buffers are compared for confirmation of the beneficial role of the AlGaAs buffer layer in suppressing some of the short-channel effects. The comparison includes consideration of DC open channel and subthreshold output and transfer characteristics, threshold voltage shift, and high frequency S-parameter measurements. A subset of these measurements are used to compare MESFETs with an improved AlGaAs buffer growth technique and three different active layer doping concentrations.

Chapter 5 presents the conclusions of chapter 4, rearranged into groups of scaling effects in a similar format to the discussions of chapter 2. The final chapter also gives some suggestions for future work.

Chapter 2 - Scaled GaAs FETs

2.1 Introduction and List of Symbols

This chapter describes the operation of scaled GaAs MESFETs. Fig. 2.1 (page 50) is a schematic of a GaAs MESFET labelled with the names and dimensions of a GaAs MESFET. Fig. 2.2 shows the five main areas of interest when considering scaling. In the chapter, the physical layout of the device is described, and the terminology of its constituent parts. Physical effects governing the electrical characteristics are introduced, leading to the definition of the figures of merit and important parameters of MESFET electrical performance;

saturation current	gate-source capacitance
threshold voltage	carrier transit time
transconductance	effective carrier velocity
K-value	effective channel length
output conductance	unity gain cut-off frequency
voltage gain	subthreshold punch-through current

The effects of a short-channel on these parameters (both beneficial and detrimental) are discussed, and further insight is gained by reviewing the development of and results from FET models. The short-channel effects arising from the models are summarised, then the effects related to the technological aspects of scaling are reviewed. This involves consideration of the buffer layer and its interface with the active layer, high channel doping and free semiconductor surface near the channel.

Finally, the reported short gate-length FET performance at DC and high frequency are reviewed. Emphasis is on MESFETs, but as the best high frequency performance has been demonstrated by modulation-doped FETs (MODFETs), results from this class of device will be reviewed.

List of Symbols

a	epitaxial channel layer thickness	h_{21}	short-circuit current gain
α	coupling coefficient of ψ_b to V_g	I_d	drain current
A_V	voltage gain	$I_{d\,sat}$	saturated drain current
β	coupling coefficient of ψ_b to V_{ds}	$I_{d\,sub}$	subthreshold drain current
C_{gs}	gate-source depletion capacitance	I_{dss}	$I_{d\,sat}$ for $V_g = 0$
C_{gd}	gate-drain parasitic capacitance	$I_d^{barrier}$	subthreshold current over potential barrier
C_{gp}	parasitic gate pad capacitance	I_d^{diode}	subthreshold reverse gate current
C_{ds}	drain-source capacitance	I_g	gate current
C_{dp}	parasitic drain pad capacitance	I_s	source current
d	gate depletion thickness	I_{SC}	space-charge limited drain current
D	diffusion coefficient	$\mathbf{J}$	electron current density
ε	permittivity of GaAs	k_B	Boltzmann constant
$\mathbf{E}$	electric field	λ_D	Debye length
E	electric field strength	κ	differential shift of V_{Tsq} with V_{ds}
E_C	critical E for velocity saturation	L_g	metallurgical gate length
E_{CB}	energy of conduction band minimum	L	channel length
f	frequency	L_{eff}	effective channel length
f_{max}	maximum frequency of oscillation	μ	low field electron mobility
f_T	unity gain cut-off frequency	n	electron concentration
ϕ	Schottky barrier height	N_D	ionised donor concentration
g_d	output conductance	q	magnitude of the electron charge
g_m	transconductance	R	recombination rate
g_m'	extrinsic transconductance	R_d	drain series resistance
γ	geometric barrier lowering	R_g	gate resistance
h	channel height	R_{in}	intrinsic channel resistance
		R_s	source series resistance
		S_g	subthreshold gate swing
		T	temperature

τ	total carrier transit time through channel
τ_d	parasitic drain delay
τ_i	intrinsic transit time
τ_r	parasitic channel charging delay
U_T	thermal voltage = $k_B T/q$
v	electron velocity
v_{eff}	effective electron velocity
v_{sat}	saturated electron velocity
v_p	peak electron velocity
V_{Bi}	gate built-in voltage
V_d'	voltage at drain end of channel
V_{ds}	drain-source voltage
V_{ds}'	voltage drop across channel
V_{dsl}	limit of V_{ds} for saturated punch-through current
V_g	gate-source voltage
V_{plc}	long-channel pinch-off voltage
V_s	source voltage (common)
V_s'	voltage at source end of channel
V_T	threshold voltage
V_{T0}	V_{Tsq} as V_{ds} -> 0
V_{Tb}	barrier height defined V_T
V_{Tsq}	square-law threshold voltage
V_{Tlc}	long-channel V_T
V_{Tsc}	short-channel V_T
x	longitudinal co-ordinate
x_{vc},y_{vc}	subthreshold virtual cathode co-ordinates
y	transverse co-ordinate
ψ	electrostatic potential
ψ_b	subthreshold potential barrier height
ψ_{blc}	long-channel ψ_b
ψ_{bsc}	short-channel ψ_b
Z	channel width

NOTE.

Symbol definitions not listed above are given immediately below their first appearance in the text.

2.2 Development of the MESFET

The idea of controlling current in a semiconductor with an electric field imposed by a metal electrode was patented in the 1930s by Lilienfeld[3].

By the 1950s semiconductor technology was rapidly progressing, following, for example, the construction by Bardeen and Brattain of the first point-contact bipolar transistor in 1947[4]. Concurrently there was progress in processing techniques such as photolithography. GaAs was identified as a semiconductor only in 1952[5].

In 1952 Shockley presented a theory of the Unipolar "Field Effect" transistor[6]. He showed how the conductivity of a layer of semiconductor could be modulated by the application of a transverse electric field. He pointed out the advantages of the possibility of voltage gain and more efficient high frequency operation, compared to bipolar transistors of the same dimensions. He described a semiconductor device (later known as a Junction Field-Effect Transistor or JFET) in which electrical current flowing from one terminal (designated "source") to another (the "drain") is controlled by a voltage bias applied to a third terminal (the "gate"). The current is a result of majority carrier flow only, unlike the bipolar devices. The gate terminal is connected to p-n junctions sandwiching either side of a conducting channel from the source to the drain. The gate voltage can reverse-bias the junctions, creating space charge (depletion) regions in which the carrier concentration is negligible. Applying a sufficiently large reverse bias to the gate causes further extension of the depletion regions into the channel until the drain current is "pinched-off". The channel height, h is defined as the thickness of conducting channel between the depletion regions.

Prof. Mead of California Institute of Technology spent his Thanksgiving break fabricating the first GaAs MESFET[7]. In this planar device a rectifying metal-semiconductor (Schottky barrier) contact acted as the gate, on just one side of the n-type channel. The other side of the channel was a semi-insulating GaAs substrate. The interface between channel and substrate acted as a barrier to current flow (it actually produces a small depletion region), thus allowing the depletion region resulting from reverse biasing of the gate to pinch-off the drain current. Mead demonstrated that such a device actually worked as a FET.

Mead emphasised the advantage of the Schottky barrier gate over a p-n junction because of its very low reverse bias leakage current and its large barrier height. He noted that the metal-oxide-semiconductor (MOS) structure for a gate is not applicable in covalent semiconductors such as GaAs, where the Fermi level at the oxide-semiconductor interface is pinned at near mid-bandgap[8].

In 1967 the first microwave GaAs MESFET was reported[9] having a maximum frequency of oscillation, f_{max} of 3GHz. By 1970 a MESFET was reported with an f_{max} of 30GHz extrapolated from measurements performed at up to 17GHz[10,11].

2.3 MESFET Operation

Now the basic FET terminology has been given, examples of the electrical characteristics for a typical device fabricated in this work are presented, useful quantities and figures of merit are defined, and a simple model of device operation is developed.

2.3.1 DC Saturated Range

Current Saturation

The MESFET channel can be formed by epitaxial growth of a doped active layer on a semi-insulating substrate or by ion implantation. The former method gives a constant doping concentration throughout the active layer and was used for the devices in this work. The ion implantation process gives non-linear doping profiles which renders much of the following analysis unsuitable for such devices.

The current/voltage output characteristic of a MESFET are shown in Fig. 2.3a (page 52). By convention the source is grounded, $V_s = 0$. Each curve is measured at a fixed gate voltage, V_g. The action of a negative going change in V_g pinching-off the drain current, I_d can be clearly seen. Three ranges of operation are evident;

i) linear, open channel

ii) saturated, open channel

iii) pinched-off or subthreshold

The latter two ranges are important in microwave and logic applications of MESFETs, and will be discussed in this chapter.

The saturated values of the drain current are apparent for large values of source-drain voltage, V_{ds}. Drain current saturation in short channel FETs is the direct result of carrier drift velocity saturation. In the linear open channel range, the electron drift velocity, v increases proportionally with E for low fields, giving a uniform low field mobility, μ;

$$v = \mu E \tag{2.1}$$

The velocity saturates

$$v = v_{sat} \tag{2.2}$$

above a critical electric field strength, E_C. In GaAs $E_C \sim 3.5$ kV/cm and $v_{sat} \sim 10^7$cm/s. In small scale devices fields of this strength are easily accomplished. Before the velocity reaches the very high field value, it peaks (at v_p). The height of the peak is larger for lower doping concentration. The form of the velocity saturation with the peak, then velocity dropback (negative differential mobility) results from a redistribution of the electron population of the different conduction band valleys[12]. At low fields the majority of electrons are in the high μ (and high v_{sat}) central valley, but they are transferred into the low v_{sat} satellite valleys at field strengths above E_C.

The saturated velocity was observed in a short-channel Si JFET by Zuleeg[13] who measured the saturation current as a function of temperature and found the same temperature dependence as that of the limiting drift velocity. Winteler and Steinemann[14] also attributed current saturation to a saturated velocity in GaAs JFETs. Zuleeg assumed velocity saturation along the whole length of the channel and expressed the saturated drain current simply as

$$I_{d\,sat} = qN_D v_{sat} Zh + I_{SC} \tag{2.3}$$

with the addition of a space charge (depletion region) current, I_{SC} which is a linear function of V_{ds}. We can assume that in planar MESFET structures a similar current flows through the depletion region in the substrate and at its interface with the active layer. An often quoted value for a FET is I_{dss}, which is defined as the value of $I_{d\,sat}$ with $V_g = 0$.

Gate Depletion and Pinch-Off

The channel thickness is modulated by the Schottky barrier potential, ϕ which originates from the diode built-in potential, V_{Bi} (about 0.6V for Ti on GaAs) and the applied gate voltage, V_g. Assuming a flat depletion region under the gate, with the same length as the gate, for small values of V_{ds} the channel thickness can be obtained from the expression for the Schottky barrier potential (using the depletion approximation)

$$\phi = V_{Bi} - V_g = qN_D d^2 / 2\varepsilon \tag{2.4}$$

where $d = (a-h)$ is the gate depletion depth. The channel is pinched-off when $h = 0$ and

$$\phi \geq V_{plc} \tag{2.5}$$

where V_{plc} is the long-channel pinchoff voltage, given by

$$V_{plc} = qN_D a^2 / 2\varepsilon \tag{2.6}$$

Threshold Voltage

A long-channel threshold voltage can be defined

$$V_{Tlc} = V_{Bi} - V_{plc} \tag{2.7}$$

so that the pinch-off condition of equation 2.5 can be rewritten in terms of V_g as the subthreshold condition thus

$$V_g \leq V_{Tlc} \tag{2.8}$$

Equations 2.3, 2.4 and 2.6 lead to

$$I_{d\,sat} = qN_D v_{sat} Za[1 - (\phi/V_{plc})^{1/2}] + I_{SC} \tag{2.9}$$

The term $[1 - (\phi/V_{plc})^{1/2}]$ is the channel opening factor and $qN_D v_{sat} Za$ is the full channel saturated current.

Transconductance

A figure of merit for a FET is the the mutual transconductance,

$$g_m = \frac{\partial I_d}{\partial V_g}\bigg|_{V_{ds} = \text{const.}} \tag{2.10}$$

Fig. 2.3b (page 52) is presented as another example of a transfer characteristic as used in this work, showing g_m, which is just the slope of the I_d versus V_g curve.

In the current saturation range of operation, by differentiating equations 2.3 and 2.4 with respect to d, equation 2.10 leads to[15]

$$g_m = \varepsilon Z v_{sat} / d \tag{2.11}$$

This equation (together with equation 2.3 known as the velocity saturation model) is based on the 1-D assumption that the gate depletion region is unaffected by the not insignificant drain bias necessary for velocity saturation.

K-Value

In logic applications, a rapid switch between the on and the off state is valuable. This can be identified by a large rate of increase of channel conductance with gate bias as pinch-off gives way to the saturated open-channel range. Such behaviour can be characterised by the K-value, defined as

$$K = \frac{1}{2}\frac{\partial g_m}{\partial V_g} = \frac{1}{2}\frac{\partial^2 I_d}{\partial V_g^2} \tag{2.12}$$

over the linear part the g_m versus V_g curve, in the range between pinch-off and maximum g_m, before g_m saturates because of velocity saturation (equation 2.11) or g_m compression (see section 2.6.5 page 42).

Such a definition assumes[16]

$$g_m = 2K(V_g - V_T) \tag{2.13}$$

which comes from the Shockley model where the electron velocity is not saturated, and is equivalent to equation 2.52 (page 30) where $K = \beta_S$.

Parasitic Resistances

Consider the effect on the DC measurements of the series resistance of the semiconducting paths at the source, R_s and drain, R_d contacts. This

modifies the voltages at either end of the channel (with $V_s = 0$);

$$V_s' = I_d R_s \tag{2.14}$$

$$V_d' = V_{ds} - I_d R_d \tag{2.15}$$

and yields an extrinsic transconductance;

$$g_m' = g_m / [1 + g_m (R_s + R_d)] \tag{2.16}$$

The surface depletion between gate and source and drain contacts causes constriction of the channel thus increasing R_s and R_d. An obvious solution is a reduction of the source-gate and gate-drain gaps. The relative effect of R_s and R_d can be reduced by using a gate recess. The effect of surface states on these parasitic resistances are discussed further in section 2.6.5 on page 42.

R_s and R_d have a strong influence on the associated gain of a MESFET. The parasitic source resistance along with the gate resistance are the largest noise sources in GaAs FETs.

Gate Capacitance

The simple gate depletion region considered here can be treated as a parallel plate capacitor with a capacitance

$$C_{gs} = \varepsilon Z L_g / d \tag{2.17}$$

Output Conductance

An important limiting factor to FET performance is the slope of the saturated I_d versus V_{ds}, the output (or drain) conductance

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \Big|_{V_g = \text{const.}} \tag{2.18}$$

It can be seen that if g_d is constant, Zuleeg's space charge current becomes,

$$I_{SC} = g_d V_{ds} \tag{2.19}$$

Voltage Gain

The ratio of transconductance to output conductance defines another important figure of merit, the unloaded voltage gain

$$A_V = \frac{\partial V_{ds}}{\partial V_g} = \frac{g_m}{g_d} \tag{2.20}$$

Threshold Voltage Shift

Equation 2.9 indicates a square law relationship between $I_{d\ sat}$ and V_g. From the equation of a straight line on the graph with axes $I_d^{1/2}$ and V_g, with an intercept on the V_g axis of V_{Tsq}, which is the square-law threshold voltage,

$$V_{Tsq} = V_g - \frac{\partial V_g}{\partial (I_d^{1/2})} I_d^{1/2} \tag{2.21}$$

but

$$\frac{\partial (I_d^{1/2})}{\partial V_g} = \frac{1}{2I_d^{1/2}} \frac{\partial I_d}{\partial V_g} \tag{2.22}$$

therefore

$$V_{Tsq} = V_g - \frac{\partial V_g}{\partial I_d} 2I_d \tag{2.23}$$

this expression was used for the calculation of V_{Tsq} from the measured I_d and V_g data by programming it as a user function into an HP4145B Semiconductor Parameter Analyser.

Equation 2.3 (page 10) introduces a linear dependence of $I_{d\ sat}$ on V_{ds}. This can be expressed equivalently in terms of a threshold voltage shift with increasing V_d[17];

$$V_{Tsq} = V_{T0} + \kappa V_{ds} \tag{2.24}$$

where κ is the differential square law threshold voltage shift, which has negative values

$$\kappa = \frac{\partial V_{Tsq}}{\partial V_{ds}} \tag{2.25}$$

and V_{T0} is the threshold voltage for V_{ds} -> 0. In a long channel device, $V_{T0} = V_{Tlc}$, but with short-channel, the threshold voltage may be shifted more negative by the channel geometry (equation 2.34 page 19).

It has been suggested that this linear threshold voltage shift with V_{ds} originates from a space charge limited[18] (SCL) buffer current. This mechanism has been observed in short-channel MODFETs by Han *et al.*[19] where it was found to dominate both the output conductance and subthreshold current.

A simple model was proposed with $I_{SC} \propto V_{ds}/L_g^{1/2}$, and with carriers travelling from source to drain in the buffer layer at a saturated velocity. From equation 2.19 (page 13), this implies that $g_d \propto L_g^{-2}$ and Han *et al.* found a good fit of their data to this relationship for MODFETs with L_g = 300 to 900nm. Only a small change in g_d with temperature (30 to 170C) reinforced the explanation that an SCL mechanism was in operation. They observed the linear V_T shift with V_{ds} up to 2V. The model also predicted that the slope of this shift, $\kappa \propto L_g^{-2}$, and this was confirmed for devices in the range 300 to 700nm. The constant of proportionality in this relationship was a function of the thicknesses of the AlGaAs donor and channel space charge layers.

In this work, MESFETs with gate-lengths in the range 40 to 300nm display a linear shift of V_{Tsq} with V_{ds} up to ~ 2V, and the dependence of g_d and κ on L_g^{-2} is investigated in section 4.5.3 in order to determine if the same SCL current mechanism is acting in these devices.

Finally, a relationship between the differential square law threshold voltage shift and the voltage gain (equation 2.20) can be obtained by combining equations 2.23 and 2.25;

$$\kappa = - \frac{\partial V_g}{\partial V_{ds}} = - 1 / A_V \qquad (2.26)$$

2.3.2 DC Subthreshold Range

Punch-through

One significant short-channel effect is an inability to pinch-off the drain current above a limiting value of the drain bias, V_{dsl} (see Fig. 2.3a page 52). This saturated punch-through current has been observed in devices fabricated in this work. This phenomenon was observed by Patrick[20] who observed an exponential dependence of V_{dsl} over a range of gate lengths (55nm to 360nm),

$$V_{dsl} \propto \exp(L_g) \qquad (2.27)$$

Patrick suggested that this relationship might arise from a tunnelling current because of a very short effective channel length or from current injection in the buffer layer.

The publication of Patrick's results prompted an explanation by Smith[21] who had observed the same characteristic in GaAs MESFETs with the same L_g/a ratio as Patrick's shortest gate device but with a long gate-length of 1μm. This pointed to a triode mode of operation[22] of the subthreshold channel. It will be shown that this approach is consistent with the work of many others in studies of solid-state triodes, JFETs, MOSFETs, GaAs/AlGaAs and pseudomorphic MODFETs. This is the first study of MESFET subthreshold characteristics from the subthreshold barrier point of view.

At large drain bias, the drain electric field lines "punch-through" the channel to the source. Thus the saturated current flowing beyond V_{dsl} is punch-through current. This is not the only punch-through current arising from DIBL. In the subthreshold range, a very small punch-through current flows which is exponentially dependent on the drain bias.

Drain Induced Barrier Lowering

In the next sections, the phenomenon of Drain Induced Barrier Lowering (DIBL) will be presented as a major short-channel effect and as the mechanism of punch-through which is one of the most severe effects limiting performance of short-channel FETs.

Consider a symmetrical (with a gate on either side), short FET channel with the channel completely pinched-off (i.e. in the subthreshold range) by the *fixed* gate reverse bias. At $V_{ds} = 0$, there is a minimum of the potential between the source and drain, and the potential at this point, ψ_{min} can be regarded as a barrier of height $\psi_b = -\psi_{min}$. As a drain bias is raised ($V_{ds} > 0$), the barrier is lowered, as the drain field punches through towards the source. This effect is DIBL. Obviously the barrier height will also be affected by the gate bias. In a planar MESFET, one gate depletion region is replaced by the substrate depletion, but the mechanism described above still operates.

DIBL has three detrimental consequences, which will be described below.

1) An increase in subthreshold punch-through current as the barrier is lowered.

2) An eventual annihilation of the barrier as V_{ds} increases (at V_{dsl}), followed by an opening of the channel to allow saturated punch-through current flow.

3) A shift in the threshold voltage from the long-channel value in short-channel FETs, equivalent to an increased output conductance, g_d.

Subthreshold Potential Barrier

From linearity of the Laplacian operator in Poisson's equation (the principle of superposition), the height of the potential barrier, ψ_b is linearly coupled to both V_g and V_{ds}. The expression for the peak height of the barrier,

$$\psi_b = -\alpha V_g - \beta V_{ds} \tag{2.28}$$

was proposed by Brewer[23] in a study of subthreshold current in JFETs and later by Gupta[24] in a unified approach to the operation of field-effect, static induction[25] and analogue[26] transistors (FET, SIT and AT). The SIT and AT are solid-state equivalents of vacuum devices, whose operation resembles that of a pinched-off FET.

However, this linear coupling can only be an approximation, as the shape of the depletion region and position of the barrier are also functions of V_g and V_{ds}. In a MESFET (not vertically symmetrical), a change in V_g will move the position of the barrier in a complicated way; a decrease of V_g could be expected to raise the barrier and move the peak towards the substrate, but also towards the drain.

An expression for the peak barrier height more suitable for the non-symmetrical case of a MESFET was proposed by Pone *et al.*[27]

$$\psi_b = -f(V_g,V_T) - \beta V_{ds} \tag{2.29}$$

where $f(V_g,V_T)$ is a non-linear function. This expression was used to explain the behaviour of subthreshold current obtained from a Monte Carlo simulation of GaAs MESFETs. The simulation revealed the potential barrier in the channel, and its lowering with the increase in V_{ds}. The output characteristic showed the transition from pinch-off to an open channel at the drain voltage V_{dsl} corresponding to annihilation of the barrier. Equating the above expression for ψ_b to zero with $V_{ds} = V_{dsl}$ leads to

$$V_{dsl} = -f(V_g,V_T) / \beta \tag{2.30}$$

Pone *et al.* derived an approximate analytical model for the near-pinchoff MESFET, from a consideration of the potential induced by the drain and a gate with cylindrical fringing of its depletion region. They derived expressions for $f(V_g,V_T)$ and β. It was found that the expression for β contained a term 1 / exp(L_g). Combining this result with equation 2.30 immediately leads to $V_{dsl} \propto \exp(L_g)$ as found by Patrick (equation 2.27).

From the drift-diffusion current transport equation (equation 2.55 page 31), they arrived at an expression for subthreshold current identical to equation 2.36 below.

Source-Drain Barrier Lowering Induced Threshold Voltage Shift

First, the different definitions of the threshold voltage, V_T will be discussed. Next, the relationship between the subthreshold potential barrier height and the threshold voltage will be described.

The long-channel threshold voltage, V_{Tlc} was defined (equation 2.7 page 11) as the minimum gate voltage which results in complete pinch-off of the channel. For practical measurements V_T has been defined in many ways, for example:

i) V_{Tb} : the gate voltage yielding a constant (small) I_d. This corresponds to a constant subthreshold potential barrier height.

ii) a linear extrapolation of I_d below current saturation to zero in the transfer characteristic

iii) V_{Tsq} : a quadratic extrapolation of $I_{d\ sat}$ to zero in the transfer characteristic (defined in equation 2.21 page 14).

In the discussion of barrier induced threshold voltage shift that follows, the condition $V_g < V_{Tb}$ defines the subthreshold (pinched-off, barrier controlled) range of operation. The latter definition, V_{Tsq} will be used for the measurement of threshold voltages for determination of the voltage gain A_V from equations 2.25 and 2.26.

It is clear that the barrier lowering is less severe for a longer channel where the spatial separation between the drain and the source end of the channel reduces the influence of the drain. In fact, DIBL is highly channel length dependent. An expression for the subthreshold barrier height in a very long channel FET, where the drain has no influence over the barrier height near to the source, was given by Brewer as

$$\psi_{blc} = -(V_g - V_{Tlc}) = \phi - V_{plc} \qquad (2.31)$$

It is possible to express the subthreshold barrier height for a short-channel FET similarly, but in terms of a short-channel threshold voltage, V_{Tsc};

$$\psi_{bsc} = -(V_g - V_{Tsc}) \tag{2.32}$$

The aim of the next section is to obtain an expression for V_{Tsc}. Let us separate the two physical effects which lower the barrier at a fixed gate bias. The first is the linear coupling to V_{ds}, characterised by the parameter β. The second is a lowering by the effect of the geometry of the short channel. Fig. 2.4 (page 53) qualitatively shows the distinct nature of these two effects (after Troutman and Fortino[28]). Fig. 2.4a shows the potential distribution in a long channel, the barrier height (given by equation 2.31 above) is independent of V_{ds}. Fig. 2.4b shows the special case of the channel just at the limit of short channel behaviour, where the barrier height is linearly dependent on V_{ds}. Fig. 2.4c shows the very short-channel case, where the barrier is lowered even at $V_{ds} = 0$ by the small aspect ratio of the channel, yet it is still linearly dependent on V_{ds}. This discussion and Fig. 2.4 leads to

$$\psi_{bsc} = \phi - V_{plc} - \gamma - \beta V_{ds} \tag{2.33}$$

where γ is a function of the epitaxial channel aspect ratio L_g/a. γ being larger for a small L_g/a ratio, i.e. short-channel. This expression for ψ_b assumes (as does equation 2.28) that γ and β are independent. That is, a small change in one parameter, V_d or V_{ds} will not produce second order effects such as distortion of the position of the barrier and thus changing the coupling of ψ_b to the other parameter, V_{ds} or V_g respectively. This assumption is found to be invalid, as is demonstrated by the results in chapter 4.

Equation 2.33 is equivalent to that of Pone *et al.* (equation 2.29), if $f(V_g,V_T) = V_g - V_{Tlc} + \gamma$.

Now an expression for the short channel threshold voltage can be obtained by equating 2.32 and 2.33;

$$V_{Tsc} = V_{Tlc} - \gamma - \beta V_{ds} \tag{2.34}$$

This equation was found to fit measured data of short-channel MOSFETs by Troutman and Fortino. In this work, difficulty in obtaining uniform recess depths led to a large scatter in the threshold voltage shift, frustrating verification of this equation, and determination of γ from measured data.

Equation 2.34 is similar to equation 2.24 (page 14) with V_{Tlc} - γ replacing V_{T0} and -β replacing κ. Note, however, that V_{Tsc} is a threshold voltage defined using the barrier height and V_{Tsq} comes from a square law extrapolation. Indeed, when the expressions were combined with equation 2.27 (page 15) to obtain V_{dsl} from the measured V_{Tsq} data, the values of V_{dsl} yielded were incorrect in most cases (see equation 4.5 page 122).

These discussions lead to the conclusion that the barrier height and the threshold voltage are strongly affected by the channel aspect ratio through the dependence of the barrier lowering parameters γ and β. Furthermore, the dependence of V_{Tsc} on V_{ds} is expected to increase the output conductance, g_d in short-channel FETs.

Subthreshold Current

Subthreshold current flows when $V_g < V_T$. Subthreshold punch-through current caused by DIBL leads to a significant stand-by power dissipation in Si MOS[29] and GaAs digital circuits and is predicted to be the ultimate limit to MOSFET miniaturisation[30]. There are several mechanisms for sub-threshold current flow, which will be discussed below.

Barrier Controlled Subthreshold Current

The link between the barrier height and subthreshold current stems from the experimentally verified assumption that the drain current varies exponentially with the barrier height normalised to the thermal voltage, $U_T = k_B T/q$. This is believable, as the current injection over the barrier would be proportional to the carrier concentration, n_{vc} at the "virtual cathode" at the source side of the barrier with co-ordinates x_{vc} and y_{vc}. The electron quasi Fermi potential, $\psi_n = \psi - U_T \ln(n/n_i)$ is flat across the device when $V_{ds} = 0$, and when V_{ds} is increased an equilibrium is reached with

$$n_{vc} = N_D \exp(-\psi_b/U_T) \tag{2.35}$$

Thus the subthreshold drain current over the barrier (subthreshold punch-through current) is given by

$$I_d^{barrier} = I_0^{barrier} Z \exp(-\psi_b/U_T) \tag{2.36}$$

Where $I_0^{barrier}$ is the current per unit width over the barrier for low V_{ds} in a long channel FET with $V_g = V_{Tlc}$.

A useful measure of the strength of coupling of ψ_b to V_g is the sub-threshold swing[31] or gate swing

$$S_g = \frac{\partial V_g}{\partial \ln I_s} \tag{2.37}$$

where I_s is the source current. I_s is used because a sub-threshold measurement of I_d would include gate reverse leakage current I_g (given by equation 2.38 below) where $I_d = I_s + I_g$.

An expression for S_g in the short channel case could be obtained from equation 2.36 if the assumption is made that barrier controlled conduction dominates and $I_s = I_d^{barrier}$ in the sub-threshold range. However, the validity of such an expression is called into question in the short-channel case by the second order dependence of α or γ on V_{ds} in the chosen expression for ψ_b.

S_g can be measured directly from a subthreshold plot of $\ln I_s$ versus V_g. A small value of S_g indicates good control of the subthreshold current by the applied gate bias, and is therefore beneficial for reducing subthreshold leakage current.

The dominant role of the barrier controlled subthreshold current was reported in an investigation of subthreshold current in 120nm - 400nm gate-length conventional GaAs/AlGaAs and pseudomorphic GaInAs/AlGaAs MODFETs[32]. In a pseudomorphic MODFET, the lattice mismatch between the different layers produces a strain which increases the conduction band discontinuity.

In the study, I_s was measured for a range of drain biases and gate-lengths. The linear behaviour of $\ln I_s$ allowed measurement of the gate swing, S_g. S_g was found to depend strongly on L_g, being larger for short gate-lengths. S_g was similar in the conventional and pseudomorphic MODFETs for low V_{ds}, where the transverse position of the virtual cathode, y_{vc} was close to the plane of the 2-D electron gas (2-DEG) channel. However, at large V_{ds}, when y_{vc} was expected to be deep in the buffer, S_g was much less in the pseudomorphic device. This indicates that the pseudomorphic MODFET, with its larger potential barrier in the buffer, confines y_{vc} closer to the gate and reduces the subthreshold current and S_g.

It is expected that in a MESFET, the increased potential barrier afforded by an AlGaAs buffer (see section 2.6.2 page 38) should decrease S_g, thus improving subthreshold performance, as compared to a GaAs buffered device. This is confirmed in the subthreshold current measurements presented in section 4.5.2 (page 114).

Space Charge Limited Subthreshold Current

A space charge limited (SCL) mechanism was used to explain the subthreshold characteristics of MODFETs by Han *et al.* (see discussion of SCL threshold voltage shift on page 15). However, no direct evidence was presented to show that the subthreshold current arose from a SCL mechanism, it was only inferred because the threshold voltage shift was shown to be so. In the GaAs buffer devices of this thesis, a current distinct from DIBL controlled subthreshold current is observed, but a SCL controlled threshold voltage shift is not. Therefore in further discussions of this current it will merely be referred to as buffer leakage current, although similar behaviour in MODFETs has been ascribed to the SCL mechanism[32]. The subthreshold buffer leakage current observed in this thesis (section 4.5.2 page 114) current may well be space charge limited, but it has not been verified as such.

Gate Leakage Subthreshold Current

The reverse leakage of the gate Schottky barrier is another source of sub-threshold current and can be obtained from[33]

$$I_g = I_d^{\text{barrier}} = Zg_r V_r \exp(-V_r/U_T) \tag{2.38}$$

for reverse voltages applied across the diode, $V_r < 0$, where g_r is the diode reverse conductance per unit length. A typical value of I_g in the MESFETs fabricated in this work is 10^{-4} A/mm with V_g = -2.5V.

Other Subthreshold Current Mechanisms

A study of ion implanted MESFETs by Tan *et al.*[34] investigated the origin of sub-threshold current by measuring its temperature dependence and correlating the resultant activation energies to two possible current paths; ohmic leakage through the substrate and a current injected through the

depleted channel via empty EL(2) deep traps. The EL(2) donor level originates from an As vacancy and is responsible for the high resistivity of non-intentionally doped high purity GaAs[35].

Tan *et al.* found that the ohmic leakage mechanism dominated at room temperatures and above, and the trap conduction dominated below 0C. Room temperature ohmic leakage current was less than 10^{-7} A/mm, much less than the current levels measured in this work. In addition, all the measurements of Tan *et al.* were performed on 1μm gate-length FETs with V_{ds} = 1.0V, thus any effects of DIBL could not be investigated.

In the MBE grown GaAs channels used in this work, the EL(2) level is not present to the same extent as in the liquid encapsulated Czochralski (LEC) grown substrate (because of the optimised growth conditions). Therefore, neither the ohmic leakage nor the EL(2) trap current are considered to be the dominant subthreshold current mechanism in the MESFETs fabricated in this work.

2.3.3 Transit Time

Assuming the channel length L equals the gate-length, L_g, the intrinsic transit time of an electron passing through the channel with a saturated velocity is

$$\tau_i = L_g / v_{eff} \tag{2.39}$$

When $v_{eff} = v_{sat}$, this becomes (from equations 2.11 and 2.17)

$$\tau_i = C_{gs} / g_m \tag{2.40}$$

this equation also follows naturally from the differential definitions[36]; $\tau_i = \partial Q_{ch} / \partial I_d$, $C_{gs} = \partial Q_{ch} / \partial V_g$, $g_m = \partial I_d / \partial V_g$, where Q_{ch} is the active stored charge in the channel.

Short-Channel Effects

The spatial electric field and velocity distributions in a short-channel FET are not consistent with the simple model described above, as will be become apparent from discussion of the FET models later in this chapter. The geometry and position of the channel will not simply be a rectangular region of length L_g directly under the gate, as assumed in equation 2.12. In addition, the electron velocity may not be saturated along the whole length of

the channel leading to a lower average velocity than v_{sat}. The velocity has been predicted to reach higher values than v_{sat} because of "velocity overshoot".

For these reasons, an effective carrier velocity, v_{eff} and effective "working channel" length, L_{eff} can be defined[37] such that equation 2.39 can be replaced with a total transit time

$$\tau = L_{eff} / v_{eff} \tag{2.41}$$

where τ is the transit time through the working channel.

High-Frequency Measurements

The transit time can also be obtained from high frequency measurements of the S-parameters[38] (scattering parameters) of a FET, easily performed using an automatic network analyser. Consider the simple intrinsic MESFET two port equivalent circuit in Fig. 2.5 (page 54). The short circuit current gain is defined in terms of an hybrid-parameter (simply related to the S-parameters) as

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2 = V_{ds} = 0} \tag{2.42}$$

Unity Gain Cut-off Frequency

The transition or unity current gain cut-off frequency, f_T is defined as the frequency, f at which $|h_{21}| = 1$. Given that in the intrinsic case $i_1 = j2\pi f C_{gs} V_g$ and $i_2 = g_m V_g$,

$$|h_{21}| = g_m / 2\pi f C_{gs} \tag{2.43}$$

thus the intrinsic f_T is

$$f_{Ti} = g_m / 2\pi C_{gs} \tag{2.44}$$

Note that $|h_{21}|$ is inversely proportional to f, so a plot of $|h_{21}|$ (in dB) versus log f will roll-off at 20dB/decade i.e. 6dB/octave, until it falls to 0dB at f_{Ti}.

Inspection of equations 2.40 and 2.44 leads to

$$\tau_i = 1 / 2\pi f_{Ti} \tag{2.45}$$

and equivalently (from equation 2.39)

$$f_{Ti} = v_{sat} / 2\pi L_g \tag{2.46}$$

So, in the more realistic case, the measured, external unity gain cut-off frequency

$$f_T = v_{eff} / 2\pi L_{eff} \tag{2.47}$$

f_T is a valuable figure of merit, for it indicates the current gain at operating frequencies much lower than f_T.

In the analysis of the equivalent circuit above, the effect of parasitic elements were ignored. A more realistic extrinsic equivalent circuit is shown in Fig. 2.6a (page 55), with the physical origin of the circuit elements in Fig. 2.6b.

Another figure of merit is the maximum frequency of oscillation, f_{max} which takes into account losses associated with parasitic elements such as gate resistance, R_g, output conductance, g_d, and gate-drain feedback capacitance, C_{gd}. f_{max} can be measured by extrapolating the maximum available gain (MAG) or power gain to zero. f_{max} can be calculated from the extrinsic equivalent circuit as[39]

$$f_{max} = \frac{f_T}{\left[4\frac{g_d}{g_m}\left(g_m R_{in} + \frac{R_s+R_g}{1/g_m+R_s}\right) + \frac{4}{5}\frac{C_{gd}}{C_{gs}}\left(1+\frac{5}{2}\frac{C_{gd}}{C_{gs}}\right)(1+g_m R_s)^2\right]^{1/2}} \tag{2.48}$$

In a small scale FET, the most significant terms in this equation are R_g, $g_m/g_d = A_V$, and C_{gs}/C_{gd}. R_g increases rapidly as the gate-length is reduced, and will severely effect f_{max}. To a lesser extent, g_m/g_d and C_{gs}/C_{gd} are sensitive to scaling, with both g_d and C_{gd} increasing as the scale is reduced.

Parasitic Transit Delays

Equation 2.41 indicates that high frequency performance can be enhanced by reducing the channel length, L_{eff} and increasing the effective electron velocity v_{eff}.

It will be shown below that in the limit of short L_g, τ can become dominated by parasitic delays caused by the extension of the channel towards the drain (so increasing L_{eff}) and the finite charging time of the channel.

Compared to conventional GaAs/AlGaAs MODFETs, pseudomorphic MODFETs have shown superior values of f_T in submicron devices (see Table 2.1). A pseudomorphic MODFET has two main differences from the conventional MODFET:

a) The electron density in the 2-dimensional electron gas (2-DEG) channel is much higher, because of the larger conduction band discontinuity.

b) The 2-DEG channel is in GaInAs, where electrons are expected to have a higher v_{eff} than in GaAs.

Moll *et al.* studied conventional and pseudomorphic MODFETs[40] and found that the high f_T in the latter comes from the large electron density in the 2-DEG channel, and not from a great difference in v_{eff}. The large electron density allows faster charging of the channel because of the smaller intrinsic channel resistance (R_{in} in Fig. 2.6 page 55).

They argued that the average carrier velocity in conventional and pseudomorphic MODFETs was similar. As evidence they noted the similarity of f_T for long gate-length (1μm) devices and nearly identical velocities as calculated from g_m and V_T (which can yield v_{sat} in the special case of a pulsed-doped device). They used pulse-doping

to ensure negligible parallel conduction in the donor layer, which would confuse the results.

Moll *et al.* explained their measured data by breaking down the total transit time τ into several parts;

$$\tau = \tau_i + \tau_r + \tau_d \tag{2.49}$$

where;

τ_i is the intrinsic transit time, given by equation 2.39 page 23.

τ_r is the channel charging delay time and is the time constant of the charging of the channel capacitance through R_{in}.

τ_d is the drain delay, arising from the extension of the channel towards the drain with increasing drain bias. $\tau_d \sim (L_{eff} - L_g)/v_{eff}$.

These quantities, τ_i, τ_r and τ_d can be extracted from plots of τ versus V_{ds}' and τ versus Z / I_d (Figs. 2.7a and 2.7b) where $\tau = 1 / 2\pi f_T$ and the voltage drop across the channel $V_{ds}' = V_d' - V_s' = V_{ds} - I_d(R_s + R_d)$ (from equations 2.14 and 2.15 on page 13).

In the plot of τ versus V_{ds}' (Fig. 2.7a page 56), at the extrapolated point where V_{ds}' = 0, the channel extension towards the drain would vanish, along with τ_d. Therefore at this intercept, $\tau = \tau_i + \tau_r$. At each measurement point V_g should be adjusted to maximise f_T.

The plot of τ versus Z / I_d (Fig. 2.7b) can be used to extract τ_r because the current density in the channel is proportional to the drain current density, assuming a constant v_{eff} in the channel. At the intercept $Z / I_d = 0$, with an infinite current density R_{in} and therefore τ_r would be 0, so $\tau = \tau_i + \tau_d$.

τ_i and τ_r should contain all of the gate-length dependence of τ, so they should dominate in a long gate-length devices, with τ_d becoming more significant as the gate-length is reduced.

This analysis is used in chapter 4, to investigate the unusually large values of τ as measured from f_T in the sub-100nm gate-length MESFETs fabricated in this work.

2.4 FET Models

Models can offer an understanding of the physics of FET operation, and can yield predictions of FET characteristics. These features can aid device and material design. Several different approaches to FET modelling have been reported, that can be grouped together as either analytical models or 2-D numerical analyses. Many of the short-channel effects were first observed in the results of these models.

In each of the following sections, the aspects of the theories that have physical significance and aid in understanding the operation of MESFETs will be considered. Analytical expressions that are only used to mould a given model to fit measured characteristics will be omitted, however useful the model may be for practical device design. An exception will be made for SPICE models because of their widespread use in circuit modelling.

A comprehensive bibliography charting the development of analytical and 2-D numerical MESFET models and their use in interpreting experimental results is given by Shur[41].

2.4.1 Analytical FET Models

Shockley Model

Shockley gave the first description of FET operation[6]. He used a one-dimensional solution of Poisson's equation to deduce the thickness of the channel (equation 2.4 page 11). A further 1-D analysis related the channel thickness along the channel to the drain bias. It assumed that the bias of the gate junction and thus channel thickness only varies gradually from source to drain (the channel height decreasing linearly towards the drain). This is the "gradual channel" approximation.

Shockley's theory is unable to describe short-channel FETs for several reasons.

a) It assumes that the transverse electric field applied by the gate is smaller than and independent of the longitudinal field, E.

b) The gradual channel approximation is only valid for FETs with large channel length/height, L/h aspect ratios. In short-channel devices the shape of the depletion region is distorted away from the gate (see page 36) and is qualitatively shown in Fig. 2.2 (page 51). Many other consequences of the 2-dimensionality of the channel field cannot be predicted by the model.

c) In the Shockley model, current saturation is caused by pinch-off of the channel. The theory is not valid beyond pinch-off (either for decreasing V_g or increasing V_{ds}) because this would imply a non-gradual channel. Part of this deficiency is that it does not deal with carrier drift velocity saturation effects; the model assumes that the drift velocity is proportional to electric field. In the model, at the pinch-off point the channel height becomes zero, and the carrier velocity must become infinite to sustain the "saturated" value of drain current.

Further Development of the Shockley Model

Early developments of the Shockley model are covered in a detailed review by Yang[42]. The general improvements to the model were;

a) consideration of the shape of the JFET junction and its depletion region[43]. The treatment was just an extension of Shockley's model to non-parallel gate electrodes, with some discussion of velocity saturation. The diffused gate junction and therefore its depletion region were approximated as semicylindrical.

The transition from each depletion region to the conductive channel occurs over a finite distance. This distance is the smallest which can remain non-neutral, without causing a large potential difference. This condition is satisfied by the extrinsic Debye length, λ_D given by

$$\lambda_D^2 = \varepsilon U_T / qN_D \tag{2.50}$$

b) interpretation of current saturation as being the result of a finite channel width at the drain end of the gate[44,43,45,46]. However, this still left the models invalid for V_{ds} beyond current saturation.

c) the introduction of two[47,48] or three[49] regions in the channel, each region operating on a different portion of a simplified velocity/field relationship. This allowed the model to be valid for V_{ds} beyond current saturation.

These modifications to the Shockley model gave good agreement with measured data, particularly in long-channel FETs. However, the approach is still inadequate for short-channel FETs, as is discussed below, at the beginning of section 2.4.2.

SPICE Models

The models described so far can roughly predict device characteristics, but for practical device simulation a more flexible approach can be adopted. By leaving behind some physics and relying on a heuristic function whose parameters can be extracted from real device characteristics, fast compact models for circuit simulations can be derived. The resulting empirical models have no physical basis, except the functional form is in agreement with measured data.

Simulation Program for Integrated Circuit Emulation (SPICE) is widely used for the application suggested by its name. SPICE was originally developed at the University of California, Berkley[50] and was released into the public domain. The program initially supported only Si device models, but has gained GaAs JFET and MESFET models, also capacitance and temperature dependent models are included. The first SPICE MESFET model was developed by Curtice[51] and the drain characteristic is described

by;

$$I_d = I_{d\,sat}(1 + \lambda_S V_{ds}) \tanh(\alpha_S V_{ds}) \quad (2.51)$$

$$I_{d\,sat} = \beta_S (V_g - V_T)^2 \quad (2.52)$$

The hyperbolic tangent function was chosen purely because it resembles the real device characteristics and can easily be scaled. The initial linear slope is determined by α_S which represents the low field channel conductance. The saturated current is determined by the quadratic equation scaled by a gain, β_S. The factor λ_S introduces a linear output conductance. The square law behaviour of $I_{d\,sat}$ comes directly from Shockley's theory.

The model has been modified[52] for a cubic dependence of $I_{d\,sat}$ and more recently[53] a transition from square law to square root behaviour of $I_{d\,sat}$ with V_g has been achieved with an interpolation formula, giving a better fit to measured data. At the same time, the computationally intensive tanh function is replaced with a simple polynomial.

Other versions of SPICE have been developed and used for simulation of GaAs logic circuits[54,31]. These models have been modified in order accurately to predict MESFET behaviour over a range of operating conditions, for instance using DIBL to predict sub-threshold current.

2.4.2 2-D Numerical Analysis

All of the closed form analytical derivations of Shockley's theory only successfully predict long-channel device characteristics. In short-channel FETs, the assumption that the longitudinal and transverse fields are independent breaks down. Closed form 2-D solutions of Poisson's equation cannot be found for FET structures. It is impractical to incorporate physical information such as spatial and temporal variation of velocity and fields, position of shallow donor and deep level concentrations, precise device geometry and free surface state densities. Numerical analysis of FETs is based on computer solutions of simultaneous, non-linear partial differential equations which govern the carrier distribution in the semiconductor, with the application of the relevant boundary conditions.

Drift-Diffusion Models

The first application of numerical analysis to a FET by Kennedy and O'Brien[55] used the drift-diffusion approximation. For electrons the associated phenomenological semiconductor equations are

Poisson's Equation

$$\nabla.\mathbf{E} = \frac{q}{\varepsilon}(N_D - n) \tag{2.53}$$

$$\mathbf{E} = -\nabla\psi \tag{2.54}$$

current transport (drift-diffusion)

$$\mathbf{J} = qn\mu\mathbf{E} + qD\nabla n \tag{2.55}$$

current continuity

$$\frac{\partial n}{\partial t} = -\frac{1}{q}\nabla.\mathbf{J} - R \tag{2.56}$$

The approach was later applied to short-channel FETs. As well as confirmation of the strongly 2-D nature of the problem and that current saturation was caused by velocity saturation, useful physical results have emerged from simulations of long and short-channel FETs that were not apparent from the analytical approaches:

a) Kennedy and O'Brien found that velocity saturation (in Si, where unlike GaAs there is no velocity dropback with increasing electric field strength) and current continuity combine to produce regions of carrier accumulation and depletion (a domain) in the pinched-off part of the channel. In saturation, most of the drain voltage is dropped across this domain. This effect was found to redistribute the gate depletion region, and was most prominent in short-channel devices.

b) There is a significant current flowing through the substrate[56] giving rise to output conductance, g_d. At the active layer/substrate interface, carrier diffusion into the substrate generates an opposing electric field and equilibrium is reached. The transverse component of the 2-D channel field can overcome this diffusion field and force carriers into the substrate. This current is enhanced by punch-through of the drain field through the substrate towards the source[57], giving rise to large g_d. The punch-through can also

increase g_d in devices with no substrate. Obviously the punch-through is most significant for short-channel devices, as the spatial separation between drain and source is less.

c) An output conductance independent of substrate current can result from rotation of the saturated electron velocity vector towards the drain with increasing V_{ds}[58]. The velocity vector follows from the transverse and longitudinal components of the electric field from V_g and V_{ds} respectively.

d) As electrons enter the high (above E_C) longitudinal field under the gate, they transfer to the satellite valleys and their velocity drops back, so accumulation occurs in addition to velocity saturation. The accumulation is accompanied by a depletion nearer the drain where the field is lower and electrons accelerate away. The dipole field associated with the resulting domain further strengthens the longitudinal channel field so reinforcing the transfer effect.

Enhancement of the dipole field strength at large V_{ds}, in particular its transverse component, resulting in a widening of the saturated channel, has been suggested[59] as an explanation of large linear g_d in short-channel MESFETs. An earlier analytical model[60] had also emphasised the role of the domain in controlling saturation.

2-D numerical drift-diffusion models have predicted that the domain will cause negative output conductance in the drain current/voltage characteristic of a short-channel GaAs device at small V_{ds}[61,62,63]. This has been confirmed by observations of Gunn domains and Gunn oscillations in MESFETs[64,65,66]. However, this effect is supressed by substrate current[63], and high doping of the active layer.

e) Wada and Frey[62] concluded that the abruptness of the gate depletion region, and hence its capacitance, C_{gs}, are determined by the diffusivity which is anisotropic with respect to electric field. At the depletion edge their model gave n increasing as a cosine function rather than a step function.

They also found that pinch-off becomes softer because of punch-through of the drain field through the channel to the source. The punch-through is facilitated by the "shorting-out" of the high field domain in the channel by the substrate current.

Hot Electron Effects and Monte Carlo Simulations

A hot electron effect of considerable importance for FET performance is velocity overshoot[67]. When the energy relaxation time is larger than the momentum relaxation time, electrons in high fields accelerate to a high velocity before many scattering events have had time to occur. The equilibrium distribution is not reached and the average velocity may exceed the equilibrium values of saturation and even peak velocity. In GaAs, momentum relaxation, and therefore overshoot, are dominated by the scattering time into satellite valleys[68]. The possibility for overshoot of electrons accelerating in the central Γ valley is enhanced by the reduced efficiency of the dominant longitudinal polar optical phonon scattering mechanism as the electron energy rises above 0.1eV on its way to the 0.3eV needed for transfer to the L valley[69].

When time scale becomes much shorter than the momentum relaxation time, and no scattering events occur, the transport is described as ballistic[70]. The very short time scale of ballistic transport means that the average velocity may still be smaller than equilibrium values.

The standard drift-diffusion approximation is inadequate for describing hot electron effects such as velocity overshoot. It assumes that the electron distribution remains close to equilibrium. That is, electrons have the same temperature as the lattice, an instantaneous response to the electric field, and that the mobility and diffusion coefficients are functions only of the local electric field.

The drift-diffusion model has been modified by Shur[71] to take into account energy and momentum relaxation effects. In such models the drift-diffusion terms in equation 2.55 (page 31) are replaced with energy and momentum conservation equations derived from the Boltzmann transport equation[72]. The important parameters introduced in these equations, along with the electron energy and velocity, are energy and momentum relaxation times.

Shur's model predicted that velocity overshoot will increase v_{eff} as gate-length is reduced below 1μm. This results in an increase of f_T above the value expected from equation 2.47 (page 25). Shur also found that v_{eff} and f_T would be decreased in the (realistic) case of a non-uniform channel field, as the overshoot would only be achieved in a small part of the channel. Other

2-D hot electron models have been applied to sub-micron MESFETs. Curtice and Yun[73] found that overshoot increases g_m, f_T and I_{dss} ($I_{d\,sat}$ for $V_g = 0$) but has no effect on V_T and C_{gs}. Snowdon and Loret's hot-electron model[74] predicted a thicker channel at the drain end of the gate in comparison to a standard drift-diffusion model. The hot electrons travel further up the potential barrier at the top of the channel towards the gate. An explanation can be found by using Boltzmann statistics (in the high-energy tail of the Fermi distribution)

$$n = N_{CB} \exp[(E_F - E_{CB}) / k_B T_e] \tag{2.57}$$

where N_{CB} is the effective density of states in the conduction band, E_F is the Fermi level energy, E_{CB} is the energy of the bottom of the conduction band and T_e is the electron temperature. This equation tells us that as the electron temperature increases, the electron density also increases. At the source end of the channel, where the electron temperature is low, the channel is again thicker in the hot-electron model, with a larger current density. This was attributed to the large electron temperature gradient in this part of the channel. As the gate-length was reduced from 0.5 to 0.3μm the temperature gradient increased and the steepest part shifted towards the source. The increased carrier density arising from both of these mechanisms increases the drain current, leading to increased g_d and a negative shift in V_T. Thus Snowden and Loret concluded that velocity overshoot is not the only important hot-electron effect to be considered in short gate-length MESFET's.

Quasi 2-D hot-electron models have been developed, for example by Carnez *et al.*[75] and Snowdon and Pantoja[76] that assume a constant transverse field throughout the device, but keep the 2-dimensionality by using 2-D models for the geometry of the gate, surface and substrate depletion regions. The field dependence of the velocity is incorporated by using Monte Carlo calculated data. The quasi 2-D approach can yield a 3 orders of magnitude increase of simulation speed over full 2-D analyses, even including relaxation effects. The model of Carnez *et al.* demonstrated an increase in g_m and f_T when taking overshoot effects into account. The same model was later used to study the effect of high channel doping concentration[77] on short-channel effects. It was found that high channel doping accompanied by a reduction of channel thickness reduces detrimental effects such as V_T shift, and high g_d, while increasing the performance via g_m and f_T.

Monte Carlo simulation is a numerical method for solving the Boltzmann equation which offers a more complete consideration of scattering phenomena. The electron motion in k-space is simulated with periods of acceleration influenced by the electric field interrupted randomly by scattering processes with weighted probabilities. Monte Carlo simulation has been used to study bulk effects in GaAs, such as velocity saturation[78]. The Monte Carlo method has been applied to MESFETs with short channels. Maloney and Frey[79] and also Yoshii *et al.*[80] performed simulations predicting increased f_T arising from velocity overshoot. Awano *et al.*[81] predicted very high g_m and I_{dss}, at the cost of large g_d and poor pinch-off, with electrons travelling almost ballistically. Al-Mudares[82] predicted an increase in g_m and f_T caused by overshoot, however, substrate current was found to reduce overshoot, so the benefit of a reduction in gate length is eliminated.

One significant result from the Monte Carlo simulation of a FET is that transverse fields can reduce the low field mobility and saturation velocity of carriers in the channel[83,84]. In open channel FET operation, transverse fields occur near the gate depletion and buffer layer interface regions. Large transverse fields can also emerge from the positive ionised donors in the gate depletion region extension towards the drain[69]. This effect may lead to a suppression of velocity overshoot effects in FETs.

High active layer doping can also reduce the low field mobility of the channel because of the increased ionised impurity scattering. Because this scattering is elastic, the critical field for velocity saturation E_C remains constant, and the result of higher doping is a reduced peak velocity[85]. The saturation velocity at high fields is unchanged by doping because it is governed by deformation potential scattering and by energy loss to polar optical phonons in the L valleys. Another consequence of high doping related to the low field mobility degradation is a reduction in velocity overshoot[82].

The conclusions of the hot electron studies are;

a) Velocity overshoot in short-channel devices may result in higher effective velocities, shorter transit times, and therefore higher values of f_T.

b) An increasing electron temperature gradient with reduced channel-length enhances the current density, and therefore g_m.

c) Hot electrons can widen the channel by climbing the confining potential walls near both the gate and substrate interface. This current reduces g_m and increases g_d.

d) Transverse fields in the FET channel can degrade carrier transport by reducing low field mobility and saturation velocity, this may have a detrimental effect on velocity overshoot.

e) Highly doped, thin active layers can reduce V_T shift and g_d and increase g_m and f_T. However, high doping reduces the low field mobility, peak velocity and the influence of the velocity overshoot effect.

2.5 Summary of Short-Channel Effects

The important issues concerning short-channel devices can be summarised;

a) A dipole can form in the channel, caused by current crowding and velocity dropback. Most of the longitudinal field is dropped across this region. The high longitudinal field ensures velocity saturation in the channel. In a short-channel FET, substrate current shorts out the dipole, so giving a reduced longitudinal channel field strength.

b) Output conductance, g_d and a corresponding threshold voltage shift can arise from several mechanisms;

i) currents in the substrate and gate depletion region, enhanced by electron heating

ii) velocity vector rotation

iii) drain influence over the transverse dimension of the channel dipole.

c) Punch-through of the drain field at large V_{ds} is prominent in short-channels and can result in;

i) an increase in saturated channel current

ii) an increase in substrate current

iii) an increase in subthreshold current via DIBL

iv) soft pinchoff and threshold voltage shift

d) The channel geometry is modified by;

i) a larger potential difference between the gate and drain at the drain end of the gate for large V_{ds}, thus extending the depletion region towards the drain

ii) fringing of the transverse electric field at each end of the gate, resulting in increased C_{gs} and reduced V_T and g_m (thus also f_T)

iii) widening of the channel by hot-electrons which reduces g_m, increases g_d, and decreases V_T.

iv) the contribution of the surface potential near each end of the gate, being more significant in a shorter channel

v) the field of the dipole formed in the channel

vi) depletion edge transition is over a finite distance governed by the Debye length and diffusion. This results in a softer pinchoff and an increase of C_{gs}.

e) Velocity overshoot and an increased electron temperature gradient are predicted to increase performance via f_T in short-channel FETs. The large electron temperature gradient increases the current density in the channel, thus increasing g_m and reducing V_T.

f) The total electron transit time, τ can become dominated by channel charging delay, τ_r and drain delay, τ_d in a short-channel FET, thus reducing performance via f_T.

g) Transverse fields in the FET channel can degrade carrier transport by reducing low field mobility and saturation velocity, this may have a detrimental effect on velocity overshoot.

h) Highly doped, thin active layers can reduce detrimental short-channel effects and improve performance. However, high doping reduces the low field mobility, peak velocity and the influence of the velocity overshoot effect.

2.6 Technological Scaling Effects

2.6.1 Active/Buffer Layer Interface

The performance of the GaAs MESFET is limited by effects related to the interface between the active layer and the insulating buffer/substrate. The short-channel MESFET needs a buffer layer to prevent substrate conduction and provide a high quality active layer interface for low noise operation[86]. Phenomena which impair performance are;

a) A space charge limited buffer/substrate current leading to poor pinch-off characteristics, degraded transconductance, parasitic output conductance, increased RF noise figure and poor frequency response[87].

b) Deep level traps (impurities and defects centres) at the interface, originating in the semiinsulating substrate material[88] lead to premature output power saturation[89,90] and increased noise figure[91]. Scattering from these deep traps reduces the mobility near pinchoff[92]. The mobility degradation has also been attributed to enhanced compensation of donor atoms from the diffusion of Cr acceptors into the channel layer[93,94], reduced screening of ionised impurity scattering because of the reduced local carrier concentration[95,96], scattering from the steep channel walls[97], and in short channel FETs a non-uniform mobility degradation along the channel arising from variations in the electric field strength at the interface[98].

c) Backgating, where a voltage applied to the substrate or an adjacent contact pad modulates the drain current. There is a finite depletion region in the active layer at interface. This is caused by a negative charge accumulation at the interface arising from the deep traps (including EL(2)[94]) at the interface and in the substrate[99,100]. It is the width of the interface depletion layer which is modulated and decreases the width of the conducting channel. Backgating has adverse effects on the saturated channel dimensions and R_s and R_d which have a strong effect on the performance of GaAs circuits[101].

d) Hysteresis in the DC output characteristics, which is caused by field sensitive ionization centres, defects and traps at the interface[102].

2.6.2 AlGaAs Buffer Layers

Some of the above problems can be remedied by the introduction of a high resistivity GaAs buffer layer[102]. It was suggested by Barrera[103] that a heterojunction interface with an AlGaAs buffer layer under the n-GaAs active layer could provide better electron confinement.

An AlGaAs buffer reduces output conductance. The reduced electron diffusion into the buffer because of the large conduction band discontinuity at the GaAs/AlGaAs interface results in a large diffusion field confining carriers in the active layer. Also, the conduction band discontinuity (ΔE_{CB} ~ 0.24eV greater for a GaAs/$Al_{0.3}Ga_{0.7}As$ interface compared to a GaAs/GaAs interface) acts as a barrier to real space transfer of carriers into the buffer, which becomes apparent especially near pinch-off in short gate length devices.

In addition the electron saturation velocity in AlGaAs is lower than that in GaAs, thus further reducing the effect of carriers injected into the buffer. In the indirect band-gap region (for Al mole fractions greater than 0.45) the saturation velocity is reduced by a factor of more than 8. This is because of the higher effective masses in the X and L valleys and intervalley scattering. MBE grown AlGaAs also has a higher resistivity than GaAs and thus allows a higher source-drain breakdown voltage.

An improvement in g_m, g_d and pinchoff with an AlGaAs buffer has been predicted using 2-D drift-diffusion model[104] and Monte Carlo simulation[82]. The results of a further Monte Carlo simulation of the devices fabricated in this work are given in chapter 4. An AlGaAs buffer should also be expected to increase the K-value (equation 2.12 page 12), because of the better carrier confinement in the channel near pinch-off.

The first GaAs/AlGaAs heterojunction (AlGaAs buffer) MESFETs were fabricated on layers grown using metal-organic vapour phase epitaxy (MOVPE)[105], liquid phase epitaxy (LPE)[106] and metal-organic chemical vapour deposition (MOCVD)[107]. These devices showed improved control of hysteresis, backgating and carrier confinement.

High performance microwave MESFETs have been fabricated on MOCVD[108] and MOVPE[109] grown layers and the effect of the Al mole fraction on transconductance was studied on MOVPE layers[110] finding a peak in g_m for an $Al_{0.2}Ga_{0.8}As$ buffer.

Molecular beam epitaxy (MBE) is well suited to the growth of heterostructures because it allows precise control of doping, thickness and composition. However, the electrical properties and morphology of the MBE grown GaAs/AlGaAs interface (GaAs on AlGaAs) are strongly dependent on the substrate temperature during growth of the buffer[111,112] (because of the relatively small surface mobility of the Al species and incorporation of oxygen from background ambient species such as H_2O and CO). This was seen in subsequent MBE growth of AlGaAs buffer MESFETs[113,114,115] which showed reduced g_d compared to GaAs buffer MESFETs, and large g_m up to pinch-off.

A thin 20nm undoped GaAs smoothing layer grown between the AlGaAs buffer and n-GaAs active layer was found to reduce greatly the sensitivity of interface quality to growth temperature[116].

The growth control of MBE allowed a comparison of the microwave performance of MESFETs with a GaAs buffer and AlGaAs buffers with abrupt, alloy graded and (3 period) superlattice (SL) graded interfaces[117]. The work concluded that the SL graded buffer gave a slight improvement in the microwave performance of a 1μm gate-length device. The same devices showed a significant reduction in backgating[118] arising from a reduction of interface traps compared to the abrupt and graded alloy devices.

The GaAs/AlGaAs superlattice buffer has been used to improve on the poor quality of the inverse interface with GaAs grown on thick AlGaAs. The SL buffer was found to improve MBE grown quantum wells and inverted MODFET structures[119]. The SL buffer (12 periods of 50nm GaAs and 50nm $Al_{0.3}Ga_{0.7}As$) was applied to GaAs microwave device fabrication using MBE[120] and was compared with GaAs and AlGaAs bulk buffers. Material characterisation included DLTS and PL which revealed Fe (hole) and EL(2) (electron) traps in the active layer grown on the AlGaAs bulk buffer. These traps were found in less concentration in the active layer grown on the SL buffer.

Subsequently a study was made of persistent conductivity in MESFETs with a SL buffer[121] (100 periods of 3nm GaAs and 27nm $Al_{0.3}Ga_{0.7}As$, i.e. thin GaAs layers). The work concluded that carriers were de-trapping from deep levels in the AlGaAs structure under the influence of light and transverse electric fields. These effects have also been observed early in this work in MESFETs with a bulk $Al_{0.7}Ga_{0.3}As$ buffer. A study of surface morphology recovery of AlGaAs during MBE growth using reflection high-energy electron diffraction (RHEED) led to a scheme of growth interruptions (with a GaAs monolayer grown at each interruption) for improving the inverted GaAs/AlGaAs interface[122] in an inverted MODFET structure.

The MBE grown bulk AlGaAs buffer has continued to be used in MESFETs with devices reported with high unity gain cut-off frequency[123], very high transconductance[124] (with an $Al_{0.7}Ga_{0.3}As$ buffer) and with high performance as power devices[125].

Recently, a new MBE bulk GaAs buffer grown with a low substrate temperature (200C) has been reported[126]. This very high resistivity buffer totally eliminates backgating and increases the output resistance, isolation

breakdown voltage and source-drain breakdown voltage. The low temperature buffer has been shown to provide immunity to many of the backgating effects encountered in digital and analog GaAs circuits[127]. It has been used to make 0.2μm gate-length MESFETs immune to backgating with an f_T of 80GHz and g_m of 600mS/mm, and circuits with a 22GHz clock rate[128]. A low temperature AlInAs buffer has been used for fabrication of AlInAs/GaInAs pseudomorphic MODFETs displaying no backgating, g_m of 880mS/mm and very high voltage gain, A_V of 150[129].

2.6.3 p-GaAs Buffer Layers

A p-type GaAs buffer layer will yield a large conduction band discontinuity and therefore good carrier confinement. The lack of MBE growth problems compared to an AlGaAs buffer, and alternatively the ability to implant the p-layer in an ion-implanted process, make p-buffers a promising technology. However, in order to prevent hole conduction in the p-layer, it has to be made so thin that it is fully depleted, thus reducing the effective barrier height. Short-channel (100nm gate-length) MESFETs have been fabricated on MBE layers with a p-buffer[130]. However, the p-buffer led to a form of breakdown at large V_{ds} originating from a parasitic bipolar transistor action at the n-p active/buffer interface. Electron-hole pair generation arising from impact ionisation in the high field region of the channel was found to be responsible for this effect.

2.6.4 High Doping Effects

A thin, highly doped active layer is an important technological route to reducing short-channel effects. This allows a large length to height, *L/h* channel aspect ratio even for a short gate-length, because the gate depletion region is so much smaller. The channel aspect ratio should be large to avoid the short-channel effect of punch-through. The high doping also increases the channel conductivity and g_m in the saturation range. However, high doping reduces the low field mobility, peak velocity and the influence of the velocity overshoot effect (see section on Monte Carlo simulation in section 2.4.2 page 35).

A highly doped active layer will reduce the surface and interface depletion thickness (see Fig. 2.2 page 51), thus reducing R_s and R_d. Further reduction in R_s and R_d may come from lower resistance ohmic contacts to higher doped active layers.

The high doping approach has been validated by Daembkes *et al.*[77] and Lee *et al.*[124] through hot electron 2-D modelling and fabrication of MESFETs which had reduced short-channel effects and high g_m.

A recent paper proposed a modification of the *v/E* characteristic used previously in a development of the Shockley model[46] so that $v \propto N_D^{1/3}/(10^{19}\text{cm}^{-3})$. This simplistic approach was claimed to simulate the effect of overshoot, but it showed some correlation to the previous results of Daembkes *et al.* and Lee *et al.*

One problem of the high active layer doping is the reduction of the height and thickness of the gate Schottky diode barrier. The reduced barrier height, ϕ leads to an increased forward bias current and therefore a smaller usable voltage swing on the gate. In reverse bias the thin, low barrier allows a tunnelling current[131] (see equation 2.38 page 22) which is one of the main components of the sub-threshold leakage current. The Schottky barrier may also be lowered by field enhancement at the ends of the gate[132].

2.6.5 Surface Effects

The free semiconductor surfaces in FETs have a large effect on the charge control mechanism. The surface potential is strongly affected by Fermi level pinning by a large density of surface states. The surface potential is thus a function of the applied electrode potentials and the charging characteristics of the interface states.

Surface depletion increases R_s and R_d, particularly in a thin active layer, and the extrinsic g_m will therefore be reduced (equation 2.16 page 13). Consequently, the microwave performance may be degraded as the noise figure and associated gain are highly dependent on these parasitic elements.

The effect of the free surface charge modulation in a MESFET was considered by Chen and Wise[133]. They treated the free surface between gate and drain as a parasitic MESFET with an effective (surface) gate bias linearly related to the gate and drain biases. The Curtice model (equations 2.51 and 2.52 on page 30) was applied to the simple two FET circuit. Alternatively, a single expression comprised of equation 2.51 multiplied by an empirical function of V_g and V_T was used. They found that the effect of the parasitic FET becomes more significant when the gate potential, ϕ is close to zero and the depth of the surface depletion approaches or is larger than the gate depletion depth. This condition is easily satisfied in a

short-channel FET with a low V_{Bi} resulting from a high doping and high gate bias (approaching and above 0). The result is a compression of g_m under exactly the optimum operating conditions of a scaled MESFET.

The channel region in a short-channel MESFET extends beyond the gate, where hot electrons will be injected into the surface depletion as well as the buffer, thus a deep surface depletion will give a larger g_d. This argument reveals another benefit of high doping of the active layer, which produces a shallower surface depletion and gives a steeper confining potential barrier to hot electrons.

Such a barrier at the surface has been provided by a light p-type implant into the source-gate and gate-drain surface[134], resulting in a reduced g_d with no effect on V_T. However a detrimental consequence was increased parasitic access resistances R_s and R_d.

A 2-D hot-electron drift-diffusion model was used to study the effects of surface depletion on MESFET performance[135]. It was found that the surface depletion extended between the source and drain, the hot electrons and high field domain moved towards the drain, and carrier injection into the buffer layer was reduced because of the smoothing out of the longitudinal electric field in the channel.

Ladbrooke and Blight[136] constructed an analytical model to explain g_m dispersion in MESFETs in the frequency range up to a few tens of MHz. The model correlated well with measured g_m dispersion, with g_m falling to a constant value at frequencies higher than the characteristic charging frequency of the surface states. A gate recess was found to reduce g_m dispersion, as was a longer L_g as a proportion of the source-drain gap.

2.7 Short Gate-Length MESFETs

This section will review the reports of short gate-length (sub 0.5μm) MESFET fabrication and performance at DC and high frequency.

In 1982 Chao *et al.*[137] reported a comparison between 1.2μm and 0.2μm gate-length MESFETs. With reduced gate-length, they found typical short-channel effects; only a small increase in g_m, soft pinch-off, a negative V_T shift, and increased g_d near pinch-off.

Patrick *et al.*[20] brought the gate-length down to 55nm on a vapour phase epitaxy (VPE) grown layer, saw similar effects, and observed saturated punch-through current (see page 15).

Jaeckel *et al.*[138], made ion-implanted MESFETs with gate-lengths down to 100nm. They saw saturated punch-through current, no large increase in g_m, and a negative V_T shift. A linear scaling of C_{gs}[139] (measured from S-parameters from 1 to 4GHz), allowed them to calculate an f_{Ti} of 80Ghz for a 330nm device (from equation 2.44 page 24). A v_{sat} of 1.5×10^7cm/s (from equation 2.46) is about the same as bulk GaAs, so gave no evidence of velocity overshoot. The same group started using MBE grown structures for MESFET fabrication[140]. A thin (75nm), highly doped (9×10^{17}/cm^3) active layer was used on a fully depleted p-type GaAs buffer. 0.5μm gate-length devices showed a high g_m of 400mS/mm, a K-value of 580mS/Vmm[141,142] and an f_{Ti} of 105GHz.

Bernstein and Ferry fabricated MESFETs with gate-lengths down to 25nm on MBE grown layers[143,144] with a GaAs buffer. However, electrical characterisation was possible only for gate-lengths of 35nm and over. The active layer doping was 2.0×10^{17}/cm^3, its thickness was 180nm, and some gates were recessed to give an estimated channel thickness of 145nm. Therefore neither the channel doping nor the L/h ratio were at all optimised for short-channel operation. Consequently the devices showed very poor performance with a maximum g_m of 85mS/mm. The short-channel effect of punch-through was clearly visible. There was no possibility of useful high frequency operation, as the gate pad was on the active mesa and surrounded by (also not isolated from) the source, thus causing very large parasitic capacitances. The gate was fed by a long, thin, and therefore highly inductive wire. Bernstein and Ferry claimed to observe velocity overshoot. The only evidence presented was one 35nm device with a g_m of 105mS/mm, compared to around 70mS/mm for 45-70nm gate-lengths.

More evidence of overshoot was provided from the same group by Ryan *et al.*[145] by DC measurements of 30 to 75nm gate-length MESFETs with active layer doping of 2×10^{17} and 1.5×10^{18}/cm^3. However, the high frequency results were presented to show no evidence of overshoot.

Of all the g_m data presented, the highest value is 110mS/mm. In both the high and low doped channel devices, a fall in g_m is observed as L_g is reduced from 75 to 55nm, but from 40 to 30nm it rises to its maximum values. Values of v_{sat} were calculated from the saturation current and an

equation due to Hauser[43] similar to equation 2.9 (page 11), but with ϕ replaced by V_{ds} - V_g in the channel opening factor. This approach completely ignores the complex, two dimensional nature of the factors which shape the channel opening as the gate-length is reduced, for example the buffer layer current. However, the v_{sat} results agreed well with simple hot-electron computer simulations. They concluded that their DC results demonstrated that velocity overshoot was occurring, and furthermore, as the gate length was reduced beyond about 37nm, the near ballistic transport reduced the average velocity and therefore the effect of the overshoot.

The high frequency measurements of Ryan *et al.*, however, did not indicate that velocity overshoot was occurring. S-parameter measurements were performed on MESFETs with gate-lengths down to 37.5nm from 2 to 20GHz using an HP network analyser and Cascade Microtech on-wafer probes. No reference was made to calibration of the S-parameter measurements. f_T was measured by extrapolating $|h_{21}|$ *at less than* 6dB/octave, thus giving exaggerated values of f_T compared to using 6dB/octave roll-off. In fact, the graph showing the $|h_{21}|$ versus f has a line drawn on it labelled 6dB/octave, which is not a 6dB/octave line when measured using the scales provided. The observed roll-off of less than 6dB/octave is probably caused by parasitic capacitances or inductances[146]. Assuming that the devices of Ryan *et al.* are fabricated to the same design as Bernstein and Ferry's, as is indicated by from inspection of the electron micrographs presented, then the origin of such parasitics are obvious as discussed above.

On a plot of ln L_g versus ln f_T, a straight line was drawn through the best measured data. The slope of the line combined with equation 2.46 (page 25) yielded a v_{sat} of 8.6×10^6cm/s. Such a method of determining v_{sat} is in error on two counts;

1) because equation 2.43 implies that f_{Ti} must be extrapolated from a roll-off of $|h_{21}|$ at 6dB/octave, if the relationship 2.46 is valid, and

2) because the slope of the line was not 45° with the axes drawn to the same scale, as required by the inverse proportionality of f_{Ti} and L_g in equation 2.46.

Nevertheless, the devices showed high values of $|h_{21}|$ at the measurement frequencies, and for the 35nm gate-length device f_T obtained from $|h_{21}|$ extrapolated at 6dB/octave is still over 150GHz. Despite their

statement that the high frequency results did not reveal overshoot, Ryan *et al.* explained the relatively poor f_T values of the shortest gate-length by the same mechanism of near ballistic transport.

One can conclude from the work of Bernstein, Ferry, Ryan and co-workers that DC measurements of saturation current combined with a modified Shockley model can indicate velocity overshoot. However, in this work, no evidence of velocity overshoot has been found for similar devices, but with much larger transconductances. The analysis that Ryan *et al.* presented of the high frequency results is incorrect. In any case, the high frequency results do not indicate that velocity overshoot is a dominant carrier transport mechanism, which concurs with the results of this work.

These factors indicate that the overshoot reported at DC by Ryan *et al.* is an artefact of the assumptions made in the calculation of the velocity.

A more reliable way to extract the effective velocity is by analysis of high-frequency measurements as described in section 2.3.3. Optimisation of the device geometry to minimise parasitic inductances and capacitances is also essential for meaningful high frequency S-parameter measurements.

Short channel-effects (but not velocity overshoot) have been observed in other DC studies of short gate-length MESFETs.

MESFETs have been fabricated on highly doped active layers with an AlGaAs buffer, and have shown high g_m (600mS/mm, N_D = 6x10^{18}/cm^3, L_g = 100nm[123] and 700mS/mm, N_D = 3x10^{18}/cm^3, L_g = 170nm[124]), and good suppression of g_d.

The first sub-100nm gate-length MODFET results[147] were published along side 50 and 100nm MESFETs which exhibited short-channel effects of large g_d and saturated punch-through current.

A study of 90 - 640nm gate-length MESFETs[148] revealed constant g_m (consistent with the velocity saturation model, equation 2.11 page 12), large g_d, V_T shift, and an increase in I_{dss}, as L_g was reduced.

The best high-frequency MESFET results are included Table 2.1.

2.8 Short Gate-Length MODFETs

The best high frequency performance of short gate-length FETs have been demonstrated by modulation-doped FETs (MODFETs)[149]. Other names for this class of device are; selectively-doped heterostructure transistor (SDHT), high electron mobility transistor (HEMT), and perhaps the most accurate, 2-dimensional electron gas FET (2-DEGFET).

In a n-MODFET a large band-gap donor layer (e.g. AlGaAs) with some doping is epitaxially grown next to an undoped smaller band-gap channel (sometimes called buffer) layer (e.g. GaAs). Band-bending occurs because of the conduction band discontinuity ($\Delta E_{CB} \sim 0.2$eV), and a potential well is formed in the conduction band. Electrons from the donor layer are transferred into the well and a 2-dimensional electron gas (2-DEG) forms. This 2-DEG is used as the channel in an FET. Refinements can be made to the structure such as:

a) Leaving a thin, undoped, large bandgap spacer layer between the donors and the well, thus spatially separating the 2-DEG from the donors and increasing the 2-DEG mobility.

b) Increasing the depth of the potential well, and therefore the 2-DEG carrier concentration, by using a strained layer to increase the bandgap discontinuity. This can be achieved with a lattice mismatch between the donor and channel layers (e.g. with an AlGaAs donor layer and a GaInAs channel). The lattice mismatch gives rise to the name pseudomorphic MODFET for such devices. FET performance is improved by the higher carrier concentration[40] in the deeper well.

c) using an InP substrate to allow the growth of AlInAs/GaInAs structure without a significant lattice mismatch to the substrate. This permits fabrication of layers without any strain but a large bandgap discontinuity ($\Delta E_{CB} \sim 0.5$eV). A pseudomorphic structure with a lattice mismatch at the donor/channel layer interface can be achieved by increasing the In concentration in the structure. This scheme has yielded the best g_m and f_T results reported to date (see Table 2.1).

d) Putting another wide band-gap layer behind the buffer, thus creating a single quantum well (SQW), so confining the carriers closer to the gate. Further doping behind (and even inside) the well will increase the carrier sheet density in the well, and indeed several wells and donor layers can be stacked on top of each other to increase the total current capacity of the FET.

e) Decreasing the detrimental effects of parallel conduction through the donor layer by using delta doping, at the cost of higher access resistance (R_s and R_d) to the channel.

MODFETs have been fabricated with a gate-length of 20nm[150], using an electron beam induced resist technology to define the unrecessed gate. A peak in g_m was found with an L_g/a aspect ratio of 3 (L_g = 200nm). No V_T shift with reduced gate-length was observed.

MODFETs with gate-lengths down to 50nm have shown poor pinch-off[147] but high g_m (600mS/mm, L_g = 100nm). MODFETs with sub-100nm gates fabricated elsewhere[148] showed incomplete pinch-off and lower g_m (400mS/mm).

Most of the work on tenth micron gate-length MODFETs has involved high frequency characterisation of devices optimised for millimetre-wave performance. An important technological aspect of such devices is the reduction of the parasitic R_g by using a T-gate (or mushroom-gate) structure[151].

The best high-frequency MODFET results are included Table 2.1.

Table 2.1 Reported high frequency FET performance

MESFETs

active layer doping and thickness (cm^{-3},nm)	L_g nm	g_m mS/mm	f_T GHz	f_{max} GHz	$L_g 2\pi f_T$ 10^7 cm/s
GaAs BUFFER					
[152] 4.4×10^{17}, 240	250	260		120	
[153] 3×10^{18}, 120	200	1400*	105	100	1.3
# [154] $1\text{-}2\times10^{18}$, (ion-implanted)	250	444	120		1.9
[155] N/A, (ion-implanted)	250	510	126		2.0
[2] 4×10^{18}, 50	250	540	50		0.8
	40	680	150		0.4
[145] 1.5×10^{18}, 50	37.5	85	170		0.4
AlGaAs BUFFER					
[156] N/A, (ion-implanted)	500	410	47		1.5
GaInAs BUFFER					
[157] 2×10^{18}, 80	250	900 1460*	75	132	1.2

MODFETS

channel/donor layer	L_g nm	g_m mS/mm	f_T GHz	f_{max} GHz	$L_g 2\pi f_T$ 10^7 cm/s
GaAs SUBSTRATE					
LATTICE MATCHED (CONVENTIONAL)					
[151,158] $GaAs/AlGaAs_\delta$	100	700	113		0.7
STRAINED (PSEUDOMORPHIC)					
[159] $GaInAs/AlGaAs_\delta$	150	640	100	350	0.9
[160] $GaInAs/AlInAs_\delta$	120	585	117	125	0.9
[161] $GaInAs/AlGaAs_\delta$	100	900	150		0.9
[162] $GaInAs/AlGaAs_\delta$	80	920		270	
[163] $GaInAs/AlGaAs_\delta$	200	570	122		1.5
InP SUBSTRATE					
LATTICE MATCHED					
[164] GaInAs/AlInAs	300	650	80		1.5
[165] GaInAs/AlInAs	150	450	112		1.1
[166] GaInAs/AlInAs	100	1000	170		1.1
STRAINED (PSEUDOMORPHIC)					
[167] GaInAs/AlInAs	100	1160	210		1.3

NOTES.

* indicates an intrinsic value for g_m

# indicates a GaInAs channel, all other MESFETs listed having GaAs channels

The suffix "$_\delta$" represents delta doping (<10nm thick)

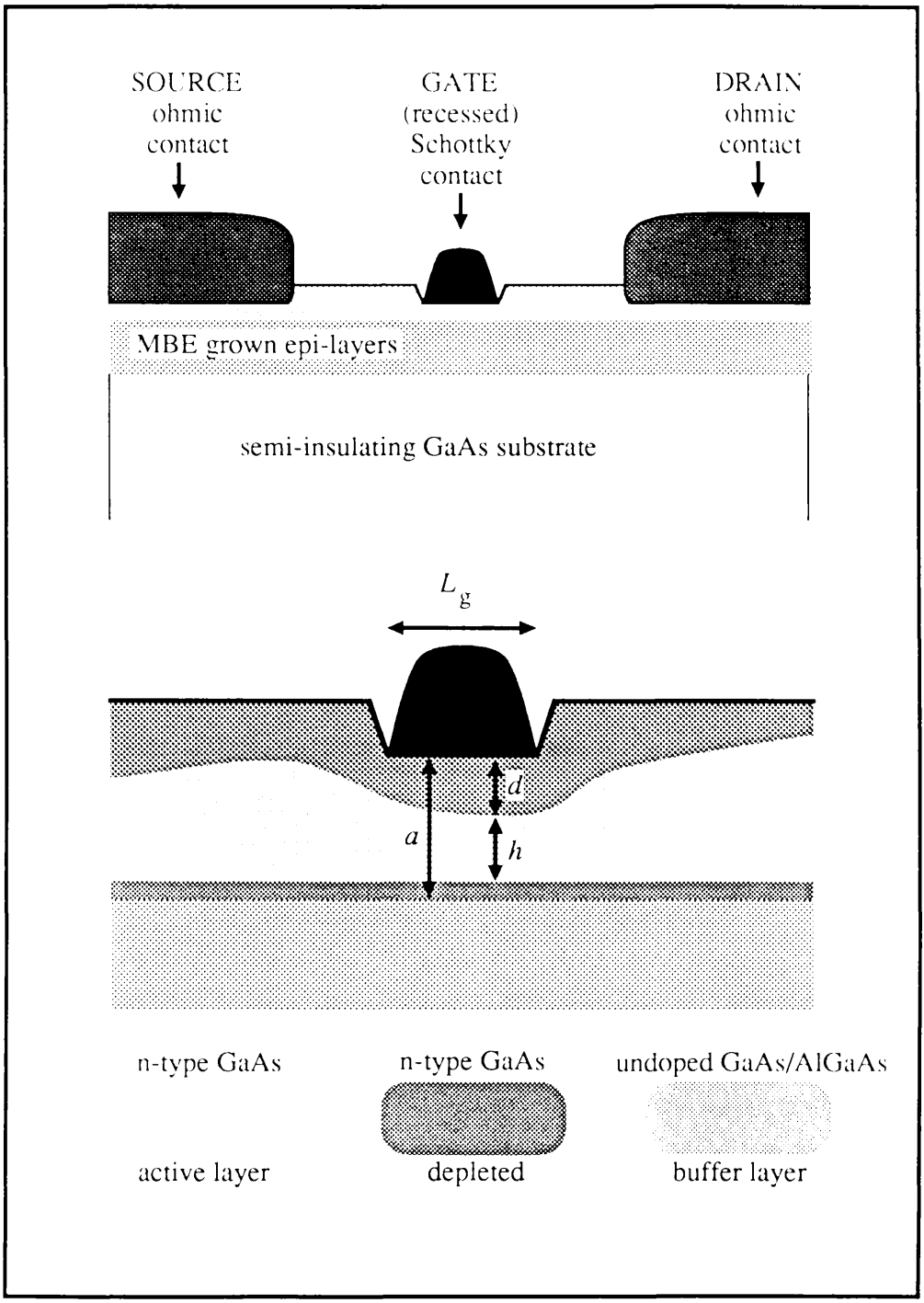


Figure 2.1 GaAs MESFET structure

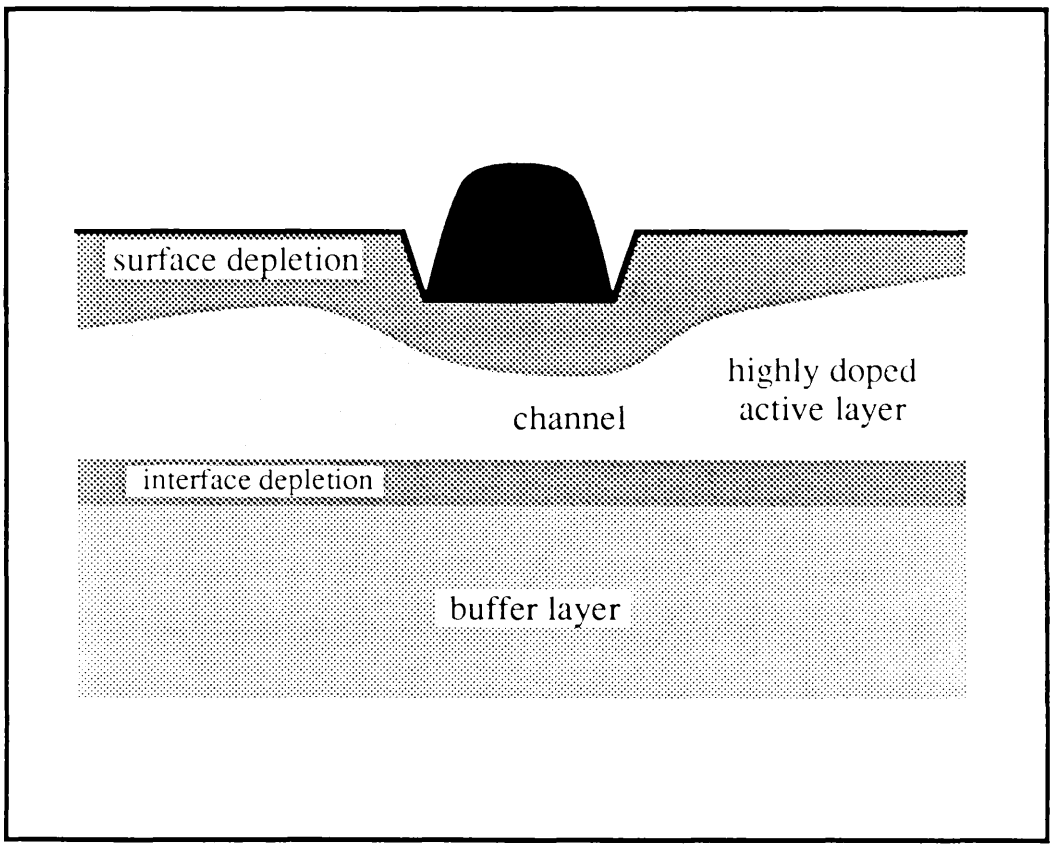


Figure 2.2 Regions of interest in a scaled GaAs MESFET

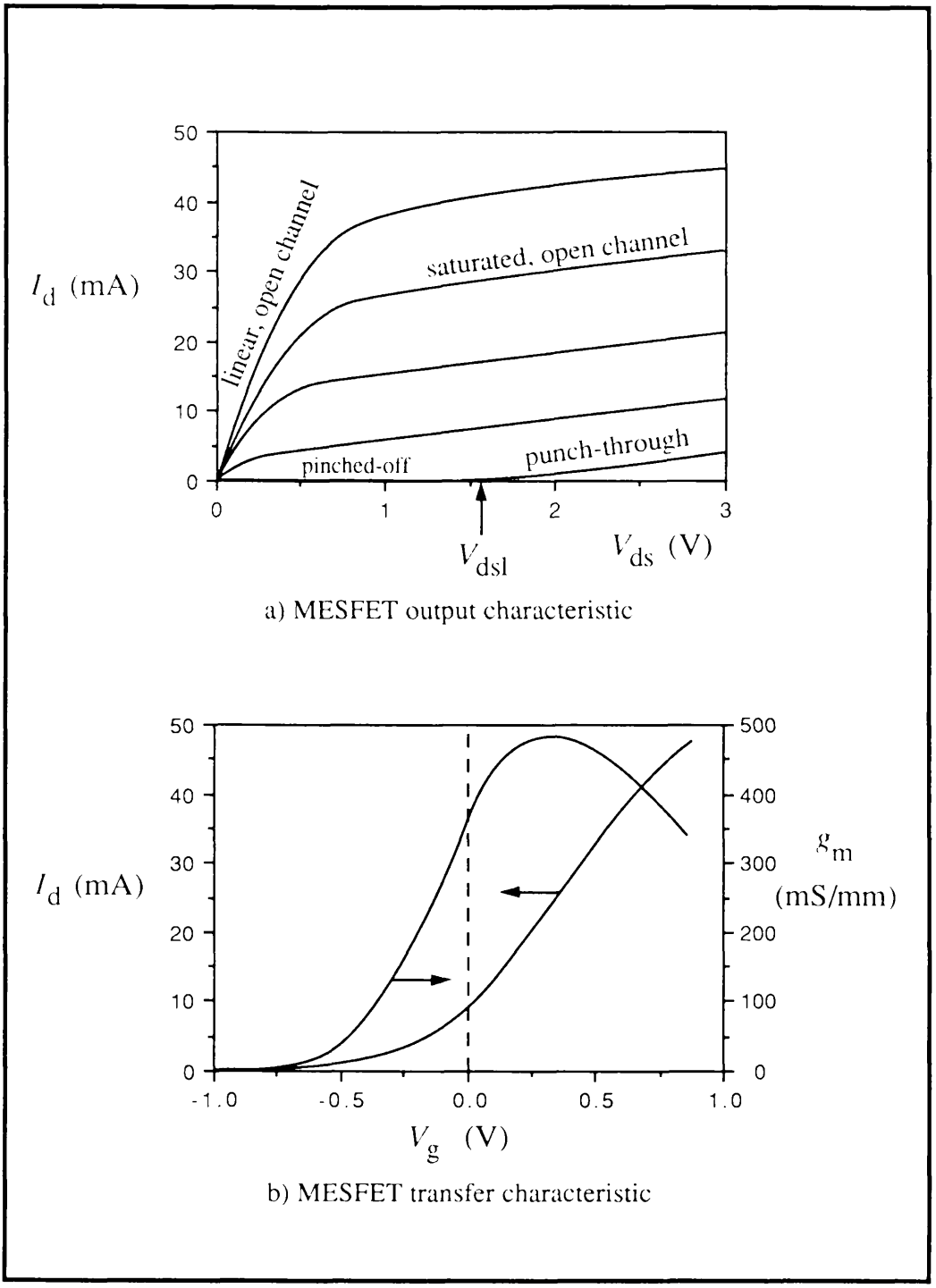


Figure 2.3 Example MESFET current/voltage characteristics

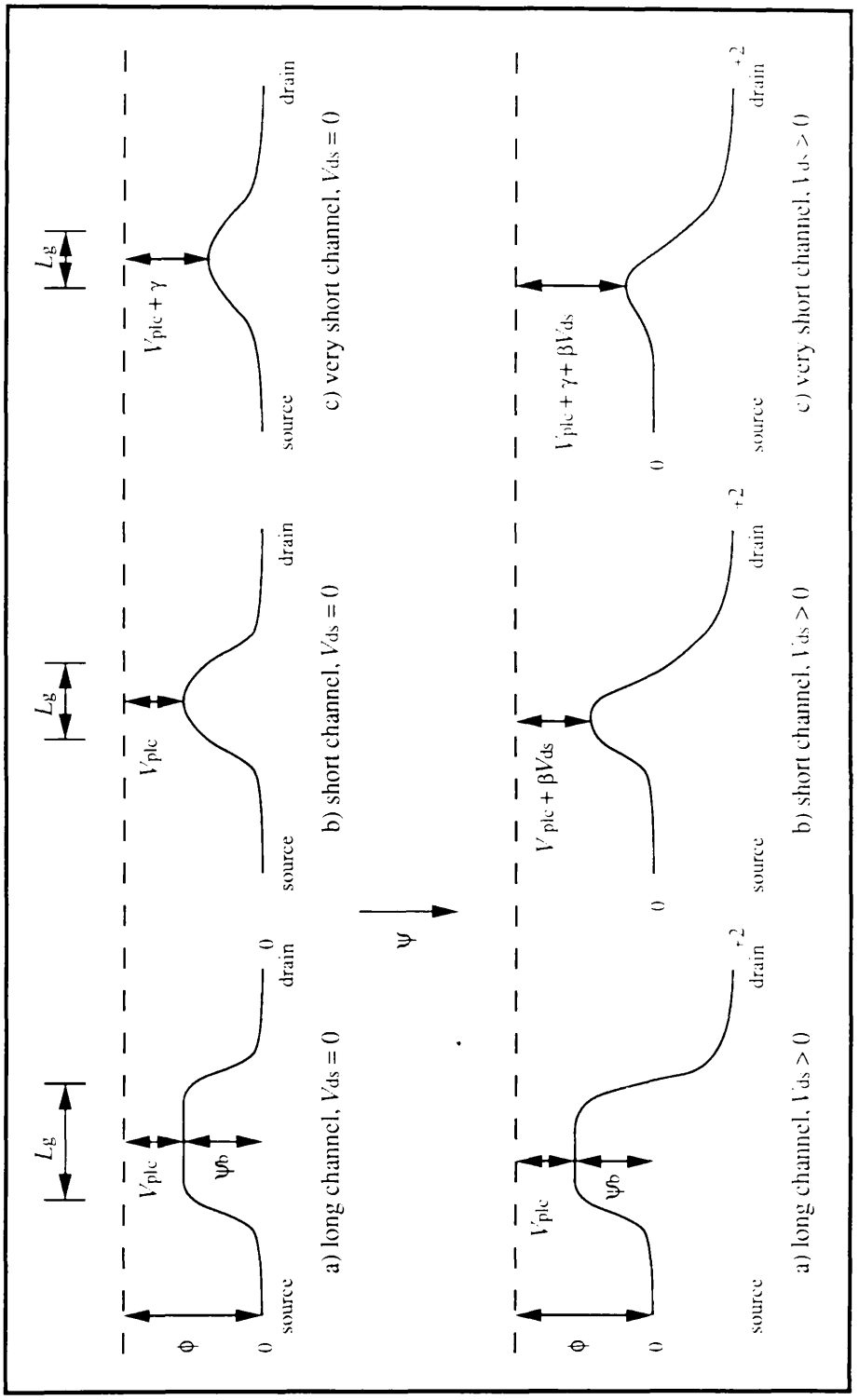


Figure 2.4 Subthreshold potential barrier lowering

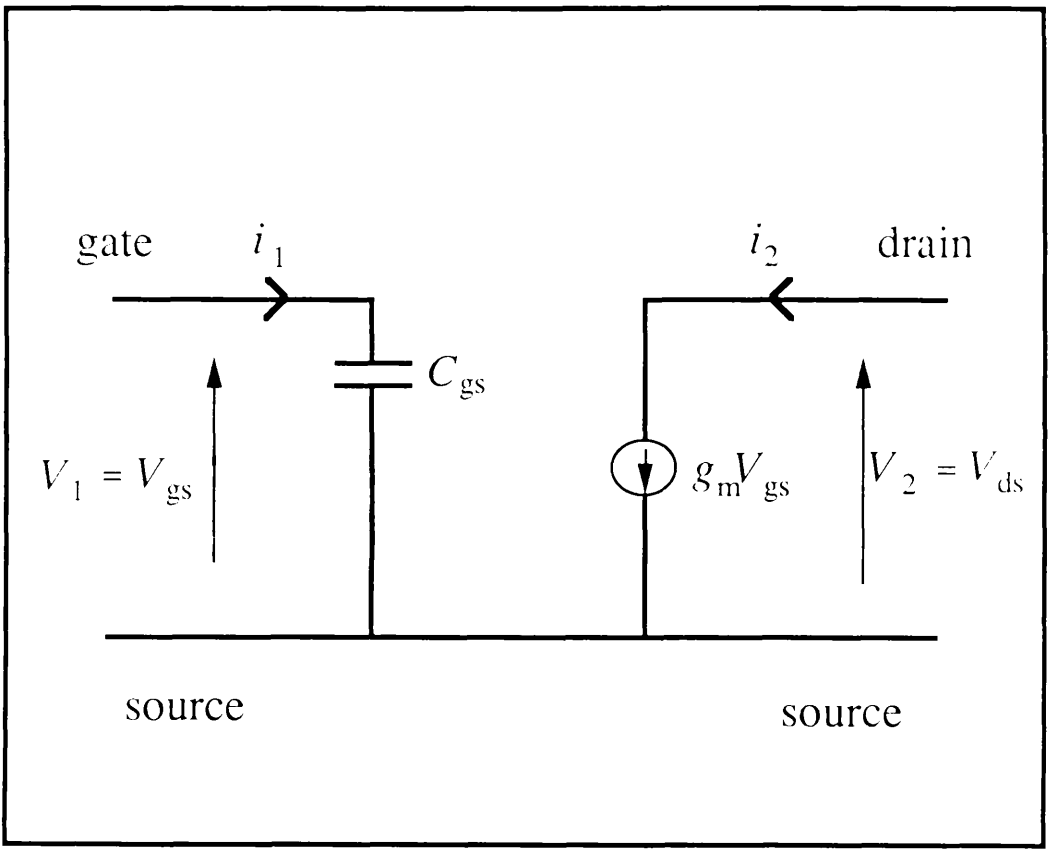
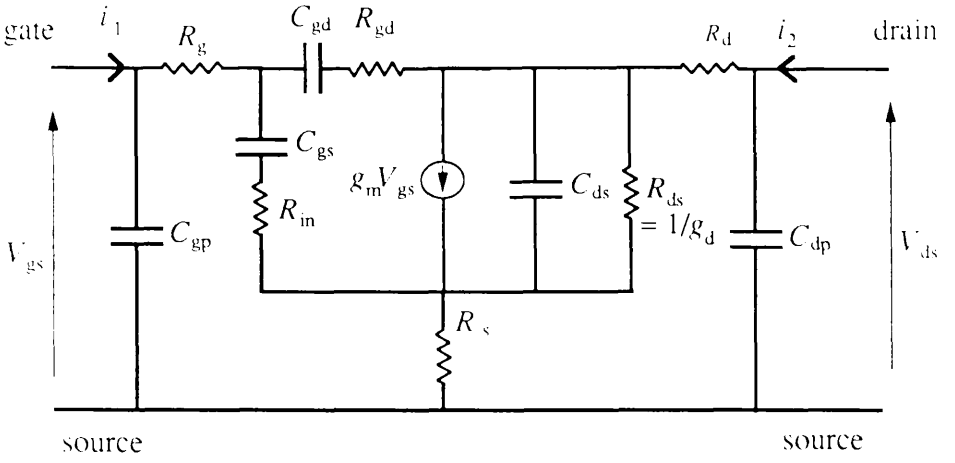
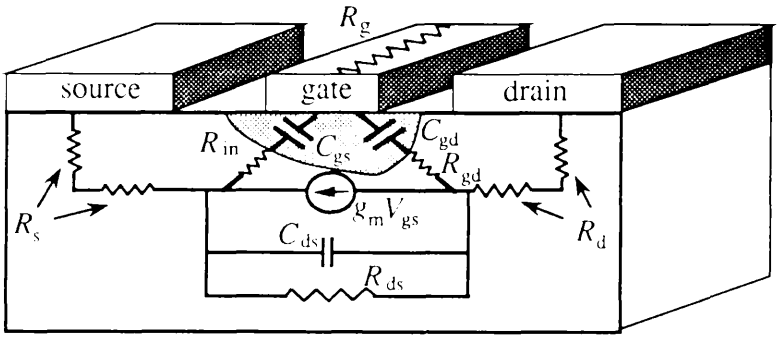


Figure 2.5 MESFET intrinsic equivalent circuit



a) Extrinsic equivalent circuit of a MESFET



b) Physical origin of equivalent circuit elements

Figure 2.6 MESFET extrinsic equivalent circuit

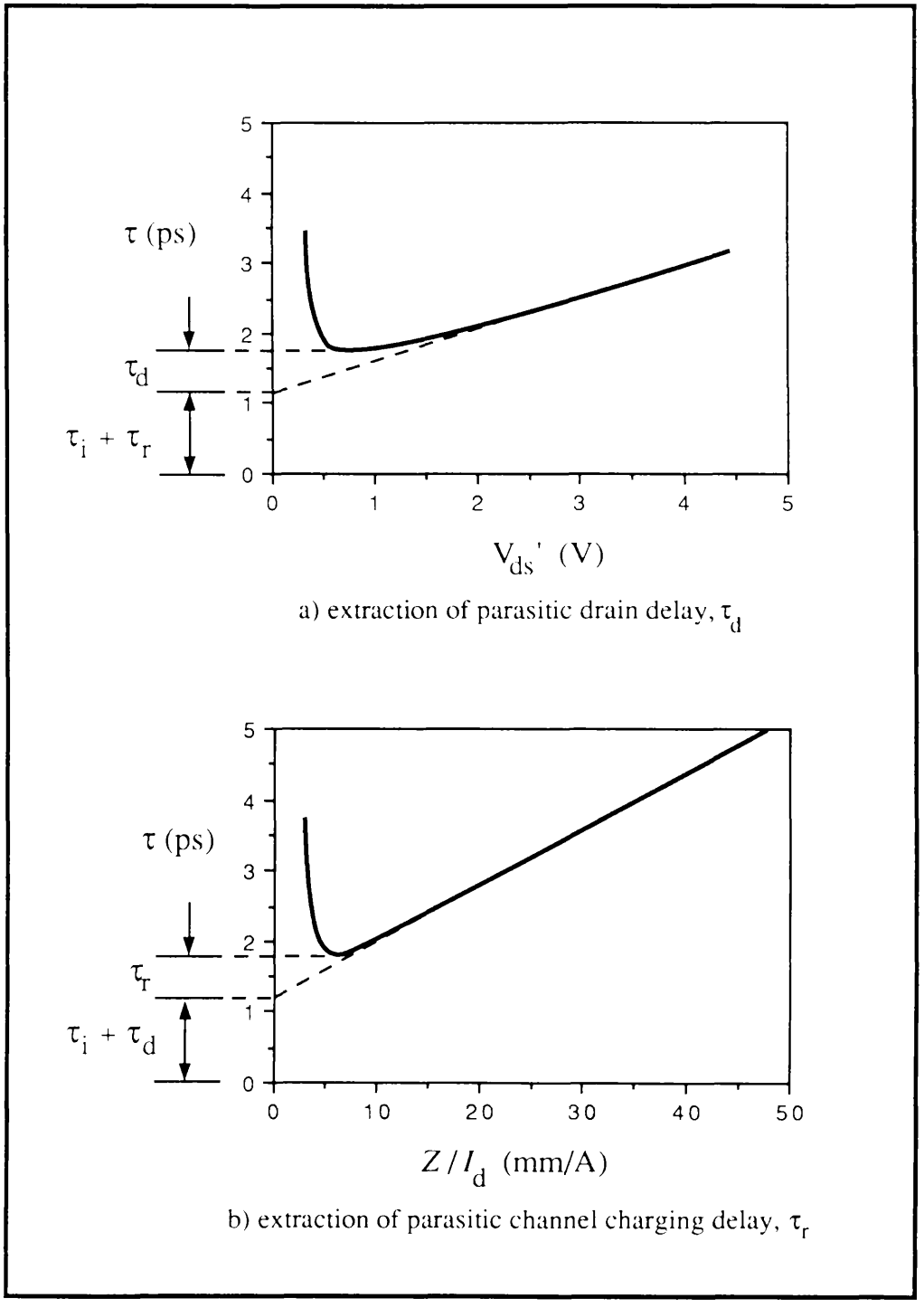


Figure 2.7 Extraction of intrinsic and parasitic transit delays

Chapter 3 - Design and Fabrication

3.1 Introduction

This chapter explains the design considerations and fabrication of very short gate-length GaAs MESFETs.

The design of the active layer and buffer layer are considered followed by discussion of the geometry and processing of each pattern level of the MESFET.

A description of the methods of electron beam lithography (EBL) is given, covering the electron beam sensitive resists and the electron beam writing system. The manual alignment method is described. Enhancements to the Electron Beam Scanning System (EBSS) software to facilitate the processing of large numbers of devices are detailed, including the automatic alignment and focusing procedures.

Finally, the process for fabrication of GaAs MESFET's. The complete sequence of fabrication is presented. The section starts with a description of wafer preparation and handling and goes through each level of the process in order, including resist preparation, exposure, development, metallisation and other steps specific to each level.

3.2 Material Design

3.2.1 Active Layer

The active layer is the main region for carrier transport in the MESFET and is therefore has a crucial effect on the device performance. In the devices of this work, carriers have to travel along the access region in active layer before and after reaching the channel, which is generally in the active layer also. The parameters over which we have control in the active layer are its

thickness and doping. Indirectly, precautions can be taken to ensure a good quality of the epitaxial active layer, by using an appropriate buffer underneath.

The active layer thickness and doping affect both the access regions and the channel, as was discussed in sections 2.6.4 (page 42) and section 2.6.5 on high doping and surface effects respectively. The discussions are summarised below.

The channel conductivity is increased but the carrier transport (low field mobility and velocity overshoot) is degraded by high doping. High doping reduces the parasitic series resistances R_s and R_d and so increases the extrinsic transconductance.

A large channel aspect ratio is beneficial for reducing short-channel effects. The aspect ratio is determined by the active layer thickness and doping, but extra control over thickness can be obtained by varying the gate recess.

The gate Schottky barrier is lowered and narrowed by high doping so increasing gate forward and reverse bias leakage currents.

A 50nm thick GaAs active layer, doped with Si to give $N_D = 3\text{x}10^{18}\text{cm}^{-3}$ had previously been used by Lee *et al.*[124] for fabrication of MESFETs with high transconductance and good suppression of short-channel effects with and AlGaAs buffer. Using the depletion approximation, the surface depletion depth as a function of N_D is given in Fig. 3.1 (page 91), assuming that mid-bandgap pinning of the Fermi level gives a 0.71V surface potential. Clearly, doping that gives N_D of over $2\text{x}10^{18}\text{cm}^{-3}$ allows an active layer thickness of 50nm with a majority of the channel undepleted.

These arguments led to the specification of an active layer 50nm thick doped with Si to $3\text{x}10^{18}\text{cm}^{-3}$.

3.2.2 Buffer Layer

The discussions of section 2.6.2 (page 38) and the results of Lee *et al.* led to the decision to use an $Al_xGa_{1-x}As$ buffer. An aluminium mole fraction, x of 0.3 was chosen.

The conduction band discontinuity at an interface between GaAs and $Al_xGa_{1-x}As$ reaches a peak at x = 0.45 which was therefore considered the upper limit for x for the buffer layer application. At values of x beyond 0.45, $Al_xGa_{1-x}As$ has an indirect band-gap and the discontinuity decreases with increasing x[168]. This is because the minimum energies of the X and L conduction band valleys do not rise as rapidly as for the Γ valley. The crossing point of the energies is at x = 0.45, above which the X valley conduction band energy is lowest. Because the layers were grown very soon after the commissioning of the Varian Gen II MBE machine, it was most convenient to select x = 0.3, which has more relaxed growth conditions over higher aluminium mole fractions. The GaAs/$Al_{0.3}Ga_{0.7}As$ interface has a conduction band discontinuity 0.24eV greater than the GaAs/GaAs case.

3.3 Device Geometry and Process Design

3.3.1 Alignment Marks

The alignment marks allow the accurate superimposition of successive pattern levels during the lithography stages of device fabrication.

The alignment mark pattern (Fig. 3.2a page 92) contained a set of marks for registration of the isolation and ohmic level alignment and another larger set for the pad level. The material name and site number lettering are included in the pattern file as @T (to be replaced with the string set by the Define Text command in the position file) and @P (replaced with the site number at each line in the position file) respectively. Thus "@T #@P" may actually be written on the chip as "A76.1 #45" for site number 45 when preceded by "DT A76.1" in the position file.

Another pattern was exposed at the top and bottom of the first column of device sites. This was the isolation test pattern, a legacy from wet etched mesa isolation. It had then been used as a check of the isolation current between two pads after mesa etching, but was retained in the dry etched mesa process simply as a large feature which allowed the chip orientation to be determined by eye.

The alignment mark metallisation was (from the substrate up) 10/70/20nm Ni/Au/Ni. The first Ni layer was for improving the adhesion of the metallisation. The Au layer provided a large secondary electron emission when scanned with an electron beam, thus giving good contrast for the

automatic alignment system. The final Ni layer was a cap which prevented sputtering of any exposed metal (the lettering) during the methane/hydrogen RIE of the mesa in the isolation level.

3.3.2 Isolation

The MESFET design included a reduced gate-width with shorter gate-length to compensate for the larger series gate resistance. This was achieved at the isolation level by using mesa widths (i.e. $Z/2$) of 10, 20, 40, 60, and 80μm for each group of 100 devices.

The isolation pattern (e.g. Fig. 3.2b page 92) contained a rectangle which defines the active region (mesa) of the device. The mesas were situated at the left hand side of the source-drain gap to give as small a gate resistance from the gate pad to the mesa as possible. Additional rectangles cover the alignment marks already on the chip to protect them from the mesa etch which was found to roughen the mark surface and interfere with the automatic alignment.

The active region was defined using a Metal On Polymer (MOP) mask[169] and dry etched mesa isolation. A 500nm Ge layer acted as a mask protecting the active region of the device from a methane/hydrogen Reactive Ion Etch (RIE) through the active layer. The Ge was deposited by lift-off on a 200nm layer of polyimide, which enabled removal of the mask after the etch (using boiling acetophenone). An oxygen RIE was used to remove the polyimide outwith the area of the mask immediately before the methane/hydrogen etch.

The Ge layer did not need to be 500nm thick to resist the etch, but such a layer had been previously found to be very rigid.

3.3.3 Ohmic Contacts

The function of the ohmic contacts is to provide a path for carriers from the external (e.g. measurement) circuitry into and out of the active layer. The contacts should have low series resistance up to the metal/semiconductor junction and a low resistance at the junction itself. The resistance should be constant as a function of applied voltage and current (i.e. obeying Ohm's Law).

The ohmic contact pattern (Fig. 3.2c page 92) consisted of three main features;

a) Source and drain contacts to the active layer. The series source and drain access resistances in the active layer were minimised by utilising a very small (0.7μm) source-drain spacing.

b) Tracks to connect the source and drain contacts to the subsequently defined probing pads, and a track connecting the gate to its pad.

c) Alignment marks for the gate level at both 1250x and 2500x magnification.

Additionally small stubs descending from the lower source contact were used for focusing at both gate level magnifications.

The $Au_{88}Ge_{12}$ eutectic has been found to give low resistance contacts to n-GaAs[170]. The metallisation used in this work is based upon a recipe optimised in this department by Patrick[171].

The ohmic metallisation was optimised for the layers used in this work by finding the metal composition with the lowest contact resistance. THis was done by annealing each composition at a range of temperatures and measuring the contact resistance using a simple transmission line model (TLM) method[172]. The EBL defined pattern for these TLM measurements consisted of five 200x100μm blocks with gaps between their long edges of 1, 2, 4 and 16μm. The resistance across the gaps was measured using an HP4145B semiconductor parameter analyser and a four point probe (two probes passing current, and two measuring voltage). On a graph of resistance versus pad separation, the intercept corresponding to zero separation gave a value of twice the contact resistance. The very large aspect ratio of the gaps allowed the fringing currents at each end to be ignored.

On each chip containing MESFETs, process control structures were used to confirm the successful annealing of the ohmic contacts and provide a more accurate measurement of the contact resistance, which eliminated current fringing at the ends of the gaps. Fig. 3.3 (page 93) is an electron micrograph of the TLM process control structure. The novel design of the contact pattern allowed a four point probe across each of the five gaps and therefore cancelled out the series resistance of the current paths between the measurement instrument and the active contacts. The mesa which defines the conducting region of the active layer can be seen in Fig. 3.3 as a feint

rectangle in the centre of the pattern. TLM measurements using these patterns confirms that very low contact resistances were being achieved on these highly doped active layers, with values typically less than 0.1Ωmm.

Fig. 3.4 (page 94) shows another process control structure which was used to confirm the reproducibility of the ohmic contact series resistance on each chip. The meander of ohmic contact metal had a resistance measured using a four point probe of about 90 to 100Ω after annealing.

3.3.4 Probing Pads

The probing pads were designed to be used with Cascade Microtech on-wafer microwave probes, which allow calibration of the S-parameter measurements up to the device under test. The probing pad pattern (Fig. 3.2d page 92) consists of source (top and bottom), drain (right) and gate (left) pads. The pads were configured as coplanar waveguides with a total width of 300μm, which is the separation of the on-wafer probe tips, which also use a coplanar waveguide (metal tracks on alumina) to give a 50Ω transmission line down to the device under test. The mark to space ratio of the tapered pads was calculated to give coplanar waveguide with a characteristic impedance, Z_0 of 50Ω. The central strip width (S) to gap (W) ratio, S/W was calculated numerically as 1.4 using the formula[173]

$$Z_0 = 30\pi \, [K(k') / K(k)] / [(\varepsilon_r + 1) / 2]^{1/2} \qquad (3.1)$$

where

$$k = S / (S + 2W) \qquad \text{and} \quad k' = (1-k^2)^{1/2} \qquad (3.2)$$

and $K(k)$ is the complete elliptic integral of the first kind. ε_r is the relative permittivity of GaAs, here assumed to be 13.1 and independent of frequency (it is actually slightly frequency dependent). The formula assumes ground planes (source pads) of semi-infinite extent, which is obviously not satisfied here, and this may decrease the accuracy of the calculated result.

The pad metallisation was relatively thick gold (300nm) to reduce series resistance from the probe tips to the ohmic contacts. A thin Ti layer was deposited first to improve adhesion.

3.3.5 Gate

The metal-semiconductor interface is the most important contact in the MESFET. The properties of the contact are largely determined by the metal used, with the Schottky barrier height and temperature stability being the main considerations. Aluminium has been used as a gate metal on GaAs, but problem have been found because of its incompatibility with gold (the "purple plague") and under certain circumstances its deformation by electromigration. Titanium has been shown to be a useful metal for this purpose[174], but it suffers from a large resistivity and a tendency to oxidise in air.

Therefore Ti was chosen as the metal in contact with the GaAs surface, because of the large Schottky diode barrier height it affords, and gold was chosen as the top layer to reduce the gate resistance and ensure good electrical contact by the subsequent wiring metallisation.

One problem found with the Ti/Au gate metallisation is a degradation of barrier height after heat treatment, because of diffusion of Au through the Ti and subsequent formation of Au containing compounds at the metal-semiconductor interface[175,176]. In this work, the 180C bake of the final wiring level was found to degrade MESFET performance by decreasing g_m and f_T, and increasing the gate forward bias leakage current. This problem was thereafter avoided by using a 120C bake for the wiring level resist. A more satisfactory solution would by the introduction of a platinum or palladium diffusion barrier in-between the Ti and Au metals, which has been shown to improve the temperature stability of such gate diodes[177].

A recessed gate structure was used to increase the extrinsic transconductance by decreasing the relative effect of the series source and drain access resistances[178].

The two main requirements for geometry of the gates in these MESFETs are conflicting with respect to the design. The gate-length should be short, yet the gate series resistance should be small. The thin resist which affords the high resolution for defining the shortest gates (less than 100nm gate-length) does not allow lift-off of more than 50nm thickness of metal, which leads to a large gate resistance. In this work the gates with lengths greater than 100nm were defined in a lower resolution resist which allows the lift-off of 150nm of metal.

Fig. 3.2e (page 92) shows the gate level pattern.

3.3.6 Wiring

The wiring level deposits an layer of metal on the area where the gate metal crosses onto the gate pad, where failure of step coverage has previously been found to massively increase the series gate resistance from high frequency measurements of MESFETs[179]. The step coverage is hindered by the undercut of the pad metal by the gate recess etch.

This level is also used to fill in the areas of the probing pads which were required to be left uncovered for the gate alignment marks. Another function of the pattern is to reinforce (i.e. reduce the series resistance of) the ohmic contact metallisation, particularly along the drain contact in-between the gates. The ohmic contact metal was necessarily thin because of the need for a thin resist at that level for defining the small source-drain gaps with high resolution. The wiring pattern is shown in Fig. 3.2f (page 92).

3.4 Electron Beam Lithography

Electron beam lithography (EBL) is a method of defining patterns on a substrate using a focused beam of electrons in a high vacuum system. The electrons are accelerated to a high energy and their impact changes the chemical and physical properties of a thin layer of resist on the substrate. The pattern is transferred by selectively removing the exposed (or unexposed) resist in a chemical development step.

EBL offers much higher resolution in the patterning of features than optical lithography which is currently the semiconductor industry's standard method. The resolution limit of EBL is in the order of 10nm, whereas that of optical lithography is in the order of 250nm. EBL allows a very rapid turnaround from pattern design to resist exposure, as no mask has to be fabricated.

However, EBL exposures are performed serially, one pixel (or block) at a time, whereas in optical lithography the exposure of all pattern features is performed in parallel over a relatively large field. The result is that even with very high exposure data rates (up to 300MHz has been used) and sensitive resists, EBL cannot compete with optical lithography in terms of exposure throughput.

For this work EBL is essential for the high resolution it affords. The fast design turnaround is a bonus.

3.4.1 Resists

In the context of EBL a resist is used as a medium for transferring a pattern onto a substrate by acting as a stencil for deposition or etching. A uniform layer of resist is deposited onto the substrate surface. The action of exposure by the electron beam allows the selective removal of either the exposed resist (in the case of a "positive" resist) or the unexposed resist (in the case of a "negative" resist).

PMMA

In this fabrication process all pattern transfer was achieved using a positive resist called poly(methyl methacrylate) (PMMA). PMMA is an organic polymer consisting of long chain molecules of $[CH_2CCH_3COOCH_3]_n$. PMMA of two average molecular weights was used:

85000 molecular weight (from BDH Chemicals Ltd.) and

350000 molecular weight ("Elvacite" from Dupont).

These resists are referred to in the text as "BDH" and "Elvacite".

Deposition

The PMMA was deposited onto the substrate as a thin film. This was achieved by dissolving the resist (supplied as a fine white powder) in a casting solvent then spin coating the substrate with the solution. The resist forms a uniform film and most of the solvent evaporates during spinning. The remaining solvent is driven out of the resist by baking at a temperature (180C), well above the glass transition point of the PMMA (118C).

The thickness of the film is determined by the viscosity of the solution (which depends on the concentration of the PMMA) and the rate of spin. In this work the solvent o-xylene is used for dissolving the PMMA in concentrations of 4% and 8% by weight of polymer. The exception is the probing pad resist where chlorobenzene is used to dissolve 15% by weight of polymer yielding a thicker layer than possible using o-xylene. O-xylene is a single isomer of xylene. It was found that using mixed isomer xylene yielded unreliable solubility and thickness of PMMA. The spin speed was 5000rpm, with the exception of the gate level where a thinner layer was obtained with a spin speed of 8000rpm.

Exposure

A high energy 50keV electron beam was directed onto the resist. This primary beam undergoes elastic collisions in the resist, which slightly spreads the beam, and in the substrate which causes backscattering into the resist over a distance of several microns[180]. Secondary electrons are generated whose inelastic collisions impart energy to the resist causing a scission of the polymer chains and a reduction of average molecular weight. The molecular weight after exposure reduces with increasing dose measured in charge or energy per unit area. This backscattered contribution to the exposure gives rise to the proximity effect in EBL[180], where the exposure at a point is equal to the sum of the exposure distributions from nearby points.

Bilayer Resists

An enhanced undercut profile has been achieved with a PMMA bilayer resist[181], which has been shown to be excellent for high resolution lithography[182,183]. This scheme uses two layers of PMMA with different sensitivities. Lithography and pattern transfer using a PMMA bilayer are shown graphically in Fig. 3.5 (page 95). The high sensitivity, low molecular weight PMMA is underneath a less sensitive high molecular weight layer. This lower layer responds to the laterally broader, lower dose part of the incident and backscattered beam. After development, an undercut profile is obtained.

There are several benefits of the bilayer resist.

1) The undercut profile facilitates subsequent pattern transfer by lift-off.

2) Over-development of the resist has little effect on the undercut profile, unlike the profile of a single layer which will be more severely affected. Thus the bilayer gives an increase in development latitude.

3) The top layer which defines the pattern is shielded from the substrate backscattered electrons by the lower layer. Therefore, another advantage of the bilayer can be a reduced proximity effect[184].

4) A bilayer resist allows use of exposures just above the critical dose for the top layer, which would not lead to a developed undercut in the absence of the more sensitive bottom layer. In this way higher resolution can be obtained with a bilayer.

Lift-off

Metal was deposited by evaporation onto the sample. The metal adhered to the substrate where the resist had been cleared by development and also to the remaining resist. The metal on top of the resist was unwanted and was dislodged by removing the underlying resist with a soak in acetone. This is called lift-off. The metal in the exposed area should be unaffected by lift-off, therefore there should be no physical connection between it and the metal on top of the resist. This can be ensured by restricting the thickness of the metal to less than about two thirds of the resist thickness and also by utilising the undercut profile obtained with a bilayer resist as described above.

Resist Characterisation

The two PMMA resists which were used for the bilayers in this process were each characterised by Binnie[185]. Further characterisation was therefore limited to exposure tests for each of the patterns used. This involved iteratively exposing and developing the patterns and changing the exposure doses at each iteration until the optimum exposure for lift-off and correct linewidth was achieved.

3.4.2 Electron Beam Writing System

The lithography in this project was performed with a Philips PSEM 500 scanning electron microscope (SEM). The machine has been modified for electron beam lithography as described by Mackie[184]. The PSEM 500 is a general purpose SEM with up to 50kV accelerating voltage, a beam diameter (spot size) variable from 1μm down to 8nm, and magnifications selectable from 20x up to 80000x. The magnification rather than field size is quoted below, this being a more natural parameter to the user of the electron beam lithography system. Secondary electrons are detected to form the image, although a transmitted electron detector is fitted. The machine has a eucentric stage which gives x and y motion in 1μm steps, as well as height (z), rotation, and tilt adjustment.

The modifications for EBL described by Mackie include:

a) external control of the beam deflection coils with Digital to Analogue Converters (DACs) being fed data from a digital pattern (scan) generator. The 12 bit resolution DACs give 2^{12} = 4096 pixel resolution in x and y across the exposure field,

b) external control of the beam blanking, and

c) a manual control of variable magnification (vari-mag.) to allow fine adjustment of each of the x and y magnification.

More recent modifications are the addition to the controlling computer system of:

a) hardware giving external automated control of the translational stage movement.

b) hardware to capture the secondary electron detector video (brightness) signal, which when synchronised with the clock of the scan generator allows the operation of automatic edge detection and alignment.

c) hardware giving external control of the focusing, leading to more reliable exposure of the finest features.

d) an IEEE-488 interface to a digital picoammeter for automatic electron beam current measurement.

Fig. 3.6 (page 96) shows schematically the current EBL system.

The external control functions have been provided by a succession of more powerful computers as they have become available. The single board microcomputer was replaced by a CP/M machine. The current system is an IBM PC compatible made by Olivetti. Improvements have been made in storage media from cassette tape to floppy then hard disks, and software development environments from machine code through successive versions of the Pascal language.

These advances have resulted in more sophisticated software for control of the EBL system and scan generator, larger patterns, and more generally, a greater ease of use and throughput of the EBL system.

Additionally, the pattern design software described by Mackie (DESIGN) has been re-written in Pascal to run on IBM PC compatibles and considerably enhanced in its capabilities. The pattern files produced with DESIGN can now be transferred directly via floppy disk to the EBL system controller.

The enhancements made to the EBL system controller software as part of this work are described in below.

3.4.3 Electron Beam Scanning Software (EBSS)

The electron beam scanning system (EBSS) is a computer program which controls the PSEM 500 electron beam writing system. The main function of the software is to direct pattern files to the scan generator of the EBL system. Functions have been added to control the repeated patterning (step and repeat) across an array of exposure sites (stage positions) and to align and focus automatically at each exposure site.

Patterns are transferred to the system as ASCII files containing numbers defining rectangle co-ordinates and special functions. The general format for the data is four integers separated by spaces, terminated by a carriage return.

The format for the simplest pattern element is

x1 y1 x2 y2

where each number is an integer in the range 1-4095 and the co-ordinate points x1, y1 and x2, y2 define the opposite corners of a rectangle in the field (x1 < x2 and y1 < y2). The general format for special functions is

0 D F D

where F is the integer defining the function and D are data related to that function. Special functions are available for:

F = 0	setting beam dwell time
F = 1	setting the exposure dose per unit area
F = 2	indicating a set of co-ordinates to define a trapezium pattern element
F = 4	repeating a group of pattern elements in an array
F = 6	scanning alphanumeric lettering
F = 8	repeatedly scanning one rectangle
F = 9	setting the automatic alignment parameters

F = 11-14 scanning rectangles with one co-ordinate adjusted as a function of stage position

F = 21-22 scanning rectangles with one dimension stretched as a function of stage position

The position file is terminated with the line

0 0 0 0

Data used for the step and repeat are held in (ASCII) position files with lines in the format

x y key exp @P

where x and y are integer stage co-ordinates (in microns) of the exposure site, key is a reference to a particular pattern file, exp is a percentage exposure dose change to the nominal pattern exposure doses, and @P is a string which may be written as text at the exposure site.

EBSS is controlled by entering two letter commands (e.g. EX for exit) from the keyboard. Commands are available to control loading and scanning of patterns, step and repeated stage movements, automatic alignment and focusing, and the entering of system constants such as magnification and measured beam current.

Groups of commands may be typed into ASCII files with their parameters and executed in batches, and may also be inserted into the position files.

Many of the features of EBSS including several of the special functions were added to the system as a part of this work, to enable patterning of the large number of devices required in this project. These additions are described in the following sections.

3.4.4 Enhancements to EBSS

This section describes the features added to EBSS which are directly relevant to this project. First, the new pattern elements introduced in addition to rectangles are described, then changes to the Step and Repeat procedure are documented.

The design for the probing pads called for trapezoidal pattern elements. These were included in pattern files as

0 0 2 0 (or 0 1 0 0)
x1 y1 x2 y2
x3 y3 x4 y4

where the points (x1,y1), (x2,y1), (x3,y4), and (x4,y4) defined the corners of a trapezium. The software used a straight line plotting algorithm to generate the end points of a set of rectangles which filled the trapezium.

In order to keep track of the large number of devices involved, it is helpful to label each device uniquely with the growth sequence number of the wafer, the chip sequence number, and the device number on that chip. EBSS was modified to recognise alphanumeric characters in pattern files, and scan these characters graphically in an exposure field. This was implemented in pattern files as

0 S 6 F text string
x1 y1 x2 y2

This causes the characters "text string" to be scanned with a position and in the field defined by the rectangle x1 y1 x2 y2. If S = 1 then the rectangle defines the size of the first character in the string. If S = 0 then the rectangle defines the boundaries of the whole text string. The F denotes which font is to be used (e.g. F = 1). Fonts are stored in files containing the bit map representations of all the characters available on the keyboard. A program was written to allow interactive editing and saving of these font files. Each character was defined on a 20 x 20 pixel grid.

Rather than create a new pattern file for each device with its unique label, a method of inserting other text sub-strings into the text string was provided. These sub-strings could come from two sources, replacing the special markers @P and @T which may appear as part of the main text string. The source of these sub-strings were:

@P from the current line in the position file (see above)

@T from an EBSS program variable set with the EBSS Define Text command

This system allowed one pattern file to contain a simple text string label such as "@T #@P" which for example could appear on the device as "A65.16 #24".

The procedure invoked by the EBSS Step and Repeat command was significantly modified. The logic of the procedure is

read and execute EBSS command lines from the position file
read a line from the position file containing
- new stage co-ordinates
- which pattern file to scan
- a percentage exposure change for the pattern
- some text to replace @P in pattern files

move the stage to the new co-ordinates
save a backup command batch file (if defined)
do automatic focus (if enabled)
do manual alignment (if enabled)
do automatic alignment (if enabled)
scan an overlay pattern (if defined)
scan the main pattern (exposure changed, text sub-strings inserted)
repeat until end of the position file or escape key pressed

The backup command file generated at each site defined the current EBSS status. In the event of a program crash, the backup command batch file could be executed with the EBSS GO command, thus restoring the program variables to their original state. The backup file name was defined with the EBSS Define Backup command. An overlay pattern was a normal pattern file which could be scanned at each exposure site, and was used where the same pattern features were wanted at every site. The overlay pattern file name was defined with the EBSS Define Overlay command.

3.4.5 Field Size and Spot Size

The PSEM 500 has a range of magnifications and spot sizes. Large features can be written using a low magnification/large field size and small features using a high magnification/small field size. With a small field size the exposure dose per unit area was increased for a given spot size, because the density of pixels is increased with the smaller separation of pixels generated by the fixed resolution scan generator DACs.

The range of spot sizes were accompanied by a range of different beam currents which result in a greater exposure charge dose to the resist. For a given exposure dose needed to develop the pattern the use of a larger spot size meant a reduced overall pattern exposure time. At lower magnification,

the large frame size led to a larger distance between each pixel. If too small a spot size were chosen, the individual pixels were found to develop out, especially at the edge of pattern features. If too large a spot size were chosen the very small dwell time on each pixel could produce a similar effect. To avoid these rough edges around features, and long pattern exposure times, the spot size was generally chosen to be slightly less than the pixel separation.

The field size was chosen such that the pattern spanned the entire field, allowing the full 4096x4096 pixel resolution of the field to be used. Table 3.1 below gives the field magnifications and corresponding field sizes use in this work.

Table 3.1 Magnifications and field sizes

Magnification	Field Size (μmxμm)
320	390x300
640	195x145
1250	100x75
2500	50x40

3.4.6 Manual Alignment

Accurate alignment (superposition) of successive pattern levels was essential for the fabrication of MESFETs. Manual alignment was achieved by scanning an raster pattern (alignment detection pattern) with a low exposure dose over some metal alignment marks on the substrate. The difference in secondary electron generation efficiency between the marks and the substrate led to an observed brightness difference. This brightness difference (contrast) could be maximised by adjusting the gain and black level controls of the SEM secondary electron detector. Adjustment of the SEM video display monitor brightness and monitor contrast was also possible. The limiting effect on the contrast for exposures using the smallest spot sizes was the low signal to noise ratio resulting from the small beam current. This was only a problem when using the 8nm spot size, but alignment could still be performed if the SEM electron source emission current was increased, yielding a higher beam current.

A reduction in the contrast was also caused by the resist coating the sample, but fortunately the thicker resists used in this work were used for levels exposed at low magnification with a large spot size.

Increasing the exposure dose of the alignment detection patterns would have increased the contrast, but it was kept as low as possible to avoid inadvertently exposing the resist covering the actual device pattern area.

The alignment detection patterns were designed so that an unambiguous contrast pattern was visible when the exposure field was superimposed correctly with respect to translation, rotation and distortion (x and y vari-mag.).

The alignment accuracy can be defined as a field displacement from perfect alignment (measured in pixels) over which the unambiguous contrast pattern is still observed. Three types of alignment detection pattern were used sequentially, each with successively finer alignment accuracy, they were:

a) coarse alignment detection pattern (accurate to ~ 20 pixels)

b) fine alignment detection pattern (accurate to ~ 3 pixels)

c) very-fine alignment detection pattern (accurate to 2 pixels in the y direction)

The alignment accuracy measured in nm depended on the exposure field size in use which determined the pixel separation. For instance, the finest alignment accuracy attained was 18nm when using the very-fine alignment detection pattern at 2500x magnification.

The coarse and fine alignment detection patterns were used at all levels after the first, and the very-fine alignment was additionally used for the gate level where the finer accuracy was needed.

The coarse alignment detection pattern (Fig. 3.7a page 97) consists of two gratings each with the minimum exposure allowed by the scan generator. Even after repeated scans of this pattern, the total exposure was below the critical dose for the resist. The stage was moved until the top left and bottom right small alignment marks were roughly in the centre of these gratings. The fine alignment detection pattern (Fig. 3.7b page 97) was a border around each of the four marks, again with a minimum exposure. The borders overlapped each mark by about 10% of the mark dimensions. The frame was shifted

until the marks were all central within the borders. This was achieved with stage movement in x, y, and rotation and a fine frame shift by adjustment of the x and y vari-mag. and beam shift controls.

The most accurate alignment was provided by the very-fine alignment detection patterns (e.g. Fig. 3.8 page 98). These patterns were used for aligning the gate patterns to the ohmic source-drain gap at each of 1250x and 2500x magnification, for each range of gate length. Alignment only in the y direction was provided by these patterns, which was the critical direction for gate alignment with respect to the source-drain gap.

Consider one of the four groups of lines in the pattern. Each line is actually composed of several short segments, progressively offset in the y direction (Fig. 3.9a page 99). The angled lines overlap the source and drain metal, thus providing the contrast necessary for alignment. When in perfect alignment the bright parts of each line are the same length. When out of alignment, the bright parts of each line are different lengths (Fig. 3.9b). The brightness (intensity) of the signal could be displayed on the second monitor of the PSEM 500 as a y displacement added to the beam y co-ordinate. This presented a graphic representation of the state of alignment (Fig. 3.9c).

Very-fine alignment gave an accuracy equal to half the y separation between the line segments. This allowed very accurate alignment in y offset, rotation and y magnification.

Fig. 3.10 (page 100) is an electron micrograph of a device which has been exposed repeatedly to the the very-fine alignment pattern, allowing the resist to develop through and pattern transfer to occur at the same time as the gate metallisation. The accurate alignment of the gate to the centre of the source-drain gap is visible.

3.4.7 Automatic Alignment

A system for automatic alignment was implemented in both hardware and software[186]. The method of alignment involved scanning single rows of pixels across the alignment marks, recording the brightness of the secondary electron detector signal, processing this signal, then moving the stage and pattern co-ordinates to align the exposure field.

The hardware consisted of:

a) an input from the SEM secondary electron detector

b) a low pass filter to remove noise from the signal

c) an analogue to digital converter (ADC) with digitally controlled potentiometers to set the gain and offset of the ADC.
d) an input from the scan generator clock to synchronise the line scan with the ADC measurements
e) connections to the controlling computer.

The software part consisted of routines to:
a) set up various system parameters (the Alignment Setup EBSS command)
b) calibrate the ADC black and white levels (by scanning over a mark) and load from a file and/or measure mark positions to build a model of their expected positions for subsequent alignments (Aligner Initialise command)
c) perform an automatic alignment.

The automatic alignment was started by searching from the expected mark positions across the frame until a mark was encountered; i.e. a bright pulse the expected size of a mark was found in the secondary electron detector signal. Then the stage was moved to bring the mark into its correct position. The search and move cycle was repeated until the mark was within 1μm (i.e. the position accuracy of the stage mechanism) of its expected position. Next, the presence of the remaining marks was determined and if enough were found the final accurate alignment would begin.

The four edges of each rectangular mark were found with further accuracy by scanning short lines parallel on either side and successively closer to each edge of the mark. This was repeated until the position of each edge was determined as the 50% threshold in contrast between substrate and mark brightness. All of the available edge positions were compared with the model and a pixel offset in x and y was generated between the actual and desired field position with respect to the sample. The pixel offsets were then added to each pattern element's co-ordinates before they were scanned.

This alignment procedure could be performed with the EBSS ALign command or at each site during the Step and Repeat sequence if the Aligner Enable command had been entered. If an automatic alignment failed, the user was allowed to re-align manually then try again or skip to another automatic alignment.

The contribution made as a part of this work to the automatic alignment system was the integration of these routines into the EBSS software both as discrete commands and embedded in the code of the Step and Repeat procedure.

3.4.8 Automatic Focusing

A simple yet very effective automatic focusing system was implemented in hardware and software[187]. The focusing method involved software calculation of an interpolated focus setting at a point on the sample, using four manual focus settings recorded near each corner of the chip.

The hardware consisted of:

a) inputs from the controlling computer for pulses indicating a change in focus and another signal indicating an increase or decrease of the focus setting

b) a 200kHz clock input from the PSEM 500 focus hardware

c) a circuit to synchronise the focus pulses with the SEM clock and combine (logical OR) them with the SEM manual control pulses

The software consisted of routines to:

a)initialise the focus system (EBSS command Focus Initialise) by prompting the user to focus near each of the four corners of the sample, recording the stage positions and focus setting.

b) perform an automatic focus.

The automatic focus routine used a set of three of the recorded position/focus data to interpolate the expected focus setting at the current stage position. This was repeated for the other three sets (combinations) of position/focus recordings, and the average of the four calculated settings was used to adjust the SEM focus. This routine was instigated directly using the FOcus command or automatically at each exposure site in a Step and Repeat sequence after entering the Focus Enable command.

Like the automatic aligner system, the contribution made as a part of this work was the integration of these routines into EBSS.

3.5 MESFET Fabrication Procedure

3.5.1 GaAs Wafer Preparation and Handling

If the wafer was supplied whole, then it was divided into quarters and marked with the growth sequence number. A protective layer of resist, 1μm thickness of PMMA, was spun onto new quarter wafers to protect them from dust during subsequent storage and scribing. In the case of immediate processing the resist was that of the alignment mark level. The quarter wafers were spun sitting directly on the rubber O-ring on a vacuum chuck. The 10mm squares needed for 400 device sites were scribed and cleaved. Plastic tweezers were used for subsequent chip handling in preference to metal to avoid cracking of the edge of chips which causes GaAs dust on the surface of the chip. In addition, plastic tweezers caused no damage to the GaAs if the surface was accidentally scratched with them. During acid etches, i.e. de-oxidisation prior to evaporation and wet gate recessing, teflon tweezers were used so as not to contaminate the etch solution with metal ions which were suspected to affect the etch rate.

3.5.2 Alignment Marks

Resist

The high resolution 310nm PMMA bilayer was used for the alignment mark level. The high resolution was needed for the small alignment marks which need to be well defined squares for consistent operation of the automatic alignment system. The resist was deposited as follows

8% BDH in o-xylene	5000rpm	40s
bake 1 hour 180C		
4% Elvacite in o-xylene	5000rpm	30s
bake 2 hour 180C		

Baking for a longer time did not affect lithography, except for long periods in the oven when dust accumulated. Baking for less time affected adhesion of the resist, but this was only critical for the wet gate recessing.

Exposure

The exposure was initiated with an EBSS command sequence which defined the appropriate patterns to be scanned and set up a position file which has 400 device sites in main site groups of 100 each with 10 rows and columns. The positions started from the bottom right corner of the 10mm square chip and the four main site groups were exposed clockwise from the bottom right. The site separation was 0.45mm horizontally and 0.35mm vertically.

A spot size of 64nm was chosen for the best definition of the smallest alignment marks, resulting in a relatively long total exposure time, however as the exposure was unattended this was not an inconvenience.

After measuring the beam current the vari-mag. controls were set to x=1.0 and y=1.0. A small piece of dust could usually be found on the chip surface for focusing at 5000x magnification, and if not the edge of the chip was used. After focusing the stage rotation was aligned to the frame (but not before focusing, because the frame rotation changes with focus). A horizontal line scan was selected, and the line was swept vertically across the bottom edge of the chip. The stage rotation was adjusted until the brightness along the line was constant at the chip edge.

Finally the Stage Enable, automatic Aligner Enable commands then the Step and Repeat command were issued and the exposure commenced, taking about 1 hour 50 minutes for 400 sites.

Development

The exposed resist was developed in 2.5:1 IPA:MIBK by volume (isopropyl alcohol : methyl iso-butyl ketone) for 30s and rinsed in IPA for 30s then blown dry with nitrogen. The 2.5:1 developer was warmed to 23C on a hotplate while being stirred with a thermometer probe. The pattern was checked with an optical microscope in case the beam current had dropped (thus leaving the resist under exposed) or the tungsten filament electron source had failed unnoticed during the exposure.

Metallisation

After wetting in IPA the chip was put directly in 1:4 HCl:H_20 for 30s then rinsed in H_20 and blown dry. This served to remove oxide from the surface, improving metal adhesion and (in later levels) electrical contact to

the semiconductor. The chip was then put into the air-locked evaporator as quickly as possible to reduce further oxidisation. The metals evaporated with a base pressure of at least $3x10^{-6}$mBar were

Ni	10nm	500Hz	(rate 20Hz/s)
Au	70nm	10kHz	(rate 50Hz/s)
Ni	20nm	1kHz	(rate 20Hz/s)

The metal thickness was measured during deposition using a crystal oscillator film thickness monitor. A quartz crystal oscillating at ~ 6MHz was positioned in the evaporation chamber near the chip and at the same distance from the evaporation sources. The mass of metal deposited on the crystal reduced the frequency of oscillation. The decrease in oscillation frequency (measured in Hz by an Intellemetrics Thickness Monitor, model IL002) is linearly related to the thickness of metal deposited, over a range of frequency of a few hundred kHz. The constant of proportionality is a function of the density of the metal being deposited. Similarly, the rate of decrease of frequency (measured in HZ/s) is a linear function of the rate of change of metal thickness. The thicknesses given above in nm were calibrated from measurements of film thickness for each metal using a Talystep.

Finally, lift-off was performed in acetone.

3.5.3 Isolation

Resist

A 0.2μm layer of polyimide was used as a parting layer to enable removal of the 0.5μm thick Ge mask after mesa etching. The positive resist for pattern transfer was a 1.5μm PMMA bilayer which gave a clean lift-off of the mask.

6% polyimide in 65:35		
acetophenone:o-xylene	5000rpm	60s
bake 1 hour 180C		
15% BDH in o-xylene	5000rpm	60s
bake 1 hour 180C		
4% Elvacite in o-xylene	5000rpm	30s
bake 2 hour 180C		

Exposure

The exposure was initiated with an EBSS command file which set up a position file containing stage co-ordinates for two groups of 100 sites. The positions started from the bottom right site of the first group (site 1). A spot size of 125nm was used.

After measuring the beam current the stage was moved to the first site on the chip and an alignment mark was used for focusing. The vari-mag. controls were set initially to x=1.0 and y=1.0. The small raster scan frame was used to locate the site and the rotation was set roughly. The magnification was set to 320x, the beam blanked, and spot mode selected. Next a manual alignment was made using the coarse and fine alignment detection patterns. Now the Aligner Initialise command was used to initialise the automatic alignment system using a batch file previously set up for the marks. The EBSS commands Stage Enable, Aligner Enable and Step and Repeat commenced the exposure which was left to expose all the sites unattended in about 50 min. After the exposure the beam current was measured again to check for drift (>5%) during the exposure which may have affected pattern development.

Development

The exposed resist was developed in 1:1 IPA:MIBK at 23C for 30s and rinsed in IPA for 30s then blown dry with nitrogen. The pattern was checked with an optical microscope.

Metallisation

The air-locked evaporator was used with a base pressure of at least $3x10^{-6}$mBar for evaporation of the metal

Ge 500nm 10kHz (rate 50Hz/s)

The metal was lifted off in acetone.

Mesa Etching

The dry etching of the mesa was a two stage process. The first was an 3 minute oxygen RIE of the polyimide in a PlasmaTech RIE 80. The flow rate was 30cc/min. The power was adjusted to 55W (adjusted to a DC bias of 200-250V, 200V minimum). There was no pressure control during the etch and the throttle valve was fully open. The second etch was a 5 minute methane/hydrogen etch in an ElectroTech 340, through the active layer. The

gas flow rate was 5:25cc/min (methane:hydrogen) and the power was 80W giving a DC bias voltage of 750V. This etch was calibrated to give a GaAs etch depth of 50nm.

Mask Removal

The etch mask was removed by soaking in boiling acetophenone for two hours to dissolve the polyimide, then ultrasonic agitation was used to ensure the isolation mask was fully dislodged. The chip was rinsed in fresh acetophenone then IPA and blown dry in nitrogen. The electron beam exposure used to define the mask was found to crosslink the polyimide underneath it, leaving a deposit which could only be removed with an oxygen plasma ash, performed in a Plasmafab 505. The disadvantage of this processing was the damage done to the surface of the active region by the physical bombardment by oxygen ions in the plasma and the resulting loss of carriers in the devices.

The mesa etch depth (mesa height) was measured in an Hitachi S800 SEM, by viewing the chip at a very shallow angle. An etch depth a few nm less than the active layer thickness (caused by fluctuations from the calibrated etch rate) could be tolerated because of surface depletion and dry etch damage.

3.5.4 Ohmic Contacts

Resist

A 310nm PMMA bilayer was used for the ohmic contact level. The high resolution of the resist allowed definition of the 0.7μm source drain gap of the ohmic contacts. The resist was deposited as follows

8% BDH in o-xylene	5000rpm	40s
bake 1 hour 180C		
4% Elvacite in o-xylene	5000rpm	30s
bake 2 hour 180C		

Exposure

The procedure for exposing the ohmic contact patterns was essentially the same as that described for the isolation level. The differences were the use of a 64nm spot size and a greater magnification of 640x. The identical

appearance of the inner set of alignment marks at this smaller frame size allowed the use of the same alignment detection patterns as before. The duration of the exposure was about 100 minutes.

Development

The exposed resist was developed in 2.5:1 IPA:MIBK (isopropyl alcohol : methyl iso-butyl ketone) for 30s and rinsed in IPA for 30s then blown dry with nitrogen. The 2.5:1 developer was warmed to 23C on a hotplate while being stirred with a thermometer probe. The pattern was checked with an optical microscope.

Metallisation

After wetting in IPA the chip was immersed in 1:4 HCl:H_20 for 30s then rinsed in H_20 and blown dry. The chip was then put into the air-locked evaporator as quickly as possible to reduce further oxidisation. The metals evaporated with a base pressure of at least $3x10^{-6}$mBar were

Au	70nm	9kHz	(rate 50Hz/s)
Ge	25nm	0.77kHz	(rate 20Hz/s)
Ni	10nm	0.6kHz	(rate 20Hz/s)
Au	15nm	2kHz	(rate 50Hz/s)

Anneal

The ohmic contact metallisation was alloyed by heating to a temperature of 340C in a reducing atmosphere of 5% H_2 in Ar for one minute. The chips were placed face up on a graphite resistance heater strip, with a thermocouple embedded in it for temperature measurement.

3.5.5 Probing Pads

Resist

The 1500nm bilayer was used to enable lift-off of the relatively thick metal used for the probing pads. The resist deposited was

15% BDH in chlorobenzene	5000rpm	60s
bake 1 hour 180C		
4% Elvacite in o-xylene	5000rpm	30s
bake 2 hour 180C		

Exposure

The exposure of the probing pads was identical to the isolation level except for using a 250nm spot size. The large spot size gave a higher video signal to noise ratio facilitating the automatic alignment and a shorter exposure time for each relatively large area pattern. This large area exposure at each site led to a total exposure time of 100 minutes for 200 devices.

Development

The exposed resist was developed in 1:1 IPA:MIBK at 23C for 30s and rinsed in IPA then blown dry with nitrogen.

Metallisation

After wetting in IPA the chip was put directly in 1:4 HCl:H_20 for 30s then rinsed in H_20 and blown dry. The chip was then put into the air-locked evaporator as quickly as possible to reduce further oxidisation. The metals evaporated with a base pressure of at least $3x10^{-6}$mBar were

Ti	30nm	0.77kHz	(rate 20Hz/s)
Au	300nm	50kHz	(rate 50Hz/s)

The interlocked evaporator was used because of the large amount of gold to be deposited.

The metal was lifted off in acetone.

3.5.6 Gate

Resist

Before the gate level resist was spun the source-drain saturation current for a representative sample of devices was measured for use with the gate recessing control (see section below on gate recessing).

Gates with lengths in the nm range were defined in the 190nm thick PMMA bilayer which gave high resolution, but did not allow reliable lift-off of more than 50nm of metal. In this case the resist was spun as follows

4% BDH in o-xylene	5000rpm	40s
bake 1 hour 180C		
4% Elvacite in o-xylene	5000rpm	30s
bake overnight 180C		

However, for gates with lengths above 100nm the thicker 320nm bilayer could be used, allowing lift-off of 150nm of gate metal yet still giving reproducible line widths. Here the resist was deposited as

8% BDH in o-xylene	5000rpm	40s
bake 1 hour 180C		
4% Elvacite in o-xylene	5000rpm	30s
bake overnight 180C		

In both cases the resist was baked overnight which was found to improve the adhesion of the resist during the subsequent recessing and deoxidising steps.

Exposure

The gate level exposure was only performed on one half of a chip (i.e. 50 sites), depending on the range of gate lengths to be exposed. The shorter gate lengths were exposed on the first 50 sites at 2500x magnification with an 8nm spot size (using the 190nm thick resist). The longer gate lengths were exposed on the second 50 sites at 1250x magnification using a 16nm spot size (using the 320nm resist). In both cases the exposure procedure was the same as for the isolation level. There were two differences. Firstly, the alignment marks used were part of the ohmic contact level pattern. Secondly, the auto-focusing system was used to ensure accurate focus control at each site of gate exposure. The auto-focusing was essential for a repeatable, high yield of the gates. When it was not used to correct for any non-horizontal seating of the chip on the stage, the drift in the focus setting (even across a 5nm chip) caused the resist not to develop fully in the finest features of the gate pattern.

The auto-focus system was initialised immediately after the measurement of the beam current. The manual focus control on the SEM was set to "fine" and not adjusted during the rest of the exposure. With the stage under automatic control, the Focus Initialise command prompted the user to move to each corner of the chip (anti-clockwise starting at the top right) and to focus by computer control via the keyboard. The focus was set at a high magnification (40000x) at an edge of pad metal of the devices nearest each corner.

The Focus Enable command set a software switch so that the Step and Repeat command would recalculate (by interpolation) and set the focus at each site during its operation.

The procedure for manually setting up the alignment before initialising the automatic aligner was also more complex for the gate level. Firstly, the standard coarse and fine alignment detection patterns were used to set up the translation and rotation of the chip with respect to the exposure frame. Next, the very-fine alignment detection pattern was used to register the frame exactly to the source-drain gap itself. After initialising the alignment system, the Align command was executed then the very-fine pattern scanned again. If the alignment was not correct, the manual alignment and initialisation procedure were repeated.

At the small frame sizes used for the gate, the stage movement errors were a significant proportion of the frame. This resulted in a large failure rate for the automatic aligner when combined with the small signal to noise ratio of the video signal (because of the small beam current). The Hit Enable command caused the system to pause at each site just before the automatic alignment. This allowed the user to move the stage into rough alignment before allowing the automatic alignment to resume.

Development

The gate pattern was developed in 2.5:1 IPA:MIBK at 23C for 30s and rinsing in IPA for 30s. The resist was then examined in a SEM to confirm that the alignment and focus had remained exact and the resist was fully developed through. The contrast between the resist and the exposed GaAs was good enough to allow the assessment to be made at a few representative sites across the chip. If the development was inadequate, further development of the resist was precluded because the SEM examination had exposed many sites. In this case the resist was stripped in acetone, re-spun and re-exposed. This examination revealed about 50% successful exposure of 30nm gates.

Recess

The gate recess was etched with a sulphuric acid based etch containing a wetting agent. The purpose of the wetting agent was to allow the etch to come into contact with the GaAs surface, even through the small slot in the resist defining the gate.

A set of new beakers was reserved for holding the gate recess etch. A 5% stock solution of the wetting agent was prepared in advance. The wetting agent, Fluorad FC-93 (manufactured by 3M) was supplied as a 25% by weight solution of active solids in IPA and water. The 5% solution was made by mixing 10:30:10 parts by volume of (25% FC-93):H_2O:IPA. The etch was prepared as follows. To 200ml of de-ionised H_2O was added 5ml of H_2SO_4, 1ml of 38% H_2O_2 solution, and 2ml of the 5% FC-93 solution. The quantities were measured with disposable 1ml plastic pipettes, one of which was used to stir thoroughly the etch solution. Two beakers of rinse were prepared, one of 30:70 IPA:H_20, the other H_2O. Some etch was transferred to a small beaker. The sample was placed in the etch for 60s and rinsed in each of H_2O, IPA:H_2O, H_20 then blown dry with nitrogen.

Several devices were probed (using the HP4145B) through the gate resist, measuring the source-drain current as a function of applied voltage. The current saturated at between 1V and 3V and this maximum saturation current was measured. The saturation current was normalised by dividing it by the original value measured before the gate level processing. The normalised value was referred to as the recess ratio and expressed as a percentage.

The sample was subjected to repeated etching and measurement until the recess ratio fell to 35±5%. This generally required 3 or 4 etch steps with the etch times reducing as the target was approached e.g. 60s, 60s, 30s, 10s. Fig. 3.11 (page 101) shows the source-drain characteristic for a device measured as the recess etch progressed. For the longer etch times the saturation becomes less pronounced as short-channel effects become apparent.

It was found that repeated probing of the same device in-between etches interfered with the progress of the etch, particularly for the shorter gate-lengths. This meant that the measured etch rate was not representative for the other devices, usually it indicated too small an etch rate. This is attributed to a distortion of the resist in the area of the gate stripe caused by the heating effect of the passing of the source-drain current. The argument is reinforced by an observed pattern transfer failure of many of the gates of devices which had been probed during the recess. The effect could be avoided by not probing the same device twice, at the cost of a reduced yield at the gate metallisation.

The reproducibility of the recess etch rate was poor. The etch rate was dependent on the age of the etch mixture, the rate decreasing over a period of a few hours from the preparation of the mixture. The etch rate also appeared to be strongly affected by the age of the hydrogen peroxide with a timescale in the order of weeks, measured from the first opening of the plastic container. Occasionally the etch rate was zero, but when a new mixture was prepared using the same ingredients and apparatus, the etch rate recovered. A possible explanation of this phenomenon is that the beakers used had become contaminated, perhaps with some organic debris which caused degradation of the etch.

The uniformity of the etch rate over the $(5mm)^2$ area of the chip was dependent on the gate-length of the devices. The etch rate is affected by the transport of the etchant into and etch products away from the GaAs surface. Because of the very small resist opening of the shortest gate-lengths, the etch rate was slower. Groups of adjacent devices of even the shortest gate-length were found to have threshold voltage differences of as little as 20mV. This is attributed to the excellent wetting properties of the surfactant added to the etch. Previous gate recessing without the surfactant had resulted in a very poor uniformity of the threshold voltage.

To summarise, the gate recess etch was uniform but only for a fixed gate-length, and not reproducible.

Metallisation

After wetting in IPA the chip was put directly in 1:4 $HCl:H_20$ for 30s then rinsed in H_20 and blown dry. The chip was then put into the evaporator as quickly as possible to reduce further oxidisation. Care was taken to keep the tungsten filament evaporation sources in a straight line when installing them, to avoid problems of shadowing during the evaporation. The sample was clamped to a holder and positioned above the evaporation sources so that the line of the gate stripe was parallel to the line of the evaporation sources. The sample was placed directly above the line of the evaporation sources, but displaced so that the metal would be incident on the vertical edge of the mesa nearest the gate pad. The Ti and Au evaporations were done from single, adjacent filaments. All of these precautions were necessary

to ensure an angle of incidence of evaporated metal which gave a gate centred in the recess (i.e. avoiding shadowing) and continuous across the edge of the mesa.

The gate metal was evaporated with a base pressure of at least $5x10^{-6}$mBar. In the case of the sub-100nm gates the metal was

Ti	20nm	1kHz	(rate 20Hz/s)
Au	34nm	4kHz	(rate 50Hz/s)

In the case of the longer gates the metal was

Ti	20nm	1kHz	(rate 20Hz/s)
Au	130nm	16kHz	(rate 50Hz/s)

The metal was lifted off in acetone.

3.5.7 Wiring

Resist

The 310nm PMMA bilayer was used for defining the wiring level. The resist deposited was

8% BDH in o-xylene	5000rpm	40s
bake 1 hour 120C		
4% Elvacite in o-xylene	5000rpm	30s
bake 2 hours 120C		

Note the 120C bake which was used because a 180C bake was found to degrade the Schottky barriers of the gates (see page 63 in the process design section).

Exposure

The wiring level was exposed using the same procedure as the isolation level, using a 125nm spot size but with a magnification of 640x.

Development

The exposed resist was developed in 2.5:1 IPA:MIBK for 30s and rinsed in IPA for 30s then blown dry with nitrogen.

Metallisation

After wetting in IPA the chip was put directly in 1:4 $HCl:H_20$ for 30s then rinsed in H_20 and blown dry. The chip was then put into the air-locked evaporator as quickly as possible to reduce further oxidisation. The metals evaporated with a base pressure of at least $3x10^{-6}$mBar were

Ni	10nm	500Hz	(rate 20Hz/s)
Au	140nm	20kHz	(rate 50Hz/s)

The metal was lifted off in acetone.

3.6 Results of Fabrication

Figs. 4.12 to 4.15 (pages 102 to 105) show electron micrographs of completed MESFETs.

Fig. 4.12 shows a plan view with the source pads at top and bottom, the gate pad at the left and drain pad at the right.

Fig. 4.13 shows an acute tilt angle view of the active region of a 120nm gate-length MESFET, where the 60μm mesa (and gate) width can be seen to occupy only $^3/_4$ of the available 80μm source-drain gap.

Fig. 4.14 shows a less acute tilt angle (40°) view of the active region of a 60nm gate-length MESFET. The length of the gate is much longer where it crosses the mesa near the gate pad at the bottom, to ensure reliable step coverage. The increased etch rate of the recess etch in this long gate-length region ensured that the active layer was fully depleted under the gate so discounting the possibility of a large, additional gate capacitance. This was confirmed by SEM examination of etch tests using the gate pattern.

Fig. 4.15 shows a 40° tilt view of the (150nm thick) gate of 100nm gate-length MESFET.

In these micrographs, the excellent flat morphology of the ohmic contact metal should be noted, which is a result of the low temperature annealing of the contacts. High magnification electron micrographs of 50 and 60nm gate-length MESFETs are given in Figs. 4.4 and 4.5 (pages 143 and 144).

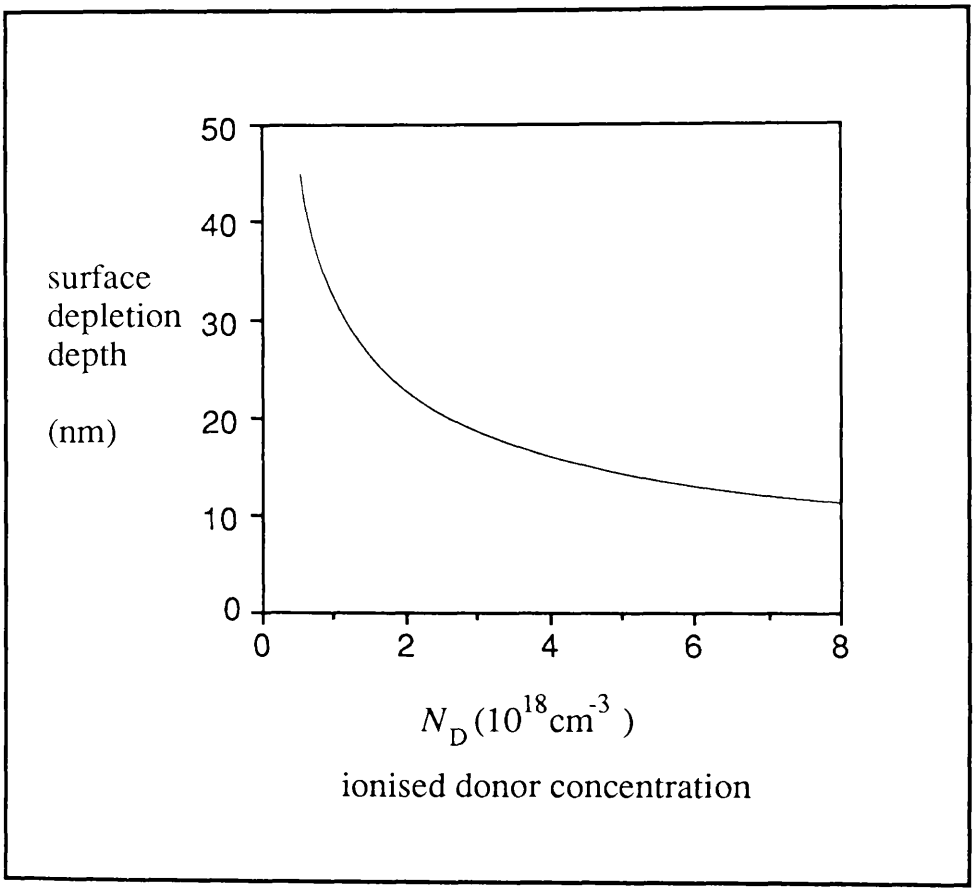


Figure 3.1 Surface depletion depth vs. ionised donor concentration
surface depletion depth = $(2\varepsilon V_{Bi} / qN_D)^{1/2}$; $V_{Bi} = 0.71V$

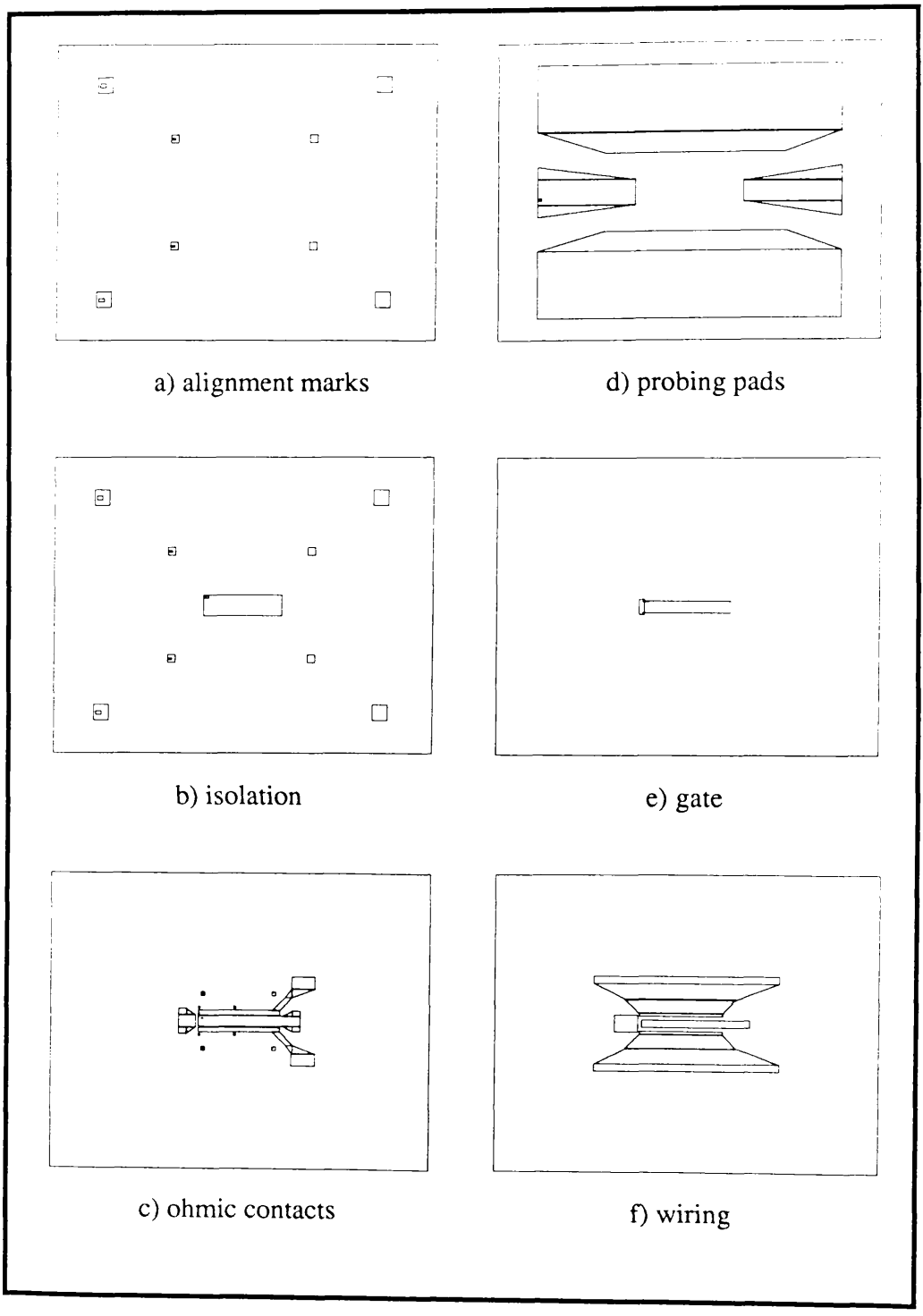


Figure 3.2 MESFET pattern levels

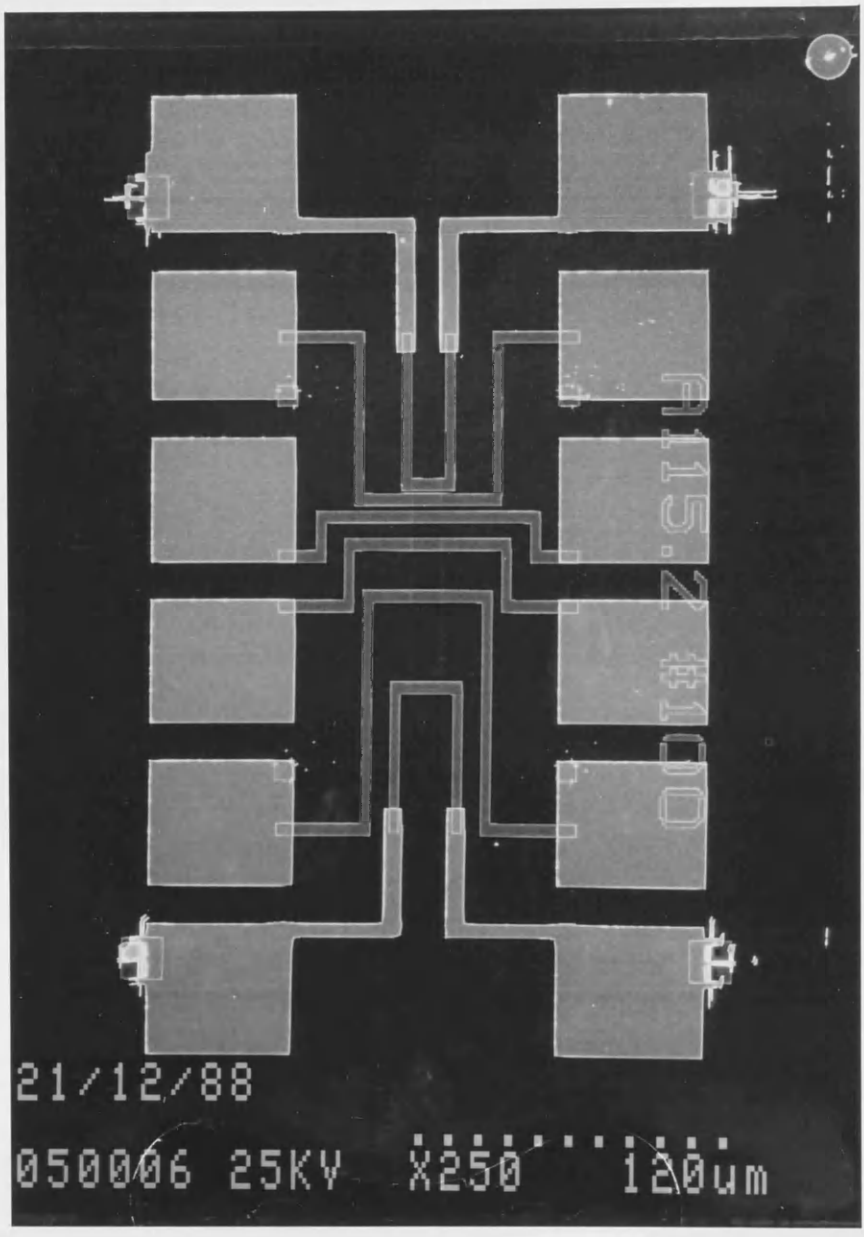


Figure 3.3 Ohmic contact resistance process control structure
(used for measurement of the ohmic contact end resistance)

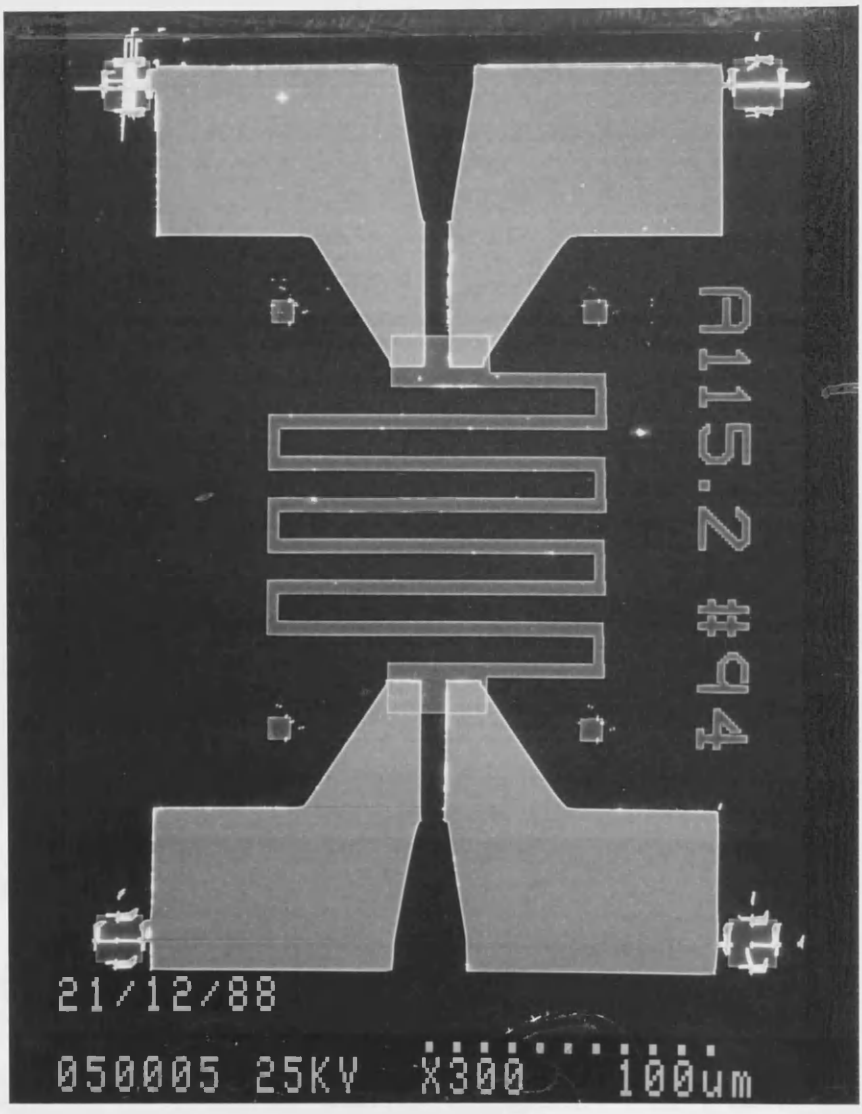


Figure 3.4 Ohmic contact resistance process control structure
(used for measurement of the ohmic contact series resistance)

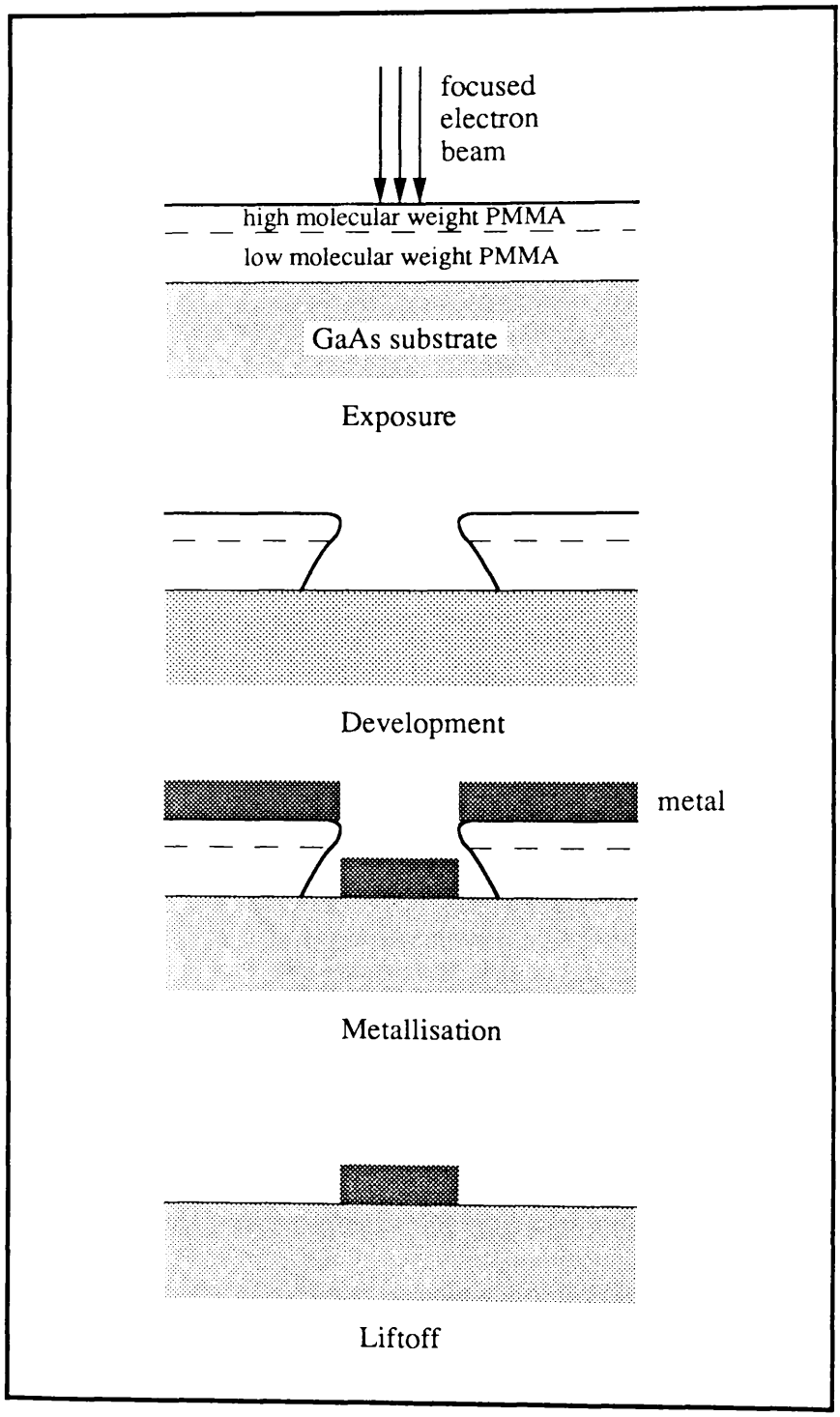


Figure 3.5 Bilayer resist lithography and pattern transfer

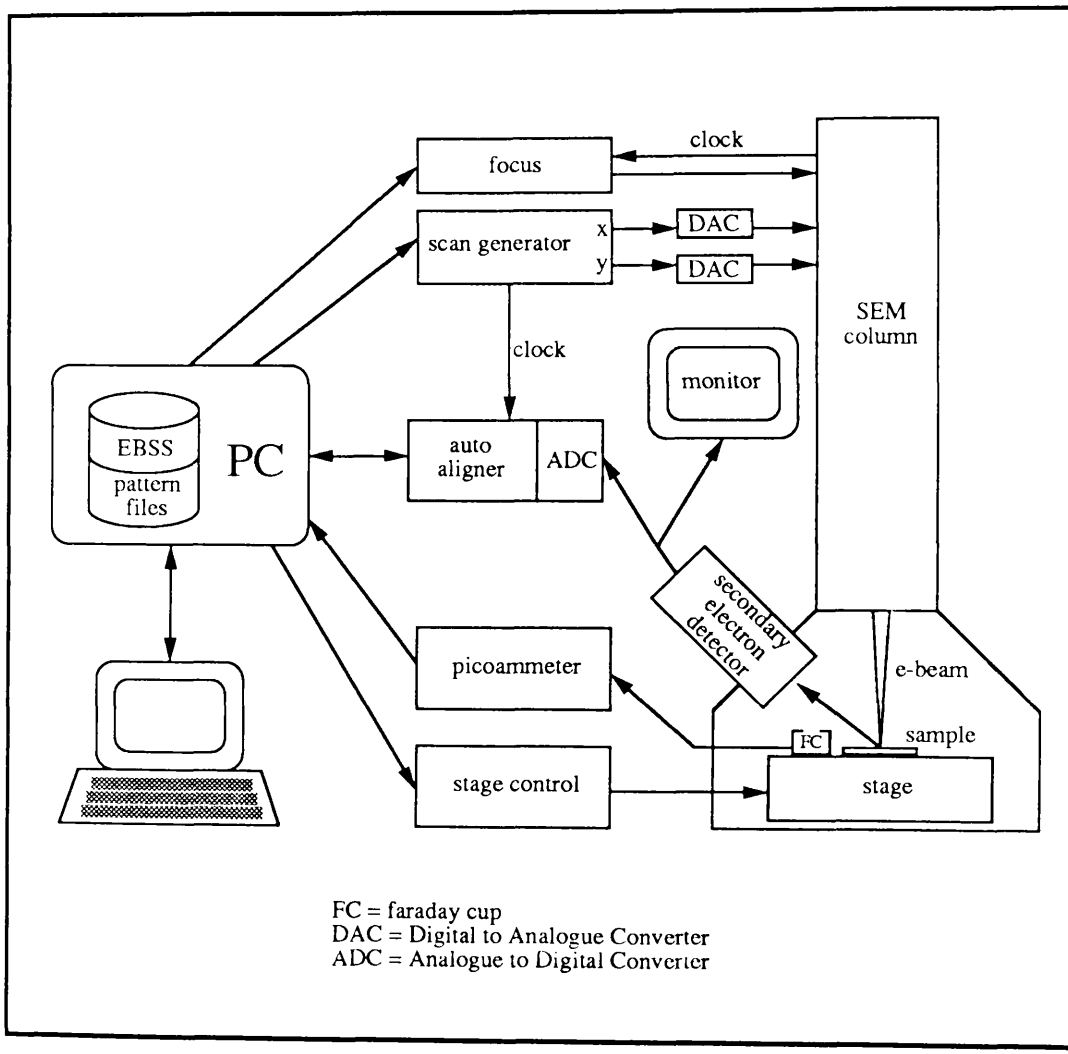


Figure 3.6 Electron beam lithography system

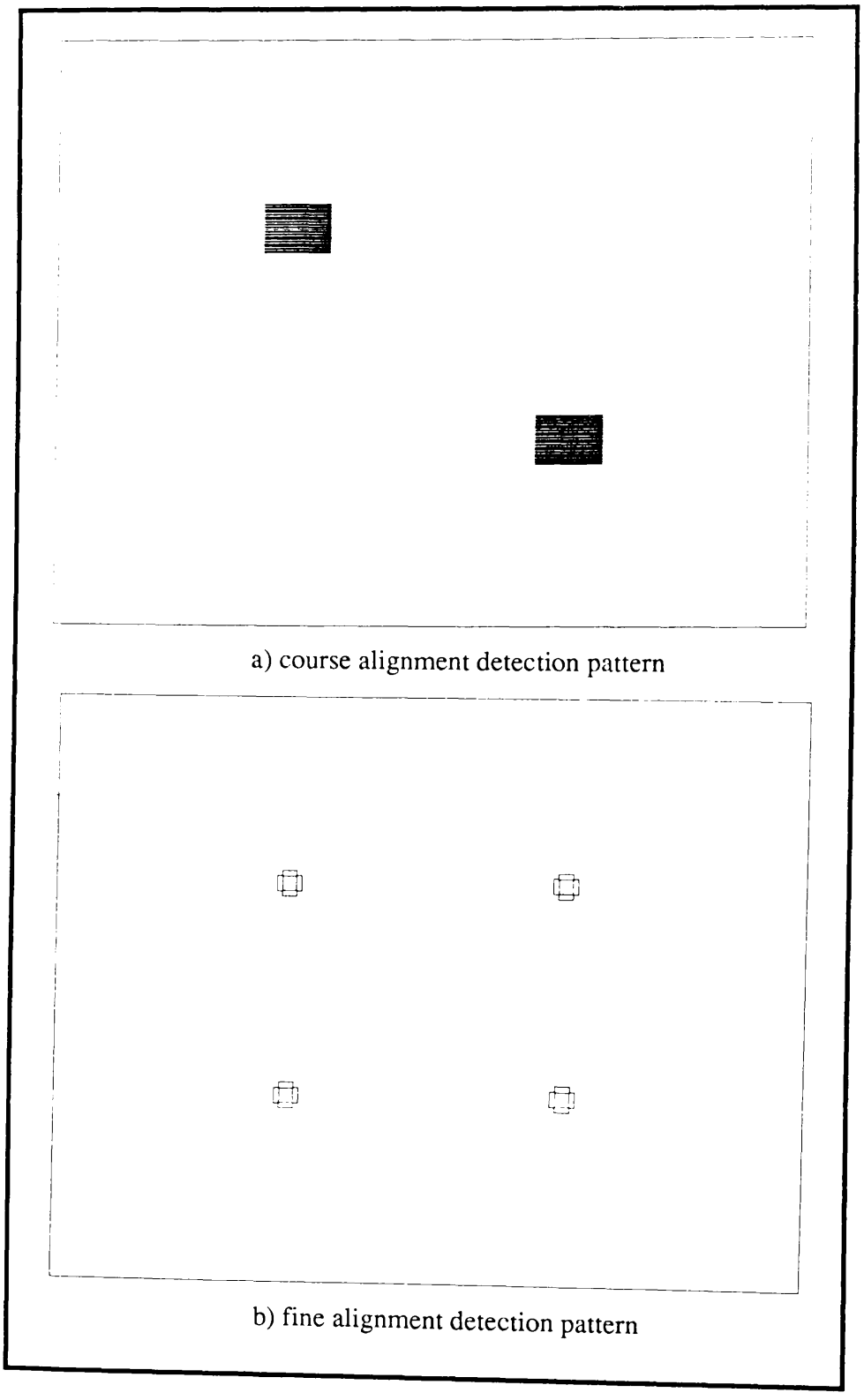


Figure 3.7 Manual alignment detection patterns

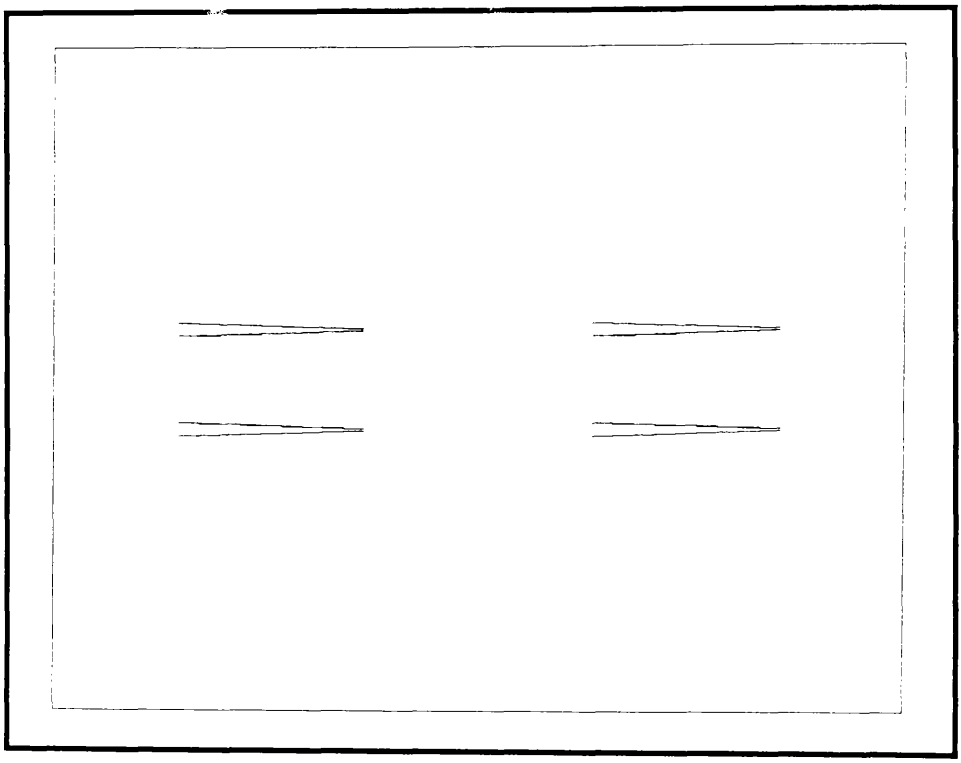


Figure 3.8 Very-fine manual alignment detection pattern

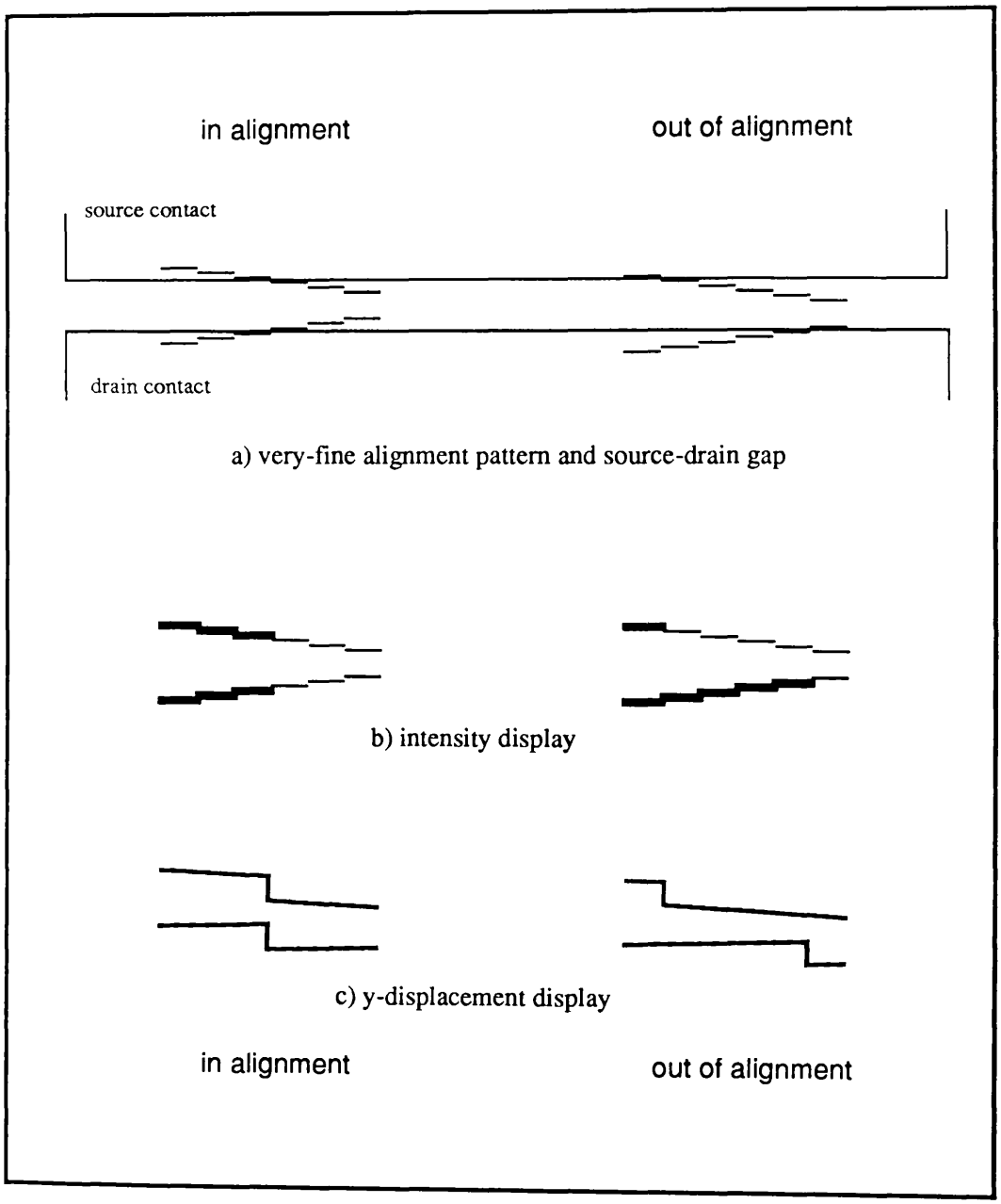


Figure 3.9 Use of the very-fine manual alignment detection pattern

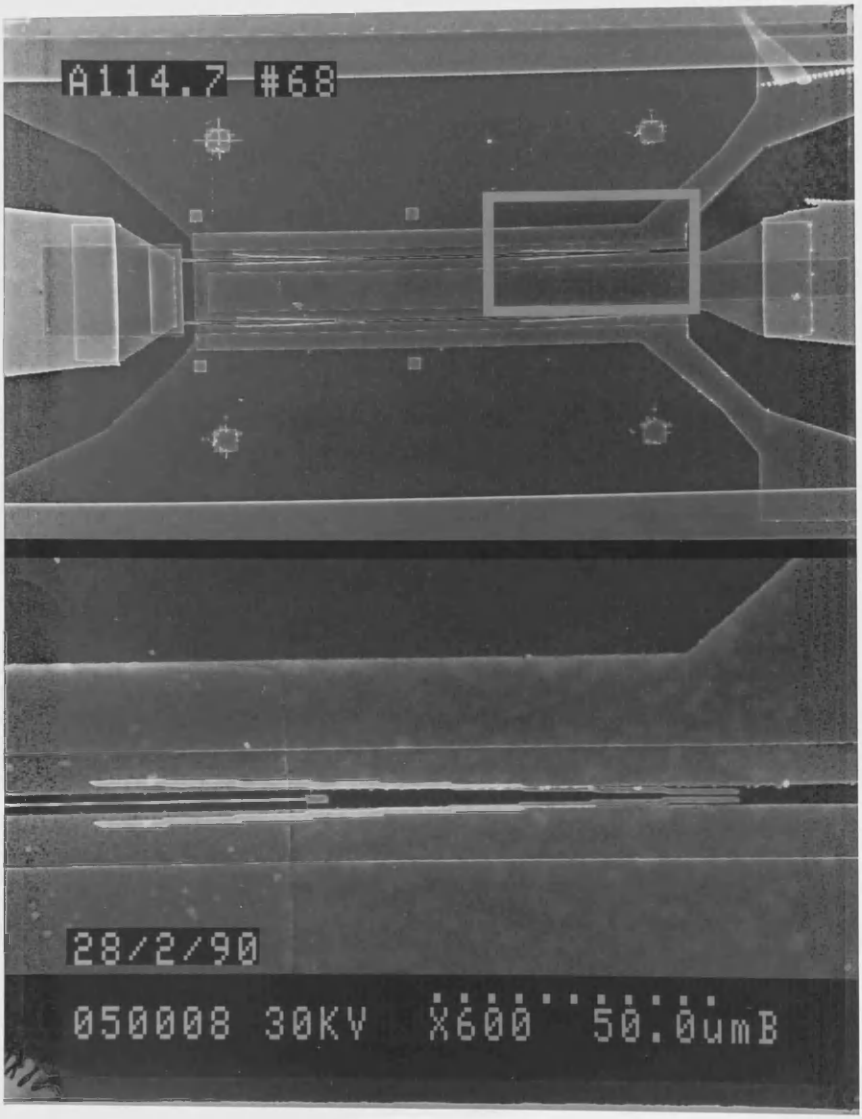


Figure 3.10 Overexposure of very-fine alignment detection pattern

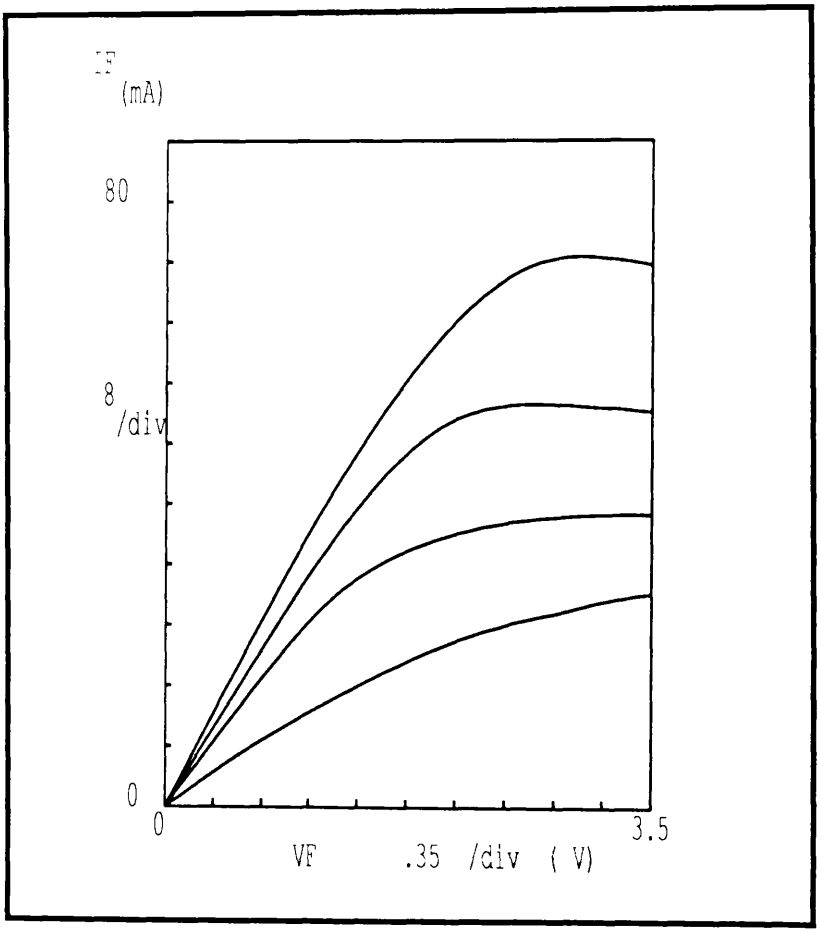


Figure 3.11 Example of monitoring of the gate recess etch

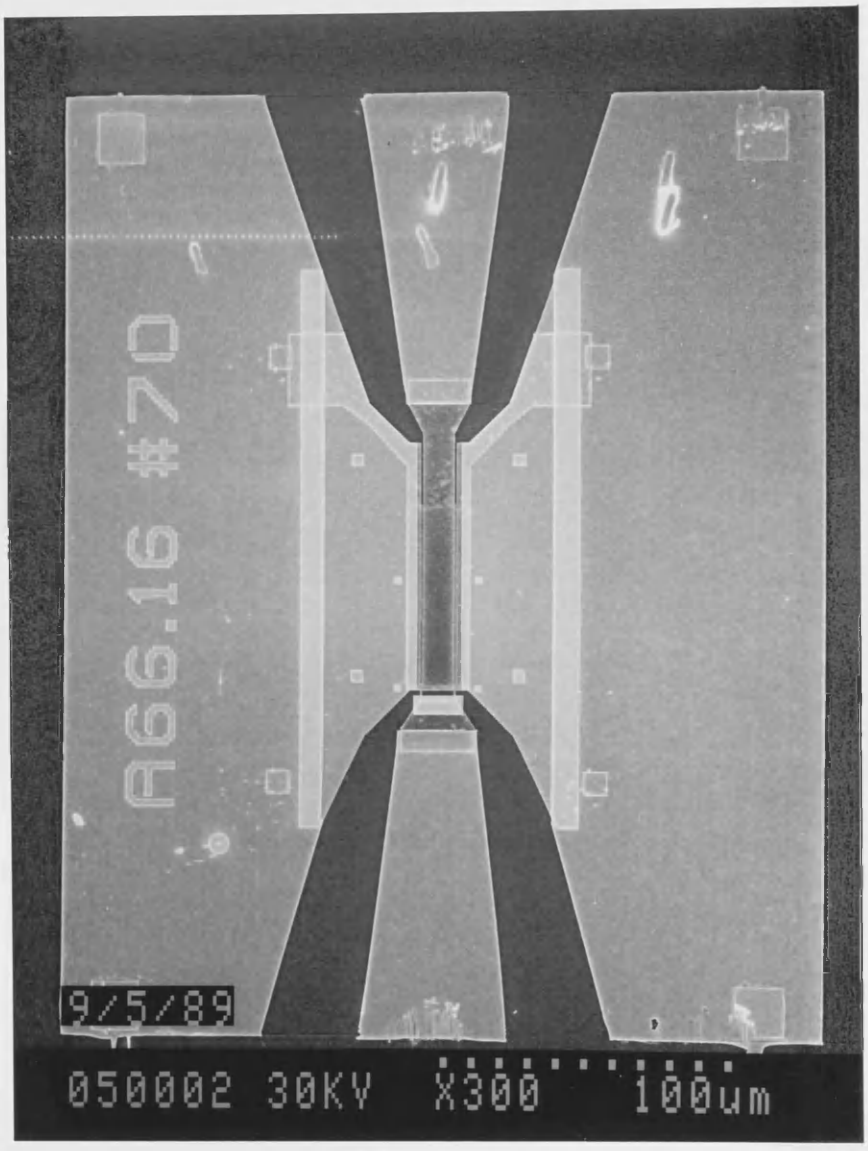


Figure 3.12 Electron micrograph of a GaAs MESFET
(source pads at left and right, gate and drain pads at bottom and top)

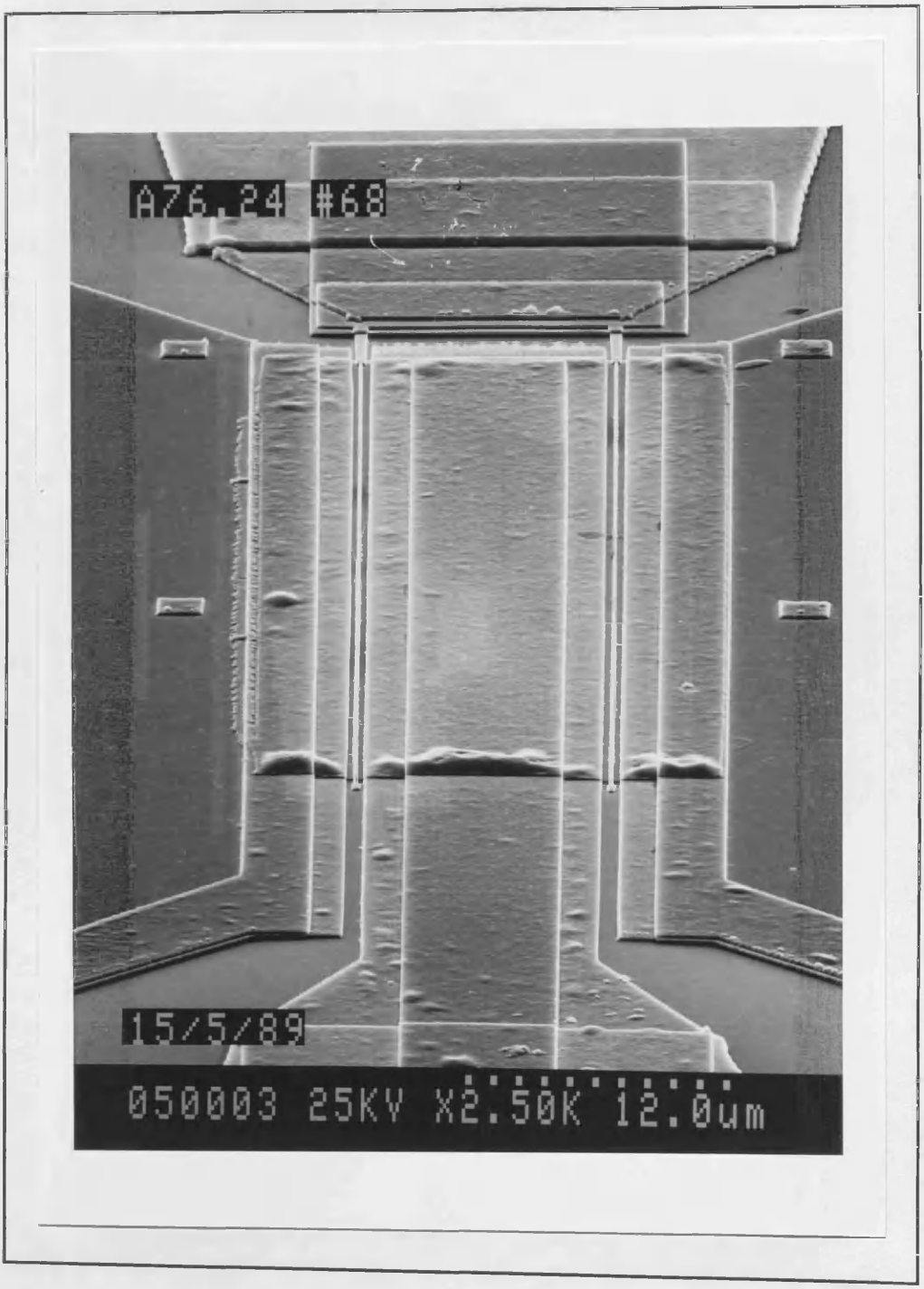


Figure 3.13 Electron micrograph of a 120nm gate-length MESFET

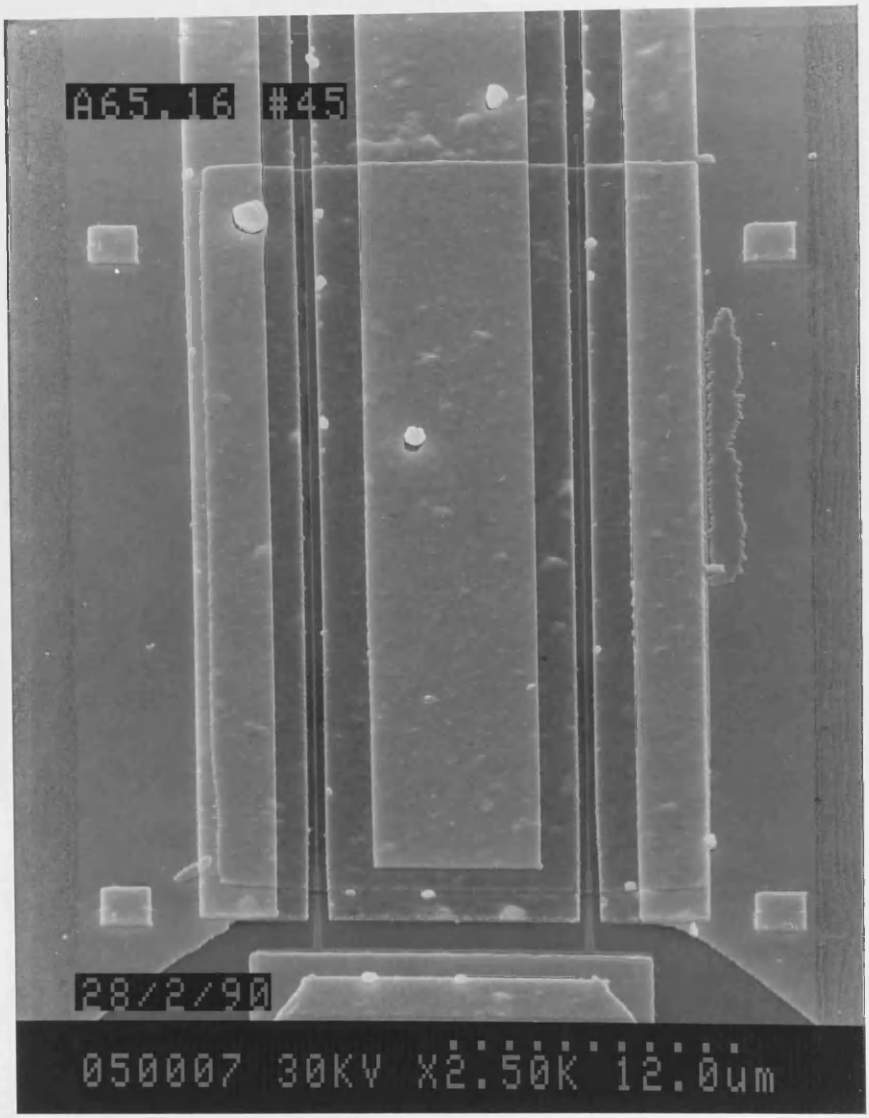


Figure 3.14 Electron micrograph of a 60nm gate-length MESFET

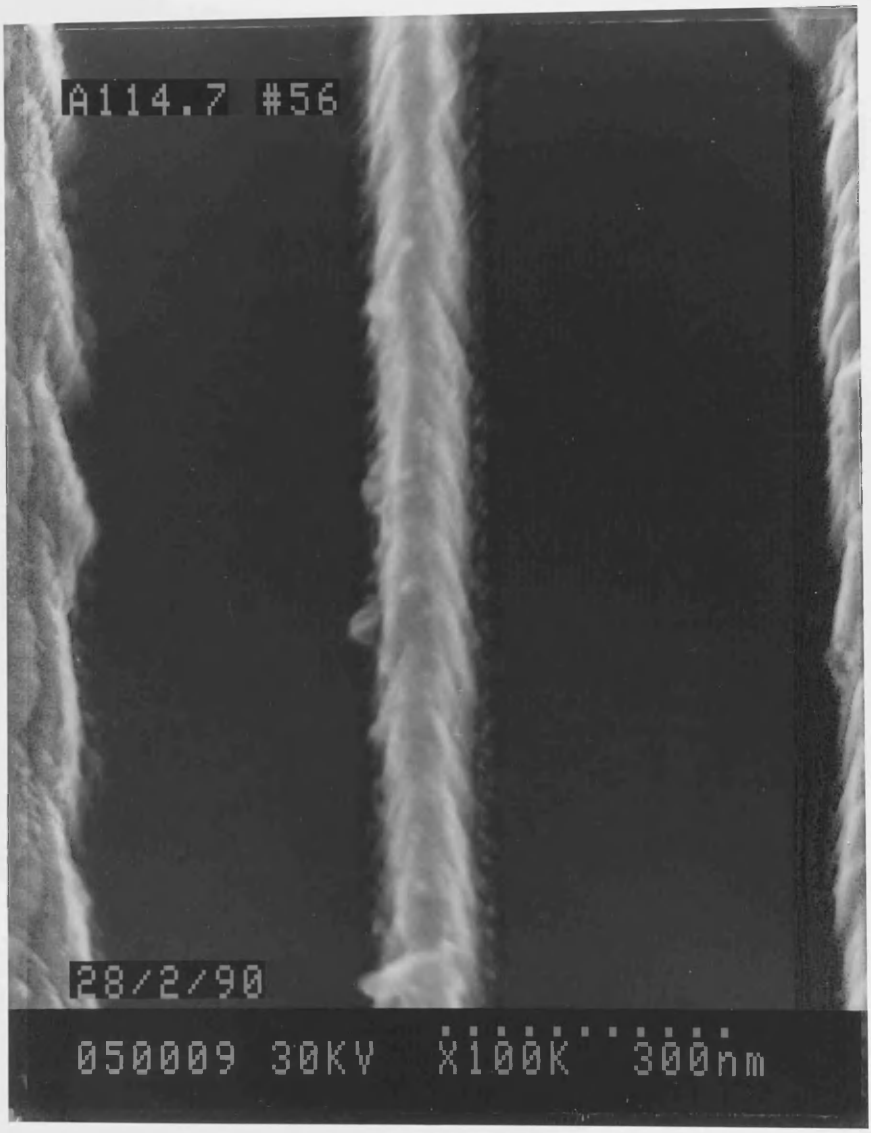


Figure 3.15 Electron micrograph of a 100nm gate-length MESFET

Chapter 4 - Results

4.1 Introduction

This chapter presents the results of DC and high-frequency electrical measurements of GaAs MESFETs with gate-lengths in the range 40 to 300nm. The purpose of the work is to investigate the various physical mechanisms responsible for short-channel effects, and obtain direct evidence of the action of these mechanisms wherever possible. Another objective is the comparison of GaAs and AlGaAs buffers, and confirmation of the beneficial role of the AlGaAs buffer layer in suppressing some of the short-channel effects.

First, characterisation of mobility and carrier concentration of the MBE grown layers and the system for DC and high-frequency measurements is described.

A discussion of gate-length measurement is followed by presentation of examples of the DC characteristics of the shortest gate-length device fabricated.

MESFETs fabricated on two wafers with nominally identical active layer thickness and doping concentration, one with an undoped GaAs buffer and the other with an undoped $Al_{0.3}Ga_{0.7}As$ buffer were compared using DC and high frequency characterisation. DC output and transfer characteristics yield figures of merit such as transconductance and output conductance. The subthreshold characteristics are examined in order to investigate the role of subthreshold buffer leakage current and drain induced barrier lowering (DIBL) controlled subthreshold current. The origins of drain bias dependent currents in the active and buffer layers which give rise to threshold voltage shift are investigated. The threshold voltage shift is equivalent to output conductance. Results obtained by S-parameter measurements in the range 45MHz to 26.5GHz are presented. Finally, an investigation of the parasitic

transit delays is presented. The delays were obtained from a series of S-parameter measurements for each device at a range of gate and drain biases.

MESFETs with ~ 130nm gate-length were fabricated on three wafers with nominally identical active layer thicknesses, the first with an undoped GaAs buffer, the second with an undoped $Al_{0.3}Ga_{0.7}As$ buffer and the third with an undoped $Al_{0.3}Ga_{0.7}As$ buffer including growth interruptions. DC and high frequency characterisation were used to compare these devices. The growth interruptions in the latter wafer are shown to improve the active/buffer layer interface quality.

MESFETs with ~ 200nm gate-length were fabricated on three wafers with nominally identical active layer thicknesses and undoped GaAs buffer layers, each with different active layer ionised donor concentration.

The conclusions of the work are summarised at the end of each section, and are collected together in the final chapter 5.

4.2 Material Characterisation

The low field Hall mobility, μ_H and carrier concentration in the MBE grown epi-layers were determined using a Bio-Rad Polaron HL5200 Hall measurement system. The measurement yielded the sheet carrier concentration, N_{sh}. This could have been converted into a volume concentration by dividing by the active layer thickness, a (= 50nm). The volume carrier concentration is assumed to be equal to the ionised donor concentration, N_D. However, in these thin active layers surface depletion (a function of N_D) reduces the thickness of the conducting layer. The smaller depletion depth from the diffusion field at the active/buffer interface is ignored here. Thus,

$$N_D = \frac{N_{sh}}{h(N_D)} \tag{4.1}$$

where the thickness of undepleted active layer,

$$h = a - (2\varepsilon V_{sp} / qN_D)^{1/2} \tag{4.2}$$

where V_{sp} is the surface potential, assumed to be 0.72V in GaAs i.e. pinned at mid-bandgap by surface states. Equation 4.1 was solved iteratively to obtain N_D. The results of this characterisation, along with details of the layer structures used in this project are given in Table 4.1 below.

Table 4.1 MESFET MBE layer structures

Layer Code	Buffer Layer	Active Layer Doping N_D (cm^{-3})	Hall Mobility μ_H (cm^2/Vs)
A65	GaAs	$4.1x10^{18}$	1520
A66	$Al_{0.3}Ga_{0.7}As$	$3.9x10^{18}$	1410
A76	$Al_{0.3}Ga_{0.7}As$*	$4.0x10^{18}$	1450
A114	GaAs	$2.2x10^{18}$	2050
A128	GaAs	$7.1x10^{18}$	1280

NOTES.
* Buffer grown with 4 interruptions (GaAs monolayer).
n-type (Si doped) active layer thickness is 50nm in all cases.
Buffer layer thickness is 200nm in all cases.

The Hall mobility technique, combined with gradual wet etching of the active layer, was used to obtain a mobility profile with depth for two of the wafers used in this work[188]. The GaAs buffer wafer A128 was compared with the AlGaAs buffer wafer A76. The Hall mobility was plotted against N_{sh} (Fig. 4.1 page 140). In the GaAs buffer case the mobility actually increases as N_{sh} is reduced by etching the active layer. This may be explained by the increase in the proportion of carriers in the higher mobility GaAs buffer layer relative to the number in the channel. In the AlGaAs buffer case the mobility drops as the active layer thickness is reduced. This is a result of the increased proportion of carriers in the low mobility AlGaAs buffer layer and/or a degradation of mobility in the active layer near the interface. This mobility degradation is expected to be worse in the AlGaAs buffered layer which was grown without interruptions (A66).

4.3 Measurement System

4.3.1 DC Measurements

All direct current (DC) measurements were performed using an HP4145B semiconductor parameter analyser. The HP4145B was connected through an HP8515A S-parameter test set to Cascade Microtech microwave probes for supplying the DC drain and gate biases during high frequency measurements. This set up was also used for DC probing (see Fig. 4.2 page 141). The low pass filters in the S-parameter test set protected the devices from voltage transients and prevented gate voltage oscillations arising from a feedback circuit containing the inductance of leads between the device source and ground. Both of these detrimental effects had been encountered when using a conventional DC probe station. The measurement system was controlled by an IBM PC compatible computer via an IEEE-488 bus. Software was written as part of this work for automating DC measurements and downloading data and graphs to the PC from the HP4145B.

4.3.2 High-Frequency Measurements

Microwave S-parameter measurements were made using an HP8510B automatic network analyser, an HP8340B synthesised sweeper (10MHz to 26.5GHz), an HP8515A S-parameter test set, and Cascade Microtech on-wafer probes, with DC biasing provided by an HP4145B semiconductor parameter analyser (see Fig. 4.2).

Measurements were made in the frequency range 0.05GHz to 26.5GHz. The system was calibrated[189] using load, short-circuit, open-circuit, and feed-through standards fabricated on GaAs using identical processing and pad geometry to the pad level of the MESFETs. This ensured that the S-parameters were measured for the active region of the device alone, so excluding the pad capacitances from the measurements.

The S-parameters were downloaded to the PC, and from them f_T was calculated by extrapolating to zero a fitted line of $|h_{21}|$ (in dB) versus f over a specified range of measurement frequencies. Two methods of fitting were employed, one a least squares fit, the other a least squares fit with the slope constrained to 20dB/decade (6dB/octave). f_{max} was calculated by extrapolating a least squares fit of the maximum available gain[132] (MAG) in

dB versus f to zero.

The results were output to a file, and graphically to the PC screen as shown in Fig. 4.3 (page 142). Some of this software system was written as part of this project.

4.4 Short Gate-Length MESFETs

4.4.1 Gate-Length Measurements

GaAs MESFETs were fabricated with gate-lengths down to 40nm. Gate-length was measured using an Hitachi S900 SEM. Fig. 4.4 (page 143) shows the recessed gate of a 40nm device. The electron micrograph appears slightly fuzzy when compared to that of a 50nm device (Fig. 4.5). This is cased by a layer of contamination (probably rotary pump oil) which had been deposited on the device during examination with an Hitachi S800 SEM. This contamination, combined with the lower resolution of the S800 compared with the S900 had previously led to an underestimation of lengths of these gates[1,2].

The high resolution micrographs from the S900 show a narrow, well defined gold stripe sitting on an irregular and wider stripe of titanium. The extra width of the titanium adds about 10nm to the previously determined gate-length.

4.4.2 DC Characteristics

The current/voltage output and transfer characteristics of the 40nm device of Fig. 4.4 are given in Fig. 4.6 (page 145). The main features of the characteristics are labelled in Fig. 2.3 (page 52). The device has a GaAs buffer (wafer A65) and it displays the short-channel effects of poor pinch-off, large output conductance, g_d (120mS/mm) and, despite a large peak extrinsic transconductance, g_m (710mS/mm), a small voltage gain, $A_V = g_m/g_d$ of 6.

g_d was measured for this and all devices at the gate bias corresponding to maximum g_m and at the same drain bias as the g_m measurement (V_{ds} = 1.4 to 1.6V).

The K-value (in this case 331mS/Vmm) was measured as half of the steepest slope of the g_m versus V_g curve.

4.5 MESFETs with GaAs and $Al_{0.3}Ga_{0.7}As$ Buffers

MESFETs with gate-lengths in the range 40 to 300nm were fabricated on two wafers with nominally identical active layer thickness and doping concentration, one with an undoped GaAs buffer (A65) and the other with an undoped $Al_{0.3}Ga_{0.7}As$ buffer (A66). In this section DC and high frequency characterisation are used to compare these devices.

4.5.1 DC Characteristics

In the comparisons below where the output and transfer characteristics are given, the devices were chosen to have similar threshold voltages. Where devices with different widths are compared, the drain current scales are normalised to the largest width device.

Long-Channel MESFETs with GaAs and AlGaAs Buffers

Figs. 4.7 and 4.8 (pages 146 and 147) show the output and transfer characteristics respectively of 300nm gate-length MESFETs with GaAs and AlGaAs buffers. Both devices can be completely pinched-off over the entire range of drain bias.

In the output characteristics (Fig. 4.7) the output conductance decreases from 31mS/mm to 19mS/mm for the GaAs and AlGaAs buffer devices respectively. In the transfer characteristics (Fig. 4.8) the maximum transconductance decreases from 540mS/mm to 525mS/mm. This gives voltage gains, $A_V = g_m/g_d$ of 17 and 28. The K-value rises from 300mS/Vmm to 440mS/Vmm, as would be expected because of the superior carrier confinement in the active layer of the AlGaAs buffer.

Short-Channel MESFETs with GaAs and AlGaAs Buffers

Figs. 4.9 and 4.10 (pages 148 and 149) show the output and transfer characteristics respectively of 60nm and 50nm gate-length devices with GaAs and AlGaAs buffers. The AlGaAs buffer device can be completely pinched-off over the whole range of drain bias, whereas the GaAs buffer device shows a punch-through current beyond $V_d \sim 0.5V$.

In the output characteristics (Fig. 4.9) the output conductance decreases from 92mS/mm to 69mS/mm for the GaAs and AlGaAs buffer devices respectively. In the transfer characteristics (Fig. 4.10) the maximum

transconductance decreases from 620mS/mm to 580mS/mm. This gives voltage gains of 7 and 8. The K-value rises from 540mS/Vmm to 570mS/Vmm.

Transconductance and Output Conductance

Figs. 4.11a, b and c (page 150) show the measured peak extrinsic transconductance, output conductance and voltage gain versus gate length for GaAs and AlGaAs buffer MESFETs with gate-lengths in the range 40 to 300nm. The extrinsic values of transconductance rather than intrinsic (see equation 2.16 page 13) are compared in these devices because the effect of the parasitic source resistances is assumed to be similar, as the contact resistance and active layer thickness and doping are the same. A possible difference could arise from unequal depths of depletion from the active/buffer layer interface. However, the assumption has been validated by noting the similar extracted values of the equivalent circuit elements ($R_s \sim 0.5\Omega$mm) from high frequency measurements (see page 125) for devices with different buffer layers and equal gate-length.

Fig. 4.11a shows an increase in peak transconductance as the gate-length is reduced below 100nm for both types of buffer layer. This could be explained by velocity overshoot effects, however this is not confirmed for these devices by the high frequency measurements presented in section 4.5.4 below (page 124). It is more likely a result of the scatter in threshold voltages as discussed in the next section and shown in Fig. 4.19a (page 158). A higher transconductance appears to be associated with a more negative threshold voltage in the sub-100nm gate-length GaAs buffer devices. This may be caused by the poor confinement of carriers in the active layer afforded by the GaAs buffer. Those devices with a more negative threshold voltage have shallower recesses and correspondingly thicker active layers under the gate. So at the operating point for peak transconductance, the edge of the gate depletion region is further away from the buffer layer where transconductance may be degraded in the GaAs buffer case by poor carrier confinement.

In Fig. 4.11a the devices with AlGaAs buffers have lower transconductances despite the superior carrier confinement over the GaAs buffer. This can be explained by mobility degradation in the active layer arising from the problems of MBE growth of the inverted GaAs/AlGaAs interface (see section 2.6.2 page 38). This would reduce the intrinsic

transconductance, because a proportion of the velocity distribution of carriers in the channel is in the low field mobility governed range of velocities. In addition, mobility degradation in the active layer will increase parasitic series resistances in the source-gate and gate-drain access regions, thus reducing the extrinsic transconductance (see equation 2.16 page 13).

Fig. 4.11b shows output conductance increasing as the gate-length is reduced. At each gate-length where a comparison can be made, the AlGaAs buffer devices have lower output conductance than the GaAs buffer devices, which is a consequence of the suppression of buffer current by the AlGaAs buffer. While this difference remains roughly constant, as the gate-length decreases both sets of devices exhibit a large increase in output conductance. This can be explained by an increase in the contribution to g_d of active layer current which is dependent on drain bias. This current can arise from several mechanisms, including hot-electron effects and punch-through, which are discussed in section 4.5.3 below (page 118).

Fig. 4.11c shows the voltage gain, $A_V = g_m/g_d$ as being similar for the GaAs and AlGaAs buffer short-channel devices. In contrast, at longer gate-lengths, the great reduction of buffer current in the AlGaAs buffer layer devices gives a significant increase in voltage gain over the GaAs buffer devices.

This reduced advantage of the AlGaAs buffer for the shortest gate-length devices stems from;

a) the reduced transconductance caused by the poor active/buffer layer interface

b) V_{ds} dependent current in the active layer, as opposed to buffer layer current, becomes an important mechanism leading to output conductance.

Summary

The following results were found in the DC output and transfer characteristics:

1) Thin, highly doped active layers with high quality interfaces grown by MBE allow fabrication of scaled MESFETs with very good extrinsic transconductance, even down to the shortest gate-lengths (720mS/mm for a 40nm gate-length).

2) AlGaAs buffer devices have slightly lower transconductance because of the the inferior active/buffer layer interface quality.

3) AlGaAs buffer devices have smaller output conductance and greater voltage gain because of the reduction of current in the buffer.

4) The output conductance, g_d rises with reduced gate-length equally for the devices with both GaAs and AlGaAs buffers. The difference between g_d at each gate-length is the contribution of buffer-layer current. At very short gate-length, the advantage of the AlGaAs buffer diminishes, because punch-through and hot-electron effects mechanisms operating mainly in the active layer become predominant.

5) AlGaAs buffer devices have larger K-values, because of the sharper pinch-off against the buffer layer, i.e. better carrier confinement in the active layer.

4.5.2 Subthreshold Current

In this section, the subthreshold characteristics are examined in order to investigate the role of subthreshold buffer leakage current and drain induced barrier lowering (DIBL) controlled subthreshold current. The buffer leakage current is distinct from the DIBL controlled current in that it does not have an exponential dependence on V_{ds}.

Long-Channel MESFETs with GaAs and AlGaAs Buffers

Fig. 4.12 (page 151) shows the subthreshold transfer characteristics of 300nm gate-length MESFETs with GaAs and AlGaAs buffers. The source current, $I_s = I_d - I_g$ is plotted against gate voltage V_g. The drain bias, V_d is incremented from 0.05 to 1.85V in steps of 0.2V.

At low V_{ds}, the two devices have similar gate swings, S_g of 160mV/decade and 120mV/decade (the right hand curves). The AlGaAs device has a lower S_g because of the better carrier confinement in the channel. The most striking differences appear as the drain bias is increased. In the GaAs buffer device, current in the GaAs buffer causes a rapid increase in the gate swing. In the AlGaAs buffer device the buffer leakage current is suppressed and the gate swing is hardly affected by the increasing drain bias.

We can confirm that much of the excess current in the GaAs device is caused by a buffer leakage mechanism by examining the subthreshold output characteristics (Fig. 4.13).

The curves on subthreshold output characteristic of the GaAs buffer device (Fig. 4.13a) show both buffer leakage and DIBL current control mechanisms. At large V_{ds} and small gate bias (the lower right curves,

V_g < -1.1V) the non-linear dependence of log I_s with respect to V_{ds} is attributed to buffer leakage current. Linear sections are apparent on the top three curves. The linear section is at small V_{ds} for the lower V_g (third curve from top, V_g = -1.1V) before giving way to buffer leakage and open channel behaviour at higher V_{ds}. The linear section grows to almost the entire range of V_{ds} for the largest V_g (top curve, V_g = -0.7V) when the channel is pinched-off less extremely.

For the AlGaAs buffer device, in the absence of buffer leakage current in the buffer, the subthreshold output characteristics (Fig. 4.13b) clearly show a linear dependence of log I_s with V_{ds}. No buffer leakage behaviour is evident.

The linear dependence of log I_s with V_{ds} is characteristic of a DIBL process, where a small diffusion current over a potential barrier is controlled by the influence of the bias on drain electrode. In these characteristics, the influence of V_{ds} on the current (corresponding to the strength of coupling of V_{ds} to the barrier height) is very small, as can be seen by the very shallow slope of the linear parts of the subthreshold output characteristics. In contrast, the coupling of the gate bias to the barrier height is very strong, with resulting small values of S_g on the subthreshold transfer characteristics.

The weakness of the DIBL control of the subthreshold current can be explained by the long-channels of these devices, where the potential barrier height at the virtual cathode near the source is unaffected by the increase in drain bias (see Fig. 2.4a page 53). Such a long-channel case has been analysed theoretically and experimentally for the JFET by Brewer[23], who calculated the diffusion current between the virtual cathode and the drain. He assumed a parabolic potential trough along the pinched-off channel with an effective width w_{eff} of $(2\pi)^{1/2}\lambda_D$. The carrier density at the virtual cathode is given by equation 2.35 (page 20). At the drain end of the channel (the "virtual anode"), the carrier density is

$$n_{va} = N_D \exp(-(\psi_b+V_d')/U_T) \qquad (4.3)$$

where V_d' is the voltage provided by the drain at this point (corrected for R_d). The diffusion current is given by

$$I_s = Zw_{eff}qD \frac{n_{vc} - n_{va}}{L} \qquad (4.4)$$

This expression explains the linear behaviour of log I_s with V_s in these long-channel MESFETs. The very strong coupling of V_g to ψ_b for all drain biases in the AlGaAs buffer device subthreshold transfer characteristic (Fig. 4.12b) explains why this current vanishes so rapidly as V_g decreases (below -1.1V in Fig. 4.13b). Recall that in the GaAs buffer device, for small V_g (< -1.1V), the subthreshold current did not vanish, but was governed by buffer leakage.

The slopes of the linear sections in the GaAs buffer subthreshold output characteristic (Fig. 4.13b) are steeper than those of the AlGaAs buffer device, and at lower current values. This could be caused by the subthreshold (diffusion current) channel being pushed into the GaAs buffer, thus decreasing the strength of coupling of V_g to ψ_b, and allowing V_{ds} more control over these currents than in the AlGaAs buffer case.

Equation 4.4 is similar to expressions derived and experimentally verified for subthreshold operation of MOSFETs[190] and buried channel MOSFETs[191].

Short-Channel MESFETs with GaAs and AlGaAs Buffers

Fig. 4.14 (page 153) shows the subthreshold transfer characteristics of 60 and 50nm gate-length MESFETs with GaAs and AlGaAs buffers respectively. Let us first consider the AlGaAs buffer device characteristic.

In Fig. 4.14b for the AlGaAs buffer device, a good pinch-off is observed, with a low gate-swing, S_g of 240mV/decade at low V_{ds} (right hand curve). Unlike the long-channel AlGaAs buffer device, an increased drain bias has a significant effect on the subthreshold current. This is DIBL, as can be confirmed by observing the linear dependence of log I_s with V_{ds} in the device's subthreshold output characteristic (Fig. 4.15b). The steeper slope of the linear part of these curves, compared to the output characteristic of the long-channel AlGaAs buffer device, indicate that the current is controlled by a simple DIBL mechanism as discussed in chapter 2 on page 20. This is expected in the short-channel case, where V_{ds} can have a direct influence over ψ_b at the virtual cathode (see Fig. 2.4b and c page 53). The fact that in Fig. 4.15b the slope becomes steeper as V_g is reduced indicate a shift of the co-ordinates of the virtual cathode away from the influence of the gate to a position where the coupling of the drain to ψ_b is stronger.

In the GaAs buffer device transfer characteristic (Fig. 4.14a), a similar behaviour to the AlGaAs buffer device is seen at large V_g and small V_{ds} (right hand side of the lower curves). In fact, an S_g of 270mV/decade is only slightly greater than that of the AlGaAs buffer device (240mV/decade) because of the inferior carrier confinement by the GaAs buffer.

As the gate bias is reduced below about -0.3V (left hand side of lower curves in Fig. 4.14a) another linear region is apparent with S_g = 3000mV/decade. A potential barrier controlled current, with a very weak coupling of V_g to ψ_b is indicated by this behaviour. This can be explained by the shift of the virtual cathode into the GaAs buffer as V_g becomes more negative. Another, equivalent description is of two parallel potential barriers, one in the active layer, and one in the buffer. The coupling of V_g to the active layer barrier height, ψ_b^{active} is very strong (hence the small S_g for V_g > -0.3V). As V_g is decreased, the subthreshold current over this barrier rapidly decreases below the current level over the buffer layer barrier, whose height, ψ_b^{buffer} is only weakly coupled to V_g (hence the large S_g for V_g < -0.3V).

This argument can be verified by examining the device subthreshold output characteristic (Fig. 4.15a). At small V_{ds}, DIBL in the buffer controls the current (log I_s is linear with V_{ds} with a shallow slope), with only a weak coupling of V_{ds} to ψ_b because of the large spatial separation between the virtual cathode and drain. At large V_{ds}, the level of current from DIBL in the active layer begins to predominate and the slope of the linear sections increases because the drain is now closer to the virtual cathode. The DIBL gives way to buffer leakage current for the largest V_g (top curves), as the pinch-off of the buffer is less extreme.

Conclusions

The following conclusions can be drawn from the subthreshold current measurements.

1) Buffer leakage current strongly magnifies the subthreshold current in GaAs buffer devices at useful operating biases.

2) The AlGaAs buffer eliminates subthreshold buffer current in long-channel devices.

3) In the absence of subthreshold buffer current, the long-channel AlGaAs buffer device exhibits a diffusion limited subthreshold current mechanism, a form of drain induced barrier lowering (DIBL). The same effect can be seen in the long-channel GaAs buffer device, at low V_{ds} and large V_g, where the channel is only just pinched-off.

4) In the short-channel devices, with both GaAs and AlGaAs buffers, subthreshold current control is dominated by DIBL. In the GaAs buffer device, the virtual cathode can move into the buffer, where the coupling of V_g to ψ_b is reduced and the DIBL current is many orders of magnitude larger than with comparable bias conditions in the AlGaAs buffer device.

5) The large scatter in threshold voltages in these devices frustrates a meaningful analysis of the DIBL with respect to gate-length, which could allow determination of the barrier lowering coefficients β and γ (described in section 2.3.2 on page 15).

4.5.3 Threshold Voltage Shift

In this section, the origins of the V_{ds} dependent currents in the active and buffer layers which give rise to threshold voltage shift are investigated. The threshold voltage shift is equivalent to output conductance.

A shift in the threshold voltage, V_T with increasing drain bias is expected to arise from the mechanisms of;

a) hot-electron effects widening the channel in the active layer and into the buffer layer, and increasing the current density in the channel

b) punch-through equivalent to drain induced barrier lowering (DIBL) widening the channel in the active and buffer layers

c) space charge limited (SCL) buffer layer current

d) velocity vector rotation

e) drain influence over the transverse dimension of the channel dipole

The latter two mechanisms have not been previously shown to cause such substantial threshold voltage shifts as seen in this work, and will not be considered as being significant.

In this section evidence of the DIBL and SCL mechanisms is sought, from measurements of the square-law threshold voltage shift, V_{Tsq} with increasing drain bias and further investigation of the output conductance as a function of gate-length. Evidence directly confirming hot-electron effects can not be found through such measurements.

Measurement of Threshold Voltage

Fig. 4.16 (page 155) shows $I_d^{1/2}$ plotted versus V_g with V_{ds} between 0.8 and 3.0V for 300nm gate-length GaAs and AlGaAs buffer devices respectively. V_{Tsq} was obtained from I_d versus V_g using equation 2.23 (page 14) and is plotted alongside $I_d^{1/2}$ in Fig. 4.16a. The measured values of V_{Tsq} were the maxima of the function at each drain bias, corresponding to the steepest slope of $I_d^{1/2}$ versus V_g.

In Fig. 4.16a, the long-channel 300nm GaAs buffer device displays a square law dependence of I_d with V_g (a straight line on these axes) for small values of V_{ds} (the right hand curves). As V_{ds} increases, a departure from the square law behaviour is apparent. At the smallest gate bias (V_g = -1.0V), a significant V_{ds}-dependent current flows. This is attributed to buffer layer current. The resulting shift in V_{Tsq} (the maximum slope of these curves) is therefore caused by *both* an output conductance, and a compression of the transconductance.

In Fig. 4.16b, the long-channel 300nm AlGaAs buffer device displays a strong square-law dependence of I_d with V_g, and as V_{ds} increases a small negative threshold voltage shift is observed. The shift becomes more pronounced as V_{ds} approaches 3V. However, no change in the slope of $I_d^{1/2}$ (and corresponding compression of g_m) is observed, this is attributed to a suppression of buffer layer current by the AlGaAs buffer.

In Fig. 4.17a, the short-channel 50nm GaAs buffer device displays only a weak square-law dependence, and as V_{ds} increases $I_d^{1/2}$ increases a large negative threshold voltage shift is observed. The shift becomes more pronounced as V_{ds} is incremented from 0.8 to 3.0V and the decrease of the slope of $I_d^{1/2}$ dominates the shift over the entire range of drain biases. This compresses g_m with increasing V_{ds}. The large increase of I_d with increasing V_{ds}, departing from the square law dependence, can be explained by an increase of the channel height by DIBL and/or hot-electron effects, in the active and buffer layers.

Fig. 4.17b shows a stronger square law dependence (straight, parallel lines) at low V_{ds}, but a much more severe g_m compression at large V_{ds} than the GaAs buffer device. This may be a result of the different geometry of the channel between these two devices (as can be seen from the larger open channel current of the GaAs buffer device at large V_g) giving rise to a different balance of competing short-channel effects.

The following conclusions can be drawn from these measurements.

1) In the long-channel GaAs buffer device, the threshold voltage shift appears to be dominated by buffer current, which causes a large departure from the square-law transfer characteristic.

2) In the long-channel AlGaAs buffer device, the threshold voltage shift is smaller than the GaAs buffer device because of the reduced buffer current.

3) In short-channel devices, very large threshold voltage shift is dominated by hot-electron effects and/or DIBL punch-through.

Threshold Voltage Shift

The square law threshold voltage, V_{Tsq} was determined at a range of drain biases in the current saturation range (V_{ds} = 0.8 to 3.0V). The gate bias was chosen at the peak in the V_{Tsq} function, corresponding to the maximum slope of $I_d^{1/2}$ versus V_g.

Fig. 4.18a (page 157) shows V_{Tsq} - V_{T0} versus V_{ds} for a range of GaAs buffer devices. The slope of each line, κ has a constant value up to V_{ds} ~ 2.0V for each gate-length, but between V_{ds} ~ 2.0 and 3.0V, the magnitude of the slope increases, more rapidly as the gate-length is reduced, reaching another apparently linear part in the range 2.6 to 3.0V.

The effects that are responsible for this behaviour depend strongly on the channel length both in their magnitude and non-linearity with respect to drain bias. Fig. 4.18b shows V_{Tsq} - V_{T0} versus V_{ds} for two 40nm devices, with GaAs and AlGaAs buffers. The devices were chosen because they have the same differential V_{Tsq} shift, κ at low V_{ds}. The departure from linearity at V_{ds} > 1.8V is obvious for both devices, but is more pronounced for the GaAs buffer device. This suggests that V_{ds} dependent buffer current has an important role in the threshold voltage shift for large V_{ds}. It is likely that the V_T shift in the AlGaAs buffer device is due in part to V_{ds} dependent buffer current arising from hot-electron effects, but to a lesser extent than the GaAs buffer case.

Let us now consider the linear parts of these curves in order to investigate the threshold voltage scatter, the role in the threshold voltage shift of space charge limited buffer current up to V_{ds} = 3V and drain induced barrier lowering up to V_{ds} = 2V.

Threshold Voltage Scatter

V_{T0} and κ were obtained from a least square fit to the linear part (V_{ds} = 0.8 to 2V) of the V_{Tsq} versus V_{ds} curve as the intercept value of V_{Tsq} at V_{ds} = 0 and the slope of the line respectively. Fig. 4.19a (page 158) is a plot of V_{T0} versus L_g for both GaAs and AlGaAs buffer devices.

A spread in threshold voltages of the 40 50 and 60nm gate-length GaAs buffer devices can be seen, which were fabricated on the same chip and recessed in the same batch. This can be explained by comparing Figs. 4.4 and 4.5 (pages 143 and 144). The different gate-lengths are accompanied by larger undercut profiles of the PMMA bilayer resist, because the gate linewidth was controlled by adjusting the exposure dose of a single scan of the electron beam. The large undercut allows a larger area and therefore deeper gate recess. Therefore the longer gate-lengths have larger (i.e. less negative) threshold voltages.

This graph is presented in order to emphasise the large scatter in threshold voltages of the shortest gate-length GaAs buffer devices, which was seen to dominate many of the measured parameters of these devices (such as g_m, g_d, K-value, κ, and drain delay, τ_d) when plotted against L_g. An unsuccessful attempt was made to smooth out the effect of the different threshold voltages by plotting the parameters against L_g/a. The channel layer thickness, a was approximated from V_{T0} by using the 1-D solution to Poisson's equation (see equation 2.6 page 11). This confirms that the scatter in these measured parameters is not simply a channel aspect ratio effect.

Space Charge Limited Current as a Mechanism for V_T Shift

Plots of $(-\kappa)^{-1/2}$ versus L_g and $(g_d)^{-1/2}$ versus L_g were used by Han *et al.*[19] (see page 15) to confirm that the threshold voltage shift in short-channel MODFETs originated from the SCL buffer current mechanism. These graphs are plotted using data measured in this work (Figs. 4.19b and c). In Fig. 4.19b κ was measured with a least squares fit of V_{Tsq} for V_{ds} = 0.8 to 2.0V (square symbols) and also at V_{ds} = 2.6 to 3.0V (triangle symbols). No linear relationship with $1/L_g^2$ of either g_d or κ is evident for the GaAs buffer devices, but it is the AlGaAs buffer devices. This linearity in the AlGaAs case is assumed to be coincidental, because the results of subthreshold measurements (presented in the previous section) indicate that the buffer current is totally suppressed by the AlGaAs buffer. Therefore the SCL

current mechanism is not regarded as be the mechanism responsible for the threshold voltage shift at either low (up to 2V) or high (2.6 to 3.0V) drain bias.

The scatter of values of $(-\kappa)^{-1/2}$ for the sub-100nm GaAs buffer devices in Fig. 4.19b resembles the scatter in threshold voltages in Fig. 4.19a, which means that the active layer thickness under the gate has a strong effect on the threshold voltage shift for these devices. This reinforces the suggestion that the principal cause of the threshold voltage shift is active layer current from hot-electron effects and/or DIBL punch-through, at least in the sub-100nm devices.

Drain Induced Barrier Lowering as a Mechanism for V_T Shift

If the linear threshold voltage shift with V_{ds} up to 2V is caused by DIBL, it should be possible to use the measured values of V_{T0} and κ for determining the limit, V_{dsl} of V_{ds} for saturated punch-through current using the equation

$$V_{dsl} = \frac{V_g - V_{T0}}{\kappa} \tag{4.5}$$

which can be derived by obtaining an expression for V_{dsl} in terms of V_g, V_{Tlc}, and the subthreshold barrier lowering coefficients γ and β (from equations 2.29, 2.30 and 2.33) then, by inspection of equation 2.24, equating $V_{Tlc} - \gamma$ with V_{T0}, and $-\beta$ with κ.

Values of V_{dsl} calculated from equation 4.5 were compared with the actual values observed on the output characteristics of GaAs and AlGaAs buffer devices. Devices were chosen where the observed V_{dsl} was less than 2V. For some devices the calculated value of V_{dsl} was coincident to that observed on the output characteristic, but not in most cases.

The validity of this analysis is questionable because of the difference in definition of V_{Tsc} and V_{Tsq}, from the subthreshold barrier height and square law extrapolation respectively. But some correlation between measured and calculated values of V_{dsl} should still be expected if DIBL was the dominant threshold voltage shift mechanism. However, in the subthreshold measurements presented in the previous section there was strong evidence of DIBL in the subthreshold output characteristics.

Therefore DIBL cannot be ruled out as being an important threshold voltage shift mechanism, although no direct evidence has been found here.

Hot-Electron Effects as a Mechanism for V_T Shift

A drain bias of 2V and the source-drain gap of 0.7μm in these devices corresponds to an average longitudinal electric field of ~ 30kV/cm, an order of magnitude above the critical field for velocity saturation in GaAs (E_C ~ 3kV/cm). As most of the voltage drop is across the channel (some is dropped across the series access resistances R_s and R_d, see equations 2.14 and 2.15 on page 13), the actual longitudinal field in the channel will be greater still, and dependent on the channel length. Therefore all of the devices in this study operate well into the hot-electron regime.

Voltage Gain

The voltage gain, A_V calculated from -1/κ (equation 2.26) was found to be smaller than A_V determined from g_m/g_d by a factor of 2 to 4 over all the devices measured. The difference can be attributed in part to the fact that the gate bias was chosen for maximum g_m in the g_m/g_d calculation, yet in the measurement of κ, the gate bias was chosen to maximise the slope of $I_d^{1/2}$ versus V_g, so g_m was not maximised. But more importantly, the short-channel and GaAs buffer devices' characteristics depart significantly from the simple square law behaviour in the transfer characteristic , which is a prerequisite of equation 2.26.

Conclusions

The following conclusions can be reached from the investigation of threshold voltage shift.

1) The small threshold voltage shift in long-channel GaAs buffer devices appears to be governed by buffer current. The evidence is the large departure from square-law behaviour in the transfer characteristic, which is absent in the long-channel AlGaAs buffer device. However, GaAs buffer devices over a range of gate-lengths do not exhibit the dependence of g_d and κ on L_g predicted for SCL buffer current, indicating that the buffer current is not space charge limited.

2) A reduced V_T shift is observed for longer gate-length AlGaAs buffer devices, but for the shortest gate-length devices the AlGaAs buffer has little effect on reducing the shift.

3) Shorter-channel devices exhibit a marked increase in threshold voltage shift as V_{ds} is increased above 2V. The fact that this is highly dependent on V_{T0} indicates that a the effects causing the V_T shift occur to a large extent in the active layer.

4) Threshold voltage shift is dominated by hot-electron effects (because of the very high longitudinal fields in these devices) and/or DIBL punch-through (as was revealed by the subthreshold measurements, although no direct evidence was found by examining the V_T shift). It is not possible to deduce the relative or absolute contributions of these two mechanisms using the methods described here.

5) A Monte Carlo computer simulation of the exact geometry and material structure of these devices would allow investigation of the carrier velocity and current density distributions, and would yield a better understanding of the mechanisms involved in this threshold voltage shift, particularly that of hot-electron effects.

4.5.4 High-Frequency Performance

This section presents the results obtained by S-parameter measurements in the range 45MHz to 26.5GHz of MESFETs with gate-lengths from 40 to 300nm with GaAs and AlGaAs buffers.

Short Circuit Current Gain, $|h_{21}|$

Fig. 4.20 shows the short circuit current gain, $|h_{21}|$ versus frequency, f for GaAs buffer devices with gate-lengths from 40 to 300nm. The long gate-length devices (L_g = 130, 220, 300nm ; lower three curves) show 6dB/octave roll-off, thus demonstrating the inverse proportionality of $|h_{21}|$ with f, predicted by the intrinsic equivalent circuit (equation 2.43 page 24). However, the devices with 40 and 60nm gate-lengths roll-off at a greater rate. This effect can be more clearly seen when the same data are presented with the gain-bandwidth product, $|h_{21}| \times f$ versus frequency, as in Fig. 4.21. This is equivalent to f_T at each point, measured by projecting $|h_{21}|$ (dB) to zero with a line of slope 6dB/octave. In Fig. 4.21, the degradation of current gain performance with increasing measurement frequency in the sub 100nm gate-length devices can be clearly seen. $|h_{21}| \times f$ drops from 167GHz at f = 5GHz to 146GHz at f = 25GHz.

The irregularities on the curves in Fig. 4.21 are the result of imperfect calibration arising from inconsistent electrical contact during probing of the calibration standards and subsequent measurements of the MESFETs.

This degradation of $|h_{21}|$ was still observed despite re-calibration of the network analyser. The same effect was observed for AlGaAs buffer devices with sub 100nm gate-length.

A significant feature of the sub 100nm gate-length devices is the thinner gate metallisation imposed by the use of thin resist for defining the gate. These devices have a gate height of 50nm, whereas the longer gate-length devices were able to have 150nm of metallisation. The small gate height, combined with the sub 100nm gate-length leads to a very large gate resistance. This resistance was measured for a 50nm gate (50nm gate height) by using a four-point probe (two probes passing current, two measuring voltage) as 8300Ω/mm. For comparison, a gate resistance of only 450Ω/mm has been reported[158] for a 100nm gate-length using a mushroom (or "T-gate") structure with a 300nm length of metallisation at the "cap" of the mushroom.

The very large gate-resistance is believed to be part of the mechanism responsible for this current gain degradation. However, in this experiment, at the outset the decision was made to scale the width of the gates with their length, in order to avoid producing devices with very small length and a large unit gate width, and yet making the widths as large as possible to facilitate accurate S-parameter measurements. Table 4.2 below gives the unit gate widths for these devices. This coincided with the requirement for a small exposure field for the lithography of the shortest gates. The ensuing width scaling makes it difficult to disembed the effect of gate resistance from the results.

Attenuation of the input signal as it travels along the width of the gate may reduce the effective width of the device. However, this would degrade g_m and C_{gs} at the same rate so having no effect on f_T. The resulting passive device at the end of the gate where the input signal was annihilated would have no effect on the high-frequency gain, despite passing perhaps a large DC current. Thus, simple attenuation of the input signal by the highly resistive gate is not regarded as the mechanism of current gain degradation.

Qualitatively similar behaviour to the greater than 6dB/octave roll-off can be obtained by adding a large parasitic gate resistance, R_g and drain pad capacitance, C_{dp} to the equivalent circuit of Fig. 2.5 (page 54) and calculating $|h_{21}|$ for the circuit. However, attempts to fit the sub 100nm

gate-length devices' S-parameter data to a full equivalent circuit model were unsuccessful. The model used a least squares algorithm to fit the measured S-parameters to those calculated from an equivalent circuit which included all the parasitic elements shown in Fig. 2.6 (page 55), and further included gate and source inductances, a resistance, R_{gs} in parallel with C_{gs}, and channel resistance and capacitance between R_d and the node joining C_{gs} and R_{in}. The model has obtained good fits to the S-parameter data from long gate-length MESFETs fabricated in this work[192]. Modifications to the model have been attempted[193], including a treatment based on a distributed input signal delay along the width of the gate, but acceptable fits to the sub 100nm gate-length data have not been found.

Unity Gain Cut-off Frequency, f_T

Fig. 4.22 shows the unity gain cut-off frequency, f_T versus gate-length on a log/log scale for MESFETs with gate-lengths from 40 to 300nm with GaAs and AlGaAs buffers. f_T was determined by projecting $|h_{21}|$ (dB) to zero at 6dB/octave from measurements at 10GHz.

The dashed line represents a velocity of 10^7cm/s, with f_T calculated using equation 2.46 (page 25). The values of f_T for devices with gate-lengths less than 200nm all fall below the line, with the departure from the line being most severe for the shortest gate-length devices. Note that significant velocity overshoot increasing with reduced gate-length would cause these data to rise above the line. Even taking the highest values of f_T from Fig. 4.21 for the 40 to 60nm gate-length results (at the lower measurement frequencies), they still fall well below the 10^7cm/s line.

These values of f_T falling below the constant velocity line are observed for devices which do not exhibit the current gain degradation discussed above (i.e. L_g = 100 to 130nm), which implies that a separate mechanism is responsible for this behaviour.

Interpretation of the total carrier transit time as being composed of an intrinsic part and parasitic parts (the parasitic parts being drain delay and channel charging delay) leads to the investigation presented in the next section. However, it is possible to use the f_T data to directly to obtain a qualitative description of the extent of the parasitic channel responsible for the parasitic delays.

The data given in Fig. 4.22 is given again in Fig. 4.23, but on linear axes and with a delay, τ calculated from f_T ($\tau = 1 / 2\pi f_T$). Again, the dashed line represents a velocity of 10^7cm/s. The solid line is a least squares fit to the data from both the GaAs and AlGaAs buffer devices, and the inverse of its slope yields a velocity of 1.3×10^7cm/s, which, given the scatter in the data (discussed in the next paragraph), is about equal to the value of v_{sat} in bulk GaAs, i.e. 10^7cm/s. The intercept of the line gives a parasitic delay of 0.8ps, which at this velocity gives an effective parasitic channel length of 100nm, which can be added to the gate-length to give the total channel length.

In these measurements, the drain and gate DC biases were chosen to maximise the f_T, and are therefore different for each device. This will introduce a scatter into the data, as the parasitic delays at each point are dependent on these biases. Nevertheless, the good correlation to the straight line indicate that the concept of a parasitic channel-length is valid here. The ~ 100nm parasitic channel-length is about twice the active layer thickness, and it is reasonable to interpret it as corresponding to an extension of the gate depletion region away from the ends of the gate. The next section (4.5.5) examines the origin of the parasitic delay more thoroughly.

It appears that the high frequency performance of these MESFETs is limited by short-channel effects associated with parasitic channel length. The large gate resistance further degrades the current gain performance.

Maximum Frequency of Oscillation, f_{max}

For all of the devices fabricated in this work, f_{max} was lower than f_T. There was no correlation of f_{max} with gate-length. Table 4.2 below gives the f_{max} results for the GaAs and AlGaAs buffer devices on wafers A65 and A66. These data were calculated from the same S-parameter measurements which gave the best values of f_T, presented in Fig. 4.22. The unit gate width, $Z/2$ is also given.

Table 4.2 f_{max} Results

A65 : GaAs Buffer

L_g (nm)	40	50	60	130	220	300
$Z/2$ (μm)	20	40	40	60	80	80
f_{max} (GHz)	48	44	48	47	44	42

A66 : AlGaAs Buffer

L_g (nm)	40	120	220	230	300
$Z/2$ (μm)	40	80	80	60	80
f_{max} (GHz)	40	46	42	54	39

There is no significant difference between the GaAs and AlGaAs buffer devices. All of these values of f_{max} are very low, compared to other reported results (see Table 2.1 page 49). Looking at equation 2.48 (page 25), we can see the important terms which need to be large for high f_{max} are; f_T, g_m/g_d and C_{gs}/C_{gd}. In addition R_g needs to be small.

f_{max} appears to be uncorrelated to f_T, which is highly dependent on gate-length for these devices. The voltage gain, g_m/g_d also has a large dependence on gate-length, which is not reflected in the values of f_{max}.

The equivalent circuit parameters for the 220nm gate-length AlGaAs buffer device (unit gate width, $Z/2$ = 80μm) were obtained using the model described above, fitting to the S-parameters measured at the DC bias point giving maximum f_T.

The relevant fitted equivalent circuit element values are

R_g = 40Ω (giving 1000Ω/mm for each gate)
C_{gs}/C_{gd} = 7
g_m/g_d = 14
C_{gs} = 190fF
g_m = 105mS
R_s = 1.5Ω

Inserting these values into equation 2.48 shows that the large gate resistance dominates over C_{gs}/C_{gd} and g_m/g_d in the expression for f_{max}, even in this relatively long gate-length device.

Therefore, an obvious way to improve f_{max} in these devices is to reduce the gate resistance, R_g by decreasing the unit gate width and/or using a mushroom gate ("T-gate") structure[194]. The problem with reducing the gate width is that the errors in measurements of the S-parameters may become unacceptably large for the shortest gate-length devices, for example because of the very small magnitude of the input capacitance.

In support of this argument, the data for the 220 and 230nm gate-length AlGaAs buffer devices show that for a similar gate-length, f_{max} can be improved from 43 to 54GHz by decreasing the unit gate width from 80 to 60μm. However, these devices were on different chips, and were fabricated at different times, so the correlation may be only an artefact.

Conclusions

The results of the high frequency measurements presented in this section are:

1) The shortest gate-length devices exhibit very high unity gain cut-off frequency, f_T of up to 150GHz. However, this performance falls short of that predicted by the simple model with f_T inversely proportional to gate-length. This can be explained by a parasitic channel length (~ 100nm) which adds to the total transit time in the devices.

2) No evidence of velocity overshoot effects have been found in these GaAs and AlGaAs buffer devices with high active layer doping giving $N_D = 4x10^{18}cm^{-3}$.

3) The shortest gate-length devices suffer a degradation of short circuit current gain, $|h_{21}|$ with measurement frequency up to 26.5GHz. The result is a roll-off of $|h_{21}|$ (dB) with $\log f$ at greater than 6dB/octave. This is attributed to the very large series gate resistance, R_g which may introduce a distributed delay along the width of gate. The problem with the experiment is that the width of the gates was scaled along with the length. It would have been better to keep the width constant, and vary both the length and height of the gate, in order to investigate the effects of R_g with other variables fixed. The use of a mushroom gate structure would greatly reduce R_g.

4) The devices are not optimised to give large f_{max}, which is governed by the large gate resistance in all devices.

5) The AlGaAs buffer devices have slightly inferior high frequency performance, as quantified by f_T, which can be explained by the inferior carrier transport because of the poor quality active/buffer layer interface. The f_{max} performance was dominated by large gate resistance, so the effect of the larger g_m/g_d of the AlGaAs buffer devices was not apparent.

4.5.5 Transit Time and Parasitic Delays

This section presents an investigation of the parasitic transit delays (see page 25) in MESFETs with gate-lengths from 40 to 300nm and with GaAs and AlGaAs buffers. The delays were obtained from a series of S-parameter measurements for each device at a range of gate and drain biases.

The smallest values of total transit time, τ for the results presented in this section are not always as small as the best values for the same devices presented in the previous section. This is a result of the general degradation in performance of the devices after being subjected to baking at 180C for the wiring level resist, which adversely affects the Ti/Au gate metallisation. The most extreme example of this is the 40nm gate-length AlGaAs buffer devices. The f_T at the same bias conditions of adjacent devices dropped from 123GHz to 89GHz after a 180C bake, performed before the harmful effects of the treatment were known.

Measurement of Parasitic Delays

Fig. 4.24 (page 163) shows examples of of the measurements used to extract a) the parasitic drain delay, τ_d and b) the parasitic channel delay, τ_r. The total transit time, τ is calculated from f_T ($\tau = 1 / 2\pi f_T$). The method of extracting these delays from the data is shown graphically in Fig. 2.7 (page 56). The straight lines were obtained with a least squares fit to the last few points (right hand side) on each graph. The errors obtained from these fits, along with the error in determining f_T (see Fig. 4.21 page 160), mean that the values of the delays (in ps) can only be given with an accuracy of one decimal place.

Fig. 4.25 (page 164) graphically presents the results of the parasitic delay extraction for MESFETs with gate-lengths from 40 to 300nm and with GaAs and AlGaAs buffers.

Drain Delay

Fig. 4.25a shows the drain delay against gate-length. There is a large scatter in the data, which corresponds to the scatter in threshold voltage (Fig. 4.19a page 158). In fact, when the drain delay, τ is plotted against threshold voltage V_{T0} in Fig. 4.26 (page 165), an almost linear relationship between the two is observed. The largest drain delay corresponds to the most shallow recess depth. If the drain delay is caused by an extension of the gate depletion region towards the drain with increasing V_{ds}. The increase of the channel length, L_d can be approximated by

$$L_d = [\, 2\varepsilon (\phi + V_{ds}) / qN_D \,]^{1/2} \qquad (4.6)$$

where $\phi = - V_g + V_{Bi}$ is the Schottky barrier potential.

The drain delay can be calculated from equation 4.6 and $\tau_d = L_d / v_{eff}$. For the wafer A65, $N_D = 4.1\text{x}10^{18}\text{cm}^{-3}$, $v_{eff} = 1.1\text{x}10^{7}\text{cm/s}$, $\phi = 0.53\text{V}$ (see section 4.7.2 page 137). With $V_{ds} = 1.5\text{V}$ the drain delay thus calculated is relatively insensitive to V_g. For example with $V_g = 0$, $\tau_d = 0.24\text{ps}$, with $V_g = -2\text{V}$, $\tau_d = 0.34\text{ps}$, and with $V_g = -10\text{V}$, $\tau_d = 0.59\text{ps}$. This demonstrates that that the scatter of τ_d in Fig. 4.26 is not a consequence of to the optimisation of V_g in the drain delay measurements for each device to obtain the best f_T. In the case of the shallow recess devices (with most negative V_{T0}), a more negative V_g was needed, but no where near -10V or beyond. A small average velocity in the extension of the channel towards the drain could explain the large drain delays, but the high longitudinal fields in these devices, particularly near the drain end of the gate, precludes such low velocities.

Two mechanisms which can combine to account for this considerable influence of V_{T0} on τ_d are a lengthening of the channel by the surface depletion and fringing of the transverse gate field. Devices with small recess depths (with most negative V_{T0}) would be more severely affected by both of these mechanisms as is seen in Fig. 4.26.

Channel Charging Delay

Fig. 4.25b shows the channel charging delay against gate-length. The delay is larger (by about a factor of two) for the GaAs buffer devices, except for the 40nm devices. This may be caused by a large proportion of carriers flowing into the channel through the GaAs buffer, with the longer path of carriers resulting in a longer channel charging delay. The sub 100nm gate-length devices with both types of buffer have the largest channel

charging delays. This may arise from a similar mechanism, with hot-electron effects causing carrier injection through depleted regions, perhaps including the AlGaAs buffer.

Intrinsic Channel Transit Time

Fig. 4.25b shows the intrinsic channel transit time, τ_i against gate-length. The slope of the lines, which are least square fits to the three longest gate-lengths, give intrinsic velocities of 1.1×10^7 and 0.9×10^7cm/s for the GaAs and AlGaAs buffers respectively. The slightly lower velocity on the AlGaAs buffer case may be a result of mobility degradation near the poor quality active/buffer layer interface (see the discussion of transconductance degradation on page 112).

The most remarkable feature of these results is the small values of τ_i. The intercepts of the lines give negative intrinsic effective channel lengths (-100 and -70nm respectively for the GaAs and AlGaAs buffer devices). These results show that carriers travel at about 10^7cm/s in an intrinsic channel which is about 100nm less than the gate-length. The sub 100nm gate-length devices do not have negative values of τ_i, but they are almost zero, corresponding to a very small intrinsic channel length of ~ 20nm (or incredibly high velocities), and the parasitic drain and channel charging delays have the largest influence on the total transit time.

This intrinsic channel is assumed to be positioned under the gate, at the drain end, where the longitudinal fields are highest. Therefore in the region under the source end of the gate, the average carrier velocity is low. Two possible reasons for the low average carrier velocity in this region are; a) the carriers are still accelerating under the influence of the longitudinal field, and b) the longitudinal field strength is less than the critical field for velocity saturation. The very high longitudinal fields in these devices resulting from the short source-drain gap make it hard to justify the latter explanation. A Monte Carlo computer simulation of these devices could give the electric field distribution, which would clarify the mechanism. In addition, a carrier velocity distribution thus obtained would validate these measurements.

Conclusions

The conclusions that can be drawn from the measurement of parasitic transit delays presented in this section are:

1) The parasitic drain delay, τ_d is a strong function of the recess depth (as characterised by threshold voltage), which points to lengthening of the channel by the surface depletion and fringing of the transverse gate field as being the most significant contribution to the drain delay.

2) Carriers flowing from the source to the channel via a long and high resistivity path through the GaAs buffer, result in a channel charging delay, τ_r approximately double that of the AlGaAs buffer case for the longer channel devices.

3) The very small intrinsic transit delays, τ_i obtained indicate that in a region under the source end of the gate, the average carrier velocity is low, perhaps because the carriers are still accelerating under the influence of the longitudinal field, or (less likely) because the longitudinal field strength is less than the critical field for velocity saturation. The length of this region reduces the intrinsic channel length to ~ 100nm less that the gate-length, tending to ~ 20nm the gate-length decreases below 100nm. This may be an explanation of the relatively poor values of f_T as the gate-length was reduced below 100nm.

4.6 Interrupted Growth $Al_{0.3}Ga_{0.7}As$ Buffer

MESFETs with ~ 130nm gate-length were fabricated on three wafers with nominally identical active layer thicknesses, the first with an undoped GaAs buffer (A65), the second with an undoped $Al_{0.3}Ga_{0.7}As$ buffer (A66) and the third with an undoped $Al_{0.3}Ga_{0.7}As$ buffer including four growth interruptions (A76). In this section DC and high frequency characterisation are used to compare these devices. The growth interruptions in the latter wafer are expected to improve the active/buffer layer interface quality.

4.6.1 DC characteristics

Figs. 4.27 and 4.28 (pages 166 and 167) show the output and transfer characteristics respectively of GaAs MESFETs with GaAs, AlGaAs and interrupted growth (IG) AlGaAs buffers. In these characteristics, the advantage of the AlGaAs buffer is demonstrated by the good pinchoff,

whereas the GaAs buffer device shows a punch-through beyond V_{ds} ~ 0.8V. Surprisingly, the IG AlGaAs buffer device also exhibits punch-through beyond V_{ds} ~ 1.0V. Its transfer characteristic (Fig 4.28c) shows a subthreshold current independent of gate bias (V_g < -0.8V). This indicates that the punch-through current does not flow through the buffer layer under the gate. It could be explained by a gate with a break near one end, but this was disproved by a SEM examination (see Fig. 3.13 page 103, an electron micrograph of the adjacent device to the one considered here). It is more likely that the gate bias dependent leakage is caused by a slightly inadequate mesa etch depth, resulting in incomplete isolation of the source and drain probing pads.

The parameters extracted from these measurements are give below in Table 4.3.

Table 4.3 Performance of interrupted growth AlGaAs buffer MESFETs

Wafer (buffer)	L_g nm	$Z/2$ μm	K mS/ Vmm	g_m mS/ mm	g_d mS/ mm	A_V	f_T GHz	f_{max} GHz
A65 (GaAs)	130	60	235	610	71	9	99	47
A66 (AlGaAs)	130	60	625	507	45	11	87	47
A76 (AlGaAs*)	120	60	595	600	43	14	103	59

NOTES.
* Buffer grown with 4 interruptions (GaAs monolayer).

The K-value is low for the GaAs buffered device compared to the AlGaAs buffer devices, because of the worse carrier confinement in the active layer by the GaAs buffer.

The transconductance is high (~ 600mS/mm) for the GaAs and IG AlGaAs buffer devices, but 20% lower for the AlGaAs buffer device. This demonstrates that the growth interruptions serve to improve the active/buffer layer interface to give an active layer quality approaching that of the layer with the GaAs buffer (recall the discussion of transconductance degradation associated with the AlGaAs buffer on page 112). Some mobility degradation near the IG AlGaAs buffer for this wafer is indicated in Fig. 4.1 (page 140)

Nearly identical output conductances of the two AlGaAs buffer devices are 40% lower than the GaAs buffer device. This is consistent with the findings of section 4.5.1, which ascribed the large output conductance to current in the GaAs buffer.

The superior transconductance of the IG AlGaAs buffer device gives it the best voltage gain, $A_V = g_m/g_d$ of 14.

4.6.2 High-Frequency performance

S-parameter measurements of the three devices, DC biased to give the best f_T, are given in Table 4.3 above.

The interrupted growth AlGaAs buffer device has an identical f_T to the GaAs buffer device, after scaling for the slightly shorter gate-length. The 13% lower f_T of the AlGaAs buffer device is attributed to the lower transconductance.

The IG AlGaAs buffer device has a higher f_{max} (59GHz) than the other devices (47GHz). It is the highest value measured for any of the MESFETs fabricated in this work. This is not a result of a thicker gate metallisation, so it may result from a combination of this device's increased g_m/g_d and other factors such as smaller source and drain contact resistances or the gate recess geometry (which can increase the C_{gs}/C_{gd} ratio[159]).

Conclusions

The conclusions from the comparison of the GaAs, AlGaAs and interrupted growth AlGaAs buffer MESFETs in this section are:

1) Growth interruptions in an AlGaAs buffer bring the DC and high-frequency performance of MESFETs as quantified by g_m and f_T up to that of a GaAs buffer devices.

2) The growth interruptions do not adversely affect the carrier confining properties of the AlGaAs buffer layer, as quantified by K-value and g_d.

4.7 Variation of Channel Doping Concentration

MESFETs with ~ 200nm gate-length were fabricated on three wafers with nominally identical active layer thicknesses and undoped GaAs buffer layers, with active layer (Si) ionised donor concentration, N_D of 2.2, 4.1 and $7.1 \times 10^{18} cm^{-3}$, as determined from the sheet carrier concentration (see section 4.1 page 107). In this section DC and high frequency characterisation are used to compare these devices.

4.7.1 DC characteristics

Figs. 4.29 and 4.30 (pages 168 and 169) show the output and transfer characteristics respectively of GaAs MESFETs with GaAs buffers and N_D = 2.2, 4.1 and $7.1 \times 10^{18} cm^{-3}$. The trend of larger current with increasing N_D is clear in these characteristics.

The parameters extracted from these measurements are give below in Table 4.4.

Table 4.4 Performance of MESFETs with varied active layer doping

Wafer	N_D 10^{18} cm^{-3}	L_g nm	$Z/2$ μm	K mS/ Vmm	g_m mS/ mm	g_d mS/ mm	A_V	f_T GHz	f_{max} GHz	$L_g 2\pi f_T$ 10^7cm/s
A114	2.2	200	60	384	437	38	11.5	92	58	1.2
A65	4.1	220	80	372	547	49	11	72	44	1.0
A128	7.1	200	80	199	370	47	8	72	29	0.9

The K-value and g_m are low for the highest N_D device, because of the not optimum (very negative) threshold voltage, resulting from too shallow a recess for the very high active layer doping. The two lower doped devices have similar DC performance as quantified by these parameters.

4.7.2 Gate Diode Characterisation

Fig. 4.31 (page 170) shows the gate diode characteristics of the three devices. A large rise in the level of reverse diode leakage current is apparent as N_D increases, which can be explained by the reduction of height and thickness of the gate Schottky barrier with increasing doping (see section 2.6.4 page 42).

The characteristic of the lowest doped device indicates that an interfacial layer of contamination was deposited immediately before the Ti gate metal during gate fabrication. The resulting metal-insulator-semiconductor structure frustrated extraction of the diode ideality factor, n and diode built in voltage, V_{Bi} from the forward bias (positive V_g) part of the characteristic. These parameters were extracted[132] for the other two devices. For N_D = 4.1 and 7.1x10^{18}cm^{-3}, the doide ideality factor, n rises from 2.2 to 3.2 and the built in voltage V_{Bi} falls from 0.53 to 0.44. These poor values are a consequence of the high doping concentration of the active layer.

The gate reverse leakage currents in the open channel operating range are not large enough to degrade DC and high-frequency performance.

4.7.3 High-Frequency performance

f_T and f_{max} from S-parameter measurements of the three devices, DC biased to give the best f_T, are given in Table 4.4 above.

Reduced transit time with lower active layer doping is demonstrated by the rise of the effective velocity $L_g 2\pi f_T$ with decreasing N_D. However, one would expect a reduced effective velocity in the low doped active layers because of the more severe parasitic channel length caused by surface depletion and gate fringing effects.

The method of parasitic delay extraction used in section 4.5.5 was applied to these devices. With increasing N_D, τ_d was determined as 0.5, 0.3 and 0.7ps. The lack of correlation to N_D is a result of the different recess depths (and therefore threshold voltages which can be seen in Fig. 4.30 page 169), which was previously found to strongly affect the drain delay in section 4.5.5. With increasing N_D, τ_r was determined as 0.9, 0.8 and 0.5ps. The reduction of τ_r with increasing N_D is because of the lower resistivity of the active layer. These results yield values of intrinsic transit time, τ_i of 0.3, 1.1

and 1.0ps for these devices with increasing N_D. The small value of τ_i for the low doped device may be related to the interfacial layer under the gate which was discussed above.

This analysis leads to the conclusion that the increase of f_T with reduced N_D despite the worsened parasitic delays is the result of improved carrier transport. It appears that the very high doping can degrade the average carrier velocity. In the low doped case, the larger average velocity is able to overcome the more severe parasitic delays to give shorter total transit times.

The insulating interfacial layer apparent in the lowest doped device does not degrade the value of f_T. In an application where the device was used to process or amplify a signal with a low frequency component, interface states associated with the interface would probably degrade the system performance. This is why MOSFET like structures cannot be fabricated from GaAs.

The behaviour of f_{max} is clearly superior as N_D is reduced. However, some of the improvement in the lowest doped device is a result of a smaller gate resistance because its unit gate width, $Z/2$ is only 60μm, compared to 80μm for the other devices. In Table 4.3 (page 128) an improvement in f_{max} from 43 to 54GHz is observed as $Z/2$ is similarly decreased from 80 to 60μm (for the 220 and 230nm gate-length AlGaAs buffer devices respectively).

An improvement of f_{max} is expected in a device with a lower doped (or thinner) active layer between gate and drain because of the increase of C_{gs}/C_{dg}[159]. The equivalent circuit parameters were obtained for these devices from S-parameters measured at the DC bias giving the highest f_T. With increasing N_D the ratio C_{gs}/C_{gd} was 11.5, 9.0 and 6.8.

The extracted values of R_g were 33, 33 and 67. The large R_g (67Ω) may also be related to the interfacial layer under the gate, and would explain the low f_{max} of the most highly doped device (34GHz) relative to the others.

Conclusions

The conclusions from the comparison of the GaAs buffer MESFETs with varied active layer doping in this section are:

1) Increasing the doping concentration causes an increased gate diode ideality factor and a lowered Schottky barrier height, but the gate reverse leakage currents in the open channel operating range are not large enough to degrade DC and high-frequency performance.

2) The observed increase of f_T with reduced N_D despite the worsened parasitic delays is the result of improved carrier transport. It appears that the very high doping can degrade the average carrier velocity. In the low doped case, the larger average velocity is able to overcome the more severe parasitic delays to give shorter total transit times.

3) An observed increase in f_{max} with reduced N_D may be due a increased C_{gs}/C_{gd} ratio.

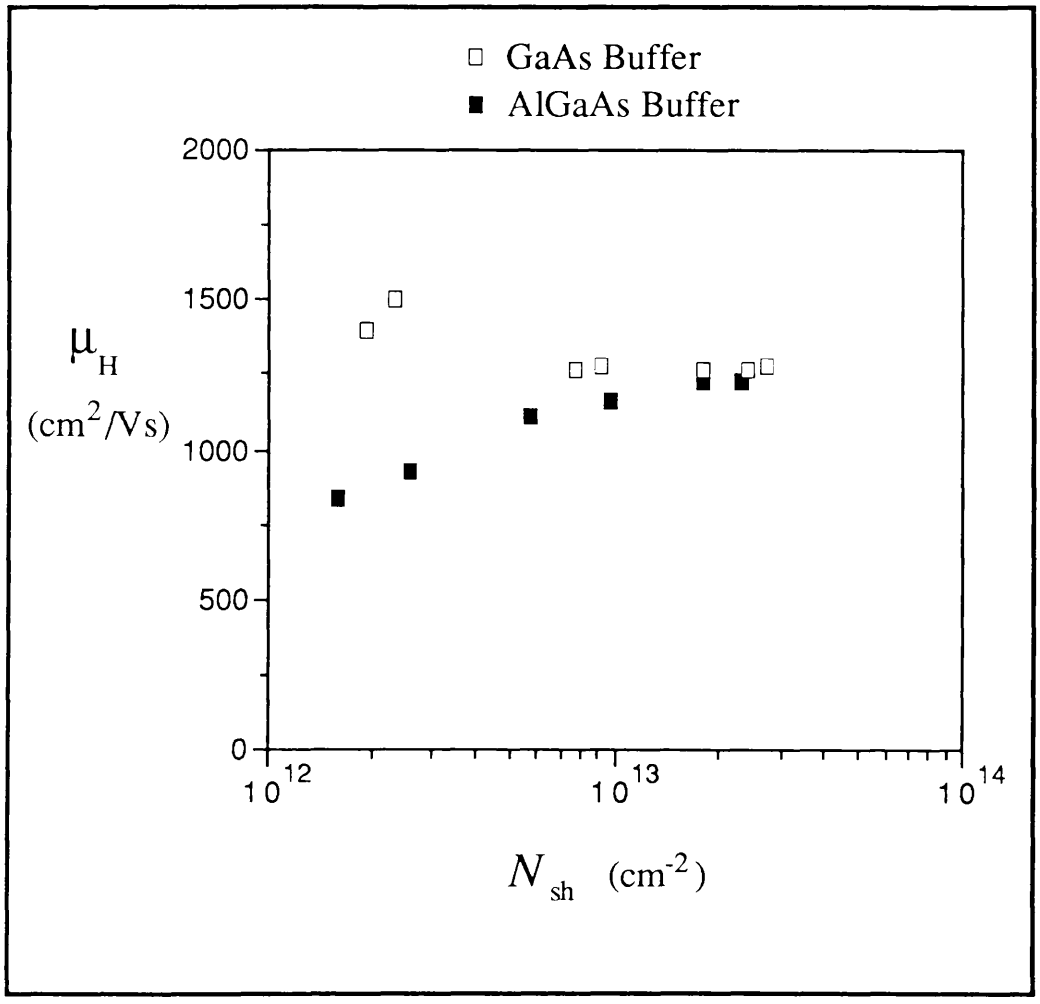


Figure 4.1 Hall mobility profile with GaAs and AlGaAs buffers
(from Cameron *et al.*[188])

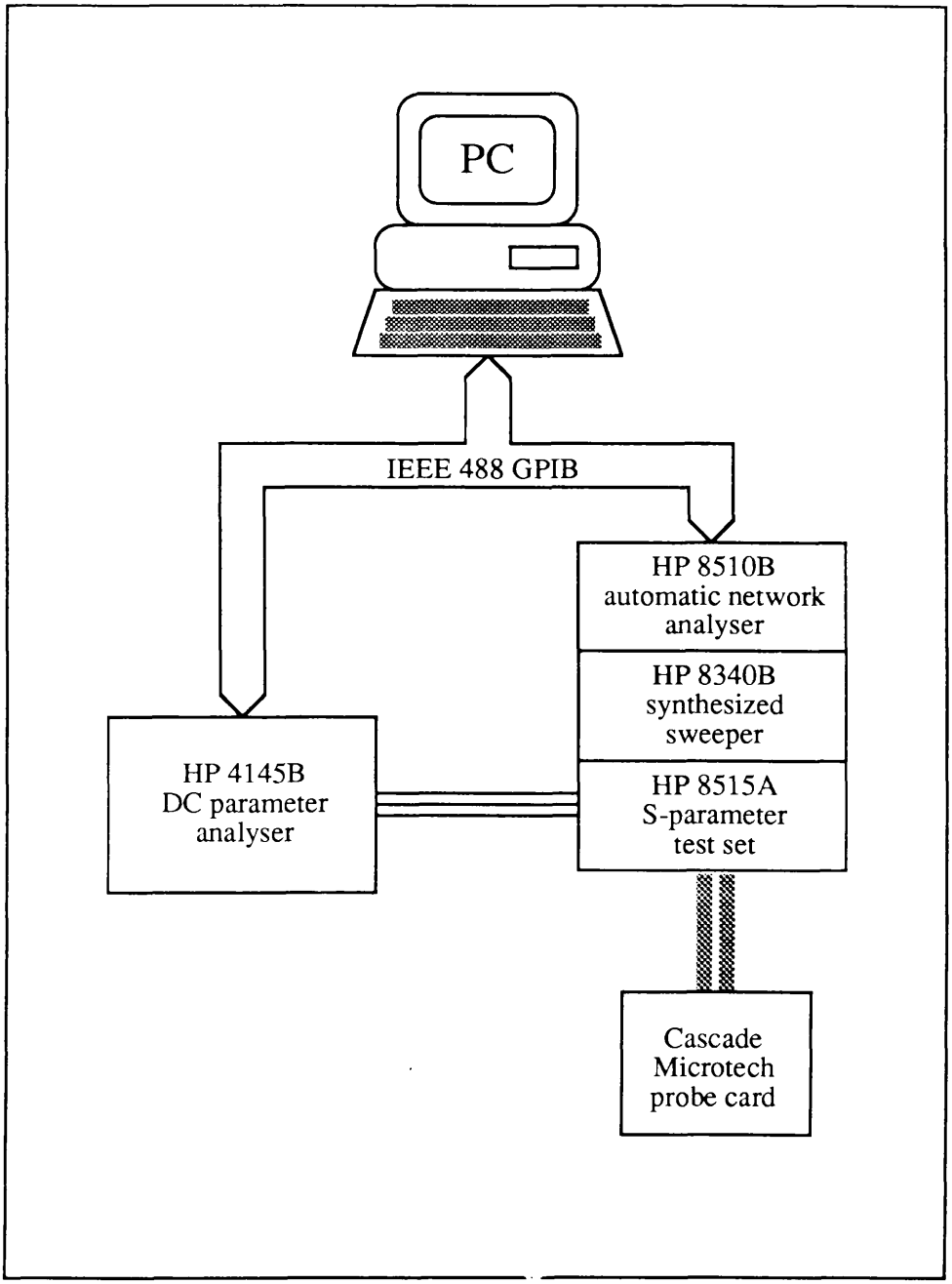


Figure 4.2 DC and high-frequency measurement system

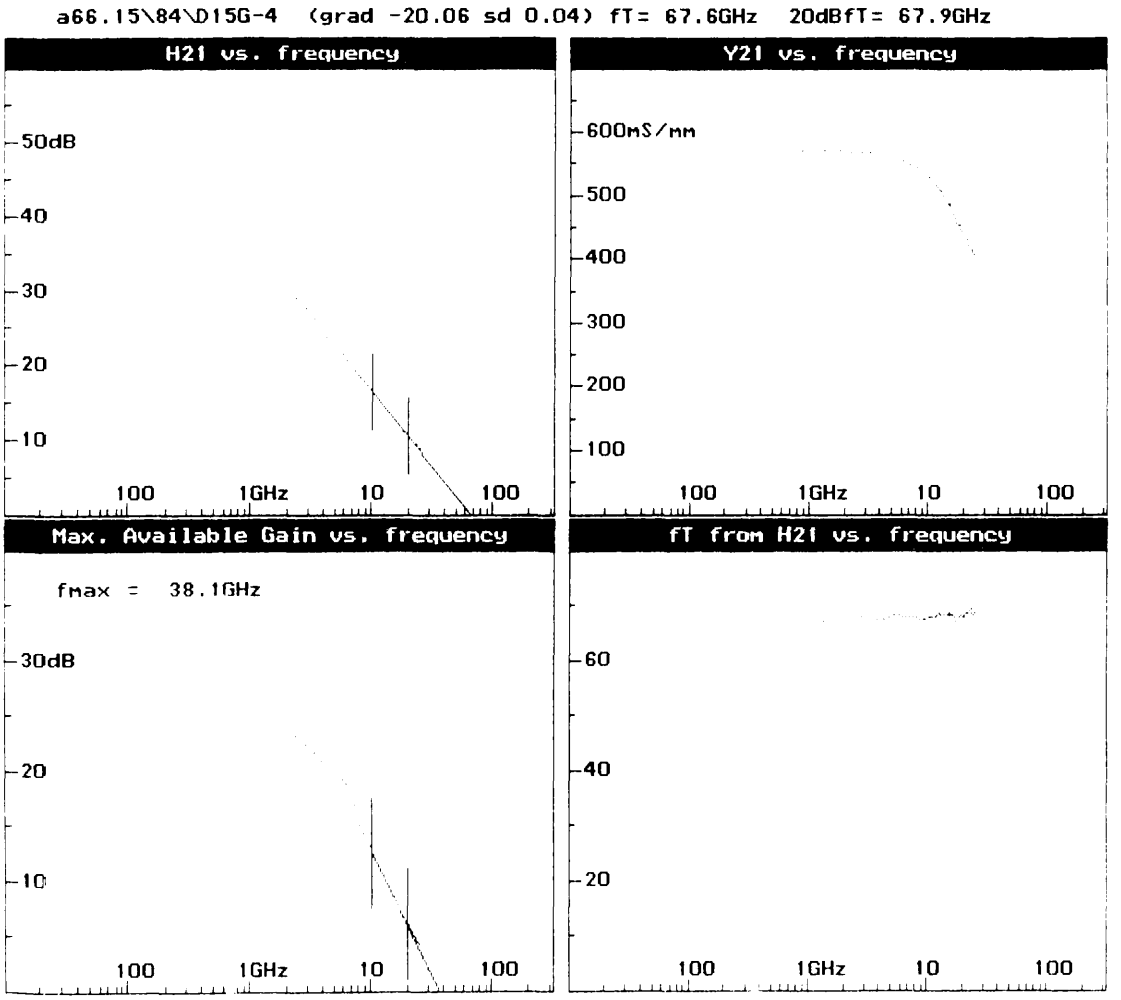


Figure 4.3 Screen dump from S-parameter analysis program

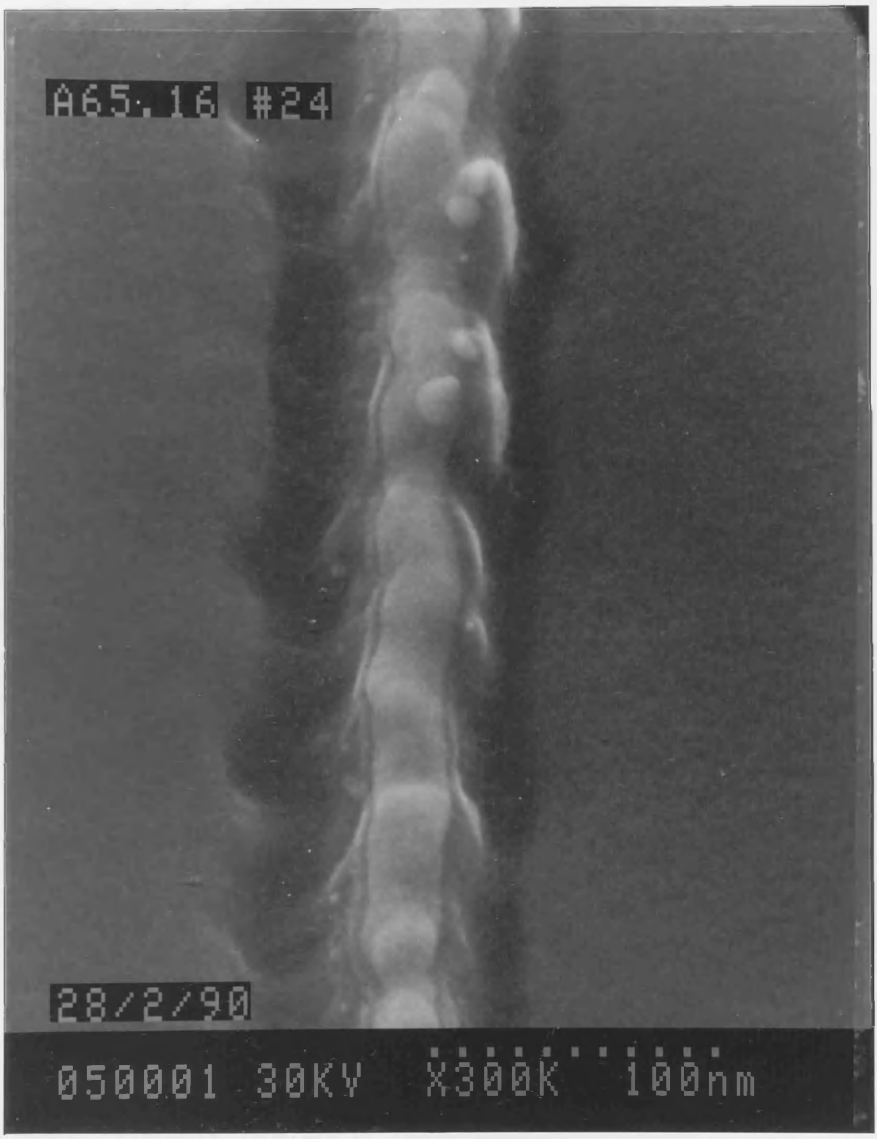


Figure 4.4 Electron micrograph of a 40nm gate

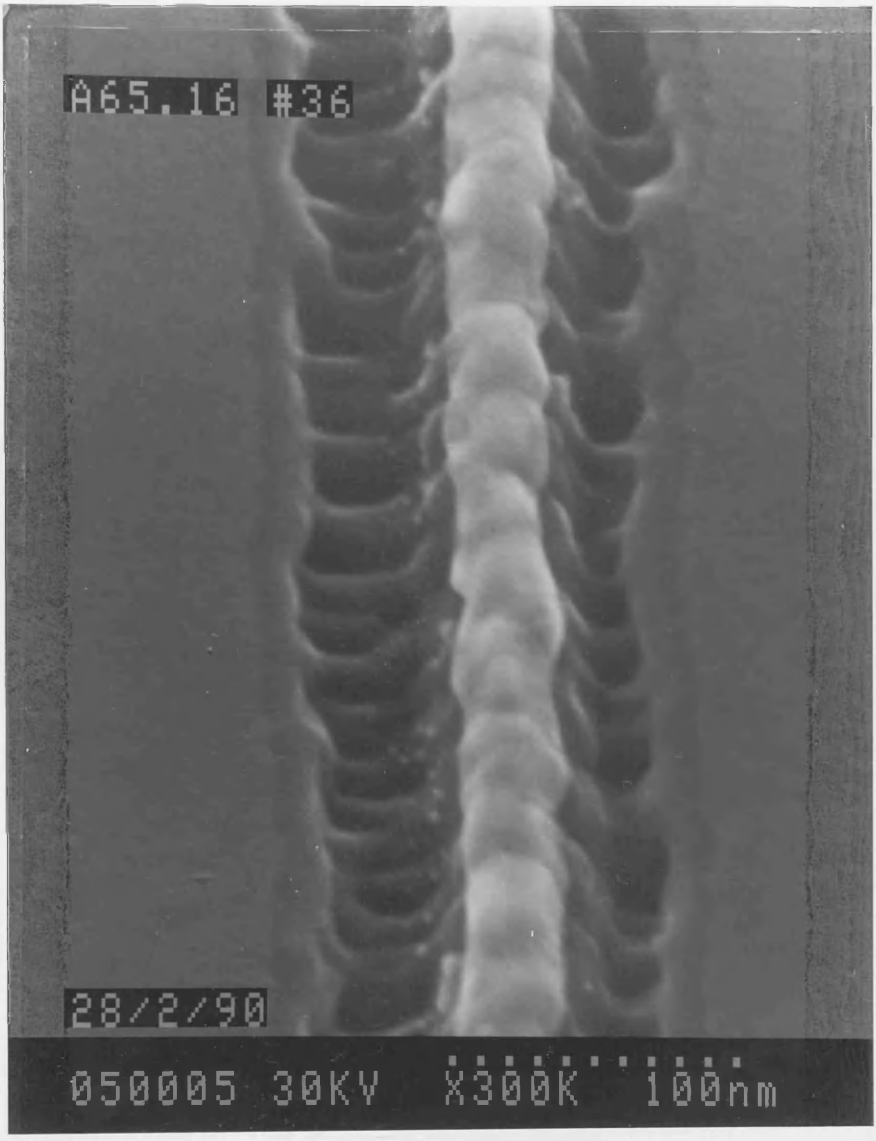
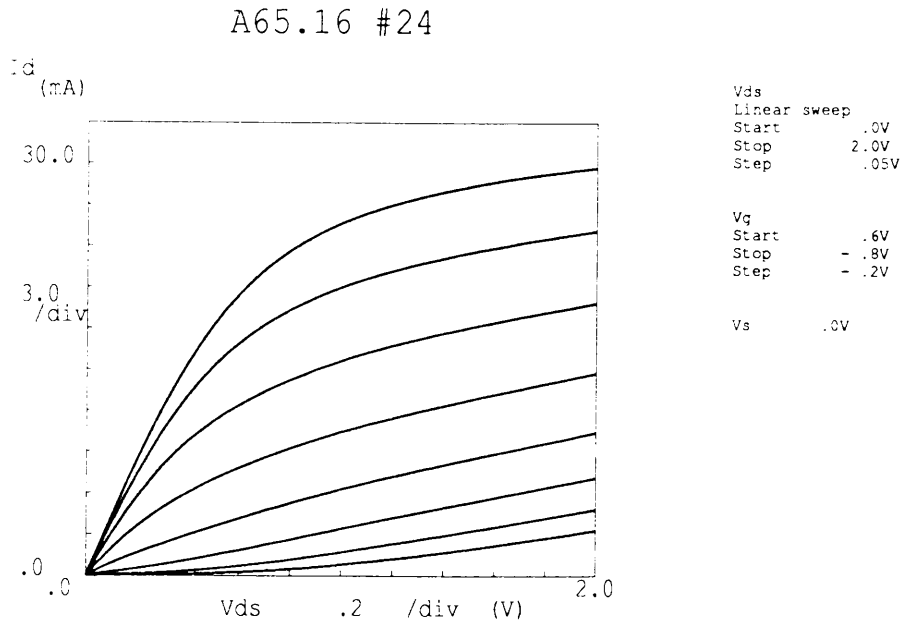
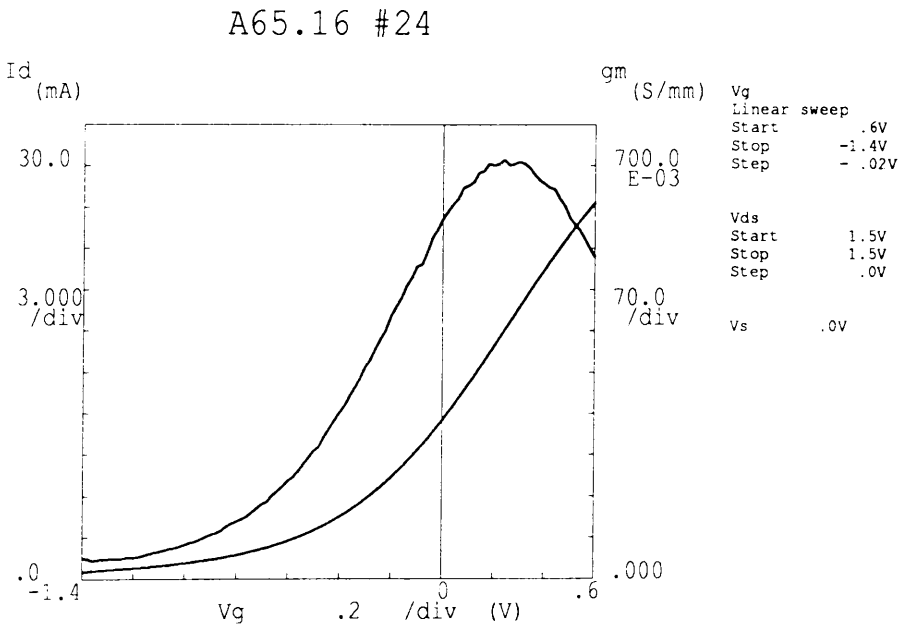


Figure 4.5 Electron micrograph of a 50nm gate

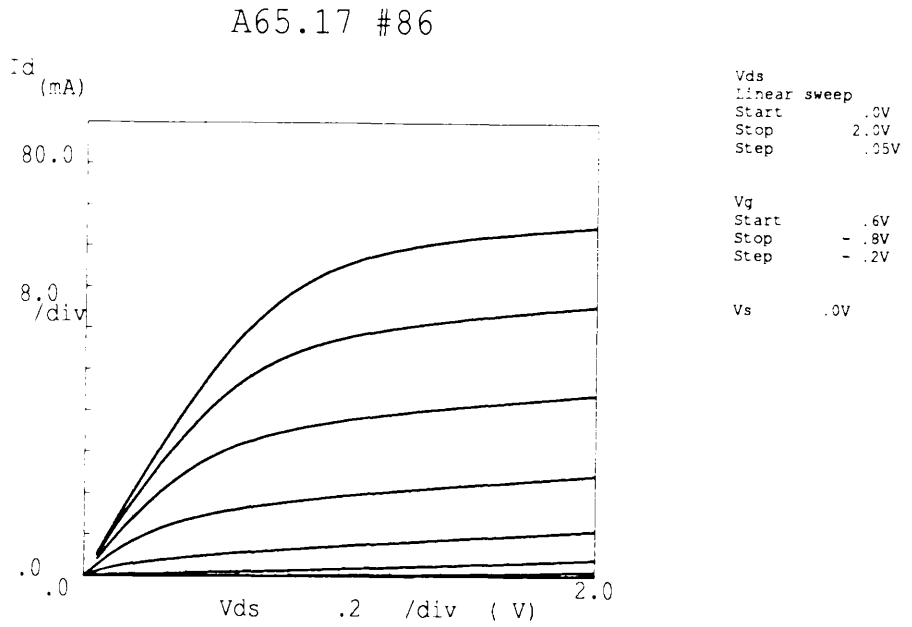


a) output characteristic

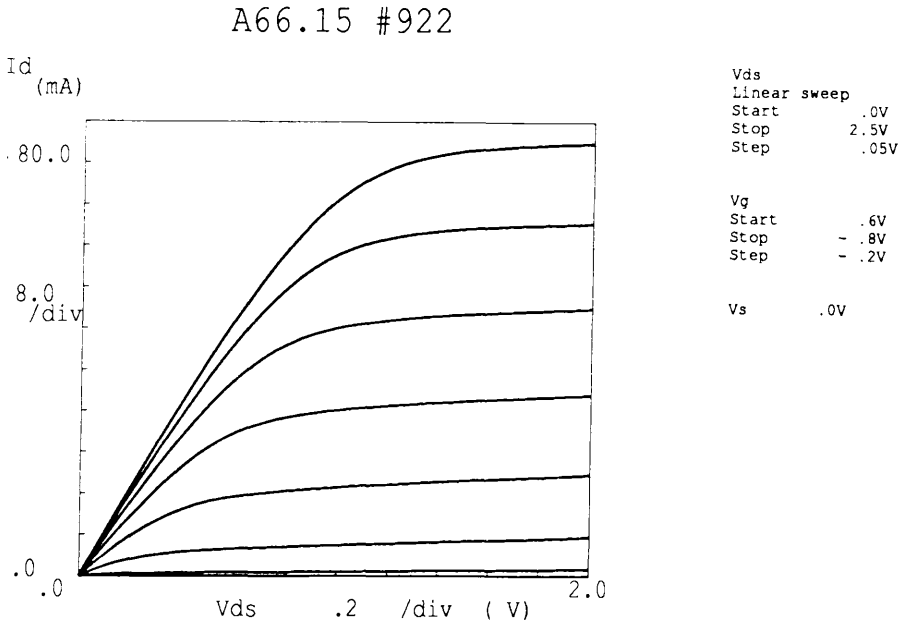


b) transfer characteristic (upper curve is g_m)

Figure 4.6 Short gate-length MESFET DC characteristics
GaAs buffer, L_g = 40nm, Z = 40μm

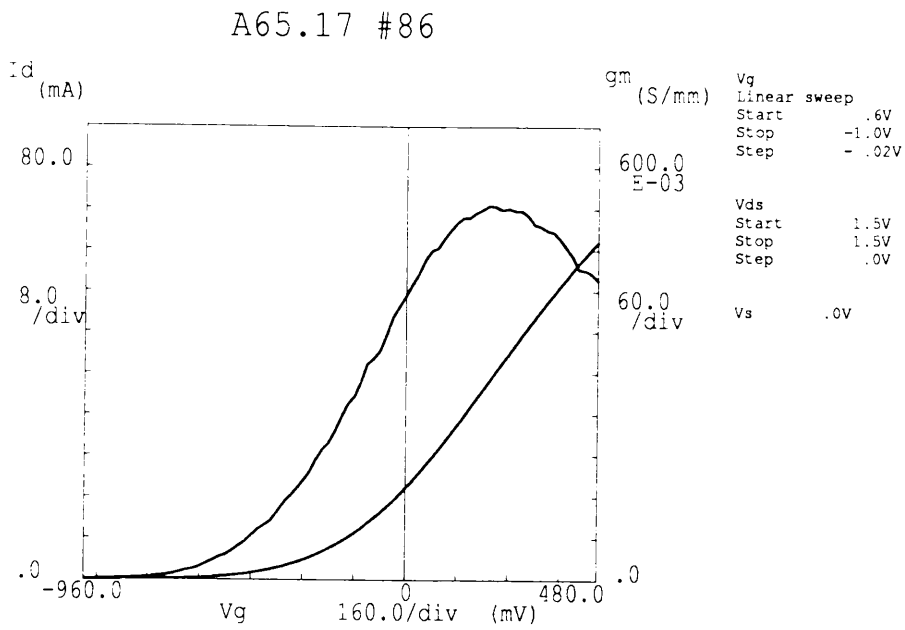


a) GaAs buffer, L_g = 300nm, Z = 160μm

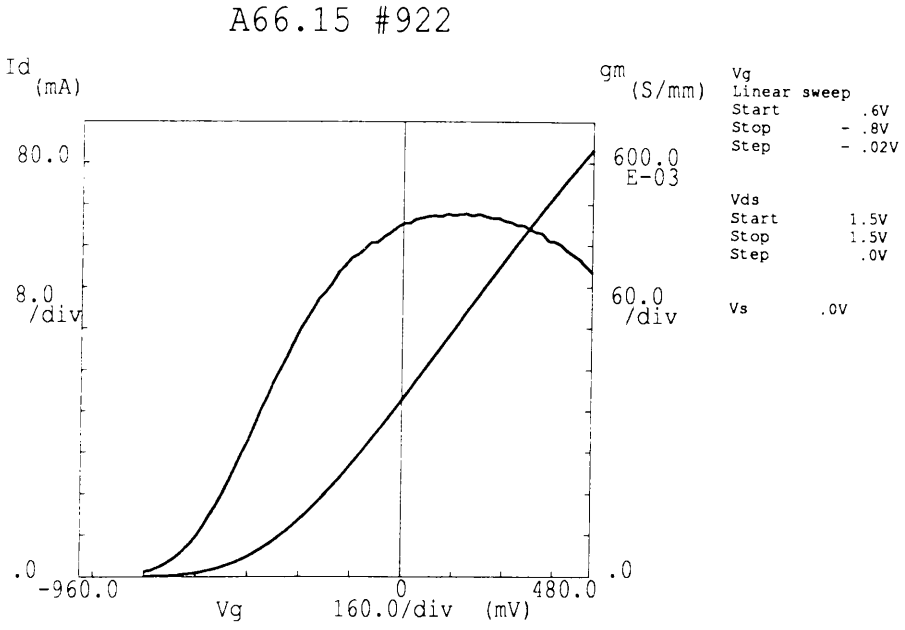


b) AlGaAs buffer, L_g = 300nm, Z = 160μm

Figure 4.7 MESFET output characteristics (long-channel).

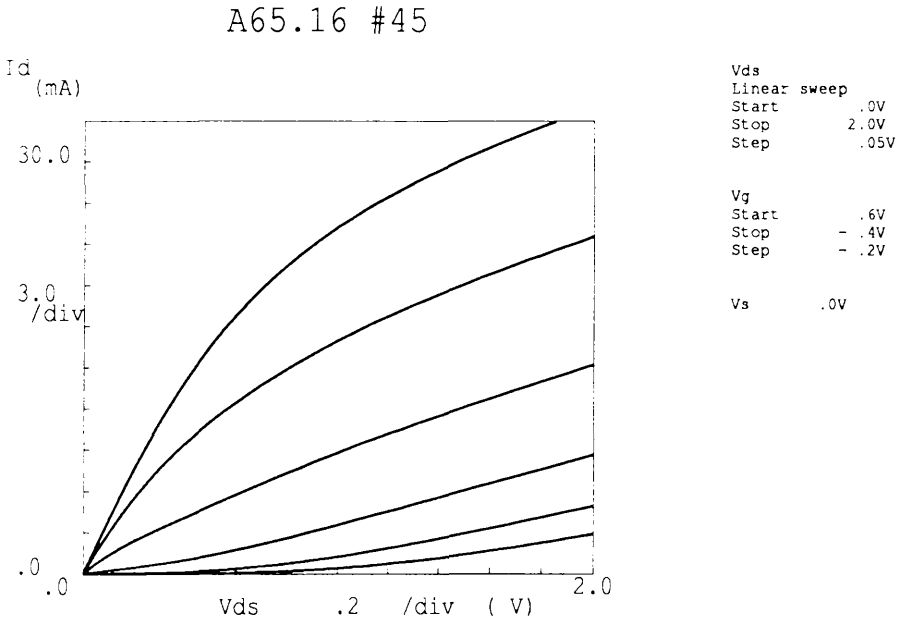


a) GaAs buffer, L_g = 300nm, Z = 160μm

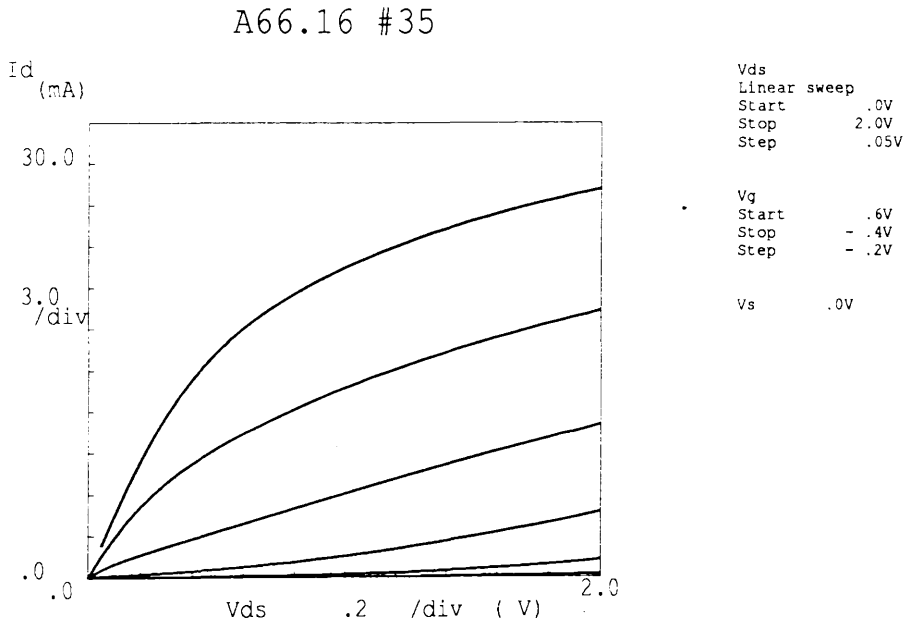


b) AlGaAs buffer, L_g = 300nm, Z = 160μm

Figure 4.8 MESFET transfer characteristics (long-channel)
(upper curves are g_m)

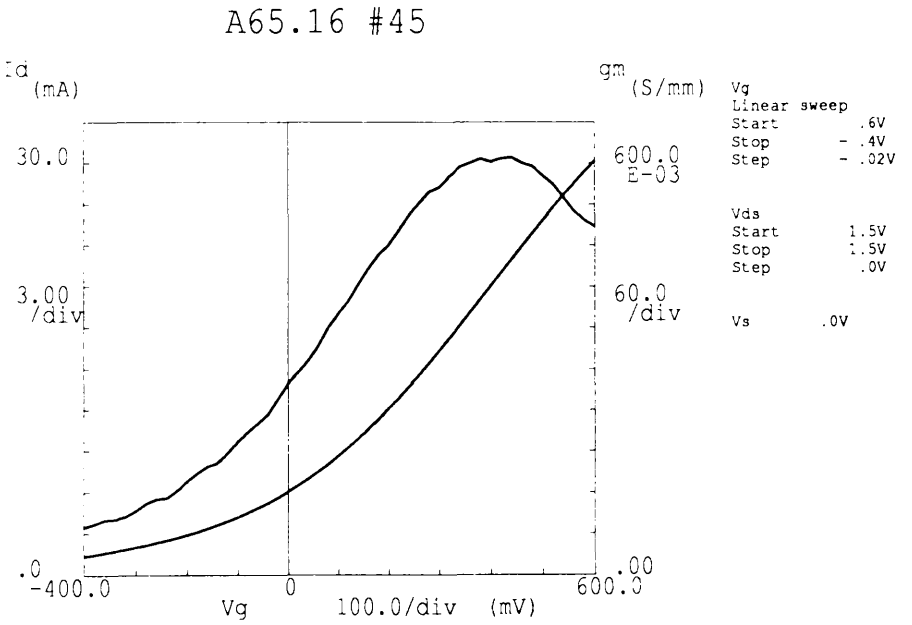


a) GaAs buffer, L_g = 60nm, Z = 80μm

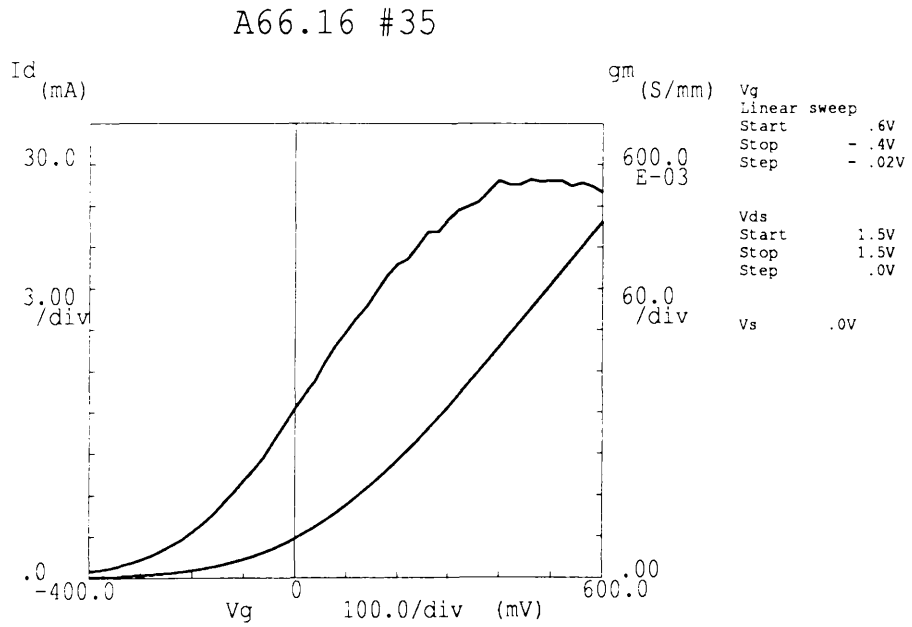


b) AlGaAs buffer, L_g = 50nm, Z = 80μm

Figure 4.9 MESFET output characteristics (short-channel)

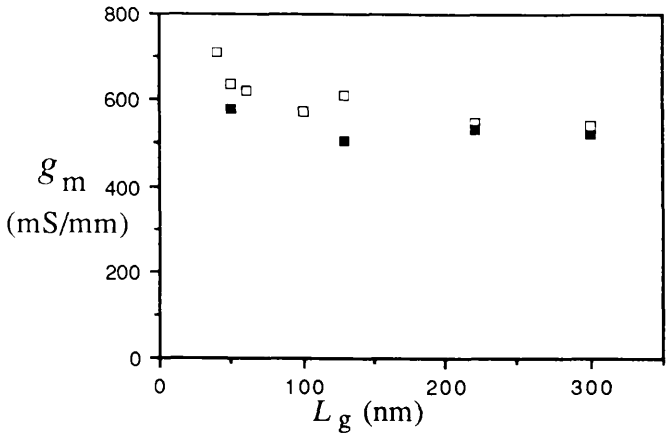


a) GaAs buffer, L_g = 60nm, Z = 80μm

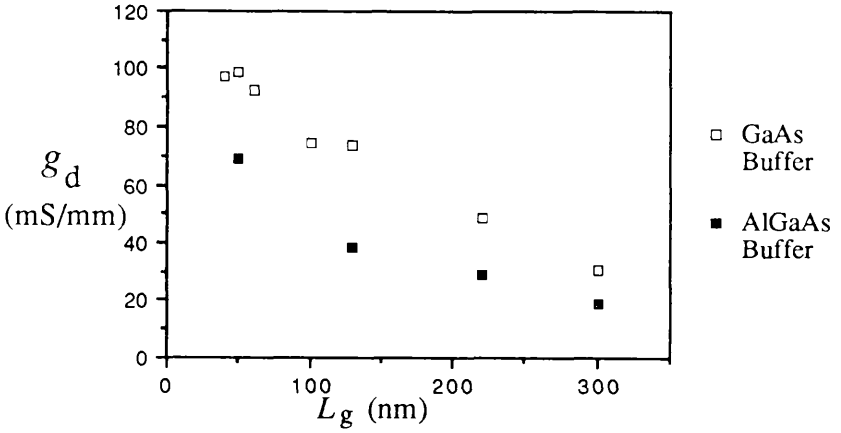


b) AlGaAs buffer, L_g = 50nm, Z = 80μm

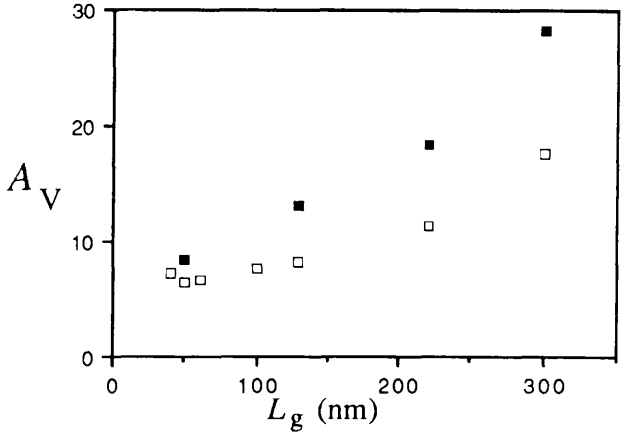
Figure 4.10 MESFET transfer characteristics (short-channel)
(upper curves are g_m)



a) peak extrinsic transconductance versus gate-length

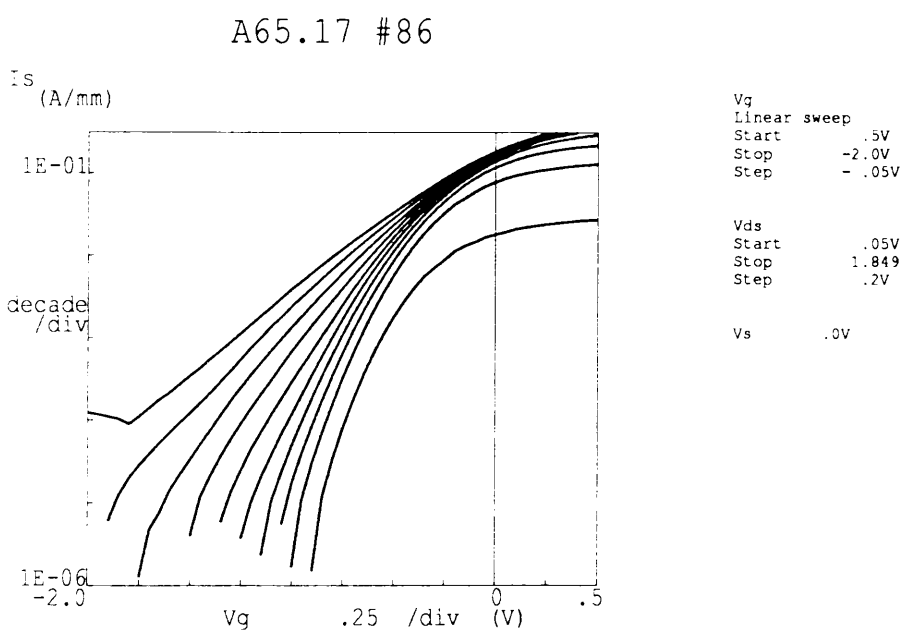


b) output conductance versus gate-length

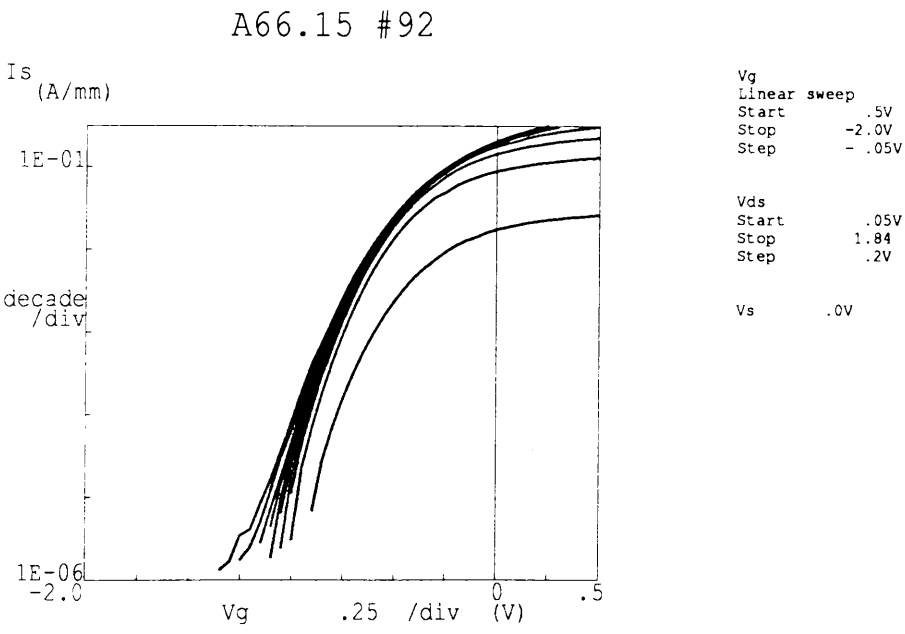


c) voltage gain versus gate-length

Figure 4.11 g_m, g_d **and** A_V **versus** L_g **with GaAs and AlGaAs buffers**

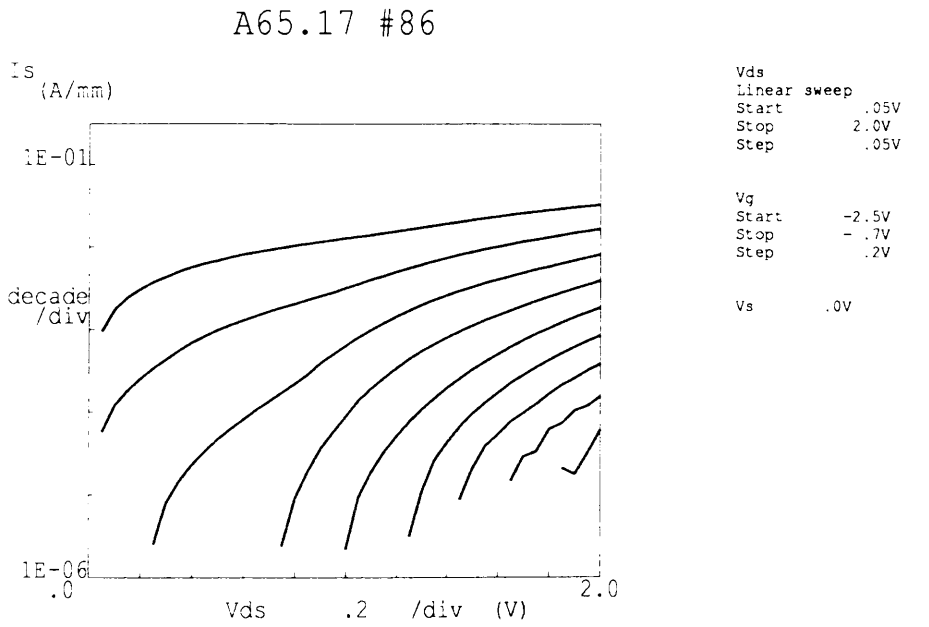


a) GaAs buffer, L_g = 300nm, Z = 160μm

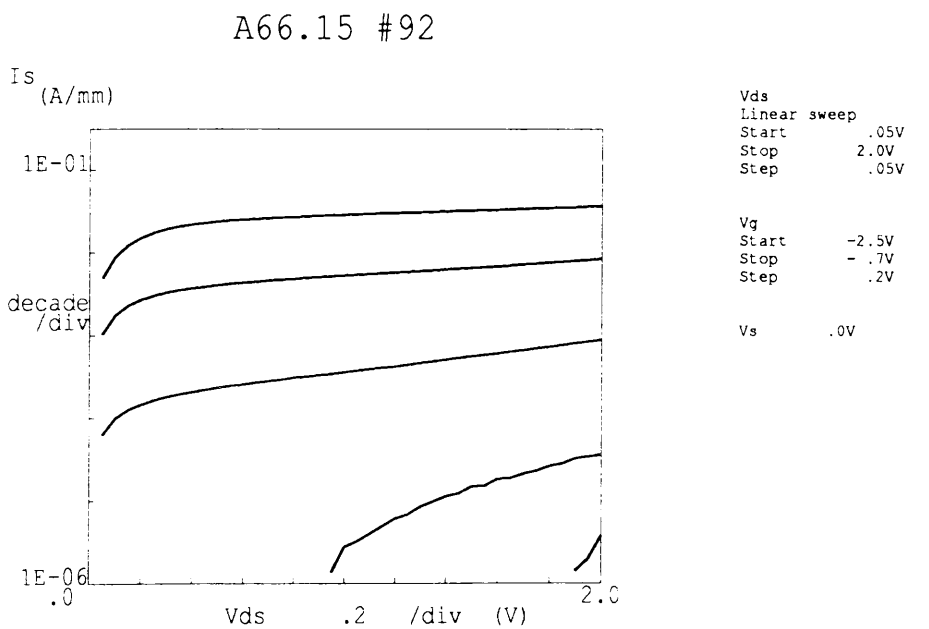


b) AlGaAs buffer, L_g = 300nm, Z = 160μm

Figure 4.12 Subthreshold transfer characteristics (long-channel)

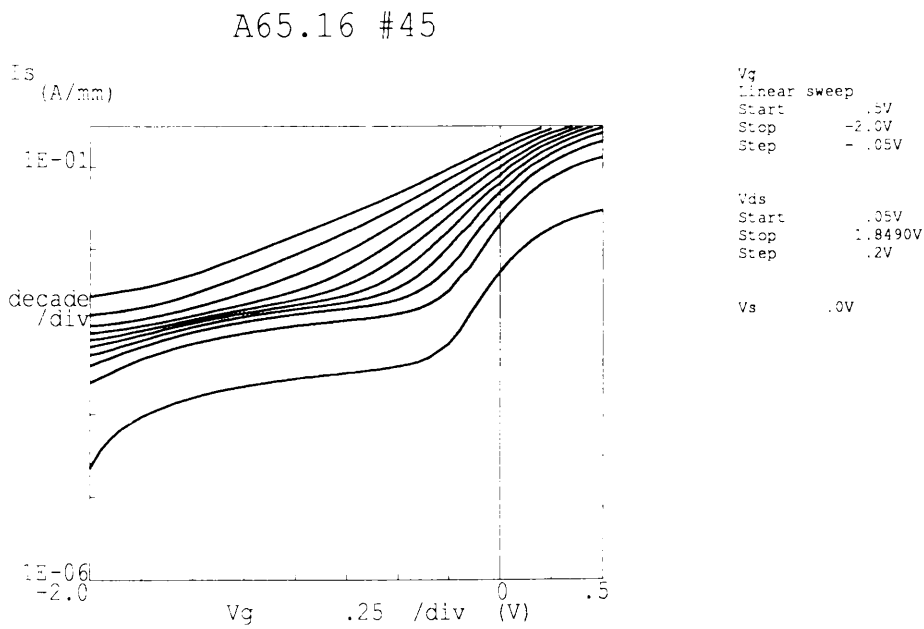


a) GaAs buffer, L_g = 300nm, Z = 160μm

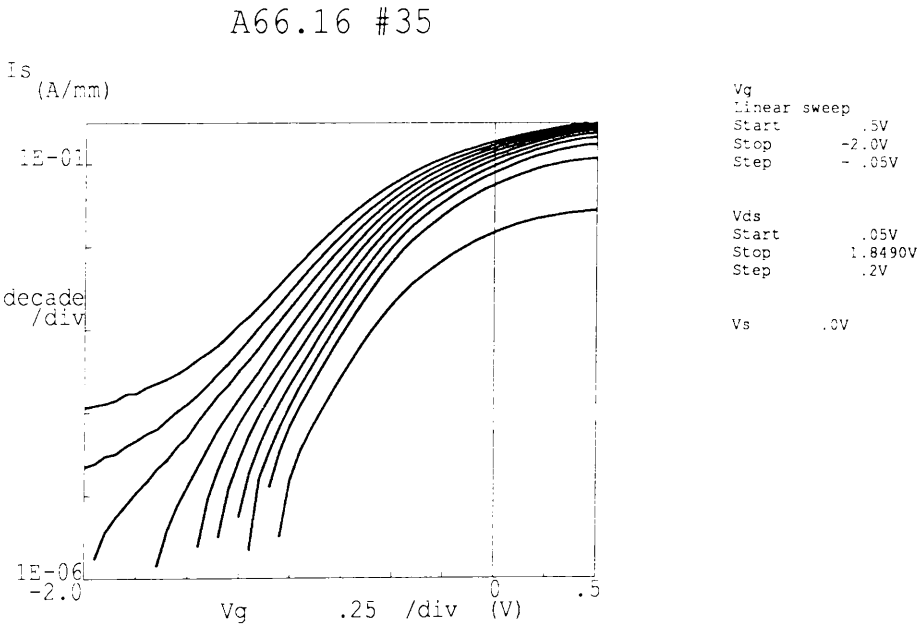


b) AlGaAs buffer, L_g = 300nm, Z = 160μm

Figure 4.13 Subthreshold output characteristics (long-channel)

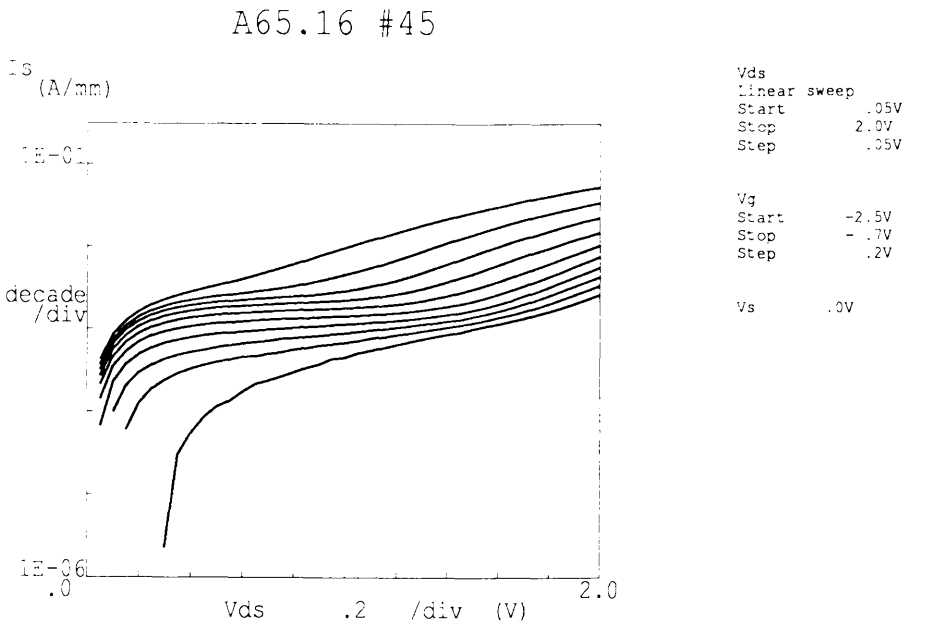


a) GaAs buffer, L_g = 60nm, Z = 80μm

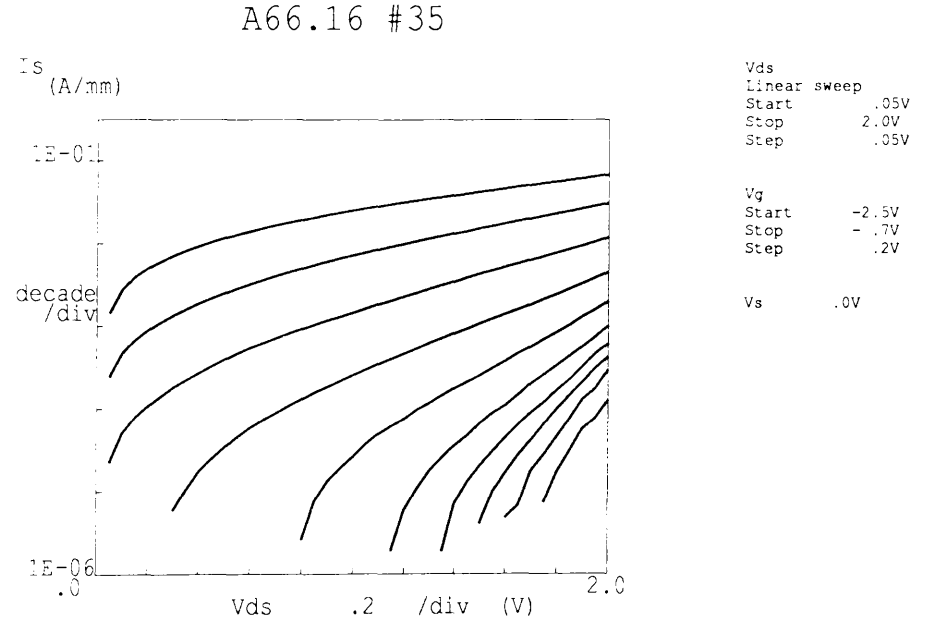


b) AlGaAs buffer, L_g = 50nm, Z = 80μm

Figure 4.14 Subthreshold transfer characteristics (short-channel)

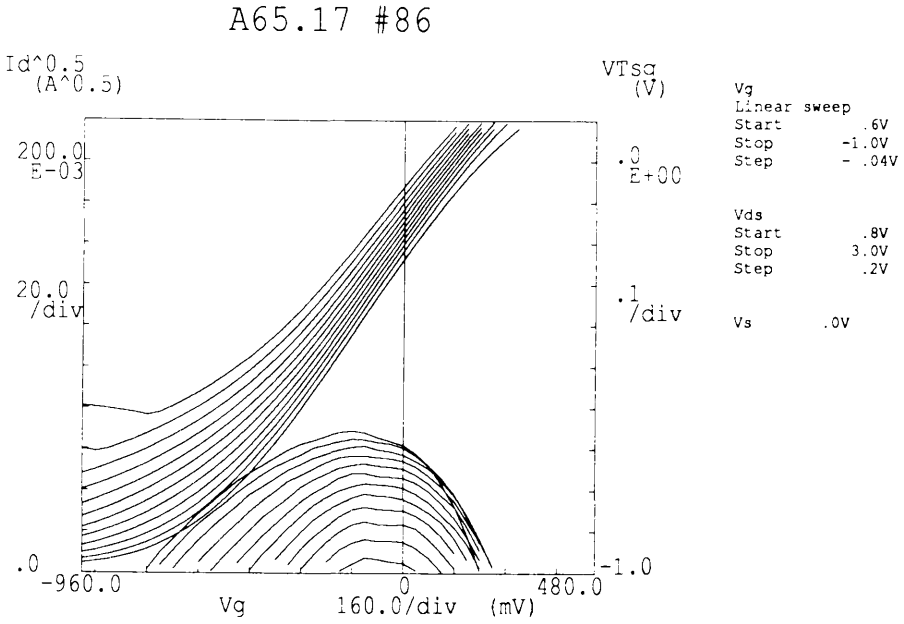


a) GaAs buffer, L_g = 60nm, Z = 80μm

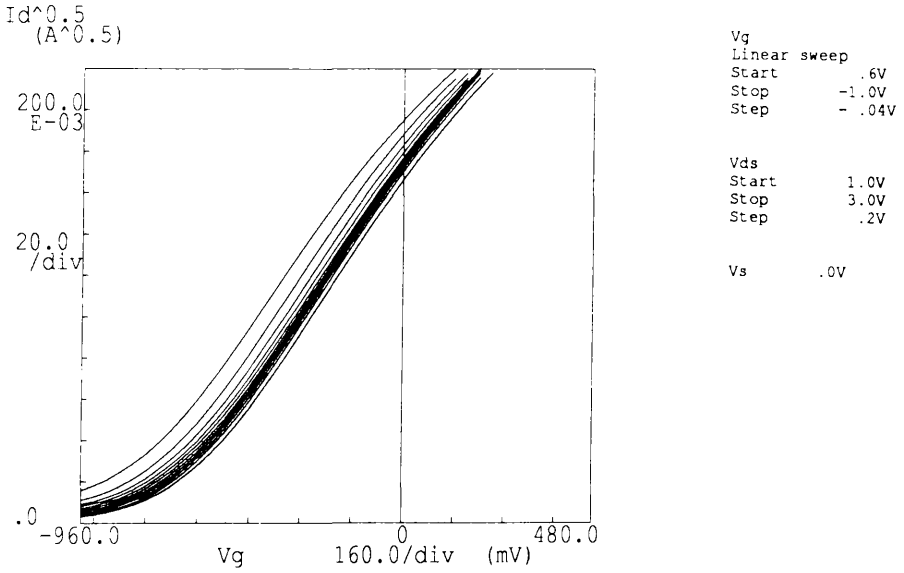


b) AlGaAs buffer, L_g = 50nm, Z = 80μm

Figure 4.15 Subthreshold output characteristics (short-channel)

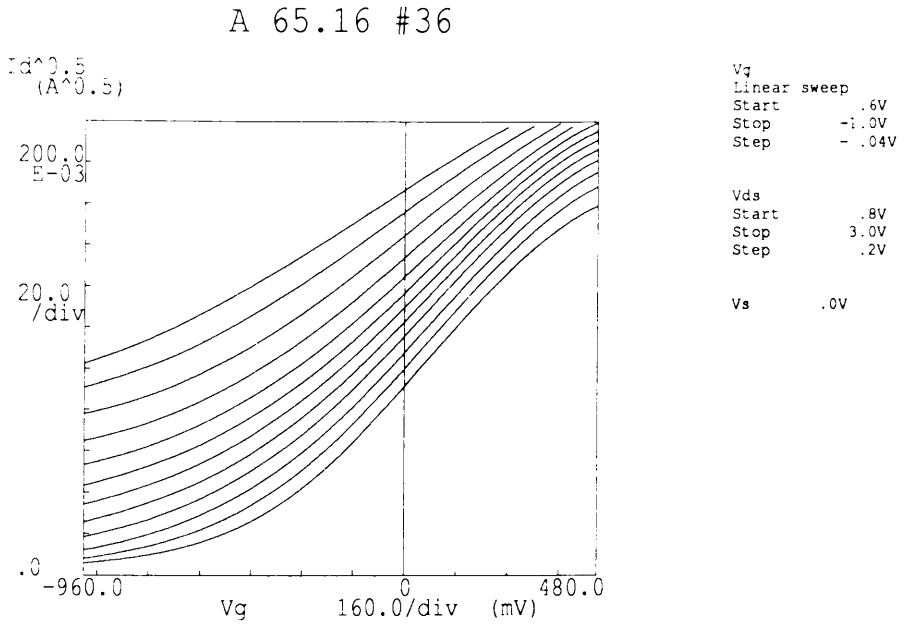


a) GaAs buffer, L_g = 300nm, Z = 160μm
$I_d^{1/2}$ and V_{Tsq} versus V_g
$V_{Tsq} = V_g - (\partial V_g/\partial I_d)2I_d$

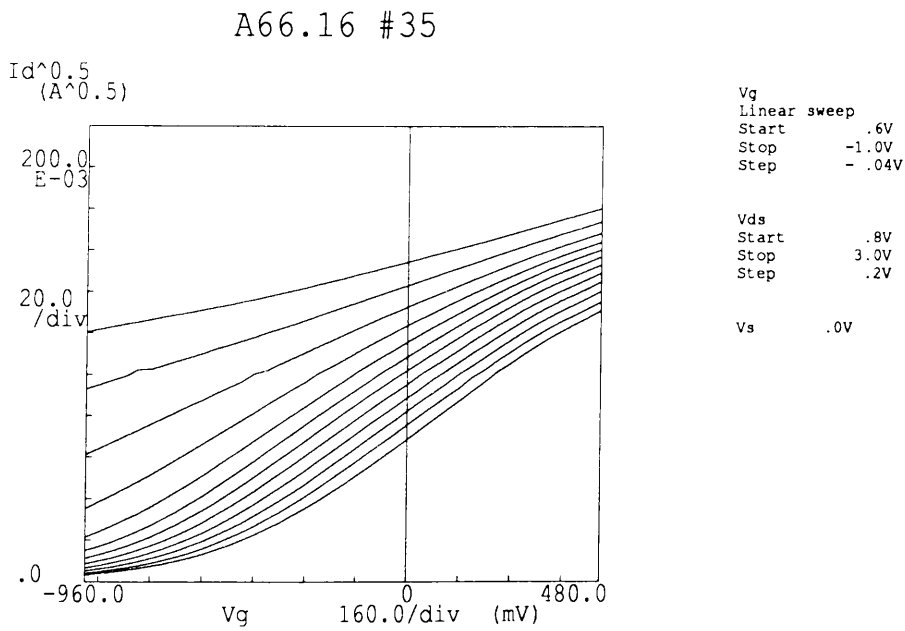


b) AlGaAs buffer, L_g = 300nm, Z = 160μm
$I_d^{1/2}$ versus V_g

Figure 4.16 Square law transfer characteristic (long-channel)
(and measurement of V_{Tsq} in Fig. a)

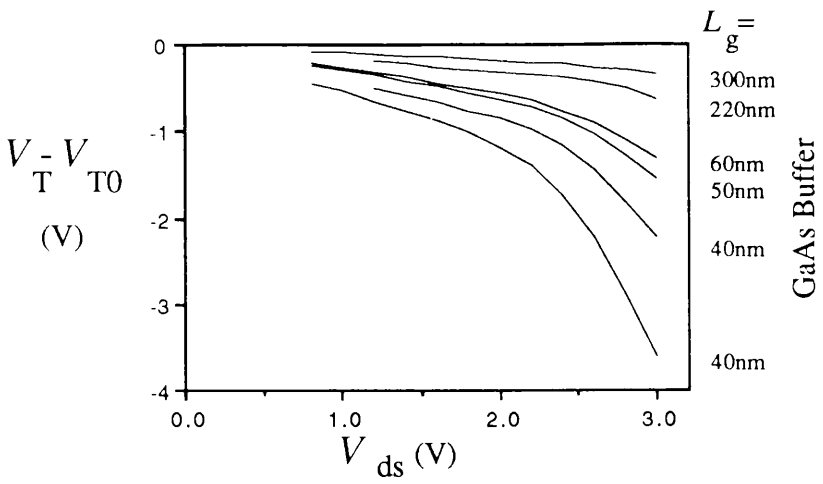


a) GaAs buffer, L_g = 50nm, Z = 80μm
$I_d^{1/2}$ versus V_g

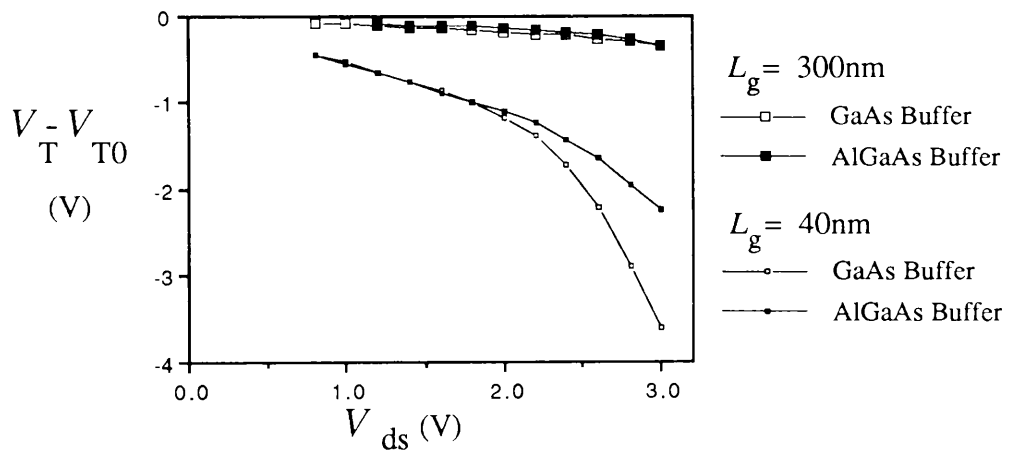


b) AlGaAs buffer, L_g = 50nm, Z = 80μm
$I_d^{1/2}$ versus V_g

Figure 4.17 Square law transfer characteristic (short-channel)

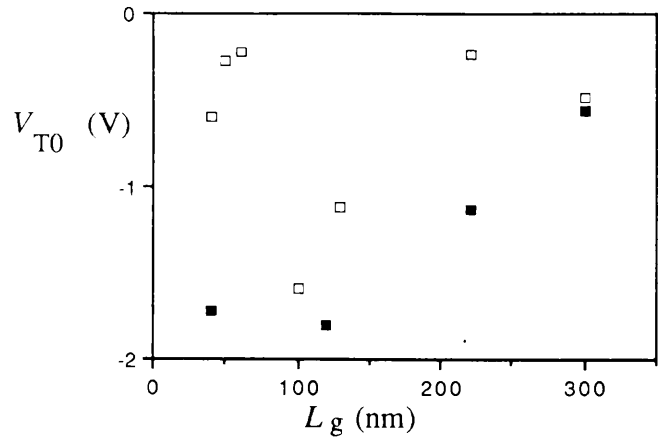


a) GaAs buffer, L_g = 40 to 300nm (bottom to top)

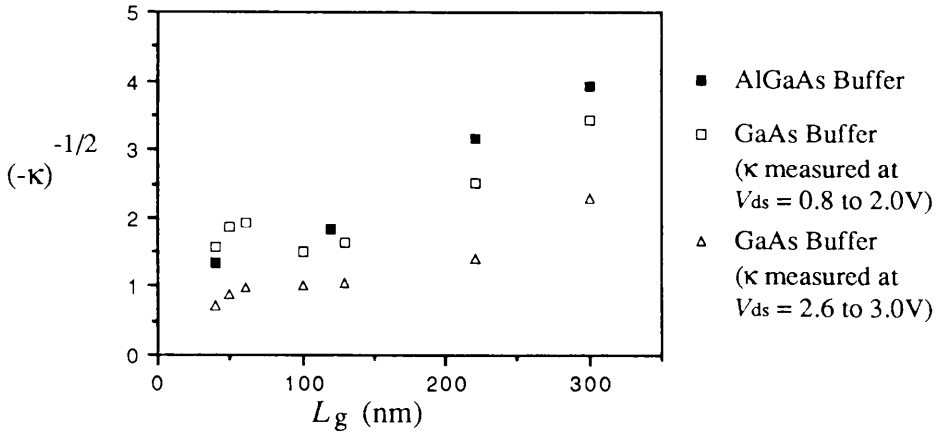


b) GaAs and AlGaAs buffers, L_g = 40nm and 300nm

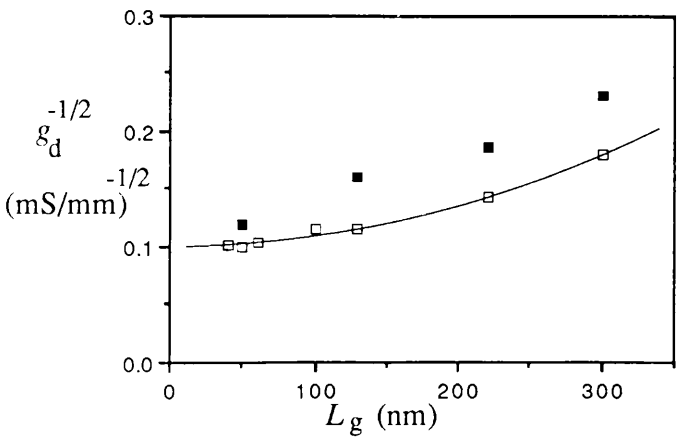
Figure 4.18 Square law threshold voltage shift



a) Threshold voltage scatter with gate-length



b) $(-\kappa)^{-1/2}$ versus L_g for GaAs and AlGaAs buffer



c) $g_d^{-1/2}$ versus L_g for GaAs and AlGaAs buffer

Figure 4.19 Investigation of threshold voltage shift

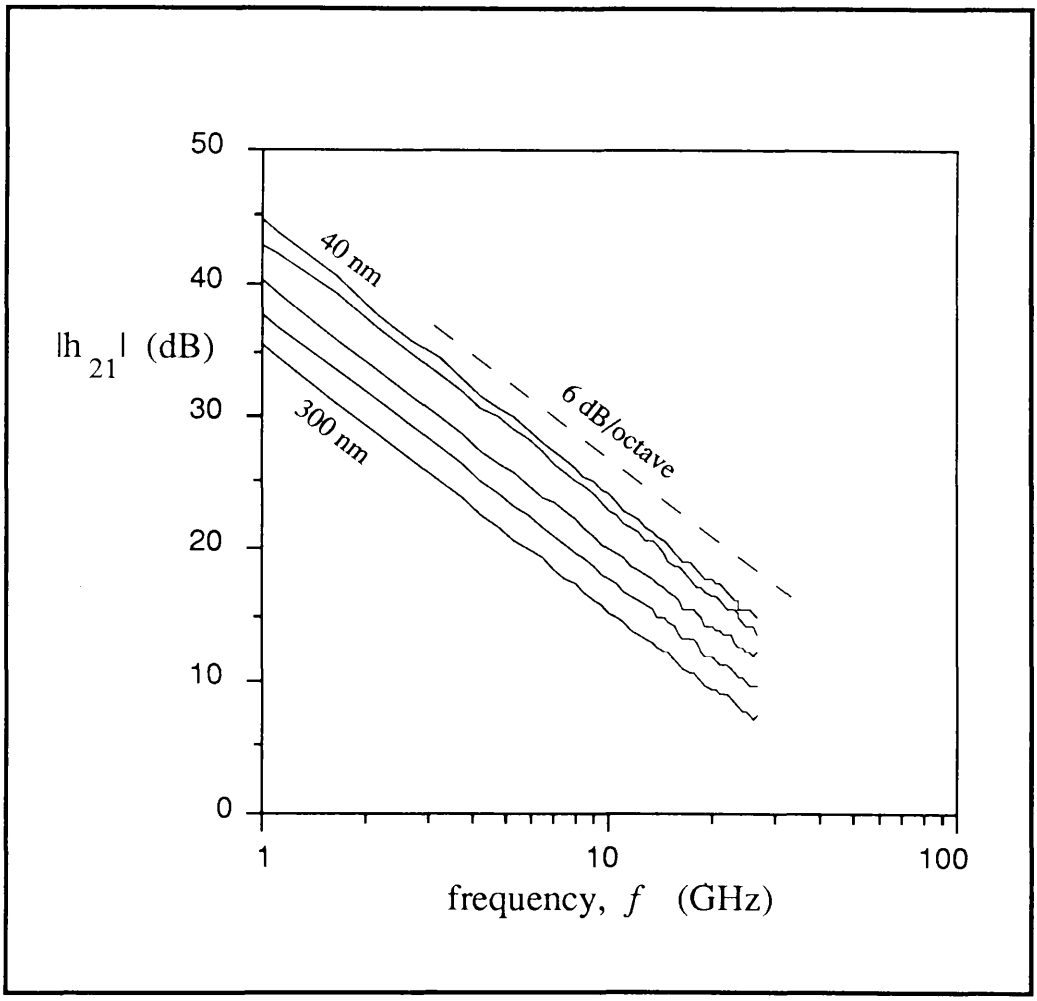


Figure 4.20 Short-circuit current gain versus frequency
GaAs buffer : L_g = 40, 60, 130, 220, 300nm
h_g = 50, 50, 150, 150, 150nm
$Z/2$ = 20, 40, 60, 80, 80μm

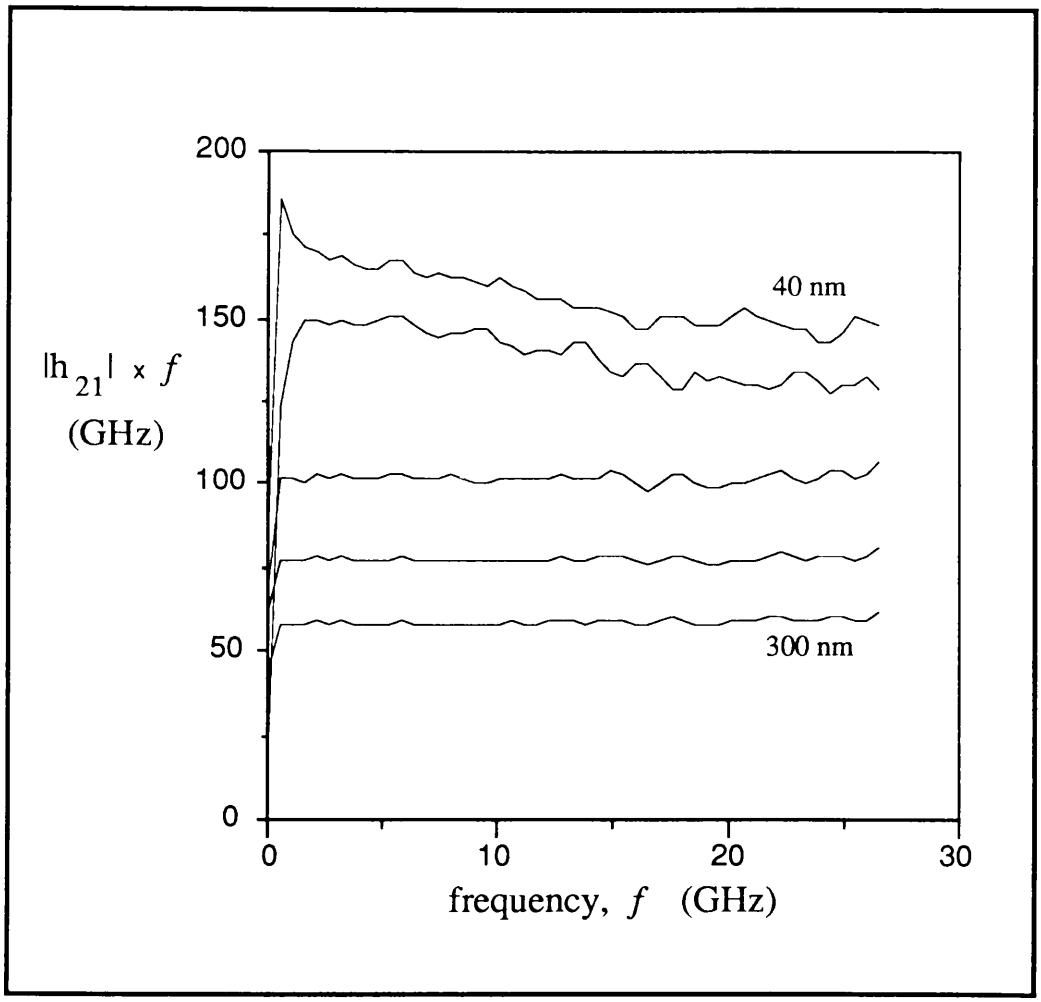


Figure 4.21 Gain-bandwidth product versus frequency

GaAs buffer : L_g = 40, 60, 130, 220, 300nm

h_g = 50, 50, 150, 150, 150nm

$Z/2$ = 20, 40, 60, 80, 80μm

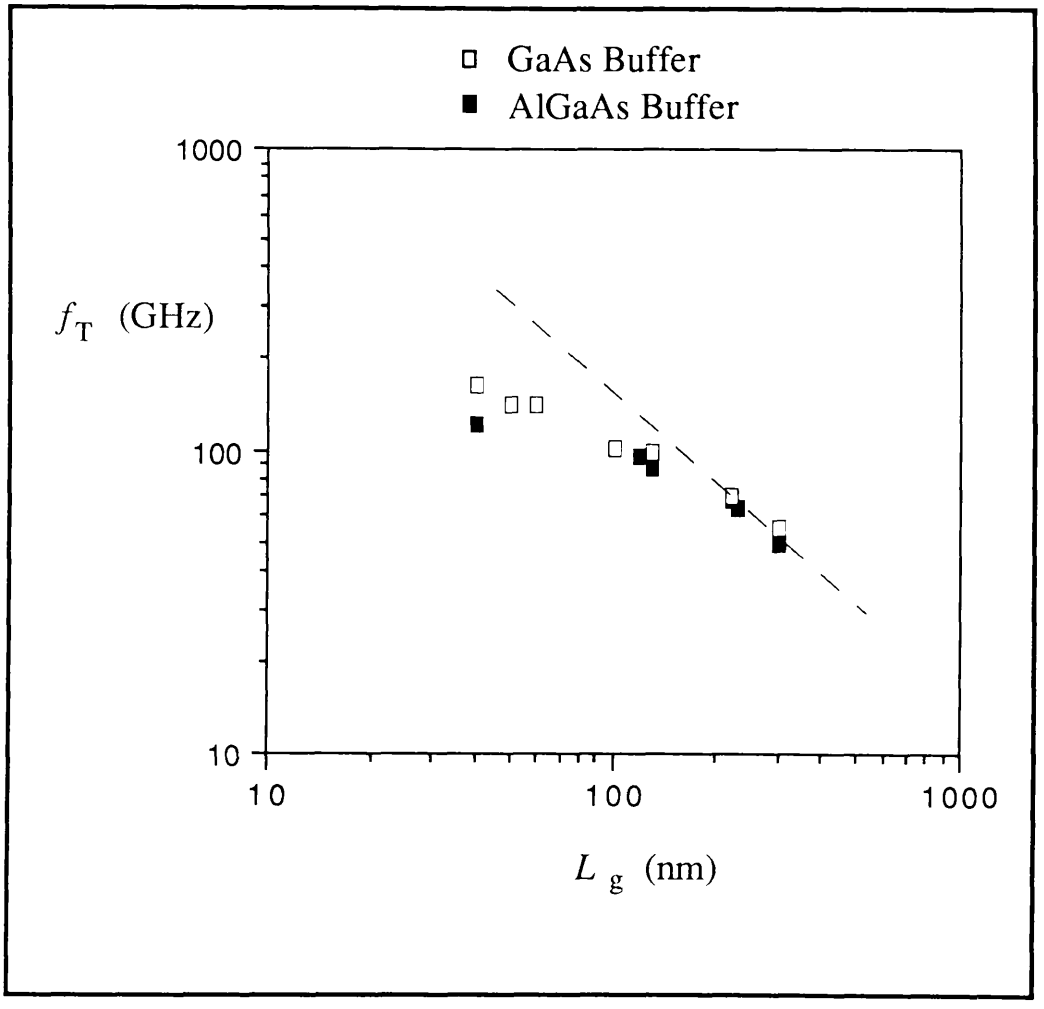


Figure 4.22 Unity gain cut-off frequency versus gate-length
The dashed line represents a velocity of 10^7cm/s

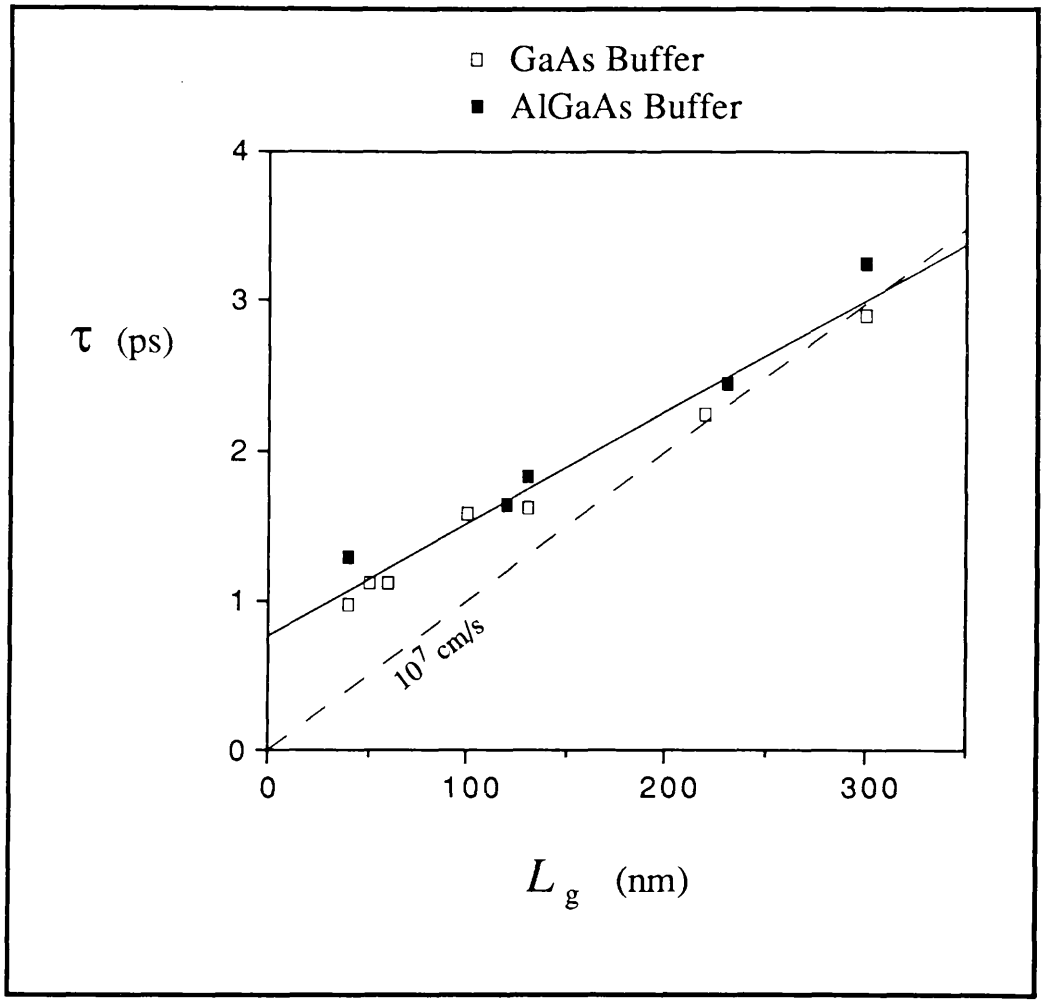
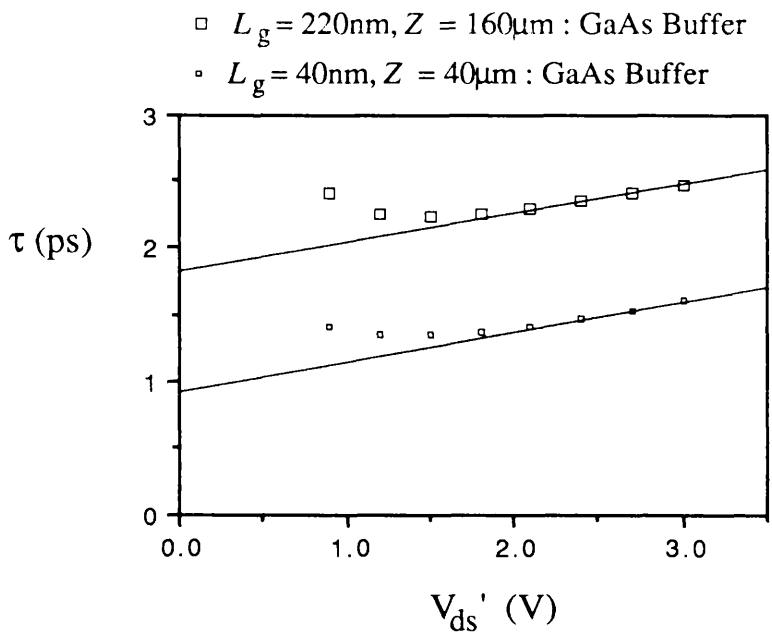


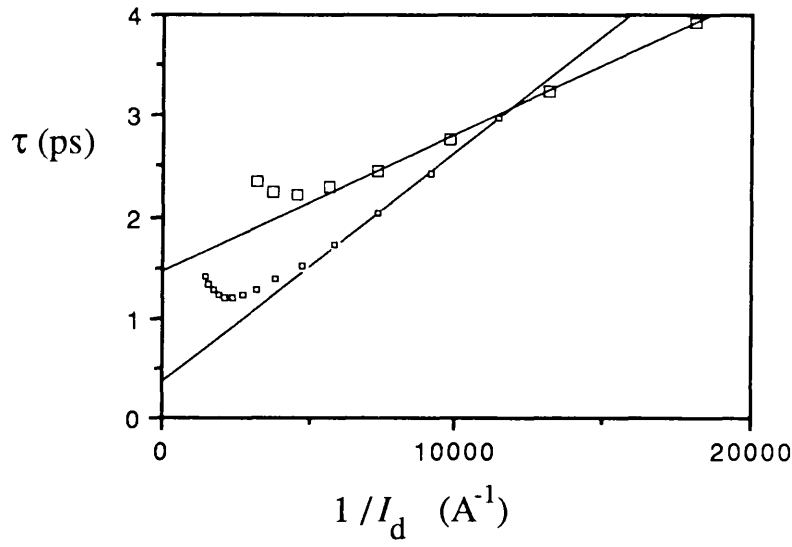
Figure 4.23 Transit time versus gate-length

$\tau = 1 / 2\pi f_T$

The dashed line represents a velocity of 10^7cm/s

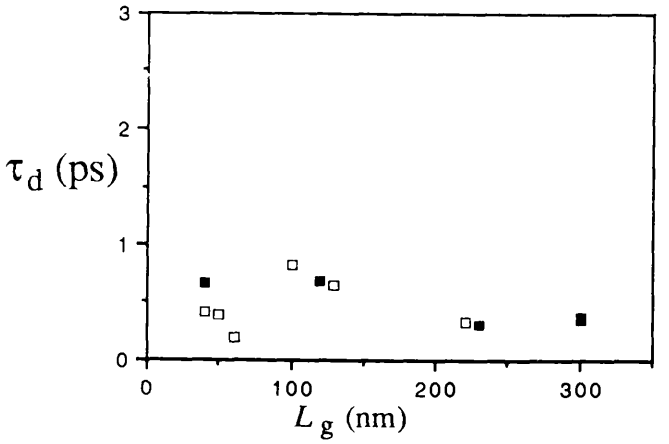


a) extraction of parasitic drain delay, τ_d

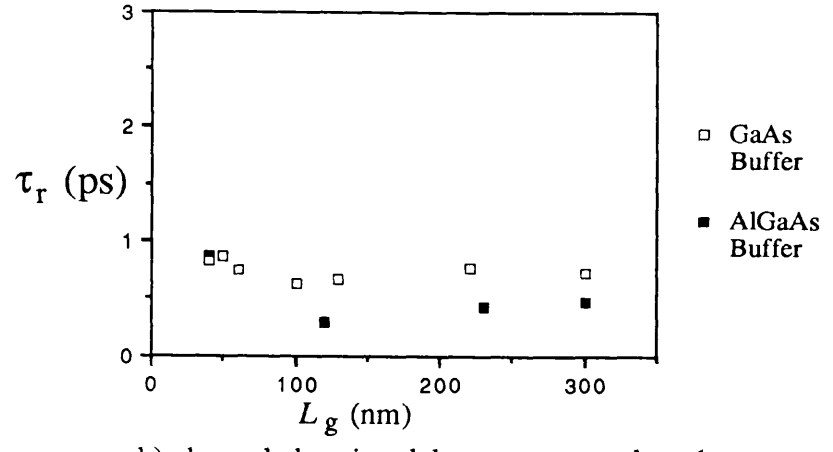


b) extraction of parasitic channel charging delay, τ_r

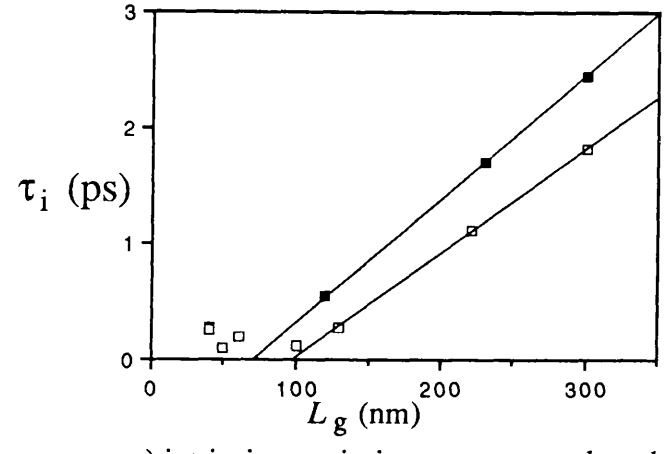
Figure 4.24 Example of extraction of parasitic transit delays



a) drain delay versus gate-length



b) channel charging delay versus gate-length



c) intrinsic transit time versus gate-length

Figure 4.25 Extracted transit times versus gate-length

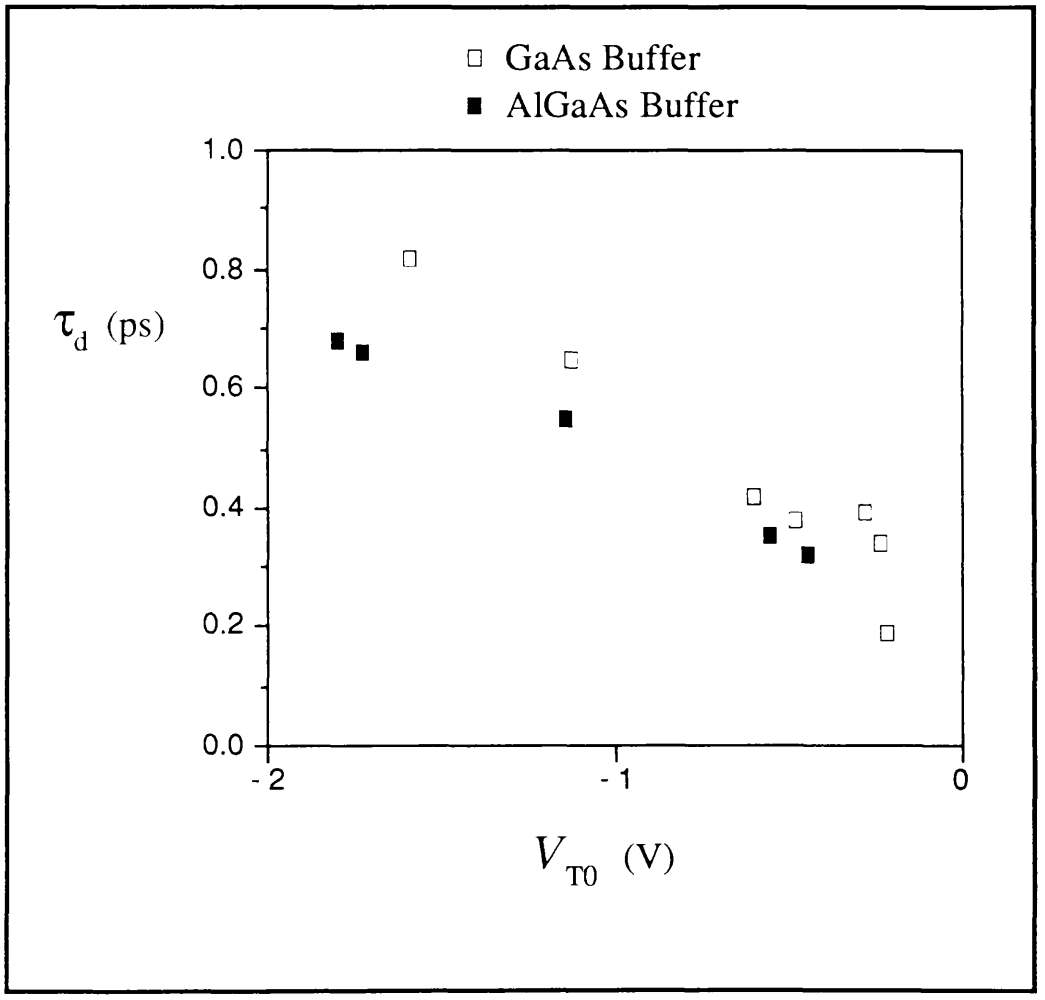
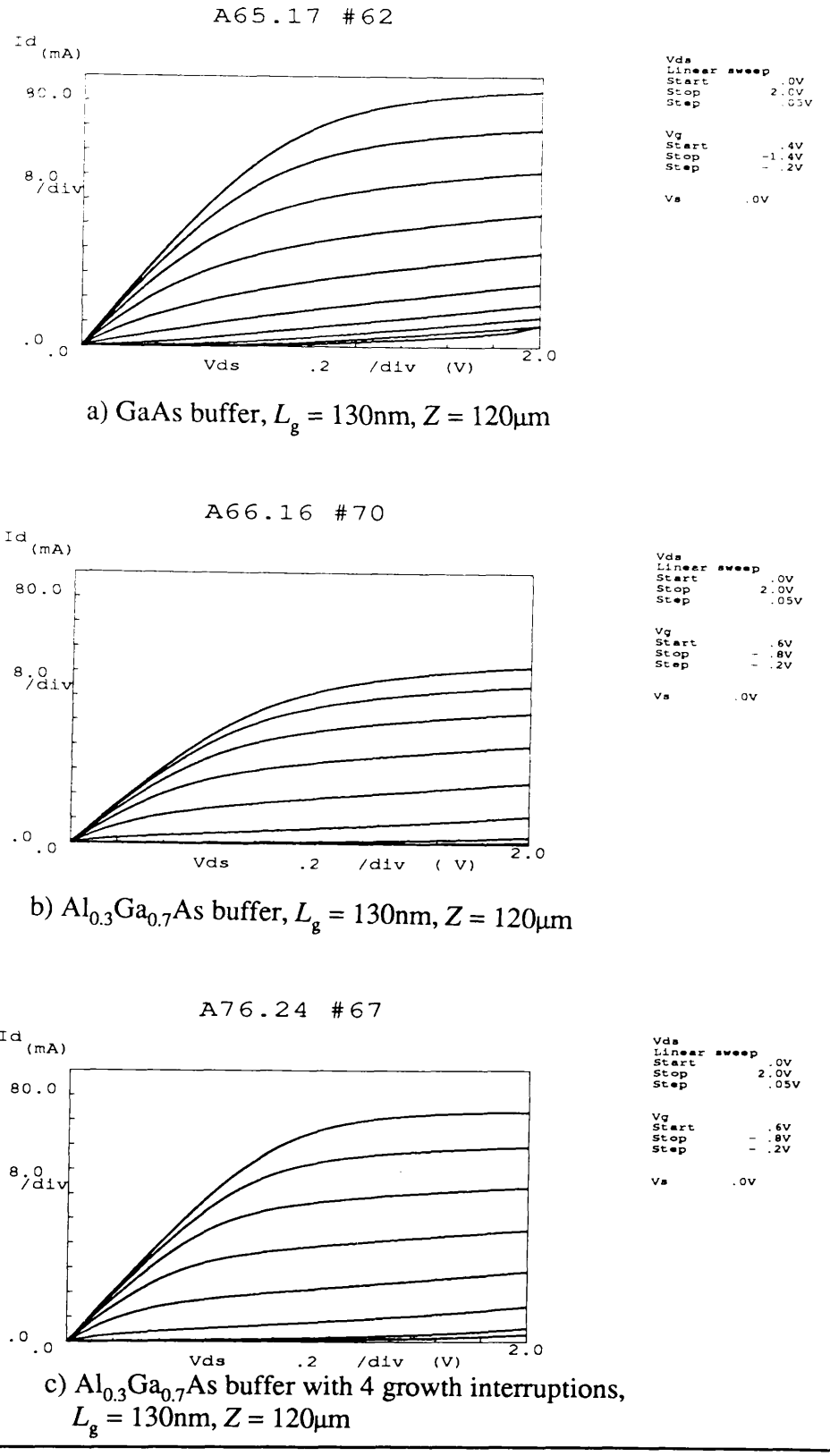


Figure 4.26 Drain delay versus threshold voltage

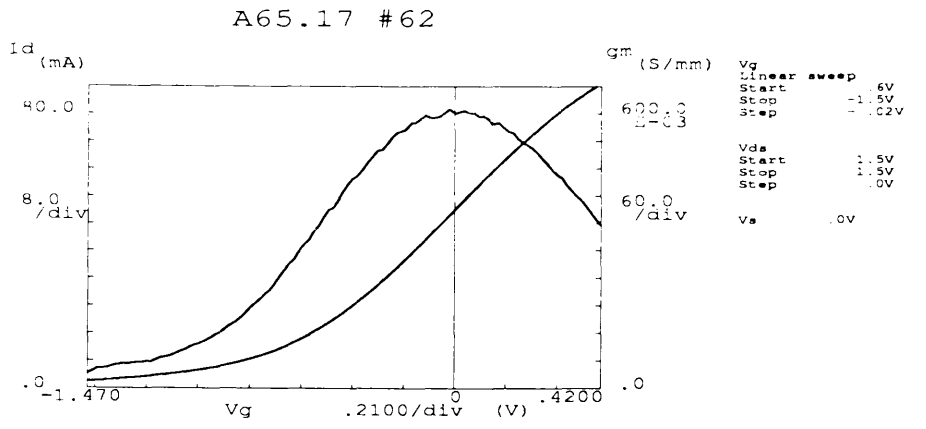


a) GaAs buffer, L_g = 130nm, Z = 120μm

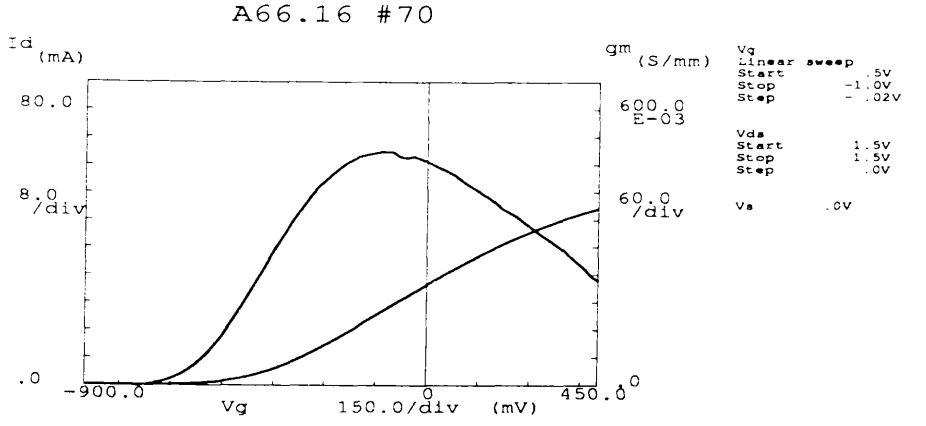
b) $Al_{0.3}Ga_{0.7}As$ buffer, L_g = 130nm, Z = 120μm

c) $Al_{0.3}Ga_{0.7}As$ buffer with 4 growth interruptions, L_g = 130nm, Z = 120μm

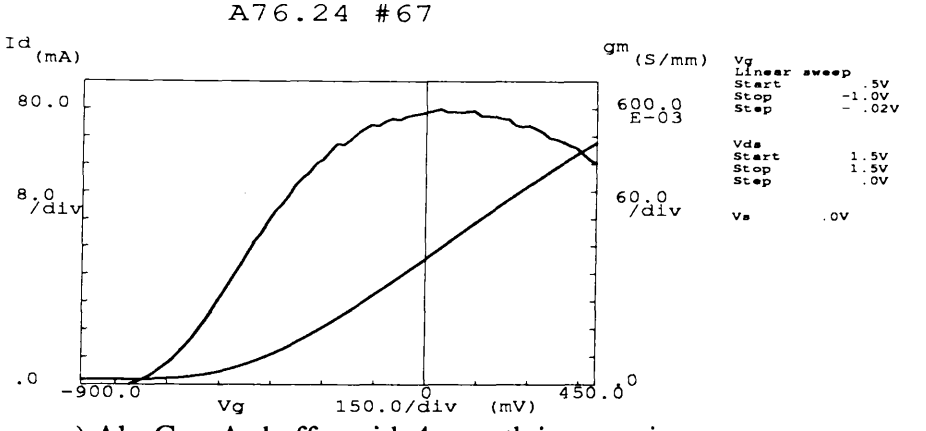
Figure 4.27 AlGaAs buffer comparison, output characteristics



a) GaAs buffer, L_g = 130nm, Z = 120μm

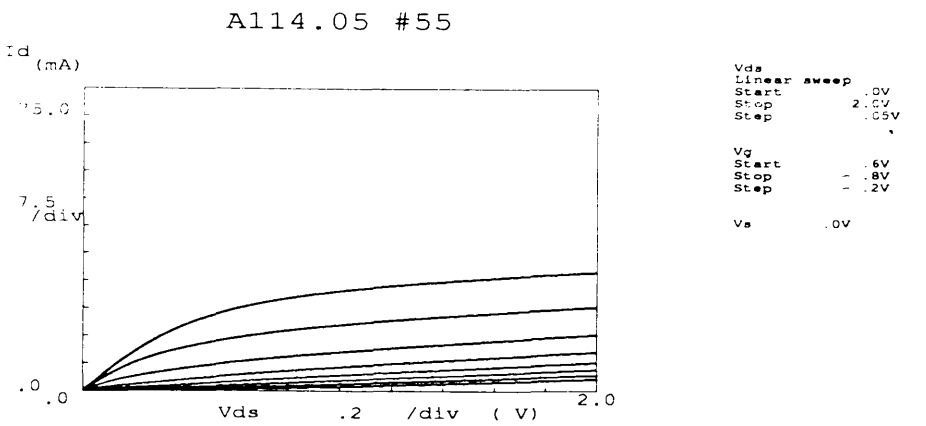


b) $Al_{0.3}Ga_{0.7}As$ buffer, L_g = 130nm, Z = 120μm

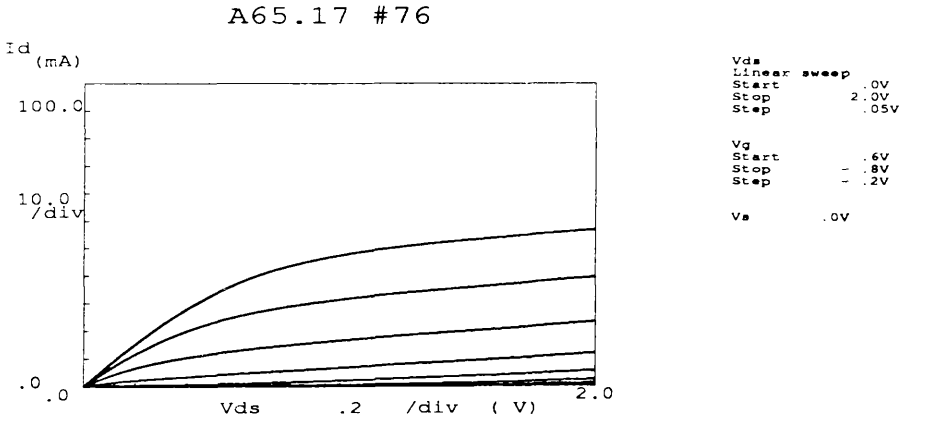


c) $Al_{0.3}Ga_{0.7}As$ buffer with 4 growth interruptions, L_g = 130nm, Z = 120μm

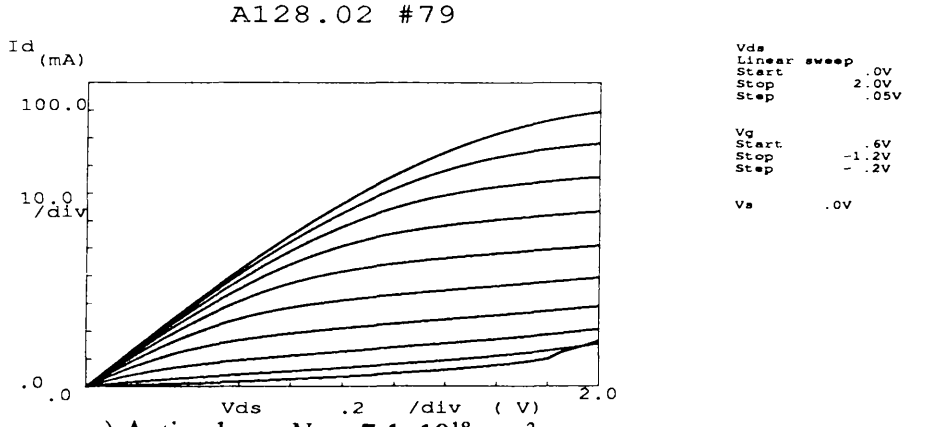
Figure 4.28 AlGaAs buffer comparison, transfer characteristics



a) Active layer $N_D = 2.2\text{x}10^{18}$ cm^{-3}
GaAs buffer, $L_g = 200$nm, $Z = 120\mu$m

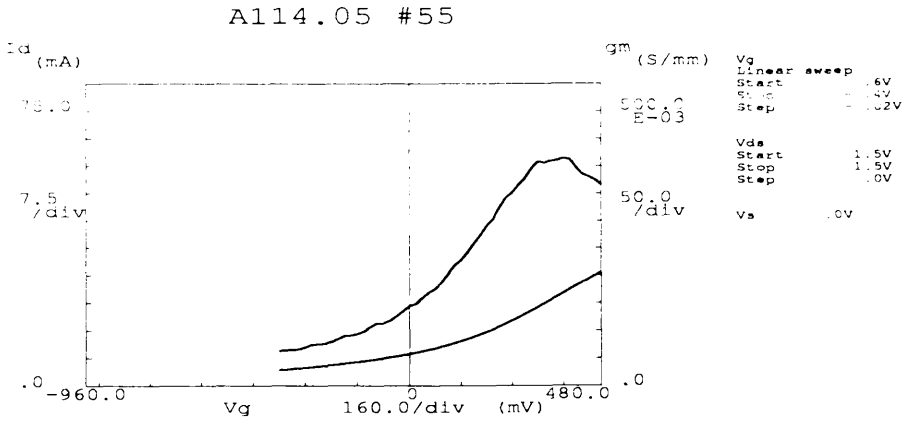


b) Active layer $N_D = 4.1\text{x}10^{18}$ cm^{-3}
GaAs buffer, $L_g = 220$nm, $Z = 160\mu$m

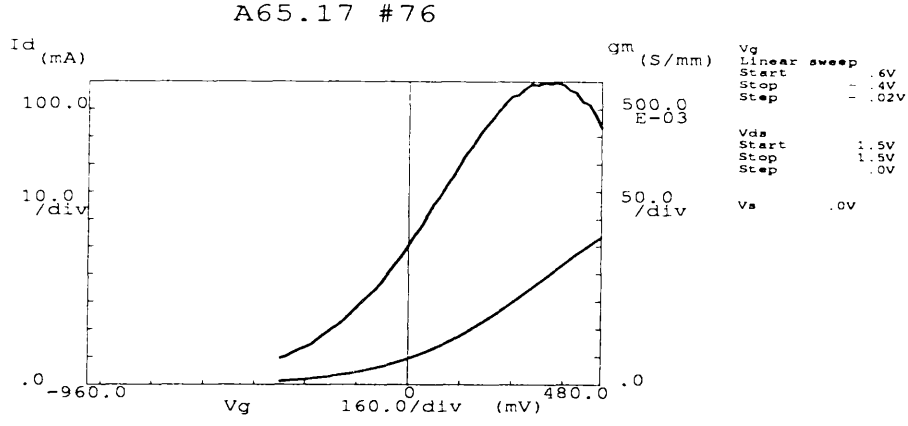


c) Active layer $N_D = 7.1\text{x}10^{18}$ cm^{-3}
GaAs buffer, $L_g = 200$nm, $Z = 160\mu$m

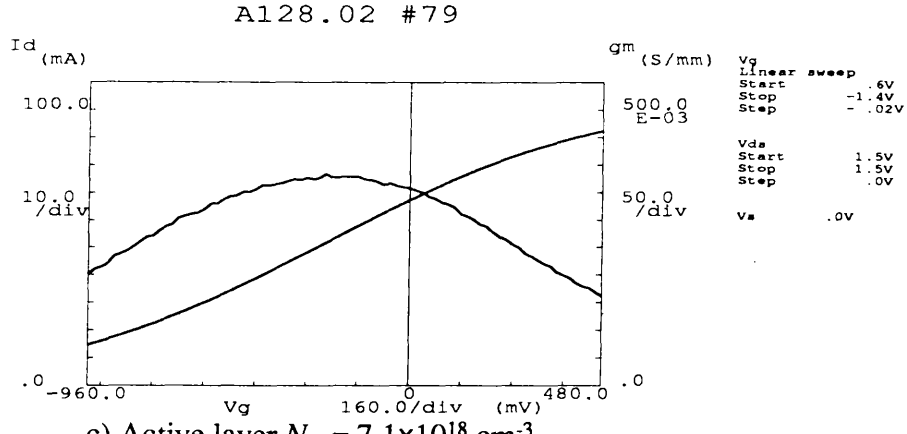
Figure 4.29 Active layer doping variation, output characteristics



a) Active layer $N_D = 2.2\text{x}10^{18}$ cm^{-3}
GaAs buffer, $L_g = 200$nm, $Z = 120\mu$m



b) Active layer $N_D = 4.1\text{x}10^{18}$ cm^{-3}
GaAs buffer, $L_g = 220$nm, $Z = 160\mu$m



c) Active layer $N_D = 7.1\text{x}10^{18}$ cm^{-3}
GaAs buffer, $L_g = 200$nm, $Z = 160\mu$m

Figure 4.30 Active layer doping variation, transfer characteristics

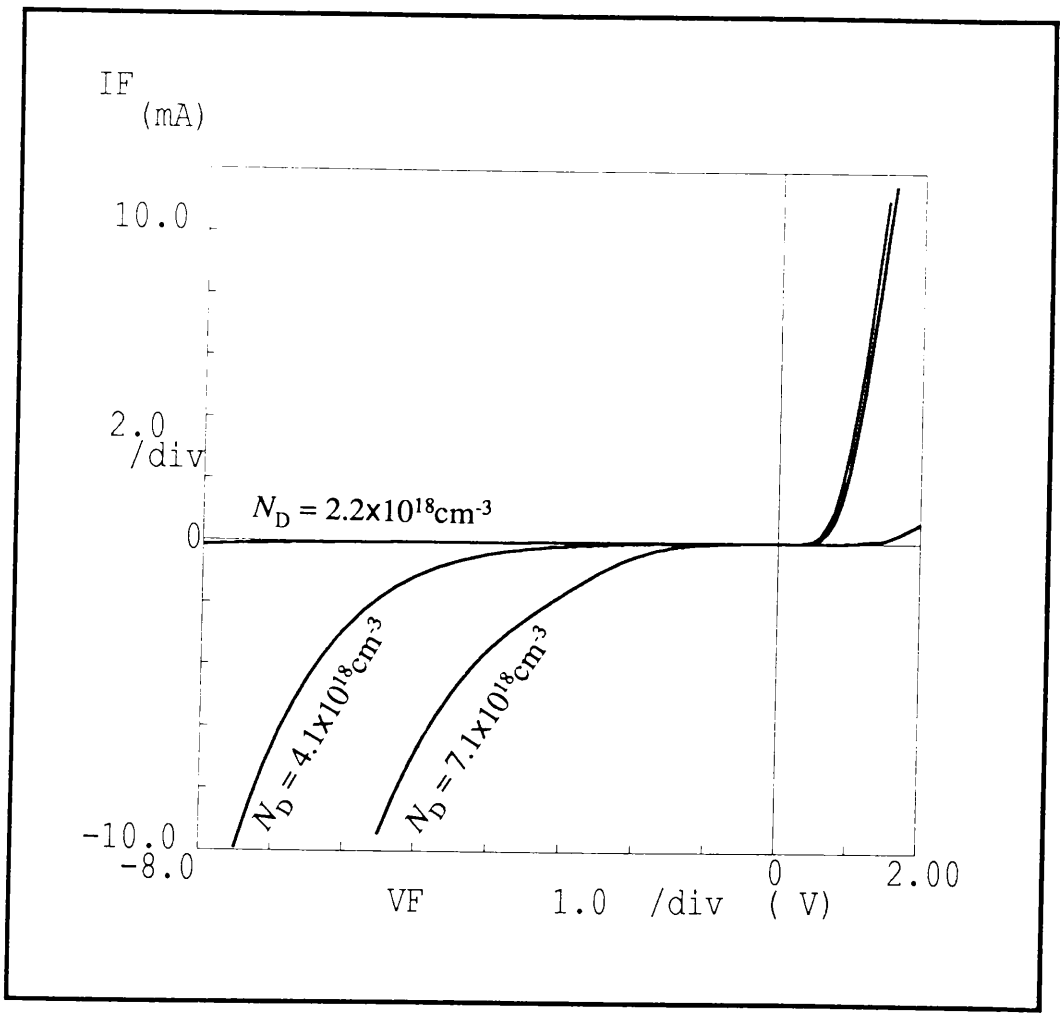


Figure 4.31 Active layer doping variation, gate characteristics

Chapter 5 - Conclusions

5.1 Summary

A process has been demonstrated for the fabrication of scaled GaAs based metal-semiconductor field effect transistors (MESFETs) suitable for high frequency characterisation with gate-lengths down to 40nm. MESFETs were fabricated with gate-lengths in the range 40 to 300nm on molecular beam epitaxy (MBE) grown layers with GaAs and AlGaAs buffers. The MESFETs were characterised electrically at direct current (DC) and high frequency.

The MESFETs have very good DC and high frequency performance, even down to the shortest gate-lengths. The performance is characterised by figures of merit such as transconductance and unity current gain cut-off frequency. MESFETs with a DC extrinsic transconductance of 720mS/mm and unity gain cut-off frequency of 150GHz (for a 40nm gate-length) have been demonstrated.

However, the performance of the MESFETs is limited by scaling effects. Some of these effects are of a technological nature such as buffer layer current, a large gate resistance, surface depletion effects, and the high active layer doping. More importantly, the performance of the shortest gate-length MESFETs is restricted by the fundamental short-channel effects of punch-through and hot-electrons. The origin and function of many of these effects have been introduced through a review of the operation and modelling of short-channel FETs (in chapter 2).

The MESFET design included features to minimise the technological scaling effects. i.e.

1) AlGaAs buffer layers to suppress buffer layer current. Experimental comparison was made with the GaAs buffer case.

2) High active layer doping to reduce the effect of surface depletion and maintain the channel aspect ratio, at the cost of deteriorated carrier transport. Devices with three different doping concentrations were compared.

3) A reduced gate-width with shorter gate-length to compensate for the larger series gate resistance.

The experimental work described in this thesis investigates the scaling effects by electrical characterisation of the devices at DC and high frequency. The measurements presented and discussed included:

1) DC open channel and subthreshold transfer and output characteristics.

2) DC threshold voltage shift, equivalent to output conductance.

3) High frequency (up to 26.5GHz) S-parameters which yield the short-circuit current gain, maximum frequency of oscillation, and parasitic carrier transit delays through the channel.

The design strategy was successful to the extent of overcoming many of the detrimental scaling effects for MESFETs with gate-lengths down to 200nm. The buffer layer current was suppressed by the AlGaAs buffer, and it was shown that interrupted growth of the AlGaAs buffer can surmount the problem of degradation of active layer quality associated with MBE growth of GaAs on AlGaAs.

On the negative side, the technological problems of large gate resistance, surface depletion effects and very high active layer doping (which inhibits carrier transport) were found to significantly degrade the high frequency performance of the devices in this work. These are all issues which could be addressed by modifications to the device design. In addition, the parasitic carrier transit delays became more significant in degradation of high frequency performance as the gate-length was reduced.

As for the more fundamental effects, the main conclusion of this thesis is that the ultimate scaling limits of hot-electron and punch-through effects govern the behaviour of the MESFETs with very short gate-lengths (in this case, less than 100nm). The most severely affected parameters are output conductance and subthreshold current. For example, the benefits of AlGaAs buffer are greatly reduced for 40nm gate-length MESFETs. Reduction of gate-length can still give an improvement in high frequency performance, but less than predicted by simple scaling of the carrier transit time and the beneficial hot-electron effect of velocity overshoot. No evidence of velocity overshoot effects has been found in these MESFETs.

The remainder of this chapter presents the conclusions arising from the electrical characterisation. A list of symbols is given in chapter 2 (page 6).

5.2 MESFET Figures of Merit

MESFETs have shown extrinsic DC transconductance of up to 710mS/mm (for a 40nm gate-length GaAs buffer device). A DC voltage gain of 28 was obtained for a 300nm gate-length AlGaAs buffer MESFET.

A unity gain cut-off frequency, f_T of 150GHz was determined for the 40nm gate-length GaAs buffer MESFET, however the short-circuit current gain was degraded at the highest measurement frequencies by large gate resistance effects.

An effective carrier velocity can be obtained from $L_g 2\pi f_T$. This velocity was 1.2×10^7cm/s for a 220nm GaAs buffer MESFET with an active layer ionised donor concentration determined as 2.1×10^{18}cm^{-3}. This velocity value is similar to the bulk electron saturation velocity in GaAs, and compares well with the best reported values in Table 2.1 (page 49). After taking into account the modification channel length (see below), this represents a large average carrier velocity in the channel.

5.3 Short-Channel Effects

5.3.1 Subthreshold Drain Induced Barrier Lowering

In the absence of subthreshold buffer current, the long-channel AlGaAs buffer device exhibits a diffusion limited subthreshold current mechanism, a form of drain induced barrier lowering (DIBL). The same effect can be seen in the long-channel GaAs buffer device, at low V_{ds} and large V_g, where the channel is only just pinched-off.

In the short-channel devices, with both GaAs and AlGaAs buffers, subthreshold current control is dominated by DIBL. In the GaAs buffer device, the virtual cathode can move into the buffer, where the coupling of V_g to ψ_b is reduced and the DIBL current is many orders of magnitude larger than with comparable bias conditions in the AlGaAs buffer device.

The large scatter in threshold voltages in these devices frustrates a meaningful analysis of the DIBL with respect to gate-length, which could allow determination of the barrier lowering coefficients β and γ.

5.3.2 Punch-Through and Hot-Electron Effects

In short-channel devices, very large threshold voltage shift is dominated by hot-electron effects and/or DIBL punch-through.

Shorter-channel devices exhibit a marked increase in threshold voltage shift as V_{ds} is increased above 2V. The fact that this is highly dependent on V_{T0} indicates that a the effects causing the V_T shift occur to a large extent in the active layer.

Threshold voltage shift is dominated by hot-electron effects (because of the very high longitudinal fields in these devices) and/or DIBL punch-through (as was revealed by the subthreshold measurements, although no direct evidence was found by examining the V_T shift). It is not possible to deduce the relative or absolute contributions of these two mechanisms using the methods described here.

5.3.3 Parasitic Transit Delays

The shortest gate-length devices exhibit very high unity gain cut-off frequency, f_T of up to 150GHz. However, this performance falls short of that predicted by the simple model with f_T inversely proportional to gate-length. This can be explained by a parasitic channel length (~ 100nm) which adds to the total transit time in the devices. The total transit time can be divided into three components: i) parasitic drain delay, ii) parasitic channel charging delay and iii) intrinsic channel delay. S-parameter measurements at a range gate and drain of bias points allowed determination of these components.

The parasitic drain delay, τ_d was a strong function of the recess depth (as characterised by threshold voltage), which points to lengthening of the channel by the surface depletion and fringing of the transverse gate field as being the most significant contribution to the drain delay.

Carriers flowing from the source to the channel via a long and high resistivity path through the GaAs buffer, result in a channel charging delay, τ_r approximately double that of the AlGaAs buffer case for longer-channel devices.

The very small intrinsic transit delays, τ_i obtained indicate that in a region under the source end of the gate, the average carrier velocity is low, perhaps because the carriers are still accelerating under the influence of the longitudinal field, or (less likely) because the longitudinal field strength is less than the critical field for velocity saturation. The length of this region reduces the intrinsic channel length to ~ 100nm less that the gate-length,

tending to ~ 20nm the gate-length decreases below 100nm. This may be an explanation of the relatively poor values of f_T as the gate-length was reduced below 100nm.

5.4 Technological Scaling Effects

5.4.1 Buffer Layers

Advantages of an AlGaAs Buffer

AlGaAs buffer devices have smaller output conductance and greater voltage gain because of the reduction of current in the buffer. AlGaAs buffer devices have larger K-values, because of the sharper pinch-off against the buffer layer, i.e. better carrier confinement in the active layer.

Buffer current strongly magnifies the subthreshold current in GaAs buffer devices at useful operating biases. The AlGaAs buffer eliminates subthreshold buffer current in long-channel devices.

The small threshold voltage shift in long-channel GaAs buffer devices appears to be governed by buffer current. The evidence is the large departure from square-law behaviour in the transfer characteristic, which is absent in the long-channel AlGaAs buffer device. However, GaAs buffer devices over a range of gate-lengths do not exhibit the dependence of g_d and κ on L_g predicted for SCL buffer current, indicating that the buffer current is not space charge limited.

At high frequency little difference is seen between GaAs and AlGaAs buffer devices. The f_{max} performance was dominated by large gate resistance, so the effect of the larger g_m/g_d of the AlGaAs buffer devices was not apparent. For long channel-length, the AlGaAs buffer reduces the channel charging delay by a factor of two, compared to GaAs buffer devices.

Disadvantages of an AlGaAs Buffer

The AlGaAs buffer devices have slightly inferior DC and high frequency performance, as quantified by g_m and f_T, which can be explained by the inferior carrier transport as a consequence of the poor quality active/buffer layer interface.

Interrupted Growth AlGaAs Buffer

Growth interruptions in an AlGaAs buffer bring the DC and high-frequency performance of MESFETs as quantified by g_m and f_T up to that of a GaAs buffer devices. The growth interruptions do not adversely affect the carrier confining properties of the AlGaAs buffer layer, as quantified by K-value and g_d.

Predominance of Punch-Through and Hot-Electron Effects in Short-Channels

The output conductance, g_d rises with reduced gate-length equally for the devices with both GaAs and AlGaAs buffers. The difference between g_d at each gate-length is the contribution of buffer-layer current. At very short gate-length, the advantage of the AlGaAs buffer diminishes, because punch-through and hot-electron effects operate mainly in the active layer.

Equivalently, a reduced V_T shift is observed for longer gate-length AlGaAs buffer devices, but for the shortest gate-length devices the AlGaAs buffer has little effect on reducing the shift. Shorter-channel devices exhibit a marked increase in threshold voltage shift as V_{ds} is increased above 2V. The fact that this is highly dependent on V_{T0} reinforces the assumption that a the effects causing the V_T shift occur to a large extent in the active layer.

5.4.2 High Active Layer Doping

Increasing the active layer doping concentration characterised by the ionised donor concentration, N_D, causes an increased gate diode ideality factor and a lowered Schottky barrier height, but the gate reverse leakage currents in the open channel operating range are not large enough to degrade DC and high-frequency performance.

The observed increase of f_T with reduced N_D despite the worsened parasitic delays is the result of improved carrier transport. It appears that the very high doping can degrade transit time by suppressing the average carrier velocity. In the low doped case, the higher average velocity is able to overcome the more severe parasitic delays to give shorter total transit times.

An observed increase in f_{max} with reduced N_D may be due a increased C_{gs}/C_{gd} ratio.

5.4.3 Surface Effects

The detrimental effect of surface depletion was evident in the strong dependence of the parasitic drain delay, τ_d on the the recess depth (as characterised by threshold voltage). This points to lengthening of the channel by the surface depletion as being a significant limit to high frequency performance.

5.4.4 Gate Resistance

The shortest gate-length devices suffer a degradation of short circuit current gain, $|h_{21}|$ with measurement frequency up to 26.5GHz. The result is a roll-off of $|h_{21}|$ (dB) with $\log f$ at greater than 6dB/octave. This is attributed to the very large series gate resistance, R_g which may introduce a distributed delay along the width of gate.

The devices are not optimised to give large f_{max}, which is governed by the large gate resistance in all devices.

5.4.5 Threshold Voltage Uniformity

The lack of control of threshold voltages in these devices would make inclusion of them into useful circuits very difficult. The nonuniformity (i.e. dependence on gate-length) and nonreproducibility of the gate recess etch are the main problem. In addition, the short-channel effects can shift the threshold voltage as a function of gate-length and drain bias.

In the context of these experiments, the scatter of threshold voltage has frustrated the analysis of the DIBL with respect to gate-length.

5.5 Other Work

Extensive enhancements were made to the electron-beam lithography system software to facilitate automated patterning of the large number of devices required for the project. This work included integration of automatic frame registration and focusing systems with the driver software, and adding support for text patterning and automatic site numbering.

5.6 Future Work

Fabrication

There are two outstanding problems with the MESFETs described in this thesis; i) the gate resistance, R_g is too large and ii) the gate recess uniformity is inadequate. The use of a mushroom gate structure would greatly reduce R_g. More measurements at DC and high frequency measurements of devices with constant width could confirm the improvement in this parasitic resistance. The recess uniformity could be improved by using a low damage dry etching process, with a suitable pattern transfer process.

The temperature stability of the gate metallisation should be improved by incorporating a thin platinum diffusion barrier between the titanium and gold layers.

Circuits

With good control of the threshold voltage by improved recessing, fabrication of circuits around these MESFETs could be undertaken to demonstrate their suitability for high speed digital processing applications. As part of this work, the lithographic process for a 17 stage ring-oscillator circuit has been demonstrated (Figs. 5.1 and 5.2 pages 180 and 181) and circuits have been fabricated up to the first (enhancement mode) gate level (Fig. 5.1). The circuit utilises direct coupled FET logic comprised of 50nm gate-length devices. The ring oscillator is the simplest digital circuit after an inverter, and it allows a measurement of the maximum inverter switching speed, albeit with the a fanout of one at each stage, which is unrealistic for logic applications.

Simulation

An invaluable aid in understanding the physical mechanisms acting in these devices is Monte Carlo simulation. Application of such a model to MESFETs of the same structure and composition as those described here will allow a quantitative study of the role of punch-through and hot-electron effects in output conductance and drain bias dependent threshold voltage shift. The velocity and field distributions obtained from such a simulation could validate and clarify the results of the transit time measurements described in this thesis.

Noise Measurements

Further characterisation of the quality of the GaAs/AlGaAs active/buffer layer interface could be obtained from high frequency noise measurements. The operating point of the MESFET for low-noise applications is in the low current (near pinchoff), high carrier velocity range, so the noise performance should be strongly affected by the mobility degradation at and near the interface.

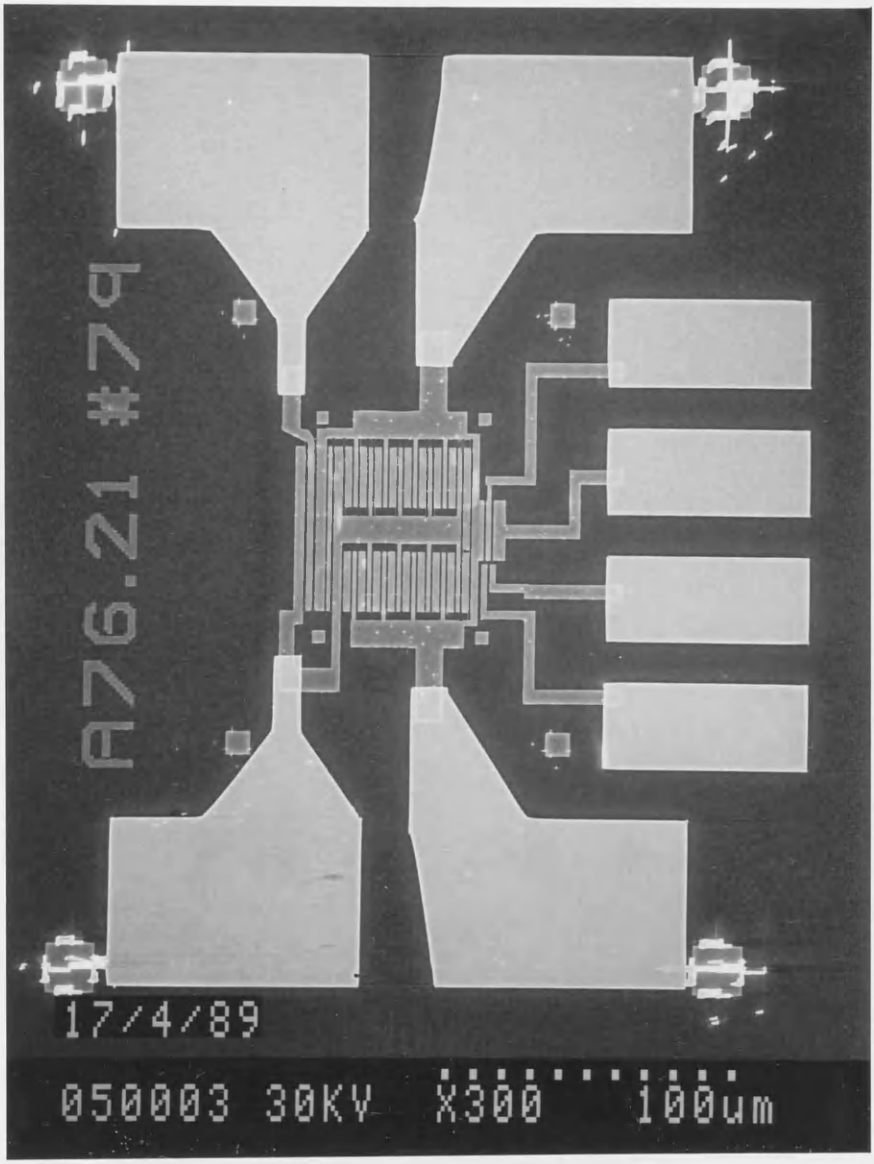


Figure 5.1 Electron micrograph of a 17 stage ring oscillator
(gate levels not defined)
Four probing pads at the right are a test inverter.
Wider devices at the left amplify the output signal.

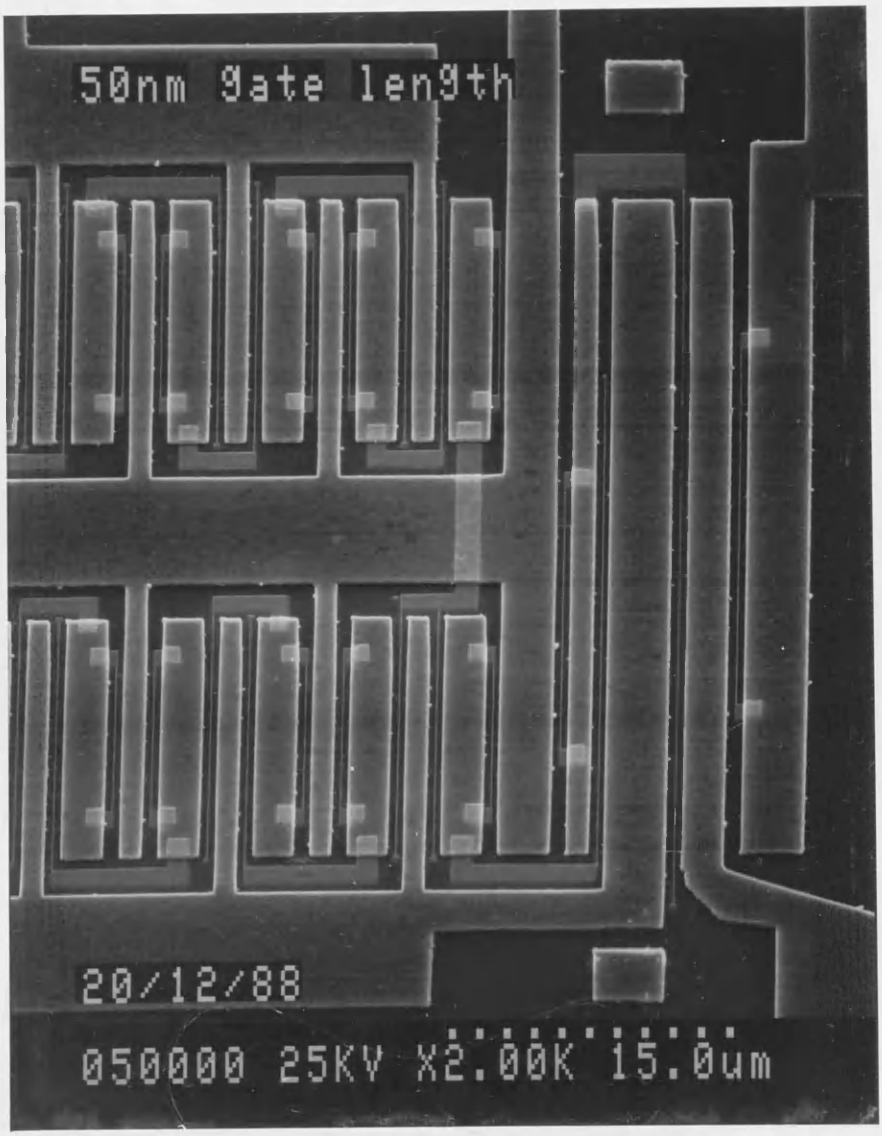


Figure 5.2 Electron micrograph of a 17 stage ring oscillator
(not a working circuit, but a demonstration of the lithographic process)

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Index

Page numbers in **bold** indicate defining equations.