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Ge/SiGe-BASED THERMOELECTRIC GENERATOR



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THESIS SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE
DEGREE OF DOCTOR OF PHILOSOPHY IN
ELECTRONICS AND ELECTRICAL ENGINEERING

SCHOOL OF ENGINEERING,
COLLEGE OF SCIENCE AND ENGINEERING
UNIVERSITY OF GLASGOW

MAY 2016

Abstract

This thesis summarizes the milestones achieved in building a thermoelectric generator (TEG) device using a novel p- and n- type 2-D thermoelectric material called Ge/SiGe superlattice; which was grown by low energy plasma- enhanced chemical vapour deposition (LEPECVD). It begins by describing in a nutshell the advances made in the area of thermoelectrics since its inception in 1821, to the present application of nanotechnology to develop state-of-the-art thermoelectric materials of which the aforementioned material is one. Next, characterisation of the Ge/SiGe superlattice using a combination of experiment and Finite Element (FE) modelling is explained and the results obtained are discussed in comparison with published experimental results. Thereafter, experimental and FE results of the application of the Ge/SiGe superlattice to fabricate a TEG device are presented and discussed. The experimental results on the fabrication of Ge/SiGe TEG device is the first major success at achieving practically feasible voltage output of up to 2.16 mV. For ease of comparison with other published work, an effective Seebeck coefficient of 471.9 μ V/K was estimated. At impedance matched loads of 15 Ω and temperature difference measured across the device of 5.6 K, a power density of 0.111 μ W/cm² and thermal efficiency factor of 0.0035 μ Wcm⁻² K⁻² were also estimated. The results though comparable to a few published works, still required further improvements. The limitations of the TEG that resulted to the low aforementioned performances were discussed; some of which include the restriction of the TEG to a unicouple, having only one p- and n-leg. This limitation is related to the development of the p-type Ge/SiGe material which was identified during the course of this research work. Another major limitation is that the improvised design of the uncoupled TEG, makes use of indium bonding to connect the p- and n- legs electrically in series and thermally in parallel. Indium has a low melting temperature of about 120°C. Hence increasing the heat source above this temperature will dislocate the legs. The consequence of this is that the attainment of a significant temperature difference across the TEG that will eventually result to a high Seebeck voltage, based on the Seebeck effect principle, is limited.

Ways to address these problems were therefore discussed as recommendations for future research work.

Publications

Publications arising from this work:

1. Odia, A., Ferre Llin, L., Samarelli, A., and Paul, D. J., Finite Element Modelling To Evaluate the Cross-plane Thermal conductivity and Seebeck Coefficient of Ge/SiGe Heterostructure., *Materials Today: Proceedings* 2.2 (2015): 510-518.
2. Odia, A., Llin, L. F., Paul, D. J., Cecchi, S., and Isella, G., Modelling and experimental verification of a Ge/SiGe thermoelectric generator. In *Ph. D. Research in Microelectronics and Electronics (PRIME)*, 2015 11th Conference on (pp. 254-257). IEEE. (2015, June).

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Acknowledgement

First and foremost, I wish to acknowledge the guidance of Almighty God for giving me strength and courage to undertake a PhD research at the University of Glasgow, Scotland, United Kingdom.

I am very grateful to my supervisor, Prof Douglas Paul for accepting to supervise me despite my background in this field of research, and most importantly for guiding me throughout the course of the research work. I wish to express my profound gratitude to Dr. Lourdes Ferre Llin whom I sometimes refer to as my 'second supervisor' for making out time to guide and encourage me, as well as proof read my work, despite her busy schedule. To the thermoelectric research team which includes Prof. Douglas Paul, Dr. Lourdes Ferre Llin, Dr. Antonio Samarelli and their partners involved in the Green Silicon project, for making available the thermoelectric materials that were used in this research work for the fabrication of the Thermoelectric generator. I would also like to acknowledge the entire staff of the James Watt Nanofabrication centre (JWNC), Glasgow for training me on how to use the equipment, that were used to fabricate the devices used in this work.

I would like to acknowledge the support of the administrative staff in the School of Engineering, most especially Elaine McNamara, for advice on financial and administrative matters pertaining to my research. To all my friends and colleagues, most especially my office mates, I thank you for the good times we have shared together.

To my church members of the Deeper Christian Life Ministry (DCLM) Glasgow, with Dr. Chima Dioka as my pastor, for their warm fellowship, prayers and support towards a successful completion of my research work.

To my parents, Prof. and Dr. (Mrs) Odia and my siblings; Etiosa, Omosivie, Iyare and Oyenwen for taking care of my responsibilities back home in Nigeria. Lastly but not the least, my loving husband Dr. Akuro Big-Alabo who played a significant role in proof reading my thesis write-up and to my beautiful and cherished daughter Boma Big-Alabo. Both of you brought an invaluable meaning to my life, most especially during the challenging stages of my research.

Finally, I am grateful to my financial sponsor, Petroleum Technology Development Fund (PTDF) Nigeria, for funding the payment of my tuition fees and upkeep for three years, thus making the PhD programme possible.

Author's Declaration

The work presented in this thesis is the original work of the author undertaken at the University of Glasgow, United Kingdom. The copy right of the material in this thesis belongs to the author. Therefore, the author's permission should be obtained if any part of this thesis is to be reproduced in any form. However, where ideas and conclusions from this thesis are referred to in any academic endeavour, it is expected that the author would be properly acknowledged.

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Nomenclature

LEPECVD	Low Energy Plasma Enhanced Chemical Vapour Deposition
Ω	Ohms
ΔT	temperature gradient (or difference)
ΔT_{meas}	Temperature difference measured at top and bottom of heat exchangers
$\Delta T_{\text{p/n_leg}}$	Temperature difference across the top and bottom of the p/n leg
$\Delta T_{\text{superlattice}}$	Temperature difference across superlattice
$\frac{\partial T}{\partial x}$	Per unit temperature gradient
A	Amperes
A_c	Area of the Cold-side heat exchanger
A_G	Generating area, $A_p + A_n$
A_H	Area of the hot-side heat exchanger
A_l	Surface area of a single p- or n- leg
B_2H_6	Di Borane
BPSG	Borophosphosilicate glass
C	Heat capacity
D	Dielectric medium
div	Division
e	elementary charge
E_F	Fermi energy
EMI	Electromagnetic Interference
FE	Finite Element
FEM	Finite Element Model
$g(E)$	Density of states (DOS)
GeH_4	liquid ammonia
H_c	Microhardness of the softer solid in contact (in this case Aluminium)
$h_{\text{constriction}}$	Contact conductance
h_{gap}	Gap conductance
$h_{\text{interface}}$	Thermal joint conductance = $h_{\text{constriction}} + h_{\text{gap}}$
I	current flow
ICP	Inductively Coupled Plasma
I_m	maximum current
J	current density
k_B	Boltzmann constant
L	Lorenz factor (approximately $2.4 \times 10^{-8} J^2 K^{-2} C^{-2}$)
l	length of either p- or n- leg
l_c	contact length
l_o	length of either p- or n- leg
L_{ph}	mean free path of phonons
M_{gap}	Gas parameter that accounts for rarefaction effects at high temperature and low gas pressure

MQW	Multiple Quantum Wells
$n(E)$	carrier density
P	Electrical Power
P_d	Power density
P_G	Generating power output
PGEC	Phonon Glass Electron Crystal
PH_3	Phosphane
P_T	Power Transferred to the Load
Q	Overall heat generated or absorbed
q	heat generated or absorbed per conductor
q	internal heat generated or absorbed.
q	charge
Q_c	rate of heat conduction from cold side (thermal flux)
Q_h	rate of heat conduction from hot side (thermal flux)
Q_{th}	Heat energy transferred due to Fourier's law of heat conduction
r	internal resistance(r_n+r_p)
r_c	total contact resistance
RFI	Radio Frequency Interference
R_L	Load resistance
r_r	realistic internal resistance ($r_n+r_p+r_c$)
R_{th_n}	Thermal resistance of n-leg
R_{th_p}	Thermal resistance of p-leg
$R_{th_{ns}}$	Thermal resistance of superlattice of n-leg
$R_{th_{ps}}$	Thermal resistance of superlattice of p-leg
SiH_4	Silane
T	Temperature
T_c	Cold-side temperature
T_{cj}	maximum temperatures at the cold junction
TE	Thermoelectric
TEG	Thermoelectric Generator
T_h	Hot-side temperature
T_{hj}	maximum temperatures at the hot junction
U_L	Overall heat transfer coefficient of the cold heat exchanger
U_H	Overall heat transfer coefficient of the hot heat exchangers
V	Voltage
V	Voltage
V_L	Load Voltage
V_{oc}	Open circuit voltage
V_r	Realistic voltage
V_{sc}	voltage measured in close circuit ($V_{sc} = V_L$)
Z	Overall Figure of Merit,
ZT	dimensionless figure of merit

Greek symbols

K	$\kappa_n + \kappa_p$, thermal conductance
τ	Thomson coefficient
u_s	Velocity of sound
Π	Pie
α	Seebeck coefficient
κ	Thermal conductivity
κ_e	Electronic thermal conductivity
κ_{ph}	Phonon thermal conductivity
κ_c	Total thermal conductivity of the contacts
$\mu(E)$	mobility
π	Peltier coefficient
σ	Electrical conductivity
σ_{aah}	Effective RMS surface roughness
κ_s	Harmonic mean thermal conductive
γ	Effective gap thickness
φ	Thermal efficiency factor

Subscripts

n	n-leg
p	p-leg
h	hot
c	cold
L	Load
S	Sound
e	Electronic
ph	phonon
1	Input or absorbed
2	Delivered or generated

1. Introduction

Thermoelectricity is a terminology that relates thermal energy with electricity. There are three types of thermoelectric effects: Seebeck effect, Peltier effect and Thomson effect. The Seebeck effect is a phenomenon that describes the generation of electrical energy due to a temperature difference at the junctions of two different conducting materials. The reverse is the case for the *Peltier effect*, where by a temperature difference is generated at the junction of two dissimilar materials when electric current from an external source flows into the device [1]. The third thermoelectric effect, known as the *Thomson effect*, describes the rate of *heating* or *cooling* of a current carrying conductor with temperature gradient. Much emphasis however will be laid on the aspect of thermoelectric generation based on the Seebeck effect principle.

Thermoelectric generators are solid state devices designed to harness unused energy ‘waste heat’ to generate electricity. These devices were predominantly used for military and space projects because they are ‘stand-alone’ reliable source of power generation, requiring little or no maintenance. More importantly, these devices are environmentally-friendly source of renewable energy, in the sense that they do not produce air or noise pollution. Despite low efficiencies (< 5%), studies have demonstrated TEGs to be promising for low temperature waste heat recovery [2]. Hence, they can be seen as a possible source of energy to charge battery cells or super capacitors for a range of autonomous sensors [3].

The overall figure of merit ZT of a thermocouple TEG is given by the following expression [4]:

$$ZT = \frac{\alpha^2}{(\sqrt{\kappa_n \rho_n} + \sqrt{\kappa_p \rho_p})^2} T \quad (1.1)$$

where α is the total Seebeck coefficient (i.e. $\alpha_p - \alpha_n$), κ is the thermal conductivity and ρ is the resistivity, T is the operating temperature. Equation (1.1) suggests that ZT is increased if α is high, ρ is low and κ is small. A higher total Seebeck coefficient will lead to increased voltage in the circuit, a low resistivity will minimise the Joule losses and a low thermal conductivity will aid in retaining maximum temperature difference between the hot and cold

junctions [5]. The material characterisation of the Ge/SiGe superlattice [6, 7] has shown that it combines a high Seebeck coefficient with a low thermal conductivity. This makes the Ge/SiGe superlattice in reference [6, 7] a suitable material for building efficient TEGs and hence the motivation of this present research.

1.1. Aim and objectives

The aim of this research is to design and fabricate an optimized Ge/SiGe-based thermoelectric generator. To achieve this aim the present research seeks to accomplish the following tasks.

1. Evaluation of the measurement techniques developed for the Material characterisation of the Ge/SiGe heterostructure: this task involves using FE modelling to validate the previously published experimental measurements [6, 7] of the cross-plane material properties of the Ge/SiGe heterostructure.
2. Micro-fabrication and measurement of the generating capacity of Ge/SiGe-based TEG module: this task involves two main research activities namely: (i) building a TEG module with single n-leg and single p-leg using the micro-fabricated Ge/SiGe heterostructure as the TE material, and (ii) testing and measuring the generating capacity of the Ge/SiGe-based TEG module.
3. Development of an FEM for Ge/SiGe-based TEG module: this task involves developing an operational FEM of the Ge/SiGe-based TEG module and validating same using the experimental measurements obtained in task 2 above. The advantage of building the FEM is that it could be used to perform complex analyses on the TEG module and obtain information that is difficult or impossible to obtain experimentally e.g. the temperature and heat distribution in the system.
4. Optimal design of the Ge/SiGe-based TEG module to improve its performance: this is the concluding task and it builds on the results obtained in task 3. Here, the validated FEM of the Ge/SiGe-based TEG module is used for optimisation analysis. The optimisation process will focus mainly on geometric (size) optimisation in order to improve the voltage output and the efficiency of the TEG module. The results obtained from this investigation

are intended to form a basis for fabricating a more efficient Ge/SiGe-based TEG that could be used for industrial applications.

1.2. Scope of work

This thesis focuses on the combination of Finite Element Modelling (FEM) and experimental observations to design and fabricate an optimized Ge/SiGe based thermoelectric generator. Mathematical modelling based on the coupled interaction of charge and heat will be used in the numerical simulation software (COMSOL Multiphysics®). Modelling parameters of the Thermoelectric (TE) material (κ , α , σ), will serve as inputs in the numerical software so that predicted outputs of voltage, V and temperatures, T can be generated.

Experimentally, a heat source can be applied to the TE material to raise the hot side temperature T_h (which is also an independent variable in the mathematical model). The generated heat is then conducted across the material so that a temperature gradient ΔT can be obtained. The magnitude of this ΔT is dependent on the thermal conductivity property of the material, κ . As a result of the created ΔT , a differential voltage output, ΔV will be generated and its magnitude is determined by the Seebeck coefficient and electrical properties (α and σ) properties of the TE material. The experimental measurements obtained in this research work, are compared with predicted output voltages and temperatures that are obtained from the numerical simulations.

Another major approach used in this research work is that the basic design theories formulated specifically for thermoelectricity, will be reviewed. These theories will help to evaluate some of the results obtained via the simulations and experiments. Section 1.4 will give some highlights of the various chapters in this work that addresses these approaches.

A flow chart in Figure 1.1 briefly explains the validation process between experiment and FEM, which is a key approach used in this research work.

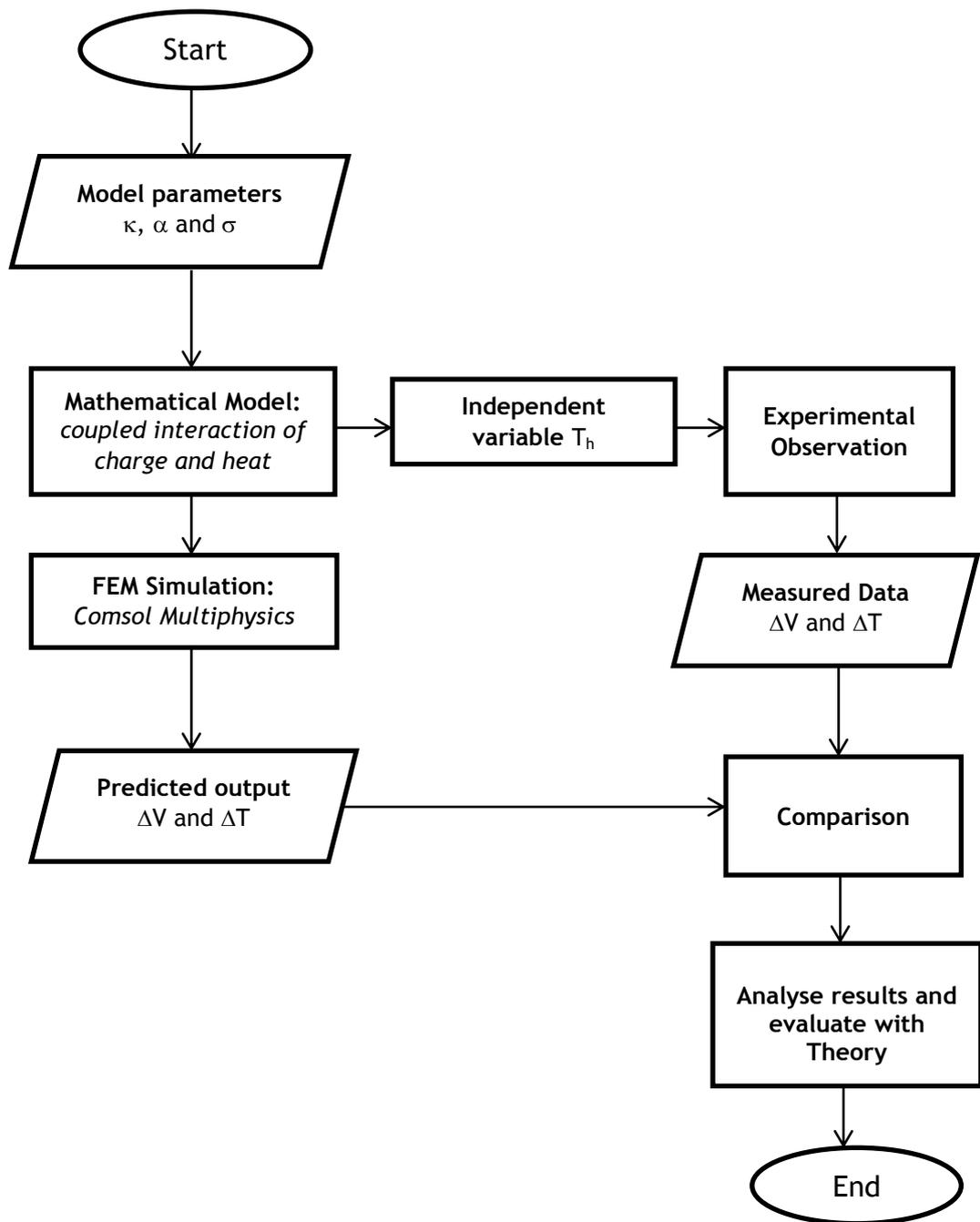


Figure 1.1: Methodological approach for comparing experimental and FEM results

1.3. Research Contributions

The Ge/SiGe heterostructure is a novel TE material that had been designed [8] and grown [9] using conduction band and phonon engineering, and it has the potential to improve on the current performance achieved in the design and fabrication of TEGs. Therefore, it is vital to accurately characterize the material's TE properties and test the material's capability to generate power.

The contributions of this research in working with this material include:

1. The use of FEM to validate previously published experimental results on the material characterisation of a micro-fabricated Ge/SiGe heterostructure [6, 7]. This investigation is the first independent verification of the published Thermoelectric (TE) properties of the Ge/SiGe heterostructure.
2. Micro fabrication of a single p and n TEG module using the Ge/SiGe heterostructure. This was the first major success at achieving a reasonable voltage output (in micro volts), for the single p and n TEG module as compared to the output obtained from the multiple legs design of reference [7] for a similar Ge/SiGe material. Chapter 4 of this research work gives a more detailed explanation of the fabrication process involved in building the TEG.
3. Development of FEM TEG module design. This design was validated based on the experimental results of (2). The verified FE modelling is then used for developing optimal design of the TEG. This will help to save time in conducting rigorous experiments based on trial and error. It will also help to avoid material wastage and thereby save cost.
4. Finally, the micro fabrication of an optimal single p- and n- TEG module, this time, using a more efficient Ge/SiGe material. A break-through in the generated voltage and power output is achieved for the novel materials used. Seebeck voltages up to 2.16 mV and power density up to $0.111 \mu\text{W}/\text{cm}^2$ were realisable in this work. These results, though not the best are comparable to a few literatures of other published works [10]. A detailed discussion of these results is explained in Chapter 6.

1.4. Structure of thesis

The thesis is structured into seven chapters, which includes the introductory and concluding chapters (Chapters 1 and 7 respectively). Chapter 2 is basically a literature survey of thermoelectricity and previously published work that are directly related to this present research work. The main body of the thesis is between Chapters 3- 6. These chapters focus on the discussion of the research contributions stated in Section 1.3. The content of Chapters 3 - 6 are highlighted as follows:

Chapter 3 introduces the design and development of the Ge/SiGe material used in this research work. Thereafter, Finite Element Modelling (FEM) of the Ge/SiGe material is discussed. FEM is used to provide confidence of an experimental technique that was recently developed by the thermoelectrics research group in the School of Engineering, University of Glasgow. The experimental technique was specifically developed for the purpose of material characterisation of the Ge/SiGe material. The FEM was conducted in-line with the published experimental results [6, 7]. This verification was considered necessary because the experimental technique involves thermal measurements which are susceptible to the problems of heat losses and this can affect the accuracy of the results obtained. Hence, this chapter explains how the FEM can be used in conjunction with the experimental technique to obtain more accurate results.

Chapter 4 presents the various stages for fabricating a single p and n- Ge/SiGe-based TEG module. The device was fabricated using the facilities at the JWNC, Glasgow. The chapter also discusses the measurements reading taken for the Seebeck voltages in open and close circuit connection and temperature difference across the device were taken. The experimental measurement was used to estimate a power density of $0.0058 \mu\text{W}/\text{cm}^2$ at $\Delta T_{\text{meas}} = 13.1$ K. The thermal efficiency factor of $0.324 \mu\text{W}/\text{m}^2\text{K}^2$ (or $3.24 \times 10^{-5} \mu\text{W cm}^{-2} \text{K}^{-2}$) was obtained for this device. A detailed explanation of these results is given in Chapter 4.

Chapter 5 presents the validation of Finite Element Model that was specifically developed to model TEGs. The validation was performed using the experimental data obtained from Chapter 4. Thereafter, the FEM was evaluated using analytical method solely for the purpose of ensuring the correctness of the

developed FEM. It is important to note that the FEM developed in Chapter 3 is at the material level and is less complex to develop, while the FEM developed in Chapter 5 is at the module design level, whereby a p-type and an n-type material are coupled together to form a TEG module.

Chapter 6 presents the use of the FEM, to develop an optimal design prior to performing a second fabrication. Optimal designs with respect to the geometrical dimensions of the TEG module were discussed. The geometry of the TEG module was varied with respect to the top and bottom substrate, overall surface area and height of the p- and n- legs. The optimal designs seek to yield an improved performance in the fabricated TEG module with minimum volume of material used, hence making the module cost effective. The second experiment conducted, yielded a far better performance than the first one discussed in chapter 4. The maximum power density realisable was $0.111 \mu\text{W}/\text{cm}^2$ at impedance matched loads of 15Ω and temperature difference measured across the device, ΔT_{meas} , of 5.6 K while a thermal efficiency factor of $0.0035 \mu\text{W cm}^{-2} \text{K}^{-2}$ was obtained.

It is important to state that the p- and n-type material used for the fabrication of the TEG module is more efficient in Chapter 6 than that used in Chapter 4. An elaborate explanation on the effect of using a more efficient material to fabricate TEG modules is discussed in Chapter 5.

2. Literature Review

This chapter reviews various aspects that relates to thermoelectricity and introduces some of the concepts that have been adopted in the present research work. It begins with a brief history of thermoelectricity from its commencement till date. The three thermoelectric effects: the Seebeck, Peltier and Thomson effect as well as the relationship between these effects are discussed. Although all three effects are interrelated, the discussions show that the Seebeck effect is the most important parameter that influences thermoelectric power generation.

The fundamental physics of these three effects are also discussed in detail: this includes the mechanism and manifestation of the three thermoelectric effects, the principles of thermal transport as well as the principles exploited to maximize ZT. Review on state of the art thermoelectric materials is also presented. The uniqueness of such materials is that they allow quasi-independent optimization of the electrical and thermal properties for improved ZT. Furthermore, the coupling of the developed thermoelectric materials for thermoelectric power generation is explained and some microfabrication techniques of TEG modules are reviewed.

Finally, discussion on modelling techniques and design theories for analysis of conventional TEGs are presented. The modelling techniques play a significant role in the evaluation of the TEG module design before fabrication and testing is carried out. This helps to avoid unnecessary waste of time and resources during the process of building the TEG.

This thesis is structured based on the various reviews presented in this chapter i.e. from choice of material to modelling and analysis of typical TEG devices to fabrication and testing of simple TEG devices.

2.1. Brief historical account on thermoelectricity

As stated earlier in Chapter 1, thermoelectricity is a phenomenon whereby thermal energy is converted to electrical energy and vice versa. It involves three major effects namely: Seebeck, Peltier and Thomson effect. The Seebeck effect was initially discovered in 1821 by a physicist named Thomas Johann Seebeck, who observed that the junction of two dissimilar metals at different

temperatures deflected a compass magnet. It was initially believed to be magnetism induced by temperature difference. However, it was soon discovered, according to ampere's law, that an induced electric current deflected the magnet. This effect has long been used for the measurement of temperature and for the detection of thermal radiation. The relationship between the induced voltage and temperature difference is defined by the equation:

$$V = \alpha \Delta T \quad (2.1)$$

In 1834, Jean Charles Peltier discovered that the passage of electric current through a thermocouple yielded a heating or cooling effect at the junction of two dissimilar conductors, depending on the direction of the current flow, I . This phenomenon is called the Peltier effect and is defined as:

$$Q_1 = \pi_1 I \quad (2.2)$$

and

$$Q_2 = -\pi_2 I \quad (2.3)$$

where Q_1 represents heat energy absorbed at the hot junction, Q_2 represents heat energy delivered at the cold junction and π is the Peltier coefficient.

Approximately thirty years later, developments in thermodynamics gave rise to interest in various energy conversion mechanisms. This interest led to the discovery of the relationship between Seebeck and Peltier effect. It also led to the discovery of a third phenomenon known as the Thomson effect. This effect consists of the generation or absorption of heat energy when current flows through a homogeneous conductor in the presence of a temperature gradient. Thus, the Thomson effect is defined as:

$$q = \frac{\partial Q}{\partial x} = \tau I \frac{\partial T}{\partial x} \quad (2.4)$$

The relationship between the Seebeck (α), Peltier (π) and Thomson (τ) coefficients are obtained from the laws of thermodynamics. For example, the first law of thermodynamics states that energy is neither destroyed nor created but changes from one form to another. It is also known as the law of conservation of energy. Based on the energy conservation in the thermoelectric circuit, Thomson derived the equation:

$$\frac{\partial \pi_{1-2}}{\partial T} + \tau_1 - \tau_2 = \alpha_{1-2} \quad (2.5)$$

where $\frac{\partial \pi_{1-2}}{\partial T}$ is the infinitesimal difference between heat absorbed at one junction and heat generated at the other junction and $\tau_1 - \tau_2$ represents the difference between the heat absorbed at one conductor and heat generated at the other conductor.

The second law of thermodynamics states that the total change in the entropy of all processes is equal to zero and this is used to derive a second thermoelectric relation defined as:

$$\alpha = \frac{\pi}{T} \quad (2.6)$$

Equation (2.6) was derived based on the assumption that all three phenomena are reversible. However, the irreversible phenomena of heat conduction and Joule heat generation are inevitable in real thermoelectric systems and hence, Equation (2.6) is inadequate for real systems [4].

Interest in exploiting thermoelectric phenomena for power generation began during the late 19th and early 20th century. Between 1909 and 1911, Altenkirch proposed a theory on what should be the qualities of a good thermoelectric material for power generation. These qualities include low thermal conductivity to minimise heat losses and retain maximum temperature difference across the junctions, and high Seebeck coefficient and electrical conductivity to produce maximum voltage and reduce joule losses in the TEG, respectively. All these qualities are embodied in the figure of merit, ZT, as shown in Equation (2.7):

$$ZT = \frac{\alpha^2 \sigma}{\kappa} T \quad (2.7)$$

Based on this equation, the quality of thermoelectric materials can be assessed. Most metals and metal alloys have a high electrical as well as a high thermal conductivity. Ways to reduce the thermal conductivity so as to improve the ZT becomes difficult because of the Wiedemann-Franz rule defined by Equation (2.8). This makes metals unsuitable materials for thermoelectric power generation.

$$L = \kappa_e / \sigma \quad (2.8)$$

where $\kappa = \kappa_e$ is the electronic thermal conductivity that dominates the total thermal conductivity in metals. Equation (2.8) implies that a reduction in the thermal conductivity, κ , will invariably lead to a reduction in the electrical

conductivity, σ , for a Lorenz factor, L . Hence, an overall improvement in ZT cannot be achieved.

In the early 1950s, semiconductors such as bulk Bi_2Te_3 and PbTe were introduced as thermoelectric materials. The thermal conductivity of a semiconductor material is composed of two parts: the electronic thermal conductivity, which is defined by the Wiedemann-Franz rule stated in Equation (2.8), and the phonon thermal conductivity defined as:

$$\kappa_{ph} = \left(\frac{1}{3}\right) v_s C L_{ph} \quad (2.9)$$

where v_s, C, L_{ph} represent the velocity of sound, heat capacity and mean free path of phonons respectively. Hence, the overall thermal conductivity of a semiconductor is given as:

$$\kappa = \kappa_e + \kappa_{ph} \quad (2.10)$$

The conventional 3D crystalline semiconductor materials, such as bulk Silicon (Si) and Germanium (Ge), have interrelated thermoelectric properties such that independent control of the thermoelectric properties is difficult to achieve. It was however, demonstrated by Ioffe [2] that these semiconductor materials could be alloyed with isomorphous element or compounds to decrease the phonon thermal conductivity, thereby decreasing the overall thermal conductivity. Since only the electronic thermal conductivity is affected by Equation (2.8), the overall thermal conductivity can be reduced without a proportional decrease in the electrical conductivity. Other methods for improving ZT, such as controlled doping and formation of solid solutions, e.g. $\text{Bi}_2\text{Te}_3\text{-Sb}_2\text{Te}_3$, PbTe-SnTe , $\text{Si}_{1-x}\text{Ge}_x$ were developed in the 1960s. Nevertheless, improvements in the ZT of thermoelectric materials were still limited by the fact that materials with suitable thermal and electrical conductivities was lacking. The search for materials with better thermoelectricity properties slowed the progress in the development of high performance thermoelectric materials until the 1990s when more advanced materials were developed due to advancements in nanostructuring. Reviews on the progresses of thermoelectricity and thermoelectric materials have been conducted in references [11] and [12]. It is based on these reviews that the historical account discussed above is developed. The discussed historical account is summarised in Figure 2.1 below.

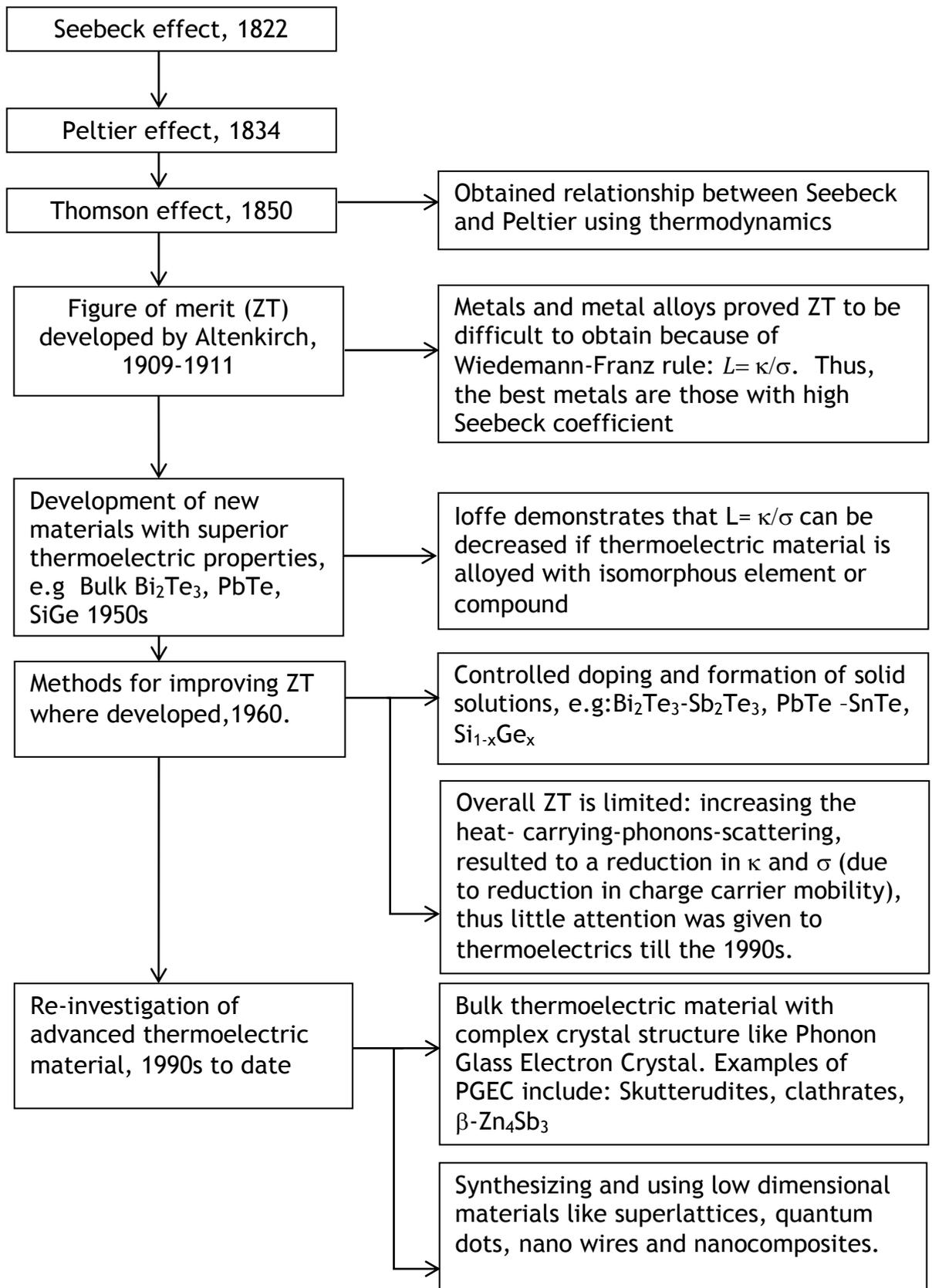


Figure 2.1: Historical account of Thermoelectricity

2.2. Fundamental physics of thermoelectricity

Thermoelectricity involves the coupled interaction between heat and current. The effects that occur in thermoelectricity are the Peltier, Seebeck and Thomson effects. Therefore, it will be worthwhile to understand the mechanism and manifestations of these thermoelectric effects.

2.2.1. Mechanism and manifestations of the thermoelectric effects

1. The Peltier effect

The Peltier effect is each electron for n-type or hole for p-type, in the current flow, carrying a certain amount of heat [13]. The application of current from right to left will cause electrons to flow in the opposite direction, i.e. from left to right while the holes flow in the same direction, i.e. from right to left. In the case of a semiconductor thermoelectric material, it is the majority charge carriers that determine the direction of heat flow. The majority carriers for n-type semiconductors are electrons while that of the p-type are holes. Biasing of n- and p-type semiconductors in the same direction will result in their charge carriers flowing in opposite directions. Consequently, opposite temperature gradients are created for n- and p-type Peltier elements. See Figure 2.2 (a) and (b) below. Also, recall Equations (2.2) and (2.3) which is used to represent these effects.

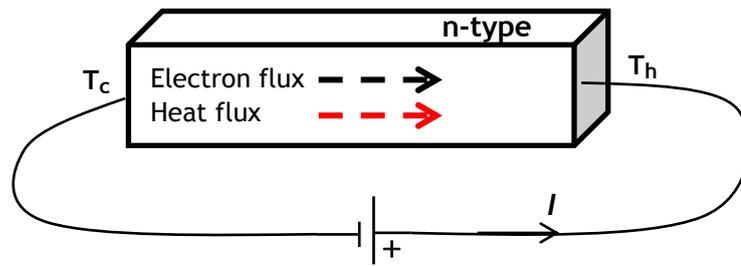


Figure 2.2: (a) Demonstration of Peltier effect in an n-type semiconductor; forward biasing results to the flow of electrons from left to right; Heat flows in the same direction as the electrons

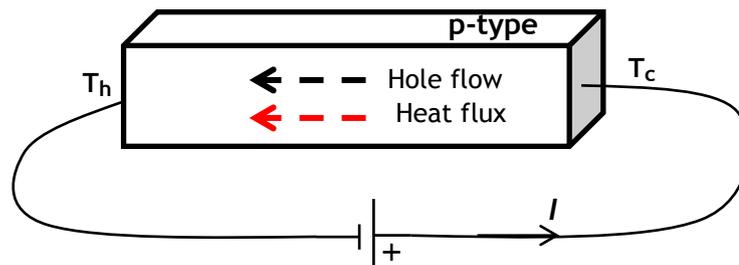


Figure 2.2: (b) Demonstration of Peltier effect in a p-type semiconductor; forward biasing results to the flow of holes from right to left. Heat flows in the same direction as the holes

The heat absorbed by the majority carrier at one end will result to a cooling effect that will cause a drop in temperature T_c , while the heat emitted by the majority carrier at the other end will result to a rise in temperature T_h . Hence, when current is made to flow through a thermoelectric device, a temperature gradient ($T_h - T_c$) will be created across the device. This principle is usually applied in refrigeration processes.

2. The Seebeck effect

The application of a temperature gradient across a semiconductor material will result to the diffusion of majority carriers from the hot to the cold end of the material. Consequently, opposite Seebeck voltages are built up across the material; a negative Seebeck voltage for an n-type material and a positive Seebeck voltage for a p-type material. See Figure (2.3(a) and (b)) below.

The Seebeck effect is given by Equation (2.1) above.

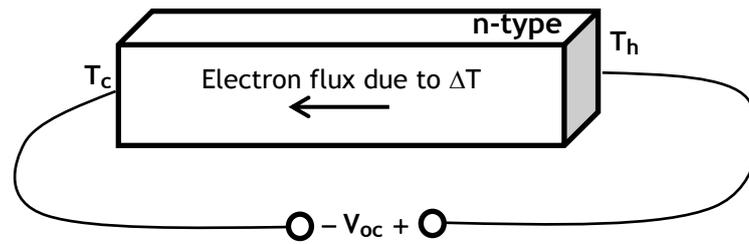


Figure 2.3: (a) Demonstration of Seebeck effect in an n-type semiconductor; application of a temperature gradient will result to a negative Seebeck voltage

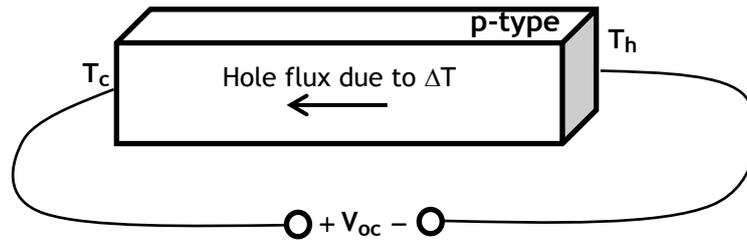


Figure 2.3: (b) Demonstration of Seebeck effect in a p-type semiconductor; application of a temperature gradient will result to a positive Seebeck voltage

3. Thomson effect

The Thomson effect is used to describe the absorption or production of heat when current flows in a material with a temperature gradient. The heat is proportional to both the electric current and the temperature gradient, and the constant of proportionality is called Thomson coefficient. Equation (2.4) above is used to represent this effect.

n-type

The presence of a temperature gradient will cause the n-type semiconductor to have a hotter end at a higher potential and a cooler end at a lower potential (similar to Figure 2.3 (a)). Thus, when current moves from the hotter end to the colder end, it is moving from a high to a low potential, so there is an evolution of heat. This is called the **positive Thomson effect**.

p-type

The presence of a temperature gradient will cause the p-type semiconductor to have a cooler end at a higher potential and a hotter end at a lower potential (similar to Figure 2.3 (b)). Thus when current moves from the hotter end to the colder end, it is moving from a low to a high potential, there is an absorption of heat. This is called the **negative Thomson effect**.

The Peltier, Seebeck and Thomson effects are referred to as reversible effects. However in practice, there are irreversible effects that can occur in the TEG module such as the Joule heating effect.

Irreversible effect

The main irreversible effect that occurs in thermoelectric devices is described by Joule's law of heating, which states that the flow of current through a resistive device will generate a certain amount of heat. Equation (2.11) below is used to explain this effect.

$$Q = I^2 \cdot R \quad (2.11)$$

Equation (2.11) shows that the amount of heat generated is dependent on the resistance of the device and the amount of current flowing through it. The heat generated is transported through the device based on Fourier's law of heat conduction. The latter states that the amount of heat transported through the device is proportional to the temperature difference across the device ($T_h - T_c$) and the dimensions of the device (A/l), where A is the area and l is the length of the device. The constant of proportionality is the thermal conductivity, κ , of the device. Equation (2.12) represents Fourier's law of heat conduction for a 1D transport along a length of solid material.

$$Q_h = -\kappa A \frac{T_c - T_h}{l} \quad (2.12)$$

2.2.2. A typical TEG module design

Thermoelectric generators consist essentially of three parts:

Heat source: the heat source refers to a heating element or substance that is placed in direct contact to one end of the TEG, for the purpose of raising the temperature, T_h , at this end.

Heat sink: refers to a device that is placed in direct contact to the opposite end of the TEG, for the purpose of dissipating heat from the TEG, thereby maintaining, as much as possible, a reduced temperature, T_c , at this end of the TEG.

Thermocouple: This is the combination of p- and n-type thermoelectric materials, in this case a semiconductor material, which converts some of the thermal energy into electrical energy. Thermocouples are often connected in series to form a thermopile with a terminal voltage that is equal to the voltage of one thermocouple multiplied by the number of thermocouples.

The *heat source* and *heat sink* help to create a temperature gradient across the *thermopile*, which is necessary for the generation of a Seebeck voltage. A simplified diagram of a thermoelectric module is illustrated in the Figure 2.4.

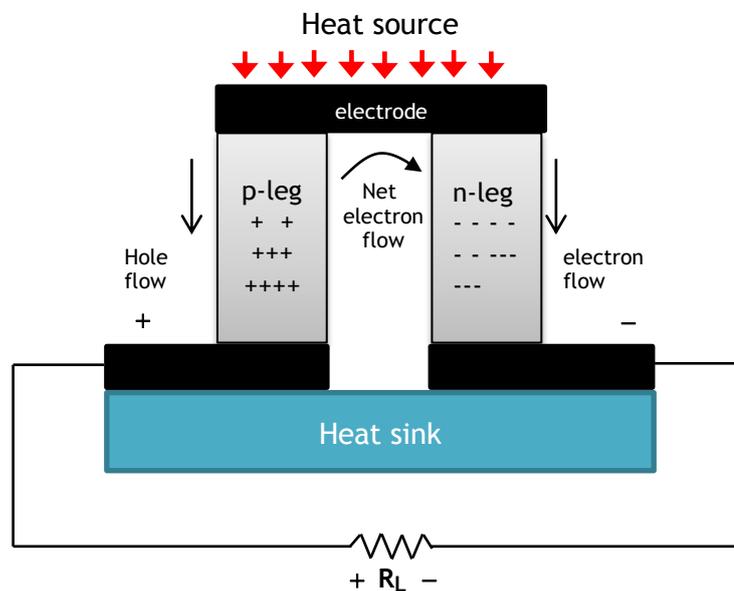


Figure 2.4: Schematic diagram of a TEG formed by a pair of p- and n- legs. A resistor R_L is connected across the module to form a close circuit connection

Let α_p and α_n represent the p-type and n-type Seebeck coefficients respectively.

The thermoelectric e.m.f of the coupled TEG is given by

$$V_{oc} = \int_{T_{cold}}^{T_{hot}} (\alpha_p - \alpha_n) dT \quad (2.13)$$

where V_{oc} is the open circuit voltage generated due to the Seebeck effect. When the circuit is closed with a resistor R_L , a load current I_L , flows through the closed circuit. The load current is determined by the Equation (2.14):

$$I_L = \frac{V_{oc}}{R_L + R_p + R_n} \quad (2.14)$$

where R_p and R_n are the resistances of the p- and n-legs respectively. The power, P_L , delivered to the load resistance is given by:

$$P_L = I_L^2 R_L \quad (2.15)$$

The efficiency, η , is defined as: $\frac{\text{power supplied to load}}{\text{heat absorbed at hot junction}}$, which is expressed mathematically as:

$$\eta = \frac{I^2 R_L}{Q_1 + Q_h - \frac{1}{2} I^2 r} \quad (2.16)$$

where Q_1 is the rate of heat that is absorbed at the hot junction due to Peltier effect. Q_h , which is based on Fourier's law of heat conduction, is the rate at which heat is conducted down the arms from the hot junction to the cold junction. The term $\frac{1}{2} I^2 r$ is based on the assumption that half of the joule heat at the hot junction is not absorbed but dissipated within the thermocouple [14].

The overall figure of merit Z of the thermocouple shown in Figure 2.4 is given by the following expression:

$$Z = \frac{(\alpha_1 - \alpha_2)^2}{[\sqrt{k_1 \rho_1} + \sqrt{k_2 \rho_2}]^2} \quad (2.17)$$

The formation of a p-type and n-type semiconductors can be described using the energy band diagram and this is discussed in the next section

2.2.3. Energy band diagram for p- and n-type semiconductors

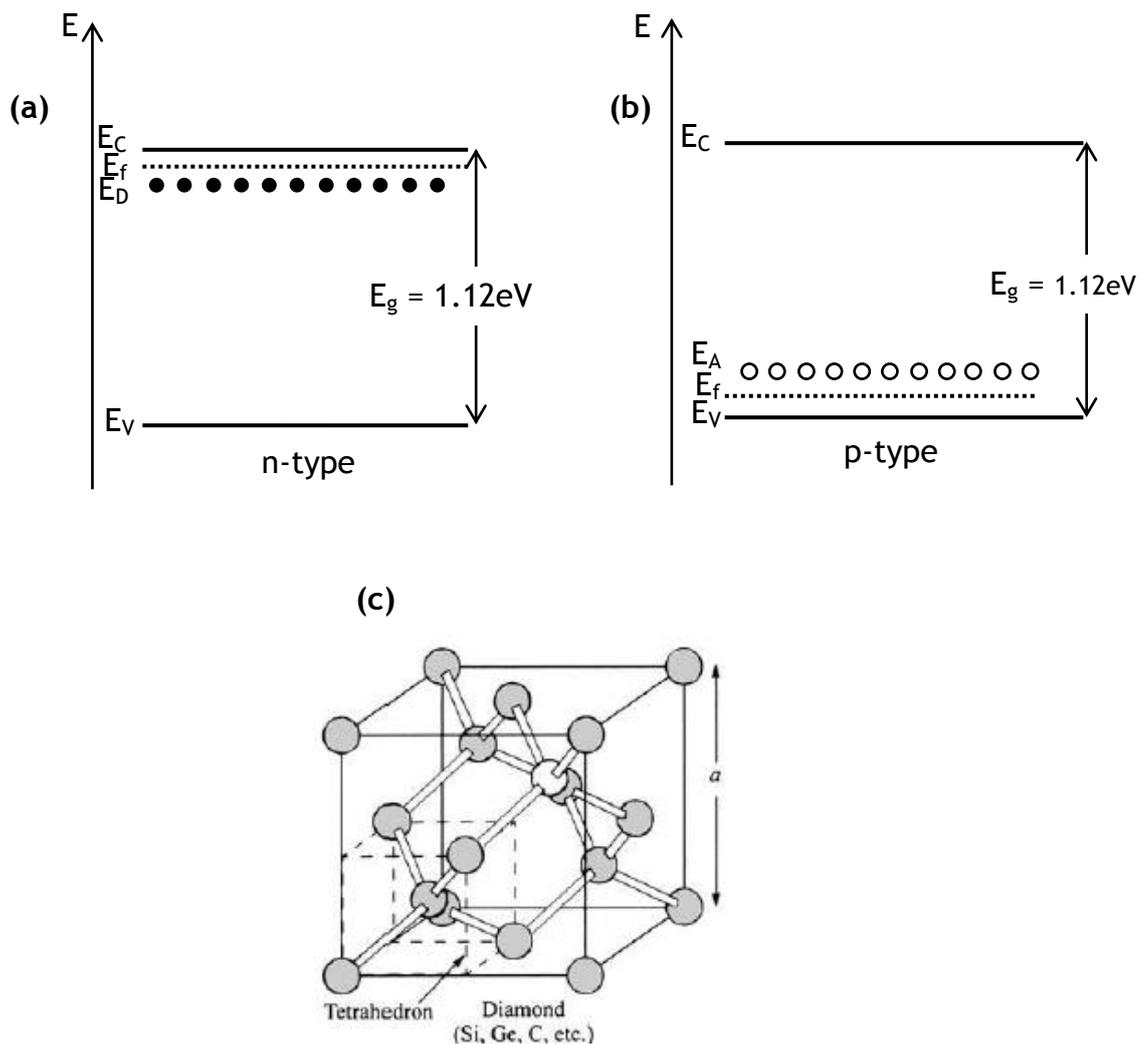


Figure 2.5: Band structure diagram of an extrinsic semiconductor, showing position of (a) donor (for n-type) and (b) acceptor levels (for p-type). E_C , E_V , E_D , E_A and E_f represent the energy levels for the Conduction band, Valence band, Donor, Acceptor and Fermi levels respectively. (c) Simple tetrahedron structure of Si, Ge [17]

The process of adding impurity to semiconductors is referred to as doping and the added impurity is referred to as dopant. There are two kinds of dopants: one that gives negative charge carriers to make an n-type semiconductor and the other that gives positive charge carriers to make a p-type semiconductor. Controlled introduction of impurities can be used to alter the conducting properties of the semiconductor.

Figure 2.5 represents the energy band diagram for a typical extrinsic semiconductor. The donor energy level in the n-type (a) is as a result of the

addition of impurities, such as Phosphorus, Arsenic and Antimony (donor impurity). Since the donor energy level, E_D is very small (0.03 - 0.07 eV) compared to the band-gap energy level of silicon, E_g (1.12 eV) at 300 K, an electron from the donor impurity will jump easily into the conduction band of silicon. The negatively charged electrons will contribute to the material's conductivity, hence making it an n-type semiconductor.

With respect to the p-type (b), the acceptor level is as a result of the addition of impurities, such as Boron, Aluminium and Gallium (acceptor impurity). Similarly, since the acceptor energy level, E_A is very small (0.03 - 0.07 eV) compared to the band-gap energy level of silicon, E_g (1.12 eV) at 300 K, an electron from the silicon valence band will jump easily into the conduction valence shell of the acceptor impurity, leaving behind a hole. The positively charged hole will contribute to the material's conductivity, hence making it a p-type semiconductor.

Many important semiconductors such as silicon have diamond lattice structures which belong to the tetrahedral phases (see Figure 2.5(c)); each atom is surrounded by four equidistant nearest neighbours which lie at the corners of a tetrahedron. The bond between two nearest neighbours is formed by two electrons with opposite spins [17].

2.2.4. Principles and Mechanism of thermal transport

The overall thermal conductivity of a semiconductor has been defined by Equations 2.8 - 2.10 above. A good thermoelectric material is expected to have both high carrier density and a decoupling of the thermal conductivity with $k_{el} \ll k_{ph}$ [13]. In other words, the thermal conductivity of thermoelectric materials is mostly dominated by the phonon contributions.

The thermal transport in such thermoelectric materials can be explained based on the kinetic theory. Assuming there are n -particles in a material, with each particle having a heat capacity, c , in the presence of a temperature gradient, ∇T , the particle will travel with a velocity, v , and its energy, E , will change at a rate of [15]:

$$\frac{\partial E}{\partial t} = cv \cdot \nabla T \quad (2.18)$$

Let the average distance a particle travels before scattering be $v\tau$, where τ is the relaxation time. Therefore, the total heat flow rate per unit area for n -particles is [15]:

$$Q = -\frac{1}{3}nc\tau v^2 \cdot T \quad (2.19)$$

The thermal conductivity as defined by Fourier's law of heat conduction is given as:

$$\kappa = -\frac{Q}{\nabla T} \quad (2.20)$$

Therefore, combining Equations (2.19) and (2.20) the expression for thermal conductivity based on the kinetic theory is obtained as:

$$\kappa = \frac{1}{3}nc\tau v^2 \cdot \nabla T = \left(\frac{1}{3}\right)Cvl \quad (2.21)$$

where $C = nc$ is the total heat capacity and $l = v\tau$ is the particle mean free path [15].

The material used in this study is a low dimensional 2D superlattice structure. A superlattice is a composite material that consists of alternating thin layers of different materials stacked periodically [16]. Superlattices are anisotropic and have different thermal conductivities in the in-plane and cross-plane directions. Thus thermal transport (a) parallel and (b) perpendicular to the layers are discussed briefly:

a. Thermal transport parallel to layers

Thermal transport parallel to the layers is similar to that of bulk semiconductors as earlier discussed. Each layer acts as a phonon waveguide that efficiently channels heat along the layer [15].

b. Thermal transport perpendicular to layers

Thermal transport through the perpendicular layers will result to a decrease in the temperature due to the presence of Thermal Boundary Resistance (TBR) posed by each layer of the superlattice. The decrease in temperature is proportional to the amount of heat that channels through the layers of the superlattices. The effect of this is that the cross-plane thermal conductivity

values will be smaller (up to 4 times) than thermal conductivity values parallel to the layers [106]. Having a low thermal conductivity is desirable for improving the ZT and hence efficiency of TEGs.

One method employed in achieving a low thermal conductivity is by increasing the number of periods in the superlattice structure. This effect has been demonstrated in [107] where the thermal resistance of Si/SiGe superlattices is increased (and hence reduced thermal conductivity) for samples with a larger number of periods. Other literatures also show the enhancement of ZT due to Ge/SiGe and Si/SiGe superlattice structures [110 and 111].

Another method is the use of phonon bandgap structures to block acoustic phonon transport in superlattice structures. This idea was first demonstrated in the literature [108], whereby only phonons at certain wavelengths could pass through the superlattice.

Figure 2.6 below presents the cumulative contribution to the heat transport of the acoustic phonon wavelengths for Si and Ge at 300 K. It suggests that the heat transport via acoustic phonons can be reduced effectively when the superlattice structure is designed to have barrier thicknesses between 1.2 and 3 nm. With this range of wavelength, about 95% of the heat transferred by acoustic phonons can be blocked, thereby reducing the thermal conductivity value.

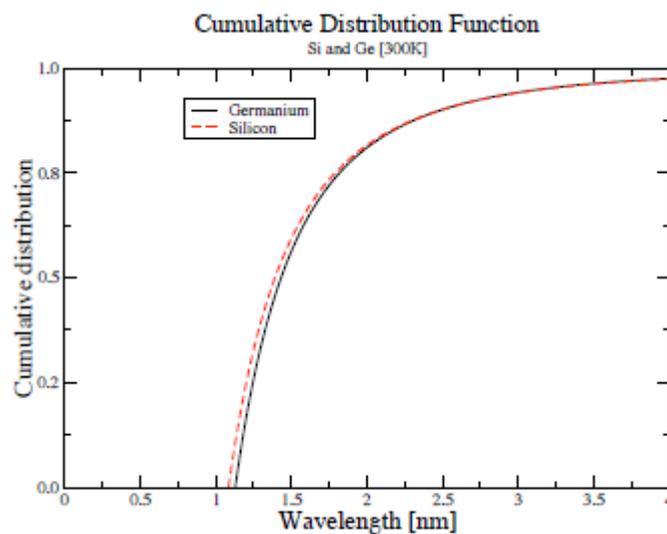


Figure 2.6: cumulative contribution to the heat transport as a function of the acoustic phonon wavelength for both Si and Ge at 300 K [109]

2.2.5. Mechanism of electrical transport

The electrical transport across the superlattice can be explained based on quantum tunnelling mechanism. In order to allow the electrons to flow across the superlattices, the barriers have to be thin enough for the electrons to tunnel. In quantum mechanics, a small barrier-gap will allow electrons to tunnel through the gap, thereby allowing electrical transport through the material. Figure 2.7 is used to describe this process whereby two types of semiconductor materials, Ge and SiGe, are combined.

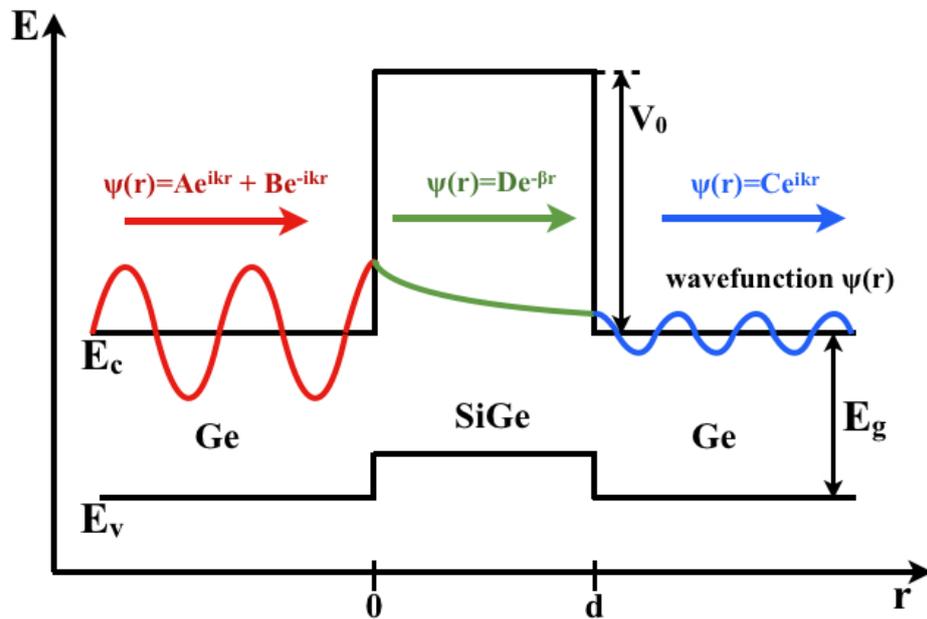


Figure 2.7: Band diagram of a single potential barrier, and the wave function of a particle in the three regions, with its corresponding solutions [18].

In Figure 2.7, three regions are represented for $r \leq 0$, $r \geq d$, and $0 \leq r \leq d$. The particles in motion are represented by the respective wave function in these three regions. Based on Louis de Broglie theory of 1924, particles are said to behave as waves.

The first region $r \leq 0$, represents an incident particle wave function with amplitude A and a reflected wave function with amplitude B , as shown in Equation (2.22) below

$$\psi(r) = Ae^{ikr} + Be^{-ikr} \quad r \leq 0 \quad (2.22)$$

where k is the wavevector defined by $k = 2\pi/\lambda$, and λ represents the wave length.

The second region $r \geq d$, represents the transmitted wave function with amplitude C

$$\psi(r) = Ce^{ikr} \quad r \geq d \quad (2.23)$$

The third region $0 \leq r \leq d$ represents the wave function with amplitude D , through potential barrier, $V(r) = V(0)$, via which the tunneling process takes place.

$$\psi(r) = De^{-\beta r} \quad 0 \leq r \leq d \quad (2.24)$$

where

$$\beta = \sqrt{2m(V_0 - E)/\hbar^2} \quad (2.25)$$

$V(r)$ is the potential energy in the system, m is the effective mass of the particle, $\hbar = h/2\pi$, h is the Planck constant and E is the total energy in the system [19]. Hence, the probability of an incident particle tunnelling through the barrier is given by the transmission coefficient (T), which decays exponentially as the width of the barrier increases [19].

$$T = e^{-2\beta d} \quad (2.26)$$

Finally, it is important to note that superlattices which have the electron transport perpendicular to the quantum well and barriers have the disadvantage that the electrical conductivity also reduces significantly, up to 3 to 4 times lower than bulk materials.

2.2.6. Principles exploited to maximise ZT

The principles exploited to maximize ZT mainly include the variation of the doping density for bulk materials; while for low dimensional structures, quantum confinement and phonon scattering can both be exploited to maximize ZT. These principles are discussed in detail below.

Bulk materials: Variation of doping density

Maximisation of the ZT for bulk material mostly requires the variation of the doping density. However, as a result of the Wiedemann-Franz law, improving one parameter, i.e. the thermal conductivity via doping density does not necessarily improve the ZT. Thus the doping density needs to be varied so as to yield optimal ZT. Figure 2.8 shows a schematic diagram of the electrical and

thermal properties of bulk Bi_2Te_3 thermoelectric material as a function of doping density.

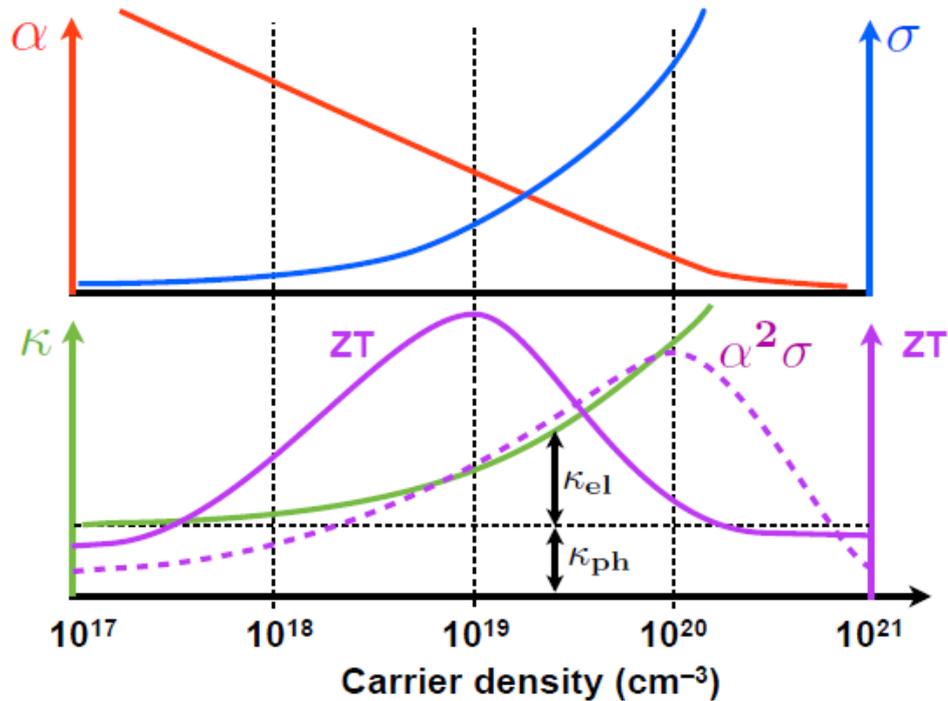


Figure 2.8: Thermoelectric parameters: ZT , Seebeck coefficient α , electrical conductivity σ , thermal conductivity κ and power factor plotted as a function of the carrier density [13]

Figure 2.8, shows the inverse relationship between carrier density and the Seebeck coefficient. A low carrier concentration, gives large Seebeck coefficient

α as given by the equation: $\alpha = \frac{8\pi^2 k_B^2}{3eh^2} m * T \left(\frac{\pi}{3n}\right)^{\frac{2}{3}}$; however, it results to low electrical conductivity as given by the equation: $\sigma = ne\mu$, where k_B is the Boltzmann constant, e is the carrier charge, h is Planck's constant, m is the effective mass of the charge carrier, μ is the mobility and n is the carrier concentration.

Also from Figure 2.8, it can be seen that by increasing the carrier concentration both the electrical and thermal conductivity will increase. These two parameters: σ and κ are linked by the Wiedemann-Franz law which states that the ratio of the electronic contribution of the thermal conductivity (κ_e) to the electrical conductivity, σ is proportional to the temperature, T (i.e. $\frac{\kappa_e}{\sigma} = LT$) where L is the Lorenz factor, which is about $2.4 \times 10^{-8} \text{J}^2 \text{K}^{-2} \text{C}^{-2}$ for free electrons.

The figure shows the maximum ZT to be close to a doping density of 10^{19}cm^{-3} while the maximum power factor is at 10^{20}cm^{-3} for bulk Bi_2Te_3 thermoelectric material.

Low dimensional structures: Quantum confinement and Phonon scattering

Dresselhaus [20] was the first to observe that reduction of the material dimension from 3D to lower dimensions lead to a significant difference in the density of the electronic state of the material. The result of this is that the thermoelectric properties of α , κ , and σ can be varied quasi-independently. Research on improving the ZT of low dimensional materials involves two procedures, viz: (a) quantum-confinement phenomena and (b) phonon scattering.

Quantum-confinement

The use of quantum-confinement phenomena to enhance the Seebeck coefficient is based on the modified form of Mott's relation [21, 22], as given by Equations (2.27 and 2.28).

$$\alpha = \frac{\pi^2 k_B^2}{3 q} T \left\{ \frac{d[\ln(\sigma(E))]}{dE} \right\}_{E=E_F} \quad (2.27)$$

Equation (2.27) shows that the Seebeck coefficient, α could be enhanced by increasing the energy dependence of the electrical conductivity:

$$\sigma(E) = n(E)e\mu(E) \quad (2.28)$$

where k_B is Boltzmann constant, E_F is Fermi Energy, q is charge, e is elementary charge, n is carrier density and μ is mobility. Hence, the enhancement of α could be achieved by enhancing the density of carriers i.e. $dn(E)/dE$, which is a function of the density of states, $g(E)$, or by enhancing the differential mobility $d\mu(E)/dE$.

The density of states, $g(E)$ at a given energy is defined by: $g(E) = dn(E)/dE$.

Low dimensional structures have the potential to enhance the density of states because they have a larger asymmetry in the density of states around the Fermi energy as compared to bulk materials; and Equation (2.27) above shows that this will increase the Seebeck coefficient. Figures 2.8 (a-d) shows the energy dependence of the density of states for bulk materials (i.e. 3D systems), 2D, 1D and 0D systems respectively. The consequence of each plot is that as the

dimensions reduces from 3D to 0D, the asymmetry around the fermi energy level, E_f becomes larger. Based on Equation (2.27), the larger the asymmetry, the larger the Seebeck coefficient will be. Hence as the dimensions reduces from 3D to 0D, the Seebeck coefficient increases as indicated by the arrow (moving from left to right) in Figure 2.9 below.

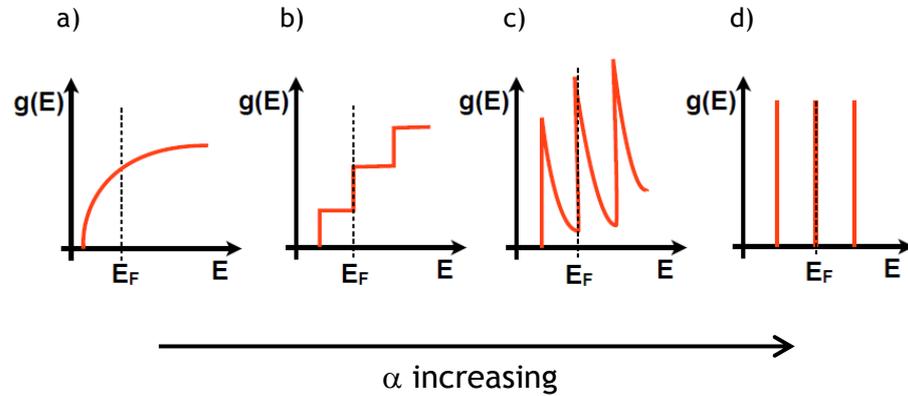


Figure 2.9: Schematic diagram of the energy dependence E of the electronic density of states $g(E)$ for (a) 3D, (b) 2D, (c) 1D and (d) 0D crystals [22]

Phonon scattering.

Theoretical investigations [23] have shown that the lattice thermal conductivity can be reduced significantly by confining phonon dispersion or their mean free path. The confinement of the phonons such that they are dispersed at different frequency range, is known as phonon scattering. Phonon scattering techniques are aimed at reducing the lattice thermal conductivity. These techniques include: umklapp (also known as phonon to phonon scattering) [24], impurity [25] and boundary scattering [26] techniques. Recalling Equation (2.9), it can be seen that confinement of the mean free path of the phonons L_{ph} , will reduce the lattice thermal conductivity.

The main goal is to choose a scattering technique that can scatter phonons more than electrons. For example, adding 0D nanoparticles or quantum dots into a material has been successful at reducing κ faster than σ in a number of material systems for both n- and p-type semiconductors [27, 28 13]. Also, the lower thermal conductivity combined with the higher Seebeck from the 2D quantum well does produce significant enhancement to ZT [13]. Reduction by phonon scattering has been proven for the cross-plane transport in $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ superlattices [29].

Figure 2.10 shows a comparison of of ZT for p-type materials: (p-Sb₂Te₃, p-PbTe, p- CeFe₄Sb₁₂, p-Yb₁₄MnSb₁₁ [97], p-Si_{0.71}Ge_{0.29} [68], 2D p Bi₂Te₃/Sb₂Te₃ [98], 1D Si [99], 0D p-SiGe [100], p-(GeTe)_{0.85}(AgSbTe)_{0.15} [1], 0D p-Bi_xSb_{2-x}Te₃ [101], 0D Mg₂Si_{0.4}Sn_{0.6} [102]); and n-type materials: n-Bi₂Te₃, n-PbTe, n-CoSb₃ [97], n-Si_{0.7}Ge_{0.3} [68], 0D PbSeTe [103], 0D n-SiGe [104], 0D n-PbSe_{0.98}Te_{0.02}/PbTe [105]), all as a function of temperature. The comparison is conducted for both bulk and low dimensional (0D, 1D and 2D) materials.

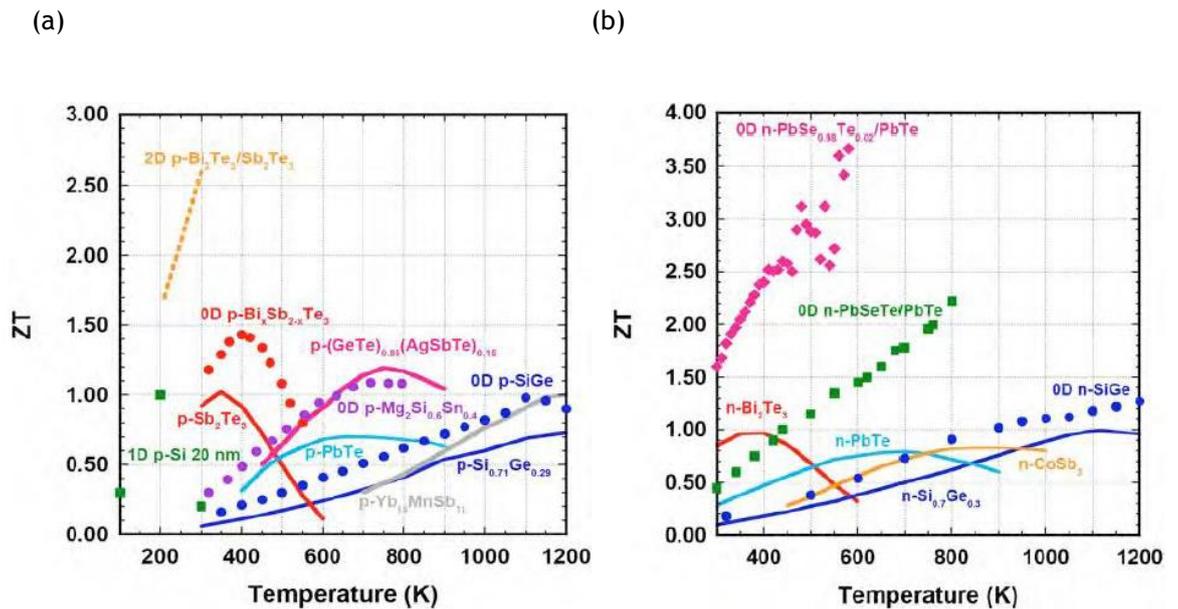


Figure 2.10: (a) a comparison of ZT for p-type material as a function of temperature (b) a comparison of ZT for n-type material as a function of temperature [13]

2.3. Microfabrication techniques and Module design

2.3.1. Infineon

The materials investigated by the Infineon group (i.e. Strasser et al) [30] are pure Poly-Si and Poly-Si_{70%}Ge_{30%}. A 400nm thick layer of the thermoelectric layer (i.e. Poly-Si or Poly-Si_{70%}Ge_{30%}) was developed on a Silicon substrate. The thermoelectric layer was grown using the Chemical Vapour Deposition technique (CVD). The p- and n- thermoelectric layers were fabricated by partial phosphorous-implantation with an energy of 130 keV for the n-legs and partial boron-implantation using 40 keV for the p-legs. Both legs had a doping dose of 10^{16} cm⁻². The thermoelectric layer was isolated from the Silicon substrate using a

1.6 μm thick thermal field oxide barrier. This isolation was considered necessary in order to allow some form of thermal isolation between the cold and the hot side of the thermoelectric legs. Optimization of the heat flux direction within the generator was performed by etching cavities into the Silicon substrate using isotropic CF_4 dry etching. The etched holes were then sealed with Borophosphosilicate glass (BPSG). The connection between the p- and n-leg was achieved using Tungsten and Aluminum [30]. In summary, both the p and n-legs are grown on a single Silicon wafer. Both legs were then connected to form thermocouples that make up the TEG module. Apparently, this approach attempts to optimize the thermal heat flux and reduce electrical resistance by the constructed cavity shown in Figure 2.11 below.

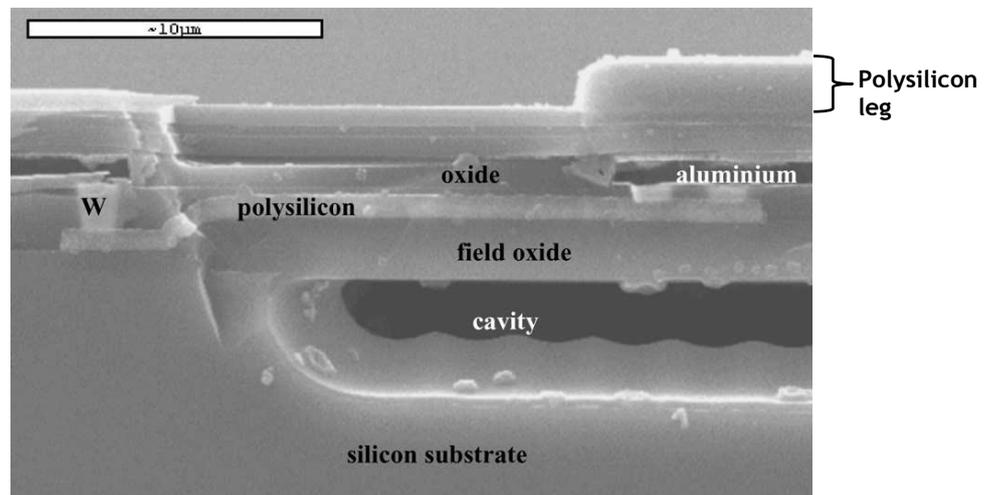


Figure 2.11: SEM-micrograph showing the left half of a micromachined CMOS thermoelectric generator cell, with one polysilicon leg [30]

2.3.2. Micropelt

The Micropelt group (Bottner et al [31]) employed a micro-fabrication technique which is based on a two wafer process; one for the p-type and the other for n-type. The thermoelectric materials investigated are V-VI compounds Bi_2Te_3 for the n-type and $(\text{BiSb})_2\text{Te}_3$ for the p-type. First, 4-inch Silicon wafers were passivated with SiO_2 insulating material. The thinness of the Silicon wafers and insulating material was designed to obtain as low a thermal resistance as possible. However, there might be issues of adhesion of the required thermoelectric layer due to differences in the thermal expansion coefficient between the substrate and the thermoelectric layer.

Next, electrodes were structured on the SiO_2 insulating layer. Thereafter, the $\text{n-Bi}_2\text{Te}_3$ was sputtered on one of the prestructured electrode wafer to form the n-type while the $\text{p-(BiSb)}_2\text{Te}_3$ was sputtered on the other prestructured electrode wafer to form the p-type material. Each of the sputtered thermoelectric material has a layer thickness of $20\mu\text{m}$. Finally, the p- and n- type materials were bonded to form the TEG via flip chip bonding method (see Figure 2.12). The SEM picture of the p-type leg is also shown in Figure 2.13.

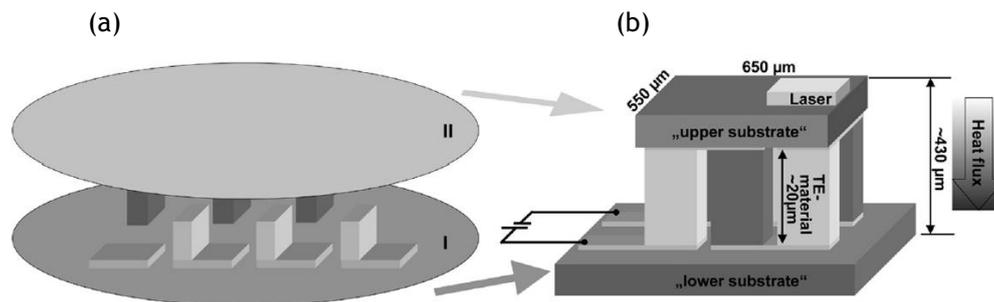


Figure 2.12: (a) Schematic diagram of the flip-chip bonded thermoelectric material and (b) schematic diagram of the device after flip chip bonding. Note wafers I and II represent the n- and p-type materials respectively [31].

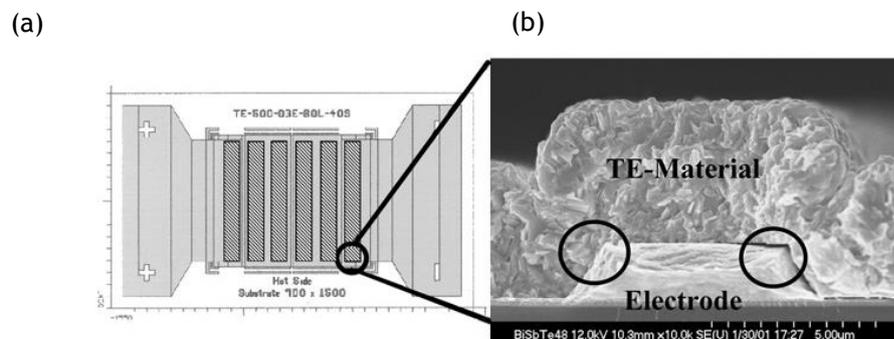


Figure 2.13 (a) Thermoelectric generator design with electrodes (or terminals) at the end (light gray) and (b) cross section of SEM picture showing the overgrowth of a $5\mu\text{m}$ thick $\text{p-(BiSb)}_2\text{Te}_3$ layer over a contact electrode [31]

In general, it is observed from the above two techniques discussed in sections 2.3.1 and 2.3.2 that only a single thin film material is deposited as the thermoelectric layer. It is also observed that multiple legs from the thin film were created on a single Silicon wafer. Hence, one can infer that the use of a single thin film material allows for creation of multiple legs, which can be made to be either continuous or discontinuous, on a single Silicon wafer.

A special kind of nanostructured TE materials is superlattices and they consist of alternating thin layers of different materials that are stacked periodically [32]. Superlattices have been used for fabrication of TEG modules [33 and 34] and offer certain advantages over single-layer TE materials. However, in comparison to the literature on single-layer TE materials relatively few studies have been conducted using superlattice because the latter is a recently emerging area of study. In the next section, a study conducted on the fabrication of TEG using superlattice is discussed to show the fabrication technique involved. Also, the limitations and advantages of using superlattices are discussed.

2.3.3. Fabrication of TEG based on superlattice TE materials

In reference [33], the thermoelectric layer used is SiGe/Si superlattice structures. SiGe is considered to be one of the best materials for high temperature applications. Moreover, superlattice structures can enhance the thermoelectric properties by reducing the thermal conductivity as well as improving the Seebeck coefficient of the thermoelectric material [33].

In fabricating the SiGe/Si-based TEG in reference [33], the first step was to grow a 3.95 μm SiGe graded buffer layer on 650 μm Silicon wafer. Next, 3 μm SiGe/Si epitaxial layers were grown on the graded buffer using Molecular Beam Epitaxy (MBE). The buffer layer is required to compensate for the lattice mismatch between the Si substrate and the SiGe/Si superlattice layer. Then, several chips grown in a similar fashion are bonded to a top and bottom Aluminium nitride (AlN) plate with gold as the connecting electrode that links the various chips. Thermal sensors are placed between the top and bottom AlN plates to read the temperature difference across the TEG module. Schematic diagrams of the power generator system are shown in Figure 2.14 (a) and 2.14 (b) below.

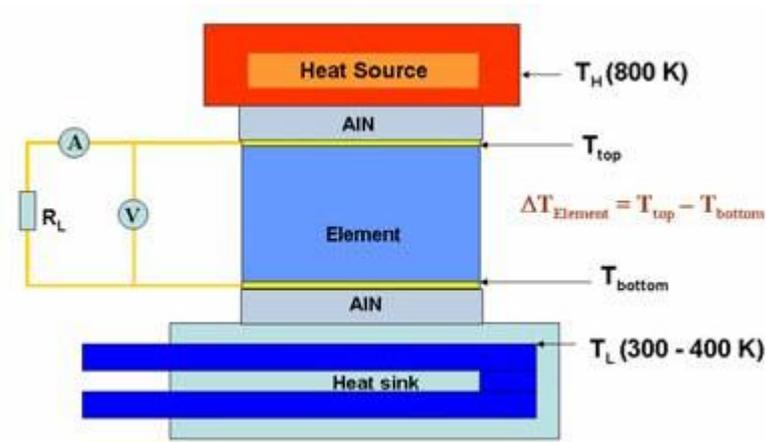


Figure 2.14 (a): Schematic diagram of power generator design [43].

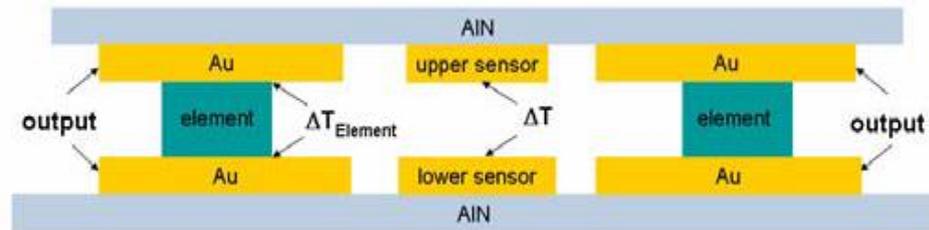


Figure 2.14 (b): Schematic diagram of multiple power generators with built-in thermal sensor [33]

In a more recent literature [34], a similar thermoelectric module design was considered whereby the p-leg was made from $\text{Sb}_2\text{Te}_3/\text{Bi}_2\text{Te}_3$ superlattice and the n-leg was made from $\text{Bi}_2\text{Te}_{3-x}\text{Se}_x$ thin film. The thermoelectric module in this case is used as a cooler rather than a generator (see Figure 2.15).

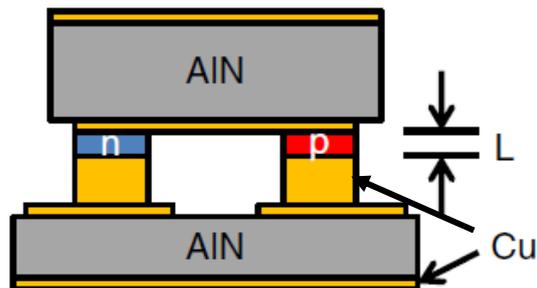


Figure 2.15: Schematic diagram of thin-film-based thermoelectric module, showing top and bottom AlN headers, Cu traces and n-type and p-type active elements. L represents $8\mu\text{m}$ length of the thermoelectric layer [34]. (Diagram not drawn to scale)

A major limitation of using superlattice structures to build TE modules is that superlattices require a buffer layer to help minimize the strain due to lattice mismatch between the alternate combinations of elements that make up the superlattice structure. By growing a buffer layer on the substrate it becomes

difficult to deposit an electrode on the substrate (or even on the buffer layer) that will help in connecting the multiple legs that can be created from the thermoelectric layer, which in this case is the superlattice.

Hence, in order to achieve a series combination of the Seebeck voltage generated by each leg, it may be necessary to grow the material and bond it to an external plate (such as AlN) as described in [33 and 34]. Thereafter, several sections can be etched down to the plate so that each leg now comprises of the superlattice, buffer and substrate layer. The p-type plate can then be bonded to the n-type plate, using flip chip bonding technique, to form the p-n TE module.

In order to overcome this limitation, the material used in this research work was developed in such way that another thin layer of semiconductor was grown on the buffer layer. This layer has the same constituents as the buffer layer except that it was made to be highly doped so that it could act as an electrode. Thereafter, the superlattice structure was grown on this ‘electrode’ layer which is referred to as the bottom contact. Multiple legs created from the superlattice structure can then be connected via the ‘electrode’ layer. A detailed description of this material will be given in Chapter 3 of this thesis. A comparison of the different TE materials and microfabrication techniques are presented in Table 2.1. The table also compares the performance of the fabricated TE module in terms of the thermal efficiency factor.

The thermal efficiency factor is an estimated factor that is used to determine the performance of a given TEG in comparison to another TEG. It is obtained by calculating the power density generated per squared temperature difference across the TEG.

The thermal efficiency factor, φ is given as [10]:

$$\varphi = \frac{P_G}{A_G \Delta T_{meas}^2} = \frac{P_d}{\Delta T_{meas}^2}$$

Table 2.1: Comparison of the performances of various micro fabricated TEGs

Group/ Author/	Material type	Material properties			Generator thermal efficiency factor $\mu\text{W}/(\text{K}^2.\text{cm}^2)$
		Seebeck coeff (μVK^{-1}) α	Electrical resistivity ($\text{m}\Omega.\text{cm}$) ρ	Thermal conductivity $\text{W}/(\text{m.K})$ κ	
Infineon/ Strasser et al [30]	Poly-Si (p-n)	160 ± 9	2.214 ± 0.004	31.4 ± 5.2	0.0426
	poly-SiGe(p-n)	136 ± 11	2.12 ± 0.04	10.3 ± 2.8	0.0352
Micropelt /Bottner et al [31]	V-VI compounds n- Bi_2Te_3 p- $(\text{BiSb})_2\text{Te}_3$	340 (p-n)	1.6/1.2 (p/n)	-2 to 3 (n)	2.4
Yang et al [35]	Poly-Si (p-n)	160 (p-n)	2.21/0.813 (p/n)	31.2/31.5 (p/n)	0.0427
Huesgen et al. [36]	Al/Poly-Si (p/n)	1.7/107 (p/n)	0.043/6.294 (p/n)	237/37.3 (p/n)	0.00363
	p- $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$ n- $\text{Bi}_{0.87}\text{Sb}_{0.13}$	100/230 (p/n)	17.25/7.15 (p/n)	1.05/3.10 (p/n)	0.00814
Perez- Marín et al. [37]	Si (Ultra thin Si membranes),	400	10	60	0.18
XIE et al [38]	Poly-Si (p-n)	147/132 (p/n)	2.786/1.932 (p/n)	31.4	0.052
Yu et al[39]	Poly-Si (p-n)	279.3 ± 1.4 (p-n)	3.3/2.3 (p/n)	31.4	0.252
Zeng et al. [33]	SiGe/Si superlattice	420	-	10	0.082

Table 2.1 presents a comparison of the performances of various micro-fabricated TEGs. The properties (i.e. α , ρ and κ) of the materials used to build the various TEGs are highlighted for either p-type or n-type materials (indicated as p/n) or a combination of both types of material (indicated as p-n). Where this is not indicated the implication is that only one type of material is used to build the TEG [33, 37].

Although there are a number of factors that affect the performance of the TEG, such as the number of thermoelectric legs and the fabrication and soldering techniques employed, the materials used in fabricating the TEG significantly affects its performance. Recall that from the definition of Figure of merit (see Equation (2.7)) a material with a high ZT is desirable. In other words, a material with high Seebeck value, low electrical resistivity and low thermal conductivity is desirable. From Table 2.1, it can be seen that Micropelt [31] yields the highest

thermal efficiency factor of 2.4. This can be attributed to the better quality of the materials used by Micropelt [31], p-(BiSb)₂Te₃/ n-Bi₂Te₃, to fabricate the TEG unlike the low quality of material, Al/Poly-Si, used by Huesgen et al. [36].

Although Micropelt [31] may be considered a matured technology and Bismuth Telluride (i.e. Bi₂Te₃/Sb₂Te₃) yields the best TEG performance, even up to date, Tellurium is considered to be the 9th rarest element available. It is toxic and volatile at high temperatures, which makes it non-ideal for commercial purposes [1, 40]. Thus, there is enormous interest from industry to move to sustainable and less volatile materials.

In the next section, modelling techniques and design theories for analyses of TEG modules are reviewed. It is vital to develop a comprehensive modelling technique that can be used to evaluate a TEG module configuration before the actual fabrication of the device. Hence, the accuracy, limitations and advantages of modelling techniques and design theories should be considered in choosing an appropriate model for pre-fabrication analysis.

2.4. Modelling techniques

The modelling techniques used in the literature to model a TEG are basically divided into two major categories: (a) models based on averaging schemes and (b) models based on local energy balance equations. The averaging scheme models assume a thermal balance of heat input Q_{in} and heat rejection Q_{out} with symmetrical distribution of the Joule heating effect of the thermoelements. It also assumes that the thermoelectric properties (i.e. α , κ and σ) of the legs do not vary with temperature. A review of some averaging scheme models, such as simplified and improved simplified models, has been conducted by Fraisse et al [41].

2.4.1. Simplified models

Consider the conventional flow of heat flux in a single thermoelectric leg as shown in Figure 2.16.

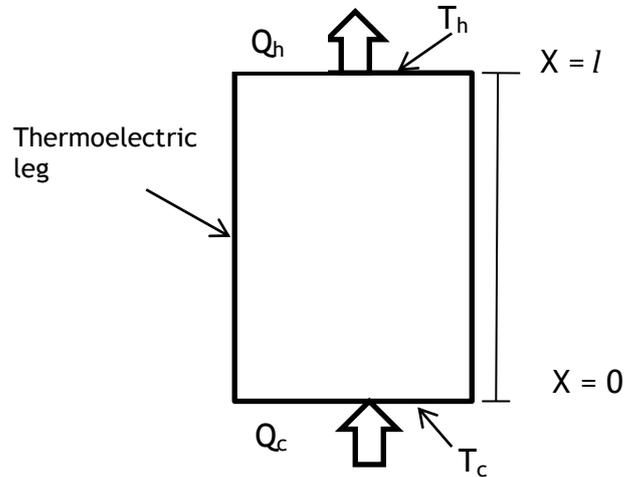


Figure 2.16: Heat flux flow in a single thermoelectric leg [41].

The thermoelectric parameters α , κ and σ are assumed constant and estimated at the mean temperature given by $T = (T_h + T_c)/2$. Hence,

$$Q_h = \alpha \cdot I \cdot T_h + K \cdot \Delta T - \frac{1}{2} r \cdot I^2 \quad (2.29)$$

$$Q_c = \alpha \cdot I \cdot T_c + K \cdot \Delta T + \frac{1}{2} r \cdot I^2 \quad (2.30)$$

$$r = \frac{l}{\sigma \cdot A} \text{ and } K = \frac{\kappa \cdot A}{l}$$

where r is the total resistance and K the total thermal conductance of the length l

The power (P) and efficiency (η) are obtained from Equations (2.29) and (2.30) as shown:

$$P = Q_h - Q_c = \alpha \cdot I \cdot \Delta T - r \cdot I^2 \quad (2.31)$$

$$\eta = \frac{P}{Q_h} \quad (2.32)$$

In some studies [42, 43] where this modelling approach has been implemented the Thomson effect is neglected because the Seebeck effect is assumed to be constant. Although this assumption is usually made for ease of calculation, it has been shown that Thomson effect affects the maximum power and conversion efficiency significantly [44]. Hence, the simplified models of Equations (2.29) and (2.30) can be modified to account for the Thomson effect as follows [45]:

$$Q_h = \alpha \cdot I \cdot T_h + K \cdot \Delta T + \frac{1}{2} r \cdot I^2 - \frac{1}{2} \cdot \tau \cdot \Delta T \quad (2.33)$$

$$Q_c = \alpha \cdot I \cdot T_c + K \cdot \Delta T - \frac{1}{2} \cdot r \cdot I^2 + \frac{1}{2} \cdot \tau \cdot \Delta T \quad (2.34)$$

The averaging scheme model has the advantage that it involves less computational effort than other methods [45]. Also, as a result of its simplicity, it provides quick information about the performance of the device being studied. However, vital information about the performance of the device may be lost when using the averaging scheme [45]. The models derived from the energy balance equations are more realistic because the thermoelectric properties are treated as being temperature-dependent. Hence, more accurate information about the distribution of temperature and heat energy across the legs of the TEG module can be obtained.

2.4.2. Model derived from the energy balance equation

Thermoelectricity involves the coupled interaction between charge and heat as stated in Equations (2.35) and (2.36). The current density is represented as J .

$$E = \rho J + \alpha \nabla T \quad (2.35)$$

$$q = \pi J - \kappa \nabla T \quad (2.36)$$

From these Equations there are four significant transport coefficients namely: resistivity (ρ), Seebeck coefficient (α), Peltier coefficient (π) and thermal conductivity (κ) [46]. Equations (2.35) can also be written as:

$$J = \sigma(E - \alpha \cdot \nabla T) \quad (2.37)$$

For thermoelectric analysis, the heat flow equation is given by:

$$\rho C \frac{\partial T}{\partial t} \cdot u + \nabla \cdot q = Q \quad (2.38)$$

and the continuity of electric charge equation is given by:

$$\nabla \cdot \left(J + \frac{\partial D}{\partial t} \right) = 0 \quad (2.39)$$

where Equations (2.38) and (2.39) are coupled by Equations (2.36) and (2.37) and by the constitutive equation for a dielectric medium [47] given in equation (2.40) below.

$$D = \varepsilon \cdot E \quad (2.40)$$

In the absence of time-varying magnetic fields (i.e. in open circuit), the electric field E can be derived from the electric scalar potential, V , and is given by:

$$E = -\nabla V \quad (2.41)$$

Under steady-state conditions, Equations (2.38) and (2.39) simplify to the following equations:

$$\nabla \cdot q = Q \quad (2.42)$$

$$\nabla \cdot J = 0 \quad (2.43)$$

By substituting Equations (2.36), (2.37) and (2.41) into Equations (2.42) and (2.43), the coupled thermoelectricity equations are derived as shown in Equations (2.44) and (2.45):

$$\nabla \cdot (\pi J - \kappa \nabla T) = Q \quad (2.44)$$

$$\nabla \cdot (\sigma \cdot \nabla V + \sigma \cdot \alpha \cdot \nabla T) = 0 \quad (2.45)$$

Rearranging equation (2.45) gives

$$\nabla V = -\alpha \cdot \nabla T \quad (2.46)$$

The electrical power spent on Joule heating is defined by:

$$Q = J \cdot E \quad (2.47)$$

From Equations (2.35) and (2.47),

$$Q = J \cdot (\rho J + \alpha \nabla T) \quad (2.48)$$

Assuming an isentropic process, Equation (2.48) can be re-written as:

$$Q = \frac{J^2}{\sigma} + J \cdot \frac{\pi}{T} \cdot \nabla T \quad (2.49)$$

Note that in arriving at Equation (2.49), the relationship $\pi = \alpha T$ was applied. The relationship between π and τ is defined mathematically as:

$$\frac{\pi}{T} = \frac{d\pi}{dT} - \tau \quad (2.50)$$

However, for steady-state conditions

$$\frac{\pi}{T} = -\tau \quad (2.51)$$

Hence, Equation (2.49) can be rewritten as:

$$Q = \frac{J^2}{\sigma} - J \cdot \tau \cdot \nabla T \quad (2.52)$$

Using Equations (2.52) and (2.44), the complete equation becomes:

$$\nabla \cdot (\pi J - \kappa \nabla T) + J \cdot \tau \cdot \nabla T = \frac{J^2}{\sigma} \quad (2.53)$$

From Equations (2.46) and (2.53), the parameters that account for reversible effects are α , π and τ while the parameters that account for irreversible effects are κ for heat conduction effects and σ for Joule heating effects. Thus, the derived models (of Equations (2.46) and (2.53)) are considered to be more realistic than the averaging scheme models, because they account for both reversible and irreversible effects [48] and incorporate all three thermoelectric effects (i.e. α , π , and τ). Solutions to these models may require much computational time and effort depending on the complexity of the structure being studied. For this reason, the models are usually implemented in computational software packages such as ANSYS™ [47] and COMSOL Multiphysics® [49, 50]. The modelling techniques discussed above can be applied to model a typical TEG module with both p-leg and n-leg connected electrically in series and thermally in parallel.

2.5. Design Theories for Modelling an Efficient Thermoelectric generator

Design theories have been developed for modelling an efficient thermoelectric generator. These analytical models include Ioffe's [4], Min and Rowe's [51-53], and Wu's [54] design theories. These models are specifically geared towards obtaining maximum power output. For example, in order to achieve maximum power output, Ioffe's [4] model shows the importance of impedance matching of the internal circuit resistance and the external load resistance. A major limitation of this model is that it does not account for thermal and electrical contact resistances which are inevitably present as the dimensions of the thermoelement reduces. The motivation therefore, for Min and Rowe's design theory is to overcome the limitation of Ioffe's [4] model. This involves modification of Ioffe's [4] model to incorporate thermal and electrical contact resistances. Min and Rowe's [51-53] model provides guideline in selecting or modifying the geometry of thermoelements to achieve maximum power output [52].

Wu's [54] theory proposes a real thermoelectric power using waste heat. The specific power output is compared with that of the Carnot reversible heat engine. The theory shows that reversible limits are not close enough to real performances of actual processes [54]. It points out that the Joulean heat loss and thermal conduction heat flow contributes to the internal irreversibility. Moreover, the reversible Carnot heat engine does not produce output power. It only provides an upper bound limit that is far from being realistic. Hence the motivation is to model a more realistic upper bound limit via which other results can be compared with.

A detailed description of all three models are discussed next.

2.5.1. Ioffe's design theory [4]

The performance of a TEG is usually evaluated based on its efficiency and output power. To develop more efficient TEGs, Ioffe [4] proposed a design theory that can be used to determine the optimum cross-sectional area between the p-leg and n-leg. The formulation of this theory is explained as follows.

Efficiency:

Based on the simple model discussed in Section 2.5.1, the efficiency (η) of a TEG is defined as the ratio of power (P) supplied to the load (R_L) to the heat energy (Q_h) absorbed at the hot junction.

The absorbed heat energy comprises of:

- The heat energy received at the hot junction due to Peltier effect defined as $Q_{\text{peltier}} = \alpha I T_h$,
- The heat energy transferred from the hot to cold junction due to Fourier's law of heat conduction defined as $Q_{\text{th}} = K(T_h - T_c)$, where $K = \kappa A/L$.
- Heat lost via Joule heat defined as half of the input heat [1].

The output power delivered by the TEG is defined as $P_{\text{out}} = I^2 R_L$. Therefore, the efficiency of a TEG is derived thus:

$$\eta = \frac{I^2 R_L}{\alpha \cdot I \cdot T_h + K \cdot (T_h - T_c) - \frac{1}{2} I^2 r} \quad (2.54)$$

From Ohm's Law, the current, I , is given by:

$$I = \frac{\alpha(T_h - T_c)}{R_L + r} \quad (2.55)$$

where $\alpha = \alpha_p + \alpha_n$. Putting $m = R_L/r$, the efficiency of the thermoelectric generator is derived as [4]:

$$\eta = \frac{T_h - T_c}{T_h} \times \frac{m/(m+1)}{1 + (Kr/\alpha^2) \times (m+1)/T_h - \frac{1}{2}(T_h - T_c) \times 1/(m+1)} \quad (2.56)$$

From Equation (2.56), Ioffe [4], considers the following parameters to be significant in order to obtain an optimum efficiency:

- hot and cold junction temperatures, T_h and T_c ;
- material properties, Kr/α^2 and
- ratio, $m = R_L/r$

Optimum cross-sectional area

The optimum cross-sectional area is the area that produces a minimum of the product, Kr , thus resulting in the maximum efficiency. Let S_p and S_n be the cross-sectional area for the p-leg and n-leg respectively. The product, Kr , is given as:

$$K r = (\kappa_p S_p + \kappa_n S_n) \left(\frac{\rho_p}{S_p} + \frac{\rho_n}{S_n} \right) = \kappa_p \rho_p + \kappa_n \rho_n + \kappa_p \rho_n \left(\frac{S_p}{S_n} \right) + \kappa_n \rho_p \left(\frac{S_n}{S_p} \right) \quad (2.57)$$

To find the minimum condition Equation (2.57) is differentiated with respect to ratio $\frac{S_p}{S_n}$ and the derivative is equated to zero. Accordingly, the expression for optimum cross-sectional area is obtained as:

$$\frac{\rho_p}{\kappa_p} \times \frac{\kappa_n}{\rho_n} = \left(\frac{S_p}{S_n} \right)^2 \quad (2.58)$$

By substituting Equation (2.58) into Equation (2.57), the following expression is obtained as the condition for optimum cross-sectional area.

$$K r = (\sqrt{\kappa_p \rho_p} + \sqrt{\kappa_n \rho_n})^2 \quad (2.59)$$

Based on Equation (2.59) Ioffe [4] obtained the expression for the figure of merit, ZT, of a TEG thermocouple as:

$$ZT = \frac{\alpha^2}{K r} T = \frac{\alpha^2}{(\sqrt{\kappa_p \rho_p} + \sqrt{\kappa_n \rho_n})^2} T \quad (2.60)$$

In order to design an efficient TEG using the optimum cross-sectional area of the p- and n-leg, it is important to accurately measure the thermoelectric material properties of α , κ and σ (or $\rho = 1/\sigma$). Derivations for the maximum power output were obtained at $m = 1$ (i.e. $R_L = r$) which is necessary for maximum power transfer for any current source. Derivations for maximum efficiency were also obtained by differentiating Equation (2.56) with respect to m and equating the derivative to zero (i.e. $\frac{d\eta}{dm} = 0$).

Ioffe's design [4] is based on the simple model, which does not account for thermal and electrical contact resistances. It has been demonstrated by Min and Rowe [51, 52] that the influence of contact resistances in the TEG becomes more significant as the ratio of length to cross-sectional area of the p-leg and n-leg decreases. Hence, modification of Ioffe's [4] derivation with respect to the efficiency and output power is necessary.

2.5.2. Min and Rowe's design theory [51- 53]

A comparison between the conventional design and a design incorporating contact resistances as proposed by Min and Rowe [52] is shown in Figures 2.17 (a) and (b).

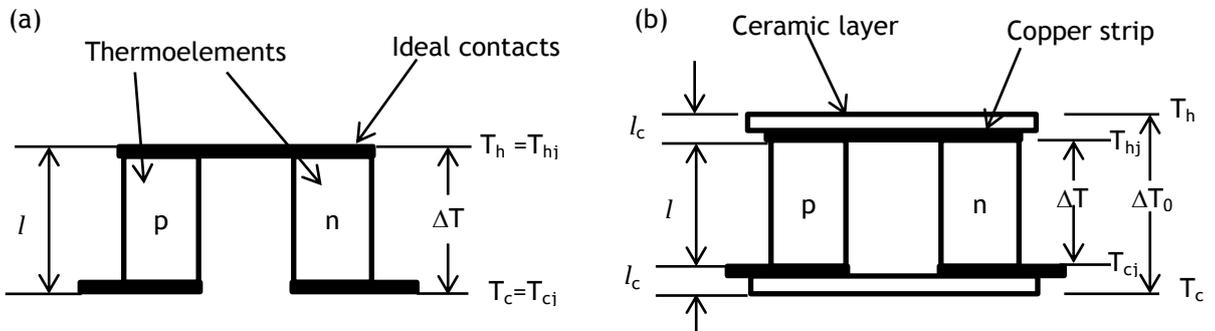


Figure 2.17: Schematic diagram of a conventional TEG: (a) assuming ideal contacts (b) with thermal and electrical contact resistances [52].

Calculation of output power for Figure 2.17 (a)

Figure 2.17 (a) represents a conventional TEG module having ideal contacts. According to the Seebeck phenomena, the total voltage output produced by the two legs is given by:

$$V = (\alpha_n + \alpha_p) \Delta T_0 \quad (2.61)$$

Assuming the thermoelectric properties are equal for both leg, i.e. $\alpha = \alpha_p = \alpha_n$, Equation (2.61) becomes:

$$V = 2\alpha \Delta T_0 \quad (2.62)$$

For impedance matched loads $R_L = r$, Equation (2.55) is modified as:

$$I = \frac{2\alpha \Delta T_0}{2r} \quad (2.63)$$

where $\Delta T_0 = T_h - T_c$. The power delivered by the TEG is then defined as:

$$P_{ideal} = I^2 R_L = \frac{(\alpha \Delta T_0)^2}{r} \quad (2.64)$$

Recall, $r = r_p + r_n$. Assuming both legs have equal length and area, and the electrical resistances are equal for both legs, then:

$$r = 2\rho \frac{l}{A} \quad (2.65)$$

Substituting Equation (2.65) into (2.64) and rearranging, the ideal power for the conventional design of Figure 2.12 (a) is obtained as [4, 53]:

$$P_{ideal} = \left(\frac{\alpha^2}{\rho}\right) \left(\frac{\Delta T_0^2}{2}\right) \left(\frac{A}{l}\right) \quad (2.66)$$

The expression in Equation (2.66) implies that the output power approaches infinity as the length of the thermoelements goes to zero. However, in practice, this limit is unrealistic due to the presence of contact resistances within the layers [48]. A more realistic model that takes into account the effect of thermal and electrical contact has been developed by Min and Rowe [51-53].

Calculation of output power for Figure 2.17 (b)

The thermal contact resistance is undesirable because it reduces the temperature difference across the device [52]. Based on Figure 2.17 (b), the actual temperature difference across the legs is ΔT , which is less than ΔT_0 . By considering the effects of the contact resistance between the ceramic layers and the legs, the expression for ΔT can be obtained as follows. Assuming there are no heat losses, the heat flux flowing through the contacts at the hot surface is equal to the heat flux through the legs so that:

$$\frac{2\kappa\Delta T}{l} = \frac{\kappa_c(\Delta T_0 - \Delta T)}{l_c} \quad (2.67)$$

After rearranging the following expression is arrived at [52]:

$$\Delta T = \frac{\Delta T_0}{1 + 2\left(\frac{\kappa}{\kappa_c}\right)\left(\frac{l_c}{l}\right)} \quad (2.68)$$

By taking into account the electrical contact resistances, the total resistance of the device is given as:

$$r = 2\rho\frac{l}{A_l} + 4\frac{\rho_c}{A_l} \quad (2.69)$$

where the total contact resistance is given as $r_c = 4\rho_c/A_l$ and a negligible interface contact length is assumed. Let $n = 2\rho_c/\rho$, then Equation (2.69) can be rewritten as [52]:

$$r = 2\rho\frac{l}{A_l}\left(1 + \frac{n}{l}\right) = \frac{2\rho}{A_l}(l + n) \quad (2.70)$$

By taking Equation (2.68) into consideration, the realistic voltage for N number of thermocouples of the TEG can be given as [52]:

$$V_r = N * \alpha\Delta T = N * \alpha \frac{\Delta T_0}{1 + 2\left(\frac{\kappa}{\kappa_c}\right)\left(\frac{l_c}{l}\right)} \quad (2.71)$$

Hence, the realistic power output can be obtained as [51]:

$$P_r = \frac{V_r^2}{r} = N * \alpha \frac{A_l * \Delta T_o}{(2\rho(l + n)) \left(1 + 2 \left(\frac{\kappa}{\kappa_c} \right) \left(\frac{l_c}{l} \right) \right)} \quad (2.72)$$

The implication of Equation (2.72) is that the contact resistance becomes more pronounced (i.e. cannot be neglected) when considering small dimensions and this will affect the power output of the device.

The experiment performed in this work deals with very small dimensions in micro-scale, thus the effect of contact resistance in the device cannot be neglected.

2.5.3. Wu's design theory [54]

A more straightforward theoretical analysis for obtaining the output power of real systems has been developed by Wu [54]. It is straightforward in the sense that knowledge of the thermal and electrical contact properties is not required for obtaining the maximum output power. This analysis was developed as a theoretical upper bound for real TEG systems since such systems cannot be evaluated based on the Carnot efficiency [54].

Wu's theory assumes a simple model, described in Section 2.5.1, in which the material properties are constant. It also assumes that the geometry is optimized and the internal and external load resistance are impedance matched for maximum output power. Based on Figure 2.17 (b), the absorbed heat energy:

$$Q_h = \alpha \cdot I \cdot T_{hj} + K \cdot (T_{hj} - T_{cj}) - \frac{1}{2} I^2 r \quad (2.73)$$

while the heat energy removed from the system is:

$$Q_c = \alpha \cdot I \cdot T_{cj} + K \cdot (T_{hj} - T_{cj}) + \frac{1}{2} I^2 r \quad (2.74)$$

Therefore, the output power is given as:

$$P = Q_h - Q_c = \alpha(T_{hj} - T_{cj})I - I^2 r \quad (2.75)$$

and the efficiency is calculated as:

$$\eta = \frac{P}{Q_h} \quad (2.76)$$

Based on Fourier's law of heat conduction the heat flow from the heat source at T_h to the junction of the legs at T_{hj} is calculated as:

$$Q_h = U_H A_H (T_h - T_{hj}) \quad (2.77)$$

and the removal of heat from the junction of the legs at T_{cj} to the heat sink at T_c is given as:

$$Q_c = U_c A_c (T_{cj} - T_c) \quad (2.78)$$

where U_H and U_c are overall heat transfer coefficients, which includes conduction, convection and radiation modes, of the hot and cold heat exchangers respectively. A_H and A_c are the respective surface area.

Combining Equations (2.73) and (2.77), T_{hj} is expressed as:

$$T_{hj} = \left(U_H A_H T_H - K. (T_{hj} - T_{cj}) + \frac{1}{2} I^2 r \right) / (\alpha I + U_H A_H) \quad (2.79)$$

Similarly, by combining Equations (2.74) and (2.78), T_{cj} is expressed as:

$$T_{cj} = \left(U_c A_c T_c + K. (T_{hj} - T_{cj}) + \frac{1}{2} I^2 r \right) / (U_c A_c - \alpha I) \quad (2.80)$$

The maximum power transfer occurs between open circuit (when $I = 0$, $P = 0$) and short circuit (when $V = 0$, $P = 0$) conditions. By taking the first partial derivative of Equation (2.75) with respect to the current I , and setting the derivative equal to zero, the maximum current I_m is obtained as:

$$I_m = \alpha \left((T_{hj})_m - (T_{cj})_m \right) / 2r \quad (2.81)$$

Substituting Equation (2.81) into Equations (2.79) and (2.80) the maximum junction temperatures are obtained thus:

$$(T_{hj})_m = (U_H A_H T_H - 2r I_m K / \alpha + 0.5 (I_m)^2 r) / (\alpha I_m + U_H A_H) \quad (2.82)$$

$$(T_{cj})_m = (U_c A_c T_c + 2r I_m K / \alpha + 0.5 (I_m)^2 r) / (U_c A_c - \alpha I_m) \quad (2.83)$$

Equations (2.81) – (2.83) are solved simultaneously to determine the current and junction temperatures that would produce the maximum output power [54].

Summary

The Equations for the output power derived by Ioffe [4], Min and Rowe [51], and Wu [54] are summarized as shown.

1. Ioffe [4]:

$$P = \left(\frac{\alpha^2}{\rho} \right) \left(\frac{\Delta T_0^2}{2} \right) \left(\frac{A}{l} \right)$$

2. Rowe and Min [51]:

$$P = N * \alpha \frac{A_l * \Delta T_o}{(2\rho(l + n)) \left(1 + 2 \left(\frac{\kappa}{\kappa_c} \right) \left(\frac{l_c}{l} \right) \right)}$$

3. Wu [54]:

$$P = \alpha \left((T_{hj})_m - (T_{cj})_m \right) I - I^2 r \quad \text{and} \quad I_m = \alpha \left((T_{hj})_m - (T_{cj})_m \right) / 2r$$

loffe's [4] power equation represents an ideal system while those of Rowe and Min [51] and Wu [54] represent a real system. loffe's [4] equation suggests that the external heat source and heat sink temperatures (i.e. $\Delta T_0 = T_h - T_c$) are the same as the junction temperatures (see Figure 2.12 a), but in reality this is not the case. The equation of Rowe and Min [51] is considered to be realistic because it takes into consideration the thermal contact resistances such that the heat exchanger temperatures are not the same as the junction temperatures (see Figure 2.12 b). Wu's equation [54] is also considered to be realistic because it deals directly with the junction temperatures, which is different from the heat exchanger temperatures.

During experiments the temperatures of the heat exchangers (i.e. $\Delta T_0 = T_h - T_c$) are easy to measure directly. This is not the case with the junction temperatures, which are difficult to measure directly, because the p- and n-legs are sandwiched between the heat source and the heat sink and difficult to access. However, the junction temperature temperatures can be estimated using Fourier's law of heat conduction once the heat exchanger temperatures are determined.

Rowe and Min's equation require accurate measurement of the resistivity of the individual legs. A major challenge in doing this is that the cross-plane resistivity for the materials that make up the superlattices are difficult to measure due to multiple quantum wells and barrier layers. Although Rowe and Min's equation is designed for a complete TEG module, it still requires a separate measurement of the contact resistance of the individual legs. Practically speaking, the measured resistance of the complete module includes all possible contact resistance that may arise due to the coupling of both legs. Therefore, Wu's equation [54] is a

more preferable option because it uses the overall resistance of the device rather than the resistance of the individual legs.

All three power equations are derived based on the simple model which assumes temperature-independent thermoelectric properties. Hence, the shortcomings that affect simple models as earlier discussed in Section 2.4.1 also affect these power equations.

The energy balance models described in Section 2.4.2 can be used to model the efficiency and output power of a thermoelectric generator. Such models are mostly implemented in Finite Element software packages such as ANSYS™ [47] and COMSOL Multiphysics® [49, 50]. These software packages are able to couple the governing equations for the electrical and thermal effects, and produce convergent solutions to nonlinear systems [50]. COMSOL Multiphysics® software package, in particular, has a user-friendly interface that allow for 1D, 2D or 3D device modelling of various types of TEG geometrical configuration. Parameters that are critical to the module performance, such as leg length, thickness of the heat exchangers, surface area and contact resistances can be explored easily [50] in COMSOL. In the next section, a review of COMSOL Multiphysics® in comparison to other numerical approaches is discussed.

2.6. Review on COMSOL Multiphysics® FE software

COMSOL Multiphysics® is a finite element solver used for simulating various physics and engineering applications. It is useful for solving engineering related problems easily and quickly [81]. For example, it is capable of solving coupled phenomena and multiphysics problems, which would have been otherwise difficult and time consuming to solve manually. The output results are usually presented in a colourful graphical form, which can be used to make impressive presentations. It also offers an extensive interface to MATLAB and its tool boxes. This allows for a large variety of programming, preprocessing and post processing possibilities. The software can be used on the platforms of Windows, Mac and Linux. It provides a conventional physics-based user interfaces and allows for entering coupled systems of partial differential equations (PDEs) [95, 96]. The versatility of the FE solver lies in its ability to model arbitrary shaped structures, work with complex materials, and apply various types of loading and

boundary conditions. The method can easily be adapted to different sets of constitutive equations, which makes it particularly attractive for coupled-physics simulation [47].

2.6.1. Relative strengths and weaknesses of COMSOL Multiphysics® Finite Element

Strengths

In this research work, COMSOL Multiphysics® was used to validate published experimental heat transfer measurements [6, 7] which are susceptible to heat losses. It allowed for the implementation of thermoelectricity which is the coupled interaction between charge and heat. More importantly, it allowed for the easy exploration of geometric configurations with three-dimensional (3D) FEMs, thus creating a platform for the improvement of thermoelectric module design.

Therefore, due to the complexity of the nano-structure investigated in this work and for the purpose of detailed analyses conducted on the nano-structure (see Chapters 3 - 6), the FE method in COMSOL Multiphysics® was used in this research.

Weakness:

Like all other FE methods, COMSOL Multiphysics® produces approximated results. Hence, there is the need to implement analytical methods that will complement the FEM. The analytical method will provide accurate bounds that can be used to verify results of FE simulation. In this research work, Wu's analytical method was used to verify the FEM in COMSOL Multiphysics®.

Another limitation is that sophisticated FE packages such as COMSOL Multiphysics® give room for misinformation, especially if the features of software are not properly understood. Proper training on how to use the FE package as well as good knowledge of the physics being applied are necessary. The implication is that expert knowledge is required to use FE packages and this requires training that is time-consuming. In contrast, analytical techniques can be easily understood and applied in a relatively short time.

Next is the review of previous works on thermoelectric analyses which have been implemented in COMSOL Multiphysics®

2.6.2. Review of Sandoz-Rosado and Steven's [50]

In the work of Sandoz-Rosado and Steven [50], a 3D modelling technique is used to design a uni-couple module configuration (i.e. TEG module having a single p- and n-leg). The parameters critical to the performance of the uni-couple include the geometry of the p- and n-leg, the solder thickness required for bonding the legs, the ceramic interface via which the device is heated up, the leg spacing and electrical contact thickness.

The study showed that increasing the spacing between the p- and n-legs results in a proportional increase in the electrical contact length and overall internal resistance and hence, a decrease in the peak power. Also, by increasing the spacing between the legs, the surface area increases and results in a reduction of the power density, P_D (power density is defined as power output per unit area i.e. P_D/A)

Furthermore, a negligible change in efficiency was observed for different leg spacings. Basically, this implies that having smaller leg spacing is preferable for improved output power. This conclusion is in agreement with the findings from previous survey [2] of TEGs, which revealed that reduction of the leg spacing (or inter-thermoelement spacing) could improve the power density.

Sandoz-Rosado and Steven [50] claim that the inclusion of the solder joints in their FEM improves the output power due to the following reason: the surface area through which the heat is conducted is larger and more heat will conduct down the legs. The result is a higher effective temperature difference across the legs. However, the authors [50] did not consider that the lack of smoothness of the solder joints influences the thermal and electrical contact resistances come and these factors may reduce the generated output power. Finally, they compared the simulation results of their 3D FEM with corresponding results obtained from 1D analytical models. The discrepancy between the two results was attributed to the solder joint included in the 3D simulation but difficult to include in the analytical method.

2.6.3. Review of Ebling et al [49]

The FEM study by Ebling et al [49] also shows a similar trend as observed in Section 2.6.1. In this work [49], FEM simulations and experiment investigations were used to show that the geometrical design of the legs, the electrical contacts and soldering process affects the efficiency and output power of a TEG. The modules were made using Bismuth Telluride material. A decrease in ZT by a factor of about 4 was observed for the module arrangement when compared to the ZT of the individual materials. This decrease was attributed to the high contact resistances. The results of Ebling et al [49] demonstrate a close match between experiment and simulation for open circuit connection, while the corresponding results for close circuit connection differ significantly. The discrepancy in the close circuit result was again attributed to the high contact resistance and other unknown mechanism of losses within the module. In both studies, i.e. [49] and [50], FEMs were validated using other independent approaches; analytical for reference [50] and experimental for reference [49].

The present research makes use of a combination of FEM developed in COMSOL Multiphysics® and Wu's analytical approach [54] to model and analyze the design of a TEG module. Furthermore, experimental investigations have been performed to validate the FEM results. Relevant concepts employed in this work for the enhancement of the power density include; increasing the leg height as this will help increase the temperature difference across the legs and hence the Seebeck voltage, having a low internal resistance of the material is important to ensure a high power output and consequently a high power density. Another relevant concept is the reduction of the contact resistance. By reducing the contact resistance, the thermal resistance (and hence thermal losses) in the device will reduce. This will help to improve the temperature difference across the legs and hence the corresponding Seebeck voltage. Eventually, there will be improvement in the power output and power density.

Details of the modelling and design of the TEG module are presented in Chapters 4 and 5 of this thesis.

Chapter summary

In this chapter, a brief historical account of discovery and application of thermoelectricity in electrical power generation was discussed. The progresses made in the development of thermoelectric materials and the fundamental physics behind thermoelectricity were discussed. The microfabrication techniques of some TE materials and TE module design employed by some literatures [30, 31, 33] and [35 - 39] were also reviewed. It was explained that the microfabrication technique of the TE material, to a large extent, has an impact on the type of method employed in the design of the TE module. For example, the module design concept for TE material having a single thin film thermoelectric layer will differ from TE materials having superlattices as the thermoelectric layer. A comparison of various microfabrication techniques and the performances of the micro fabricated devices were conducted.

Finally, the various modelling techniques and design theories were reviewed with the aim of choosing an appropriate approach for pre-fabrication analysis. The modelling techniques fall under averaging schemes models and local energy balance equations models. The advantage of simple models is that the models provide quick information about the performance of the device being studied. The disadvantage however, is that the averaging scheme models may not give enough information about the performance of the device being studied. The models derived from the energy balance equations are more realistic and give more accurate information about the performance of the device. As a result of the complexity of these models, Finite Element softwares such as ANSYS™ [47] and COMSOL Multiphysics® [49, 50] are employed to facilitate the solution of such models.

Design theories have been proposed for evaluating the performance of TEGs; some of which include theories proposed by Ioffe [4], Min and Rowe [51] and Wu [54]. It was shown that Min and Rowe [51], and Wu's [54] theories are more realistic than that of Ioffe [4]. This is because the former takes into consideration the effect of contact resistances which significantly affect the performance of TEGs at the micro and nano-scale level. The latter only assumes ideal conditions whereby contact resistances are negligible at the macro scale level.

Based on the reviews discussed in this chapter, this thesis is patterned in similar fashion, whereby the thermoelectric material investigated is discussed. Subsequently the microfabrication of the TEG module using the investigated material and the modelling techniques adopted for pre fabrication analysis are discussed in detail.

3. Material: Ge/SiGe superlattice

The material used in this research work is a novel nano-fabricated 2D Ge/SiGe superlattice. The material was developed as part of the GreenSi project with the intention of using this material to build micro fabricated TEGs that can power a commercial sensor having a power rating of 3mW [18]. The partners that were involved in this project were: the Politecnico di Milano, the Johannes Kepler University of Linz, ETH Zurich and University of Glasgow. The modelling and band structure analysis was performed by Prof. Douglas Paul, the head of the project at Glasgow University. The material was grown at Politecnico di Milano at L-Ness of Como. The X-ray Diffraction (XRD) and Transmission Electron Microscopy (TEM) analysis were performed by the Johannes Kepler University of Linz and ETH Zurich, respectively. Finally the thermoelectric characterization of every material was performed at Glasgow University

The Ge/SiGe superlattice is an alternating layer of Ge and SiGe alloy stacked periodically in the z-direction as shown in Figures 3.1 (a) and (b). Ge represents the 2D quantum well while $\text{Si}_{1-x}\text{Ge}_x$ alloy forms the barriers required to reduce the lattice thermal conductivity of the material. The alternate combination of the Ge quantum wells and $\text{Si}_{1-x}\text{Ge}_x$ barrier forms the superlattice structure. In general, the significance of a superlattice structure is that the electronic potential difference at the interfaces and the resulting phonon scattering and band structure modifications can be exploited to improve the thermoelectric properties by means of reduced phonon thermal conduction and enhancement of electron transport [32]. Various superlattice designs of Si-Ge alloys (such as Ge/SiGe and Si/SiGe superlattices) and band structure modifications have been investigated [6, 7 and 18]. The findings of these investigations showed that the thermal and electrical conductivity are higher in the lateral direction than in the vertical. Also, the Seebeck coefficient has a higher value in the vertical direction than in the lateral direction, and this confirms the anisotropic nature of the material.

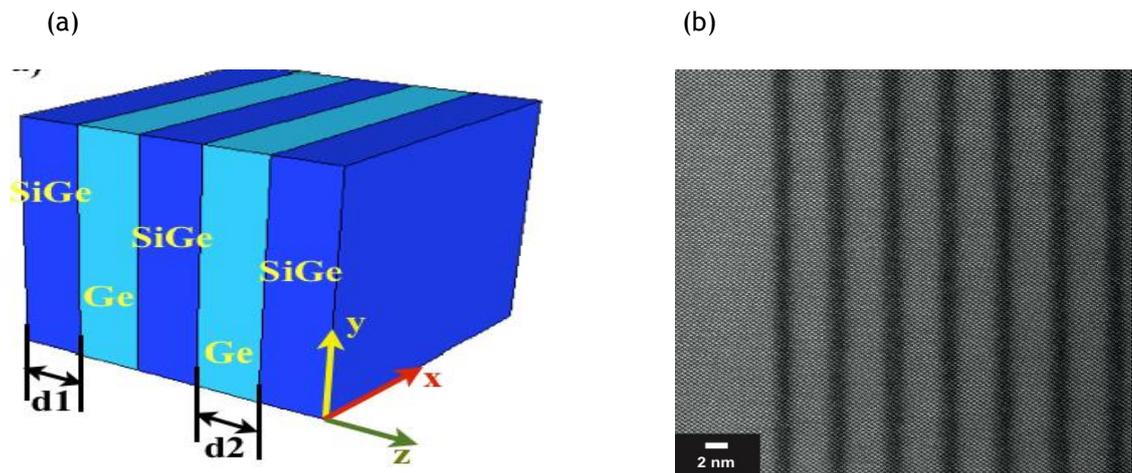


Figure 3.1: (a) Schematic diagram (b) TEM image of Ge/SiGe superlattice [18]

The technique applied in the growth of the Ge/SiGe material used in the present research is the LEPECVD. The main advantage of this technique is that it has a wide range of epitaxial growth rate, i.e. from $< 1 \text{ \AA/s}$ - 10 nm/s , at comparatively lower substrate temperature ($500 - 750^\circ\text{C}$) compared to the aforementioned growth techniques stated in Section 2.2.3 [56, 57]. Most importantly, this technique allows the fabrication of high-quality relaxed SiGe buffer layers that can minimize thread dislocation due to strain. Thread dislocation refers to the existence of defects and dislocations that may occur during the elastic accommodation of cells with different lattice constant (see Figure 3.2 below). This can result to degradation of the electrical, optical and thermal properties of the devices.

3.1. Development of Ge/SiGe- based material

The Ge/SiGe superlattice heterostructure [18] is developed (or grown) on top of a silicon substrate by an oriented growth technique called Epitaxy. The main factors that affect the quality of the materials grown are chemical instabilities and lattice mismatch of the different materials. The Ge/SiGe material growth is made possible because silicon and germanium are both group IV elements in the periodic table. Although, the silicon cell has a lattice constant which differs by 4% from Ge, these cells can contain each other by means of elastic accommodation (i.e. accommodation by strain) [18]. Figure 3.2 is an example of elastic accommodation of materials with different lattice constants a_1 and a_2 . As a result of the strain, the permissible thickness of the superlattice is limited to a few micrometers ($< 10 \text{ }\mu\text{m}$).

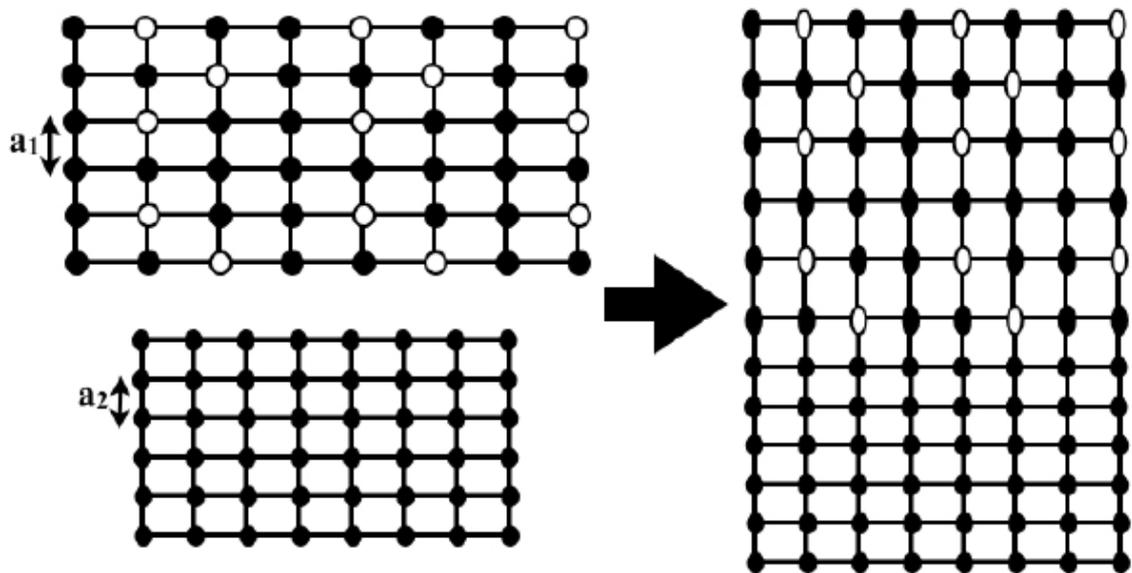


Figure 3.2: Elastic accommodation of cells with different lattice constant ($a_1 > a_2$) [18, 58]

3.1.1. Material design and growth technique

Epitaxial growth

The epitaxial growth techniques are categorized into two broad methods, namely: physical vapour deposition and chemical vapour deposition methods.

Physical vapour deposition

The physical vapour deposition technique, also known as Molecular Beam Epitaxy (MBE), is a technique that grows the material by effusion cells under ultra-high vacuum conditions. The effusion cell is an MBE component that is designed for evaporation or sublimation of a variety of elements and compounds such as Al, Ga or In. MBE is mostly known for its excellent control over the layer thickness, chemical composition and doping concentration [18, 59]. The major disadvantage of this technique is that there might be formation of particles which can cause defects in the grown film [59].

Chemical vapour deposition (CVD)

The CVD approach grows the epitaxial layer through chemical reaction of various gases. It overcomes the limitations of MBE and at the same time retains an excellent control of the dopant and compositional profiles. This makes it suitable for high quality strained layers. Examples of this approach include Low-Pressure Chemical Vapour Deposition (LPCVD) and Low Energy Plasma Enhanced CVD (LEPECVD).

LPCVD differs from LEPECVD in the sense that the LPCVD operates at high temperatures above 600°C and permits the processing of large wafer batch sizes. The main advantages of LPCVD are the excellent uniformity of thickness and purity, high reliability, homogeneity of deposited layers and reproducibility. The disadvantages however include lower deposition rates and higher temperatures required for the process limits the type of material that can be used. However, the high temperature does allow for greater uniformity with lesser defects.

LEPECVD on the other hand requires addition of plasma in the deposition chamber with reactive gases to create the desired solid surface on the substrate. Advantages of LEPECVD include faster operation, low temperature that does not limit the type of material used, higher film density for higher dielectric and more compression, and ease of cleaning the chamber. Disadvantages include the expense of the equipment and the stress of plasma bombardment [60].

Finally, LEPECVD can only deposit the film on one side of 1-4 wafers while LPCVD can deposit films on both sides of at least 25 wafers. Whichever method that is employed, it is important that the lattice constant of the epitaxial layer is close to that of the substrate wafer in order to avoid dislocation due to strain. The p-type and n-type Ge/SiGe material samples are grown on 100 mm diameter p-type (001 crystal orientation) Silicon wafer of 5 – 10 $\Omega\text{-cm}$ using the LEPECVD technique. Figure 3.3 is a schematic diagram of an LEPECVD reactor.

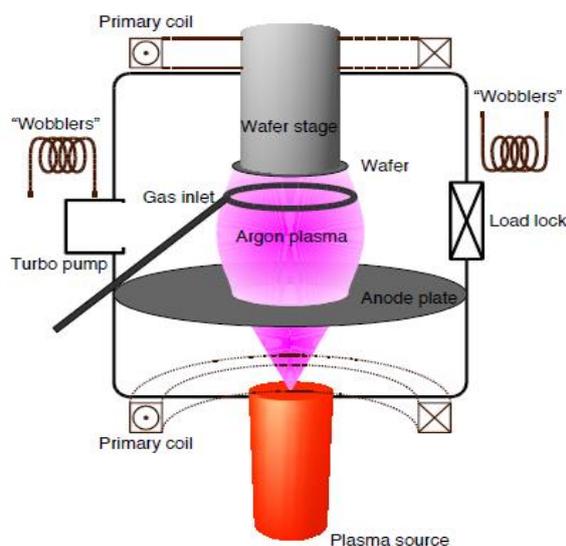


Figure 3.3: Schematic diagram of an LEPECVD reactor [18, 61]

Gases are transported through the gas inlet into a vacuum chamber where Argon plasma energy is created to break the gaseous molecules necessary for growing the epitaxial layer. The gases used for growing the Ge and SiGe alloy (i.e. Ge/SiGe) are SiH_4 and GeH_4 . The Ge/SiGe is then doped to n-type using the gas PH_3 while the doping of the alloy to p-type is B_2H_6 .

An inter-medium ($<13 \mu\text{m}$ thick) $\text{Si}_y\text{Ge}_{1-y}$ grade buffer layer (i.e. Si with Ge end concentrations between 10 and 100%) is first grown on the p-Si (001) wafer at a rate of 5 - 10 nm/s. This layer is required to relax the structure so as to accommodate the lattice mismatch between Ge and Si and hence, control the threading dislocation due to strain [3, 9]. On top of the buffer is grown a 500 nm highly doped contact layer, which will serve as the connecting electrode. Thereafter, the superlattices are grown at a rate of 1.0 - 1.5 nm/s for both p- and n-designs. The growth rates are chosen to allow control of the layer content, the thicknesses and the doping levels. In order to grow a total superlattice thickness of $4 \mu\text{m}$, 922 repeats are required for the p-type design while 889 repeats are required for the n-type design. Both superlattices are uniformly doped to a doping density of about $2.0 \times 10^{18} \text{ cm}^{-2}$. A final top contact layer of 60 nm (highly doped) is grown on top of both superlattices, to allow the fabrication of Ohmic contacts. Figure 3.4 (a) shows a schematic diagram of the p-type design and Figure 3.4 (b) shows a transmission electron microscopy (TEM) image of a grown Ge/SiGe superlattice structure [3, 9].

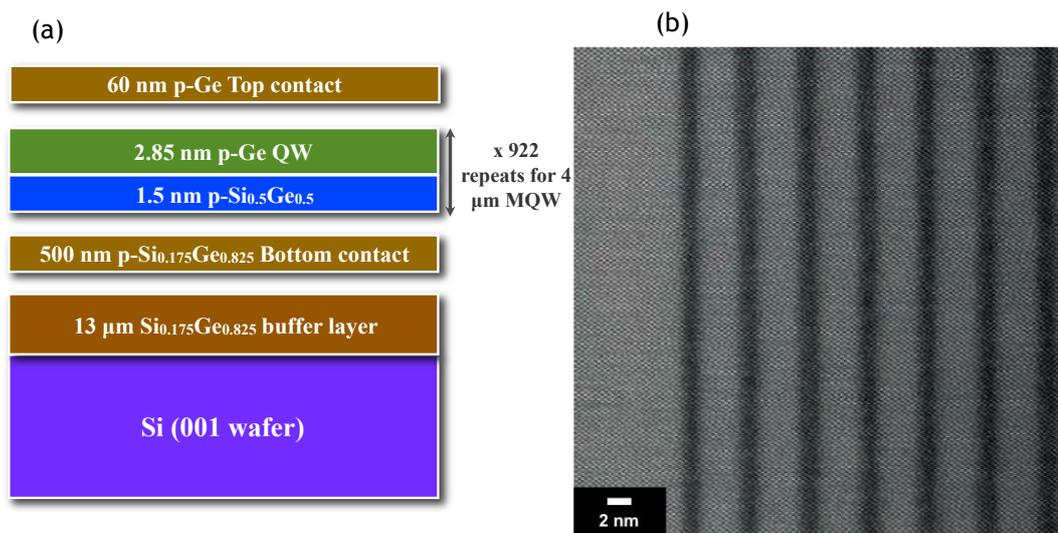


Figure 3.4: Schematic diagram of (a) p-type design and (b) TEM image of the Ge/SiGe superlattice structure [3, 6].

Several designs of Ge/SiGe superlattice with varying quantum well, barrier thicknesses and doping densities have been grown using the LEPECVD technique [9]. Consequently, the thermoelectric properties of the variety of Ge/SiGe superlattice materials are expected to differ from one to the other. Hence, there is need to characterize the Ge/SiGe superlattice material to evaluate its properties.

3.2. Material characterization techniques.

Material characterization of the Ge/SiGe superlattice involves determination of the thermoelectric properties, i.e. κ , α and σ , required to evaluate the figure of merit. The materials grown are anisotropic in nature because of the superlattice structure. This means that the thermoelectric properties in the in-plane direction differ from those in the cross-plane direction. In-plane direction implies that the electrical and thermal transports are along (or parallel to) the quantum wells (QWs) while cross-plane direction means that the transports are perpendicular to the quantum wells.

Previous work has investigated the thermoelectric properties of Ge/SiGe in the in-plane and cross-plane directions [62]; it shows that the estimated value of the in-plane electrical conductivity is higher than the estimated value of the cross-plane electrical conductivity. This is because the in-plane electrical resistance is much lower than that of the cross-plane which has more barrier layers. However, in another study [6], it has been shown that a combination of higher Seebeck coefficient and lower thermal conductivity is obtainable in the cross-plane direction compared to the in-plane direction. The overall ZT in the cross-plane direction is therefore higher than that in the in-plane direction.

Evaluating the cross plane thermal conductivity, κ accurately, has been found to be difficult in comparison to the other two properties i.e. Seebeck coefficient, α and electrical conductivity, σ . This is because thermal conductivity measurements are usually performed by determining the temperature gradient produced across a solid when a steady flow of heat is applied in one direction e.g. z-direction. A major challenge with thermal measurements is that there might be heat losses due to radiation, convection and/or conduction. Hence, not

all the heat energy flows into the device whose thermal conductivity is measured [63]. If the heat losses are negligible then the measured thermal conductivity is acceptable. Heat losses by radiation and convection can be neglected for the experiments conducted in this study, as shown below. Calculations for heat losses by radiation, convection and conduction are considered as follows:

Heat loss by radiation:

The amount of heat lost or generated by radiation, Q_{rad} is defined by:

$$Q_{rad} = \sigma \varepsilon (T_{ext}^4 - T^4) * A \quad (3.1)$$

where Stefan-Boltzmann constant, $\sigma = 5.67 * 10^{-8} \text{ W/m}^2/\text{K}^4$; ε ranges between 0 – 1; area, $A = 0.224 \times 10^{-4} \text{ m}^2$ (i.e. the area is obtained from the experimental device in section 6.33) and assuming T_{ext} is maintained at room temperature of 25 K and $T = 0 \text{ K}$.

Therefore, heat lost by radiation is $4.96 \times 10^{-7} \text{ W}$. This amount of heat lost is negligible compared to the amount of heat (ranging between 0.1 - 0.02 W) inputted into the TEG by the heat source.

Heat loss by convection:

Heat lost by convection is defined by:

$$Q_{conv} = h (T_{ext} - T) * A \quad (3.2)$$

where $h = 5 \text{ W}/(\text{m}^2\text{K})$ for natural convection. Thus, heat lost by convection is estimated as 0.0028 W. Heat lost by convection can be much smaller than the estimated value of 0.0028 when the temperature difference ($T_{ext} - T$) is very small as was observed in the experiments conducted in this study. This means that heat lost by convection can be neglected when compared to the input heat ranging between (0.02 - 0.1 W). Also, convective heat transfer was accounted for in the FEM for determining the thermal conductivity and the FE simulations showed that the effect of convective heat losses is negligible.

Heat loss by conduction:

The heat lost by conduction is calculated using Fourier's law of heat conduction as defined by Equation (2.12) above. This is the most prominent heat loss

mechanism that cannot be ignored and the amount of heat lost is dependent on the contact area of the device that is in contact with the TEG.

A common measurement technique that is used in the literature to overcome the challenge of conductive heat losses is the 3ω method [63].

3.2.1. 3ω method

The 3ω method involves the fabrication of metal lines with four contacts on the sample whose thermal conductivity is to be measured. These metal lines act both as heaters and thermometers [63] as shown in Figure 3.5. A sinusoidal current at angular frequency of ω is passed through one end of the metal contacts and heats up the surface of the sample. Consequently, the temperature fluctuates at a frequency of 2ω . Due to the temperature-resistance relationship of the metal contacts the electrical resistance will also oscillate at a frequency of 2ω . Thus, the small voltage drop across the metal line is 3ω . This voltage is used to measure the temperature oscillations and hence the thermal response of the superlattice [63 -66]. The 3ω component of the voltage is then measured by a lock-in-amplifier instrument [63].

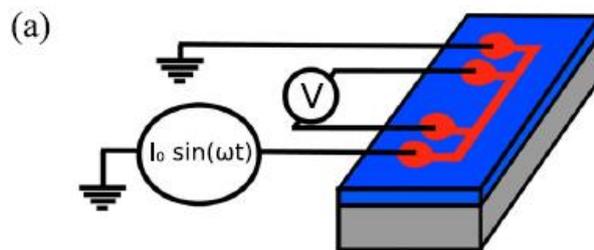


Figure 3.5: 3ω method for measuring the cross-plane thermal conductivity [64]

A challenge with this technique is that not all lock-in-amplifiers have a built-in 3ω detection unit [65]. Hence, an external unit may be required, which may not be expensive. Also, when working with superlattices that are anisotropic in nature the 3ω method becomes complicated as it requires some computational effort to evaluate the cross-plane κ . Moreover, the 3ω method will give a response from all the layers buried underneath the thermometers and heaters rather than only the superlattice, which is the layer of interest. Therefore, the 3ω method is not suitable for measuring the κ property of the Ge/SiGe material used in this work.

3.2.2. Heated test structure

A unique measurement technique [6] has been developed to measure simultaneously, the cross-plane thermal conductivity and Seebeck coefficient of the Ge/SiGe material investigated in the present research. The experimental technique was designed to simultaneously produce and measure the differential temperature and voltage output in the cross-plane direction, and the measured results are used to estimate κ and α . This technique involves creating a 4 μm etched mesa which forms the total thickness of the Ge/SiGe superlattice. Thereafter, metallic structures that can serve as Ohmic contacts, thermometers and heaters are micro-fabricated on top and below the etched mesa. Figure 3.6 (a) presents the fabricated structures on a Ge/SiGe sample while Figure 3.6 (b) shows a schematic diagram of the different layers of the fabricated structure.

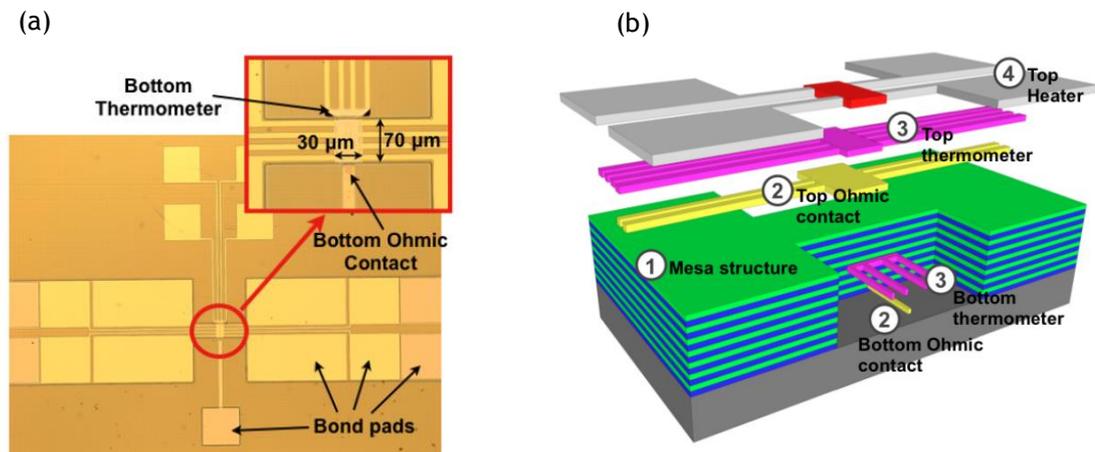


Figure 3.6: (a) Optical microscope images of the micro-fabricated structure (b) Schematic diagram of the different layers of the structure used for measurement of cross-plane properties [18].

The Ohmic contacts are necessary for measuring the differential voltages between the top and bottom of the mesa. The thermometers, which are made of Ti/Pd, are used to measure the differential temperatures at the top and bottom of the device. A Si_3N_4 insulator is used to passivate the centre of the thermometers to isolate it from the NiCr heater. The aim of this isolation is to allow the sample to be heated up by the NiCr heater without allowing any form of electrical contribution from an external power source. The thickness of the structure was designed to be within a few nanometers so that heat losses in the lateral direction are minimized.

Table 3.1 presents the estimated values of κ and α obtained from measurements of some Ge/SiGe materials with varying quantum well sizes and doping densities (N_A). All the listed parameters are obtained from reference [6].

Table 3.1: κ and α measurements of p-type Ge/SiGe superlattices with varying quantum well sizes and doping densities, N_A [6].

Material	N_A (cm ⁻³)	α (μ V/K)	κ (W/mK)
SL1: 3.03 nm QW	1.9×10^{17}	533 ± 25	6.0 ± 0.4
SL2: 2.57 nm QW	9.7×10^{17}	393 ± 7	4.5 ± 0.4
SL3: 3.43 nm QW	2.0×10^{18}	394 ± 6	5.1 ± 0.4
SL4: 2.48 nm QW	1.2×10^{18}	113 ± 7	5.6 ± 0.3
SL5: 1.18 nm QW	2.0×10^{18}	91.8 ± 2.8	5.1 ± 0.1

Despite the uniqueness of the above technique there is still the need to address the challenge that comes with thermal measurement of heat flow in the perpendicular direction, resulting in heat losses [63]. Moreover, any physical connection to the thermometers or heaters produces undesirable heat paths which can affect the measurements [6]. This can result to significant error in the estimation of the thermal conductivity. Hence, the first major task of the present research was to evaluate the measurement technique for determining the cross-plane κ and α of a micro-fabricated Ge/SiGe heterostructure using Finite Element Modelling (FEM). A detailed discussion on how the FEM is used to evaluate the measurement technique is discussed next.

3.3. Finite Element Modelling to Evaluate the Cross-plane κ and α Properties of Ge/SiGe Heterostructure

The quality of thermoelectric materials is usually evaluated based on the conversion efficiency and generated output power. The efficiency is defined by the ZT and the generated output power is defined by the power factor, and these are determined by Equations 3.1 and 3.2 respectively [4].

$$ZT = \frac{\alpha^2 \sigma}{\kappa} T \quad (3.3)$$

$$\text{Powerfactor} = \alpha^2 \sigma \quad (3.4)$$

Equations (3.3) and (3.4), show that the figure of merit, ZT and power factor depend on α , κ and σ . Therefore, there is need to determine these properties for the Ge/SiGe superlattice. Experiments have been conducted to determine the cross-plane values of α and κ for the micro-fabricated Ge/SiGe heterostructure [6, 7]. However, there has been no independent verification of the experimental measurements prior to this research. Validation of the experimental measurements is considered to be important because of the difficulties

encountered in thermal measurement [63] as explained in the previous section. Hence, this section demonstrates the use of FEM to validate the cross-plane thermal conductivity and Seebeck coefficient estimated from experimental measurements.

The third property, which is the electrical conductivity, is not discussed in this work. However the experimental measurement techniques for this property can be found in the literature [6]. Thus, the focus of the FEM is on the evaluation of the cross plane thermal conductivity and Seebeck coefficient measurements techniques. The dependency of the Seebeck coefficient on the thermal conductivity property of the material will be described later on in this chapter.

3.3.1. Geometry and Material Specification

The fabricated microstructure device used for experimental measurement of the properties of the Ge/SiGe material is shown in Figure 3.7(a). The FEM for the fabricated device is represented in Figure 3.7(b). The FEM was developed in Comsol Multiphysics® with all the layers specified as shown in Figure 3.7(c). The material properties and geometrical dimensions are given in Table 3.2. All input values specified in Table 3.2 are the same as those used in the experiments [6, 7] to which the FEM results are compared. Note that the κ values for the superlattice heterostructure are not included in Table 3.2 because they are determined from the FEM.

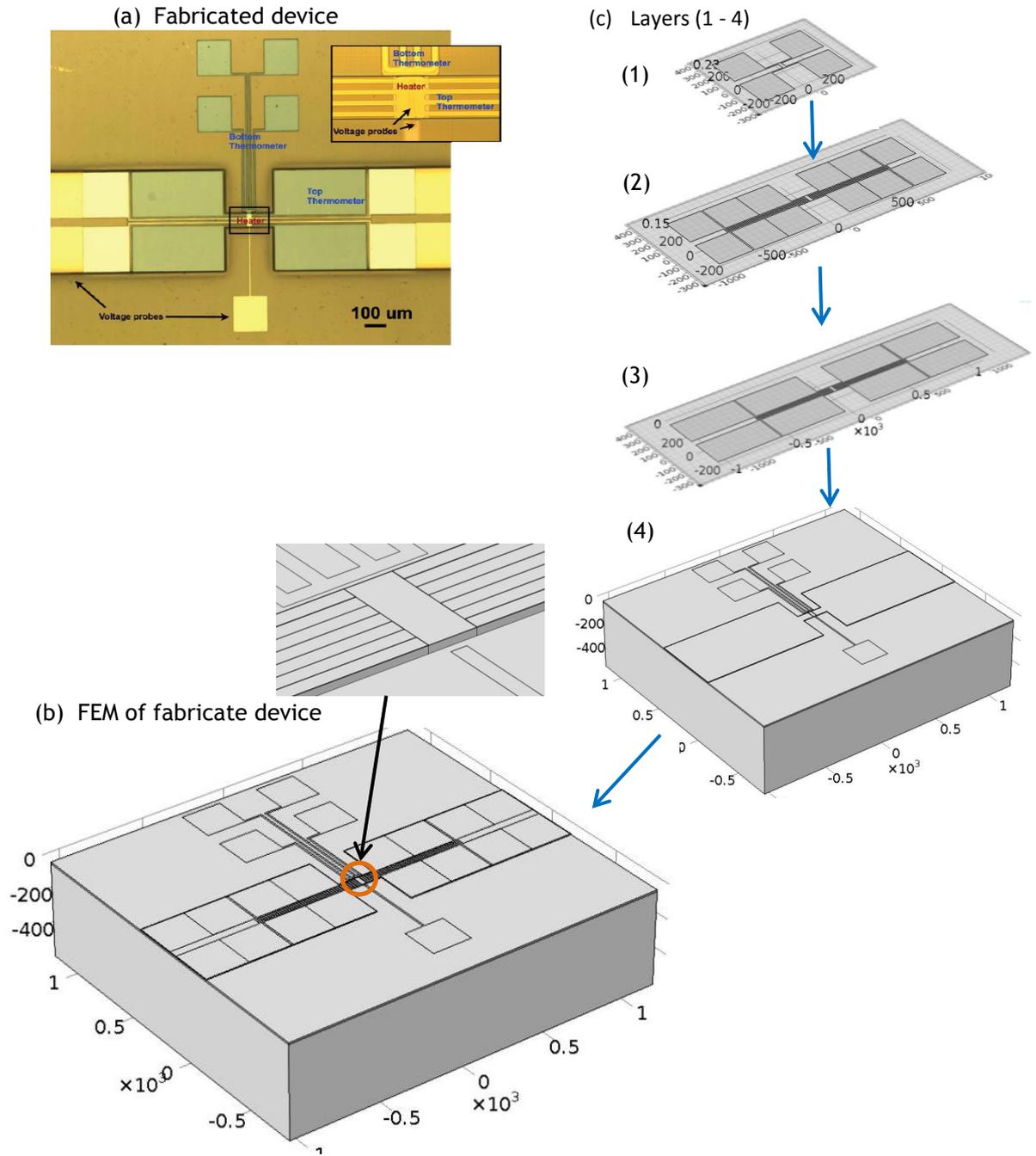


Figure 3.7: (a) Optical top – view full image of the fabricated device [6,7] (b) 3 – D FEM of the fabricated device (c) layers of fabricated device representing (1) NiCr heaters (2) Ti/pd thermometers (3) Ohmic contacts (4) Etched mesa of the superlattice with bottom contact and thermometer.

Table 3.2: Material properties and layer dimensions of the micro fabricated device.

ID	Constituent materials	κ [W/(mK)]	Thickness(nm)
Heater	NiCr	11 [67]	33
Thermometer	Ti/Pd	71.8 [67]	80
Ohmic Contact	AgSb/Pt	429 [67]	150
Superlattice_Exp1	Ge/Si _{0.5} Ge _{0.5}		4000
Superlattice_Exp2	Ge/Si _{0.5} Ge _{0.5}		3000
Buffer layer	Si _{0.175} Ge _{0.825}	20 [68]	10000
substrate	Si	150 [67]	530000
Insulator	Si ₃ N ₄	20 [67]	70
Capping	Au	317 [67]	100

The resulting superlattice thermal conductivity value also accounts for the effect of interfacial contact resistances. This is because the estimation of the thermal conductivity was based on experimental temperature measurements that are been affected by contact resistances. The κ -values are not expected to change with layer thickness because at the nanoscale level the effect of thermal contact resistance and interfacial roughness becomes more pronounced compared to layer thickness. Therefore, these effects are taken into consideration when calculating the thermal conductivity rather than layer thickness. Moreover, studies [69, 70] have shown that interfacial roughness is responsible for the reduction observed in the measured thermal conductivity at the nanoscale level. Thus, thermal conductivity of thinner film is not necessarily lower than that of the bulkier counterpart and this shows that the κ -values listed in Table 3.2 are reliable.

3.3.2. Measurement set-up and modelling

In the measurement setup, the bottom of the sample was placed on a copper block, acting as heat sink at room temperature. The heat source for the hot side was supplied using electrical power that was varied from 0.02 – 0.1 W and passed through the NiCr heater on the top of the sample. As a result, Joule heat is generated and conducted through the material due to the temperature gradient. A Ti/Pd thermometer was fabricated and calibrated [6] and used to measure the temperature difference across the superlattice for each input power. The applied electrical power and the respective temperature differences measured across the superlattice were used to estimate the thermal

conductivity κ of the material by applying Fourier's law of heat conduction (see Equation (3.5)).

$$Q = \kappa \frac{A}{L} \Delta T \quad (3.5)$$

Simultaneously, the temperature gradients measured across the superlattice produces corresponding differential voltages, V . These voltages were measured in open circuit via the Ohmic contacts at the top and bottom of the superlattice. The Seebeck coefficient α is then estimated using Equation (3.6).

$$\Delta V = a \Delta T \quad (3.6)$$

Joule heating model

The investigation of the material characterisation of the Ge/SiGe superlattice, was carried out using an FEM that incorporates both the heat flow and continuity of the electric charge equations. This was achieved using the Joule heating model (see Equations (3.7) and (3.8)) as the governing equation to describe thermal and electrical processes in the FEM for the superlattice. The Joule heating model can be expanded to account for the coupled thermoelectric effects in the heterostructure. This approach can be used to determine both the thermal conductivity and the Seebeck coefficient simultaneously. Derivation of the expanded-Joule heating model has been discussed in Section 2.4.2 of Chapter 2.

The expanded-Joule heating model incorporates both Peltier and Seebeck effect. It accounts for the electrical processes that produce the voltage output from the temperature gradient across the superlattice. The equations for the expanded-Joule heating model used in the FEM are [47]:

$$\nabla \cdot (\pi J + \kappa \nabla T) = \nabla \cdot q \quad (3.7)$$

and

$$\nabla \cdot \sigma (\nabla V + \alpha \cdot \nabla T) = \nabla \cdot J \quad (3.8)$$

Since the experiments were performed in open circuit,

$$\nabla \cdot J = 0 \quad (3.9)$$

Therefore, Equation (3.8) becomes

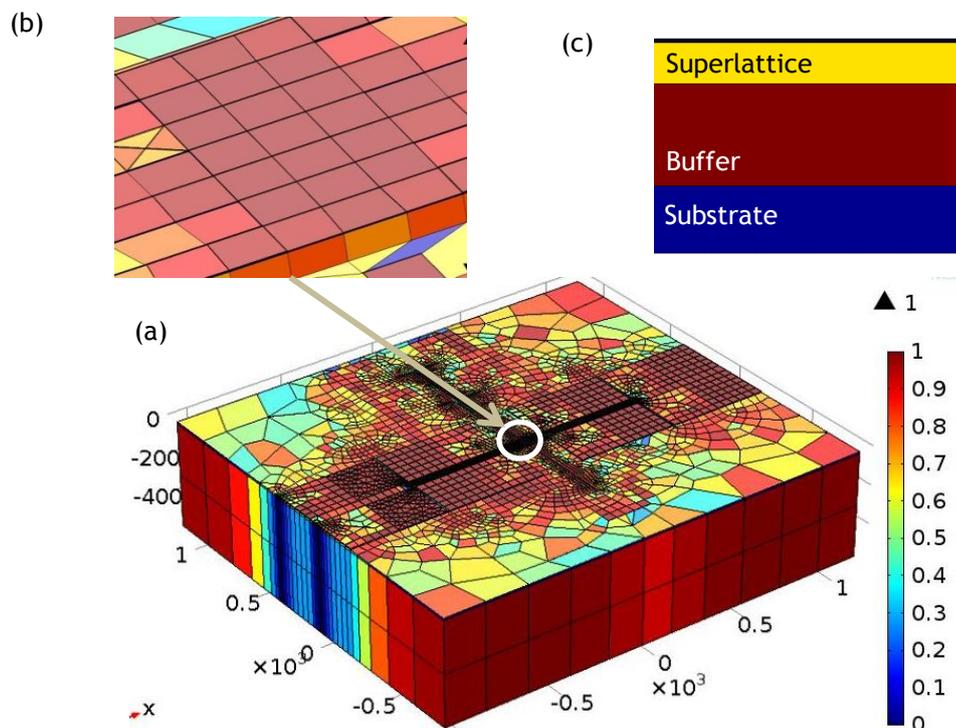
$$\nabla V = -\alpha \cdot \nabla T \quad (3.10)$$

where α is equal to α_n or α_p depending on the type of material used.

Although the FEM based on expanded-Joule heating model requires much longer computational time compared to the conductive heat transfer FEM, it has the advantage that it can be used to determine the temperature and voltage distribution in the heterostructure, whereas the conductive heat transfer FEM cannot be used to determine the voltage distribution. The Joule heating model is expanded to account for the coupled thermoelectric effects in the heterostructure. This approach can be used to determine both the thermal conductivity and the Seebeck coefficient simultaneously.

3.3.3. Meshing

The FEMs for the Ge/SiGe heterostructure were built in Comsol MultiPhysics® based on the architecture shown in Figure 3.7(a). The geometrical model of Figure 3.7(b) is discretized into small units of simple shapes (or meshed elements) as shown in Figure 3.8 (a). The software has an inbuilt mesh generator that performs the discretization. In this case, the discretization resulted to a total of 10121 meshed elements. The mesh was partitioned into domains, boundaries, edges and points; this partitioning is essential to set up the physics of the FEM [69].



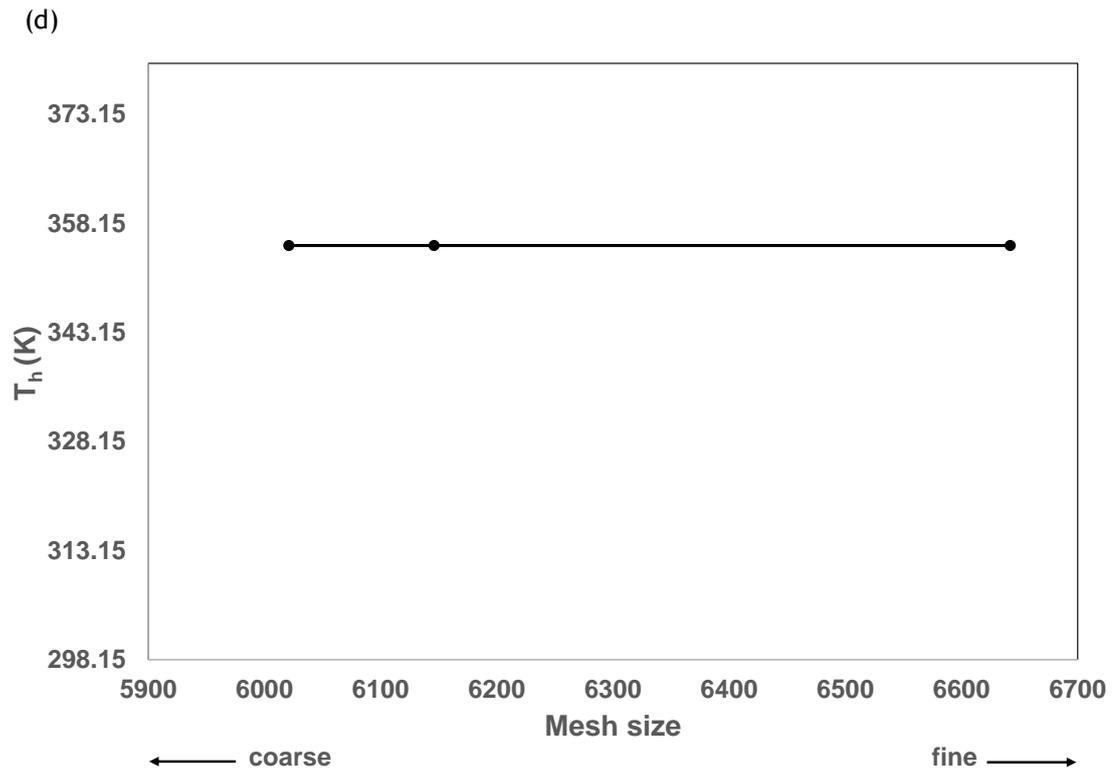


Figure 3.8: (a) Meshed diagram of the micro-fabricated heterostructure for FE simulation (b) expanded diagram showing the centre of the heterostructure (c) a sliced 2-D diagram showing the quality of the mesh under the surface of the device. (d) Evaluation of Mesh dependency of results

It can be seen from Figure 3.8(a) that the mesh is finer towards the centre of the geometry. This is to allow for sufficient accuracy at the area of interest, which is the middle of the heterostructure (see the expanded diagram of Figure 3.8 (b)). Additionally, using fine mesh at the area of interest and coarse mesh at other areas of the geometry saves computational time compared to the use of fine mesh throughout the geometry of the FEM. The mesh sizes of the heterostructure was varied within the range of 6000 - 6650 domain elements as shown in Figure 3.8 (d). The significance of this variation is to provide evidence that the results obtained from the simulation are accurate. The heterostructure could only be meshed within this small range because of the challenge faced in meshing the heterostructure which is a combination of very thin and very large layers (see the 4th column of Table 3.2).

Another aspect of meshing to consider is the quality of the mesh elements. Figure 3.8(a) also shows the mesh quality of the FEM, which ranges between 0 – 1, where 0 represented by the dark blue colour indicates the lowest mesh quality while 1 represented by the red colours indicates the highest mesh quality [71]. A low quality mesh is more likely to result in systematic errors in the final

solution compared to a high quality mesh. The figure shows that low quality mesh only exist farther away from the area of interest so that any error arising thereby would not have any significant impact on the final results. A slice through the diagram is shown in Figure 3.8 (c) to show the internal mesh quality of the device. From this diagram, it can be seen that the superlattice structure, which is the area of interest, has a mesh quality of about 0.7, which implies that the results obtained from the FEM are 70% reliable. Moreover, identical simulations were run using different mesh sizes (i.e. between normal and extra coarse mesh sizes) and the results obtained remained the same. This exercise confirms that the mesh in Figure 3.8 is of good quality for the present FEM.

A mesh quality of 0 is observed at the substrate level of Figure 3.8c. It is important to note that this quality of mesh does not affect the simulation results for the following reasons: the temperature profile is relatively the same throughout the substrate level due to its high thermal conductivity of 150 W/mK (see the sliced diagram of Figure 3.10a below). Recall that the boundary temperature was specified at the bottom of the substrate to be at room temperature (i.e 298.15 K). This temperature remains relatively the same until it gets to the buffer layer where the temperature begins to vary slightly because it has a much lower thermal conductivity of 20 W/mK. A significant variation in temperature is then seen for the superlattice because of its low thermal conductivity of 4 W/mK. Hence it will suffice that a good mesh quality is necessary for the buffer and superlattice layer but not necessary for the substrate. Thus the substrate's mesh quality of ~ 0 does not compromise the simulation results.

3.3.4.FE simulations and analysis for material characterization of Ge/SiGe superlattice

The input dimensions and the κ values for each layer used in the simulation are stated in Table 3.2. Also, in-line with the published experiments [6, 7], two simulations were carried out, namely: (i) full structure and (ii) half-structure Ge/SiGe superlattice.

Full structure: this is a completely fabricated Ge/SiGe superlattice (see Figure 3.9(a)) and its FEM is represented in 3D-view as shown in Figure 3.9(b). The temperature profile shown on Figure 3.9(b) is for $\kappa = 5$ W/mK

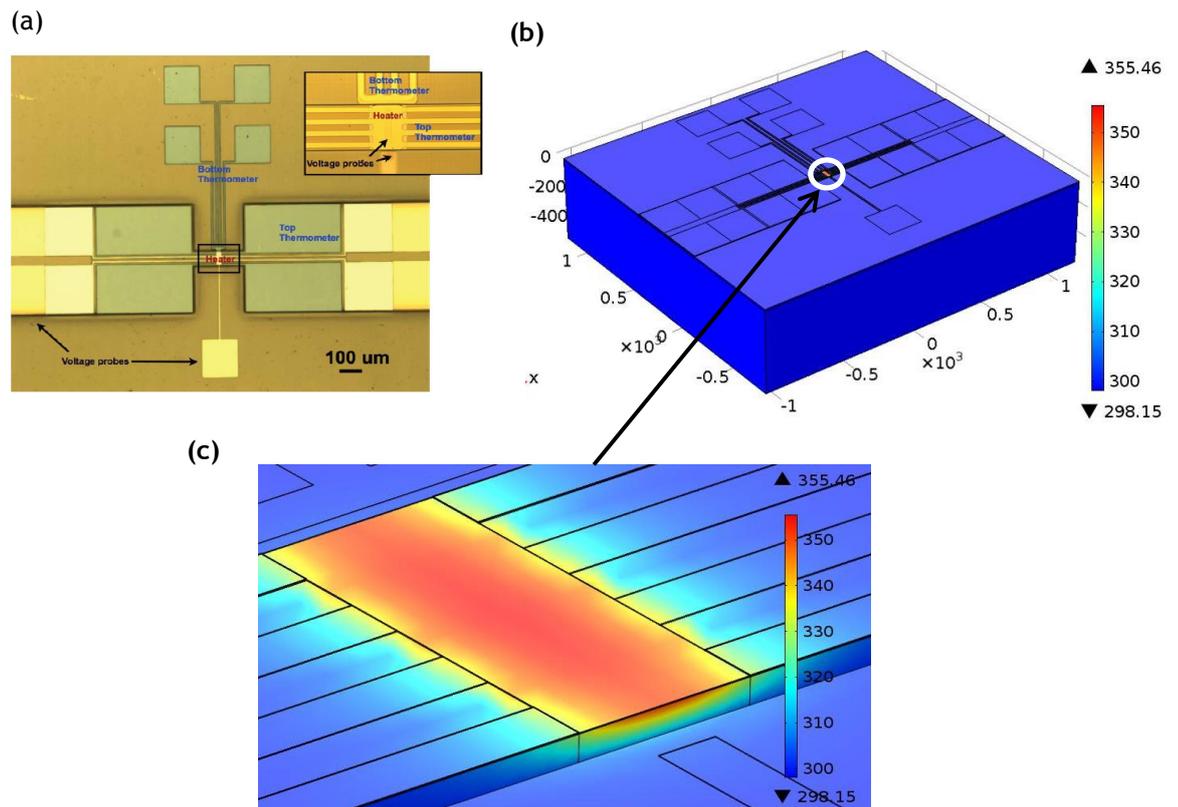
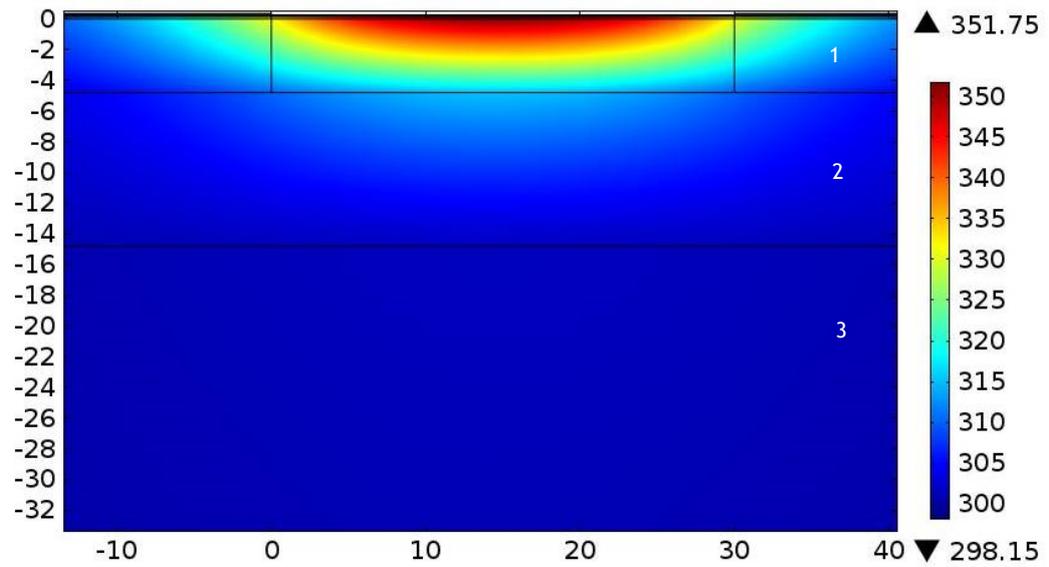


Figure 3.9: (a) Optical microscope image of the fabricated full-structure [6, 7] (b) FEM Simulation of the full-structure Ge/SiGe superlattice for $\kappa = 5 \text{ W/mK}$ (c) Expanded view of the centre image of (b) highlighted by the white circle.

Note that Figures 3.10 (a) and (b) are not drawn to scale and shows an enlarged section of the area of interest. These figures reveal that most of the heat is conducted downwards through the superlattice because the heat is applied in the vertical direction. Also, the underlying silicon substrate is large both in size and κ -value when compared to the other layers and acts as an efficient thermal sink. The temperature plot shows the largest ΔT for the superlattice region, which can be attributed to its small κ -value.

(a) Temperature distribution



(b) Heat distribution (W)

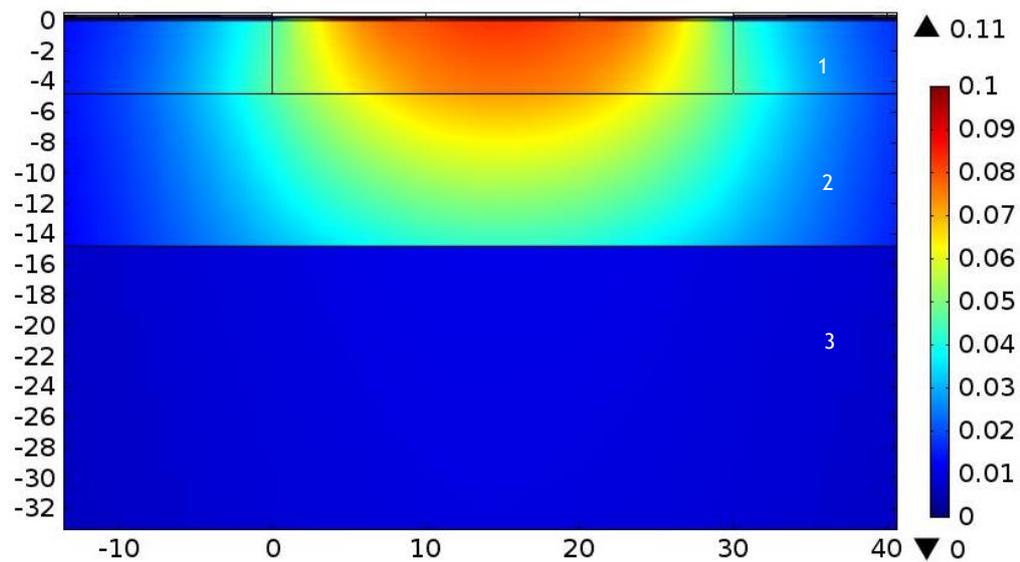


Figure 3.10: Expanded view of 2-D profile showing (a) Temperature distribution and (b) Heat distribution, for $\kappa = 5 \text{ W/mK}$; 1-superlattice, 2-Buffer layer and 3-silicon substrate.

Half structure: The half structure was designed with half of the superlattice etched away. This structure was used in the experiments [6, 7] to estimate the heat losses in the device. Therefore, for completeness and comparison, the half structure is also modelled as shown in Figure 3.11.

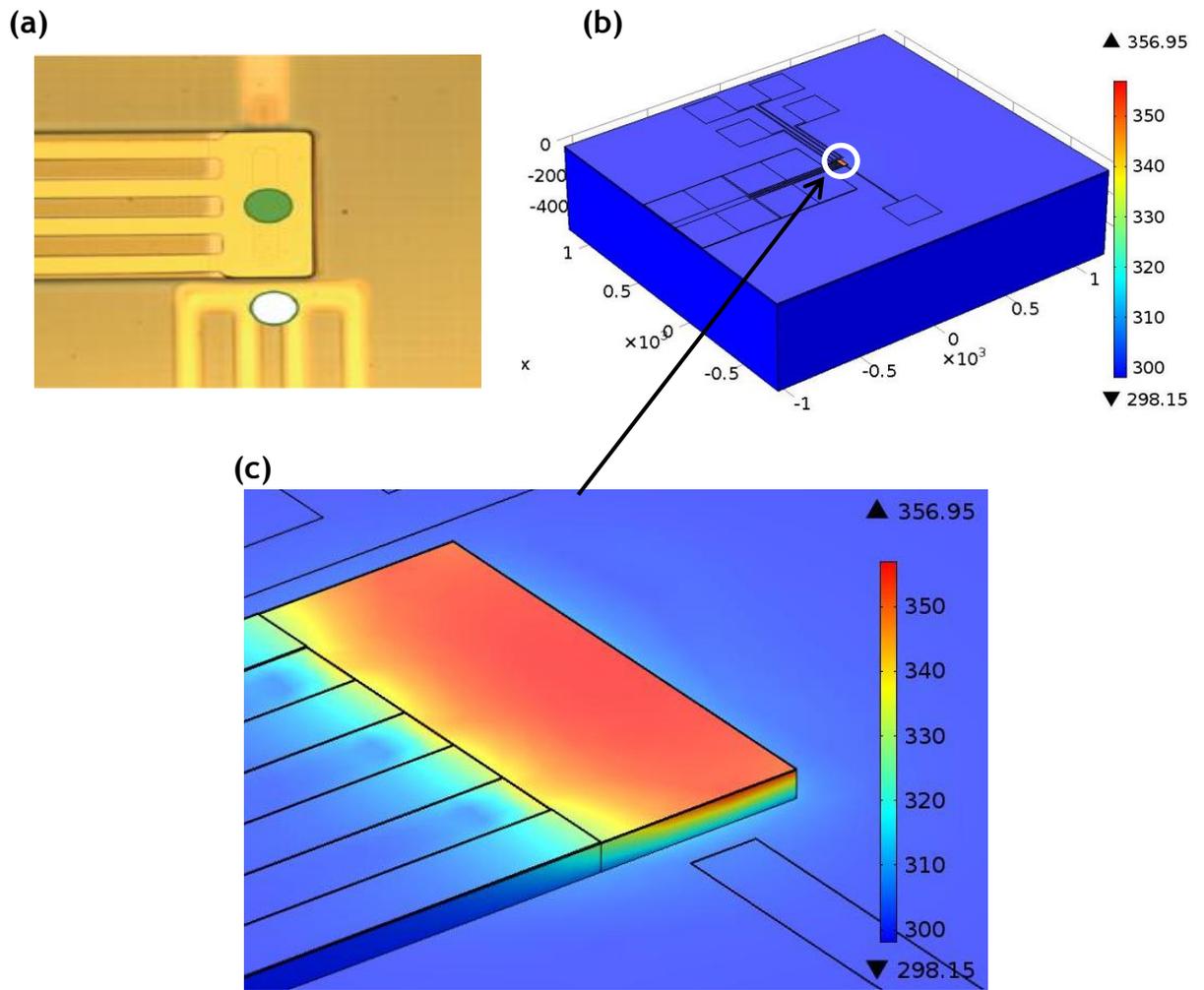


Figure 3.11: (a) Optical microscope image of the fabricated half-structure [6, 7] (b) FEM simulation of the half-structure Ge/SiGe superlattice for $\kappa = 5 \text{ W/mK}$ (c) Expanded view of the centre image of (b) highlighted by the white circle.

3.4. Comparison of FEM with Experimental Results

The FEMs used for comparison are based on two separate experiments reported in references [6] and [7] respectively. Both experiments were conducted using the same micro-fabrication technique. The major difference between the experiments is that the material used in experiment 1 has a superlattice thickness of $4 \mu\text{m}$ while that of experiment 2 has a thickness of $3 \mu\text{m}$ (see Table 3.2). The variation in thickness is as a result of different designs of the superlattice [6]. The purpose of these designs is to determine the material with the highest ZT and power factor.

In this section the thermal conductivities for both experiments [6, 7] are compared with FEM results. With respect to the Seebeck coefficient, only one

experiment [7] is considered for comparison because the second experiment [6] does not discuss the Seebeck coefficient.

3.4.1. Thermal conductivity

Experiment 1: $\kappa = 5.1 \pm 0.4$ W/mK [7]; Simulation $\kappa = 5$ W/mK

The value of κ estimated from experiment [7] is equal to 5.1 ± 0.4 W/mK. Based on the error margin for this estimate, a range of κ values between 4.8 - 5.4 W/mK was used as input to the FEM simulation, and a value of $\kappa = 5$ W/mK was observed to produce similar results that are comparable to that of the experiment (see Figure 3.12). This shows that the value of κ obtained from the FEM simulation differ from that of the experiment by approximately 3% only.

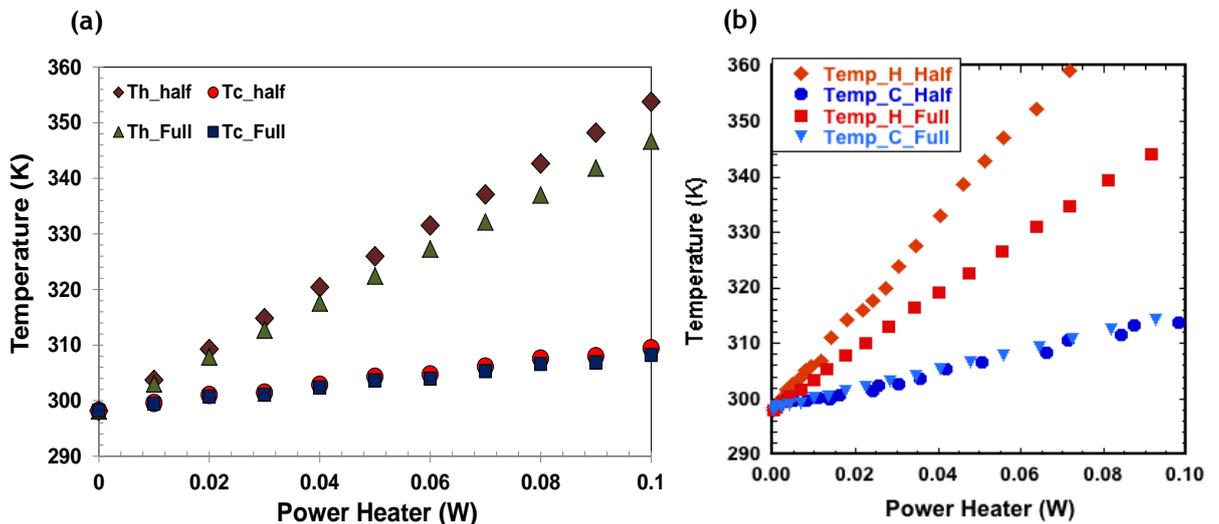


Figure 3.12: (a) Temperature profile versus power heater for a simulated full and half structure with a κ value of 5 W/mK (b) Experimental data [7] for both half and full structures.

For the full structure, the FEM simulation produces similar estimates of the temperature profile as the experiments for both hot and cold sides. In the case of the half-structure, the FEM simulation produced similar estimates of the temperature profile as the experiments for the cold side, but there are significant differences between both results for the hot side. The measurement results [7] reported for the hot side of the half structure were reproduced from a linear fit analysis of the actual recorded temperatures. The linear fit was performed based on the assumption that most of the heat is lost in the in-plane direction due to the high κ value of the metals in the Ge/SiGe heterostructure. Thus, it was supposed in reference [7] that by etching away half of the

heterostructure, including the metals and the superlattice, the heat loss will be greatly reduce and a large ΔT can be obtained. The simulations performed in this study for the half structure FEM suggests otherwise. Since the dimensions of the metal interconnectors are small (in nano-scale) compared to the superlattice structure (in micro-scale), the conductive heat losses in the in-plane direction through the metal connectors are much smaller than supposed in reference [7]. This explains why the simulation of the half structure FEM predicts a heat loss of about 27% in the superlattice compared to 41% reported in reference [7].

Experiment 2: $\kappa = 6 \pm 0.4$ W/mK [6]; Simulation $\kappa = 6.4$ W/mK

A similar Ge/SiGe material was used for the second experiment [6]. The main difference is that it has a superlattice thickness of $3\mu\text{m}$ as compared to that of experiment 1 which has a thickness of $4\mu\text{m}$ (see Table 3.1). Similar results were obtained for experiment 2 based on the analyses described above. Simulated temperatures for a κ -value of 6.4W/mK closely matched the experimental temperatures that produced an estimated κ value of 6 ± 0.4 W/mK (see Figure 3.13). A difference of 8.3% was recorded between the κ values of the FEM simulation and experiment.

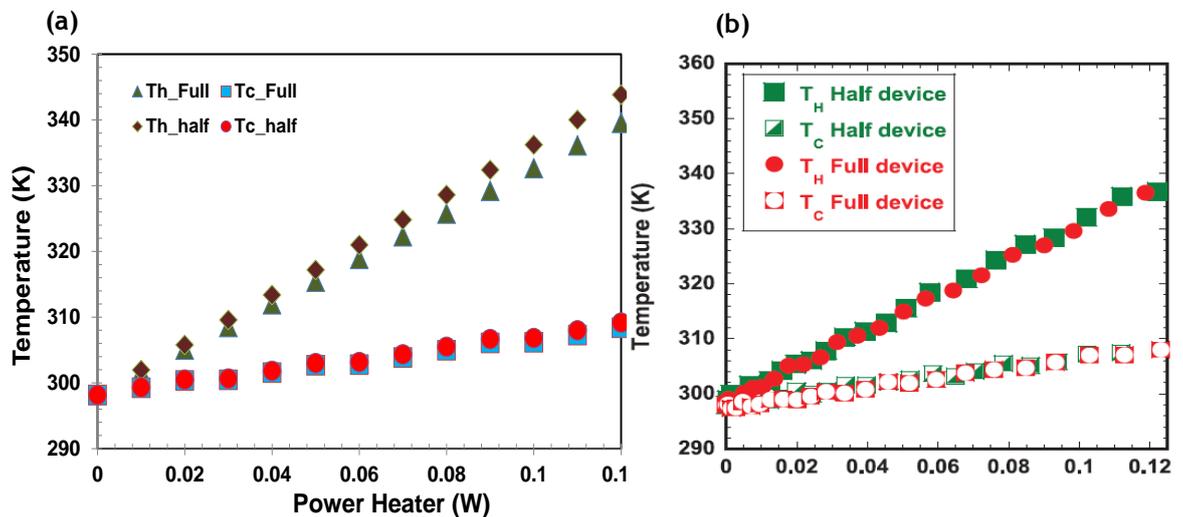


Figure 3.13: (a) Temperature profile versus power heater for a simulated full and half structure with a κ value of 6.5 W/mK (b) Experimental data [6] for both half and full structures.

The experimental plots (see Figure 3.13(b)) for T_h do not show any significant difference between the full and half structure. However, the FEM results for T_h predict a difference between the full and half structure with the latter having higher values. Furthermore, the difference in T_h between both structures

increases with increasing power input and this was also observed in experiment 1 (recall Figure 3.12). The implication of the difference in T_h between both structures is that there is more heat loss in the full structure compared to the half-structure, and the FEM simulation estimates this difference in heat loss as 22.2%. Note that reference [6] does not give an estimate of this heat loss, apparently because there were no significant differences in the measured values of T_h for both structures.

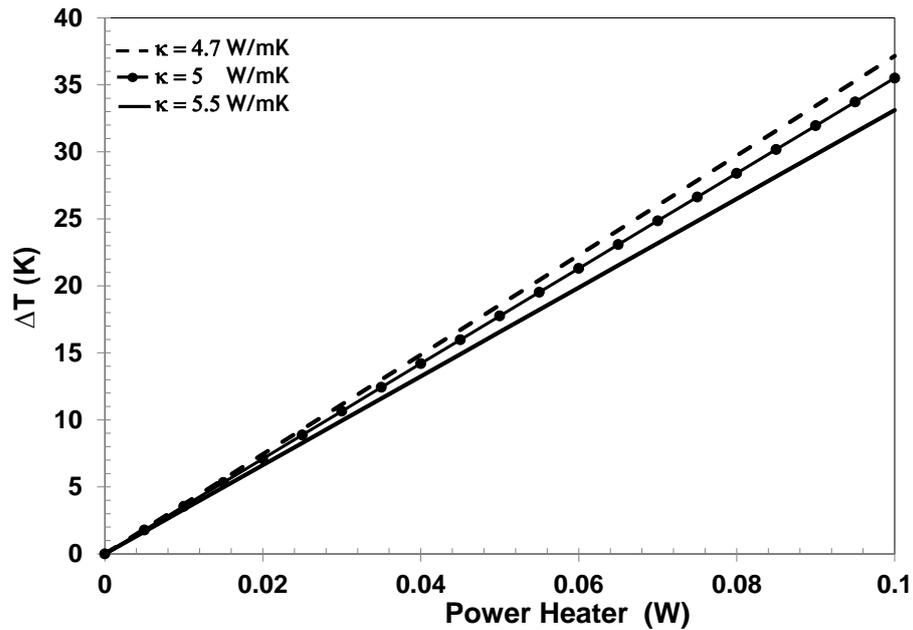


Figure 3.14: The effect on κ on ΔT for varying power heater [72].

Further analysis was carried out, using the FEM, to show the effect of varying thermal conductivities on the ΔT for a specific power input. Figure 3.14 shows the results of the analysis. An increase in thermal conductivity results to an increase in the heat losses in the system, especially in the lateral direction. Consequently a drop in the temperature difference across the superlattice is observed as the thermal conductivity increases (see Figure 3.14). This analysis shows that a thermoelectric material with low thermal conductivity is more efficient for building thermoelectric generators.

3.4.2. Seebeck Coefficient

The calculation of α based on Equation (3.4) depends on accurate estimation of ΔT and ΔV across the superlattice structure. For the metallic layers, the respective Seebeck coefficients are very small [4, 67] in comparison to the Seebeck coefficient of the superlattice structure. Hence, contributions from the metallic layers are considered to be negligible. Based on the simulated temperature profile of the superlattice (see Figure 3.15) it is observed that the temperature at the bottom surface, T_{cb} , is slightly higher in value than the side temperatures, T_c . Experimentally, it is difficult to measure T_{cb} because the superlattice was grown directly above the buffer layer and therefore, its bottom surface is not accessible for temperature measurements. Hence, the closest measurement that can be taken is T_c .

The experimental temperature measurements are obtained using the principle of the 4-terminal probe (observe the 4 metallic lines of the thermometers in Figure 3.11(a)). The principle of operation of a four-terminal probe is illustrated in Figure 4.10 (page 90) of this thesis. The 4-point terminal probe measurement is used to accurately determine the resistance, R between the voltage sensing connections for both the top and bottom thermometers (see the marked region indicated by the green and white circle in Figure 3.11(a)). Thereafter, the Thermal Coefficient of Resistance (TCR) of the fabricated thermometers is used to translate the change in resistance into a change of temperature and this will give an accurate reading of the temperature difference, ΔT measured across the mesa [18].

An increase in the heat source will result to an increase in the expansion of the metallic lines and hence an increase in the measured resistance and consequently an increase in the measured temperature. The four-terminal probe principle is applied for each measurement taken whereby current of known value is passed through one end of the metallic lines and the differential voltage reading is taken via the two middle metallic lines. By using Ohm's law, the resistance across the two middle metallic lines is obtained. Thereafter, TCR is used to obtain the equivalent temperature.

The green and white circles are used to indicate the position of the top and bottom thermometers. The experimental thermometers are actually rectangular in shape (not circular) and are positioned between the two middle lines of the 4-terminal probe (i.e. at the centre of the 4-terminal probe). The distance of the experimental thermometer from the mesa is approximately $4\ \mu\text{m}$; while that of the simulated thermometer is $10\ \mu\text{m}$. This discrepancy is as a result of the difficulty in meshing the structure when the thermometers are very close to the mesa. Thus, average temperature readings from the position of the rectangular surface area of the simulated thermometer were taken and compared with average temperature readings taken directly on the side line of the mesa and this two readings only differed by 0.9%. This implies that any temperature reading taken between $0 - 10\ \mu\text{m}$ are approximately the same. Therefore the simulated temperature readings are comparable to that of the experimental temperature readings; since the distance of the experimental thermometer from the mesa is approximately $4\ \mu\text{m}$ and falls within the range of $0 - 10\ \mu\text{m}$.

The results for the experiment and FE simulation are observed to be in good agreement for the full mesa structure, (see Figures 3.12 and 3.13). Therefore, the FEM can be used for further analysis such as the determination of the true temperature gradient (i.e. $\Delta T = T_h - T_{cb}$) which is difficult to obtain experimentally. This limitation of the experiments in determining T_{cb} due to the inherent physical constraint of the experimental design set-up underscores a key advantage of the FEM. Referring to Figure 3.15(b), it can be seen that the optical image for the experiment is only able to take temperature readings for T_c and T_h , because the bottom surface required for taking temperature readings, T_{cb} , is inaccessible. The multi-layered heterostructure is a combination of three major layers which are: the superlattice, at the top most; the buffer layer, which is directly below the superlattice; and the silicon-substrate at the bottom of the device. The layer of interest is the superlattice, which allows temperature readings for T_h to be taken. However temperature readings for T_{cb} cannot be taken because its bottom surface is attached to the buffer layer. Therefore the approximate temperature reading, T_c that can be taken from the experimental device is at the bottom side of the superlattice. Thus the advantage of the FEM is that it can be used to estimate the desired bottom

surface temperature T_{cb} , thereby allowing for more information of the experimental device to be obtained.

In principle, T_{cb} is the actual temperature that should be used to estimate ΔT across the superlattice structure i.e. $\Delta T = T_h - T_{cb}$.

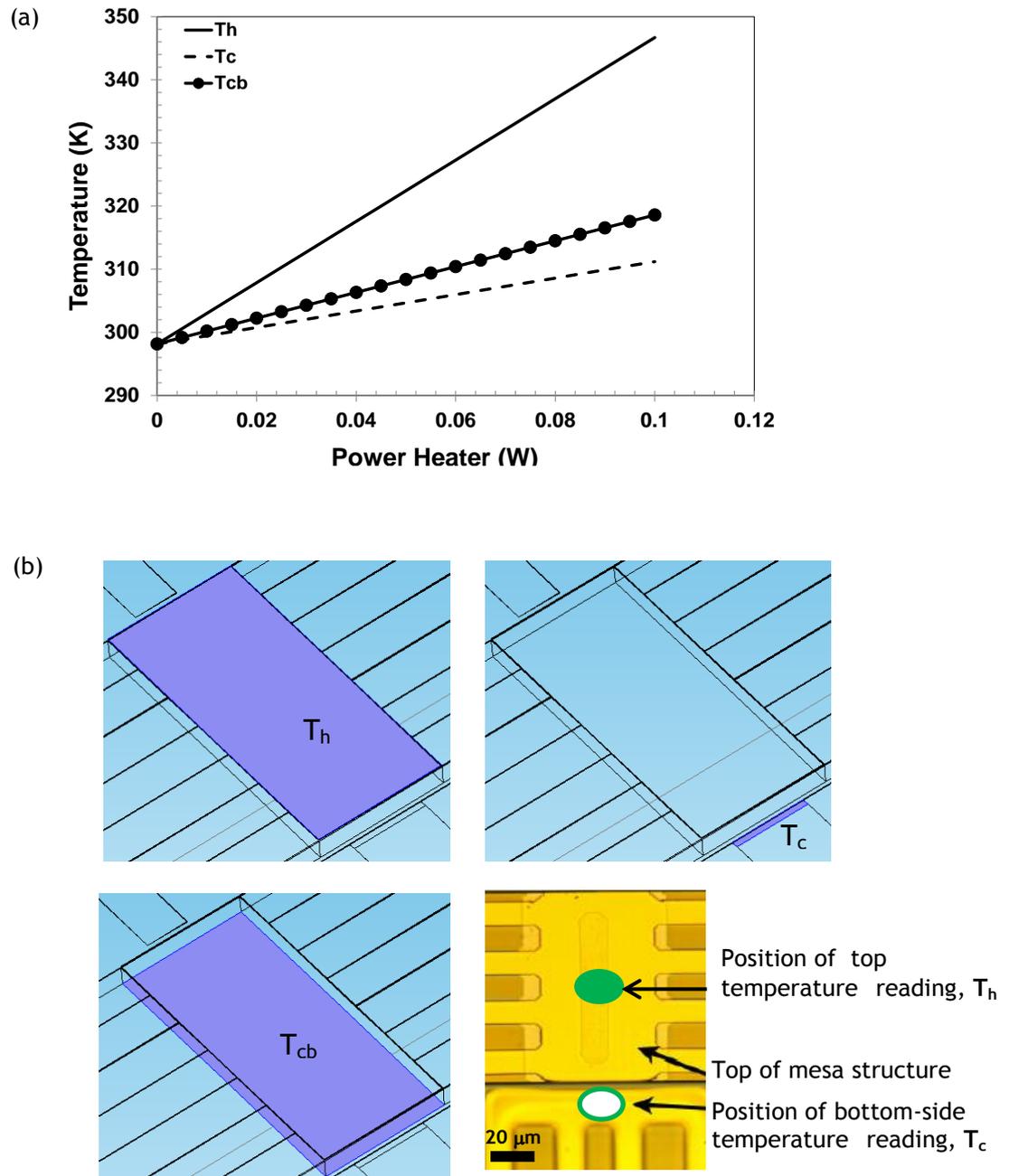


Figure 3.15: (a) Simulation of temperature profile for T_h , T_{cb} and T_c (b) Diagram illustrating the positions where T_h , T_{cb} and T_c were estimated in comparison to the optical microscope image of the fabricated Full-structure [6, 7] (bottom-right)

Determination of α based on $\Delta T = T_h - T_c$:

As explained earlier, the temperature profile of the cold side of the superlattice were obtained by taking measurements at the bottom side of the superlattice because its bottom surface is inherently inaccessible by design. Hence, FEM simulations were carried out in which the cold side temperature profile was estimated at bottom side of the superlattice, in order to determine a simulated Seebeck coefficient that could be compared with the experimental estimates of reference [7]. The gradient of the open circuit voltage versus ΔT plot gives the Seebeck coefficient. The FEM simulation predicts an α value of $400\mu\text{V/K}$ whereas the experimental estimate of α is $394.1 \pm 6 \mu\text{V/K}$ (Figure 3.16). The percentage difference in both results is 1.5% and the FEM prediction of α falls within the tolerance range of the experimental estimate. This suggests that the FEM simulation validates the experimental estimate of α that was obtained based on measurements of the cold side temperature taken at the bottom side of the superlattice.

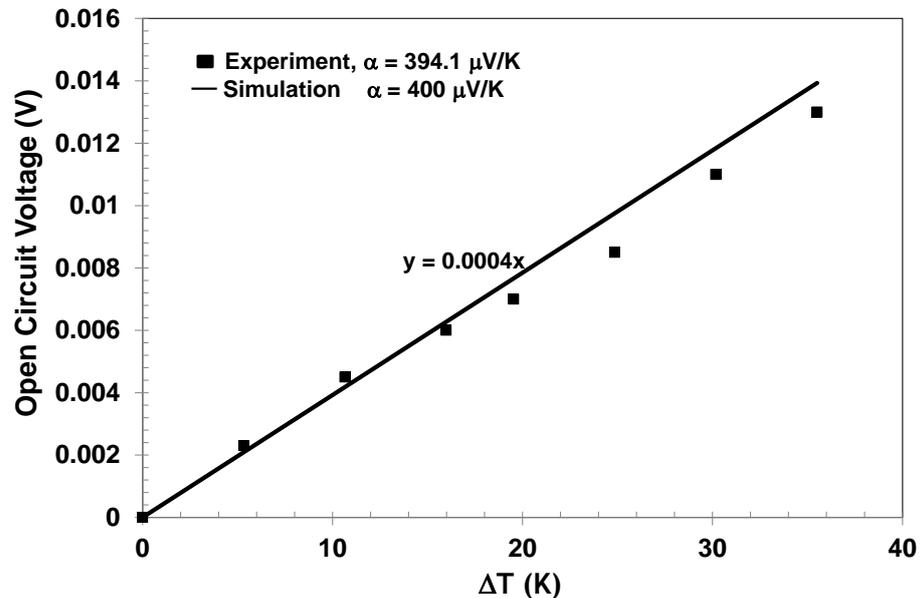


Figure 3.16: Comparison of simulated open circuit voltage with corresponding experimental voltages obtained from reference [7].

Determination of α based on $\Delta T = T_h - T_{cb}$

A second FEM simulation was performed in which the cold side temperature is estimated at the bottom surface of the superlattice. This investigation was conducted because the temperature difference in the superlattice should be estimated based on the temperatures at the top and bottom surfaces. For this

case an α value of $500 \mu\text{V/K}$ was predicted (see Figure 3.17). This prediction gives a difference of 21% compared to the experimental estimate of reference [7].

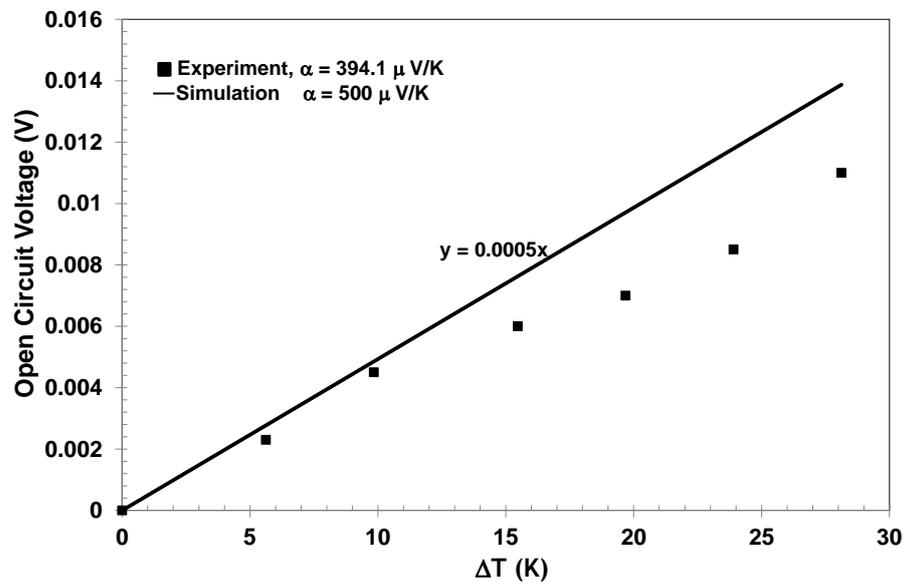


Figure 3.17: Open circuit voltage versus $\Delta T = T_h - T_{cb}$

Based on the foregoing analyses, it can be concluded that the experimental technique in combination with the FEM is valid for extracting the α and κ of the Ge/SiGe heterostructure. An important advantage of the FEM is that it can be used to observe the heat and temperature distribution in the heterostructure so that the possible mechanisms of parasitic heat loss in the device can be identified.

Finally, the estimated ZT at 300 K by the literature [7] is 0.08 ± 0.011 . Assuming high temperature applications of up to 1000 K, the ZT can roughly be estimated to be 0.27 ± 0.011 (i.e. assuming linearity). Recall from Figure 2.9 (a) of Chapter 2 that the 0D SiGe-based material for the p-type has a ZT of 0.95 at ~ 1000 K. Although the ZT value of the investigated Ge/SiGe material falls below the literature values of Figure 2.9 (a), it can still be considered to be acceptable. This is due to the fact that the Ge/SiGe is a novel material that was recently developed. Also, the design and development of the Ge/SiGe gives more room for further improvements in the near future.

Chapter Summary

This chapter presents a novel nano-fabricated 2D Ge/SiGe superlattice that is used in this work. The material was developed as part of the Green Si project for building microfabricated TEGs. The technique used in growing the material is the Low Energy Plasma Enhanced Chemical Energy Vapour Deposition (LEPECVD) technique [9]. The quality of the developed Ge/SiGe material is evaluated based on the conversion efficiency defined by ZT, and generated output power defined by the power factor. Thus, measurement of the thermoelectric properties of the Ge/SiGe superlattice structure was performed, as described in the literatures [6, 7], with the purpose of ascertaining the quality of the developed material. To this effect, an experimental technique was developed [6, 7] to measure simultaneously both the Seebeck and thermal conductivity properties of the Ge/SiGe superlattice. Due to the issue that arises with thermal measurements, it becomes difficult to obtain an accurate estimation of the thermal conductivity property.

Thus an independent verification, which is based on Finite Element Modelling (FEM), was required to evaluate the recently developed experimental technique [6, 7]. The FEM was developed using Comsol Multiphysics®. The software package allows for the geometrical representation of the Ge/SiGe material and the specification of the individual properties for the different layers i.e. Silicon substrate, buffer layer, superlattice and metal contacts. The governing equation used for the FEM simulation is the Joule heating model which was expanded to account for the thermoelectric effects. A significant step in the development of the FEM is the meshing or discretization of the geometrical representation of the material. A high quality mesh is required at the middle section of the Ge/SiGe material where the heat source is applied and the temperature and voltage measurements are taken. This is to allow for sufficient accuracy of the results obtained from the FEM simulation.

Finally, a comparison of FE simulation and experimental results was performed. Based on this comparison, it was concluded that the FEM can be used in conjunction with the experimental technique to obtain accurate estimations of the thermal conductivity and Seebeck coefficient for material characterization purposes.

4. Experiment: Microfabrication and Testing of Ge/SiGe-based Thermoelectric Generator

Previous experimental work of the properties of the Ge/SiGe heterostructure [6 7] has been validated by Finite Element Modelling (FEM), using COMSOL Multiphysics® as software. Details of the validation are discussed in Chapter 3 of this thesis. This validation gives confidence in the estimated values of the thermoelectric properties of the Ge/SiGe heterostructure. The next logical step in investigating the Ge/SiGe heterostructure is to determine its power generating capacity when used as a Thermoelectric generator (TEG). This chapter presents details of the fabrication and testing of a simple Ge/SiGe-based TEG module. The fabrication process was performed in the James Watt Nanofabrication Centre (JWNC), University of Glasgow. The major components of the TEG module are: a single p-leg and a single n-leg fabricated from p-type and n-type Ge/SiGe heterostructures respectively, a connector to join the p-leg and n-leg electrically in series and thermally in parallel, and a bonding material to bond both legs to the connector. In the experiment, the legs were connected electrically in series using an Aluminum connector. Indium metal was used to bond the legs to the Aluminium connector. The fabricated module was tested based on the Seebeck effect principle i.e. a temperature gradient is created across the device in order to generate a Seebeck voltage. Two sets of temperature and voltage measurements were taken: one for open-circuit and another for closed-circuit connections. The experimental measurements of the Seebeck voltage were used to investigate the power generating capability and efficiency of the Ge/SiGe-based TEG module.

4.1. Fabrication of Ge/SiGe-based TEG Module

A simple Ge/SiGe-based TEG module consisting of one p-leg and one n-leg was fabricated and tested at the JWNC, University of Glasgow. The fabrication process involves five main stages, namely:

1. Photolithography
2. Etching
3. Metallisation
4. Bonding and
5. Continuity test.

The stages of the fabrication process were carried out in the order listed above. This was necessary because each stage depends on the immediate preceding stage. A detailed discussion of each of these stages is presented next.

4.1.1. Photolithography

Photolithography is a micro-fabrication technique that uses ultraviolet light to transfer geometrical patterns from a photomask unto a photoresist on the substrate [73, 74]. The photomask used is usually an opaque 4-inch low expansion glass-ferric plate with pre-defined transparent patterns on it. When ultraviolet light passes through the photomask the pre-defined patterns are transferred to a light sensitive chemical called photoresist. Prior to photolithography, the following basic steps are conducted.

1. **Cleaning of the sample:** first, the wafer samples of the Ge/SiGe superlattice are cleaned in acetone and subsequently in isopropyl alcohol solutions in order to remove traces of particles or organic impurity. The samples are placed in beakers containing the cleaning chemicals and each beaker is placed in an ultrasonic bath where it is shaken for about five minutes. Shaking the beakers makes the removal of impurities to be more effective. Figure 4.1a shows a section of the JWNC clean-room, where the cleaning process takes place. Figure 4.1b shows an in-built ultrasonic bath containing a beaker and the cleaning chemicals.

(a)



(b)



Figure 4.1: (a) a section of the JWNC clean room (b) Ultrasonic bath holding a beaker containing the sample and cleansing chemical (acetone-isopropyl).

2. **Resist Coating:** this process involves placing a photoresist on the cleansed wafer and spinning the wafer to allow even distribution of the photoresist on the wafer. Two types of photoresist were used namely: (a) negative photoresist (AZ2070) which is mostly used for metallisation and (b) positive photoresist (AZ4562) mostly used for etching process. The spinning speed for both types of resist is 4000rpm. After each spin, a resist thickness of 7.0 μm and 6.2 μm is obtained for the negative and positive resist respectively.
3. **Soft baking:** after placing the photo resist on the sample, it is baked on a hot plate for a few minute. The baking temperature and time depend on the type of photo resist being used whether negative or positive. A negative photo resist requires soft baking at 110°C for 90 seconds while positive photo resist requires soft baking at 100°C for 380 seconds. Although most of the solvents are removed from the photo resist during the spinning process, soft baking helps to further remove any residual solvents from the photoresist coating. This allows for further adhesion of the photoresist to the sample thereby preventing the mask plate from sticking to the sample during photolithography.
4. **Mask alignment and exposure:** a mask plate or photomask plate is a chrome plate with transparent patterns through which ultraviolet light passes, thereby transferring the pattern unto the sample coated with a photoresist. The light source used in this case is a 350 W mercury lamp. A photoresist is a chemical substance that is sensitive to light. The mask plate is aligned such that the geometrical patterns are faced directly above the sample and ultraviolet light is passed through the transparent patterns of the mask plate. The patterns are then transferred onto the spun sample described in (2) above. The section exposed for a positive photoresist becomes hardened, while the section exposed for a negative photoresist becomes softened as illustrated in Figure 4.2. The equipment used for the mask alignment and exposure is called MA/6 [75] (see Figure 4.3).

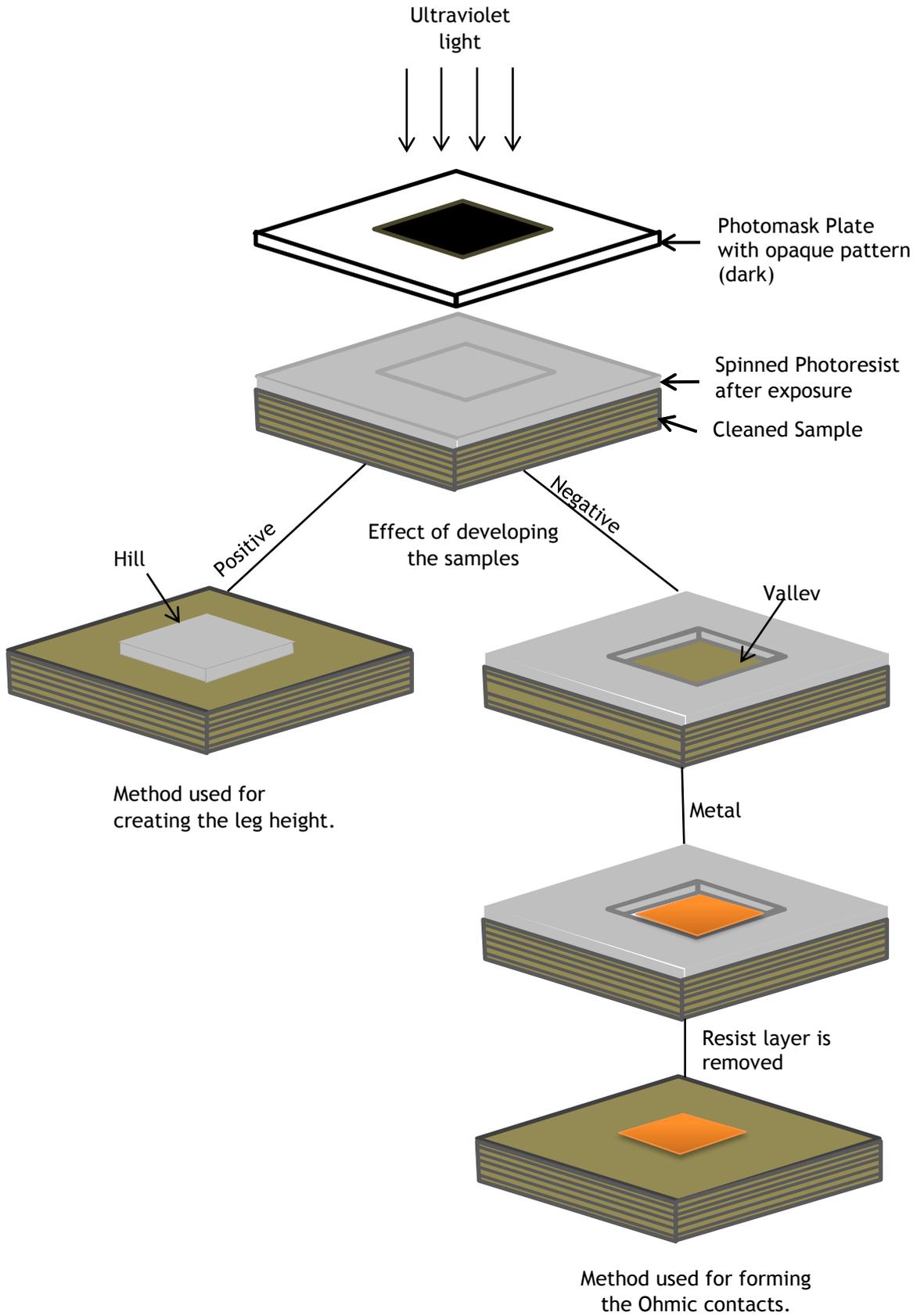


Figure 4.2: Photolithography process: Etching and Metal deposition



Figure 4.3: MA/6 tool used for mask alignment and exposure to transfer a defined pattern onto the sample [76]. Red arrows points to the optical microscopes and hand knobs for viewing the sample during alignment. The white circle shows the ultraviolet light exposure after alignment. The exposed sample and photomask is beneath the light.

5. **Post-baking:** during post-baking the AZ2070 negative resist samples are baked on a hot plate for a minute at 110°C in order to finish the cross linking process that starts with exposure. Developing the sample immediately after exposure, without post-baking, will wash away all the desired patterns. Hence, post baking for the AZ2070 negative resist is required in order to retain the desired patterns obtainable after development. Regarding the positive photoresist, AZ4652, post baking is not a necessary requirement.
6. **Development:** this process involves developing the post-baked sample in a chemical (MF-319) in order to remove the unexposed photoresist of a negative photoresist; hence, creating a valley that allows metals to be deposited directly on the sample in a defined pattern. For a positive photoresist, the sample is developed in a chemical called AZ400K to remove the exposed photoresist, hence leaves a hill as shown in Figure 4.2.

4.1.2. Etching

Etching is the removal of unwanted sections from the material sample. By etching, the pattern of the hill resist is transferred to the underlying layer to form a mesa structure (see Figure 4.2). This approach was used to form the p-type and n-type legs of the Ge/SiGe-based TEG. Prior to etching, a positive photoresist (AZ4562) was used for the photolithography process in order to create the desired pattern for the legs. A Surface Technology System (STS) [77,

78] was used to create a vertical etch around the masked pattern in order to produce a mesa that forms the legs. The STS is an Inductively Coupled Plasma (ICP) tool that produces plasma (or excited ions) from reactive gases, in this case SF_6 and C_4F_8 . The plasma is produced by subjecting the gases to a strong electromagnetic field that is created by two Radio Frequency (RF) power generators. The excited ions bombard the exposed section of the sample there by etching it away. The etched depth of the legs for the Ge/SiGe-based TEG module is $3.4 \mu\text{m}$ (see Figure 4.4(a)). A DeKtak measuring tool was used to measure the actual depth of the legs as shown in the plot of Figure 4.4(b). The red circle in the plot indicates the measured height in Angstrom.

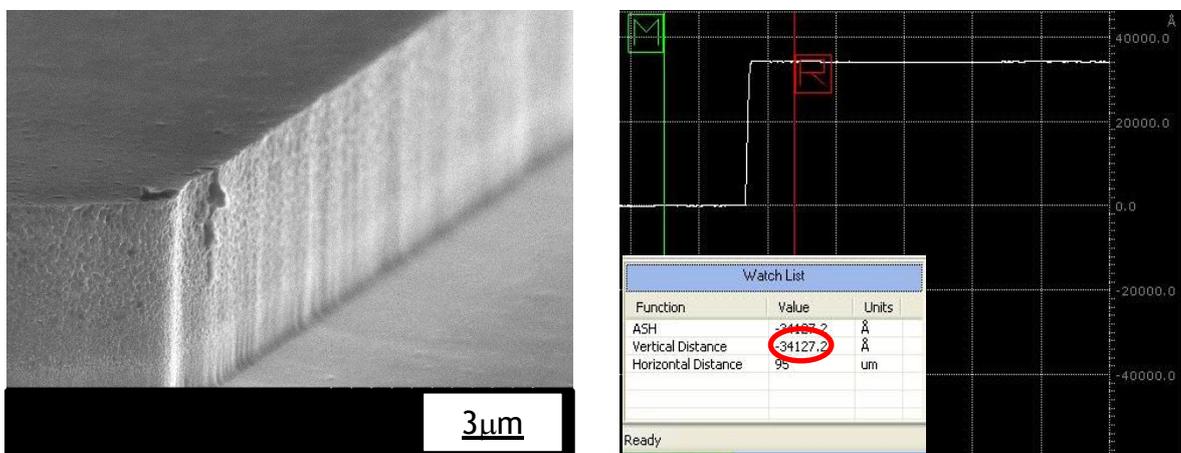


Figure 4.4: (a) SEM image of the n-type leg, etched depth is magnified by $3 \mu\text{m}$. (b) shows the plot of the leg-height ($3.4 \mu\text{m}$) measured from a DeKtak measuring tool.

4.1.3. Metallisation

Metallisation or metal deposition is the use of electron beam to evaporated metals onto the sample. A negative resist, AZ2070, was used in this case to create a valley, after development as shown in Figure 4.2. Lift-off is then conducted by placing the sample in a beaker of Acetone and placing the beaker in a warm water bath of about 50°C . This makes the resist layer to Lift-off (or detach) from the sample, thereby leaving only the desired metal pattern on the valley section of the sample. The valley section is the section without a resist layer, which was removed during development.

In fabricating the Ge/SiGe TEG module, 5 nm of nickel and 50 nm of platinum were deposited on the p-leg in order to create the top and bottom Ohmic contacts, while 50 nm of Silver alloy (99% Ag/1% Sb) was used to create the Ohmic contacts on the n-leg. Next, the p-leg was annealed for 30 seconds at

340°C while the n-leg was annealed for 5 minutes at 400°C. Annealing reduces the contact resistance at the interface between the metal and semiconductor. Figure 4.5 shows the n-leg with top and bottom Ohmic contacts. The design and fabrication of the p-leg follows a similar procedure as the n-leg. It is important to note that the total height of the superlattice structure is 4 μm . Of this total height, 3.4 μm was used to form the legs and hence the two-step etched section for the top Ohmic contact as shown in the exploded view of the blue circle in Figure 4.5. The bottom Ohmic contact (exploded view of the red circle in Figure 4.5) shows only one etched step because only 0.6 μm of superlattice structure is left, and this represents the bottom of the leg. Figure 4.6 shows a schematic of a vertical cross-section of the thermocoupled p-leg and n-leg, and the composition and thickness dimensions of the layers that make up the legs are specified.

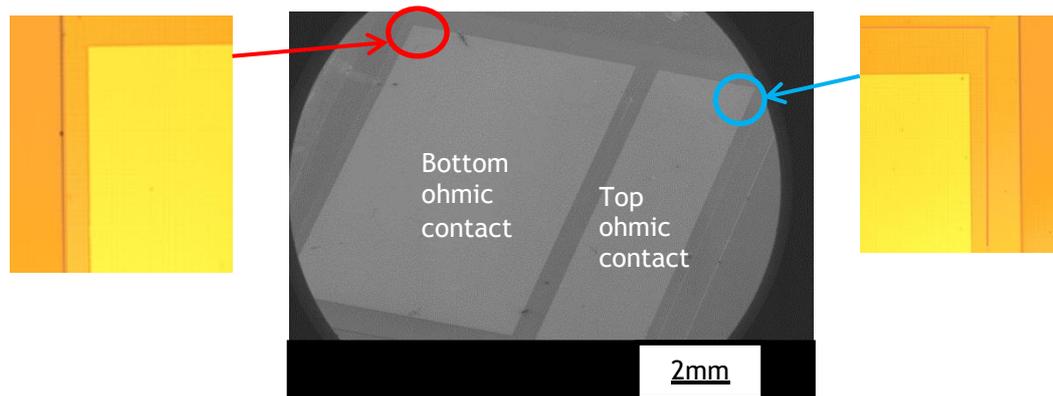


Figure 4.5: SEM image showing a top view of the n-type leg with top and bottom Ohmic contacts, Aluminium pads and Indium solder. (The image is zoomed in to 2mm)

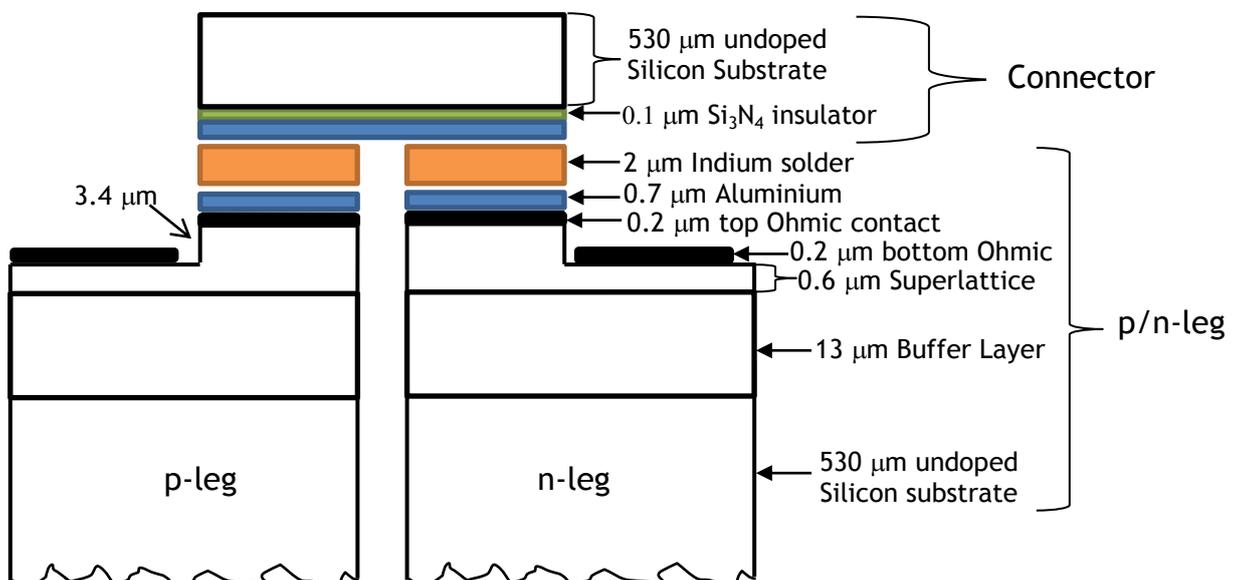


Figure 4.6: Schematic diagram of single p-leg and single n-leg connection

4.1.4. Bonding

The bonding stage entails making an electrical connection between the p- and n-legs. This involves bonding the legs to the aluminium connector using a flip chip bonder (Figure 4.7).

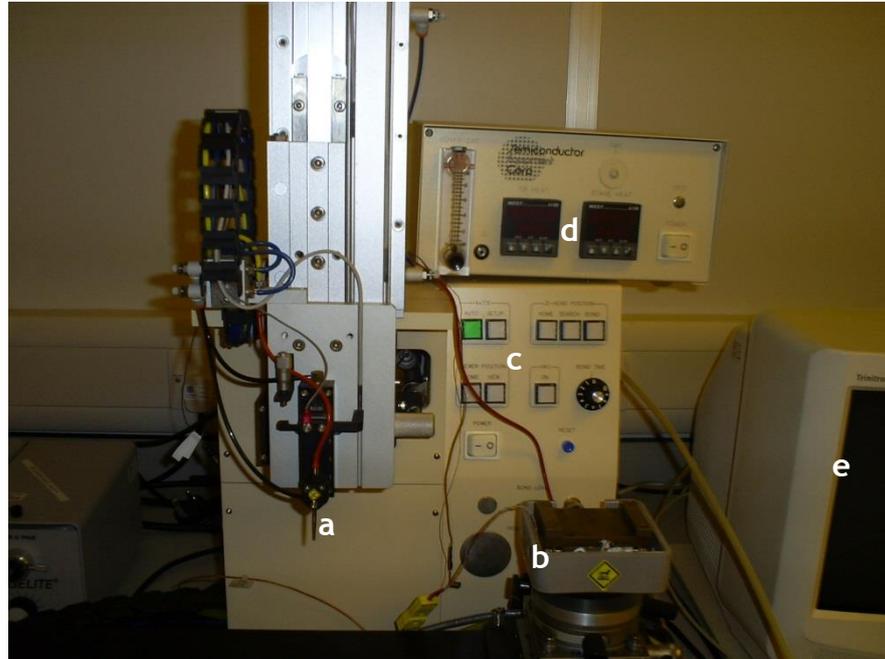


Figure 4.7: Flip chip bonder: (a) Z-head positioner (b) Stage (c) Switch buttons (d) Temperature controller (e) CPU monitor

The main features of the flip chip bonder are:

- a. **Z-head positioner:** this is used to pick the sample, hold it under vacuum and then bond it to the connector.
- b. **Stage:** is used to hold down the connector under vacuum so that the sample on the Z-head positioner can be bonded to it.
- c. **Switch buttons:** are used for two types of control: (i) search and (ii) home. These buttons are used to control the camera and Z-head positioner. The search camera button brings out the camera for viewing the sample while the home camera button returns the camera to its initial position. The same procedure is applicable to the Z-head positioner buttons.
- d. **Temperature controller:** is used to regulate the temperature required for melting the indium, making it suitable for bonding.

- e. **CPU monitor and Camera:** two cameras and a CPU monitor are used to view and align the sample on the Z-head positioner to the connector sample held under vacuum onto the Stage prior to bonding.

In order to prepare the p- and n- legs for the bonding process, 700 nm of Aluminium was evaporated on the top Ohmic contacts. Thereafter, a 2 μm thick layer of Indium was patterned on top of the Aluminium pads. The deposited Aluminium helps to prevent the Ohmic contacts from cracking during bonding. It also helps to promote a firm connection between the legs and connectors.

The connector consisted of an intrinsic Silicon substrate that is passivated (coated) with Si_3N_4 insulator (see Figure 4.6). The purpose of this passivation is to avoid electrical leakages into the Silicon substrate. Next, 700 nm of Aluminium is evaporated on top of the sample. The Aluminium metal allows the conduction of electrons from the p-leg to the n-leg and vice-versa. Next, Indium solder is deposited, to allow bonding of the connector to the p- and n- legs.

The samples (comprising of the legs and connector) were heated for 5 minutes at 150°C to allow the indium to become malleable. A flip chip placement system (Model 850 from SEC) was used to align (Figure 4.8(a)) and bond the legs to the connector (Figure 4.8(b)). After bonding, the system is cooled to room temperature in order to create a strong bond between the legs and the connector.

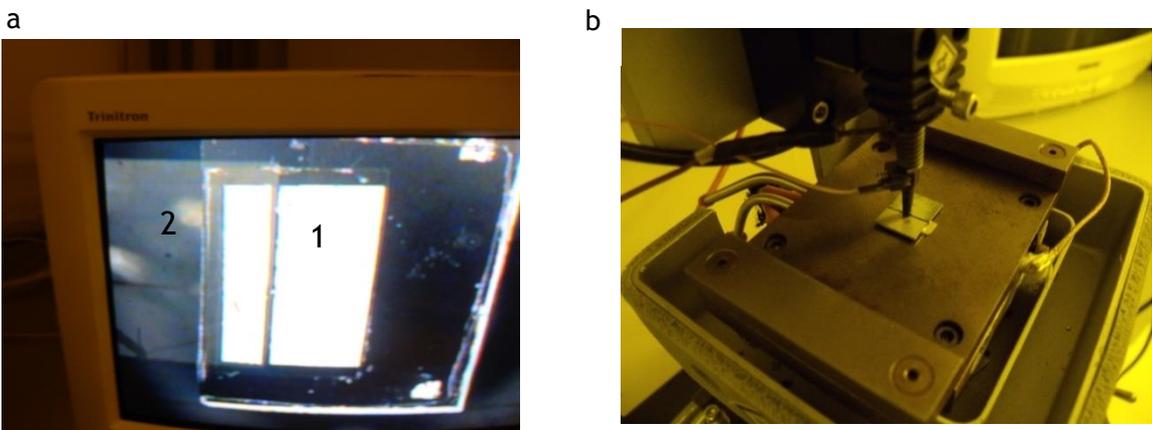


Figure 4.8: (a) Alignment of n-leg (indicated by 1) to the connector (indicated by 2) with the aid of two cameras and a CPU monitor (b) Optical image of the p- and n-leg connection after alignment. The Z-head positioner of the flip chip placement system was used to bond and hold the two legs in place, while allowing it to cool to room temperature.

4.1.5. Continuity Test

The final stage of the fabrication process involves the performance of a continuity test between the p- and n- leg via the connector. To obtain accurate measurements a 4-point probe measuring equipment (Figure 4.9) was used to measure the effective electrical resistance between the legs.

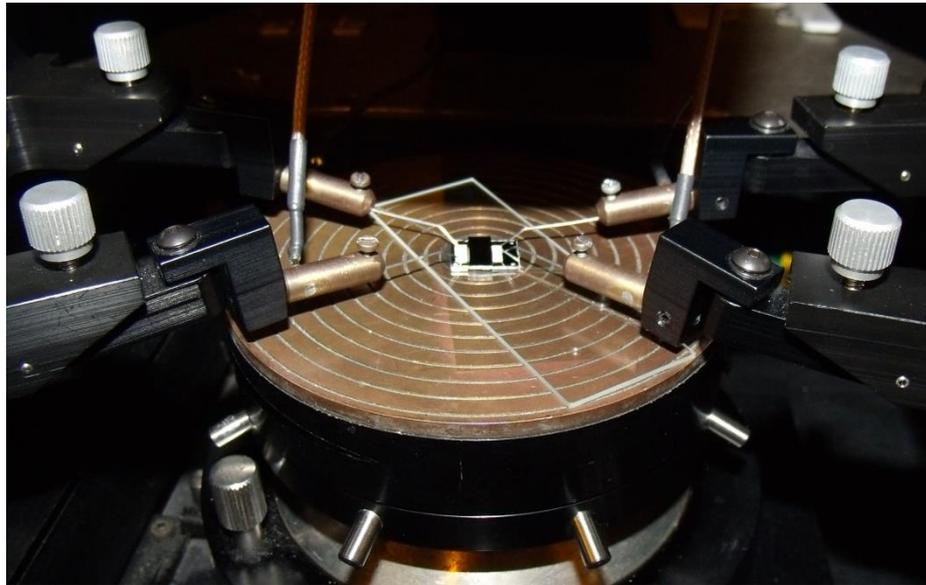


Figure 4.9: Four-terminal probe station used to check for continuity between the the p- and n- leg.

The four-terminal probe measurement is used for low resistance applications [79] and hence suitable for a continuity test. The principle of operation of a four-terminal probe is illustrated in Figure 4.10.

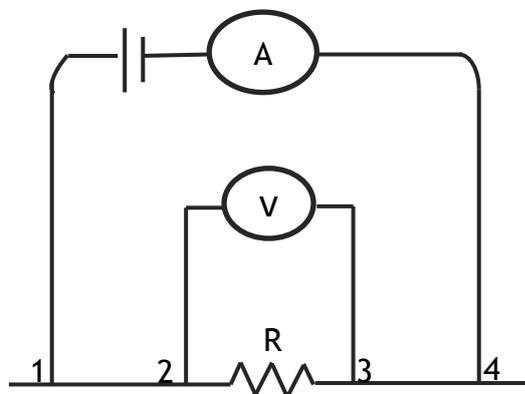


Figure 4.10: A 4-point terminal probe measurement to accurately determine the resistance, R between the voltage sensing connections 2 and 3. Current is supplied via 1 and 4.

4.2. Measurement of the power generating capacity of the Ge/SiGe-based TEG module

4.2.1. Measuring instrument

After fabrication of the Ge/SiGe TEG module, the next stage in the experiments involves measurement of the power generating capacity of the TEG module. The measurement process basically involves obtaining results of the Seebeck voltage for both open and closed circuit connections of the TEG module. Other electrical quantity such as the power density can be derived from the voltage measurements. The measuring instruments used are: Peltier heater, four-terminal probe instrument and commercial thermocouples (type-K).

- **Peltier heater:** in typical applications of TEG, waste heat is normally harnessed to heat up the hot-side of the TEG whereas the cold-side may be connected to a heat sink or allowed to maintain surrounding temperature. It is this temperature difference that produces the required voltage in the TEG. Hence, to simulate this effect in the fabricated TEG module, a Peltier heater is used to heat up the hot-side of the TEG while the cold side is exposed to air, initially at room temperature. A major challenge faced however, is the incorporation of a heat sink that can help maintain the cold side temperature of the device. This is because the size of the TEG module is very small compared to the available heat sink. The Peltier heater consists of a positive and a negative terminal (electric wires), several thermocouples and two ceramic plates. The terminals are connected to power supply and the thermocouples are embedded between the two ceramic plates (see Figure 4.11).

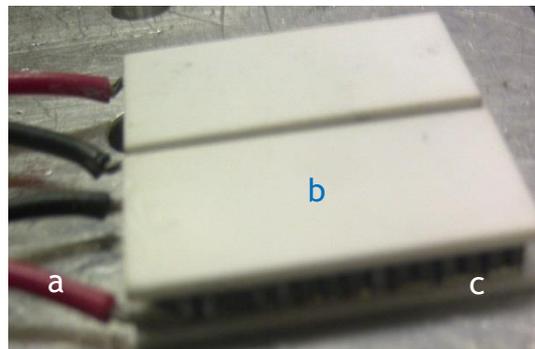


Figure 4.11: Two commercial Peltier devices: (a) electrical terminals (b) ceramic plates (c) thermocouples.

On application of current through the terminals, Peltier effect occurs in the thermocouples such that a uniform heat distribution is generated on one of the ceramic plates while the opposite plate becomes cold. The hot side of this heater is then used as the heat source to the TEG module. In the set-up used for this experiment, the Peltier device is much larger than the TEG module and this make it impractical to take advantage of the cold side of the device as a heat sink due to its weight. A smaller Peltier device may be appropriate to use as heat sink but one was not available in the course of this experiment.

- Four-terminal probe instruments: this is similar to the diagram described in Figure 4.9 and 4.10. This instrument is used mainly as a voltmeter to measure the Seebeck voltage generated from the TEG module for both open and closed circuit connections.
- Type-K thermocouples: two commercially available type-K thermocouples were used to monitor the temperature difference between the top and the bottom of the TEG module. The thermocouple operates within the range of -270 to $1,260^{\circ}\text{C}$ and is based on the Seebeck effect principle, whereby a voltage is generated when a temperature gradient is applied across two dissimilar conductors called thermocouples (e.g. chromel and alumel). The temperature - voltage relationship of the thermocouple is then calibrated for use as a thermometer.

Figure 4.12 (a) shows a type-K thermocouple that was already inbuilt to the multimeter while Figure 4.12 (b) shows the principle of operation of the thermocouple. The leads of the thermocouples were attached to the TEG, using kapton tape. Kapton tape was used because it can withstand temperatures up to 400 K

a)



b)

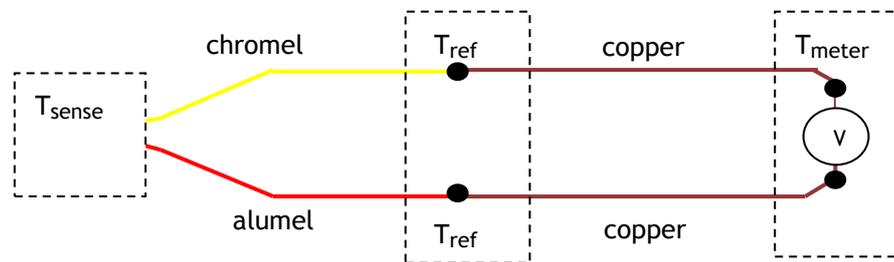


Figure 4.12: (a) Thermocouple (1) attached to a multimeter (2) (b) Principle of operation and internal circuitry of the thermocouple [80].

Figure 4.13 demonstrates the connection of voltage probes and thermocouples on the TEG module. It also shows the placement of the TEG module on the Peltier heater

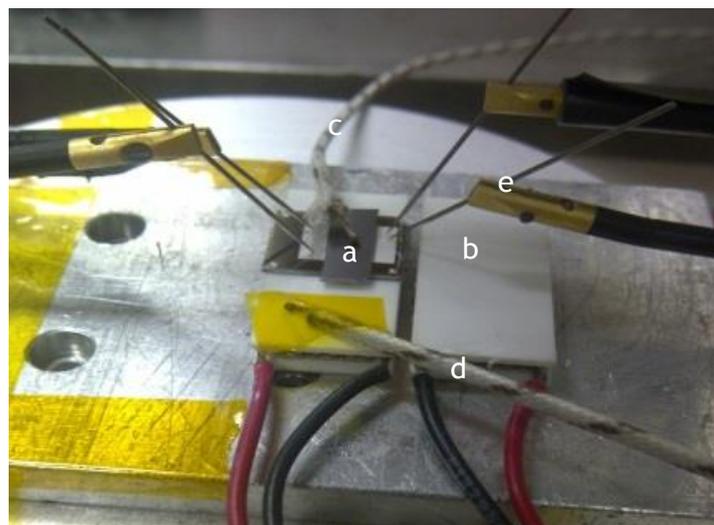


Figure 4.13: Image of the fabricated TEG module (a) placed on top of a Peltier heater (b). The image also shows the two thermocouples (c) and (d) used to monitor the temperature at the top and bottom surface of the fabricated device respectively, and the four-terminal measurement (e) used to measure the Seebeck voltage output.

4.2.2. Measurements in open and close circuit

The measurement set-up for the open connection involves connecting the TEG module directly to a voltmeter via the four-terminal probes. A temperature gradient is created between the top and bottom surface of the TEG module by placing one of its sides (i.e. the bottom) on the Peltier heater. A uniform temperature is created at the bottom of the TEG module while the top is exposed to ambient temperature. This creates a temperature difference across the p-/n- legs of the superlattice, which results to the generation of a Seebeck voltage.

The close circuit measurement set-up is similar to that of the open-circuit with the exception that a load resistance is connected across the TEG module. By connecting a load resistance across the TEG module the circuit becomes a close-circuit. Therefore, load voltage readings are obtained by connecting the voltmeter across the load resistance. In the experiments, a load resistance of 1.5 ohms was connected across the TEG module. This load was chosen simply because of its availability and closeness in value to the measured internal resistance of 1.2 ohms.

Estimation of temperature difference across the superlattice

Since it is difficult to directly measure the temperature across the p-/n- legs of the superlattice, an approximate estimate of the temperature difference can be obtained. Thus, Fourier's law of heat conduction was used to estimate the temperature difference across the superlattice ($\Delta T_{\text{superlattice}}$) for each temperature difference measured across the TEG module (ΔT_{meas}). The individual thermal conductivities that was used in the Fourier's calculation was obtained via material characterization technique described in Chapter 3 of this work and in references [6, 7]; with estimates of 5.5 W/mK for the p-type superlattice and 26.3 W/mK for the n-type superlattice.

The first step involves estimation of the total thermal resistances for the different layers that make up the TEG module; all the layers are connected thermally in series except the p- and n-legs which are connected thermally in parallel. Therefore the total thermal resistance of the device is estimated as:

$$Rth_{total} = Rth_{connector} + \frac{Rth_p \times Rth_n}{Rth_p + Rth_n}$$

where Rth_p and Rth_n comprise of the combination of thermal resistances from the superlattice, buffer layer, substrate and Ohmic contacts that make up the p-type and n-type materials respectively. The second step involves dividing the temperature differences measured (ΔT_{meas}) across the TEG module by Rth_{total} to obtain the total amount of heat input to the system:

$$Q_{total} = \frac{\Delta T_{meas}}{Rth_{total}}$$

The effective temperature difference across the superlattices of both the p and n-leg can then be obtained by multiplying the effective thermal resistances of the superlattice with Q_{total} [81]:

$$\Delta T_{superlattice} = Q_{total} \times \frac{Rth_{ps} \times Rth_{ns}}{Rth_{ps} + Rth_{ns}}$$

It is important to note that the temperature differences measured across the TEG module also accounts for the thermal contact resistances at the interface of the various layers. For ease of calculation, Matlab™ (version R20013a) software is used to generate codes that will calculate the $\Delta T_{superlattice}$ for each ΔT_{meas} . The generated matlab codes are shown in Appendix 1. Figure 4.14 (a) and (b) shows the estimated temperature difference across the superlattice for each measured temperature difference across the TEG module, for open and close circuit connections respectively.

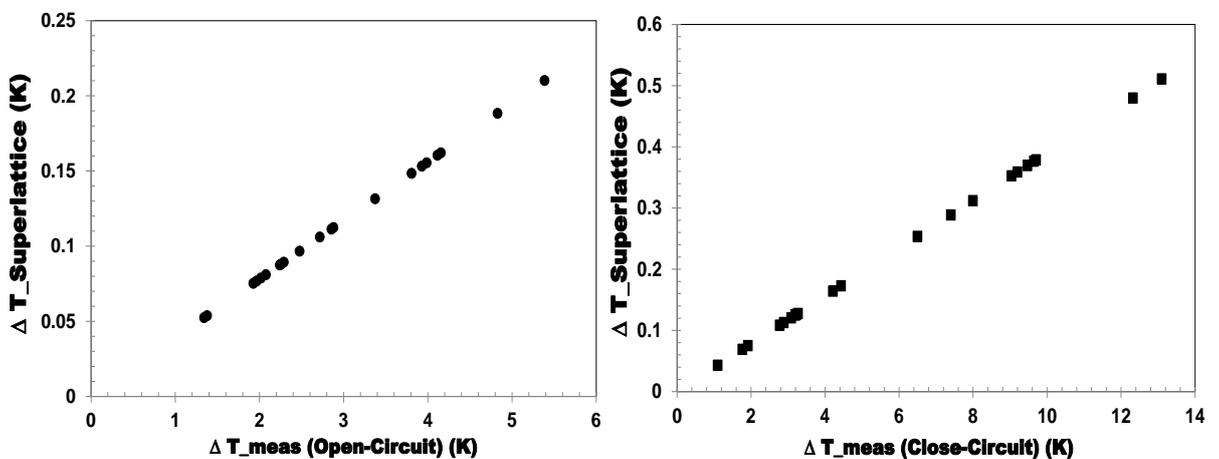


Figure 4.14: Estimated temperature difference across the superlattice versus measured temperature difference across the TEG module for (a) open-circuit and (b) closed-circuit.

From Figures 4.14 (a) and (b), it is observed that the temperature difference across the device and the superlattice is quite small. This limitation is due to the absence of a heat-sink to help maintain the temperature at the cold side of the TEG module. As the heat input to the TEG module increases the temperature of the cold side increases also, and this is not desirable. This makes the temperature difference across the legs of the superlattice to be smaller than expected. Another reason is that the thermal conductivities of both legs are not the same, with the n-leg having a thermal conductivity that has a high value of 26.5 W/mK as compared to that of the p- leg having a value of 5.5 W/mK.

A major flaw with the estimated temperature differences across the superlattice is that it is an average of the temperature difference across the p- and n-leg. In reality, this is not true because the thermal conductivities are different ($p = 5.5$ and $n = 26.5$ W/mK) and both have the same dimensions. However the information is still considered useful in the sense that it can be used to obtain a rough estimate of the effective Seebeck coefficient of the TEG module. Thereafter, Finite Element Method (FEM) will be used to evaluate a more accurate value of the effective Seebeck coefficient and this will be discussed in detail in the next chapter (5).

Measured voltages in open circuit

The measured open circuit voltage was plotted against $\Delta T_{\text{superlattice}}$ (Figure 4.15) with all the data points having an error less than 0.5%. The quoted error is obtained from the standard deviation of five (5) measurements. The regression model is produced from the experimental data and the intercept of the regression line was set at the origin (0, 0) even though the experimental data has an initial offset of (0.11, 0) from the origin. This offset can be attributed to the noise inherent in the measuring instrument. The Seebeck equation that was derived in Chapter 3 suggests the gradient of the regression model can be used to estimate the effective Seebeck coefficient.

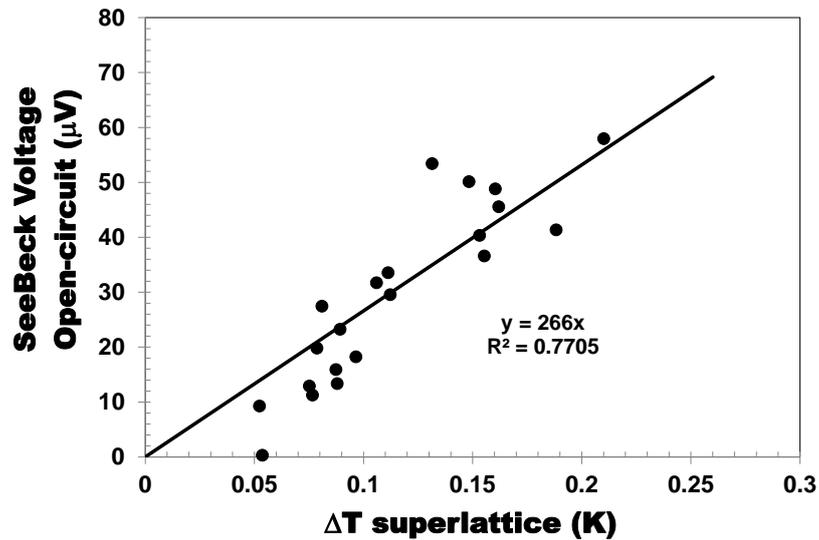


Figure 4.15: Measured Seebeck voltages in open circuit with regression line for estimating the effective Seebeck coefficient.

For open circuit connection a Seebeck coefficient of $266 \mu\text{V}/\text{K}$ was estimated from the regression model for the experimental measurements (see Figure 4.16). The R-squared value shows the closeness of the experimental data to the fitted regression model. An R-squared value of 0.77 indicates that the regression model can only account for 77% of the variance in the measured data points. The low voltage output observed is due to a low temperature difference across the p-leg and n-leg. The randomness of the experimental data points shows that the errors and disturbances in the system are not negligible because of the very low measurement values. Despite these flaws, the trend of the experimental data plotted in Figure 4.15 shows a casual pattern of increase in voltage with increase in $\Delta T_{\text{superlattice}}$.

Measured voltages in close circuit

Similarly, the measured load voltage (or Seebeck voltage in closed circuit) is plotted against $\Delta T_{\text{superlattice}}$ in Figure 4.16. Also shown in this figure is the regression model for the experimental measurements, and the R-squared value of the model is 0.9497.

From the regression model, the Seebeck coefficient for the close-circuit connection was estimated as $97 \mu\text{V}/\text{K}$. The closed-circuit connection gives a much lower estimate of the Seebeck coefficient compared to the open-circuit

connection, and appears to be less affected by the inherent sources of error in the fabrication process and measuring instruments. This observation can be explained in terms of circuit theory as presented in section 4.2.3.

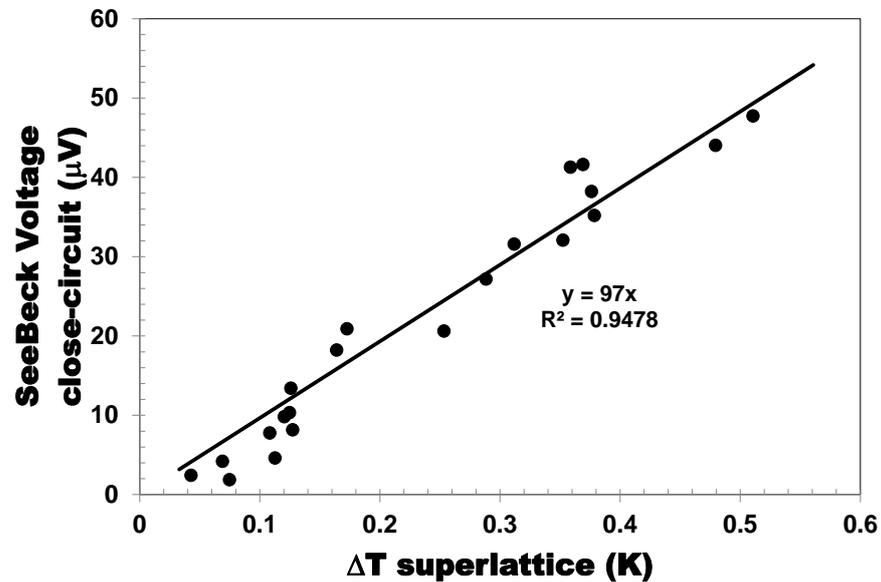


Figure 4.16: Measured Seebeck voltages with regression line for estimating the effective Seebeck voltage in closed-circuit.

Regression model and residuals

From Figures 4.15 and 4.16, the R-squared values are 0.77 and 0.9479 respectively. These numbers indicate that the regression models can only account for 77% variance of the data points in open-circuit and 94.79% in close-circuit. The residual plots shown in Figures 4.17 can be used to check if the observed errors (or residuals) are consistent with stochastic error analysis (i.e. unpredicted randomness of the residuals). If the residuals follow a predictable pattern then the regression model is inadequate, but when the residuals shows a random (stochastic) pattern then the regression model is good.

From Figure 4.17, it can be observed that the residuals are stochastic with a maximum deviation of 18 μV for open circuit and 7 μV for close-circuit voltages. This means that the regression models can be considered good for predicting the response of the TEG module. Also, the estimates of the Seebeck coefficients for open- and close-circuits can be written as $266 \pm 18 \mu\text{V/K}$ and $97 \pm 7 \mu\text{V/K}$ respectively.

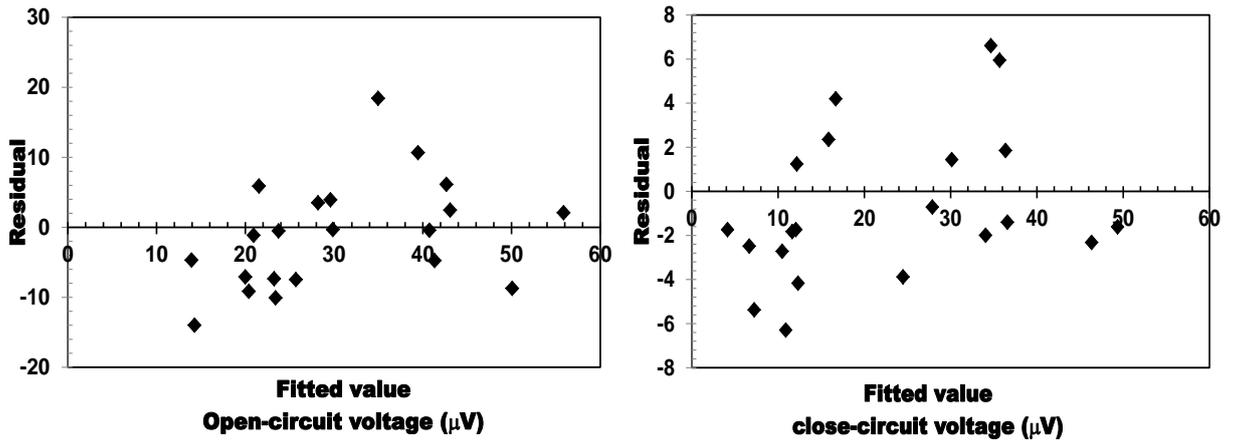


Figure 4.17: Residuals from regression models of (a) open-circuit and (b) close-circuit voltages.

4.2.3. Circuitry of the TEG connected to a load.

A TEG is basically an open circuit that has a voltage source, V_{oc} , and an internal resistance, r , connected electrically in series with it [82]. When a load resistance, R_L is connected across it, the circuitry is closed and load current flows through it. From the circuitry in Figure 4.18, the relationship between the open circuit voltage, V_{oc} , and load voltage, V_L , is obtained as follows:

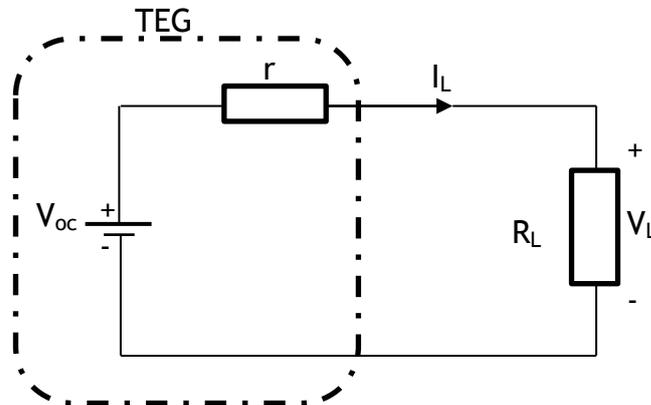


Figure 4.18: Closed circuitry describing the connection of TEG to an external load, R_L .

$$V_L = I_L R_L \quad (4.1)$$

and according to Kirchoff's voltage law,

$$V_{oc} = I_L r + V_L \quad (4.2)$$

Substituting equation (4.1) into equation (4.2),

$$V_{oc} = I_L (r + R_L) \quad (4.3)$$

Again, from Equation (4.1), $I_L = V_L/R_L$. Therefore, substituting this expression in Equation (4.3), and making V_L subject of the formula,

$$V_L = V_{oc} \times \frac{R_L}{r + R_L} \quad (4.4)$$

Assuming the internal resistance, r , and the external load resistance, R_L , are equal (i.e. the impedance is matched) and there are no electrical losses (or contact resistances), then

$$V_L = \frac{V_{oc}}{2} \quad (4.5)$$

Equation (4.5) shows that the theoretical load voltage of the close-circuit is 50% of the open-circuit voltage for impedance matched loads. By comparing Figures 4.15 and 4.16, the load voltage is estimated to be 36.3% of the open-circuit voltage. The drop in load voltage from the theoretical prediction can be attributed to additional resistances introduced by the leads of the probes that connect the load resistance to the TEG module. Further analysis can be carried out to evaluate the contact resistance in the circuit (i.e. additional resistance occurring at the interface of the connections). For this reason, Equation 4.2 can be modified as shown.

$$V_{oc} = I_L r + I_L R_{contact} + V_L \quad (4.6)$$

The gradients of the regression models in Figures 4.16 and 4.17 show that

$$V_{oc} \cong 2.75V_L \quad (4.7)$$

Substituting Equation (4.7) into Equation (4.6) gives:

$$2.75V_L = I_L r + I_L R_{contact} + V_L \quad (4.8)$$

which simplifies to

$$1.75V_L = I_L r + I_L R_{contact} \quad (4.9)$$

Substituting Equation (4.1) into Equation (4.9) and dividing through by I_L gives

$$1.75R_L = r + R_{contact} \quad (4.10)$$

Upon substituting $R_L = 1.5 \Omega$ and $r = 1.2 \Omega$ the contact resistance for the experiment is estimated as $R_{contact} = 1.425 \Omega$. This estimate of the contact resistance is considered to be reasonable as it only causes a drop in the load voltage by 13.7% (i.e. $50 - 36.3\%$) from the theoretical prediction for an impedance matched connection.

4.2.4. Determination of power generating capacity of Ge/SiGe-based TEG module.

Thermoelectric generators are usually designed to generate power that can energize an electrical device such as a light bulb or sensor. The generating power, P_G , of the TEG is defined by Equation (4.11) below.

$$P_{out} = V_{oc}I - I^2r \quad (4.11)$$

or

$$P_{out} = \frac{V_L^2}{R_L} \quad (4.12)$$

This power can be maximized if the internal resistances and load resistances are impedance matched (i.e. $r = R_L$). In the case of the fabricated Ge/SiGe-based TEG module the power transferred to the load (i.e. P_{out}) can be obtained directly from the measured closed circuit voltage of Figure 4.16 and using Equation (4.12).

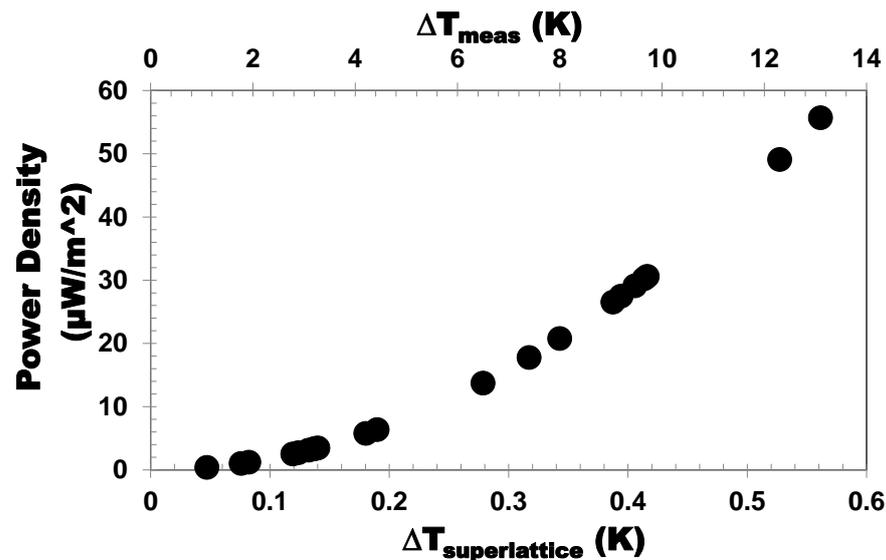


Figure 4.19: Power per unit area transferred to the load of 1.5Ω

The total area of the p-leg and n-leg is 0.224 cm^2 . Therefore, the power density (i.e. P_{out} per Area) of the fabricated Ge/SiGe-based TEG module can be obtained as shown in Figure 4.19. The figure shows that an increase in $\Delta T_{\text{superlattice}}$ will result to an increase in the power output of the device. The maximum power density of $58 \mu\text{W}/\text{m}^2$ was achieved at $\Delta T_{\text{meas}} = 13.1 \text{ K}$ and a corresponding $\Delta T_{\text{superlattice}} = 0.51 \text{ K}$.

4.2.5. Determination of thermal efficiency of Ge/SiGe-based TEG module.

The thermal efficiency of a TEG is the ratio of the power output generated to the external heat source applied to the system as described by Equation (4.13)

$$\eta_{th} = \frac{P_G}{Q} \quad (4.13)$$

Heat measurements are usually difficult to obtain. Hence, an approximate factor called thermal efficiency factor is usually used in estimating the efficiency of TEGs. The thermal efficiency factor is given as [10]:

$$\varphi = \frac{P_G}{A_G \Delta T_{meas}^2} = \frac{P_d}{\Delta T_{meas}^2} \quad (4.14)$$

where P_d is the power density. This implies that the thermal efficiency can be estimated from the gradient of a plot of power density against the square of the temperature difference across the TEG module.

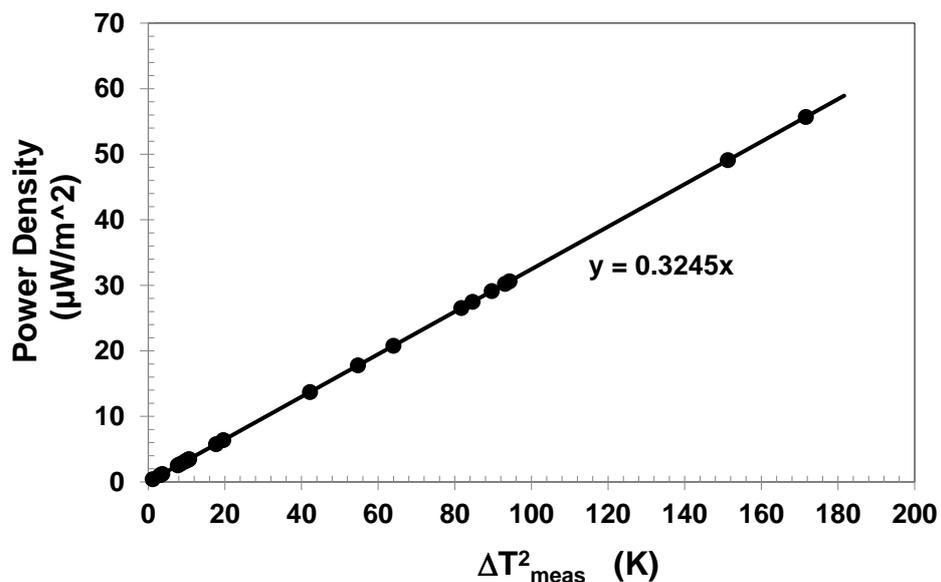


Figure 4.20: Determination of the Thermal efficiency factor for fabricated Ge/SiGe-based TEG module.

From Figure 4.20, a linear plot is obtained and the gradient of that plot gives the thermal efficiency factor of $0.3245 \mu\text{W}\cdot\text{m}^{-2}\cdot\text{K}^{-2}$ (or $3.245 \times 10^{-5} \mu\text{W}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$) for the fabricated Ge/SiGe-based TEG module. The linearity of the plot suggests that increasing the amount of heat, Q , supplied to the system does not necessarily improve the thermal efficiency of the device. However, the thermal efficiency of the device may be improved upon by using a more efficient material, for fabricating the device.

Chapter Summary

In this chapter, the micro fabrication of a TEG module using the Ge/SiGe material is discussed. A step-by-step description of the fabrication processes used in building the device is presented. The basic fabrication processes include: photolithography, etching, metallisation, bonding and continuity test. The generating capability of the fabricated device was tested using the following measuring instruments: Peltier heater, four-terminal probe instrument and commercial thermocouples (type-T).

The Peltier heater is required for raising the temperature at the hot-end of the TEG while the cold side is exposed to air, initially at room temperature. The TEG module is made to sit on top of the Peltier heater, which heats up the device from the bottom upwards. This approach was specifically chosen for two main reasons: (1) to ensure that the Seebeck voltage is generated only from the TEG module, thus avoiding possible electrical contributions from an external source; (2) to ensure uniform heat distribution throughout the device. A major limitation with this approach is that the set-up makes it difficult for a heat sink to be incorporated. This is because the size of the TEG module is very small compared to the available heat sink. Thus, it is not feasible to place a large heat sink on top of a very small device.

The four-terminal probe instrument is used for measuring the Seebeck voltages in open and close circuit, while the commercial thermocouples are used for taking temperature measurements for a corresponding Seebeck voltage. Based on the experimental results obtained, the power density and thermal efficiency factor of the device were obtained. The results obtained suggest the need for a more efficient thermoelectric material in building the TEG module. Chapter 6 of

this work presents a second experiment that was conducted using a more efficient material to fabricate the Ge/SiGe TEG module. Thus, it will be seen that the utilization of a more efficient material does help to improve the performance of the TEG module.

Finally, the results presented in this chapter can be used to validate a Finite Element model for the Ge/SiGe-based TEG module, and this endeavour is the subject of Chapter 5.

5. Finite Element Modelling of Ge/SiGe Thermoelectric Generators

This chapter discusses the development of a Finite Element Model for the Ge/SiGe-based TEG module using Comsol Multiphysics® (version 4.3b). The FE approach is based on the experimental conditions discussed in Chapter 4. Two separate FEMs are developed, one for open circuit and the other for close circuit, so that the simulated FE results can be compared with the experimental results. The input parameters used for the FEM include the experimental measurements of the top and bottom surface temperatures, internal resistance and open circuit Seebeck coefficient. Also, the contact resistances obtained from circuit theory analysis are used as inputs in the FEM.

A major limitation of the experiment discussed in Chapter 4 is the absence of a heat sink to dissipate the heat at the cold side of the TEG module. Another issue is that a material of low efficiency was used to build the TEG module used for the experimental test. However, the experiment reported in Chapter 4 forms the basis of building a FEM for further analysis, and is used to validate the FEM. The FEM is used to simulate the effect of a heat sink and to investigate the effect of using a more efficient material on the output performance of the TEG module. It also shows that having the external load resistance to be equal to the internal resistance does give the optimum performance of the device.

In order to evaluate the FEM of the Ge/SiGe TEG module, the performance of the FEM (i.e. load current, open circuit voltage, power output and efficiency) is compared to the theoretical maximum performance determined using the analytical formulation of Wu [54]. The purpose of the comparison is to determine the closeness of the output performance of the FEM to the theoretical maximum performance. An advantage of the FEM is that it reduces the number of prototypes and experiments that have to be run when designing and optimizing the TEG module. Secondly, the FEM allows for simulation of the TEG module for different real-world conditions that would be expensive and time-consuming to investigate experimentally. It also gives insight to the temperature and voltage distribution of the TEG module under varying operating conditions.

The development of the FEM in Comsol Multiphysic[®] involves the following main stages:

1. Geometry design of the TEG-module. This stage is straight-forward as it only requires a 3-D drawing of the fabricated TEG module.
2. Specification of material properties and boundary conditions. The material properties used in the experiments are used for the FEM and the Dirichlet boundary condition is applied in the FEM.
3. Specification of the governing equations that describe the thermoelectrics effects of the TEG.
4. Meshing (or discretization) of the TEG module.
5. FE simulation and analysis of results.

5.1. Geometry design of Ge/SiGe-based TEG module

The p-type and n-type material are connected together by a connector as shown in Figures 5.1 (a) and (b). All dimensions in Figures 5.1 (a) are in centimetres while Figures 5.1 (b) shows an expanded view of the different layers. The labels (a) – (f) in Figure 5.1 (b) represent:

- a) 0.6 μm of the unetched superlattice.
- b) 0.2 μm of Ohmic contact (99% Ag/1% Sb for n-type).
- c) Two layers of 0.7 μm aluminium; one deposited on the legs (i.e. both p- and n-type), the other deposited on the connector.
- d) Two layers of 2 μm indium; one deposited on the legs, the other deposited on the connector.
- e) 0.1 μm layer of insulating nitride (Si_3N_4) for preventing electrical leakages to the connector substrate.
- f) 530 μm layer of Si substrate that is used in forming the connector.

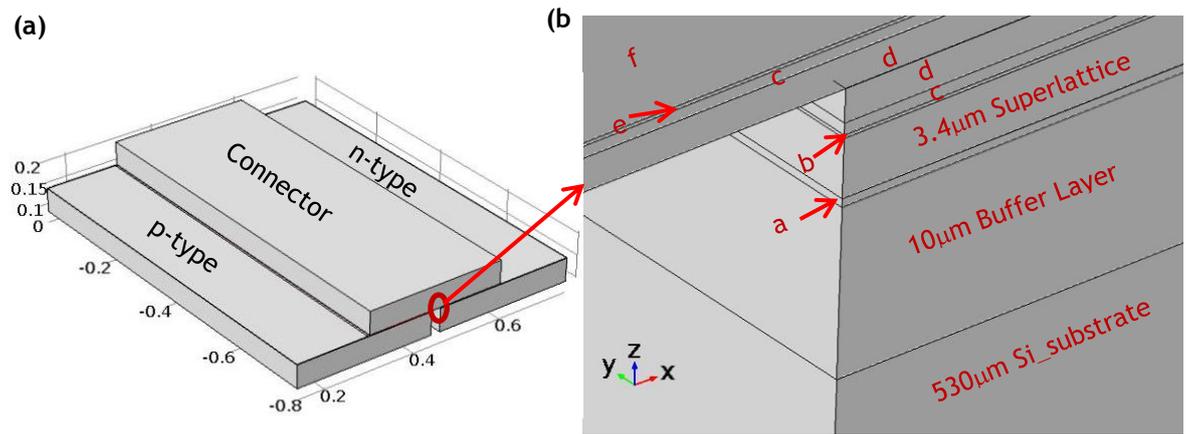


Figure 5.1: (a) Geometrical design representing the Ge/SiGe TEG-module (b) Expanded view of the different layers and connections labelled a-f.

5.2. Material properties and boundary condition specifications

5.2.1. Thermoelectric Material properties

The thermoelectric material properties required for the FEM are the thermal conductivity, Seebeck coefficients and electrical conductivity.

Thermal conductivity, κ

Thermal conductivity is the measure of a material's ability to conduct thermal energy through a solid medium, in the presence of a temperature gradient across its surfaces. The higher the thermal conductivity, the more the thermal energy conducted through the medium and the less the temperature difference generated across the surface of the material for a given heat input. In thermoelectricity, a large temperature difference is required based on the Seebeck effect principle. Hence, a low thermal conductivity is desirable in order to minimize the conduction of thermal energy from the hot region to the cold region. This will aid the generation of a high Seebeck voltage. The measurement technique discussed in chapter 3 of this work and references [6, 7] was used to measure the κ properties of the Ge/SiGe for both p and n-type materials. A value of 5.5 W/mK for p-type and 26.5 W/mK for n-type of the respective superlattice layers were obtained.

Seebeck coefficient, α

The Seebeck coefficient refers to the induced voltage per temperature difference across the material. Based on the measurement technique of references [6, 7], the individual Seebeck coefficient for p- and n-type material was recorded as: 112 $\mu\text{V/K}$ and $-269 \mu\text{V/K}$ respectively. However, the coupling of the p and n type material to form a TEG module resulted to a significant voltage drop so that the effective Seebeck voltage of $180\mu\text{V/K}$ was estimated. This drop in voltage is as a result of the thermal and electrical contact resistances at the bonding joints and at the interfaces of the various layers that make up the TEG module. During the experimental measurements, an effective Seebeck value of $180\mu\text{V/K}$ was obtained from the fabricated TEG module. A detailed discussion of how this value was estimated is discussed later on in Section 5.6.1 of this work. Based on the assumption that most of the voltage output generated emanates from the superlattices of the p and n-type material, an equal value of $90\mu\text{V/K}$ was specified for each of the materials. Since the legs are connected electrically in series, according to theory [1], the Seebeck values of each of the legs should add up.

Electrical conductivity, σ

The electrical conductivity is a measure of the ease of flow of the valence electrons in the material. The internal resistance of the TEG is dependent on its electrical resistivity (or conductivity). A four terminal probe can be used to measure the internal resistance and hence the effective electrical conductivity of the TEG module [79]. In this research work, the measured internal resistance of 1.2Ω was obtained for the TEG module. Here, it was assumed that this value included possible contributions from the p- and n- type superlattices, buffer layer, silicon substrate, Al connectors, indium bond and internal contact resistances at the interfaces. At this stage however, it is difficult to estimate the exact electrical conductivity for the superlattice layer, which is the layer of interest, as well as the internal contact resistances. However, an approximate estimate of the effective electrical conductivity for the p-leg and n-leg of the TEG module can be obtained by estimating the resistance contribution from the silicon substrate, buffer layer and superlattice. It can be assumed that the other resistance contributions are negligible due to their small thicknesses as compared with that of the silicon substrate, buffer layer and superlattice (see

5th column of Table 5.1). A rough estimate of the effective electrical conductivity is given below:

Total area of the p- and n-leg: $A = 2 \times 0.14 \times 0.8e^{-4} m^2$.

The measured resistance: $r = 1.2 \Omega$.

The total thickness (i.e. Si substrate + buffer layer + superlattice) is equal to $543.5\mu m$.

The effective electrical conductivity, which includes the superlattices, buffer layer and silicon substrate is

$$\sigma_{effective} = \frac{L}{(r * A)} = 20.22 \text{ S/m} \quad (5.1)$$

where L in this case is the total thickness of $543.5\mu m$.

Derivation of the formula for effective electrical conductivity

In order to set a value for each of the legs in the FEM simulation, it is of paramount importance to know how the electrical conductivities of the p- and n-legs are related. Since the legs are connected electrically in series: the electrical resistance for a series combination is given as [84]:

$$R_{total} = R_p + R_n \quad (5.2)$$

where by:

$$R_p = R_n = \frac{\rho L}{A} = \frac{L}{\sigma A} \quad (5.3)$$

the area, A and length L, of both p- and n- legs were fabricated to have equal dimensions. Thus, substituting Equation (5.3) into Equation (5.2),

$$\frac{1}{\sigma_{effective}} = \left(\frac{1}{\sigma_p} + \frac{1}{\sigma_n} \right) = \frac{1}{20.22 \text{ S/m}} \quad (5.4)$$

Based on Equation 5.4, an electrical conductivity of 40.44 S/m is estimated for each of the legs. It therefore implies that each of the legs will have an electrical conductivity that falls within the range of $1 - 40.44 \text{ S/m}$. This is a far cry from the measured values of 4099 S/m for the p-type material and 9400 S/m for the n-type material, which were measured using the material characterization technique of reference [6].

A major reason for this discrepancy is that during the course of this research work, a high electrical leakage inside the substrate was observed. The effect of this leakage in the thermoelectric material will become more pronounced when it is coupled into a TEG. This means that the combined effect of coupling a p and n material will reduce significantly as most of the current will drain into the substrate.

Another major reason is that the effect of the leakage was not taken into consideration in the calculation of the sigma value for the individual material. Hence there is a possibility of the sigma values to be overestimated during material characterization.

Moreover the addition of the indium bond for the purpose of coupling the p- and n-type materials will introduce an oxide layer and hence increase the contact resistance. Consequently the power output of the TEG module will reduce significantly. Minimizing these effects would help to an improved electrical conductivity and consequently improve the performance of the TEG module.

This deviation is relevant to this work because it helps to explain the reason for the low power output observed experimentally (refer to Figure 4.19 of Section 4.2.4). Recall that the power factor (p.f) is related to the electrical conductivity by $p.f = \alpha^2 \sigma$

At this stage, it is difficult to state an exact value of electrical conductivity for each of the legs because of the rough estimation performed above and because there could be additional contact resistance contributions that are not known. However, the estimation does show that the increased resistance due to the bonding of the two legs will have a significant effect on the output results. A comparison of the output results affected by the contact resistances and that without the effect of the contact resistances is performed later on, in Section 5.82 of this chapter.

Therefore, the stated values used in the FEM simulations for the thermal conductivity, Seebeck coefficient and electrical conductivity of the Ge/SiGe-based TEG module, are summarised in Table 5.1.

Table 5.1: Material properties used in the FEM simulations

Material type	Thermoelectric material properties			Dimensions
	α ($\mu\text{V/K}$)	κ (W/mK)	σ (S/m)	Height[nm]
Nickel	-18 [20]	90.7 [67]	13.8×10^6 [67]	200
Silver	2.4 [20]	429 [67]	61.6×10^6 [67]	200
Aluminium	-1.5 [20]	237 [67]	35.5×10^6 [67]	700
Indium	6.5 [20]	81.6 [67]	11.9×10^6 [67]	2000
Ge/SiGe superlattice (p-type)	90	5.5	-1 -40.44	3500
Ge/SiGe superlattice (n-type)	90	26.5	-1 -40.44	3500
SiGe Buffer (p/n)	1	20 [68]	1	10000
Si substrate (p/n)	1	155 [67]	1	530000
Si ₃ N ₄ insulator	1	20 [67]	1	100

The Seebeck coefficient and electrical conductivity of the buffer layer and silicon substrate were given arbitrary values of 1 S/m respectively. In Comsol Multiphysics®, a value of 0 cannot be used for the electrical conductivity otherwise the results of the simulation will not converge. Also, with respect to both the Seebeck voltage and electrical conductivity, some leakage currents were observed in the buffer layer and Silicon substrate during the course of fabrication. Hence, the unity value helps to account for these leakages

5.2.2. Boundary conditions

Boundary conditions are mathematical expressions of the thermal (and/or electrical) conditions at the boundaries or surfaces of the problem domain [81]. In the present FEM, Dirichlet boundary conditions are applied at the following boundaries: the voltage at the bottom of the p-leg is set to ground (i.e. $V_0 = 0$), while the temperatures at the top and bottom surface of the TEG module are set to the measured temperatures, T_c and T_h respectively. Figure 5.2 shows the set position for the boundary conditions.

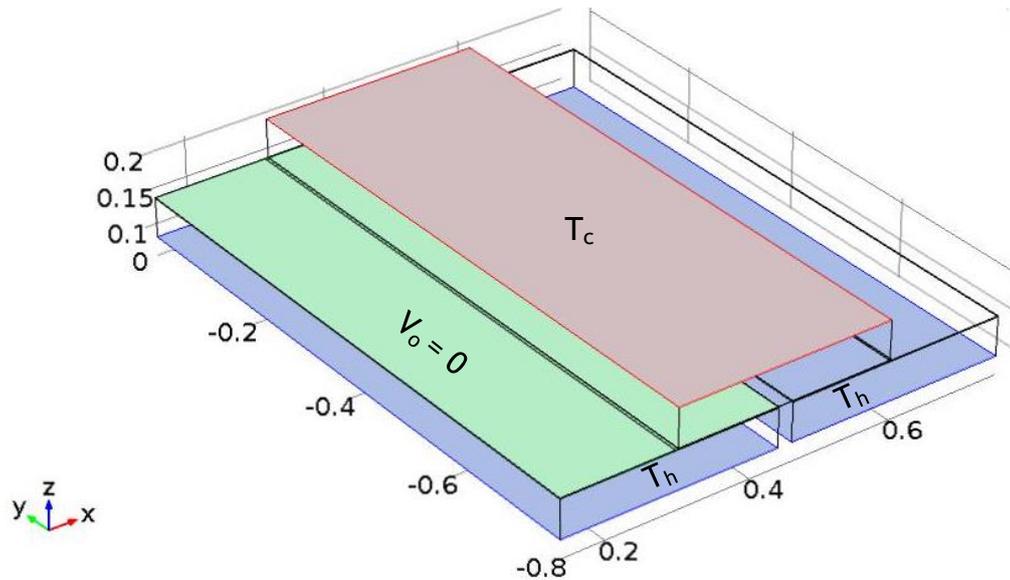


Figure 5.2: set boundary conditions for FE simulation of the TEG module.

5.3. Governing Equations

The governing equations used to model the TEG module are based on the heat flow equation given by:

$$\rho C \frac{\partial T}{\partial t} \cdot u + \nabla \cdot q = Q \quad (5.5)$$

and the continuity of electric charge equation given by:

$$\nabla \cdot \left(J + \frac{\partial D}{\partial t} \right) = 0 \quad (5.6)$$

which are coupled by the set of thermoelectric equations (Equations 5.7 and 5.8)

$$J = \sigma(E - \alpha \cdot \nabla T) \quad (5.7)$$

$$q = \pi J - \kappa \nabla T \quad (5.8)$$

A detailed explanation of these equations has been given in Section 2.5.2 of Chapter 2.

5.4. Meshing of the TEG Module:

The final stage in developing the FEM is the meshing or discretization of the TEG module. Both tetrahedral and swept meshes are used to discretize the TEG module. The tetrahedral mesh was implemented first to mesh the Ohmic contacts; thereafter, a swept mesh was used to transfer the meshed pattern to the remaining parts of the module. The significance of the swept mesh is that it helps to reduce the number of mesh elements and consequently, decreases the processing time, without affecting the accuracy of the results.

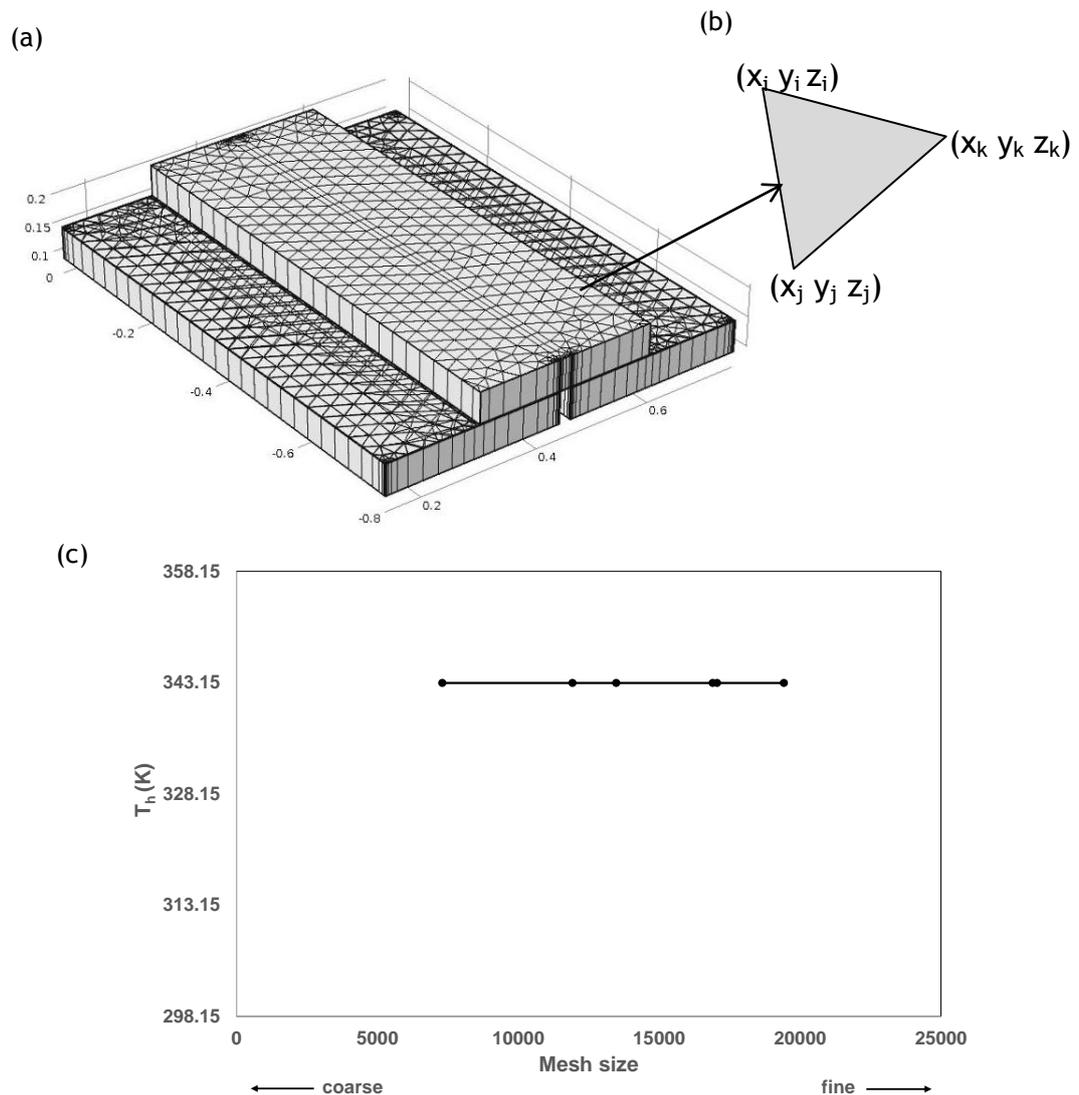


Figure 5.3: (a) Meshed diagram for FEM of Ge/SiGe-based TEG (b) Expanded view of a single element with its coordinate vertices. (c) Evaluation of mesh dependency of result

A total of 15,972 tetrahedral elements were used to discretize the TEG module (see Figure 5.3(a) and (b)). Also the mesh sizes were varied between coarse and fine meshing and the results remained relatively the same with an insignificance

deviation of $< 0.6\%$. Coarse meshing has fewer elements than fine meshing and shortens computational time. Domain elements is used to represent the mesh size (refer to Figure 5.3 (c))

The FE software (COMSOL Multiphysics®) has an inbuilt function that formulates the equilibrium equations for the individual elements shown in Figure 5.3 (a). A system of equations based on the nodal coordinates of each element is generated and solved. Hence, an approximate solution of the governing equations (described in section 5.3) is obtained.

Figure 5.3 (c) shows the mesh dependency of the hot side temperature to be uniform for the specified range of mesh sizes. This is an indication that the subsequent results obtained from the simulations are accurate.

5.5. FE Simulation and Results

The FEM can be used to generate a number of results including temperature profiles, open and close circuit voltages, load current, heat transfer and output power of the TEG device. Other results such as efficiency and power density can be derived from the aforementioned results. The temperature profile between the top and bottom surfaces is presented in Figure 5.4(a) and the corresponding open circuit voltage is presented in Figure 5.4 (b). A legend on the right of each of the figures shows the magnitudes of the temperature and voltage distribution. For the temperature and voltage distributions the red colour represents the highest value while the blue colour the lowest values. The colours between the blue and the red represent magnitudes between the lowest and highest values. The close circuit voltages are obtained when an external resistance is connected across the device. This was achieved in the FEM by specifying the resistance value at end of the voltage profile (Figure 5.4b). The effect of connecting an external resistance is a drop in the voltage output.

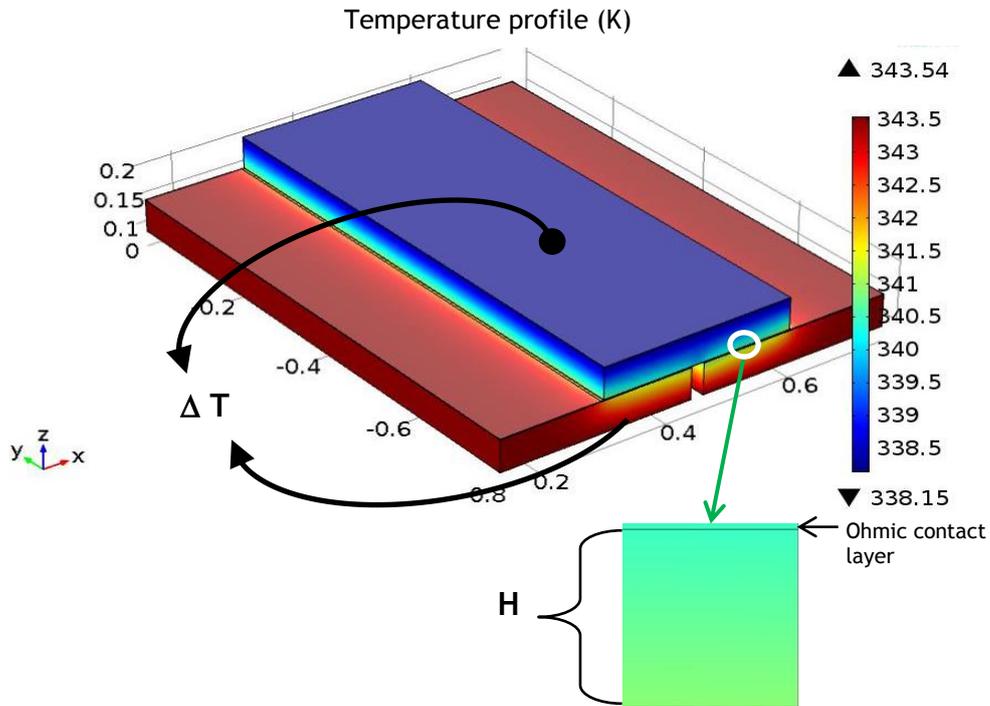


Figure 5.4(a): Temperature distribution for $\Delta T_{\text{meas}} = 5.3\text{K}$; The arrows indicate where the temperature measurements were taken. H represents height of superlattice.

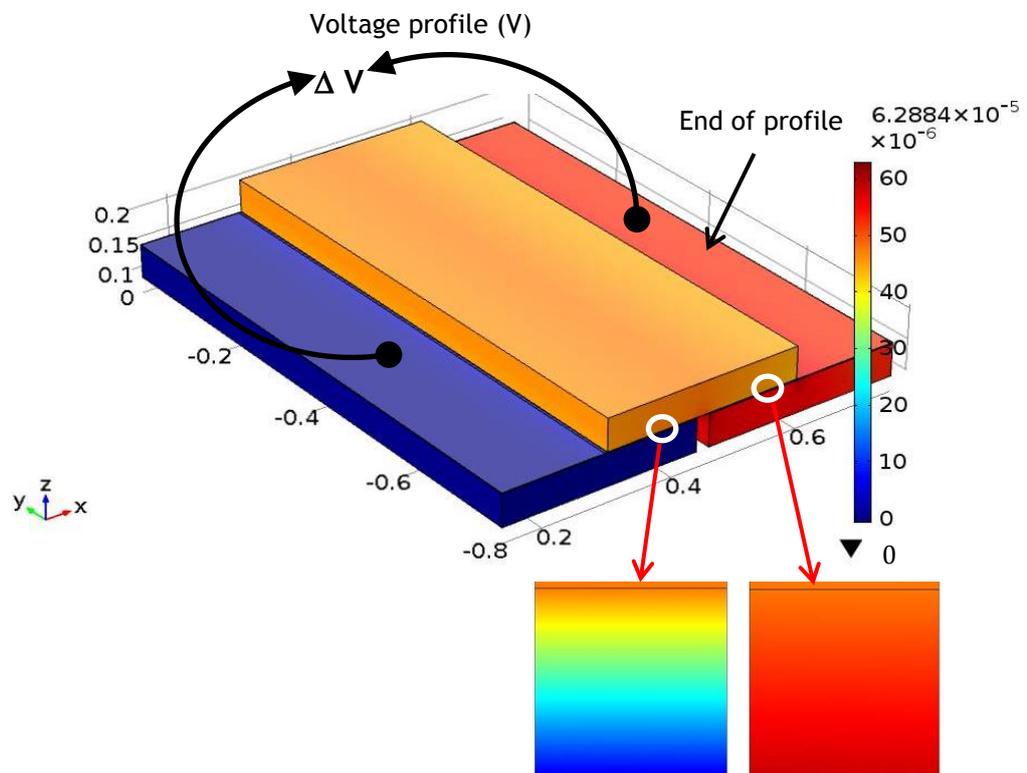


Figure 5.4(b): Corresponding voltage distribution (in open circuit). The arrows indicate the positions where the voltage measurements were taken.

5.6. Validation of FEM with experimental results

The experimental measurements discussed in Chapter 4 are used to validate the FEM for both open and close circuit connections. The values of the Seebeck coefficient estimated from experiment are used as an input parameter for both open and close circuit FEM. The load resistance and the estimated contact resistance (that was obtained based on circuit theory) are used as input for the close circuit FEM, while all other input parameters remain the same for both open and close circuit FEMs.

A parametric study was conducted for different Seebeck coefficients in order to determine the Seebeck coefficient that yields voltage outputs that closely match the experimentally measured voltages. Since the Seebeck coefficient is a material property, it is expected that the value of the Seebeck coefficient that produces simulated voltages closely matching the experimental voltages in open circuit connection, should also produce simulated voltages that match the experimental voltages in close circuit connection. This way, the FEM estimate for the Seebeck coefficient of the Ge/SiGe is validated and is used for further analysis.

5.6.1. Comparison of Seebeck voltages in open circuit

First, the experimentally measured open circuit voltages is compared with the simulated open circuit voltages for $\alpha = 265.91\mu\text{V}/\text{K}$. Recall from section 4.22 that $\alpha = 265.91\mu\text{V}/\text{K}$ is an estimated value based on the assumption that the temperature difference across the p-leg is the same as that for the n-leg. The regression model of the experiment data is used rather than the data points and ΔT_{meas} is used rather than $\Delta T_{\text{superlattice}}$, for ease of comparison and uniformity.

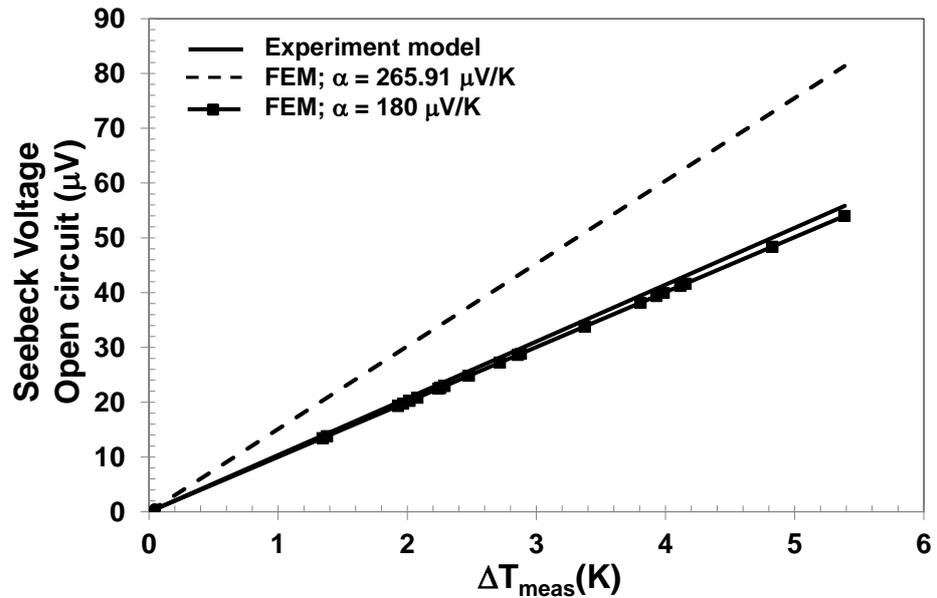


Figure 5.5: Comparison of simulated and experimental measured open circuit voltages.

When a Seebeck coefficient of $265.91 \mu\text{V/K}$ was used in the FEM of the TEG module the simulated voltage outputs were found to be higher than the corresponding voltages estimated from experiment (see Figure 5.5). From parametric studies, conducted by varying the Seebeck coefficient of the TEG module, it was observed that a Seebeck coefficient of $180 \mu\text{V/K}$ produced simulated voltage outputs close to the corresponding voltages estimated from experiment (see Figure 5.5). Therefore, a percentage difference of 32.3% is obtained between the Seebeck coefficient of $265.91 \mu\text{V/K}$, which was estimated from the regression line of Figure 4.15, and the FEM Seebeck coefficient of $180 \mu\text{V/K}$. The reason for this discrepancy is that the FEM accounts for the fact that $\Delta T_{\text{superlattice}}$ for the p-leg is different from that of the n-leg. On the other hand, the analytic estimation is based on the assumption that both the p-leg and n-leg have the same $\Delta T_{\text{superlattice}}$ and the latter is estimated using an effective value obtained from Fourier's law of heat conduction (see Section 4.2.2 for details). The FEM approach is considered to be more realistic because the two legs have different thermal conductivities and should therefore produce different temperature difference. Figure 5.6 shows a comparison of both the analytical and simulated results for the temperature differences across the superlattice of the p- and n-leg.

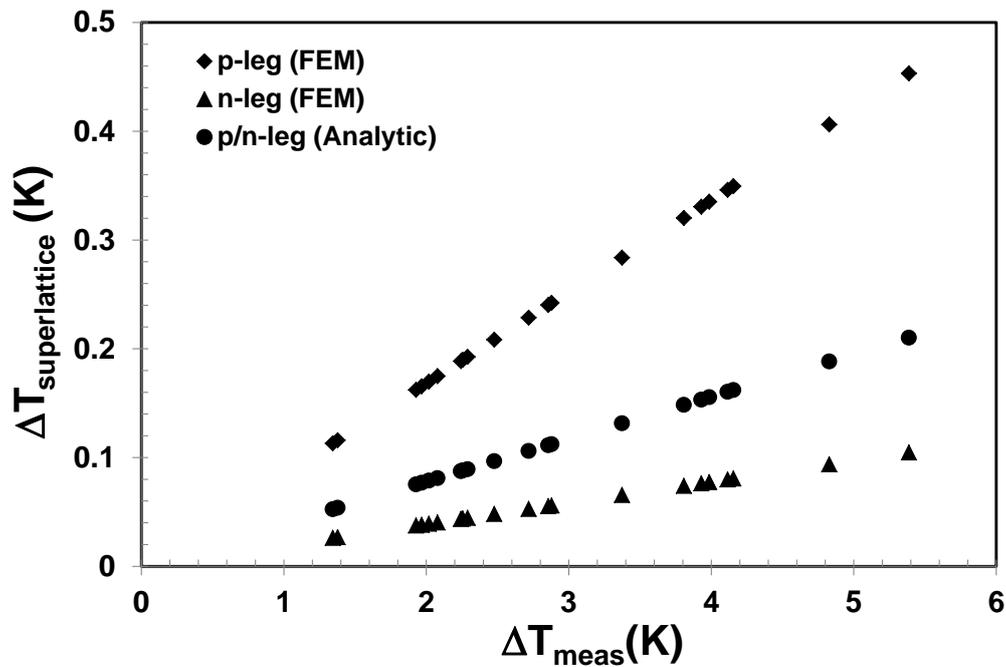


Figure 5.6: Comparison of analytical and FEM approach for estimating the temperature differences across the superlattice of the p- and n-leg.

The results presented in Figure 5.6 are independent of both open and close circuit connections. As earlier explained, it is the temperature difference that generates the voltages based on the Seebeck effect. It is observed that the p-leg has a higher temperature difference compared to the n-leg.

The analytical estimates based on Fourier's law, gives effective temperature differences that lie between the corresponding simulated values for the p-leg and n-leg. Since the FEM accounts for different temperature difference for the p-leg and n-leg, the Seebeck value of $180\mu\text{V/K}$, which produced simulated voltage outputs that matched the corresponding measured voltages, is considered to be the correct estimate for the Ge/SiGe-based TEG module. The validity of the simulated estimate of the Seebeck coefficient is confirmed by comparing simulated voltage outputs for close circuit connection with corresponding close circuit measured voltage outputs and this is discussed next.

5.6.2. Comparison of Seebeck voltages in close circuit

The Seebeck voltages in close circuit are the voltages obtained when an external load resistance is connected to the TEG device. In simulating the FEM of the close circuit connection an external load resistances of 1.5 ohms in conjunction with the estimated contact resistance (based on circuit theory) of 1.42 ohms were used. Thus, the input parameters specified for the close circuit connections include those of Table 5.1, as well as the parameters summarized in Table 5.2 below.

Table 5.2: Additional inputs for the FEM of the TEG module in close circuit connection

s/n	Parameter	Quantity
1	R_L	1.5 Ω
2	R_{contact}	1.42 Ω

The simulated Seebeck voltage output for the close circuit connection is compared with the corresponding measured voltage outputs in Figure 5.7.

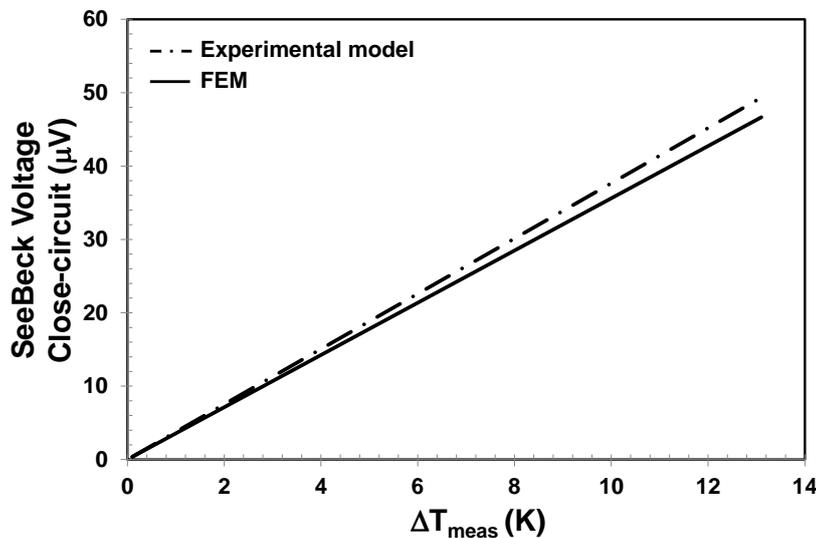


Figure 5.7: Comparison of FEM with experimental for close circuit connection

The maximum deviation of the simulated result from the experiment is about 6% and this shows a good agreement between both results. It can then be concluded that the simulated estimates for the effective values of α and σ are accurate. In the next section, effectiveness of the FEM for the Ge/SiGe-based TEG module is tested by comparing the simulated FEM results with results obtained from the analytical approach proposed by Wu [54].

5.7. Analytical approach based on Wu's method.

The analytical approach discussed in this section is based on the theoretical model derived by Wu [54]. The model proposes to predict a more realistic theoretical limit for the maximum specific power output and efficiency of a waste-heat TEG by accounting for both internal and external irreversibilities. The model can be used as a guide for designing TEGs and therefore, simulations of the FEM are compared with the results of the model in order to determine the effectiveness of the FEM for the Ge/SiGe-based TEG module. A detailed explanation of the derived Equations of (5.9 – 5.11) has been given in section 2.6.3 of Chapter 2:

$$I_m = \alpha(T_{hj} - T_{cj})/2R \quad (5.9)$$

$$T_{hj} = (U_H A_H T_H - 2RI_m K/\alpha + 0.5(I_m)^2 R)/(\alpha I_m + U_H A_H) \quad (5.10)$$

$$T_{cj} = (U_L A_L T_L + 2RI_m K/\alpha + 0.5(I_m)^2 R)/(U_L A_L - \alpha I_m) \quad (5.11)$$

The unknown variables are I_m , T_{hj} and T_{cj} which represent the maximum current output and the junction temperatures at the hot and cold side of the TEG, respectively. All input parameters are obtained from Tables 5.1 and 5.2 with the exception of the external load. The external load used is equal to the internal resistance of the TEG (i.e. 1.2 ohms) because Wu's model is based on impedance matching. Equations (5.9 - 5.11) are a set of coupled non-linear algebraic equations that require numerical solution. Hence, the *fsolve* tool in Matlab™ (version R20013a) was used to solve these equations. In using this tool, a good initial guess of the unknown variables is required because non-linear equations pose a problem of the possibility of multiple solutions or may not convergent to any solution. For the TEG module investigated in this section the initial guesses of the unknown variable were made based on the experimental results. Once the maximum current output and the temperatures at the hot and cold side of the TEG are determined, other outputs such as the open and closed circuit voltages i.e. V_{oc} and V_L , and the output power, P_L can be determined. The expressions for these outputs are given below:

$$V_{oc} = \alpha(T_{hj} - T_{cj}) \quad (5.12)$$

$$V_L = I_m R \quad (5.13)$$

$$P_L = I_m^2 R \quad (5.14)$$

Appendix 2 presents the Matlab codes that were developed to solve Wu's equations and estimate the theoretical maximum for open and close circuit voltages, load current and power output of the Ge/SiGe-based TEG module. The flow chart in Figure 5.8 is used to describe how the code works.

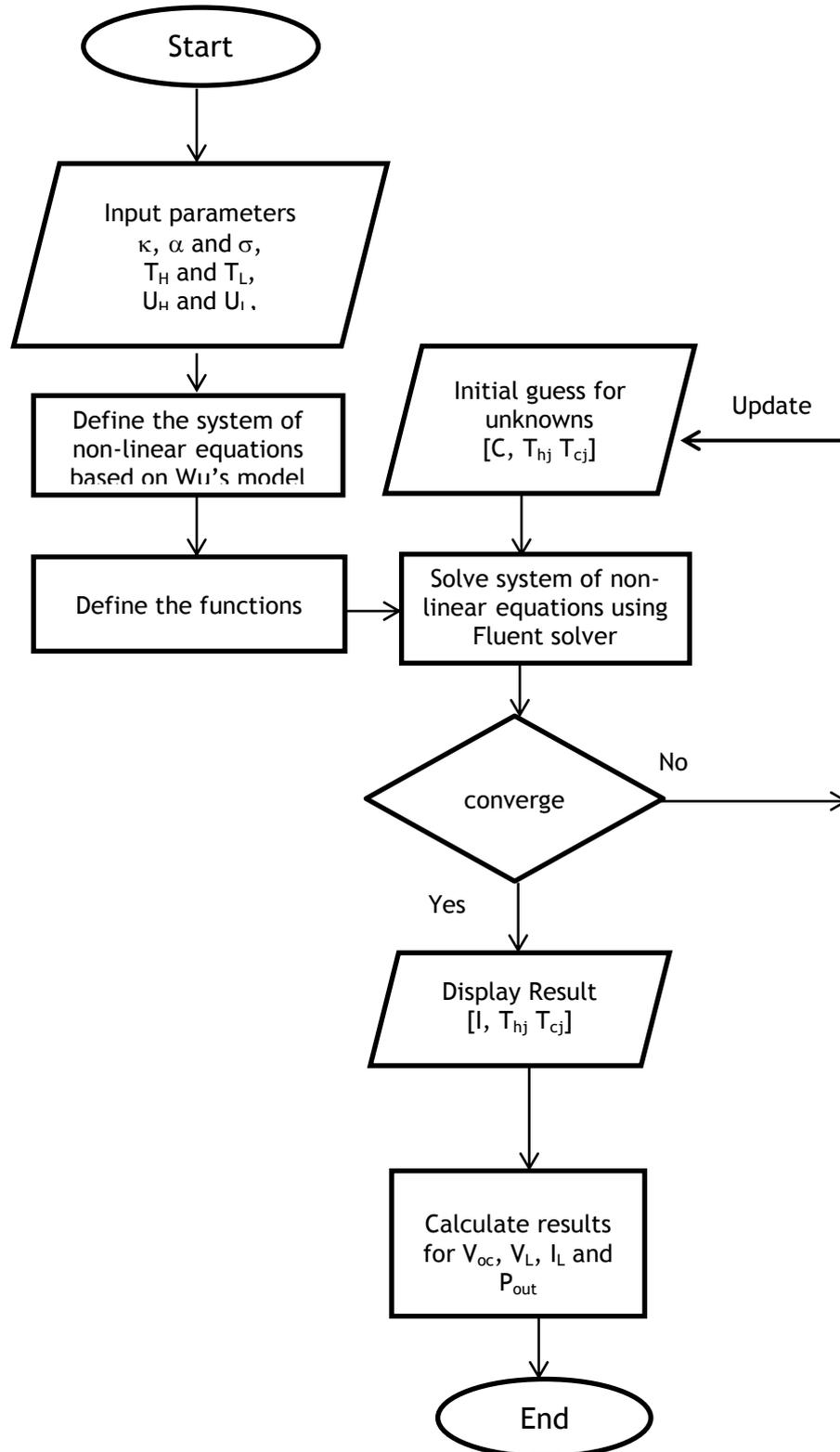


Figure 5.8 Flow chart used to describe the operation of the Fluent solver performed at each time step of the simulation.

1. Define the system of non-linear equations:

The system of non-linear equations is obtained by inputting parameters into Wu's analytical model as defined by Equations 5.9 – 5.11. The input parameters include:

1. Effective thermal conductivity of the TEG module: K
2. Effective Seebeck coefficient of the TEG module: α
3. Resistance of the TEG module. The resistance is obtained directly from the experiment conducted in Chapter 4. It is actually a representation of the effective electrical conductivity of the TEG module
4. Heat source and heat sink temperature: T_H and T_L
5. Heat transfer coefficient of heat source and heat sink.: U_H and U_c

The input parameters used in Wu's analytical model are stated in Table 5.1. The heat source and heat sink temperatures were varied between 298.15 K - 398.15K so that the maximum temperature difference obtained between both heat exchangers is 100 K. The parameters used for Wu's analytical model are similar to that of the FEM so that results obtained from both approaches can be compared comparatively.

2. Define the function:

This involves converting the system of nonlinear equation to a function. The following commands in Matlab is used to achieve this.

```
function fcns=eqns(z)
```

```
    C = z(1); % where C= current
```

```
    Thj = z(2); % Temperature at the hot junction of the TEG
```

```
    Tcj = z(3); % Temperature at the cold junction of the TEG
```

```
% These are the three unknowns in the simultaneous equations defined below
```

```
fcns(1) = (alpha*(Thj-Tcj)/(2*R))-C;%
```

```
fcns(2) = ((UH*AH*TH-2*R*C*(K/alpha)+0.5*C^2*R)/(alpha*C+UH*AH))-Thj;
```

```
fcns(3) = ((UL*AL*TL+2*R*C*(K/alpha)+0.5*C^2*R)/(UL*AL-alpha*C))-Tcj;
```

3. Apply the Fluent solver

The systems of nonlinear equation is solved using the Fluent solver (fsolve tool)

The command used in Matlab for applying the fluent solver is:

```
result = fsolve(@eqns, guess);
```

which means that by an iterative process starting with the initial guess values, approximate the roots that satisfy the set of non-linear equations (referring to Equations 5.9 - 5.11) and display the results. Therefore, an initial guess is set for each of the three unknowns of Equations 5.9 - 5.11 (i.e. current, C , temperature at the hot junction T_{hj} and temperature at the cold junction T_{cj}). The initial guess is necessary so as to avoid having multiple or no solution after a number of iterations. Where the solutions do not converge, (i.e. the function values are not close to zero), the initial guess will be updated or replaced using the results from previous calculation and inputting back into the system of nonlinear equations.

4. Display and Calculate results

The solutions from the system of non-linear equations converge after 7 iterations. Results for open circuit voltage, load voltage, load current and output power are therefore calculated from these solutions. These results are then compared with the FEM results as shown in Figures 5.8 (a)-(d) below.

5.7.1. Evaluation of FEM results with Wu's analytical approach

The results from simulation of the FEM are compared with the corresponding analytical results obtained using Wu's method. For ease of comparison and uniformity, temperature differences (i.e. $\Delta T_{meas} = T_h - T_c$) ranging from 10 - 100 K was specified across the heat exchangers of the TEG module for both FEM and Wu's method. Figures 5.9 (a-d) shows are plots of open circuit voltage, load voltage, load current and power output against ΔT across the TEG. The plots show that Wu's method produces higher estimates than the FEM. This is expected because the Wu's method provides a theoretical maximum gives an upper bound for real thermoelectric generators [54]. However, the FEM results

are close to the theoretical limits this shows that the Ge/SiGe-based TEG module is effective.

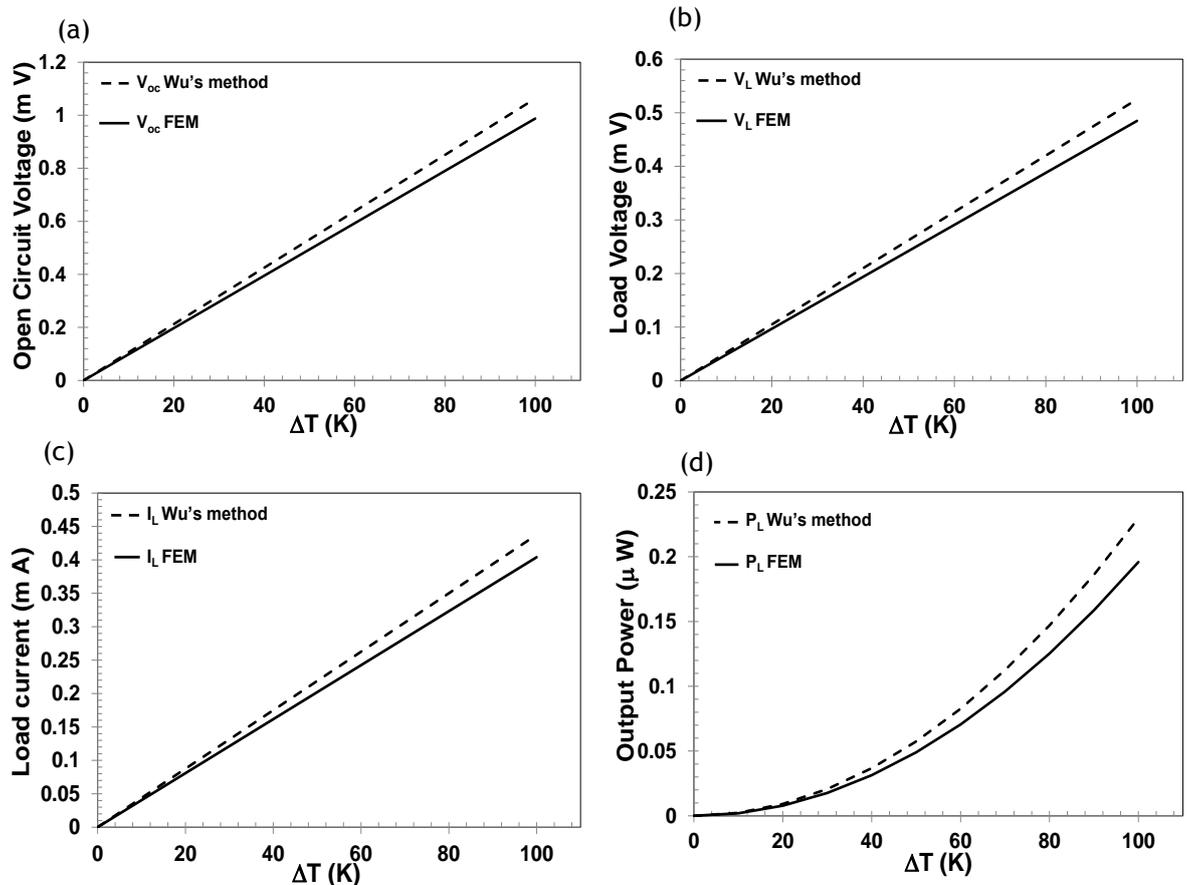


Figure 5.9 Comparison of FEM results with Wu's theoretical maximum approach for Ge/SiGe-based TEG module: (a) open circuit voltage (b) load voltage (c) load current (d) output power

The discussions presented in the previous sections provide detailed validation of the FEM for the Ge/SiGe-based TEG module and therefore, the FEM can be used for further analysis of the TEG module. For example, a limitation of the experiment discussed in Chapter 4 is the absence of a heat sink to aid dissipation of the heat in the system and achieve a higher temperature difference across the TEG module. The validated FEM can be improved by incorporating a heat sink and the effect of the heat-sink on the performance of the TEG module can be observed. Additionally, the effect of the material properties of the superlattice on the performance of the Ge/SiGe-based TEG module is investigated using the FEM.

5.8. Effect of heat sink on the performance of Ge/SiGe-based TEG module

A heat sink is a component that aids the dissipation of heat from a device (usually an electronic device), so as to avoid overheating. Incorporation of a heat sink is significant for dissipating most of the heat from the cold side of the TEG module. This helps to maintain the cold junction temperature of the TEG module at a constant temperature, irrespective of the amount of heat that is inputted into the system. By maintaining the cold side at a predetermined temperature, a significant temperature difference is created across the hot and cold junction of the TEG module. The thermal boundary conditions set for the TEG module and heat sink are the experimentally measured hot-side temperatures applied at the top of the device and ambient temperature at the bottom of the heat sink. The added heat sink can be simulated as a large copper block or as a set thermal boundary condition of 298.15 K at the cold side of the TEG module. The inclusion of a heat sink is expected to dissipate most of the heat away from the cold junction of the TEG module as shown in Figures 5.10 (a) and (b)

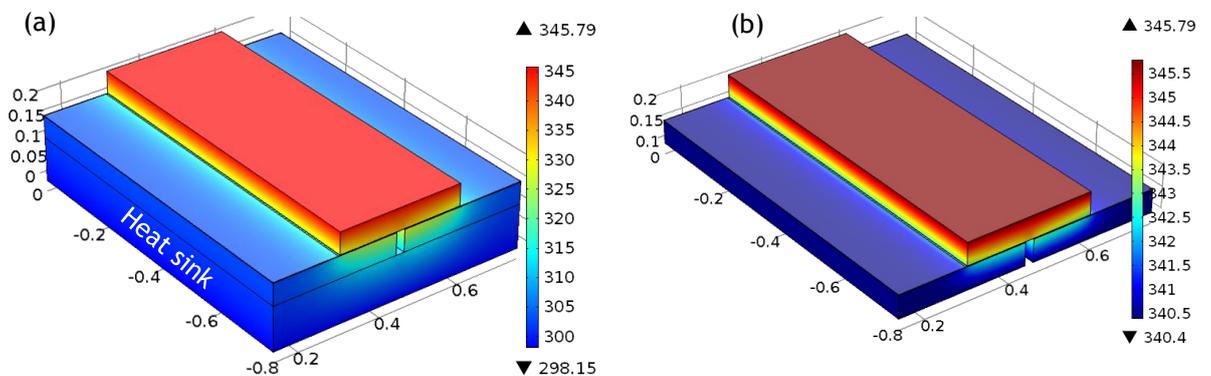


Figure 5.10: Device with (a) attached heat sink and (b) without a heat sink

Hence, the cold side temperature is set at a fixed temperature of 298.15 K (ambient temperature) in contrast to the case without heat sink where the cold side temperature varies as the hot side temperature varies (see Figure 5.9(b)). In this case, the heat source is applied at the top of the device and conducts downwards. From Figures 5.10 (a) and (b), it can be seen that the heat sink helps to reduce the bottom surface temperature of the Silicon substrate by 32.45 K (i.e. 340.4 – 307.95 K). Thus, the temperature difference across the

superlattice will increase and this will result to an improvement in the overall Seebeck voltage of the device as shown in Figure 5.11.

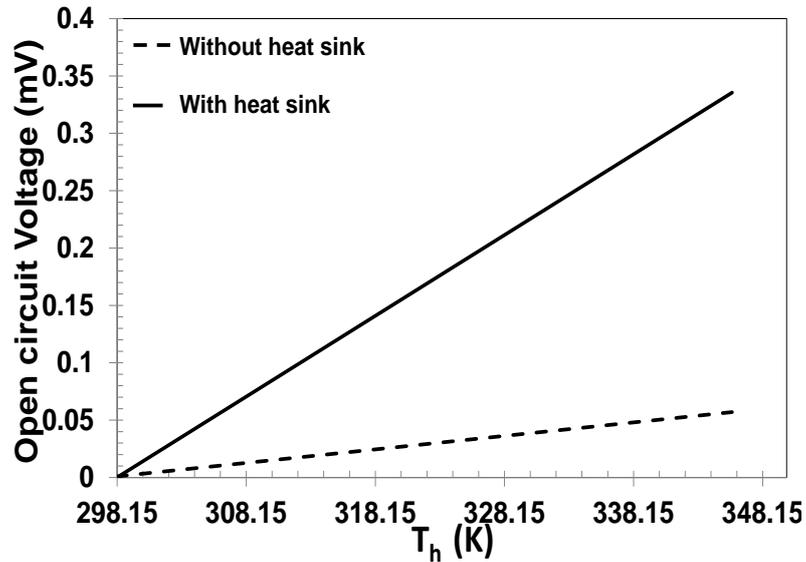


Figure 5.11: Effect of heat sink on the open circuit Seebeck voltages of the TEG module.

Subsequently, an improvement in the open circuit voltages will also result to an improvement in the load voltage (i.e. Seebeck voltage in close circuit), load current and power output of the device.

5.8.1. Effect of thermal contact boundary condition

In reality, the mounting of a heat sink onto a device or vice versa, may introduce thermal contact resistance between the bottom surface of the TEG module and the connecting surface of the heat sink. Thermal contact resistance may occur due to the voids created by interface roughness between the two surfaces and this can adversely affect the heat dissipative mechanism of the heat sink.

In the FEM software, thermal linkage between TEG module and the heat sink is made using the Thermal Contact boundary condition. This condition is defined by Equation (5.15) [85, 86]:

$$h_{\text{interface}} = h_{\text{constriction}} + h_{\text{gap}} = 1.25\kappa_s \frac{m}{\sigma_{\text{aah}}} \left(\frac{P}{H_c}\right)^{0.95} + \frac{\kappa_{\text{gap}}}{Y + M_{\text{gap}}} \quad (5.15)$$

where σ_{aah} is the average asperities height with a set value of 1 μm , and m , the average asperities slope, which is set at a value of 0.5. H_c is the micro hardness of Aluminium, which is equal to 165MPa. The contact pressure, P , is set to 20

kPa. The thermal conductivity κ_{gap} is referred to the medium in the interstitial gap. In this case, air at atmospheric pressure is assumed a value $0.025 \text{ W/(m}\cdot\text{K)}$. Figures 5.12 and 5.13 show the effect of thermal contact resistance on the heat dissipative mechanism of the heat sink.

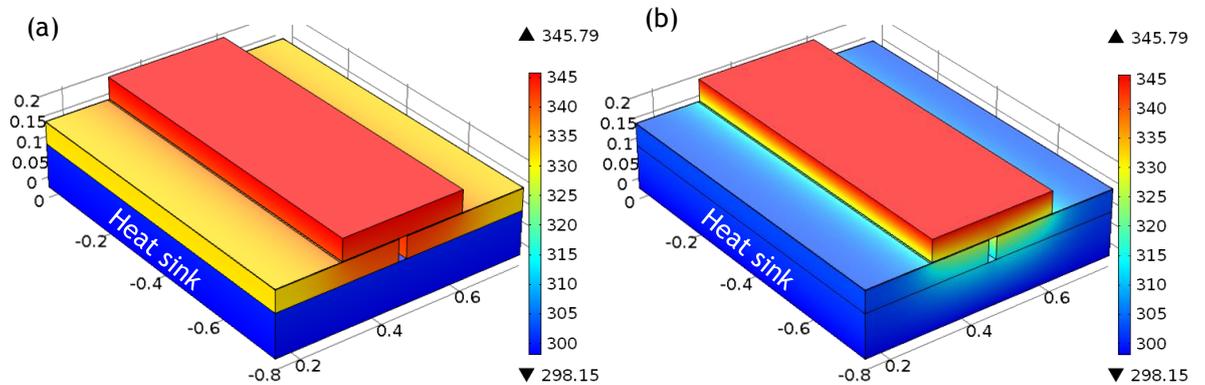


Figure 5.12: heat dissipative mechanism of the heat sink due to (a) thermal contact resistance (b) non-thermal contact resistance.

In Figure 5.12 (a), a steep thermal gradient is observed between the top of the heat sink and the bottom of the TEG module. This will adversely affect the temperature difference, $\Delta T_{\text{superlattice}}$ across the superlattice of the TEG module. This is not the case with (b); the heat sink effectively dissipates away the heat from the bottom surface of the TEG module and this will result to an improved $\Delta T_{\text{superlattice}}$. Subsequently, the open circuit voltages will be affected as shown in Figure 5.13.

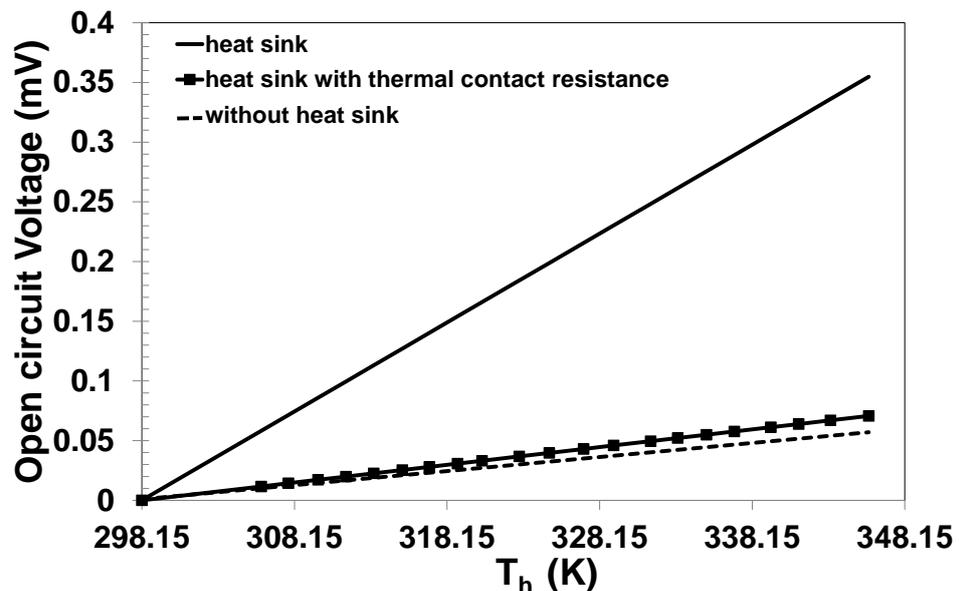


Figure 5.13. Comparison of open circuit voltages for a heat sink, heat sink with thermal contact resistance and without a heat sink attached to the TEG module

In Figure 5.13 a significant reduction in the open circuit voltage is observed for the device affected by thermal contact resistance, which is a slight improvement from the device without a heat sink. Experimental findings in the literature [81], has suggested that the thermal contact resistances can be minimized by the application of thermal grease. This will aid in filling up the air gaps between the heat sink and the bottom of the TEG module. Another approach to minimizing the contact resistance is to insert a soft metallic foil such as Tin, Silver, Copper, Nickel, or Aluminum between the two surfaces [81].

5.9. Effect of the material properties, electrical contact resistances and load resistance on the performance of Ge/SiGe-based TEG module

The properties of the thermoelectric material in a TEG module play a significant role on the conversion efficiency and power generated by the TEG module. A high Seebeck coefficient will lead to increased voltage in the circuit, a low resistivity (or high electrical conductivity) will minimise the Joule heating losses and a low thermal conductivity will aid in maintaining a high temperature difference between the hot and cold junctions of the TEG module [3].

5.9.1. Effect of material properties on the performance of TEG module

Table 5.3 presents the properties of two sets of thermoelectric material used for building a TEG.

Table 5.3: Properties of two types of thermoelectric materials

Property / Material	κ (W/mK)		α ($\mu\text{V}/\text{K}$)		σ (S/m)	
	p-type	n-type	p-type	n-type	p-type	n-type
Material 1 (M1)	5.5	26.1	112	269	4099	9400
Material 2 (M2)	5.0	6.0	394.4	455.4	8633	1834.6

The properties of M 1 and M 2 were obtained via material characterization techniques of reference [6]. M1 refers to the first set of p- and n- type materials that were used in fabricating the TEG module that was discussed in chapter 4 of this work, while M2 refers to the material that is used subsequently to build an improved TEG module. Both M1 and M2 refer to the building of a TEG module that is void of thermal and electrical contact resistance

By inspection of Table 5.3, it can be seen that the Seebeck and thermal conductivity values are more preferable in M2 than in M1. However, the electrical conductivity of M2 for the n-type material is less preferable than M1. Still, M2 is considered to be more efficient than M1 because of the overall ZT of the p and n-type material combinations. The overall ZT is defined as [4]:

$$ZT = \frac{\alpha^2}{(\sqrt{\kappa_n \rho_n} + \sqrt{\kappa_p \rho_p})^2} T \quad (5.16)$$

whereby $\alpha = \alpha_p + \alpha_n$. Thus, at 300 K, M1 has a ZT of 0.0055, while M2, which is more efficient, has a ZT of 0.03288.

The performances of M1 and M2 are assessed based on the Seebeck voltage in open circuit, load current, generated output power for an external load resistance of 1.0Ω and efficiency. Also, the hot side temperature is varied from ambient temperature of 25°C (or 298.15 K) to 100°C (or 398.15 K), the upper limit being determined by the melting point of the Indium bond (i.e. 120°C). Figure 5.13 (a - d) show the comparisons of the output results for M1 and M2.

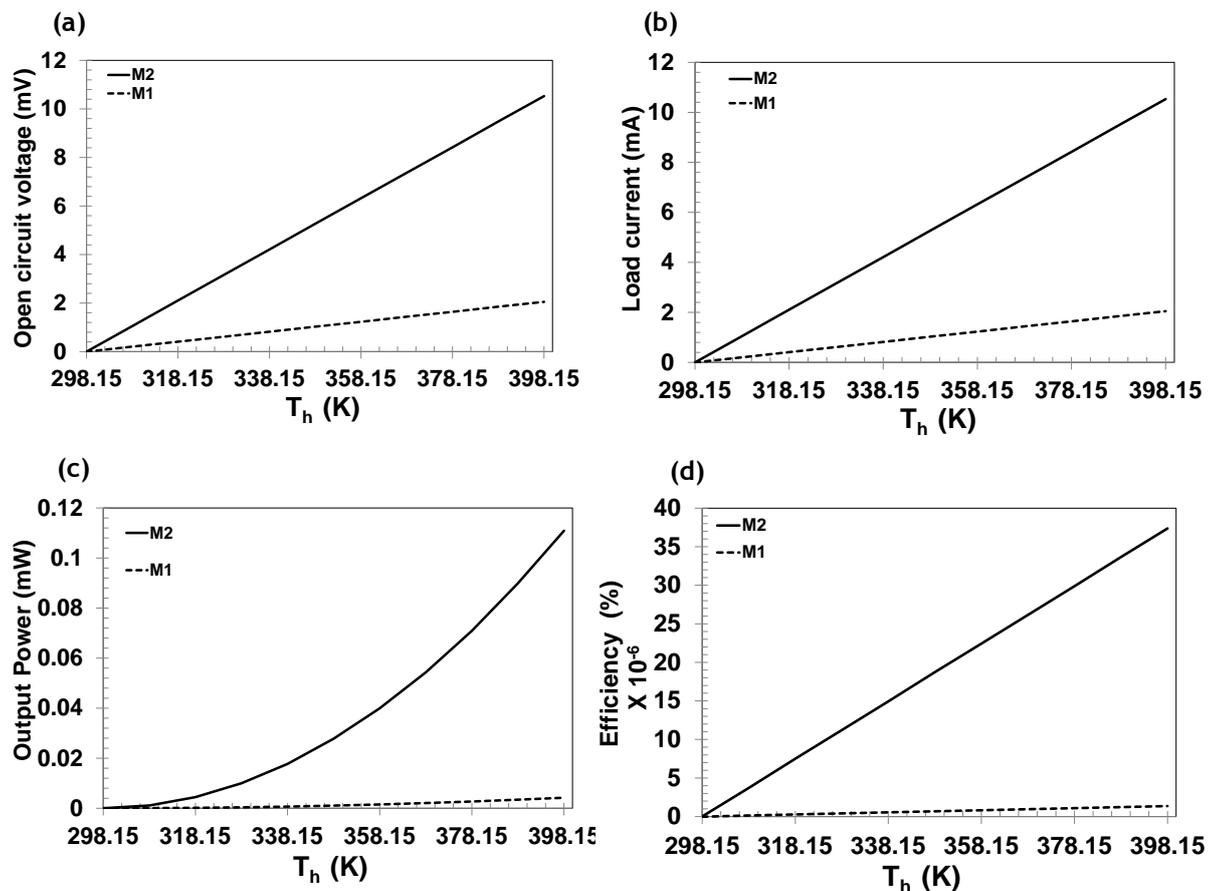


Figure 5.14: Comparison of M 2 and M 1 for (a) open circuit voltage (b) load current (c) output power and (d) efficiency

It is observed from Figure 5.14 (a) that the open circuit voltages for M2 are much larger in magnitude than that of M1. This is because of the significant difference in the total Seebeck values of the p- and n- type materials for M2 as compared to that of M1. Moreover, M2 has a much lower thermal conductivity than M1 and (see Table 5.3), which helps to further increase the open circuit voltage based on the Seebeck effect.

A similar trend is observed for the load currents in Figure 5.14 (b). It also indicates the magnitude of the load voltage, which is the same as the load current, because a load resistance of 1Ω was connected to the device in close circuit. The plots further suggest that by connecting an external load resistance of 1Ω , there is minimal voltage drop between the open circuit and load voltage for M2 and M1. Recall from the circuit theory analysis discussed in Section 4. 2. 3 of Chapter 4, that the load voltage can be determined from the voltage division rule:

$$V_L = V_{oc} \times \frac{R_L}{R_L + r}. \quad (5.17)$$

If $r \ll 0$, then $V_L \approx V_{oc}$. Therefore, for the present analysis the magnitude of the parameters V_{oc} , V_L and I_L are equal. Hence, from Table 5.3, it can be seen that M2 and M1 have a high electrical conductivity. Thus, the internal resistance of M2 and M1 is very small so that the open circuit and load voltages are almost equal. In reality, it is difficult to obtain such a low internal resistance that is negligible compared to the external load resistance. Moreover, there are issues of electrical contact resistance that affect the performance of the TEG, and this will be discussed in Section 5.9.2. It is also unreasonable to increase the external resistance indefinitely because it will affect the performance of the device. Further explanation on the effect of external load resistance on the performance of the TEG module is discussed in the Section 5.9.3. A significant drop in the output power, (Figure 5.14 (c)), is observed for M1 as compared to M2. From Table 5.3, M2 is expected to have a higher output power as compared to M1 as defined by Equation 5.17 [4]:

$$Power\ factor = \alpha^2 \sigma \quad (5.17)$$

A similar trend is observed for the efficiency plots of Figure 5.14 (d). Given the same amount of heat input, Q represented by the heater temperature T_h (which

was varied from 298.15 K to 398.15 K, it is expected that M2 will have a higher efficiency. Given the output power P , the efficiency is defined as:

$$Efficiency = \frac{P}{Q} \times 100\% \quad (5.18)$$

5.9.2. Effect of electrical contact resistance on the performance of Ge/SiGe-based TEG module

In order to illustrate the effect of contact resistance on the device performance, the results obtained from the analyses of the first experiment conducted in Chapter 4 will be used. Let M1 refer to the building of a TEG module that is void of thermal and electrical contact resistance while M1 + contact refers to the building of the TEG module that is affected by contact resistance. Table 5.4 is used to show the material properties obtained for M1 and M1 + contact

Table 5.4: Properties of M1 and M1+contact

Property / Material	κ (W/mK)		α (μ V/K)		σ (S/m)	
	p-type	n-type	p-type	n-type	p-type	n-type
Material 1 (M1)	5.5	26.1	112	269	4099	9400
Material 1 + contact	5.5	26.1	90	90	15.5	15.5

The properties of M1 + contact was obtained from fabrication and simulations of the TEG module discussed in the previous sections (i.e. Sections 5.2.1, 5.6.1 and 5.6.2). The electrical conductivity for M1+ contact is said to fall within the range of 1 - 40 S/m based on previous discussions (Refer to Table 5.1). However, a specific value within this range (i.e. 15.22 S/m) is set for the subsequent analyses that will be discussed shortly.

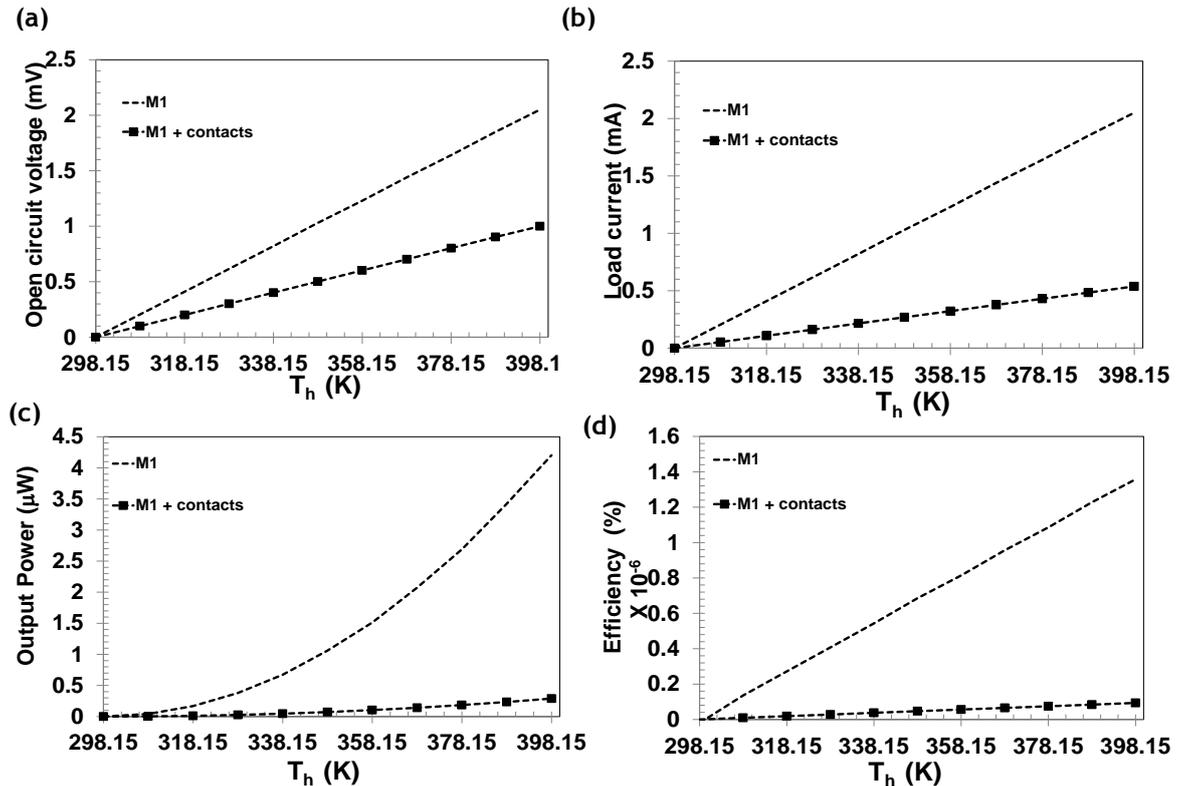


Figure 5.15: Comparison of M 1 and M 1+ contact for (a) open circuit voltage (b) load current (c) output power and (d) efficiency

The plots in Figure 5.15 (a), suggest that the open circuit voltage of the TEG module was reduced by less than half, due to the presence of contact resistance in the device. The consequence of the contact resistance is also seen in the other figures (i.e. (b)-(d)).

The figure in (b) shows that the load voltage for M1 + contact drops by approximately half of its open circuit voltage displayed in (a). Recall, for M1 + contact, the internal resistance was measured to be approximately 1.2Ω which is approximately the same in value as the external load resistance. This explains the half drop in voltage for M1 + contact as illustrated by Equation 5.17.

Figures 5.14 shows the comparison of M2 and M1, thereby showing the effect of using a more efficient material in building the TEG, while Figure 5.15 shows the comparison of M1 and M1 + contact, thereby showing the effect of contact resistance on the device performance. Thus there is no need to include M2 + contact as this will show a similar effect as M1 + contact. Based on the above analyses in Sections 5.9.1 and 5.9.2, it can be deduced that the performance of TEGs to a large extent are affected by both the type of material being used as

well as the contact resistances. The contact resistance will significantly reduce the performance of the TEG. Hence, measures need to be taken to improve the efficiency of the thermoelectric material as well as reduce the contact resistance to its barest minimum for improved performances.

5.9.3. Effect of load resistance on the performance of Ge/SiGe-based TEG module

As earlier explained, it is important to appreciate the effect of load resistance on the output power and load voltage of the TEG module. The TEG module for M1 + contact is used for this analysis. Already, it has been discussed that this device has an internal resistance of approximately 1.2Ω . Hence, the external load resistances will be varied between 0.2 to 100Ω . This variation is considered important for the following reasons:

- To study the effect of load resistance on the output power and load voltage
- To evaluate the effect of impedance matched loads (i.e. $R_L = r$) on the output power and load voltage.
- To ascertain Equation 5.17.
- To know the optimum external load resistance that should be connected to the TEG module.

Figures 5.16 (a) and (b) presents the results obtained for the output power and load voltage with increase in the external resistance.

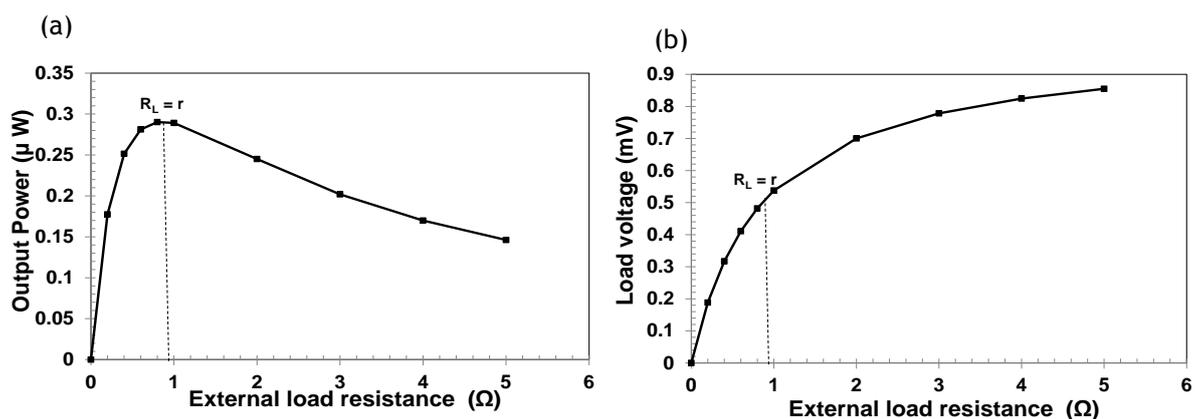


Figure 5.16: Effect of load resistance on the (a) output power and (b) load voltage of the TEG module

Figure 5.16 (a) shows a rapid increase in the output power until it reaches a maximum peak where the load resistance R_L equals the internal resistance r of the TEG module. Thereafter, the output power decays exponentially with

further increase in the load resistance beyond $R_L = r$. An exponential growth is however observed for the load voltage as it tends towards the open circuit voltage (see Figure 5.16 (b)). This trend is confirmed by Equation 5.17. It also shows that at impedance matched loads, the load voltage is approximately 50% of the open circuit voltage, which is again confirmed by Equation 5.17. Furthermore, comparison of the two plots show that impedance matched loads does give the optimum performance of the device.

Chapter Summary

In this chapter, the development of an FEM for Ge/SiGe-based TEG module and the validation of the FEM using experimental data and Wu's theoretical maximum for irreversible TEGs are discussed. The validation was performed by considering Seebeck voltages in open and close circuit connections. A lower estimate of Seebeck coefficient ($180\mu\text{V/K}$) was obtained from simulation of the FEM as compared to the estimate from the experimental measurements ($265.91\mu\text{V/K}$). The legs of the TEG module have different thermal conductivities and this situation results in an imbalance of heat transferred through the legs. In an ideal case, both legs should be impedance matched, so that equal amount of heat flows through the legs simultaneously. The FEM is able to account for this imbalance and hence gives a more realistic estimate of the Seebeck coefficient unlike the experimental estimate of the Seebeck coefficient that is based on the average temperature differences across the legs.

The open circuit Seebeck coefficient estimated from the FEM was used for simulation of the TEG in close circuit connection. The results of the close circuit voltages were compared with corresponding experimental voltages in order to validate the FEM. This investigation confirmed that the FEM produced outputs that are in good agreement with experimental measurements. Also, FEM results such as the load current and output power were evaluated using Wu's theoretical maximum [54]. The investigation confirmed that the FEM developed here produced performances that are very close to the theoretical maximum predicted by Wu's models. Hence, the present FEM for the Ge/SiGe-based TEG module is reliable and can be used for cost-effective design and optimisation of high performance TEGs. The next chapter discusses the optimal design of the Ge/SiGe-based TEG module using the present FEM.

6. Optimal design and Experimentation of an Efficient Ge/SiGe-based Thermoelectric Generator

An optimal design for the Ge/SiGe-based TEG module obtained using FEM is discussed here. The design is developed based on the results and observations of the test TEG module that was discussed in Chapter 4. From observations of the experimental results in Chapter 4 it was recommended that a TEG module with higher performance can be achieved by improving the heat transfer mechanism and the using of a TE material with better material properties. Using the FEM developed in Chapter 5, the present chapter discusses parametric studies that were carried out in line with the recommendations of Chapter 4, in order to produce an optimal design for the Ge/SiGe-based TEG module.

Thus, the main goal of developing this optimal design is to maximize the power generating capability while minimizing the total volume of materials used for fabricating the TEG module. TEG performance improvement methods that have been considered in previous published works include varying the geometrical dimensions of the TEG i.e. leg length and the surface area [87, 88], thermal impedance matching (such that the external thermal resistances of the heat exchangers are equal to the internal thermal resistances of the TEG module) [89] and electrical impedance matching between the p-leg and n-leg of the TEG. Other techniques include matching of the load resistance to the internal resistances for maximum output power [4]. Optimization of all the components in the energy system i.e. thermal system, electrical system, and the TE device itself have also been studied [90].

In the present chapter, optimal design of a Ge/SiGe-based TEG module is conducted within the limits and constraints posed by the material properties of the Ge/SiGe TE material and the fabrication technique used in building the TEG module at the JWNC, University of Glasgow. A uncouple TEG module design, which involves only one p-leg and one n- leg, is considered. Optimal design is conducted mostly from geometrical considerations using parametric analysis of the FEM of the Ge/SiGe-based TEG module.

Finally, a second experiment is conducted, taking into consideration the optimal designs discussed in the simulations. The more efficient Ge/SiGe TE material described in Section 5.8.2 of Chapter 5 is used for this experiment. The experimental results obtained from the fabricated optimal design are discussed in comparison with other published works.

6.1. The optimization concept

Optimization involves specification of the objective function, which is a quantitative measure of a device's performance, for example the maximum power output of a TEG module. The set objective is dependent on a set of variables which affects its performance. For example, the variables that influence the maximum power output of a TEG are length of the p-leg and n-leg, thickness of the substrate, heat source and heat sink temperatures and external load connected to the device. Often times, these variables are constrained by certain factors such as the strain or stress capability of the material, availability of measurement equipment or the operating conditions. Such constraints have to be accounted for when conducting optimization studies [91]. The major constraint observed during the course of fabrication of the Ge/SiGe-based TEG module is that the heat source temperature must be below 120°C (or 393 K), which is the melting point of the indium bond that was used to connect the p-leg and n-leg. The variation of the heat source temperature is achieved by regulating the power supply to the Peltier heater. Therefore, the design techniques using FEM are developed based on the assumption that the heat sink is able to maintain the cold side temperature at 300 K and the hot side temperature at 400 K.

The sample has been observed to exhibit electrical leakages at the substrate layer of the p- type Ge/SiGe material and this is not desirable. Hence, in order to avoid a short circuit between the p-leg and n- legs after flip- chip bonding (see Figure 6.1 (a)), the p- and n-type material had to be cut in size (less than 1 cm²) and then linked together at one end while the other end is separated as shown in Figure 6.1 (b).

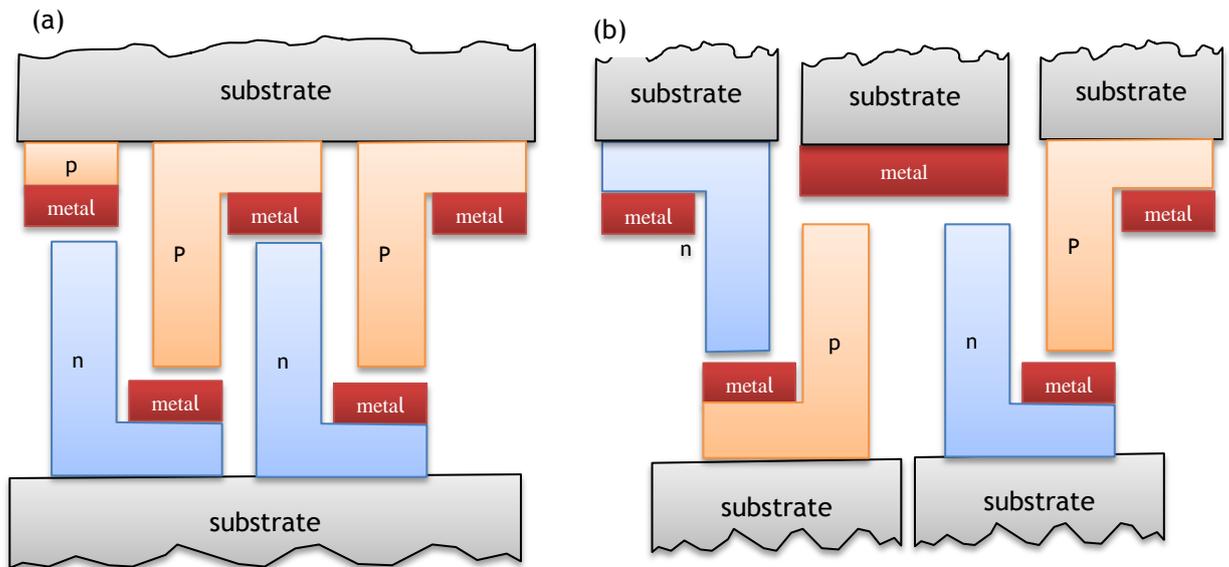


Figure 6.1: (a) Flip chip bond to connect p- and n-leg (b) connection of p- and n- leg after separation to avoid short circuiting

Multiple p- or n-type legs can be formed from a single piece (1 cm^2) of Ge/SiGe material, assuming the substrate is non-conducting. All the p-type legs formed from the single piece of material can be bonded at the same time to the n-type legs by flip chip method and this forms TEG modules with multiple legs (Figure 6.1 (a)). However, due to the limitation posed by the unwanted conducting substrate, minimum cut size of the cross sectional for both p and n-leg is $0.3 \times 0.3 \text{ cm}^2$. Cutting of the material beyond this value may break the samples, thus rendering them un-useable for fabrication. The focus therefore is to obtain the optimal geometrical configuration, based on the schematic of Figure 6.1(b), for maximum output power and optimal conversion efficiency.

6.2. Geometrical variation of Ge/SiGe - based TEG module.

The variation of the geometry of Ge/SiGe-based TEG module is performed in three different stages:

- Variation of the top and bottom substrates
- Variation of the overall surface area of the TEG module
- Variation of the leg height, which is represented by the thickness of the superlattice structure.

6.2.1. Variation of thickness of top and bottom substrates

The top and bottom substrates of the TEG module have an original thickness of $530\ \mu\text{m}$. These substrates act as heat exchangers because the top substrate is in contact with the cold heat sink while the bottom substrate is in contact with the heat source. Therefore the thicknesses of these substrates play a significant role in the performance of the TEG module. Three (3) different designs are considered; (a) the variation of only the top substrate; (b) variation of only the bottom substrate and (c) variation of both top and bottom substrates. All three designs are then compared with the original design to determine which design produces a better performance. Figure 6.2 (b-d) shows the three designs in comparison to the original design in Figure 6.2 (a).

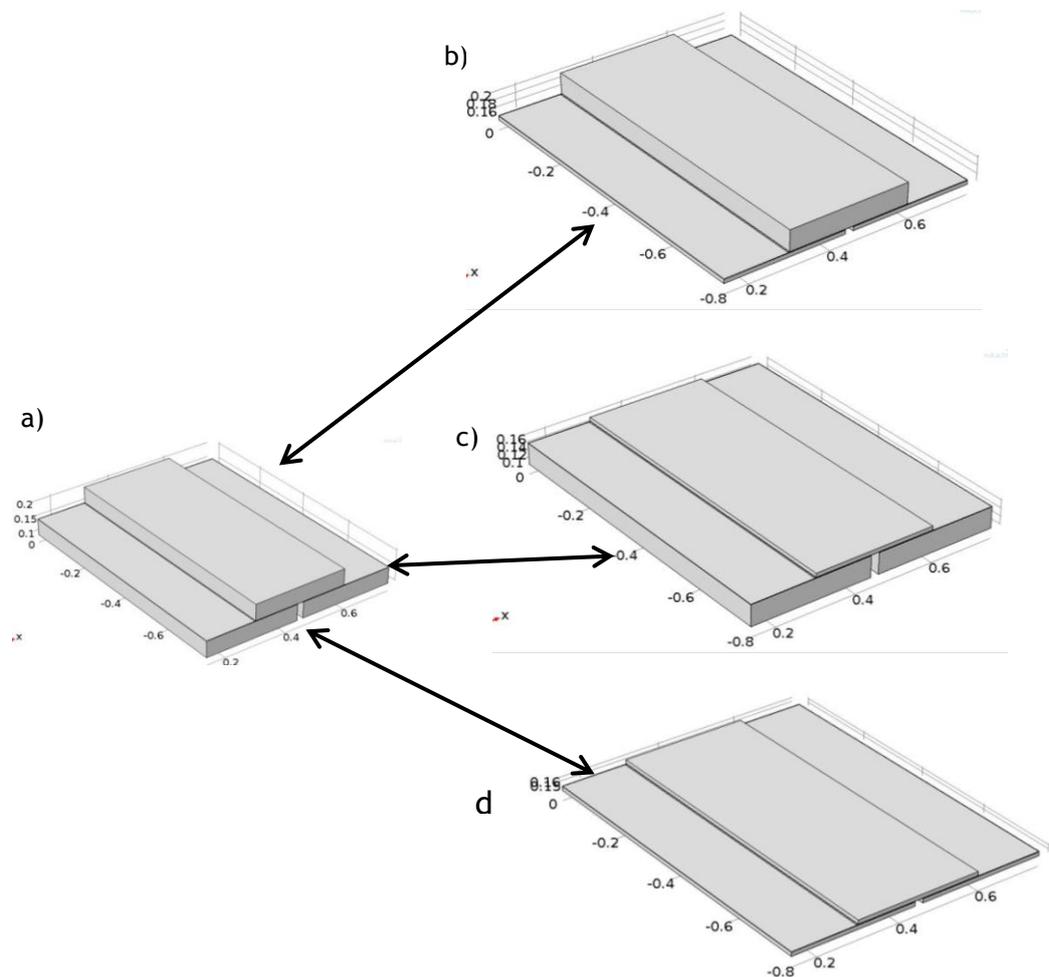


Figure 6.2:(a) Original design; variation of (b) bottom substrate (c) top substrate (d) top and bottom substrate;substrate thickness is reduced to $100\ \mu\text{m}$ in all three cases.

The thickness of the top and bottom substrate is varied within a range of $530 - 100\ \mu\text{m}$. Reducing the substrate thickness of the Ge/SiGe material beyond $100\ \mu\text{m}$ is possible but not practically reasonable because the sample will become too fragile for handling and is very susceptible to damage during the

course of fabrication. The critical parameters that determine the performance of the TEG module, i.e. temperature difference across the superlattice - $\Delta T_{\text{superlattice}}$, open-circuit voltage - V_{oc} , heat input - Q_h , load current - I_L , efficiency and generated power output, are compared for the four case studies. Since an external load resistance value of 1Ω is used for the geometrical analyses, it is expected that the load voltage will have the same magnitude as the load current based on Ohms Law (i.e. $V_L = I_L R_L$). Also, a more efficient material for the TEG module will be expected to have a high electrical conductivity and hence a low internal resistance, which means that $V_L \approx V_{\text{oc}}$ based on Equation 5.17. Therefore, for the present analysis the magnitude of the parameters V_{oc} , V_L and I_L are equal. As a result, only plots showing the variation of V_{oc} with $\Delta T_{\text{superlattice}}$, efficiency and output power are presented (Figure 6.3).

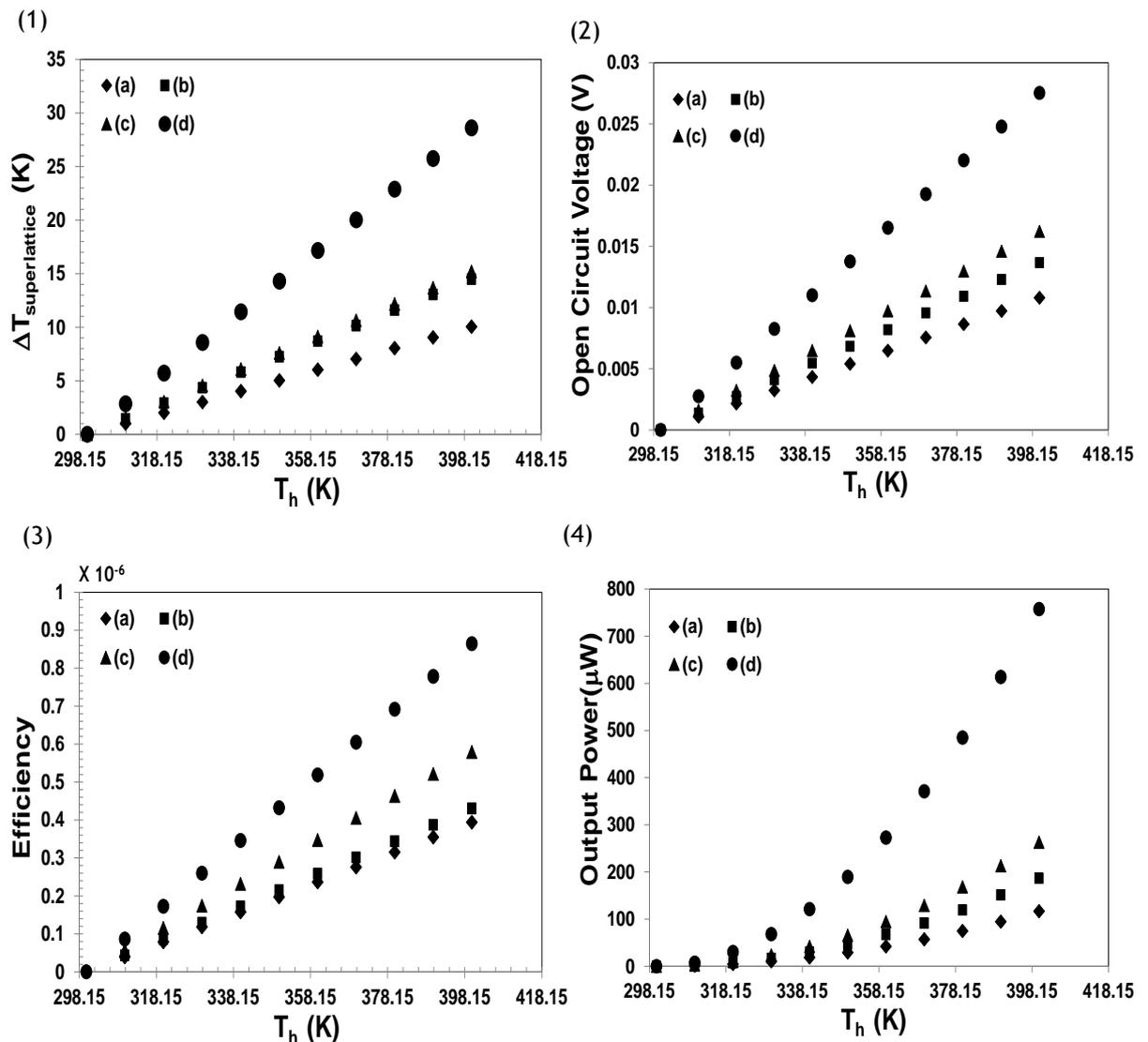


Figure 6.3: (1) Temperature difference across superlattice (2) corresponding open circuit voltage (3) Efficiency and (4) power output generated for the various geometrical configurations described in Figure 6.2

Figure 6.3 (1) - (4) presents the results obtained for the various geometrical configurations described in Figure 6.2. The temperature difference across the superlattice, $\Delta T_{\text{superlattice}}$ for the different configuration is estimated as shown in Figure 6.3(1). It is observed that the thermal losses decrease with reduction in the substrate thickness; the largest $\Delta T_{\text{superlattice}}$ is obtained for configuration (d). A similar trend has also been observed in the literature [88], whereby as the thickness of the substrate increases, the thermal loss in the substrate becomes larger than that in the thermoelements. Configurations (b) and (c) appear to have very close temperature differences. This implies that the thermal contributions from the bottom substrate are nearly the same as that of the top substrate. This is expected because both top and bottom substrates have the same surface to volume ratio for the p-leg and n-leg, and both are made of the same material. Hence, with both substrates reduced as shown in configuration (d), twice the increase in $\Delta T_{\text{superlattice}}$ can be observed. The corresponding open circuit voltage, V_{oc} , for the four configurations is shown in Figure 6.3 (2). These voltages are dependent on $\Delta T_{\text{superlattice}}$ based on the Seebeck effect principle. Therefore, the largest output voltage is also observed for configuration (d).

Figure 6.3 (3) and (4) presents the respective plots for efficiency and output power generated. It is observed that the efficiency of configurations (a) and (b) are almost the same while for the output power generated, configuration (b) almost doubles configuration (a). A simple explanation for this is that twice the amount of heat input is required to maintain the same overall temperature difference across the device (i.e. ΔT_{meas}) in (b) than in (a). The removal of the bottom substrate in (b) leads to reduced thermal losses as compared to (a). The reduced thermal losses makes (b) to have a higher voltage output than (a). Refer to the voltage readings in Figure 6.3 for configurations (a) and (b). By taking the square of the voltages and dividing by a resistance value of 1Ω , the respective power outputs are obtained. Thus the power generated in (b) is double that of (a). Since efficiency is estimated as the ratio of output power to heat input, both (a) and (b) are most likely to have similar efficiencies (i.e. efficiency = $P_b/Q_b = 2P_a/2Q_a$)

6.2.2. Variation of the overall area of the TEG module

It has been shown in the Section 6.2.1 that configuration (d) produces the best performance considering thickness variations of the top and bottom substrates. Hence, this configuration is investigated further by considering variations in the overall surface area. Two surface areas are considered: the surface area of the TEG module, of $0.64 \times 0.8 \text{ cm}^2$, which was discussed in Chapter 4; and a reduced area of $0.64 \times 0.35 \text{ cm}^2$ as shown in Figure 6.4. The reduced area is based on physically realisable constraints as earlier described in the paragraph below Figure 6.1.

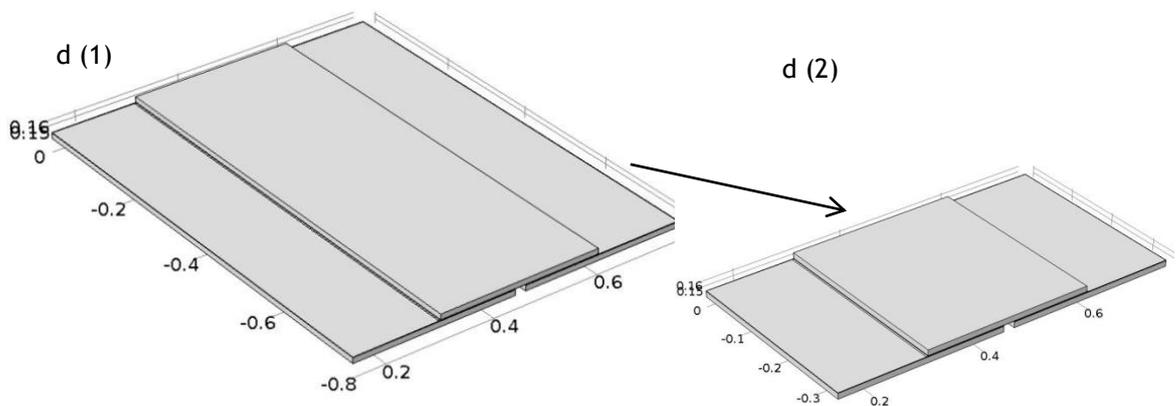


Figure 6.4: Reduction of overall area of configuration (d) from d (1) to d (2)

The overall area of configuration (d) is reduced to observe the performance of the device. Again, results for $\Delta T_{\text{superlattice}}$, open-circuit voltage, generated output power and efficiency are obtained for the reduced configuration and are compared against the original. Comparison of the simulated results for the reduced configuration d(2) and that of d(1) is presented in Figure 6.5.

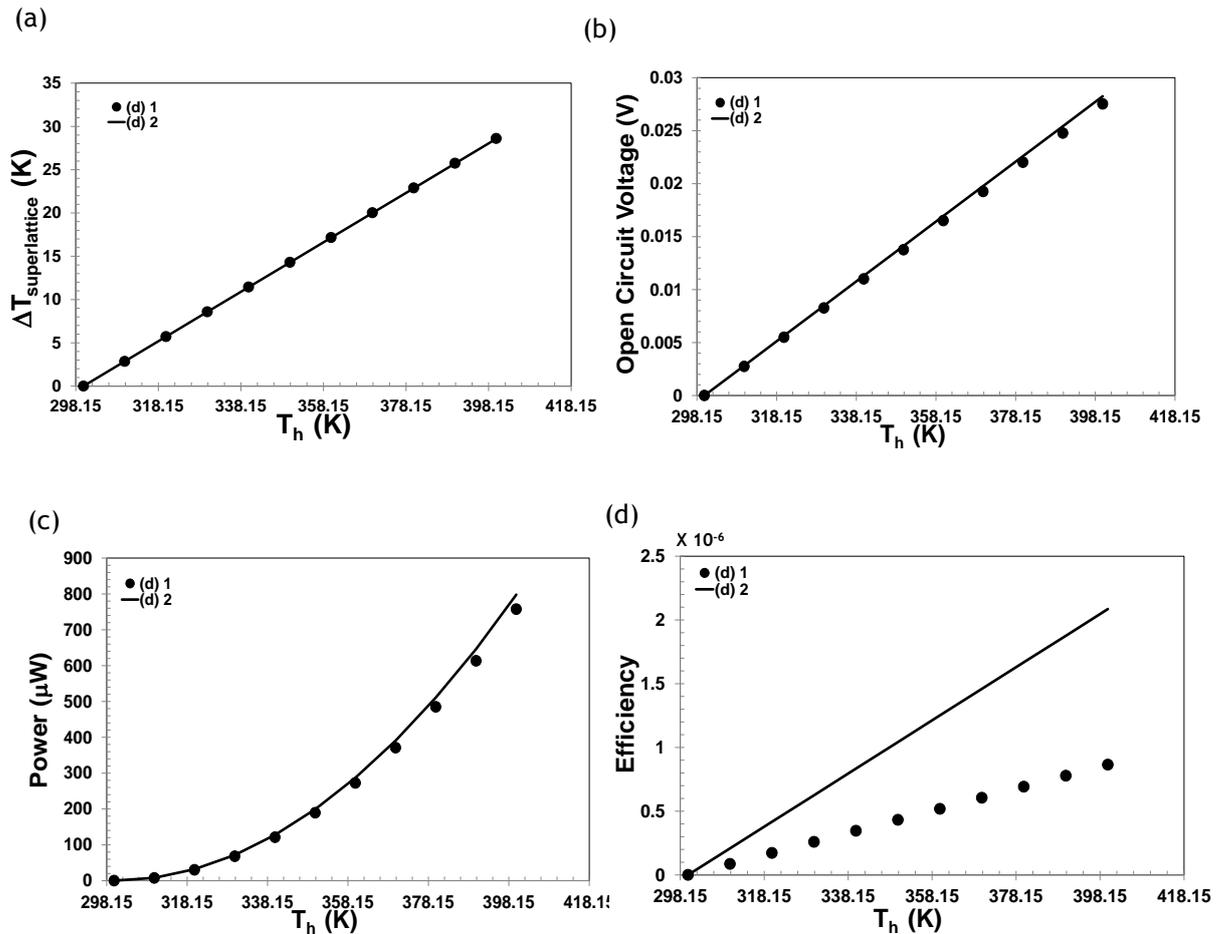


Figure 6.5: Comparison of (a) temperature difference across superlattice (b) open circuit voltage (c) output power and (d) efficiency for the geometrical configurations d(1) and d(2).

Figure 6.5(a) shows the comparison of d(1) and d(2) with respect to the temperature difference across the superlattice. It is observed from these plots that the temperature difference remain the same after the reduction of the overall area from d(1) to d(2). This is simply because the heat source and the heat sink were maintained at a fixed temperature based on the assumption that the heat absorbed and rejected are equal and both occur at the same rate. It therefore implies that a less amount of input heat, Q_h , is required to maintain the specified temperature difference for d(2) as compared to d(1). This is further explained taking into consideration Fourier's law of heat conduction: $Q_h = \kappa A \Delta T$. In order to maintain ΔT , Q_h will have to increase as the area, A , increases and vice versa. The implication is that in order to maintain a constant ΔT while the leg area is scaled up, the Seebeck voltage and power output will remain almost the same but the efficiency produced for the larger surface area is reduced.

In (b) it can be seen that at higher temperatures, (i.e. as the heat source increases), d(2) has an improved voltage output that is less than 2% better than d(1), even though it is not very obvious from the plots in (b). This not so obvious heat loss is due to d(1) having a larger dimension than d(2) and hence acquires more heat losses than d(1). Since the voltage is directly proportional to the temperature difference based on the Seebeck effect, the difference in voltage output between d(2) and d(1) is not expected to be much. A similar trend is also observed in (c).

In (d), it becomes obvious that d(2) is a better configuration than d(1) because of their respective efficiencies. Recall that efficiency is the ratio of output power to input power. Since there is not much difference in the power generated by both devices, and the larger device d(1) acquires more heat input than d(2) to maintain the same temperature difference, the efficiency for d(1) will be less than that of d(2). The physical meaning of these results is that smaller dimensions are more cost effective in terms of the amount of heat input required and in terms of the volume of material needed to build a TEG module.

In summary, having a bigger device does not necessarily give a better performance than a smaller device with respect to the voltage and generated power output. Also, smaller devices are preferred and are more cost effective since a lesser amount of material is required to produce almost the same results and has a better efficiency than bigger devices.

6.2.3. Variation of the leg height of the superlattice

It has been shown in the Section 6.2.1 that configuration (d) produces the best performance considering thickness variations of the top and bottom substrates. Hence, this configuration is investigated further by considering variations in the superlattice height for the p- and n- leg. In this case, it is assumed that the p- and n- leg are of the same height. The leg heights are therefore varied between 3.5 – 1.5 μm . Figures 6.6 (a) - (d) shows the effect of varying the leg height with temperature difference, open circuit voltage, output power and efficiency.

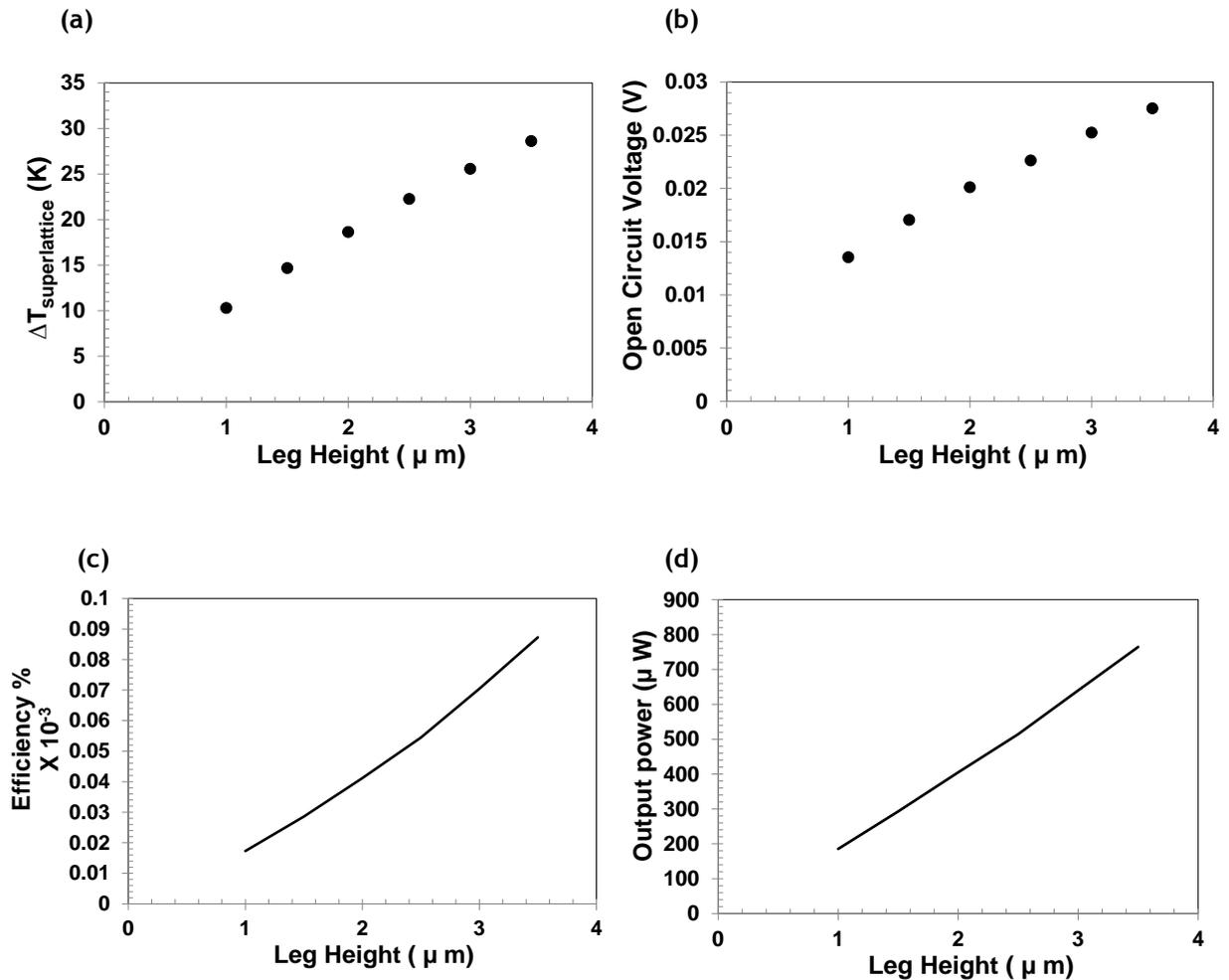


Figure 6.6: Effect of Leg height on the (a) Temperature difference across superlattice (b) corresponding open circuit voltage (c) Efficiency and (d) power output generated

From Figure 6.6 (a), it can be seen that the temperature difference across the superlattice increases with increase in the leg height (or superlattice thickness). This results to a corresponding increase in the open circuit Seebeck voltage, as shown in (b) and improved performances in the output power and efficiency, as shown in (c) and (d) respectively. The physical interpretation of this is that the higher the thickness of the superlattice layer, the better the performance of the device. This implies that the generation of a Seebeck voltage is limited by the thickness of the superlattice layer.

In general, the various simulations discussed in Sections 6.2.1 - 6.2.3 show that reduction of the thermal resistance by reducing the top and bottom substrates will help to improve the temperature difference across the superlattice and subsequently improve the performance of the system. Reduction of the cross

sectional area of the device is more efficient and cost effective. Finally, the magnitude of the Seebeck voltage that can be produced is dependent on the thickness of the superlattice layer.

It is important to note that the simulations have been performed based on ideal conditions whereby the effect of thermal and electrical contact resistances is negligible. In practice, however, this is not the case; there might be other factors, such as probe measurement resistances, interfacial thermal and electrical contact resistances, that can affect the performance of the TEG device.

A second experiment, similar to that of Chapter 4 but with a more efficient Ge/SiGe material was conducted. The second experiment takes into consideration some of the conclusions of the simulations previously discussed in Sections 6.2.1 - 6.2.3; The dimension of the TEG module is reduced to that of the geometrical configuration of d(2) as presented in Section 6.2.2. The substrates however remained at their initial thickness of 530 μm because of time constraint and long breakdown of the equipment required to etch down the substrates to the various thickness discussed in Section 6.2.1. The result of the second experiment is discussed next.

6.3. Experimentation of an efficient Ge/SiGe-based Thermoelectric Generator

The purpose of conducting a second experiment is to obtain better performances than that of the previous experiment discussed in Chapter 4.

The following precautions were taken during the course of taking the measurements:

1. The functionality of the thermocouples used for the temperature measurements were checked using a temperature control hotplate. Thereafter, the two leads of the thermocouples are labelled to differentiate between T_h and T_c . This will help to avoid mix-up when taking readings for the hot and cold side temperatures.

2. The needles of the voltmeter are properly fixed on the fabricated device to measure the generated Seebeck voltage. In order to confirm that the needles are properly fixed, an approximate value of 0.00 should be seen on the voltmeter, since there is no temperature difference created at the onset.
3. About 2mins wait period was given to allow the system to stabilize before taking any reading.

A pictorial diagram of the fabricated device is shown in Figure 6.7 below.

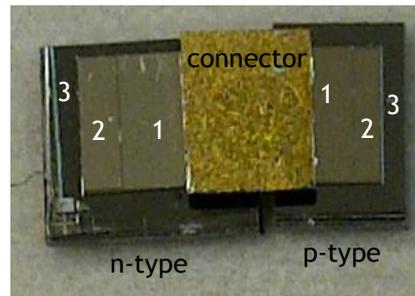


Figure 6.7: Diagram of fabricated TEG-module with surface area dimensions of 0.64 X 0.35 cm²

The numbers 1, 2, 3 refer to the superlattice, buffer layer (at a depth of 6.4 μm) and silicon substrates (having a depth of 28 μm). Also, the fabricated device has the surface area of the n-type to be larger than that of the p-type material (i.e. $A_n \approx 1.98 A_p$). This was done to allow for thermal and electrical impedance matching, using the equation derived by Ioffe [4] and the thermal and electrical properties for material M2 of Table 5.3, Section 5.9 of Chapter 5.

$$\rho_n/k_n \times k_p/\rho_p = \left(A_n/A_p \right)^2 \quad (6.1)$$

The determination of the optimal position for taking measurement readings is discussed next.

6.3.1. Determination of optimal position for taking measurements readings

The fabricated device for D(2) was designed in such a way that voltage readings could be taken both at the bottom and at the top of the p- and n- legs as shown in Figure 6.8. Taking measurements at the bottom of the legs is usually the

conventional way of taking measurements. However, it was considered useful to take measurement readings at the top, and compare the results with that obtained at the bottom. The purpose for this comparison was to see if the silicon substrates for the p- and n-type materials contribute to the generated Seebeck voltage. The position with the better result was then used for subsequent measurement readings.

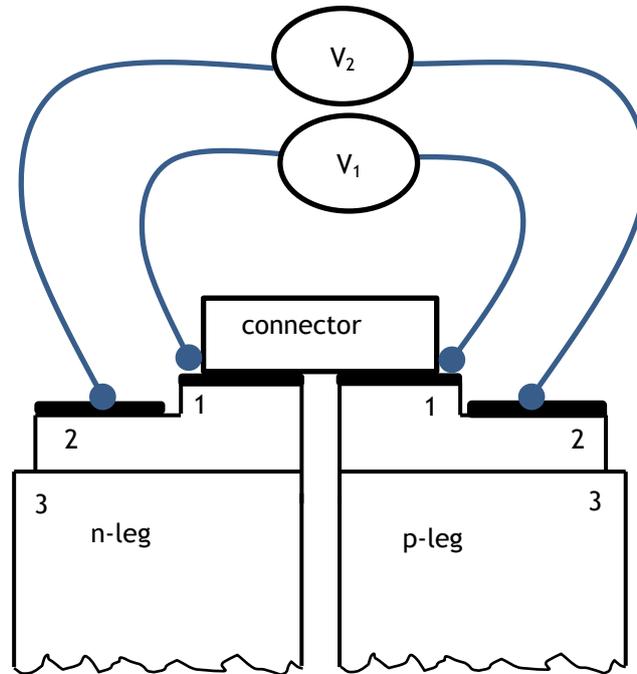


Figure 6.8: Schematic diagram of single p-leg and single n-leg connection with measurement positions for taking voltage readings, V_1 and V_2 .

The schematic diagram is used to demonstrate two positions via which voltage readings were taken. Voltage readings in open circuit were taken for this analysis. The better position was then used to take subsequent readings throughout the measurements. Figure 6.9 presents two plots obtained for the open circuit voltage readings obtained at V_1 and V_2 .

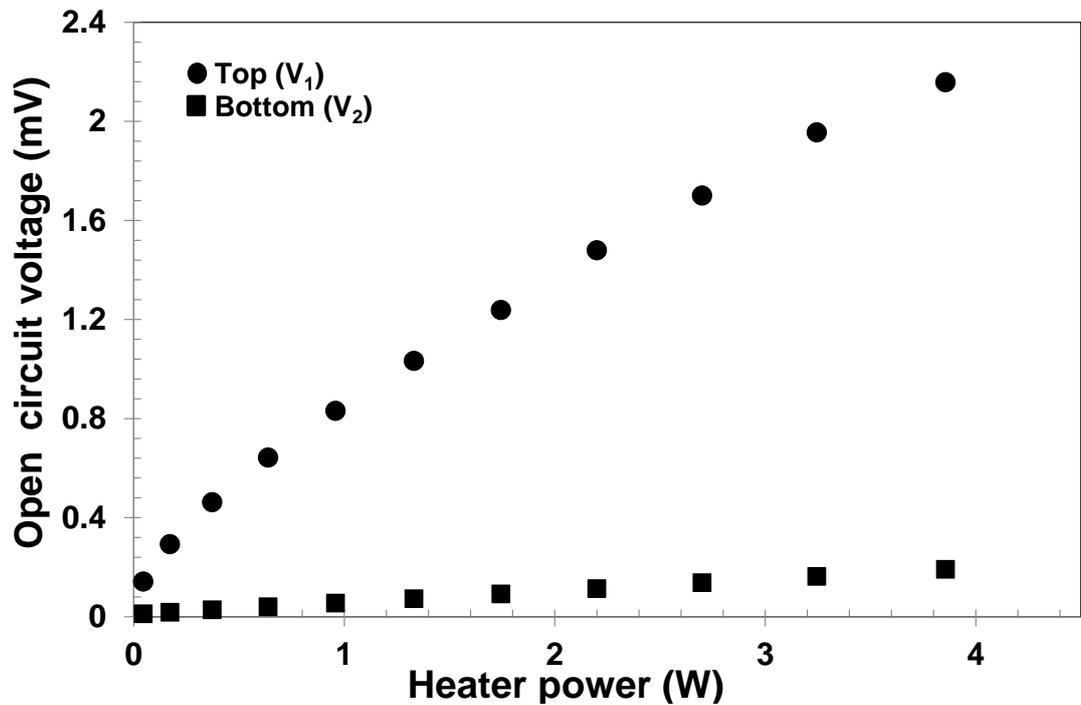


Figure 6.9: Comparison of voltage readings taken at the positions V_1 and V_2 .

It can be seen in Figure 6.9 that there is a significant improvement in the voltage readings obtained for V_1 as compared to V_2 . It was also observed during the course of the experiment that the corresponding voltage reading in close circuit connection was still higher for V_1 than V_2 . Conventionally, measurement readings are taken at the bottom of the legs, away from the connecting end as can be seen in reference [4]. This was supposedly to allow all the voltage contributions to be added up. However, from the results obtained in Figure 6.9, it appears not to be the case for the Ge/SiGe material. Hence, further analyses were conducted to observe the contribution from each of the p- and n- legs for the Ge/SiGe material.

The connectors were removed leaving only the legs with the contacts as shown in Figure 6.10. Thereafter, an external contact was created below the substrate using Copper tape and Silver paste. The Silver paste was required to stick the Copper tape to the back of the sample. It was observed that there was continuity between the Copper tape and the p-leg; however, there was no continuity between the Copper tape and the n-leg. An obvious explanation for this is that the n-leg has a non-conducting substrate, while the p-leg has its substrate to be conducting, thereby allowing continuity between the leg and the

copper tape. Thus, Seebeck voltage readings were taken at the positions (a) - (d). The corresponding plots are presented in Figure 6.11 below.

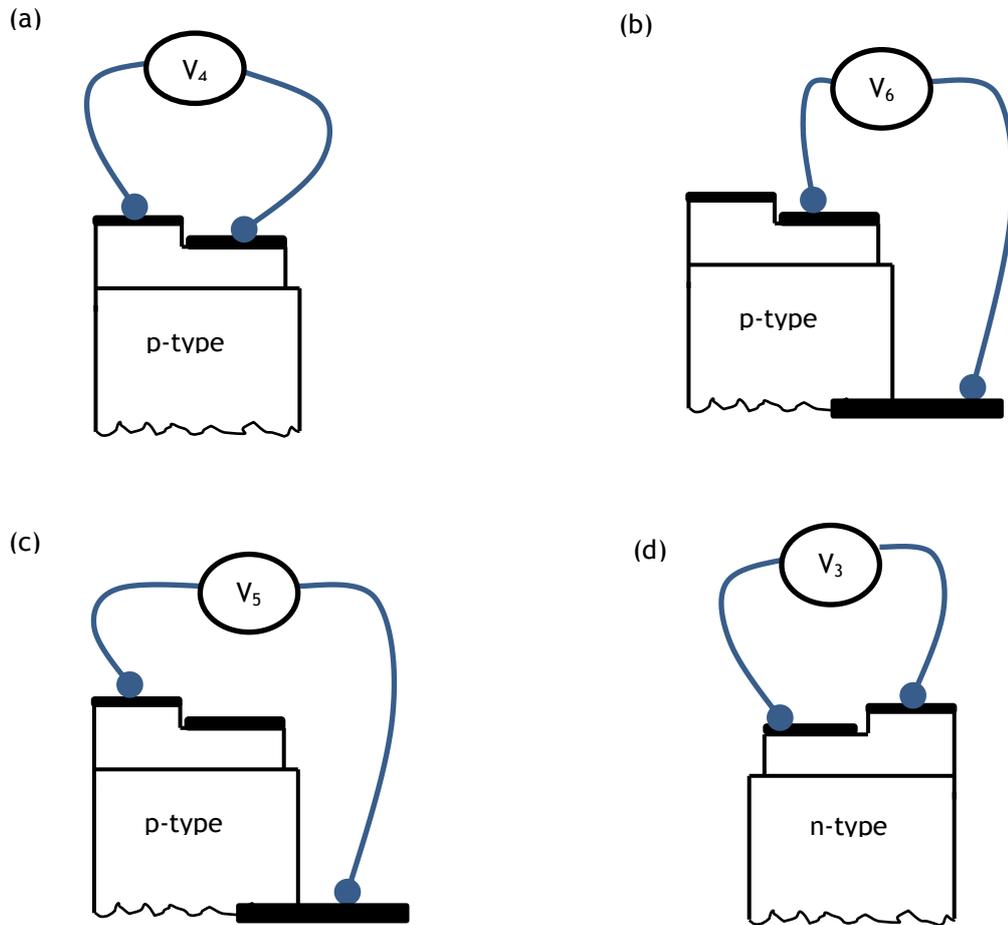


Figure 6.10: Seebeck voltages taken at various position of the fabricated device shown in Figure 6.8 above

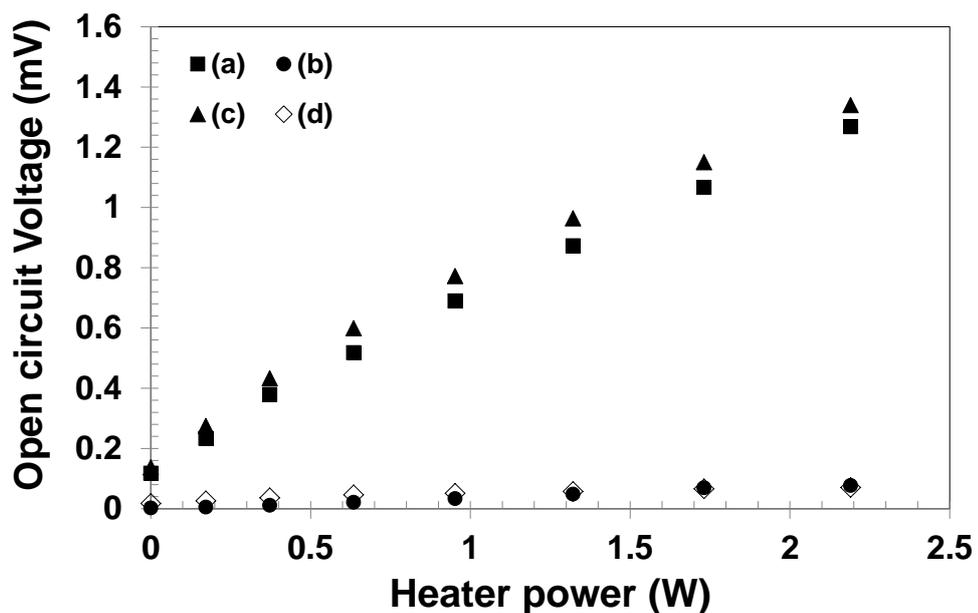


Figure 6.11: Comparison of Seebeck voltages in open circuit for diagrams (a) – (d).

The diagrams labelled (a) - (c) in Figure 6.10 show the various positions for taking Seebeck voltage readings for the p-type material. The corresponding plots in Figure 6.11 show a high voltage output, of 1.26 mW for a heater power of 2.2 W. The same heater power yields a low voltage output of 0.07 mW for (b) and a high voltage output of 1.34 mW for (c). The high outputs recorded for (a) and (c) suggests that there is some voltage contribution from the p-type substrate, apparently because of the continuity between the substrate and the superlattice. The low voltage output obtained for the n-type in (d) is an indication that there is no contribution from the substrate, apparently due to the discontinuity between the substrates and the superlattice. Again, the high voltage output for the p-type in (a) and (c) can be attributed to its high electrical conductivity of 8633 S/m in the superlattice region as compared to the low electrical conductivity of 1834 S/m for the n-type in (d).

The result for (b) does not give any indication of this contribution because of the low voltage output recorded. However, the low voltage output can be attributed to the high electrical resistance between the buffer layer and the silicon substrate. The high electrical resistance will reduce the voltage output generated by the Seebeck effect. These results can be further explained by estimating the Seebeck coefficient for the measurements taken for the p-type in (a) - (c) as presented in Figure 6.12.

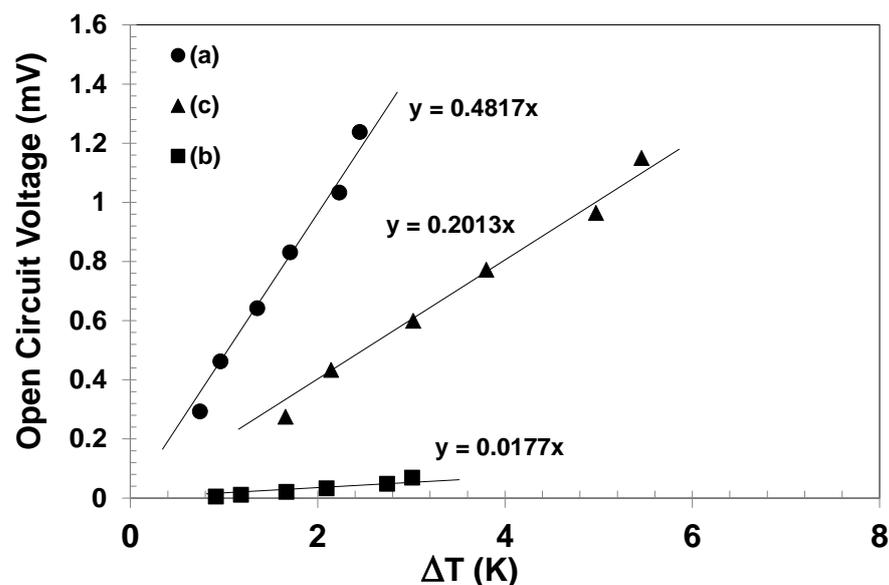


Figure 6.12: Estimation of the Seebeck coefficient for diagrams (a) – (c).

From Figure 6.12 it can be seen that the highest Seebeck coefficient is estimated for (a) with a value of 0.4817 mV/K, and then (c) with a Seebeck coefficient of 0.2013 mV/K. The least is (b) with a Seebeck coefficient of 0.0177 mV/K. Recall that (a) and (c) have almost the same voltage output; with (c) slightly higher than (a) (as shown in Figure 6.11). However (c) has a higher temperature difference than (a) and this resulted to the lower Seebeck coefficient in (c) than in (a). The estimated Seebeck values were obtained by first estimating the temperature difference across the respective layers where the voltage readings were taken in (a) - (c). The temperature differences were estimated using analytical method as shown in the Matlab codes generated in Appendix 3. Thereafter, the measured voltages were divided by the estimated temperature differences to obtain the Seebeck coefficient of the different layers of (a) - (c).

The purpose of estimating the Seebeck coefficients for the different layers is basically to know the degree of contributions from each of the layers. Thus, from the results obtained, it can be seen that the superlattice lattice region contributes most of the Seebeck voltage as shown in (a). The voltage drops along the buffer layer and substrates as shown in (c). The result in (b) suggests that the buffer and substrates contributes the least Seebeck voltages, and this confirms the assumptions made in the FEM discussed in Chapter 5. Also, by using the voltage readings for V_1 in Figure 6.8, the overall Seebeck coefficient for the device is estimated as 0.471 mV/K as shown in Figure 6.13.

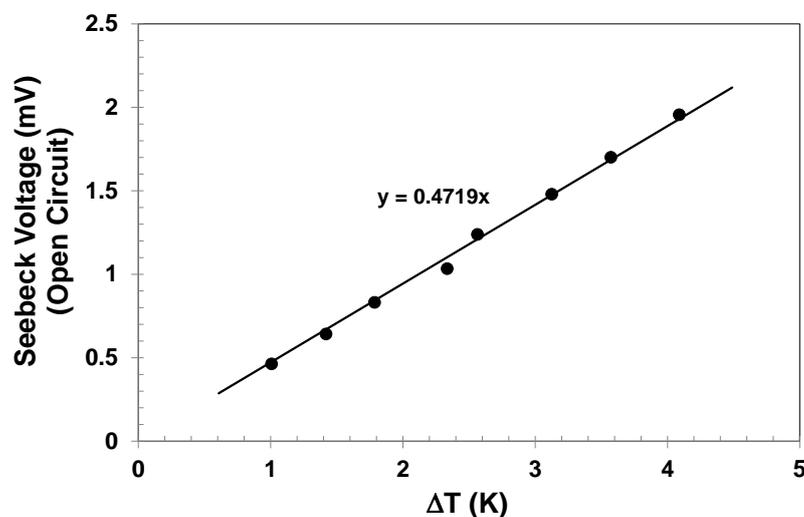


Figure 6.13: Estimation of the Seebeck coefficient for the fabricated device shown in Figure 6.8 above

6.3.2. Evaluation of load voltage and power generating capabilities of the TEG module

Further analyses are performed on the data that was collected from the measurements. These include estimation of the load voltages, power densities and thermal efficiency factor for varying load conditions. The purpose of these analyses is basically for ease of comparison with other published works in the area of thermoelectricity.

Estimation of load voltage and output power generated for varying load conditions

The load voltages were measured and then used to estimate the generated output power for external load resistances of 1.3, 2, 4.3, 15 and 130 Ω . The purpose of this experiment was to see if the Ge/SiGe material is able to generate power. Thus by varying the external load connected across the fabricated device, the load voltages and output power should also vary in line with theory (Recall Figure 5.14 of chapter 5). The output power is estimated based on the equation ($P = V_L^2/R_L$).

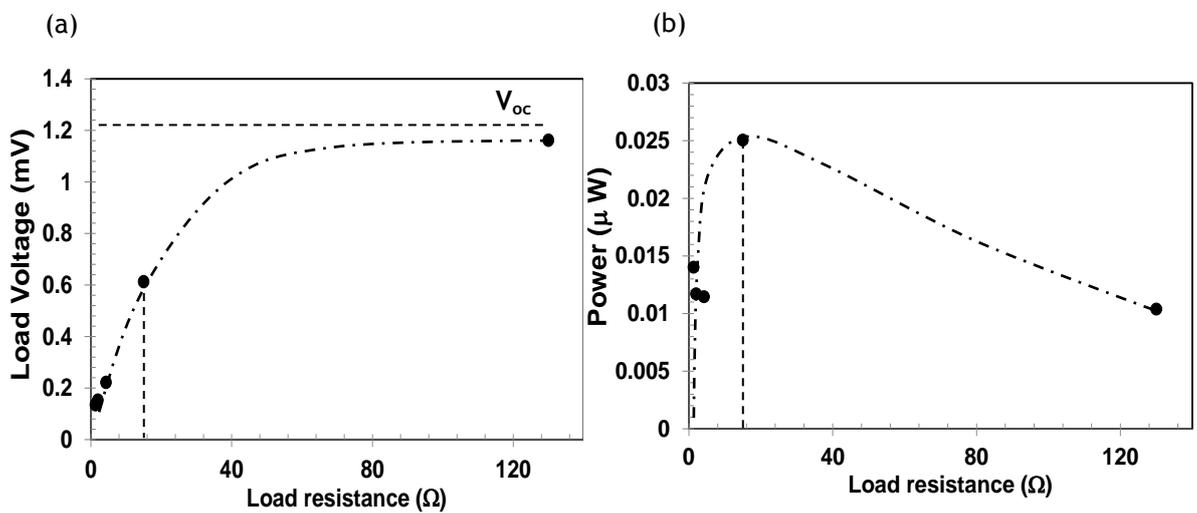


Figure 6.14: Variation of (a) load voltage and (b) power with increase in load at $\Delta T_{meas} = 5.6$ K

Figure 6.14 (a) and (b) presents the plot of varying load voltage and power with increase in external load resistance respectively. In (a), it can be seen that the load voltage increase exponentially as it tends towards the open circuit voltage V_{oc} . The plots suggest an impedance matching at a load resistance of 15 Ω . This implies that the internal resistance of the fabricated device and connections fall

around this value. It is at the impedance matched load that the load voltage is approximately half of the Seebeck voltage and the generated power is at its peak. Next, the power density and thermal efficiency factor of the device is estimated.

Estimation of power density and thermal efficiency factor

The power density is defined as the output power generated per unit area:

$$P_d = \frac{V_L^2}{R_L} * \frac{1}{Area} \quad (6.1)$$

while the thermal efficiency factor is obtained as:

$$\varphi = \frac{P_d}{\Delta T_{meas}^2} \quad (6.2)$$

The power densities, P_d and thermal efficiency factor, φ of the fabricated device is estimated for an external load resistance value of $R_L = 15 \Omega$ because it is at this load that the generated power is maximum.

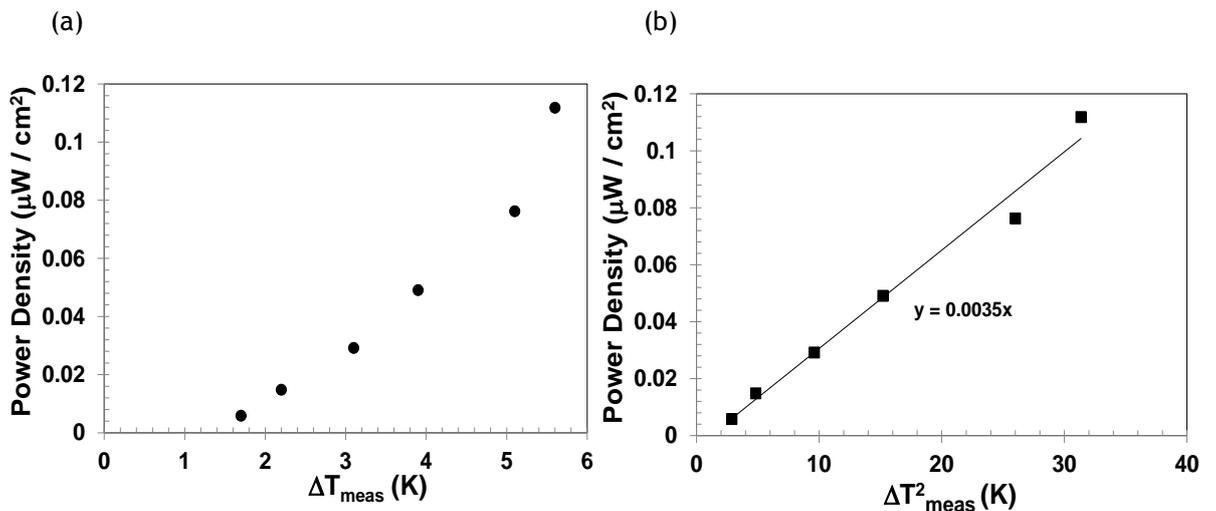


Figure 6.15: Estimation of (a) power density and (b) thermal efficiency factor of the TEG module

From the plots in Figure 6.15 (a), the maximum power density at 5.6 K is estimated as $0.111 \mu\text{W}/\text{cm}^2$ while the thermal efficiency factor obtained for the TEG module is $0.0035 \mu\text{Wcm}^{-2} \text{K}^{-2}$ as shown in (b).

A review of the thermal efficiency factor obtained by various group was conducted by Glatz et al [10]; for example, the thermal efficiency factor of $0.0011 \mu\text{Wcm}^{-2} \text{K}^{-2}$ was obtained by the group in UW Cardiff; $0.091 \mu\text{Wcm}^{-2} \text{K}^{-2}$ for

HSG-IMIT; $0.0352 \mu\text{Wcm}^{-2} \text{K}^{-2}$ for Infineon, $0.089 \mu\text{Wcm}^{-2} \text{K}^{-2}$ for D.T.S Halle, and approximately $7.4 \times 10^{-5} \mu\text{Wcm}^{-2} \text{K}^{-2}$ for Tokai [10]. Although the results obtained in this study are not the best, it is hoped that by fabricating more p- and n- legs, the thermal efficiency factor will improve, since the result obtained is just for a single p- and n- leg. Moreover, the material properties limit the amount of voltage and power that can be generated from the device. As a result of these limitations, a unicouple Ge/SiGe-based TEG module, however optimized, cannot generate significant power to energize low-energy devices e.g. autonomous sensors. Hence, several p-legs and n-legs are needed to yield significant power output. The effect of incorporating more legs on the performance of the performance of the TEG is discussed next.

6.3.3. Effect of multi couples on the device performance

The optimized TEG module d(2) can be extended to incorporate more p- and n- legs. This is achievable by modifying the material design such that an insulating barrier, like SiO_2 is placed between the bottom contact and the buffer layer of Figure 3.4 of Chapter 3. This will help to prevent electrical leakages to the Si substrate; thereby, making the substrate to be non-conducting. Having a non-conducting substrate will make the design of Figure 6.1 (a) feasible; since this was the initial intention for the design and development of the Ge/SiGe 0.224 cm^2 material.

The unicouple TEG has a total surface area of (refer to Figure 6.7). Thus, with the modified material design and the available fabrication technology at the JWNC, multiple p- and n- legs can be created on the same surface area as that of the unicouple. The implication is that the multiple legs will become more compactly arranged than that of the unicouple. Previous work [2] has shown that the approach of making the legs compact improves the power density of the module. The power density is often used as a design parameter to produce as much power as possible from a given heat transfer area [92]. In order to compare results with other literatures, the thermal efficiency factor needs to be calculated from the power density as previously explained. The thermal efficiency factor for multicouples can simply be obtained by multiplying the number of thermocouples, N , with the results obtained for the unicouple. (i.e. $N \times$ thermal efficiency factor of a unicouple)

Table 6.1 below gives an insight on the performance of the TEG module as the number of thermocouples, N increases.

Table 6.1: Effect of increasing the number of thermocouples on the thermal efficiency factor

N thermocouples	Thermal efficiency factor ($\mu\text{Wcm}^{-2} \text{K}^{-2}$)
1	0.0035 (experiment value)
2	0.007
10	0.035
50	0.175
100	0.35
200	0.7
500	1.75

At 500 multicouples, the thermal efficiency factor scales up to an estimated value of $1.75 \mu\text{Wcm}^{-2} \text{K}^{-2}$. This value is comparable to the literature values presented in Table 2.2 of Chapter 2 as well as the reviewed literatures by Glatz et al [10]. Micropelt [31] values are still the best so far, with fabricated thermocouples of up to 500. It is hoped however that by improving the Ge/SiGe material design and its thermoelectric properties, the thermal efficiency factor of the Ge/SiGe based TEG will significantly improve.

Chapter summary.

This chapter represents the final stage of this research work. This chapter seeks to find optimal designs of the Ge/SiGe -based TEG module that are within the fabrication constraints. The validated FEM is mainly used for this purpose. Optimal designs with respect to the geometrical dimensions of the TEG module were discussed. The geometry of the TEG module was varied with respect to the top and bottom substrate, overall surface area and height of the p- and n- legs, represented by the thickness of the superlattice. Although the simulations were performed based on ideal conditions, the simulations served as pointers to the optimal designs that should be considered prior to fabrication. Such optimal design will not only yield an improved performance but will also be cost effective.

Also discussed in this chapter is the experimental investigation of more efficient Ge/SiGe-based TEG modules. Experiments on the optimal position for taking voltage readings was discussed. It was observed that taking measurement at the surface of the legs is more preferable than at the bottom. Hence subsequent voltage readings were taken at the surface. Experiments were conducted for open and close circuit connections. The open circuit voltages and temperature difference across the superlattices were used to estimate a Seebeck coefficient of $471.9 \mu\text{V/K}$ for the TEG module. The voltages in close circuit were used to estimate the power density and thermal efficiency factor of the TEG module. At impedance matched load of 15Ω and ΔT_{meas} of 5.6 K , a power density of $0.111 \mu\text{W/cm}^2$ and thermal efficiency factor of $0.0035 \mu\text{Wcm}^{-2} \text{ K}^{-2}$ was obtained. The results obtained were compared with previous published works. Based on this comparison, it was suggested that as future work, the TEG module should be extended to multiple legs in order to yield better performances.

7. Conclusion and Recommendations

7.1. Conclusion of Thesis

This thesis reports investigations on the combination of Finite Element Modelling (FEM) and experimental observations to design and fabricate an optimized Ge/SiGe based thermoelectric generator. The motivation for embarking on this thesis is that previous studies [6, 7] have shown that the Ge/SiGe material has favourable thermoelectric properties such as high Seebeck coefficient and low thermal conductivity. The Ge/SiGe material used in this study is a novel 2D Ge/SiGe superlattice thermoelectric material, that was developed as part of a Green Silicon project, with the intention of building micro-fabricated TEGs that can power commercial sensors with ratings of up to 3mW [18]. Therefore, this thesis examines the following questions:

1. What significant role does FEM play in analysing the Ge/SiGe material and the Ge/SiGe based TEG module?
2. Can the novel Ge/SiGe material generate power when used as a TEG?
3. How do the results of the Ge/SiGe-based TEG compare or contrast with other literatures in this field?

7.1.1. What significant role does FEM play in analysing the Ge/SiGe material and the Ge/SiGe based TEG module?

Material characterization technique has been conducted in previous studies [6, 7] in order to ascertain the quality of the developed Ge/SiGe material. The quality of thermoelectric materials in general is evaluated based on the ZT and power factor. The figure of merit requires knowledge of the thermoelectric properties: α , σ and κ . To this end, a heat-test measurement technique has been developed to measure simultaneously the Seebeck coefficient, α , and thermal conductivity, κ , of the Ge/SiGe material [6, 7]. A major limitation of this technique is that any physical connection to the thermometers or heaters produces undesirable heat paths that can introduce significant errors in the estimation of these two properties. Hence, the first major task of the present research work is to evaluate the heat-test measurement technique using Finite Element Model (FEM).

FEM plays a significant role in the sense that it can be used to complement/validate experimental results. For example, the design of the Ge/SiGe material is such that it comprises of multiple layers. From the bottom to the top are the following layers: the silicon substrate, buffer layer, bottom contact, Ge/SiGe superlattice and top contact layer. The Seebeck coefficient of the material is estimated by measuring the temperature and voltage readings between the top and bottom surface of the Ge/SiGe superlattice. The ratio of the voltage to the corresponding temperature difference across the Ge/SiGe superlattice gives the Seebeck coefficient of the material.

The top surface is easily accessible for measurement but the bottom surface is not accessible by design and hence, in the measurement technique that was developed [6, 7], the temperature of the bottom surface had to be estimated using measurements at the bottom-side of the Ge/SiGe specimen. In the present research work, FEM was used to estimate the temperature readings at the desired location, which is the bottom surface. Furthermore, the bottom side temperatures were also estimated via the FEM so as to provide a means of validating the experimental estimates of the thermoelectric properties of the Ge/SiGe superlattice. Thus, the voltage results obtained from FEM were compared against the experimental results [6, 7] for both bottom surface and bottom sides.

There was good agreement between FEM voltage readings taken at the bottom side and experimental results. This is expected since the experimental results had to be measured at the bottom side because of inaccessibility of the bottom surface. A second FEM voltage reading was then taken at the bottom surface and the results obtained from the FEM were also compared with the experimental results measured at the bottom side. A maximum deviation of 21% for the voltage measurements was observed. This result is expected since the deviation is due to the difference in position where the measurement readings were taken. The findings of this analysis therefore suggest that thermal measurements should be performed together with modelling to ensure accuracy of results. Moreover, the FEM can be seen to play a significant role by complementing the experimental technique [6, 7] developed for material characterization purpose.

A second FEM was developed taking into consideration the experimental conditions and constraints of the micro fabricated Ge/SiGe-based TEG. It is important to note that this second FEM was developed at the module level while the first FEM was developed at the material level. The FEM results were evaluated using Wu's theoretical maximum for irreversible TEGs [54]. The results obtained revealed that the FEM produces performances that are very close to the theoretical maximum as predicted by Wu's models. This implies that the FEM for the Ge/SiGe-based TEG module is reliable and can be used for cost-effective design and optimisation of high performance TEGs. Hence, evaluation of FEM results using analytical modelling techniques such as Wu's method [54] is recommended.

The FEM for the Ge/SiGe-based TEG module was used to conduct parametric studies in order to investigate the optimum dimensions for the TEG. The main goal of developing this optimal design is to maximize the power generating capability while minimizing the total volume of materials used for fabricating the TEG module. Dimensional parameters of the TEG module examined include the top and bottom substrate, the overall surface area and height of the p- and n- legs represented by the thickness of the superlattice. It was observed that reduction of the top and bottom substrates as well as reduction of the overall cross sectional area of the TEG yielded improved performance. However, increase in the thickness of the superlattice proved to yield better results than a smaller thickness. These observations are in conformity with other published work on optimal design of TEGs [87 - 89]. Although the simulations were performed based on ideal conditions (i.e. assuming there are no thermal or electrical contact resistances) the simulations serve as guides for the optimal design of microfabricated superlattice-based TEGs. Such optimal designs will not only yield an improved performance but will also produce cost effective TEGs.

Finally, the FEM was used to conduct further analyses such as: showing the effect of incorporating a heat sink and the effect of thermal contact boundary on the performance of the TEG module. The simulations showed that the inclusion of a heat sink will help to dissipate most of the heat away from the cold junction side of the TEG module as the hot junction temperature increases. This will help to improve the temperature difference across the TEG.

FEM was also used to simulate the effect of thermal contact resistance between the bottom surface of the TEG module and the connecting surface of the heat sink. In reality, the mounting of a heat sink onto a device or vice versa, may introduce thermal contact resistance. Thermal contact resistances may increase due to the voids created by interface roughness between the two surfaces and this can adversely affect the heat dissipative mechanism of the heat sink. Experimental findings in the literature [81], have suggested that the thermal contact resistances can be minimized by the application of thermal grease or soft metallic foil so as to fill up the air gaps between the heat sink and the bottom of the TEG module.

The FEM was used to show the effect of electrical contact resistances on the performance of Ge/SiGe-based TEG module. The simulation results showed a significant reduction of approximately 50% in the load voltage for the device with contact resistance as compared to the ideal device without contact resistance. The results therefore show that contact resistance are undesirable and does affect the performance of the TEG.

Further FE simulation analysis was conducted to evaluate the effect of external load resistance on the load voltage and generated output power. The results showed that at impedance matched loads (i.e. internal resistance equals external load resistance), the load voltage is approximately 50% of the open circuit voltage, which is confirmed by circuit theory analysis. The results also showed that the maximum power from the TEG is achievable at impedance matched loads.

7.1.2. Can the novel Ge/SiGe material generate power when used as a TEG?

A step-by-step description of the fabrication processes used in building the Ge/SiGe based TEG is presented in this study. The basic fabrication processes include: photolithography, etching, metallisation, bonding and continuity test. The generating capability of the fabricated device was tested using the following measuring instruments: Peltier heater, four-terminal probe instrument and commercial thermocouples (type-T). Thermal and Seebeck voltage measurement require some precautions to ensure accuracy result. The precautions considered

during the course of taking the measurements in this research work include the following:

- The thermocouples used for the temperature measurements were checked manually to ensure that they are functioning. Also labels were used to avoid confusion when taking readings for the hot and cold side temperatures.
- The needles of the voltmeter should be properly fixed on the fabricated TEG module to measure the generated Seebeck voltage. In order to confirm that the needles are properly fixed, an approximate value of 0.00 should be seen on the voltmeter, since there is no temperature difference created at the onset.
- About 2mins wait period should be given to allow the system to stabilize before taking any reading.

The results obtained revealed a poor performance in the Ge/SiGe material used in building the TEG module. Thus, a second experiment had to be conducted using a more efficient Ge/SiGe material to fabricate the TEG module. The second experiment yielded far better results than the first because of two major reasons: the material used for the first experiment had an estimated ZT of 0.0055 while that of the second material was 0.03288. It has been shown in the literature [4] that materials with higher ZTs are more efficient and yield better performances in TEGs. A second reason is that the TEG of the second experiment was fabricated taking into consideration the optimal design that was developed by the FEM in this study. The first experiment was conducted mainly on trial and error basis to ascertain the generating capability of the fabricated Ge/SiGe-based TEG.

The results obtained from the second experiment yielded far better than that of the first experiment. The second experiment estimates a Seebeck voltage $471.9 \mu\text{V}/\text{K}$ and thermal efficiency factor of $3.5 \times 10^{-3} \mu\text{W}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$, while the first experiment estimates a Seebeck voltage $265.91 \mu\text{V}/\text{K}$ and thermal efficiency factor of $3.245 \times 10^{-5} \mu\text{W}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$. This shows that utilization of a more efficient material as well as performing optimization analyses will help to improve the performance of the TEG module, as would be expected.

7.1.3. Comparison of results with other literatures

The results obtained were compared with previously published works stated in Table 2.2 of Chapter 2 and studies reviewed by Glatz et al [10]. The key parameter used in evaluating the performance of TEGs is the power density, which is often used as a design parameter to produce as much power as possible from a given heat transfer area [92]. In order to compare results of the present study with some other studies, the thermal efficiency factor had to be calculated from the estimated power density. The thermal efficiency factor is defined as the power density generated per squared temperature difference across the TEG.

As earlier stated, the thermal efficiency factor obtained for the second experiment of this study is $3.5 \times 10^{-3} \mu\text{Wcm}^{-2}\text{K}^{-2}$. The review of Glatz et al [10] shows thermal efficiency factors of the following groups:

UW Cardiff: $1.1 \times 10^{-2} \mu\text{Wcm}^{-2}\text{K}^{-2}$; Tokai: $7.4 \times 10^{-5} \mu\text{Wcm}^{-2}\text{K}^{-2}$; HSG-IMIT: $9.1 \times 10^{-2} \mu\text{Wcm}^{-2}\text{K}^{-2}$; Infineon: $3.52 \times 10^{-2} \mu\text{Wcm}^{-2} \text{K}^{-2}$; D.T.S Halle: $8.9 \times 10^{-2} \mu\text{Wcm}^{-2}\text{K}^{-2}$ [10]. Also, the results presented in Table 2.1 of Chapter 2 showed that Micropelt [31] has the highest thermal efficiency factor of $2.4 \mu\text{Wcm}^{-2} \text{K}^{-2}$.

Based on these comparisons it is suggested that future work can focus on extension of the TEG module to incorporate multiple thermocouples (i.e. multiple p- and n-legs) for the purpose of yielding better performances. The thermal efficiency factors envisaged with increase in the number of thermocouples is presented in Table 6.1 of Chapter 6. The results presented in Table 6.1 showed that at 10, 100 and 500 thermocouples, the thermal efficiency factor will be 0.035, 0.35 and $1.75 \mu\text{Wcm}^{-2}\text{K}^{-2}$ respectively.

7.1.4. Limitation of work

The research work reported in this thesis was constrained by a number of limitations:

One of the main challenges encountered was that the silicon substrate of the p-type Ge/SiGe material was found to be conducting resulting in the passage of

leaked current from the superlattice layer to the substrate. The consequence of this is that when multiple thermocouples are created there will be short-circuiting of the thermoelectric legs resulting in a very low power output. This reason necessitated the limitation of the TEG design used in the present study to a single thermocouple. Fortunately, an FEM of the single thermocouple TEG was developed and validated using experiments. The FEM for the single thermocouple TEG can be readily modified to incorporate multiple thermocouples and the latter can be simulated to obtain estimates of the power output in the absence of short circuiting. Most importantly, this thesis has been able to show that the novel Ge/SiGe is capable of generating power and this gives hope to designers and developers of these materials that further improvements can be achieved.

In typical applications of TEG, waste heat is normally harnessed to heat up the hot-side of the TEG whereas the cold-side may be connected to a heat sink or allowed to maintain surrounding temperature. It is this temperature difference that produces the required voltage in the TEG. Hence, to replicate this effect in the fabricated TEG module, a Peltier heater is used to heat up the hot-side of the TEG while the cold side is exposed to air, initially at room temperature. The TEG module is made to sit on top of the Peltier heater, which heats up the device from the bottom upwards. Application of the heat from the bottom upwards was found to be preferable than from upwards downwards because the former gave a more uniform heat distribution than the latter. It was difficult to obtain a uniform heat distribution from the upward-downward approach because of the large size of the thermoelectric legs. However, the consequence of using the preferred option, which is the bottom-upward approach, is that it became difficult to incorporate the heat sink. The heat sink ought to be placed on top of the TEG module in order to maintain the cold side temperature of the device, while the device is heated from the bottom. However, the size of the TEG module is very small and fragile compared to the size and weight of the heat sink.

Another limitation of this work is that the indium bond used in bonding the p- and n- leg to the electrode has a melting point of about 120°C. The temperature of the heat source, which is applied at the hot end of the TEG module, must

therefore be below 120°C to avoid dislocation of the legs. The consequence of this is that higher temperatures that will yield a significant ΔT across the legs of the TEG module cannot be achieved. Also, the ΔT is limited by the thickness of the legs. The smaller the legs, the smaller the ΔT across it and this will limit the amount of Seebeck voltage that can be generated by the TEG. However, it is not advisable to grow very thick layers of superlattices because of the problems of strain that may result to a crack or dislocation in the material. The strain occurs as a result of lattice mismatch between the alternate combinations of elements that make up the superlattice, in this case the Ge/SiGe. The maximum thickness of the Ge/SiGe superlattice that has been achieved so far is 4 μm .

7.2. Recommendations for future research

One of the limitations of this study is that the substrate of the p-type material was found to be conducting. This constrained the experimental investigations on the Ge/SiGe-based TEG to single thermocouple design. This is because problems of short-circuiting will arise for more than one thermocouple due to the conducting substrate. The layers that make up the Ge/SiGe material from the bottom upwards are: the silicon substrate, SiGe buffer layer, bottom contact, Ge/SiGe superlattice structure and a top contact layer. Hence as future research work, it is recommended that the SiGe buffer layer be grown on an SOI wafer, which has a buried SiO₂ layer. The advantage of this is that the SiO₂ layer will help to provide electrical insulation between leg pairs and this will prevent the problems of short-circuiting.

As future work, the superlattices could be graded or grown with a combination of materials that are most efficient at varying temperature scales. Basically, as the temperature reduces down the leg, the combined thermoelectric materials can be optimised to maximize the temperature gradient across the legs. Further, research work can be done to investigate suitable temperature - dependent materials.

Also, further work can be done to build a high temperature thermoelectric generator using bulk SiGe rather than superlattices. Studies [12, 68] have shown that bulk SiGe can allow for high temperature applications ranging from 300 - 1300 K. Moreover, the issue of strain due to lattice mismatch can be avoided and

hence longer legs up to 10s of micro meter can be grown. In going for higher temperature applications, the following precautions have to be considered. The indium bond needs to be replaced with a material that can allow for a much higher temperature that is over 120°C, for example the use of copper bonding material. It is important to ensure that the fabricated Ohmic contact and interconnect metals do not diffuse but have a combination of good adhesion and a diffusion barrier. Moreover, the automotive applications require cheap devices that can operate at 500°C so bulk SiGe may be ideal. Mass manufacture of TEGs will require cheap materials and SiGe are integrateable with silicon MEMS foundries.

The performance of a TEG in terms of its conversion efficiency and power output can be improved upon by taking into consideration the heat exchange process between the thermopile (i.e. thermocouples that make up the TEG) and its two heat reservoirs: heat source and heat sink. The Carnot efficiency of any heat engine is the maximum efficiency that can be obtained if used in a completely reversible condition. In reality thermodynamically reversible TEGs are impossible to build; hence, real TEGs have an efficiency that is less than the Carnot efficiency. The heat source and heat sink act as external irreversible heat engine which exchanges heat with its surroundings through a finite temperature difference. Internal irreversibility in the thermopile is as a result of the Joulean heating and thermal conduction heat flow. Hence, the external and internal irreversible heat engines need to be thermally impedance matched in order to maximize the conversion efficiency and power output. Analytical expressions have been derived in the literature [89], taking into consideration the concept of thermal impedance matching between the external and internal irreversible heat engines. Thus, clear thoughts about this concept need to be considered for future research work.

The incorporation of a heat sink is essential for the creation of a large ΔT across the TEG module. The module arrangement can be modified such that a heat sink is placed at the bottom of the device (i.e. the TEG module can be made to sit on the heat sink). Then, an external heat source can be applied on top of the TEG module. The size and weight of the heat source should be small such that it becomes easy to place it on top of the TEG module. The creation of multiple

legs must be done in such a way that the surface areas of the legs are in the micro-scale. This way the applied heat can be uniformly distributed across the legs. However, if the legs are large, like the ones fabricated in this study, it will be difficult to create a uniform heat distribution across the legs.

Finally, apart from the α and κ properties, the ZT also depends on the σ property. In this study it was observed that the σ -property of the Ge/SiGe material was quite low and this resulted to the low power output that was generated by the TEG module. Further work could focus on improved design of the Ge/SiGe material to its σ property. Moreover, it would be nice to model the experimental approach [6] adopted in measuring the σ -property since the experimental approach for measuring the α and κ properties has been modelled in this research work. Hence future work can focus on modelling optimal designs, taking into consideration all three properties, for improve performances.

In concluding this study, it is important to highlight the relevance of thermoelectric power generation and how this research work contributes to the wealth of knowledge in this area. Thermoelectric generators basically, are stand-alone devices that find usefulness in very remote regions such as outer space and beneath the ocean. For example, TEGs can be used to power autonomous sensors which can be used in these remote areas, thereby replacing the use of battery cells. Furthermore, by replacing batteries with these energy harvesters, the amount of rare and hazardous material used in the environment is minimized [93]. In general, TEGs are durable and require little or no maintenance because of their solid state property. This makes them suitable for use in remote regions that are difficult to access by humans.

The best material used for building TEGs so far is the $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ material. However, Tellurium is considered to be the 9th rarest element available, it is toxic and volatile at high temperatures. This makes them non-ideal for commercial purposes [1]. Thus, Ge/SiGe material can serve as an alternative to the $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ material. Ge/SiGe material can operate at substantially higher temperatures (>1000 K) than most of the other TE materials [94]. Although these materials have a poor ZT at room temperatures, they could be used for high

temperatures applications such as TEGs for harnessing electrical energy from automobile exhaust. Other advantages include: non-toxicity and integrability with silicon platform, which is mostly used in the semiconductor industry.

This study proves that the novel Ge/SiGe material is an addition to the various state-of-the-art thermoelectric materials that have been developed over the past few decades. Hence, the fabrication of the Ge/SiGe-based TEGs gives a new perspective to power generation at the micro-scale level.

Appendices

Appendix 1

Matlab codes to calculate $\Delta T_{\text{superlattice}}$ for open and close circuits

```

%Determination of effective temp diff across p/n superlattce, DTsup
clc
% Module design parameters for TEG module
N = 1; % Number of p-n couples
% p/n leg design
L = 3.4 * 10^-6 ; % etched Leg length in m
A = (0.14*0.8*10^-4); % Leg area in m^2
Kappan = 26.5; % n-type thermal conductivity in W/mK
Kappap = 5.5; % p-type thermal conductivity in W/mK

Ls = 0.6 * 10^-6 ; % remaining Leg length in m
As = (0.3*0.8*10^-4); % Leg area in m^2
Kappan = 26.5; % n-type thermal conductivity in W/mK
Kappap = 5.5; % p-type thermal conductivity in W/mK

%ohmic contacts
Lcontactp = 100 * 10^-9; % Thickness of ohmic contact for p-type
Kappacontactp=90.7; %thermal conductivity for Ni

Lcontactn = 100 * 10^-9; % Thickness of ohmic contact for n-type
Kappacontactn=429;% thermal conductivity for Ag

%(2) Buffer layer
LBuffer=10*10^-6;
KappaBuffer = 20; % SiGe buffer thermal conductivity in W/mK

%Substrate

SubstrateThick = 530*10^-6; % Substrate thickness in m
SubstrateKappa = 155; % Substrate thermal conductivity in W/mK

%connector
Aconnector = (0.3*0.8*10^-4); % area connector

LInsulator = 100 * 10^-9; % electrical insulator thickness in m for Si3N4
KappaInsulator = 20; % Thermal conductivity of electrical insulator in
W/mK

% Metal
Lconnector_AL = 700 * 10^-9; % Thickness of metal contact between legs in
m
Kappaconnector=237;

%indium
Lbond_Ind =2 * 10^-6; % Thickness of indium bond in m
Kappabond=81.6;%Thermal conductivity for indium
% Material parameters

% Calculate thermal resistances
RTpp = L/(N*A*Kappap); % Thermal Resistance of N p-type legs in parallel
RTnn = L/(N*A*Kappan); % Thermal Resistance of N n-type legs in parallel

RTps = Ls/(N*As*Kappap); % Thermal Resistance of N p-type legs in
parallel

```

```

RTns = Ls/(N*As*Kappan); % Thermal Resistance of N n-type legs in
parallel

RTBuffer = LBuffer/(N*As*KappaBuffer); % Thermal Resistance of the buffer
RTSubstrate = SubstrateThick/(As*SubstrateKappa); % Thermal Resistance of

RTbond = Lbond_Ind/(N*A*Kappabond);
RTconnector_leg = Lconnector_AL/(N*Aconnector*Kappaconnector);

RTohmicp=Lcontactp/(N*A*Kappacontactp);
RTohmicn=Lcontactn/(N*A*Kappacontactn);

RTp=RTpp+RTps+RTBuffer+RTSubstrate+RTbond+RTohmicp+RTconnector_leg;
RTn=RTnn+RTns+RTBuffer+RTSubstrate+RTbond+RTohmicn+RTconnector_leg;

RTLegs = 1/((1/RTp)+(1/RTn)); % Thermal resistance of the TEG
legs+subs+buffer+ohmic+bond

RTconnector = Lconnector_AL/(N*Aconnector*Kappaconnector); % Thermal
Resistance of the Aluminium connector
RTbond = Lbond_Ind/(N*Aconnector*Kappabond);
RTInsulator = LInsulator/(Aconnector*KappaInsulator); % Thermal
Resistance of insulator
RTSubstrate_connector = SubstrateThick/(Aconnector*SubstrateKappa); %
Thermal Resistance of

RT = RTLegs+RTInsulator+RTbond+RTconnector+RTSubstrate; % Total thermal
resistance of module

%open circuit temperature measurement
RTsup_leg = 1/((1/RTpp)+(1/RTnn)); % Thermal resistance of the TEG legs

DeltaT_op=
[1.3784,1.3436,1.9674,1.9282,2.2562,2.2424,2.477,2.0184,2.2896,2.078,2.87
96,2.718,2.8558,3.9858,3.9298,4.8284,4.1552,3.807,4.1142,3.3738,5.3874];
% linspace(1,20,49*4); % Delta T in K
Qop=DeltaT_op./RT;
DTsup_op=Qop.*RTsup_leg;
figure(1)
plot(DeltaT_op,DTsup_op);
xlabel('Delta T (K)');
ylabel('DTsuperlattice T (K)');

%close circuit temperature measurement
RTsup_leg = 1/((1/RTpp)+(1/RTnn)); % Thermal resistance of the TEG legs

DeltaT_cl=
[1.10,1.92,1.77,2.89,2.78,3.27,3.09,3.20,3.23,4.21,4.43,6.50,7.40,8.00,9.
04,9.71,9.65,9.47,9.20,12.3,13.1]; % % Delta T in K
Qcl=DeltaT_cl./RT;
DTsup_cl=Qcl.*RTsup_leg;
figure(2)
plot(DeltaT_cl,DTsup_cl);
xlabel('Delta T (K)');
ylabel('DTsuperlattice T (K)');

```

Appendix 2

Matlab codes to determine theoretical maximum limit of performance for Ge/SiGe-based TEG module

```
% Analytical modelling of Ge/SiGe TEG using Wu's method
function solveeqs()
clc
global alpha r R AH UH TH TL;% global is used to avoid repeating local
variables for each function.
guess=[1, 400 350];% make an initial guess for [I Thj Tcj] i.e. [current
hot-side-temperature cold-side-temperature]
[result, fval, exitflag, output]
=fsolve(@eqns,guess); %print solution and number of iterations

% Display the solutions of the simultaneous equation for [I Th Tc]

Isc=result(1)% Display the first result in the matrix named guess. This
gives the short circuit current
Thj= result(2);
Tcj= result(3);

Voc=alpha*(result(2)-result(3))% Display result for Open circuit voltage

VL= Isc*R % calculate Load voltage across the external load R=1.5 ohms

VL1=Voc-Isc*(R); % or calculate the load voltage using circuit theory
analysis.

PL= Isc^2*R

output
end

function fcns=eqns(z)
global alpha R AH AL UH TH TL K UL;
%Define material property for Seebeck coefficient
a_pn= 180*10^-6; % effective Seebeck coefficient for thermocouple (i.e.
ap+an)

a_Al=3.5*10^-6; a_Ag=6.5*10^-6; a_Ni=-(15*10^-6); a_in=6.5*10^-6;

a_m=((3*a_Al)+a_Ag+a_Ni+(3*a_in));%Total Seebeck coefficient for the
individual metals

alpha= a_pn+a_m;% Total Seebeck coefficient of the TEG-module

%Define resistances

R=1.2;

%heat transfer coefficient of heat source and heat sink
% silicon acts as the heat source and heat sink
Si=(155*530*10^-4)/(0.3*0.8);

UH= Si;% + Al+SiN3+In;% W/mK*m/m^2 =W/m^2K so 155*530*10^-
4/(0.3*0.8)+2.37*0.7*10^-4/(0.3*0.8)+0.20*0.2*10^-
4/(0.3*0.8)+0.816*2*10^-4/(0.3*0.8) all units in cm si + Al metal +SiN3
AH=(0.3+0.3)*0.8;%Total surface area below the two legs directly where
the heat is applied.
```

```

DT=10; % temperature difference measured from experiment
%DT= [10, 20, 30, .....100]% change values for DT.

TH=DT+298.15;% unit in Kelvin
TL=298.15; % unit in Kelvin

UL= Si;
A_L= 0.3*0.8; % Total area at top of p and n-leg.

%Define thermal conductivities
kn=0.2613; kp=0.05;% W/cmK

Ln=(3.5)*10^-4; An=0.8*0.14;%Length and area of n-leg; unit in cm and
cm^2 respectively
Lp=(3.5)*10^-4; Ap=0.8*0.14;% Length and area of p-leg

Kn=(kn*An)/Ln;
Kp=(kp*Ap)/Lp;

K=Kn+Kp; %effective thermal conductivity

C=z(1);% C= current
Thj=z(2); % Temperature at the hot junction of the TEG
Tcj=z(3);% Temperature at the cold junction of the TEG

%Simultaneous equations

fcns(1)=(alpha*(Thj-Tcj)/(2*R))-C;%
fcns(2)=(UH*AH*TH-2*R*C*(K/alpha)+0.5*C^2*R)/(alpha*C+UH*AH)-Thj;
fcns(3)=(UL*AL*TL+2*R*C*(K/alpha)+0.5*C^2*R)/(UL*AL-alpha*C)-Tcj;

end

```

Appendix 3

```

%Determination of effective temp diff across p/n superlattice, DTsup
clc
% Module design parameters for TEG module
N = 1; % Number of p-n couples
% p/n leg design
L = 6.8 * 10^-6 ; % etched Leg length in m
A = (0.3*0.35*10^-4); % Leg area in m^2 (Total surface area of both legs
is approximately 0.224 cm2
Kappan = 4.55; % n-type thermal conductivity in W/mK
Kappap = 5; % p-type thermal conductivity in W/mK

%Ohmic contacts
Lcontactp = 100 * 10^-9; % Thickness of ohmic contact for p-type
Kappacontactp=90.7; %thermal conductivity for Ni

Lcontactn = 100 * 10^-9; % Thickness of ohmic contact for n-type
Kappacontactn=429;% thermal conductivity for Ag

% Buffer layer
LBuffer=8*10^-6;
KappaBuffer = 20; % SiGe buffer thermal conductivity in W/mK

%Substrate

SubstrateThick = 530*10^-6; % Substrate thickness in m
SubstrateKappa = 155; % Substrate thermal conductivity in W/mK

%connector
Aconnector = (0.3*0.35*10^-4); % area connector

LInsulator = 100 * 10^-9; % electrical insulator thickness in m for Si3N4
KappaInsulator = 20; % Thermal conductivity of electrical insulator in
W/mK

% Metal
Lconnector_AL = 700 * 10^-9; % Thickness of metal contact between legs in
m
Kappaconnector=237;

%indium
Lbond_Ind =3 * 10^-6;% Thickness of metal contact between legs in m
Kappabond=81.6;%Thermal conductivity for indium
% Material parameters

% Calculate thermal resistances
RTpp = L/(N*A*Kappap); % Thermal Resistance of N p-type legs in parallel
RTnn = L/(N*A*Kappan); % Thermal Resistance of N n-type legs in parallel

% RTps = Ls/(N*As*Kappap); % Thermal Resistance of N p-type legs in
parallel
% RTns = Ls/(N*As*Kappan); % Thermal Resistance of N n-type legs in
parallel

RTBuffer = LBuffer/(N*As*KappaBuffer); % Thermal Resistance of the buffer
RTSubstrate = SubstrateThick/(As*SubstrateKappa); % Thermal Resistance of

RTbond = Lbond_Ind/(N*A*Kappabond);
RTconnector_leg = Lconnector_AL/(N*Aconnector*Kappaconnector);

```

```

RTohmicp=Lcontactp/(N*A*Kappacontactp);
RTohmicn=Lcontactn/(N*A*Kappacontactn);

RTp=RTpp+RTBuffer+RTSubstrate+RTbond+RTohmicp+RTconnector_leg;
RTn=RTnn+RTBuffer+RTSubstrate+RTbond+RTohmicn+RTconnector_leg;

RTLegs = 1/((1/RTp)+(1/RTn)); % Thermal resistance of the TEG
legs+subs+buffer+ohmic+bond

RTconnector = Lconnector_AL/(N*Aconnector*Kappaconnector); % Thermal
Resistance of the Aluminium connector
RTbond = Lbond_Ind/(N*Aconnector*Kappabond);
RTInsulator = LInsulator/(Aconnector*KappaInsulator); % Thermal
Resistance of insulator
RTSubstrate_connector = SubstrateThick/(Aconnector*SubstrateKappa); %
Thermal Resistance of

RT = RTLegs+RTInsulator+RTbond+RTconnector+RTSubstrate; % Total thermal
resistance of module

DeltaT= [1.7, 2.2, 3.1, 3.9, 5.1, 5.6]; %temperature measured top and
bottom % linspace(1,20,49*4); % Delta T in K

%Estimate temperature difference across superlattice for diagram (a)
Q=DeltaT./RT;
DTsup_pleg=Q.*RTpp; % estimation of temperature difference across
superlattice for p-leg
figure(1)
plot(DeltaT,DTsup_pleg);
xlabel('Delta T (K)');
ylabel('DTsuperlattice_pleg T (K)');

%Estimate temperature difference across buffer and substrate (b)
Q=DeltaT./RT;
DTbuffer_substrate_pleg=Q.*(RTBuffer+RTSubstrate); % estimation of
temperature difference across buffer and substrate for diagram (b)
figure(2)
plot(DeltaT,DTbuffer_substrate_pleg);
xlabel('Delta T (K)');
ylabel('DTbuffer+substrate T (K)');

%Estimate temperature difference across superlattice buffer and substrate
(c)
DTsuperlattice_buffer_substrate_pleg=Q.*(RTpp+RTBuffer+RTSubstrate); %
estimation of temperature difference across buffer and substrate for
diagram (b)
figure(3)
plot(DeltaT,DTsuperlattice_buffer_substrate_pleg);
xlabel('Delta T (K)');
ylabel('DTsuperlattice + buffer+substrate T (K)');

```

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