INVESTIGATION OF SILICON-CADMIUM SULPHIDE HETEROJUNCTION PHOTODETECTORS

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SUMMARY

Heterojunction photodetectors have been fabricated by the electron-beam evaporation of compound CdS onto thermally cleaned silicon substrates at pressures less than 10^{-7} torr in an oil free vacuum system. Quantum efficiencies of up to 40% at 600 nm were obtained with the appropriate Si doping conditions. The response time of the photodetector was approximately 0.5 μs.

The investigation entailed studies of film structural and transport properties using transmission electron diffraction, X-ray diffraction and Hall measurements, because it was expected that the CdS film properties have an important bearing on the device characteristics. The silicon substrate doping level was also an important factor determining the heterojunction characteristics.

The formation of a thin SiOx layer which rapidly forms when silicon is exposed to the air was thought to cause poor adhesion of CdS films deposited on silicon. An electron-beam gun was used to heat the silicon substrates up to 1000°C, prior to CdS film deposition, thereby removing the SiOx layer. SiO_2 layers, however, were stable at these temperatures and consequently it was still possible to use oxide masking techniques.

Transmission electron diffraction, a technique suitable for examining thin films (less than 1000Å) can also be used for nucleation studies, while X-ray diffraction is generally used for thicker films (in excess of one micron). The technique of transmission electron diffraction was utilised to examine the structural quality of thin CdS films deposited on (100) oriented silicon. As it was important to examine films grown on silicon itself (rather than say on NaCl) it was necessary to thin the silicon to about 1000Å so that the composite CdS--Si structure was less than 2,000Å thick. A preferential etching technique was developed to

fabricate suitable (100) oriented silicon specimens for examination using the electron microscope. However, CdS films deposited under a range of growth conditions proved to be polycrystalline on (100) oriented Si. X-ray back reflection Laue was then used to examine films deposited on both (100) and (111) oriented Si, as the preferential etching technique was only suitable for the (100) orientation. It was found that epitaxial films grew on thermally cleaned (111) oriented Si at substrate temperatures above 300°C. It was not possible to grow epitaxial films on silicon which was not thermally cleaned. The X-ray results confirmed that only polycrystalline films grew on (100) oriented Si.

The transport properties of the CdS films were investigated using Hall measurements. The Hall mobility increased from 115 cm^2/V-sec for a substrate temperature of 200°C to 315 cm^2/V-sec at 340°C for films deposited on (111) oriented Si. The Hall mobility of films grown on (100) oriented Si was significantly lower i.e. 85 cm^2/V-sec.

Electrical and optical measurements were related to a proposed band model which included the effects of surface states and reasonable agreement was found. Capacitance versus voltage and capacitance versus frequency measurements indicated that traps were present. The optical measurements showed that at least three traps were present at 0.25, 0.41 and 0.83 eV below the CdS conduction band. These traps reduced the quantum efficiency of the heterojunction photodetector and were thought to limit the response time of the device. An approximate method was used to estimate the depletion width in the silicon and relate this to the quantum efficiency.

It is thought that significant improvements may still be possible with better film deposition techniques, resulting in reduced defect and trap densities. A possible application for the devices fabricated using the present technique, is as a heterojunction solar cell. Heterojunctions fabricated from near intrinsic Si ($N_A = 6 \times 10^{12}$ cm^{-3}) were found to have power conversion efficiencies of 12% under A.M.1 conditions.

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INTRODUCTION

The work presented in this thesis is concerned with the evaluation and fabrication of nCdS-pSi heterojunction photodetectors. The main advantage a heterojunction has when compared with a conventional p-n homojunction photodetector is that the junction may be placed deeper in the former than in the latter because of the "window effect". In a heterojunction, as well as the change in conductivity type across the junction, there are also differences in permittivity, refractive index, work function, electron affinity and crystal structure.

Chapter 1 is a general introduction to heterojunction concepts. It relates the different methods of growth to the type of junction which will result i.e. abrupt or graded heterojunctions. The crystal structures found in the CdS-Si system are discussed and the possible consequences of lattice mismatch, interface states and traps are mentioned. An idealised band model of the junction is introduced to show, for example, how the contact potential results from the difference in the work functions of the two semiconductors. The importance of the vacuum level as the reference point for potentials is indicated. The final sections of Chapter 1 give some insight into the optical properties of heterojunctions. A special feature of the heterojunction, the window effect, is discussed and the different idealised band structures which result from the different energy gap and conductivity type configurations are related to the optical properties of the junction.

As the properties of the CdS film clearly have some influence on the performance of the heterojunction it is necessary to consider factors which affect the nature of film growth. The identifiable steps in film growth are discussed in Chapter 2, together with theoretical and experimental results of other research workers, concerning the factors which

promote the epitaxial growth of one material on another.

A theoretical band model is presented in Chapter 3 for the four different silicon substrate doping levels which were used in the experimental work. A simple model, which is an extension of the homojunction band model, is first discussed, then the model is modified by introducing the effects of surface states which are thought to pin the Fermi level at the silicon surface. Expressions are developed and related to the current-voltage characteristics and the optical properties in a later chapter.

Some of the important stages in the processing of the silicon substrate prior to the CdS film growth are discussed in Chapter 4. Oxidation, and diffusion of p-type conductivity layers into silicon are used both for the preparation of the nCdS-pSi heterojunction and for thinned silicon specimens. The silicon is thinned using a preferential etching technique to permit analysis of the CdS film structure using a transmission electron microscope (T.E.M.).

Chapter 5 deals with the technological processes required for the fabrication of an nCdS-pSi heterojunction. The 21 stages involved can be broken down into 8 distinct processes, i.e.: polishing, oxidation, diffusion, photolithography, etching, silicon cleaning in vacuo, evaporation, and bonding. One of the problems associated with the growth of a crystalline material on silicon is the formation of a thin oxide (SiOx) on the silicon surface when silicon is exposed to the air. A thermal cleaning process was used to remove the SiOx under high vacuum conditions ($< 10^{-7}$ torr).

The structural and transport properties of the CdS films grown on silicon are discussed in Chapter 6. X-ray diffraction analysis and a transmission electron microscope, in the diffraction mode, are used to give information about the structure of the CdS films grown on a variety of silicon substrates. It is found that the removal of the SiOx layer

makes it possible to grow epitaxial CdS films at temperatures in excess of 300°C. Hall measurements indicate that there is an increase in the Hall mobility of the film, for increasing values of the substrate temperature maintained during film growth, rising to 315 cm^2/V-sec at 340°C. The mobility increases as the degree of orientation of the film improves.

The main experimental results are presented in Chapter 7 and are compared with the theoretical model developed in Chapter 3. A number of different electrical measurements are made which include current-voltage, photocurrent-voltage, capacitance-voltage, capacitance-frequency, and response time to an optical pulse. The results, in broad agreement with the theoretical model including the effects of surface states, indicate that the silicon substrate doping level determines the photodetection properties of the device. The measurements are used to calculate the barrier potentials, which are found to be in reasonable agreement with those predicted using the theoretical model. There is experimental evidence both from the capacitance-voltage and the photosensitivity-wavelength measurements that traps are present in the CdS film. The position of these traps in the CdS band gap is calculated from the experimental results. The sensitivity of the nCdS-pSi heterojunction as a photodetector is comparable to that of a commercial p-i-n silicon photodiode, i.e. a quantum efficiency of 40% as compared with 38% at 600 nm for the p-i-n photodiode. However the fastest rise time currently obtainable of 0.5 μs does not compare favourably with a typical rise time of 1 ns for a p-i-n photodiode. In general, it is found that heterojunctions fabricated using uncleaned silicon have characteristics less consistent than and inferior to those which have been cleaned at high temperature.

The main conclusions together with suggestions for future work are presented in Chapter 8. It is thought that the molecular beam epitaxy (M.B.E.) technique may be a more suitable method than electron-beam

evaporation of compound CdS to obtain high quality films. One possible application for an nCdS-pSi heterojunction photodetector is as a solar cell. Power conversion efficiencies of up to 12% have been observed under A.M.1. conditions.

CHAPTER 1 BASIC HETEROJUNCTION CONCEPTS

1.1 Introduction

The interface between two different semiconducting materials is commonly called a heterojunction[1], and represents a generalisation of the p-n homojunction obtained in a single material. In a heterojunction the reference point for the potentials is no longer arbitrary. Instead, the vacuum level is chosen as the reference point. Factors such as work function, ϕ, and electron affinity, θ, are used to characterise the transport properties of the heterojunction, while it is the change in Fermi levels which characterises the transport properties in the homojunction case. The barrier potential or diffusion voltage is the difference between the two semiconductor work functions.

The heterojunction structure was first envisaged by Preston[2] in 1950. Gubanov[3,4,5] produced an analysis of heterojunctions with n-n, p-p, and p-n conductivity type combinations. Shockley[6] proposed a circuit device incorporating a change in the magnitude of the forbidden gap in the transition region of a p-n junction. Kroemer[7,8] proposed the use of heterojunctions as a wide-gap emitter to increase the injection efficiency of transistors. Since then, heterojunctions have been extensively studied, and many applications have been proposed, such as the majority-carrier rectifier, the high-speed band-pass photodetector, the beam of light transistor, the tunnel diode and the injection laser.

The experimental investigation of heterojunctions has become possible as a result of the improvements in the techniques used to grow high quality single crystal materials. A heterojunction can be formed by various methods: (i) The interface-alloy technique,[9,10,11] utilises the difference in melting points between the two semiconductors for selective melting and regrowth. This technique requires high temperatures, with the attendant

possibilities of impurity cross-diffusion. Initial ultra-clean surfaces and careful crystal orientation are required.

(ii) The solution-growth technique in which a molten alloy is heated on the surface of a semiconductor thereby melting a small area. The re-crystallised region can then be a derivative material of the original semiconductor, e.g. an alloy containing In on GaAs would result in a recrystallised layer of (GaIn)As. In this technique, temperatures may again be high, risking impurity diffusion. However, since the interface is within the original bulk material, initial surface contamination is not so important.

(iii) Liquid-phase epitaxy is again a high temperature technique and, although risk of contamination can be considerably less than for the methods just described in (i) and (ii), an abrupt junction cannot be guaranteed.

(iv) Vapour-phase epitaxy has been widely used in both closed and open tube forms. The iodide disproportionation reaction for the deposition of Ge is a relatively simple process. The deposition temperature can be relatively low; all that is required is that individual deposited atoms be sufficiently mobile to take up their preferred crystal sites.

(v) Evaporation is a low-temperature technique with virtually no chance of impurity diffusion. However, stoichiometry is often difficult to achieve, for compound semiconductors, due to the frequently large difference in the vapour pressures of the component materials.

A perfect match of lattice constants and thermal expansion coefficients, however, is not normally possible in heterojunctions, and therefore, defects such as interfacial dislocations are generally present at the heterojunction interface[12]. However, Panish and Sumski[13] found that the GaAs - $Al_xGa_{1-x}As$ alloy interface shows a negligibly small number of states. This type of junction is called a graded junction since there is a gradual transition from the semiconductor on one side of the junction to

the semiconductor on the other side of the junction. In contrast, the CdS-Si heterojunction, fabricated by vacuum deposition of CdS on silicon, is called an abrupt heterojunction. Interface states can act as trapping centres and severely limit the device potential in certain cases. Traps or defects in deposited CdS films can also take part in the equilibrium process, in addition to the normal band to band transfer of charge. An additional problem associated with Si is the thin oxide which always forms when Si is exposed to the air.

1.2 Crystal Structure

Most of the elemental group IV, compound group II-VI and group III-V semiconductors belong to the closely related diamond, sphalerite (zinc blende) and wurtzite structures. All three are a result of strongly directional tetragonal covalent bonds. Cadmium sulphide, a II-VI compound, can crystallise either in the wurtzite or sphalerite structures depending on the substrate and the evaporation conditions. The wurtzite structure consists of two interpenetrating hexagonal close-packed lattices, one of which contains the cadmium atoms, while the other contains the atoms of sulphur. The lattices are displaced in the C-direction. When cadmium sulphide crystallises in the sphalerite structure its atomic arrangement consists of two interpenetrating face-centred cubic lattices with cadmium atoms located on one set of sides and sulphur atoms on the other. The displacement lies in the (111) direction of the face-centred cubic cell. The group IV elemental semiconductor silicon has the diamond lattice structure, which can be derived by the substitution of a single type of atom for both types appearing on lattice sites in the sphalerite structure.

The substrate surface plays an important role in determining the crystal structure of the film. Holt and Wilcox[14] found that the vacuum-evaporated epitaxial films of II-VI compounds grew on (100) and (110)

substrate surfaces with the cubic sphalerite structure. The situation is less clear cut on (111) substrates as both the wurtzite and sphalerite structures can match the rotational symmetry of the substrate surface. Which of the two structures grows is probably determined by the growth conditions and the substrate temperature.

1.3 Lattice Mismatch, Interface States and Traps

Figure 1.1 shows the distribution of lattice parameters among the more common semiconductors of the related wurtzite, sphalerite, and diamond structures. The lattice mismatch between the sphalerite form of CdS and silicon is 7% while for the wurtzite form it is 7.7%. It was recognised by Oldham and Milnes[12] that significant misfit inevitably arises when materials of unequal lattice parameters are interfaced. In particular Oldham and Milnes drew attention to the point that interfacial dangling bonds, the consequence of the lattice mismatch, could be expected to provide electrically active interface states acting either as charge traps or as recombination sites. Figure 1.1 shows that there are five groups of materials, each group covering about 1% mismatch, from which closely matched pairs can be selected. This does not mean that it is impossible to obtain epitaxial growth for pairs with significantly larger lattice mismatches. Single-crystal GaAs-InSb heterojunctions with a 14% mismatch have been successfully produced[15] by the interface alloy technique. The three-dimensional case of misfit dislocation in diamond and sphalerite structures has been considered by Holt[16]. He assumes that the structure of a deposited layer is a continuation of that of the substrate. Expressions for dangling bond density are developed which, it must be emphasised, represent an upper limit. Strain in one or both of the crystals may take up some of the lattice mismatch. Another point to consider is the extent to which the remaining dangling bonds are electrically or photoelectrically active. Esaki[17], and Hampshire[18], found that the number of interface

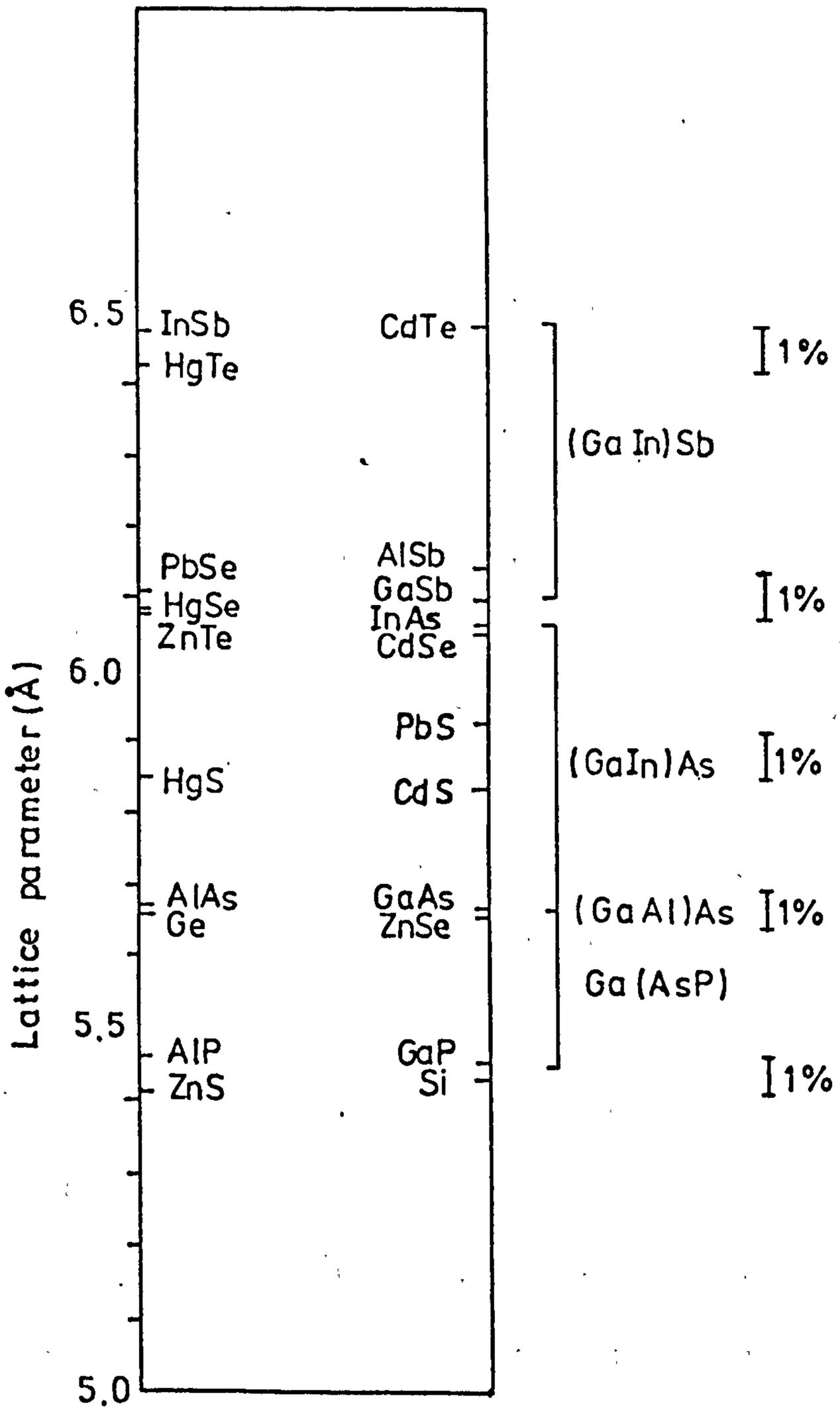


Fig 1.1 Distribution of lattice parameter among the more common semiconductors of the related wurtzite, sphalerite, and diamond structures.

states was about two orders of magnitude less than predicted.

Trapping centres can also be found in the energy gap of semiconductors. These can be due either to impurity levels or to defects in the crystal structure. The fact that a film is epitaxial does not necessarily mean that it is defect-free or that it does not contain any trapping centres. In general, since high quality single crystal silicon substrates were utilised in the work of this thesis, trapping effects in the silicon were restricted to those which result from impurity centres associated with the doping. In contrast, it is defects in the CdS crystal structure, associated with sulphur and cadmium vacancies, which predominantly cause trapping and recombination effects in the CdS films, for the CdS-Si device.

1.4 Idealised Interface Band Profile

Using improved vapour growth techniques, Anderson[1,19] analysed experimentally the basic junction characteristics of Ge-GaAs heterojunction diodes. Figure 1.2(a) illustrates two different isolated semiconductors. The two semiconductors are assumed to have different band gaps (E_g), different dielectric constants (ε), different work functions (ϕ) and different electron affinities (θ). Work function and electron affinity are defined, respectively, as the energy required to remove an electron from the Fermi level (E_F) and from the bottom of the conduction band (E_c) to a position outside the material (vacuum level). The material on the left (subscripted 1) is narrow-gap and p-type, while that on the right has a wider gap and is n-type. Figure 1.2(b) shows that when the two materials are brought into intimate contact, carriers are redistributed throughout the interface in direct analogy with the homojunction case, until a state of thermal equilibrium is reached. The difference in the work functions of the two materials gives the total built-in voltage (V_D). This voltage is equal to the sum of the partial built-in voltages, ($V_{D1}+V_{D2}$),

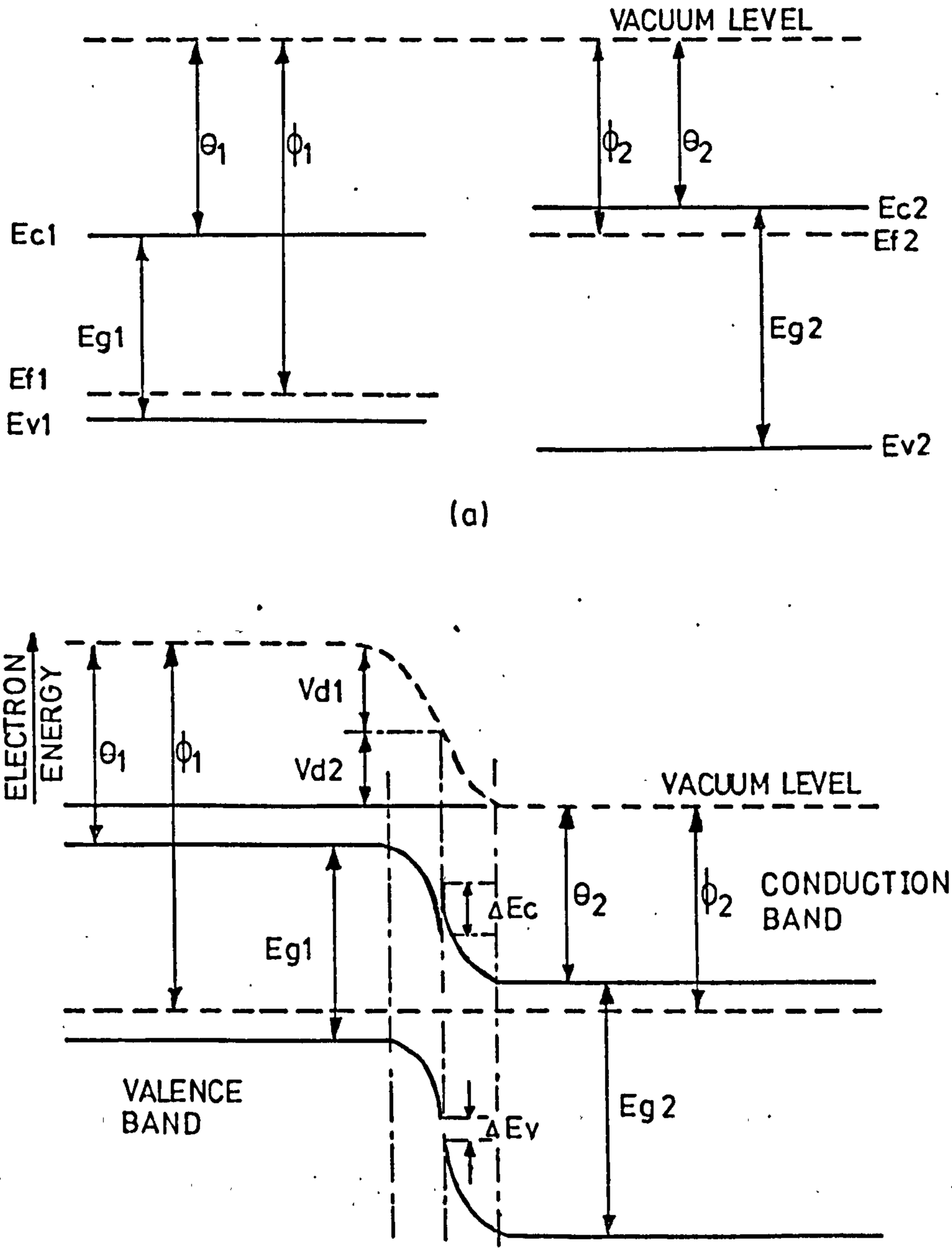


Fig 1.2 Equilibrium band diagram when two semi-conductors in isolation are brought together.[1]

where V_{D1} and V_{D2} are the electrostatic potentials supported at equilibrium by semiconductors 1 and 2, respectively. Since voltage is continuous in the absence of dipole layers, and since the vacuum level is parallel to the band edges, the electrostatic potential difference (ψ) between any two points is represented by the vertical displacement of the vacuum level between these two points. As a result of the difference in the dielectric constants in the two materials, the electrostatic field is discontinuous at the interface. Since the vacuum level is everywhere parallel to the band edges, and is continuous, the discontinuity in conduction-band edges (ΔE_c) and valence band edges (ΔE_v) is invariant with doping, provided that the material is non-degenerate.

Solutions of Poisson's equation, with the assumption of a step junction, are used to give expressions for the transition widths on either side of the interface. The voltage profile in the interface region is determined by solving for the electric field strength (E) on either side of the interface and using the condition that the electric displacement ($D = \varepsilon E$) is continuous at the interface.

This simple model for abrupt heterojunctions, using Shockley's homojunction theory together with a diode emission model, was sufficient to predict the saturation current and current-voltage characteristics of Ge-GaAs heterojunctions. This model ignored effects due to interface states, this being justifiable since the lattice mismatch was small. Anderson indicated that his model would also be modified by tunnelling effects, image effects, and carrier generation and recombination.

Later work made use of the band structure proposed by Anderson, but with modifications to make allowance for other effects such as those due to interface states.

A special feature of a heterojunction is that it permits the formation of junctions between semiconductor materials that cannot be doped to give

both p-type and n-type conductivity. Work has been carried out on this problem with II-VI compound semiconductors, in most of which it is difficult to achieve significantly p-type conductivity because of compensation mechanisms.[20,21,22] There are two basic categories of heterojunction, as far as conductivity type is concerned, anisotype and isotype. Anisotype is the name given when the two materials used to make a heterojunction are of different conductivity types. Isotype describes the situation where the two materials are of the same conductivity type. Figure 1.3[23] describes the idealised band structure for all combinations of isotype and anisotype heterojunctions. The effects of changes in doping levels are also shown.

1.5 Optical Properties of Heterojunctions

The "window effect" is an important feature of a heterojunction photodetector. This effect permits the junction to be placed deeper from the surface than in a homojunction without greatly reducing efficiency. The deeper junction leads to reduced surface-recombination losses and sheet-resistance losses. The performance is adversely affected, of course, if the interface has a high recombination velocity. The light is usually incident on the front surface of the wide-gap material of the photo-detector. Photons having energies greater than the forbidden energy gap of the wide-gap semiconductor ($E_p > E_{g1}$) are absorbed rapidly. Those photons with energies smaller than the forbidden energy gap of the narrow-gap material ($E_p < E_{g2}$) are transmitted through the whole structure. Intermediate energy photons however ($E_{g1} > E_p > E_{g2}$) are transmitted to the interface, where they are absorbed in the transition region of the narrow-gap material. Ideally, each absorbed photon generates an electron-hole pair which, by virtue of the opposite charge signs, separates in the

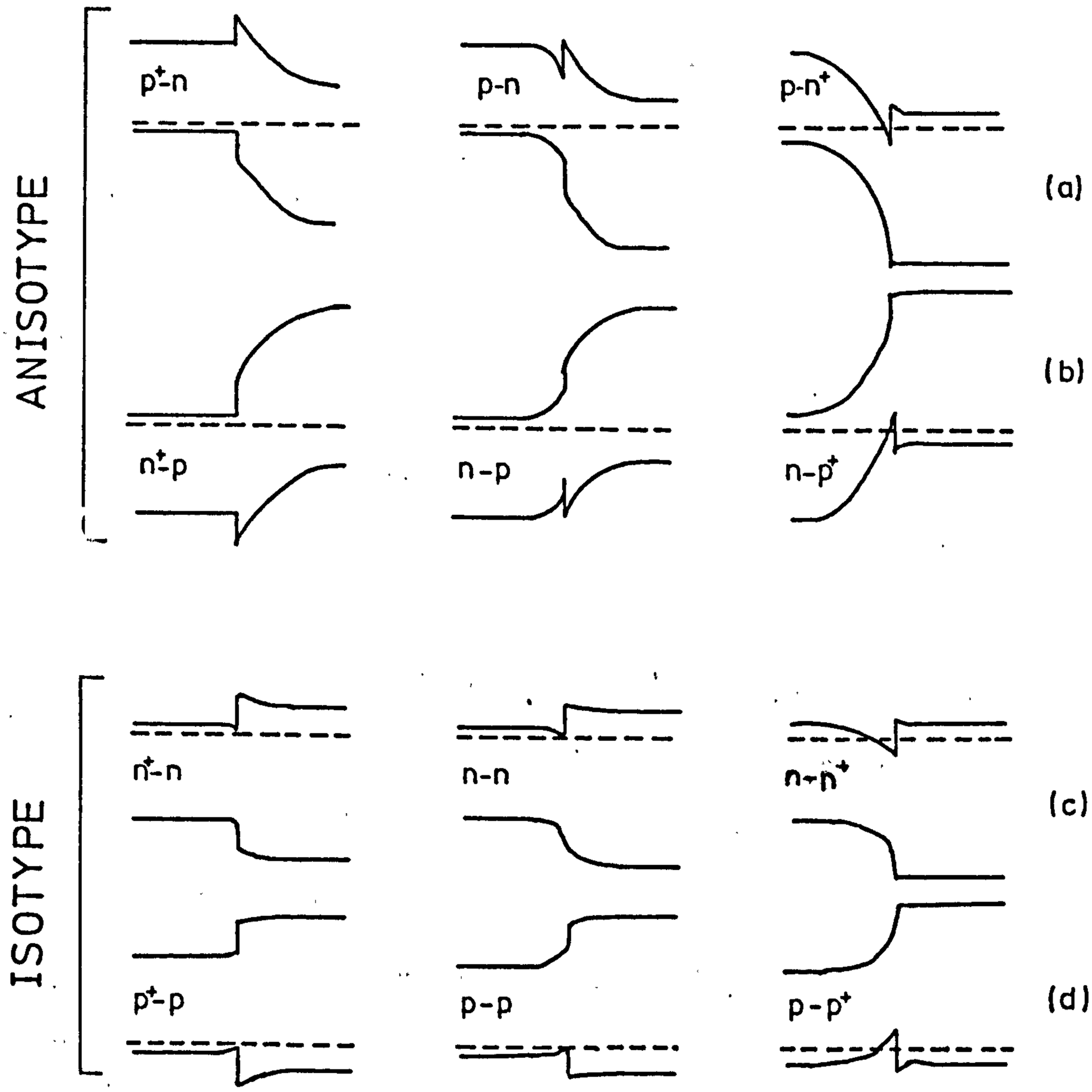
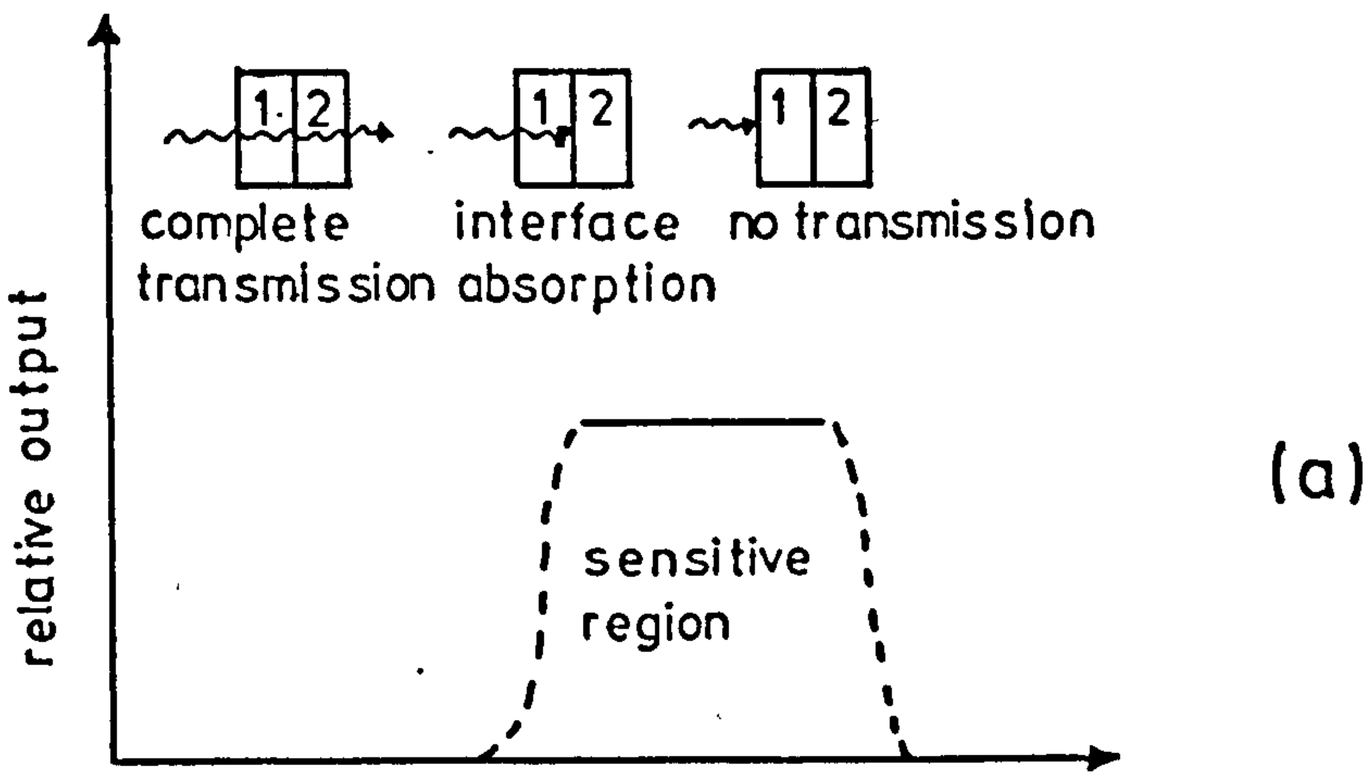


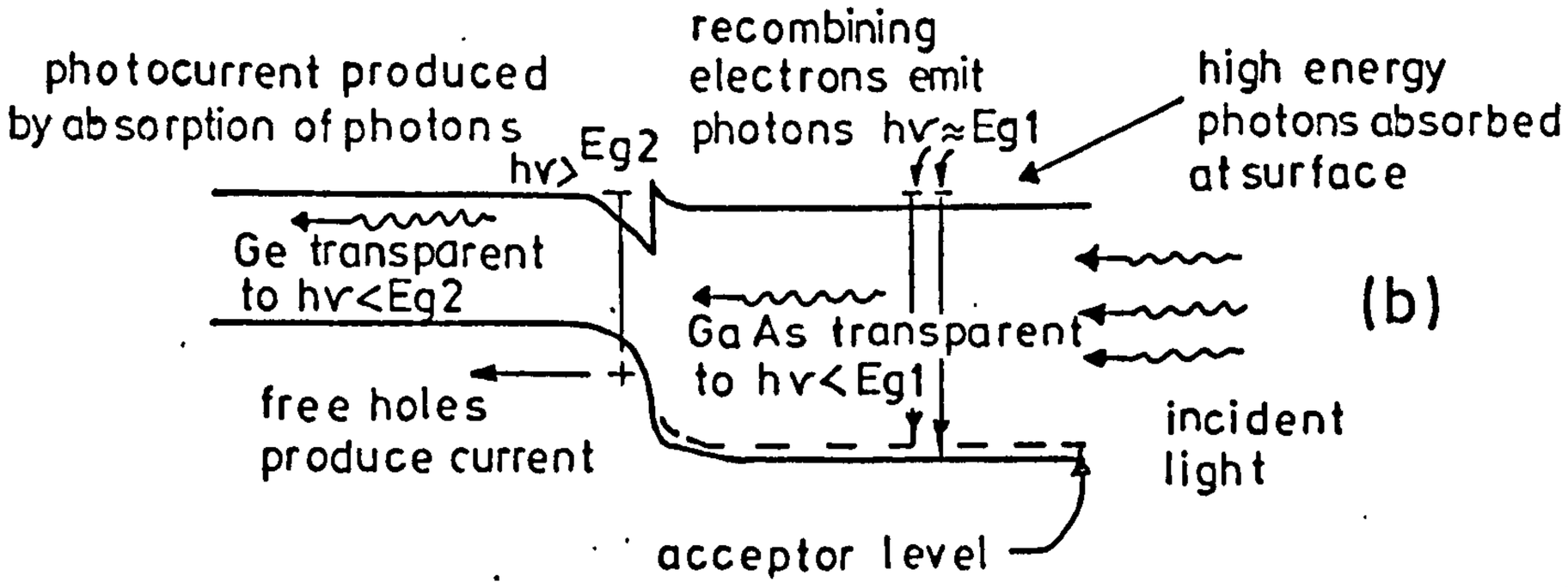
Fig 1.3 Examples of isotype and anisotype hetero-junctions showing the effect of changes in doping (23)

transition field and produces a voltage across the diode. In the photovoltaic mode, the sensitivity is determined by the absorption coefficient of the photodetector material. In the photoconductive mode, an applied bias widens the depletion region and so increases the sensitivity. This widening of the depletion region decreases the capacitance and as a result reduces the response time. Figure 1.4 illustrates the "window effect", together with one of the results of Anderson.[19] For all the anisotype heterojunctions (p-n and n-p) shown in Figure 1.3, the minority photocarrier is swept towards the interface and the majority carrier into the bulk of the narrow-gap material. The doping conditions are now important, since efficient conversion of incident optical energy to external electrical energy depends upon three factors[24]:

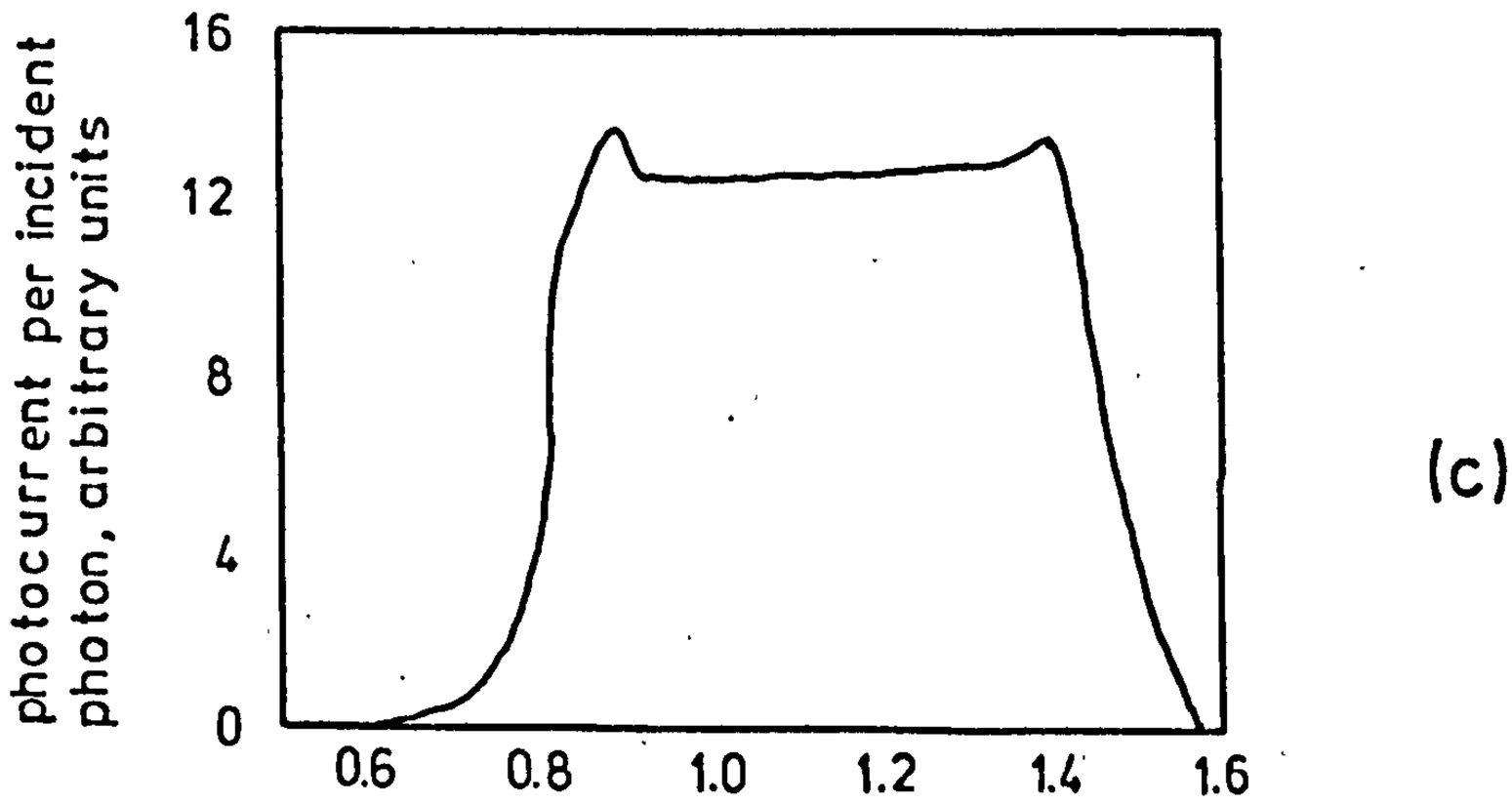
(i) The narrow gap transition region width must be approximately equal to or greater than the photon absorption length. Photocarriers generated within the transition region are quickly separated, minimising the probability of recombination and hence loss of efficiency. This separation process is very fast. In the case of a transition region which is narrow compared to a typical photon absorption length, the majority of electron-hole pairs are generated in the field-free bulk narrow-gap material adjacent to the transition region. Minority carriers must then diffuse into the region in order that an output signal should result.[25] Not only is the diffusion process relatively slow, hence increasing the device response time, but in materials having a short minority carrier lifetime this delay will increase the probability of recombination, so that efficiency is also reduced. It is worthwhile estimating the possible time constant which might be expected. The conversion time constant for photogeneration in the depletion region is approximately d/V, where d is the depletion region width and V the drift velocity. For generation in the bulk and subsequent diffusion over a distance t with diffusion constant D the approximate time



(a)



(b)



(c)

Fig 1.4 Schematic showing, (a),(b), photon absorbtion, (c), short-circuit photocurrent per incident photon (19)

constant is t^2/D, so that the time constant for the complete process is

$$\tau = \frac{d}{V} + \frac{t^2}{D} \qquad (1.1)$$

Berchtold et al.[23] observed that for a typical silicon surface barrier device with d = t = 1 micron, the diffusion term was 10^{-9} seconds and the drift term about 10^{-10} seconds.

(ii) The magnitude of the transition field must be sufficiently great to separate electrons and holes before they recombine; this also becomes more important in the shorter lifetime materials.

Both the transition field and the depletion width are, in general, increased by increased reverse bias, which makes factors (i) and (ii) less critical.

(iii) The interface band structure must be such as to permit the transfer of minority carriers into the wide-gap material, where they attain the status of majority carriers. These criteria can be applied to the structures of Figure 1.3 in order to eliminate those which are unsuitable for opto-electronic detection applications. Condition (i) eliminates all those permutations in which a relatively small fraction of the diffusion voltage is dropped across the narrow-gap material. This is the situation for all the structures in the first column. This result is reinforced by the application of condition (ii), which also serves to eliminate the isotype (p-p and n-n) structures for the following reason: since space-charge neutrality must be conserved, Fermi level balancing must yield a dipole layer composed of one depletion region and one accumulation (or even inversion) region. Also, the accumulation region must always arise in the narrow-gap material, at least for the electron affinity difference chosen for Figure 1.3. Qualitatively it can be seen from a comparison of the zero bias band profiles of Figure 1.3 (a and b) with Figure 1.3 (c and d) that the fraction of the diffusion voltage appearing in the narrow-gap

material (accumulation region) of an isotype junction is, at most, about equal to the magnitude of the discontinuity in the majority-carrier band edge. In the anisotype junctions, however, it is apparent that under proper doping conditions, this part of the diffusion voltage can be almost as large as the wider of the two band gaps. Another point is that in such a structure the greatest part of an applied reverse bias is taken up in increasing the component of the diffusion voltage in the narrow-gap material. For an isotype junction it can be shown that little enhancement of the accumulation region will take place under reverse bias.[26] On this basis the isotype heterojunctions can be neglected in seeking optimum conversion efficiency. While to some extent fulfilling condition (ii), the anisotype heterojunctions of approximately symmetrical doping clearly present a potential well trap because of the "spike and notch" profile of the band in which photogenerated carriers attempt to cross the interface. This is where the consequences of the high concentrations of interface states are likely to be felt. The probability of recombination at a notch is greatly enhanced, and conversion efficiency thus greatly reduced, by the presence of a ladder of allowed states down to the valence band.[27] It is therefore necessary to ensure that photocarriers are not notch trapped. The best arrangements are the $p\text{-}n^+$ and $n\text{-}p^+$ cases in which the narrow-gap material is more lightly doped. The minority photocarriers are injected over the top of the notch into the wide-gap material.

In addition to possible recombination losses, the charge content of such interface states will deform the band profile,[12] possibly into a shape disadvantageous to efficient photoconversions. In practice this band deformation will not be important for those doping asymmetries in which notch trapping can be neglected.

1.6 Reflection Loss

Since the refractive index of most semiconductors is high (for silicon $n \approx 3.5$), the reflection loss from the surface can be significant. The lower refractive index of CdS ($n \approx 2.45$) allows it, to a certain extent, to act as a matching layer. The thin film CdS layer acts as an interference filter, having maxima and minima of reflected or transmitted radiation. Because the silicon substrate is an absorbing medium, its refractive index is expressed in complex form

$$N = n - jK \tag{1.2}$$

The index of refraction n is defined as the ratio of the phase velocity of light in vacuum to the phase velocity of light in the material. The extinction coefficient K is related to the exponential decay of the radiation as it passes through the medium, and is defined as:

$$K = \frac{\alpha\lambda}{4\pi} \tag{1.3}$$

where α is the absorption coefficient and λ is the wavelength of the radiation. It is possible, knowing the refractive indices of silicon and CdS at a given wavelength and the CdS film thickness, to calculate the percentage of the incident radiation that is reflected.[28] Details of the refractive indices of silicon and CdS as a function of wavelength are known.[29,30] Because it is necessary to know the CdS film thickness to a high degree of accuracy (in the worst case a 0.01 micron change in the CdS film thickness results in a 23% change in reflectivity) it is more useful to calculate the minimum and maximum values of reflection at a given wavelength.[31] For example, assuming that for CdS, n = 2.484 and that for silicon, n = 3.975 -j 0.168 at 600 nm wavelength, the minimum and maximum reflectivities are 4.6% and 35.9% respectively.

CHAPTER 2 CRYSTAL GROWTH AND STRUCTURE

2.1 Introduction

Many of the physical properties of CdS films are quite sensitive to the method of deposition used and to the details of the fabrication and processing techniques. The microstructure, including crystallographic phases, crystallite size and orientation, and the surface features like roughness and uniformity are dependent on many factors, e.g. substrate temperature, deposition rate and angle, and ambient pressure. The stoichiometry, impurity content and degree of film stress, vary appreciably for different fabrication methods. These variations are particularly important in influencing the electrical and opto-electronic properties of the films and in causing anomalous behaviour or properties significantly different from bulk ones.

It is possible to grow films of II-VI compounds, in vacuo, using either a compound source of the material or a source of each of the compounds. Compound evaporated films are produced by evaporating single crystals of CdS or powdered CdS in a vacuum and then condensing the resultant vapour, composed of Cd atoms and S_2 molecules, on a substrate. In contrast, the condensing vapour in co-evaporated film deposition is composed of Cd atoms and S_8 molecules.[32]

2.2 Vaporisation of CdS Compound

Thermal evaporation of compound CdS in vacuum can be performed under two types of conditions. In the first, equilibrium between vapour and solid is maintained, while in the second a marked deviation from equilibrium is involved.

The vaporisation characteristics of the majority of solids, (including CdS) are different for non-equilibrium and equilibrium conditions,[33,34] e.g. because of factors such as the evaporation rate, vapour and solid

composition. Non-equilibrium conditions usually prevail during the vacuum evaporation of these solids. Equilibrium measurements yield thermodynamic data (e.g. enthalpy, free energy) about the vaporisation reaction and data on the vapour composition-solid equilibrium.[35,36] Non-equilibrium studies,[34,37-41] however, have led to an understanding of the evaporation mechanisms of solids, from which better means of control over the evaporation rate and vapour composition can be developed. Such control is essential in the deposition of stoichiometric films.

There is strong experimental evidence to indicate that the vaporisation of solids proceeds, in general, by means of several consecutive or parallel reaction steps.[33,34,37-41]

CdS has been found to dissociate, upon vacuum evaporation, into a vapour composed predominantly of Cd atoms and S_2 molecules, together with smaller amounts of the heavier species S_3, S_4, S_5, S_6, S_7 and S_8. The relative proportions of these heavier molecules of sulphur depend on the temperature and pressure of the environment, and on whether or not equilibrium or steady state conditions exist.[35,36,42,43] The net dissociation reaction can be written as

$$CdS\ (Solid) \rightleftharpoons Cd\ (Vapour) + \sum_{n=2}^{8} \left(\frac{1}{n}\right) Sn\ (Vapour) \qquad (2.1)$$

The intermediate reaction steps thought to be involved in this dissociation reaction have been determined from measurements of CdS evaporation rates[34,37,38] and studies of CdS surface topographies under non-equilibrium and equilibrium conditions of evaporation.[40,41] These steps may be described as[34,37,38]: (i) diffusion of ionised vacancies between the bulk and vaporising surface of CdS, (ii) charge transfer and neutral atom formation, and (iii) removal of neutral atoms or molecules to the vapour.

Somorjai and Lester[34,37] have postulated that CdS generally

vaporises via a charge transfer controlled mechanism. Recent results from studies of surface topographies of evaporated CdS crystals by Munir and Hirth[40] and Leonard and Searcy[41] have suggested that there are other rate-controlling steps, namely, ledge formation with indirect effects by charged carriers or the desorption reaction steps, respectively. A possible explanation of this disagreement is that the conditions of the reaction have not been the same in the two studies.

Thin films are commonly prepared by the condensation of atoms from the vapour phase of a material. At the earliest stage of observation, atomistic condensation takes place, in the form of three-dimensional nuclei which subsequently grow to form a continuous film by diffusion-controlled processes.[44]

2.3 Condensation

The condensation of a vapour is determined by its interaction with the surface on which it impinges. The atom loses its velocity component normal to the surface in a short time, provided the incident kinetic energy is not too high. The vapour is then physically adsorbed (forming an "adatom") but it may not be completely in thermal equilibrium with the surface. It may move over the surface by jumping from one potential well to another because of thermal activation from the surface and/or its own kinetic energy parallel to the surface. The adatom has a finite stay or residence time on the surface during which it may interact with other adatoms to form a stable cluster and be chemically adsorbed (incorporated into the surface) with the release of the heat of condensation. If not adsorbed, the adatom re-evaporates or desorbs into the vapour phase. Therefore, condensation is the net result of an equilibrium situation between the adsorption and desorption processes. The probability that an impinging atom will be incorporated into the substrate (surface) is

called the "condensation", or "sticking" coefficient. It is measured by the ratio of the amount of material condensed on a surface to the total amount which impinges.

Langmuir[45] and Frenkel[46] formulated a condensation model in which the adsorbed atoms move over the surface during their lifetimes to form pairs, which in turn act as condensation centres for other atoms. From this model the concept of a critical beam density was developed. Although this concept is in accord with the experimental observations of Cockroft[47] (condensation of Cd on Cu surface), its relationship with the beam and substrate temperatures is by no means as simple, since a nucleation barrier exists for condensation to occur. This barrier depends sensitively on the temperature, chemical nature, structure, and cleanliness of the surface. The value of the critical beam density drops markedly immediately after the initial nucleation has occurred.

When compounds are thermally evaporated, the components may evaporate at different rates because of their different vapour pressures. In addition other important factors are the different tendencies of components to react with the substrate material, and possible thermal decomposition of the substrate or parent material. Figure 2.1 shows the vapour pressure temperature relationship for CdS, Cd, S_2 and S_8.[48]

There are two approaches used to tackle the two-component condensation problem: (i) The empirical method of Gunther,[49,50] and (ii) The theoretical analysis of Reiss.[51] Both approaches have their limitations, but they provide semi-quantitative predictions which agree reasonably well with experimental observations.

2.3.1 Gunther's Model

Gunther[49,50] extended the concepts of the condensation of a one component vapour to involve the behaviour of a two-component vapour.

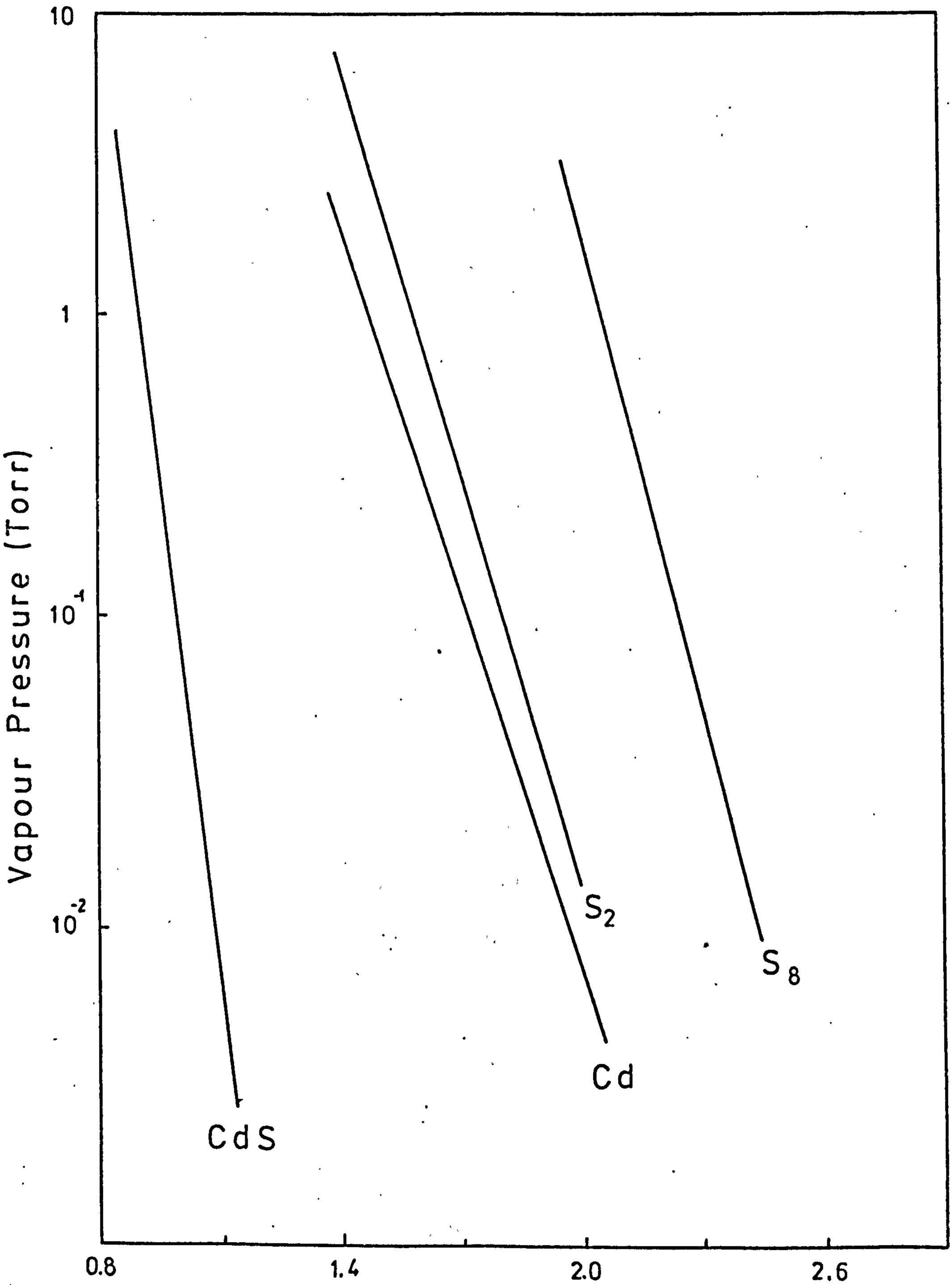


Fig 2.1 Vapour pressure versus absolute temperature (48)

For the case of a vapour consisting of two components, A and B, the condensation coefficient of each component is assumed to increase in the presence of the other component, after their adsorption on to a substrate. The probability of mutual interaction between the particles, A and B, being a function of the densities of the adsorbed particles, and of the effective "lifetime" of the particles, should be enhanced. The "lifetime" is the time interval between being adsorbed upon a substrate and being captured by a nucleation centre or re-evaporated from the substrate. Interactions between particles, A and B, lead to the formation of molecules of a stable compound AB, i.e. $A + B \rightleftharpoons AB$. The critical condition under which progressive condensation of compound AB occurs, can be expressed as:

$$N^*_{+B(A)} << N^*_{+B} \text{ , if } P_{e(B/AB)} << P_{eB} \qquad (2.2)$$

$$T^*_{B(A)} > T^*_{B} \qquad (2.3)$$

where $N^*_{+B(A)}$ is the critical flux of component B in the presence of component A, $P_{e(B/AB)}$ is the partial pressure of B in equilibrium with compound AB, P_{eB} is the equilibrium vapour pressure of B, $T^*_{B(A)}$ is the critical temperature of B in the presence of A and T^*_{B} is the critical temperature of B.

2.3.2 Reiss's Model

Reiss's approach is based on the capillarity theory of nucleation. The nucleation process is characterised by a phase transition from a super-saturated mother phase to a new bulk condensed phase, which involves the following sequence of events:

(a) the formation of clusters or embryos of the new condensed phase,

(b) the growth or decay of these embryos,

(c) the attainment of a critical size of embryo (i.e. a nucleus) and its change into a stable aggregate of the new condensed phase in equilibrium

with the mother phase. The rate of formation of these critically sized embryos is given by:

$$I^* = C \exp(-W_o/KT) \qquad (2.4)$$

where W_o is the energy required to produce an embryo which remains in equilibrium and C is a constant to be determined. A kinetic theory of phase transition in a binary system has been developed by Reiss. The final expression for the nucleation rate is:

$$I^* = \frac{gN_{+A} \cdot N_{+B} \left[1 + (y/x)^2\right]}{N_{+B} + N_{+A}(y/x)^2} \cdot \exp(-W_o/KT) \qquad (2.5)$$

where g is a constant factor which depends on the total number of molecules present in the system, the surface tension of the nucleus and the characteristics of the energy surface; $N_{+A,B}$ are the impingement rates of components, A and B; W_o is the free energy of formation of a nucleus, and (y/x) is the stoichiometric ratio of the composition of the nucleus.

2.3.3 Deductions from the two models

From Gunther's model, the condensation flux N_K and, therefore, the composition of the condensed compound are dependent on the incident fluxes of components, A and B. When the composition of the condensed compound is expressed as a function of N_{+A} and N_{+B} it can be shown that there is a region where a stoichiometric compound can be condensed. This stoichiometric region also depends on the substrate temperature, and increases with temperature but only for a limited range of temperatures. In terms of the vapour pressures of the compound and the components, a stoichiometric region only occurs if the following condition holds:

$$P_{e(AB)} < P_{eA} , P_{eB} \qquad (2.6)$$

where P_e is the equilibrium vapour pressure. The existence of a

stoichiometric region cannot be easily inferred from Reiss's model.

The condensation rate of component AB can be shown to approach a maximum value of $N_K = 2N_{+A} - N_{eA}$, providing $N_{+B} > N_{+A}$ (Gunther [49,50]). This dependence of N_K on N_{+A}, where component A is taken to be less volatile than component B, can be expressed as:

$$N_K \simeq 2N_{+A} \tag{2.7}$$

The equilibrium value N_{eA} is neglected because it is constant and smaller than N_{+A}.

It is possible, by making a number of assumptions, to simplify the expression for progressive nucleation or growth of compound AB from Reiss's model. The main assumption is that, for the case of continuous condensation of compound AB at a constant temperature, the exponential term in the rate expression ($\exp(-W_o/KT)$) can be considered to be a slowly varying function, i.e. almost a constant. The nucleation expression can now be written as

$$I \approx \frac{N_{+A} \cdot N_{+B} \left[1 + (y/x)^2\right]}{N_{+B} + N_{+A} \cdot (y/x)^2} \tag{2.8}$$

This expression can then be examined for the different stoichiometric ratios (y/x):

$$(y/x) = 1 \qquad I \approx 2N_{+A} \qquad (N_{+B} >> N_{+A}) \tag{2.9}$$

$$(y/x) = \tfrac{1}{2} \qquad I \approx {}^5/_4 N_{+A} \qquad (N_{+B} > N_{+A}) \tag{2.10}$$

$$(y/x) = {}^1/_n \qquad I \approx N_{+A} \qquad (N_{+B} \geq N_{+A}) \tag{2.11}$$

$$\text{where } (y/x) = \frac{\text{number of particles of component B}}{\text{number of particles of component A}} \tag{2.12}$$

and the interaction is of the type, A atoms with B_n molecules.

Both models of condensation in a two component system demonstrate

the dependence of the nucleation or growth rate on the incident flux of the less volatile component N_{+A}, providing $N_{+B} > N_{+A}$.

2.3.4 Cadmium-Sulphur System

The relationship of the two models to this system can now be investigated. Considering Figure 2.1, showing the vapour pressure of CdS, Cd, S_2 and S_8 versus temperature, the vapour pressure criteria of the Gunther model hold:

$$P_{e\ (CdS)} < P_{e\ (Cd)},\ P_{e\ (Sn)} \qquad (n = 2,3 \ldots 8) \qquad (2.13)$$

$$P_{e\ (Cd)} < P_{e\ (Sn)} \qquad (2.14)$$

It should therefore be possible to deposit stoichiometric films of compound CdS, where the less volatile component A is cadmium, and the more volatile component B is sulphur.

2.4 Nucleation

There are two main theories for nucleation, the capillarity theory and the statistical or atomistic theory. The capillarity model assumes that the film is formed by heterogeneous nucleation and growth. In this theory, clusters (also called embryos, or subcritical nuclei) are formed by collisions of adatoms on the substrate surface, and in the vapour phase if supersaturation is sufficiently high. These nuclei are assumed to be in the form of spherical caps which "wet" the substrate and further it is assumed that macrosopic thermodynamic quantities (energies etc.) are applicable to these nuclei.

A cap-shaped nucleus is shown in Figure 2.2. The equilibrium contact angle θ is related to the surface and interfacial tensions defined in Figure 2.2 by the equation (21):

$$\sigma_{SV} = \sigma_{CS} + \sigma_{CV} \cos\theta \qquad (2.15)$$

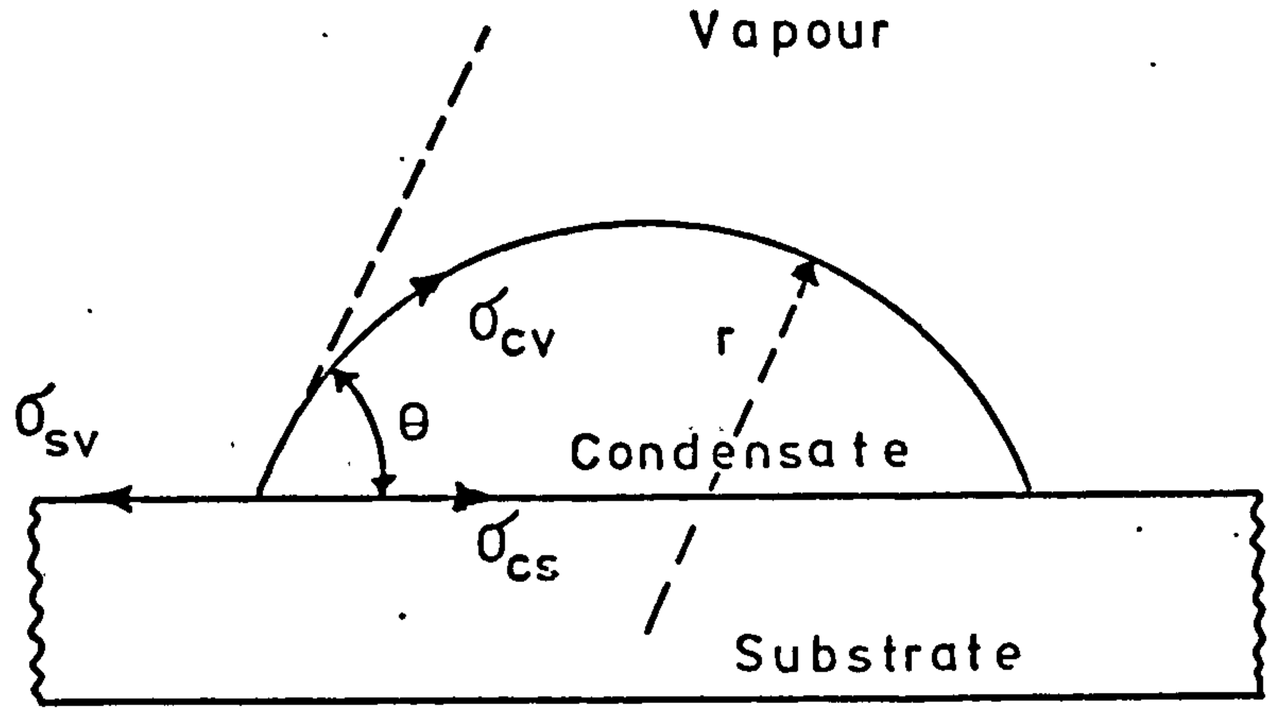


Fig 2.2 Spherical cap-shaped nucleus (52)

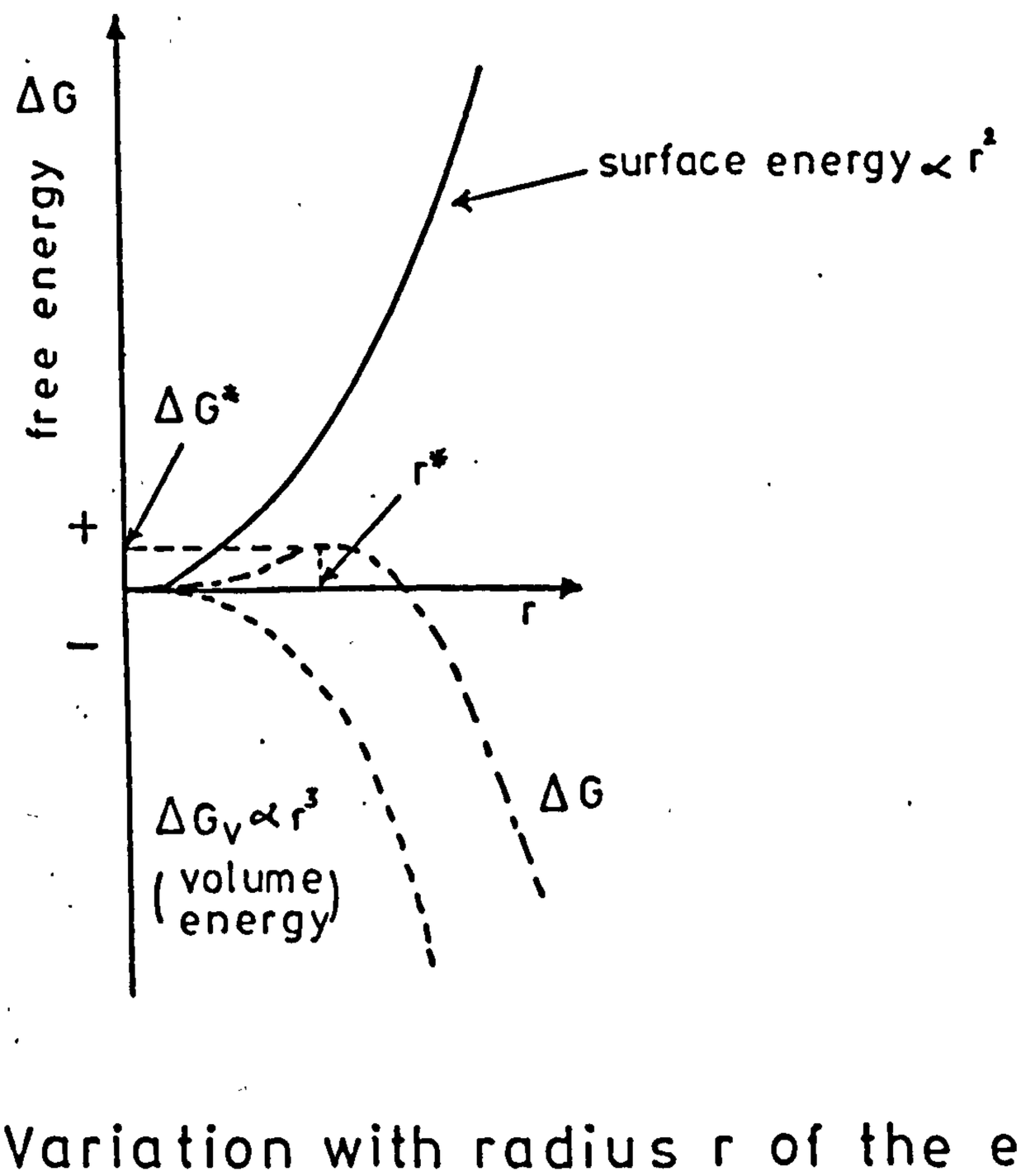


Fig 2.3(a) Variation with radius r of the energy of a nucleus on the capillarity model (52)

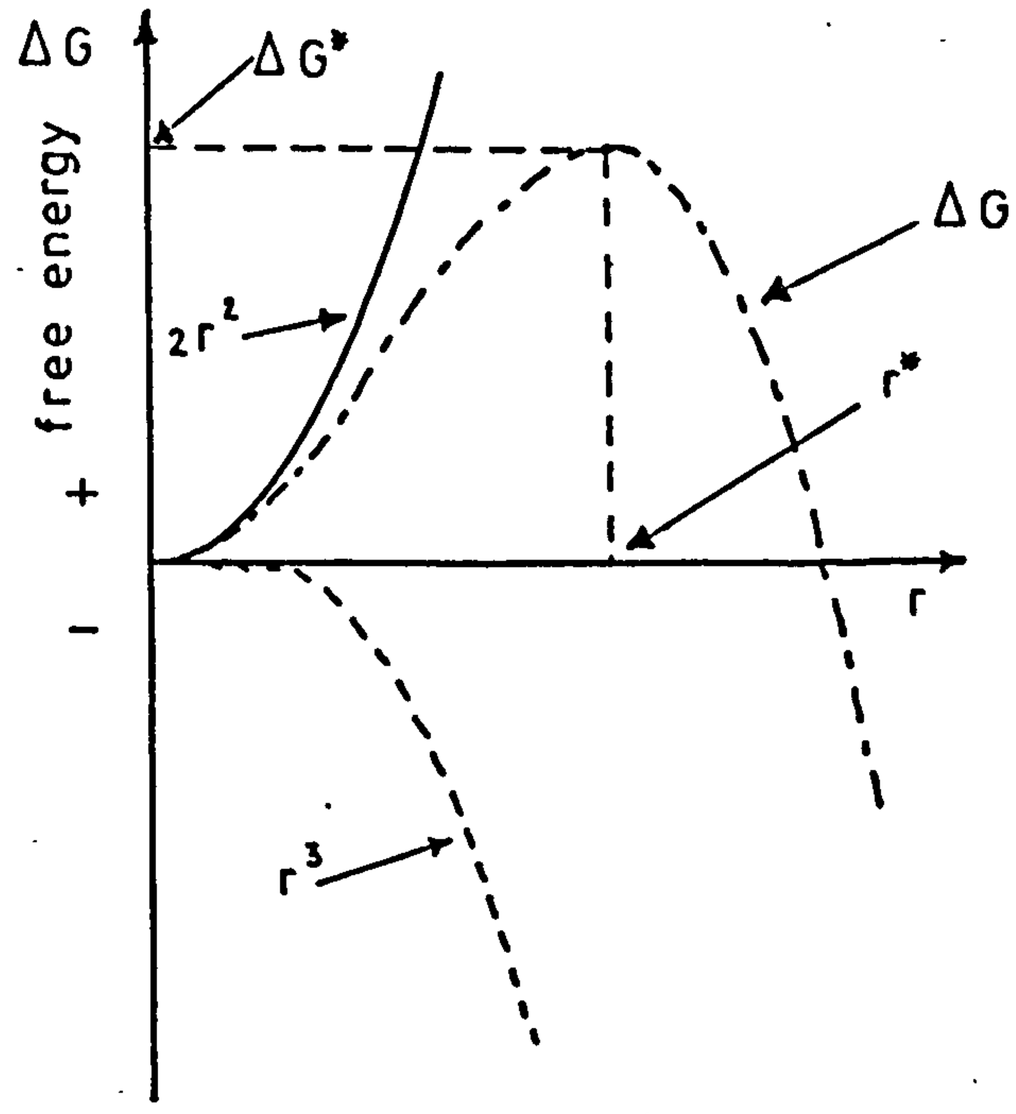


Fig 2.3(b) Showing that for a higher interfacial energy per unit area, due to less favourable orientation of the nucleus, both r^* and ΔG^* are increased (52)

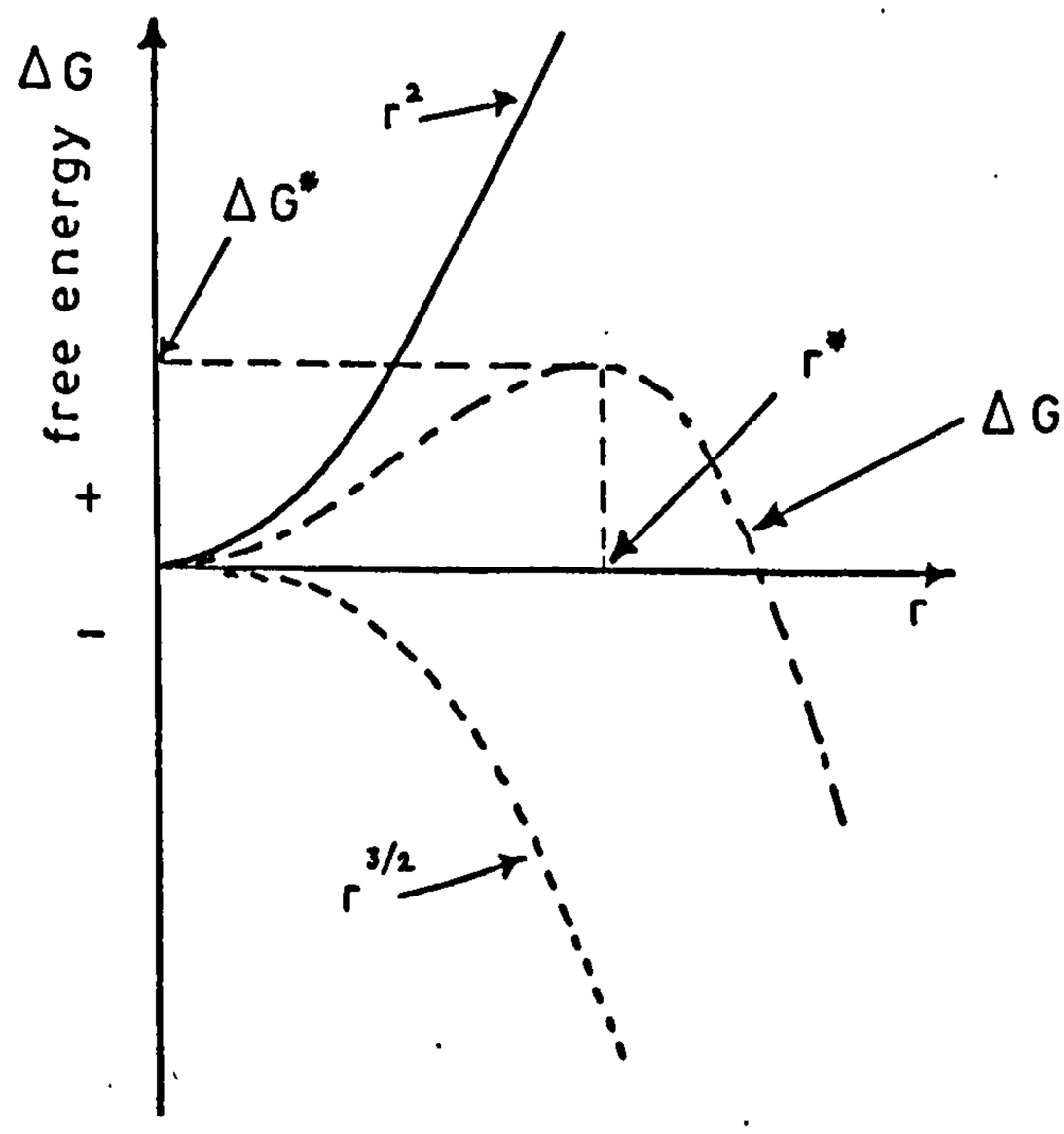


Fig 2.3(c) Showing that both r^* and ΔG^* are increased for a smaller G_v (52)

Therefore, since

$$\theta = \cos^{-1}\left(\frac{\sigma_{SV} - \sigma_{CS}}{\sigma_{CV}}\right), \qquad (2.16)$$

those nuclei with the lowest interfacial energies, σ_{CS}, will have the smallest contact angle θ.

The free energy of a nucleus or "embryo" is the sum of surface energy terms, which increase as r^2 where r is the radius of the sphere, and a (negative) volume energy term, which increases in magnitude as r^3. From Hirth and Pound[52]:

$$\Delta G = \pi r^2 \sin^2\theta\,(\sigma_{CS}-\sigma_{SV}) + 4\pi r^2\phi_1(\theta)\sigma_{CV} + (4\pi/3)r^3\phi_2(\theta)\Delta G_V \qquad (2.17)$$

where ΔG_V is the energy of the crystalline phase per unit volume and ϕ_1 and ϕ_2 are geometric functions of θ. This energy has a maximum value ΔG^* for a critical radius r^*, as shown in Figure 2.3(a). The values of ΔG^* and r^* will both be increased for unfavourable orientations (higher σ_{CS}) of the same crystalline structure (whether wurtzite or sphalerite) and for nuclei of the higher energy (smaller ΔG_V) structure. The rate of nucleation, which is the formation of "embryos" of radii $r \geq r^*$ which will tend to grow rather than disintegrate, varies as $\exp(\Delta G^*/KT)$. Thus, favourably oriented nuclei and nuclei of the lower energy phase will be formed at higher rates than those of the less favourable orientation.

A lower interfacial energy means a smaller contact angle θ. This in turn confers an advantage in growth on the nuclei having lower σ_{CS}. The reason for this is that a smaller value of θ means a lower and wider shape for a given volume, while a larger value of θ results in a narrower, higher form. The low, wide form gains doubly in growth, since atoms or molecules add onto the nucleus in two ways: (i) by direct impact on the top surface of the nucleus, and (ii) by addition at the periphery of atoms or molecules diffusing over the substrate surface. The low, wide form

has a larger collecting surface area for direct impacts and a larger collecting circumference for surface diffusing adatoms, for a given volume. Since the initial (critical) nuclei are thought to consist of only a few atoms, the use of bulk thermodynamical quantities for such small clusters, in the capillarity theory, is at least questionable.

This problem is overcome in the atomistic approach by writing the partition functions and potential energies for the reacting species and products.[53] An approximate analysis which considered the energies and bonds of nucleation clusters treated as macromolecules has been given by Walton.[54,55] At low substrate temperatures or very high supersaturations, the critical nucleus may be a single atom which will form a pair with another atom by random occurrence to become a stable cluster and grow spontaneously. The stability of a pair is derived from an assumed availability of one bond per atom. At higher substrate temperatures, a pair of atoms may no longer be a stable cluster. The next smallest stable cluster is one that has a minimum of two bonds per atom, which may be achieved by putting atoms at the corners of a triangular configuration.

Although alternative atomistic models have been proposed, for the reason mentioned, the capillarity model is of the simplest and gives reasonable results.[56]

2.5 Growth Process

The characteristic sequential growth stages are: (i) randomly distributed, three dimensional nuclei are first formed and rapidly approach a saturation density with a small deposit of material. These nuclei then grow to form observable islands whose shapes are determined by interfacial energies and deposition conditions. The growth is diffusion-controlled. Adatoms and subcritical clusters diffuse over the substrate

surface and are captured by the stable islands, (ii) as the islands increase their size by further deposition and come closer to each other, the larger ones appear to grow by coalescence of the smaller ones. Island density decreases monotonically at a rate determined by the deposition conditions. This stage involves considerable mass transfer by diffusion between the islands, (iii) when the island distribution reaches a "critical" state, a rapid large-scale coalescence of the islands results in a connected network structure, and the islands are flattened to increase surface coverage. This process is very rapid initially, but slows down considerably on formation of the network which contains a large number of empty channels, (iv) the final stage of growth is a slow process of filling the empty channels, which requires a considerable amount of material to be deposited. Whenever large surface areas are vacated by coalescence to form a composite structure, secondary nucleation occurs. These nuclei generally grow and coalesce very slowly with further deposition. This effect is particularly marked when the secondary nuclei are completely surrounded by the deposited material.

2.6 Epitaxial Films, Growth and Structure of II-VI Compounds

The II-VI compounds consist of equal numbers of atoms of an element from the II(b) column of the periodic table and of an element from the VI(b) column. They are related in crystallography and physical properties to the semiconducting III-V compounds and the IV(b) elements Ge and Si.

The wide and direct forbidden energy gaps of the compounds of S, Se and Te with Cd and Zn, make these materials attractive for opto-electronic solid state devices. Figure 2.4 shows the distribution of forbidden energy gap, wavelength, and compound group, among the more common semiconductors. Polycrystalline CdS films are used in photoconductive and photovoltaic

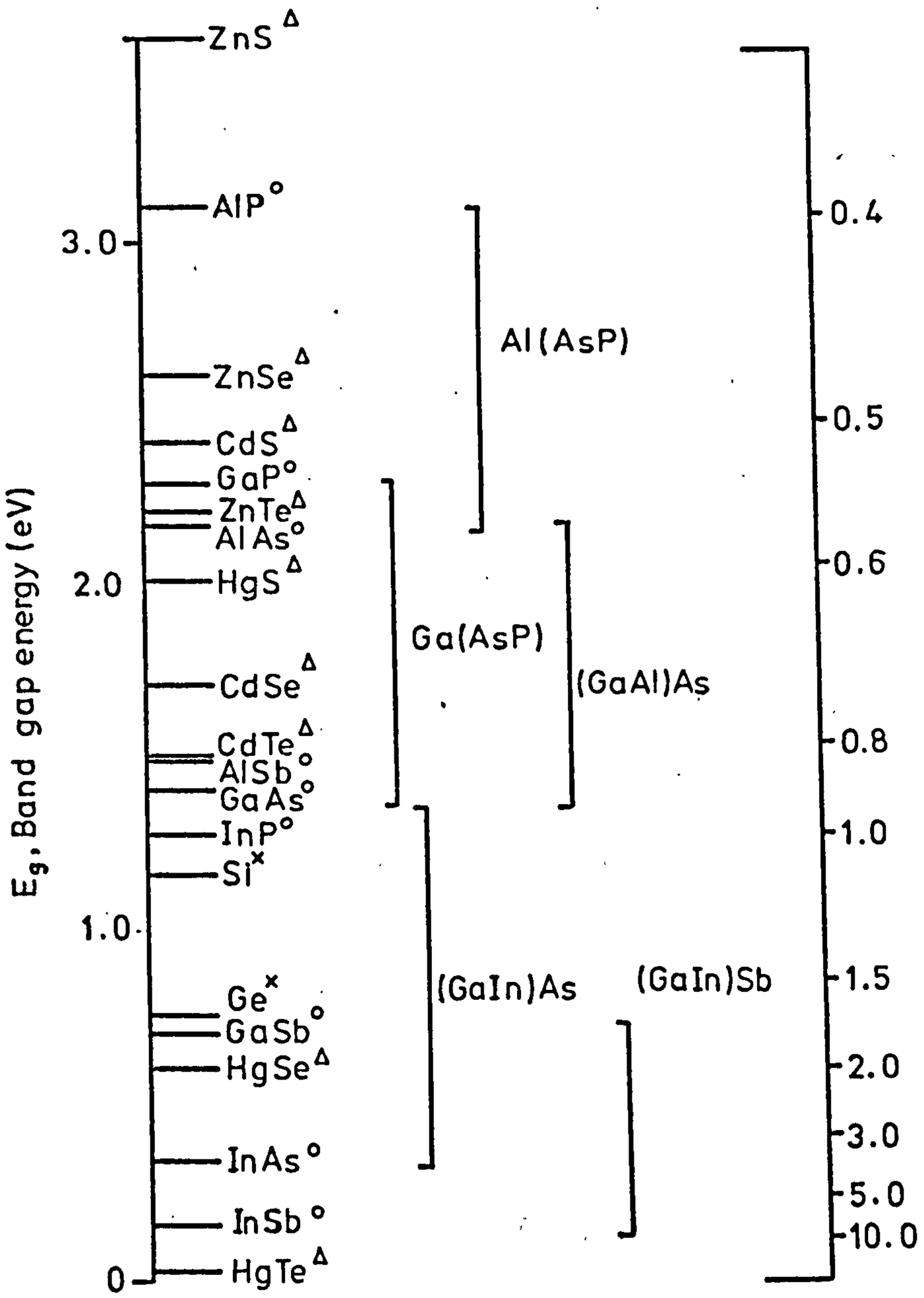


Fig 2.4 Distribution of energy gap among the more common semiconductors

devices. However, it is desirable to produce the II-VI compounds as bulk crystals and as thin films of high perfection and purity with controlled doping and stoichiometry. This should then make it possible to make junctions of predictable properties between say II-VI compounds and group IV compounds, an example being a CdS-Si junction (heterojunction).

2.6.1 Epitaxy

Royer[57] introduced the term epitaxy ("arrangement on") to denote the phenomenon of the oriented growth of one substance on the crystal surface of a foreign substance. Since then, epitaxial growth of films of metals, insulators, and semiconductors has been the subject of extensive investigation. The oriented growth of a material over itself is now termed "auto-epitaxy", and over another material "hetero-epitaxy" or simply epitaxy.

In a review of epitaxy, Pashley summarised firstly the knowledge obtained mainly by electron diffraction[58] and secondly that obtained principally by means of transmission electron microscopy (T.E.M.).[59] The earlier work on electron diffraction provided information on the crystal structures of epitaxial films, on the epitaxial orientation relations of the films on the substrates, and on the optimum conditions for epitaxial growth. The T.E.M. work provided information on the nucleation and growth mechanisms involved in epitaxy and on the defects in epitaxial films.

There are a number of parameters which affect the oriented growth of films deposited on single-crystal substrates. These include the orientation of the substrate, the substrate temperature, the substrate cleanliness, the deposition conditions, and the vacuum conditions.

As has been mentioned earlier, silicon crystallises in the diamond structure, while CdS crystallises in either the closely related sphalerite (cubic close-packed) or the wurtzite (hexagonal close-packed) structure.

Figure 2.5 shows a diagrammatic representation of the three different crystallographic structures.

2.6.2 Influence of Substrate Orientation

The single-crystal substrate has a dominant influence on the oriented growth of the deposit. Epitaxy can occur between substrates of completely different crystal structures and of different types of chemical bonds (covalent, ionic). Table 2.1 illustrates some of the cases where epitaxial growth of CdS has been observed. A striking feature of the data of Table 2.1 is that in all cases, except that of Chopra and Khan[60], vacuum evaporated epitaxial films of CdS grew on (100) and (110) substrate surfaces with the cubic sphalerite structure.[14] The sphalerite structure was obtained in epitaxial (100) and (110) films of all the II-VI compounds for which results have been reported, whether sphalerite or wurtzite was the stable bulk structure over the epitaxial growth range of substrate temperatures. Holt[14] suggested that wurtzite structure films do not grow on (100) or (110) substrate faces due to the impossibility of matching the symmetry of (100) planes or (110) planes exactly by planes in the hexagonal structure. That is, in whatever orientation the wurtzite structure might nucleate on (100) or (110) faces, there must always be a large fraction of non-coincident lattice sites with unsatisfied bonding requirements.

Chopra and Khan[60] obtained epitaxial growth of CdS on (100) surfaces of NaCl at temperatures down to 20°C, and the films grown at the lowest epitaxial temperatures had the wurtzite structure. In contrast, Wilcox and Holt[61] obtained epitaxial growth of CdS on (100) NaCl, only for substrate temperatures in the range 150-300°C, and the films always had the sphalerite structure in agreement with the general rule quoted above. The reason for the disagreement between the two studies is not known,

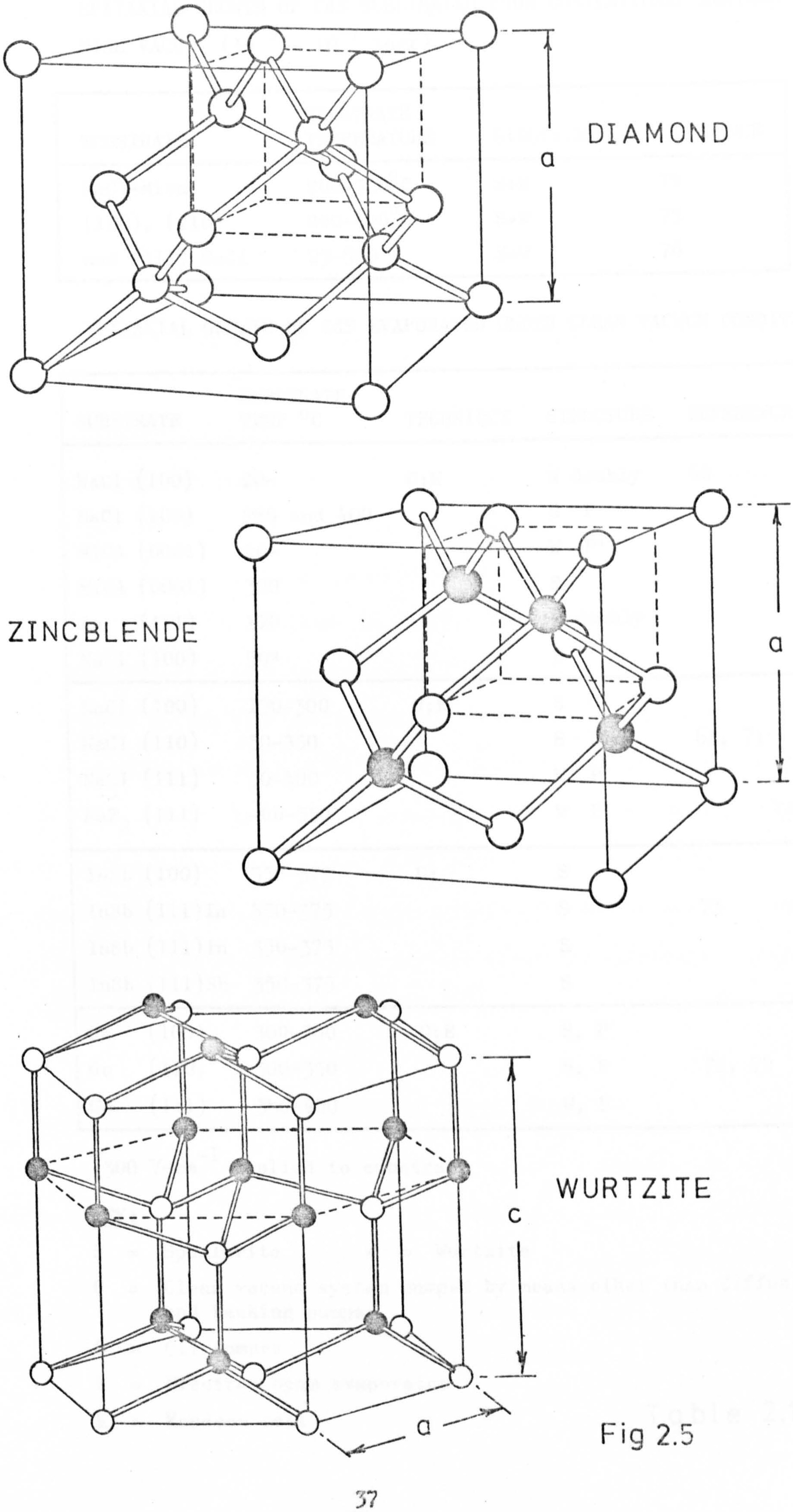


Fig 2.5

EPITAXIAL GROWTH OF CdS SUBLIMATED FROM CONVENTIONAL HEATERS IN HIGH VACUO (10^{-5} - 10^{-7} torr)

SUBSTRATE	SUBSTRATE TEMPERATURE	STRUCTURE	REFERENCE
NaCl+Mica	200-300°C	S+W	74
(100), (110)	200-400°C	S+W	75
and (111) NaCl	23-500	S+W	76

EPITAXIAL GROWTH OF CdS EVAPORATED UNDER CLEAN VACUUM CONDITIONS

SUBSTRATE	SUBSTRATE TEMP °C	TECHNIQUE	STRUCTURE	REFERENCE
NaCl (100)	20-	C;K	W doubly	60
NaCl (100)	280 and 400		S P	
MICA (0001)	20-		W P'	
MICA (0001)	320		S	
Ag (111)	170		W doubly	
NaCl (100)	50*		S	
NaCl (100)	150-300	O;E	S P	
NaCl (110)	50-350		S P	61, 71
NaCl (111)	50-400		W P'	
BaF_2 (111)	-60-550		W P'	
InSb (100)	350-375	C;	S	
InSb (111)In	350-375		S	73
InSb (111)In	350-375		S	
InSb (111)Sb	350-375		S	
Ge (100)	300-500	O;E	S, P	
Ge (110)	300-350		S, P	71, 72
Ge (111)	360-460		W, P	

*300 V-cm^{-1} applied to substrate

KEY:

S = Sphalerite W = Wurtzite

C = Clean vacuum system pumped by means other than diffusion and backing pumps

O = Oil pumped

E = Electron beam evaporator

K = Knudsen cell

Table 2.1

although, as can be seen from Table 2.1(b), Chopra and Khan used both a different type of vacuum system and different evaporation methods. Another factor which might be responsible for the difference is contamination. Henning and Vermaak[62,63] showed that exposure of cleaved NaCl surfaces to air containing water vapour alters the surface from a "chloride" form to an "hydroxide" form and this in turn results in marked changes in the nucleation of face centred cubic metal films evaporated onto the surfaces in vacuum.

The parallel orientation between sphalerite-structure II-VI films and substrates with cubic crystal structures, [i.e. (h, k, l) film parallel to (h, k, l) substrate with [u, v, w] film parallel to [u, v, w] substrate which is a direction in the (h, k, l) plane], occurs very commonly, whether the substrate surface is (100), (110) or (111). These cases are indicated by P in the "structure" column in Table 2.1(b). The geometrically equivalent atomic relation in the case of the wurtzite-structure films, namely (0001) film// (111) substrate and $[11\bar{2}0]$ film//[110] substrate, which is denoted by P´ in Table 2.1(b), also occurs commonly. The important point to be noted is that sphalerite-structure II-VI compound films grown on cubic substrates always have the parallel orientation, P, and wurtzite-structure II-VI compound films grown on cubic crystal strucutre substrates always have the quasi-parallel orientation, P´.[56]

2.6.3 Substrate Temperature: Epitaxial Growth Range

Chopra[44] states that an increasing substrate temperature may improve epitaxy by (i) aiding the desorption of adsorbed surface contaminants, (ii) lowering supersaturation thus allowing the dilute gas of adatoms sufficient time to reach the equilibrium positions, (iii) providing activation energy for adatoms to occupy the positions of potential minima,

(iv) enhancing recrystallisation due to the coalescence of islands by increasing surface and volume diffusion, and (v) assisting a possible ionisation of surface atoms.

Suito and Shiojiri[64], and Holt[65], published a series of electron diffraction patterns showing the effect of substrate temperature on the structural perfection of the film growth. At low substrate temperatures the films grew with fine-grained randomly oriented polycrystalline structures which gave rise to ring diffraction patterns. At higher temperatures epitaxial films grew which gave rise to spot diffraction patterns. At intermediate temperatures the films grew with partially oriented structures which gave rise to mixed ring and spot patterns.

Holt[56] has shown that, in general, the cleaner the growth conditions, the lower is the minimum epitaxial temperature. In addition, there is a cut-off temperature for the deposition of the particular compound/substrate combination. This temperature, unlike the minimum epitaxial growth temperature, is insensitive to contamination. In the case of Ge and Si substrates the films grow epitaxially up to the cut-off temperature. In the case of ionic crystal substrates, there is often a drop in the degree of orientation in the films for growth temperatures near the top deposition cut-off temperature. In the case of ionic crystal substrates the cut-off temperature is believed to be the sublimation temperature of the substrates. This was definitely established for the case of ZnS on NaCl.[56]

In the case of Ge and Si substrates the cut-off temperatures are far lower than the substrate sublimation temperatures and vary with the compound being evaporated. In general, Ge and Si substrates which were held above the cut-off temperature while a II-VI compound was evaporated onto the surface, exhibited afterwards a pitted, roughened or tarnished appearance. This suggested that some form of chemical attack had taken place.

Holt and Steyn[56] studied, in detail, the case of CdS on Si. They found that the problem was particularly severe, as the deposition cut-off temperature at 10^{-5} torr was only 300°C, and only polycrystalline films were obtained below this temperature. Cleaner techniques and a better vacuum (an oil-free 10^{-9} torr) brought the cut-off temperature down to 250°C. Thermodynamic calculations were made of the free energy changes involved in the reactions:

$$Cd(g) + \tfrac{1}{2} S_2(g) \rightarrow CdS(s) \qquad (2.18)$$

$$Si(s) + \tfrac{1}{2} S_2(g) \rightarrow SiS(g) \qquad (2.19)$$

$$Si(s) + S_2(g) \rightarrow SiS_2(s) \qquad (2.20)$$

where (s) and (g) indicate that the material is solid or gaseous respectively. The main features of the results are shown in Figure 2.6. The gain in energy on forming the compounds is plotted downwards on this graph. The lower lying line, for any given temperature and pressure, therefore represents the energetically favoured reaction. It can be seen that the reaction forming CdS becomes less favourable as the temperature rises, because the CdS formation lines have positive slopes. On the other hand, the reaction producing the volatile product, SiS, becomes more energetically favourable with increasing temperature. Thus, for any given vapour pressure of the constituent gases there is a cross-over temperature. Below this temperature CdS forms and a film grows, while above it SiS forms and vapour-phase etching of the Si substrate takes place. From Figure 2.6, the cross-over temperatures (deposition cut-off temperatures) were about 200°C at 10^{-9} torr, 300°C at 10^{-6} torr and 450°C at 10^{-3} torr. Holt and Steyn[56] confirmed experimentally that the deposition cut-off temperature was in fact pushed up to above 400°C by increasing the sulphur pressure in the vacuum system to this extent.

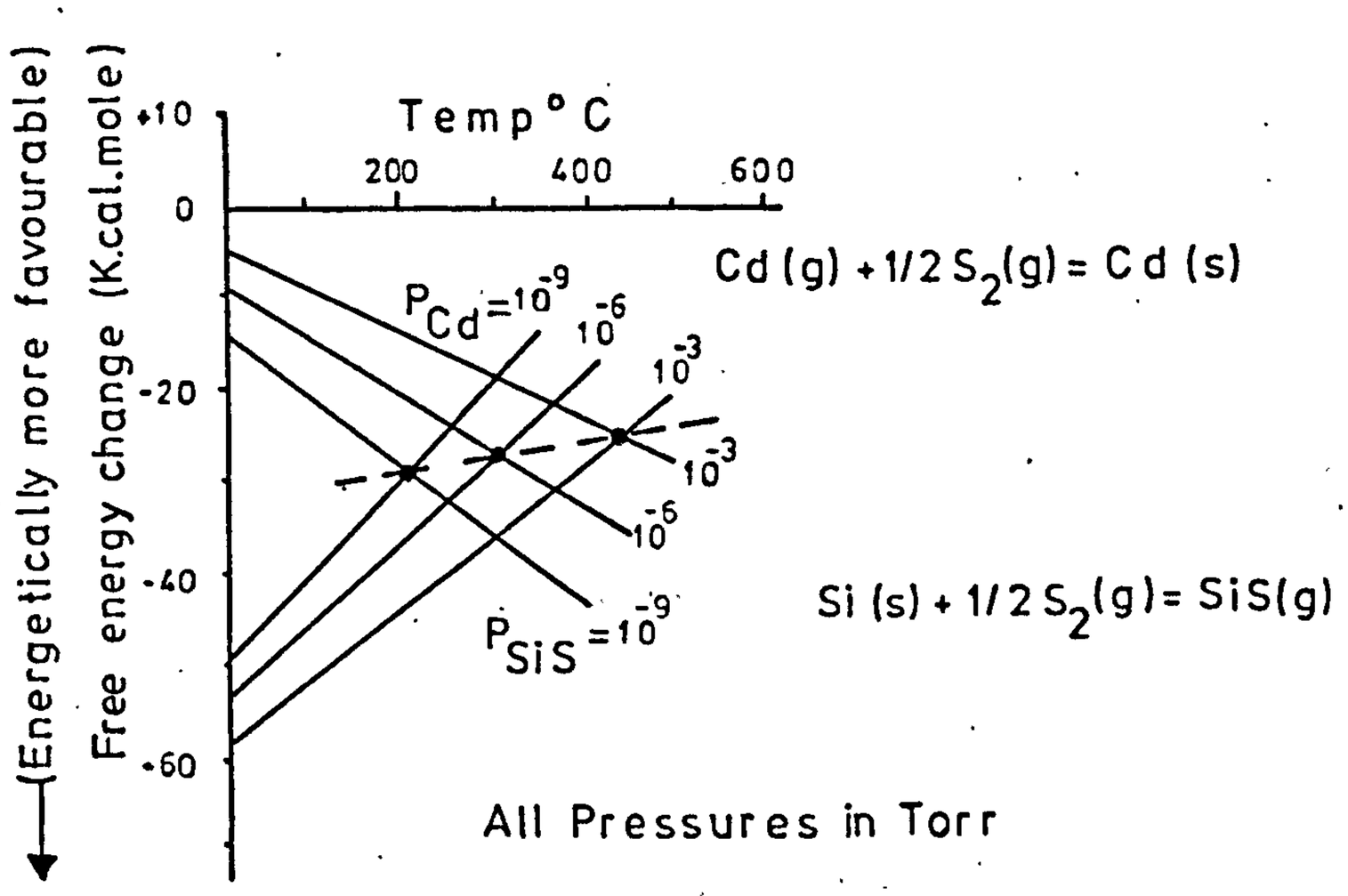


Fig 2.6 Calculated free energy change curves for reactions between Cd and S vapour and a Si surface (56)

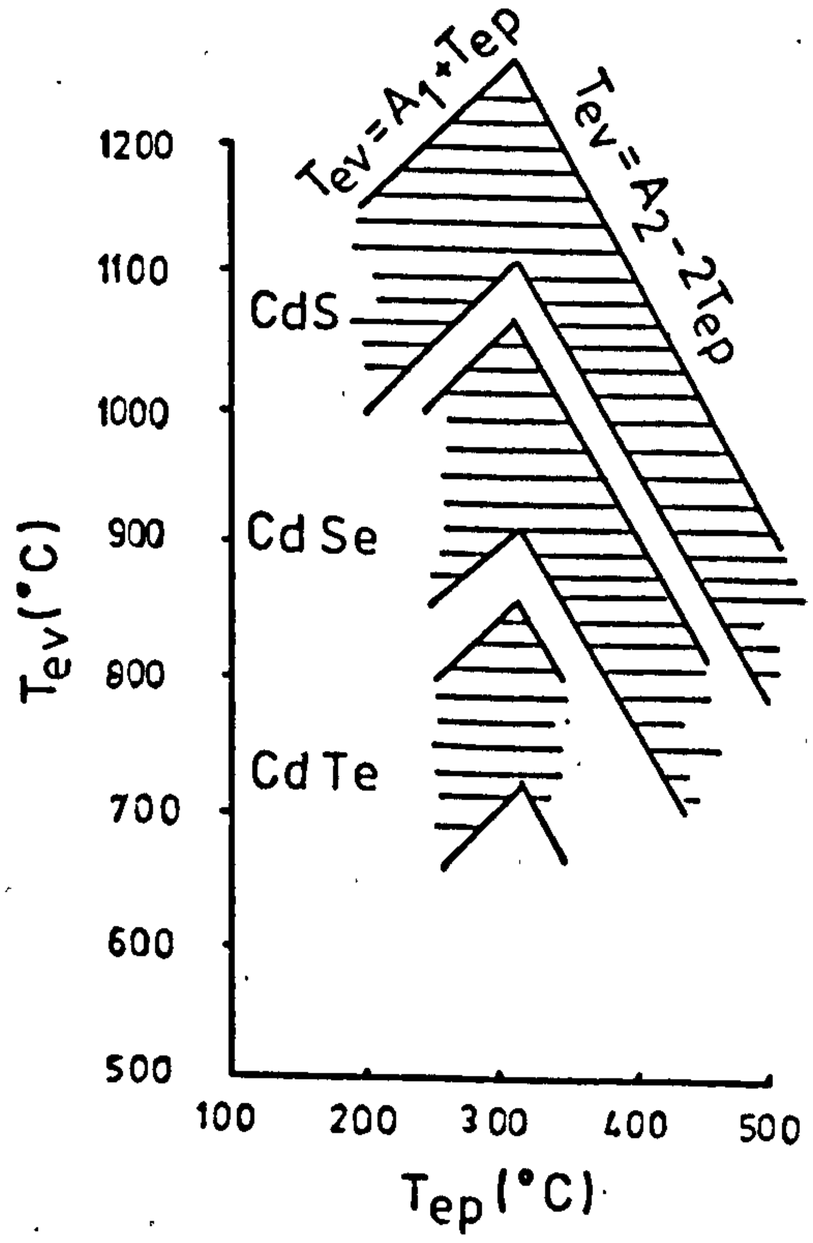


Fig 2.7 Conditions of substrate temperature T_{ep} and evaporator temperature T_{ev} for epitaxial growth (hatched area) (66)

Kalinkin et al.[66] and Muravjeva et al.[67] studied the epitaxial growth of the II-VI compounds, evaporated from Knudsen cells in vacuo in the 10^{-4} torr to 10^{-5} torr range, on cleavage faces of mica. They found that epitaxial growth only occurred for certain combinations of the substrate ("epitaxial") temperature T_{ep} and the evaporator temperature T_{ev}, as shown in Figure 2.7. Single-phase epitaxial films were obtained for the growth conditions represented by points in the cross-hatched areas. Points outside these areas represent conditions giving rise to polycrystalline, partially-ordered, films. Muravjeva et al, state that over the temperature range 200-300°C gases and water vapour are gradually desorbed from mica surfaces. They suggest that this may be partly responsible for the form of the relations they found.

2.6.4 Annealing

A possible method of improving the structural perfection of as-grown epitaxial films further is by annealing. However, in some cases it has been found that annealing has no effect on the structure that is detectable by T.E.M. examination. Chopra and Khan[60] found that CdS films with either the sphalerite (100) or the wurtzite (0001) structure were unchanged on annealing at temperatures of up to 600°C in a hot stage in a T.E.M.

A similar negative result was found in the case of (0001) wurtzite structure films of CdTe on (111) Ge substrates, which were unchanged by annealing at 400°C for up to 3 hours. On the other hand, while (100) sphalerite-structure films of CdTe on (100) Ge substrates showed no phase-change on annealing for the same time at this temperature, the films did undergo some reduction in the density of defects.[68] A reduction in the streaking of the diffraction pattern was observed after annealing, the streaking being a result of a high density of planar defects.

The annealing of sphalerite-structure (100) films of ZnS at 350, 450, and 550°C for 1 hour in vacuum or in H_2S was ineffective in reducing the defect density. However, it was found that annealing at 550°C in H_2S did lead to the appearance of satellite spots in the diffraction patterns, which had originally only contained streaks, so that some form of phase-change was apparently initiated by this treatment.(69)

A dramatic improvement in film structure as a result of annealing has been reported by Newbury and Kirk.(70) Films of ZnSe evaporated onto (100) surfaces of Ge were sealed in evacuated quartz ampoules containing small lumps of ZnSe. These films which had been grown at 430°C were annealed at 900°C for 2 hours. Sharply defined Kikuchi patterns were obtained, showing that the film was single crystal. The stacking faults and dislocations in the micrographs were well resolved and the stacking fault density was estimated to be of the order of 10^7 cm^{-2}, a reduction from 10^{13} cm^{-2} found before annealing.

2.7 Summary

This chapter has reviewed the various stages in the formation of a film of one material on the surface of another material. It has been pointed out that there is a distinction between the use of a separate source of Cd and S, and using compound CdS to grow films of cadmium sulphide. As the vapour pressure criteria of Gunther's model for condensation is satisfied, it was thought that it should be possible to grow stoichiometric films of CdS in situations where the vapour pressures of Cd and S can be controlled.

The remaining sections of the chapter were concerned with the growth of epitaxial films. Epitaxial growth is only possible under certain conditions, e.g. a high degree of substrate purity and cleanliness, and suitable substrate orientation and temperature. There are special problems

associated with the growth of CdS on silicon both because of the thin SiOx layer, normally present, which must be removed, and because of the probable chemical reaction between CdS, in vapour form, and the Si substrate.

CHAPTER 3 THEORY OF nCdS-pSi HETEROJUNCTION PHOTODETECTOR

3.1 Introduction

In common with homojunction diodes, the photodetection characteristics of the nCdS-pSi heterojunction are determined by the junction barrier potential. Consequently it is important in the understanding of the photo-characteristics to establish a band model for such diodes. In addition, the basic I-V characteristics of heterojunctions are related to the photo-characteristics, as they are also determined by the junction potential. It is interesting to compare various features of heterojunction diodes with those of homojunction diodes. An important feature is that of surface states. In a properly fabricated homojunction diode surface states are not relevant in the actual junction; furthermore it is possible to minimise the effect of surface states in a p-n homojunction diode by suitable choice of metal contact and doping conditions. In contrast, for a heterojunction, surface states occurring in the contact region between the two semiconductor materials are likely to be very important. Clearly, it is essential to allow for the effect of surface states when formulating a model for a heterojunction diode. Band models are proposed for the situation, both with and without surface states, and the experimental results are compared with both these cases in Chapter 7.

The model gives a useful insight into the nCdS-pSi device physics and also substantial qualitative and quantitative agreement with the current-voltage and photodetection characteristics that are found experimentally. The effect of recombination is allowed for by including an empirical coefficient n in the usual exponential I-V characteristics.

3.2 The Homojunction Diode

It is worthwhile reconsidering the salient features of the homojunction diode before describing the additional factors involved in a heterojunction. This approach brings out the differences between the two structures more clearly.

The theory of the p-n junction is basic to an understanding of the physics of many semiconductor devices.

The theory of the current-voltage characteristics of p-n junctions was established by Shockley.[77] This theory was then extended by Sah et al.[78] and by Moll.[79]

Figure 3.1 shows a number of diagrams relevant to the understanding of an abrupt p-n junction in thermal equilibrium. It is possible to write expressions for the number of electrons, n, in the conduction band and the number of holes, p, in the valence band. These equations are written on the assumption of Boltzmann statistics, i.e. in a nondegenerate situation.

$$\text{(In n-region)}\quad n = N_D = N_c \exp -\left(\frac{E_{cn}-E_{Fn}}{KT}\right) = N_c \exp -\left(\frac{-qV_n}{KT}\right) \tag{3.1}$$

$$\text{(In p-region)}\quad p = N_A = N_v \exp -\left(\frac{E_{Fp}-E_{vp}}{KT}\right) = N_v \exp\left[-\frac{E_{Fp}-E_{cp}-E_g}{KT}\right]$$

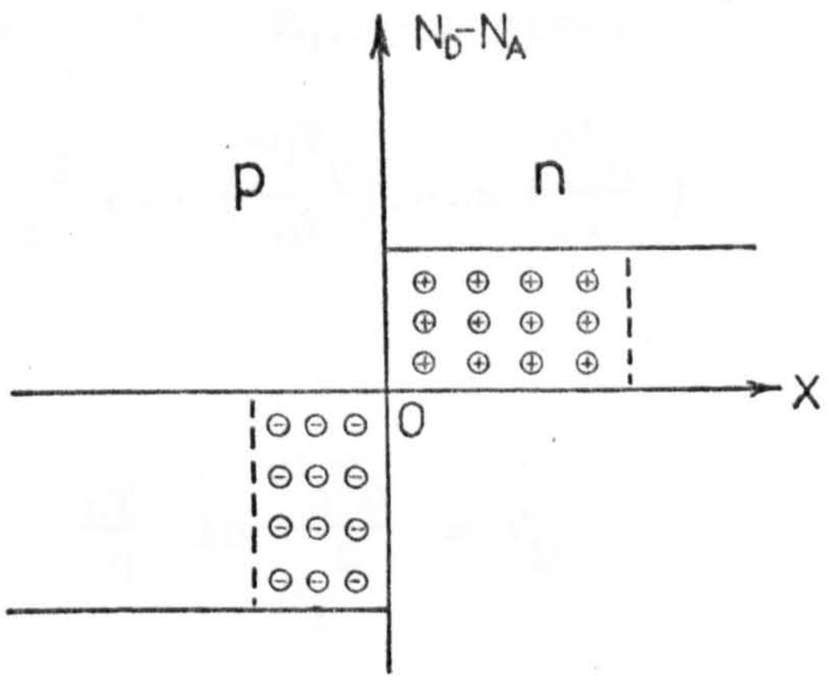
$$= N_v \exp\left(\frac{-E_g}{KT}\right)\exp\left(\frac{-qV_p}{KT}\right) \tag{3.2}$$

Also it can be shown that

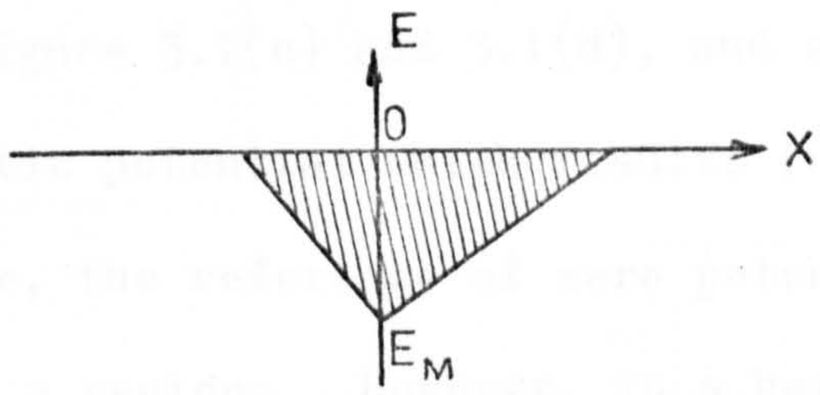
$$n_i^2 = N_c N_v \exp\left(\frac{-E_g}{KT}\right) \tag{3.3}$$

where n_i is the intrinsic carrier concentration. Substituting from Eq. 3.3 into eq. 3.2 gives

$$N_A = \frac{n_i^2}{N_c} \exp\left(\frac{-qV_p}{KT}\right) \tag{3.4}$$



(a)



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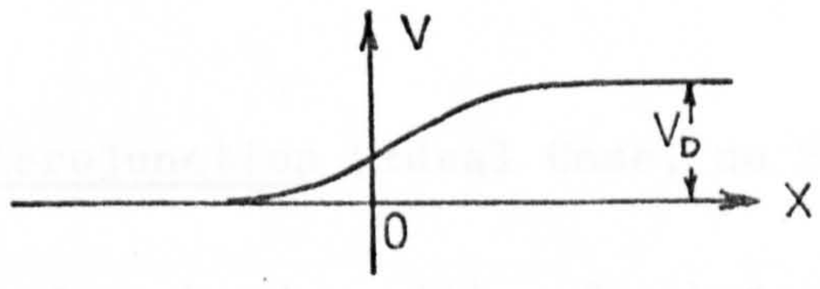

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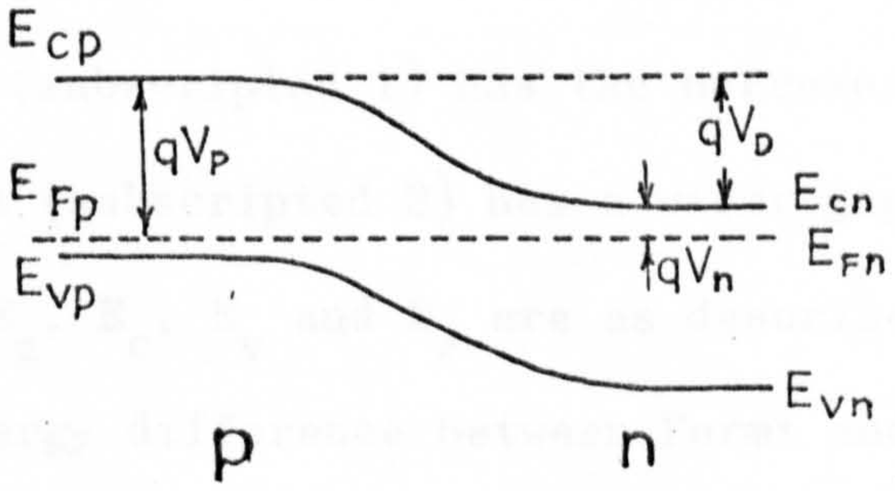


(d)

Fig. 3.1 Abrupt p-n junction in thermal equilibrium
(a) impurity distribution
(b) field distribution
(c) potential variation with distance
(d) energy band diagram, where V_b is the built-in voltage.

Multiplying Eq. 3.4 by Eq. 3.1 gives

$$N_A N_D = n_i^2 \exp\left(\frac{-qV_p}{KT}\right).\exp\left(\frac{qV_n}{KT}\right) \qquad (3.5)$$

Hence

$$V_p - V_n = \frac{KT}{q} \ln \frac{N_A N_D}{n_i^2} = V_D \qquad (3.6)$$

This equation gives the diffusion potential, or built-in voltage, V_D, as shown in Figure 3.1(c) and 3.1(d), and shows that it is the difference in electrostatic potential which results in V_D. In the case of a homojunction diode, the reference of zero potential is arbitrary as it applies to both p and n regions. However, in a heterojunction, the reference of zero potential must be the same for both regions i.e. the vacuum level.

3.3 The Heterojunction (Ideal Case, no Surface States)

The inferface band profile of a heterojunction, in a simple case is shown in Figure 3.2. First of all let us consider two different semiconductors in isolation as illustrated in Figure 3.2(a). The material on the left (subscripted 1) has the narrower gap and is p-type, while that on the right (subscripted 2) has a wider gap and is n-type. The bulk parameters E_g, E_c, E_v and E_F are as described previously. The work function ϕ is the energy difference between Fermi and vacuum levels, while the electron affinity θ is the energy required to raise an electron from the bottom of the conduction band to the vacuum level.

On bringing the two materials into contact, carriers are redistributed through the interface region, in direct analogy with the homojunction case, until thermal equilibrium is reached. This situation is illustrated by Figure 3.2(b), which does not include the effect of charged interface states, or traps within the band gap.

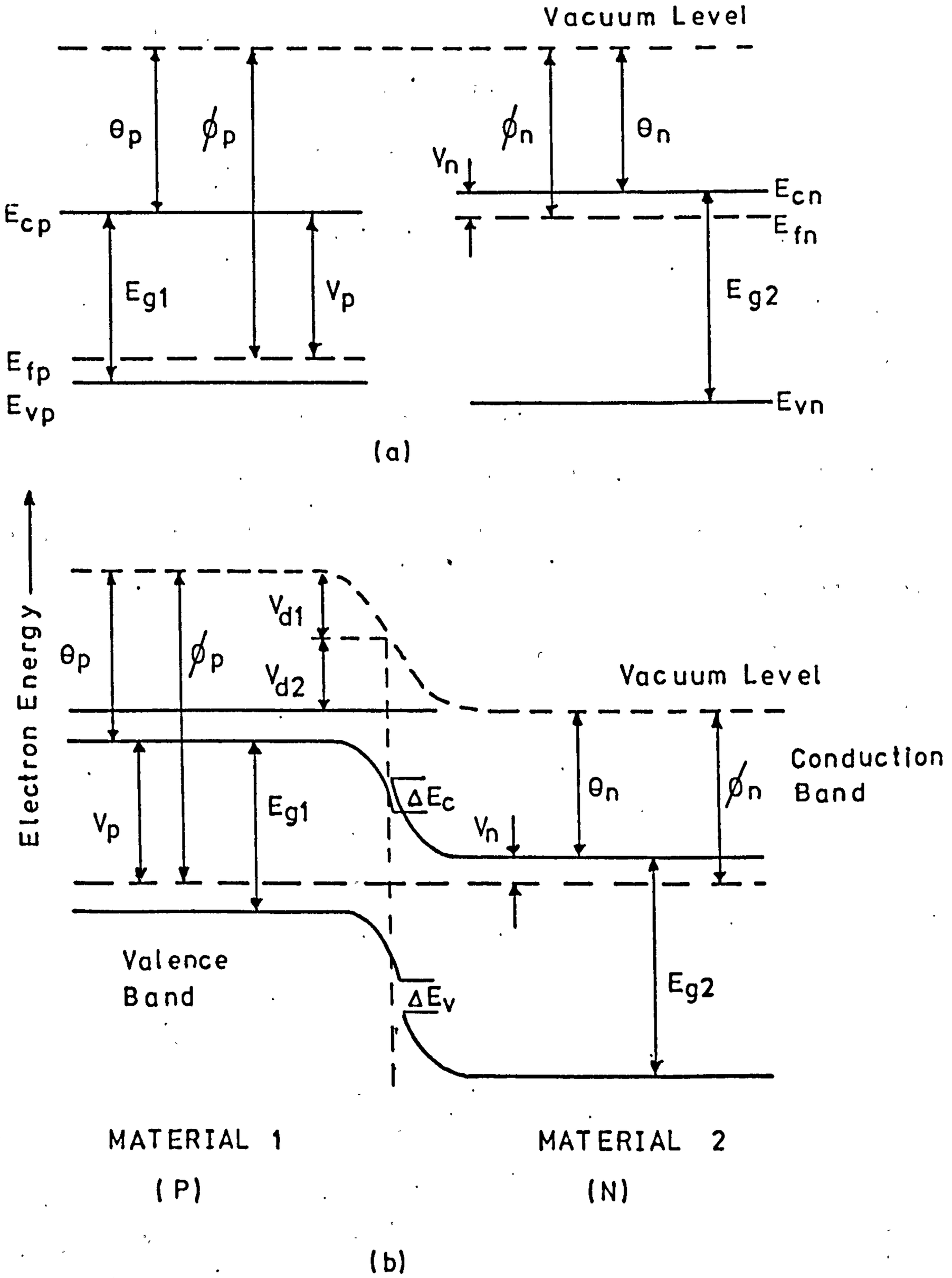


Fig 3.2 Heterojunction band diagram

In order to make use of equations 3.1 and 3.2 account must be taken of the fact that the barrier potential is not simply due to the potentials V_n and V_p, as in the homojunction. This is because the band edges E_{cp} and E_{cn} are at different potentials with respect to the reference point, i.e. the vacuum level. The barrier potential, V_D, is the difference in work function, ϕ, for the two materials.

$$V_D = \phi_p - \phi_n$$

$$= (\theta_p + V_p) - (\theta_n + V_n) \qquad (3.7)$$

where the subscripts p and n refer to the p and n-type materials respectively. Clearly Eq. 3.7 simplifies to the homojunction case when $\theta_p = \theta_n$. Another difference, in the heterojunction case, is that the potential of the valence band edge is $\theta + E_g$, and in consequence the hole barrier potential is different from the electron barrier potential, because of the difference in the energy gaps. This difference in barrier potentials can be illustrated by writing the barrier potentials in terms of hole and electron concentrations:

$$n_n = N_{cn} \exp - \frac{(E_{cn}-E_{Fn})}{KT} \qquad (3.8)$$

$$n_p = N_{cp} \exp - \frac{(E_{cp}-E_{Fp})}{KT} \qquad (3.9)$$

$$p_n = N_{vn} \exp - \frac{(E_{Fn}-E_{vn})}{KT} \qquad (3.10)$$

$$p_p = N_{vp} \exp - \frac{(E_{Fp}-E_{vp})}{KT} \qquad (3.11)$$

Using these expressions it can be shown that

$$V_{Dn} = (\theta_n-\theta_p) + (V_p-V_n) = \frac{KT}{q} \ln \left(\frac{n_n N_{cp}}{n_p N_{cn}}\right) \qquad (3.12)$$

$$V_{Dp} = (\theta_n-\theta_p) + (V_p-V_n) + (E_{g2}-E_{g1})/q = \frac{KT}{q} \ln \left(\frac{p_p N_{vn}}{p_n N_{vp}}\right) \qquad (3.13)$$

Equations 3.12 and 3.13 show that the hole barrier potential exceeds that of the electrons by ΔE_g, which is $(2.43 - 1.12) \approx 1.3$ eV in the case of the nCdS-pSi heterojunction.

Figure 3.3 illustrates four different examples of the nCdS-pSi heterojunction showing the effect of changes in the Si doping, with the assumption that there are no surface states. The valence band of the CdS is not shown for clarity. It is clear from Figure 3.3 that the diffusion potential can be varied by changing the doping of either or both of the semiconductor materials.

The position of the Fermi level in the CdS film is estimated as 0.3 eV with the assumption that $N_c = 5 \times 10^{17}$ cm^{-3} and $N_D = 5 \times 10^{13}$ cm^{-3}. While the mobility of the CdS films can be estimated from the Hall measurements, the resistivity and hence the net carrier density is not known to the same accuracy because of the technique used. This technique is discussed in more detail in Chapter 6. The band diagrams for the nCdS-pSi heterojunction illustrated in Figure 3.3 represent a situation radically different from the homojunction diode case where both sides of the junction are depleted (i.e. the p region of holes and the n region of electrons). Figure 3.3 shows that the p-type Si region is depleted while the n-type CdS region is an accumulation region. The common feature, illustrated by figures 3.3(a), (b), (c) and (d), is that the difference in potential between the CdS and Si conduction bands at the surface is always the difference in the electron affinities $\theta_n - \theta_p = 4.8 - 4.05 = 0.75$ eV.

3.4 The Heterojunction (Including the Effect of Surface States)

The above model of the band structure of an ideal heterojunction explains some of the basic properties of a heterojunction. It explains, for example, the role of the electron affinities in determining the barrier

$\underline{\underline{N_A = 3 \times 10^{17} \text{ cm}^{-3}}}$

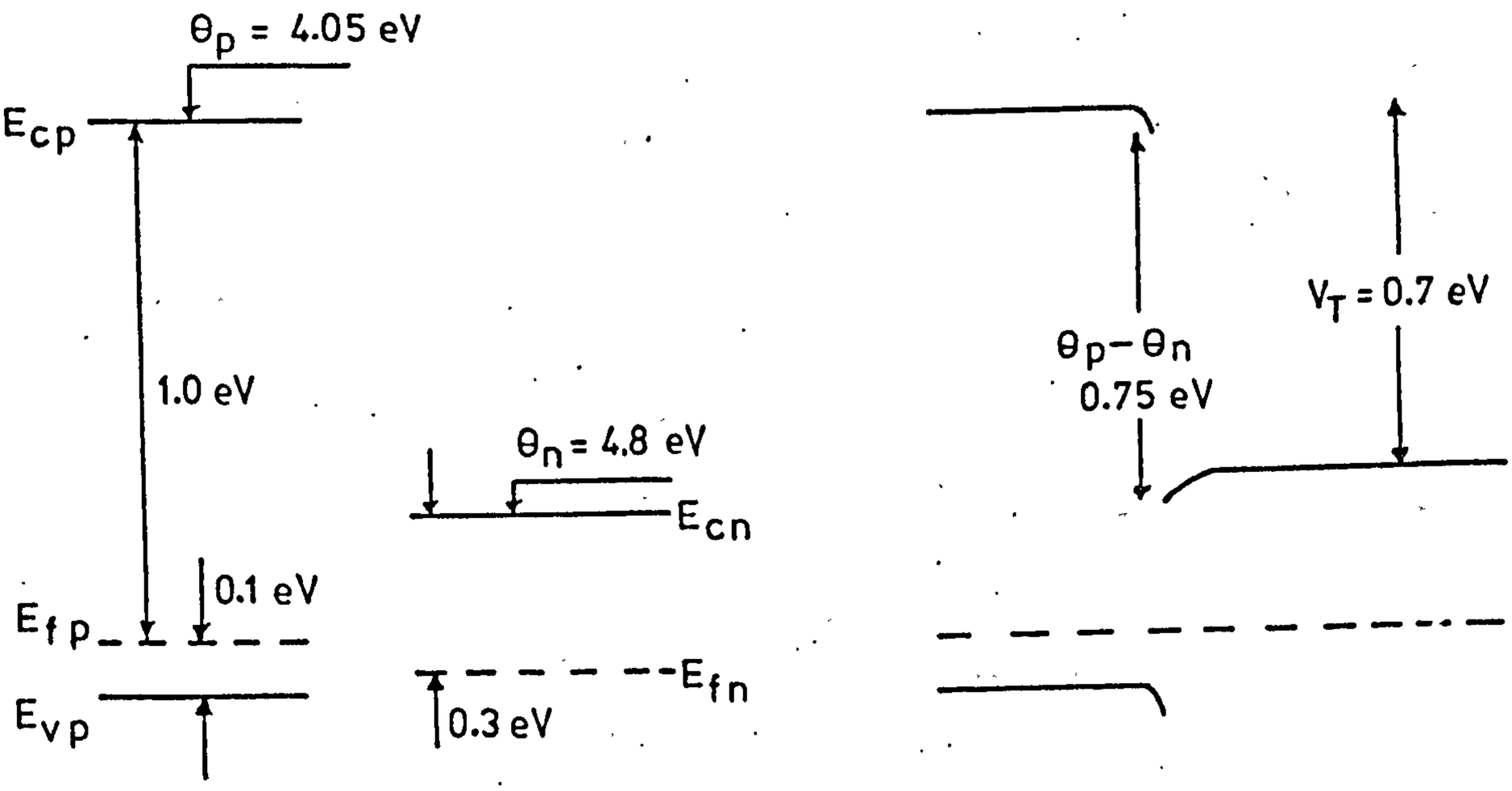


Fig 3.3(a)

$\underline{\underline{N_A = 3 \times 10^{15} \text{ cm}^{-3}}}$

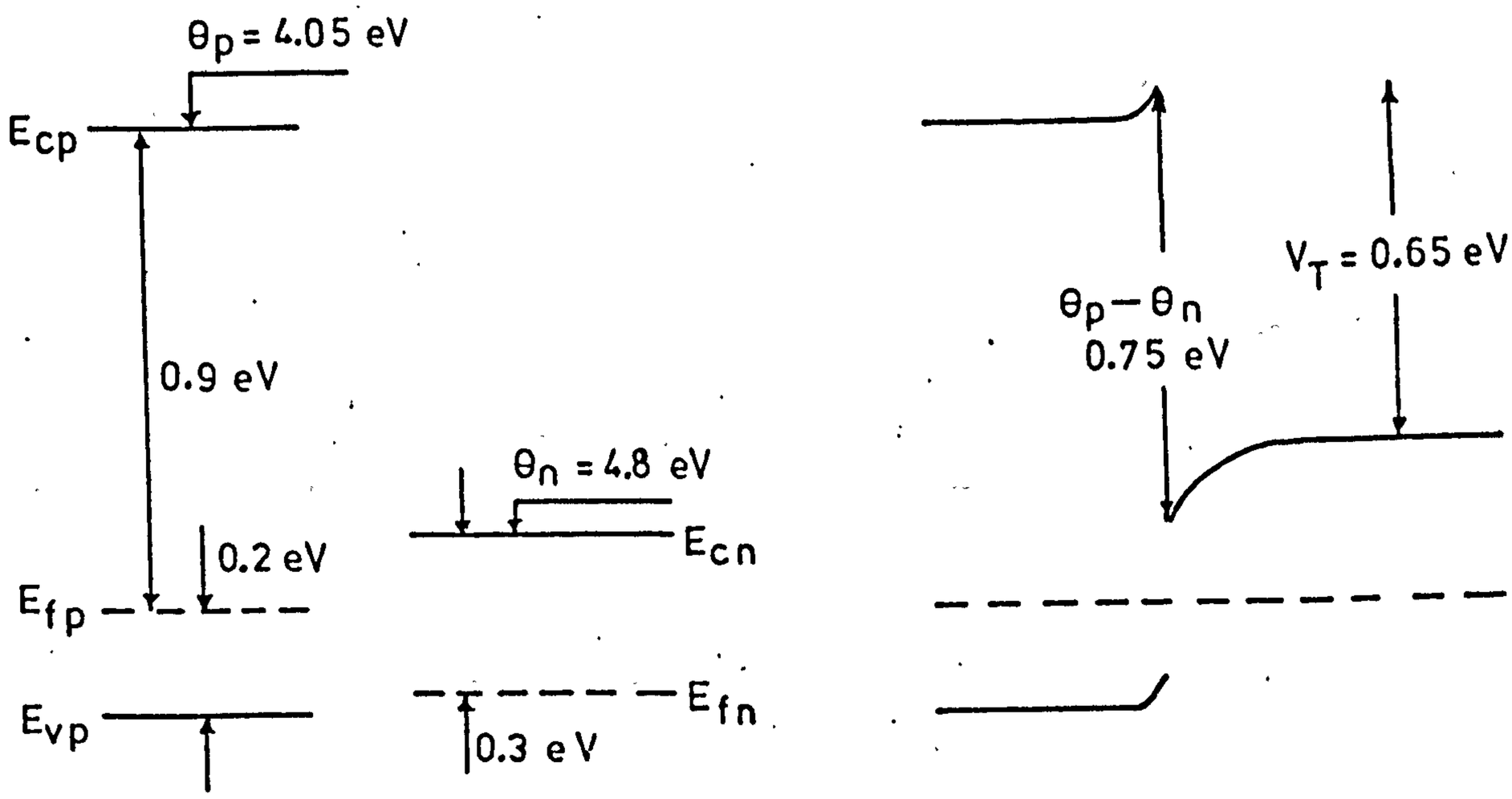


Fig 3.3(b)

$\underline{\underline{N_A = 6 \times 10^{13} \text{ cm}^{-3}}}$

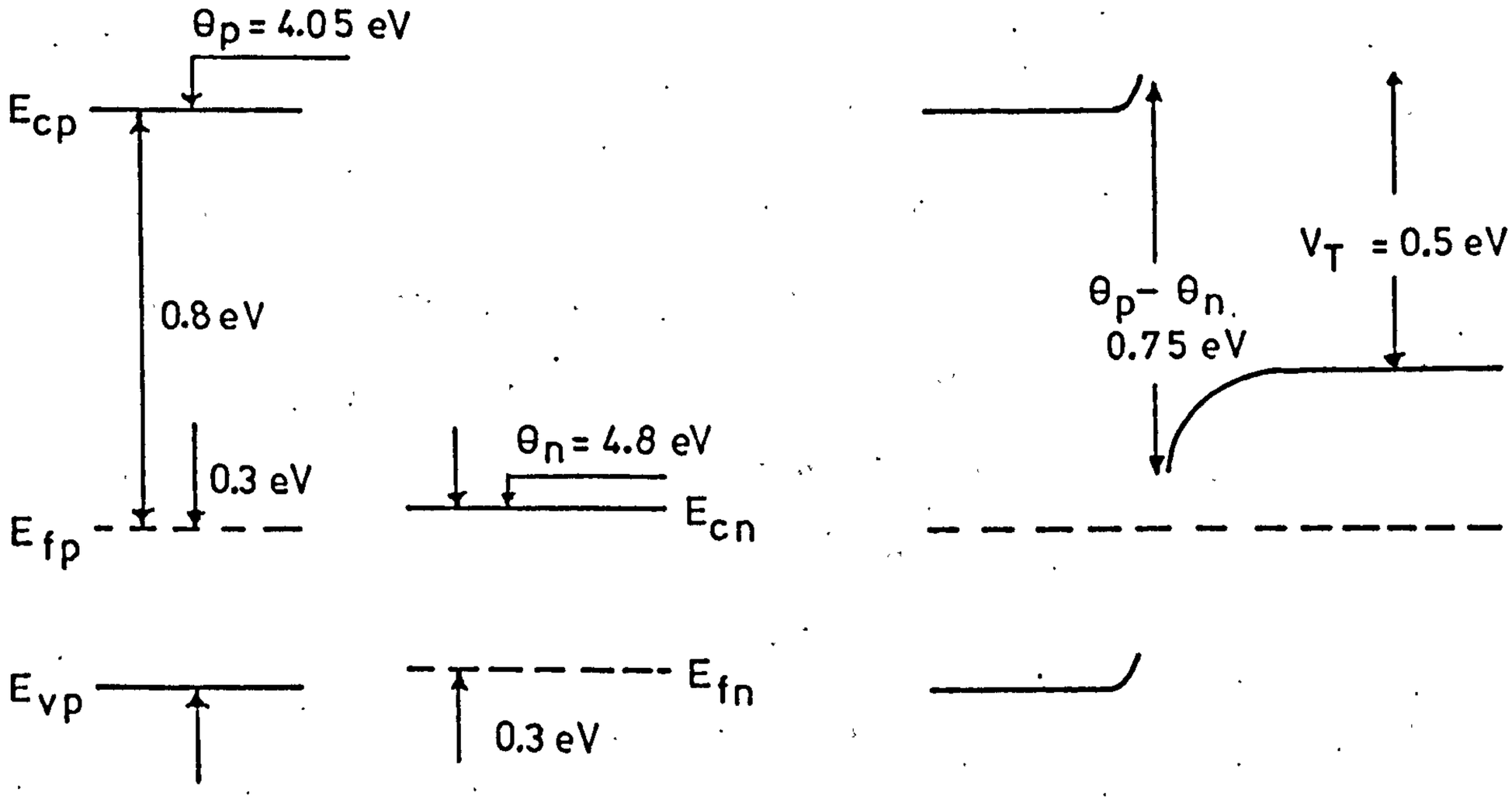


Fig 3.3 (c)

$\underline{\underline{N_A = 6 \times 10^{12} \text{ cm}^{-3}}}$

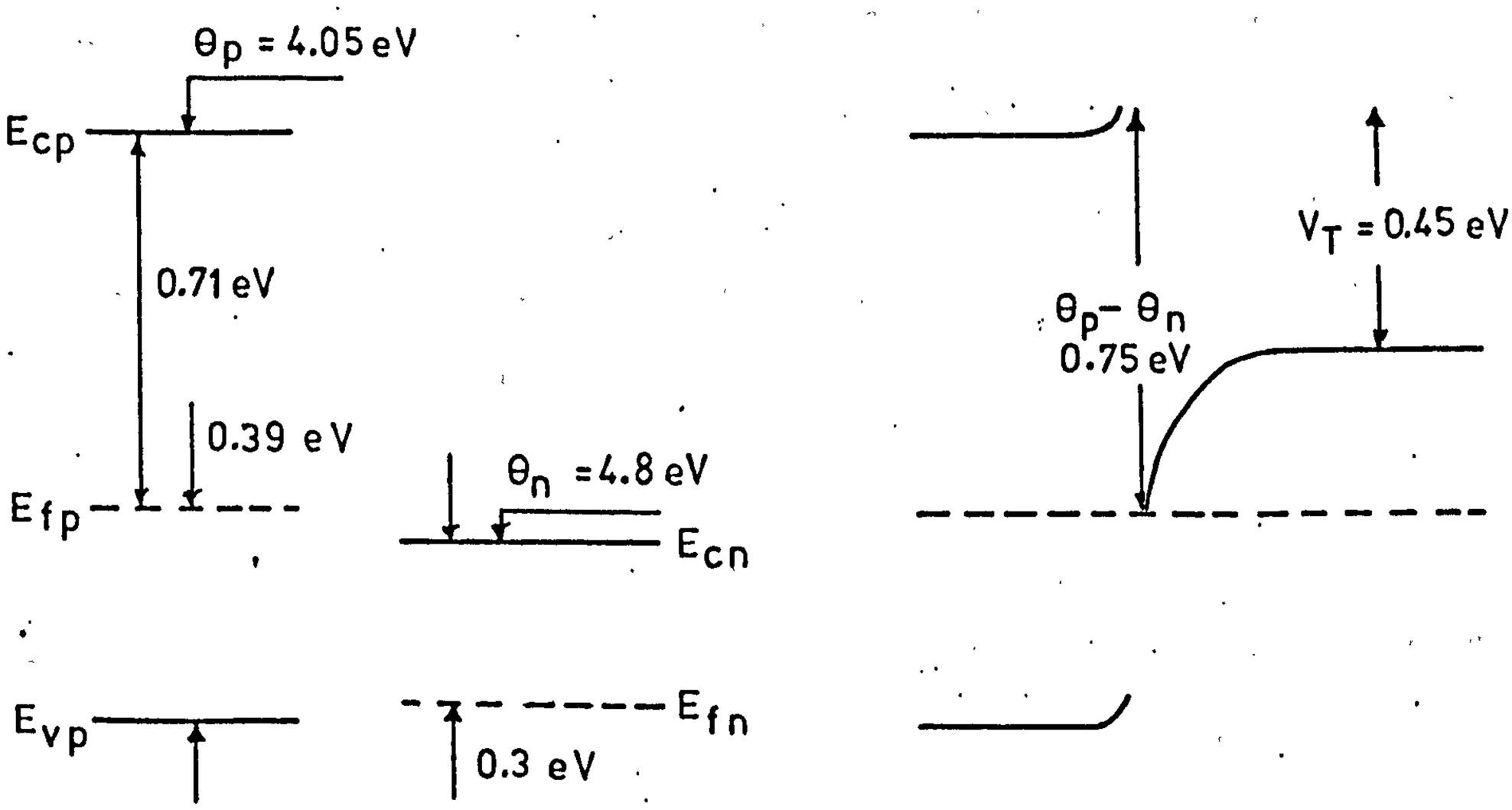
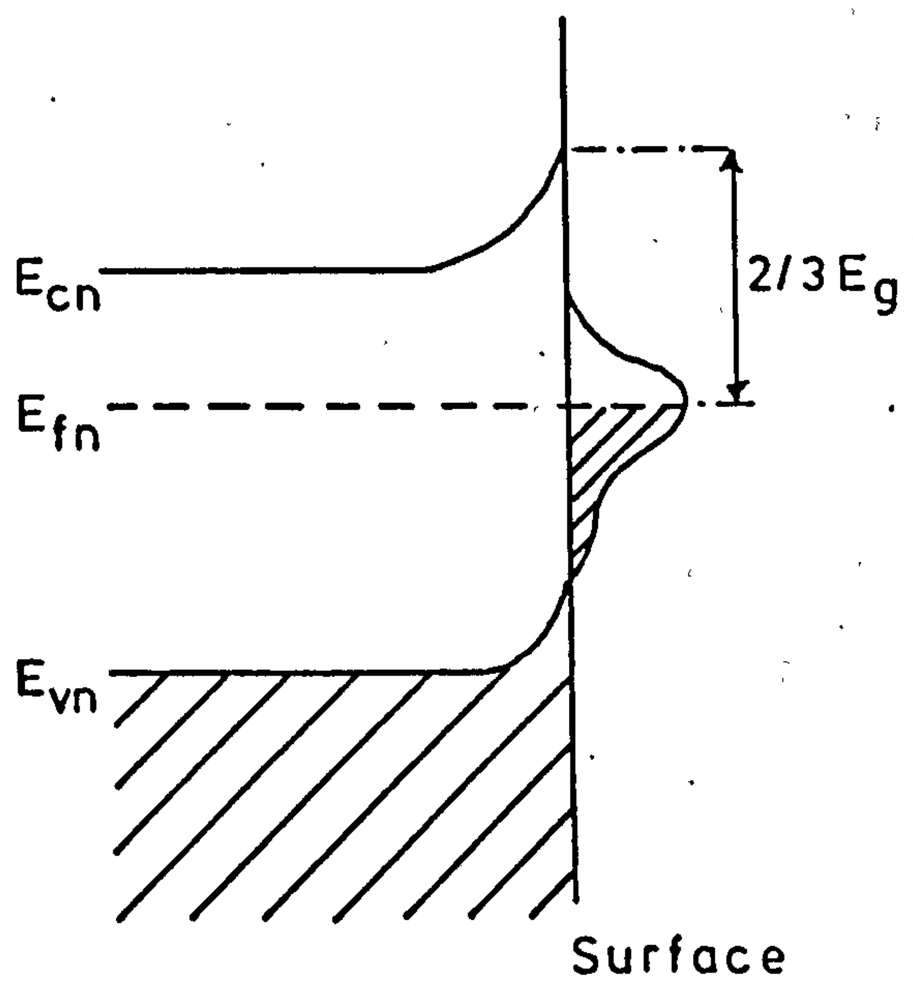


Fig 3.3(d)

potentials, through their relations to the Fermi levels. However, it does not adequately represent a heterojunction experimentally. Amongst other things, it is necessary to include the effect of surface states since a junction is formed between the surfaces of two semiconductors.

The complicated discontinuity that a free surface represents, produces a large number of localised states with energies in the forbidden energy gap. These may be either donor or acceptor states, and they arise from a number of different causes. Firstly there are the Tamm states, which come about because the surface terminates the periodic potential, leaving all of the surface atoms with an unsatisfied bond.[12] There are also states that result from the accumulation of various impurities at the surface. The surface impurity layer represents a termination that is somewhat less abrupt than an atomically clean surface. Whatever their source, the surface states seem to lie mostly near the middle of the gap (deep states), and are dense near the surface.[80] These extra states require the bands to bend, just as more shallow donor or accepter states do. In most cases, these surface states are so dense that the Fermi level must pass very close to the centre of their distribution. Figure 3.4 illustrates the expected energy band diagram, 3.4(a) showing the bands bent upwards for an n-type semiconductor and 3.4(b) showing the bands bent downwards for a p-type semiconductor. It has been found, from work on metal-semiconductor contacts, that the Fermi level at the interface in most semiconductors is "pinned" by the surface states.[81] The barrier height is independent of the metal work function and is determined entirely by the doping and surface properties of the semiconductor. Bardeen[81] found that the difference between the metal and semiconductor work functions was compensated by charge in surface states, rather than by space charge as is ordinarily assumed. Another interesting point was found experimentally by Mead and Spitzer.[82] They found that most semiconductor surfaces have a high peak density of surface states nearly one-third of the band



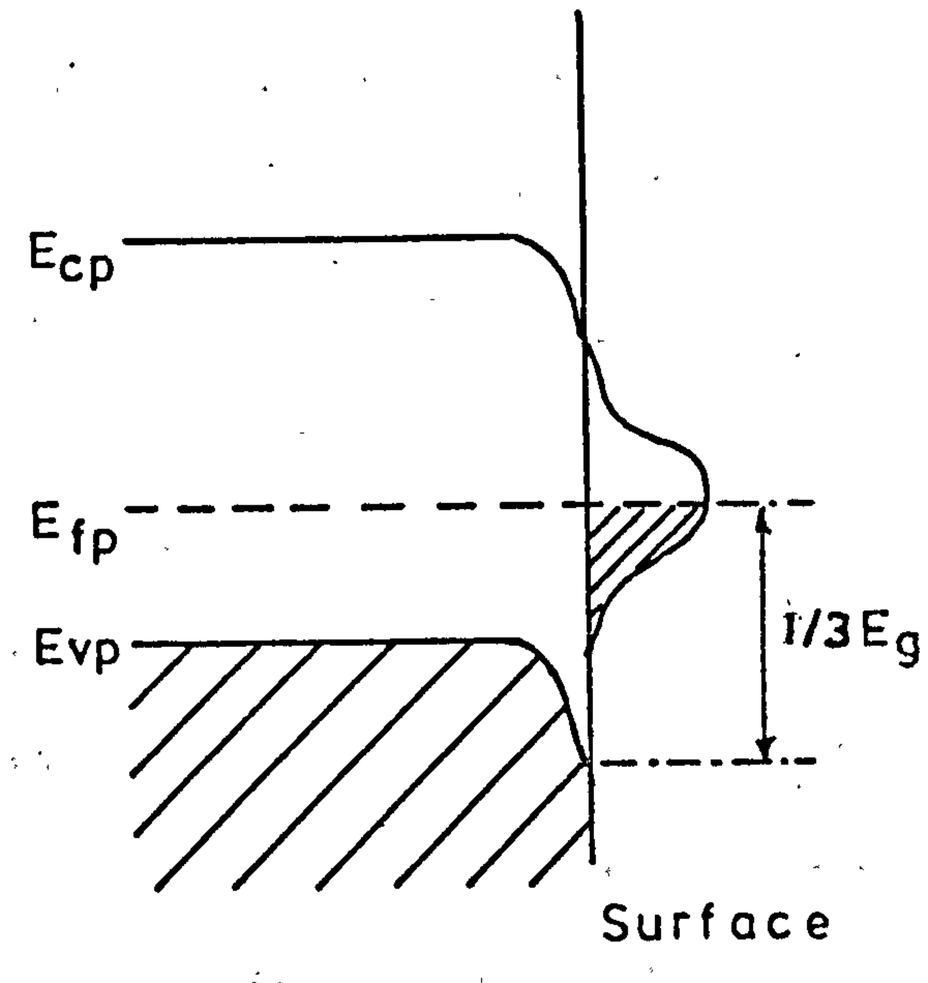


Fig 3.4

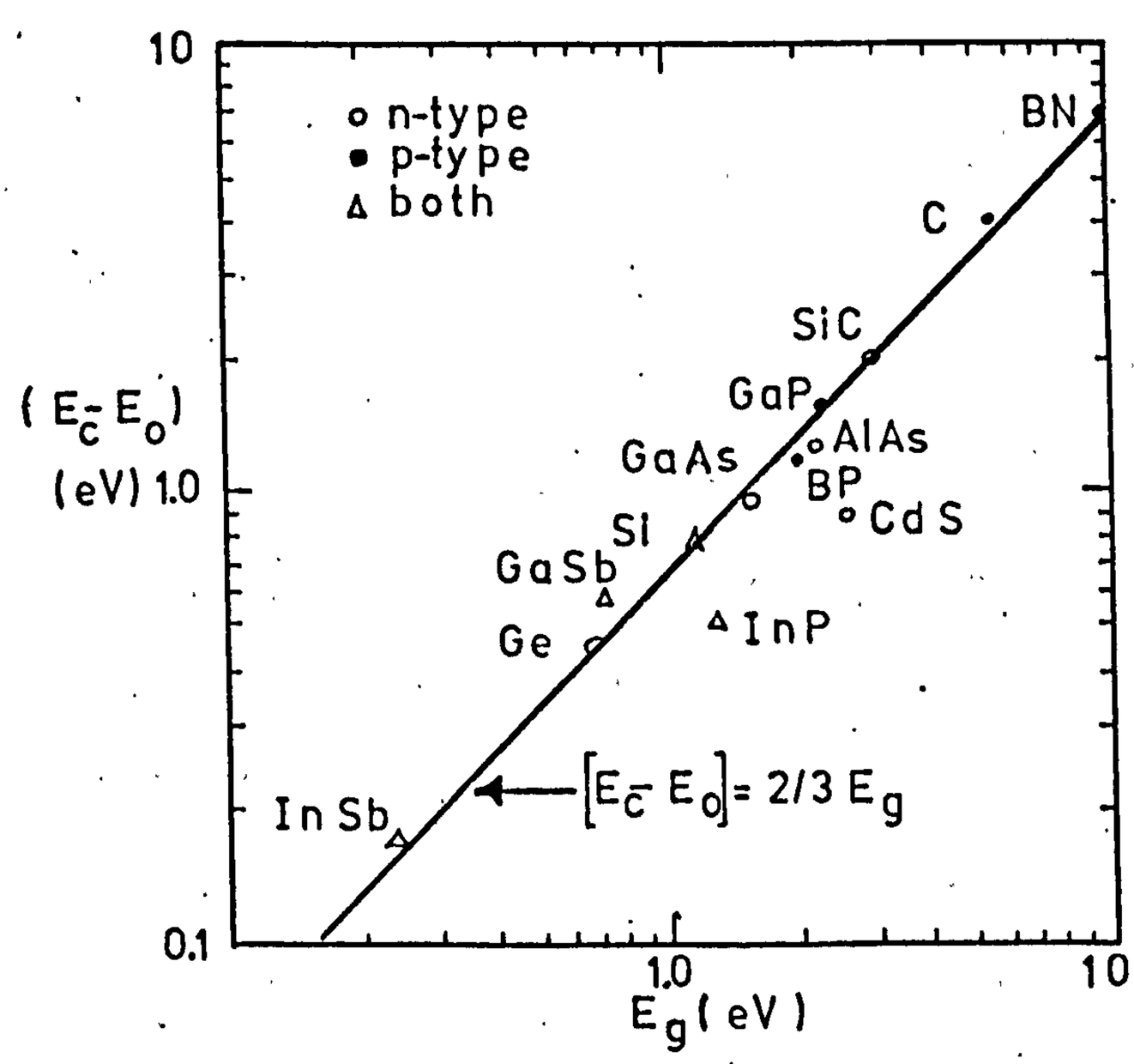


Fig 3.5 Gold contacts on various surface state controlled materials (E_o is the Fermi level at the surface) (82)

gap above the valence band edge. Figure 3.5 shows that a straight line of slope $(E_c-E_o) = \frac{2}{3}E_g$ passes through the experimental points, where E_o is the position of the fermi level at the surface. These experiments were carried out on vacuum-cleaved specimens of the semiconductors. The use of these results to predict the behaviour of surface states in a CdS-Si heterojunction is dependent on the cleanliness of the silicon substrates on which the CdS films are grown.

It will be assumed here that the surface of electron-beam cleaned silicon in vacuum approaches the degree of perfection of silicon cleaved in vacuum. Support for this viewpoint is twofold: (i) while CdS films will grow epitaxially on (111) oriented Si which has been electron-beam cleaned in vacuum, polycrystalline films are obtained on uncleaned substrates, (ii) CdS films grown on uncleaned silicon is prone to lift-off during the following photolithographic processes, whereas CdS films grown on cleaned silicon substrates adhere.

The behaviour of the metal-CdS system is radically different to the metal-Si system as illustrated by Figure 3.5. The metal-CdS system behaves as if there were a low density of surface states.[83] This may be explained by the fact that the surface states are very close to the band edge; and the Fermi level at the interface can therefore move up or down in energy over a relatively large range without requiring large amounts of surface charge to fill or empty these states.

With the assumption of the "pinning" of the Fermi level at $\frac{2}{3}E_g$ in the Si, it is possible to redraw the band diagrams of the CdS-Si heterojunction to take account of the surface states.

The effect of the surface states on the band structure for the four different silicon dopings discussed earlier is shown in Figure 3.6(a), (b), (c) and (d).

As Figure 3.4(b) illustrates, the position of the "pinned" Fermi

level at the surface in the p-type Si is determined by the bulk Fermi level which is a function of the doping. When the junction (CdS-Si) is formed, the redistribution of charge occurs between these surface states and the CdS conduction band, maintaining the difference in the electron affinities, $(\theta_{CdS} - \theta_{Si})$, as was the case when no surface states were present (Figure 3.3). When the two semiconductors, CdS and Si, are brought together there is a redistribution of carriers between the bands in the ideal case (Figure 3.3) and between the surface states and the bands in the case which includes surface states (Figure 3.6). Figure 3.6(a), (b) and (c) show that the three heterojunctions of different p-type doping in the silicon have similar band structure, although they have different barrier potentials. The junction in the silicon is depleted while an accumulation region exists in the CdS junction. The situation for near intrinsic silicon, illustrated by Figure 3.6(d), differs from Figure 3.6(a), (b) and (c) in that there is an accumulation region in both the silicon and the CdS junctions.

The effect on the photodetection properties of this difference will be discussed more fully in conjunction with the experimental results in Chapter 7.

3.5 Current-Voltage Characteristics

In the previous discussion, barrier potentials were expected to be similar to those of conventional p-n junctions in that there was a barrier voltage to electrons between the CdS and the Si. One would expect these nCdS-pSi heterojunctions, with positive barriers, to have a similar I-V relationship to that observed for conventional p-n junctions. The four heterojunction diodes, with different Si doping would have different I-V characteristics from each other not only because of the different p-type doping but also because the heterojunction with the near intrinsic silicon

$N_A = 3 \times 10^{17}\ cm^{-3}$

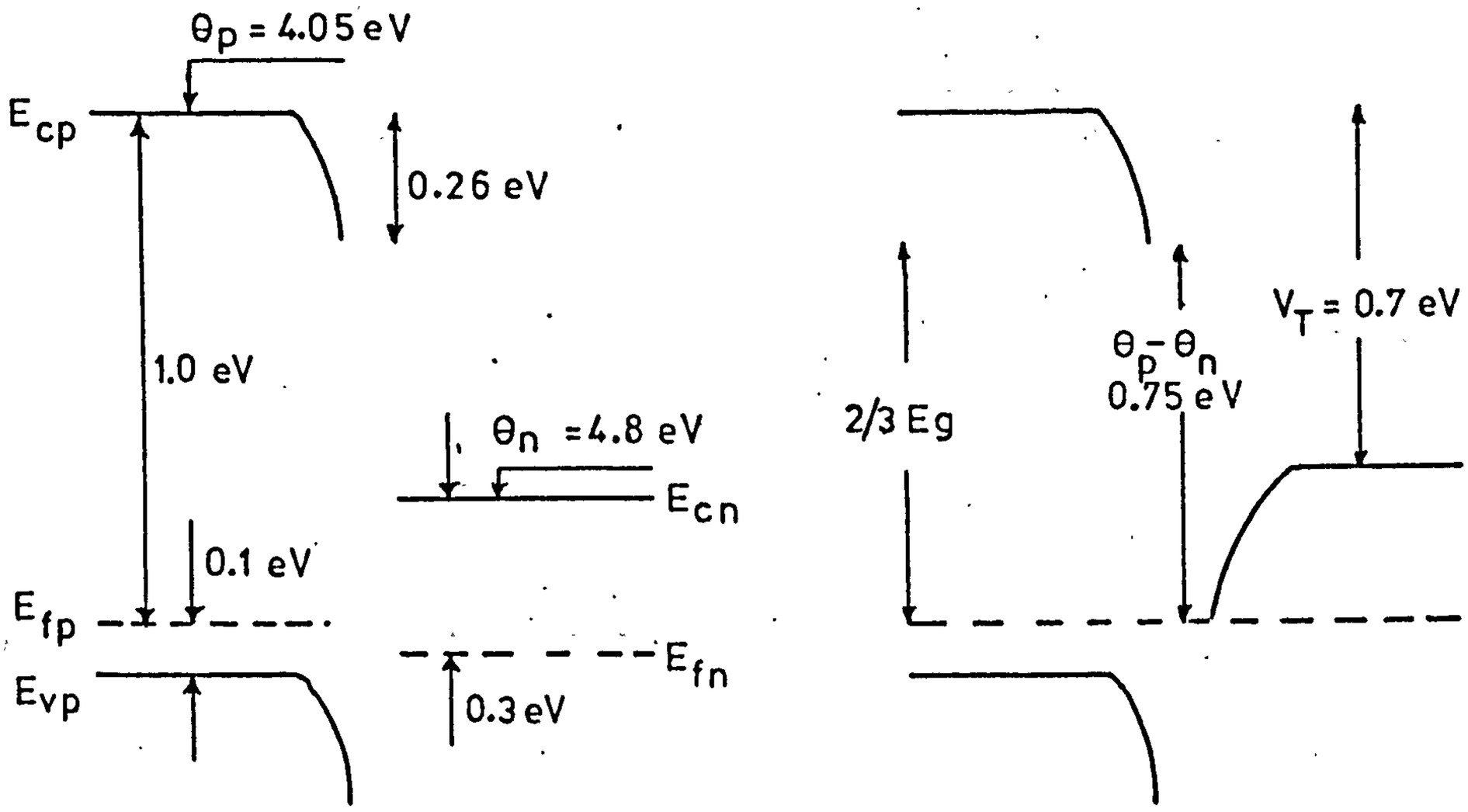


Fig 3.6 (a)

$N_A = 3 \times 10^{15}\ cm^{-3}$

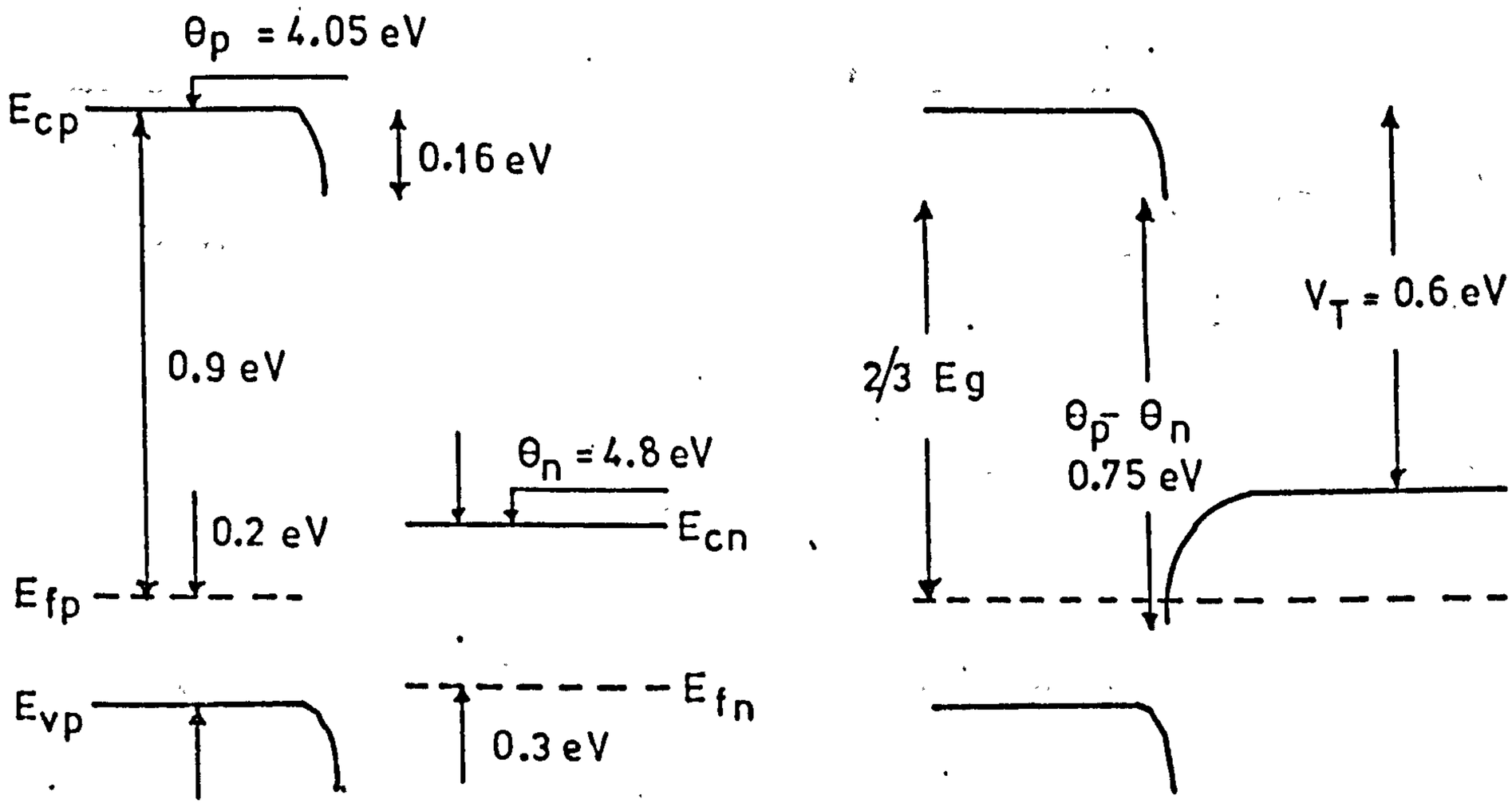


Fig 3.6 (b)

$N_A = 6 \times 10^{13}\ cm^{-3}$

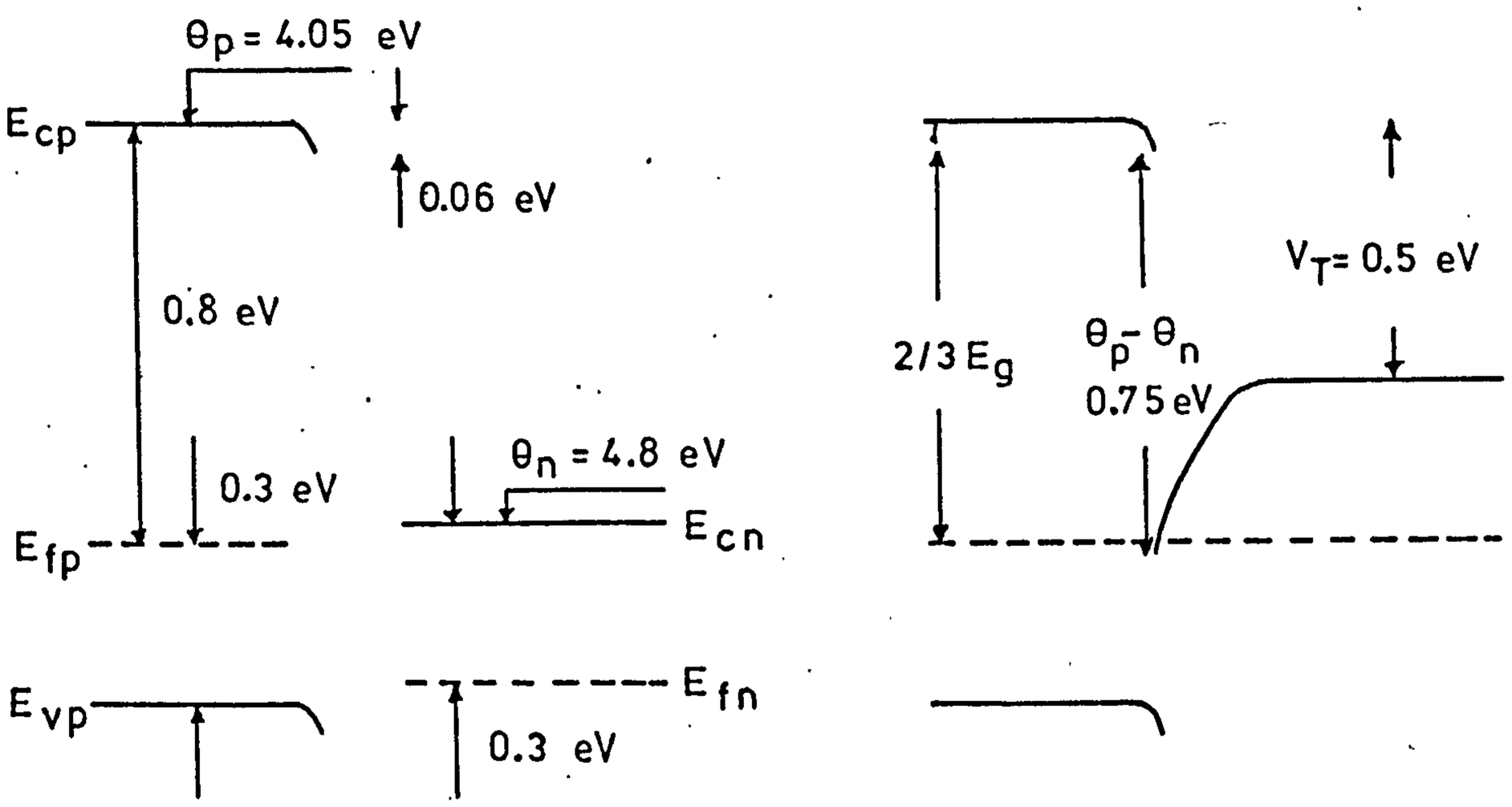


Fig 3.6(c)

$N_A = 6 \times 10^{12}\ cm^{-3}$

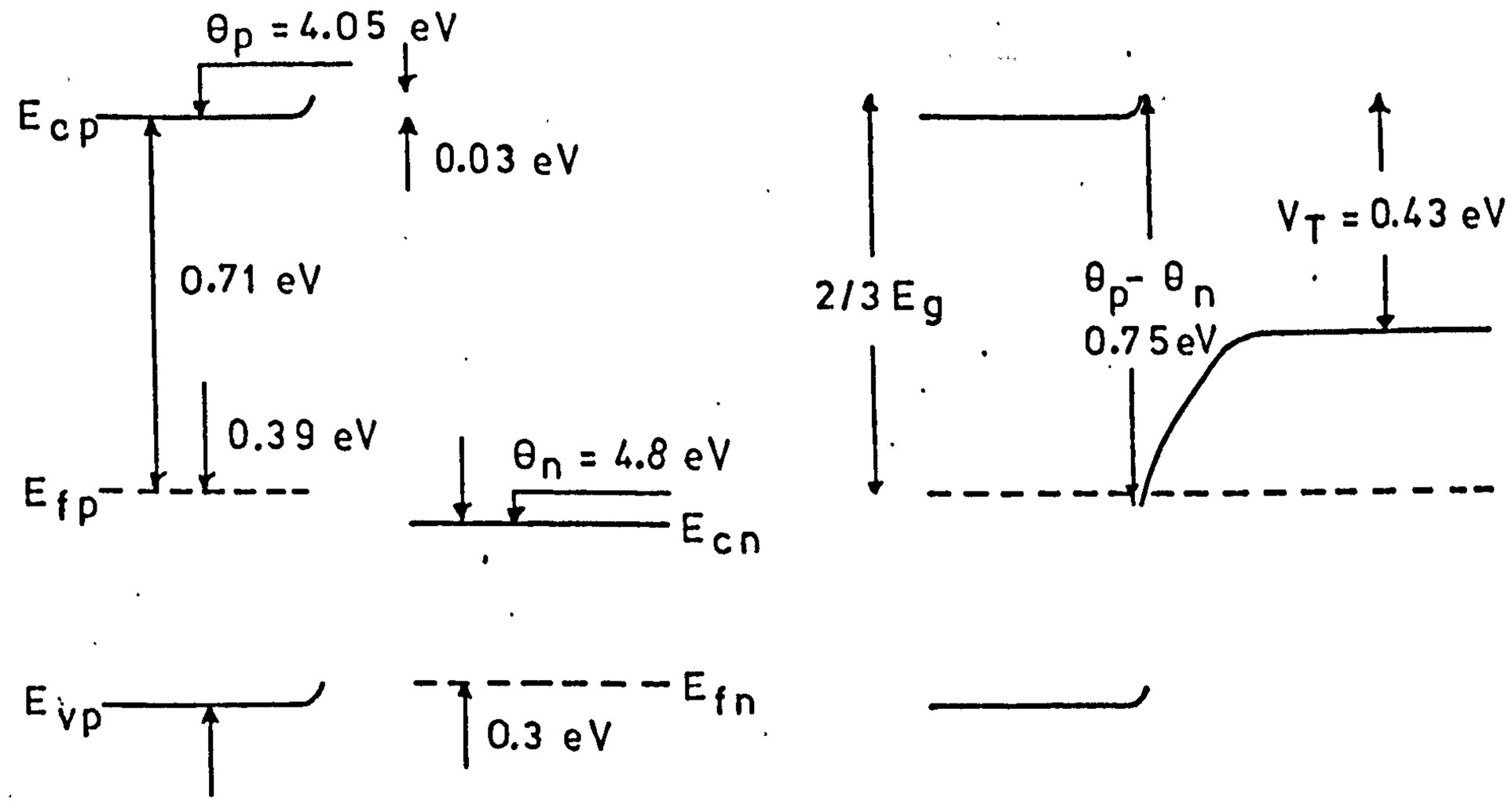


Fig 3.6(d)

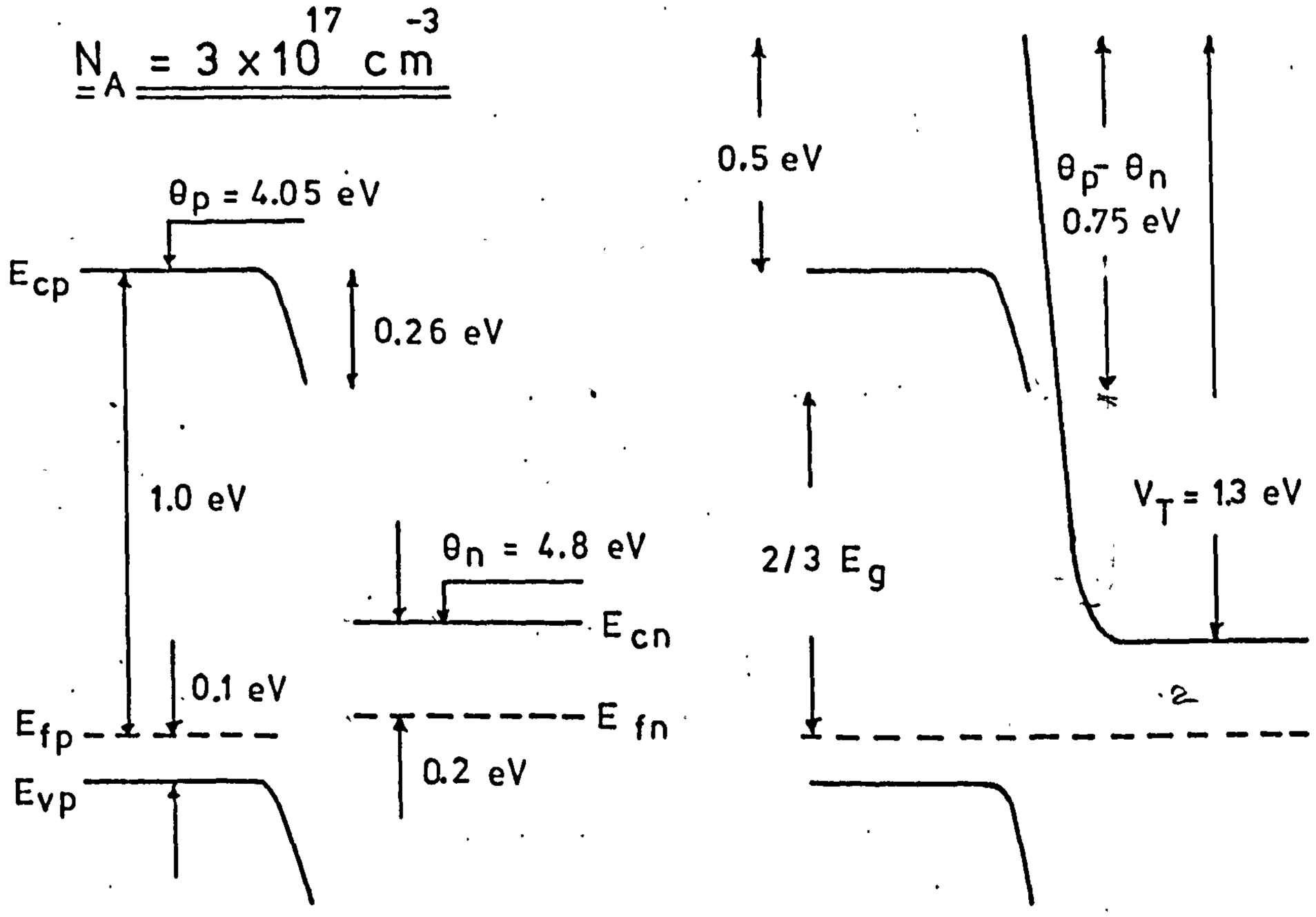

$N_A = 3 \times 10^{17}$ cm^{-3}
θ_p = 4.05 eV
E_{cp}
0.26 eV
1.0 eV
θ_n = 4.8 eV
E_{cn}
0.1 eV
E_{fp}
E_{fn}
0.2 eV
E_{vp}
0.5 eV
$\theta_p - \theta_n$
0.75 eV
V_T = 1.3 eV
2/3 E_g
2

Fig 3.6(e)

has an accumulation region in both CdS and Si junction regions. As a result of the accumulation region, this heterojunction would have I-V characteristics in which forward bias would be similar to reverse bias and reverse bias would be similar to forward bias in a conventional diode.

3.5.1 I-V Characteristics for Positive Barrier Case

The I-V characteristics for this case can be expressed as

$$J = J_S \exp\left(\frac{qV}{KT}\right) \qquad (3.14)$$

In this form, the equation only applies in the absence of recombination in the depletion region. With a forward bias voltage, the barrier potential is reduced and electrons are injected from the n region into the p region (the converse is true for the heterojunction with the accumulation region in both CdS and Si). For a given voltage the current will be determined by J_S, the saturation current density, which can be due to one of two mechanisms, namely, diffusion or barrier emission.

The saturation current density for diffusion can be expressed as:

$$J_{SD} = q\frac{D_p p_{no}}{L_p} + q\frac{D_n n_{po}}{L_n} \qquad (3.15)$$

where p_{no} is the equilibrium concentration of holes in the n-type material, D_p and L_p being the diffusion coefficient and diffusion length of holes respectively. This expression is the same as the saturation current for p-n homojunctions.

The saturation current density for barrier emission is:

$$J_{SB} = AT^2 \exp\left(\frac{-q\phi}{KT}\right); \quad \phi = V_T + V_n \qquad (3.16)$$

where A is the Richardson constant and ϕ is the barrier potential. This is the expression used to calculate the saturation current for rectifying metal-semiconductor contacts. Perlman and Feucht[84] have shown that two

distinct types of heterojunction I-V characteristic are predicted; metal-semiconductor type operation where the current is limited by the ability of the carriers to surmount the potential barrier at the junction interface; and homojunction type operation where the current is limited by the ability of the carriers to diffuse away from the junction depletion region. It is possible to decide which is the limiting mechanism by considering the magnitudes of the saturation currents, using equations 3.15 and 3.16 respectively. Table 3.1 shows the results of calculations for the four different dopings being considered. It is clear that these simple calculations, neglecting recombination effects, show that the nCdS-pSi heterojunction is barrier limited. This is the result which might be expected from the band diagrams, which include the effect of surface states. However, this analysis neglects the effects of recombination and surface leakage currents. It is justifiable to neglect these effects when considering the I-V characteristics of germanium p-n junctions at low current densities. This is not, however, the case for silicon. The effect of recombination will be discussed in section 3.7.

3.5.2 I-V Characteristics of a Negative Reverse Barrier Junction

It is evident, on examination of Figure 3.6(a), that if the position of the Fermi level in the CdS film is significantly different from the 0.3 eV estimated, this difference will be reflected in a change in the magnitude of the barrier potential. However, an unusual situation might arise if $(E_c - E_F)$ for CdS were in the region of say 0.2 eV. In this situation, the Fermi level in the CdS is above the Fermi level in the silicon, implying that electrons flow out of the CdS into the silicon for equilibrium. The CdS conduction band edge must bend upwards as shown in Figure 3.6(c), as a result of the depletion of this region caused by electrons flowing into the silicon during the equilibrium process. The position of the

Ω -cm	cm^{-3}	cm^{-3}	A/cm^2	eV	A/cm^2
ρ	N_A	n_{po}	J_{SD}	ϕ	J_{SB}
.05	3×10^{17}	1.1×10^{3}	6.9×10^{-11}	1.0	3.1×10^{-11}
5	3×10^{15}	1.1×10^{5}	6.9×10^{-9}	0.9	1.5×10^{-9}
200	6×10^{13}	4.3×10^{6}	2.7×10^{-7}	0.8	7.1×10^{-8}
2000	6×10^{12}	4.3×10^{7}	2.7×10^{-6}	0.73	1.1×10^{-6}

Where $\phi = V_T + V_n$ in Equation 3.16

i.e. $\phi = V_T + 0.3$ eV

Table 3.1

termination of the CdS conduction band is again determined by the difference in electron affinities. It is clear, in this situation, that in addition to the barrier potential illustrated in Figures 3.6(a), (b), (c) and (d), there is also a reverse barrier potential to electrons between the silicon and the CdS. This is referred to as a negative reverse barrier potential. However, unlike the situation illustrated by figures 3.6(a),(b),(c) and (d), the larger (reverse) barrier potential in Figure 3.6(c) is determined by the difference in the electron affinities and so it is questionable whether bulk electron affinities are applicable in this case. It is worthwhile considering what effect this type of barrier might have on the I-V characteristics. Because a barrier to electrons exists in both the n and p region the I-V characteristics will be of the form

$$J = J_{SF} \exp \frac{qV_F}{KT} - J_{SR} \exp \frac{-qV_R}{KT} \qquad (3.17)$$

where $V_F + V_R = V$, the applied voltage, and V_F and V_R are the applied voltages across the forward and reverse barriers respectively.

With forward bias the expression simplifies to

$$J = J_{SF} \exp \frac{qV_F}{KT} \qquad (V_F >> \frac{KT}{q}) \qquad (3.18)$$

Similarly for reverse bias one obtains

$$J = J_{SR} \exp \frac{qV_R}{KT} \qquad (V_R >> \frac{KT}{q}) \qquad (3.19)$$

The relative voltage supported in each of the semiconductors can be related to the doping levels as:

$$\frac{V_F}{V_R} = \frac{N_A \varepsilon_A}{N_D \varepsilon_D} = m \qquad (3.20)$$

where ε_A and ε_D are the relative permittivities of silicon and CdS respectively. Equations 3.18 and 3.19 can be rewritten in terms of the

applied voltage V and the constant m using the relation

$$V_R + V_F = V \tag{3.21}$$

Hence equations 3.18 and 3.19 can be written as:

$$J = J_{SF} \exp \left[\left(\frac{m}{m+1}\right). \frac{qV}{KT} \right] \tag{3.22}$$

$$J = -J_{SR} \exp \left[\left(\frac{m}{m+1}\right). \frac{qV}{KT} \right] \tag{3.23}$$

In principal the constant m can be determined from the I-V characteristics as can the forward and reverse barrier potentials. However, in practice the numerical value of n (discussed in section 3.7.1) will be different in both forward and reverse bias and so m has not been calculated experimentally.

3.6 Photo-characteristics, The Window Effect

As mentioned previously, a notable feature of heterojunctions made from two different semiconductors is the window effect. This effect is a result of the different energy gaps of the two materials comprising the heterojunction. It is worthwhile considering the case of an nCdS-pSi heterojunction with illumination on the CdS front face. At energies less than the CdS band gap, 2.43 eV, most of the radiation would be absorbed by the silicon after transmission through the CdS. At energies greater than the CdS band gap the radiation would be absorbed by the CdS, and as a result the contribution to the photocurrent due to the silicon would fall. At energies less than the silicon band gap, 1.1 eV, the photocurrent would be very low, and would be due solely to impurity levels within the band gap of either semiconductor, which could produce a photocurrent at lower energies.

As has been mentioned earlier, the principal advantage of a hetero-

junction, compared with a homojunction, as a photodetector is not basically in the voltage or current performance. The advantage is in the extent to which the surface-recombination losses and sheet-resistance losses are reduced, because the window effect allows the junction to be placed further from the surface than in a homojunction detector. The magnitude of this advantage depends on the particular design geometry, the materials chosen and other practical aspects of fabrication. The performance is adversely affected, of course, if there is a high recombination rate at the interface.

3.6.1 Reflection Losses

Since the refractive index of most semiconductors is high, (CdS, $n \approx 2.45$, Si, $n \approx 3.5$), the reflection from the surface of the photodetector can also be high.

It is possible to calculate the reflection loss at normal incidence for the nCdS-pSi photodetector.[28] The following expression is for the case where the CdS film has a real refractive index, while the refractive index of the silicon is complex. It is therefore appropriate, to a good approximation, for the range $\lambda = 0.5$ to 1.0 μm. The intensity reflectance at normal incidence R is:

$$R = \frac{r_1^2 + r_2^2 + 2r_1r_2 \cos (V-D)}{1 + r_1^2r_2^2 + 2r_1r_2 \cos (V-D)} \qquad (3.24)$$

where:

$$r_1 = \frac{n_1-n_o}{n_1+n_o} \qquad r_2 = \frac{(n_2-n_1)^2+K_2^2}{(n_2+n_1)^2+K_2^2}$$

$$V = \frac{4 \pi n_1 h_1}{\lambda_o} \qquad D = \text{TAN}^{-1} \left(\frac{2n_1K_2}{n_1^2-n_2^2-K_2^2}\right)$$

n_o, n_1 and n_2 are the refractive indices of air, CdS and silicon respectively, K_2 is the extinction coefficient of silicon, and h is the CdS film thickness. The extinction coefficient K is related to the absorption coefficient $\alpha(\lambda)$, at wavelength λ_o by the expression:

$$K = \frac{\alpha(\lambda)\lambda_o}{4\pi} \qquad (3.25)$$

Figures 3.7 and 3.8 show the real part of the refractive indices for CdS and Si versus photon energy respectively. Figure 3.9 shows the extinction coefficient (imaginary part of refractive index) for single crystal silicon as a function of photon energy. Figure 3.10 shows a graph of reflectance versus film thickness at a fixed wavelength for the nCdS-pSi heterojunction, and illustrates the fact that the film acts, to some extent, as an interference filter to the incident radiation.

Figure 3.11 shows the minimum and maximum values of reflectance, as a function of wavelength. These results will be modified by the presence of traps in the CdS film, if such traps cause significant absorption.

3.6.2 Generation of Photocurrent

The wavelength response is usefully measured over the wavelength range in which appreciable photocurrent can be generated. The absorption coefficient α in the silicon is an important factor determining the response as a function of wavelength. The intensity of illumination I, at a point in an absorbing medium, can be related to the intensity I_o at the surface by the following expression

$$I = I_o \exp - \alpha x \qquad (3.26)$$

where x is the distance from the surface. For efficient conversion of light into photocurrent, the depletion region in the Si must be equal to or greater than the photon absorption length

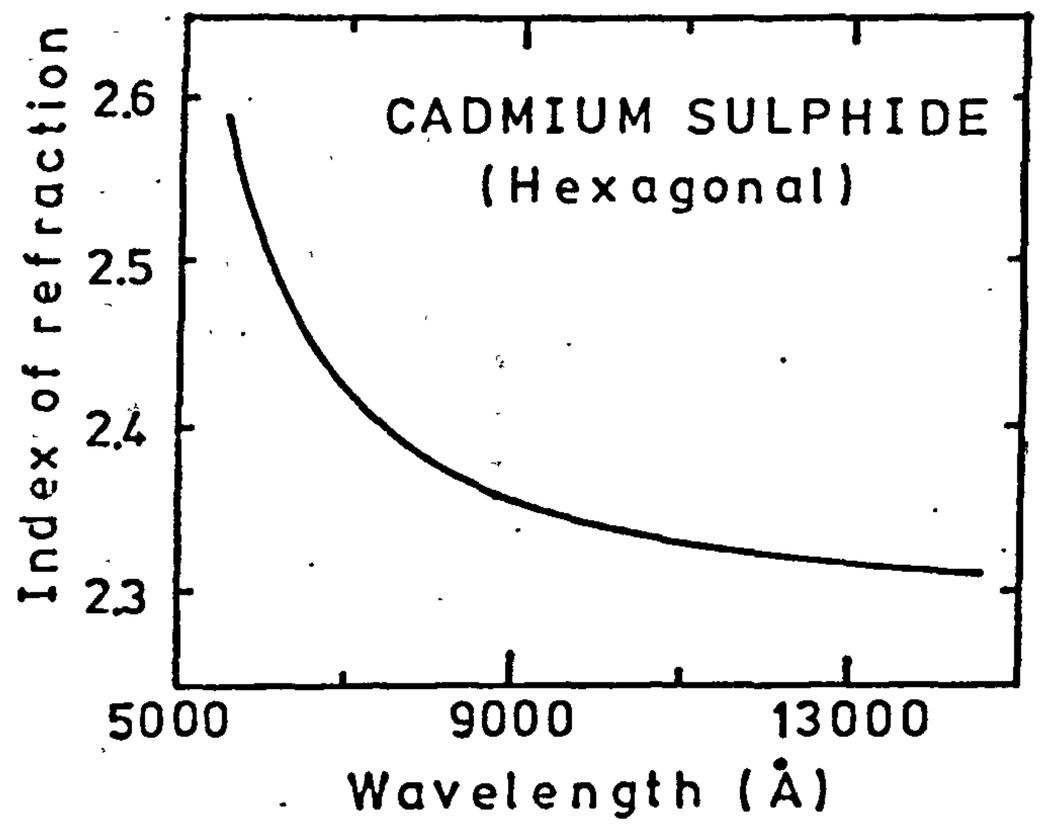


Fig 3.7 Real part of the refractive index of CdS versus wavelength [30]

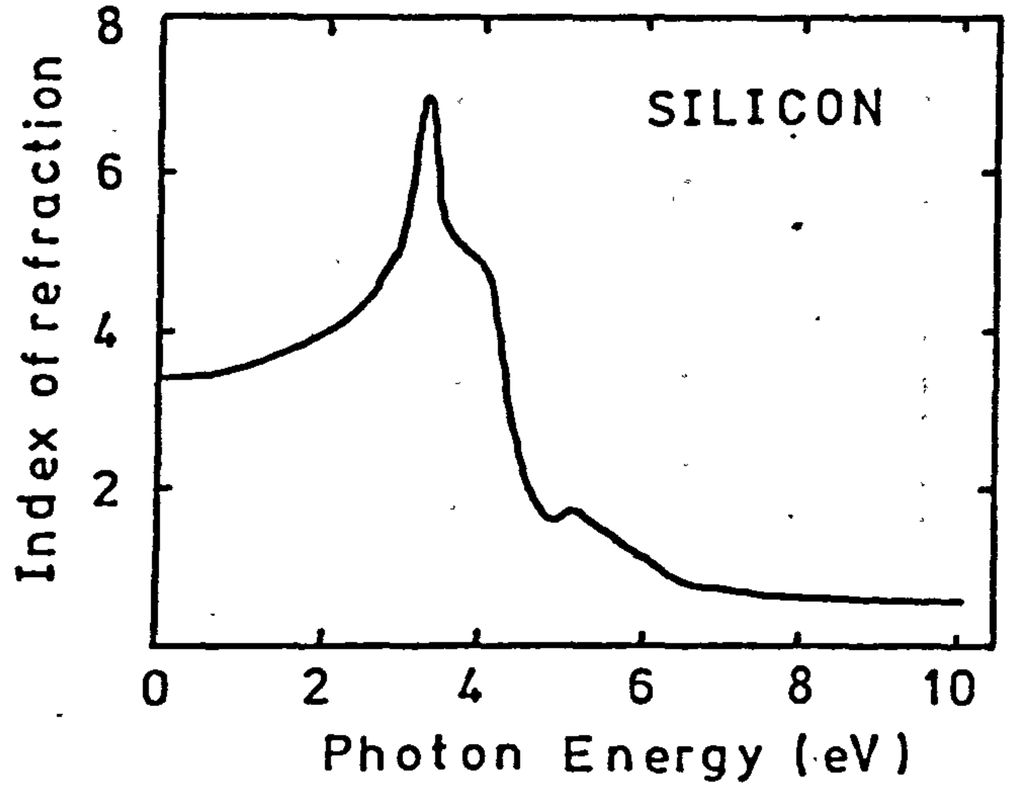


Fig 3.8 Real part of the refractive index of silicon versus photon energy [29]

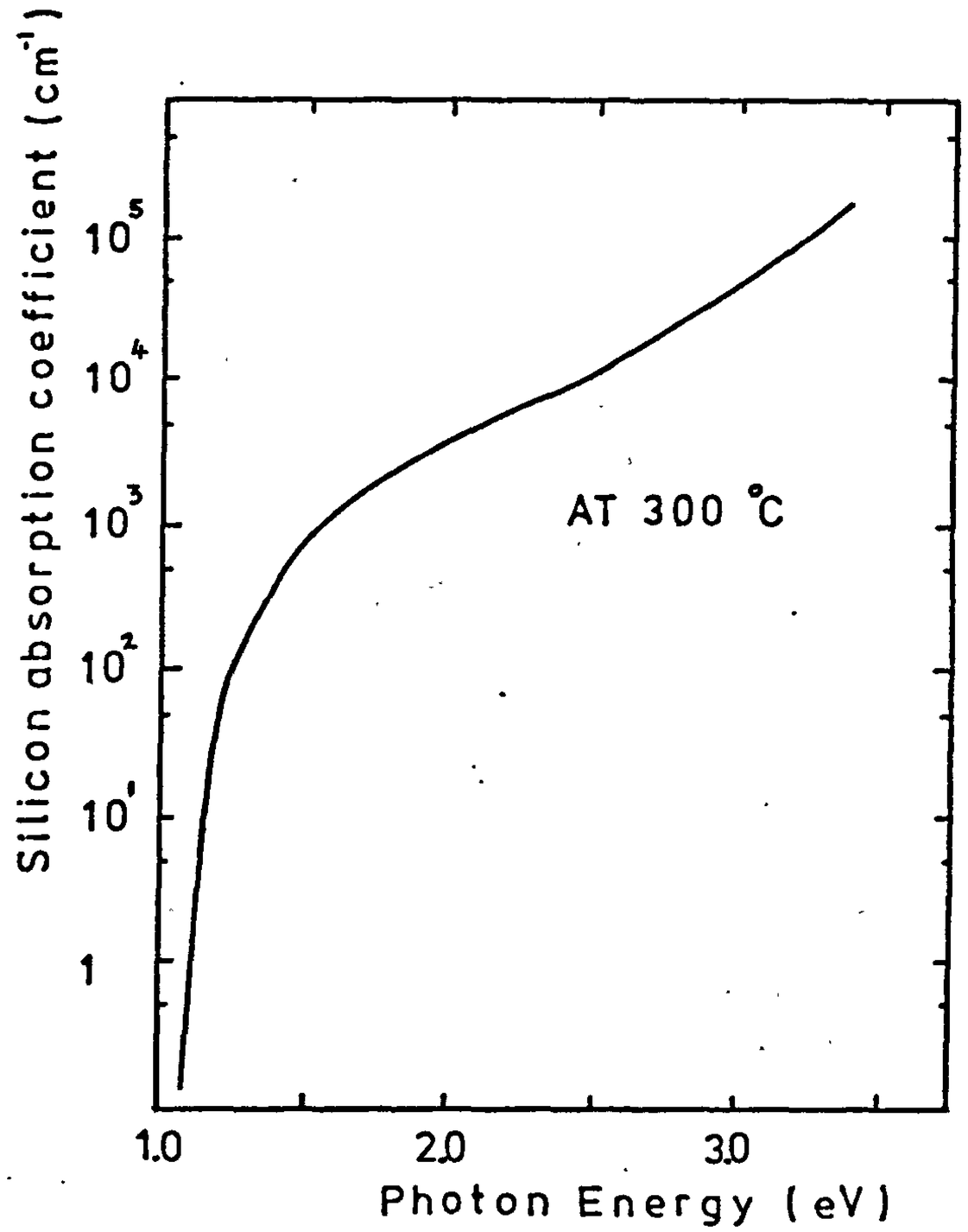


Fig 3.9 Silicon absorption coefficient versus photon energy [85]

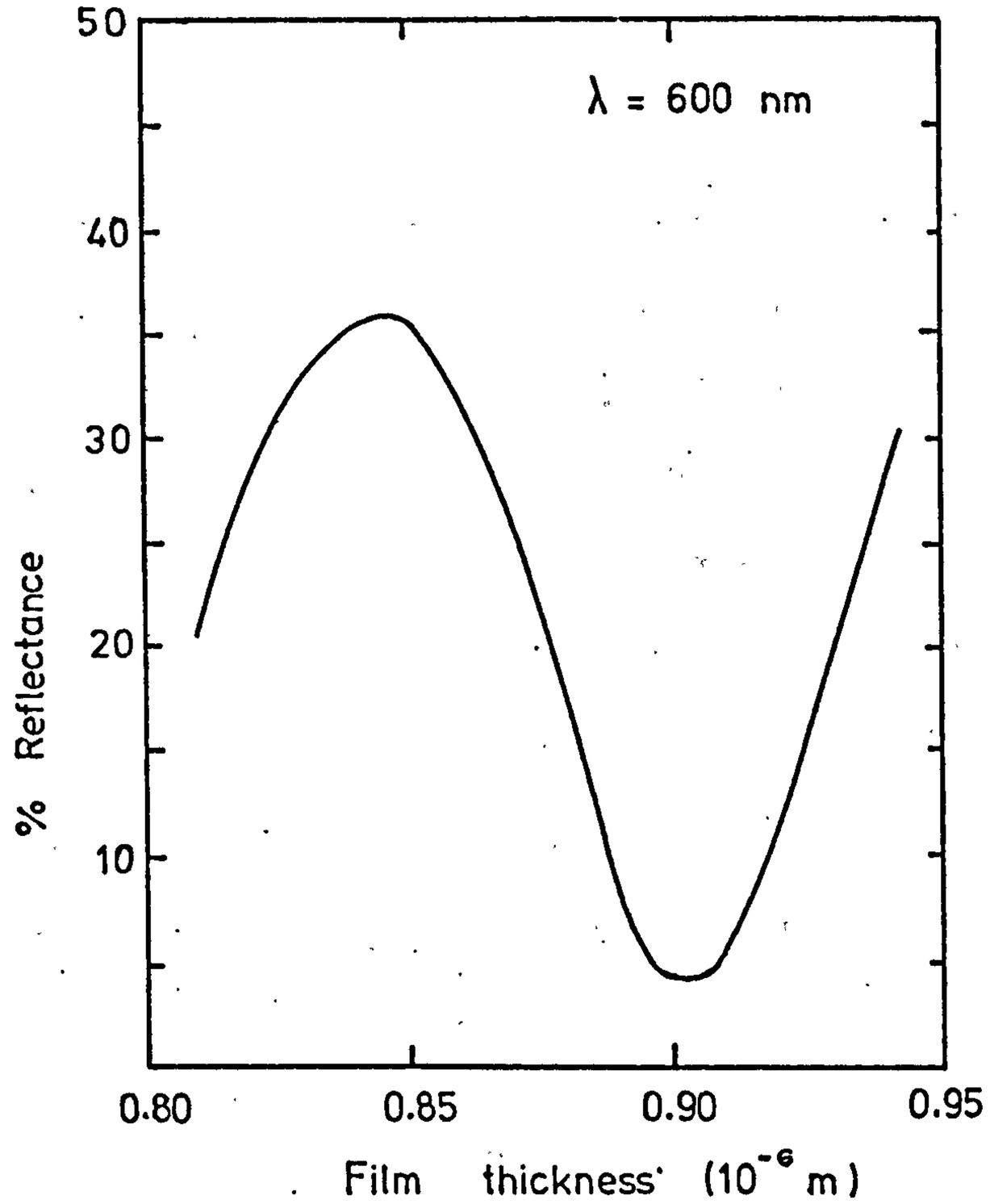


Fig. 3.10 Reflectance versus film thickness.

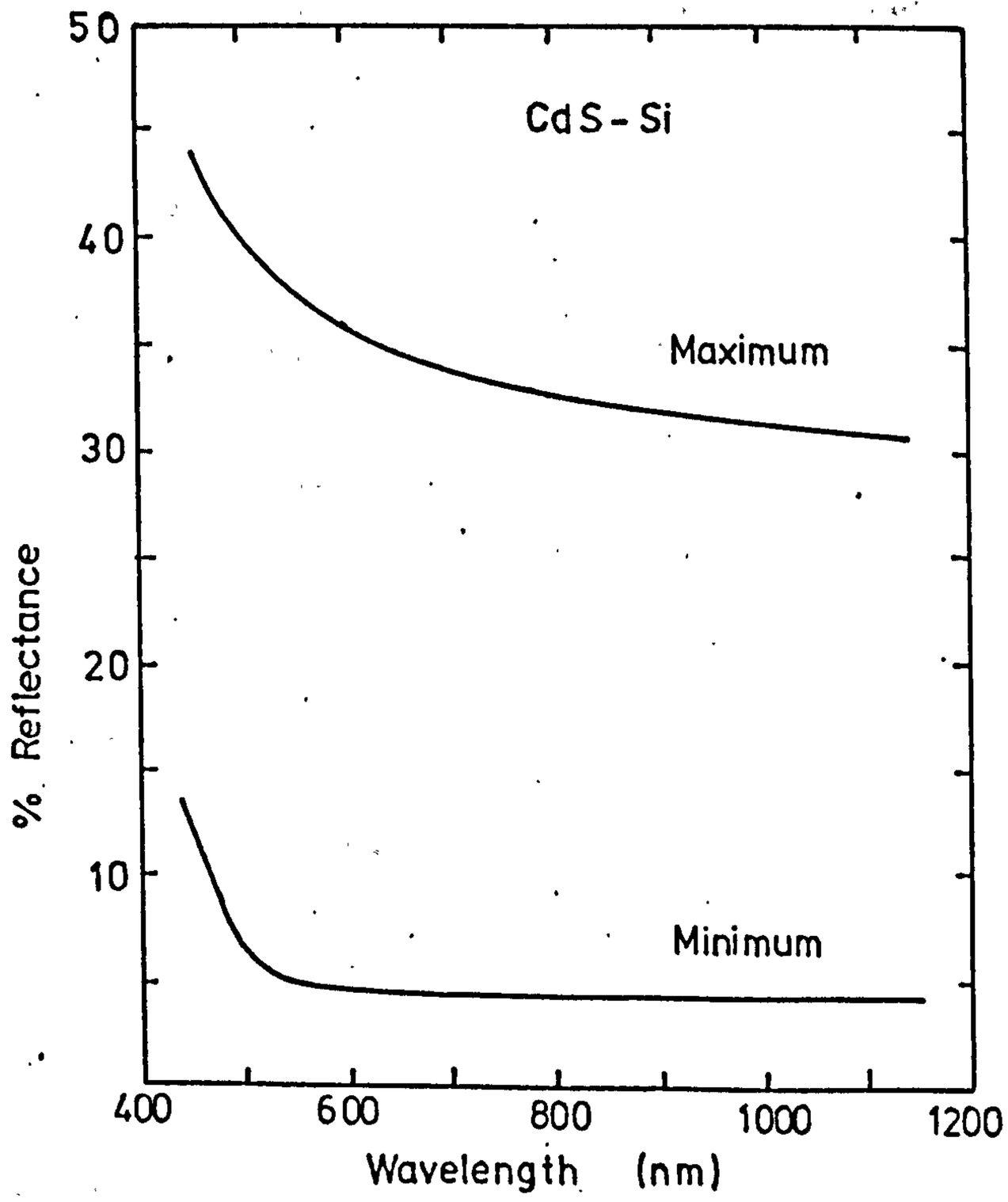


Fig. 3.11 Reflectance (maximum and minimum) versus wavelength for CdS-Si photodetector.

i.e. $x_d \geq 1/\alpha$

The depletion region should not be too wide, however, or transit time effects will limit the frequency response. On the other hand, the depletion region must also not be too thin, or excessive capacitance C will result in a large RC time constant, (where R is the series resistance of the device). At a wavelength of 600 nm, α for CdS is $\approx$ 3 cm^{-1},[86] while in silicon it is $\approx$ 5×10^3 cm^{-1}[85]. This indicates that there is only a small amount of light absorption in the CdS film.

Under steady-state conditions the total current density through the reverse biased heterojunction neglecting recombination is given by:

$$J_{TOT} = J_{DR} + J_{DIFF} \qquad (3.27)$$

J_{DR} is the drift current due to carriers generated inside the depletion region. J_{DIFF} is the diffusion current density due to carriers generated outside the depletion layer in the bulk of the Si and diffusing into the reverse-biased junction. The hole-electron generation rate $G(x)$ is given by

$$G(x) = N_o \alpha \exp(-\alpha x) \qquad (3.28)$$

N_o is the total incident photon flux and is given by

$$N_o = \frac{P}{A.E_p} \qquad (3.29)$$

where P is the incident light power, A is the area, and E_p is the photon energy

$$J_{DR} = -q\int_o^w G(x)dx = qN_o(1-\exp-\alpha w) \qquad (3.30)$$

where w is the depletion width.

For $x > w$, the minority carrier flow (electrons) in the Si is determined by the one dimensional diffusion equation

$$D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{po}}{n} + G(x) = 0 \qquad (3.31)$$

It can be shown that for this case[87a] the diffusion current, J_{DIFF}, is given by:

$$J_{DIFF} = qN_o \left[1 - \frac{\exp -\alpha w}{(1+\alpha L_n)} \right] \exp^{-\alpha w} + qn_{po} \frac{D_n}{L_n} \qquad (3.32)$$

Hence combining the two expressions for J_{DIFF} and J_{DR} one obtains the equation for the total photocurrent.

$$J_{TOT} = qN_o \left[1 - \frac{\exp -\alpha w}{(1 + \alpha L_n)} \right] + qn_{po} \frac{D_n}{L_n} \qquad (3.33)$$

Under normal operating conditions the term involving n_{po} is much smaller than the expression in the square brackets. This means that the photocurrent will be proportional to the photon flux. For example assuming that N_o is 3×10^{16} photons/cm^2-sec (P = 100 μW at 600 nm and A = 10^{-2}cm^2) and that n_{po} is 4×10^6 cm^{-3}. ($N_A = 6 \times 10^{13}$ cm^{-3}, $D_n = 40$ cm^2/sec and $L_p = 6 \times 10^{-4}$ cm) then the first expression in equation 3.33 has the value 5×10^{-3} A/cm^2 and the second expression has the value 3×10^{-8} A/cm^2. It is clear also that to maximise the photocurrent it is desirable that $\alpha w >> 1$ and $\alpha L_n >> 1$. As mentioned earlier, the absorption coefficient for Si at 600 nm is approximately 5×10^3 cm^{-1}. This suggests that a depletion width of approximately 10 microns is sufficient to satisfy the conditions mentioned above. If the equilibrium depletion width is not deep enough, the application of a large enough reverse bias will, in most cases, remedy the situation. High sensitivity for moderately low bias can be achieved for nCdS-pSi photodiodes with positive barrier potentials. However, photodiodes with highly doped Si substrates which have a reverse barrier potential will exhibit low sensitivity for two reasons. Firstly the depletion region is narrow and secondly the optically generated electrons must overcome the reverse barrier. In the diodes with a positive barrier

no such barrier exists to the electrons and the carriers are readily swept through the junction by the field into the p region.

The photoconduction characteristics of the positive barrier junctions can be used to determine the barrier potentials experimentally.

The I-V characteristics of the photodiode under illumination are given by

$$I = I_S \left(e^{qV/KT} - 1\right) - I_L \qquad (3.34)$$

where I is the current flowing in the external load, I_S is the saturation current, and I_L is the current generated by the incident radiation. Under short circuit conditions, V = 0 and $I = I_L = I_{SC}$. Under open circuit conditions I = 0 and

$$V = V_{oc} = \frac{KT}{q} \ln \left(\frac{I_L}{I_S} + 1\right) \qquad (3.35)$$

The saturation current I_S and hence J_S can be found from the measured values of short circuit current and open circuit voltage. The barrier potential ϕ can then be calculated from the equation

$$J_S = AT^2 \exp - \frac{q\phi}{KT} \; ; \; \phi = V_T + V_n \qquad (3.36)$$

3.7 Recombination Processes

Whenever the thermal-equilibrium condition of a physical system is disturbed i.e. $pn \neq n_i^2$, there are processes whereby the system can be restored to equilibrium i.e. to $pn = n_i^2$. The basic recombination processes are shown in Figure 3.12. Figure 3.12(a) illustrates the band-to-band recombination process where an electron-hole pair recombines. This transition of the electron from the conduction band to the valence band is possible by the emission of a photon (radiative process) or by transfer of the energy to another free electron or hole (Auger process).

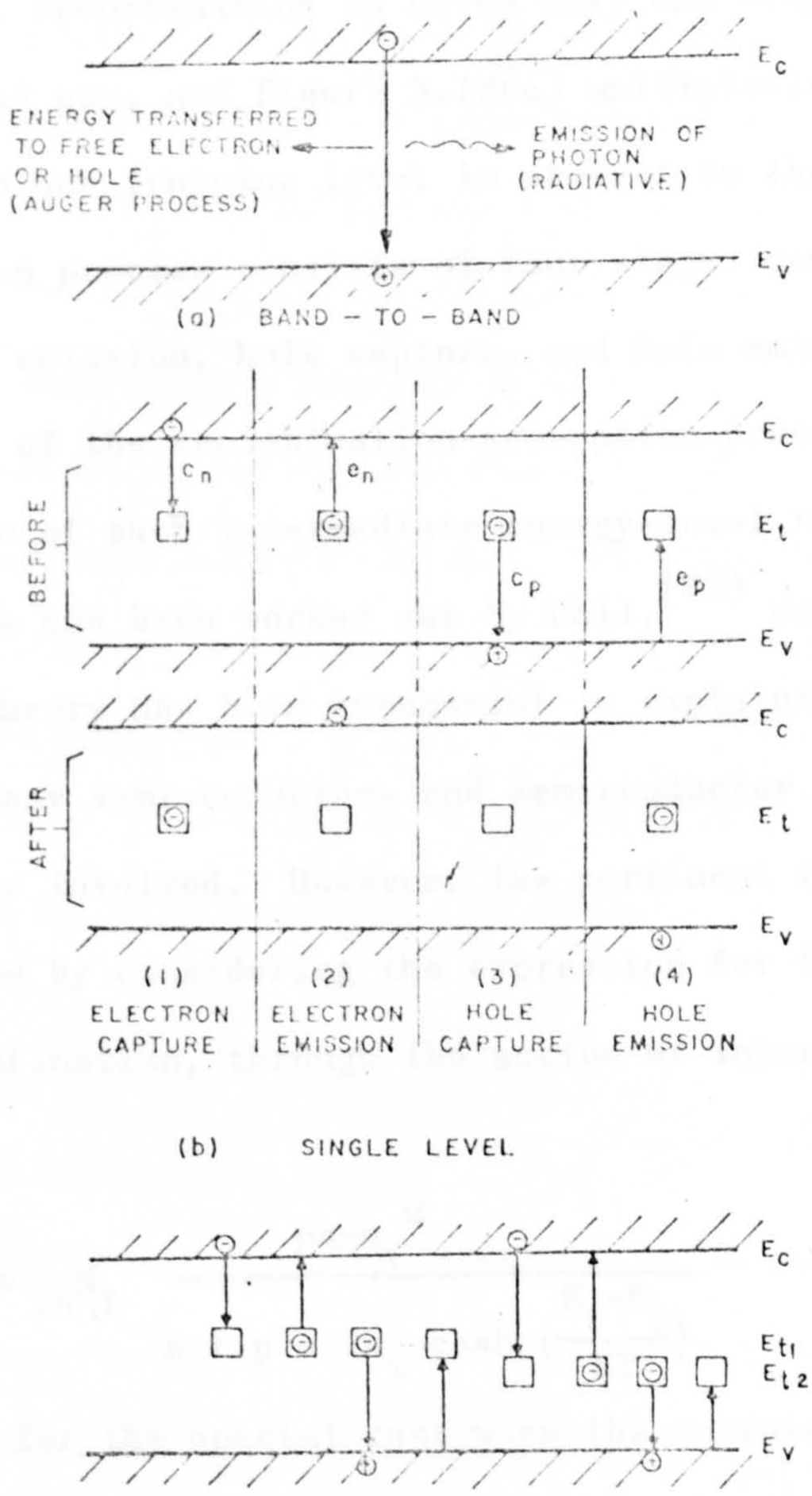


Fig 3.12 Recombination Processes (87C)
AND THERMAL EMISSION}

(a) Band-to-Band Recombination (Radiative or Auger Process)
(b) Single-Level Recombination
(c) Multiple-Level Recombination

The latter process is the inverse process of impact ionisation, and the former is the inverse process to direct optical transitions. Figure 3.12(b) shows single-level recombination in which only one trapping energy level is present in the band gap, and Figure 3.12(c) multiple-level recombination in which more than one trapping level is present in the band gap. The single-level recombination process consists of four steps: namely, electron capture, electron emission, hole capture, and hole emission.

The theory of the recombination-generation process taking place through the action of such intermediate energy-level recombination-generation centres has been worked out by Hall,[88] and by Shockley and Read.[89] This theory has been successful in explaining a wide variety of phenomena in many semiconductors and semiconductor devices although the analysis is fairly involved. However, the pertinent features of the process may be interpreted by considering the expression for the steady-state, net rate of recombination, through the action of intermediate centres, U ($cm^{-3}sec^{-1}$),

$$U = \sigma v_{th} N_T \frac{pn - n_i^2}{n + p + 2n_i \cosh\left(\frac{E_t - E_i}{KT}\right)} \qquad (3.36)$$

This equation is for the special case when the capture cross sections for electrons and for holes are equal, i.e. $\sigma_p = \sigma_n = \sigma$. The other parameters in the equation are: v_{th} is the carrier thermal velocity, N_T is the concentration of centres, E_i is the energy of the intrinsic Fermi level and E_t is the energy of the recombination centre.

The "driving force" for recombination is the term $pn - n_i^2$, which is in fact the deviation from the equilibrium condition. The n and p terms in the denominator show that the recombination rate decreases with increasing hole and electron concentration. The third term in the denominator increases as E_t moves away from the middle of the energy gap E_i and approaches either the conduction-band or the valence-band edge.

In such a case one of the emission processes becomes increasingly probable and this reduces the effectiveness of the recombination centre. This is because after an electron is captured by the centre, a hole must be captured by it next, to complete the recombination process. If, however, the energy level of the centre is very near the conduction-band edge, it will be more likely to re-emit the captured electron into the conduction band, thereby preventing the completion of the re-combination process. A similar argument holds for centres near the valence-band edge.

Thus a recombination centre is most effective if the two emission probabilities are about the same, i.e. when its energy level is near the middle of the energy gap.

The net rate of recombination in the bulk of an n-type semiconductor can be described by the linearised expression

$$U = (1/\tau_p)(p_n - p_{no}) \qquad (3.37)$$

where τ_p is the lifetime of holes.

It is possible to show using the previous expression for the recombination rate that the lifetime of holes in low-level injection in an n-type semiconductor is

$$\tau_p = 1/(\sigma_p v_{th} N_t) \qquad (3.38)$$

It is clear that the lifetime does not depend on the electron concentration, and that as one might expect the greater the density of recombination centres the shorter will be the recombination time.

Some physical examples of recombination-generation centres, both in the bulk and at the surface are, impurities, radiation damage and surface states.

When introduced into a Si sample, column III and column V impurities lead to energy levels within the forbidden gap. Because

these elements are relatively similar to Si (a column IV element), the energy levels associated with them will be shallow, i.e. they will be close to the valence and conduction band edges. However, in contrast with column III and V elements, gold (a column I element) introduces an energy level near the middle of the forbidden gap of Si and therefore acts as an efficient recombination-generation centre. The same situation occurs for CdS[90], where various impurities cause donor levels at .03 eV below the conduction band and acceptor levels at 0.6 eV and 1 eV respectively above the valence band. In addition, a cadmium vacancy results in an acceptor level of 1 eV above the valence band, thus implying that non-stoichiometric films of CdS can have recombination centres caused by cadmium and sulphur vacancies.

It might be expected that the drastic irregularity associated with the surface of a crystal, where the semiconductor lattice is terminated, should also result in the introduction of a large density of levels into the forbidden gap. If some of these surface states should have energy levels near the middle of the forbidden gap, one would expect them to act as efficient surface recombination centres. Theoretical estimates of the density of surface states yield values of the same order as the density of surface atoms, $\approx 10^{15}$ cm^{-2}. Such densities have been observed on very clean semiconductor surfaces obtained by cleaving samples under high vacuum.[91]

3.7.1 Effect of Recombination on Measured Characteristics

As far as the I-V characteristics are concerned, the measured currents are higher for a given voltage than would be expected from theory which does not include the effect of recombination.

The total reverse current (for $P_{no} >> n_{po}$ and $|V| > 3KT/q$) can be approximately given by the sum of the diffusion components in the neutral

region and the generation current in the depletion region:

$$J_R = q\sqrt{\frac{D_p}{\tau_p}} \cdot \frac{n_i^2}{N_D} + q\frac{n_i w}{\tau_e} \qquad (3.39)$$

where w is the depletion layer width and τ_e is the effective lifetime. The first point to note is that the diffusion component is proportional to n_i^2 while the recombination component is proportional to n_i. For semiconductors with large values of n_i (such as G_e with $n_i = 2.4 \times 10^{13} cm^{-3}$) the diffusion component will dominate at room temperature and the reverse current will follow the Shockley equation; but if n_i is small (such as Si, $n_i = 1.6 \times 10^{10} cm^{-3}$ and CdS, $n_i \simeq 4 \times 10^{-2} cm^{-3}$), the generation current may dominate. Like the generation current in reverse bias, the recombination current in forward bias is also proportional to n_i. The experimental results, in general, can be represented by the following empirical form:[87b]

$$J = J_S \exp\left(\frac{qV}{nKT}\right) \qquad (3.40)$$

where the factor n = 2 when recombination current dominates, and n = 1 when the diffusion current dominates.

As far as the nCdS - pSi heterojunctions are concerned, the exponential law applies in forward bias but the n values are larger than 2 probably because a more complicated trapping process is involved, i.e. there is not just a single level trapping centre. A factor n is also included in the expressions governing the photocurrent versus voltage characteristics to allow for recombination. The effect of recombination is to reduce the maximum theoretical photocurrent due to carrier generation in the depletion region. This is a result of electron-hole pairs recombining, via recombination centres in a time less than the drift transit time through the depletion region. Thus if the recombination time $\tau_r << $ the drift transit time τ_D, significant reduction in the photocurrent I_L, will occur.

CHAPTER 4 SILICON PROCESSING

4.1 Introduction

In this work the diffusion of acceptor impurities into Si substrates and photolithographic techniques are used in the fabrication of the nCdS-pSi diodes. The former technique is used to make p^+ ohmic contacts to the Si substrate and the latter to produce isolated regions of exposed silicon over which the CdS film is grown. Such processes are extensively used in almost all semiconductor device work and are fully documented in standard texts.[92] Consequently there would be no justification for a detailed presentation of these techniques if they were only limited to the fabrication of ohmic contacts to the above device. However, an important aspect of this thesis is the structural analysis of the CdS film on an Si substrate using transmission electron diffraction. With this technique the combined thickness of film and substrate must be less than 2,000Å, to obtain an effective transmitted intensity of the diffracted electron beam. Selective etching is used, in addition to the techniques mentioned previously, for the fabrication of thinned silicon substrates, 1000Å thick. A detailed analysis of diffusion, oxidation, photolithography and selective etching processes is therefore justified.

4.2 Oxidation

Silicon dioxide (SiO_2) layers grown on silicon can be formed by various methods.[93,94,95] The method which is used here is that of thermal oxidation. The silicon wafers were placed in a furnace at a temperature of 1180°C. Either steam or oxygen (which can be dry or wet) is passed through the furnace tube to oxidise the silicon. Wet oxygen was used, in this work, to grow SiO_2 layers both for the heterojunction

diodes and for the thinned silicon. Wet oxidation describes the case where dry oxygen is first passed through a water bath prior to being introduced into the oxidation furnace. Since oxidation proceeds much more rapidly in water vapour, than in dry oxygen, the water content of the carrier gas is the most important variable for determining the oxide thickness for a given time and temperature. A 1 inch internal diameter quartz furnace tube with 'Q' type glass to glass fittings on the input was utilised. The water bath was maintained at 90°C, the O_2 flow rate was 0.6 l/min and the furnace temperature was 1180°C. A heating tape was wound round the part of the quartz furnace tube, which was exposed to the ambient, to prevent condensation of water at the entrance to the furnace. For the conditions described, the oxide thickness was 0.6 microns after a 2 hour oxidation process. This thickness is more than adequate to prevent boron diffusing through the SiO_2 under the conditions pertaining. Oxide thickness measurements were obtained by removing the oxide on one half of an oxidised wafer, using photolithographic techniques, and measuring the height of the step using an interference microscope.

It must be emphasised that the cleanliness of the wafer before, during, and after oxidation, is perhaps the most important requirement for obtaining high quality oxides. A polished silicon surface is a prerequisite. Without the smooth, clean surface, the structure of the oxide grown tends towards cristobalite,[96] which is denser than silica glass. Under these conditions the boundaries between the amorphous regions and the denser crystalline regions are porous to both surface contamination and impurities during diffusion. The silicon was mechanically lapped and polished, the final stage using a one micron diamond paste. After polishing, the silicon was washed in electronic grade trichloroethylene in an ultrasonic bath, to remove any residual wax used in the polishing stage. The silicon was then washed thoroughly in deionised water prior to oxidation.

Although the polishing does create some surface damage to the silicon, this effect is substantially reduced because of the oxidation stage and the subsequent cleaning at high temperature in the vacuum system.

4.3 Theoretical Aspects of Diffusion

Diffused layers of either conductivity type are normally formed in a two-step process. In the first step, impurities are introduced into the semiconductor to a depth of a few tenths of a micron. This process is called the predeposition step. Once the impurities have been introduced into the semiconductor, they are then diffused to the required depth to provide a suitable concentration distribution without any further impurities being added to the semiconductor. This second step is called the drive-in diffusion step. For the fabrication of both the nCdS-pSi heterojunction and the thinned silicon specimens, only the predeposition step is required.

The transport equation for the diffusion of impurities into silicon can be written as[89]:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} \qquad (4.1)$$

where C is the concentration of the diffusing species and D is the diffusion coefficient. Two assumptions were made in obtaining equation 4.1, (i) D is a constant, and (ii) there is no applied electric field. To solve this equation for a particular case it is necessary to know the initial and boundary conditions. During the predeposition stage, the surface concentration C_S of the diffusing species is kept constant. This results because the diffusion is carried out at the solid solubility limit of the diffusant in silicon at the given temperature. A graph showing the solid solubilities of various impurities in silicon[97] is shown in Figure 4.1.

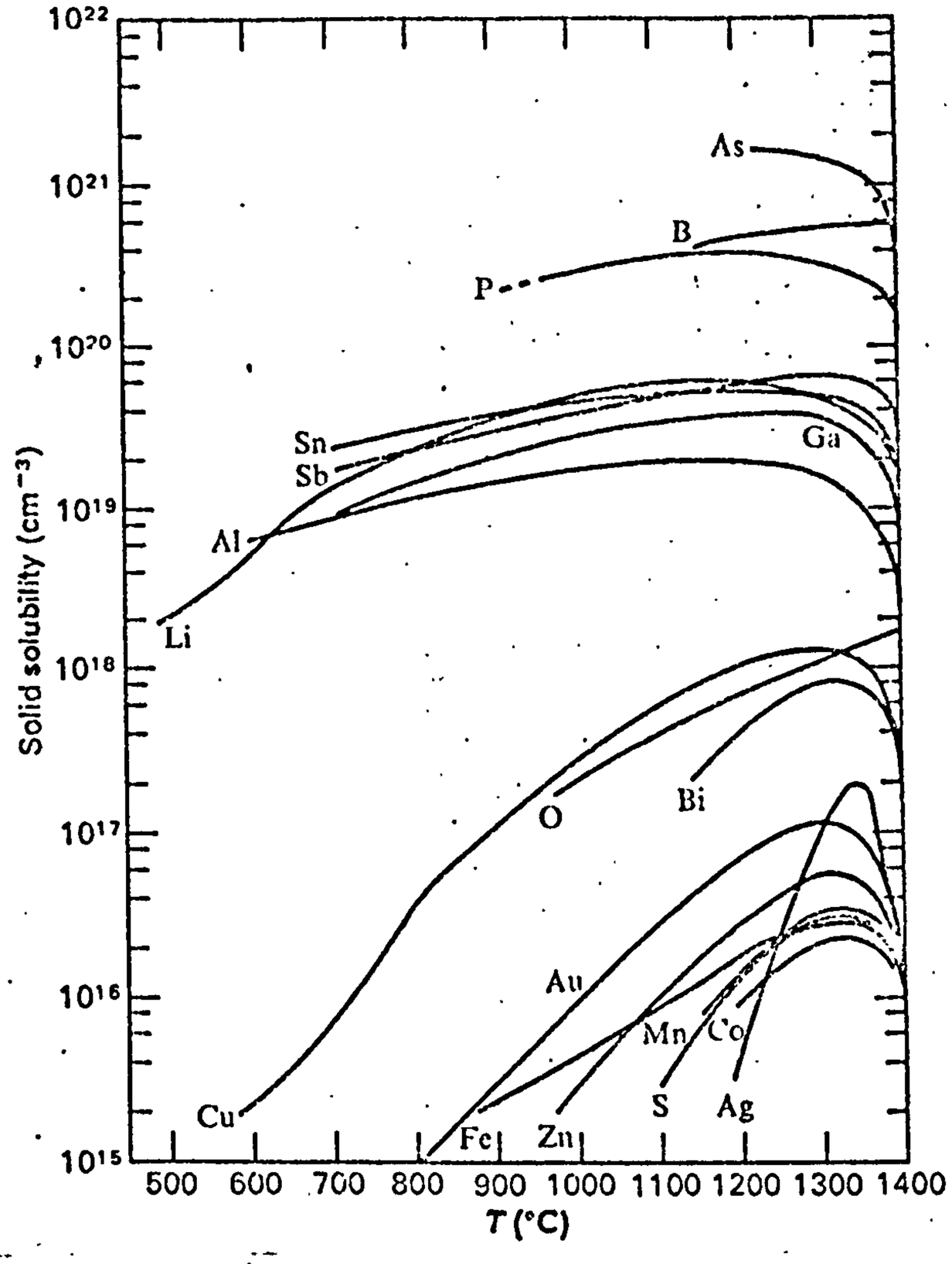


Fig 4.1 Solid Solubilities of Various Impurities in Silicon (97)

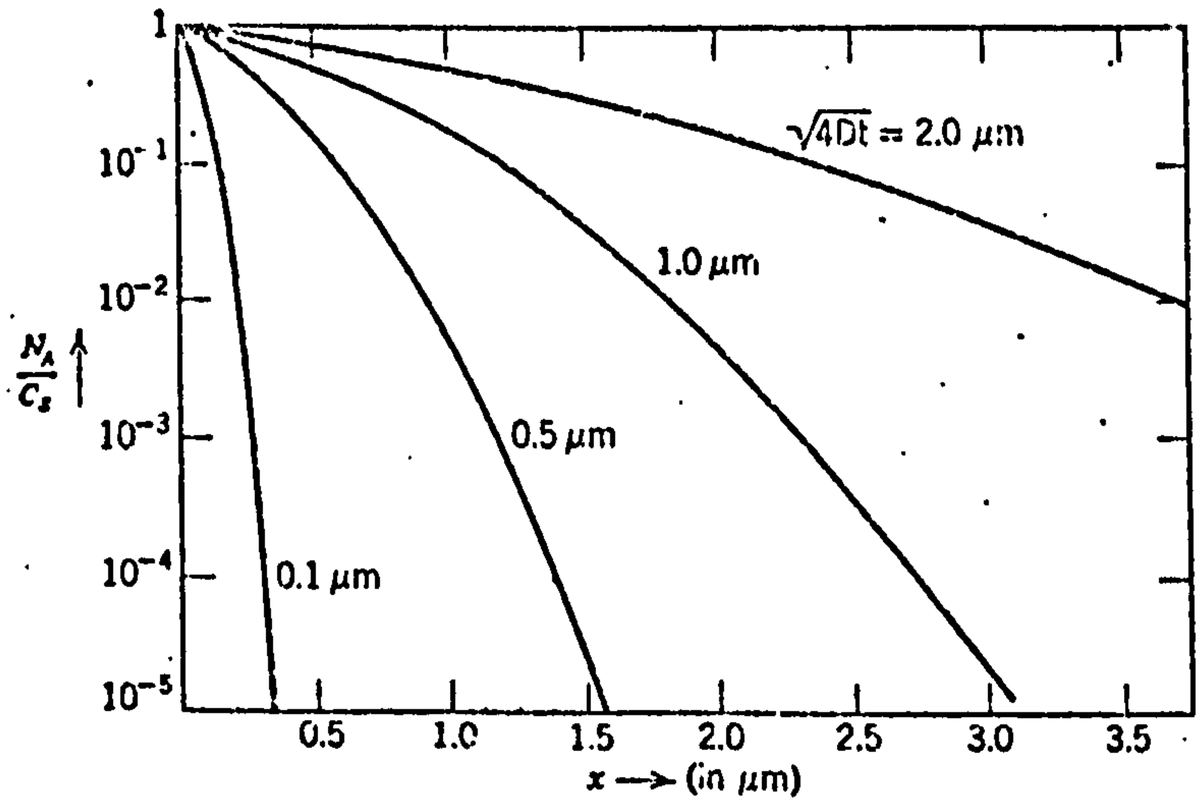


Fig 4.2 Normalised Impurity Concentration as a Function of Diffusion Depth Plotted for Four Different Values of $2\sqrt{Dt}$ (erfc profile) (80)

The solution of equation 4.1 for constant surface concentration C_S is given by

$$N_A(x,t) = C_S \text{ erfc } \left[\frac{x}{2\sqrt{Dt}} \right] \qquad (4.2)$$

where N_A is the net acceptor concentration as a function of diffusion depth x and diffusion time t. erfc denotes the complementary error function, defined by

$$\text{erfc } (x) = 1 - \frac{2}{\sqrt{\pi}} \int_0^x \exp(-y^2)\, dy \qquad (4.3)$$

This function has been evaluated and is available in tabular form.[99] Figure 4.2 shows the variation of the normalised impurity concentration as a function of diffusion depth for four different values of $2\sqrt{Dt}$. The only other parameter required is knowledge of the diffusion constant D as a function of temperature.[92] Figure 4.3 shows a graph of diffusion coefficient as a function of temperature for a number of different acceptor impurities.

In order to obtain thinned silicon specimens the conditions required are that the surface concentration C_S must be greater than 7×10^{19} cm^{-3} and that the distance from the surface to the region where the boron concentration is 7×10^{19} cm^{-3} must be approximately 0.1 microns.

At $1000^{\circ}C$ $D_B = 5 \times 10^{-3}$ $\mu m^2/hr$

$C_S = 2 \times 10^{20}$ cm^{-3}

From these parameters erfc $\left[\frac{x}{2\sqrt{Dt}} \right] = 0.35$.

The tabulated values of erfc give the value of $\left[x/2\sqrt{Dt} \right]$ as 0.662. Hence the required time, t, is 1 hour 8 minutes. The diffusion depth is not critical as far as ohmic contacts to the CdS-Si heterojunction is concerned.

A four point probe method was used to check that the junction depth

was close to the depth calculated from theory. As the silicon substrates for nCdS-pSi heterojunctions were already p-type, the four point probe was used to verify that the resistivity was low enough for an ohmic contact. Corrections to the four point probe measurements were made using methods suggested by Valdes[99].

4.3.1 Diffusion through an SiO_2 Layer

It is of considerable importance to determine the minimum oxide thickness required to prevent the formation of a junction in the silicon because of diffusion through the oxide.

The equation relating the junction depth in the silicon to the silicon dioxide thickness is given below.[93]

$$\frac{x_j}{\sqrt{t}} = \frac{1}{r}\frac{x_o}{\sqrt{t}} + 2\sqrt{D}\ \arg\left[\operatorname{erfc}\left(\frac{(m+r)C_B}{2mrC_o}\right)\right] \qquad (4.4)$$

where x_j is the junction depth in the silicon

x_o is the oxide thickness

C_B is the silicon bulk impurity concentration

C_o is the oxide surface concentration = C_S

m is the segregation coefficient of impurities at the Si/SiO_2 interface

r is defined as $\sqrt{D_1/D}$

D_1 is the diffusion coefficient of boron in SiO_2

By setting $x_j = 0$, the minimum oxide thickness x_o can be calculated. Worst case conditions are:

Diffusion temperature = $1000^{o}C$

Diffusion time t = 1 hr 10 mins

D_1 (100) = 8×10^{-5} $\mu m^2/hr$

m (101) = 0.016

C_B (2,000Ω-cm) = 6×10^{12} cm^{-3}

Using these values, the minimum oxide thickness x_o is 0.047 microns. Hence the oxide thickness of 0.6 microns, used throughout, was certainly more than adequate for masking purposes.

4.3.2 Diffusion, Experimental

Diffusion processes can be divided into two categories, closed tube and open tube; it is the latter method which is used here. In the open-tube system, a continuous flow of gas is maintained across the silicon wafers during the diffusion. The source of the diffusant is usually deposited on the surface of the slice in a previous step[102] or carried in by the gas stream.[14]

In the present work, boron nitride (BN),[14] was used as a source of boron for the diffused p-type layers. BN is supplied commercially in the form of an opaque white wafer, slightly larger in diameter than the silicon wafers which are to be doped. The BN wafer source used throughout the diffusions was Union Carbide "Ucar" grade H.B.G. boron nitride. It has significant advantages over other sources of boron; it gives excellent uniformity of doping across the silicon slice, and flow pattern problems are eliminated since the BN slice is placed in close proximity to the silicon. In addition, only one inert carrier gas is required, and BN is an inert easily handled material available in high purity. Because the quantity of available boric oxide is limited, the common problem of sticky furnace tubes is eliminated.

Before the BN slice could be used it had first to be degreased, etched

and then oxidised. The expected oxidation and deposition reactions are as follows:[104]

Oxidation : $2BN + 3O_2 \longrightarrow 2B_2O_3 + 2N_2$ 4.5(a)

$B_2O_3 + H_2O \longrightarrow 2HBO_2$ 4.5(b)

Deposition : $2HBO_2 + 2Si \longrightarrow 2SiO_2 + 2B + H_2$ 4.6

Elevated temperature storage of BN wafers oxidation is necessary because of the great affinity of boric oxide for water. Rupprecht,[104] found that no reasonable degree of tolerance, as far as sheet resistance was concerned, could be obtained with BN wafers stored at room temperature and room humidity.

Since all diffusions were carried out at 1000°C, N_2 was used as the carrier gas. At significantly higher temperatures it is necessary to use argon to avoid the formation of silicon nitride layers.

The furnace used for the diffusions was the same type as used for the oxidations. The N_2 gas was introduced directly to the furnace and the output of the furnace was connected via a water "bubbler" to the ambient.

The "bubbler" made certain that there was back pressure and that gas was flowing out through the furnace, not through a crack in the wall of the quartz tube.

The BN and silicon wafers were mounted side by side on a quartz boat, 4 mm apart, perpendicular to the direction of the gas flow. Every day, before use, the BN was oxidised and stabilised to ensure that it was in an active state. After stabilisation, the BN and silicon wafers were placed in the centre of the furnace at 1000°C with an N_2 gas flow rate of 0.2 l/min, for the time needed to give the required diffusion profile.

The only significant problem encountered was that sometimes the diffused silicon was stained. This stain was found to be insoluble in buffered H.F., (a solution of 140 ml 40% H.F. and 389 gms NH_4F made up

to 1 litre with distilled water), which etches both SiO_2 and B_2O_3. This staining problem was caused by water absorption, and the remedy suggested by the manufacturer was to introduce 1-2% dry O_2 during predeposition. It was possible to remove this stain by the following process.[105] This consisted of boiling the wafer for 10 minutes in concentrated HNO_3, washing for 10 minutes in deionised water, followed by a 30 second wash in buffered H.F.

An improved planar boron source has now been developed which does not require periodic reactivation procedures. This is because the source is a glass-ceramic material, in which the boron is already present in its oxidised, (B_2O_3), state.[106]

4.4 Photolithography

Photolithographic techniques were used both to define the junction area of the nCdS-pSi heterojunctions and to define the preferential etching regions of the specimens for the transmission electron microscope work. After spinning Shipley AZ 1350H photoresist, on an SiO_2 coated silicon wafer, the photoresist was exposed, developed and post-baked. The oxide was then etched in buffered H.F. and the remaining photoresist removed by placing the silicon wafer in electronic grade acetone.

This technique was also utilised in the final stage of the fabrication of an nCdS-pSi heterojunction. The procedure used was called "lift off". When a wafer, with a photoresist pattern defined on top, was coated with metal and then placed in a bath of acetone, the metal "lifted off" those areas which were coated with photoresist and adhered elsewhere. The "lift-off" technique was essential, since most etchants which are used to define a metal pattern also etch the CdS films.

The main problem associated with photoresist was its poor adhesion to the wafer if the humidity was too high. This problem was more severe

on wafers that used SiO_2 to mask the Si during the diffusion. As a result of the diffusion, the SiO_2 was coated with B_2O_3 which absorbs moisture very readily, causing poor photoresist adhesion. This problem was circumvented by removing the B_2O_3 prior to coating the wafer with photoresist.

4.5 Preferential Etching of Si

Several ternary liquid mixtures, which etch silicon at different rates in the principal crystal directions have been described in the literature.[107-109] These mixtures consist of an oxidant, which oxidises silicon to hydrated silica, and a complexing agent to react with the silica and form a soluble complex ion and water. The latter appears to function as a catalyst, in providing excess $(OH)^-$ ions, for the oxidation step.

Ethylene diamine (E.D.),[107] hydrazine[108] and potassium hydroxide[109] have been employed as oxidants and pyrocatechol (P.C.) and iso-2-propyl alcohol (I.P.A.) as complexing agents.

The reasons for the choice of ethylene diamine and pyrocatechol as the etchant solution, rather than some of the others mentioned above, are as follows:

i) The hydrazine - H_2O - I.P.A. solution has no major advantage compared with the other methods, except that vacuum deposited aluminium films may be used as a mask to define a pattern.

ii) The potassium hydroxide - H_2O - I.P.A. solution does not permit the use of aluminium as a masking medium. However, Price[110] found that the etch rate is a function of the boron concentration in p-type layers. The etch rate in the (100) direction is 60 μm/hr until the boron concentration reaches 10^{18} atoms/cm^3 after which it drops to a limiting value of about 5 μm/hr at 10^{20} atoms/cm^3. Donor impurities such as As, P and Sb used to produce n-type layers have no effect on the etch rate.

iii) The most important feature of the E.D. - H_2O - P.C. solution is that the etch rate in the (100) direction is a function of the boron concentration and etching stops completely when the boron concentration reaches 7×10^{19} atoms/cm^3. This provides a convenient method of producing thinned silicon samples, suitable for transmission electron microscopy analysis, simply by ensuring that the boron concentration is higher than 7×10^{19} atoms/cm^3 in the region just below the surface. This is possible using conventional diffusion techniques, where the impurity concentration, as a function of depth in the silicon wafer, is known.

In common with the other two etchants mentioned, thermally grown silicon dioxide layers form an effective barrier against the etchant, the etch rate being approximately 200Å/hr, while that of the silicon is about two orders of magnitude higher. The etch rates on (100), (110), and (111) oriented silicon are approximately 50:30:3 μm/hr respectively.

The overall chemical reaction as proposed by Finne,[107] is as follows:

$$\underset{\text{(E.D.)}}{2\,NH_2\,(CH_2)_2\,NH_2} + Si + \underset{\text{(P.C.)}}{3\,C_6H_4\,(OH_2)} \longrightarrow$$

$$2\,NH_2\,(CH_2)_2\,NH_3 + \left[Si\,(C_6H_4O_2)_3\right]^{=} + 2\,H_2 \qquad (4.7)$$

Although water does not appear in the overall reaction, it is a product of one of the intermediate states. The addition of water to the solution is essential, since in the absence of water no oxidation can take place.

Figure 4.4 shows the etch rate of silicon as a function of resistivity for the (100), (110) and (111) orientations.

Two years later, Greenwood[111] found that when a sample was etched containing a p-n junction, the etching of the p-type part of the sample appeared to be completely inhibited, until the n-type part of the sample was etched away. However, Bohg[112] found no preferential etching of

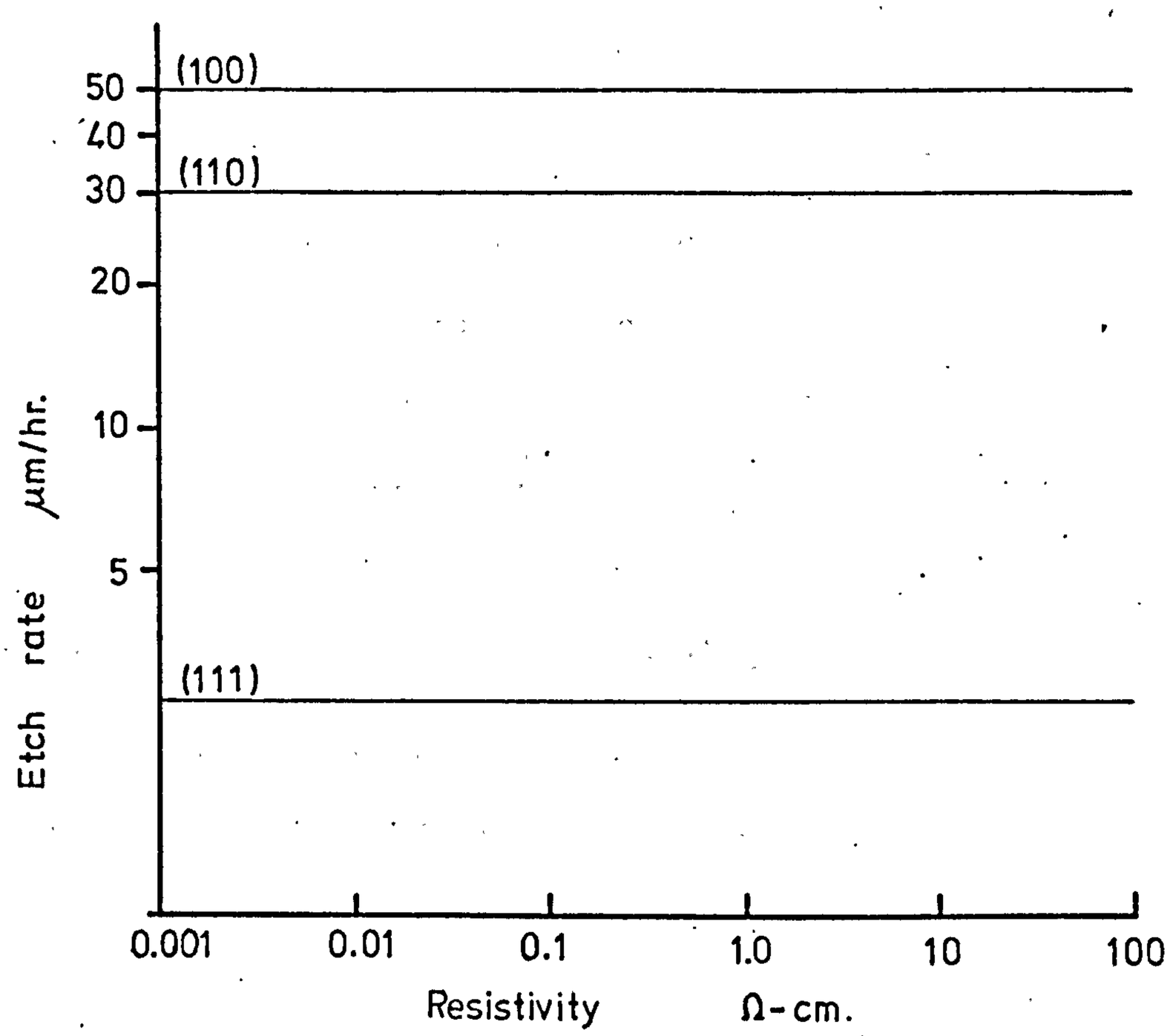


Fig. 4.4 Etch rate of silicon as a function of resistivity (107)

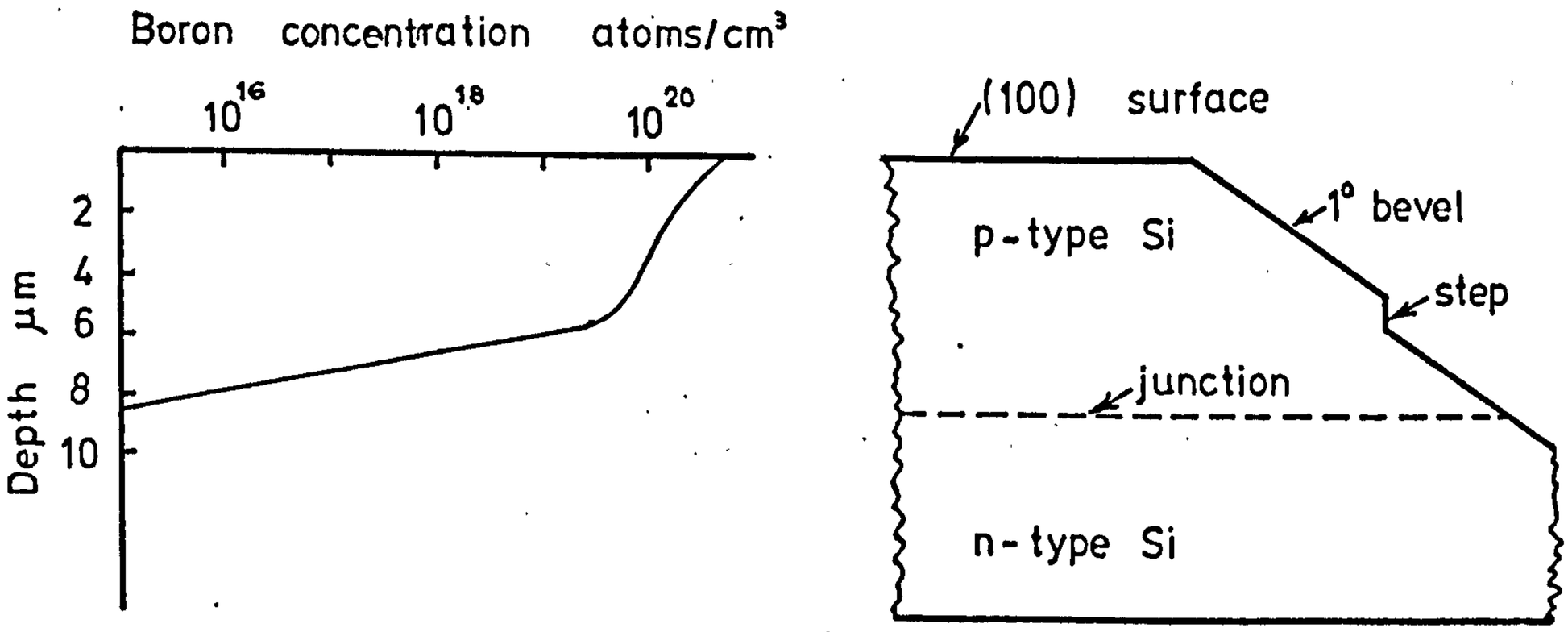


Fig. 4.5 Cross section of etched sample with corresponding boron concentration profile (112)

p-n junctions, only an abrupt change in the etch rate with concentration for boron doped silicon. Experimental evidence[112] was obtained by etching a silicon sample with a 1^{o} bevel of a (100) oriented surface, the background doping being 10^{17} cm^{-3} of As and the surface concentration being 5×10^{20} cm^{-3} of boron. Figure 4.5 shows a diagram of his results.

4.6 Preparation and Fabrication of T.E.M. Samples

Other methods have been used to prepare thin silicon and germanium samples for transmission electron microscopy analysis.[113,114] These methods use non-preferential etches which are generally more difficult to control but do permit the fabrication of samples of orientations other than (100).

The silicon used for the preparation of the thinned specimens was n-type 3-4 Ω-cm, (100) orientation oval shaped, of dimensions 30 mm by 15 mm and approximately 0.3 mm thick. The silicon was mechanically polished on both sides, the final stage utilising a one micron size diamond polishing compound. The silicon was cleaned in trichloroethylene prior to the thermal growth of a 0.6 micron SiO_2 film on both sides. Using conventional photo-lithographic techniques, the SiO_2 was removed on one side using buffered H.F. On removal of the photoresist, the silicon was then doped using a BN source at $1000^{o}C$ for 1 hr 8 mins. At this temperature, the surface concentration of boron, C_S, is approximately 2×10^{20} cm^{-3}, the boron concentration falling to 7×10^{19} cm^{-3} at a distance of 1000Å from the surface. When the doped silicon was removed from the diffusion furnace the B_2O_3 glass film had first to be removed using buffered H.F., while at the same time, protecting the SiO_2 on the non-doped side. In some cases, when an SiB phase was also present, a two stage etching process was required. The remaining SiO_2 on the undoped side was then used to define the areas to be removed by the preferential etch using photolithographic techniques.

One major advantage of choosing (100) oriented silicon was that this was the only one of the major planes which the (110), (111), (100) and (211) planes intercept with rectangular symmetry. For this reason it was necessary to align the sides of the mask along the (110) direction in the wafer.

On removal of the photoresist the silicon was then ready to be placed in the etching apparatus, which consisted of a glass refluxing system, in order to prevent composition changes by loss of volatile material. A stream of N_2 was bubbled through the etching solution, at $110^{o}C$, to prevent air oxidation of the amine and complexing agent, and to provide agitation of the solution. Reagent grade materials were used throughout. The silicon was placed in a pyrex holder which was attached to a length of pyrex rod connected to a 'Q' type glass to glass fitting. The holder assembly was then inserted through a matching port in the refluxing system and the etching commenced. The etching time was approximately 3 hours but depended on the actual silicon thickness and on the degree of agitation provided by the N_2 bubbler.

On removal from its holder, the entire silicon wafer was carefully washed in methyl alcohol to remove any remaining etching solution. Individual samples were then obtained by pressing out the thick walled areas of silicon using fine tweezers. The thinned specimens were then stored, until required, in a closed container of electronic grade methyl alcohol. A schematic representation of an individual sample is shown before and after etching in Figure 4.6.

The boundary of the "window" in the silicon was almost invisible when observed from the smooth face. This was because the diffused boron goes into the silicon substitutionally. Since this layer has a lattice constant, which was smaller than that of the bulk silicon[115], the window was in a state of tension.

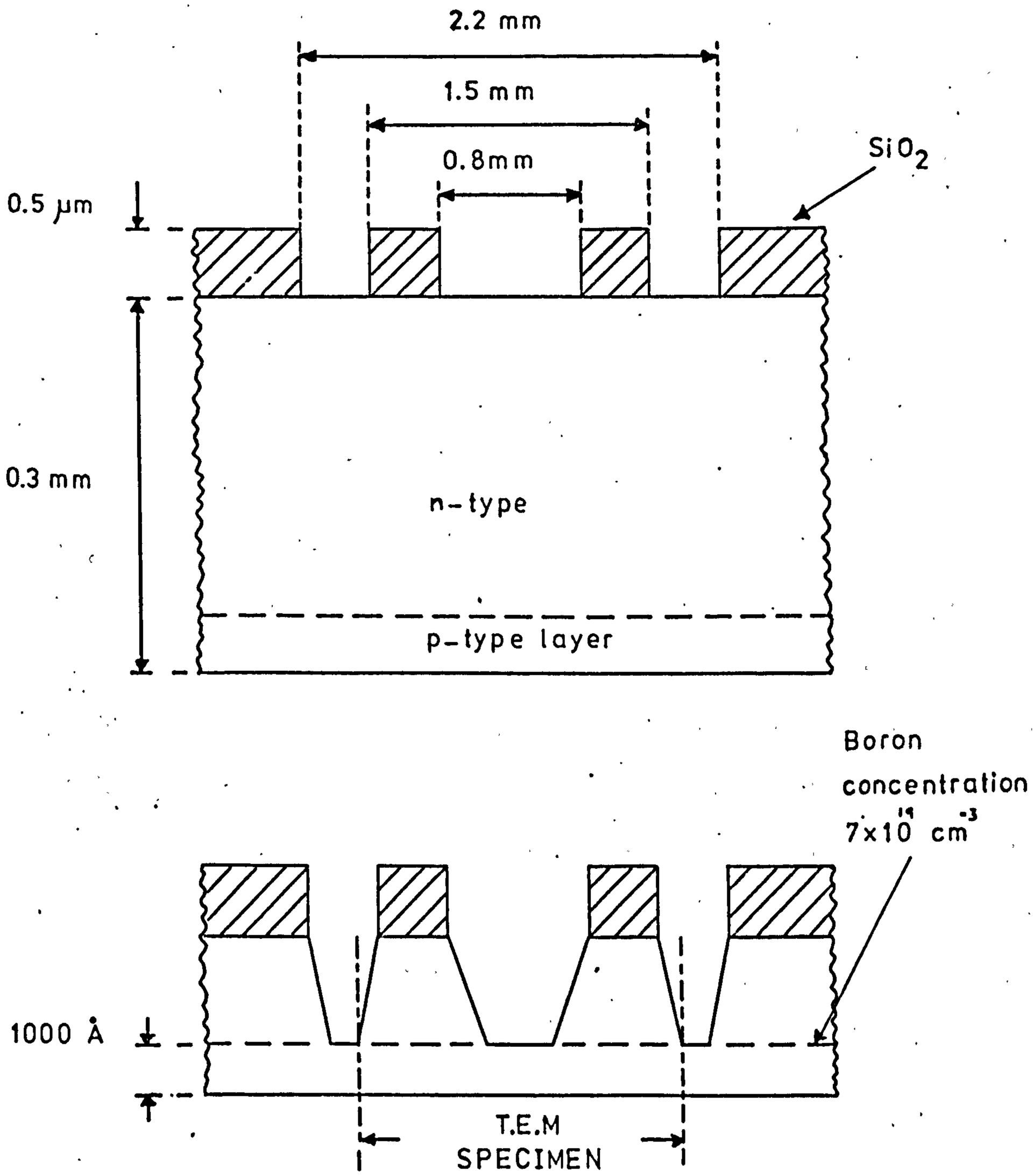


Fig 4.6 Cross-section of silicon before and after etching (not to scale)

The thinned specimens were placed in recessed holes in a piece of silicon which was placed in the clean high vacuum (C.H.V.) system in the same position as a normal sized sample. It was found necessary to cover the holder with a thin piece of silicon to prevent the thin samples moving. The samples were electron-beam cleaned at 1000^{o}C and once the silicon was at the correct temperature, the CdS evaporation was carried out. For temperatures below 200^{o}C at 5 mA emission current, the evaporation time was 10 seconds, while at higher temperatures it was considerably more. On removal from the C.H.V. system, the silicon was placed in the copper holder of the transmission electron microscope. If the sides of the specimen were etched for too long, then it was necessary to support them between two copper grids.

Figure 4.7 shows a photograph of a (100) oriented silicon sample which has been etched in buffered H.F. to remove the SiO_2. The 'white' regions are exposed silicon, which are etched when the wafer is placed in the E.D-H_2O-P.C. solution. Figure 4.8 shows a photograph of an etched silicon sample. The silicon has an orange peel effect, due to non uniform etching, when viewed from inside. The reverse side, on which the CdS film is grown, still retains the original mirror finish.

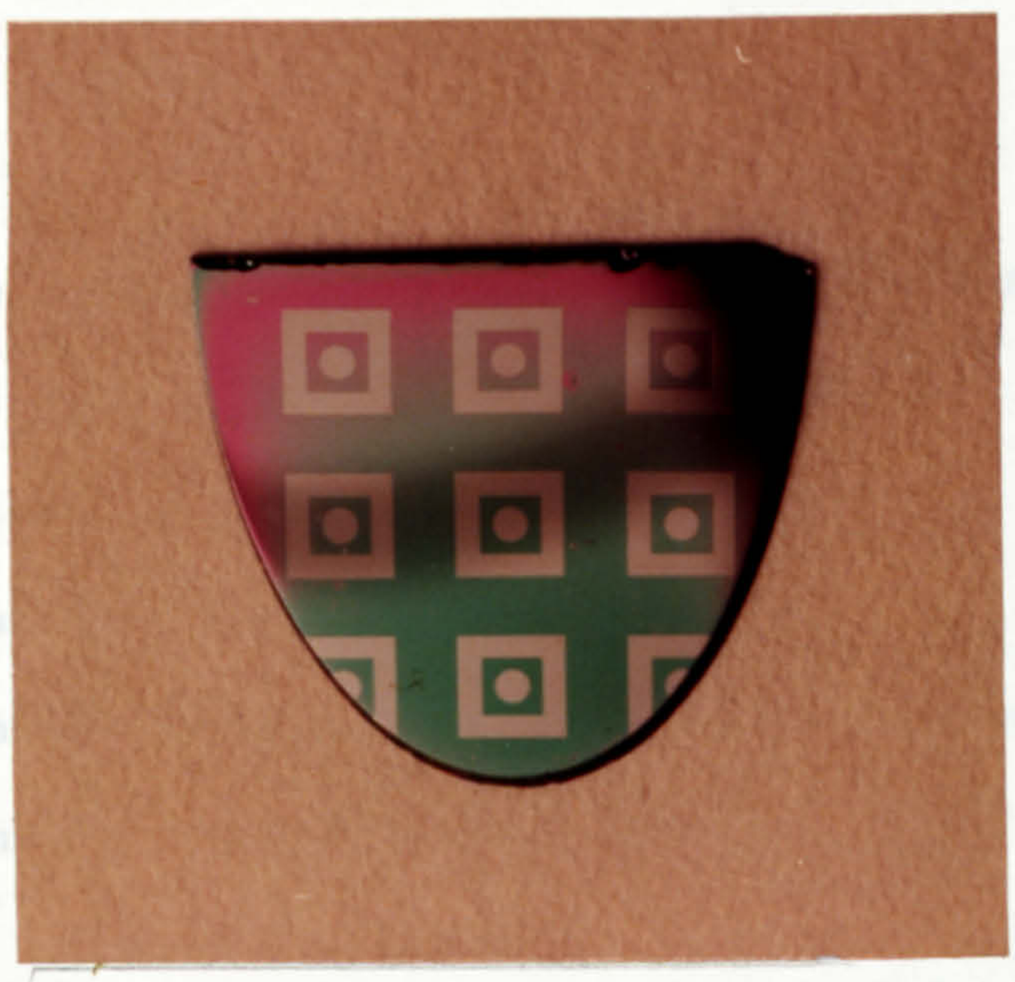


Fig 4.7 (100) Oriented Silicon Sample with SiO_2 Removed Ready for Etching

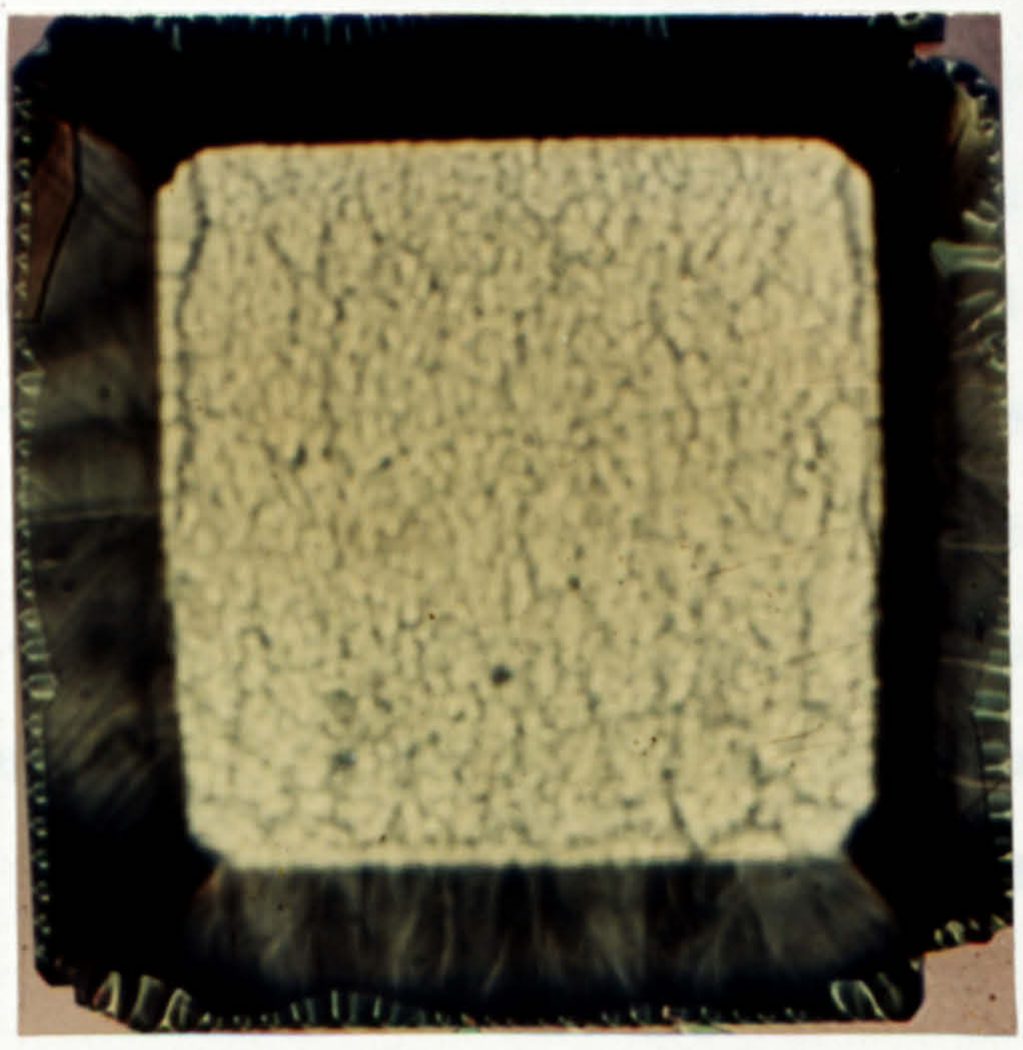


Fig 4.8 Plan View of an Etched Silicon Sample

CHAPTER 5 FABRICATION OF nCdS-pSi HETEROJUNCTIONS

5.1 Introduction

Many different techniques are required in the fabrication of an nCdS-pSi heterojunction, Figure 5.1 shows schematically the 21 stages involved. Rather than mention each individual step, it is more succinct to discuss the eight main technological processes, viz. polishing, oxidation, diffusion, photolithography, etching silicon, cleaning in vacuo, evaporation, and bonding. Since some of these processes have been discussed in Chapter 4, only the main features will be elucidated.

5.2 Polishing

The silicon used for fabricating both the T.E.M. specimens and the heterojunctions were supplied unpolished, in wafer form, by the manufacturer. The silicon was mechanically polished to an optical finish, the final stage utilising a one micron diamond compound.

All mechanically lapped or polished surfaces are left with surface layers of structurally damaged silicon. The damaged region may be removed by chemical [116] or electrolytic [117] means. Chemical polishing, while successful in removing damaged silicon, creates a rippled "orange peel" surface finish, which is not optically flat. Electrolytic polishing can produce an optically flat surface but requires the construction of an electropolishing apparatus. The method chosen was to remove the damaged layer by oxidising the surface and then etching the oxide using buffered H.F.

5.3 Oxidation

As mentioned earlier, the silicon was oxidised for 2 hours at 1180^{o}C with an oxygen gas flow rate of 0.6 litres/min. and a water bath

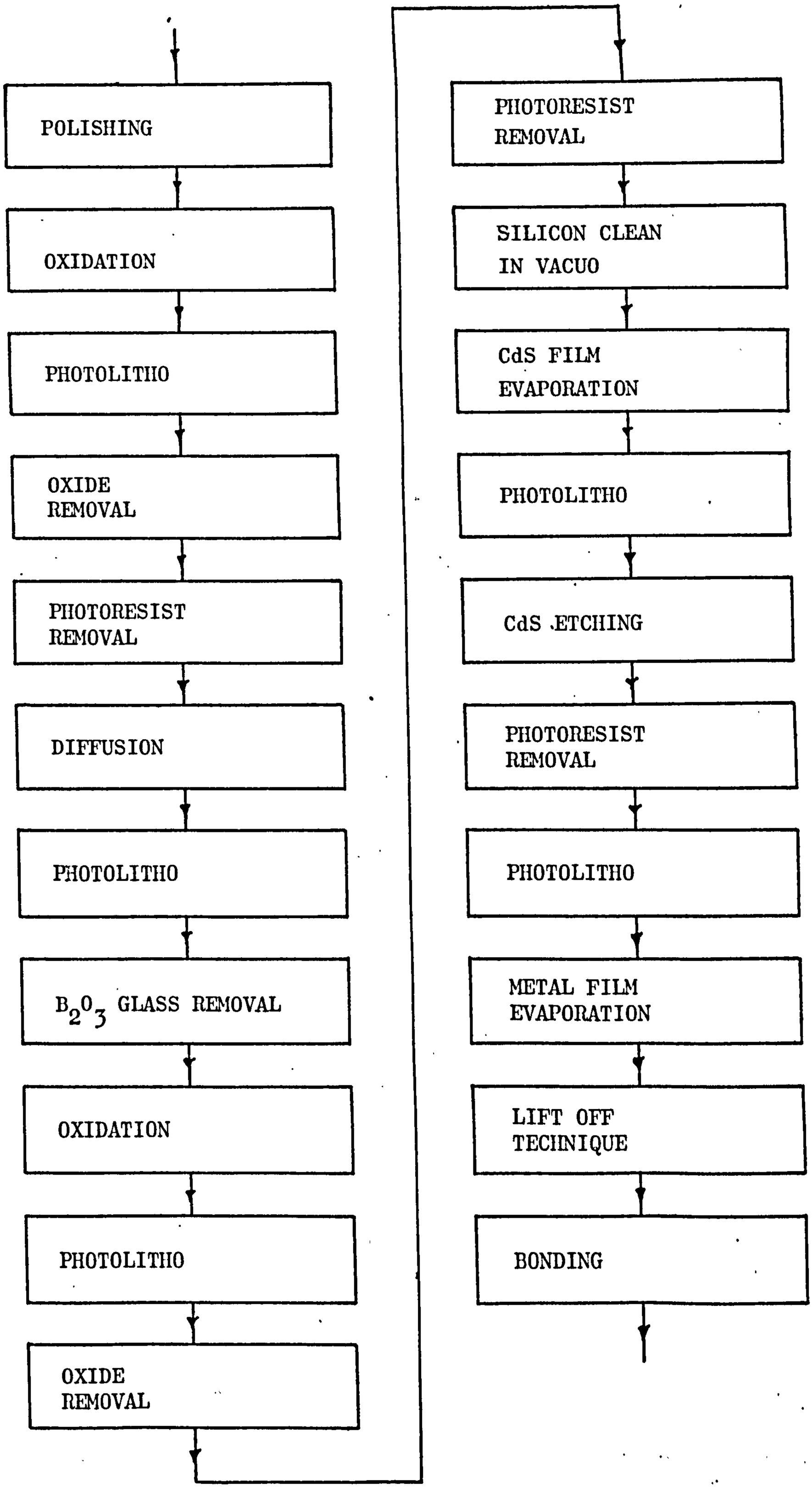


Fig 5.1 Processing Stages

temperature of 90°C. SiO_2 films 0.6 microns thick, having a uniform clear appearance from edge to edge, were grown under these conditions.

5.4 Diffusion

The back surface of the heterojunction was doped p^+ to ensure that the contact to the p-type silicon was ohmic. The diffusion was carried out at 1000°C for 30 minutes, with an N_2 flow rate of 0.2 litres/min., using a BN source. A problem was encountered when these substrates were cleaned at high temperature. It was discovered that heterojunctions fabricated using this method had ohmic characteristics. The boron was out-diffusing from the back surface and doping the surface where the CdS films were grown. This problem was circumvented by oxidising the silicon after the diffusion stage to seal the surface.

5.5 Photolithography

The basis of the masking process is the photoresist technique. A similar procedure to that used for the T.E.M. samples was employed. Three different masks were used in defining (i) the junction region by removing SiO_2 using buffered H.F, (ii) the CdS coverage by removing excess CdS using dilute hydrochloric acid, and (iii) the electrode metallisation pattern using lift-off. In cases (i) and (ii), the photoresist had to be post-baked, to harden it sufficiently, to resist the etchant. Provided the photoresist was not baked excessively, it could then be dissolved in acetone.

5.6 Silicon Cleaning in Vacuo

Silicon reacts virtually instantaneously with O_2 at room temperature to form a stable oxide (SiOx) layer which is approximately 30Å thick.

It is desirable to remove this residual oxide prior to the growth of the CdS film. Firstly, the amorphous oxide will influence the growth conditions for epitaxy[118] and may in fact inhibit epitaxy. Secondly, the interfacial insulating oxide will influence the barrier potentials at the heterojunction interface.

It has been found[119, 120] that a clean surface on a silicon single crystal can be obtained by thermal treatment, care being taken to use a very pure sample, excellent vacuum conditions, and to reduce other sources of contamination.

The temperature required, to clean silicon thermally in a high vacuum, depends on the partial pressure of oxygen at the surface. Lander and Morrison[121] found that there was a critical temperature above which a clean silicon surface could be obtained. This temperature was 670, 720, and 770°C at 10^{-9}, 10^{-8} and 10^{-7} torr respectively. The greater the excess of temperature over the critical value the greater was the rate of cleaning.

There are a number of sensitive experimental techniques available to examine silicon in the vacuum system before and after cleaning. These include measurements of oxidation and gas absorption rates, Auger neutralisation of He^+ ions, measurement of the threshold for photoelectric emission, low energy electron diffraction (L.E.E.D.), and reflection high energy electron diffraction (R.H.E.E.D.). Unfortunately, since none of these techniques was available, the only approach was to follow the heat treatment conditions of Hill and Simpson.[122] A method was therefore required to heat the silicon substrate to temperatures in excess of 1000°C. It was also important to localise the heated region, to minimise the rate of outgassing and contamination from stainless steel fittings adjacent to the silicon in the vacuum system.

A number of methods was available which included a radiant heater using an ellipsoidal reflector,[123] a resistively heated tungsten

radiator,[118, 124] argon ion bombardment,[125] and electron-beam cleaning.[122]

Argon ion bombardment was one of the methods which was tried. The distinguishing feature of this heat treatment is that the (inert) argon atoms, embedded after the bombardment, do not combine chemically with the substrate to be cleaned. The surface region is, however, heavily disturbed and damaged[125] by the treatment. Annealing is necessary both to cause the argon atoms to diffuse away and to restore the lattice structure. Better results are often achieved by applying a number of sequences of ion bombardment and annealing. This method was tried, but, as the photograph of Figure 5.2 shows, very severe damage to the silicon resulted. It was also found that it was difficult to maintain the discharge at the silicon surface. As it was particularly important to ensure that the silicon surface was not damaged, it was felt that this method was unsuitable.

The radiant heating method used by Unvala et al.[123] required a 1 kW heating source, and forced air cooling of the bell jar. Moreover the temperature was not uniform over the sample.

The resistively heated tungsten radiator of Jones et al.[118] and Unvala et al.[124], while able to provide uniform heating, required an internal heat shield with water cooling, and 700 W electrical power to reach 1200°C. There was also a significant time lag between completion of the cleaning and commencement of the evaporation.

A combination of both tungsten filament and electron-beam heating was used by Hill and Simpson.[122] The tungsten filament was used for low temperatures while the electron-beam heater was used for higher temperatures. The main advantage of the electron-beam gun was that the focus could be varied, i.e. the diameter of the hot region could be enlarged or decreased, and as a result outgassing was kept to a minimum.

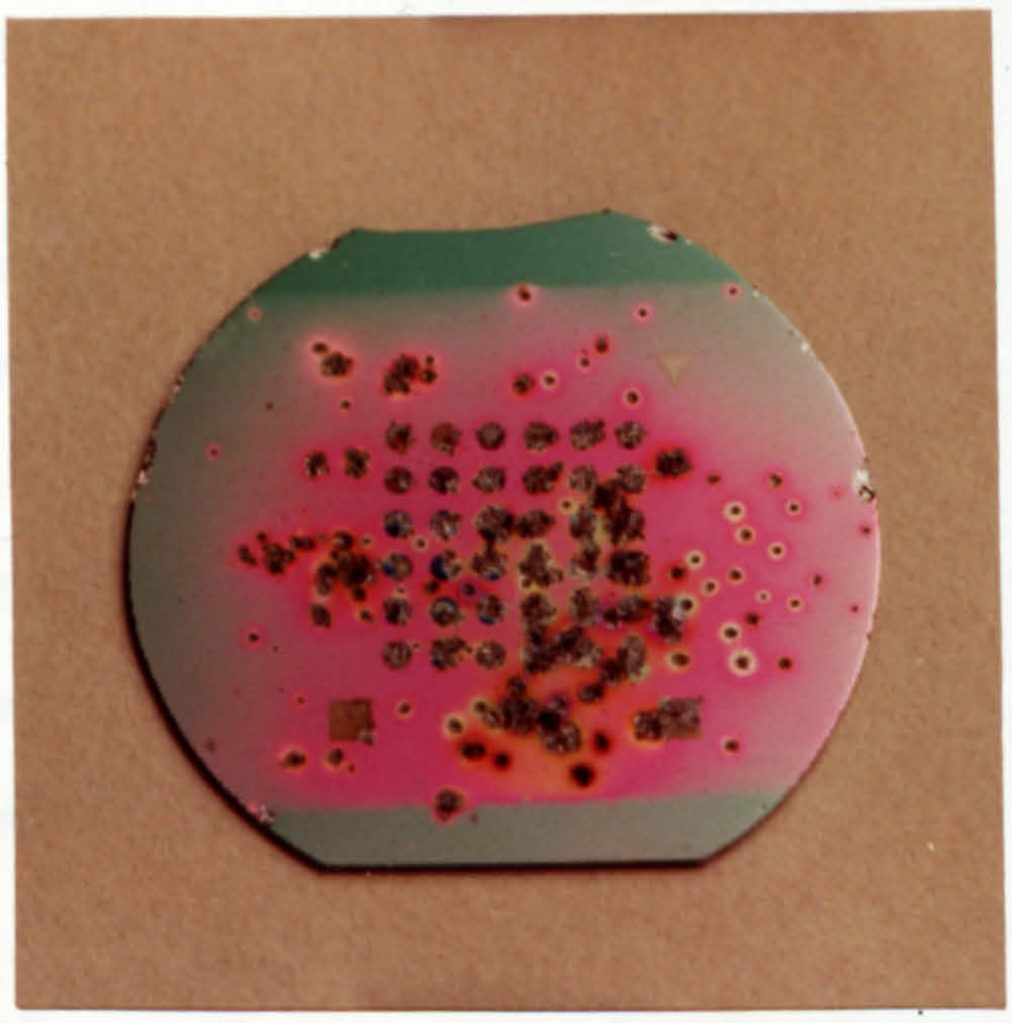


Fig 5.2 Surface Damage as a Result of Argon Ion Bombardment

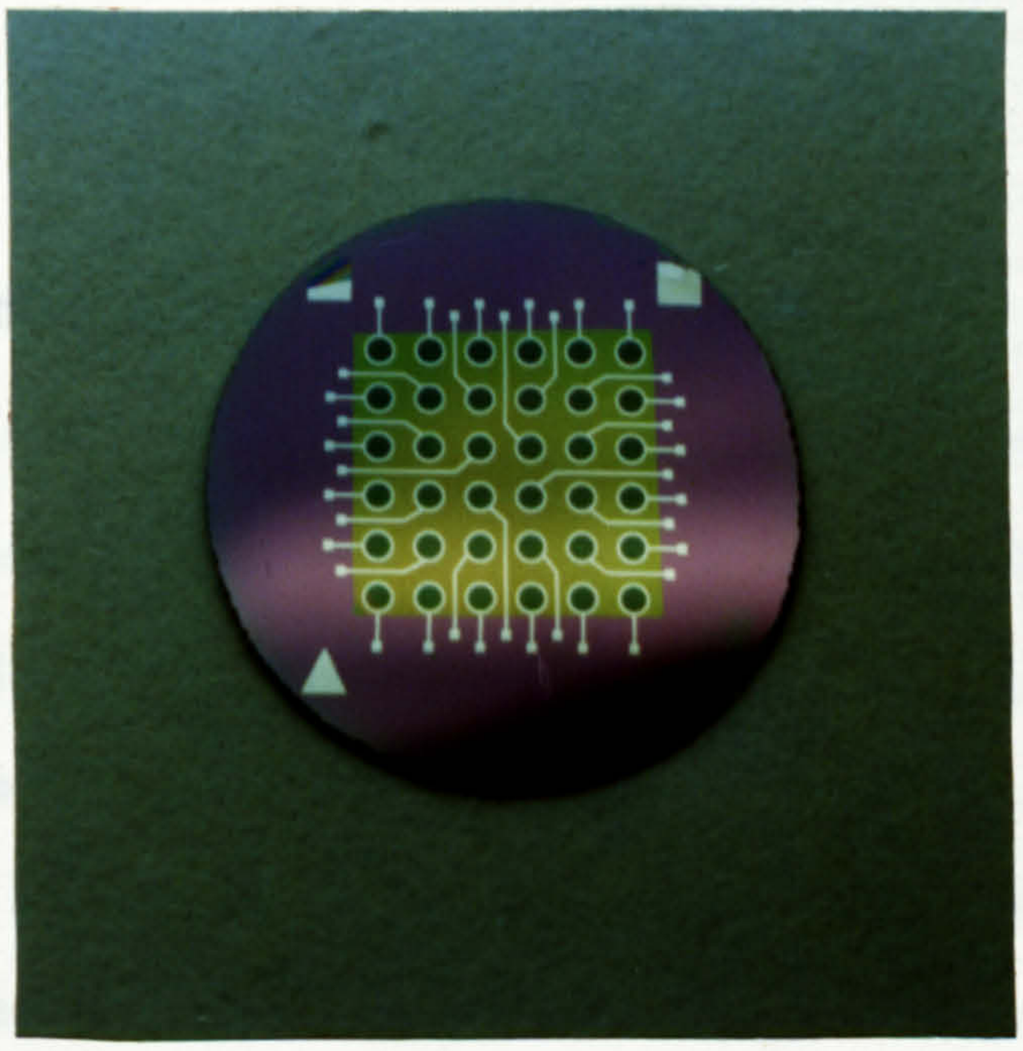


Fig 5.3 Completed nCdS-pSi Heterojunction Photodetector (2 1/4 X actual size)

The electrical power required, for the electron-beam gun used in this work, was only 180 W for a uniform temperature of 1000°C across a 19 mm silicon sample.

The first design of gun utilised magnetic deflection, with a stainless steel mesh to confine the fields. However, the temperature was not uniform across the sample. The major problem created by the design was that of contamination. Contamination by SiC was revealed by the T.E.M. diffraction patterns. The stainless steel mesh was heating up locally to temperatures close to 1000°C and was probably acting as a source of carbon. The gun was redesigned by W. Duncan and A. R. Smellie utilising electrostatic focussing. Not only was there no SiC contamination, but the temperature was uniform across the sample.

Some initial trouble was experienced when the temperature of the heated silicon was measured with a platinum-platinum/rhodium thermocouple. When the temperature was raised above 1000°C the platinum formed an alloy with silicon so destroying the thermocouple. The problem was remedied by placing a thin piece of molybdenum foil between the silicon and the thermocouple.

5.6.1 Silicon Cleaning, Experimental

The silicon was heated using the above electron-beam gun to 1000°C for 5 minutes at a pressure less than 5×10^{-8} torr. These conditions ensure the removal of the thin SiOx layer which grows at room temperature and any solvents or chemical contaminants which remain.[122] Figure 5.4 shows a schematic diagram of both the electron gun used for cleaning the silicon, (upper), and the electron gun used for the CdS evaporations, (lower). The substrate heater gun consisted of a thoriated tungsten filament, a cylindrical lens[126] and a molybdenum anode. The lens consisted of two stainless steel cylinders each maintained at potentials V_1 and V_2 and

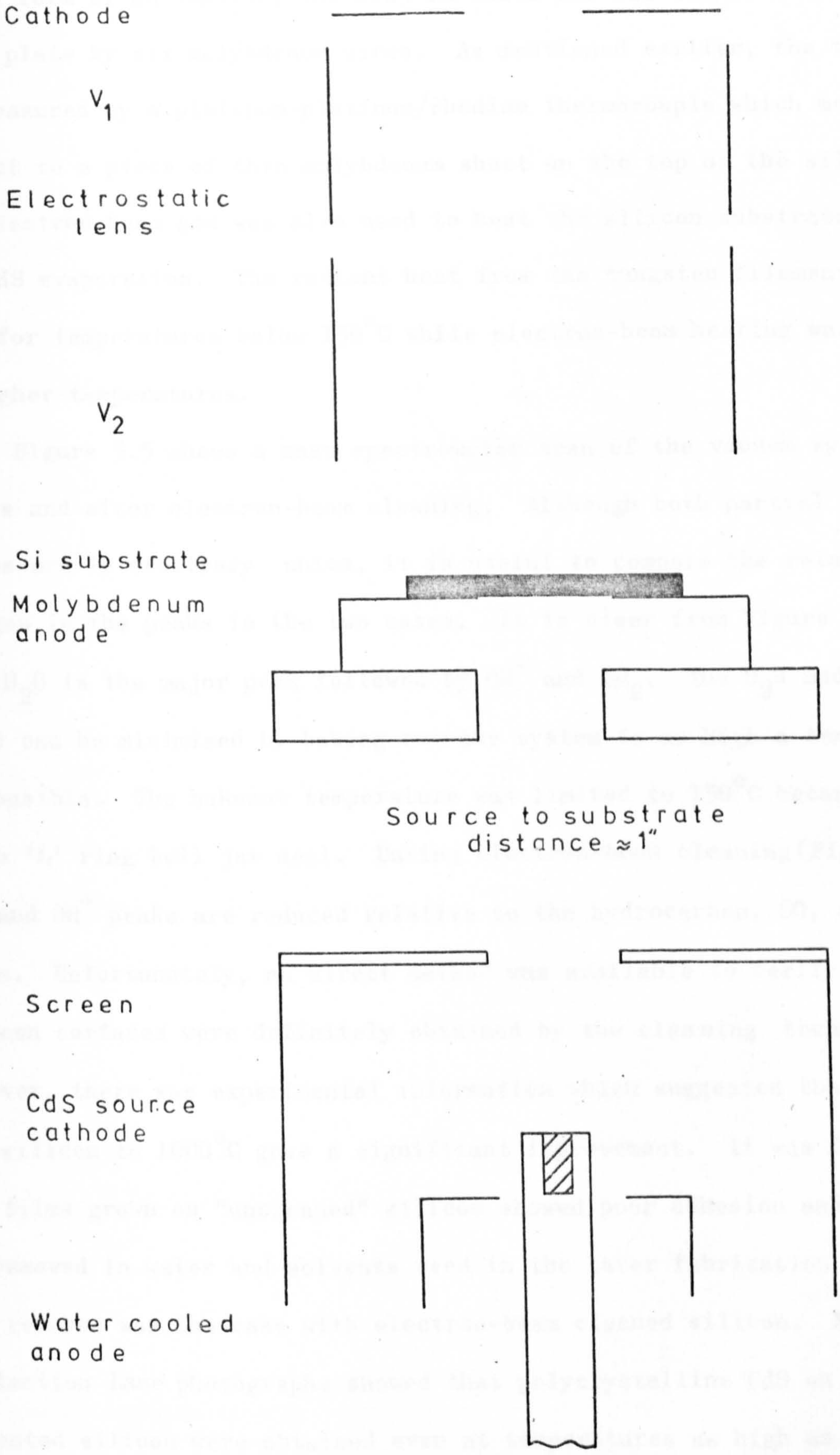
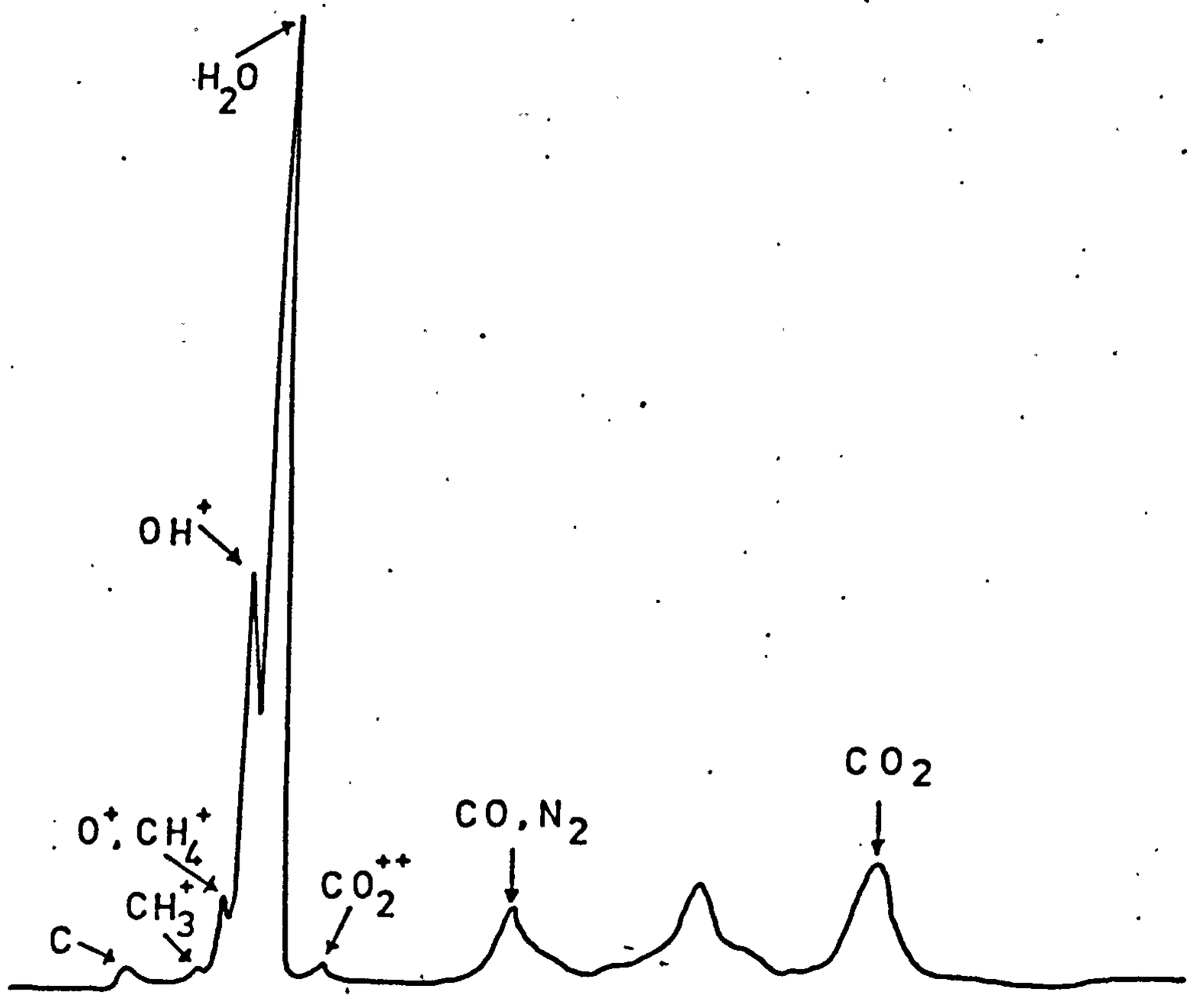


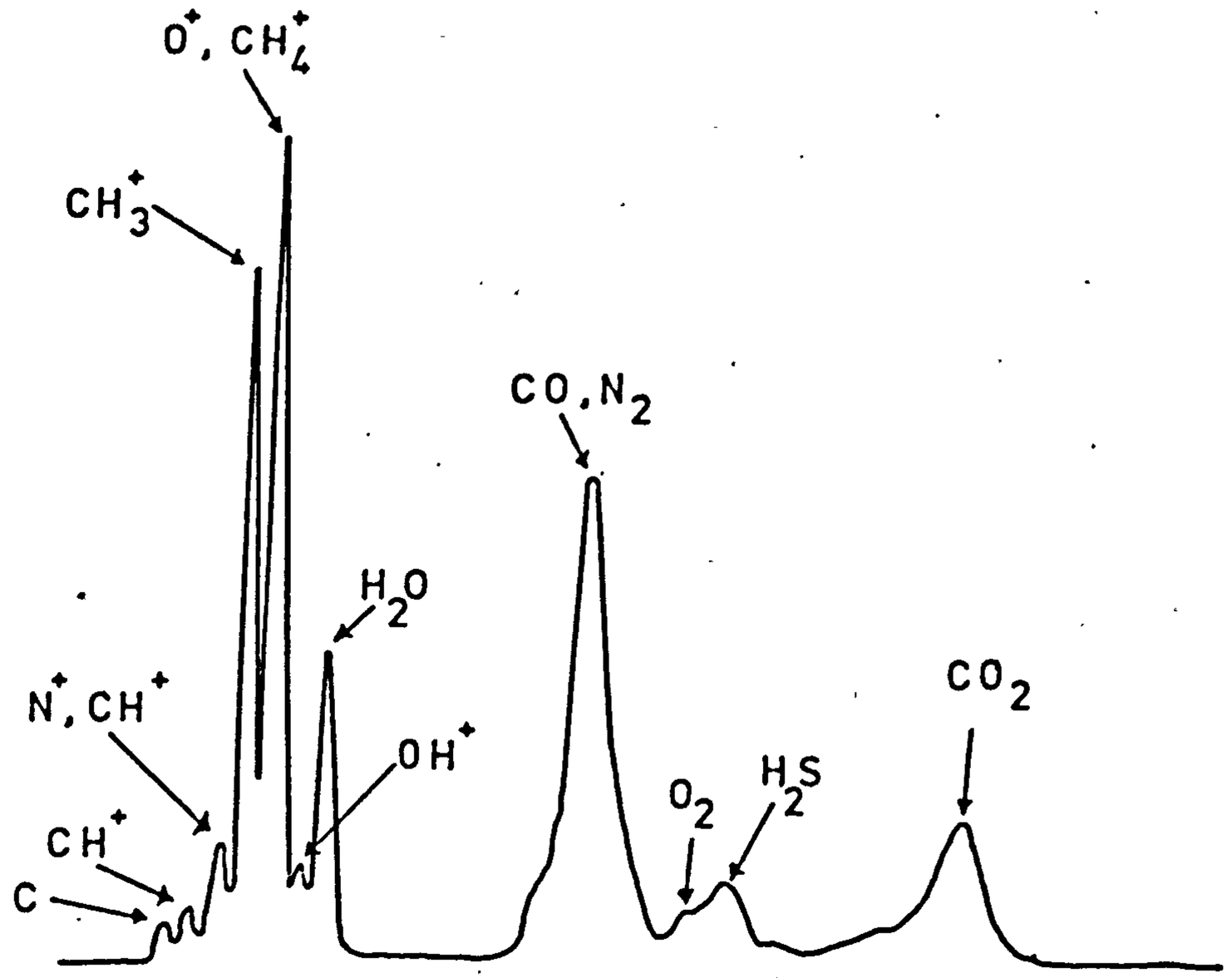
Fig 5.4 Electron-beam gun assembly

the beam was focussed by adjusting these voltages. The molybdenum anode, in the form of an annulus, was 0.25 mm thick and was supported on a stainless steel plate by six molybdenum wires. As mentioned earlier, the temperature was measured by a platinum-platinum/rhodium thermocouple which made a pressure contact to a piece of thin molybdenum sheet on the top of the silicon. The electron-beam gun was also used to heat the silicon substrate during the CdS evaporation. The radiant heat from the tungsten filament was used for temperatures below 150°C while electron-beam heating was used at higher temperatures.

Figure 5.5 shows a mass spectrometer scan of the vacuum system before and after electron-beam cleaning. Although both partial pressure scales are in arbitrary units, it is useful to compare the relative changes in the peaks in the two cases. It is clear from Figure 5.5(a) that H_2O is the major peak followed by OH^+ and CO_2. The H_2O and OH^+ peaks can be minimised by baking out the system to as high a temperature as possible. The bakeout temperature was limited to 150°C because of the Viton 'L' ring bell jar seal. During electron-beam cleaning (Figure 5.5(b)) the H_2O and OH^+ peaks are reduced relative to the hydrocarbon, CO, and CO_2 peaks. Unfortunately, no direct method was available to verify that clean silicon surfaces were definitely obtained by the cleaning technique used. However, there was experimental information which suggested that heating the silicon to 1000°C gave a significant improvement. It was found that CdS films grown on "uncleaned" silicon showed poor adhesion and could often be removed in water and solvents used in the later fabrication stages. The reverse was the case with electron-beam cleaned silicon. X-ray back reflection Laue photographs showed that polycrystalline CdS on (111) oriented silicon were obtained even at temperatures as high as 400°C, whereas epitaxial CdS films were obtained at substrate temperatures in



(a) Before Electron-Beam Cleaning



(b) During Electron-Beam Cleaning

Fig 5.5 Mass Spectrometer Scans (arbitrary scales)

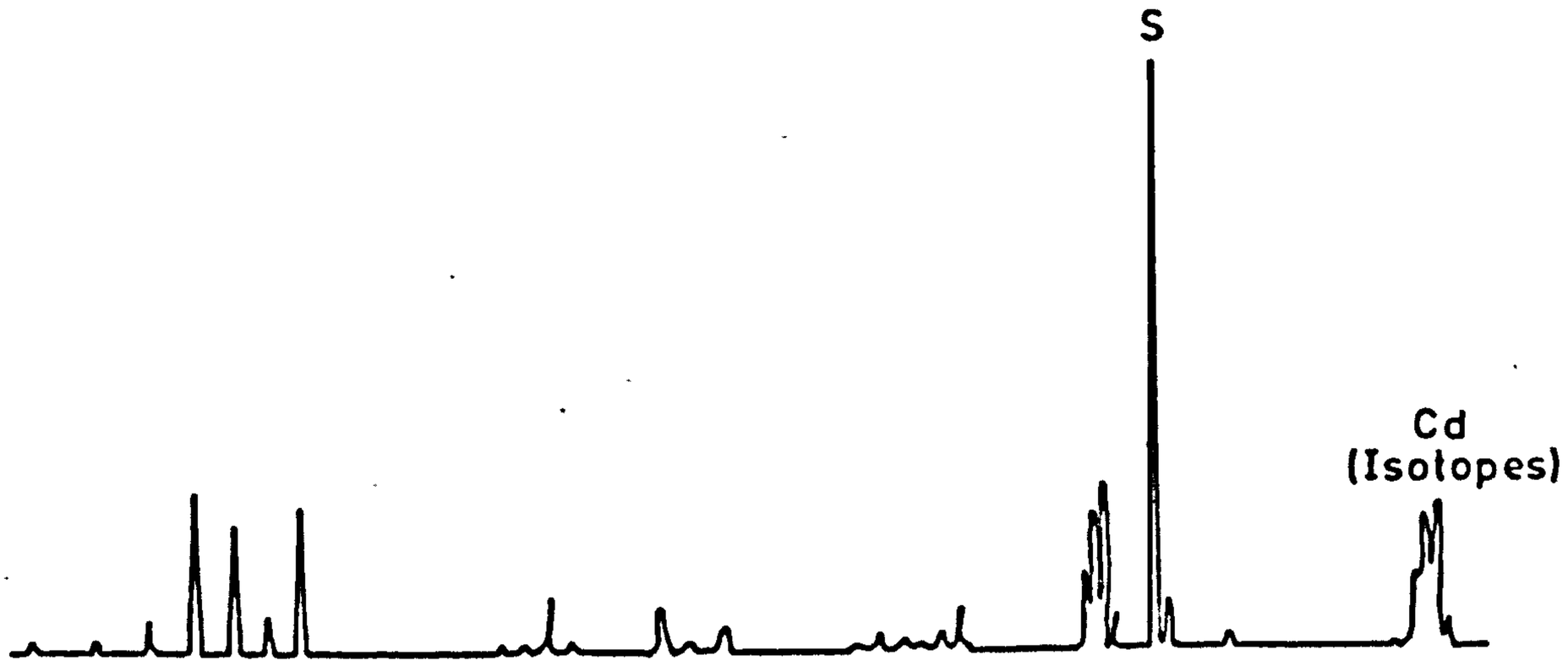
excess of 300°C when the silicon was cleaned. Heterojunction devices fabricated using cleaned silicon showed significantly more reproducible characteristics compared with those made using "uncleaned" silicon.

5.7 Vacuum Deposition

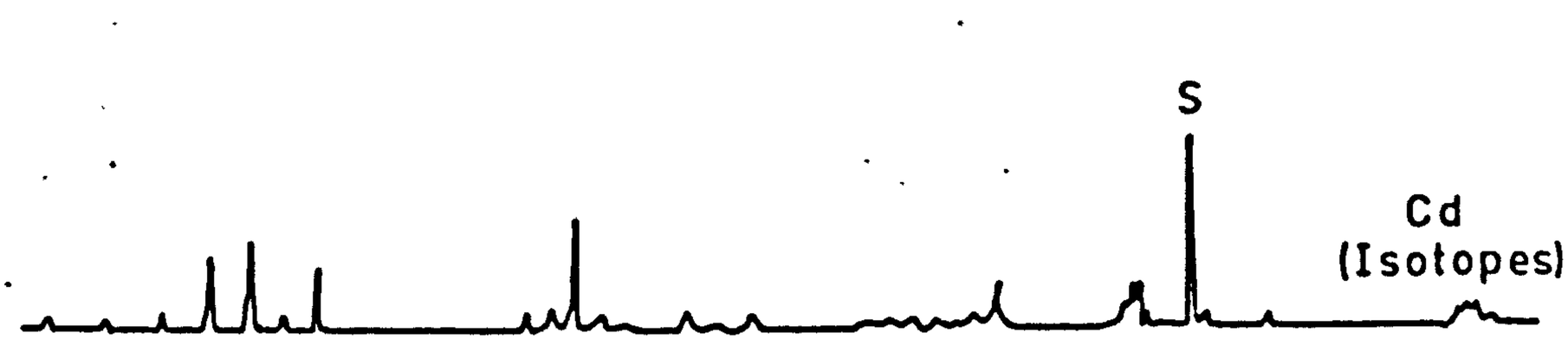
The system used for CdS evaporations consisted of a two stage 200 litre/sec rotary pump with a zeolite trap backed by a 50 litre/sec ion pump and titanium sublimation pump. The chamber was baked out for 12 hours at 100°C to obtain pressures below 10^{-9} torr by reducing the partial pressure of water vapour.

CdS films were grown at pressures below 10^{-7} torr, using an electron gun (Vacuum Generators type E.G.2), on Si substrates which had been previously cleaned at 1000°C. The E.G.2 gun utilised a water cooled copper anode hearth to minimise contamination. The complete gun assembly is shown schematically in Figure 5.4. Typical substrate temperatures were between room temperature and 350°C. At room temperature dark, cadmium rich, films were obtained; while at higher temperatures yellow sulphur rich films were obtained.

The CdS source material was either Eagle Picher grade 'A', single crystal, or 'Optran' grade, polycrystal, from B.D.H. Chemicals. A mass spectra scan is shown in Figure 5.6 taken during evaporations of 'Optran' and grade 'A'. The AEI MS10 mass spectrometer used for the scan was of higher resolution than the AEI Minimass used in obtaining the results in the section on cleaned silicon. As the partial pressure scale is arbitrary in both cases shown in Figure 5.6, comparisons cannot be made directly between the two mass spectra. However, the ratio of the sulphur partial pressure to the total partial pressures of the cadmium isotopes is 1.5 for Optran and approximately 4 for grade 'A'. Most of the evaporations



(a) CdS 'Optran' Grade



(a) CdS 'A' Grade

Fig 5.6 Mass Spectrometer Scan During Evaporation of CdS

were carried out using Optran material.

Metal evaporations were carried out in an Edwards oil pumped coating unit at approximately 3×10^{-5} torr. Metal coatings were typically 0.5 microns thick using either an electron-beam evaporator or a resistively heated filament.

5.7.1 Sulphur-Silicon Reactions

Holt and Steyn[56] made some calculations of the free energy changes involved in the possible reactions between CdS and Si. They found that as the substrate temperature was increased it became energetically favourable to form gaseous SiS a reaction which caused pitting of the silicon and no CdS film growth. Their work indicated that a CdS film would grow if SiS_2, a solid, was formed. A quartz crucible containing sulphur was used to introduce sulphur while the silicon was at 1000°C in order to promote the formation of SiS_2. This process did increase the deposition cut off temperature but at the cost of sulphur diffusing into the silicon. Sulphur is a fast n-type dopant in silicon,[127] with a diffusion coefficient of 6.6×10^2 μm^2/hr compared with 5×10^{-3} μm^2/hr for boron at 1000°C. A calculation showed that if silicon ($N_A = 6 \times 10^{12}$ cm^{-3}) at 1000°C was exposed to sulphur for 5 minutes the junction depth would be 27 microns. This method, which had only been used in the fabrication of two devices, was discontinued immediately. The deposition cut off temperature was increased by decreasing the source to substrate distance and/or increasing the evaporation rate.

5.8 Bonding

A Hughes Model HPB-360 pulsed thermal compression bonding machine was used to make electrical connections to the metal electrode deposited

on the CdS film.

Figure 5.3 shows a photograph of a completed nCdS-pSi heterojunction photodetector $2\frac{1}{4}$X actual size. The three marker regions, used to align the different masks, are round the periphery of the device. The purple coloured region is SiO_2 while the yellow square region is the deposited CdS film. The contacts are made to the CdS region using the aluminium ring electrode. The aluminium pads on the SiO_2 are used for bonding purposes. The region inside the ring is CdS and is darker than the surrounding CdS because the SiO_2 has been removed.

There were problems associated with bonding. It was usually only possible to make bonds to about 80% of the 36 contact pads. Examination, using an optical microscope, revealed that failure was either caused by too thin a film or lack of adhesion. The former was easily remedied while reasons for the latter were not completely understood. Only two metals have been found satisfactory for their ability to provide a good mechanical bond to SiO_2; aluminium and chromium. Both these metals are active reducing agents and can combine with the oxygen from the silicon dioxide layer. Three probable reasons for poor adhesion were, a residual layer of photoresist, solvent and/or chemical contamination, or the presence of a thin surface layer of B_2O_3 glass.

CHAPTER 6 STRUCTURAL AND TRANSPORT PROPERTIES OF CdS FILMS GROWN ON SINGLE-CRYSTAL SILICON

6.1 Introduction

The structure of CdS films grown on single-crystal silicon substrates was examined using both transmission electron diffraction and X-ray diffraction techniques. Transmission electron microscopy can provide information on the nucleation and growth mechanisms involved in epitaxy and on the defects in epitaxial films. It was only possible, however, to use transmission electron diffraction, in this work, for examining CdS films grown on (100) oriented silicon substrates because of the preferential etching technique used. As some work carried out in this department by D. Cameron showed that it was possible to grow epitaxial CdS films, of the wurtzite structure, on (100) oriented NaCl, it was thought that the restriction to the use of (100) oriented silicon substrates was not a serious limitation. However, it was found that only polycrystalline CdS films were obtained on (100) oriented silicon substrates over a wide range of growth temperatures (100-400^{o}C). X-ray diffraction, therefore, was used both for CdS films grown on (100) and (111) oriented silicon. A requirement of transmission electron diffraction was that the thickness of the composite structure, CdS film grown on Si substrate, must not exceed about 2,000Å. This ensured that the intensity of the transmitted beam was not reduced to such an extent that the diffraction pattern could not be observed. On the other hand, when using the back reflection Laue technique, it was necessary to have CdS film thicknesses in excess of one micron to ensure that the CdS film would diffract the X-ray beam. Although the Laue technique was valuable for correlating the transport properties with thick films, it was not a suitable technique for carrying out nucleation studies, as thin films are required. It would have been useful to examine CdS films grown on (111) oriented silicon using transmission electron diffraction, but the non-preferential etches, which might have been used,[113,114] are difficult

to control.

Hall measurements were used to give information regarding the net impurity carrier concentrations, its conductivity type, and the Hall mobility of CdS films grown on both (100) and (111) oriented p-type silicon substrates over a range of growth temperatures (200-340°C).

6.2 Transmission Electron Diffraction on (100) oriented Si

An electron diffraction pattern is essentially a record of the structure of the specimen under examination. If the specimen is a single-crystal then the diffraction pattern consists of a simple array of bright spots. The arrangement of the spots in the single-crystal diffraction pattern depends on the orientation. The diffraction pattern of a poly-crystalline specimen consists of a series of concentric rings. This is really the pattern of a large number of single-crystal diffraction patterns, each rotated by a small amount with respect to each other. If the poly-crystalline specimen has a preferred orientation the diffraction pattern consists of concentric rings, but with certain parts of the rings very much brighter than others. Figure 6.1 shows a schematic representation of the electron scattering, intensity distributions, and final diffraction patterns from a single crystal and a polycrystalline specimen. It is the spacings between the individual planes, in the sets of parallel planes, known as d-spacings, and the orientation relationship between the various sets of parallel planes, that can be determined by electron diffraction analysis. The particular orientations, at which sets of lattice planes, with certain d-spacings will diffract the electron beam to form discrete diffraction spot or ring reflections, are defined by the Bragg law:

$$\lambda = 2d_{hkl} \text{ Sin } \theta \qquad (6.1)$$

where the wavelength of incident electrons λ, varies with the accelerating voltage applied to the electron gun and, at 80 KV, $\lambda = 0.004$ nm. Using

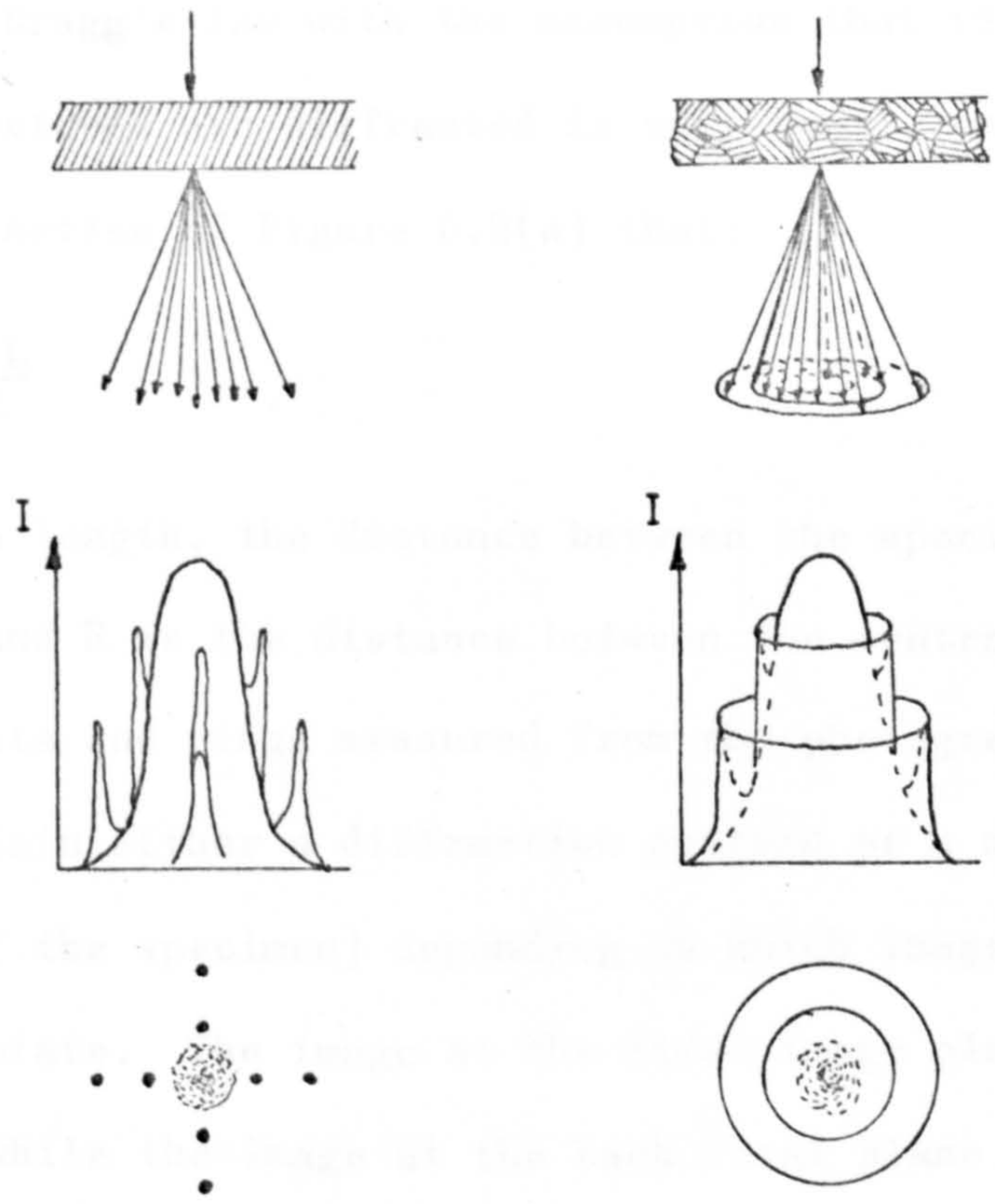
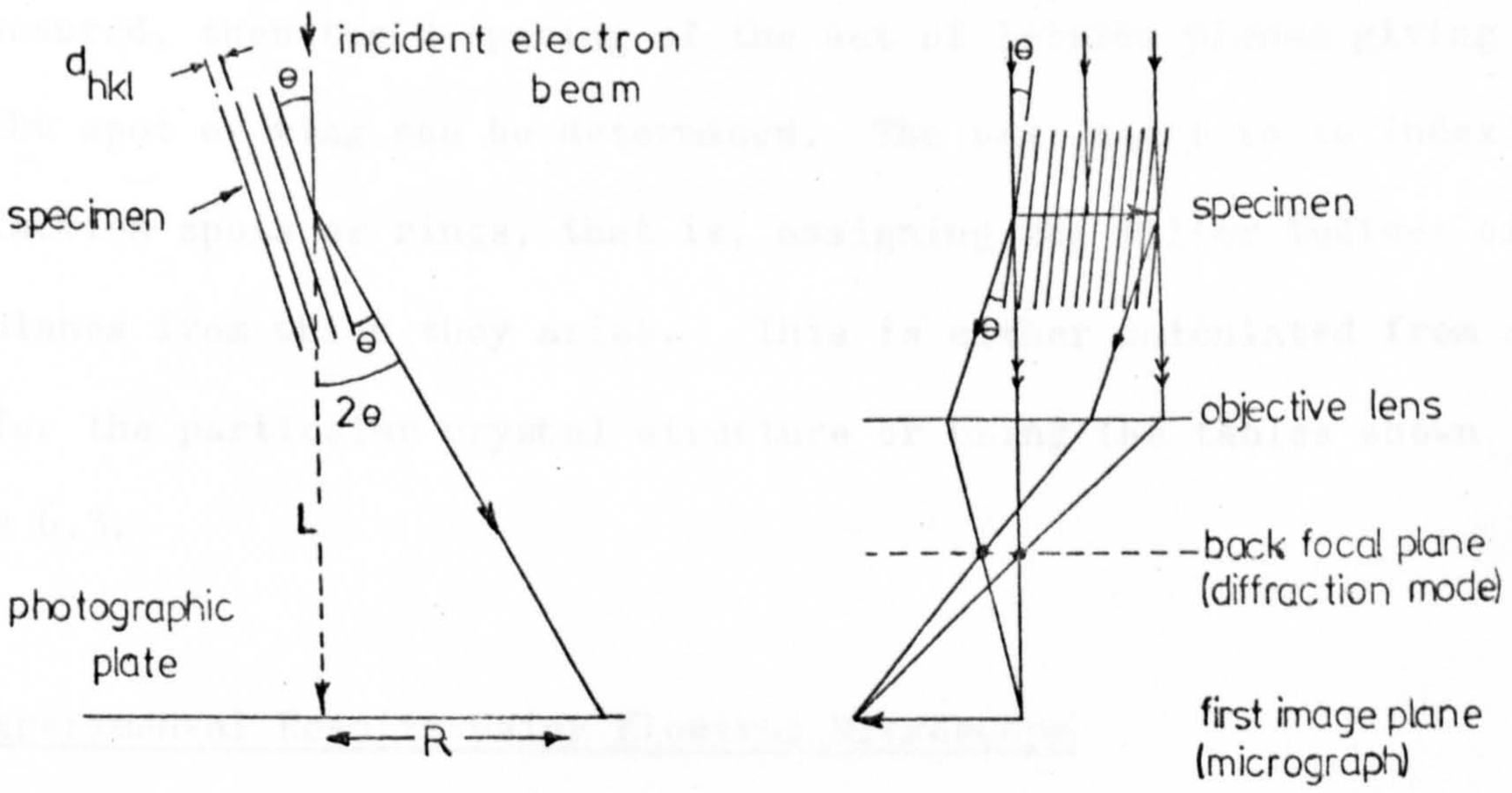


Fig 6.1 Schematic representation of the electron scattering, intensity distributions and final diffraction patterns from a single-crystal and a polycrystalline specimen.(128)



(a) (b)

Fig 6.2 Ray diagrams tracing paths of electron beam.(128)

simple geometry, and Bragg's law with the assumption that the angle through which the electrons are diffracted is very small, only 1^{o}-2^{o}, it can be shown by examination of Figure 6.2(a) that:

$$d = \frac{\lambda L}{R} \qquad (6.2)$$

where L is the camera length, the distance between the specimen and the photographic plate, and R is the distance between the central spot and the other diffraction spots and rings measured from the photographic plate. It is possible to obtain either a diffraction pattern or a micrograph (a magnified image of the specimen) depending on which image is recorded on the photographic plate. The image at the first image plane gives the electron micrograph while the image at the back focal plane gives the diffraction pattern. Figure 6.2(b) is a ray diagram showing the transmitted and diffracted beams, and the position of the back focal plane and the first image plane.

If values of R, L, and λ for a particular diffraction spot or ring can be measured, then the d-spacing of the set of lattice planes giving rise to the spot or ring can be determined. The next stage is to index the diffraction spots or rings, that is, assigning the Miller indices of the lattice planes from which they arise. This is either calculated from a formula for the particular crystal structure or using the tables shown in Figure 6.3.

6.2.1 Experimental Results Using Electron Microscope

CdS films were grown on electron-beam cleaned, thinned, silicon at temperatures in the range 100-400^{o}C. At the initial stages, it was found that the silicon was too thick, being of the order of 5,000Å. Figure 6.4 shows a photograph of a diffraction pattern from a silicon sample which was too thick for the purposes of examination of composite

d	3.16	3.58	3.36	3.58	CdS	
I/I$_1$	100	75	60	75	Cadmium Sulfide	(Greenockite)

Rad. CuKα	λ 1.5405	Filter Ni
Dia.	Cut off	Coll.
I/I$_1$ Diffractometer		d corr. abs.?
Ref. NBS Circular 539 Vol II pp 15-16 (1955)		

Sys. Hexagonal			S.G. $P6_3mc$ (186)	
a_o 4.136	b_o	c_o 6.713	A	C 1.623
α	β	γ	Z 2	
Ref. Ibid.				

ε α	nωβ 2.506	γ 2.529	Sign +
2V	Dx 4.82 mp	Color Yellow	
Ref. Dana's System of Mineralogy 7th Ed., Vol. I			

Sample from R.C.A. Spect. Analysis: <0.01% Al, B, Fe, Mg, Si; <0.001% Ca, Cu.
X-ray pattern at 25°C.
The sample was heated at 400°C for 30 hours in S atmos. to eliminate cubic phase.

d Å	I/I$_1$	hkl	d Å	I/I$_1$	hkl
3.58	75	100	1.1249	8	302
3.36	60	002	1.0743	6	205
3.16	100	101	1.0540	2	214
2.450	25	102	1.0340	4	220
2.068	55	110	0.9934	4	310
1.898	40	103	.9881	6	222
1.791	18	200	.9842	6	116
1.761	45	112	.9827	6	311
1.731	18	201	.9729	2	304
1.679	4	004	.9533	10	215,312
1.581	8	202	.9265	2	107
1.520	2	104	.9081	8	313
1.398	16	203	.8956	2	400
1.3536	6	210	.8878	2	401
1.3271	12	211	.8804	4	224
1.3032	8	114	.8653)	4 1	(402
1.2572	12	105	.8624)	4 1	(216
1.2247	2	204	.8315	4	403
1.1940	8	300	.8166	4	306
1.1585	12	213	.8158	4	321

(a) Hexagonal form of Cd S

d	3.36	2.06	1.75	3.36	β-CdS	β-CdS
I/I$_1$	100	80	60	100	Beta Cadmium Sulfide	Hawleyite

Rad. CuKα	λ 1.5418	Filter Ni	Dia. 57.54mm
Cut off	I/I$_1$ Visual		
Ref. Traill and Boyle, Am. Min. 40 555 (1955)			

Sys. Cubic			S.G. $T_d^2 - F\bar{4}3m$ (216)	
a_o 5.818	b_o	c_o	A	C
α	β	γ	Z 4	Dx 4.87
Ref. Ibid.				

ε	nωβ	γ	Sign
2V	D	mp	Color Yellow
Ref. Ibid.			

Sample from Hector-Calumet mine, Galena Hill, Yukon.
Yellow coating on Sphalerite and Siderite.

d Å	I/I$_1$	hkl	d Å	I/I$_1$	hkl
3.36	100	111			
2.90	40	200			
2.058	80	220			
1.753	60	311			
1.680	10	222			
1.453	20	400			
1.337	30	331			
1.298	20	420			
1.186	30	422			
1.120	30	333,511			
1.028	5	440			
0.985	20	531			
.918	5	620			
.887	5	533			

(b) Cubic form of Cd S

Fig. 6.3 A.S.T.M. Index showing the d-spacings and Miller indices for both hexagonal and cubic forms of Cd S .

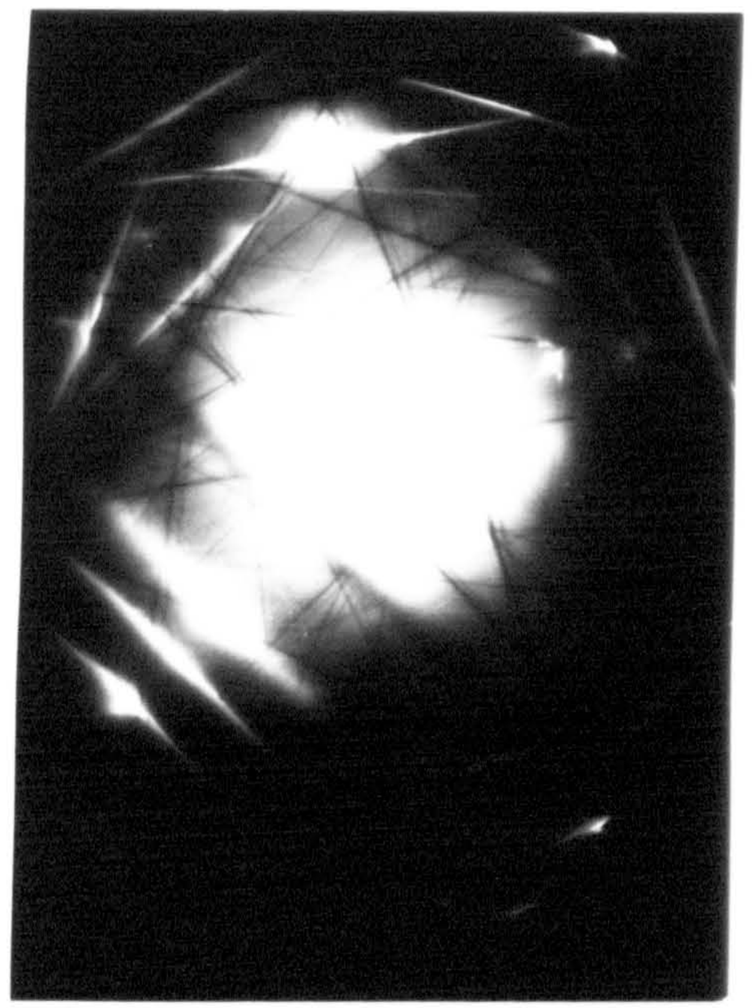


Fig. 6.4 Photograph of transmission electron diffraction pattern showing Kikuchi lines on (100) oriented Si.

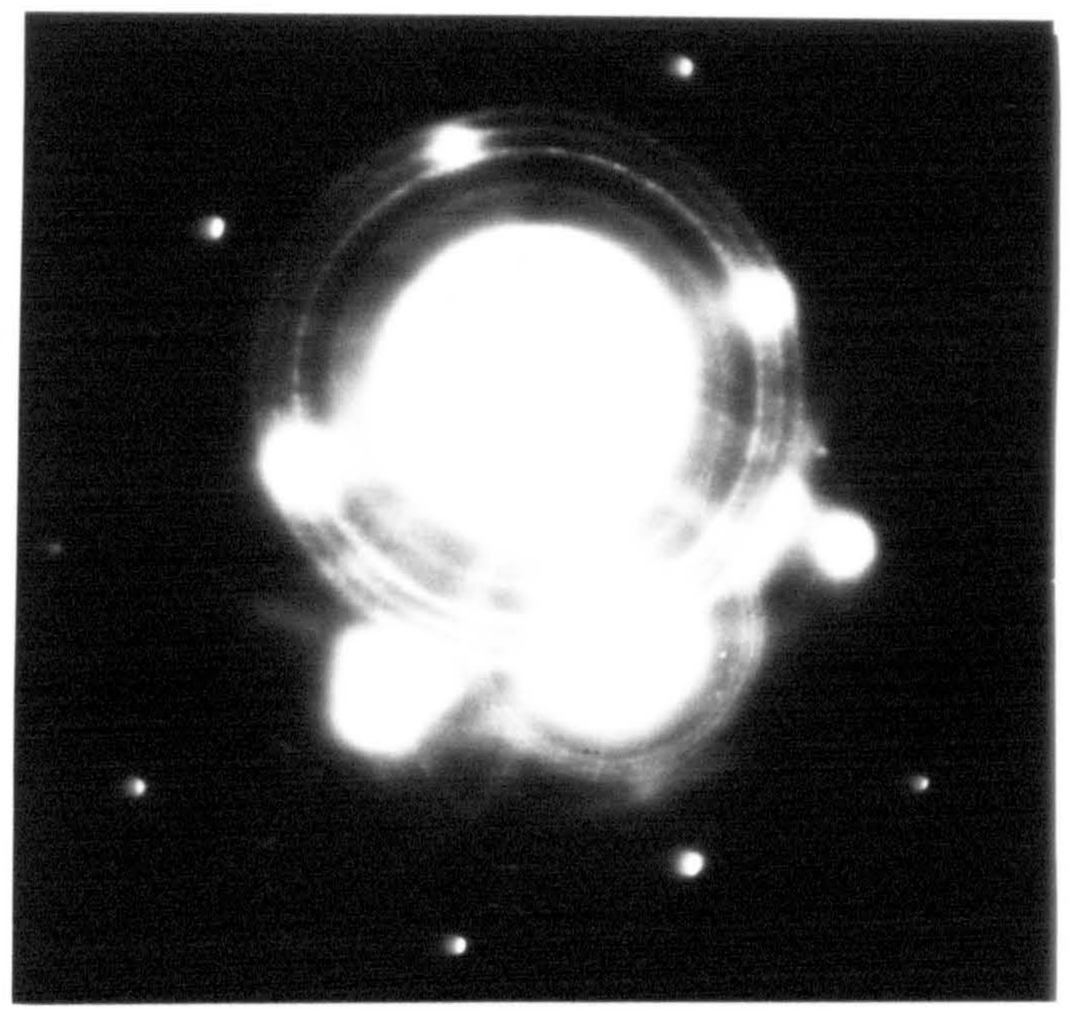
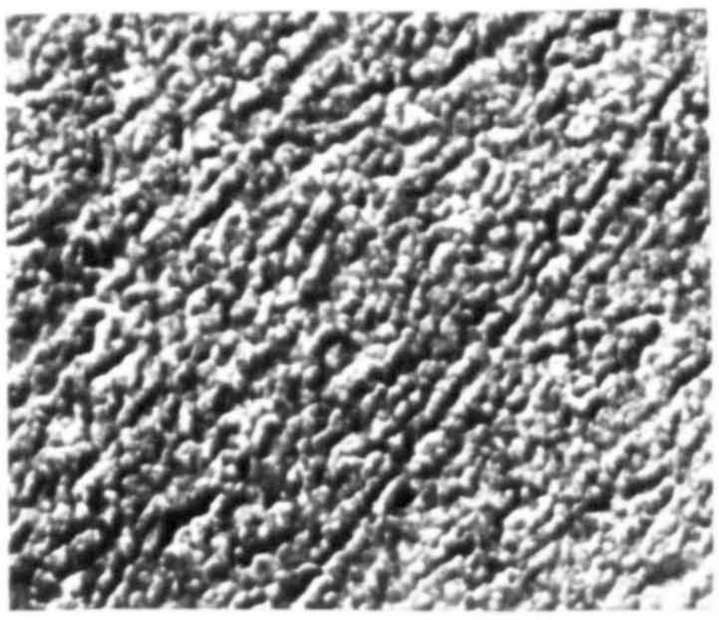


Fig. 6.5 Photograph of transmission electron diffraction pattern of CdS grown on (100) oriented Si. CdS growth temperature 300°C.

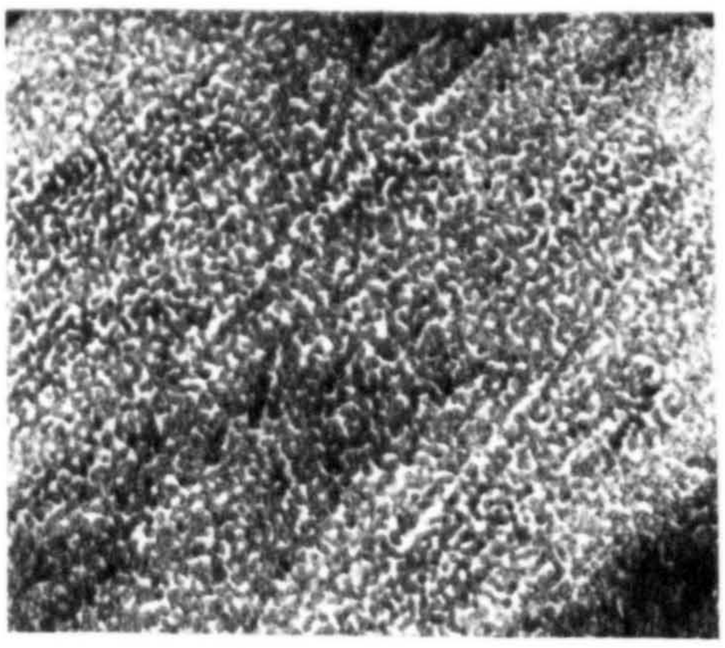
structures of CdS and Si. The dark lines crossing the photograph in all directions, called Kikuchi lines, are an indication that the Si was single-crystal and were only seen when the silicon was thick.

Randomly oriented films giving ring diffraction patterns were obtained over the temperature range 100-400°C. A photograph of a typical ring diffraction pattern is shown in Figure 6.5 for a film grown at a substrate temperature of 300°C. The ring diffraction pattern of the CdS film (randomly oriented) is superimposed on the spot pattern of the silicon substrate (single-crystal). The seven diffraction rings correspond to the following planes, (100)H, (002)H or (100)C, (101)H, (102)H, (110)H or (220)C, (103)H and (112)H or (311)C where 'H' and 'C' denote hexagonal or cubic structure respectively. As can be seen from the results and from Figure 6.3(a) and 6.3(b) it is not possible to say categorically whether the CdS film was the hexagonal (wurtzite) or the cubic (sphalerite) form. However, although three of the d-spacings measured could be assigned a Miller index of both cubic and hexagonal CdS, the d-spacings which could only be assigned one type of structure were of the hexagonal (wurtzite) form of CdS. The results are by no means conclusive but suggest that the CdS films were of the wurtzite structure.

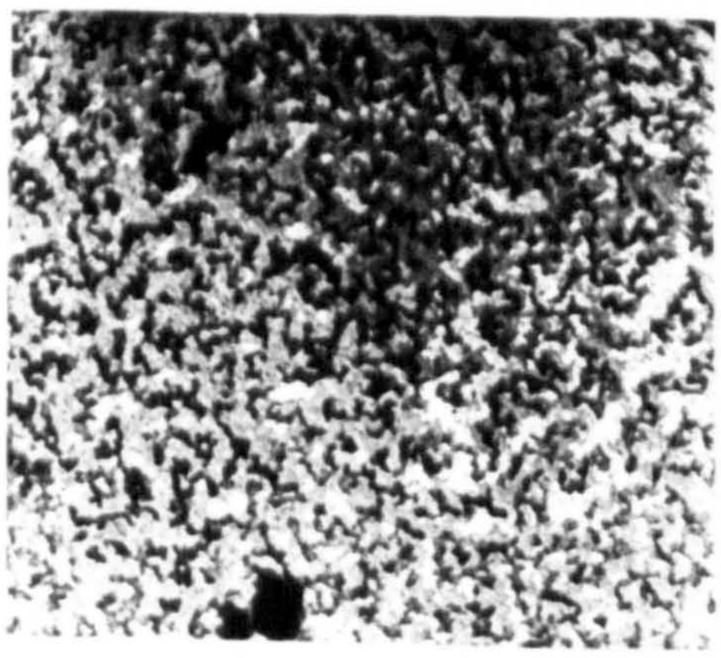
Figure 6.6 shows micrographs (20,000 X magnification) of CdS films grown at substrate temperatures of 100, 220 and 390°C respectively. It must be emphasised that the CdS film thickness was different in the three micrographs. The thickest film is shown in Figure 6.6(c) followed by 6.6(a) and then Figure 6.6(b). The CdS film shown in Figure 6.6(a) is nearly continuous and as a result it is not possible to identify individual crystallites. It is possible to identify individual CdS crystallites in Figure 6.6(b) their typical size being about 100Å. The darker regions are CdS crystallites while the white regions are thicker CdS. Because the CdS film shown in Figure 6.6(c) is thick it is not possible to identify



(a) Substrate temperature 100°C.



(b) Substrate temperature 220°C.



(c) Substrate temperature 390°C

Fig. 6.6 Transmission electron micrographs of CdS films grown on (100) oriented Si at 100, 220 and 390°C respectively (20,000 × magnification)

individual CdS crystallites. The thicker CdS regions (white) are beginning to form an interconnecting network. The micrographs show that the CdS films of thickness $\leq$ 1000Å are not perfectly flat and have variations in thickness from one region to the next.

6.2.2 SiC Contamination

In one of the initial experiments the thinned silicon was cleaned at high vacuum and was removed from the vacuum system without growing a film. Photographs of both the diffraction pattern and the micrograph are shown in Figure 6.7. The photograph of the diffraction pattern shows that there is a spot and ring pattern superimposed on the spot pattern observed previously for the (100) oriented silicon. On comparing the d-spacings shown in the A.S.T.M. index[129] it was discovered that two forms of silicon carbide were present. The spot diffraction pattern was due to epitaxial β SiC which is cubic, and the ring diffraction pattern was due to polycrystalline α SiC which is hexagonal. By moving the silicon specimen in the beam of the electron microscope, in the diffraction mode, it was possible to identify the regions of α and β SiC on the micrograph. The regions on the micrograph which appear to have been etched away i.e. the white areas, are the randomly oriented α form while the cubic shaped darker regions are the epitaxial β form of SiC. It was thought that the source of this contamination was the stainless steel mesh used in the first design of electron-beam cleaning gun. During the cleaning process it was observed that the mesh was heating locally to temperatures close to 1000°C. When the electron-beam cleaning gun was redesigned, without the stainless steel mesh, SiC contamination was no longer detected on the transmission electron diffraction patterns of thermally cleaned silicon.

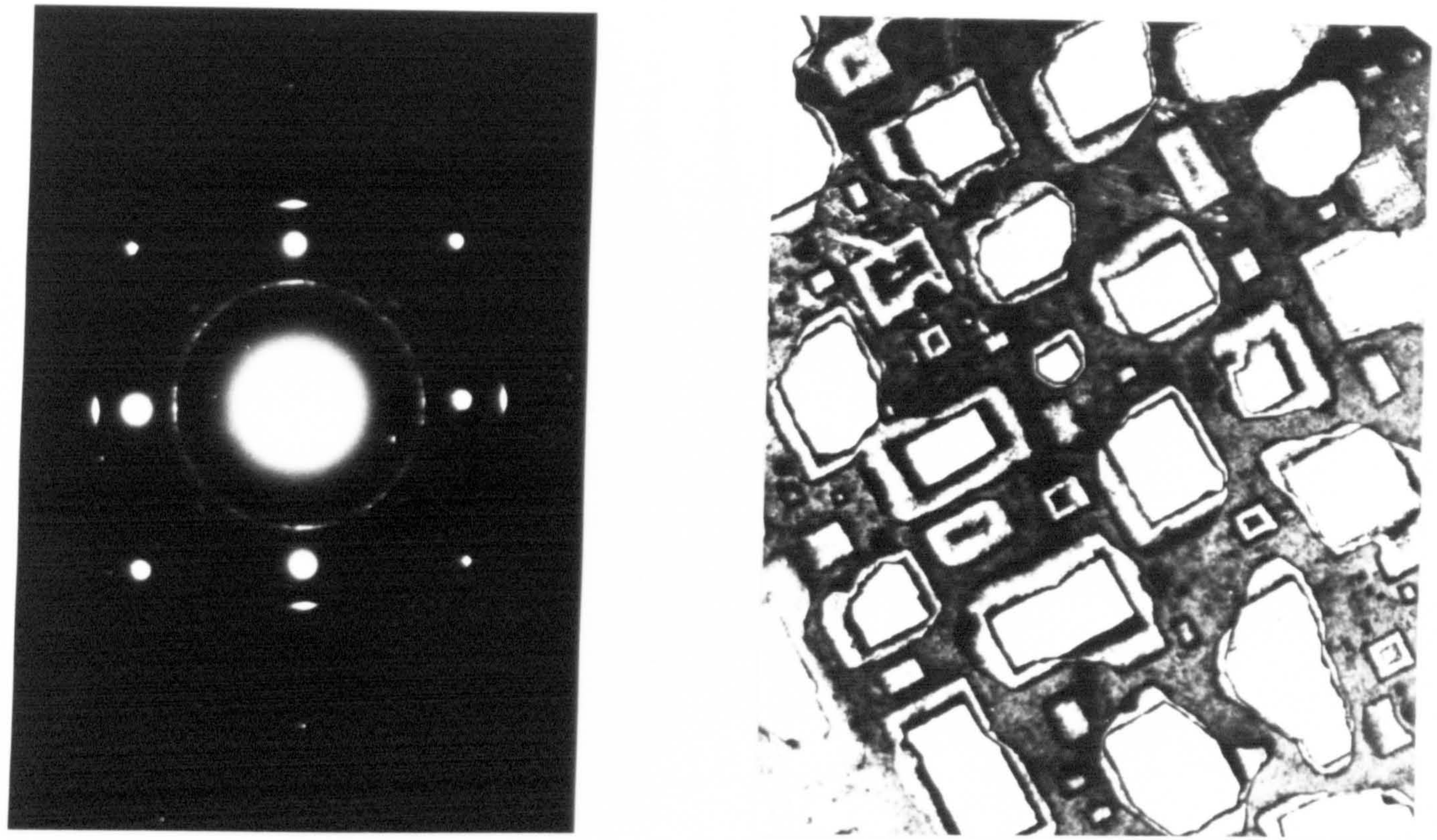


Fig. 6.7 Photograph of transmission electron diffraction pattern and micrograph (40 000 × magnification) for α and β SiC on (100) oriented Si.

6.3 X-ray Diffraction

Two of the main X-ray diffraction techniques are the Laue and powder methods.[130] In the Laue method λ is variable while θ is fixed. The converse is true for the powder method.

6.3.1 Laue Diffraction

There are two variations of the Laue method, depending on the relative positions of source, crystal, and photographic film. In each method the film is flat and placed perpendicular to the incident beam. The film in the transmission Laue method is placed behind the crystal in order to record the beams diffracted in the forward direction. In the back-reflection Laue method the film is placed between the crystal and the X-ray source, the incident beam passing through a hole in the film, and the beams diffracted in a backward direction are recorded. Both methods are shown schematically in Figure 6.8.

In either method, the diffracted beams form an array of spots on the film. If a photograph is examined carefully, the spots are seen to lie on certain curves. These curves are generally ellipses or hyperbolas for transmission patterns and hyperbolas for back-reflection patterns. This is illustrated in Figure 6.9.

6.3.2 Powder Method

Either a finely powdered specimen or a fine-grained polycrystalline specimen may be used in this method. Each particle of the powder is a tiny crystal oriented at random with respect to the incident beam. Figure 6.10(a) shows one plane in the set of (h, k, l) planes and the diffracted beam formed. If this plane is now rotated about the incident beam as axis, in such a way that θ is kept constant, then the reflected beam will

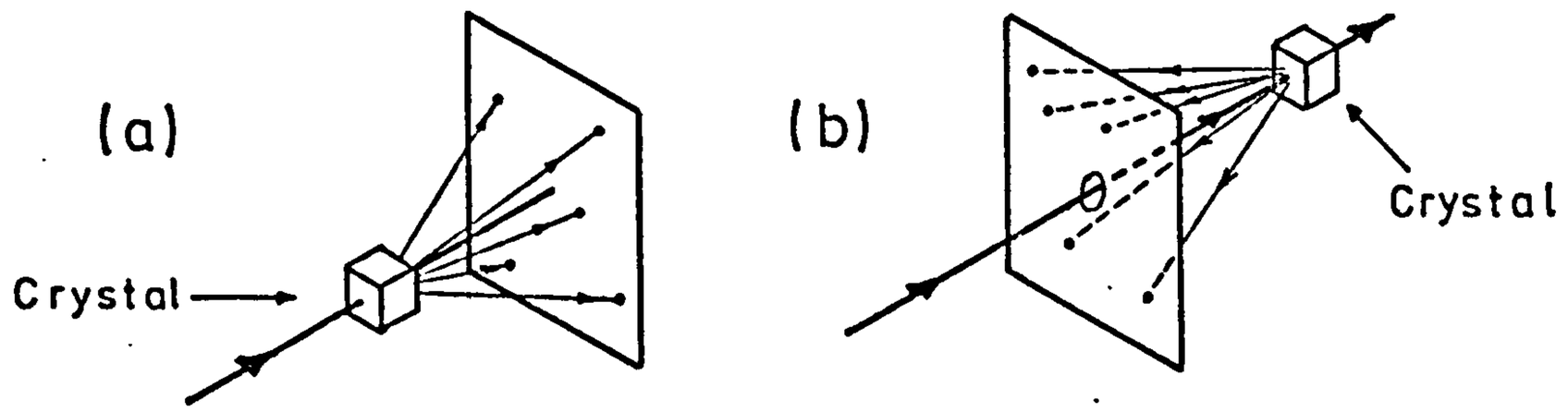


Fig 6.8 Laue methods: (a) transmission and (b) back-reflection [130]

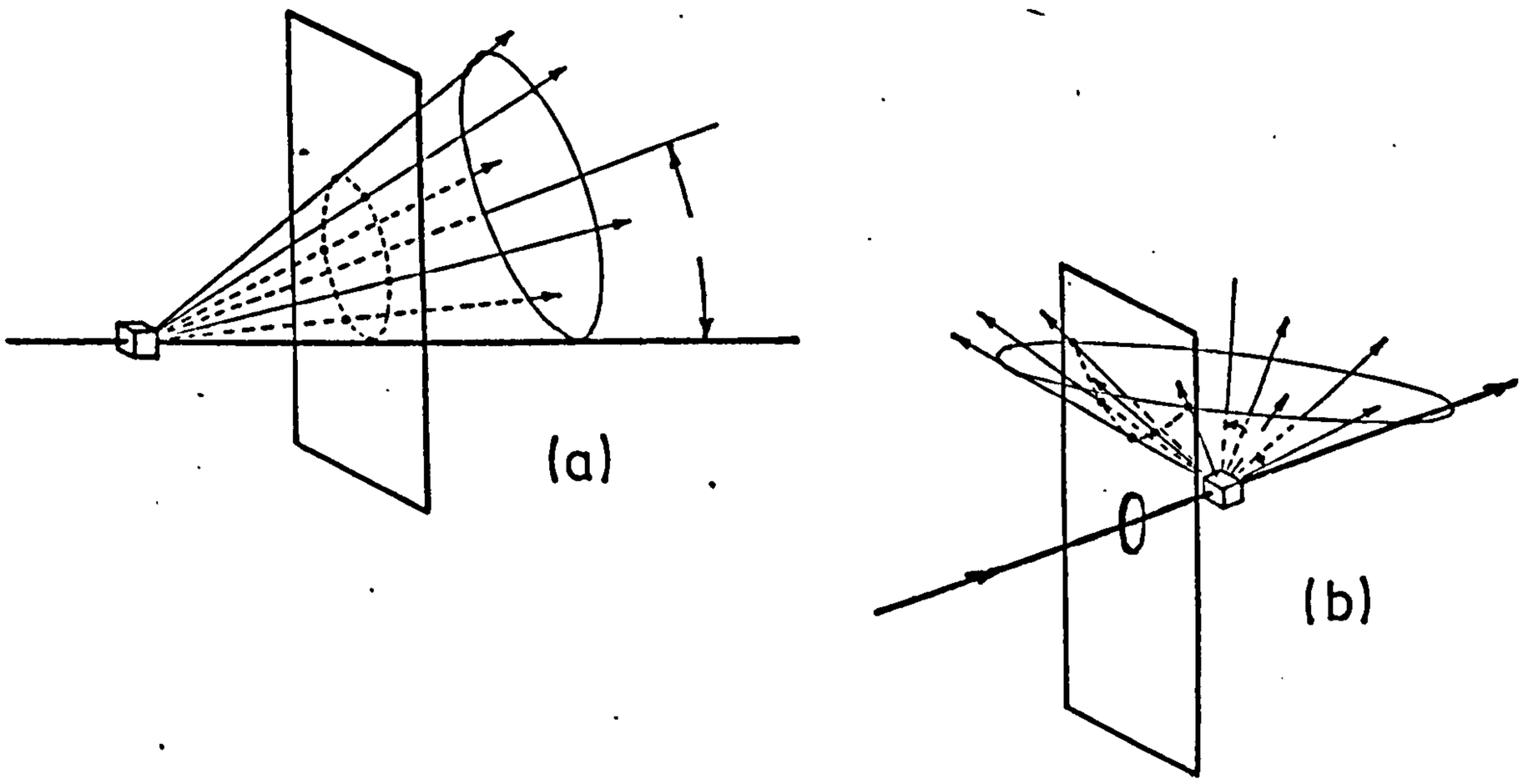


Fig 6.9 Location of Laue spots: (a) on ellipses in transmission and (b) on hyperbolas in back-reflection [130]

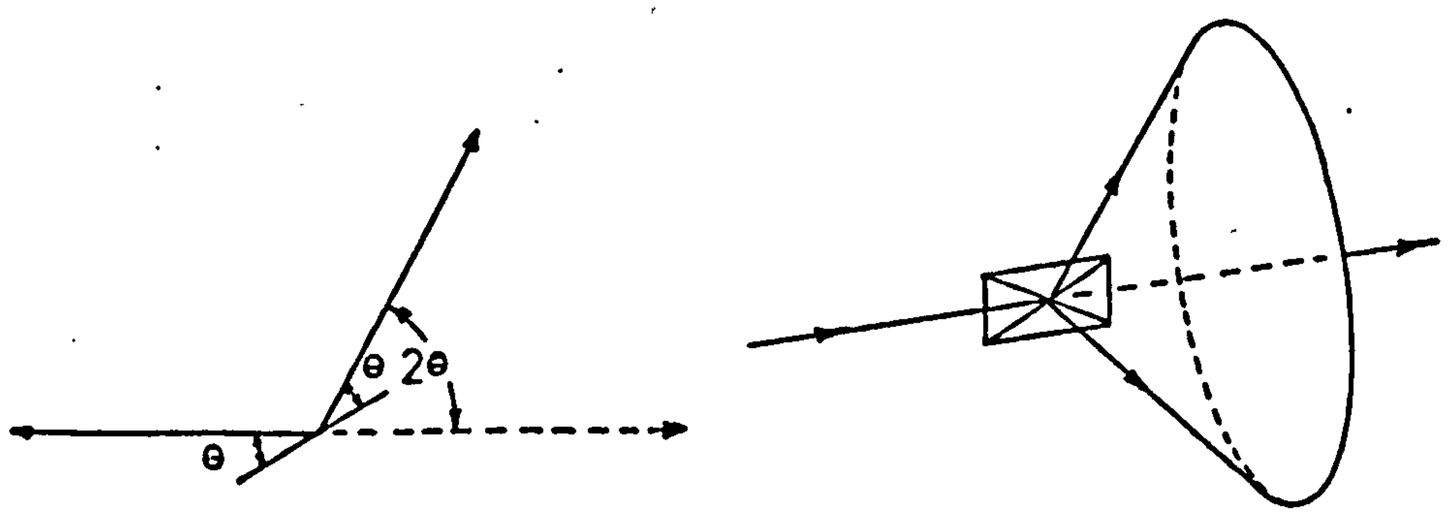


Fig 6.10 Formation of a diffracted cone of radiation in the powder method [130]

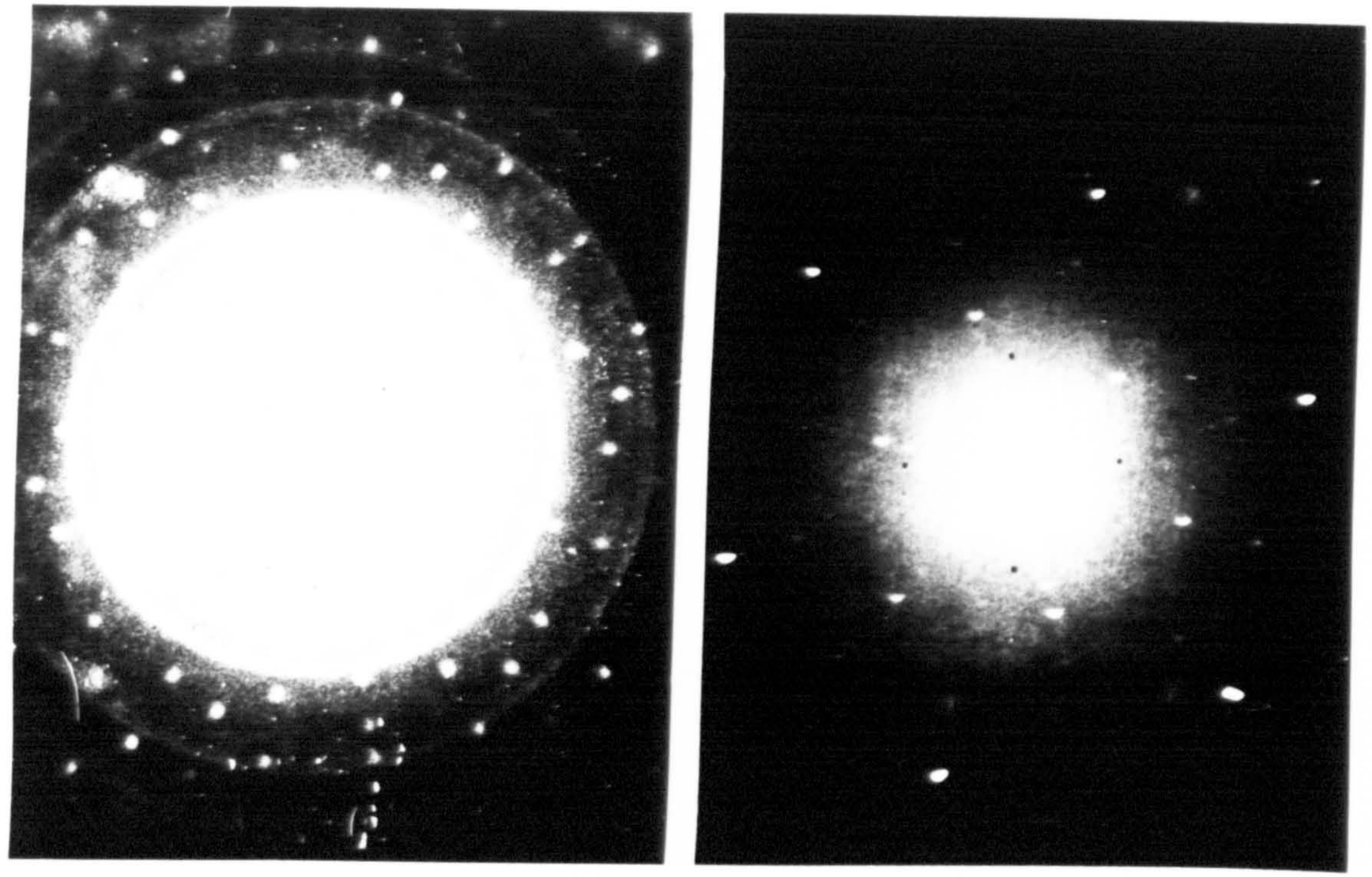
travel over the surface of a cone as shown in Figure 6.10(b), the axis of the cone coinciding with the transmitted beam. If the polycrystalline specimen has a preferred orientation, the diffracted rays comprise only segments of cones. Analysis of the results for the powder method is either by using film or a diffractometer.

6.3.3 Experimental Results

The powder method was used to find the orientation of the polycrystalline CdS films grown on (111) oriented Si. Using a diffractometer, only the (002) and (004) reflections were indicated by the trace of intensity versus Bragg angle 2θ. Because of the presence of only these two reflections, it was certain that the C-axis of the CdS was close to normal to the Si substrate.

Back reflection Laue was used to examine CdS films grown on Si substrates of both (100) and (111) orientation at three different growth temperatures, 200, 280, and 340°C respectively. It was found that polycrystalline films grew on thermally cleaned (100) oriented silicon over the above temperature range, in agreement with the results obtained using the transmission electron microscope.

A different result was found with (111) oriented silicon over the temperature range investigated. At 200°C a polycrystalline ring diffraction pattern was observed whereas somewhat distorted rings appeared at 280°C. At 340°C a spot diffraction pattern was observed, showing that at this temperature an epitaxial film of CdS had grown. Analysis of the symmetry of the diffraction pattern indicated that the epitaxial film was of the wurtzite structure. Photographs of the diffraction patterns for growth temperatures of 200°C and 340°C are shown in Figure 6.11. Further experiments were carried out to investigate the importance of the electron-beam cleaning



(a) Substrate temperature = 200°C. (b) Substrate temperature = 340°C.

Fig. 6.11 X-ray Laue photograph of Cd S film grown on (111) oriented Si. The silicon was electron beam cleaned.

of the silicon prior to film growth. Films were grown at temperatures up to 400°C (the deposition cut-off temperature) on (111) oriented silicon substrates which were not electron-beam cleaned. The films were polycrystalline, as shown by a ring diffraction pattern. A photograph of an X-ray Laue diffraction pattern at a growth temperature of 340°C on an uncleaned (111) oriented silicon substrate is shown in Figure 6.12. The results demonstrate clearly the important fact that it is possible to grow epitaxial CdS films on (111) oriented silicon substrates provided that the silicon is electron-beam cleaned before film growth and that the substrate temperature is in excess of about 300°C.

6.4 Hall Measurements

A measurement of the Hall voltage is a convenient method of measuring the impurity carrier concentration directly. As well as indicating which is the predominant impurity carrier from the sign of the Hall voltage, it is also possible to evaluate the Hall mobility. It must be emphasised that the Hall mobility μ_h differs from the drift mobility, μ_n or μ_p, by the factor r. The value of r depends on the scattering mechanism. Its value is 1.18 for phonon scattering and 1.93 for ionised impurity scattering. Impurity scattering is the more important mechanism when considering the case of films. It is to be expected that the mobility is sensitive to the perfection of the semiconductor material. Thus measurement of the Hall mobility should indicate changes in crystal structure as the silicon substrate temperature is increased.

It was advantageous to measure the Hall mobility of CdS films grown on silicon substrates directly, rather than to measure the Hall mobility of CdS films grown on a single crystal insulating substrate. In order to obtain a reasonable degree of isolation between film and substrate,

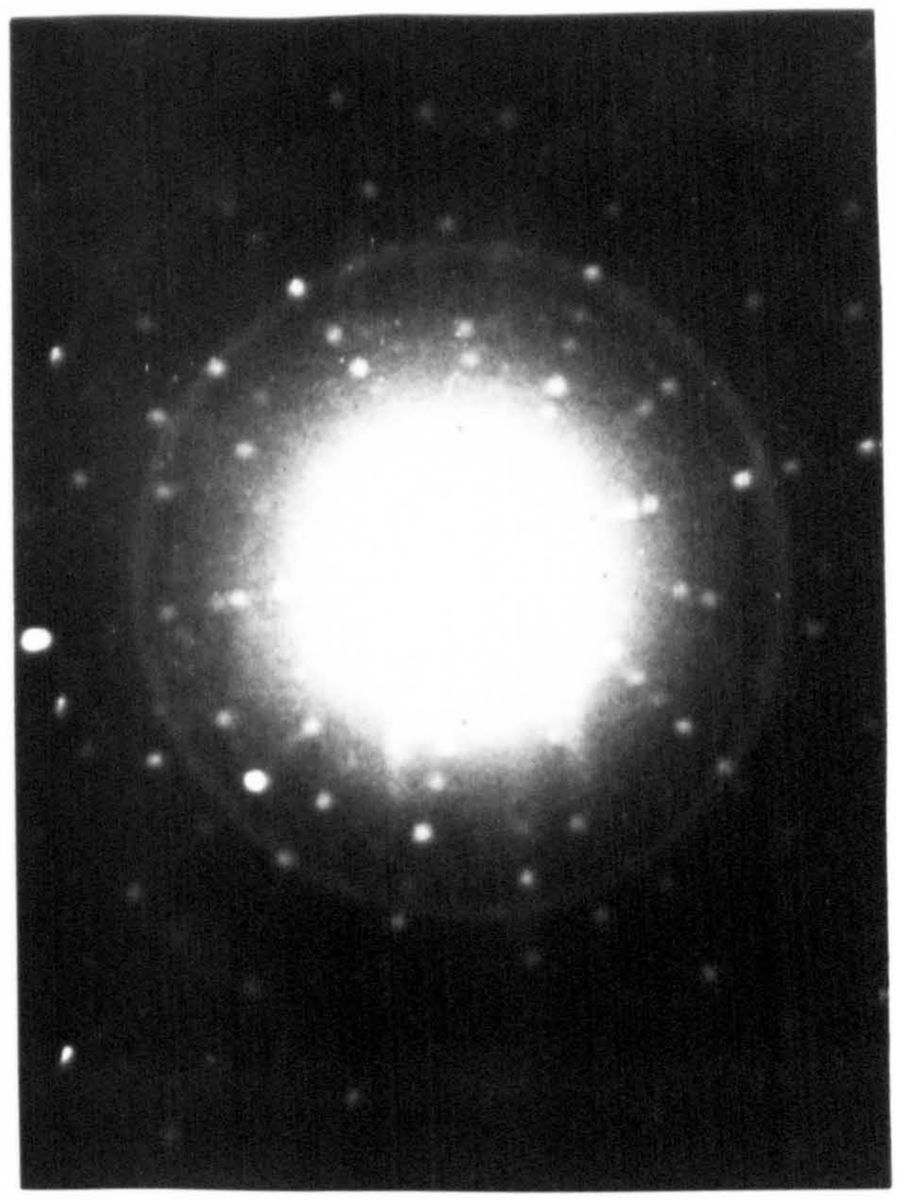
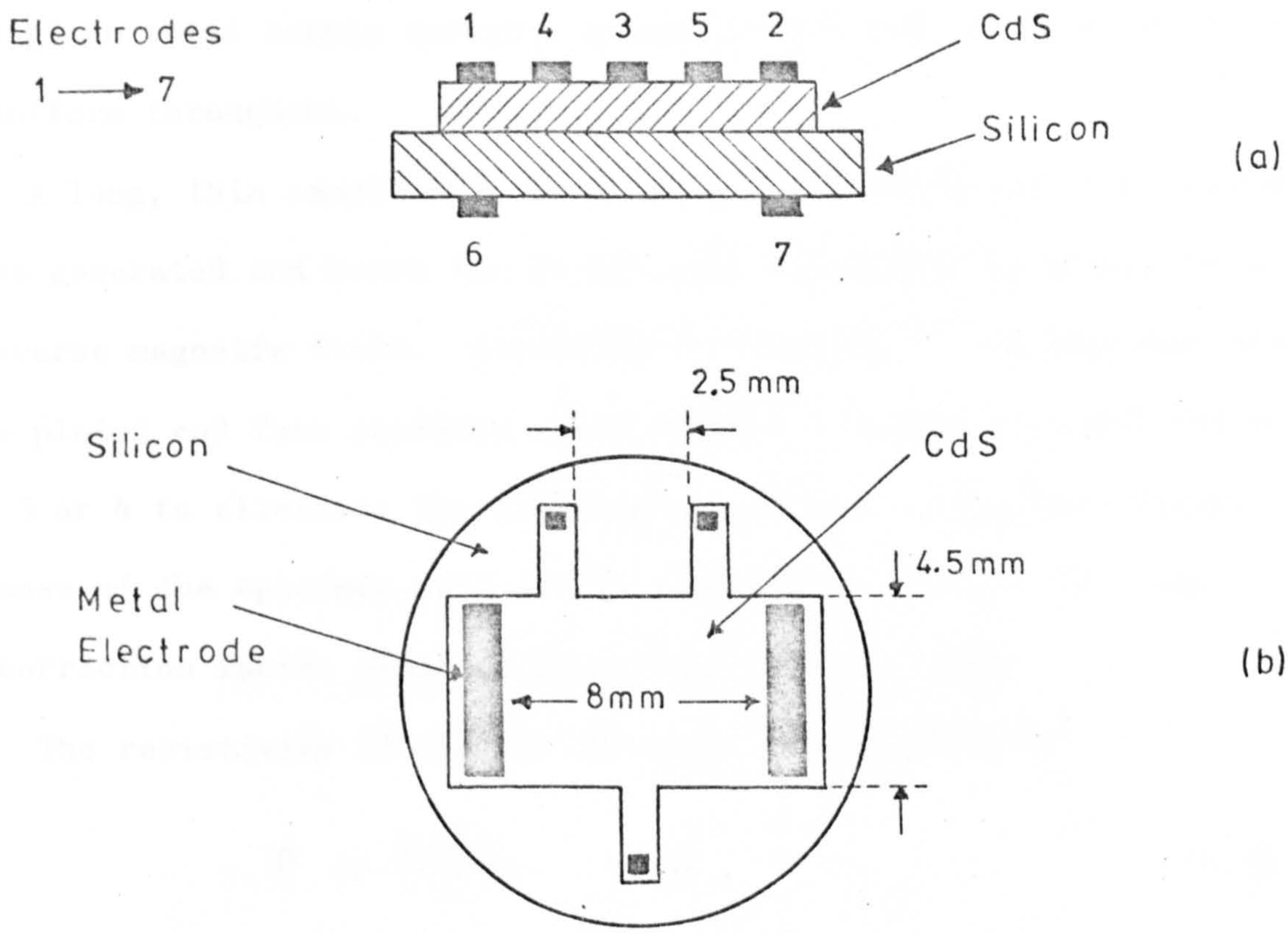


Fig. 6.12 X-ray Laue photograph of Cd S film grown on (111) oriented Si.
Substrate temperature = 340°C.
The silicon was not electron beam cleaned.

high resistivity p-type silicon was used ($> 3 \times 10^3 \Omega$-cm). The sign of the Hall voltage provided a convenient method of checking that the measured Hall mobilities were due to electrons in the n-type CdS rather than holes in the p-type silicon. Two different silicon orientations were used, (100) and (111), at several different substrate temperatures i.e. 200, 280, and 340°C. A schematic diagram showing the specimen geometry and the measuring system is shown in Figure 6.13. The amplifier, with unity gain, was a high input impedance ($> 10^{11} \Omega$) differential amplifier.

The measurement procedure was as follows:- The sample current was set by varying the dc supply voltages to obtain equal current readings on the two microammeters. A potentiometer was used to null the output of the amplifier. The specimen was then placed in the magnetic field and the Hall voltage measured. The experiment was repeated a number of times to obtain an average reading as the null point tended to drift with time. Throughout the experiment the sample was kept in the dark to avoid any majority carrier injection, which would have complicated the analysis of the results. The film resistivity was obtained by measuring the voltage across limbs 4 and 5 while applying a voltage across contacts 1 and 2. This method avoids the problems of contact resistance since no current flows externally between limbs 4 and 5 because a high impedance voltmeter was used. Both the CdS Hall effect and the metal electrode pattern were obtained using a mechanical mask. Since it was appreciated that there was a possibility of current flow in the substrate, contacts 6 and 7 were placed on the underside of the silicon, in the same relative position and of the same dimensions as electrodes 1 and 2 shown in Figure 6.13(a). Since the silicon resistivity was known from a four point probe measurement[99], it was possible to calculate the current flowing in the silicon substrate for a given total sample current by measuring the voltage across the electrodes placed on the underside of the silicon. From this



Hall Specimen : (a) Cross-Section and (b) Plan View

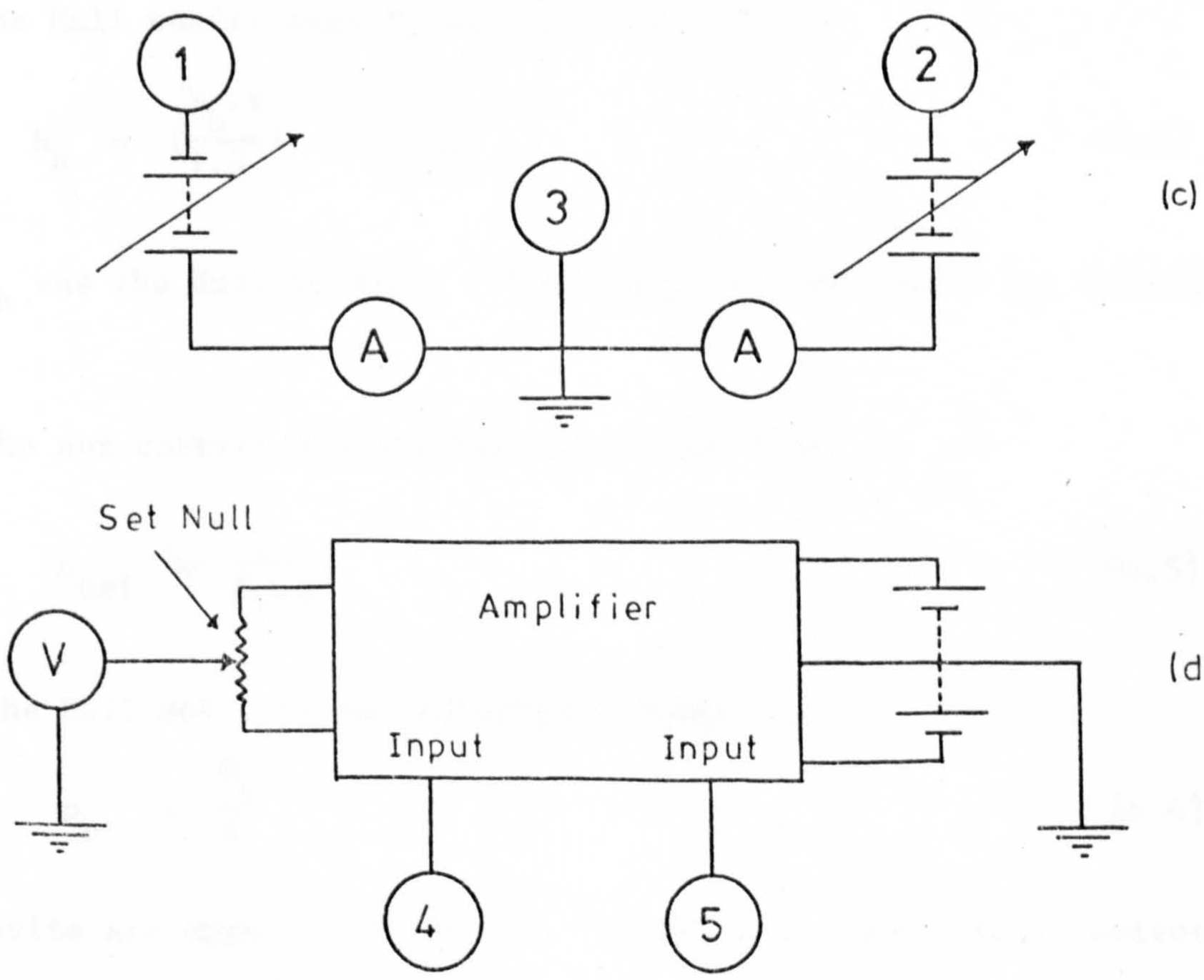


Fig 6.13 Hall measurement system

measurement, it was possible to calculate the current in the CdS film, for a given total sample current, assuming that the CdS film resistivity was uniform throughout.

A long, thin sample must be used so that the full dc Hall field can be generated and hence the dc mobility can remain unaltered by a transverse magnetic field. According to Isenberg[131] a specimen with large plated end face contacts would require a length to width ratio greater than 3 or 4 to eliminate the shorting-out effect on the Hall field. In the case of the specimen used in the experiment the L/W ratio was 1.78. The correction factor obtained from Fig. 6.14 was 0.88.

The resistivity of the CdS film was calculated from

$$\rho = \frac{R.W.t}{L} \qquad (6.3)$$

where R was the resistance of the film, W was the width of the film, t the thickness of the film and L the length of the specimen.

The Hall coefficient R_h was calculated from

$$R_h = \left(\frac{V_h.t}{I.B.}\right) \times \left(\frac{1}{0.88}\right) \qquad (6.4)$$

where V_h was the Hall voltage, I the simple current and B the magnetic field.

The net carrier density was calculated from:

$$n_{net} = \frac{r}{R_h.q} \qquad (6.5)$$

The Hall mobility was calculated from:

$$\mu_h = \frac{R_h}{\rho} \qquad (6.6)$$

The results are shown in Table 6.1. In the case of the (111) oriented silicon, the Hall mobility increases with increasing substrate temperature.

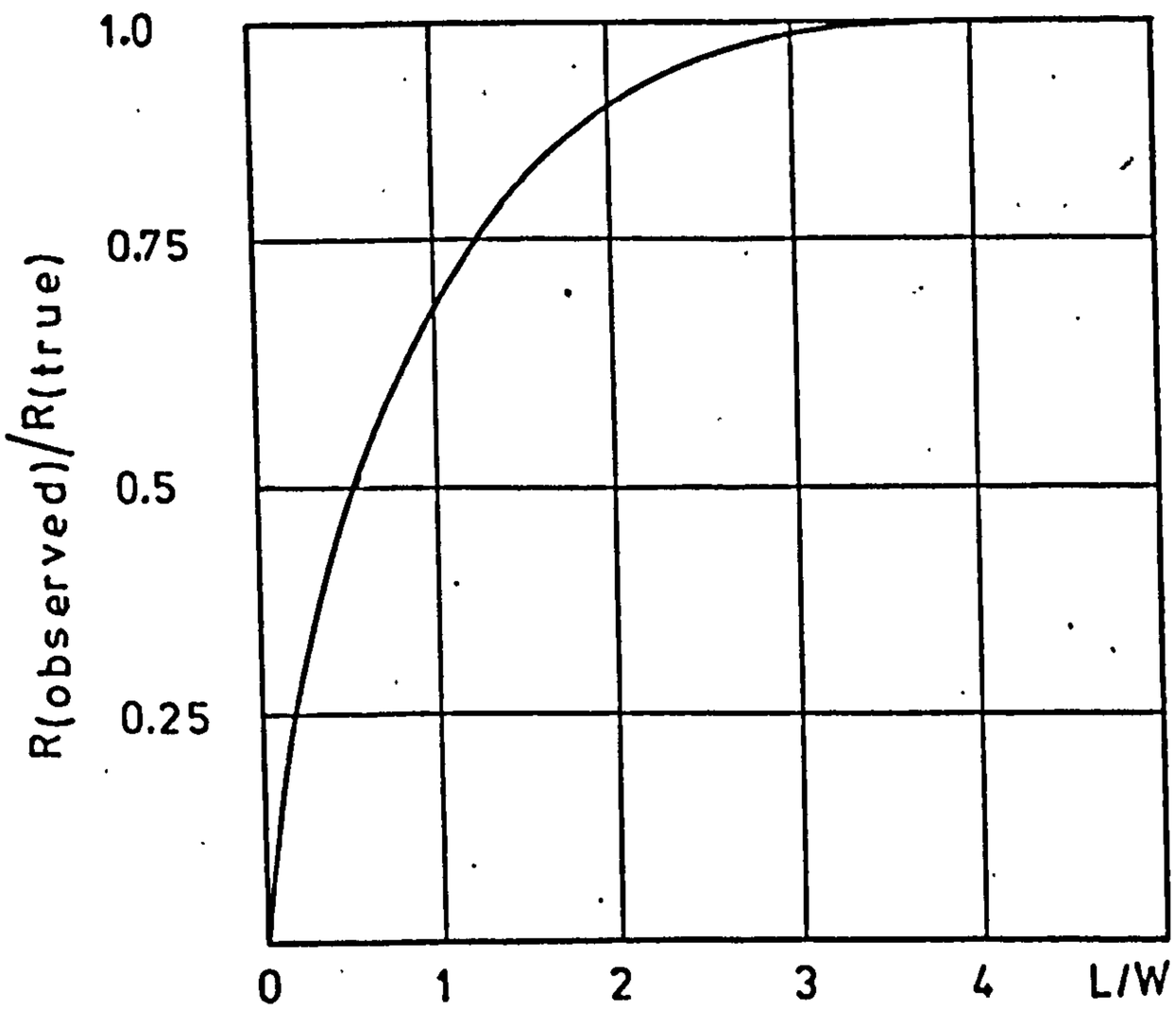


Fig 6.14 Correction factor for R_h for different L/W ratios (131)

PARAMETER	UNITS	(100) 200°C	(100) 280°C	(100) 340°C	(111) 200°C	(111) 280°C	(111) 340°C
FILM THICKNESS	m	3.5×10^{-6}	1.6×10^{-6}	4×10^{-6}	4×10^{-6}	1.1×10^{-6}	1.2×10^{-6}
ρ (CdS)	Ω-cm	1.45×10^{2}	3.2×10^{2}	2.7×10^{1}	1.9×10^{1}	1.1×10^{1}	2×10^{1}
R_h	cm^3/coul	8.5×10^{-3}	7.4×10^{-3}	2.3×10^{-3}	2.2×10^{-3}	2.5×10^{-3}	6.3×10^{-3}
n_{net}	cm^{-3}	7.3×10^{14}	8.4×10^{14}	2.7×10^{15}	2.9×10^{15}	2.5×10^{15}	9.9×10^{14}
μ_h	cm^2/V-sec	60	25	85	115	235	315

Table 6.1 Hall Measurement Results (AT ROOM TEMPERATURE)

On the other hand the mobilities for (100) oriented silicon decrease from 60 cm^2/V-sec at 200°C to 25 cm^2/V-sec at 280°C and then increase to 85 cm^2/V-sec at 340°C. A further experiment indicated that the reason for this behaviour was a thickness factor, as a 4 μm thick CdS film, grown on (100) oriented silicon at 280°C, had a mobility of 60 cm^2/V-sec. These two sets of results (one set for (100), one set for (111)) should be viewed in the light of the transmission electron diffraction and the X-ray diffraction results. In the case of (100) oriented silicon, there was no appreciable improvement in the diffraction patterns for both X-ray and T.E.M. analyses. In other words, both diffraction techniques showed that a polycrystalline CdS film was present which did not show any preferred orientations as the substrate temperature was increased. In the case of (111) oriented silicon, however, the X-ray diffraction pattern showed a steady improvement until oriented growth was obtained at around 340°C.

A further experiment was carried out as a check on the measured resistivity values. The current-voltage characteristics were measured across electrodes 1 and 2 (shown in Figure 6.13(a)) and the measurement repeated after the film had been removed. The change in sample current at a fixed voltage, was used to calculate the resistivity from the geometry of the specimen. An estimated value of film resistivity of approximately $10^4 \Omega$-cm was obtained using this method. This suggested that the current through the CdS film was lower than the calculated value, making allowance for current through the silicon substrate in the previous set of experiments. However, this does not alter the validity of the Hall mobility results, since $\mu_h = R_h/\rho$ and the CdS film current were the same when both the resistivity ρ and Hall coefficient R_h were calculated. The increased CdS film resistivity implies that the net carrier density is approximately 7×10^{12} cm^{-3} for the (100) oriented silicon and approximately 2×10^{12} cm^{-3}

for the (111) oriented silicon at a growth temperature of 340°C.

It might be expected that the *film mobility* μ_f would be less than the bulk mobility μ_b because of scattering by the boundary surfaces in addition to the normal bulk scattering. Chopra[44] gives an expression relating μ_f and μ_b:

$$\mu_f = \frac{\mu_b}{1 + 1/t} \tag{6.7}$$

where l is the mean free path and t is the film thickness. Chopra also gives the expression for the mean free path l as:

$$l = \mu_b \frac{h}{q} \left(\frac{3}{8\pi} n_b\right)^{\frac{1}{3}} \tag{6.8}$$

where q is a unit electronic charge, h is Planck's constant and n_b is the net carrier density in the bulk.

Taking μ_b = 200 cm^2/V-sec, $n_b = 10^{15}$ cm^{-3} and t = 2 microns the mean free path l is 8Å which means that $\mu_f \simeq \mu_b$.

Some of the drift mobilities μ_d quoted for single-crystal CdS are 240 Spear[132], 300 Sze[87c], 340 Milnes[133], and 400 cm^2/V-sec Piper.[134] It is not possible to estimate the drift mobility with confidence, from the Hall mobility in this work, because of the presence of traps in the CdS film. Evidence of traps was found from the experimental results presented in Chapter 7.

6.5 Conclusions

X-ray and transmission electron diffraction have shown that CdS films grown on (100) oriented silicon in the temperature range 100-400°C are polycrystalline. It was found, using X-ray diffraction, that epitaxial films of CdS grew on electron-beam cleaned (111) oriented silicon at temperatures in excess of 300°C. It was further found that polycrystalline

films grew on (111) oriented silicon, in the epitaxial temperature range (300-400°C), if it was not electron-beam cleaned prior to the CdS film growth. The Hall mobility of the CdS films increased from 115 cm^2/V-sec at T_s 200°C to 315 cm^2/V-sec at T_s 340°C for films grown on (111) oriented silicon. On the other hand, the Hall mobility of CdS films grown on (100) oriented silicon were significantly lower, i.e. 85 cm^2/V-sec at T_s 340°C.

* $T_s \equiv$ SUBSTRATE TEMPERATURE DURING CdS FILM GROWTH

CHAPTER 7 EXPERIMENTAL RESULTS

7.1. Introduction

The experimental measurements of photo-characteristics, I-V characteristics and C-V characteristics are presented in this chapter. In general, epitaxial CdS films were used as described in the previous chapter. These measurements were carried out on nCdS-pSi heterojunctions fabricated on (111) oriented silicon substrates over a range of p-type doping levels namely 6×10^{12}, 6×10^{13}, 3×10^{15} and 3×10^{17} cm^{-3}. The results of these measurements have then been used to determine the barrier potentials appropriate to the particular diode and correlated with the theory and band models presented in Chapter 3.

Results obtained from heterojunctions with substrates which were not thermally cleaned are also presented. There is a great deal of experimental evidence to indicate that polycrystalline CdS films grow on (111) oriented silicon which has not been thermally cleaned (Chapter 6). It is worthwhile comparing the measurements of devices fabricated from both uncleaned and cleaned silicon substrates. In this way it is possible to ascertain the role of both polycrystallinity in the CdS films and the role of surface contamination.

7.2 EXPERIMENTAL TECHNIQUES AND METHODS

7.2.1 I-V Measurements

Current-voltage measurements were made both by using an X-Y chart recorder and by using an ammeter and a high impedance voltmeter for the lower current ranges.

If the I-V measurements are plotted as $Log_e(I)$ versus bias voltage then it is possible to calculate J_s (from a measurement of I_s and knowledge of the junction area) and n, the parameters described by equation 3.40

shown below:

$$J = J_s \exp\left(\frac{qV}{nKT}\right) \qquad (3.40)$$

Measurements of the forward bias I-V characteristic are used to estimate J_s and n, since edge leakage current effects tend to dominate in reverse bias. A typical set of data has been plotted in the manner discussed above, for an nCdS-pSi heterojunction with a silicon doping level of 6×10^{13} cm^{-3}, and is illustrated in Figure 7.1. The value of the parameter n may be calculated from the slope of the straight line portion of the characteristic which is equal to (q/nKT). The extrapolated value of current at zero bias gives the saturation current I_s and hence the saturation current density J_s. As Figure 7.1 shows, in a practical situation the I-V characteristic does not follow an exponential law throughout the voltage range. This is because recombination dominates at low bias; while, at higher bias, drift currents and series resistance effects must be considered.

7.2.2 Photocurrent—Voltage measurements

Photocurrent-voltage measurements were carried out using a conventional optical system, consisting of a Xenon lamp, a variable neutral density filter, a range of filters from 450 nm to 1155 nm and a slotted disc driven by a d.c. motor to "chop" the light. The motor speed could be varied to produce a chopping frequency over the range, 200 to 1000 Hz, with stabilised speed control of the motor throughout. Optical power was measured using a Hilger-Watts FT4 thermopile. The main advantage of a thermopile is that its response is independent of the optical wavelength over a large range (with the glass window fitted the response was flat over the range 0.3 to 2.8 μm). On the other hand, its bandwidth

$N_A = 6 \times 10^{13}\ cm^{-3}$

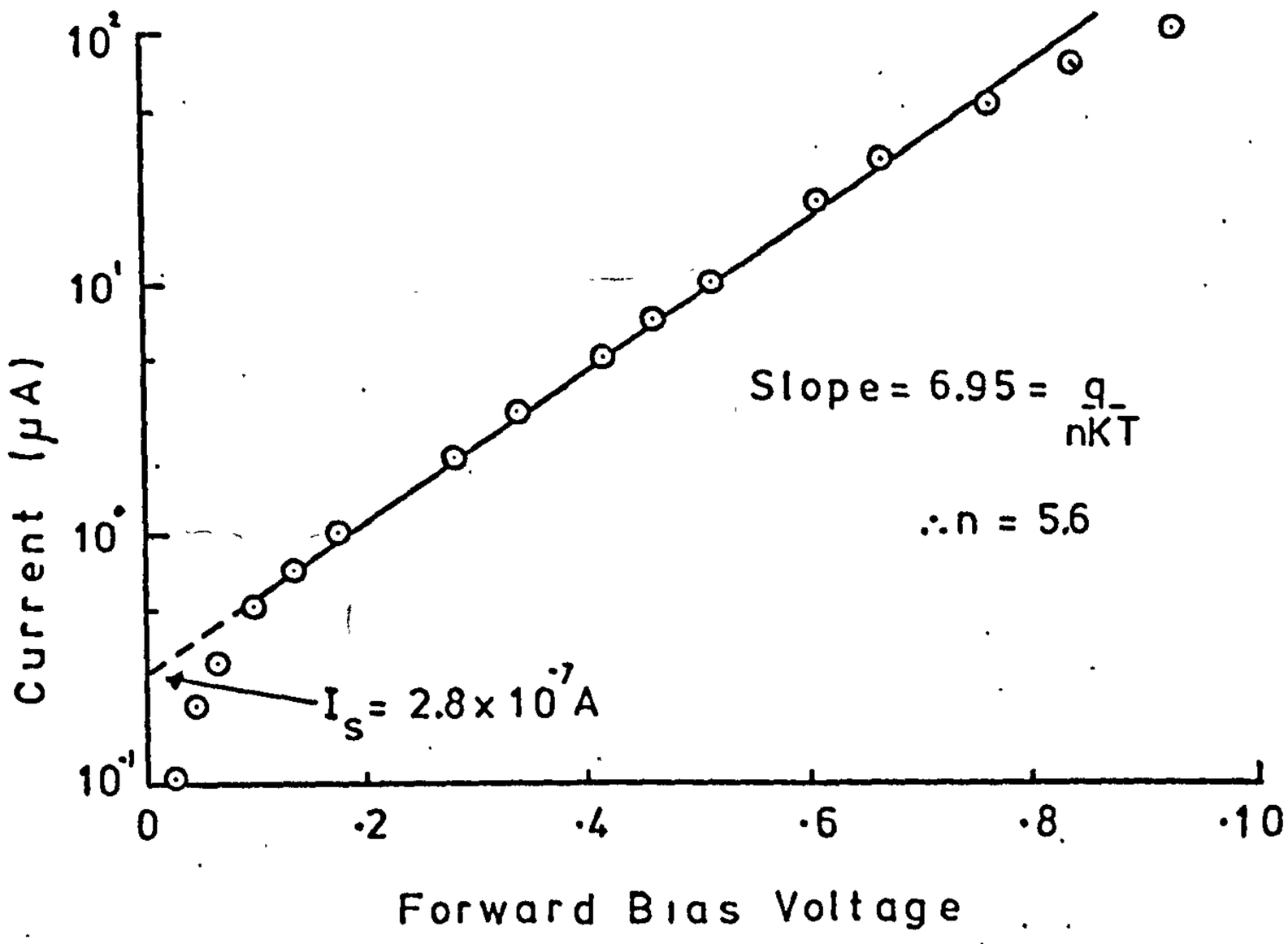


Fig 7.1 $Log_e(I)$ Versus Forward Bias Voltage

$N_A = 6 \times 10^{13}\ cm^{-3}$

$R_s = 2.2 \times 10^{3}\ \Omega$

Junction Area = $8 \times 10^{-3}\ cm^2$

$I_{sc} = 2.7 \times 10^{-5}\ A$

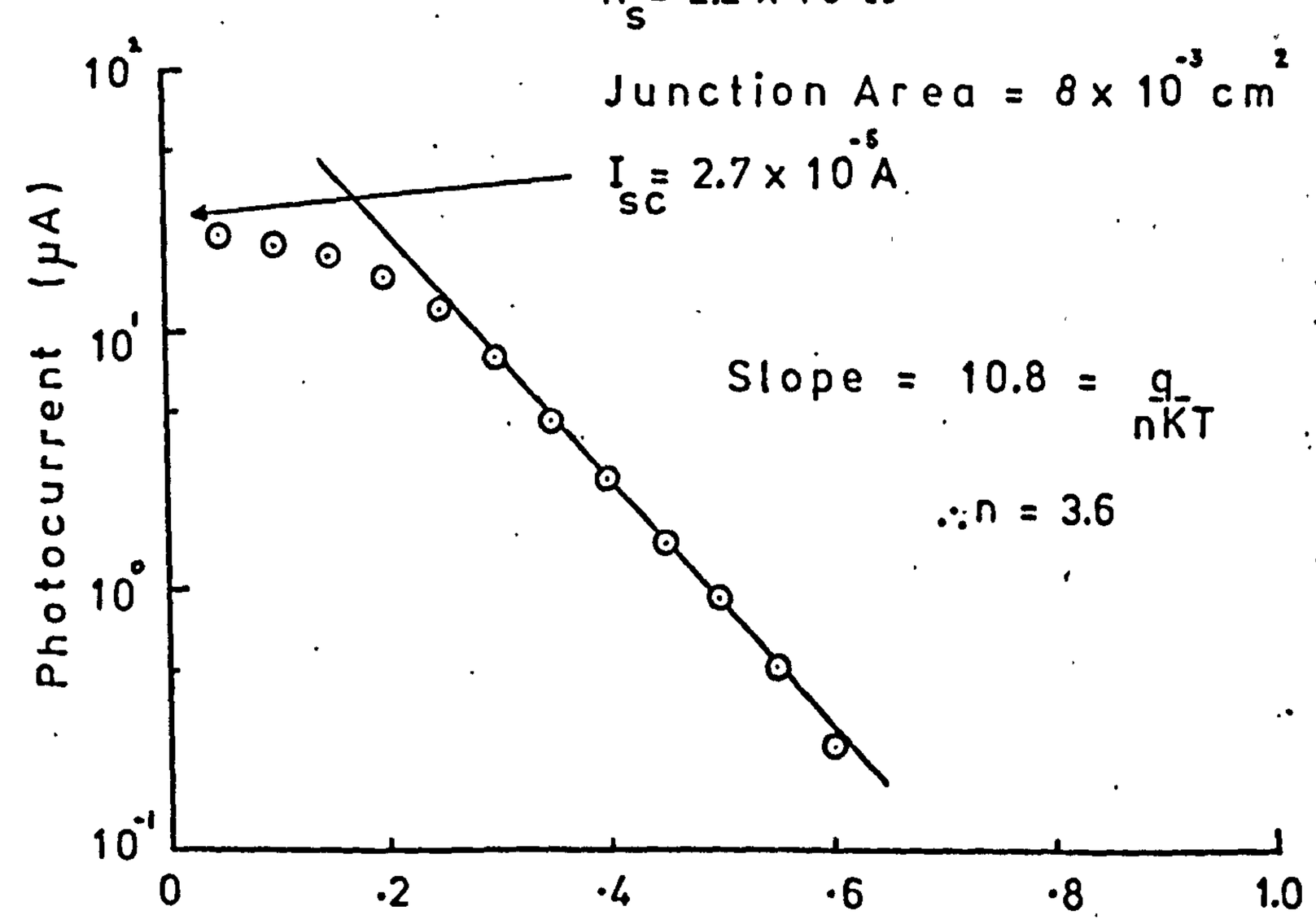


Fig 7.2 $Log_e(I_{ph})$ Versus Bias Voltage

is limited to about 200 Hz and the signal output level is only 1.2 μV/μW.

A modified form of equation 3.35 is used to calculate the saturation current I_s, hence J_s; and then the barrier potential is calculated from equation 3.16. Equations 3.35 and 3.16 are given below:

$$V_{OC} = \frac{KT}{q} \cdot \text{Ln} \left(\frac{I_L}{I_s} + 1\right) \qquad (3.35)$$

and

$$J_{SB} = AT^2 \exp \left(\frac{-q\phi}{KT}\right) \qquad (3.16)$$

The modified form of equation 3.35 which includes the factor n obtained from the photocurrent (I_{ph})-voltage characteristic and a factor which allows for the series resistance of the silicon substrate is:

$$I_{sc} = I_s \left[\exp \left(\frac{qV_{oc}}{nKT}\right) \exp - \left(\frac{qI_{sc}R_s}{KT}\right) - 1 \right] \qquad (7.1)$$

where I_{sc} is the short circuit photocurrent, V_{OC} is the open circuit photovoltage and R_s is the series resistance of the silicon substrate. The extrapolated value of bias voltage for zero photocurrent gives V_{OC} and the maximum value of photocurrent gives I_{sc}. Figure 7.2 shows how the factor n is obtained from the slope of the $\text{Log}_e (I_{ph})$ versus bias voltage characteristic. The calculated value of J_s from the optical measurement is then used to calculate the barrier potential using equation 3.16.

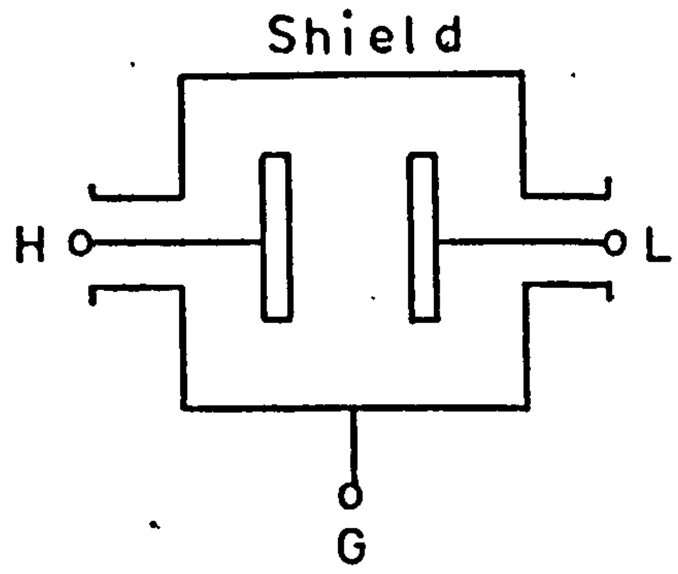
7.2.3 C-V measurements

A standard capacitance bridge, General Radio type G.R 1615-A, together with a low distortion signal generator and tuned detector was used to measure capacitance versus voltage. Readings were taken of dissipation factor D and series capacitance C_s. It was quite simple to calculate the parallel capacitance C_p from knowledge of D and C_s

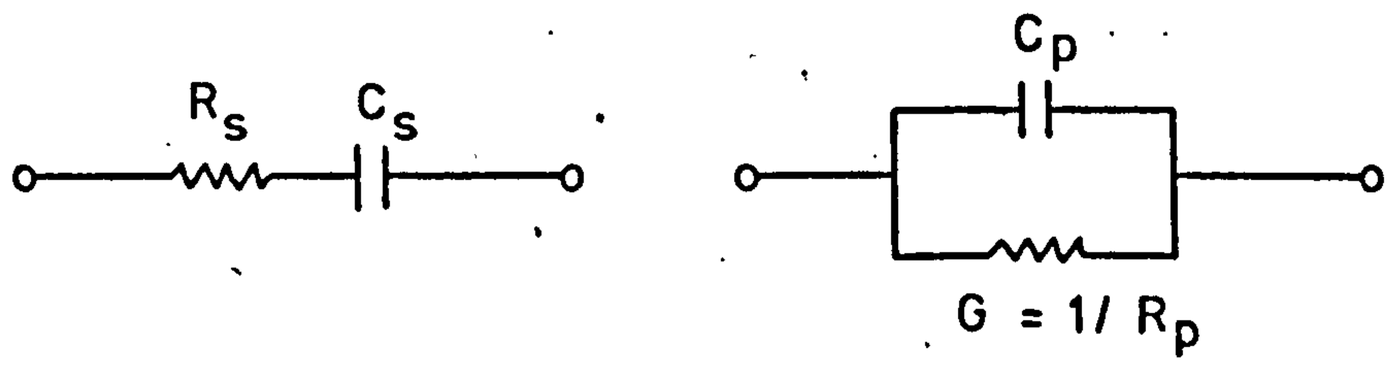
as shown in Figure 7.3 The capacitance bridge was used in the three term mode so that all capacitances to the shields or to ground are excluded from the direct capacitance, between the terminals 'H' and 'L', measured by the bridge. As the upper frequency limit of the capacitance bridge was 400 KHz, a Hewlett Packard type 4815A R.F. Vector Impedance Meter was used for measurements over the range 500 KHz to 30 MHz. The Vector Impedance Meter gave the modulus and phase angle of the impedance of the diode from which it was possible to calculate the capacitance. To minimise the effects of stray capacitance at the higher frequencies, the Vector Impedance Meter was connected directly using contacts soldered to the printed circuit board to which the heterojunction diodes were, in turn, connected via thermal compression bonded gold wires.

7.2.4 Response to pulsed optical input

It was only possible to make this measurement on the more sensitive photodetectors because of noise problems. A GaAs light emitting diode (L.E.D.) with a 50 ns rise time and a wavelength of 904 nm, was driven by a Hewlett Packard type 214A pulse generator. The L.E.D. was mounted in an assembly which had an input impedance of 50 Ω. The pulse generator, with its 50 Ω output impedance, was capable of delivering pulses of up to one ampere to the L.E.D. The heterojunction photodetector was also terminated in a 50 Ω load. A Tektronix type 531A oscilloscope was used to measure the rise and fall times of the optical pulse. A Hewlett-Packard type 5082-4220 p-i-n photodiode, with a rise time of less than 1 ns when operated in the photoconductive mode with a 50 Ω load resistor, was used to verify that the rise and fall times of the optical pulses were less than 100 ns.



(a) Diagram of 3-Terminal Capacitor



(b) Series Parallel

(c) Equations Relating R_s, R_p, C_s and C_p

(i) $D = \omega R_s C_s = G/\omega C_p = 1/\omega R_p C_p$

(ii) $C_s = C_p (1 + D^2)$

(iii) $G = 1/R_p = \omega C_s D/(1 + D^2) \simeq \omega C_s D$

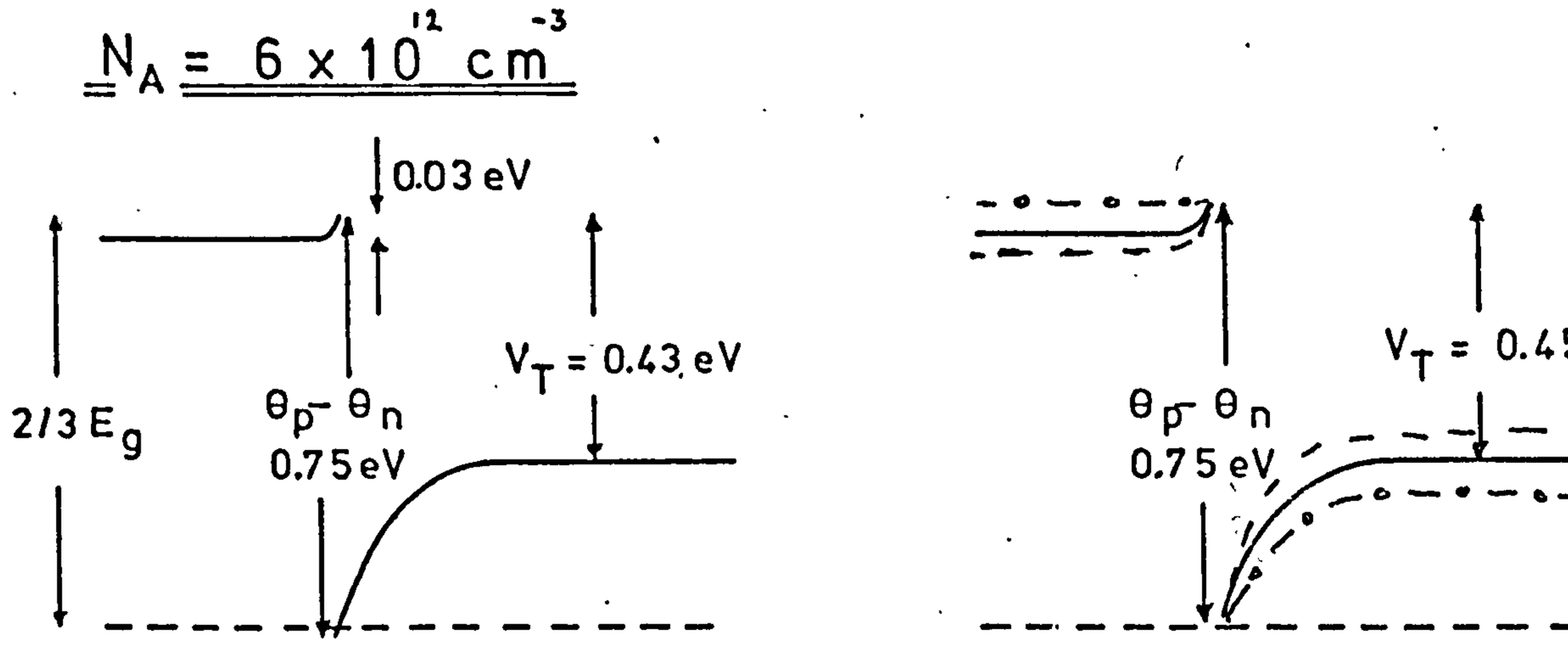
(iv) $R = G/[(\omega C_p)^2 (1 + D^2)] \simeq G/(\omega C_p)^2$

Fig 7.3

7.3 EXPERIMENTAL RESULTS

7.3.1 Case 1 $N_A = 6 \times 10^{12}$ cm^{-3}

The band structure for this Si doping is shown in Figure 7.4(a) and 7.4(b), where 7.4(a) includes the effect of surface states while 7.4(b) neglects surface states. Both the CdS and Si junction are regions of accumulation. In this particular case there is very little difference between the model with surface states and the model without i.e. a 0.02eV difference in the potential barrier. The I-V characteristics are shown in Figure 7.5 with two different current scales to emphasise the difference between the forward and reverse I-V characteristics more clearly. The reverse I-V characteristic is very "soft" while the forward characteristic requires moderate voltages for turn-on. If one were to consider the I-V characteristic on its own the immediate conclusion would be that this was a poor diode. However, the model shows that the Si junction is an accumulation region and this accumulation region is enhanced by increasing reverse bias. One might expect that in forward bias the Si enhancement would be reduced and so the current would be lower than in reverse bias. This is the situation observed from Figure 7.5 and the increase in current at higher voltages is a result of the reduction in the barrier potential in forward bias. When the I-V characteristics are plotted as $\mathrm{Log}_e(I)$ versus bias voltage, it is found that there are three different regimes namely an exponential characteristic from .01 μA to 1 μA (a bias range of 0.04 to 0.2 volts) with n = 1.2, an exponential characteristic from 1 μA to 10 μA (a bias range of 0.2 to 0.36 volts) with n = 2.8, and non-exponential characteristics at still higher currents. As mentioned in Chapter 3, n = 1 indicates that the diffusion current dominates while n = 2 holds when the recombination current dominates. It is clear that other effects in addition to recombination are important in the region



(a) Surface States
(b) No Surface States

Fig 7.4 Band Diagram

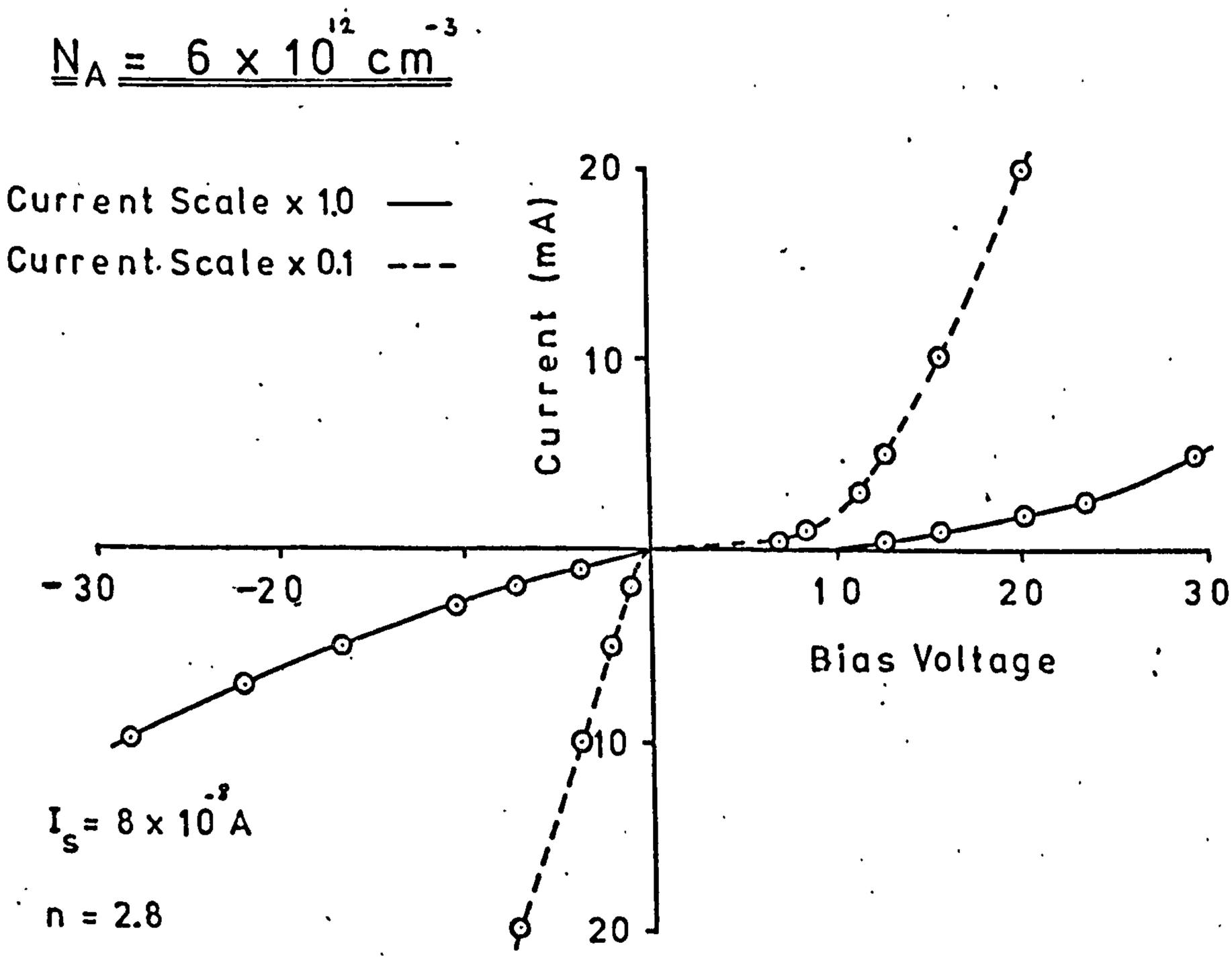


Fig 7.5 I-V Characteristic

where n = 2.8, for example trapping effects in the CdS film and series resistance effects due to the high resistivity of both CdS film and Si substrate. Although the forward I-V characteristic should normally be used to obtain n, and the saturation current I_s, for reasons outlined at the beginning of the chapter, the reverse I-V characteristic was used here because for this Si doping,reverse bias is equivalent to forward bias found in a normal diode i.e. the roles of forward and reverse bias are interchanged.

The photo characteristics are shown in Figure 7.6. The important feature to note is that the photodiode requires forward bias to increase the sensitivity, implying that forward bias widens the depletion region (reduces the accumulation region) in the silicon. This behaviour is qualitatively in agreement with both the band model and the I-V characteristics The quantum efficiency at 600 nm, is around 25% at 1.0 volts bias, rising to 32% at 5.0 volts forward bias. The open circuit voltage V_{OC}, was 0.49 volts, the short circuit photocurrent I_{sc}, was 2.6×10^{-5}A and n was 4.6. The fact that n was again significantly different from the value of 2 for recombination indicates that more complicated processes are occurring, for example trapping at a number of different energy levels. The barrier potential was calculated to be 0.27 eV using the measured parameters and equation 7.1. This is in reasonable agreement with the theoretical value of 0.43 eV calculated on the assumption that the Fermi level in the CdS film is 0.3 eV below the conduction band and that the conduction band of the silicon is "pinned" at $\frac{2}{3}$ Eg above the Fermi level in the Si. The quantum efficiency of 32% at 600 nm compares reasonably well with the 38% quantum efficiency quoted for the Hewlett-Packard p-i-n photodiode with the same load and at the same wavelength.

The capacitance versus voltage characteristics are shown in Figure 7.7 for both the series capacitance C_s, and the parallel capacitance C_p,

$\underline{\underline{N_A = 6 \times 10^{12}\ cm^{-3}}}$

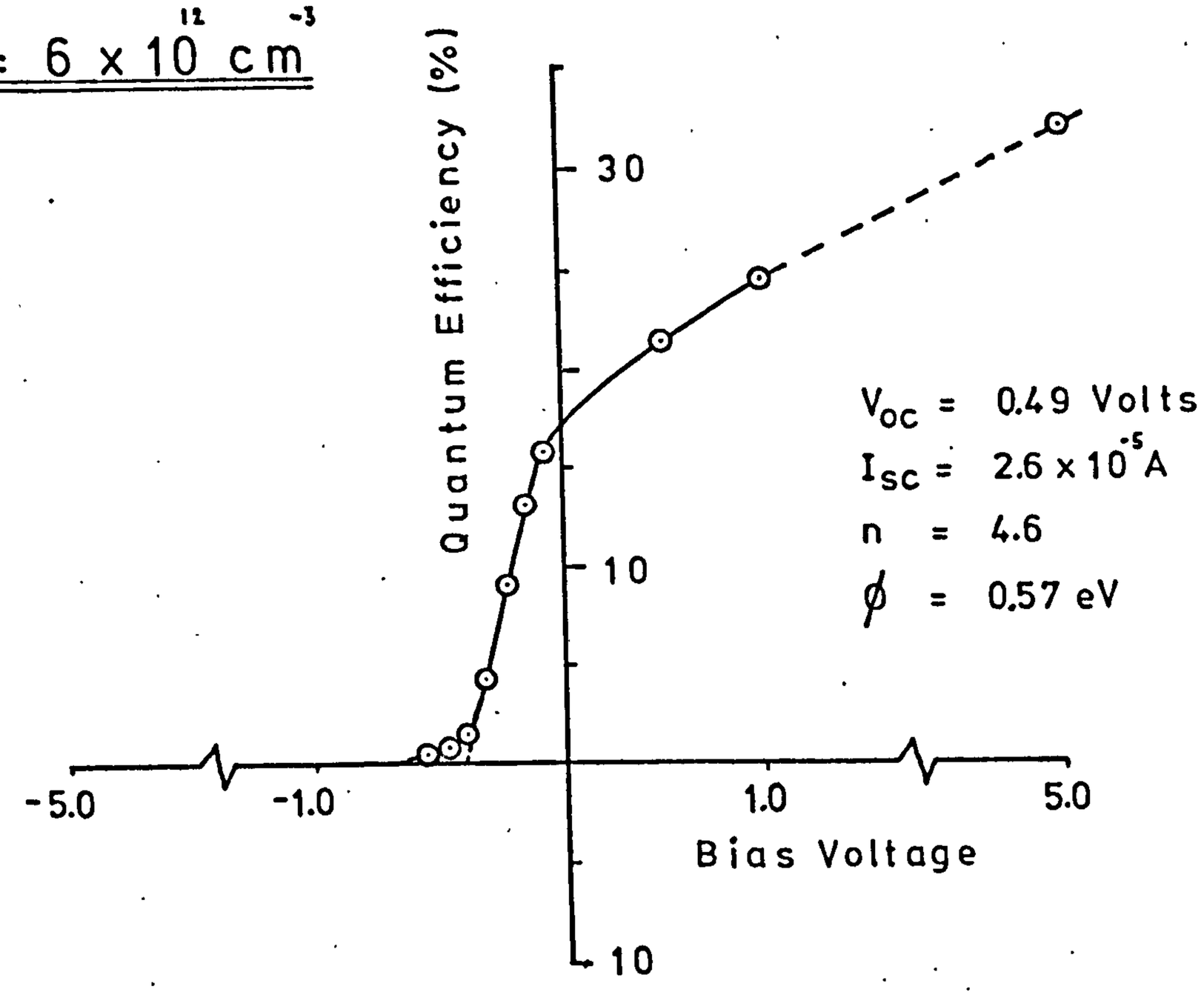
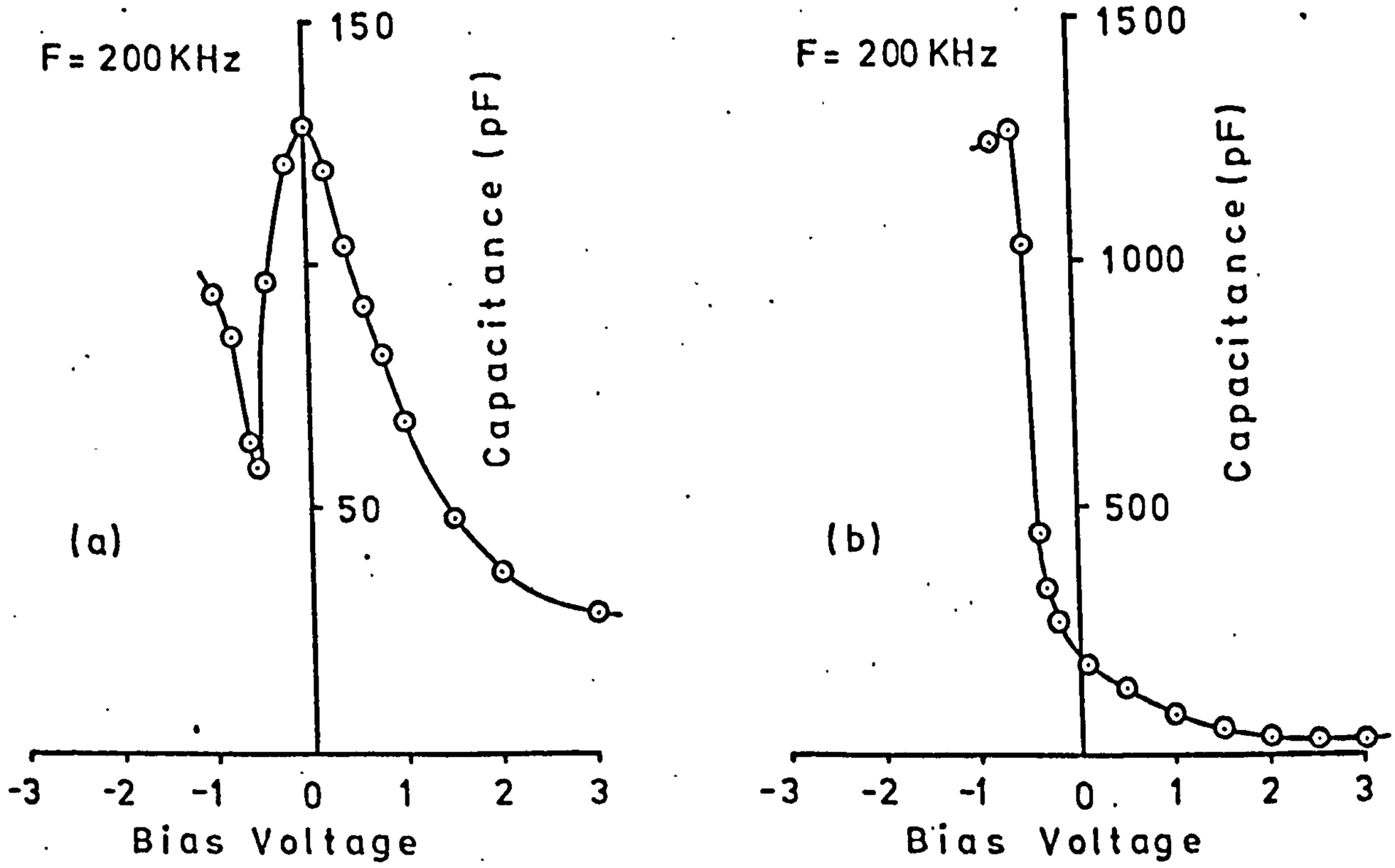


Fig 7.6 Photo Characteristic

$\underline{\underline{N_A = 6 \times 10^{12}\ cm^{-3}}}$



(a) Parallel Capacitance (b) Series Capacitance

Fig 7.7 Capacitance Voltage Characteristic

at 200 kHz. It was thought that since devices of this doping (N_A = 6×10^{12} cm^{-3}) would have relatively high series resistance associated with the silicon substrate that the C_s value would be more appropriate. C_s shows a rapid decrease with reduction in the reverse bias voltage from -0.6 to -0.3 volts. The series capacitance C_s then starts to decrease more slowly and reaches a constant value at 3 volts forward bias. The C_s-V characteristic is in keeping with the photo-characteristics illustrated in Figure 7.6 which show that the sensitivity starts to increase at around -0.6 volts and then to increase more rapidly at around -0.4 volts with a decreasing rate of increase in sensitivity from about -0.1 volts to forward bias voltages. This behaviour of the photosensitivity characteristic implies that the depletion region in the silicon widens (the accumulation region is reduced) with a reduction in the reverse bias voltage which also implies that the capacitance of the heterojunction will also be reduced. These arguments on physical grounds are indeed borne out by the C_s versus bias voltage measurements. The I-V, I_{ph}-V and C_s-V measurements confirm the general behaviour which would be expected from the band model shown by Figure 7.4 i.e. that the silicon junction is an accumulation region. On the other hand the parallel capacitance, Figure 7.7(a), shows a different variation of capacitance versus bias voltage, when compared with the series capacitance C_s, and one which does not appear to agree with the other independent electrical measurements i.e. I-V and I_{ph}-V. Consequently C_s is thought to represent the heterojunction equivalent circuit because of the series resistance of the silicon substrate, as outlined earlier.

The capacitance versus frequency measured at zero bias is shown in Figure 7.8, indicating that trapping at recombination centres is occurring, because the heterojunction exhibits capacitive dispersion. This phenomenon is discussed in detail by Milnes.[135] In many junctions

$N_A = 6 \times 10^{12}\ cm^{-3}$

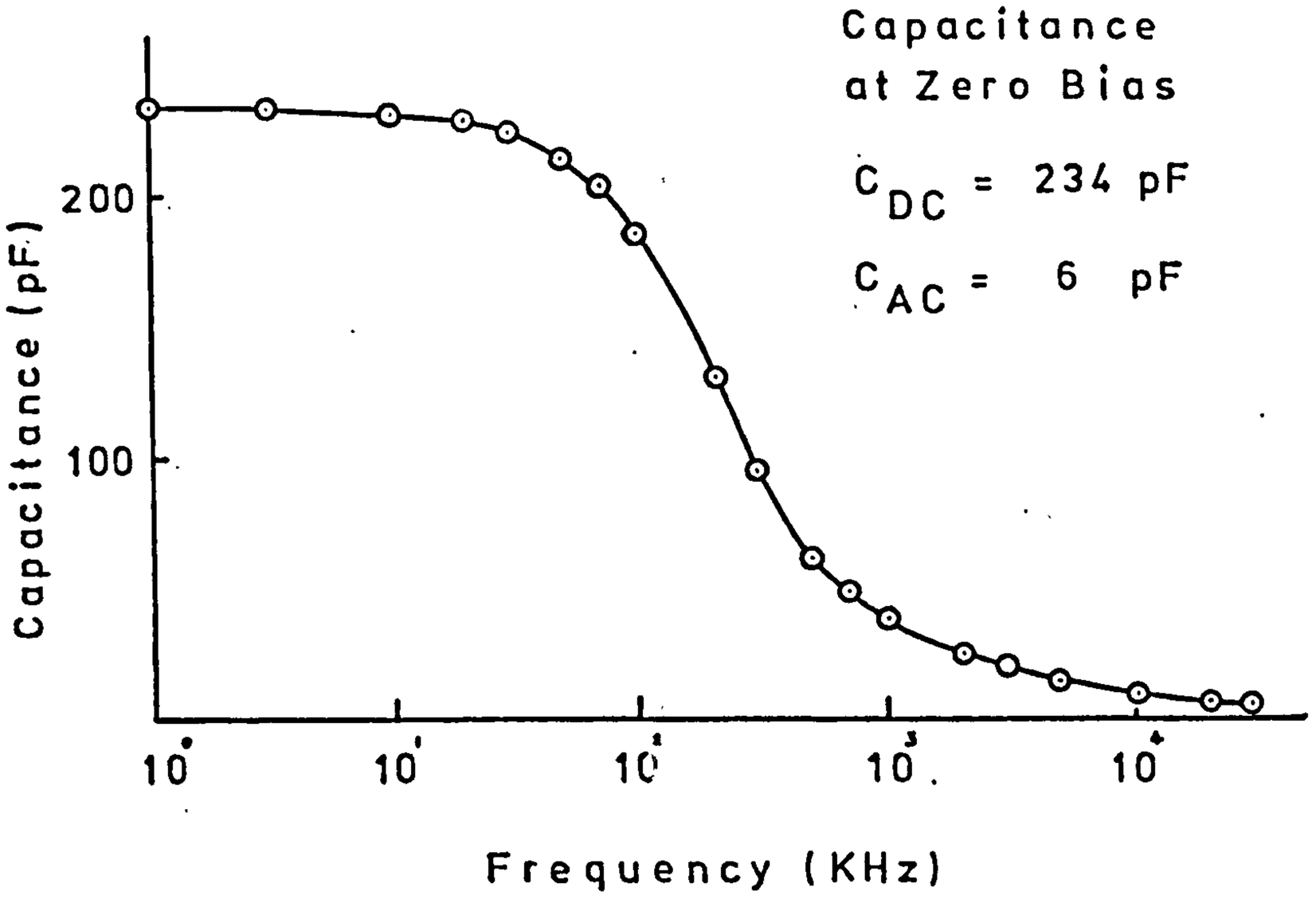


Fig 7.8 Capacitance Frequency Characteristic

$N_A = 6 \times 10^{12}\ cm^{-3}$

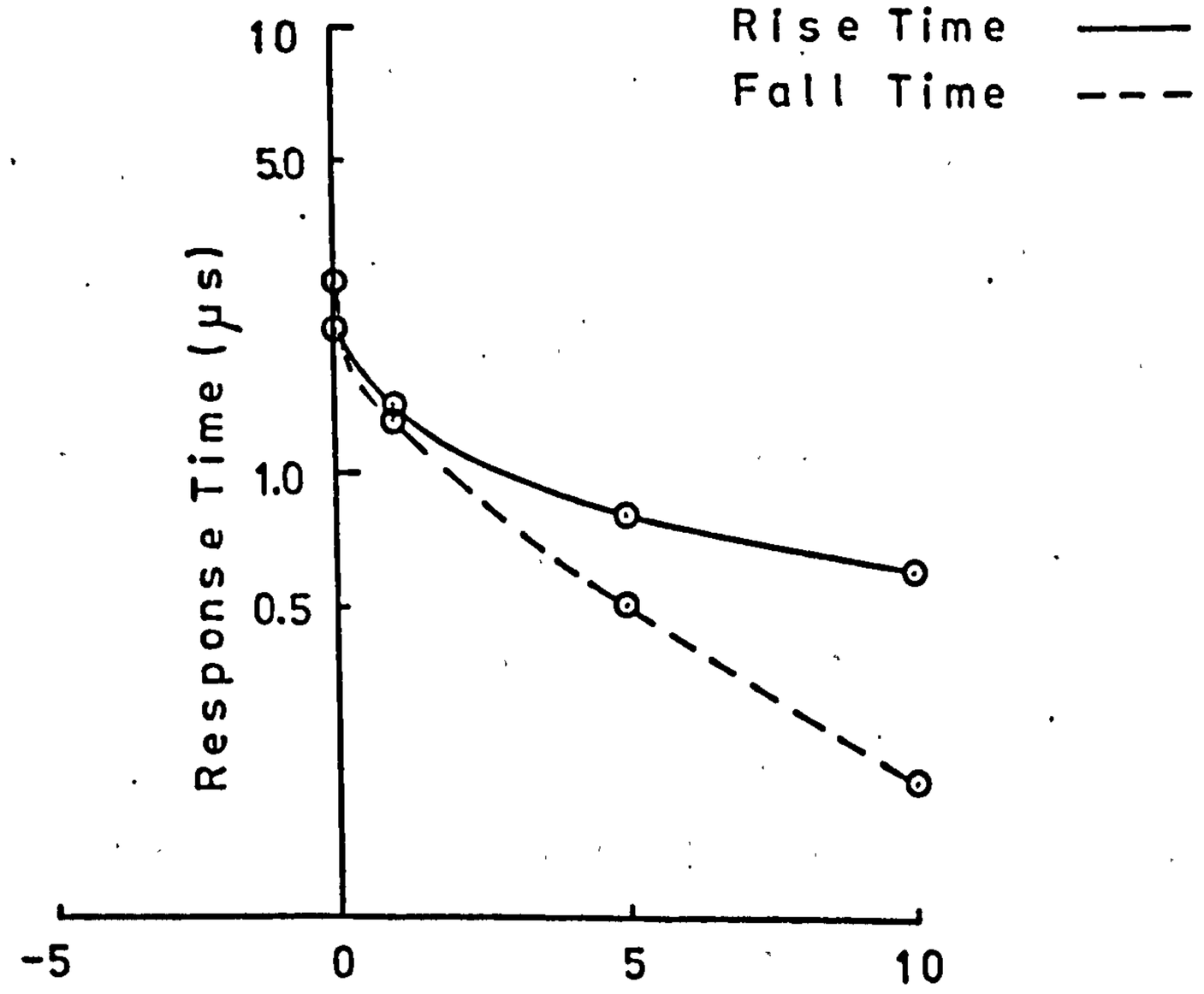


Fig 7.9 Optical Response Time Measurement

containing deep impurities it is not unusual for a region to exist in which the deep impurity is the dominant dopant. This is particularly likely to occur in studies of large energy gap semiconductors (e.g. CdS) but may also be observed in silicon if an excess amount of deep impurity is present. The low-frequency capacitance, C_{DC} is determined by the total effect of deep and shallow impurities, but the high frequency capacitance, C_{AC} is given by the free-carrier density. For small trap densities the frequency effect is small (a few percent); however, if the deep level impurity is dominant, the frequency effect is large i.e. C_{DC} is considerably greater than C_{AC}. Figure 7.8 shows that the low frequency capacitance C_{DC} is 234 pF while the high frequency capacitance C_{AC}, is 6 pF, which implies that one or more deep trapping levels are present. Hampshire[18] observed capacitive dispersion effects with nSi-pGe heterojunctions and attributed the effect to the relaxation of interface states. It is the presence of deep traps in the CdS film which are thought to be the cause of the capacitive dispersion in the nCdS-pSi heterojunctions described in this work. Experimental evidence to justify this viewpoint (quantum efficiency of heterojunction photodetector as a function of optical wavelength) will be discussed shortly. It is clear from the results of capacitance versus frequency, that the capacitance versus bias voltage measurements were carried out at a frequency (200 KHz) which was in a region where trapping effects were present. However, there is little point in measuring capacitance versus bias at higher frequencies (greater than 10 MHz) since it is then difficult to correlate this measurement with the other measurements where traps were present i.e. such a measurement would not be representative of the nCdS-pSi heterojunction.

The response time to an optical pulse is shown in Figure 7.9. The rise and fall times of the detected optical pulse decrease with

increasing forward bias; in general agreement with the capacitance versus bias voltage measurements. However, there is not a commensurate decreasc in response time with decrease in capacitance e.g. the ratio of C_s at 0 and +3 volts bias is 6.7 while the ratio of the rise times and fall times is 4.3 and 2.9 respectively at these two bias voltages. This discrepancy is perhaps not surprising as there are a number of differences between the two techniques (i) the resistance as well as the capacitance determines the RC time constant, (ii) the capacitance measured at 200 KHz as a function of bias does not take account of all the traps that are present, as the capacitance versus frequency characteristic indicates, (iii) the detection of the optical pulse with wavelength 904 nm will primarily be affected by traps at energies near the equivalent energy of this wavelength (i.e. 1.38 eV)..

The spectral response characteristic is shown in Figure 7.10 and it is obvious that the "window effect" photoresponse, discussed earlier in the thesis, is significantly reduced at three different wavelengths. The reduction in quantum efficiency at 578, 616, and 780 nm corresponds to a photon energy of 2.15, 2.02 and 1.59 eV respectively. The CdS energy gap value of 2.43 eV, means that the traps are 0.28, 0.41, and 0.84 eV respectively below the conduction band or above the valence band.

The energy depths (below conduction band) of six traps, found by Woods and Nicholas,[136] were 0.05 eV (5×10^{-24} cm^2), 0.14 (10^{-22} cm^2), 0.25 (5×10^{-24} cm^2), 0.41 (10^{-20} cm^2), 0.63 (-), and 0.83 (10^{-14} cm^2) respectively. The figures in brackets are approximate values of the electron capture cross section. Thus the traps identified by the spectral response measurement are thought to be the ones found by Woods at 0.25, 0.41 and 0.83 eV below the conduction band. The reason for the small discrepancies, up to 0.03 eV, was that the exact position of the minima of quantum efficiency was not precisely determined, in the present work,

$N_A = 6 \times 10^{12}\ cm^{-3}$

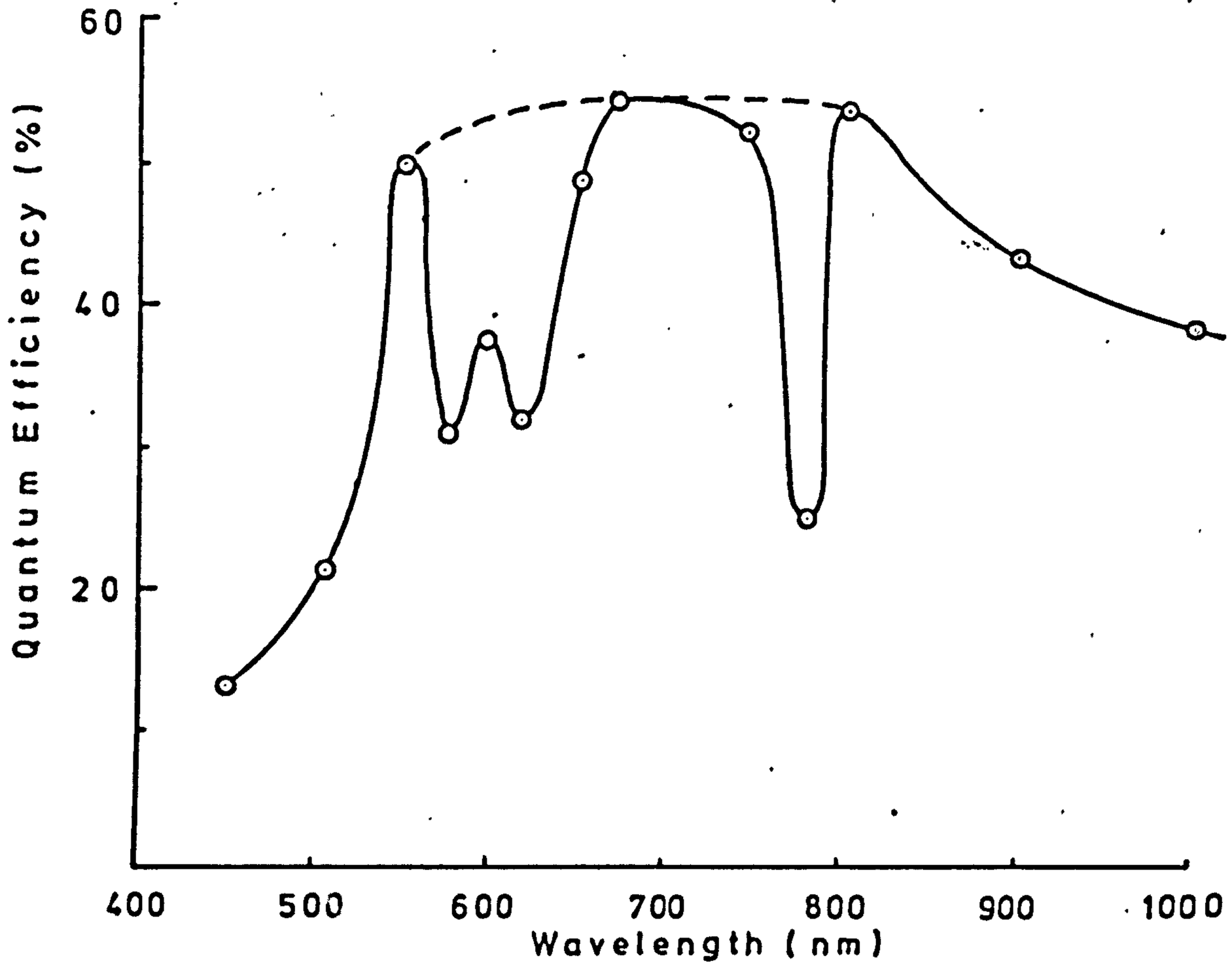


Fig 7.10 Spectrum Response Characteristic

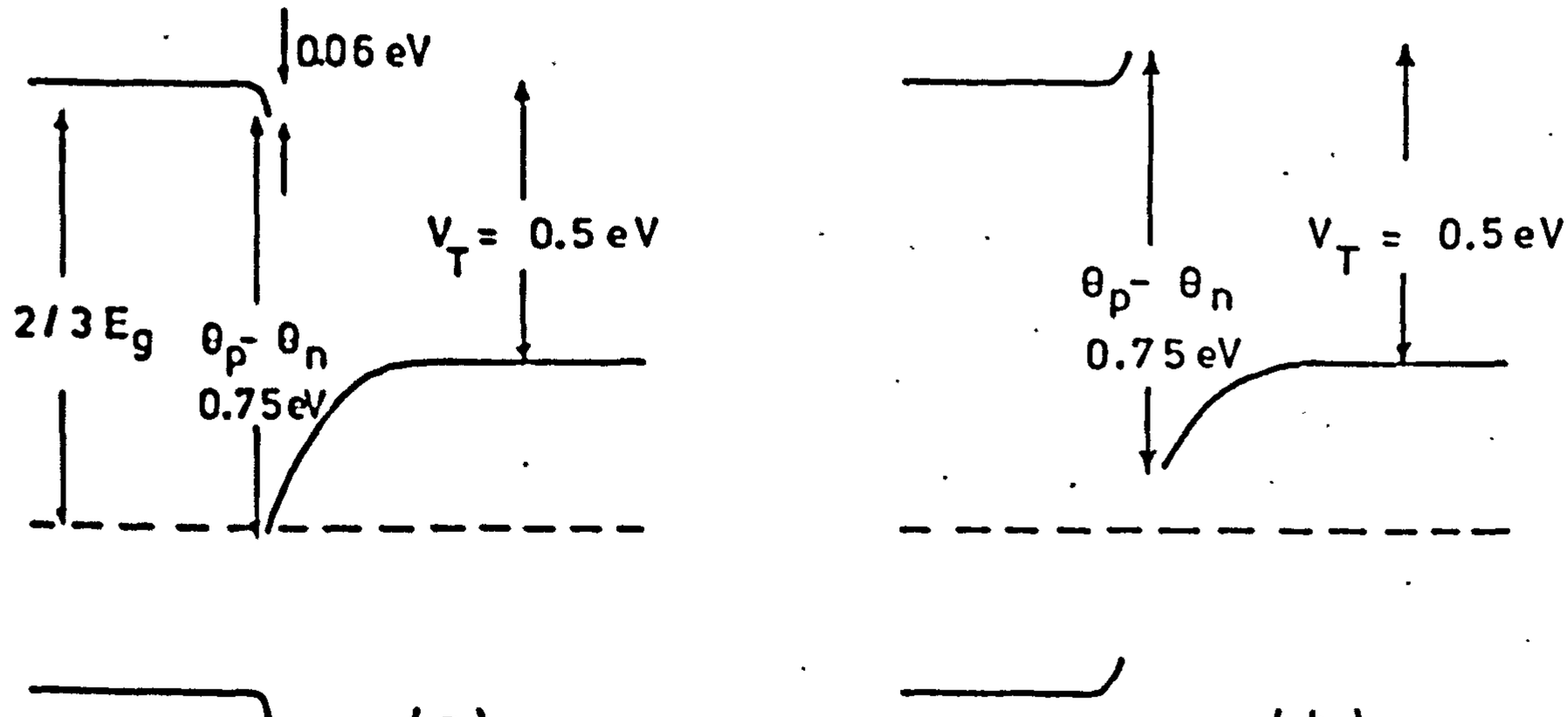
since fixed wavelength filters were used.

It is worthwhile considering the general features of a heterojunction fabricated using a silicon substrate, which was not thermally cleaned, with the same acceptor doping ($N_A = 6 \times 10^{12}$ cm^{-3}). The saturation current I_s was considerably higher, 10^{-5}A compared with 8×10^{-8}A, and the n factor was 4.6 compared with 2.8 for a thermally cleaned device. The photodetection properties showed that V_{OC} was lower, 0.35 compared with 0.49 volts, and the n factor was 7.3 compared with 4.6 for a thermally cleaned device. To summarise, devices fabricated using silicon substrates which have not been thermally cleaned are generally of poorer performance. The higher values of n both from I-V and I_{ph}-V measurements, indicate that the CdS films probably have higher trap densities and that surface contamination effects may be important.

7.3.2 Case 2 $N_A = 6 \times 10^{13}$ cm^{-3}

The band structures for this value of doping are shown in Figure 7.11(a) and 7.11(b), where 7.11(a) represents the expected situation with surface states and 7.11(b) the situation without the inclusion of surface states. Figure 7.11(a) shows that the Si region is depleted and the CdS is an accumulation region. On the other hand, Figure 7.11(b) shows that both semiconductor junctions are accumulation regions, a similar situation to that found in case 1 (Figure 7.4).

The current-voltage characteristics, shown in Figure 7.12 are quite different to those measured for case 1. The reverse I-V characteristic is "hard" while the forward I-V characteristic is exponential and is similar to a conventional p-n homojunction characteristic except that the turn-on voltage and forward voltage drop are considerably higher in this case. The band structure of Figure 7.11(a) predicts that reverse bias increases the barrier potential and increases the width of the depletion region



(a) Surface States

(b) No Surface States

Fig 7.11 Band Diagram

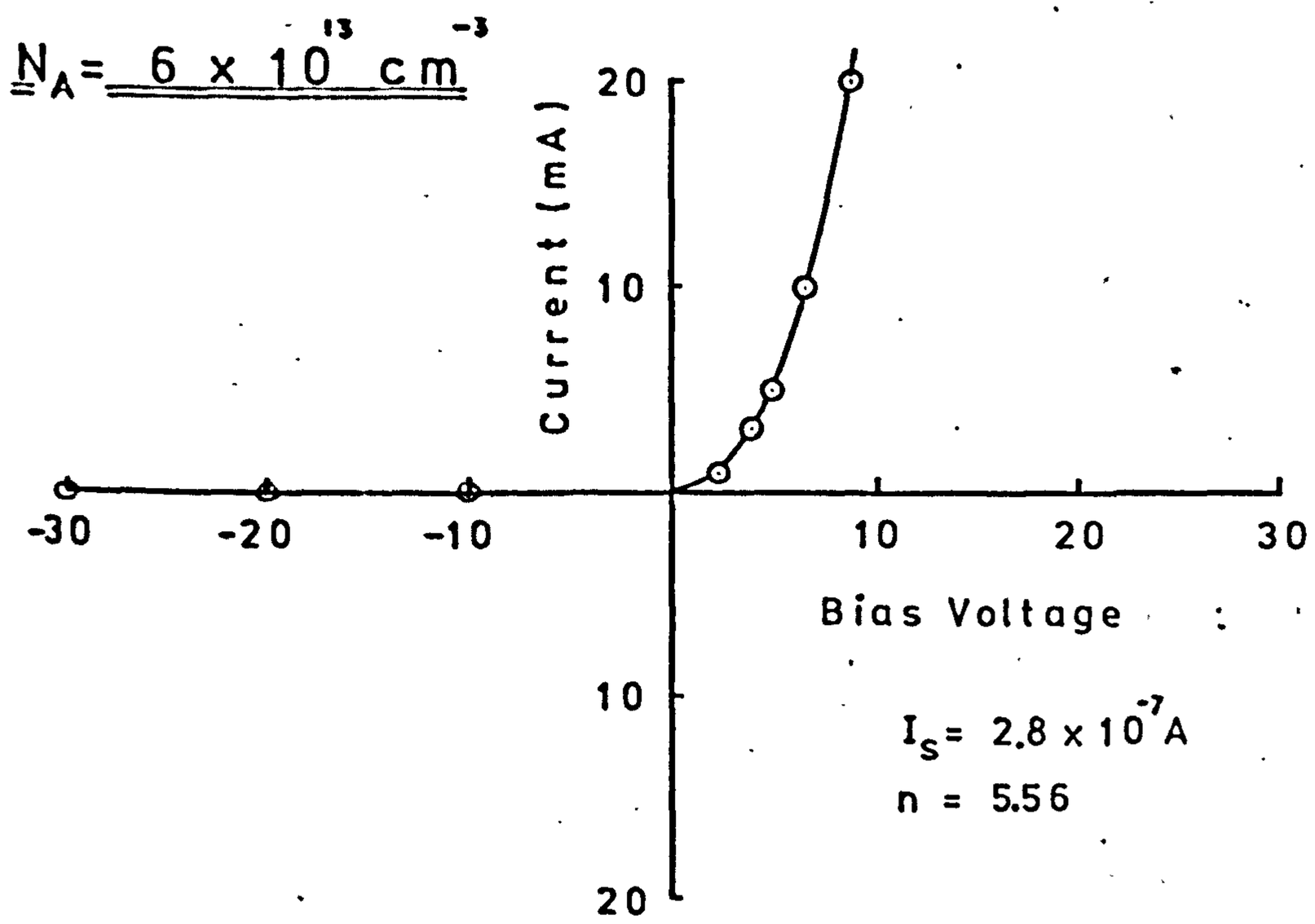


Fig 7.12 I-V Characteristic

in the Si, implying that in reverse bias the current will be low for a given voltage. In contrast a forward bias voltage will reduce the barrier potential, reduce the depletion region in the Si and so current will increase with increasing forward bias. This behaviour is observed experimentally. If Figure 7.11(b) were the appropriate band model then the behaviour of the I-V characteristics would be qualitatively similar to case 1, but this is not observed experimentally. Thus there is experimental evidence suggesting that the band model which includes the effect of surface states gives a better qualitative explanation of the I-V characteristics than a band model neglecting surface states. The model with surface states also gives an insight into the reason for the considerable difference in the I-V characteristics of cases 1 and 2, which only differ in acceptor doping level by a factor of 10. Since the value of n, from the I-V measurements, is 5.6 compared with the theoretical value of 2 for recombination, this suggests that more complex trapping mechanisms are involved.

The photocurrent versus bias characteristic is shown in Figure 7.13; this time showing an increase in sensitivity in reverse bias, in contrast to case 1 (Figure 7.6). The maximum quantum efficiencies are fairly similar, around 40% at 600 nm, while the open circuit voltage is lower, 0.41 compared with 0.49 for case 1. A calculation, using equation 7.1, gives the barrier voltage as 0.32 eV compared with the 0.5 eV from the theoretical model, again reasonable agreement.

Because the silicon junction region is depleted and the CdS junction is an accumulation region most of the applied bias voltage will be dropped across the lower conductivity silicon region. This fact makes it possible to treat the heterojunction as a one sided abrupt junction, at least to a first approximation. The depletion width for this situation can be written as:

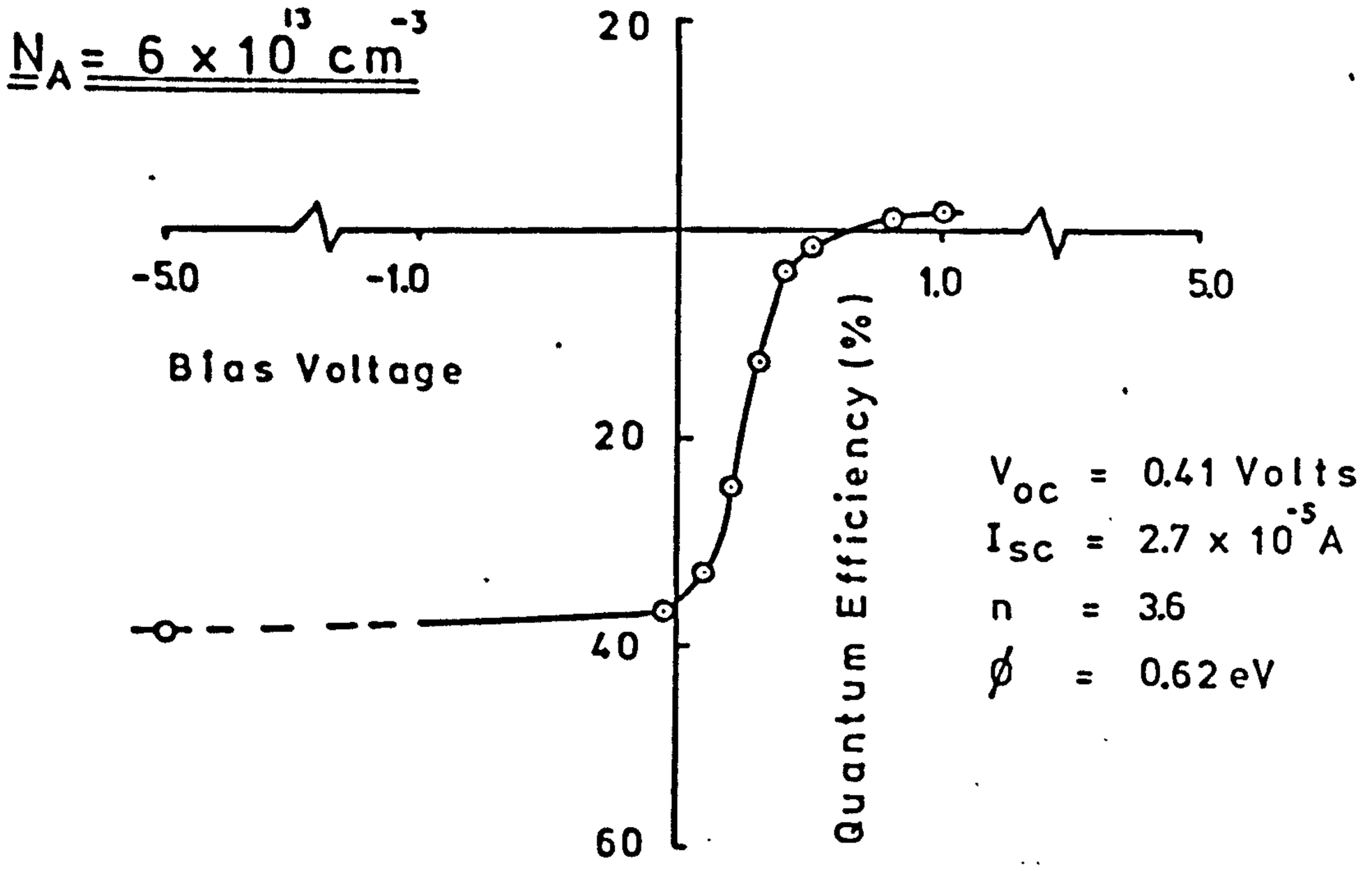


Fig 7.13 Photo Characteristic

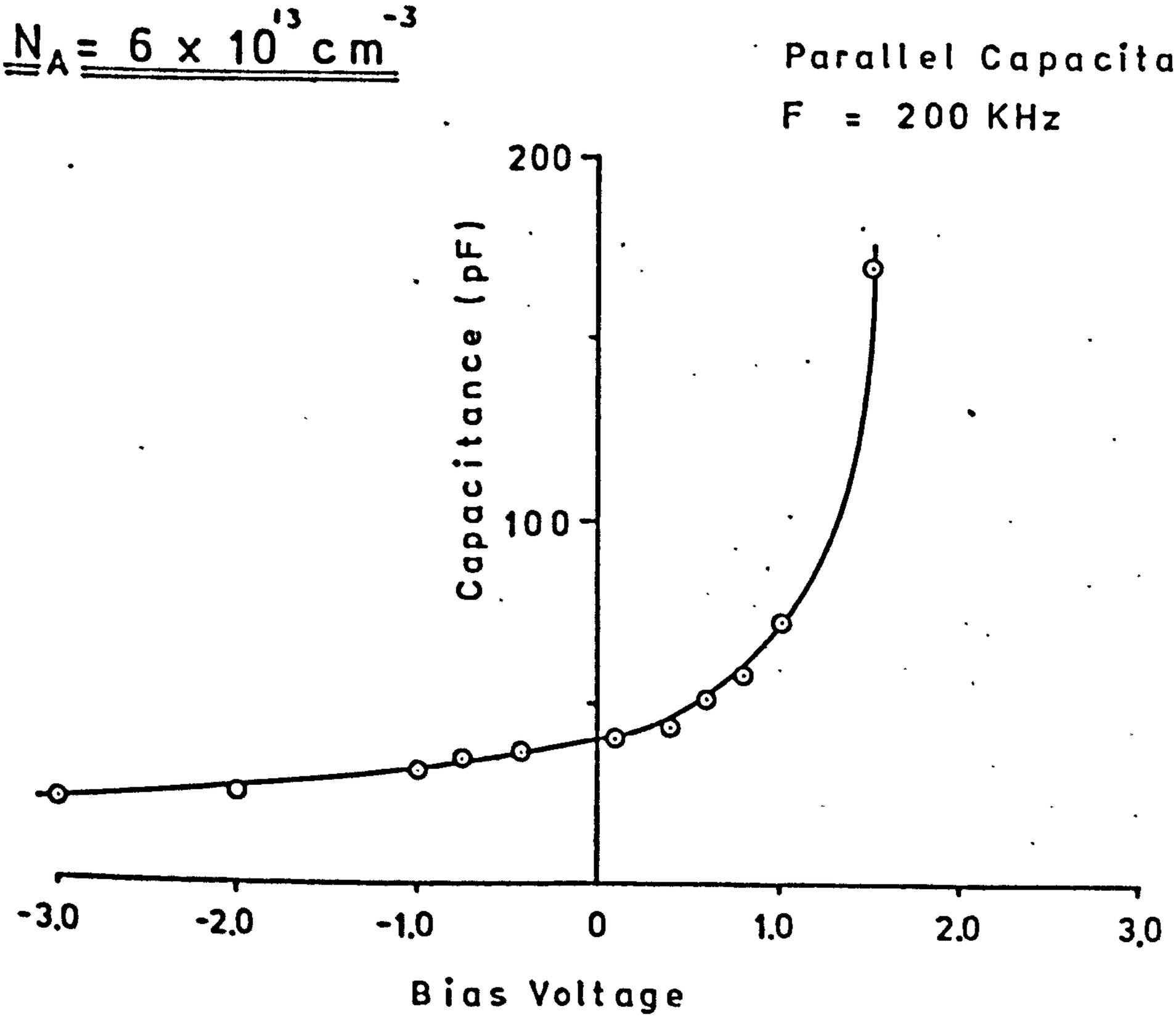


Fig 7.14 Capacitance Voltage Characteristic

$$w = \sqrt{\frac{2\varepsilon_r \varepsilon_o (V_D - V)}{qN_A}} \qquad (7.2)$$

where ε_r is the relative permittivity for silicon, 11.8, ε_o is the permittivity of free space, 8.85×10^{-12} F/m, and V_D, the barrier potential, is 0.6 eV (from Figure 7.11(a)). Using equation 7.2, the depletion width w, at -1.0 volts bias, is 4.8 μm. Using equation 3.33 it is possible to calculate the maximum theoretical photocurrent and compare this value with the experimentally measured photocurrent. As mentioned in Chapter 3 the diffusion term may be neglected and only the term in the square brackets need be considered, namely:

$$I_{ph} = \frac{qP}{E_p} \left[1 - \frac{\exp -\alpha w}{1+\alpha L_n} \right] \qquad (7.3)$$

At 600 nm $\alpha \simeq 5 \times 10^3$ cm^{-1}, L_n is estimated to be 6.2×10^{-4} cm and the optical power measured was 131 μW (using thermopile). Using these values, $\exp(-\alpha w)$ is 0.06 and the theoretical photocurrent is 64 μA. The measured photocurrent is of course less than this figure since not every photon produces an electron-hole pair. The measured photocurrent was 25 μA i.e. the quantum efficiency was 39%. The calculation and the experimental results show that the depletion width w in the silicon was sufficiently large to minimise the term involving the exponential inside the square bracket. The quantum efficiency would be higher if traps were not present. A typical spectral response characteristic is shown in Figure 7.10, for case 1; the dotted part of the curve is drawn to estimate what the quantum efficiency might be if traps were not present. If traps were not present, the quantum efficiency would be 44% higher at 600 nm, i.e. an absolute value of 56% instead of 39%.

The capacitance versus voltage characteristic is shown in Figure 7.14. The capacitance increases as the reverse bias is reduced and at

around 0.5 volts forward bias the capacitance starts to increase more rapidly with increasing forward bias. This rapid increase in capacitance may be a result of traps in the CdS film as well as the narrowing of the depletion region illustrated by the photo-characteristics (Figure 7.13) where the photocurrent falls to zero at 0.6 volts forward bias. The I-V, I_{ph}-V and C-V characteristics all provide experimental evidence that the depletion region in the silicon narrows in forward bias and widens in reverse bias. These results would be expected from the band model including surface state effects presented in Figure 7.11(a). Figure 7.15 illustrates the variation of capacitance with frequency. This variation has the same form as the measurements for Case 1 shown in Figure 7.8. The low frequency capacitance C_{DC} was 145 pF while the high frequency capacitance C_{AC} was 5 pF. As mentioned in the discussion of Case 1, C_{AC} is given by the free-carrier density. Using the abrupt one sided junction approximation which is applicable to Case 2 the junction capacitance can be expressed as:

$$C = \frac{\varepsilon_r \varepsilon_o A}{w} \qquad (7.4)$$

where ε_r is the silicon permittivity 11.8, A is the junction area, 8×10^{-3} cm^2 and w is the depletion width. The depletion width, using this approximate method is calculated to be 16.7 μm. This value is in fair agreement with the 4.8 μm depletion width calculated from equation 7.2.

The response time measurements are given in Figure 7.16. There is a reduction in rise and fall time as the bias is changed from +1.0 volt forward bias to -1.0 volt reverse bias which can be associated qualitatively with the reduction in capacitance shown in Figure 7.14. The measurements show that to maximise the sensitivity and minimise the response time it is advantageous to operate the heterojunction photodetector for Case 2

$\underline{N_A = 6 \times 10^{13}\ cm^{-3}}$

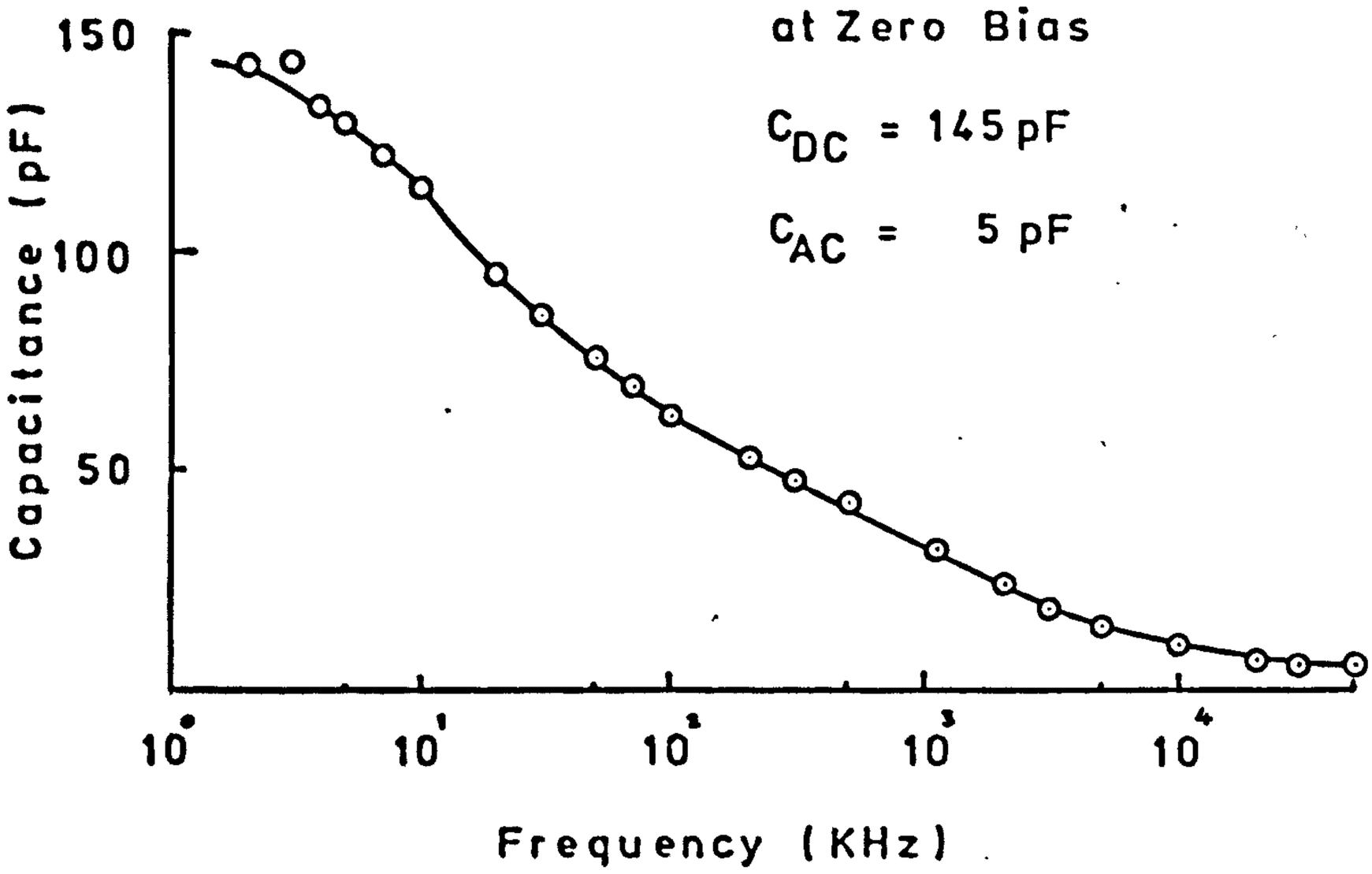


Fig 7.15 Capacitance Frequency Characteristic

$\underline{N_A = 6 \times 10^{13}\ cm^{-3}}$

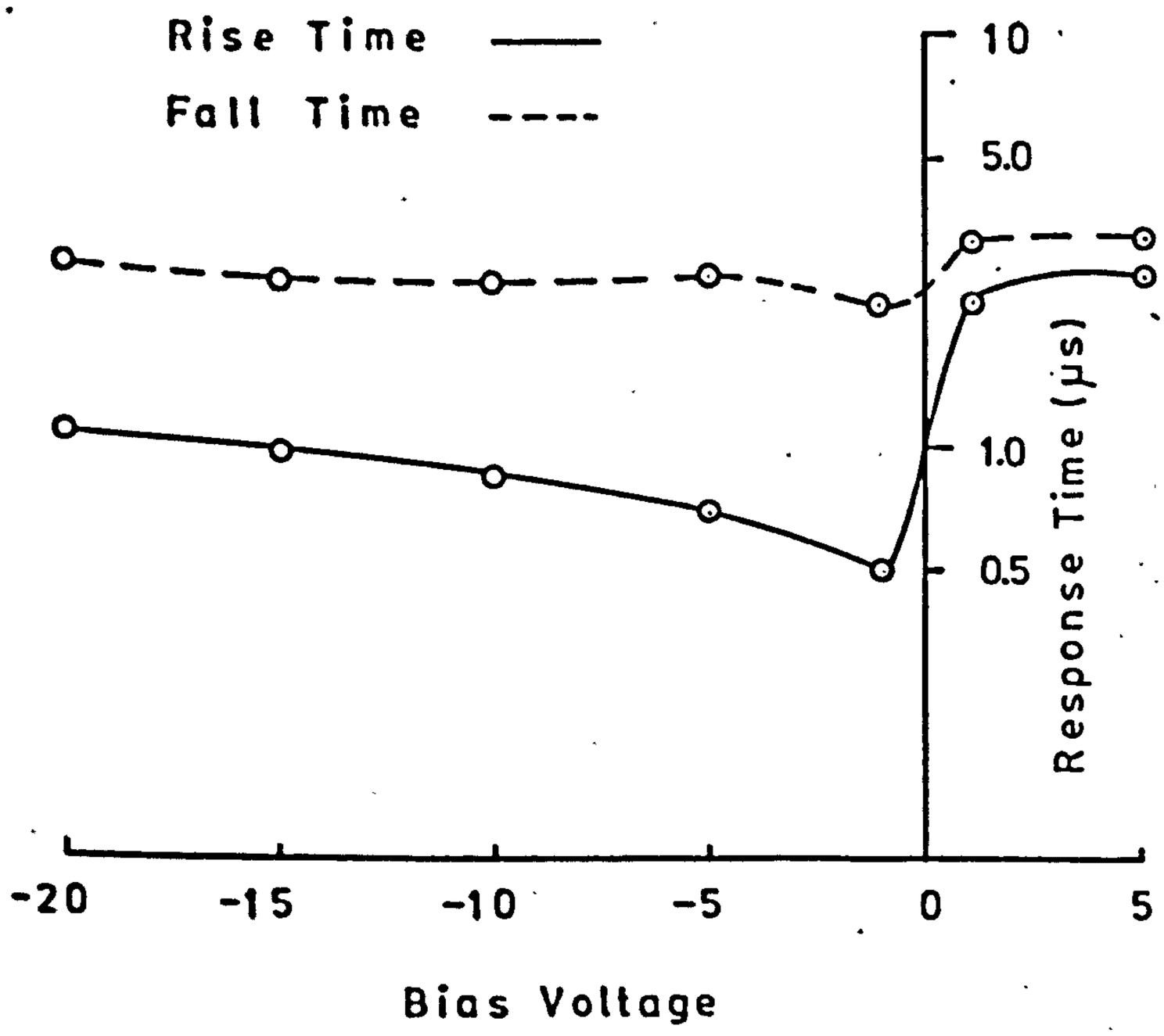


Fig 7.16 Optical Response Time Measurement

at -1.0 reverse bias .

The results from a device which had not been thermally cleaned show the same qualitative differences to the thermally cleaned device as previously for Case 1; higher saturation current and n factor, lower quantum efficiency and a lower open circuit voltage. In addition, a response time measurement showed a much slower response. At -2.0 volts reverse bias, the rise time was 1.3 μs compared with 0.5 μs while at -20 volts reverse bias it was 30 μs compared with 1.1 μs.

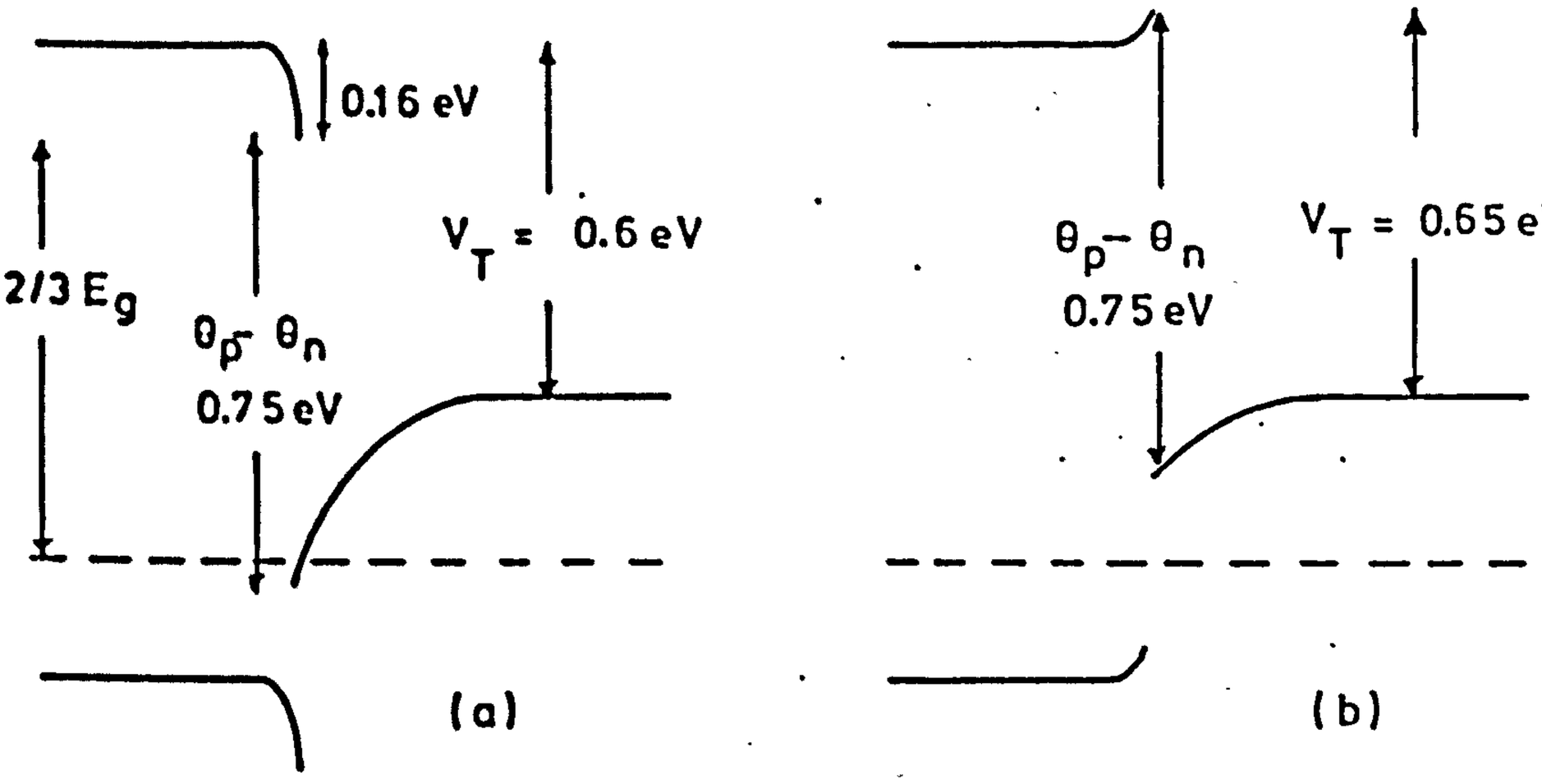
7.3.3 Case 3 $N_A = 3 \times 10^{15}$

Figure 7.17(a) and 7.17(b) show the band diagrams for this case with and without the inclusion of surface states. As the band diagrams for Case 3 are similar to those of Case 2, apart from the difference in barrier potential associated with the change in doping, the experimental measurements should also be qualitatively the same.

The I-V characteristics are given in Figure 7.18, and show low reverse bias current together with a very rapid turn on in forward bias. The reduction in turn-on voltage compared with the Case 2 heterojunction may be associated with the reduction in the silicon resistivity as a result of the increased doping level. However, the change in turn-on voltage is not as large as would be expected from doping considerations because of the increase in barrier potential. The n factor of 2.1 from the forward bias characteristic, which is exponential over the entire range measured, suggests that recombination is the dominant process.

Figure 7.17(a), the band model with surface states shows that the silicon junction region is depleted while the band model without surface states Figure 7.17(b), shows that the silicon junction is an accumulation region. Thus the band model with surface states would have a conventional p-n

$\underline{\underline{N_A = 3 \times 10^{15}\ cm^{-3}}}$



(a) Surface States

(b) No Surface States

Fig 7.17 Band Diagram

$\underline{\underline{N_A = 3 \times 10^{15}\ cm^{-3}}}$

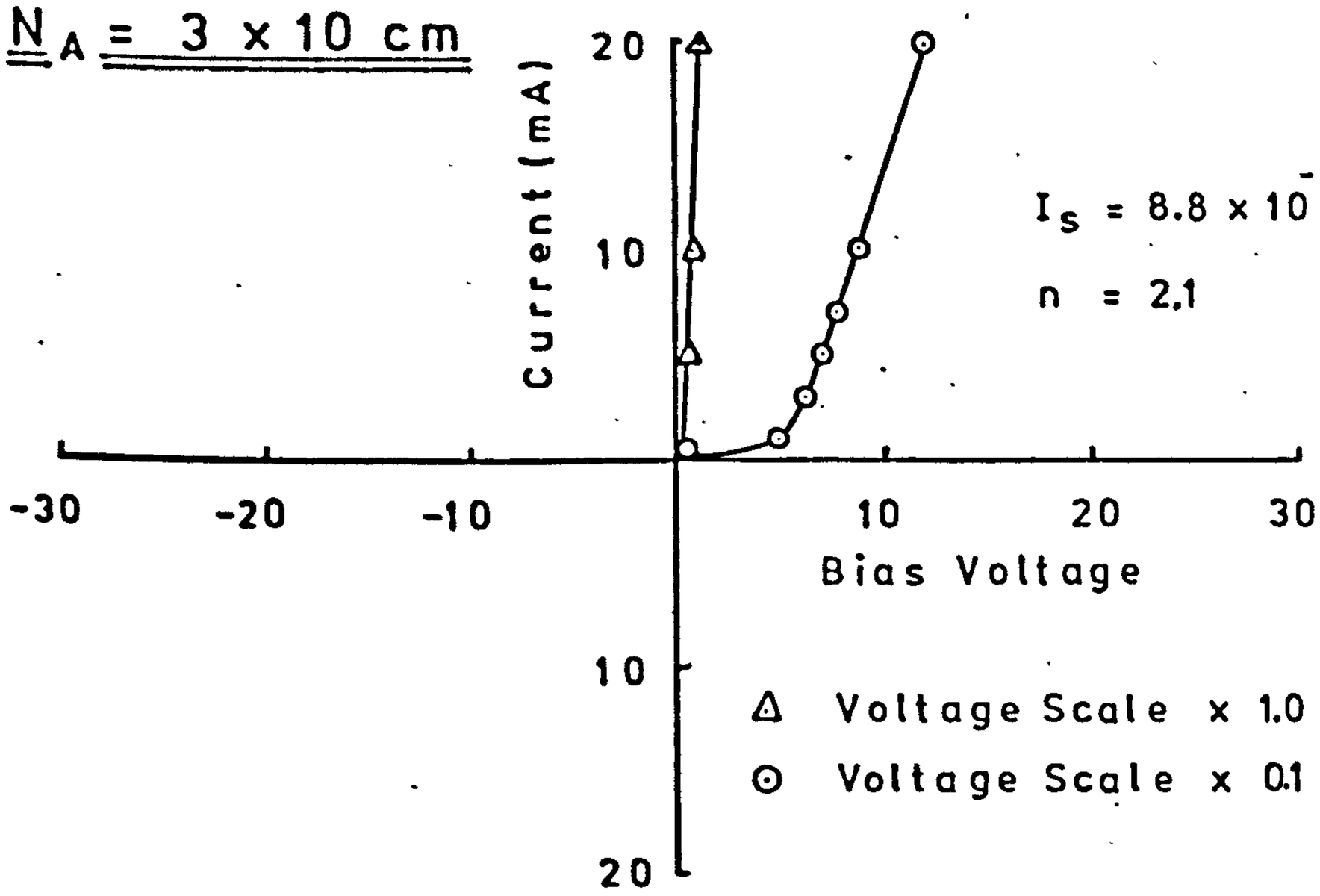


Fig 7.18 I-V Characteristic

homojunction characteristic while the model without surface states would have an I-V characteristic qualitatively similar to the Case 1 heterojunction diode where forward bias was the low current region. On this basis, the band model which includes the effect of surface states, appears to qualitatively explain the experimental I-V characteristics.

The photo characteristics are shown in Figure 7.19. They indicate that the band model without surface states is not applicable because forward bias would be required, like the Case 1 diode, to result in any appreciable sensitivity. Figure 7.19 shows that the sensitivity increases with increasing reverse bias and this is the behaviour that is described when surface states are considered, i.e. reverse bias increases the depletion width. The barrier potential calculated from the measurements of the photo characteristics is 0.39 eV, again in reasonable agreement with the theoretical value of 0.6 eV. The quantum efficiency is 26% at -1.0 volts reverse bias and V_{OC} is 0.34 volts. The reduction of both the quantum efficiency and V_{OC} compared with the Case 2 heterojunction photodetector is because of the narrower depletion region. Using the one sided abrupt junction approximation and equation 7.2, the calculated depletion width in the silicon at -1.0 volts reverse bias is 0.71 μm compared with 4.8 μm for the Case 2 heterojunction. Using equation 7.3 it is possible to estimate the maximum theoretical photocurrent for this depletion width at 600 nm. In this particular case the optical power was 53 μW. Hence the value of exp $-\alpha w$ is 0.45 and the theoretical photocurrent is 22.5 μA. It is clear that, because of the narrower depletion region, it is no longer possible to neglect the exponential term in the square brackets (equation 7.3). The measured photocurrent was 6.7 μA corresponding to a quantum efficiency of 30% when based on the maximum theoretical photocurrent.

Figure 7.20 gives the capacitance versus bias voltage characteristic

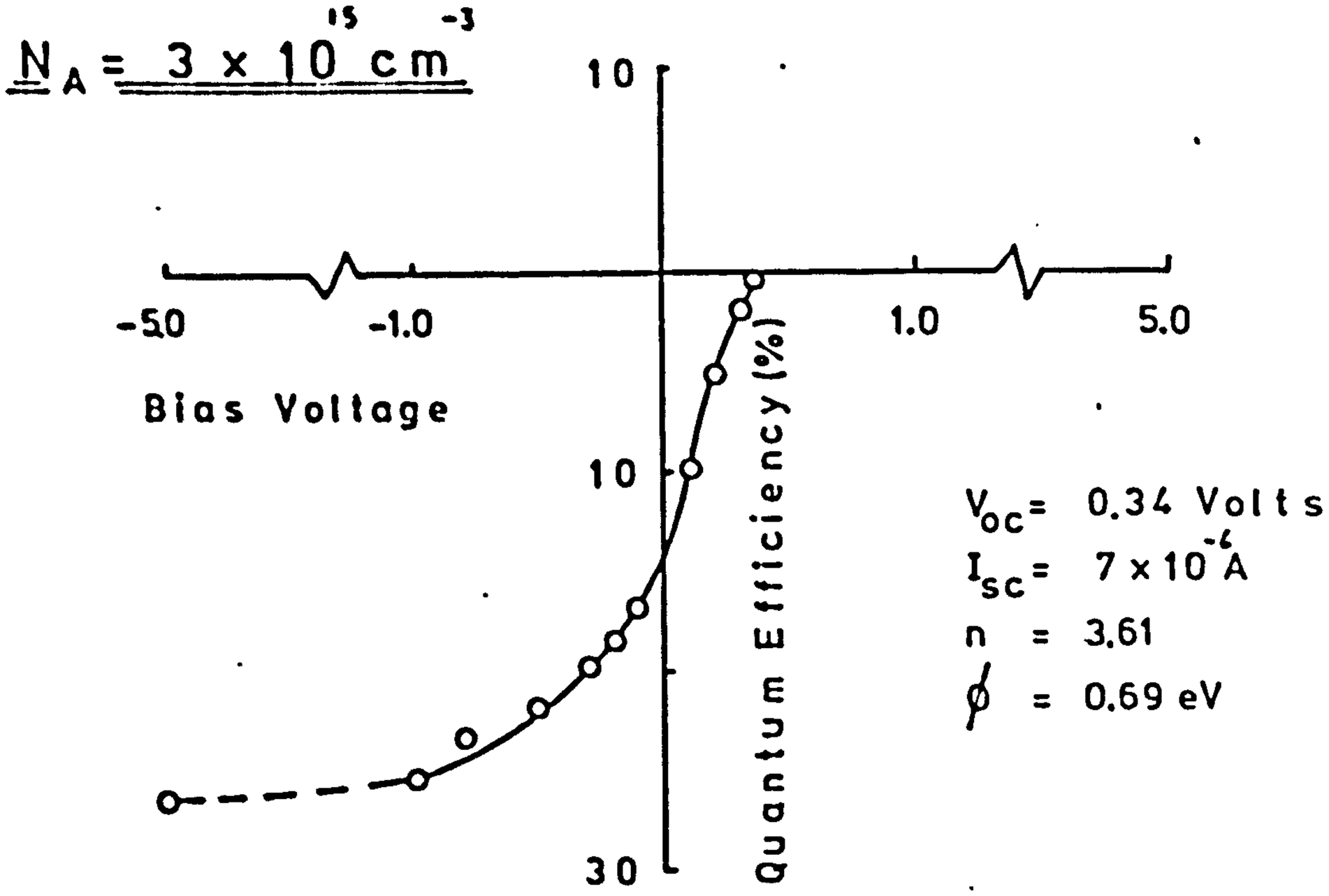


Fig 7.19 Photo Characteristic

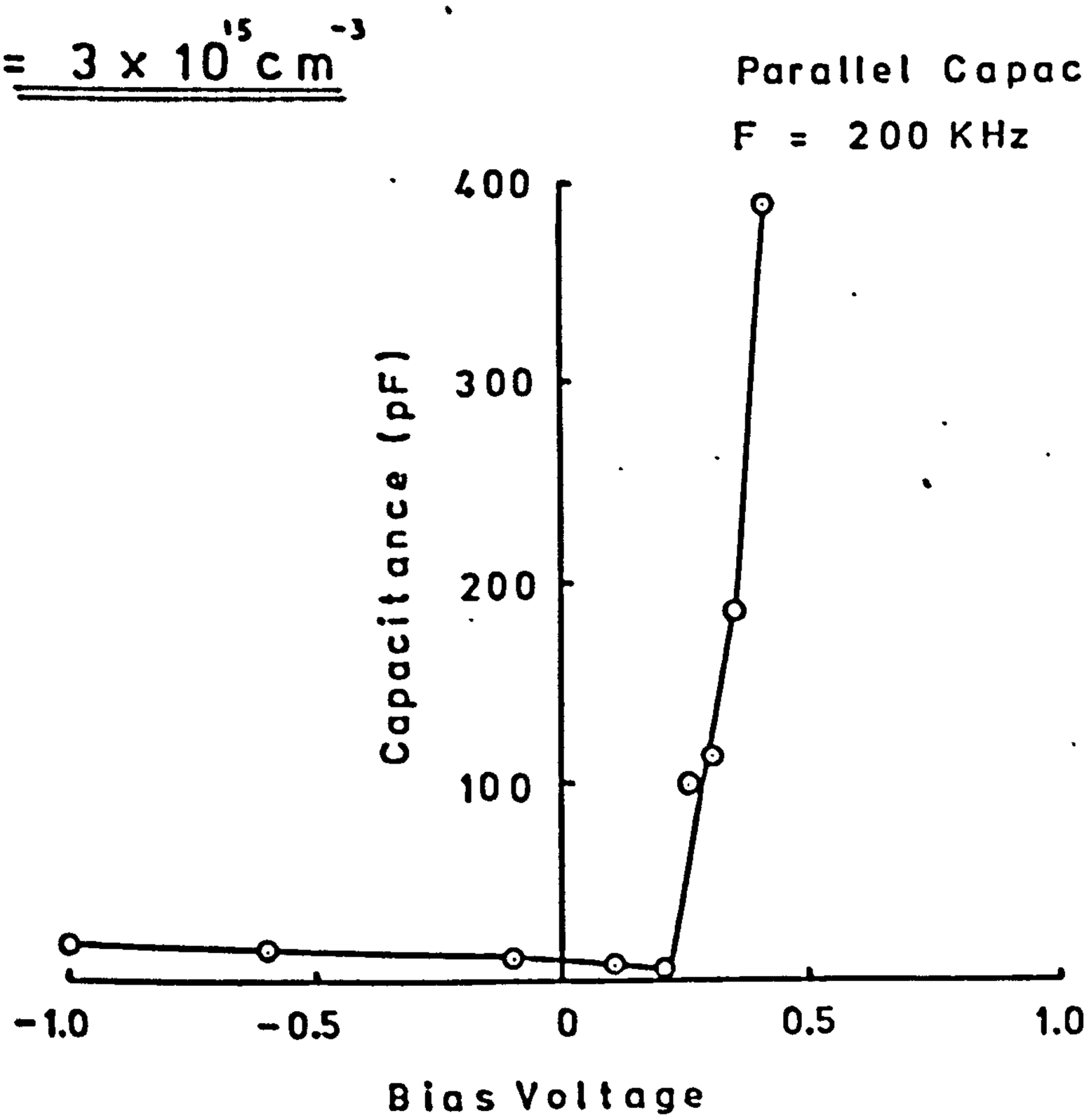


Fig 7.20 Capacitance Voltage Characteristic

for Case 3. In forward bias the capacitance increased by a very large amount over a relatively small bias voltage range. While this does agree with the forward bias I-V characteristics, showing that the depletion width is narrowing, the capacitances are so high that recombination at trapping centres must be occurring.

The capacitance versus frequency at zero bias are given in Figure 7.21, again indicating that traps are present. The low frequency capacitance C_{DC} was 150 pF while the high frequency capacitance C_{AC} was 70 pF. The same calculation can be carried out, with the assumption of an abrupt one sided junction, as in Case 2, to estimate the depletion region in the silicon. Using equation 7.4 and with C_{AC} as 70 pF, the depletion width is 1.2 μm, in fair agreement with the value calculated using equation 7.2.

Figure 7.22 gives the response time measurements to an optical pulse. They show broadly the same behaviour as the Case 2 heterojunction although the Case 3 heterojunction is about a factor of 4 or 5 slower. The longer response time may be attributed to the narrower depletion region for the Case 3 diode and possibly differences in the trap densities.

Experimental measurements on devices which have not been thermally cleaned show the same comparative trend as was observed with uncleaned devices of Cases 1 and 2; higher n values, lower V_{OC} and quantum efficiencies, i.e. 16% compared with 26% at -1.0 volts reverse bias.

7.3.4 Case 4 $N_A = 3 \times 10^{17}$ cm^{-3}

Figure 7.23(a) and 7.23(b) give the proposed band model for heterojunctions with N_A of 3×10^{17} cm^{-3}, with and without surface states. It is clear that the barrier potential is the same, 0.7 eV and that in both 7.23(a) and 7.23(b) the silicon junction is depleted while the CdS junction is an accumulation region. The only difference is the degree

$\underline{\underline{N_A = 3 \times 10^{15} \text{ cm}^{-3}}}$

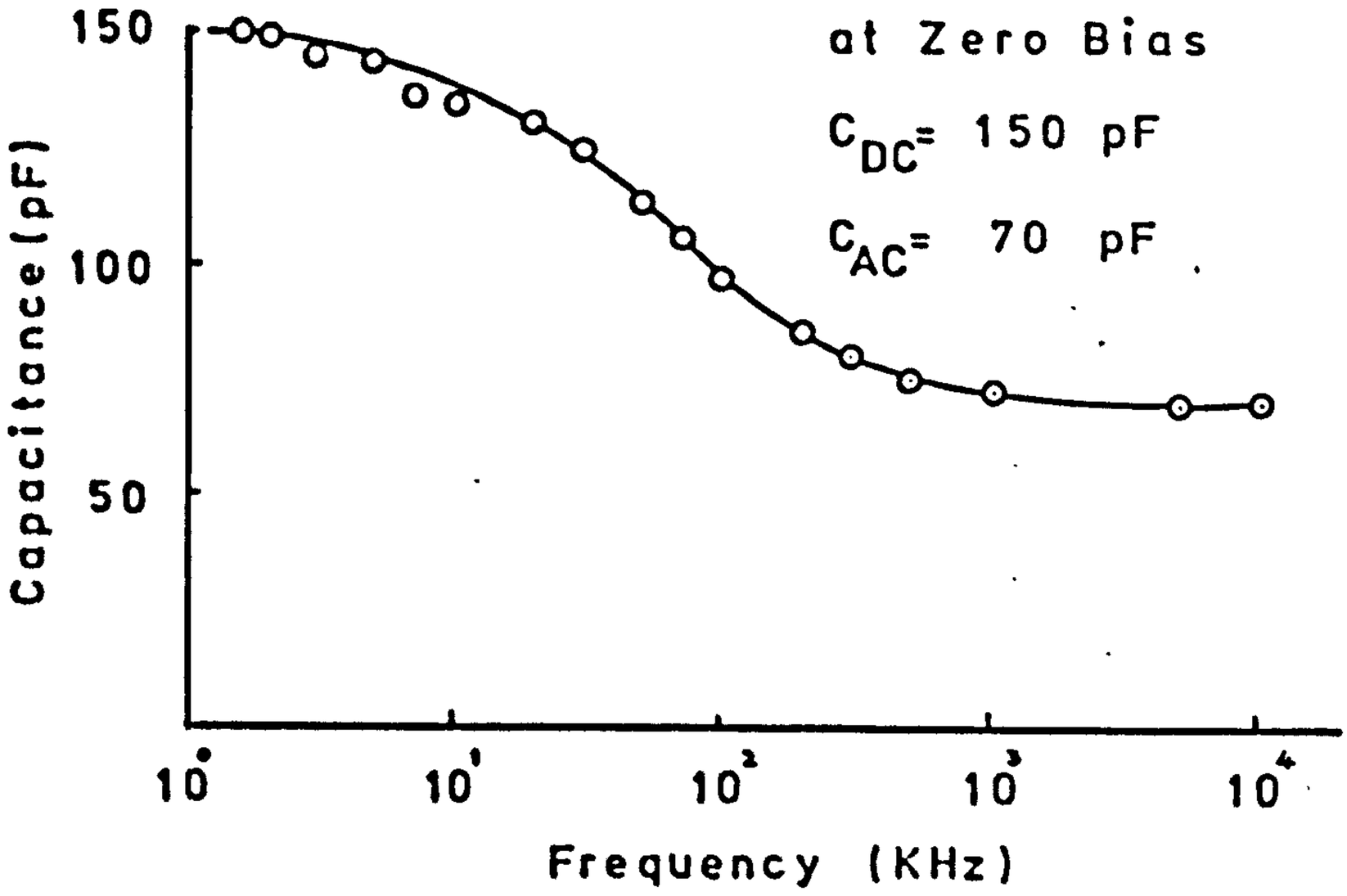


Fig 7.21 Capacitance Frequency Characteristic

$\underline{\underline{N_A = 3 \times 10^{15} \text{ cm}^{-3}}}$

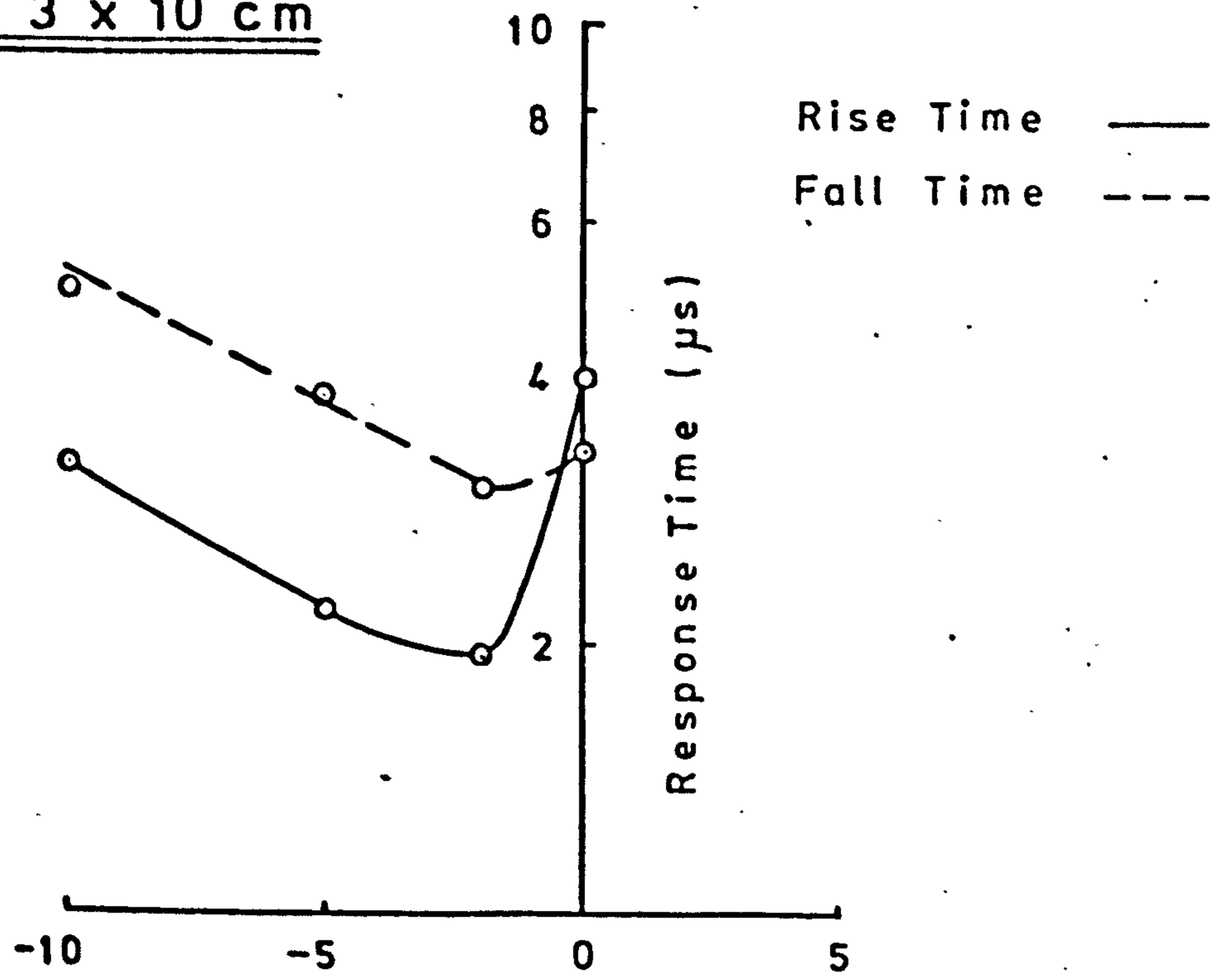
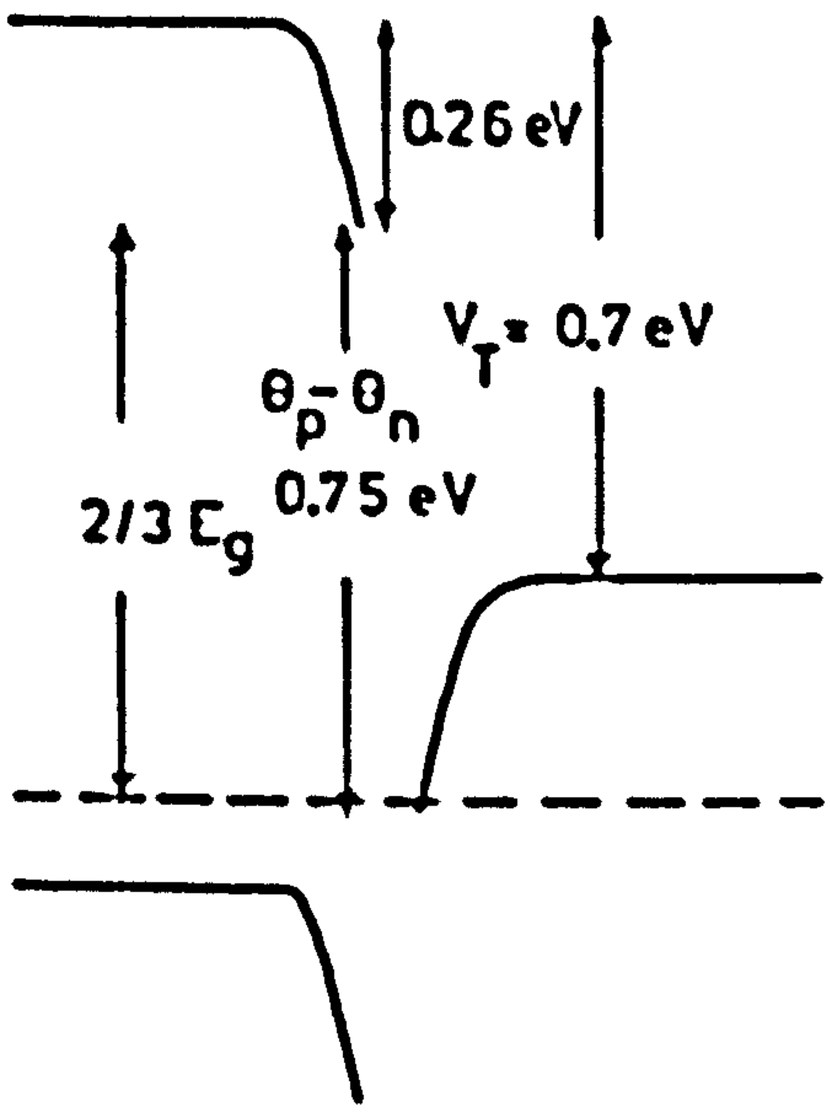
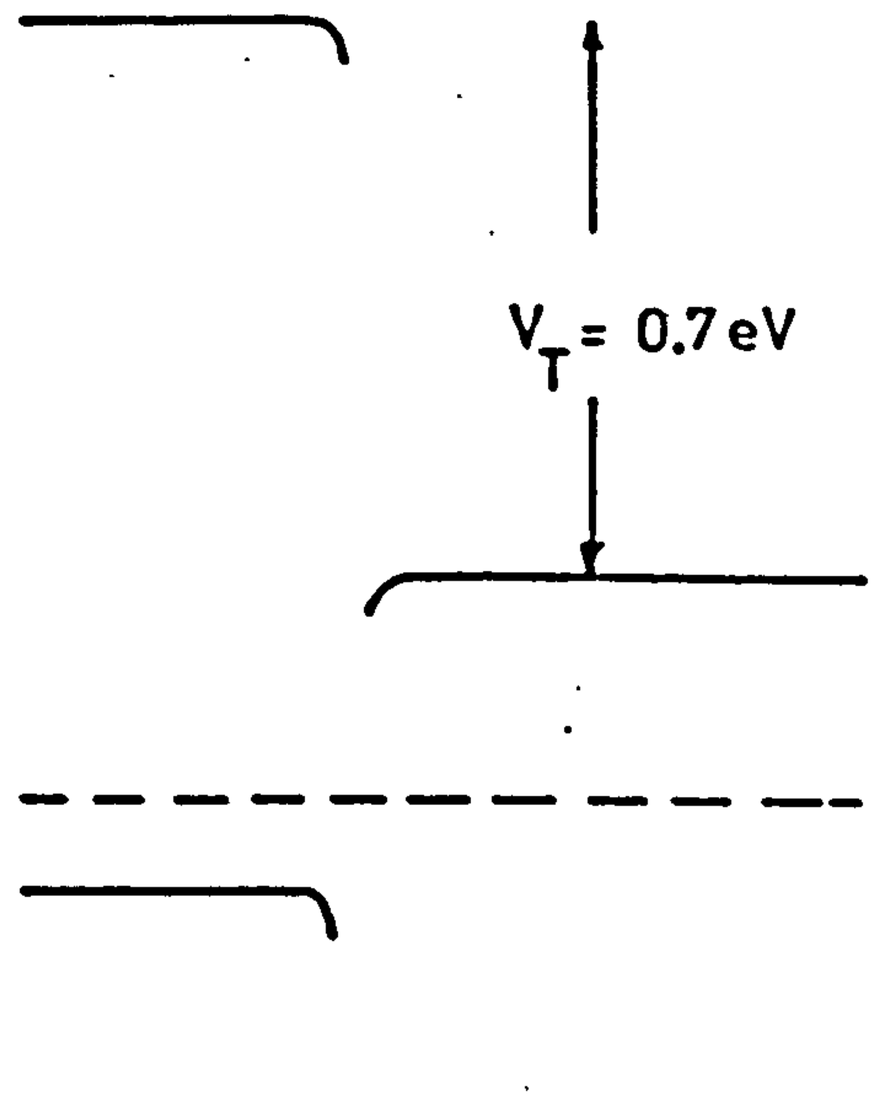


Fig 7.22 Optical Response Time Measurement

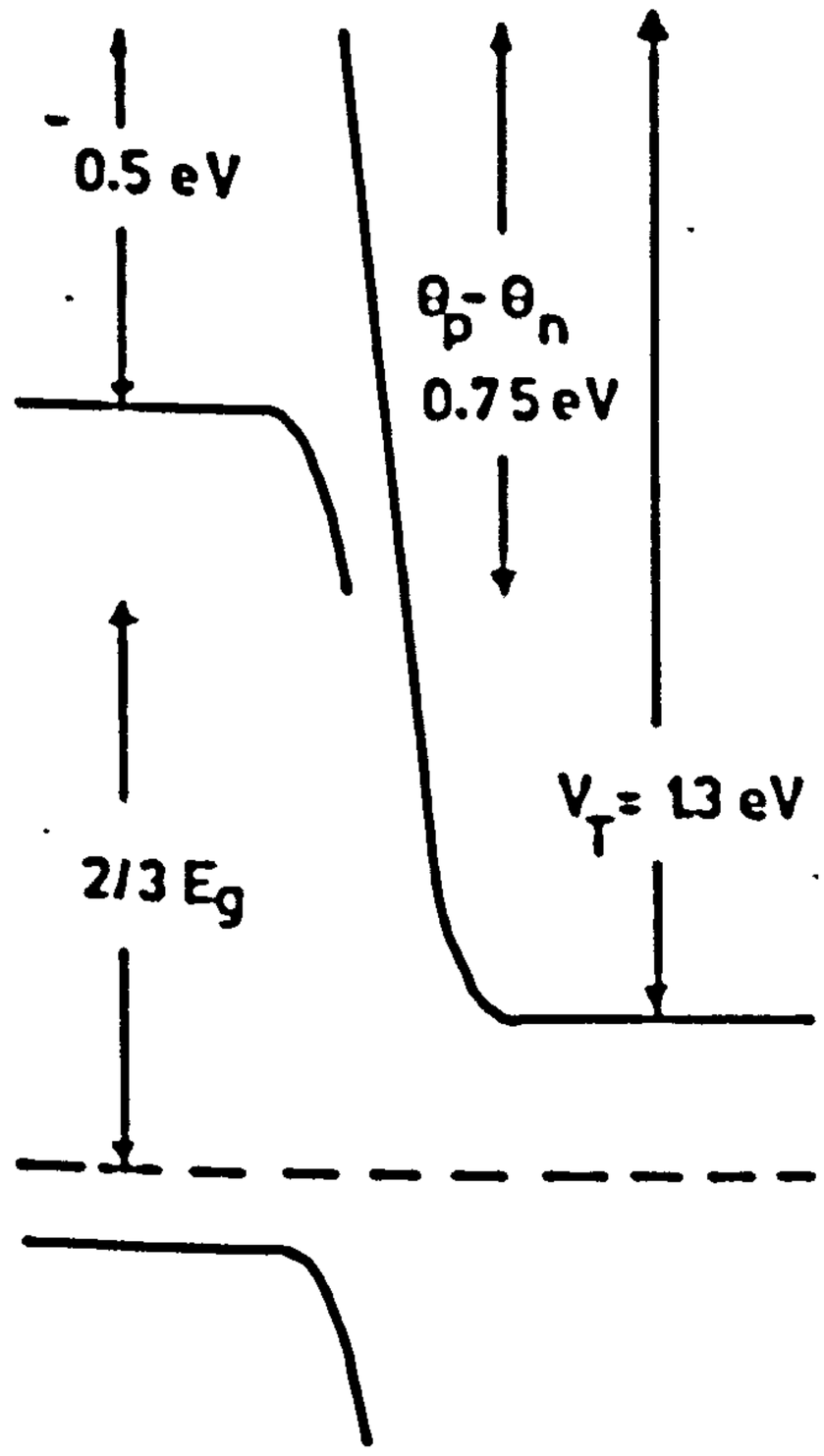
$N_A = 3 \times 10^{17}\ cm^{-3}$



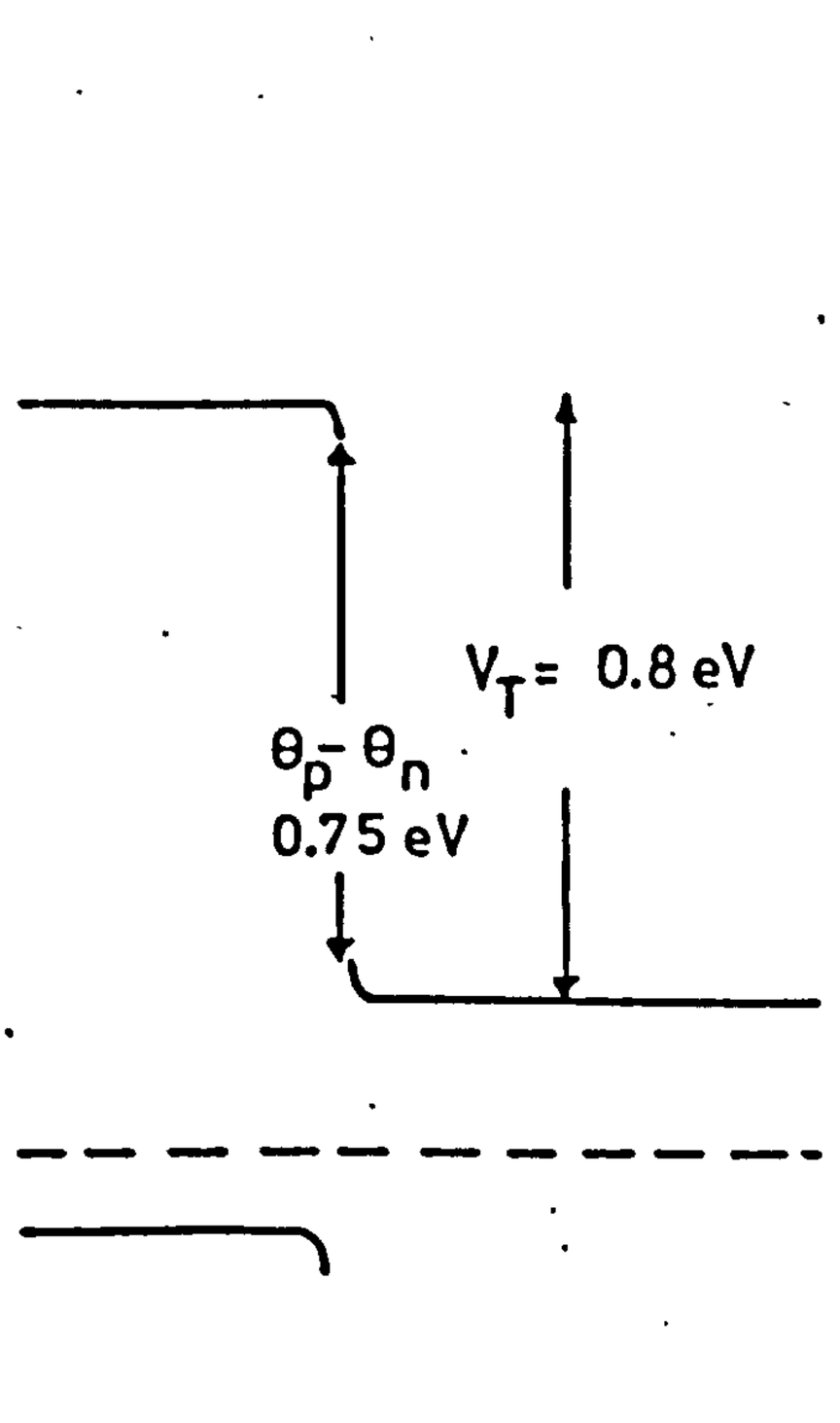
(a) Surface States



(b) No Surface States



(c) Surface States



(d) No Surface States

Fig 7.23 Band Diagram

of band bending at the interface. Figure 7.23(c) and 7.23(d) illustrates a possible situation which may arise if the Fermi level is 0.2 eV below the conduction band rather than 0.3 eV. Both the Si and CdS junction regions are depleted in Figure 7.23(d), the case without surface states. Figure 7.23(c) again shows that both junction regions are depleted but in this case there is, in addition to the barrier potential of 0.8 eV illustrated in Figure 7.23(d), a negative reverse barrier potential of 0.5 eV. As mentioned in Chapter 3, as this reverse barrier potential is determined by the difference in the electron affinities, it is questionable whether bulk electron affinities are applicable in this case.

The I-V characteristics are given by Figure 7.24. The characteristics have very high n values in both forward and reverse bias compared with Case 1, 2, and 3 heterojunction, approximately 40 times greater. The characteristic is similar to what might be expected by connecting two diodes with low breakdown voltages back to back. Equations 3.22 and 3.23 can be used to see if there is any agreement between the proposed reverse barrier model illustrated in Figure 7.23(c). The factor in the exponent, i.e. m/(m+1) in equation 3.22, must be modified to include the factor n to allow for recombination i.e. the factor becomes m/(m+1)n ; the same modification is made to equation 3.23 although the n factors for forward and reverse bias may be different. If the simplifying assumption that the n values are the same is made then, using the experimental values of "n" given by the I-V characteristics one can write:

$$\left(\frac{m}{m+1}\right)\cdot\frac{1}{n} = \frac{1}{176} \qquad (7.5)$$

$$\left(\frac{m}{m+1}\right)\cdot\frac{1}{n} = \frac{1}{215} \qquad (7.6)$$

Solving 7.5 and 7.6 gives the values of m and n as 1.22 and 97 respectively. The m value of 1.22 implies that the voltage distribution across the CdS

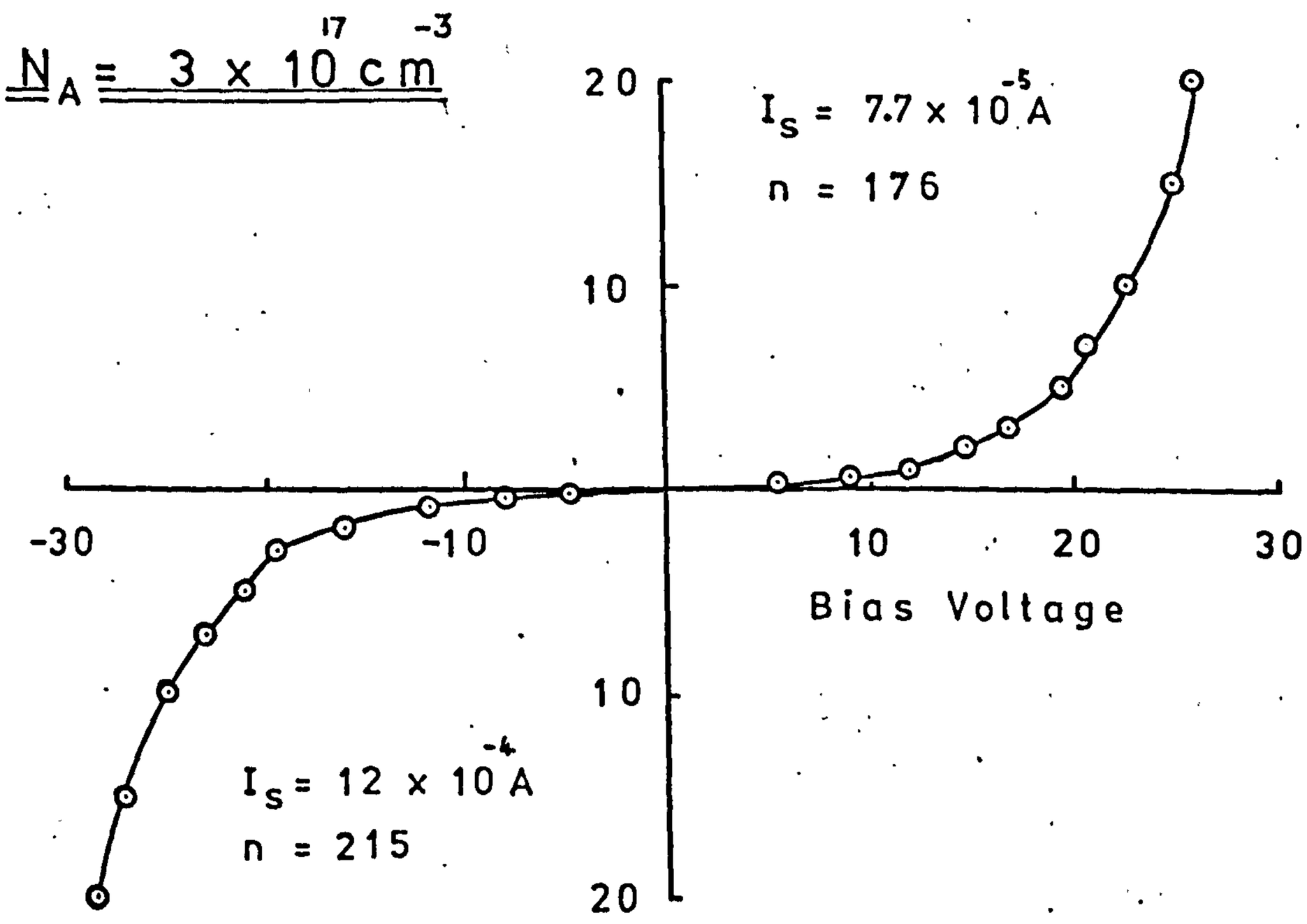


Fig 7.24 I-V Characteristic

and Si junction regions is approximately the same (equation 3.20). However, this in turn implies that the doping levels in the CdS film and the Si substrate are approximately the same. As the doping level in the silicon is known to be 3×10^{17} cm^{-3} (four point probe measurement) and the doping in the CdS film is thought to be in the region of 10^{13} to 10^{14} cm^{-3} this does not appear to agree with the measurements, i.e. $m \approx 10^{4}$ would be obtained using equation 3.20. The value of 97 for n is also very much higher than previous values for Case 1, 2 and 3 diodes. It does not seem possible to say which of the band models is appropriate to the Case 4 heterojunction diodes from the I-V characteristics.

Figure 7.25 gives the results of the photo characteristics for this case. The sensitivity increases with increasing reverse bias i.e. widening of the depletion region in the silicon. The quantum efficiency of the photodiode is very low because of the narrow depletion region in the silicon. It is worthwhile using equations 7.2 and 7.3, on the assumption of an abrupt one-sided junction, to obtain an estimate of the depletion width w and theoretical maximum photocurrent. Equation 7.2 gives the depletion width w, at -3.0 volts reverse bias, as 0.12 μm significantly less than the 0.71 μm depletion width estimated for Case 3. Hence, with an optical power of 1 mW, exp $-\alpha w$ is 0.94 and the theoretical photocurrent is 490 μA. Therefore, the photocurrent of 490 μA is considerably more than the measured photocurrent of 0.075 μA, a quantum efficiency of .015% based on the maximum theoretical value. These results indicate that the depletion width in the silicon may be much narrower than the 0.12 μm predicted and that most of the applied voltage is across the CdS junction because of the large difference between the theoretical and experimental values, i.e. implying that the one-sided junction approximation is not valid in this situation.

The capacitance versus bias characteristics are given by Figure 7.26.

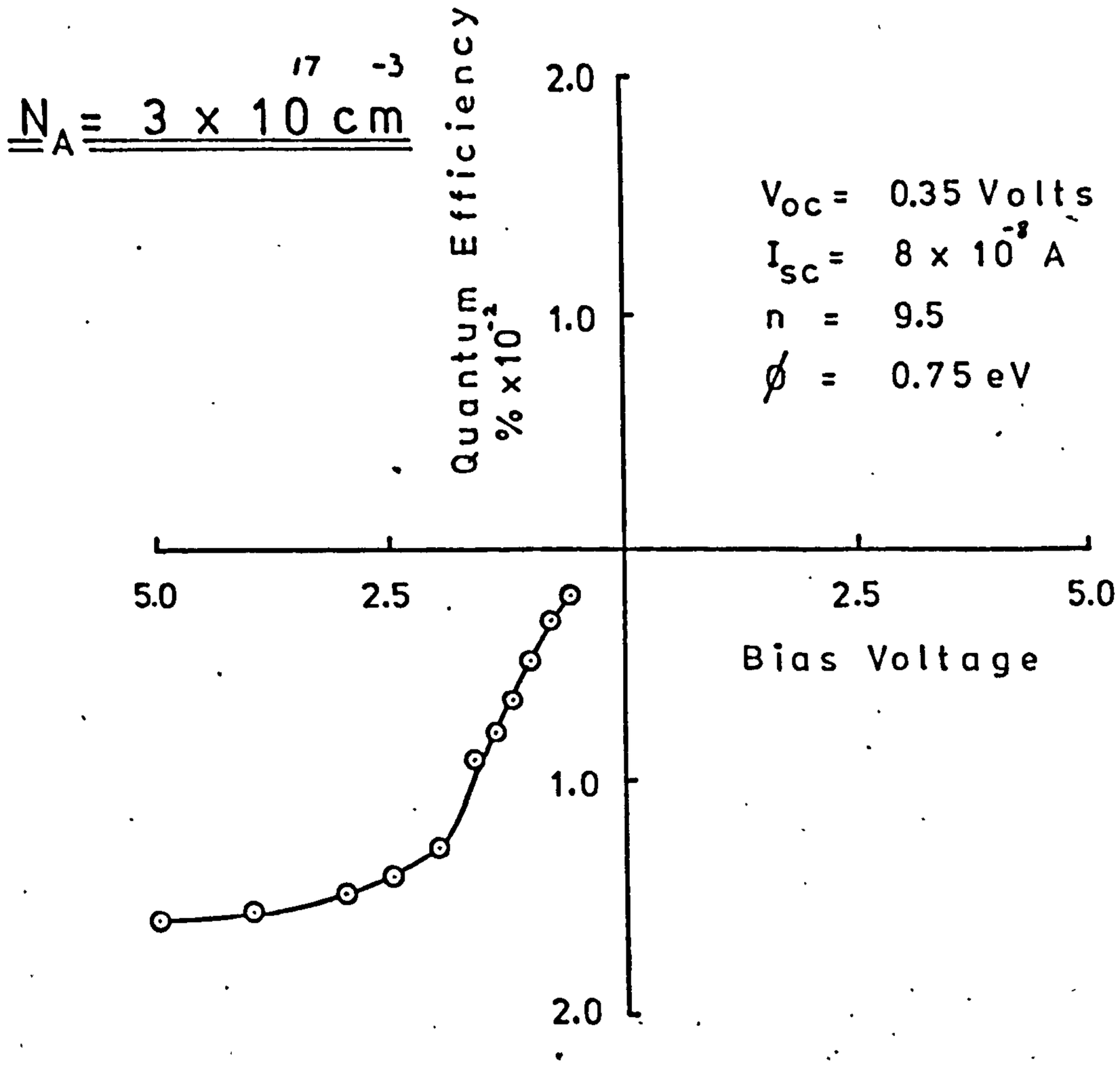


Fig 7.25 Photo Characteristic

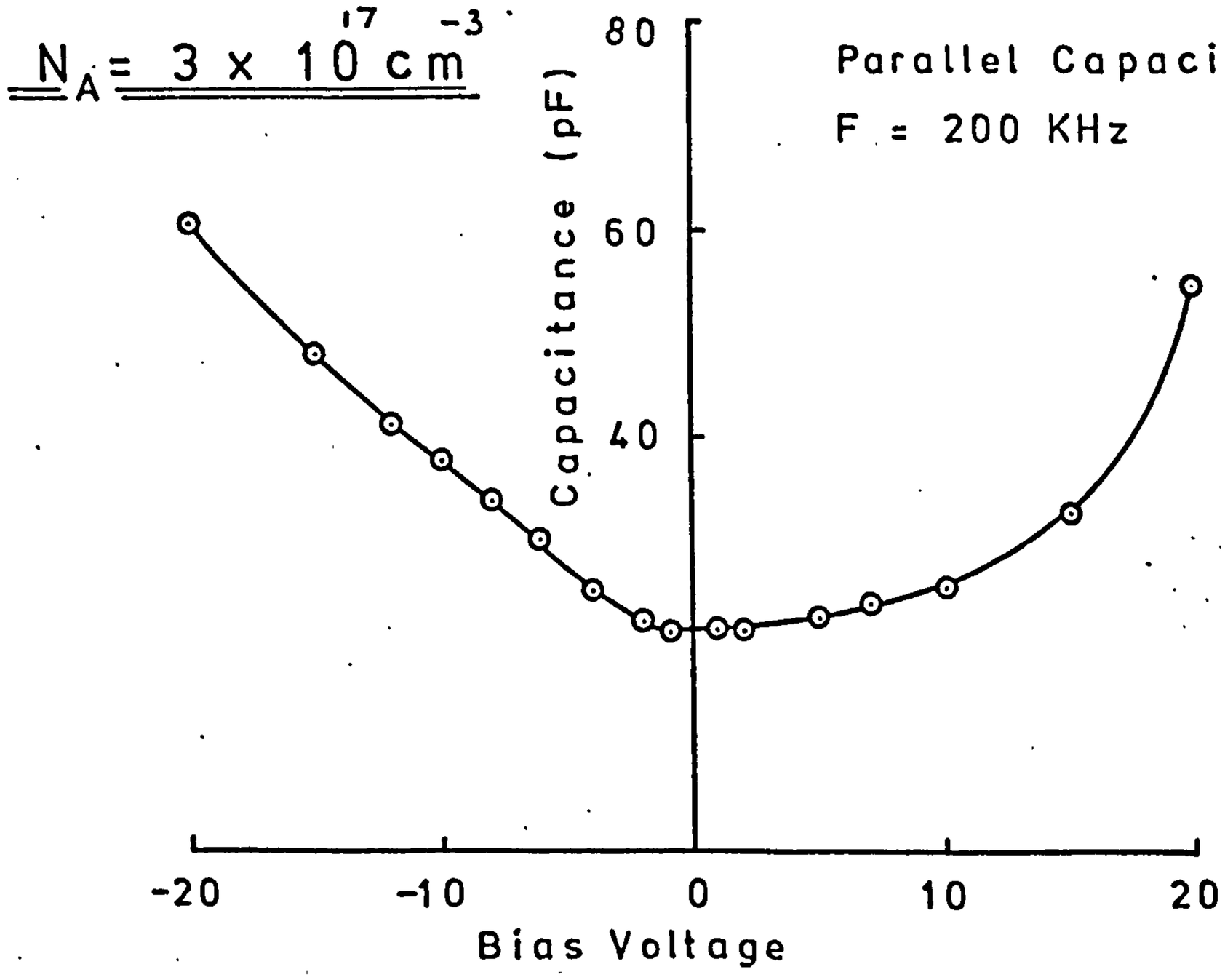


Fig 7.26 Capacitance Voltage Characteristic

They show that the capacitance is a minimum at zero bias and increases with both forward and reverse bias i.e. the depletion region in either the Si or CdS junctions is narrowing with bias. The behaviour of the capacitance results, like the I-V measurements, could be explained by two diodes back to back i.e. one of the diodes would be forward biased and of high capacitance with say forward bias; while the other diode would be forward biased and of relatively high capacitance with reverse bias.

It is clear that the measurements of the Case 4 diodes are not explained completely by the simple band models presented in Figure 7.23(a),(b),(c) and (d). In some respects the model given in 7.23(c) with the high negative barrier potential may explain the very poor photodetection properties. However, the experimental results do not fit the solutions of equations 3.22 and 3.23.

There was some experimental evidence to suggest that the aluminium electrodes evaporated onto the CdS, for Case 4 heterojunction diodes with N_A of 3×10^{17}, did not always provide an ohmic contact. It was found that if the incident radiation was focussed at the edge of the ring electrode rather than in the centre a substantial increase in photocurrent (50 times) was observed with Case 4 heterojunction photodetectors. This effect may be the result of a barrier contact between the aluminium and the CdS. Bube[90] gives some details of investigations on electrodes on CdS crystals. These investigations showed that ohmic contacts could be made to CdS crystals with a variety of metals if the contact area were first either subjected to electron bombardment or ionic bombardment by an electric discharge. These results are in accord with thinking of the contact barrier as caused by surface states on the CdS itself; the bombardment formed a high-conductivity surface layer through which ohmic contact to the CdS could be made. The observation that a neutral

or reducing atmosphere increased the effect of the bombardment, whereas an oxidising atmosphere hindered it, suggested that the effect was associated with the reduction of surface layers and with the formation of sulphur vacancies. Oxygen which may diffuse into CdS evaporated layers usually acts like an acceptor i.e. a p-type layer is formed. Experiments carried out by W. M. Tsang, of this department, on nCdS-pSi heterojunction solar cells showed that the short circuit photo-current increased by 50% when the devices were heated to 400°C in a reducing atmosphere.

It would be worthwhile evaporating metal contacts onto the CdS films deposited on silicon of $N_A = 3 \times 10^{17}$ cm^{-3} prior to removal of the device from the vacuum system to discover whether there was any change in the characteristics. In any case, this silicon doping would not be chosen for a heterojunction device to be used for photodetection applications.

7.4 Summary

The experimental results show that, as the doping in the silicon increases, the depletion region in the silicon decreases, reducing the efficiency of heterojunction photodetectors from the maximum quantum efficiency of 40% for the Case 1 heterojunction diode to 0.02% for the Case 4 diode. The Case 4 diode which may have a reverse barrier is very inefficient as a photodetector. The band model which includes surface states predicts the behaviour of the I-V, Iph-V and C-V characteristics for Case 1, 2 and 3 diodes.

The calculations of the barrier potentials from the photo-characteristic are in reasonable agreement with the model which includes surface states.

Capacitance and spectral response measurements have provided

evidence of several traps and their positions in the band gap. The n factors, obtained from the I-V characteristics in forward bias, indicate that trapping and recombination mechanisms are dominant. The n factors with values in excess of 2 are thought to be due to the fact that there may be trapping and recombination centres at more than a single energy level in the CdS energy gap.

The experimental measurements on devices fabricated from silicon substrates which have not been thermally cleaned, when compared with those which have, show that thermally cleaned devices have better and more predictable characteristics.

CHAPTER 8 CONCLUSIONS

8.1 Conclusions from Measurements and Results

It has been shown that the photodetection and I-V characteristics of nCdS-pSi heterojunctions are determined by:

(i) the film growth processes since they determine the structural quality of the film, and

(ii) the acceptor doping of the Si substrates, since this determines the junction potential barrier.

It has been shown that both the orientation of the substrate and the degree of surface cleanliness control the growth characteristics of the resulting CdS film and that such control yields films with transport properties approaching those of bulk crystals. It has been established from X-ray analysis and Hall mobility measurements that epitaxial films of CdS are obtained on suitably prepared (111) oriented silicon substrates. In addition, the substrates must be thermally cleaned at temperatures in excess of 800^{o}C, and at pressures of less than 10^{-7} torr to ensure the removal of both the residual SiOx and absorbed impurities. X-ray back reflection Laue photographs show that epitaxial CdS films of the wurtzite structure are obtained under these conditions. Both X-ray and transmission electron diffraction techniques indicated that polycrystalline CdS films were obtained on (100) oriented silicon substrates under similar growth conditions.

Experiments showed that the sensitivity of the heterojunction photodetectors decreased with increasing p-type silicon doping. This reduction in sensitivity was a result of the decreasing width of the depletion region in the silicon and it was further shown that the depletion width w must be larger than the reciprocal of the absorption

coefficient α to ensure that the term exp $-\alpha w$ is small compared with unity. The quantum efficiencies at 600 nm ranged from around 40% for the Case 1 diode ($N_A = 6 \times 10^{12}$ cm^{-3}) to around 0.02% for the Case 4 diode ($N_A = 3 \times 10^{17}$ cm^{-3}). It is thought that the low quantum efficiency for the Case 4 diode cannot be attributed entirely to the narrow depletion region in the silicon but may also be influenced by a barrier contact to the CdS. The heterojunction photodiodes compared favourably with a commercial silicon p-i-n photodiode which had a quantum efficiency of 38% at 600 nm. Measurements of the spectral response showed the "window effect", a characteristic of a heterojunction in which the CdS film behaves as a window to incident optical radiation at energies less than the band gap value of 2.43 eV. The window effect was modified by absorption associated with structural defects in the CdS film.

The band model, which included the effect of surface states, gave a simple but valuable insight into the physics of the nCdS-pSi hetero-junction and was found useful in interpreting some of the experimental results. The reversal of the photosensitivity and I-V characteristics for the Case 1 diode ($N_A = 6 \times 10^{12}$ cm^{-3}), for example, could be associated with the accumulation region in the silicon predicted by the band model. Fair agreement was found between the theoretical and experimental values of barrier potential. It was more difficult to explain the results of the Case 4 diode ($N_A = 3 \times 10^{17}$ cm^{-3}) because of the doubt as to which barrier model was applicable. In addition, there was some experimental evidence to suggest that there may have been a non-ohmic contact to the CdS in this case. If there were a barrier contact, it should be possible to estimate the value of the barrier height by focussing the incident light close to the contact region and plotting the square root of the photocurrent per incident photon as a function of wavelength.

The extrapolated value of wavelength (energy) at zero photocurrent would then give the barrier height of the aluminium -CdS contact.

Capacitance versus frequency measurements which show dispersion have indicated that traps were present. Optical measurements, i.e. photosensitivity as a function of wavelength, have shown that the traps were predominantly in the electron-beam evaporated CdS films and that the three different trap energy levels present were due to defects in the film resulting from non-stoichiometric growth. These traps can act as recombination centres reducing the sensitivity of the heterojunction, since optically generated carriers recombine before reaching the junction and so cannot contribute to the photocurrent. However, although traps were present in the CdS films, quite respectable quantum efficiencies were measured for the Case 1 and 2 heterojunction photodetectors.

Perhaps the most serious limitation of the nCdS-pSi heterojunction as a photodetector, in some applications, is the poor response time. The fastest rise time, in response to an optical pulse, was 0.5 μs for a Case 2 diode with -1.0 volts reverse bias. The poor response time is thought to be a result of the high density of traps in the CdS film. The fact that X-ray results showed that epitaxial films could be grown under certain conditions does not mean that the films were without defects which could act as trapping and recombination centres.

8.2 Applications

An application for which the nCds-pSi heterojunction appears suitable, even at the present state of the art, is the solar cell. It has been shown by Livingstone et al.[137] that the small area photodetectors investigated in this work have power conversion efficiencies of up to 12% under A.M.1 conditions. The advantage of a heterojunction solar cell is that, in principal, the incoming radiation is not absorbed by the n-type CdS film, while in a p-n silicon homojunction the nSi

region must be very thin to avoid significant absorption of the light and also recombination of the generated carriers before reaching the p region. The power conversion efficiencies for the small area devices (1 mm^2) ranged from about 5% for the Case 3 diode to 12% for the Case 1 diode while efficiencies never exceeded 3% for larger area devices (1 cm^2). The lower efficiency observed with the larger area cells was thought to be due to lateral resistance loss in the film. It would be possible to improve on the 12% conversion efficiency quoted, both by reducing the silicon substrate thickness, thus reducing a significant series resistance, and also by reducing the trap density in the CdS films.

Work on nCdS-pSi heterojunction photodetectors arose initially out of experiments by Stanley and Duncan[138] on the use of CdS films as planar optical waveguides (for light at 1.1 μm wavelength); and of CdS-Si heterojunctions as "integrated-optical" photodetectors for visible light. In the integrated optical photodetector device, light was guided to illuminate the junction along a thin-film sputtered 7059 glass waveguide. Although the device appeared to be reasonably sensitive, it was recognised at an early stage that there was a need to investigate and optimise photodetector properties such as quantum efficiency and response time. As the work presented in this thesis has shown, the nCdS-pSi heterojunction has a comparable sensitivity with commercially available silicon p-i-n photodetectors, its use however is likely to be restricted to frequencies below 1 MHz because of the defects in the CdS films.

8.3 Future Work

It is thought that no further significant improvements in CdS film structural quality may be obtained by the method of electron-beam

evaporation from compound CdS crystals. While it is a very convenient method, a serious disadvantage is that it is not possible to control the vapour pressures of S_2 molecules and Cd atoms independently. The growth of CdS under such non-equilibrium conditions results in significant non-stoichiometry, the films having high defect densities which can act as trapping and recombination centres. A technique called molecular beam epitaxy (M.B.E.) is a possible method of obtaining higher quality films. Because separate sources of sulphur and cadmium are used it should be possible to control independently the vapour pressures of S_2 and Cd using mass spectrometer monitoring facilities. It is also thought that carrying out evaporations at even lower pressures, of the order of 10^{-9} torr or less, will reduce the contamination level still further and may improve the film structure. More sophisticated methods of film analysis such as L.E.E.D. and Auger would give information regarding the cleanliness of the silicon surface and structural perfection and also information during the CdS film deposition itself. It would be worthwhile developing an etching method for obtaining thinned (111) oriented silicon specimens for transmission electron diffraction studies. The transmission electron diffraction technique would be valuable in the investigation of the nucleation of epitaxial CdS films. Nucleation studies are important in the context of a heterojunction because when the properties of the CdS film in the interface region are significantly different from those of the "bulk" of the CdS film, the device characteristics may be influenced. It is possible that, although the X-ray back reflection Laue technique indicated that epitaxial films of 1-2 microns grew under the conditions described, that the initial layer, perhaps of several hundred Angstroms, may be polycrystalline. It seems probable, however, that there must be some disorder at the interface as a result of the lattice mismatch (approximately 7%) between the silicon and CdS lattices. In addition, there is experimental evidence to show that Si is chemically attacked

by the S_2 and Cd vapour. Again, this may have a significant effect on the heterojunction characteristics.

The work has indicated (Case 4 diode) that great care is necessary when making electrical contacts to CdS. It might be worthwhile evaporating metal contacts onto the CdS film before removing the heterojunction from the vacuum system to avoid oxygen diffusing into the surface. The fabrication of the heterojunction with a guard-ring, a method used to reduce edge leakage effects in p-i-n photodiodes, may also improve the device characteristics.

Since it is clear that defects in CdS films are a problem it would be sensible to extend the measurement techniques to estimate the number of traps present as well as their position in the CdS band gap. Milnes,[135] for example, describes a method for obtaining the trap densities from the capacitance versus frequency characteristic with an applied bias voltage.

The power conversion efficiencies of up to 12% when the heterojunction was used as a solar cell are very encouraging. Significant reduction in weight, cost and series resistance would be possible if thin epitaxial silicon films were used as the substrate material. It may well be that a polycrystalline thin film heterojunction of nCdS and pSi, albeit with a lower conversion efficiency than an epitaxial thin film device, may be a good compromise between efficiency, cost and weight considerations.

It is clear from the work described in this thesis that improvements in substrate preparation (thermal cleaning) have improved the quality of the CdS films and in turn the characteristics of the nCdS-pSi heterojunction photodetectors. However, it is important to make the distinction between the CdS film itself and the complete photodetector. While it may be possible to produce defect-free epitaxial films using suitable growth techniques, this does not guarantee significantly improved heterojunction

characteristics The nCdS-pSi heterojunction photodetector is very sensitive, with quantum efficiencies up to 40% at 600 nm. In solar cell applications it has shown power conversion efficiencies of up to 12% and can probably be improved still further by using thin film silicon substrates and a better CdS film growth technique. The photodetector could also be used in other applications at frequencies less than 1 MHz.

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