ALGAN/GAN BASED ENHANCEMENT MODE MOSHEMTS

BY

ABHISHEK BANERJEE

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DEDICATION

This thesis is dedicated to my parents Achintya Kuman Banerjee and Manjusri Banerjee

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ABSTRACT

This thesis describes a new gallium nitride (GaN) based transistor technology for electronic switching applications. Conventional GaN based transistors are of the high electron mobility transistor (HEMT) type and are depletion mode devices. These are not suitable for switching applications since an extra DC supply is required to bias the device in the cut-off (off-state) region and the devices are not fail-safe, i.e. incase of malfunction a short-circuit can exist between the main DC supply and ground. Enhancement mode (E-Mode) or normally-off devices can overcome these limitations and if realized in the GaN material system would benefit from the good material properties that support large breakdown voltages and low On-resistances.

Fabrication of high performace E-mode GaN devices with low On-resistance and high breakdown voltage still remains a big challenge to date. In this thesis a new method for realizing enhancement mode aluminium gallium nitride - gallium nitride (AlGaN/GaN) devices using a localized gate-foot oxidation has been described. Thermal oxidation of the AlGaN barrier layer converts the top surface/part of this layer into aluminium oxide (Al_2O_3) and gallium oxide (Ga_2O_3), which serve as a good gate dielectric and improve the gate leakage current by several orders of magnitude compared to a Schottky gate. The oxidation process leaves a thinner AlGaN barrier which can result in normally off operation. Without special precaution, however, the oxidation of the AlGaN barrier is not uniform

from the top but occurs at higher rates at the defect/dislocation sites. This makes it impossible to control the barrier thickness and so rendering the barrier useless. To avoid the problem of non-uniform oxidation, a thin layer of aluminum is first deposited on the barrier layer and oxidized to form aluminium oxide on top. This additional oxide layer seems to ensure uniform oxidation of the AlGaN barrier layer underneath on subsequent further oxidation. Results of the fabricated 2 μm x 100 μm AlGaN/GaN MOS-HEMTs with a partially oxidized barrier layer showed a threshold voltage of -0.5 V (compared to -3.1 V for a Schottky devive fabricated on the same epilayer structure) and a maximum drain current of $\backsim 800mA/mm$ at high gate bias of 5 V with very little current compression. The peak extrinsic transconductance of the device is 160 mS/mm at a drain-source voltage of 10 V with a very low specific On-resistance of 9.8 $m\Omega.mm^2$ and an off-state breakdown voltage higher than 42 V. Capacitance-Voltage (C-V) measurements of $Al_2O_3/AlGaN/GaN$ circular test metal-oxide-semiconductor structures were observed and measured. They exhibit no hysteresis, indicating the good quality of the thermally grown aluminium oxide for realizing AlGaN/GaN based E-Mode devices for high frequency and high power applications.

PUBLICATIONS

[**1**] Currently working on a patent application with University of Glasgow to protect the idea of fabricating E-Mode devices using localized gate foot oxidation.

[**2**] Abhishek Banerjee, Sanna Taking and Edward Wasige, "Development of AlGaN/GaN Enhancement Mode MOSHEMTs using Localized Gate-Foot Oxidation," European Microwave Conference, Sept 2010. (Paper Accepted)

[**3**] Abhishek Banerjee, Sanna Taking, Douglas MacFarlane and Edward Wasige, "Enhancement Mode GaN based MOSHEMTs," ARMMS-The RF and Microwave Society, RF and Microwave Society, April 2010.

[**4**] Abhishek Banerjee, Sanna Taking, Faiz Rahman and Edward Wasige, "Process Development for High Al-content GaN HEMTs," UK Semiconductors Conference, Sheffield, 2008.

[**5**] Sanna Taking, Abhishek Banerjee, Haiping Zhou, Xu Li, Ali Khokhar, Richard Oxland, Ian McGregor, Steven Bentley, Faizal Rahman, Ian Thayne, Amir Dabiran, Andrew Wowchak, Bentao Cui and Edward Wasige, "Surface passivation of AlN/GaN MOS-HEMTs using ultra-thin Al2O3 formed by thermal oxidation of evaporated aluminium," Electronics Letters, Vol. 46, No. 4, 2010, pp. 301-302.

[**6**] Sanna Taking, Abhishek Banerjee, Faiz Rahman and Edward Wasige, "Low Resistance Ohmic Contacts for AlN/GaN HEMTs," UK Nitride Consortium, Sheffield, 2008.

[**7**] Faiz Rahman, Sun Xu, Ian M. Watson, Dinesh Kumar Baid Mutha, Richard K. Oxland, Nigel P. Johnson, Abhishek Banerjee and Edward Wasige, "Ohmic contact formation to bulk and heterostructure gallium nitride family semiconductors," Applied Physics A: Materials Science Processing, Vol. 94, No. 3, 2009, pp. 633-639.

ABBREVIATIONS AND ACRONYMS

2DEG: two dimensional electron gas

AC: alternating current

Al: aluminium

AlN: aluminium nitride

AlGaAs: aluminium gallium arsenide

AlGaN: aluminium gallium nitride

Ar: argon

Au: gold

C-V: capacitance voltage

CMOS: complementary metal oxide semiconductor

DCFL: direct coupled FET logic

DC: direct current

DHEMT: double high electron mobility transistor

DHFET: double heterojunction field effect transistor

D-Mode: depletion mode

E-beam: electron-beam

E-Mode: enhancement mode

FET: field effect transistor

GaAs: gallium arsenide

GaN: gallium nitride

HBT: heterojunction bipolar transistor

InAlGaN: indium aluminium gallium nitride

ICP: inductive coupled plasma

IGBT: insulated gate bipolar transistor

InN: indium nitride

IPA : isopropyl alcohol

I-V: current-voltage

JFoM: Johnson figure of merit

MBE: molecular beam epitaxy

MOCVD: metal organic chemical vapour deposition

MOS: metal oxide semiconductor

MOSHEMT: metal oxide semiconductor high electron mobility transistor

MOSFET: metal oxide semiconductor field effect transistor

Ni: nickel

PFoM: power figure of merit

QW: quantum well

RF: radio frequency

RIE: reactive ion etching

RTA: rapid thermal annealer

Si: silicon

SBFL: super buffer FET logic

SEM: scanning electron microscope

SiC: silicon carbide

SPA: semiconductor parameter analyzer

Ti: titanium

TEM: transmission electron microscope

TLM: transmission line method

UV: ultraviolet

WBG: wide band-gap

LIST OF CONSTANTS AND CHEMICAL SYMBOLS

Al_2O_3 : aluminium oxide

C_{13},C_{33}: stiffness constant (the subscripts refer to their respective crystal directions in the tensor)

C_G: gate capacitance

$(CH_3)Al$: trimethyl aluminium

$(CH_3)Ga$: trimethyl gallium

e: charge of electron

e_{33},e_{31}: piezoelectric constant (the subscripts refer to their respective crystal directions in the tensor)

E_C: conduction band energy

ΔEc: conduction band offset

E_c : critical electric field

E_f: Fermi level energy

$E_F(x)$: Fermi level with respect to conduction band edge

E_g: bandgap

E_v: valence band energy

f_{MAX}: maximum frequency of operation

f_T: unity current gain cut-off frequency

Ga_2O_3 : gallium oxide

G_M: transconductance

H_2: hydrogen

H_2O: water

I_D: drain current

I_{DS}: source-drain current

L_g: gate length

L_{SD}: source to drain length

L_T: transfer length of an ohmic contact

N_2: nitrogen

NH_3: ammonia

P_{PE}: piezoelectric polarization

P_{SP}: spontaneous polarization

R_C: ohmic contact resistance

R_{CH}: resistance of the channel region under the gate-foot

R_d: drain resistance

R_{DS}: drain-source resistance

R_{GD}: resistance of the active region between gate and drain

R_{GS}: resistance of the active region between gate and source

R_{ON}: on resistance of a device

R_S: source resistance

R_{SD}: source-drain resistance of a device

R_{SH}: sheet resistance

V_{BR}: breakdown voltage

V_{DS}: drain source voltage

V_{FB}: flat band voltage

V_{GS}: gate source voltage

V_P: pinch-off voltage

V_{TH}: threshold voltage

V_x: effective voltage in the channel

SF_6: sulphur hexafluoride

Si_3N_4, SiN: silicon nitride

t_{OX}: thickness of oxide

T_{OX}: oxidation time

W_g: gate width

x_0: initial thickness of an oxide film

v_{sat} : saturation electron velocity

LIST OF GREEK SYMBOLS

ϵ_r: dielectric constant

μ_e: mobility

ϕ_b: Schottky barrier height

σ: polarization induced sheet density

ε_0: permittivity of vacuum

$\varepsilon(x)$: relative permittivity of the (alloy composition) barrier layer

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CHAPTER 1

INTRODUCTION

1.1 Overview

Semiconductor power devices play a significant role in the modern world of power electronics and energy conversion with a current market exceeding billions of dollars. Applications of power electronics mainly include high voltage switching applications such as DC-AC inverters, DC-DC converters, electric induction heating, motor drives, switching power amplifiers, digital applications, etc. Development of power electronics is solely based on the improvement of the semiconductor power device itself, which are designed to switch high currents and blocking voltages at the same time being as fast and reliable as possible. Intrinsic properties of the semiconductors itself are the key factors in the improvement of the system performance in terms of efficiency, size, cost and complexity. An ideal switch must be able to switch high currents and voltages with minimal or no on-state or switching losses, ability to withstand high voltage and temperature, has a very high operational switching frequency and simplified gate drive circuitry [1],[2].

To date silicon has been the dominant semiconductor of choice for high voltage

switching applications. However, for high power and high frequency applications silicon devices fail to perform efficiently due to the limitations of their intrinsic material properties such as inversion layer mobility, low saturation velocity, low breakdown voltage and high device resistance [2]. These limitations of silicon devices have generated a strong motivation for researching wide bandgap semiconductors (WBG) such as gallium nitride (GaN) and diamond for high temperature and power switching applications. GaN-based metal oxide semiconductor high electron mobility transistors (MOS-HEMTs) benefit from superior material properties like high saturated electron velocity, high electric breakdown voltage and extremely low on-state resistance and very high frequency of operation and hence offer several potential advantages over silicon devices in the field of efficient switching (faster and low loss) operations. Furthermore, GaN grown on silicon carbide (SiC) or silicon (Si) substrates provide much better thermal conductivity than GaN grown on sapphire, which facilitates in draining out the dissipated power reducing cooling requirements. In order to realize faster and more efficient switching circuitry for such applications high efficiency semiconductor power switching devices have been a key research topic for the last few decades [1],[2],[3].

1.2 III-Nitride (GaN) Based Semiconductor Material

Wide band-gap III-Nitride semiconductor materials possess many superior material properties compared to conventional silicon (Si), gallium arsenide (GaAs),

indium phosphide (InP) or other III-V compounds. The major advantages of these nitride-based devices, which make them capable for high power and high frequency applications are high breakdown fields, high sheet carrier concentrations at hetero-junction interfaces, high electron mobility and saturation velocity, and low thermal impedance when grown on suitable substrates like 4H-SiC or bulk AlN [4],[5],[6]. Owing to these superior intrinsic properties, group III-Nitride semiconductors provide great promise for overcoming the fundamental limitations associated with silicon and GaAs semiconductors. III-nitrides are chemically inert and provide excellent temperature stability, which makes them more reliable for high temperature operation. They also find very useful applications in the field of power electronics as they allow for high power switching with sub micro and nano second switching times. The comparison between the material properties of GaN and common semiconductors is presented in Table 1.1 [7],[8].

III-N HEMTs (High Electron Mobility Transistors) are the most widely used devices for designing high speed devices for high power and high frequency applications due to their large bandgap, high output current and higher voltage handling capabilities. They consist of a high mobility buffer layer structure underneath a wider bandgap layer, which confines the majority carriers in a two dimensional (2D) quantum well formed at the hetero-junction due to the dissimilarity in the bandgap and the lattice structures. Hence, GaN based HEMTs offer a rugged and reliable technology for high frequency and high power applications such as RF,

Material	Dielectric Constant ϵ_r	Mobility μ_e, (cm^2/V.s)	Bandgap E_g, (eV)	Breakdown Voltage V_{BR} (V/cm)	Thermal Conductivity λ (W/cm.K)	Saturation Velocity,$\mathbf{v}_{sat}$ ($\times 10^7$ cm/s)
Si	11.4	1300	1.1	6.0×10^5	1.5	1
GaAs	13.1	8500	1.4	6.5×10^5	0.46	1
GaN	9.5	1500	3.4	3.5×10^6	1.7	1.5
SiC	10.1	1000	3.2	3.5×10^6	4.9	2
Diamond	5.5	2200	5.4	10.0×10^6	22	2.7

Table 1.1: Comparison of material properties of GaN and other semiconductors. [7],[8]

micro and millimetre wave amplifiers, radar and space electronics including base-station transmitters, Ku-Ka band (12 - 40 GHz) very small aperture terminal and broad-band satellites, local multipoint distribution systems, digital radio, military applications, inverter systems [6],[7], where the (output power) performance far exceeds any silicon or gallium arsenide based devices. Its high breakdown voltage enables it to work at high operating voltages like 28V and potentially up to 42V, hence reducing cost of the circuitry by eliminating the voltage step-down circuit [6].

1.2.1 Crystal Structure and Material Properties

Group III-nitrides crystallize in the stable hexagonal (wurtzite) structure or in the metastable cubic (zincblende) structure. However, the gallium nitride ma-

terial's crystal structure used in this project is a wurtzite structure and hence other GaN crystal structures are not discussed in this section. The so-called GaN wurtzite structure has a hexagonal cell. Under ambient conditions the wurtzite structure is the thermodynamically stable phase consisting of two interpenetrating hexagonal close-packed lattices, which are shifted with respect to each other ideally by $3/8 \cdot c_0$, where c_0 is the height of the hexagonal lattice cell. The bond between Ga and N atoms are predominantly covalent, however, the difference in the electronegativity of Ga and N atoms generate a significant ionic contribution to the bond. The GaN wurtzite crystal lattice lacks inversion symmetry along the [0001] or c axis, which is the direction vector pointing from a Ga atom to its nearest N atom along the c or [0001] axis. Lack of inversion symmetry in wurtzite GaN can be defined by an atom position on a close-packed plane with coordinates (x, y, z) which is not invariant to the position (-x,-y,-z), since inversion results in replacement of group III atoms (Ga) by nitrogen atoms and vice versa [9],[10],[11].

The wurzite GaN crystal is grown in the form of a structure that consists of alternating bi-atomic closely-packed diatomic planes of Ga and N pairs stacked in an ABABAB sequence along the wurtzite direction [0001] as explained in details in Reference [12]. The polarity of the crystal is based on the bonds parallel to the c-axis, namely whether they are from cation (Ga) sites to anion (N) sites or vice versa. Hence, GaN crystals can be grown with two distinctive polarities, Ga-face and N-face. Figure 1.1a and 1.1b show the GaN crystal structure [9],[10]. The

crystal structure grown along the c-axis ([0001] direction) and are called crystals with Ga-face polarity as shown in Figure 1.1a. Similarly those crystals, which are grown in the $[000\bar{1}]$ direction possess N-face polarity as shown in Figure 1.1b. In Ga-face crystals, the Ga atom is below the N atom, for N-face crystals we have the opposite. The wurtzite GaN crystal is generally defined by three parameters, edge length of the basal hexagon (a_0), the height of the hexagonal cell (c_0), and the cation-anion bond length ratio (u_0) along the [0001] direction in units of c_0. The subscript "0" indicates that these values are of the equilibrium lattice. For an ideal wurtzite structure the $c_0/a_0 = \sqrt{\frac{8}{3}} = 1.633$ and u_0 is 0.375 [10],[11]. Because in the difference in the metal cations in AlN, GaN and InN the bondlength and c_0/a_0 ratio varies. It is clear from Table 1.2 that the GaN crystal lattice is the closest to ideal wurtzite lattice followed by InN and AlN. The non ideality factor plays a significant role in determining polarization effects in III-N semiconductor materials.

In III-N semiconductors the presence of nitrogen plays an important part in determining the cation-anion bond properties in the crystal lattice. Due to strong electron affinity of N atom generated from its $1s^2 2s^2 2p^3$ electronic configuration, the Ga-N covalent bonds possess strong ionicity [11]. Although this ionic effect also exists in zinc-blende crystals such as GaAs and InP grown along [111] direction but it is much less pronounced because of the smaller ionicity of the covalent bond [11] due to the absence of the N atom. In III-nitrides, although the cova-

lent bond parallel to the c-axis is strongly ionic and is primarily responsible for the spontaneous polarization, the other three covalent bonds in the tetrahedral structure are also equally ionic. This ionic character combined with the crystal's non ideality factor gives rise to large polarization effects. Since this polarization occurs in III-N materials under zero strain it is known as spontaneous polarization. As the c_0/a_0 ratio decreases, the three in-plane covalent bonds forms a wider angle from the c-axis and their resultant compensation polarization decreases thus increasing the overall spontaneous polarization [11].

Apart from spontaneous polarization, additional polarization effects can also be introduced in the lattice structure through strain. If external stress is applied to the III-V lattice structure, the lattice parameters c_0 and a_0 of the crystal structure will try to modify itself to accommodate the stress thus changing the polarization strength. This additional polarization in strained III-V crystals is called piezoelectric polarization. It has been shown that piezoelectric polarizarions exerts a substantial influence on the 2DEG density and the electric field distributions in strained zinc blende semiconductors such as GaAs and InP grown in [111] orientation and in strained wurtzite III-N materials grown in [0001] orientation [10]. However, the magnitude of piezoelectric polarizarion in III-N materials are about five times higher than those seen in GaAs semiconductor materials [10]. If tensile stress can be applied by the growth of different metal-N crystals on top of another the net polarization increases as the piezoelectric and spontaneous polarizations

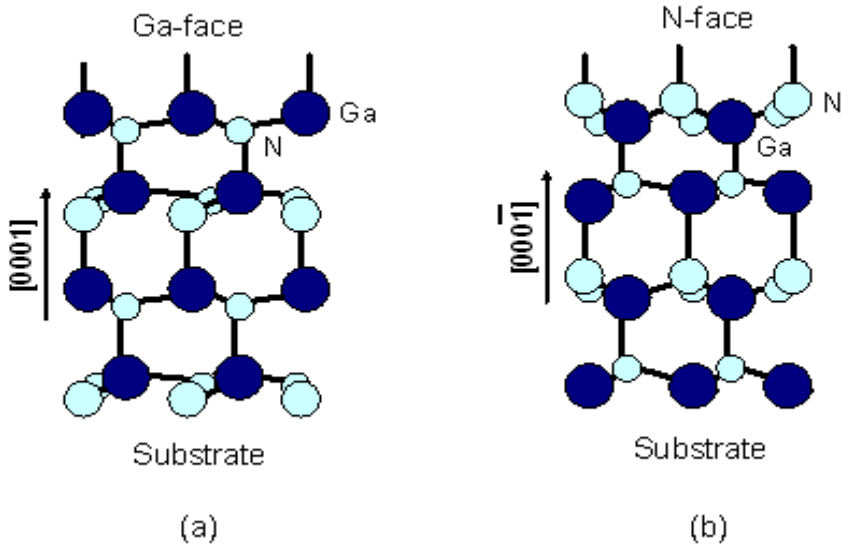


Figure 1.1: GaN crystal structure with Ga-face and N-face polarity [9],[10].

acts in the same direction. This is discussed in details in Section 2.3. The net polarization effects plays a significant role in determining the density of electrons in the two dimensional electron gas (2DEG) formed at the hetero-structure interface [10],[11].

GaN grown for device fabrication purposes are Ga-face due to their superior crystal properties over N-face structures. The material properties of AlN, InN and GaN including the energy band-gaps, dielectric constants, lattice constants, stiffness constants, piezoelectric constants and effective electron masses are tabulated in Table 1.2 [10],[11],[13],[14],[15]. Some of these values will be used in Chapter 2 in the computation of the properties of high electron mobility transistor structures formed from these materials.

Material Properties	**AlN**	**GaN**	**InN**
Band gap, E_g (eV)	6.2	3.44	0.6
Dielectric constant	8.5	8.9	15.3
Lattice constant, a_0 (nm)	0.3112	0.3188	0.354
Lattice constant, c_0 (nm)	0.4982	0.5185	0.5705
c_0/a_0 ratio (exp)	1.601	1.626	1.611
c_0/a_0 ratio (cal) [9]	1.6190	1.6336	1.6270
Stiffness constant C_{13} (GPa)	115	105	95
Stiffness constant C_{33} (GPa)	285	395	200
Piezoelectric constant e_{33} (C/m^2)	-0.58	-0.33	-0.22
Piezoelectric constant e_{31} (C/m^2)	1.55	0.65	0.43
Spontaneous polarization (C/m^2)	-0.081	-0.029	-0.032
Electron in-plane effective mass (m^o)	0.26	0.2	0.1
Electron normal effective mass (m^o)	0.25	0.2	0.1

Table 1.2: Material Properties of AlN, GaN and InN crystals [9],[10],[11],[12],[13].

1.3 Enhancement Mode (E-Mode) Devices

Conventional GaN based transistors are of the high electron mobility transistor (HEMT) type and are depletion mode (D-Mode) devices [5],[6]. These are not suitable for switching applications since an extra DC supply is required to bias the device in the cut-off (off-state) region and the devices are not fail-safe, i.e. in case of malfunction a short-circuit can exist between the main DC supply and ground. Enhancement mode (E-Mode), or normally-off devices can overcome these limitations and if realized in the GaN material system would benefit from the good material properties that support large breakdown voltages and low On-resistances.

Enhancement mode devices are those which have an open channel between the source and drain for any negative or zero voltage at the gate electrode. Enhancing the magnitude of the gate positive voltage increases the electric field and hence attracts more free electrons towards the gate. This in turn increases the density of the electrons in the channel and hence the current flow increases resulting in a higher drain output current. Since no channel is formed originally at the gate electrode the device is said to be normally off. The device begins to conduct with the application of a positive voltage at the gate and is therefore known as an enhancement mode or E-mode device. The minimum value of the positive gate voltage that creates the channel and facilitates electrical conduction is known as the threshold voltage of the device. This is illustrated in Figure 1.2 [16],[17].

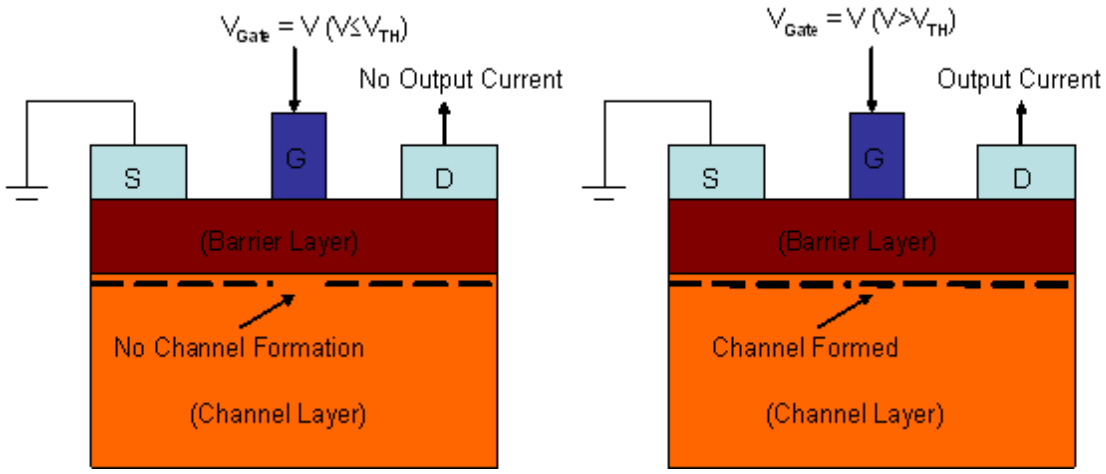


Figure 1.2: Operation principle of enhancement-mode devices.

1.4 Applications of Enhancement Mode devices

1.4.1 Why "Normally-Off" devices ?

Most of the development to date in GaN-based HEMTs has been focused on depletion mode (D-Mode) AlGaN/GaN devices which operate at negative gate threshold voltages. This is so because the basic AlGaN/GaN heterostructure creates a 2DEG channel which is used to conduct current in these devices. The 2DEG exists even without the application of the gate bias and a negative gate voltage must be applied to deplete the region under the gate of electrons to switch off the device. Conventional AlGaN/GaN devices are as such D-Mode or normally-on devices.

On the other hand, enhancement mode (E-Mode) devices operate only with positive gate voltages and there is no longer a need for a negative power sup-

ply which reduces the cost and complexity of the circuit. Unlike their D-Mode counterparts, E-Mode devices are highly advantageous in that they are fail-safe, i.e. if there is no input voltage from the preceding circuitry due to any failure the device acts as an open-circuit protecting any further damage to the circuitry [18],[19]. Primary applications of E-Mode devices include electrical inverters (DC-AC conversion, induction heating, motor drive control, automotive applications such as hybrid cars, variable frequency drives, etc.), switched mode power supplies (DC-DC converters, etc), motor driver circuits, logic circuits like direct coupled FET logic (DCFL), super buffer FET logic (SBFL), etc. For instance, the electric motors used in electric or hybrid cars are induction motors which require 3-phase AC input. The electrical energy for these vehicles is however stored in 12 V DC batteries. The DC-AC inverters required for this are usually implemented using insulated gate bipolar transistors (IGBTs) but could be much more efficiently done using E-mode GaN MOS-HEMTs. All these applications operate with positive gate voltages and require very low drain-source resistance (R_{DS}/R_{ON}) for high efficiency switching as they demand low on state conduction losses, high input impedance, thermal stability and high switching speeds in the order of sub micro and nano second range which can be comparable to their D-Mode equivalent switches, e.g. $\backsim$5 ns [16],[20],[21].

Properly engineered E-mode AlGaN/GaN switches would also benefit from other advantages of the GaN material system, i.e. high current capability and high

breakdown voltages, would make these devices very competitive in the market for switching applications.

1.4.2 Advantages of GaN over Conventional Technologies

GaN-based MOS-HEMTs are capable of transmitting high powers at high frequencies due to the wide band gap of GaN. The devices have higher breakdown voltages (V_{BR}) and hence the devices can be biased at higher drain voltages. Table 1.3 shows the key advantages of GaN over Si or GaAs from the material's intrinsic point of view [22] and Table 1.4 shows a comparison of typical switching parameters between GaN, GaAs and Silicon field effect transistors.

Figure of Merits are the parameters used to compare semiconductor devices for specific operations such as high power conversion, high operating frequency, high breakdown voltage, etc. Power Figure of Merit (PFoM) is the parameter used to compare high power devices of different semiconductor materials and is characterized by the device resistance and its breakdown voltage. Devices with high PFoM are very useful for high power conversion / switching applications. Figure 1.3 shows the comparison of Power Figure of Merit (PFoM) between GaN, GaAs and Silicon, which is plotted from an estimation based on the specific On-resistance (R_{ON})and breakdown voltage (V_{BR}) data from Table 1.4. The power figure of merit is defined as

$$PFoM = \frac{V_{BR}^2}{R_{ON}} \tag{1.1}$$

Similarly as PFoM, Johnson figure of merit (JFoM) is also used to characterize high power and high frequency semiconductor devices and is defined as

$$JFoM = \frac{E_c v_{sat}}{2\pi} = \frac{E_c}{2\pi}(2\pi L_G f_T) = E_c L_G f_T \tag{1.2}$$

where $v_{sat} = 2\pi L_G f_T$, L_G is the effective gate length, f_T is the unity-gain cut-off frequency, E_c is the critical electric field and v_{sat} is the saturation electron velocity [23],[24]. Since, both E_c and v_{sat} are directly proportional to the breakdown voltage V_{BR} and f_T, respectively, hence, keeping the effective gate length contant for different semiconductor materials the JFoM can be expressed as a plot presenting the difference between the semiconductors from their breakdown voltage and the cut-off frequency point of view as shown in Figure 1.4. Compared to Si and GaAs, GaN has (potentially) the lowest On-resistance, highest breakdown voltage and high frequency of operation as shown in Figure 1.3 and 1.4.

1.5 Motivation for Research

Fabrication of Enhancement-mode AlGaN/GaN HEMTs with a low On-resistance, high output current and a very high breakdown voltage still remains a big challenge. As will be discussed in this thesis a thin barrier layer (AlGaN) is ideal for normally off operation but the sheet resistance tends to increase with the decreasing barrier thickness, which in-turn gives a very high On-state resistance and low output current. Several research groups have been working on this specific topic since the last decade but so far none of them have been able to standard-

Material Feature	**Merits of Power Device**
Wide bandgap	High power High temperature operation High voltage operation High breakdown voltage High output impedance Better linearity
High carrier density, high mobility	High power density High frequency operation Low R_{ON} and smaller die area

Table 1.3: Key Advantages of GaN (3.4 eV) over Si (1.1 eV) or GaAs (1.4 eV).

Material	**On-resistance** ($\Omega.mm^2$)	$\mathbf{I}_{D,MAX}$ (mA/mm)	**Breakdown voltage** (V)	**Reference**
AlGaN/GaN	$\backsim 0.5-1$	>1000	$\backsim 100-1500$	[25],[26],[27]
AlGaAs/GaAs	$\backsim 0.2-1$	<500	$\backsim 10-60$	[28],[29],[30]
Silicon	$\backsim 1-100$	<100	$\backsim 20-680$	[30],[31],[32]

Table 1.4: Comparison of device parameters for switching applications.

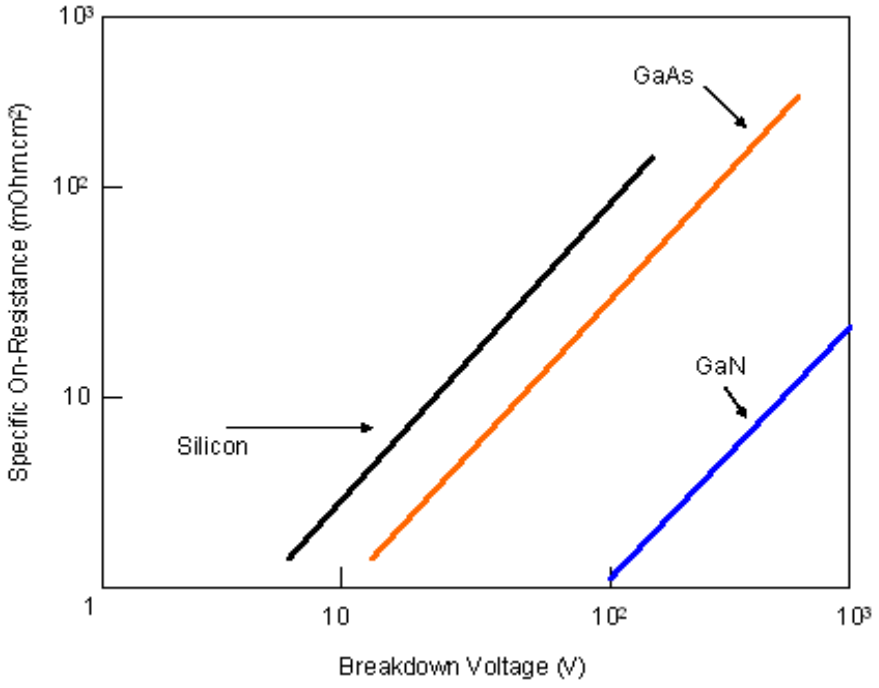


Figure 1.3: Power Device Figure of Merit between GaN, GaAs and Si.

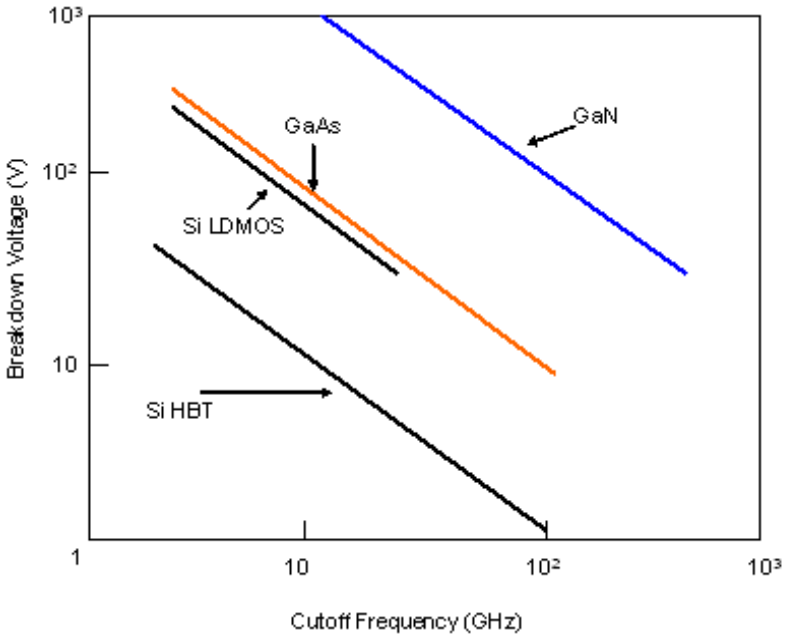


Figure 1.4: Johnson Figure of Merit between GaN, GaAs and Si.

ize a technology, which is reproducable and reliable. The approaches adopted by the various groups will be described in Chapter 3. The current methods used to fabricate "normally-off" devices mainly depend on techniques like gate-foot recessing etching [33],[34] or fluorine ion-implantation [17], which not only include complex fabrication steps but also require significant parameter control and expensive tools. Another major drawback of the conventional technologies is that they are non-uniform and involve a lot of post processing problems like increased surface roughness, instability of implanted ions, etc. Moreover, there is a significant loss of the semiconductor's current density post fabrication as compared to their depletion mode (D-Mode) equivalents.

The main motivation behind this project was to research a new technique to fabricate E-Mode devices that is reliable, reproducible, controlled and does not require expensive equipment. Also the method should be capable of providing E-Mode devices with very low On-resistance, high output drain current and high breakdown voltage.

1.6 Thesis Outline

This thesis is organized in the following way. Chapter 2 describes the basic operation mechanism of the AlGaN/GaN HEMTs. It provides a detailed description and the principle of formation of the two dimensional electron gas (2DEG).

Chapter 3 deals with the current E-Mode device fabrication technologies including their advantages and drawbacks including the state of the art E-Mode devices. It also provides a summary of the state-of-the-art GaN devices. Chapter 4 explains the fabrication procedure of a novel technique used to fabricate normally off devices on a standard AlGaN/GaN structure using localized gate-foot oxidation. It gives a detailed description of the idea, fabrication technique and the results of this approach, which not only provides an uniform barrier thinning but also creates a good quality dielectric.

Chapter 5 describes a new AlN/AlGaN/GaN double barrier HEMT structure. Simulation results of this structure are described and show that it can be used to realize future high performance E-mode devices. Chapter 6 provides a review

of the main conclusions that can be drawn from the work described in this thesis including recommendations for future research.

CHAPTER 2

BASIC ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTOR TECHNOLOGY

2.1 Introduction

Aluminium gallium nitride - gallium nitride (AlGaN/GaN) high electron mobility transistors (HEMTs) consists of an AlGaN barrier layer grown on a much thicker GaN buffer layer grown on an insulating substrates like sapphire, diamond or aluminium nitride (AlN) or semi-insulating ones like silicon carbide (4H-SiC) or silicon [5],[6]. This chapter describes the formation of the quantum well (QW) at the AlGaN/GaN hetero-structure and the calculation of the 2DEG sheet charge density based on the material properties. This chapter also introduces the required metal-semiconductor contacts.

2.2 Standard AlGaN/GaN HEMTs Structure

A typical AlGaN/GaN HEMT layer structure is shown in Figure 2.1 and it consists of a 2 nm GaN cap layer on top of a 20 nm undoped $Al_xGa_{1-x}N$ (Aluminium content, $x = 20\%$) barrier layer. Below it is a 3 μm undoped GaN buffer layer which is grown on a very thin (typically $2 \backsim 5$ nm) AlN nucleation layer

Figure 2.1: A standard AlGaN/GaN HEMT structure.

sandwiched between the GaN buffer layer and the 350 μm sapphire substrate[6]. A similar layer structure with 35% Al-content ($x = 35\%$) has been used during the earlier stages of research for TEM analysis of the thermally grown oxide and MOS device fabrication as discussed in Section 4.5.

The substrates on which epitaxial GaN layers are grown have different lattice constants, which means that a lattice mismatch occurs between the GaN epilayers and the substrate. This mismatch induces strain which results in dislocation or defect areas. In order to reduce dislocation densities, a thin nucleation layer of GaN or AlN is grown on top of the substrate, on top of which the buffer and barriers layers are subsequently grown [6].

2.3 Polarization Effects in AlGaN/GaN Hetero-Structure [10],[11]

In the absence of external electric fields the total polarization P of a GaN or AlGaN layer is the sum of spontaneous polarization P_{SP} and piezoelectric polarization P_{PE}. Spontaneous polarization P_{SP} arises from the lack of symmetry of the wurtzite crystal whereas piezoelectric polarization P_{PE} generates from the stress and strain created due to the lattice mismatch of the GaN and AlN layers as previously discussed in Section 1.2.1. Structural parameters play a significant role in determining spontaneous polarization, which explains the differences in polarization of GaN and AlN [10]. The increasing non-ideality of the crystal structure from GaN to AlN [u_0 being the anion-cation bond length along the [0001] axis in units of c_0 increases, c_0/a_0 decreases] increases the spontaneous polarization. A standard AlGaN/GaN epitaxial film is grown along the [0001] axis as descibed in Section 1.2.1 and hence polarizations along that axis are only considered. The spontaneous polarization along the c axis is given by $\mathbf{P}_{SP}$=P_{SP}·$\widehat{\mathbf{z}}$, whereas the piezoelectric polarization is given by the piezoelectric co-efficients e_{33} and e_{13} as:

$$P_{PE} = e_{33}\varepsilon_z + e_{13}(\varepsilon_x + \varepsilon_y) \tag{2.1}$$

and $\varepsilon_z = (c - c_0)/c_0$, which is the strain along the c axis. The in-plane strain is assumed to be isotropic and is given by $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$, where a_0 and c_0 are the equilibrium values of the lattice parameters. The relationship of the lattice

constants of wurtzite GaN is given by equation (2.2)

$$\frac{c - c_0}{c_0} = 2\frac{C_{13}}{C_{33}}\frac{a - a_0}{a_0} \tag{2.2}$$

where C_{13} and C_{33} are elastic constants. Combining equations (2.1) and (2.2), the net piezoelectric polarization along c axis can be calculated as:

$$P_{PE} = 2\frac{a - a_0}{a_0}(e_{13} - e_{33}\frac{C_{13}}{C_{33}}) \tag{2.3}$$

Since $[e_{13} - e_{33}(C_{13}/C_{33})] < 0$ for AlGaN over the whole range of compositions, the piezoelectric polarization is negative for tensile and positive for compressive strain barriers, respectively [11].

The spontaneous polarization for Ga-face GaN and AlGaN are negative because the direction vector of the same points towards the substrate as shown in Figure 2.2. Similarly for N-face materials spontaneous polarization direction vectors points away from the substrate. For both Ga-face and N-face materials, the piezoelectric and spontaneous polarizations are parallel in case of tensile strain and antiparallel for compressively strained barrier layers which is shown in Figure 2.2. The polarization-induced charge density in space is given by $\rho_P = \nabla \cdot \mathbf{P}$. The polarization sheet charge density at an abrupt interface of an AlGaN/GaN or GaN/AlGaN hetero-structure is given by

$$\sigma = P(top) - P(bottom) \tag{2.4}$$

$$= \{P_{SP}(top) + P_{PE}(top)\} - \{P_{SP}(bottom) + P_{PE}(bottom)\} \tag{2.5}$$

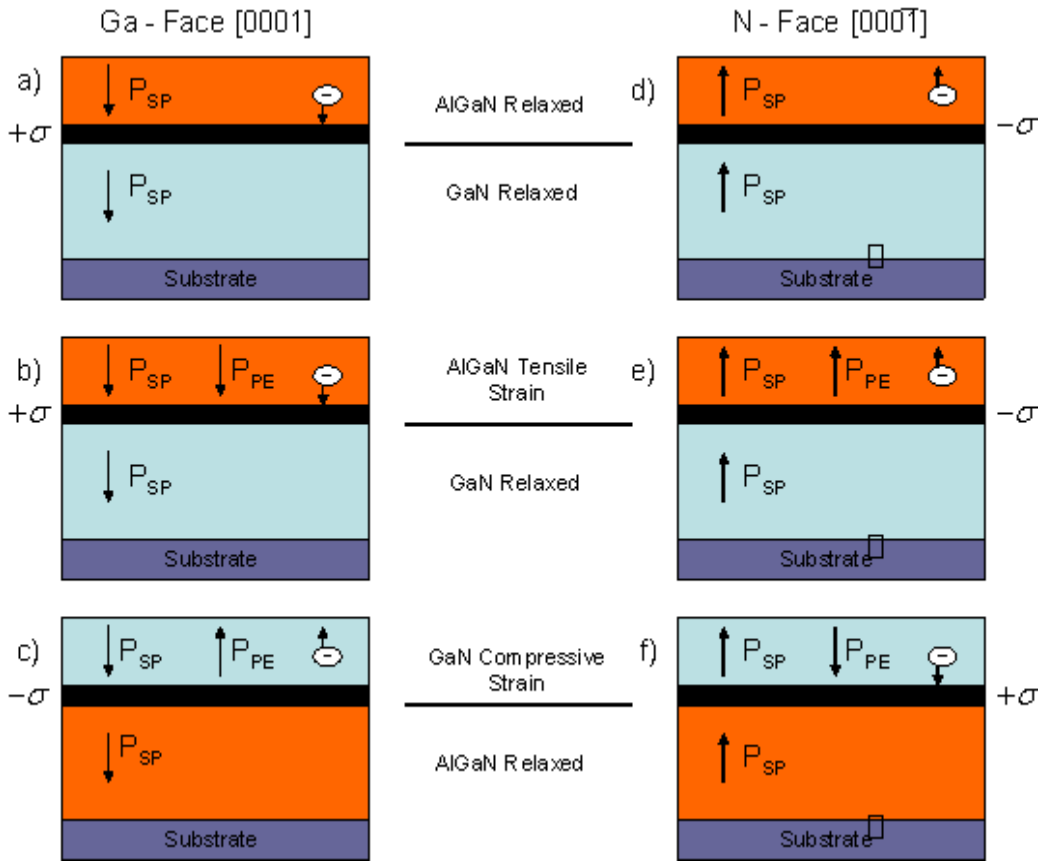


Figure 2.2: Spontaneous and piezoelectric polarizations in Ga and N-face GaN/AlGaN heterostructures [10].

However, if the polarization induced sheet density is positive ($+\sigma$), free electrons will try to compensate for the charges induced by polarization and vice versa. These charges will accumulate at the hetero-junction of the barrier and the buffer layer to create a two dimensional electron gas (2DEG) which is characterized by the sheet carrier concentration N_S. In the case of Ga-face structures with AlGaN on top of GaN the polarization induced sheet density is positive as shown in Figure 2.2a. If the hetero-structure is grown pseudomorphically the piezoelectric polarization of the tensile strained AlGaN barrier layer will increase the difference P(AlGaN)-P(GaN) and in-turn increasing the sheet charge density ($+\sigma$) and the electron confinement in the 2DEG. On the other hand for N-face AlGaN/GaN hetero-structures, the spontaneous and piezoelectric polarizations have opposite directions (points away from the substrate) than Ga-face AlGaN/GaN structures (points towards the substrate) and so the polarization induced sheet charge density is negative ($-\sigma$) and shown in Figure 2.2d and 2.2e. The negative sheet charge density assists to confine holes at the hetero-junction creating a two dimensional hole gas (2DHG). In order to calculate the magnitude of the polarization induced sheet charge density (σ) at AlGaN/GaN or GaN/AlGaN hetero-junctions the following sets of equations are used [11]. Depending on the physical properties of GaN and AlN the lattice constant depending on the Al content x is given by

$$a(x) = (-0.077x + 3.189) \times 10^{-10}\ m \tag{2.6}$$

The elastic constants are given by

$$C_{13}(x) = 5x + 103\ GPa \tag{2.7}$$

$$C_{33}(x) = -32x + 405\ GPa \tag{2.8}$$

The piezoelectric constants are given by

$$e_{13}(x) = -0.11x - 0.49\ C/m^2 \tag{2.9}$$

$$e_{33}(x) = 0.73x + 0.73\ C/m^2 \tag{2.10}$$

and the spontaneous polarization is given by

$$P_{SP}(x) = -0.052x - 0.029\ C/m^2 \tag{2.11}$$

The total amount of polarization induced sheet charge density for an undoped $Al_xGa_{1-x}N/GaN$ hetero-structure can be calculated using equations (2.3), (2.4) and (2.11) which is given by [10]

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)| \tag{2.12}$$

$$|\sigma(x)| = \left|2\frac{a(0) - a(x)}{a(x)}\{e_{13}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)}\} + P_{SP}(x) - P_{SP}(0)\right| \tag{2.13}$$

The magnitude of the polarization induced sheet charge density (σ) for both Ga-face or N-face hetero-structures is always the same but the sign changes. Most devices including those studied on this project employ Ga-face GaN.

2.3.1 Formation of Quantum Well

Beside polarization effects the sheet charge density is also influenced by the formation of the quantum well at the hetero-junction due to the difference in the bandgap of $Al_{0.20}Ga_{0.80}N$ (bandgap = $\backsim$ 4 eV) and GaN (bandgap = 3.4 eV). When the AlGaN layer is grown on the GaN layer a quantum well is formed as shown in Figure 2.3 due to the alignment of the fermi levels (E_F) of the two layers. In order to be in a stable state the electrons residing in the conduction bands of the AlGaN and GaN layers move towards the quantum well formed at the hetero-junction. Hence, a high density accumulation of electrons occurs, giving rise to the two-dimensional electron gas (2DEG). The maximum electron concentration in the 2DEG depends on the bandgap energy difference of the barrier and the underlying buffer layer. The 2DEG density in HEMTs is enhanced by the piezoelectric and spontaneous polarizations due to the strain caused by the crystal lattice mismatch of the layers and the lack of inversion symmetry of the III-Nitride semiconductor materials, respectively. This effect of unintentional doping is known as 'polarization doping' and is one of the main advantages of III-Nitride HEMTs [6].

Increasing the Al-content in the barrier layer increases the bandgap offset and also the polarization effects due to the increase in strain between the layers. Hence, higher Al-content devices exhibit higher output current and power density [35].

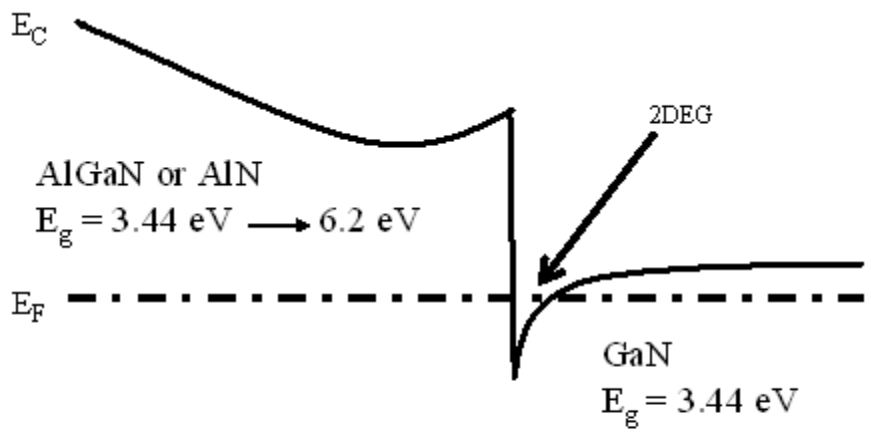


Figure 2.3: Energy band diagram of an undoped AlGaN/GaN HEMT.

2.4 Metal-Semiconductor Contacts

Generally, there are two types of metal-semiconductor contacts, ohmic (drain and source contact) and Schottky (gate contact). Metal-semiconductor contacts are usually characterized by the barrier height, i.e. the energy difference between the metal Fermi level and the conduction band edge of the semiconductor at the surface [36]. When a metal and a semiconductor are brought into intimate contact, a hetero-junction is formed at the interface and their Fermi levels align, and electrons diffuse from the semiconductor into the metal (where the Fermi level is generally in the conduction band). The diffusion creates an electric field, causing band-bending, until the Fermi levels align and an equilibrium is reached [36]. The alignment of the Fermi levels causes a conduction band offset at the metal-

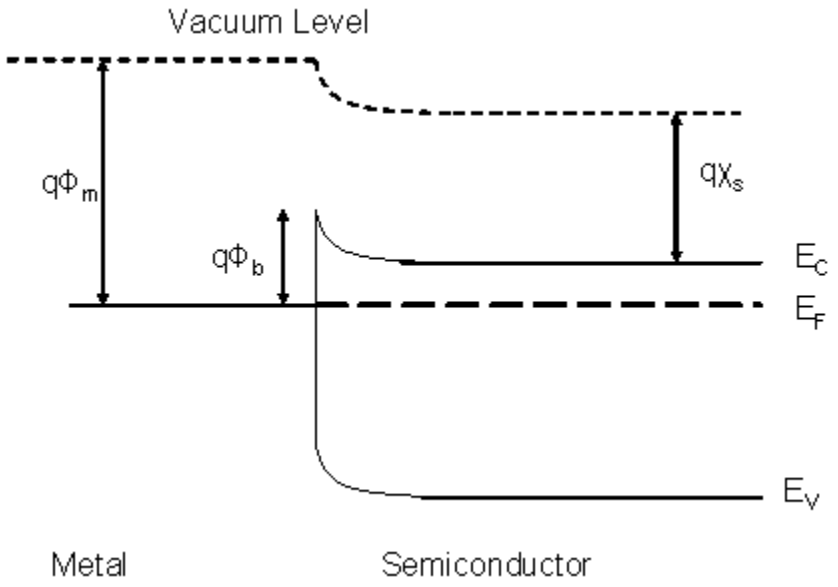


Figure 2.4: Band diagram of an ideal Schottky contact.

semiconductor interface and is known as the Schottky barrier which is illustrated in Figure 2.4 [36].

The height of the Schottky barrier, ϕ_b for an unpinned surface is therefore given by [36]

$$q\phi_b = q(\phi_m - \chi_S) \tag{2.14}$$

where ϕ_m is the work function of the metal and χ_S is the electron affinity of the semiconductor. Hence, if the Fermi level is unpinned the barrier height can be easily tailored by controlling the metal used for a specific semiconductor.

III-V semiconductors have a large surface state density and the interface states are sufficient to pin the Fermi level below the conduction band, with the conse-

quence that the energy barrier becomes independent of the metal work function [37]. The band diagram illustrating the pinned Fermi level is shown in Figure 2.5 [38]. The region between the metal and semiconductor is the interfacial region of thickness δ defined by the surface state density supporting a potential difference of Δ. The required energy at which surface states must be filled to ensure charge neutrality is denoted by ϕ_0, whilst ϕ_n is the offset of the Fermi level from the conduction band edge and V_{bi} is the built-in voltage. If incase the surface state density is quite large then ϕ_b is compensated by the surface states. Unde these circumstances no diffusion of electrons occurs and the process is fairly dominated by bandgap of the semiconductor and the surface states only and is given by [37]

$$\phi_b = E_g - \phi_0 - \phi_n \tag{2.15}$$

The width of the depletion region formed by the barrier can be calculated using Poisson's equation and is given by [36],

$$w = \sqrt{\frac{2\epsilon_S}{qN_D}(q\phi_b - V_{APP})} \tag{2.16}$$

where w is the depletion width, ϵ_S is the dielectric constant of the semiconductor, N_D is the dopant concentration, $q\phi_b$ is the barrier height and V_{APP} is the applied voltage.

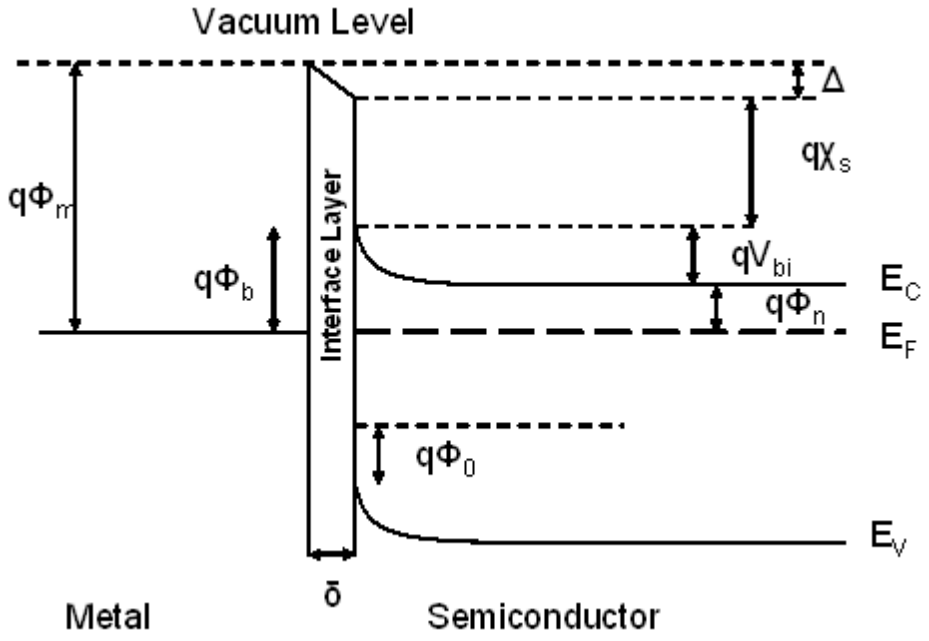


Figure 2.5: Band diagram of metal-semiconductor contact where the Fermi level is pinned by surface states and the the energy barrier is independent of work function.

2.4.1 Mechanism of Carrier Transport Across Barrier

In order for the current to flow across the barrier the energy barriers imposed by metal-semiconductor interfaces must be overcome. The main mechanisms by which carriers (electrons) can transit a barrier are thermionic emission, field emission and thermionic field emission and is shown in Figure 2.6a and 2.6b under forward and reverse bias conditions [36],[39], respectively. However, since majority carrier transport is considered detailed discussion on transport mechanism of minority carriers by recombination and hole transport via the valence band is not discussed here. In practice, the three mechanisms play a significant role in carrier transport though the dominant method is determined by the barrier width and its magnitude which are dependant on the material's intrinsic properties and the dopant concentration [36].

2.4.1.1 Thermionic emission

The mechanism of carrier transport using thermionic emission relies on thermal energy to excite the electrons with sufficient energy to cross the barrier height. In case of undoped or low doped semiconductors thermionic emisision is the dominant mechanism for carrier transport as the energy barrier is too wide for the carriers to tunnel across the barrier. Hence, based on this fact the carriers (electrons) must possess energy (E_e) higher than the barrier height ($E_e > q\phi_b$) in order to transit the barrier as shown in Figure 2.6. Those carriers which due to the ab-

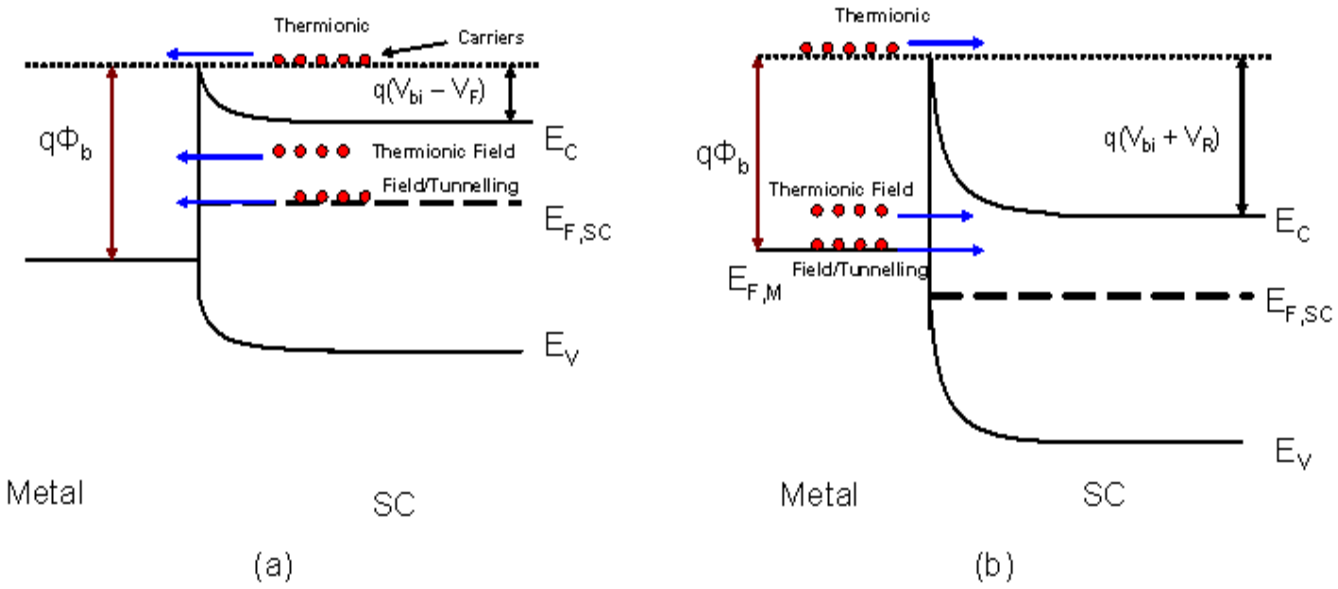


Figure 2.6: Overview of various barrier-transition mechanisms under forward-bias (a) and reverse-bias (b) conditions.

sorption of thermal energy occupy states above the barrier height will drift over the barrier under the influence of an external electric field. In other words, the thermal energy source supplies the carriers with significant kinetic energy to pass through the high electric field region at the metal-semiconductor interface over the barrier edge. The current density under thermionic emission (J_{TE}) conditions is directly proportional to the exponential of the ratio of barrier energy ($E_{barrier}$) to the absolute temperature (T) of the system and given by [36]

$$J_{TE} \propto \exp\left(-\frac{E_{barrier}}{k_B T}\right) \tag{2.17}$$

where k_B is the Boltzmann's constant. As a result, increased temperature

will enhance thermionic emission, as will reduce the barrier magnitude. Under zero bias conditions, $E_{barrier}$ is equal to the barrier height, i.e. ($E_{barrier} = q\phi_b$) and hence under constant temperature the current density is inverse exponentially dependent on the barrier height.

2.4.1.2 Field Emission

Field emission is based on the quantum mechanical tunnelling of carriers through the barrier, and is caused by the tail of the electron wave function extending through a very thin barrier. This process tends to occur in highly-doped ohmic contacts. Field emission occurs when carriers dont have enough energy to cross the barrier thermionically, but are able to tunnel through the barrier allowing current flow from either metal to semiconductor or vice versa and hence is independent of the system temperature and is shown in Figure 2.6. The tunnelling probability is dependent on the barrier energy and width leading to tunnelling current densities (J_{FE}) as described by [36],

$$J_{FE} \propto \exp\left(-\frac{E_{barrier}}{E_{00}}\right) \tag{2.18}$$

where E_{00} is the tunnelling parameter:

$$E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_D}{\epsilon_S m_e}} \tag{2.19}$$

where m_e is the mass of an electron and $\hbar$ is the Planck's constant. Hence,

based on Eqs (2.18) and (2.19) it can be seen the tunnelling current depends directly on $\sqrt{N_D}$. Since the barrier width varies with dopant density, the tunnelling probability increases as the barrier thins. In case of GaN ohmic contacts field emission is the dominant mechanism for carrier transport since annealing of the ohmic contacts creates a lot of n vacancies under the contact region and due to the presence of excessive carriers the tunnelling probability/current increases resulting in low resistance ohmic contact as opposed to a rectifying contact. Current will flow in equal magnitude from the metal to the semiconductor and vice versa under forward and reverse bias conditions.

2.4.1.3 Thermionic Field Emission

Thermionic field emission occurs in those scenarios where thermionic and field emission dominate. This is a combination of both thermal and field emission (tunnelling) phenomena, where carriers have insufficient energy to cross the barrier thermally, and the barrier is too wide for direct tunnelling. Electrons with a degree of thermal excitation, however, may be able to tunnel through the barrier, since its width decreases with increasing energy, which results in the flow of thermionic field current density (J_{TFE}) and is given by [36],[39],

$$J_{TFE} \propto \exp\left(\frac{E_{barrier}}{E_{00}\coth\left(\frac{E_{00}}{k_BT}\right)}\right) \tag{2.20}$$

where E_{00} is given by Eq (2.19). Thermionic field emission is therefore ex-

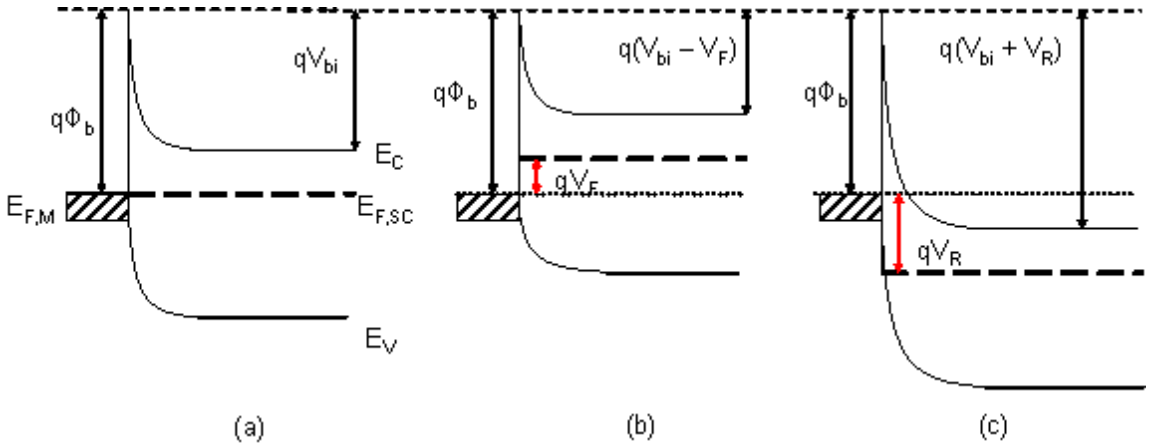


Figure 2.7: Band diagram of a metal-semiconductor Schottky contact under various bias conditions.

pected to increase with increasing temperature, and is strongly dependent on both barrier magnitude and dopant density. In particular, as for field emission, thermionic field emission will increase for a higher dopant density. The thermionic field emission phenomena is illustrated in Figure 2.6.

2.4.2 Rectifying (Schottky) Contact

Schottky or rectifying contacts play a significant role in controlling the current flowing between the drain and the source. In order to achieve a high quality Schottky contact the barrier height between the gate metal and the semiconductor should be as high as possible. Band diagrams of a Schottky metal-semiconductor under various bias conditions are shown in Figure 2.7 [36].

Figure 2.7a shows the condition when no bias is applied on the gate metal

and the Fermi level is aligned and the barrier height is given by Eq. 2.14. When forward biased the barrier height impeding electron flow from semiconductor to metal is reduced to $q(V_{bi} - V_F)$ as the Fermi level aligns to an energy equal to the applied voltage above the work function of the metal, increasing the probability of electrons acquiring enough energy to cross the barrier into the metal allowing current flow from metal to semiconductor. This phenomenon is illustrated in Figure 2.7b. When the junction is reverse biased, the effective barrier height increases and is dependant on the reverse bias voltage V_R, as shown in Figure 2.7c [36]. However, for an ideal Schottky contact the effective barrier height under reverse bias condition should be high enough so that carrier transition from semiconductor to metal is blocked and there is no current flow from metal to semicondcutor allowing rectification.

For wide bandgap materials like GaN, diamond, etc., the barrier height is strongly influenced by the work function of the Schottky contact metal [40]. For GaN based semiconductors metals with high workfunction are generally used to fabricate Schottky (gate) contacts. A list of metals with their work functions are shown in Table 2.1 [40],[41]. As seen from the table, platinum (Pt) and nickel (Ni) serves as the best candidates for Schottky contact due to their high workfunctions. However, Pt suffers adhesion problems with GaN and hence based on that Ni is one of the most widely used Schottky contact metal for GaN based semiconductors. Hence, all the derivations made in this thesis are based on Ni as

Metal	**Workfunction (eV)**
Ag	4.26
Al	4.28
Ti	4.33
Mo	4.60
Au	5.10
Ni	5.15
Pt	5.65

Table 2.1: Workfunction for various metals.

a Schottky contact. The metal scheme used generally for gate electrode is Ni/Au 50/150 nm. The Au layer prevents the oxidation of the Ni layer.

2.4.3 Ohmic Contact

The design strategy to obtain good ohmic contact is quite different than a Schottky contact. For ohmic contacts, the barrier height should be minimized to achieve a low-resistance connection as opposed to Schottky contacts, where it should be maximized to obtain rectification (diode characteristics) [42].

Most ohmic contacts on AlGaN/GaN hetero-structures are based on Ti/Al metallization schemes [42],[43]. The metallization scheme used for drain and source contacts in this project consisted of Titanium (Ti) / Aluminium (Al) / Nickel (Ni) / Gold (Au) 30/180/40/100 nm annealed at temperatures between

800^0C and 900^0C for the intermixing and the creation of the N-vacancies allowing tunnelling of electrons through the metal-semiconductor barrier as described in section involving field emission mechanism for carrier transportation. Each metal in the stack has its own purpose [44].

1. Titanium serves as an adhesion layer to provide good mechanical stability, dissolves the native oxide on the AlGaN surface and create nitrogen vacancies by reacting with nitrogen atoms to form TiN in the AlGaN layer. This process renders the surface highly doped, which enables electrons to tunnel through the metal-semiconductor barrier easily thus reducing the contact resistance.

2. Aluminium reacts with Ti to form an Al_3Ti layer that prevents the underlying Ti layer from oxidizing and serves as a diffusion barrier for the metals on top of Al as they form high Schottky barriers.

3. Nickel, being the third layer prevents the mixing of the Aluminium with Gold as the reaction between Al and Au forms 'purple plague' a highly resistive layer.

4. Gold is added to improve conductivity.

Similarly, a Schottky contact is designed for the gate to achieve diode characteristics and control the current flow through the channel.

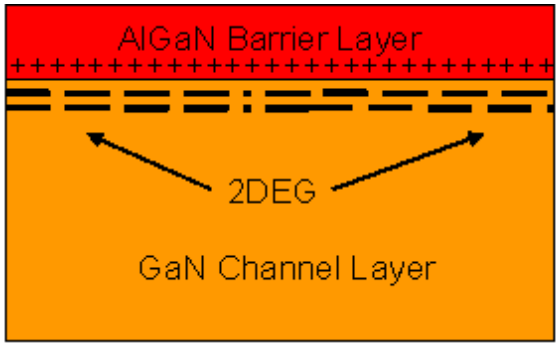


Figure 2.8: Formation of 2DEG at the AlGaN/GaN heterolayer.

2.5 Calculation of Sheet Carrier Concentration in the 2DEG

The net polarization in the AlGaN/GaN hetero-structure induces a very high density of positive charges at the AlGaN/GaN or GaN/AlGaN interface as shown in Figure 2.8. In order to compensate for the net positive charge a 2-Dimensional Electron Gas (2DEG) forms also at the hetero-layer within 5-7 nm deep in the GaN layer [45]. The sheet carrier concentration at the interfaces of undoped structures can be calculated using Ambacher et al., model [10] which is based on self consistant Poisson-Schrodinger equation and is given by

$$N_S(x, d_{AlGaN}) = \frac{\sigma(x)}{e} - \frac{\varepsilon_0 \varepsilon(x)}{e^2 d_{AlGaN}} \times (e\phi_b(x) + E_F(x) - \Delta E_C(x)) \qquad (2.21)$$

where x is the aluminium mole fraction and d_{AlGaN} is the thickness of the $Al_xGa_{1-x}N$ layer, $\sigma(x)$ is the magnitude of the total bound sheet charge, e is the charge of electron, ε_0 is permittivity of vacuum, $\varepsilon(x)$ is relative permittivity of the barrier layer, ϕ_b is Schottky barrier height, $E_F(x)$ is the Fermi level with the respect to the GaN conduction band edge and ΔEc is conduction band offset at the AlGaN/GaN

interface. In order to solve equation (2.21), the following approximations are used

$$\varepsilon(x) = -0.5x + 9.5. \tag{2.22}$$

As discussed in previous Section, Ni is the best candidate for Schottky metal contact for GaN materials. Hence, all the calculations are based with Ni as the Schottky metal and the nickel-semiconductor barrier height based on the Al content is given by [46]

$$e\phi_b = 1.3x + 0.84\ eV \tag{2.23}$$

Fermi level energy [47]

$$E_F(x) = E_0(x) + \frac{\pi\hbar^2}{m^*(x)} N_S(x) \tag{2.24}$$

where the ground sub-band level $E_0(x)$ of the 2DEG is obtained by solving the Schrodinger and Poisson equations self-consistently, is given by

$$E_0(x) = \left(\frac{9\pi\hbar e^2}{8\varepsilon_0\sqrt{8m^*(x)}} \frac{N_S(x)}{\varepsilon(x)} \right)^{\frac{2}{3}} \tag{2.25}$$

where $m^*(x) \approx 0.228m_e$ is the effective electron mass. Band offset is defined by [48],[49]

$$\Delta E_C(x) = 0.7[E_g(x) - E_g(0)] \tag{2.26}$$

where $E_g(x)$ is the bandgap dependant on the Al-content (x) is calculated using Vegard's Law with a bowing parameter and is given by [50]

$$E_g(x) = xE_g(AlN) + (1-x)E_g(GaN) - x(1-x)1.0\ eV \quad (2.27)$$

$$= x6.2 + (1-x)3.44 - x(1-x) \times 1.0\ eV \quad (2.28)$$

$$= x^2 + 1.76x + 3.44\ eV \quad (2.29)$$

The total bound sheet charge is given by

$$\sigma(x) = P_{PE}(x) - P_{PE}(0) + P_{SP}(x) - P_{SP}(0) \quad (2.30)$$

where P_{PE} is piezoelectric polarization and P_{SP} is spontaneous polarization. The GaN layer is considered to be fully relaxed and therefore $P_{PE}(0)$ is set to zero. The spontaneous polarization has a quadratic dependence on x and is given by

$$P_{SP}(x) = 0.09x - 0.034(1-x) + 0.02x(1-x) \quad (2.31)$$

The piezoelectric polarization can be approximated based on Ambacher et al, 2000 model [13] as

$$P_{PE}(x) = -0.0525x + 0.0282x(1-x) \quad (2.32)$$

For different values of x (Al content), a simulation was carried out based on equations (2.21) to (2.32) using Ni as the Schottky contact metal, and the graph showing the variations of the sheet charge density with Al content is plotted in Figure 2.9.

From the graph shown in Figure 2.9 it is clear that the sheet charge density increases with Al- content and barrier layer thickness. For instance, to reach a

carrier concentration of 10^{13} cm^{-2} only $\sim$ 3 nm of AlN, $\sim$ 5 nm of $Al_{0.60}Ga_{0.40}N$ and $\sim$ 20 nm $Al_{0.25}Ga_{0.75}N$ barrier is required. But in reality increasing the AlGaN layer thickness over a certain thickness for a specific Al-content increases the strain at the hetero-layer causing high surface roughness, high dislocation densities and even cracks, which tends to relax (no longer strained) the entire hetero-structure and reduce the polarization effects and hence the sheet charge density can decrease drastically [51],[52],[53]. Note however that it is easier to grow barrier layers with 20-25% or 100% Al-content AlGaN barriers. For high Al-content barriers (>30%) growth is more difficult and the ohmic contact resistance is higher [54].

Conventional AlGaN/GaN devices employ 20-25% Al content and the barrier thickness is approx. 20 nm [6]. These AlGaN/GaN HEMTs are therefore depletion mode devices. More recent devices have employed just an AlN barrier and they are also depletion mode devices [55]. Figure 2.9 also shows that no 2DEG forms below a certain barrier thickness, e.g. $<$ 9 nm for $x = 15\%$, $<$ 6 nm for $x = 25\%$. Therefore for this Al-content, barrier thicknesses of less than 9 nm and 6 nm, respectively, would be desirable to realize E-mode devices because no channel is formed prior to the application of a positive gate voltage. It will be shown in the subsequent two chapters that this is indeed one of the main methods of achieving E-mode operation, but the barrier has to be this thin only underneath the gate electrode if good device performance is to be achieved.

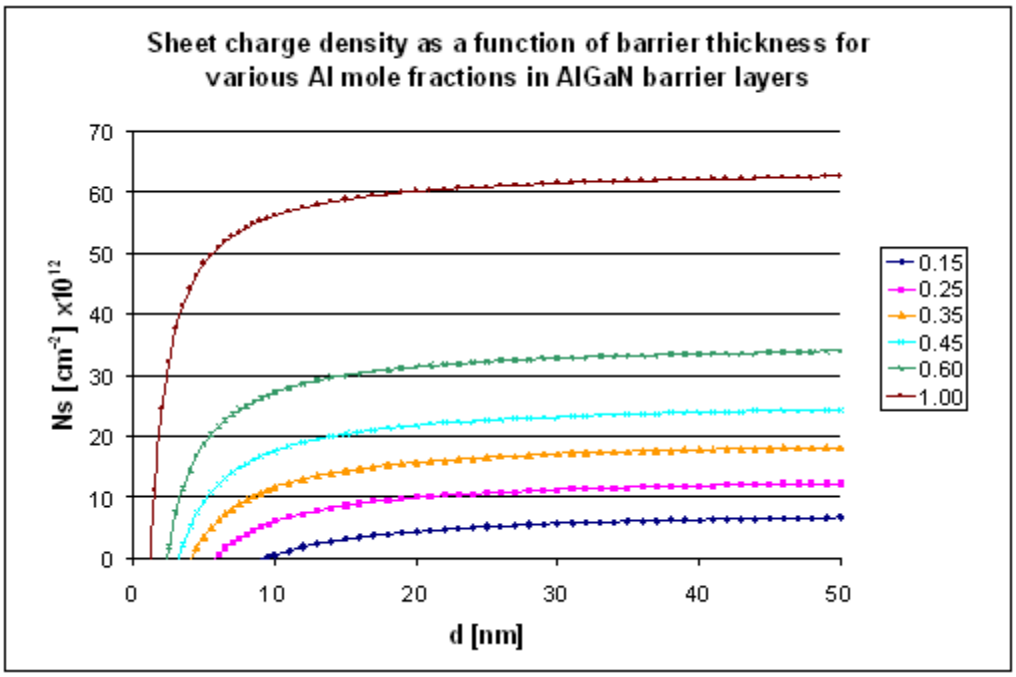


Figure 2.9: Graph showing the variations of the sheet charge density versus barrier layer thickness (d_{AlGaN}) for different Al percent.

2.5.1 Discussion

The data calculated using Ambacher et. al., model described in the previous section bears a close resemblance to current AlGaN/GaN materials' specifications commercially available for specific Al content. However, very small variations in the data of the graph described in Figure 2.9 can be seen when compared to the calculations and the graphical plot described in the Reference [10], which can be due to the usage of more accurate data of material properties such as AlN (6.2 eV instead of 6.13 eV) and GaN (3.44 eV instead of 3.42 eV) bandgap, updated polarization and lattice constants, etc.

2.6 Principle of Operation of AlGaN/GaN HEMTs

An AlGaN/GaN HEMT is formed by fabricating drain and source (ohmic) contacts and a gate (Schottky) contact to the device layer. A schematic layout of the equivalent circuit elements for a standard AlGaN/GaN HEMT is shown.in Figure 2.10 [52],[56].

The efficiency of the transistor is based on the functionality of the 2DEG, which can be controlled by the capacitance between the gate contact and the 2DEG.

$$C_{2DEG} = \frac{\partial q\sigma_{2DEG}}{\partial V_a} = \frac{\varepsilon_{AlGaN} \times A_{2DEG}}{d_{eff}} \tag{2.33}$$

where d_{eff} is the effective gate to 2DEG separation and is constant for this calculation. Integrating equation (2.33) over the entire channel length (dx) the charge

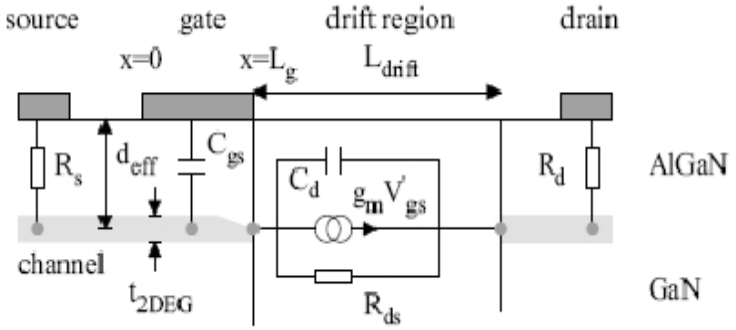


Figure 2.10: A schematic layout of AlGaN/GaN HEMT

distribution along the channel due to the application of the drain-source voltage (V_{DS}) is given by [52],

$$q\sigma_{2DEG} = \frac{\varepsilon_{AlGaN}\ A_{2DEG}[V_{GS} - V_P - V_X]}{d_{eff}} = C_{2DEG}[V_{GS} - V_P - V_X] \qquad (2.34)$$

where V_{GS} is the gate-source voltage, V_P is the pinch-off voltage and V_X is the effective voltage in the channel due to the application of the drain-source voltage. This causes σ_{2DEG} to be to be dependent on the position along the gate, near the source it will be higher and near the drain comparatively lower. Moreover, based on the principle of current continuity ($\sigma_{2DEG}\times$ electron velocity,v_e =constant) it can deduced that v_e increases moving from source to drain. The electric field experienced by the electrons in the channel due to the V_X can be defined as $E_X = \partial V_X/\partial x$. For, $E_X \geqslant 2E_G$, electrons travel at saturated velocity v_{SAT} and for $E_X < 2E_G$, we have

$$v_e = \frac{\mu_e E_X}{1 + E_X/2E_S} \qquad (2.35)$$

where E_G is the electric field under the gate, v_e is the electron velocity, μ_e is the

low field electron mobility and $E_S = v_{SAT}/\mu_e$. Neglecting the source and drain resistances R_S and R_d respectively, the source-drain current I_{DS} for a transistor of gate length L_g and width W_g, operating in the linear region is given by [52]

$$I_{DS} = \frac{W_g}{L_g}\int_0^{L_g} q\sigma_2 v_e dx = \frac{1}{R_n}\frac{2(V_{GS}-V_P)V_{DS}-V_{DS}^2}{(V_{DS}+2V_L)} \tag{2.36}$$

where, $R_n = (W_g C_{2DEG} v_{SAT})^{-1}$, $\sigma_{2DEG} v_e$ is a constant, V_{DS} is the drain-source voltage and $V_L = E_G L_g$. Increasing the V_{DS} causes the electrons to reach v_{SAT} and the voltage that marks this point is known as the drain saturation voltage $V_{DS,SAT}$. Similarly, the current flowing through the drain at $V_{DS} = V_{DS,SAT}$, is the drain saturation current ($I_{D,SAT}$) and can be calculated by combining equations (2.34) and (2.36) [52].

$$\begin{aligned} I_{D,SAT} &= C_{2DEG}[V_{GS}-V_P-V_{DS,SAT}]W_g v_{SAT} \\ &= \frac{1}{R_n}\frac{(V_{GS}-V_P)^2}{(V_{GS}-V_P+2V_L)} \end{aligned} \tag{2.37}$$

As explained before the electron density decreases from source to drain and thereby their velocities increases as indicated by the principle of current continuity. When the transistor operates in saturation the electrons near the drain side has very high velocities with very low densities. However, when the electrons passes the gate region their densities and velocities do not instantaneously return to low-electric field values found between the source and gate region. Instead, between the gate and drain a drift region (L_{drift}) is formed, which is characterized by

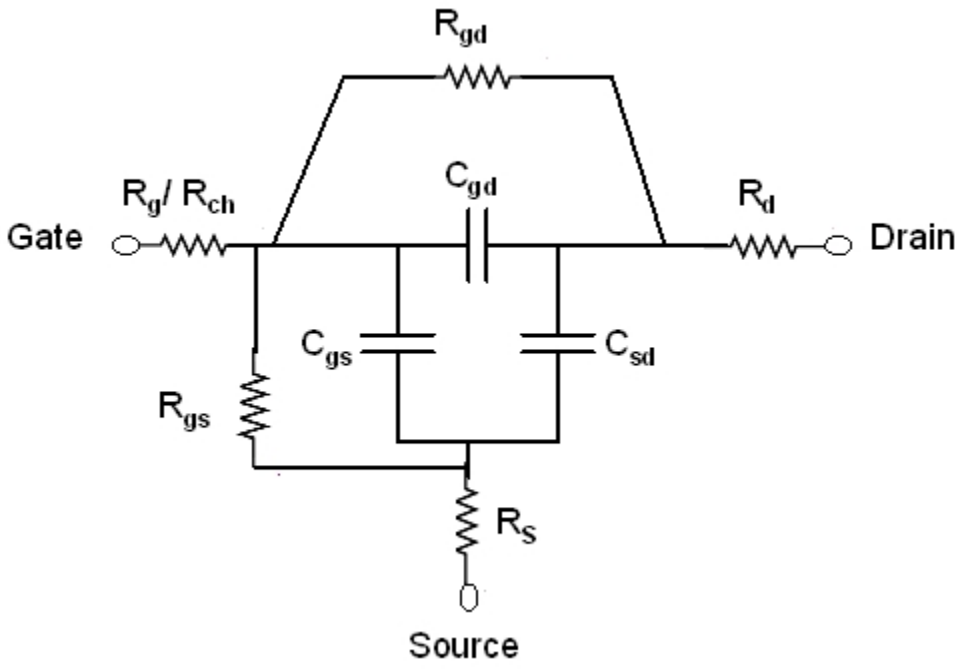


Figure 2.11: Simplified model of a MOS-HEMT as a switch.

high electric fields, high electron velocities and low electron densitites as shown in Figure 2.10 [52]

A simplified model of a MOS-HEMT as a switch including the parasitic components is illustrated in Figure 2.11 [57]. The Figure of Merit (FoM) of a switch is defined by the product of the device resistance (explained in the following section) and the total gate charge ($C_{gs} + C_{gd}$) required to drive the MOS-HEMT [58]. Hence, a lower value of the gate and drain capacitances can significantly improve the device performances.

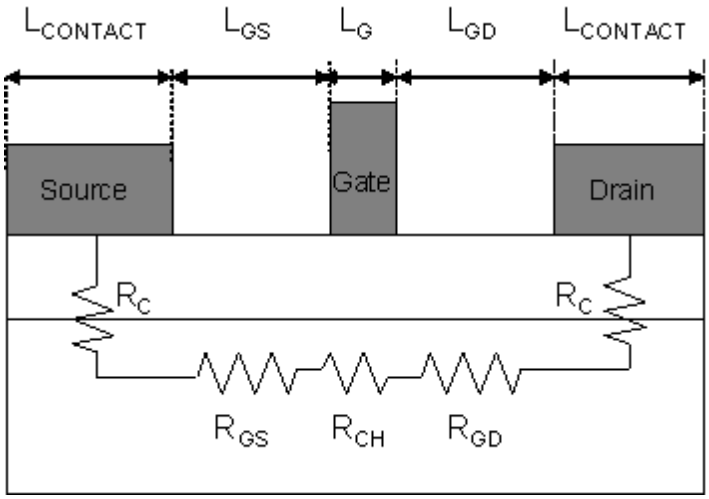


Figure 2.12: Resistance and size parameters for the calculation of On-resistance of a HEMT.

2.7 On-Resistance (R_{ON}) of a HEMT Structure

On-resistance or R_{ON} of a device is the combined resistances of all the regions of the device as shown in the crosss-section of the device in Figure 2.12 and is generally used to calculate heat loss in the device for high voltage switching applications.

The total device resistance or R_{ON} can be calculated using equation (2.38)

$$R_{ON} = R_C + R_{GS} + R_{CH} + R_{GD} + R_C \tag{2.38}$$

$$= R_{GS} + R_{CH} + R_{GD} + 2R_C \tag{2.39}$$

where R_C is the ohmic contact resistance, R_{GS} is the resistance of the active region between source and gate, R_{GD} is the resistance of the active region between gate and drain and R_{CH} is the resistance of the channel region under the gate-foot.

Saito et al.[34] calculated the resistance components individually based on the size parameters of the HEMT structure and are given by

$$R_{GS} = \frac{L_{GS}}{q\mu N_{2DGS}} \tag{2.40}$$

$$R_{GD} = \frac{L_{GD}}{q\mu N_{2DGD}} \tag{2.41}$$

where q is the charge of an electron, μ is the electron mobility at the hetero-interface, L_{GS} and L_{GD} are the source-gate and gate-drain distance, respectively, N_{2DGS} is the 2DEG density in the active region between source and gate and N_{2DGD} s the 2DEG density in the active region between gate and drain. However, the calculation of the channel resistance R_{CH} varies depending on the device technology, e.g. Schottky, MOS-HEMT, etc. For Schottky structures R_{CH} is given by[34]

$$R_{CH} = \frac{L_G}{\mu C_G(V_{G,ON} - V_{TH} - \phi_B)} = \frac{L_G \times t_{Barrier}}{\mu \varepsilon_{Barrier} A_G(V_{G,ON} - V_{TH} - \phi_B)} \tag{2.42}$$

as where L_G or L_{CH} is the gate length, C_G is the gate capacitance, ϕ_B is the Schottky barrier height, $\varepsilon_{Barrier}$ is the dielectric constant of the barrier, $V_{G,ON}$ is the on-state gate voltage of the device, V_{TH} is the threshold voltage, $t_{Barrier}$ and is the thickness of the barrier layer and A_G is the area of the gate region. However, for MOS-HEMT devices the equation changes due to the presence of an insulator (oxide film) as it directly influences the gate capacitance, threshold voltage and barrier height of the device as is given by [34]

$$R_{CH} = \frac{L_G}{\mu C_{MOS}(V_{G,ON} - V_{TH,MOS} - V_{FB})} \tag{2.43}$$

$$V_{TH,MOS} = \left(1 + \frac{C_G}{C_{MOS}}\right) V_{TH} \tag{2.44}$$

$$C_{MOS} = \frac{\varepsilon_{Barrier} \times \varepsilon_{MOS}}{\varepsilon_{Barrier} \times t_{OX} + \varepsilon_{OX} \times t_{Barrier}} \tag{2.45}$$

where C_{MOS} and $V_{TH,MOS}$ are the gate capacitance and the threshold voltage of the MOS device, respectively, V_{FB} is the flat-band voltage and ε_{OX} and t_{OX} are the dielectric constant and thickness of the oxide film.

The On-Resistance values used in this thesis are all specific values of measured device resistance and is denoted as $R_{ON,meas}$. The specific On-resistance $R_{ON,sp}$ is usually obtained by multiplying $R_{ON,meas}$ with the total area A of the device as shown in Eq 2.46 or by multiplying the source-drain distance, L_{SD} with the normalized On-resistance $R_{ON,norm}$ and is given by Eq 2.47,

$$R_{ON,sp} = R_{ON,meas} \times A = R_{ON} \times (L_{SD} \times W)\ \Omega.mm^2 \tag{2.46}$$

$$R_{ON,sp} = R_{ON,norm}\ (\Omega.mm) \times L_{SD}\ (mm) = R_{ON,norm} \times L_{SD}\ \Omega.mm^2 \tag{2.47}$$

For high performance E-mode devices the resistances R_C, R_{GS}, R_{GD} and R_{CH} should be minimized. R_C is minimized by optimizing the metal semiconductor ohmic contacts. On the other hand, R_{GS} and R_{GD} can be minimized by employing a barrier thickness that creates high 2DEG density at the hetero-junction, e.g. 20

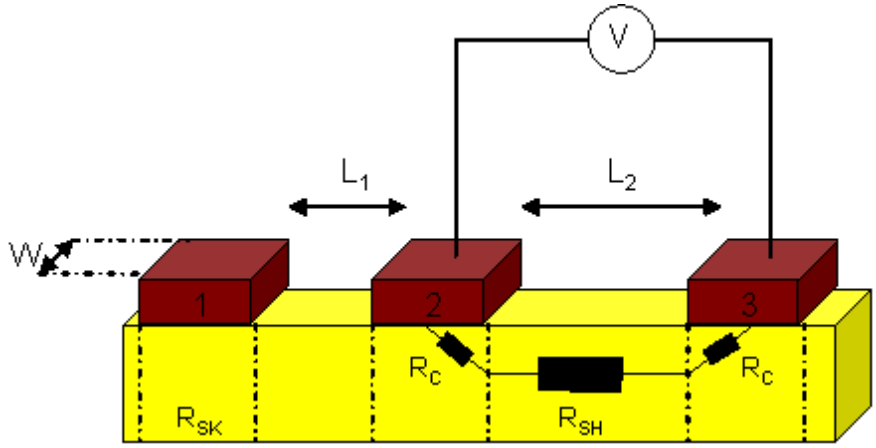


Figure 2.13: TLM characterization technique.

nm AlGaN barrier for $x = 20\%$ creates $1 \times 10^{13}\ cm^{-2}$ sheet carrier concentration. To achieve E-mode operation the barrier thickness underneath the gate (above R_{CH}) has to be less than the critical thickness and therefore this resistance is an open circuit for zero gate voltage. However for positive gate bias the device has to be designed such that a 2DEG channel re-forms underneath the gate to have low R_{CH} resistance values. R_{CH} can also be minimized by using short gate lengths (sub 200 nm).

2.8 TLM Characterization

The Transmission Line Method (TLM) is a procedure to determine the contact resistance (R_C) between the semiconductor and metal. The technique involves making a series of metal-semiconductor contacts separated by various distances (transmission line length). A basic layout of a TLM pattern is shown in Figure

2.13. Applying a voltage and measuring the resultant current gives the resistance between a pair of contacts. The current flows from the measuring probes though the metal contact, across the metal-semiconductor region, though the semiconductor transmission line (L_1, L_2 etc) and into the second probe though the second metal-semiconductor region and metal as shown in Figure 2.13. The net resistance obtained is the sum of the two metal contacts and the sheet resistance of the semiconductor. Several such measurements are made and are plotted against the transmission line length as shown in Figure 2.14 with the gradient of the line being the per unit sheet resistance of the semiconductor [59]. G.K. Reeves et al.[59] derived the total resistance between the contacts as a function of the material parameters and is given by

$$R_{TOTAL} = \frac{2R_{SK}L_T}{W} + \frac{R_{SH}L}{W} \tag{2.48}$$

where R_{SK} is the modified sheet resistance under the metal contacts, L_T is the transfer length, R_{SH} is the sheet resistance of the semiconductor, L is the transmission line lengths (L_1, L_2 etc) and W is the width of the metal pads.

As shown in the Figure 2.14, the point where the curve intercepts the y-axis gives us twice the contact resistance value. Hence, by using this procedure both the metal-semiconductor contact resistance (R_C) and the sheet resistance of the semiconductor (R_{SH}) can be easily calculated [59].

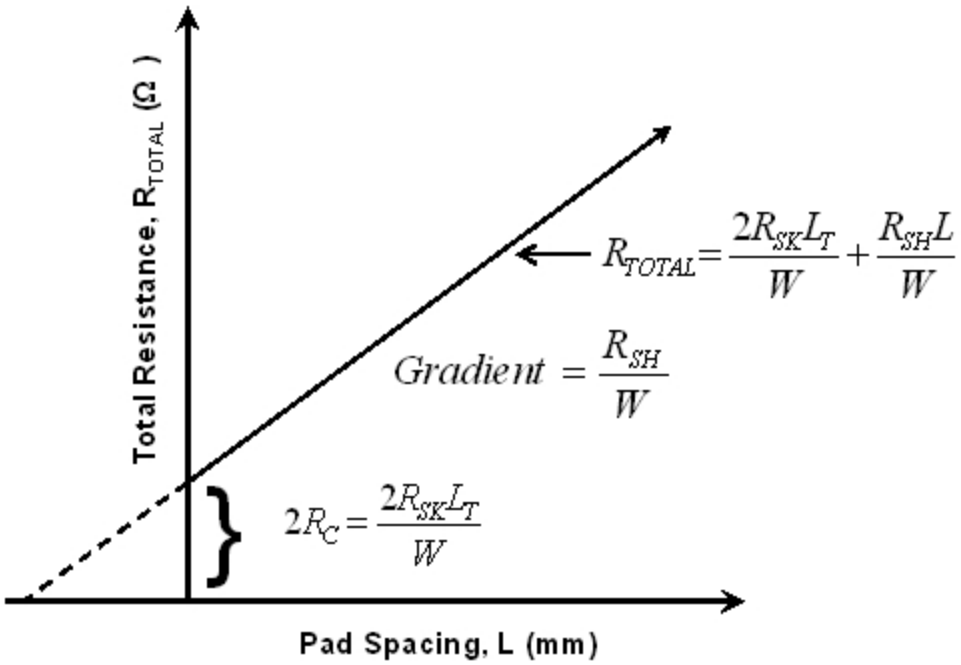


Figure 2.14: Graph showing TLM measurement and calculation of contact and sheet resistance.

2.8.1 Mathematical Extraction Technique of Resistance Figures from TLM Measurements

The mathematical technique used to extract resistance figures from the TLM measurement graphs is known as Least Squares Method [60]. For TLM measurements the error is only calcuated for values of Y axis assuming the values of X axis are error free. This methodology is known as ordinary least squares since errors are calculated for one variable only. Ordinary least squares (OLS) is a statistical technique that uses sample data to estimate the true population relationship between two variables [60]. Consider the scatter plot diagram illustrated in Figure 2.15 showing the actual, observed data points on the graph and e_i is the residual (error), represents the distance between the sample regression line and the observed data point, (X_i, Y_i). OLS produces a line that minimizes the sum of the squared vertical distances from the line to the observed data points. The line that minimizes the sum of these distances is the one that gives us the best fit. The sample regression line is given by $Y_i = f(X_i) = (B_0 + B_1 X_i)$. The ordinary least squares method helps to determine B_0 and B_1. However, some of the values of the residuals are negative in sign while others are positive. By the summation of the residuals, positive values will cancel out negative values so the sum will not accurately reflect the total amount of error [60].

OLS helps to generate a regression like which minimizes the sum of the squared vertical distances ($\sum e_i^2$) from the data points, i.e., it minimizes the residual sum

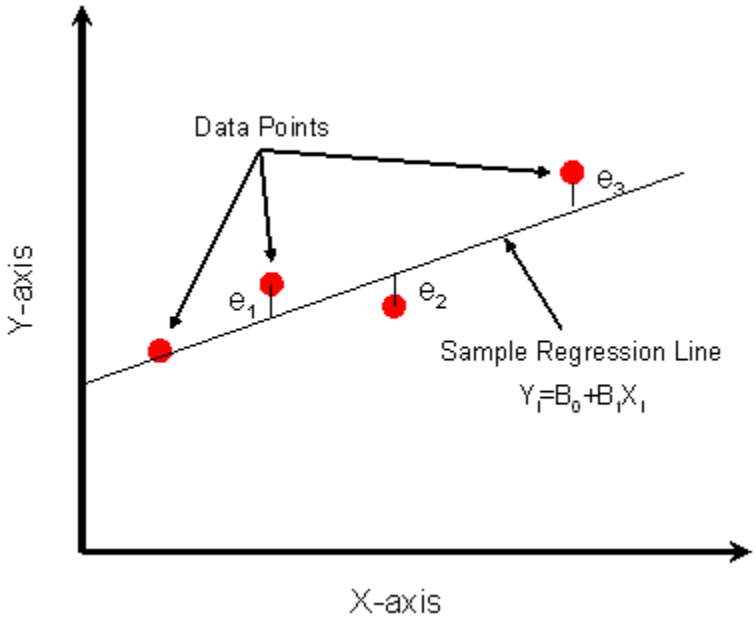


Figure 2.15: Data plot showing the "best fit" Regression Line obtained using least squares method.

of squares ($\sum e_i^2$),

$$\sum e_i^2 = e_1^2 + e_2^2 + e_3^2 + e_4^2 + ... + e_n^2 \quad (2.49)$$

$$= \sum (Y_i - B_0 - B_1 X_i)^2 \quad (2.50)$$

as the error $e_i = Y_i - f(X_i)$, $\sum = \sum_{i=1}^{n}$, n is the total number of data points and i = 1,2,3.... n etc..

In order to minimize the sum of the squared error terms the Eq (2.50) needs to be minimized. In terms of calculus this means to find the critical points of a function. To find the values of B_0 the first derivative of Eq (2.50) with respect to B_0 is set equal to zero and is given by [60],

$$B_0 = \frac{\sum Y_i - B_1 \sum X_i}{n} \quad (2.51)$$

In order to solve for B_1 the first derivative of Eq (2.50) with respect to B_1 is set it equal to zero and is given by [60],

$$B_1 = \frac{n \sum X_i Y_i - \sum X_i Y_i}{n \sum X_i^2 - (\sum X_i)^2} \quad (2.52)$$

Replacing the values of B_1 from Eq.(2.52) in Eq (2.51) we have

$$B_0 = \frac{\sum X_i^2 \sum Y_i - \sum X_i \sum X_i Y_i}{n \sum X_i^2 - (\sum X_i)^2} \quad (2.53)$$

The standard error of estimate (S_E) between the calculated regression line and its data points is given by [60],

$$S_E = \sqrt{\left(\frac{\sum Y_i^2 - B_0 \sum Y_i - B_1 \sum X_i Y_i}{n-2}\right)} \tag{2.54}$$

2.9 GaN Based Semiconductor Growth Techniques

Material growth is an important aspect as high quality GaN epitaxial wafers are necessary for good device performances. Metal Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE) are the most common and popular techniques used for GaN epitaxial growth.

2.9.1 MOCVD (Metal Organic Chemical Vapor Deposition)

Metal Organic Chemical Vapour Deposition (MOCVD) is a technique used to grow materials using volatile metal-organic compounds to transport metal ions which are relatively non-volatile at deposition temperature. The metal-organic compounds are transported by a carrier gas, H_2, to a heated substrate which reacts with hydrides to form semiconductor films. The procedure involved in the growth of GaN involves the introduction of trimethyl gallium and ammonia gas simultaneously into the reaction chamber with a substrate heated to temperatures usually in the range of $800^0C \backsim 1000^0C$ [61],[62],[63],[64],[65].

$$(CH_3)Ga(g) + NH_3(g) = GaN(s) + 3(CH_3)H(g) \tag{2.55}$$

However, for the growth of ternary compounds like AlGaN, InGaN, etc, trimethyl aluminium or trimethyl indium simultaneously are generally reacted with trimethyl gallium and ammonia at elevated temperatures. Adjusting the gas-phase compostion of the metal-organic compounds in the reaction chamber controls the composition of the ternary compounds formed [64],[65].

$$x(CH_3)Al + (1-x)(CH_3)_3Ga + NH_3 \rightarrow Al_xGa_{1-x}N + ... \quad (2.56)$$

Currently MOCVD is used to grow high quality GaN epitaxial wafers for commercial uses like high brightness blue LED and injection laser diodes.

2.9.2 MBE (Molecular Beam Epitaxy)

Molecular Beam Epitaxy (MBE) is one of the modern techniques used to grow single crystals. The main advantage of this technique is high quality layers, slow deposition rate (<1 μm/hr) and good control of thickness, doping and concentration. In conventional solid-source MBE the ultra-pure elements like aluminium, gallium, indium, etc are heated in effusion cells to sublimate and allowed to condense on a substrate where the elements react with each other to form thin film layers. However, the atomic nitrogen.is created by electron cyclotron resonance (ECR) plasma sources. MBE growth chamber temperatures vary in the range between 600^0C and 900^0C. A computer controls the effusion cell shutters allowing precise control of the thickness of each layer [63],[64],[66],[67].

CHAPTER 3

GAN BASED ENHANCEMENT-MODE DEVICE TECHNOLOGY

3.1 Current E-Mode Technologies

Enhancement mode GaN-based HEMTs, are in high demand in the market because of their normally-off and high power switching capabilities at RF frequencies [68],[69]. This chapter explains the technologies presently used to fabricate GaN based Enhancement Mode devices including their advantages and drawbacks.

3.1.1 Barrier Thinning Using Etching Techniques

One of the most common ways to achieve E-Mode operation from the conventional AlGaN/GaN structure is by physically thinning the barrier layer [33],[34] till it reaches the critical thickness of the layer and the channel acts as an open circuit under the gate-foot region enabling normally-off operation. The thinning, however, is carried out physically by the assistance of plasma based Reactive Ion Etching (RIE) technique using chlorine based gases or by wet etch techniques using alkali (KOH/NaOH) based solutions [70],[71],[72],[73]. The basis of this technique is that there is no formation of 2DEG below a certain barrier thickness

which is also known as the critical barrier thickness, t_{CR}. Etching of the barrier is generally carried out locally under the gate-foot region using an etch-resistant mask material like SiO_2 or SiN etc, till the thickness becomes equal or less than the critical barrier thickness so that there is no formation of the 2DEG under the gate-foot region, as shown in Figure 3.1 [33],[34],[74]. The deposition of the gate metal creates a Schottky contact which further depletes the region underneath of electrons and helps to achieve enhancement-mode or normally-off operation.

To date dry etch is the only effective and widely used etch method for GaN based semiconductors as wet etching techniques researched so far are not repeatable and requires complex equipments setup such as electrolytic equipments, UV lights, precise alkaline solutions, etc. Moreover, it has also been proved that high quality Ga-face GaN wafers cannot be chemically etched due to smoother surfaces and crystal orientation and hence cannot be used for device fabrication purposes [75]. However, RIE also has major disadvantages such as reproducibility and uniformity [76]. Since RIE involves a physical etch, it damages the sample surfaces and is also hard to control and hence over-etching is an issue. Also, the generated RF plasma is not uniform in every part of the chamber and thus the etch rate is not uniform over large wafers and hence the threshold voltage varies from device to device [76].

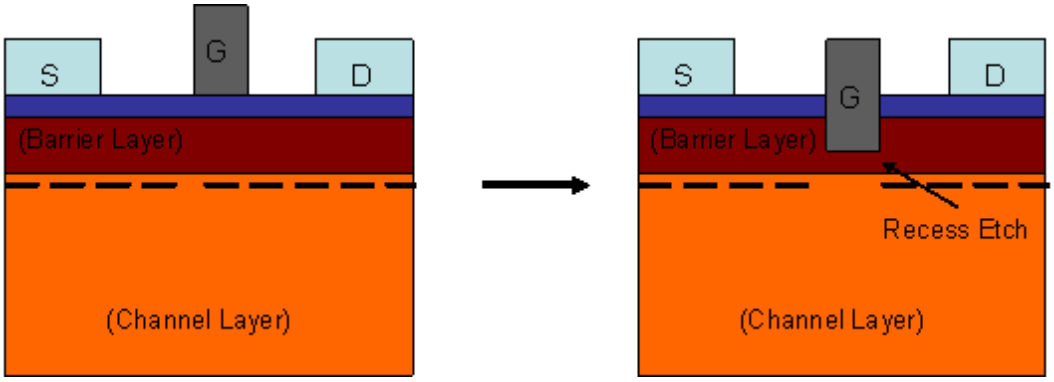


Figure 3.1: E-mode or 'normally-off' operation using recess etching technique.

3.1.2 Double HEMT Structure With Etch-Stop Layer

The etch-stop layer technique for fabricating E-Mode devices involves hetero-structures with two active barrier layers. The top active layer can be selectively etched using dry or wet-etching techniques until the second active/barrier layer which acts as an etch-stop layer is reached as illustrated in Figure 3.2. This method follows the same principle as recess etching to fabricate E-Mode devices as described in the previous section. The thickness of the second active/etch-stop layer is generally less than the critical thickness required for the formation of 2DEG at the hetero-interface. If the etching is selective the process stops once it reaches the etch-stop layer, it becomes a reproducible and repeatable technique.

The main shortcoming of the etch-stop layer fabrication technique is the lack of variability in options of the layer structure. In the GaN family of semiconductors only Aluminium Nitride (AlN) [76],[77] can be selectively chemically etched using warm ($>60^oC$) AZ400K developer solution [78],[79],[80] over other III-N materials

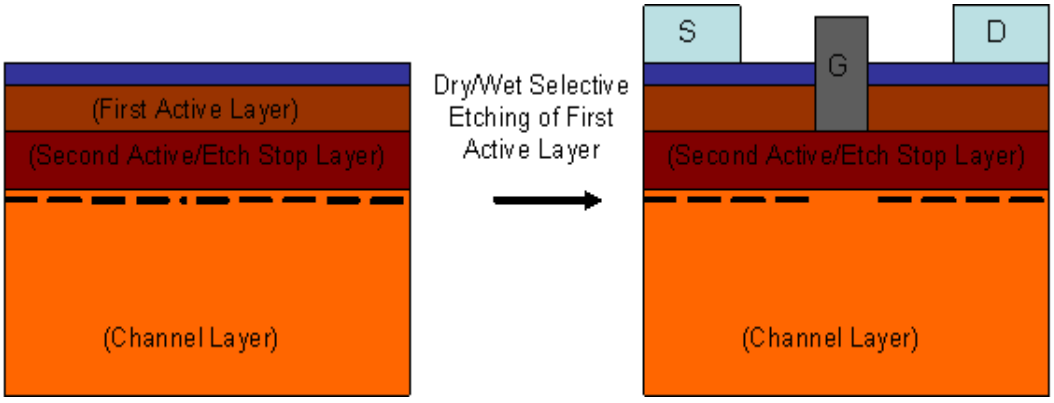


Figure 3.2: E-mode operation using selective barrier etching technique.

limiting the device structure to only have AlN as the top active layer. On the other hand, procedures involving dry recess etching technique the etch-stop layer is only limited to any Indium (In) related chemistries, such as InN, InGaN or InAlN as they require a very high table-temperature for etching [81],[82],[83].

Recently Anderson et al [77] used this technique to fabricate E-mode devices. The structure consisted of 4 nm AlN/8 nm AlGaN/2 μm GaN and the AlN active layer was selectively etched undeneath the gate-foot and E-mode operation was achieved. However, this epitaxial layer structure was not optimized and had very high sheet resistance (1100 Ω/sq), the 2DEG sheet carrier density ($\backsim$ 6 $\times$ 10^{12} cm^{-2}) and mobility ($\backsim$ 700 cm^2/V.s) were low and hence the full potential of the device structure was not achieved. Nonetheless, if this material system was properly engineered as will be demonstrated in Chapter 5 using numerical simulations, much higher performance devices compared to conventional devices could be achieved.

3.1.3 Fluorine Ion Implantation Technique

Ion implantation is a process in which ions of one material are implanted into another hereby changing the material properties of the latter. This method involves an ion source generating the desired ions, which are then impinged to the target material using a high voltage ion accelerator [84]. Currently, GaN based E-Mode devices are being fabricated using a localized ion implantation technique, which involves highly negative Fluorine (F^-) ions [85],[86],[87],[88]. The Fluorine ions are implanted in the barrier layer using a high-energy source ($\backsim 20-25$ keV) from a standard ion implantation machine, eg. Varian CF3000. The doping can be controlled using the dose (density of incident ions) and the energy of ions [89]. These negatively charged ions when implanted in the gate-foot region deplete the channel of electrons and this shifts the threshold of the devices in the positive direction as illustrated in Figure 3.3.

This process eliminates the dry etch problems incurred from recess RIE technique. However, the implanted fluorine ions have a tendency to move around in the GaN crystal lattice, which makes the devices very unstable and also degrades the drain breakdown voltage of the devices and hence reliability is an issue. Moreover, this method requires post implantation annealing for a long time at elevated temperatures ($>500^oC$) to repair the implantation-induced damage in the barrier and the buffer layers [89].

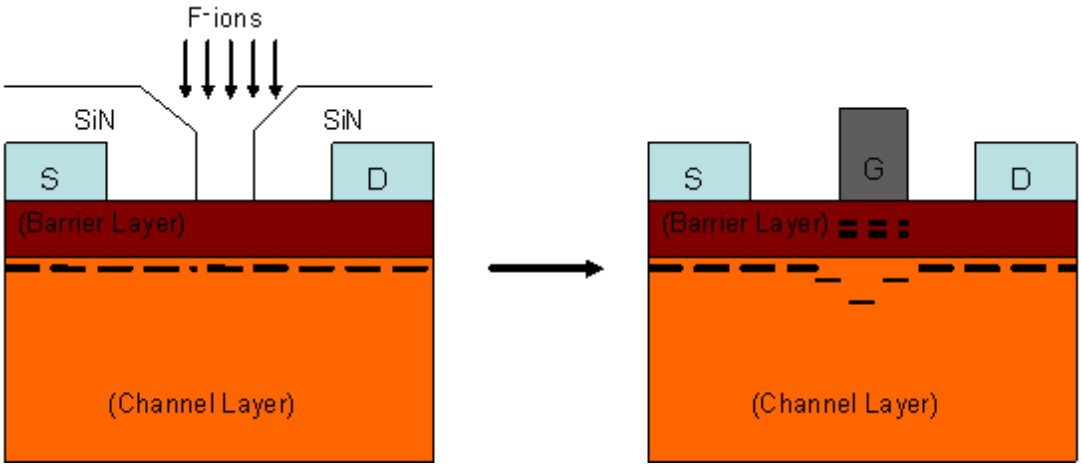


Figure 3.3: E-mode operation using Ion Implantation technique.

3.1.4 Ultra-Thin Barrier Layer HEMTs

In recent years ultra-thin barrier layers (AlN, InAlN) grown by direct epitaxy have attracted a lot of interest for E-mode devices [81],[90],[91]. Since the barrier layer is very thin ($\backsim 3-5$ nm) as compared to a standard 20 nm AlGaN barrier the 2DEG lies about 5-7 nm from the surface and can be easily modulated. In this case, the gate (Schottky) contact may be sufficient to deplete the channel of electrons and so it could be easier to fabricate E-Mode devices. In the InAlN/AlN/GaN material system described in reference [81], higher Al content increases the polarization effects resulting in higher 2DEG density and the high bandgap (AlN$\backsim$6.2 eV) helps in better electron confinement, reducing alloy disorders and improving low and high-field carrier transport qualities. The structure in Ref. [81] utilizes an n++ GaN cap layer which is selectively etched underneath the gate to achieve E-mode operation.

Inspite of the advantages of easy fabrication steps for E-Mode devices with AlN and better material properties there are a few significant drawbacks, which limits the development of devices with ultra-thin barrier layers. The main problem faced so far is material related since growth of high quality AlN wafer is still an issue [92], which restricts the achievement of the true potential of these device structures. Secondly, the barrier layer is ultra-thin and also the 2DEG lies very close to the surface. Thus, process chemicals and even atmospheric gases easily affect the channel and hence, proper passivation is necessary during processing [55].

3.1.5 P-Type Doping

This method involves the creation of a p-n diode under the gate-foot using an Mg doped (p-type) AlGaN or GaN based layer over a standard undoped AlGaN/GaN devices [93],[94],[95],[96] as shown in Figure 3.4. The localized p-type layer helps to uplift the potential of the channel beneath it by forming a p-n junction diode, which depletes the channel underneath it and hence facilitates to achieve a normally-off operation. However, with the increase of the gate voltage in the positive direction the diode starts to operate in forward bias allowing injection of holes in the barrier layer, which in turn attracts a lot of free electrons at the channel and allows conduction.

The main drawback of this technique is the creation of the p-type AlGaN or

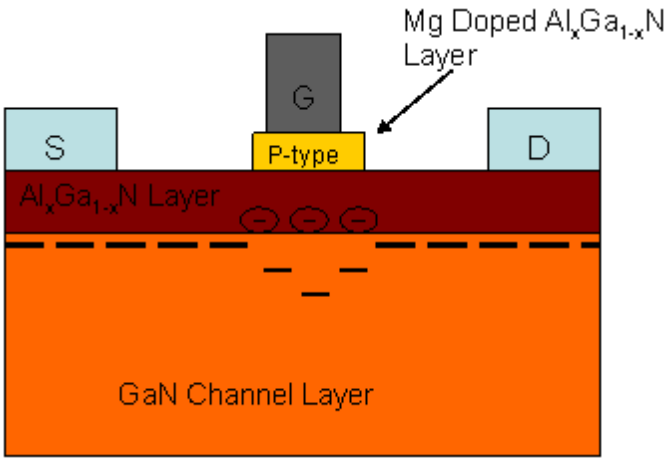


Figure 3.4: E-mode operation using P-Type doped localized barrier layer.

GaN layer selectively under the gate-foot, which can be realized either by selective growth or by selective etching of the p-type layer. Since after growth once the sample is taken out and processed its relatively complicated to re-grow another layer selectively on top it as it carries a high risk of contaminating the growth chamber. Also, due to the lack of availability of proper etch recipes for selective etching of p-type AlGaN or GaN layers its practically impossible to control the etch depth.

3.2 State-of-the-Art GaN Based E-Mode Devices

Fabrication of high performace GaN based "normally-off" devices with high output currents, operating at RF and microwave frequencies still remains a big challenge. Much attention has been given in the last decade to enhance the performance of the conventional E-mode device fabrication technology using several

process development techniques in order to achieve a threshold voltage of 1 V with a very high output current drive with very low On-resistance of the devices. Majority of E-mode devices fabricated using conventional techniques suffer from low drain output current ($\backsim < 500\ mA/mm$) as compared to their D-mode counterparts ($> 1000\ mA/mm$) which in turn increases the device resistance leading to high switching losses. It has been a big challenge so far to revive the entire current density of the devices as a significant amount of the 2DEG is lost after E-mode device fabrication as compared to their D-mode equivalents. However, higher $\mathbf{I}_{D,MAX}$ is only achievable with very narrow (sub-200 nm) gate lengths. Table 3.1 shows the DC characteristics of some of the state of the art GaN based E-mode devices fabricated in the last decade including their maximum drain current, threshold voltage and On-resistances.

As listed in Table 3.1, Saito et al [34], used gate recess technology to fabricate E-mode devices on standard AlGaN/GaN material, which shifted the threshold voltage from -4 V to $\backsim$ 0.14 V. However, the devices suffered from a very low maximum drain current ($I_{D,MAX}$) of 83 mA/mm and a high On-resistance of 400 $m\Omega.mm^2$. After Saito, several research groups used the gate recess technique with applied modifications to achieve high performance E-mode devices. In 2009, Kaneko et. al. [97], reported an E-mode AlGaN/GaN HEMT using gate recess and thermally grown nickel oxide (NiO_X) under the gate region and achieved a $I_{D,MAX}$ of 127 mA/mm with a V_{TH} of 0.8 V and a comparatively lower On-

$\mathbf{L}_G$ (μm)	$\mathbf{I}_{D,MAX}$ (mA/mm)	$\mathbf{V}_{TH}$ (V)	$\mathbf{R}_{ON}$ $m\Omega.mm^2$	**Device Technology**	**Reference**
1	83	$\backsim$ 0.14	400	Gate recess etching	[34]
2	127	0.8	280	Gate recess etching	[97]
1	240	0.018	500	Gate recess etching	[102]
0.8	800	3	$\backsim$ 53	Gate recess etching	[98]
0.16	1200	0.1	–	Recess + F^- ion implantation	[87]
1	400	0.5	12	F^- ion implantation	[69]
1	273	0.75	28	F^- ion implantation	[88]
1	420	2	23	F^- ion implantation	[99]
1.5	190	$0 - 3.5$	–	F^- ion implantation	[86]
1	300	0.75	25	F^- ion implantation	[103]
1	328	0.3	–	F^- ion implantation	[104]
2	$\backsim$ 130	$\backsim$ 0	3000	Ultra thin barrier	[105]
1.9	> 100	0.4	–	Ultra thin barrier	[106]
0.5	800	0.7	–	Ultra thin barrier	[81]
2	480	1	125	Ultra thin barrier	[100]
2	200	1	260	p-AlGaN	[95]
2	170	0	–	p-AlGaN	[101]

Table 3.1: State of the art DC characteristics of GaN-based E-mode HEMTs.

resistance of 280 $m\Omega.mm^2$ than Saito et. al. The latest results published in 2010 by Kanamura et. al.[98], reported a high performance GaN/AlN/GaN/AlGaN E-mode MISHEMT by combining multiple ultrathin barriers with gate recess technology. The 0.8 μm devices showed a high $I_{D,MAX}$ of 800 mA/mm with a threshold voltage of 3 V and a low specific R_{ON} of $\backsim$ 53 $m\Omega.mm^2$.

Apart from gate recess technology, other popular E-mode device fabrication technologies like flourine ion implantation, ultra thin and p-type doped barriers have also been researched in order to find a technology which is reproducible and reliable. Palacios et. al.[87], combined the gate recess technology with negatively charged flourine ion implantation to fabricate a state-of-the-art high performance E-mode device on a standard AlGaN/GaN material. These 160 nm devices exhibited a record output current of 1.2 A/mm with a V_{TH} of 0.1 V combined with a very high transconductance of over 400 mS/mm. These devices are still one of the best E-mode devices fabricated till date. However, the publication lacks information regarding the reproducibility of the technology. In the same year, Shuo Jia et. al.[69], employed CF_4 plasma in a RIE system at a power of 170 W for 120 seconds under the gate region to achieve E-mode operation. The devices with a threshold voltage of 0.5 V showed a $I_{D,MAX}$ of 400 mA/mm with an very low R_{ON} of $\backsim$ 12 $m\Omega.mm^2$. Inspite of the very low R_{ON} the devices suffered from low output current. In the same year using similar fabrication technique as S. Jia, Yong Cai et. al.[88], developed a normally-off (V_{TH} of 0.75 V) device with $I_{D,MAX}$

of 273 mA/mm and Ruonan Wang et. al.[99], reported devices with $I_{D,MAX}$ of 420 mA/mm and a V_{TH} of 2 V. The specific On-resistance for both the cases were low though the devices suffered a lot from low $I_{D,MAX}$.

Inspite of all the working devices reported by several research groups, the issue of reproducibility and repeatability of the gate recess and ion implantation techniques has been raised over the last few years. Hence, in the recent years using alternative E-mode device fabrication techniques like ultra-thin barriers or p-type doped barriers have attracted much attention since they can readily provide E-mode operation without involving any etching or ion implantation. In 2009, Ostermaier et. al.[81], developed E-mode devices using an n-doped GaN cap /ultrathin InAlN/AlN double barrier HEMT. The devices were fabricated by selective etching of the GaN cap using a gas mixture of silicon tetrachloride ($SiCl_4$) and suphur hexafluoride (SF_6) and direct Schottky contact of the gate metal with the InAlN barrier. The devices which showed a $I_{D,MAX}$ of 800 mA/mm and a V_{TH} of 0.7 V. Recently, IMEC, Belgium published results of a normally off (V_{TH} of 1 V) SiN/AlN/GaN/AlGaN DHFET on Si substrate. The devices were fabricated using a localized selective etching of SiN under the gate-foot region and the results showed a low $I_{D,MAX}$ of 480 mA/mm with a R_{ON} of $\backsim$ 125 $m\Omega.mm^2$ [100]. Medjdoub et. al., however, managed to address one of the most fundamental parameters for normally-off operation as the devices exhibited a V_{TH} of 1 V but the devices suffered from low current drive.

Yasuhiro Uemoto et. al. [95], reported a normally-off GaN-based transistor using conductivity modulation. This new device principle utilized hole-injection from p-AlGaN to AlGaN/GaN heterojunction. The fabricated devices exhibited a threshold voltage of 1 V with a $I_{D,MAX}$ of 200 mA/mm. The obtained on-state resistance was 260 $m\Omega.mm^2$. Similarly, Mitsuaki Shimizu et. al.[101], achieved normally-off operation by using a AlGaN/GaN/AlGaN double heterojunction layer structure. The aluminium compositions of the AlGaN heterobarriers were designed so as to deplete the electron carriers in the AlGaN/GaN/AlGaN channel, which gave a threshold gate voltage of about 0 V. The $I_{D,MAX}$ achieved was over 170 mA/mm.

As seen from Table 3.1 only a few groups have managed to fabricate normally-off devices which exhibited a combination of very high drain current and a very low On-resistance. Majority of device results presented showed an average $I_{D,MAX}$ of $\leqslant$ 500 mA/mm with a considerably high R_{ON} except a few groups who used sub 200 nm gate lenghts. However, none of the groups made a direct comparison between their E-mode and D-mode devices and hence it cannot be concluded whether their devices suffered any loss of the current density. Hence, based on the published results so far, the main objective of this research was to develop a new technology which can be used to fabricate E-mode devices which are capable of providing high drain output current with a very low On-resistance and the device characteristics are comparable with their D-mode equivalents.

CHAPTER 4

ENHANCEMENT-MODE DEVICE TECHNOLOGY BASED ON LOCALIZED GATE-FOOT OXIDATION

4.1 Introduction

This Chapter describes a new way of realizing enhancement mode GaN-based devices using the conventional AlGaN/GaN epilayer structure. The technique developed relies on the uniform oxidation of the AlGaN barrier layer. It overcomes most of the limitations of the presently used E-mode device technologies. Achieved experimental results show that the new approach could lead to the realization of very high performamce E-mode devices.

4.2 AlGaN/GaN HEMT Structure

Two AlGaN/GaN HEMT structures were used in this study and were both grown using Molecular Beam Epitaxy (MBE) on sapphire substrate (Al_2O_3) with a Ga-face (0001) orientation. One structure was supplied by SVT Associates from the USA and the other by NTT Corp. from Japan. The structure from SVT Associates was described in Section 2.2, Chapter 2 (Figure 2.1). This structure was used in initial tests for the new device concept to be described in this chapter.

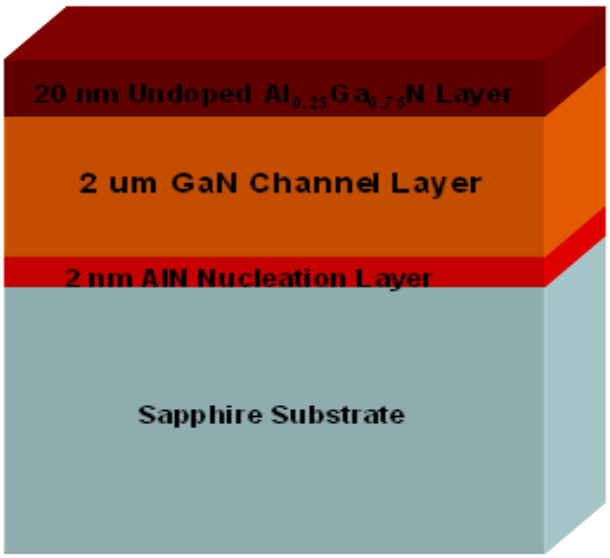


Figure 4.1: AlGaN/GaN HEMT structure used in the project for device fabrication.

The structure of the material from the Japanese supplier is shown in Figure 4.1 and consists of (from top) an undoped 20 nm $Al_{0.25}Ga_{0.75}N$ layer followed by a 2 μm undoped GaN buffer layer grown on sapphire with a thin AlN nucleation layer sandwiched between the substrate and the buffer layer with a 2DEG concentration of $1.1 \times 10^{13} cm^{-2}$ and a mobility of $\backsim$ 1600 cm^2/V.s.

4.3 Barrier Layer Oxidation under the Gate-Foot

A dry oxidation technique was originally developed by Masato et al.[107] for device isolation in AlGaN/GaN devices. On this basis, oxidation of AlGaN in dry oxygen ($800^0C - 900^0C$) was initially investigated. If successful, selective oxidation of the AlGaN layer underneath the gate-foot could be employed for the

effective thinning of this barrier layer and thereby achieving E-mode operation by locally reducing/eliminating the 2DEG carrier concentration. The mixture of the aluminum and gallium oxide created by the oxidation process also serves as a good gate dielectric, which helps in reducing the gate leakage.

The AlGaN/GaN structure described above was used for device fabrication using selective oxidation of the AlGaN layer underneath the gate-foot region for effective barrier thinning and locally reducing/depleting the 2DEG channel. Theoretically, at higher positive gate bias voltages carriers are attracted to re-form the channel with no loss in the output drain current. Initially, the AlGaN barrier layer was oxidized directly without any special precautions. Fabrication steps for the proof-of-concept are detailed below and also illustrated in Figure 4.2. This approach could have major benefits over conventional methods as discussed below:

1. It effectively thins the barrier without any physical etch or ion implantation and the rate of thinning (oxidation) can be accurately controlled by the oxidation temperature and time.

2. The oxidation process uses the aluminium and gallium from the barrier layer to form aluminium oxide (Al_2O_3) and gallium oxide (Ga_2O_3), which when grown at high temperatures like 800^0C and above is highly crystalline and provides with a good dielectric/insulator under the gate foot [108]. This dielectric/insulator underneath a field plate improves the device breakdown voltage and can further enhance the device performance by reducing the

gate leakage current.

3. Since the device is fabricated from the standard AlGaN/GaN structure both E-mode and D-mode devices can be fabricated on the same chip for digital logic applications in harsh environments.

4.4 Kinetics of Oxidation Mechanism

Thermally grown silicon dioxide is used in all silicon MOS technologies except for sub-50nm nodes. High quality thermally grown oxides (titanium-aluminium oxide, hafnium-aluminium oxide, aluminium oxide, etc) have recieved much attention recently for use as high-k dielectrics for wide bandgap MOSFETs [109]. Hence, knowing the kinetics of the mechanism regarding the formation of the above-mentioned oxides is very important. The main factor that controls the oxidation kinetics is the rate of diffusion of the oxidizing species through the thin films of oxide to reach the material (metal/semiconductor) and form a new oxide layer making the film thicker. However, the rate of diffusion depends on several important factors like oxidization temperature, pressure, the activation energies (higher activation energies are required for a dry oxidation process than wet oxidation) and also the volume of the oxidant reaching the material surface [109].

Based on the experimental data available for metal or semiconductors, it is believed that the oxidation process takes place by the inward movement of the oxidizing species (oxygen molecules) rather than the outward movement of the

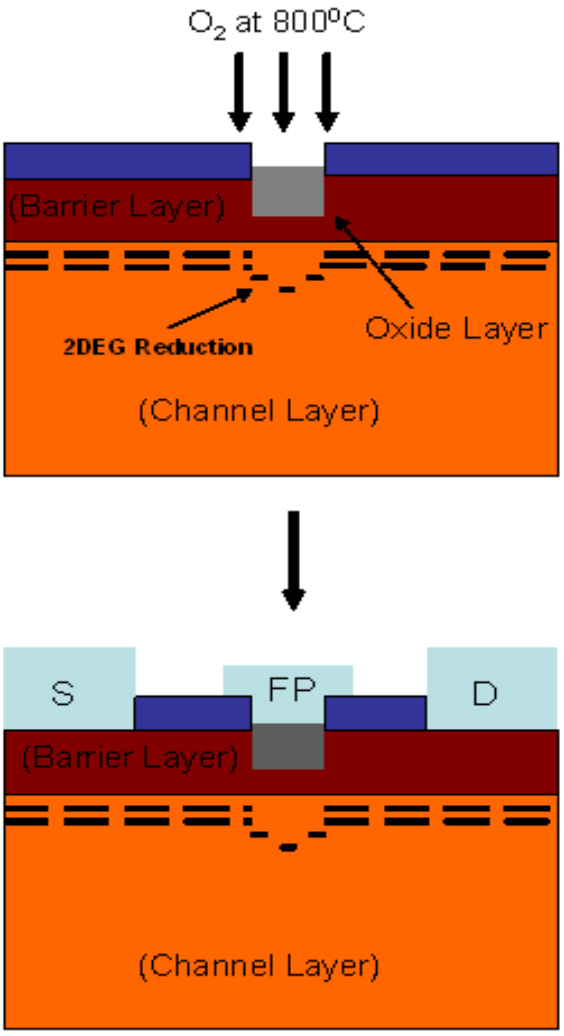


Figure 4.2: Concept and process flow for AlGaN/GaN MOS-HEMTs.

material [109],[110],[111],[112]. The entire oxidation procedure is based on the following events:

1. The oxidizing agent (oxygen molecules) attacks the material's surface to form the first thin layer of oxide film.

2. The agent is absorbed by the upper layer of the film and diffuses through it to reach the material's surface.

3. The agent reacts with the material to form a further oxide film, which makes the oxide thicker.

As shown in Figure 4.3, the oxidizing agent diffuses from outside through the oxide film to reach the material surface and in the process the oxide film thickens. However, based on a fixed rate of diffusion through any oxide the rate of oxidation of the material slowly decreases as the oxide film thickens (x_0 increases) and the time required by the oxidant to reach fresh material surface increases. Hence, based on the steady state condition of rate of diffusion through any oxide film it can be concluded that the rate of oxidation for a longer period of time can be either parabolic or logarithmic. Based on experimental data it was deduced that for a longer period of oxidation the thickness of the oxide film (x_0) is directly proportional to the square root of the time (t) and can be expressed as [109],[113],[114],[115]:

$$x_0^2 \cong B \times t$$

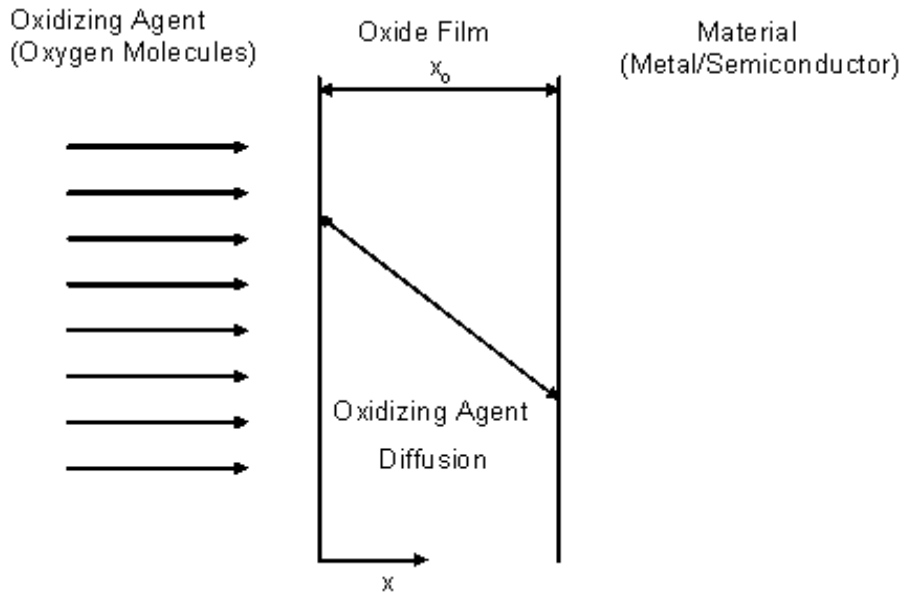


Figure 4.3: Illustrative model of the oxidation procedure.

where B is the parabolic rate constant of oxidation and is material specific for different oxidation parameters.

4.5 Gate-Foot Oxidation Technology

4.5.1 Direct Oxidation of the AlGaN Barrier Layer

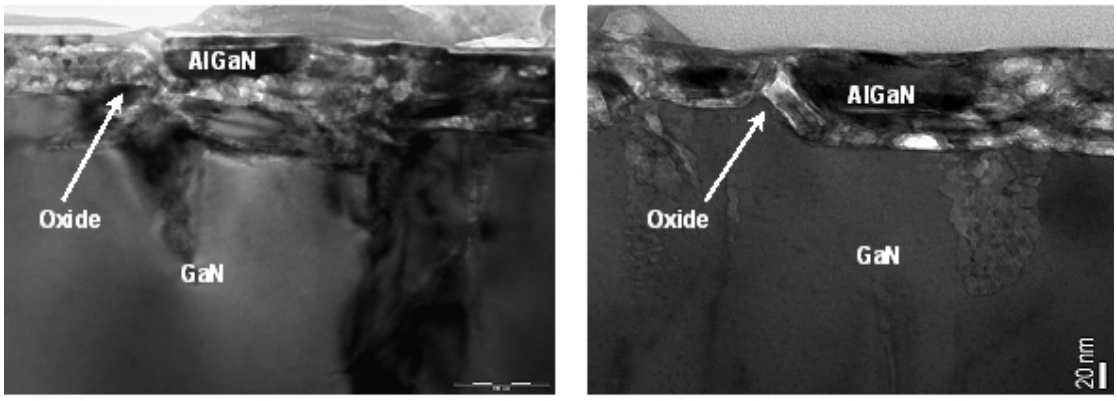
Localized gate-foot oxidation technology was attempted before on the AlGaN/GaN structure by Roccaforte et al [116] and Mistele et al ,[117]. This approach was also attempted in the InAlN/GaN material system by Alomari et al [118]. Whilst good results were achieved for the InAlN/GaN material system, the experimental results for the AlGaN/GaN material system were poor and E-mode operation was not achieved.

Initial investigations focussed on the oxidation of the AlGaN barrier layer. Samples from SVT Associates, USA, which were similar to the material described in section 2.2, Chapter 2 (Figure 2.1) were used. This sample consists of a 2 nm GaN cap layer on top of a 20 nm undoped $Al_xGa_{1-x}N$ (Aluminium content, $x = 35\%$) barrier layer followed by a 3 μm undoped GaN buffer layer, which is grown on a very thin (2 nm) AlN nucleation layer sandwiched between the GaN buffer layer and the 350 μm sapphire substrate.

In order to evaluate how the AlGaN barrier oxidizes, transmission electron microscopy (TEM) analysis were done on directly oxidized samples. Sample preparation were carried out using a standard cross-section encapsulation method to prepare 3 mm electron transparent discs from oxide/AlGaN/GaN thin samples known as thin foils or lamellae with a 40 nm platinum coating layer. Special care was taken in order to reduce any sample damage during sample preparation related to lamella thickness, preparation speed or the amount of amorphous material left from the preparation process [119]. Obtaining uniform lamella thickness is critical since it helps to reduce any edge or interface effects and facilitates accurate TEM analysis. The thinning process is carried out by the ion milling by a precision ion polishing system (PIPS) using a focussed ion beam (FIB) [119],[120]. The discs were carefully centred in a suitable sample holder and placed into the PIPS where two Ar ion beams milled away material from the centre of each dimpled surface. The sample during this process is kept rotating and the two Ar ion guns are placed

above and below with respect to the sample. FIB-based preparation systems leave behind a damaged surface after milling. The thickness of this damaged layer depends on the orientation of the FIB beam to the sample surface (typically a few degrees) as well as the beam energy [120]. Each beam was incident on the surface with an angle of 4^o for this purposes. For these films ion beam energy of 4 kV was used until a hole was observed in the glue line. Once the hole appeared the ion energy was dropped down to 2 kV in order to obtain a smooth surface and less damage [120].

Two samples were directly oxidized in an Annealsys's AS-ONE rapid thermal annealer (RTA), one for 5 mins and the other for 10 mins at 800^0C. Cross-sectional TEM analysis of both the samples were carried out and the TEM pictures are shown in Figure 4.4a and Figure 4.4b. The oxide, AlGaN and GaN layers are marked in the pictures and show that the oxide layer is not only on top of the barrier layer but penetrates through parts of the barrier and has also formed at the hetero-interface. These results show that the oxidation was not uniform from the top but rather throughout the barrier layer (assumed to be along the dislocation/defect sites). The oxidation rate within the barrier seems to be at a much faster rate. Figure 4.5 shows the oxygen mapping in the oxidized barrier confirming the non-uniform oxidation. However, it must be noted that due to limited TEM access, comparison could not be made to sample prior to oxidation process.



(a) (b)

Figure 4.4: Cross-sectional TEM analysis showing the non-uniformity of the oxidation rate at the dislocation sites.

The dislocation/defect regions oxidize at a much faster rate resulting in the formation of the oxide non-uniformly over the entire barrier as shown in the oxygen mapping in Figure 4.5. This pattern of non- uniform oxidation along defects completely agrees with the work and analysis done by Roccaforte et al [116] and Mistele et al ,[117]. which completely destroys the 2DEG leading to drastic fall in the output current as discussed in Reference [117]. Therefore this approach could not be used to realize devices unless a method to ensure uniform oxidation of the AlGaN barrier layer was developed.

4.5.2 Schottky Device Fabrication

To evaluate the effect of thermal oxidation of the gate-foot area on device performace two separate samples of $Al_{0.35}Ga_{0.65}N$/GaN (Grower: SVT Assoc.) were

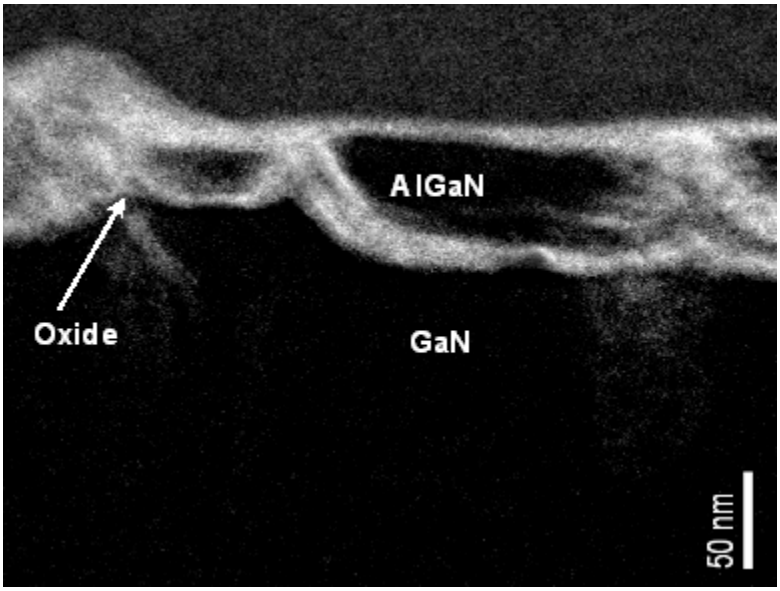


Figure 4.5: Cross-sectional TEM analysis showing the Oxygen mapping. The white patches in the picture are the oxygen rich (oxide) areas.

processed. One a conventional Schottky gate device and the other was oxidized under the gate-foot for 2 min at 800^oC using a simple gate wrap-around device structure [121] as shown in Figure 4.6. The device consists of two ohmic contacts for the source and the drain electrodes, but the drain contact is encircled by the Schottky gate. An SEM picture of the completed device is shown in Figure 4.6.

An illustrated version of the process flow used to fabricate the Schottky devices is shown in Figure 4.7. This process is not the standard way of fabricating D-mode devices but has been modified to incorporate steps required to oxidize the gate-foot region so that a comparison with the new MOS-HEMT devices can be made. The process flow of the fabricated Schottky gate device is given below and

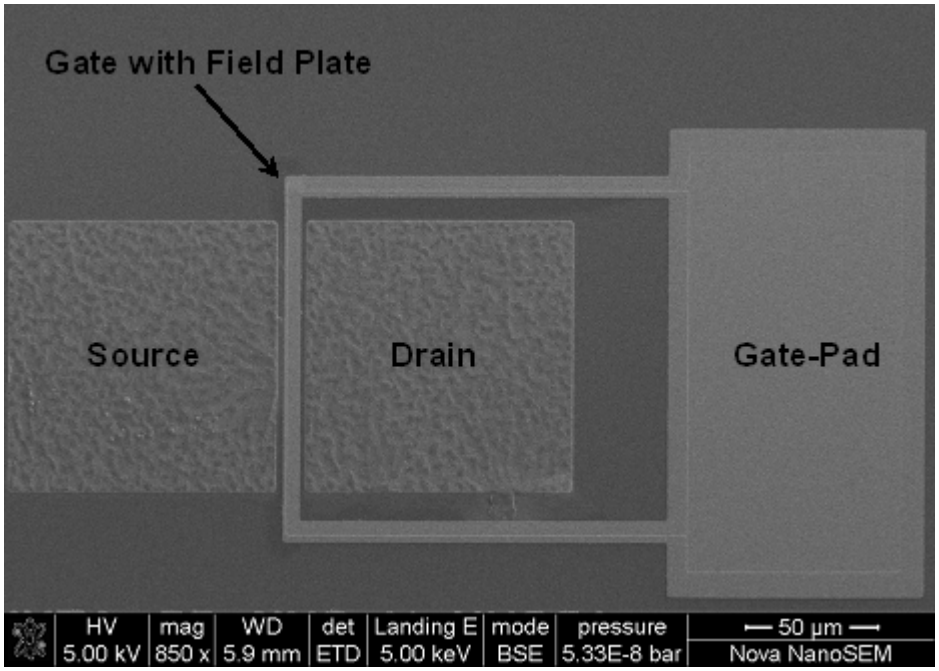


Figure 4.6: SEM picture of the device structure fabricated for DC Measurements.

details of all key process steps are given in Appendix C.

1. Deposition of 150 nm Inductive Coupled Plasma Silicon Nitride (SiN) all over the sample. The SiN has a very high thermal stability and is used as a hard mask to protect the rest of the device during the gate-foot oxidation process at high temperatures (800^0C). For this Schottky gate process the SiN only acts as a passivation layer.

2. Definition of ohmic contacts (source and drain contacts) using photolithography.

3. Dry Etching of SiN using SF_6/N_2 gas in RIE machine (80+RIE).

4. Metal deposition for ohmic contacts [Titanium (30 nm) / Aluminium (180 nm) / Nickel (40 nm) / Gold (100 nm)] using conventional lift-off technique followed by annealing at 800^0C for 30 sec in N_2 environment.

5. Alignment of gate contact using photolithography and dry etching of SiN using SF_6/N_2 gas in RIE machine (80+RIE).

6. Alignment of field plate and deposition of metal [Nickel (50 nm) / Gold (150 nm)] using conventional lift-off technique.

The 2 $\mu m \times 100$ μm effective gate device consists of 100 $\mu m \times 100$ μm ohmic contacts, a source-drain distance (L_{SD}) of 12 μm, gate-source (L_{GS}) and gate-drain (L_{GD}) distance of 5 μm.

A field plate (FP) is generally used to enhance the breakdown voltage of MOS devices by uniformly spreading the electric field over the effective gate and the drain region and is usually fabricated with a longer edge towards the drain contact. Furthermore, gate based FPs tend to increase the effective area of the gate region thereby, increasing the gate capacitance thus detoriorating high frequency device performance [122]. For the MOS-HEMT device fabrication the sole purpose of the FP was to avoid any alignment errors during the photolithography of the gate-foot region and hence the metal edges are kept symmetrical on both sides of the gate. Further process development is required in the future to optimize the metal edges of the FP to enhance breakdown voltage and high frequency operation of the RF MOS-HEMT devices.

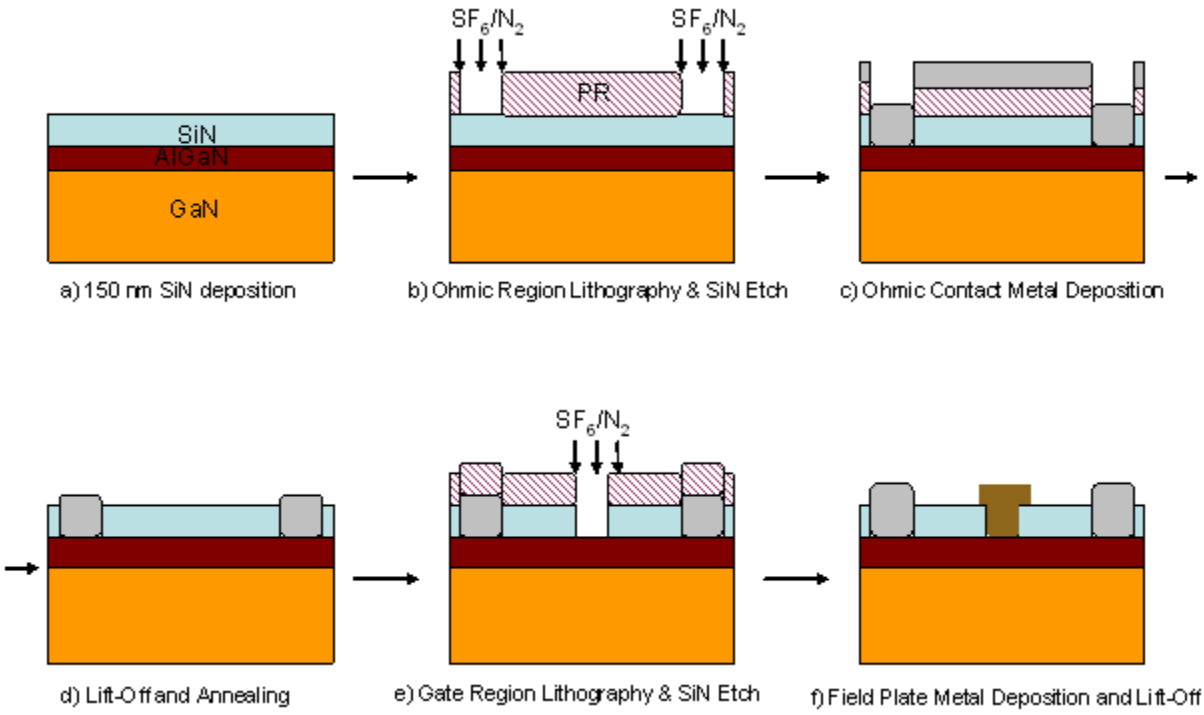


Figure 4.7: Process flow for Schottky device fabrication.

4.5.3 MOS-HEMT Device Fabrication with Direct Oxidation of AlGaN Barrier

In order to compare the electrical properties of the MOS-HEMT device with the Schottky (reference) device, a similar MOS-HEMT device with the same dimensions as the reference device was fabricated. The barrier of the MOS-HEMT device was locally oxidized under the gate-foot region in order to effectively thin the barrier. The process flow used to fabricate the MOS-HEMT device is given below and an illustrated version of the same is shown in Figure 4.8.

1. Deposition of 150 nm Silicon Nitride (SiN) all over the sample using Inductive Coupled Plasma (ICP).

2. Gate alignment using optical lithography. Gate foot defined in SiN for eventual oxidation with SiN as a mask.

3. Dry etching of SiN with SF_6/N_2 gas (RIE) using photoresist as an etch mask.

4. Oxidation of the barrier in an RTA in O_2 environment at 800^0C for 2 min in order to reduce the barrier thickness accordingly.

5. Etching of SiN using RIE with SF_6/N_2 to define ohmic contact areas.

6. Alignment of ohmic contacts followed by deposition of a metal stack of Ti (30 nm)/Al (180 nm)/Ni (40 nm)/Au (100 nm). This is then annealed at 800^0C for 30 sec in N_2 environment.

7. Deposition of Field Plate over the gate foot, Ni (50 nm) / Au (150 nm).

Comparison of the $I_D - V_D$ characteristics of both the devices measured using a B1500A Semiconductor Parameter Analyzer (SPA) are shown in Figure 4.9. The unoxidized sample (shown in red), which is a normal Schottky gate device, has a threshold voltage of -5 V and reaches full current compression for a gate voltage $V_{GS} = 3\ V$. Current compression in a MOS-HEMT is a term used to define the reduction in the slope of the transfer characteristics of the device. In this case, further enhancement of the gate bias voltage ($V_{GS} \geq 3\ V$) does not attract any more carriers in the channel and hence their is no increment in the output drain current as can be seen from the top most trace of the Schottky device (red trace) for $V_{GS} = 3\ V$ as shown in Figure 4.9. Thus the output current is considered to be fully compressed for $V_{GS} \geq 3\ V$. On the other hand, the oxidized sample's (shown in blue) threshold has been moved from -5 V to 0 V and there is no current compression at $V_{GS} = 3\ V$. These results seemed to show that the oxidation process modifies the barrier as the threshold voltage was shifted but there is a significant drop in the maximum drain current of the device (0.65 A/mm for the un-oxidized sample and 0.28 A/mm for the oxidized sample). It would seem that the large drop in output current is due to the non-uniform oxidation of the barrier layer as described by Roccaforte et al [116] and Mistele et al ,[117]. The comparison between the Schottky and MOS-HEMT devices fabricated by direct oxidation of the $Al_{0.35}Ga_{0.65}N$/GaN barrier is given in Table 4.1.

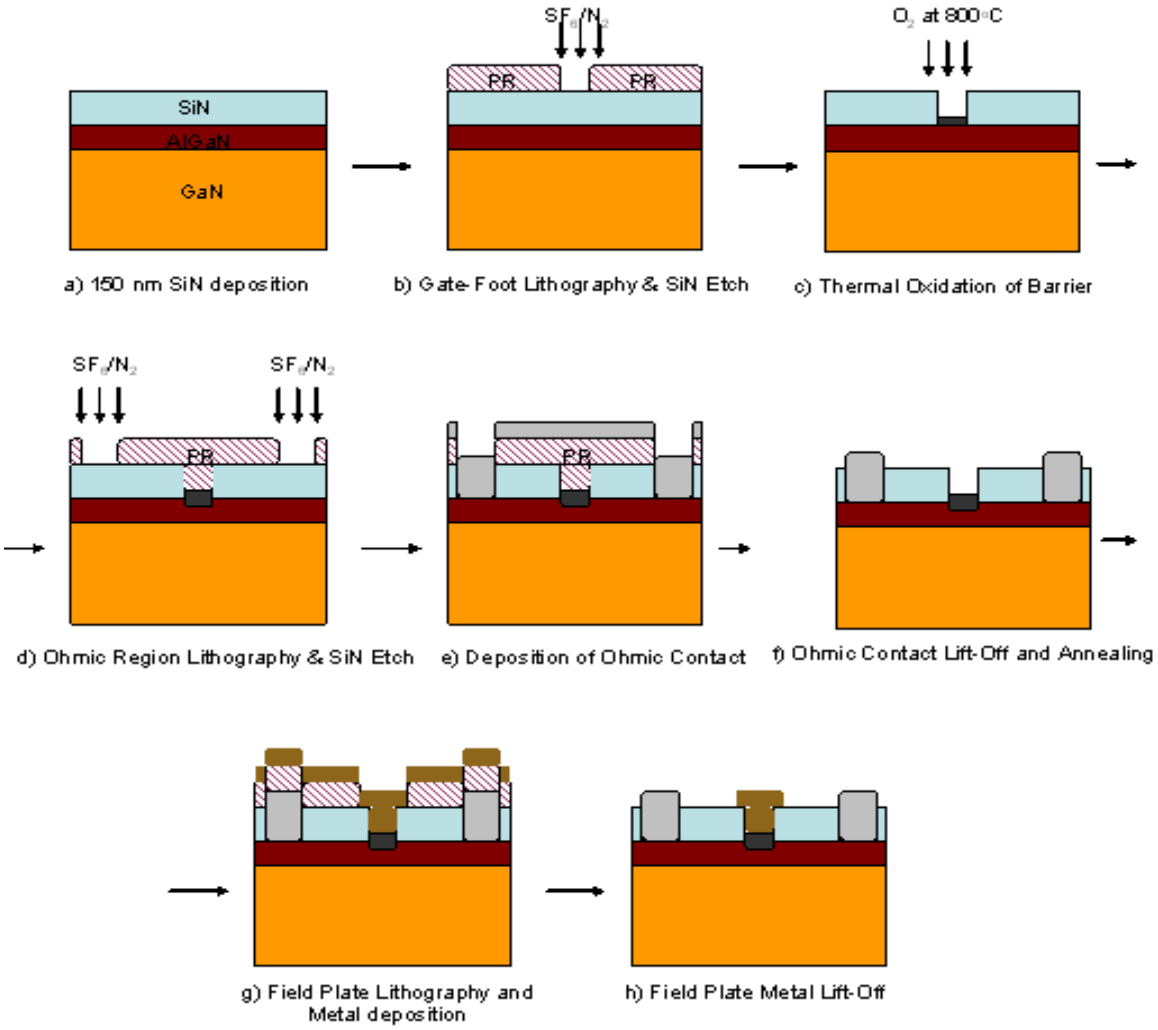


Figure 4.8: Process flow for MOS-HEMT device fabrication with direct oxidation of the AlGaN barrier.

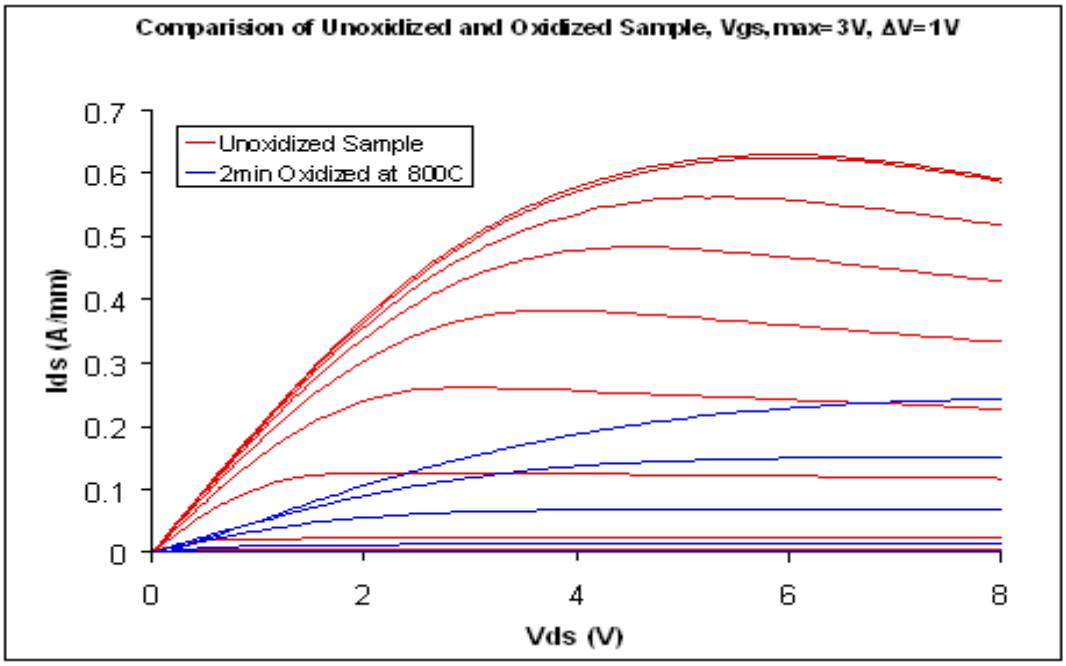


Figure 4.9: Graph comparing the electrical characteristics of an un-oxidized sample and sample oxidized for 2 min at 800^0C without any protection layer

Device	**Threshold Voltage** V_{TH} (V)	**Maximum Drain Current** $I_{DS,MAX}$ (A/mm)
Schottky	-5	0.65
MOS-HEMT	0	0.28

Table 4.1: Comparison of electrical characteristics between Schottky and MOS-HEMT devices fabricated with direct oxidation of the AlGaN barrier

4.5.4 Al-capped Oxidation Approach of the AlGaN Barrier Layer

TEM analysis proved that direct oxidation of the barrier layer could not be used to fabricate devices because of its non-uniformity of the formed oxide, which practically renders the barrier useless. Hence, to protect the dislocation sites a very thin layer of aluminium (2 nm) was deposited before oxidation of the samples. The samples were then annealed at 800^0C for 30 sec in N_2 environment in a rapid thermal annealer (RTA) for proper integration of aluminium with the barrier layer making it Al-rich. The reason for using 800^0C as the annealing temperature is that the oxide created at this temperature provides the best morphology with GaN crystals [108]. They were then oxidized for 2.5 mins at 800^0C in the RTA in an O_2 environment.

Scanning transmission electron microscopy (S-TEM) analysis was performed on the samples and a micrograph of this analysis is shown in Figure 4.10. The oxide, AlGaN and GaN layers are marked and are clearly in the expected order with the oxide layer only at the top. It would therefore seem that depositing an aluminium layer on top significantly improves the quality and the uniformity of the oxidation. During oxidation, the Al oxidizes first forming Al_2O_3 which acts as a protective layer and deters the dislocation sites from being oxidized. When oxidized for a longer time the oxide grows uniformly underneath the initial

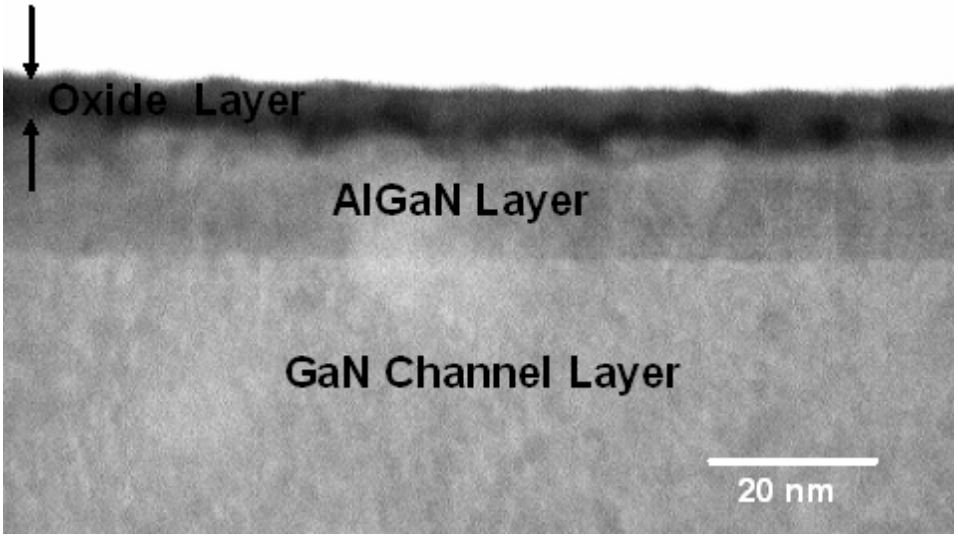


Figure 4.10: Cross-sectional S-TEM analysis showing the uniformity in the oxide growth.

Al_2O_3 layer consuming the barrier layer's aluminium and the barrier height thins uniformly.

The rate of oxidation as extracted from the cross-section after 2.5 mins of oxidation shows a average growth rate of 2 nm/min for the semiconductor itself with a total oxide thickness of around 9 nm. The oxide consists of the initial 2 nm aluminium (4 nm oxide) and the 5 nm from the AlGaN barrier layer as 15 nm of the barrier was still found intact. The average oxide growth rate of the semiconductor has only been explained since detailed analysis are required to provide experimental evidence to whether or not the entire deposited Al layer was oxidized prior to the oxidation of the AlGaN barrier layer. Furthermore, the rate of oxidation (for both metal and semiconductor) is parabolic and is inversely proportional to the oxide thickness as the diffusion time of the oxidant increases

with the formed oxide. Further extensive TEM analyses are required to determine the presence of any initial native oxide formed due to the deposition of the Al layer and especially to evaluate the rate of the oxide growth for different oxidation times in order to determine the parabolic rate contact for this specific AlGaN/GaN material.

4.6 Device Fabrication and Characterization with Al-capped Oxidation Approach

4.6.1 Schottky Device Characteristics

Due to insufficient availablity of the $Al_{0.35}Ga_{0.65}N/GaN$ material due to growth problems from the supplier (SVT Assoc.) a separate layer structure as described in Section 4.1 (Figure 4.1) was used for the rest of the experimental procedures. Since, a different layer structure was going to be used for the rest of the fabrication process a reference Schottky device was fabricated using a similar process flow and device dimensions described for Schottky devices in the previous section in order to assess the D-mode device characteristics of this new $Al_{0.25}Ga_{0.75}N/GaN$ material structure (supplier: NTT Corp., Japan). The $I_D - V_D$ characteristics of the device were measured using B1500A SPA for gate biases varying from -5 V to 3 V for a maximum drain bias (V_{DS}) of 10 V as shown in Figure 4.11. The maximum drain current $I_{DS,MAX}$ obtained for a gate voltage $V_{GS} = 3\ V$ is 620 mA/mm. The transfer characteristic ($I_D - V_G$) of the device is shown in Figure 4.12. The transfer

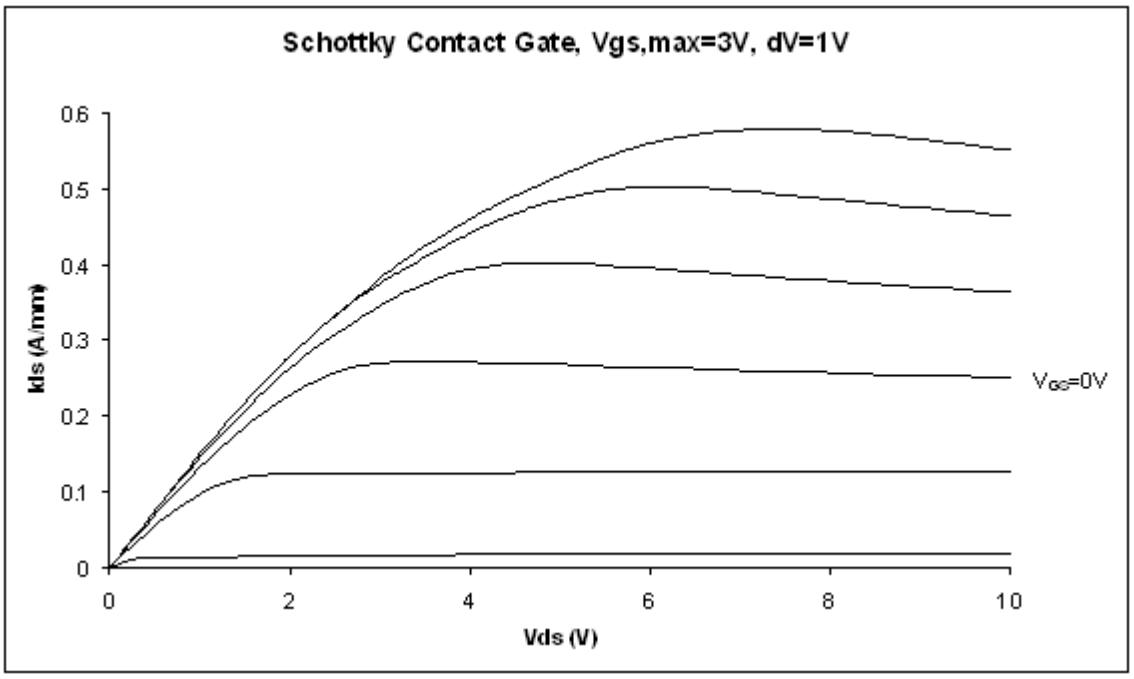


Figure 4.11: $I_D - V_D$ characteristics of the $Al_{0.25}Ga_{0.75}N$/GaN Schottky (reference) gate contact device.

and transconductance characteristics of the Schottky gate device shows that the threshold voltage (V_{TH}) of the device to be -3.1 V. The peak transconductance ($G_{M,PEAK}$) was calculated to be 154 mS/mm and is obtained between a gate bias of -2 V and -1 V.

4.6.2 MOS-HEMT Device Fabrication Process Flow

In order to shift the threshold voltage of the D-mode structure to realize normally-off operation, the gate-foot region of the samples were selectively oxidized using the thin aluminium protection layer as described in the previous

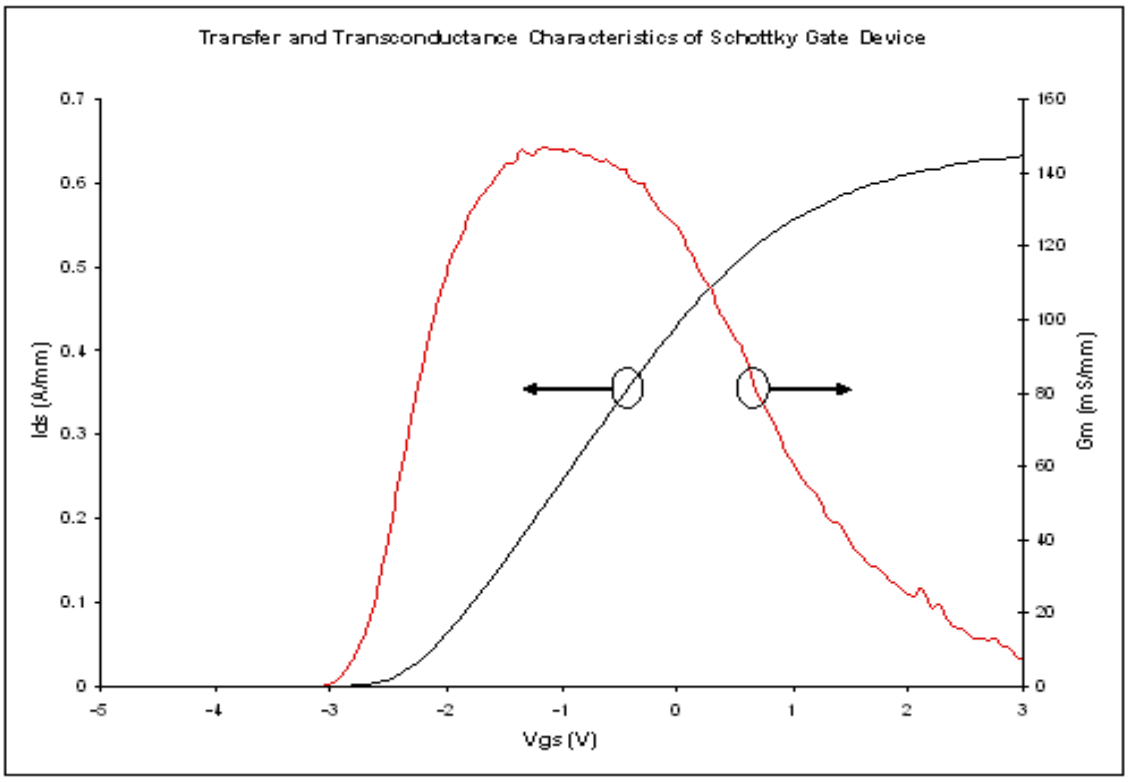


Figure 4.12: $I_D - V_G$ and G_M characteristics of the Schottky gate device.

sections. An illustration of the process is shown in Figure 4.13 and is described below.

1. Deposition of 150 nm Silicon Nitride (SiN) all over the sample using Inductive Coupled Plasma (ICP).

2. Gate alignment using optical lithography. Gate foot defined in SiN for eventual oxidation with SiN as a mask.

3. Dry etching of SiN with SF_6/N_2 gas (RIE) using photoresist as an etch mask.

4. Deposition of a thin ($\backsim$ 2 nm) aluminium layer using conventional lift-off.

5. Annealing of the aluminium at 800^0C for 30 sec in N_2 environment for proper integration with the upper layer of the barrier.

6. Oxidation of the barrier in an RTA in O_2 environment at 800^0C for a desired time span in order to reduce the barrier thickness accordingly.

7. Etching of SiN using RIE with SF_6/N_2 to define ohmic contact areas.

8. Alignment of ohmic contacts followed by deposition of a metal stack of Ti (30 nm)/Al (180 nm)/Ni (40 nm)/Au (100 nm). This is then annealed at 800^0C for 30 sec in N_2 environment.

9. Deposition of Field Plate over the gate foot, Ni (50 nm) / Au (150 nm).

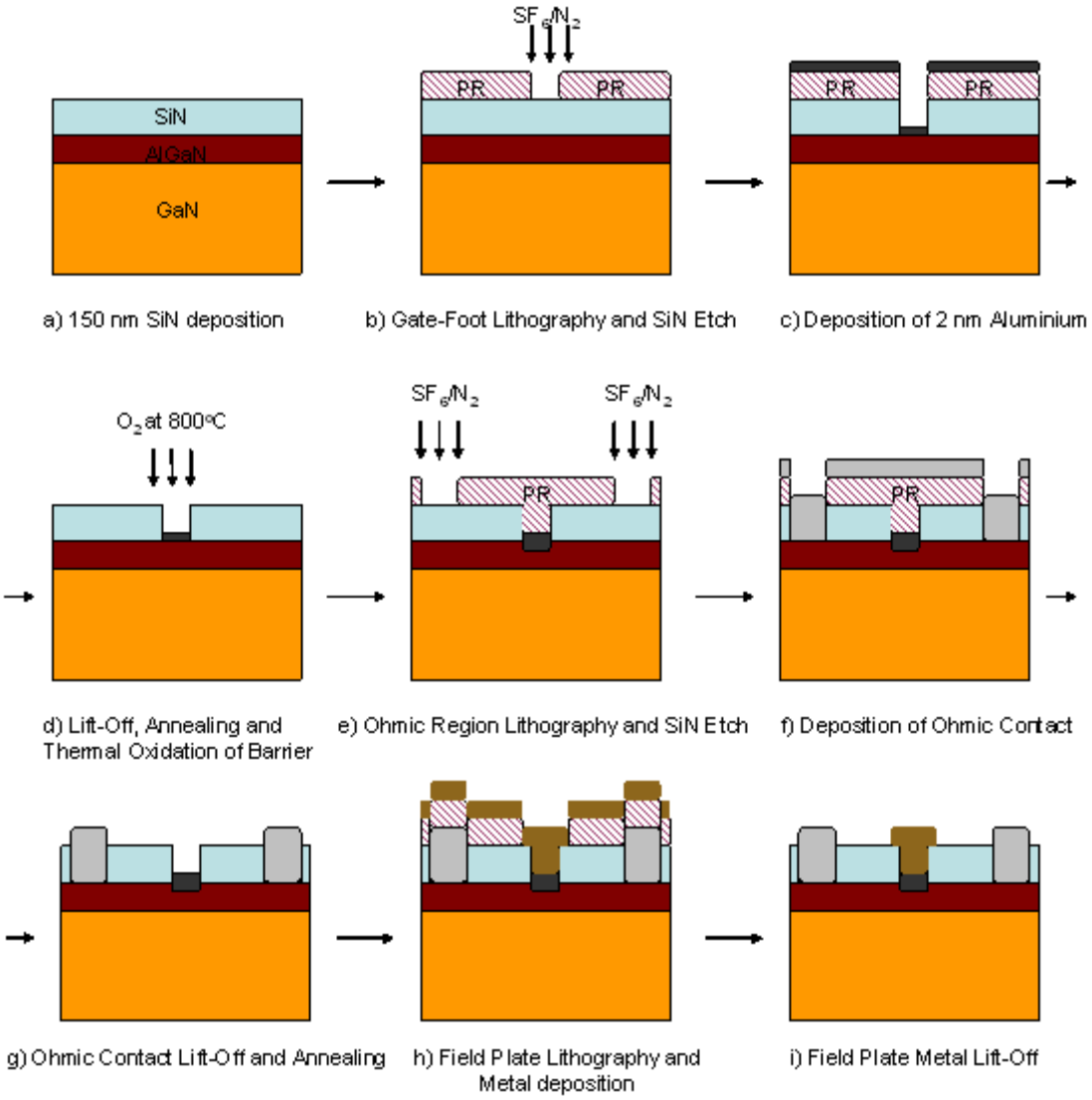


Figure 4.13: Illustrative version of the process flow for MOS device fabrication.

4.6.2.1 Discussion

This modified approach proved to form a uniform oxide layer and consistent barrier thinning and the fabricated devices showed a uniform shifting of the threshold voltage. During the initial stages of experiments, samples which were oxidized for more than 6 minutes completely lost gate control. Figure 4.14 shows an example measurement of $I_D - V_D$ characteristics (SPA measurement format) of a device oxidized for 8 minutes. It was unclear as to why the devices behaved this way. To investigate this problem, several samples were annealed for 30 sec at temperatures 650^0C, 700^0C, 750^0C and 800^0C and then they were oxidized for 8 and 10 minutes at 800^0C. The devices which were annealed at 650^0C and 700^0C are the only ones which retain gate control for longer periods of oxidation. Hence, based on these results the rest of the samples were annealed for 30 sec at 700^0C in N_2 environment prior to oxidation at 800^0C for the required times. Further analysis needs to be done to understand details of the oxidation process.

4.6.3 MOS-HEMT Device Characteristics

In order to assess the effect of high temperature thermal oxidation on the shift of the threshold voltage of the MOS-HEMT devices, several samples were oxidized using the process flow mentioned above. The dimensions of the MOS-HEMT devices were kept the same as the Schottky device for ease of comparison. The $I_D - V_D$ characteristics of the devices with 2 min and 4 min oxidation at

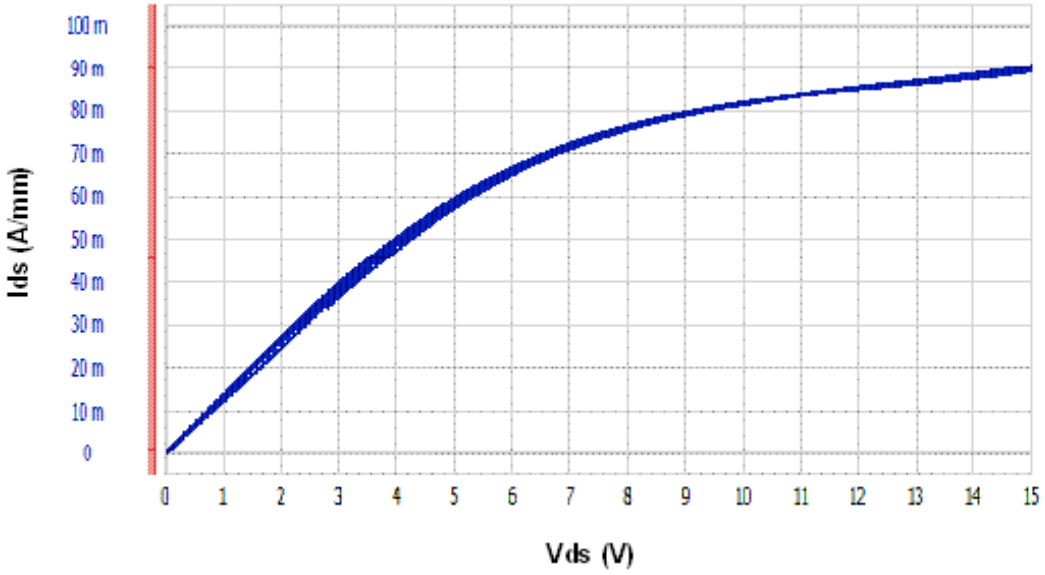


Figure 4.14: $I_D - V_D$ characteristics of a device oxidized for 8 min showing no gate control.

800^0C with prior annealing at 700^0C for 30 sec in N_2 environment are shown in Figure 4.15 and 4.16, respectively. It indicates a shift of the I_{DSS} (drain current at $V_{GS} = 0\ V$) as compared to the Schottky device which means the barrier layer is thinning during oxidation but probably oxidation for such short duration (2 and 4 min) does not thin the barrier enough so that a significant shift in the threshold voltage can be noticed. Based on these results, samples were then oxidized for 8 min and 15 min. The $I_D - V_D$ characteristics of the MOS devices with 8 min and 15 min oxidation are shown in Figure 4.17 and 4.18, respectively.

The $I_D - V_D$ characteristics shown in the graphs depict a shift of the threshold voltage in the positive direction leading to the maximum drain current being

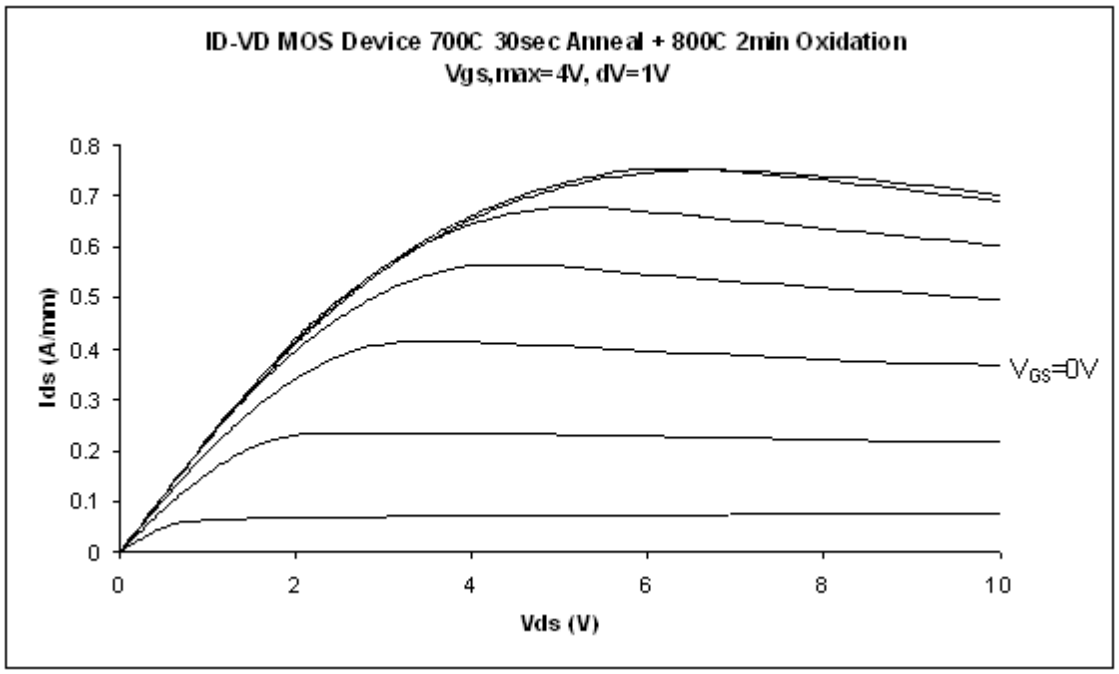


Figure 4.15: MOS-HEMT Device $I_D - V_D$ characteristics with 2 min Oxidation at 800^0C.

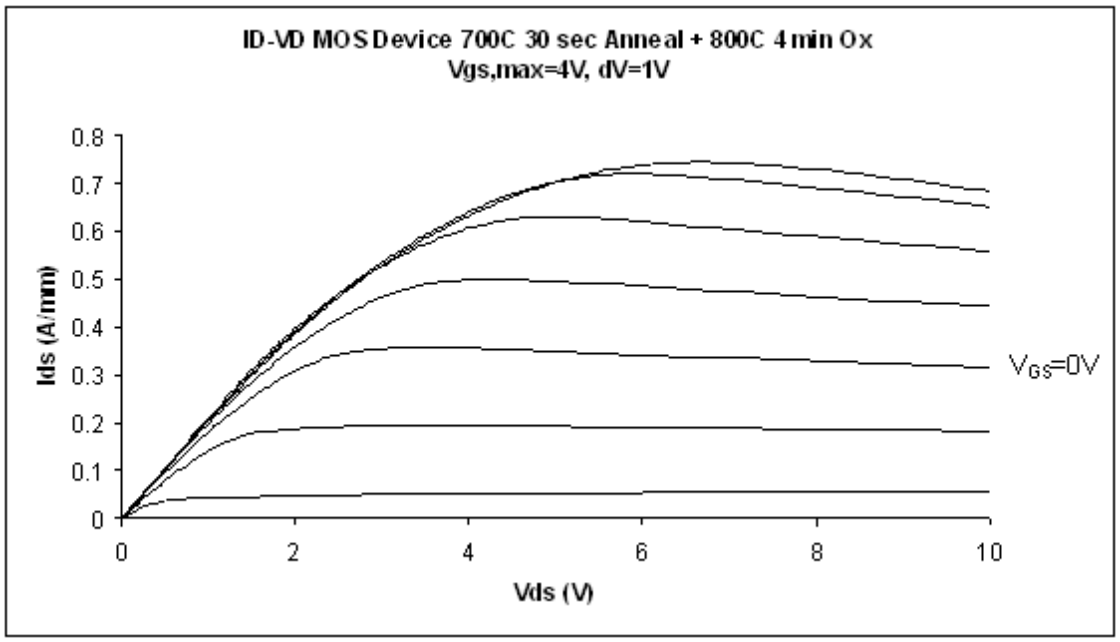


Figure 4.16: MOS-HEMT Device $I_D - V_D$ characteristics with 4 min Oxidation at 800^0C.

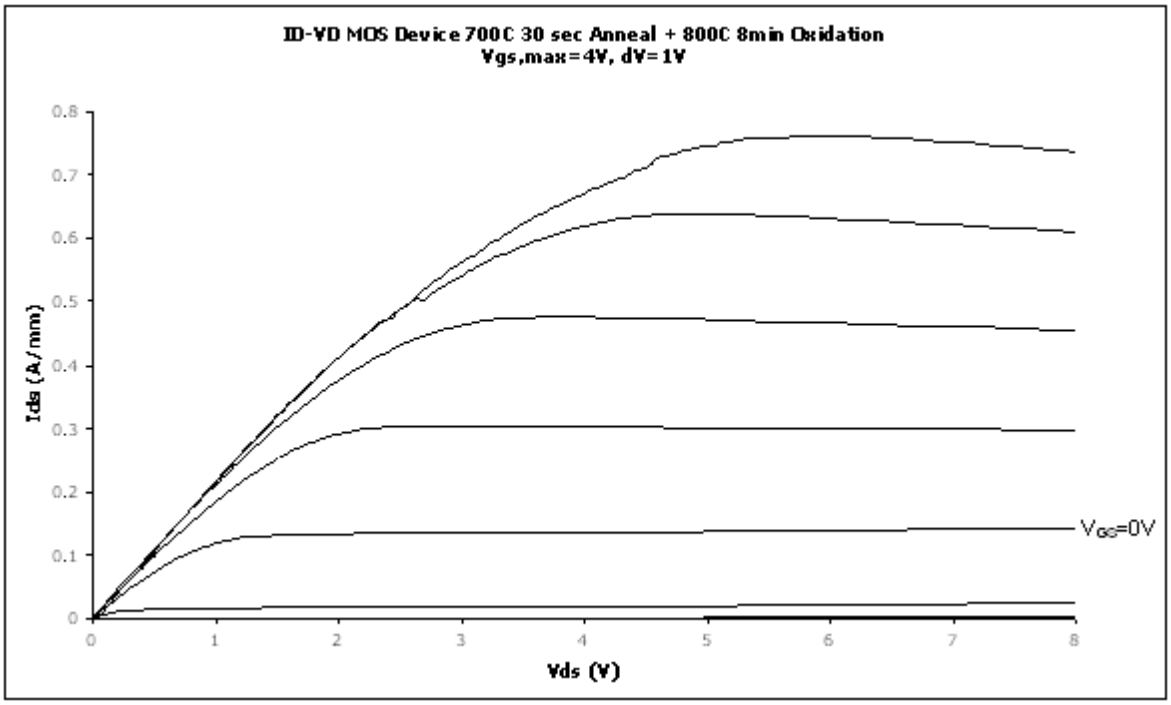


Figure 4.17: MOS-HEMT Device $I_D - V_D$ characteristics with 8 min Oxidation at 800^0C.

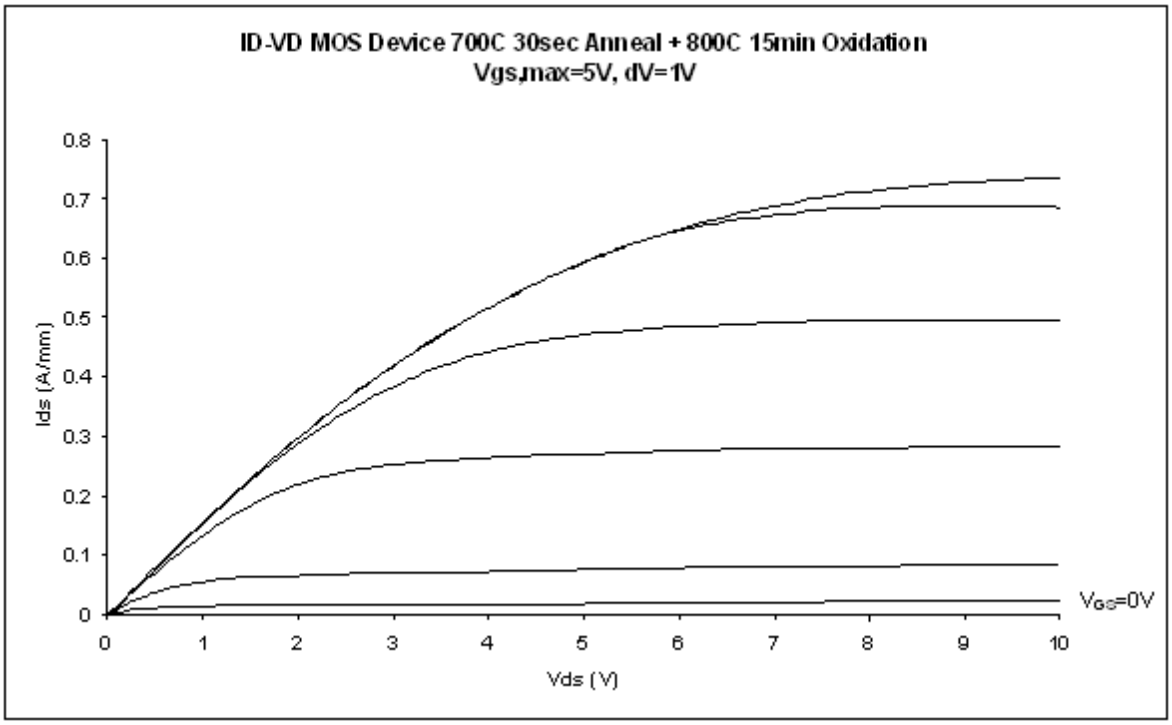


Figure 4.18: MOS-HEMT Device $I_D - V_D$ characteristics with 15 min Oxidation at 800^0C.

achieved at a much higher gate bias voltage with very low current compression. Further verification of the shift of the threshold voltage can be seen from the graph showing the comparison of the transfer characteristics ($I_D - V_G$) (measured at $V_{DS} = 8\ V$) and the transconductance (G_M) between the Schottky and the MOS-HEMT devices which are shown in Figure 4.19 and 4.20, respectively. There is a significant increase in the maximum output drain current $I_{DS,MAX}$ for MOS-HEMT devices ($\backsim$ 760 − 800 mA/mm) as compared to the Schottky device ($\backsim$ 620 mA/mm). This is probably due to the presence of a good quality dielectric under the gate-foot region which helps in reducing surface states resulting in higher output current. The results show a clear shift of the threshold voltage of the MOS-HEMT devices in the positive direction depending on the duration of oxidation without any loss of transconductance or the maximum output drain current $I_{DS,MAX}$. MOS-HEMT devices which underwent longer oxidation could be biased at gate voltages as high as $V_{GS} = 5\ V$ with little current compression as compared to the Schottky devices which suffered from full current compression at $V_{GS} = 3\ V$.

There is no noticeable threshold voltage shift between the MOS-HEMT devices oxidized for 2 min and 4 min. One probable reason for this is that in the beginning of the oxidation process the first 2 $\backsim$ 3 min the thin aluminium layer is oxidized first before the AlGaN barrier starts to oxidize. Once the aluminium is fully oxidized the latter part of the oxidation process is used solely to oxidize the barrier

Device	$\mathbf{V}_{TH}$ V	$I_{D,MAX}$ (mA/mm)	*Current Compression*	$G_{M,MAX}$ @ $V_{DS} = 8V$ (mS/mm)
Schottky	-3.1	620	Very High @ $V_{GS} = 3V$	148
4 min Ox.	-3.0	780	High @ $V_{GS} = 4V$	160
8 min Ox.	-1.6	800	Very Low @ $V_{GS} = 4V$	182
15 min Ox.	-0.5	760	High @ $V_{GS} = 5V$	160

Table 4.2: Comparison between Schottky and MOS-HEMT device parameters

layer and hence the V_{TH} shift starts depending on the rate of oxidation (effective thinning) of the barrier layer. Also, sufficient amount of the barrier needs to be thinned before a significant shift in the threshold voltage can be noticed. Hence, those devices which underwent oxidation for 2 and 4 min probably did experience some barrier thinning but not enough to shift their threshold voltage. Further extensive TEM analyses are required with very short oxidation intervals (30 sec) in order to understand the mechanism during the initial stages of the oxidation process. However, since the MOS-HEMT devices oxidized for less than 4 min didn't show any significant change in the device characteristics, hence won't be discussed in details. As explained earlier, the oxide grows thicker over the course of time meaning that the oxidant molecules take a longer time to reach the AlGaN surface. As a result of this, the rate of oxidation decreases. A comparison between the Schottky and MOS-HEMT device parameters are summarised in Table 4.2.

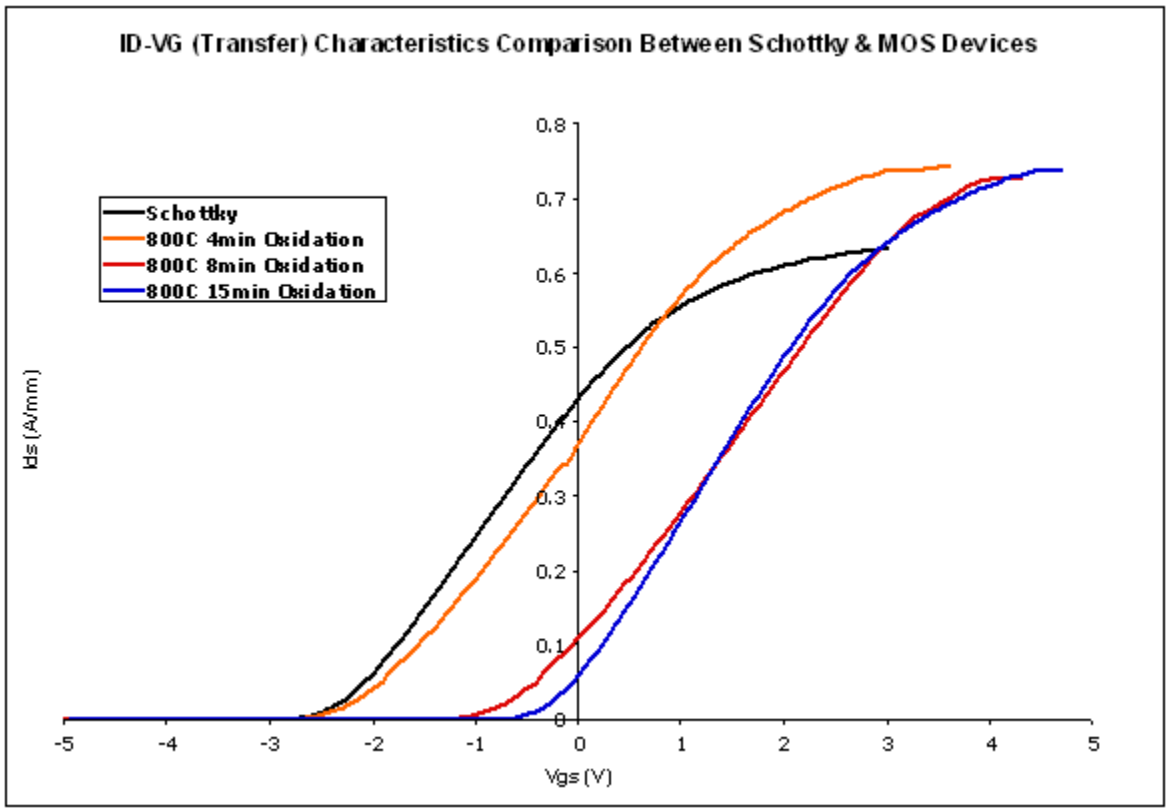


Figure 4.19: Comparison of $I_D - V_G$ (Transfer) characteristics between Schottky and MOS-HEMT devices.

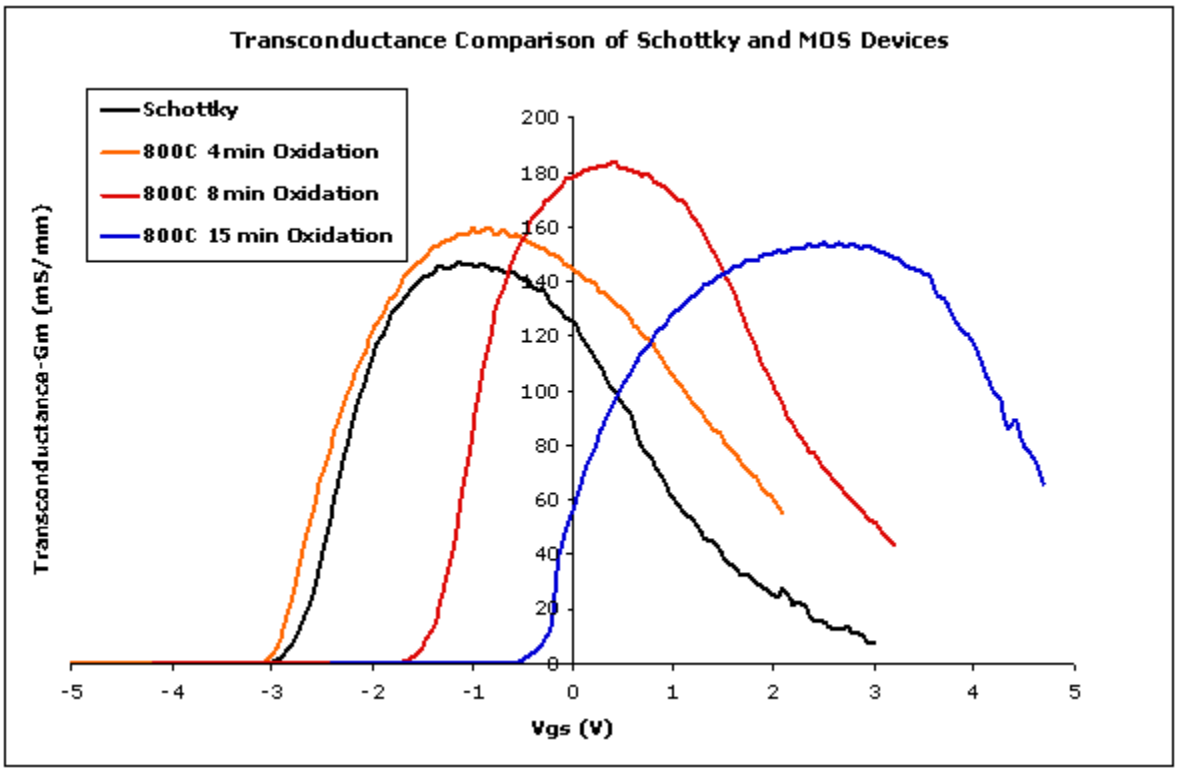


Figure 4.20: Transconductance characteristics comparison between Schottky and MOS-HEMT devices.

4.6.3.1 Discussion

The device results presented in the previous section provides the proof of concept and indicate the potential advantages of this unique gate-foot oxidation technology over conventional E-mode device fabrication techniques such as recess etching, ion implantation, etc. The output, transfer and transconductance characteristic graphs presented here are the best case results whereas the data presented in Table 4.2 presents the average case results among the group of devices measured on the same sample ($10\ mm \times 5\ mm$) which consisted of about 15-18 devices in order to prove the potential of this technology. However, it must be noted that there are significant variations in results of the devices fabricated using similar process flows from different areas of the wafer. For example, majority of devices fabricated using 4 min oxidation showed a threshold voltage of $\backsim 3\ V$ (showed in Table 4.2) whereas the best result obtained from a few devices on the same sample showed a threshold voltage of $\backsim 2.2\ V$. Similarly, the sample area used to fabricate devices with 8 min oxidation showed similar output characteristics but exhibited higher peak transconductance than any other devices fabricated using other areas of the wafer (showed in Table 4.2 and Figure 4.20). After careful analysis of the best case and the average case results (shown in Table 4.2) it can be concluded that there is $\backsim 15-20\%$ variation in the measured data. This inconsistency in device results can lead to question the reliability and reproducibility of the oxidation process, which could have been answered by repeating same pro-

cedures on larger samples from different areas of the wafer. However, due to the lack of sample availability this was not possible. One potential reason for this irregularity in device results can be the explained by the non-uniformity of the wafer. Furthermore, carefull analysis of the data sheet of the wafer supplied by NTT Corp., will reveal a few anomalies such as the average epi layer thickness is $\backsim 1.9\ \mu m$, which is expected to be over 2 μm as the buffer layer thickness specified in the data sheet was 2 μm itself. Secondly, the wafer is a capless structure and TLM measurements (unpassivated) showed very high contact and sheet resistance with large ($\geq 5\%$) variations over the whole wafer.

Anyhow, based on the achieved results it can be safely concluded that the localized gate-foot oxidation technique is one of the most effecient ways to fabricate GaN based E-mode devices. Though further extensive analysis and repeatation of same process flows are required on larger sample areas to verify repeatability and reproducibility of this process.

4.6.4 On-Resistance (R_{ON}/R_{DS}) Extraction

On Resistance (R_{ON}) or Source-Drain Resistance (R_{SD}) is the resistance between the source and drain terminal of a MOS-HEMT when it is fully turned on. The R_{ON} is extracted in the linear region of the $I_D - V_D$ characteristic at the maximum gate bias voltage ($V_{GS,MAX}$) possible with minimum drain-source bias [123]. Therefore the R_{ON} was calculated from the data of Figure 4.11 and 4.18,

which are the $I_D - V_D$ characteristics of the Schottky device and the MOS-HEMT device oxidized for 15 min, respectively, when they were fully ON. The plot of the R_{ON} ($m\Omega.mm^2$) against drain voltage (V_{DS}) is shown in Figure 4.21. The minimum specific value of R_{ON} for the MOS-HEMT device oxidized for 15 min was calculated to be 9.8 $m\Omega.mm^2$ measured at $V_{DS} = 1\ V$ and $V_{GS} = 5\ V$ for a device with $L_G = 2\ \mu m$ and $L_{SD} = 12\ \mu m$ and a die area of 0.0212 mm^2, whereas that for the Schottky device with similar device parameters was calculated to be 14.14 $m\Omega.mm^2$ measured at $V_{DS} = 1\ V$ and $V_{GS} = 3\ V$. From the extracted values it is quite clear that there is a significant improvement in the value of R_{ON} for MOS-HEMT devices as compared to its Schottky counterpart which indicates the concept of reviving the entire 2DEG current density for the MOS-HEMT devices with the application of higher gate bias voltages. Based on these extracted characteristics it can be deduced that for sub-micron gate lengths and small source-drain spacing record values of R_{ON} can be achieved.

4.6.5 OFF State Breakdown Voltage (V_{BR}) Measurement

During the OFF state the channel of the MOS-HEMT is open under the gate-foot region. Application of higher positive voltage at the drain increases the electric field around the gate region and starts to attract the electrons to complete the channel. The voltage at which the electric field is powerful enough to attract enough electrons and complete the channel allowing conduction of current is called

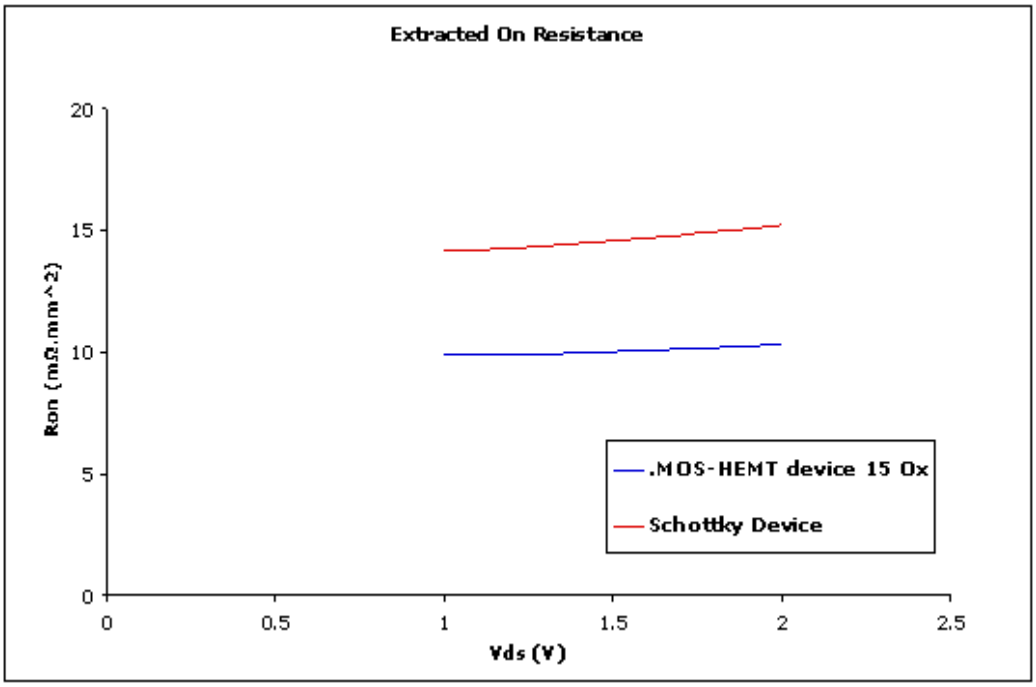


Figure 4.21: Plot showing the extraction of R_{ON} for Schottky and MOS-HEMT device oxidized for 15 min.

the breakdown voltage and depends mainly on the gate-drain distance (L_{GD}) and the thickness of the barrier epitaxial layer [124].

The breakdown voltages of the Schottky and MOS-HEMT devices were measured using Agilent's B1500A semiconductor device analyzer. The gate was biased with a voltage just below threshold for the devices to be OFF and the drain voltage was increased slowly in the forward direction to the point where it starts conducting. The Schottky device was biased at a gate voltage of -3.5 V ($V_{TH} = -3.1\ V$) and MOS-HEMT device (oxidized for 15 min) was biased at -1 V ($V_{TH} = -0.5\ V$). The drain voltage was increased from 8 V to 42 V for both the devices but no conduction was noticed. However, further increment of the drain voltage wasn't possible due to the limitation of the measurement equipment.

Normally, for AlGaN/GaN HEMTs with large gate-drain distances ($L_{GD} \geqslant 10\ \mu m$) breakdown voltages higher than 100 V are expected [125]. Since at 42 V there was no conduction in both the Schottky and MOS-HEMT devices it can be concluded that the off-state breakdown voltages of these devices are much higher than 42 V.

4.6.6 Gate Leakage (Diode Characteristics) Comparison

One of the major advantages of the oxidation procedure is that it creates a very high quality crystalline oxide, which works as an excellent dielectric and hence helps to reduce the gate leakage current significantly at very negative bias voltages

as high as -20V. The $I_G - V_G$ characteristics of the Schottky and the MOS-HEMT devices are shown in Figure 4.22. The maximum leakage at $V_G = -20\ V$ for the MOS device oxidized for 15 min at 800^0C was found to be about 18 nA/mm, which is a significant improvement over the Schottky device which exhibits a gate leakage of 0.56 $\mu A/mm$. The oxidation process improves the gate leakage current of the MOS-HEMT devices by three orders of magnitude over the Schottky device. Oxidation at high temperatures helps the formation of a mixture of high quality aluminium and gallium oxide (Al_2O_3 and Ga_2O_3) dielectric which prevents tunnelling of the electrons to the gate contact through the AlGaN barrier and the oxide layer.

4.6.7 Capacitance-Voltage (C-V) Measurements

Capacitance-Voltage (C-V) measurements play a significant role in analysing the electrical properties of the gate dielectric, such as charge trapping, dielectric constant, etc. Good quality gate dielectric facilitates in enhancing the breakdown voltage and device's frequency of operation by reducing charge trapping effects [126],[127]. Reduction of traps is responsible for the carrier velocity enhancement in the channel of the MOS-HEMT thus improving the output drain current characteristics. Futhermore, parasitic charges gives rise to very high gate capacitances, C_{gs} (gate-source capacitance) and C_{gd} (gate-drain capacitance) which directly influences the device's frequency of operation and is given by the formula in Eq.4.1

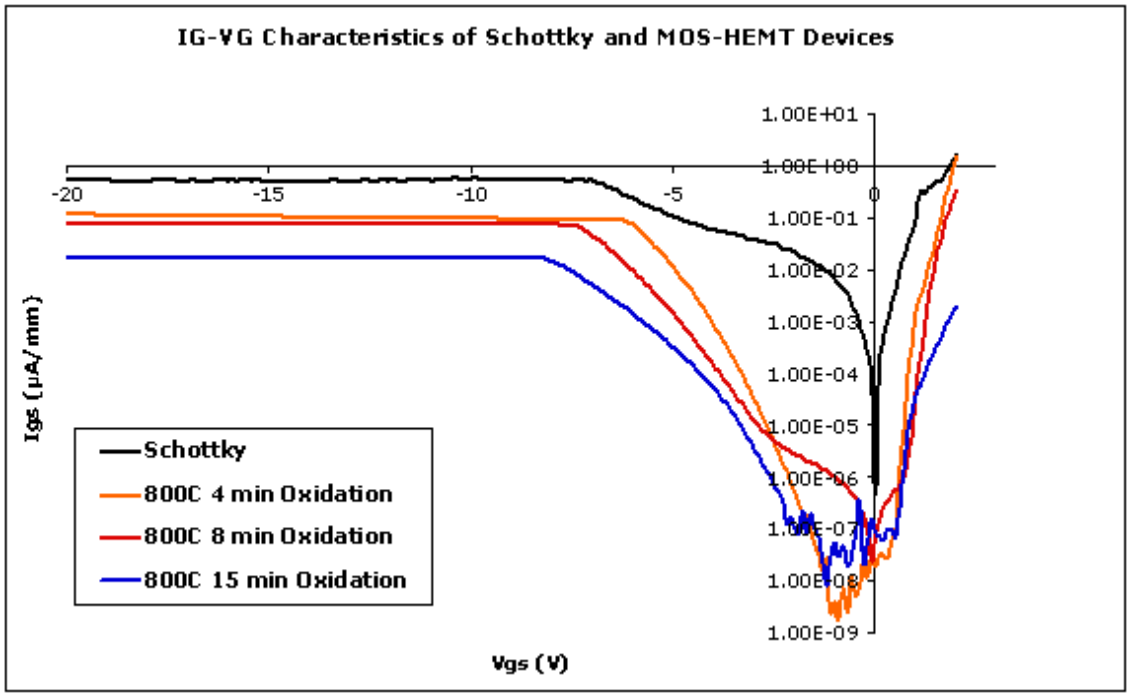


Figure 4.22: Comparison of gate leakage curent (logarithmic scale) for Schottky and MOS-HEMT devices.

[127]. Charge trapping depends on the quality and thickness of the dielectric used [126]. The most common dielectrics used for MOS-HEMT or MOSFET fabrication are silicon dioxide (SiO_2), silicon nitride (SiN), Al_2O_3, etc. Low quality dielectrics like amorphous Al_2O_3, poor quality SiN, etc., contains substantial amount of parasitic charges. The trapped charges are responsible for reduction of carrier velocity underneath the gate region thus degrading device performance [127]. The work described in this thesis mainly involves the use of a thermally grown dielectric which consists of an oxide mixture containing Al_2O_3 and Ga_2O_3.

$$f_T = \frac{g_m}{2\pi(C_{gs}^2 + C_{gs}C_{gd})^{1/2}} \tag{4.1}$$

Capacitance-Voltage measurements were performed on circular MOS-HEMT test structures of 100 μm diameter, fabricated using the MOS-HEMT device process flow in order to evaluate the quality of the oxide of $Al_2O_3/AlGaN/GaN$ hetero-structure. The SEM image of the circular test structure is shown in Figure 4.23. The contact on the oxide area was fabricated using a wider field plate on top of the oxide region using conventional lithography and lift-off. The ohmic region surrounding it provides the ground contact for characterization.

The room temperature C-V characteristics of the MOS-HEMT structures were measured using B1500A SPA at 1MHz at a gate bias voltage range of -5 V to 0.5 V. The test structure was oxidized for 15 min at 800^0C in an RTA. The C-V characteristics of the circular test structure are shown in Figure 4.24. Initial

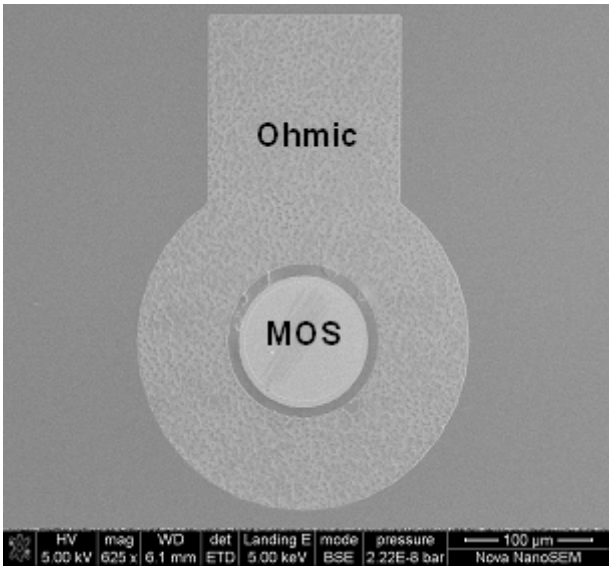


Figure 4.23: Circular MOS-HEMT test structure for C-V characterization.

measurement showed deep depletion behaviour for reverse gate bias voltage and the overlapping of forward and reverse traces depicts the absence of any kind of hysteresis and charge trappings, hence attesting to the good quality and crystallinity of the oxide. However, it must be noted these characterizations are just preliminary results and further extensive C-V analysis of the oxide like different frequency sweeps, different temperature measurements other than room temperature, etc are required for proper characterization to integrate this technology in high frequency devices.

4.6.8 Characterization of Ohmic Contacts

Optimization of ohmics contacts were carried out by another member of the research group for similar AlGaN/GaN HEMT layer structures and based on

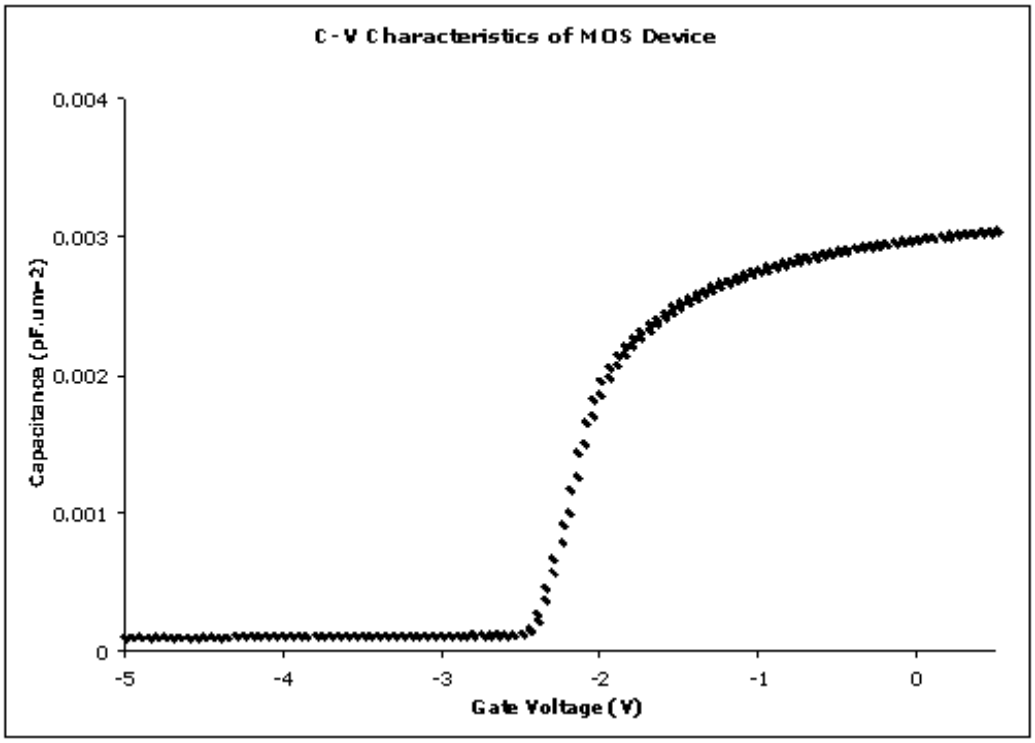


Figure 4.24: C-V characteristics of $Al_2O_3/AlGaN/GaN$ circular test MOS-HEMT structure (diameter $100\mu m$).

the achieved results similar metal stack and annealing parameters were used to fabricate ohmic contacts for this project [128]. Transmission line method (TLM) measurements were carried on several areas of the wafer to check the uniformity of growth and as well as for the comparison between unpassivated Schottky and passivated Schottky and MOS-HEMT devices. The structure of the TLM pattern consists of 100 $\mu m \times 100$ μm pads with a spacing of 5 μm, 7 μm, 9 μm and 11 μm between them. The metal stack consisted of Titanium (30 nm) / Aluminium (180 nm) / Nickel (40 nm) / Gold (100 nm) annealed at 800^0C in N_2 environment for 30 sec. The extraction of resistance figures from the TLM graphs were done using the least squares method as described in Chapter 2, Section 2.8.1 including their standard estimate errors. The unpassivated device showed a very high contact and sheet resistance of 0.85 ± 0.21 $\Omega.mm$ and 454.27 ± 127 Ω/sq shown in Figure 4.25. These extracted values are quite similar to the data obtained from the material's datasheet, reproduced in Appendix B.

In order to improve the contact and sheet resistance the samples (Schottky and MOS-HEMT) were passivated with 150 nm Inductive Coupled Plasma silicon nitride (ICP-SiN). The samples were processed with the same process as for MOS-HEMT devices described in Sec. 4.6.3. As shown in Figure 4.26 the contact and sheet resistance of the passivated devices were extracted to be 0.44 ± 0.27 $\Omega.mm$ and 258.82 ± 93 Ω/sq, respectively. The passivation seems to enhance the 2DEG sheet density and thereby reducing the R_C and R_{SH}.

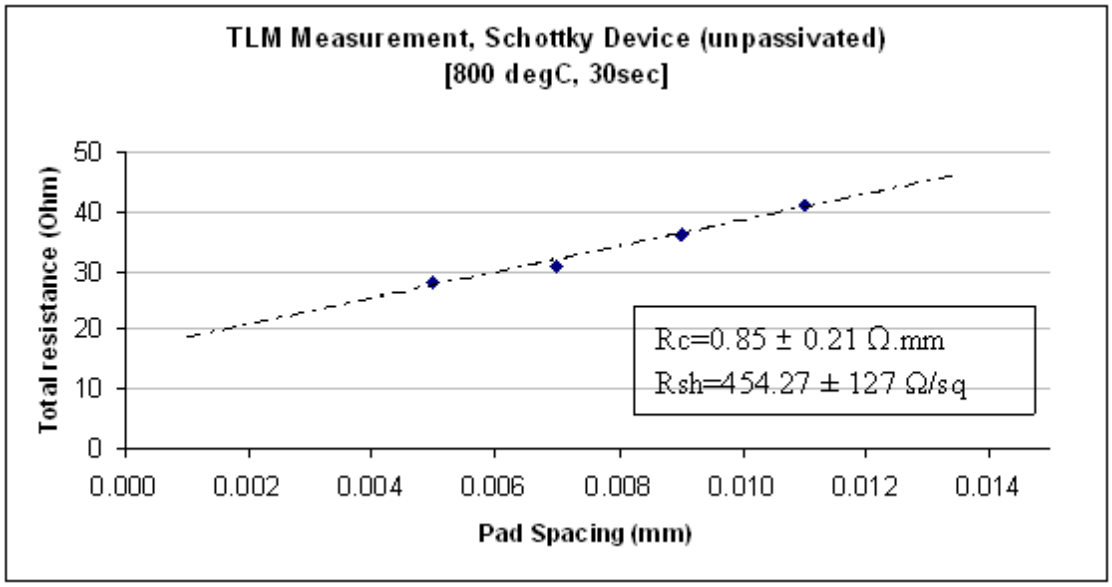


Figure 4.25: TLM measurement graph of an unpassivated Schottky device.

TLM measurements of passivated Schottky and MOS-HEMT devices showed more or less the same values for R_C and R_{SH} with $\backsim$ 5% variation, which can be accounted for by growth non-uniformity. This also proves that the 150 nm thick ICP SiN has a very high thermal stability and is capable of protecting the passivated areas during the gate-foot high temperature oxidation process. The comparison of R_C and R_{SH} for unpassivated Schottky and passivated Schottky and MOS-HEMT devices are shown in Table 4.3.

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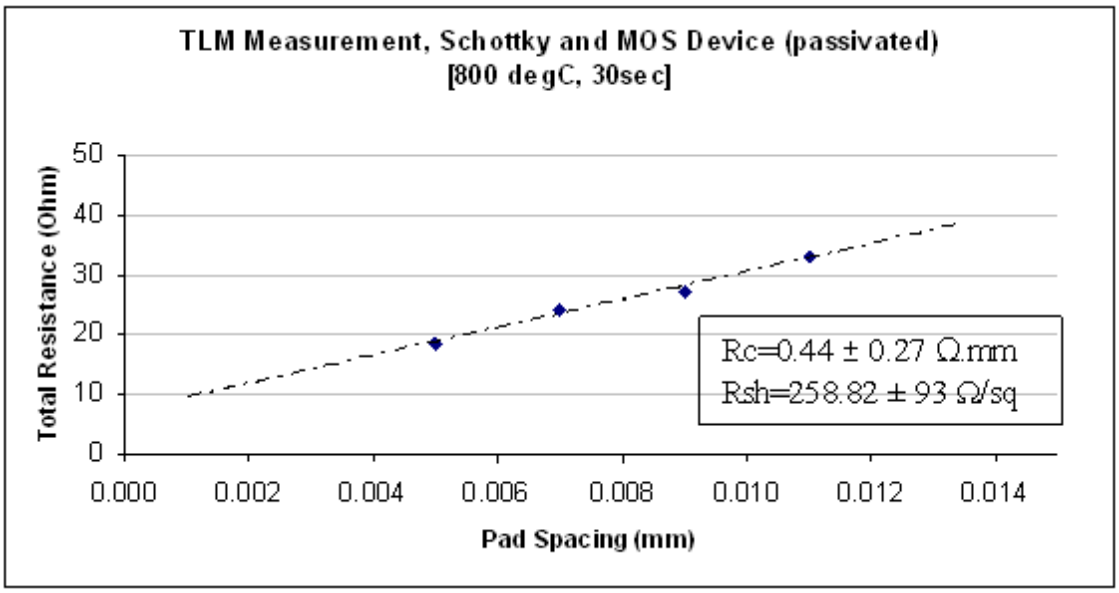

Figure 4.26: TLM measurement graph of the passivated Schottky and MOS devices.

Device	$\mathbf{R_C}(\Omega.mm)$	$\mathbf{R_{SH}}(\Omega/sq)$
Schottky (unpassivated)	0.85 ± 0.21	454.27 ± 127
Schottky and MOS-HEMT (passivated)	0.44 ± 0.27	258.82 ± 93

Table 4.3: Comparison of contact and sheet resistances for unpassivated and passivated devices

4.7 Conclusion

A simple and novel method for fabricating enhancement mode MOS-HEMTs using standard AlGaN/GaN HEMT structures using localized gate-foot thermal oxidation has been described in this Chapter. The thermal oxidation of the gate-foot region in dry oxygen seem to effectively and uniformly thin the barrier layer. The key to this process is the thin Al layer evaporated on the epitaxial layer structure. Annealing of this thin layer of evaporated Al helps in uniform integration of the metal with the top layer of the AlGaN barrier. Further oxidation of the barrier layer leads to the formation of an uniform oxide layer, which has already been proved by TEM analysis. DC measurements revealed a maximum drain current ($I_{D,MAX}$) equal to $\backsim$ 800 mA/mm in all the MOS-HEMT devices with gate length of 2 μm and gate width of 100 μm with a peak transconductance of $\backsim$ 160 mS/mm and an off-state breakdown voltage of over 42 V. The transfer characteristics showed a shift of threshold from -3.1 V for Schottky devices to -0.5 V for MOS-HEMT devices, which underwent 15 min of oxidation in a RTA at 800^0C. A major advantage of this unique way of E-mode device fabrication is that all the MOS-HEMT devices exhibited more or less the same maximum drain current. This proves that there is no loss of the current density in the channel even after the thermal oxidation process and that the entire 2DEG density can be revived by the application of high gate bias voltages (even as high as 5 V).

The thermal oxidation improved the gate leakage current of the MOS-HEMT

device oxidized for 15 min by a three orders of magnitude over the Schottky device (0.56 $\mu A/mm$) exhibiting a very low leakage current of 18 nA/mm for a negative gate bias of -20 V. Furthermore, the formed oxide also improved the metal-oxide-semiconductor contact allowing better gate control and higher output drain current. The measured specific R_{ON} for the MOS-HEMT device oxidized for 15 min was found to be 9.8 $m\Omega.mm^2$ for a very large source-drain spacing of 12 μm, which can be considered quite low for such large active regions. TLM measurements revealed a contact and sheet resistance of $R_C =\backsim 0.44\ \Omega.mm$ and $R_{sh} =\backsim 258.82\ \Omega/sq$, respectively. Capacitance-Voltage (C-V) characteristics of the $Al_2O_3/AlGaN/GaN$ circular test MOS-HEMT structures were measured and observed. Preliminary results showed no hysteresis and deep depletion behaviour under reverse bias conditions, indicating the good quality of the thermally grown oxide. However, further detailed analysis is required for proper integration of this oxide mixture for switching and RF applications.

CHAPTER 5

ALN/ALGAN/GAN DOUBLE BARRIER HIGH ELECTRON MOBILITY TRANSISTOR

Standard AlGaN/GaN structures with 20 nm barrier layer are normally D-mode devices and it reqiures complex processing steps to effectively thin the barrier in order to make them operate as E-mode devices. In order to achieve "normally-off" operation the barrier needs to be either physically (recess etching) or effectively (e.g. converted to an oxide as described in Chapter 4) thinned till the thickness reaches the critical barrier thickness (t_{CR}) for that specific Al content below which no 2DEG is formed as described in Chapter 3. However, for conventional $Al_{0.20}Ga_{0.80}N/GaN$ ($x = 20\%$) the t_{CR} is $\backsim 5\ nm$ (simulation results shown in Section 5.2 of this Chapter) which implies that about 15 nm of the barrier needs to be thinned. Controlling the physical etch process using Cl_2 based gases in order to stop precisely at 5 nm is an issue and hence reproducibility and repeatability of the process as well. The localized gate-foot oxidation technology described in Chapter 4 can be implied for the thinning purposes but conversion of 15 nm barrier into oxide in order to achieve a positive threshold voltage requires a long time thermal treatment of the wafer at high temperatures (800^0C). One major disad-

vantage of this technique is that such long time thermal treatment can generate stress related problems within the wafer and specially when Si is used as a substrate. Currently, Si is an attractive option as a substrate since its cheaper than sapphire or SiC and it facilitates circuit integration of GaN (GaN grown on Si) technology with the existing ones. Since, the thermal stability of Si is much lower than sapphire or SiC the localized gate-foot oxidation described in this thesis can have damaging effects to the devices fabricated using GaN epi-layers grown on Si wafers.

Hence, after careful analysis of the pros and cons of the current E-mode device fabrication technologies including the gate-foot oxidation technology described in this thesis, an alternative concept of E-mode device technology involving two active barrier layers was developed which is discussed in the subsequent sections.

5.1 Concept of Double Barrier HEMT

Conventional $Al_{0.20}Ga_{0.80}N$/GaN HEMT structures have good 2DEG concentrations ($\backsim$ 1×10^{13} cm^{-2}) with excellent room temperature mobility ($\backsim$ 1700 cm^2/V.s). The contact resistance of AlGaN/GaN devices has been optimized by many groups in the last decade and hence a value for R_C lower than that of AlN/GaN devices is achievable. Due to the thick AlGaN barrier ($\backsim$ 20 nm) surface passivation is not required. E-mode device fabrication on standard AlGaN/GaN structures have been demonstrated using recess etching, ion implantation, etc, as

described in Chapter 3, which are neither reliable nor reproducible. Recess etching and ion implantation are the most common technique to fabricate E-mode devices on AlGaN/GaN structures and since both the processes involves the sample to be exposed to plasma, so plasma-induced damages are a major concern [129]. Moreover, reproducibility is a major issue with these processes and hence the fabricated devices suffer from varying threshold voltage problems.

The recently introduced AlN/GaN HEMTs (AlN barrier thickness $\backsim$ 3 nm) have high 2DEG carrier concentration ($\backsim$ 2×10^{13} cm^{-2}) with excellent room temperature mobility ($\backsim$ 1500 $cm^2/V.s$). In addition to higher polarization fields, one of the main reasons for both very high 2DEG density and high mobility is the reduction in alloy disorder and roughness scattering by removing gallium (Ga) from the barrier and forming ultra-abrupt AlN/GaN interfaces [130]. AlN/GaN devices suffer from very high contact resistance ($\backsim$ 1 $\Omega.mm$) and passivation problems [55].

In this chapter the concept of a new double barrier AlN/AlGaN/GaN HEMT structure will be discussed. This structure is capable of combining the advantages of both single barrier structures and it can enable simple processing of E-mode devices. The device and fabrication concept is shown in Figure 5.1. It consists of a very thin AlGaN layer capped with an AlN layer. The incorporated thin AlGaN layer is only used to control the threshold voltage of the device and hence the thickness is kept around the critical thickness of the layer for the specific

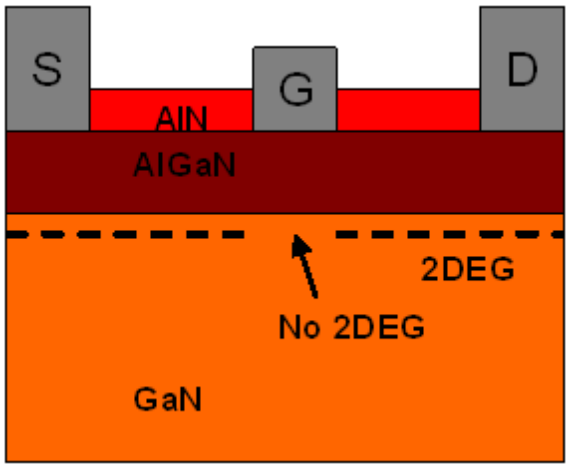

Figure 5.1: Device and fabrication concept of the new AlN/AlGaN/GaN HEMT structure.

Al-content. Therefore the threshold voltage is set by epitaxy. However, the polarization charge induced by the thin AlGaN layer is not sufficient to generate high carrier concentration in the channel. Adding an AlN cap on top of the AlGaN layer induces a large polarization field because of the inherent spontaneous polarization as a result of lattice mismatch and larger conduction band offset thereby enhancing the carrier concentration in the channel. Also, the AlN acts as a very high bandgap insulator layer and helps in reducing the number of surface states, leading to high carrier concentration in the channel [131]. The 2DEG concentration can be controlled by the thickness of the two barriers and the Al-content of the AlGaN barrier layer. In terms of device processing, the AlN layer can also be selectively etched over AlGaN using AZ400K solution and hence the recessed gate would sit on the AlGaN layer enabling E-mode operation as described in Chap-

ter 3 [77]. This approach allows for precise repeatable control of the threshold voltage with no etch or plasma induced damages. Moreover, this technique also provides the possibility of developing very low recessed ohmic contacts in which the metallization can be deposited directly on the AlGaN layer after etching away the AlN.

5.2 Simulation of the Double Barrier HEMT Structure

In order to calculate the critical barrier thickness (t_{CR}) for the AlGaN barrier ($x = 20\%$), a simulation was carried out using the 1D Schrödinger-Poisson equation solver of NEXTNANO III-V 3D Nano-device Simulator Tool [132]. Nextnano is a device simulator tool for simulating quantum dots, quantum wires, RTDs, MOSFETs, HEMTs, etc. for group IV (Si, Ge, SiGe), all III-V and II-VI materials. The simulations were carried out by varying the epi layer thicknesses of the barriers and buffer layers for specific Al-contents.

Figure 5.2 shows the variation of the simulated 2DEG density for different AlGaN barrier thickness. If the AlGaN barrier layer thickness falls below 6 nm, no 2DEG is generated because the polarization effects are not sufficient enough to generate the electron concentration in the channel. Therefore the thickness of the $Al_{0.20}Ga_{0.80}N$ layer needs to be under 6 nm if no 2DEG is to be created underneath the gate-foot.

Simulations for the new AlN/AlGaN/GaN device structure were then carried

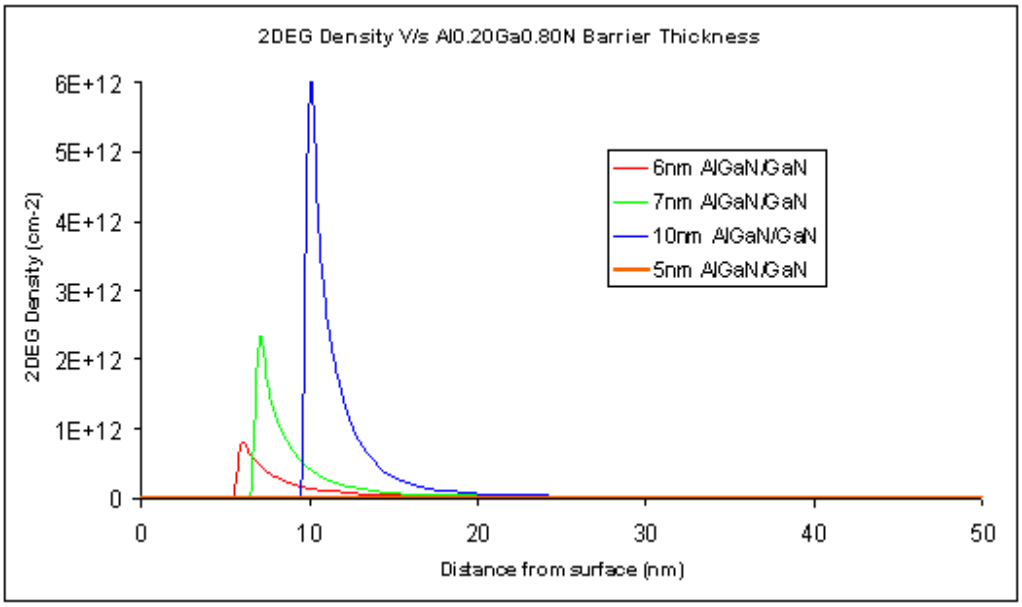

Figure 5.2: Calculation of critical barrier thickness of $Al_{0.20}Ga_{0.80}N$ barrier.

out to design the new composite barrier layer consisting of two active barriers, AlN (top active layer) and conventional $Al_{0.20}Ga_{0.80}N$ (second active layer) followed by a 3 μm GaN buffer layer. The variation of the 2DEG density with the change of the $Al_{0.20}Ga_{0.80}N$ barrier thickness is shown in Figure 5.3. These results show that the composite barrier can yield high 2DEG density. Also, the 2DEG density of 2 nm AlN/6 nm $Al_{0.20}Ga_{0.80}N$/GaN ($\backsim 2.35 \times 10^{13}\ cm^{-2}$) is higher than a 1 nm GaN cap/3 nm AlN/GaN ($\backsim 2.2 \times 10^{13}\ cm^{-2}$) and nearly double than a standard 20 nm $Al_{0.20}Ga_{0.80}N$/GaN structure ($\backsim 1.2 \times 10^{13}\ cm^{-2}$). The plot also includes the results of a standard 20 nm $Al_{0.20}Ga_{0.80}N$ /GaN and 1 nm GaN cap/3 nm AlN/GaN in order to compare the simulation results.

Increasing the thickness of the AlN layer or decreasing the AlGaN layer in

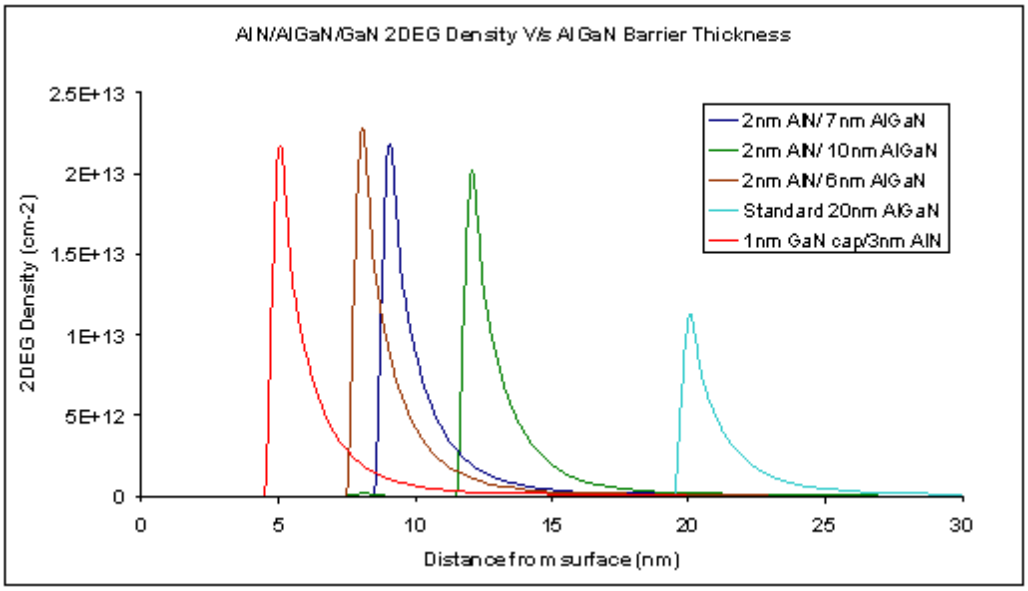

Figure 5.3: Variation of the 2DEG density with the AlGaN barrier thickness.

the composite layer structure will result in an even higher 2DEG concentration but this will also result in a decrease in mobility due to presence of excessive carriers in the channel resulting in poor device performance [133]. Hence, in order to maintain parity between the carrier concentration, high mobility and E-mode operation the $Al_{0.20}Ga_{0.80}N$ and the AlN layer thickness should be set at 6 nm and 2 nm, respectively. Also when grown with a high temperature in-situ SiN cap layer the latter can act as a high quality passivation layer and also as a hard mask for wet etching of AlN. Variation of the 2DEG density with the AlGaN barrier thickness. The final device structure is shown in Figure 5.4. The main reason responsible for such high density of carrier confinement in the channel is the large conduction band bandgap offset between the AlN, AlGaN and GaN. AlN has a

very high bandgap ($\backsim$ 6.2 eV) and it sits on 6 nm $Al_{0.20}Ga_{0.80}N$ (bandgap $\backsim$ 4 eV), which is grown on thick GaN (bandgap $\backsim$ 3.44 eV) and hence the quantum well formed at the hetero-junction due to the large band offsets is quite deep. This facilitates in the formation of such high 2DEG density and probably much higher output drain current than conventional AlGaN/GaN or even AlN/GaN hetero-structures.

A comparison of the band profiles of the different double barrier HEMTs presented in this chapter is not shown since the main aim of this device simulation is not the carrier density but to develop the concept of a high performance device structure which can provide E-mode operation by the combination of two active barriers in such a way that the thickness of the second active layer ($Al_{0.20}Ga_{0.80}N$) is kept as close to its critical thickness as possible. Based on the device fabrication concept when the first active layer (AlN) is selectively etched or effectively thinned a normal Schottky contact should be capable of depleting the electrons in the channel achieving normally-off operation.

5.3 Discussion

The concept of a new AlN/AlGaN/GaN D-HEMT structure described in this chapter is potentially capable of providing E-mode operation with a very high output current and can be fabricated using simple steps. Since selective etching of AlN is possible and the AlGaN barrier layer is kept just above the critical

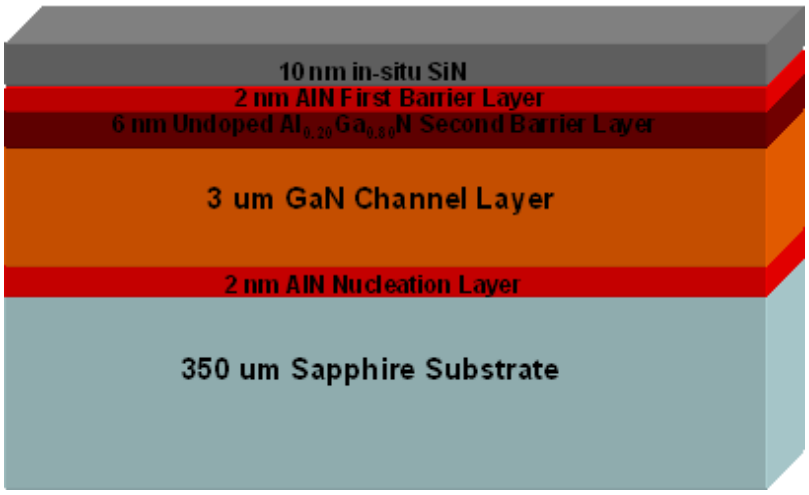

Figure 5.4: Device Structure of 2nm AlN/6 nm $Al_{0.20}Ga_{0.80}N$/GaN.

thickness, a normal Schottky contact on the AlGaN layer (after etching the AlN layer) might be enough to deplete the channel underneath the gate region and help achieve normally-off operation. Moreover, the gate-foot thermal oxidation can still be employed after the selective etching step in order to form a good quality dielectric. Furthermore, the localized gate-foot oxidation technology can also be implemented directly to this layer structure instead of selective etching of AlN since the barrier that needs to be thinned is only $\backsim$ 2-3 nm (2 nm AlN and 1 nm AlGaN layer) and hence a short oxidation time can effectively convert the barrier into oxide. The issue of thermal stress generated from longer oxidation times for standard 20 nm AlGaN/GaN structures can be easily erradicated. However, the oxidation only process needs to be carefully optimized for a positive threshold voltage.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

This thesis explored a simple and novel method for realizing enhancement mode AlGaN/GaN MOS-HEMTs by using localized thermal oxidation of the AlGaN barrier under the gate-foot. The proposed technology may be a better alternative to current E-mode fabrication technologies like recess etching, ion implantation, etc. in terms of reproducibility and reliability. The selective gate-foot oxidation process with the protective cap of thin aluminium layer is capable of thinning the barrier uniformly. Moreover, initial investigations (device characteristics and C-V measurements) of the formed oxide mixture of Al_2O_3 and Ga_2O_3 reveal promising results of a high quality dielectric, which may be capable of enhancing device performance. The oxide mixture thermally grown at high temperatures ($\backsim 800^0$C) is of much better quality [108] than oxides deposited by atomic layer deposition (ALD) at lower temperatures ($\backsim 300^0$C) as the latter can cause charge trapping problems leading to poor device performance [134]. In addition, the oxide layer significantly reduces gate leakage current.

The work presented in the thesis is a preliminary study into the proof of con-

cept of E-mode device fabrication using the localized gate-foot oxidation process. DC measurements indicate that local gate-foot oxidation is a feasible method for achieving high performance normally-off devices. The results demonstrate that there is no loss of current density of the 2DEG even after the oxidation process. However, it must be noted that even though most of the devices in the same area of the sample show similar characteristics but there are significant variations in the obtained results for similar process flow from different areas of the sample which can lead to questioning the reproducibility of the process. One potential cause for such variations can be explained as growth error, because the sample datasheet obtained from NTT, Corp., showed very high sheet resistance and significant variations in the total epi-layer thickness in certain areas of the sample. Therefore, further anaysis with different layer structures obtained from several growers are required for a detailed analysis to test the reproducibility and repeatability of the process. Initial Capacitance-Voltage (C-V) characteristics of the $Al_2O_3/AlGaN/GaN$ MOS-HEMT structures showed no hysteresis and deep depletion behaviour for reverse bias conditions, indicating the good quality of the thermally grown oxide. However, further extensive C-V analysis is required for a detailed overview of the oxide quality and for its possible integration in switching and high frequency applications. Therefore, further development of the fabrication procedure may lead to much higher output current and record low On-resistance as compared to other GaN based E-Mode devices or conventional

Si-based MOSFETs. Since both E-Mode and D-Mode AlGaN/GaN-based devices can be fabricated on the same wafer, a technology for realization of GaN-based logic circuits is potentially available.

Apart from the gate-foot oxidation technology, a new concept structure of AlN/AlGaN/GaN has also been discussed. Initial simulation results show a very high carrier confinement in the channel due to large conduction band offset between AlN, AlGaN and GaN. Also, the device can provide E-mode operation using selective etching of the first active layer (AlN) and deposition of a normal Schottky contact on the second active layer (AlGaN) as the latter is kept at just above its critical thickness. Since this is just a concept structure, actual fabrication is needed to prove the true potential of this unique device structure.

6.2 Future Work

Experimental results based on output, transfer and transconductance characteristics prove the concept of enhancement mode operation is possible. Further work on process optimization to reach positive threshold voltages, device characterization and modelling, reliability tests and circuit integration needs to be done. Following is a list of suggestions for future work:

1. Longer oxidation of the gate-foot region in order to achieve normally-off operation and have a positive threshold voltage of the MOS devices.

2. Detailed analysis of the oxide growth (oxide characteristics like ratio of Al_2O_3

to Ga_2O_3 in the oxide mixture, crystallinity of the oxide, etc) and rate of oxidation using step-by-step TEM analysis for regular oxidation time intervals.

3. Extensive C-V analysis at different sweeping frequencies needs to be done to verify the electrical characteristics of the thermally grown oxide and to determine possible methods to integrate the oxidation technology for RF devices with sub micron gate lengths.

4. Fabricate devices with sub-micron gate lengths and shorter source-drain spacing with improved ohmic contacts in order to improve the On-resistance and better DC and RF characteristics for high power switching applications.

5. Process development of the fabricated devices using different Schottky gate metals with different workfunctions to enhance barrier height and to maximize device performance.

6. Conduct high temperature DC measurement and RF measurements for both D-mode and E-mode devices to test their limit for high temperature sensing or digital applications.

7. Extensive reliability measurements including thermal, DC and RF stress need to be carried out to for improvement of device processing and to close the gap between laboratory experiments and commercial applications.

8. Fabrication of E-Mode devices with different barrier layers like AlN, InAlN, etc., using the gate-foot oxidation technology in order to prove the universal application of this process for most GaN based semiconductor devices..

9. Device characterization and extraction of equivalent circuit model parameters of both E-mode and D-mode devices for circuit simulation.

10. Device fabrication and characterization of the new AlN/AlGaN/GaN Double Barrier HEMT structure.

APPENDICES

A. Equipment and Process Information

Reactive Ion Etching

Reactive ion etching (RIE) is a kinetically-assisted plasma etching which involves sample bombardment by chemically-reactant ions accelarated across the plasma sheath. In the RIE reactors the sample is usually placed on the anode and the chamber acts as the cathode. The area of the anode region is much larger as compared to its cathode implying a large voltage drop across the plasma sheath which in turn increases the ion energy on the sample resulting in an anisotropic etch. Also RIE uses low pressure than plasma etching which increases the mean free path of the reactants between the plasma and the sample reducing the scattering within the reactant gas and increasing the directionality [135]. Furthermore, the usage of low pressure results in slow, controlled and less damage etching process. An overview of the RIE process is shown in Figure A.1.

In this project the RIE processes used to etch the inductive coupled plasma deposited (ICP-Dep) silicon nitride were carried out in an Oxford Instruments

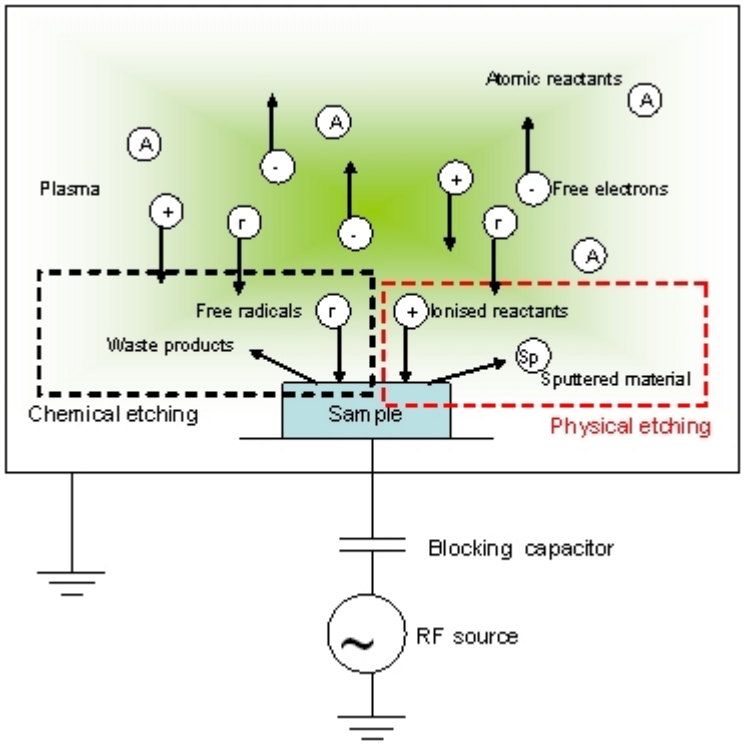

Figure A.1: Overview of reactive ion etching technique.

Plasmalab Systems-100 machine using a sulphur hexaflouride plasma with nitrogen as the carrier gas.

Inductive Coupled Plasma Silicon Nitride Deposition

Inductive coupled plasma deposition (ICP-Dep) follows the same configuration as RIE process chambers by providing gaseous reactants and exposing the mixture to an energetic plasma whose bi-products can be deposited on a sample surface in a controlled manner. For the depostion of ICP silicon nitride (SiN), silane (SiH_4) provides the silicon and the gaseous nitrigen provides the nitrogen as shown in equation (A.1)[136].

$$3\,\mathrm{Si}\,H_4 + 2N_2 \rightarrow \mathrm{Si}_3\,N_4 + 6H_2 \uparrow \tag{A.1}$$

Generally, the remote high density nitrogen plasma in the upper region of the chamber which then reacts with the silane source to form high densities of both species which can be deposited on the sample surface with much lower bias power. The high density plasma benefits the overal process in two ways. Firstly, it requires reduced operating temperature (room temperature deposition) thus protecting the samples and metal contacts (Schottky) from thermal damage. Secondly, as the plasma is of very high density, relative concentrations of reactive elements are higher than the residual or secondary contributions, resulting in a high quality and pure film. In this project the passivation layer was deposited using room temperature ICP-Dep SiN in an Oxford Instruments Plasmalab Systems-100

machine.

Lithography

Lithography is the process used to pattern a surface (usually a semiconductor) using a masking layer and is the backbone of modern semiconductor fabrication. Lithography can be subdivided into soft lithography such as stamping or printing using transfer stamps or imprint lithography. Current lithography techniques use a radiation-sensitive polymer known as resist, which is uniformly coated on the surface of the semiconductor. On exposure to radiation the chemistry of the resist changes, becoming either more or less soluble in a developer solution.

Resists are of two types, positive and negative resists. In case of positive resists exposure to UV-light causes a depolymerization by chain scission. If the exposure time is long enough the polymer film breaks down completely in the exposed areas. A suitable developer can dissolve the depolymerised regions. Hence in positive resists the exposed regions dissolve after exposure and development as shown in Figure A.2a.

On the other hand, in negative resists the unexposed area dissolves in a developer solution. Exposure of negative resists causes a radical cross-linking of the polymer chains, increasing their density and length. Hence when developed the exposed regions remain, as they are relatively insoluble and remains unaffected whilst the unexposed regions are removed. The realizable resolution of a litho-

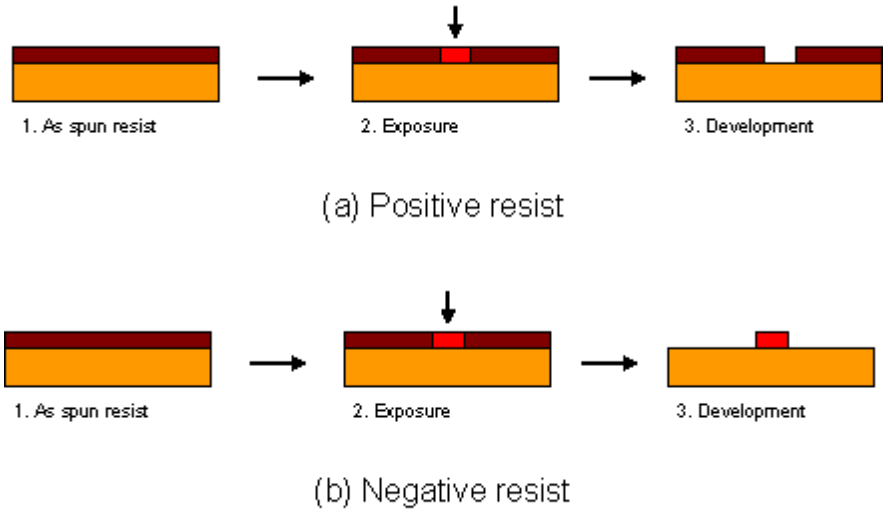

Figure A.2: Positive and negative resist development.

graphic process is defined by two main factors, such as the type of exposure and the chemistry of the resist as shown in Figure A.2b.

Optical lithography

Optical lithography provides low cost processing high through-put and relatively low running costs and hence are widely used for semiconductor processing in industries. Basic photolithography uses a mask, which is held in contact with the sample. The sample is generally processed under vacuum to ensure an uniform contact with the mask allowing coherent UV-light exposure. The achievable resolution for photolithography mainly depends on the wavelength of the UV-light, λ, and the distance of separation between the mask and the sample, s, and is given by equation (A.2).

$$l = \sqrt{\lambda s} \tag{A.2}$$

In combination of the resist thickness and deep UV-light exposure ($\lambda = 193$ nm), contact lithography can theoretically achieve a resolution of around 300 nm. However in most laboratories a cheaper 365 nm UV-light sources are used limiting the minimum feature size to around 1 μm. The resolution of a projection system is given by equation (A.3)[137].

$$l = \frac{\lambda k}{NA} \tag{A.3}$$

where k is a resist related ideality factor and NA is the lens' numerical aperture, which specifies the refractive properties including aberrations. Low k resist systems in combination with high NA lenses has resulted in optical systems capable of resolutions as small as 30 nm. However future optical lithography techniques extends to the use of short wavelength extreme UV (EUV) sources and immersion techniques, where the air gap is replaced by a high refracting index liquid improving the resolution [138],[139].

In spite of possessing advantages like low cost and high through put, it also suffers from a number of drawbacks. Firstly for optical lithography the resolution is limited by its wavelength. Secondly optical stepper systems used to improve resolution are very expensive to implement. Hence for nanometre resolution the lithography process becomes very expensive and complicated. Contact photolithography processed used in this work were carried out using the mask aligner (MA

6) generation 2 machine generating a UV-light of wavelength of 365nm.

Metallization

The main methods used to deposit metal on semiconductors are, a) evaporation, b) sputtering and c) plating. However, evaporation and sputtering are the most common methods used to deposit thin metal films on semiconductors whereas plating is used to deposit a much thicker metal cost. For this research all the metals were deposited using the evaporation technique.

Deposition of metal using evaporation technique involves heating the metal to a temperature at which it vaporises. Generally, a magnetically focussed very high energy electron beam (10 kW) produced using a high accelarating voltage applied between a thermionic emmision and the crucible is used to heat up the metal to its vapourizing point. The main evaporator used to deposit the metal stack layers for gate (field plate) and ohmic contacts was Plassys MEB 550S. Figure A.3 shows a schematic diagram of the evaporator. After the insertion of the sample in chamber, the chamber is evacuated to $\backsim 2 \times 10^{-6}$ Torr by a rotary (low vacuum) and cryogenic pump (high vacuum). A high vacuum facilitates in increasing the mean free path of the metal vapours for uniform coating of the sample surface and also to reduce contamination. The sample holder is located approximately 30 cm from the metal crucibles and is protected by two shutters (source and target). They protect the sample from any rate fluctuations of the

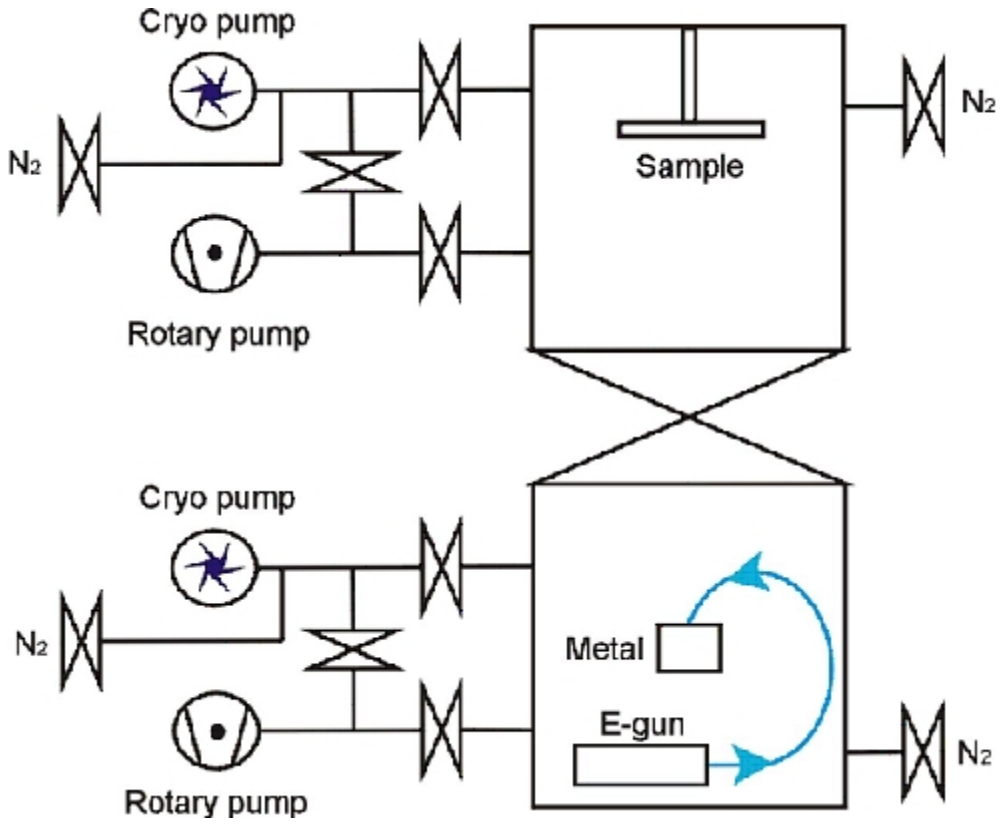

Figure A.3: Schematic diagram of the Plassys MEB 550S electron beam evaporator.

evaporated metal during the initial heating up process. Once the deposition rate fairly stablizes the source shutter opens. The rate of deposition is then controlled to a steady evaporation rate of $\backsim 0.3\ nm/sec$ using a quartz crystal and closed loop feedback. Once the rate stablizes the target shutter opens exposing the sample to the evaporant flux. The depostion parameters like beam current, depostion rate, metal thickness, etc are controlled by an efficient software program ensuring repeatability and uniformity.

Rapid Thermal Annealing

Rapid thermal annealing (RTA) refers to a fabrication process in which semiconductor wafers are heated to very high temperature for a short duration of time by high intensity lamps or lasers in a controlled environment. The temperature of the chamber is generally monitored by a thermocouple or a pyrometre which is operated by a software for real time control and reproducibility of the process. This allows precise control of the temperature ramping and during of the annealing process. Annealing can be done is an inert or an active environment depending on process requirements like oxidation, metal-semiconductor contant formation, activate dopants, repair damage from ion implantation, etc.

In this project the gate-foot oxidation and metal-semiconductor contact annealing was done using Annealsys' AS-ONE RTA equipment.

B. List of Wafers Used in the Project

Datasheet of AlGaN/GaN sample (N3663-5)

The datasheet of the AlGaN/GaN wafer used to fabricate devices in this project is shown in Figure B.1. The distribution of the sheet resistance over the AlGaN/GaN sample is shown in Figure B.2.

Sample	Wafer Layer Structure	Grower	Parameters	Applications
N.A.	2 nm GaN cap 20 nm $Al_{0.35}Ga_{0.65}N$ barrier 3 μm GaN buffer 2 nm AlN nucleation 350 μm sapphire substrate	SVT Assoc., USA	$N_S = \backsim 1.3 \times 10^{13} cm^{-2}$ $\mu_e = \backsim 1700$ cm$^2/V.s$ $R_{SH} = \backsim 200\ \Omega/sq$	Initial analysis of direct oxidation
N3663-5	20 nm $Al_{0.25}Ga_{0.75}N$ barrier 2 μm GaN buffer 2 nm AlN nucleation 350 μm sapphire substrate	NTT. Corp., Japan	$N_S = \backsim 1.1 \times 10^{13} cm^{-2}$ $\mu_e = \backsim 1600$ cm$^2/V.s$ $R_{SH} = \backsim 450\ \Omega/sq$	Device fab. with Al-capped oxidation process

Table B.1: Information regarding the wafer structures used during the project.

NTT AT

2011

Evaluation sheet

2 inch standard HEMT structure on Sapphire

Nano-Technology Business Unit
Advanced Products Business Headquaters
NTT Advanced Technology Corporation

1. Product item: 2 inch standard HEMT structure on Sapphire

2. Epi list

wafer No.	epi-structure	substrate spec
N3663-5	AlGaN / GaN HEMT	2-inch Sapphire substrate diameter: 50.8 ± 0.25mm thickness: 430 ± 25μm orientation: a-axis (0001)±0.1° m-axis (0001) 0.15° ±0.05 orientaion flat: <11-20>±0.3° 16.0±1.5mm polished: One-side mirror polished

3. Quantity 1 piece

4. Date of production
N3863 2009/6/30

5. Epi-layer structure

Structure(set point)

Layer	Material	Thickness (nm)	Al composition	Dopant	Doping
3	un-AlGaN	20	0.25	-	-
2	un-GaN	2000	-	-	-
1	nucleation layer	-	-	-	-
substrate	sapphire				

6. Evaluation data

		N3663-5
Sheet resistance	average (Ω/□)	431.2
	variation (%)	3.75
Mobility	center (cm^2/Vs)	1613
AlGaN barrier	Al composition center	0.247
	AlGaN thickness (nm) center	19.5
Total epi-thickness	average (nm)	1986.3
	variation (%)	1.72
BOW	BOW (μm)	17.79
	SORI (μm)	17.79

Figure B.1: Grower (NTT Corp. Japan) datasheet of AlGaN/GaN HEMT structure used for device fabrication.

N3663-5
Statistical Summary

Number of points	:	28
Average measurement	:	431.2 ohm/sq.
Max. value	:	438.4 ohm/sq.
Min. value	:	422.2 ohm/sq.
Variation in measurement	:	3.753 %
Std. dev. from average	:	5.56 ohm/sq.
Uniformity of wafer	:	1.28 %
Contour Interval	:	1.6

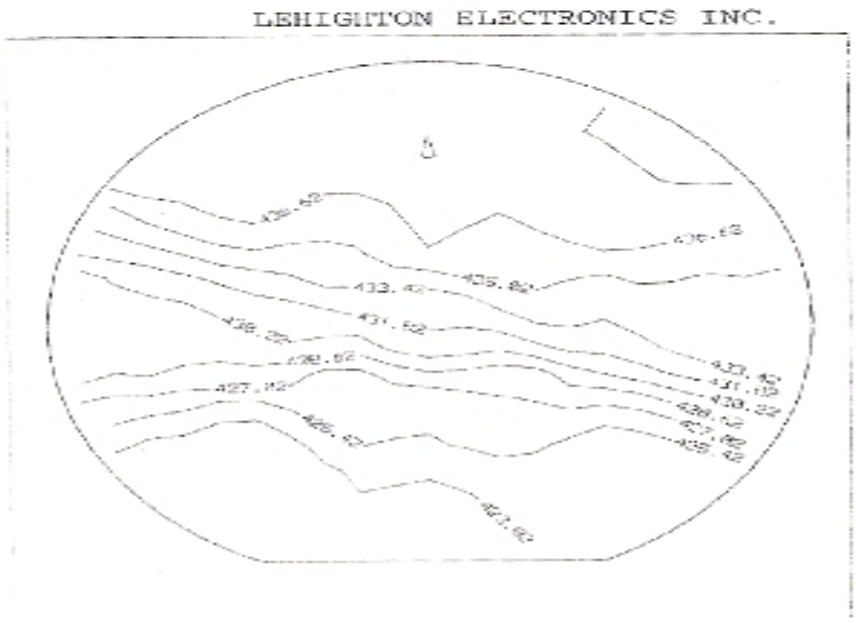

Figure B.2: Sheet resistance distribution of the AlGaN/GaN wafer from NTT Corp., Japan.

C. Device fabrication

Sample Scribing

The wafer was coated with a thick resist film (S1818) before the scribing process in order to protect the sample surface from particles generated during scribing. The wafers were cleaved to small rectangular samples measuring approximately 10 $mm \times 5$ mm.

Sample Cleaning

1. Ultrasonic bath in acetone for 20 minutes.

2. Ultrasonic bath in IPA for 5 minutes.

3. Blow-dry with N_2

Passivation Layer Deposition

1. Deposition of 150 nm Silicon Nitride (SiN) using Inductive Coupled Plasma (ICP).

Gate-Foot Oxidation

1. Spin S1805 at 4000 rpm for 120 sec.

2. Bake on hotplate at 65^0C for 2 min.

3. Post Bake Develop in (1:1) Microposit Developer Concentrate : Water for 60 sec.

4. Rinse in RO water for 60 sec.

5. Blow-dry with N_2.

6. Expose in Mask Aligner 6 (MA6) for 3 sec using Vacuum Contact.

7. Post Exposure development in (1:1) Microposit Developer Concentrate : Water for 75 sec.

8. Rinse in RO water for 60 sec.

9. Blow-dry with N_2.

10. Ash in Gala Asher for 1 min at 60 W.

11. Etch the SiN under the developed gate-foot region using System 100 machine using SF_6/N_2, 15 W, 15 mTorr, 25/25 sccm for 20 min (locally known as 80+RIE machine).

12. Deposit 2 nm Aluminium (Plassys 2).

13. Soak in warm Acetone (50^0C) for 30 min for lift-off.

14. Agitate solution with a dropper to facilitate lift-off and transfer to IPA.

15. Blow-dry with N_2.

16. Anneal the sample at 700^0C for 30 sec in RTA in N_2 environment.

17. Further anneal the sample at 800^0C for required minutes in RTA in O_2 environment.

Ohmic Contact Formation

1. Spin S1818 at 4000 rpm for 120 sec.

2. Bake on hotplate at 65^0C for 2 min.

3. Post Bake Develop in (1:1) Microposit Developer Concentrate : Water for 60 sec.

4. Rinse in RO water for 60 sec.

5. Blow-dry with N_2.

6. Expose in Mask Aligner 6 (MA6) for 5 sec using Vacuum Contact.

7. Post Exposure development in (1:1) Microposit Developer Concentrate : Water for 75 sec.

8. Rinse in RO water for 60 sec.

9. Blow-dry with N_2.

10. Ash in Gala Asher for 1.5 min at 60 W.

11. Etch the SiN under the developed gate-foot region using System 100 machine using SF_6/N_2, 15 W, 15 mTorr, 25/25 sccm for 20 min (80+RIE machine).

12. Deposit n-type ohmic contact of 30 nm Titanium / 180 nm Aluminium / 40 nm Nickel / 100 nm Gold (Plassys 2).

13. Soak in warm Acetone (50^0C) for 30 min for lift-off.

14. Agitate solution with a dropper to facilitate lift-off and transfer to IPA.

15. Blow-dry with N_2.

16. Anneal the sample at 800^0C for 30 sec in RTA in N2 environment.

Field Plate Formation

1. Spin S1805 at 4000 rpm for 120 sec.

2. Bake on hotplate at 65^0C for 2 min.

3. Post Bake Develop in (1:1) Microposit Developer Concentrate : Water for 60 sec.

4. Rinse in RO water for 60 sec.

5. Blow-dry with N_2.

6. Expose in Mask Aligner 6 (MA6) for 3 sec using Vacuum Contact.

7. Post Exposure development in (1:1) Microposit Developer Concentrate : Water for 75 sec.

8. Rinse in RO water for 60 sec.

9. Blow-dry with N_2.

10. Ash in Gala Asher for 1 min at 60W.

11. Deposit 50 nm Nickel / 150 nm Gold (Plassys 1 or 2).

12. Soak in warm Acetone (50^0C) for 30 min for lift-off.

13. Agitate solution with a dropper to facilitate lift-off and transfer to IPA.

14. Blow-dry with N_2.

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