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# Current Collapse and Device Degradation in AlGaN/GaN Heterostructure Field Effect Transistors

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Submitted in fulfilment of the requirements for the Degree of *Doctor of Philosophy* 

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Dedicated to Sophie Isabel, Izabela and my parents

### Abstract

A spectrum of phenomena related to the reliability of AlGaN/GaN HEMTs are investigated in this thesis using numerical simulations. The focus is on trap related phenomena that lead to decrease in the power output and failure of devices, i.e. the current collapse and the device degradation. The current collapse phenomenon has been largely suppressed using SiN passivation, but there are gaps in the understanding of the process leading to this effect. Device degradation, on the other side, is a pending problem of current devices and an obstacle to wide penetration of the market.

Calibration of I-V measurements of two devices is performed with high accuracy to provide a trustworthy starting point for modelling the phenomena of interest. Traditionally, in simulations of nitride based HEMTs, only direct piezoelectric effect is taken into account and the resulting interface charge is thence independent of the electric field. In this work, the impact of the electric field via the converse piezoelectric effect is taken into account and its impact on the bound charge and the drain current is studied, as a refinement of the simulation methodology.

It is widely believed that the current collapse is caused by a virtual gate, i.e. electrons leaked to the surface of the device. We have found a charge distribution that reproduced the I-V measurement that shows current collapse, hence validating the concept of the virtual gate. While it was previously shown that the virtual gate has a similar impact on the I-V curve as is observed during the current collapse, we believe that this is for the first time that a wide range of gate and drain voltages was calibrated.

High gate/drain voltage leading to permanent degradation was also investigated. The hypothesis that stress induced defects and dislocations might be responsible for the degradation was tested but not fully confirmed.

Finally, the leakage of electrons thought to be responsible for formation of the virtual gate and the current collapse due to the Poole-Frenkel emission, is simulated in order to explain the surface charge distribution responsible for the current collapse and deduced in Chapter 5.

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### **List of Conferences and Publications**

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### **1** Introduction

### 1.1 Background

The semiconductor industry has been dominated by silicon technology for decades with its established CMOS process. The major driving force for the growth of the industry was scaling. 22-nm node technology is currently in development and 11-nm node is predicted to reach the market in 2015 [1]. In this or the following decade, further scaling will reach the limits. Hence, new semiconductor materials, SiGe, SiC, III-V and II-VI, and new transistor architectures are investigated to replace or to complement silicon.

The conventional III-V semiconductors (As-based and P-based) achieved considerable success in optoelectronic devices, i.e. light emitting diodes (LEDs) and laser diodes (LDs), ranging from infrared to yellow (As-based) and green (P-based) part of the spectrum, and high-frequency devices (HEMTs). However, relatively narrow band-gap prevents them from being used in high-power and high-temperature applications and from reaching blue, violet and UV part of the spectrum.

High-power high-frequency devices are required by wireless communication (satellite communications, TV broadcasting, broadband wireless internet connection, transmitter base station amplifiers) and military (radars, missile seekers) applications [2]. To meet these needs, research has focused on devices based on Si, SiGe, SiC, GaAs and GaN. The band-gap width is an important parameter, since it implies large breakdown electric field, which allows for devices with large breakdown voltages. The suitability of a material for high-power high-frequency applications is assessed by Johnson's figure of merit (JM) [3],

listed for the above mentioned materials in Table 1.1, along with other related material parameters. JM is a product of the breakdown electric field and saturation velocity. By comparing the JM values, it becomes clear that the most promising materials for high power, high frequency applications are SiC and GaN. However, with respect to fabricating transistors, GaN has the advantage over SiC of forming heterojunctions.

Table 1.1: Johnson's figure of merit (JM) [3] and related material parameters for different materials. Values taken from [4,2], except for a) reference [5] b) reference [6] c) reference [7] d) reference [8].

	Si	Si <sub>1-x</sub> Ge <sub>x</sub>	4H-SiC	GaAs	GaN
Eq (eV)	1.12	$1.12-0.41x + 0.008x^{2a}$	3.26	1.42	3.42
	indirect	indirect	indirect	direct	direct
$\mu$ (cm <sup>2</sup> .V <sup>-1</sup> .s <sup>-1</sup> )	1350	2500 (x=0.3) <sup>b</sup>	700	8500	1200 (bulk)
					2000 (2DEG)
$v_{sat} \left(10^7 \text{m/s}\right)$	1.0	0.6 (x=0.3) °	2.0	1.0	2.5
$E_{br}$ (MV/cm)	0.3	-	3.0	0.4	3.3
$JM/JM_{Si}$	1		20	2.7	27.5
$(JM=E_{br}v_{sat}/2\pi)$		-	60 <sup>d</sup>	3.5 <sup>d</sup>	80 <sup>d</sup>

Apart from the large band-gap and favourable JM, the material properties of N-based semiconductor compounds furnish also other advantages over the conventional III-Vs, leading to superior performance parameters. The presence of spontaneous polarization and the fact that the piezoelectric polarization is approximately ten times higher than in Asbased semiconductors, give rise to *polarization doping* in N-based heterostructures, first predicted by Bykhovski *et. al.* [9], which makes the elemental doping of the N-based devices unnecessary. From the absence of doping follows the reduction of ionized impurity scattering and therefore increase in electron mobility. The resulting two-dimensional electron gas (2DEG) density in GaN-based devices reached above 10<sup>13</sup>cm<sup>-2</sup>, making it five times larger than that of GaAs. The AlGaN/GaN 2DEG was for the first time observed by Asif Khan *et. al.* in 1992 [10], followed by the first demonstration of promising DC [11] and RF [12] performance of AlGaN/GaN HEMTs. Nowadays, the achieved output power density of 30-40W/mm is more than ten times higher than that of GaAs based transistors. As a consequence, to achieve the same output power, the size may be ten times reduced, reducing the cost of the device [13]. With respect to applications in optoelectronic devices, the advantage of GaN over SiC rests on the direct band-gap, allowing for higher intensity of the emitted light, and the advantage over GaAs rests on larger band-gap, allowing for LEDs and LDs with shorter wavelength. The GaN/InGaN/GaN double heterostructure was first used to fabricate efficient blue light LED in 1993 [14] and LD in 1997 [15] by Nakamura. Since then, GaN was also utilized for fabricating UV detectors [16].



Figure 1.1: Summary of failure mechanisms in AlGaN/GaN HEMTs. Taken from [17].

GaN-based devices have shown remarkable high-power high-frequency performance, yet achieving the reliability and stability, at the same time as the high performance [18], remains an open problem that restrains the wider commercial use of these devices. The failure mechanisms are studied intensively, reviewed [17,19,20] and include the device degradation [21,22], current collapse [23,24,25,26] and self-heating [27,28]. Device degradation is a permanent reduction of the drain current after long life tests, exceeding 10<sup>3</sup>hours. The current collapse is a temporary drain current reduction due to trapping effects at the surface and in bulk. Both the degradation and current collapse are trap-related phenomena; the degradation involves creating new trap states, while current collapse involves trapping electrons in already existing traps. The failure mechanisms are summarized in Figure 1.1. Two leading hypotheses for the cause of device degradation are hot-electron effects [17] and stress-induced defect generation via the converse piezoelectric effect [29]. The latter hypothesis is supported by experimental measurement of increased strain using the micro-Raman technique [30] and the fact that the device is degraded when it is biased above a critical drain-to-gate voltage [31], even in an OFF-state. During current

collapse, electrons are trapped mainly on surface states. It is proposed that the mechanism responsible for the electron leakage from the Schottky contacts to the traps is Poole-Frenkel electric field dependent surface conduction model [32,33,34,35], first described in 1938 [36].

#### 1.2 Aims and Objectives

In this thesis, we aim to develop numerical simulations methodology for studying the failure mechanisms related to trapped charge, i.e. current collapse and device degradation. This task includes the following objectives:

- (i) As a starting point, to accurately *calibrate* the numerical simulations of real measured AlGaN/GaN test bed devices in the absence of current collapse and degradation.
- (ii) To develop a self-consistent methodology for including the impact of the *field induced polarization* on the transistor characteristics and the accuracy of the calibration process.
- (iii) To study the *current collapse* in GaN HEMTs and to develop an automated procedure for extracting the distribution of the related trapped charge that would reproduce the effects as measured by I-V characteristics.
- (iv) To explore the *non-linear transport of carriers* injected from the gate to the HEMT surface and the following trap-to-trap hopping to reproduce the surface charge distribution obtained by the current collapse calibration.
- (v) Since the device degradation is thought to be related to converse piezoelectric effect, we will also study the impact of this effect on the stress formation in the transistor in relation to the permanent transistor *degradation*.

#### 1.3 Outline

The rest of this thesis is organized as follows.
Chapter 2 introduces the crystal, electrical and elastic properties of III-N materials, discusses the polarization effects and the origin of the resulting 2DEG. Furthermore, N-based heterostructures and their properties, such as band discontinuity and polarization induced bound charge, are discussed. Finally, the operation of AlGaN/GaN HEMTs is explained, with referral to state of the art devices and key challenges in the technology.

Chapter 3 describes the methods and tools used in this work, i.e. the commercial simulator Sentaurus by Synopsys and scripts developed to manipulate the input files and to automatically perform and evaluate simulations. Besides that, the model with its basic equations governing the simulations is described. Finally, the calibration of the numerical simulations against the experimental data is explained in detail and exemplified in respect of the two transistors used later on in this study.

Chapter 4 investigates the impact of the converse piezoelectric effect on polarization induced bound charge, using self-consistent simulation. A coupled model for piezoelectric materials, including the impact of the field, is used to determine the strain, the polarization and the bound charge distribution in the device. The impact on the transistor current-voltage characteristics is quantified.

Chapter 5 investigates trap related phenomena, namely current collapse, more specifically DC-RF dispersion or "knee" walkout, and device degradation. Since the surface trapped charge plays role in both phenomena, the impact of various distributions on I-V characteristics is investigated, to build on the gained insights later. The current collapse experimental data is calibrated with an asymmetrical exponential surface charge distribution. Further, the electric field is linked to mechanical stress generated in the device and that stress, in turn, to defects with trapped charge. Two relationships between the stress in the device and the trapped charge are proposed and investigated through their impact on the I-V characteristics.

Using the surface charge distribution obtained by the current collapse measurement calibration in Chapter 5 as a target, Eyring's reaction rate model and Poole-Frenkel emission model are employed to reproduce the distribution in Chapter 6. Wide range of input parameters is considered to investigate the temporal evolution of several quantities,

such as the electron surface distribution, the electric field at the surface and at the gate edges and the surface current densities at the gate edges.

Chapter 7 summarizes the results obtained in previous chapters and draws the corresponding conclusions. It also outlines future challenges in GaN HEMT reliability simulations.

# 2 GaN and Related Devices

This chapter provides background information about GaN as a semiconductor material and its implementation in the design of high electron mobility transistors (HEMTs) for high frequency – high power applications. Section 2.1 outlines the physical properties of GaN as a semiconductor material. Section 2.2 deals with its polarization properties that play important role in the formation of 2DEG at the AlGaN/GaN interface. The properties of the 2DEG are discussed in more details in Section 2.3. Section 2.4 introduces the basic concepts and operation of AlGaN/GaN HEMTs while Section 2.5 discusses some of the challenges of the GaN technology.

# 2.1 Physical Properties

## 2.1.1 Crystal Structure

III-N (AlN, GaN, InN) semiconductors crystallize in both the wurtzite hexagonal close packed (HCP) ( $\alpha$ -phase) and cubic zinc-blende ( $\beta$ -phase) crystal structures. The wurtzite is the more stable structure and possesses the spontaneous polarization  $P_{sp}$ , which can be exploited in creating high-density 2DEG (two dimensional electron gas) at III-N heterointerfaces. This crystal structure is therefore the structure of choice for device production, and hence will be of interest in this work. On the contrary, the conventional III-V semiconductors, such as GaAs or InP, crystallize in the zinc-blende structure.



Figure 2.1: III-Nitrides crystallize in cubic zinc-blende (left) and hexagonal wurtzite (right) structure. They both lack the centre of symmetry, so they show piezoelectricity. The wurtzite, which is a lower symmetry crystal, possesses also the spontaneous polarization. The lattice parameters a, c and u are shown for the wurtzite structure. The arrows on the zinc-blende structure depict the set of <111> directions. Adapted from [37].

The wurtzite structure is characterized as tetrahedrally coordinated, with a hexagonal Bravais lattice with four atoms per unit cell [38]. The structure, shown in Figure 2.1 (right), is fully defined by three lattice constants. The length of a side of the hexagonal base is labelled a, the height of the cell is labelled c and an internal dimensionless parameter u determines the length of a III-N bond along the c-axis in multiples of c. In an *ideal* wurtzite structure, i.e., for touching hard spheres, the ratio of these parameters is u/c = 3/8 = 0.375 and  $c/a = \sqrt{8/3} \approx 1.633$ . Due to the low symmetry of wurtzites, even an ideal structure will exhibit spontaneous polarization of approximately one third to one half of the actual  $P_{sp}$  of a real structure [39]. The rest comes from structural non-ideality of III-N semiconductors. The structural parameters of III-Ns are reported in Table 2.1.

The wurtzite structure lacks inversion symmetry along its *c*-axis (called the pyroelectric axis) and hence the directions [0001] and [0001] are not equivalent, as shown in Figure 2.2. This lack of symmetry gives rise to the spontaneous polarization in III-N semiconductors. The conventional positive direction of the *c*-axis in III-Ns is the one that follows the direction from the group III atom to the N atom. According to the atom on the top position of the {0001} bilayer, the (0001) plane is called the Ga- (Al-, In-) face, while the plane (0001) is called the N-face. The crystal is then said to have a Ga-(Al-, In-)

polarity or N-polarity. The electric dipole in III-Ns is directed from the N to the Ga (Al, In) atom, i.e. the value of the polarization is negative. III-Ns are usually grown in either of before mentioned directions, i.e., perpendicularly to the {0001} basal plane. In this way, the abrupt change of the polarization at the interface of a heterostructure can be exploited in device operation. Since polarization is a bulk property [40], the polarity of the crystal does not depend on the surface layer, i.e. the termination, but solely on the direction of the crystal structure.



Figure 2.2: Ga- and N- face of GaN. AlN and InN show similar structure. The *c*-axis is the polar axis in wurtzite crystals. The group III (Al, Ga, In) and N atoms along this bond form the dipoles, which are the basis for the macroscopic polarization. Taken from [41]

## 2.1.2 Electrical Properties

Large band-gap in GaN and AlN leads to high breakdown electric field in these materials, 3.3 MV/cm in GaN and 11.7 MV/cm in AlN [42]. These are very high fields compared to the 0.3MV/cm in Si. Combined with high thermal conductivities of these materials, it makes them suitable for high-power and high-temperature applications, and due to their high saturation velocity, they can operate at high frequencies. The fact that the III-Ns are direct band-gap semiconductors makes them a good candidate for optical applications as well. The values of some parameters determining the electronic properties of III-Ns are summarized in Table 1.1.

While the values of band-gap energies of GaN (3.42 eV) [43] and AlN (6.13 eV) [43] are well established and variation in the literature is minor, there is still a considerable

disagreement over the band-gap energy of InN (0.7 eV – 1.9 eV) [44]. Nitride ternaries and quaternaries form a continuous range of band-gap energies  $E_g$  in between that allows for precise band-gap engineering. The interpolation of  $E_g$  is in general not linear; it is well approximated using a parabolic model employing a so-called bowing parameter *b*. For an arbitrary parameter *p*, the model is expressed as

(2.1) 
$$p(A_x B_{1-x} N) = xp(AN) + (1-x)p(BN) + b_{ABN} x(1-x)$$

In the discussed case, the parameter p is the band-gap energy. The band-gap bowing parameter b takes the following values: -0.8 eV for AlGaN, -3.4 eV for AlInN and -1.4 eV for GaInN [44]. The bowing parameters for In containing alloys assume lower values of InN band-gap energies.

Table 2.1: Structural parameters of III-N wurtzite semiconductors

Parameter	GaN	AIN	InN
a (Å)	3.197 <sup>a</sup>	3.108 <sup>a</sup>	3.580 <sup>a</sup>
c/a	1.6297 <sup>a</sup>	1.6033 <sup>a</sup>	1.6180 <sup>a</sup>
$(u-u_{ideal}) \times 10^{-3}$	1.9 <sup>a</sup>	6.4 <sup>a</sup>	3.7 <sup>a</sup>

a) Reference [45]

## 2.1.3 Elastic Properties

The elastic properties of III-Ns are crucial for calculating the piezoelectric polarization. The magnitude of this polarization makes these materials unique for employing in electronic devices. Moreover, the areas strained extensively during the device operation are prone to form defects and hence cause device degradation.

The elastic properties of a material describe the relationship between external forces and internal deformations. The external forces can be described by the stress tensor  $\sigma_{ij}$ , applied on the crystal and related to the resulting deformation, described by the strain tensor  $\varepsilon_{ij}$ . The first index indicates the direction of stress / strain, the second one indicates the direction that is perpendicular to the surface on which the force acts in the case of stress or that is deformed in the case of strain. The relation between these two tensors is given by

(2.2) 
$$\sigma_{ij} = C_{ijkl} \varepsilon_{kl} \quad \text{or} \quad \varepsilon_{kl} = S_{klij} \sigma_{ij}$$

where *C* is the elastic constants (stiffness) tensor and *S* (= *C*<sup>*I*</sup>) is the elastic compliance tensor. Only the symmetrical part of the stress tensor  $\sigma_{ij}$  deforms the crystal, the nonsymmetrical part rotates it. Similarly, the strain tensor  $\varepsilon_{ij}$  can be separated into a symmetrical part representing the deformation and the rotation part. Since body torques have no effect on polarization or defect formation, we are interested in the symmetrical part of the tensors only, and therefore will assume that  $\sigma_{ij} = \sigma_{ji}$  and  $\varepsilon_{ij} = \varepsilon_{jii}$ . From this symmetry follows the symmetry of the elastic tensors  $C_{ijkl} = C_{ijlk} = C_{jilk}$  (true for *S* as well) [46, p. 132]. This reduces the number of independent components as well as allows for reducing the number of indices by rewriting these tensors to matrices using the Voigt notation given in Table 2.2. If a tensor is symmetrical in two of its indices, we can use one index instead and call it the matrix notation, because the new created mathematical object is no more a tensor, merely a matrix. This index will now run from 1 to 6.

Table 2.2: Voigt notation for reducing the number of indices of a property that is symmetrical in two of its indices.

Tensor notation	11	22	33	23, 32	31, 13	12, 21
	xx	уу	ZZ	yz, zy	ZX, XZ	xy, yx
Matrix notation	1	2	3	4	5	6

The matrix of the elastic constants C (which is the same as that of the elastic compliances S) is fully determined by the crystal class of the material and in wurtzites has the form

$$C = \begin{pmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & (C_{11} - C_{12})/2 \end{pmatrix}$$

There are five  $(C_{11}, C_{12}, C_{13}, C_{33}, C_{44})$  independent elastic constants in wurtzites and they are given in Table 2.3 on page 15.

## 2.2 Polarization in III-Ns

#### 2.2.1 On the Origin of Polarization

Polarization in III-Nitride materials is a crucial material property that enables and determines the actual operation of Nitride based devices. The basis for macroscopic polarization in materials with bound charges is a microscopic polarization of atoms due to bonds between atoms, when the centre of negative charge (electrons) shifts away from the centre of the positive charge (nuclei) [47]. Such a polarized atom constitutes a dipole with a dipole moment p. Polarization state of a material can be then described by the vector of electric polarization P, which is defined as a total dipole moment of a unit volume. If the dipoles are identical and their concentration is n, the formula can be expressed as

(2.3) 
$$\vec{P} = n\vec{p} = \vec{p} / \Omega_0$$

where  $\Omega_0$  is a volume that is occupied by a single dipole. If there is no electric field present, most materials have either no dipoles or the orientation of the dipoles is random and hence the total polarization is zero. However, in low symmetry compound crystals, this may not be true and the asymmetry of the bonding may form dipoles, which are consequently a source of polarization. A condition for a structure to exhibit *piezoelectric* polarization  $P_{pz}$ , which is a polarization originating in a mechanical deformation, is to lack a centre of symmetry. Moreover, if the crystal class has either no rotation axis or a single rotation axis, which is not an inversion axis, the bonding in this crystal will be intrinsically asymmetric. Under this condition, the material is a pyroelectric and will show a built-in *spontaneous* polarization  $P_{sp}$ , even without any mechanical or electrical perturbation. This low symmetry axis in the crystal, parallel with the built-in polarization, is called the pyroelectric field are the ferroelectrics. In these materials,  $P_{sp}$  can be inverted by applying a strong electrostatic field. This effect allows an accurate measurement of the spontaneous polarization,  $P_{sp}$ , which is not possible in pyroelectrics.

The most of III-V semiconductors crystallize in either cubic zinc-blende (crystal class  $\overline{4}3m$ ) or hexagonal wurtzite (crystal class 6mm) structures. Both structures meet the

condition of non-centrosymmetricity, therefore they are both piezoelectric materials. The wurtzite has a single six-fold rotational symmetry axis, which does not have inversion symmetry, i.e., meets the condition to possess a spontaneous polarization. Zinc-blende has four three-fold rotational symmetry axes and an inversion axis, therefore it does not meet the condition for a spontaneous polarization and is not a pyroelectric.

An alternative view on the polarization is based on the physical chemistry of bonding. Both the zinc-blende and wurtzite are tetrahedrally coordinated semiconductors, with bonds created by  $sp^3$  hybridization [47]. In an unstrained zinc-blende, the hybridization is perfect, and therefore this structure shows no spontaneous polarization. In wurtzite crystals, on the other hand, the hybridization is not perfect and the bond along the [0001] direction has a different ionicity than the other bonds and hence the wurtzites show the spontaneous polarization. If a strain is applied to the zinc-blende crystal structure in the <111> direction, which has four equivalent directions as seen in Figure 2.1, the bond in that direction is changed and the crystal exhibits piezoelectric polarization. In conclusion, macroscopic polarization arises in low symmetry crystals due to a perturbation (built-in, mechanical, electrical, etc.) in the crystal symmetry or more accurately, in the bond symmetry.

For small strains, the polarization depends on strain linearly. If there is a non-zero polarization at zero strain, we call this polarization spontaneous. There is no other difference between piezoelectric and spontaneous polarization. The total polarization is a sum of both types of polarization,  $P = P_{sp} + P_{pz}$ .



# 2.2.2 Piezoelectricity and Related Material Properties in a Wurtzite

Figure 2.3: The relationships between electrical and mechanical properties of a crystal. The names of the variables (ovals) and the properties (squares) and their corresponding symbols that will be used in this work are shown. The rank of the tensors representing the corresponding variables and properties can be deduced from the number of their indices. Adapted from [46].

Figure 2.3 shows all variables and properties associated with piezoelectricity in crystals and the relationships between them. Let us concentrate on the direct piezoelectric effect (left side of the diagram) for a moment and not take the converse effect into account. This is, in fact, the standard approach in calculating the fixed charge at the heterostructure interface and determining the electron sheet density thus created [48]. From the diagram we can see that, the piezoelectric polarization can be expressed, in various ways, e.g., as [46]

(2.4) 
$$P_i^{pz} = \sum_{jk} d_{ijk} \sigma_{jk} = \sum_{jk} d_{ijk} \left( \sum_{lm} C_{jklm} \varepsilon_{lm} \right) = \sum_{lm} e_{ilm} \varepsilon_{lm} = \sum_{lm} e_{ilm} \left( \sum_{lm} S_{lmjk} \sigma_{jk} \right)$$

This set of formulae, as well as the diagram, gives (besides the expression for the polarization) the relationships between other variables and material properties, e.g.

piezoelectric constants  $e (= d \cdot C)$ , piezoelectric moduli  $d (= e \cdot S)$ , elastic constants (stiffness) C and elastic compliance  $S (= C^{I})$ , too.

The variables depend on external conditions (electric field E, stress  $\sigma$ , and the resulting strain  $\varepsilon$  and piezoelectric polarization  $P^{pz}$ ) and therefore can take different forms.

Parameter	GaN	AIN	InN
$e_{31}$ (C.m <sup>-2</sup> )	-0.34 <sup>a</sup>	-0.53 <sup>a</sup>	-0.41 <sup>a</sup>
e33 (C.m-2)	0.67 <sup>a</sup>	1.50 <sup>a</sup>	0.81 <sup>a</sup>
$e_{15} (C.m^{-2})$	-0.17 °	-0.35 °	-0.11 <sup>c</sup>
$d_{31}$ (pm.V <sup>-1</sup> )	-1.3 °	-1.9 °	-3.3 °
	-1.0 <sup>e</sup>	-2.1 <sup>b, e</sup>	-3.5 <sup>b, e</sup>
d <sub>33</sub> (pm.V <sup>-1</sup> )	2.7 °	5.4 <sup>b, e</sup>	9.3 °
	1.9 <sup>e</sup>		7.6 <sup>b, e</sup>
$d_{15}$ (pm.V <sup>-1</sup> )	1.8 °	2.9 °	5.5 <sup>b, e</sup>
	3.1 <sup>d, e</sup>	3.6 <sup>d, e</sup>	
C <sub>11</sub> (GPa)	367 <sup>f</sup>	396 <sup>f, e</sup>	223 <sup>f, e</sup>
	390 <sup>g, e</sup>		
C <sub>12</sub> (GPa)	135 <sup>f</sup>	137 <sup>f, e</sup>	115 <sup>f, e</sup>
	145 <sup>g, e</sup>		
C <sub>11</sub> + C <sub>12</sub> (GPa)	413 <sup>b</sup>	506 <sup>b</sup>	266 <sup>b</sup>
C <sub>13</sub> (GPa)	68 <sup>a</sup>	94 <sup>a</sup>	70 <sup>a</sup>
	103 <sup>f</sup>	108 <sup>f, e</sup>	92 <sup>f, e</sup>
	106 <sup>g, e</sup>		
C <sub>33</sub> (GPa)	354 <sup>a</sup>	377 <sup>a</sup>	205 <sup>a</sup>
	$405^{\rm f}$	373 <sup>f, e</sup>	224 <sup>f, e</sup>
	396 <sup>g, e</sup>		
C <sub>44</sub> (GPa)	95 <sup>f</sup>	116 <sup>f, e</sup>	48 <sup>f, e</sup>
	105 <sup>g, e</sup>		
$Psp(C.m^{-2})$	-0.034 <sup>a</sup>	-0.090 <sup>a</sup>	-0.042 <sup>a</sup>
a) Reference [45]	e) Refe	rence [44]	

Table 2.3: Essential electromechanical properties of III-Nitrides.

b) Reference [49]

c)

Reference [51] f)

Reference [47]

Reference [52] g)

Reference [50] d)

On the other hand, the forms of the tensors representing internal properties of a crystal (piezoelectric constants e and moduli d, and the already mentioned elastic constants C and compliance tensor S) are fully determined by the crystal class of the material. We have discussed symmetries of the elastic tensors in Section 2.1.3. Similar considerations can be applied to the piezoelectric tensors. The body torques do not produce electric polarization and the electric field can distort a crystal, but does not cause a body to rotate. This fact can be expressed assuming that both the piezoelectric constants e and moduli d are symmetrical in their second and third indices, i.e.  $e_{ijk} = e_{ikj}$  (the same being true for d).

Similarly to the elastic tensors C and S, e and d can be rewritten in a similar manner, using the Voigt notation defined in Table 2.2. The form of the matrix of the piezoelectric constants e, which is the same as the one for the piezoelectric moduli d, for a wurtzite crystal structure, is as follows

$$e = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix}.$$

Only five piezoelectric constants are non-zero in a wurtzite, and only three  $(e_{31}, e_{33}, e_{15})$  of them are independent. Table 2.3 shows the values of the properties that determine piezoelectric and mechanical behaviour of III-Nitrides. There is disagreement over the values of the elastic and piezoelectric constants of III-Ns in literature. The table lists some of the most cited values. Theoretical and experimental results for parameters d and C are discussed in an overview paper [44], and their recommended values are reported. The theoretical calculations of Bernardini *et al.* [45,47,49] provide other set of values. Their elastic constants are usually lower than those given by other authors. Moreover, the constants C, e and d are not arbitrary; they are connected via the equation  $e = d \cdot C$ . Unfortunately, the reported values do not meet this condition, even if given by one set of authors.



Figure 2.4: Spontaneous polarization of III-N binary and ternary alloys. The thin lines show linear Vegardlike interpolation, thick lines show the approximation to second order in disordered ternary nitride alloys, calculated using the parabolic model (2.1) and the previously mentioned bowing parameters [53]. The higher is the mismatch between the lattice constants of the parent binaries, the higher is the spontaneous polarization bowing.

Linear interpolations between two binary compounds of lattice [39] and piezoelectric and elastic [54] constants are assumed for ternary alloys. Piezoelectric moduli depend on piezoelectric and elastic constants, and hence they depend nonlinearly on alloy composition. However, due to nonlinear dependence of the internal parameter u on alloy composition, the spontaneous polarization is a nonlinear function of composition as well [55].

The  $P_{sp}$  of III-N alloys can be expressed using the parabolic model (2.1) with the following bowing parameters: 0.019 C/m<sup>2</sup> for AlGaN, 0.038 C/m<sup>2</sup> for InGaN, and 0.071 C/m<sup>2</sup> for AlInN [53].

Figure 2.4 compares linear and second order interpolation of the spontaneous polarization of III-N ternaries. It is clear that the deviation is smallest for AlGaN. For In containing ternaries, the discrepancy can be up to 40%. It has to be noted that both the linear and the parabolic relationships are only approximate expressions and not precise formulas.

## 2.3 Heterostructure and 2DEG

A junction between two different materials is called a heterojunction, in contrast to a homojunction, which is a junction composed of differently doped regions of only one semiconductor material. Heterostructure is a structure employing a heterojunction. The bandgap energy of a semiconductor is one of the main parameters describing its electrical behaviour. Both materials that form the heterostructure have different band structures and the resulting band structure determines the behaviour of a device based on the heterostructure and therefore is of great importance. The polarization difference between the two materials and the resulting bound charge at their interface play an additional role in determining the band diagram in III-Ns. A device is connected to the outside world via non-rectifying metal-semiconductor contacts, known as ohmic contacts (source and drain terminals of the transistor). This type of contact has virtually no barrier between the metal and the conduction band of the semiconductor. It is a low-resistance junction and it is used to supply the device with carriers. The gate of a HEMT is realized as a rectifying metal-semiconductor contact, known as a Schottky barrier diode. The barrier between the metal and the conduction band of the semiconductor is given as a difference between the work-function of the metal and the affinity of the semiconductor. The contacts have an impact on the final band diagram of the device.

#### 2.3.1 Band Diagram

One of the semiconductors forming a heterostructure will have wider band-gap than the other. In the case of an Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN heterostructure, Al<sub>x</sub>Ga<sub>1-x</sub>N is the wide band-gap semiconductor and GaN is the narrow band-gap semiconductor. At an interface of the two semiconductors, there will be a band-gap discontinuity  $\Delta E_g$ , given by the differences of the band-gap energies of the two materials. The band-gap discontinuity can be separated to the conduction band offset (CBO)  $\Delta E_c$  and the valence band offset (VBO)  $\Delta E_v$ ,  $\Delta E_g = \Delta E_c + \Delta E_v$ . Figure 2.5 shows an energy band diagram of a heterostructure interface. In general, in the presence of doping in either of the two semiconductors, the bands will bend but in III-Ns, a high electron density is created in the device thanks to the high polarization fields and hence it is not necessary to dope the semiconductor. Therefore, we will further assume no doping in the heterostructure.



Figure 2.5: A heterojunction of two different semiconductors, which have different band-gap energies  $E_g$  and affinities  $\chi$ . The difference of the affinities determines the conduction band discontinuity  $\Delta E_c$  and that together with the band-gap energy difference determines the valence band discontinuity  $\Delta E_v$ . In a heterostructure, the electrons and holes see a different barrier height. Doping of either of the semiconductors would result in band bending. However, in III-N based devices, the channel electrons are provided by the polarization difference of the two semiconductors, which is sometimes referred to as polarization doping. Hence there is no need for doping.

There are two models in literature to calculate the two offsets in III-Ns at a particular fraction x from  $\Delta E_g$ . One splits the discontinuity evenly for all fractions x of a binary compound in the ternary, e.g.  $\Delta E_c = 0.68\Delta E_g$  [56], or VBO is interpolated linearly [57]. In the latter one, all of the band-gap bowing is limited to the conduction band. A further complication arises from the non-equivalence of the (0001)- and (0001) - face, which results in a dependence of the values of the offsets on the direction of the junction [58]. E.g., for AlN/GaN (0001)  $\Delta E_v = -0.2$  eV, while for GaN/AlN (0001)  $\Delta E_v = 0.85$  eV [59].

As will be shown in subsection 2.3.3, the difference in polarization of the materials will produce bound charge at the interface. In the case of AlGaN/GaN heterostructure grown in the (0001) direction, there will be a positive charge at the interface and negative at the heterostructure surface. Figure 2.6 shows how this affects the conduction band; the effect on the valence band is the same.



Figure 2.6: The impact of interface and surface charges on the conduction band of a heterostructure. The thin solid line represents the conduction band without any bound charges. However, the difference in polarization of the two semiconductors induces a positive bound charge at the heterointerface. This pulls the conduction band down evenly in the thin barrier layer (thick dashed line, which coincides with the thick solid line in the narrow band-gap semiconductor). This charge attracts electrons on the side of the narrow band-gap semiconductor. These electrons screen the electric field and, as a consequence, bend the conduction band upwards. Finally, the polarization field induces a negative bound charge at the surface, which pulls up the conduction band, as shown by the thick solid line.

#### 2.3.2 Polarization in a Heterostructure

Nitride devices are based on exploiting the difference in polarization between two or more layers of Nitride alloys in creating a bound sheet charge at their interfaces. For the sake of clarity, let us consider the simplest heterostructure, consisting of only two layers grown in the Ga-face direction. Usually it is GaN bulk with a ternary nitride alloy on top of it. Without the loss of generality, we can presume it to be  $Al_xGa_{1-x}N$ . Let us now investigate the magnitude of this charge as a function of the alloy composition *x*. Naturally, all III-N compounds that are used in electronics, namely AlN, GaN, and InN, have different lattice constants in an unstrained condition. When, for instance, an AlGaN layer is grown on top of GaN, its lattice has to be strained in order to match the underlying material.

For the purpose of further analysis, we label the *c*-axis and the  $\{0001\}$  plane of the crystal as the *z*-axis and the *xy*-plane, respectively. As mentioned before, the direction of growth of III-Ns employed in devices is parallel (or antiparallel) to the *c*-axis of the crystal, which is normal to the  $\{0001\}$  basal plane. Therefore, the lattice constant of the two layers that has to match in both of them is the side of the hexagonal base *a*. The six-fold rotational

symmetry along the *c*-axis of a wurtzite structure compels the strain in x and y direction to be the same. The strain in the basal plane can be then expressed as

(2.5) 
$$\varepsilon_1 = \frac{a - a_0}{a_0}$$

where  $a_0$  and a are the lattice constants of an unstrained (relaxed) and a strained structure, respectively. In HEMT devices, the GaN layer is usually several orders of magnitude thicker than the AlGaN layer, which is only several nanometers thick. Therefore, it is a plausible assumption that the GaN layer will be fully relaxed, and hence show no piezoelectric polarization, while the AlGaN layer will be strained. In this constellation, awill be the lattice constant of an unstrained GaN (to which the AlGaN crystal structure has to fit / stretch) and  $a_0$  the lattice constant of an unstrained AlGaN and therefore

(2.6) 
$$\varepsilon_1 = \frac{a(0) - a(x)}{a(x)}$$

where a(x) is the lattice constant of an unstrained Al<sub>x</sub>Ga<sub>1-x</sub>N layer and *x* the Al fraction in this layer.

The forces during the epitaxial growth of the top layer act in the *xy*-plane. There is no force acting in the *z*-direction and there are no shear stresses or strains. The relation between piezoelectric polarization  $P_{pz}$  and strain  $\varepsilon$  in formula (2.4), the form of the piezoelectric constants *e* matrix, and the equality of strain in *x* and *y* direction ( $\varepsilon_1 = \varepsilon_3$ ), tell us that in the absence of shear strains the only non-vanishing component of the polarization vector will be the *z*-component taking the following form

(2.7) 
$$P_3^{pz} = 2e_{31}\varepsilon_1 + e_{33}\varepsilon_3$$

From the relation between strain  $\varepsilon$  and stress  $\sigma$  in formula (2.4), the form of the elastic stiffness *C* matrix, and from the assumption of no force applied in the *z*-direction ( $\sigma_3 = 0$ ), we obtain the relation between the strain along the polar axis (in the growth direction)  $\varepsilon_3$  and in the basal plane  $\varepsilon_1$  as

(2.8) 
$$\varepsilon_3 = -2\frac{C_{13}}{C_{33}}\varepsilon_1$$

Combining the previous formulas gives the expression of the piezoelectric polarization in the strained Al<sub>x</sub>Ga<sub>1-x</sub>N layer as a function of the Al fraction *x* (via strain in the *x* direction  $\varepsilon_l$ ) of this layer in two alternative forms

(2.9) 
$$P_{3}^{pz} = 2\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)\varepsilon_{1} = 2d_{31}\left(C_{11} + C_{12} - 2\frac{C_{13}^{2}}{C_{33}}\right)\varepsilon_{1}$$



Figure 2.7: The lattice constants (in this oversimplified drawing, the atoms that have to form bonds are represented by red dots) of an unstrained AlGaN are different from that of an unstrained GaN (left). Yet, when AlGaN grows on the top of GaN, the lattice constant *a*, defining the dimensions of the basal hexagon, has to match the lattice constant of GaN. This exerts a strong stress on the grown layer in the *xy*-plane. This stress causes strain (right) in both of the basal plane ( $\varepsilon_1$ ) and the growth ( $\varepsilon_3$ ) directions, described by the equations (2.6) and (2.8), respectively. The dashed line represents an unstrained piece of AlGaN. In piezoelectric materials, the strain results in polarization field  $P^{pz}$ . In this figure, the Ga-face growth is assumed. In the case of the N-face growth, the orientation of the polarization would be opposite. *a*(0) is the lattice constant of an unstrained GaN or epitaxially strained AlGaN, *a*(*x*) the lattice constant of the wurtzite structure in the middle represents the orientation of the wurtzite structure in the heterostructure.

Three things shall be noted here. First, as a by-product of the equation (2.8), it is possible to express the lateral stress  $\sigma_I$  from (2.4) for epitaxially grown III-N layer as a function of the lateral strain  $\varepsilon_I$ 

(2.10) 
$$\sigma_1 = \left(C_{11} + C_{12} - 2\frac{C_{13}^2}{C_{33}}\right) \varepsilon_1$$

We would like to illustrate some typical values of the lateral stress and strain in III-Ns. In the case of Al<sub>0.28</sub>Ga<sub>0.72</sub>N/GaN heterostructure, the barrier layer grows with a lateral strain  $\varepsilon_1 \approx 8 \times 10^{-3}$  and stress  $\sigma_1 \approx 3.6$ GPa.

Second, the constants that enter the last two formulas, in all the three III-Ns employed in electronic devices, have such values that the dependence of the piezoelectric polarization on the strain is negative, i.e.,  $\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right) < 0$  for all Al<sub>x</sub>In<sub>y</sub>Ga<sub>1-x-y</sub>N, where  $0 \le x \le 1$  and  $0 \le y \le 1 - x$ . From this follows that tensile (compressive) strain, i.e.,  $\varepsilon_l > 0$  ( $\varepsilon_l < 0$ ) results in negative (positive) piezoelectric polarization, i.e., the piezoelectric polarization vector points towards the N-face (group III-face) and hence is parallel (antiparallel) with the spontaneous polarization and acts to increase (reduce) the polarization. The lattice constants of AlN (InN) are smaller (larger) than that of GaN. Therefore, AlGaN grows with a tensile strain on top of GaN depends on the composition. The sign of the piezoelectric constants is the same as in II-VI compounds and opposite to other III-Vs. The values are an order of magnitude larger than in GaAs based crystals [60].

Third, the piezoelectric constants e are calculated in the equilibrium [61] and do not describe the structure under strain. Therefore, the linear dependence given by the equation (2.9) holds only for small strains. For typical strain values in usual III-N structures, the nonlinearity of piezoelectric polarization in the binaries can be reproduced by a second-order polynomial [55]:

(2.11) 
$$P_{AlN}^{pz} = -1.808\varepsilon_1 + 5.624\varepsilon_1^2 \quad \text{for } \varepsilon_l < 0$$
$$P_{AlN}^{pz} = -1.808\varepsilon_1 - 7.888\varepsilon_1^2 \quad \text{for } \varepsilon_l > 0$$

$$P_{GaN}^{pz} = -0.918\varepsilon_1 + 9.541\varepsilon_1^2$$
$$P_{InN}^{pz} = -1.373\varepsilon_1 + 7.559\varepsilon_1^2$$

where  $\varepsilon_l$  is the strain of the binary compound in the basal plane, expressed by the equation (2.6). Unlike the spontaneous polarization, the piezoelectric polarization is independent of microscopic structure [61]. From that follows that the Vegard's law holds and hence the  $P_{pz}$  of a ternary alloy can be calculated as

(2.12) 
$$P_{A_xB_{1-x}N}^{pz} = xP_{AN}^{pz}(\varepsilon(x)) + (1-x)P_{BN}^{pz}(\varepsilon(x))$$

The nonlinearity of piezoelectric polarization comes from nonlinear response of the polarization on the strain of the binary compounds.

Figure 2.8 shows piezoelectric polarization,  $P_{pz}$ , of III-Nitrides grown on GaN plotted against their lattice constants *a*, as well as comparison between the linear and non-linear response model to the epitaxial strain. The impact on the calculation of polarization of AlGaN is not large (see the inset). On the other hand, for alloys with high In content, due to high lattice mismatch and hence high built-in strain, the impact of non-linearity is more pronounced.

The prediction for  $P_{pz}$  assumes pseudomorphic growth of a III-N alloy on a relaxed buffer layer (e.g. AlGaN on GaN). That means that the upper layer (AlGaN) grows with the lattice constant *a* of the buffer (GaN) and hence is fully strained. However, if the mismatch between the lattice constants *a* of the two layers in a relaxed state is above a certain threshold, the upper layer (e.g. AlGaN with a high content of Al) starts to grow partially relaxed and with the lattice constant closer to the relaxed value. For a very high content of Al, the AlGaN layer grows fully relaxed. For thickness of the AlGaN layer of approximately 30nm, the degree of relaxation can be approximated by [48]

(2.13) 
$$r(x) = \begin{cases} 0 & 0 \le x < 0.38\\ 3.5x - 1.33 & 0.38 \le x \le 0.67\\ 1 & 0.67 < x \le 1 \end{cases}$$

The piezoelectric polarization, calculated by either the linear (2.9) or non-linear [using the equations (2.11) and (2.12)] model, has then to be multiplied by a factor of (1 - r(x)) to obtain a realistic prediction.



Figure 2.8: Piezoelectric polarization of III-N ternaries epitaxially grown on GaN. Dashed lines with crosses represent linear piezoelectric response to strain, given by the equation (2.9). The spacing between the crosses represents 10% increase in a binary alloy fraction. The solid lines represent non-linear response to strain in binary compounds and then linearly interpolated for the ternaries. The inset shows the impact of non-linearity of piezoelectric response to strain in the case of AlGaN grown on GaN. For Al fraction up to 65%, the error is lower than 3%.

#### 2.3.3 Bound Charge

A heterointerface of two different III-Ns will induce a discontinuity in the polarization P. As explained previously the polarization vector is associated with a bound charge. The relationship, in its integral and differential form, is as follows

(2.14) 
$$\oint_{\Sigma} \vec{P} \cdot \vec{dS} = -Q_b$$
$$\vec{\nabla} \cdot \vec{P} = -\rho_b$$

where  $Q_b$  is the total bound charge enclosed by the surface  $\Sigma$ ,  $\rho_b$  is the bound charge density. From the assumption of growth in the direction perpendicular to plane {0001} follows that the discontinuity will be in the *z* direction. From the absence of shear strain during the epitaxial growth of the barrier and the form of the piezoelectric tensor *e* follows that the only non-vanishing component of the polarization vector will be the *z* component. To calculate the bound charge at the interface we will use the integral form of (2.14) and construct a closed surface  $\Sigma$  composed of two symmetrical surfaces *S* just above and below the interface and an infinitesimal surface  $\varsigma$  connecting these two surfaces, perpendicular to them and the interface, as shown in Figure 2.9. The bound sheet charge  $\sigma_b$  can be then expressed in terms of the charge enclosed by surface  $\Sigma$ 

(2.15) 
$$\sigma_b = \frac{Q_b}{S} = -\frac{1}{S} \oint_{\Sigma} \vec{P} \cdot \vec{dS} = \frac{1}{S} (P_L - P_u) S = P_L - P_u$$

makes the third step in the equation above possible.

where  $P_L$  is the polarization in the lower layer and  $P_u$  in the upper. The polarization vector is perpendicular to the normal of the surface  $\varsigma$ , hence  $\oint \vec{P} \cdot \vec{dS} = 0$  and the polarization at  $\varsigma$  that surface does not contribute to the value of the integral in the equation (2.15). This



Figure 2.9: The closed surface  $\Sigma$  around an interface with abrupt change of polarization, e.g. AlGaN/GaN interface, is used to calculate the bound sheet charge density by the equation (2.15). The polarization in the figure is drawn in the negative direction, as it is true for all tensile and moderate compressive strains (with no or low content of In) in III-Ns. So, if the magnitude of  $P_u$  is larger than that of  $P_L$ , e.g., in the Ga-face grown AlGaN on GaN, the bound charge will be positive.

In the case of Ga-face AlGaN/GaN interface (2.15) can be rewritten as

(2.16) 
$$\sigma_{b} = P_{GaN} - P_{AlGaN} = P_{GaN}^{sp} + P_{GaN}^{pz} - P_{AlGaN}^{sp} - P_{AlGaN}^{pz}$$
$$= P^{sp}(0) + P^{pz}(0) - P^{sp}(x) - P^{pz}(x)$$

where the argument x is the aluminium fraction of Al<sub>x</sub>Ga<sub>1-x</sub>N. Since the GaN layer is usually several orders of magnitude thicker than AlGaN, it is considered to be relaxed and hence without piezoelectric polarization,  $P^{pz}(0) = 0$ . The values in this equation are zcomponents of P; therefore, all non-zero terms are negative. Since, according to Table 2.3 or Figure 2.4, the magnitude of the spontaneous polarization is higher in AlGaN than in GaN, there will be a positive bound charge at the AlGaN/GaN interface. However, there is usually a material that lacks any polarization (either air or a passivation layer) at the AlGaN surface of the device. Hence,  $P_u$  in the equation (2.15) will be zero, and since  $P_L$  is negative, there will be a negative bound charge at the surface of the device. The situation will be reversed in N-face heterostructure, in which there will be a negative charge at the interface (which will attract holes) and positive at the surface. In theory, there should be some polarization charge at the bottom GaN interface as well, but the induced electric field is assumed to be negligible due to screening by impurities, defects and traps in the GaN layer [56].

Figure 2.11 a) shows the values of the bound sheet charge that appears at the interface due to discontinuity in the polarization, and the contribution of the two types of polarization, in an AlGaN/GaN heterostructure. For low Al concentrations x, the contribution of spontaneous and piezoelectric polarization is of similar magnitude. For higher x, the AlGaN barrier is more and more relaxed and less strained, and hence the piezoelectric polarization of that layer drops down. For very high Al concentrations, the whole bound sheet charge is only due to the difference in spontaneous polarizations between the two layers.

## 2.3.4 2DEG



Figure 2.10: Vertical cross-section of the conduction band in the heterostructure. The dotted line is the position of the Fermi level in the semiconductor.  $\Phi_b$  is a barrier height. In the case of a heterostructure or a HEMT far from the gate the barrier height is determined by the surface sheet charge. Under the gate of a HEMT, it is determined by the Schottky barrier, modified by the applied gate voltage.  $\Delta$  is the penetration of the conduction band edge below the Fermi level at the AlGaN/GaN interface,  $\Delta E_C$  is the conduction band offset,  $E_0$ , is the lowest subband level of the 2DEG. The labels correspond to the ones used in equations (2.17) and (2.18). Adapted from [62].

The large polarization difference at the heterostructure interface produces large bound charge, which in turn gives rise to a high electron sheet density,  $n_s$ . The electron density is affected by the barrier height  $\Phi_b$  [63], and the electron sheet density is calculated as [64]

(2.17) 
$$n_{s}(x,d) = \frac{\sigma_{b}(x)}{e} - \frac{\varepsilon_{0}\varepsilon(x)}{e^{2}d} (e\phi_{b}(x) + \Delta(x) - \Delta E_{c}(x))$$

where  $\Delta$  is the penetration of the conduction band edge below the Fermi level at the ABN/GaN interface (A and B stand either for Al, In or Ga),  $\Delta E_C$  is the conduction band offset,  $\varepsilon_0$  is the dielectric constant of vacuum,  $\varepsilon$  is the relative dielectric constant of the barrier layer.  $\Delta$  is calculated using the expression

(2.18) 
$$\Delta(x) = \left(\frac{9\pi\hbar e^2}{8\varepsilon_0\sqrt{8m^*}}\frac{n_s(x,d)}{\varepsilon(x)}\right)^{2/3} + \frac{\pi\hbar^2}{m^*}n_s(x,d)$$

where the first term, in the Figure 2.10 labelled as  $E_0$ , is the lowest subband level of the 2DEG with the effective electron mass  $m^* \approx 0.0228 m_e$  [65]. It follows from the equations (2.17) and (2.18) that the formula to calculate electron sheet density  $n_s$  is itself dependent

on  $n_s$ , thus the calculation has to be carried out self-consistently. Figure 2.11 b) shows the 2DEG concentration as a function of barrier thickness for various Al concentrations.



Figure 2.11: a) Contributions of spontaneous and piezoelectric polarizations to the creation of the bound sheet charge at the AlGaN/GaN interface. The dotted line represents piezoelectric polarization in fully strained layer. However, the AlGaN layer has been found to relax [48] for higher strains. If we take the relaxation of the layer to account, as given by (2.13), the piezoelectric polarization follows the dependence that is shown as the thick dashed line. The difference in spontaneous polarizations between AlGaN and GaN layers is the only contribution for high Al concentrations. For lower concentrations, it is similar to the piezoelectric contribution. b) The dotted lines represent the bound charge at the interface (calculated in the subfigure a as P\_total) for various Al concentrations. As a consequence of the bound charge, 2DEG forms in the GaN channel, as given by the equation (2.17). The solid lines represent the electron density as a function of the AlGaN barrier thickness. For every Al concentration, there is a critical barrier thickness under which no 2DEG is formed.

## 2.4 AIGaN/GaN HEMTs

## 2.4.1 Introduction

A transistor is a semiconductor device with three or more terminals. Its operation is based on controlling a signal at one pair of terminals by a signal applied at another pair of terminals. The main functions of a transistor are to amplify or to switch electronic signals. In a Field Effect Transistor (FET), the current flows between the source and drain terminals (ohmic contacts) through a channel. The channel conductance is modulated by an electric field perpendicular to the surface produced by the voltage applied between the source and gate. In this type of transistors, only the majority carrier is involved in its operation. The gate can be separated from the channel by an insulator (as in a MOSFET), can form a pn junction (JFET), or a Schottky barrier junction with the channel [MEtal Semiconductor FET (MESFET)]. A modification of the MESFETs is the High Electron Mobility Transistor (HEMT), which utilizes a heterostructure to create a potential well perpendicular to the heterointerface. The electrons that are confined to this potential well are free to move parallel to the interface, forming a 2DEG. The conventional HEMTs are GaAs based. Arsenide III-Vs do not possess spontaneous polarization and the piezoelectric constants are an order of magnitude lower than those of nitrides. Therefore, undoped III-V arsenide heterostructures cannot induce high 2DEG. Even with doping, the conventional GaAs based HEMTs can achieve 2DEG density of approximately  $2 \times 10^{12}$  cm<sup>-2</sup>. However, intentional doping is not necessary for GaN based devices, since, due to the high polarization, the 2DEG densities are already on the order of  $10^{13}$  cm<sup>-2</sup>. Moreover, doping could reduce the electron mobility via scattering.



Figure 2.12: Schematic structure of a HEMT device. The figure is not to scale. In a real transistor, the length of the device is much larger than the thickness of the AlGaN barrier. The 2-dimensional electron gas (2DEG) is in the potential well in the GaN layer, which is the lower band-gap semiconductor in this heterostructure, near the heterostructure interface. The 2DEG creates the channel, which leads current in the device. The current flows between the ohmic contacts, the source and the drain, and is modulated by the voltage applied at the gate, which is a Schottky contact.

Figure 2.12 shows a schematic view of a GaN-based HEMT device. The gate is placed asymmetrically. At high drain voltages, the electric field between the gate and drain can be very high, having a peak at the drain edge of the gate. The gate is shifted away from the drain to reduce this field and hence increase the breakdown voltage of the device. However, increasing the distance between the gate and drain has a negative impact on the performance of high frequency devices, especially reducing the cut-off frequency.



#### 2.4.1.1 Principle of Operation



Figure 2.13: Closing the channel with increasing the negative gate voltage  $V_G$ . Positive (negative) voltage applied on the gate lowers (increases) the Schottky barrier  $\Phi_b$ . The solid line represents the conduction band and the dotted line represents the Fermi level.  $E_{F,m}$  is a) A fully open channel where the applied  $V_G$  is positive, but this is not necessary. b) Conduction band of a HEMT with negative applied  $V_G$ , but the channel is still open. c) The negative  $V_G$  is larger than the threshold voltage  $V_T$  and the channel is closed.

As mentioned above, the channel conductance in HEMTs is modulated by the voltage  $V_G$  applied to the gate, which is a Schottky contact. The contribution of  $V_G$  will therefore transform the expression for the electron sheet density, given in equation (2.17), to

(2.19) 
$$n_s(x,d) = \frac{\sigma_b(x)}{e} - \frac{\varepsilon_0 \varepsilon(x)}{e^2 d} (e(\phi_b(x) - V_G) + \Delta(x) - \Delta E_c(x))$$

Figure 2.13 shows the band structure of the device under the gate for various gate voltages and hence various regimes of operation. There is a high 2DEG density in the channel in the saturation regime; the density gets smaller with the gate voltage approaching the threshold voltage  $V_T$  in the linear regime; and finally, there are virtually no free electrons to carry current when the channel is closed (as the negative  $V_G$  exceeds  $V_T$ ).

The conducting channel (under the heterointerface, between the source and drain terminals) can be viewed as a resistance. For small drain-source voltage  $V_D$ , the drain current  $I_D$  is approximately linear. When a negative voltage is applied to the gate, the

electrons are partially depleted from the channel and its resistance increases. As the negative gate voltage  $V_G$  is increased, a threshold voltage  $V_T$  is reached. At the threshold, the channel is closed, i.e., completely depleted of electrons, and the  $I_D$  drops to zero. This condition is called *pinch-off*. The evolution of the conduction band with respect to changing  $V_G$  is shown in Figure 2.14 a). Such a transistor, which is switched *on* (the channel is conducting) at zero  $V_G$ , and requires a negative gate voltage to shut down the current, is called *depletion mode* or *normally on* transistor. A device, which is off at zero  $V_G$ , and requires a positive gate voltage to switch the device *on*, is called *enhancement mode* or *normally off* transistor. If  $V_D$  is increased at a fixed  $V_G$ , the drain edge of the gate begins to be reversely biased in respect to the channel, which causes electron depletion in that region. Now, the channel resistance becomes position dependent and since the current has to remain constant, all the additional voltage drops in the region with high resistance, near the drain edge of the gate. The electric field in the source region will not increase anymore and the current will saturate. The potential across the channel is shown in Figure 2.14 b) and the electric field close to the source in its inset.



Figure 2.14: The conduction band across the channel. Gradual closing of the channel due to reverse biasing the gate at a constant drain voltage is shown in the subfigure a). The *x*-component of the electric field close to the source is shown in the inset. As shown in the subfigure b), for small drain voltages, the voltage drop is spread across the whole channel. However, as the drain edge of the gate becomes depleted, any additional voltage applied drops in that region and the electric field near the source does not increase anymore. This is the saturation region. Again, the inset shows the *x*-component of the electric field near the source. The drain current is determined by this electric field. The position of the contacts is indicated at the bottom of each subfigure.

#### 2.4.2 Surface Trap States

The term *traps* refers to energy states in the band-gap of a semiconductor. The origin of traps can be a consequence of several factors, e.g. crystal defects, dislocations, or the presence of impurities. These trap states may be empty or occupied by electrons, which has an impact on the charge they carry. Trap states in the upper part (above the neutral level) of the band gap (closer to the conduction band) are acceptor-like, neutral when empty and negatively charged when occupied. Trap states in the lower part (below the neutral level) of the band gap (closer to the valence band) are donor-like, positively charged when empty and neutral when occupied. Traps at the interface or the surface of a device play an important role in the device operation and performance.

#### 2.4.2.1 Origin of 2DEG

One of the conclusions of Section 2.3.3 was that there is large negative bound charge at the surface of the device. The negative charge would repel the electrons away from the interface and deplete the channel. Moreover, there is a question, what is the origin of the electrons in 2DEG. It was suggested that, after the growth, during the cooling process, free electrons would compensate the polarization-induced charge [64]. As a different solution to both problems, nowadays widely accepted, it was suggested that surface donor-like traps could be the source of both the channel electrons and the positive charge screening the large negative polarization-induced bound charge [66,67]. For low AlGaN barrier thickness, the surface trap level is below the Fermi level, the traps are occupied and hence neutral. At a critical barrier thickness, the surface traps reach the Fermi level and the electrons from these traps are driven into the channel by the strong polarization-induced electric field in AlGaN [56]. The band diagram, with the energy level of the surface traps, with varying barrier thickness is shown in Figure 2.15 a). As the donor-like traps are emptied, they become positively charged and in effect they reduce (passivate) the negative bound charge. In the absence of holes, the energy of these traps has been theoretically predicted to be  $\sim 1.65$  eV in Al<sub>0.35</sub>Ga<sub>0.65</sub>N [67] and, by fitting simulations to experimental data, determined to be in the range of 1.42 eV [66] to 1.85 eV [56] below the conduction band, both in  $Al_{0.27}Ga_{0.73}N$  layer.

#### 2.4.2.2 Impact on HEMT Performance

At large negative gate voltage, electrons from gate may leak to the trap states in the ungated surfaces and create a 'virtual gate' and modulate the depletion region [68]. The corresponding charge distribution in the device is shown in Figure 2.15 b). In pulsed operation, the gate voltage changes abruptly and since the response of the trapped electrons is not immediate, it leads to RF drain current collapse phenomenon. The transient time constants depend on the energy level of the traps [69]. The surface donor-like traps used to explain the origin of 2DEG can explain RF current collapse with time constants on the order of seconds [70], as observed experimentally [71]. However, transients with shorter time constants (10-100  $\mu$ s) can be explained by the existence of surface donors with energy level 0.3 eV [70] resp. 0.25 eV [72] above the valence band.



Figure 2.15: The effect of surface traps on 2DEG creation, reduction of the negative surface bound charge and current collapse. a) The polarization charge induces large electric field in the AlGaN layer. For thin AlGaN barrier, the trap energy level is below the Fermi level and the states are filled. As the barrier reaches a critical thickness, the trap level hits the Fermi level and the traps start to empty and become positively charged and, due to the strong electric field, the electrons transfer to the channel [66,56]. The diagram is only schematic, in reality, the bands in GaN change with the barrier thickness. For a thin barrier, all electrons are in the traps and not in the channel; hence the conduction band will be above the Fermi level and will not bend. b) Large negative  $V_G$  bias will induce high electric field close to the gate and the electrons form the gate leak to the empty surface states, create a "virtual gate" [68] and deplete the channel. In pulsed operation, after the abrupt change of  $V_G$ , it takes some time to remove the trapped electrons and for that time the channel remains partially depleted. This reduces the drain current and hence the expected output power. This phenomenon is called RF current collapse.

#### 2.4.3 Substrates

The most widely used substrates in the GaN technology are Si, sapphire  $(Al_2O_3)$ , and SiC. Recently, diamond and GaN have been employed as substrates as well. The advantage of the diamond is its high thermal conductivity, while the using of GaN reduces the density of impurities. One of the main tasks of a substrate is to conduct and dissipate the heat generated during device operation. This process is governed by the heat flow equation [73]

(2.20) 
$$c\frac{\partial T}{\partial t} = \vec{\nabla} \cdot \left(\kappa \vec{\nabla}T\right) + H$$

where *c* is the heat capacity,  $\kappa$  is the thermal conductivity and *H* is the heat generation rate, usually considered to be equal to Joule heat  $H = \vec{j} \cdot \vec{E}$ . Table 2.4 summarized material parameters determining thermal behaviour of the substrates.

Table 2.4:	Material	parameters	that	determine	heat	dissipation	by	the	substrate.	a)	Reference	[28],	b)
Reference [	74].												

Substrate	Thermal Conductivity (W.cm <sup>-1</sup> .K <sup>-1</sup> )	Heat Capacity (J.g <sup>-1</sup> .K <sup>-1</sup> )	Density (g.cm <sup>-3</sup> )
Al <sub>2</sub> O <sub>3</sub>	0.35 <sup>a</sup> 0.42 <sup>b</sup>	0.77 <sup>a</sup>	3.98 <sup>a</sup>
Si (111)	1.5 <sup>b</sup>		
4H-SiC	3.6 <sup>a</sup> 3.3 <sup>b</sup>	0.66 <sup> a</sup>	3.21 <sup>a</sup>
GaN	1.6 <sup>a</sup> 1.7 <sup>b</sup>	0.49 <sup>a</sup>	6.1 <sup>a</sup>

#### 2.4.3.1 SiC

Lattice mismatch between SiC and GaN is 4%. Thanks to its very good thermal conductivity, it is the most attractive substrate. Layers of GaN grown on this substrate exhibit an excellent crystallographic quality: the density of dislocations is under  $3 \times 10^8$  cm<sup>-2</sup>, thanks to a nucleation layer of AlN, which ensures a smooth transition between the crystal structure of SiC and GaN. Of all substrates, it is the preferred one for high frequency applications. Unfortunately, SiC is very expensive.

#### 2.4.3.2 Sapphire (Al<sub>2</sub>O<sub>3</sub>)

Of the commonly employed substrates, sapphire has the largest lattice mismatch with GaN. Depending on their relative orientation to each other, the mismatch is between 14% and 23%. The main disadvantage of this material, however, is its poor thermal conductivity. This is a problem especially in applications, in which it is necessary to dispose of heat effectively, and it may result in overheating the device. On the other hand, the advantage of this substrate is that it is cheap and available in wafers with large diameters.

#### 2.4.3.3 Si

Si possesses an acceptable thermal conductivity and is reasonably priced. The lattice mismatch with GaN is 17% and its lattice constant is larger than that of GaN. Hence, GaN grows with a tensile stress, which leads to creation of crystal defects, which reduce the performance of the device. An advantage of this substrate is that it offers an opportunity to utilize the advantages of both Si and GaN technologies and to build heterogeneous integrated circuits combining Si MOSFETs with GaN HEMTs on a single chip [75].

#### 2.4.4 State of the Art

GaN HEMT technology is an excellent vehicle for high-power high-frequency applications [2]. The 2009 edition of the International Technology Roadmap for Semiconductors (ITRS) stipulates that in power amplifiers in base stations for wireless communication, in the range of 0.4-10 GHz, GaN has supplanted GaAs [1]. To reduce the negative impact of the surface states, such as RF current collapse, described in Subsection 2.4.2.2, Si<sub>3</sub>N<sub>4</sub> surface passivation was introduced [76]. At high voltage operation, the electric field induced at the drain edge of the gate is very large and can reach the breakdown field and damage the device. To overcome this problem and still be able to go to high voltages and avoid breakdown, field plates were implemented on the drain side of the gate, on the top of the passivation layer [77,78]. The field plates spread the area of the voltage drop, and hence reduce the peak electric field. Figure 2.16 shows the achieved power performance of the state-of-the-art devices employing the three substrates mentioned in Section 2.4.3, without/with the passivation layer and implementing the field plates. To show the

improvement of the technology in the last decade, the figure includes also the first RF data, measured in 1996 [12].



Figure 2.16: Achieved power performance of AlGaN/GaN HEMT technology.

a) Reference [12]	b) Reference [79]	c) Reference [80]
d) Reference [81]	e) Reference [82]	f) Reference [78]
g) Reference [83]	h) Reference [84]	i) Reference [85]

Other devices shown in the figure are from references [86,87,88,89,90,91,92]

# 2.5 Key Challenges in Current GaN Technology

## 2.5.1 Self-Heating

As mentioned earlier, the strength of GaN-based HEMTs, due to their large band-gap, is operation at high voltages. During high-voltage operation, high electric fields and current densities are induced, which in turn generate large amount of heat [73]. Self-heating of the device leads to increase of the lattice temperature, and hence to deterioration of transport properties [93,94]. The performance in high power operation will depend on the quality of the substrate, namely on its thermal conductivity, since it is desirable to dissipate as much heat as possible. The thermal behaviour of GaN-based HEMTs, with emphasis on the influence of the substrate, is extensively investigated. Using micro-Raman spectroscopy [28] for SiC and sapphire substrates, it was shown that the increase of temperature on SiC

is slower than on sapphire. Moreover, on the sapphire substrate, the reached temperature is higher. It was found that the rise and fall of the temperature after switching the device on or off, is very fast for both substrates, below 200 ns. Therefore, apart from DC operation, this phenomenon will affect RF or pulsed operation as well. Using electro-thermal Monte Carlo method [74] for SiC, sapphire, Si, and GaN substrates, it was shown that SiC provides the highest current and the lower peak in temperature and hence is the most suitable substrate for high-power applications. Recently, it was shown that due to thermal effects, the current saturation occurs at a lower electric field than the field at which current saturates in the bulk GaN [95], indicating again, that the thermal effects play a considerable role in the GaN-based HEMT operation.

#### 2.5.2 Current Collapse and Degradation

In the literature, the term *current collapse* is used with two meanings. In a wider sense, it means a class of phenomena that lead to drain current degradation. Historically, however, it was defined, during the development of GaAs-based HEMTs, as a persistent yet recoverable reduction of the dc current at a high  $V_D$  [96]. Some of the other phenomena that fall under the wider meaning of the current collapse are gate and drain lag, and DC-RF dispersion [96]. Gate (drain) lag refers to  $I_D$  transient in response to gate (drain) voltage pulses keeping the drain (gate) voltage constant. The corresponding measurement techniques are combined in the I-V pulsed measurement, in which both the gate and drain voltages are pulsed at the same time from a quiescent bias. The difference between DC operation and I-V pulsed measurement is referred to as DC-RF dispersion, also known as "knee walkout" [97,26] due to the representation of the effect in the I-V plane, illustrated in Figure 5.1 b). All of these effects are recoverable. The leakage current from the gate, and carrier trapping in general, into the surface (as described in Section 2.4.2) and buffer traps is the physical cause behind the current collapse class of the phenomena.

*Device degradation* refers to the unrecoverable  $I_D$  degradation, which occurs after stressing the device by a high voltage for long periods of time, typically for several hours. The effect of the device degradation on the I-V characteristics is similar to that of the DC-RF dispersion. After exhaustive stress experiments, in which it was established that, the device is degraded by operation at high voltages, and not as much at high currents, following explanation of the phenomenon was offered [29]. At high voltages, and hence high electric fields, excessive stress is induced through the inverse piezoelectric effect [98]. The stress forms lattice defects, which act as traps. Thus, the device degradation is also caused by trapping of carriers in the surface and in the buffer. The difference between the current collapse and the device degradation is that, the former is caused by trapping carriers in existing traps, while the latter by creating more traps, probably of energy levels that retain the trapped charges. The recoverable current collapse due to trapping in surface states has been largely suppressed by the means of passivation. On the other hand, device degradation is still a pending problem in GaN technology, and we may quote from the ITRS again, "key challenge in GaN technology ... [is the] reduction of leakage current and understanding of failure mechanisms" [1].

## 2.6 Summary

This chapter discussed the properties of III-N semiconductor materials that are most important for the operation of devices fabricated from this class of materials, such as electrical and elastic properties, and the HEMT devices based on heterostructures from their alloys. Special attention was given to the polarization in III-Ns, because this quantity is much stronger in these materials than in other semiconductors and has a strong influence on the operation of these devices. The difference in the polarization in two III-N alloys at their interface leads to polarization induced bound charge which attracts electrons and creates high concentration 2DEG without the need for doping. Also, the interplay between the mechanical and electrical properties, i.e. the direct and converse piezoelectric effect, was discussed, because this plays an important role in some phenomena affecting the III-N based HEMTs, e.g. in device degradation. The converse piezoelectric effect is elaborated in Chapter 4, where it directly affects the electric field induced polarization and also taken into account in Chapter 5 in investigation of the device degradation. The principle of HEMT operation was discussed along with related topics, such as the influence of surface traps, the substrates used for these devices. An overview of current front end devices was given, as well as current challenges facing the nitride-based devices. The following chapter will exploit the principles laid out here with the final aim of calibrating two devices using a commercial simulator, also introduced in the next chapter.

# **3** Simulation Methodology

This chapter describes the simulation methodology used in the thesis. All simulations are carried out with the commercial simulation tool Sentaurus. The simulation platform is described in section 3.1. The underlying drift diffusion approach is described in section 3.2. The scripts developed to manipulate and have better control over the Sentaurus simulation tool are described in section 3.3. Finally, the calibration procedure is described in section 3.4.

# 3.1 The Simulation Platform

Sentaurus, which is the simulation platform used in this thesis, is a TCAD (Technology Computer-Aided Design) simulation tool from Synopsys [99], which solves a system of partial differential equations to model the electrical behaviour of semiconductor devices [100]. Synopsys TCAD offers a set of simulation tools for process and device simulations. In this work, the following tools were used. *Sentaurus Workbench (SWB)*, a flexible framework environment with advanced visualization and programmability, *Sentaurus Structure Editor (SSE)*, a 2D/3D device editor, *Sentaurus Device (SD)*, a 2D/3D device simulator, and the tools for visualising the simulation results, *Inspect*, used for viewing one-dimensional functions, e.g. I<sub>D</sub>-V<sub>G</sub>, and *Tecplot SV*, used for viewing the distributions of parameters in the device in 2D and 3D. A description of selected tools, by no means exhaustive, follows.
## 3.1.1 SWB: Sentaurus Workbench

*SWB* is a visual environment to manage simulation projects described in detail in [101]. A project is a sequence of simulation tools and an arbitrary number of parameters with an arbitrary number of values assigned to those parameters. Each of the simulation tools has an input file that specifies how the simulation will be run. The parameters can be read from within an input file of any of the simulation tools.



Figure 3.1: Project Editor view of Sentaurus Workbench.

Figure 3.1 shows an example of a project, in a Projector Editor view of *SWB* graphical user interface (GUI). In this specific project, *SSE* has one parameter associated with it (*x*), *SD* has three parameters (*Vgmin*, *Vgmax*, *Vd*), and *Inspect* has none. However, the parameter *x*, that stands for the fraction of Al in the Al<sub>x</sub>Ga<sub>1-x</sub>N barrier layer, is read by both *SSE* and *SD*, and the three parameters associated with *SD* are read by *Inspect* as well, to plot the correct I<sub>D</sub>-V<sub>G</sub> characteristics. *SD* performs simulations of I<sub>D</sub>-V<sub>G</sub> in the range between Vgmin=-6V and Vgmax=2V at ten different values of  $V_D$ . The global parameters make it possible to have general input files and still have consistency between them. Before running the simulations, it is necessary to pre-process the files to convert the parameters to the values specified in the project and to make necessary calculations within the command files using a scripting language of the specific simulation tool.



Figure 3.2: Simulation flow of the Sentaurus simulations platform. Only the tools that were used in this work are mentioned. Not all input/output files are shown. Each simulation tool here corresponds to an input file. First, using *SSE*, files defining the MESH and DOPING are created. Using these files and the simulation tool *SD*, the device simulation (set of voltage sweeps at one of the electrodes) is performed and two types of output files are produced. CURRENT, that records the current and voltage at all electrodes, and DATA, that records all pre-specified simulated parameters in all mesh points, e.g. the electric field, the conduction band, the current density, the electron density, etc. *Inspect* and *Tecplot SV* visualise the CURRENT and DATA files, respectively.

#### 3.1.2 SSE: Sentaurus Structure Editor

SSE is used to define the structure of a device, including the electrodes, doping etc. [102]. In order to create the device structure, it is possible to either directly write/modify the input file or use the GUI, which will create the input file for the user. The *SSE* tool will create the actual device structure based on the input file. The output of *SSE* are several files, two of which are of interest to us (Figure 3.2), a file defining the MESH and a file defining the DOPING in the device that is matched to the mesh points defined in the MESH file. The *SSE* command file has several sections. At the beginning, the user may define variables that will be used later in the file and use simple mathematical operations on them. The advantage of doing this is that a single variable may be used in various places in the input file and so to change all instances, it is necessary to change the definition of that variable only. This is true for all Sentaurus tools' command files. Next, using rectangles or other polygons, the device structure is defined as regions of different materials, with names given to each region, to be used as a reference later in the file and in the *SD* command file. Doping profiles may be defined in this input file. High concentration donor doping is used in a small region around the ohmic contacts (source and drain) of the device to emulate the



Figure 3.3: HEMT structure created in *SSE*, showing the mesh. GaN layer is in grey colour, insulator between the contacts is in red, AlGaN layer between these layers is not visible in this scale due to its thinness and the density of the mesh in that region. The three dents on top of the device, represented by the green lines, not originally shown in the *SSE*, are the electrical contacts; from left to right it is the source, the gate and the drain.

metal spikes. The electrodes are placed at some of the edges of the device. Finally, the mesh density is defined by creating windows in a shape of lines, rectangles or polygons and specifying the mesh density at the ends of the window. At last, using all the specifications, another Sentaurus tool *Mesh* is called from the *SSE* to generate the mesh in the MESH file with doping concentration assigned to each mesh point in the DOPING file. A typical mesh is shown in Figure 3.3 in an *SSE* window with the highest mesh density around the gate. A detail of the gate region is shown in Figure 3.4.



Figure 3.4: Detail of the region under the gate of the HEMT device structure shown in Figure 3.3.

The mesh density is an important aspect of device simulation. Increasing the density has positive impact on the precision of the calculation of current in the device and other parameters of interest, but also negative impact on simulation time. It is therefore necessary to balance the need for precision and reasonable simulation time. High density of the mesh is used in regions important for the operation of a device, i.e. where there are large gradients of parameters such as the electric field or current density. The region of high mesh density in the vertical direction is usually the heterointerface and the channel, and in horizontal direction it is the gate edges, especially the drain edge. In our simulations, the vertical mesh spacing at the AlGaN/GaN interface was around 4Å, the horizontal mesh spacing under the gate was up to 4nm, near the drain edge limited to approximately 1nm. Between the gate and the drain, far from both electrodes, the mesh was sparser, in the order of 10nm. Total mesh size of the simulated devices was in the order of tens of thousands of mesh points. In the investigation of current collapse in Chapter 5, where we placed rapidly changing surface charge, and especially in Chapter 6, in which we investigate trap to trap hopping of electrons along the device surface, the region of high mesh density was extended further towards the electrodes. As mentioned above, reducing the mesh spacing and hence increasing the number of mesh points leads to higher precision of the simulation until a limit is reached above which only the simulation time is increased. The optimal mesh size depends on the investigated problem. We haven't encountered any mesh size related convergence problems.

#### 3.1.3 SD: Sentaurus Device

Sentaurus Device is a tool to define physical models used in the simulation, the model and material parameters and to define and run the actual simulation [103]. Two types of input file are necessary to run a simulation using this tool. A material parameter file, one for each material defined in the device, and a command file, with parameters relating to the whole device.

The command file is divided into several sections governing different aspects of the simulation. The section *Electrode* defines the types of used electrodes (ohmic, Schottky contact, etc.), the initial voltage applied to the electrodes and parameters depending on the type of the contact, e.g. work-function for Schottky contact or contact resistance for ohmic

contacts. The section *Physics* defines the physical models to be used in the device simulation e.g. mobility models, generation-recombination models, etc. The models can be global or specific for a region, a material, an interface or an electrode. Other quantities that can be defined in this section are a fixed charge at a specified interface, traps in the bulk with either uniform or Gaussian profile, etc. The section *Plot* specifies the quantities calculated in the simulation to be output in the DATA file for each mesh point at specified moments of the simulation. The section *Solve* specifies what is actually simulated, i.e., which equations are solved, e.g. Poisson's equation (3.2), current continuity equation for electrodes should change, e.g. for I-V<sub>G</sub> or I-V<sub>D</sub> characteristics. Additionally, it is possible to specify the names for the CURRENT output file for sections of the simulation and specify when to save the DATA output files. Moreover, it is possible to save the state of a simulation and load that state later in the command file.

The material parameters that must be specified in the input file include among others the relative permittivity, temperature dependent band-gap, affinity, electron and hole effective mass or density of states. Other parameters depend on the selected physical models defined in the command file. The drift-diffusion simulation requires a mobility model, defining the low-field mobility, and other model-dependent parameters, such as the saturation velocity.

# 3.2 Carrier Transport

To describe the transport of carriers in a device, we will first introduce the concept of mobility (3.2.1), which relates the motion of the carriers in the device to the electric field. Then, we introduce the fundamental equations that govern the transport of carriers (3.2.2), i.e., the Poisson's equation, which is used to calculate the electrostatic potential  $\Psi$  self-consistently with the electron and hole concentrations, *n* and *p*, and the current continuity equations for electrons and holes.

To close the circle and make the solution self-consistent, it is necessary to calculate the current densities,  $J_n$  and  $J_p$ , from the electrostatic potential  $\Psi$  and the mobile charge concentrations *n* and *p*. This is accomplished by one of the transport models. *Sentaurus Device* implements the following models: *Drift-diffusion (DD), Thermodynamic (TD)*,

*Hydrodynamic* (*HD*) and *Monte Carlo* (*MC*). *Drift-diffusion* implements semiconductor equations in a drft-diffusion approximation to the Boltzmann transport equation (BTE). *TD* model is *DD* extended to include self-heating by solving in addition the heat flow equation including the impact of the temperature gradient on the current densities, with a single temperature for the electrons, holes and the lattice. *HD* model implements energy balance equations to describe non-equilibrium transport conditions assuming different electron, hole and lattice temperatures. *MC* is the most general transport approach, providing solution to the general BTE, but with high computational requirements.

*DD* model cannot capture velocity overshoot which becomes crucial in deep submicron devices and is not accurate in estimating the impact ionization generation rates [103]. *HD* model overcomes these deficiencies of *DD* model at some computational cost. In our work, we have not investigated or considered the impact ionization and the dimensions of the devices was on the order of microns. For these reasons, we have used only the *Drift-diffusion* approach and therefore, from now on we will concentrate on this model (3.2.3).

## 3.2.1 Mobility

In a semiconductor, in the presence of scattering the average velocity of the carriers is proportional to the electric field

$$v_d = \pm \mu E,$$

where  $\mu$  is mobility, a measure of response of the ensemble of carriers to the electric field E, and  $\pm$  accounts for positively/negatively charged particles, i.e., holes and electrons. The mobility is determined by a variety of scattering mechanisms including phonon, ionised impurities, surface roughness and other types of scattering.

## 3.2.2 Transport Equations

The transport in a semiconductor device in the presence of an electric field is described by the self-consistent solution of the Poisson and the current continuity equations for electrons and holes. The Poisson's equation is given by

(3.2) 
$$\nabla \cdot \varepsilon \nabla \psi = -q(p-n+N_{D^+}-N_{A^-}),$$

where *n* and *p* are the electron and hole concentrations,  $\varepsilon$  is the dielectric constant,  $\psi$  is the electrostatic potential, *q* is the elementary charge,  $N_{D^+}$  is the concentration of ionized donors and  $N_{A^-}$  is the concentration of ionized acceptors.

The time dependent current continuity equations for electrons and holes are given by

(3.3) 
$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - R$$
 and  $\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - R$ 

where *R* is the net electron-hole recombination rate (recombination – generation). (3.2) and (3.3) are the basic equations for simulating the carrier transport in semiconductor devices. In a steady state, equation (3.3) becomes

(3.4) 
$$\nabla \cdot J_n = 0$$
 and  $\nabla \cdot J_p = 0$ 

#### 3.2.3 Drift-Diffusion Model

Charged particles in motion give rise to electric current. The electric field sets the charge particles into directed motion and in a semiconductor the average drift velocity of such charged particle is given by equation (3.1). Since the current is defined as a flow of positively charged particles, the current density vector has the direction of the drift of the holes and in the direction opposite to the drift of electrons. Hence, using (3.1), the drift current is given by

(3.5) 
$$J_{drift} = q(-nv_{dn} + pv_{dp}) = q(n\mu_n + p\mu_p)E,$$

where  $\mu_n$  and  $\mu_p$  is the electron and hole mobility.

When a type of particle is distributed unevenly in an environment where it can move freely, the particles will, on average, due to the random thermal motion, move from the region of high concentration to the region of low concentration. This process is called diffusion. The diffusion flux is directly proportional and in the opposite direction to the concentration gradient of the particles. The diffusion current is, similarly to the drift current, oriented in the direction of the diffusion of holes and in the direction opposite to the diffusion of electrons, which leads to

(3.6) 
$$J_{diff} = q (D_n \nabla n - D_p \nabla p),$$

where  $D_n$  and  $D_p$  are diffusion coefficients of electrons and holes.

In the absence of any external bias applied to the semiconductor, the combined drift and diffusion current must be, both for the electrons and holes, equal to zero. Taking into account the expression linking the electron concentration to  $E_F$ - $E_i$ , i.e. the Boltzmann relationship for electrons,

(3.7) 
$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right),$$

and the fact that  $\nabla E_i = -qE$ , we arrive at the Einstein relationship

$$(3.8) D_n = \mu_n \frac{kT}{q},$$

This relationship links the two constants from the expression of the drift (3.5) and diffusion (3.6) currents and shows that they represent the same quantity and differ only by a multiplication coefficient. In the previous equation,  $E_F$  is the Fermi level energy, i.e. the highest occupied energy level at 0K or energy level with 50% probability of being occupied at T > 0K,  $E_i$  is the intrinsic energy level, i.e. the level of  $E_F$  in an intrinsic semiconductor, and  $n_i$  is intrinsic carrier concentration, which is a function of only temperature and band-gap. Under thermodynamic equilibrium conditions,  $E_F$  for electrons and holes is the same. For non-equilibrium conditions it is not true, but (3.7) holds, if separate quasi-Fermi levels are assumed for electrons and holes

(3.9) 
$$\phi_n = \psi - \frac{kT}{q} \ln\left(\frac{n}{n_i}\right)$$

$$\phi_p = \psi + \frac{kT}{q} \ln\left(\frac{p}{n_i}\right)$$

Substituting the Einstein relationship into the drift and diffusion current and using the definition of quasi-Fermi levels, the combined drift-diffusion current density can be expressed as

(3.10) 
$$J_n = -nq\mu_n \nabla \phi_n$$
 and  $J_p = -pq\mu_p \nabla \phi_p$ .

The underlying assumptions of the drift-diffusion model include the relaxation time approximation, equal temperatures of the carriers and the lattice and a slowly varying electric field [104].

# 3.3 Scripts

In order to accomplish the tasks set out in this work, a number of scripts were developed. The tasks can be grouped as follows. Firstly, the scripts included calculations performed outside the scope of the Sentaurus simulator, based on the results from a previous Sentaurus simulation and automatically read from an output file. Based on these calculations, the input files for the next simulations were rewritten and a following simulation performed. Secondly, the scripts included automated loops of Sentaurus simulations to generate a family of results with varying selected parameters in order to calibrate, i.e. find specific values of the parameters that reproduced the measurements, the investigated physical processes. Thirdly, the scripts included automated evaluation of the large number (thousands) of simulation results.

Since some of the subtasks were required repeatedly in different tasks, the appropriate developed procedures were reused multiple times. These include ReadCoords that reads the coordinates of a mesh that represents a device from the MESH file, ReadData that reads a property from the DATA output file in all of the mesh points, WriteData that writes a file in the format of the DATA output file with calculated parameters so that they can be easily visualised using *Tecplot SV*, ReadDoping that reads the doping concentration from the DOPING file that is used by the simulator and WriteDoping that rewrites the doping concentration in the DOPING file. In the following we offer description of some of the scripts used in this work.

Shdop: simply puts sheet charge, converted to charge concentration, at a line with one axis constant and between two points at the other axis, according to the values defined in the script's input file. To accomplish this task, the script uses ReadDoping, to preserve any doping already present in the device, and WriteDoping that writes the original doping with the addition of the specified sheet doping.

Polariz: was used in the simulations of Polarization Induced Bound Charge, reported in Chapter 4, using equation (4.8) for the bound space charge generated by the converse piezoelectric effect and equation (4.9) for the sheet space charge at the AlGaN/GaN interface modified by the same effect. The simulation flow is illustrated in Figure 4.5. In this script, ReadCoords and ReadData read the MESH and DATA files from an initial simulation to access the electric field calculated by Sentaurus and to assign the value to a specific mesh point with its coordinates. Then, the actual calculation of several quantities of interest, such as the lateral stress  $\sigma_3$  (4.4), the vertical strain  $\varepsilon_1$  (4.3), *z*-component of the polarization *P* (4.7) and the bound charge  $\rho_b$ , was performed. Since Sentaurus requires the space charge to be defined in the simulations, the sheet charge was converted to the space charge. Finally, WriteData output the calculated quantities.

StressChrg: was used in investigation of stress induced device degradation, in section 0, and is a slight modification of Polariz, in which the bound charge calculation is replaced by a trapped charge assumed in the regions of high stress, according to one of the proposed models translating the mechanical stress to defect formation.

ChrgDop: Reads the DOPING file by ReadDoping and the DATA file produced either by Polariz or StressChrg, searches for the quantity named "Charge" and writes a new DOPING file by WriteDoping with the original doping and the new charge-as-doping combined. In the investigation of the impact of the converse piezoelectric effect on the I-V characteristics, Polariz and ChrgDop were repeated in a loop until the electric field in the device converged.

CurrColl: was used to calibrate a proposed model of trapped charge at the surface responsible for the current collapse phenomenon, in section 5.4. The script consists of a loop, in which all predetermined values of the searched parameters are selected. Inside of

this loop, Shdop is called to insert an exponential charge distribution at both sides of the gate and a constant charge distribution under the gate. Then, *SD* is called to perform the device simulation with the created doping file. Finally, the I-V characteristics is archived for further analysis.

Extract: was used to extract and evaluate the set of the simulated I-V characteristics, produced by CurrColl, by automatically comparing them to the experimental measurements. First, the appropriate experimental  $I_{D/G}$ - $V_{D/G}$  is read. Then, the first simulation I-V *SD* output in the CURRENT format is read. In general, the values of V in both files are different. Therefore, the next step is to calculate the simulation current at voltages at which the current was measured. Next, the deviation is calculated as a square of the differences between the measured and simulated current for all points and the values are added, and the final value is recorded. Continue with reading the next simulation I-V until all are analysed. Find the simulation simulation of this script was also used in the assessment of the accuracy of the calibration in this chapter, in subsection 3.4.3.3, where it was necessary to compare the measured and the simulated I-V characteristics at bias points that were different in the two sets of data.

PF: was used to simulate the Poole-Frenkel emission and transport mechanism, suggested to be responsible for the electrons leaked to the surface of the device causing the current collapse mechanism, reported in Chapter 6. This procedure is described in detail in section 6.4.

# 3.4 Calibration of the Simulator

## 3.4.1 The parameters



Figure 3.5: The electron mobility in a GaN HEMT as a function of electron concentration at three different values of the temperature [105]. The symbols are at  $V_G = 0V$ .

The aim of the calibration is to reproduce the measured I-V characteristics or other dependence in the simulation, using realistic physical models and realistic values of physical parameters. The parameters of interest are the bound charge at the interface  $\sigma_i$  and surface  $\sigma_s$  of the device, the band-gaps, the permittivity in both GaN and AlGaN, electron effective mass  $m_e^*$ , low-field electron mobility  $\mu_{n0}$  and saturation velocity  $v_{sat}$  in GaN, the contact resistance of the ohmic contacts (source and drain)  $R_c$ , and the gate metal workfunction  $W_f$ , which determines the Schottky contact barrier as  $\phi_{Sch} = W_f - \chi$ , where  $\chi$  is the affinity of a semiconductor, in our case of AlGaN, since the gate is on top of this material. The (positive) bound charge  $\sigma_i$  can be calculated using equation (2.16) and the more general equation (2.15) and the same properties, but determining this parameter accurately becomes more complicated. As was explained in subsection 2.4.2.1, this (negative) charge is partially compensated by emptying the donor-like traps that become in effect positively charged. Hence,  $\sigma_s$  becomes a fitting parameter.

The concept of field dependent mobility (3.2.1) is introduced in the drift-diffusion simulations to take into account the carrier velocity saturation in high electric field

assuming local relation between the velocity and the electric field. One of the most common field dependent mobility models is the Caughey-Thomas model [106] illustrated in Figure 3.6, expressed as

(3.11) 
$$\mu_n = \frac{\mu_{n0}}{\left(1 + (\mu_{n0}E/\nu_{sat})^\beta\right)^{1/\beta}},$$

where  $\mu_{n0}$  is the low-field mobility,  $v_{sat}$  the saturation velocity and  $\beta$  is a fitting parameter that controls how smooth is the transition between the linear and saturated region of the dependence of velocity on the electric field, for electrons usually set to 2.



Figure 3.6: Mobility and velocity as a dependence of the electric field parallel with the carrier current in the Caughey-Thomas mobility model [106]. The mobility in low electric field is governed by  $\mu_{n0}$  and the velocity in high electric field by  $v_{sat}$ , hence the names of the parameters.

Several parameters used in the calibration can be measured independently. This includes, for example, *Rc*. For Ni gate,  $\Phi_{Sch}$  dependence on the Al fraction was measured [107,108] and calculated [109] and assumed to be a linear function. The relative permittivity was reported to be 10.4 for GaN and 10.1 for AlN [48]. It is possible to estimate this parameter for the barrier layer of AlGaN based on the fact that it determines the slope of the

dependence of the electron sheet density on the gate voltage, given by equation (2.19), if there is such a measurement at disposal.  $m_e^*$  in GaN was experimentally measured to be  $0.20m_{e0}$  [110,111] with approximately 1% anisotropy [44]. The experimental values of  $\mu_{n0}$ obtained experimentally at 300K and used in simulations range from  $1070\text{cm}^2$ .V<sup>-1</sup>.s<sup>-1</sup> [23] to  $2000\text{cm}^2$ .V<sup>-1</sup>.s<sup>-1</sup> [112] and the values of  $v_{sat}$  range from  $1 \times 10^7 \text{cm.s}^{-1}$  [23] to  $2.5 \times 10^7 \text{cm.s}^{-1}$ [113]. Yet, when the measured or calculated parameters are used in the simulator without any modification, the simulated I-V does not reproduce accurately the experimental, since parameters like  $\Phi_{Sch}$ ,  $\mu_n$  and  $v_{sat}$  may depend on the implementation of the gate, the heterojunction, the layer structure and other device parameters. Therefore, it is useful to consider the measured and reported values only as a guiding advice and to use the parameters as fitting parameters. Each of the parameters has a distinct impact on the I-V characteristics.

The I-V characteristics can be split into several distinct sections. For  $V_G < V_T$  there is a negligible current in the device, for  $V_G > V_T$ , there is a region of linear dependence of current on voltage and a saturation region. In between the linear and saturation regions there is a transitional "knee" region. In calibrating a device, it is necessary to match the  $V_T$ , the "knee" point in the I-V plane and the slope in the saturation region. The slope in the linear region is given by  $V_T$  and the "knee".  $V_T$  is defined by  $\sigma_i$  and  $W_f$ . Figure 3.7 shows the impact of several fitting parameters,  $\mu_e$  and  $v_{sat}$  in subfigure a) and  $R_c$ ,  $\sigma_s$ ,  $W_f$  in subfigure b), on the "knee" point in the I-V characteristic. E.g. increasing both the mobility and saturation velocity increases both the slope of the linear region and the saturation current but, higher  $v_{sat}$  causes the current to saturate at lower  $V_G$ , while higher  $\mu_e$  at higher  $V_G$ .

## 3.4.2 The procedure

The calibration procedure depends on which parameters we know from the measurements or literature and with what certainty. In general, we proceed from fitting low to high current. First, by adjusting  $W_f$ , we fix  $V_T$ , then, by adjusting  $\mu_{e0}$ , we fit the linear regime and finally, by adjusting  $v_{sat}$ , we fit the saturation current. However, the different parts of the I-V characteristics are not independent and most parameters have an impact on more than one part. Therefore, this procedure is not straightforward and has to be iterated until reproducing the experimental I-V characteristics.



Figure 3.7: Impact of various fitting parameters on  $I_D$ - $V_G$  with focus on the transition from linear regime to saturation. The parameter that is changed between two simulations is enclosed in a box. The units of  $\sigma_s$  are % of what is expected from (2.16) not taking the surface states into account, as discussed in 2.4.2.1. a) The low field mobility (green line) and the saturation velocity (blue line) are changed with respect to the simulation represented by the red line. b) The change of the work-function translates to a shift along the  $V_G$  axis. The impact of the surface charge and the contact resistance is illustrated as well.

Taking into account Figure 3.7, we can view the impact of the fitting parameters as vectors in the I-V plane, shifting the transition region. However, the shift depends on  $V_D$  and the values of other parameters. The combined impact of the parameters is non-linear but, it is possible to take advantage of the view of the fitting parameters as operators that shift the transition region of I-V characteristics.

Figure 3.8 illustrates the calibration method using this transition shift model for I-V curves shown in Figure 3.7 a). For simplicity, here we assume that only three parameters are calibrated and keep the rest of the parameters constant.

- 1. Identify the linear and saturation part of the experimental  $I_D$ - $V_G$  characteristics and, by the means of linear regression, find the straight lines that approximate both parts. Calculate the point where the lines cross and label this point in the I-V space as M.
- 2. Perform an initial simulation.

- 3. Calculate the crossing-point for the initial simulation as in step 1 and label this point as  $S_0$ . Label a vector  $v_0 = M S_0$ , which is the shift of the transition region necessary to calibrate the measured data.
- For each of the fitting parameters, perform a simulation, where this parameter is changed with respect to the initial simulation and keep other parameters constant. Label the change of the parameter Δ*p<sub>i</sub>*, where *i* is the parameter iterator.
- 5. For each of the simulations performed in step 4, calculate the crossing-point and label this point as  $S_i$ . Calculate vectors  $v_i = S_i S_0$ .
- 6. Calculate coefficients  $\alpha_i$ , so that  $\sum \alpha_i v_i = v_0$ . Since we are fitting three parameters and the I<sub>D</sub>-V<sub>G</sub> space is two dimensional, there is freedom in setting one of the parameters. Therefore, we may set several values of one parameter and calculate other parameters for all set values.
- 7. Perform simulations with the values of parameters changed by  $\alpha_i \Delta p_i$  for all sets of  $\alpha$  calculated in step 6.
- 8. If one of the simulations performed in step 7 reproduced the experimental data well, the calibration is finished. If not, choose the best one, label it the initial simulation and go to step 3. Alternatively, choose several promising simulations, label them as the initial one, split the calibration flow and for each of them go to step 3.

It is advisable to find more than one set of parameters, since, using this method, one only finds parameters that reproduce the transition point, not the saturation slope. Having more than one calibration, we can choose the one that is closest to the experimental I-V characteristics. Moreover, the calibration is done only for one value of  $V_D$  and may be off at other  $V_D$ . To avoid this problem, it is best to search in two I<sub>D</sub>-V<sub>G</sub> planes, at two  $V_D$  simultaneously, since this reduces the freedom of calculating the parameters in step 6 and thus leads to increased precision or it is possible to search for more than three parameters at once.



Figure 3.8: Calibration procedure employing the view of the fitting parameters as operators shifting the transition region. The  $I_D$ - $V_G$  simulations (dashed lines) are taken from Figure 3.7 a). The linear and saturation regions are identified (solid thick lines) and straight lines (solid thin lines) that approximate the selected I-V regions are found. A crossing-point (empty circles) is calculated for each pair of the straight lines. These points are then used to calculate by how much we must change the parameters in the next step to shift the transition point to that of the experimental curve.

## 3.4.3 Calibration of Real Devices

#### 3.4.3.1 Device description

Figure 3.9 shows the cross section of the devices simulated in this thesis. Let us label the two devices simulated in this work as Device A and Device B. The structure of the devices is 23nm thick  $Al_xGa_{1-x}N$  barrier, with  $x \approx 28\%$ , on 1.9µm thick GaN layer, which is on top of a SiC substrate. The source-drain separation is 4µm, the source-gate separation is 1µm, and the Ni/Au gate length is 0.25µm. The GaN layer is Fe-doped, which acts as a deep level acceptor with the energy level ≈1eV below CB, for punch-through suppression [114]. Fe concentration is  $1\times10^{16}$ cm<sup>-3</sup> at the AlGaN/GaN interface, increasing to  $1\times10^{18}$ cm<sup>-3</sup> at 1µm deep and then constant to SiC substrate. As mentioned in 3.1.2, high concentration donor doping is used in a small region around the ohmic contacts (source and drain) of the device in the simulator, to emulate the metal spikes. The width of Device A and B is  $2\times50\mu$ m and  $4\times125\mu$ m, respectively. The devices were produced by the same process, with the main difference that the wafer, on which Device B was fabricated, shows more sensitivity to stress and larger DC-RF dispersion, probably because of lost control during processing [115]. It was taken to our advantage and, in this work, in Chapters 5 and 6, the stress sensitive Device B was used in investigation of the current collapse and device

degradation. Device A was used in investigation of the impact of converse piezoelectric effect and impact of the gate voltage on the bound charge at the AlGaN/GaN interface, in Chapter 4.



Figure 3.9: Schematic illustration of the two HEMT devices simulated in this work (not to scale). The structure of the devices is 23 nm thick  $Al_{0.28}Ga_{0.72}N$  barrier on 1.9µm thick GaN, which is on top of a SiC substrate (not shown here). The source-drain separation is 4µm, the source-gate separation is 1µm, and the Ni/Au gate length is 0.25µm. The electrodes, i.e. the source, the gate and the drain, are represented by thick black lines. The light orange shading in the GaN layer represents Fe doping. The abrupt change in the total polarization, spontaneous (2.2.1) and piezoelectric (2.3.2), represented by the red arrows, gives rise to the bound charge (2.3.3), represented by violet circles with + and – signs, which induces the 2DEG (2.3.4), represented by the green dashed line, which makes the operation of a HEMT possible (2.4.1.1).

#### 3.4.3.2 Calibration Results

Certain regions of the I-V characteristics are affected mainly by some parameters and the fitting parameters usually affect certain regions more than others. This fact is employed in the calibration of a device, exemplified here on Device A, in Figure 3.10. This figure illustrates the extraction of three parameters from certain regions of the I-V characteristics. It is the Schottky barrier height  $\phi_{Sch}$  from the threshold region of I<sub>D</sub>-V<sub>G</sub>, the contact resistance  $R_c$  from the slope of I<sub>D</sub>-V<sub>D</sub> close to V<sub>D</sub> = 0V and the low-field mobility  $\mu_{n0}$  from the linear region of I<sub>D</sub>-V<sub>G</sub> at low  $V_D$ . The calibration of  $\mu_{n0}$  is not straightforward, since fitting the saturation velocity  $v_{sat}$  and the surface charge  $\sigma_s$  disrupts the already calibrated mobility. Therefore, calibration of these parameters is an iterative process. The final

calibration, reported in Figure 3.12 for a wide range of  $V_G$  and  $V_D$ , yielded higher  $\mu_{n0}$  and  $v_{sat}$  than reported in Figure 3.10 c), which is due to the higher calibrated value of  $\sigma_s$ . The calibrated parameters are listed in Table 3.2.



Figure 3.10: Extraction of some of the parameters in the calibration of Device A. a) Matching the  $V_T$  in the simulations with the experimental data determines the Schottky barrier height  $\phi_{Sch}$ . b)  $(dI_D/dV_D)_{V_D=0}$  is affected by the contact resistance  $R_c$ . c) Fitting the linear region of  $I_D$ -V<sub>G</sub> characteristics yields low-field mobility  $\mu_{n0}$ . However, to fit the ON-current too, it is necessary to change the saturation velocity, which disrupts the already fitted part of the curve. The same is true for the surface charge. Therefore, it is necessary to calibrate the device in an iterative process. I-V characteristics for wide range of gate and drain voltages of the calibrated Device A is shown in Figure 3.12 with the values reported in Table 3.2.

Device B was calibrated using the procedure described section 3.4.2 and the calibration of this device is documented in Figure 3.11 with the parameters used in each of the simulations listed in Table 3.1. The initial set of simulations is shown in subfigure a). First, a simulation is performed with a set of parameters, labelled *orig*, and a simulation for each parameter in which that parameter is changed with respect to orig, while other parameters are kept constant. In this case, the fitting parameters are the mobility, the surface charge and the saturation velocity, while the contact resistance ( $R_c = 750\Omega.\mu m$ ) and the Schottky barrier height ( $\phi_{Sch} = 0.95 \text{eV}$ ) were held constant. Then, a crossing point between the linear and saturation region of I<sub>D</sub>-V<sub>G</sub> characteristics is extracted for each of the simulations, as well as for the experimental data, illustrated in subfigure b). It is possible to calculate the modification of each parameter necessary to reach the crossing point of the experimental data. For three parameters, there is an infinite number of combinations but, for a given modification of one parameter, the two other are determined. The impact of increasing the mobility on the crossing point is almost the same as the impact of decreasing the surface charge, but other parts of the I-V characteristics are affected differently by these two parameters.



Figure 3.11: Calibration process of Device B, follows the procedure described in section 3.4.2. The units of the parameters are cm<sup>2</sup>.V<sup>-1</sup>.s<sup>-1</sup> for mobility, % of the surface charge according to equation (2.15), i.e. without the effect of the surface traps, equal to  $-3.4 \times 10^{13}$  cm<sup>-2</sup> and  $\times 10^{6}$  cm.s<sup>-1</sup> for the saturation velocity. a) initial simulation *orig* with estimated fitting parameters and simulations with one parameter changed each, *mob* (mobility), *surf* (surface charge  $\sigma_s$ ) and *v\_sat* (saturation velocity). b) the corresponding crossing points. c) and d) show the I<sub>D</sub>-V<sub>G</sub> characteristics at V<sub>D</sub> = 3V and V<sub>D</sub> = 10V, respectively, calculated from the points in b). As is obvious, the curves differ negligibly at V<sub>D</sub> = 3V, which validates the procedure. Using this method, we can generate a subspace of parameters that give good agreement at a particular voltage and then select a specific combination based on curves at a different voltage. e) and f) show I<sub>D</sub>-V<sub>G</sub> characteristics after several iterations, *simul 31* was selected as the best fit. I-V characteristics using these parameters for a wide range of  $V_D$  and  $V_G$  are reported in Figure 3.13.

The saturation velocity will change very little, since the direction of its impact is almost perpendicular to the desired shift of the crossing point. The subfigures c) and d) show simulation results using parameters generated in this way. Since  $I_D$ -V<sub>G</sub> curves at  $V_D = 3V$ were used as a basis for the calculations, the new curves at this drain voltage, shown in the subfigure c), virtually overlap. This is not the case at  $V_D = 10V$ , shown in the subfigure d). At the higher voltage, the characteristics follow the same path up to a certain  $V_G$  and then deviate. The subfigures e) and f) show the simulated characteristics after a few iterations. The first set of simulations (subfigure d) offer a better calibration for  $V_G \leq -2V$ , but overestimate the current between -1V and 1V and thereafter saturate abruptly, what is not seen in the experimental data. The final calibration (subfigure f) underestimates the current for  $V_G \leq -2V$  but provide a better calibration for  $V_G$  close to 0V, when the device is ON and the saturation appears less abruptly. I-V characteristics using this set of parameters, listed in Table 3.2, for a wide range of  $V_D$  and  $V_G$  are compared to the experimental data and reported in Figure 3.13.

Table 3.1: Fitting parameters used in the simulations of Device B, reported in Figure 3.11. The best fit was achieved in *simul 31*, printed in bold font.

simulation	low-field electron	surface charge	saturation velocity			
	mobility	$\sigma_s$ (% of -3.4×10 <sup>13</sup> cm <sup>-2</sup> )	$v_{sat}$ (×10 <sup>6</sup> cm.s <sup>-1</sup> )			
label	$\mu_{n0} (\mathrm{cm}^2.\mathrm{V}^{-1}.\mathrm{s}^{-1})$					
orig	1200	10	10			
mob	1400	10	10			
surf	1200	12	10			
v_sat	1200	10	8			
simul 01	1312	9.0	10.21			
simul 02	1405	10.5	10.32			
simul 03	1528	12.5	10.46			
simul 04	1621	14.0	10.57			
simul 29	1350	9.59	9.65			
simul 30	1400	10.17	9.59			
simul 31	1450	10.75	9.53			
simul 32	1500	11.33	9.47			



Figure 3.12: Calibration of Device A.  $V_T \approx -5V$ . The parameters used in the calibration are as follows. The low-field mobility  $\mu_{n0} = 1350 \text{ cm}^2 \text{.V}^{-1} \text{.s}^{-1}$ , the saturation velocity  $v_{sat} = 1.04 \times 10^7 \text{ cm} \text{.s}^{-1}$ , the contact resistance  $R_c = 350\Omega$ .µm, the Schottky barrier height  $\Phi_{Sch} = 1.2\text{ eV}$ , the charge at the interface  $\sigma_i = 1.28 \times 10^{13} \text{ cm}^{-2}$  and the charge at the surface  $\sigma_s = -4.76 \times 10^{12} \text{ cm}^{-2}$ .



Figure 3.12 and Figure 3.13 show the calibration of Device A and B, respectively. The accuracy of these results is discussed in the following subsection. Here we focus on the values of the fitted parameters, summarized in Table 3.2, and compare them with values reported in literature.

The dispersion of reported values of  $\mu_{n0}$  is large, e.g. 1460cm<sup>2</sup>.V<sup>-1</sup>.s<sup>-1</sup> [116] and 2000cm<sup>2</sup>.V<sup>-1</sup>.s<sup>-1</sup> [112] have been demonstrated in AlGaN/GaN HEMTs by Hall measurements and 1070cm<sup>2</sup>.V<sup>-1</sup>.s<sup>-1</sup> [23] and 1700cm<sup>2</sup>.V<sup>-1</sup>.s<sup>-1</sup> [56] were used in device simulations, reported to be in agreement with Hall measurements too. The values of the low-field mobility that we have obtained, i.e.  $1350cm^2.V^{-1}.s^{-1}$  and  $1450cm^2.V^{-1}.s^{-1}$  for Device A and Device B, respectively, are well within this wide range of reported values. The situation with  $v_{sat}$  is similar, by Monte Carlo calculations it was predicted to reach  $2.5 \times 10^7 \text{ cm.s}^{-1}$  [113], while measurements continuously show significantly lower values,  $1.1 \times 10^7 \text{ cm.s}^{-1}$  [117] and  $1.32 \times 10^7 \text{ cm.s}^{-1}$  [23] to  $2.3 \times 10^7 \text{ cm.s}^{-1}$  [56]. The values that we have obtained from the calibration are on the lower end of the range of the reported values,  $1.04 \times 10^7 \text{ cm.s}^{-1}$  and  $0.953 \times 10^7 \text{ cm.s}^{-1}$  for Device A and Device B, respectively. The dielectric constant for AlGaN was extracted from the calibration of the dependence of the

2DEG concentration  $n_s$  on  $V_G$ . According to equation (2.19) it is a linear dependence with the slope determined by the dielectric constant and thickness of the barrier. The linear dependence of  $\varepsilon_r$  on the Al fraction was taken from [119]. However, the calibrated  $\varepsilon_r$  is slightly lower than the reported values. The dependence of  $\Phi_{Sch}$  of Ni gate on Al<sub>x</sub>Ga<sub>1-x</sub>N barrier on the Al fraction x is derived in [109] and for x = 0.28 it yields 1.3eV. However, in the case of the simulated devices, the gate was Ni/Au, the value of x is only approximate and the real value of  $\Phi_{Sch}$  depends also on the process of fabrication of the gate. The calibrated value for Device A, 1.2eV, is still close to the calculated one, while the value for Device B, 0.95eV, is little low. The difference in the calibrated values comes from the difference in  $V_T$  of the two devices. Although the difference in  $V_T$  is 0.2V, the difference in  $\Phi_{Sch}$  is 0.25V. This is caused by the difference in the surface charge density. In reality, there may be other reasons for this difference, such as the Al fraction not being the same, resulting in different bound charge at the interface, despite best effort during the fabrication. To simplify the calibration procedure, the interface charge  $\sigma_i$  was not considered to be a fitting parameter, but was calculated using equation (2.16) for x = 0.28, although, in theory, the measurement of the Al fraction in the barrier may not be accurate and the resulting value depends on the spontaneous polarization constants and the piezoelectric polarization model employed, i.e. linear as given by equation (2.9) or nonlinear as given by equations (2.11) and (2.12), and the selected parameters of those models. We have used the non-linear model and sponatneous polarization constants reported in Table 2.3. The surface charge  $\sigma_s$  depends also on the surface trap density and the energy level of the traps, which are not precisely known parameters, and therefore it is necessary to consider this parameter as a fitting parameter. E.g. [56] report a polarization charge density of  $1.75 \times 10^{13}$  cm<sup>-2</sup> and a surface trap density of  $1.36 \times 10^{13}$  cm<sup>-2</sup>, which, in the case of fully emptied traps, as discussed in subsection 2.4.2.1, would result in the surface charge density of  $-3.9 \times 10^{12}$  cm<sup>-2</sup>, which is close to the values yielded by our calibration process. The surface trap density heavily depends on the fabrication process, therefore it cannot be expected that the value will be the same for different devices from different wafers, let alone from different labs. Initially we did not know the value of the contact resistance  $R_c$ and therefore tried to find a reasonable value that would reproduce the measured I-V characteristics. The measured  $R_c$  is unusually high, probably due to lost control in the fabrication process [115]. The discrepancy between the calibrated and measured values has

an impact on some of the other calibrated parameters. Higher  $R_c$  would result in higher  $\mu_{n0}$  and  $v_{sat}$ .

parameter	symbol	Device A	Device B	literature
low-field mobility	$(am^2 V^{-1} s^{-1})$	1250	1450	1070 <sup>a</sup> , 1460 <sup>b</sup> , 1700 <sup>c</sup> ,
(at 300K)	$\mu_{n0}$ (cm · v · · · · · · · · · · · · · · · · ·	1550	1450	2000 <sup>d</sup>
saturation	$(\times 10^7 \text{ cm s}^{-1})$	1.04	0.053	1 <sup>a</sup> , 1.1 <sup>e</sup> , 1.32 <sup>f</sup> , 2.3 <sup>c</sup> ,
velocity	$V_{sat}$ (*10 cm.s )	1.04	0.935	2.5 <sup>g</sup>
dialactria constant			ı	-0.3x+10.4 <sup>h</sup>
	$\varepsilon_r(x)$	-0.4x+9.1		0.03x+10.28 <sup>i</sup>
of Al <sub>x</sub> Ga <sub>1-x</sub> N				-0.4x+9.5 <sup>j</sup>
Schottky barrier	$\Phi_{\rm TA}({\rm aV})$	1.2	0.05	1.2 for Ni <sup>k</sup>
height	$\Psi_{Sch}(ev)$	1.2	0.93	1.5 101 111
interface charge	$\sigma_i (\times 10^{12} \mathrm{cm}^{-2})$	12.8	12.8	eq. (2.16) <sup>i</sup>
surface charge	$\sigma_s (\times 10^{12} \mathrm{cm}^{-2})$	-4.76	-3.65	-3.9 °
contact resistance	$R_c \left( \Omega. \mu \mathrm{m} \right)$	350		750 <sup>1</sup>
			750	1000 <sup>1</sup>
a) Reference [23]	b) Reference [116]	c) Reference [56]		d) Reference [112]
e) Reference [117]	f) Reference [118]	g) Reference [113]		h) Reference [48]
i) Reference [54]	j) Reference [119]	k) Reference [109]		l) Reference [115]

Table 3.2: The values of the fitting parameters in the calibrated devices and in the literature.

#### 3.4.3.3 Accuracy of the Calibration

When we calibrate a device, we do not check the  $I_D$ -V<sub>G</sub> characteristics for all measured  $V_D$ and  $I_D$ -V<sub>D</sub> characteristics for all measured  $V_G$  every time a parameter is changed, since this would be overly time consuming. However, it is necessary to perform the calibration using at least two I-V curves, otherwise it is possible to achieve an excellent fit for a particular  $V_D$  and reproduce the  $I_D$ -V<sub>G</sub> very accurately, yet at a different  $V_D$ , the simulated  $I_D$ -V<sub>G</sub> may be very far from the measured characteristics. Usually, we compare the simulated and measured data for  $I_D$ -V<sub>G</sub> at low and high  $V_D$  (e.g. at 3V and 10V) or at one  $I_D$ -V<sub>G</sub> (e.g. at  $V_D = 3V$ ) and one  $I_D$ -V<sub>D</sub> (e.g. at  $V_G = 0V$ ). In this way we ensure a reasonably good calibration of the drain current for a wide range of both the gate and the drain voltages. Nevertheless, after finding the fitting parameters of a calibration in this way, it is still necessary to estimate the calibration error for the range of  $V_G$  and  $V_D$  of interest.



Figure 3.14: I<sub>D</sub>-V characteristics of Device A. a) The measured dependence of the drain current  $I_D$  on the drain and gate and voltage,  $V_D$  and  $V_G$ . (Figure 3.12 (a) and (b) combined). Calibration error of the simulated  $I_D$ , expressed in % above/below the measured values, (b) as a function of both  $V_D$  and  $V_G$  and separately, as a function of (c)  $V_G$  and (d)  $V_D$ .

As a measure of the accuracy of calibration, we introduce the calibration error term, which is calculated as  $\Delta I_D = (I_{D,s} - I_{D,m})/I_{D,m}$ , where the indices *s* and *m* represent the simulated and measured current, respectively. The measured  $I_D$  (a) and the calibration error, expressed in the figures in %, (b) as a function of  $V_D$  and  $V_G$  are shown in Figure 3.14 for Device A and in Figure 3.15 for Device B. The subfigures (c) and (d) show  $\Delta I_D$  as a function of  $V_G$  and  $V_D$ , respectively. The different views of  $\Delta I_D$  allow to indicate the regions of the  $V_D$ - $V_G$  plane that are well calibrated. For the calibration of Device A, the error is less than 3% for  $V_D \ge 5V$  and  $V_G = (-3 \dots 0)$  V As it is clear in Figure 3.12, the transition from the linear region is smoother in the experimental data than in the simulations, which leads to higher error in that region. This is represented by the ridge of high values in Figure 3.14 b) that starts for low  $V_G$  and  $V_D$  and shifts to higher voltages at both electrodes simultaneously. For the calibration of Device B, the error is less than 3% for  $V_D \ge 2V$  and  $V_G = (-1 \dots 2) V$  with the exception of six bias points. By comparing the subfigures (c) and (d) of Figure 3.14 and Figure 3.15 we can infer that, since the error dispersion is lower in the Device B, that the calibration of this device is more accurate.



Figure 3.15: I<sub>D</sub>-V characteristics of Device B. a) The measured dependence of the drain current  $I_D$  on the drain and gate voltage,  $V_D$  and  $V_G$ . (Figure 3.13 (a) and (b) combined). Calibration error of the simulated  $I_D$ , expressed in % above/below the measured values, (b) as a function of both  $V_D$  and  $V_G$  and separately, as a function of (c)  $V_G$  and (d)  $V_D$ .

The calibration is accurate if  $\Delta I_D$  is close to zero; large negative or positive values are undesirable. To compare the accuracy of the calibration of the two devices, we show the average of absolute values of  $\Delta I_D$  for range of  $V_D$  and  $V_G$  values for both devices in Figure 3.16. For Device A, the error at  $V_G = -5V$  was large (almost 25%) and is out of range of the subfigure a). However, considering that  $V_T \approx -5V$  in Device A and  $I_D$ 

 $(V_{T,A}) \approx 0$ , a large percentage error still means a negligible error in the absolute values. Therefore, this value is excluded from the calculation in subfigure b). In Device A, the average error for all values of  $V_D$  is below 6%. In Device B, the error minimum is shifted to slightly higher values of  $V_G$ . For  $V_G$  between -3 and 0V in Device A and between -1 and 2V in Device B, the average error is below 2.5% and 3.5%, respectively.



Figure 3.16: The calibration error as a dependence of a)  $V_G$  and b)  $V_D$ , averaged over a range of simulated  $V_D$  (1 – 10 V) and  $V_G$  (-4 – 1 V) points, respectively. The error for  $V_G = -5V$  (almost 25% for Device A), since it is close to  $V_T$ , is excluded from the calculation in subfigure b). The average error for all values of  $V_D$  is below 6%. For  $V_G$  between -3 and 0V in Device A and between -1 and 2V in Device B, the average error is below 2.5% and 3.5%, respectively.

# 3.5 Summary

This chapter provided an overview of the Sentaurus simulation platform from Synopsys with an introduction to its tools that were most important for this work, the Sentaurus Workbench, Sentaurus Structure Editor and Sentaurus Device. Further, the most important physical concepts were briefly introduced, such as mobility, drift and diffusion currents, as well as the equations that are solved by Sentaurus Device tool in the drift-diffusion model, such as the Poisson's equation, current continuity equations and the expression for the drift-diffusion current. An important ingredient of this thesis was to automate the simulation process to perform large number of simulations with predetermined sets of values for various fitting parameters, to perform simulations in a loop, in which the following run depended on the results from the previous run, to perform calculations

outside the scope of the Sentaurus simulation platform and couple those calculations to the simulations and, finally, to evaluate the results from all performed simulations. To accomplish these tasks, various procedures and scripts were developed and described concisely in section 3.3. The first indispensable step in investigating any as yet not fully understood aspect of a phenomenon with the help of physical simulations, is to calibrate the simulator against the experimental data in well-known conditions, thus validating the model, the implementation, i.e. the simulation tool, the applicability of the model and the used parameters. In the case of transistors, this is usually accomplished by the calibration of I-V characteristics of the device, discussed thoroughly in section 3.4. First, we introduce the fitting parameters used in the calibration with values reported in the literature, describe the method used in the process of calibration, where we discuss the impact of several of the parameters on different regions of the I<sub>D</sub>-V dependence, and finally, we give an account of the calibration of the two devices used throughout this thesis. Then, we give a detailed description of the devices, extraction of some of the parameters from different parts of the I-V characteristics, the calibrated I-V for wide range of applied drain and gate voltages, we discuss the calibrated parameters and compare their calibrated values to values reported in literature. Finally, we comment on the accuracy of the calibration and estimate the calibration error, which is below 3% for a wide range of bias conditions, specified in 3.4.3.3, and does not exceed 10%, except for  $V_G$  close to  $V_T$ , where  $I_D$  is very low. The calibrated devices are used in the rest of the thesis. As mentioned in 3.4.3.1, Device A was used in the investigation of the polarization induced bound charge and its dependence on  $V_G$  in Chapter 4, and Device B was used in the investigation of current collapse and device degradation phenomena in Chapter 5 and Poole-Frenkel conduction mechanism probably responsible for DC-RF dispersion in Chapter 6.

The simulations in this thesis were performed on the computing cluster that is used by the Device Modelling Group at the University of Glasgow. The cluster is a 1232 core cluster and contains 64 chips (256 cores, 4 cores per chip) of E5462 2.8GHz Xeon with 8GB per node (1G per core) and 122 chips (976 cores, 8 cores per chip) of E5530 2.4Ghz Xeon with 24GB per node (3GB per core).

The CPU time of a device simulation depends on the size of the mesh, on the range of voltages and on the convergence of a given problem. The simulation time of single I-V

simulations (e.g.  $I_D$ - $V_G$  at a particular  $V_D$ ) performed in this thesis typically varied between ten minutes and one hour. However, to fully investigate a phenomenon or achieve a goal, such as device calibration, it is necessary to perform number of simulations. In the case of the device calibration, as reported in Table 3.1, it took 32 iterations plus four initial simulations, all at two different drain voltages, resulting in total 72 device simulations, i.e. approximately 36 hours of CPU time. In Chapter 5, in the search for the surface charge density distribution of a 'virtual gate' that reproduces the current collapse phenomenon, two iterations of all  $3^6x4$  parameter combinations, reported in Table 5.1, were performed, resulting in 5832 simulations, which was approximately 3000 CPU hours. And finally, in Chapter 6, in the investigation of Poole-Frenkel transport mechanism that leads to the 'virtual gate' responsible for the current collapse, 250 iterations were performed at high drain voltage (resulting in longer simulation time) for a single set of investigated parameters. In total, 76 different combinations of four model parameters were simulated. This results in 19'000 simulations, which translates to minimum of  $10^4$  CPU hours. The large cluster was indispensable in achieving the results presented in this thesis.

# 4 Polarization Induced Bound Charge

# 4.1 Introduction

Using self-consistent numerical simulation, we have studied the impact of the fieldinduced polarization on the characteristics of AlGaN/GaN HEMTs. In the simulations, the strain induced by external electric fields is added self-consistently to the built-in strain due to lattice mismatch. It has been suggested that this additional strain can play a role in the device degradation and failure [29]. The study is carried out using commercial TCAD tool carefully calibrated against the measured characteristics of 0.25 µm physical gate length AlGaN/GaN transistors. A coupled model for piezoelectric materials, including the impact of the field, is used to determine the strain and thus the polarization in the device. The spatial charge distribution is derived from the gradient of the polarization and is fed back self-consistently to the simulator.

# 4.2 Converse Piezoelectric Effect

The diagram in Figure 2.3 shows the relationships between physical variables in a piezoelectric material. Until now, we have only considered the direct piezoelectric effect, i.e., the electric polarization field induced by the stress applied to a crystal, which is represented by the left side of the diagram and described by the equation (2.4). By doing so, we have neglected the impact of the electric field on the stress, strain, and polarization of the crystal. However, during the operation of a HEMT, a large electric field is induced

in the device, especially near the contacts. This field induces additional stress in the device. To capture the stress, strain, and polarization distribution in the device, the impact of the electric field has to be included. The right half of Figure 2.3 demonstrates the converse piezoelectric effect, i.e., the deformation of a crystal induced by the electric field. To take the converse piezoelectric effect into account, the simple relationship between stress  $\sigma$  and strain  $\varepsilon$ , given by (2.2), has to be extended to include the contribution of the electric field. The fully coupled equation [120] for piezoelectric materials can be read from the diagram in the Figure 2.3 as

(4.1) 
$$\sigma_i = C_{ij}\varepsilon_j - e_{ki}E_k$$

or

$$\varepsilon_i = S_{ij}\sigma_j + d_{ki}E_k \qquad (i, j = 1 \dots 6, k = 1 \dots 3)$$

where *E* stands for components of the electric field vector and all the indices are given by the Voigt notation, as defined in Table 2.2.

#### 4.2.1 The Clamped Model

(4.1) is a complex system of equations that has to be solved numerically. To get a straightforward analytical solution, we are going to make some simplifying assumptions, known as the "clamped model" [121,30]. The biaxial strain parameters,  $\varepsilon_1$  and  $\varepsilon_2$ , are assumed to be decoupled from the electrical properties [121] and are determined solely by the atomic alignment given by (2.5). This transforms them into constants of equal value given by the lattice mismatch of the two materials. Moreover, from the electric field in *x* and *y* directions, i.e., parallel with the heterojunction interface, induces only shear stresses and strains. These are ignored in the clamped model. Further assumption is that no force is applied in the growth direction [54], i.e., assuming a free surface [121], which means that the vertical stress has to be zero,  $\sigma_3 = 0$ . If these assumptions are applied to the electric field (4.1), we obtain the expression for stresses in the crystal as a function of the electric field



Figure 4.1: Schematic representation of the converse piezoelectric effect, based on the set of equations (4.1). The crystal direction is shown on the left. The wurtzite structure is asymmetrical in the z direction, so the z-component of the electric field,  $E_z$ , will have opposite effect in the positive and negative directions. The two rows represent the opposite directions of  $E_z$ . Other components of E induce only shear strains. In all pictures, the thick grey lined square represents the crystal without the effect of E; the thin black lined square represents the deformation due to the E, as well as external stresses needed to maintain the desired shape. The three columns represent three different boundary conditions. The first column is in the absence of any mechanical external forces,  $\sigma_i = 0$ , for all *i*. In this case, the crystal simply expands in one direction and contracts in the other. The second column is for a completely fixed structure, without the possibility to change the shape. In this case, E will produce forces on surrounding material. The arrows are in the direction of external forces that need to be applied on the structure to prevent it from deforming. Finally, the clamped model, given by the equations (4.3) and (4.4), is shown in the third column. The dashed line represents a freestanding structure, the grey line represents a strained structure, e.g. a thin AlGaN barrier layer grown on GaN, strained to match the underlying layer, and the black line represents the structure under the impact of E. The stress shown in this column is a change in the stress already present due to the layer being already strained.

(4.2) 
$$\sigma_2 = \sigma_1 = (C_{11} + C_{22})\varepsilon_1 + C_{13}\varepsilon_3 - e_{31}E_3$$
$$0 = \sigma_3 = 2C_{13}\varepsilon_1 + C_{33}\varepsilon_3 - e_{33}E_3$$

Using the latter equation, the vertical strain can be expressed as

(4.3) 
$$\varepsilon_3 = -2\frac{C_{13}}{C_{33}}\varepsilon_1 + \frac{e_{33}}{C_{33}}E_3$$

Substituting the vertical strain in the expression for the lateral stress we obtain

(4.4) 
$$\sigma_1 = \left(C_{11} + C_{12} - 2\frac{C_{13}^2}{C_{33}}\right)\varepsilon_1 + \left(\frac{C_{13}}{C_{33}}e_{33} - e_{31}\right)E_3$$

In the absence of the electric field, the equations (4.3) and (4.4) are reduced to (2.8) and (2.10), respectively. Figure 4.1 shows the essence of the converse piezoelectric effect, with different boundary conditions. The rightmost column shows the clamped model approximation. A detailed explanation is given in the caption to the figure.

To give an idea about the magnitude of strains and stresses in devices under the impact of the electric field, we plot them in Figure 4.2 as a function of E for various Al fractions x. To demonstrate the fact that the electric field always increases the strain state of the crystal, the strain energy per unit volume, which is calculated as [46, p. 136-137]

(4.5) 
$$W = \frac{1}{2} C_{ij} \varepsilon_i \varepsilon_j ,$$

is plotted as well. The part of the equation (2.4) that holds, even after taking the converse piezoelectric effect into account, is the relation between the piezoelectric polarization  $P^{pz}$  and strain  $\varepsilon$ . Using the Voigt notation, the relation can be rewritten as [121]



Figure 4.2: Subfigures a) and b) show vertical strain  $\varepsilon_3$  (4.3) and lateral stress  $\sigma_1$  (4.4) respectively, in accordance with the clamped model, as a function of the *z*-component of the electric field  $E_3$ , for various Al fractions *x* of AlGaN, assumed to grow on a thick relaxed GaN layer. From the subfigure a) it may seem that an electric field parallel with the *z* direction ( $E_3 > 0$ ) reduces the strain. Nevertheless, we must remember that, the layer grows with a built-in lateral strain  $\varepsilon_1$ ; the vertical strain  $\varepsilon_3$  is a result of the assumption of no force applied in the *z* direction. Since the electric field in any direction exerts an additional force, any variation in strain will only increase the total strain of the crystal. This is demonstrated by the subfigure c) in which strain energy per unit volume versus the vertical strain or electric field is plotted. A non-zero electric field can increase or decrease the vertical strain, but it always increases the strained state of the crystal.

Considering the expression for the vertical strain  $\varepsilon_3$  given by (4.3), the *z* component of the piezoelectric polarization can be expressed as

(4.7) 
$$P_3^{pz} = 2 \left( e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right) \varepsilon_1 + \frac{e_{33}^2}{C_{33}^2} E_3$$

Again, in the absence of the electric field (or by neglecting its contribution), we arrive at the previously derived equation (2.9). We will label the part of the piezoelectric polarization that is independent of the electric field as  $P_0^{pz}$ . It can be the first term in the

formula (4.7), which is identical to equation (2.9), in the model of linear dependence of piezoelectric polarization on strain, or the combination of the equations (2.11) and (2.12) for the non-linear model, as discussed before.

The clamped model is an approximation and as such has its limitations, which are a consequence of the simplifying assumptions behind the model. The strain / stress in a particular location depend only on built-in strain and the *z* component of the electric field in that location. Apart from ignoring the impact of other components of the electric field and the resulting shear strain / stress, the model neglects mechanical forces exerted by the surrounding material. The non-equilibrium situation produced by this model in a region with  $E_z$  rapidly changing in the *x* direction is shown in Figure 4.3.



Figure 4.3: The deficiency of the clamped model comes from its simplifying assumptions is shown by considering two adjacent elements of a piezoelectric material. Dashed lines represent the situation before applying the electric field. The electric field in the "element 2" is greater than that in the "element 1". From (4.3) and (4.4) it follows that, the lateral stress and vertical strain in those two elements will be different. Two obvious problems arise from this result. One is non-equilibrium in stress; the "element 2" will press on the "element 1" with larger force than the other way around. The second is that a point on the top boundary of the two elements (full circle) will split in two under the influence of the electric field. In a solid matter, this is not possible. As a consequence, even by neglecting (or in the absence of) the x and y components of the electric field, there will still be shear strains and stresses in the device.

## 4.2.2 The Impact of the Bound Charge in the Device

During the device operation under bias, there is a spatially varying electric field. This has two important consequences. Firstly, according to the equation (4.3), there will be spatially varying strain field in the device, which can lead to a change in device properties [122]. In addition, a long-time (several hours) operation under high electric and hence strain field may result in defect formation and therefore in the device degradation [29]. Secondly, according to the equation (4.7), there will be varying polarization field in the device. If we link this result with the fact that, the divergence of the electric polarization is associated with the bound charge (2.14), we realize that, apart from the discontinuity at the interface, as given by (2.15), there will be bound charge also in the bulk of the device. After substituting the expression for the piezoelectric polarization  $P_{pz}$  (4.7) in the differential form of (2.14), we obtain the expression for the bound space charge as

(4.8) 
$$\rho_b = -\frac{e_{33}^2}{C_{33}} \frac{dE_3}{dz}$$



Figure 4.4: The impact of the converse piezoelectric effect on the bound sheet charge at the heterojunction interface. The situation on the left is without taking the effect into account. The spontaneous polarization is not shown, because it is not affected by the electric field or the additional strain. The gray square represents the unstrained AlGaN. AlGaN grows with strain on the relaxed GaN, which results in piezoelectric polarization in AlGaN, and according to (2.15), the difference in the polarizations leads to formation of the interface charge. The charge induces the electric field *E* and, via the converse piezoelectric effect, produces additional strain in both AlGaN and GaN. This modifies the polarization in both layers and hence alters the bound charge, as derived in (4.9). The bias applied at the electrodes, especially the gate, modifies the electric field and therefore the bound interface charge.

Moreover, the bound sheet charge  $\sigma_b$  at the interface will be modified as well. Substituting (4.7) into the general formula for  $\sigma_b$  (2.16), we obtain

(4.9) 
$$\sigma_b = P^{sp}(0) - P^{sp}(x) - P_0^{pz}(x) + \frac{e_{33}^2(x)}{C_{33}(x)} E_3(AlGaN) - \frac{e_{33}^2(0)}{C_{33}(0)} E_3(GaN)$$
The first three terms are those that are present in the formula even without taking the converse piezoelectric effect into account. The last two terms arise due to the converse piezoelectric effect. The  $E_3$  in the formula is the electric field in the two materials, right next to the interface. The impact of the electric field via the converse piezoelectric effect is shown in Figure 4.4.

## 4.3 Simulation Methodology

We have developed a simulation methodology to introduce field-induced strain, i.e., converse piezoelectric strain induced by an applied bias to the transistor, and associated this strain with a charge in a TCAD simulation. Figure 2.12 shows a typical HEMT simulation domain indicating the source, the drain and the gate of the device. We have simulated an  $Al_{0.28}Ga_{0.72}N/GaN$  HEMT with 0.25µm asymmetrical gate and 4µm source-drain distance. The thickness of the AlGaN layer is 23nm. The GaN layer is doped with iron, which acts as a deep level acceptor, with a concentration of  $10^{16}$  cm<sup>-3</sup> at the AlGaN/GaN interface, increasing to  $10^{18}$  cm<sup>-3</sup> at 1µm depth, then constant to the SiC substrate [114].

The first step in the self-consistent cycle is to perform simulations without any additional electric field-induced charge. This was used to calibrate the TCAD simulator in respect to the measured  $I_D$ -V<sub>G</sub> characteristics of a real HEMT achieving the excellent agreement as illustrated in Figure 3.12. Initially, we consider only the built-in polarization, i.e., the spontaneous polarization and the piezoelectric polarization originating from the strain of the Al<sub>0.28</sub>Ga<sub>0.72</sub>N barrier only, which results in the interface charges and induces carriers in the channel. At this stage, the spatial distribution of the electric field and the corresponding field induced polarization and space charge in the two materials are excluded from the solution of the Poisson equation.

Based on this initial simulation, the electric field is evaluated at all locations in the device. Then, using the electromechanical coupling (4.3), this electric field is linked to the strain. Subsequently, this strain is linked to polarization (4.6) and, finally, the polarization to the charge distribution in the device, while using equation (4.8) inside the device and equation (4.9) to modify the charge at the interface of the device. Charge distribution is then fed back into the simulator and the simulations are performed again. This procedure, schematically shown in Figure 4.5, is repeated until convergence is achieved making the whole simulation process self-consistent.



Figure 4.5: Simulation flow to show the impact of the converse piezoelectric effect on the simulated I-V characteristics and electric field distribution in the device.

# 4.4 Results



### 4.4.1 Uncoupled Simulation (Direct Piezoelectric Effect only)

Figure 4.6: Distribution of the electric field in the device at drain voltage  $V_{DS} = 3V$  and gate voltages  $V_{GS} = -6V$  and  $V_{GS} = 0V$ , just under the threshold.



Figure 4.7: The electric field *E* distribution near the gate in the GaN layer, 0.1 nm under the interface, in the linear regime,  $V_D = 3V$ , and saturation,  $V_D = 20V$ . The position of the gate is indicated by the thick solid line at the bottom of each graph and vertical thin dashed lines on the edges of the gate.

The first stage in the simulation loop is to simulate the device (especially the I-V characteristics and the electric field) considering the built-in strain and the resulting direct piezoelectric effect only, i.e., for i = 0 in Figure 4.5. Figure 4.6 shows the initial distribution of the electric field in the transistor, at two different gate voltages ( $V_G = 0V$ , at the on-current, and  $V_G = -6V$ , which is just below the threshold) at drain voltage  $V_D = 3V$ . Figure 4.7 shows the x and z components of the electric field along the channel, 0.1 nm under the AlGaN/GaN interface, for three different gate voltages:  $V_G = 0V$  (ON-current),  $V_G = -4V$  (linear regime), and  $V_G = -6V$  (OFF-current).  $E_x$  is decoupled from the clamped model since it induces shear strains only and they are neglected in the model. However,  $E_z$ alters the bound charge distribution in the device, which has an impact on the electrostatic potential distribution and therefore on  $E_x$ . So, as a result,  $E_x$  will change as well. According to equation (4.3), the vertical electric field induces strain in the device, in addition to the built-in strain that is already present due to lattice mismatch between the layers. This additional strain is displayed in Figure 4.8 at low drain voltage,  $V_D = 3V$ ,  $V_G = -6V$ , and in Figure 4.9 and Figure 4.10 at high drain voltage,  $V_D = 20V$ , in off- ( $V_G = -6V$ ) and on-state  $(V_G = 0V)$  of the device, respectively. The strain, in turn, induces spatially varying piezoelectric polarization, which gives rise to bound charge, given by equation (2.14) in general or (4.8) and (4.9) in the case of wurtzites using the *clamped model*, in both off- and on-state conditions. Figure 4.11 and Figure 4.12 show the distribution of the bound charge near the gate at low (3V) and high (20V) drain voltage, respectively. Feeding this charge distribution back into the device, the simulation of the I<sub>D</sub>-V<sub>G</sub> characteristics was performed until convergence, as indicated in Figure 4.5. The results of the self-consistent simulations are analysed in the following subsections.



Figure 4.8: The distribution of change of the vertical strain in the region close to the gate in the off-state and at a low drain voltage,  $V_D = 3V$ ,  $V_G = -6V$ .



Figure 4.9: The distribution of change of the vertical strain in the region close to the gate in the off-state and at a high drain voltage,  $V_D = 20V$ ,  $V_G = -6V$ .



Figure 4.10: The distribution of change of the vertical strain in the region close to the gate in the on-state and at a high drain voltage,  $V_D = 20V$ ,  $V_G = 0V$ .



Figure 4.11: Distribution of the polarization induced charge in the device, close to the gate, at  $V_{DS} = 3V$ .



Figure 4.12: Distribution of the polarization induced charge in the device, close to the gate, at  $V_{DS} = 20V$ .



#### 4.4.2 Bound Space vs. Bound Sheet Charge

Figure 4.13: Simulation of  $I_D$ - $V_G$  characteristics (top) in the linear region of the device, at  $V_D = 3V$ . The *uncoupled* simulation is without the contribution of the converse piezoelectric effect. The simulation labelled as *coupled (space)* takes the contribution of the bound space charge into account, and the simulation labelled as *coupled* takes also the modification of the bound sheet charge at the interface into account. The two bottom graphs show the drain current shift in the *coupled (space)* (left) and *coupled* (right) models, with respect to the gate voltage  $V_G$ . In saturation regime, the contribution of both effects is comparable, while for the linear regime and at the threshold voltage, the modification of the bound sheet charge at the interface is dominant.

The converse piezoelectric effect results in (i) induced bound space charge in the device, given by (4.8), which was studied in [123,124], and in (ii) modified bound sheet charge at the interface, given by (4.9). In order to determine how do these two effects contribute to the simulation of the operation of the device, i.e., whether one of them is dominant or they are comparable, we ran simulations at  $V_D = 3V$ , i.e. in the linear region of the device.

The simulation was run in three conditions (i) *uncoupled*: neglecting the converse piezoelectric effect, which is the standard method in the most simulations of III-N devices (ii) *coupled (space)*: taking only the bound space charge into account and finally (iii) *coupled:* taking both the bound space charge and modification of the bound sheet charge into account. The  $I_D$ -V<sub>G</sub> characteristics for all three simulations are shown in Figure 4.13. In the two bottom subfigures, we can see that the impact of both of the coupled conditions increases with increasing the negative gate voltage, because of the higher electric field. In the saturation region, at  $V_G \approx 0V$ , the spatial bound charge increases the drain current by approximately 0.5%. When the modification of the sheet charge is added to the simulation, the overall effect is reduction of the I<sub>D</sub> by approximately 0.5%. Hence, the effect of the two types of the bound charge is of similar magnitude, but the sheet charge modification overrides the effect of the space charge. However, at higher negative gate voltages, especially close to the threshold voltage, i.e.,  $V_G \approx V_T$ , the sheet charge effect becomes dominant, and the space charge can be neglected. The main impact of the change in the bound sheet charge is a threshold voltage shift. The gate voltage, at which the saturation region is reached, is virtually unchanged. For the rest of this chapter, all the coupled simulations will take both the bound space and sheet charge into account.

### 4.4.3 Electro-Mechanically Coupled Simulations

Figure 4.14 shows how the bound sheet charge is changed at the interface due to the converse piezoelectric effect, as given by (4.9). In order to investigate how this effect depends on the drain voltage, we performed the self-consistent simulations at high drain voltage ( $V_D = 20V$ ) as well. Figure 4.15 shows the impact of the converse piezoelectric effect on the I<sub>D</sub>-V<sub>G</sub> simulated characteristics. The effect is essentially the same as for low drain voltage ( $V_D = 3V$ , already reported in Figure 4.13). To make an insight, the drain current change at both simulated drain voltages is included in the figure.



Figure 4.14: Modification of the bound sheet charge  $\sigma_b$  at the interface. Away from the gate, the electromechanical coupling results in a constant reduction (approx. 1.5%) of the charge, irrespective of the voltage applied. Under and close to the gate, the electric field is strongly modified by the voltage applied at the electrodes, especially at the gate. Therefore, the bound sheet charge is modified as well.



Figure 4.15: The impact of electro-mechanical coupling on the  $I_D$ -V<sub>G</sub> characteristics at a high drain voltage,  $V_D = 20V$ . The effect is virtually independent on the drain voltage. To give an insight, the drain current shift for low drain voltage ( $V_D = 3V$ , from Figure 4.13) is included in the figure as well. Again, the main effect is in the threshold voltage shift, and diminishes with increasing the gate voltage.



Figure 4.16: The electric field *E* distribution along the channel, under or close to the gate, 0.1 nm under the heterojunction interface. The top subfigures show the electric field change at low drain voltage, the bottom subfigures at high  $V_G$ .  $E_x$  is shown on the subfigures on the left,  $E_z$  on the right. The effect of the polarization induced bound space charge alone (top: *coupled (space)*) on the simulation of *E* is negligible. At gate voltages below threshold (left), the change of  $E_x$  is independent of  $V_D$ .

The polarization induced charge and its modification due to the electro-mechanical coupling has an impact on the electric field distribution in the device. To illustrate this effect, in Figure 4.16 we plot the *x* and *z* components of the electric field along the channel, 0.1 nm under the AlGaN/GaN interface at both low ( $V_D = 3V$ ) and high ( $V_D = 20V$ ) drain voltages. At  $V_D = 3V$ , the distinction between the two coupled models (induced space charge vs. space and sheet charge) is made. As expected from the already shown I-V characteristics, the effect of the induced space charge on the electric field is negligible. However, at high negative gate voltages, the fully coupled model causes an increase of  $E_x$  at the source edge of the gate, which in effect raises the barrier for electrons. Hence the threshold voltage shift observed in Figure 4.15.



Figure 4.17: The conduction band (CB) in the channel, 0.1 nm under the heterojunction interface. The top subfigures show the CB below the threshold voltage of the device, where the potential barrier prevents electrons from flowing through the channel and hence the channel is closed. For both of the considered drain voltages, the barrier is increased. In the bottom subfigure, the CB shift due to the converse piezoelectric effect for various bias conditions is summarized. For voltages below and around the threshold voltage, the region that has an impact on the device operation is under the gate, since it determines the height of the potential barrier. For voltages above the threshold, the important region is between the source and gate. With increasing the gate voltage, the CB shift in this region fades away.

The impact of the electro-mechanical coupling on the conduction band is demonstrated in Figure 4.17. For a closed or nearly closed channel, i.e.  $V_G \approx V_T$ , the region that affects the operation of the device is under the gate. This region determines the value of  $V_T$  ( $V_G$  at

which the channel closes). At high  $V_D$ , the largest CB shift due to piezoelectric coupling appears at the drain edge of the gate. But this is already behind the potential barrier, and the electrons, if there were any, will be accelerated towards the drain anyway. Therefore, the CB shift in this region plays no role. However, under the gate, the CB shift is similar to the conditions at low  $V_D$ . At that point, where the potential barrier along the channel is the highest, the CB shift at  $V_D = 20$ V is approximately equal to 0.14 eV while, at  $V_D = 3$ V, it is 0.13 eV. Hence, the resulting  $V_T$  shift is virtually the same for all voltages. The shift at the low drain voltage ( $V_D = 3$ V) and when the channel is open channel ( $V_G = 0$ V) was virtually zero, which resulted in no change in the drain current.

### 4.5 Summary

The effect of the electric field induced strain on the I-V characteristics at conditions considered in this chapter is not dramatic. At higher voltages, the strain induced by the converse piezoelectric effect may lead to defect formation. The main purpose of this chapter is to illustrate a self-consistent approach to couple the electric field with the space charge as advancement to the previous approach that does not take the converse effect into account.

We have demonstrated a self-consistent methodology to include the link between electric field, strain, polarization, and bound charge, which will affect the calculation of carrier distribution in the device. To the best of our knowledge, such self-consistent simulation of the impact of field induced polarization on the field distribution and current in contemporary AlGaN/GaN HEMT is reported here for the first time. The simulations show that the additional induced charge does not induce significant changes in I-V characteristics of the device. However, if the converse piezoelectric strain is large enough to cause the defect generation, this could result in device degradation [29], which will be investigated in Chapter 5.

# 5 Current Collapse and Device Degradation

### 5.1 Introduction

Current collapse and device degradation in GaN HEMTs associated with charge movement and trapping in the device present a serious reliability problem. Current collapse has been analysed previously using numerical simulations [97], and was explained in the context of a 'virtual gate' [116,34], associated with additional charge trapping at the interface or in the bulk regions of the transistors. The proposed explanation of the device degradation mechanism [29] is that it occurs due to creating lattice defects by excessive mechanical stress caused by converse piezoelectric effect in the regions with high electric field. These defects act as traps. In this chapter, we aim to find the surface or volume charge distribution that would reproduce the I-V characteristics during the current collapse and the I-V characteristics of a degraded device after a high voltage stress test run for 12.5 hours.

In section 5.2 we explain the operation mode (measurement technique), at which the current collapse phenomenon occurs. Then we report the results of our investigation of this phenomenon. First, we investigate the impact of the trapped charge on the I-V characteristics, by uniform slabs of charge, in section 5.3.1. Next, in section 5.4, we obtain exponential distributions on both sides of the gate on the device surface that provides a

reasonable fit to the experimental I-V measurements pulsed from a class AB point. In subsection 5.4.2 we explain the automated procedure to obtain the fitting.

In section 5.5 we identify areas of the device that undergo an excessive stress due to converse piezoelectric effect at high voltages and, by introducing trapped charge in those areas, attempt to reproduce I-V characteristics of a degraded device.

# 5.2 The Current Collapse and Device Degradation Phenomena

The current collapse and device degradation have similar impact on the I-V characteristics, both reduce the current flowing through the channel, especially in the knee region of the I-V plane. The main difference, as described in section 2.5.2, is that the current collapse is reversible and the degradation is not. The difference in the mechanism is that the current collapse is caused by trapping of the electrons in existing traps while the device degradation is caused by creating new defects and hence new traps in the device, on which charge is permanently trapped.

During a pulsed measurement, the device is pulsed to a measurement voltage ( $V_G$  and  $V_D$ ) for time  $t_m$ . In between the pulses, the device is held at a quiescent bias (at a gate voltage  $V_{G,q}$ , and drain voltage  $V_{D,q}$ ) for time  $t_q$ . This is repeated for how many  $V_G$ - $V_D$ combinations the current is measured.  $t_q$  is typically several orders of magnitude larger than  $t_m$ . The pulsed I-V characteristics of a device depends not only on the actual measurement voltage V, but on the quiescent bias  $V_q$ , too. If the quiescent bias is zero volts on both the gate and the drain electrodes,  $V_{G,q} = 0$ V and  $V_{D,q} = 0$ V, it is called the openchannel condition. At a different quiescent bias, the current during the pulse will change. This change in the pulsed-current is referred to as the current collapse that causes the DC-RF dispersion and is illustrated in Figure 5.1. This effect is caused by electron leakage mainly to the surface and also to the bulk of the device in between the pulses, as shown in Figure 5.2, at  $V_q$ .





Figure 5.1: c) An illustration of the dependence of the measured current on the quiescent bias at which the device is hold before the actual measurement. The real a)  $I_D$ - $V_G$  and b)  $I_D$ - $V_D$  characteristics for two different quiescent bias voltages. The term open-channel refers to the quiescent bias of  $V_{G,q} = 0V$ ,  $V_{D,q} = 0V$ ; whereas the measurement that showed the current collapse to  $V_{G,q} = -4V$ ,  $V_{D,q} = 25V$ . The dots

represent the measurement point of  $V_G = 0V$ ,  $V_D = 5V$ , but the measured current depends on the quiescent bias, a bias applied before the measurement. This phenomenon is referred to as DC-RF dispersion or "knee-walkout" due to its representation in the I-V plane (blue arrow), as mentioned in section 2.5.2. The I-V characteristics for a degraded device in the open-channel condition is shown in blue lines.

During the stress test, a device is subjected to high electric field which, via the converse piezoelectric effect, discussed in 4.2 and described by equations (4.1) and (4.4), induces strong mechanical stress in the region of the device with high E, which in turn leads to additional strain of the material, given by equation (4.3). According to [29] this leads to defects in the semiconductors' lattice structure and therefore to creation of new traps.

In our calibration, we have used three sets of experimental data, shown in Figure 5.1. I-V characteristics pulsed from an open-channel condition – this was used to calibrate the device, and from the quiescent bias of  $V_{G,q} = -4V$ , and  $V_{D,q} = 25V$  – this was used to calibrate the pulsed I-V characteristics to find a surface electron distribution that would reproduce the measured current collapse data. The measurement time was  $t_m = 1\mu$ s, and the time between the pulses was  $t_q = 1$ ms. In Chapter 6, this distribution was used to simulate the actual leakage mechanism. Finally, I-V measurement pulsed from an open-channel condition after the device was stressed and therefore degraded by high electric field. The device was degraded during RF power test at  $V_G = -2.7V$ ,  $V_D = 25V$  for 12.5 hours, in

which the RF output power dropped to 2W/mm at 2.8GHz from the initial 4W/mm [115]. In our simulations, we have identified the region where, due to the high electric field, a high stress is expected. Assuming that new traps will be created in this region, we attempted to reproduce the post-degradation measurement by putting charge with a corresponding distribution in this region.



Figure 5.2: The mechanism responsible for the current collapse. Due to the strong electric field (red arrow), through the means of the Poole-Frenkel conduction (green arrow), the electrons leak to the surface of the device and electrostatically deplete the channel (blue arrow) and hence cause reduction of the saturation current. This is the primary Poole-Frenkel mechanism. The secondary mechanism is that the electrons at the surface create additional electric field which forces the later leaked electrons to transfer to the traps in the bulk and to the AlGaN/GaN interface. During a stress test, in the region of the high electric field (red arrow), new dislocations, and therefore traps, are created. This leads to a permanently degraded device and reduced current in subsequent measurements. Adapted from [125]

# 5.3 Investigation of the Impact of the Surface Electron Distribution

When the current collapse/knee walkout or degradation is apparent (Figure 5.1 b), the  $I_D$ - $V_D$  slope in the knee region decreases, whereby indicating an increase in the differential access resistance. The saturated current is also reduced. A threshold voltage shift present in the  $I_D$ - $V_G$  characteristics of the current collapse measurement, unlike that of a degraded device, as shown in Figure 5.1 a), indicated the presence of charge trapped under the gate in addition to that on the ungated surface. Figure 5.3 shows three regions of the device, where the trapped charge was placed to capture the current collapse phenomenon. To reproduce the experimental current collapse and degradation in the simulation, we studied the impact of various distributions of trapped charge at the surface of the device.



Figure 5.3: A scheme of the device with focus on the regions (red lines) with the trapped charge to reproduce the pulsed measurements of the I-V characteristics from the class AB point.

# 5.3.1 Uniform Slabs of Charge: Symmetric and Asymmetric Charge Distributions



Figure 5.4: Schematic representation of charge distributions used in simulations investigating the impact of uniform slabs. The red letter 'G' represents the position of the gate, each shade of grey represents different simulation. The corresponding simulated I-V characteristics are shown (a) in Figure 5.5, (b) in Figure 5.7, (c) in Figure 5.6 and (d) in Figure 5.8.

All figures in this section showing simulation results of I-V characteristics also show the measurements pulsed from an open-channel condition and those showing the current collapse effect. However, the insights in terms of the impact of the trapped charge on the I-V characteristics gained here are valid also for the calibration of the device degradation. The position and the concentration of the trapped charge and its impact on the I-V characteristics have been studied, as reported in [126]. In this section, all reported I<sub>D</sub>-V<sub>D</sub> and I<sub>D</sub>-V<sub>G</sub> experimental data and simulations were measured or performed at V<sub>G</sub> = 0V and V<sub>D</sub> = 3V, respectively. Another important figure of merit in the analysis of a device is transconductance  $g_m$ , which indicates the amount of control the gate voltage has on the drain current. It is defined as the ratio of the current change at the output port to the voltage change at the input port, i.e.,  $g_m = (\partial I_D / \partial V_G)_{V_D}$ . As a function of  $V_G$ ,  $g_m$  has a hat-shaped

dependence, shown in Figure 3.13 c), which rises sharply around  $V_T$ , then reaches a plateau and falls moderately before  $I_D$  saturates. In the following we illustrate the impact of the surface charge upon this parameter.





Figure 5.5: (a)  $I_D$ - $V_G$  and (b)  $I_D$ - $V_D$  characteristics for different values of surface electron density, 1- $3 \times 10^{13}$  cm<sup>-2</sup>, placed at the edges of the gate, in a region extending 50nm towards the other electric contacts. Increasing the amount of charge leads to reduction of the saturation current, but the slope of the linear regime of  $I_D$ - $V_D$  remains unchanged. (c) The impact of the surface charge on the transconductance of the device, the black line represents the device with no trapped charge.

Initial simulations used rectangular charge slabs [97], which were placed on the source and drain sides of the gate and varied in length and charge density. First, we assume symmetrical charge distribution on both sides of the gate. The dimensions and charge density of the slabs are schematically illustrated in Figure 5.4. The impact of changing the surface electron density  $(1-3\times10^{13}$ cm<sup>-2</sup>) in a region of a constant size, 50nm from the gate towards the other two electric contacts, is investigated in Figure 5.5. The impact of the length (30-70 nm) of the region at a constant surface electron density,  $2\times10^{13}$ cm<sup>-2</sup>, is investigated in Figure 5.7. In both cases, increasing the total amount of charge reduces the saturation current, but fails to increase the access resistance and hence change the slope of the linear region, necessary to fit the experimental I<sub>D</sub>-V<sub>D</sub> characteristics.

Figure 5.6 compares a)  $I_D$ - $V_G$  and b)  $I_D$ - $V_D$  characteristics for charge extending 50 nm and 150 nm away from the gate. Charge close to the gate shifts the threshold voltage, while charge that extends further away from the gate reduces the ON-current. With increasing the region where the charge is trapped, the saturation  $I_D$  increases less with increasing  $V_D$ , yet the impact on linear region of  $I_D$ - $V_G$  is lowered.



If the region of the trapped charge is relatively small and the charge density is high, as will be demonstrated in Figure 5.10 c), the decline of  $g_m$  happens over wider range of  $V_G$  than without the trapped charge. The value of  $V_G$  at which  $g_m$  in the simulation with and without the trapped charge cross, is determined mainly by the length of the region, as is clearly demonstrated in Figure 5.6 c), for 150nm length of the region. This nearly holds for 50nm as well, shown in Figure 5.5 c), although here the cross-point shifts slightly and  $V_T$  is affected significantly with varying the surface charge density. The impact of varying the length of the region while keeping the surface charge density constant, shown in Figure 5.7, is similar to varying the charge density, but here the cross-point shifts clearly and significantly.

c)



The impact of charge trapped at the AlGaN/GaN interface under the gate is investigated in Figure 5.8. This charge partly neutralises the bound charge under the gate at the AlGaN/GaN interface originating from the difference in polarization between the two materials, as explained in subsection 2.3.3. The impact of this charge on the conduction band is illustrated in Figure 2.6. This charge hence directly depletes the 2DEG under the gate and shifts the threshold voltage,  $V_T$ .



Figure 5.8: The sole effect of charge trapped at the AlGaN/GaN interface under the gate is the threshold voltage,  $V_T$ , shift. The slope and the ON-current remain unchanged. Apart from the varying charge under the gate, there was sheet charge density of  $6.5 \times 10^{12}$  cm<sup>-2</sup> extending to 150 nm on both sides of the gate, reported in Figure 5.6.

Further on, we investigate the impact of the charge on the drain and source sides of the gate on I<sub>D</sub>-V<sub>G</sub> and I<sub>D</sub>-V<sub>D</sub> characteristics, for two regions of trapped charge of different extent. In Figure 5.9 we have used much larger region and lower charge density of the trapped charge than previously, 1µm on both sides of the gate, and in Figure 5.10 we have used a previously reported region of 50nm and the sheet charge density  $2 \times 10^{13}$  cm<sup>-2</sup> (green line in Figure 5.5 and Figure 5.7). The 1µm region of the trapped charge, shown in Figure 5.9, was enough to change the access resistance, as seen from the changed slope of I<sub>D</sub>-V<sub>D</sub> characteristics. From the I<sub>D</sub>-V<sub>G</sub> graph it becomes clear that both areas have the same effect on the ON-current, while only the charge on the source side changes the slope in the linear regime. Therefore, this suggests that, to achieve the change in the slope seen in the experimental data, we need to include the trapped surface charge at the source side. For drain voltages of up to  $V_D = 4V$ , the charge in both areas has the same effect on the linear regime. For higher drain voltages, the current is limited by the charge on the source side. In the I<sub>D</sub>-V<sub>D</sub> characteristics, the charge at the source side saturates current at lower V<sub>D</sub>, whereas the experimental data show continuous increase in the current as in the case when charge on the drain side is included. From this fact, we conclude that, to reproduce the experimental slow increase in the saturation current, the trapped charge needs to be mainly on the drain side of the gate.





Figure 5.9: Asymmetric charge distribution around the gate. The impact of the trapped charge at the source and drain sides of the gate is investigated separately, for *low* charge density in a *large* region. (a)  $I_D-V_G$  and (b)  $I_D-V_D$  characteristics and (c) transconductance are compared.

The impact of charge trapped on either side of the gate on the  $g_m$ -V<sub>G</sub> dependence is most clearly demonstrated using moderate surface charge density in a large region, shown in Figure 5.9 c). The charge on the source side lowers the plateau of the hat-shaped dependence which translates to change of the I<sub>D</sub>-V<sub>G</sub> slope in the linear region. The charge on the drain side shifts  $I_D$  saturation to lower values of  $V_G$ . Charge on both sides combines these effects.

For higher surface charge densities in a smaller region, the effects become more complex, as shown in Figure 5.10 c). To the aforementioned effects of the charge one must add the following. On the source side, it is  $V_T$  shift to higher values of  $V_G$  and reduced rate of decline of  $g_m$  in the region before saturation, hence shifting the saturation to higher values of  $V_G$ . On the drain side, it is blurring the transition from linear region to saturation, i.e.  $g_m$  starts to fall at lower values of  $V_G$ , but the decline continues to higher values of  $V_G$  than without the trapped charge.





Figure 5.10: Asymmetric charge distribution around the gate. The impact of the trapped charge at the source and drain sides of the gate is investigated separately, for *high* charge density in a *small* region. (a)  $I_D-V_G$  and (b)  $I_D-V_D$  characteristics and (c) transconductance are compared.

The best achieved fit of the pulsed I-V measurement, using uniform slabs of charge, is shown in Figure 5.11. The charge density used in this simulation was asymmetrical, with  $3 \times 10^{12}$  cm<sup>-2</sup> on the drain side and  $2.5 \times 10^{12}$  cm<sup>-2</sup> on the source side of the gate, with

additional charge of  $1 \times 10^{12}$  cm<sup>-2</sup> under the gate that provided for a threshold voltage shift. The charge on the surface stretched 1µm away from the gate. The blue ellipse in the figure shows the region of I-V characteristics, where, for various examined combinations of charge blocks on both sides of the gate and underneath it, the simulation results were invariably divorced from the experimental results.

Examining the shape of the measured  $I_D$ -V<sub>G</sub> characteristic suggested that there was trapped charge on both the source and drain sides of the gate, with most of the charge on the drain side. However, using uniform slabs of charge, a good fit to the experimental data was not possible. These simulations indicated that to capture the current collapse behaviour, high charge density close to the gate has to be present, whilst a low charge extended to considerable distance away from the gate. This observation is consistent with the charge distribution implied by the Poole-Frenkel transport mechanism observed in [97,127] and modelled in [128].



Figure 5.11: The best fit of pulsed I-V characteristics using uniform blocks of trapped charge placed asymmetrically around the gate. While achieving reasonable fit of  $I_D$ - $V_D$ , as well as  $V_T$ , and ON-current, the transition between the linear regime and the ON-current in  $I_D$ - $V_G$  (blue ellipse) remained problematic. This appeared for all simulated values of  $V_D$ , from 1V to 10V (not reported here).

# 5.4 Current Collapse Calibration: Exponential Charge Distribution

#### 5.4.1 The Model



Figure 5.12: a) Schematic illustration of the exponential charge distribution model, which, via the parameters A, B and  $\lambda$ , allows for independent control of the sheet charge density at the gate edge  $Q_S(0)$ , on the front of the distribution  $Q_S(d)$  and the total charge  $Q_L$  trapped at the surface on either side of the gate. The method of calculation of the parameters A, B and  $\lambda$  is described in the next subsection, 5.4.2, and given by equations (5.3) and (5.4). b) Schematic illustration of the arrangement of the charge distribution in the device. Exponential distribution on the source and drain sides of the gate and a constant sheet charge density under the gate.

Results reported in this section are reported in [129]. Previous modelling efforts [128] assumed a triangular charge distribution at the gate edge. For a more accurate modelling, we have assumed here an empirical exponential function

(5.1) 
$$Q_S(x) = A \exp(-\lambda x) + B,$$

for the surface charge distribution on both sides of the gate, where *A*, *B* and  $\lambda$  are fitting parameters, which allowed to set the charge close to the gate,  $Q_S(0)$ , very far from the gate,  $Q_S(d)$ , and the total charge on each side independently,  $Q_L$ , as shown in Figure 5.12 a). Additionally, a constant charge density under the gate on the AlGaN/GaN interface was assumed, as indicated in Figure 5.3.

### 5.4.2 The Procedure

In order to find the trapped charge distribution that would yield the best fit to the experimental data using the above described model, we need to find the parameters A, B

and  $\lambda$ , and the distance *d* to which the charge extended, for both sides of the gate, and the value of the charge density under the gate  $Q_{S,G}$ , which, in total, results in nine parameters to fit. To reduce the complexity of the problem, *d* was limited to  $d_D = 1\mu m$  on the drain side and  $d_S = 0.5\mu m$  on the source side, since previous simulations have suggested that there is larger charge on the drain side. These values were consistent with [71], where it has been shown, that the electrons can migrate up to  $1\mu m$  away from the gate. This reduces the number of fitting parameters to seven. This arrangement is schematically illustrated in Figure 5.12 b). The equation (5.1) allows us to calculate  $Q_S$  in a specific distance *x* from the gate but, we need to control the variables Q(0), Q(d) and  $Q_L$  and calculate the fitting parameters from these variables. First, from (5.1), we express the variables as

(5.2) a) 
$$Q_S(0) = A + B$$

b) 
$$Q_S(d) = A \exp(-\lambda d) + B$$

c) 
$$Q_L = \int_0^d Q_S(x) dx = \frac{A}{\lambda} \left( 1 - exp(-\lambda d) \right) + Bd$$

Now we need to express the parameters. First, we substitute (5.2) b) and then a) into c) and rearrange the formula, to get  $\lambda$ , in equation (5.3) a). Then we substitute (5.2) a) into b) and get the parameter *A*, in (5.3) b). Finally, rearranging (5.2) a) we get the parameter *B*, in (5.3) c).

(5.3) a) 
$$\lambda = \frac{Q_S(0) - Q_S(d)}{Q_L - Bd}$$

b) 
$$A = \frac{Q_S(d) - Q_S(0)}{(exp(-\lambda d) - 1)}$$

c) 
$$B = Q_S(0) - A$$

The obvious problem with this set of equations is that, to get A and B, we need to know  $\lambda$ and, to calculate  $\lambda$ , we need to know B (or A). To solve this problem, we make a preliminary assumption that, because the charge density drops down quickly as we move away from the gate,  $B \approx Q_S(d)$ . We use this relationship to estimate the initial value of the parameter  $\lambda$  and label it  $\lambda_0$ ,

(5.4) 
$$\lambda_0 = \frac{Q_S(0) - Q_S(d)}{Q_L - Q_S(d)d}$$

From this value we calculate *A* and then *B* and again  $\lambda$ . Then we update the value of  $\lambda$  until the initial and final value is, within predetermined error, the same, i.e.,  $|\lambda - \lambda_0| < error$ .

The actual procedure of fitting the distribution parameters was as follows:

- Based on the insights gained from performing the simulations with uniform slabs of charge in section 5.3.1, create a list of values p<sub>i,j</sub> for all seven fitting parameters, where p<sub>i</sub> is a parameter, i = 1..7 and j = 1..N<sub>i</sub>, N<sub>i</sub> is the number of values of the parameter p<sub>i</sub> in the list. The number of combinations is N = ∏<sup>7</sup><sub>i=1</sub>N<sub>i</sub>.
- 2. Read the grid file (produced by *SSE* (3.1.2) and read by *SD* (0)) to find out the sequence of mesh points in the file, which is the same sequence as the one used in the file specifying the doping (*the doping file*) in the device.
- 3. Select a previously unselected combination of the parameters.
- 4. Calculate respective parameters A, B and  $\lambda$  used in the exponential charge distribution model, using equations (5.3) and (5.4) and the procedure described above.
- 5. Using equation (5.1), calculate  $Q_S$  (and convert to charge concentration) for the appropriate mesh points, defined as

Drain side:	$x \ge x_{G,D}$	and	$x \leq x_{G,D} + d_D,$	$y = y_{surface}$
Source side:	$x \ge x_{G,S} - d_S$	and	$x \leq x_{G,S},$	$y = y_{surface}$
Under the gate:	$x \ge x_{G,S}$	and	$x \leq x_{G,D},$	$y = y_{interface}$

- 6. Rewrite the appropriate mesh points in the doping file with the calculated values.
- 7. Using the calculated charge, run  $I_D$ - $V_G$  simulation at  $V_D = 3V$  and  $I_D$ - $V_D$  at  $V_G = 0V$ .

- 8. Have all combinations of the values of the parameters been selected? If yes, continue. If not, go back to step 3.
- 9. List through all N results (I<sub>D</sub>-V<sub>G</sub> and I<sub>D</sub>-V<sub>D</sub> characteristics) and for each do the following steps.
- 10. Linearly interpolate the I-V simulations to the values of V at which the current was measured. E.g., we may have the value of  $I_m$  at  $V_m$  from the measurement, yet  $I_{s1}$  at  $V_{s1} < V_m$  and  $I_{s2}$  at  $V_{s2} > V_m$  from the simulation. In that case, calculate  $I_s$  at  $V_m$  as  $I_s = \frac{V_m V_{s1}}{V_{s2} V_{s1}} (I_{s2} I_{s1}) + I_{s1}$ . Do this for values of I at all measured values of V.
- 11. Assign the value deviation  $\mathcal{D} = \sum_{k=1}^{2} \frac{1}{n_k} \sum_{l=1}^{n_k} (I_{s,l} I_{m,l})^2$  to each of N combinations of parameters and their respective simulated I-V characteristics. *k* lists through all I-V curves (in our case two, one I<sub>D</sub>-V<sub>D</sub> and one I<sub>D</sub>-V<sub>G</sub>), n<sub>k</sub> is the number of measured points of k-th I-V characteristics, *l* lists all values of I at the measured values of V of a particular I-V characteristics and I<sub>s</sub> and I<sub>m</sub> are the simulated and measured current at the same V. In the following text, good/bad results will mean low/high deviation as defined here.
- 12. Choose the charge distribution with the lowest deviation  $\mathcal{D}$  as the one that fits the experimental data best.

Table 5.1: List of values of the parameters used in the calibration of the exponential charge model. The top table represents the first set of values, combinations of which were simulated. Based on the results from these simulations, some values were swapped for new ones, shown in the bottom table. The new values are printed in bold.  $Q_S$  (cm<sup>-2</sup>) is sheet charge and  $Q_L$  (cm<sup>-1</sup>) is total charge of the distribution.

parameter	Drain Side ( $d_D = 1 \mu m$ )			Source	Gate		
	$Q_{s}(0)$	$Q_{S}(d_{D})$	$Q_L$	$Q_{S}(0)$	$Q_{S}(d_{S})$	$Q_L$	Qs
es	2×10 <sup>13</sup>	$2.0 \times 10^{12}$	5.0×10 <sup>8</sup>	$0.6 \times 10^{13}$	$1.0 \times 10^{12}$	$1.1 \times 10^{8}$	0
of valu	3×10 <sup>13</sup>	$3.0 \times 10^{12}$	6.0×10 <sup>8</sup>	$1.0 \times 10^{13}$	$1.5 \times 10^{12}$	$1.3 \times 10^{8}$	$0.4 \times 10^{12}$
	5×10 <sup>13</sup>	$4.0 \times 10^{12}$	$7.0 \times 10^{8}$	$1.5 \times 10^{13}$	$2.0 \times 10^{12}$	$1.5 \times 10^{8}$	$0.8 \times 10^{12}$
list							$1.2 \times 10^{12}$

n o no no oto n	Drain Side ( $d_D = 1 \mu m$ )			Source Side ( $d_S = 0.5 \mu m$ )			Gate
parameter	$Q_{S}(0)$	$Q_{S}(d_{D})$	QL	$Q_{s}(0)$	$Q_{S}(d_{S})$	$Q_{L}$	Qs
of values	2×10 <sup>13</sup>	2.0×10 <sup>12</sup>	3.5×10 <sup>8</sup>	0.6×10 <sup>13</sup>	0.6×10 <sup>12</sup>	0.6×10 <sup>8</sup>	0
	3×10 <sup>13</sup>	2.5×10 <sup>12</sup>	4.0×10 <sup>8</sup>	1.0×10 <sup>13</sup>	0.8×10 <sup>12</sup>	0.9×10 <sup>8</sup>	$0.4 \times 10^{12}$
	5×10 <sup>13</sup>	$3.0 \times 10^{12}$	4.5×10 <sup>8</sup>	$1.5 \times 10^{13}$	$1.0 \times 10^{12}$	1.2×10 <sup>8</sup>	$0.8 \times 10^{12}$
list e							$1.2 \times 10^{12}$

The values used for the parameters mentioned in step 1 are listed in Table 5.1. Two sets of simulations were performed. After the first run, the values that yielded the worst results were dropped and substituted with new ones, printed in bold in the table. The values that gave the best results from the second run of the simulations, which were better than the results from the first run, are reported in the next subsection, 5.4.3.

#### 5.4.3 The Result





Figure 5.13: a)  $I_D$ - $V_G$  and b)  $I_D$ - $V_D$  calibration of current collapse measurement, from class AB point, at  $V_D = 3V$  and at  $V_G = 0V$ , respectively. Subfigure c) shows the impact of the surface trapped charge on transconductance, where the simulations without and with the current collapse are represented by thin and thick lines, respectively. The colours are consistent with a). Figure 5.14 shows the corresponding surface electron distributions at the source and drain sides of the gate.



Figure 5.14: The surface charge distribution obtained by calibrating the pulsed I-V characteristics, shown in Figure 5.13. The parameters of these distributions are summarized in Table 5.2.

The best fit to the  $I_D$ - $V_D$  and  $I_D$ - $V_G$  measurement achieved at the class AB operating point is shown in Figure 5.13 left and right, respectively. The exponential distribution on both sides of the gate for the best fit is shown in Figure 5.14 with the parameters given in Table 5.2. Total charge on the drain side is more than five times higher than that on the source side. The obtained distribution is consistent with the understanding that the current collapse is due to charge injection from the gate corners and migration of the injected charge away from the gate due to Poole-Frenkel emission mechanism. Space charge effects in interplay with the trap activation energy and the corresponding 'hopping mobility' determine the lateral distribution of the injected charge.

Table 5.2: Parameters of the exponential distribution that yielded the best agreement with experimental data, as shown in Figure 5.13.  $Q_S$  (cm<sup>-2</sup>) is sheet charge and  $Q_L$  (cm<sup>-1</sup>) is total charge of the distribution at the specified side of the gate. The surface electron distributions are visualized in Figure 5.14.

Position:	Drain Side ( $d_D = 1 \mu m$ )			Source Side ( $d_S = 0.5 \mu m$ )			Gate
sheet	$Q_{S}(0)$	$\mathbf{Q}_{\mathbf{S}}\left(d_{D}\right)$	QL	Q <sub>S</sub> (gate)	$Q_{S}(d_{S})$	QL	Qs
charge	5×10 <sup>13</sup>	$2.5 \times 10^{12}$	$3.5 \times 10^{8}$	$1.5 \times 10^{13}$	6×10 <sup>11</sup>	6×10 <sup>7</sup>	$1.2 \times 10^{12}$
fitting	A (cm <sup>-2</sup> )	$B(cm^{-2})$	$\lambda$ (cm <sup>-1</sup> )	A (cm <sup>-2</sup> )	$B (cm^{-2})$	$\lambda$ (cm <sup>-1</sup> )	
parameters	4.75×10 <sup>13</sup>	$2.5 \times 10^{12}$	$4.75 \times 10^{8}$	$1.44 \times 10^{13}$	6×10 <sup>11</sup>	$4.8 \times 10^{5}$	

### 5.4.4 Accuracy

The accuracy of the calibration of the device I-V characteristics in the absence of current collapse is discussed in section 3.4.3.3. Here we discuss the accuracy in the presence of current collapse. In the first case, the calibration parameters are physical parameters with known impact on the characteristics. Moreover, the range of possible values of these parameters is known from literature. In the latter case, on the other hand, the calibration parameter is the surface charge distribution, which, in principle, can be any function. We have simplified the scale of this problem by making some assumptions about the distribution, discussed in section 5.4.1, which made the calibration possible but in that we have potentially sacrificed high accuracy of the simulated I-V characteristics. Therefore, in the presence of the current collapse, one cannot expect to achieve the same accuracy as in its absence.



Figure 5.15: a) The simulated  $I_D$ -V characteristics during the current collapse (Figure 5.13 a) and b) combined). The error of the calibration with respect to the measured characteristics (squares in Figure 5.13)

(b) as a function of both  $V_D$  and  $V_G$  and separately, as a function of (c)  $V_G$  and (d)  $V_D$ .

Figure 5.15 shows the error of the collapsed drain current calibration. For the reported values, the error is contained within 15%, with the majority of points being within 5%. Subfigure c) reveals that the calibration is best for  $V_G$  of -2 and -1V and subfigure d) reveals systematic error that at lower drain voltage ( $V_D < 4V$ ) the drain current tends to be overestimated while at higher drain voltage ( $V_D > 6V$ ) tends to be underestimated. Performing further simulations using an optimisation procedure would most probably yield more accurate calibration, but these results are sufficient to show that using asymmetrical exponential surface charge distribution can lead to accurate description of the current collapse phenomenon.

### 5.5 Device Degradation

In this section, we attempt to calibrate I-V characteristics of a device that, as mentioned in section 5.2, was degraded during RF power test at  $V_G = -2.7V$ ,  $V_D = 25V$  for 12.5 hours. Initially, we perform a simulation of a device at the above mentioned bias to identify regions with high electric field and quantify the stresses that these regions undergo, using equation (4.4). This equation comes from the clamped model, discussed in section 4.2.1. This model is only an approximation of the strains and stresses that are introduced by the electric field in the device via the converse piezoelectric effect for reasons discussed in that section. Therefore, the calculated lateral stresses and vertical strains should be considered only as guidance to identify the regions and relatively quantify the likelihood that the dislocations will be created. Figure 5.16 shows the lateral stress in the AlGaN barrier of the device. The highest stresses are located under the drain edge of the gate. This is consistent with [130], where it was shown that high reverse bias results in the formation of defects located at the edge of the gate contact [22]. A local maximum is also at the source edge of the gate, albeit the stresses here are more moderate. We have used two models to translate this estimated stress to trapped charge density in the device. A constant charge density model and linear dependence model, both with two parameters. The two models can be formally defined as



Figure 5.16: The lateral stress  $\sigma_x$  in the device at  $V_G = -4V$  and  $V_D = 25V$  as calculated from (4.4) within the clamped model. The bottom subfigure offers a few cross-sections of the parameter. The value *y* in the top subfigure indicates the distance from the interface while in the bottom subfigure it indicates the distance from the surface. The gate is indicated as a pink line in the top subfigure and by the vertical lines in the bottom subfigure.

Constant charge density model:

$$\rho_i = 0; \ \sigma_i < \sigma_0$$

 $\rho_i = \rho_0; \ \sigma_i \ge \sigma_0$ 

Linear dependence model:

$$= \rho_0' \times (\sigma_i - \sigma_0); \ \sigma_i \ge \sigma_0$$

$$ho_i = 0; \ \sigma_i < \sigma_0$$

 $\rho_i$ 

The index *i* stands for an arbitrary mesh point of the device in the simulator. In both models,  $\sigma_0$  defines the threshold stress, under which no charge is introduced at that mesh point. In the constant charge density model, the parameter  $\rho_0$  defines the charge density in all mesh points, where the stress exceeds the threshold value. In the linear dependence model, the parameter  $\rho_0'$  determines the increase rate of the trapped charge density as a linear function of the lateral stress.



Figure 5.17: I-V simulations using the constant charge density model. The impact of the varying charge density  $\rho_0$  was investigated, while the threshold stress  $\sigma_0$  was kept constant.



Figure 5.18: I-V characteristics for various values of the threshold stress and trapped charge density. The third value in the legend is the total charge introduced in the device in each particular simulation.

From Figure 5.1 it is obvious that there was no  $V_T$  shift after the device was degraded by the stress test. From the simulations performed in the section 5.3 we know that  $V_T$  shift is caused by the charge trapped under the gate. When we combine these two pieces of information, we can conclude that in calibrating the device degradation measurements we need to avoid putting too much charge under the gate. Taking into account the 2D graph of the lateral stress in the device in Figure 5.16, this gives us a lower estimate of the threshold stress  $\sigma_0$  to be used in the calibration as 3.26GPa, preferably higher. We have to note here that the maximum lateral stress in the device under the simulated bias conditions, which is right under the drain edge of the gate, 3.51GPa, is only 11% higher than the lateral stress coming from the lattice mismatch between  $Al_xGa_{1-x}N$  and GaN for x = 0.28, 3.15GPa. The highest stress here corresponds to the in-grown stress in the AlGaN layer for x = 0.31. If it was the simple lateral stress that caused the defect formation and the following device degradation, then a HEMT employing the  $Al_{0.31}Ga_{0.69}N/GaN$  heterostructure would be degraded even without any stress test. This clearly is not the case. It is more probable that what causes the defects are shear stresses and strains produced by the strong gradient of the stress field. Therefore, the normal stress that is calculated by (4.4) and reported in Figure 5.16 is taken only as a proxy to determine the region where the most defects will be formed.



Figure 5.19: Simulated I-V characteristics using the linear dependence model for various values of the parameters. Note that the total charge introduced in the device in the *blue* simulation is lower than in the *green* simulation, yet the impact on the reduction of the drain current is stronger. Due to higher threshold value, the region where the charge is introduced is smaller.

The measured I-V characteristics in this section, both before and after degradation, were pulsed from an open-channel. The data labelled as *fresh* are the same as those labelled *open-channel* in sections 5.3 and 5.4. Simulation results using the constant charge density model are presented in Figure 5.17 and Figure 5.18. Figure 5.19 shows simulation results using the linear dependence model. By using the lateral stress as a proxy to identify the region where new traps are formed, it was unavoidable to introduce large density of charge in the vicinity of the gate. Consistently with the investigation in section 5.3, such a charge reduces the transconductance for  $V_G$  just above  $V_T$ . Since this is not what we see in the experimental measurements of  $I_D$ -V<sub>G</sub> characteristics of a degraded device, this effect prevented us to find such parameters as to calibrate the measurements successfully. Therefore we conclude that to reproduce the I-V characteristics of a degraded device it is not sufficient to identify a region with high stress using the clamped model and to introduce trapped charge in that region. The newly formed traps may form a gateway for the electrons, an easier path to tunnel form the gate, to other, pre-existing traps.

### 5.6 Summary

We have investigated the impact of various distributions of charge trapped in an AlGaN/GaN HEMT on the I-V characteristics and compared the simulation to experimentally measured data which show moderate current collapse. We have found that in order to reproduce the current collapse measurements it is necessary to introduce trapped charge in the simulations on both sides of the gate, which is consistent with [131]. In order to achieve the threshold voltage shift observed in the experimental data, interface charge at the GaN/AlGaN interface under the gate, representing the bulk trapping, needs to be included.

Using the insights gained in this investigation, we have calibrated the measured I-V characteristics with a manifested current collapse phenomenon (Figure 5.13). The trapped charge distribution was found to be asymmetrical, with the majority of the charge residing on the drain side, and non-uniform, with highest surface charge concentration close to the gate while a comparably lower charge density extended out several gate lengths away from the gate (Figure 5.14) in agreement with [128].

The estimated exponential shape of the surface charge proved to be sufficiently general to reproduce the experimental current collapse measurements. Good agreement between our simulation results and the experimental data was achieved, for a large range of simulated voltages. This good agreement lends strong support to the virtual gate model and suggests that non-linear transport of carriers injected from the gate via Poole-Frenkel emission [35] is likely to be the explanation for the current collapse. Using this distribution as an *ideal*, in Chapter 6 we will report on simulations of the electron leakage from the gate, by means of Poole-Frenkel emission, to find the parameters that would reproduce the mentioned distribution.

Using the clamped model and accounting for the converse piezoelectric effect, we have determined a region in the device that undergoes high lateral stress during high power tests at high voltages. We have used this information and introduced trapped charge into the region to capture I-V characteristics of a degraded device. Within the selected model, it proved impossible to fit the measurements.
# 6 Poole-Frenkel Electron Leakage Mechanism

## 6.1 Introduction

In the previous chapter we have investigated the current collapse phenomenon. Specifically, we attempted to reproduce the pulsed I-V characteristics using trapped electron distribution in the device. In section 5.4 we found an exponential distribution that reproduced the measured I-V characteristics reasonably well. In this chapter we examine to what extent the charge distribution obtained as a best fit in Chapter 5 can be reproduced by simulation of the electron leakage to the surface of a HEMT device. To perform the simulation of the electron leakage to the surface of the device, we need the following models (as a dependence on the local electric field):

- 1. electron emission from the gate (red line in Figure 6.1)
- 2. electron transport along the surface (blue arrows in in Figure 6.1)

We model the actual process of the electrons emitting from the gate, described in section 6.2, and "hopping" via surface trap states, described in section 6.3. In section 6.4 we list the steps of the simulation. In section 6.5 we aim to calibrate the electron emission and transport process that would lead to that distribution. In subsection 6.5.2.2 we compare the distributions obtained by simulating the electron transport with the exponential distribution found to reproduce the experimental I-V characteristics.



Figure 6.1: At high electric field E at the edge of the gate, electrons leak to the surface (red line). Then, due to the strong E, they are transported away from the gate (blue arrows).

## 6.2 Electron Emission from the Gate

For temperatures above 250K, the electron leakage from the gate, which is a Schottky contact, is described by **Frenkel-Poole emission model** [132]. In this model, the current density is given as

(6.1) 
$$J = CEexp\left[-\frac{q(\Phi_t - \sqrt{qE/\pi\varepsilon_0\varepsilon_s})}{kT}\right],$$

where *E* is the electric field at the metal-semiconductor interface, *q* is the elementary charge,  $\Phi_t$  is the barrier height for electron emission from the trap state,  $\varepsilon_s$  is the relative dielectric permittivity at high frequency, *T* is temperature,  $\varepsilon_0$  is the permittivity of free space, and *k* is the Boltzmann constant. The equation is later rearranged in the paper into a linear form

(6.2) 
$$\ln(J/E) = m\sqrt{E} + b,$$

where

$$m = \frac{q}{kT} \sqrt{\frac{q}{\pi \varepsilon_0 \varepsilon_s}},$$
 and  $b = -\frac{q\phi_t}{kT} + \ln C.$ 

The value of the parameter C isn't reported in the paper and cannot be recovered from the graphs. In the above equation, the current density has dimensions  $A.m^{-2}$  (electrons that

cross a unit surface per unit time). However, we are interested in electron transport at the surface and hence in the surface current density,  $j_{\sigma}$ , the dimension of which is A.m<sup>-1</sup> (electrons that cross a line of a unit length (the red line in Figure 6.1) per unit time). Therefore, we will use the equation (6.2) only as a guideline and consider *m* and *b* to be fitting parameters.

#### 6.2.1 The parameters *m* and *b*

Since we do not know what the proper values of m and b for surface leakage current are, we can tackle the problem from the other end. If we know, what surface current we expect at two specific values of the electric field, we can calculate m and b. From equation (6.2) we get

(6.3) 
$$m = \ln\left(\frac{j_2}{j_1}\frac{E_1}{E_2}\right) / (\sqrt{E_2} - \sqrt{E_1}), \text{ and}$$

(6.4) 
$$b = m\sqrt{E_i} + \ln(E_i/j_i),$$

where  $j_i$  is the surface current density at the electric field  $E_i$ . Figure 6.2 shows the electric field distribution at the surface of the device at a quiescent bias of  $V_{D,q} = 25$ V and  $V_{G,q} = -$ 4V. The electric field at the source and the drain edge of the gate is  $E_S = 0.84$  MV/cm, and  $E_D = 3.51$  MV/cm, respectively. To estimate the surface current density at both edges of the gate,  $j_S$  and  $j_D$ , we will use our exponential surface charge distribution calibration (Figure 5.14) of the pulsed I-V characteristics. As reported in Table 5.2, the total amount of the surface charge at the source and the drain side of the gate is  $Q_{L,S} = 6 \times 10^7 \text{ cm}^{-1}$ , and  $Q_{L,D} = 3.5 \times 10^8 \text{cm}^{-1}$ , respectively. The time between the pulses in this measurement was  $t_q = 1$ ms. This is the upper estimate of the leakage time,  $t_{leak}$ , it takes for the electrons to assume the final distribution. Thus, the average surface current densities throughout the time between measurements  $t_q$ , at the source and the drain edges, are  $\overline{J_S} = 6e^- \cdot \mu m^{-1} \cdot$  $\mu s^{-1}$ , and  $\overline{J_D} = 35e^- \cdot \mu m^{-1} \cdot \mu s^{-1}$ , respectively. As the electrons leak to the surface, the electric field at the gate edges is reduced and therefore the surface current densities are reduced as well. To achieve an average  $\overline{J_{\sigma}}$ , the electrons must start to leak with a higher initial surface current density  $j_{\sigma,0}$ , at the time of simulation t = 0. So, the reported estimates of the average  $j_{\sigma}$  are lower limits for the values used in the simulations. In principle, there are two possible scenarios to be considered. One is that  $j_{\sigma,0}$  is only slightly higher than  $j_{\sigma}$ and reducing slowly, which results in  $t_{leak}$  being close to  $t_q$ . The other is that  $j_{\sigma,0} \gg j_{\sigma}$ , resulting in most of the electrons being leaked in a short time,  $t_{leak} \ll t_q$ , and  $j_{\sigma}$  dropping dramatically thereafter with the electrons transporting and rearranging in the remaining time, until the measurement. Obviously, there is no clear distinction between these two scenarios and one naturally morphs to another. We will refer to these scenarios as *low*- and *high- density surface leakage current*.



Figure 6.2: The magnitude of the *x*-component of the electric field at the surface of a HEMT device with respect to the distance from the gate edge.



Figure 6.3: The dependence of the surface current density,  $j_{\infty}$  on the *x*-component of the electric field for various values of parameters *m* and *b*, calculated using equations (6.3) and (6.4). The values of *E* at the drain  $(E_D = 3.51 \text{ MV/cm})$  and source edge  $(E_S = 0.84 \text{ MV/cm})$  of the gate, at  $V_G = -4\text{V}$  and  $V_D = 25\text{V}$  in the simulated device, were taken for  $E_I$  and  $E_2$ . The value of  $j_D$  was set to  $45 \ e^- \cdot \mu m^{-1} \cdot \mu s^{-1}$  (solid lines) and  $30 \ e^- \cdot \mu m^{-1} \cdot \mu s^{-1}$  (dashed lines), the ratio  $j_D/j_S$  was set to 5 (blue), 10 (green), and 15 (red).

Finally, Figure 6.3 demonstrates the dependence of the surface current density  $j_{\sigma}$  on the electric field for various selected values of  $j_D$  and  $j_D/j_S$ . The graphs for higher  $j_D$  look the same, only with higher values on the *y*-axis.

# 6.3 Electron Transport

Electron transport along the surface by the means of thermionic emission frequency can be described by **Eyring's reaction rate model** [133]

(6.5) 
$$v = \frac{2kT}{h} exp\left(-\frac{\Delta G}{kT}\right) \sinh\left(\frac{qEs}{2kT}\right),$$

where v is the electron emission frequency, h is the Planck constant,  $\Delta G$  is the activation energy for the surface electron-hopping process and s is the spacing between the surface trap locations. The velocity v of an electron is then defined as

$$(6.6) v = s \times v$$

[128] estimate that  $\Delta G = 0.25 \sim 0.3$  eV and  $s = 0.1 \sim 0.3$  nm. Figure 6.4 and Figure 6.5 show the electron emission frequency and electron velocity, given by equations (6.5) and (6.6), for this range of values, respectively.

The above mentioned range of values of  $\Delta G$  and *s* translates to a wide range of electron velocities. In the linear region, the variation between the highest ( $\Delta G = 0.25 \text{eV}$ , s = 0.3 nm) and lowest ( $\Delta G = 0.3 \text{eV}$ , s = 0.1 nm) velocities is more than sixty-fold. This results in a great uncertainty in the simulations. Table 6.1 shows the combinations of values of these two parameters used in the simulations to represent the wide range of electron velocities in this model. We also report on the time the electric field was frozen for,  $t_f$ . The higher was the velocity, the shorter was  $t_f$ .



Figure 6.4: The dependence of the emission frequency, with which an electron tunnels from a surface trap to the next trap, on the electric field, according to the Poole-Frenkel transport model, expressed by equation (6.5).



Figure 6.5: The velocity of an electron travelling across a HEMT surface travelling from trap to trap, as given by equation (6.6).

Table 6.1: The values of physical parameters, that enter the Poole-Frenkel transport model, used in the simulations.

line type in Figure 6.5			
$\Delta G (eV)$	0.3	0.25	0.25
<i>s</i> (nm)	0.1	0.1	0.3
el. field frozen for $t_f(\mu s)$	4	2	0.8
reference in the following text:	slow	moderate	fast

## 6.4 Simulation Flow

We have performed self-consistent simulations taking into account the impact of the leaking electron distribution on the electric field at the gate edge and device surface. The steps in the simulation procedure are as follows:

- 1. Initially, perform a simulation at the quiescent bias with no surface charge.
- 2. Extract the electric field at the surface from the simulation. The electric field is frozen for time  $t_{f}$ .
- 3. Inject  $j_S \times t_{step}$  electrons at both edges of the gate, according to the equation (6.2) and the local electric field, where  $t_{step} \ll t_f$  is a time step, and  $t_f = n \times t_{step}$ , where *n* is an integer.
- 4. Move the surface electrons by  $v \times t_{step}$ , where v is the electron velocity given by the equations (6.5) and (6.6), shown in Figure 6.5.
- 5. Repeat steps 3 and 4 n times (until time  $t_f$  is reached).
- 6. According to their positions, assign the electrons the appropriate mesh points of the device in the simulator.
- 7. Perform a simulation to recalculate the electric field in the device.
- 8. Repeat steps 2-7 *N* times (time  $t_{sim} = N \times t_f$  is simulated).

# 6.5 Simulation Results



#### 6.5.1 Low Density Surface Leakage Current

Figure 6.6: Profiles of the electron density on the device surface at the drain side of the gate. The gate edge is positioned at  $x = 1.25 \mu m$ . All four graphs show four different values of initial surface currents on the drain edge of the gate,  $j_{D,0}$ , namely 50, 45, 40 and 35 e<sup>-</sup> $\mu m^{-1} \cdot \mu s^{-1}$ , represented by thick solid, dotted, thin solid and dashed lines, respectively. The ratio between initial surface currents at the drain and source sides is in all cases  $j_{S,0}/j_{D,0} = 5$ . The top row shows the distribution at two specific moments, using (a) *slow* and (b) *moderate* velocity profiles. The bottom row compares the distributions that result from different velocity profiles, at a specific time of the simulations. c) *Slow* and *moderate* at 400 µs, and (d) *slow*, *moderate* and *fast* at 160 µs.

Figure 6.6 shows the electron distributions at different moments, resulting from different initial surface electron density and different electron velocity profiles, defined in Table 6.1. The unsurprising result of comparing the velocity profiles is that, the higher the velocity, the further the electrons travel away from the gate. However, it is interesting to note that with higher velocities, the electron distribution is not only stretched, but skewed as well. Increasing the velocity near the gate edge lowers the electron density there disproportionately. This phenomenon can be explained as follows. First, for lower velocity, at a specific time, the electrons are closer to the gate. This leads to reduction (in absolute

terms) of the electric field closer to the gate, and hence the reduction of velocity and further accumulation of electrons there, in a positive feedback. Lower velocity profile will lead to higher electron concentration closer to the gate.



Figure 6.7: a) The electric field distribution using *slow* and *moderate* velocity profiles after 160µs and 80µs, respectively. The black line is the electric field before the electron leakage. Higher leakage current and hence higher electron density (solid lines) leads to higher electric field and therefore higher velocity at the front of the electron distribution. This results in the electrons getting farther from the gate. The colouring corresponds to the Figure 6.6 c). b) The electric field (arrows) before (top) the leakage and the electric field (blue and green) associated with the leaked electrons (bumps) and its effect on the total electric field (red arrows with blue and green outlining). Higher electron concentration increases the electric field and velocity at the front of the stream of electrons and reduces it at the end close to the gate. The vertical black line represents the position of the gate edge. Note: The bump on the graph of  $E_x$  in the figure on the left is due to an abrupt change in mesh spacing in the simulator.

Another observation is the fact that increasing the electron surface leakage current not only provides more electrons to the surface, but also stretches the electron distribution in both directions, towards and away from the gate. To understand why, we need to turn our attention to the scheme in Figure 6.7 b). The thick black line represents the gate edge, and the arrows represent the strength and direction of the electric field. The top row shows the situation before any electrons leak to the surface. There is a very high electric field at the gate edge (red arrows), which decreases rapidly with distance (as shown in Figure 6.2). Then the electrons start to leak to the surface. We consider higher and lower  $j_{D,0}$ , which results to different amount of electrons, represented by blue and green bumps, respectively.

The electric field associated with the electrons (blue and green arrows) is proportional to their concentration. In the case with more electrons, the resulting electric field (red arrows with blue outlining) is lower closer to the gate, and higher at the other end. From this follows that, the electrons closer to the gate will move slower than in the case with fewer electrons (red arrows with green outlining). This is illustrated in Figure 6.7 a). Higher  $j_{D,0}$  results in higher electron density and higher negative electric field at the front of the electron distribution, which in turn means higher velocity.



Figure 6.8: The electron distribution on (a) the source and (b) drain sides of the gate after 160 $\mu$ s (solid) and 400 $\mu$ s (dashed). The simulations were done for all three above mentioned velocity profiles, *slow* (blue), *moderate* (red) and *fast* (green). b) (drain side) also shows the impact of changing the  $j_{D,0}/j_{S,0}$  ratio (light coloured lines). The effect is stronger for slower velocities. Using the *fast* velocity profile, the electrons on the drain side crossed almost 1 $\mu$ m in just 160 $\mu$ s. The gate is positioned between x=1 $\mu$ m and x=1.25 $\mu$ m.

The electron sheet density on both sides of the gate, for various velocity profiles, is shown in Figure 6.8. In the subfigure b), showing the drain side of the gate, two ratios of initial current on the drain and source sides are compared,  $j_{D,0}/j_{S,0} = 5$ , 10. This has impact on the dependence of the surface current leakage on the electric field, as shown in Figure 6.3. When the electrons are closer to the gate, due to the lower velocity, they reduce the electric field at the gate edge more. Therefore, the effect is more pronounced for lower electron velocity. On the source side, the effect is negligible for the two simulated ratios.



Figure 6.9: The electric field at the drain (a) and source (b) edges of the gate. Red lines show simulations with same electron leakage parameters  $(j_{D,0}, j_{D,0}/j_{S,0})$  and different velocity profiles, given by different combinations of  $\Delta G$  and s. Solid lines show simulations with *slow* electron velocity, the same  $j_{D,0}/j_{S,0}$  ratio, but varying initial surface current density  $j_D$ . On the drain side, pink and orange dashed lines represent simulations with the same  $j_D$  as the red line, but varying  $j_{D,0}/j_{S,0}$  ratio.



Figure 6.10: Due to the electric field at the edge of the gate, the electrons tunnel from the gate to the device surface. a) Electron surface current density on the drain edge  $j_D$  given by the Frenkel-Poole emission model. b) The total charge leaked to the surface. The colour coding is the same as in Figure 6.9, except for the *fast* velocity profile in b), where the dotted red line is replaced with solid black, to make the graph more readable.

The temporal evolution of the *x*-component of the electric field,  $E_x$  (at the drain and source edges of the gate), the surface leakage current density  $j_D$  and the total leaked charge at the surface (on the drain side of the gate), which is an integral of  $j_D$ ,  $Q_L(t) = \int_0^t j_D(t) dt$ , are shown in Figure 6.9 and Figure 6.10, respectively. The red lines show results from simulations with the same leakage parameters,  $j_{D,0} = 50 \text{ e} \cdot \mu \text{m}^{-1} \cdot \mu \text{s}^{-1}$  and  $j_{D,0}/j_{S,0} = 5$ , and different velocity profiles (Table 6.1). The higher are the velocities, the further away the electrons move from the gate and the less the electric field at the gate edge is decreased.

From this follows that, lower velocities reduce the leakage current density faster and, as a result, fewer electrons leak to the surface. Solid lines show the impact of varying  $j_{D,0}$ , keeping the velocity profile (*slow*),  $\Delta G = 0.3$  eV and s = 0.1nm, and the ratio of the initial surface current densities on the drain and source side,  $j_{D,0}/j_{S,0} = 5$ , constant. Unsurprisingly, the higher is the  $j_{D,0}$ , the stronger is the effect on the electric field and all related quantities. Let us note that, even the relative effect on  $j_D$  is stronger. After 800µs of simulation,  $j_D = 0.65 (0.74) j_{D,0}$ , for  $j_{D,0} = 50 (35) e^{-}\mu m^{-1} \cdot \mu s^{-1}$ . Finally, the impact of changing the electron leakage dependence (Figure 6.3) on the electric field on  $E_x$ ,  $j_D$  and  $Q_L$  at the drain edge of the gate, by setting  $j_{D,0}/j_{S,0}$  to 7 and 10, is represented by the pink and orange dashed lines, respectively. Since this parameter affects the current density  $j_D$  at lower electric fields, increasing the  $j_{D,0}/j_{S,0}$  ratio reduces the total leaked charge  $Q_L$  and the reduction of the electric field at the gate edge is less pronounced.

To summarize, we will make three observations. Firstly, the electron distributions, in Figure 6.6 and Figure 6.8, are not exponential and do not approximate the pattern "a lot of electrons close to the gate, less electrons further away", previously determined to fit the *I-V* data best. Secondly, the electric field at the gate edges, as shown in Figure 6.9, is being reduced very slowly, and so is the surface leakage current density  $j_D$ , shown in Figure 6.10, left. This means that, the electrons tunnelling from the gate during the whole time  $t_q$  in between the measurements, and after the measurement of one  $V_G$ - $V_D$  point, which takes 1µs only, as the device is biased to  $V_{G,q}$ - $V_{D,q}$  again, the electrons continue to leak. This will further change the electron distribution and will invalidate any attempt to fit the pulsed I-Vmeasurement with a single surface charge distribution. Of course, in theory, this cannot be ruled out and is a possible scenario of electron leakage from the gate. However, to avoid this at least in the simulation, we can increase  $j_{D,0}$  significantly, whereby reducing  $E_x$  at the gate edge and  $j_D$  much faster, and so securing an electron distribution that will not change significantly after each measurement. Then, we have to judge the plausibility (whether it fits the pulsed *I-V* measurement data) of the resulting electron distribution. Thirdly, the higher are the velocities, the worse are the problems described above (the distributions resemble the previously determined pattern less;  $E_x$  at the gate edge and  $j_D$  are less reduced).

To address these issues, simulations with high  $j_{D,0}$  (200-2000 e<sup>-</sup> $\mu$ m<sup>-1</sup> $\mu$ s<sup>-1</sup>) employing the *slow* and *moderate* velocity profiles and very high  $j_{D,0}$  (5000 e<sup>-</sup> $\mu$ m<sup>-1</sup> $\mu$ s<sup>-1</sup> and more) employing only *slow* velocity profile, were performed in 6.5.2. Additionally, the impact of the values used for the ratio  $j_{D,0}/j_{S,0}$  (5, 7 and 10) on the electron distributions (Figure 6.8 b) was negligible. Therefore, in the simulations that follow, we used the values 5 and 20 for the  $j_{D,0}/j_{S,0}$  ratios.

#### 6.5.2 High Density Surface Leakage Current

Table 6.2 lists all simulations that were performed in this section, along with the colour codes used in the following figures. The colour coding is not kept when comparing simulations with the same  $j_{D,0}$ . The values in the table report on the time of the simulations the electric field was kept constant (frozen). A simulation of the device, and hence the recalculation of the electric field, takes approx. 30-40 minutes. So, choosing longer  $t_f$  allows us to simulate the electron leakage for a longer time of the process for a given simulation time, or, simulation of a given real world time takes less simulation time. On the other hand, with the electrons changing their positions, the electric field distribution changes as well and therefore the electron leakage and transport are also changed. Not updating the electric field often enough leads to huge errors. Obviously, there is a balance to be struck. This issue is addressed in section 0, where the simulations with the same parameters, but different  $t_f$  are compared, as noted in Table 6.2.

Table 6.2: List of simulations analysed in this section.  $t_f$  is the time step, for which the electric field was frozen in each simulation. Where there are two numbers, two simulations were performed, to analyse the impact of the time step on the evolution of the electric field and the resulting electron distribution. The colours of the lines represent the colours used in the following figures for the respective simulations.

$t_{f(rozen)}$ (µs)		$j_{D,0} (e^- \cdot \mu m^{-1} \cdot \mu s^{-1})$								
		200	500	1,000	2,000	5,000	10,000	20,000	50,000	75,000
$j_{D,0}/j_{S,0}$	$\Delta G (eV)$									
5	0.3	2	0.8	0.4	0.4	0.4	0.2	0.1	0.2/0.1	-
20	0.5	2	0.8	0.4	0.4	0.4	0.4	0.1	0.2/0.04	0.4/0.02
5	0.25	2	0.8	0.4	0.4	-	-	-	-	-
20		2	0.8	0.4	0.4	-	-	-	-	-

In reporting the simulation results of quantities such as the x-component of the electric field  $E_x$  at the source/drain edge of the gate, the surface electron leakage current to the source/drain side  $j_S/j_D$ , total amount of electrons leaked to the surface  $Q_L$  of the source/drain side of the gate, and finally the electron distributions themselves, we concentrate on the drain side, since the leakage is in principle the same. To capture the DC-RF dispersion, we are mostly interested in the final distribution of the electrons in the moment of the pulsed measurement, and whether such a distribution is actually assumed or not. To achieve a final distribution, one of two scenarios must occur. Either, the leakage of electrons and their velocity drop to very low levels so that the distribution is more or less fixed for the time of the measurement and all subsequent measurements, or the leaked electrons are compensated by the flow of electrons that are transported away by the Frenkel-Poole mechanism. To put it in other words, either, the leakage and subsequent flow of the electrons, due to low values of the electric field, stops or significantly slows down, or, the leakage and transfer of electrons reach a steady state at which the overall distribution does not change, while the surface electrons continue to move from trap to trap. If neither of those can be achieved, the whole concept of using a single surface electron distribution to calibrate the pulsed I-V characteristics is questionable.

# 6.5.2.1 The electric field at the Gate Edges and Emission of the Electrons from the Gate to the Surface of the Device

An essential part, in search for the answer to the question of the stability of the surface electron distribution, is obtaining  $E_x$  at both of the gate edges, which, via the Poole-Frenkel emission model, determines  $j_{D,0}$  and  $j_{S,0}$ .  $E_x$  is reported in Figure 6.11, Figure 6.13 and Figure 6.15 for lower and higher  $j_{D,0}$  on the drain edge and all values of  $j_{S,0}$  on the source edge of the gate, respectively. The corresponding  $j_D$  and  $j_S$  are reported in Figure 6.12, Figure 6.14 and Figure 6.16. We can make some observations based on this set of figures. The impact of the ratio  $j_{D,0}/j_{S,0}$  (5 vs. 20) and of the velocity profile, represented by the parameter  $\Delta G$  (0.25eV vs. 0.3eV), as well as the  $j_{D,0}$  parameter, are compared. Firstly, higher  $j_{D,0}$  means more electrons burst to the surface initially, which leads to faster reduction of the electric field. This in turn reduces  $j_D$  and  $j_S$  faster. Not only relatively, as a portion of  $j_{D,0}$  and  $j_{S,0}$ , but, as may be seen on the right of the figures showing  $j_D$  and  $j_{S,0}$ . For the



Figure 6.11:  $E_x$  at the drain edge of the gate simulated for various values of  $j_{D,0}$ , using two different velocity profiles and two different electron leakage profiles, with one combination missing, for the sake of clarity of the figure. This is a follow-up to Figure 6.9 left, for simulations with higher  $j_{D,0}$ , with the highest  $j_{D,0}$  from that figure reprinted in this one with grey lines. Follow-up to this figure with even higher  $j_{D,0}$  is Figure 6.13. Increasing  $j_{D,0}$  further reduces the electric field even faster. For  $j_{D,0} = 2,000 \text{ e}^{-1} \text{ µm}^{-1} \text{ µs}^{-1}$ , the electric field at the gate edge drops to half its initial value in less than 6 µs. This has a huge impact on the development of the electron distribution. The corresponding electron distributions are presented in Figure 6.17: solid lines  $(\Delta G = 0.3 \text{ eV}, j_{D,0}/j_{S,0} = 5) - top \ left$ ; dashed lines  $(\Delta G = 0.3 \text{ eV}, j_{D,0}/j_{S,0} = 20) - top \ right$ ; dotted lines  $(\Delta G = 0.25 \text{ eV}, j_{D,0}/j_{S,0} = 5) - bottom \ left$ ; unreported here  $(\Delta G = 0.25 \text{ eV}, j_{D,0}/j_{S,0} = 20) - bottom \ right$ . Figure 6.20 right compares the distributions (top) and  $j_D$  (bottom) simulated with the same value of  $j_{D,0} = 2,000 \text{ e}^{-1} \text{ µm}^{-1} \text{ µs}^{-1}$  (red lines here). The corresponding  $j_D$  is shown in Figure 6.12.



Figure 6.12: The dependence of the temporal evolution of  $j_D$  on  $j_{D,0}$ , on the emission model parameters and on the transport velocity of the electrons. Higher  $j_{D,0}$  results in faster reduction of  $j_D$  both relative to  $j_{D,0}$  (left) and in absolute values (right).  $Q_L$ , which is the integral of  $j_D$ , for  $\Delta G = 0.3$  eV is reported in Figure 6.22 and Figure 6.23 for  $j_{D,0}/j_{S,0} = 5$  (solid lines) and  $j_{D,0}/j_{S,0} = 20$  (dashed lines), respectively. The corresponding  $E_x$  is shown in Figure 6.11, all other parameters as described therein.



Figure 6.13:  $E_x$  at the drain edge of the gate, for  $j_{D,0} = 5,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$  and more, which is a follow-up figure to Figure 6.11 (with one of the simulations shown in that figure reprinted here). As expected, further increase in  $j_{D,0}$  speeds up the reduction of  $E_x$  at the gate edge and hence the electron tunnelling to the device surface. For the parameters  $j_{D,0} = 20,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$  and  $j_{D,0}/j_{S,0} = 5$ ,  $E_x$  drops to half its initial value in 0.47 µs, and for  $j_{D,0} = 50,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$  and  $j_{D,0}/j_{S,0} = 20$  in 0.25 µs. Some of the corresponding electron distributions are reported in Figure 6.18 ( $j_{D,0}/j_{S,0} = 5$ ), Figure 6.19 ( $j_{D,0}/j_{S,0} = 20$ ) and Figure 6.21 ( $j_{D,0} = 20,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ ). The corresponding  $j_D$  is shown in Figure 6.14.



Figure 6.14: Further increase of  $j_{D,0}$  causes further acceleration of the reduction of  $j_D$  (left) which, for high  $j_{D,0}$  quickly drops below the  $j_D$  of the lower  $j_{D,0}$  (right). The higher is difference between  $j_{D,0}$  of two simulations, the faster this happens (right).  $Q_L$  is shown in Figure 6.22 and Figure 6.23 for  $j_{D,0}/j_{S,0} = 5$  (solid lines) and  $j_{D,0}/j_{S,0} = 20$  (dashed lines), respectively. The corresponding  $E_x$  is shown in Figure 6.13, all other parameters as described therein. Note: the slight oscillation in the simulation of  $j_D$  for  $j_{D,0} = 20,000 \text{ e}^{-1} \text{ µm}^{-1} \text{ µs}^{-1}$  and  $j_{D,0}/j_{S,0} = 5$  (solid black line) is caused by the fact that the time step was insufficiently short. This will be expanded on in the next section (0).

parameters  $j_{D,0} = 50 \text{ e}^{-1} \mu \text{m}^{-1} \mu \text{s}^{-1} (j_{D,0}/j_{S,0} = 5)$  and lower,  $E_x$  at the gate edge did not even approach half its initial value in the simulated time of 800 µs, as reported in the previous section in Figure 6.9, and included for comparison in Figure 6.11. In contrast, for  $j_{D,0} = 2,000 \text{ e}^{-1} \mu \text{m}^{-1} \mu \text{s}^{-1} (j_{D,0}/j_{S,0} = 5) E_x$  reached half its initial value in just under 6µs, for  $j_{D,0} = 20,000 \text{ e}^{-1} \mu \text{m}^{-1} \mu \text{s}^{-1} (j_{D,0}/j_{S,0} = 5)$  in 0.47µs and for  $j_{D,0} = 50,000 \text{ e}^{-1} \mu \text{m}^{-1} \mu \text{s}^{-1} (j_{D,0}/j_{S,0} = 5)$  in 0.47µs and for  $j_{D,0} = 50,000 \text{ e}^{-1} \mu \text{m}^{-1} \mu \text{s}^{-1}$ ( $j_{D,0}/j_{S,0} = 20$ ) in 0.25µs. Therefore, to shut off the leakage of electrons from the gate, the value of  $j_{D,0}$  must be even higher than those used in the reported simulations.

Another observation from these figures is that higher-velocity profile impedes shutting-off the electron emission from the gate. This is due to the fact that higher velocities move the electrons faster away from the gate and hence they have lower impact on the  $E_x$  reduction. Similarly, higher value of the  $j_{D,0}/j_{S,0}$  ratio has a similar effect on  $E_x$ . To conclude, high  $j_{D,0}$ , low  $j_{D,0}/j_{S,0}$  and low velocity profile are conductive in shutting off the electron leakage from the gate.

It has to be noted that two of the reported simulation results here show clear signs of insufficiently short  $t_f$  with respect to the chosen parameters. It shows as oscillations in the time dependence of  $E_x$  and/or j. These are the  $j_{D,0} = 20,000 \text{ e}^{-1} \text{ µm}^{-1} \text{ µs}^{-1}$ ,  $j_{D,0}/j_{S,0} = 5$  and  $t_f = 0.1 \text{µs}$ , reported as solid black lines in Figure 6.14 and the  $j_{S,0} = 1,000 \text{ e}^{-1} \text{ µm}^{-1} \text{ µs}^{-1}$ ,  $j_{D,0}/j_{S,0} = 5$ ,  $\Delta G = 0.3 \text{ eV}$  and  $t_f = 0.4 \text{µs}$ , reported as solid light green line in Figure 6.15 and Figure 6.16. However, since this behaviour follows the general dependence and trend set by other results, we believe that apart from the oscillations, they approximate the correct result reasonably well.



Figure 6.15:  $E_x$  at the source edge of the gate. The corresponding distribution and  $j_s$  for  $j_{s,0} = 100 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$  (orange lines), compared with  $j_{D,0}/j_{s,0} = 20$  (not shown in this figure) is shown in Figure 6.20, top and bottom left, respectively. The  $j_s$  corresponding to this figure are shown in Figure 6.16.



Figure 6.16:  $j_S$  for various  $j_{S,0}$  and various velocity profiles.  $Q_L$  for  $\Delta G = 0.3$  eV is reported in Figure 6.24 left; the corresponding  $E_x$  in Figure 6.15; and other parameters as described therein. The cause of the oscillations for  $j_{S,0} = 1,000$  e<sup>-</sup> $\mu$ m<sup>-1</sup> $\cdot$  $\mu$ s<sup>-1</sup> (solid light green line) is a too large time step.

#### 6.5.2.2 Surface Electron Distributions

After investigating the electron leakage to the surface of the device, let us turn our attention to the actual electron distribution, and how it evolves with time, to see, whether or not, the distribution comes close to the one obtained by calibrating the pulsed I-V

characteristics, shown in Figure 5.14. Let us call it the *ideal* distribution to refer to later in the text. Figure 6.17 shows the distributions on the drain side of the gate at two time points, at 20µs and 100µs, for moderate initial surface electron leakage currents,  $j_{D,0} = 200 - 2,000 \text{ e}^-\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ . The four subfigures compare the impact of the velocity profiles, defined by the parameter  $\Delta G$ , and impact of the emission model parameter  $j_{D,0}/j_{S,0}$ . Figure 6.18 and Figure 6.19 show the distributions for high values of leakage current,  $j_{D,0} = 2,000 - 50,000 \text{ e}^-\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ , each using 5 and 20 as values of the parameter  $j_{D,0}/j_{S,0}$ , respectively, this time only for the *slow* velocity profile. Figure 6.20 compares the impact of the velocity profile and the ratio  $j_{D,0}/j_{S,0}$  on the distributions and  $j_D$  on both sides of the gate in one figure, keeping  $j_{D,0}$  constant, at 2,000 e<sup>-</sup>·µm<sup>-1</sup>·µs<sup>-1</sup>. Figure 6.21 shows the impact of  $j_{D,0}/j_{S,0}$  on the distribution on the drain side, for the *slow* velocity profile and for  $j_{D,0} = 20,000 \text{ e}^-\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ .



Figure 6.17: The electron distributions at the drain side of the gate for four different values of  $j_{D,0}$  at two time points, 20µs (dotted lines) and 100µs (solid lines). Figures shows simulation results for *slow* (top) and *moderate* (bottom) velocity profiles, and two electron emission profiles,  $j_{D,0}/j_{S,0} = 5$  (left) and  $j_{D,0}/j_{S,0} = 20$ (right). The distributions from simulations for  $j_{D,0} = 2,000 \text{ e} \cdot \mu \text{m}^{-1} \cdot \mu \text{s}^{-1}$  are compared in Figure 6.20, right.  $E_x$ and  $j_D$  for all simulations, except the one on bottom right, are reported in Figure 6.11 and Figure 6.12;  $Q_L$  for top left ( $\Delta G = 0.3 \text{eV}$ ,  $j_{D,0}/j_{S,0} = 5$ ) and top right ( $\Delta G = 0.3 \text{eV}$ ,  $j_{D,0}/j_{S,0} = 5$ ) are shown in Figure 6.22 and Figure 6.23, respectively.

The overall trend, when increasing  $j_{D,0}$ , is clear. For higher  $j_{D,0}$ , the electrons tend to accumulate close to the gate and also spread further away from the gate. However, the latter effect diminishes with increasing the  $j_{D,0}$ . Lower velocity and lower  $j_{D,0}/j_{S,0}$  give distributions closer to the *ideal*, which is clear especially in Figure 6.20. For the lower velocity, the electrons reach only to 300µm away from the gate in 100µs, which is reasonable, since  $t_q = 1$ ms, and there is enough time to cover 1µm, maybe more.



Figure 6.18: A follow-up to Figure 6.17 top left, the electron distributions for three different values of  $j_{D,0}$  at three time points, 2µs, 10µs and 30µs. In spite of grand differences in distributions shortly after the start of the leakage, at 2µs (dotted lines), due to unequal drop in  $E_x$  and hence  $j_D$ , the distributions converge to roughly the same "shape" later, at 30µs (solid lines). One of two main differences among the distributions is the maximal distance the electrons reached, which changes less and less with higher values of  $j_{D,0}$  (compare with Figure 6.17). The other is that with higher  $j_{D,0}$ , the electron density at the gate edge is higher (right). The corresponding  $E_x$  and  $j_D$  are reported as solid lines in Figure 6.13 and Figure 6.14, respectively; the corresponding  $Q_L$  is shown in Figure 6.22.



Figure 6.19: A follow-up to Figure 6.17 top right, the electron distributions for very high  $j_D$ . As in true for simulations in Figure 6.18 ( $j_{D,0}/j_{S,0} = 20$ ), higher  $j_D$  means more electrons at the gate edge and the front of the distribution is further away, although the latter is less significant for very high  $j_D$ . Otherwise, the resulting distributions are similar. The corresponding  $E_x$  and  $j_D$  are reported as dashed lines in Figure 6.13 and Figure 6.14, respectively; the corresponding  $Q_L$  is shown in Figure 6.23.



Figure 6.20: The electron distributions (top) and  $j_s$  as a function of time (bottom) for the source (left) and drain (right) sides of the gate. This figure compares simulations with the same  $j_{D,0}$  ( $j_{S,0}$ ), for two different velocity profiles (given by the parameter  $\Delta G$ ) and two different electron emission parameters ( $j_{D,0}/j_{S,0}$ ). Slower velocity and lower  $j_{D,0}/j_{S,0}$  both mean more electrons close to the gate and hence a distribution closer to the "ideal". On the drain side, the corresponding  $E_x$  and  $j_D$  are reported as red lines in Figure 6.11, Figure 6.12, respectively. Blue and green lines in this figure are results of simulations with the same parameters for both the source and the drain sides. The distributions (top) are a higher  $j_D$  follow-up to Figure 6.8.



Figure 6.21: While Figure 6.18 and Figure 6.19 compare the electron distributions for varying  $j_{D,0}$ , while keeping  $j_{D,0}/j_{S,0}$  constant, this figure compares the impact of varying  $j_{D,0}/j_{S,0}$  at  $j_{D,0} = 20,000 \text{ e}^{-1} \text{ µm}^{-1} \text{ µs}^{-1}$ . It is a higher  $j_D$  follow-up to Figure 6.20 top right for  $\Delta G = 0.3 \text{ eV}$ . As, keeping the previous results in mind, one would expect, the difference between these simulations reduces with time and the main difference is the electron density close to the gate. The corresponding  $E_x$  and  $j_D$  are shown in Figure 6.13 and Figure 6.14, respectively.



Figure 6.22: The total amount of the electrons leaked to the drain side of the gate for various  $j_{D,0}$  at  $j_{D,0}/j_{S,0} = 5$ , for *slow* velocity profile. The higher is the initial leakage, the more electrons leak to the surface. However, since  $j_D$  falls rapidly for simulations with high  $j_{D,0}$  (Figure 6.12 right and Figure 6.13 right), the increase of  $Q_L$ , after the initial burst, reduces faster for higher  $j_{D,0}$ . This is well demonstrated in the figure on the top right. The corresponding electron distributions are reported in Figure 6.17 top right and Figure 6.18.

Another important parameter of the simulations is the total amount of electrons leaked to both of the sides of the surface,  $Q_L$ , since we have an estimate of how many electrons we should expect, reported in Table 5.2 in section 5.4. Figure 6.22 and Figure 6.23 show  $Q_L$ leaked to the drain side of the gate for  $j_{D,0}/j_{S,0} = 5$  and  $j_{D,0}/j_{S,0} = 20$ , respectively. Figure 6.24 shows the same on the source side. It is encouraging, that for the wide range of values of  $j_{D,0}$ , which covers more than two orders of magnitude,  $Q_L$  is in the vicinity of the expected values, even though, for longer simulation times,  $Q_L$  exceeds the expected value. For all simulated values of  $j_{D,0}$  and simulated times, it is true that higher  $j_{D,0}$  reach higher  $Q_L$  at a specific time. However, as may be seen in Figure 6.22 top right, the higher the  $j_{D,0}$ is, after the initial burst, the slower the  $Q_L$  grows, so, in a finite time, higher  $j_{D,0}$  may result in lower  $Q_L$ . To see that, we would need to run the simulations for longer and for even higher  $j_{D,0}$ .



Figure 6.23:  $Q_L$  for various  $j_{D,0}$  at  $j_{D,0}/j_{S,0} = 20$ , for *slow* velocity profile. The corresponding electron distributions are reported in Figure 6.17 top left and Figure 6.19.



Figure 6.24: The electrons leaked to the surface side of the gate for  $j_{D,0}/j_{S,0} = 5$  (left) and  $j_{D,0}/j_{S,0} = 20$  (right).

We have investigated the electron emission from the gate and subsequent transport at the surface for a wide range of values of the initial surface current density. Here we estimate the plausibility of the used values. The highest value used in our simulations, as reported in Table 6.2, was 75'000  $e^{-}\mu m^{-1} \cdot \mu s^{-1}$ , which translates to  $1.2 \times 10^{-8} \text{A} \cdot \mu m^{-1}$ . The electrons leak to the surface at the quiescent bias  $V_G = -4V$ ,  $V_D = 25V$ , at which the drain current in this device was measured to be 180mA, which is  $3.6 \times 10^{-4} \text{A} \cdot \mu m^{-1}$ , considering the  $4 \times 125 \mu m$  width of the device. The charge in the channel is confined to a very narrow region next to the interface. As an upper limit, we can take 1.5nm, at which the charge density falls approximately tenfold, resulting in average current density  $j = 0.24 \text{A} \cdot \mu m^{-2}$ . It is not clear what is the thickness of the path through which the surface electrons propagate. As an approximation, one could take the lattice constant *c*, which is the height of the wurtzite crystal, equal to approximately 0.5nm, as reported in Table 2.1. Then the current density of surface leakage will be  $j = 2.4 \times 10^{-4} \text{A} \cdot \mu \text{m}^{-2}$ . This is three orders of magnitude less than the current density in the channel. This constitutes a reasonable limit to the value of the surface current density.

# 6.5.3 The impact of the Time Step on the Surface Charge and Leakage Current

Figure 6.25 shows  $j_S$  (left) and  $j_D$  (right) for simulations with very high  $j_{D,0}$ . Different  $t_f$  are compared.  $t_f$  is shortened two-fold, five-fold and twenty-fold, in the top, centre and bottom subfigure. It shows that the higher is the ratio between the values of  $t_f$ , the change and precision enhancement is increased. Too large values of  $t_f$  result in oscillations of j between values that are alternately too low or too high. In the first case, the oscillations are reduced. The second case is a good example how reducing  $t_f$  can lead to increasing the precision of the simulation, while in the third case, the larger  $t_f$  is clearly inapplicable, but reducing the  $t_f$  twenty-fold prevents  $j_D$  to swing to negative values.



Figure 6.25: The impact of the time step on the simulations, here exemplified using the physical parameters  $j_s$  (left) and  $j_D$  (right). The parameters used for these simulations are as follows. Top:  $j_{D,0} = 50,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ ,  $j_{D,0}/j_{s,0} = 5$ ; Centre:  $j_{D,0} = 50,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ ,  $j_{D,0}/j_{s,0} = 20$ ; Bottom:  $j_{D,0} = 75,000 \text{ e}^{-}\mu\text{m}^{-1}\cdot\mu\text{s}^{-1}$ ,  $j_{D,0}/j_{s,0} = 20$ . The difference in the time the electric field was kept constant (frozen)  $t_f$  was also different in these simulations. The decrease in  $t_f$  was two-fold (top), five-fold (centre) and twenty-fold (bottom). The higher is the difference in  $t_f$  the more the simulation is changed.

Fluctuations at the front of the surface charge distribution can be observed in the simulation results, e.g. in the Figure 6.6, Figure 6.17 and Figure 6.20. This is not a real effect, it is a residue of too large a time step for which the electric field is kept constant. The reason behind this effect following. In the absence of trapped electrons at the surface, the lateral electric field  $E_x$  is highest at the gate edge and monotonously declines towards the other contacts. Yet, when the electrons leak to the surface, they modify  $E_x$  and, for concentrations high enough, due to the repelling force of the electrons on other electrons,

 $E_x$  increases and then falls sharply. This is demonstrated in Figure 6.7 a) by the orange lines, and explained in the caption more thoroughly. This peak and sharp decline in the electric field translates to higher and lower velocities respectively. In a real world scenario, the position of the peak moves as the electrons move away from the gate. Yet when the electric field is held constant for a specific time step, some electrons leak behind the peak and their velocity is first artificially increased at the peak position and later decreased. This, in turn, leads to artificial decrease of the concentration at the peak position and accumulation of electrons thereafter. The created fluctuation in the electron concentration translates into another fluctuation of the electric field and in positive feedback more peaks and valleys in the surface charge distribution are introduced. Reducing the time step reduces this unwanted effect due to more frequent recalculation of and hence more realistic electric field. However, this would result in an unwanted increase in simulation time.

#### 6.6 Summary

We found that, for high values of the initial electron surface leakage  $j_{D,0}$  and low velocity profile, the assumed electron distribution resembles the *ideal* the most, in that it follows the pattern, a lot of electrons at the gate, less electrons further away, stretching for several gate lengths. In simulations with high value of  $j_{D,0}$ , the electron leakage drops fast to low levels and hence has the potential to fix the amount of leaked electrons in some time. However, for none of the simulated parameters, the velocity of the electrons seems to drop enough for the electrons to effectively stop moving and even the promising distributions, i.e. those with high electron density close to the gate, lose those electrons in further electron transport away from the gate via traps. To determine whether it is possible to achieve a quasi-final electron distribution, it would be beneficial to run the simulation for longer "real" time, which would require longer simulation time, and with higher  $j_{D,0}$ , which would require shorter  $t_f$ , also resulting in longer simulation time. In Figure 6.25, we have demonstrated that, to simulate the electron leakage for  $j_{D,0} = 75,000 \text{ e}^{-1} \text{ }\mu\text{s}^{-1}$ , one has to consider  $t_f$  no longer than 0.02 µs. To simulate at least one interval between the measurements,  $t_q = 1$ ms, we would need 50,000 cycles, each taking approximately half an hour, resulting in enormous 25,000 hours, i.e., almost three years.

The charge close to the gate and the electric field come to equilibrium and the charge flow (leakage current density) is stabilized and never falls to zero. Moreover, the field further away from the gate is non-zero as well – that means that the electrons never cease to move and hence it is probably not possible to arrive at a "final" distribution.

# 7 Conclusions

The aim of this thesis was to investigate some of the processes determining the degradation and failure of AlGaN/GaN HEMTs, namely DC-RF dispersion, a subclass of current collapse phenomena, and device degradation, using numerical simulations. The commercial simulation platform Sentaurus from Synopsys and a set of scripts to manipulate and automate the device simulations were utilised and developed to perform this task. Both the current collapse and the device degradation are trap-related phenomena. DC-RF dispersion is associated with charge leaked to and trapping mainly at the surface of the device, in already existing traps, forming a 'virtual gate' [116,34]. The device degradation is a process that leads to creation of new defects and dislocations and hence new traps in the device and has a similar, even though not identical, permanent effect on the I-V characteristics as the current collapse. One of the recent hypotheses for the mechanism responsible for the device degradation is defect generation due to electric field induced stress [29] in the vicinity of gate edges, particularly on the drain side, with the converse piezoelectric effect as the underlying physical phenomenon. Another consequence of the converse piezoelectric effect is related to the additional strain in the material that modifies the spatial distribution of the piezoelectric polarization, the bound charge and the transistor characteristics. The current collapse is associated with mobile charge leakage along the surface via Poole-Frenkel emission [36,35].

Chapter 1 discussed the potential of III-Ns in comparison with other semiconductor materials, as a vehicle for high-frequency high-power transistors. The two parameters that

determine suitability of a material for fabrication of such devices are the saturation velocity and the breakdown electric field, as given by the Johnson's figure of merit (JM) [3]. The comparison of the values of JM for various materials makes GaN stand out as the material of choice. The two classes of GaN devices with high application potential, the optoelectronic devices [14,15,16] and the high-frequency transistors [13,2], were introduced, later of which is the focus of this work.

Chapter 2 started by discussing the material parameters of III-Ns with focus on the properties that make this class of materials distinct from the conventional III-Vs, such as the wurtzite crystal structure with the consequence of spontaneous and piezoelectric polarization. This results in a bound charge at a III-N heterostructure interface, which gives rise to a large 2DEG density in the channel without the need for doping. Relation between the electrical properties, i.e. the electric field and piezoelectric polarization, and mechanical properties, i.e. the stress and strain, was discussed. The related direct and converse piezoelectric effects were introduced with the implication of the electric field induced strain and stress, utilized in Chapters 4 and 5 in the investigation of the gate dependent bound charge and device degradation, respectively. Then, the principle of operation of AlGaN/GaN HEMTs, the device, which is in the focus of this thesis, was discussed and an overview of key challenges in current GaN technology was provided.

The simulation methodology was discussed in Chapter 3. A brief overview of the simulation platform Sentaurus was given, with a description of the simulation tools utilized in this work with emphasis on the drift-diffusion model used in the simulations of the devices investigated in the thesis. The scripts developed in the course of the work for the purpose of calibrating the simulation tools in respect of the measured transistor characteristics, were described. Finally, the calibration process was followed detailing the fitting parameters and their literature values, and the search procedure delivering the optimal values of the parameters that reproduce the measured data. The calibrated I-V characteristics of two devices used in the rest of the parameters and the accuracy of the simulated I-V characteristics. The calibration error below 3% for a wide range of gate and drain voltages and not exceeding 10% validates the calibration process and is an important stepping stone for the rest of this work.

Voltage applied to the gate modifies the electric field at the edges of the gate and in the channel under the gate significantly. This leads to strain, induced via the converse piezoelectric effect, being dependent on the gate voltage. From this follows that the piezoelectric polarization and hence the bound charge, induced in the bulk and modified at the heterojunction interface, will vary with the applied voltage too. This phenomenon was investigated in Chapter 4. First, the theory behind the converse piezoelectric effect was elaborated. Because the computation of the stress and strain distribution from the electric field in the device is a complex electro-mechanical problem that goes beyond the scope of this thesis, a simplifying 'clamped model' [121,30] was adopted, which decouples the x and y components of the electric field from the mechanical properties of the crystal and also ignores the impact of mechanical stresses of the surrounding material on the local strain. In this chapter, we have, for the first time, evaluated the magnitude and the importance of this effect. Even without the impact of the gate voltage, the coupling of the electric field to the piezoelectric polarization decreased the difference in polarizations of the AlGaN and GaN layers and hence decreased the polarization induced sheet charge that lead to reduction of the drain curren, although this effect is moderate, leading to less than 1% current change at  $V_G \approx 0V$ . However, negatively increasing the gate voltage amplified this effect and the drain current reduction becomes more pronounced, leading to the threshold voltage shift. The current reduction was found to be virtually independent of the drain voltage.

Since both the current collapse and device degradation are trap related phenomena, Chapter 5 first investigated the impact of electrons, trapped at the surface of the device and under its gate, on the I-V characteristics. In order to gain insight, uniform distributions of charge on either side of the gate were used both with symmetric and asymmetric charge distributions in respect to the gate. These simulations yielded a conclusion that to reproduce the DC-RF dispersion the charge had to be trapped on both sides of the gate as well as under the gate, with the majority of the charge on the drain side and that the surface charge distributions should follow the pattern of "high electron sheet density at the gate and low sheet density extending away from the gate over several gate lengths". Since this is the pattern that is also followed by an exponential function with a negative argument, we made a hypothesis that the trapped surface charge could be following an exponential distribution. Performing a large number of simulations with the exponential charge distribution, employing the scripts developed for the purpose of automating and evaluating a set of simulations described in Chapter 3, we eventually found the values of the fitting parameters that reproduced the measured pulsed I-V characteristics showing current collapse accurately. In order to reproduce the I-V characteristics of a degraded device, we linked the electric field, via the converse piezoelectric effect, to regions of excessive mechanical stress, under the assumptions of the 'clamped model'. Then, we attempted to relate the calculated stress to defect density and subsequently to a charge density assumed to be trapped in the stress generated defect states. However, this strategy was unable to reproduce accurately the measured I-V characteristics of a degraded device. From the insights gained in the investigation of the impact of the surface charge on the I-V characteristics, it is obvious that, to reproduce the characteristics of the degraded device, charge has to be trapped further away from the gate, yet the region of high stress is located very close to the gate, which explains the failure to reproduce the measurements.

In Chapter 5 we found a surface charge distribution that reproduced the pulsed I-V characteristics that shows current collapse. In Chapter 6, using numerical simulations, we study the process that could result in the calibrated charge distribution. The electron emission from the gate and trap-to-trap hopping via Poole-Frenkel emission mechanism between the surface states was introduced and studied. Poole-Frenkel emission is strongly nonlinear with respect to the electric field. The model for the emission rate of electrons from the gate to the surface [132] and trap-to-trap emission frequency employs the Eyring's reaction rate model [133,128], which determines the propagation velocity of the electrons leaked from the gate, as a function of the electric field, each offering two fitting parameters. These four fitting parameters will determine the electron leakage to the surface and the temporal evolution of the surface charge distribution. In Chapter 6, the electron leakage is examined for a range of values of those parameters. The charge distribution was found to be strongly dependent on the initial surface current density of the electrons leaking from the gate and the resulting distribution resembles the exponential distribution only above a certain threshold value for the leakage current. By default, this model could never result in a stationary distribution.

## 7.1 Future Work

The converse piezoelectric effect was taken into account during the investigation of two phenomena in this thesis, the electric field impact on the polarization induced bound charge in Chapter 4, and the electric field induced mechanical stress leading to defect formation and hence to device degradation. Yet, the electro-mechanical coupling was done using the simplifying assumptions known as the 'clamped model' that omits the impact of the electric field component perpendicular to the crystal *c*-axis and the stresses exerted by the surrounding matter. An indication that the 'clamped model' is insufficient to describe the stress field in a device is that the strain/stress measured by micro-Raman spectroscopy is ten times higher than the calculated strain/stress, although the patterns of the strain/stress distributions agree [30]. Therefore, it would be beneficial to perform coupled electromechanical simulation of a device solving the equation (4.1), without employing the clamped model, to obtain more realistic strain/stress distribution, including the strain parallel with the *a*-axis of the crystal (and stress parallel with the *c*-axis), the shear strain/stress originating from the component of the electric field perpendicular to the *c*-axis and from strong gradients of the strain/stress field, and the strain/stress propagation in the device.

Another enhancement of the work in this thesis would be to calibrate the I-V characteristics of a degraded device searching for the appropriate distribution of the trapped charge irrespective of the underlying mechanism, i.e. irrespective of the exact defect distribution, and/or using the stress distribution obtained as suggested in the previous paragraph.

The simulation of the leakage of the electrons from the gate to the device performed in Chapter 6, took only primary leakage mechanism into account, i.e., to the surface of the device. To obtain a more realistic picture of the charge distribution, one could simulate the leakage including the secondary leakage mechanism, i.e. to the bulk of the device [125,128].

Finally, another improvement of the work done in this thesis would be further automation of the simulations. E.g. currently, the procedure is to perform all simulations and evaluate

all simulations thereafter. A more efficient method would of course be to perform one or several simulations, evaluate the results, modify the parameters accordingly and perform the simulations until a goal, i.e. a calibration of some sort, is achieved. This could be done using either a gradient method, which is easier to code, but has the disadvantage that it may get stuck in a local extreme, or using a genetic algorithm, which is more demanding on computational time, but scans the phase space of parameters more efficiently.

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