Simulation of Charge-Trapping in Nano-Scale MOSFETs in the Presence of Random-Dopants-Induced Variability

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Abstract

The growing variability of electrical characteristics is a major issue associated with continuous downscaling of contemporary bulk MOSFETs. In addition, the operating conditions brought about by these same scaling trends have pushed MOSFET degradation mechanisms such as Bias Temperature Instability (BTI) to the forefront as a critical reliability threat. This thesis investigates the impact of this ageing phenomena, in conjunction with device variability, on key MOSFET electrical parameters.

A three-dimensional drift-diffusion approximation is adopted as the simulation approach in this work, with random dopant fluctuations—the dominant source of statistical variability—included in the simulations. The testbed device is a realistic 35 nm physical gate length n-channel conventional bulk MOSFET. 1000 microscopically different implementations of the transistor are simulated and subjected to charge-trapping at the oxide interface. The statistical simulations reveal relatively rare but very large threshold voltage shifts, with magnitudes over 3 times than that predicted by the conventional theoretical approach. The physical origin of this effect is investigated in terms of the electrostatic influences of the random dopants and trapped charges on the channel electron concentration. Simulations with progressively increased trapped charge densities—emulating the characteristic condition of BTI degradation—result in further variability of the threshold voltage distribution. Weak correlations of the order of 10^{-2} are found between the pre-degradation threshold voltage and post-degradation threshold voltage shift distributions.

The importance of accounting for random dopant fluctuations in the simulations is emphasised in order to obtain qualitative agreement between simulation results and published experimental measurements. Finally, the information gained from these device-level physical simulations is integrated into statistical compact models, making the information available to circuit designers.

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Publications

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Chapter 1

Introduction

This work investigates, by means of a numerical simulation, the effects of interface-trapped charges in conventional bulk metal-oxide-semiconductor field-effect transistors (MOSFETs). In this introductory chapter, the motivation behind this study is presented starting with a brief overview of the variability issues and reliability concerns associated with progressive downscaling of contemporary MOSFETs. These mould the aim and specific objectives of this project, as presented in Section 1.2. Following this, an outline of this thesis and a description of the subsequent chapters are laid out.

1.1 Motivation

The phenomenal growth of the semiconductor industry is characterised by the remarkable increase of transistor count in integrated circuits, as epitomised by the well-known Moore's Law [1]. In 1971, the world's first commercially available microprocessor the Intel 4004 held 2300 transistors; by contrast a typical microprocessor embedded in today's personal computers is a large scale integration of hundreds of millions of transistors. This was partly accomplished by downscaling (miniaturisation) of the transistors, which simultaneously increases component density and switching speed, enabling overall improvement of computational complexity, memory capacity and processing speed of the chip. However as scaling enters the nanometer scale, fundamental physical limits start to affect the operational integrity of bulk MOSFETs [2].

Among the critical issues affecting contemporary MOSFETs are intrinsic variability [3] and performance degradation due to stress [4]. Intrinsic variability refers to the stochastic dispersion of the electrical characteristics, caused by atomic scale variation in the structures of the otherwise macroscopically identical transistors. As transistor features are shrunk into the deca-nanometer scale, these microscopic non-uniformities start to exert an increasingly significant impact on the device behaviour. This variation is termed intrinsic because it arises from the microscopic granularity of matter, which cannot be eliminated by tightening the manufacturing process controls [5]. Well known sources of intrinsic variability in bulk MOSFETs are random dopants [6, 7], gate line edge roughness [8, 9], local oxide thickness variation [10] and metal gate granularity [11, 12]. It has been reported that random dopants alone account for approximately 60% of the threshold voltage variation measured from the fairly recent 45 nm transistors [5]. Intrinsic variability already affects SRAM design [13], and causes timing problems in logic circuits [14].

The typical operating environment of modern integrated circuits also exerts a tremendous amount of stress on the transistors. Over time, this condition leads to the device performance degradation which will eventually compromise circuit reliability. A general type of degradation is the defect formation occurring at the Si/SiO_2 interface, or deeper in the gate oxide layer, known as Bias Temperature Instability (BTI) [15-17]. This microscopic structural damage acts as a source of trapping centres for charge carriers in the channel, causing changes in the transistor's electrical parameters which shortens its functional lifespan. Experimental [18, 19] and 3D simulation studies [20, 21] have shown that the trapping of just a *single* charge carrier in a transistor of short channel length is sufficient to cause drastic changes in the device's electrical behaviour. This effect is, in essence, analogous to intrinsic variability where atomic scale phenomena exert a dramatic impact on the device's electrical characteristics. Anomalously large threshold voltage shifts of 0.5 V have been measured in 65 nm flash memory [22]. This imposes a critical challenge to the

reliability of memory, which relies on stable device threshold voltage for read and write operations [23].

In the past, relatively large, micron-scale bulk MOSFETs could reasonably be considered as identical in terms of electrical characteristics. Similarly, the application of a given stress would result in an identical magnitude of degradation across all the devices in a given design. With the gradual downscaling of transistor dimensions, performance variations between devices start to appear due to the various sources of variability. Consequently, the application of a fixed stress on such devices results in a distribution of the parameter shifts instead of identical and uniform parameters drift. Understanding this effect is crucial in order to correctly estimate the performance and reliability of transistors, and of the systems comprising them.

1.2 Aims and Objectives

The general aim of this Ph.D is to study the effects of interface-trapped charges in the presence of a dominant source of intrinsic variability. The specific objectives of this work are to:

- Investigate the electrostatic effects of single-charge trapping and the generic dependencies of the resulting magnitudes of current reduction and threshold voltage shift;
- Identify the ways in which the random dopants influence the statistical distribution of the magnitudes of current reduction and threshold voltage shift;
- Analyse the distribution of electrical parametric shifts arising from an ensemble of MOSFETs with random-dopants-induced variability, each of which is subjected to a single trapped charge at the Si/SiO_2 interface;
- Study the impact of progressive increase of interface-trapped charges on the

distribution of transistor electrical parameters;

- Encapsulate the effects of interface charge-trapping in the presence of random-dopants-induced variability in device compact models, and investigate the impact of progressive BTI degradation on inverter circuit delay using the extracted compact models.

1.3 Thesis Outline

This thesis is organised in the following structure — Chapter 2 details the essential background on the intrinsic variability of contemporary bulk MOSFETs. The origins of variability are described in more detail and the forms of variability classified. This is followed by a review of the degradation mechanisms, specifically related to charge-trapping, affecting current and future generations of transistors.

Chapter 3 discusses the simulation methodology employed in this study. It starts with a general description of well-established simulation approaches employed for the simulation of semiconductor devices. These are described in tandem with the relative advantages and drawbacks associated with each method, with respect to the objectives of this work. This is followed by an overview of the Glasgow 'atomistic' device simulator used in this research. The techniques used to implement each intrinsic variability source in the simulator are explained, along with the measures incorporated to ensure reliable solutions. This chapter concludes with a description of the testbed device henceforth simulated in this study.

Chapter 4 examines the impact of random dopants on the magnitudes of electrical parametric shift induced by interface-trapped charges. This chapter begins with a series of systematic simulations of single-charge trapping event, where the generic dependencies of the resulting magnitudes of current change are first identified.

Following this, we analyse the distribution of parametric shifts in a simulation sample of 1000 transistors in the presence of random-dopants-induced variability, each of which is subjected to single-charge trapping.

In Chapter 5, Positive Bias Temperature Instability (PBTI) degradation is simulated on statistical samples of 1000 transistors, by progressively increasing the density of interface-trapped charges. The effect of increasing trap density on the threshold voltage distribution of the transistors in the sample is analysed and compared against experimentally observed distributions and theoretical predictions.

Chapter 6, which is entitled “Integrating the Effects of Trapped Charges into Compact Models”, focuses on the framework to incorporate the information gained from the physical simulations into device compact models, and thus make the information available to circuit designers. This chapter explains the compact model parameter extraction strategy, and evaluates the accuracy of the resulting compact models. Subsequently, the extracted compact models are also used in inverter circuit simulations, whereby the resulting delay degradation due to progressive increase of trapped charges is analysed.

Finally in Chapter 7, the findings of this thesis are summarised and restated. The direction of possible future work is also proposed.

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Chapter 2

Background

This chapter lays out the essential background regarding MOSFET intrinsic variability, and the device reliability concerns associated with charge-trapping degradation, with an emphasis on their inter-related effects on device electrical characteristics. The classification, origins and effects of variability are first discussed. Subsequently, the mechanism and effects of charge-trapping degradation are elaborated through a review of the related existing studies.

2.1 Intrinsic Variability

It is widely recognised that one of the critical challenges to further downscaling of contemporary bulk MOSFETs is the variability of the device electrical parameters [1, 2]. This is because the variation of electrical parameters caused by the various sources of variability increases in every new technology generation, adversely affecting circuit designs and yield [3, 4].

The MOSFET variability has systematic and random components [5], both of which co-exist within a die. Systematic variability is normally related to the nature of the physics of the manufacturing processes and follows well understood trends. Examples of systematic variation are the optical proximity effect and layout mediated strain. The optical proximity effect is caused by light diffraction during the photolithography process which leads to structural irregularities, such as a printed line being narrower or wider than intended in the design. Such diffraction phenomena are unavoidable

because the patterned feature length in contemporary CMOS technologies is significantly smaller than the wavelength of the light which is used to print it. For example, the feature length of the 45 nm technology node is approximately 5.5 times smaller than the 193 nm wavelength of the light which prints it. The resulting layout distortions, if left uncorrected, may significantly alter the electrical characteristics of the patterned elements compared with their designed values. Strain engineering, which was first introduced in the 90 nm technology node to boost carrier mobility, is now an essential component of CMOS technology. However, the magnitude of the strain is strongly dependent on layout – such as the spacing between transistors and the distance to the nearest shallow trench isolation. The non-uniform stress distribution in transistors of different spatial arrangements on the die consequently results in variation of carrier mobility and hence drive current. Although systematic variability, as illustrated in the examples above, is critically important, it is deterministic in nature and therefore falls under certain measures of control. For example, layout distortions anticipated during the photolithography process can be largely eliminated by optical proximity correction [6], while the impact of layout-induced strain variations can be accurately predicted and factored into the design stage, allowing optimised design margins [7, 8].

Random variability, on the other hand, is truly stochastic and varies from transistor to transistor. Unlike in the case of systematic variation whose impact can be predicted and modelled down to the level of individual transistor characteristics, in the case of random variability only the collective statistical behaviour of an ensemble of transistors can be simulated or characterised. The statistical nature of random variability is linked to the fundamental atomicity of matter and granularity of materials, which will occur even under ideal processing conditions. In that sense, the sources of random variability are *intrinsic* to the device and technology. Furthermore, random variability is exacerbated by transistor scaling, which widens the design margins needed to ensure circuit functionality. Transistor scaling into the deca-

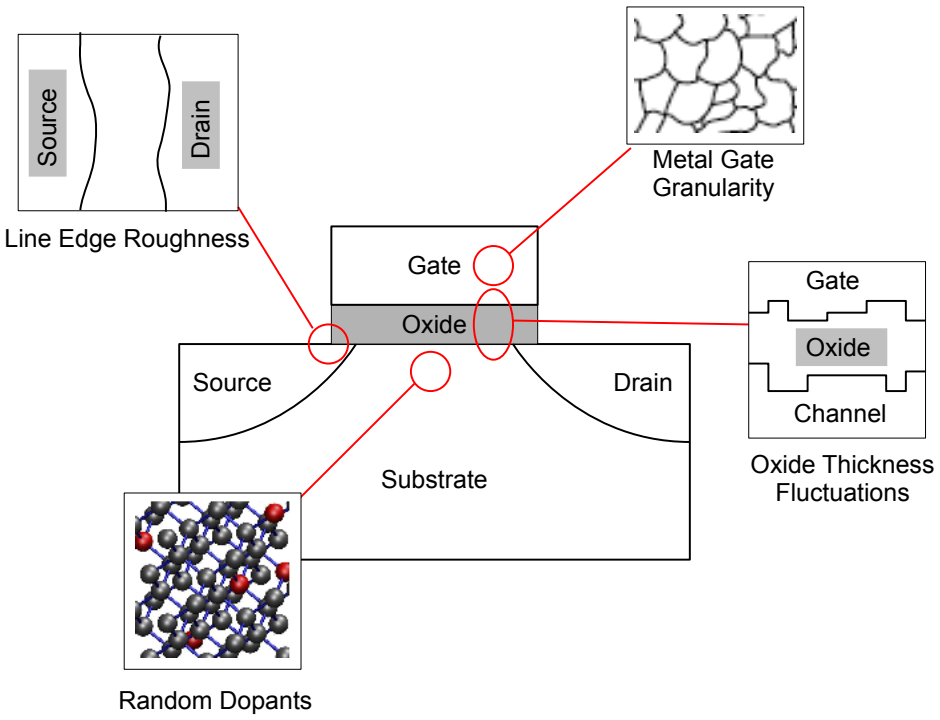


Figure 2.1: Illustration of some key sources of intrinsic variability in conventional bulk MOSFETs.

nanometer regime has effectively decreased the ratio of the device dimensions with respect to the fundamental atomic scale. The granularity of matter at this extremely small spatial scales starts to become more obvious, appearing as non-uniform and abrupt changes in device structure. More importantly, these atomic-scale non-uniformities also start to affect the device electrical characteristics to a significant degree.

Figure 2.1 illustrates the well documented sources of intrinsic variability in conventional bulk MOSFETs. The sources are gate line edge roughness, microscopic oxide thickness variations, metal gate granularity and random dopant fluctuations, all of which causes device-to-device variation of electrical parameters. Gate line edge roughness is caused by molecular scale variation in the boundaries of the photoresist

which is transferred onto the patterned gate edge during fabrication process [9], causing the channel length in a transistor to locally deviate from an ideal uniformity throughout the width of the device. Microscopic oxide thickness fluctuations refers to the atomic scale roughness of the channel-oxide interface, which lowers the channel carrier mobility [10] and increases statistical gate leakage [11]. The random orientation of crystal grains in metal gates gives rise to local variations in the metal gate workfunction, which leads to threshold voltage variability [12, 13]. Random dopant fluctuations is the phenomena of device-to-device variation in the number and microscopic spatial location of individual impurity atoms, which cannot be controlled to atomic precision during the fabrication process. Random dopant fluctuations are currently the primary source of variability in contemporary bulk MOSFETs, contributing up to 60% and 65% of the threshold voltage variability measured in 45 nm and 65 nm technology generation transistors [5]. This thesis investigates the impact of interface-trapped charges in the presence of this dominant source of intrinsic random variability.

2.1.1 Random Dopants

The effects of random dopant fluctuations on threshold voltage variability was first predicted in the 1970's [14, 15]. It has since been experimentally confirmed in a number of studies [16, 17], and extensively studied analytically [18, 19], and by 2D [20] and 3D [21-25] simulations. Figure 2.2 reports the decreasing average number of dopants in the channel region as the CMOS technology advances. In the past, transistor features were micron-scale sized and the dopant count in the channel region averaged in the thousands. As transistor dimensions are downscaled into the deca-nanometer regime, device behaviour is determined by fewer and fewer impurity atoms, and consequently becomes increasingly sensitive to their exact number and spatial position in the device active region. The effect of the variation in the number of dopants on the threshold voltage can be understood from the following basic formulation of MOSFET threshold voltage:

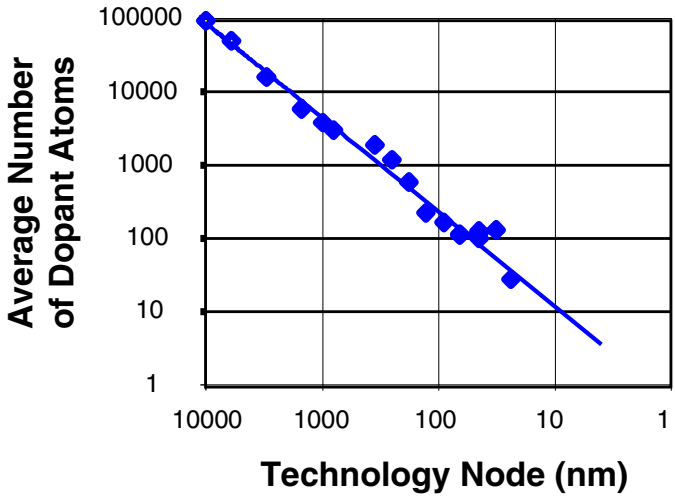


Figure 2.2: Average number of dopant atoms in the channel expressed as a function of advancement of technology node. After [87].

$$V_T = V_{fb} + 2\psi_B + \frac{\sqrt{4\epsilon_{Si} q N_a \psi_B}}{C_{OX}} \tag{2.1}$$

where V_{fb} is the flat-band voltage, ψ_B is the difference between Fermi level and intrinsic Fermi level, ε_{Si} is silicon permittivity and C_{OX} is the oxide capacitance. The square root term represents the depletion charge which explicitly depends on the nominal substrate doping N_A, the variation of which, leads to a first order estimation of V_T variation. Transistor scaling has effectively reduced the number of dopants to such a level that the stochastic spread in the dopant distribution becomes increasingly significant. By way of a numerical example, based on the data in Figure 2.2, there were on average 10^5 dopant atoms in the channel of 10 micron transistors. Assuming that the actual dopants count from device to device follows a Poisson distribution, the standard deviation ($\sqrt{10^5}$) represents a tiny percentage of ~ 0.3% of the nominal doping. By comparison, there are around 100 dopant atoms in the sub-0.1 micron transistors. The standard deviation of the dopants count is then ~ $\sqrt{100}$, which constitutes around 10% of the nominal doping — clearly a significantly larger

fluctuation.

The above description does not provide a full picture of random dopants effects as it does not take into account the random spatial positions of the impurity atoms. The fabrication process of modern bulk MOSFETs involves several ion implantation steps to introduce doping impurities into the device [26]. During implantation, the dopants are beamed into the semiconductor with high energy, and randomly scatter many times before coming to a rest. The semiconductor is then annealed to activate the impurities, during which the dopants diffuse further and replace the silicon atoms in the crystal lattice. Due to the random scattering events during implantation and diffusion during annealing, the final positions of individual dopant atoms vary from one device to another. Each transistor is essentially microscopically unique even though they may share a macroscopically identical doping design and structural layout.

3D simulation studies have shown that threshold threshold voltage variability can occur due to the spatial variation of the dopant atoms, even in the chance cases when the number of dopant atoms are identical between two transistors [25]. For example, random dopants are shown to exert the greatest impact on the threshold voltage if they happen to be located in the middle of the channel where the maximum potential barrier separating the source and drain lies, and/or close to the oxide interface where inversion takes place [23]. The spatial distribution of dopants has also been shown to significantly influence transport properties in the inversion layer, causing transconductance variations and the spreading out of drive currents at high drain bias [27].

Random dopants introduce inhomogeneity into the electrostatic potential landscape of the transistor channel [28]. As a result, within any given transistor, local portions of the channel will turn on before others and there will exist random variations of local

carrier concentration as the current percolates between the peaks in the electrostatic potential centred on discrete ionised impurities. None of these effects are accounted for in the conventional simulation approach where the MOSFET is modelled assuming an ideal continuous distribution of charge.

Intrinsic variability inevitably requires an adoption of a new paradigm in the simulation of ultra-scaled devices, in two major aspects: Firstly, the simulated device must reflect the real-world intrinsic variations in its structure, because these exert a significant degree of influence on the electrical metrics. Secondly, intrinsic variability necessitates that the simulations are done on a statistical scale because it is no longer sufficient to only simulate a single device. A statistical ensemble of microscopically unique transistors has to be simulated to describe the statistical behaviour of the electrical characteristics. In addition, intrinsic sources of variability must also be considered when assessing device reliability, because the transistors may not degrade identically under the application of a given stress.

2.2 Charge-Trapping

The silicon atom has four valence electrons and therefore requires four bonds to form a saturated valence shell. In the bulk crystalline structure, each silicon atom establishes bonds with its four neighbouring atoms, leaving no unpaired bond. At the bare surface however, silicon atoms are missing therefore there are unsatisfied, electrically active dangling bonds resulting in defect states in the band gap known as interface traps, as illustrated in Figure 2.3. After thermal oxidation, most of the traps are paired with oxygen atoms forming the SiO_2 layer. Further improvement of the interface quality is done through passivation with hydrogen, forming the inert Si-H bonds [29]. With this treatment, the interface traps density is reduced to 10^{10} cm^{-2} or below [30].

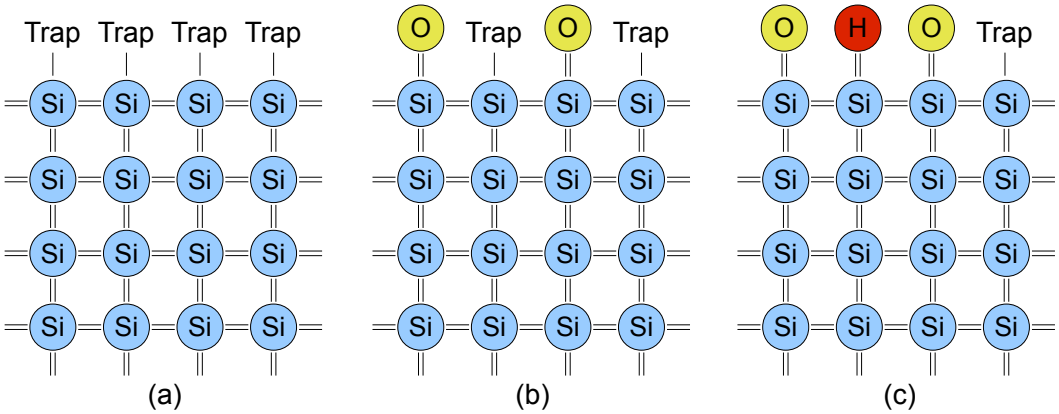


Figure 2.3: (a) Unpaired valence electrons at the silicon surface form electrically active interface traps. (b) Thermal oxidation pairs most of the silicon surface atoms with oxygen atoms, thus reducing the number of interface traps. (c) After annealing with hydrogen ambient the amount of interface traps is further reduced.

2.2.1 Random Telegraph Signal

The remaining traps located at the interface or in the oxide can capture and re-emit some of the charge carriers flowing in the channel connecting the source and drain. When a trap captures a carrier, the drain current is affected because the number of available carriers for conduction changes, and the charged trap centre becomes a Coulomb scattering centre, affecting carrier mobility in the channel. The erratic trapping and detrapping of carriers at or near the interface defects is widely accepted to be responsible for the so-called Random Telegraph Signal noise [31-33].

Extensive studies of RTS are spurred by the increase of electrical noise in MOSFETs as the device is downscaled. For the case of an n-channel MOSFET, the random capture and emission of a single electron by an individual interface trap results in discrete switching between low and high current levels. As illustrated in Figure 2.4, RTS is characterised by the capture (t_c) and emission (t_e) times, and the amplitude of

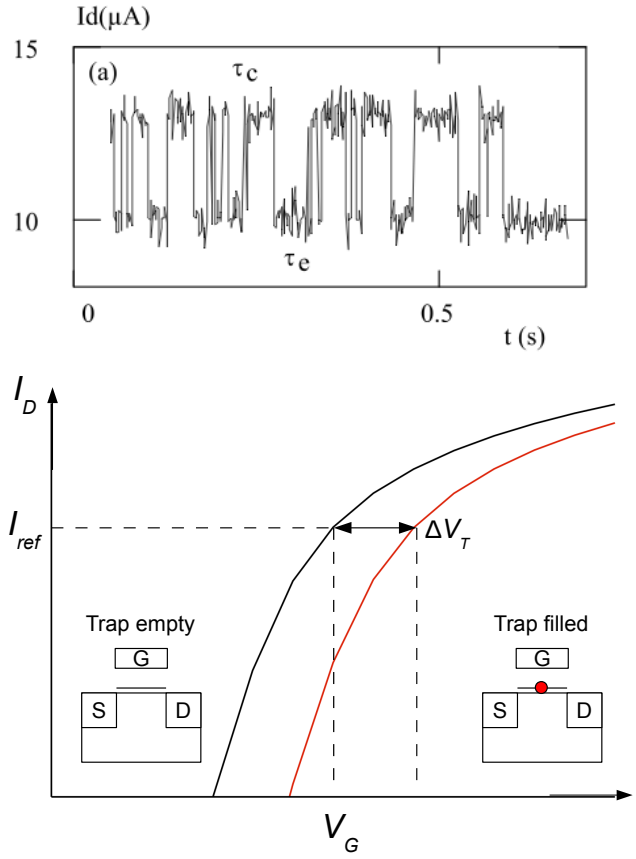


Figure 2.4: *Top*) Typical plot of drain current fluctuations due to RTS, after [34]. *Bottom*) Definition of threshold voltage shift caused by RTS.

current and threshold voltage change. The threshold voltage shift caused by a single interface-trapped charge can be expressed to first order as [34-36]:

$$\Delta V_T = \frac{q}{C_{OX} W L} \tag{2.2}$$

where q is elementary charge, C_{OX} is capacitance of gate dielectric per unit area and W and L are the channel width and length respectively. The corresponding amplitude of drain current change due to this electrostatic effect can then be expressed as $\Delta I_D = -g_m \Delta V_T$, where g_m is the transconductance. RTS magnitude increases with scaling due to the inverse relationship with channel area [37, 38]. Already RTS amplitudes as high as

60% have been reported in deca-nanometer channel width devices [37]. RTS is particularly worrisome in memory circuits such as SRAM and flash memory where large magnitudes of RTS are a major concern due to the induced threshold voltage instabilities which compromise the reliability of read and write operations [39-41]. Other experimentally measured RTS amplitudes are widely scattered even for a given device design [38, 42], and sometimes amplitudes anomalously larger than estimated by the conventional formula described above have been reported [43-45]. These so-called 'giant' RTS amplitudes have been attributed to several factors. It was suggested, for instance, that the mobility fluctuations caused by Coulomb scattering by the trapped charge could amplify the RTS amplitudes [33, 36, 46]. Simultaneous trapping of multiple discrete charges has also been suggested as a possible mechanism responsible for anomalously large RTS magnitudes, as evidenced by the experimentally observed multiple discrete levels of current switching [41]. Inhomogeneous channel conduction was also thought to give rise to the statistical spreading of RTS amplitudes, where the channel non-uniformity is attributed to the potential fluctuations from oxide thickness variation [36] and fixed oxide charges [47].

A more recent proposition, in line with increased understanding of MOSFET intrinsic variability, is that the random dopants are responsible for the statistical spread and anomalously large RTS amplitudes. 3D simulation studies in [35, 44, 48-51] demonstrate that unlucky charge trapping in critical current paths of a random-dopants-induced inhomogeneous channel can result in large RTS amplitudes, much larger than predicted by the simple 1D approximation of Equation 2.2. However, with the exception of the more recent studies in [49], the previous authors have focused on the impact of single stray charges and did not consider the statistical distribution for a number of charged defect states in a single transistor. Such simplification may underestimate the distribution of current and threshold voltage changes recorded from the simulated ensemble of devices.

2.2.2 Bias Temperature Instability (BTI)

2.2.2.1 Causes and Effects of BTI

BTI is a type of MOSFET degradation phenomena which is generally attributed to interface trap creation at the oxide interface [52, 53]. During fabrication, the transistors are annealed in ambient hydrogen to passivate the silicon dangling bonds, thus reducing the interface trap density. However, over the device operating lifetime these passivated bonds are gradually broken, causing performance degradation. With the downscaling of transistors, BTI has emerged as a significant reliability concern for digital and analog circuits in CMOS technology. In particular, the aggressively scaled oxide thickness which leads to higher oxide field, in conjunction with elevated operating temperatures (due to ambient dissipation from increasingly dense circuits), are found to accelerate the bond-breaking at the oxide interface [54, 55]. Typical stress temperatures lie in the range of 100 - 250˚C, with oxide electric fields typically below 6 MV/cm. These are not only typical conditions encountered during burn in, but are also approached during routine operation of high performance ICs.

BTI degradation can be observed in both p- and n-channel MOSFETs. For a p-channel MOSFET, the degradation is found most profound when the device is stressed with negative gate voltages [52] causing the so-called Negative Bias Temperature Instability (NBTI). This stress corresponds to the routine operating condition of a CMOS inverter when the input voltage is at a low state, as illustrated in Figure 2.5. NBTI in pMOSFETs results in a build-up of positive charges at the interface or in the oxide layer, leading to performance reduction. With the introduction of high-*k* gate dielectrics in the 45 nm process technology, the Positive Bias Temperature Instability (PBTI) associated with electron trapping in n-channel MOSFETs started to emerge as a new reliability threat [56, 57]. The use of high-*k*/metal gates have proven to be an effective measure to suppress gate leakage and boost transistor performance [58], however the dielectric material exhibits significant charge-trapping due to its higher

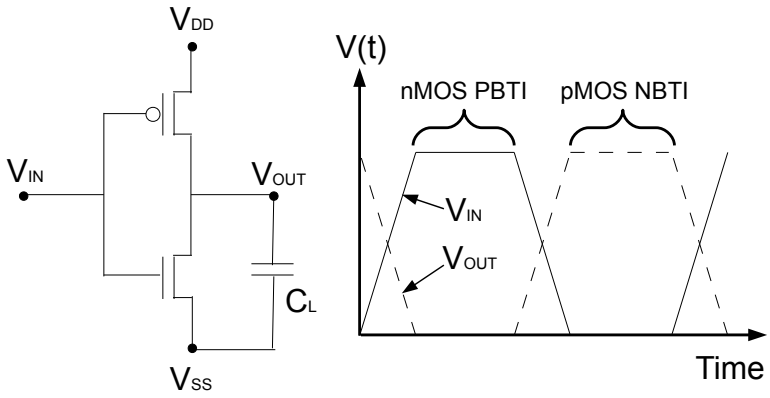


Figure 2.5: (*Left*) Circuit schematic of a CMOS inverter driving a capacitive load. (*Right*) Timing diagram illustrating degradation modes during CMOS inverter operation.

trap density [59, 60].

It is helpful to review some basic MOSFET concepts in order to understand the effects of BTI. The MOSFET threshold voltage is given by:

$$V_T = V_{fb} + 2\psi_B + \frac{\sqrt{4\epsilon_{Si} q N_a \psi_B}}{C_{OX}} \tag{2.1}$$

where the flat-band voltage, V_{fb} , is given by:

$$V_{fb} = \phi_{ms} - (\frac{Q_f + Q_{it}}{C_{OX}}) \tag{2.3}$$

where Φ_{ms} is the workfunction difference between the gate metal and the semiconductor, Q_f is the oxide fixed charge density and Q_{it} is the interface trapped charge density. From these equations, it can be seen that electron trapping in nMOSFET PBTI increases the threshold voltage V_T which leads to positive shift of threshold voltage. On the other hand, positively charged defect states in the case of pMOSFET NBTI cause negative threshold voltage shift. In both cases, the increase in the absolute value of V_T reduces the drain current, as indicated by the following basic

formulation of MOSFET saturation current:

$$I_D = (\frac{W}{2L})\mu_{eff}C_{ox}(V_G - V_T)^2 \quad (2.4)$$

where V_G is the gate voltage and all other parameters have the same previously mentioned meanings. The effective carrier mobility in the channel, μ_{eff}, is also affected by the interface traps via additional surface-related scattering [53] which also contributes to the drain current reduction. This performance degradation consequently reduces circuit switching speed (because lower current takes longer capacitor charging time) [61] and may eventually result in operational failure [62].

2.2.2.2 Time-Dependence Model of BTI

The Reaction-Diffusion (RD) model is the most prevalent description of NBTI [55, 63, 64], which was first proposed by Jeppson and Svensson in 1977 [65]. The model is capable of reproducing the stress time dependence of the device degradation due to NBTI over a wide range of measurements. There are various refinements to the standard RD model [66, 67] but only the elementary aspects of the basic RD model will be described here. The model attributes the degradation to a combination of two effects as illustrated in Figure 2.6. During the initial reaction phase, the passivated silicon-hydrogen bonds are dissociated with a linear dependence on stressing time generating interface traps and releasing hydrogen according to the model:

$$Si_3{\equiv}SiH \rightarrow Si_3{\equiv}Si\bullet + H \quad (2.5)$$

where $Si_3{\equiv}SiH$ is a hydrogen terminated silicon bonds at the interface and Si• is an unpaired silicon dangling bond. In the subsequent diffusion phase, the hydrogen diffuses away from the interface into the dielectric during which the trap generation exhibits a fractional power-law stress time dependence t^n , where n is frequently reported as 0.25. These different phases can be seen in Figure 2.6 as the change in rate

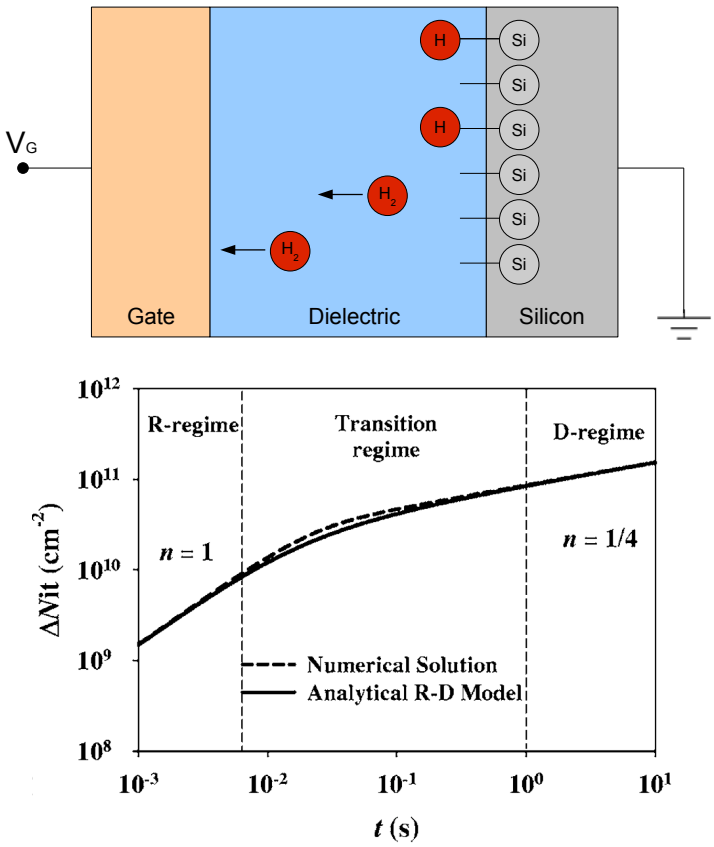


Figure 2.6: (*Top*) Illustration of the RD model: passivated Si-H bonds at the interface are broken and the hydrogen diffuses away into the dielectric, leaving behind electrically active interface traps. (*Bottom*) Interface trap generation calculated with the analytical RD model, showing the reaction and diffusion regimes of NBTI, after [63].

at which the interface traps are generated throughout the applied stressing time. In addition, the reverse process is also possible where the silicon dangling bonds are re-passivated by the free hydrogen.

According to the standard RD model, the electrochemical process at the channel interface can be modelled by the following rate equation:

$$\frac{\partial N_{it}(t)}{\partial t} = k_f(N_0 - N_{it}(t)) - k_r(N_{it}(t)N_x(0,t))^{\frac{1}{a}} \tag{2.6}$$

where k_f is the interface-trap generation and k_r is the annealing rate. N_{it} is the interface trap density, N_0 is initial pre-stress number of Si-H bonds, $N_X(0,t)$ is the concentration of diffusing hydrogen at the interface, and a is the order of reaction. The equilibrium of the forward reaction (interface-trap generation) and backward reaction (annealing) is governed by the hydrogen density at the interface $N_X(0,t)$. Consequently, the transport of the hydrogen away from the interface characterises the degradation, as manifested in the time-dependent shift of the transistor electrical parameters.

For the whole stress phase, the solution of the standard RD model consists of four different regimes. These regimes are characterised by different time exponents n for the degradation, as schematically depicted in Figure 2.7. Regime 1 is the very early and brief stage of the stress, which occurs when the amount of free hydrogen at the interface $N_X(0,t)$ is extremely low. The amount of already broken Si-H bonds at the interface N_{it} is also practically negligible. Therefore, Equation 2.6 is only limited by the forward reaction rate k_f :

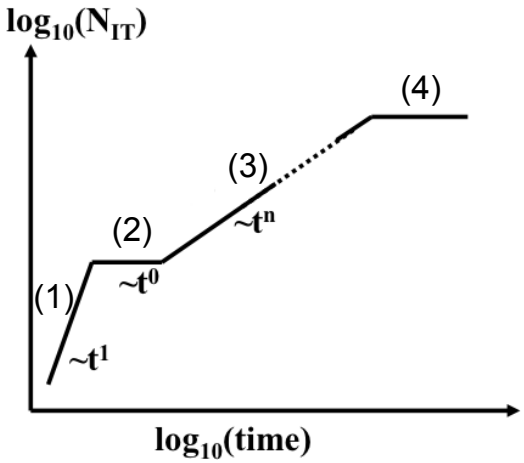


Figure 2.7: The schematic of 4 different regimes of the stress phase of the classical RD model of NBTI. Regime 3 is the most observed characteristic feature of NBTI stress, exhibiting the power-law stress time dependence of the degradation.

$$\frac{\partial N_{it}(t)}{\partial t} \approx k_f(N_0) \tag{2.7}$$

yielding a solution for the interface-trap generation:

$$N_{it}(t) \approx k_f(N_0)t \tag{2.8}$$

with the time exponent *n* in Regime 1 equal to 1. Regime 2 sets in when the hydrogen at the interface reaches considerable amount, and consequently the forward reaction reaches a quasi-equilibrium with the backward reaction:

$$k_f(N_0 - N_{it}) \approx k_r N_{it} N_x \tag{2.9}$$

As the initial available number of Si-H bonds N_0 is very large compared to N_{it},

$$k_f(N_0) \approx k_r N_{it} N_x \tag{2.10}$$

In this regime, a considerable amount of hydrogen has not yet diffused away from the interface, therefore the amount of interface traps equals the amount of hydrogen at the interface. Hence:

$$N_{it} \approx N_x \tag{2.11}$$

Rearranging Equation 2.10, this results in:

$$N_{it} \approx \sqrt{\frac{k_f N_0}{k_r}} \tag{2.12}$$

This time-independent equation can be rewritten as:

$$N_{it} \approx \sqrt{\frac{k_f N_0}{k_r}} t^0 \tag{2.13}$$

with the resulting time dependence $n = 0$. There is no further degradation of the interface as long as the diffusion of hydrogen away from the interface has not reached a considerable magnitude.

In Regime 3, the diffusion of hydrogen away from the interface sets in and acts as limiting factor for the degradation. This is the most prevalent regime in the typical

lifetime of a MOSFET. It sets in after some seconds of stress and, depending on the stress conditions, may last up to several years. However, reported power-law time exponents in the literature are widely varied, covering at least a factor of 5, from about 0.05 [68] to 0.25 [65, 69], and have been observed to exhibit dependencies on experimental conditions (e.g. stress-measure technique, on the fly technique) [68]. Other contradictory published data on this point also includes temperature dependence of n , which is either shown to increase with temperature [55, 68, 70], or to have no distinctive temperature-dependence behaviour [71].

After all interface bonds N_0 are broken, theoretically $N_{it} \approx N_0$, thus no further degradation can occur in this model. This is the Regime 4, which is the saturation phase. Therefore the rate of change in N_{it} and the time exponent n are zero. Once all of the possible interface states have been generated, the charge trapping is the only mechanism left which causes the parameter shifts. Subsequently, after the total possible charges have been trapped, the rate of degradation is expected to eventually cease.

2.2.2.3 Dynamic BTI: Frequency and Duty Cycle Dependencies

In a real operational routine of many CMOS circuits such as logic gates, the MOSFETs are constantly switched with alternating binary low and high voltage signals, and are thus exposed to a *dynamic* stress, as opposed to a constant, static DC stress. When the stress is relieved, the MOSFETs will immediately start to recover from the degradation (the electrical parameters partially return to pre-stress values), as will be further explained in Section 2.2.2.6. The recovery phase of the degradation is of particular importance in projecting a realistic functional lifetime of the circuits, because recovery provides added margin of lifetime as compared to the case when only static DC stress (hence, no recovery) is considered.

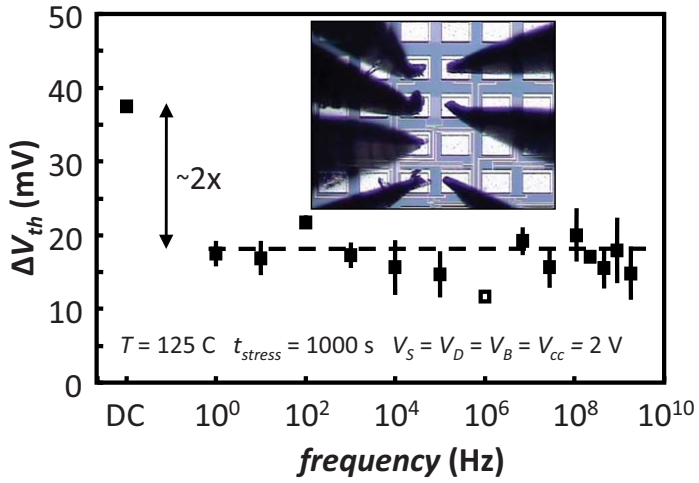


Figure 2.8: Threshold voltage shifts due to AC NBTI stress are seen independent of the applied frequencies. Threshold voltage shift due to DC stress measured from identical device is shown for comparison. Inset shows micrograph of on-chip circuit for the measurements consisting of a ring oscillator, a frequency divider, a buffer, a multiplexer and the device under test. After [72].

Figure 2.8 reports NBTI measurements [72] showing that the degradation is present at frequencies up to the gigahertz range. However, the magnitude appears to be independent of the entire range of applied frequencies of 1 Hz to 2 GHz. Also shown in the figure (leftmost location) is the magnitude of degradation in a similar device due to a DC stress, in comparison with the case of dynamic AC stress. The DC stress results in a magnitude of threshold voltage shift approximately 2 times larger than that of AC stress. AC signals thus reduce BTI with respect to the DC stress. This additional reliability margin can be factored in during the design phase, providing a more realistic projection of the circuit's functional lifetime.

In a digital circuit, the average length of time a signal being in the high state can vary between 0% to 100% over the entire cycle of the signal. The dependence of BTI on the stress signal's duty factor (DF) is shown in Figure 2.9 [72]. The shape of DF-

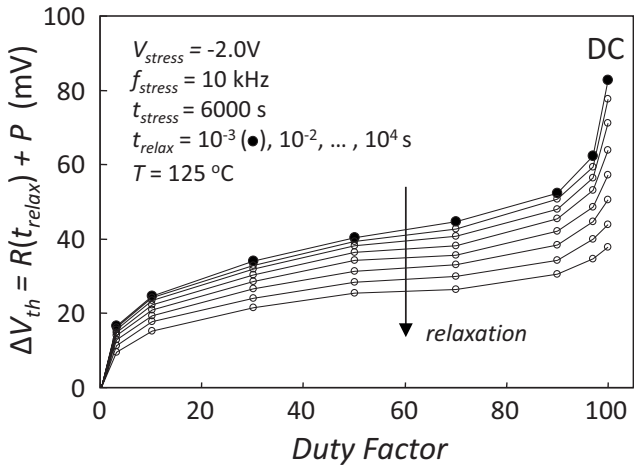


Figure 2.9: Total threshold voltage shifts consisting both *R* (recoverable) and *P* (permanent) components due to 6000 seconds of AC NBTI stress, at different relaxation times. Weak dependence on DF is observed from ~10% to ~90%, followed by a rapid increase of degradation for outermost DF values. After [72].

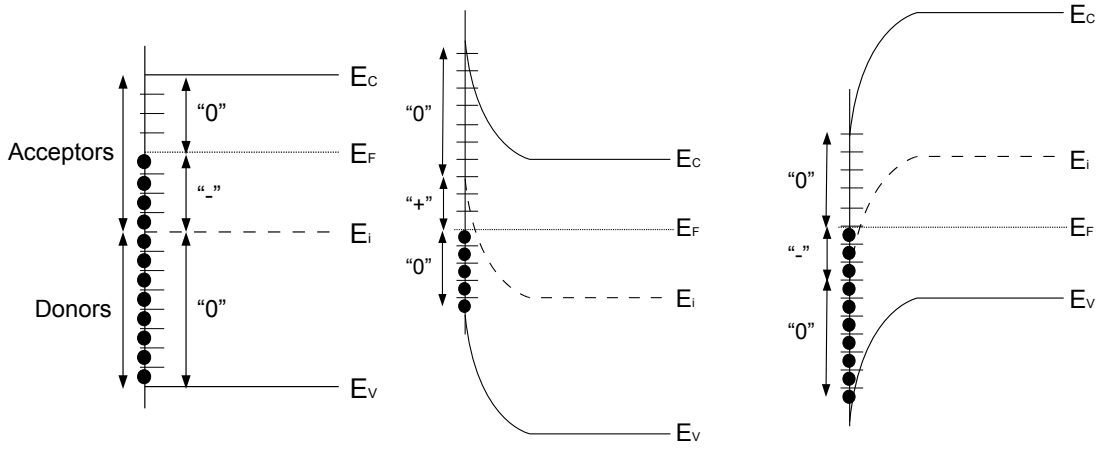
dependence is identical over many relaxation times, exhibiting a weak dependence or a sort of "plateau" between DF of 10% to 90% , and a rapid increase of threshold voltage shift when the stress signals are of the outermost values of DF. These recent reports suggest that in the case of a dynamic BTI, the magnitude of degradation is independent of the frequency of the applied AC signal, but the DF appears to have a more dominant impact on the degradation particularly at higher range of DF values approaching to that of a DC stress.

2.2.2.4 Types and Energy Distribution of the Traps

The generated interface traps are electrically active defects with energy distribution throughout the silicon band gap. The traps are acceptor-like in the upper half and donor-like in the lower half of the band gap [73]. Acceptor-like interface traps are electrically neutral when empty and negatively charged when occupied by electrons. Donor-like interface traps are positively charged when empty and neutral when

occupied by electrons. Hence, the occupancy of the traps determine their charge as illustrated by the band diagram in Figure 2.10(a) for the case of n-type substrate.

At flat band condition, the electrons occupy the interface states below the Fermi level, hence the donor-like traps become electrically neutral (designated by "0"), while the occupied acceptor-like traps between the Fermi level and mid gap are negatively charged (designated by "-"). The unoccupied acceptor-like traps above the Fermi energy remain electrically neutral. At strong inversion $\Phi_S=|2\Phi_F|$, a p-channel MOSFET has positively charged interface traps (designated by "+") attributed to empty donor-like defect states as illustrated in Figure 2.10(b), leading to negative threshold voltage shifts. Figure 2.10(c) shows the case for an n-channel MOSFET in strong inversion, where negatively charged traps are induced due to occupied acceptor-like traps, resulting in threshold voltage increase.



(a) (b) (c)

Figure 2.10: (a) Band diagram at flat band condition of an n-type substrate illustrating the occupancy of the two types of interface traps and the resulting charge polarities. (b) Positively charged interface traps at the strong inversion of a p-channel MOSFET. (c) Negatively charged interface traps at the strong inversion of an n-channel MOSFET. After [53].

2.2.2.5 Time Scales of the Traps: Similarity Between BTI and RTS Noise

The capture and emission time scales of BTI typically observed are widely distributed, exhibiting long, log(*t*)-like behaviour during both the initial portion of BTI degradation as well as in the recovery phase [72, 74]. This is shown in Figure 2.11(a), together with the *rate of degradation* $d\Delta V_{th}/dt_{relax}$ extracted from the ΔV_{th} NBTI relaxation transient, which follows $1/t_{relax}$ dependence for over 7 decades. This is a signature behaviour of states with discharging time constants covering many decades [19]. On the other hand, superposition of states with widely distributed time scales has always been the standard and widely accepted explanation of the 1/f noise spectra [20], as clearly observed in pMOFETs reported Figure 2.11(b).

This similarity leads Kaczer *et. al* in a recently published study [72] to argue that the same states play a fundamental role in both the NBTI and low-frequency noise as well their manifestation as RTS noise in deeply-scaled MOSFETs. This direct correspondence is supported by several other experimental observations, including the

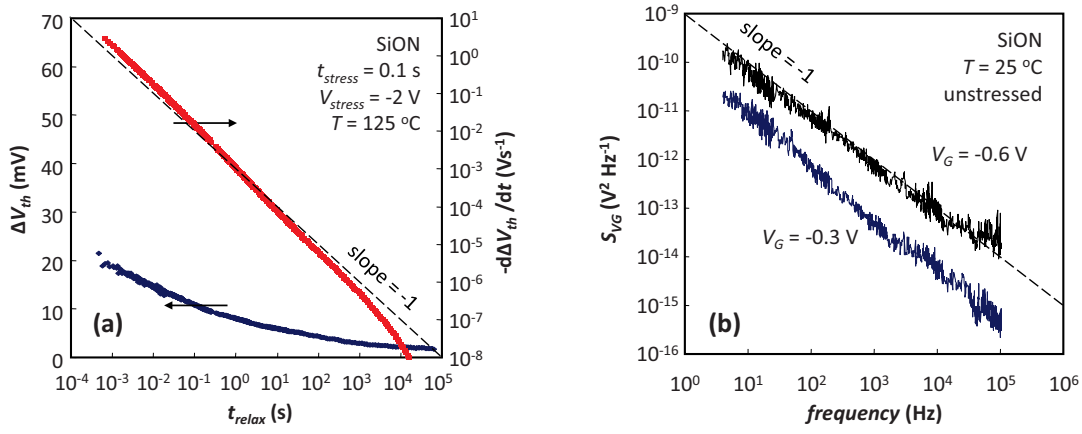


Figure 2.11: (a) The rate of recovery $d\Delta V_{th}/dt_{relax}$ extracted from the ΔV_{th} NBTI relaxation transient follows $1/t_{relax}$ for ~7 decades. (b) Gate-referred noise spectra measured on the same unstressed device shows a clear 1/f behaviour, which is widely accepted to be a superposition of states with widely distributed time scales. After [72].

substantial increase in both the log(*t*)-like relaxation component and the 1/f noise spectra as a result of nitridation of a (high-*k*) gate stack [75, 76], and the weak temperature dependencies of both the relaxation rate and the 1/f noise [77].

Based on this common property, Kaczer *et. al* [72] proposes an equivalent circuit as shown in Figure 2.12(a) to qualitatively model the states with the widely distributed time scales. In such a circuit, the states are modelled by resistance-capacitance elements with the total threshold voltage shifts of the MOSFETs being proportional to the sum of voltages across all of the capacitors. The two diodes with different parameters emulate different charging *i.e.*, capture and discharge *i.e.*, emission time constants of each defect. Such a circuit is found to correctly reproduce the experimentally measured DF-dependence reported in Figure 2.9, as shown in Figure 2.12(b), and also the log-like relaxation and the log-like initial phase of stress [78].

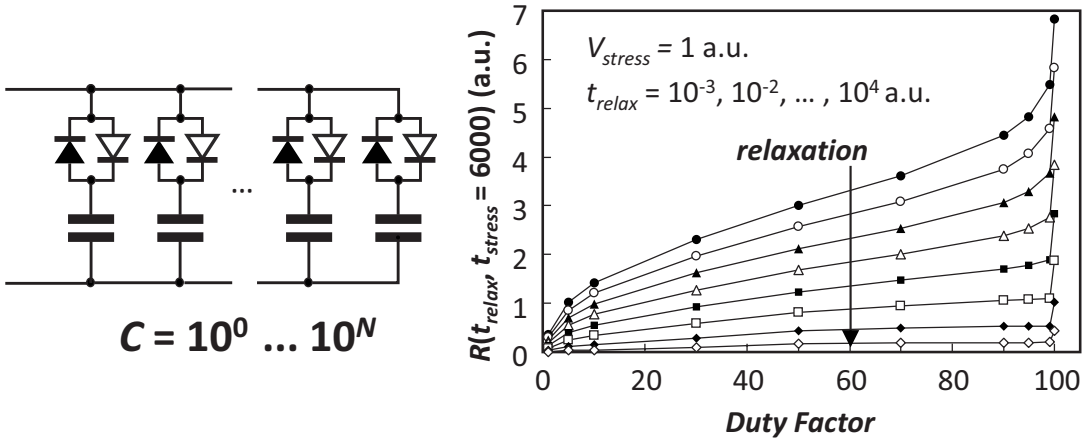


Figure 2.12: (a) The capture and emission time constants of traps are modelled by asymmetric diodes, while the total threshold voltage shift is proportional to the sum of voltages across the capacitors. (b) The experimentally reported DF-dependence of NBTI is qualitatively well-reproduced by the equivalent circuit over many relaxation times. After [72].

2.2.2.6 Recovery Effect

One of the most important aspects of BTI is the recovery behaviour, that is, when the stress is removed the degradation relaxes, as shown in Figure 2.13. The recovery effect is attributed to annealing of the interface traps by free hydrogen in the gate dielectric [55, 69], as well as charge detrapping/neutralisation [79]. From Figure 2.13 it can also be seen that during relaxation, the threshold voltage shift does not fully return to the initial, pre-stress value. This is because there are two different components of recovery, which are the recoverable component, and the final, non-recoverable (permanent) component. It is generally accepted that the permanent component of degradation is attributed to the generated interface states, while the recoverable part is caused by charge detrapping [70].

Recovery helps extend the device lifetime under AC stress, but it can also distort characterisation measurements [53]. This is because there is usually a time delay between the stress and characterisation; while it take many seconds to generate BTI damage, it subsequently recovers very rapidly within microseconds after the stress is

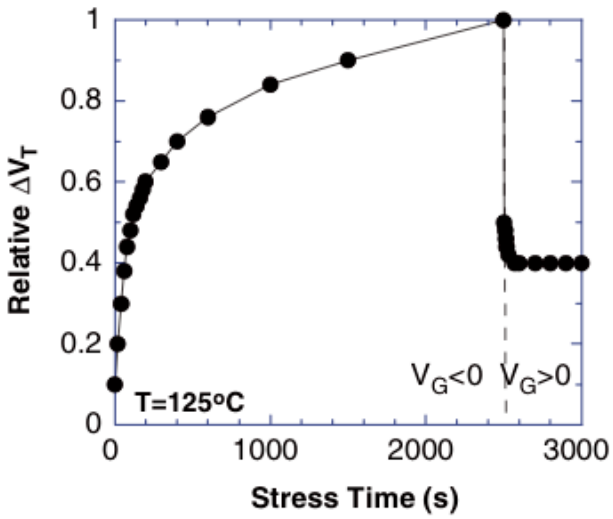


Figure 2.13: Relative threshold voltage shift due to NBTI as a function of stress time. After [53]. Recovery is observed after stress voltage is relieved ($V_G>0$)

lifted which results in inaccurate assessments of the extent of the damage. The recovery has been observed to show approximately logarithmic time dependence, with time scales ranging from ~ 10^{-6} to 10^{6} seconds [80-82].

2.2.2.7 BTI Characterisation Technique

Characterisation of BTI is done by means of an accelerated test condition, in which the MOSFET is stressed with higher gate voltages and temperatures than the intended operating conditions. The stress is periodically interrupted to measure the device parameters such as V_T, I_D and N_T . The interface trap density can be extracted by a variety of methods, one of which is called “charge-pumping” [83]. The method requires periodic pulses applied to the gate with the source and drain grounded. This setup drives the MOSFET to alternate between the accumulation and inversion conditions. During the inversion phase for the case of nMOSFET, electrons flood the channel area and some of them become trapped in the interface traps. When the gate pulse subsequently drives the nMOSFET into accumulation, the trapped electrons recombine with the holes flooding the channel, yielding a net substrate current flowing in the direction perpendicular to the channel. The same process occurs when the transistor is driven back to inversion, with opposite carrier types. The magnitude of this current depends on the number of available traps, which increases over time with the applied stress and therefore can be used to ascertain the trap density.

2.2.2.8 Statistical Aspects of BTI Degradation

With ever decreasing transistor sizes, statistical aspects of BTI degradation start to appear. In the past, when the relatively large MOSFETs of any given design were subject to similar use conditions, they were expected to degrade identically in terms of electrical performance. Accordingly, previous characterisation measurements, modelling and simulation efforts did not consider the variation in performance degradation due to stress. With progressive downscaling of MOSFETs, the application

of identical stress to an ensemble of small devices will result in a statistical distribution of performance degradation instead of a uniform response. Indeed, such variation of electrical parameter shifts due to BTI degradation has been recently reported for a large array of nano-scale transistors [70, 84].

Similar to random dopant fluctuations, the nature of the underlying charge-trapping process in BTI degradation is random and discrete. In very short channel transistors, variation in the number and spatial position of generated traps from device-to-device becomes relatively more significant, manifesting itself as clear variations in performance degradation. The randomness of the parameter shifts in identical transistors is a serious reliability concern in matched analog circuits such as current mirrors, which rely on strictly matched electrical characteristics of the transistor pair [85]. In digital circuits, signal processing may become corrupted if digital signals arrive earlier or delayed with respect to the latching clock edge, due to variation in transistor drive currents. The statistical aspect of degradation also means that the probability of a circuit to encounter a lethal failure mode increases as the number of circuit transistors increases — with millions of transistors subjected to the stress, a small number are likely to generate extremely large parameter shifts.

For the case of RTS noise, simulation studies have already demonstrated that the inclusion of random dopant effects is essential for reproducing both the shape and the magnitude of the experimentally observed RTS amplitude distributions [35, 48-51, 86]. The same charge-trapping phenomena which leads to RTS noise underlies the BTI degradation — in the presence of the same primary source of intrinsic variability. It is therefore likely the inclusion of random dopants in a study of BTI degradation will lead to deeper insights into BTI, which is already industrially important, and, as discussed above, will become more important as devices continue to shrink. In addition, as the effects come from the similar root cause, the same simulation tools to those used in the investigation of RTS noise can be profitably applied to BTI

investigations. As a final benefit to using the same simulation toolset, it will be possible to study the impact of the progressive increase in trapped charge (characteristic of BTI) on the initial pre-degradation V_T variation dictated by the random dopants, and the correlations between the pre- and post-degradation distribution of electrical parameters.

2.3 Summary

This chapter has discussed the growing impact of random dopant fluctuations on the electrical characteristics of scaled down transistors. Previous simulation studies have suggested that this dominant source of intrinsic variability is responsible for the wide distribution and anomalously large RTS amplitudes measured from physical experiments. The most recently published experimental measurements suggest that the same defects responsible for RTS noise is also the underlying mechanism involved in BTI. However, random dopants effects have not been considered and studied in detail for the case of BTI degradation, despite the identical nature of the underlying process to that of RTS noise.

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Chapter 3

Simulation Methodology

3.1 Introduction

This chapter outlines the most established methods employed in the simulation of modern semiconductor devices. The strengths and drawbacks associated with each method, with specific pertinence to the aims of this study, are discussed. These comparisons are then summarised and presented as a justification for the particular simulation technique adopted for this work. Finally, the implementation details of the software chosen and developed to carry out our specific simulations are presented, along with a description of the testbed device selected for simulation.

3.2 Simulation Techniques

There are a number of different techniques available for semiconductor device simulation. Each may be differentiated by the nature and complexity of the underlying physical methods and models, the corresponding accuracy which can be achieved for device parameters of interest, as well as the associated computational costs. To select the method which will best suit the objectives of this work, key features pertaining to these different approaches must be benchmarked against the research specific requirements.

A key objective of this work is to study the impact of trapped charges in the presence of intrinsic parameter fluctuations introduced by random discrete dopants. These

effects are inherently three-dimensional in nature due to the granularity of matter and charge. It is therefore essential that the particular simulation technique employed could properly resolve discrete impurities and trapped carriers in real space in order to produce accurate simulation results. The proper treatment of discrete charges is also imperative because their number and spatial arrangement exert a significant influence on the electrical characteristics of a highly-scaled transistor [1].

The second requirement arises out of the statistical nature of intrinsic parameter fluctuations. It is obviously a monumental task to exhaustively simulate a complete population of microscopically different transistors by considering every possible configuration of the random discrete dopants and trapped charges. The conventional practice is to simulate a sufficiently large sample of devices so that the statistical parameters characterising the distribution can be extracted with an acceptable level of accuracy. As an indication of the computational efforts involved, to obtain a ~5% error in the estimate of the standard deviation of a particular device figure of merit such as the threshold voltage, a statistical sample of approximately 400 microscopically different transistors have to be simulated. This requires the simulation technique adopted by this work to be relatively fast and efficient, allowing a simulation of a large statistical ensemble of transistors within an acceptable time frame. Since we are analysing these effects for given device designs rather than using the results to optimise those designs, a turnaround simulation time of the order of days is reasonable. Under these constraints serial simulation times of 2-3 minutes per I_D value are required.

Due to the underlying assumptions in its physical model, a simulation technique which is accurate and sufficient when applied to one particular mode of transistor operation may be inaccurate in terms of capturing important physical details when applied at different bias conditions. Most of the reliability studies of charge-trapping-related degradations are concerned with the shift in threshold voltage induced by the

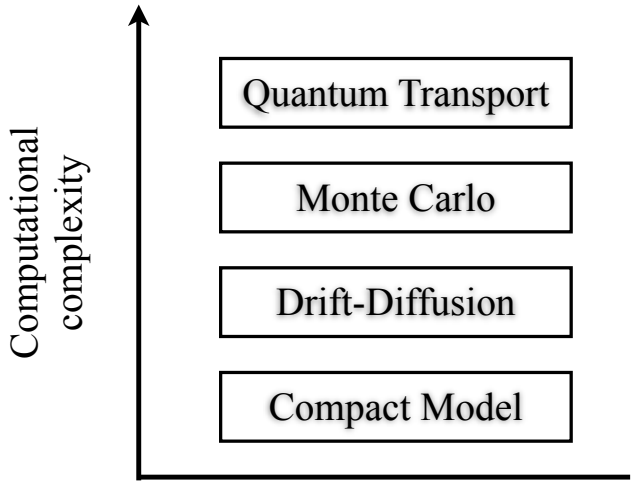

Figure 3.1: Simulation approaches available in the Glasgow Device Modelling Group and their hierarchical order of computational complexity.

trapped carriers [2-7]. To measure these shifts, it is necessary for the simulation technique adopted to accurately capture the important physical effects within the sub-threshold regime of the device operation. This ability to accurately simulate the device in the sub-threshold regime is the third of the key requirements for selecting the simulation technique to be used in this work.

Figure 3.1 depicts the hierarchy of well-established simulation approaches [8] currently available in the Glasgow Device Modelling Group, ordered according to their computational complexity. At the bottom of the hierarchy lies the compact model approach. Compact models are most useful in circuit-level simulations, in which a system of inter-connected building blocks of transistor and passive devices is modelled by linking device compact models together. A compact model essentially treats the semiconductor device it represents as a black box component by relying on semi-analytical expressions and fitting parameters to reproduce the transistor current-voltage characteristics. Such simplification enables large-scale simulations involving thousands of transistors to be completed in minutes. Despite the enormous

computational efficiency, compact models offer little physical insight into device operation and are therefore not particularly useful for studying the physical effects of trapped charges and random discrete dopants on the electrical characteristics of transistors.

The quantum transport approach which models transport phenomena based on the wave-like nature of sub-atomic particles, resides at the top-most level in the hierarchy due to its overwhelming computational complexity. Quantum transport simulations are required at the extremes of device scaling where quantum effects dominate and semi-classical approaches lose validity [9]. At below 10 nm channel lengths, quantum transport simulations become a necessity [10]. A quantum transport-based simulation approach is not suited to this study because it is computationally prohibitive to simulate the 35 nm gate length testbed device chosen in this work, even for single device simulations. Additionally, studies in [11, 12] demonstrate that the inversion layer quantization effects in a 30 nm gate length transistor and the corresponding increase of threshold voltage can be captured with sufficient accuracy by semi-classical approaches. In between these extreme ends of the hierarchy are simulation techniques which attempt to capture important physical details at varying levels of computational complexity. The following section reviews these two different approaches with respect to the aforementioned requirements of this work.

3.2.1 Drift-Diffusion

The drift-diffusion (DD) approximation is the simplest charge transport model derived from Boltzmann transport equation (BTE) [8]. Consider the case for n-channel MOSFETs, unipolar devices whose terminal current is determined by the transport of electrons. A steady-state DD simulation approach for such a device involves self-consistently solving Poisson's (Equation 3.1) and current-continuity (Equation 3.2) equations until convergence in the current solution is met.

$$\nabla \cdot (\epsilon \nabla \psi) = q\left(n - p + N_A^- - N_D^+\right) \tag{3.1}$$

$$\nabla \cdot J_n = 0 \tag{3.2}$$

N_A^- and N_D^+ are acceptor and donor concentrations, ε is the dielectric permittivity, n and p are electron and hole concentrations, and q is the elementary charge. The solution of Poisson's equation yields the electrostatic potential, Ψ , which is then included in the calculation of electron current density, $\boldsymbol{J}_{\mathrm{n}}$. The DD model of charge transport represents the electron current density as a superposition of carrier drift and diffusion.

$$J_{\mathbf{n}} = qD_n \nabla n - qn\mu_n \nabla \psi \tag{3.3}$$

The first term on the right represents the diffusion current which is a motion of carriers due to a gradient of its concentration in the system, where D_{n} is the electron diffusion coefficient which is related to electron mobility μ_{n} and temperature T via Einstein's relation $D_{\mathrm{n}} = \mu_{\mathrm{n}} (k_B T / q)$, where k_B is Boltzmann's constant. The second term describes the drift current which is a motion of carriers driven by an electric field.

The DD model derivation is based on a string of significant simplifying assumptions in the BTE [13] and these place a limit on its validity. The applicability of the DD approach can be empirically extended by the use of mobility models for the channel electrons with doping and electric field dependencies [14], and the incorporation of quantum corrections [15] to model quantum confinement effects in ultra-small devices. Even with these refinements, the DD approximation is still strictly valid only for devices with slowly varying electric fields, as it assumes that the carriers are able to respond instantaneously to changes in the field. In reality, the lateral field in a short channel length transistor varies rapidly, and the carriers require a finite time and distance to respond to the field. Under such condition the carrier velocity overshoots

the saturation velocity which consequently leads to a current increase—a transport effect not accounted for in the DD model [9, 13]. DD approach is found to well model transistor's on-current of gate lengths down to 40 nm, with less than 10% difference from the more accurate and computationally expensive Monte Carlo simulations [16].

When considering 'atomistic' devices, DD simulation inherently accounts for the electrostatic modulation of carrier density by the potential of the ionized discrete impurities, via the solution of the Poisson's equation. However, discrete impurities and interface-trapped carriers also act as Coulomb scattering centres which affect charge transport. In this respect, a DD simulation underestimates the current variations from device to device because its mobility model, based on bulk values, is insensitive to the variation of number and position of scattering centres in the device. It has been demonstrated by Monte Carlo simulation featuring "*ab-initio*" ionized impurity scattering, that transport variation due to position-dependent Coulomb scattering results in a significant increase of current variation, in addition to the electrostatic modulation of carrier density that is alone captured by DD simulation [17]. The study reveals that transport variations contribute approximately 45% of the total drain current variation for 35 nm gate length transistor estimated from self-consistent Monte Carlo simulation, which implies that DD simulation only captures 55% of the total variation by failing to include transport variation [17].

Despite its shortcomings, a DD approximation is still perfectly adequate when applied in the sub-threshold regime where the lateral field exerts a relatively minor influence on the diffusion-dominated charge transport. In this instance, the height of the potential barrier separating the source and drain is sufficiently high that little mobile charge inhabits the channel. The height of the barrier, which is controlled by the gate voltage, determines how much charge is able to diffuse into the drain. Under these conditions, the resulting current is essentially a function of carrier density governed by the gate electrostatics, rather than carrier drift controlled by the lateral field. A major

advantage of the DD approach lies in its efficiency and easy numerical implementation. The relatively short simulation time required to completely analyse the current-voltage characteristics of a single sub-micron transistor—typically on the scale of hours—clearly makes a DD-based simulator a competitive tool to be considered in a simulation of a large statistical ensemble of devices.

3.2.2 Monte Carlo

Monte Carlo (MC) methods are a general class of computational algorithms characterised by the use of repeated random sampling to model a physical or mathematical system. MC simulation offers a numerical solution of the BTE by simulating charge transport in a fundamentally different way to that of the DD approach. The MC method traces the actual real space trajectories of carrier particles throughout a simulation period; trajectories described by a series of field-driven free-flights intercepted with scattering events as illustrated in Figure 3.2. Scattering events can include carrier interaction with phonons, fixed impurities and other carriers.

A typical flow of MC simulation starts with initialisation of the system, with initial

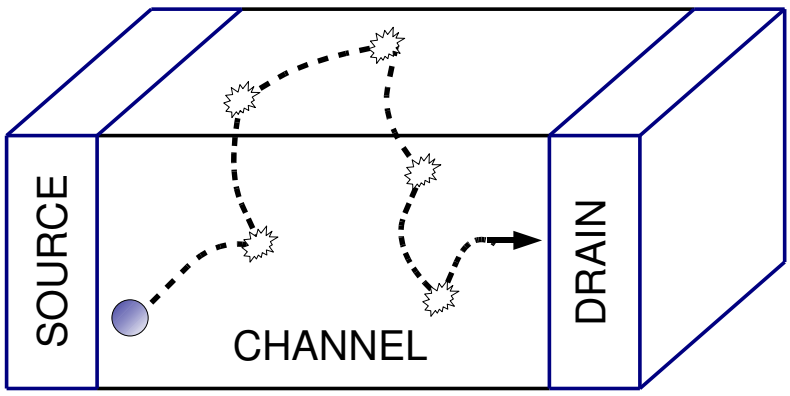

Figure 3.2: Illustration of a charge carrier travelling from source to drain being randomly scattered in between periods of free-flight in a Monte Carlo simulation.

conditions often obtained from the output of a simpler simulator, such as a DD simulator. The carriers are then propagated under the influence of the initially calculated electric field. For each carrier, a period of free-flight is ended by a scattering event, and the free flight period, scattering event, and post scattering event carrier velocity and direction are stochastically determined by random numbers with suitably adjusted, physically relevant probability distributions. An important step at this stage is the gathering of carrier data such as velocities and other quantities of interest. The particle movement can now be coupled with Poisson's equation to allow update of the electric field driving the carriers. This flight-and-scatter processes are then repeated until the quantities of interest converge, and the convergent values can be extracted with sufficient precision.

The MC procedure, which tracks the microscopic physics of individual carrier motions, results in an improvement in physical accuracy over the DD method, which is based on the average properties of the charge transport system. MC simulation is capable of capturing non-equilibrium transport effects for rapidly spatially varying fields such as velocity overshoot [9, 18]. Such effects are relevant, as the disproportionate scaling between supply voltages and device geometry is continuously increasing the on-state electric field from technology generation to technology generation, resulting in electric fields which rapidly vary over the device's short length scales. In 'atomistic' device simulation, the transport variation associated with the Coulomb scattering of ionized discrete impurities and interface-trapped carriers is properly considered through the real space trajectories of the carriers. Additionally the carrier density modulation by the ionized fixed impurities is inherently accounted for by coupling the carrier movement to Poisson's equation. These advantages make an MC-based simulator naturally suited for characterising the impact of discrete dopants and trapped charges on the drive current.

The improved physical accuracy delivered by MC approach comes at the expense of

significantly larger computational overhead. MC simulations require extended simulation times in order to gather reliable data in the presence of statistical noise, which is particularly large in the sub-threshold regime where the number of carriers and scattering events are low. For this reason, MC is not an efficient tool for extracting threshold voltage changes induced by trapped charge. In general, the long simulation times of MC simulations, often spanning days or weeks (instead of the more acceptable scale of hours) renders the MC method ill-suited to large-scale statistical simulation of devices.

3.2.3 Cost-Accuracy Analysis

The general review of MC and DD simulation techniques is concluded in this section with a summary of their relative accuracy and computational costs. Figure 3.3 shows the I_D-V_G characteristics of a uniform 22 nm gate length MOSFET, computed using

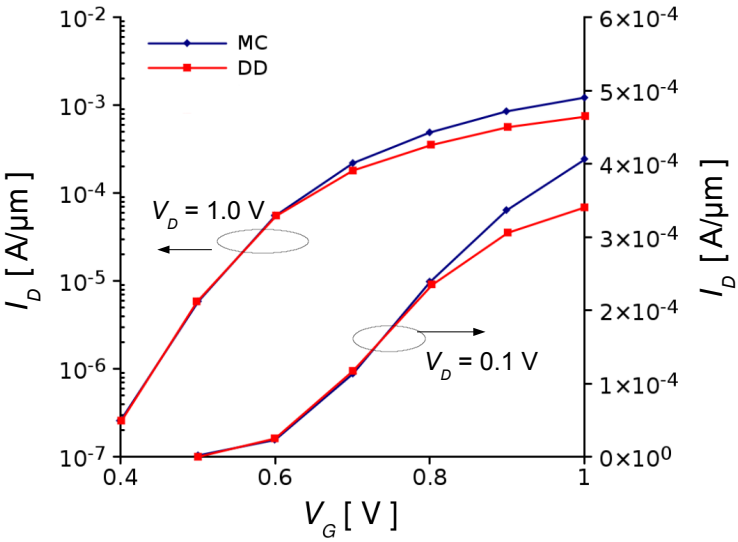

Figure 3.3: Comparison of I_D-V_G characteristics from MC and DD simulations of the same device. DD current is markedly lower at high drain bias but compares well against MC simulation at low drain bias. (*Data courtesy of S. Markov, C. Alexander and A. R. Brown*)

MC and DD simulations. Currents at high drain bias (V_D = 1.0 V) are plotted on a logarithmic scale with reference to the left vertical axis, while the low drain bias (V_D = 0.1 V) *IV* curves are plotted on a linear scale with respect to the right axis. Unfortunately, the MC approach cannot be used in the deep sub-threshold regime due to the large statistical noise associated with very low carrier density and scattering events, requiring excessively large simulation times to accumulate sufficient statistics in order to accurately estimate the sub-threshold current. Thus, to ensure a reliable and fair comparison, both MC and DD simulations are applied with gate voltages ranging only from 0.4 V to 1.0 V, as shown in Figure 3.3. At this bias range where a considerable number of carriers already populate the channel, a lengthy but tolerable computation time of approximately 10 days per IV point is needed to gather the sufficient statistics, allowing the MC simulation to be reliably compared against the DD counterpart.

It can be seen that the current from DD simulation tends to be lower than that from MC simulation. This is because the DD current is limited by velocity saturation and this effect is noticeably stronger at high drain bias. However, at low drain bias, both methods are in good agreement for the entire range of applied gate voltages. Similar *IV* characteristics from both simulations are also observed at high drain voltage when the applied gate bias is kept low. This is because at low gate voltages corresponding to weak inversion conditions, the resulting current is largely due to carrier diffusion whose magnitude is governed by the electrostatic conditions of the device. These can be captured by the relatively simpler DD simulator just as well as in the more rigorous MC simulator.

Because this work is primarily focused on the impact of interface-trapped charge as measured by the induced threshold voltage shift, the superior accuracy of MC simulator which lies above threshold current condition is of little relevance. Additionally, it has also been demonstrated that in the sub-threshold regime the effect

of a single interface-trapped charge is predominantly as result of electrostatics (via carrier density modulation) rather than being transport-related (via scattering) [19]. These comparisons lend a strong confidence to the accuracy of the DD simulator for the purpose of studying the impact of trapped charges when the bias conditions are kept in the above-specified conditions. In terms of computational cost, the DD simulator typically takes a few minutes to compute an *IV* point of the simulated structure, while the MC simulator running on the same CPU typically requires approximately 10 days per *IV* point. In summary, these comparisons present a clear justification to adopt the relatively fast and reasonably accurate DD simulation technique to fulfil the requirements of this study.

3.3 Glasgow 'Atomistic' Device Simulator

This section describes the simulation framework used in this study, which is the 3D 'atomistic' device simulator developed over more than 10 years by the Glasgow Device Modelling Group. The simulator was first used in 1998 for an extensive simulation study of random-dopants-induced threshold voltage fluctuations in sub-0.1 micron nMOSFETs [20]. It has since been employed to study MOSFET intrinsic parametric fluctuations introduced by gate line edge roughness [21], microscopic oxide thickness fluctuations [22] and combined various sources of intrinsic fluctuations [23]. A more detailed account of its development and internal operating mechanism is described in [23, 24]. The simulator self-consistently solves the Poisson (Equation 3.1) and current continuity (Equation 3.2) equations within the drift-diffusion approximation. These equations are discretised onto a fine three-dimensional Cartesian grid of 1 nm mesh spacing to ensure the steep variation of potential fluctuations from the random discrete dopants are properly accounted for.

Quantum mechanical effects exert an increasingly significant influence on ultra-small device characteristics. An important quantum effect is the quantisation of inversion

charge distribution which has the equivalent effect of increasing the oxide thickness as the peak carrier concentration is pushed away from the interface, leading to an increased threshold voltage than might be expected from a purely classical analysis [25]. To account for this quantum confinement effect, the classical DD model can be extended by incorporating quantum corrections. This Glasgow 'atomistic' device simulator incorporates the Density Gradient (DG) formalism whose derivation is described elsewhere [15]. DG quantum corrections have the effect of altering the DD electron current density due to an additional driving force related to the gradient of the carrier density;

$$J_{\mathbf{n}} = qD_n\nabla n - qn\mu_n\nabla\psi + 2q\mu_n\nabla\left(b_n\frac{\nabla^2\sqrt{n}}{\sqrt{n}}\right) \tag{3.4}$$

where b_n is density gradient dependence parameter. Note the additional term has a form similar to the diffusion current component $qD_n\nabla n$, in the sense that both currents are driven by the gradient in carrier concentration, n. In the simulations, the inclusion of the additional driving term has the effect of pushing the peak carrier concentration away from the oxide interface, which reproduces the quantized carrier distribution in the channel and is consistent with the solutions obtained from 1–D Poisson-Schrödinger simulation [11]. In addition, the introduction of DG quantum corrections is also useful in alleviating some of the problems associated with the introduction of discrete impurities in classical DD simulation described in Section 3.3.1. In a classical DD approach, the majority carrier concentration will become erroneously localised in the deep potential wells of the ionised discrete impurities. With DG quantum corrections included, the same force which pushes the peak carrier concentration away from the interface also exerts a similar effect around the discrete impurities, which helps to prevent this artificial carrier localisation [11].

3.3.1 Modelling Random Discrete Dopants and Trapped Charges

There are two important aspects in correctly simulating systems involving discrete

impurities. Firstly, the distribution of discrete dopants must represent a given doping concentration profile; secondly, the charge of the ionised impurities must also be properly resolved to produce physically-consistent solutions. The 'atomistic' simulator adopts the dopant placement technique first proposed by Frank *et. al* [26], which allows implementation of arbitrary non-uniform doping profiles on the simulation meshes. For a given device structure, the simulator generates silicon lattice sites independently of the numerical discretisation grid. A random number is then generated at each of these lattice sites. The probability of finding a dopant atom at a given lattice site is computed from the ratio of the desired local doping concentration and the intrinsic silicon concentration. A dopant atom will replace a silicon atom if this probability exceeds the random number generated for the lattice site.

Because dopant placement is referenced to the silicon crystalline lattice, the resulting dopant positions do not match the discretisation grid nodes. It is therefore necessary to methodically assign the doping from each impurity atom to adjacent grid nodes as it will be included in the Poisson equation via N_A^- and N_D^+ , which are position-dependent for non-uniform doping profile. The doping density of a single dopant atom is related to $1/V$, where V is the elemental volume of the mesh cell. The 'atomistic' simulator distributes this density to the neighbouring 8 grid nodes of a mesh cell using the Cloud-in-Cell method [27] illustrated in Figure 3.4. This technique assigns a fractional magnitude of the doping density to a grid node based on the distance between between the node and the dopant atom, as given in Equation 3.5.

$$\rho(x, y, z) = w_x w_y w_z \frac{1}{V} \tag{3.5}$$

ρ is the doping density of a grid node at position (x, y, z) and w_x, w_y and w_z are weight factors given by Equation 3.6.

$$w_x = \begin{cases} 1 - |x_i - x_g| & |x_i - x_g| \leq 1 \\ 0 & otherwise \end{cases} \tag{3.6}$$

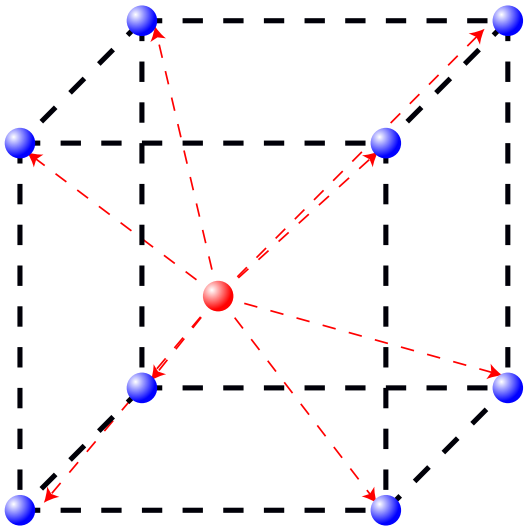

Figure 3.4: The Cloud-in-Cell charge assignment splits the doping density of an impurity atom (red sphere) to the 8 grid nodes of a mesh cell. After [24].

Equation 3.6 demonstrates the weighting factors depend on the distance between the position of the dopant atom x_i and the grid node x_g. Therefore the closer a grid node is to a dopant atom, the larger the doping density is assigned to that point.

In our simulations, we assume that the charge carriers − electrons, in the case of our n-channel template device − are trapped only at the Si/SiO_2 interface. In reality, the carriers may be trapped deeper into the gate oxide [28, 29], and a previous simulation study [30] has shown that the trapping distance (measured from the Si/SiO_2 interface) affects the magnitude of the resulting current reduction. This is because as a charge is trapped deeper into the gate oxide, the impact of its Coulomb potential on the surface potential in the channel is reduced, thus the magnitude of the resulting current reduction is less pronounced compared to the case the charge is trapped nearer to the channel. For simplicity, these effects are not taken into account in our simulations. Nevertheless, despite these necessary simplifications, our simulations are able to reproduce a few major features of the experimentally measured characteristics of

NBTI/PBTI degradation, as will be discussed in Chapter 5.

In our work, an interface-trapped electron is modelled by assigning a single electronic charge to a randomly-determined point at the Si/SiO_2 interface plane. Similar to the case of a doping impurity, the sharp potential spike associated with the singularity of the Coulomb potential of the trapped charge is resolved using the well-established Density-Gradient (DG) formalism. The effective quantum potential applied by the DG correction ensures physically-consistent solutions of the electron concentration surrounding a discrete charge, while simultaneously taking into account the screening effect. The DG quantum correction renders unnecessary the conventionally used approach of splitting the Coulomb potential into short- and long-range components based on screening considerations [31, 32], which suffers from several drawbacks including arbitrary choice of the short-long range cut-off parameter, and inability to account for the change in the screening in the channel with the change of the gate bias and the inversion carrier concentration. The DG quantum correction is also the most physically accurate and computationally efficient method [23, 33] to account for quantum effects in conventional drift-diffusion simulations, without resorting to a computationally-prohibitive, full quantum transport solution. To ensure physical accuracy, the parameters used by the DG quantum correction in our simulator have been carefully calibrated and verified [34, 35] against a more rigorous 3D quantum transport simulation based on Non-Equilibrium Green's Functions (NEGF). Through such calibrations, not only does our quantum-corrected drift-diffusion simulation able to reproduce the carrier quantization effect at the MOSFET channel interface, but it also agrees very well with the NEGF-based solutions of the electron concentrations around localised discrete charges associated with stray dopants and trapped carriers, over a wide range of bias conditions [34, 35]. These prevent the unphysical localisation of carriers in the deep potential wells of the ionised impurities, thus avoiding artificial increase of the channel resistance [23]. These thorough validations give confidence that discrete charges and trapped carriers in our simulated systems are

properly treated with quantum mechanically-consistent description of charge distribution in nano-scale MOSFETs.

The introduction of discrete impurities and trapped charges into the continuum world of classical drift-diffusion simulation also results in a few other inter-related problems. The charge assignment method explicitly relies on the mesh spacing used; for a finer grid the doping density of a dopant atom $1/V$ increases as the elemental volume decreases. This strongly localised doping density creates a deep potential well for the majority carriers within its vicinity which will be strongly attracted and localised in it [36]. This would in turn reduces the number of free carriers otherwise available for conduction and artificially increases the resistance of the device. The localised carrier concentration depends on the depth of the well, which is in turn determined by the mesh spacing used. If a finer grid is used the singularity of the Coulomb potential of the dopant atom is more sharply resolved, which increases the localised carrier density. These effects introduce an undesirable mesh-dependent aspect into the solution generated by the simulator.

These issues are managed in a quantum-mechanically consistent way. The DG quantum correction incorporated within the 'atomistic' simulator results in a significant reduction of the amount of mobile charge localised around an ionised discrete impurity. This reproduces the effect of quantisation within the steep potential well of the impurity [37]. In addition, the quantum-corrected electrostatic potential and electron concentrations are less sensitive to the mesh spacing than the corresponding classically computed distributions, with negligible differences when a mesh spacing of 1 nm or below is used [24]. These measures remove the artificial conductance degradation due to mobile charge localisation, and generate mesh-independent *IV* characteristics.

As previously covered in Chapter 2, the NBTI/PBTI degradation is a time-dynamic

and complicated process. The time-dependent aspect of the degradation has been extensively observed in the capture and emission times of the charges [38, 39], in the trap generation rate which is exponentially related to the applied stress-time [28, 40], as well as in the recovery effect after the device is relieved off the stress [3, 4]. On the other hand, the location of the trap itself may be influenced by the underlying distribution of individual dopants in the channel. This may be the result of individual impurities near the channel interface moderating the Fermi level within their immediate surroundings, which in turn cause local variations of energy distribution of the traps, leading to the location of trapped charges being correlated with the distribution of the individual channel dopants. In addition, under other stress conditions such the Hot-Carrier Injection stress, the carriers are trapped in a spatially non-uniform manner throughout channel interface because as a carrier accelerates towards the drain, it gains excess energy which enables it to surmount the potential barrier of the oxide relatively easier near the drain side of the channel [41].

Undoubtedly, the kinetic details of the degradation process are important in understanding the phenomena as new, refined models of the process are developed by the research community. Unfortunately, for the purposes of this work, it is impossible to track the time-evolution *IV* characteristics of each device in our simulation ensemble of 1000 microscopically unique transistors, due to the enormous computational costs which such a feat demands. This practical limitation does not allow us to simulate the time-varying aspect of BTI involving the trapping/detrapping and trap generation processes, as well as the recovery effect. However, we have developed an alternative, *frozen-in-time*, statistical approach of describing the progressive degradation, by taking statistical snapshots of the degradation represented by different increasing levels of sheet densities of the trapped charge. Four sheet densities — 1×10^{11} cm^{-2}, 3×10^{11} cm^{-2}, 5×10^{11} cm^{-2} and 1×10^{12} cm^{-2} — are selected to represent the early, intermediate, and later ageing stages. For each level of degradation, the exact number of trapped charges in any particular MOSFET in the

simulation ensemble is randomly chosen based on a Poisonian distribution with its mean determined by the sheet density. The location of each of these trapped charges is randomly chosen at the Si/SiO_2 interface. At this point, another simplification is introduced by neglecting possible correlations of the location of the trapped charges and the underlying distribution of channel dopants. As an overall result, both the number of trapped charges and their individual locations differ from device-to-device. For each level of trapped charge sheet densities, a statistical sample of 1000 microscopically different devices is simulated. This statistical manner in which of trapped charges are implemented in the simulations is explained with more details in Chapter 5.

Clearly, our approach of modelling the spatial distribution of the traps and time-evolution aspect of BTI introduces a distinct level of simplifying assumptions. These simplifications are, however, necessary in order to allow the statistical aspects of the degradation to be analysed. Our approach has been recognised as a very useful engineering approach for circuit designers to check to what extent their designs will work under progressive BTI degradation, while being simultaneously aware of the design constraints put forward by the statistical variability of the transistors [42]. The same approach has been adopted in three European-funded research collaborations (Reality, Trams, Modern) [43], and has also been recently verified with respect to experimental measurements, capable of reproducing both the qualitative and quantitative details of the degradation [44], as will be discussed in Chapter 5. The results of this well-adopted approach have also been published in reputable well-ranked journals [42, 44-46] and reported at important reliability conferences [47, 48]. Of course, any modelling approach can be further elaborated to include ever finer details of the degradation process, and there is an intention to implement a more refined NBTI/PBTI model in our Glasgow ‘atomistic’ simulator, but at the moment and for the purposes of this Ph.D work, we will adopt the approach with the afore-mentioned assumptions.

3.3.2 The Simulated Device

In order to realistically assess the impact of trapped charges, the simulated MOSFET should be as realistic as possible. The testbed device used in this work is based on a 35 nm physical gate length, n-channel bulk MOSFET fabricated and reported by Toshiba in 2001 [49]. It has a poly-silicon gate and silicon oxynitride gate dielectric with EOT of 0.88 nm. Figure 3.5 shows the 2D net doping profile of the device, generated using the commercial Taurus Process and Device simulator [24, 50]. The doping design features a retrograde channel doping with shallow source and drain extensions to suppress punch through and other short channel effects.

To ensure simulation accuracy, the 'atomistic' simulator has been carefully calibrated to match commercial TCAD simulation and experimental measurements. The calibration procedure which is described in full detail elsewhere [24, 51], involves tuning of the parameters in the Caughey-Thomas mobility model [14] used by the

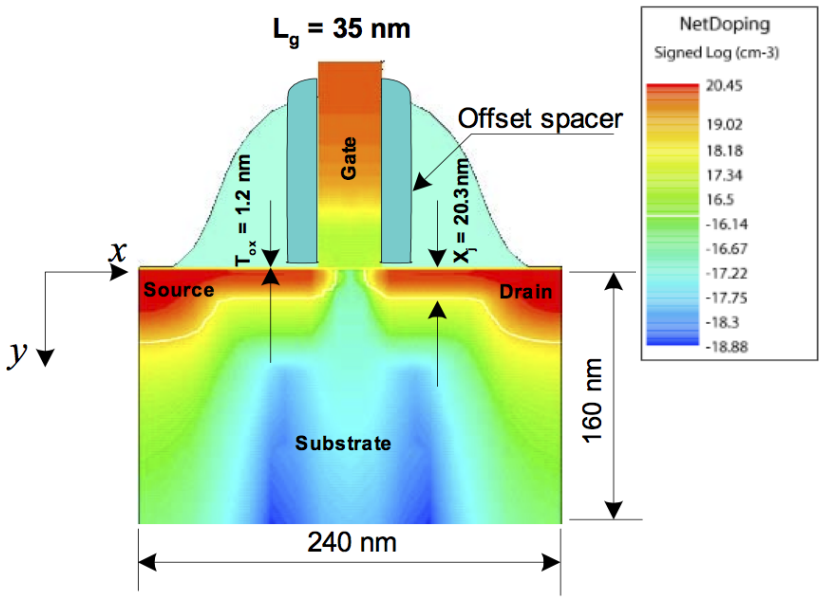

Figure 3.5: The 2D doping net doping profile of the template device used in this study. After [51].

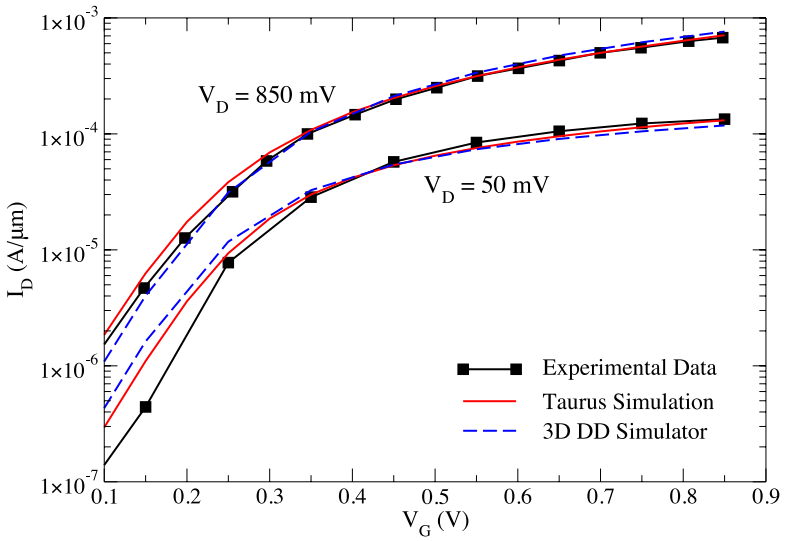

Figure 3.6: The experimentally measured I_D-V_G characteristics of the 35 nm Toshiba MOSFET compare well with the characteristics obtained from the TCAD and 'atomistic' simulator. After [24].

'atomistic' simulator, in which the mobility depends on both the doping concentration and electric field. Figure 3.6 compares the device's experimentally measured I_D-V_G characteristics against those obtained from simulations, demonstrating a good agreement and the capability of the 'atomistic' simulator to closely reproduce the device characteristics. In an 'atomistic' device simulation, the testbed device is randomly populated with discrete dopants based on the continuous doping concentration profile imported from the Taurus simulator. This procedure is repeated for each desired sample size, creating an ensemble of *macroscopically* identical devices with *microscopic* variations in impurities distribution.

Figure 3.7 shows the I_D-V_G characteristics from a simulation of 200 microscopically different versions of the testbed device simulated at low drain bias of V_D = 100 mV. It can be seen that the relative magnitude of current variations as a fraction of the continuous device current is large in the sub-threshold region of operation, and is

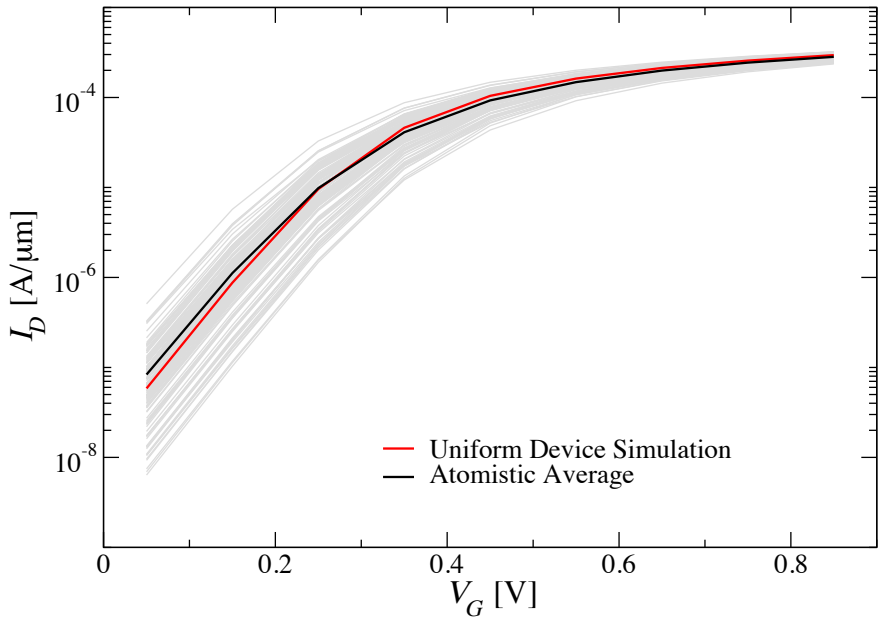

Figure 3.7: The I_D-V_G characteristics of 200 microscopically different version of the testbed transistor simulated at low drain bias of V_D = 100 mV. After [24].

reduced with the increase of gate voltage above threshold. This behaviour can be understood from the potential fluctuations of the random discrete dopants which are barely screened in weak inversion condition. Depending on the random configuration of in its channel, a device will have a larger sub-threshold current if its channel happens to be relatively free of the dopants. Conversely, the transistor will have a weaker sub-threshold current if its flow is uniformly impeded by the dopants crowding the channel region. This effect is reduced above threshold as the increased carrier concentration starts to effectively screen the potential fluctuations of the random discrete dopants. This result demonstrates that measurable differences in *IV* characteristics can arise out of the random variation in impurity distribution, even though from macroscopic view, the devices share an exactly similar doping profile. An important question which this work attempts to address is how do the atomicity and randomness of the impurities affect the electrical characteristics of the device when subjected to charge-trapping-related degradations.

3.4 Summary

The established methods employed for the simulation of modern semiconductor devices have been reviewed. Of the available techniques, the drift-diffusion method with Density Gradient quantum corrections was chosen for this work as it offers the optimal balance between physical accuracy and computational cost.

Following this, the framework of the Glasgow 'atomistic' device simulator used in this study was described. A brief description of the technique used for converting a given continuous doping concentration profile into a representative distribution of discrete impurities was presented, and specific issues in modelling discrete impurities in the simulations were discussed, along with the measures incorporated in the simulator to ensure physically-consistent results.

This chapter concluded with a description of the template device used in this study and how the implementation of discrete impurities in representing its continuous doping concentration profile results in variations of its I_D-V_G characteristics. These results clearly showed that microscopic variations in the device impurity distribution will result in measurable *IV* differences across an ensemble of devices with identical nominal doping. The following chapter examines the effects of randomly positioned and discretely charged impurities on the electrical parametric shift induced by interface-trapped charges.

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Chapter 4

The Effects of Interface-Trapping of Single Discrete Charge

4.1 Introduction

The reliability of contemporary MOSFETs has become a matter of growing concern over recent years [1, 2]. Especially worrying are the increasing electric fields in the active regions of devices, and elevated operating temperatures—conditions resulting from aggressive scaling and device integration. These conditions give rise to Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) degradations [3-5], which are essentially carrier trapping events at the channel-oxide interface and/or further into the gate insulator.

As MOSFETs are scaled into deca-nanometer dimensions, atomic scale variations stemming from the discreteness of charge and matter are also becoming more significant, resulting in measurable variations of key electrical parameters such as drive current and threshold voltage, even between otherwise macroscopically identical devices. Of particular interest to this work is the investigation, by means of realistic numerical simulations, the impact of such atomistic effects on the reliability of the devices within the context of charge trapping-related degradations.

This chapter begins by examining the generic dependencies of the magnitude of charge-trapping-related degradation due to a single charge trapping event. In order to

discern the role of atomicity in the degradation, the simulations initially assume a continuous charge representation of the doping concentration in the device. The devices are then analysed again, now with the continuous doping densities represented by randomly positioned ionised impurity atoms. The magnitude of transistor characteristic changes observed in both types of simulation is then discussed, with key features highlighted.

4.2 Simulation Approach

This study employs the well-established 'atomistic' device simulator developed by the Device Modelling Group at Glasgow, which has a long history of development and refinement spanning more than a decade. It was used for initial studies of the impact of various sources of intrinsic variability—such as random discrete dopants, line edge roughness and oxide thickness fluctuations—on MOSFET operations [6-12]; as well as for exploratory work on the effects of single charge trapping [13-16].

However, the early studies assumed simplified MOSFET structures with idealised doping profiles. Despite this early limitation, the simulator had been successfully validated against experimentally observed RTS amplitudes in relatively large MOSFETs, as shown in Figure 4.1. Both the simulations using continuous doping distribution and random discrete dopants for an idealised MOSFET follow the general feature of the experimental dependence, which saturates in weak inversion and exponentially decreases with the drain current in strong inversion. The maximum possible saturated value of the RTS amplitude obtained for a single electron trapped in the middle of the channel in the continuously doped case is lower than the measured one. However, when random discrete dopants are introduced into the simulations, the results show a larger variation in RTS amplitudes, more closely resembling these experimental measurement and reproducing the wide scatter of RTS amplitudes experimentally observed in identical MOSFETs [17-19]. These results shall be

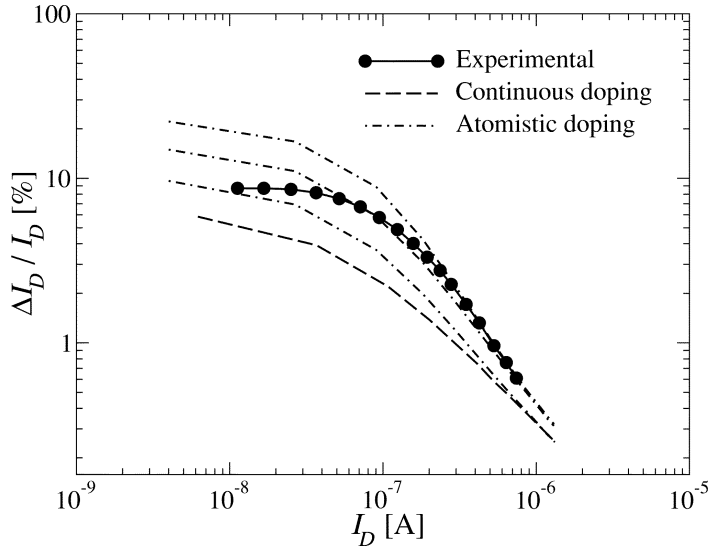

Figure 4.1: Dependence of the RTS amplitude (defined as the drain current change normalised to the empty-trap state current) on the drain current in a relatively large MOSFET with channel width 0.1 μm, channel length 1 μm, oxide thickness 20 nm and channel doping 10^{17} cm^{-3} measured and simulated at V_D = 50 mV. The maximum possible RTS amplitudes from simulations based on continuous doping is lower than the measured amplitudes. Also shown are three curves from three microscopically different transistors with discretely charged and randomly distributed impurities, demonstrating larger RTS amplitudes with a wide variation. After [15].

discussed in detail in Section 4.4.

In contrast to the earlier work reported in [15] which is based on a structurally idealised MOSFET, this work employs an advanced version of the Glasgow 'atomistic' device simulator which has the ability to import realistic doping profiles generated by commercial 3D process simulators into the simulation grid. This feature is highly desirable in order to correctly simulate advanced device designs with increasingly complex doping strategies involving, for example, including HALO channel doping and source/drain extensions to suppress short channel effects. For the

purpose of this research, the simulator was carefully calibrated to reproduce the I_D-V_G characteristics of a real, 35 nm n-channel MOSFET fabricated and reported by Toshiba [20], as explained in detail in Chapter 3. This successful calibration produced a testbed device to allow a proper estimation of the reliability of a real device under the onslaught of charge-trapping related degradations. Additionally, this chapter as an extension to [15] also presents simulations and analysis on the statistical properties of the distribution of current changes caused by a trapped charge at three different gate biases corresponding to leakage, threshold and drive current conditions. Furthermore, while the focus of the study in [15] is the impact of single-charge trapping associated with RTS noise, this work investigates the impact of accumulative trapping of carriers as manifested in Bias Temperature Instability (BTI) degradation. Finally, this work also advances the degree of realism in the simulations with the use of a statistically representative number of trapped charge across the ensemble of simulated MOSFETs, as opposed to a uniformly fixed single trapped charge throughout the ensemble as assumed in [15]. The effects of this methodical difference on the resulting distribution of threshold voltage shifts are discussed in Section 5.3.

4.3 Continuous Doping

In this section, the effects of a single electron trapped at the channel-oxide interface in the 35 × 35 nm n-channel Toshiba MOSFET are investigated. To provide a useful comparison against the effects of dopant atomicity, the simulations presented in this section assume continuous charge representation of the doping profile over the entire device. Only the trapped electron is discretely represented by assigning its charge to the nearest grid nodes. To gain a physical understanding of its effects, we first study the electrostatic impact of the trapped charge on the potential distribution and electron concentration within the transistor. From then, the magnitude of the impact on the drain current is examined at various bias conditions and spatial configurations of the trap.

4.3.1 Effects of a Single Trapped Electron on Potential Distribution and Electron Concentration

The electrostatic potential distribution inside the testbed device with one electron trapped exactly in the middle of the channel is presented at the bottom of Figure 4.2. The simulation is carried out at low drain bias of V_D = 10 mV and at threshold gate voltage estimated by current criterion $I_T = 1 \times 10^{-8}\ W / L$ [A], where W and L are the width and length of the channel respectively. The contour plot at the top of the same

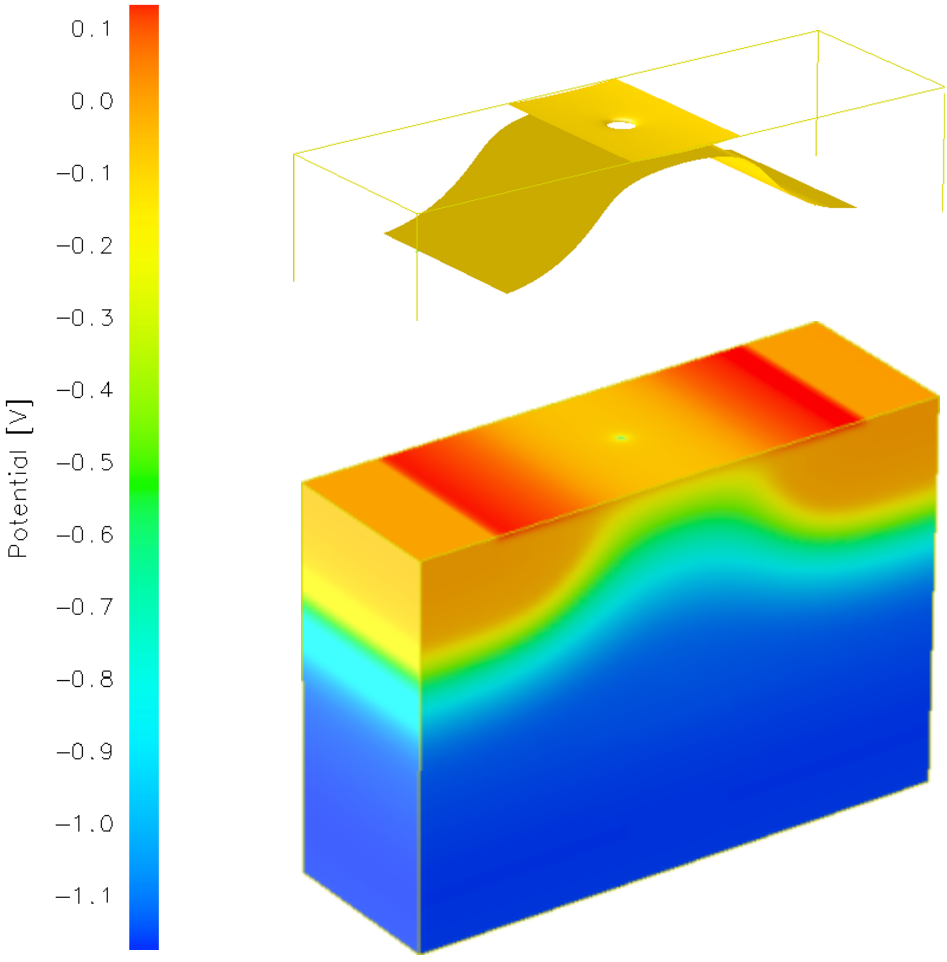

Figure 4.2: Potential distribution inside a 35 × 35 nm n-channel MOSFET with a single electron trapped in the middle of the channel interface. The top plane shows an electron equi-concentration contour.

figure represents an electron equi-concentration layer, in which a cored out circular region surrounding the trapped electron is apparent. This is a natural consequence of the raised electron potential energy at the site of the trapped electron shown as the localised drop in electrostatic potential in the middle of the channel. In effect, the trapped electron repels other electrons in the channel of this n-channel MOSFET, creating a mobile charge exclusion region. This has the effect of reducing the density of carriers which would otherwise participate in the current flow, and consequently lowers the drain current. The size of the cored out region—which is essentially a manifestation of the Coulomb potential of the trapped charge—determines the magnitude of the resulting current reduction. A large charge exclusion region will cause a big reduction in the current because a large fraction of the channel is excluded from the conduction. The effective radius of the region in turn depends on bias conditions and consequent screening from mobile carriers, as shall be demonstrated in the following sections.

4.3.2 Gate Bias Dependence

The I_D-V_G characteristic of the same device at the same bias settings, with and without a single mid-channel trapped electron, is presented in Figure 4.3. It can be seen that the I_D-V_G curve with the trapped charge is shifted into the right side of the I_D-V_G curve without the trapped charge. These effects are graphically magnified in the inset of the same figure: Firstly, the gate voltage which is required to achieve a given reference current is increased with the presence of trapped charge, yielding a threshold voltage shift ΔV_T. Secondly, for any given gate voltage, the drain current is reduced when the MOSFET has a trapped charge.

The magnitude of the drain current reduction for the range of the applied gate biases is presented in Figure 4.4. A charge trapped in the deep sub-threshold regime results in a current reduction of as high as 18% for this particular device. At low gate voltages, the inversion charge density is low and cannot efficiently screen the Coulomb potential of

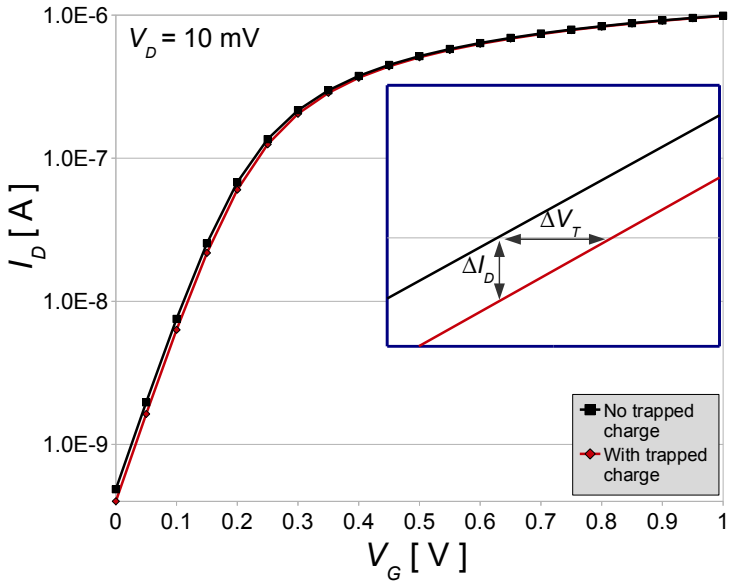

Figure 4.3: I_D-V_G curve of a 35 × 35 nm n-channel MOSFET simulated with and without a single mid-channel trapped electron. Inset figure shows the definition of threshold voltage shift ΔV_T and drain current change ΔI_D caused by the trapped charge.

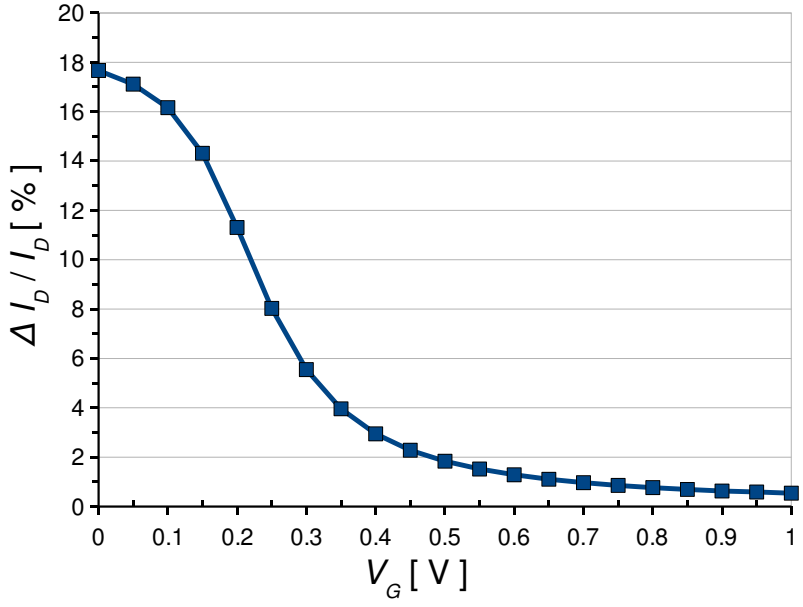

Figure 4.4: Gate bias dependence of the relative drain current change caused by a electron trapped in the middle of the channel.

the trapped charge. This results in a large charge exclusion region and consequent large reduction in current. As the gate voltage increases and the potential barrier in the channel lowers, the magnitude of current change reduces as a result of the increased population of mobile charge in the channel, screening the Coulomb potential of the trapped charge and shrinking the charge exclusion region.

4.3.3 Positional Dependence

It is clear from Figure 4.2 that at low drain voltage an electron trapped in the middle of the channel, where the peak of the potential barrier is, will exert the greatest impact of the drain current. This is illustrated in Figure 4.5 showing the positional dependence of the current reduction caused by a single trapped electron placed at equally spaced width-centre positions running from the source to the drain junction, and evaluated at threshold current condition for all drain bias. At low drain voltage of 10 mV, the positional dependence is bell-shaped with minimal effect in regions close to the metallurgical *p-n* junctions of the source and drain. The relatively higher doping and mobile carrier concentrations in the source and drain regions regions effectively screen the Coulomb potential of the the trapped charge leading to a reduced radius of the charge exclusion region.

However, the inversion layer electron concentration decreases towards the middle of the channel. Thus an electron trapped close to the middle of the channel remains barely screened, leading to a wider area of the charge exclusion region and resulting in a more significant current reduction. The inset figure shows the drain current reduction caused by a single trapped electron placed at every positions over the entire channel-interface plane evaluated at V_D = 10 mV, from which it can be seen that the magnitude of current change is nearly uniform throughout the entire width of the device. The non-uniformity near the edge is introduced by the Neumann boundary condition used in the simulation.

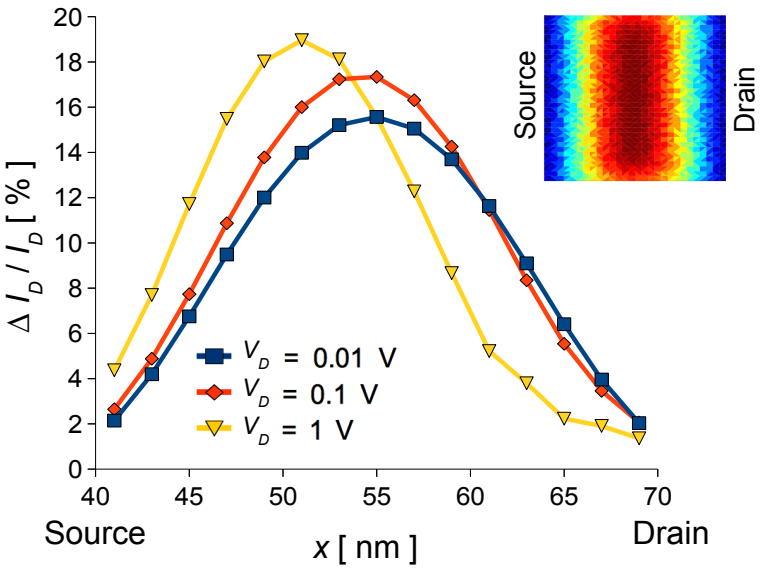

Figure 4.5: The relative current reduction caused by a single trapped electron moved across the width-centre positions along the channel-oxide interface from source to drain at various drain voltages. The inset figure shows relative current change by a single electron trapped at the positions over the entire channel-interface plane at V_D = 10 mV.

At high drain voltage, the peak of potential barrier of the channel shifts from the centre of the channel towards the source end, causing a similar shift in the positional dependence of current change. The shift in peak potential is shown in Figure 4.6. An increase of V_D from 10 mV to 100 mV at constant drain current results in a minor increase in the potential barrier as the gate partially loses some control of the current to the increased electrical field at the drain. An electron trapped at this heightened potential barrier causes a somewhat more significant current reduction compared to the V_D = 10 mV case. Another order of magnitude increase in V_D to 1.0 V will pinch the channel off at the drain end, markedly shortening the channel conduction length, as well as causing a further shift of the barrier peak towards the source end. The resulting effects are two-fold:- i) The shortened channel length and the narrower

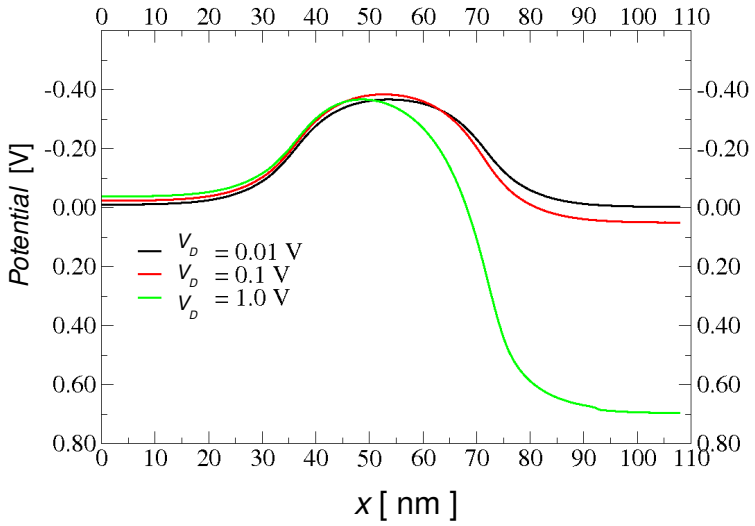

Figure 4.6: Potential profile along the channel interface plane from source to drain at various drain bias voltages.

potential barrier enhances the impact of the charge exclusion region, resulting in a bigger current reduction. ii) The trap position for the maximum current reduction shifts towards the source. This offers an explanation for the drain voltage dependence of the experimentally measured RTS amplitudes [21, 22], and has been used to deduce the positions of trapped charges as reported in [23].

4.3.4 Drain Bias Dependence

The drain bias dependence of the fractional drain current reduction caused by a single charge trapped in the mid-channel position is summarised in Figure 4.7. The trend is in agreement with experimental observations [19] showing a plateau in weak inversion and a roll-off inversely proportional to I_D in strong inversion. Such a roll-off is well-explained by the elementary carrier number fluctuation estimate [24], yielding $1/(W_{eff}\ L_{eff}\ N_s)$ amplitudes of relative drain current change when the correlated fluctuation of mobility is neglected (N_s is the inversion layer carrier density per unit area). At any given drain current level in strong inversion, the fractional current

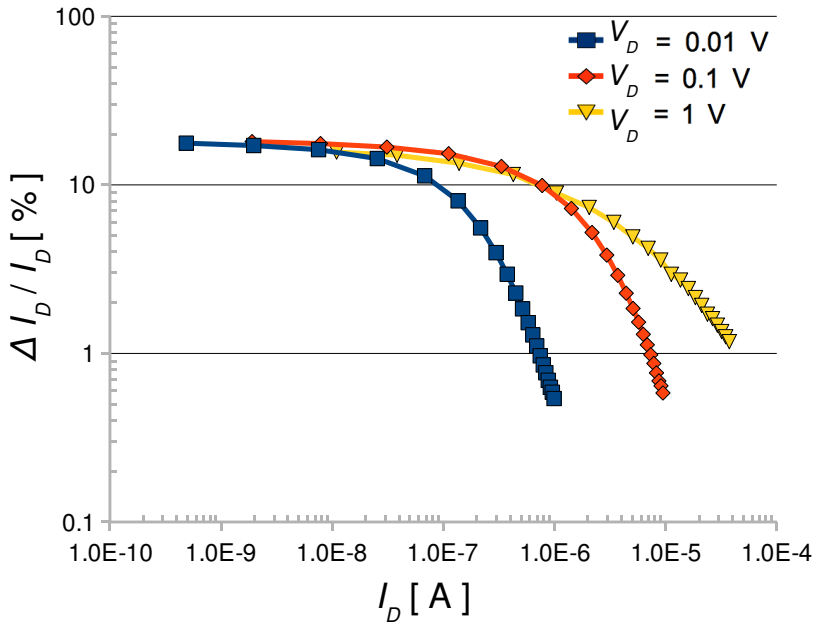

Figure 4.7: The dependence of relative drain current reduction on the drain current caused by a single trapped charge in the middle of the channel at various drain voltages.

reduction is bigger at higher drain voltage due to the lower applied gate bias and the consequent higher potential barrier in the channel. This results in the horizontal shift of the drain bias dependence curve with the increase in drain voltage. At the highest applied drain voltage of 1.0 V, the drain current increases more dramatically with every step increase in the applied gate bias. Consequently, the slope of the roll-off in $\Delta I_D/I_D$ magnitudes in strong inversion is reduced.

4.4 Atomistic Doping

During device fabrication, the number and individual position of the dopant atoms implanted into the bulk silicon lattice cannot be precisely controlled, resulting in

random numbers and positions of dopants in nominally identical devices. The distribution of the individual dopant atoms within the active regions affects the electrostatics and the transport within a transistor, leading to variation of the device characteristics and performance. The Glasgow 'atomistic' device simulator is able to realistically construct this atomic-scale variation by statistically assigning discrete dopant atoms on the silicon lattice based on the continuous doping distribution in the nominal device, thereby creating an ensemble of macroscopically identical transistors with microscopic differences in the doping configurations.

Figure 4.8 illustrates the electrostatic potential distribution inside the same 35 nm n-channel transistor simulated in the previous section, now with random discrete dopants introduced in the active regions only while the contact regions and substrate significantly below the depletion region remain represented by continuously doped. The electron concentration at the channel-interface plane is projected on the middle plot while the top plot shows an electron equi-concentration contour connecting the source and drain. It can be seen that in regions with the discrete dopants, there exist random and localised potential fluctuations as opposed to the smoothly distributed potential in the continuously doped regions. The potential fluctuations from the discrete dopants also alter the local electron concentration and the corresponding current densities in the channel. The electron current percolates through the channel by moving in the valleys between the potential energy spikes introduced by the negatively charged ionized acceptors. This results in a channel with a non-homogeneous electron concentration shown in the middle plot, where the paths between the dopants have relatively higher density of carriers than the area immediately surrounding the dopants.

The formation of such random conducting paths in a landscape of potential peaks and valleys, shown in the top plot by an electron iso-concentration contour connecting the source and drain, gives rise to variations in electrical characteristics. An easily formed

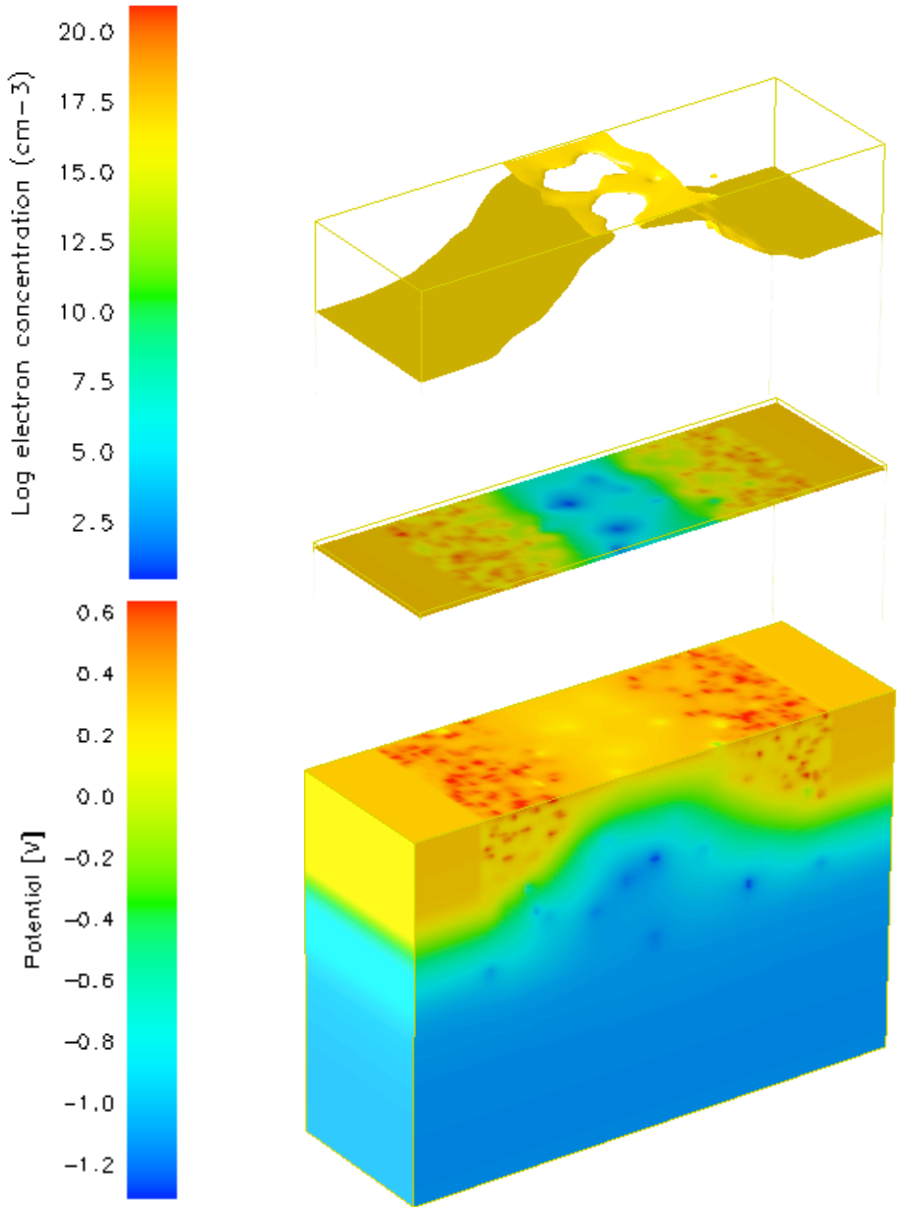

Figure 4.8: The effects of atomicity coming from the discrete impurities can clearly be seen as the random and localised variations of potential (*bottom bulk*) and electron concentration (*middle and top plots*).

percolation path will enable the device to partially turn on earlier than an idealised, continuously doped transistor, as the gate voltage is slowly raised. Conversely, a channel which happens to be uniformly blocked by a string of strategically placed

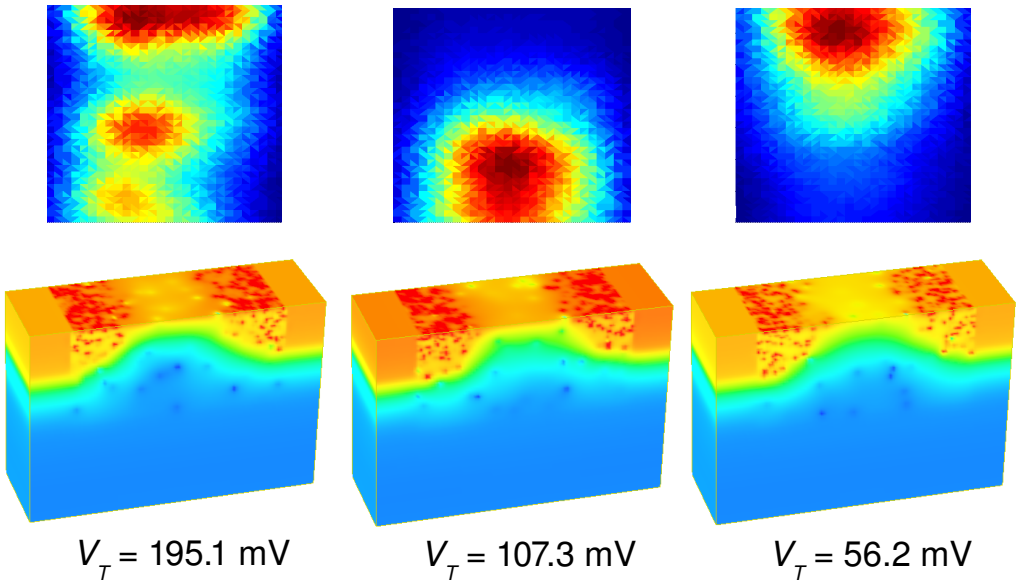

Figure 4.9: Potential distribution in three microscopically different transistors with random discrete doping is shown in the bulk. The positional dependence of relative current reduction mapped as a function of the trap's location over the entire channel area is projected on the top plane of each transistor.

dopants will impede the formation of a conducting path, resulting in a higher overall threshold voltage than expected from continuously doped transistor theory. The resulting potential fluctuations from the discrete dopants also alter the boundaries of the depletion region due to various local dopant positions; all of these effects result in a more complicated device characteristics compared to those obtained from conventional simulation with continuous doping distribution.

Figure 4.9 shows the positional dependence of current change caused a single trapped charge mapped over the entire channel area of three microscopically different transistors with three randomly different discrete doping configurations. The figures depict the transistors with threshold voltages decreasing from left to right. A distinctly different feature in discrete doping simulations is that the maximum impact of the

trapped charge might not be uniformly distributed in the centre of the channel, in contrast to what is observed in a continuously doped transistor biased at low drain voltage (refer inset of Figure 4.5). In addition, as a result of the marked differences in discrete dopants configurations, each device has a unique, fingerprint-like characteristic of the sensitivity map of the impact of a single trapped charge. This implies that even if a charge happens to be trapped in the same exact locations in all three transistors, they might still not result identical magnitudes of degradation. All of these distinct and significant features introduce a statistical aspect into the reliability of the devices which merits a move beyond a single-device description into a statistical domain by describing the responses of a large statistical ensembles of devices.

4.4.1 Statistical Simulation of the Effects of Single Trapped Charge

To investigate the effect of a single trapped charge in a statistical ensemble of transistors, 1000 microscopically different random dopant implementations of the 35 nm MOSFETs are simulated using the Glasgow 'atomistic' device simulator described in detail in Chapter 3. The drift-diffusion approximation implemented in the simulator does not capture non-equilibrium and ballistic transport. Neither does it capture transport variations due to ionised impurity scattering from randomly positioned dopants in microscopically different transistors. As a result, the simulations are unable to accurately predict quantitatively the current reduction due to the additional scattering which plays an important role at high current levels [25]. However, even without capturing local mobility modulation around trapped charge, the simulator *is* very well-suited to handle the electrostatics of the trapped charge, and accurately captures details in threshold and sub-threshold where the electrostatic effects dominate the transistor behaviour.

Due to the microscopic differences in the number and random spatial configurations of the dopants in the ensemble of devices, each MOSFET requires a different gate

voltage to produce the same drain current. To ensure the MOSFETs are biased at the same region of operation, the simulator initially adjusts the gate voltages at which three reference current levels occur in each of the devices. These currents correspond to the leakage (I_D at V_G = 0 V), threshold ($I_D = 1 \times 10^{-8}$ A) and drive current (I_D at V_G = 1.0 V) conditions of a continuously doped transistor. A single discrete charge representing a trapped electron is then assigned to a randomly-determined location in the channel-interface area of each transistor in the ensemble. Following this, the simulator again solves for the currents at the three pre-determined gate voltages for each transistor. The resulting relative drain current change ($\Delta I_D/I_D$) and threshold voltage shift (ΔV_T) induced by the trapped charge are then recorded.

4.4.2 Distribution of Drain Current Change

The distribution of relative drain current reduction at gate biases corresponding to leakage, threshold and drive currents, all at drain bias of 10 mV, are plotted in Figure 4.10. The maximum magnitude of current reduction occurs in the deep sub-threshold regime. This current reduction gradually decreases in magnitude as the transistors are driven into saturation regime at higher gate biasing.

It can be seen that increasing gate bias changes both the shape and width of the $\Delta I_D/I_D$ distribution. At leakage and threshold current conditions, the distribution has a high probability density at low $\Delta I_D/I_D$ values and a low probability density at high $\Delta I_D/I_D$ values. It can also be seen that at these gate biases, the magnitudes of $\Delta I_D/I_D$ values have relatively wider distributions than at drive current condition. This can be explained by the fact that at weak inversion regime, the channel has very few carriers, therefore the electrostatic potentials of the channel dopants remain barely screened. Consequently, the distribution of carriers in the channel is exceedingly non-homogeneous as the carriers percolate through the hills and valleys of the unscreened electrostatic potential of the channel dopants. In local areas of the channel where there happens to be a crowding of dopants, the local carrier concentration there will be

relatively lower, therefore a trapped charge in these specific areas will result in minimal change on the overall current. Conversely, in local areas which are relatively free of channel dopants, the local carrier concentration is relatively higher, thus a trapped charge in these specific areas will result in a profound reduction in the overall current. It is this inhomogeneity in the carrier distribution which results in the wide distribution of the $\Delta I_D/I_D$ values at weak inversion. At higher gate biasing corresponding to drive current condition, the carrier distribution in the channel becomes somewhat more homogeneous as the Coulomb potential of the channel

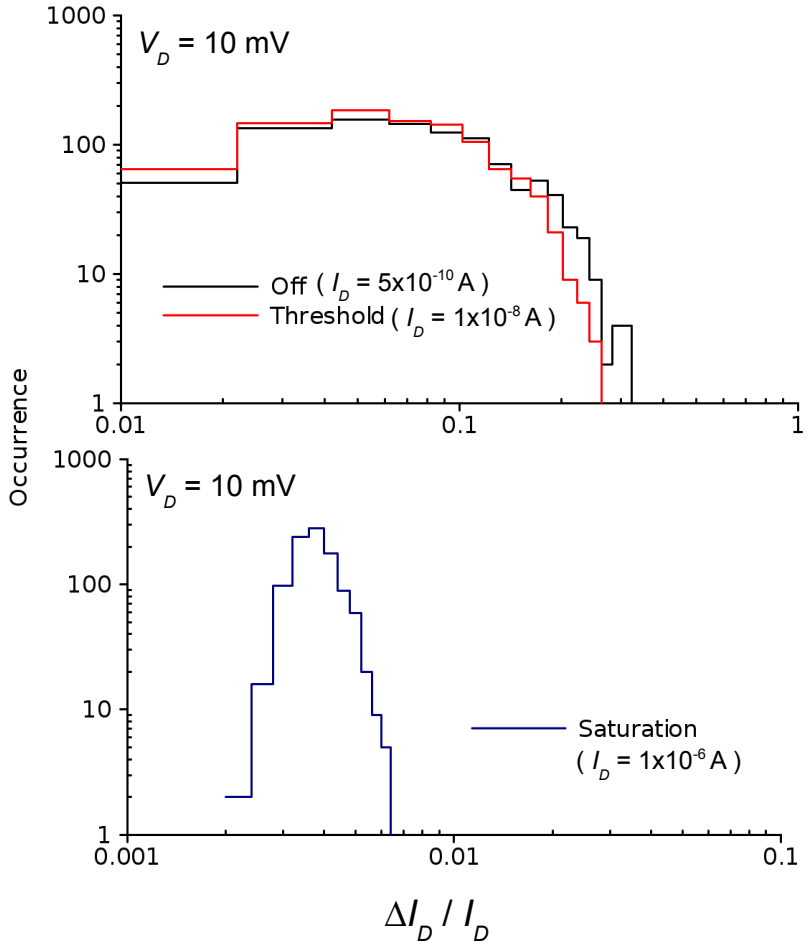

Figure 4.10: Distribution of drain current reduction caused by a single trapped charge in 1000 35 × 35 nm MOSFETs simulated at three gate biases corresponding to leakage, threshold and drive.

dopants are strongly screened by the higher number of available carriers. Charge trapping in regions of the channel will then cause minimal and closely identical magnitudes of current reduction. Consequently, the shape of the $\Delta I_D/I_D$ distribution evolves to become more symmetric and narrower in the saturation regime.

To analyse the statistical properties of the drain current reduction at differing gate bias conditions, we make use of the Weibull distribution which is given by the cumulative distribution function (CDF):

$$F((\frac{\Delta I_D}{I_D}); k, \lambda) = 1 - e^{-(\frac{\Delta I_D}{I_D})/\lambda)k} \tag{4.1}$$

where k and λ are the shape and scale parameters respectively. $k = 1$ indicates that distribution is exponentially distributed while $k \approx 2$ characterises a right-skewed distribution. The scale parameter λ reflects the dispersion of the data; the greater its magnitude the wider the distribution. Parameters k and λ can be estimated by regression on the linearised form of the CDF. Rearranging and taking the natural logarithm on both sides of the CDF yields:

$$\ln(1 - F(\frac{\Delta I_D}{I_D})) = -((\frac{\Delta I_D}{I_D})/\lambda)k \tag{4.2}$$

Reversing the sign and taking natural logarithm on both sides of Equation 4.2 forms:

$$\ln(-\ln(1 - F(\frac{\Delta I_D}{I_D}))) = k\ln(\frac{\Delta I_D}{I_D}) - k\ln(\lambda) \tag{4.3}$$

Equation 4.3 has the general form of a linear equation $y = mx + c$, where;

$$y = \ln(-\ln(1 - F(\frac{\Delta I_D}{I_D}))) \tag{4.4}$$

$$m = k \tag{4.5}$$

$$c = -k\ln(\lambda) \tag{4.6}$$

Data in Figure 4.10 is now replotted in Figure 4.11 based on Equation 4.3, with superimposed logarithmic regression lines giving estimates of parameters k and λ. In leakage and threshold, the slope of the $\Delta I_D/I_D$ distribution, which is also the value of parameter k, is approximately 2, indicating that the distribution is right-skewed which is in agreement with the histogram in Figure 4.10. The magnitudes of $\Delta I_D/I_D$ values in both of these current conditions are relatively large and widely distributed, which can be observed from both the range of $\Delta I_D/I_D$ values generated by the simulation and the calculated values of λ. This is intuitively expected as the channel is markedly non-homogeneous in terms of electron concentrations due to the barely screened potentials

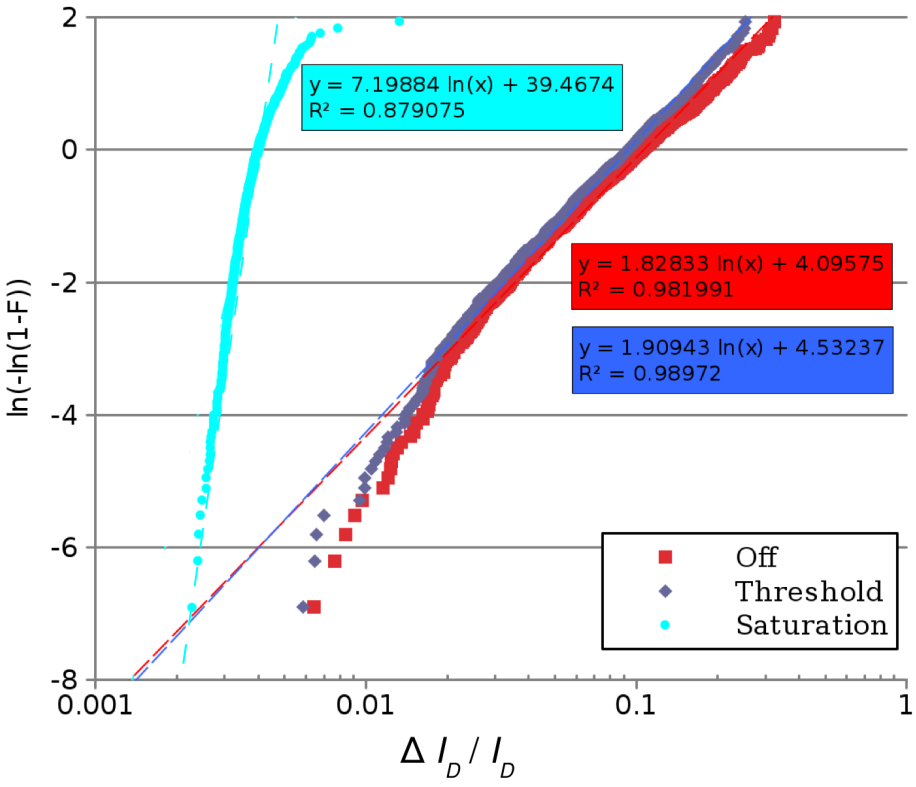

Figure 4.11: Weibull probability plot of normalized drain current change caused by a single trapped charge in 1000 35 × 35 nm MOSFETs simulated at three gate biases corresponding to leakage, threshold and drive current conditions.

Gate bias	*k*	λ
Off	1.828	0.106
Threshold	1.909	0.093
Saturation	7.199	0.004

Table 4.1: Values of parameters *k* and λ are altered with the increase of gate bias, reflecting a change in the shape and dispersion of the $\Delta I_D/I_D$ distribution.

of the dopants and trapped charge at weak inversion. Consequently, a trapped charge in weak inversion exerts a more profound effect which results in large magnitudes of current reduction, while the channel non-homogeneity gives rise to a wide variation of magnitudes of current change. Such an effect is analogous to the impact of discrete dopants causing bigger variations in the sub-threshold regime than on the on-current.

Each distribution also has a slight bending, where the lowest range of $\Delta I_D/I_D$ values (from 0.006 to 0.02) collectively has steeper slope compared to rest of $\Delta I_D/I_D$ values. This is the result of each device in the ensemble being mandatorily assigned with one trapped charge. Consequently the simulated ensemble *must* result in a certain minimum value of $\Delta I_D/I_D$. In reality, the number of trapped charge in an ensemble of devices varies statistically, where some device may not have any trapped charge at all, thus the lowest range of $\Delta I_D/I_D$ values will go even lower and its slope becomes less steep. This is shown in Chapter 5 (Figure 5.8), where we statistically vary the number of trapped charge in the ensemble of devices, and the resulting distribution of threshold voltage change more closely resembles the experimental measurements.

The transition from leakage to threshold causes only a slight increase in the slope of

the $\Delta I_D/I_D$ distribution and a slight decrease of its width. However, as the transistors are driven into saturation the value of parameter k is markedly increased indicating the distribution shape is pronouncedly altered, and the greatly reduced parameter λ reflects a tighter distribution. At higher gate biases, the channel becomes more uniform as the potentials of the dopants and trapped charge are screened by the increased inversion charge. Charge trapping in any region of the channel will then cause smaller magnitudes of current change with relatively narrower distributions, because the underlying carrier density is higher as well as more uniformly distributed throughout the channel. This results in a reduction as well as convergence of the magnitudes of $\Delta I_D/I_D$, and changes the shape of the distribution to be relatively more symmetric centred around the average magnitude of current reduction.

However, as previously mentioned the fact that the mobility modulation by the trapped charge is not accounted for in these simulations implies that the magnitudes of current change at high gate bias are underestimated. It has been demonstrated, for example, by Monte Carlo particle simulations that "*ab initio*" inclusion of carrier scattering by the Coulomb potential of trapped charge at high gate bias results in much larger current reduction compared to drift-diffusion approximation due to the increasingly significant role of Coulomb scattering by the trapped charge at high current levels [25]. This finding is based on a study for a 30 nm channel length nMOSFET with a single mid-channel trapped electron simulated in [25]. The comparative study reports a 7% and 10% decrease in drain current by drift-diffusion and Monte Carlo simulations respectively, both at gate bias of 0.4 V and low drain voltage of 50 mV. At higher gate voltage of 1.0 V, the drift-diffusion simulation only gives 1% current reduction while the Monte Carlo simulation gives 3% current reduction. Because the electrostatic potential and electron distributions in the "frozen field" Monte Carlo simulations performed in the study are obtained directly from the preceding drift-diffusion simulations, it can be argued that the additional decrease of current by given the Monte Carlo simulations are attributed by carrier scattering by

the Coulomb potential of the trapped charge, which is not accounted for in the corresponding drift-diffusion simulations. More revealingly, as the same study concludes, the growing discrepancy between the drift-diffusion and Monte Carlo simulations from 30% at near threshold to several times at strong inversion condition indicates that the electrostatic influence of the trapped charge is primarily responsible for the reduction in current at low gate bias, while additional scattering is the relatively dominant mechanism at high gate bias.

The distribution of current change generated by simulations which include the effect of random discrete dopants is distinctly different from that produced by simulations assuming continuous doping. In order to the highlight these differences, the simulation strategy above is repeated using 1000 transistors with continuous doping, each of which is assigned with a single trapped charge at a randomly-determined location on the channel-interface plane. The resulting distribution of current changes from both types of simulations at threshold current condition is shown in Figure 4.12. The continuous doping simulations result in a double-headed distribution with high densities at both the smallest and the highest $\Delta I_D/I_D$ values, with a sharp cut off at $\Delta I_D/I_D \approx 15\%$. Such a distribution is expected from the bell-shaped positional dependence of the current change amplitudes illustrated in Figure 4.5 where traps near the source and drain junctions are responsible for the peak in the distribution at low $\Delta I_D/I_D$ values, while traps along the middle of the channel result in the peak in the distribution at $\Delta I_D/I_D \approx 15\%$. In the discrete doping simulation, the distribution has high occurrence at the small amplitudes just like in the continuous doping simulations. But unlike in the case of continuous doping setting, there is an exponential decrease towards a *much higher* $\Delta I_D/I_D$ amplitudes recorded from the discrete dopants simulations, with the largest current change recorded from the sample being nearly 30% — twice the maximum amplitude from the continuous doping simulation. The introduction of discrete dopants into the simulations therefore extends the tail of the distribution resulting in closer qualitative resemblance to the distribution of RTS

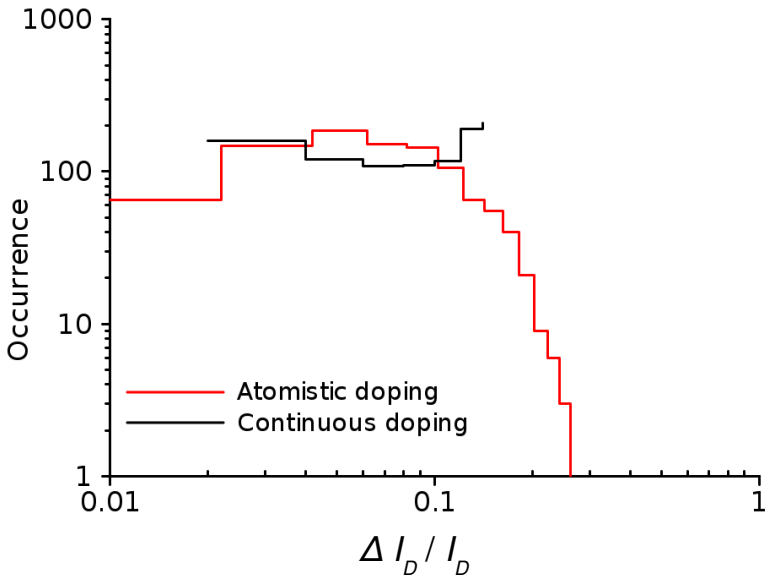

Figure 4.12: Distribution of drain current change at threshold gate biases from continuous and 'atomistic' doping simulations in 1000 35 × 35 nm MOSFETs. Simulations with 'atomistic' doping result in larger magnitudes of current reduction which extend the tail of the distribution.

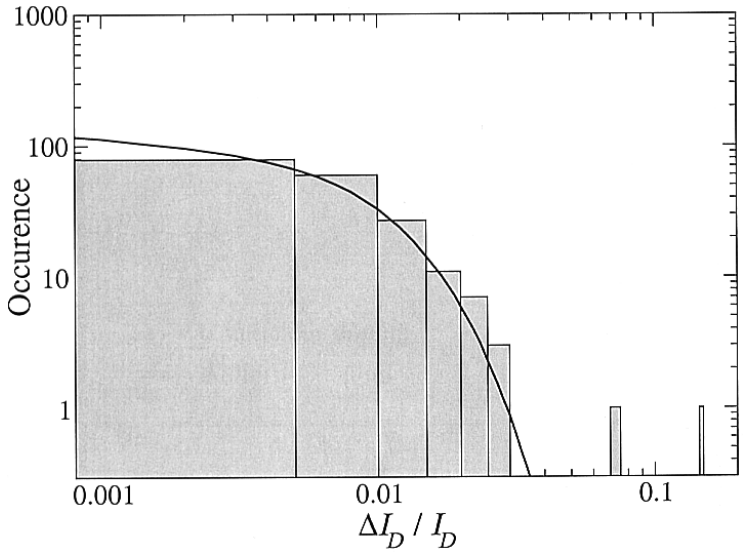

Figure 4.13: Experimentally observed distribution of RTS amplitudes in 187 500 × 500 nm MOSFETs. After [15].

amplitudes from experimental observations shown in Figure 4.13. This confirms that the statistical interplay between the discrete dopants and the trapped charge is responsible for the experimentally observed tails in the distribution.

4.4.3 Origin of Anomalously Large Magnitudes of Current Reduction

To investigate the origin of the anomalously large current reduction generated by the 'atomistic' simulations, a transistor is selected from each ends of the current change distribution and an inspection is made into the pre- and post-trapping potential distribution and electron concentration within each transistor. Figure 4.14 displays a transistor with one of the largest current changes (28.5%) recorded in the ensemble. The reference potential distribution without the trapped charge is shown in the left

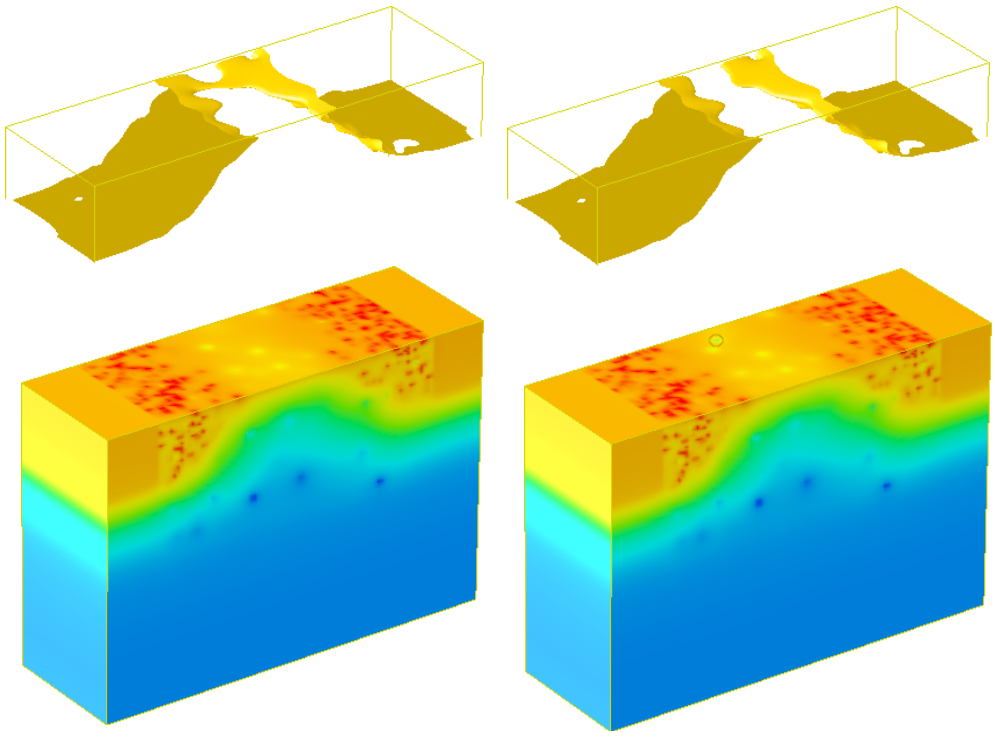

Figure 4.14: Potential distribution in a MOSFET with a large current change; (*left*) with no trap, and (*right*) with a trapped electron (location is marked by circle) cutting off a critical current path. Top planes show electron iso-concentration surface.

side of the same figure. A careful observation shows that in this particular MOSFET, the dopants are concentrated in the lower-half of the channel, leaving the upper-half as a dominant path for the current to flow at any given gate voltage.

The resulting effect on the electron concentration is shown in top plot representing the maximum electron iso-concentration surface connecting the source and drain. The effects of discrete dopants located near the interface can be seen by formation of a narrow current path of high carrier density sandwiched between larger areas of lower density due to the raised local potential energy by the dopants. By chance, a single charge happens to be trapped in that critical current percolation path which completely cuts off the electron equi-concentration layer connecting the source and drain, resulting in a huge drop of current. This exceptionally large effect is not replicable in a

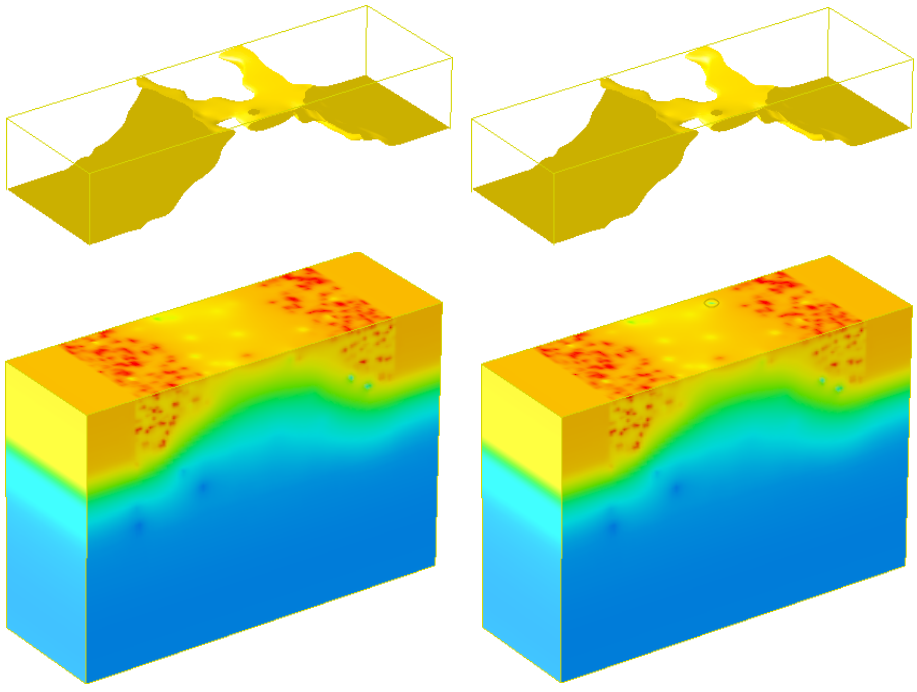

Figure 4.15: Potential distribution in a MOSFET with a small current change; (*left*) with no trap, and (*right*) with a trapped electron (location is marked by circle) leaving the current path unaffected. Top planes show electron iso-concentration surface.

continuous doping simulation because charge trapping in a homogeneous channel will simply cause the current to flow around it, whereas such compensation is not possible in a channel having discrete dopants already blocking the regions outside the boundaries of the percolation path.

Figure 4.15 shows the potential and electron concentration from a transistors sampled from the low amplitude end of the current change distribution. This device, which is biased similarly to the device in Figure 4.14, is only mildly affected by the trapped charge (a current reduction of only 0.61%) because the activated trap is located in an area already crowded with dopants at the upper half of the channel with relatively low local current density. This leaves the dominant current path located in the lower half of the channel barely affected.

4.4.4 Distribution of Threshold Voltage Shift

Besides measuring the change in current at a fixed bias, another way of assessing the magnitude of degradation due to charge trapping is by the resulting shift in threshold voltage, ΔV_T. We define ΔV_T as the difference in the gate bias to give the threshold current before and after a charge trapping event. The threshold voltage V_T is an important parameter in MOSFET design because adjusting V_T for devices in a circuit adjusts the balance between higher drive current and better leakage performance. An electron trapping event in an n-channel MOSFET induces a local modulation of the surface potential and carrier density, which consequently shifts the I_D-V_G curve, increasing V_T. Such a shift, if large enough, may reduce the drive current available from a device past design tolerances and result in binary errors in digital logic circuits. Even relatively small increases in V_T, and thus relatively small reductions in drive current, will have an effect on circuit timing, and can result in timing errors in digital logic circuits.

The distribution of ΔV_T obtained from simulations of the 1000 MOSFETs, each with a

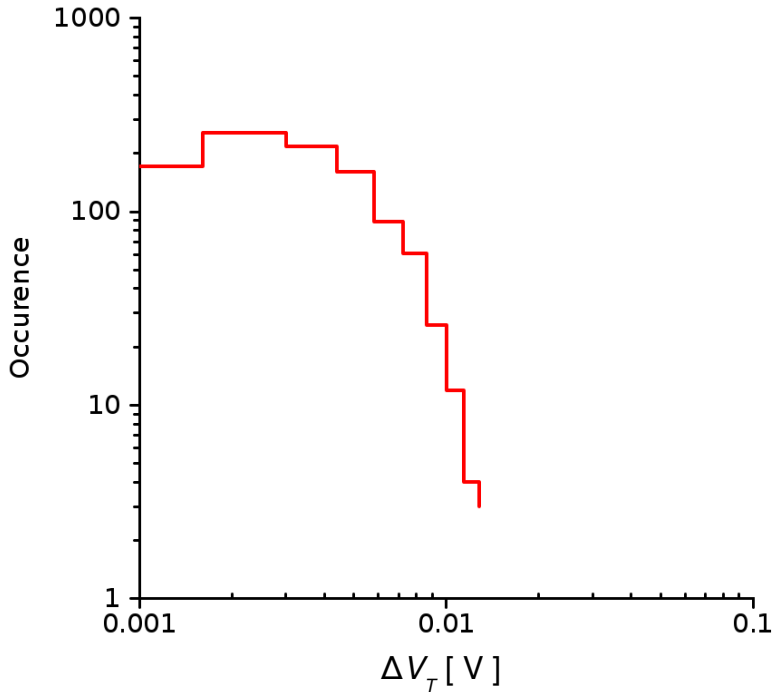

Figure 4.16: Distribution of threshold voltage shift in an ensemble of 1000 atomistically doped 35 × 35 nm MOSFETs, each with a single interface-trapped charge.

single randomly positioned trapped charge, is plotted in Figure 4.16. The average threshold voltage shift recorded from the sample is 3.90 mV while the maximum shift, with a probability of 0.2%, is approximately 14 mV. Larger amplitudes can be expected at lower probability levels if the size of the simulation sample is further increased. For comparison, the ΔV_{T} for the simulated device calculated using the standard formula based on continuous charge:

$$\Delta V_T = \frac{Q_T}{C_{OX}} \tag{4.7}$$

is 4.06 mV, where Q_T is the total charge of the trapped electron per unit area and C_{OX} is the oxide capacitance per unit area. While the theoretical approximation gives a

close value to the average shift computed from these simulations, the model proves insufficient in explaining the extreme values of the shift, dubbed as "anomalously" large as reported in experimental observations [19, 26, 27]. Such discrepancy arises from the fact that the simple one dimensional theoretical approximation does not capture the spatial configuration of the trapped charge in inhomogeneous channels caused by the potential fluctuations coming from the discrete dopants.

An interesting question then arises—to what degree is the initial V_T correlated to the threshold voltage change, ΔV_T ? Such information would be useful for circuit designers in projecting the reliability of their designs based on the initial parameters extracted from the fresh components. To investigate the relationship, a scatter plot of the two variables is plotted in Figure 4.17 where the initial threshold voltage for each device is plotted on horizontal axis while its threshold voltage shift is plotted against the vertical axis. It can be observed that the points are fairly well-scattered indicating

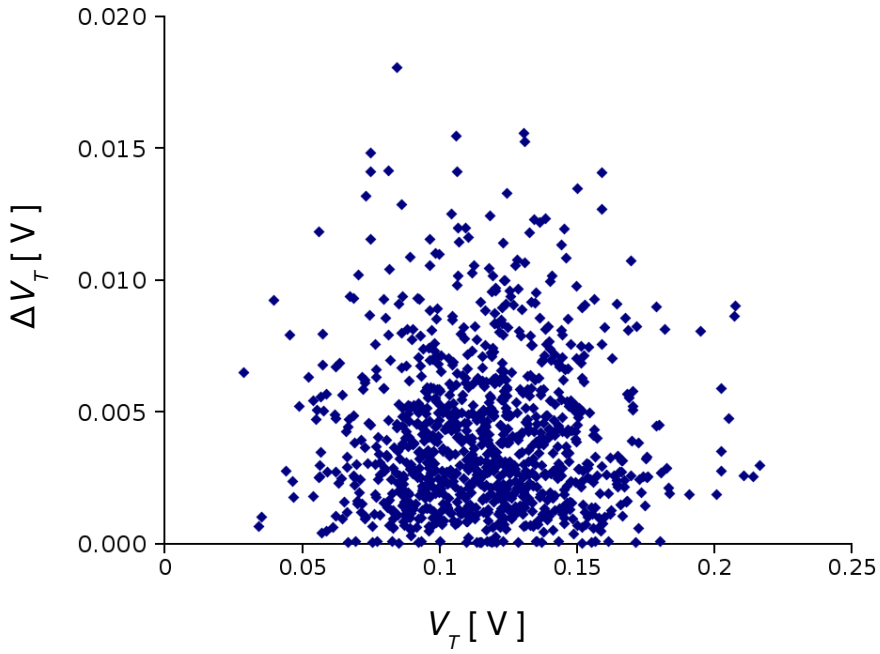

Figure 4.17: Scatter plot showing the correlation between an initial threshold voltage V_T and the resulting threshold voltage shift ΔV_T in 1000, 35 × 35 nm MOSFETs subjected to a single trapped charge.

a lack of correlation. If a correlation existed, a distinct and elongated pattern would be observable. A calculation of the correlation coefficient between of the two variables yields a small value of 1.1×10^{-3} , which is in agreement with the visual indication. However, the small *positive* correlation indicates that devices with large initial V_T values are somewhat more likely to generate large ΔV_T values. This is intuitively reasonable considering the fact that in a MOSFET with a high V_T , the channel is uniformly blocked by dopants [6, 28] which results in the formation of percolation paths of high current density; whereas in a low V_T transistor its channel is relatively free of dopants thus such paths are likely to be absent. The presence of such paths make the devices statistically more likely to give huge responses to trapped charge.

4.4.5 Gate Voltage Dependence of ΔV_G

Figure 4.18 and illustrates the measured normalised step height (measured gate voltage shift, normalised to the shift expected from charge sheet approximation of Equation 4.7) for four different traps in linear and saturation mode, for a p-channel MOSFET of an undisclosed design [29]. For trap #4 in saturation mode, the step height decreases linearly with the applied gate voltage, as can be understood from the gate bias dependence explained in Section 4.3.2, where the increased carrier density resulting from increased gate bias screens the trap's potential thus reducing the step height. Since the trap also records the biggest response in weak inversion for the whole set of measurements, it can even be assumed that this trap may lie in a critical current percolation path, such as the one as illustrated in Figure 4.14. However, the responses of other traps are contradictory. For example, traps #1 and #3 give increasing step height with increased gate bias, while trap #2 gives a more complicated response; an initial steady increase of step height with gate bias until $V_G \approx -0.6$ V and then a sudden drop for higher gate biases. The initial hypothesis was that the different location of the traps with respect to the percolation path might have a role in the resulting non-identical trend in their responses. A trap which is initially outside the percolation path at weak inversion may find itself within the path at higher gate

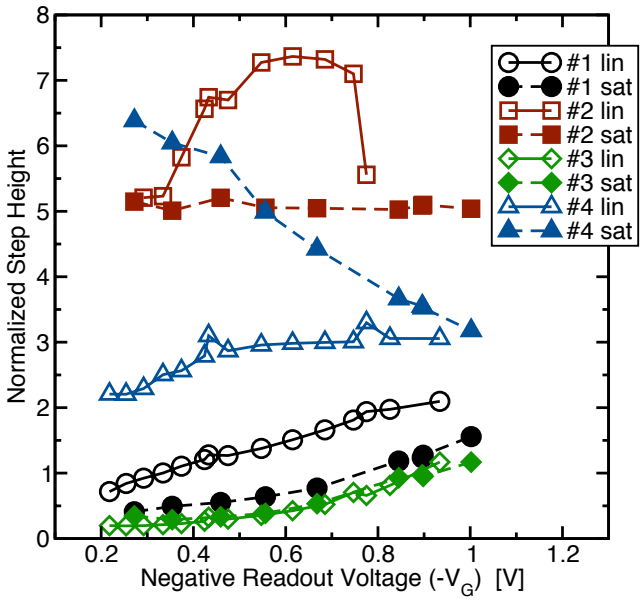

Figure 4.18: Experimentally recorded step heights (measured gate voltage shift normalised to the shift expected from charge sheet approximation) by single defects in a pMOSFET across varying readout voltages [29].

bias, and hence starts to register responses. In order to gain a clearer understanding of these phenomena, a 3D physical 'atomistic' simulation was carried out.

The testbed device for the study with a suitable random doping configuration is chosen by simulating a sample of 200 microscopically unique transistors at low drain bias of 10 mV with a single trapped charge in each, from which a member of the ensemble with an anomalously large response is selected. In order to study the gate voltage dependence of the threshold voltage change associated with charge trapping at different strategic positions, the sensitivity of the selected device to trap position is first mapped by measuring the current drop caused by a single trapped charge placed at positions across the entire channel-interface plane, as illustrated by the inset in Figure 4.20. From this map, the location of the current percolation path can be ascertained.

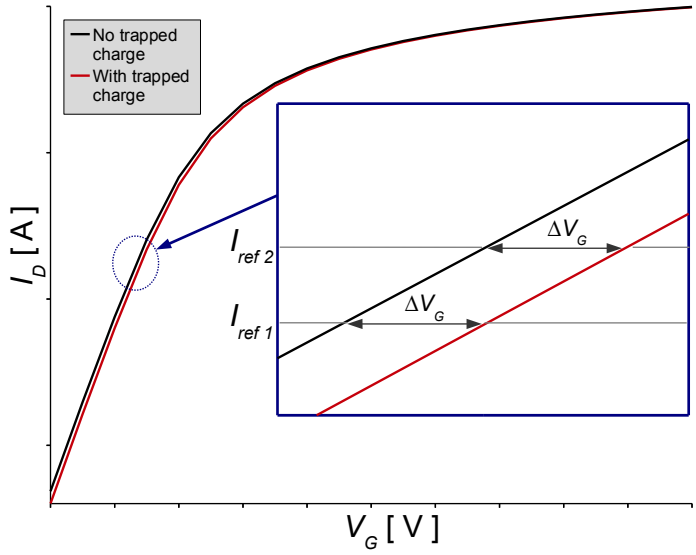

Figure 4.19: The definition of the ΔV_G parameter which is the change in gate voltage to give common reference current levels, before and after the charge trapping event.

Then, a single trapped charge is moved across the width of the device on a path normal to the percolation path, intersecting it at the most sensitive position, while registering the resulting step height (ΔV_G) across a range of applied V_G. The ΔV_G is defined as the change in gate voltage to give a common reference current level, before and after the charge trapping event, that is, $\Delta V_{G(Iref)} = V_{G(Iref,\ \text{with trapped charge})} - V_{G(Iref,\ \text{without trapped charge})}$, where I_{ref} is the particular reference current point at which we wish to calculate the corresponding ΔV_G. This definition for parameter ΔV_G is schematically illustrated in Figure 4.19. To allow fair comparison between different devices, ΔV_G is normalised to ΔV_T expected from standard charge sheet approximation of Equation 4.7.

Figure 4.20 summarises the normalised ΔV_G as a function of the trap's position across the width of the device, clearly showing its bias and positional dependence. When the trapped charge is in a close proximity of the most sensitive position in the percolation path (located in the interval between 25 nm to 35 nm), the resulting ΔV_G decreases

with the increase of V_G, replicating the experimentally observed behaviour of defect #4 in Figure 4.18 and as expected from the discussion in Section 4.3.2. The opposite behaviour, that is ΔV_G *increases* with the applied V_G, is observed when the trapped charge is located further away from this region, replicating the behaviour of the more common other defects in Figure 4.18. The responses for these charged defects are summarised in Figure 4.21. Another experimentally observed trend replicated in the simulations is that the responses from all of the defects converge at high absolute value of the gate voltage.

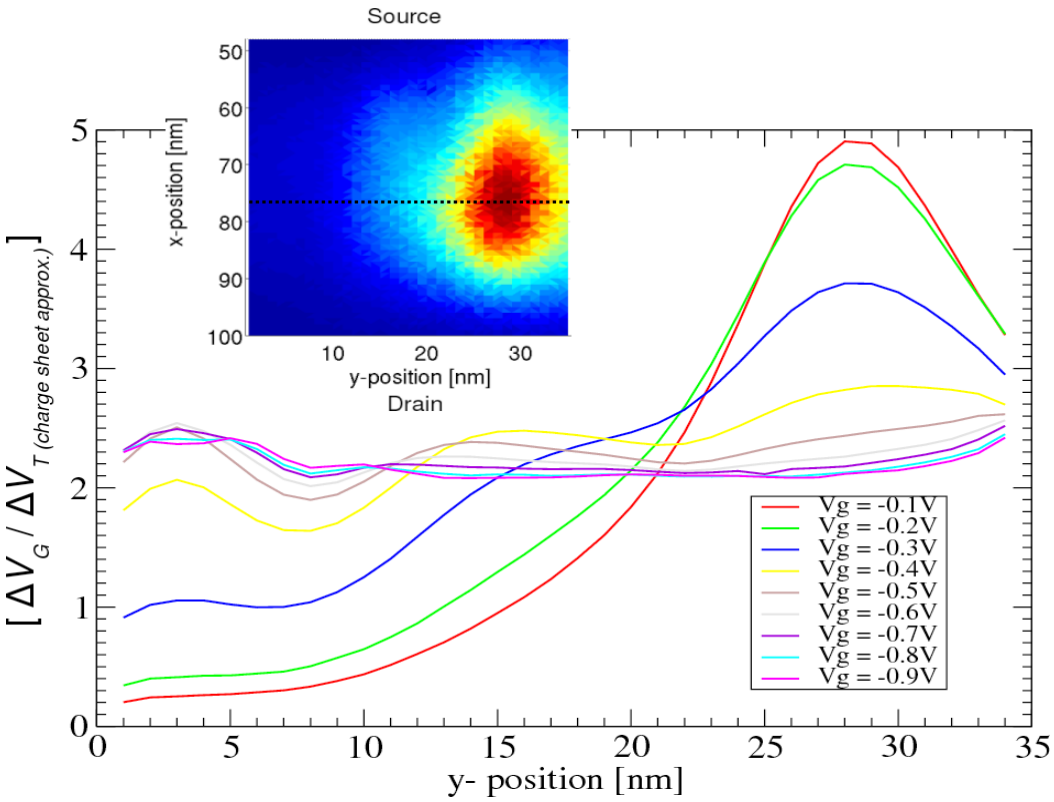

Figure 4.20: The ΔV_G registered by a single trapped charge at positions across the width of the device. Inset figure shows the sensitivity map of the entire channel area; the dotted line marks the path along which the trapped charge is placed. Large responses are observed when the charge is trapped in the sensitive regions which decreases with the increase in gate bias. The opposite V_G-dependence behaviour is observed when the charge is trapped outside the percolation path.

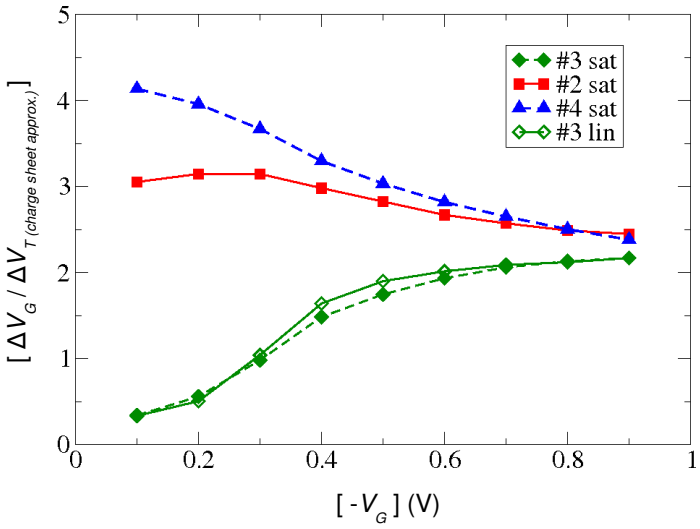

Figure 4.21: Selected defects from the simulations which closely replicate some of the experimentally measured responses shown in Figure 4.18. Based on the simulation, the gate voltage dependence response is found to be influenced by the relative location of the defect from the current percolation path.

4.5 Summary

In this chapter, the impact of a single interface-trapped charge on the characteristics of scaled MOSFETs has been investigated. A systematic simulation study was presented on the effects of a single interface-trapped electron in a realistic n-channel MOSFET, with the initial assumption of continuous charge representation of the device doping. The trapped charge was found to induce a localised suppression in the carrier density and surface potential responsible for the resulting current drop. The positional and bias dependence of the current drop was then investigated, from which a wide variation of the current change amplitude was found.

Armed with this basic understanding of the effects of a trapped charge, randomly positioned and discretely represented dopant charges were introduced into the

simulations, in addition to the presence of the single interface-trapped charge. The impact of atomic scale differences in doping configuration resulting in variation of the electrical characteristics of otherwise macroscopically identical transistors was briefly discussed. The introduction of random discrete dopants requires a statistical-scale simulation approach, because a single-device description is no longer apt for an ensemble of microscopically different devices, each of which has a unique fingerprint response to a trapped charge.

The introduction of discrete dopants extends the high-end tail of the distribution, resulting in substantially enhanced, albeit with relatively rare probabilities, magnitudes of current and threshold voltage change. The origin of such large responses is attributed to an unlucky random arrangement of doping configuration and its associated non-homogeneous potential landscape, and the charge trapping along the resulting current percolation path with high local current density. This broad spectrum of changes is not captured by the elementary one-dimensional charge sheet approximation, while the potential fluctuations from the discrete dopants elude the simulations based on continuum charge. In summary, the realistic use of discrete dopant distribution in the simulations is essential for the accurate estimate of statistical reliability effects and reproducing of the experimentally-observed distribution of electrical parameter shifts.

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Chapter 5

Statistical Simulation of Progressive PBTI Degradation

5.1 Introduction

Variability of electrical parameters which results from the discreteness of charge and matter in ultra-small devices, is one of the major challenges for the semiconductor industry [1, 2]. In addition, statistical aspects of MOSFET degradation associated with the trapping of carriers in stress-generated defect states at the channel-oxide interface and/or deeper into the gate stack dielectric are rapidly becoming a matter of growing concern [3, 4]. The stochastic trapping of individual or multiple discrete charges in defect states results in progressively larger temporary and permanent electrical parametric changes, creating acute problems in flash and SRAM memories [3, 5-7], as well as in digital logic blocks.

So far, this thesis has studied the electrostatic impact of a single trapped electron in an n-channel MOS transistor, and examined the effect of such a trapping event on the drain current and threshold voltage. MOSFET simulations which assumed devices with idealised continuous doping were unable to fully explain experimental measurements. The introduction of random dopants—a critical source of variability in conventional bulk MOSFETs [1, 2, 8]—resulted in significantly larger current and threshold voltage shifts across a device ensemble, and bore close qualitative resemblance to the experimentally observed distributions of RTS amplitudes. This is attributed to the critical current percolation paths with high localised current densities

shaped by the underlying random dopants, and chance charge-trapping events in these paths which produce extreme device parameter shifts.

However, the statistical simulations of Chapter 4 assume that the ensemble of transistors has a fixed *number* of trapped charge uniformly distributed across the ensemble. In reality, at any particular sheet density of interface defects, the number of trapped charge in each transistor varies statistically obeying a Poisson distribution. Under these realistic conditions, a transistor may have more than a single trapped charge or may have none at all. This will clearly affect the distribution of device currents and threshold voltages changes across the ensemble. An investigation into the impact of statistically distributed number of trapped charges—as opposed to the charges being uniformly distributed—will be presented in Section 5.3.

It has been widely reported that MOSFETs subjected to the stresses of high electric fields and elevated temperatures typically encountered during the routine operation of deep sub-micron devices may generate new interface defects [9-11]. Such phenomena include the Bias Temperature Instability (BTI) degradations, where the pre-existing interface defect density of a device increases when the annealed Si-H bonds at the interface gradually break. This microscopic structural damage consequently leads to a build-up of trapped charges. In addition to the clear and widely appreciated reliability issues resulting from BTI, the results from Chapter 4 indicate that such charge build up may have additional and disproportionate impact on device electrical parameters due to interactions with the intrinsic variability source. The remainder of this chapter will present statistical simulations of device parameters at various, increasing trapped charge densities as an analysis of this effect. The aim is to evaluate the impact of prolonged degradations in the presence of random dopants, the underlying dominant source of intrinsic variability.

5.2 Simulation Approach

The methods outlined in this chapter aim to investigate the impact of progressive degradations on the distribution of key electrical parameters, compared with the electrical parameters of 'fresh' transistors, in the presence of a dominant source of variability. The simulation approach 'freezes' the statistical description of the degradation at particular stage of degradation process, and evaluates the corresponding distribution transistor parameters. The degradation is described by the value of the average density of trapped charges, where the early, middle and advanced stage of the degradation are considered. For each sheet density of trapped charges, the distribution of the threshold voltage (V_T) and threshold voltage shift (ΔV_T) induced by statistical trapping of electrons on acceptor-type defect states at the Si/SiO_2 interface in n-channel MOSFETs, are calculated. This corresponds to Positive Bias Temperature Instability (PBTI) degradation which is observed in n-channel MOSFETs with high-*k* gate stacks. Statistical ensembles of 1000 microscopically unique (in terms of atomic dopant distribution) MOSFETs are simulated using the Glasgow 3D 'atomistic' device simulator described in detail in Chapter 3. The reference device is based on a real 35 nm gate length n-channel MOSFET fabricated and published by Toshiba [12].

5.2.1 The Justification for the Choice of Simulated Device

Although the main reliability concern in poly-silicon gate CMOS is the Negative Bias Temperature Instability (NBTI) related to holes trapping in p-channel MOSFETs, an n-channel testbed device is used in this work in order to maintain methodological consistency with the earlier phase of this research presented in Chapter 4. A study based on NMOS devices will also contribute towards the existing body of knowledge, because a string of previous papers have already extensively studied their statistical variability [8, 13-15]. In addition, high-*k* based dielectrics have been adopted in the 45 nm technology by Intel [11, 16] as a replacement for SiO_2 gate oxides in order to suppress gate leakage current in ultra-scaled devices. Despite the higher dielectric

constant enabling increased oxide thickness and reduced gate leakage, the reliability of high-*k* gate oxides has been a subject of much scrutiny due to their inherently higher defect density [17-19], which brings the relevant concerns of PBTI in n-channel MOSFETs into picture [20, 21]. The practical aspect of reliability study on NMOS devices is also supported by other studies which have shown that carrier-trapping-induced parametric fluctuations in n-channel MOSFETs may adversely affect the operations of flash memories [5, 6, 22], which rely on electron-trapping mechanisms to represent the stored bit logic state.

5.2.2 Statistical Assignment of Trapped Charges

The number of trapped charges across an ensemble of MOSFETs varies statistically and is commonly assumed to follow a Poisson distribution. The Poisson distribution is a discrete probability distribution which expresses the probability of a number of events occurring in a fixed period of time (or any other pre-defined intervals such as area, volume or distance), if these events occur with a known average rate and independently of the time since the last event. A Poisson distribution with, on average, of one interface-trapped charge in the simulated square 35 × 35 nm MOSFET corresponds to a trapped charge sheet density of approximately 1×10^{11} cm^{-2}. For a given average number of trapped charge, the actual number of trapped charge in each MOSFET of the simulation sample is randomly generated based on a Poisson distribution with the above mean, and then each trapped charge is independently assigned to a random locations in the channel-oxide interface plane. As a result, both the number and position of the individual trapped charges vary from one transistor to another. The 3D simulations of the 1000 devices—now including a number of trapped charges—are then repeated and the differences between the fresh and degraded device characteristics are recorded.

By increasing the expected number of the trapped charges, μ , in the distribution, the effect of increasing sheet density of trapped charges due to progressive degradation

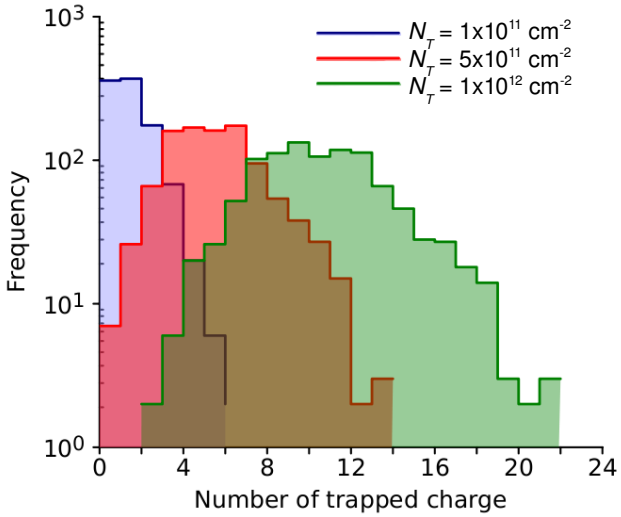


Figure 5.1: The distribution of the number of trapped charges in the simulated ensembles of 1000 MOSFETs is modelled by a Poisson distribution for a given N_T with its mean (μ) corresponding to the average number of trapped charge found in the whole sample.

can be simulated and studied. Four different μ's are chosen to represent different stages of the PBTI degradation, which are the early (μ=1), intermediate (μ=3 and μ=5) and later (μ=10) ageing stages. These approximately correspond to trapped charge sheet densities $N_T = 1 \times 10^{11}$ cm^{-2}, $N_T = 3 \times 10^{11}$ cm^{-2}, $N_T = 5 \times 10^{11}$ cm^{-2} and $N_T = 1 \times 10^{12}$ cm^{-2} respectively. The distribution of the number of trapped charges for the different N_T's in the simulated ensemble of 1000 units of MOSFETs is given in Figure 5.1. The number of trapped charges has a zero-bound, single-sided distribution in the early phase of the degradation where a relatively large proportion of the simulated transistors do not have any trapped charge at all. The distribution of trapped charge broadens as the degradation progresses from mid-stage to the advanced regime, and evolves into an approximate bell-shaped distribution. At this stage, for a given probability level, a transistor can either have relatively few or large number of trapped charges, which corresponds to either the left or right tail of the distribution.

5.3 The Effects of Statistical Distribution of Trapped Charges

Previous 3D simulation studies of single charge-trapping in idealised MOSFET structures have already demonstrated that the inclusion of random discrete dopants is essential for reproducing both the shape and the magnitudes of the experimentally observed RTS distributions [22-25]. However, with the exception of [25], the studies have focused on the impact of only a single stray charge and did not consider the statistical distribution of the number of charged defect states in a single transistor. In order to realistically predict the reliability of the device under the onslaught of stress-generated fixed and trapped charges, it is imperative not only to consider realistic device structures and doping profiles, but also a statistically representative distribution of the trapped charges.

The distribution of threshold voltage shift, ΔV_T , obtained from simulations of 1000 microscopically unique MOSFETs with *an average* of one trapped charge in each member of the ensemble is presented in Figure 5.2. The ΔV_T distribution presented in Chapter 4, where *each* of the devices has been fixed to have a single randomly trapped charge, is reproduced in the same figure for comparison. There are three noticeable consequences of statistical modelling in the number of trapped charges: first, an increase of the average ΔV_T to 4.42 mV from 3.90 mV when the number of traps is fixed; second, the occurrence of large ΔV_T values is enhanced, as shown by the vertically-shifted right tail, contributing to the overall increase in the average of ΔV_T; finally, the statistical assignment of trapped charge extends the high-amplitudes tail of the ΔV_T distribution resulting in a larger maximum threshold voltage shift of nearly 30 mV, compared to a maximum shift of approximately 14 mV when the number of trapped charges is fixed to one.

Such a widening of the distribution can be explained by the presence of multiple

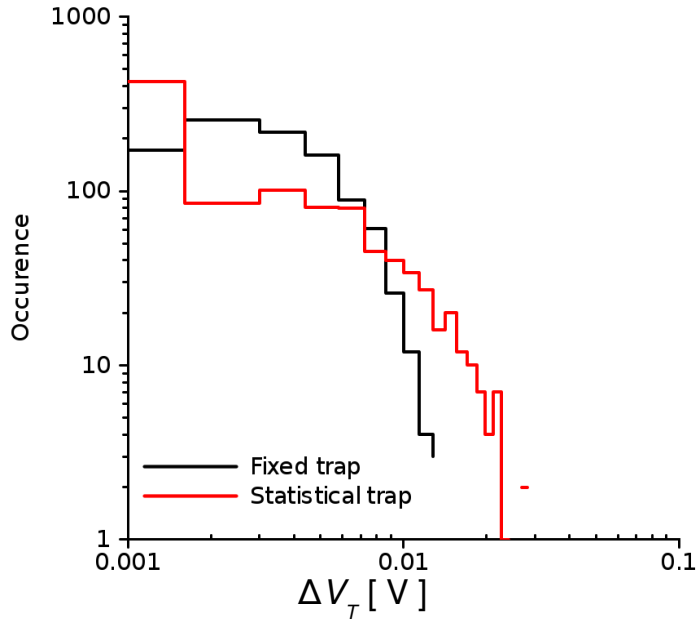


Figure 5.2: The distribution of threshold voltage change in an ensemble of 1000 units of MOSFETs simulated with statistical number of trapped charges and uniformly fixed, single trapped charge.

trapped charges and their combined effects, resulting in larger ΔV_T values. This is confirmed by an inspection of a device sampled from the high amplitude tail, shown in Figure 5.3. This particular MOSFET which records a threshold voltage shift of 26.5 mV has, by chance, 3 trapped charges all of which happen to be aligned across the dominant current path resulting in great suppression of the local carrier concentration and the overall current flow. The Poisson statistics also dictates that a certain number of transistors in the ensemble will not have any trapped carriers. This explains the higher density at the lowest amplitudes end of the distribution compared to the case of fixing a single charge to be trapped in each of the transistors.

The next pertinent question is: does the statistical treatment in assigning the number of trapped charges also modify the degree of correlation between the pre-stress V_T and

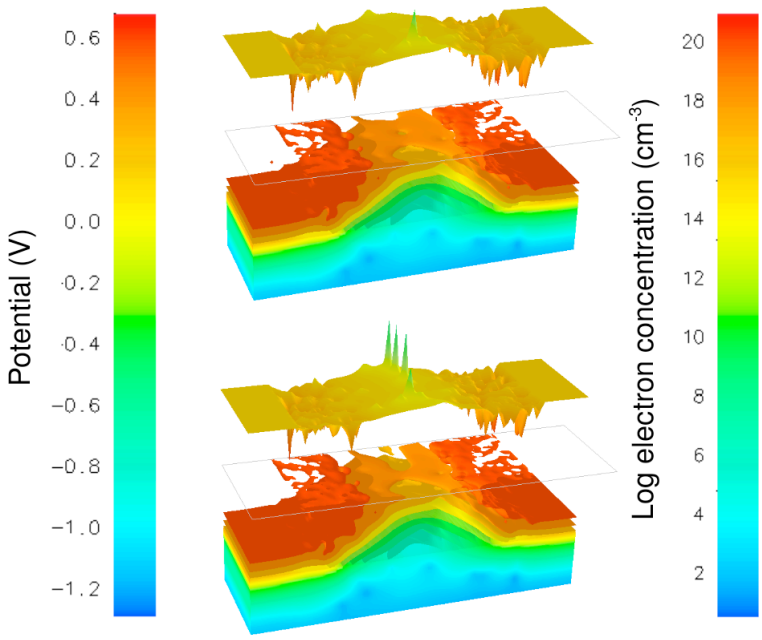


Figure 5.3: Electron concentration at threshold gate voltage in a MOSFET with large threshold voltage change; (*top figure*) with no trapped electrons; (*bottom figure*) with randomly trapped carriers blocking the main current path. The top planes show the potential at the Si/SiO_2 interface plane, from which the presence of discrete dopants and trapped charges can be inferred by the associated sharply peaked Coulomb potential.

the post-stress ΔV_T ? The scatter plot of the V_T and its corresponding ΔV_T for each transistor is illustrated in Figure 5.4, showing little correlation. However, a calculation of the correlation coefficient yields a small *negative* value of -0.0394, implying that devices with higher initial V_T values are statistically not likely to have high ΔV_T. This result contradicts to the situation when each transistor in the sample is fixed to have a single trapped charge, yielding a small *positive* correlation coefficient of 0.0011 as presented in Section 4.44 of Chapter 4. The positive correlation in such simulation setting implies the high V_T devices would be more likely to have high ΔV_T. Because identical ensembles of transistors (in terms their microscopic distribution of dopants)

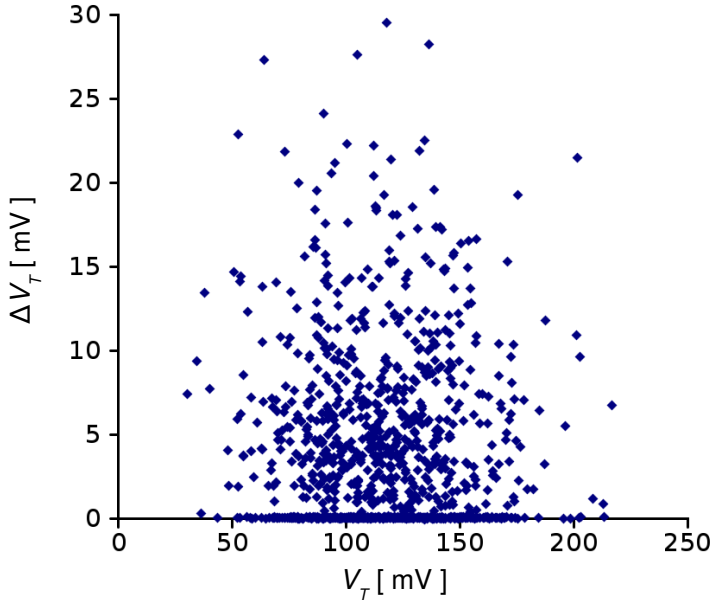


Figure 5.4: Correlation plot between initial threshold voltage in 1000 'fresh' devices and their post-stress threshold voltage shifts subjected to trapped charge density of N_T = 1 × 10^{11} cm^{-2}. The number of trapped charge in each transistor is randomly generated based on a Poisson distribution with an average value of one.

are simulated in both settings, it is clear that the contradictory V_T - ΔV_T correlations must be a result of the way the trapped charges are distributed.

When each of the transistors has a single trapped charge, the high V_T devices are statistically likelier to generate large ΔV_T values, owing to the presence of well-defined current percolation paths which are determined by the dense underlying distribution of random discrete dopants in the channel. These critical current paths are absent in low V_T devices, thus a single charge trapping event would likely result in a minimal impact on its current. However, this correlation no longer holds when the number of trapped charges varies statistically, allowing a transistor to have multiple trapped charges. In such cases, even low V_T devices can give large responses to trapped charges due to the *combined* impact of multiple trapped charges.

5.4 Impact of Progressive Degradation

Degradation mechanisms related to fixed and trapped charge, including BTI and HCI degradations, are usually characterised by a progressive changes in device parameters. Most often the threshold voltage is monitored and is related to corresponding changes in the sheet density of trapped and/or fixed charges. The degradation is associated with an increased number of discrete charges trapped at the interface or deeper within the gate dielectric. An important question is how do these extra trapped charges affect the initial random-dopant-induced parameter distribution, in particular, the threshold voltage distribution. The evolution of this distribution will exacerbate the statistical variability problems already extant in fresh circuits.

5.4.1 Evolution of Threshold Voltage Distribution

The evolution of threshold voltages from the statistical simulation of 1000 MOSFETs as a result of progressive increase of the sheet density of trapped electrons, N_T, is plotted on the normal probability plot in Figure 5.5 and summarised in Table 5.1. A normal probability plot is a graphical technique to assess the normality of the distribution, and it aids a rapid visual identification of a normal distribution. Normally distributed data points would form a straight line when plotted on a normal probability plot; a departure from a straight line indicates a departure from normal distribution. The slope of the line corresponds to the dispersion of the distribution; a steep line indicates a tight distribution while a horizontally-inclined line characterises a distribution with a wide variability.

It can be seen that even in the absence of trapped charges in the ‘fresh’ transistors, the threshold voltages are already widely distributed due to the random-dopant-induced variability with a small number of transistors having threshold voltages which deviate from a normal distribution as shown in the tails. The progressive degradation and its associated increase in trapped charges exert two noticeable effects on threshold

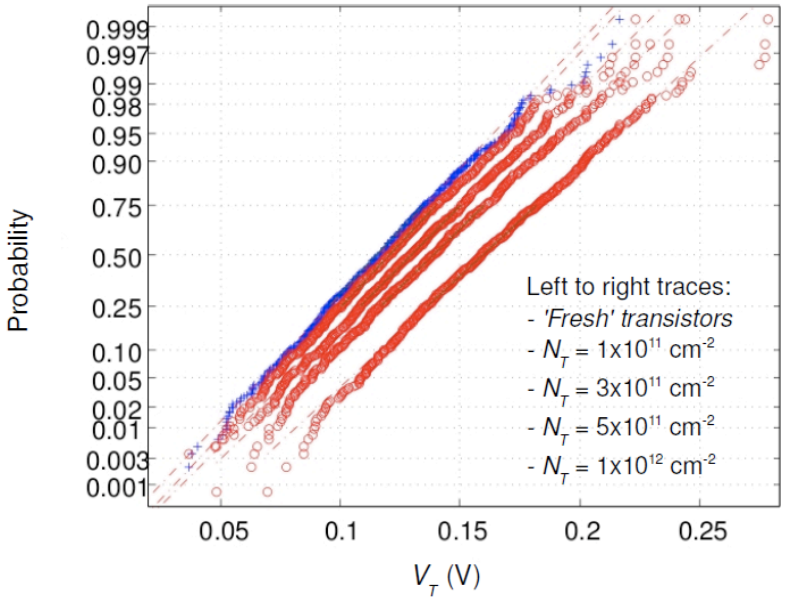


Figure 5.5: Distribution of threshold voltages in 1000 'fresh' (blue crosses) and 'degraded' (red circles) MOSFETs subjected to progressive increase of the sheet density of trapped electrons.

N_T (cm^{-2})	Average number of trapped charges	Average V_T (mV)	σV_T (mV)
0	0	116.4	30.0
1 × 10^{11}	1	120.7	30.5
3 × 10^{11}	3	129.7	31.6
5 × 10^{11}	5	138.5	31.9
1 × 10^{12}	10	159.8	33.4

Table 5.1: V_T distributions at various instances of increasing trapped charge densities N_T.

voltage distribution:- i) An almost linear increase in the average V_T which is to be expected from the simple relationship between the charge and voltage drop in a MOS capacitor; and, ii) Broadening of the V_T distribution with the standard deviation increasing by approximately 3 mV at $N_T = 1 \times 10^{12}$ cm^{-2}. In addition, the magnitude of deviations from normality at the high V_T tails—especially important from reliability point of view—grows increasingly large with the increase in degradation levels. It is expected that such deviations will be of higher occurrences and of bigger magnitudes in digital circuits when millions of transistors are subjected to the degradations.

An alternative representation of the impact of this progressive degradation is by the distribution of threshold voltage change, ΔV_T, between the fresh and the degraded devices at different trapped electron sheet densities. These are presented in Figure 5.6. It can be seen that the increased densities of trapped charges evolve the shape of the ΔV_T distribution from a single-sided distribution into a Gaussian-like distribution centred around the average ΔV_T associated with the corresponding trapped sheet

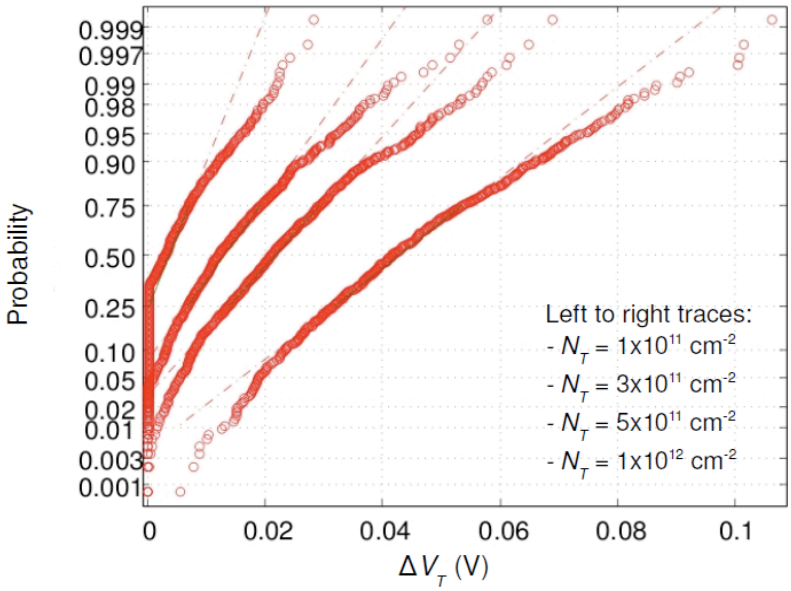


Figure 5.6: The distribution of threshold voltage change in 1000 nMOSFETs subjected to progressive increase of the sheet density of trapped electrons.

N_T (cm-2)	Average number of trap	Average ΔV_T (mV)	ΔV_T (0.1%) (mV)	Rare/ Average
0	0	-	-	-
1×10^{11}	1	4.4	30	6.8
3×10^{11}	3	13.4	58	4.3
5×10^{11}	5	21.7	70	3.2
1×10^{12}	10	43.4	108	2.5

Table 5.2: Effect of the increased sheet density of trapped charge and the relative magnitude of rare threshold voltage shifts.

charge density. In the early phase of degradation when the average number of trapped charges from the Poisson distribution is only one, a large population of the ensemble would not have any trapped charge at all and thus records no increase in their threshold voltages.

As the number of trapped charges is generated based on Poisson distribution where the variance of the distribution is equal to the mean, the spread in the number of additional charges becomes significantly larger at higher trapped charge densities. This consequently leads to the wider spread in the threshold voltage shift distributions with increasing trap density, which can be seen by the change in the slope of the distributions. This is also compounded by the dependence of the threshold voltage shifts on the locations of the trapped charges, where unlucky charge-trapping along significant current paths would result in large threshold voltage shifts. It should also be noted that while the pre- and post-degradation V_T distributions generally follow a normal distribution at the various instances of trapped charge densities (Figure 5.5),

the *difference* between the V_T distributions which give the ΔV_T distributions, are clearly non-normal. Table 5.2 summarises the relation between the average ΔV_T and the ΔV_T occurring at 0.1% probability level at the different sheet densities of the trapped charge. It is clear that with each increase of the trapped charge density the difference between the average ΔV_T and the rare ΔV_T decreases from 6.8 times at 1×10^{11} cm^{-2} to 2.5 times at 1×10^{12} cm^{-2}.

The statistical trends obtained from the simulations compare well with published experimental measurements. Huard *et al.* have reported the distribution of ΔV_T

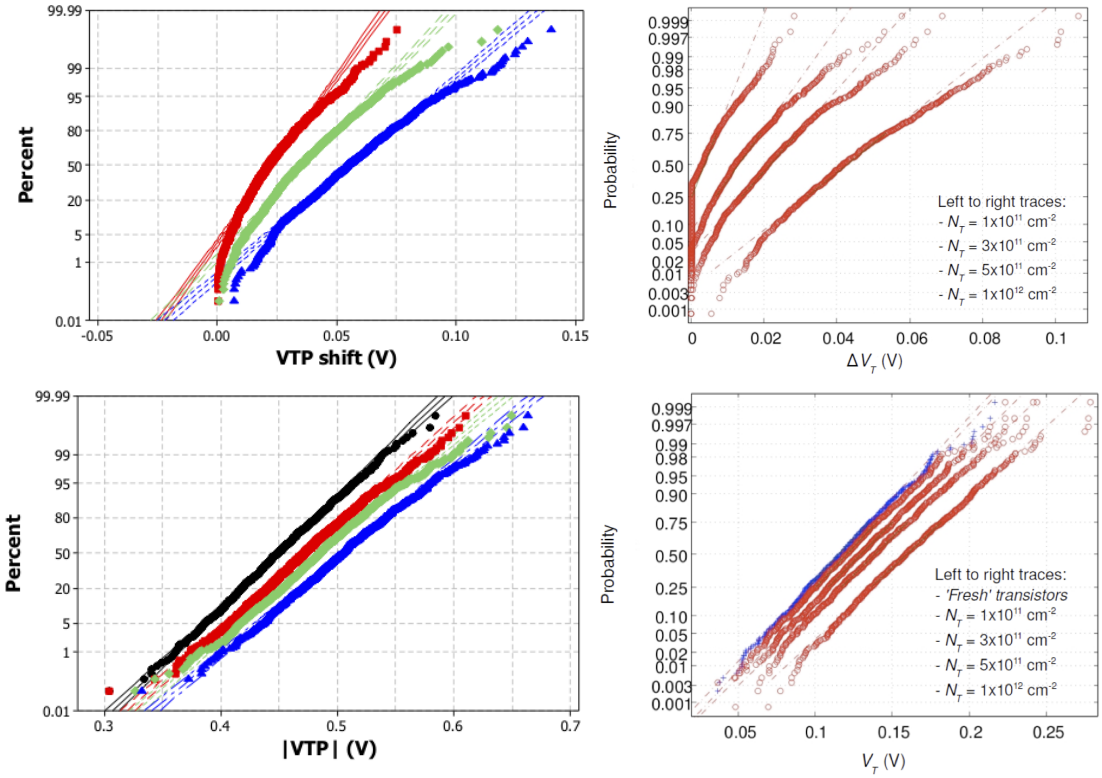


Figure 5.7: (*Left top and bottom*) The experimentally measured distribution of threshold voltage change and threshold voltage of more than a thousand PMOS transistors at three different stress times; after Huard *et al.* [26]. (*Right top and bottom*) The corresponding simulation results of this work.

observed in more than a thousand SRAM-sized PMOS transistors from a 45 nm process flow from ST Microelectronics, measured at three different stress times [26]. The measurements are shown in Figure 5.7 with the corresponding simulation results of this work shown earlier in Figures 5.5 and 5.6 reproduced alongside to aid comparison. Despite the apparent difference in the types of devices measured/ simulated and stress levels representation (Huard reports the applied stress as a function of time), it is clear that the simulations reproduce some key qualitative trends of the experimentally observed distributions. Both works demonstrate that approximating the distributions of ΔV_T by a normal distribution underestimates the high ΔV_T tails. Additionally, the spread of the ΔV_T distribution increases dramatically with the trapped charge densities associated with prolonged stress. The corresponding experimentally measured V_T distributions from the same sample—before and after the three distinct stress levels—is shown in the bottom of the same figure. The same

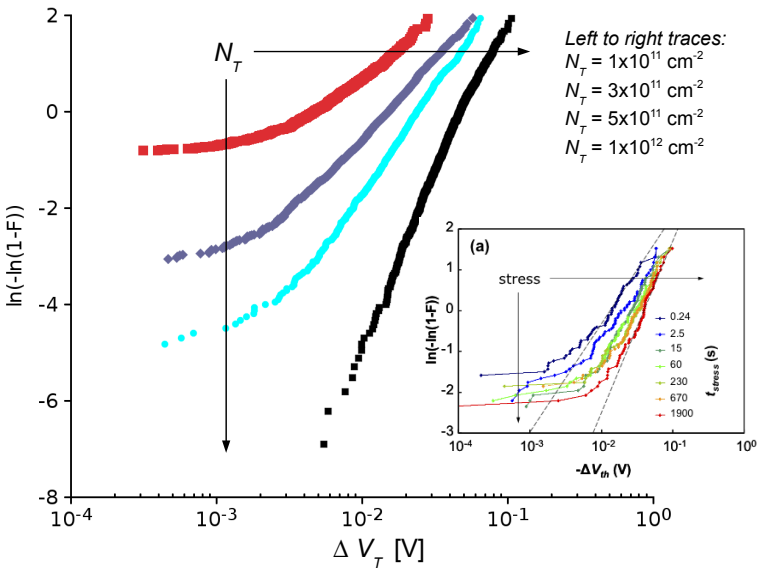


Figure 5.8: Weibull plot of the distribution of threshold voltage change in 1000 nMOSFETs subjected to progressive increase of the sheet density of trapped electrons. Inset: Distribution of threshold voltage change from 72 pMOSFETs measured at various increasing stress times, after [27].

statistical trend is also produced by the simulations from this work, shown alongside. In both works, the V_T distribution, before and after stress, closely follows a normal distribution with increasing variance with the increase of stress levels.

In Figure 5.8, the probability distribution of threshold voltage change from the simulation is replotted on a Weibull plot, with the inset figure showing experimental measurements of threshold voltage change recorded from 70 nm gate length pMOSFETs at increasing stress times as reported in [27]. We note that in both works the magnitude of maximum ΔV_T increases with stress, as shown by the horizontal shift in the high-end tails. Additionally, the plot emphasizes the effect of increased stress on the probability distributions of small ΔV_T's, which are seen to dramatically decrease as the trapped charges accumulate resulting in larger minimum ΔV_T's, as indicated by the vertical down-shift of the low-end tails.

Despite the qualitative similarity of the distributions of V_T and ΔV_T between the simulation results of this work and the reported experimental measurements, one may still have reasonable concerns on the validity of comparing the degradation of the nMOSFETs simulated in this work against the experimentally measured pMOSFETs of Figures 5.7 and 5.8, because the comparisons are between devices of different types and technologies. Unfortunately, a direct verification by simulating an exact replicate of an industrially-relevant device was not possible to be carried out in this work. This is because it is very difficult for the purpose of this Ph.D study to obtain access to real device descriptions and technology from the industry due to such information being closely guarded intellectual property. Due to this practical limitation, the choice of template device for this Ph.D study is limited to the 35 nm Toshiba nMOSFET, primarily because its design is readily available from the literature [12, 28]. However, to the best of our knowledge, there has been no published report of experimental measurements of BTI degradation of devices similar to the one we adopt in our simulations.

Even though the our choice of template device does not allow a direct comparison with any corresponding experimental measurement, the validity of our simulation approach has been confirmed by a more recent simulation-and-measurement study [29] of NBTI degradation of realistic devices carried out independently of this Ph.D study by the Device Modelling Group (University of Glasgow) with industrial collaborators from ARM (UK) and ST Microelectronics (Italy). The study was carried out within the framework of European Community funded project named REALITY (Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies) [30]. The Glasgow team was granted confidential access to low-power transistors developed by ST Microelectronics based on their 45 nm process platform. This has allowed, for the first time, a direct comparison of NBTI effects predicted by Glasgow 'atomistic' statistical simulations against corresponding experimental measurements of an equivalent device. Incidentally, ST Microelectronics has also allowed the results of this successfully-rated project to be published in IEEE Transactions on Electron Devices [29], therefore the comparison are reproduced in Figure 5.9 with the permission of the authors.

In Figure 5.9, the top figure shows the threshold voltage (V_T) distribution obtained from 200 45-nm pMOSFETs simulated by the Glasgow team with trap sheet densities of 1×10^{11}, 5×10^{11} and 1×10^{12} cm^{-2}, while the inset shows the corresponding experimental results for an ensemble of similar devices measured and published by ST Microelectronics [26]. The bottom figure shows the simulated and measured (inset) [26] distribution of threshold voltage *change* (ΔV_T) of the same sample of devices for the same sheet densities of trapped charges. It can be seen from Figure 5.9 that the simulation results are in excellent agreement—both qualitative and quantitatively—with the experimental measurements by reproducing all the major features of the degradation, which are non-normality of the V_T and ΔV_T distributions as well as increased variability with the increased in trapped charge density.

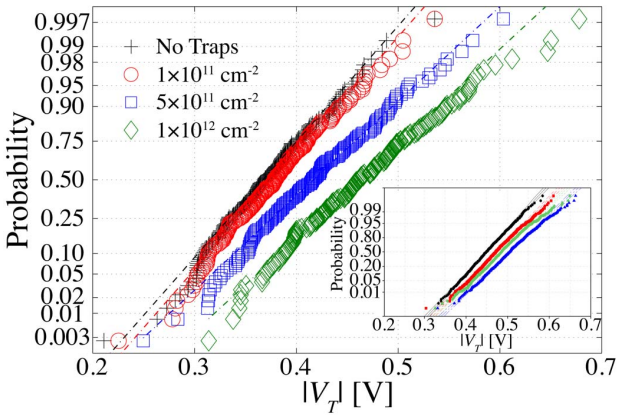
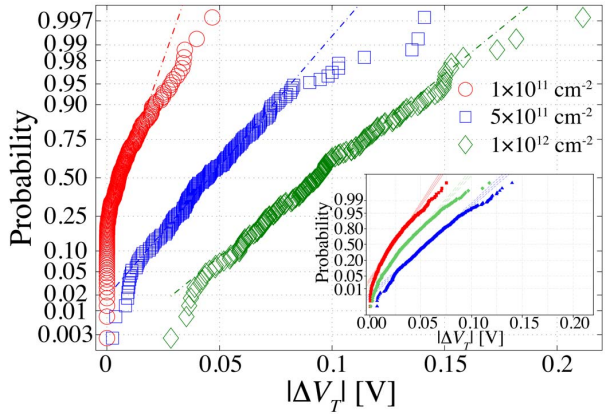


Figure 5.9: (*Top*) Threshold voltages V_T of 200 microscopically different 45-nm p-channel devices simulated in with trap sheet densities of 1×10^{11}, 5×10^{11} and 1×10^{12} cm^{-2}. Inset shows experimental results for a similar device [26]. After [29].



(*Bottom*) Threshold voltage change ΔV_T of the same 200 simulated devices. Inset figure shows experimental results for a similar device [26]. After [29].

The significance and relationship of these results to this Ph.D study is as follows:- the simulations carried out for the REALITY project was based on the same simulation approach first developed in this Ph.D work. In both works, the simulations are *frozen-in-time* (hence they disregard the time-varying trapping/detrapping and recovery processes) by taking snapshots of the degradation represented by different levels of trapped charge density; the trapped charges are assumed to be randomly distributed in the Si/SiO_2 interface plane only; and the correlation between the trapped charge location with the underlying channel dopants is neglected. Even with these necessary simplifications, the simulations for REALITY agree well with the corresponding experimental measurements of the same device. These results have been published in a reputable peer-reviewed journal [29] and the simulation methodology is now widely adopted by the industry. In another study by the Device Modelling Group, the exact simulation approach was adopted to investigate PBTI/NBTI related variability in 32-

nm thin-body silicon-on-insulator (TB-SOI) and 22-nm double-gate (DG) MOSFETs; the results of which were reviewed and published in IEEE Electron Device Letters [31]. These are clear indications that our approach of modelling the PBTI/NBTI degradation is a well-accepted engineering approach which has also been verified by experimental measurements. Despite the fact that this Ph.D study does not have access to a real device from the industry, the simulation approach first developed in this work has been directly verified by the experimental measurements carried out for the REALITY project, and is well-accepted by the research community as demonstrated by the publications in the well-ranked journals.

5.4.2 Variability-Enhanced Degradation

Interestingly, qualitative agreement between the simulations and experimental measurements can only be attained if the dominant source of intrinsic parameter fluctuations introduced by random discrete dopants is accounted for in the simulations. To demonstrate this point, a statistical simulation of 1000 MOSFETs without considering the effects of random discrete dopants are conducted. In these simulations, the MOSFETs are also subjected to the same increasing sheet densities of trapped charges. The resulting V_T distribution is presented in Figure 5.10. The experimentally observed V_T distribution [26] shown earlier in Figure 5.7 is reproduced along with the results when random dopants are accounted for in the simulations as presented earlier in Figure 5.5.

It can be clearly seen that when the effects of random discrete dopants are neglected in the simulations, the resulting shape of V_T distributions due to progressive degradation are in stark contrast to experimental measurements. In the absence of random-dopants-induced variability, V_T distribution deviates markedly from normality and its variance increases dramatically as the trapped charge density increases. This result suggests that the experimentally observed distribution of the V_T due to charge-trapping degradation is a result of the statistical interplay between the trapped charges and the

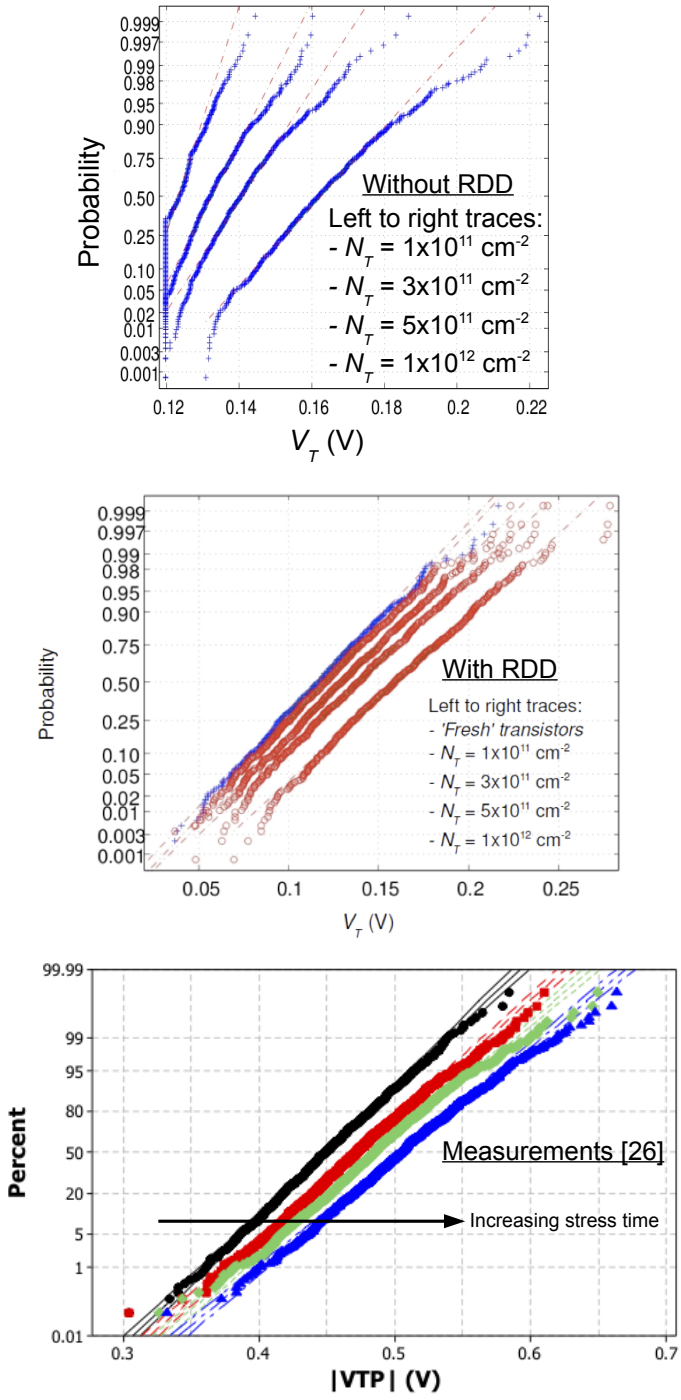


Figure 5.10: (*Top*) V_T distribution obtained from simulations of MOSFETs subjected to progressive degradation without considering for the effects of random discrete dopants. (*Middle*) Corresponding distributions when the simulations take into account the random dopants effects. (*Bottom*) Experimentally measured V_T distributions [26].

underlying distribution of random dopants within the devices. It also further reinforces the necessity to account for the dominant source of intrinsic variability in the device simulations of statistical reliability.

To further highlight the effects of random discrete dopants on the magnitude of ΔV_T induced by the trapped charges, the relative threshold voltage change ($\Delta V_T/V_{Tref}$) for each transistor is calculated, where V_{Tref} is the initial threshold voltage of the transistor before degradation i.e. at 'fresh' state. Figure 5.11 shows the distribution of $\Delta V_T/V_{Tref}$ from both the simulations with and without accounting random discrete dopants. It can be seen that the inclusion of random discrete dopants produces a maximum ΔV_T nearly twice the magnitude of its 'fresh' threshold voltage, as well as a more pronounced increase in the variance of the distributions at each N_T. This is because in

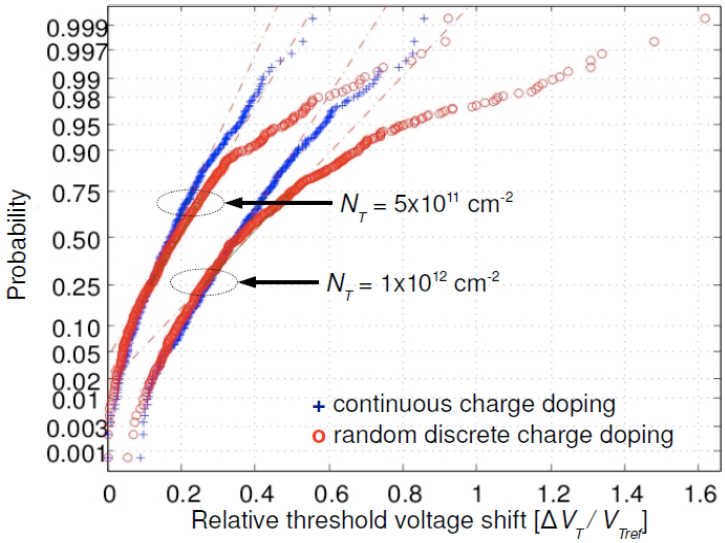


Figure 5.11: Relative threshold voltage change ($\Delta V_T/V_{Tref}$) distribution from simulations of MOSFETs with continuous doping and random discrete dopants subjected to the same increasing densities of trapped charges. The inclusion of random discrete dopants produces maximum threshold voltage shift nearly twice the of 'fresh' threshold voltage, and increases the variance of the distributions.

devices with continuous charge doping, the V_{Tref} is identical for all devices, thus the magnitude of $\Delta V_T/V_{Tref}$ ratio is solely determined by the effect of the trapped charge alone as manifested in the magnitude of post-degradation ΔV_T. But in devices with random discrete dopants, the V_{Tref} varies from one transistor to transistor and is uniquely determined by the number and spatial configurations of the underlying random discrete dopants within the active region of the each individual transistor [13, 14, 32-34]. The magnitude of the $\Delta V_T/V_{Tref}$ ratio in the case of atomistic doping is therefore determined by both the initial 'fresh' state V_{Tref} and the post-stress ΔV_T — both of which are also influenced by random-dopants-induced statistical variability. Thus, the presence of statistical variability enhances the statistical aspects of degradation by inducing extreme shifts in the threshold voltage and broadening of the distributions.

5.4.3 Correlations

The simulations performed in this work assume that the density of trapped charges in a device is independent of its initial V_T and the traps are uniformly distributed throughout the interface plane. An analysis of the correlation between the initial V_T and post-stress ΔV_T reveals negligibly small negative correlation for all densities of trapped charges, as shown in scatter plots of Figure 5.12 and summarised in Table 5.3. The negative correlation implies that the effect of the trapped charge is statistically less pronounced in devices with higher initial V_T, and that large ΔV_T values do not necessarily add to the large random-dopant-induced V_T. Due to the weak correlations, the threshold voltage shifts can be studied independently from the initial pre-stress threshold voltage distribution. These weak correlations between initial V_T and post-stress ΔV_T are also in agreement with experimental observations in SRAM devices reported in [3] and 70 nm gate length p-channel MOSFETs [27].

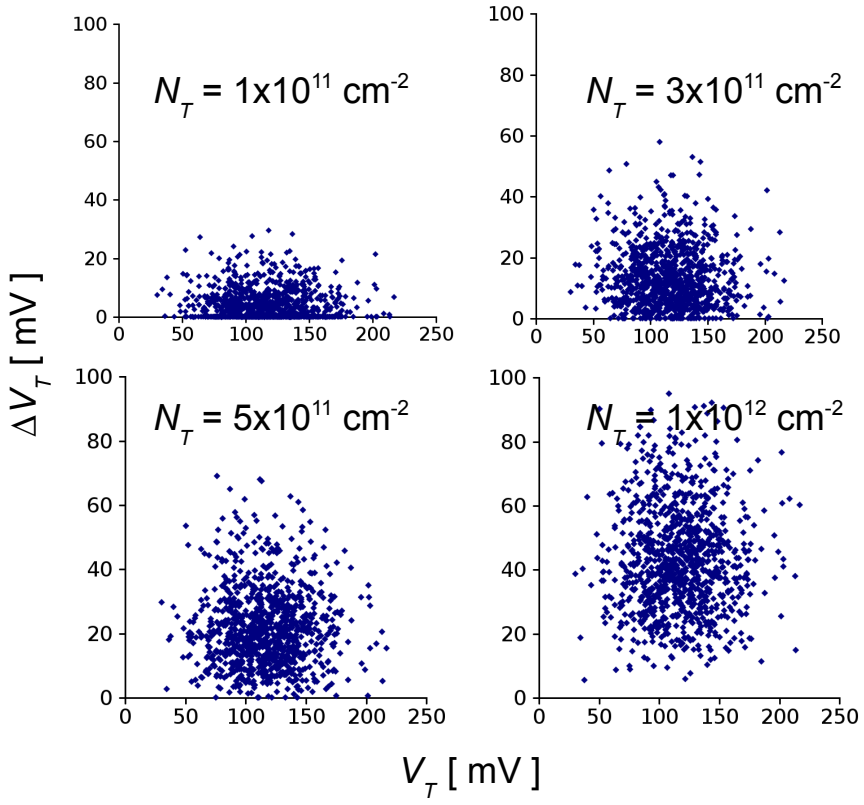


Figure 5.12: Correlation plot between initial threshold voltage V_T in 1000 'fresh' devices and their post-stress threshold voltage shifts ΔV_T at four levels of interface-trapped charge density N_T .

	ΔV_T			
V_T	-0.039 N_T=1 ×10^{11} cm^{-2}	-0.044 N_T=3 ×10^{11} cm^{-2}	-0.028 N_T=5 ×10^{11} cm^{-2}	-0.047 N_T=1 ×10^{12} cm^{-2}

Table 5.3: Correlation coefficient between pre-stress threshold voltages V_T and the corresponding post-degradation threshold voltage shifts ΔV_T of the 1000 units of simulated transistors at various instances of increasing interface-trapped charge density N_T.

5.4.4 Comparison Against Theoretical Predictions

Figure 5.13 depicts the average ΔV_T and the standard deviation of the threshold voltage shifts, $\sigma(\Delta V_T)$, for different sheet densities of trapped charges obtained from the simulations and compared against simple theoretical approximations. Also shown in the plot are the corresponding results from continuous doping simulations. The change in V_T corresponding to expected number of trapped charges μ is given by:

$$\Delta V_T = \frac{Q_T}{C_{OX}} = \frac{qN_T t_{OX}}{\epsilon_{OX}} = \frac{q\mu t_{OX}}{\epsilon_{OX} WL} \tag{5.1}$$

where Q_T and C_{OX} are the total charge of the trapped electrons per unit area and the oxide capacitance per unit area respectively, t_{OX} is the oxide layer physical thickness and ε_{OX} is its permittivity. The analytical expression for the standard deviation of threshold voltage shifts based on the number variation of trapped charges is given by:

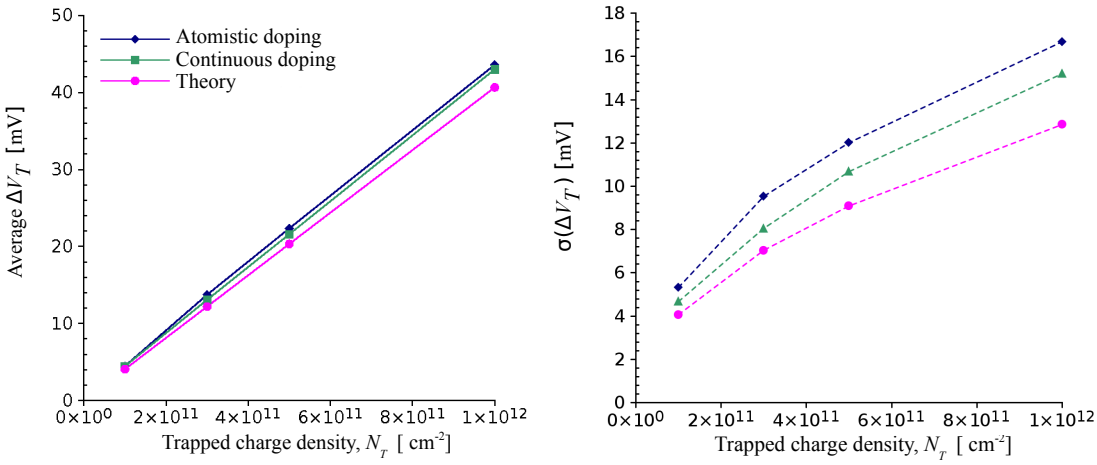


Figure 5.13: (*Left*) Average threshold voltage change, and (*Right*) its standard deviation as a function of interface trap density obtained from the simulations compared against calculations.

$$\sigma(\Delta V_T) = \frac{qt_{OX}\sigma(N_T WL)}{\epsilon_{OX} WL}$$

$$= \frac{qt_{OX}\sqrt{\mu}}{\epsilon_{OX} WL} \tag{5.2}$$

where *WL* is the area of the channel; hence, ($N_T WL$) is the expected number of trapped charges in the channel, μ. Assuming that the actual number of trapped charges follows a Poisson distribution, it then has standard deviation $\sigma(N_T WL) = \sqrt{\mu}$. Not surprisingly the simple expression, which takes into account only the variation in the number of trapped charges, underestimates the average ΔV_T and its standard deviation for all levels of degradation. This is due to the fact that at even for a constant number of trapped charges, their random positions, in conjunction with the underlying randomness of the channel dopants, introduce significant variation in the ΔV_T.

From Figure 5.13 it can also be seen that the 3D continuous doping simulations which capture the impact of random spatial positions of the trapped charges on the magnitudes of ΔV_T , in addition to the variation in the number of trapped charges, result in an increased average ΔV_T and standard deviation compared to the theoretical calculations which capture only the trapped charge number variation. The introduction of random dopants into the simulation further increases the average magnitudes of the V_T shifts and widens its distributions. Following the method outlined in [26], the relative contribution of the position of the trapped charges and the random dopant fluctuations to the variance of the ΔV_T distribution can each be ascertained. The threshold voltage shift ΔV_T is related to the number of trapped charges, *N*, by:

$$\Delta V_T = \frac{q.N}{C_{OX} WL} = K_N.N \tag{5.3}$$

Assuming the variation in the number of trapped charges follows a Poisson distribution, we have:

$$\mathrm{Var}(N) = \mathrm{Mean}(N) = \frac{\mathrm{Mean}(\Delta V_T)}{K_N} \tag{5.4}$$

Variance of ΔV_{T} can then be written in terms of mean ΔV_{T} , K_N and constant K :

$$\mathrm{Var}(\Delta V_T) = K.K_N.\mathrm{Mean}(\Delta V_T) \tag{5.5}$$

When constant K is equal to 1, only the fluctuation in the number of trapped charges is accounted for in the variation of threshold voltage shift. Constant K is thus introduced to accommodate the additional variance in the threshold voltage shift contributed by the spatial variation of the trapped charges and the random dopants.

Figure 5.14 shows the plot of variance of ΔV_{T} against mean ΔV_{T} obtained from the simulations and theory, with the value of constant K calculated from the slope stated for each simulation type. K is highest in the case of atomistic doping simulation which results in the largest variation of ΔV_{T} . It can be inferred from the graph that the position of the trapped charge and the random dopants each contribute equally to the

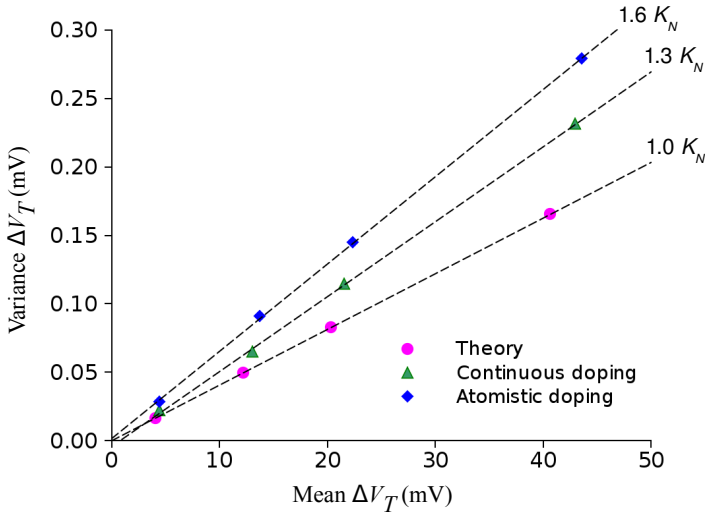


Figure 5.14: Variance of threshold voltage shift ΔV_{T} is fully described by mean ΔV_{T} and constant K, which quantifies the impact of the position of the trapped charge and random dopants on the ΔV_{T} distribution.

total variation of threshold voltage shifts. It can also be noted from the figure that the variance of the ΔV_T can be fully described by K and mean ΔV_T for all of the simulated interface trapped charge densities.

5.5 Summary

The reported 3D simulations of realistic devices highlight that the potential fluctuations (and corresponding percolation paths) associated with random discrete dopants, substantially enhance the current changes and threshold voltage shifts resulting from the profound effect of traps strategically located in regions of high local current densities. The statistical distribution in the number of trapped charge increases the large ΔV_T occurrences and the maximum magnitude ΔV_T , compared to the case when the number of trapped charge is fixed in the simulation. The accumulative trapping of electrons in nMOSFETs, as a result of progressive degradation results not only in gradual increase of the average threshold voltage but also in an increased dispersion of its distribution by 3 mV at $N_T = 1 \times 10^{12}$ cm^{-2}. For all the simulated levels of interface trapped charge densities, the resulting distribution threshold voltage shits are found to be weakly correlated with the initial, ‘fresh‘ state threshold voltages, with all of the magnitude of correlation coefficients in the order of 10^{-2}. In summary, this work has demonstrated that the dominant variability source stemming from the random discrete dopants must be accounted for to properly simulate of the effects of progressive degradation of bulk nMOSFETs.

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Chapter 6

Integrating the Effects of Trapped Charges into Compact Models

6.1 Introduction

Chapters 4 and 5 examined how random-dopants-induced intrinsic variability gives rise to a statistical distribution in the electrical parameter changes induced by interface-trapped carriers. In addition, the evolution of the distribution of these electrical parameters in 1000 nMOSFETs as a result of progressive increase in the densities of interface-trapped charges in the devices was studied. These results were generated by 3D numerical simulations with computational costs which are not tolerable in an IC design environment, which involves very large scale transistor integration and the competitive requirement to keep a minimum product development time. It is, however, critically important to understand, correctly predict and minimise the impact of BTI degradation at an early design stage to ensure circuit reliability for the desired period of time.

A number of authors have recently proposed approaches which can be used in circuit-level simulations for the purpose of predicting the circuit performance under BTI degradation. In [1], a V_T degradation model based on the reaction-diffusion framework is used in inverter circuit simulation to analyse the resulting delay degradation. Authors in [2, 3] developed a SPICE-compatible MOSFET V_T degradation model which considers technology-dependent parameters and recovery effects. In [4], an

NBTI model is proposed for a.c. circuit simulations. Even though these previous works have addressed the main concerns of BTI degradation on circuits, they are generally based on the assumption of a nominal V_T degradation when transistors of an identical design are subjected to a similar stress level. However, due to random variation of the number of traps within any given transistors, there exists statistical variation in the V_T degradation even when the devices are subjected to similar stress levels [5, 6]. This results in an *additional* V_T variation on top of the pre-degradation V_T variation caused by the intrinsic random dopants fluctuations. Neglecting this statistical aspect of BTI degradation can result in a significant error in estimating the lifetime of the circuits [7]. The more recent work of [7] proposes a model which takes into account the statistical variation of V_T degradation due to NBTI and random dopant fluctuations. However, the model requires *a priori* knowledge or assumption of the V_T variation caused by random dopants.

A compact model can provide an essential link between the computationally expensive device-level physical simulation and the high efficiency requirement of circuit-level simulations. This chapter presents a framework to integrate the statistical aspect of charge-trapping degradation, taking into account the MOSFET's random-dopants-induced intrinsic variability, into the device compact model. Based on the proposed approach, the important physical effects delivered by the 3D Glasgow 'atomistic' simulator are propagated into the compact model without making prior assumptions of the compact model parameter distributions. In Section 6.2, the compact model parameter extraction methodology employed in this work is described, and the accuracy of the compact models is evaluated in Section 6.3. In Section 6.4, a simple method to bypass the requirement for physical simulations in building statistical compact models is described. The accuracy of the compact models built by this so-called "naïve" approach is analysed, with suggestions for future improvements highlighted.

6.2 Statistical Parameter Extraction Strategy

A compact model contains a set of physical and empirical parameters which needs to be calibrated against device data obtained either from measurements or simulations. Hence, an integral component of a high quality compact model is a good parameter extraction strategy which can aptly capture the device characteristics. This work uses the industry-standard BSIM4 [8] compact model and HSPICE as the circuit simulator. By default, the BSIM4 compact model does not specifically account for random dopants and trapped charge effects. However, it is equipped with a number of parameters aimed at modelling various process conditions. It has been previously demonstrated [9] that a carefully chosen set of these parameters, in combination, is able to mimic the effects of random dopant fluctuations on the current-voltage characteristics. By extension, it should be able to capture the effects of interface-trapped charges as well, because trapped charges induce essentially similar physical effects as ionised discrete dopants on the drain current.

The compact model parameter extraction strategy adopted by this work closely follows those described with more details in [9-13]. Figure 6.1 illustrates the basic idea of the two-stage parameter extraction strategy. The method uses the I_D-V_G characteristics of the 1000 35 nm n-channel MOSFETs analysed in the previous chapters as the source data for the rest of the extraction methodology. In the first stage, a complete set of BSIM4 compact model parameters is extracted from the current-voltage characteristics of an ideal version of the 35 nm nMOSFET, that is, with continuous doping distribution and without the trapped charges. Therefore this process needs only to be done once for the entire ensemble of microscopically different transistors. The parameter extraction is carried out using Aurora [14], a general-purpose optimisation software tool for fitting SPICE compact models to the device electrical data. Aurora extracts the compact model parameters by minimising the root means square (RMS) error between the current-voltage values of the source

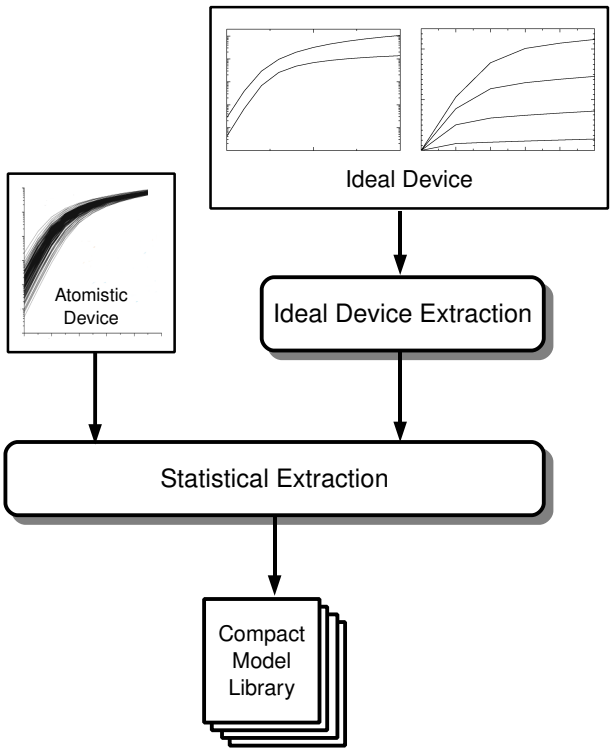


Figure 6.1: Flowchart of the two-stage compact model parameter methodology used in this work.

data and the corresponding values generated by the compact model. The extracted parameters are then grouped into two groups: those which are insensitive to random dopant fluctuations are fixed to their nominal values, while those which are sensitive are re-extracted in the second-stage of extraction.

From the point of view of MOSFET operation, random dopants and trapped charges exert three crucial effects. First, they induce significant drain current and sub-threshold slope variations in the weak inversion regime. Secondly, they cause significant spreading of the threshold voltage and finally, they introduce variations in the device drive current. On the basis of these physical effects, 6 BSIM4 compact model parameters are chosen to be re-extracted in the second-stage of parameter

extraction. The parameters are V_{TH0}, U_0, N_{factor}, V_{OFF}, R_{dsw} and D_{sub}. V_{TH0} is the basic threshold voltage parameter and it accounts for the threshold voltage variation. U_0 is the low-field mobility parameter and is chosen to account for the current variation. N_{factor} and V_{OFF} are basic sub-threshold parameters, accounting for the sub-threshold slope and leakage current variations. R_{dsw} accounts for the random dopants effects on the source/drain, while D_{sub} accounts for drain-induced barrier lowering (DIBL) variation.

By tuning these parameters to the specific I_D-V_G characteristics of each of the 'atomistic' devices, the effects of random dopants and trapped charges can be captured by the compact model. Because the values of these parameters are unique to each of the 1000 microscopically different transistors, the second-stage extraction procedure needs to be done for each devices in the entire simulation sample. This statistical parameter extraction strategy is also repeated for each levels of trapped charge

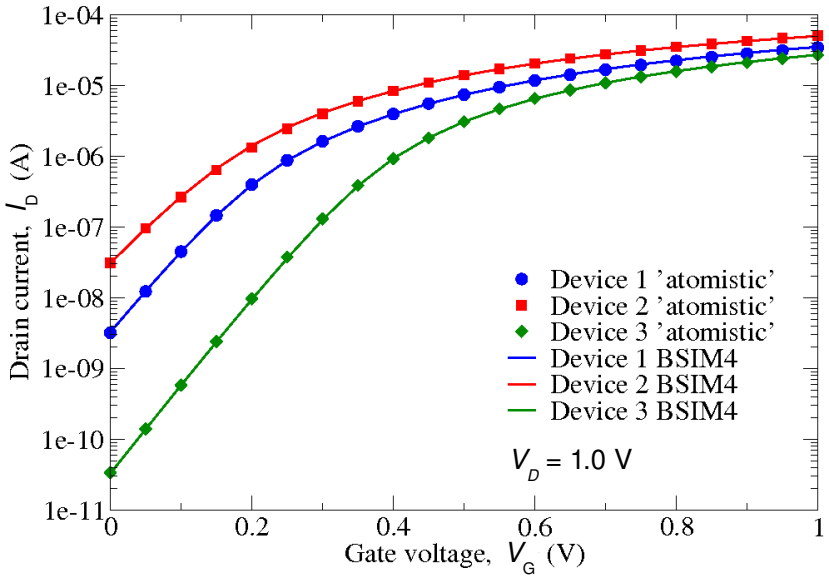


Figure 6.2: I_D-V_G characteristics of 3 microscopically different MOSFETs, obtained from HSPICE simulations utilising BSIM4 compact models containing key parameters extracted from the corresponding 3D 'atomistic' simulations.

densities simulated in Chapter 5. Figure 6.2 shows an example of the BSIM4-generated current-voltage characteristics compared against the corresponding data supplied by the Glasgow 'atomistic' simulator, for the same set of 3 microscopically different transistors. The overall good match between both data sets reflects the suitability of the extraction procedure to capture the wide variations of I_D-V_G characteristics caused by random dopants fluctuations.

6.3 Extraction Results and Evaluation of Accuracy

The accuracy of the compact models generated by the method outlined in the previous section generally depends on the choice of the statistically extracted parameters, and the size of this particular set of chosen parameters. For the purpose of assessing the fidelity of the compact models in reproducing the 'atomistic' device characteristics, 3 figures of merit have been chosen as the basis of comparison. The figures of merit are threshold voltage (V_T), leakage current (I_{off}) and on current (I_{on}). Shown in Figure 6.3 is a typical histogram of the figures of merit obtained from the 1000 simulated transistors. In general, the shape and width of the distribution of figures of merit generated by the BSIM4 statistical compact models compare well to the original corresponding distributions generated by the 3D Glasgow 'atomistic' simulator.

Figure 6.4 reports the mean and standard deviation of the figures of merit obtained from simulations of 1000 nMOSFETs subjected to increasing levels of interface-trapped charge densities. Physical device simulations by the 3D Glasgow 'atomistic' simulator indicate that the trapped charges increase the average V_T , making the MOSFETs harder to turn on. The increased level of interface-trapped charges also degrades the average drive current and lowers the average leakage current. These effects are reproduced by the HSPICE simulations utilising the BSIM4 statistically extracted compact models to a high degree of accuracy. A close agreement is also

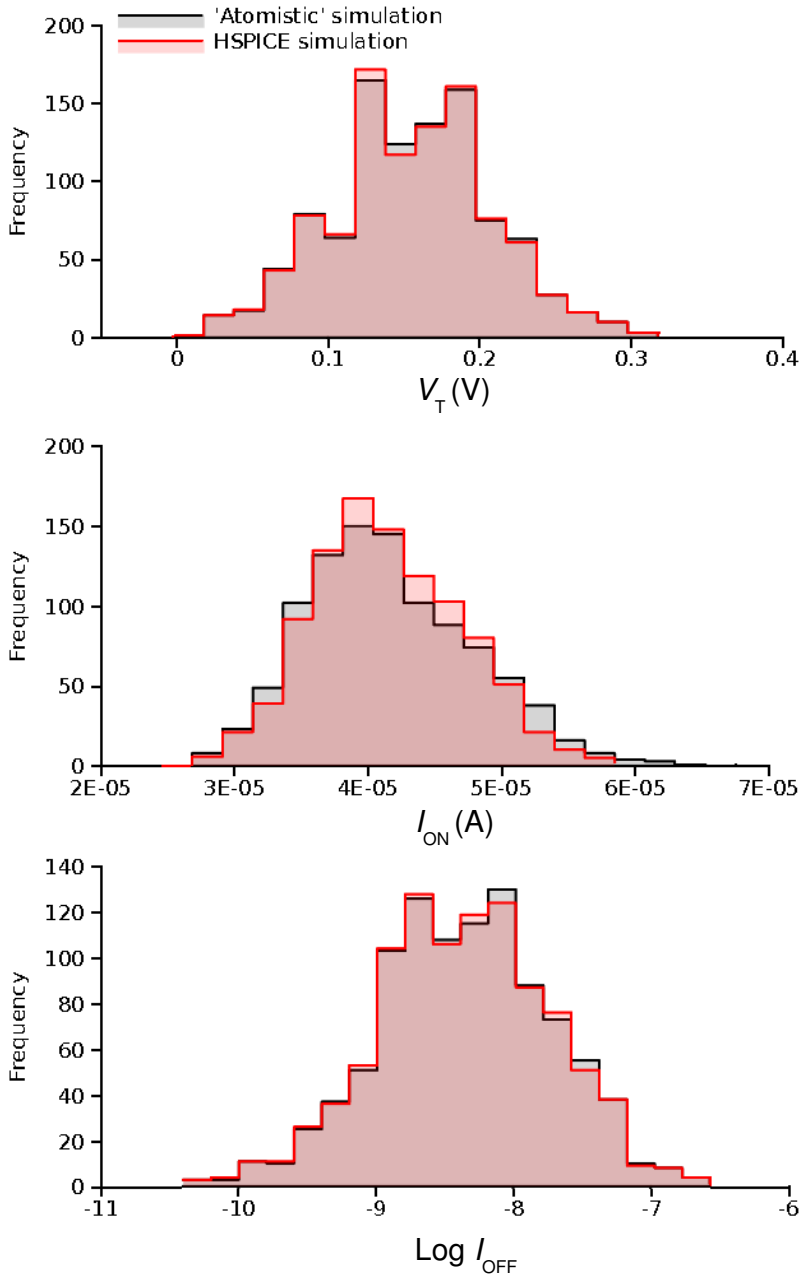


Figure 6.3: The distribution of threshold voltage, on current and leakage current obtained from HSPICE simulations of 1000 nMOSFETs compared against the corresponding distributions generated by 3D physical simulations of the same ensemble of devices. The distribution shown are for MOSFETs with interface-trapped charge density of $N_T = 2\times10^{11}$ cm^{-2}.

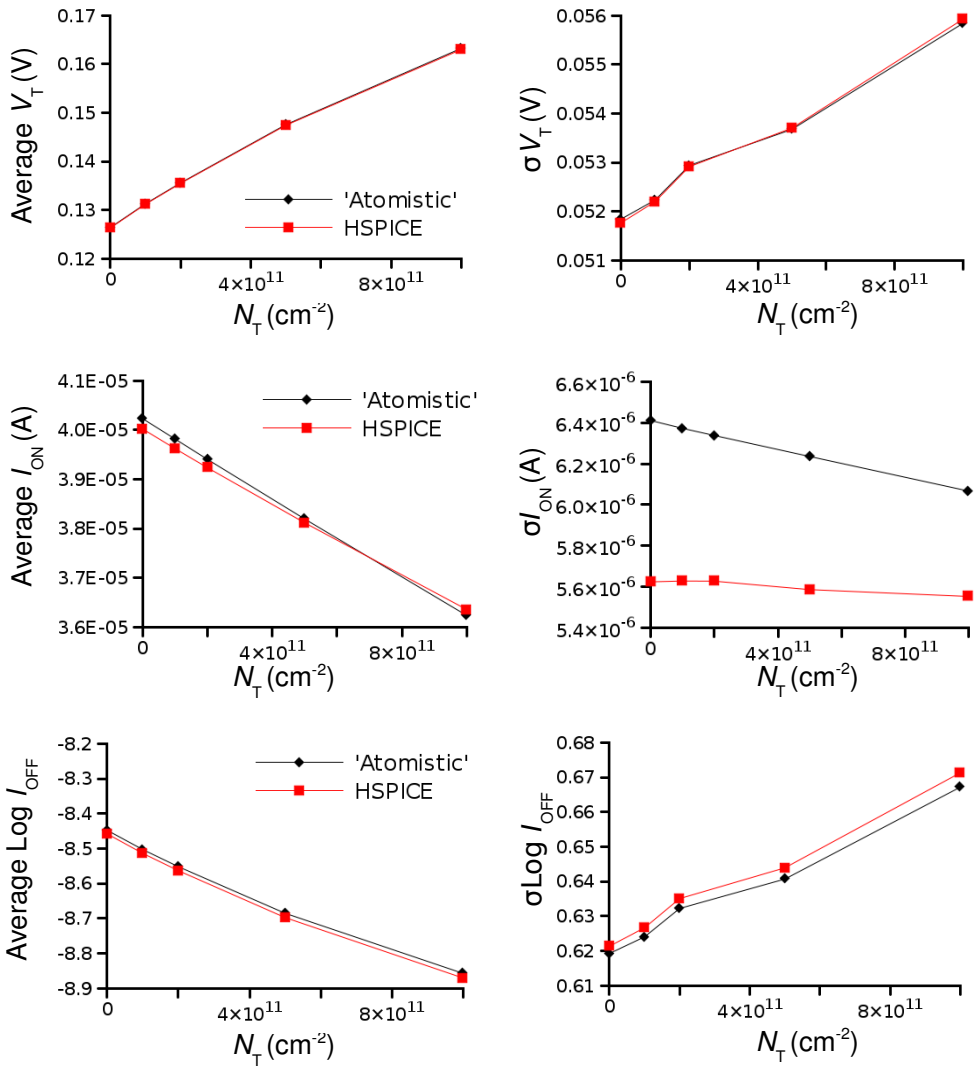


Figure 6.4: Mean and standard deviation of the figures of merit at increasing levels of interface-trapped charge densities, obtained from 'atomistic' simulations compared against the corresponding HSPICE simulations.

observed in the standard deviations of the figures of merit, particularly in the sub-threshold regime. However, the statistical compact models are found to underestimate the drive currents variability, with average percentage difference of 10.8% across the simulated N_T's. This difference seems more obvious due to the choice of non-zero'ed axes on this graph. In principle, the accuracy can be further improved by extracting a

few more parameters which are specifically sensitive to inversion variation in the devices. But in our case, this poses a trade-off consideration between keeping a minimum number of parameters with clear trends which can be extrapolated (explained in Section 6.4), or a better accuracy modelled with a bigger set of parameters but not having a clear trend across the N_T .

A high quality compact model must not only closely reproduce the figures of merit of the modelled device, but also preserve the degree of correlations between them. For example, a MOSFET which has a relatively higher threshold voltage will correspondingly have a lower leakage and drive currents. An example of these correlations is shown in Figure 6.5, plotted for both the 3D 'atomistic' simulations and HSPICE simulations. The figure visually indicates that the correlations are closely replicated by the HSPICE simulations, which are also quantitatively indicated by the good match between the correlation coefficients compared in Table 6.1. These indications validate the compact model extraction strategy in preserving the important physical effects from the 'atomistic' simulations. It is also worth mentioning that the average RMS error resulting from the statistical parameter extraction procedure was less that 2% for all the simulated levels of interface-trapped charge densities, again indicating the compact model's high fidelity in representing the 'atomistic' device current-voltage characteristics.

V_T	-0.8315	-0.9965
-0.7762	I_{on}	0.5253
-0.9961	0.5043	I_{off}

Table 6.1: Correlation coefficient between figures of merit obtained from 3D 'atomistic' simulations (*bottom left figures*) and HSPICE simulations (*top right figures*) for $N_T = 1\times10^{12}$ cm^{-2} .

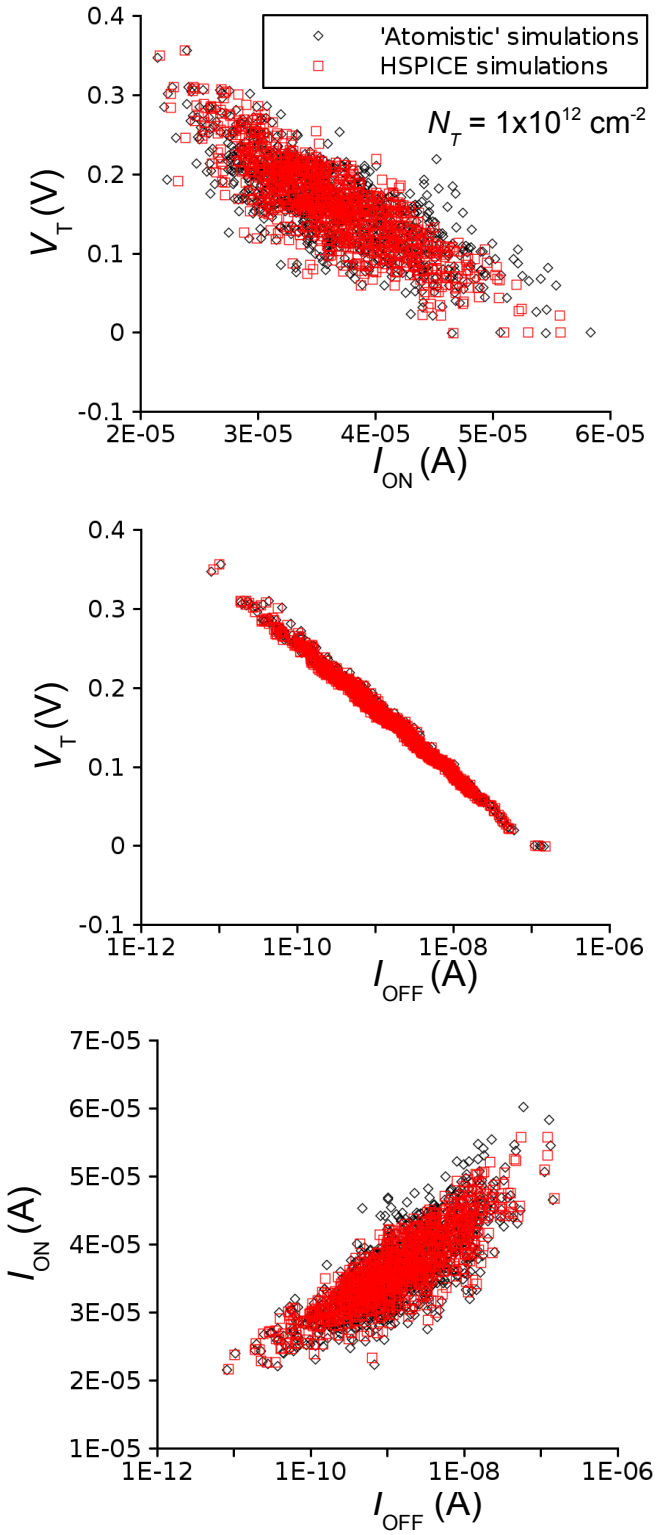
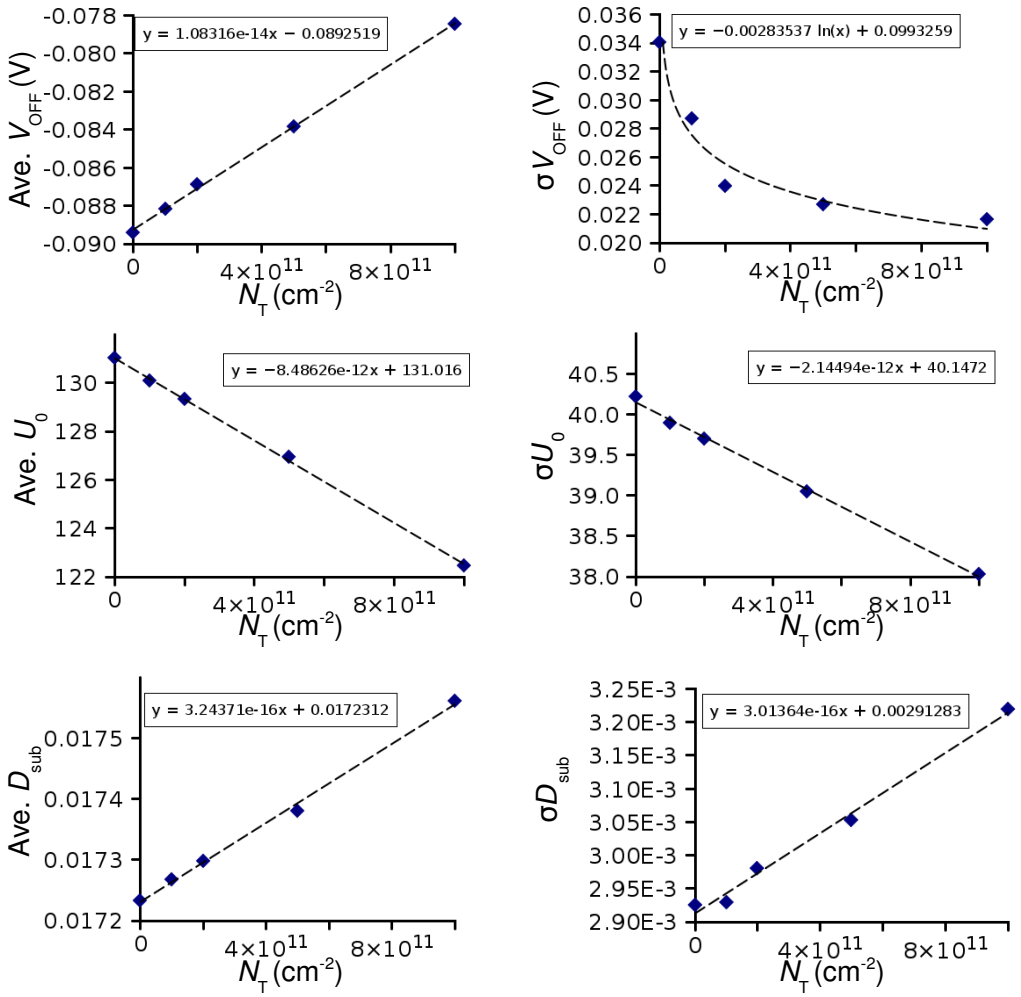


Figure 6.5: Scatter plots between figures of merit obtained from HSPICE and 3D 'atomistic' simulations of 1000 MOSFETs.

6.4 Generating Statistical Compact Model Parameters

Figure 6.6 shows the mean and standard deviation of the 6 BSIM4 compact model parameters directly extracted from the 3D 'atomistic' simulations of 1000 nMOSFETs subjected to increasing levels of interface-trapped charge densities N_T . The graphs are shown with the best possible trend line and fitting equation for the distribution of each parameter. It should be noted that these trends are unique to the specific extraction strategy outlined in Section 6.2. A different strategy involving, for instance, other parameters or a bigger set of parameters will yield a different distributions across the N_T due to the underlying correlations between the parameters.



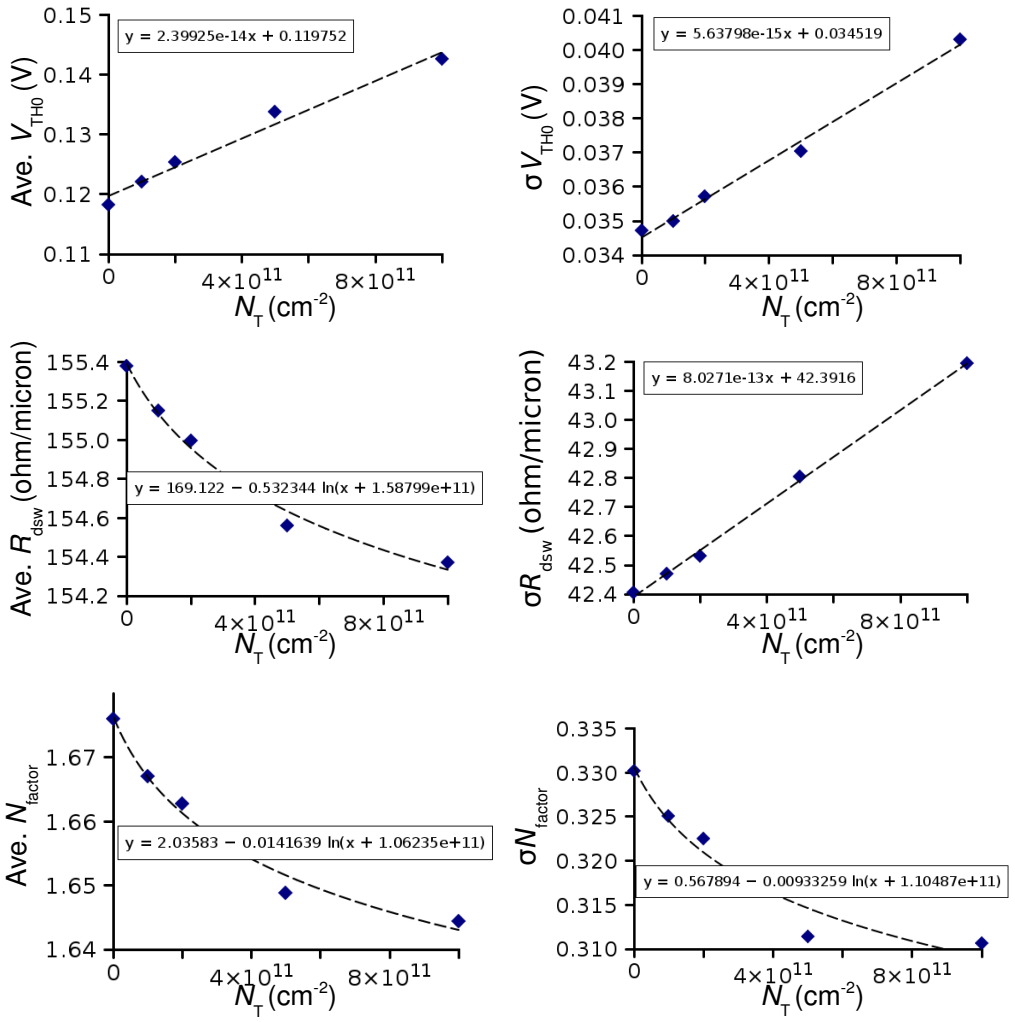


Figure 6.6: Mean and standard deviation of the 6 BSIM4 compact model parameters extracted from 1000 physically simulated MOSFETs with at various increasing levels of interface-trapped charge densities.

Even though the direct parameter extraction strategy gives a reasonably good accuracy, its application is constrained by the requirement for statistical scale physical simulations from which the compact model parameters need to be extracted. By establishing the parameter interpolations as a function of N_T, it is possible to generate statistical compact model parameters for arbitrary levels of N_T, without the need to extract them from the corresponding time-consuming 3D physical simulations. This

can be done by the so called "naïve" approach, where each parameter is assumed to follow a normal distribution, and is independently generated based on its mean and standard deviation calculated for the desired particular N_T . These artificially-generated parameters are then directly inserted into the compact models to be used in HSPICE simulations. The figures of merit obtained from HSPICE simulations utilising the statistical compact models generated by the naïve approach, are shown in Figure 6.7. For all the simulated levels of N_T , the naïve approach closely reproduces the average V_T , I_{off} and I_{on} generated by the 3D 'atomistic' simulations. However,

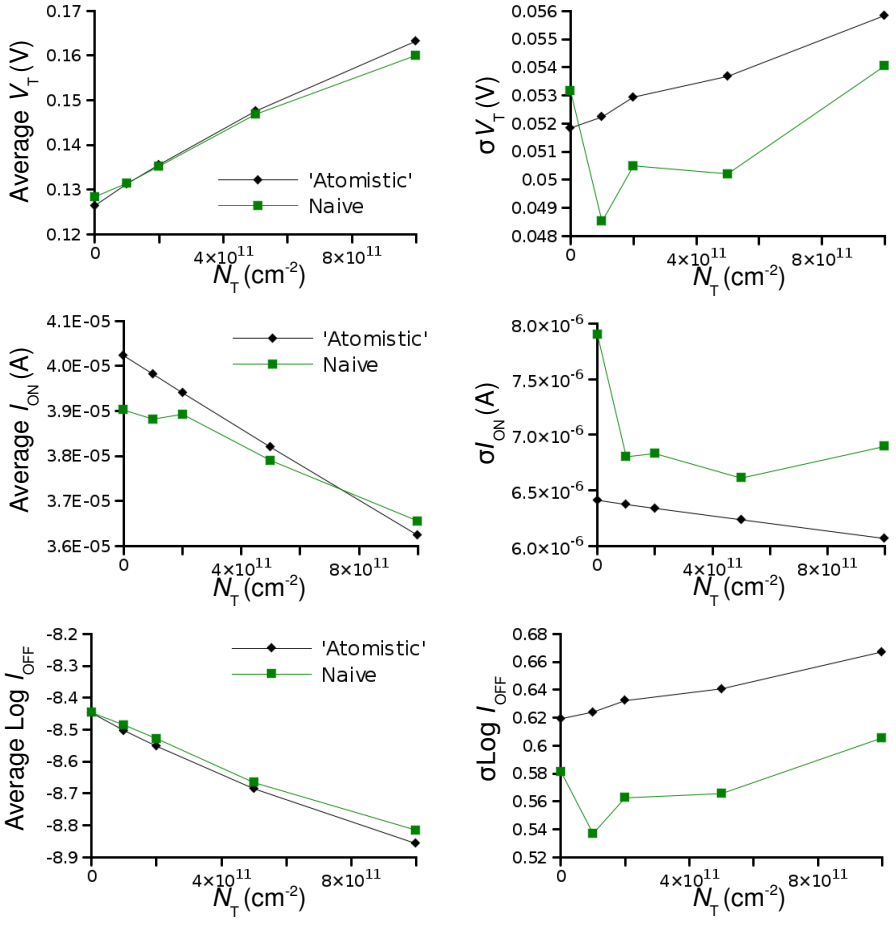


Figure 6.7: Mean and standard deviation of the figures of merit at increasing levels of interface-trapped charge densities obtained from 'atomistic' simulations and naïve approach.

there are marked differences in the standard deviations of the figures of merit generated by the naïve approach. This is also evident in Figure 6.8 showing the correlations between the figures of merit. Even though the naïve approach of statistical compact model parameter generation generally results in wider variability, the overall physical correlation between the figures of merit remain largely intact.

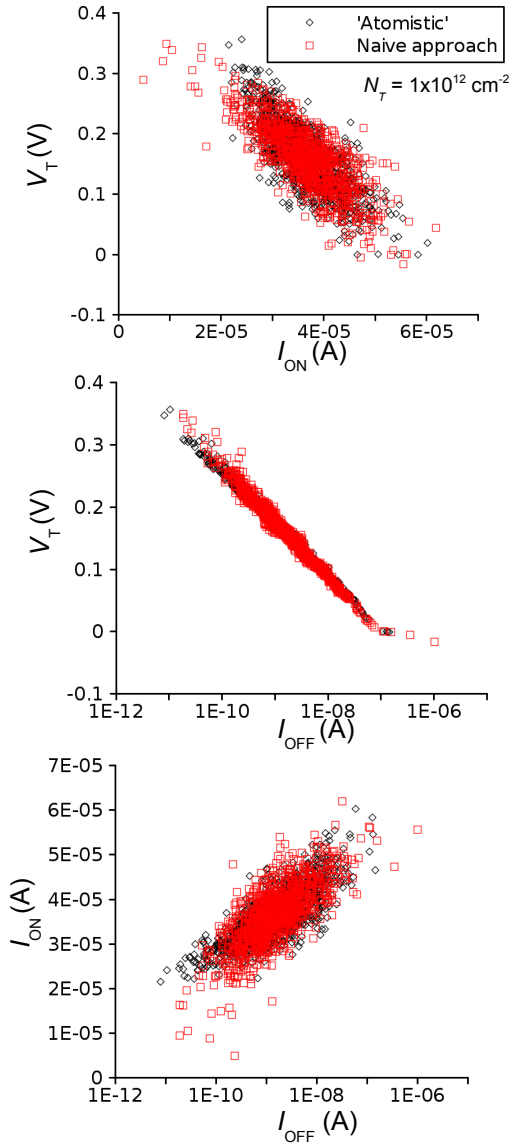


Figure 6.8: Scatter plots between figures of merit obtained from naïve approach of statistical compact model parameter generation, and 3D 'atomistic' simulations of 1000 MOSFETs.

V_T	-0.7828	-0.9885
-0.7762	I_{on}	0.2170
-0.9961	0.5043	I_{off}

Table 6.2: Correlation coefficient between figures of merit obtained from 3D 'atomistic' simulations (*bottom left figures*) and naïve approach (*top right figures*) for $N_T = 1\times10^{12}$ cm^{-2}.

The naïve approach compares less favourably, in terms of accuracy, with the statistical compact models directly extracted from the 3D physical simulations. This inherent shortcoming of the naïve approach stems from the fact that it assumes the 6 compact model parameters follow a normal independent distribution. This is not the case, as shown in Figures 6.9 and 6.10 displaying an example of distribution and correlation between the 6 compact model parameters directly extracted from the 3D 'atomistic' simulations. The parameter distributions are not strictly normal, and furthermore some of them exhibit relatively strong correlations with one another. By independently generating these parameters, the naïve approach effectively destroys the correlations between the parameters, which are then reflected in the distorted physical correlations between the figures of merit.

Statistical parameter generation based on Principal Component Analysis (PCA), which takes into account the correlations between the compact model parameters, results in better-reproduced physical correlations between the electrical figures of merit [15]. However, PCA approach still falls short in preserving the tails of the distribution of the figures of merit, because it assumes normal distribution of the compact model parameters [15, 16]. The most recent and novel workaround for this issue is the use of statistical Nonlinear Power Method (NPM), which takes into account both the non-normality and correlations between parameters. This methodical

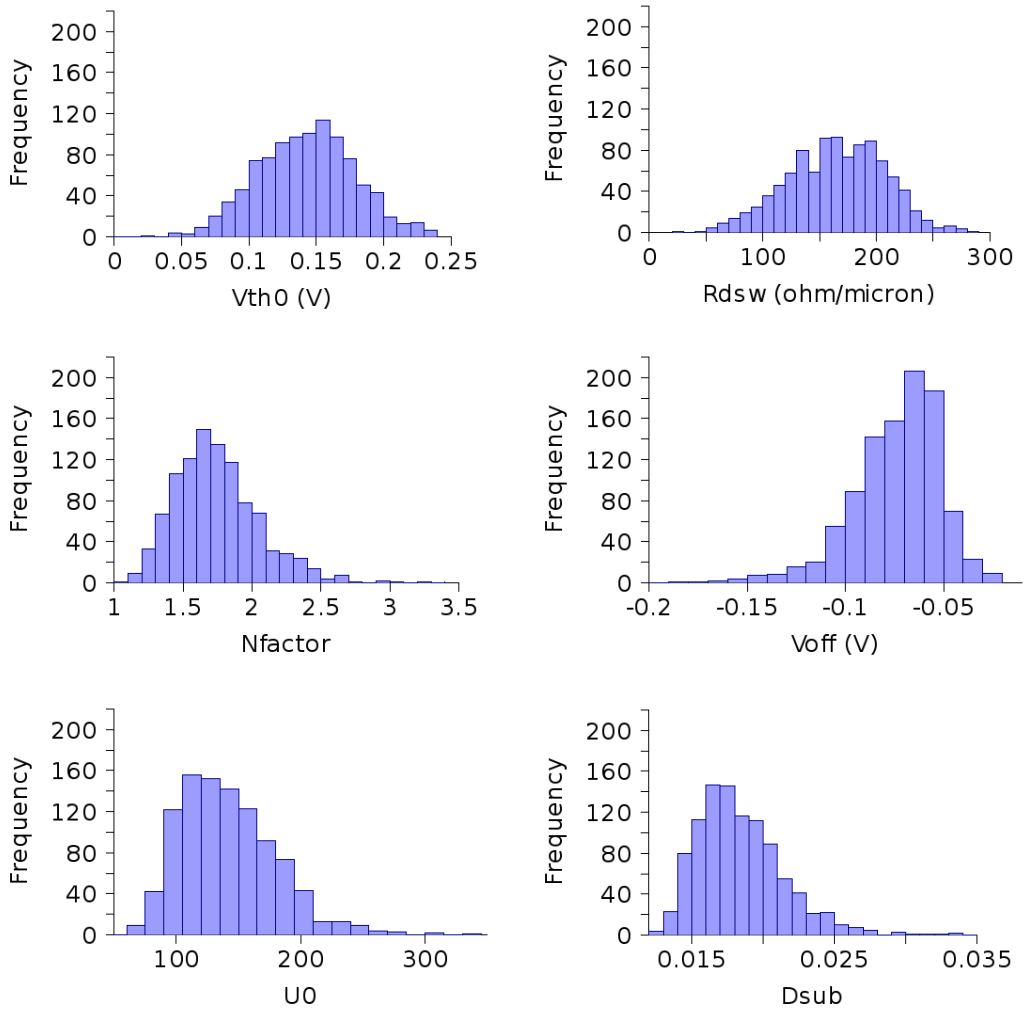


Figure 6.9: Distribution of compact model parameters directly extracted from the 3D 'atomistic' simulations of 1000 microscopically different transistors subjected to N_T = 5×10^{11} cm^{-2}.

improvement of statistical compact model parameter generation results in an improved accuracy, which can be seen even in the tails of the distribution of the figures of merit [16]. NPM is a promising step forward towards the development of a general statistical compact modelling approach. However, the implementation of NPM is beyond the scope of this work.

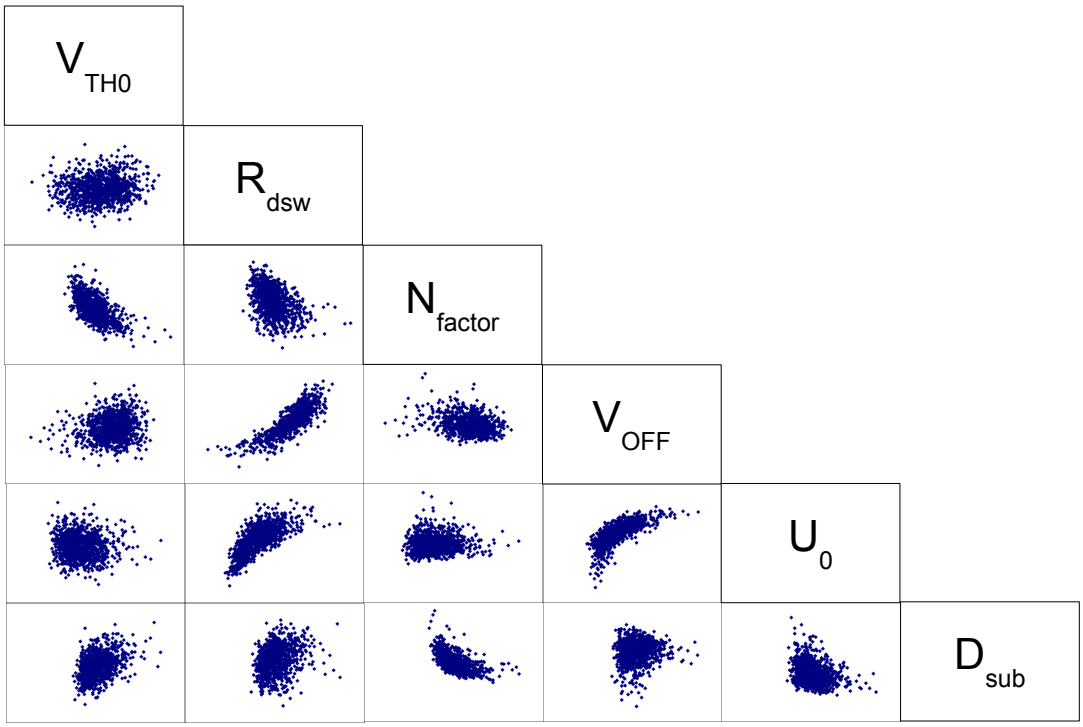


Figure 6.10: Scatter plots illustrating the correlations between the compact model parameters directly extracted from the 3D 'atomistic' simulations of 1000 microscopically different transistors subjected to $N_T = 5\times10^{11}$ cm^{-2}.

The purpose of this work is to capture the device *IV* characteristics from the 3D 'atomistic' simulations under the onslaught of progressive PBTI degradation in the intrinsic presence of random-dopants-induced variability. We have proposed a statistical compact modelling approach and demonstrated its reasonable accuracy by comparing the electrical parameters generated by the compact models against the corresponding values computed by the computationally-expensive 3D physical simulations for the same ensemble of devices. We do not have at our leisure, other device datasets nor experimental measurements for the purpose of validating this approach against other device type or against experimental measurements. Admittedly, statistical compact modelling is an early technology as well as a vibrant field of

research. It presents a complex problem with no ready solution because compact models do not have natural parameters to capture the statistical aspects of BTI degradation. With the aim to capture BTI effects in the intrinsic presence of statistical variability, we have evaluated particular choice of the available compact model parameter sets with physical associations with BTI, which can best reproduce the main features of the degradation. Therefore our main contribution is demonstrating a feasible method by which the statistical aspects of BTI degradation can be captured in statistical compact models. This would be useful for circuit designers to check the extent of which their design will work under progressive BTI degradation, while simultaneously being aware of the required design margin imposed by the device statistical variability.

In a recent study published in the IEEE Electron Device Letters [17], the same

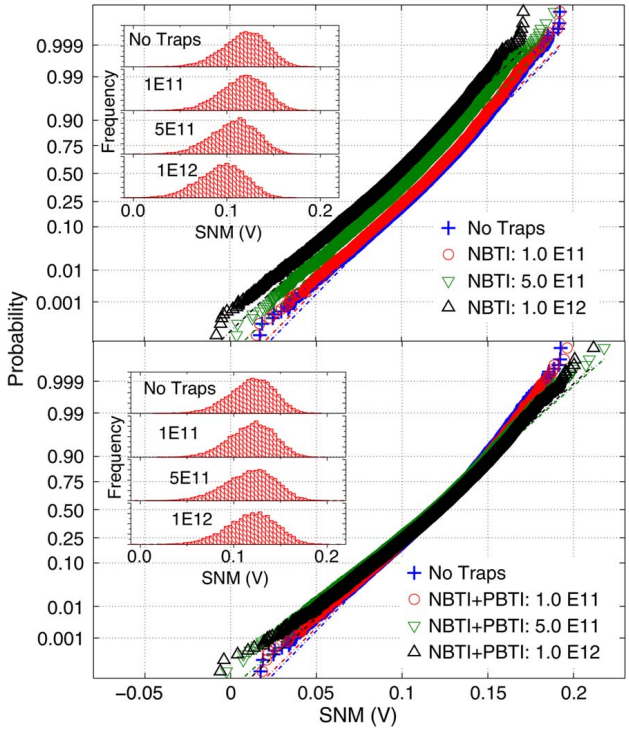


Figure 6.11: Probability plot of SNM for SRAM at different degradation stages of NBTI only and NBTI + PBTI. Inset: Corresponding distributions of SNM. After [17].

approach for integrating BTI effects in compact models developed in this work has been applied for investigating the impact of NBTI/PBTI on the stability Static Random-Access Memory (SRAM). Similar to this work, the afore-mentioned study initially takes snapshots of the NBTI/PBTI degradation at different levels of trapped charge densities, and then transfers the device characteristics to BSIM4 compact models via the 2-stage compact model extraction adopted in this work. The resulting compact model library is then used in SRAM circuits simulation, where a degradation of the Signal-to-Noise Margin (SNM) is found, as shown in Figure 6.11. The study demonstrates the immediate practical use of the approach developed in this work, while the publication of the study in a well-ranked, peer-reviewed journal indicates that the methodology is well-accepted.

6.5 Statistical Circuit Simulation: Impact of Progressive PBTI in the Presence of Random-Dopants-Induced Variability

In this section, we demonstrate the application of the extracted compact models in investigating the impact of PBTI on inverter circuits. A CMOS inverter logic circuit as shown in Figure 6.12(a) consists of a pair of n- and p-channel MOSFETs. Because we only have compact models extracted of n-channel MOSFETs, the resulting circuit degradation in our simulations is only the result of PBTI in the nMOSFET, while the pMOSFET based on a model card extracted from a uniform device is assumed to be undegraded and identical across the ensemble of simulated circuits. Figure 6.12(b)-6.12(d) shows the transfer characteristics of 1000 inverters obtained from the statistical HSPICE simulations using the 1000 microscopically different n-channel MOSFETs, at three different levels of trapped charge densities and supply voltage V_{DD} of 1.0 V.

It can be seen from Figure 6.12(b) that even during the “fresh” condition when the

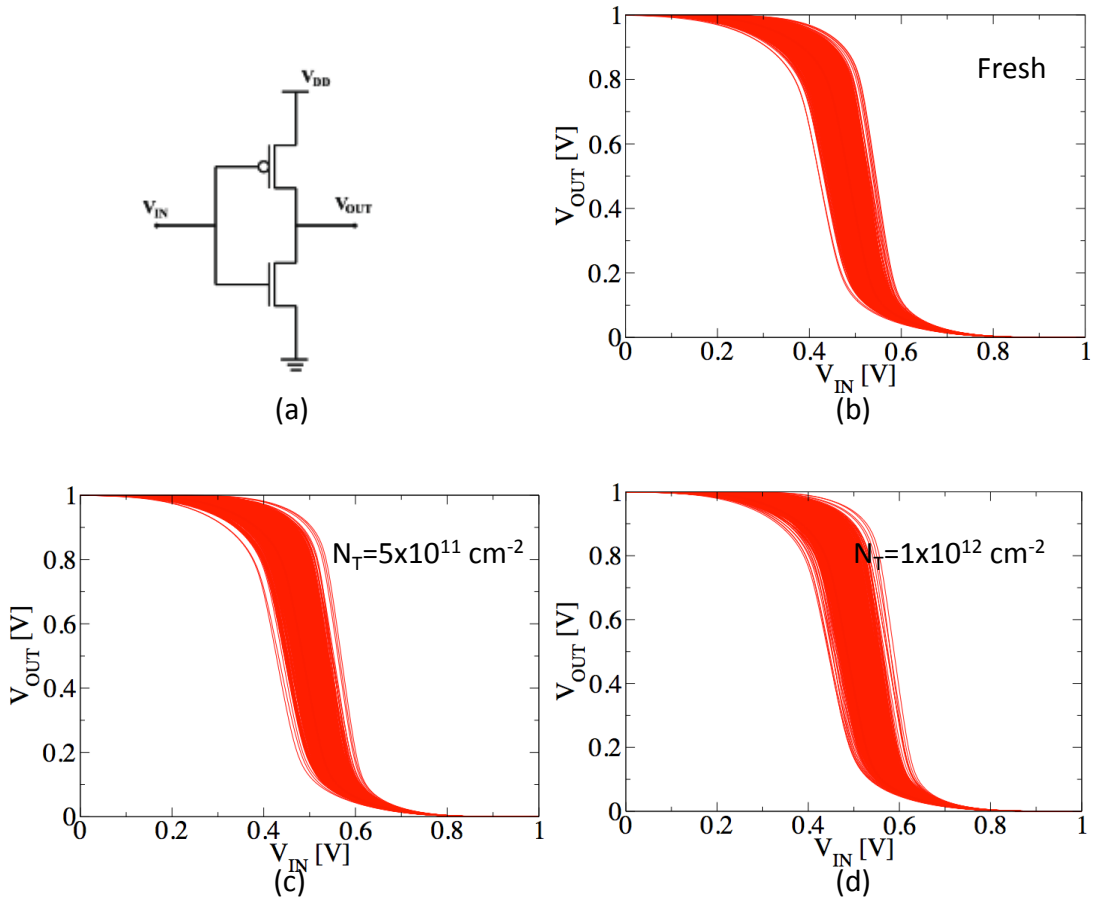


Figure 6.12: (a) Circuit schematic of a CMOS logic inverter. Transfer characteristics of 1000 inverters at (b) with no trapped charges, (c) with trapped charge density N_T=5x10^{11} cm^{-2}, (d) with trapped charge density N_T=1x10^{12} cm^{-2}.

nMOSFETS are not yet degraded (no trapped charge), the transfer curves are already widely distributed due to the threshold voltage variability caused by random discrete dopants. As the level of trapped charge density increases, there is a small but noticeable horizontal shift as well as a wider distribution of the transfer curves. This is confirmed by analysing the distribution of the flip voltages of the inverters. The flip voltage V_{fp} is defined as the value of input voltage V_{IN} at which the output voltage V_{OUT} is equal to one-half of the supply voltage, V_{OUT} =V_{DD} /2. For an ideal, well-balanced inverter, V_{fp} is equal to the V_{OUT}. However, due to the initial random-

Flip voltage, V_{fp}	Fresh	N_T=5x10^{11} cm^{-2}	N_T=1x10^{12} cm^{-2}
Average (V)	0.484	0.499	0.512
Std. dev. (V)	0.020	0.021	0.022

Table 6.3: Average and standard deviation of flip voltages of 1000 inverters at three different levels of trapped charge densities

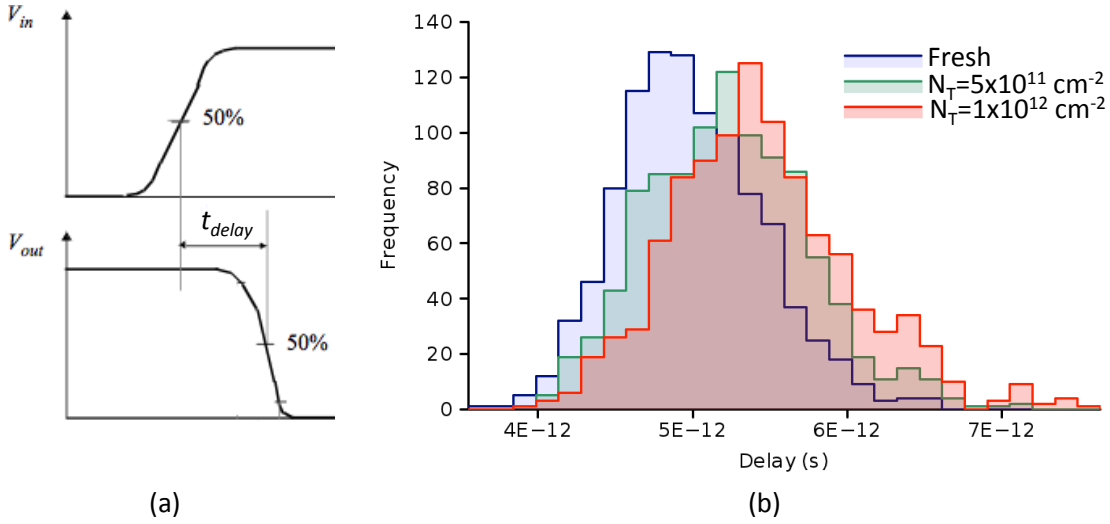


Figure 6.13: (a) Inverter circuit delay definition. (b) Distribution of delay of 1000 inverters at three different levels of trapped charge densities.

dopants-induced threshold voltage variability, the V_{fp} is widely varied across the ensemble of 1000 simulated inverters even when the devices are not yet degraded. The subsequent progressive PBTI degradation further degrades the V_{fp} by increasing both the mean and variation of V_{fp} of the circuits, as summarised in Table 6.3.

The impact of PBTI on the circuits can also be assessed by its effects on the delays of the circuits. The CMOS inverter delay, t_{delay} , is defined as the time taken for its

inverted output to reach 50% of the output voltage, measured from the time its input reaches 50% of the input voltage, as schematically shown in Figure 6.13(a). In Figure 6.13(b) and Table 6.4, the distribution of the delays for the 1000 simulated inverters at the three different levels of trapped charge densities are shown. It is clear from Figure 6.13(b) that PBTI degrades the circuit performance by increasing the average delay (hence slowing down circuit switching speed), and widens the initial distribution of the intrinsic delay due to the random-dopants-induced threshold voltage variability. It can be reasonably expected that if the NBTI degradation of the pMOSFETs are taken into account in addition of the PBTI of the nMOSFETs, the resulting delay degradation will be more severe due to the increased mismatch between the transistor pairs as the both degradation processes grow progressively worse.

Delay, t_{delay}	Fresh	N_T=5x10^{11} cm^{-2}	N_T=1x10^{12} cm^{-2}
Average (s)	4.84x10^{-12}	5.08x10^{-12}	5.30x10^{-12}
Std. dev. (s)	4.64x10^{-13}	5.24x10^{-13}	5.83x10^{-13}

Table 6.4: Average and standard deviation of delays of 1000 inverters at three different levels of trapped charge densities

6.6 Summary

A method to integrate the effects of interface-trapped charges in MOSFET compact models has been presented. The method is based on an existing framework which was previously designed to capture and study the impact of MOSFET intrinsic variability on circuit performance. The procedures enable the statistical aspects of BTI degradation, arising from random configurations of traps and discrete dopants in the devices, to be considered in circuits simulations. Through a careful selection of

relevant parameters, the compact models built by direct parameter extraction provide a high degree of reproducibility (average RMS error of < 2%) of the electrical characteristics of the physically simulated devices. By interpolating the distributions of the extracted parameters, compact model libraries can be built for arbitrary levels of stress without the need to extract them from the corresponding physical simulations. However, the simplest approach for doing this results in degraded accuracy as it neglects the non-normality of, and correlations between, the parameters.

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Chapter 7

Conclusion

The aim of this work was to investigate the impact of interface-trapped charges in conventional bulk MOSFETs. The underlying motivation stems from the fact that charge-trapping-related degradations in present nano-scale bulk MOSFETs cause dramatic changes in their electrical characteristics, threatening circuit functionality and reliability. This ageing phenomena occurs in the simultaneous presence of various intrinsic sources of variability, with the dominant source being random dopant fluctuations. Device-to-device variation in the number and spatial arrangement of dopant atoms gives rise to performance variations across the ensemble. Consequently, the application of a given stress on these small transistors results in a statistical distribution of parameter changes instead of the identical responses otherwise expected, and seen in larger devices.

The simulation methodology chosen for this work was described in Chapter 3. The chapter also discussed other established modern semiconductor device simulation techniques available in the Device Modelling Group, namely quantum mechanical approaches, the Monte Carlo method, drift-diffusion (DD) based simulation and compact models. Through a careful review of the relative advantages and drawbacks associated with each of these methods, the DD approximation with density-gradient quantum corrections was chosen, as it offers the optimal balance between computational cost and accuracy, enabling large scale statistical simulations along with a physically consistent treatment of the discrete dopants and trapped charges in the simulated device. The testbed device simulated in this work was based on a real 35 nm gate length n-channel bulk MOSFET developed by Toshiba, allowing realistic

assessment of the impact of trapped charges, after simulator calibration.

Chapter 4 discussed the results obtained from simulations of 1000 MOSFETs subjected to a single interface-trapped charge. Initially, through a series of systematic simulations of single charge-trapping in an ideal continuously doped transistor, the generic dependencies of the magnitude of the resulting drain current change were identified. One of the key observations was that the drain current is most profoundly affected when the trap is located near the middle of the channel and throughout its width, at the point of the peak of the potential barrier separating the source and drain. However, this was found not to be the case when random dopants were introduced into the simulations, where large responses could occur at random locations of the trap anywhere in the channel-interface plane. By implication, two devices with different microscopic doping configurations would also respond differently to a given identical spatial location of a trapped charge. This consequently necessitates statistical scale simulations in order to characterise the effects of trapped charges in an ensemble of microscopically different transistors.

The statistical simulations revealed relatively rare occurrences of large ΔV_T, with magnitudes exceeding 3 times than that predicted by conventional theoretical approaches. Larger shifts can be expected at lower probability levels if the sample size is increased. These anomalously large changes are attributed to unlucky charge-trapping along narrow current percolation paths shaped by the electrostatic potential of the random discrete dopants. These paths have a higher local electron concentration than the surrounding portions of the channel. Consequently charge-trapping along these critical paths which connect the source and drain results in large current changes. The simulations with and without taking into account random dopant fluctuations give two distinctly different distributions of current changes, but only the one accounting for random dopants qualitatively reproduces the experimentally measured RTS amplitude distributions. These results confirm that random dopant

fluctuations are responsible for the wide statistical spread and anomalously large RTS amplitudes reported in the literature.

Chapter 5 analysed the impact of progressively increasing trapped charge densities on MOSFET threshold voltage. 4 successively increased levels of interface-trapped charge densities N_T were simulated, emulating the characteristic condition of prolonged BTI degradation. Unlike in Chapter 4 where the number of traps in the simulation ensemble was fixed (a single trap in *every* device), in Chapter 5 the number of traps was statistically varied based on a Poisson distribution with a given average value, thus replicating the realistic condition found in real transistors. Compared to Chapter 4 results, the ensemble of MOSFETs having *on average of* 1 trap results in larger maximum ΔV_T (due to multiple charge-trapping) and higher occurrences at the low-end ΔV_T distribution tail (by devices in the ensemble not having any trap at all).

The simulated increase in N_T gave rise to the increase in both the average and standard deviation of both the V_T and ΔV_T . The bulk of the V_T distribution was roughly Gaussian for all the simulated trapped charge densities, however the ΔV_T distribution evolved from a single-sided distribution to a Gaussian-like distribution with increasing N_T. In both cases, the normal approximation underestimates the probabilities of large V_T and ΔV_T . These results are in qualitative agreement with with experimentally observed statistical V_T degradation due to BTI stresses. Further analysis revealed that this agreement could only be attained if random dopant fluctuations are accounted for in the simulations, indicating the role of statistical interplay between the trapped charges and the underlying random dopants responsible for the observed distributions of parameter shifts. Weak correlations in the order of 10^{-2} were found between the pre-degradation V_T and post-degradation ΔV_T distributions.

Chapter 6 presented a framework to propagate the results generated by these device-

level physical simulations to circuit-level simulations using BSIM4 compact models. Based on the physical effects of the trapped charge and random dopants, 6 compact model parameters were selected for extraction. The full I_D-V_G data generated by the 'atomistic' simulator served as the source data for extraction. The extraction methodology yielded an average RMS error of less than 2%, indicating the high fidelity of the compact models in reproducing the electrical characteristics of the physically simulated devices. Analysis of the correlations between selected figures of merit (V_T, I_{on}, I_{off}) generated by the compact models compared against the original data by the 'atomistic' simulations also showed a high degree of reproducibility. A major drawback of the proposed framework is the requirement to run large scale statistical physical simulations, from which the compact model parameters need to be extracted. A simple approach to bypass this requirement, by statistically generating the compact model parameters, yielded in a degraded accuracy because it neglected the correlations between the parameters.

7.1 Future Work and Outlook

There are several aspects of the work presented here which can be extended. Other sources of intrinsic variability such as gate line edge roughness and metal gate granularity can be included in the simulations, enabling comparative analysis on the relative impact of each sources.

The simulations carried out in this work were primarily focused on the sub-threshold regime and at low drain voltage, where the device behaviour is pre-dominantly governed by electrostatics. It would also be useful to study the impact of trapped charges at drive gate bias and high drain voltage. However, at such bias conditions the transport effects related to Coulomb scattering by the trapped charges and discrete dopants exert more significant impact on the current, whereas the DD approximation which can only account for electrostatic effects would underestimate the resulting

parameter shifts. A physically inclusive way of assessing the impact of trapped charges on the drive current is by Monte Carlo simulation, or to have the DD simulation calibrated to a corresponding Monte Carlo simulation at the appropriate bias conditions, to aptly capture both the transport and electrostatic effects of the trapped charge and discrete dopants.

In 2011, Intel Corporation introduced a tri-gate transistor design on its 22 nm logic technology, citing among other things, improved switching characteristics, higher drive current and >50% power reduction. As of May 2011, Intel plans to incorporate the tri-gate transistors in its yet-to-be-released new line of processors codenamed as Ivy Bridge. A natural development path for the Glasgow 'atomistic' simulator in order to stay industrially-relevant is to have multi-gate transistor designs in its library of testbed devices, enabling studies on the statistical reliability of such new device architectures. For circuit-level study, the immediate application of the compact models extracted in Chapter 6 is in the investigation of the impact of BTI degradation on the performance of various circuit designs.

As transistor densities continue to scale exponentially, a naive analysis of the associated parameter variations will be too optimistic. The problem of statistical reliability and its effect on system lifetime will become a critical one for the semiconductor industry, which should be considered at a number of levels. At the systems level, research on fault tolerance and sub-system redundancy providing a reliability safeguard are needed more than ever, particularly for applications where human lives are critically concerned. At the same time, research on devices which are locally more resistant to such charge-trapping events (for instance, undoped channel devices) is required, even if those devices are no faster than previous generations, simply in order to keep transistor density scaling on track — and thus improving functionality per area square of silicon die, which is the core industry driver.