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Gated Lateral Silicon p-i-n Junction Photodiodes

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Declaration of Authorship

I, Kamran Abid, declare that this thesis titled “Surface Gated Lateral p-i-n Junction Photodiode” and the contributions presented in it are my own. I confirm that:

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In the name of Allah, the most Merciful, the most Beneficent.

Faith is, not believing that GOD can, it is knowing, that GOD will.

Abstract

Research in silicon photonics has recently seen a significant push to develop complete silicon-based optical components for optical communications. Silicon has shown its potential to overcome the bandwidth limitations of microprocessor interconnect, whereas, the silicon platform has already displayed the benefits of low manufacturing costs and CMOS compatibility. The work on "gated lateral silicon p-i-n junction photodiodes" has demonstrated the silicon potential, to detect optical radiations, compatibility to standard CMOS process flow and tuneable spectral response. The lateral structure of gated p-i-n junction photodiodes contributes to high responsivity to short wavelength radiations in these single and dual gate devices.

The final objective of this work was to develop high responsivity, CMOS-compatible silicon photodiodes, where the spectral response can be modulated. The lateral p-i-n junction architecture led to high responsivity values, whereas, the MOS gate structure became the basis for tuneable spectral response. The MOS gate structure, made the devices appear as a transistor to the surrounding circuitry and the gate structure in dual gate devices can be used to modulate the spectral response of the device. Single gate devices showed higher responsivity values and comparatively high blue and ultraviolet (UV) response as compared to conventional photodiodes. Surface depletion region in these devices is utilized by placing a MOS gate structure and by patterning an integrated metal grating to detect polarized light.

Single and dual gate devices with two variations were fabricated to characterise the device response. Novel lateral architecture of p-i-n junction photodiodes provides a surface depletion region. It is generally anticipated that photodetectors with surface depletion region might produce higher noise. In these devices the surface depletion region has a lateral continuation of gate dielectric which acts as a passivation layer and thus considerably reduced the noise. Physical device modelling studies were performed to verify the experimentally obtained results, which are provided in the relevant measurement chapters. In these devices the speed of operation is a compromise over the high responsivity, CMOS compatibility and tuneable spectral response.

List of Publications

From this research work

Published Papers

1. Kamran Abid, and Faiz Rahman, *Gated Lateral p-i-n Junction Device for Light Sensing.* **P**hotonics **T**echnology **L**etters, IEEE. **23**(13): p. 911-913. ***[Journal Paper]***
2. Kamran Abid, and Faiz Rahman, *High spectral responsivity gated silicon photodiodes*. **U**K Semiconductors 2011, University of Sheffield, UK. p. 117. ***[Conference Paper]***

Submitted Papers (Under review)

3. Kamran Abid and Faiz Rahman, *High Responsivity Gated Silicon p-i-n Photodiode with Enhanced Blue and Ultraviolet Response*. **Submitted to** Applied Physics-B. **{Under Review}**
4. Kamran Abid and Faiz Rahman, *Gated Silicon p-i-n Photodiode with Enhanced Blue and Ultraviolet Response*. **Submitted to** Sensors and Actuators. **{Under Review}**
5. Kamran Abid and Faiz Rahman, *Optical polarization detection by a lateral p-i-n photodiode with integrated metal grating*. **Submitted to** Applied physics B.
6. Kamran Abid, Faiz Rahman, Chris Park, Xingsheng Wang, *Gate bias-induced modulation of spectral responsivity in lateral p-i-n photodiodes*. **Submitted to** Applied Physics Letters.

Other Publications

7. Chee Heng Teo, Nireeksha S. Karode, Kamran Abid, Faiz Rahman, *Interfacial behaviour of polyaniline as an organic electronic material*. Journal of physics and chemistry of solids. **72** (2011) page 886–890. ***[Journal Paper]***
8. Faiz Rahman, Kamran Abid, Schmidt, C., Pfaff, G. and Koenig, , *Interference pigment coated solar cells for use in high radiant flux environments*, in *International Conference on Green Energy and Sustainability 2009*. 2009: Amman, Jordan. ***[Conference Paper]***

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Symbol Table

Symbol	Description	Symbol	Description
I_{ph}	Photo current	P_o or P	Incident Optical Power
e or q	Electron Charge	λ	Wavelength
h	Plank's Constant	$\mathcal{R}$	Reflectivity
c	Speed of Light	$d,\ L\ or\ l$	Height or distance or Length
α_o	Absorption Coefficient	E_g	Band-gap
T	Temperature	λ_c	Cut-off Wavelength
η	Quantum Efficiency	ν	Frequency of the light wave
T_{op}	Percentage Optical Power	F_{EHP}	Optically Generated - Electron –hole pairs
SR	Spectral Responsivity	n	n-type Silicon Material
p	p-type Silicon Material	φ	No. of Photons arriving per second
$W\ or\ \omega$	Width	τ	Mean Life Time
n_i	Intrinsic Carrier Concentration	E_F	Fermi Energy
E_i	Intrinsic Fermi Energy	N_D	Donor Concentration
N_A	Acceptor Concentration	V_o	Built in Potential
ε_{si}	Dielectric constant of silicon	V_f	Forward Voltage Applied
V_r	Reverse Voltage Applied	l_p	Width of the depletion region in p type Silicon
l_n	Width of the depletion region in n type Silicon	ε_0	Permittivity of the free space
τ_{PIN}	Temporal response pin diode	τ_{rec}	Recombination time
J_n	Current density of electrons	J_p	Current density of holes
Ψ	Built-in Potential	p^+	Heavily p-doped substrate
n^+	Heavily n-doped substrate	π	Lightly p-doped silicon (near intrinsic)

Symbol	Description	Symbol	Description
I_{DS}	Drain to source current	C_{OX}	Oxide Capacitance
V_G	Gate bias	μ_P	Mobility of holes
V_{DS}	Drain to source Voltage	μ_n	Mobility of electrons
V_{GD}	Voltage applied on Drain side gate	V_{GS}	Voltage applied on source side gate
$I_{DS(blue)}$	Drain to source current with blue light incident on the device	$I_{DS(red)}$	Drain to source current with red light incident on the device
ϕ_y	Magnitude of the electric field vector in y direction	ϕ_x	Magnitude of the electric field vector in x direction
α	Ionization coefficient of electrons	β	Ionization coefficient of Holes
M	Multiplication Factor for APD	I	Total output current

TO THE LAST MESSANGER OF GOD

HAZRAT MUHAMMAD (P.B.U.H)

Chapter 1

Introduction

1. Existing Scenario

In 1963 Frank Wanlass at 'Fairchild Semiconductor' invented CMOS circuits, although commercial CMOS integrated circuits were first fabricated only in 1969. In the early days, the CMOS devices were slow, and were mainly used in applications that required low power consumption. Over the following decades, with further improvements, CMOS technology became the almost universal choice for integrated circuits. Besides low power consumption, CMOS processing allows the integration of dense circuits. In late 1990's, CMOS-compatible processes to fabricate photodetectors opened up their use in a variety of further applications like, motion detection, [1, 2] solid state imaging cameras [3] and whole-cell biosensors [4]. CMOS-compatible, photodetectors have monolithically integrated digital and analog signal processing circuits on the same substrate. Until early this century, CMOS-compatible photodetectors were mainly investigated for imaging applications. Although a MOS technology based NTSC colour camera was reported by 'vision' in 1997, the spectral filtering capabilities of standard CMOS processes were rarely exploited.

M. L. Simpson and his colleagues reported CMOS-compatible methods for realizing photodiodes with independent spectral response. These methods included (1) the use of SiO_2 and polycrystalline silicon as thin-film optical filters, (2) formation of photodiodes of different junction depths and (3) controlling the density of interfacial trapping centres at $Si - SiO_2$ interface. They further demonstrated a low-cost monolithically integrated photo-spectrometer using standard CMOS-compatible photodiodes. Realization of a complete portable photo-spectrometer, combined with on-chip digital, analog and wireless circuits, is useful for environmental monitoring, chemicals & drugs detection, for biological and scientific micro-instrumentation and in certain applications which are constrained to low power consumption, low-cost and portability [5]. Until then the reported photodetectors were based on conventional vertical doping profile with buried depletion region, thus limiting the ability of silicon to detect short wavelengths especially in the UV region. Furthermore, conventional photodetectors were not compatible with CMOS process flows and, therefore, could not be monolithically integrated on a single-chip.

Silicon is sensitive to UV, visible and near-infrared regions i.e. from around 200 nm to 1100 nm of wavelength, with its peak response in the near-infrared region. This peak response can be modified to suit specific applications using special antireflection coatings and filters. The electromagnetic spectrum is shown in figure 1.1 where the visible spectrum and the intrinsic silicon detectable spectrum have been highlighted.

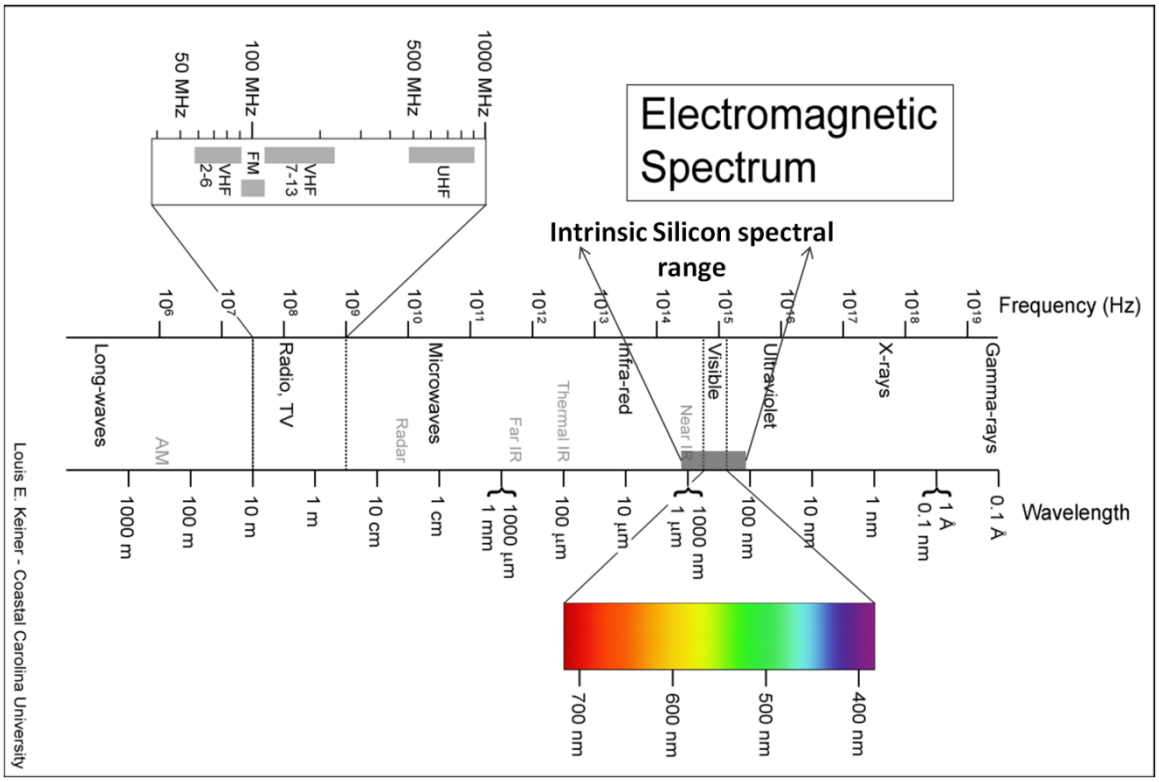

Figure 1.1: Electromagnetic radiation spectrum

1.1. Device Functionality

In this work, two different approaches were employed to fabricate a silicon-based gated lateral p-i-n junction photodetector. The resulting devices are CMOS-compatible and can be easily integrated with surrounding CMOS circuitry. In principle, the device appears as a diode-transistor-like hybrid and detects light with its built-in lateral p-i-n-junction architecture; whereas its vertical MOS gate(s) structure controls the lateral conduction making it appear as a MOSFET for the surrounding circuitry. The devices demonstrated in this work have distinct transistor-like vertical structure with single and double MOS gate(s) to control the quiescent operating characteristics. All the hybrid-photodetectors described in this work use similar lateral p-i-n junction-based architecture.

These gated lateral devices showed gate-bias-induced control over device response. Furthermore, while comparing the lateral device to a conventional vertical photodiode, increased sensitivity to blue wavelengths around 480 nm was observed. The single gate devices showed better response to blue wavelength as compared to conventional photodiodes. In dual gate devices, with the application of proper gate bias, modulation of the spectral

responsivity of the device was observed. This became quite prominent in overlapping dual gate devices, where properly biased double gate structure showed modulation of spectral sensitivity to such an extent that the red (630 nm) and blue (480 nm) wavelength's spectral responses were seen to be inverted. At starting gate bias conditions ($0\text{V}, -5\text{ V}$ and -10 V) the device's response was that of a typical conventional photodiode, however, with further increase in gate bias (-13 V), the device showed similar sensitivities to red and blue wavelengths and with even higher gate bias, it gradually became more sensitive to blue (480 nm) wavelength.

1.2. Gated Structures Reported in Literature

Several types of gated-photodetectors have been reported to date. Their details are discussed in Chapters 3, 5 and 6 [6-11]. Some photodetectors use a transparent gate, light passes through the transparent gate and enters the light detection region, while others use a partial metal gate and here the light passes through the sides of the metal gate structure. Transparent gates can be further classified into two categories. The first category is of devices that use transparent conducting oxides (TCOs), indium tin oxide (ITO) and zinc oxide (ZnO) are examples of it [12], while the second category is of devices that use thin metal gate structure with around 10 nm or less, metal thickness. Due to the thinness of the metal film, excessive absorption of light in the metal is suppressed [12, 13]. The lateral p-i-n photodetectors described in this research work, had metal gate(s) on top whereas the silicon dioxide (SiO_2) acted as an insulator and a passivation layer. The reverse-biased lateral p-i-n diode element detects light which enters into the device through the sides of the gated structure. The idea of a field-effect transistor photodetector, a gated-photodetector, was first introduced by Taylor and Simmons in 1987 whereas Sun et al. in 1989 proposed a gate-controlled photodiode whose external quantum efficiency could be modulated by an applied gate bias. However, significant research interest in such devices has only emerged over the past few years.

1.3. Use of Near-intrinsic Material

Near-intrinsic float zone silicon material was chosen for this project because of a number of reasons.

- Float-zone silicon has smaller amount of background impurities and thus provides longer life time for minority carrier than Czochralski silicon.
- A wide depletion region can be formed that enhances device sensitivity.
- The near-intrinsic region can be fully depleted when the diode is reverse-biased. This results in further widening of the depletion region.
- It has been reported that float-zone silicon has potential advantages for fabricating photodetectors for ultra-low signal levels [14, 15].

1.4. Aims of the Project

The interest in silicon photonics has grown manifolds in the last few years with a view to exploit the established capabilities of silicon electronics for making optoelectronic integrated circuits (IC's). A special focus issue of nature photonics on 'silicon photonics' in August 2010 provided a comprehensive research review of the latest progress and also introduced new ideas for future research trends and challenges. The research described here to make a gated lateral junction photodetector is inline with the general growing interest in silicon photonics.

The chapters in the rest of this thesis describe the work in complete detail. Here is a brief synopsis of their contents.

Chapter 2 comprises of an introduction to semiconductor detectors, their types, theory of operation, operating principles and other characteristics. Finally, different types of pn-junction devices are discussed followed by a brief overview of Charge Coupled Devices.

In Chapter 3 there is a review of existing work on photodetectors, which covers conventional silicon, silicon carbide and compound semiconductor photodetectors. After that, new ideas, introduced by different researchers and devices based on simple lateral p-i-n junction architecture, and gated lateral p-i-n junction architecture are discussed, with reference to the existing literature.

Chapter 4 describes the fabrication tools and techniques employed in the fabrication of gated (single and double) lateral p-i-n photodiodes and integrated metal grating photodetectors. The chapter starts with an introduction and then describes the properties of silicon used for device fabrication, followed by the process steps; illustrated in sequence. Complete details of the

fabrication processes for single gate, double gate and metal integrated devices have been provided in appendix "I" as well.

Chapter 5 treats the two different types of single gate lateral p-i-n photodiodes with regards to their design and operations. Two different types of single gate photodetectors are offset gate photodetector and centre gate photodetector. Their device behaviour is explained with optical and electrical characteristics followed by noise and spectral responsivity measurements.

Chapter 6 is dedicated to dual gate devices, where simple dual gate and overlapping dual gate structures are described in a similar way as in Chapter 5. The overlapping gates actually overlap the adjacent doped n and p regions. The overlapping dual gate device showed gate bias-induced modulation of spectral responsivity.

Chapter 7 outlines the device's sensitivity to linearly polarized white light. The device polarization sensitivity measurements were performed at different angles of a polarizer sheet with respect to the integrated metal grating pattern over the device. As white light is a mixture of red, green and blue lights, so the device's response to linearly polarized red, green and blue light sources is also described there.

Finally, Chapter 8 concludes the research work presented in this thesis. The first part summarizes the whole research work, whereas, in the next half, the future work possibilities are discussed that could follow on form the present research.

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Chapter 2

Semiconductor Light Detectors: Principles

2. Introduction

Light detectors are devices that absorb incident light and generate an output response which may be a chemical, mechanical or electrical change. Semiconductor light detectors – the most commonly used type of light detectors – generate a change in electrical current or voltage to indicate the detection of light. These are also called optical sensors. Such devices are of vital importance in many applications. Optical detectors are used for photography, security screening, medical science, machine vision, scientific research and many other endeavours [1]. Photographic film and moving arm bolometers are examples of very early light detectors. William Herschel used an ordinary thermometer with a blackened bulb to detect infrared radiation. In the twentieth century, optical detectors developed rapidly. Photomultiplier tubes were invented during the early part of that century and are still used for low level light detection. With the birth of solid state electronics in the nineteen-forties, semiconductor-based photodetectors started appearing on the scene and ever since many different kinds of such detectors have been developed. Commercially available detectors include photodiodes, charge coupled devices and avalanche photodiodes.

This chapter provides a brief overview of light detectors with the aim of putting the rest of the thesis in context of existing types of semiconductor light detectors.

2.1. Types of detectors

Detectors act as signal transducers. A light detector when illuminated absorbs photons whose energy is equal to or higher than the band-gap energy of the material, and as a result an electrical signal is produced. This signal, using suitable techniques, may be amplified and then may be converted into a desired output form. Optical detectors, however, function in three different ways.

2.1.1. Photon Detectors

A photon detector detects photons. The photon upon absorption, releases charge carries in the detector that may either modulate the electric current in the device or may result in a chemical change. Photon detectors may be used for the detection of radiation in all spectral regions, extending from infrared (IR), to X – ray.

2.1.2. Thermal Detectors

Thermal detectors soak up photons and convert their energy into heat [2]. Generally, this energy changes the electrical properties of the detector material. As a result electrical current flowing through the detector is modulated. Such detectors feature a broad spectral response. Thermal detectors are important at infrared and sub-millimeter wavelengths and may also be used as X-ray detectors. Bolometers are an example of thermal radiation detectors.

2.1.3. Coherent Receivers

Electric field strength of an electromagnetic wave can be detected by coherent receivers; such detectors store phase information about incoming photons. Their operating principle is based on the interference of the incident photon’s electric field with the electric field of a coherent local oscillator. These detectors are suitable for use in radio and sub-millimetre regions but may also cover the IR region.

2.2. Semiconductor Materials

Semiconductors can be either elemental semiconductors or compound semiconductors. In elemental semiconductors each atom such as Ge or Si is bonded with neighbouring atoms of the same type, forming a covalent bond. Compound semiconductors are alloys of two or more elements in a certain ratio. Common examples of compound semiconductors are GaAs and InP. Semiconductor materials due to their particular properties can be used as conductors or insulators, or even as materials with intermediate properties. In semiconductors there is a small energy gap between the valence and conduction bands.

Silicon is the most widely used semiconductor material. It has four electrons in the outer shell. Atoms in silicon are linked together to form an ordered crystal structure called the "diamond structure". In silicon, atoms are tightly bonded and thus very few free electrons are available; therefore pure silicon behaves almost as an insulator and is also referred to as "intrinsic" silicon. The behaviour of silicon can be changed from an insulator to a conductor; this can be done by adding impurity atoms to silicon. Impurities also called dopants, are other elements and are added through a doping process. Silicon is a group IV element, thus impurities from group III or group V elements can be added to it. An impurity atom like boron (group III) or phosphorous (group V) will add free holes or electrons, respectively, to silicon.

For making silicon electron-rich, phosphorous atoms are diffused so that they replace some of the silicon atoms. As the silicon is tetravalent, it makes four covalent bonds with the phosphorous atoms. The fifth electron, which is an extra electron, is released in the crystal structure making the semiconductor $n-$type doped. Similarly a hole is released upon diffusion of a group III element atom. Group III elements like boron form three covalent bonds, whereas the fourth bond remains missing and acts as a hole. This makes the semiconductor $p-$type doped. In the diffusion process, when an electron is released, the impurity is called a donor, whereas if a hole is produced then, the impurity element is called an acceptor. Heavily doped semiconductors are more conductive and thus have less resistance.

2.3. Semiconductor Photo-detectors

Many types of junction-based detectors exist, Schottky diodes, Quantum well infrared photodiodes, Superconducting tunnel junction (STJ) and semiconductor photodiodes are some examples of such detectors. The interface between a semiconductor and a metal forms a schottky diode, whereas the growth of thin layers of different semiconductors through epitaxy forms quantum wells. A semiconductor-based photodiode is formed by making two oppositely-doped zones adjacent to each other on a single semiconductor substrate. The region at the junction of these two oppositely-doped regions is free from charge carriers and thus has high impedance. The formation of two oppositely doped adjacent regions in silicon or germanium makes a detector highly sensitive.

The function of a semiconductor optical detector is to transform an input optical signal into a useable electrical output. When light falls on the surface of a semiconductor material, photons whose energy is in excess of the band-gap energy of the semiconductor material, are absorbed. This absorption excites an electron to jump into the conduction band and as a result a hole is left in the valence band. These promoted electrons and valence band holes behave as free particles and travel under intrinsic or externally-applied electric field. This continuous separation of electron-hole pairs due to the absorption of photons and their subsequent transport to the respective electrodes in the detector setup, gives rise to a photocurrent (I_{ph}). This photocurrent is directly proportional to the intensity of the incident light.

The process of collecting these optically-generated charge carriers by the electrodes enables us to differentiate between two types of light detectors: photoconductors and photodiodes. Photoconductors are made up of just a slab of semiconductor material, where the applied electric field between the electrodes causes the mobile charge carriers to reach their respective electrodes. In photodiodes the internal electric field of a pn or p-i-n junction performs the charge separation and the charge carriers are later collected by the electrodes. In p-i-n junction photodiodes, unlike in $\mathrm{pn-junction}$ photodiodes an intrinsic region between the p and n regions is left in its pure un-doped state to form an extra-wide depletion region between the n and p doped regions.

When a photon is absorbed by a semiconductor, an electron-hole pair is produced. As silicon is an indirect band-gap semiconductor so there is a strong wavelength dependency which is

described in terms of an absorption coefficient α. The Photocurrent produced as a result of photon absorption can be written as

$$\boldsymbol{I_{ph} = P_o . \frac{e.\lambda}{h.c} . (1 - \mathcal{R}) . [1 - exp(-\alpha_o d)]} \quad 2.1$$

Where P_0 is intensity of the light source, λ is the wavelength of light, e is the electron charge, $\mathcal{R}$ is reflectivity, d is distance and h is the Planck's constant. In Figure 2.1 optical absorption coefficients of some common semiconductor materials are given as a function of wavelength and light penetration depth. These include silicon, germanium, gallium arsenide, indium gallium arsenide and indium gallium arsenide phosphide. In order to select a semiconductor material, for detection in a specific wavelength region, the absorption coefficient of the material plays a key role. In the case of silicon, its 1.12 eV band-gap corresponds to 1100 nm of wavelength. Table 2.1shows the band-gap and other semiconductor material properties for some commonly used semiconductor materials.

Semiconductor	T (K)	E_g (eV)	λ_c (μm)	T (life time)
Intrinsic				
Si	295	1.12	1.1	50 ps
Ge	295	0.68	1.8	10 ns
PbS	295	0.46	2.7	0.1 – 1 ms
PbS	195	0.4	3.1	1 – 10 ms
PbS	77	0.32	3.8	1 – 10 ms
PbSe	295	0.31	4	1 – 10 μs
PbSe	195	0.29	4.3	10 – 100 μs
PbSe	77	0.24	5.2	10 – 100 μs
PbTe	295	0.41	3	1 – 10 μs
PbTe	77	0.27	4.5	10 – 100 μs
CdTe	295	1.55	0.8	
CdSe	295	1.8	0.67	10 ms
CdS	295	2.4	0.53	50 ms
InSb	77	0.22	5.5	1 – 10 μs

Semiconductor	T (K)	E_g (eV)	λ_c (μm)	T (life time)
$Hg_{0.8}Cd_{0.2}Te$	77	0.1	10 – 25	<1μs
Extrinsic				
Ge:Au	77	0.15	8.3	30 ns
Ge:Cu	15	0.041	30	0.5 ns
Ge:Cd	20	0.06	21	10 ns
Ge:Zn	4	0.032	40	10 ns
Si:Ga	4	0.073	17	1 μs
Si:As	20	0.056	22	0.1 μs

Table 2.1: Properties of various Intrinsic and Extrinsic Semiconductors

Semiconductor-based devices generally have many advantages over others like vacuum tube photo-detectors. Unlike vacuum tube photo-detectors, semiconductor-based photo-detectors require low voltages to function and the fabrication process is much simpler and economical. The spectral sensitivity of semiconductor-based photodetectors spans the electromagnetic spectrum from the far-infrared to UV radiation. Semiconductor-based devices can be categorized into photoconductors and photodiodes. These are discussed in their respective sections after a discussion of performance characteristics.

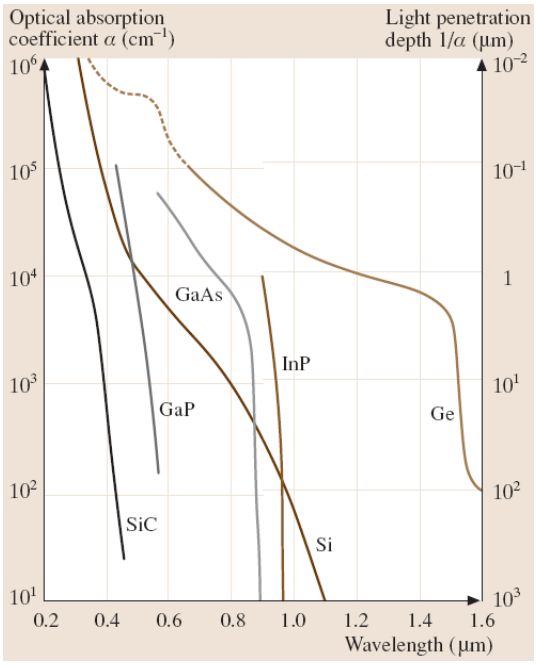

Figure 2.1: Optical absorption curves for common elemental and compound semiconductor materials. [3]

2.3.1. Performance Characteristics

Detectors are generally classified on the basis of some of the following parameters; these are sometimes called figures of merit [4].

2.3.1.1. Quantum Efficiency

Quantum efficiency is the probability, that a single incident photon will generate an electron-hole pair that will contribute to the photo-detector output current. The quantum efficiency η can be represented by the following two equations.

$$\boldsymbol{\eta = \frac{I_{ph}/q}{P/h\nu}} \quad \mathbf{0 < \eta < 1} \qquad 2.2$$

Here, P is the power of the incident light source (in watts). Quantum efficiency can also be expressed as

$$\boldsymbol{\eta = T_{op} F_{EHP} (1 - e^{-\alpha L})} \qquad 2.3$$

Here T_{op} is the percentage optical power transmitted inside the photo-detector, at the photo-detector-interface, F is the fraction of optically-generated electron-hole pairs which have contributed to the photo-current. α is the absorption coefficient and L is the length of the photo-detector. Coupling and reflection losses are represented by T_{op}. All the electron-hole pairs produced, do not contribute to photo-current, some of them recombine in the traps. These recombination centres are usually abundant and are mostly found at the material surface. Absorption increases with increase in length of the photo-detector. As the absorption coefficient is wavelength dependant so the quantum efficiency is also a function of wavelength.

Quantum efficiency is influenced by the absorption coefficient. The quantum efficiency of good detectors is close to unity. It is to be noted that the quantum efficiency is independent of the energy of photons striking the surface of the semiconductor.

2.3.1.2. Spectral Response

Spectral response of a photodetector is the efficiency with which different wavelengths are detected. Spectral responsivity can be written as.

$$SR = {I_{ph}}/{P_o} \qquad 2.4$$

Here, I_{ph} is the photo-induced current and P_o is the power absorbed from the optical source. Its unit is Amps/Watt. As the spectral response reveals how the responsivity of a photo-detector varies with change in wavelength, so it is often the basis for selecting a detector for a particular application in a specific wavelength range. The expression for quantum efficiency can also be used to determine the spectral sensitivity as:

$$SR = \eta \frac{e.\lambda}{h.c} \qquad 2.5$$

The responsivity of an ideal photodiode when compared to a typical silicon photodiode shows that the difference in responsivity for short wavelength photons is due to thermal losses, whereas for longer wavelengths it is due to the reduction in absorption coefficient. Responsivity increases in silicon with increase in wavelength as shown in Figure 2.2 however, it falls sharply just close to the cut-off wavelength λ_c.

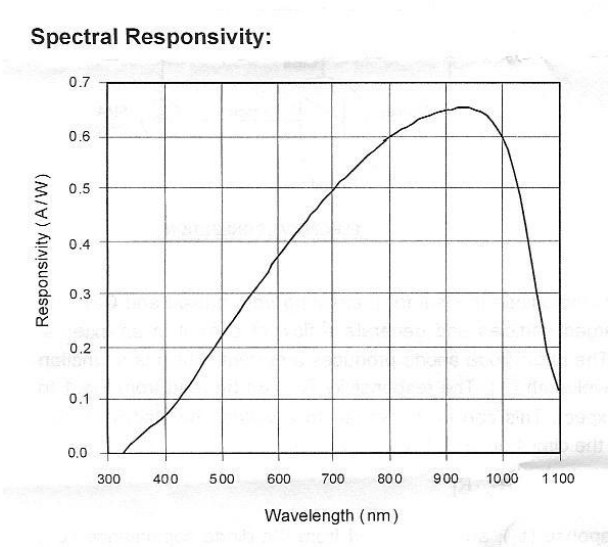

Figure 2.2: Spectral response of silicon.

2.3.1.3. Linearity

Detectors are classified by the linearity of their response in which the output is linear with incident intensity for a broad range of inputs. If the output of the detector is plotted against the input power, then ideally, there should be no change in the slope of the curve. Therefore, a photodetector is said to be linear if the responsivity is constant i.e. independent of incident optical power [5].

2.3.1.4. Dynamic Range

Dynamic range is the maximum range of input optical power over which a detector can operate properly.

2.3.1.5. Noise

Detector response inevitably contains electrical noise in it. This noise is caused by several mechanisms operating during the light detection process. Noise can be defined as any undesired signal contained within a desired signal. Unwanted noise signals mask the actual signal and affect the detection process. In optical detectors often four noise sources are seen, namely Johnson noise, Shot noise, 1/f noise, and Photon noise.

Johnson noise or nyquist noise, arises due to thermal fluctuations in the conducting material, whereas shot noise is produced by fluctuations in the stream of electrons in the device, it is also referred to as generation-recombination (G-R) noise. $1/f$ noise generally exists when the modulation frequency f is low. It is also commonly referred to as excess noise, whereas photon noise is due to random arrival rate of photons [4]. Some sources of noise can be eliminated whereas others can only be reduced. External noise sources, like photon noise, cannot be reduced. The impact of a single noise factor or combination of various types of noise will set the maximum detectivity of an optical detector.

2.3.1.6. Temporal Response

For many applications it is important to ascertain how fast the detector responds to the changes in the intensity of light, i.e. to the arrival rate of photons. Terms associated with temporal response of a detector are: rise time and fall time. Rise time is defined as the time difference required to reach from 10 % to 90 % of the peak response. Whereas, the fall time is opposite to it, i.e. the time difference required to reach from 90 % to 10 % of the peak response on the trailing edge, sometimes it is also called decay time [4].

2.3.1.7. Frequency Response

The response time of a photodiode is dependent on three fundamental factors: (1) drift time of the carriers to cross the depletion region, (2) diffusion time of carriers generated outside the depletion region and (3) junction capacitance [6]. The drift of carriers through the depletion region is usually quite rapid due to the built in electric field of the junction. Drift velocity can be further increased with an applied reverse bias until it reaches its saturation value. Saturation drift velocity for silicon is $\sim 10^7\ \mathrm{cm/s}$ [7]. The diffusion process, on the other hand, is influenced by the recombination time "τ", and is thus relatively slow. The diffusion time can be improved by ensuring that all the electron-hole pairs are produced within the depletion region or within one diffusion length from the depletion region. The capacitance effect on frequency response is discussed in the capacitance section below and later in the $pn-$ junction photodiode section as well.

2.3.1.8. Capacitance

p and n regions separated by an insulating depletion region form a capacitor in junction diodes. The capacitance of a photodiode is relatively high as the charge distribution across the junction forms a parallel plate capacitor with a very small gap between the plates. Capacitance can influence the frequency response of a photodiode and it often determines the limiting noise of the amplifier used to read out its signal. Low junction capacitance increases the frequency response of photodiode and improves the device speed. However, if the capacitance of the junction is too low i.e. the depletion region is wide enough, it would cause increased transit time which will slow down the overall device response.

2.3.2. Photoconductors

A photoconductor is formed from a uniform slab of semiconductor material. When the incident light falls upon it, a portion of the light is reflected and the rest of the light is absorbed into the semiconductor, thus increasing the conductivity of the semiconductor material through the generation of free charge carriers. Photoconductors can be made using intrinsic or extrinsic semiconductor materials. Operating mechanism, advantages and disadvantages of both types of photoconductors are discussed next.

2.3.2.1. Intrinsic Photoconductor

Intrinsic photoconductors are made from high resistance pure semiconductor materials. When light shines on the surface of an intrinsic photoconductor, photons with higher energy than the band-gap energy of the semiconductor material are absorbed. Photons break bonds, so an electron gets excited from the valence band and jumps into the conduction band, leaving a hole in the valence band. This phenomenon is depicted in Figure 2.3.

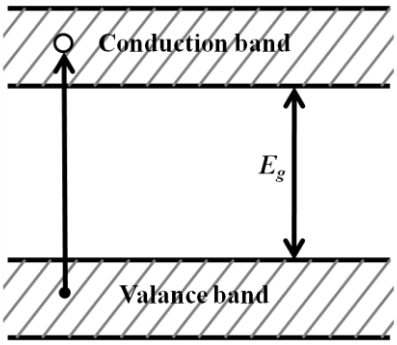

Figure 2.3: Intrinsic Photoconductor [8]

These free charge carriers i.e. electrons and holes, under the influence of applied electric field, drift through the semiconductor. As the electrons move quickly because of their lower effective mass so the increased photo conductivity mainly comes from increased photo-induced electron density. Electron mobility in silicon varies with change in temperature. The mobility of an electron at different temperatures is shown in Figure 2.4.

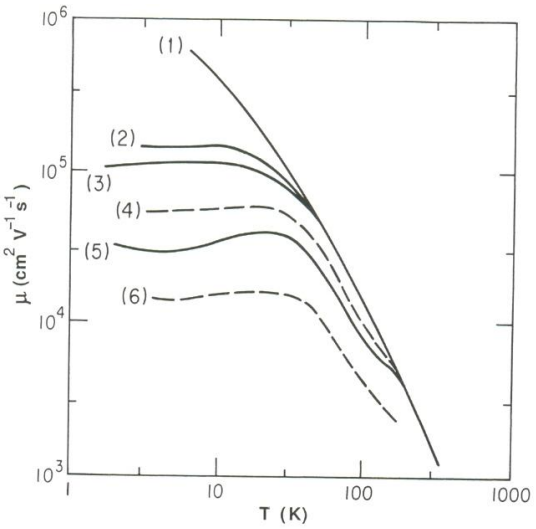

Figure 2.4: Variation of electron mobility in silicon with temperature and impurity concentration (After Norton, Braggins and Levinstein (1973), and Canali et al., (1975), The solid lines are for phosphorus doped material at concentrations of $\leq 1 \times 10^{12}$, 4×10^{13}, 2.5×10^{14}, and 1×10^{16} cm^{-3}, respectively, for curves (1) − (3) and (5), The dashed lines are for arsenic doped material at concentrations of 8×10^{15}, and 8×10^{16} cm^{-3}, respectively, for curves (4) and (6).[2])

Intrinsic photoconductors have high resistance regions due to the availability of very few free charge carriers. An electric field is maintained in this high resistance region to control the movement of photo-induced free charge carriers. This eventually produces a current in the external circuit when charge carriers drift to collecting electrodes.

In intrinsic photoconductors, the spectral response is generally limited to photons which have higher energy than the band-gap energy of the semiconductor material. In semiconductor materials like germanium and silicon, these band-gap energies correspond to wavelengths of 1.8 μm and 1.1 μm, respectively. The performance of an intrinsic photoconductor degrades with increase in wavelength beyond 15 micron. Intrinsic photoconductors are used for their rapid response time; however, these photoconductors suffer from high Johnson noise [2]. A reference intrinsic photoconductor with transparent contacts is shown in Figure 2.5.

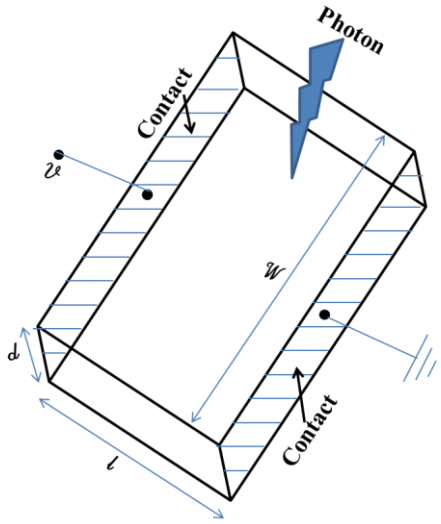

Figure 2.5: Photoconductors and transverse contacts [2]

The carrier concentration of p and n-type carriers in an intrinsic photoconductor is the same. Here $n = p = {}^{\varphi\eta\tau}/_{\omega dl}$ where n and p are carrier concentration of n and p type carriers. φ is the number of photons arriving per second, η is the quantum efficiency and τ is the mean life time of the charge carriers. The product of $\omega, d \,\&\, l$ represents the volume of the photoconductor i.e. width, depth and length.

2.3.2.2. Extrinsic Photoconductors

Intrinsic photoconductor material can be made extrinsic by modifying the impurity concentration through doping. Silicon-based extrinsic photoconductors typically contain $10^{15}\ cm^{-3}$ to $10^{21}\ cm^{-3}$ impurity atoms. Diffusion of impurity atoms from elements of column III and V of the periodic table, form p and $n-$ type extrinsic semiconductor material, respectively. This addition of dopant atoms to adjust the dopant concentration increases the dark current in extrinsic photoconductors. The dark current is extremely temperature dependent and it increases with increase in temperature and doping. Extrinsic photoconductors are based on smaller band-gap (E_g) semiconductors to detect low energy photons i.e. those from mid and far IR regions. Stressed detectors and Blocked impurity band (BIB) detectors are two examples of extrinsic photoconductors.

Using stressing technique with p-type photoconductors, the acceptor binding energy can be reduced. In Ge:Ga photoconductors for instance the stressing process extends the wavelength

range from 115 μm to beyond 200 μm. BIB detectors work with low conductivity and high absorbance. To achieve this, different layers of varying impurity concentration are needed. In BIB detectors, a separate n-type layer is used for photon absorption with a small quantity of p-type impurity in it.

Extrinsic photoconductors with dopant states located in the band-gap are suitable for longer wavelengths in the range of $10-100\,\mu m$. Figure 2.6 explains the physics behind the absorption of photons in extrinsic semiconductors. In the case of a semiconductor with $P-$ type conductivity an electron can be energized from the valence band to the acceptor level. Whereas, for a semiconductor with $n-$ type conductivity, photon absorption can cause an electron to get excited and jump from the donor level to the conduction band.

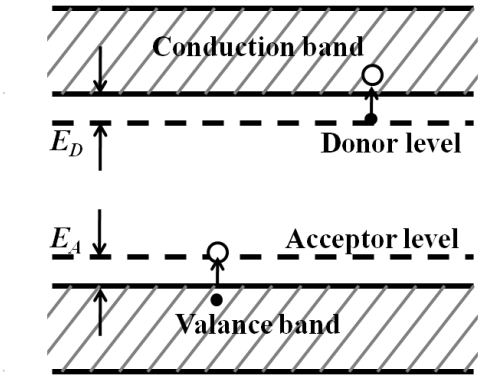

Figure 2.6: Extrinsic Photoconductor [2]

In Figure 2.6 a photon whose energy (hν) is greater than the acceptor level energy E_A excites an electron to the acceptor level, leaving a hole in the valence band. This causes change in conductivity of the material. Similarly, for $n-$ type photo conductivity, a photon whose energy (hν) is greater than the energy of the donor level E_D promotes an electron from the donor level to the conduction band. As a result, the long wavelength limit for photon detection is increased significantly as donor and acceptor levels are close to conduction and valence band edges, respectively, as shown in Figure 2.6. Band gap energy, long-wavelength-limit, and the life time of excited states for various intrinsic and extrinsic semiconductors are shown in Table 2.1 [8].

As stated earlier for extrinsic photoconductors, the experimentally determined long-wavelength-limit is about 100 μm. This can be achieved by the use of pure semiconductors like Ge or InSb, at very low temperatures. Intrinsic photoconductivity processes require higher

energies to operate whereas extrinsic photoconductivity can be triggered by lower energy photons. Lower excitation energies cause increase in thermally produced dark current. This dark current can be minimized by operating these detectors at low temperatures.

2.3.3. pn-Junctions

Silicon's properties can be changed by changing its carrier concentration through either diffusion or ion implantation. Impurity atoms such as phosphorous or boron, introduced inside the material, using suitable doping technique, can make silicon n or $p-$type.

Adjacent p and n type regions in a semiconductor form a $pn-$junction. Such structures allow current to flow in only one direction. In intrinsic silicon the Fermi energy lies in the centre of the band-gap. In $n-$type semiconductor, where donor impurities like phosphorous or arsenic contribute mobile electrons, the Fermi level lies close to the conduction band. However, in $p-$type material the Fermi-level lies close to the valence-band. Here acceptor impurities contribute mobile holes. The Fermi energy depends upon carrier concentration and the two are related as: [8]

$$\boldsymbol{n = n_i e^{\left(\frac{E_F - E_i}{kT}\right)}} \qquad 2.6$$

$$\boldsymbol{p = n_i e^{\left(\frac{E_i - E_F}{kT}\right)}} \qquad 2.7$$

Here, n and p refer to the number density of electrons and holes in conduction and valence band, respectively. Whereas, n_i refers to the number density of intrinsic electrons and holes in the conduction and valence bands. In silicon at 300 K, n_i is 1.45×10^{10} cm^{-3}. The mass-action relationship specifies the dependence of intrinsic carrier concentration on the concentration of mobile electrons and holes. The Law of mass action states that $np = n_i^2$. The number of donor atoms N_D in $n-$type silicon corresponds very closely to the number of mobile electrons, whereas the number of acceptor atoms, N_A, in $p-$type silicon is approximately equal to the number of mobile holes.

The formation of a carrier depleted region in a pn-junction is described next. Majority carriers from both p and n regions, i.e. electrons from the $n-$type region and holes from the $p-$type region diffuse into the opposite region. Electrons diffusing into the $p-$type region

combine with the majority holes present there, and holes diffusing into the n – type region combine with the majority electrons found there. This process then produces positively charged donor ions and negatively charged acceptor ions. Thus at the junction of the p and n regions an area depleted of majority charge carriers is formed where an electric field is present due to positive donor ions and negative acceptor ions. This field starts opposing the further diffusion of majority carriers into the opposite regions. This region depleted of mobile majority charge carriers lies at the junction and is referred to as the depletion region. This is illustrated in Figure 2.7(b). At equilibrium the depletion layer has a net built-in potential V_o, which causes band bending as illustrated in Figure 2.7(d).

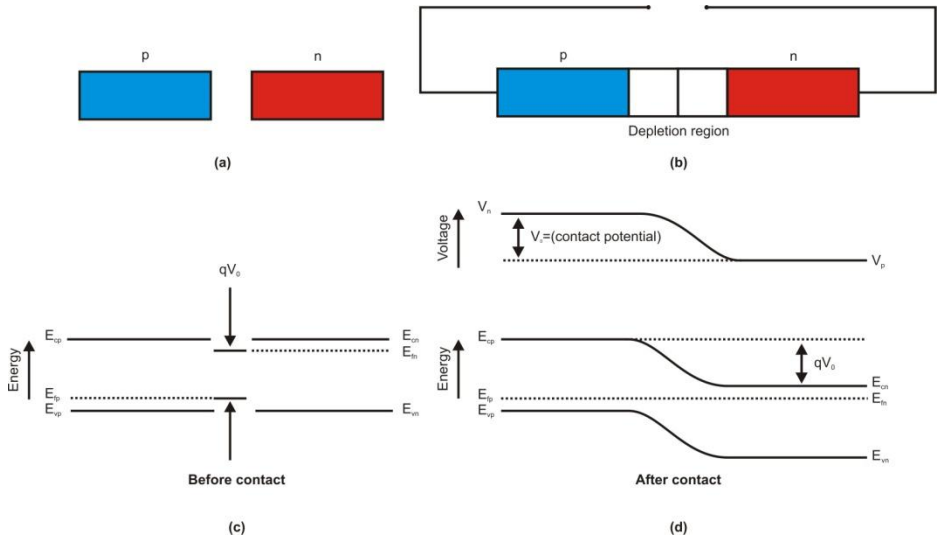

Figure 2.7: (a) p and n regions before contact, (b) p and n regions after contact, (c) Visualization of potential before contact and (d) Development of a contact potential and band diagram

Figure 2.7 (a)-(d) show separate p and n type materials and the formation of depletion region when these two oppositely doped regions come into contact. This built-in potential in the depletion region can be calculated using equation 2.8, if carrier concentration values in both the n and p regions are known.

$$\boldsymbol{V_o = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}} \qquad 2.8$$

Here, N_A and N_D stands for the concentration of acceptors and donors impurity atoms on the p and n side of the material. Once the built-in potential is known, the width of depletion region can also be calculated using the following equation.

$$W = \left[\frac{2\varepsilon V_o}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2} \quad 2.9$$

Here, ε is the permittivity of the medium. In this equation thickness of the depletion layer depends mostly upon the carrier concentration in the lightly doped region, and that most of the depletion region exists in the lightly doped region.

In a pn − junction the current can be divided into diffusion and drift currents. Diffusion current is produced due to different carrier concentrations in the two adjacent p and n regions, whereas an electric field e.g. built-in electric field across the depletion region, causes drift current to flow. When a bias is applied to the pn − junction diode, the equilibrium level is disturbed. The forward and reverse bias cases are discussed next.

In forward bias when a positive voltage is applied to the p side of the junction and a negative voltage to the n side, the resulting electric field starts opposing the built-in potential of the pn − junction. This changes the Fermi level as well. Opposition to the built-in potential of the pn − junction due to biasing reduces the built-in potential of the junction. This results into more electrons having sufficient energy to overcome the potential barrier, causing an increase in diffusion current. The diffusion current starts dominating, because the small drift current is relatively independent of applied bias. Finally, the width of the deletion region is reduced due to forward biasing, by the factor of applied bias i.e. $V_o - V_f$.

In forward bias, the junction becomes conducting when biased with a voltage greater than V_o. The forward and reverse bias characteristics of a pn-junction diode are shown in Figure 2.8.

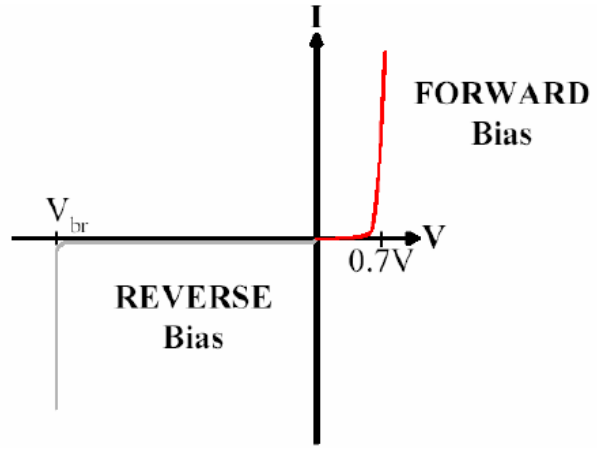

Figure 2.8: Current-Voltage (I-V) Characteristics of a silicon pn-junction

In reverse bias when a negative potential is applied to the p side of the junction and a positive potential to the n side, the resulting electric field supports the built-in electric field of the junction. This causes an increase in the height of the potential barrier and in turn reduces the diffusion of charge carriers. Now fewer electrons are available to diffuse through this high energy barrier. In reverse bias, drift current dominates and there is a nearly constant reverse saturation current. It is nearly constant because the controlling factor for drift current is the generation time of minority carriers within a diffusion length of the depletion region, not the strength of the applied field. Reverse bias aids the built-in potential of a $pn-$junction, as a result the width of the depletion region increases by a factor $V_o + V_r$. As explained above, the reverse saturation current is relatively small and of constant value. Thus no current flows initially. Even in the presence of an increased reverse bias a very small current flows. Increasing the reverse bias, eventually causes junction break down. Once the break down occurs the junction becomes highly conducting. At high reverse bias, avalanching effect also causes the junction to breakdown.

Carrier tunnelling can also cause the break down to occur at modest biasing conditions. In this case the reverse bias brings the conduction band in the n-type material below the valence band in the p-type material. Here energetically it is favourable for the electron to get into the depletion region without first moving into the conduction band of the p-type material. If the depletion region is thin enough, there is a finite probability that electron with its wave nature, will tunnel through the junction.

In Figure 2.9 the electric field, width of the depletion region and energy band diagrams of a $pn-$junction are shown when no bias is applied and with forward and reverse bias configurations.

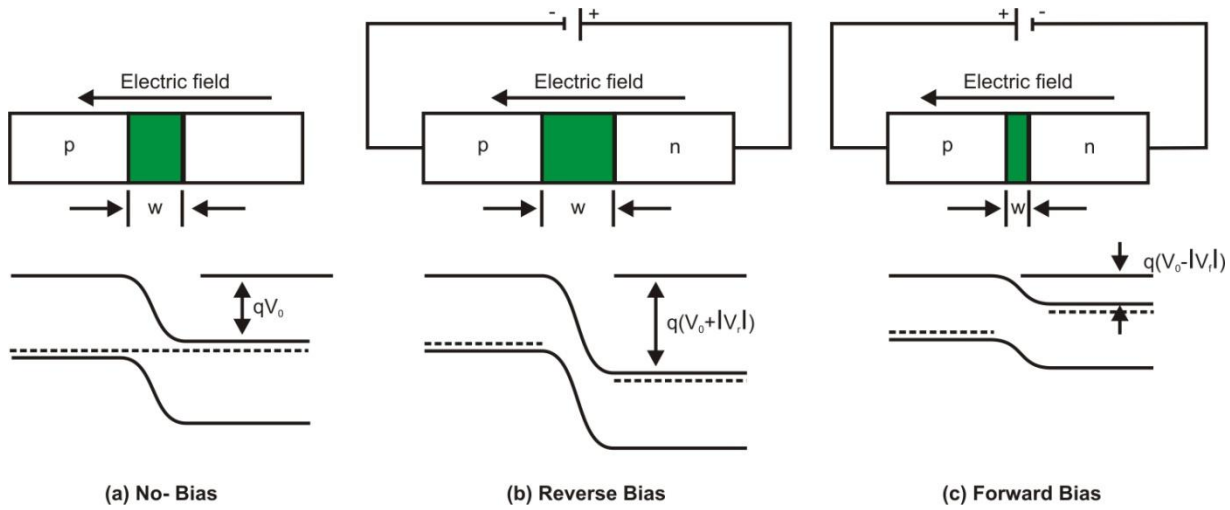

Figure 2.9: pn-junction under unbiased, forward and reverse biased configuration

2.3.3.1. pn-Junction Capacitance

A pn-junction consisting of two conducting regions separated by a depletion region is characterized by a capacitance. The distribution of positive and negative charges across the junction (depletion region) of a diode determines this capacitance. The capacitance of a diode influences its frequency response. It also determines the limiting noise of the amplifier, used to read out its output signal. The length of the n and p part of the depletion region varies with the impurity concentration, as:

$$\mathbf{N_A l_p = N_D l_n} \qquad 2.10$$

Using the bias voltage $V_o - V_b$, the widths *"l_p"* and *"l_n"* of p and n parts of the depletion region can be calculated using the following equations.

$$\boldsymbol{l_p} = \left[\frac{\mathbf{2\varepsilon N_D(V_o - V_b)}}{\mathbf{qN_A(N_A + N_D)}}\right]^{1/2} \qquad 2.11$$

$$\boldsymbol{l_n} = \left[\frac{\mathbf{2\varepsilon N_A(V_o - V_b)}}{\mathbf{qN_D(N_A + N_D)}}\right]^{1/2} \qquad 2.12$$

The collective width of the depletion region can be calculated by summing up the width of the n and p parts of the depletion region. Thus,

$$\mathbf{w} = \boldsymbol{l_p} + \boldsymbol{l_n} = \left[\frac{\mathbf{2\varepsilon(N_A + N_D)(V_0 - V_b)}}{\mathbf{qN_AN_D}}\right]^{1/2} \quad 2.13$$

Finally, the junction capacitance can be calculated by the parallel plate capacitor formula,

$$\mathbf{C_j} = \boldsymbol{\varepsilon}\,\frac{\mathbf{A}}{\mathbf{w}} = \boldsymbol{\varepsilon_{si}\varepsilon_o}\,\frac{\mathbf{A}}{\mathbf{w}} \quad 2.14$$

Here, ε_{si} & ε_0 are the dielectric constant of the semiconductor material and the permittivity of free space, respectively, while A is the junction area. The capacitance of a $\mathrm{pn-junction}$ decreases with increase in width of the depletion region. Operating the diode in reverse bias further increases the depletion layer width i.e. it decreases the capacitance and improves the speed of the device. However, if the depletion region is too wide, the transit time across the junction starts limiting the overall temporal response of the photodiode.

2.3.4. Photodiodes

Photodiodes are pn-junction diodes fabricated for the purpose of light detection. Photodiodes are fabricated with oppositely doped regions on a semiconductor substrate. These adjacent regions of opposite impurity doping result in the formation of a space charge region, which is free from charge carriers and has high impedance. Most $\mathrm{pn-junction}$ photodiodes are fabricated using silicon or germanium. They exhibit high sensitivity for detecting visible and near IR wavelengths at room temperature [9]. When light falls on a pn-junction photodiode, the photons which have energy higher than the band-gap energy of the material, generate electron-hole pairs. Photodiodes may either operate in photoconductive or photovoltaic mode. Minimum dark current is seen in photovoltaic mode, whereas fast switching speed is seen in photodiodes when working in the photoconductive mode [10]. In reverse bias "photoconductive mode" under the influence of an applied electric field the hole is attracted towards the anode, and the electron is attracted towards the cathode which produces a photo-current, provided the circuit is externally closed.

$\mathrm{pn-junction}$ diodes have specific current-voltage characteristics as shown in Figure 2.8. Under illumination these characteristics change as seen in Figure 2.11, when photons are absorbed and additional electron-hole pairs are produced. The generation mechanism of electron-hole pairs and their movement are illustrated in Figure 2.10. Here thick solid arrows indicate the fast drift process within the depletion region, and thin dashed lines represent the

diffusion of charge carriers into the depletion region, from within one diffusion length of the depletion region.

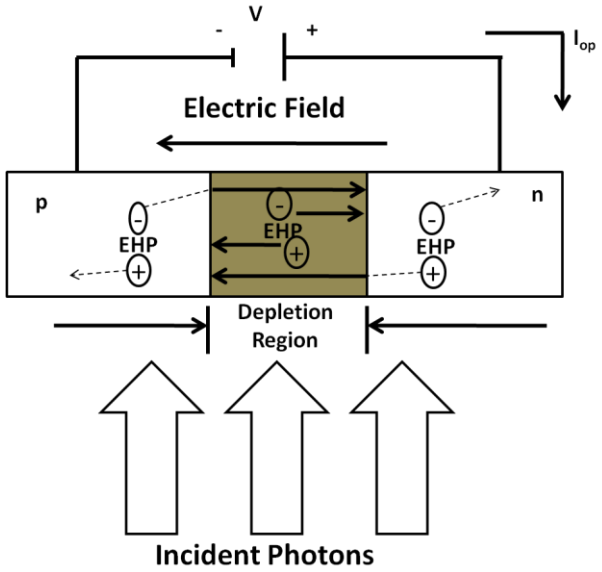

Figure 2.10: Drift and diffusion of photo-generated electron-hole pairs in reverse bias pn-junction

In reverse bias configuration, electron-hole pairs produced in the depletion region are swept across by the junction electric field. Electrons combine with holes in the n region, whereas holes combine with electrons in the p region of the photodiode. Additional electrons necessary for recombination with photo-generated holes in the p region are pulled across the terminal from the n region. A similar mechanism fills in additional holes in the n region of the photodiode. Electron-hole pairs produced farther away from the depletion region, i.e. more than a diffusion length away do not contribute to photo-current I_{op} and recombine randomly.

The current-voltage characteristics of a diode can now be modified by adding the photo-current parameter to the diode equation:

$$\mathbf{I = I_o\left(e^{\frac{qV}{kT}} - 1\right) - I_{ph}} \qquad 2.15$$

The photocurrent produced in a $\mathrm{pn-junction}$ photo-detector is proportional to the incident optical power, before the photo-detector reaches its saturation level. Ideal current-voltage characteristics of a $\mathrm{pn-junction}$ photodiode at different optical powers are shown in Figure 2.11.

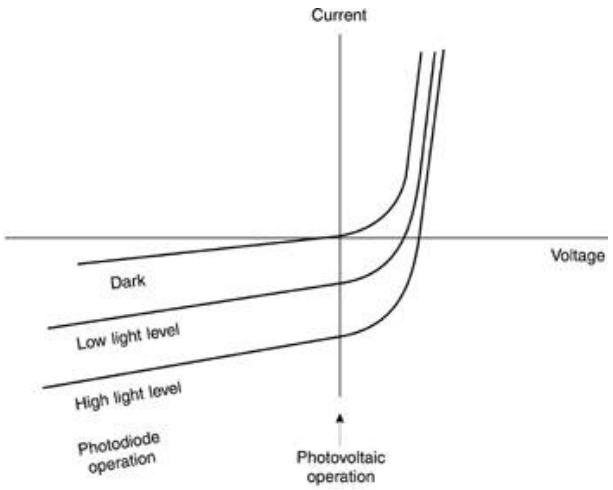

Figure 2.11: Ideal current-voltage characteristics with three different incident optical powers.

When photons are absorbed, electron-hole pairs are produced; a fraction of electron-hole pairs which are produced outside the depletion region move towards the junction by means of diffusion. The diffusion mechanism is important to understand the electrical behaviour of a diode. Diffusion of charge carriers and the rate at which photons are absorbed are main factors affecting the quantum efficiency of a photodiode, whereas the junction capacitance of a pn – junction photodiode determines its temporal response and the upper frequency limit of its operation.

2.3.4.1. Photoconductive Mode

A photodiode when reverse biased operates in photoconductive mode. The response time is reduced i.e., the photodiode becomes faster, however, the noise is also considerably increased. Reduced response time results from increased depletion layer width, and thus decreased junction capacitance. These two factors contribute to a faster response time. When the diode is reverse-biased a small amount of reverse or saturation current flows. The photocurrent, however, remains the same, as it is linearly proportional to the intensity of light.

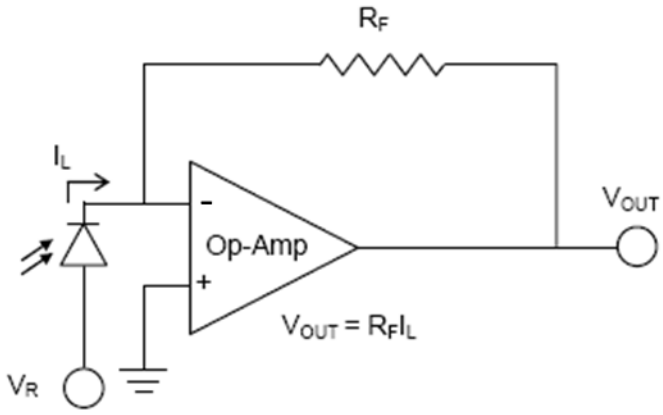

Figure 2.12: Photoconductive mode operation

2.3.4.2. Photovoltaic Mode

A photodiode when operating in a photovoltaic mode has no bias applied across it. Initially, no photo current flow through the device and a voltage builds up. As a result the diode becomes forward-biased and a current begins to flow. A dark current, however, flows in the direction opposite to the photocurrent. This is the fundamental principle behind a solar cell. A solar cell is also referred to as a large area photodiode.

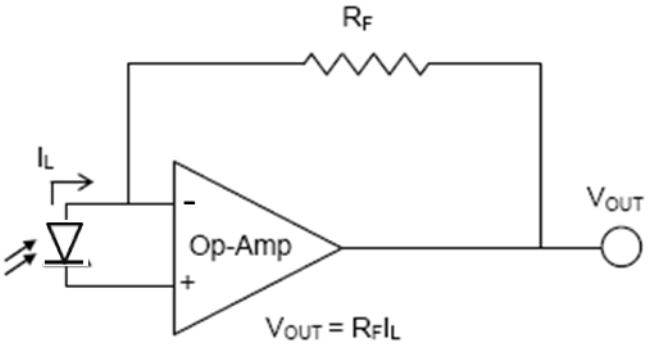

Figure 2.13: Photovoltaic Mode

2.3.5. p-i-n Photodiode

A p-i-n junction diode is a commonly used variation of the pn – junction architecture. Figure 2.14 illustrates a p-i-n junction diode and its energy band diagram. A p-i-n junction diode is

formed with an intrinsic or near-intrinsic semiconductor material with p and n regions on the two sides. A p-i-n junction diode fabricated with pure intrinsic silicon material is classified as a p-i-n junction diode, whereas if a lightly n or p doped near-intrinsic silicon material is used then the p-i-n junction diode structure is referred to as $p-\pi-n$ or $p-\upsilon-n$ architecture, respectively. In case, intrinsic silicon is used to fabricate the p-i-n junction diode, two depletion regions would be formed and these can be forced to overlap in the intrinsic region, this overlap eventually appears as a single large depletion region covering the whole intrinsic part of a p-i-n junction diode.

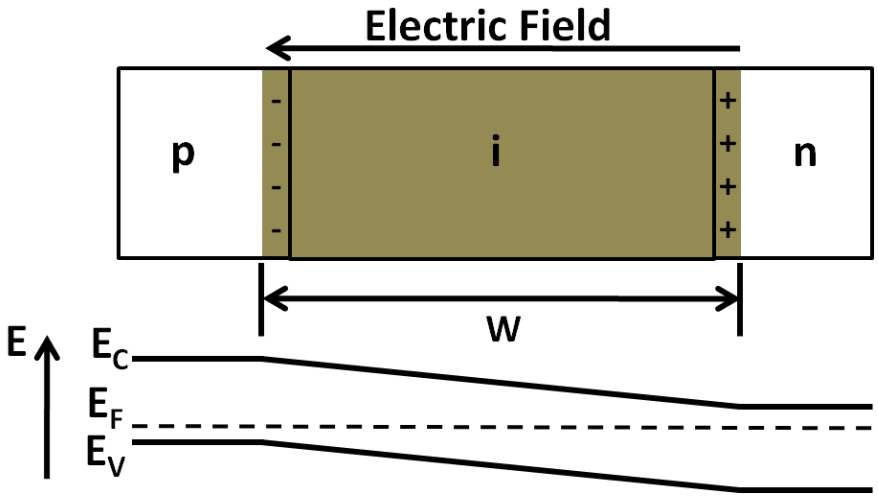

Figure 2.14: p-i-n junction diode and its energy band diagram

Capacitance equation 2.14 shows that the junction capacitance is reduced as the depletion region gets wider. Generally a photodiode is fabricated in such a way that most of the photons are absorbed in the depletion region, and the optically-induced free charge carriers drift under the influence of the built-in electric field of the depletion region. This improves the frequency response of the diode. The width of the depletion region can be increased by decreasing the impurity concentration in the region of the diode that forms the junction. Alternatively a high resistivity intrinsic or near-intrinsic layer can be added in between the highly n and p doped regions of the diode creating a p-i-n junction diode. In this vertical p-i-n architecture, light is absorbed into the diode and passes through a very thin p doped top layer. This p doped top layer, over a near-intrinsic region is deliberately made thin enough so that negligible absorption occurs in this thin layer, and most photons are able to reach the intrinsic layer where the depletion region and its electric field exist.

One important structural parameter for the p-i-n junction diode is the thickness of the intrinsic region which must be made thin enough so that the carriers while drifting across the depletion region are able to reach the electrodes before they recombine.

Numerically, τ_{PIN} should ideally be less than the recombination time (τ_{rec}).

The temporal response of a p-i-n junction diode is given by,

$$\tau_{PIN} = \frac{l^2}{\mu(V_0 + V_b)} \qquad 2.16$$

This shows that at a high biasing voltage, the detector will have a very fast response. The device structure discussed in the context of gated photodiodes in Chapters 5 and 6, and the grating-based architecture discussed in Chapter 7, is a lateral structure that is not like the conventional vertical structures. However, the current-voltage characteristic of a lateral p-i-n junction photodiode is very similar to that of a vertical p-i-n junction photodiode. p-i-n junction photodiodes have very high breakdown voltage; typical biasing voltage can reach ~ 100V.

2.3.6. Avalanche Photodiode

Another type of a pn-junction photodiode is an avalanche photodiode (APD). Its structure is more sophisticated than that of a p-i-n junction diode. It features a region with an exceptionally high electric field. A standard APD is illustrated in Figure 2.15.

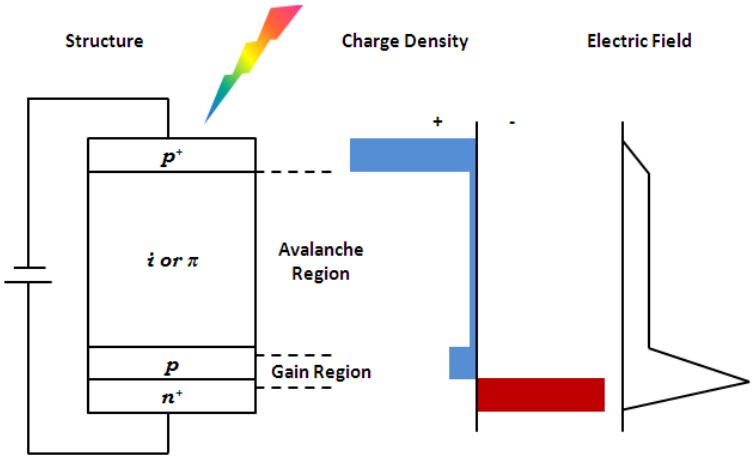

Figure 2.15: Standard APD

In the depletion region of an APD, most of the photons are absorbed and primary carriers are produced. These primary carriers can acquire sufficient kinetic energy in the avalanche region to excite additional electron-hole pairs. The newly created electron-hole pairs on the way again acquire sufficient kinetic energy in the gain region to produce further electron-hole pairs. This phenomenon is called avalanche multiplication. The process of avalanche breakdown in a normal reverse bias diode is based on impact ionization, and requires very high (100 – 400 V) reverse bias voltages [11].

Internal gain in an APD, combines the benefits of both $p-i-n$ diode and a photomultiplier. These high-gain APDs are superior to normal photodiodes in many applications like light-wave communication systems, where fast junction-based detectors with small time constant are needed. The avalanche process predominantly reduces the relative contribution of Johnson noise, in a similar way as is the case with photo-multiplication process. Silicon APDs are most suitable for the wavelength range from 0.8 to 0.9 μm, where they show relatively low noise and fast response [8].

The fabrication of APDs is similar to that of normal photodiodes; however, an important consideration is to obtain uniform amplification over the entire photosensitive area. This requires greater care for ensuring the uniformity of the junction. In an APD, the top $p-$ layer is kept very thin usually less than 1 μm to let the incident power reach the intrinsic region. If the incident power is absorbed in the intrinsic region, the avalanche gain builds up quickly. This is because silicon has larger ionization coefficient for an electron than that of a hole, thus free charge carriers are mainly produced by the electrons. This is further supported by the high reverse bias voltage that creates a strong field in the intrinsic region. This makes silicon a preferred material to fabricate APDs [8].

2.3.6.1. Multiplication Process

Here, we take a closer look at the carrier multiplication process in APDs. As shown in Figure 2.16, the electrons drift in the positive direction with velocity v_n and the holes drift in the negative direction with velocity v_p. The width of the space charge region is w.

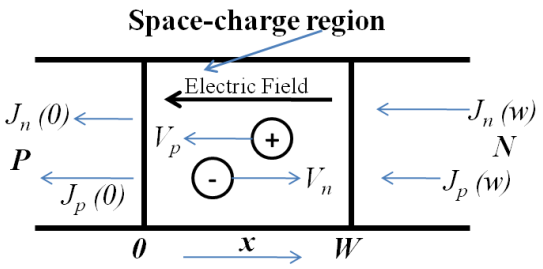

Figure 2.16: Avalanche Multiplication process in APDs [8]

The current density for electrons and holes are J_n and $J_{p,}$ respectively. These in turn relate to carrier densities n and p by the relations $J_n = -env_n$ and $J_p = epv_p$. Here, e is the value of the electron charge. The total current then becomes $J = J_n + J_p$, which is positive in the direction of the field. In multiplication process, $|J_n|$ increases, while $|J_p|$ decreases.

In an APD, the electric field due to the applied bias is located in the depletion region, because of its high resistance. When the electric field strength reaches values of the order of 10^5 Vcm^{-1}, electron-hole pairs are created. This phenomena is described by α and β, the ionization coefficients of electrons and holes, respectively [8].

It is quite important to ensure carrier multiplication without producing excess noise. In APDs it is crucial to keep the ratio of the ionization coefficient of electron and hole to a minimum. In silicon this ratio is a strong function of the electric field. Thus, to keep the noise at the minimum level, the electric field required for an avalanche to build-up must be kept at the lowest possible level. The multiplication factor M corresponds to the internal gain provided by the APD. [12]

$$\boldsymbol{M = \frac{I}{I_{ph}}} \qquad 2.17$$

Here, I denotes total output current, once carrier multiplication takes place, whereas, I_{ph} is the initial or primary photocurrent, before the carrier multiplication starts.

2.3.6.2. Multiplication Noise

The noise at the output of an APD is a combination of noise produced due to signal amplification, and due to the multiplication process. The noise produced because of the

multiplication process, depends upon the relative magnitude of α and β, i.e. ionization coefficients of electrons and holes [13]. Generally, the best case is encountered when either the ionization coefficients for electron or hole is zero while the worst case is met with when both the ionization coefficients are equal [8].

2.3.7. Schottky Photodiodes

In another type of diode a junction is formed between the semiconductor and a metal. This type of junction between a metal and a semiconductor creates an asymmetric potential barrier which acts as a diode. These diodes are called Schottky diodes and can be formed by depositing one of several different metals on silicon. Each metal produces a typical barrier height Ψ_{ms}, and a corresponding cut-off wavelength for optical response. Some common schottky diodes include Pd_2Si ($\Psi_{ms} = 0.35$ eV, $\lambda_c = 3.5$ μm) and PtSi ($\Psi_{ms} = 0.22$ eV, $\lambda_c = 5.6$ μm).

The p-i-n and APDs discussed already are both pn-junction based photodetectors. In contrast the Schottky photodiode is based on metal-semiconductor junction to separate and collect the optically generated electron-hole pairs. Structure of a Schottky photodiode is illustrated in Figure 2.17. It illustrates the operation of a most commonly used metal-n-n^+ schottky photodiode. Incident photons pass through the semi-transparent metal (Au) film and are absorbed in the near-surface depleted n-type substrate. If the electron-hole pairs produced in the depletion region, are swept out by the built-in field of the depletion region, this gives rise to a photocurrent. Although the Schottky photodiode has no p layer, yet the remaining structure and its operation resembles to that of a p-i-n photodiode.

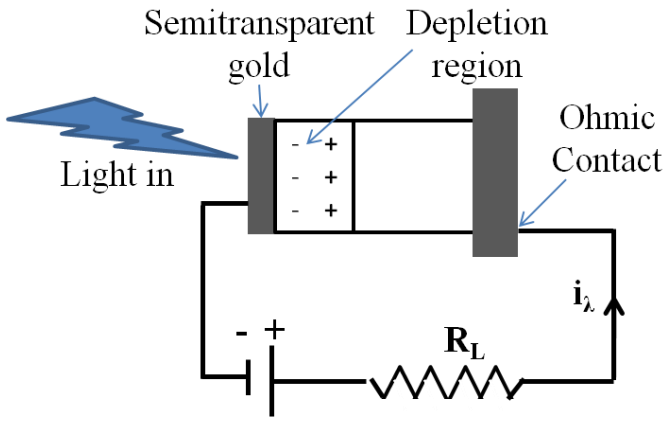

Figure 2.17: Schottky photodiode

2.4. Charge Coupled Device

When a photon is absorbed by a semiconductor detector, the released electrons and holes are free to move around in the crystal structure. CCD's are designed to store these photo-generated electrons and prevent them from wandering around the lattice. This way a pattern of electron concentration is captured at the CCD's pixels which corresponds directly to the pattern of the incident illumination or image. The corresponding electron charge pattern is then transported for read out using electronic circuits, and is finally digitized by the camera circuitry to map out an actual digital representation of the object, imaged by the CCD's sensor. Normally, CCD sensors are fabricated on Silicon wafers and are designed for charge generation, charge collection, transfer of charge, and read out. For making CCDs, approximately $10 - 20\ \mu m$ thick epitaxial layer of silicon is grown over a highly doped thick silicon substrate. Typical resistivity of the silicon wafer is less than $0.01\ \Omega - cm$ [14].

The thick silicon substrate used for this purpose is to support processing in the upper epitaxial layer, as it provides a good electrical ground for the device. The substrate is highly doped and, therefore, is not sensitive to light. This is because optically-generated electrons in the substrate region recombine quickly with the holes that are provided by the dopants. This behaviour plays an important role in achieving high charge transfer efficiency (CTE) and good spatial resolution among the pixels in a CCD sensor[2].

The performance of CCDs is dependent on a number of factors, which include the quality of silicon, impurities in semiconductor material, and lattice imperfections. The CTE mainly depends on the quality of the epitaxial layer. It is very important because CCDs are generally required to transfer very small charge packets through several inches of silicon without any loss. Thus, high quality silicon epitaxy with minimal density of defects or traps is critically important for high performance CCDs [14].

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Chapter 3

Semiconductor Light Detectors: Review

3. Introduction

pn – junction semiconductor photo-detectors were first conceived in the early 1940's. At Bell laboratories, Russel Ohl observed photo-voltaic effect when light was shining on a silicon rod. Further investigations on these observations became the basis for a silicon-based pn – junction photo-detector [1]. From this accidental invention of a pn – junction diode it took a long time to realise a practical device with similar characteristics. Gradually, it was understood that light incident on a pn – junction, results in exciting an electron to flow from the n – region to the p – region, causing a photo-voltaic effect in the diode. These pn – junction diodes were used for military applications before they were made commercially available. In 1947, J. Bardeen and Walter Brattain invented the transistor by adding another doped region to a pn – junction diode. This device was capable of controlling the flow of charge carriers. These observations i.e. the formation of an accidental pn – junction and the creation of a transistor were theoretically explained by Shockley (Shockley, pn – junction theory 1948) and these became the basis for the first semiconductor device.

Shockley published his results in the Bell system technical journal in 1949 where he also proposed the design of a possible junction transistor. Later on he materialized his research by making the device while working in collaboration with Morgan Sparks and Gordon Teal. These transistors opened up lots of new application areas in solid state electronics. In 1952 a pn – junction was set up in a single silicon crystal by dividing a single crystal into two zones of opposite impurity types. At the junction of these two zones, a small voltage exists i.e. the built-in voltage of the region depleted of charge carriers. Here, light falling on the junction may knock loose electron from one of the crystal's atoms, creating an electron-hole pair. Because of the existing voltage difference, i.e. the junction electric field, the electron is pushed one way and the hole in the other. If the zones are connected by an external circuit, a current will flow [2]. Following the successful demonstration of a pn – junction diode and a pn – junction transistor, in 1957 Robert Noyce and Kurt Lehovec used the pn – junction concept for device isolation as well.

Untill the end of 1950's, the work on photo-detectors was only carried out with elemental semiconductor materials. From early 1960's compound semiconductor materials also started to be used for the fabrication of photo-detectors. In 1976 Hunsperger et al. demonstrated a dual mode diode. In forward bias it worked as a light emitter while in reverse bias it worked as a photo-detector.

Silicon-based pn-junction photodiodes are now widely used in radiation sensing applications. The detectors are further classified according to their performance in specific spectral regions, and based on the semiconductor material used for their fabrication, and lastly on the basis of the operating mechanism of the detector. Silicon covers the visible and near-IR region of the EM spectrum. Silicon detectors are good for radiation detection in the near-IR region, whereas in the short wavelength, blue and UV region, their performance degrades. UV detectors have gained interest due to their widespread usage in defence, environment and medical applications [3]. These are usually made from wide band-gap semiconductors such as gallium nitride or silicon carbide.

The spectral range for UV light covers 400 nm - 100 nm and reaches into the soft X-ray spectral region. This UV spectral range is further divided into four regions, namely UV – A (400 – 320 nm), UV – B (320 – 280 nm), UV – C (280 – 200 nm) and Far – UV (200 – 100

nm). UV detectors are used in several applications like emitter calibrations, flame sensors, spatial optical communications and as biological and chemical sensors. These applications include solar UV measurements, astronomical studies, missile plume detection, combustion engine control, spatial optical secure satellite communications, ozone detection, pollution and biological agent detection.

Initially, photomultiplier tubes were used to detect UV light [4]. Advancements in semiconductor technology, established that semiconductor-based UV photodetectors are more reliable and can be fabricated to be much smaller in size than photomultiplier tubes. These detectors include photoconductors, Schottky photodiodes and p-i-n photodiodes.

Semiconductor photodiodes primarily designed for visible spectral range have also been tested in the vacuum-ultra-violet (VUV) spectral region. Silicon-based photodiodes show drastic decrease in spectral responsivity in this region. Gallium phosphide and Gallium Arsenide phosphide Schottky diodes have shown excellent stability and high quantum efficiency. These Schottky diodes are therefore suitable alternatives in the VUV spectral region [5].

3.1 Silicon-based Photodetectors

Semiconductor detectors can be classified into three categories based on their operating mechanism. These are photoconductive detectors, pn-junction photodetectors and Schottky barrier detectors. Their operating mechanism has already been explained in Chapter 2. Silicon-based photodetectors are generally used for detecting in the visible spectral range, and are a cheap solution for detecting radiation from 400 nm to 1100 nm range. Silicon can also be used for detecting UV radiation. For UV radiation detection a distinct structural arrangement and a specific fabrication process is needed to fabricate such short wavelength-sensitive detectors.

Conventional pn-junction silicon photodiodes are less sensitive to UV radiations. This is because high energy photons are absorbed mostly in a very thin top surface layer. 350 nm to 200 nm UV photons are practically absorbed within less than 10 nm length, this results in the loss of photo-generated charge carriers due to surface recombination in conventional photodiodes. In diffused photodiodes, photo-generated charge carriers are also lost by recombination in the defect and trap centres introduced during the diffusion process.

Spectral sensitivity of the most widely used silicon detectors varies rapidly with UV radiation. Factors like multiple ionization and recombination effects degrade the performance of the detector [6]. Therefore, it becomes difficult to maintain the quantum efficiency with UV radiation. To address these performance issues with UV detection, a high pass optical absorbent filter is commonly used to adjust the spectral range as per the targeted application, and a phosphor coating is used for wavelength conversion to increase the life time of the device. Resultantly, the manufacturing cost of the device increases. L. R. Canfield et al. [7] indicated that UV sensitivity of silicon photodiode can be controlled by the quality and careful handling of $Si - SiO_2$ interface.

A UV-sensitive silicon photo-detector and a photo field effect transistor (photo-FET) were reported by Von Muench et al. in 1976 [8]. They demonstrated high UV sensitivity using a special boron diffusion process to make a very thin top p layer in order to make the silicon sensitive to such short wavelength photons. A thin and patterned, dry SiO_2 layer was used to control the surface acceptor concentration of boron atoms and the diffusion depth. The surface area covered with dry SiO_2 resulted in shallow diffusion whereas the un-covered areas i.e. without SiO_2 ended up with deep impurity diffusion. This resulted in shallow and deep diffusion profiles at selective surface locations. The junction was formed at a depth of 200 nm and exhibited responsivity of 0.1 A/W at 253 nm wavelength. Furthermore, this boron-doped UV photodiode gave superior response especially in the 190 nm to 250 nm spectral range.

In 1979, Ouchi and colleagues carried out experimental studies with a silicon $pn-$ junction diode [9]. Their aims were to make a photodiode sensitive to UV spectral region with low dark current, high reliability and reduced responsivity to visible radiation. Unlike the thin dry oxide layer approach described by Von Muench et al. for shallow diffusion, Ouchi used the approach of controlled sheet resistance to control the junction depth. The sheet resistance decreases linearly with increase in diffusion temperature. The experimental results showed that 0.15 μm junction depth was achieved at 800 ℃ diffusion temperature.

An n-type silicon wafer was used to fabricate the photodiode. A guard ring fabricated in the device structure was kept at large junction depth to reduce the possibility of junction breakdown. The heavily doped channel stop region helps in controlling leakage current at the

$Si - SiO_2$ interface. For reduced responsivity in the long wavelength region two different architectures of photodiode were fabricated which are discussed below.

The top diffusion layer, in which a built-in field was induced by the impurity gradient, was optimized for values of sheet resistance in the range of 800-2000 Ω/□. The device responded to wavelengths in the range of 200 nm to 1000 nm and showed responsivity of 0.065 A/W at 200 nm wavelength. The $p^+ - n - p^+$ device exhibited high reliability with exposure to high energy photons, and reduced responsivity in the long wavelength part of the spectrum than the $p^+ - n - n^+$ device architecture. The device was designed with an extended electrode, which helped in preventing silicon surface degradation as a result of UV exposure. The device showed little degradation after 1000 hours of exposure to short wavelength photons. The $p^+ - n - p^+$ device architecture also helped in reducing stray light effects in spectroscopic measurements.

Korde et al. fabricated three different UV-sensitive photodiode structures, (1) n on p type photodiode i.e. phosphorous doped, (2) p on n-type photodiode i.e. boron-doped and (3) natural inversion layer type photodiode [7, 10-12]. A 60 nm thick dry SiO_2 layer was thermally grown at the top surface. The same process was repeated with boron diffusion on n-type substrate. It appears that donor impurities like phosphorous or arsenic tend to pile up near the silicon surface during thermal oxidation, forming a built in electric field near the $Si - SiO_2$ interface. This oxide thickness absorbed all the radiation up to 120 nm, making this detector unsuitable for high energy UV photons such as those from the vacuum UV spectral region. Here the authors have described 100% internal quantum efficiency for the wavelength range from 350 to 600 nm, whereas the internal quantum efficiency was larger than unity for wavelengths shorter than 350 nm. This mainly arises due to secondary impact ionization phenomenon.

To characterise the inversion layer photodiode [11, 12] natural n-type inversion layer produced near the thermally-oxidized p-type silicon surface, due to fixed surface state charge is made use of. These fixed positive charges are due to excess silicon ions in a narrow region next to the silicon surface i.e. SiO_2. The charge inversion photodiodes appeared to be similar to MOS structures designed for FET applications. The photo-detection process was mainly influenced by the inversion field induced at the surface near the $Si - SiO_2$ interface [13]. The

strong electric field due to the inversion layer was established near the surface of the photodetector where incident high energy UV photons were likely to be absorbed. As the depletion region was formed close to the surface i.e. at the Oxide-silicon interface, it helped in collecting the charge carriers produced due to the absorption of short wavelength UV photons, thereby enhancing the internal quantum efficiency in the 250 to 500 nm spectral range with a cut-off wavelength of 120 nm. The reason for this, as already discussed, was the absorption of high energy photons by the layer. Disadvantage associated with this photodetector was its high sheet resistance in the inversion layer which caused slow response times.

Both the diffused photodiodes p-on-n and n-on-p, were fabricated with similar processes. However, based on the device response, Korde et al. concluded that n-on-p photodiodes were more stable in the UV spectral region than the p-on-n photodiodes. However, stable p-on-n devices can also be produced with adequate care. Fragile $Si - SiO_2$ interface made it difficult to eliminate the recombination states at the interface and to prevent these states from reforming due to environmental stresses. The presence of the diffused inversion layer on p-type photodiodes i.e. n-on-p and inversion layer devices, minimizes the time that photo-generated minority carriers spend near the interface. This considerably reduced the sensitivity of these devices. Boron-doped devices i.e. p-on-n photodiodes were sensitive to moisture unlike the other two devices. Therefore, growth of dry oxide in ultra clean and dry environment made the n-on-p device relatively stable for UV exposure. Whereas, in the case of the inversion layer device, the stability of the trap centres in the oxide layer prevented the loss of linearity over the UV range.

In 1989 R.F. Wolffenbuttel [14] demonstrated an electrically programmable spectral filter using a silicon photodiode which could be tuned to attain high UV sensitivity. High surface absorption of UV / blue short wavelength photons was seen in silicon photodiodes. A special programmable biasing technique was used for selective detection in the spectral region of choice. Wolffenbuttel used a special biasing arrangement for the detection of selective optically-generated free charge carriers in the space charge region. The width of the space charge region was controlled by reverse bias arrangement, as is usual with photodiodes. Measurement results confirmed the effectiveness of this reverse biasing arrangement i.e. electronic control for detection in the UV-B region. This enhanced operation of a photodiode

in the short wavelength region with electronic control may become the basis of programmable silicon colour filters.

Schottky barrier UV photodiodes have been fabricated using a variety of semiconductor materials. K. Solt et al. reported surface-illuminated $(PtSi - n - Si)$ silicon Schottky barrier photodiodes for vacuum UV spectral region [15]. These Schottky diodes were fabricated using n-type 25 $\Omega - cm$ silicon wafers. Contacts and guard ring diffusion were done using ion-implantation. The platinum was deposited using magnetron sputtering in a high vacuum system. The silicide was formed $in\ situ$ after deposition by annealing at 500 ℃. The resulting less than 10 nm thick films were partially epitaxied to the silicon forming an abrupt, contamination free, laterally uniform interface between PtSi film and the silicon substrate. The photodiode showed 0.03 A/W responsivity for the spectral region below 250 nm. This value was comparable to the reported responsivity values for GaAsP Schottky photodiodes. The PtSi-n-Si diode showed spatially uniform and virtually stable response after long exposure to VUV radiation at 120 nm wavelength. The diode response made it a promising choice for use as photon detectors for satellite-based UV and VUV astronomy. These diodes can also be used in front-illuminated short wavelength sensitive CCD arrays.

3.1.1 Silicon Carbide UV Photodetectors

Silicon carbide has special properties that make it suitable for making UV detectors. It has a high breakdown field that results in much smaller drift regions i.e. lower drift region resistance. Higher thermal conductivity in SiC allows heat to dissipate quickly and a wide band-gap (2.9 eV) endows it with extreme radiation hardness in the UV spectral region. Furthermore, UV photodiodes made with SiC are visible blind. These properties make SiC a suitable material for making detectors for the UV or VUV regions [12].

The best SiC UV photodiodes were made by the diffusion of Al into n-type substrates. The diffusion at 2000 ℃ results in structural decomposition of the surface layer and, therefore, the devices showed high leakage current and low quantum efficiency [16]. An improved design proposed by Glassow et al. made use of a 5 μm p-type epitaxial layer grown on a p-type substrate. The authors utilized n-implantation to form a very shallow $n^+ - p$ junction in the epitaxial layer. To activate the implanted nitrogen, furnace annealing and rapid thermal

annealing techniques were used. The fabricated devices exhibited 75% quantum efficiency at a peak wavelength of 280 nm at room temperature. The diode showed high leakage current of the order of 10^{-5} A/cm^2 at -10 V. This is because sintering the contact at high temperature diffused the contact metal to n^+ layer through the crystal defects causing increased diode leakage current.

Anikin et al. reported a realization of high quality Schottky junctions on SiC(n). The authors fabricated two sets of 6H – SiC UV photodiodes, one using Schottky junctions while the other was based on shallow pn-junctions [17]. The author's work relied on Au-SiC barrier technology, which the authors had developed earlier. The Schottky junction had an area of $3\ x\ 10^{-3}\ cm^2$. The Au-SiC barrier showed low leakage current of the order of $\sim 10^{-10}$ A, up to the breakdown voltage of 100 – 170 V at room temperature, whereas at 573 K the leakage current reached $\sim 10^{-8}$ A. The pn-junction structure had an area of $1.7\ x\ 10^{-2}\ cm^2$ and produced a leakage current of 10^{-12} A at 1 V reverse bias. The spectral sensitivity of Schottky barriers and shallow pn-junctions were 0.15 A/W at $\lambda = 215$ nm and 0.13 A/W for $\lambda = 225$ nm, respectively. Both SiC-based diodes showed high sensitivity to UV radiation with low leakage current and, therefore, could be used for UV detection even at higher temperatures.

4H-SiC vertical Schottky photodiodes have been reported by Feng et al. They used 2 inch wafers based on n-SiC epilayers grown over n^+ SiC substrate [18]. A semitransparent 7.5 nm thick Schottky contact was deposited over an SiO_2/Si_3N_4 dielectric layer. The photodiodes showed extremely low leakage current at -1 V bias. Furthermore, the diodes showed 37% quantum efficiency in the 240 to 300 nm wavelength range. They also showed high detectivity over 10^{15} cm. Hz$^{1/2}$. W^{-1} in the 210 to 350 nm spectral range with a peak detectivity of $3.6\ x\ 10^{15}$ cm. Hz$^{1/2}$. W^{-1} at 300 nm wavelength.

So far, state of the art silicon and SiC-based photodetectors reported in the literature have been discussed, whereas industries like automotive, aerospace, oil exploration and others demand highly reliable and technologically advanced UV detectors, which are resistant to high temperatures and are suitable for adverse conditions. New generation of UV detectors are mainly fabricated using wide band-gap semiconductors – the most promising are diamond and AlGaN [12]. Recent developments in the diamond-based UV photodetector were the basis for

the realization of short cutoff wavelength photoconductors ($\lambda_c = 225\,nm$). They also show high contrast to UV and visible part of the spectrum [19, 20] and thus were useful for applications requiring visible UV and highly energetic particles detection. Diamond due to its radiation-hardness property, remains resistant to high energy particles.

Until the early 80's, thermal diffusion was used to add dopants to semiconductor materials. Thermally diffused impurities caused higher leakage current and, therefore, higher noise. Replacement of diffusion technique by ion implantation reduced the leakage current by three orders of magnitude i.e. from $\mu A/cm^2$ leakage to nA/cm^2 [21]. Ion implantation technique produces a very shallow heavily $p-$doped top layer resulting in enhancement in sensitivity of pn and $p-i-n$ diodes to the blue spectral region. This is due to dosage precision and better command over the impurity diffusion profile by ion implantation technique. Further research in fabrication techniques has improved the diffusion process as well. C. Z. Shou and W. K. Warburton, while comparing thermal diffusion and ion implantation processes, devised a technique that yields less leakage current with thermal diffusion than with ion implantation. They used high resistivity n-type silicon wafers, the large leakage current as a result of boron diffusion, was considerably reduced (by about a factor of 2) by adding a boron skin removal step, following the thermal diffusion process. The boron-doped layer, formed a brown coloured skin, which was hard to remove using acid etching. However, by using wet oxidation, the boron skin was converted into borosilicate glass, which could then be removed using plasma dry etching. It is believed that thermal diffusion causes less lattice damage than ion implantation process. The only drawback with the new technique was the additional fabrication processing required [22].

Ciftcioglu and colleagues [23] demonstrated an integrated silicon $p-i-n$ photodiode using a deep $n-$Well in a standard $0.18-\mu m$ CMOS technology. This p-i-n photodiode showed a 2.2 GHz bandwidth response at 850 nm wavelength, as against the 1.15 GHz and 0.94 GHz response of vertical and lateral p-i-n photodiodes, respectively. The responsivity of the photodiode was approximately 0.14 A/W up to 10 V of bias. Furthermore, at 15.5 V bias, the bandwidth response of new photodiode reached up to 3.13 GHz. Responsivity of this photodiode could be increased up to 0.4 A/W when operating in the avalanche region at 16.2 V bias.

3.1.2 Metal-semiconductor-metal Photodiodes

Metal-semiconductor-metal (MSM) silicon photodetectors suitable for near-IR (800–900 nm) spectral range exhibit low responsivity. This is caused by the small absorption coefficient of near-IR spectrum in silicon. M. Y. Liu. et al. [24] demonstrated the first reported 510 GHz MSM photodiode using GaAs and 110 GHz photodiode on bulk silicon. The response time was dependent on the wavelength of incident light, i.e. a shorter response time for short wavelength radiations and a relatively slow response for long wavelength radiations. GaAs based MSM photodiodes also showed reduced bandwidth of 40 GHz at long wavelengths. To address this issue, the authors demonstrated a silicon-on-insulator SOI photodiode which showed 140 GHz bandwidth. The unique device structure stopped carriers generation deep inside the semiconductor substrate, causing the detector response to be independent of the incident radiation's wavelength. Here the substrate structure separates the top scaled silicon layer from the bulk silicon using a buried oxide layer. This structure had many advantages over the previous reported devices. The detector response became independent of the incident wavelength, the device had smaller capacitance and the results showed its possible use in high speed nano-scale FET applications. The device showed $0.2\,\mathrm{pA}/\mu\mathrm{m}^2$ dark current. The top epitaxial silicon layer was p-type with a doping concentration of $10^{15}\ \mathrm{cm}^{-3}$ and was thinned down to 100 nm using oxidation and wet etching techniques. 100 nm interdigitated electrodes were fabricated using electron-beam lithography and lift-off techniques. The device with 100 nm top scaled silicon layer, showed responsivity of 5.7 mA/W at 780 nm and 12 mA/W at 633 nm. This low responsivity was caused mainly by the thin active top silicon layer.

The authors predicted that if the finger spacing was reduced from 100 nm to 25 nm the silicon-on-insulator metal-semiconductor-metal photodiode could have response time as small as 1 ps and a bandwidth as high as 400 GHz. This would certainly need to reduce the thickness of the active silicon layer over the buried oxide, and would show a high speed at the expense of low responsivity. This tradeoff between responsivity and speed can be avoided using a number of different methods. One such technique was proposed by Lee and Zeghbroeck where they proposed a novel silicon MSM photodetector fabricated on a textured silicon membrane [25]. This membrane ensured that the carriers were generated within the active region only. Scattering at the textured membrane surface increased the average path length between the top and bottom surface of the membrane, whereas trapping of light in the thin membrane caused

minimal reduction in responsivity, while reducing the transit time of the carriers. Another method was proposed by Ho and Wong [26] utilizing a trench structure using SOI wafer. They obtained 19% efficiency at 790 nm at a bandwidth of 2.3 GHz.

J. D. Schaub et al. in 1999, fabricated and tested a resonant-cavity-enhanced high-speed silicon p-i-n photodiode grown by epitaxial lateral overgrowth. This device exceeded 34 GHz bandwidth with 2.7 pA dark current at 5 V reverse bias. Higher values of quantum efficiency were reported ranging from 42% to 31% at 704 nm and 836 nm wavelengths, respectively. The product of bandwidth and efficiency was among the state of the art silicon p-i-n photodiode [27].

Vertical p-i-n photodiodes have limitations in optical communication at 850 nm wavelength. This is due to deep optical absorption at 850 nm wavelength and the carrier transit distance in silicon [28]. Lateral p-i-n photodiodes where the pn-junction is formed through either ion-implantation [29] or diffusion [30] and interdigitated metal-semiconductor-metal photodetectors [31] face absorption layer thickness limitations. The devices based on thin SOI material had also shown decrease in responsivity [24] although a very high bandwidth was reported. Silicon detectors based on resonant-cavity enhancement [27] have shown both high speed and responsivity. The resonant-cavity, however, induces undesired wavelength selectivity.

Yet another high-speed, high-sensitivity silicon lateral trench photodetector, capable of decoupling the carrier transit distance from the light absorption depth was reported by Min Yang et al. [32]. This structure was capable of both high speed and high responsivity. External quantum efficiency was reported to be 68% at 845 nm wavelength. The wire-bonded lateral trench detector and a BiCMOS transimpedance amplifier together demonstrated 2.5 Gb/s data transfer rate at 845 nm wavelength, with 3.3 V applied bias.

3.1.3 Avalanche photodiodes

Silicon avalanche photodiodes (APD) provide internal gain, amplifying weak optical inputs. APDs have inherent charge multiplication which causes signal enhancement. The ionization rate for electrons is higher than that for holes, causing higher gain and lower noise when compared with other types of silicon detectors with no internal gain mechanism [33, 34].

In 2002, Rochas and colleagues fabricated a CMOS-compatible APD which showed high sensitivity to UV / blue radiation [35]. The photodiode was fabricated in a twin tub with a guard-ring structure formed through laterally diffused n-well regions. The lateral diffusion of two n-wells designed at a small distance "d" apart is advantageous in making two guard-rings without any additional processing. The photodiode showed a very small dark current which was nearly 400 $\mathrm{pA/mm^2}$. The approach used by the authors was discussed in [36].

Though $\mathrm{p-i-n}$ diodes are suitable for high speed operations and their sensitivity is better than $\mathrm{pn-junction}$ diodes, further advancements in the APDs have resulted in devices that can detect a single photon. E. Sciacca. demonstrated a single photon APD (SPAD) in planar technology, suitable for monolithic integration of SPAD [37].

3.2 Lateral pn-Junction Photodiodes

Tsutsui and colleagues developed an analytical model in 2001 for "QW lateral $\mathrm{pn-junction}$ photodiode", [38]. This lateral $\mathrm{pn-junction}$ photodiode model ensured low capacitance and short transit time and thus could operate at higher signal frequencies. This model was based on the assumption that the electron-hole movement is due to drift-diffusion process. The authors showed that the combination of short carrier transit time and very low capacitance in lateral $\mathrm{pn-junction}$ photodiodes provide significant advantages over other photodiodes like metal-semiconductor-metal (MSM) photodetectors [39-41] and lateral $\mathrm{p-i-n}$ junction photodetectors [42, 43].

3.3 Gated pn-junction Photodiodes

A new silicon-based gate-controlled vertical $\mathrm{pn-junction}$ photodetector was described by Sun et al. [44]. The gated part of $\mathrm{pn-junction}$ diode modulated its external quantum efficiency and photocurrent and controlled the depletion layer depth.

The gate-controlled vertical pn-junction photodiode was fabricated using n-type phosphorous-doped silicon substrate with doping concentration, $\mathrm{N_D = 1\,x\,10^{19}\,cm^{-3}}$ and a resistivity of $0.006\,\Omega-\mathrm{cm}$. It was based on a pn-junction diode whose surface was covered with a metal electrode. The transparent polysilicon MOS gate was vertically aligned to the p-doped region such that with negative biasing on the gate an inverted channel would form under the MOS

gate. This inversion layer and n type silicon formed a depletion region under the MOS gate. Here the width of the depletion region was controlled through the applied gate-bias. The advantage of this structure was that the gate-bias-induced depletion region got interconnected with the pn-junction depletion region. The function of the pn-junction depletion region was to collect the charge carriers which form the photocurrent. Upon illumination, short wavelength photons were absorbed within the depletion width i.e. the depletion region under the transparent gate. Long wavelength photons were absorbed outside the depletion region deep into the substrate and thus did not contribute to photocurrent. The photocurrent was proportional to the product of gate voltage and light intensity in linear region only. The photo-generated electrons drift towards the grounded substrate whereas the holes transfer in the transverse direction parallel to the semiconductor-oxide interface towards the pn-junction. Holes which successfully reached the pn-junction contributed to photo current. Unlike conventional photodiodes, here diffusion was the dominant mechanism and possibly slowed down the device response. To address this issue a special device structure was investigated using a stepped-oxide-thickness gate to increase the transverse electric field whereas an epitaxial structure and n^+ ring were used to reduce the series resistance.

Another transistor, based on gated vertical $p-i-n$ structures for purely electronic applications, has been described by Bhuwalka et al. [45]. They demonstrated a three terminal p-i-n diode which could be operated with a reverse bias for optical detection. When the gate was biased with a positive voltage with respect to the source, p^+ and n^+ tunnel junctions were formed between the heavily p-doped source and the inverted channel. The gate bias, therefore, controlled the tunnelling width and the tunnelling current. The device performance was further improved using gate work function engineering and band-gap modulation at the tunnel junction.

It is clear from the past research that the location of the depletion region is vitally important for short wavelength radiation detection applications. The vertical, gated junction diodes have depletion regions buried inside the semiconductor surface, whereas in the gated lateral junction diodes, the depletion region starts right from the top surface, which can be utilized in many novel applications.

Furthermore, the fixed architecture of diode-based detectors, is a source of inflexibility in that their operating characteristics cannot be changed once these devices have been incorporated in a circuit. The bipolar junction photo-transistor can be used in such situations as its base terminal, when properly utilized, can be used to adjust its operating parameters. However, as most integrated circuits are based on MOSFETs so a bipolar transistor device does not fit very well into the overall circuit design philosophy. A hybrid device can be a suitable solution to this problem - a device that has features of both pn-junction diodes and MOSFETs.

The concept of a silicon-on-insulator-based lateral p-i-n photodiode with transparent gate has been discussed by Zeng Yun et al. in a recent publication [46]. The authors have presented a physical model which was based on standard semiconductor equations. Their analytical model described a lateral device with high sensitivity and signal to noise ratio, together with low dark current. Using this model, the photoelectric characteristics of lateral p-i-n gated photodiode could be optimized. The proposed device would operate as a p-i-n junction photodiode but it also incorporates a transparent insulated gate to control the electrical aspects of its operation. The resulting device detects light through pn-junction mediated charge carrier separation and appears as a MOSFET for the purpose of circuit design.

It should be pointed out here that a gated phototransistor was reported by Kang et al. in the context of metamorphic high-electron-mobility transistors a few years ago [47]. However, their device was a back-illuminated compound semiconductor device with characteristics too different from that of transistors and thus was not compatible with silicon-based integration. A gated light-sensing heterostructure FET was also described by Taylor and Simmons many years ago [48]. Yet another phototransistor based on indium phosphide structures was described recently by Zhenghua An and colleagues which operated with a photo-emissive gate [49].

3.4 Black Silicon

Silicon-based devices are commonly used in optoelectronic and microelectronic industries. It has a crucial disadvantage that limits its use in optical communications. The two primary wavelengths used for optical communications are $1300\ \text{nm}$ and $1550\ \text{nm}$. These fall beyond the spectral detection capability of silicon i.e. beyond $1100\ \text{nm}$. Therefore, normal silicon cannot be used in optical communications. However, silicon could be made sensitive to

wavelengths suitable for optical communications. This is done in a process where gases pass over the silicon surface, react with the top layer and finally form a so-called black silicon layer on top of normal silicon. Black silicon formation reduces surface reflection and traps light thereby increasing the sensitivity of silicon to longer wavelengths [50].

Black silicon is a promising new material for enhancing the sensitivity of silicon for infrared detection. Photo-detectors fabricated with black silicon are very sensitive to near infrared (NIR) and short wavelength infra-red (SWIR) regions. It is generally found that black silicon improves the wavelength response considerably to which silicon is normally sensitive i.e. black silicon has enhanced IR sensing capability, as shown in Figure 3.1. For making black silicon, the photoconductive and absorptive properties of normal silicon are changed using a short pulse femtosecond laser. This material is formed through, the irradiation of silicon with an ultra fast laser in a sulfer hexafluoride environment. As a result, black silicon is formed with a highly doped, nano-structured surface layer. This layer exhibits photoconductive gain and enhanced infrared absorption at room temperature. Its response exceeds as compared to that of a standard silicon photodiode in visible and near infrared regions and is competitive with InGaAa and germanium response in SWIR region [50].

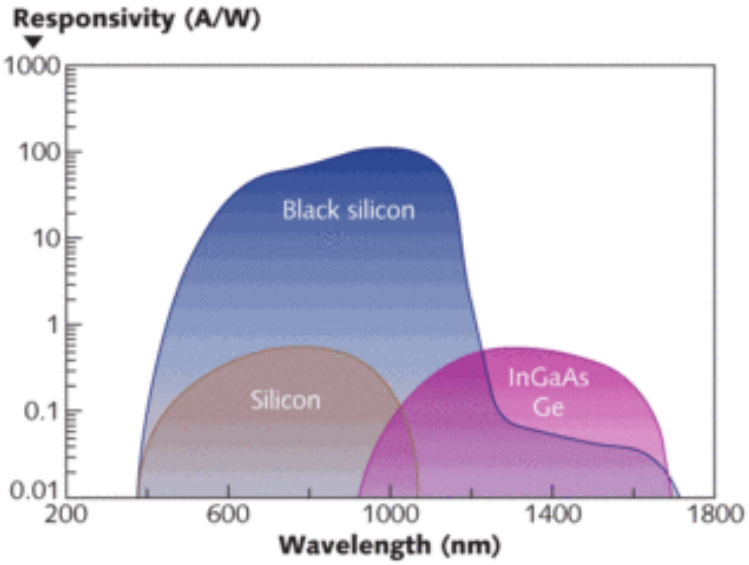

Figure 3.1: The responsivity of a black-silicon detector [50].
Compared to that of ordinary Silicon and InGaAs detectors.

First photodetectors fabricated using black silicon showed high photoconductive gain at room temperature, where the responsivity reached 100 A/W in the near infrared region. The

magnitude of signal produced with each photon is nearly equal to that with a silicon avalanche photodiode (APD). However, this is achieved without the added complexity of high voltage and protection circuitry as required with traditional avalanche photodiodes.

Improved signal strength from high photoconductive gain reduces the burden of signal processing by downstream electronics. The absorption properties of silicon are also tailored as a result of femtosecond-laser processing. The combination of increased optical path length and defect engineering enable black silicon to radically reduce the amount of silicon needed to absorb NIR and SWIR light. This allows silicon to detect optical communication wavelengths. Aoife and colleagues [51] have presented novel black silicon $p-i-n$ photodiodes of various sizes. These photodiodes were characterized for all parameters and were compared with similar-sized photodiodes made on the same silicon wafer, which was used to make black silicon. A p-i-n photodiode fabricated with black silicon has shown, more than 50% increase in responsivity as compared to normal p-i-n silicon photodiode.

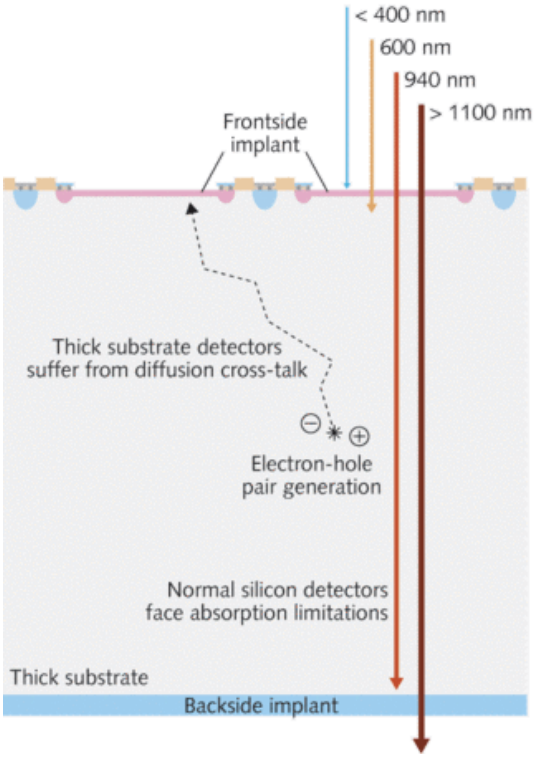

Figure 3.2: .The absorption depth in standard silicon detectors [50].

In normal silicon-based CMOS imagers the absorption depth of photons is quite large in the near-IR region. As a result most of the light just travels through the detector as if it was a transparent material. For this reasons, the CMOS imager uses no less than 10 μm of silicon in

the “receptive region”. High performance charge-coupled devices (CCDs) have a very thick sensing zone, however, it still appears transparent to wavelengths in the SWIR region. (λ >1100 nm) as illustrated in Figure 3.2. Therefore, use of black silicon to fabricate a detector would result in reduced absorption depth for NIR and SWIR light. In black silicon, electron-hole pairs are produced within a thickness that is similar to that of the silicon used in CMOS devices. High efficiency, photoconductive gain and increased absorption are the benefits of black silicon as a detector material [50].

Black silicon is being used in digital night vision applications and in the medical and defence fields where detectors made from black silicon have shown improved results as compared to normal silicon detectors.

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Chapter 4

Device Fabrication Techniques

4 Introduction

This chapter contains a description of the silicon material used for device fabrication, techniques in processing of CMOS-based Surface Gated Photo-detectors (SGPD) and the basic design of these gated photo-detectors. Silicon is the most widely studied material in the world. It is either available in its pure un-doped high resistivity form or, more commonly, doped with impurity atoms which make it n or p type. This adjustment of dopants is critical to device operation. The device fabrication part of this chapter deals with the fabrication techniques used in processing the SGPDs. These are cleaning, oxidation, patterning, etching, diffusion and metallization. The fabrication process is summarized with illustrations to explain the sequence of fabrication. Later part of this chapter deals with the variations in the structure of SGPDs. One set of devices deals with single gate photo-detectors with variations in dimension and placement of gate, whereas the second deals with dual gate architectures. A very brief overview of the fabrication is given to highlight the variation in SGPDs. Further details of these variations are given in single and dual gate device chapters, respectively.

4.1 Material for Device Fabrication

Optoelectronic devices transform electrical signals into optical radiation or vice versa and thus can be categorized as light sensing or light emitting devices. Phototransistors, charge-coupled devices (CCDs) and photodiodes are examples of light sensing devices, whereas lasers and light emitting diodes (LEDs) fall into the light emitter category. The gated lateral p-i-n photodiode described here detects light through $\mathrm{pn-junction}$ mediated charge carrier separation. In pn or $\mathrm{p-i-n\ junction}$ photo-detectors the electric field in the depletion layer, separates the electron-hole pairs generated through photon absorption. Use of the semiconductor material critically determines the spectral range over which the photo-detector operates. Silicon based lateral p-i-n photodiodes are suitable for 400 nm to 1100 nm range of electromagnetic (EM) spectrum. Conventional photodiodes with vertical doping profile appear transparent to long wavelength radiations, whereas short wavelength radiations are essentially absorbed at the surface even before the depletion region is encountered. In this region minority carriers have a very short diffusion length thus they recombine with majority carriers and do not contribute to output current. In order to address this issue, we fabricated the lateral surface gated photo-detectors where the depletion region starts right from the top. The lateral surface gated photo-detector was fabricated using $\mathrm{p-type}$ Float Zone (FZ) silicon wafers. The float zone (FZ) wafer was lightly boron doped with $< 100 >$ crystal orientation. It had a high resistivity of $4\ \mathrm{K\Omega-cm}$. Properties of silicon are shown below in Table 4.1.

Crystal structure	**Diamond**
Number of atoms in 1 $\mathrm{cm^3}$	5×10^{22}
Energy gap	1.12 eV
Energy separation (ΕΓL)	4.2 eV
Intrinsic carrier concentration	$1 \times 10^{10}\ \mathrm{cm^{-3}}$
Intrinsic resistivity	$3.2 \times 10^{5}\ \Omega \cdot \mathrm{cm}$
Effective conduction band density of states	$3.2 \times 10^{19}\ \mathrm{cm^{-3}}$
Effective valence band density of states	$1.8 \times 10^{19}\ \mathrm{cm^{-3}}$
Breakdown field	$\approx 3 \times 10^{5}\ \mathrm{V/cm}$
Mobility electrons	$\leq 1400\ \mathrm{cm^2\ V^{-1}s^{-1}}$
Mobility holes	$\leq 450\ \mathrm{cm^2\ V^{-1}s^{-1}}$

Dielectric constant (static)	11.7 at 300 K
Infrared refractive index n(λ)	n = 3.42 at 300 K

Table 4.1: Properties of Silicon.

4.2 General Considerations

Semiconductor devices are fabricated in thin material slices called wafers. Wafers, in semiconductor terminology, are also referred to as substrates. The fabrication process ends with hundreds of tiny devices on a single substrate. With the advent of micro and nano technology, the device size keeps on shrinking. This helps in making fast nano scale devices. This way better performance is achieved whereas the device requires low power to operate. Micro and nano scale device processing requires clean fabrication environment and apart from this cleaning of the substrate is also of immense importance.

Adherence to a good cleaning process ensures removal of impurities and residues from the substrate. The substrate, in cleaning solvents, is placed in an ultrasonic bath in a series of steps, where impurities and residual matter are removed from the substrate surface. Opticlear, Acetone, Methanol, and RO water are generally used as cleaning solvents. In MOS structure fabrication, the cleaning process is followed by thermal oxide growth.

In MOS structures, an oxide layer is sandwiched between the metal and the semiconductor. This thin layer can be added over the substrate either by an oxide growth technique or by a deposition process. Use of the appropriate technique depends upon the specific needs and requirements of the device structure, temperature limitations and the precision required in the thickness of the oxide layer. Once formed, the oxide layer can be patterned using lithography techniques.

At the patterning stage, device patterns are created over a thin layer of resist using lithography techniques. General lithography techniques used for patterning are photolithography or electron beam lithography. Following the UV or electron beam exposure the sample is developed in a developer solution. The pattern can now be seen in the thin resist layer. The oxide layer can next be etched using a suitable etching technique. The patterned resist layer is used to transfer the resist pattern into the oxide layer. Patterned oxide layer can be used for selective diffusion process or to form the contacts.

A thin layer of dopants, using spin-on-glass (SOG) technique, is produced over the patterned oxide layer. This patterned oxide layer acts as a barrier layer for selective diffusion. The substrate is then soft baked over a hotplate to dehydrate the SOG layer before it undergoes heat treatment in a furnace at 1135 ℃. This step diffuses the impurity layer into the bare silicon surface. The diffusion occurs in an environment where a gas or a mixture of gases passes through the furnace at a specific temperature and pressure. Heat treatment is also needed after metallization to anneal the contacts. This thermal annealing process requires far less temperature than oxidation or diffusion processes [1]. In this chapter fabrication processes are discussed with particular focus on lateral gated diode fabrication.

4.3 Fabrication of Lateral p-i-n Photodiode

Here the fabrication process is illustrated in a self explanatory way. This starts with the silicon dry etch process to form the photolithography markers and device isolation patterns, followed by dry oxidation, selective wet etching and thermal diffusion processes. It further moves on to explain the growth of gate dielectric, formation of metal contacts and the subsequent lift off processes. Here similarities in fabrication process of all variations of the device are highlighted. Finally, emphasise is given to explain the variation in dimension and placement of MOS gate structure in single and dual gate devices.

4.3.1 Process Flow

The process flow explains the sequence of device fabrication. Dry etching of silicon is carried out as the very first step after cleaning the substrate and subsequent patterning of resist layer to form the pattern for dry etch. In Figure 4.1 (a) to (d) the process is illustrated. Here cleaning of the sample and resist spinning is shown in (a), patterning of resist layer using mask aligner is presented in (b), dry etch of silicon using STS-ICP with SF_6/C_4F_8 gases shown in (c). Here red colour has been used for $S1818$ photo-resist and the white pattern represents developed resist layer as shown in (b). Finally in (d) the resist layer is removed and the etched pattern in silicon persists.

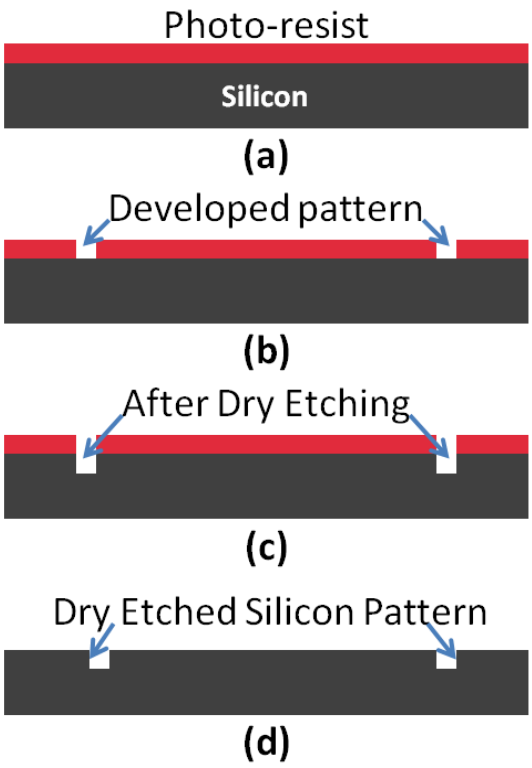


Figure 4.1: Sequence of process explaining Silicon Dry etch.

4.3.1.1 Oxidation and Diffusion

Oxidation and diffusion processes are shown in Figure 4.2 and Figure 4.3. Here in (c) light blue layer is the thermally grown oxide layer and the red layer is for $S1818$ photo resist. A $250\ nm$ thick layer of thermally grown dry oxide as shown in (b) was formed at $1135^{o}\ C$. This oxide layer was patterned for selective p and n diffusions in two separate steps. Each diffusion process (a to h refer to n type diffusion and i to p refer to p type diffusion) was followed by wet etch with 40% HF to clear off the silica layer primarily patterned for diffusion. Figure 4.2 (g) and Figure 4.3(o) show layers of n and p type dopants using spin-on-glass (SOG) material. Here in Figure 4.3 (p) the cross-section of device isolation pattern and selectively diffused p and n regions are shown. The solid fill blue and orange colour near the top surface of silicon correspond to p and n doped regions, whereas the solid fill blue colour at the bottom of the silicon substrate represents bulk p doped region. These regions of higher impurity concentration serve as p and n contacts of the diode.

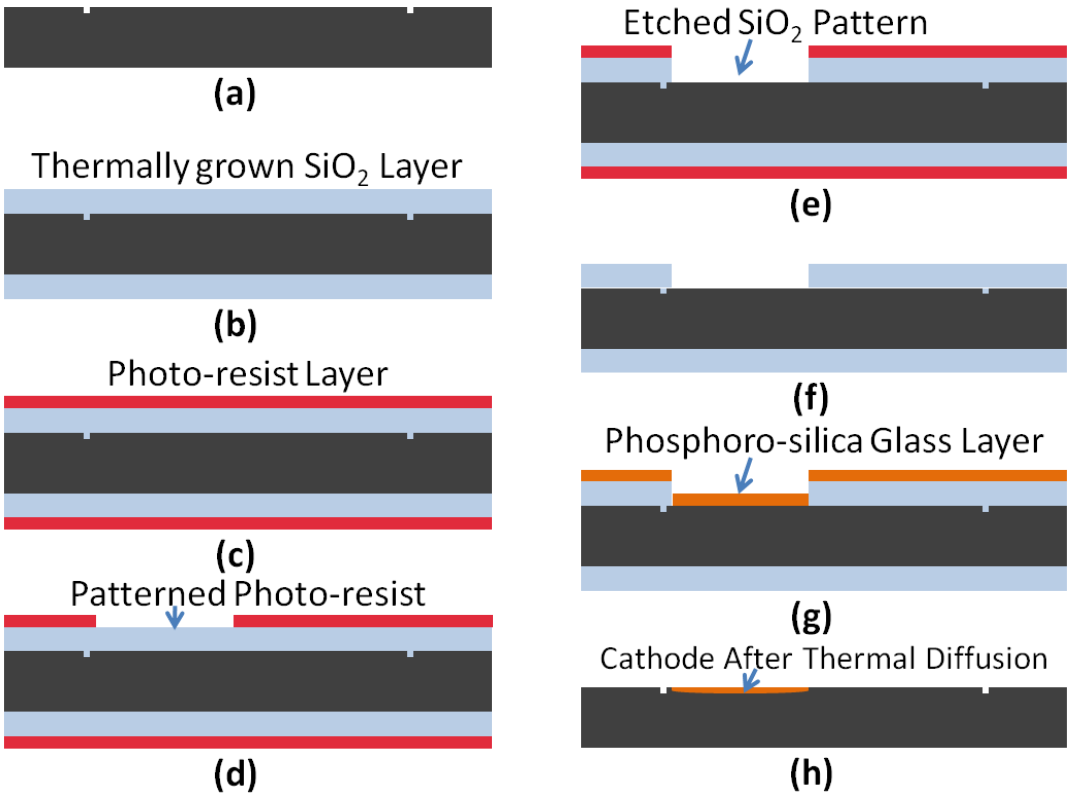


Figure 4.2: Oxidation & selective diffusion process (Phosphorous)

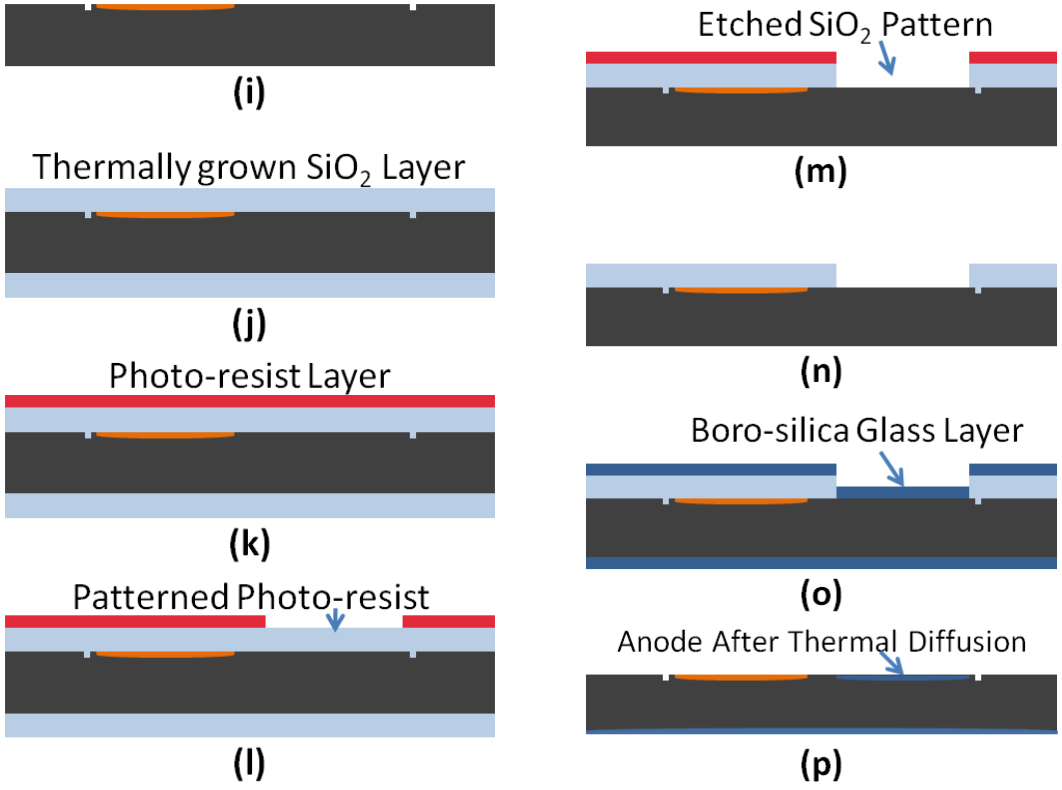


Figure 4.3: Oxidation & selective diffusion (Boron)

4.3.1.2 Growth of Gate Dielectric and Contact Metallization

Following the diffusion process, 50 *nm* thick gate dielectric was grown thermally as shown in Figure 4.4 (q). A photo resist layer was patterned as shown in (s) to etch the silica above n and p doped silicon regions. The silica etched layer is shown in (t). For alignment, photolithography markers on the mask were mapped onto the etched photolithography markers into silicon substrate. These markers were made using a silicon dry etch technique with STS-ICP, as already explained in Figure 4.1. The substrate was then metallized to form the top and bottom contacts. The metallized substrate was processed for lift-off in acetone by placing it in a hot water bath. Annealed contacts to p and n regions at the top surface and back contact are shown in Figure 4.4 (w). The fabrication process explained so far i.e. from Figure 4.1 to Figure 4.3 was the same for all sets of devices. It is imperative to note that in Figure 4.1 (b) different device isolation pattern masks were used for single and dual gate devices.

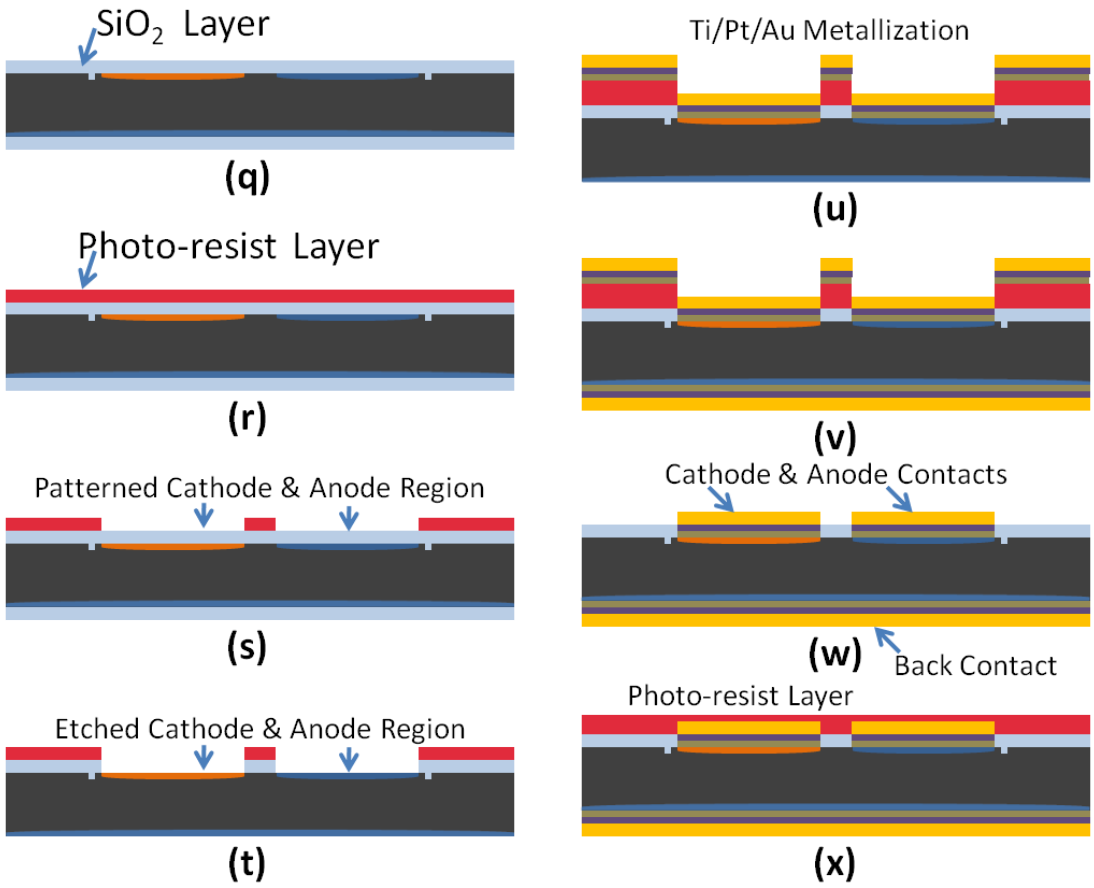


Figure 4.4: p,n and back contacts metallization.

4.3.1.3 Offset and Centre Single Gate Devices Processing

As already explained, variations in gated diodes differ from each other in terms of number of gates i.e. single / dual and placement / size of gate. Here two variations are discussed in single gate configuration. One set deals with the offset gate lateral p-i-n photodiode, whereas, the other deals with centre gate p-i-n photodiode. The fabrication process for both sets of devices is illustrated in Figure 4.5 (a) to (c) and (d) to (f), respectively. Offset gate structure towards p region is 20 μm x 500 μm, whereas the centre gate structure is 12 μm x 500 μm, which is placed half way between the two electrodes.

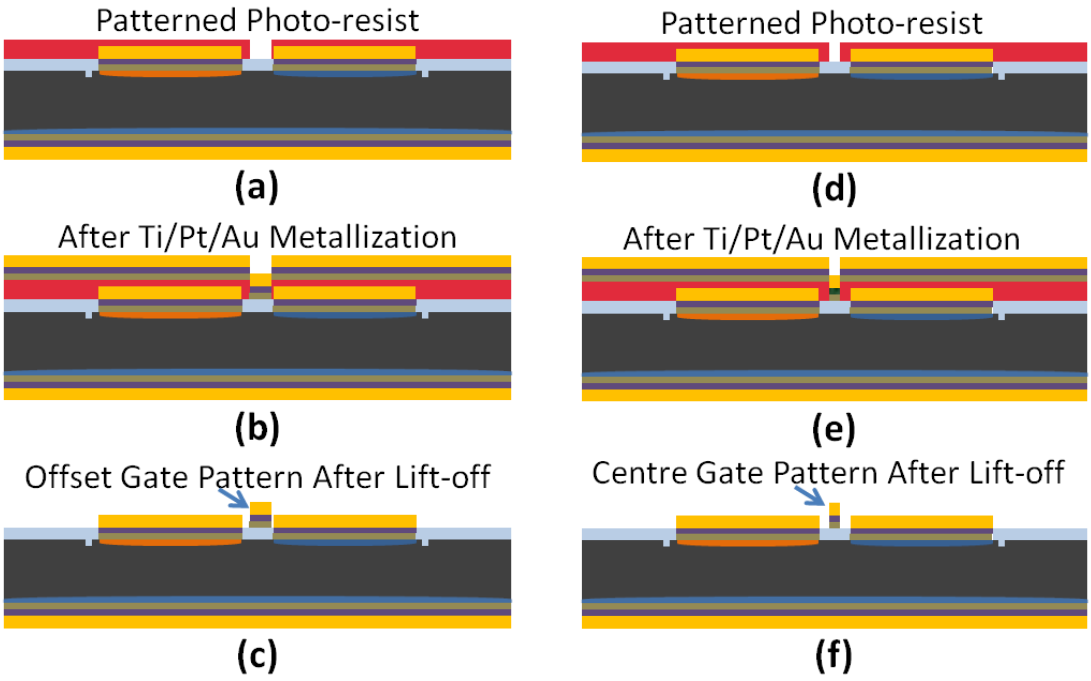


Figure 4.5: Offset and Centre Single Gate Fabrication steps

4.3.1.4 Normal and Overlapping Dual Gate Devices.

The initial fabrication process for the normal and overlapping dual gate devices follows the same steps as explained for single gate devices up to Figure 4.4. A normal dual gate device with two 9 μm x 500 μm gate structures are shown in Figure 4.6 (a) to (c) whereas from (d) to (f) the fabrication process for 15 μm x 498 μm overlapping dual gate device is illustrated. It is to be noted that the fabrication process for overlapping dual gate devices differed slightly, as explained in Figure 4.4 (s), where instead of patterning 500 μm x 500 μm square windows for

top anode and cathode contacts, 490 μm x 490 μm square windows were patterned, etched and metallized. This way both 15 μm gates overlapped the diffused regions under the gate dielectric. In both types of dual gate devices, the gates were 4 μm apart from each other.

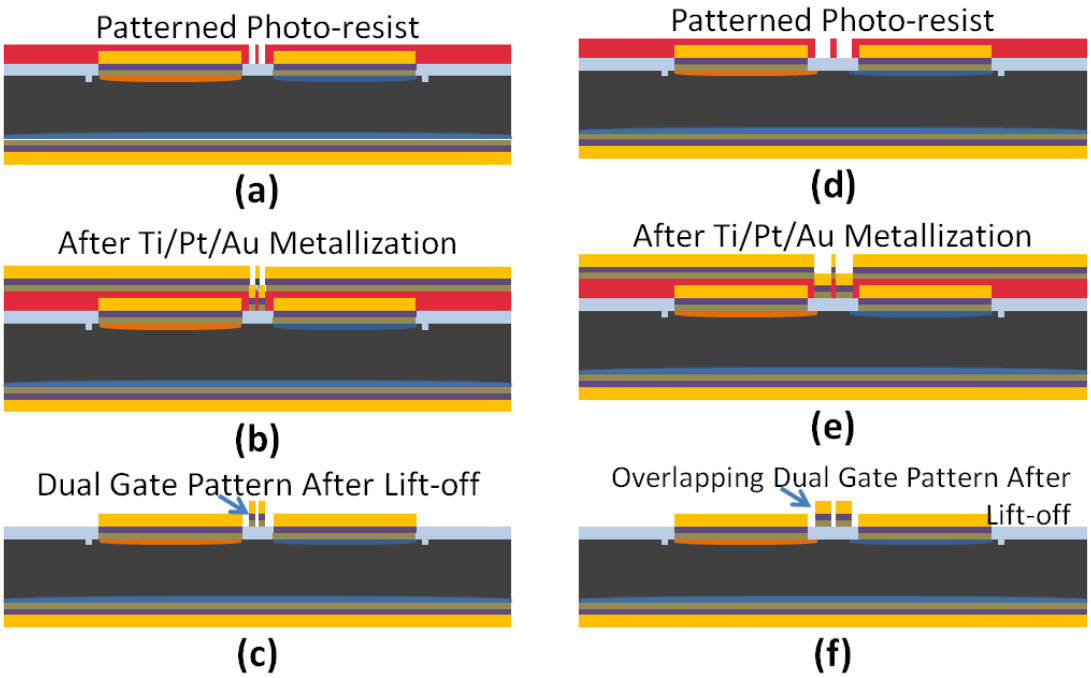


Figure 4.6: Dual Gate and Overlapping Dual gate Processing steps.

4.3.1.5 Grating Structure Patterning

Integrated metal grating structure was patterned using electron-beam lithography. The process for base device i.e. lateral p-i-n photodiode structure is the same as explained up to Figure 4.4 (w). In the next step a bi-layer electron-beam resist Poly methyl methacrylate (PMMA) 2010 15 % and PMMA 2041 4 % was spin coated as shown in Figure 4.7 (a). After baking the substrate in 180 ℃ oven the sample was exposed to electron-beam for grating pattern, followed by development process. The development process is described in the electron-beam lithography section, whereas the developed sample is shown in Figure 4.7 (b). After development process, the sample was metallized (with 50 nm and 150 nm aluminium) using an electron-beam evaporator, Plassys-II. Then it was processed for lift-off in Acetone, while placing the beaker containing acetone and sample was in hot water at 50 ℃. Finally, 1 µm wide and 500 µm long 14 integrated (aluminium) metal grating lines were patterned in the

32 μm intrinsic region between the two electrodes as shown in Figure 4.7 (d). It should be noted that Figure 4.7 (b),(c) and (d) show the image of grating area encircled in Figure 4.7 (a).

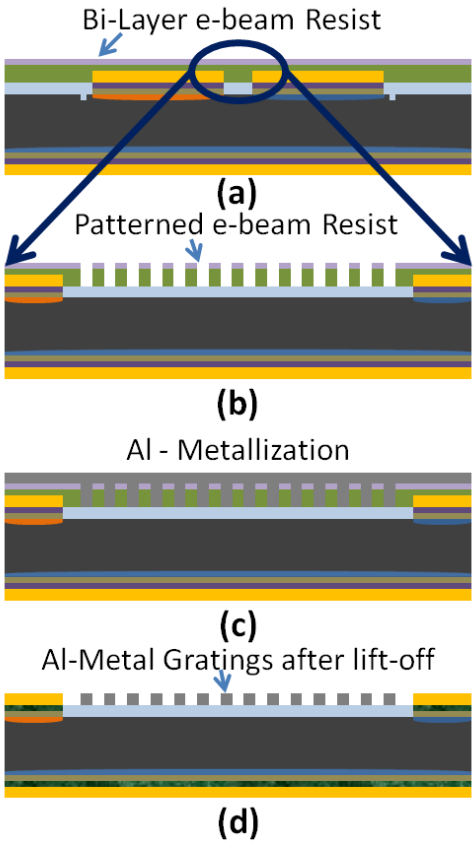


Figure 4.7: Patterning the grating structure

4.4 Fabrication Procedures

In the earlier sections, fabrication steps are described, whereas in this section details of the processes and critical factors affecting the fabrication process are given.

4.4.1 Substrate Cleaning

Device substrates require proper cleaning to remove contaminants and residues from prior process steps. Dust particles may also get on to substrates because of the sample cleaving process. Particulates can also arise as a result of certain fabrication processes, e.g. wet etching, dry etching, plasma etching, Chemical Mechanical Polishing (CMP) or metallization. Improper cleaning during fabrication processes may result in unwanted residue for the following fabrication step. These unwanted residues are mainly, films of native oxides,

common salts, bacteria or plastic residue [2]. Contaminants in the form of a very tiny dust particle can affect the pattern over the substrate, or impair the functioning of the device. In some cases, it may even result in a completely non-functional device.

Substrate cleaning is performed using cleaning solutions i.e. opticlear, acetone and methanol in a proper order. Opticlear is used to remove thicker oil/grease or wax layers which are normally produced after packaging, mechanical polishing or dry etching. Initially, the sample is placed into opticlear to remove any oil, grease or wax from the surface. Acetone is then used to clear the remaining oil and grease particles from the substrate which persist even after the use of opticlear. It removes organic impurities from the substrate as well. These impurities, in turn, contaminate the acetone solution. As acetone has a very high evaporation rate, so the substrate might be left with a layer of contaminated acetone and therefore it requires a rinse in methanol, which is a powerful solvent for contaminated acetone. During each cleaning step, the sample is placed in a cleaning solvent such as opticlear, acetone or methanol; in an ultrasonic bath for five minutes. Finally the substrate is rinsed in RO water and is dried with a stream of nitrogen gas.

4.4.2 Forming the Oxide Layer

Forming an oxide layer is a layering process in device fabrication. In this process, a layer of oxide is either deposited or grown over the substrate. Oxide can be deposited in different ways, which include Chemical Vapour Deposition (CVD), Plasma Enhanced Chemical Vapour Deposition (PECVD) and Molecular Beam Epitaxy (MBE). CVD is also known as Vapour-Phase Epitaxy (VPE). CVD if done, at atmospheric pressure is called Atmospheric Pressure Chemical Vapour Deposition (APCVD); at low pressure it is called Low Pressure Chemical Vapour Deposition (LPCVD). When plasma energy is added to the thermal energy of a conventional CVD system, the energy-enhanced CVD method is known as PECVD [3]. MBE on the other hand, is an epitaxial process carried out at ultra-high vacuum conditions (nearly $\sim 10^{-8}$Pa). It involves the reaction of one or more thermal beams of atoms or molecules on a substrate surface [4].

Oxide, if not deposited, may be grown over the substrate thermally. This thermal growth of oxide can be done with either wet or dry oxidation processes. Furnace temperature for oxide growth is dependent on fabrication requirements; normal temperature range for thermal

oxidation is from 300 ℃ to 1200 ℃. Wet oxidation is relatively faster than dry oxidation, and it is used for thicker oxide layers, whereas dry oxidation is used for the precise growth of high quality thin oxide layers. In the fabrication of these devices, wet oxide was grown at the rate of 2.85 nm/min, and dry oxide was grown at the rate of 1.65 nm/min, while the furnace temperature was set at 1135 ℃ and O_2 gas flow was fixed at 6 cm^3/min (ATP) . A schematic diagram of the furnace used for oxidation is shown in Figure 4.8. During the fabrication of the surface gated photo-detector, 250 nm and 50 nm of oxide were grown by dry oxidation at a furnace temperature of 1135 ℃. The quality of dry SiO_2 layer produced is better and it is less porous as compared to wet oxidation or deposited silica films.

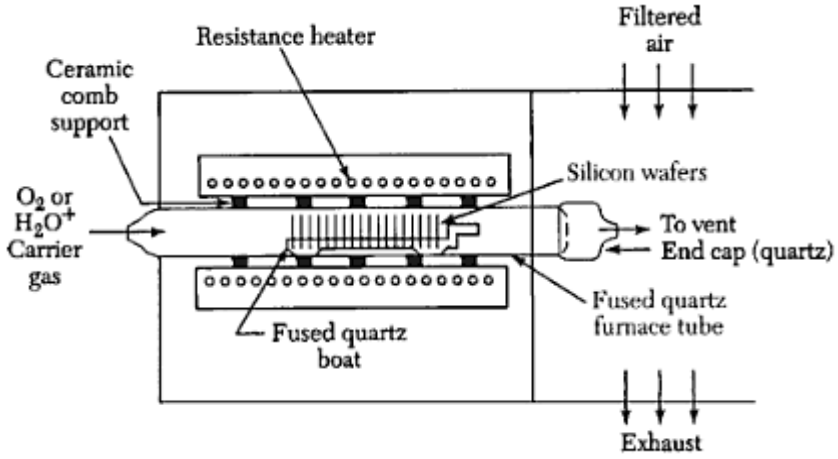


Figure 4.8: Schematic diagram of oxidation Furnace [5].

4.4.2.1 Factors Affecting Oxidation Rate

Oxide growth is affected by many factors like atmospheric pressure, crystal orientation, wafer type i.e. n – type or p – type and temperature. The impact of temperature is relatively more pronounced than other factors and it affects both dry and wet oxidation processes. Repeated oxidation processes during the fabrication of these devices have shown the same oxidation rate at a given temperature. The impact of other factors is either nominal or may be seen only when two or more factors combine. The oxide growth rate for silicon oxidation, under the same conditions, varies for wet or dry oxidation processes. The gated photodiode devices have a lateral p – i – n doping profile; the oxidation rate varies for p and n doped regions. A 50 nm silica layer is formed after diffusion of p and n type impurities. Finally, the SiO_2 growth profile is uniform over the surface of silicon substrate, however, it varies in thickness at

impurity doped areas, i.e. boron doped, phosphorous doped and normal silicon area, as shown in Figure 4.9.

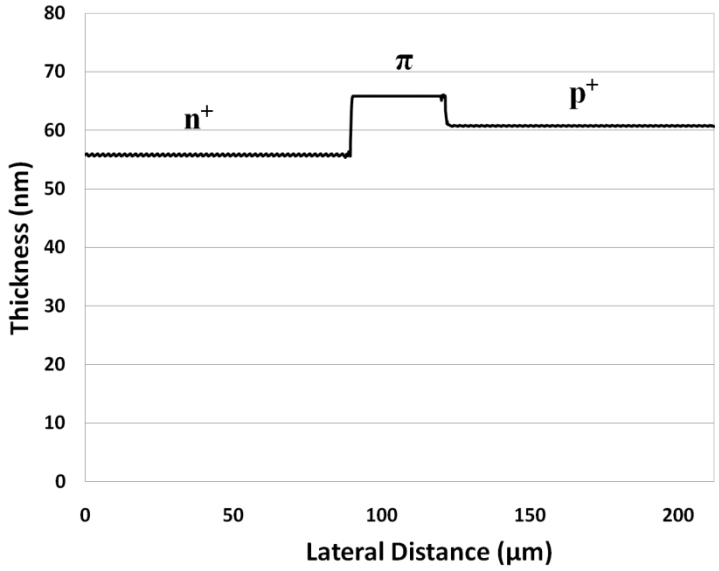


Figure 4.9: Dry oxide growth at n^+, π and p^+ regions.

The presence of water vapours in the oxidation environment affects the oxidation rate. As water molecules are highly soluble in silicon dioxide, they reach the silicon – silicon dioxide interface quicker than the oxygen molecules. This high diffusivity of water molecules accounts for the higher wet oxidation rate. Higher pressure of the gaseous oxidizing agent can also result in higher oxidation rates. This can be seen particularly at lower temperatures. Low pressure of oxidizing agent at low temperature can be used to grow more precise thin oxide layers using dry oxidation processes.

The growth rate and quality of the oxide also depends upon the crystal orientation of the silicon wafer i.e. $< 100 >$ or $< 111 >$. These two crystal orientations are commonly used for MOS and bipolar devices, respectively. The surface gated photo detector is a MOS structure, so a $< 100 >$ crystal orientation $p-$type, float zone wafer was used for its fabrication. Growth rates for silicon with crystal orientation $< 100 >$ and $< 111 >$ are shown in Figure 4.10 and Figure 4.11. It can be clearly observed that the oxidation rate difference for silicon crystal orientations $< 100 >$ and $< 111 >$ is negligible when oxidized for larger duration, i.e. over thirty (30) minutes [6].

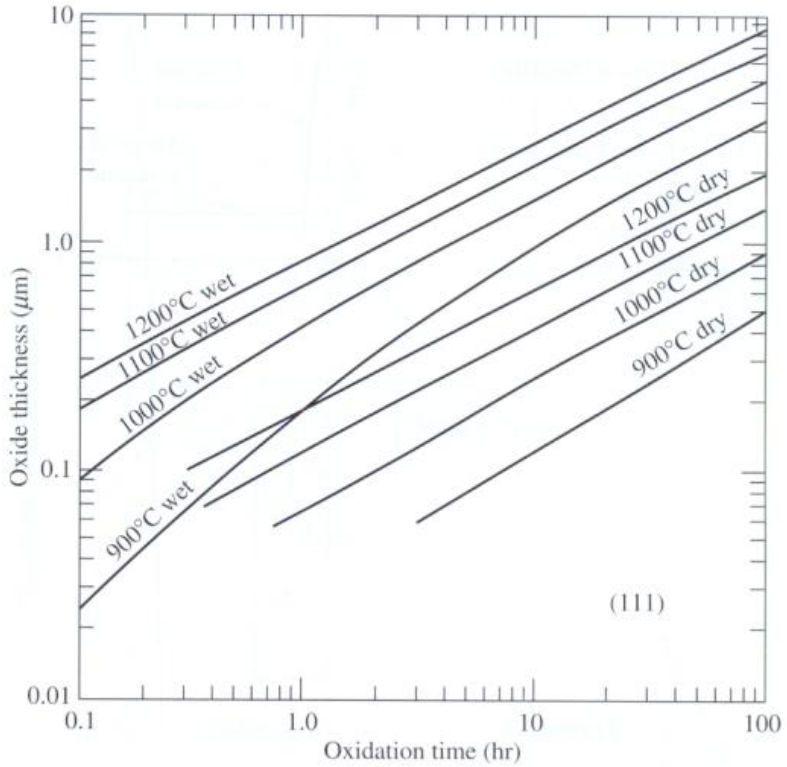


Figure 4.10: For <100> crystal orientation [6]

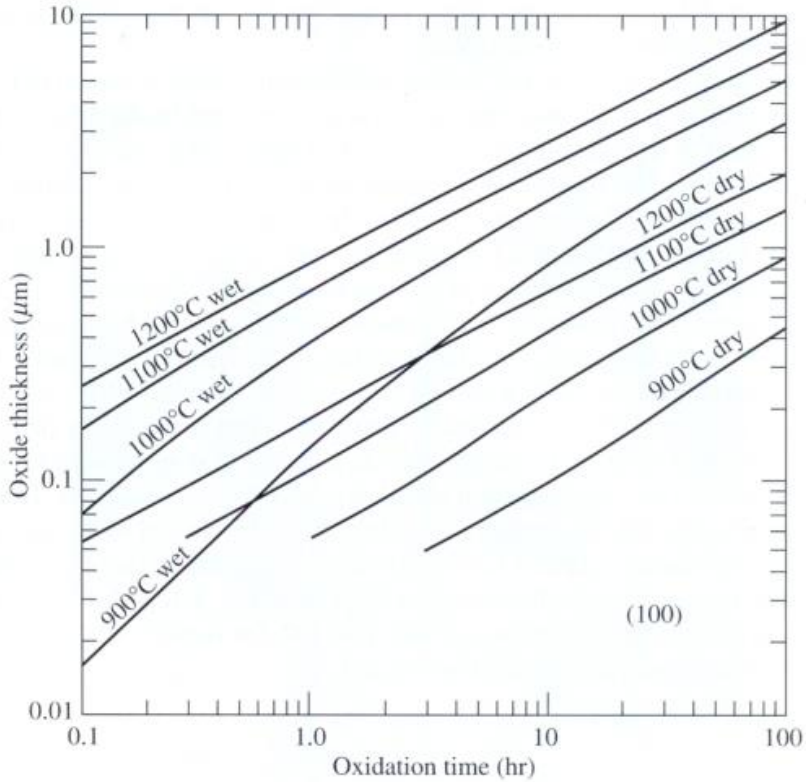


Figure 4.11: For <111> crystal orientation [6].

In order to analyze the variations in dimension and placement of single and dual gate devices the thicknesses of the oxide layer and the scheme of the metal contacts should be identical. In the surface gated devices, hydrofluoric acid (40 %) was used, to clear the silica layer after the diffusion processes. Furthermore, diffusion technique was used instead of ion implantation. This required thicker barrier layer (SiO_2) instead of normal thin dielectric layer. To overcome the issue of metal marker's stability at higher temperature, etched markers were made instead of metallized markers. For this, dry etch technique was used with STS-ICP using SF_6/C_4F_8. The oxide layer was patterned, either for diffusion or for contacts, by aligning the etched photolithography (PL) markers on the substrate to the PL markers on the mask. Once all the diffusion processes were over, the final thin gate dielectric (50 nm) layer was grown over the substrate using dry oxidation. A repeated oxidation process, for selective diffusions and gate dielectric, is likely to redistribute the impurity atoms over the surface of p and n doped regions. Carrier concentration results showed that the doping level in the p doped region is a little less than that in n doped region. This is because p type impurity was diffused first and the substrate was then oxidized to process for n type impurity diffusion, this oxidation process caused p type impurity atoms to migrate.

Hydrogen atoms during oxidation (i.e. wet oxidation) or diffusion act as catalysts for boron diffusion into SiO_2 layer. In fabricating surface gated devices dry oxidation process was used for both barrier layer (SiO_2) growth and for the gate dielectric. This ensured a fairly low probability of hydrogen atoms being present in the oxidation process. Thus, the dry oxidation process was likely to have a negligible impact on the substrate with regard to impurity redistribution. This negligible impact can be seen on comparing the carrier concentration values of p and n doped regions, which are $6.38 \times 10^{17}\ cm^{-3}$ and $1.48 \times 10^{18}\ cm^{-3}$, respectively.

4.4.3 Lithography

In device fabrication, lithography is the transfer of a pattern onto the substrate surface. Photolithography and Electron beam lithography are two widely used methods in semiconductor device fabrication. These two methods were used at different stages while fabricating the devices described in this thesis. Other variants of lithography are x-ray

lithography, interference lithography, shadow masking, nanoimprint and scanning probe lithography [7].

4.4.3.1 Photolithography

Photolithography is a process of transferring patterns using a mask onto a thin photosensitive layer, called photo-resist. The tone of the photo-resist may be either positive or negative. Use of the photo-resist mainly depends upon the mask used to transfer the pattern and the limitation of the fabrication process. Furthermore, positive and negative photo-resists are used for dark field and light field masks, respectively. During the fabrication of these devices, a dark field mask was used with S1818 positive photo-resist.

Large patterns can be easily transferred using photolithography. Soaking of the sample in chlorobenzene after dehydrating the resist layer, makes it a bi-layer resist which helps in making an undercut profile after development. This helps in making small features and precise edges in metallization and subsequent liftoff processes.

4.4.3.1.1 Positive Resist

The exposure of positive photo-resist to UV light changes the chemical composition of its exposed portion and it becomes more soluble in the developer solution. This way the resist exposed to UV light is washed away and the rest remains on the wafer. For positive resist it is said that “whatever shows goes” [8].

4.4.3.1.2 Negative Resist

In contrast, the exposure of negative photo-resist to UV light changes the chemical composition of the exposed portion of the photo-resist. It is transformed into a cross-linked polymer, which becomes harder and thus, cannot be dissolved in the developer solution. After development the polymerized portion of the resist stays and the rest of the resist gets dissolved in the developer solution.

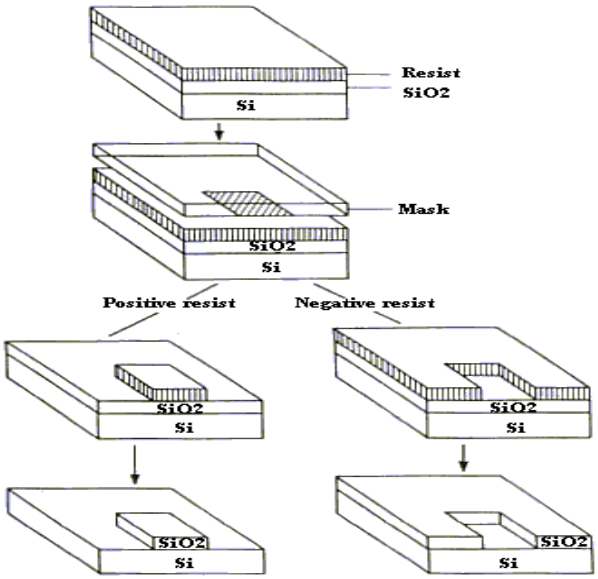


Figure 4.12: Development of positive and negative photo-resist [8]

4.4.3.2 Resist coating

A smooth profile of the photo-resist coated over the substrate is vitally important for homogeneous exposure and uniform development processes. In order to coat the photo-resist layer over the substrate, a spinner with a vacuum chuk is needed. The substrate is placed on the vacuum chuk for spinning the photo- resist. Use of a spinning chuk or a spinning cabinet for different types of photo-resists, may possibly add the danger of cross contamination. Thus in standard clean-room environment, spinners are normally categorized for different types of resists and chuks are placed in respective spinning cabinets. There is always the risk that cross contamination may influence the exposure routines or the development process. The substrate, placed over the chuk, is carefully covered with drops of photo-resist, such that no air bubbles are introduced in the photo-resist material. The substrate is then spun for a set duration and at a specific spin speed in order to achieve the desired thickness of resist. Thickness of the thin resist layer is a function of spin speed. [Thickness $\propto {}^{1}\!/\!_{\sqrt{\text{spin speed}}}$]. However, it depends upon the viscosity (solid content) of the resist as well.

Adhesion of the resist layer to the surface of the substrate is another issue, which come across while spinning the resist over the substrate. If this is a problem then a very fine and thin layer of adhesive liquid, hexamethyldisilazane (HMDS) is spun before spinning the photo-resist [6].

The substrate after the adhesive liquid and the photo-resist layer is then soft baked at 100 ℃ for 10 minutes on a hotplate in order to make the adhesion stronger and to remove any residual solvent from the thin photo-resist layer. For these devices, layers of adhesion promoter HMDS and S1818 photo-resist were produced by spinning the substrate at 4000 RPM for 5 seconds and 30 seconds, respectively. Final thickness of the photo-resist layer produced over the device substrate was 1.8 μm.

4.4.3.3 Mask Alignment and Exposure

Device fabrication involves multiple lithography exposures. The size of the pattern and the alignment accuracy are the main parameters important for either photolithography or electron beam lithography. In some cases a combination of both techniques can be used to form a desired pattern. In either lithography technique, alignment markers are needed to expose the mask pattern exactly over the substrate pattern, except for the first exposure. The process of aligning markers on the mask, to the markers on the substrate is called mask alignment.

The shape and size of alignment markers vary in different lithography techniques. Once the mask pattern is aligned to the substrate design, the photo-resist is exposed to high intensity UV light for a specific time [6]. For single gated devices, all device patterning was done with optical lithography using S1818 photo-resist and a Karl-Suss i-line mask aligner at $7.2\ mW/cm^2$ UV exposure dose. Exposed substrates were then developed to form the pattern in the resist layer.

4.4.3.4 Development

Following the exposure, the sample was processed for development. The strength of the developer solution and the length of the development time vary for different exposure routines. These details are provided by the photo-resist manufacturer. In the device fabrication, the substrate was exposed to UV light for 4 seconds and was then placed in the developer solution for 80 seconds and finally it was rinsed in RO water for 80 seconds. The developer solution was composed of a fresh mixture of micro-posit developer and RO water in 1: 1 ratio.

4.4.3.5 Electron Beam Lithography

Karl-Suss i-line mask aligner can be used to pattern features down to 2 micron dimensions. Smaller and more closely spaced structures can be made using electron beam lithography, which is a development from Scanning Electron Microscopy (SEM). It allows for patterning extremely thin and fine features in the nanometre range.

4.4.3.5.1 Resist Coating

Resist coating for electron beam lithography is similar to that for photolithography, except for the use of a special electron beam resist. Like photolithography, the substrate may be coated with either positive or negative electron beam resist. Among electron beam resists, Poly-Methyl Methacrylate (PMMA) is used as a positive electron beam resist whereas Hydrogen Silsesquioxane (HSQ) is used as a negative electron beam resist. In electron beam lithography, selected resist recipes, namely mono-layer, bi-layer or tri-layer schemes, are used for specific purposes. In the case of mono-layer, bi-layer or tri-layer recipes, the final thickness of the resist layer is the sum of the thicknesses as a result of spin cycles for each layer. In the devices with dual gates, pattern of the gate structure was transferred with electron beam lithography using a bi-layer recipe. Resist coating was done by spinning PMMA – 2010 15% at 5000 RPM for 60 seconds to make the first layer. It was then hard baked for 30 minutes at 180 ℃ in an oven to remove any residual solvent from the resist layer and to make the adhesion stronger. Another layer of PMMA – 2041 4% was spun at 5000 RPM for 60 seconds and was then placed in an oven at 180 ℃ for 90 minutes. The thickness for the bi-layer resist was 1200 nm for PMMA – 2010 15% and 126 nm for PMMA – 2041 4% which sum up to 1326 nm of total thickness. Tri-layer resist, however, may be used to make larger patterns and to obtain more stable undercut.

4.4.3.5.2 Exposure

The column containing the electron source is the primary component of any electron beam lithography system. A heated tungsten filament in the electron source generates a beam of electrons using thermionic emission. The beam is formed and accelerated by electro-optic lenses. Features of the electron beam influence the exposure in a variety of ways, including,

the size of the virtual source, its brightness and energy spread. The size of the virtual source determines the level of demagnification that the beam must undergo to affect the target whereas the brightness of the beam is determined by the size of virtual source and this must be sufficient enough to affect the resist layer. The energy spread determines the pattern of electrons moving outwards from the source in the direction of the main electron beam. In the chamber, underneath the column, there is a stage to load and unload samples. A specific vacuum is maintained during loading and unloading of the sample through the load lock mechanism [9].

A specialized computer controls the electron beam lithography exposure processes, like loading the job, aligning and focusing the electron beam and transferring pattern data to the pattern generator. Due to mask-less exposure process and flexible use over a variety of semiconductor materials, electron beam lithography has become very important. The electron beam exposure breaks the positive resist polymer into fragments. Once the exposure is over, the sample can be developed in a developer solution and as a result, the resist layer is patterned. Electron beam lithography is specialized and more precise, however, it is much slower than conventional photolithography. It is also expensive as it uses a specialized piece of equipment and thus requires frequent maintenance and calibrations. For the dual gate devices, electron-beam jobs were run using electron beam markers. These electron beam markers were made using a photolithography mask by aligning the photolithography markers on the mask to the etched photolithography markers on the silicon substrate.

4.4.3.5.3 Development

The developer solution for PMMA is a mixture of Isopropyl Alcohol (IPA) and Methyl Isobutyl Ketone (MIBK) with the ratio 1:1. Normally, the development is done in a series of steps. These steps may vary slightly depending upon the exposure routine and the thickness of the resist layer. Exposed device substrate was developed in the developer solution (IPA and MIBK in the ratio of 1:1) for 60 seconds, while the temperature of the solution was kept at 23 ℃. The sample was then rinsed twice in fresh RO water for 60 seconds each, and finally it was dipped in IPA for 60 seconds.

4.4.4 Diffusion

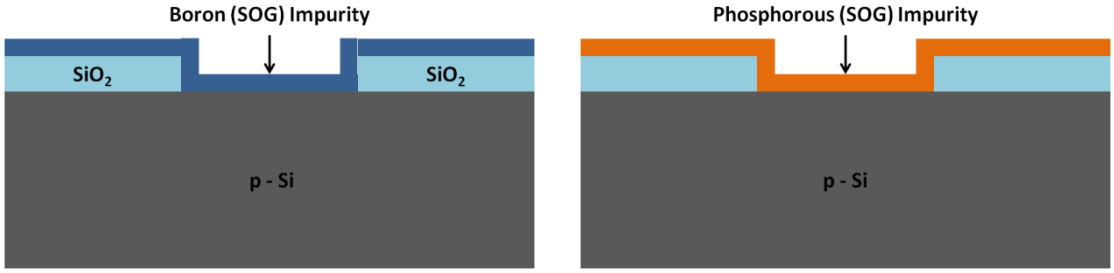
The amount of impurity atoms can be adjusted using different techniques which depend upon how precise and deep the impurity profile is required to be. A layer of dopant impurity is pre-deposited through spin-on-glass technique which is subsequently diffused through a thermal treatment. This results in a less precise doping profile and the process is called thermal diffusion. However, for well controlled and precise doping profile, ion implantation is generally used. Doping profile (impurity concentration and thickness) can be controlled by controlling the parameters of ion implantation. While fabricating the devices mentioned here the thermal diffusion technique was used exclusively.

4.4.4.1 Thermal Diffusion

The surface gate diodes differ from ordinary $p-i-n$ photodiodes in having a lateral doping profile. The p, i and n regions are arranged horizontally. These regions were created by doping parts of the structure strongly n and p type while leaving a gap in between. Float zone silicon was used to fabricate the devices. The starting wafer material had a resistivity of $4\ k\Omega-cm$. Selective and bulk diffusion processes were used for dopant diffusion. In a bulk diffusion process, no mask is needed, as is the case with backside diffusion to make the back contact strongly $p-$ type, whereas in selective diffusion a patterned barrier layer e.g. SiO_2 is needed, as is the case with surface gated photo detectors, where 250 nm thick thermal oxide was grown all over the substrate through dry oxidation at 1135 ℃. This was to serve as a doping mask for selective diffusion. Windows were opened in the oxide to dope anode and cathode regions, with p and n type impurity, respectively. Dopant source coating was done using spin-on-glass technique. These anode and cathode regions were squares of area 500 μm x 500 μm. Doping was performed through elevated temperature diffusion from phosphorus and boron containing spin-on-glass (SOG). The p-region was doped to $6.38 \times 10^{17}\ cm^{-3}$ whereas the n-region was doped to $1.48 \times 10^{18}\ cm^{-3}$. Thickness of the diffusion barrier i.e. SiO_2 depends upon the impurity type, diffusion time and the temperature at which the diffusion takes place.

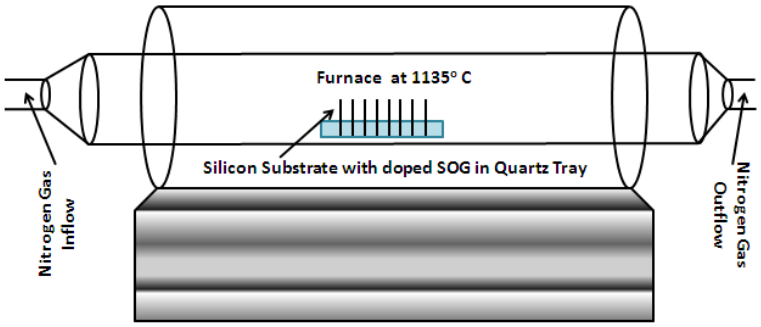
The dopant source coating has a specific thickness based on the viscosity and the spin speed, as is shown in Figure 4.13 (a) and (b). The diffusion strength is determined by the temperature and duration for which the sample is placed in the furnace. The oxide layer acts as a barrier

layer for selective diffusion as shown for selectively diffused samples in Figure 4.13 (d) and (e). Here the substrates shown were etched with HF after thermal diffusion to remove the oxide layer. To avoid further oxidation during diffusion process nitrogen gas is used which purges the furnace to minimize the oxidation process on silicon substrate.



(a) (b)

Boron and Phosphorous doped impurity layer using SOG technique for selective diffusion.



(c)

(d) (e)

Doped Boron and Phosphorous impurity at selective regions, after thermal diffusion in furnace.

Figure 4.13: Schematic illustration of diffusion process.

During the fabrication of these devices, the substrates with n and p type dopant source coating layer using SOG were diffused for 20 min at 1135 ℃ in the furnace. The nitrogen gas flow was maintained at 6 cm^3/min(ATP).

4.4.5 Etching

In semiconductor fabrication, etching is the process of removing a layer or material from a semiconductor wafer by means of liquid or gaseous agents. This process may etch the semiconductor material itself or any deposited layer over the semiconductor material. The deposited layer may be insulating or metallic. Etching can be done using dry or wet etching mechanisms, both of these means provide selective and bulk etching. A sample can be patterned for selective etching using lithography techniques. Dry etching is also called plasma-assisted etching. Both advantages and disadvantage are associated with wet and dry etching. In the process selective silicon etching was done using dry etching technique, whereas selective wet etching was used to etch the silica layer.

4.4.5.1 Dry Etching

Dry etching processes combine both chemical reactions and physical bombardment to remove material. The chemical reaction uses reactive gas plasma, whereas the physical removal component uses momentum transfer to expose new material. Plasma etching refers to a pure chemical dry etching technique, whereas ion beam milling or physical sputtering are physical material removal techniques. In plasma etching, reactive species are produced in the plasma which are diffused and subsequently adsorbed on the surface of the wafer. The reaction takes place at the surface of the wafer and produces volatile products, which in turn are absorbed into the bulk of the gas and can simply be pumped out of the system. In this process, it is important to formulate the etch recipe for selective etch, so that the patterned mask used as the barrier layer is not etched away. For good dry etching, high selectivity i.e. the ratio of etch rate of target material to the etch rate of mask material, is usually needed. High etch rate and etch uniformity play an important role in selecting a dry etch recipe. Another important factor that must be considered for selective etching, is ‘anisotropy’ of etching. This essentially means that the etch recipe with a pronounced anisotropy behaviour will avoid etching horizontally i.e. undercutting can be avoided. This can be seen in Figure 4.14, where isotropic and anisotropic etching behaviours are shown.

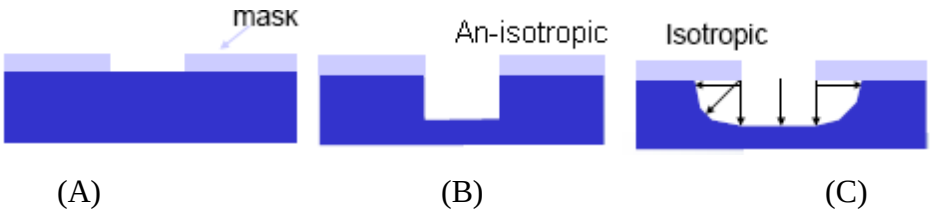
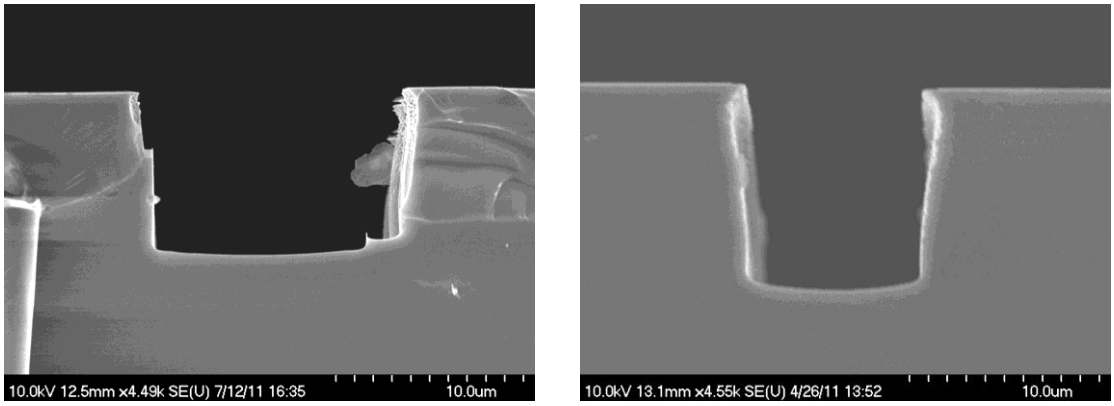


Figure 4.14: Isotropic and An-isotropic etch profile

However, if a high degree of accuracy is needed in an-isotropic behaviour, then dry etch techniques that emphasize physical removal of material should be used. This technique makes use of a stream of highly energetic and inert species or ions to bombard the surface. This process also affects the mask and thus, cannot be used for deep etching. A process which involves a mix of both physical sputtering and chemical process may result in an acceptable combination of isotropy and selectivity; Reactive Ion Etching (RIE) is one such process. It is also referred to as Reactive Sputter Etching (RSE)

Dry etching processes have both advantages and disadvantages. On the positive side, dry etching uses small quantity of chemicals to achieve either isotropic or anisotropic profiles. Besides better process control, it also provides less undercutting, high resolution and directional etching independent of crystal orientation. On the other hand, the use of toxic and corrosive gases and the possibility of re-deposition of non-volatile compounds produced as by products are main disadvantages of the dry etching technique. Re-deposition also compromises selectivity.

In the device fabrication process a 10 μm wide trench was created all around the device for isolation purposes. All silicon etches were carried out in a Inductively Coupled Plasma (ICP) tool using C_4F_8/SF_6 gas mixture in the ratio of 50: 40 standard cm^3 per minute (sccm). The power used for the etch process was kept at 600/10 W for the coil/platen process. Coil and platen process actually represent chemical and physical etching processes, respectively. The entire process was carried out at 10 mTor background chamber pressure. Standard etch rate for this recipe is 0.84 μm /minute. C_4F_8 gas was used for passivation and SF_6 was used for etching. In Figure 4.15 (a) and (b) SEM micrographs show the profile of silicon dry etches with two different etch recopies i.e. $HPTEST-4$ and $RYT-1$. Isotropic and anisotropic behaviour can be seen clearly with these two recipes. The anisotropic profile of etched markers however, helps in fine alignment better than an isotropic profile.



(a) (b)

Figure 4.15: SEM micrograph of silicon dry etch with (a) HPTEST 4 and (b) RYT-1recipe.

4.4.5.2 Wet Etching

A wet etching process is suitable for silicon bulk etch or to etch large patterns. Silicon wet etching is relatively slower than dry etching. In wet etching, reactants reach the surface of the sample through diffusion, where reaction occurs and bulk or selective area is etched away. Etch rate is influenced by two major factors: temperature and concentration of the etch solution. Just like the oxidation of silicon, wet etching also shows a dependence on the orientation of the silicon crystal lattice.

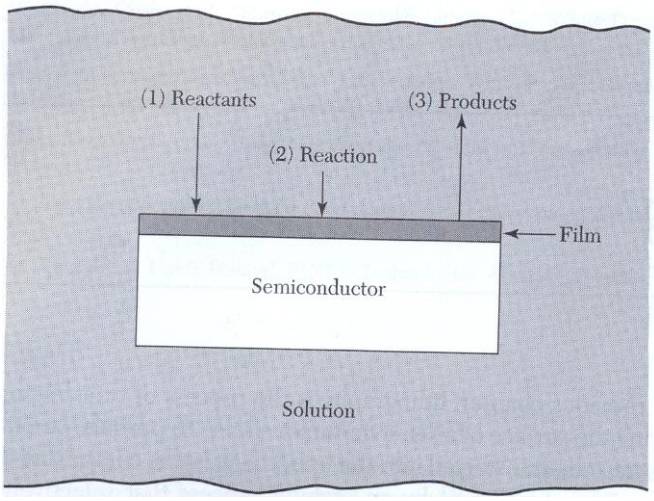


Figure 4.16: Basic mechanism in wet chemical etching [3].

Since silicon with lattice plane $< 111 >$ has more bonds available per unit area than $< 110 >$ or $< 100 >$, the wet etch rate of $< 111 >$ lattice plane, is relatively slower than others. Ratio of the etch rates for the $< 100 >, < 110 >$ and $< 111 >$ planes is $100: 16: 1$ at $80\ ℃$ [3]. A

commonly used wet etch for silicon is, a solution of KOH and water. It is important that etch rate remains constant for the whole of the reacting surface, otherwise, the etched surface will not be uniform. Uniformity of the etch rate can be calculated by the following formula [10].

$$\text{Etch rate univormity (\%)} = \frac{(\text{Maximum etch rate} - \text{Minimum etch rate})}{(\text{Maximum etch rate} + \text{Minimum etch rate})} \text{ X } 100\%$$

To etch Silicon dioxide (SiO_2), a diluted solution of HF is preferred. The presence of ammonium fluoride (NH_4F) in HF makes it a buffered HF solution. Its presence on the one hand replenishes the depleted fluoride ions and on the other hand controls the pH value. As a result, stable etching performance and uniform etch rates are achieved. The absence of NH_4F may result in a less uniform etched surface [3, 10].

The etch rate of silicon dioxide SiO_2 is influenced by the quality of oxide layer, concentration of etching solution and its temperature. Parameters like, porosity, density and the presence of impurity in the oxide layer, define the quality of oxide. Thus the oxides deposited through CVD or grown through thermal oxidation have different etch rates. Since the oxide deposited through CVD is more porous and is likely to have more impurities than thermally grown oxide, it therefore, shows faster etch rates. For these devices, 250 nm thick thermal oxide was grown all over the substrate through dry oxidation at 1135 ℃. This was to serve as a doping mask. Using HF solution (1: 5) selective areas were etched to metalize the anode and cathode regions. These selections were squares of area 500 μm x 500 μm. Figure 4.17 shows the etch profile of SiO_2. Here it is clearly seen that the wet etching profile is isotropic i.e. etching solution attacks all directions, uniformly.

4.4.6 Metallization

During the fabrication process devices are metallized to obtain electrical contacts. Metallization techniques generally used in semiconductor fabrication include: thermal evaporation, electron-beam evaporation, flash evaporation, induction evaporation and sputtering. The most common technique in semiconductor device fabrication is electron beam evaporation. In electron beam evaporation, metal vaporization and coating over the substrate is achieved by a high current focused electron beam. This beam increases the temperature of the

crucible to vaporize the material and in order to maintain the temperature below the melting point of the crucible; the crucible is placed in a water-cooled arrangement.

Contacts are of two types, rectifying and ohmic. In rectifying contacts the metal-semiconductor junction, conducts with only one bias polarity and not with the other. A weak rectifying behaviour is seen in almost all metal-semiconductor junctions. Ohmic contacts in contrast, conduct for both polarities. Thus, in order to provide input or obtain output signal from a contact, ohmic contacts are needed. Contacts can be made ohmic either by a proper selection of contact metal and further annealing the contact to lower the barrier height or by making the barrier very narrow by means of heavy doping $\sim 10^{17}$ dopant atoms/cm^3 or more. A tri layer Ti/Pt/Au metallization was used to make the ohmic contacts on both the anode and cathode region in these devices. This tri layer metal stack was only used for convenient wire bonding and can be avoided in a CMOS process flow.

4.4.7 Lift-off

Contacts can be made either by a lift-off process or by etching the metal. In case the contacts are made using a lift-off process, the resist layer is patterned first, followed by metallization and subsequent lift-off. Lift-off is normally done by placing the sample in hot acetone for 20 to 25 minutes in a temperature-controlled environment at 50 °C. Whereas, when the contacts are formed through etching, bulk metal is deposited over the substrate surface, followed by spinning the resist layer over the metal surface. This resist layer is then patterned to etch the exposed metal to form the final contacts.

In fabricating the devices, metal was deposited using Plassys I and Plassys II machines in the JWNC facility. These machines works with electron beam sources, to vaporize the metal. The metallization recipe used for contacts was Titanium (33 nm) / Pd (33 nm) / Au (240) and Titanium (33 nm) / Pt (33 nm) / Au (240) for plassys-1 and plassys-II, respectively. An SEM micrograph is shown in Figure 4.17, which shows the metal and a slight gap (~160 nm) between the gate dielectric. This is due to isotropic behaviour of HF i.e. wet SiO_2 etching.

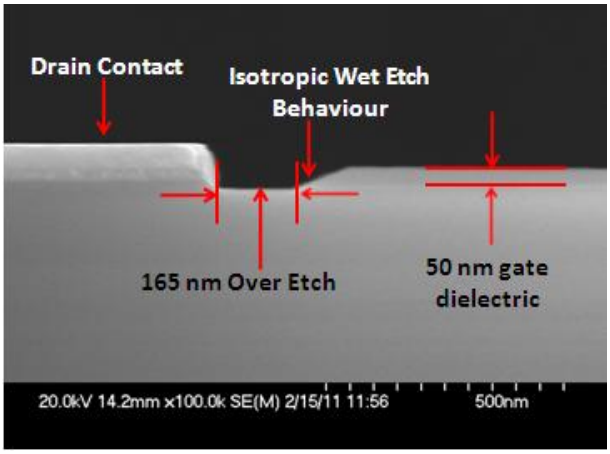


Figure 4.17: Contact metal and gate dielectric

4.4.8 Device Isolation

The fabrication of semiconductor devices, involves a large number of devices on a single chip. Micro and nano fabrication techniques have put these devices very close to each other separated by microns or sometimes even less. One device may interfere in the operation of the adjacent devices. Normally, these devices should ideally perform their operations, independently, without any external effect. Isolation is needed to block any unnecessary transmission path between or around the device(s), which also reduces the leakage current. In order to functionally isolate these devices from others or limit the operational semiconductor area, device isolation techniques are imperative in fabrication processes.

4.4.8.1 Techniques

The isolation of the components from one another is critically important while fabricating devices, thus making the design of a device flexible and independent of interference from the nearby devices.

One simple way of implementing the isolation is by making two components of a semiconductor device effectively isolated by using a pn- junction. This is called pn−junction isolation. Other techniques include forming independent pockets of active semiconductor material called mesa isolation, or alternatively the oxide isolation technique can be used to form insulating trenches to separate the different pockets of semiconductor. Individual or combination of isolation techniques may be used to fabricate devices [2].

4.4.8.1.1 pn – Junction Isolation

The isolation technique most suitable with semiconductor device fabrication is pn – junction isolation. It is basically an electrical isolation of a device, which is surrounded by a junction depleted of charge carriers. When it is reversed biased, the junction width increases and exhibits a high resistance, thus isolating the device from the surrounding components. This is known as pn – junction isolation. Its main advantage is its suitability with semiconductor device fabrication. The disadvantages include longer diffusion time than normal diffusions, as it is a lateral diffusion and the junction area is actually a wastage of substrate space and parasitic capacitance as a result of junction formation. These issues can easily be overcome in dielectric / oxide isolation technique.

4.4.8.1.2 Mesa Isolation

Devices or circuits which are fabricated on insulating or semi-insulating substrates may be processed with mesa isolation. In the context of silicon devices, epitaxial silicon grown over sapphire (SOS) is masked with patterned photo-resist. The exposed semiconductor is etched with wet chemical etch and as a result mesas (individually separated islands) are formed. The device is fabricated on the resulting isolated islands of silicon. These islands are called mesas; hence the technique is termed mesa isolation. The substrate is etched deep enough, so that electrical isolation is achieved.

4.4.8.1.3 Oxide (dielectric) Isolation

In silicon devices, isolation can be achieved by making individual bulk regions of active material separated by an oxide layer [11]. Techniques to make the individual regions of active layer may vary slightly. Steps involved in forming individual bulk regions of active layer start by oxidizing the n – type silicon. This oxide layer is patterned by selective dry etch to have a "V" shape silicon anisotropic profile as shown in Figure 4.12 (b). Following the silicon dry etch, the mask i.e. SiO_2 is removed using HF. The bare patterned silicon wafer is then doped with n – type impurity. This will result in the formation of a strongly n – type layer across the wafer. This layer may be used for low resistance Ohmic contacts. Oxide is grown over the silicon wafer and then a polycrystalline silicon layer 250 – 500 μm is deposited over the oxide

layer. The oxide layer now acts as an insulator. The other side of the wafer is thinned, so as to achieve the structure as shown in the Figure 4.12 (e). A critical step involved in oxide isolation is considerable thinning of the wafer to achieve the isolated active regions [2].

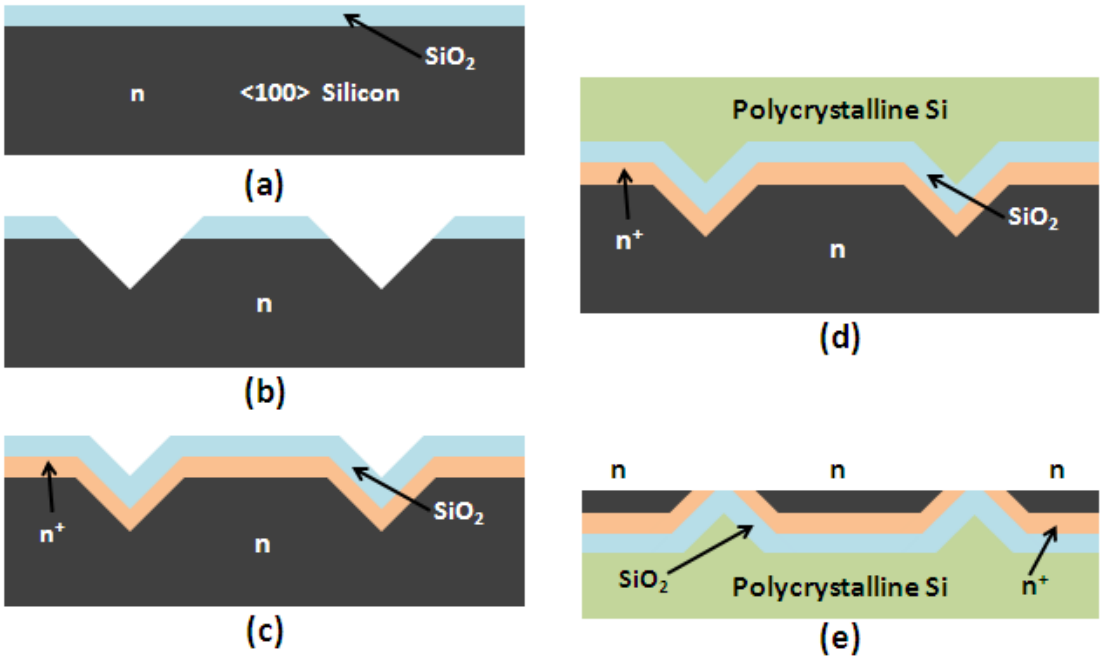


Figure 4.18: Oxide isolation scheme.

4.5 Device Isolation for Surface Gated Photo-Detector

The isolation structure in surface gated photo detectors is a 10 µm deep isolation trench all around the device. This may also considerably reduce unwanted flow of the signal that contributes to background noise.

4.6 References

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Chapter 5

Single Gate Silicon p-i-n Photodiodes

5. Introduction

In this chapter silicon-based lateral p-i-n junction devices for light sensing applications are described. These devices were based on MOS-architecture and, therefore, had a gate for controlling their electrical operating point. Device fabrication is described in brief, followed by a description of the device's electrical and optoelectronic properties including current-voltage (I-V) characteristics, optical characteristics and noise measurements. These devices showed good linearity and high optical responsivity for visible red and blue wavelengths. These devices, in single gate configurations, exhibited high sensitivity to UV light as well. The associated gate can be used to control the quiescent operating point thus making it easy to interface the detector with ordinary MOSFETs.

Junction diodes are widely used for sensing light and ionizing radiation in many different applications. Many different types of semiconductor light detectors are available in both discrete and integrated forms. As no one device can satisfy the many requirements that exist so several different types of optical detectors have been developed to date [1]. A variety of devices, suitable for particular uses are commercially available. Some provide high sensitivity whereas others are suitable for high speed operation. Avalanche photodiodes (APDs) [2] and p-i-n diodes [3, 4] are respective examples of these types.

Often such diodes are interfaced with transistors for various circuit requirements. When this combination is needed for integrated circuits then a problem arises because most contemporary ICs are based on Complimentary Metal Oxide Semiconductor (CMOS) technology which does not accommodate light sensing diodes very readily. This restriction is relaxed when one deals with compound semiconductor devices where good performance can be obtained from phototransistors based on direct band gap materials such as InGaAs [5] or AlGaAs [6, 7]. Present generation of so-called CMOS imagers contain embedded junction diodes [8] but their fabrication entails significant changes in procedure compared to those utilised for making CMOS logic chips. This makes CMOS imaging integrated circuits into a specialized product that not all fabs are able to handle.

This transistor-like light sensing device is fully compatible with conventional CMOS processing techniques, enabling light sensors to be easily integrated with biasing and signal processing transistors on monolithic ICs. In addition, due to its lateral doping profile, it features a depletion region that is located at the top of the device, endowing it with very high responsivity and much superior response to short wavelength visible radiation than is the case with ordinary silicon photodiodes with vertical doping profiles [9]. Such a device can replace photodetectors made from silicon carbide and gallium nitride for sensing radiation below 450 nm wavelength, in applications where speed of response is not important. Furthermore, the lateral architecture exposing the depletion layer at the surface also allows for the possibility of integrating other materials and structures with such a device; enabling the fabrication of novel types of sensors such as polarization sensitive detectors and monolithically integrated visible / UV radiation detector for battlefield applications. The later can be accomplished using a short wavelength pass filter material coating on alternate p-i-n photo-detectors in an array of such detectors as referred in Figure 8.3.

Single gate photodiodes with two variations were fabricated in this work. Comprehensive fabrication details are given in the device fabrication chapter. The lateral p-i-n junction architecture detects the light in these devices whereas the insulated gate, when properly biased, manages the current flow through the device. The response of the device changes with the change in dimension and placement of insulated gate. To understand such devices two different type of devices were fabricated with varying gate architectures. Other fabrication details and device processing conditions were the same for both devices. In each case, the gate

was placed within the 32 μm region between the two electrodes. Variation one involved the placement of the 20 μm long MOS gate offset to anode in the 32 μm lightly p-doped (π) region. In this design a gap of 2 μm and 10 μm existed in between the anode and the gate and the cathode and the gate, respectively. This variation will be referred to as "offset single gate device". The second variation had a 12 μm long partial gate in between the 32 μm 'π' region. The gate was placed at equal distance (10 μm) from the anode and the cathode within the 32 μm gap between these electrodes. In the rest of the discussion, this device will be named "Centre single gate device". Later sections of this chapter will separately deal with the electrical and optical behaviour of these two set of devices.

One can understand the transition of pn-junction diode to conventional vertical p-i-n junction diode to achieve higher sensitivity and lower junction capacitance on account of large depletion region. The vertical architecture with buried depletion region enhances the sensitivity of p-i-n junction diodes, but still the short wavelength photons are absorbed in the inactive silicon region, minimizing its sensitivity to short wavelengths. Lateral p-i-n junction photo-detector can be considered as a step forward in this evolution. This design enhances the responsivity of silicon to shorter wavelengths. In order to make a gated lateral p-i-n photo-detector, an insulated gate is added at the top of the near-intrinsic π region. Due to the presence of this MOS gate, single offset gate lateral p-i-n photo-detector appears as a transistor to the surrounding circuitry.

In offset single gate lateral p-i-n photo-detector, light mainly penetrates the device through the gap between the gate and the cathode. Here the gate is negatively biased with respect to the source, to accumulate holes underneath the gate. This accumulation layer electrically shrinks the device length by extending the p^+ region under the gate and thus controls the current flowing through the device. The offset device still appears as a transistor to the surrounding circuitry. A further step in the transition of lateral p-i-n photo-detector is the placement of a MOS gate in the centre of the π region. This then becomes a centre single gate lateral p-i-n photo-detector. In this architecture, light is incident on both sides of the gate. Unlike the offset gate architecture, the gate is biased positively with reference to the source in order to have an inversion layer underneath the gate. As the π region is a lightly p doped region, so a very thin inversion layer will appear under the gate. The formation of the inversion layer controls the flow of current through the device by suppressing the possibility of holes recombining with

electrons in the π region, giving rise to more current flowing through the device. Both devices have varying optical and electrical characteristics. These features are presented in this chapter and discussed in detail.

5.1. p-i-n Junction Diode

Pn-junction diodes are sensitive light detectors but their sensitivity can be further enhanced by increasing the extent of their depletion layer. This is usually done by inserting a near-intrinsic layer between the n and p regions. Such p-i-n junction diodes enable higher sensitivity on account of having a much larger depletion volume where the built-in field can separate electron-hole pairs (EHPs) formed by photon absorption. Conventional p-i-n diodes are vertical devices as shown in Figure 5.1, where the different regions are produced in a vertical stack either through doping or epitaxy.

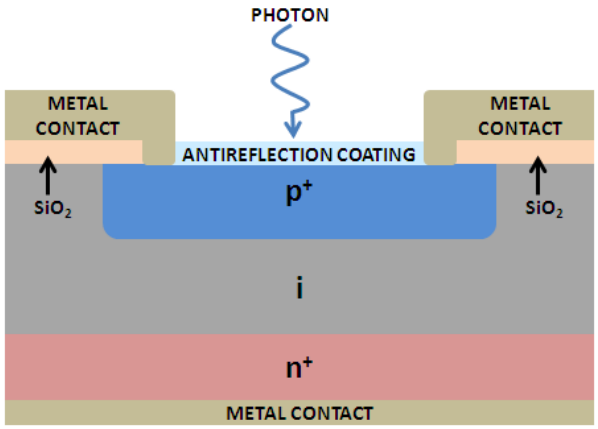


Figure 5.1: Conventional vertical p-i-n diode

5.2. Offset Single Gate Lateral p-i-n Photodiode

The device described here, in contrast, had a horizontal distribution of p, i and n regions. The 'i' or intrinsic region was in fact a low doping concentration p-type region and thus can also be referred to as a 'π' region. In this section, the structure of the offset-gate device, its operating mechanism, experimental setup and its electrical and optical characteristics are described.

5.2.1. Device Design

The device described here, was fabricated with a lightly p doped near-intrinsic 'π' type substrate. The n^+ and p^+ regions were thermally diffused such that the 32 μm wide near intrinsic 'π' region was left in between in its original doping concentration. This 'π' region had thermally grown SiO_2 and a partial gate over it, which makes the p-i-n photodiode a gated lateral p-i-n photo-detector. The doping levels of the n^+ and p^+ contact regions were 1.48×10^{18} cm^{-3} and 6.38×10^{17} cm^{-3}, respectively. The doping level of the intrinsic 'π' region was 1.94×10^{13} cm^{-3}. It should also be noted here that the doped regions were formed by localized diffusion doping into float zone silicon material with a resistivity of $4\ k\Omega - cm$. It is pertinent to mention here that the use of float zone silicon is not essential for making this type of device as the dopant concentration in the carrier drift region can be adjusted by an appropriate ion implantation step. This can further optimize the wavelength response of the device [10]. Dopant compensation through implantation does increase recombination trap centre density somewhat and leads to a reduction in carrier lifetime [11] and thus a concomitant reduction in photocurrent.

From standard pn-junction theory, the device had a depletion layer thickness of 6.81 μm, almost all of it lying in the 'π' region. Figure 5.2 shows three dimensional schematic view of device geometry showing the gate and contact regions.

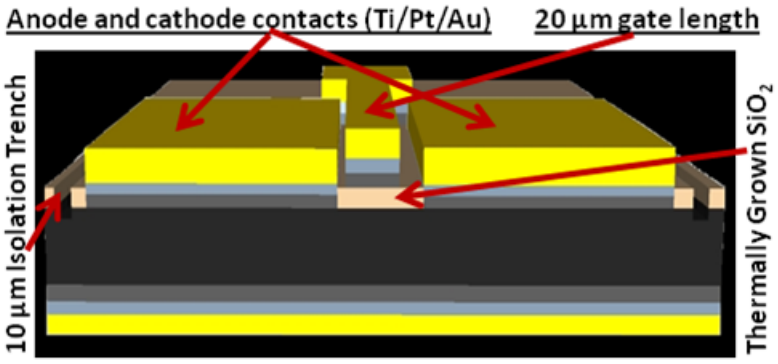


Figure 5.2: Three dimensional schematic view of device geometry showing the gate and contact regions.

The vertical cross-section of the device resembles that of a MOSFET. In contrast to earlier attempts at making photo-MOSFETs this device did not utilise transparent gates [12, 13] or annular electrodes [14-17]. The gate stack was formed by dry oxidation of the silicon surface at 1135 ℃ followed by Ti/Pt/Au deposition as the tri-layer gate metal. The top gold layer only

served as a device contact pad and can be omitted in a CMOS process flow as the presence of gold is not essential to the functioning of this device and can indeed be detrimental in the fabrication of integrated circuits.

The SiO_2 gate dielectric thickness was 50 nm. The gate was 20 μm long within the 32 μm gap between the two electrodes; resulting in a 37.5% fill factor. The gate was offset such that it was closer to the p-doped contact region than it was to the n-doped region. These devices were fabricated in an array of 4 x 5 devices. The devices also had a 10 μm wide and 10 μm deep etched isolation trenches all around them.

5.2.2. Operating Mechanism and Characteristics

The central idea behind the device is that light is detected by the p-i-n structure where the depletion region electric field between the n and i regions separates the electron hole pairs formed. Accordingly, the p-i-n structure was kept under reverse bias. Due to the use of very lightly doped float zone silicon employed in device fabrication, the depletion region had a large lateral extent which helped in increasing its sensitivity to light. Almost the entire depletion region existed in the 'π' region of the device adjacent to the cathode, as seen in Figure 5.3. Its width was affected by the lateral drain to source bias (V_{DS}), across the structure, in accordance with the relation:

$$\boldsymbol{W = \sqrt{\left[\frac{2\varepsilon_o\varepsilon_{si}}{q}\left\{\frac{(N_A+N_D)}{(N_AN_D)}\right\}(V_{bi}-V_{DS})\right]}} \qquad 5.1$$

Where ε_{si} is the semiconductor dielectric constant, ε_o is the permittivity of free space, q is charge of electron, N_A is acceptor concentration, N_D is donor concentration, V_{bi} is built in voltage in the depletion region and V_{DS} is the applied drain to source voltage. The heavily n-doped and p-doped regions that form the two lateral electrodes of the device are similar to the cathode and anode contacts of a junction diode but will be referred to as drain and source, respectively, in this description. This is because the overall structure and apparent functioning of the device resembles to that of a MOSFET very closely.

The carriers coming out of the depletion region, drift under the source-drain field and are collected by the cathode and the anode. The MOS gate adjacent to the p-type electrode controlled the amount of current flowing through the device and thus makes the device appear

as a transistor to the surrounding circuitry. Figure 5.3 shows a schematic diagram of the device showing both the lateral doping profile and the placement of the MOS gate.

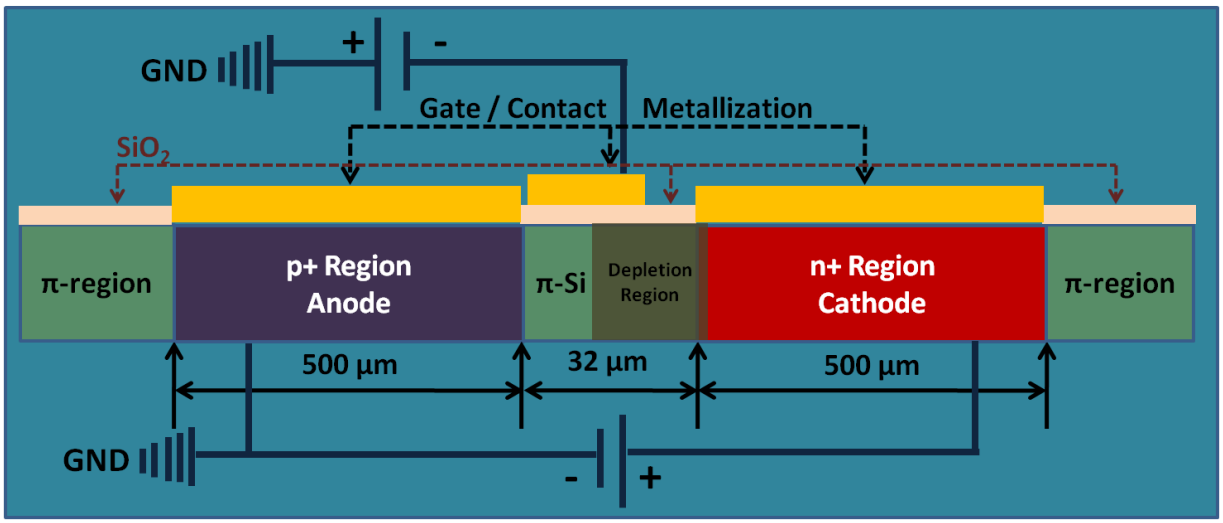
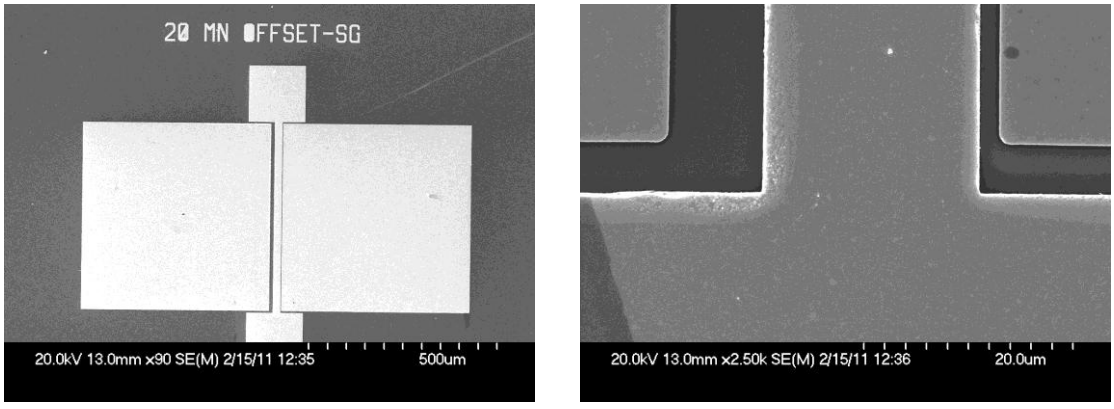


Figure 5.3: Schematic diagram of the offset single gate photo-detector showing both the lateral doping profile and the placement of the MOS gate

Figure 5.4 (a) shows an SEM micrograph of the actual offset single gate photodiode where the anode (source) and cathode (drain) pads can be seen as well as the gate contact pad at the top and bottom. In Figure 5.4 (b) an SEM micrograph of the highlighted gate region at the gate contact end is shown. In this figure it can be seen that the gate is offset towards the source rather than the drain.



(a) (b)

Figure 5.4: (a) SEM micrograph of the offset single gate photo detector (b) SEM micrograph on the highlighted gate region.

This configuration makes this device very different from ordinary p-i-n diodes so that it is much more suited for detecting low light intensities over a large wavelength range while its

speed of operation is significantly reduced. This geometry also allows one to investigate the effect of placing secondary structures, such as gates or gratings, on the intrinsic region. In fact, the device described here had an integrated MOS gate structure to enable the control of current flowing through the device, independent of any photocurrent. This can be seen in Figure 5.7, where in absence of any light source, the gating action controls the flow of current through the device.

5.2.3. Experimental Setup

Devices were characterized using wafer probers and a number of different instrument setups. The current-voltage (IV) characteristics were measured with a Hewlett-Packard 4155B semiconductor parameter analyzer (SPA). Some of the optical measurements such as I_{DS} as a function of red and blue light intensity were also performed using SPA. Spectral responsivity measurements were performed with THR 1000 Monochromator using 51006180 grating from JOBIN YVON, whereas an SR530 lock in amplifier from Stanford research systems was used in this setup. It is imperative to mention here that, the responsivity values reported for single and dual gate devices have been calculated by taking into account, the entire near-intrinsic, π region in between the two electrodes, as the device sensing area. In order to measure the device response from optical to electrical domain with pulsed light, a function generator GFG-8216A from GW INSTEK and InfiniiVision DS05014A digital storage oscilloscope from Agilent Technologies were used to record the dataset. Noise measurements were taken with an Agilent 4395A network / spectrum / impedance analyzer.

5.2.4. Electrical Response

In this section the electrical response of the offset gate device is described. The forward and reverse characteristics of a lateral p-i-n photodiode and with gate bias are illustrated. A transconductance plot is shown which is derived from the $I_{DS} - V_{GS}$ graph.

5.2.4.1. Forward and Reverse Bias Characteristics

To examine the forward bias characteristics of gated lateral p-i-n diode, a few volts were applied across the lateral p-i-n structure, without taking into account its gated structure. A characteristic curve shown in Figure 5.5 is similar to the forward bias characteristics of an

ordinary diode. Here 0.8 V forward diode drop is observed in lateral p-i-n diode as against 0.7 V in normal pn-junction diode.

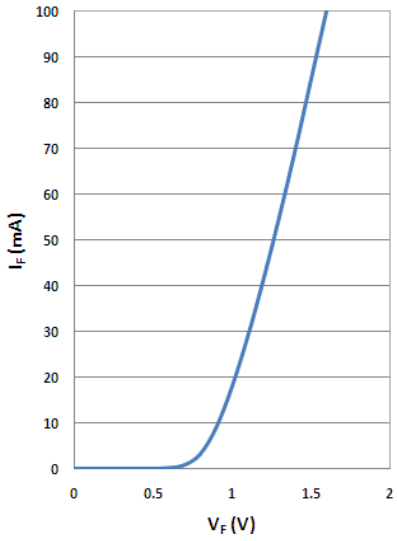


Figure 5.5: Forward bias characteristics of offset p-i-n photo detector.

A reverse bias of a few volts was applied across the lateral p-i-n structure, as is usual with photodiodes. Reverse bias characteristics of a lateral p-i-n diode are shown in Figure 5.6, where a dark current of 4.6 μA is seen at V_{DS} = 15 V. The high value of dark current is due to the leakage of current below the doped regions. This can be minimized by fabricating the device using silicon-on-insulator (SOI) material.

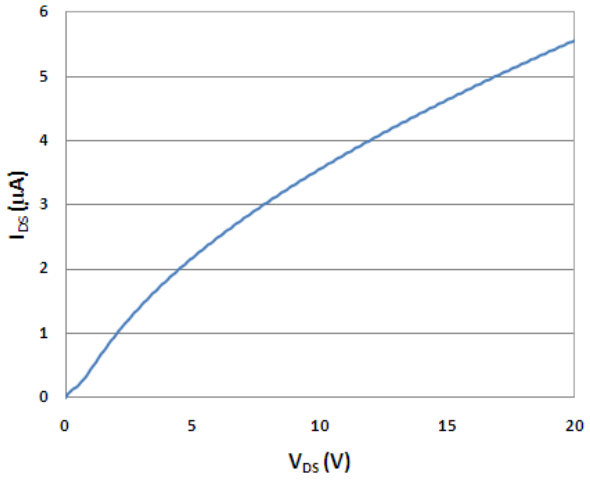


Figure 5.6: Reverse bias characteristics (dark current) of an offset p-i-n diode.

5.2.4.2. Current – voltage (I-V) Characteristics

So far the biasing conditions in isolated diode configuration has been described. In order To understand the hybrid characteristics, its lateral diode structure and the vertical MOS transistor structure have to be biased simultaneously. In order to do this, the gate was biased with a negative voltage referenced to the source (which was at the ground potential). This caused the region underneath the gate to accumulate holes. The accumulated holes had the effect of extending the anode region laterally so that the electrical width of the device was reduced and its effective conductivity was greatly enhanced. This is seen in Figure 5.7 which depicts the current-voltage characteristics of the device. It is interesting to note that what appear as conventional transistor characteristics are simply the reverse-biased characteristics of a diode. The different curves here are for the device operating with different gate biases. With increasing negative gate bias, more current flows through the device and the characteristics shift upwards.

Here it is to be noted that at 0 V V_{DS} and 0 V V_{GS}, the output current is 0 A. This is because the drift current is controlled by the electric field due to applied V_{DS}. Therefore ideally, at 0 V V_{DS} and higher (negative) gate bias values the output current should be zero. Whereas in Figure 5.7 25 µA output current is flowing at -5 V V_{GS} and 0 V V_{DS}, this offset in output current at higher gate bias values is likely to be the contribution from the gate leakage current. This contribution of gate leakage current can be minimized by careful handling at the oxide formation step while fabricating the MOSFETs. It however cannot be reduced to zero even, in commercial fabrication facilities where state of the art equipment is available.

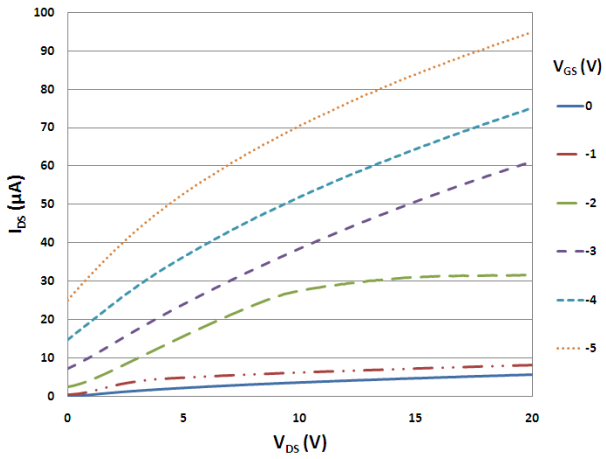


Figure 5.7: Current-voltage (I-V) characteristics of the offset gate device at different gate voltages.

5.2.4.3. Transconductance

A transconductance curve can be derived from $I_{DS} - V_{GS}$ measurements and is shown in Figure 5.8. This particular curve corresponds to a drain-source bias of 10 volts. The transconductance at V_{GS} = -15 V was 0.08 mA/V. These plots show that the device appears as a transistor as far as its terminal behaviour is concerned, although with unusual biasing polarities. For this reason we also refer to the anode and cathode terminals as source and drain, respectively.

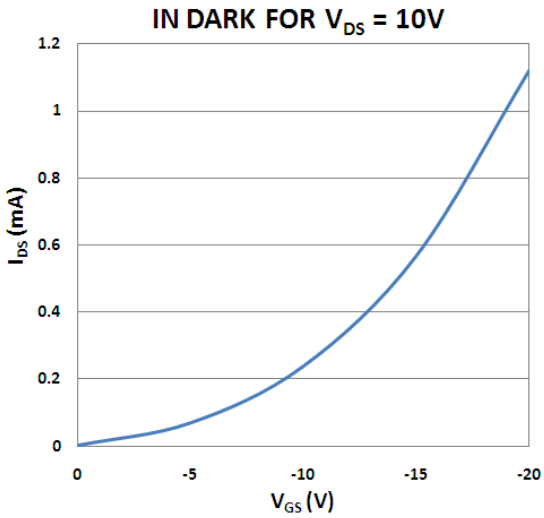


Figure 5.8: I_{DS} –V_{DS} plot of the device for V_{DS} = 10 V. This was taken in the dark.

The transistor-like behaviour makes it easy to accommodate this device in transistorized circuits. Conventional circuit design techniques can be employed for this purpose. Moreover, gated p-i-n devices are much simpler to fabricate and use as compared to recently demonstrated infrared-detecting silicon nano-MOSFETs [18]. The drain to source current of this device in the linear region can be related to drain and gate voltages by the equation:

$$\boldsymbol{I_{DS}} = {}^{(\boldsymbol{e\, C_{OX} V_G \mu_P V_{DS}})}/_{\boldsymbol{d}} \qquad 5.2$$

Where, I_{DS} is the drain to source current, C_{OX} is the gate (oxide) capacitance, V_G is the applied gate voltage, V_{DS} is drain to source voltage and d is the distance between source and drain. This relation holds once accumulation charge density underneath the gate has reached the

same magnitude as the dopant density in the p^+ region so that the p^+ region becomes effectively extended under the gate.

5.2.5. Optical Response

Optical measurements were taken with red and blue Light Emitting Diodes (LEDs) centred at 630nm and 480 nm wavelengths, respectively, as sources of illumination. The spectra of red and blue Light Emitting Diodes are shown in Figure 5.9 (a) and (b), respectively.

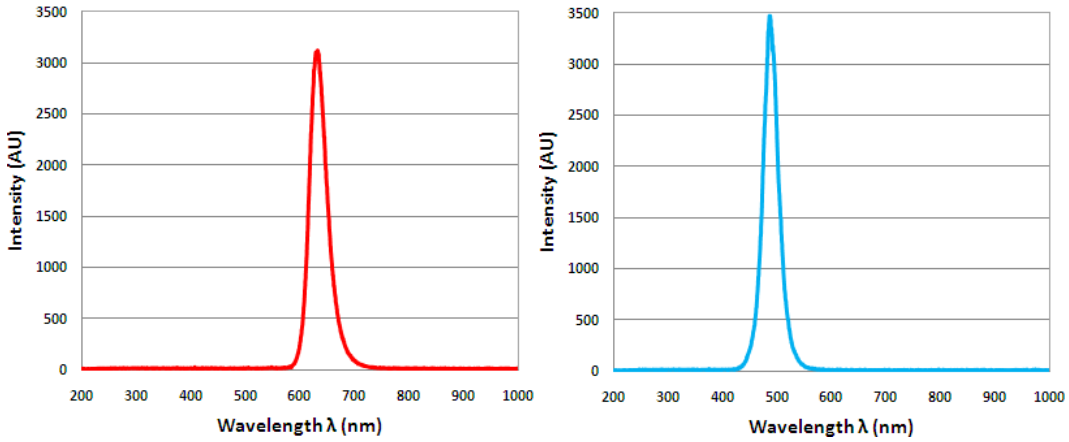
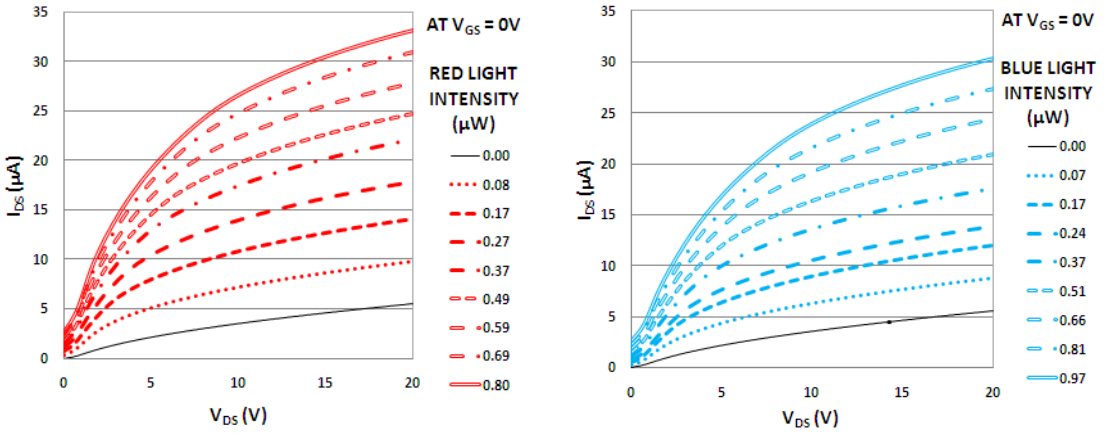


Figure 5.9: Spectrum of red LED centred at 630 nm wavelength (b) Spectrum of blue LED centred at 480 nm wavelength.

The first set of measurements deals with the device response with red and blue light illuminations at 0 V gate-source bias i.e. using only its lateral p-i-n diode structure. Whereas, the second set of measurements was based on its hybrid diode-transistor structure. These measurements show the device response with similar red and blue light intensity at different gate-source bias values. The response of the device with red and blue lights shows similar behaviour, however, a slightly reduced output current was seen with blue light as compared to red light, which is usual with silicon detectors. These gated p-i-n diodes have shown better sensitivity to blue light than ordinary p-i-n diodes with vertical doping profile. The optical response of the device at normal incidence with red and blue wavelength at different light intensities is shown in Figure 5.10 (a) and (b). The response of the device, with different red and blue light intensities is very well behaved. This indicates that the device can be utilized in principle as an optically switched transistor.

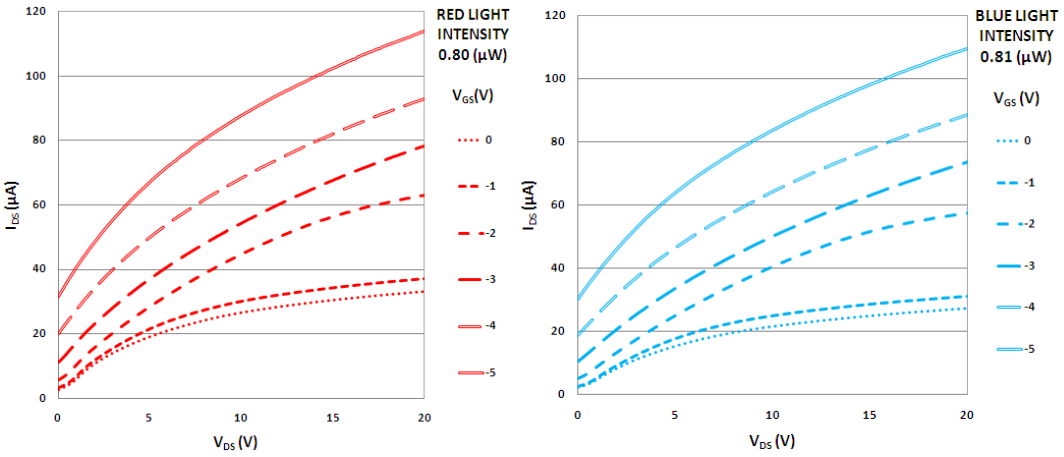


(a) (b)

Figure 5.10: Optical response of the device with (a) red and (b) blue light at 0 V V_{GS}.

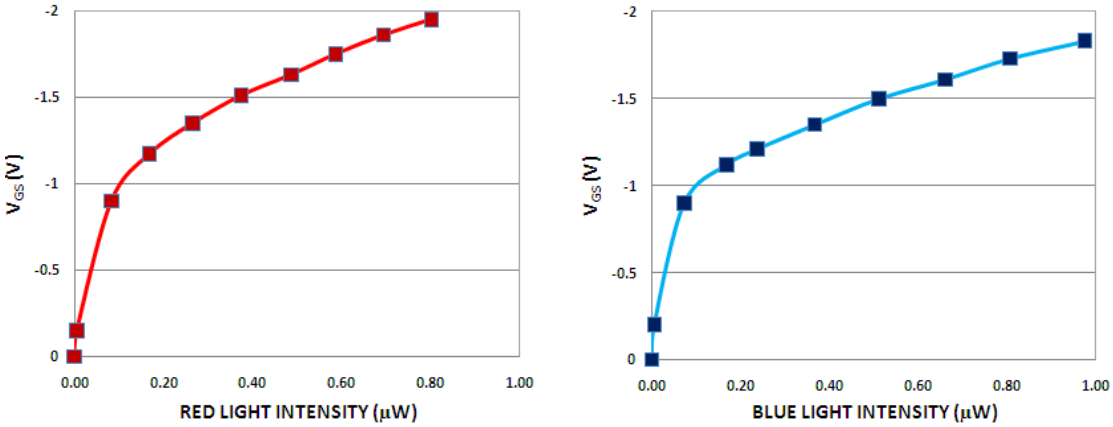
An increase in device response is seen with increasing light intensity as shown in Figure 5.10. It clearly shows that the current flowing through the device is controlled by the incident light. This light-induced response of the device is better behaved than the response of the device when the gate-source bias is used as a parameter to control the current flow through the device.

The device behaviour in its transistorized configuration where the gate-source bias is applied to control the current through the device is shown in Figure 5.11 (a) and (b) for red and blue lights of similar fixed intensity, respectively. Here the current through the device was controlled by applying different gate-source biases. The spectrum of the light source used for illumination is the same as shown in Figure 5.9. Here two parameters i.e. the gate-source bias and fixed light intensity, were used to control the current through the device. In fact, the incident light contributes to the output current of the device as if some gate bias was applied to the device. This correlation of light intensity to gate-source bias is shown in Figure 5.12 (a) and (b) for red and blue light, respectively.



(a) (b)

Figure 5.11: Transistorized optical measurements with (a) fixed red light intensity and (b) fixed blue light intensity.



(a) (b)

Figure 5.12: Light intensity to gate-source bias correlation in offset single gate p-i-n photo-detector. (a) with red light (b) with blue light.

In order to meaningfully compare the device response with red and blue illumination, the optical response of the hybrid device in red and blue light is plotted in Figure 5.13. The optical output characteristics of the device have been plotted at different incident light intensities here. The lowest curve (continuous line) is the response of the device in dark, for reference. Dotted lines and dashed lines represent the response of the device in red and blue light. Ellipses indicate pairs of measurements at similar red and blue light intensities.

Very good sensitivity to blue light is evident from these plots. The responsivity of the offset gate device to red and blue light centred at 630 nm and 480 nm was 12.9 A/W and 10.15 A/W, respectively (at V_{DS} = 20 V and V_{GS} = 0 V). These values are higher than those for commercial silicon photodiodes, such as the BPX65 from Centronics. Such high values of responsivity have been predicted in lateral p-i-n junction photodiodes recently by Yun Zeng and colleagues

[19]. These large values arise because the depletion region is right at the top of the device so that incident photons do not have to traverse a region of 'inactive' silicon before reaching the space charge region where electrons and holes they form can be separated effectively.

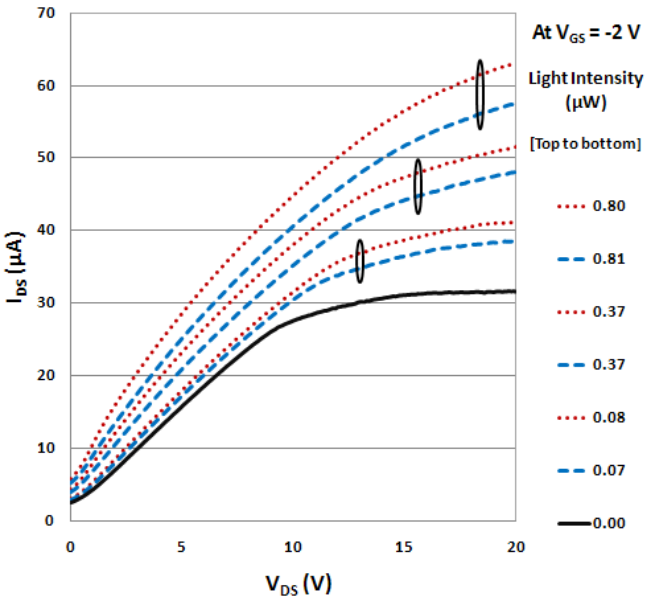


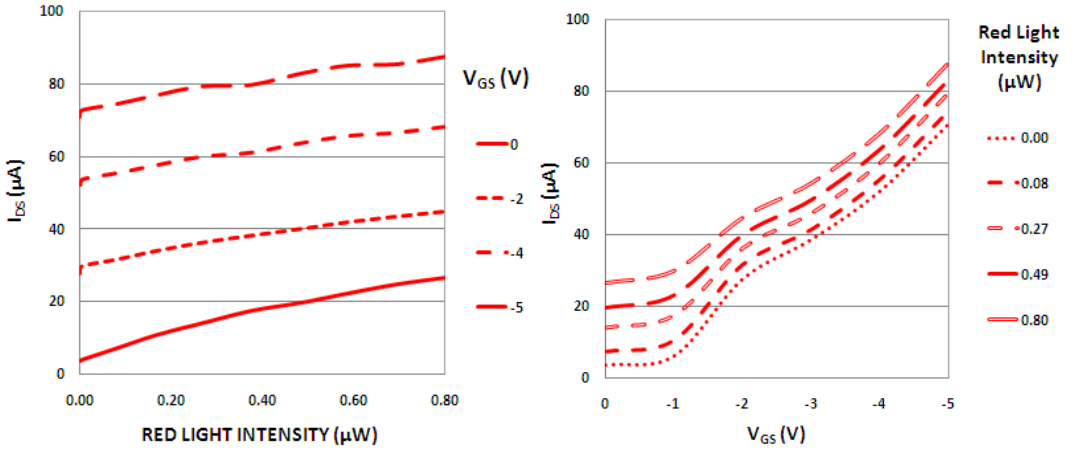
Figure 5.13: Optical output characteristics of the device, taken at V_{GS} = -2 V and at various red and blue light powers.

The fact that there is only 21.3% fall in responsivity in going from the red region to the blue region attests to the remarkable blue sensitivity of this device as commercial devices often show a decrease of 40% or more in going from the red region to the blue region. The change in output current in going from red to blue illumination, at the stated biasing conditions and for 0.08 μW incident optical power, was even smaller at 8.6%. This shows that because of the presence of depletion region at the surface of the device and due to the lateral doping profile, the sensitivity to blue light is greatly enhanced over devices with buried depletion regions. Other types of silicon-based detectors have to rely on back-thinning techniques and back illumination to achieve similar results [20].

5.2.5.1. Optical and Electrical Transfer Characteristics

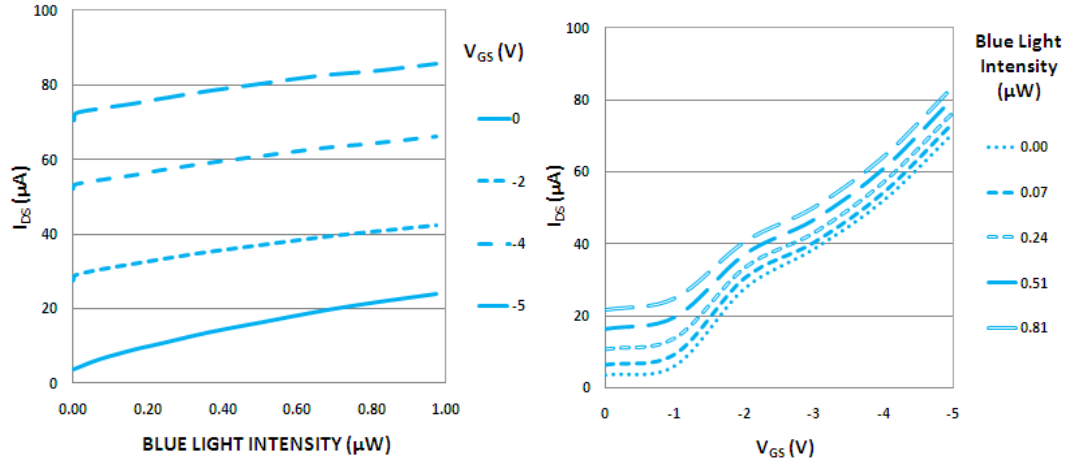
The almost linear optical transfer characteristics imply that the device introduces very little non-linear distortion when transducing signals from the optical to the electrical domain. Optical and electrical transfer characteristics are shown in Figure 5.14 (a) and (b) and Figure

5.15 (a) and (b) for red and blue light, respectively. We have verified this by building circuit based on the offset gate device.



(a) (b)

Figure 5.14: (a) Optical transfer characteristics and (b) Electrical transfer characteristics of the device.



(a) (b)

Figure 5.15: (a) Optical transfer characteristics and (b) Electrical transfer characteristics of the device at different blue light intensities.

Tests of the switching response of the device with pulsed red light have shown very good linearity in optical-to-electrical conversion as shown in Figure 5.16. Here the lower trace is the optical driving signal from a red LED and the upper trace is the output voltage from the device. The signal inversion seen is the result of the common-source (CS) biasing circuit used with the transistor-like detector.

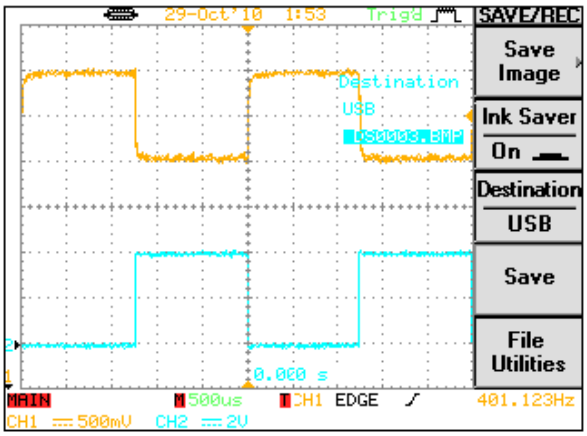


Figure 5.16: Optical to electrical conversion exhibited by the device with pulsed red light.

5.2.5.2. Spectral Responsivity

The complete responsivity curve of the device for the 400 to 1100 nm range appears in Figure 5.17. This also shows the responsivity of a typical commercial silicon photodiode (scaled up 72 times), for comparison.

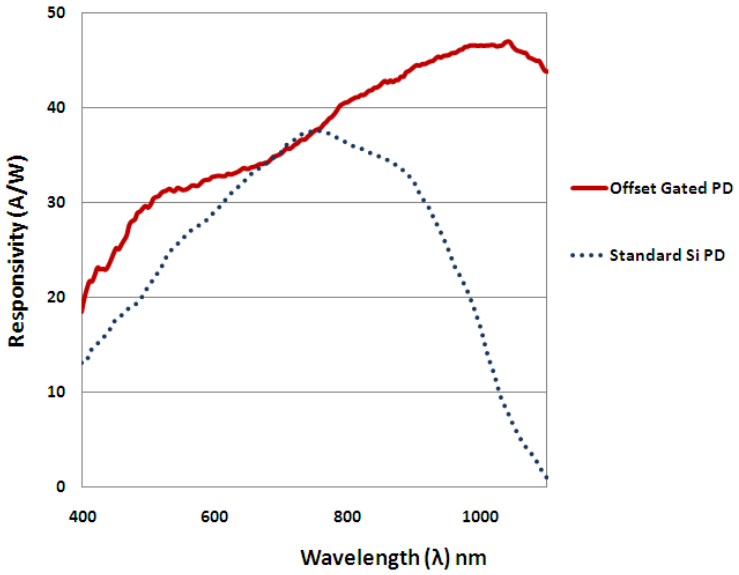


Figure 5.17: Spectral responsivity of the single gate devices for the 400 to 1100 nm range. The dotted line is the responsivity of a typical commercial silicon photodiode. Part No. DSS-SG020A, Manufacturer: Electro-Optical Systems Inc.

Furthermore, the device was tested with ultraviolet (UV) radiation from mercury discharge lamps and found much enhanced sensitivity to radiation of wavelengths less than 400 nm. Figure 5.18 shows plots of these measurements taken at V_{GS} = -1 V. The top curve is the

response with both visible and UV radiation incident on the device. The middle curve shows response with only UV radiation (visible wavelengths were cut off by a short wavelength pass filter). The spectra of UV radiation with and without filter are shown in Figure 5.19. The bottom curve shows the response in dark for reference. These measurements yield a UV responsivity of 0.15 A/W at a wavelength of 313 nm (at V_{DS} = 15 V). These UV responsivity values compares very favourably with performance parameters measured with GaN- and SiC-based p-i-n photodetectors [21] where very similar figures for UV responsivity have been quoted. Thus, whereas, these silicon-based devices are not solar blind they do approach the responsivity of devices made from wide direct band-gap semiconductors very closely and can detect radiation in UV-A, UV-B and UV-C bands. It thus appears that the surface depletion layer configuration of these detectors is able to utilise the above-unity quantum yield of UV photons very effectively [22]. Using the relationship between responsivity and internal quantum efficiency at different wavelengths [21], a value of 69% for quantum efficiency in the red region can also be obtained.

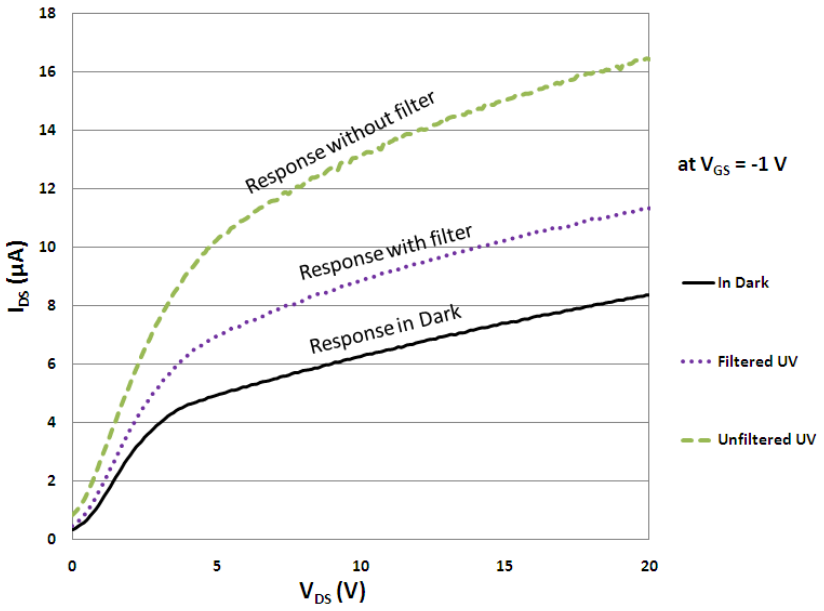
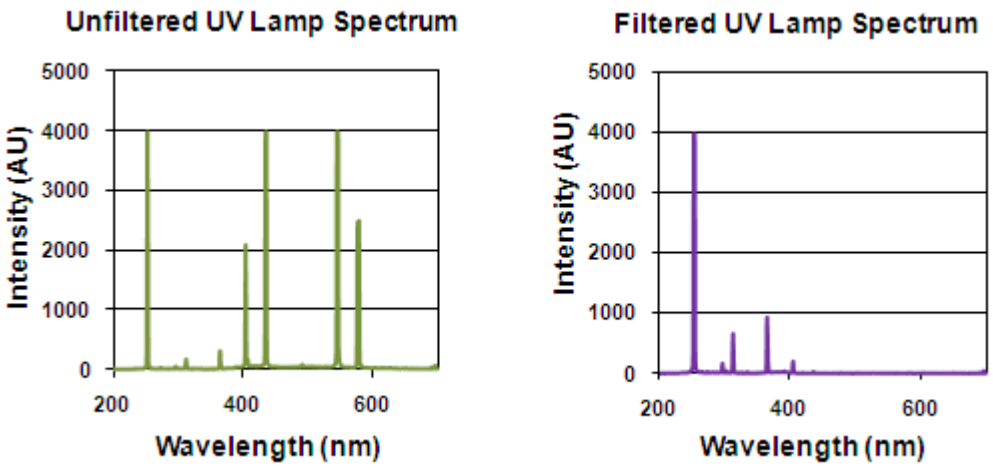


Figure 5.18: Optical output characteristics of the device for UV radiation. Data taken at V_{GS} = -1 V.



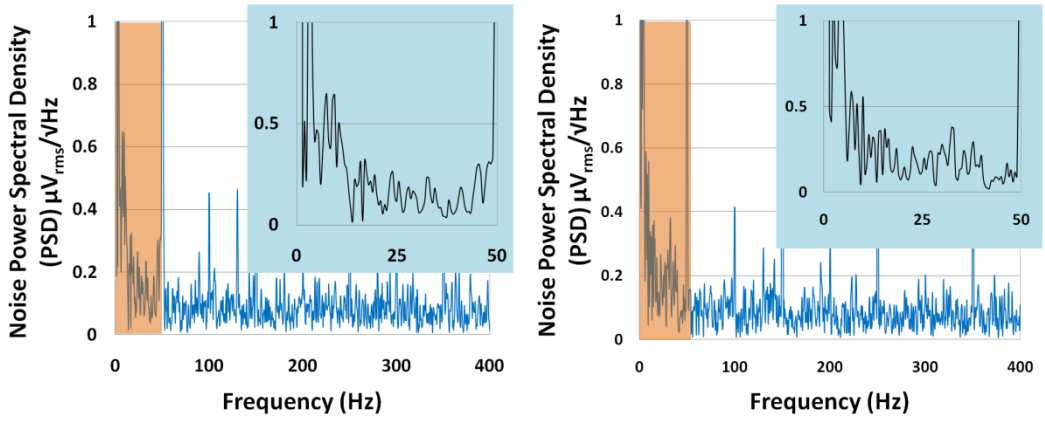
(a) (b)

Figure 5.19: Spectra of illuminating radiation without and with short wavelength pass filter are shown in (a) and (b), respectively.

It is to be noted that the lateral structure reduces the junction capacitance but increases the carrier transit time. This can be improved by shrinking the device. In its current form the device showed a 3 dB response at around 230 kHz. This is enough for many applications where steady or low frequency pulsed light detection is required.

5.2.6. Noise Measurements

The top surface location of the depletion layer in this device resulted in a higher level of dark current (Figure 5.6) but no excessive noise compared to what a buried depletion layer device would produce. The amount of dark current at a typical biasing voltage of V_{DS} = 15 V (in the absence of any gate voltage) was 4.6 μA. We performed power spectral density measurement of the device at V_{DS} = 10 V and different gate bias points and found average noise voltages of only a few $nV_{rms}/\sqrt{Hz}$. Figure 5.20 shows noise measurements for an offset gated p-i-n photo-detector. It is to note that the inset shows the highlighted region of the main graph.



(a) (b)

Figure 5.20: Noise measurements of offset gate device with insets showing 1/f dependence of the pink highlighted section (a) at -6 V V_{GS}. (b) at 0 V V_{GS}.

It appears that the silicon-dioxide layer (lateral continuation of the gate dielectric) serves as a good passivation layer and is effective in reducing $Si-SiO_2$ interface noise [23, 24]. This device can be further improved if it is fabricated on silicon-on-insulator (SOI) material as that would eliminate the current that leaks from the region underneath the doped regions; thus reducing its dark current [19]. This is very much possible as other types of photodetectors have already been demonstrated in SOI material [25, 26].

5.3. Centre Single Gate Lateral p-i-n Photodiode

So far we have explored a diode-transistor hybrid device and used its gating action to electrically shrink the device and thus control its electrical operating point. The next variation was to fabricate a device with a partial MOS gate placed right in the centre of the lightly doped p region. The dimension of the gate was again 12 μm x 500 μm and it was placed in the centre, at equal distance from both electrodes. Again, this device had the features of both pn-junction diodes and MOSFETs as was the case with the variation described earlier. Here again, light acts as an additional control variable. This device can simplify both analogue and digital designs that have to employ light detectors. This device had shown wide spectral response and it was found to be suitable for light sensing from about 900 nm to less than 400 nm. It is particularly useful for applications such as light sensing in machine vision applications. Next sections will deal with the structure and optoelectronic characteristics of the centre single gate device.

5.3.1. Device Design

Similar to the previous case, the device described here consisted of a hybrid diode-MOS transistor structure. The lateral structure was that of a p-i-n diode whereas the vertical structure was that of a transistor with a partial gate i.e. a gate that covered only a part of the region between the source and drain. The different parts of the device have been identified on the schematic diagram in Figure 5.21.

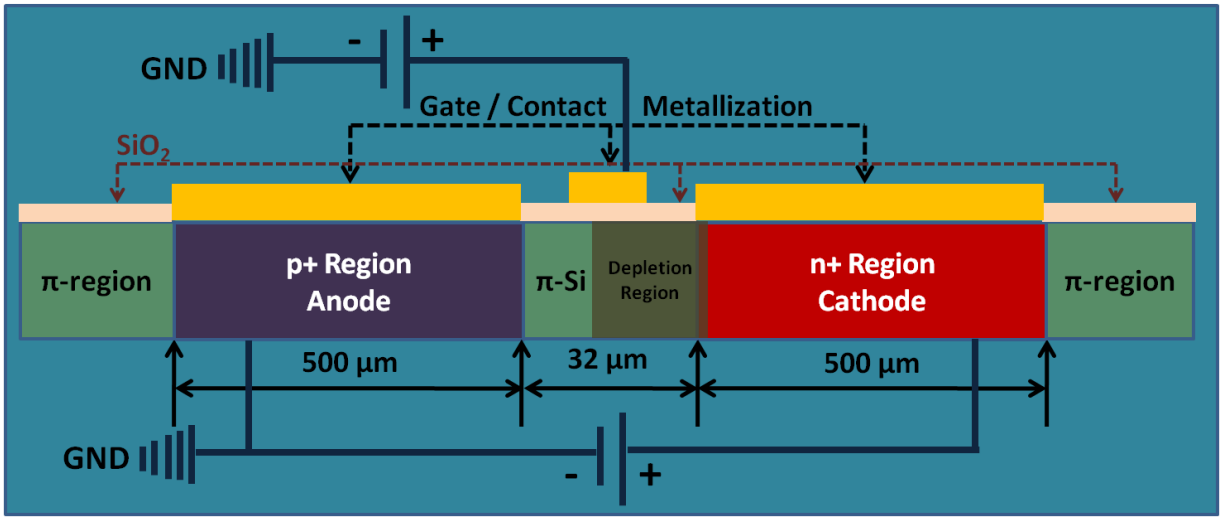


Figure 5.21: Schematic diagram of the centre single gate p-i-n photo-detector showing both the lateral doping profile and the placement of the MOS gate

The fabrication, processing and substrate details are exactly same as that of the offset single gate device described earlier, except for the dimensions and the placement of gate. The gate, in this case, was 12 µm, long within the 32 µm gap between the source and drain; resulting in a 62.5% fill factor. A 3D cross-section is shown in Figure 5.22, highlighting the placement and dimension of the gate and other contacts. It should be noted here that *Bhuwalka et al*, have described gated vertical p-i-n structures, for purely electronic applications [1].

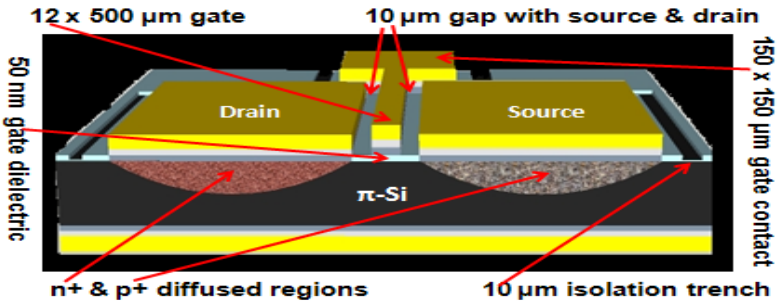


Figure 5.22: 3D labelled Cross-section of the centre single gate device.

The region between the source and drain was left in its low p-doped state. Geometrically, this *'π'* region had a width of 32 µm. The structure, therefore, resembled a lateral p-i-n junction diode with an extra-long 'i' region. The doping levels of the n^+, p^+ contacts and the lightly p doped near intrinsic *'π'* region, were 1.48×10^{18} cm^{-3}, 6.38×10^{17} cm^{-3} and 1.94×10^{13} cm^{-3}, respectively. As a result of this doping profile, a depletion layer thickness of 6.81 µm is produced; almost all of it lying in the 'π' region. An SEM micrograph of the fabricated device is shown in Figure 5.23.

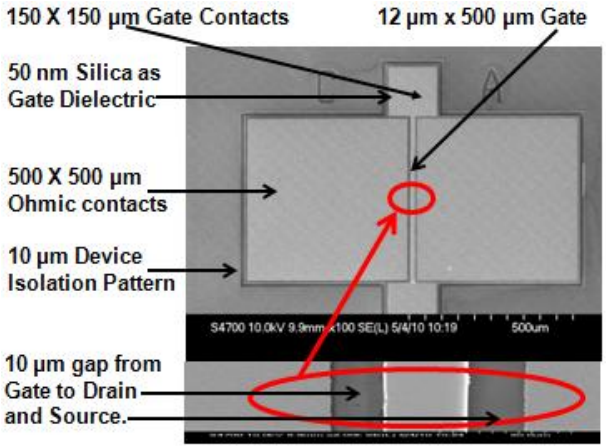


Figure 5.23: SEM micrograph of device with close-up view of the gate region in bottom.

In this case too, a layer of silicon-dioxide, 50 nm thick, was formed on the float zone silicon substrate by thermal growth in an oxygen atmosphere. A Ti/Pt/Au metal gate was deposited half-way through the 'i' region, on top of the SiO_2 layer. This design allowed incident light impinging on the device to enter the 'i' region on both sides of the gate through the transparent oxide layer. An etched isolation trench 10 µm deep surrounded each device to provide electrical isolation from any neighbouring devices.

5.3.2. Operating Mechanism and Characteristics

Several devices were fabricated on various pieces of float zone silicon wafer material in arrays of 4 x 5 devices each. Devices were characterized using wafer probers and a number of different instrument setups. The current-voltage (IV) characteristics were measured with a Hewlett-Packard 4155B semiconductor parameter analyzer (SPA). Measurements were taken in the source-to-drain voltage range of 0 to 20 volts while gate voltages of 0, 10, 15 and 20 volts were successively applied. The voltage applied between the source and drain was such as to reverse bias the lateral p-i-n diode. In the absence of a gate bias a reverse leakage current of

4 μA at 15 V V_{DS} was observed. Plot showing reverse leakage current of centre single gate p-i-n photo-detector is shown in Figure 5.24.

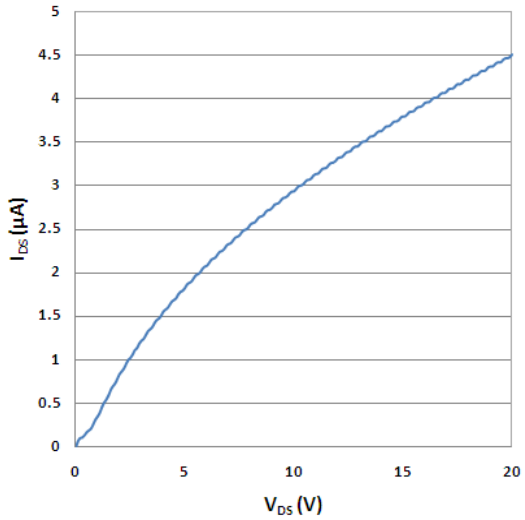


Figure 5.24: Reverse leakage current of centre single p-i-n photo-detector.

5.3.3. Electrical Response

In this section electrical response of the centre single gate device is described.

5.3.3.1. Current – Voltage (I-V) Characteristics

With increase in applied gate-source bias (positive with respect to the source), the electrical conductivity through the device was seen to increase. The mechanism for this appears to be the removal of minority electrons, due to gate action, from the region between the end of depletion layer and the source (on the right in Figure 5.22). Carrier recombination of holes, ejected out from the depletion region with the minority electrons in the π region was thus suppressed, giving rise to the drain current. Due to low background p-type doping of the float zone silicon used for these devices, minority electrons were significantly reduced from the π region underneath the positively biased gate. This accounts for the rapid rise in drain current with increase in gate-source bias. This is shown in Figure 5.25.

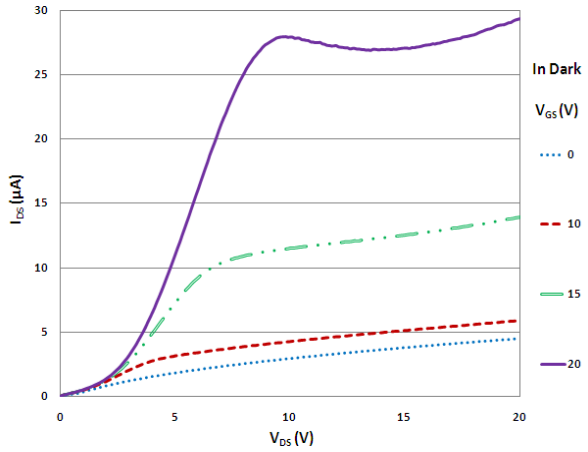


Figure 5.25: I_{DS}-V_{DS} (output) characteristics of the device with gate voltage as the parameter. Taken without an input light signal

5.3.3.2. Transconductance

A transconductance of 2.61 μA/V was seen at a V_{DS} value of 15 V. The $I_{DS} - V_{GS}$ characteristic in Figure 5.26 show that the terminal behaviour of the device is like that of a transistor.

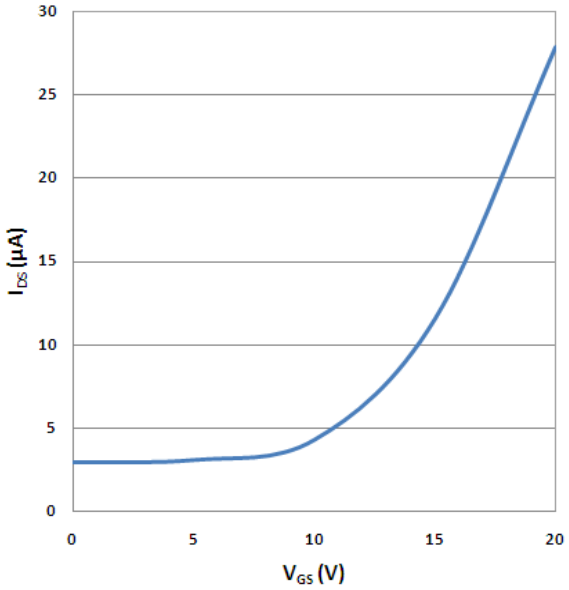


Figure 5.26: I_{DS}-V_{DS} characteristics of the centre single gate device at V_{DS} = 10V in the dark.

Device simulation gives an insight into the device operation, physical device modelling studies were also performed to verify the experimentally obtained characteristics. The simulator used for these simulations is Sentaurus, version E-2010.12, Synopsys. In the simulation process, the dimensions of the device and its analytical doping profile were

employed that match the measured data as shown in Figure 5.27. Simulation structure and doping profiles are illustrated in Figure 5.27. The simulation process utilizes the drift-diffusion model, which includes Poisson's equation and carrier continuity equations. It also employs doping-dependent interface and high field degradation mobility models. A raytracing model was used to determine the optical generation rate for the simulation process. Figure 5.28 (a) and (b) show simulated results of single centre gate device at different light intensities [diode measurements] (a) and at fixed light intensity with different gate bias values [transistor measurements]. The simulations were performed by Xingsheng Wang from device modelling group.

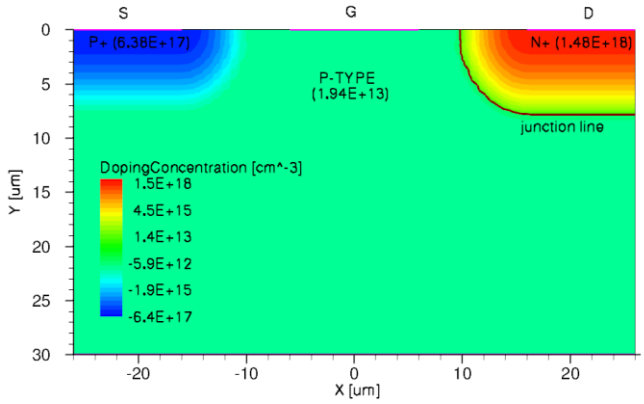
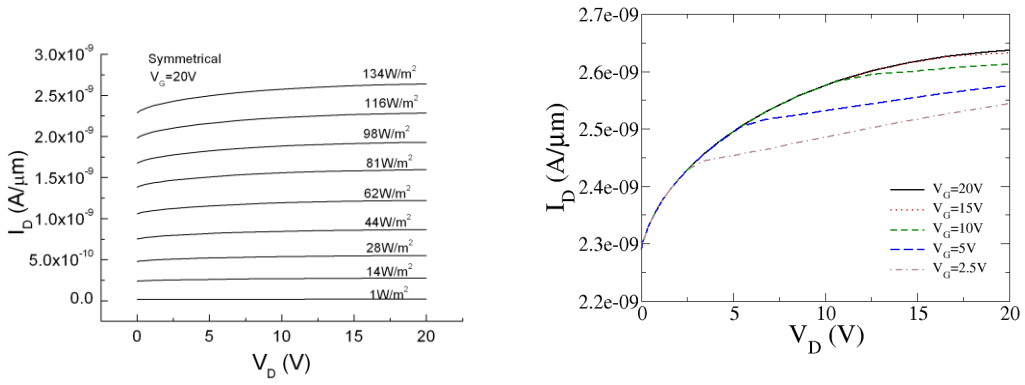


Figure 5.27: The simulation structure and doping profiles for the centre single gate device



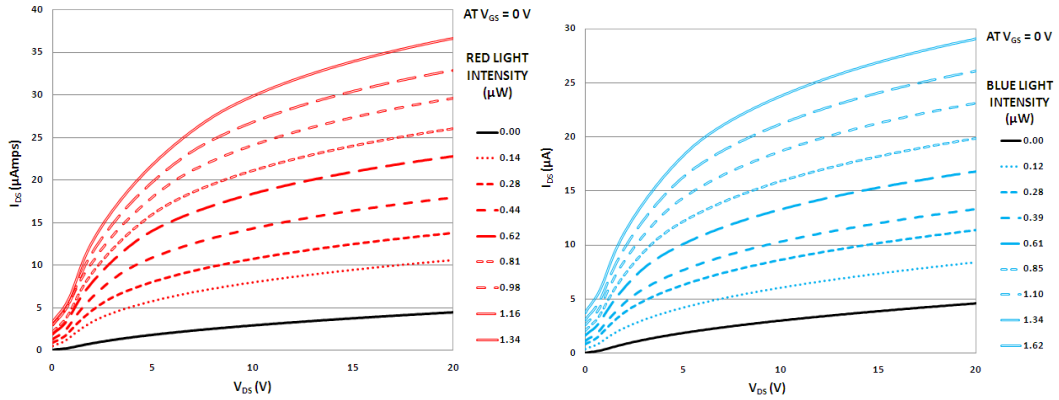
(a) (b)

Figure 5.28: Simulated result of single centre gate device (a) with different red light intensities (b) at fixed light intensity with different gate bias.

5.3.4. Optical Response

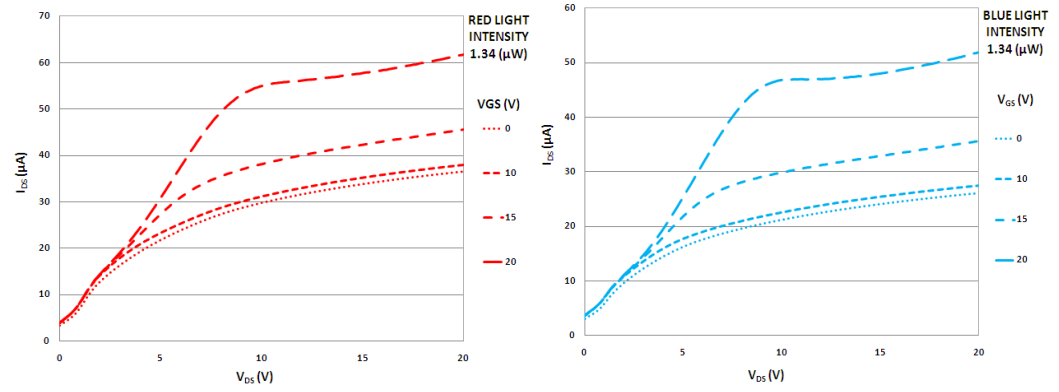
Similar to the offset single gate device, the centre single gate device can also be driven into saturation with an input light signal which has a similar but more well-behaved action than an

applied gate-source bias. Similar light sources and measurement setup, as were used for offset gate device, were used to measure the optical response of the centre single gate device. Optical response of the device with red and blue light was measured in two different sets of measurements. One accounts for diode measurements taking into account the lateral part of the device. Device response with red and blue light is shown in Figure 5.29 (a) and (b). The second set of optical measurements deals with the vertical MOSFET part i.e. $I_{DS} - V_{DS}$ characteristics with an input red and blue fixed light intensity. This is seen in Figure 5.30 (a) and (b). This shows the output characteristics with different gate bias values as the plot parameter.



(a) (b)

Figure 5.29: I_{DS}-V_{DS} (output) characteristics of the device with (a) red illumination. (b) blue illumination. In both cases optical power is the parameter here.



(a) (b)

Figure 5.30: I_{DS}-V_{DS} (output) characteristics of the device with gate voltage as the parameter taken with. (a) red light illumination. (b) blue light illumination.

Similar to the offset single gate device, an outstanding feature of this device is its enhanced blue sensitivity. This is seen in Figure 5.31 where pairs of output characteristic curves taken at

similar powers of red and blue light have been grouped together. The lowest curve is the characteristics in the absence of light. Red light, as expected, produced a larger increase in drain current for given values of V_{DS} and V_{GS} but the response from blue light was also very prominent. The responsivity of the device to 2.15 μW blue light intensity at V_{GS} = 10 V and V_{DS} = 20 V was 10 A/W. Similar to the offset single gate device, this enhanced blue sensitivity originates from the surface location of the depletion layer where charge separation takes place. In vertical p-i-n devices the depletion layer is buried within silicon whereas in these devices it extends to the top surface of the device. The lateral structure reduces the junction capacitance but increases the carrier transit time. This can be improved by shrinking the device. In its current form the device showed a 3 dB response at around 230 kHz. This is enough for many applications where steady or low frequency pulsed light detection is required.

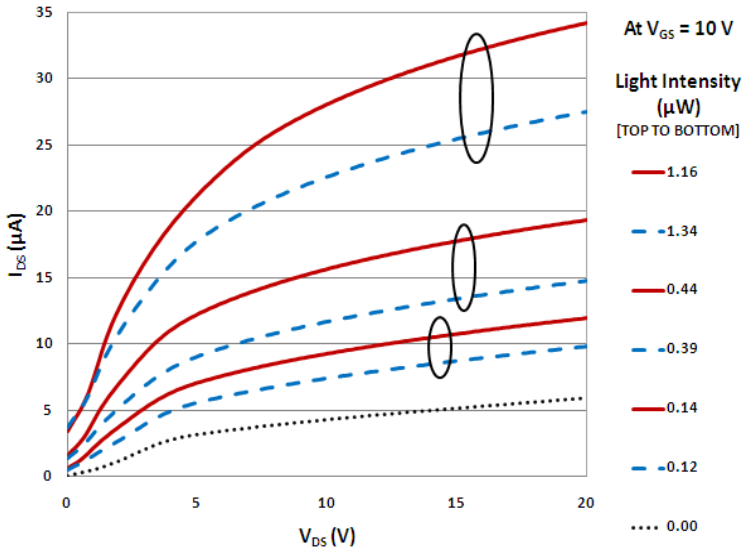
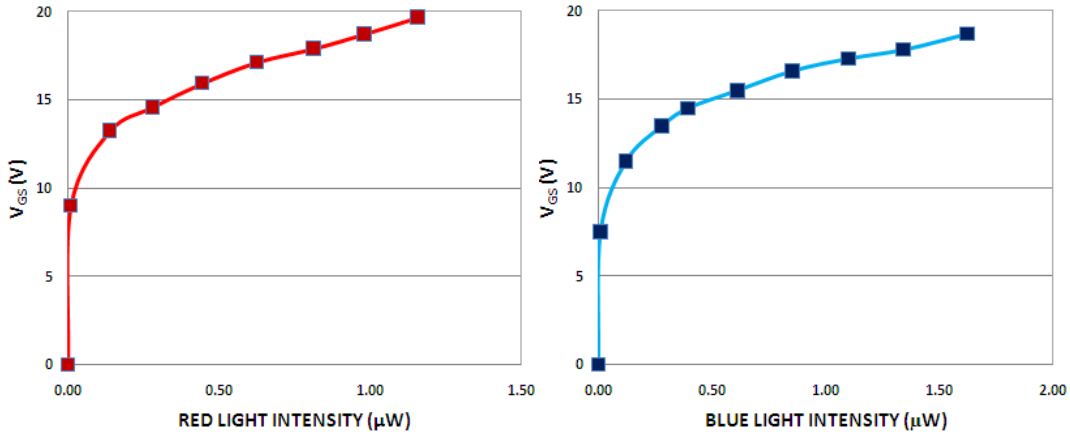


Figure 5.31: I_{DS}-V_{DS} (output) characteristics of the device with red and blue optical power as the parameter. Solid line, dashed line and dotted line represent responses with red light, blue light and in the dark, respectively at 10 V gate bias.

Similar to the behaviour of offset gated p-i-n photodiode, this device can be biased with either a light source or with a gate bias. Figure 5.29 (a) and (b) shows the device response when biased using red and blue light source, respectively. Device response with incident light as the driving parameter is seen to increase smoothly and that change is even better behaved than if it was brought about by the application of a gate-source bias. A correlation of light intensity to gate-source bias is shown in Figure 5.32 (a) and (b) for red and blue light, respectively. It is clearly seen that low red light intensity correlates to a higher gate-source bias than is the case

with blue light. Numerically, 1.16 µW red light produced drain to source current equivalent to 19.7 V of applied gate-source bias, whereas in the case of blue light 1.62 µW produced drain to source current equivalent to 18.7 V of applied gate-source bias. This behaviour is expected due to the known spectral responsivity of silicon.



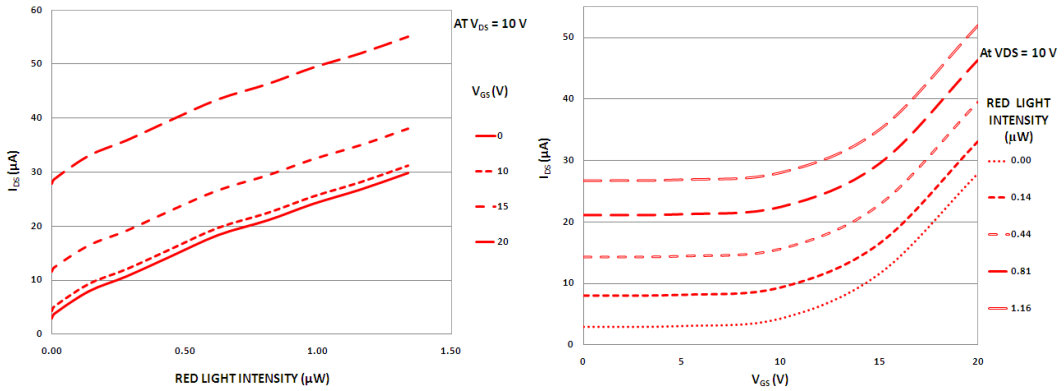
(a) (b)

Figure 5.32: Light intensity to gate-source bias correlation in centre single gate p-i-n photo-detector with. (a) red light (b) blue light.

5.3.4.1. Optical and Electrical Transfer Characteristics

Light intensities were measured with a calibrated Si-photodiode-based optical power meter. The results in Figure 5.30 and Figure 5.31 clearly show that this device acts as a transistor-like component whose lateral conduction can be controlled using both a gate voltage and an optical signal. At a given gate-source voltage, the drain-source current showed an almost linear variation with changes in red light intensity. A family of plots showing these variations appears in Figure 5.33(a). The almost constant spacing between the curves shows that light-induced increase in drain current is fairly linear as is seen in the Figure 5.33(b). This is the counterpart of traditional transconductance curves relating drain-source current to gate-source voltages. The electrical transconductance curves show that the device obeys square-law behaviour as an ordinary MOSFET but has a non-zero current at zero gate voltage due to its always-on characteristic. The electrical transconductance value at V_{DS} = 10 V, V_{GS} = 10 V and incident red light power of 0.44 µW was 0.703 µA/V. The optical responsivity of the centre gate device at V_{DS} = 20 V and V_{GS} = 10 V, is 14.96 A/W for 2.14 µW red light**.** This is much higher than the optical responsivity of typical commercial silicon photodiodes such as BPX65 from Centronics (around 0.6 A/W in the red region) and is comparable to responsivities

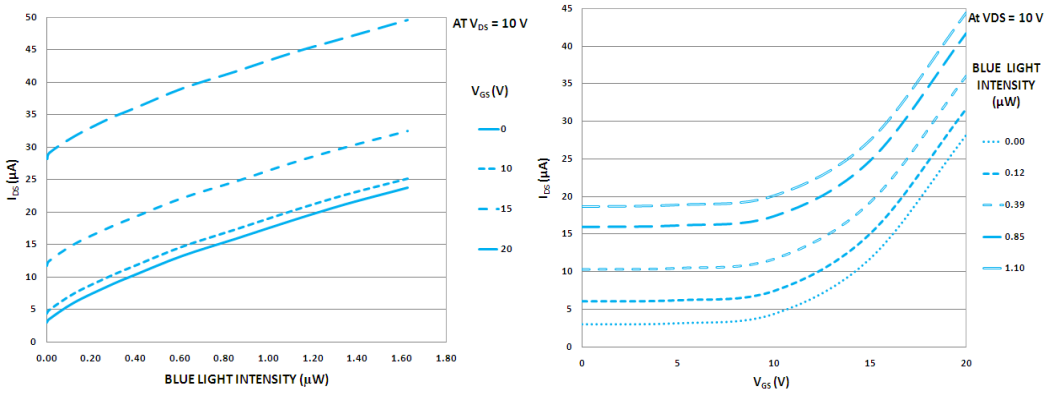
exhibited by good photodetectors made from direct band-gap semiconductors such as InGaAs [27].



(a) (b)

Figure 5.33: (a) Optical transfer characteristics and (b) Electrical transfer characteristics of the device at different red light intensities.

A similar set of optical and electrical transfer characteristics as appeared in Figure 5.33 (a) and (b) are shown with blue light of similar intensity incident on the device in Figure 5.34 (a) and (b)



(a) (b)

Figure 5.34: (a) Optical transfer characteristics and (b) Electrical transfer characteristics of the device at different blue light intensities.

The switching response of centre gate device with pulsed red light has also shown good linearity in optical-to-electrical conversion as shown in Figure 5.35.

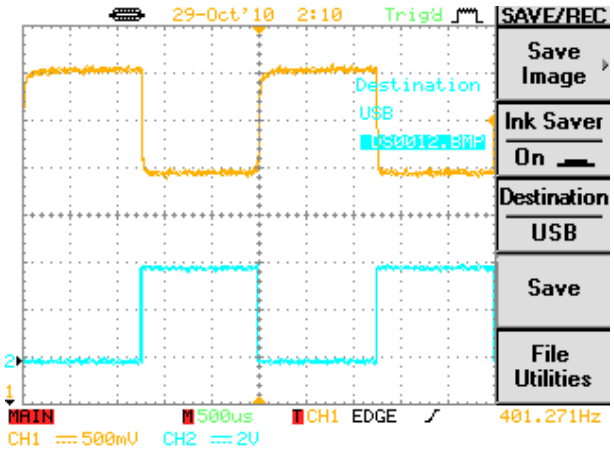


Figure 5.35: Optical to electrical conversion of the device with pulsed red light.

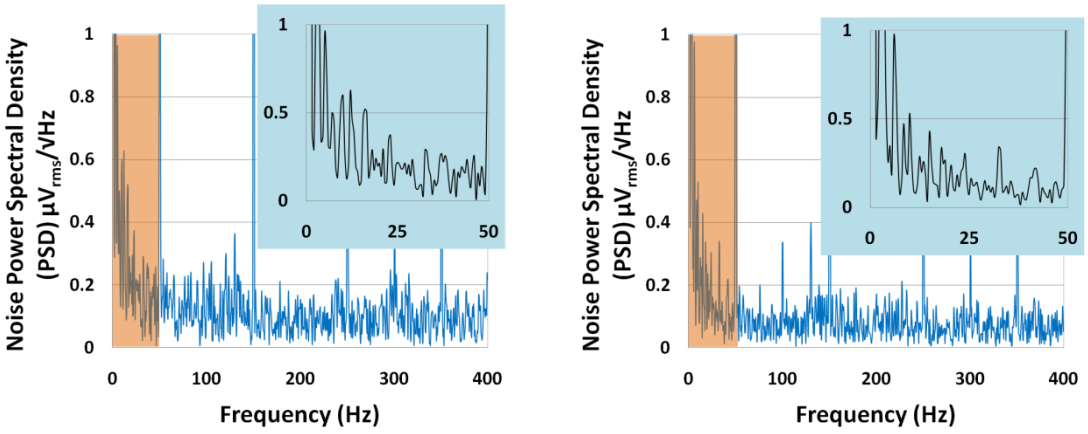
The almost linear optical transfer characteristics imply that the device introduces very little non-linear distortion when transducing signals from the optical to the electrical domain. The measured non-linearity using the second order derivative of output current versus input optical power was 7.45×10^{-6} A/W per microwatt. The functional behaviour of this device can be utilized in silicon integrated circuits for sensing light in either analogue or digital applications. The diode structure with extended n^+-to-'π' depletion region makes it a good light detector whereas the gate makes it appear as a MOSFET and can be used to adjust output electrical signal levels in order to interface easily with other transistors.

5.3.4.2. Spectral Responsivity

Both single gate devices have shown similar spectral responsivity curve. This has already been shown in Figure 5.17. It should be noted that the centre single gate device had shown relatively low responsivity values to that of the offset single gate device.

5.3.5. Noise Measurements

It is clear from the power spectral density measurements of the centre gate device shown in Figure 5.36, that noise voltages of only a few $nV_{rms}/\sqrt{Hz}$ are produced. Similar to the previously discussed device, the continuation of the SiO_2 layer on the near-intrinsic π region serves as an effective passivation layer. The noise behaviour is thus similar to good conventional vertical p-i-n photodiodes. . It is to note that the inset shows the highlighted region of the main graph.



(a) (b)

Figure 5.36: Noise measurements of centre single gate device with insets showing 1/f dependence of the pink highlighted section (a) at 20 V V_{GS} (b) at 0 V V_{GS} .

5.4. Conclusion

In this chapter, two variations of single gated-diode that features a p-i-n junction diode-like doping profile horizontally and a partial MOS gate profile vertically are described. These devices acts as a hybrid diode-transistor where the diode elements detect incident light and the transistor structure can be used to adjust the current flow through the device. These devices have advantages which include easy integration into CMOS process flows, ease of circuit design with conventional MOSFETs and high sensitivity to the short wavelength blue and UV region compared to vertical p-i-n diodes. These devices are characterised electrically and optically to highlight both the optical detector and transistor-like functionality of these devices.

5.5. References

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Chapter 6

Dual Gate Silicon p-i-n Photodiodes

6 Introduction

Detectors based on both silicon and compound semiconductors are widely used to detect light for a variety of applications. These devices work on different principles but the central mechanism is always the excitation of a charge carrier across an energy gap through the absorption of one or more incident photons. The capability and efficiency of the detection process is determined by a host of factors that depend both on the properties of the detector material and the details of device design. Prominent parameters that are often the basis for selecting detectors for particular applications include the wavelength coverage (detection band), quantum efficiency of the detection process, responsivity (output generated with unit power input), signal-to-noise ratio and dark current (detector output in the absence of any input signal) [1]. No one detector excels in all desirable attributes and thus a number of different types of detectors exist – each suitable for a specific type of application [2]. pn-junction-based semiconductor detectors are the most widely used optical detectors and come in a variety of forms to satisfy different operational requirements. Their technology has diversified from simple vertical pn-junctions to more involved architectures, capable of single photon detection and even high resolution imaging, when incorporated as a focal plane array.

Most parameters of a given detector are fixed through the choice of material, processing techniques and device structure. However, some important parameters such as sensitivity and response time can be varied to some extent by appropriately biasing the detector. For most light sensors, spectral responsivity, i.e. the relative responsivity of a detector at different wavelengths is principally determined by the energy level structure of the material and device cannot be altered significantly through external biasing. This limitation necessitates the use of various kinds of filters to obtain wavelength-specific responses from semiconductor pn-junction light detectors. In fact, most optical filters are used for delineating desired regions of a sensor's spectral responsivity curve to match a particular operational requirement. Electronic control of spectral responsivity is extremely desirable as it will allow a detector's spectral response to be customised to an application requirement merely through appropriate biasing of the device. The device described in this chapter allows one to realise this extra functionality by using a pair of metal-oxide-semiconductor (MOS) gates on a lateral pn-junction. It is demonstrated that when appropriately biased such a device allows the peak of spectral responsivity to be shifted over quite a broad range of wavelengths.

Silicon's absorption coefficient for different wavelengths is dependent on the distance traversed by photons inside the material. For photon energies above the band gap of silicon, shorter wavelength photons are predominantly absorbed close to the surface of a device whereas the longer wavelength photons penetrate deeper into the material and are absorbed more weakly. This dependence of photon absorption coefficient on path length inside the semiconductor can be made the basis of a scheme for wavelength discrimination. Previously, this has been attempted by making tiered device structures where separate detection layers at different depths have been incorporated in a vertical geometry. While such an architecture is effective, its characteristics are fixed through fabricated design and cannot be changed 'on the fly' [3]. The device discussed here, in comparison, had a simple planar structure which is fully CMOS-compatible and allows continuous tuning of wavelength response simply by altering the voltages applied to two surface gates.

This chapter, continuing the theme of Chapter 5, describes transistor-like dual gate light sensing devices. These dual gate devices use the same base architecture i.e. lateral p-i-n diode as the single gate devices described in Chapter 5. These devices are also CMOS compatible and, therefore, have gates to control their quiescent operating point. This light sensing device

can be monolithically integrated with other transistors on the chip. Device fabrication details are the same as described in "device fabrication techniques" within Chapter 4. Here the device response is explained with regards to its electrical, optical and noise characteristics. These devices exhibit short-wavelength sensitivity and the ability to modulate the spectral responsivity with proper biasing on the dual gate structure. The gates are used in a similar way to control the lateral conduction of the device as in the case of single gate devices. The overlapping dual gate device has, specifically, shown gate bias-induced modulation of spectral responsivity, where the sensitivities at red and blue wavelengths (630 nm and 480 nm, respectively) cross-over and the device at higher gate bias values becomes more sensitive to blue wavelengths than to red wavelengths.

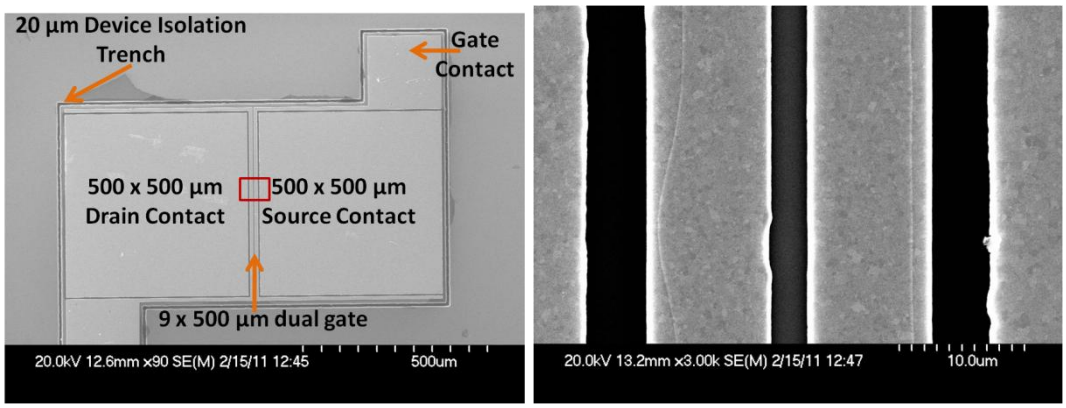
6.1 Device Design

Similar to the single gate devices, the dual gate devices detect light through a lateral p-i-n junction structure, where the dual gate structure, when properly biased, controls the current through the device. Two different types of dual gate photodiodes were fabricated. The first type of dual gate device was a normal dual gate device with two gates, each, 9 microns in length. The second set of devices was with two 15 microns long overlapping gates. Fabrication details have been described in the fabrication techniques chapter, whereas the design details are explained and illustrated in the next section. These dual gate devices have exhibited the ability to modulate the spectral responsivity of the device when both gates [i.e. drain side gate (V_{GD}) and source side gate (V_{GS})] are appropriately biased.

6.1.1 Normal Dual Gate Lateral p-i-n photodiode

As explained earlier, all the devices (single gate, dual gate and integrated metal grating devices) reported in this work used the same lateral p-i-n junction architecture and these devices were fabricated with similar processing techniques. However, certain changes in the placement and dimension of gate structure and contact electrodes were made to better explore the behaviour of these devices. Coming back to the dual gate device, the normal dual gate device has exactly the same lateral structure as that of single gate devices, except for the gate structure. In the normal dual gate device, 9 microns long and 500 microns wide dual MOS gate structures were metallized over the 32 microns, insulated, near-intrinsic region. This was done in such a way that both the gates were placed 5 microns away from respective electrodes

i.e. source and drain and both the gates were 4 microns apart from each other. In Figure 6.1 (a) an SEM micrograph of an actual normal dual gate device is shown.



(a) (b)

Figure 6.1: (a) An SEM micrograph of normal dual gate device and (b) highlighted SEM micrograph showing the boxed gate region.

It illustrates the actual device design with 500 x 500 microns (anode) source and (cathode) drain contacts and two "U" shaped gate structures surrounding the respective electrodes. Each gate had 200 x 200 microns contacts as shown in the Figure 6.1 (a). The red boxed region in Figure 6.1 (a), is shown in Figure 6.1 (b). Here the gate structure, along with the gap in between the gates and electrodes, is illustrated. In Figure 6.2 a labelled cross-section image of the normal dual gate device is shown. The cross-section represents the same red boxed region as shown in Figure 6.1 (a). Except for the structural variation, all other fabrication processes were the same as that of single gate devices. In the rest of the discussion, this device will be referred to as the normal dual gate device.

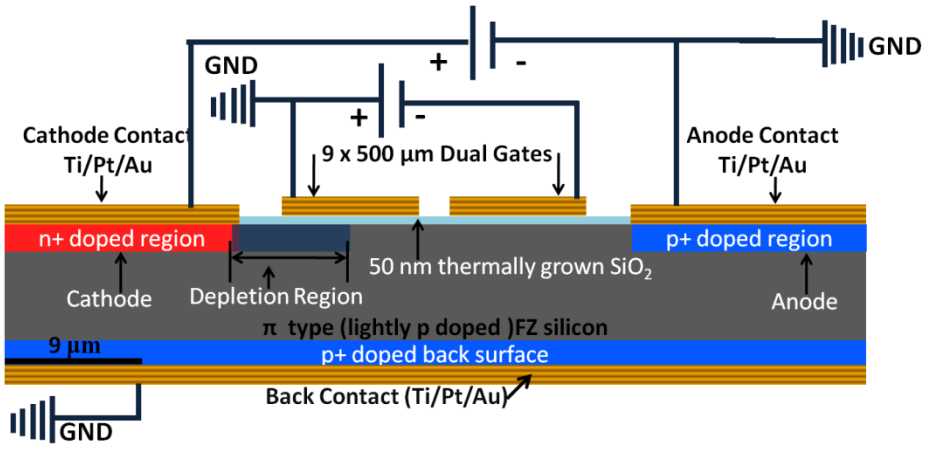
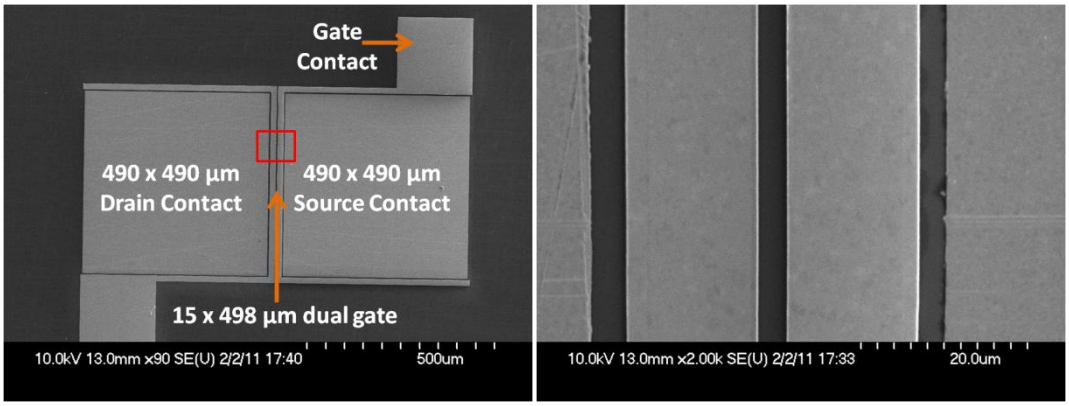


Figure 6.2: Cross-section of the normal dual gate lateral p-i-n photodiode.

6.1.2 Overlapping Dual Gate Lateral p-i-n Photodiode

The fabrication of overlapping dual gate device followed the same steps as the devices described earlier until the diffusion process to make heavily-doped source and drain contacts i.e. p and n type contacts. Unlike the normal dual gate device, the overlapping dual gate lateral p-i-n photodiode had 490 x 490 microns metal contacts such that the metal contacts were in the centre of 500 x 500 microns heavily-doped p and n regions. This configuration left a 42 microns distance between the two electrodes i.e. source and drain, instead of 32 microns as in the normal dual gate device. This 42 microns gap covered the 5 microns diffused region from both ends of the 32 microns near-intrinsic π region. The 15 microns overlapping dual gate structure was patterned over the 42 microns long insulated region such that both the gates were 4 microns away from adjacent electrodes. The gap between the two electrodes was 4 microns in both types of dual gate devices. In this configuration, the 15 microns gate structure over the oxide layer was patterned such that from the inner side of 'U' shaped surrounding gate, 1 micron gate region overlapped the adjacent doped region.



(a) (b)

Figure 6.3: (a) An SEM micrograph of overlapping dual gate device (b) Highlighted SEM micrograph of boxed gate region.

In terms of distances, 4 + 15 + 4 + 15 + 4 = 42, here the middle 4 microns represents the gap between the 15 microns overlapping dual gates, whereas the 4 microns on the edges was the distance from the respective electrodes. An SEM micrograph is shown in Figure 6.3 (a) which highlights the source and drain contacts and the overlapping dual gate structure. It should be noted that both the structures i.e. normal dual gate and overlapping dual gate, look similar in the SEM micrographs. However, the cross-sectional diagram of both devices clearly explains

the differences. The boxed region in Figure 6.3 (a) is actually the gate region and is highlighted in Figure 6.3 (b). In Figure 6.4, labeled cross-section of the boxed region is shown to highlight the heavily-doped p and n regions, depletion region, back contact, oxide region and contact metallization. In the rest of the discussion this device will be referred to as the overlapping dual gate device.

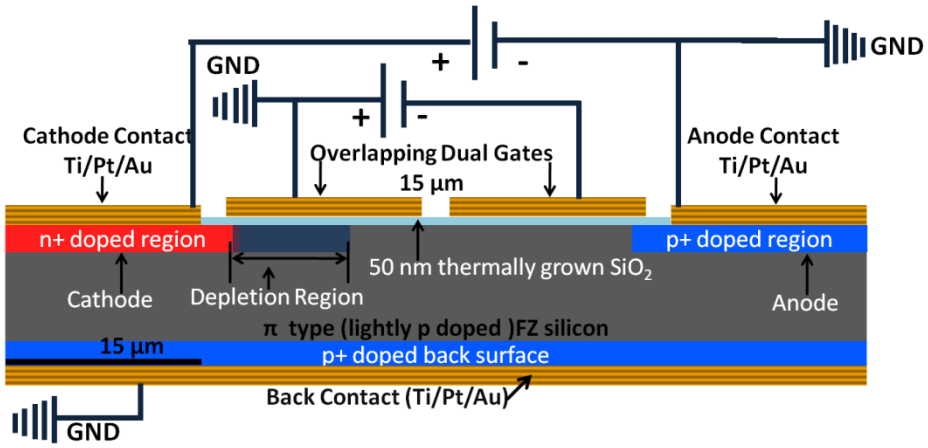


Figure 6.4: Cross-section of overlapping dual gate lateral p-i-n photodiode.

6.2 Device Operation

Both sets of dual gate devices (normal dual gate and overlapping dual gate) were operated with a reverse bias lateral p-i-n junction biasing, as is usual for light detection applications. The dual gates in the vertical MOS structure were biased with 8 different biasing configurations, however, results from one such biasing arrangement are presented here. In the measurement setup the source side gate (V_{GS}) was biased at a negative potential with reference to the drain side gate (V_{GD}) which was biased at zero reference potential. The measurements were performed at 0, -5, -10, -15 and -20 V, successive gate-source biases and are described in various sections. Furthermore, the next section deals with the simulation of overlapping dual gate device.

6.2.1 Device Simulation

The operation of the overlapping dual gate device was investigated using physical device modelling techniques. The results obtained from the physical device modelling studies match the actual measurements performed on fabricated devices. The details of the simulation model are similar to the explanations already given in the previous chapter. Simulation structure of

the overlapping dual gate device is shown in Figure 6.5, where two gates are shown overlapping the adjacent doped regions. In Figure 6.8 the gate bias-induced increase in carrier density of the accumulation layer is shown.

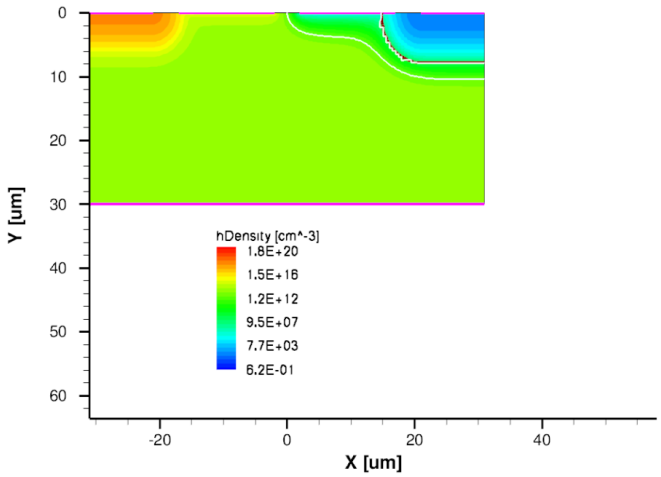


Figure 6.5: Hole density simulated result with biased overlapping dual gate

The simulation results for IV characteristics of the overlapping dual gate device in dark are shown in Figure 6.6. The simulations were performed to anticipate the device response in dark at different gate bias values. The increasing 'trend' in output current as a result of increase in gate bias agrees with the actual IV characteristics of the an overlapping dual gate device, obtained from the physical measurements as shown in Figure 6.21. It is to be noted that in simulation due to ideal conditions the gate leakage current is zero at 0 V V_{DS} and at different V_{GS} values.

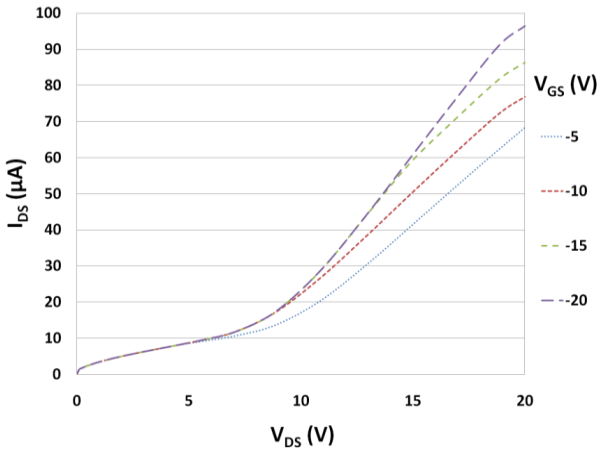
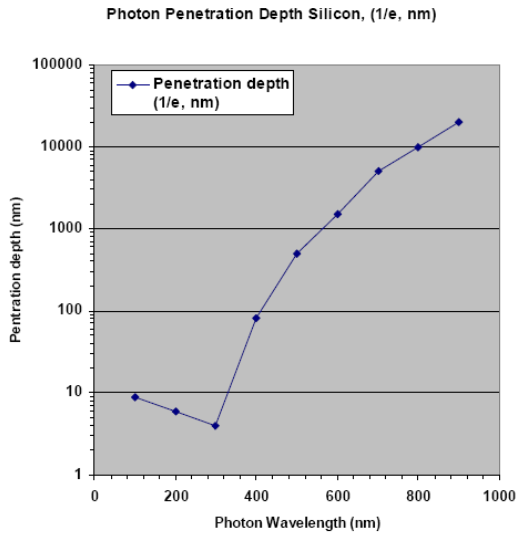


Figure 6.6: Simulated (I-V) characteristics of the overlapping dual gate device at different gate bias values in dark.

6.2.1.1 Wavelength and Penetration Depth

Incident photons, depending on their energy, are absorbed in silicon at different depths. The photons from short wavelength radiations like UV and blue wavelengths are absorbed close to the surface, whereas the longer wavelength photons like that from the red and near-IR regions penetrate deeper inside silicon. A penetration depth graph of varying wavelength incident photons in silicon is shown in Figure 6.7 [4]. This penetration depth can be correlated to the gate bias-induced change in carrier density and the thickness of accumulation layer. This leads to the concept of gate bias-induced change in spectral responsivity of the dual gate lateral p-i-n photodiode.



(a)

Figure 6.7: Penetration depth (μm) as a function of wavelength (nm).

6.2.1.2 Gate Bias-induced Change in Carrier Density of Accumulation Layer

Gate bias-induced change in accumulation-layer-carrier-density was obtained using physical device modelling techniques and is shown in Figure 6.8. It can be clearly seen that the carrier density is higher close to surface and decreases with depth farther away from the surface. The carrier density in the accumulation layer is higher at higher gate bias values i.e. higher negative gate bias voltage on source side gate with reference to drain side gate.

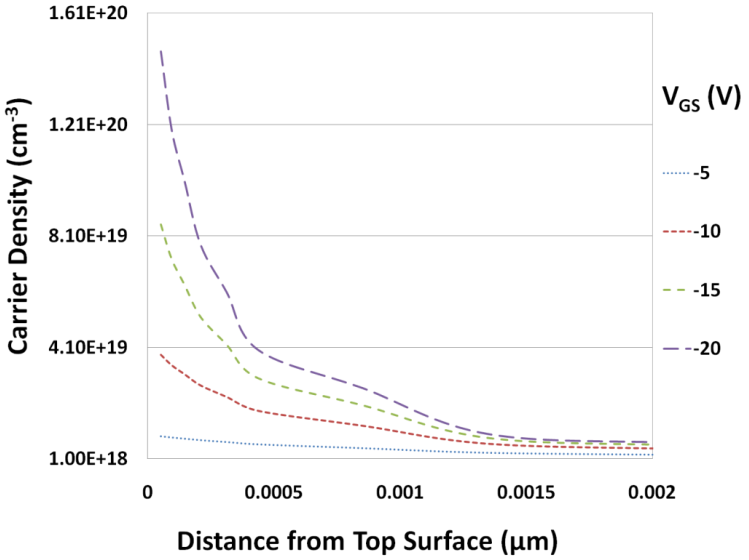


Figure 6.8: Gate bias-induced change in carrier concentration of the accumulation layer.

6.3 Normal Dual Gate Device Operation

The heavily-doped n and p regions form the two lateral cathode and anode contacts of the p-i-n junction photodiode. As the vertical MOS structure of the device is similar to that of a transistor, therefore these two contacts are referred to as the drain and source contacts of the normal dual gate device. Light detection process in the normal dual gate device works with reverse-biased lateral p-i-n junction, its mechanism is similar to that described for the single offset gate device in Chapter 5. The depletion layer between the heavily-doped n region and the lightly doped (near-intrinsic) π region is theoretically 6.81 microns wide, and the major part of the depletion layer lies in the near-intrinsic π region. With the increase in reverse bias the width of the depletion region increases [5]. This is in accordance with equation 5.1 in Chapter 5. The electron-hole pairs produced in the depletion region are separated by the depletion region electric field and are swept across the junction. Electrons simply move into the heavily n-doped adjacent region whereas the holes are ejected out of the depletion region, diffuse through the intrinsic region and reach the heavily p-doped anode region. In Figure 6.2 the cross-section of the normal dual gate device is shown with the two MOS gates over the 50 nm thick SiO_2 layer. The electrical response of the device increased under influence of both the reverse bias diode and biasing the gate. This increase in the dark current with an increase in reverse bias is normal and is already explained in the literature. However, the increase in device current with increase in gate-source bias is due to the partial transistor element which works in enhancement mode to increase the conductivity of the device. The difference in

operation of single and normal dual gate device and in normal dual gate and overlapping dual gate device is mainly due to difference in the gate bias and reference potential.

6.4 Normal Dual Gate Device Characteristics

The normal dual gate device electrical and optical characteristics are described here followed by spectral responsivity and noise measurements. Some measurements were performed with reverse-biased p-i-n diode part of the device, whereas other measurements take into account the gating action as well.

6.4.1 Electrical Response

In the absence of any gate bias, the forward and reverse bias characteristics of the device have been shown in Chapter 5. These characteristics are the same for the normal and overlapping dual gate devices as well. Here the electrical response of the normal dual gate device in dark is explained. In the next section the device current-voltage characteristics and transconductance response are described.

6.4.1.1 Current-Voltage Characteristics (dark)

To understand the overall device characteristics, the diode-transistor-like device was biased by applying both a cathode-anode bias and a gate bias. The source side gate was biased at a negative potential with reference to the drain side gate which was kept at zero reference potential. This resulted in a hole-rich region underneath the source side gate i.e. an accumulated layer of holes. Both the gates were close enough to the adjacent heavily n and p-doped regions and thus the accumulated holes had the effect of laterally extending the source region. This lateral extension shrunk the electrical width of the device and caused the resistance to decrease. This is seen in Figure 6.9, where the current-voltage characteristics at different gate biases (in dark) are shown. Similar to the single gate devices, these characteristics appear like conventional transistor characteristics. The different curves represent the device response at different gate bias voltages. With increase in the gate bias (negative with respect to the source side gate) the depth of the accumulation layer increases, which gives rise to the device response and the device characteristics shift upward. Here at higher gate bias values and 0 V V_{DS}, a gate leakage current is seen, to which an explanation

has already been given in section 5.2.4.2 where similar response of an offset gate device is discussed.

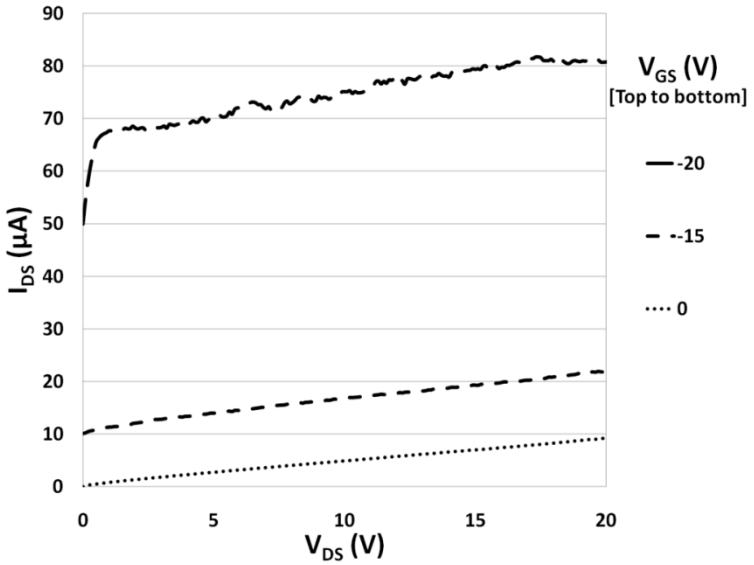


Figure 6.9: Current-Voltage characteristics of normal dual gate device at different gate bias in dark.

6.4.1.2 Transconductance

A transcoductance curve can be derived from data on drain-source current as a function of gate-source bias. In Figure 6.10 the $I_{DS} - V_{GS}$ curve corresponds to 10 V V_{DS}. The transconductance at -15 V V_{GS} and 0 V V_{GD} was 7 μA/V. Although the device is biased with unusual polarities, still the $I_{DS} - V_{GS}$ graph shows that the device obeys square law and appears as a transistor as far as its terminal behaviour is concerned. More accurately, the device operates partially as an enhancement mode transistor.

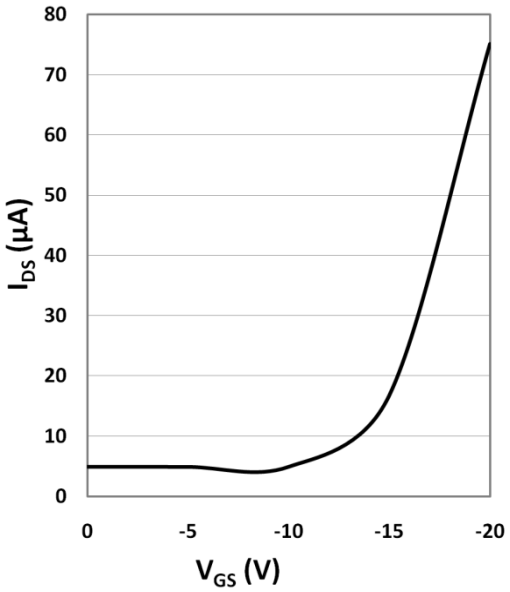
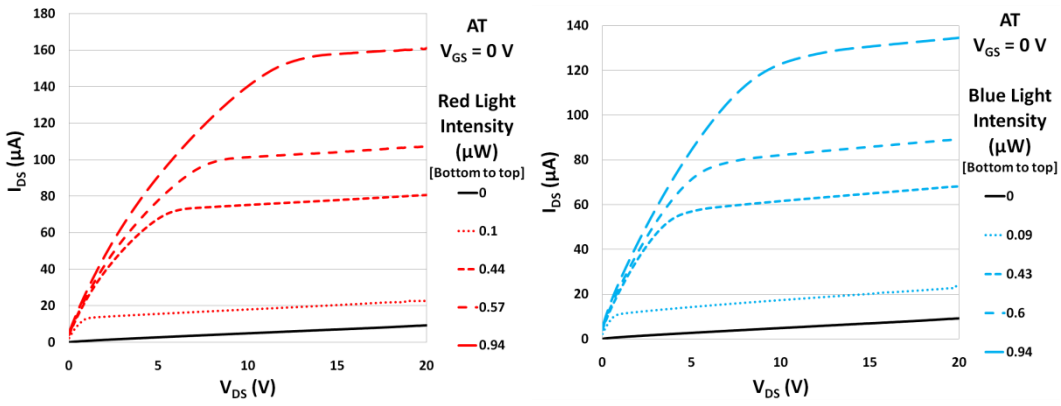


Figure 6.10: Transconductance plot of normal dual gate device in dark.

6.4.2 Optical Response

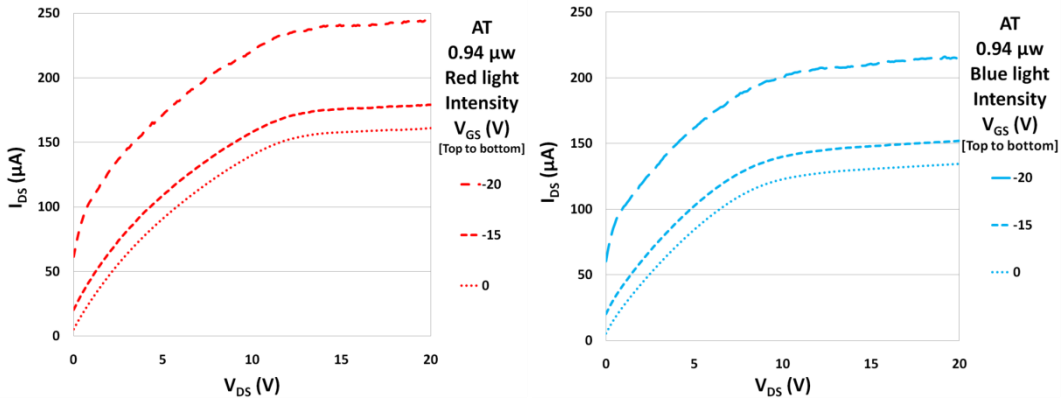
Optical measurements were taken with red and blue light emitting diodes with emission wavelengths centred at 630 nm and 480 nm, respectively as sources of illumination. The light spectra have already been shown in Figure 5.9 of Chapter 5. In optical measurements, the first set of measurements deals with the pure diode characteristics i.e. with 0 V gate bias and with different red and blue light intensities. Whereas, the second set of measurements deals with the transistorized configuration, where both the lateral and vertical elements of the normal dual gate device were biased and tested for different red and blue light intensities. The device showed similar characteristic response with different intensities of red and blue light. The normal dual gate device response to red and blue light intensities was similar to the offset single gate device, and appeared very much similar to that of a conventional Si photodiode response. The normal dual gate device showed better blue wavelength (480 nm) response although the blue wavelength response was still less than that of the red wavelength (630 nm). This was mainly due to the presence of surface depletion region in the lateral p-i-n junction photodiode. This surface depletion region did contribute to excess dark current, that, however, is a compromise over the high responsivity values. The optical response of the device at normal incidence of different red and blue light intensities is shown in Figure 6.11 (a) and (b), respectively.



(a) (b)

Figure 6.11: Optical response of the device at 0 V V_{GS} at different light intensities with (a) red light (b) blue light

An upward shift in the reverse bias diode characteristics when illuminated with higher intensities of light is an expected behaviour. This clearly shows that the lateral conduction in the device can also be controlled with the intensity and wavelength of the incident light source. Here three parameters i.e. the reverse bias voltage, intensity and wavelength of the light source are used to control the output current through the device. In Figure 6.11 it is clear that the optical response of the device at different light intensities is better behaved than the response of the device where gate bias is used as a parameter to control the current flow through the device.



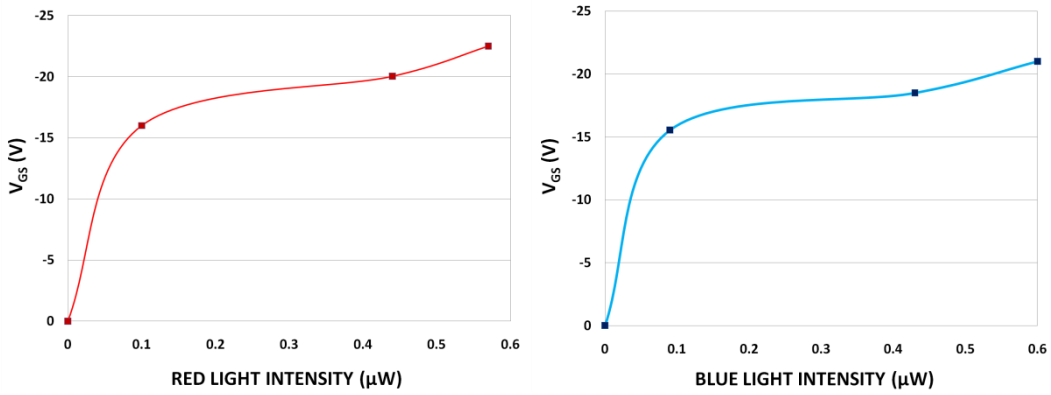
(a) (b)

Figure 6.12: Transistorized optical measurements with fixed (a) red light intensity (b) blue light intensity.

The optical response of the device in transistorized configuration is shown in Figure 6.12 (a) and (b) for red and blue light intensities, respectively. The device was reverse-biased while the source side gate was biased at 0, -15 and -20 V, with reference to the drain side gate which

was kept fixed at 0 V reference potential. The device was exposed to 0.94 µW fixed red and blue light intensities.

Considering the device response in Figure 6.9 and in Figure 6.11 (a) and (b), where current-voltage characteristics in dark and the optical response of the device with reverse-biased diode element of the device are shown with red and blue light sources. A correlation can be derived where optically generated output current equals the gate bias induced output current. This correlation for red and blue light intensities is shown in Figure 6.13 (a) and (b), respectively. It appears similar for red and blue lights, where lower red light intensity can produce current equivalent to higher gate bias values than that would be produced with equivalent blue light intensity. In Figure 6.13 the correlation of the gate bias as a function of light intensity is shown. Here 0.6 µW incident blue light power produced current equivalent to -21 V gate bias, whereas 0.57 µW incident red light power produced current equivalent to -22.5 V gate bias.

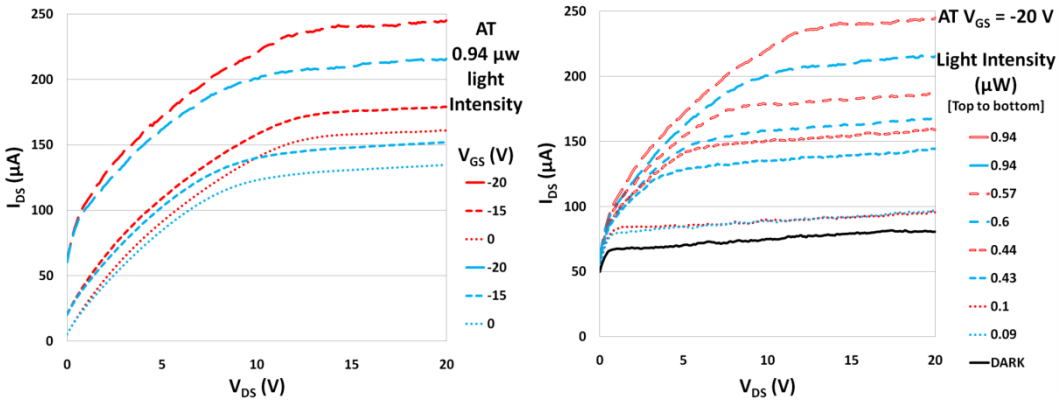


(a) (b)

Figure 6.13: Light intensity to gate-source bias correlation in normal dual gate p-i-n photo-detector with (a) red light (b) blue light.

In addition, the device response with red and blue light is compared in Figure 6.14 (a) and (b). In Figure 6.14 (a) the device response is compared for red and blue light at fixed intensity for different gate bias values. It should be noted that the biasing arrangement for both the gates remained similar for all sets of measurements, where the source side gate was biased at 0, -15 and -20 V gate bias values with respect to the drain side gate which was biased at 0 V reference potential. In order to differentiate the device response, in red and blue light at the same gate bias values, responses are plotted with the same line style.

In order to meaningfully compare the device response in red and blue light, the transistorized response of the device at -20 V gate bias was plotted in Figure 6.14 (b) at different light intensities. The lowest solid black line represents the device response in dark. The optical response of the device for similar red and blue light intensities was plotted with similar line style, in order to be identified quickly. Here it is further clarified that the device showed very good sensitivity to short-wavelength radiations. The responsivity of the normal dual gate device to red and blue light was 41.51 A/W and 38.29 A/W, respectively at (V_{DS} = 5 V and V_{GS} = -10 V) showing a percentage decrease of 8 % from red to blue wavelengths. These responsivity values are higher than those exhibited by single gate devices. It should be noted that higher responsivity values have already been predicted by Yun Zeng et al. [6]. Responsivity values for single gate devices have already been compared to commercial silicon photodiode BPX65 and were found to be two orders higher. These high responsivity values are due to the presence of space charge region at the top surface where the separation of optically-induced electron-hole pairs takes place. Other types of silicon-based photodetectors with high responsivity values relied on back illumination and back-thinning techniques [7].



(a) (b)

Figure 6.14: Current-voltage characteristics (a) with red and blue light at different V_{GS} (b) with red and blue light of different intensities at fixed V_{GS}.

Another graph can be derived from Figure 6.14 (a) where the ratio of $I_{DS(red)}$ to $I_{DS(blue)}$ and the ratio of $I_{DS(blue)}$ to $I_{DS(red)}$ can be calculated to ascertain the change in device response at a particular gate bias voltage. Here in Figure 6.15 it is clearly seen that the device response to a particular wavelength changes with gate bias voltage i.e. beyond -10 V gate bias. This shows that the normal dual gate device with appropriately biased gates can modulate the device

response. This change in responsivity with change in gate bias is due to the presence of two gates, which are biased with reference to each other.

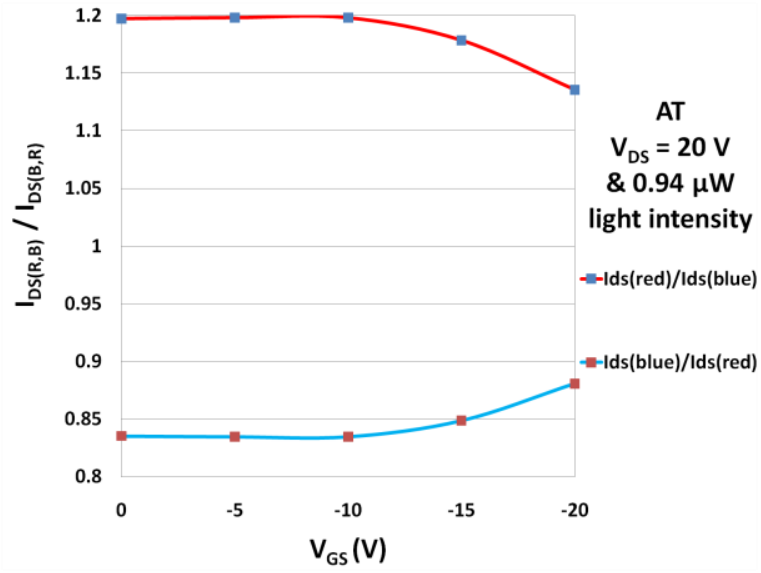
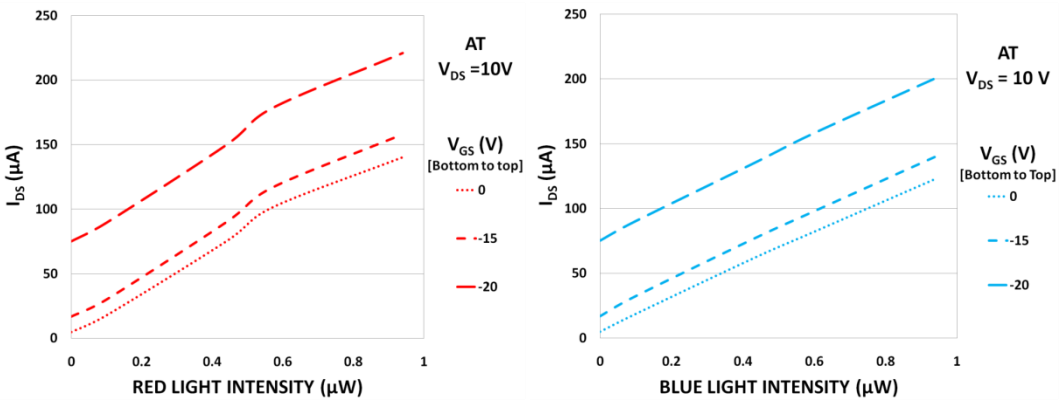


Figure 6.15: $I_{DS(red,blue)}$ / $I_{DS(blue,red)}$ as function of V_{GS} with fixed light intensity.

Based on Figure 6.14 (a) the percentage change in device output current in going from 630 nm wavelength to 480 nm wavelength at -20 V gate bias is 11 % and at 0 V gate bias it is 15 %. This percentage difference is less than that of the value exhibited by single gate devices which is 21%. This percentage change in output current when calculated using Figure 6.14 (b) comes to 11% for 0.94 µW incident light power and 9% for 0.44 µW incident light power.

6.4.2.1 Optical and Electrical Transfer Characteristics

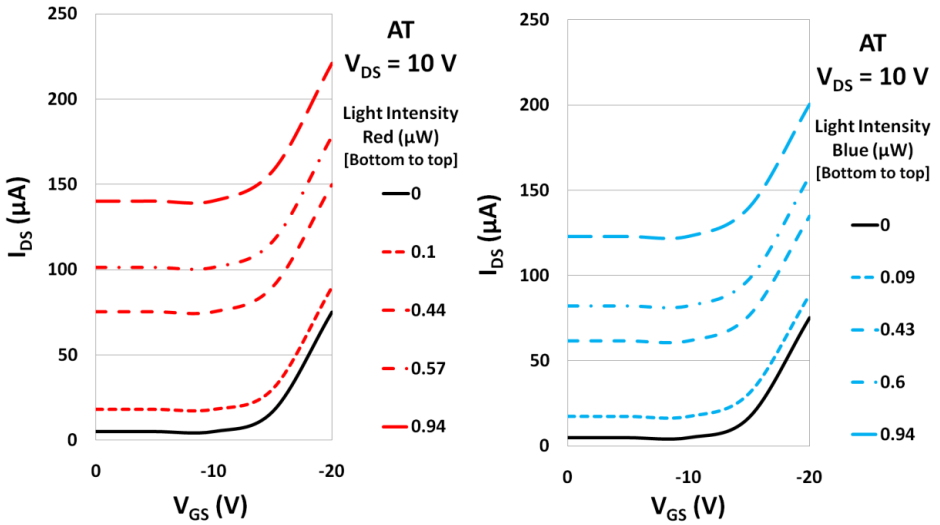
The optical transfer characteristics of the normal dual gate device for red and blue light illumination are shown in Figure 6.16 (a) and (b). The normal dual gate device with red and blue light centred at 630 nm and 480 nm have shown fairly linear optical transfer characteristics. This implies that the device would bring in very little non-linear distortion when converting optical signals to signals in the electrical domain.



(a) (b)

Figure 6.16: Optical transfer characteristics at different gate bias (a) with red light (b) with blue light.

The transconductance curve shown in Figure 6.10 was taken in dark and implies that the device obeys square law behaviour and thus appears as a transistor to the surrounding circuitry. Here the transconductance curves are plotted at different intensities of red and blue light as shown in Figure 6.17 (a) and (b), respectively. The solid black line in both graphs is the device response in dark, as already shown in Figure 6.10. Here each curve represents the device response at different intensities of red and blue light.

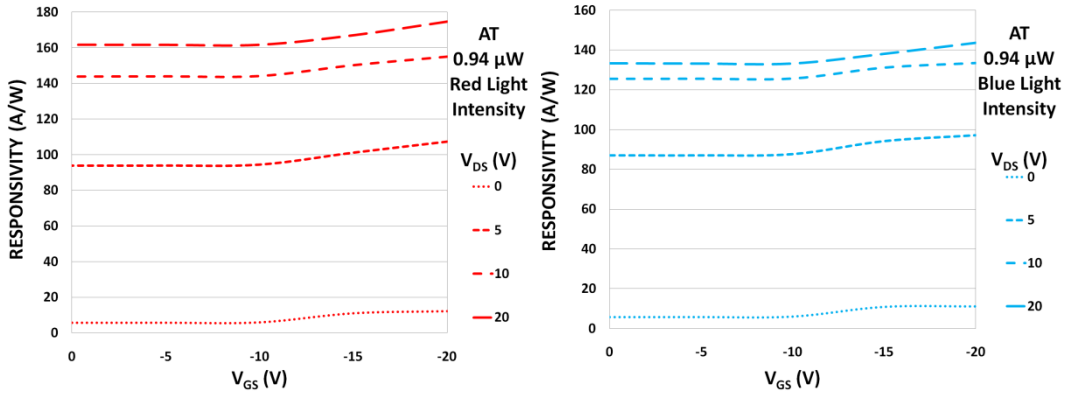


(a) (b)

Figure 6.17: Electrical transfer characteristics in dark and at different light intensities (a) with red light (b) with blue light.

6.4.2.2 Responsivity as a Function of Gate Bias

The normal dual gate devices were measured in both dark and light. Under illumination the devices were measured with normal incidence of red and blue light flux centred at 630 nm and 480 nm, respectively. In Figure 6.18 (a) and (b) absolute responsivity as a function of gate bias is shown. The response of the device is influenced with gate bias and follows similar behaviour for both red and blue illumination. This becomes the basis for gate-bias-induced change in spectral responsivity of the normal dual gate device. The graph showing spectral responsivity as a function of gate bias is shown in the next section. The graphs shown in Figure 6.18 (a) and (b) where responsivity changes as a function of gate-source-bias, justify the device response in Figure 6.15 where the ratio of $I_{DS(red)}$ to $I_{DS(blue)}$ and ratio of $I_{DS(blue)}$ to $I_{DS(red)}$ are shown.



(a) (b)

Figure 6.18: Responsivity as a function of V_{GS} at different V_{DS} values with (a) red light (b) blue light.

6.4.2.3 Spectral Responsivity

The complete spectral responsivity of the normal dual gate device for the 400 nm to 900 nm range was measured using the same monochromator setup as was used for measuring the single gate devices. Spectral responsivity measurements were taken while the lateral p-i-n diode was reverse-biased at 10 V V_{DS} whereas the normal dual gates in the vertical MOS structure were biased at different gate bias voltages. The drain side gate was kept fixed at 0 V reference potential whereas the source side gate was biased with 0, -5, -10, -15 and -20 V with reference to the drain side gate. All the five responsivity curves at different gate-source-bias

voltages are shown in Figure 6.19. Here it should be noted that all the plots have been scaled vertically in order to make useful comparisons.

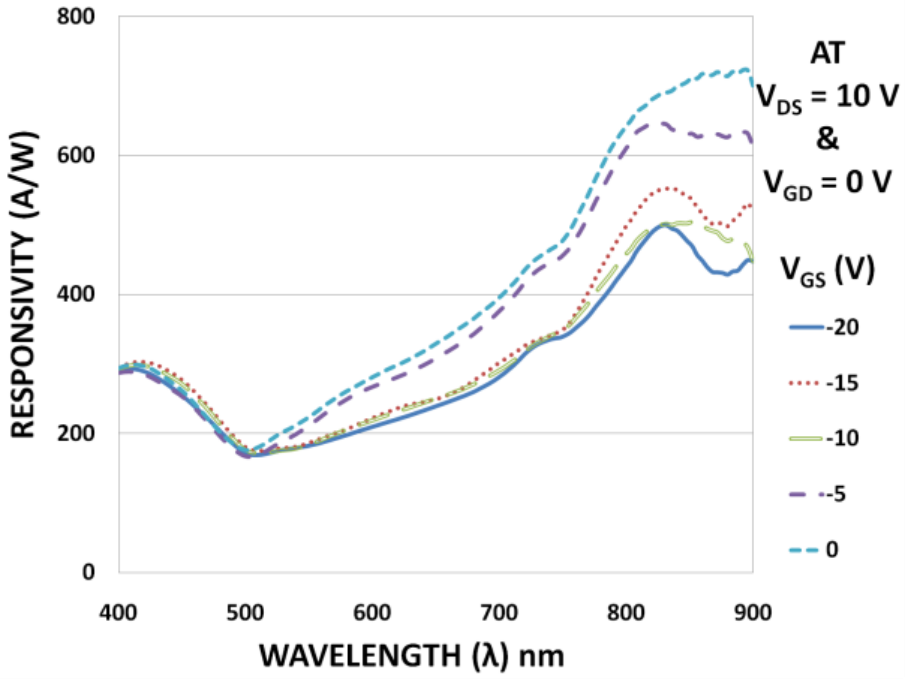


Figure 6.19: Spectral responsivity of the normal dual gate device

6.4.3 Noise Measurements

The normal dual gate device structure and its fabrication process as already mentioned is exactly the same as that of single gate devices, except for the change in the gate pattern over the gate-dielectric (SiO_2). In Figure 6.9, at 15 V V_{DS} (reverse bias) and in the absence of any gate bias, the amount of the dark current is 7 μA. This is a higher value for dark current as compared to that for typical conventional vertical p-i-n photodiodes and is mainly due to the surface location of the depletion region. This is due to a phenomenon called "skin effect" where the broken bonds at the surface of a diode form a surface leakage path. Here the surface acts as a conducting channel and broken bonds form trapping centres to enhance the generation-recombination effects. Therefore, these surface imperfections give rise to leakage current. This phenomenon causes higher noise levels in devices with surface depletion region. The power spectral density measurements for a normal dual gate device at V_{DS} = 10 V and at different gate bias voltages, have shown average noise voltages of a few $nV_{rms}/\sqrt{Hz}$ as shown in Figure 6.20. The inset shows the highlighted region of the main graph. This value is comparable to that of conventional silicon photodiodes. Similar to the single gate devices, the

lateral continuation of the gate dielectric served as a good passivation layer and has effectively reduced the $Si - SiO_2$ interface noise [8, 9]. The amount of the dark current in the device can be further reduced if it is fabricated with SOI material [1, 10].

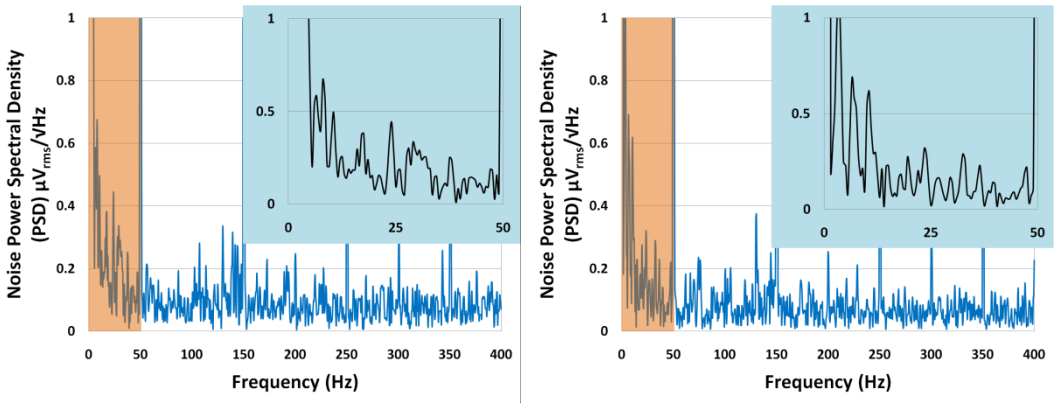


Figure 6.20: Noise measurements of normal dual gate device with insets showing 1/f dependence of the pink highlighted section (a) at V_{DS} = 10 V, V_{GS} = 0 V, V_{DG} & BC = 0 V. (b) at V_{DS} = 10 V, V_{GS} = -20 V, V_{DG} & BC = 0 V.

6.5 Overlapping Dual Gate Device Operation

The overlapping dual gate device operates in a similar way as a normal dual gate device. The fabrication details are nearly same as that for a normal dual gate device, so the width of the depletion region, the junction electric field and most other parameters would remain the same. However, there are other conditions to consider while anticipating the device response. This includes the fact that overlapping dual gate devices have two gates which overlap the adjacent heavily doped n and p regions by 1 micron. Therefore, the overlapping dual gate device would show some variation in its gate bias-induced response. The overlapping dual gate device characteristics are further explained in the coming section. The difference in response of the normal dual gate and overlapping dual gate device is mainly due to the difference in the gate bias, reference potential and placement of the gate structure.

6.6 Overlapping Dual Gate Device Characteristics

In this section the overlapping dual gate device electrical and optical characteristics are explained, followed by its spectral responsivity and noise characteristics. The overlapping dual gate device characteristics are similar to that of normal dual gate device. These characteristics

appear to be more elaborate than that of the normal dual gate device and are described in the following section.

6.6.1 Electrical Response

Overlapping dual gate device's electrical response is illustrated here with the help of current-voltage characteristics and its transconductance graph.

6.6.1.1 Current-Voltage Characteristics

The current-voltage characteristics of an overlapping dual gate device were measured in transistorized configuration. The biasing arrangements were same as was the case with normal dual gate device. In a similar way, the lateral conduction of the overlapping dual gate device is controlled through applied reverse bias to the lateral p-i-n junction and with properly biased vertical MOS gates. The increase in current is seen, with an increase in reverse bias and an upward shift is seen with an increase in gate bias. This upward shift in the gate bias response of the device as shown in Figure 6.21 depends upon the increasing thickness of the gate bias-induced accumulation layer. Here the results are shown while the device is in dark. The overlapping dual gate device was simulated and the current voltage characteristics showed an increase in current with increasing gate bias, when operated in dark. This is shown in Figure 6.6. Similar to the other IV characteristics in dark, at 0 V V_{DS} and at higher gate bias values, a gate leakage current is seen, to which an explanation has already been given in section 5.2.4.2 where similar response of an offset gate device is discussed.

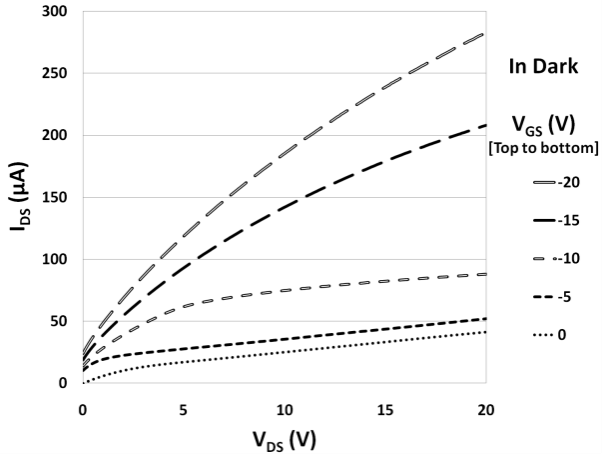


Figure 6.21: Current-voltage characteristics of the overlapping dual gate device in dark.

6.6.1.2 Transconductance

A transconductance plot derived from the current-voltage characteristics of the overlapping dual gate device measured in dark (Figure 6.21) is shown in Figure 6.22. This shows that the device nearly obeys square law and the terminal behaviour of the device appears as a transistor to the neighboring circuits. A transconductance value of 10 μA/V is seen at -15 V V_{GS}.

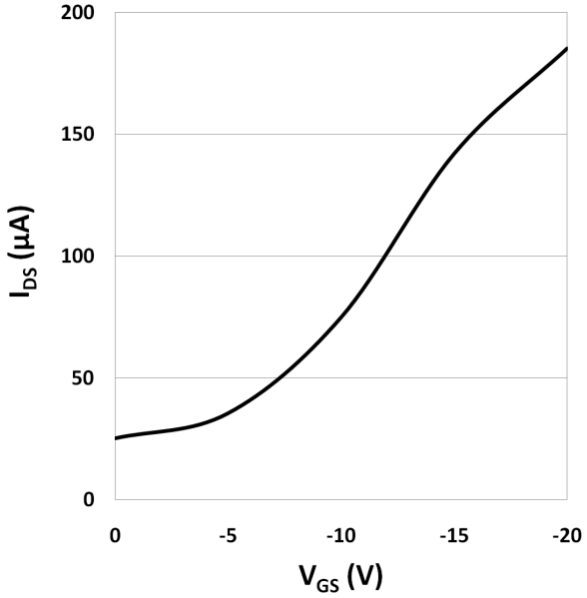
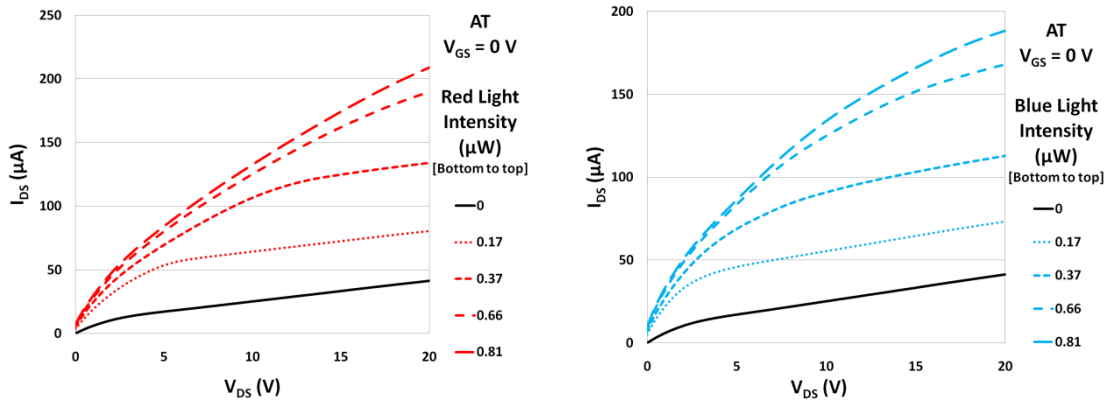


Figure 6.22: Electrical transfer characteristics of the over lapping dual gate device in the dark.

6.6.2 Optical Response

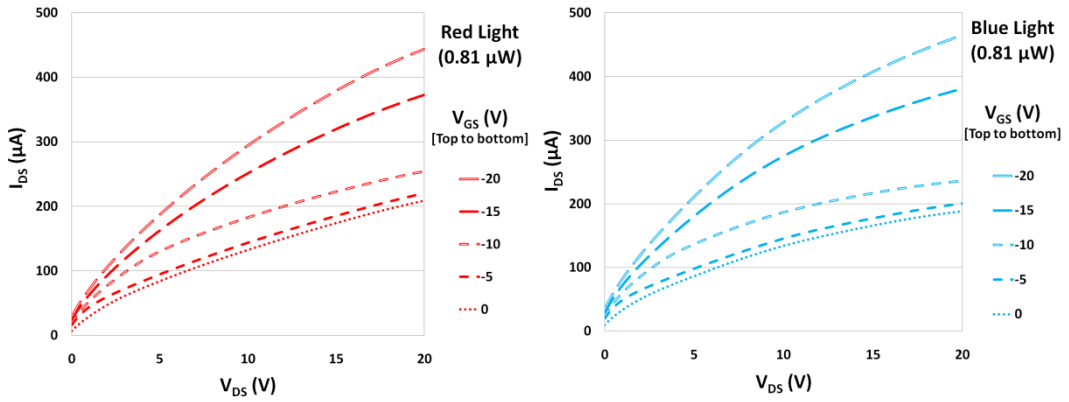
As discussed earlier, the device output current can be controlled through either controlling the intensity of incident light or by changing the gate bias voltage. The optical response of the device was measured in two configurations. In the first arrangement the reverse-biased diode element was characterized whereas the second set of measurements of the device deals with its transistorized configuration. The optical sources used for these measurements were exactly the same as those used for normal dual gate device measurements. In Figure 6.23 (a) and (b) the overlapping dual gate device was measured in its diode configuration with different intensities of red and blue light centred at 630 nm and 480 nm wavelengths, respectively.



(a) (b)

Figure 6.23: Optical response of the overlapping dual gate device with optical power as parameter in (a) red illumination (b) blue illumination.

The current-voltage characteristics of the overlapping dual gate device in its transistorized configuration are shown in Figure 6.24 (a) and (b). In both set of measurements as shown in Figure 6.23 (a) and (b) and in Figure 6.24 (a) and (b) enhanced blue sensitivity is seen. Here it should be noted that in Figure 6.24 (b) the overlapping dual gate device has shown higher response to blue than to red light, as shown in Figure 6.24 (a). Another graph is plotted where transistorized response of the overlapping dual gate device with red and blue light is meaningfully illustrated. In Figure 6.25 it is clear that at initial gate bias voltages, the overlapping dual gate device shows conventional response to red and blue wavelength radiations, i.e. higher response to red wavelengths than to blue wavelengths.



(a) (b)

Figure 6.24: Transistorized optical transfer characteristics of overlapping dual gate device with fixed intensity of (a) red illumination (b) blue illumination.

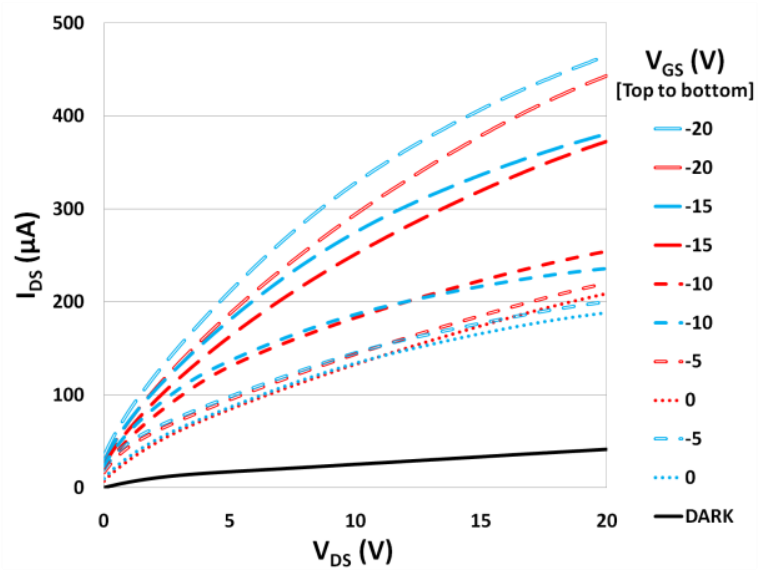


Figure 6.25: Current-voltage characteristics with red and blue light at different gate bias.

With further increase in gate bias voltage the response of the overlapping dual gate device to red and blue wavelengths became the same at around -13 V and from this point onwards, further increase in the gate bias showed a crossover behaviour in the overlapping dual gate device response to red and blue wavelength radiations. This feature is highlighted in Figure 6.26 where ratios $I_{DS(red)}$ to $I_{DS(blue)}$ and $I_{DS(blue)}$ to $I_{DS(red)}$ are plotted to show the crossover in the output current of the device to red and blue light at different gate bias voltages. This gate bias-induced modulation of spectral responsivity is as a result of the novel overlapping dual gate structure of the device. Here it should be noted that the normal dual gate device had also shown a trend of modulation in the spectral responsivity with gate bias. However, it had not shown the inversion of spectral responsivity, which is very much the case with the overlapping dual gate device.

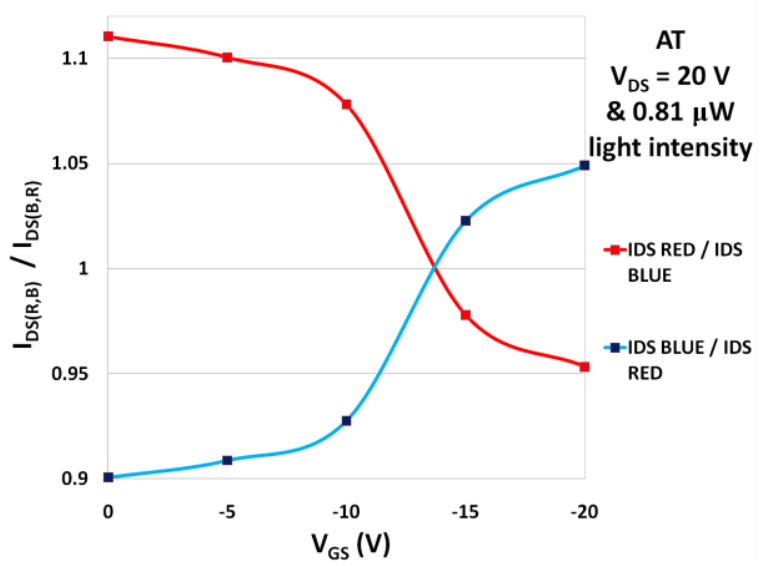
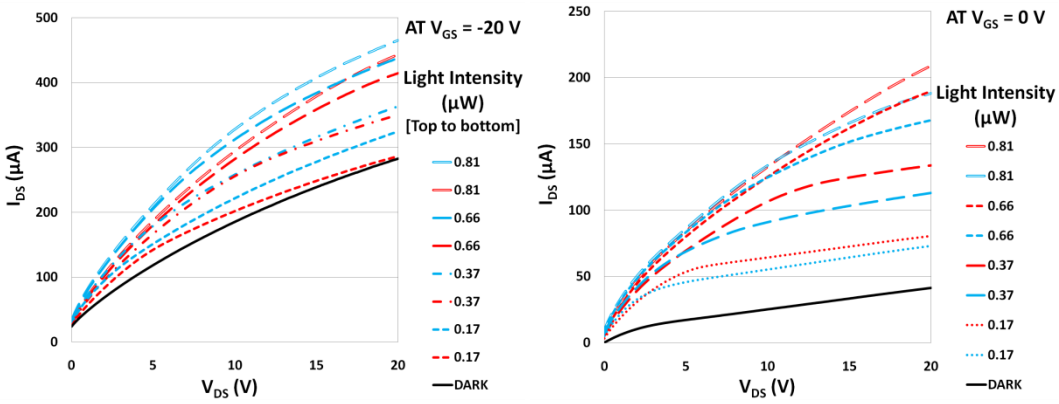


Figure 6.26: $I_{DS(red,blue)}$ / $I_{DS(blue,red)}$ as function of V_{GS} with fixed light intensity.

Furthermore, the overlapping dual gate device response in Figure 6.23 (a) and (b) is plotted together in Figure 6.27 (b). As this response is at 0 V gate bias, so it looks similar to the usual response of silicon photodiodes, although higher blue sensitivity is evident from the results. Yet another similar graph at -20 V gate bias is plotted in Figure 6.27 (a), where the inverted responsivity to red and blue wavelengths is shown. At 0 V to 10 V gate bias the overlapping dual gate device is more sensitive to red wavelength and at -15 V and higher gate bias the device responsivity changes and it becomes more sensitive to blue wavelengths. Here it should be noted that the curve for similar intensities of blue and red lights are plotted in similar style. At 15 V V_{DS} and -15 V gate bias overlapping dual gate device has shown 49.92 A/W and 55.89 A/W red and blue responsivity values, respectively. Whereas, at 15 V V_{DS} and -5 V gate bias the device has shown 50.43 A/W and 47.32 A/W responsivity values for red and blue lights, respectively. These high responsivity values and change in responsivity as a function of gate bias were due to novelty in the device architecture i.e. overlapping dual gates and surface depletion region of the device. It should be noted that, at -15 V gate bias, (at source side gate, while the drain side gate is at 0 V fixed reference potential) the device has shown 10.6 % increase in blue responsivity, whereas, at -5 V gate bias, the device has shown 6.16 % decrease in blue responsivity.

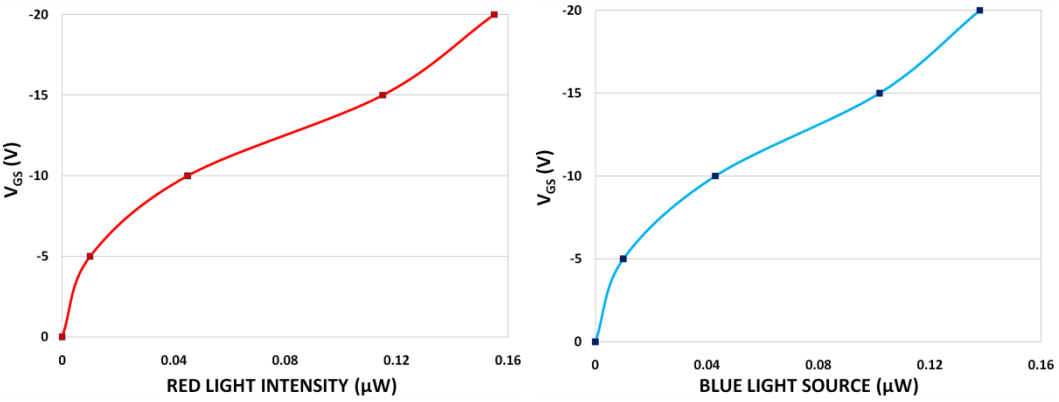


(a) (b)

Figure 6.27: Current-voltage characteristics with red and blue light intensities at (a) -20 V V_{GS} (b) 0 V V_{GS}.

6.6.2.1 Light Intensity to Gate Bias Correlation

It is clear that the overlapping dual gate device can be driven into saturation with either optical power or using high enough gate bias. Therefore, these two driving parameters can be used to derive a correlation. The light intensity to gate-source bias correlation graph is shown in Figure 6.28 (a) and (b) for red and blue light, respectively. It should be mentioned here that unlike the correlation graph for normal dual gate device for red and blue lights, the overlapping dual gate device, has produced slightly more output current with blue optical power than equivalent amount of red optical power. Numerically 0.15 µW red light intensity produced drain to source current equivalent to -20 V gate-source bias whereas 0.14 µW blue light intensity produced drain to source current equivalent to -20 V gate bias.

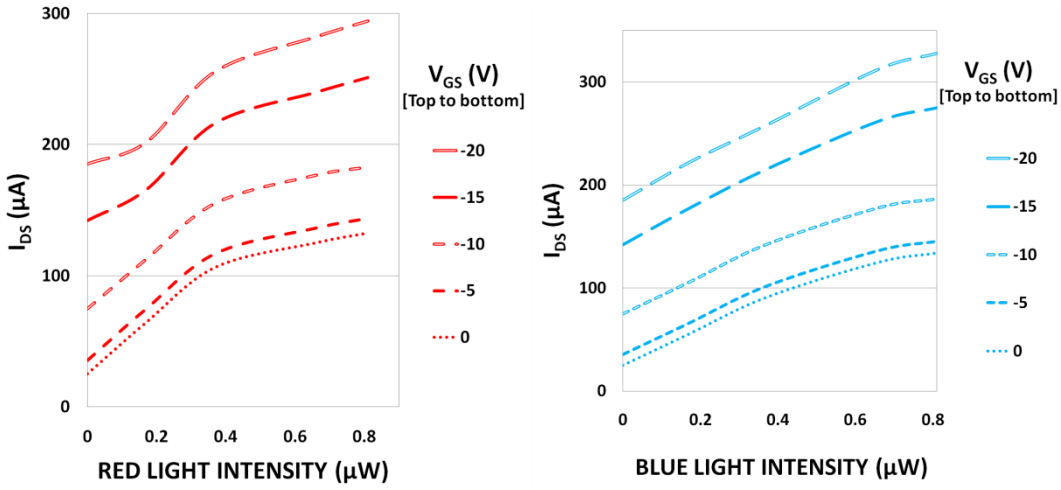


(a) (b)

Figure 6.28: Light intensity to gate-source bias correlation with (a) red light (b) blue light.

6.6.2.2 Optical and Electrical Transfer Characteristics

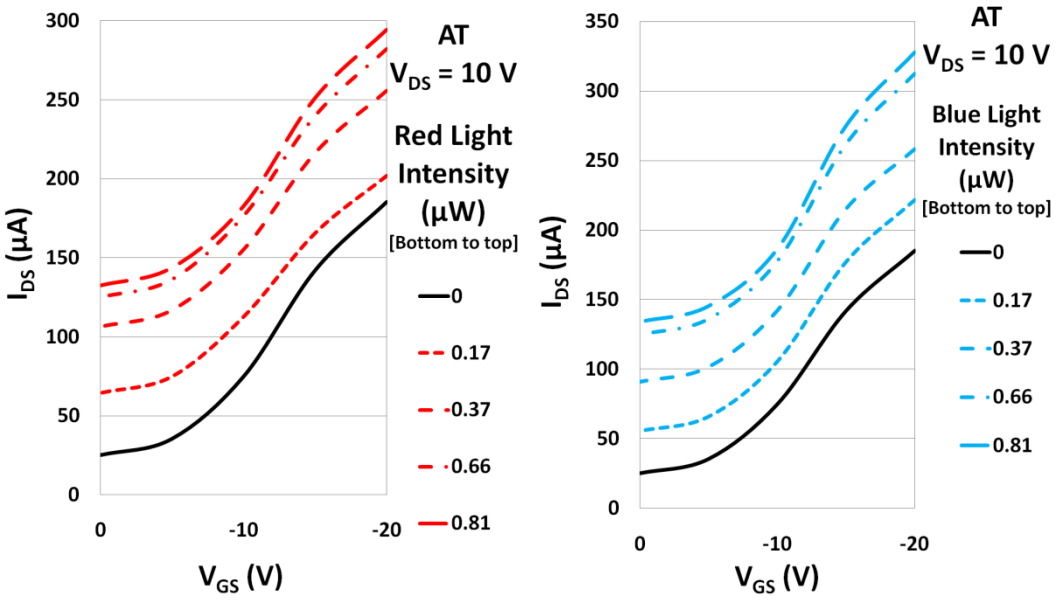
The optical transfer characteristics of overlapping dual gate device are shown in Figure 6.29 (a) and (b). The drain to source current showed linear variation as a function of red and blue light intensity.



(a) (b)

Figure 6.29: Optical transfer characteristics of overlapping dual gate device at different V_{GS} values with (a) red light (b) blue light.

The constant spacing between the electrical transfer characteristics of the overlapping dual gate device at different light intensities show that the increase in optically-generated drain to source current is fairly linear. This is seen in Figure 6.30 (a) and (b) for different red and blue light intensities. Here the solid black line is the device response in dark, whereas the other responses correspond to different red and blue light intensities. The electrical and optical transconductance curves show that the device follows square-law and would behave like an ordinary MOS transistor. The electrical transconductance value at V_{DS} = 10 V, V_{GS} = -10 V and incident optical power of 0.37 µW is 9.941 µA/V

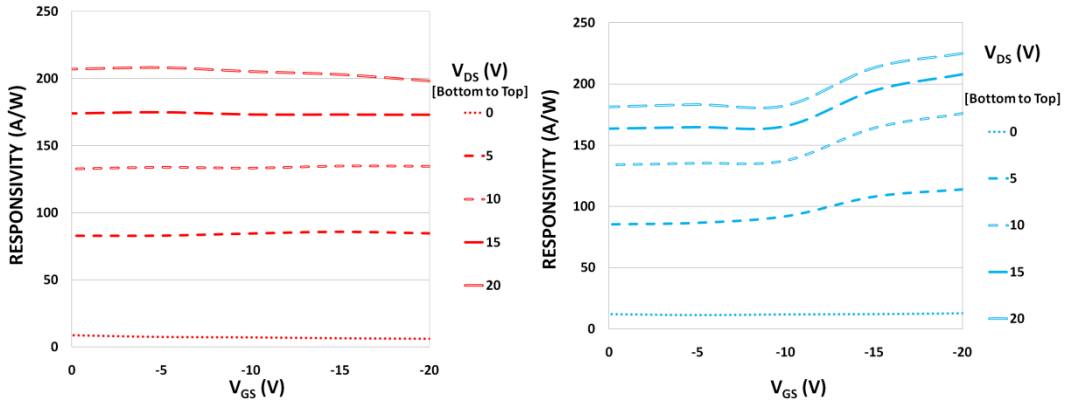


(a) (b)

Figure 6.30: Electrical Transfer characteristics of overlapping dual gate device at different light intensities with (a) red light (b) blue light.

6.6.2.3 Responsivity as a Function of Gate Bias

The absolute responsivity as a function of gate bias is shown here in Figure 6.31 (a) and (b). The absolute responsivity graphs for red and blue wavelengths clearly show that the red responsivity remains almost constant at all gate bias voltages, whereas the blue responsivity starts increasing beyond -10 V gate bias, as is shown earlier in Figure 6.26. The individual curves in absolute responsivity graph correspond to a typical V_{DS} voltage. The graphs are shown in Figure 6.31 (a) and (b) for absolute responsivity at red and blue wavelengths, respectively. Here responsivity changes as a function of gate bias, justify the device response in Figure 6.26 where the ratio of $I_{DS(red)}$ to $I_{DS(blue)}$ and the ratio of $I_{DS(blue)}$ to $I_{DS(red)}$ have been shown.

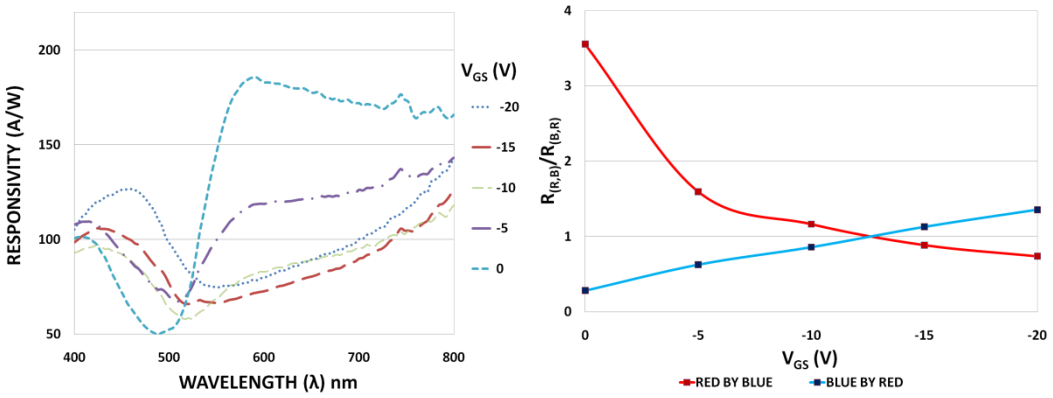


(a) (b)

Figure 6.31: Responsivity as a function of gate-source bias at different reverse-bias values with (a) red light (b) blue light.

6.6.2.4 Spectral Responsivity

Complete spectral responsivity results of overlapping dual gate device for 400 nm to 800 nm at different gate bias voltages are shown in Figure 6.32 (a). In Figure 6.32 (b) the ratio of responsivity at red and blue wavelengths and the ratio of responsivity at blue and red wavelengths is plotted to confirm the cross-over behaviour in spectral responsivity of the overlapping dual gate device. It should be noted that the spectral responsivity curves are vertically scaled to meaningfully compare the results at different gate bias values.

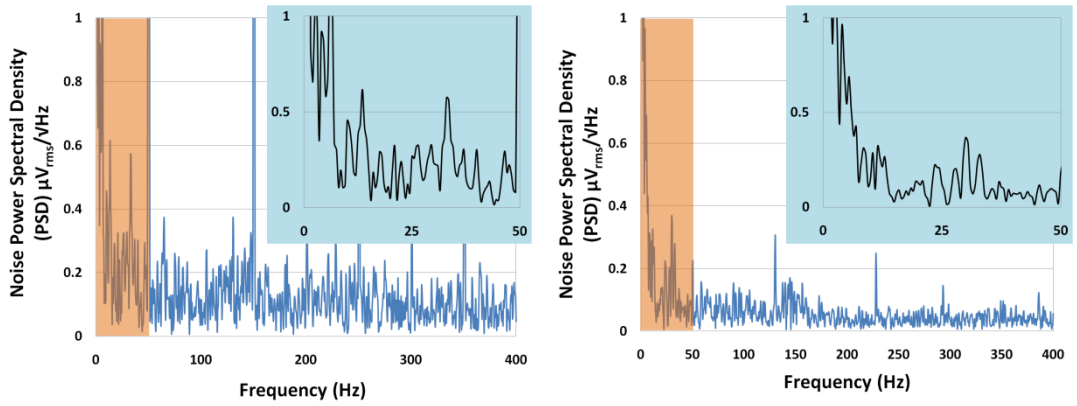


(a) (b)

Figure 6.32: (a) Spectral responsivity of the device (b) Ratio of red, blue and blue, red responsivity as a function of V_{GS}.

6.6.3 Noise Measurements

In Figure 6.21 at 15 V V_{DS} (reverse bias) in the absence of any gate bias, the dark current for overlapping dual gate device is 33 μA. This value is high as compared to that of typical conventional photodiodes and is even higher when compared to normal dual gate device. Noise measurements showed similar results as that for normal dual gate devices. In power spectral density measurements for overlapping dual gate device at V_{DS} = 10 V and at different gate bias voltages the device showed average noise voltage of a few $nV_{rms}/\sqrt{Hz}$ as shown in Figure 6.33 (a) and (b). The inset shows the highlighted region of the main graph. This low noise is simply because of the lateral continuation of gate dielectric, which serves as a passivation layer as well.



(a) (b)

Figure 6.33: Noise measurements of overlapping dual gate device with insets showing 1/f dependence of the pink highlighted section (a) at V_{DS} = 10 V, V_{GS} = 0 V, V_{DG} & BC = 0 V. (b) at V_{DS} = 10 V, V_{GS} = -20 V, V_{DG} & BC = 0 V.

6.6.4 Device Applications

The lateral p-i-n junction gated photodiodes have shown considerably higher spectral responsivity than typical, commercial vertical p-i-n junction photodiodes. Both the dual gate devices have also shown gate bias-induced modulation of spectral responsivity. The overlapping dual gate device has shown it to such an extent that there is crossover in gate bias-induced modulation of spectral responsivity. From the spectral responsivity data of overlapping dual gate device, a peak wavelength graph can be extracted, showing the wavelength of maximum responsivity at particular gate bias values. The peak wavelength shift

graph as shown in Figure 6.34 illustrates the overlapping dual gate device's coverage of the visible spectrum (400 – 700 nm) from -5 V to -10 V gate bias. Knowing all peak wavelength-shift values and by scanning the incident wavelength or monochromatic light source at all gate bias values for visible spectrum, the device in its current form can be used to specify the wavelength or colour of incident radiation. Therefore, the device can be used to make a colour sensor or a wavelength meter. This might become the basis of a silicon-based micro-spectrometer.

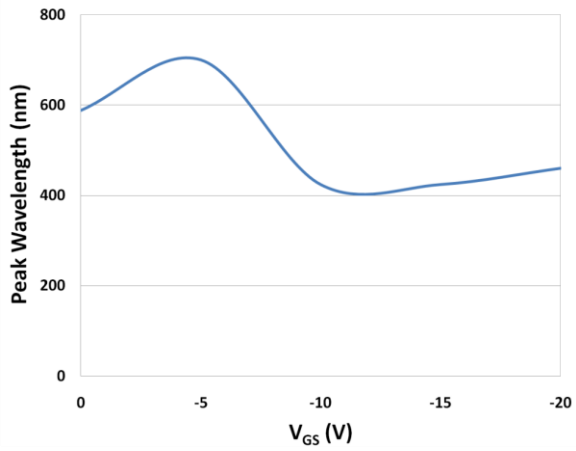


Figure 6.34: Peak wavelength shift as a function of V_{GS}.

6.7 Conclusion

In this chapter, electrically tuneable spectral responsivity in silicon-based photodetectors is described. The current flowing through these lateral p-i-n junction photodiodes can be changed by changing either the bias voltage applied to a system of metal-oxide-semiconductor (MOS) gates or the intensity of incident light. The normal dual gate and overlapping dual gate devices have exhibited optical responsivities of over 40 A/W and 50 A/W respectively. These devices when properly biased show enhanced blue response with overlapping dual gate device, the peak sensitivity of the device can be changed over the entire visible region by changing the gate voltage in a 5 V range. This happens because with increasing gate bias an accumulation layer of holes is pulled closer to the Si-SiO_2 interface. Furthermore, the device has a planar architecture and can be used on a CMOS platform.

6.8 References

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Chapter 7

Lateral p-i-n Photodiode & Optical Polarization Detection

7. Introduction

Detection of the polarization state of visible and near-infrared radiation is often required, for instance, in optical communications, magneto-optic data storage, astrophysics, stereo-sensitive bio-fluorescence studies and laser beam diagnostics [1, 2]. Solid-state light sensors with built-in polarization sensing capabilities can be of immense utility in such applications. Various attempts have been made in the past to develop such devices. Grating couplers were once shown to be capable of detecting the polarization state of incident free-space light beams. Polarization state of the incident free space light beam was detected, with the mode dispersion of waveguide and high selectivity of the coupling condition of the grating [3]. The devices were hard to fabricate and, therefore, did not see widespread commercial success. Nowadays the most widely used technique to accomplish this is the use of a linear polarizer coupled with a suitable light detector [4, 5]. This approach usually works satisfactorily but leads to system complexity and reduced sensitivity because of the extra absorption of light through the polarizing material. Polarization anisotropy of the absorption coefficient of ordered GaInP has also been utilized to fabricate polarization detectors and polarization threshold switches whose electrical output can be switched “on” and “off” by rotating the linear polarization of the input light [6]. Topographic detectors have also been proposed for detecting the polarization of

light. One such suggestion was made by Onat and Unlu. They demonstrated polarization detection with resonant cavity enhanced photodetectors suitable for use in the visible and infrared regions of the electromagnetic spectrum [7, 8]. An alternative approach was recently demonstrated by Chen and colleagues where they used a corrugated quantum-well infrared photodetector (C-QWIP) to analyse light into its orthogonal components [9]. Polarization-sensitive detectors have also been described in the nitride material family where Rivera and colleagues showed the possibility of building polarization-sensitive detectors from M-plane GaN photodiodes grown on $LiAlO_2$ substrates [10]. All of these approaches suffer from either fabrication complexity or reduced sensitivity. The integrated grating structure over the lateral p-i-n photodiode has high sensitivity to polarization detection and overcomes both of these objections. The device described in this chapter is a silicon photodiode with an integrated metal grating polarizer. This device is different from any such previous device in making use of the novel photodiode architecture described in earlier chapters. This is particularly effective at avoiding the loss of sensitivity common to other grating-based approaches. It is to be noted that optical polarization detection has assumed increased importance since the demonstration of polarized light emission from LEDs injected with spin-polarized currents [11]. Optical devices based on spintronics promise to enable new paradigms in information processing and the integration of complete functionality on monolithic chips will require polarization detection devices.

7.1. Polarization of Light

Light is a transverse electromagnetic wave where the electric and magnetic field vectors oscillate at right angles to each other. By virtue of its transverse character, light can be polarized such that the field vectors assume an ordered arrangement in space and time. For linear polarization the electric field vectors all lie in a well-defined plane called the plane of polarization. The magnetic field vectors then lie in an orthogonal plane. The process of transforming un-polarized light into polarized light is known as polarization. There are a variety of methods to make un-polarized light into polarized light. These include polarization by transmission, by reflection, by refraction and by scattering. If the magnitude of the electric field vector is constant in x and y direction and there is no change in the phases i.e. $\phi_x = \phi_y$ then the polarization is called linear polarization. But if there is a change in the phases such as $\phi_x = \phi_y \pm {}^{\pi}/_{2}$ and no change in the magnitude of the electric field vectors, then the

polarization is called circular polarization. When both the phase and the magnitude of the electric field vectors are not equal then the polarization is called elliptical polarization. Polarization effects can be seen in LCD screens and have many other applications in various fields.

7.2. Device Design and Fabrication

The base device used for single and dual gate architectures and integrated grating pattern was the same and had a lateral p-i-n architecture as explained in the device fabrication chapter. The base device geometry produced a low-capacitance, large-area light sensing device. The large available sensing area can be used to accommodate other functional structures. A polarizing grating is a good example of the type of structure that can be usefully integrated with a lateral p-i-n photodiode. After demonstrating the gated structures and their variations as described in Chapters 5 and 6, an integrated grating pattern was fabricated over the high sensitivity region using electron-beam lithography.

The gated structure as explained in earlier chapters, when properly biased is a CMOS compatible photodetector. The device thus appears as a transistor to the surrounding circuitry. However, the integrated grating pattern did not affect the diode-like behavior of the base device. Single gate photo-detectors exhibit enhanced sensitivity to short wavelength visible radiations [12]. This is due to the surface location of the depletion region. The integrated grating pattern, taking into account the increased responsivity of the base device, made the device sensitive to polarized light.

The structure of a lateral p-i-n diode is illustrated in Figure 7.1 (a) which shows the placement of the various regions, whereas in Figure 7.1(b) an SEM micrograph of the grating pattern is highlighted. An SEM micrograph of the device isolation trench is shown on the right Figure 7.1(c).

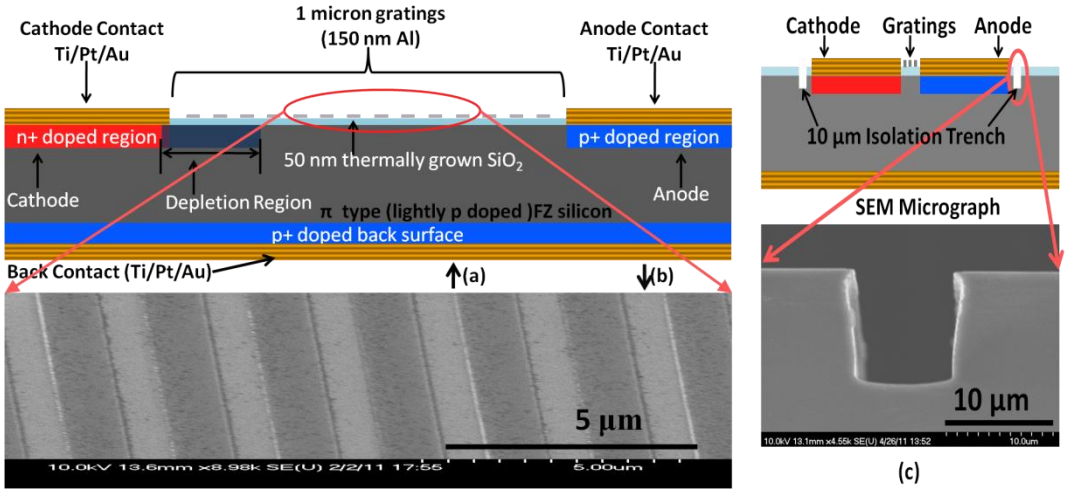


Figure 7.1: Integrated metal grating lateral p-i-n photodiode

(a) Schematic diagram showing the planar structure of a lateral p-i-n photodiode. (b) SEM micrograph of a grating-integrated lateral p-i-n photodiode. (c) Device Isolation trench surrounding the device structure.

A metal grating was fabricated in the middle intrinsic part of the diode by evaporating aluminium through a grating structure defined in resist using electron-beam lithography. Subsequent lift-off left the grating structure on the diode as an integrated element as shown in Figure 7.1 (b). Several thicknesses of aluminium films were investigated for this purpose. Some light managed to get through the thin films and because of the sensitivity of the lateral p-i-n architecture caused a reduction in polarization sensitivity. This issue was especially relevant in the context of sensing polarization sensitivity because the base device, i.e. lateral p-i-n photodiode has high sensitivity to blue light and the fact that the thin aluminium films become slightly more transmissive towards the shorter wavelengths of visible radiation. This can be seen in the percentage spectral transmission plot shown in Figure 7.2 (a). Here the light passed through a thin glass sheet which had a 50 nm thick aluminium film deposited on it. The transmission of light through thicker aluminium films was rapidly quenched, as seen in Figure 7.2 (b). Hence no light could pass through the metalized region of the integrated grating structure if its thickness was 150 nm or above. The noise seen in the plot of Figure 7.2(a) originates because a small amount of light makes it through the metal film. In order to block even the small amount of shorter wavelength light that might get into the device from the metalized part of the grating region, finally 150 nanometers of aluminium film forming the grating lines was used. A spectrum of the light source used for the measurements is shown in Figure 7.2(c). Figure 7.3 shows the optical micrograph of a typical grating pattern consisting of 14 lines, each 1 micron wide and 510 micron long with 1 micron gaps in between. This

covered almost all the 32 micron space in between the two lateral electrodes of the p-i-n device.

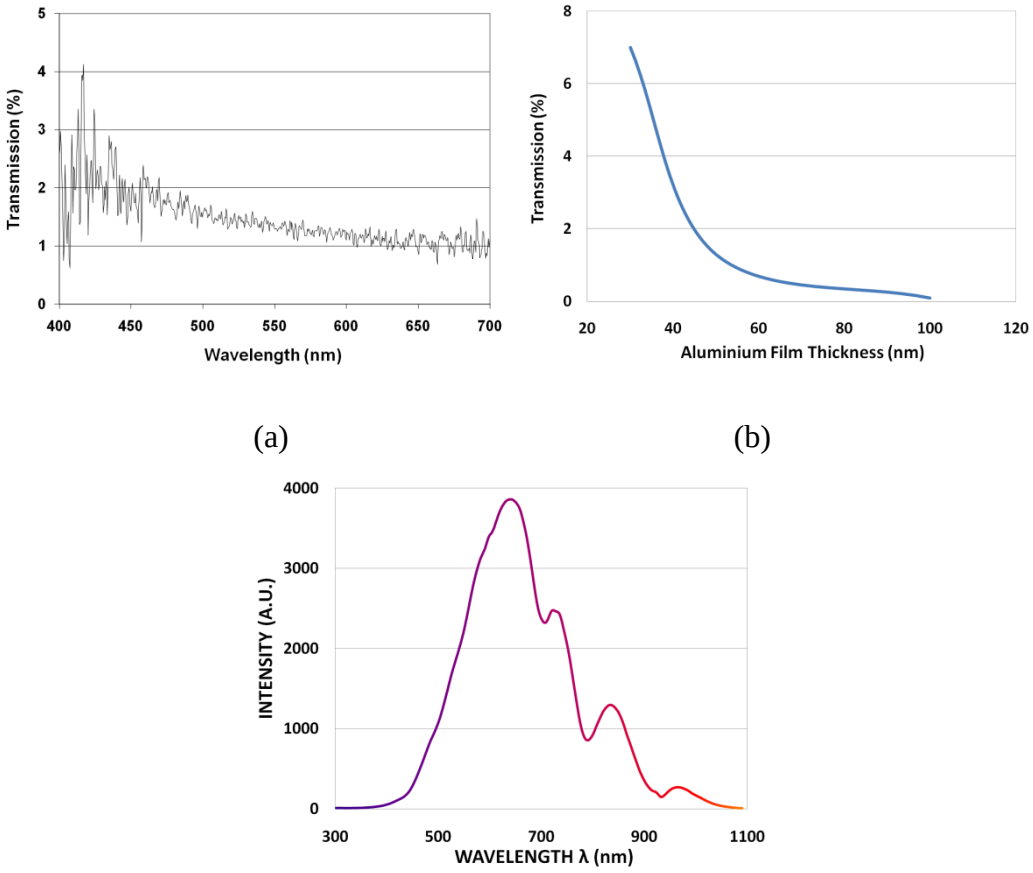


Figure 7.2: (a) Percentage transmission of incident light source (400 nm to 700 nm) at 50 nm Al thickness (b) Amount of light transmitted for various thicknesses of Al films. (c) spectra of light source used for polarization measurements..

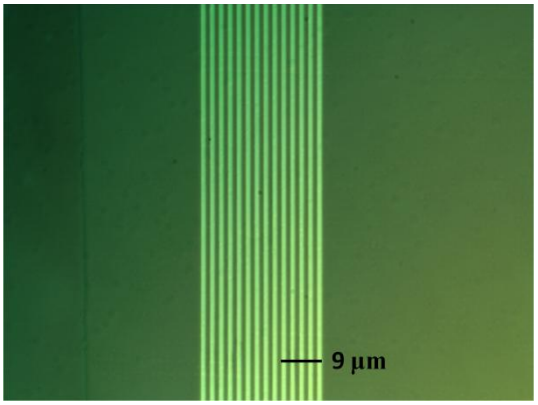


Figure 7.3: Optical micrograph of an aluminium grating.
The lines and spaces in between are all 1 micron wide.

7.3. Measurement Setup

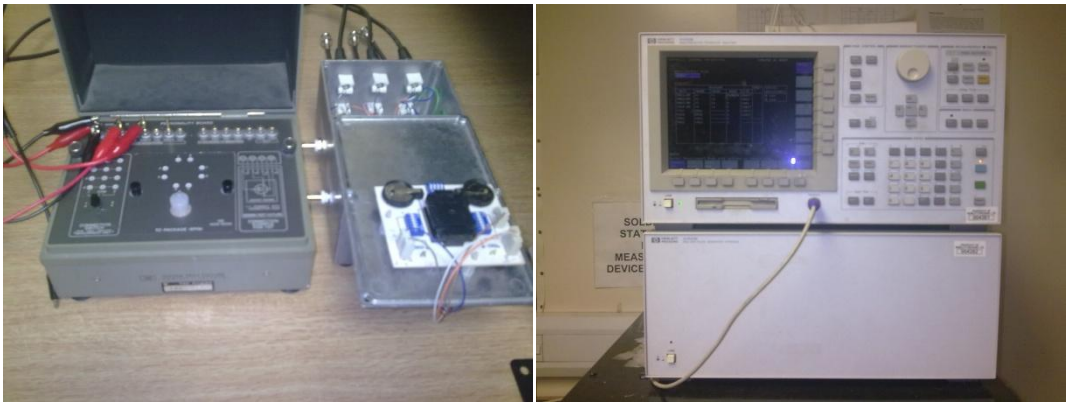
Polarization measurements were performed by using a goniometer holding a Kodak polarizing sheet at a fixed orientation. The neutral density polarizing sheet could generate light that was approximately 90% linearly polarized. The grating-integrated lateral p-i-n photodiode device was held at a fixed orientation while the polarizing sheet could be rotated with respect to it at different angles. The output voltage of the device was measured for different relative angles between the integrated grating lines on p-i-n photodiode and the direction of polarization i.e. the polarizing sheet. The polarization sensitivity measurement set up is shown in Figure 7.4. The bonded device on the ceramic chip carrier was placed inside the black box and its contacts were brought out to BNC connectors. The lateral p-i-n photodiode was reverse biased using an external power supply. This is usual with photodiodes. Upon illumination the device showed a voltage drop in the digital multimeter connected to the output of the device in the measurement setup. The difference of the output voltage before and after illumination gave the actual voltage drop for a specific angular position of the polarizer sheet with reference to the integrated metal grating pattern over the device. The same process was repeated for each referenced angular position of the polarizer sheet. The Polarizer sheet was rotated to complete 180 degrees of rotation for a complete set of measurements.

(a) (b)

Figure 7.4: Experimental setup for Polarization sensitivity measurements (a) with light and (b) without light

These forward and reverse bias current-voltage (IV) measurements were taken with an HP 4155 semiconductor parameter analyzer (SPA). An image of the measurement setup for IV measurements is shown in Figure 7.5. Figure 7.5(a) shows how, the bonded device was placed inside the black box and connected to the SPA setup through coaxial cables, whereas in Figure

7.5 (b) programmable interface and output screen of the semiconductor parameter analyzer are shown.



(a) (b)

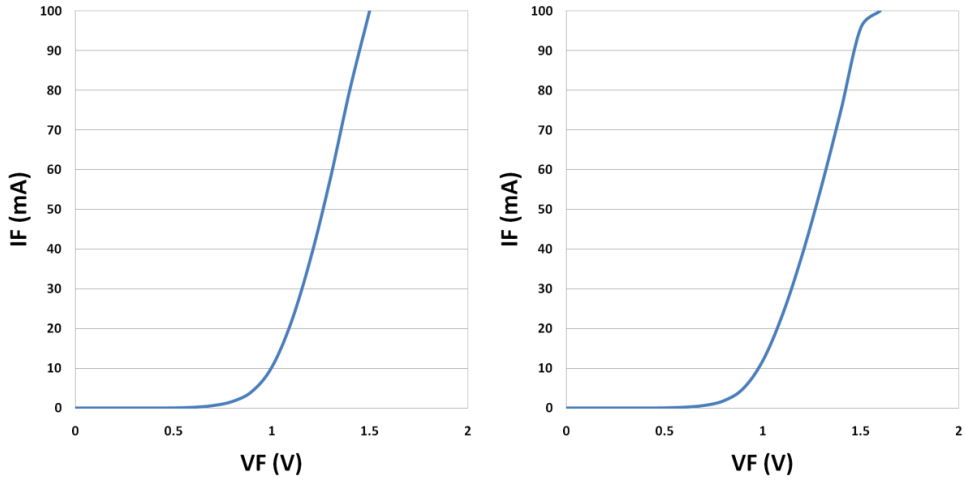
Figure 7.5: Current-voltage (IV) characteristics measurement setup

7.4. Device Characterization

In this section forward and reverse bias characteristics of the device are described.

7.4.1. Forward Bias IV Characteristics

Forward bias, current-voltage (IV) characteristic measurements were carried out on the base device using a semiconductor parameter analyzer. The forward bias characteristics appear here in Figure 7.6 (a) and (b) for 50 nm and 150 nm thick integrated metal grating devices, respectively. As the forward bias current-voltage measurements were taken in dark, so the response of the two devices does not take into account the thickness of metal integrated grating pattern. Here the description of the grating pattern is just to differentiate between the two different devices of similar base structure fabricated under similar conditions. Both the devices have similar forward characteristics curve and is comparable to that of a conventional p-i-n photodiode with vertical doping profile.



(a) (b)

Figure 7.6: Forward bias (IV) current-voltage characteristic of lateral p-i-n diodes in dark.
(a) 50 nm thick integrated grating (b) 150 nm thick integrated grating

7.4.2. Reverse Bias IV Characteristics

In the present series of measurements dark current was measured for both the silicon based lateral $p-i-n$ junction diodes using the semiconductor parameter analyzer arrangement. Both devices showed similar reverse bias current-voltage (IV) characteristics as shown in Figure 7.7 (a) and (b), respectively. Similar forward and reverse bias response of both the devices established that any variation in optical response of the devices would be influenced by the variation in the integrated metal grating structure. This is further clarified in the polarization sensitivity measurements section.

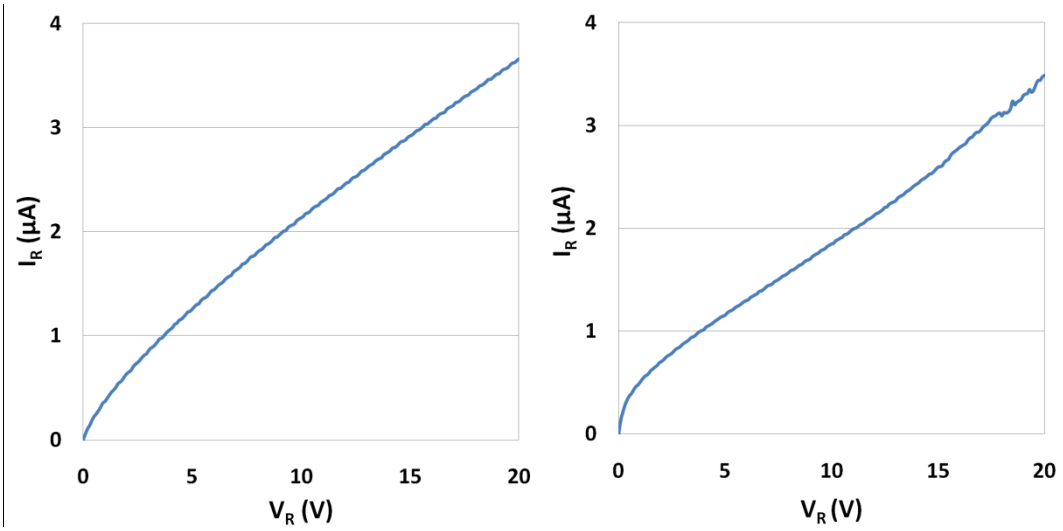


Figure 7.7: Reverse bias characteristics of lateral p-i-n photodiode
(a) 50 nm and & (b) 150 nm thick aluminium integrated grating devices

7.4.3. Polarization Sensitivity Characteristics

Similar to other photoconductive measurements, the polarization sensitivity measurements were performed when the p-i-n diode was reverse biased. These measurements were taken at different relative angles by rotating the polarization states of the incident light over the integrated metal grating based p-i-n diode. The voltage that was measured was developed across a biasing resistor such that larger photocurrents resulted in lower voltages being measured and vice versa. This arrangement is usual when photodiodes are used in reverse bias. A larger fraction of the incident light getting through would be expected to produce more photocurrent and thus a lower output voltage.

The device with 50 nm thick integrated metal grating structure was measured. The voltage drop was measured as a function of the angular position of the polarizing sheet with respect to the integrated metal grating pattern over the device and is shown in Figure 7.8. The measurement started with the direction of the polarizing sheet orientated parallel to the integrated metal grating pattern. As can be seen from the plot the device then produced a low output voltage consistent with a large photocurrent flowing through it. As the relative angle was increased the photocurrent decreased, this resulted in increased output voltage. The 50 nm thick aluminium metal layer becomes slightly transmissive for short wavelength of light as shown in Figure 7.2(a). Some short wavelength light therefore managed to get into the device even through the metalized part of the grating pattern. This produced a little photo-current independent of the degree of polarization. This fraction of photo-current in conjunction with photo-current produced through polarized light caused less output voltage. This voltage difference was always higher than in the device with 150 nm thick integrated metal grating as shown in Figure 7.8 & Figure 7.9.

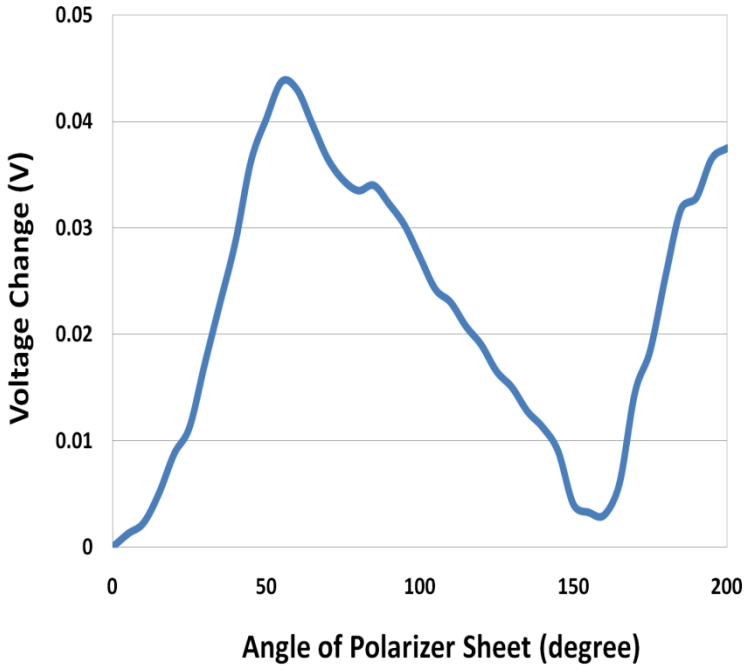


Figure 7.8: Polarization response of the grating-integrated sensor with 50 nm thick Aluminum Gratings.

Thicker (150 nm) aluminium metal layer is quite opaque, thus the polarized light can get into the device through the non-metalized clear regions only. In photoconductive mode, the photo-current is proportional to the incident optical power. In this device, light only managed to get in through the clear regions and produced less photocurrent and a higher voltage output as is seen in Figure 7.9. The photo-current produced here is therefore only based on the angle of polarization and is better behaved than for the 50 nm thick aluminium metal gratings. Figure 7.8 & Figure 7.9 differentiate both the devices with respect to their voltage-drops. Higher voltage drop was seen in Figure 7.9, due to the fact that the response was absolutely based on the polarized light at different angular positions that managed to get into the device and the opacity of the 150 nm thick metal grating that immediately quenched the transmission of light through metalized region. Furthermore, the total response in Figure 7.9 is a result of sensing the polarized light through the grating pattern only. In contrast the 50 nm thick aluminium gratings allow small amount of light to penetrate into the device through the metalized part of the gratings as well. More light means higher photocurrent and thus low output voltage as shown in Figure 7.8.

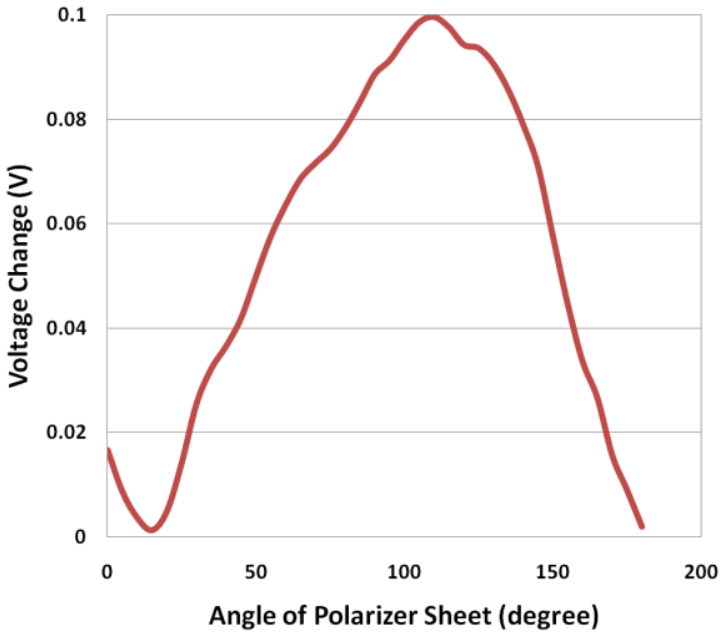


Figure 7.9: Polarization response of the grating-integrated sensor with 150 nm thick Aluminum Gratings.

The effect of light leaking through the thin aluminium lines of the 50 nm thick aluminium film sample is seen in the reduced dynamic range for that device (44 mV) versus that for the device with 150 nm thick aluminium film (100 mV). The 56% reduction in dynamic range for polarization sensitivity shows the effect of the presence of extraneous light injection in these devices. The polarization sensitivities for the 50 nm thick and the 150 nm thick aluminium samples were 0.48 mV/degree and 1.1 mV/degree, respectively.

Another nice feature of this device is that its polarization response is wavelength neutral throughout the visible part of the spectrum. Although the device's sensitivity depends on the range of wavelengths used to illuminate it, the output signal due to polarization changes is independent of the exact colour of light incident on the device. This is shown in Figure 7.10.

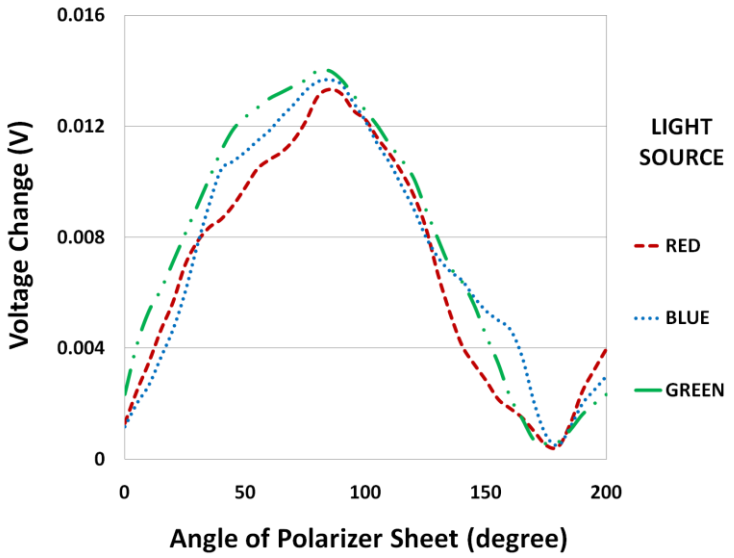


Figure 7.10: Polarization response of the grating-integrated sensor with red, green and blue linearly polarized light.

Reverse bias characteristics were taken for both the devices in dark and in un-polarized light i.e. without a polarizer sheet. Looking at Figure 7.11 (a) and (b) where, reverse bias characteristics in dark (dotted line) and in un-polarized light (dashed line) are shown for both the devices. Here light of the same intensity was incident on the device as was used for polarization sensitivity measurements. Reverse bias characteristics in dark for both the devices were approximately the same, whereas the photocurrent produced for 50 nm thick aluminium metal grating structure was higher than for the 150 nm thick aluminium metal grating structure. This compliments the lower output voltage phenomenon for 50 nm thick metal grating device and the higher output voltage for the device based on 150 nm thick metal grating structure.

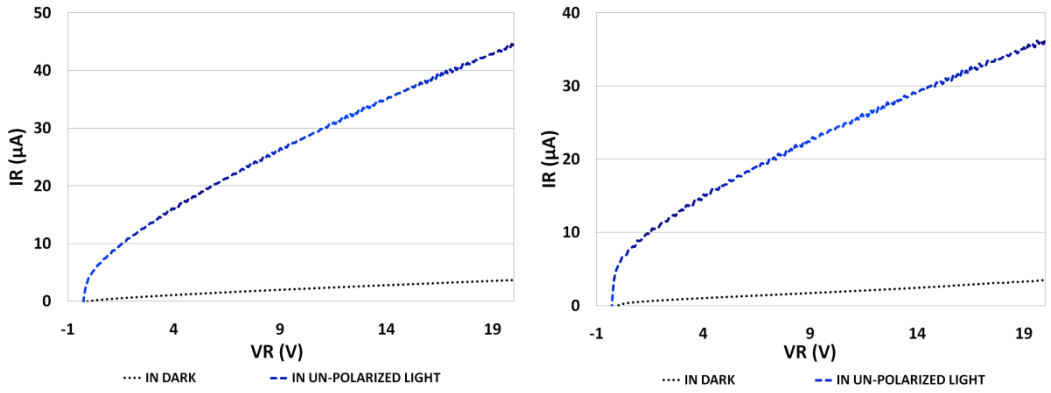


Figure 7.11: Reverse bias current-voltage (IV) characteristics in dark and with un-polarized light. (a) with 50 nm thick aluminium grating (b) with 150 nm thick aluminium grating

We see that the lateral p-i-n junction architecture endows the device with enhanced sensitivity so that it can detect changes in linear polarization even when the incident light is quite weak.

7.5. Conclusion

In this chapter a grating-integrated semiconductor polarization detector is characterized that makes use of a novel base device as the underlying light sensor. The lateral p-i-n junction architecture endows the device with enhanced sensitivity so that it can detect changes in linear polarization even when the incident light is quite week. This is a result of the surface location of the light-detecting depletion region in the device. The polarization response was found to be wavelength independent in the visible region where such measurements were taken with broadband red, green and blue illumination. The device can be potentially used for detecting and monitoring the plane of polarization of light in electro-optical instrumentation, bio-medical equipment and visible light optical communication systems.

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Chapter 8

Summary and Suggested Future Work

8. Introduction

Monolithic optoelectronic integrated circuits have, to a great extent, overcome the limitations in electrical interconnects. Integrated photodetector and its circuitry on the same substrate has reduced electrical parasitic, increased the speed of operation and has become, generally, a more reliable and cost-effective solution for emerging optoelectronic applications. Increasing the flexibility of optoelectronic components, such as detectors, through electronic control has been the subject of this work. The fabrication process of a CMOS-compatible, light sensing device is described in Chapter 4 and its characteristic response is further described in Chapters 5 and 6. It has the lateral structure of a p-i-n junction photodiode, whereas its vertical structure appears like a transistor to the surrounding circuitry. In fact the partial gate(s) over the intrinsic region controls the lateral conduction of the device, making the device appear as a transistor to the surrounding circuitry. In Chapter 7, a possible use of the wide surface depletion region is described by characterizing the sensitivity of grating-integrated p-i-n junction devices to linearly-polarized visible light. This chapter contains a summary of the work and proposed future enhancements.

8.1. Summary

Silicon's intrinsic properties make silicon detectors a suitable choice for radiation detection in the near-infrared and visible region. It also provides radiation-hardness and thus can also be used in high energy physics experiments as a particle detector. Silicon naturally provides a better quality dielectric – SiO_2, through thermal oxidation which is another advantage in making detectors out of silicon. Silicon detectors are used in a variety of applications, in digital cameras to form images with visible light, in particle physics experiments to detect charged particles, in astrophysics satellites to detect X-rays and gamma rays and in many other consumer and industrial applications.

The work described here on lateral p-i-n junction photodiodes was motivated by the limitations of ordinary diode-based photodetectors. The diode structure limits the tuneability of the device, as the operating characteristics of such a device cannot be changed, once fabricated. In bipolar junction photo-transistor the base terminal when properly utilized, can be used to adjust the operating characteristics. It however, does not conform to the CMOS fabrication process and therefore cannot be integrated with other circuit elements.

The hybrid device developed in this work, operates as a reverse-biased p-i-n junction photodiode and therefore detects light through pn-junction mediated charge carrier separation, whereas a partial insulated gate on the top is used to control the quiescent operating point thus making it easy to interface the detector with ordinary MOSFETs. Single and dual gate photodiodes are described in Chapters 5 and 6. The characteristics of single gate devices are more like a typical silicon photodetector which has a buried depletion layer. Although these devices showed higher responsivity to red light ($\lambda = 630$ nm), yet their response to short wavelength radiations (blue light $\lambda = 480$ nm) was considerably enhanced due to the lateral p-i-n structure. The performance of these devices can be further enhanced to show better response at even shorter wavelengths i.e. below 350 nm. This would require an even thinner dielectric layer so that the high energy photons may pass through the thin dielectric layer and get absorbed in the top of the silicon surface. The speed of operation can be increased by careful scaling of, the near-intrinsic region and the placement of insulated gate structure in relation to the width of the depletion region.

The intensity of incident radiations influences the reverse bias response of a typical photodiode. The partial gate in the gated lateral p-i-n photodiode controls the lateral conduction in a somewhat similar way. These devices therefore have two control parameters i.e. intensity of light and the gate bias that control the lateral conduction of the device.

Unlike the conventional p-i-n photodiode this lateral p-i-n photodiode has shown higher level of dark current and higher output noise values. These values are higher than the reported values for typical silicon photodiodes with vertical doping structure. The lateral continuation of SiO_2 has contributed in reducing the $Si - SiO_2$ interface noise, whereas the dark current can be reduced by fabricating this device on SOI material.

Both, normal dual gate and overlapping dual gate photodiodes showed similar characteristics as described in Chapter 6. In dual gate devices, the two gates can be used to control the lateral conduction of the device. Biasing the two gates produces an inversion or accumulation layer underneath the respective gates. The bias on the gates and distance of the induced layer from the respective electrodes i.e. source or drain, influence the spectral response of the device. This change in spectral responsivity is much pronounced in the case of overlapping dual gate structure. An analytical model of the device operations is also discussed in Chapter 6.

With the increase in bias on the source side gate with respect to the drain side gate (negative bias on the source side gate, while the drain side gate experiences zero reference potential) and reverse bias on lateral p-i-n junction photodiode, the lateral conduction of the device increases and a change in spectral sensitivity is seen. However, at a certain gate bias the device exhibits the same responsivity to blue light at 480 nm wavelength as the responsivity to red light at 630 nm wavelength. With further increase in gate bias the responsivity of the device increases for blue light (480 nm wavelength) in comparison with that for red light (630 nm wavelength), which is unlike the response of typical silicon-based photodetectors.

The test results show that 50 nm of SiO_2 layer requires 23 V to breakdown, therefore the results described in Chapter 6 are from 0 to -20 V gate-source-bias. In normal dual gate devices the spectral responsivity changes with change in gate bias, but at no gate bias value the red and blue spectral sensitivities are inverted. In normal dual gate devices, the use of thicker dielectric layer would increase the dielectric breakdown voltage. It however, may or may not invert the spectral response of the device at the two wavelengths i.e. for red and blue

light. The device with overlapping dual gate structure showed gate bias-induced modulation of spectral sensitivity, simply by overlapping the gates over the p and n doped regions, when biased at 0 V to -20 V. Overlapping dual gate device characteristics demonstrate that the peak spectral responsivity at different gate bias values (-5 V to -10 V) covers the complete visible spectrum i.e. from 400 to 700 nm wavelengths. Therefore, if a monochromatic light of a specific wavelength falls on the device and the device scans it for all gate bias values to sense visible light, it is possible to find the value of the wavelength of the incident radiation. Therefore, the overlapping dual gate device at this stage can be used as a colour sensor or in a wavelength meter. This might become the basis of a silicon detector as a micro spectrometer or as a lateral p-i-n CMOS imager.

It is essential to study the tradeoffs between the interdependent design variables in the fabrication of a new detector in order to operate the detector in a specific or varying wavelength region. Some ideas are given here for future work to look into further possibilities available with the silicon lateral p-i-n photodetector architecture.

8.2. Future Directions

The hybrid transistor-like-photodiodes described in Chapters 5 and 6 and possible applications to utilize the surface depletion region in the lateral p-i-n photodiode presented in Chapter 7 are preliminary possibilities. These investigations have identified some interesting directions for future work in gated lateral p-i-n junction photodiodes. There is a possibility to either modify the design of the single and dual gate structure over the lateral p-i-n photodiodes or to make two dimensional (2D) arrays to uncover the hidden potential of these devices in different applications. These may include imaging, security and medical applications, among others. The fabrication process and structure of the standalone devices as described in Chapters 5 and 6 can be further improved and new structures as described in the following sections, which use the lateral p-i-n base architecture, can be fabricated. The following sections will highlight the possibilities for future work.

8.2.1. Structural Change in Single Gate Devices

A similar set of devices can be fabricated and characterized using lightly n doped $'\upsilon'$ type float zone silicon or with silicon-on-insulator (SOI) material. Once the devices are fabricated with

the new material, their controlling parameters can be modified to suit different applications. These parameters are thickness of the oxide layer, placement, dimension and structure of the gate. A new single gate structure with suitable dimensions can be made over the intrinsic part of the device between the two surface electrodes, leaving the window above the depletion region uncovered as an inlet for incident radiations. Biasing the gate would result in electrical shrinking of the device and this can increase the bandwidth response of the device as well. A possible device structure is shown in Figure 8.1.

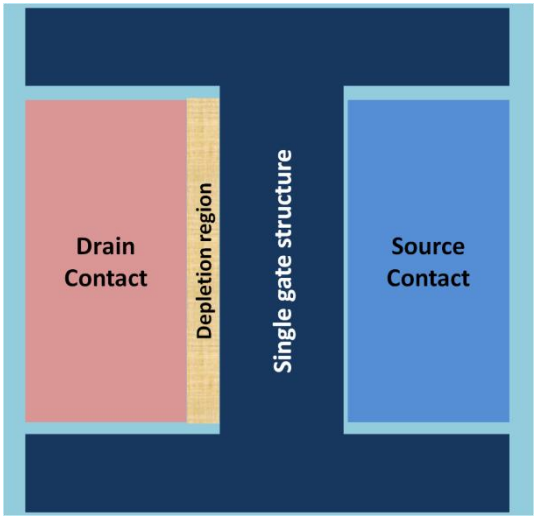

Figure 8.1: Single gate covering the near-intrinsic region in between the two electrodes

8.2.2. Expanding Lateral p-i-n Structure to an Array

Standalone grating-based lateral p-i-n junction photodiode as described in Chapter 7, where, its sensitivity to linearly polarized light is discussed. A similar 2D array of lateral p-i-n junction photodiodes can be used to make an integrated metal grating-based device useful for determining the plane of polarization of incident light. The concept of such a device is discussed in section 8.3.2.1. Devices which employ gates and are integrated in a 2D array can either operate by applying gate bias on each individual gate or all gates of the same type can be merged together to bias them collectively. The distance between the two gates when properly biased in a dual gate device controls the device functionality, in addition to the conditions described in section 8.2.1.

8.2.2.1. p-i-n Junction Photodiode Array to Detect the Plane of Polarization

Here the concept of a lateral diode array is discussed where four lateral p-i-n junction photodiodes "A-E", "B-E", "C-E" and "D-E" are used together. Here contact "E" is a phosphorous-doped drain contact and is shared among all surrounding source contacts. This square-shaped n contact is surrounded by four boron-doped square-shaped p contacts namely "A", "B", "C" and "D" as shown in Figure 8.2. The near-intrinsic part of the three lateral p-i-n photodiodes namely "A", "B" and "C" is covered with integrated metal gratings at 0 degree, 90 degree and 45 degree orientations, respectively, whereas the depletion region of the fourth p-i-n junction photodiode "D" is left uncovered. When light falls on the "quad" lateral p-i-n photodiode, the response from any of the three p-i-n photodiodes with integrated metal gratings is compared with that of the fourth uncovered p-i-n photodiode to determine the plane of polarization. There is a possibility that four of these devices may have slightly different responses and therefore this correction factor must be taken into account while calculating the plane of polarization. Surrounding the device with an isolation trench would isolate the four devices to limit their influence on the surrounding devices.

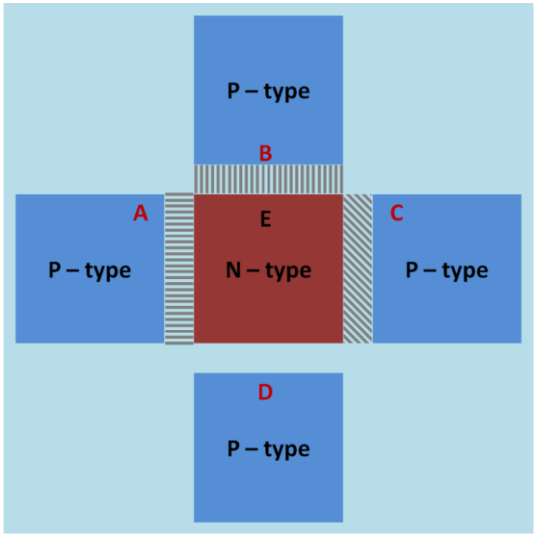

Figure 8.2: Array of lateral p-i-n photodiode for angle of polarization detection

8.2.2.2. 2D Array of Gated Lateral p-i-n Photodiodes

The characteristics of overlapping dual gate device described in Chapter 6 showed its possible use as a colour sensor. In the proposed 2D array of overlapping dual gate lateral p-i-n

photodiodes, each pixel i.e. pn-junction, would scan the incident light at gate bias values with peak sensitivities in red, green and blue regions. This way a single pixel in an array will sense the colour and intensity of the incident light. Whereas, CCD-based digital imagers use a complex algorithm based "demosaicing" method to reconstruct the image from colour CCD samples [2]. The CCD treats a set of 2x2 (red, green, blue green) pixels as a single unit to estimate the actual colour intensity. In the proposed CMOS imaging arrays each pixel will store intensity and colour information to reconstruct the image.

Due to large scale interconnects the proposed device features large pixel sizes and, therefore, cannot capture images with high resolution. It, however, has effectively a large number of pixels compared to a normal array, i.e. in a 3 x 3 array the proposed device has 12 pixels as against 9 pixels in the normal CCD. Due to its novel architecture, it does not require any colour filters, yet it has processing overhead limitations to store three times more data compared with a normal CCD imager. Furthermore, CMOS imagers are superior to CCDs as they utilize less power and can result in miniaturized imaging system (the later is not true at the current stage of this proposed CMOS imager). CMOS imagers are now designed for IP security cameras and are used in intelligent vehicles, mobile cameras and high-speed machine-vision cameras. A 3x3 array of lateral p-i-n photodiode is shown in Figure 8.3. Here it should be noted that one set of a p-i-n diode forms one pixel.

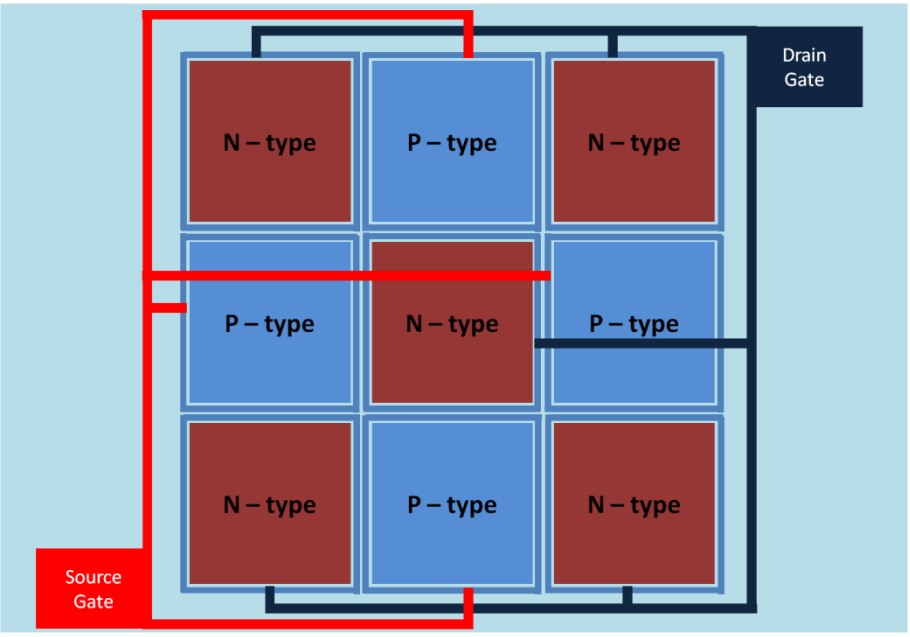

Figure 8.3: 2D array of lateral p-i-n junction photodiode with overlapping double gate structure

8.2.2.3. Thermal Imaging Array

Silicon has its peak responsivity in the infrared region at around 900 nm to 1000 nm range. Beyond 1000 nm, the responsivity of silicon falls sharply and silicon becomes transparent beyond the cutoff wavelength i.e. 1100 nm. Radiation beyond 1050 nm penetrates more than 500 μm inside silicon and therefore is less likely to be absorbed. Penetration depth of radiation in the 400 to 1100 nm range in silicon is shown in Table 8.1

A 2D array of lateral p-i-n photodetectors as shown in Figure 8.3 can be patterned with a coating of material that blocks visible radiations on alternate pixels as shown in Figure 8.4. These visible-blind pixels i.e. the coated ones, will allow only the infrared radiation to pass through, whereas the uncoated pixels will let both the visible and infrared radiations to pass. This way the proposed detector array can keep track of both visible and near-infrared radiations through alternate normal and visible-blind detector elements.

The proposed array can be used for applications like near-infrared night vision system in conjunction with a near-infrared illuminator. A near-infrared lamp illuminates the scene that is eventually captured by the proposed 2D imaging device. Typical near-infrared wavelength used to illuminate the scene is in the range of 800 nm to 900 nm, which a human eye cannot detect. However, the captured image through the near-infrared CCD or CMOS imager resembles closely the human visual perception. It should be noted that night vision systems are offered by premium automotive brands to enhance the driver's ability to see at night [3]. Using the proposed device a low light video security surveillance system can also be developed.

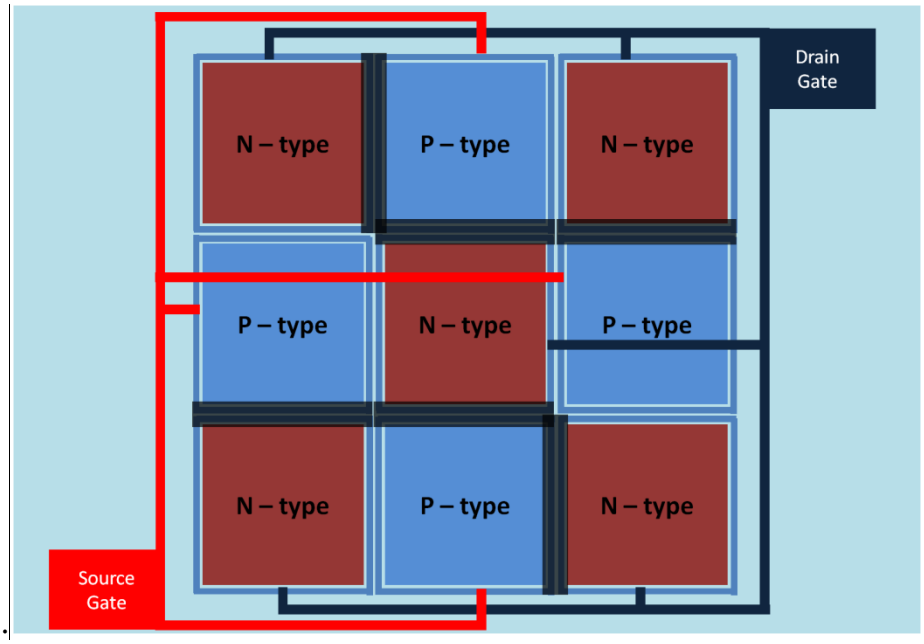

Figure 8.4: 2D array of p-i-n photodiode for night vision applications.

Wavelength (nm)	Penetration Depth (µm)
400	0.19
450	1.0
500	2.3
550	3.3
600	5.0
650	7.6
700	8.5
750	16
800	23
850	46
900	62
950	150
1000	470
1050	1500
1100	7600

Table 8.1: Photon absorption depth at different wavelengths

8.2.3. Mesa p-i-n Photodiode Structure

The quantum efficiency of semiconductor detectors varies with change in wavelength of the incident radiation. Therefore, normal silicon detectors do not show similar quantum efficiency for short and long wavelength radiations i.e. for blue and red regions. The proposed mesa p-i-n photodiode has a lateral doping structure. Here the proposed device is doped through the side walls of the mesa structure and the patterned top surface as well. Therefore, the diffused region starts right from the silicon top surface and extends deep inside the silicon through the walls of the mesa structure, making the depth of the doped region equal to the height of the mesa structure i.e. 150 µm. The penetration depth of near-infrared photons i.e. up to 950 nm wavelength is 150 µm. Therefore, the device would show similar quantum efficiency values for 400 nm to 950 nm radiation.

The proposed mesa device can have the gate structure as shown in Figure 8.5. The proposed mesa lateral p-i-n photodetector is expected to reduce the dependence of the carrier transit distance on the light absorption depth and might give high-speed and better responsivity [4]. A simple device with lateral mesa p-i-n junction structure can be characterized first and then the gate structure can be incorporated accordingly.

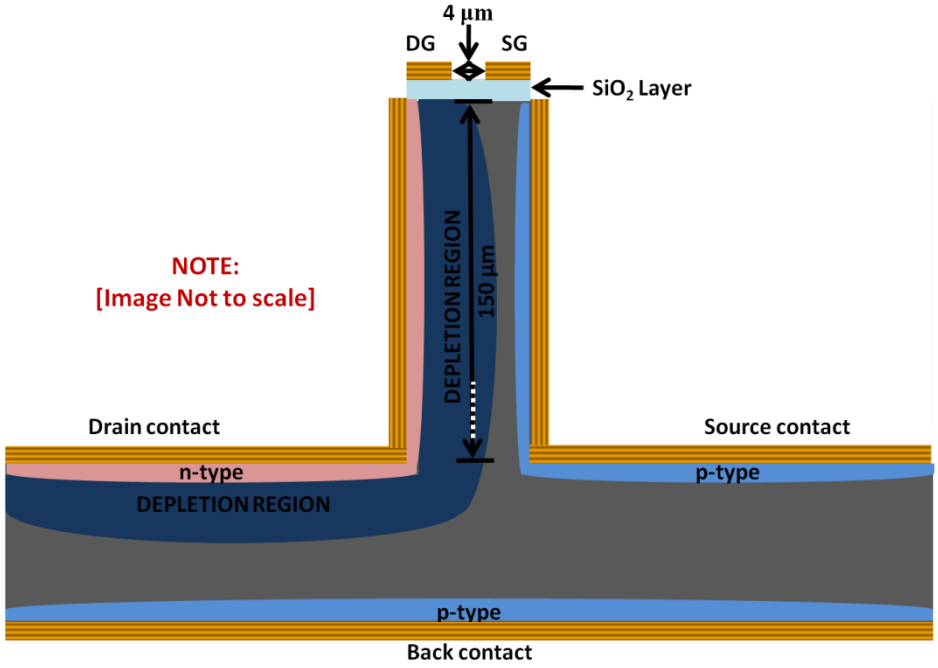

Figure 8.5: MESA lateral p-i-n photodiode for wide range wavelength detection (400 – 950 nm)

This structure, as a standalone single device, can work for detecting visible to near-infrared radiations with similar quantum efficiency values. However, if a two dimensional (2D) array of this mesa structure is made as shown in Figure 8.3 this might show some interesting features for night vision and machine vision applications as discussed earlier [3].

Another device with similar top structure of mesa silicon p-i-n photodetector is proposed with an addition of dual back gates as shown in Figure 8.6. It can be particularly useful for detecting long wavelength radiations i.e. red to near-infrared regions. Due to the presence of surface depletion region and lateral doping structure, this device can still be used for short wavelength near-UV and blue radiations. As both ends of the proposed device have similar structure, therefore front and back illumination methods can be used for detecting infrared radiations. However, it should be noted that if the device is illuminated through the top, the back gates when biased might influence the device response in the near-infrared region. The device will show a different response in the proposed configuration as shown in Figure 8.6 to the device shown in Figure 8.7 where the top and bottom contacts are diffused from the sides so that the top and bottom contacts appear as a single contact. The latter device can only be used as a standalone device.

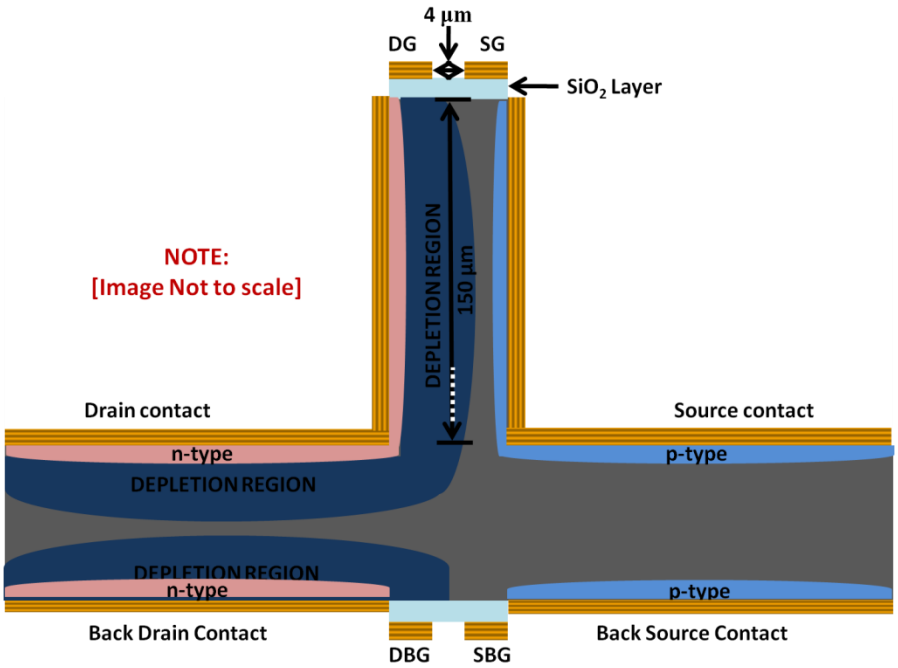

Figure 8.6: MESA structure with front and back dual gates

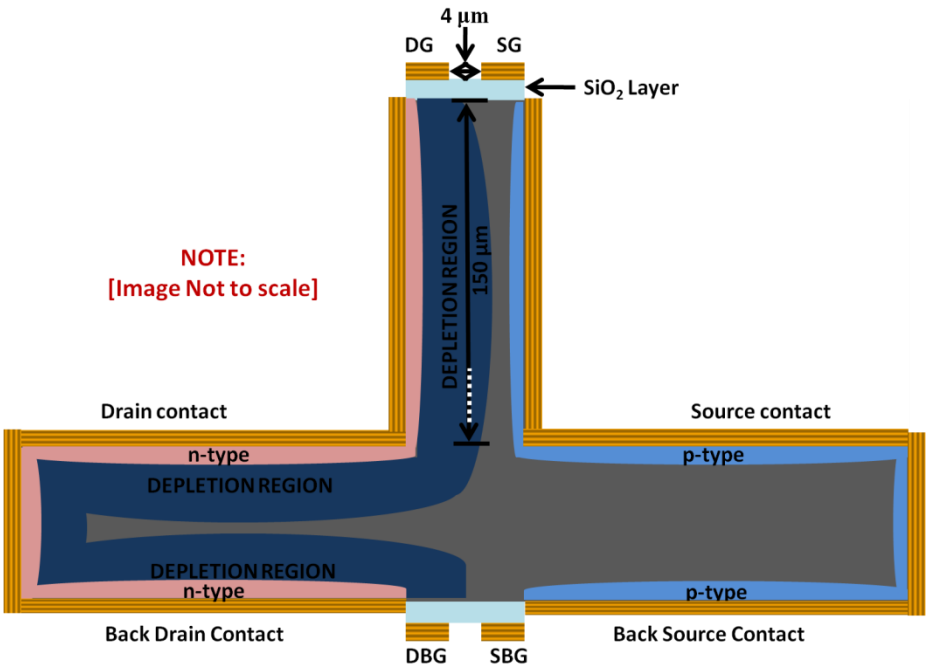

Figure 8.7: MESA structure with front and back dual gates with merged source contacts and drain contacts

8.2.4. Interdigitated Structure for Illumination Positioning

Finally an interdigitated lateral p-i-n structure as shown in Figure 8.8 is proposed. This device employs two gates overlapping the n and p doped drain and source finger regions. The device, if fabricated on SOI material, might demonstrate a lower dark current, higher responsivity and a better bandwidth response. The dimensions of the fingers and the spacing in between can be varied to control the device response.

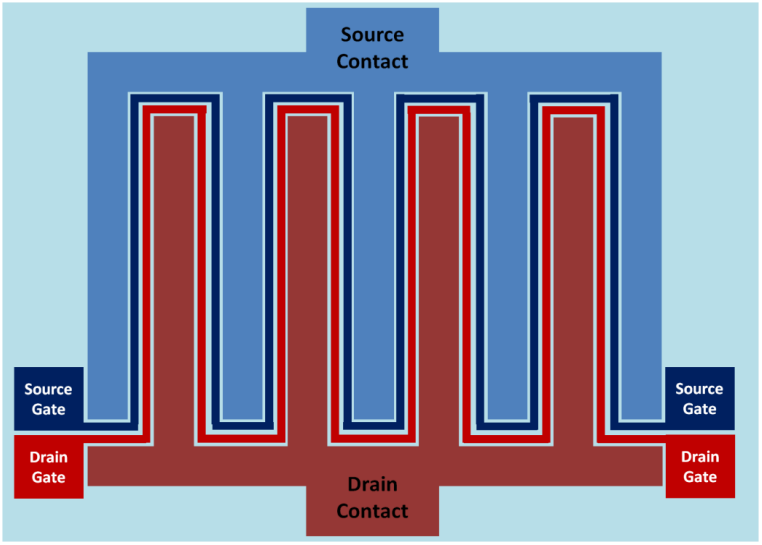

Figure 8.8: Interdigitated lateral p-i-n photodiode

8.3. References

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Appendix – 1 Fabrication Process Sheet

Sr. No	Process	Details	Conditions
1	Clean the substrate	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
2	Spin primer	Hexamethyldisilazane (HMDS)	4000 RPM for 5 seconds
3	Spin resist	S1818	4000 RPM for 30 seconds
4	Bake	Hotplate	15 min at 90 degree
5	Photolithography exposure	Photolithography markers & Device Isolation Pattern (Pattern 1)	4.5 Seconds - Hard Contact
6	Development	In 1:1 ratio of Microposit Developer and RO Water freshly made solution	75 Seconds in 1:1 solution & 75 seconds in RO Water
7	Blow dry	with nitrogen blow	
MOUNTING OF SAMPLES ON SILICON WAFER FOR DRY ETCH			
8	Dry etch	RYT1 (Recepie) 10 micron deep	12.5 minutes
9	Clean the substrate (post dry etch) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
10	SiO_2 Growth using (Oxidation furnace)	Growth rate is 100 nm per hour for thicker oxidations. Oxygen gas flow at 6 cm^3/min (ATP).	250 nm in 180 minutes [Put test sample for oxide exact etch time calculation]
11	Clean the substrate (post oxidation) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
12	Spin primer	Hexamethyldisilazane (HMDS)	4000 RPM for 5 seconds
13	Spin resist	S1818	4000 RPM for 30 seconds

Sr. No	Process	Details	Conditions
14	Bake	Hotplate	15 min at 90 degree
15	Photolithography exposure	Expose Source window (500 x 500) micron. Allignment to be made with markers on the mask to the etched photolithography markers on the substrate (Pattern 2)	4.5 Seconds - Hard Contact
16	Development	In 1:1 ratio of Microposit Developer and RO Water freshly made solution	75 Seconds in 1:1 solution & 75 seconds in RO Water
17	Blow dry	with nitrogen blow	
18	Bake (Post Development)	Hotplate	5 minutes at 90 degree
19	HF etching	1:5 ratio solution of HF. 100 nm per minute etch rate	2.5 minutes (First check the exact oxide growth with test sample oxidized in the same environment)
20	Clean the substrate (post etching) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
21	Check the Oxide growth	Using Dektek	using test sample
22	Spin-on-glass for boron diffusion	Borosilica glass	2000 RPM for 20 seconds
23	Bake	Hotplate	15 minutes at 90 degree
24	Thermal Diffusion (Boron Diffusion Furnace)	Nitrogen + 5 % oxygen gas to flow at 6 cm3/min (ATP).	at 1135 degree for 20 minutes
25	HF Cleaning	40 % HF concentrated solution	Approximately 3 minutes to clear off all the silica layer

Sr. No	**Process**	**Details**	**Conditions**
26	Clean the substrate (post HF 40 % etching) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
27	SiO_2 Growth using (Oxidation furnace)	Growth rate is 100 nm per hour for thicker oxidations. Oxygen gas flow at 6 cm^3/min (ATP).	250 nm in 180 minutes [Put test sample for oxide exact etch time calculation]
28	Clean the substrate (post oxidation) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
29	Spin primer	Hexamethyldisilazane (HMDS)	4000 RPM for 5 seconds
30	Spin resist	S1818	4000 RPM for 30 seconds
31	Bake	Hotplate	15 min at 90 degree
32	Photolithography exposure	Expose Drain window (500 x 500) micron. Allignment to be made with markers on the mask to the etched photolithography markers on the substrate (Pattern 3)	4.5 Seconds - Hard Contact
33	Development	In 1:1 ratio of Microposit Developer and RO Water freshly made solution	75 Seconds in 1:1 solution & 75 seconds in RO Water
34	Blow dry	with nitrogen blow	
35	Bake (Post Development)	Hotplate	5 minutes at 90 degree
36	HF etching	1:5 ratio solution of HF. 100 nm per minute etch rate	2.5 minutes (exact etch time as calculated at step 19)
37	Clean the substrate (post etching) &	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub

Sr. No	Process	Details	Conditions
	blow dry		
38	Check the Oxide growth	Using Dektek	using test sample
39	Spin-on-glass for phosphorous diffusion	Phosphorosilica glass	2000 RPM for 20 seconds
40	Bake	Hotplate	15 minutes at 90 degree
41	Thermal Diffusion (Phosphorous Diffusion Furnace)	Nitrogen + 5 % oxygen gas to flow at 6 cm3/min (ATP).	at 1135 degree for 20 minutes
42	HF Cleaning	40 % HF concentrated solution	Approximately 3 minutes to clear off all the silica layer
43	Clean the substrate (post HF 40 % etching) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
44	SiO_2 Growth using (Oxidation furnace)	Growth rate is 100 nm per hour for thicker oxidations. Oxygen gas flow at 6 cm^3/min (ATP).	50 nm in 18 minutes (for thin oxidation the growth time is relatively less) [Put test sample for oxide exact etch time calculation]
45	Clean the substrate (post oxidation) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
46	Spin primer	Hexamethyldisilazane (HMDS)	4000 RPM for 5 seconds
47	Spin resist	S1818	4000 RPM for 30 seconds
48	Bake	Hotplate	15 min at 90 degree

Sr. No	**Process**	**Details**	**Conditions**
49 (a)	Photolithography exposure [for both single gate, normal dual gate and for grating-based devices]	Expose Source & Drain window (500 x 500) micron. Allignment to be made with markers on the mask to the etched photolithography markers on the substrate (Pattern 4)	4.5 Seconds - Hard Contact
49 (b)	Photolithography exposure [for overlapping dual gate devices]	Expose Source & Drain window (490 x 490) micron. Allignment to be made with markers on the mask to the etched photolithography markers on the substrate (Pattern 5)	4.5 Seconds - Hard Contact
50	Development	In 1:1 ratio of Microposit Developer and RO Water freshly made solution	75 Seconds in 1:1 solution & 75 seconds in RO Water
51	Blow dry	with nitrogen blow	
52	Bake (Post Development)	Hotplate	5 minutes at 90 degree
53	HF etching	1:5 ratio solution of HF. 100 nm per minute etch rate	30 seconds (First check the exact oxide growth with test sample oxidized in the same environment i.e. step 44) then etch the actual samples.
54	Cleaning	In normal RO water & blow dry.	Note: do not clear the resist.
55	Metallization (front patterned Source & Drain windows)	Ti (33 nm), Pt (33 nm) & Au (240 nm)	Plassys II. (An electron-beam evaporator for metallization). Put acetone

Sr. No	Process	Details	Conditions
			in a beaker in parallel and place in hot tub for hot acetone available to lift-off after metallization)
56	Lift-off	Put the sample in 50 degree tub in acetone beaker	Approximately for 15 to 20 minutes for good lift-off.
57	Clean the substrate (post lift-ff) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
58	Metallization (backside)	Ti (33 nm), Pt (33 nm) & Au (240 nm)	Plassys II
59	Annealing (front side)	RTA	Use recipe CDF-360
60	Annealing (back side)	RTA	Use recipe CDF-360
61	Clean the substrate (post annealing) & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
62	Spin primer	Hexamethyldisilazane (HMDS)	4000 RPM for 5 seconds
63	spin resist	S1818	4000 RPM for 30 seconds
64	Bake	Hotplate	15 min at 90 degree
65	Soaking	Clorobenzene	10 minutes & simply blow dry
66	Bake	Oven	15 min at 90 degree
67 (a)	Photolithography exposure for Single Centre Gate structure	Expose (Pattern 6)	5.5 Seconds - Hard Contact

Sr. No	**Process**	**Details**	**Conditions**
67 (b)	Photolithography exposure for Single Offset Gate structure	Expose (Pattern 7)	5.5 Seconds - Hard Contact
67 (c)	Photolithography exposure for Normal Dual Gate structure	Expose (Pattern 8)	5.5 Seconds - Hard Contact
67 (d)	Photolithography exposure for Overlapping Double Gate structure [only for samples processed using pattern 5 at step 49 (b)]	Expose (Pattern 9)	5.5 Seconds - Hard Contact
68	Development	In 1:1 ratio of Microposit Developer and RO Water freshly made solution	75 Seconds in 1:1 solution & 75 seconds in RO Water
69	Blow dry	with nitrogen blow	
70	Metallization	Ti (33 nm), Pt (33 nm) & Au (240 nm)	Plassys II Put acetone in a beaker in parallel and place in hot tub for hot acetone available to lift-off after metallization)
71	Lift-off	Put the sample in 50 degree tub in acetone beaker	Approximately for 15 to 20 minutes for good lift-off.
72	Blow dry	with nitrogen blow	
73	Testing	Using SPA current-voltage characteristics	
74	Cleaving	Using cleaver	

Sr. No	**Process**	**Details**	**Conditions**
75	Mounting of cleaved devices on ceramic chip carrier	Mounting with silver paint or silver epoxy	
76	Wire Bonding	Using wire bonder (gold or aluminium wires)	
77	Testing	Using specialized setup with bonding device fitted in and connected to SPA	
ELECTRON BEAM LITHOGRAPHY JOBS FOR GRATING PATTERN OR IN SOME CASES FOR GATE STRUCTURE			
78	Clean the substrate & blow dry	Acetone, Methanol & RO water	5 minutes each in ultrasonic tub
79	Spin primer	Hexamethyldisilazane (HMDS)	4000 RPM for 5 seconds
80	Spin resist	S1818	4000 RPM for 30 seconds
81	Bake	Hotplate	15 min at 90 degree
82	Soaking	Clorobenzene	10 minutes & simply blow dry
83	Bake	Oven	15 min at 90 degree
84	Photolithography exposure	Expose Photolithography & electron beam lithography markers (Pattern 10)	5.5 Seconds - Hard Contact
85	Development	In 1:1 ratio of Microposit Developer and RO Water freshly made solution	75 Seconds in 1:1 solution & 75 seconds in RO Water
86	Blow dry	with nitrogen blow	
87	Metallization	Ti (33 nm) & Au (100 nm)	Plassys II Put acetone in a beaker in parallel and place in hot tub for hot acetone available to lift-off after metallization)

Sr. No	Process	Details	Conditions
88	Lift-off	Put the sample in 50 degree tub in acetone beaker	Approximately for 15 to 20 minutes for good lift-off.
89	Blow dry	with nitrogen blow	
90	Electron beam resist spin	PMMA 2010 15 %	5000 RPM for 60 seconds
91	Bake	Oven	30 min 180 degree
92	Electron beam resist spin	PMMA 2041 4 %	5000 RPM for 60 seconds
93	Bake	Oven	90 min 180 degree
94	Submit e-beam Job	1 micron gratings structure OR gate structure if needed	
95	Development		
	95 (a)	MIBK:IPA 1:1 solution	60 seconds 23 degree temperature
	95 (b)	RO Water	60 seconds
	95 (c)	IPA	60 seconds
	95 (d)	RO Water	60 seconds
96	Blow dry	with nitrogen blow	
97	Metallization	Al (50 & 150 nm) for grating structure OR Ti (33 nm), Pt (33 nm) & Au (240 nm) for gate structures	Plassys II Put acetone in a beaker in parallel and place in hot tub for hot acetone available to lift-off after metallization)
98	Lift-off	Put the sample in 50 degree tub in acetone beaker	Approximately for 15 to 20 minutes for good lift-off.
99	Blow dry	with nitrogen blow	
100	Follow steps 73-77		