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Impact of Atomistic Device Variability on Analogue Circuit Design

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**Submitted in fulfilment of the requirements to award
the degree of Doctor of Philosophy
in Electronics and Electrical Engineering**

School of Engineering

University of Glasgow

For Lingting and My Parents

Abstract

Scaling of complementary metal-oxide-semiconductor (CMOS) technology has benefited the semiconductor industry for almost half a century. For CMOS devices with a physical gate-length in the sub-100 nm range, extreme device variability is introduced and has become a major stumbling block for next generation analogue circuit design. Both opportunities and challenges have therefore confronted analogue circuit designers. Small geometry device can enable high-speed analogue circuit designs, such as data conversion interfaces that can work in the radio frequency range. These designs can be co-integrated with digital systems to achieve low cost, high-performance, single-chip solutions that could only be achieved using multi-chip solutions in the past. However, analogue circuit designs are extremely vulnerable to device mismatch, since a large number of symmetric transistor pairs and circuit cells are required. The increase in device variability from sub-100 nm processes has therefore significantly reduced the production yield of the conventional designs.

Mismatch models have been developed to analytically evaluate the magnitude of random variations. Based on measurements from custom designed test structures, the statistics of process variation can be estimated using design related parameters. However, existing models can no longer accurately estimate the magnitude of mismatch for sub-100 nm “atomistic” devices, since short-channel effects have become important. In this thesis, a new mismatch model for small geometry devices will be proposed to address this problem.

Based on knowledge of the matching performance obtained from the mismatch model, design solutions are desired at different design levels for a variety of circuit topologies. In this thesis, transistor level compensation solutions have been investigated and closed-loop compensation circuits have been proposed. At circuit level, a latch-based comparator has been used to develop a compensation solution because this type of comparator is extremely sensitive to the device mismatch. These comparators are also used as the fundamental building block for the analogue-to-digital converters (ADC). The proposed comparator compensation scheme is used to improve the performance of a high-speed flash ADC.

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Publications

Conference Papers:

- [1] **F. Hong**, B. Cheng and D. Cumming, "Mismatch Modelling for a 35 nm Differential Amplifier with Impact of Variability", IEEE Proc. ULIS 2010, March. Glasgow, U.K. pp. 161-164
- [2] **F. Hong**, D. Cumming, "Source Compensation Scheme for Reducing Impact of Variability on Differential Amplifier in 35 nm CMOS", IEEE Proc. ICECS Dec. 2010, Athens, Greece, pp. 344-347
- [3] **F. Hong**, B. Cheng, S. Roy and D. Cumming, "An Analytical Mismatch Model for NanoCMOS Device Under the Impact of Intrinsic Device Variability", IEEE ISCAS May 2011, Brazil, pp. 2257-2260.
- [4] S. Saha, J. Grant, Y. Ma, A. Kalid, **F. Hong** and D. Cumming, "Terahertz Frequency Domain Spectroscopy for Polar Alcohol", Proc. IEEE IRMMW-THz, Oct. 2011, Houston Texas, U.S.
- [5] S. Saha, J. Grant, Y. Ma, A. Kalid, **F. Hong** and D. Cumming, "Frequency Domain Spectroscopy of DNA at Terahertz Frequency", Proceeding of Bioengineering, Sept. 2011, London, U.K.

Journal Papers:

- [1] **F. Hong** and D. Cumming "A Novel Offset Compensation Scheme for Latch-type Comparator in 35 nm CMOS", IET Letter 2011 (Submitted)
- [2] S. Saha, J. Grant, Y. Ma, A. Kalid, **F. Hong** and D. Cumming, "Method for Vector Characterisation of Polar Liquids Using Frequency-Domain Spectroscopy", Journal of Optics Letter, Vol. 36, Iss. 17, pp. 3329-3331, 2011
- [3] S. Saha, J. Grant, Y. Ma, A. Kalid, **F. Hong** and D. Cumming, "Terahertz Frequency-domain Spectroscopy Method for Vector Characterization of Liquid Using an Artificial Dielectric", IEEE Trans. of Terahertz Science and Technology. (Accepted)

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Glossary of Symbols

Symbols

L	Gate Length
W	Gate Width
V_{GS}	Gate-Source Voltage
V_{DS}	Drain-Source Voltage
V_{BS}	Bulk-Source Voltage
V_S	Source Voltage
V_{TH}	Threshold Voltage
I_{DS}	Drain-Source Current
β	Current Factor
γ	Body Effect Coefficient
λ	Channel Length Modulation Coefficient
θ	Mobility Degradation Factor
Φ_F	Fermi Level Potential
v_{sat}	Saturated Velocity
E_C	Critical Field Strength
μ	Carrier Mobility
C_{OX}	Gate Oxide Capacitance per Unit Area
g_m	Transistor Transconductance
ρ	Sheet Resistivity
r_0	Output Resistance

Acronyms

CMOS	Complementary Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
UDSM	Ultra-deep Submicron

RDD	Random Discrete Dopant
LER	Length Edge Roughness
PGG	Poly-Gate Granularity
OTF	Oxide Thickness Fluctuation
ADC	Analogue-to-Digital Converter
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductor
SOI	Silicon On Isolator
IPF	Intrinsic Parameter Fluctuation
DUT	Device Under Test
IEEE	Institute of Electrical and Electronics Engineers
ICMTS	International Conference on Microelectronics Test Structure
DAC	Digital-to-Analogue Converter
INL	Integral Nonlinearity
DNL	Differential Nonlinearity
LSB	Least Significant Bit
UV	Ultraviolet
RBB	Reverse Body Biasing
FBB	Forward Body Biasing
ABB	Adaptive Body Biasing
III-V	A group of materials which are compounds of elements in columns 13 to 15 of the periodic table, e.g. GaAs
BSIM	Berkeley Short-channel IGFET Model
DNL	Differential Nonlinearity
INL	Integral Nonlinearity
DFT	Discrete Fourier Transform
FFT	Fast Fourier Transform
SNR	Signal to Noise Ratio
SINAD	Signal to Noise and Distortion Ratio
THD	Total Harmonic Distortion
SFDR	Spur Free Dynamic Range
ENOB	Effective Number of Bits
LNA	Low-Noise Amplifier
OTA	Operational Transconductance Amplifier

Chapter 1 Introduction

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1.1 Motivation

The aggressive dimension scaling of complementary metal-oxide-semiconductor (CMOS) device has benefited the industry for over half a century. The trend in the growth of the number of transistors that can be inexpensively integrated on a chip was first concluded by Gordon Moore in 1965. Since then, this self-fulfilling prophecy has guided both industry and academics to research and develop new technology innovations. From analogue circuit design point of view, the scaling of the CMOS transistor can enable high-speed circuit designs that operate in the radio frequency range. Such designs could only be implemented using different processes and materials in the past, for example BiCMOS, InP and GaAs. It is desirable to cheaply integrate the high-speed amplifiers and data converters on the same chip with other digital systems for high-speed applications, such as software design radio, broadband data wired & wireless communication systems and data storage read channels. However, since the Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have reached the ultra-deep submicron (UDSM) regime where the gate-length (L_{GATE}) is smaller than 100 nm, the extreme statistical variability has become a great challenge for next generation circuit design and fabrication. As the size of the device has reached the limit of achievable manufacturing accuracy, the discreteness of charge and matter has introduced a significant variation in device electrical performances between nominally identical CMOS transistors. A significant mismatch problem has been introduced to analogue circuit design. Furthermore, the scaled supply voltage and increased oxide aging mechanisms have posed more challenges during the design practice.

Analogue circuit design is extremely vulnerable to device variability as large number of symmetric circuit topologies are used, such as differential pairs and current mirrors. The conventional approach to cope with the mismatch problem is to aggressively increase the sizes of the transistor, limited by the design constraints of the silicon area and power. However, this approach must be carefully applied when using UDSM devices. This is because the increased gate-length (L) will reduce the unity gain frequency range of the transistor and slow down the speed of the whole circuit. The drain current will be increased if one widens the gate width (W). As the UDSM devices have an ever smaller resistance, the increased drain current dramatically consumes more power at a given supply voltage.

A variety of analytical mismatch models have been developed to evaluate the impact of process variations on the electrical performances of devices and circuits. Based on the statistical information of the threshold voltage and the current factor, the voltage and current differences between nominally identical transistors can be mathematical modelled. Eventually, the yield of a circuit can be estimated as a function of transistor dimensions without committing the circuit to fabrication. This mismatch estimation is extremely important as new IC products reach the market after few or no prototype stages. Once the chips are fabricated, they cannot be readily modified. In the UDSM regime, the existing mismatch models become less accurate as short-channel effects have begun to dominate the electrical performance of the device. Since the existing methods have become inadequate to provide accurate estimation of mismatch for the most recent technologies, it is necessary to develop new mismatch models for the use of nanoCMOS transistors.

The mismatch problem is not new for analogue circuit design. Existing compensation technologies have been developed to overcome this imperfection. At transistor level, floating-gate and body-biasing are widely used in different applications. At circuit level, a variety of compensation techniques have been developed at a large supply voltage. However, these existing solutions are not necessarily applicable for the UDSM designs. Improved or new solutions need to be found in order to cope with the new device and design constraints.

In this thesis, the challenges mentioned above have been investigated. A novel mismatch model for UDSM devices, with major short-channel effects taken into consideration, is proposed. The design solutions to overcome the impact of device variability have been developed at transistor level and circuit level. Furthermore, it will be demonstrated that these compensation solutions can be easily migrated with system level designs. The

simulations carried out in this research are based on the 35 nm gate-length BSIM4 model library developed by the device-modelling group at the University of Glasgow. The models meet the International Technology Roadmap for Semiconductor (ITRS) requirements for the 45 nm technology node. Each model represents a transistor with a nominally identical macroscopic device design, but with different atomic configurations of random discrete dopant (RDD), length edge roughness (LER) and poly-gate granularity (PGG).

1.2 Aims and Objectives

The aims of this research are: (a) to analytically evaluate the impact of device variability on analogue circuit design when process variation information is available; and (b) to develop new robust circuits at different design levels using UDSM devices with a low power supply voltage. The topics that will be discussed in this thesis are:

- To develop a new mismatch model for the UDSM devices with major short-channel effects taken into account.
- To analytically investigate the potential compensation principles at transistor level, and to implement and verify the principles with applicable compensation circuits using 35 nm CMOS.
- To investigate and implement an applicable compensation scheme for a high-speed latch-based comparator with low supply voltage taken into consideration.
- To develop a new high-speed analogue-to-digital converter (ADC) that is suitable for radio and communication application with the impact of device variability.

1.3 Thesis Outline

The remainder of this thesis is organised as follows. Chapter 2 reviews the main origins of the device variability. The causes of systematic variations and random variations are traced back to their fabrication and physical origins. The major sources of random variations are introduced, including RDD, LER and PGG. The typical test structures that are used to extract the variation information are illustrated. Based on the extracted fabrication process statistics, existing mismatch models are reviewed. How to apply these models in real design practice in order to evaluate the circuit matching performance and yield are demonstrated. Furthermore, with the impact of inevitable device variability, the merits and drawbacks of the popular existing compensation design solutions are discussed.

Chapter 3 focuses on developing a new analytical mismatch model for UDSM devices. The simulation methodology used in the rest of this thesis is also presented. Major short-channel effects, including velocity saturation and mobility degradation are taken into account in the proposed model. Statistical information of the process is extracted using the 35 nm BSIM4 models. The existing long-channel mismatch model is also applied as a comparison. A case study of how to apply the proposed short-channel mismatch model in evaluating a differential amplifier is illustrated.

In Chapters 4, 5 and 6, the compensation solutions have been investigated and developed from transistor level to circuit level. High-speed robust designs have been achieved. It is further demonstrated that the performance of the compensation solutions are superior than that would be achieved by simply increasing the transistor size.

In Chapter 4, basic ideas of using each individual terminal of a MOSFET to overcome the device mismatch have been reviewed. The current-voltage relationship at each terminal is mathematically modelled. Three novel compensation schemes have been proposed, including body-biasing compensation, drain compensation and source compensation.

A novel high-speed latch-based comparator has been proposed in Chapter 5. Low power consumption and low supply voltage are the two major design targets to meet, whilst maintaining the speed of the comparator. Performance improvements have been achieved over the existing designs in the literature. Furthermore, taking the impact of device variability into account, a custom designed compensation scheme is added to improve the offset voltage without compromising the speed performance.

Based on the high-speed comparator proposed in Chapter 5, a 3-bit 10 GHz flash ADCs is proposed in Chapter 6. The performance of this ADC is further improved by using the compensation scheme for the comparators. The static and dynamic characteristics of the ADC are estimated. Monte Carlo simulations are carried out before and after the compensation scheme is applied to the ADC. In the end, it is proved that applicable high-speed flash ADC using for radio frequency range applications can be designed in the presence of extreme statistical variability using 35 nm CMOS.

The final chapter, Chapter 7, summarises the conclusions from the previous chapters. Opportunities for future work are also discussed.

Chapter 2 Literature Review

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2.1 Introduction

Since the invention of the integrated circuit (IC) in 1950s, the famous Moore's law has been credited as an unshakeable example of a self-fulfilling prophecy and technological trajectory in both academic and popular press [1]. It has been regarded as one of the few stable rules on which manufacturers could rely in a constantly changing environment. Although it was revised for three times, Moore's theory successfully predicted the trend of IC complexity over the past five decades [1-3]. Moreover, since 1993 a group of semiconductor industry experts from the US, Europe, Japan, Korea and Taiwan have begun to evaluate and report detailed parameters and technology innovations necessary to continue the Moore's law. Their annual report, known as the International Technology Roadmap for Semiconductor (ITRS), has become a widely acknowledged guideline for both designers and manufacturers in the IC industry [4]. In 2010's update report, ITRS predicted that the last generation of applicable bulk MOSFETs would have a physical gate length of 17 nm in 2015. After that, new alternative architectures, materials and technologies, such as the multi-gate device [5], fin-FET [6], III-V materials [7] and silicon-on-insulator (SOI) [8], would be introduced to take over the conventional silicon bulk MOSFETs. For the meantime, bulk MOSFETs would still be the main workhorse for the industry. The cutting edge technology that is in mass production nowadays is the 32 nm technology process developed by Intel [9]. However, Intel cannot wait until 2015 and has announced its 22 nm 3D gate fin-FET structure this May [10].

Since the aggressive scaling of MOSFETs have reached the UDSM regime, regardless of the unavoidable systematic variations, the device statistical variability introduced by the intrinsic parameter fluctuations (IPF) has become one of the major stumbling blocks for both manufacturers and circuit designers. For example, Intel has reported a lot of fabrication difficulties as the devices have scaled to less than 100 nm [11-13]. The dominant sources of IPF are random discrete dopants [14], line edge roughness [15], oxide-thickness variations [16] and poly-gate granularity [17]. All these sources will be discussed in detail in the Section 2.2. It is also interesting to mention that these uncertainties have existed for a long time [18] and cannot be eliminated by tightening the process control. Traditionally, continuous approximation of the device structure was reasonably applied, as the fabricated dimensions of MOSFETs were much larger than the scale of these uncertainties. As scaling progressed, these fabrication uncertainties have not shrunk simultaneously and have already reached the same scale as the devices themselves

that makes the approximation of the continuous device structure invalid [19]. These macroscopically identical atomistic devices are now microscopically different, as they significantly manifest their discrete nature at such scale. Furthermore, the electrical parameters of these nominally identical devices in transistor pairs exhibit significant mismatch. In the context of circuit design, the device electrical property mismatch has been translated into significant performance degradation for both analogue and digital circuits among all different design hierarchies. For digital circuit designs, the variability reduces the timing and power performances of different paths and blocks in the circuits [20]. For analogue circuit designs, well-matched transistor pairs, such as current mirror or differential amplifier, are required as the fundamental circuit building blocks over a wide range of applications. The drain current variations and input referred offset voltages are introduced due to the mismatch between these nominally identical pairs. The offset voltage would be further interpreted into a variety of performance degradations for analogue circuits, such as operational amplifiers [21], comparators [22, 23], ring oscillators [24], phase-lock loops [25] and data converters [26, 27]. Eventually, yields of such circuits would dramatically drop increasing the fabrication cost per chip.

Detailed research and investigations have been carried out in order to understand the mismatch problem [28-36]. Manufacturers and foundries have already developed a variety of test structures for the evaluation of both systematic and random variations [37-40]. The principle of the evaluation is to obtain the stochastic information of the drain currents (I_{DS}) from a large sample of devices under test (DUT) by sweeping the gate-source voltage (V_{GS}) at a low drain-source voltage (V_{DS}). The mean values of I_{DS} measured from different dies and wafers represent the systematic variation that is normally treated as a predictable parameter as a function of process and spatial information [41]. The random process uncertainties are reflected by the spread of the drain current distribution that are further interpreted using the mean and the variance of current factor (β) and threshold voltage (V_{TH}) variations [30]. Different analytical mismatch models have been developed using the statistics of β and V_{TH} , from various perspectives in order to accurately describe the phenomena and provide a deep insight into the origins of the random uncertainty [42, 43].

In order to overcome the impact of variability, a number of design solutions have been reported [44-46]. At transistor level, researchers and design engineers have developed the floating-gate transistor [47] and the body-biasing technique to compensate transistor level mismatch [48]. At circuit level, auto-zeroing, correlated double sampling and chopper stabilization [45] have been reported and become the main stream for the discrete and

continuous applications using long-channel devices. In this chapter, the primary origins of device variability are described. These origins can be catalogued into systematic variation and random variation. Two types of test structures are introduced for the characterisation of the systematic and random variations, respectively. Existing analytical mismatch models for long-channel device will be reviewed as well. These models are used to estimate the circuit electrical matching performance based on the extracted statistical information of I_{DS} that are used to represent the process variations. In the end, existing variability-aware design techniques will be discussed.

2.2 Origins of Variability

The variations that can significantly degrade the performances of the CMOS circuit can be catalogued into two types of factors: environmental variations and physical variations[49]. Environment introduced variability is mainly derived from the power supply nets, temperature and noise during the operation of the circuits. Detailed research and investigations of these interferences have been achieved over past couple of decades [50, 51]. Noise that corrupts an IC can be summarised into two kinds: thermal noise and flicker noise. The main origin of the thermal noise is the random motion of electrons in a conductor that results a voltage measure fluctuation across the conductor with a zero averaged current. Its power spectrum density (PSD) is proportionally related to the absolute temperature. Therefore, it is called thermal noise. Flicker noise is another important noise source. It is introduced by some randomly trapped and later released carriers in the channel, due to the “dangling” bonds sandwiched between the channel and the dielectric [52, 53]. Its PSD is inverse-proportional to the operation frequency, as the trap and release phenomenon is more likely to occur at low frequency. Therefore, it is also known as 1/f noise. Many circuit-level solutions have been developed to cancel or reshape the noise power spectrum density, for example auto-zeroing, correlated double sampling and chopper stabilization [45, 51]. These techniques will be introduced in detail in Section 2.4. To overcome other environmental factors introduced variations, the band gap reference has been developed to provide an accurate voltage reference that is immune to the temperature change [54]. Differential pairs are widely used at the circuit input stage to reject the supply voltage turbulence or any other common-mode fluctuations. Despite their significance, these environment factors were not the primary focus of this research and will not be discussed in this thesis.

On the other hand, the physical factors are mainly caused by the limitations of fabrication procedures, including mask imperfection [55], lithography distortion [56] and intrinsic parameter fluctuations [19]. Unfortunately, these process induced variations increase with technology scaling, as the fabrication tolerance margins cannot be scaled simultaneously. The magnitudes of device mismatch are now approaching the actual device dimensions. In order to obtain the knowledge of these variations, custom designed test structures can be embedded at different locations on a wafer to retrieve the statistical information of these variations. The measurements of these test structures can reveal the nature (systematic or random), magnitude and scale (intra die, inter die or inter wafer) of the sources of variations. Systematic variations normally have a strong correlation with (a) process temperature, (b) layout position and (c) layout topology style [57]. Therefore, design solutions and fabrication solutions of eliminating systematic variation can be developed based on the knowledge of these correlations. However, some of the variations have a random nature among all the devices. They can be only described by their statistical distributions, and are therefore called random variations. Moreover, it is impossible for foundries and manufacturers to eliminate the random variations.

2.2.1 Systematic Variations

On a single piece of wafer, systematic variations are normally classified as the across-field or the layout dependent variations [58]. The across-field systematic variation could be caused by photolithographic and etching sources, such as mask errors [55], lens aberrations [56], exposure variations [59] and variations in etch loading [60]. As a consequence, the characteristics of devices have a strong correlation with their relevant positions regarding to the reticle. For example, the on-current and oxide thickness gradually change from the centre to the edge on a wafer [61]. Based on the above observations, it is relatively easy to model the across-field systematic variation as a function of positions in reticle using the embedded test structures.

However, the layout dependent variation, which causes two different layouts of the same device behaving differently, is normally predictable and can be expressed using the information of the layout structure and surrounding topologies [58]. For example, the differences in orientations and shapes of poly silicon gates, or the positioning and spacing of the contact pads between the poly and diffusion (active) regions can all cause variations in device characteristics. It was demonstrated in [62] that a central symmetric layout has a better matching performance than an interleaved finger symmetric layout. Furthermore,

well proximity effect is another important source of device threshold voltage variation due to the layout [63]. During deep well implants, the dopant ions can scatter out of the well masking photoresist and increase the dose in the devices that are close to the well edge, which will result in well layout dependent threshold voltage variations between the devices [61]. Stress can also lead to layout dependent variation due to the introduction of uniaxial stress in channel areas for carrier mobility enhancement via dual stress liners [64] and e-SiGe [65]. Therefore, if layout topologies are carefully designed, the layout dependent variation can be significantly reduced. It should further be noted that the fabrication conditions are not constant among wafers, lots and factories. These condition changes lead to a global systematic variation for each wafer as well. However, compared with random variations, systematic variations are relatively easier to be modelled and engineered out at a low cost.

2.2.2 Random Variations

Process uncertainties introduced by random variations normally cause a much more significant mismatch between two nominally identical devices compared with systematic variations. Besides their nature of unpredictability, random variations have become dramatically worse when the scaling of CMOS transistors gets to lower than 100 nm. The discreteness of charge and matter of a CMOS transistor at this scale introduces intrinsic parameter fluctuations, which accounts for over 50 % of the total variability in the current 45 nm technology node [66, 67]. It has been widely regarded as one of the major factors limiting the operational precision of the integrated circuit design in the nanometre regime. The conventional concepts and understandings of smooth boundaries and continuous ionized dopant charge are no longer appropriate. The dominant sources of IPF are random discrete dopants [14], line edge roughness [15], oxide thickness fluctuations [68] and poly silicon gate granularity [69].

2.2.2.1 Random Discrete Dopants

As the number of dopants in the active region of an atomistic device has reduced to a relatively small amount, the variation in dopant numbers between devices follows a Poisson distribution [70]. The device's behaviour is predominated by the number and position pattern of the dopant atoms. Compared with a conventional long-channel device, the doping concentration of these atomistic devices cannot be assumed as statistically averaged. The potential profiles of a continuously doped and an atomistic device are

plotted in Figure 2.1 to present the inhomogeneity. Due to the doping profile variations, certain parts of the device will be turned on earlier than other parts, which will decrease the average threshold voltages of atomistic devices compared with a continuously doped device [71, 72]. It is also observed that the threshold voltage has a stronger correlation with the dopants that are closer to the dielectric [73]. A typical atomistic simulation domain and dopant distributions is shown in Figure 2.2 (a). The potential distribution at threshold voltage due to the positions of discrete dopants is plotted in Figure 2.2 (b).

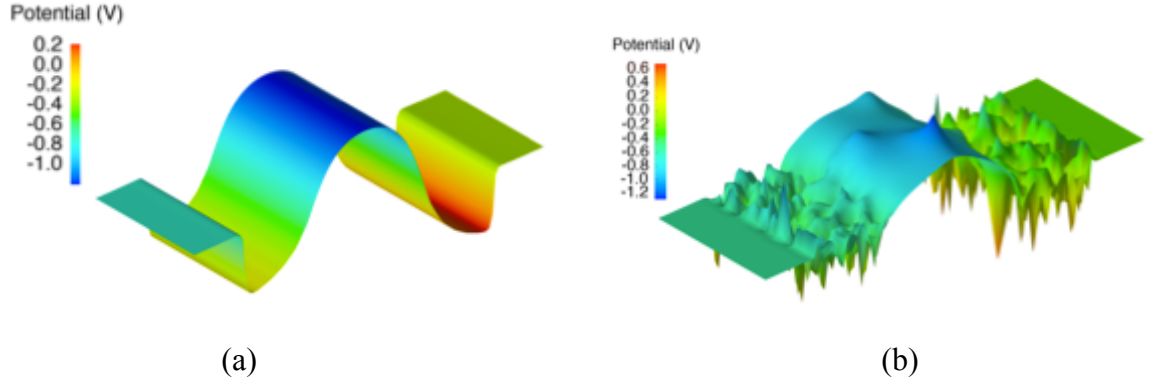


Figure 2.1 Potential profile of (a) a continuously doped device and (b) an atomistic device [74].

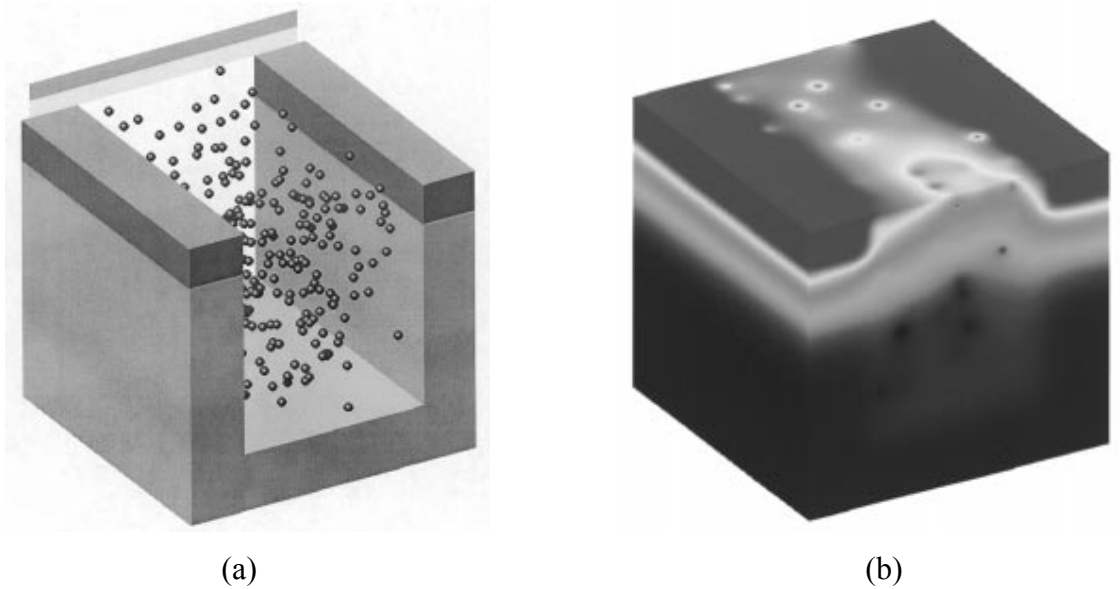


Figure 2.2 (a) Typical atomistic simulation domain and dopant distribution used in the simulation of a $30 \times 50 \text{ nm}^2$ n-channel MOSFET with oxide thickness $t_{ox} = 3 \text{ nm}$, junction depth $x_j = 7 \text{ nm}$, and channel acceptor concentration $N_A = 5 \times 10^{18} \text{ cm}^{-3}$. (b) Potential distribution at threshold voltage obtained from the atomistic density gradient simulation of a $30 \times 50 \text{ nm}^2$ MOSFET with design parameters given in (a) [70].

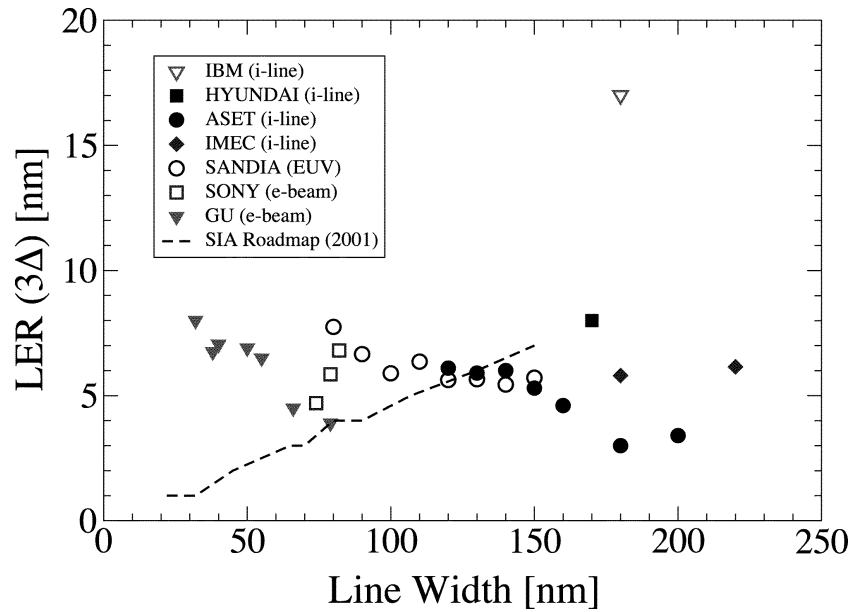


Figure 2.3 Actual data from various advanced lithography processes reported by different labs showing that LER does not scale with line width according with the Roadmap requirements [15].

2.2.2.2 Line Edge Roughness

Unfortunately, the random discrete dopant is not the only source of IPF for modern and future CMOS transistors. Line edge roughness is yet another important source [15]. It arises due to the discrete molecular nature of photoresist used to coat the wafer during the fabrication process. Line edge roughness caused little impact on the critical dimensions of CMOS in the past, as its magnitude is negligible compared with the gate-length. However, it is confirmed by different labs that LER does not scale with the device, as shown in Figure 2.3, and becomes an increasingly larger fraction of the gate. Furthermore, it should be also noted that the impact of LER will not only affect transistors, but also device metal interconnections [75].

2.2.2.3 Oxide Thickness Fluctuations

The oxide thickness fluctuation of an atomistic device is another random variation source [68]. As the MOSFET gate length reduces, so must be the oxide gate thickness. For MOSFETs gate length less than 30 nm, the oxide thickness is 1 nm [76]. The interfaces between Si/SiO₂ and Gate/SiO₂ are extremely difficult to be precisely fabricated at this scale. With only a few silicon atomic layers, the interface roughness will derive significant

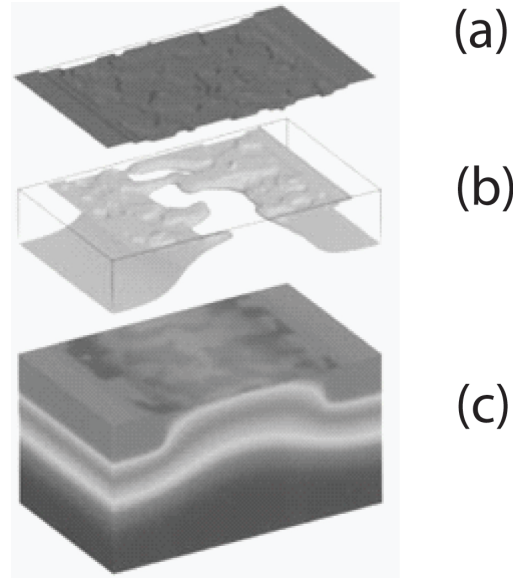


Figure 2.4 (a) Typical profile of the random Si/SiO₂ interface in a $30 \times 30 \text{ nm}^2$ MOSFET, followed by (b) an equiconcentration contour obtained from density gradient simulation, and (c) the potential distribution [68].

oxide thickness fluctuations underneath the gate area. Each device will eventually has a unique random oxide thickness landscape and interface pattern, which will lead to variations in carrier mobility, gate tunnelling current [77] and threshold voltage [16, 78] among devices. In Figure 2.4, a typical profile of a Si/SiO₂ interface in a $30 \times 30 \text{ nm}^2$ MOSFET is presented, which demonstrates a potential distribution due to the OTF.

2.2.2.4 Poly silicon Gate Granularity

The poly-silicon gate granularity is regarded as another important source of statistical variability [17, 69, 79]. The grain boundaries can enhance dopant diffusion that may cause a non-uniform doping within the poly silicon gate, where high doping regions may result in a localized penetration of dopants into the device channel [79]. However, the most significant source of variation within the poly-gate may possibly be the Fermi-level pinning at the boundaries between grains [80]. The surface potential within the MOSFET channel varies due to the Fermi-level pinning at the interface between the grain boundaries and the dielectric. For example, the electrostatic potential of a $30 \times 30 \text{ nm}^2$ MOSFET with Fermi level pinning at polysilicon grain boundaries is shown in Figure 2.5. These potential fluctuations in surface will induce significant variations of threshold voltages and device characteristics among the devices, depending on the specific pattern of the polysilicon grain boundaries in the gate for each individual device.

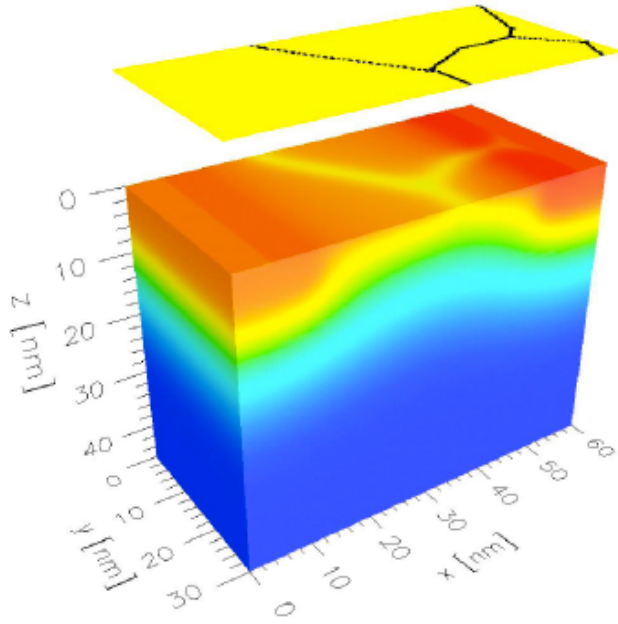


Figure 2.5 Electrostatic potential in a $30 \times 30 \text{ nm}^2$ MOSFET showing the impact on the channel potential of Fermi level pinning at the polysilicon grain boundaries. The location of the grain boundaries are shown in the plane above the device [69].

2.3 Modelling of Variability

Fabrication-induced variations have been identified as one of the most significant impediments for the IC design. The magnitude of the variations highly depends on the relevant IC technology process. Research and investigations have been carried out to characterise and model the device variability [28, 29, 43, 62], to estimate its impact on circuit behaviour [81, 82] and to develop new topologies and design techniques that can reduce the impact [44, 83]. Among all these efforts, characterising and modelling the variability lays the fundamental knowledge for the experimental investigations. The methodology of modelling and corresponding design procedures varies depending on the nature of the variations.

In the case of systematic variations, it is relatively easy to model and develop design solutions, since these types of variations can be expressed as a function of spatial parameters and process implementations. Corresponding layout solutions can be developed and applied during the floor planning and layout stages, such as using symmetry style and adding dummy components. Therefore, the cost of compensation is relatively low. However, it should be noted that there are a few systematic variations that cannot be addressed during the design phase and fabrication process improvements are expected

instead. For example wafer level non-uniformity cannot be cancelled by changing the design [41]. In this thesis, the impact of systematic variations will not be discussed.

On the other hand, random variations are much more difficult to eliminate for the circuit designers. The available data of the parameters are normally the statistical distributions of each variation source. From the design point of view, sufficient design margins should be left during the design phase in order to reach all design corners and achieve a sensible yield level. However, this over engineering would normally trade with more silicon area, power consumption and circuit speed [81], which will further increase the final chip cost. Furthermore, more money for characterising the variations is required to be invested during the scaling of MOSFETs to a new technology generation. This is because the magnitude of existing random variation sources may increase, new random variability sources may be explored or existing random source may be identified with a systematic nature. All these understandings and interpretations due to the extra investment will in turn facilitate a reduction in design margin costs. Therefore, to model the variability is a compulsory step for both existing and new technology generations.

2.3.1 Test Structure

To retrieve the information of systematic or random variations, custom designed circuit layouts are used. Each of them has a unique arrangement that is used to characterise one specific type of variation. These circuits are called test structures and regularly embedded on particular positions of each wafer. Different manufacturers and foundries have published a variety of test structures to achieve better characterization performances. A famous annual conference from IEEE is even dedicated to discuss the test structures under different circumstances: International Conference on Microelectronic Test Structures (ICMTS) [84].

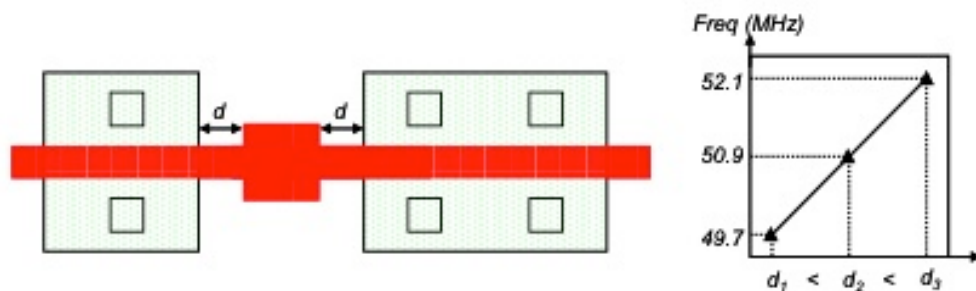


Figure 2.6 Measured dependence of mean ring oscillator frequency on polysilicon contact landing pad to the diffusion region spacing [57].

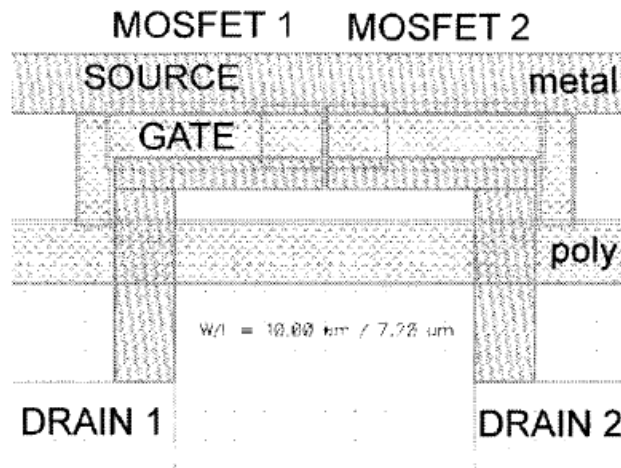


Figure 2.7 Layout of test structure [85].

The requirements of test structures for systematic and random variations are different. For the systematic variations, it should be ideally designed to reflect the gradient of systematic change without being contaminated by the random variations. It was reported in [58] that ring oscillator based structures are popular to measure the layout dependent effects, as the random variation are averaged out across all the oscillator stages. Furthermore, the results could be easily retrieved by reading the output of the frequency counters. In Figure 2.6, the impact of spacing between the poly gate contact landing pad and the diffusion region is investigated using the mean ring oscillator frequency.

However, for the case of random variations, the requirements of the test structures are much more strict. The test structures should have a large measurement sample in order to obtain a confident statistical estimation. All the devices under test (DUT) need to be placed close to each other and should be measurable individually. Furthermore, the layout of each DUT should: (a) be identically designed and oriented so as to guarantee the currents flow in the same direction, (b) have identical metal connections from DUT to the contact pads, (c) have double (force and sense) contact pads for all terminals, (d) is placed "infinitely" far away from disturbing topography and crystal edges and (e) is symmetrical with respect to the surrounding metallization. Although it is difficult to fulfil some of the requirements, a good estimation of the magnitude of the random variations can still be obtained using carefully designed test structures. Furthermore, despite the strict requirements for test structures mentioned above, more unwanted mismatch would also be added during IC packaging and measuring. For example, during chip bonding, non-uniform die heating may impact the device performance. During chip measurement, every machine has a limited reproducibility and resolution, near which the measurements are normally performed.

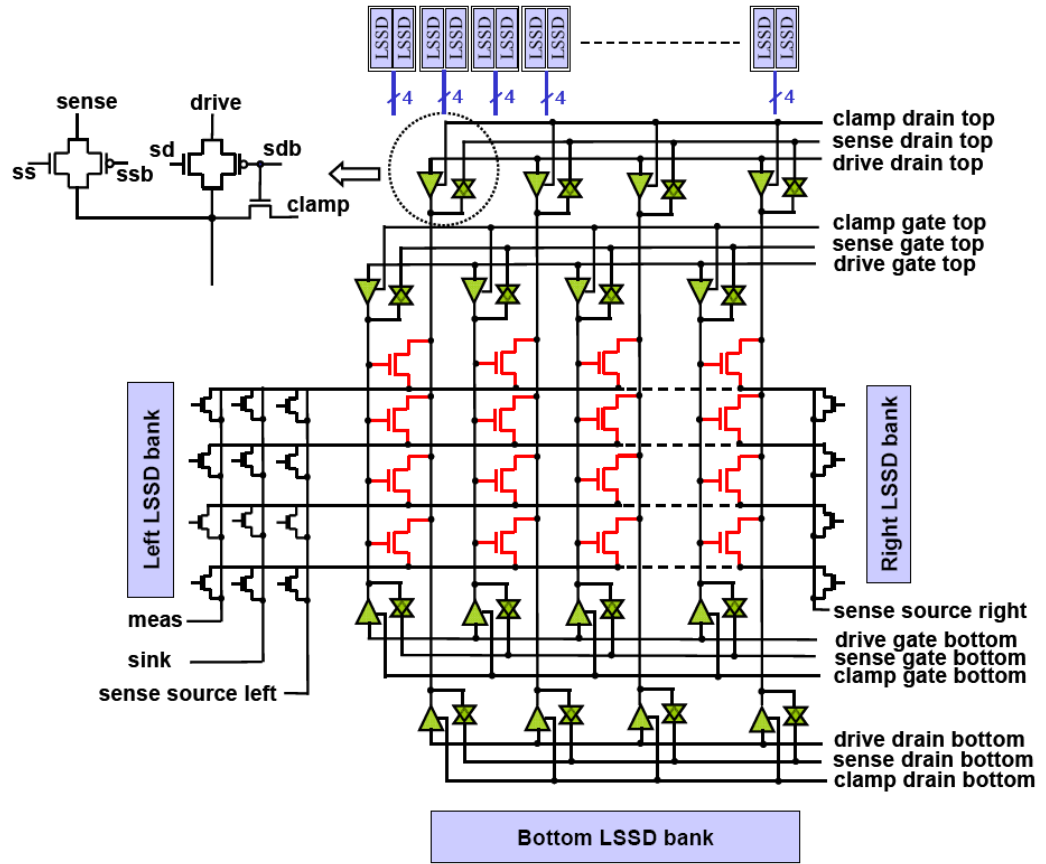


Figure 2.8 Device array for characterizing random variations [37].

Different random variation test structures have been published. In [85], a typical test structure for measuring random variations is introduced, as shown in Figure 2.7. The two devices under test have a common symmetric gate, source and bulk connections. Their drains were bonded to different pads and measured using two switching matrix units (SMU). The sizes of this pair were selected to be $W/L = 10 \mu\text{m}/7.2 \mu\text{m}$. After measurements of 1176 pairs with different sizes from different chips, the random variation information of drain currents was extracted. Furthermore, IBM developed another random variation test structure in 2006 [37], as shown in Figure 2.8. A total of 96,000 devices were placed in 1,000 columns with 96 devices in each column that occupy a silicon area of $1250 \mu\text{m}$ by $110 \mu\text{m}$. Four level sensitive scan design latch banks were placed on four sides of the test structure. The top and bottom banks can select the column for testing, whilst connecting the non-selected columns to the clamp voltage. The left and right banks set up proper measure, sink and tow-sense for each row.

2.3.2 Device Mismatch Modelling

By using the random variation test structure introduced above, the measurements are normally in the form of drain currents (I_{DS}) as a function of gate voltage (V_{GS}) when drain voltage (V_{DS}) is low [30]. The ensemble of all the measured currents contains combined information of random variations that could be further interpreted using an analytical mismatch model with design-related parameters. The mismatch model is widely used by both sides of manufacturers and designers in order to translate the process variations in form of sensible design parameters.

The modelling of mismatch can be traced back to the early 1980s, when circuit designers tried to migrate the analogue designs from bipolar technology to the standard digital CMOS processes. In 1984, an early version of a mismatch model for capacitors and n-channel MOS transistors was published in [28]. The model included some major sources of variances that are still considered today, including edge effect, implantation and surface state charges, oxide effect and channel mobility effect. In the work, five test chips were fabricated and measured using 3.5 μm NMOS technology from the Xerox Microelectronics Centre in order to verify the model. The trend that increasing transistor size will reduce device mismatch was observed. However, this model contained too many process-related parameters rather than design-related parameters for designers to use and missed the opportunity to show that variation decreases with the square root of the effective area. Inspired by [28], an improved mismatch model for analogue circuit design was published in 1986, with an objective that can "predict mismatch in the drain current over a wide range of operation conditions using a minimum set of measured data, and simultaneously to throw light on the detailed causes of mismatch" [29]. For the first time, the model described the device mismatch using both the standard deviations of device V_{TH} and β . These deviations can be tracked back to the potential causes in device physics as well. The drain current expression used in the paper was a typical long-channel quadratic function:

$$I_{DS} = \frac{\beta}{2} (V_{GS} - V_{TH})^2 \quad \text{Eq. (2.1)}$$

The normalised variance of the drain current was given by:

$$\frac{\sigma^2(I_{DS})}{I_{DS}^2} = \frac{\sigma^2(\beta)}{\beta^2} + 4 \frac{\sigma^2(V_{TH})}{(V_{GS} - V_{TH})^2} - 4r \frac{\sigma(V_{TH}) \cdot \sigma(\beta)}{\beta(V_{GS} - V_{TH})} \quad \text{Eq. (2.2)}$$

where $\sigma^2(*)$ represents the variance of the term, r is the correlation coefficient between mismatch in V_{TH} and β . In the paper, it was admitted that the quadratic current model is not an accurate description of I_{DS} / V_{GS} relationship and argued that the absolute value of drain current would cancel out to the first order during mismatch estimation. However, this is not true for small geometry devices in the UDSM regime, as will be shown in Chapter 3. In 1989, it was pointed out in a milestone publication of the mismatch modelling [30] that the current factor mismatch ($\sigma^2(\beta)/\beta$) estimation in [29] was wrong and limited variation in W/L ratios cannot be distinguished by alternative hypotheses. In [30], the variation of a design parameter (ΔP) between two rectangular devices was mathematically proved to be:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D \quad \text{Eq. (2.3)}$$

where A_P is the area proportionality constant for parameter P , S_P is the variation of P with the spacing and D represents the spacing information. This expression has become the fundamental relationship for modelling the process mismatch for subsequent researches. Furthermore, by replacing P with V_{TH} and β , technology constants A_{TH} and A_β are widely used by manufacturers and foundries for describing the process random variation after this research. These technology constants are also reported annually in the ITRS roadmap [4]. A more precise I_{DS} / V_{GS} relationship was also used in the paper:

$$I_{DS} = \beta \left\{ \frac{\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}}{1 + \theta(V_{GS} - V_{TH})} \right\} \quad \text{Eq. (2.4)}$$

where θ is the mobility degradation factor. The threshold voltage V_{TH} was further expressed as:

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|V_{SB}| + 2\Phi_F} - \sqrt{2\Phi_F} \right) \quad \text{Eq. (2.5)}$$

where V_{SB} represents the source bulk voltage, V_{TH0} is the threshold voltage when $V_{SB} = 0$ V, γ represents the body effect factor and Φ_F is Fermi potential in strong inversion. In the paper, V_{TH0} , γ , and β were all regarded as random parameters and their variations were given by:

$$\sigma^2(V_{TH0}) = \frac{A_{V_{TH0}}^2}{WL} + S_{V_{TH0}}^2 D^2 \quad \text{Eq. (2.6)}$$

$$\sigma^2(\gamma) = \frac{A_{\gamma}^2}{WL} + S_{\gamma}^2 D^2 \quad \text{Eq. (2.7)}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_{\beta}^2}{WL} + S_{\beta}^2 D^2 \quad \text{Eq. (2.8)}$$

Furthermore, a random mismatch parameter evaluation flow chart was also established and widely used in the subsequent researches, as shown in Figure 2.9.

It should be pointed out that, after the publication of the above research, two opposite flavours of mismatch modelling methodologies were widely diverted since 1990s. Realising that the accuracy of the drain current expression was critical for the estimation of mismatch, some researchers have been focusing on improving the precision of the drain current expression by including more and more physical related parameters into the device model [42]. Nowadays, the drain current model has over hundreds of parameters, such as (Berkeley Short-channel IGFET Model, version 4) BSIM4 and (Penn State Philips) PSP

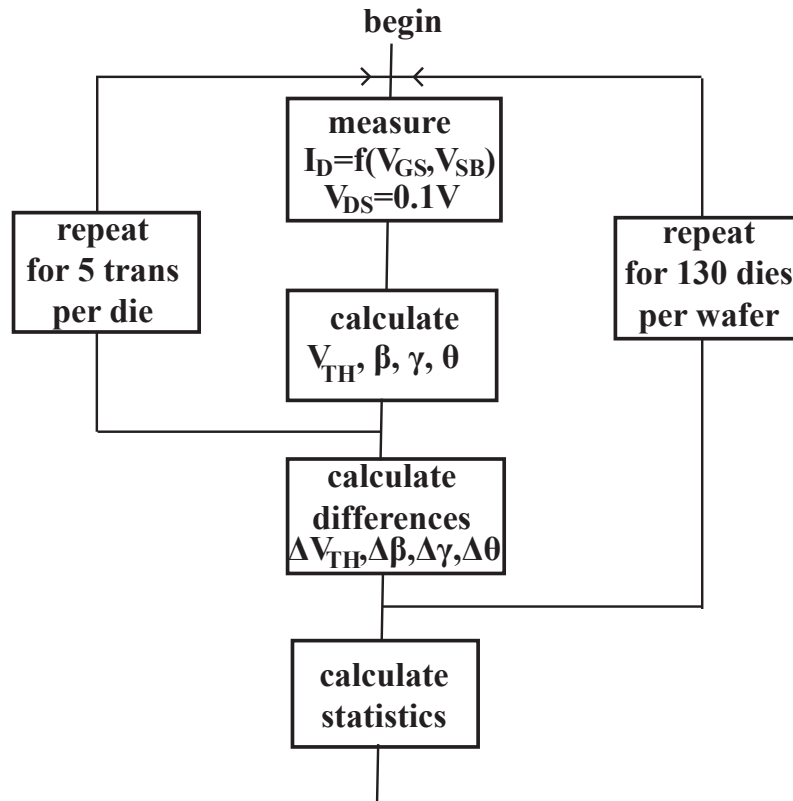


Figure 2.9 Random variation evaluation procedure [30].

transistor models, and can only be handled by using computer-based numerical simulators. The mismatch evaluation could be carried out by using Monte Carlo simulations that have an incontrovertible accuracy. However, the simulation results gave no indication in the form of meaningful design parameters for the circuit designers, such as size, working currents and voltages. This mismatch modelling method gradually became the methodology for the device modellers and only used as a verification tool in terms of circuit design.

Meanwhile, other efforts have been spent on modelling the mismatch using an improved simple drain current expression that is suitable for hand calculation and can give insights into design parameters for circuit designers. Following the style of initial papers of [29, 30], this approach has been significantly contributed by research groups from IMEC and Katholieke Universiteit Leuven in Belgium [32, 34, 36]. In 1995, another improved drain current expression was used in [86]:

$$I_{DS} = \frac{1}{2} \cdot \frac{\beta}{1 + \theta(V_{GS} - V_{TH})} (V_{GS} - V_{TH})^2 \quad \text{Eq. (2.9)}$$

where all the parameters (including current factor β , mobility degradation θ and threshold voltage V_{TH}) were curve fitted by using the measured drain current from a 1.2 μm process test structure. The drain current variation was given by:

$$\begin{aligned} \sigma^2\left(\frac{\Delta I_D}{I_D}\right) &= \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4}{(V_{GS} - V_{TH})^2} \sigma^2(\Delta V_{TH}) + \left[\frac{(V_{GS} - V_{TH})^2}{1 + \theta(V_{GS} - V_{TH})}\right] \sigma^2(\Delta\theta) \quad \text{Eq. (2.10)} \\ &+ 2\rho\left(\frac{\Delta\beta}{\beta}, \Delta V_{TH}\right) \left[-\frac{2}{(V_{GS} - V_{TH})}\right] \sigma\left(\Delta V_{TH}\right) \sigma\left(\frac{\Delta\beta}{\beta}\right) \\ &+ 2\rho\left(\frac{\Delta\beta}{\beta}, \Delta\theta\right) \left[-\frac{(V_{GS} - V_{TH})}{1 + \theta(V_{GS} - V_{TH})}\right] \sigma(\Delta\theta) \sigma\left(\frac{\Delta\beta}{\beta}\right) \\ &+ 2\rho(\Delta V_{TH}, \Delta\theta) \left[-\frac{2}{1 + \theta(V_{GS} - V_{TH})}\right] \sigma(\Delta\theta) \sigma(\Delta V_{TH}) \end{aligned}$$

where $\rho(*)$ is the correlation term. Compared with Eq. (2.1) and Eq. (2.4), this model has achieved a good agreement between the theory and the practice. Furthermore, the correlation terms have been taken into account in the model for the first time. From the same research group, another more general model was presented in 2002 [43]. By applying

the Taylor expansion to any drain current expression to the first derivative term, the drain current mismatch can be expressed as:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial P_1} \Delta P_1 + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial P_2} \Delta P_2 + \dots \quad \text{Eq. (2.11)}$$

where parameters $(\Delta P_1, \Delta P_2, \dots)$ described the mismatch in drain current model parameters (P_1, P_2, \dots) . Furthermore, the mean $\mu(*)$ and variance $\sigma^2(*)$ of drain current mismatch can be expressed as:

$$\mu\left(\frac{\Delta I_{DS}}{I_{DS}}\right) = \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial P_1} \mu_{\Delta P_1} + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial P_2} \mu_{\Delta P_2} + \dots \quad \text{Eq. (2.12)}$$

and

$$\begin{aligned} \sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) &= \left(\frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial P_1}\right)^2 \sigma_{\Delta P_1}^2 + \left(\frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial P_2}\right)^2 \sigma_{\Delta P_2}^2 \\ &+ \frac{2}{I_{DS}^2} \frac{\partial I_{DS}}{\partial P_1} \frac{\partial I_{DS}}{\partial P_2} \rho(\Delta P_1, \Delta P_2) \sigma_{\Delta P_1} \sigma_{\Delta P_2} + \dots \end{aligned} \quad \text{Eq. (2.13)}$$

This model is a general summary of previous models, and can also be applied to the short-channel devices. Based on the knowledge of mismatch modelling introduced in this section, a new mismatch model for short-channel devices will be discussed in detail in Chapter 3 with the velocity saturation and mobility degradation taken into consideration.

2.3.3 Circuit Performance & Yield Estimation

In [29], besides the proposed the mismatch model, a demonstration of how to apply the model in estimating the yield of a current source digital-to-analogue converter (DAC) was given. The schematic of the DAC from [29] is illustrated in Figure 2.10. After the drain current mismatch data was extracted from each branch, the statistical information of DAC output x and its complementary value y was calculated. The yield was defined as the percentage of functional devices that have integral nonlinearity (INL) less than half of a least significant bit (LSB). The normalised output $z=x/(x+y)$ was assumed to have a Gaussian distribution with a joint probability variance from the variances of x and y . The yield of the current DAC was given as:

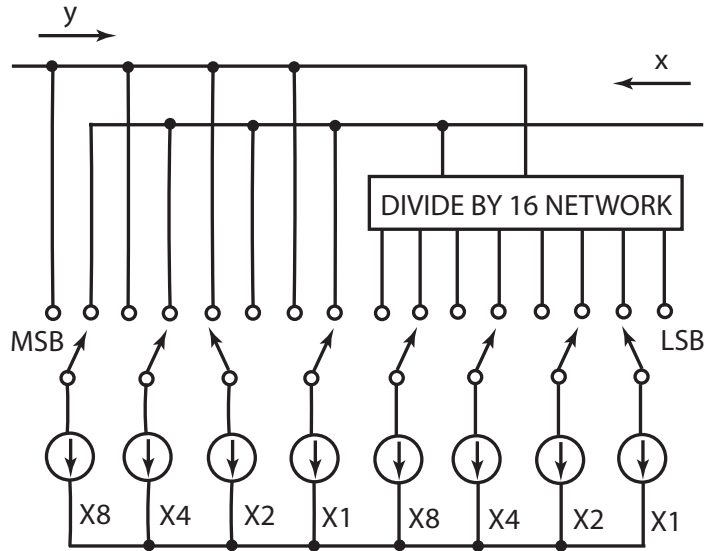


Figure 2.10 Schematic of a multiple current-source DAC [29].

$$\begin{aligned}
 G &= \prod_{i=127}^{128} \frac{1}{\sqrt{2\pi} \cdot \sigma_z} \int_{\bar{z}-\frac{1}{512}}^{\bar{z}+\frac{1}{512}} \exp\left\{-\frac{(z-\bar{z})^2}{2\sigma_z^2}\right\} \cdot dz \\
 &= \prod_{i=127}^{128} \operatorname{erf}\left(\frac{Q}{\sqrt{2}}\right)
 \end{aligned}
 \tag{2.14}$$

where $1/512$ was normalised $1/2$ LSB value, erf is the error function and Q is given by:

$$Q = \frac{1}{512 \left[\frac{\bar{z}(1-\bar{z})}{15 + 15/16} \right]^{1/2}} \frac{\sigma}{\bar{I}}.
 \tag{2.15}$$

Another example of yield estimation has given for an ADC. In 1993, an 8-bit ADC design was published in [27]. In the paper, an early version of the criteria that used for estimating the yield of a flash ADC were given as:

- (a) $\text{Yield} = (1-p)^{2^N-2}$, with
- (b) $p = \text{probability}\left(\frac{V_{inN} - V_{inN-1} - 1\text{LSB}}{\sigma\sqrt{2}} < \frac{-1\text{LSB}}{\sigma\sqrt{2}}\right)$
- (c) $\text{LSB} = \frac{\text{input range}}{2^N}$.

This theory requires a good evaluation of the offset voltage of a comparator. However, the CMOS comparator design in early 1990s was "lack of accuracy". Little attention was paid to modelling the offset voltage of a comparator. Only until recently, the modelling of the

offset voltage of a latch-based comparator has come into circuit designer's scope [22, 87, 88]. This is mainly because that the dynamic positive feedback of the latch stage is difficult to be modelled.

The yield estimation of an operational amplifier (op-amp) is relatively easy, as the op-amp works at a fixed operational point. The offset voltage of an op-amp is mainly introduced by the symmetric analogue cells, such as the differential pair and current mirror. Based on the I/V characteristics of the operation point and the readily available process variation data, the magnitudes of mismatch from these symmetric cells can be estimated. Drain current mismatch (ΔI_{DS}) and gate voltage mismatch (ΔV_{GS}) are two metrics used for measuring the mismatch in the current mirrors and differential pairs, respectively [81]. The offset voltage of the op-amp can then be obtained based on the collected mismatch information from all the symmetric cells within the circuit.

In Chapter 3, a new drain current mismatch model and a gate voltage mismatch model will be presented for short-channel devices. A case study of how to apply the proposed mismatch model in evaluating the offset voltage of a differential amplifier will also be demonstrated. These models are verified by using Monte-Carlo simulations with two ensembles of 200 BSIM4 compact model cards that describe the NMOS and PMOS transistors of the 35 nm gate-length technology. Each BSIM4 model card represents a transistor with a nominally identical macroscopic device design with different microscopic configurations of RDD, LER and PGG. All of the model cards have met the requirements of the 45 nm technology node from ITRS [89].

2.4 Design for Variability

Mismatch introduced design constraints have confronted analogue circuit designers for decades. The trade-offs among accuracy, power and speed pose significant design challenges as devices are scaled. Different design solutions have been investigated and developed at different design hierarchies. At transistor level, the floating-gate technology has been migrated from digital applications to analogue. Body-biasing technology has also been reported for analogue applications that were initially used for digital circuit post-silicon tuning. At circuit level, auto-zeroing and correlated double sampling were developed for discrete signal circuits. Chopper stabilisation was used for continuous applications. In this section, these variation-aware designs will be reviewed in detail.

2.4.1 Transistor Level Compensation

2.4.1.1 Floating-Gate Structure

The principle of the floating-gate structure is to use the polysilicon gate of an MOSFET wrapped in silicon dioxide to store adjusted charge during the circuit operation [90]. The charge can be modified by means of: (a) ultraviolet (UV) light projection, (b) Fowler-Nordheim tunnelling and c) hot-electron injection. It is stored on the integrated capacitor with a continuous value. The charge can further be interpreted as an extra voltage applied to the gate that changes the threshold voltage of the device accordingly. However, since there is no DC path to the floating-gate terminal, it is almost impossible to analyse this transistor element using standard numerical simulators, such as SPICE. Although a few approaches have been proposed to replace the floating-gate device with an equivalent circuit, these models were not based on the physics of the device, so the accuracy of estimation varies from the actual measurements and could only be used to simulate particular aspects of the floating-gate devices [91-93].

The floating-gate structure has been prevalent as a circuit adjustment solution. It can be dated back to 1967, when Kahng and Sze first reported the structure as a solution for non-volatile information storage [94]. Later on, this structure was used for a significantly long period in IC history as a non-volatile digital information storage method for circuits like EPROMs, EEPROMs, and flash memories [95] that were used in every personal computer [96]. During the late 1980s, researchers began to engineer and merge floating-gate structure into analogue IC design solutions [97, 98]. In the 1990s, the number of analogue applications using floating-gate was further increased [99, 100]. More importantly, the structure could also be cheaply implemented using a standard CMOS process [101] that providing mix-signal circuit designers with a wider choice of solutions.

The use of the floating-gate device for mismatch compensation in analogue circuit design began to flourish after the new millennium. In 2002, an offset removal circuit using the floating-gate was proposed for differential amplifiers and mixers using MOSIS 0.5 μm process. The floating-gate differential pair was initialised to zero by Fowler-Nordheim tunnelling and charged iteratively using hot-electron injection until a balanced drain current was achieved [44, 102]. Despite of the gate leakage and gain error [103], it was demonstrated that floating-gate devices could be one of potential solutions to the mismatch

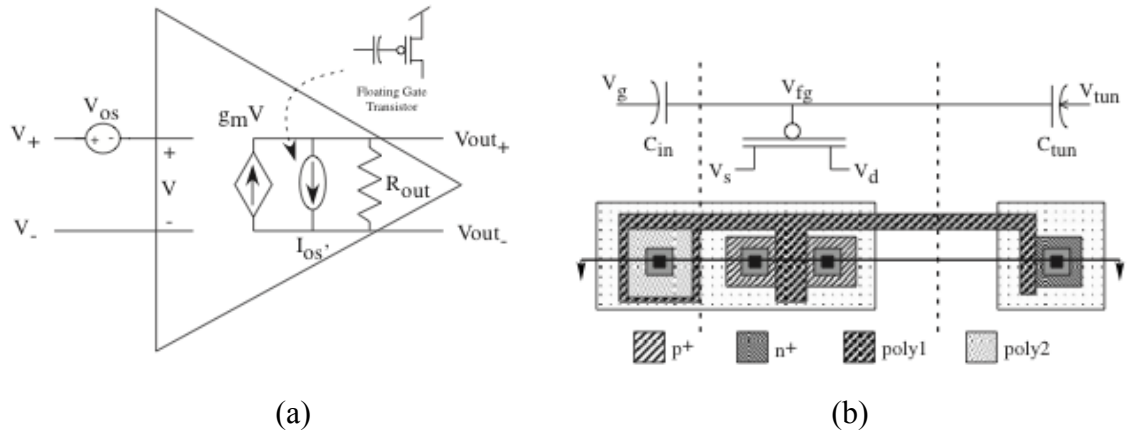


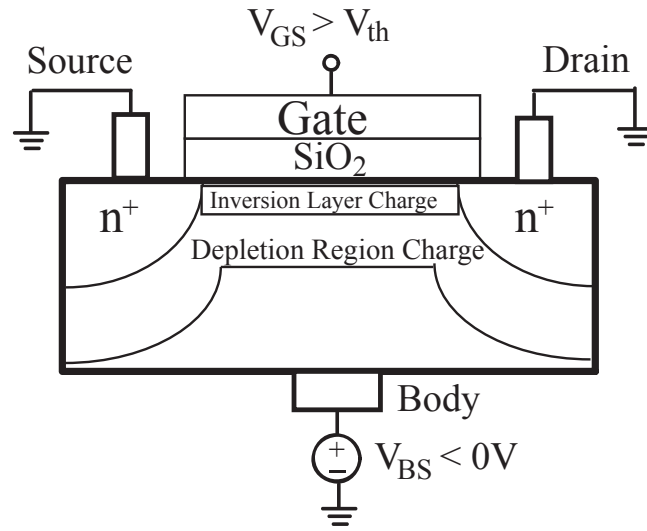
Figure 2.11 (a) Offset Cancellation Macromodel: Offset voltage of the amplifier is compensated by programming an offset current I_{os} . (b) Circuit schematic and layout of PMOS floating-gate transistor [47].

problem in analogue circuit design. An operational amplifier using floating-gate for offset cancellation was presented in 2005 [47]. The conceptual equivalent circuit of this op-amp is shown in Figure 2.11 (a). An adjustable current source (I_{os}), implemented using floating-gate transistor, was used for offset compensation. Figure 2.11 (b) shows the floating-gate transistor's layout. Furthermore, other different kinds of analogue circuits with floating-gate compensation were published, including: current mirror [103, 104], voltage reference [105], flash ADC [106] and DAC [107]. It was a well-established technology used by long-channel processes for precision analogue design and sensor designs.

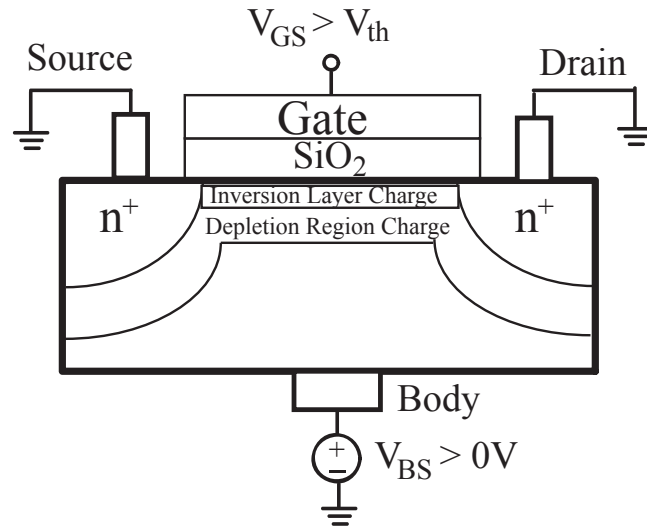
However, as the new technology process and materials merged into atomistic devices, analogue circuit design using floating-gate structure becomes more difficult. High-density gate stack makes the layout difficult to control. Gate-leakage due to high-k inter-poly dielectrics is also considerably increased. Moreover, only changing the threshold voltage by using floating-gate device cannot eliminate the device gain error introduced by mismatch. Aside from the above reasons, since there is no access to any foundry for this research, the floating-gate technology will not be used as one of the solutions in this thesis.

2.4.1.2 Body-Biasing

Low power consumption, low leakage current and high operation speed are always the main design objectives for portable and embedded devices. However, temperature and process introduced variation significantly reduces production yields, since more and more



(a) RBB.



(b) FBB

Figure 2.12 Body biasing principles. (a) Reverse Body-biasing. (b) Forward Body-biasing

dies fail to meet the power and delay specifications. Supply voltage scaling was widely used to decrease the power consumption in digital circuit design. However, circuit speed was inevitably decreased as a result of reduced drive currents. Alternatively, body-biasing technology was introduced to provide another knob to maintain the delay performance despite of the scaled supply voltage. The basic principle of body biasing technology is to change the threshold voltage of MOSFET device by adjusting the bulk-source potential (V_{BS}). The relationship has been expressed in Eq. (2.5). Depending on the polarity of V_{BS} applied to the bulk, body-biasing technology is catalogued into reverse body-biasing (RBB) and forward body-biasing (FBB). If a negative voltage is applied across the bulk-to-source P-N junction, the MOSFET is reversely body biased, as illustrated in Figure 2.12 (a). As a consequence, the width of the depletion region beneath the gate increases,

whilst the inversion layer decreases in order to maintain the charge balance. Therefore, the threshold voltage is increased, since a larger gate voltage is required to achieve a similar level of channel inversion as compared to a zero biased transistor. It is noted that an increased V_{TH} will help to reduce the sub-threshold current leakage that will further minimise the power consumption when the circuit is idle. However, it will also degrade the circuit speed due to the reduction of transistor current. Forward body bias works exactly opposite. If a positive voltage V_{BS} is applied, the threshold voltage decreases as the depletion region becomes thinner. It will increase the circuit speed at the cost of an increased subthreshold current leakage, as shown in Figure 2.12 (b).

Body biasing technology was firstly introduced in 1995 [108] to retain the device performance in terms of current driving capability and switching speed. It was further developed as an approach to adjust digital circuits in order to meet design specifications, such as delay and power. It is normally used in two typical scenarios [109]. Known as static body biasing, the first scenario is to apply RBB to a cluster of digital blocks or even the whole processor during the stand-by state, in order to reduce subthreshold leakage current. It would significantly reduce the power consumption of the portable devices and increases the battery life. The optimal biasing voltage could be calculated by using different algorithms [110, 111]. The second scheme is widely known as adaptive body biasing (ABB) that can operate in RBB or FBB to recover dies that are skewed by process variation through post-silicon tuning. The ABB was further used during the design of digital signal processors (DSP) [112] and microprocessors [109]. In terms of analogue applications, Bacinschi extended the technology for reducing the mismatch between differential pairs [48]. Grasso derived a Miller operational transconductance amplifier (OTA) with body-biased output stage to compensate the PVT variations [113]. It was also implemented in other analogue circuits, such as band-gap reference [114] and low-noise amplifier (LNA) [108] in order to overcome the mismatch problem.

However, as the gate-length of the transistor is scaled, the body effect of the bulk silicon device has also be reduced that further decreases the efficiency of body biasing technology. Furthermore, a triple-well process is normally required if NMOS transistors are body biased. Despite of the reduction in efficiency, an applicable compensation scheme using body biasing to overcome the device variability is still achievable in 35 nm CMOS. In Chapter 4, three body-biasing compensation schemes will be proposed, including RBB, FBB and ABB, respectively.

2.4.2 Circuit Level Compensation

From a signal processing point of view, mismatch introduced offset voltage can be regarded as a low frequency or DC noise that is relatively constant over time. Therefore, as part of noise cancellation and reshaping methods, high-pass filter and modulation techniques could be extremely useful for eliminating this imperfection. Auto-zeroing and correlated double sampling are two popular schemes developed using this idea and widely applied in the discrete signal systems, such as camera image sensors, to eliminate the process and temperature introduced variations. Chopper stabilization is another technology that is popular in relatively low frequency applications, such as bio-medical sensors. In this section, these existing variability-aware designs will be reviewed.

2.4.2.1 Auto-zeroing and Correlated Double Sampling

Auto-zeroing is a widely used method to cancel the offset voltage in the discrete signal circuits and systems, such as switch capacitor circuits. The principle of auto-zeroing is to store the unwanted dc offset voltage and noise during the sample and hold phase (ϕ_1), and subtract them from the signal at either the input or output stage during the operation phase (ϕ_2). It is normally implemented at a stage between input and output of the op-amp, named N, as shown in Figure 2.13. In Figure 2.13 (a), an analogue sample and hold circuit is used, whilst the same function is achieved using a digital circuit with a DAC in Figure 2.13 (b). By applying auto-zeroing cancellation method, not only the input offset voltage will be eliminated, but also the low frequency noises, such as $1/f$ noise, are significantly degraded. However, at the same time, wide band thermal noise is folded into the baseband, which will double the noise power spectral density. As the thermal noise is a time varying random process, its autocorrelation between two samples at ϕ_1 and ϕ_2 decreases fast compared with $1/f$ noise for a certain time interval τ .

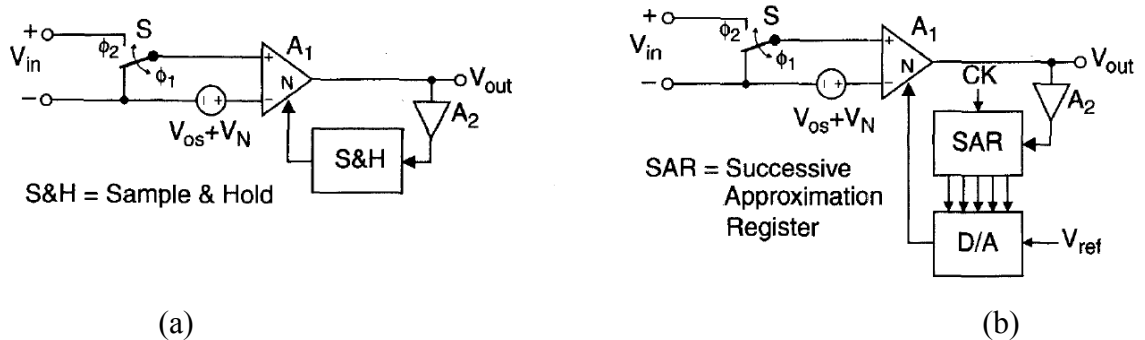


Figure 2.13 Basic Auto-zeroing Stages. (a) Analogue offset control storage and (b) digital offset control storage. [45]

In order to reduce the impact of folded thermal noise whilst still maintaining low offset voltage, an improved scheme is introduced, named correlated double sampling [115, 116]. In the scheme, two identical S/H circuits are attached after the amplifier rather than just one compared with the auto-zeroing. During the sample and hold phase ($\phi 1$), offset voltage, $1/f$ noise and the thermal noise are sampled by two S/H circuits at the same time. During the operational phase ($\phi 2$), the input signal is amplified and added with one sample at the amplifier output. The second sample is used to subtract from the above sum at the final output stage. The output signal is then free of offset voltage, $1/f$ noise and more importantly, folded thermal noise.

2.4.2.2 Chopper Stabilisation

Chopper stabilisation is another popular technology used for low frequency applications [45, 50, 117]. The basic principle of the chopper stabilisation technique is to modulate the input signal by the chopper frequency $\mathbf{m(t)}$ using the multiplier M1, as shown in Figure 2.14 (a), to avoid any contamination from offset or low frequency noise. After the modulated signal went through the amplification stage, the signal will be demodulated back to baseband using the multiplier M2. The signal is then free from the offset voltage and low frequency noise. The chopper carrier $\mathbf{m(t)}$ is a square-wave at a frequency of f_{chop} . To avoid any signal aliasing, f_{chop} should be at least twice higher than the maximum frequency of the signal. Figure 2.14 (b)-(d) shows the signal spectrum at different stages of the processing chain. It is noted that this scheme is extremely sensitive to the frequency response and delay of amplifier A1. Finite frequency response and delay of the amplifier A1 could introduce significant distortions to the system. For example, under a real application context, it can be assumed that: (a) the input signal is a DC signal with a value of V_{in} , (b) the amplifier A1 has a finite bandwidth with a constant gain of A_v up to $2f_{chop}$ and will be zero for the rest of the spectrum. The signal at the output of multiplier M1 has an amplitude of V_{in} , which is streamed into the amplifier A1. A1 rather than $A_v V_{in}$ will amplify the signal amplitude to $4/\pi A_v V_{in}$, due to the low-pass characteristics of A1. The demodulation multiplier M2 will rectify the signal by multiply the carrier $\mathbf{m(t)}$. The output amplitude will be decreased to $(8/\pi^2 A_v V_{in}) \approx 0.8 A_v V_{in}$ after the low-pass filtering at the end. The delay of the main amplifier A1 is another important factor that could potentially introduce a system failure. If the delay is equal to a quarter of the period of $\mathbf{m(t)}$, using the carrier $\mathbf{m(t)}$ for both multipliers M1 and M2 will lead to a zero output after the low-pass filtering.

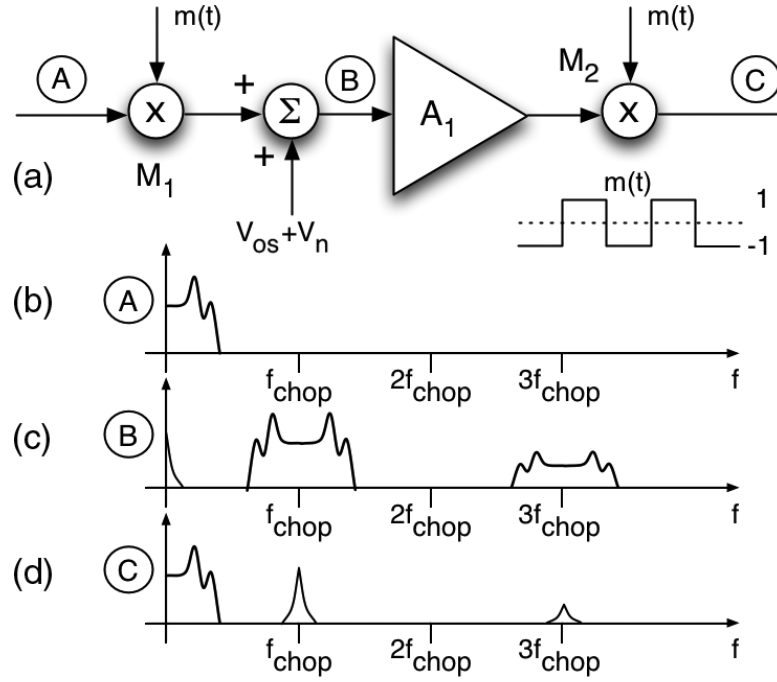


Figure 2.14 Chopper stabilisation principle.

Furthermore, since the input signal frequency is limited to be less than a half of the carrier frequency $m(t)$, chopper stabilisation technique can only be used in relatively low-frequency applications to avoid any signal aliasing during the modulation and demodulation stages.

2.5 Summary

In this chapter, different variation sources have been reviewed. These variations can be traced back to environmental and physical origins. Although the environment-induced variations can significantly degrade the performance of the circuits, these will not be discussed, since it is not in the main scope of this research. Process-induced systematic and random variations have also been introduced. The systematic variation can be cheaply engineered out, because it has a strong correlation with the position and layout style of a chip. However, the random variation is much more difficult to be eliminated. The magnitude of the random variation can only be expressed using its statistics. In the UDSM regime, the random variation is mainly contributed by the intrinsic parameter fluctuations (IPF). The main physical sources of IPF, including RDD, LER, OTF and PGG, have been discussed in detail. Existing test structures for the systematic and random variations have been reviewed. It is noted that the requirements of random variation test structures are

much more strict than that of the systematic variation test structures. Both kinds of test structures are important for the analogue circuit design, since the process-induced variations can be measured and extracted by embedding these structures on different locations of a wafer. These extracted parameters can further be interpreted into design-related parameters for circuit designers using the mismatch model.

In Section 2, important existing mismatch models have been reviewed. The mismatch performances and yields of a circuit can be evaluated using these models. Furthermore, it is noted that the existing mismatch models are developed based on the quadratic drain current expression of the long-channel device. Short-channel effects were not taken into account in these models. Therefore, as the scaling of the gate-length reached the sub-100 nm regime, the existing models could not fulfil the accuracy requirements for the atomistic devices. In Chapter 3, a novel mismatch model will be proposed to fulfil this gap. A case study of applying the proposed model to estimate the offset voltage of a differential amplifier will be given as well.

After the knowledge of the process variations has been obtained, design solutions are desired to overcome the impact of the extreme device variability. In Section 2.4, two transistor level techniques have been discussed. However, the floating-gate technique is difficult to use for atomistic devices due to a considerably large gate leakage and high stack density of the process. Body-biasing, on the other hand, could be a potential solution for the variability compensation. An applicable compensation scheme based on body-biasing will be proposed in Chapter 4. Inspired by the body-biasing technique, it is noted that the drain and the source terminals can also be used for variability compensation. Therefore, two additional compensation schemes, drain compensation scheme and source compensation scheme, will be presented in Chapter 4 as well. Furthermore, popular circuit level offset cancellation schemes have been reviewed in this chapter as well. It is noted that autozeroing and correlated double sampling are only suitable for discrete signal applications. Chopper stabilization is limited to relatively low frequency applications. None of them could fulfil the requirements of compensating a high-speed ADC. Therefore, a new low-power high-speed comparator with a compensation scheme will be proposed in Chapter 5. The limitations of low power and low supply voltage have been taken into account during the design of the comparator. Furthermore, it has been successfully used to build a 3-bit 10 GHz flash ADC as described in Chapter 6.

Chapter 3 Mismatch Modelling for Atomistic Device

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3.1 Impact of Variability at Transistor Level

As the feature size of the bulk silicon MOSFETs progressively scales into the UDSM regime, statistical device variability has become a major challenge for the next generation circuit design. As most analogue and digital circuits are built from large numbers of nominally identical transistor pairs, physical and electrical mismatch between the devices making up these pairs reduces circuits' reproducibility, reliability of functions, and may lead to a low yield after fabrication. Analogue circuit designs are particularly vulnerable as they work in small-signal mode where the operating precision is a top-priority design consideration. Due to the device variability, the electrical performance mismatch will have a further impact on the achievable accuracy of large circuit blocks, for example phase lock loops [25], flash ADCs [106] and DACs [107]. Therefore, an accurate estimation of the device mismatch is desired to quantitatively measure the performance degradation of these circuits during the design phase when process statistics are readily available.

During the evaluation of the device mismatch, two alternate methods are widely used. The first method is widely known as the Monte Carlo (MC) simulation method. Based on the same experiment settings and circuits under test, the method requires the simulation to be repeatedly carried out for a sufficient number of times in order to acquire a statistically accurate estimation. During the iterative simulation process, device variability is taken into account by randomising the transistors used in the circuit under test. The statistical information of output currents and voltages can then be acquired, where each simulation output is based on a randomised circuit arrangement. The method can provide superior accuracy based on the complex mathematical device models, for example BSIM4 and PSP. However, as the required number of simulations is significantly large, the convergence of the simulation dramatically decreases as the circuit size getting larger. The costs of the simulation CPU time will be significantly increased as well. On the other hand, analytical mismatch modelling is an alternative method that uses the simple device drain current equations and the fabrication process statistics to evaluate the mismatch. It can swiftly derive the mismatch information based on relatively simple mathematical expressions, and can provide similar estimation accuracy compared with the MC method. Furthermore, the estimation results of this method are given in form of the design parameters, such as transistor sizes and operational point, rather than a set of statistical test results that obtained from the Monte Carlo method. These design parameters can provide in-depth guidance

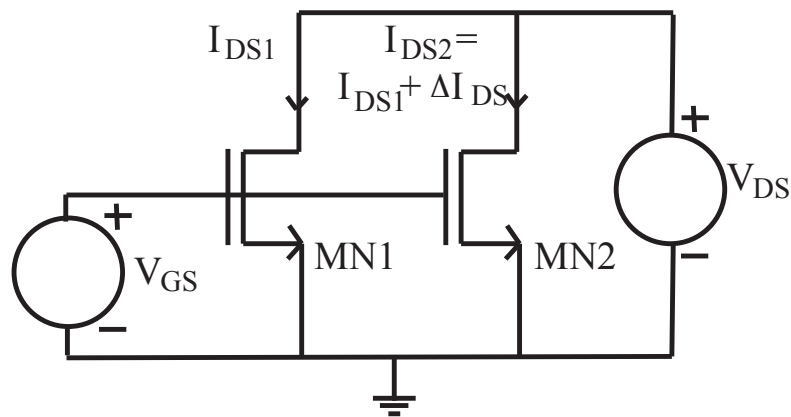
during the design phase, and aiding circuit designers to make design decisions. The process statistics are normally given in terms of the V_{TH} and β , where both of them have a Gaussian distribution. Furthermore, the drain current mismatch (ΔI_{DS}) and the gate voltage mismatch (ΔV_{GS}) can be expressed using the V_{TH} and β , where both ΔI_{DS} and ΔV_{GS} are used to describe the device electrical performance mismatch. In this thesis, MC simulation results will be used as test structure measurements from real silicon to verify the accuracy of the proposed analytical mismatch model. It is also used to test the functionality of the proposed compensation schemes in the following chapters.

The accuracy of the analytical mismatch modelling heavily relies on how well the drain current expression can describe the behaviour of a certain technology process. For the atomistic devices, this accuracy can be significantly improved by introducing two major short-channel effects. The first one is known as the mobility degradation. It can be observed when a large perpendicular field is applied to the transistor. The high electric field forces the channel under the silicon dioxide to become thinner and that leads to a significant charge carrier scattering and hence decreases the carrier mobility. Adding one extra fitting parameter into the short-channel expression can easily model this effect. The second effect is known as the velocity saturation. It arises because of the high lateral electric field (around 1 V/ μm) is applied between source and drain. When carriers enter the channel from the source, their accelerated speed begins to saturate to a constant value at some point between the source and drain. In the extreme case, the velocity saturation will immediately occur after the electrons dived into the channel. With these two short-channel effects take into account in the proposed analytical mismatch model, excellent agreements have been achieved between the MC method and the analytical method, as will be shown in Section 3.2.5.

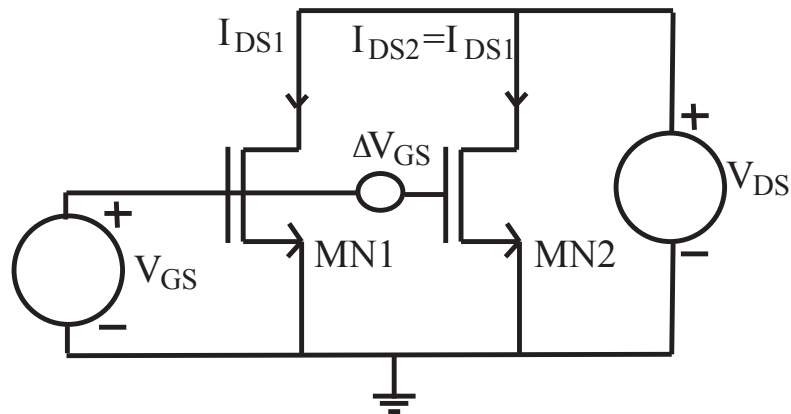
In this chapter, the impact of device variability on nominally identical transistors will be reviewed. The test circuit arrangement for this investigation will be illustrated. 200 n-MOSFETs and 200 p-MOSFETs BSIM4 compact models are used during the HSPICE simulations. These compact models have a gate-length of 35 nm, where each one has a unique configuration of RDD, LER and PGG. The simulation methodology that will be used through out this thesis will also be presented. Next, the accuracy of the proposed analytical mismatch model will be compared with the existing long-channel mismatch model to demonstrate the improvements. Moreover, a case study of how to apply the short-channel mismatch model to quickly and accurately evaluate the offset voltage of a differential pair will be presented in the Section 3.4.

3.1.1 Impact of Mismatch on Nominally Identical Transistors

The investigation of the device variability problem should start at the evaluation of the electrical behaviour mismatch between two nominally identical transistors [81]. As shown in Figure 3.1 (a), two macroscopically identical but microscopically different transistors MN1 and MN2 are biased using the same drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}). Due to the device variability, a drain current mismatch ($\Delta I_{DS} = I_{DS1} - I_{DS2}$)



(a)



(b)

Figure 3.1 (a) The transistor arrangement used to investigate drain current mismatch ΔI_{DS} of MOSFET devices under the same voltage bias conditions. (b) A transistor arrangement used to investigate gate voltage mismatch ΔV_{GS} for MOSFET devices. In both circuits MN1 is selected to be a reference model for all simulations.

is introduced, which can further be used as an indicator to quantitatively reflect the mismatch between the two devices. The other parameter that can also indicate the device mismatch is known as gate voltage mismatch (ΔV_{GS}). It describes the difference of V_{GS} required for MN2 to draw the same drain current as MN1 when the same biasing voltages are applied, as shown in Figure 3.1 (b).

Quantitative analysis of ΔI_{DS} and ΔV_{GS} are possible as both of them can be expressed using the differences of threshold voltage (ΔV_{TH}) and current factor ($\Delta\beta$) between MN1 and MN2. For 200 n-MOSFETs, the threshold voltage V_{TH} of the ensemble has a Gaussian distribution with a mean value of 255 mV and a standard deviation of 38.6 mV. In this thesis, the notations of V_{TH} and $\sigma^2(V_{TH})$ will be used to represent the mean and the variance of the threshold voltage, respectively. Similarly, β and $\sigma^2(\beta)$ will represent the mean and the variance of the current factor. Since the difference of the threshold voltages is defined as $\Delta V_{TH} = V_{TH1} - V_{TH2}$, it is easy to know that ΔV_{TH} also has a Gaussian distribution with a mean of zero and a variation of $2\sigma^2(V_{TH})$. This applies to $\Delta\beta$ as well.

Based on the above test bench arrangements, the ensemble of n-MOSFET BSIM4 compact model was iteratively tested. Transistor MN1 in Figure 3.1 (a) and (b) is selected as a reference transistor during the simulations. The compact model used for MN1 has a uniform configuration profile of RDD, LER and PGG, whilst a randomly picked compact model is used for MN2. In Figure 3.2, the simulation results of the above circuit arrangements are plotted. Figure 3.2 (a) shows the DC analysis simulation results of the circuit arrangement in Figure 3.1 (a) using all the compact models. The drain current of the reference transistor MN1 is plotted using the red curve. The rest model cards that are iteratively used for MN2 are plotted in yellow. The mean value curve of all drain currents is plotted using blue. For a given gate voltage ($V_{GS} = 0.64$ V), the histogram of the drain current spread is shown in the inset of the Figure 3.2 (a). The bins that contain the "uniform" model and the mean value are highlighted in red and blue, respectively. Next, Figure 3.2 (b) shows the drain currents of the randomised MN2 after an extra gate voltage (ΔV_{GS}) is applied in order to match the current of MN1 (I_{DS1}). The ΔV_{GS} used for MN2 was calculated using the short-channel mismatch model that will be introduced in the Section 3.2. With the same gate-source voltage ($V_{GS} = 0.64$ V) and drain-source voltage ($V_{DS} = 1$ V), the drain currents of all the devices are approximately compensated at the same point. The histogram of required ΔV_{GS} for all the devices is plotted in the inset of Figure 3.2 (b). If the "uniform" model is selected for MN2 as well, the required ΔV_{GS} will

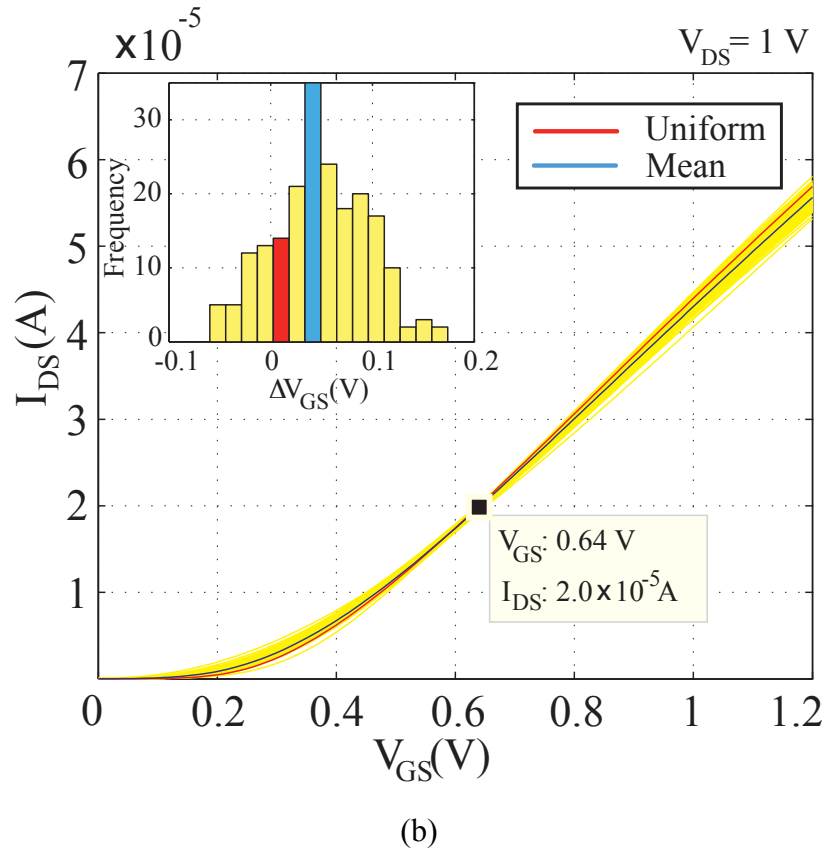
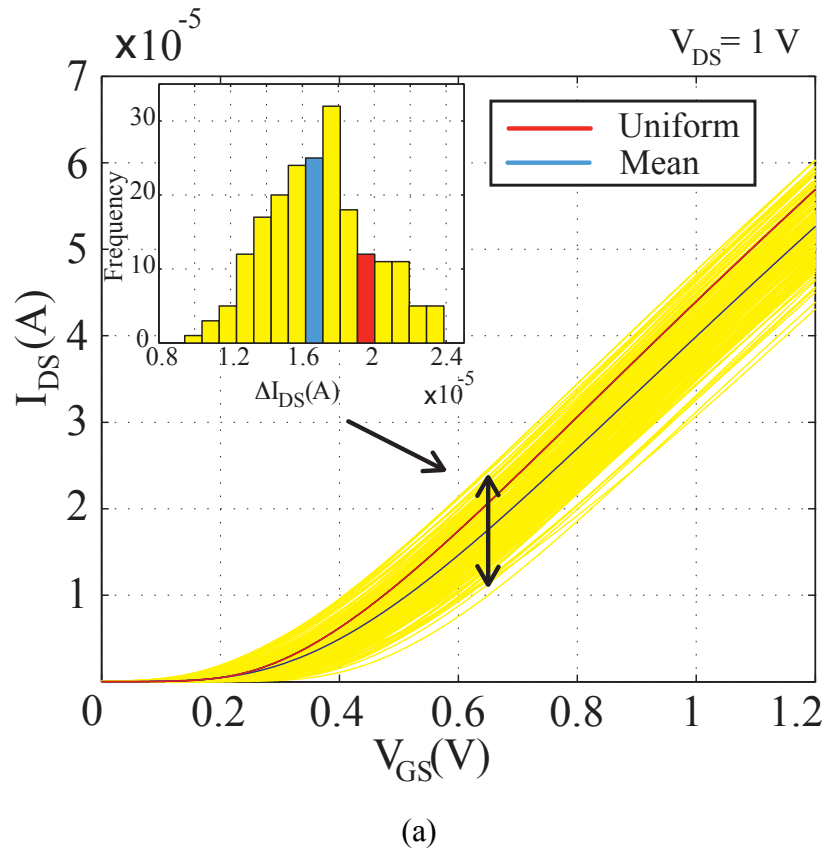


Figure 3.2 (a) I_{DS} / V_{GS} characteristics of all model cards using the circuit arrangement in Figure 3.1 (a). Inset: A histogram of ΔI_{DS} . (b) I_{DS} / V_{GS} characteristics when V_{GS} to MN2 is offset from MN1 to match I_{DS} in both MOSFETS. Inset: A histogram of ΔV_{GS} .

be zero voltage that falls into the red bin in the inset of Figure 3.2 (b). Furthermore, the required ΔV_{GS} is 0.048V for calibrating the mean drain current that is highlighted using blue in the same histogram. It is further noted that for the rest region of the compensated curves in Figure 3.2 (b), small gain errors still exist. This imperfection will be further discussed in Section 4.1.2 in the Chapter 4.

From the Figure 3.1 (a), it could be observed that the drain current of the uniform device is not same as the mean value of all the drain currents. This is because the drain current of an atomistic device is not linearly related to all the variation sources. For example, the gate capacitance per unit area C_{OX} in the drain current expression is inversely-proportional to the thickness of the silicon dioxide t_{ox} . Therefore, if the mean value of t_{ox} is 3 nm and uniformly distributed between 1 nm and 5 nm, the distribution of the C_{OX} will be skewed from $0.2 \times 10^9 \times \epsilon_0 \epsilon_{SiO2}$ to $10^9 \times \epsilon_0 \epsilon_{SiO2}$, where the C_{OX} of $t_{ox}=3$ nm is $0.33 \times 10^9 \times \epsilon_0 \epsilon_{SiO2}$. The distribution of the drain currents will be skewed accordingly.

The experiment results shown in Figure 3.2 quantitatively illustrate that the variability has a significant impact on the marching performance of the atomistic devices. Both ΔI_{DS} and ΔV_{GS} can be used to evaluate the performance variations. A linear relationship is also found between ΔI_{DS} and ΔV_{GS} as a voltage change at the gate will result a corresponding drain current change. The coefficient is equal to the device transconductance (g_m).

3.1.2 Monte Carlo Simulation Methodology

The Monte Carlo (MC) simulation method has a superior accuracy advantage over the analytical mismatch model. In this research, it is assumed that the results of Monte Carlo simulations can accurately represent real measurements from fabricated silicon. This is because that the BSIM4 compact model cards used in this research were developed from quantum physics simulations and proved to be accurate against published technologies [19]. The MC method will be used to verify the accuracy of the results estimated by the analytical method for the transistor pairs in this chapter. It will further be used to estimate the improvements of the compensation circuit in Chapter 4, 5 and 6.

The flow chart of the Monte Carlo simulation methodology is shown in Figure 3.3. It starts from a generic circuit netlist describing the circuit under test. This netlist is used as a template for generating a large number of randomised netlists, typically a few thousand.

Combined with the compact model library, the randomised netlists are created using MATLAB where the model keyword in the generic netlist is replaced by a randomly picked compact model name from the library. Then, the generated randomised netlists are pushed into HSPICE simulator for analysis. The HSPICE output data files are stored in plain text format. The data is then extracted using MATLAB and saved as data matrices for statistical analysis during the data processing stage. The netlists are simulated using a Linux workstation with an AMD Athlon X2 processor and 4 GB memory. The simulation flow is automatically carried out and controlled by using C-shell script files.

The number of MC simulation is critical to obtain an accurate estimation that is within an engineering tolerance. The estimation error of independent simulations can be calculated using the expression \sqrt{N}/N , where N is the number of simulations. For example, the estimation errors of 1000 and 2000 simulations are 3.1 % and 2.2 % from its true value, respectively. Both of them are satisfied within an engineering tolerance of 5 % in this research. This theory will also be verified in Section 4.3.3. It is true that better accuracy can be acquired by carrying out more simulations. However, with a limited computing power constraint, a reasonable simulation number should be selected for a given circuit topology. In this thesis, 2000 MC simulations will be carried out for the circuit-level compensation schemes in Chapter 4 and 5. For the system-level ADC, as the size of the circuit is significantly increased, only 1000 simulations will be carried out to investigate the performance degradation due to device variability.

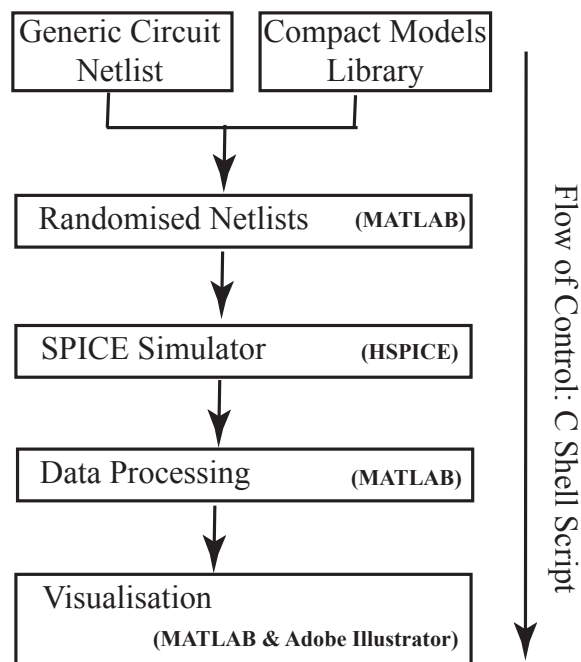


Figure 3.3 The Monte-Carlo simulation flow chart.

3.2 Short-Channel Device Mismatch Model

3.2.1 Saturation Regime

For the UDSM technology processes, one of the most important short-channel effects is known as the velocity saturation. Carrier mobility will approach a saturated velocity (v_{sat}) when the source-drain voltage (V_{DS}) is high enough to create a critical field strength $E_c = V_{DS,sat}/L$, where $V_{DS,sat}$ represents the drain voltage value when velocity saturation occurs. Therefore, unlike long-channel devices whose drain current goes into the saturation regime at the point defined by $V_{DS} = V_{GS} - V_{TH}$, for short-channel UDSM devices, the drain current enters the saturation regime at a much lower current, limited by the charge carrier velocity saturation. Furthermore, the v_{sat} of the carriers can be given as $\mu_0 E_c$, where μ_0 is the low-field carrier mobility. The drain current of atomistic device in the saturation regime, when the velocity saturation occurs, is then given by:

$$\begin{aligned} I_{DS} &= v_{sat} C_{OX} W (V_{GS} - V_{TH}) \\ &= \mu_0 C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS,sat} = \beta (V_{GS} - V_{TH}) V_{DS,sat} \end{aligned} \quad \text{Eq. (3.1)}$$

where C_{OX} is the gate oxide capacitance per unit area, W and L are the effective width and length of device. Furthermore, the current factor β is defined as $\mu_0 C_{OX} W/L$. It is noted that β and V_{TH} are the only process-related parameters in Eq. (3.1) that are suitable to describe the mismatch between devices. Furthermore, the variances of $\Delta\beta$ and ΔV_{TH} between nominally identical transistors have a direct relationship to the electrical performance mismatch that includes ΔI_{DS} and ΔV_{GS} . Drain current mismatch ΔI_{DS} is the current difference between two nominally identical devices under same biasing conditions, as shown in Figure 3.1 (a) and Figure 3.2 (a). After Taylor expansion of Eq. (3.1) to the first derivative term, the ΔI_{DS} is expressed as:

$$\begin{aligned} \Delta I_{DS} &= \frac{\partial I_{DS}}{\partial \beta} \Delta\beta + \frac{\partial I_{DS}}{\partial V_{TH}} \Delta V_{TH} \\ &= (V_{GS} - V_{TH}) V_{DS,sat} \cdot \Delta\beta - \beta V_{DS,sat} \cdot \Delta V_{TH} \end{aligned} \quad \text{Eq. (3.2)}$$

It is noted in Eq. (3.2) that ΔI_{DS} is not only related to $\Delta\beta$ and ΔV_{TH} , but also is a function of the V_{GS} . The drain current mismatch between a given nominally identical transistor pair

could also be changed by V_{GS} . Therefore, the ΔI_{DS} is normalised using its absolute value I_{DS} that can be used to estimate the drain current mismatch for a given transistor pair at a determined operational point where V_{GS} is fixed. The normalised drain current mismatch expression is developed as:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \beta}{\beta} - \frac{1}{(V_{GS} - V_{TH})} \Delta V_{TH} \quad \text{Eq. (3.3)}$$

When the process statistics information of $\Delta \beta$ and ΔV_{TH} is readily available, the variance of the normalised drain current mismatch could be further expressed as:

$$\begin{aligned} \sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right) &= \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \frac{1}{(V_{GS} - V_{TH})^2} \sigma^2(\Delta V_{TH}) \\ &\quad - \frac{2}{\beta(V_{GS} - V_{TH})} \text{Cov}(\Delta \beta, \Delta V_{TH}) \end{aligned} \quad \text{Eq. (3.4)}$$

where $\text{Cov}(*)$ represents the covariance of the term within the bracket. The calculation of the covariance term will be given later in Section 3.2.4. Furthermore, as mentioned in the Section 3.1, the gate voltage mismatch ΔV_{GS} can be developed using the transconductance of the device. From Eq. (3.1), the transconductance g_m can be expressed as:

$$\frac{\partial I_{DS}}{\partial V_{GS}} = g_m = \beta V_{DS,sat} \cdot \quad \text{Eq. (3.5)}$$

Therefore,

$$\Delta I_{DS} = \beta V_{DS,sat} \cdot \Delta V_{GS} \cdot \quad \text{Eq. (3.6)}$$

Based on Eq. (3.2) and Eq. (3.6), the expression of ΔV_{GS} can be developed as:

$$\Delta V_{GS} = (V_{GS} - V_{TH}) \cdot \frac{\Delta \beta}{\beta} - \Delta V_{TH} \cdot \quad \text{Eq. (3.7)}$$

If the statistics information of $\Delta \beta$ and ΔV_{TH} are available, its variance can be obtained as:

$$\begin{aligned}\sigma^2(\Delta V_{GS}) &= (V_{GS} - V_{TH})^2 \cdot \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \sigma^2(\Delta V_{TH}) \\ &\quad - \frac{2(V_{GS} - V_{TH})}{\beta} \text{Cov}(\Delta\beta, \Delta V_{TH}).\end{aligned}\tag{Eq. (3.8)}$$

The process statistics are normally described using the mean and variance of $\Delta\beta$ and ΔV_{TH} . Their mean values are expected to be zero and their variance can be obtained from the foundry or by measuring the random variation test structures embedded on the wafer. In this research, the process statistical information is obtained by simulating every BSIM4 compact model from the ensembles. After curve-fitted the plots of I_{DS}/V_{DS} of the compact models, the values of β and V_{TH} can be extracted. This device characterisation method will be introduced in detail in the Section 3.2.4.

During the design phase, according to Eq. (2.3), the variance of $\sigma^2\left(\frac{\Delta\beta}{\beta}\right)$ and $\sigma^2(\Delta V_{TH})$ are inversely-proportional to the effective size of the transistors:

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta^2}{W \cdot L}\tag{Eq. (3.9)}$$

and

$$\sigma^2(\Delta V_{TH}) = \frac{A_{V_{TH}}^2}{W \cdot L},\tag{Eq. (3.10)}$$

where A_β and $A_{V_{TH}}$ are technology related constants. Therefore, the variances of drain current mismatch and gate voltage mismatch in saturation regime expressed in Eq. (3.4) and Eq. (3.8) can be further developed as a function of transistor sizes and operation point (determined by V_{GS}):

$$\begin{aligned}\sigma^2\left(\frac{\Delta I_{DS}}{I_{DS}}\right) &= \frac{A_\beta^2}{W \cdot L} + \frac{1}{(V_{GS} - V_{TH})^2} \cdot \frac{A_{V_{TH}}^2}{W \cdot L} \\ &\quad - \frac{2}{\beta(V_{GS} - V_{TH})} \text{Cov}(\Delta\beta, \Delta V_{TH})\end{aligned}\tag{Eq. (3.11)}$$

and

$$\begin{aligned}\sigma^2(\Delta V_{GS}) &= (V_{GS} - V_{TH})^2 \cdot \frac{A_\beta^2}{W \cdot L} + \frac{A_{V_{TH}}^2}{W \cdot L} \\ &\quad - \frac{2(V_{GS} - V_{TH})}{\beta} \text{Cov}(\Delta\beta, \Delta V_{TH}).\end{aligned}\tag{Eq. (3.12)}$$

3.2.2 Triode Regime

The mismatch model in the triode regime has received much less attention compared with the case in saturation. This is mainly because most long-channel transistors are designed to work in the saturation regime as the supply voltage can provide enough voltage swing overhead. However, as the device size and supply voltage has scaled downwards, the threshold voltage is not proportionally scaled. The voltage swing overhead is reduced making cascode design more difficult to be applied when using small geometry devices. Some transistors are inevitably forced to work in triode regime. Therefore, device mismatch modelling in triode regime is becoming increasingly important.

The drain current expression of an atomistic device in the triode regime is given as:

$$I_{DS} = \beta \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} . \quad \text{Eq. (3.13)}$$

Similar to the case in the saturation regime, the drain current mismatch can be developed by using a Taylor expansion as a function of $\Delta\beta$ and ΔV_{TH} :

$$\Delta I_{DS} = \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} \cdot \Delta\beta - \beta V_{DS} \cdot \Delta V_{TH} . \quad \text{Eq. (3.14)}$$

It can be further normalised as:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta\beta}{\beta} - \frac{1}{\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right)} \cdot \Delta V_{TH} \approx \frac{\Delta\beta}{\beta} - \frac{1}{(V_{GS} - V_{TH})} \cdot \Delta V_{TH} . \quad \text{Eq. (3.15)}$$

where $1/2V_{DS}$ is neglected as the typical value of $V_{DS,sat}$ will be around 0.3 V in this work and V_{DS} at any point in the triode regime therefore is less 0.3 V. The overdrive voltage $(V_{GS} - V_{TH})$ is normally much higher than $1/2V_{DS}$. Furthermore, the gate voltage mismatch ΔV_{GS} can be similarly developed using the transconductance of the device in the triode regime and is given by:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta V_{DS} . \quad \text{Eq. (3.16)}$$

Therefore the gate voltage mismatch ΔV_{GS} can be developed from Eq. (3.14) and Eq. (3.16) as:

$$\Delta V_{GS} = \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) \frac{\Delta \beta}{\beta} - \Delta V_{TH} \approx (V_{GS} - V_{TH}) \frac{\Delta \beta}{\beta} - \Delta V_{TH}. \quad \text{Eq. (3.17)}$$

It is interesting to observe that the drain current mismatch ΔI_{DS} has the same expression in both the saturation and the triode regime (Eq. (3.3) and Eq. (3.15)) for short-channel devices. This is also true for the gate voltage mismatch expressions ΔV_{GS} (Eq. (3.7) and Eq. (3.17)). Therefore the variations of ΔI_{DS} and ΔV_{GS} would have the same expressions as Eq. (3.11) and Eq. (3.12) in the triode regime. Mismatch estimation can be easily carried out in both regimes by using one expression, when the process statistics and transistor size information are available.

3.2.3 Drain Current Decrease Due to Mobility Degradation

Another important short-channel effect that introduces a great imperfection on UDSM technologies is known as the mobility degradation. The mobility of carriers will begin to drop if the gate voltage (governing the perpendicular electric field) is much higher than the drain-source voltage (governing the lateral electric field). In this thesis, the typical criterion of this phenomenon occurring is $V_{GS} - V_{DS} > 0.7 V$. Therefore, the expression of the mobility degradation will be added to the drain current expressions in both triode and saturation regimes to account for its contribution.

To account its contribution, the mobility degradation is introduced by replacing the low-field carrier mobility μ_0 in Eq. (3.1) and Eq. (3.13) with an effective carrier mobility μ_{eff} , given by:

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \approx \mu_0[1 - \theta(V_{GS} - V_{TH})], \quad \text{Eq. (3.18)}$$

where the fitting parameter θ is called the mobility degradation factor with a typical value of $0.27 V^{-1}$. From the expression Eq. (3.18), it is clear that μ_{eff} will be reduced if the gate voltage is increased. Furthermore, the drain current expressions in both the saturation and triode regimes can be re-written as:

$$I_{DS} = \beta[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})V_{DS,sat} \quad \text{Eq. (3.19)}$$

and

$$I_{DS} \approx \beta[1 - \theta(V_{GS} - V_{TH})] \left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS} \right) V_{DS} \quad \text{Eq. (3.20)}$$

Following by the same strategy in the Sections 3.2.1 and 3.2.2, after Taylor expansion, the normalised drain current mismatch in the saturation and triode regimes can be expressed as a function of process related parameters to $\Delta\beta$ and ΔV_{TH} :

$$\begin{aligned} \frac{\Delta I_{DS}}{I_{DS}} &= \frac{\Delta\beta}{\beta} - \frac{\beta V_{DS}[1 - 2\theta(V_{GS} - V_{TH})]}{\beta[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})V_{DS}} \Delta V_{TH} \\ &= \frac{\Delta\beta}{\beta} - \frac{1}{[1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})} \Delta V_{TH}, \end{aligned} \quad \text{Eq. (3.21)}$$

and

$$\begin{aligned} \frac{\Delta I_{DS}}{I_{DS}} &= \frac{\Delta\beta}{\beta} - \frac{\beta V_{DS}[1 - \theta(V_{GS} - V_{TH})] - \beta V_{DS}\theta \left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS} \right)}{\beta[1 - \theta(V_{GS} - V_{TH})] \left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS} \right) V_{DS}} \\ &\approx \frac{\Delta\beta}{\beta} - \frac{1}{[1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})} \Delta V_{TH}. \end{aligned} \quad \text{Eq. (3.22)}$$

As both Eq. (3.21) and Eq. (3.22) have the same expression, the variation of drain current mismatch in both saturation and triode regimes with both saturation velocity and mobility degradation taken into account can be unified as:

$$\begin{aligned} \sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right) &= \sigma^2 \left(\frac{\Delta\beta}{\beta} \right) + \left\{ \frac{1}{[1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})} \right\}^2 \cdot \sigma^2(\Delta V_{TH}) \\ &\quad - \frac{2}{\beta} \left\{ \frac{1}{[1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})} \right\} Cov(\Delta\beta, \Delta V_{TH}) \\ &= \frac{A_\beta^2}{W \cdot L} + \left\{ \frac{1}{[1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})} \right\}^2 \cdot \frac{A_{V_{TH}}^2}{W \cdot L} \\ &\quad - \frac{2}{\beta} \left\{ \frac{1}{[1 + \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})} \right\} Cov(\Delta\beta, \Delta V_{TH}) \end{aligned} \quad \text{Eq. (3.23)}$$

The transconductance can be derived from Eq. (3.19) and Eq. (3.20) and is given by:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \beta V_{DS,sat} [1 - 2\theta(V_{GS} - V_{TH})] \quad \text{Eq. (3.24)}$$

and

$$\begin{aligned} g_m = \frac{\partial I_{DS}}{\partial V_{GS}} &= \beta V_{DS} \left\{ [1 - \theta(V_{GS} - V_{TH})] - \theta \left(V_{GS} - V_{TH} - \frac{1}{2} V_{DS} \right) \right\} \\ &\approx \beta V_{DS} [1 - 2\theta(V_{GS} - V_{TH})]. \end{aligned} \quad \text{Eq. (3.25)}$$

The gate voltage mismatch is obtained based on the ΔI_{DS} from Eq. (3.21) or Eq. (3.22) as:

$$\begin{aligned} \Delta V_{GS} &= \frac{V_{DS} [1 - \theta(V_{GS} - V_{TH})] (V_{GS} - V_{TH}) \frac{\Delta \beta}{\beta}}{V_{DS} [1 - 2\theta(V_{GS} - V_{TH})]} - \Delta V_{TH} \\ &= [1 + \theta(V_{GS} - V_{TH})] (V_{GS} - V_{TH}) \frac{\Delta \beta}{\beta} - \Delta V_{TH} \end{aligned} \quad \text{Eq. (3.26)}$$

Therefore, the variation of ΔV_{GS} with mobility taken into account is developed as:

$$\begin{aligned} \sigma^2(\Delta V_{GS}) &= \{ [1 + \theta(V_{GS} - V_{TH})] (V_{GS} - V_{TH}) \}^2 \cdot \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \sigma^2(\Delta V_{TH}) \\ &\quad - 2 [1 + \theta(V_{GS} - V_{TH})] (V_{GS} - V_{TH}) \cdot \text{Cov}(\Delta \beta, \Delta V_{TH}) \\ &= \{ [1 + \theta(V_{GS} - V_{TH})] (V_{GS} - V_{TH}) \}^2 \cdot \frac{A_\beta^2}{W \cdot L} + \frac{A_{V_{TH}}^2}{W \cdot L} \\ &\quad - 2 [1 + \theta(V_{GS} - V_{TH})] (V_{GS} - V_{TH}) \cdot \text{Cov}(\Delta \beta, \Delta V_{TH}) \end{aligned} \quad \text{Eq. (3.27)}$$

So far, the expressions of $\sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right)$ and $\sigma^2(\Delta V_{GS})$ have been developed in both triode and saturation regimes as a function of transistor effective sizes and the operational point. As the velocity saturation occurs when V_{DS} reaches around 0.3 V for 35 nm CMOS, the $1/2 V_{DS}$ term in the triode regime drain current expression is neglected. Consequently, the expressions for $\frac{\Delta I_{DS}}{I_{DS}}$ and ΔV_{GS} are the same in both triode and saturation regimes.

Furthermore, when the perpendicular field is much higher than lateral field, $V_{GS} - V_{DS} > 0.7$ V in this thesis, mobility degradation is taken into consideration. It is more likely to happen in the triode regime, as the drain-source voltage V_{DS} is relatively low. Therefore, updated expressions of $\sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right)$ and $\sigma^2(\Delta V_{GS})$ have developed by adding a fitting parameter θ to the effective mobility term, and given in Eq. (3.23) and Eq. (3.27).

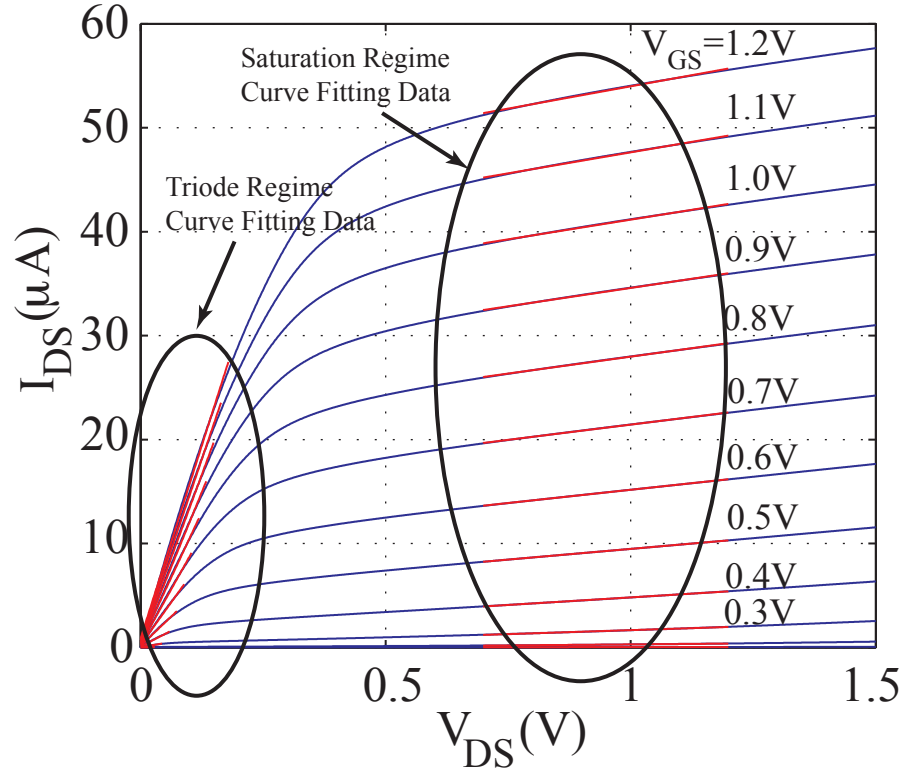


Figure 3.4 The output characteristic curves of a typical 35 nm NMOS transistor with $W = L = 35$ nm. The blue lines are simulation data. The red lines are curve fitted data.

3.2.4 Device Characterisation

Device characterisation is conventionally carried out by measuring the device current-voltage (I/V) curves from the random variation test structures embedded on a fabricated wafer and using curve-fitting to extract the statistical parameters of the device. In this research, these I/V curves are obtained from HSPICE simulations using the BSIM4 model card library instead. A novel parameter extraction technique has been developed to obtain all the parameters for short-channel devices. Mobility degradation factor θ , threshold voltage V_{TH} , low field carrier mobility μ_0 and channel length modulation factor λ can be extracted using the same data set. Compared with the conventional methodology that uses input characteristics curves (I_{DS}/V_{GS}) to extract mismatch model parameters, device output characteristic curves (I_{DS}/V_{DS}) were used in this Thesis. This is mainly because the mobility degradation occurs within triode regime that can be clearly defined using an I_{DS}/V_{DS} plot. Furthermore, channel length modulation factor can also be obtained from the same data set. The extraction procedures are introduced below.

As mobility degradation normally occurs when V_{GS} is much higher than V_{DS} , it is highly likely that it will happen in the triode regime where V_{DS} is relatively small. Therefore, the drain current expression in the triode regime is used to extract the parameters of θ , β and V_{TH} . As mentioned in Eq. (3.20), the drain current in the triode regime can be expressed as:

$$\begin{aligned} I_{DS} &= \beta[1 - \theta(V_{GS} - V_{TH})] \left(V_{GS} - V_{TH} - \frac{1}{2}V_{DS} \right) V_{DS} \\ &\approx \beta[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH})V_{DS}. \end{aligned} \quad \text{Eq. (3.28)}$$

It is noted that I_{DS} and V_{DS} have a linear relationship. Their coefficient is a quadratic function of V_{GS} :

$$\begin{aligned} f_1(V_{GS}) &= \beta[1 - \theta(V_{GS} - V_{TH})](V_{GS} - V_{TH}) \\ &= -\beta\theta V_{GS}^2 + \beta(2\theta V_{TH} + 1)V_{GS} - \beta(\theta V_{TH}^2 + V_{TH}). \end{aligned} \quad \text{Eq. (3.29)}$$

It is further noted that $f_1(V_{GS})$ is the slope values of I_{DS}/V_{DS} curves in triode regime, as shown in red fitting lines in Figure 3.4. Therefore, the $f_1(V_{GS})$ can be extracted as a function of V_{GS} . Noted that $f_1(V_{GS})$ has a format of $y = -ax^2 + bx - c$, the three coefficients of $f_1(V_{GS})$ can be defined as:

$$a = \beta\theta, \quad \text{Eq. (3.30)}$$

$$b = \beta(2\theta V_{TH} + 1), \quad \text{Eq. (3.31)}$$

$$c = \beta(\theta V_{TH}^2 + V_{TH}). \quad \text{Eq. (3.32)}$$

Based on the collected data sets, all the parameters can be calculated using a, b and c as:

$$\beta = \sqrt{b^2 - 4ac}, \quad \text{Eq. (3.33)}$$

$$V_{TH} = \frac{b - \sqrt{b^2 - 4ac}}{2a}, \quad \text{Eq. (3.34)}$$

$$\theta = \frac{a}{\beta}. \quad \text{Eq. (3.35)}$$

In the saturation regime, the current keeps increasing after the device current saturated due to a finite output resistance. A common approach for modelling this phenomenon is to add a channel length modulation term $(1 + \lambda V_{DS})$ into the saturation expression:

$$I_{DS} = \beta(V_{GS} - V_{TH})V_{DS,sat} \cdot (1 + \lambda V_{DS}) . \quad \text{Eq. (3.36)}$$

Note that, for a given V_{GS} , I_{DS} and V_{DS} have a linear relationship in the saturation regime, as shown in Figure 3.4. The coefficient of the Eq. (3.36) can be expressed as:

$$f_2(V_{GS}) = \lambda\beta V_{DS,sat}(V_{GS} - V_{TH}) . \quad \text{Eq. (3.37)}$$

This coefficient represents the slope of output characteristics in the saturation regime and it is obtained by fitting the I_{DS}/V_{DS} data as plotted in red in the Figure 3.4. Furthermore, the coefficient is also proportional to V_{GS} as well with a ratio of $\lambda\beta V_{DS,sat}$. Therefore, the $f_2(V_{GS})$ can be estimated using the curve fitting data in saturation regime, as shown in the Figure 3.4. Since β has been obtained using the data in the triode regime as shown above, λ is straightforward obtained as a typical value of $V_{DS,sat}$ is 0.3 V. The parameter extraction procedures introduced above have been applied to every single BSIM4 model card in the ensembles. With a total number of 200, each model that represents a real microscopic device would have a set of fitted parameters, including: current factor β , threshold voltage V_{TH} , mobility degradation parameter θ and channel length modulation factor λ . The statistical data of β , V_{TH} and their product βV_{TH} for 200 devices of both NMOS and PMOS are listed below in Table 3.1. The βV_{TH} is used to calculate the covariance term:

$$\begin{aligned} Cov(\Delta\beta, \Delta V_{TH}) &= \mu(\Delta\beta \Delta V_{TH}) - \mu(\Delta\beta)\mu(\Delta V_{TH}) \\ &= 2\mu(\beta V_{TH}) - 2\mu(\beta)\mu(V_{TH}), \end{aligned} \quad \text{Eq. (3.38)}$$

where $\mu(*)$ represents the expectation calculation. It is noted that θ and λ vary between devices. With typical values of 0.28 and 0.143, the variations of both of θ and λ have a minor impact when taken into the terms of $1 - \theta(V_{GS} - V_{TH})$ and $1 + \lambda V_{DS}$. Therefore, they are treated as constants in this thesis.

Table 3.1 Statistical data from the 35 nm NMOS/PMOS transistors.

	$V_{TH}(\text{mV})$	$\beta (\text{F/sV})$	$\beta V_{TH} (\text{A})$
Mean	255/243	$2.19 \times 10^{-4} / 8.89 \times 10^{-5}$	$5.59 \times 10^{-5} / 2.15 \times 10^{-5}$
Standard Deviation	38.6/32	$5.9 \times 10^{-6} / 6.17 \times 10^{-6}$	---

3.2.5 Simulation Results

The Monte Carlo simulations have been carried out to obtain the standard deviation of ΔV_{GS} at different biasing points, as shown in Figure 3.5. During the simulation, the size of transistors are selected to be $W = L = 35$ nm. It is clear that mobility degradation manifests itself when $V_{GS} - V_{DS} > 0.7$ V. Additionally, the source-drain resistance also has a finite impact in UDSM regimes, for convenience its contribution is counted using the expression of mobility degradation. On the other hand, the results from the analytical analysis of ΔV_{GS} based on Eq. (3.12) and Eq. (3.27) have been calculated and compared with the MC method, as shown in Figure 3.6 and Figure 3.7. Excellent agreements between the two approaches have been achieved at different device sizes. In Figure 3.6, the drain-source voltage V_{DS} is 0.1 V, which is lower than $V_{DS,sat}$. Therefore, the device is in triode regime. In Eq. (3.17), the term $V_{DS}/2$ in the triode regime has been neglected due to its minor impact on the standard deviation of ΔV_{GS} , which has been confirmed in Figure 3.6. The figure has shown the differences of estimations of $\sigma(\Delta V_{GS})$ with and without the $V_{DS}/2$ term. It can be observed that only a minor error has been introduced to the estimation after neglecting of the term. Meanwhile, the advantage of neglecting the term is that a unified expression can be obtained to estimate the $\sigma(\Delta V_{GS})$ in both triode and saturation regimes. Due to the mobility degradation, Eq. (3.12) has been used when $V_{GS} < 0.8$ V whilst Eq. (3.27) is

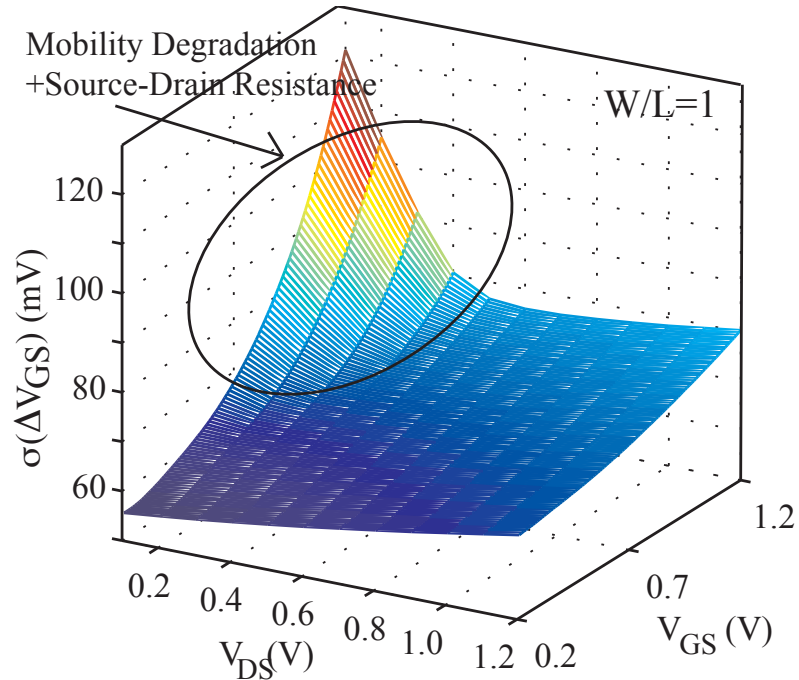


Figure 3.5 A plot of the standard deviation of NMOS gate voltage mismatch ΔV_{GS} obtained by Monte Carlo simulation method. Each data point is based on a standard deviation of 40000 simulation results. The device has a width ratio of $W/L = 1$. The results are dramatically increased when $V_{GS} - V_{DS} > 0.7$ V occurs.

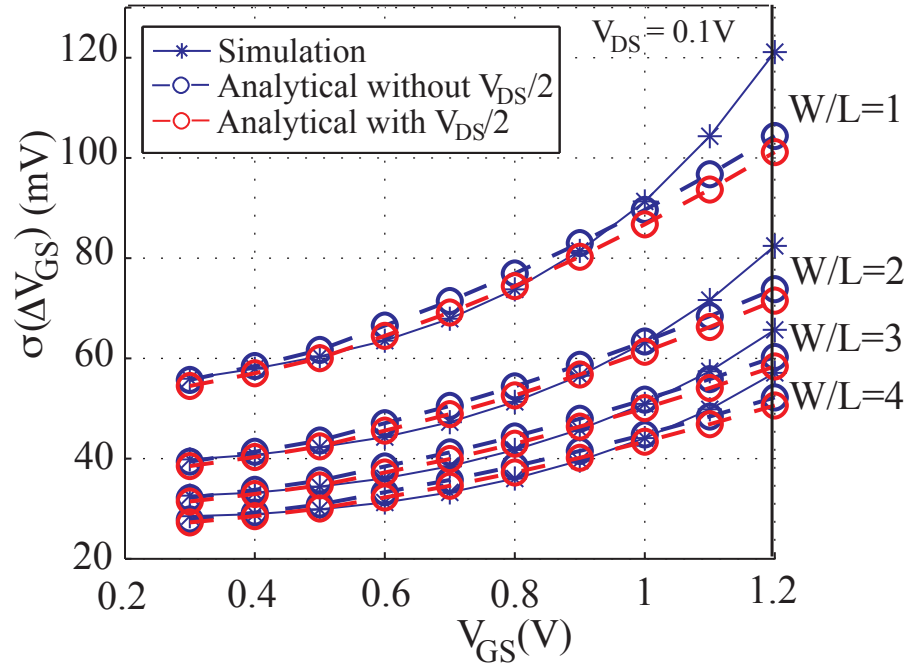


Figure 3.6 A plot of the standard deviation of NMOS gate offset voltage ΔV_{GS} in the triode regime obtained by Monte Carlo simulations and proposed analytical model for different width ratios. In this simulation $V_{DS} = 0.1 \text{ V}$, when $V_{GS} > 0.8 \text{ V}$, the standard deviations dramatically increases due to mobility degradation. The differences with and without $V_{DS}/2$ have been plotted using circle with dashed lines.

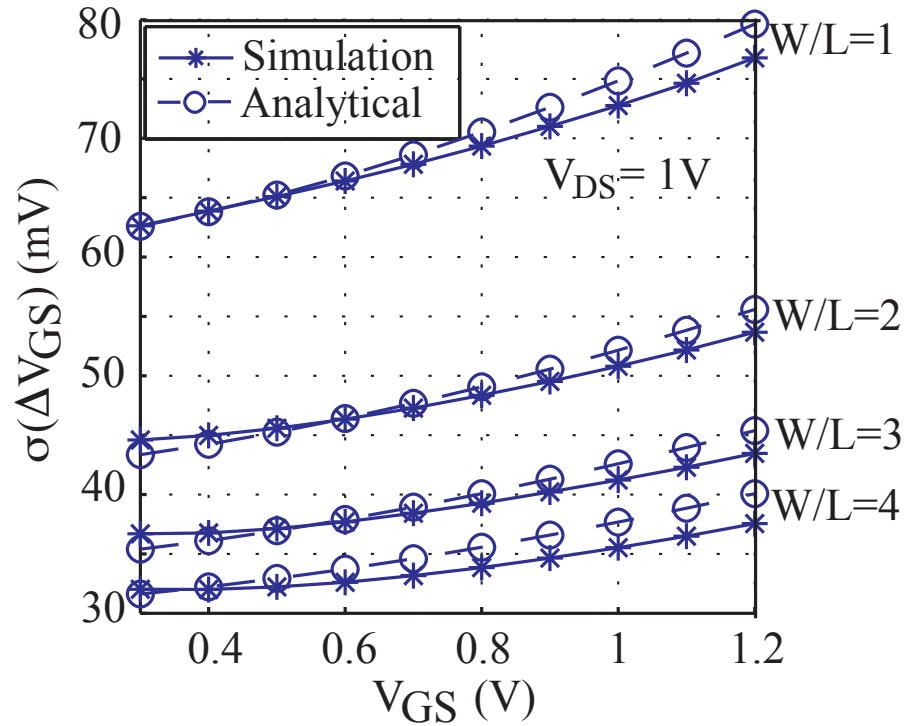


Figure 3.7 A plot of the standard deviation of NMOS gate offset voltage ΔV_{GS} in saturation regime obtained by Monte Carlo simulations and proposed analytical model for different width ratios. In this simulation $V_{DS} = 1 \text{ V}$, therefore the results are free from the impact of mobility degradation.

used when $V_{GS} > 0.8$ V. A smooth boundary is obtained between these two expressions. In Figure 3.7, V_{DS} is selected to be 1 V where the mobility degradation is not taken into account, only Eq. (3.12) is used. From the analytical mismatch model of Eq. (3.12) and Eq. (3.27), it can be observed that that the standard deviation of ΔV_{GS} would (a) be reduced when the transistor size increases and (b) increases as if gate voltage is increased. These observations have been confirmed the MC method, as shown in Figure 3.6 and Figure 3.7.

3.3 Long-Channel Device Mismatch Model

Well documented in most textbooks, the long-channel device drain current equation is the most widely used mathematical description for analysing and designing MOSFET devices in analogue circuit design. It has also used to develop mismatch models for evaluating long-channel devices matching performances as well. However, due to the increased short-channel effects, the accuracy of estimations using the long-channel equation and its mismatch model are not adequate to be applied to the UDSM devices. In this section, the previously published mismatch model that was based on the long-channel drain current equation will be briefly reviewed. The corresponding parameter extraction method is applied to the BSIM4 model library as well. More importantly, the estimation results with Monte Carlo simulation data will be compared at the end of this section.

3.3.1 Saturation Regime

The long-channel drain current equation is a quadratic function of the over-drive voltage ($V_{GS} - V_{TH}$), given by:

$$I_{DS} = \frac{1}{2} \beta (V_{GS} - V_{TH})^2 \quad \text{Eq. (3.39)}$$

where I_{DS} is the drain-source current, β is the current factor that can be further expanded as $\mu_0 C_{OX} \frac{W}{L}$, μ_0 represents carrier mobility, C_{OX} is the oxide capacitance per unit area, W and L are the effective width and length of the gate, respectively, V_{GS} is the gate-source voltage and V_{TH} is the threshold voltage. The drain current mismatch ΔI_{DS} due to the device variability can be expressed as a function of $\Delta \beta$ and ΔV_{TH} using a Taylor expansion to the first derivative term:

$$\begin{aligned}
\Delta I_{DS} &= \frac{\partial I_{DS}}{\partial \beta} \Delta \beta + \frac{\partial I_{DS}}{\partial V_{TH}} \Delta V_{TH} \\
&= \frac{1}{2} (V_{GS} - V_{TH})^2 \cdot \Delta \beta - \beta (V_{GS} - V_{TH}) \cdot \Delta V_{TH}
\end{aligned}
\tag{Eq. (3.40)}$$

where $\Delta \beta$ and ΔV_{TH} are the differences between two nominally identical transistors. A normalised expression of drain current mismatch ΔI_{DS} is developed by dividing Eq. (3.40) with Eq. (3.39):

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \beta}{\beta} - \frac{2}{(V_{GS} - V_{TH})} \Delta V_{TH}
\tag{Eq. (3.41)}$$

The ratio of drain current mismatch and gate voltage mismatch is the transconductance of the device, given by:

$$\frac{\partial I_{DS}}{\partial V_{GS}} = \beta (V_{GS} - V_{TH}),
\tag{Eq. (3.42)}$$

whilst the gate voltage mismatch ΔV_{GS} is obtained from Eq. (3.40) and Eq. (3.42) as:

$$\Delta V_{GS} = \frac{V_{GS} - V_{TH}}{2\beta} \Delta \beta - \Delta V_{TH}
\tag{Eq. (3.43)}$$

Both ΔI_{DS} and ΔV_{GS} have a mean of zero. The variances of Eq. (3.41) and Eq. (3.43) can be expressed as:

$$\begin{aligned}
\sigma^2 \left(\frac{\Delta I_{DS}}{I_{DS}} \right) &= \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \frac{4}{(V_{GS} - V_{TH})^2} \sigma^2 (\Delta V_{TH}) \\
&\quad - \frac{4}{\beta (V_{GS} - V_{TH})} \text{Cov}(\Delta \beta, \Delta V_{TH}) \\
&= \frac{A_\beta^2}{W \cdot L} + \frac{4}{(V_{GS} - V_{TH})^2} \frac{A_{V_{TH}}^2}{W \cdot L} - \frac{4}{\beta (V_{GS} - V_{TH})} \text{Cov}(\Delta \beta, \Delta V_{TH})
\end{aligned}
\tag{Eq. (3.44)}$$

and

$$\begin{aligned}
\sigma^2 (\Delta V_{GS}) &= \frac{(V_{GS} - V_{TH})^2}{4} \sigma^2 \left(\frac{\Delta \beta}{\beta} \right) + \sigma^2 (\Delta V_{TH}) \\
&\quad - \frac{V_{GS} - V_{TH}}{\beta} \text{Cov}(\Delta \beta, \Delta V_{TH}) \\
&= \frac{(V_{GS} - V_{TH})^2}{4} \frac{A_\beta^2}{W \cdot L} + \frac{A_{V_{TH}}^2}{W \cdot L} - \frac{V_{GS} - V_{TH}}{\beta} \text{Cov}(\Delta \beta, \Delta V_{TH})
\end{aligned}
\tag{Eq. (3.45)}$$

3.3.2 Triode Regime

The drain current expressions in the triode regime for both long-channel and short-channel devices are the same, as the MOSFET behaves as a resistor with a sheet resistivity, $\rho_{sh} = 1/[\mu_{eff} C_{ox} (V_{GS} - V_{TH})]$, modulated by the gate voltage. Therefore, as derived in the

previous section, the variations of ΔI_{DS} and ΔV_{GS} are given in Eq. (3.23) and Eq. (3.27) with mobility degradation taken into consideration.

3.3.3 Device Characterisation

As mentioned in the Section 3.2.4, the conventional parameter extraction methodology is based on the input transfer curves (I_{DS}/V_{GS}) for device characterisation, as shown in Figure 3.8. From the quadratic drain current expression in Eq. (3.39), it can be further developed that:

$$\sqrt{I_{DS}} = \sqrt{\frac{\beta}{2}} (V_{GS} - V_{TH}) = \sqrt{\frac{\beta}{2}} V_{GS} - \sqrt{\frac{\beta}{2}} V_{TH}, \quad \text{Eq. (3.46)}$$

where $\sqrt{I_{DS}}$ is a linear function of V_{GS} . Since it has a format of $y = ax + b$, the coefficients a and b are given as:

$$a = \sqrt{\frac{\beta}{2}} \Rightarrow \beta = 2a^2, \quad \text{Eq. (3.47)}$$

$$b = -\sqrt{\frac{\beta}{2}} V_{TH} \Rightarrow V_{TH} = -\frac{b}{a}. \quad \text{Eq. (3.48)}$$

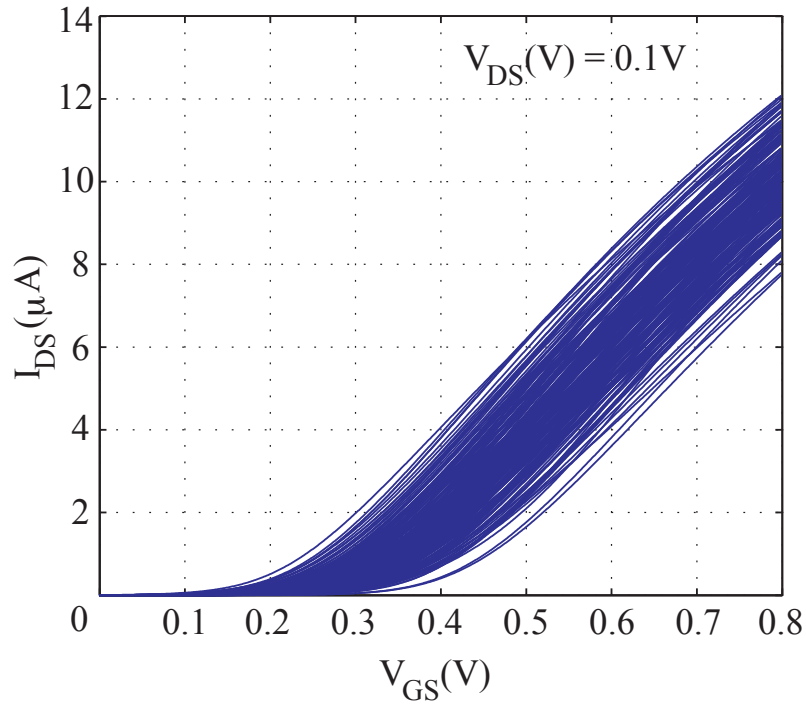


Figure 3.8 Input curves (I_{DS}/V_{GS}) of all BSIM4 model cards from the NMOS ensemble. The drain source voltage is configured to be 0.1 V, since such a voltage will reduce the channel length modulation effect.

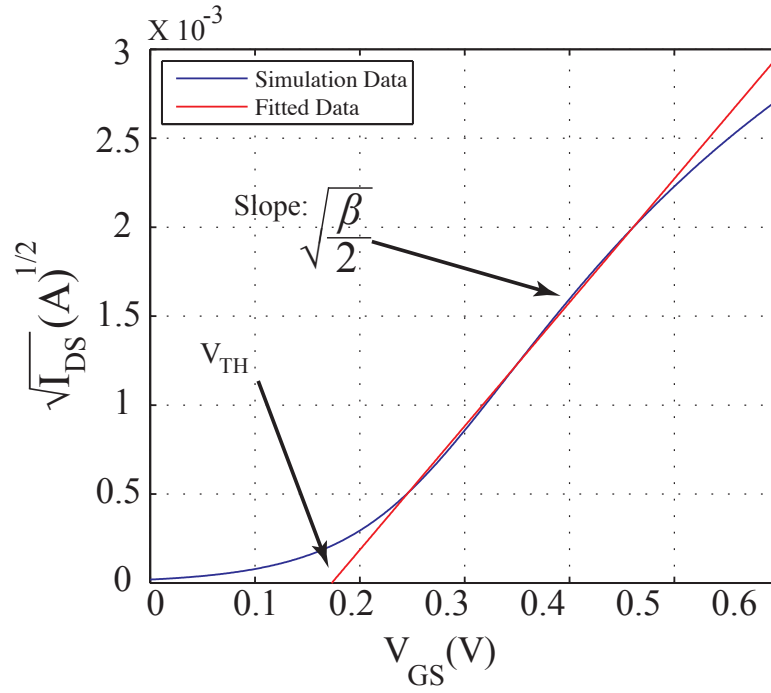


Figure 3.9 Curve fitting process for long channel device characterisation.

As shown in Figure 3.9, the square root of one randomly selected drain current curve I_{DS} is plotted against gate voltage V_{GS} in blue. The curve fitting data is plotted in red and has been optimised in a least squares sense. Current factor β can be obtained from the slope fitting parameter a . Threshold voltage V_{TH} is the cross point of fitted data and the x-axis. After applying this fitting procedure for the rest of the data from Figure 3.8, the statistical information of β and V_{TH} for the BSIM4 library are summarised in Table 3.2.

3.3.4 Simulation Results

Similar to the Section 3.2.5, the gate voltage mismatch ΔV_{GS} is used to demonstrate the accuracy between the analytical long channel mismatch model and the MC simulation results. Based on the Eq. (3.45) and the statistical data of the parameters in Table 3.2, the analytical estimations are plotted against MC simulation results in Figure 3.10 and Figure 3.11. Obviously, the long-channel mismatch model fails to provide an accurate estimation compared with the proposed model.

Table 3.2 Parameters extracted using long-channel model.

	V_{TH} (mV)	β (F/sV)	βV_{TH} (A)
Mean	166.4	1.34×10^{-4}	2.21×10^{-5}
Standard Deviation	43.4	1.25×10^{-5}	-----

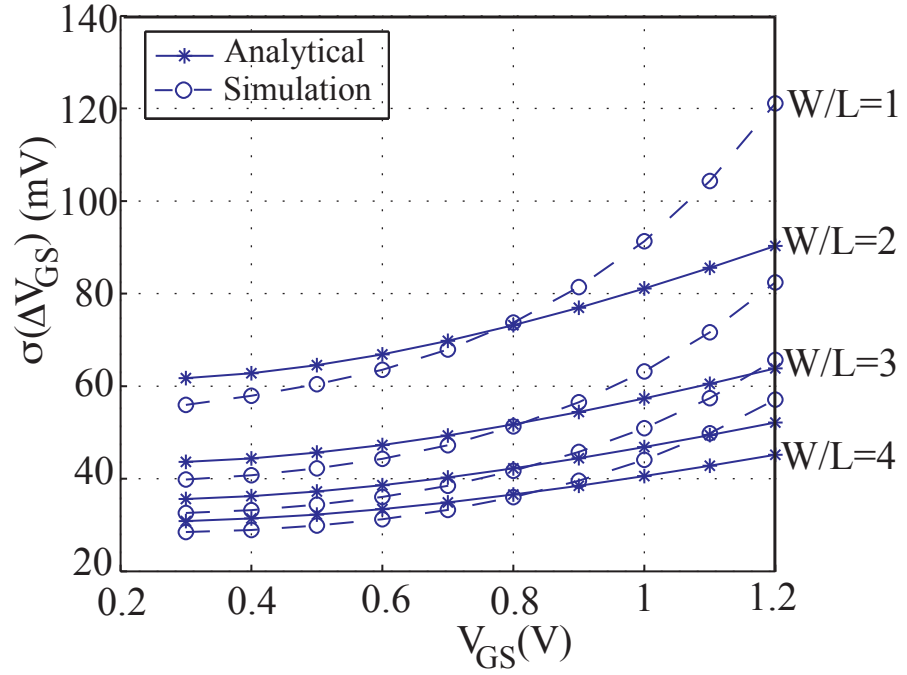


Figure 3.10 A plot of standard deviation of NMOS gate offset voltage ΔV_{GS} in the triode regime obtained by Monte Carlo simulations and the long-channel analytical mismatch model for different width ratios. The drain source voltage is set to be $V_{DS} = 0.1$ V.

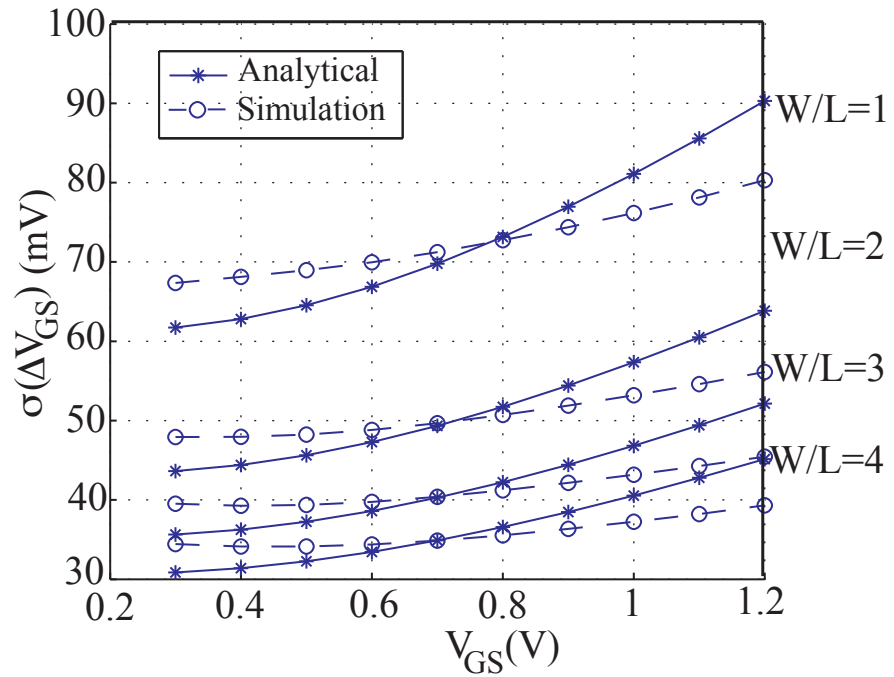


Figure 3.11 A plot of standard deviation of NMOS gate offset-voltage ΔV_{GS} in saturation regime obtained by Monte Carlo simulations and the long-channel analytical mismatch model for different width ratios. The drain source voltage is set to be $V_{DS} = 1$ V.

3.4 A Case Study: Modelling the Input Offset Voltage of A Simple Differential Pair

As discussed in the previous sections, the analytical mismatch model can reveal the fact that transistor effective sizes and device operational points are not only related to circuit power and speed, but also determines the operational accuracy of the circuit. This analytical approach is essential for circuit designers to estimate the design margins of a circuit with the impact of device variability. These design margins are critical information to show the robustness of the circuit. Furthermore, these design margins can be improved by resizing the signal path transistors, or by applying appropriate compensation circuits. A robust design, therefore, can be achieved that would significantly increase the fabrication yield and reduces the cost per chip.

In this section, a simple differential amplifier with active load will be used as an example to demonstrate how the proposed short-channel mismatch model developed in Section 3.2 can be applied in a real design scenario using UDSM devices. Furthermore, the estimation results of the proposed mismatch model will be verified using Monte Carlo simulations at the end of this section.

3.4.1 Input Referred Offset Voltage Estimation

The differential pair is a popular design that is used as the input stage of most analogue circuits. However, it is extremely vulnerable to device mismatch. The major advantages of differential pair over its single-ended alternatives include: (a) it can reject any common mode turbulence, (b) its biasing circuit is simpler, (c) it has a higher linearity and (d) it can increase the maximum achievable voltage swings. Although it will occupy twice the silicon area compared with its single-ended counterparts, this is a minor drawback during real design. On the other hand, these features can only be achieved if two branches are symmetric. An unbalanced differential pair would dramatically decrease the achievable circuit resolution, as a significant input referred offset voltage (V_{OFF}) would be introduced. The offset voltage is defined as a DC differential voltage required between two inputs to force the output zero, and is widely used as a metric to reflect the magnitude of the circuit's achievable accuracy. For example, the offset voltage of a comparator could determine the achievable value of the least significant bit (LSB), if the comparator is used as one segment

of an ADC. As V_{OFF} has a Gaussian distributing, the proposed mismatch model can extract its statistical information based on the circuit topology and process statistics. In this section, the test bench circuit used for the V_{OFF} extraction is shown in Figure 3.12. The circuit is a source-coupled differential pair (MN1 and MN2) with PMOS active load (MP1 and MP2) supplied by a 1V supply voltage. The dimensions of MN1 and MN2 are chosen to be $W/L = 35 \text{ nm}/35 \text{ nm}$ and MP1 and MP2 are $W/L = 70 \text{ nm}/35 \text{ nm}$. The PMOS transistors are wider since the mobility of electrons is around twice that of holes. The drain currents of the left and right branches are I_{DS1} and I_{DS2} , respectively. The transistor MN3 provides a biasing current for the whole circuit.

In order to mathematically estimate the magnitude of the offset voltage it is a common practice to assume that: (a) all the transistors are free from variability and the circuit is perfectly balanced and (b) the circuit mismatch only arises due to the "virtual" DC offset voltage V_{OFF} that is connected to MN1, as shown in Figure 3.12. From the circuit schematic, it is noted that when the same common mode input voltage V_{IN} is applied, the V_{OFF} will result an unwanted differential output voltage ΔV_{OUT} , given by

$$\Delta V_{OUT} = V_{OUT1} - V_{OUT2} = r_{o,P} \cdot \Delta I_{DS} = r_{o,P} \cdot \beta_N V_{DS,sat} \cdot V_{OFF} \quad \text{Eq. (3.49)}$$

where $r_{o,P}$ is the output impedance of the PMOS transistors MP1 and MP2 and $\beta_N V_{DS,sat}$ is the transconductance of MN1 and MN2.

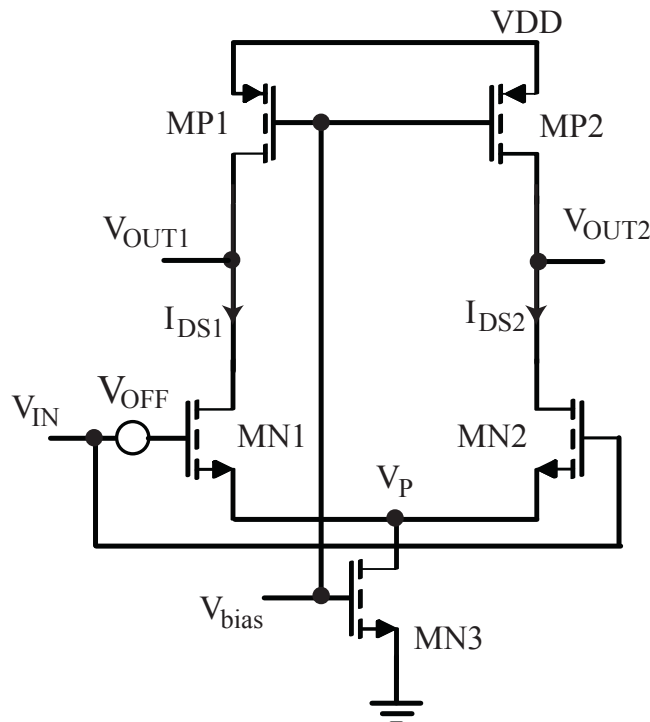


Figure 3.12 Offset voltage evaluation test bench circuit.

However, the origin of V_{OFF} is actually attributed from two parts: the mismatches between MN1-MN2 and MP1-MP2. Derived from Eq. (3.12), $V_{OFF,N}$ and $V_{OFF,P}$ are used to express the mismatch that arises from MN1-MN2 and MP1-MP2. Their variances can be expressed as:

$$\sigma^2(V_{OFF,N}) = (V_{in} - V_P - V_{TH,N})^2 \frac{A_{\beta,N}^2}{W_N L_N} + \frac{A_{TH,N}^2}{W_N L_N} - \frac{2}{\beta_N (V_{IN} - V_P - V_{TH,N})} Cov(\Delta\beta_N, \Delta V_{TH,N}) \quad \text{Eq. (3.50)}$$

and

$$\sigma^2(V_{OFF,P}) = (V_{VDD} - V_{bias} - V_{TH,P})^2 \frac{A_{\beta,P}^2}{W_P L_P} + \frac{A_{TH,P}^2}{W_P L_P} - \frac{2}{\beta_P (V_{VDD} - V_{bias} - V_{TH,P})} Cov(\Delta\beta_P, \Delta V_{TH,P}). \quad \text{Eq. (3.51)}$$

where V_P is voltage at the source of MN1 and MN2. The $V_{OFF,N}$ can be applied to the gate of MN1. However, the $V_{OFF,P}$ is the voltage difference required to be applied between the gate of MP1 and MP2, as plotted in Figure 3.13. It is noted that any gate voltage change in MP1 can be equivalent to a voltage change at the gate of MN1 by multiply the transconductance ratio between MP1 and MN1. Therefore, $V_{OFF,P}$ can be modeled as an

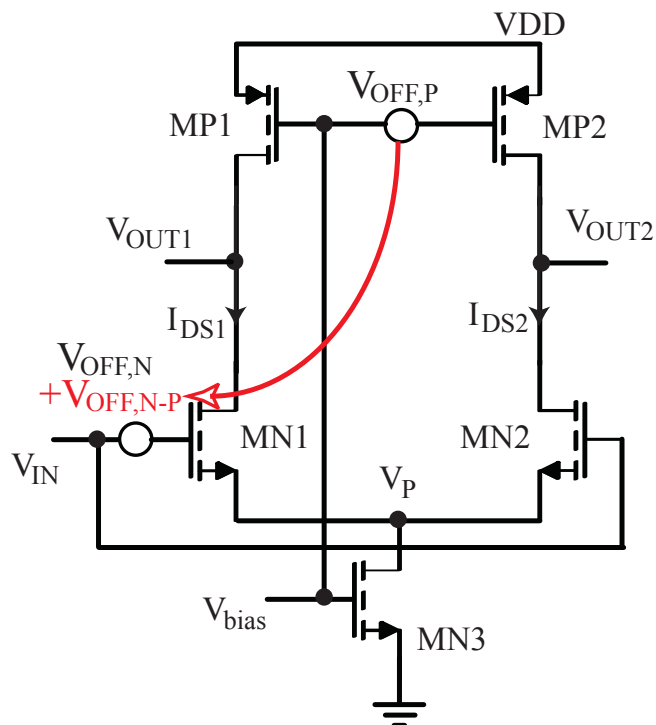


Figure 3.13 Offset voltages contributed from MN1-MN2 and MP1-MP2.

equivalent offset voltage $V_{OFF,P-N}$ at the gate of MN1 by multiplying the transconductance ratio of PMOS and NMOS, which is given by:

$$V_{OFF,N-P} = V_{OFF,P} \cdot \frac{\beta_P \cdot V_{DS,satP}}{\beta_N \cdot V_{DS,satN}}. \quad \text{Eq. (3.52)}$$

Eventually, the standard deviation of the total offset voltage V_{OFF} can then be accumulated from these two parts and derived as:

$$\begin{aligned} \sigma(V_{OFF}) &= \sqrt{\sigma^2(V_{OFF,N}) + \sigma^2(V_{OFF,N-P})} \\ &= \sqrt{\sigma^2(V_{OFF,N}) + \left(\frac{\beta_P \cdot V_{DS,satP}}{\beta_N \cdot V_{DS,satN}} \right)^2 \cdot \sigma^2(V_{OFF,P})}. \end{aligned} \quad \text{Eq. (3.53)}$$

where $\sigma^2(V_{OFF,N})$ and $\sigma^2(V_{OFF,P})$ are given in Eq. (3.50) and Eq. (3.51).

3.4.2 Simulation Verification

The Monte Carlo simulations were carried out to verify the accuracy of the derived analytical estimation in Eq. (3.53). The circuit arrangement in the Figure 3.12 was used as the circuit under test. A common mode input voltage $V_{IN} = 0.4$ V was applied to both MN1 and MN2. V_{bias} was set to be 0.58 V. Both NMOS and PMOS were taken device variability into account during the simulation. A total of 2,000 randomised netlists were generated and

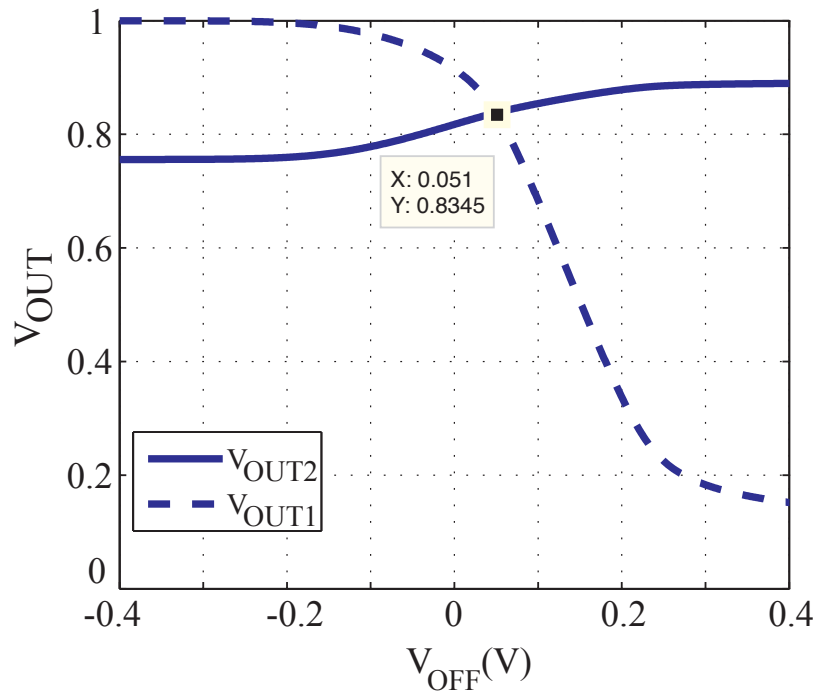


Figure 3.14 The output voltages of a randomised netlist during the V_{OFF} DC analysis.

simulated using HSPICE. DC analysis was performed for each netlist. The offset voltage V_{OFF} in Figure 3.12 was swept from -0.4 V to 0.4 V, whilst the output voltages V_{OUT1} and V_{OUT2} were observed. The output voltages of a randomised netlist are plotted in Figure 3.14. Since the $V_{IN} = 0.4$ V, when $V_{OFF} = -0.4$ V, the gate voltage of MN1 is zero. Therefore, MN1 was switched off and $V_{OUT1} = V_{DD}$, as shown in Figure 3.14. As V_{OFF} gradually increases, MN1 is switched on and draws more current flow through the left branch. Therefore, the load transistor MP1 will generate a voltage drop, which reduces the V_{OUT1} . A balanced V_{OUT1} and V_{OUT2} is achieved when $V_{OFF} = 51$ mV for this netlist, as shown in the label of the Figure 3.14. The V_{OFF} is therefore obtained.

After the measurement of 2000 netlists, the standard deviation of the offset voltage was obtained and plotted in Figure 3.15. The experiment was also repeated for different width ratios of the circuit. As expected, the offset voltage was decreased as the width getting larger. Furthermore, the MC simulations were carried out when taking only NMOS variability or PMOS variability into consideration by setting the rest transistors to be ideal. Based on the proposed mismatch model, analytical analysis of the offset voltage has achieved excellent agreement with the MC simulation results. Compared with the MC method, the analytical method can further provide a quick estimation of the offset voltage without large simulations. Furthermore, this method can be extended to be applied to larger multiple stage operational amplifier circuits as well.

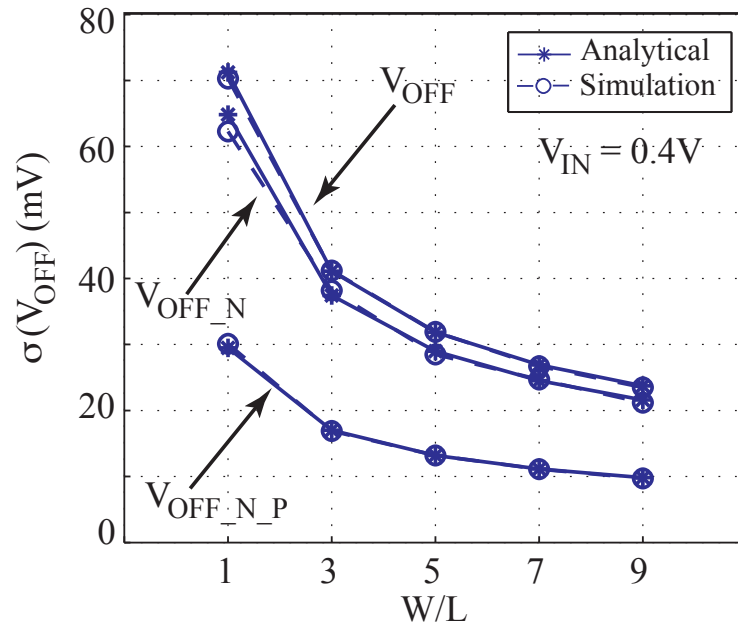


Figure 3.15 The comparison between simulation results and analytical estimations of the diff-amp offset voltage standard deviation. Multiple width ratios are tested.

3.5 Summary

The device mismatch problem has plagued analogue circuit design over decades, as the operational precision is one of most important specifications that analogue designers want to achieve. A quantitative estimation of mismatch is desirable by using an analytical model with the process statistics. Not only can the model be used to estimate the yield of the circuit, it can also provide insights on how to reduce circuit mismatches when design decisions are made. Moreover, using the estimated mismatch information, appropriate compensation circuits or techniques can be used to improve the operation precision as well.

In this chapter, a novel analytical mismatch model for UDSM transistors under the impact of intrinsic device variability has been proposed. Major short-channel effects, such as mobility degradation and velocity saturation, are accounted in the model for the first time. Furthermore, it is noted that the drain current mismatch ΔI_{DS} and gate mismatch voltage ΔV_{GS} in both the triode and saturation regimes can be expressed using the same equation whether or not mobility degradation is taken into account. It is also observed that mobility degradation has a significant contribution to mismatch only when $V_{GS} - V_{DS} > 0.7$ V.

A comparison between the proposed model and a conventional long-channel mismatch model was made. Without considering short-channel effects, the long-channel mismatch model cannot provide an adequate estimation during circuit analysis and design. A case study of how the proposed model can be used during the real design scenario was presented as well. For a differential amplifier with an active load, the input offset voltage, a measure of circuit mismatch, was mainly introduced due to the mismatch between load transistors MP1 and MP2 and input differential pair MN1 and MN2. Based on the proposed model, excellent estimations were obtained and verified using Monte Carlo simulations. The proposed analytical mismatch model provides designers clear design indications on how to minimise the impact of process variation during the design phase, before committing to silicon fabrication. It can also avoid time consuming MC simulations that is especially important for large analogue circuits and systems. In the next chapter, transistor level compensation techniques will be discussed based on the knowledge of the magnitude of the device mismatch.

Chapter 4 Compensation

Schemes at Transistor Level

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4.1 Transistor Level Compensation

As the device feature size approaching the achievable precision limits of the fabrication machinery, the statistical device variability significantly increases the physical variations between the fabricated identically-designed devices, such as their shapes of the gates, active-area doping concentrations and landscapes of silicon dioxide. A couple of transistor-level solutions have been developed and are widely used by circuit designers to overcome the impact from above the imperfections. The solutions are derived based on the fact that the electrical performance of MOSFET devices is not only related to the physical characteristics, but also the biasing conditions of the transistor. As the MOSFET is a four terminal device, each terminal can potentially become an adjustment knob that can be used to overcome the physical device variations and to achieve a matched drain current for a nominally identical transistor pair.

Therefore, four different approaches can be developed to compensate the device variability at transistor-level that can be further categorised into two kinds by their cause in the drain expression: (a) over-drive voltage related method and (b) output resistance related method. The over-drive voltage of a transistor, defined as $(V_{GS} - V_{TH})$, is the most straightforward way to control the drain current, which is controlled by the gate and the bulk voltages of the transistor. The gate voltage is reflected by the magnitude of V_{GS} in the expression. Meanwhile, the bulk voltage can be indirectly controlled using the V_{TH} due to the body effect phenomenon of the transistor. The output resistance related method is implemented by manipulating the drain-source voltage V_{DS} . As a MOSFET device has finite output resistance, the drain voltage can be used to compensate the unbalanced transistors to achieve the same drain currents. Last but not least, the source terminal is normally regarded as a reference point of voltage measurements from all other terminals. This makes the source terminal compensation as the most efficient transistor-level approach out of all other terminals.

It should be pointed out that the above engineering solutions have limitations. These approaches work perfectly on the targeted static operational point. However, the fixed compensation voltage cannot lead to a perfect matching over the whole range of voltage swing. A small gain error still exists for the rest of the operational regimes. This problem arises because β and V_{TH} are partly correlated as they share some common source of variability origins. This two-dimension problem space cannot be simply solved by using

one fixed solution. The small gain error could be potentially further amplified if multiple stages are used. Therefore, the introduced techniques should be used carefully to maintain a satisfactory outcome that meets the requirements of design specifications.

In this chapter, the basic principle of each scheme will be discussed in detail. The compensation efficiencies of all terminals will be compared. Gain error limitation will be further explained and demonstrated using simulation results. Furthermore, three novel compensation schemes based on body-biasing, drain compensation and source compensation will be proposed. Their performances will be evaluated using HSPICE simulations with the BSIM4 model card library.

4.1.1 Principles of Transistor Level Compensation

4.1.1.1 Over-Drive Voltage Related Methods

The principle mechanism of a MOSFET device is to manipulate the drain current using the over-drive voltage ($V_{GS} - V_{TH}$) when other terminal voltages are biased to appropriate voltages. Changing the gate voltage is an efficient and straightforward method to overcome the device mismatch, as shown in Figure 4.1 (a). The required gate voltage mismatch ΔV_{GS} is used as a measurement of the magnitude of the transistor mismatch. It was derived in Chapter 3, as:

$$\Delta V_{GS} = \frac{\Delta I_{DS}}{g_m} = (V_{GS} - V_{TH}) \cdot \frac{\Delta \beta}{\beta} - \Delta V_{TH}, \quad \text{Eq. (4.1)}$$

where $\Delta \beta$ and ΔV_{TH} can reflect the physical differences between two nominally identical transistors. It is noted that the ΔI_{DS} is proportional to the ΔV_{GS} in Eq. (4.1). Therefore, an analytical estimation of ΔV_{GS} can be given if the I_{DS} and V_{GS} are readily available. For example, due to the device variability, if the drain current variation ΔI_{DS} of a transistor is $\pm 10\%$ of its absolute value I_{DS} , ΔV_{GS} would also be $\pm 10\%$ of the corresponding V_{GS} at the same point. As the value of V_{GS} should be operating between the threshold voltage (0.25 V) and the supply voltage (1 V), if it is assumed that V_{GS} is 0.6 V in the above case, the magnitude of the required ΔV_{GS} will be ± 0.06 V. This example will be further used to compare the efficiency of other terminal compensation methods for the rest of this section.

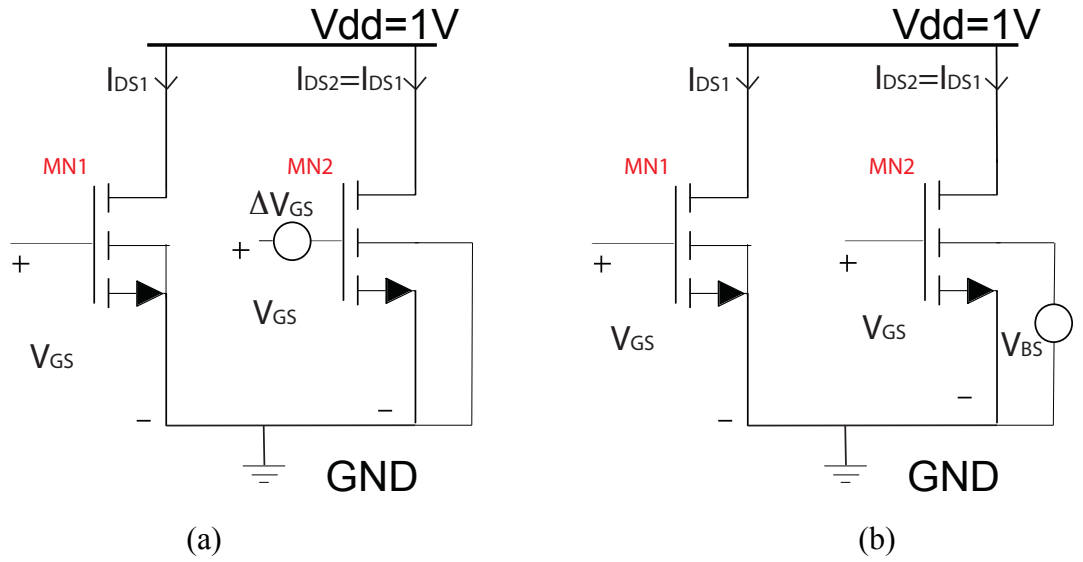


Figure 4.1 Over-drive voltage modification methods. (a) To compensate drain current mismatch by applying ΔV_{GS} at the gate of MN2. (b) To compensate drain current mismatch by applying bulk-source voltage V_{BS} that further results a change in threshold voltage.

Next, how to implement ΔV_{GS} using a circuit solution is the next challenge to tackle. The most widely used circuit implementation of gate terminal compensation is the floating-gate technology that has been introduced in Chapter 2. However, the implementation of this technology will not be discussed in this thesis. This is mainly because although it is a well-established technology that can be implemented by the foundry at an acceptable extra cost, the floating node of the circuit is difficult to simulate using a numerical simulation tool, for example HSPICE, as there is no DC path to the node. There are some existing equivalent circuits developed for simulating the floating gate device. However, these equivalent circuits are not based on the physics of the real device and are limited to evaluate certain perspectives of the floating-gate device. Furthermore, for the circuit design using atomistic devices, the gate leakage increases significantly as the oxide thickness of atomistic devices gets thinner. As a result, it is difficult for such a small geometry device to hold the charge in the floating capacitor for a long time. Therefore, the attractiveness of the floating-gate technology has reduced.

On the other hand, due to the body effect, the threshold voltage V_{TH} is a function of the bulk voltage V_{BS} when the other terminals are fixed:

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|} \right), \quad \text{Eq. (4.2)}$$

where V_{TH0} is the threshold voltage when $V_{BS} = 0$, γ represents the body effect parameter with a typical value of 0.14 and $2\Phi_F$ is the surface potential with a typical value of 0.91 V. Therefore, by changing V_{BS} , the drain current mismatch can be eliminated, as shown in

Figure 4.1 (b). Based on Eq. (4.1) and Eq. (4.2), any change in the bulk voltage will result in a drain current change ΔI_{DS} of:

$$\Delta I_{DS} = -\beta \cdot \gamma \left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|} \right). \quad \text{Eq. (4.3)}$$

Furthermore, the required bulk compensation voltage V_{BS} for compensating a drain current mismatch of ΔI_{DS} will be:

$$\begin{aligned} V_{BS} &= \left(\frac{\Delta I_{DS}}{\beta \cdot \gamma} \right)^2 - 2\sqrt{|2\Phi_F|} \cdot \frac{\Delta I_{DS}}{\beta \cdot \gamma} \\ &= \left(\frac{\Delta V_{GS}}{\gamma} \right)^2 - 2\sqrt{|2\Phi_F|} \cdot \frac{\Delta V_{GS}}{\gamma}. \end{aligned} \quad \text{Eq. (4.4)}$$

With the typical values of γ , $2\Phi_F$, it can be calculated that in order to compensate the same $\pm 10\%$ of ΔI_{DS} , the range of required for V_{BS} is ± 0.63 V. It is much higher than that of ΔV_{GS} , which is ± 0.06 V. The efficiency of body-biasing is therefore quite low compared with the gate terminal compensation. The efficiency will be further degraded as the device scales downward, as the body effect coefficient will become even smaller.

Despite the efficiency problem for a single MOSFET device, it is noted that both the input and the load transistors can be used for body biasing at the same time, in order to increase the compensation range in real design practice. In this chapter, body-biasing compensation schemes have been successfully developed by carefully designing the implementation circuitry to overcome the variability of a differential amplifier. The proposed schemes could not only be used to overcome the mismatch problem, but also can be used to adjust circuit speed and gate leakage. The schemes will be explained in detail in Section 4.2.

4.1.1.2 Output Impedance Related Methods

The ideal MOSFET is designed as a voltage-controlled current source whose output impedance is infinite. However, all real devices have a finite output impedance (r_o) that is normally modelled using channel-length modulation factor λ , and expressed using:

$$I_{DS} = \beta(V_{GS} - V_{TH})V_{DS,sat} \cdot (1 + \lambda V_{DS}). \quad \text{Eq. (4.5)}$$

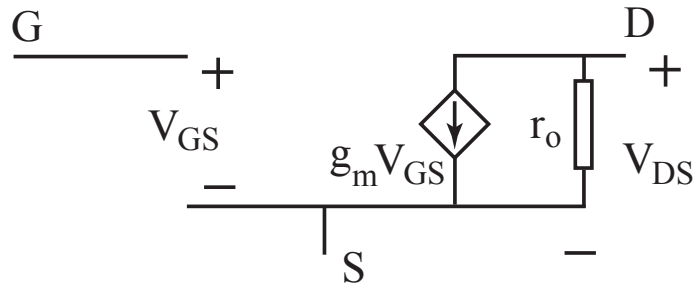


Figure 4.2 MOSFET device small signal equivalent circuit.

Figure 4.2 shows the output impedance (r_o) of a MOSFET device using a small signal equivalent circuit. The r_o will result in a drain current I_{DS} change if any modification in drain voltage V_{DS} is applied. Therefore, for the drain current mismatch of ΔI_{DS} due to device variability, the required drain compensation voltage ΔV_{DS} , as shown in Figure 4.3 (a), is given by:

$$\Delta V_{DS} = \frac{\Delta I_{DS}}{r_o} = \frac{\Delta I_{DS}}{\lambda \beta (V_{GS} - V_{TH}) V_{DS,sat}} = \frac{\Delta V_{GS}}{\lambda (V_{GS} - V_{TH}) V_{DS,sat}}. \quad \text{Eq. (4.6)}$$

Based on the typical value of $\lambda = 0.143$, the required value of ΔV_{DS} is required to compensate $\pm 10\%$ fluctuations of ΔI_{DS} is ± 5.29 V. Therefore, the drain compensation method is the most inefficient method compared with methods introduced above, as the required voltage has even exceeded the supply voltage. Therefore, less attention has been

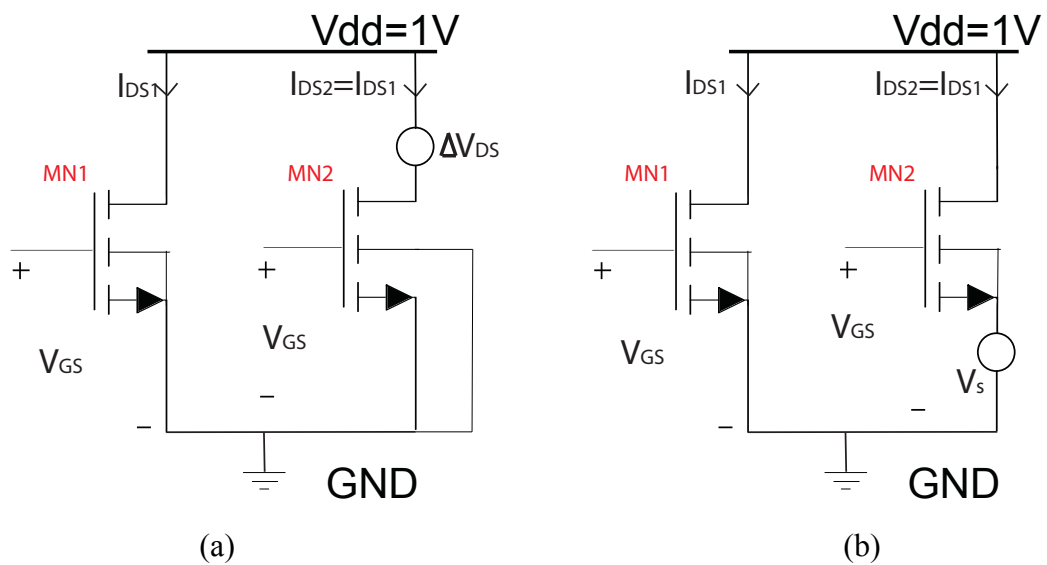


Figure 4.3 Output impedance related methods. (c) To compensate drain current mismatch by applying an additional drain-source voltage ΔV_{DS} . (d) To compensate drain current mismatch by changing the source voltage V_s .

paid to implement this idea into real design. However, this does not necessarily mean that the drain compensation approach is inapplicable. The above evaluation is based on only one single transistor. During real circuit design, the output impedance is not only related to the input transistor, but also the load transistor. Therefore, for an unbalanced differential amplifier, the drain voltage can be modified by changing the load transistor in order to achieve a balanced status. A novel compensation scheme based on drain compensation will be proposed and will be explained in detail in Section 4.3.

Last but not least, source compensation is based on the idea that all other three terminals are using the source terminal as a reference point for measurement, for example V_{GS} , V_{BS} and V_{DS} . Therefore, changing the source voltage will simultaneously change the voltage measurements of all other terminals. Therefore, it is expected to be the most efficient approach compared to the others introduced above. For example, to compensate a drain current mismatch of ΔI_{DS} with $\pm 10\%$ fluctuations when $V_{GS} = 0.6$ V, the required source compensation voltage V_S is a combination of all the voltages that have introduced above:

$$\begin{aligned}
\Delta I_{DS} &= \beta \Delta V_{GS} - \beta \cdot \gamma \left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|} \right) \\
&\quad + \lambda \beta (V_{GS} - V_{TH}) V_{DS,sat} \cdot \Delta V_{DS} \\
&= \beta V_S - \beta \cdot \gamma \left(\sqrt{|2\Phi_F - V_S|} - \sqrt{|2\Phi_F|} \right) \\
&\quad + \lambda \beta (V_{GS} - V_{TH}) V_{DS,sat} \cdot V_S
\end{aligned} \tag{4.7}$$

where $\Delta V_{GS} = V_{BS} = \Delta V_{DS} = V_S$. It is known that to compensate 10 % fluctuations of drain current mismatch of ΔI_{DS} , the required $\Delta V_{GS} = \Delta I_{DS} / \beta = 0.06$ V. Therefore, the above expression can be further developed as:

$$0.06 = V_S - \gamma \left(\sqrt{|2\Phi_F - V_S|} - \sqrt{|2\Phi_F|} \right) + \lambda (V_{GS} - V_{TH}) V_{DS,sat} \cdot V_S \tag{4.8}$$

V_S is then obtained as 0.056 V, based on the typical value of each parameters listed previously. This mathematical result has verified the qualitative analysis above.

Because of its superior efficiency, a corresponding compensation scheme to overcome the matching problem of the differential amplifier will be proposed as well. It can be achieved by slightly modifying the structure of the circuit. A significant improvement can be obtained. A detailed description of the scheme is presented in Section 4.4.

4.1.2 Finite Gain Errors

The principles of all four different terminal compensation methods at transistor-level have been introduced above. It can be noted that the compensation voltage in each method can be further interpreted using ΔV_{GS} . As a part of over-drive voltage ($V_{GS} - V_{TH}$), any change in V_{GS} is actually equivalent to a compensation of threshold voltage mismatch ΔV_{TH} between nominally identical transistors. Therefore, all the methods introduced above, in nature, can be regarded as threshold voltage adjusting compensation method.

Apart from ΔV_{TH} , current factor mismatch $\Delta\beta$ is the other parameter used to evaluate device variability. Unfortunately, the variation of β cannot be trimmed cheaply and accurately after the circuits have been fabricated. However, as introduced in previous chapters, β and V_{TH} are partly correlated, as they shared some common variation sources. The threshold voltage related compensation method thus could partly improve the variation of β as well. However, as they are not fully correlated, the mismatch in β cannot be fully eliminated simultaneously. A finite gain error still exists after the compensation is applied.

To demonstrate the gain error, all the BSIM4 compact models based on the arrangement shown in Figure 4.1 (a) have been compensated. The uniform device is used for MN1 and plotted in red in Figure 4.4. The rest models are compensated by applying a gate voltages calculated based on Eq. (3.7), and plotted in blue. Two operational points: $V_{GS} = 0.64$ V and $V_{GS} = 0.87$ V were selected for evaluation. It is obvious that the gain slopes achieve excellent agreement only at the operational point rather than the regime far away. However, the existence of these minor errors will not be a design problem for atomistic device, as multi-stage amplification will rarely be used.

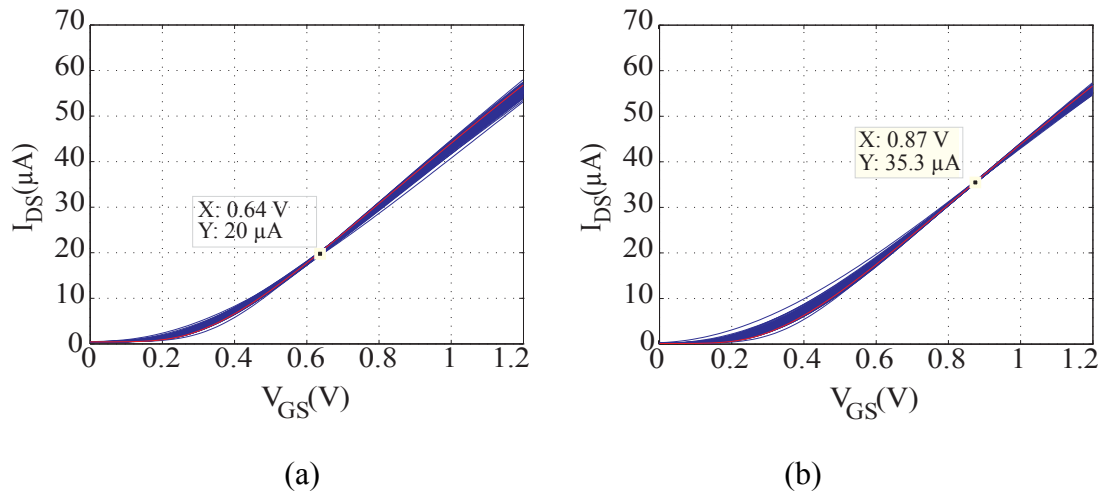


Figure 4.4 (a) Compensated I_{DS}/V_{GS} at $V_{GS} = 0.64$ V. (b) Compensated I_{DS}/V_{GS} at $V_{GS} = 0.87$ V.

4.2 Body-Biasing Compensation Scheme

As the device feature size is scaled, the supply voltage is also scaled to reduce the power budget. However, limited by the nature of silicon material and fabrication process, the threshold voltage is not proportionally scaled. As a result, threshold voltage adjusting technology is required as a knob to adjust the design trade offs among circuit speed, leakage current, power consumption and voltage swing overhead. Body biasing thus has become the prevalent threshold voltage adjusting technology in CMOS IC design. In digital circuit design, it is used to adjust the speed and power between different blocks to match the clock speed and reduce delay. It is also used to adjust the substrate voltage of the whole chip, if the substrate leakage current has not fulfilled the specification. In analogue circuit design, it is not only a potential approach for the transistor-matching problem, but also a method for designing low power and low leakage circuits.

The basic principle of body-biasing is to adjust the V_{BS} based on the body effect of a MOSFET device. Depending upon the polarity of the voltage applied, body-biasing can be categorized into reverse body biasing and forward body biasing. The device threshold voltage would be increased or decreased by reverse or forward bias the substrate, respectively. Forward body bias has the merit of increasing the circuit speed, but at a price of increasing substrate leakage current. Reverse body biasing, on the other hand, behaves exactly the opposite.

It should be noted that the phenomenon of MOSFET body effect reduces as the technology scales. Therefore, the efficiency of this method for compensating the device variability problem will be compromised as well. However, it will be proved that an applicable compensation scheme can still be achieved by careful design.

4.2.1 Differential Amplifier Using Body-Biasing

The differential pair is a widely used design to implement the input stage of operational amplifiers, comparators and many other analogue circuits. However, it is extremely vulnerable to the device statistical variability due to its symmetric topology. Thus, an unwanted offset voltage is easily introduced that has become a critical issue for high precision analogue circuit design.

In this section, the proposed body-biasing schemes have been applied to the test bench circuit of a conventional long-tail differential amplifier with active load. As shown in Figure 4.5, the test-bench differential amplifier is composed by the PMOS active loads (MP1 and MP2) on a source-coupled pair (MN1 and MN2). The NMOS transistors (MN1 and MN2) have been sized using their minimum dimensions $W/L=35\text{ nm}/35\text{ nm}$. As the mobility of electrons is about twice as that of holes, the size of $W/L=70\text{ nm}/35\text{ nm}$ for the load transistors (MP1 and MP2) has been chosen. The biasing transistor MN3 has the size of $W = 2L = 70\text{ nm}$ in order to provide an adequate biasing current. I understand that in a real design scenario, the minimum sizing will not be used in analogue circuit design. A reasonably large size will be selected for each transistor. However, from the research point of view, this sizing configuration is the worst case, as the variation will be reduced if the sizes increase. The whole circuit is biased using a 1 V supply voltage. A common mode input voltage V_{IN} is applied to the gate of the input transistors MN1 and MN2. The gates of MP1 and MP2 are connected to a DC biasing voltage V_{BIAS} , same as biasing transistor MN3. The bulk terminals of MN1 and MN2 are V_{BS1} and V_{BS2} that are connected to ground. V_{BS3} and V_{BS4} are the bulks of MP1 and MP2 that are connected to V_{DD} . However, during the compensation phase, all of them will be used to overcome the circuit variation, as demonstrated in the following sections.

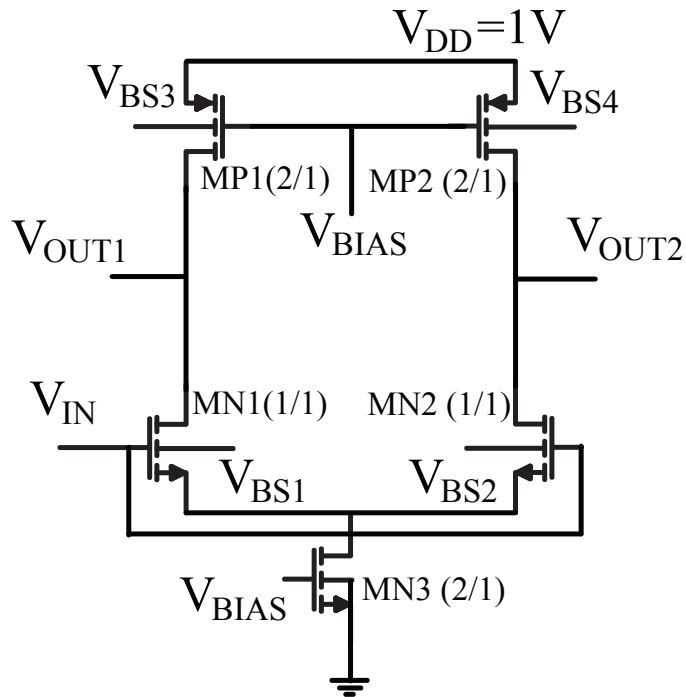
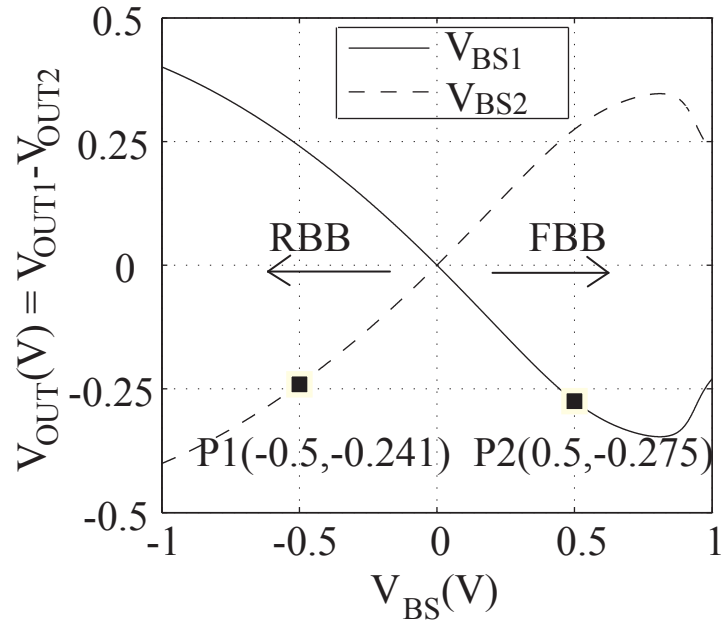
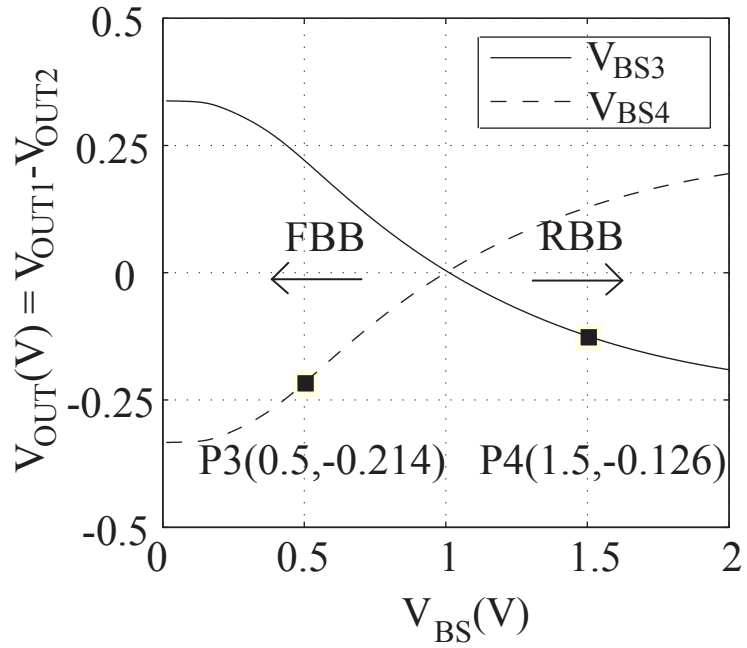


Figure 4.5 Test bench differential amplifier used for body biasing compensation scheme.



(a)



(b)

Figure 4.6 Body biasing efficiency evaluation of the test bench differential amplifier. (a) Bulk voltage V_{BS1} and V_{BS2} of MN1 and MN2 are swept by applying a DC analysis. If the voltage is positive, it is forward body biasing. Otherwise, it is reverse body biasing. (b) Bulk voltage V_{BS3} and V_{BS4} of MP1 and MP2 are swept by using the same DC simulation. It is forward body biased if the voltage lower than 1 V (V_{DD}). Otherwise, it is reversely biased.

To quantitatively understand the achievable magnitude of the compensation when applying body-biasing to the above differential amplifier, the bulk terminals of MN1, MN2, MP1 and MP2 have been tested separately. When one terminal is under test, the rest are connected to their original supply nets. V_{IN} and V_{BIAS} are set to be 0.5 V and 0.58 V, respectively. The whole circuit is perfectly symmetric during the test. The differential output voltage ($V_{OUT} = V_{OUT1} - V_{OUT2}$) is measured and plotted against each bulk voltage V_{BS} by using HSPICE DC analysis.

Figure 4.6 (a) shows the differential output voltage as a result of forward and reverse body biasing by adjusting V_{BS1} or V_{BS2} of MN1 or MN2, respectively. During the DC simulation, V_{BS1} is swept from -1 V to 1 V and plotted using a solid curve in the figure, whilst V_{BS2} is connected to ground. In the region of -1 V to 0 V, a differential output voltage achieves -241 mV when $V_{BS1} = -0.5$ V at point P1 where MN1 is reverse body biased. The opposite is the case when V_{BS1} is in the region of 0 V to 1 V, where MN1 is forward body biased. A differential output voltage of 275 mV is observed at $V_{BS1} = 0.5$ V. Special attentions have been paid to these two values because a large V_{BS} will lead to unwanted current leakage in practice. Therefore, the biasing range of the proposed scheme will be reasonably limited to $-0.5 \text{ V} < V_{BS} < 0.5 \text{ V}$ for MN1 and MN2. The dashed curve represents the differential output voltage when V_{BS2} of MN2 is simulated using a DC sweep, whilst V_{BS1} of MN1 is connected to ground. As expected, its behaviour is horizontally symmetric to the performance of V_{BS1} . Therefore, it can be concluded that if the device variability resulted in a differential output voltage within the range of -241 mV to 275 mV when the same input voltage is applied, either MN1 or MN2 can be body-biased to compensate this mismatch.

As a part of the differential amplifier, body-biasing can also be applied to the active load transistors MP1 and MP2. As shown in Figure 4.6 (b), V_{BS3} and V_{BS4} are separately tested. Since both of them are initially connected to $V_{DD} = 1$ V, V_{BS3} and V_{BS4} are tested from 0 V to 2 V during the experiments. However, they will be limited to 0.5 V to 1.5 V by the real design constraints due to the leakage current. Taking V_{BS3} as an example, MP1 is forward body biased when $0.5 \text{ V} < V_{BS3} < 1 \text{ V}$ and reverse body biased when $1 \text{ V} < V_{BS3} < 1.5 \text{ V}$. The achievable magnitude of differential output voltage is from -214 mV to 126 mV. Similarly as case of MN1 and MN2, the behaviour of MP2 is horizontally symmetric to MP1. Combined with the case for NMOS, it is possible to achieve a wider range of compensation by body biasing both NMOS and PMOS simultaneously. This idea will be implemented in the proposed body-biasing scheme.

4.2.2 Proposed Body Biasing Compensation Scheme

The basic principle of the proposed compensation scheme is illustrated in Figure 4.7. There are two working phases: compensation phase $\phi 1$ and operational phase $\phi 2$. During the compensation phase $\phi 1$, the same common mode input voltage (V_{IN}) is applied to the differential input pair (MN1 and MN2). The output voltages of two branches (V_{OUT1} and V_{OUT2}) are measured and compared by using a comparison circuit, whose output voltage represents the polarity and magnitude of the differential output voltage ($V_{OUT} = V_{OUT1} - V_{OUT2}$) of the test bench amplifier. This output voltage is then used to trigger the control circuit to initialize the biasing circuits of the two branches. These biasing circuits will charge the corresponding capacitors until the differential output voltage is balanced. The compensation circuit will then be disconnected from the differential amplifier during the operational phase $\phi 2$.

The test bench differential amplifier used in this section is shown in Figure 4.5. It is noted that both input transistors (MN1 and MN2) and load transistors (MP1 and MP2) can be used to apply the body-biasing method to increase the achievable compensation range. In this section, three schemes that are based on reverse body biasing (RBB), forward body biasing (RBB), and adaptive body biasing (ABB) are proposed. The advantages and disadvantages will be discussed. During the simulation phase, statistical device variability is taken into consideration for both the differential amplifier and the compensation scheme. The statistical simulation results are shown and discussed at the end of this section.

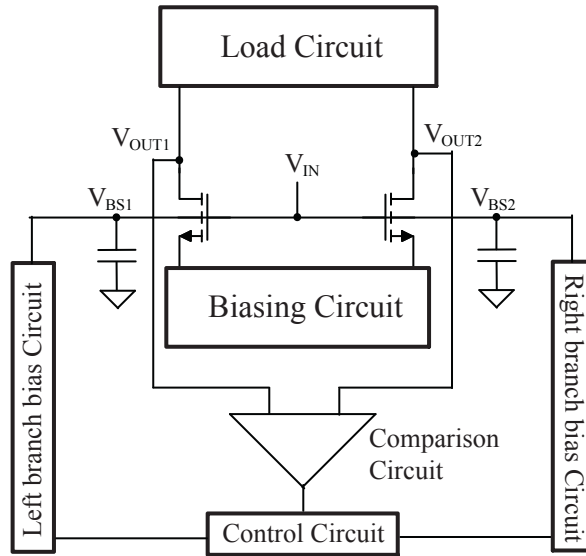


Figure 4.7 Body biasing compensation scheme.

4.2.2.1 Reverse Body Biasing Scheme

As shown in Figure 4.8, both input pairs (MN1 and MN2) and load transistors (MP1 and MP2) are used for body biasing. To achieve a wider range of compensation, the bulk terminals of the relevant transistors (V_{BS1} , V_{BS2} , V_{BS3} and V_{BS4}) are connected with a dedicated capacitor to charge and hold the compensated voltages. Two working phases of this scheme are controlled by switches. During the compensation phase, the output voltages of the test bench differential amplifier V_{OUT1} and V_{OUT2} are compared using a comparison circuit. This comparison circuit is known as a very-wide common-mode-range differential amplifier (VCDA) proposed in [118] that can perform a high performance comparison function and provide a corresponding rail-to-rail output voltage. This output voltage is connected with the control circuit that is composed of two inverter chains to provide biasing decisions. For example, if $V_{OUT1} > V_{OUT2}$, the output voltage of the comparison circuit will be higher than 0.5 V (half V_{DD}). This will trigger the first and second inverter chains to generate a 1.5 V and -0.5 V for the following biasing circuits. There are two types of biasing circuits used in this scheme: "bring-up" biasing circuit and "bring-down" biasing circuit. The "bring-up" biasing circuits are labeled as A1 and A2 in the Figure 4.8. They consist of a PMOS differential input pair followed with an NMOS current mirror load. The circuit can generate an output voltage of 1.5 V when it is active and 1 V (V_{DD}) when it is idle. The "bring-down" biasing circuits work in exactly the opposite fashion. They are used for MN1 and MN2, and labeled as B1 and B2, respectively. Followed by the control signals 1.5 V and -0.5 V from first and second inverter chains, the A1 and B2 will be active accordingly that will reverse bias MP1 and MN2. In the mean time, A2 and B1 remain idle. This is because reversely biased MP1 and MN2 will reduce V_{OUT1} and achieve balanced output voltages when a common mode V_{IN} is applied. After the test bench circuit is compensated, the compensation circuitry will be disconnected for the operational phase.

It should be pointed out that the reverse body biasing can not only effectively compensate the unwanted offset voltage, but can also significantly reduce the substrate leakage currents. These merits are achieved at the cost of consuming additional silicon area for the compensation circuit and using two additional power supply voltages: -0.5 V and 1.5 V. However, as it will be shown at the end of this section, simply increasing the transistor sizes of the test bench circuit to a similar silicon area will not achieve a better compensation performance than used in this scheme. Therefore, a carefully designed compensation circuit is better than passive device scaling.

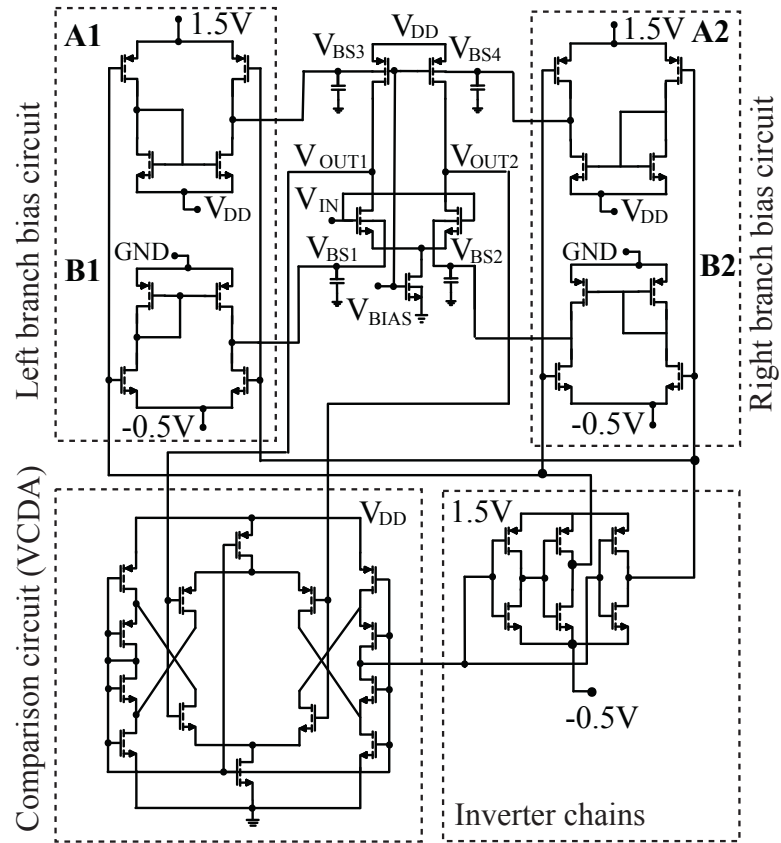


Figure 4.8 Proposed reverse body biasing scheme.

4.2.2.2 Forward Body-Biasing Scheme

As shown in Figure 4.9, the forward body-biasing scheme is based on the same principle and implemented in a similar way compared with reverse body biasing scheme introduced above. In the proposed scheme, MP1 and MP2 are biased using two "bring-down" biasing circuits with a range of 1 V (V_{DD}) to 0.5 V. This is due to the fact that the forward body biasing requires the bulk voltage to be lower than the source voltage for PMOS transistors. Furthermore, no additional 1.5 V supply net is required. For NMOS transistors, two "bring-up" biasing circuits are used to adjust V_{BS1} and V_{BS2} from 0 V (GND) to 0.5 V. Therefore, only one shared 0.5 V supply voltage net is needed, rather than two supply nets 1.5 V and -0.5 V in the reverse body-biasing scheme. Furthermore, the control signal becomes 1 V (V_{DD}) or 0 V (GND), as the inverter chains are supplied using the same voltage sources as the test bench differential amplifier. For example, if $V_{OUT1} > V_{OUT2}$, the comparator will have an output voltage higher than 0.5 V. The first and second output of the inverter will be 1 V and 0 V. Then, B1 and A2 will be active, whilst both A1 and B2 remain idle.

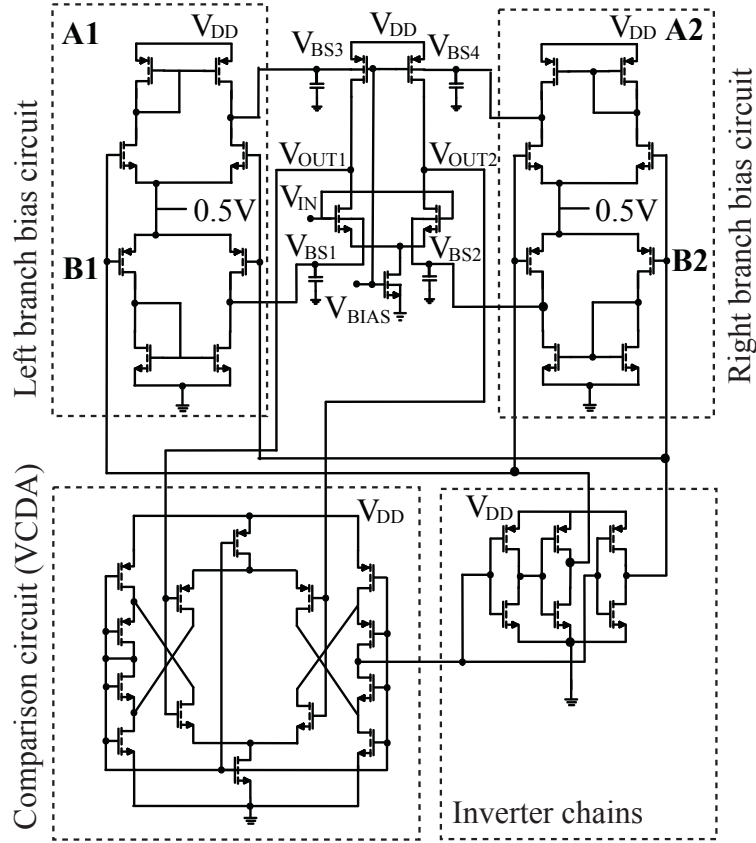


Figure 4.9 Proposed forward body biasing scheme.

The whole compensation circuit can be detached after the compensation phase, similar to the reverse body-biasing scheme introduced above. Although only one additional power net is required, forward body biasing can significantly increase the circuit speed at the cost of increased substrate leakage current. This will become a significant problem when the differential amplifier is heavily used, for example the pre-amplifier array of a high-resolution flash ADC. Compared with the reverse body-biasing scheme, this scheme achieves a better compensation performance with only one additional supply voltage net, as will be shown in Section 4.3.2.

4.2.2.3 Adaptive Body-Biasing Scheme

The proposed adaptive body-biasing scheme is illustrated in Figure 4.10. The idea of "adaptive" is to take the merits of both the forward and reverse body biasing schemes. As demonstrated in Figure 4.10, the circuit topology is the same as the forward body-biasing scheme presented above. However, the supply voltage of the "bring-up" biasing circuit has been increased to 1.5 V. The ground voltage of the "bring-down" biasing circuit has been

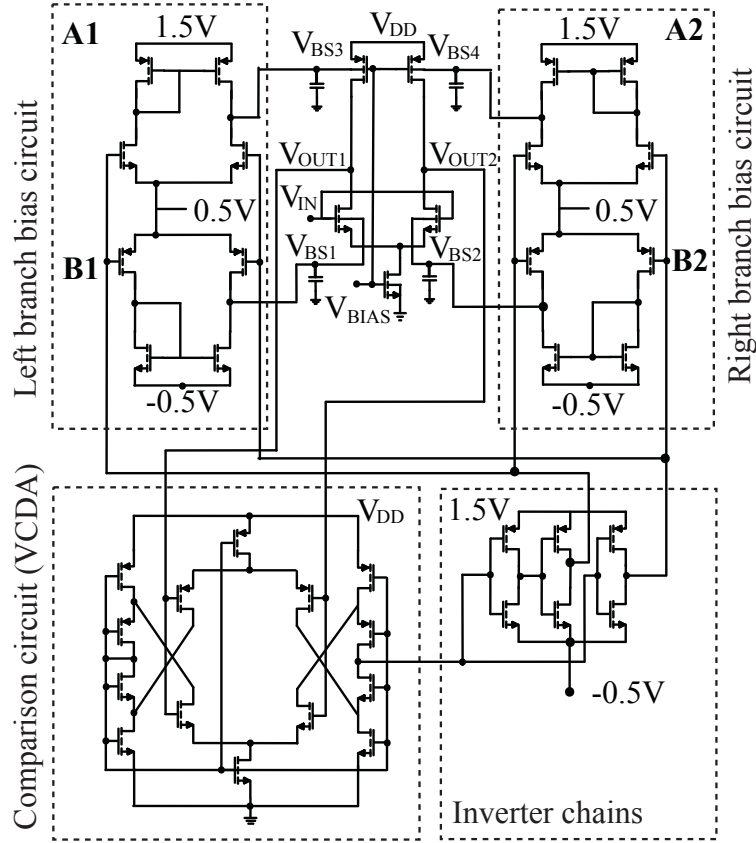


Figure 4.10 Proposed adaptive body biasing scheme.

reduced to -0.5 V. The corresponding control signals have been adjusted accordingly by extending the supply range of the inverter chains. During the compensation phase, the bulk terminals V_{BS1} , V_{BS2} , V_{BS3} and V_{BS4} are all reverse biased before the comparison starts, as this will minimise the substrate leakage currents of the whole circuit at the initial status. Then, if $V_{OUT1} > V_{OUT2}$ is detected, the "bring-down" biasing circuit A1 and the "bring-up" biasing circuit B2 will begin to change the voltages at V_{BS3} and V_{BS2} in order to achieve balanced output voltages. This scheme can cover a wider range of compensation, as it combines both NMOS and PMOS compensation plus forward and reverse biasing range. Therefore, an even lower offset voltage is achieved compared with above two schemes. It also can maintain the substrate leakage current at a reduced level, just like the reverse body biasing scheme. However, it will require 3 supply nets instead of 2 and 1 in the previous schemes.

4.2.3 Simulation Results and Conclusions

Statistical simulations were carried out to evaluate the compensation performances of the test bench differential amplifier with and without the compensation schemes. The circuit

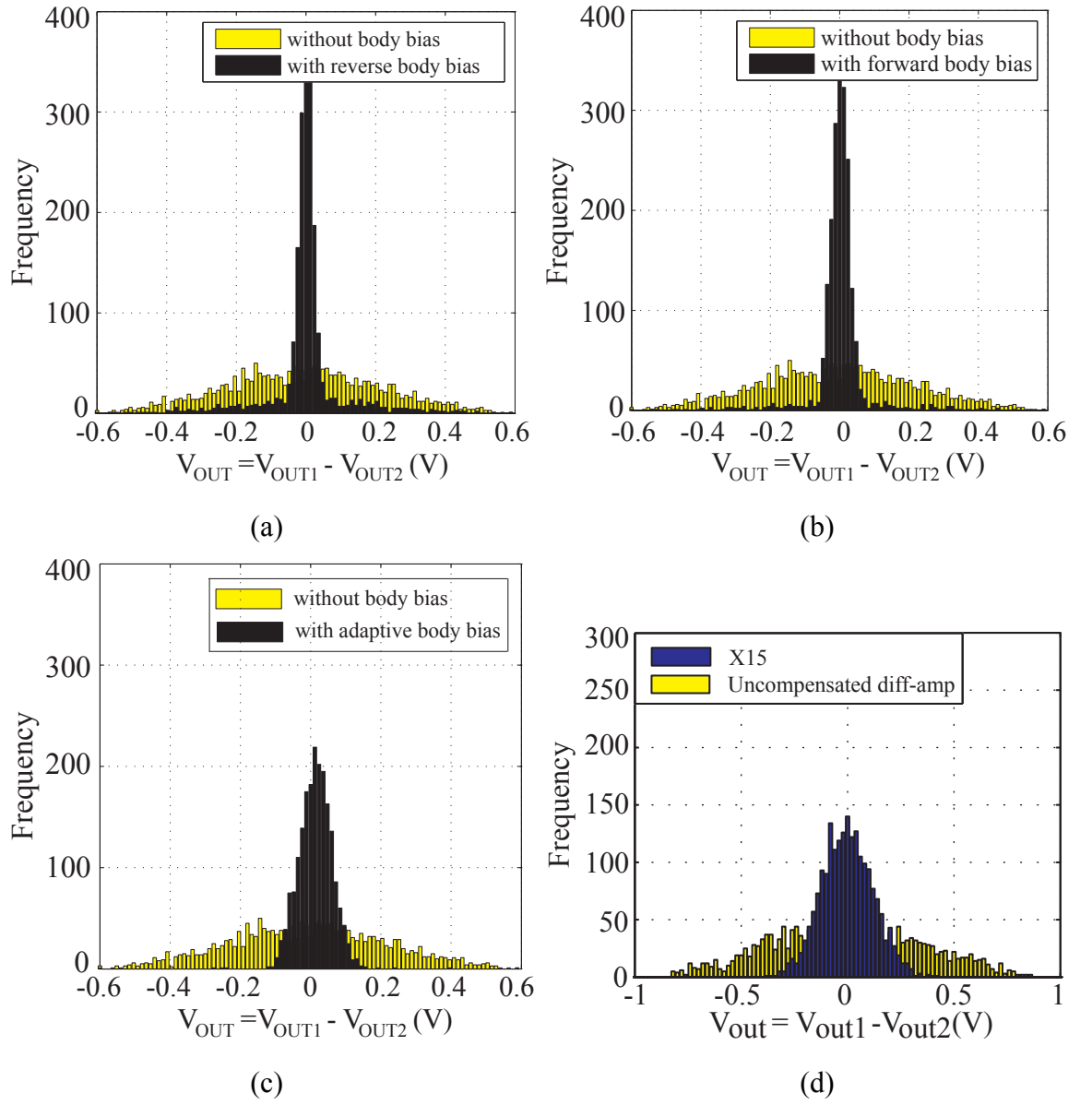


Figure 4.11 V_{OUT} histogram comparison before and after compensation. (a) Reverse body biasing is applied. (b) Forward body biasing is applied. (c) Adaptive body biasing is applied. (d) The test bench circuit is increased by 15 times.

was designed and simulated using the 35 nm gate-length BSIM4 model card library. After obtaining a sample of 2000 randomised netlists of the above schemes, the statistical parameters of differential output voltage ($V_{OUT} = V_{OUT1} - V_{OUT2}$) are extracted. Based on the minimum device size as illustrated in Figure 4.5, the standard deviation of V_{OUT} of the test bench circuit without any compensation is 281 mV. Furthermore, by applying reverse body biasing, forward body biasing and adaptive body biasing with variability taken into consideration for the whole schemes, the same parameter is 106 mV, 60 mV and 21 mV, respectively. Improvements of 62% (RBB), 79% (FBB), 92% (ABB) are achieved. In Figure 4.11 (a), (b) and (c), the histograms of V_{OUT} when there no compensation is applied

are plotted in yellow. The histograms of V_{OUT} when the corresponding body biasing schemes are applied are plotted in black.

It is arguable that the compensation scheme is a large design overhead compared with the differential amplifier itself. Extra 36 transistors are added to the test bench circuit, where there are 18 NMOS transistors and 18 PMOS transistors. If the silicon area occupied by these transistors is used to passively scale the test bench circuit itself, MN1, MN2, MP1 and MP2 will be increased by an extra 9 times. Taking the interconnections and layout style into account, 36 transistors will occupy even more area. Therefore, it is necessary to make a comparison between the compensation schemes and the enlarged circuit. The dimensions of each transistor in the test bench circuit have been increased by 15 times, which is a little overestimated to make the comparison fair. Each enlarged transistor in the test bench circuit is combined by 15 randomised parallel-connected square devices. The standard deviation of V_{OUT} of the enlarged test bench circuit has reduced to 121 mV. The histogram of this simulation is shown in Figure 4.11 (d). From the simulation result, it is noted that the result is still worse than any of the compensation schemes. Therefore, it can be concluded that although sizing is still an effective way to reduce the matching problem, a carefully designed compensation circuit will perform better than simply increase the size of the device. Furthermore, in a real design practice, transistor sizing and compensation methods should both be considered and used to achieve lower mismatch, lower leakage current and lower power.

From all the results shown above it is clear that adaptive body biasing achieves the best offset voltage compensation performance, compared with other two schemes. The main features of three schemes have been listed in Table 4.1. These features represent different design considerations and corners, and also performance trade-offs with each other in design practice. Therefore, depending on the most important circuit perspective, one scheme can be selected.

Table 4.1 Feature comparison among different body biasing schemes.

	$\sigma(V_{OUT})$	Supply nets	Reduced leakage	Increased speed
Uncomp	281 mV	--	--	--
RBB	106 mV	2	Yes	No
FBB	60 mV	1	No	Yes
ABB	21 mV	3	Yes	No

4.3 Drain Compensation Scheme

Drain compensation is another potential approach used to overcome the imperfection of circuit mismatch. Its basic principle is based on the fact that every MOSFET device has limited output impedance. Therefore, the unbalanced drain current can be calibrated by adjusting the drain voltages of nominally identical transistors. As demonstrated in the Section 4.1, the required compensation voltage for a single transistor can even exceed the supply voltage in order to overcome 10 % variation of drain current mismatch. It seems that this approach is not efficient enough to be used in real design practice. Therefore, it has received little attention from circuit designers.

However, it is found that to design an applicable compensation circuit by manipulating the corresponding drain terminals is possible. It is well known that the input transistor of an amplifier is normally loaded with an active device to achieve a satisfactory gain at a small cost of voltage swing overhead. This is one of the reasons that circuit designers do not want to use passive resistors as the load circuit. Based on this feature of the active load, a balanced output for a differential amplifier can be achieved by manipulating its load circuit. In this section, the same test bench differential amplifier will be used to demonstrate the proposed compensation circuit. The compensation scheme used in body biasing is reused in this section with some necessary modifications. Simulation results and discussions will be presented as well.

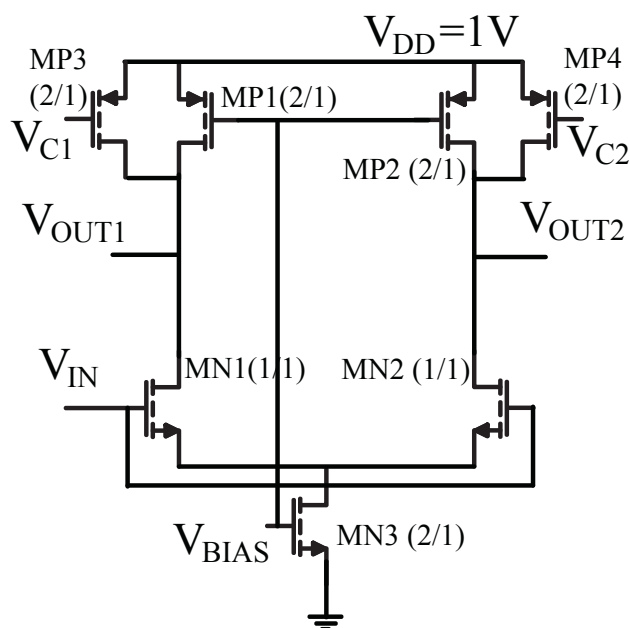


Figure 4.12 Drain compensation test bench circuit.

4.3.1 Principle of Drain Compensation Scheme

Figure 4.12 illustrates the idea of the drain compensation circuit. Compared with a conventional differential amplifier, two extra compensation transistors MP3 and MP4 are added in parallel with the load transistors MP1 and MP2, respectively. Their gate terminals V_{C1} and V_{C2} are initially biased to V_{DD} that turns off both MP3 and MP4. During the compensation phase, if the differential output voltage ($V_{OUT} = V_{OUT1} - V_{OUT2}$) is not zero when same V_{IN} is applied, one corresponding gate terminal (V_{C1} or V_{C2}) can be adjusted that further be interpreted as a modification of the load circuit to compensate the mismatch of the test bench circuit. MP3 and MP4 are sized to be $W/L = 70 \text{ nm} / 35 \text{ nm}$, has the same size as MP1 and MP2. MN1 and MN2 are sized using the minimum size of $W/L = 35 \text{ nm} / 35 \text{ nm}$. V_{IN} and V_{BIAS} are set to be 0.5 V and 0.58 V, respectively.

In order to test the functionality of the proposed circuit in Figure 4.12, V_{C1} is firstly connected to V_{DD} and V_{C2} is swept from 0 V to V_{DD} by using a HSPICE DC analysis. As shown in Figure 4.13, V_{OUT} was adjusted from 0 V to 400 mV and plotted using a solid curve. A symmetric result is achieved by sweeping V_{C2} when V_{C1} is connected to V_{DD} . It is plotted using a dashed curve in the figure. This can be interpreted as by adding MP3 and MP4, the compensation range of V_{OUT} can reach up to $\pm 400 \text{ mV}$. Therefore, the next task is to appropriately control V_{C1} and V_{C2} using a compensation circuit.

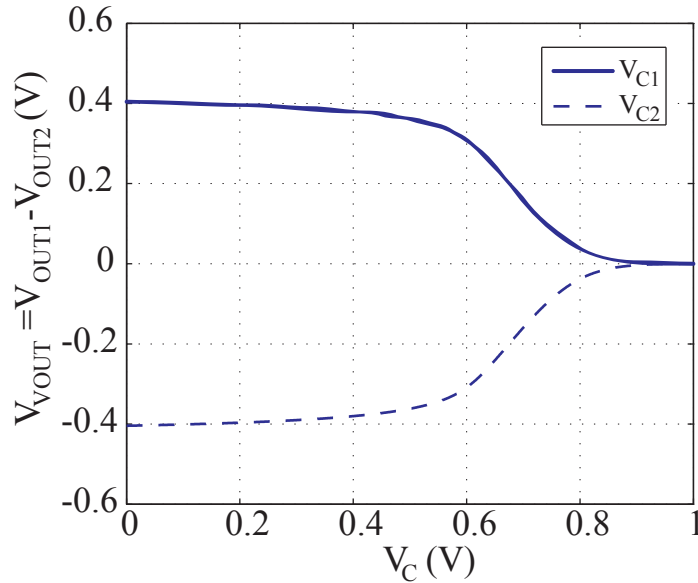


Figure 4.13 The evaluation of drain compensation scheme efficiency. By applying V_{C1} or V_{C2} to the test bench differential amplifier, the differential output voltage can vary from -0.4 V to 0.4 V .

4.3.2 Proposed Drain Compensation Scheme

The proposed drain compensation circuit is illustrated in Figure 4.14. The whole compensation part of the scheme is similar to the circuit that has been used in the body-biasing scheme. Some necessary changes have been made to meet the requirement of the compensation transistors MP3 and MP4. There are two "bring down" biasing circuits A1 and A2 are used to bias the MP3 and MP4, whose output voltage will be V_{DD} when A1 or A2 is idle, and lower than V_{DD} when it is active. The control circuit uses the same supply nets as other parts of circuit. The comparison circuit is also the same. No additional supply net is required.

Similar to the body-biasing scheme, two working phases are required. During the compensation phase, the comparison circuit will evaluate the magnitude of V_{OUT1} and V_{OUT2} . Its output is then fed into the control circuit that will further switch one bias circuit into active mode and the other into idle, depending on the comparison result. The idle biasing circuit will fully charge the hold capacitor to V_{DD} that will turn off the corresponding compensation transistor. The active biasing circuit will charge its capacitor to an appropriate value until the output voltages are matched. The test bench circuit then enters the operational phase, whilst the compensation circuit is then disconnected.

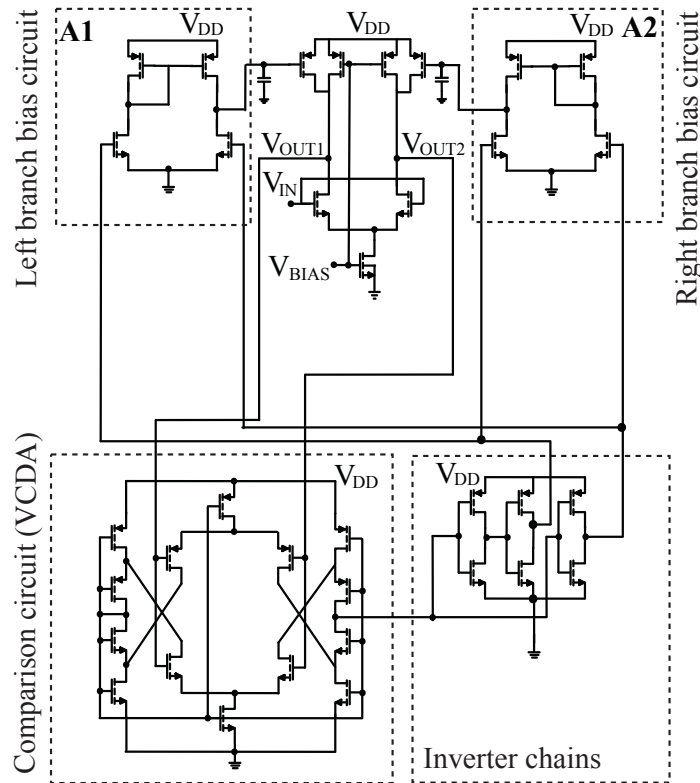


Figure 4.14 Proposed drain compensation scheme.

4.3.3 Simulation Results

Based on the same methodology, statistical simulations are carried out by using the 35 nm BSIM4 model card library. Randomized netlists are generated and simulated using HSPICE. However, it may be interesting to know how many simulations should be run in order to obtain a reliable result from the statistical point of view. Therefore, 6000 randomized netlists have been simulated. It is observed that as the data sample gets larger, the standard deviation of V_{OUT} begins to converge around one data point. For example, in Figure 4.15 (a), the standard deviation of V_{OUT} of the test bench circuit without compensation begins to saturate around 281 mV after 1000 data points are collected. Figure 4.15 (b) shows the same parameter of the circuit with the drain compensation. The standard deviation of V_{OUT} achieves 72 mV after 1000 simulations as well. Therefore, based on this observation, it can be concluded that a data sample of above 1000 simulation results will provide trustworthy results for the compensation circuit design. This observation is also true for the rest of the circuits in this thesis. 2000 statistical simulations have been carried out for a proposed high-speed comparator in Chapter 6. The flash ADC in Chapter 7 has carried out 1000 statistical simulations. This is because the size of the flash ADC is much larger than the test bench circuit used in this chapter. Therefore, the simulation time has been significantly increased.

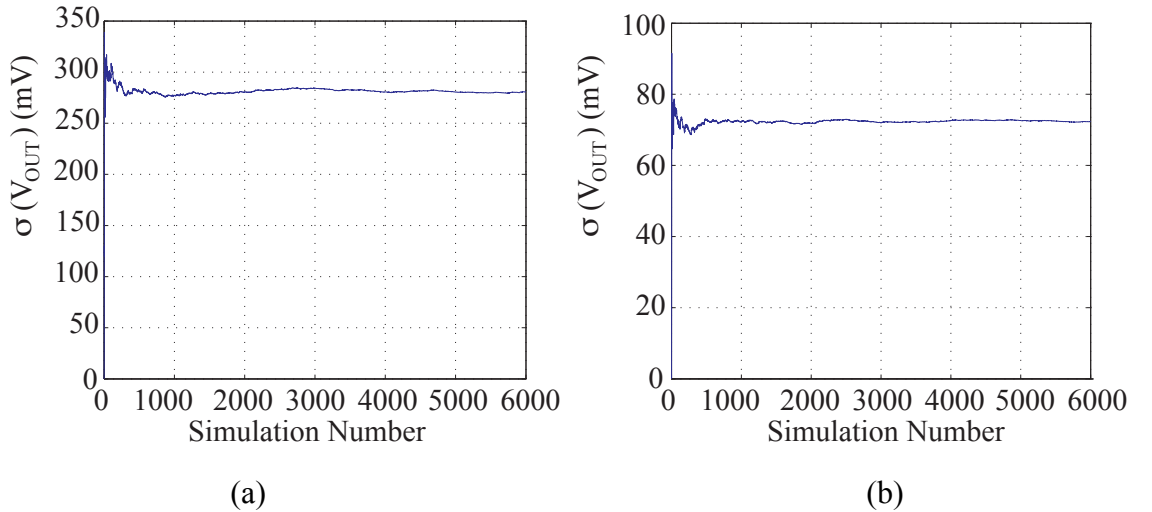


Figure 4.15 Statistical trust region test. (a) The standard deviation of V_{OUT} of the test bench circuit is obtained as a function data sample size. (b) The same parameter of drain compensated result is plotted as a function of data sample size.

4.4 Source Compensation Scheme

Source compensation is another transistor level solution to overcome the mismatch problem between nominally identical devices. As introduced in Section 4.1, the source terminal is used as a reference point for the other three terminals to define their voltage potentials. Therefore, changing the source voltage will result in a change in all the terminals that can be further used to adjust the drain current mismatch.

4.4.1 Principle of Source Compensation Scheme

Regarding the test bench differential amplifier, there are two potential approaches to implement the source compensation concept: (a) adding compensation voltages V_{S1} and V_{S2} at the source of input transistors MN1 and MN2 or (b) adding the voltages at the source of load transistors MP1 and MP2, as shown in Figure 4.16 (a) and (b), respectively. The first approach is difficult to implement in practice because the compensation voltages are hard to control. It may also have a further impact on the biasing transistor MN3 when the circuit is operating. However, the second approach is relatively easy to be achieved. Therefore, two compensation transistors, MP3 and MP4, as shown in Figure 4.17, are added to MP1 and MP2 to implement V_{S1} and V_{S2} , respectively. Appropriate voltages can be obtained and stored in the capacitors, C1 and C2. Furthermore, all the transistors in the test bench differential amplifier in Figure 4.17 have the same sizes as the amplifier in Figure 4.12.

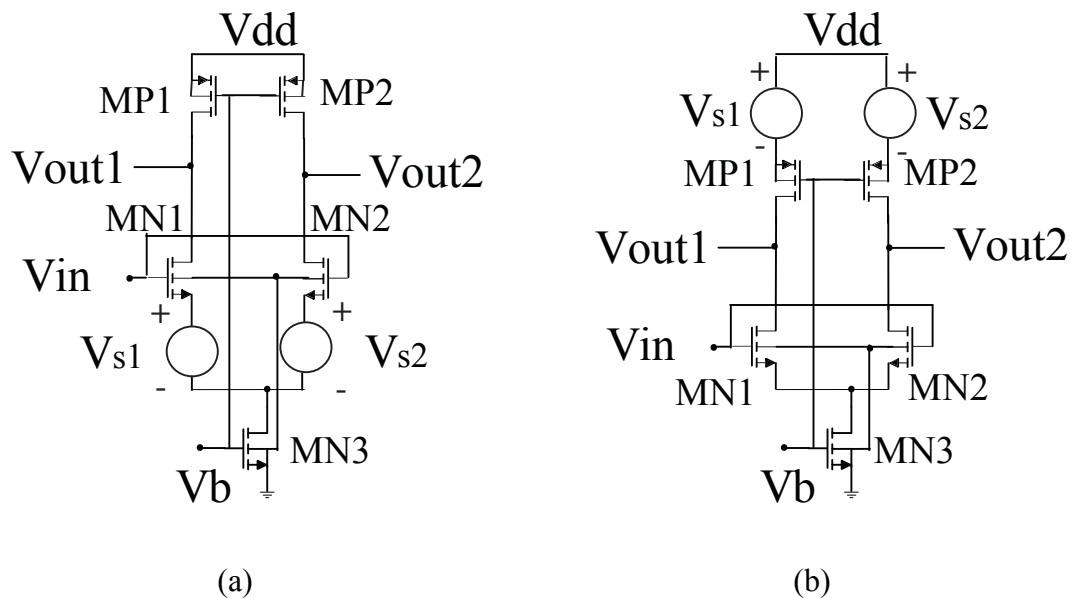


Figure 4.16 Two potential approaches to implement source compensation.

4.4.2 Proposed Source Compensation Scheme

The compensation circuit used to control V_{C1} and V_{C2} is shown in Figure 4.17. The schematic of this compensation circuit is based on the body biasing compensation scheme as well. Necessary changes have been made in order to control the compensation transistors MP3 and MP4. Two "bring up" biasing circuits A1 and A2 are used to bias the MP3 and MP4, respectively. The output voltage of the biasing circuits will be 0 V when A1 or A2 is idle, and can achieve up to V_{DD} when it is active. Therefore, the both MP3 and MP4 will be initialised to be "on" to enable the current flows of two branches. During the compensation phase, one of them will be appropriately adjusted according to the polarity and magnitude of the offset voltage, whilst the other will still acts as a resistor.

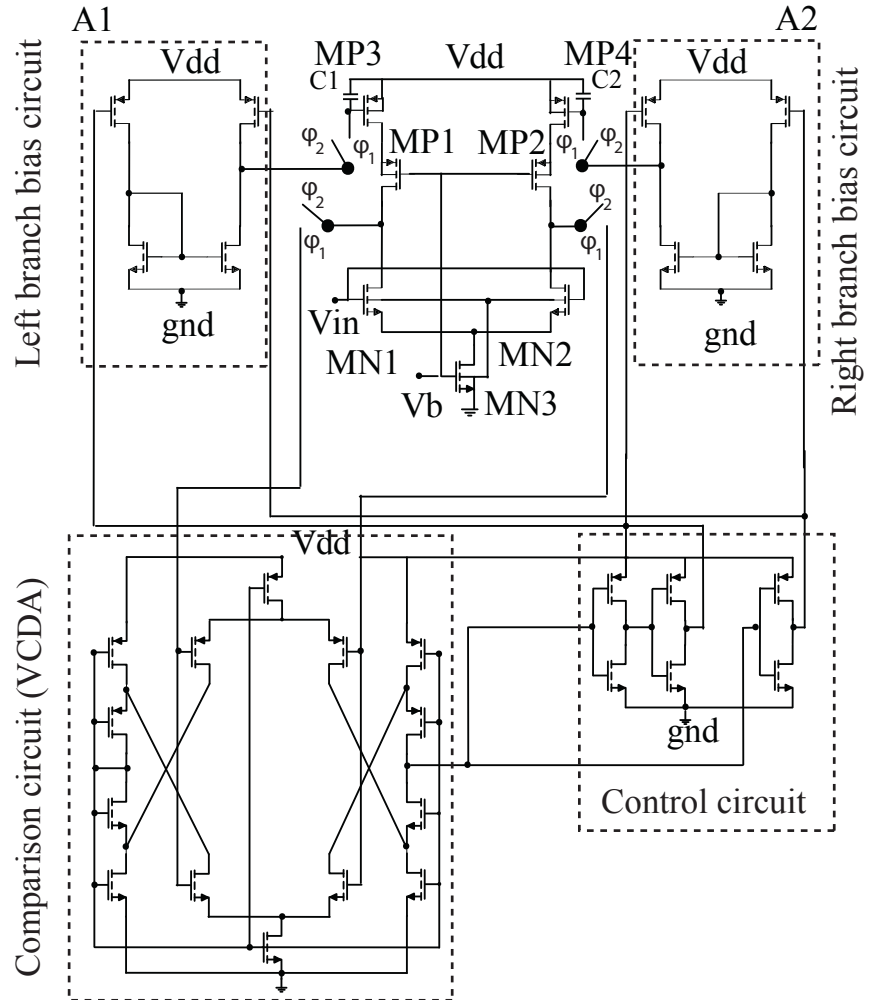


Figure 4.17 Proposed source compensation scheme.

There are two working phases required as well. During the compensation phase ϕ_1 , the comparison circuit (VCDA) will evaluate the magnitude of V_{OUT1} and V_{OUT2} . If $V_{OUT1} > V_{OUT2}$, the output of VCDA will be higher than 0.5 V (half V_{DD}). The output of the first inverter will be set to 1 V (V_{DD}) and the second will be set to 0 V (GND). This will activate A1 and leave A2 idle. The active biasing circuit will charge its capacitor to an appropriate value until the output voltages are matched. The test bench circuit then enters the operational phase, whilst the compensation circuit is then disconnected.

4.4.3 Simulation Results

Similarly to previous compensation schemes, Monte Carlo simulations have been carried out for the proposed source compensation scheme. 2000 random netlists are generated and simulated using HSPICE. Similarly, the output characteristics of the test bench circuit without the compensation scheme have been evaluated. As shown in Figure 4.18 (a), 2000 output voltages of V_{OUT1} from the uncompensated randomized netlists are plotted. The V_{OUT2} behaves very similarly. Then, the output results of one randomly selected netlist before and after compensation are plotted in Figure 4.18 (b). The left branch output voltages V_{OUT1} are plotted in solid red curves, and its counterpart branch is plotted in dashed blue curves. The output voltages without compensation are illustrated with triangle data points, whilst compensated output voltages are presented with square data points. It is noted that V_{OUT1} and V_{OUT2} achieve an excellent agreement over the entire biasing region after the test bench circuit is compensated.

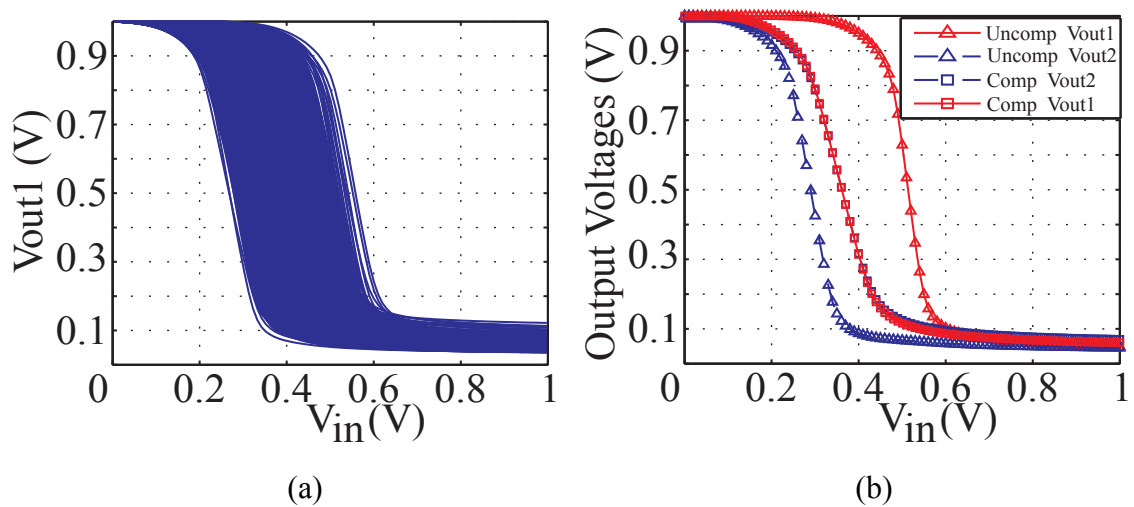


Figure 4.18 (a) The output voltages of V_{OUT1} after 2000 simulations. (b) V_{OUT1} and V_{OUT2} before and after compensation.

The result in Figure 4.18 (b) was achieved by compensating the randomized test bench circuit with an ideal compensation circuit, which is free from device variability. The result proved that the compensation circuit is fully working and the performance is excellent. However, it is known that the transistors in the compensation circuit will also suffer from device variability in real design. Therefore, all the transistors in both differential amplifier and the compensation scheme were randomized and simulated again. Based on a data set of 2000 results, the standard deviation of V_{OUT} is 73.8 mV for the source compensation scheme with device variability taken in to account. The improvement is 79 % compared with the uncompensated test-bench circuit. The histogram of V_{OUT} before and after using source compensation is plotted in Figure 4.19.

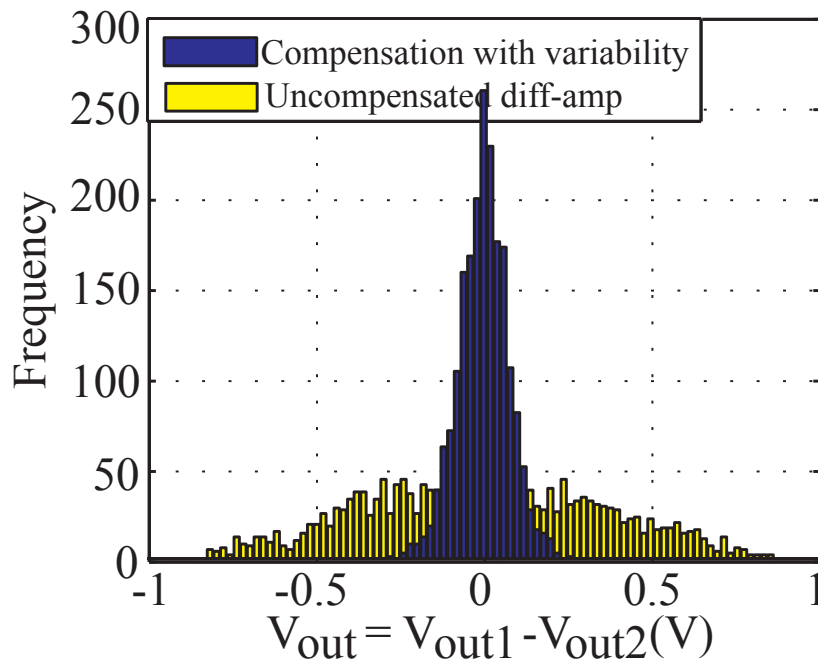


Figure 4.19 Histogram of differential output voltage.

4.5 Summary

Since the device feature size has reached the nanometre regime, process introduced device variability has become a major stumbling block for circuit designers. The performances of both analogue and digital circuits have been significantly degraded. These imperfections cannot be engineered out at the fabrication phase, as the magnitudes of device variations are at the same level of the achievable precision of the fabrication machinery. On contrast,

solutions have been successfully developed during the design phase at the transistor level, base on the fact that the drain current of a MOSFET can be controlled by it four terminals.

In this chapter, the basic ideas of using four different terminals to overcome the device variability have been reviewed. Furthermore, three novel compensation schemes have been proposed, including body-biasing compensation, drain compensation and source compensation. In the body biasing section, reverse body biasing, forward body biasing and adaptive body biasing compensation circuits have been introduced. The merits and trade-offs have been discussed as well. Excellent performances have been achieved, as the standard deviation of the differential output voltage has been improved from 281 mV to 106 mV, 60 mV and 21 mV by using RBB, FBB and ABB, respectively. Furthermore, the body-biasing scheme is the only technology that can adjust the substrate leakage current, circuit speed and threshold voltage. Drain compensation and source compensation are based on the fact that a MOSFET device has limited output impedance. Therefore, changing the load circuits can modify the drain current. Their compensation circuits are similar to the one used in the body biasing scheme, with necessary modifications. A good 72 mV and 73.8 mV of standard deviation of V_{OUT} have been achieved as well.

Furthermore, during the simulations, the minimum size for each transistor in the test bench circuit and the compensation circuit have been chosen. This is done for researching and investigating the impact of variability on these circuits only. In practice, larger transistor sizes will be used and the actual mismatch will be smaller as well, as illustrated in Figure 4.11 (d). The figure shows the statistical results of the 15 times enlarged test bench circuit. It further proved that a carefully designed compensation scheme could achieve better performance than passively increasing the transistor size. Last but not least, the data sample size has been discussed from a statistical point of view. It has been observed that a data sample of 1000 netlists is required to obtain a reliable result. Furthermore, these compensation ideas can be further used in circuit level compensation designs.

Chapter 5 Impact of Variability on High-Speed Comparator Design

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5.1 High-Speed Comparator Design Using Atomistic Device

A high-speed comparator is the key building block in designing a flash ADC in analogue circuit design. After two input signals are applied, it is expected to generate a binary output at a short propagation delay. In order to achieve this design target, a high-speed comparator normally consists of a pre-amplification stage, a regenerative (latch) stage and an output buffer stage. The pre-amplifier is required to have a wide bandwidth that can amplify and propagate the input signals to the next stage with little delay. This stage is also used to improve the comparator's sensitivity and to avoid switching noise from the following regenerative stage. Furthermore, it is also possible to apply a compensation circuit at this stage in order to reduce the input offset voltage. The regenerative comparator, also known as the latch, uses a positive feedback mechanism to achieve a fast comparison between two signals. The key part is implemented by using two identical head-to-tail connected inverters, surrounded by the reset circuits. The last output buffer stage is used to provide a binary signal that is able to drive large capacitive loads.

As device scaling reaches the UDSM regime, the speed performance of a comparator has been increased due to a reduced device parasitic capacitance. The scaled device dimensions also decrease the power consumption of the comparator and increase the integration density on a unit silicon area. However, the high-speed comparator circuit is extremely sensitive to the device statistical variability due to its symmetric input stage and latched inverters. This worsens as the scaling of the device, where device variability is predominantly introduced by intrinsic parameter fluctuations that cannot be eliminated by the use of layout techniques or tightening the process control. As a result, the impact of unwanted input-referred offset voltage, which degrades the circuit performances and yield, is significantly increased.

Meanwhile, applicable design solutions can still be implemented to overcome the impact of variability on a high-speed comparator. After reviewed the comparator structure, it is widely acknowledged that compensation circuits are difficult to be applied to the regenerative or the output buffer stage. Therefore, the pre-amplification stage has become a popular choice during real design practice [119]. Most of pre-amplifier is implemented using a differential pair followed by certain load and biasing circuitry. This topology

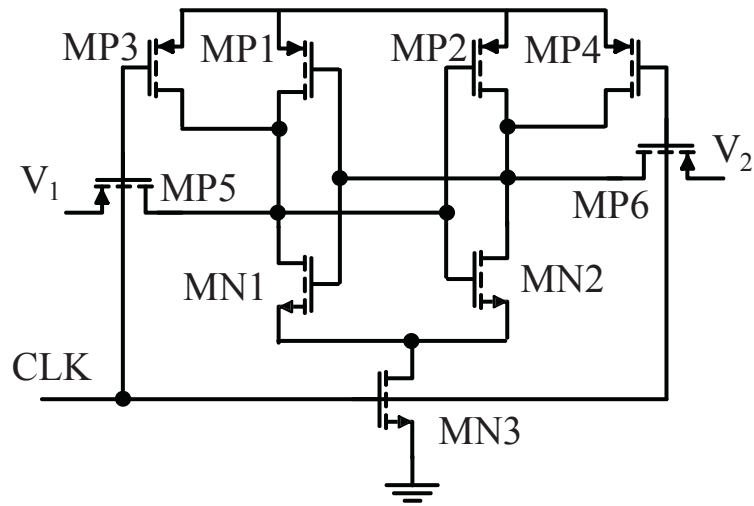
provides the designers the opportunity to apply the compensation principles introduced in previous sections to a high-speed comparator.

In this Chapter, a novel high-speed low-power comparator circuit will be presented and verified using 35 nm CMOS. At a supply voltage of 1 V, the comparator operates at a clock speed of 15 GHz and consumes 0.28 mW. At a reduced 0.5 V supply voltage, the comparator consumes as little as 15 μ W at a speed of 4 GHz. This high-speed comparator can be further used as a key building block for a flash ADC that will be introduced in the Chapter 6. However, the operational accuracy of the proposed comparator will be inevitably reduced by the device variability. In this Chapter, a new offset compensation scheme for the proposed comparator will also be presented using the drain compensation principle. It has successfully reduced the offset voltage of the comparator from 67.4 mV to 29 mV at a supply voltage of 0.5 V and from 43.1 mV to 20.3 mV at a 1 V supply voltage.

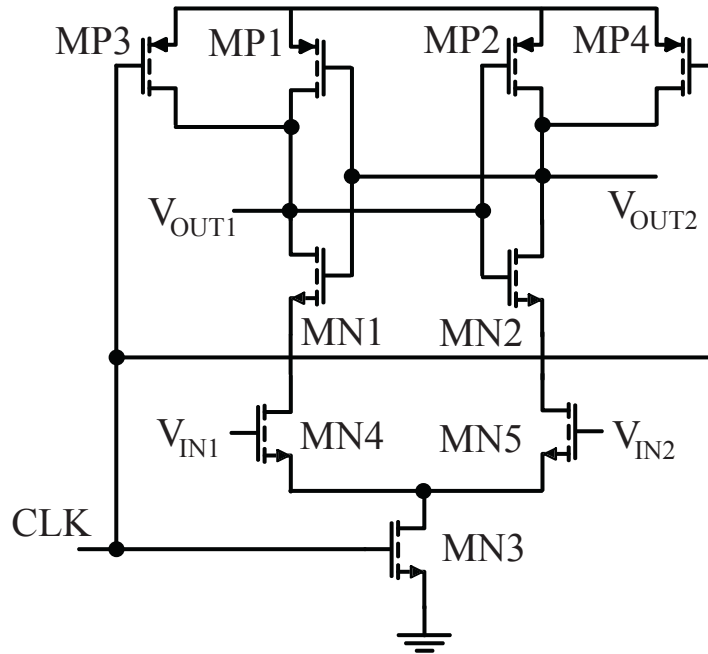
5.1.1 High-Speed Comparator Design

5.1.1.1 Conventional Comparator Arrangements

A regenerative stage is widely used in comparator design to achieve a fast decision due to its positive feedback mechanism. It often follows a pre-amplifier that has wide bandwidth. During design practice, the regenerative stage is also known as latch comparator or sense amplifier. Two types of circuit implementations are commonly used, known as voltage latch sense amplifier (VLSA) and current latch sense amplifier (CLSA) [88]. As shown in Figure 5.1 (a), the VLSA is composed by two cross-coupled inverters (MN1-MP1 and MN2-MP2), followed by a tail transistor MN3. Two PMOS transistors (MP3 and MP4) are controlled by the clock signal and used to reset the latch accordingly. Since the input terminals are physically the same as the output terminals, they can only be shared at different time slots. To achieve this separation, two PMOS transistors MP5 and MP6 are used as switches according to the circuit clock. During the operation of the comparator, when the clock signal "CLK" is low, the comparator is in the reset phase. MN3 is closed, stopping any static current flow through the circuit. MP3 and MP4 are turned on to reset the latch comparator, whilst MP5 and MP6 are on allowing V_1 and V_2 to be sensed by the comparator. When the clock signal "CLK" is high, the comparator enters the comparison phase. The difference between V_1 and V_2 are held and initiate a positive feedback on the latch. A comparison result is swiftly obtained and the current flow stops immediately. Hence, no static power will be consumed afterwards.



(a)



(b) CLSA

Figure 5.1 The schematics of conventional comparator designs. (a) Voltage Latch Sense Amplifier (VLSA). (b) Current Latch Sense Amplifier (CLSA).

The second popular configuration CLSA is shown in Figure 5.1 (b). High impedance input differential stage (MN4 and MN5) is added between the latch (MN1-MP1 and MN2-MP2) and the tail transistor MN3. The difference of input voltages V_{IN1} and V_{IN2} will result in a current difference between the two branches that will initiate positive feedback of the latch. Since the current is used to trigger the comparison, it is known as current latch sense amplifier. Controlled by the clock signal, transistors MP3, MP4 and MN3 are used to reset the latch circuit and minimise the static power consumption of the CLSA.

The above two arrangements are widely used in different design practices based on their merits and drawbacks. It is noted that unlike the case of VLISA, the input and output terminals of the CLISA are separated. This is a great advantage over VLISA where the control switches MP5 and MP6 form two decoupling resistors in a real design. They will further introduce voltage drops between two branches, deteriorating the available input voltage difference. Furthermore, the transistor sizes of MN4 and MN5 in the CLISA provide circuit designers a knob to adjust the offset voltage of the circuit. This is not possible during the design of VLISA. However, VLISA can achieve a higher sensing speed at a lower cost of layout area compared with CLISA when the same transistor sizes are used. Meanwhile, as fewer transistors can be stacked between supply voltage and ground, the static power consumption of VLISA is lower as well. This is a critical design consideration when using atomistic devices. Based on the above analysis, the VLISA and CLISA are used under different scenarios depending on the requirements of the application.

5.1.1.2 Proposed High-Speed Comparator

As shown in Figure 5.2, following by the conventional design philosophy, the proposed high-speed comparator is composed of three stages: a pre-amp stage, a latch stage and an output buffer stage. The pre-amp stage has a differential input pair (MN4 and MN5), followed by current control transistors (MN6 and MN7) and a tail transistor (MN8). The configuration of the latch stage is the same as the VLISA. Followed by a tail transistor MN3, the latch consists of two inverters: MN1-MP1 and MN2-MP2. MP3 and MP4 are controlled by the clock signal "CLK" to reset the latch. The circuit arrangement of the last output buffer stage is implemented using two NAND gates (NAND1 and NAND2).

The requirements of achieving low power consumption and a high circuit speed using small supply voltages are all taken into account while designing this comparator. When the clock signal "CLK" is low, the comparator is in the reset phase. Both V_{OUT1} and V_{OUT2} are charged to V_{DD} by MP3 and MP4, turning on the differential pair (MN4 and MN5) and the current control transistors (MN6 and MN7). Transistors MN8 and MN3 are turned off to minimise the static power consumption. When the "CLK" signal is high, the comparator enters the comparison phase. MN8 is turned on, driving the pre-amplifier in to working mode. The difference between V_{IN1} and V_{IN2} will be interpreted into a current difference between the symmetric branches. Furthermore, the unbalanced working currents lead to a voltage difference at the V_{OUT1} and V_{OUT2} . The second latch stage then triggers the positive feedback process.

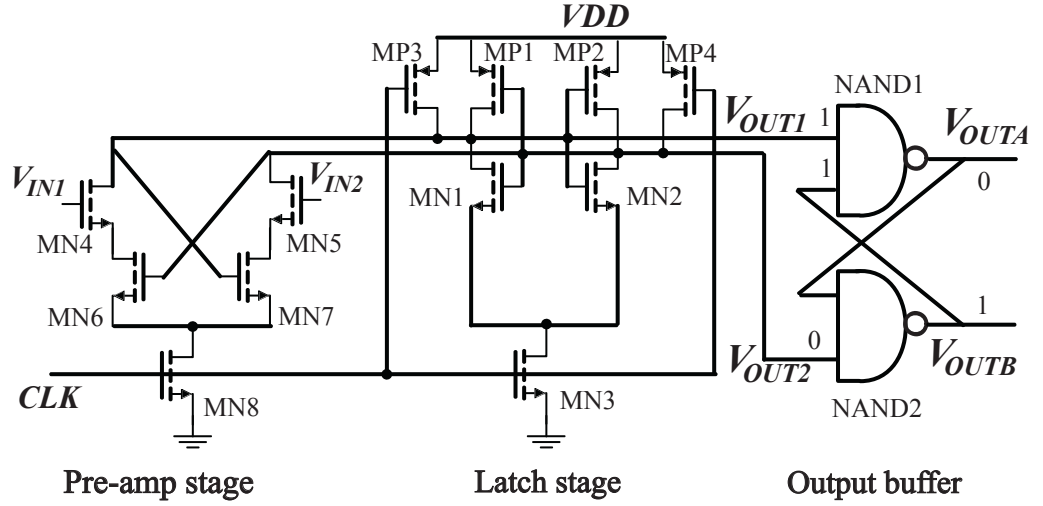


Figure 5.2 Proposed High-Speed Comparator.

After the comparator is latched, the lower one between V_{OUT1} and V_{OUT2} is pushed to 0 V and the higher one is pulled to 1 V. The status of all the transistors can then be reviewed by assuming that $V_{OUT1} = 1$ V and $V_{OUT2} = 0$ V. In the pre-amp stage, since $V_{OUT2} = 0$ V, transistor MN6 is turned off and there is no static current flow through the left branch. The current can only flow through MN5, MN7 and MN8. However, this is not possible, because the drain voltage of MN5 equals $V_{OUT2} = 0$ V. Therefore, no static power is consumed in the pre-amp stage, as both branches are off. In the latch stage, reset transistors MP3 and MP4 are turned off by the "CLK". MN1 and MP2 from the left and right branches are switched off based on the values of V_{OUT1} and V_{OUT2} , respectively. The power consumption from this stage is minimised as well. The last output stage is used to provide binary outputs that can drive high capacitive loads. As $V_{OUT2} = 0$ V, "NAND2" will have a binary "1" at the output, regardless of the value of another input. This output is pushed into "NAND1". Combined with $V_{OUT1} = 1$ V, the output of "NAND1" is "0".

In this design, a maximum of three transistors are serially connected between supply rails among all the stages. This design consideration is based on the trend of the scaled supply voltage in UDSM regime. Furthermore, the pre-amplification stage has the merits of CLVA that: (a) the offset voltage can be reduced by increasing the dimensions of MN4 and MN5 and (b) input and output terminals are physically separated. The latch stage inherits the fast decision speed feature from VLSA. Last but not the least, power consumption has been minimised by using MN8 and MN3, as introduced above.

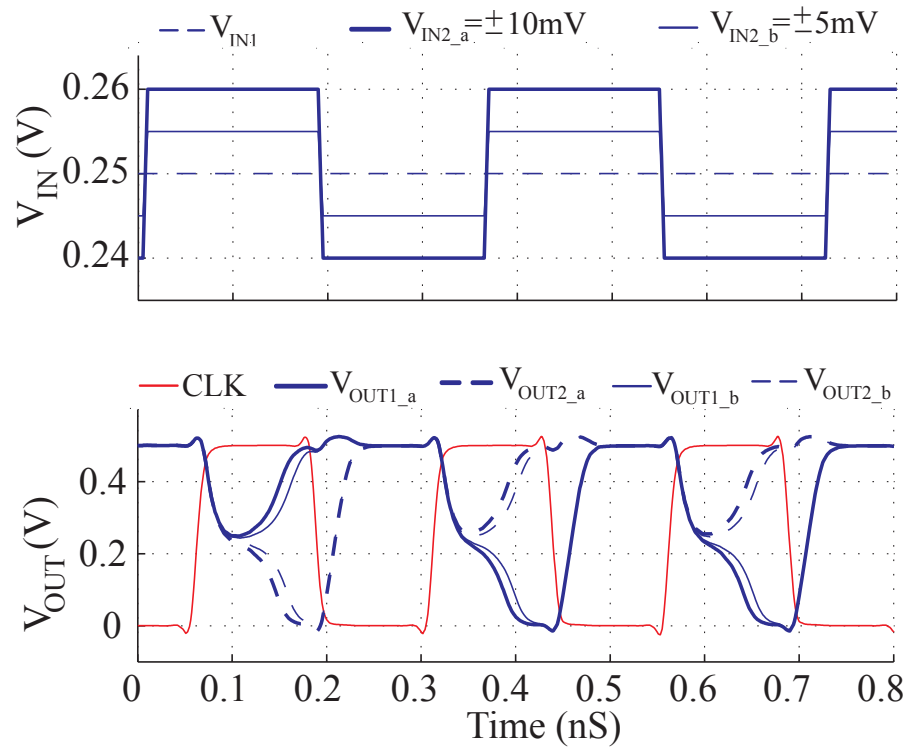
5.1.2 Performance Evaluation

Based on the proposed circuit configuration, transient analysis was performed to evaluate the desired design perspectives. The 35 nm BSIM4 model card library has been used for HSPICE simulation. The parasitic capacitances from the drain and source were taken into account. During the evaluation of circuit speed and power consumption, the models of NMOS and PMOS with uniform configuration profiles were used. The circuit is then evaluated under different supply voltages and clock speeds. During the test of the input offset voltage, a binary search algorithm is developed and used for statistical simulations. The proposed comparator was randomised into 2000 netlists for simulation. Statistical information of the input offset voltage was extracted from the simulation results, and will be presented using histograms in this section.

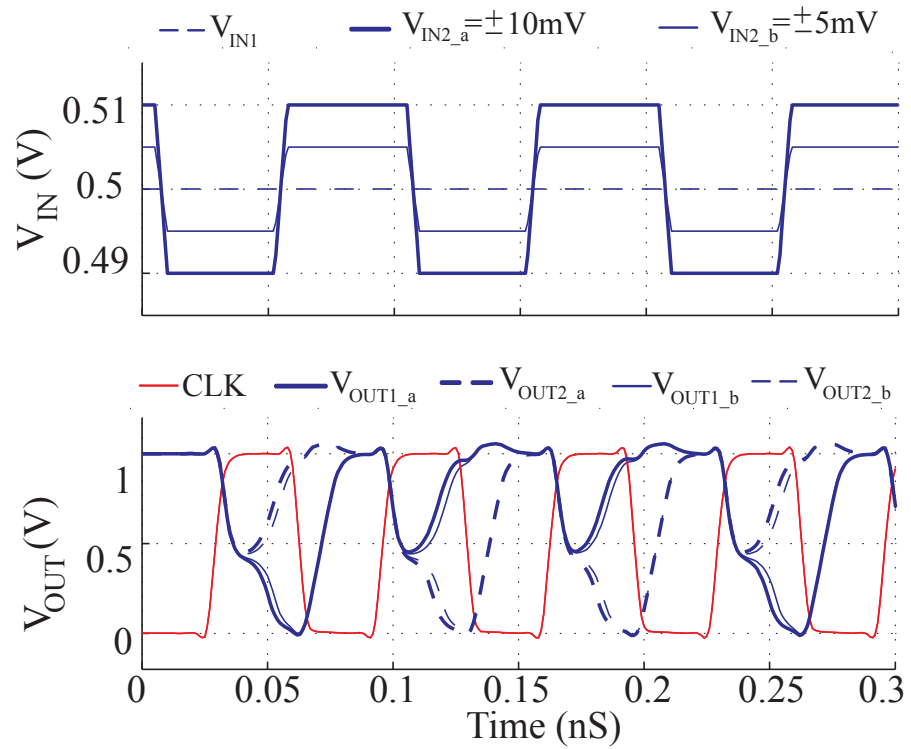
5.1.2.1 Circuit Speed and Power Analysis

The achievable operation speed of the comparator is closely related to the supply voltage of the circuit, as a higher supply voltage can provide a stronger current that will charge and discharge the intrinsic parasitic capacitors at a faster rate. Therefore, the circuit has been tested using 0.5 V and 1 V supply voltages. The power consumption of the circuit is also tested under the above conditions.

As shown in Figure 5.3 (a), the signals of the comparator are plotted when a 0.5 V supply voltage is applied. Input signals V_{IN1} and V_{IN2} are illustrated using dashed and solid curves, respectively. Two square waves (V_{IN2_a} and V_{IN2_b}) are applied to V_{IN2} one by one with an offset at 0.25 V and amplitude of ± 10 mV and ± 5 mV, whilst V_{IN1} is fixed to be 0.25 V. The speed of the comparator is controlled by the clock signal "CLK" with a frequency of 4 GHz (clock cycle of 250 ps), and is presented as the solid red curve in the figure. When the "CLK" is low, the comparator enters the reset phase. Both V_{OUT1} and V_{OUT2} are charged to V_{DD} by MP3 and MP4. As soon as the rising edge arrives, the comparison detects the input difference and triggers the circuit to operate. As shown in Figure 5.3 (a), during the three clock cycles swift decisions were achieved at the rising edges of the clock. It is noted that an amplitude difference of ± 10 mV between input signals has a faster response than the case of ± 5 mV. The power consumption is as low as 15 μ W under this test condition. In Figure 5.3 (b), under the same test setup, the circuit is simulated with an increased supply voltage of 1 V and a clock speed of 15 GHz. The power consumption increases to 0.28 mW.



(a)



(b)

Figure 5.3 Detailed plots of signals from the transient Analysis of the proposed comparator. Input voltage differences of $\pm 5\text{ mV}$ and $\pm 10\text{ mV}$ are applied using the testing. (a) The comparator is tested with a 0.5 V supply voltage at a clock speed of 4 GHz. (b) The comparator is tested with a 1 V supply voltage at a clock speed of 15 GHz.

5.1.2.2 Input Offset Voltage

The methodology of measuring the offset voltage of a comparator is significantly different from the way used in measuring the same parameter of an operational amplifier. This is because that an operational amplifier has a static operational point, around where DC analysis of the input signal can be applied. The input and output voltages have a linear relationship. In practice, the offset voltage can be obtained by a single simulation analysis.

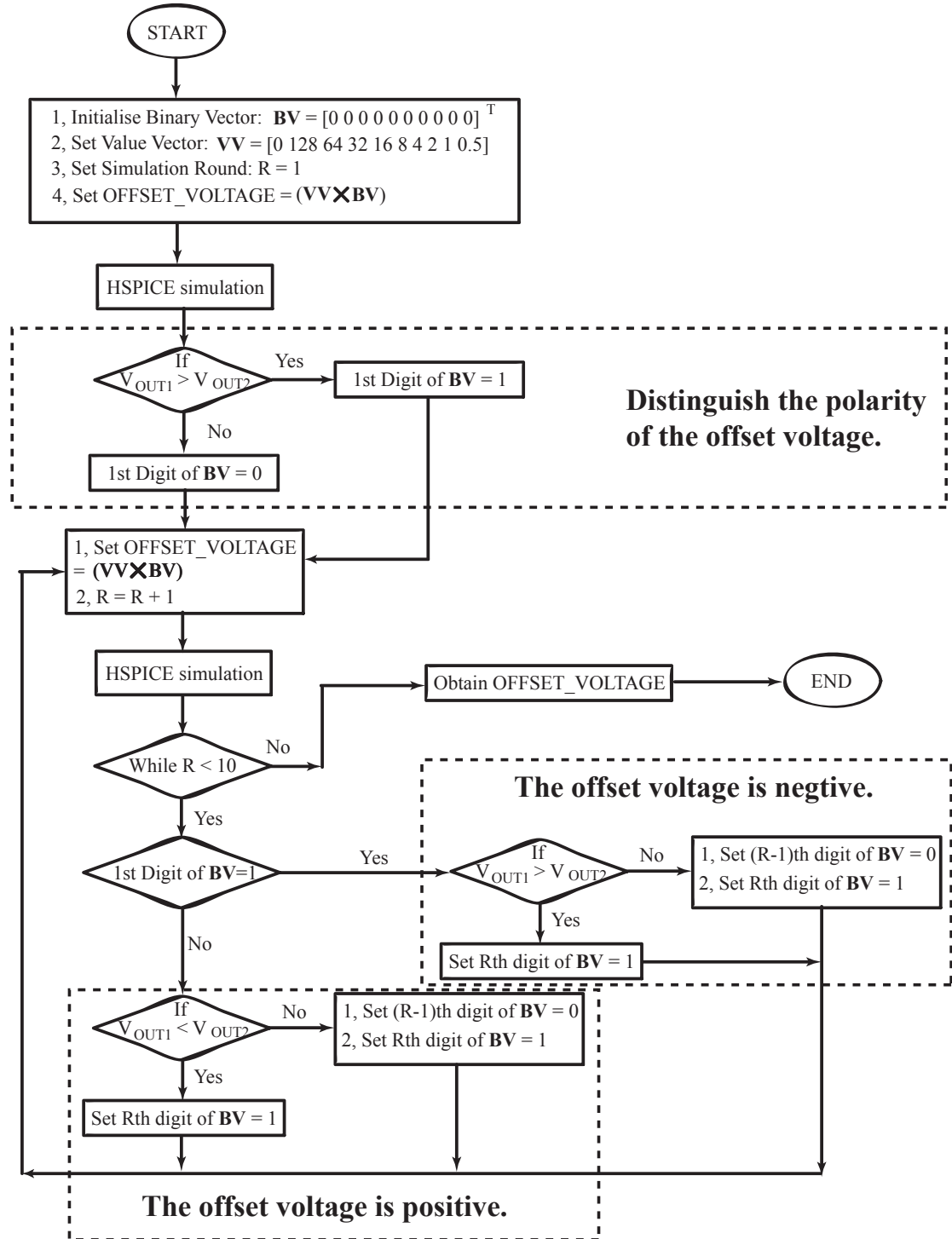


Figure 5.4 The flow chart of offset evaluation using a binary search algorithm.

However, this is not the case for evaluating the offset voltage of a comparator. The output voltage of the comparator is expected to be a binary value as a result of the input voltage difference polarity. Therefore, DC analysis is not appropriate for evaluation, as there is no fixed operational point for a comparator. Transient analysis is the only way to evaluate the behaviour of a comparator.

The proposed offset voltage evaluation methodology is shown in Figure 5.4. The basic idea is to carry out a binary search algorithm for evaluating the offset voltage. After 2000 randomised comparator netlists are generated, each one is examined from the start to the end using the above algorithm. For every netlist, one fixed common mode DC signal is provided, for example $V_{IN} = 0.5$ V if $V_{DD} = 1$ V or $V_{IN} = 0.25$ V when $V_{DD} = 0.5$ V. The terminals of the netlist V_{IN1} and V_{IN2} are configured to have values of V_{IN} and $V_{IN} + \text{OFFSET_VOLTAGE}$, where "OFFSET_VOLTAGE" is a keyword that will be replaced later on during the evaluation. The keyword replacement is achieved by using MATLAB. The value of OFFSET_VOLTAGE is equivalent to the vector product of the Binary Vector (BV) and the Value Vector (VV). The Binary Vector has a size of ten by one, where the first digit represents the polarity of the offset voltage. The Value Vector is a one by ten vector that defines the achievable range of the offset voltage. In this algorithm, a range of 512 mV can be set during the simulation that is from +256 mV to -256 mV with a minimum step of 0.5 mV.

After initialising the BV and VV, the OFFSET_VOLTAGE is equal to 0 V and the simulation round flag is set to be 1. The first HSPICE simulation of the selected randomised netlist can determine the polarity of the offset voltage. The BV is set accordingly. Next, the evaluation loop starts to determine the binary search result that is saved in the BV. It is noted that the evaluation process for the positive and negative cases are different, as it is larger for a negative value if it has a smaller absolute value. After another 9 loops, the value of the offset voltage can be determined. The algorithm is implemented using MATLAB and controlled by a C-shell script under Linux environment.

The offset voltages of 2000 randomised netlists are shown using histograms in Figure 5.5. In Figure 5.5 (a), the randomised netlists are tested using a 0.5 V supply voltage and a common mode input voltage of 0.25 V. The standard deviation of the offset voltage is 67.4 mV. In Figure 5.5 (b), the same randomised netlists are biased using a 1 V supply voltage and a common mode input voltage of 0.5 V. The standard deviation of the offset voltage reduces to 43.1 mV.

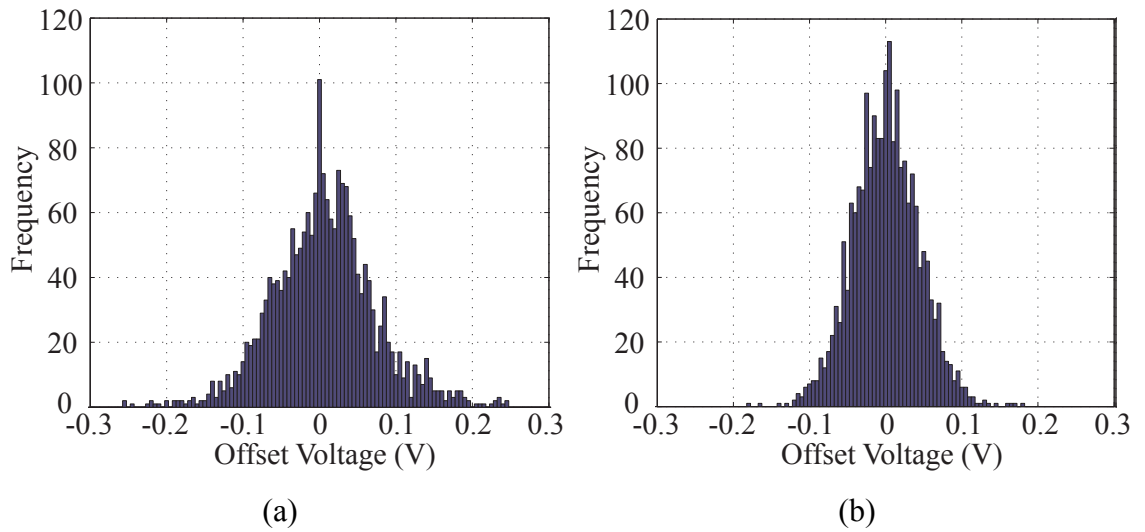


Figure 5.5 Histograms of the offset voltage based on a sample of 2000 randomised comparator netlists. (a) The proposed comparator is tested using 0.5 V supply voltage at a speed of 4 GHz. (b) The proposed comparator is tested using 1 V supply voltage at a speed of 15 GHz.

5.2 Offset Compensation Scheme for High-Speed Comparator Design

A high-speed comparator is widely used in flash ADC designs as it can provide fast decisions. Its offset voltage is a critical parameter that limits the achievable resolution of a flash ADC. It is required that the standard deviation of the offset voltage has to be smaller than $1/3$ of the least significant bit (LSB) in order to receive a reliable design margin. For example, if a flash ADC has a 1 V supply voltage with a resolution of 3-bits, the value of LSB equals to $1/2^3 = 0.125$ V. Then, the required offset voltage of the comparator used is $1/3 \times 125 \text{ mV} = 41.6 \text{ mV}$. Therefore, the comparator precision proposed in the previous section is almost good enough to meet this design target.

However, it is possible to improve the impact of variability to the circuit accuracy by applying a compensation scheme. In this Section, a customised compensation circuit is proposed and tested for the high-speed low-power comparator. Two extra transistors are added to the pre-amplification stage. A significant improvement in the standard deviation of the offset voltage has been achieved. Transient analysis is carried out to evaluate the speed performance. The proposed offset voltage evaluation methodology is reused to test the compensated comparator circuit at the end of this section.

5.2.1 Proposed Compensation Scheme

5.2.1.1 Design Consideration

A high-speed comparator normally consists of three stages as introduced above. However, the latch stage has a positive feedback mechanism in order to swiftly derive a comparison decision. Therefore, it is difficult to apply any adjustment either in the reset phase or in the comparison phase. The output stage is a pure digital implementation that does not have the ability to impact the result from the previous stages. The specially designed pre-amplifier is the only stage that is suitable for the compensation to be applied.

It is noted that a differential pair is used as the input stage of the amplifier. This reminded me of the compensation principles introduced in the Chapter 4. Since the floating-gate and the body-biasing techniques have become less attractive, the drain compensation principle is selected as the sources of MN4 and MN5 are used to reduce the static power consumption.

5.2.1.2 Circuit Description

In Figure 5.6 (a), two compensation transistors MP5 and MP6 are added to the drains of the differential input pair MN4 and MN5, respectively. Their gates are controlled by two capacitors C1 and C2. Both capacitors are initially charged to be V_{DD} that turns off both MP5 and MP6. An additional control signal "Comp" is used to decide whether the compensation is applied or not. Thus, the whole circuit will either operate in compensation phase $\phi 1$ or operational phase $\phi 2$. During the compensation phase, one corresponding capacitor will be discharged judged by the polarity of the offset voltage, whilst the other is held to V_{DD} . The offset voltage will be regarded as fully compensated when the output voltage polarity of the comparator flips. The voltage in the compensation capacitor will then be held for the rest of the operation.

The compensation circuit shown in Figure 5.6 (b) is used to distinguish the polarity of the offset voltage and to control the S1 and S2. It is implemented using a latch and two NAND gate (NAND_a and NAND_b). By testing the impact of MP5 and MP6 to the offset voltage of the comparator, it could be learned that if the V_{OUTA} is "0", the gate of C1 should be discharged to compensate the circuit mismatch. The C2 should be discharged if $V_{OUTB} = 0V$. Therefore, the output voltages from the buffer stage not only represent the

polarity of the offset voltage, but also can be used to control the compensation capacitors. As shown in Figure 5.6 (b), V_{OUTA} and V_{OUTB} are connected to C1 and C2 controlled by switches S1 and S2, respectively. Next, two NAND gates provide control signals "Ctrl1" and "Ctrl2" to switch the circuit between compensation phase $\phi 1$ and operational phase $\phi 2$. This is achieved by connecting both of the gates to the signal "Comp", where if "Comp" is "0", the circuit is in $\phi 2$. Both gates will result "1"s at their output. These output voltages will turn off two PMOS switches S1 and S2. Otherwise, the circuit is in $\phi 1$. One of the gates will be turned on to discharge a corresponding capacitor. The last part in the compensation scheme to be introduced is the latch that is used to hold the status of the output voltages of the main comparator. It is a VLSA circuit without reset and tail transistors, and is controlled by the "Flag" signal. After the V_{OUTA} and V_{OUTB} are sensed by the latch, their status will be held permanently by the latch without consuming any static power. Detailed plots of the key signals are illustrated in the Section 5.3.2 to further demonstrate the working principle.

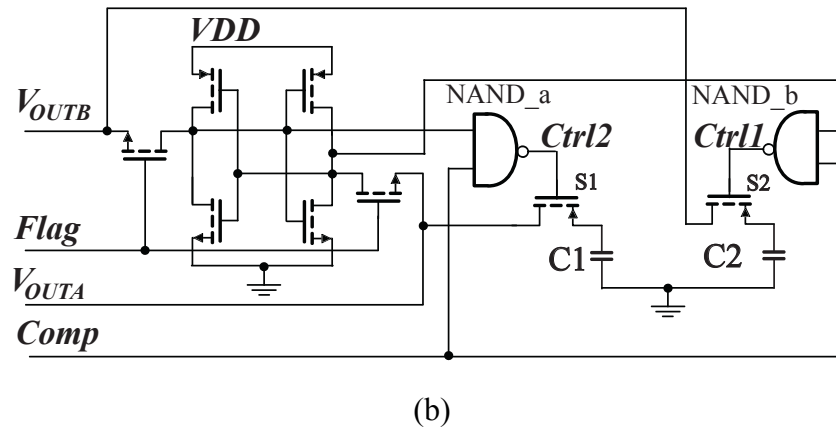
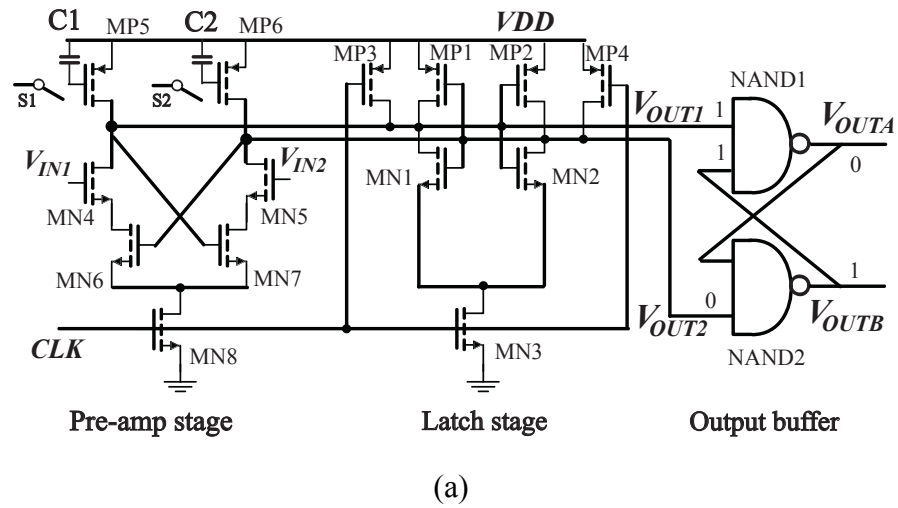


Figure 5.6 Proposed compensation scheme. (a) Two compensation transistors MP5 and MP6 are added to the drains of MN4 and MN5, respectively. (b) The compensation circuit is composed by a latch and two NAND gates. It is used to control the switches of S1 and S2.

5.2.2 Performance Evaluation

A fully functional comparator combined by a main comparator part and a compensation circuit part is proposed above. The functionality is evaluated by performing a transient analysis using HSPICE. The simulation setup is identical as the procedures introduced in the previous section. The 35 nm gate-length BSIM4 model card library was used, and the parasitic capacitances from source and drain regimes were taken into account during the simulation. The key signals of one randomised circuit are illustrated in Figure 5.7. Statistical analysis of the offset voltage using the binary search algorithm is performed with the compensation taken into account. The results of the offset voltage before and after compensation are presented as histograms at the end of this section.

5.2.2.1 Circuit Transient Analysis

As shown in Figure 5.7, the signals from important nodes of the whole circuit are illustrated. All of the signals are based on the same time frame, as shown at the bottom of the figure. The supply voltage of the comparator is 1 V. Figure 5.7 (a) shows that the clock signal "CLK" is operating at a speed of 15 GHz. The latch stage of the main comparator is reset when "CLK" is 0 V and operated when "CLK" is 1 V. During the simulation, the same common mode input voltage (0.5 V) is applied to the V_{IN1} and V_{IN2} of the main comparator, shown in Figure 5.6 (a). The V_{OUT1} and V_{OUT2} from the latch stage are plotted using blue and red curves in Figure 5.7 (b). These voltages result in two binary outputs at output buffer stage V_{OUTA} and V_{OUTB} , shown in Figure 5.7 (c). During the compensation phase ϕI (from 0 to 4ns shown in Figure 5.7 (d)), the latch in the compensation circuit has detects the values of the output voltages and locks this information for the switch control NAND gates. This process is finished within the first clock cycle and controlled using the "Flag" signal. Two switch control signals "Ctrl1" and "Ctrl2" are generated from the control NAND gates, shown in Figure 5.7 (e). Thus, two PMOS switch transistors S1 and S2 are turned on and off, respectively. The compensation capacitor C2 is still holding its original charge of 1 V, whilst C1 is discharged to overcome the impact of the offset voltage, shown in Figure 5.7 (f). After around 1ns, C1 has been discharged to around 0.8 V, flipping the output values of V_{OUTA} and V_{OUTB} . Since V_{OUTA} is still connected to C1 after its value flipping to "1" and S1 is still turned on, C1 is slightly re-charged back to maintain this compensation. After the compensation phase ϕI is over, both S1 and S2 are turned off. The charges in C1 and C2 are held for the operational phase that starts from 4 ns.

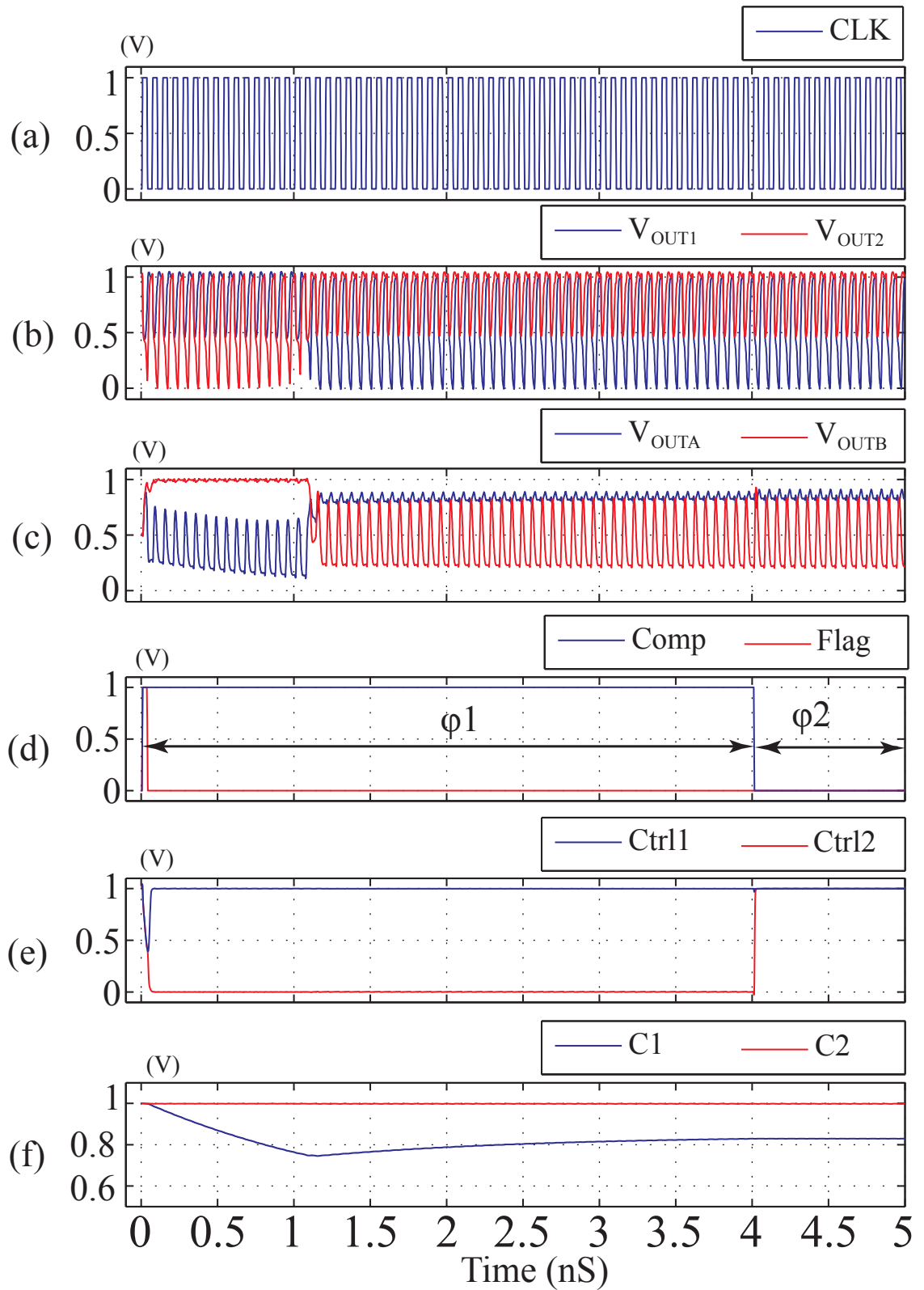


Figure 5.7 Transient analysis the compensated comparator. The simulation is divided into compensation phase ϕ_1 and operational phase ϕ_2 . (a) Clock signal at a speed on 15 GHz. (b) V_{OUT1} and V_{OUT2} from the latch stage. (c) V_{OUTA} and V_{OUTB} from the output buffer stage. (d) Two control signals "Comp" and "Flag" for the compensation circuit. "Comp" controls the whole circuit whether in compensation phase ϕ_1 or operational phase ϕ_2 . "Flag" controls the latch in the compensation circuit to hold the output polarity information. (e) Control signals "Ctrl1" and "Ctrl2" for the switches S1 and S2. (f) The charge stored in C1 and C2.

5.2.2.2 Offset Voltage Evaluation

Offset voltage evaluations of 2000 randomised netlists were carried out in the operational phase ϕ_2 using the binary search methodology presented in the previous section. Device variability has been taken into consideration for both the main comparator and the compensation circuit scheme by randomising every transistor. It should be pointed out that the main comparator before and after compensation is randomised using the same pseudo-random seed in order to make a fair comparison. The simulations were carried out with a supply voltage of 0.5 V and 1 V, at a speed of 4 GHz and 15 GHz. The evaluated results are plotted and compared using histograms as shown in Figure 5.8. In Figure 5.8 (a), the standard deviation of the offset voltage improves from 67.4 mV to 29 mV with a 0.5 V supply voltage and 4 GHz clock frequency. In Figure 5.8 (b), the same parameter has been improved from 43.1 mV to 20.3 mV when a 1 V supply voltage and 15 GHz clock speed were used. Uncompensated results are plotted in yellow.

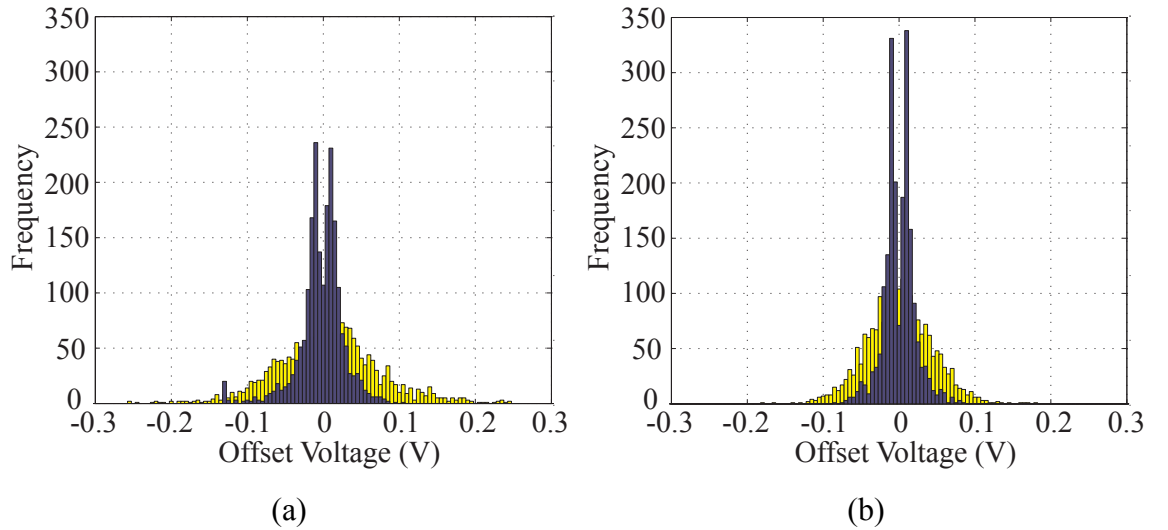


Figure 5.8 The histogram of the offset voltage of the comparator before and after compensation. 2000 randomised netlists are used as data sample. The uncompensated results are plotted in yellow, whilst compensated results are plotted in black. (a) The proposed comparator is tested using a 0.5 V supply voltage at a speed of 4 GHz. Standard deviation of the offset voltage has been improved from 67.4 mV to 29 mV. (b) The proposed comparator is tested using a 1 V supply voltage at a speed of 15 GHz. Standard deviation of the offset voltage has been improved from 43.1 mV to 20.3 mV.

5.3 Summary

The target of analogue circuit design in UDSM regime is to achieve high-speed and low-power designs using the well-established digital fabrication process, as it will reduce the fabrication cost and increase the integration of functionality on a single chip. However, the design precision will be degraded in contrast of the above advantages in UDSM regime, since the device variability significantly increases. A high-speed comparator is a typical analogue circuit that would be used under this design context. This impact will be further relayed to other parts of a large circuit block, for example a flash ADC. Furthermore, a high-speed comparator also suffers from other common limitations when using atomistic devices, for example scaled supply voltage.

In this chapter, a novel high-speed low-power comparator design using a 35 nm gate-length process has been proposed. The speed and power consumption was tested using HSPICE simulations. A binary search algorithm for evaluating the offset voltage of a comparator is proposed and implemented using MATLAB. During the simulation, the proposed comparator is randomised into 2000 netlists that have the same circuit arrangement but implemented using randomised transistor models. The comparator is simulated under two operation conditions: (a) 0.5 V supply voltage and 4 GHz clock speed and (b) 1 V supply voltage and 15 GHz clock speed. The comparator is fully functional under the above conditions with power consumptions of 0.28 mW and 15 μ W, respectively. The standard deviations of the offset voltage from a data set of 2000 under the same testing conditions are 67.4 mV and 43.1 mV, respectively.

It is noted that compared with the excellent speed and power performance, the offset voltage limits the application of the comparator. Improvements can be achieved by using compensation circuit attached to the main comparator. In Section 5.2, a custom designed compensation scheme is presented. After the evaluations under the same test bench, the offset voltage has significantly improved from 67.4 mV to 29 mV and from 43.1 mV to 20.3 mV. An excellent balance between speed, power and accuracy has been achieved. This compensated comparator will be used as a part of a flash ADC that will be presented in the next Chapter.

Chapter 6 Impact of Variability on High Performance ADC Design

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6.1 High-Speed Flash ADC Design

Analogue-to-digital converters that operate within the X-band frequency range (8-12 GHz) are critical circuit blocks for a wide range of the high-speed wired and wireless communication applications, such as software defined radio [120, 121], radar signal capture [122] and fibre-optical receiver [123]. These applications necessitate the next generation receiver to have high sampling rate and low-power consumption in order to fulfil the requirements of handheld equipment. Within the receiver, the high-speed low-power ADC can be attached to the front-end in order to take advantage of the high computing power of a digital signal processor. The majority of signal processing can then be performed in the digital domain. Many high-speed ADCs have been designed and published in the past [121, 122, 124]. However, these solutions are implemented using different process technologies, such as InP, SiGe and BiCMOS, with a relatively high power consumption and large die area. These factors prevent them from being integrated in a single chip with other digital blocks. On the other hand, owing to scaling of the CMOS transistor, it is now possible to design a high-speed ADC using the same standard CMOS process as for digital blocks. Therefore, a single chip receiver solution will significantly reduce the cost compared with multi-chip solutions.

In the previous Chapter, a high-speed low-power comparator was proposed and simulated in 35 nm CMOS. A custom designed compensation scheme was also introduced to reduce the offset voltage of the comparator. The proposed comparator with compensation scheme can be further used in designing system-level blocks, such as ADCs. During the designing of an ADC, many design targets and requirements are commonly desired to be achieved, for example low power consumption, low noise level, small silicon layout area, high conversion speed and high resolution. However, in practice, these targets cannot be obtained simultaneously. One characteristic can usually be improved at a cost of sacrificing others. For example, the high conversion speed of an ADC can be achieved using the UDSM technologies because smaller transistors have a higher unity current gain frequency. However, the achievable resolution will be degraded, because the increased device variability will reduce the matching performance at the transistor-level. This imperfection will be relayed from the basic analogue cells to the system-level ADC block. On the other hand, if mismatch compensation solutions can be found at the transistor or circuit level without reducing the circuit speed, the matching performance of the system-level blocks can be enhanced if these solutions are used.

To illustrate this possible improvement, the proposed high-speed comparator with the compensation scheme in Chapter 5 is used as an example of using circuit-level solution to overcome the mismatch problem of a system-level ADC. After reviewed the existing ADC structures, such as flash, pipeline, successive approximation and oversampled approaches, flash ADC structure has the highest conversion speed that is suitable for the high-speed applications. It is arguable that the flash ADC will consume more silicon area than other architectures, since the number of comparators required will be doubled if the resolution is increased by 1 bit. However, this will not be a major concern for the high-speed applications in design practice, as the resolution requirement is quite low (less than 4 bits). Therefore, flash ADC architecture will be used in this chapter to demonstrate the matching performance improvements at the system-level in 35 nm CMOS.

In the first section of this Chapter, the proposed 3-bit flash ADC at 10 GSample/s will be discussed in detail. Two different comparator circuits will be used to build the ADC. As the comparator introduced in Chapter 5 has NMOS transistors at the input stage, it will be called as N-type comparator and used for the input voltage range from 0.5 V to 1 V. This is because this circuit, as is the case with all circuit of this type, is not suitable for use with the input range in the lower half of the supply range (i.e. 0 V ~ 0.5 V). Moreover, a complementary comparator is designed using PMOS transistors at the input stage. This circuit will be named as P-type comparator and could operate from 0 V ~ 0.5 V. By combining these two comparators in the proposed ADC design, a full-scale input range can thus be enabled. The main static characteristics of the flash ADC will be estimated by applying the histogram test method. These characteristics include the offset voltage, the gain error, the differential nonlinearity (DNL) and the integral nonlinearity (INL). The dynamic characteristics are evaluated using the Discrete Fourier Transform (DFT) method. The frequency of signal and high-order harmonic distortions can be obtained by analysing the output codes of the flash ADC. In the Section 6.2, an improved 3-bit flash ADC is built using a combination of both P-type and N-type comparators with their custom-designed compensation schemes, respectively. Both static and dynamic characteristics of the improved flash ADC will be evaluated using the same approaches as in the Section 6.1. Furthermore, 1000 Monte Carlo simulations will be carried out for both of the uncompensated and compensated ADCs. By statistically comparing their static and dynamic characteristics, the operation accuracy improvements of the compensated ADC can be observed.

6.1.1 Proposed High-Speed Flash ADC

Due to its parallel processing mechanism, flash ADC has the highest conversion speed over other ADC architectures. The conversion speed can be maximised by using the smallest available gate-length devices. At the same time, the resolution is limited by the scaled supply voltage and the increased statistical device variability. The least significant bit (LSB) that determines the minimum voltage difference that a flash ADC can distinguish is equal to $V_{REF}/2^N V$, where V_{REF} is the reference voltage and N is the number of bits. During design, if the standard deviation of the offset voltage for a comparator is defined as σ_{OFFSET} , the LSB should be equal to or larger than $3\sigma_{OFFSET}$ in order to maintain a large enough design margin. Based on these criteria, the high-speed comparator proposed in the Chapter 5, whose $\sigma_{OFFSET} = 43 \text{ mV}$, can almost fulfil the requirements of a 3-bit flash ADC with a reference voltage of 1 V, whose $LSB = 125 \text{ mV}$. Despite the intention of integrating this ADC with other digital circuits on the same die, this ADC will be simulated without the existence of any other digital block. As the target of this chapter is to investigate the impact of variability on the system-level analogue blocks, in this case a flash ADC, the imperfection from other sources will not be taken into account, such as the supply voltage fluctuations and resistor-induced variations.

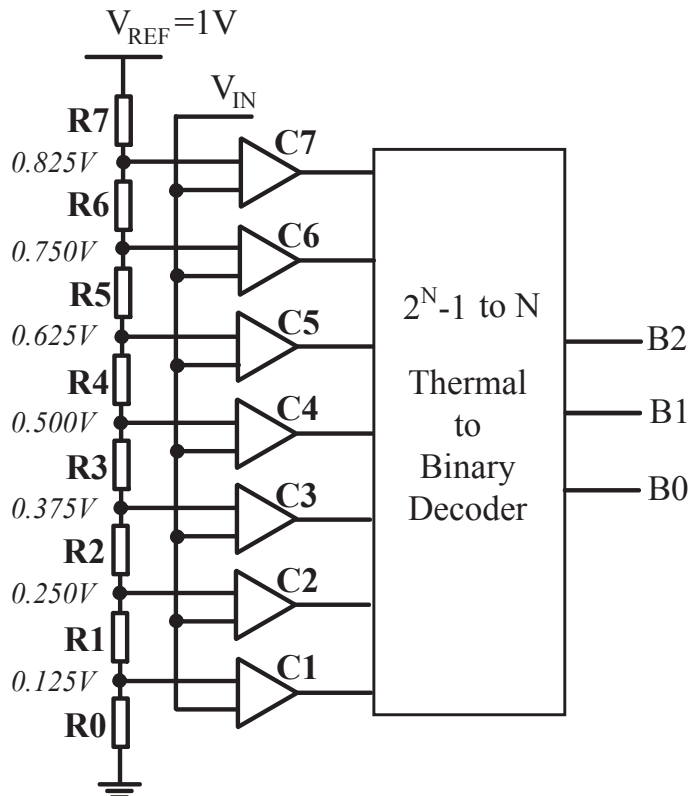


Figure 6.1 The schematic of the proposed 3-bit 10 GS/s flash ADC.

6.1.1.1 ADC Schematic

The schematic of the proposed flash ADC is shown in Figure 6.1. The reference voltage is 1 V that has the same value with the supply voltage. A resistor ladder is used to divide the reference voltage into $2^N - 1$ different values, in this case $N = 3$ bits. Each value is then fed into a corresponding comparator (C1 to C7). The P-type comparator is used for C1 to C3, whilst the N-type comparator is used for C4 to C7. After applying an analogue input signal V_{IN} simultaneously to all the comparators, a 7-digit thermometer code will be generated and interpreted into a 3-bit binary code using the thermometer-to-binary decoder. The thermometer code can represent 8 different voltage levels. The levels below the V_{IN} have a value of "1" and all above are "0".

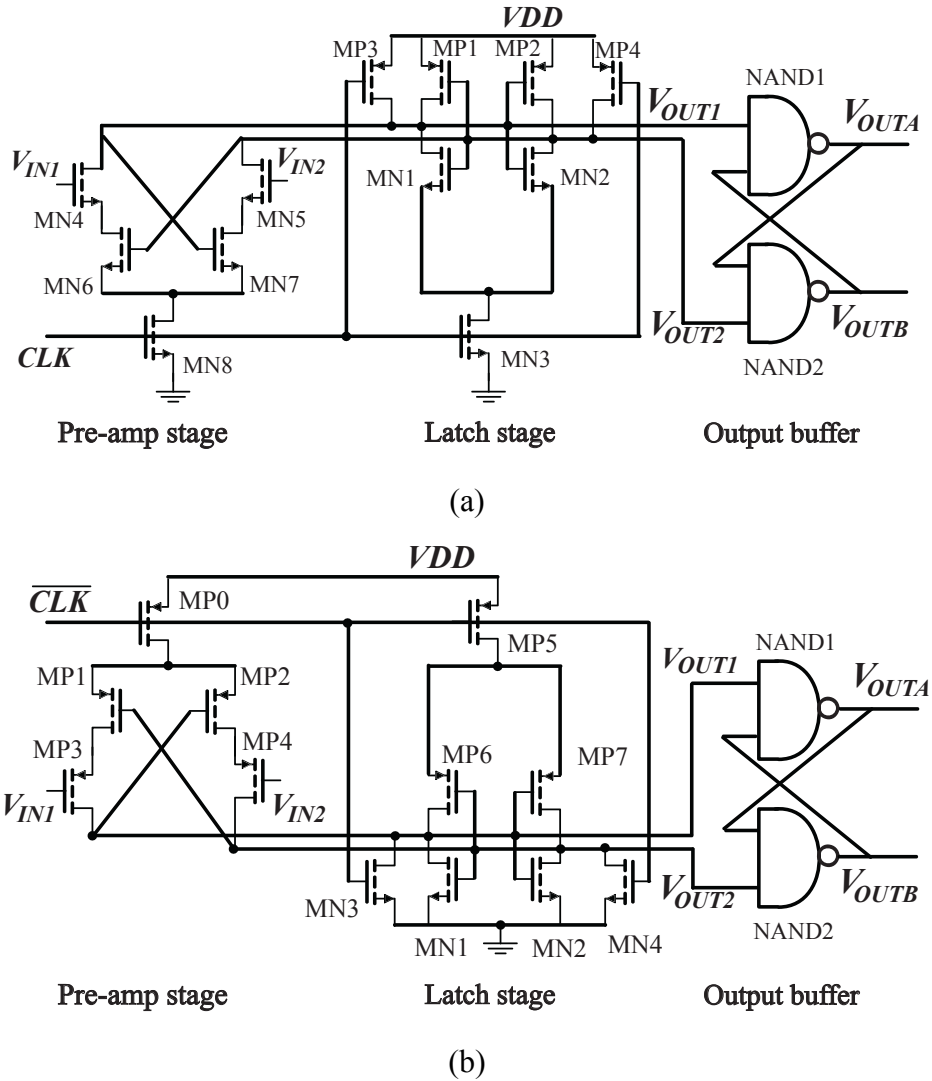


Figure 6.2 Comparator schematics used in the proposed 3-bits 10 GSample/s flash ADC. (a) N-type high-speed comparator. (b) P-type high-speed comparator.

6.1.1.2 Comparator Schematics

In Figure 6.2, the schematics of both N-type and P-type comparators are illustrated. As shown in Figure 6.2 (a), the input differential stage of the N-type comparator is implemented using NMOS transistors (MN4 and MN5), it will not give an accurate comparison result if the input voltage is lower than the threshold voltage (i.e. 0 V to 0.255 V), because both MN4 and MN5 will not be turned on until the input voltage exceeds the threshold voltage. From system point of view, the achievable input range of the ADC will thus be limited. To extend to a full-scale input range, a complementary design of comparator is introduced in Figure 6.2 (b). Two PMOS transistors MP3 and MP4 are used to compose the differential input stage of the pre-amplifier. Current control transistors MP1 and MP2 are connected to the source of the input pair. Controlled by the clock signal " \overline{CLK} ", the tail transistor MP0 is placed between MP1-MP2 and supply voltage (V_{DD}). The signal " \overline{CLK} " has the same speed and amplitude as the system clock signal " CLK ", but with a 180-degree phase shift. In the latch stage, reset transistors MN3 and MN4 are used to control the latch comparator (MN1-MP6 and MN2-MP7). The operation of the tail transistor MP5 is synchronised with the reset transistors MN3 and MN4 by the " \overline{CLK} ". Similar to the comparator in Figure 6.2 (a), two NAND gates are used as output buffer to provide binary outputs. It is noted that if only N-type comparator is used for all the comparators (C1 to C7), the ADC could run at a clock speed of 15 GHz. However, due to the slower speed of PMOS transistors, the clock speed of the complementary system is reduced to 10 GHz in order to satisfy the timing constraints.

6.1.2 Static Characteristics Evaluation

The static characteristics of an ADC are used to measure the quality of the signal conversion process. Primary static parameters include: the resolution, the offset voltage, the gain error, the differential nonlinearity (DNL) and the integral nonlinearity (INL). The resolution of an ADC indicates the smallest analogue value that can be distinguished. It can be calculated using the number of bits N of an ADC. The offset voltage of an ADC is defined as the lateral shift between the measured and the ideal transfer curves. The gain error describes the difference between the ideal and measured gain slopes. The DNL of an ADC output code is defined as the width difference between the ideal and the measured conversion steps. The INL of an output code can be calculated by adding up all the DNL values of the previous output codes. However, because there is no silicon measurement in this research, the measured transfer curve mentioned above will be replaced by the

simulated transfer curve from the HSPICE. Each simulated curve accurately represents that found in a physical circuit implementation. In this chapter, the evaluation of these static characteristics will be accomplished by using the histogram test method.

6.1.2.1 Histogram Test Method

The histogram test method is a widely used approach in evaluating the static characteristics of an ADC. The basic principle of this approach is to apply a slowly increasing ramp signal at the input of the flash ADC V_{IN} and count the number of the generated output codes within a certain length of time. For an N-bit ADC, there are 2^N different output codes in total. If each code is assigned to a dedicated bin, the number of counts in each bin can represents the width of each conversion step. For example, in the estimation of the proposed 3-bit flash ADC, a ramp signal is configured to linearly vary from 0 V to 1 V for 40 ns. As the system clock speed is 10 GHz, the ADC will generate 10 digital codes for every 1 ns. A total of 400 codes will be generated for all 8 conversion steps for the duration of 40 ns. To choose the duration of input signal as 40 ns is based on the computing power of the Linux workstation. The workstation has 4 GB memory and an AMD 2.6 GHz dual core processor. It requires 20 minutes to simulate one ADC netlist with the above experiment settings. One simulation output file consumes about 8 MB disk storage. As illustrated in Chapter 4, the statistical results of a circuit under test will be converged after 1000 simulations, which is also true for the ADC estimation. To simulate 1000 randomised ADC netlists, it would take about 14 days to finish the simulation and will consume 8 GB of disk storage. Therefore, the choice of 40 ns is reasonable according to the computing power of the machine. Furthermore, it can provide an adequate accuracy as well.

In the ideal case of a 3-bit ADC, there will be 50 counts in each output code bin, as shown in Figure 6.3 (a). This bin size of 50 counts represents one ideal step width of the transfer curve that is also equivalent the value of LSB. Therefore, each count can represents a voltage change of $0.125 \text{ V} / 50 = 2.5 \text{ mV}$ of V_{IN} . However, due to the impact of device variability on the accuracy of each comparator, the output codes will not be uniformly distributed among 8 bins. For example, an flash ADC netlist with variability taken into account is simulated and plotted in Figure 6.3 (b). As the counts in each code bin present the actual width of the conversion step, the transfer curves of the ideal and the randomised ADC can then be reconstructed using the information from Figure 6.3 (a) and (b). In Figure 6.4, the comparison between the transfer curves are plotted, where the blue stair represents the ideal transfer curve and red curve shows the simulation data.

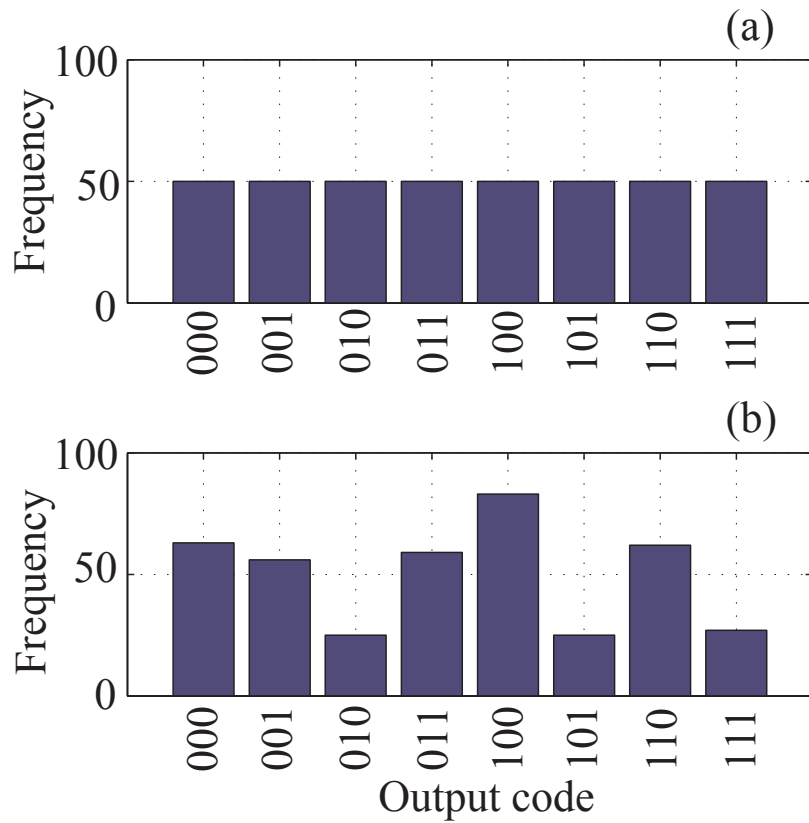


Figure 6.3 Histogram of the output codes. (a) In the ideal case, 50 identical output codes will be counted for each bin where the bin numbers represent the output codes. (b) In a simulated case, the counts vary between each bin.

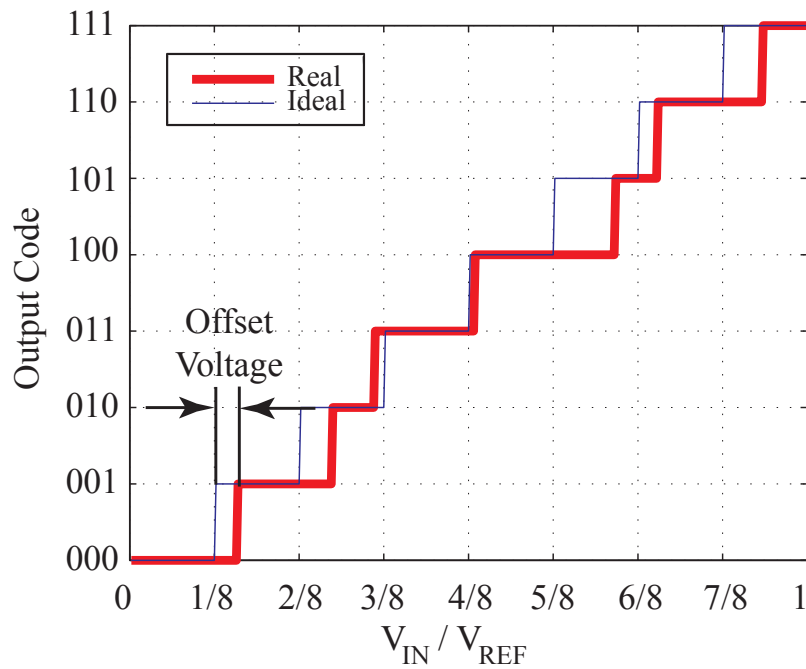


Figure 6.4 Transfer curves from the simulations of an ideal and a simulated ADC with variability taken into account. The red curve represents the simulated data of the simulated 3-bit flash ADC. The blue line represents the ideal transfer curve of the ADC. The offset voltage is highlighted in this figure as well.

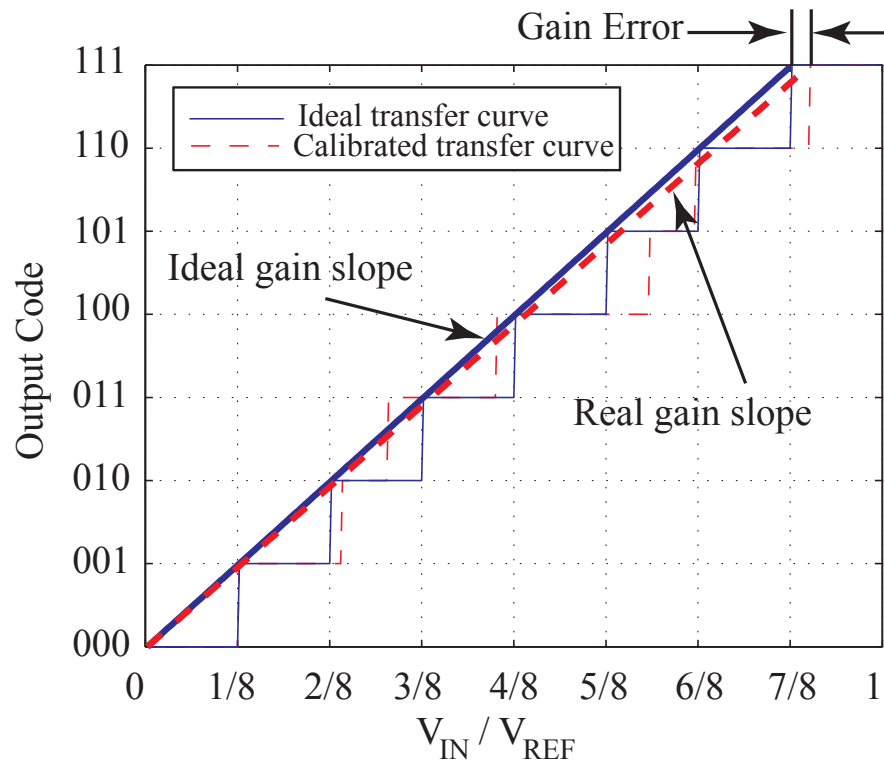


Figure 6.5 Plot of gain error of a flash ADC. The gain error is the measured using the ideal gain slope as a reference. After the offset voltage is eliminated, the real gain slope is obtained by connecting the first and the last transition points.

6.1.2.2 Offset Voltage and Gain Error

From the transfer curve shown in Figure 6.4, the offset voltage of a randomised ADC can be observed. It is defined as the lateral shift between the ideal curve and the measured curve, and calculated as the width difference of the first conversion steps between two transfer curves. The magnitude of the offset voltage is normally measured using the unit of LSB. The offset voltage in Figure 6.4 of a real ADC is 0.26 LSB. After 1000 statistical simulations, the standard deviation of the offset voltage for the proposed ADC schematic is 0.37 LSB.

Gain error is another static parameter to describe the imperfection of an ADC. It is defined as the difference between the ideal simulated gain slopes. Before calculating the gain error, the offset voltage should be calibrated first, so both ideal and simulated gain slope have the same starting point, as shown in Figure 6.5. The offset voltage is calibrated by shifting the simulated transfer curve to the left by 0.26 LSB. The calibrated transfer curve is plotted using the dashed red line in Figure 6.5. The gain slope is obtained by connecting the first and the last transition points of the transfer curve that can be found on the edge of the first

and last conversion steps. The ideal and simulated gain slopes are illustrated using thick solid blue line and thick dashed red line in Figure 6.5, respectively. The gain error is calculated at the end of two lines in the unit of LSB. In this case, the gain error is 0.2 LSB. The larger the input voltage is, the larger the output error will be. As an important static parameter, the statistical information of the gain error is important. Based on the 1000 randomised simulation results obtained above, the standard deviation of the gain error is 0.61 LSB.

6.1.2.3 Differential Nonlinearity

Differential nonlinearity is another important static parameter used to describe the variations of every single conversion step of an ADC. It is defined as the lateral differences between the ideal and simulated conversion steps for each output code, where the width of an ideal step is equal to 1 LSB. By using histogram test method, the step width variation is calculated by the difference between the number of counts of the ideal and simulated data, where the ideal counts for each code bin is 50. Therefore if the number of counts in each bin from the simulated data is assumed to be N_i , where i represents the bin number, the DNL of each code is then given by:

$$DNL_i = (N_i - 50)/50 . \quad \text{Eq. (6.1)}$$

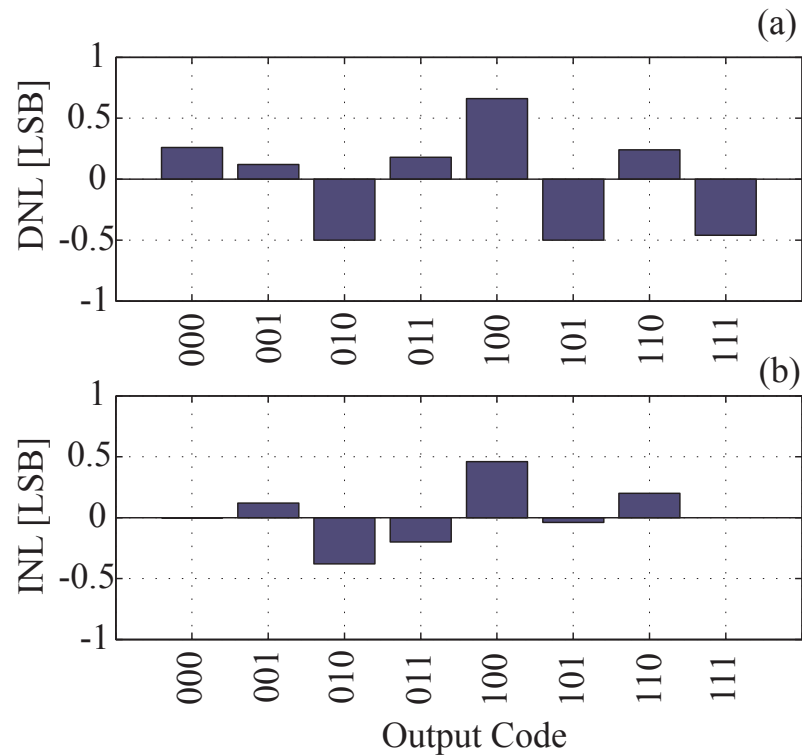


Figure 6.6 (a) the DNL and (b) the INL of a randomised 3-bit 10 GSample/s flash ADC.

Based the transfer curve shown in Figure 6.4, the DNL of each output code can be calculated. The DNL values are listed in Table 6.1 and plotted in Figure 6.6 (a). In this example, the maximum DNL is 0.66 LSB and the minimum DNL is -0.5 LSB. During design, the maximum absolute values of DNL (DNL_{Max}) are used to reflect the fidelity of an ADC. A good design will require the DNL_{Max} less than 0.5 LSB. Based on the 1000 Monte Carlo simulations of this ADC, only 22.4% have met the criterion.

Table 6.1 DNL data of the example ADC.

DNL1	DNL2	DNL3	DNL4	DNL5	DNL6	DNL7	DNL8
0.26	0.12	-0.50	0.18	0.66	-0.5	0.24	-0.46

6.1.2.4 Integral Nonlinearity

Integral Nonlinearity is used to measure the lateral difference between the transition points of a simulated ADC and the ideal gain slope with no offset and gain error. The physical representation of INL can be observed from the evaluation in Figure 6.5. In practice, INL can be obtained from DNL values. This is because the INL value of one output code arises from the accumulation of the previous non-ideal step widths. Therefore, the INL value of a transition point i can be given by:

$$INL_i = \sum_{n=2}^{i-1} DNL_n, i \neq 1 \text{ and } 2^N. \quad \text{Eq. (6.2)}$$

It is noted that during the calculation of INL, the DNL of first code and the last code will not be used, because offset and gain error are neglected. The INL values of the given example are listed in Table 6.2 and visualised in Figure 6.6 (b). The maximum INL is 0.46 LSB and the minimum INL is -0.38 LSB. A good design will require the absolute value of maximum and minimum INL less than 0.5 LSB as well. Based on the 1000 Monte Carlo simulation results used above, only 46.5 % of the ADC netlists have met the criterion.

Table 6.2 INL measurement of the example ADC.

INL1	INL2	INL3	INL4	INL5	INL6	INL7	INL8
0	0.12	-0.38	-0.20	0.46	-0.04	0.20	0

6.1.3 Dynamic Characteristics Evaluation

Dynamic characteristics of an ADC are normally referred as the frequency domain information of the signals, the noises and the harmonic distortions. The information can be analysed by applying Discrete Fourier Transform (DFT) to the finite time domain output digital code. Besides the unavoidable thermal noise and flicker noise of the circuit, quantisation noise will be inevitably introduced when converting the continuously-valued analogue signal into a finite-valued digital code, even if the ADC is ideal. Furthermore, unwanted harmonic distortions will be introduced by the nonlinearity of the ADC.

The evaluation of the dynamic characteristics should be carried out by applying a sine wave test signal with full input range amplitude and a frequency less than half of the sampling frequency. Based on this input signal, a finite output digital code segment from the ADC can be collected and analysed using DFT algorithm. In this section, the principle of the DFT method will be introduced. The limitation of the DFT method will also be illustrated. One example from 1000 Monte Carlo simulations of the ADC will be used to demonstrate how to apply DFT for the proposed ADC. The results of signal-to-noise-and-distortion ratio (SINAD), total harmonic distortion (THD), spur free dynamic range (SFDR) and effective number of bits (ENOB) will be analysed. Furthermore, the statistical information of the above parameters will be analysed based on the 1000 simulation results.

6.1.3.1 Discrete Fourier Transform Testing Methodology

Analogue-to-digital conversion is a process that involves signal sampling and quantisation. According to Nyquist sampling theory, the information of the input signal can be perfectly reconstructed if the sampling frequency is higher than twice of the highest frequency component of the original signal. Based on a finite length output code, the DFT algorithm is an efficient approach to analyse the frequencies of the signal and harmonic distortions and the power spectrum density of the noise. The efficiency of the algorithm can be boosted if the data length is equal to an integer power of 2. If this is the case, the algorithm is also widely known as Fast Fourier Transform (FFT). In this thesis, a segment of 1024 data points will be generated by carefully selecting the sampling frequency. The FFT will be performed to the output data segments of the proposed ADC in the frequency domain.

6.1.3.2 Frequency Leakage Problem

During the analysis process, attention is paid to the well-known frequency leakage problem when FFT is applied. If the experiment is not carefully configured, the output data from the ADC will lead to a significant frequency domain distortion by using the FFT algorithm. The frequency leakage arises as the DFT implicitly assumes that the sample block will be repeated every N data samples, where N is the code length from an observation window. If the signal period is not an integer within the observation window, a discontinuity at the sample block boundary will occur. The energy from the signal bin will be spread into other frequency bins, referred as the frequency leakage. As shown in Figure 6.7 (a), one cycle of the sine wave is sampled using 8 data points within the observation window. On contrast, the observation window contains 1.5 cycle of the same signal in Figure 6.7 (b). Figure 6.7 (c) shows the frequency of above two signals where the leaked signal is highlighted in red.

The problem can be addressed by either select an integer number of sinusoid cycles in each block, or use windowing method to reshape the input signal in order to attenuate the leakage. In this thesis, the first approach is selected. In order to avoid the problem, the input signal is set to be 1.25 GHz with a full-scale (0 V to 1 V) amplitude in this research. With a sampling rate of 10 GSample/s, there will be 8 data sample points in each sine wave cycle. For a 1024-point FFT analysis, a total of 128 cycles will be included within the 1024 points observation window.

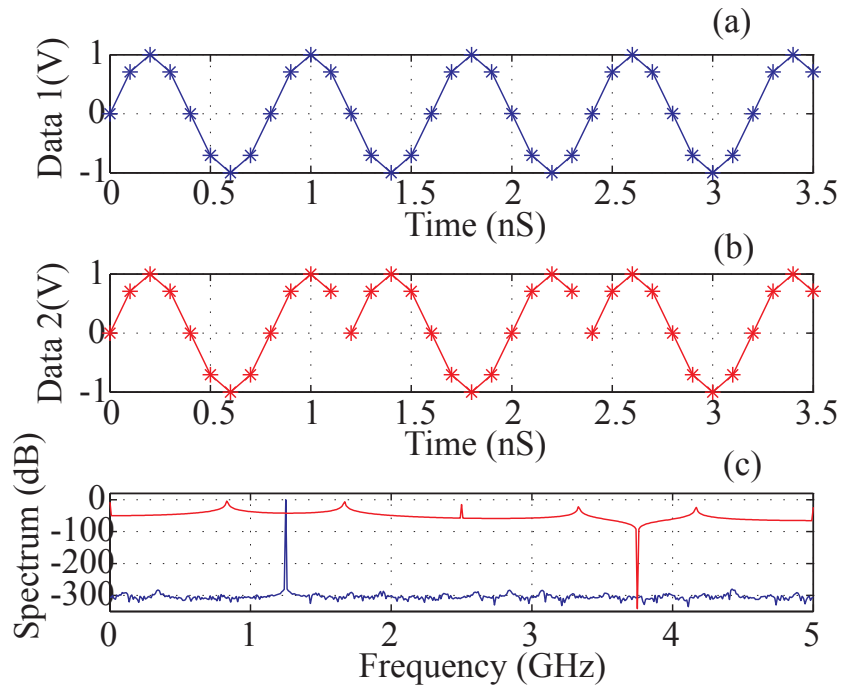


Figure 6.7 Frequency leakage problem. (a) Continuous signal. (b) Discontinuous signal. (c) Frequency spectrum.

6.1.3.3 Signal and High Order Distortion Analysis

As shown in Figure 6.8 (a), a sampled and quantised signal is reconstructed based on the output code of a randomised ADC. As mentioned in the Section 6.1.3.2, the input signal frequency is set to be 1.25 GHz. A segment of 128 cycles of data was collected for FFT analysis where each cycle contains 8 data points. A total of 1024 data points is collected for FFT analysis. However, as shown in Figure 6.8 (a), the bottom part of the reconstructed signal has been distorted due to the device variability. This distortion can also be observed in the frequency spectrum as harmonic distortions. In Figure 6.8 (b), a single side spectrum of a 1024-point FFT analysis is illustrated. The frequency range is from 0 to 5 GHz. In Figure 6.8 (b), the two peaks on the left hand side are the power of DC voltage and input signal that are -1.16 dB and -7.78 dB, respectively. The other two peaks on the right hand side are the high order harmonic distortions HD_1 and HD_2 whose power are -24.08 dB and -29.50 dB. The total harmonic distortion (THD) is used to describe the magnitude of the ADC signal distortion, and is expressed by the ratio of the signal power to the mean value of the root-sum-square of its harmonics. In this example, the THD is 18.22 dB. Despite their existence during the real silicon measurement, thermal noise and flicker noise are not considered in this case during the computer simulation. Therefore, total signal to noise ratio (SNR) will be the same as the signal to quantisation noise ratio (SQNR), that is calculated as $6.02 \times N + 1.76 = 19.82$ dB. The spurious free dynamic range (SFDR) is defined as the difference between the signal power and the highest distortion power, which in this case is 16.31 dB. Signal-to-noise and distortion ratio (SINAD) can be calculated based on SNR and THD, as shown in Appendix A, giving:

$$SINAD = -10\log_{10} \left(10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}} \right) = 15.94 \text{ dB} \quad \text{Eq. (6.3)}$$

Based on the value of SINAD, the effective number of bits (ENOB) in this case is then expressed as:

$$ENOB = \frac{SINAD - 1.76}{6.02} = 2.36 \text{ bits} . \quad \text{Eq. (6.4)}$$

The ENOB is one of most important dynamic parameter that can describe the fidelity of the ADC. It is used as a straightforward metric to reflect the impact of the distortion and the noise on the performances of the ADC. The distortions can be regarded as neglectable

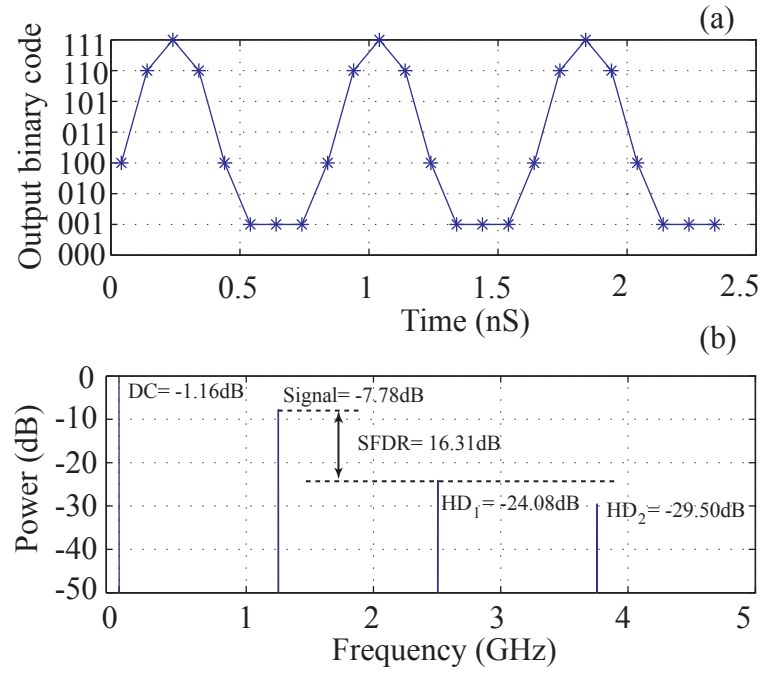


Figure 6.8 Output power spectrum of a randomised 3-bit 10 GS/s flash ADC. (a) The reconstructed output signal. (b) The power spectrum of the signal in (a) analysed by FFT.

when the THD is equal or lower than the SNR, as the power of the distortions are less than the noise level. When the THD is equal to SNR for the 3-bit ADC, the ENOB is 2.5 bits. Therefore, it can be regarded as a good ADC netlist if its ENOB is equal or higher than 2.5 bits. After 1000 Monte Carlo simulations, only 46 % of the ADC netlists have met this criterion.

6.2 High-Speed Flash ADC with Comparator Compensation Scheme

In the previous section, a 3-bit 10 GS/s flash ADC has been designed using 35 nm CMOS. The histogram test method and the FFT method were introduced and applied to estimate the static and dynamic characteristics, respectively. Based on the proposed ADC schematic, 1000 Monte Carlo simulations have been carried out using HSPICE. The statistical estimations of the critical parameters, such as DNL and ENOB, are poor. This degraded performance of the ADC can be tracked back to the mismatch of the proposed high-speed comparator at circuit-level. On the other hand, as presented in Chapter 5, the matching performance of the N-type comparator was improved by using a custom designed compensation scheme. The standard deviation of the offset voltage was reduced from 43 mV to 20 mV. Therefore, the presented 3-bit flash ADC could benefit from the

proposed compensation scheme. In this Section, the compensation scheme will be added to the N-type comparator. A new compensation scheme for P-type comparator will be designed. Based on the same 3-bit ADC structure in Figure 6.1, a combination of P-type and N-type comparators with compensation schemes will be used to rebuild the high-speed ADC. A comparison of critical performances of the flash ADC before and after compensation will also be discussed in this section.

6.2.1 Comparator with Compensation Scheme

In Figure 6.9, the N-type high-speed comparator and its compensation scheme are illustrated. Figure 6.9 (a) shows the proposed N-type high-speed comparator. Two compensation transistors MP5 and MP6 are added to the pre-amplification stage. These two transistors are controlled by the custom compensation scheme illustrated in Figure 6.9 (b). The detailed mechanism of compensation has been introduced in Chapter 5. However, it is noted that even after the compensation scheme is applied, the input voltage range is still limited by the threshold voltage of the differential input pair (MN4 and MN5). In the previous section, this problem is addressed using a complementary P-type comparator,

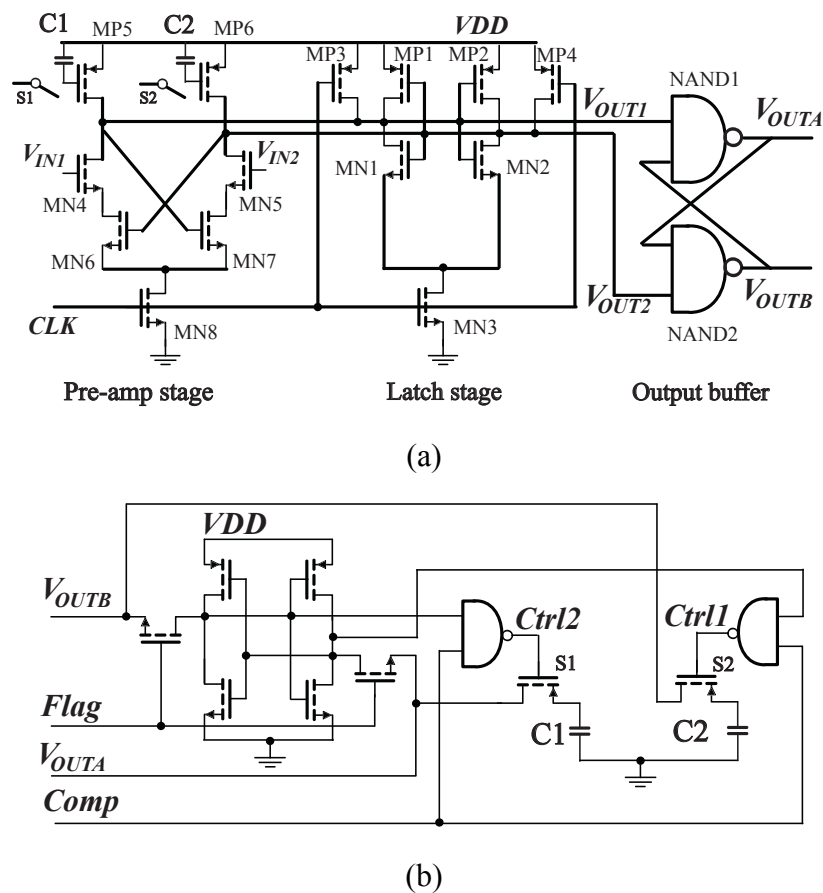
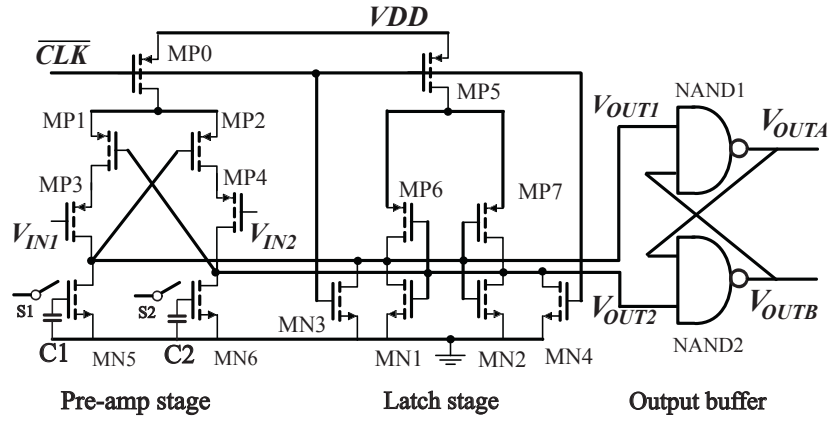
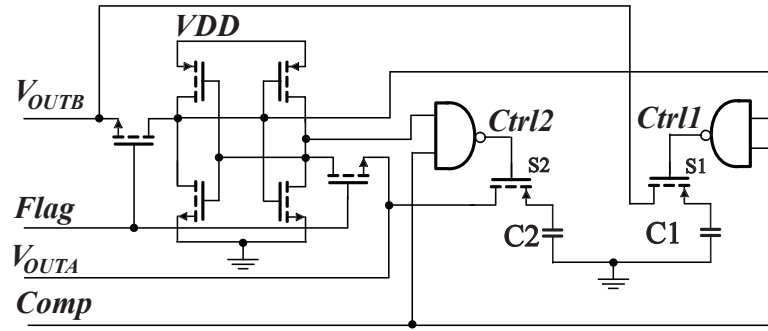


Figure 6.9 Compensation scheme for the N-type high-speed Comparator. (a) The schematic of the N-type comparator. (b) The schematic of the custom designed compensation circuit.



(a)



(b)

Figure 6.10 Compensation scheme for the P-type high-speed Comparator. (a) The schematic of the P-type comparator. (b) The schematic of the custom designed compensation circuit.

whose schematic is presented in Figure 6.10 (a). Meanwhile, a compensation scheme will also be needed, as the P-type comparator is not immune from the impact of device variability. In Figure 6.10 (a), two compensation transistors (MN5 and MN6) are connected to the drain of the input pair MP3 and MP4. The gates of MN5 and MN6 are controlled by capacitors C1 and C2, both of which are initialised to the ground at the beginning of the compensation phase. The compensation circuit used to control C1 and C2 are illustrated in Figure 6.10 (b). During the compensation phase, the polarity of the offset voltage of the P-type comparator is detected by comparing the output voltages V_{OUTA} and V_{OUTB} . This information is hold by the latch circuit in Figure 6.10 (b). Furthermore, two complementary control signals are generated according to the polarity information for the switches S1 and S2. For example, if the offset voltage is positive, the V_{OUTA} will be higher than V_{OUTB} . The control signals will turn on S1 to charge C1, whilst keep S2 off to maintain C2 as uncharged. At the end of compensation phase, S1 and S2 will switch off to hold the acquired compensation voltages in C1 and C2. The N-type comparator with compensation scheme will be used as C4 to C7 in the flash ADC structure, as shown in Figure 6.1. The P-type comparator with compensation scheme will be applied to C1 to C3.

Two extra control signals "Comp" and "Flag" signals will need to be introduced for both comparators. The signal "Comp" is used to control whether the circuit is in compensation phase or operation phase. The signal "Flag" is used to control the latch circuit in the compensation scheme to hold the offset polarity information.

6.2.2 Static Performance Evaluation

For the improved 3-bit flash ADC with compensation scheme, the major static parameters are estimated using the same methodology presented in the Section 6.1. These parameters include the offset voltage, the gain error, the DNL and the INL. One of 1000 Monte Carlo simulations for the improved ADC will be selected as an example to demonstrate the performance improvement compared with the example in the previous section. During the simulation, the compensation phase is set to be 3 ns. Therefore, during the first 3 ns, the ramp signal has the same value as the reference voltage from the resistor ladder for compensating the corresponding comparators. After the compensation phase is over, the ADC enters operation mode. The value of the ramp signal changes from reference voltage to 0 V at 3.1 ns, and vary from 0 V to 1 V. It takes a total of 40 ns for the ramp signal to reach 1 V at 43.1 ns. Compare with Figure 6.3, the output code histogram is much closer to the ideal case, as shown in Figure 6.11.

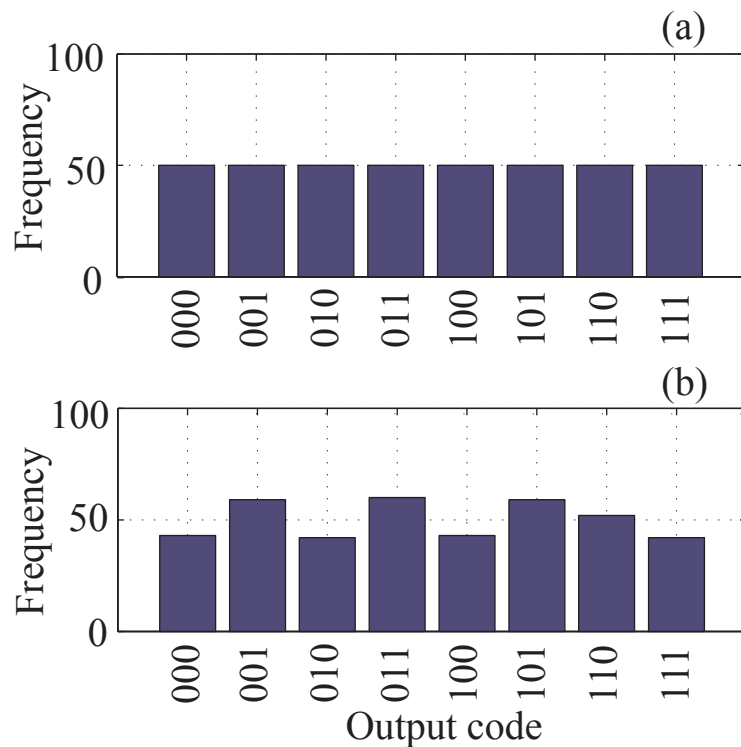


Figure 6.11 Output code histogram. (a) In an ideal case, 50 output codes will be counted for each bin. (b) In a real case, this number of counts varies between each bin.

6.2.2.1 Offset Voltage and Gain Error

In Figure 6.12, the transfer curves of both the ideal case and the simulated example are plotted according to the histogram in Figure 6.11. The offset voltage in this case is -0.14 LSB. After estimating 1000 randomised ADC netlists, the standard deviation of the offset voltage is 0.23 LSB, where the same number for the uncompensated ADC is 0.37 LSB. The improvement of the standard deviation of the offset voltage is 38% . In Figure 6.13, the offset voltage is calibrated by shifting the entire transfer curve to the right by 0.14 LSB, and plotted using dashed red line. The ideal gain slope and the simulated gain slope are obtained by connecting the transition points of the first and the last conversion steps of both transfer curves. Both of the slopes are highlighted using thick lines as shown in Figure 6.13. The gain error in this case has a value of -0.3 LSB. The estimation procedure has been repeated for the ensemble of the randomised ADC netlists. The standard deviation of the gain error is 0.42 LSB, where LSB is equal to 0.125 mV for a 3-bit ADC. An improvement of 33% has been achieved in the standard deviation of the gain error, where the same number for the uncompensated ADC was 0.61 LSB.

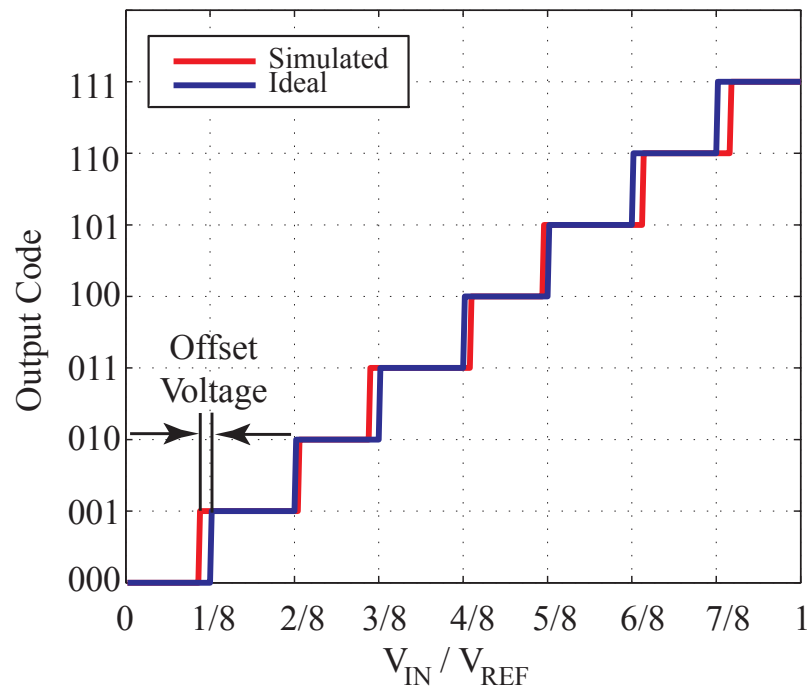


Figure 6.12 Transfer curves from the measurements of an ideal and the improved flash ADC. The red curve represents the simulated data of a randomised 3-bit flash ADC. The blue line represents the ideal transfer curve of the ADC. The offset voltage is highlighted in this figure.

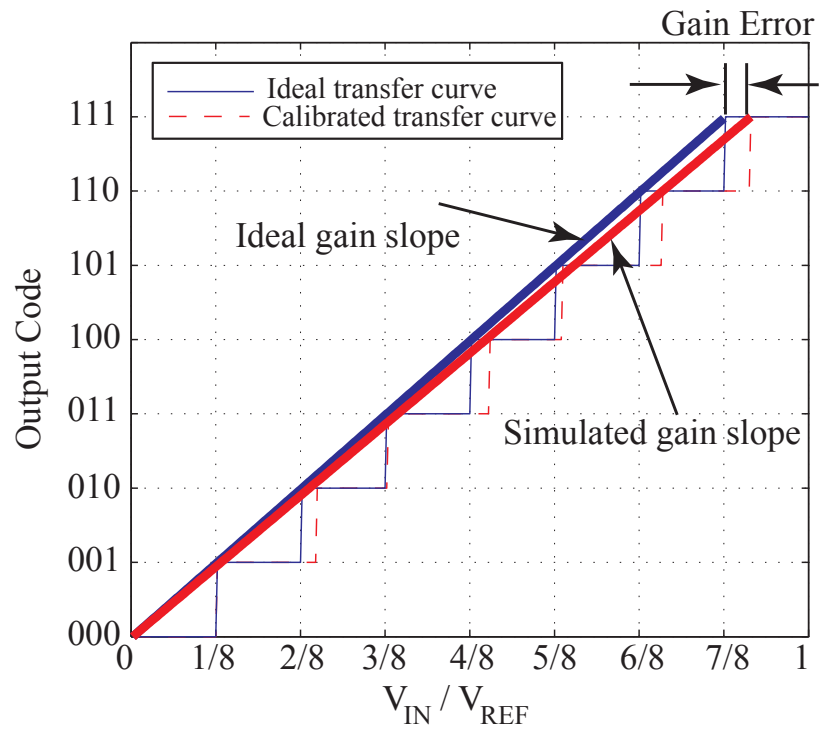


Figure 6.13 The gain error measurements. Gain slopes are obtained by connecting the first and the last transition points of the transfer curves.

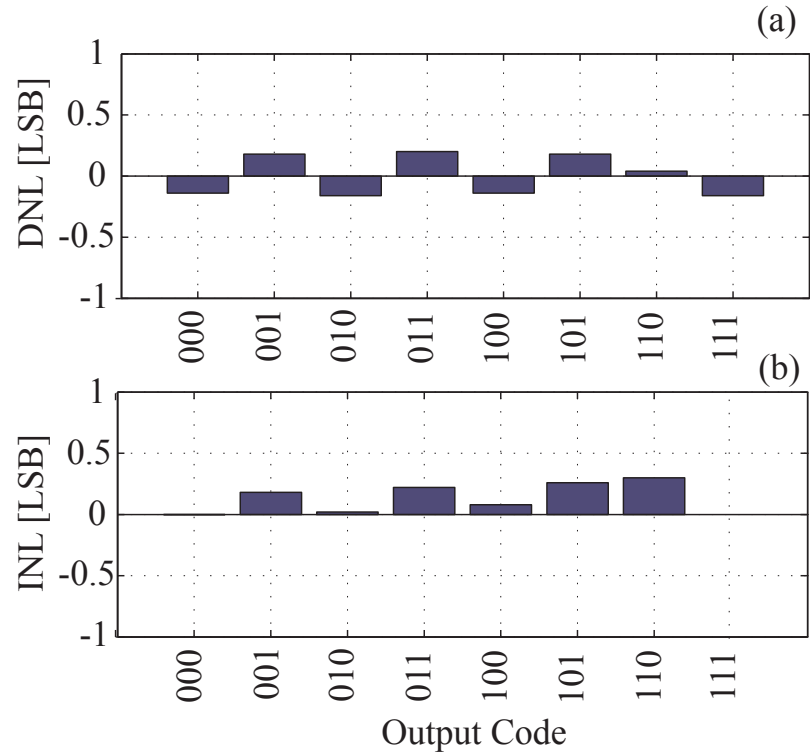


Figure 6.14 (a) DNL and (b) INL of the example of improved 3-bit ADC with compensation scheme.

6.2.2.2 Differential Nonlinearity

The DNL values of the improved 3-bit ADC with compensation scheme are estimated using the same method as presented in the last section. By using Eq. (6.1), the DNL of each output code from Figure 6.12 are illustrated in Figure 6.14 (a). In practice, the maximum and minimum values of DNL are mostly concerned whose absolute value DNL_{Max} are expected to be lower than 0.5 LSB. In the case, the maximum DNL is 0.18 LSB and the minimum DNL is -0.16 LSB. After 1000 Monte Carlo simulations, 65 % of the ADC netlists have their DNL_{Max} less than 0.5 LSB. A significant improvement in accuracy has been achieved, since this number for the uncompensated ADC was just 22.4 %.

6.2.2.3 Integral Nonlinearity

Based on the DNL measurements shown above, the INL of a digital code can be obtained by accumulating the previous DNL values, as given in Eq. (6.2). Its values have been illustrated in Figure 6.14 (b). Similarly to the DNL, the maximum and minimum INL values are normally given in the data sheet of a flash ADC. The maximum INL of this measurement is 0.26 LSB and the minimum INL is 0 LSB. Furthermore, 1000 Monte Carlo simulations have shown that 73 % of the ADCs have their maximum and minimum INL less than 0.5 LSB, compared with 46.5 % for the uncompensated case.

6.2.3 Noise and Distortion Evaluation

In Figure 6.15, the output code of one randomised ADC netlist is reconstructed and analysed as an example. Using the same experiment settings as the 3-bit ADC, the input signal is a full-scale sine wave at a frequency of 1.25 GHz. The clock signal of the ADC is 10 GHz that is 8 times higher than the signal. Therefore, for every cycle of the sine wave, 8 data points will be sampled. The data segment used for dynamic analysis contains 128 cycles that have 1024 data points. Three of the cycles are plotted in Figure 6.15 (a). After performed a 1024-point FFT analysis, the signal and distortions are illustrated in the single side frequency spectrum in Figure 6.15 (b). It can be observed that the DC signal power is -1.16 dB at 0 Hz. The input sine wave has a power of -7.11 dB at a frequency of 1.25 GHz. The power of the only harmonic distortions HD is -30.1 dB. Therefore, THD, obtained from the signal and the HD, is 22.97 dB. As there is only one HD, the SFDR is the same as THD. The SNQR can be obtained using $6.02 \times N + 1.76 = 19.82$ dB, which is equal to SNR in

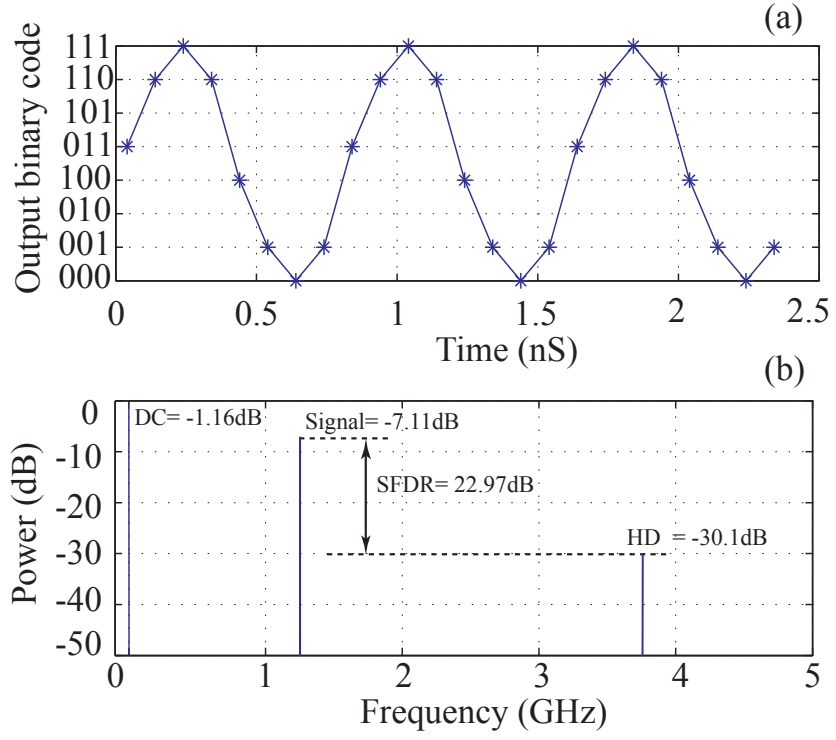


Figure 6.15 Output power spectrum of an example of the improved 3-bit flash ADC. (a) The reconstructed output signal. (b) The power spectrum of the signal in (a) analysed by FFT.

this simulation. Based on Eq. (6.3), the SINAD is equal to 18.01 dB, which is calculated using SNR and THD. At last, the Effective number of bits (ENOB) of this illustrated ADC is 2.72 bits. 1000 Monte Carlo simulations have been carried out for dynamic characteristics evaluation. As the most important parameter, the number of ENOB is higher than 2.5 bits is 79 %. This number was 46 % for the uncompensated ADC.

Three metrics were used to estimate the performance of the proposed flash ADC, including DNL, INL and ENOB. From the analysis, it could be observed that the requirement of $DNL_{max} < 0.5$ LSB is more difficult to meet because INL is more likely to be averaged out during the sum operation using Eq. (6.2). However, this does not necessarily mean that the set of $INL_{max} < 0.5$ LSB would be a subset of $DNL_{max} < 0.5$ LSB. The DNL was mainly used to estimate the monotonicity of a flash ADC. The INL was mainly used to determine the linearity and the yield of the ADC. Furthermore, the variability-introduced errors will manifest themselves as noise in frequency domain. The ENOB was used to reveal the magnitude of this impact. Although it could provide a straightforward interpretation of the impact of variability on the resolution, this parameter contains no information of the monotonicity and linearity.

6.3 Summary

The low-resolution flash ADC has become more and more attractive for high-speed low-power applications. The fabrication cost can be significantly reduced if the ADC block can be implemented on the same chip with the digital processor using a standard CMOS fabrication process. Small geometry UDSM devices can enable a high-speed design due to the reduced parasitic capacitance, but their extreme variability significantly reduces the accuracy of the data converter. Other common design constraints for UDSM devices, such as scaled supply voltage and the total power budget, will also degrade the design margin of an ADC block. Therefore, while high-speed is readily achievable with flash ADC design, it comes at the cost of a degrading other characteristics, such as resolution.

In the first section of this chapter, the previously proposed high-speed low-power comparator is used to design a 3-bit flash ADC using the 35 nm gate-length process. A complementary implementation is further developed in order to accomplish a rail-to-rail input range. By applying the histogram test method, the static characteristics, including the offset voltage, the gain error, the DNL and the INL, were calculated from 1000 Monte Carlo simulations of the ADC. However, only around 22.4 % and 46.5 of the netlists have met the requirements of DNL and INL, respectively. Furthermore, dynamic characteristics of the ADC were obtained via the FFT analysis. The frequency of signal and harmonic distortions are obtained in frequency domain. Important parameters, including SINAD, SNR, THD, SFDR and ENOB, are measured. Based on the statistical numbers of ENOB, only 46% of ADC can reach above 2.5 bits.

In the second section, an improved 3-bit flash ADC was proposed using the high-speed comparator with the compensation scheme. Full scale input range was achieved using the complementary P-type comparator with its compensation scheme. During the operation of the ADC, a 3 ns compensation phase was required to reduce the impact of the offset voltage before switch the ADC back to the operation phase. Static parameters and dynamic characteristics were evaluated using the same histogram test method and FFT method. After 1000 Monte Carlo simulations, 65 % and 73 % of the ADC netlists have met the requirements of DNL and INL. Over 79 % of ADC netlists have an ENOB higher than 2.5 bits. Therefore, a great performance improvement has been achieved for the compensated flash ADC over the uncompensated one.

Chapter 7 Conclusions and Future Work

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7.1 Thesis Summary

The industry has benefited from device scaling for over five decades. However, as the scaling of transistors approaches the atomistic level, significant device variability has become a major challenge for both circuit designers and manufacturers. Major sources of intrinsic parameter fluctuations that have been taken into account in this research include: RDD, LER and PGG. These unpredictable random sources lead to a significant electrical performance variation between nominally identical devices with the same biasing conditions. Furthermore, systematic process variations introduced when processing large wafers, can also degrade the circuit matching performance. Because systematic variations can be measured using on-wafer test structures, existing design techniques can be applied to reduce its impact. Analogue circuits are extremely vulnerable to intrinsic device variability when high precision operations are required. Differential pairs and current mirrors are intensively used as input stages and active loads in analogue circuits. Their matching performances directly determine the offset voltage of a circuit. At system level, the offset voltages from different blocks will eventually accumulate and degrade the yield of the fabrication and increase the cost of the product. Furthermore, the scaled supply voltage squeezes the allowable voltage swing. The number of transistors that can be stacked between two supply rails is decreased. Design solutions, such as the cascode topology, will become harder to apply.

The objectives of this thesis were: (a) to analytically evaluate the impact of device variability on analogue circuit design when process variation information is available; and (b) to develop new robust circuits at different design levels using UDSM devices with a low power supply voltage. The main achievements of this research are:

- A new short-channel mismatch model for the UDSM devices has been developed.
- The potential compensation principles at transistor level have been analytically investigated. Furthermore, applicable compensation circuits using 35 nm CMOS have been implemented.
- A high-speed latch-based comparator at low supply voltage has been investigated and implemented with a custom-designed compensation scheme for offset voltage reduction.
- A new high-speed analogue-to-digital converter (ADC) that is suitable for radio and communication application with the impact of device variability has been developed.

In Chapter 2, the major sources of variability were reviewed. These sources can all be tracked back to environmental and physical origins. The magnitude of different systematic variations can be measured using suitable embedded test structures. Using on measurement data, design solutions can easily be developed to eliminate predictable imperfections. However, this approach is not applicable for the case of random variations. Sources of intrinsic parameter fluctuations, including RDD, LER, OTF and PGG, have become dominant. Test structures for statistically measuring the random variations were reviewed. Existing mismatch models were introduced to establish a connection between the process variation and the electrical performance mismatch. The models are also useful for estimating the yield before committing a circuit to fabrication. Previously proposed design solutions for mismatch reduction were reviewed. Although they cannot be directly applied when UDSM devices are used, their principles provided a good starting point for the proposed design in the later chapters of this thesis.

Since the long-channel mismatch model is no longer adequate for evaluating the mismatch of short-channel devices, a new mismatch model that takes major short-channel effects into account is proposed in Chapter 3. These short-channel effects are velocity saturation and mobility degradation. The proposed model describes the device mismatch in both the triode regime and the saturation regime of a MOSFET's IV characteristic. It is noted that

the expressions in both regimes are unified when velocity saturation is taken into account. Furthermore, mobility degradation significantly contributes to the mismatch only when the perpendicular field is much higher than the lateral field. This occurs for this research when $V_{GS} - V_{DS} > 0.7$ V. All the mismatch model parameters are extracted using a new mathematical method. A comparison between the proposed mismatch model and the conventional long-channel mismatch model is given to demonstrate the accuracy improvements. At the end of Chapter 3, a case study is given to illustrate how to apply the proposed mismatch model in the context of real design practice; in this case a differential amplifier.

From the work of Chapter 3 we obtain knowledge of: (a) the origins of device statistical variability and (b) how to measure its magnitude in real design practice. The next question one would naturally ask is how to reduce the impact of device variability when UDSM devices are used during design phase? In Chapter 4, the basic concepts of using the four transistor terminals to overcome extreme device variability were reviewed. The analytical expressions of corresponding compensation voltages required at each terminal were given. Three compensation schemes were proposed and evaluated using statistical HSPICE simulations, including the body-biasing scheme, the drain compensation scheme and the source compensation scheme. For the body-biasing scheme, the principle is to use the body effect of the transistors to overcome the drain current mismatch. A drain compensation scheme is designed based on the fact that each transistor has a finite output resistance. If the drain voltages of the unbalanced transistor pairs can be adjusted accordingly, the drain current mismatch can then be eliminated. In the proposed drain compensation scheme, the modification of drain voltages is achieved by adjusting the load circuits. The source compensation scheme is the most efficient approach, as the voltages of all other terminals are measured using the source terminal as a reference point. Carefully adjusting the source voltages between two unbalanced transistors can compensate for drain current mismatch. The three compensation schemes achieved superior performances than would be obtained by simply increasing the transistor gate-length.

In Chapter 5, the scope of compensating for device variability is extended to the circuit level. Because UDSM devices are desired for use in high-speed applications, a novel comparator was proposed. It contained two current control transistors in the pre-amp stage to reduce the static power consumption. Because there are no more than three transistors stacked between two supply rails, it is suitable for low supply voltage applications. A regenerative stage was used to achieve a high comparison speed. Compared with the

existing high-speed comparator circuits in the literature, excellent performance was achieved compared to prior results obtained using similar simulation methods. Furthermore, it is noted that applying the compensation principles proposed in Chapter 4 can further reduce the offset voltage of this comparator. A custom designed compensation scheme was then developed. Using 2000 statistical simulations, the results confirmed that the offset voltage could be reduced to less than half of its original value.

Based on the proposed high-speed comparators in Chapter 5, a 3-bit 10 GSAMPLE/s flash ADC was built. Significant performance degradation was observed from the results of static and dynamic simulations. The flash ADC is then improved by adding compensation schemes to the high-speed comparators. After evaluating 1000 randomised ADC netlists, over 79% of the netlists had an ENOB higher than 2.5 bits. For circuit simulations where no compensation was deployed on 46 % of netlists had an ENOB of more than 2.5 bits. Only 22.4 % of netlists have their DNL_{Max} less than 0.5 LSB when no compensation was used. The number of netlists exhibiting $DNL_{\text{max}} < 0.5$ LSB was improved to 65 % after the compensation circuit is applied. These results have demonstrated that a high-speed ADC that works in the radio frequency range is possible and can be cheaply implemented with a standard UDSM CMOS process.

7.2 Future Work

There are a number of aspects of the research presented in this thesis that can be further extended and investigated. For the proposed short-channel mismatch model, a more sophisticated analytical model could be developed for multiple stage amplifiers and latch-based comparators. Based on the readily prepared process statistics, the total offset voltage accumulated from every transistor pairs of each stage could be quickly calculated. The yield estimation could be swiftly made without carrying out time-consuming Monte-Carlo simulations. This is especially valuable for large circuits, as the computational tasks will exponentially increase with the number of transistors. From a circuit design point of view, the precision of analogue filters and high-speed operational amplifiers will inevitably be reduced by the statistical device variability in the UDSM regime. New design and compensation solutions should be investigated with the constraint of scaled supply voltage. Furthermore, at system level, the flash ADC is only one of four popular architectures. Innovations could be obtained in developing robust pipeline, successive approximation and oversampling ADCs. A high-speed digital-to-analogue

converter (DAC) is also needed in a communication system to convert the processed data into high-speed analogue signals. DACs are also extremely vulnerable to extreme device variability. Investigations and research into the effect of extreme device variability on DACs should be carried out to enable the development of high-precision, high-speed and low-power circuits.

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Appendix A: How to calculate the signal-to-noise and distortion ratio (SINAD)

In this section, the mathematical relationship between SINAD, SNR, THD and ENOB are developed. These relationships are based on the tutorial of Walt Kester from the ANALOG DEVICES. These equations are based on the assumption that the input signal is a full-scale sine wave. The unit of SNR, THD and SINAD is dB. The expressions of SNR, THD and SINAD are given as:

$$SNR = 20 \times \log_{10} \left(\frac{S}{N} \right), \quad \text{Eq. A-1}$$

$$THD = 20 \times \log_{10} \left(\frac{S}{D} \right), \quad \text{Eq. A-2}$$

$$SINAD = 20 \times \log_{10} \left(\frac{S}{N + D} \right). \quad \text{Eq. A-3}$$

Therefore, the numerical ratio of $\frac{S}{N}$, $\frac{S}{D}$ and $\frac{S}{N+D}$ can be developed as:

$$\frac{N}{S} = 10^{-SNR/20}, \quad \text{Eq. A-4}$$

$$\frac{D}{S} = 10^{-THD/20}, \quad \text{Eq. A-5}$$

$$\frac{N + D}{S} = 10^{-SINAD/20}. \quad \text{Eq. A-6}$$

The root sum square of $\frac{N}{S}$ and $\frac{D}{S}$ equals to $\frac{N+D}{S}$, which is given as :

$$\frac{N + D}{S} = \left[\left(\frac{N}{S} \right)^2 + \left(\frac{D}{S} \right)^2 \right]^{\frac{1}{2}} = \left[(10^{-SNR/20})^2 + (10^{-THD/20})^2 \right]^{\frac{1}{2}} \quad \text{Eq. A-7}$$

$$= [10^{-SNR/10} + 10^{-THD/10}]^{\frac{1}{2}}$$

Therefore,

$$\frac{S}{N + D} = [10^{-SNR/10} + 10^{-THD/10}]^{-\frac{1}{2}} \quad \text{Eq. A-8}$$

and thus if SNR and THD are known,

$$SINAD = 20 \times \log_{10} \left(\frac{S}{N + D} \right) = -10 \times \log_{10} \left[10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}} \right]. \quad \text{Eq. A-9}$$

Similarly,

$$SNR = 20 \times \log_{10} \left(\frac{S}{N} \right) = -10 \times \log_{10} \left[10^{-\frac{SINAD}{10}} - 10^{-\frac{THD}{10}} \right] \quad \text{Eq. A-10}$$

and

$$THD = 20 \times \log_{10} \left(\frac{S}{D} \right) = -10 \times \log_{10} \left[10^{-\frac{SINAD}{10}} - 10^{-\frac{SNR}{10}} \right]. \quad \text{Eq. A-11}$$

Finally, the effective number of bits can be given as:

$$ENOB = \frac{SINAD - 1.76}{6.02}. \quad \text{Eq. A-12}$$