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University  
of Glasgow

School of Engineering  
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**Design and Implementation of Miniaturised  
Capsule for Autofluorescence Detection with Possible  
Application to the Bowel Disease**

Mohammed Abdul Wahab Al-Rawhani

Submitted in fulfilment of the requirements for the  
degree of Doctor of philosophy of the University of Glasgow

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# Abstract

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Early signs of intestinal cancer may be detected through variations in tissue autofluorescence (AF), however current endoscope-based AF systems are unable to inspect the small intestine. This thesis describes the design, fabrication, implantation, testing and packaging of a wireless pill capable of detecting the autofluorescence from cancerous cells, and able to reach parts of the gastrointestinal tract that are inaccessible to endoscopes. The pill exploits the fact that there is a significant difference in the intensity of autofluorescence emitted by normal and cancerous tissues when excited by a blue or ultra violet light source. The intensity differences are detected using very sensitive light detectors. The pill has been developed in two stages. The first stage starts with using an off-chip multi-pixel photon counter (MPPC) device as a light detector. In the second stage, the light detector is integrated into an application specific integrated circuit (ASIC). The pill comprises of an ASIC, optical filters, an information processing unit and a radio transmission unit, to transmit acquired data to an external base station. Two ASICs have been fabricated, the first stage of this work involved implementing an ASIC that contains two main blocks; the first block is capable of providing a variable DC voltage more than 72 V from a 3 V input to bias the MPPC device. The second main block is a front-end consisting of a high speed transimpedance amplifier (TIA) and voltage amplifiers to capture the very small current pulses produced by the MPPC. The second ASIC contains a high voltage charge pump up to (37.9 V) integrated with a single photon avalanche detector (SPAD). The charge pump is used to bias the SPAD above its breakdown voltage and therefore operate the device in Geiger mode. The SPAD was designed to operate in the visible region where its photon detection efficiency (PDE) peaks at 465 nm, which is near to human tissues autofluorescence peaking region ( $520\pm 10$  nm). The use of the ultra low light detector to detect the autofluorescence permits a lower excitation light intensity and therefore lower overall power consumption. The two ASICs were fabricated using a commercial triple-well high-voltage CMOS process. The complete device operates at 3V and draws an average of 7.1mA, enabling up to 23 hours of continuous operation from two 165mAh SR44 batteries.

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# List of Acronyms

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ADC	Analogue to Digital Convertor
AFI	Autofluorescence Imaging
AMS	Austriamicrosystems
APD	Avalanche Photodiode
ASIC	Application Specific Integrated Circuit
BSIM4	Berkeley Short-channel IGFET Model
CCD	Charge Couple Devices
CE	Capsule Endoscope
CS	Common Source amplifier
CMIM	Metal-insulator-Metal structure
CMOS	Complementary Metal-Oxide Semiconductor
CPLD	Complex Programmable Logic Device
DCR	Dark Count Rate
DRC	Design Rule Check
DNWELL	Deep N-type WELL
DPWELL	Deep P-type WELL
FLIM	Fluorescence lifetime imaging
FPGA	Field-Programmable Gate Array
FWHM	Full Width Half Maximum
GI	Gastrointestinal
H35	0.35 $\mu\text{m}$ High voltage process
HBT	Heterojunction Bipolar Transistors
HEMT	High Electron Mobility Transistor
kcps	kilo count per second
LED	Light Emitting Diode
OD	Optical Density
LVS	Layout Versus Schematic
MCU	Microcontroller unit
MOS	Metal–Oxide–Semiconductor
MPPC	Multi-Pixel Photon Counter
NMOS	N-type Metal–Oxide–Semiconductor
NMOSIT20	Isolated HV (20 V) Thin-oxide N-channel MOS

NMOS20HS	HV (20V) symmetrical Thick-oxide n-channel MOS
NWELL	N-type WELL
PCB	Printed Board Circuit
PDE	Photon Detection Efficiency
PDIFF	P-type Diffusion
PMOS	P-type Metal–Oxide–Semiconductor
PMT	Photomultiplier tubes
PQC	Passive Quenching Circuit
PWELL	P-type WELL
QE	Quantum Efficiency
RGC	Regulated Cascade
RPWELL	Shallow P-type WELL + Deep P-type WELL
SiPM	Silicon Photo Multiplier
SF	Source Follower amplifier
SOAC	Safe Operation Area Check
SoC	Systems on a Chip
SPAD	Single Photon Avalanche Photodiode
TIA	Transimpedance Amplifier

# List of Symbols

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$c$	Speed of light
$C_d$	SPAD's junction capacitance
$C_L$	Capacitive load
$C_s$	SPAD's parasitic capacitance
$E$	Energy
$f$	Charge pump clock frequency
$g_m$	Transconductance
$h$	Plank's constant
$I_D$	SPAD Current
$I_{out}$	Charge pump output current
$Q$	Quantum yield
$k_f$	Decay rate of the fluorescence emission
$k_i$	Decay rate of the non-radiative process
$k_x$	Decay rate of the intersystem crossing
$L$	Transistor gate length
$M$	mole/L
$R_{eq}$	Equivalent resistance
$R_d$	Diode resistance of the SPAD
$R_L$	Resistive load
$R_s$	Series resistance
$V_B$	SPAD breakdown voltage
$V_{Bias}$	SPAD reverse bias voltage
$V_{Breakdown}$	SPAD breakdown voltage
$V_{B-Sub}$	Bulk-P- substrate
$V_{BS}$	Bulk Source Voltage
$V_D$	Diode Voltage
$V_{DD}$	Supply Voltage
$V_{D-Sub}$	Drain-P- substrate
$V_{ex}$	Excess voltage
$V_{G-SB}$	Gate-Source, Gate-Bulk Voltage
$V_{out}$	Charge pump output voltage
$V_R$	Ripple Voltage

$V_{th}$	Transistor Threshold Voltage
$V_{\phi}$	Clock amplitude
$W$	Transistor gate width
$\tau$	Decay lifetime
$\lambda$	Photon's wavelength
$\phi$ & $\phi_b$	Non-overlapping Clocks

# Chapter 1 Introduction

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## 1.1 Motivation

The realization and implementation of non-invasive devices for biomedical applications has become increasingly viable due to the advantages of low cost, low power consumption, high reliability and potential for large scale integration of electronic components. The Capsule Endoscope (CE) is one such device that has seen a rapid progress in its development since the advent of the first CE in 2000. The development of CEs has dramatically changed the diagnosis and treatment method of many diseases that are found in the small intestine, such as obscure gastrointestinal bleeding, Crohn's disease, small bowel tumours and polyposis syndromes, amongst many others [1, 2]. The low-cost, and ease of use, coupled with increasing specificity, sensitivity and predictability, have enabled CE to become the gold standard for the diagnosis of most diseases of the small bowel [3, 4]. Another type of swallowable pill has been also developed to allow *in vivo* telemetric studies of the GI tract such as measurements of temperature, pH or pressure [5]. The Microelectronic System (MST) Group at the University of Glasgow has developed swallowable pills (55mm in length and 16mm in diameter) for measurements of pH levels in the GI tract [5].

Rapid advances and developments are also taking place to improve the conventional endoscopic instruments which are mainly used in the upper and the lower part of the gastrointestinal (GI) tract. The detection of cancerous tumours through autofluorescence is one such advance that has been adopted by conventional endoscopic instruments for the purpose of improving its sensitivity and predictability [6]. This method exploits the fact that the concentration of the indigenous fluorophores in living tissues varies depending on the health status of these tissues [7]. Cancerous tissues contain fewer of these fluorophores than those of the healthy ones. These fluorophores autofluorescence when excited by a blue light source. Depending on the concentration of these fluorophores, the intensity of

emitted autofluorescence varies, which can then be used to distinguish between healthy and non-healthy tissues [6, 8, 9].

Based on this fact, autofluorescence imaging (AFI) has been developed and incorporated into a conventional endoscopic instrument. This technique has the potential for distinguishing between cancerous and healthy tissue and is able to provide qualitative and quantitative diagnostic information for early signs of cancer more effectively, and with higher sensitivity, than that of white light imaging [6]. Olympus Corporation has employed this technique in one of their commercially available endoscopic systems [6]. However, this technique is still commercially confined to conventional endoscopic systems. The problem with these endoscopic systems is that they are limited to the upper and lower part of the GI tract. A part of the GI tract such as the small intestine is still inaccessible by these endoscopes. Thus, a diagnostic pill that has the AIF capability is required to cover the entire tract to exploit the potential of the AFI to its fullest. In this research, our effort is focused on investigating an effective way of migrating the basic principle of AIF and thereafter implementing it into a swallowable miniaturized capsule that can be used to detect cancer in the small intestine.

## **1.2 Aims and objectives**

The aims of this work are:

To design, fabricate and characterise a swallowable endoscopic capsule (pill) for detecting cancer in the GI tract by measuring changes in the autofluorescence emissions of the GI tissue.

The main objectives of this work are:

- To design, fabricate and characterise a miniaturized prototype for an autofluorescence radiometric system in a pill format smaller than 50 mm in length and 16 mm in diameter.
- To design, fabricate and characterise a pill that is capable of producing illumination in the band between 400nm - 500nm and to detect autofluorescence emission at wavelength 500nm - 700 nm.

- The detector to have high photon detection efficiency (PDE) of more than 20 % in the region above 510 nm (the most widely used detectors for autofluorescence are PMTs which have photon detection efficiency in the range of ~ 20%) [10, 11].
- The pill should be capable of exciting and detecting the weak autofluorescence from the human tissue (i.e the autofluorescence Quantum yield (Q) of a healthy human tissue is 0.00038).
- The pill should be able to transmit wirelessly the acquired data to an external work station within a 1 meter radius
- The pill should be able to operate using two SR44 (1.55 V, 165 mAh) watch batteries and operate for more than 9 hours; time typically required to traverse the human intestine.

### **1.3 Thesis outline**

The rest of this thesis is organised as follow. **Chapter 2** reviews the tissue fluorescence phenomenon and its characteristics including intensity, lifetime and its excitation and emission spectra. The behaviour of fluorescent substances is also presented which leads to a deep understanding on how the autofluorescence phenomenon is efficiently exploited in many applications. This chapter focuses on explaining how the indigenous fluorescent substances of living organisms is exploited to evaluate the health status of these organisms. This is followed by an overview of the essential components of the basic instrument that is used to measure fluorescence lifetime and intensity from fluorescent substances. Understanding the operating principle of this instrument will establish the main aim of this work which is to miniaturise this instrument into a swallowable capsule form that can take fluorescence measurements from within the human body's small intestine.

**Chapter 3** reviews design considerations for some existing diagnostic pills. The components and design parameters for a pill that is capable of detecting cancer in the small intestine are reviewed and accordingly a design proposal for the pill is presented. A key component of this pill is an ultra sensitive light detector. Based on a comparison of existing sensitive light detectors that are capable of detecting autofluorescence emission, the MPPC device was chosen to be incorporated into the pill. In order to operate the MPPC, an ASIC block diagram is proposed. This ASIC contains a high voltage charge pump that can generate more than 72 V and a TIA that is capable of capturing the 10 MHz pulses generated by the MPPC. A literature review of the two main blocks of the ASIC is

presented as an introduction to the design and implantation of the ASIC which is discussed in chapter 4 and chapter 5.

**Chapter 4** considers the design and fabrication of the very high voltage charge pump that can generate a variable high voltage greater than 72 V and to deliver a current greater than 70  $\mu\text{A}$  which is required to operate the MPPC device. The design aspects of the charge pump which consists of 5 cells are discussed and presented in a way that justifies the design topology and the components that are used in the design. With the proposed topology of charge pump it will be seen that the charge pump has achieved high efficiency. It will be also seen that the charge pump was designed to be controlled by a single input clock which permits the generated voltage to be varied. The charge pump is characterised and its operation is evaluated and presented in a detailed manner. Its ability to deliver the required voltage and current to the MPPC is verified by directly biasing the MPPC to the output of the charge pump.

**Chapter 5** discusses the steps of designing and implementing the front-end that can work in conjunction with the MPPC device that has a very large capacitance of 37 pF. The front-end consists of a transimpedance amplifier (TIA) and a post-amplifier stage. The design of the TIA is based on a regulated cascode input stage (RGC). It will be seen that the proposed design helps to ease the relationship between the large input capacitance and the achieved bandwidth and input impedance. The front-end is laid out and fabricated in the same chip with the charge pump designed in chapter 4. The front-end is then tested and evaluated when working with the MPPC.

**Chapter 6** begins with a feasibility study into integrating a SPAD with a charge pump into a single chip by testing a SPAD that was fabricated by The University of Oxford and a component of the charge pump that was discussed in chapter 4. The designs of the two devices are integrated and fabricated into a single chip. Electrical and optical evaluation measurements of the SPAD, the charge pump and the two blocks are presented. This is followed by biological measurements that are conducted using a lamb's small intestines. The measurement verified the operation principal of the system and showed that the fabricated ASIC has met the design expectations. All the implemented components that were designed to be incorporated in to the capsules were fitted into a 16mm (diameter) x 45mm (length) glass capsule to demonstrate the size viability. However, due to the manual nature of the final assembly, the relatively small capacitor

(0402 packaging) and the wire bonds to the ASIC, the final capsule in its final form could not be tested.

**Chapter 7** concludes the works from the previous chapters. Potential future work is also discussed.

# Chapter 2    Background: Cancer detection through fluorescence

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## **2.1 Introduction**

This chapter goes on to introduce the fluorescence phenomenon and its characteristics such as its intensity, lifetime and its excitation and emission spectra. This introduction leads to a better understanding of the behaviour of fluorescence substances and therefore, understanding how they are exploited in an efficient way in many applications. This is followed by introducing some of the indigenous fluorescence substances in living organisms, which later will be referred as autofluorescence and how they are exploited to evaluate the health status of some organisms. Later on, it will be explained how the autofluorescence in the small bowel is being used to detect early signs of cancer, by means of detecting the intensity, or the lifetime of its indigenous fluorescence substances. This will be followed by a section which will have an overview of the essential components of the basic instrument which is used to measure the fluorescence lifetime and its intensity. This section will establish the main aim of this work, which is, to miniaturise this instrument into a swallowable capsule form that can take fluorescence measurements from within the small intestine in the body.

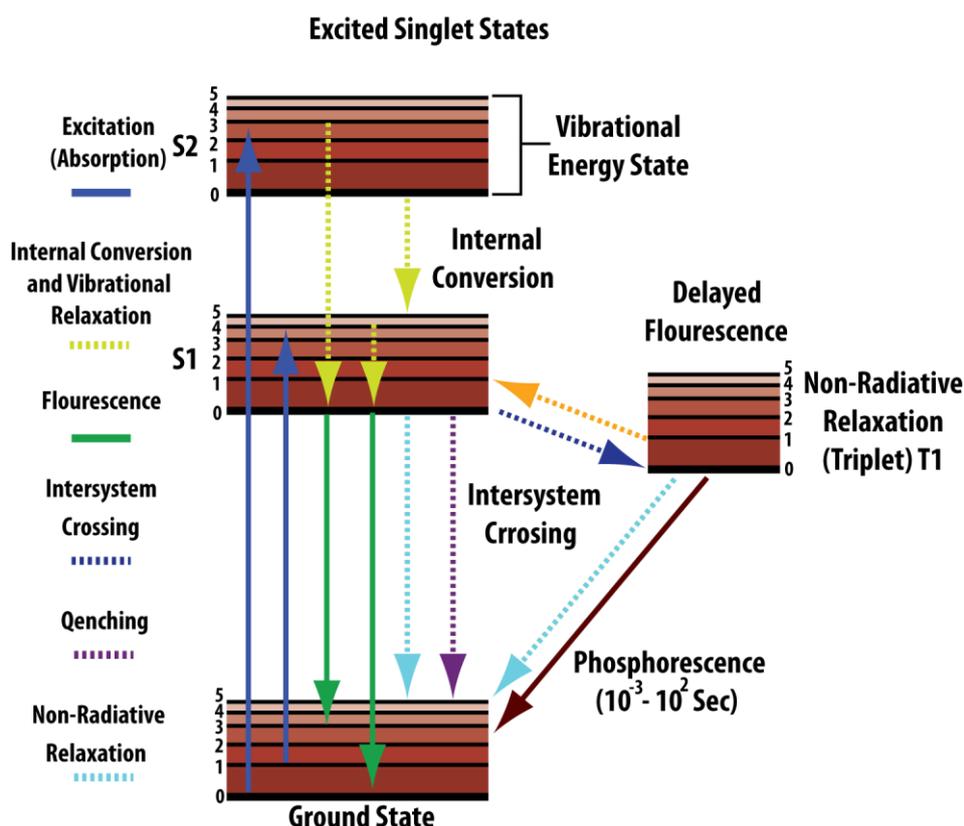
## 2.2 *What is fluorescence?*

Fluorescence is a natural phenomenon exhibited by certain group of molecules. These molecules, sometimes referred to as fluorophores, absorb light at one wavelength and emit light back at another, typically longer, wavelength [12]. In general, the phenomenon where luminescence is generated through the excitation of a molecule by ultraviolet or visible light photons, is known as photoluminescence. This is divided into two categories, fluorescence and phosphorescence, depending upon the electronic configuration of the excited substance and the emission pathway. Mostly, it can be said that the process of fluorescence and phosphorescence occurs in a similar manner, but with a much longer excited state lifetime in the case of the latter [13].

The phenomenon of fluorescence was first observed by Sir Frederick William Herschel in 1845. Sir Frederick reported that quinine solution emitted fluorescence when exposed to sunlight [14]. His experiment can be repeated easily by exposing a glass of tonic water, which contains quinine, to sunlight, or to any blue light source, and observing the emitted light, at the right angle which is relative to the source light direction. Fluorescence is typically produced from substances that have aromatic molecules. Quinine, Rhodamine B and POPOS, are examples of typical fluorescence aromatic molecules, that can be encountered in our every day life. For example, trace quantities of Rhodamine can be found in antifreeze, which glows green-orange or Red when excited [14].

The process which describes how the molecules in fluorescent substances absorb and emit fluorescence, was first described by Professor Alexander Jabłoński in 1935. The molecular energy state diagram, often referred to as a Jabłoński Diagram, is shown in **Figure 2.1** and illustrates this process in detail. The diagram shows how electrons in fluorophores are excited from the ground state, into higher electronic energy states, and the events that occur as these excited molecules emit photons and fall back into lower energy states.

**Figure title: Jablonski Diagram.**



**Figure 2.1 Jablonski Diagram: illustrates the luminescence process.**

The sequence of events that occurs during the illumination process, can be explained as follows: Prior to excitation, the electronic configuration of the molecule is described as being in the ground state (S0). When a molecule is excited with radiation which has a wavelength ranging from the ultraviolet to the visible ranges (250 nm to 700 nm), as presented in **Figure 2.1** (left-hand blue arrow), the molecule absorbs the excitation photon, an energetically excited state is formed, and then the electrons may be raised to a higher energy, and vibration levels of the (S1) or second level (S2) energy state. Immediately following this step, several processes will take place with varying probabilities, depending upon the exact nature of the fluorophore and its surroundings, the most likely will be relaxation to the lowest vibrational energy level, the first excited level (S1). This process is known as internal conversion or vibrational relaxation, (loss of energy in the absence of light emission) and generally occurs in picoseconds or less. If the excited molecule stays in the first level for long time (a period in time-scale of nano-seconds) before relaxing to the ground state, it will be accompanied by the emission of a photon, the process is formally labeled as fluorescence.

**Table 2.1 Timescale Range for Luminescence Processes [15].**

Transition	Process	Timescale (Seconds)
S0 → S1 or S2	Absorption (Excitation)	$10^{-15}$
S2 → S1	Internal Conversion	$10^{-14}$ to $10^{-10}$
S1 → S1	Vibrational Relaxation	$10^{-12}$ to $10^{-10}$
S1 → S0	Fluorescence	$10^{-9}$ to $10^{-7}$
S1 → T1	Intersystem Crossing	$10^{-10}$ to $10^{-8}$
S1 → S0	Non-Radiative Relaxation Quenching	$10^{-7}$ to $10^{-5}$
T1 → S0	Phosphorescence	$10^{-3}$ to 100
T1 → S0	Non-Radiative Relaxation Quenching	$10^{-3}$ to 100

Excited fluorophores in high energy levels can take several other relaxation pathways that compete with the fluorescence emission process. The energy state can be dissipated non-radiatively as heat to its surroundings (depicted by the cyan dashed arrow in **Figure 2.1**). It can also be also dissipated as non-radiative heat in a collision between the excited molecule and another molecule (as illustrated by the purple dashed arrow). This phenomenon is exploited in what is known as quenching technique, which is used to suppress any unwanted fluorescence in some biological experiments. This is achieved by adding some other molecules, this forces the unwanted fluorophores to dissipate their excited energy state into the non-radiative process rather than the fluorescence process which emits photons. Another event that can take place, although rarely occurs, is known as intersystem crossing to the lowest excited triplet state (depicted in blue dashed arrow). This event can result either in the emission of a photon through phosphorescence, or a transition back to the excited singlet state which yields delayed fluorescence. In **Table 2.1**, all the possible process that can take place during luminescence have been listed, along with typical timescales [15].

## 2.3 Characteristics of fluorescence

The unique characteristics of fluorescent substances have been exploited in a wide range of applications, varying from environmental, to biological and biomedical applications. This section will highlight the most important characteristics of fluorescence molecules, this will build a bigger picture of the behaviour and the properties of fluorescence emission. Mainly, there are three basic fluorescence observables, than can characterise the fluorescence emission of a certain fluorophore [16].

### 2.3.1 Quantum yield and fluorescence intensity

The emission intensity of a fluorophore is perhaps the most important property which characterises a certain fluorophore. In this work, as we will discuss in the next chapter, we have adopted the intensity of the fluorescence, as a way in which we can distinguish between cancerous tissues and healthy ones. For fluorophore solutions, the fluorescence intensity can be accurately represented by the efficiency, which is known as quantum yield ( $Q$ ). The quantum yield is the mean ratio of the number of emitted photons, to the number absorbed, averaged over the entire fluorescence spectrum range [17]. Based on our discussion in the previous section, it has also become clear that not all excited molecules will relax to the ground state by fluorescence emission; alongside the fluorescence emission of photons there are two other process that can take place, non-radiative process energy loss and intersystem crossing through the triplet state, therefore the quantum yield is a function of the competing decay rates of these three process, this can be given by [17]

$$Q = \frac{k_f}{k_f + k_i + k_x} \quad 2.1$$

Where  $Q$  is the quantum yield,  $k_f$  is the decay rate of the fluorescence emission,  $k_i$  decay rate of the non-radiative process and  $k_x$  is the decay rate of the intersystem crossing. The quantum yield of a fluorophore can be close to unity if  $k_i + k_x \ll k_f$ . The closer the quantum yield to unity the brighter the fluorescence emission produced by the fluorophore [14].

The quantum yield can be accurately determined in a controlled environment, where all photons in the excitation source are directed towards the fluorophore solution sample. Generally, in the case of fluorophore solutions where the quantum yield is high ( 0.05 to 1) [18], researchers resort to using a comparative method to measure the fluorescence

emission. In this method, the targeted solution is compared to other solutions of a well-known concentration, such as the quinine salt, and accordingly the quantum yield is determined. However, when dealing with biological samples, such as human tissue, accurately determining  $Q$  becomes impractical, due to the scattering problem, and due to the difficulty of estimating the concentration of the fluorophores and their surroundings [14]. The existence of many fluorophores in one sample at the same time also acts as a major obstacle. For example measurements of quantum yield ( $Q$ ) obtained in vivo from a normal human cervix can vary greatly in the range between  $6.1^{-5}$  to 0.0038 [19]. Therefore, instead of using the quantum yield, as in the case of fluorophore solutions, the term intensity becomes the parameter of choice in biological or medical applications. In this work, the main goal is to measure the autofluorescence intensity from living tissues. Counting how many photons are emitted over a certain period of time is sufficient to provide an indicator of the intensity level of the autofluorescence emission from these tissues. This intensity is propositional to the spatial concentration and the quantum yield of each fluorophore which exists in the human tissue and therefore provides an indicator of whether the targeted tissue is a normal or a diseased tissue, as will be explained in more details in **section 2.5** [6, 14].

### 2.3.2 Fluorescence lifetime

The lifetime of fluorescence is defined by the average time in which the molecule remains excited prior to returning to the ground state, which typically ranges from  $10^{-9}$  to  $10^{-7}$  seconds. The fact that different molecules have different lifetimes is employed to distinguish between different fluorophores, and can offer an alternative method of characterisation to that of measuring the quantum yield. However, the ultra short time that the molecule spends in the excitation state, requires more complicated instruments than that used to measure the intensity [20].

The standard way of measuring the fluorescence lifetime is by exciting a fluorophore solution with an ultra short laser pulse and then measuring exponential decay lifetime which can be given by [17]

$$\tau = \frac{1}{k_f + k_i + k_x}$$

2.2

Where,  $\tau$  is the decay lifetime of the fluorophore. Due to the random nature of the fluorescence emission, few molecules will emit their photons at exactly time =  $\tau$ . Therefore,  $\tau$  is measured several times, and the average of these measurements represents the lifetime of that specific fluorophore.

### 2.3.3 Fluorescence excitation and emission spectra

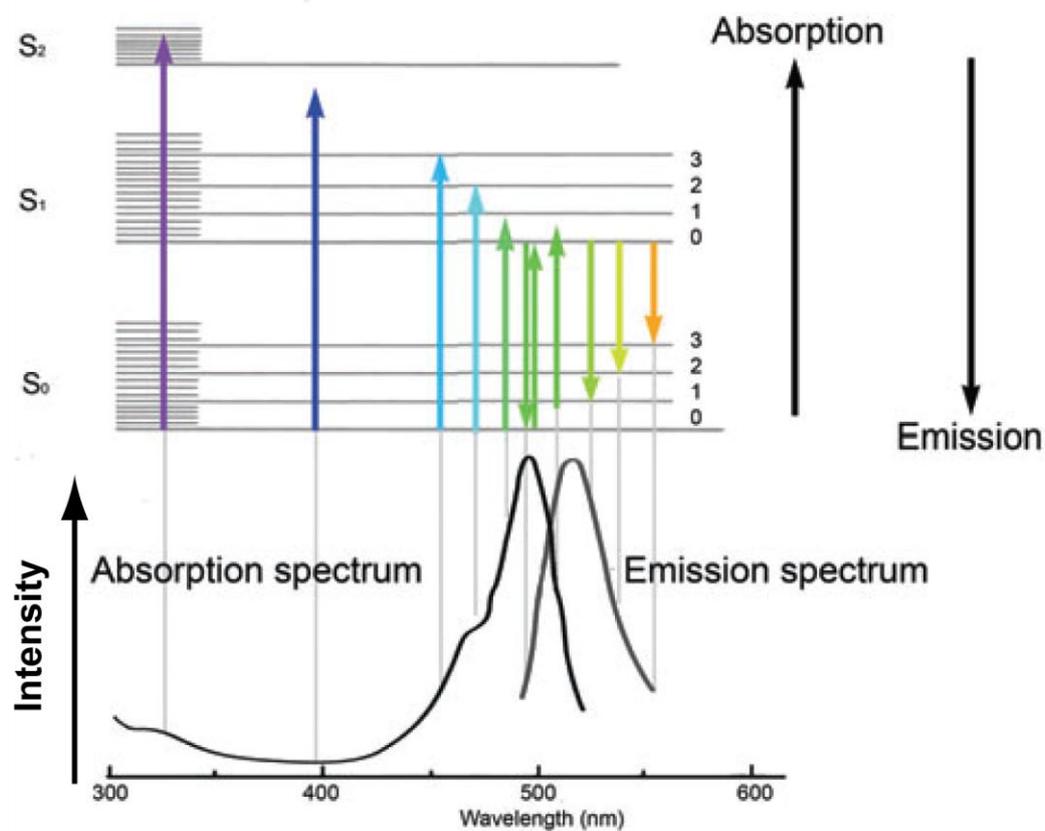
The aspect of fluorescence that makes it useful in many applications is the difference between the exciting and the emitting wavelengths. This phenomenon is known as Stokes' shift. This shift occurs as a result of the loss of vibrational energy when molecules go from an excited vibrational state to the ground state. The absorption and emission spectra are usually symmetrical curves, as shown in **Figure 2.2**. The spectral characteristics of these curves are related to the size of the energy steps of the transitions from one level to another. When a photon is absorbed by a molecule in a fluorophore, all the energy possessed by that photon will be transferred to the molecule. This energy is inversely related to the photon's wavelength and is given by [17]

$$E = \frac{hc}{\lambda} \quad 2.3$$

Where  $h$  is Planck's constant,  $c$  is the speed of light and  $\lambda$  is the wavelength of the photon in a vacuum. If the photon's energy absorbed by the molecule is greater than energy needed to exactly move it from the ground state to the lowest energy level of S1, the molecule will move to a higher state S2. This indicates that the molecule can be excited and moved between energy levels by changing the energy of the incident photons, this can be achieved easily by changing the photon's wavelength. In **Figure 2.2**, the absorption and emission spectra of a common fluorophore known as (FITC), is sketched below the Jabłoński diagram to illustrate how the spectra is formed. Each vertical gray line aligns the spectra with the energy of the absorbed photons (arrows pointing up) or the energy of the emitted photons (arrows pointing down). The colours of the arrows represent the wavelengths. For example the purple arrow to the left, represents the energy of an ultra violet photon that caused a molecule to transition from the ground state to the second excited state. On the other side of the spectra, an orange arrow represents the lowest energy photon that can be emitted by this molecule, as it drops back from the lowest energy state of S1, to the highest

vibrational state of  $S_0$ . The symmetry between the absorption and emission curves is attributed to the similarity of transitions to vibrational states in  $S_0$  and  $S_1$ .

**Figure title: Absorption and emission spectra.**



**Figure 2.2 Absorption and emission spectra of the common fluorophore FITC [17].**

Maximum fluorescence intensity can be achieved when the fluorophore is excited at or near the peak of the excitation curve. The wavelength of both the absorption peak and the emission peak differs between one fluorophore and another [21].

## **2.4 Autofluorescence in living organisms**

Fluorescence is widely used in biological and medical research to characterise and study cells and organisms. Most of this research focuses on the use of exogenous fluorescent molecular fluorophores (also referred to as ‘labels’ or ‘probes’). Introducing these probes into cells or tissues can give us information regarding spatial localization. This can be also be used to provide us with some information about different pH concentrations [22, 23].

The use of such molecular probes in biological and medical fields has led to significant advances in our understanding of the molecular biology of the cell. However, introducing these probes to a biological system can be toxic, or it can add a negative or unwanted effect to the biological system under investigation, and as a result, cellular viability and biological integrity can not be relied upon [24]. For these reasons, endogenous fluorescent molecular fluorophores, or commonly known as autofluorescence which exists in biological systems have become of interest, since it can provide some information about the biological system without the need of adding any external influence. However, in fluorescence microscopy, cellular autofluorescence can also become a problem and cause an interference with other fluorescents of interest [25]. For this reason the quenching technique mentioned in **section 2.2** is used to eliminate this interference by autofluorescence by using a wide variety of small molecules or ions that act as quenchers for unwanted autofluorescence [26].

Some examples of the endogenous fluorophores that can be found in human tissues of the GI tract are summarized in **Table 2.2**, with their optimal excitation wavelength and the peak autofluorescence emission. The main contributors of the autofluorescence emission spectra of the GI tract are mainly the endogenous intercellular small molecules such as flavins and vitamins, and extracellular matrices, such as collagen or elastin.

Autofluorescence can be also found in plant tissues. As with human tissues, plants tissues have endogenous molecules that absorb light in many regions of the near-ultraviolet and visible light spectrum. One of the main contributors to autofluorescence emitted by plants is chlorophyll, other fluorophores such as lignins, carotenes, and xanthophylls also produce a significant level of fluorescence emission when excited with the proper wavelength. The autofluorescence intensities or its lifetime are used to identify plants and to characterize their state of health [27, 28].

**Table 2.2 Example of endogenous fluorophores in human tissues of the GI tract. [8, 29].**

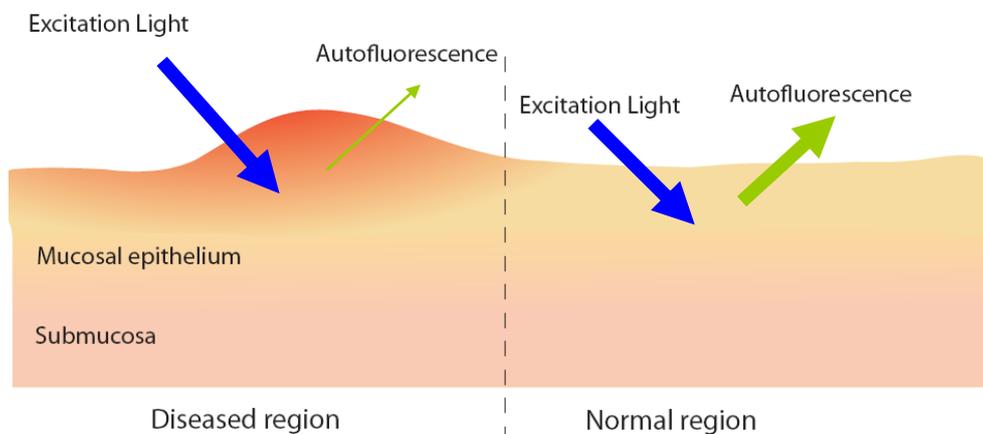
<b>Endogenous Fluorophore</b>	<b>Optimal Excitation Wavelength (nm)</b>	<b>Peak Autofluorescence Emission (nm)</b>
<b><u>Amino acids</u></b>		
Tryptophan	280	350
Tyrosine	275	300
Phenylalanine	260	280
<b>Structural proteins</b>		
Collagen	330	390
Elastin	360	410
<b><u>Enzymes and coenzymes</u></b>		
NADH	340	450
Flavins	450	520
NADPH	336	464
<b><i>Vitamins</i></b>		
Vitamin A	327	510
Vitamin K	335	480
Vitamin D	390	480
<b><u>Vitamin B6 compounds</u></b>		
Pyridoxine	332,340	400
Pyridoxamine	335	400
Pyridoxal	330	385
Pyridoxic acid	315	425
Pyridoxal 5-phosphotae	315	425
Vitamin B12	275	305
<b><u>Lipids</u></b>		
Phospholipids	436	540
Lipofuscin	340-395	540,430-460
Porphyrins	400-450	635, 690

## 2.5 Gastrointestinal cancer detection through autofluorescence

The Gastrointestinal (GI) tract, including the oesophagus, stomach, small intestine, large intestine, and colon, is somewhere many types of cancers can occur. Most cancers start when abnormal cells grow out of control and form a tumour. The tumour can continue to grow such that cancer begins to spread to other parts of the body. The longer the tumour goes unnoticed, the greater the chance that the cancer has spread and become a life-threatening disease. However, cancers are easier to be treated and cured if they are detected in early stages [30].

In the upper and lower part of the GI tract, autofluorescence visual endoscopy has been proven to be a highly effective approach, for detecting precancerous and early cancerous tissues when compared to the standard white-light endoscopy [3-8]. In this type of endoscopy, highly specific filters, sensor arrays and light sources are incorporated into the scanning probe of the device. The probe is capable of streaming video that show the distribution of the tiny amounts of autofluorescence light.

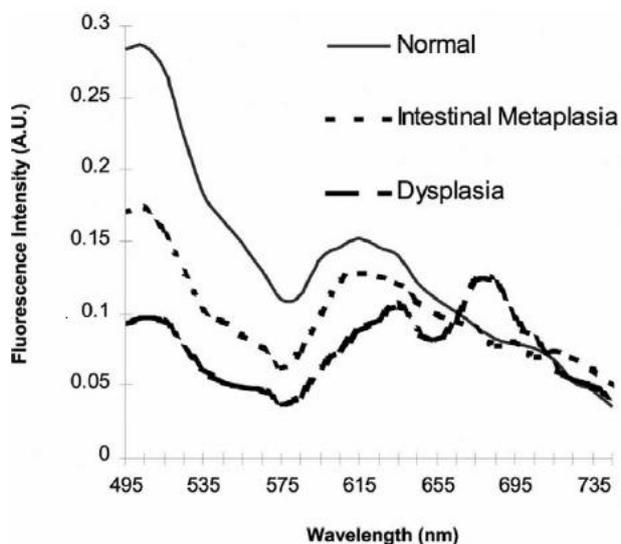
**Figure title: Cancer detection concept.**



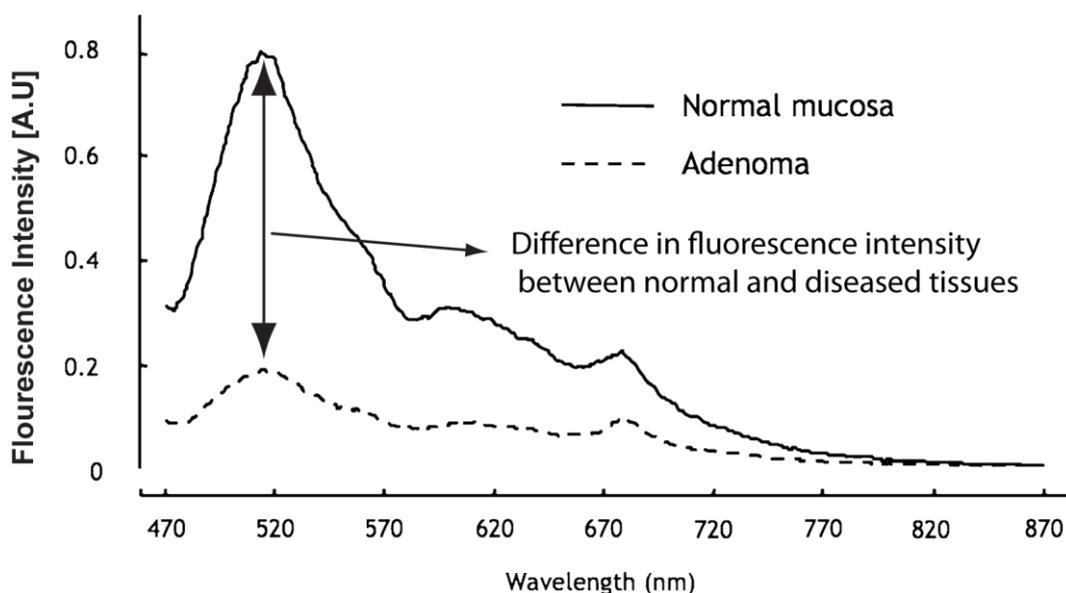
**Figure 2.3 Autofluorescence intensity varies between diseased regions and normal regions.**

**Figure title: Autofluorescence emission spectra**

a)



b)



**Figure 2.4 Spectroscopic patterns of normal and diseased regions: a) patterns of normal and dysplastic oesophagus [8] . b) Patterns of normal mucosa and adenoma [6].**

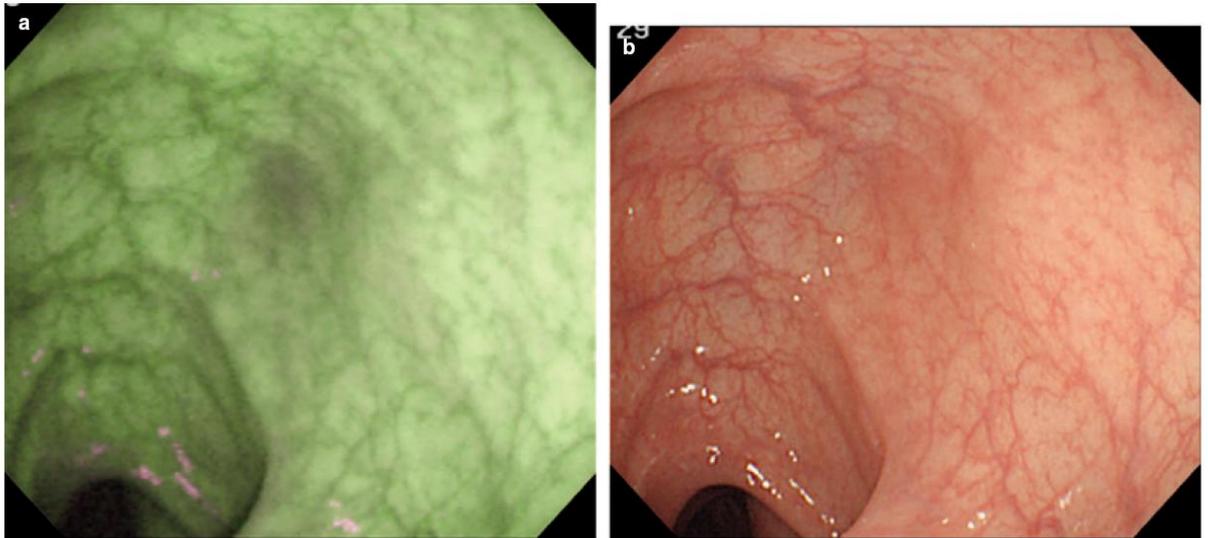
Autofluorescence endoscopy exploits the natural autofluorescence phenomenon, where human living tissues emit green light (520 nm) when excited with a shorter wavelength blue light (380-500 nm). The amount of the emitted green light depends on the amount of endogenous fluorophores and this varies according to the health of the tissue.

**Figure 2.3** illustrates the basic mechanism for detecting cancer through autofluorescence; when tissues are excited with same amount of blue light, diseased regions can give up to three times lower autofluorescence intensities than normal ones. This decrease in autofluorescence is due to the absorption and scattering of light, in the epithelium of mucosal membranes in cancerous tissue. This reduction can be mainly attributed to the lower concentration of endogenous fluorophores. The increased number of blood vessels that are usually developed in cancerous regions, reduce the spatial concentration of endogenous fluorophores, such as flavins, collagen and elastin [7].

The intensity variation between the cancerous and healthy tissues has been widely investigated by several studies *in-vivo* and *in-vitro* [6, 8, 9, 31-35]. All the reported studies have concluded that there is a significant difference between the intensity of autofluorescence emitted by normal and cancerous tissues, over a wide range of excitation and emission wavelengths.

Some of these studies have reported autofluorescence intensity measurements that were conducted on different parts of the GI tract, on cancerous and normal regions, and over different spectra ranges. Shown in **Figure 2.4**, some reported results from [6, 8, 9] clearly show that the autofluorescence intensity of normal tissues are much higher than that of cancerous tissues, over the range (470-700nm). In [8] the measurements were conducted *in-vivo* on; normal squamous oesophagus; Barrett's metaplasia; and Barrett high-grade dysplasia. **Figure 2.4.a**, shows a spectral decay, especially around 580 nm, this decay is attributed mainly to haemoglobin absorption which is heavily present in the high-grade dysplasia than on other samples. Another *in-vivo* pilot study [6] has examined autofluorescence using the autofluorescence imaging system (AFI) from Olympus Medical Systems. In this study, spectroscopic patterns of normal colon mucosa and adenomatic mucosa, shown in **Figure 2.4.b**, confirm the same concept that other studies have concluded. The overall intensity at the tumour, was almost three times lower than that of the normal mucosa, especially around 520 nm. This reduction in emission from endogenous tissue fluorophores, can be attributed to the changes in the concentration, or depth distribution, of these fluorophores [6].

**Figure title: Autofluorescence imaging and white light imaging.**

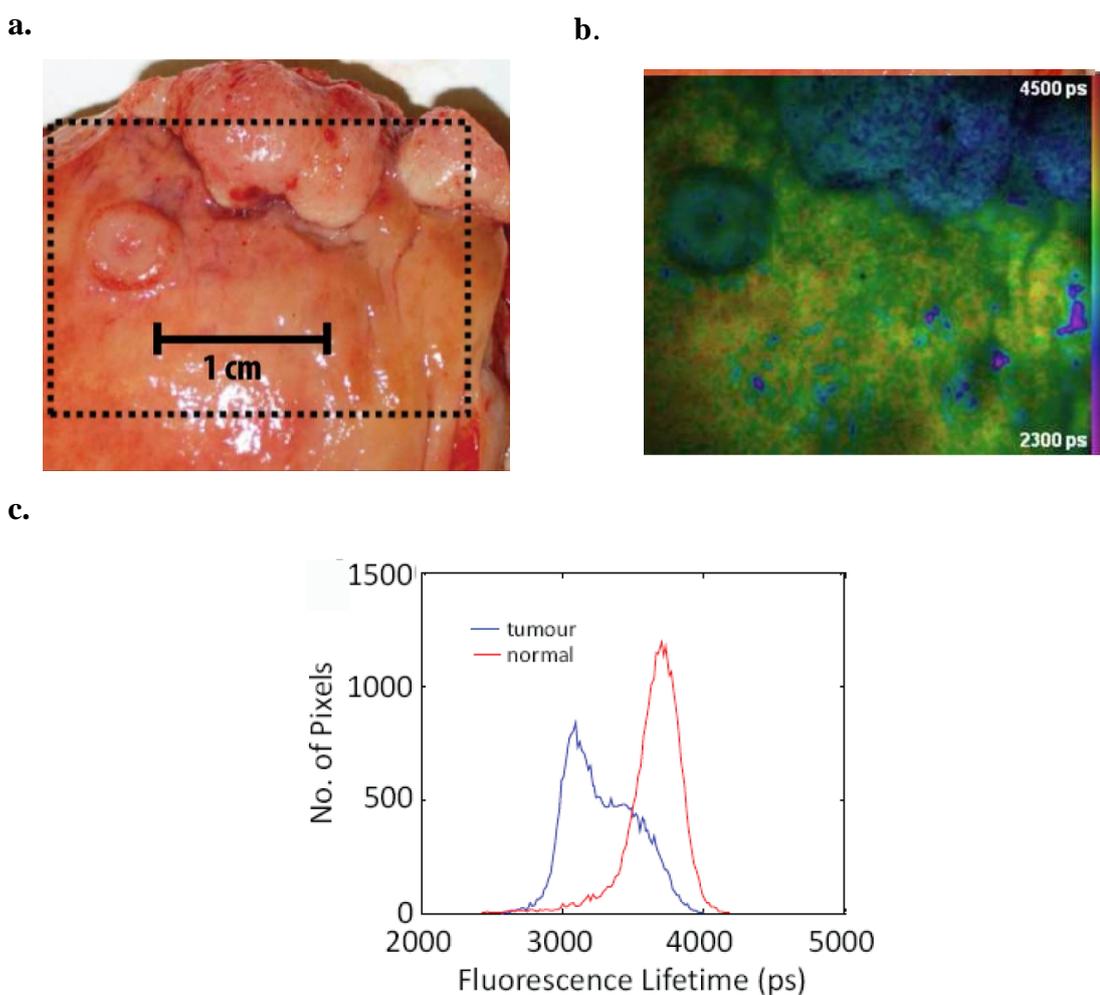


**Figure 2.5 Endoscopic images of a small flat adenoma: (a) the lesion was detected by autofluorescence imaging as a purple area in green background. (b) On white light observation it was hard to see [6].**

The autofluorescence emitted by human tissues can be seen in the images reported by [6]. The reported images, shown in **Figure 2.5** are for a section of the upper part of the GI tract that has flat lesions. When observing this region with white light, it was hard to notice any abnormality. However, the lesions were distinctively obvious from the surrounding regions when it was observed by AFI.

Cancerous and healthy tissues can be also distinguished by lifetime measurement. The intensity difference can be obtained by a life time measurement of the emitted autofluorescence as we will see in next chapter. Work conducted in [36], has reported both visual results and data collected from measurements. **Figure 2.6.a** shows a white light image of a freshly resected bladder, containing a moderately differentiated squamous cell carcinoma in the left side. The other image (**Figure 2.6.b**) is of the same tissue, but with fluorescence lifetime imaging (FLIM). A histogram of a lifetime distribution is shown in part c. The intensity for the lifetime period of the autofluorescence at the normal part of the bladder is higher than that of the cancerous part of the bladder. This is also true for the absolute autofluorescence lifetime of the normal part, which is higher than that of the cancerous part [36].

**Figure title: White light imaging and autofluorescence lifetime imaging.**



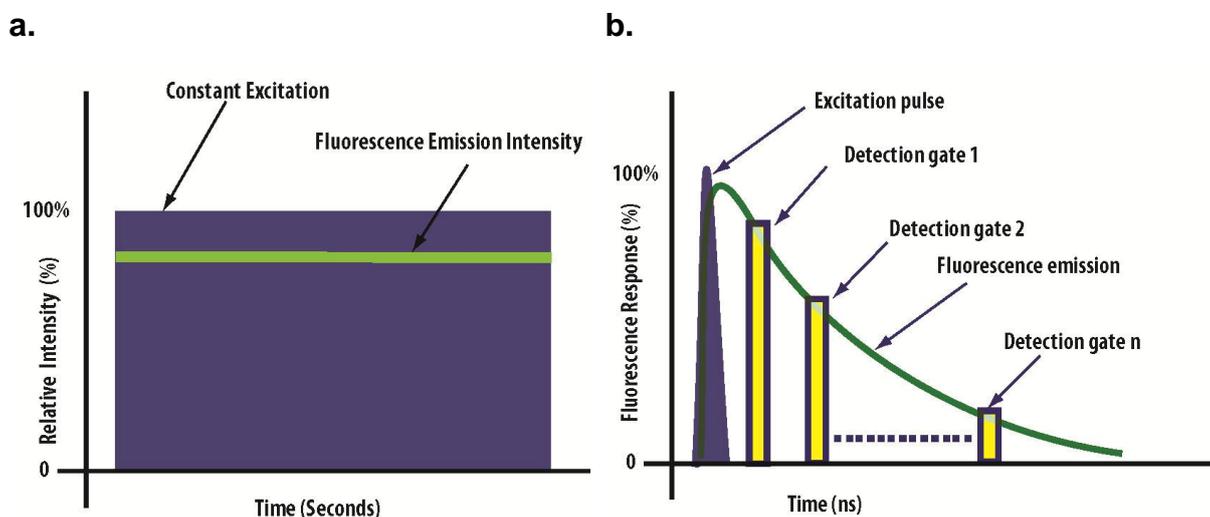
**Figure 2.6 (a) White light image of a specimen of freshly resected bladder (area of fluorescence imaging outlined). (b) Intensity-weighted false-colour FLIM image. (c) Histogram showing fluorescence lifetime distributions from normal and cancerous regions of interest [36].**

## 2.6 Spectrofluorometer

In general, there are two distinct approaches to fluorescence measurement, steady state and time-resolved measurements. The most common type of measurements are steady state measurements which are conducted using constant illumination and observation. The sample is excited with a continuous beam of light, and the intensity of the emitted fluorescence is recorded over a period of time, as shown in **Figure 2.7.a**. Whereas, the second type, illustrated in **Figure 2.7.b**, is conducted by measuring the intensity decays. For this type of measurement, the sample is excited by ultra-short laser pulses that are usually much shorter than the time decay of the fluorescence emission. The intensity decay

is sampled with a very high speed detection system, usually on a picosecond timescale [37].

**Figure title: Concept of steady state and time resolved measurements.**

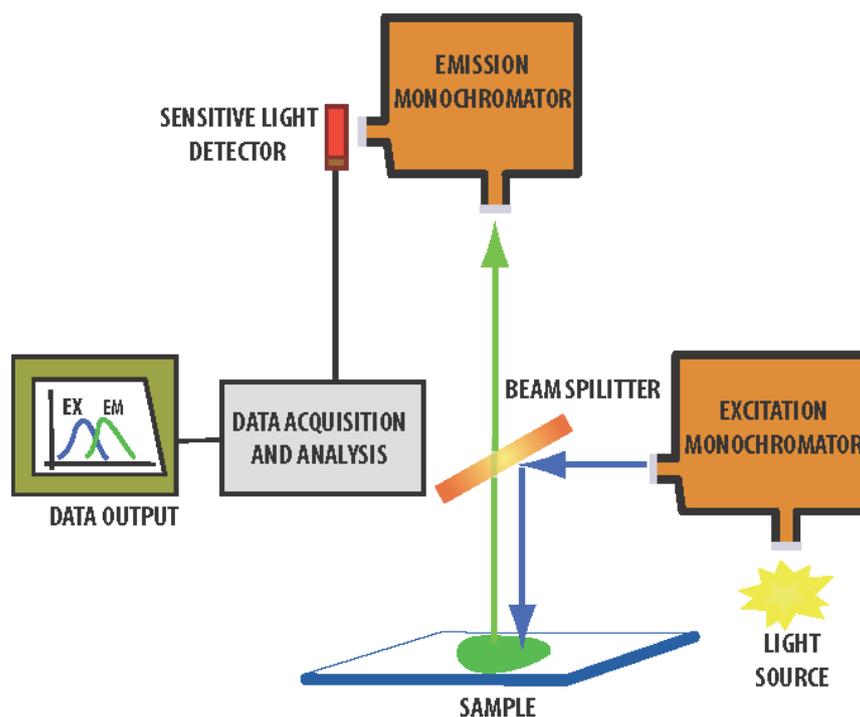


**Figure 2.7 a. Steady state: constant illumination and observation. The level of the fluorescence emission is function of the quantum yield of the targeted fluorophore.**  
**b. Time resolved: pulsed excitation and high speed detection.**

Typically an instrument known as a spectrofluorometer is used for both types of measurement. A schematic of a general purpose spectrofluorometer is shown in **Figure 2.8**. Generally, spectrofluorometers use high intensity white light sources, with a monochromator which allows you to select a certain wavelength, so that the fluorescence sample is excited at the wavelength of interest. Another monochromator is used at the detection side to scan the emission spectra of the fluorescence sample. A precise excitation and emission spectra can be obtained with spectrofluorometers that have the following characteristics:

- The light source must yield a constant photon output at any given wavelength.
- The efficiency of the monochromator must be equal for all wavelengths.
- The efficiency of the light detector must be equal at all wavelengths.

**Figure title: Spectrofluorometer.**

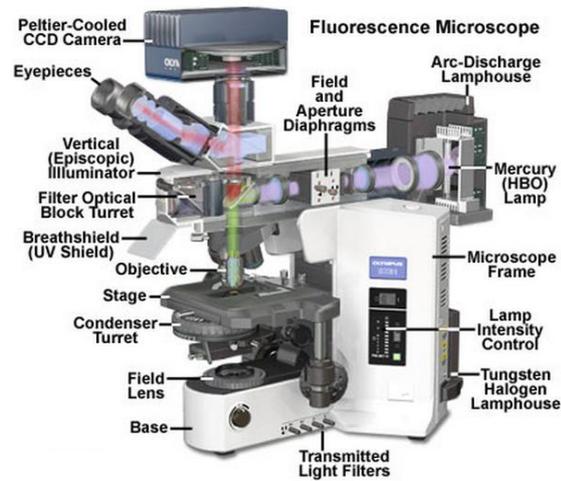


**Figure 2.8 Schematic diagram of a spectrofluorometer.**

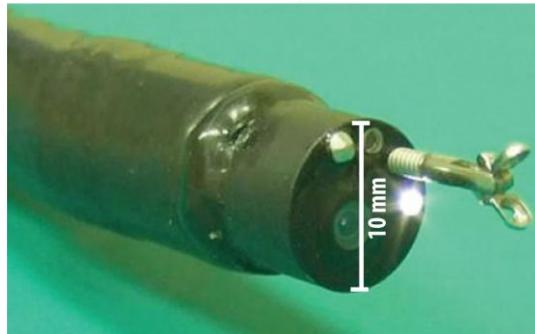
The difference between the two types of measurements can be summarized by how the excitation light is controlled and how the yield output data is processed. In the case of steady-state, the light is kept constant for a period of time, usually a few seconds or more, while the emitted fluorescence is measured continuously. This measurement is repeated at different wavelengths. For time-resolved measurements, the light is replaced by an ultra-short laser pulse generator, usually picoseconds. The detector, which usually consists of an array of micro-detectors (pixels), detects the emitted fluorescence during an observation window, which is synchronized with the laser trigger. The emitted fluorescence is recorded using all pixels for a programmable gated number of times ( $N$ ). Due to the random nature of the fluorescence emission, this measurement is repeated for several windows. At the end of a full measurement, it is possible to sketch a histogram reporting the intensity of fluorescence and the time constant of the fluorescence process, like the one shown in **Figure 2.6.c** [16]. If only one window is used, the sensor provides an average intensity measurement which is often satisfactory for many applications (e.g., DNA micro-arrays) [37].

**Figure title: Fluorescence detection instruments.**

**a.**



**b.**



**Figure 2.9 a. Fluorescence microscope. b. Endoscopic probe used with the Autofluorescence imaging system (AFI, Olympus Medical Systems).**

The spectrofluorometer has developed over many years, and has taken many forms and shapes, that can serve many purposes and applications, ranging from environmental applications, to *in-vivo* and biomedical applications. One of the most popular instruments is fluorescence microscope, shown in **Figure 2.9.a**, which is a combination of a spectrofluorometer and a microscope. The spectrofluorometer used in the microscope shown is equipped with a high sensitivity imager, instead of the single light detector used in conventional spectrofluorometer. In 2007, Olympus Corporation incorporated a spectrofluorometer into an endoscopy system that can be used in the medical field, to detect signs of cancerous tissues in the upper and lower part of the GI tract. The autofluorescence imaging system (AFI, Olympus Medical Systems) incorporates a spectrofluorometer into a conventional endoscope, which enables this system to perform autofluorescence imaging alongside white light imaging. However, The AFI endoscope

can not reach some parts of the GI tract as is the case with conventional endoscopes. Shown in **Fig. 2.9.b**, the AIF probe has an external diameter of 10 mm and is designed to be used in the upper and the lower part of the GI tract. For the 6 meter long small bowel, it is very necessary to have a more noninvasive device, with fluorescence measurement capability that can reach such regions. In this work, we propose a pill that can detect cancer through autofluorescence.

## **2.7 Summary**

This chapter has reviewed the background theory of the fluorescence phenomenon. The mechanism of the fluorescence process and its characteristics that make it useful in many applications have been reviewed. This was followed by a detailed explanation of how indigenous fluorophores are exploited in detecting cancer and abnormalities in the small GI tract. It was also seen that the autofluorescence imaging (AFI) technique, has more capability to detect early signs of cancerous tissues than that of the white imaging techniques. The AIF technique is based on the autofluorescence intensity measurement which can be performed by a simpler instrument known as spectrofluorometer. This instrument is also used to perform other fluorescence measurements such as lifetime measurements. The two main autofluorescence measurement methods have been reviewed, and the detection techniques that are used in both measurements methods were explained. Finally, it was concluded that in order to perform intensity measurements inside the GI tract, the spectrofluorometer instrument needs to be miniaturized into a swallowable pill that can detect the autofluorescence intensity, and then transmit the results to a workstation terminal outside the body.

# Chapter 3 Design considerations of the Pill

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## **3.1 Introduction**

The autofluorescence potential for detecting cancer in the upper and lower part of the GI tract presents a substantial case to justify implanting a pill that can reach the small intestine part of the GI tract. This chapter starts with a review on the existing diagnostic pill technologies. This is followed by a section that reviews existing ultra sensitive light detectors in which a Multi-Pixel Photon Counter (MPPC) is chosen as a light detector for autofluorescence detection. Base on this, and other information from the previous chapter, a design diagram of a pill that is capable of autofluorescence measurements is proposed. A key component of this design is an Application Specific Integrated Circuit (ASIC) that contains a high voltage charge pump and front-end block. A review of both building blokes of the ASIC is presented in this chapter.

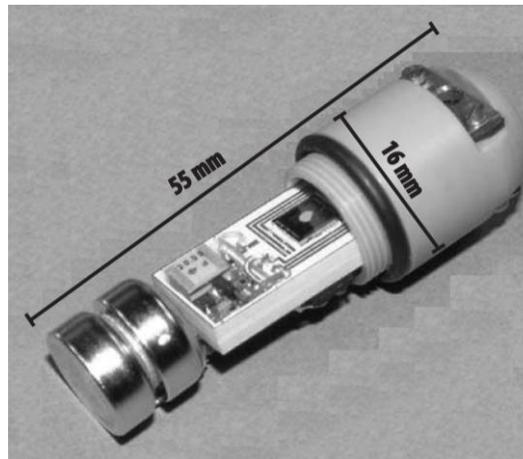
## **3.2 Pills for cancer detection**

The capsule endoscope (CE) is a swallowable wireless miniature camera that allows for noninvasive imaging of all regions of the GI tract. In 2000, for the first time in medical history, the Given Diagnostic Imaging System (Given Imaging Ltd., Norcross, Ga) became the first CE reported to be used in literature, and it was approved by the Food and

Drug Administration (FDA) in August of the same year [38]. Given Imaging Ltd. manufactures the PillCam SB, which evaluates the small intestine, and PillCam ESO for the esophagus. Recently, several new types of capsule endoscope have been developed, such as the Olympus CE for the small bowel, PillCam ESO for investigation of esophageal diseases and PillCam COLON for detection of colonic neoplasias [12]. Biotelemetry capsules are also another type of swallowable pill that allows *in vivo* telemetric studies of the GI tract such as measurements of temperature, pH or pressure [5]. Shown in **Figure 3.1.a** is an example of a swallowable pill developed by the MST group at the University of Glasgow for measurements that including pH, temperature and dissolved oxygen.

**Figure title: Different types of capsules.**

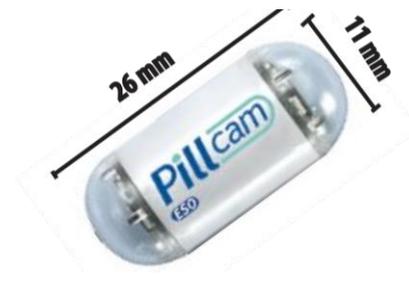
a.



b.



c.



**Figure 3.1 a) . Pill developed by the MST group at the University of Glasgow for in situ measurements such as pH, conductivity temperature and dissolved oxygen. b) Olympus CE for the small bowel c) The PillCam SB developed by Given Imaging Ltd for small bowel white imaging.**

The reported systems consists of three basic parts: the first part is a capsule “endoscope”; the second part is a sensing system composed of sensing pads, a data recorder or transmitter, and a battery pack; and the third part is a personal computer workstation or pocket base station with software that is able to review and interpret the collected data [1]. The capsules produced by Olympus and Given Imaging Ltd. are imaging capsules. The PillCam SB capsule (11 mm × 26 mm, 3.64 g) which is used for small bowel measurements consists of a complementary metal oxide silicon (CMOS) chip imager, a short focal length lens, six white-light-emitting diode illumination sources, two watch batteries and a UHF-band radio telemetry transmitter. Imaging features include a 140° field of view, 1 : 8 magnification, 1- 30mm depth of view and a minimum detection size of about 0.1 mm. The activated PillCam SB capsule captures images at a frequency of 2 frames per second until the battery expires, after about 8 h, which enables the device to take up to 55000 still images (JPEG format). The CE developed by Olympus shown in **Figure 3.1.b** has similar features to that of PillCam SB which is shown in **Figure 3.1.c**. The difference between the Olympus CE and PillCam SB systems is that the Olympus capsule has a higher resolution CCD and an external real-time monitor [2, 39].

Some aspects of consideration for the CE have to be taken into account; one of the most important is the role of bowel preparation. Before the patient takes an endoscopic pill, the whole bowel has to be prepared, in order to have adequate visualization and reliable results. Dark fluid, debris, and bubbles in the lumen can obscure the mucosa and result in missed artifacts, therefore preparation liquids are used to clean the bowel prior to CE usage. Some studies have looked at oral sodium phosphate preparation and some have looked at polyethylene preparation, all studies have concluded that bowel cleansing has improved the quality of the images [40]. Another problem, known as regional transit abnormality where the capsule remains in a particular region of the small intestine for a period of more than 60 minutes, results in increasing the test time and as a result, the battery may run out of power before the test is complete. Patients with known gastroparesis or suspected small intestinal dysmotility are highly likely to encounter this problem. This problem can be overcome by using prokinetics prior to CE. A prokinetic is a type of drug that enhances gastrointestinal motility by increasing the frequency of contractions in the small intestine, this results in shortening of the small intestine transit time [41]. One of the most serious complications that can accompany the use of endoscopic capsules is known as capsule retention, which is defined as the presence of a capsule in any part of the GI tract for at least two weeks. Study [42] shown that 5 retention cases out of 100 patients in whom a CE was performed. In another study [43] the retention rate was 1.9%, in these cases

surgical or endoscopic retrieval was required [38]. Both studies agreed that a high rate of the cases that had the retention problem occurred with patients with suspected bowel obstruction or confirmed Crohn's disease.

CEs are mainly employed to detect tumours and abnormal blood vessel formations in the small intestine, where conventional endoscopy devices are unable to reach [2, 44]. However, CE is not the only method of detecting cancer and other abnormalities in the small intestine. Methods such as radiological imaging and intraoperative endoscopy are also employed for the same purpose. Several studies have however demonstrated that capsule endoscopy helps detect more tumors than radiologic imaging. [40]

In a comparative study conducted by [45], intraoperative endoscopy was regarded as the gold standard for complete small intestine evaluation. However, intraoperative endoscopy is always considered as a last option for evaluation of the small bowel [40] as it is usually performed in an operating room with the patient under general anesthetic. An endoscope is inserted into the bowel by the surgeon and passed through the small bowel manually, while the gastroenterologist views the image [46]. Therefore, when comparing with the methods mentioned above, CE is seen to be less invasive and therefore more appropriate as the first response for diagnosis of abnormal growth in the small intestine [45].

### **3.3 Pill for cancer detection through autofluorescence**

As was mentioned in previous chapter, autofluorescence detection techniques have been employed in upper endoscopy systems in order to enhance the performance of these devices and increase their capability of detecting abnormalities in the upper and the lower part of the GI tract. Therefore it is expected that introducing this feature and incorporating it into a CE will improve the capability of CEs in detecting cancer in its early stages.

#### **3.3.1 Operating wavelengths**

A difference between intensities of cancerous tissues and normal ones have been confirmed in several studies that were conducted *in vivo* as mentioned in the previous section. The main objective of our work is to incorporate a spectrofluorometer into a swallowable diagnostic pill capable of detecting these differences. The spectrofluorometer shown in **Figure 2.8** can be used for general purpose tasks. However, our

spectrofluorometer will be an application specific one that will be dedicated to do a specific task. Limiting the operation of the spectrofluorometer to a specific task is accomplished by limiting the operation wavelengths to specific bands. By applying this limitation, the proposed pill will lose some functionality but gain two advantages; the first one is the size, which will be smaller than a device that operates over the entire ultra-violet and visible bands. The second advantage is the power consumption, which will be reduced when operating at a specific band, rather than scanning the entire visible spectrum.

**Table 3.1 Summary of autofluorescence spectra obtained by different studies for healthy and cancerous tissues of the GI tracks.**

Study	Excitation source band	Collected autofluorescence range	Wavelength where maximum fluorescence difference occurred	Tissues with higher intensity	Part of GI tract	
[35]	370nm± unknown	400-700nm	470nm	Normal tissues	Colon	<i>in vivo</i>
[9]	425±52nm	470-700nm	520nm	Normal tissues	Stomach	<i>in vivo</i>
[34]	351± 40nm	400-550nm	445nm	Cancerous cells	Esophagus	<i>in vivo</i>
[31]	405±unknown	500-700nm	510nm and 630nm	Normal tissues then cancerous cells respectively	Colon	<i>in vivo</i>
[6]	557±67nm	470-870nm	520nm	Normal tissues	Colon	<i>in vivo</i>
[33]	425±52nm	470-700nm	520nm	Normal tissues	Colon	<i>in vivo</i>
[32]	425±52nm	470-700nm	520nm	Normal tissues	Esophagus	<i>in vivo</i>

In order to achieve the goals specified above, we must determine the best operational excitation source band and corresponding detection band. As explained in **section 2.42.4**,

every fluorophore has an optimal excitation wavelength at which it yields the maximum autofluorescence emission. These optimal wavelengths are to be decided according to the information obtained from studies [6, 9, 31-35]. **Table 3.1** lists the excitation light bands used in every study. It can be concluded from the wavelengths used to excite the tissues in most of the mentioned studies that the excitation source should ideally operate at wavelengths ranges between 390-470nm. Whereas, the optimal difference between the auto fluorescence intensity of the normal tissues and the cancerous one mostly occurred at 520 nm. In order to allow the greatest separation between excitation and fluorescence wavelengths, we have therefore chosen 520 nm to be our detection wavelength.

### 3.3.2 Autofluorescence detectors

The most important part in the spectrofluorometer instrument illustrated in **Figure 2.8** is the fluorescence detector which is simply a light detector that is capable of detecting photons with wavelengths in the range 470-700 nm. For detecting fluorescence sample of an exogenous fluorophores, a photodiode can be used [47, 48]. However, when detecting autofluorescence generated from living organisms such as human tissues, special practical considerations have to be taken into account; specifically that the autofluorescence emission is relatively weak compared to that emitted from exogenous fluorophores, which have to some extent been selected or designed to fluoresce efficiently[14]. Some exogenous fluorophore can have a quantum efficiency (QE) up to 1.0 whereas indigenous fluorophores in human tissues can have QE equal to 0.00038 [18, 19]. Therefore detecting autofluorescence requires a more sensitive light detector and a more powerful excitation light. Photomultiplier tubes (PMTs) have traditionally been the device of choice for this due to their very high sensitivity [10, 49]. However, PMTs are usually expensive, and have limited photon detection efficiency, ranging from (2% to 20%). In our case, where the size of our CE device is very critical, PMTs are not suitable due of their bulky size and the very high voltage required to operate them, typically in the region of kV [14].

The solid state alternative to MPT is Charged Couple Devices (CCDs). Measurements of autofluorescence emissions produced by human tissues reported by [6, 9, 31-35] used CCD imagers with high intensive light sources for excitation such as the 300 W short-arc xenon lamp (Storz GmbH, Tuttlingen, Germany) which were used on [9, 32, 33], Having such a powerful excitation source allowed the CCDs to detect the fluorescence emissions produced by heavily induced endogenous fluorophores. In the case of the Olympus endoscopy system, the excitation source is an array of LEDs with moderate light intensity,

consequently in order to guarantee good detection with the moderate excitation offered by the LEDs, a newly developed CCDs with high sensitivity was incorporated into the end-probe of the system.

When developing a CE, power is a major issue and using a powerful excitation source for excitation becomes impractical if not possible. Based on the linear relationship between the excitation intensity and the autofluorescence emission, the lack of a high intensity light source can be compensated by using an ultra sensitive light detector to measure the weak autofluorescence emission. A single Photon Avalanche Photodiode (SPAD) has the ability to detect light at photon level and they can be a suitable alternative to CCDs [50]. In addition, when compared to CCDs, SPADs consume much less power [51]. Another key advantage of SPADs over the CCD is that they can be fabricated in the commercially available CMOS technology, whereas CCDs require special silicon process which can not be cheaply realized [50, 52]. Fabricating in commercially standard CMOS offers a great opportunity for full integration of the detector, the analog and digital processing, and the control circuits on the same chip [53]. Furthermore, SPADs need no cooling and can operate at normal room temperature, whereas CCD's must be cooled due to their relatively high dark current [54].

Photodiodes are another type of sensitive light detector which are compatible with CMOS process like SPADs. However, in comparison with SPAD which has high gain that can reach more than  $10^6$ , photodiodes do not have gain and therefore require an extra amplification process or an integrated current mode analogue to digital convertor (ADC) [18]. Furthermore, autofluorescence generated by endogenous fluorophores, such as NADH, FDA flavin and tryptophan, which are primary endogenous fluorophores, usually have very low biological concentration which can vary up to 135  $\mu\text{M}$  (mole/L), 301 nM and 98  $\mu\text{M}$ , respectively. SPAD has been confirmed to be capable of detecting fluorescence generated by fluorophores with a concentration as low as 10 nM using 16x 4 array of SPADs, whereas a 250x250 array of photodiodes is used to detect the same concentration. [55-57]. With the advantage of the internal gain of the SPAD, and the higher sensitivity, SPADs are selected to be the detector of choice for this work.

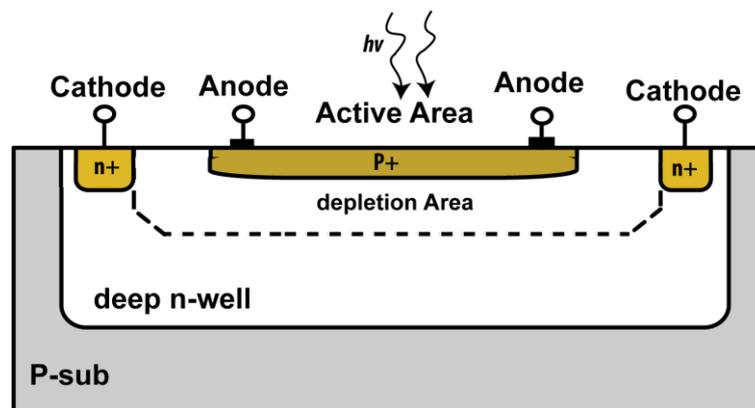
### **3.3.3 Single Photon Avalanche Diodes (SPADs)**

An avalanche photodiode (APD) is a highly sensitive semiconductor that can detect light at photon count level. The concept of photon counting techniques has been developed over

many years by exploiting the operation of MPTs [58]. This concept was exported to semiconductor technology and resulted in the development of single-photon avalanche photodiodes (SPADs). Essentially, APDs are p-n junction diodes that are purposely made to operate at high electric field in order to achieve an internal gain [59]. When reverse biased, the electric field increases with the biased voltage, which causes the drift velocity and kinetic energy of charge carriers injected in the depletion region to increase. As a result, an electron (or a hole) can reach to an energy level that is high enough to break a bond when colliding with lattice atoms. This causes generation of a new electron-hole pair, and consequently loses part of its energy. This process is called impact ionization. Both the original carrier (electron or hole) and the secondary electron and hole will be accelerated by the electric field and participates in generating more electron-hole pairs. This process triggers generating events of a huge number of carriers, hence the term avalanche [59].

An example of an APD in CMOS is shown in **Figure 3.2**. APD can operate in two different ways depending on whether the bias voltage is below or above the breakdown point [60]. If the reverse bias is below the breakdown point of the APD, each absorbed photon creates on average a finite number  $M$  of electron-hole pairs. This mode of operation is called ‘linear’ because the number of collected carriers is proportional (by a factor of  $M$ ) to the number of absorbed photons, normally in the range between a few tens and a few hundreds [59].

**Figure title: CMOS APD**

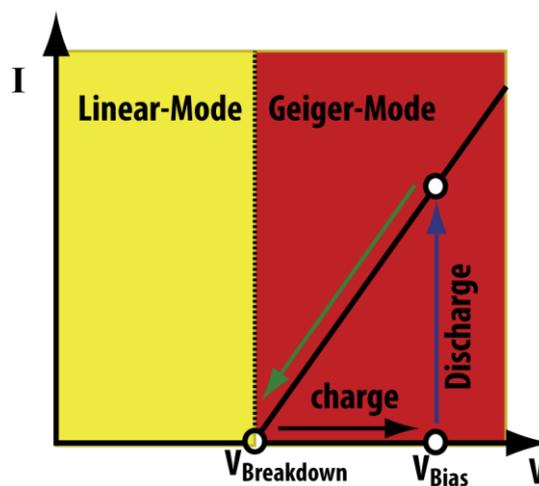


**Figure 3.2 Cross section of CMOS APD.**

The second way of operation is achieved by biasing the APD above the breakdown point. This mode of operation is known as ‘Gieger mode’ and in this case, the APD is called (SPAD). At this bias condition, the electric field is so high that a single carrier injected into the depletion region can trigger a self-sustaining avalanche. The current rises sharply to a

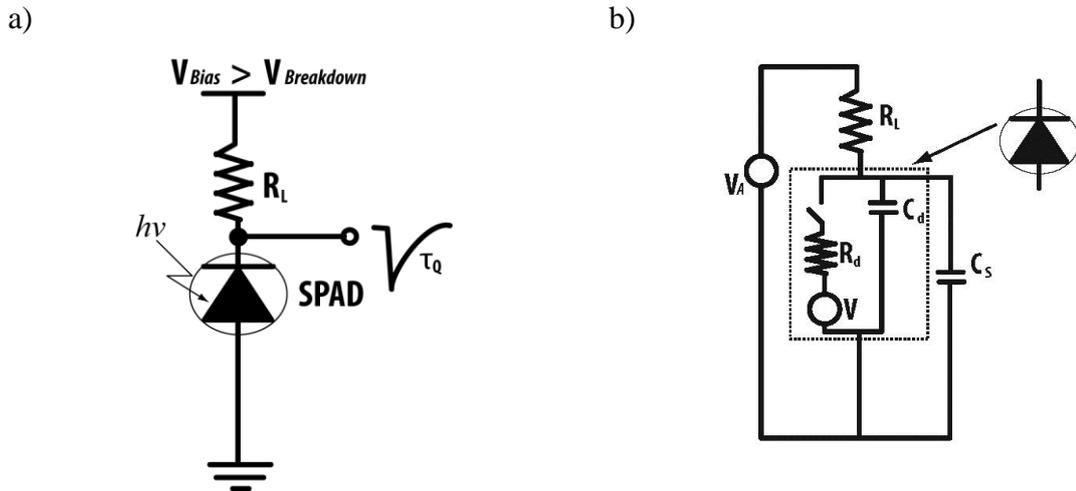
microampere level, sometimes into the milliampere range [58, 61]. The carrier initiating the avalanche can be either thermally generated (noise source of the device) or photogenerated (useful signal). If the carrier is photogenerated, the leading edge of that avalanche pulse marks the arrival time of a photon with a precision of a few picoseconds. The current keeps flowing until the avalanche is quenched and the biased voltage lowered down to or below the breakdown voltage  $V_{Breakdown}$ , then the reverse bias returns to  $V_{Bias}$  by recharge, so Geiger mode operation can begin again and be ready to detect another photon. This is illustrated in **Figure 3.3** [58].

**Figure title: Geiger-mode operation principle**



**Figure 3.3 Principle of Geiger mode APD operation summarised in three steps: 1) Discharging: the APD discharges when a photon hits the active area of the APD. 2) Quenching: when the current flows through the quenching resistor, the reverse voltage drops to  $V_{Breakdown}$ . 3) Recharging: the reverse bias returns to  $V_{Bias}$  by recharge, so Geiger mode operation starts again [59].**

In Geiger mode, when biased above the breakdown voltage, if the SPAD is connected directly to a voltage supply the avalanche process will be self-sustained. To create a system that can be used to detect single photons, the avalanche process initiated by each photon must be quenched by reducing the voltage across the photodiode whenever a photon is detected. This means that the photodiode must be connected to the high biasing voltage via a device that reduces the voltage across the photodiode whenever a charge pulse occurs.

**Figure title: Quenching circuit**

**Figure 3.4 a) Basic Passive Quenching Circuit (PQC). b) Equivalent circuit of the PQC.**

In order to quench the avalanche process, a suitable circuit, usually referred to as a quenching circuit, must be used. The most popular and simplest quenching circuit is known as a Passive Quenching Circuit (PQC), shown in **Figure 3.4.a**. Here, the SPAD is reverse-biased through a high ballast resistor  $R_L$ . When no current is flowing ( $I_D=0$ ), the SPAD cathode is reverse-biased at  $V_{Bias}$ , therefore the diode bias voltage  $V_D$  equals  $V_{Bias}$  (the total reverse bias). Once a photon strikes the active area of the SPAD, the multiplication process fires the avalanche and the current swiftly rises (in picoseconds time) to a few milliamperes at its peak which is given by [61]

$$I_{Peak}(0^+) = \frac{V_{Bias} - V_{Breakdown}}{R_d} \quad 3.1$$

where,  $V_{Bias} - V_{Breakdown}$  is the excess voltage ( $V_{ex}$ ) above the break down voltage and  $R_d$  is the diode resistance of the SPAD, which is in parallel with  $C_d$  the junction capacitance (typically  $\sim 1\text{pF}$ ), as shown in the equivalent circuit in **Figure 3.4.b**. This current discharges the parasitic capacitance ( $C_s$ ) at the cathode node, so the excess voltage decreases exponentially towards zero with a time constant given by [61].

$$\tau_Q = (C_d + C_s)R_L // R_d \quad 3.2$$

The overall bias voltage at the cathode of the SPAD never drops beyond the breakdown voltage, so the avalanche is not quenched and the current continues to flow through the SPAD. The final current value is given by [61]

$$I_f = \frac{V_A - V_B}{R_d + R_L} \quad 3.3$$

If  $I_f$  is very small, the current intensity becomes slow and therefore the number of carriers that cross the avalanche region is so few that the multiplication process can not take place and the avalanche is said to be self-quenching. On the other hand if  $I_f$  is high enough, the presence of carriers is increased and the probability for the multiplication process to happen becomes high. In this case, it can be said that the avalanche is self-sustaining. This imposes a minimum value of  $R_L$  that will be high enough to force the SPAD to be self quenched. For this value to be determined, a threshold value for  $I_f$  is often assumed to be (100  $\mu$ A). This value is referred to as the “quenching threshold” [62]. When the SPAD is quenched, it recharges again to its initial bias voltage, hence is ready for the next photon to be detected. The time which is required for the SPAD to be ready to detect another photon can be calculated by equations **3.1** and **3.2**. For an excess voltage  $V_E$  equal to 5 V and for  $I_{peak}$  equal to 200  $\mu$ A, the  $R_d$  is 25 k $\Omega$ . Therefore, by using external  $R_L$  equal to 100 k $\Omega$  and for large  $(C_d + C_s)$  equal to 10pF, the SPAD needs 400 ns to be ready to detect another photon after each quenching process. This 400 ns is considered as a dead time in which other photons hitting the active region can not initiate an avalanche process.

SPADs are sometimes quenched using a technique called active quenching. The Active Quenching Circuit (AQC) exploits the steeped rising edge of the avalanche pulse and employs a circuit that senses the rising edge and acts to force the SPAD to quench immediately, therefore preparing the SPAD for another avalanche [58, 63]. This technique reduces the quenching time constant which results in increasing the dynamic range of the SPAD, reducing the power dissipation and allowing for very fast measurement to take place, such as the fluorescence lifetime measurements [37, 62].

The performance of any SPAD can mainly be characterised by three parameters:

**a. photon detection efficiency**

The performance of a SPAD is primarily determined by its Photon Detection Efficiency (PDE). For a photon to be detected, it is not enough to hit the active area of the SPAD and generate a primary carrier (electron-hole pair), it is also very important for that carrier to trigger an avalanche. Increasing the excess bias voltage improves the detection efficiency as a photon is more likely to create an avalanche if the electric field is high [64].

**b. dark-count rate**

Thermal generation affects the performance of SPAD by causing it to generate current pulses even in the absence of illumination. The Dark Count Rate (DCR) constitutes false counts and is a measure of how noisy the detector is. The larger the number of dark carriers, the larger the dark-count probability is. As is the case of the PDE, the DCR also increases at higher bias voltages, since the probability of a thermally generated carrier producing an avalanche increases [65].

**c. Detection Probability**

As not all the incident photons will generate a pulse, the ratio of the generated pulses to the incident photons is referred to as the Photon Detection Probability (PDP). In the photon detection process, some photons are not absorbed, or if they are absorbed, they do not trigger an avalanche. The highest PDP occurs when the SPAD is biased at certain voltage above the break down voltage [66].

The main limitation of an SPAD operating in the Geiger mode, whether with active quenching or passive quenching, is that the output pulse is independent of the number of photons that are hitting the active area. This is attributed to the dead time that is spent after each avalanche process. In order to partially overcome this limitation, an array of SPADs is connected in parallel to a single output. Each SPAD when hit by a photon, generates the same current response, so the output signal is the sum of all the signals and is proportional to the number of SPADs hit by photons. The dynamic range is limited by the number of SPADs in the device, and the probability that two or more photons hit the same SPAD depends on the size of the SPAD itself. This structure is called a Silicon Photo Multiplier

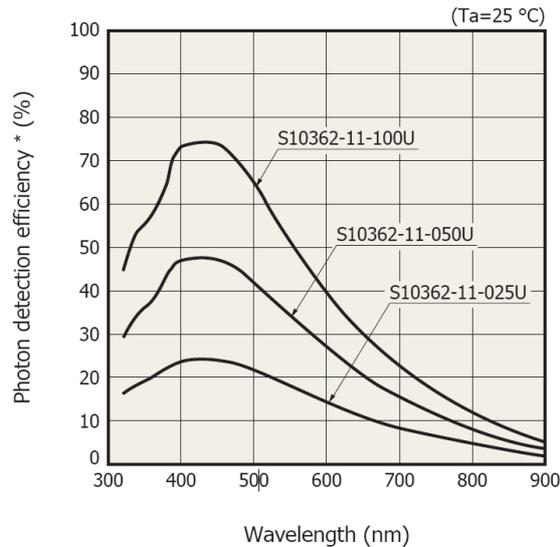
(SiPM) [60]. Using such devices offers a higher sensitivity to that offered by a single SPAD.

### 3.3.4 Photon multiplier Multi-Pixel Photon Counter (MPPC)

The MPPC (Multiple Pixel Photon Counter) newly developed by HAMAMATSU PHOTONICS K.K. is a commercial SiPM device that offers higher sensitivity to that of a single SPAD. The MPPC basically consists of multiple avalanche photo diode (APD) pixels connected in parallel and operating in Geiger mode [61]. The ability of the MPPC to detect extremely weak light at photon counting level makes it the best choice for our application. The device has: a very high gain ( $10^5$  to  $10^6$ ); bias voltage operation of  $<100\text{V}$ ; room temperature operation; low dark count rate ( $<1\text{MHz/mm}^2$ ); high Photon Detection Efficiency (PDE) (as **shown in Fig. 3.5**); is not sensitive to magnetic field; low power consumption and mechanical robustness [67, 68].

The MPPC is a combination of an integrated Geiger-mode APD and quenching resistor. The quenching resistor value is typically a few hundred  $\text{k}\Omega$ . The combination of Geiger mode APD and a resistor makes one pixel. Several pixels are connected together to make up the MPPC.

Hamamatsu has produced three types of MPPC, with 100 pixels (S10362-11-100U), 400 pixels (S10362-11-050U) and 1600 pixels (S10362-11-025U). The 100 pixel device has a fill factor of 78.5%, whereas for the 400 pixel device it is 61%, and 30.8% for the 1600 pixel device. The high fill factor of the 100 pixel means it has the highest PDE among the family, as shown in **Figure 3.5**. The very high PDE offered by the 100 pixel MPPC is desirable for extremely low-light detection applications such as autofluorescence [67]. However, there is trade off between the PDE and the input dynamic range [20]. The MPPC device can give an indication of how many pixels have been hit, regardless of the number of photons that might hit a single pixel at the same time. Since all pixels are connected to one readout channel, the output pulses from the APD pixels overlap each other creating one large pulse. By measuring the height, or the electrical charge of this pulse, the number of photons detected by the MPPC can be estimated [67].

**Figure title: Photon detection efficiency**

**Figure 3.5 Photon detection efficiency (PDE) for three types of MPPCs [67]. The MPPC (S10362-11-100U) has the highest PDE (60%) at 520nm.**

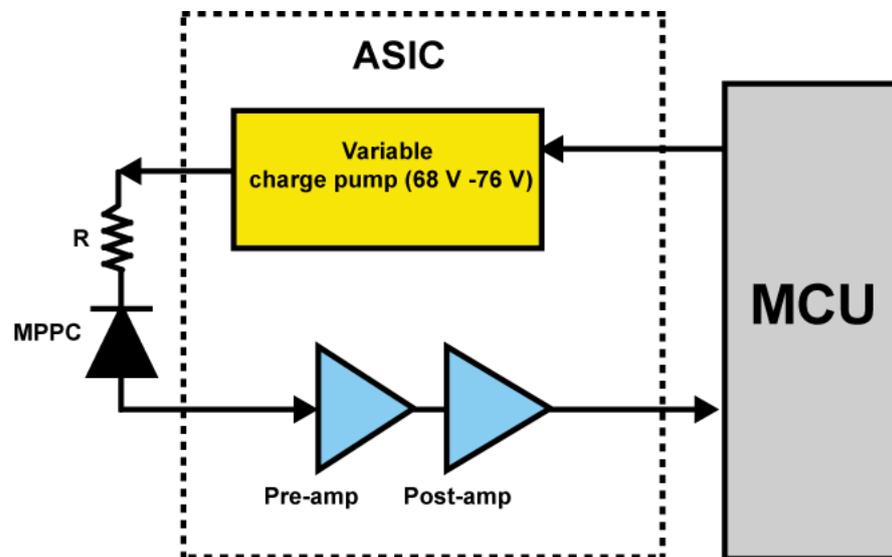
The capsule will incorporate the MPPC device with 100 pixels (S10362-11-100U) which has the highest PDE (60 %) at 520nm thus reducing the required excitation light as much as possible. The signal produced by the device when all the 100 pixels are hit by one or more photons should give a clear indication that the region being scanned is a normal region. If the device produced several weak signals, this should give an indication that the region being scanned is a cancerous region. Furthermore, the decision of determining whether the readings are accurate or not will also depend on parameters like the movement rate of the capsule, the average area of excitation coverage, the detection frequency and others. Such parameters must be investigated to ensure high accuracy of decision making.

### **3.4 Proposed pill**

#### **3.4.1 Application Specific Integrated Circuit (ASIC)**

In order for any diagnostic capsule to be used in the GI track, it has to have a reasonable size so that it can be swallowable. Therefore, the components to be incorporated into this capsule must each be as small as possible including the battery. This means they must also consume very low power. Rapid developments in nano-technology enable us to achieve low-power and very small systems on a chip (SoC) and therefore design a miniaturised endoscopy capsule.

**Figure title: System block diagram**

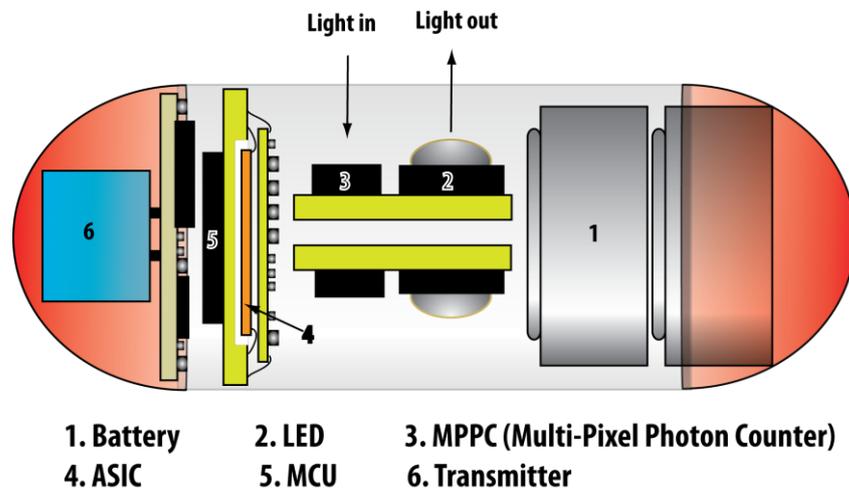


**Figure 3.6 Block diagram of an autofluorescence cancer detection system using a MPPC as a light detector.**

The complete system is designed to acquire and process the signal provided by the MPPC device. The heart of this system is a microcontroller unit (MCU), which obtains and processes a digitised signal provided by an application-specific integrated circuit (ASIC). The ASIC has been designed according to the unique specifications of the MPPC and its operational requirements. The main building blocks of the system are illustrated in **Figure 3.6**. Basically, the ASIC consists of two main blocks; the first one is a variable high voltage DC-DC converter to provide the needed biasing voltage for the MPPC. The second main block is the front-end which will act as an interface between the MPPC the MCU.

The AMS H35 process provided by Austriamicrosystems has been chosen for designing the ASIC, the main features of this process is its ability to combine the high voltage and standard devices in the same substrate. Most of the ASIC blocks were designed from transistor level, however some existing IP blocks provided by the AMS library were used whenever it was possible.

**Figure title: Capsule layout**



**Figure 3.7 Proposed capsule for cancer detection through autofluorescence using MPPC as a light detector.**

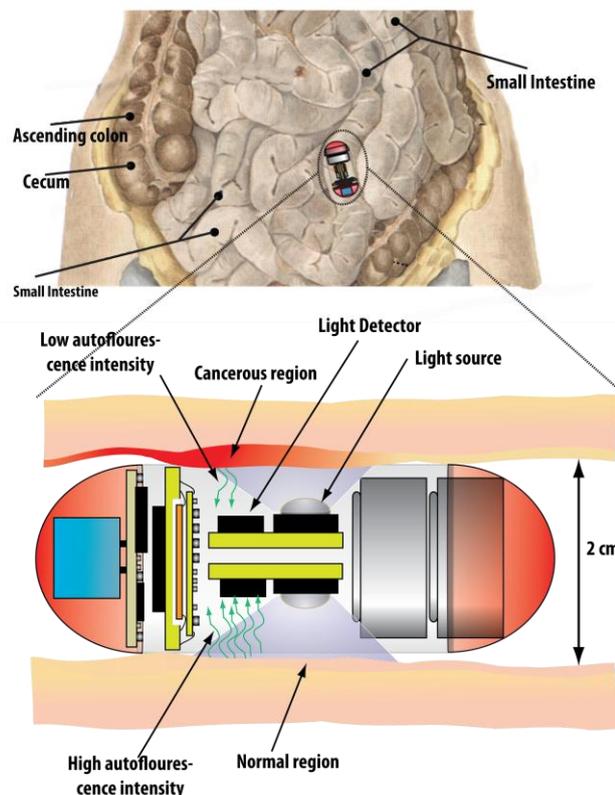
Based on the concept of the spectrofluorometer and the requirement of the ASIC, the capsule layout and its fundamental features are sketched in **Figure 3.7**. The capsule consists of six main parts; a Blue LED as an excitation source, a MPPC device, ASIC, microcontroller unit, transmitter and batteries.

### 3.4.2 Scanning approach

The proposed capsule was inspired by the autofluorescence Imaging (AFI) system from Olympus which could stream linear data to a workstation near to the patient being examined. This method is a labour-intensive surveillance strategy [69]. Instead of dealing with thousands of images for the entire 6-meter-long small-intestine, this capsule is designed to acquire intensity measurements which can be plotted into a single graph. Possible cancerous regions are determined if a significant drop below a certain threshold was measured. This strategy will reduce the complexity of the system to be incorporated into the capsule and therefore minimizes the size as well as the power consumption.

Most of the CEs which adopt this imaging strategy are equipped with imagers and light sources which are usually placed in the front-end of the CE. However, using the same approach to measure the ultra-weak autofluorescence emissions by placing the MPPC at the front-end of the capsule may result in faulty readings. For an ideal setup as we have discussed in **Section 2.62.6**, the MPPC should be placed consistently at the same distance away from the targeted sample to ensure that the 2 cm diameter of the intestine walls are induced by the excitation light uniformly [70]. This can be achieved by using a capsule with wide diameter, as close as possible to 2 cm diameter of the small intestine.

**Figure title: Autofluorescence detection principle**



**Figure 3.8 Principle operation of the proposed capsule as it is making its way through the small intestine.**

To overcome this problem, our proposed capsule adopts a scanning approach in which two MPPCs and LEDs are placed in the sides of the capsule, so that the MPPCs will be at the same distance away from the targeted sample throughout the small intestine. The same concept is applied to the LEDs which are situated next to the MPPCs and will be at the same distance from the intestinal wall all the time. Shown in **Figure 3.8**, an illustration of the capsule and the operation principle of the scanning approach that is adopted.

### **3.5 ASIC main building blocks: a review**

#### **3.5.1 Charge pump: a review**

Since the discovery of electricity, generating a high voltage supply from an available low voltage supply has been desired for many applications. The first attempt to accomplish this was carried out by the British physicist and chemist Michael Faraday in 1831. For this purpose, he used electromagnetic induction and transformers [71]. This invention was later adopted by many scientists and inspired numerous techniques to improve the basic transformer design, and thus generate high voltages with high efficiency. However, a transform only works with an alternating input voltage source, whereas, quite often, electronic circuits require DC supply voltages. Therefore, the AC output voltage generated from the transformer is converted to a DC voltage using a rectifier circuit. However, generating a high DC voltage through use of a transformer and rectifier increases the complexity of the circuit and it can become very large, heavy and inefficient. This is especially inconvenient in applications where small size is important. Furthermore, for applications which use a DC voltage source as the primary supply ( i.e. battery), transformers are useless. This is also true for other kinds of transformers that requires an AC input supply such as piezoelectric transformers (PZT) [72].

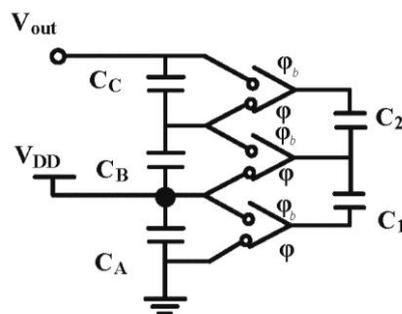
In this work, where the power supply is a DC source, a DC-DC converter is used to convert the DC input voltage ( $V_{in} = 3 \text{ V}$ ) to more than 72 V (DC), and to deliver more than 70  $\mu\text{A}$  which is required to operate the MPPC. As the power supply is limited, it is very critical for the DC-DC converter to achieve high efficiency as much as possible ; in a recent publication where  $V_{out}$  has a gain of 20, the converter has achieved more than 35% efficiency [73]. One type of DC-DC convertor that can achieve high gain and high efficiency is called a boost converter, which requires at least two semiconductor switches (a diode and a transistor) and at least one or two energy storage elements (inductors) for one stage to be implanted. However, for such device to be integrated in a CMOS chip, the breakdown limit imposed by the technology will dictate the number of stages required. Therefore, the number of inductors will increase as the number of stages increases. For this reason, boost DC-DC converters are usually implanted off chip especially for applications where there is no restrictions on space [74, 75]. Another type of DC-DC converter is known as a charge pump; in which a capacitor is used as a storage element. Unlike

inductors that are used in the boost converters, capacitors uses less area whether implemented on chip or off chip which is a good advantage especially for the capsule application where area is very limited [76]. Therefore, the charge pump was adopted in this work to supply the high bias voltage for the MPPC.

### 3.5.1.1 Dickson Charge pump

The first type of charge pump was implemented by the Swiss physicist Heinrich Greinacher. He was the first to propose a circuit capable of converting a low DC input voltage to a high DC output voltage. This was achieved by cascading stages consisting of a diode and capacitor in series. This method was later adopted and used by Douglas Cockcroft and Ernest Thomas Walton to generate 800 kV volts. This high voltage was used by them to power their particle accelerator. They used this accelerator for investigations into subatomic physics and helped them, in 1951, to win the Noble Prize for Physics for their research entitled "Transmutation of atomic nuclei by artificially accelerated atomic particles". The 800 kV was generated by multiplying the 200 kV generated from a transformer by a voltage multiplier that used an elaborate stack of capacitors connected by diodes acting as switches [77].

**Figure title: Cockcroft Walton circuit**



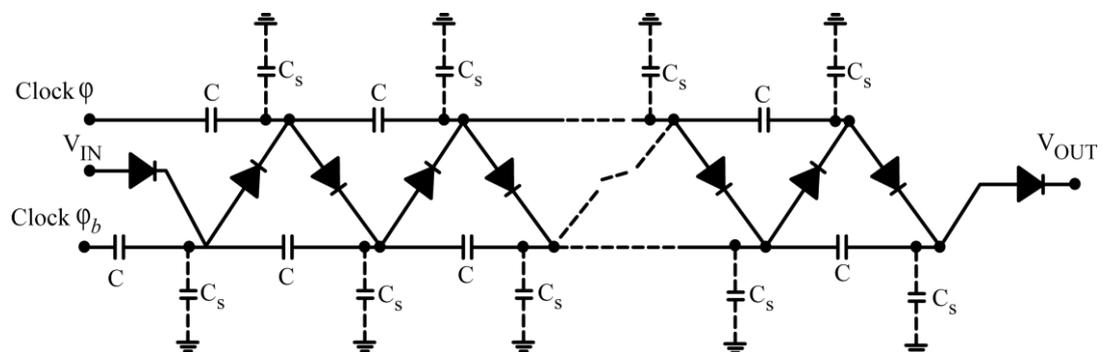
**Figure 3.9 Cockcroft Walton multiplying circuit principle of operation.  $\phi$  and  $\phi_b$  correspond to the switch phases.**

The Cockcroft Walton multiplying circuit is shown in **Figure 3.9**. Three capacitors,  $C_A$ ,  $C_B$  and  $C_C$  are connected in series. Capacitor  $C_A$  is connected to the supply voltage  $V_{DD}$ . Capacitor  $C_1$  is connected to  $C_A$  by a switch which can be practically implemented by a diode. When phase  $\phi$  is on it is charged to voltage  $V_{DD}$ . During phase  $\phi_b$ , the charge in  $C_1$  will be shared with  $C_B$  and the same amount of charge, proportional to  $V_{DD}/2$ , will be

stored in each capacitor if they are equal. In the next cycle,  $C_2$  and  $C_B$  share a charge proportional to  $V_{DD}/4$ , while  $C_1$  is once again charged to  $V_{DD}$ . If this operation is continued for several cycles, charge will transfer to all capacitors until the voltage at the output node reaches  $3 V_{DD}$ . This principle can be easily extended by adding more capacitors and switches so that any multiple of the supply voltage,  $V_{DD}$ , may be achieved.

A practical implementation of the Cockcroft Walton multiplier is shown in **Figure 3.10**. In this configuration it is very important to note that, because the coupling capacitors are connected in series, efficient multiplication will occur only if the coupling capacitors ( $C$ ) are much greater than the stray capacitances ( $C_s$ ). Therefore, this configuration is always implemented with discrete components, where sufficiently large capacitors can be employed. When implemented in monolithic integrated form, the Cockcroft Walton multiplier becomes somewhat inefficient due to the large (compared with the lumped capacitances) stray capacitance at the nodes of each stage. Consequently, the efficiency of the multiplier is degraded. Furthermore, the output impedance increases rapidly with the number of multiplying stages [77, 78].

**Figure title: Implementation of Cockcroft Walton circuit**

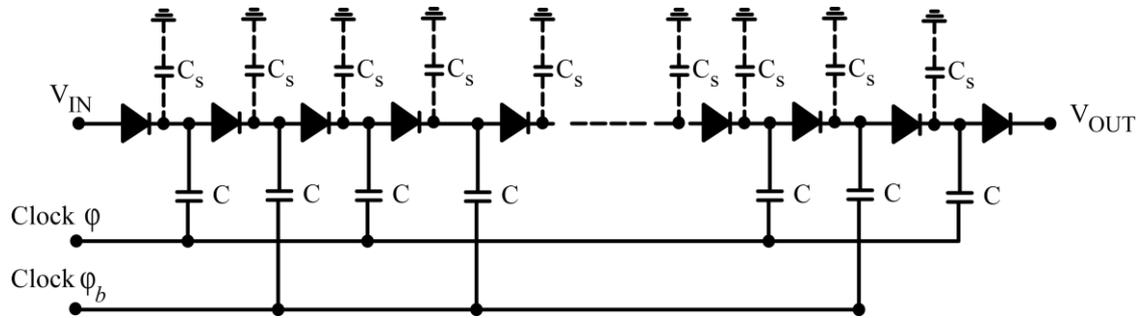


**Figure 3.10 Implementation of Cockcroft Walton multiplying circuit using diodes.**

To overcome these limitations, an alternative charge pump topology which is more suited to monolithic integration was proposed by John F. Dickson [78]. The introduction of the Dickson charge pump has made it possible for circuits that operate with both high and low supply voltages to be implemented on the same chip and to share the same primary power supply. Furthermore, the continuous scaling down of IC technology has increased the demand for the charge pump to be employed in a vast variety of integrated systems such as

operational amplifiers, voltage regulators, switched capacitor circuits, SRAMs, LCD drivers, piezoelectric actuators, RF antenna switch controllers etc [79].

**Figure title: Dickson charge pump.**



**Figure 3.11 Implementation of the Dickson charge pump using diodes.**

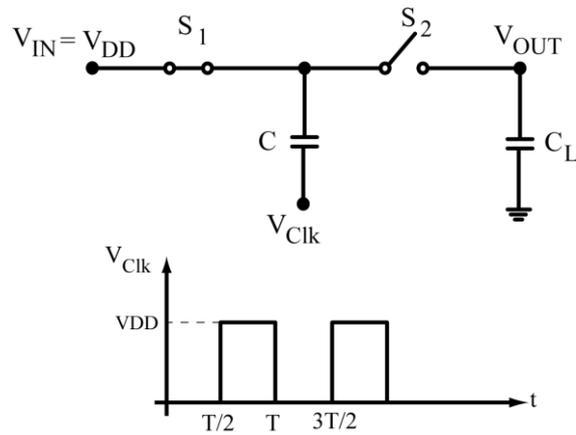
**Figure 3.11** shows the first implementation of the Dickson charge pump. It operates in the same manner as the Cockcroft Walton multiplier. However, unlike the Cockcroft-Walton multiplier, the coupling capacitors are connected in parallel to the diode nodes instead of in a series configuration. Capacitors in a parallel configuration have to withstand the full voltage at the end of each node which implies a limit to the maximum voltage equal to that imposed by the capacitor fabrication process.

To understand the behaviour of the Dickson charge pump, let us first consider the ideal one-stage configuration shown in **Figure 3.12** which consists of a boosting capacitance ( $C$ ), two switches ( $S_1$  and  $S_2$ ) and a clock signal with an amplitude equal to the power supply  $V_{DD}$ . During the first half period ( $0$  to  $T/2$ ),  $S_1$  is closed and  $S_2$  is open, therefore,  $C$  will be connected to the power supply ( $V_{in}$ ) and is charged to  $V_{DD}$ . In the second half period ( $T/2$  to  $T$ ), the switches change their positions and the charge stored in  $C$  will be transferred to the capacitive load,  $C_L$ . Thus, the ideal output voltage is given by [79]

$$V_{out} = 2V_{DD} \frac{C}{C + C_L} \quad 3.4$$

The presence of the load capacitor ( $C_L$ ) will reduce the amount of the output voltage. If a load resistance ( $R_L$ ) is added to the output, a ripple voltage  $V_R$  will be generated at  $V_{OUT}$ , as we will see later.

**Figure title: Dickson charge pump.**



**Figure 3.12 Ideal one-stage of a Dickson charge pump.**

Based on the explanation of the ideal charge pump, the operation and analysis of the Dickson charge pump is illustrated in **Figure 3.13** [77, 80], which shows the typical waveforms of n-stage multiplier. The charge pump being illustrated is a practical implementation of the Dickson charge pump. The diodes are replaced by diode-connected MOS transistors. The problem with using diodes is that in most semiconductor processes, isolated diodes are not available. Therefore, diode-connected MOS transistors are used instead of diodes [78, 81].

As we can see in **Figure 3.13**,  $\phi$  and  $\phi_b$  are non-overlapping clocks with amplitude  $V_\phi$  and are coupled via capacitors. For optimum performance, the clocks have to be generated by a low impedance source. The voltage at subsequent nodes is increased by pumping charges during the first half of the clock cycle and then discharging during the next half of the clock cycle. The coupling capacitors along the chain of the diode-connected transistors build up the voltage potential at every successive stage of charge pump. The difference in the voltage potential of two successive nodes is given by [79]

$$\Delta V = V_{n+1} - V_n = V_\phi' - V_{th} \quad 33.5$$

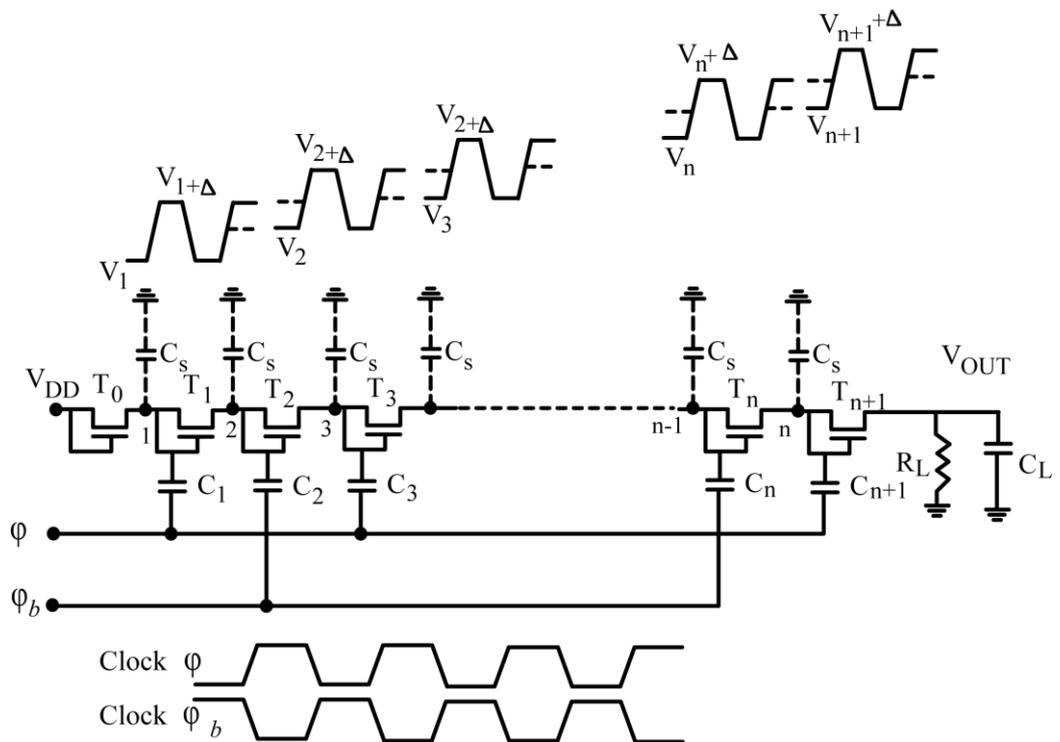
where,  $V_{th}$  is the threshold voltage of  $T_n$ ,  $V_\phi'$  is the voltage swing at each node due to the capacitive coupling from the clock which can be given [79]

$$V_{\phi'} = \left( \frac{C}{C + C_s} \right) V_{\phi} \quad 3.6$$

When the clock  $\phi$  is low, and assuming clock period is sufficient enough to fully charge the coupling capacitors, the first transistor  $T_0$  is on and therefore the Capacitor  $C_1$  is charged up until the voltage potential at node 1 is settled at  $V_{DD} - V_{th}$ . At the next cycle of the clock, when  $\phi$  changes its state to high, the voltage potential at node 1 will increase to [79]

$$V_1 = V_{DD} - (V_{\phi'} - V_{th}) \quad 3.7$$

**Figure title: Dickson charge pump operation**



**Figure 3.13 Internal waveforms of Dickson charge pump.**

During the time the clock is low, transistor  $T_1$  is off, and therefore the charge on  $C_1$  is transferred to  $C_2$  until the voltage potential at node two becomes [79]

$$V_2 = V_{DD} + (V_{\phi'} - V_{th}) - V_{th} \quad 3.8$$

After that, when the  $\phi$  becomes high, the  $C_2$  is charged up by  $V_{\phi}$ , and the voltage potential at node 2 is given by [79]

$$V_2' = V_{DD} + 2(V_{\phi'} - V_{th}) \quad 3.9$$

This operation continues for the N-stages. As the voltage rises at each stage, the maximum output voltage that the charge pump can achieve is limited by  $V_{DS}, V_{BS}$  of the transistor  $T_n$  and the dielectric breakdown voltage of the capacitor  $C_n$ . The value of these parameters varies according to the CMOS process used as we will see in next chapter. The final output voltage can be calculated as [79]

$$V_{out} = V_{DD} - V_{th} + n(V_{\phi'} - V_{th}) \quad 3.10$$

This equation is for calculating the output voltage in an ideal situation when the charge pump is not connected to output load. However, when the charge pump is connected to a load, an output current  $I_{out}$  is delivered by the pump and a voltage drop  $V_{drop}$  is developed at each stage due to this current and is given by [80, 82]

$$V_{drop} = \frac{I_{out}}{(C + C_S)f} \quad 3.11$$

where,  $f$  is the frequency of the clocks  $\phi$  and  $\phi_b$ . The previous equation implies that the output voltage for N stages can be reduced by [79]

$$V_{drop} = \frac{N \times I_{out}}{(C + C_S)f} \quad 3.12$$

The output voltage then can be rewritten as

$$V_{out} = V_{DD} - V_D + N \left( V_{\phi'} - V_{th} - \frac{I_{out}}{(C + C_S)f} \right) \quad 3.13$$

where  $V_{out}$  is the maximum DC voltage at the last node, n. Using the equation above, we can start designing a charge pump that can specifically deliver the required 72 V output voltage at 70  $\mu$ A current that are needed for biasing and operating the Multi-Pixel photon Counter (MPPC).

The output voltage at the last node, where a capacitive load ( $C_L$ ) is connected, tends to experience a ripple effect once a resistive load ( $R_L$ ) is connected to the output node. This happens each time transistor  $T_{n+1}$  is turned off when  $\phi_b$  is low, and allows  $R_L$  to discharge the load capacitor  $C_L$ . When  $\phi_b$  goes high,  $T_{n+1}$  is turned on and  $C_L$  will be charged up again. The continuation of this operation will give a rise to a very important aspect of the charge pump known as charge pump ripple. This is denote as  $V_R$  and can be represented as [79]

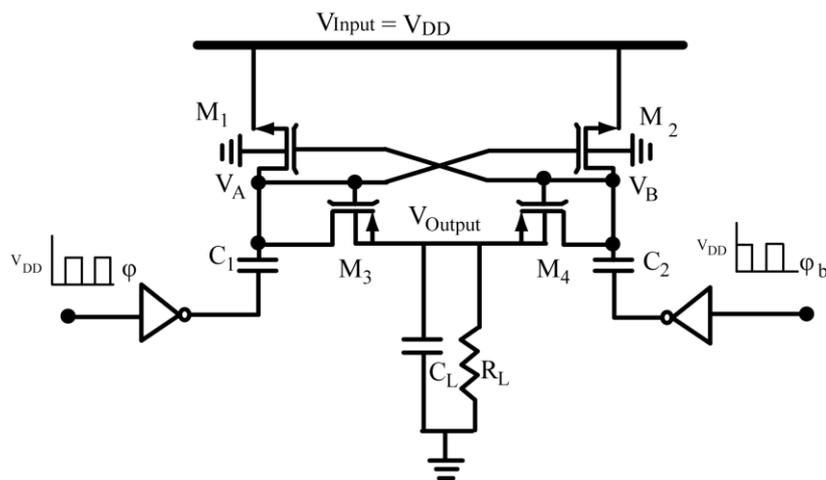
$$V_R = \frac{I_{out}}{f \times C_L} = \frac{V_{out}}{f \times R_L \times C_L} \quad 3.14$$

The ripple is generally considered as noise which affects the operation of the loading circuit e.g. operational amplifiers, voltage regulators, switched capacitor circuits, SRAMs, LCD drivers and of course, the MPPC as in our case. Therefore, the amplitude of  $V_R$  should be kept as small as possible. As can be seen from **equation 3.14**, the most straightforward way of keeping the ripple small is by increasing the clock frequency of the charge pump. Increasing the size of the capacitor also has a great impact on reducing the ripple. However, we should remember that the greater the load capacitor, the greater the drop voltage  $V_{drop}$  at the output. Increasing the frequency also has an effect on the efficiency of the pump as we will see later in this chapter. Therefore, with a good balance between the size of the load capacitor and the clock frequency one can achieve a reasonable ripple. After all, the effect of the ripple depends on how sensitive the loading circuit is to variation in its DC supply.

### 3.5.1.2 Voltage doubler

Another type of charge pumps is a crossed-coupled voltage doubler [83]. Shown in **Figure 3.14** is a schematic of a voltage doubler that is capable of producing  $2 V_{DD}$  at the output node. The basic operation of the charge pump depends on the non-overlapping  $V_{DD}$  peak to peak clocks  $\phi_b$  and  $\phi$ . The clocks charge the capacitors  $C_1$  and  $C_2$  successively to produce a shifted clock alternating between  $V_{DD}$  and  $2 V_{DD}$  at nodes A and B. The two outputs of the voltage doubler are then passed by the two PMOS transistor ( $M_3$  and  $M_4$ ), which are finally accumulated at the load capacitor  $C_L$  and generate a DC voltage equal to  $2 V_{DD}$ . Despite the fact that NMOS transistors provide higher carrier speed than that offered by the same size PMOS transistors, the PMOS transistors are used mainly to avoid the  $V_{th}$  drop at each gate of the NMOS transistors [84].

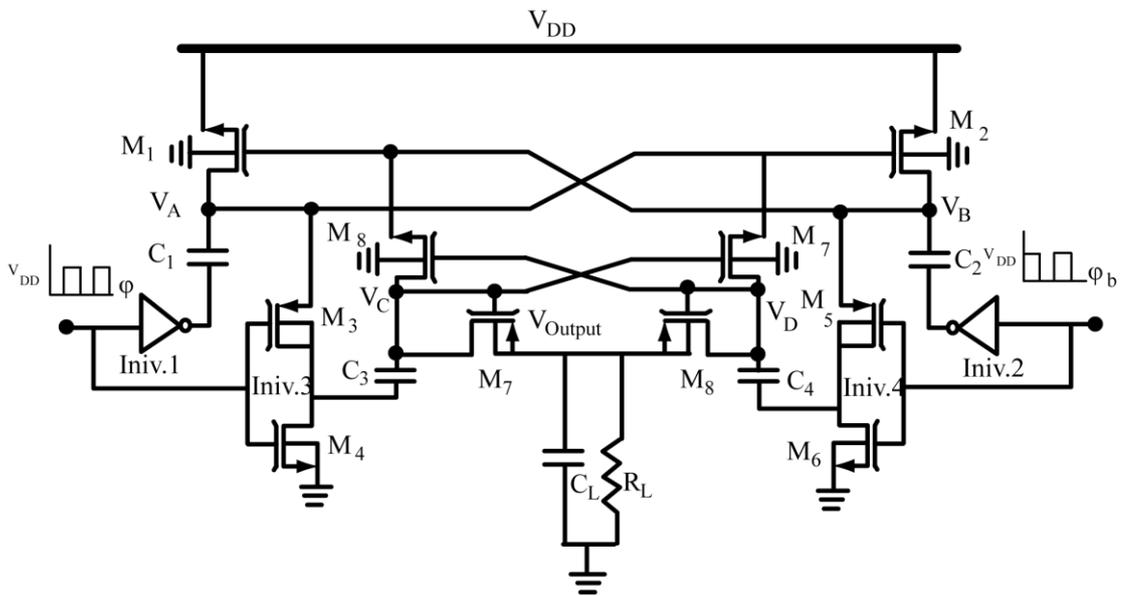
**Figure title: Voltage doubler**



**Figure 3.14 Conventional configuration of a voltage doubler.**

In order to double the generated voltage by the voltage doubler, another voltage doubler is cascaded by directly connecting the output voltage of the first doubler to the input voltage of the second doubler. However, a different way of cascading the voltage doublers can be used to reduced the number of used components as shown in **Figure 3.15** [85]. In this configuration the second voltage doubler inputs are connected to nodes  $V_A$  and  $V_B$  of

**Figure title: Two voltage doublers**



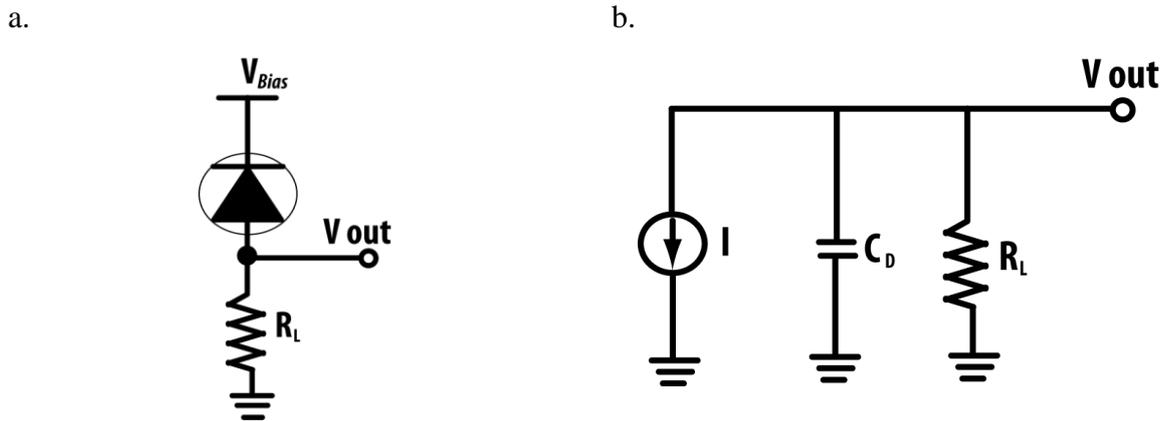
**Figure 3.15 Area efficient dual voltage doubler.**

the first doubler. The capacitors of the second voltage doubler ( $C_3$  and  $C_4$ ) are charged by clocks alternating between 0 and  $2 V_{DD}$  from inv.3 and inv.4 and the  $2 V_{DD}$  clocks that are passed by  $M_7$  and  $M_8$ . This generates voltages at node  $V_C$  and  $V_D$  that alternate between  $2 V_{DD}$  and  $4 V_{DD}$  which are then passed to the load capacitance  $C_L$  to generate a DC voltage equal to  $4 V_{DD}$ .

### 3.5.2 Transimpedance amplifier (TIA) : a review

In systems where photon sensing is taking place, the generated current from light detectors such as photodiodes and APD are generally small and most of the subsequent processing occurs in the voltage domain, thus it needs to be converted into voltage. MPPC as all other single-photon avalanche diodes (SPAD's) can operate in two modes: voltage-mode where voltage signals can be directly read out of the device, and as any photodetector device the MPPC can be operated in current mode where current signals needed to be converted to

**Figure title: Current to voltage converter**



**Figure 3.16 a. Simple resistive optical front-end for a photodetector device b. equivalent circuit of configuration in a.**

voltage signals. A disadvantage of the voltage mode output is that the timing performance is not fully exploited [58]. So, operating the SPAD in current-mode is preferred, especially if their avalanche current is very small such as the case of the MPPC. However, some SPADs do not require current to voltage conversion and can be operated directly in voltage mode where the timing performance is still preserved. These SPADs are usually biased with very high biasing voltage as high as 400 V and with excess voltage more than 20 V can produce a significant avalanche current that can reach up to 100 mA [86]. For the MPPC it is recommended by the manufacturer to operate it in current mode. Operating in current mode requires a current to voltage converter, or as known as a Transimpedance amplifier (TIA) that is capable of converting and amplifying the avalanche current signals generated by the MPPC. The TIA should be capable of capturing and amplifying the 10 MHz signal produced by the MPPC and produce a significantly large signal that can be processed afterwards.

TIA's are widely used as a sensor interface unit in the front-end of many optical systems that require current sensing at the input and a useful voltage at the output. The simplest optical front end that can convert current to voltage can be achieved by a using a simple resistor which is connected to the anode of the photodetector, as shown in **Figure 3.16.a**. This circuit configuration has a Transimpedance gain equal to  $R_L$ , and has a time constant equal to

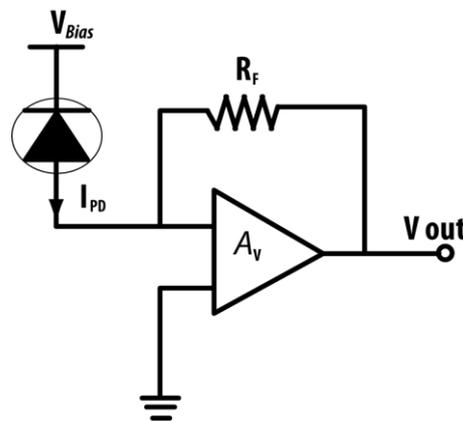
$$\tau = R_L \times C_d \quad 3.15$$

where,  $R_L$  is the resistance of the resistor connected and  $C_d$  is the terminal capacitance of the light detector. The small signal equivalent circuit of this configuration is depicted in **Figure 3.16.b**. The value of  $\tau$  is proportional to the bandwidth of the I-V convertor which is given by

$$f_{-3db} = \frac{1}{2\pi \times R_L \times C_d} \quad 3.16$$

Having the terminal capacitor of the light detector fixed, the bandwidth of the TIA is therefore a trade-off with the gain of the TIA. In the case of the MPPC, where the terminal capacitance is equal to 37 pF, in order to achieve a gain of 2 k $\Omega$ , the bandwidth of the TIA will be restricted to 2.15 kHz which is clearly not sufficient to capture the 10 MHz pulses generated by the MPPC [67].

**Figure title: Amplifier-based TIA**



**Figure 3.17 Schematic of an amplifier-based TIA.**

Due to the incapability of the simple resistor I-V convertor to achieve higher bandwidth and high gain at the same time, the TIA is chosen to be used instead. Most of TIAs can be categorised into two main categories; a voltage amplifier-based TIA and a common gate input TIA. The voltage amplifier-based TIA shown in **Figure 3.17** has been developed to relax the trade off relation between the gain and the band width that strongly exists when

using a simple resistor to convert the current to voltage. The use of an amplifier with a feedback resistor introduces the amplifier gain-bandwidth product (GBW) to the bandwidth equation, which can be given by[87]

$$f_{-3db} = \sqrt{\frac{GBW}{2\pi \times R_F \times C_D}} \quad 3.17$$

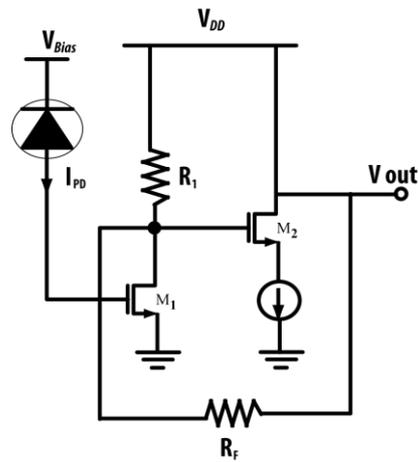
In addition to expanding the bandwidth, when integrated with digital processors, the amplifier-based TIA provides great immunity from power supply noise, substrate bounce and substrate coupling from adjacent digital circuitries [87].

Alongside the challenges in having to achieve a wide bandwidth; designing a TIA involves challenges such as achieving high gain, wide input dynamic range and low noise. These factors are a trade off with the bandwidth of the TIA. Managing a high gain, low noise and high input dynamic range is always at the expense of the bandwidth of the TIA. This relation is clearly presented especially in CMOS technology which is inherently slower in speed and higher in noise when compared with other technologies such as GaAs, InP-based (Heterojunction Bipolar Transistors) HBT and High Electron Mobility Transistor (HEMT) [88, 89]. Designing a TIA for optical devices that have a large terminal capacitance can be especially difficult due to the effect of the capacitance on the bandwidth such as the 37 pF terminal capacitance of the MPPC. The terminal capacitance of devices optical devices can vary from one device to another and therefore the maximum Transimpedance gain and bandwidth will vary as well. **Table 3.2** summarises a list of some recent work in literature, along with their terminal  $C_t$ , bandwidth and gain. It is seen that how the terminal capacitance of the optical devices affects the bandwidth of the TIA.

**Table 3.2 TIAs fabricated in different CMOS technologies**

Parameter	[90]	[91]	[92]	[93]
Bandwidth	30.5 GHz	7 GHz	9 GHz	860 MHz
Gain	51 dBΩ	55 dBΩ	54 dBΩ	58 dBΩ
Optical device terminal capacitance	50 fF	0.2pF	0.5pF	1pF
CMOS Technology	0.18-μm	0.18-μm	0.18-μm BiCMOS	0.6-μm

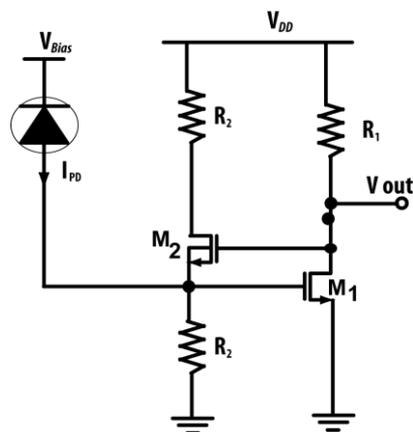
**Figure title: Common-gate TIA**



**Figure 3.18 Configuration of a common-gate TIA.**

This problem can be solved or at least eased by further more expanding the bandwidth of the TIA, this is achieved by using the common gate input TIA shown in **Figure 3.18**. This type of TIA is designed to decouple the light detector terminal capacitance from the feedback resistor, and therefore decrease the influence of the terminal capacitance on the bandwidth of the TIA [87]. This concept is improved and expanded by using a regulated cascade (RGC) TIA which is an improved version of a common-gate configuration, with active feedback instead of passive feedback. This active feedback provides a lower input impedance than the simple common-gate TIA does [91].

**Figure title: RGC TIA**



**Figure 3.19 Regulated cascade (RGC) TIA.**

In this work we propose a low impedance-high gain TIA which is developed based on the conventional RGC. It is capable of accommodating the 37 pF large capacitance of a MPPC while maintaining a relatively wide bandwidth and high gain at the same time. The RGC TIA configuration, shown in **Figure 3.19** has been used in some TIAs design [91, 93, 94] and is used as a backbone for our TIA design that will be discussed in **Chapter 5**. The RGC configuration enhances the effectiveness of the small Transconductance  $g_m$  of the MOS transistor which, results in reducing the input impedance that can make the amplifier at the input node sit at virtual ground. This relation between the impedance and the  $g_m$  helps in relatively isolating the influence of the terminal capacitance of the MPPC from degrading the TIA bandwidth [87].

### **3.6 Summary**

This chapter has reviewed the design of existing diagnostic pills. A pill smaller than 50 mm in length and 16 mm in diameter is estimated to host the wireless sensor system that is capable of detecting autofluorescence emission variations. A key component of this pill is an ultra sensitive light detector. Based on a comparison of existing sensitive light detectors that are capable of detecting autofluorescence emission, the MPPC device was chosen to be incorporated into the pill. The MPPC has a high photon detection efficiency, ~60% at 520 nm, which makes it suitable to detect the autofluorescence emission spectra (500-700 nm). The other main components of the pill were determined based on the MPPC requirements for operation. The MPPC device requires a very high voltage generator that can produce more than 72 V and deliver more than 70  $\mu$ A. Based on a review of existing voltage converters, a Dickson charge pump voltage converter was chosen to convert the 3 V (DC) which is supplied by two SR44 (1.55 V, 165 mAh) to more than 72 V. The other component that is required to operate the MPPC is a TIA that is capable of capturing the 1 $\mu$ A peak-peak, 10 MHz pulses generated by the MPPC. The charge pump and the TIA are to be integrated in the same AISC. In order for the pill to operate for 9 hours, which is the time required for the pill to traverse the small intestine, the maximum power consumption of the entire capsule has to be less than 28.4 mW. A literature review of the charge pump and the TIA was presented as an introduction to the design and implantation which is to be discussed in chapter 4 and 5.

# Chapter 4 Charge pump

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## **4.1 Introduction**

Based on the literature review of the existing charge pump topologies that was presented in the previous chapter, the design of a very high voltage charge pump that can generate more than 72 V is discussed. This chapter begins with a section that contains: 1) the design the Dickson part of the charge pump, 2) the design of the high voltage clock generator part of the charge pump and 3) the design of the final charge pump which consists of 5-cell where each cell is a combination of a Dickson charge pump and a high voltage clock generator. This is followed by detailed evaluation measurements of the charge pump part of the ASIC.

## **4.2 Designing a charge pump in AMS H35 process**

The first step towards designing a charge pump is to determine the technology that will be used. Since the first integration of the Dickson charge pump into a chip, CMOS technology has been the technology of choice for many designers. Depending on the targeted output voltage, designers will choose between standard CMOS technology [78, 82, 95] or High voltage CMOS technology [73]. Advanced technologies may have a capability greater than that of some commercially available technologies. However, choosing the most advanced technology is not always the best solution as the final product can be very costly to produce. In our case, we are interested in a commercially available CMOS technology that can handle and produce the desired very high voltage that is needed to bias the MPPC. For some considerations, that we will explain later in this chapter, the high voltage process AMS H35 provided by Austriamicrosystems has been chosen for designing the ASIC. Moreover, by using this technology, integrating the low voltage front end and the high voltage charge pump is possible.

According to the data sheet provided by Hamamatsu Co. the MPPC is best biased at 72 V for operation at 37 °C ambient temperature - which is the typical body temperature in which the capsule will be working. Using **equation 4.7**, and by assuming the ideal case where  $V_{\phi'}$  is equal to  $V_{\phi}$  and  $V_{th}$  is neglected, the number of charge pump stages can be estimated. Thus, if we assume that the peak voltage swing of the clock is equal to 3 V, we need a charge pump that consists of 23 stages.

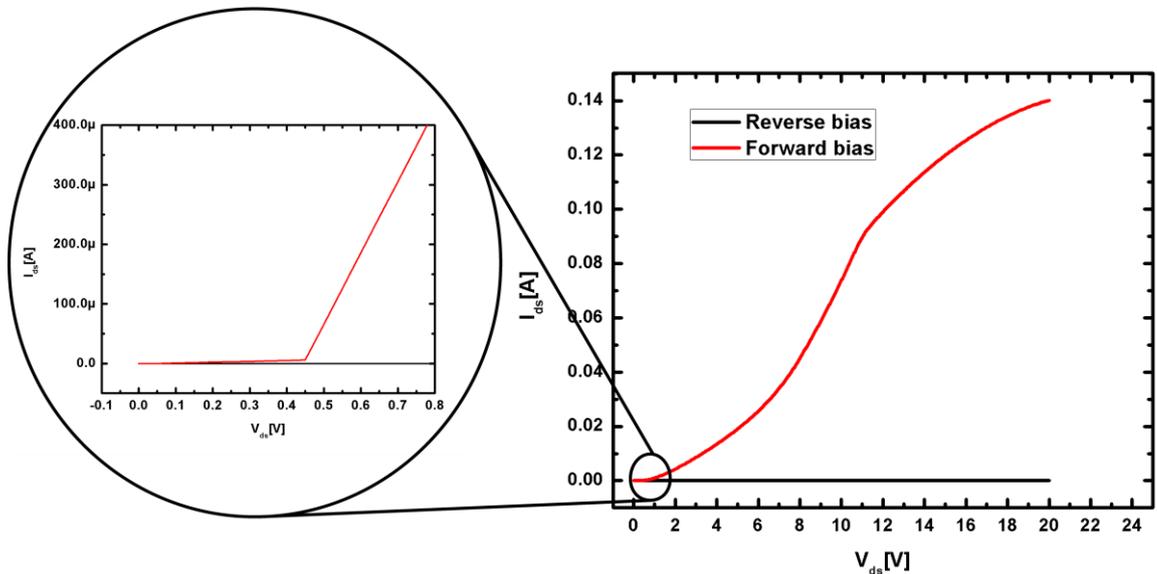
Implementing these stages by using NMOS transistors in a standard CMOS technology encounters two main obstacles. The first one is the restriction on the maximum operating voltages of the transistors. In particular, the bulk source voltage  $V_{BS}$  increases with each stage of the charge pump. This places a limit on the number of stages and the operating points which are possible. The second obstacle is the maximum voltage the capacitors, in the particular CMOS technology used, can safely have applied across their plates [78]. Consequently, there is a limit on the voltage that can be generated using the standard Dickson topology with the standard CMOS technology. However, this limitation can be overcome by extending the breakdown limits beyond the standard values by means of a transistor stacking technique as described in [96] or by using extend-Drain NMOS as in [97] that extends the breakdown voltage limits by placing the N-type source/drain (NSD) implants inside larger N-well geometries. The N-well diffuses outward to produce a very lightly doped drain capable of withstanding high voltages.

Another way to overcome the limitation of the breakdown voltage between the bulk and the source is by using diode connected PMOS transistors. In this way the bulk is connected to the source, and therefore the voltage potential between the two terminals is always zero [85]. The isolation provided by the n-well of the PMOS transistor confines the voltage bias that develops at the bulk terminal to the n-well of the PMOS, However, PMOS transistors are not a good choice to be used for charge transfer tasks. PMOS transistors make use of holes instead of electrons as the majority carriers. PMOS transistors are inherently slower because they rely on holes which have two to three times lower mobility than electrons [98]. Hence designers focus their efforts on designing charge pumps with diodes or diode-connected NMOS transistors [73, 99, 100]. However, these solutions can only extend the breakdown limitations by a few extra volts. Another solution that has been adopted in this work to overcome the  $V_{BS}$  breakdown limitations is using the triple well CMOS process [100, 101]. The great advantage of the latter solution is to tie the bulk to

the source and thus set  $V_{BS}$  always to zero while other breakdown limitations can be extended up to 400 V in some CMOS processes [102].

The high voltage H35 process provided by AMS is one of these multi-well technologies. Therefore, it was chosen to design the ASIC that includes the charge pump. It has in its library a variety of isolated NMOS transistors that are suitable for our purpose. An NMOSIT20 (Isolated HV (20 V) Thin-oxide N-channel MOS ) has been chosen to be used as a diode-connected transistor. This transistor can withstand a potential voltage of up to 22 V between the source and the drain. This will allow to use a very high voltage clocks and therefore increases the efficiency of the charge pump as we will see later in this chapter. The high voltage transistors in high voltage CMOS technologies are obtained by creating a diffused p-type channel in a low-doped n-type drain region. An example of such a transistor is the NMOSIT20. The source of the NMOSIT20 is implanted in RPWELL (shallow PWELL + deep PWELL) which is diffused in a low doped deep NWELL. The low doping in the drain side results in a large depletion region with a high breakdown voltage [96].

**Figure title: NMOSI20 diode characteristics**



**Figure 4.1 I-V Characteristics of the internal diode of the NMOSIT20.**

The NMOSIT20 transistor is configured in a different way to that of the normal transistor to create a diode-connected transistor. In low voltage NMOS transistors, the gate is connected to the drain of the transistor to make a diode-connected configuration. However,

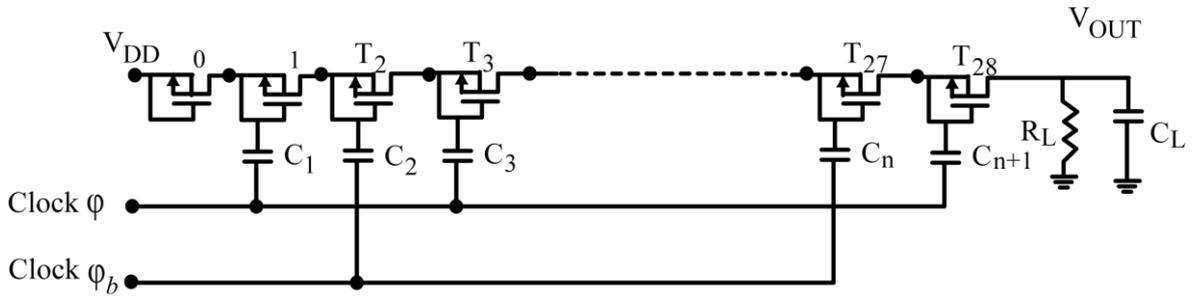
in the high voltage case, where the transistors are more bi-directional, the gate of the NMOSIT20 is connected to the source of the transistor and the source is connected to the bulk. This configuration has three advantages over the conventional configuration:

- Connecting the source to the gate overcomes the  $V_{G-SB}$  breakdown limit imposed by the technology - typically 3.6 V.
- This configuration increases the current driveability of the charge pump when compared with low voltage diode-connected transistors-especially at high voltage biasing. The I-V characteristic of the diode-connected transistor when forward biased is shown in **Figure 4.1**. The diode thus formed is able to transfer very high current  $> 100$  mA at 20 V bias. This diode like characteristic is attributed to the P-N junction developed between the shallow p-well of the transistor and the deep- n-well.
- Connecting the source to the body eliminates the impact of the body effect on the Dickson charge pump. The threshold voltage of the diode-connected NMOS transistor is increased proportionally as the voltage developed between the source and the bulk increases at each stage. The threshold voltage of a NMOS transistor is represented as

$$V_{th} = V_{th0} + \gamma \left( \sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s} \right) \quad 4.1$$

Where  $\phi_s$  is the surface potential at the threshold,  $\gamma$  is the body effect coefficient and  $V_{th0}$  is the zero-bias threshold voltage. When the body and the source terminals of the NMOS transistors are connected, the threshold voltage  $V_{th}$  is kept constant at  $V_{th0}$  (see **equation 4.1**). On the other hand, if the bulk is connected to ground as is the case with single well CMOS processes, the value of the threshold voltage will grow as  $V_{BS}$  grows which consequently increases the Body effect of the transistor and can seriously diminish the charge pump performance [80].

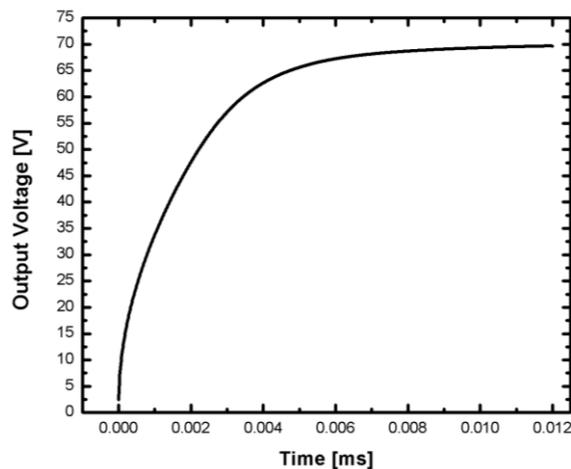
**Figure title: Dickson charge pump**



**Figure 4.2 Implementation of Dickson charge pump using NMOSI20.**

The final implementation of the Dickson charge pump is shown in **Figure 4.2**. Based on the technology that has been chosen for implantation in this project and the transistor to be used as diode is known, **equation 3.10** can be used to estimate the practical number of stages needed to produce the required 72 V can be estimated more accurately. From **Figure 4.2**, it can be found that the diode voltage  $V_D$  is 0.46 V. Thus, the degradation of the transferred voltage caused by  $V_D$  at each stage results in an overall loss of 10.6 V. The loss caused diode-connected NMOSI20 will henceforth be referred to as  $V_D$  instead of  $V_{th}$  and the device will be referred to as diode. This can be related to the fact that we are actually using the internal diode that is formed between the shallow p-well of NMOSIT20 and the deep- n-well when the device is configured as mentioned previously.

**Figure title: Dickson charge pump**



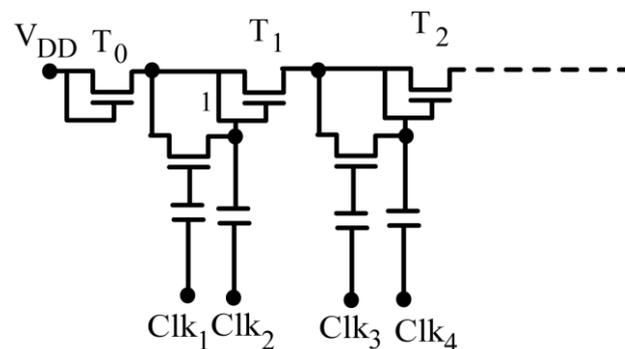
**Figure 4.3 Simulated results of a 28 –stage Dickson charge pump.**

Furthermore, another source of loss in the amount of transferred voltage at each stage is caused by the stray capacitors  $C_s$ . Unlike the loss caused by  $V_D$ , this loss is difficult to estimate as the stray capacitors and their value varies depending on whether the coupling capacitors are integrated or off-chip [77]. Therefore, in order to obtain a rough estimate of the number of stages needed to generate the 72 V, the loss caused by  $C_s$  will be neglected for the time being. In order to compensate for 10.6 V loss, 5 extra stages are added and the total number of stages is raised to 28.

The charge pump shown in **Figure 4.2** was implemented using 28-stages and then simulated using the Spectre tool provided by Cadence. The Spectre tool runs the AMS 72.0 Hit-kit provided by Austriamicrosystems. This Hit-kit is the high voltage Hit-Kit that contains the BSIM4 model of the NMOSIT20. Using this advanced model of the NMOSIT20 device enables accurate simulations of the expected performance of the charge pump circuit. Furthermore, this hit-Kit has a very important feature known as Safe Operation Area Check (SOAC). This feature helps the designer to make sure that that he/she is operating the high voltage devices in the safe operation. If the safe operating area is exceeded, warning messages are given.

The simulated output voltage is shown in **Figure 4.3**. With no resistive load, the charge pump produces 69.6 V - which is close to the target value. The 2.4 V loss is mainly attributed to the parasitic resistance and capacitance in each transistor as defined by the BSIM4 model of the NMOSIT20 transistor which is provided by Austriamicrosystems (AMS).

**Figure title: Improved charge pump**



**Figure 4.4 Charge pump with four-phase clock scheme.**

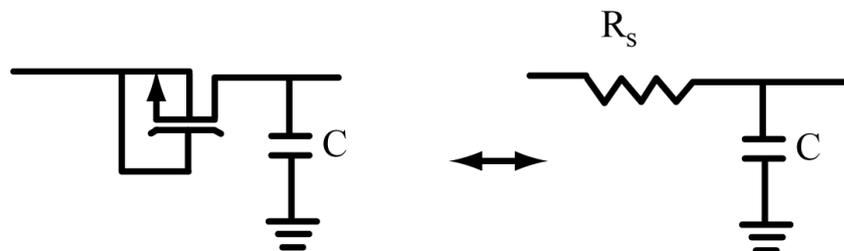
The degradation caused by  $V_D$  at each stage can be avoided using a common technique called four-phase clocking. In this technique a four-phase clock is used to cancel the  $V_D$  effect and therefore allow full transfer of charge between stages. This can be achieved by introducing additional bootstrapping circuits on the gate of the diode connected transistor and clocking the whole circuit using a four clocking scheme instead of two as shown in **Figure 4.4** [103]. However, adding extra circuitry to the design means additional routing area for new clocks and the new transistors which can result in doubling the size of the charge pump. This technique is more effective for low voltage charge pumps.

The  $V_D$  degradation problem can be overcome efficiently by reducing the stages needed to produce the 72 V. This solution is based on the concept of using a very high amplitude clock signal design. By increasing the amplitude of the clock, the number of stages required will decrease dramatically. More importantly, increasing the clock amplitude increases the efficiency of the charge pump.

#### 4.2.1 Dickson charge pump power efficiency

The power efficiency of a charge pump is one of the important characteristics of the charge pump that should be taken into consideration when designing and implementing a charge pump. For efficiency purposes, the Dickson circuit can be modelled by the simple equivalent circuit shown in **Figure 4.5**. In addition to the losses caused by the diode voltage  $V_D$  and the presence of the stray capacitors, the power efficiency of the charge pump is also affected by the losses of the output series resistance of the charge pump  $R_s$ .

**Figure title: Charge pump model**



**Figure 4.5** Equivalent representation of a single pump stage.

This loss can be calculated from **equation 3.12** by dividing the drop voltage  $V_{drop}$  at one stage by the output current delivered to  $R_L$ .

$$R_s = \frac{V_{drop}}{I_{out}} = \frac{1}{(C + C_s) \times f} \quad 4.2$$

Another source of loss which also appears when current is delivered to the load is attributed to the equivalent resistance of the diode. By adding this resistance to **equation 4.2**, the series resistance,  $R_s$  becomes

$$R_s = \left( \frac{1}{(C + C_s) \times f} + R_{eq} \right) \quad 4.3$$

Where,  $R_{eq}$  is the resistance between the source and the drain of the diode. A single stage of the charge pump can be represented as  $R_s$  connected with the boosting capacitor as illustrated in **Figure 4.5**. From the simulated I-V curve (**Figure 4.1**), the  $R_{eq}$  that represents the internal diode of the NMOSIT20 can be given by

$$R_{eq} = \frac{V_{DS}}{I_{DS}} \quad 4.4$$

For N stages,  $R_s$  becomes

$$R_s = N \left( \frac{1}{(C + C_s) \times f} + \frac{V_{DS}}{I_{DS}} \right) \quad 4.5$$

By modifying **equation 3.13** to add the extra loss which was introduced by  $R_{eq}$  to  $R_s$ , the total output voltage is given by

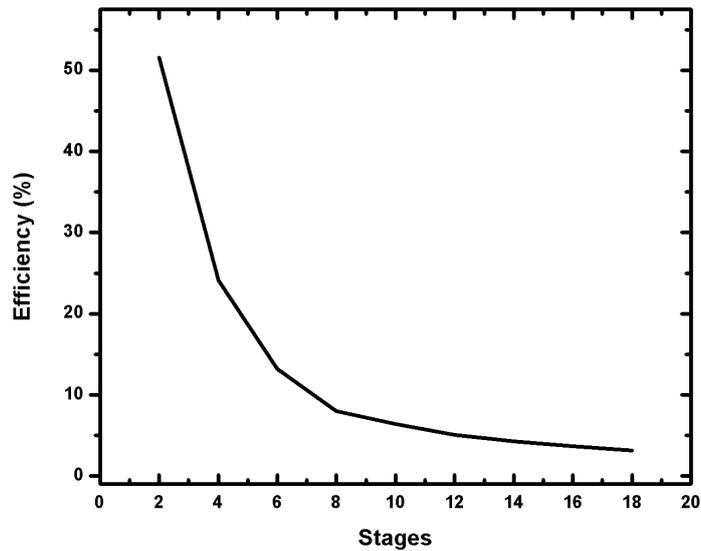
$$V_{out} = V_{DD} - V_D + N \left( V_{\phi} - V_D - \frac{I_{out}}{(C + C_s) \times f} - I_{out} \times R_{eq} \right) \quad 4.6$$

The presence of  $R_s$  at each stage affects dramatically the efficiency performance of the Dickson charge pump. The greater the number of stages used, the greater the charge pump efficiency is degraded. This power efficiency can be calculated as [84, 104]

$$Efficiency = \left( \frac{P_{out}}{P_{in}} \right) \times 100\% = \left( \frac{\overline{V_{out}} \cdot \overline{I_o}}{\overline{V_{DD}} \cdot \overline{I_{in}}} \right) \times 100\% \quad 4.7$$

Where,  $\overline{V_{out}}$ ,  $\overline{I_o}$ ,  $\overline{V_{DD}}$ ,  $\overline{I_{in}}$ , are the mean values of  $V_{out}$ ,  $I_o$ ,  $V_{DD}$ ,  $I_{in}$ . The equation above has been used to calculate the efficiencies of the charge pump shown in **Figure 4.2** for different numbers of stages. **Figure 4.6** shows the results of simulations of power efficiency of the Dickson charge pump versus the number of the pumping stages and shows clearly that the power efficiency drops in proportion to the number of stages.

**Figure title: Power efficiency**



**Figure 4.6 Simulated Power efficiency of Dickson charge pump decreases proportionally as the number of pumping stages increases.**

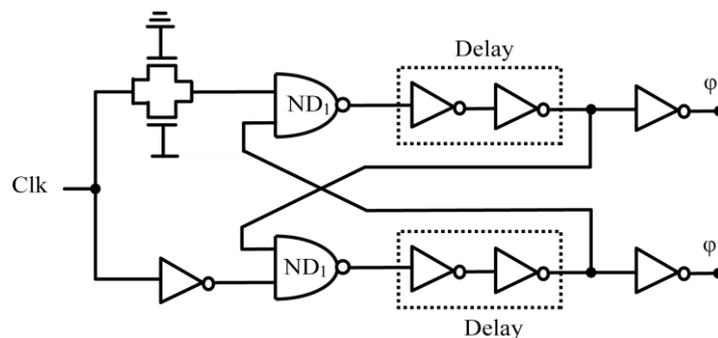
By inspecting **equation 4.3**, we can see that three parameters can be used to reduce the value of  $R_s$  and, consequently, improve the efficiency of the charge pump. The first parameter is the boosting capacitor  $C$ . the larger the capacitor the smaller is the value of  $R_s$ . This is also true for the stray capacitor. Ironically, according to **equation 4.3** the larger the value of the stray capacitor, the more it contributes in improving the charge pump

efficiency. Nevertheless, it has the opposite effect with the amplitude of the clock signals as in **equation 3.6**. Therefore, it is always recommended the stray capacitances are kept as low as possible. The second parameter is clock frequency. As the clock frequency is increased, the series resistance,  $R_s$ , decreases. Another very important parameter, as discussed in the previous section, is the clock amplitude. Increasing the amplitude of the clocking signals  $\phi$  and  $\phi_b$  reduces the value  $R_{eq}$  of the diode.  $R_{eq}$  is inversely proportional to the value of  $V_{DS}$  as in **equation 4.4**. In addition to decreasing the value of  $R_s$ , increasing the amplitude of the clocking signals will result in an overall reduction in the number of pumping stages needed to generate the targeted high voltage which consequently yields a lower overall equivalent charge pump series resistance. Furthermore, a lesser number of stages yield a lower overall voltage drop.

#### 4.2.2 High Voltage non-overlapping voltage generator

For optimum functioning, the charge pump requires a non-overlapping clock generator. For the two phases Dickson charge pump shown in **Figure 4.2** two clocks generator is commonly used which is able to generate the two clocks from single clock input. In this type, one clock is used as a clock source and its inversion is used as another clock source. The non-overlapping clock generator is shown in **Figure 4.7**. The operation of this circuit is based on the fact that the falling edge of the input clock passes immediately through the NAND gate  $ND_1$ . In contrast, the inverted clock in the other branch has to first pass through a passive delay element to the other NAND gate,  $ND_2$ , and then to the delay elements. The passive delay element, consisting of a NMOS and PMOS transistor, is used to compensate for the delay that is caused by  $INV_1$ , so that symmetric clocks are provided to  $ND_1$  and  $ND_2$ . The other delay elements consist of an even number of inverters.

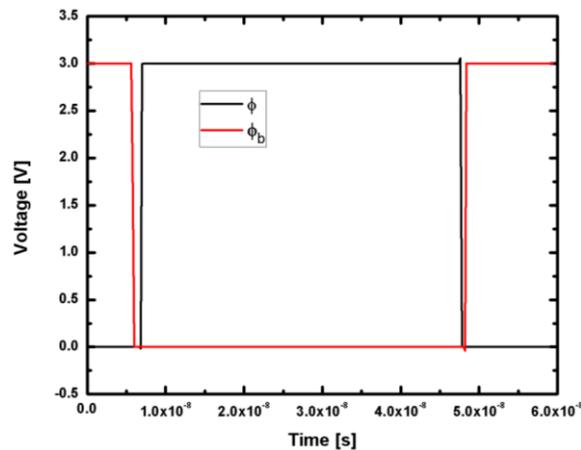
**Figure title: Clock generator**



**Figure 4.7 Single-clocked clock generator.**

It is essential for the clocks which operate the charge pump to non-overlap, so the charge transfer of the clock is even at each stage. Overlapping clocks will result in a truncated charge transfer in one stage and a longer period of transfer in the next one. This affects dramatically the charge pump efficiency - especially if clock time periods are short. The operation of this circuit has been simulated and the generated non-overlapping clocks are shown in **Figure 4.8**.

**Figure title: Non-overlapping clock**

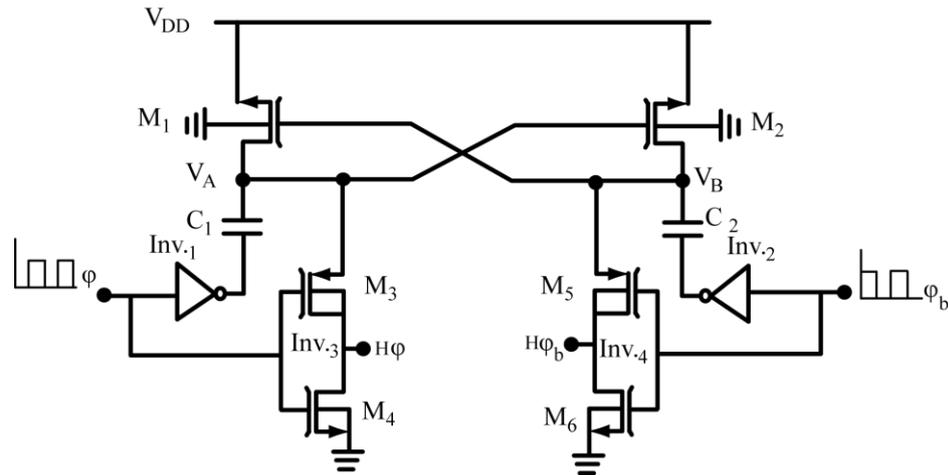


**Figure 4.8 Simulated non-overlapping clocks.**

In order to increase the amplitude of the non-overlapping clock produced by the clock generator, a clock booster is required. The voltage doubler proposed by [83] has been used for this purpose. As shown in **Figure 4.9**, a high voltage clock generator is based on a voltage doubler. This circuit consists of two cross-connected NMOS transistors. The use of NMOS transistors has two desirable features: the first is the higher carrier speed and the second advantage is that the NMOS transistors provide an automatic reverse bias of the junctions [84]. Since the low voltage NMOS transistor can not be used due to its low  $V_{DS}$  breakdown voltage, a high voltage transistor with high  $V_{DS}$  break down voltage is used. Unfortunately, the NOMOSIT20 lacks the feature of the automatic reverse bias of the junctions that exists in normal voltage NMOS transistors. This means that the source and the drain of the transistor are not interchangeable. This feature is essential for cross connecting transistors to act like switches. Therefore, in order to overcome this obstacle a symmetrical high voltage transistor available in the AMS library NMOS20HS (HV (20V)

symmetrical Thick-oxide n-channel MOS) is used instead. However, it is important to note that the one-sided device has a significant size advantage over the symmetrical transistors [105]. The NMOS20HS demonstrates a symmetrical structure which gives it an advantage over the NMOSIT20 when it comes to using it as a switch.

**Figure title: High voltage clock generator**



**Figure 4.9 High voltage clock generator based on a voltage doubler [85].**

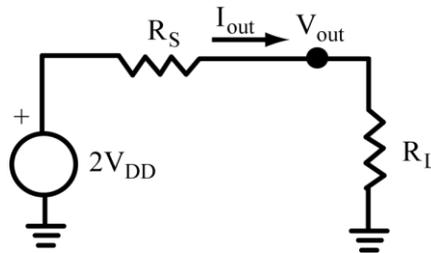
The basic operation of the charge pump depends on the non-overlapping 3 V peak to peak clocks  $\phi$  and  $\phi_b$  generated by the clock generator shown in **Figure 4.7**. The clocks  $\phi$  and  $\phi_b$  charge the capacitors  $C_1$  and  $C_2$  successively to produce a shifted clock alternating between 3 and 6 V at nodes  $V_A$  and  $V_B$ . The two outputs of the voltage doubler are then connected as the power supply to inverters 1 and 2 in order to create a boosted clock that swings between 0 V and 6 V.

The efficiency of the voltage doubler is mainly limited by the losses caused by the series resistance which develops at the sources of transistors  $M_1$  and  $M_2$  when current is delivered to the resistive load  $R_L$ . From an efficiency perspective, the voltage doubler can be modelled as in **Figure 4.10**. Here, the effective series resistance of the voltage doubler, which will be denoted as  $R'_s$  in order to be distinguished from  $R_s$  of the Dickson charge pump, can be given by

$$R'_s = \left( \frac{1}{2 \times (C + C_s) \times f} \right)$$

Where  $C = C_1 = C_2$  and The factor of 2 comes from adding the two capacitors in parallel. In the case when the boosting capacitors are integrated, the stray capacitor,  $C_s$ , is the total of the capacitance  $C_{TP}$  that develops between the top plate of the boosting capacitor and the substrate in parallel with the capacitance  $C_{BP}$  that develops between the bottom plate of the boosting capacitor and the ground. In the case of using external boosting capacitors,  $C_s$  is equal to output driver capacitance plus pads and board wiring parasitic capacitance.

**Figure title: Voltage doubler model**



**Figure 4.10 Voltage doubler equivalent circuit.**

The ON resistance that appears when the transistor is ON also contributes to the losses that can degrade the performance of the voltage doubler. The ON resistance is added to the series resistance thus

$$R'_s = \left( \frac{1}{2 \times (C + C_s) \times f} + 2 \times R_{on} \right) \quad 4.9$$

Where  $R_{on}$  is the resistance that appears between the drain and the source of the transistor when operating as a switch and is given by

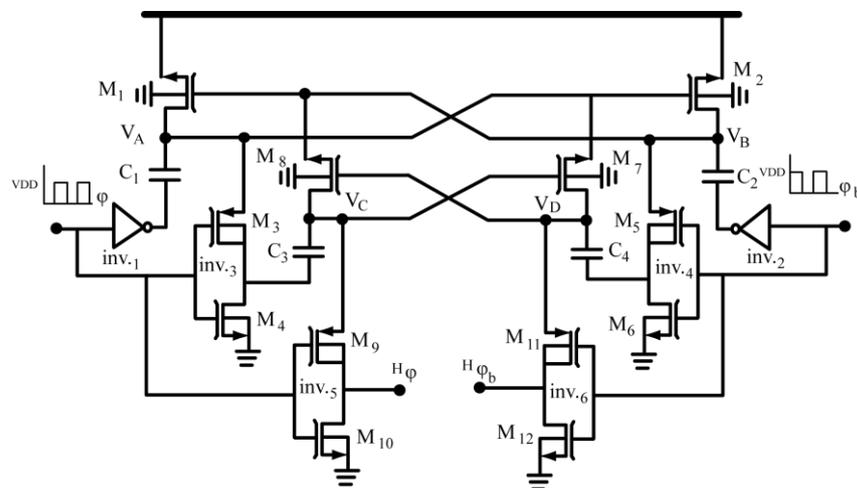
$$R_{on} = \left( \frac{1}{\mu_n \times C_{ox} \times \frac{W}{L} (V_{GS} + V_{TH})} \right) \quad 4.10$$

Where  $\mu_n$  is the charge-carrier effective mobility,  $W$  is the gate width,  $L$  is the gate length and  $C_{ox}$  is the gate oxide capacitance per unit area. By neglecting the effect of the high voltage inverters (inv. 3) and (inv. 4) in **Figure 4.9** which have insignificant drain capacitances, the output voltages at nodes  $H_\phi$  and  $H_{\phi b}$  according to the equivalent circuit in **Figure 4.10**, is given by

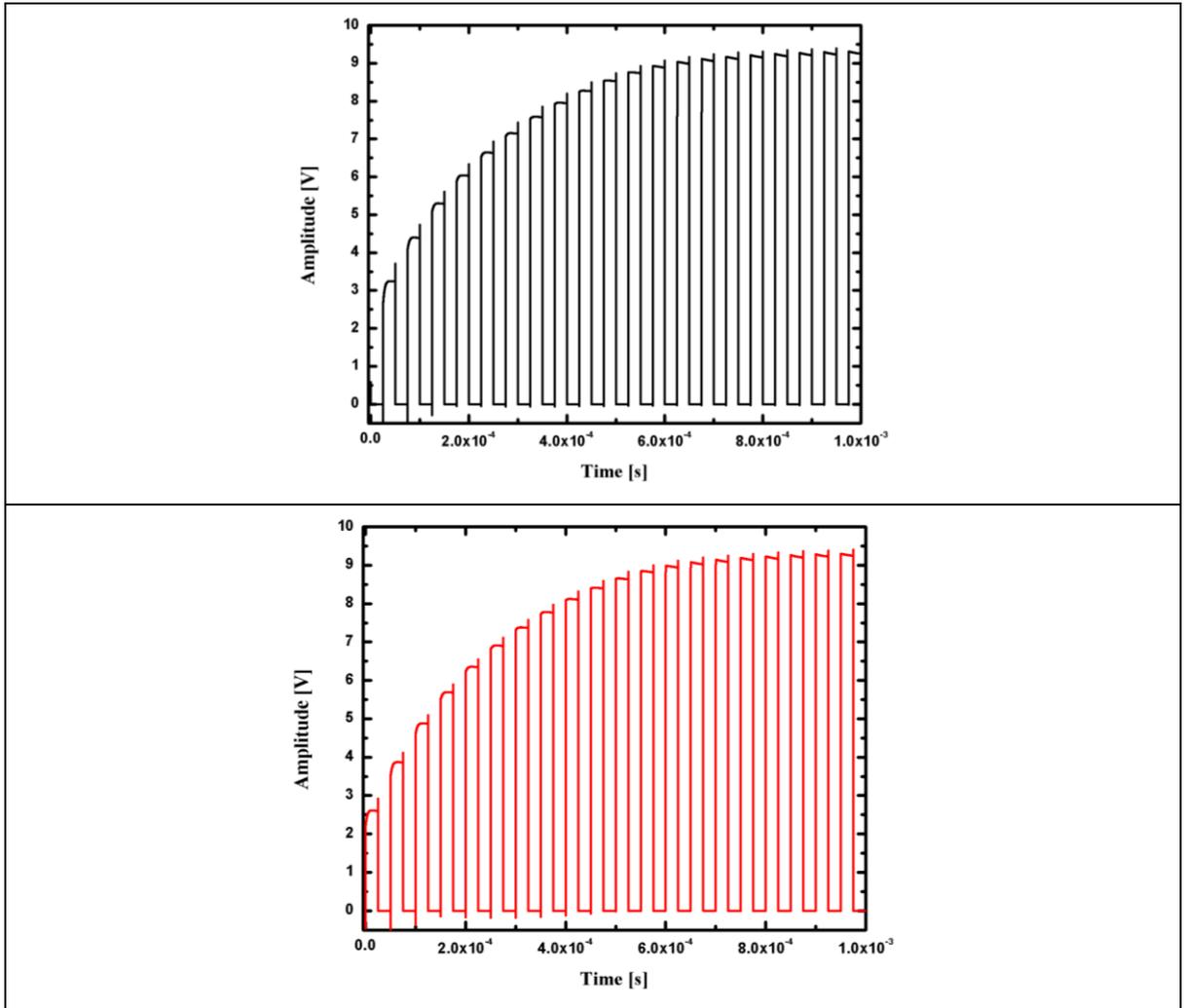
$$V_{out} = 2 \times V_{DD} - (I_{out} \times R'_s) \quad 4.11$$

Accordingly, the smaller the series resistance  $R'_s$ , the more efficient is the voltage doubler. Therefore, in order to have an efficient voltage doubler,  $R'_s$  has to be kept as small as possible. As was the case with the Dickson charge pump, the main contributor to the losses is  $R'_s$ , as given by **equation 4.8**. This can be reduced by increasing the size of the boosting capacitor and the operating clock frequency. The more extended form of  $R'_s$ , which is given by **equation 4.9** suggest that  $R'_s$  can be also reduced by decreasing the value of  $R_{on}$  which is inversely proportional  $W/L$  ratio  $I_{ds}$  of the device [106]. Therefore, small  $R_{on}$  is achieved by making the width  $W$  of  $M_1$  and  $M_2$  as large as possible. Furthermore, the value of  $I_{out}$  also determines the amount of voltage loss in the voltage doubler. As we will see in next section, for the 70  $\mu A$  current to be delivered to the output load (**Figure 4.13**), the spectre simulator suggests that the width of the transistor should to be as large as 2000  $\mu m$  with a length of 1.8  $\mu m$ .

**Figure title: Two stages high voltage clock generator**



**Figure 4.11 Schematic of two stages high voltage clock generator.**



**Figure 4.12** Simulations of the non-overlapping high voltage clocks generated from two stages high voltage clock generator.

The output voltage produced by the voltage doubler in **Figure 4.9** can be furthermore doubled using another voltage doubler that can be cascaded with the previous one. A cascaded voltage doubler is shown in **Figure 4.12**. In this configuration the outputs of the first voltage doubler are connected to the bottom plate of  $C_3$  and  $C_4$ . The supply voltage of this doubler is acquired by connecting the drains of  $M_8$  and  $M_7$  to the gates of  $M_1$  and  $M_2$  respectively. Now, at this stage the cascaded voltage doubler can generate a voltage that alternates between 6 V and 12 V at top plate nodes of  $C_3$  and  $C_4$ . These nodes are connected as supply voltage for the inverter (inv. 5) and inverter (inv. 6). The output of these inverters generates two non-overlapping clocks which alternate between 0 V and 12 V in the ideal case.

From an efficiency point of view and according to **equation 4.9**, it can be noted that  $R_{on}$  at the second stage is less than that of the first. The decrease in  $R_{on}$  is attributed to the increase in the value of  $V_{GS}$ . The threshold value  $V_{TH}$  also contributes to the decrease in  $R_{on}$  through the body effect phenomenon mentioned earlier in this chapter. In addition, the increase in the value of  $V_{TH}$  contributes in reducing the leakage current to the substrate - as will be shown later in this chapter.

Based on the fact that  $R_{on}$  in the cascaded stage is less than that of the previous one, one can say that increasing the number of the cascaded stages will not greatly affect the efficiency as the number of stages grows. In fact the effect of that decrease in  $R_{on}$  becomes insignificant to the effect of the series resistance that is accumulated when more stages are added. The overall  $R'_s$  dramatically affects the efficiency performance of the charge pump. Therefore, this topology has been confined to two stages where it gives its best performance. With no load at the output, the simulated output non-overlapping clocks generated from this topology are shown in **Figure 4.13**. The output clocks alternate between 0 and 9.42 V and can be calculated from

$$V_{out} = 4 \times V_{DD} - (I_{out} \times R'_s) \quad 4.12$$

Where  $R'_s$  becomes

$$R'_s = \left( \frac{1}{4 \times (C + C_s) \times f} + 2 \times R_{on(stage1)} + 2 \times R_{on(stage2)} \right) \quad 4.13$$

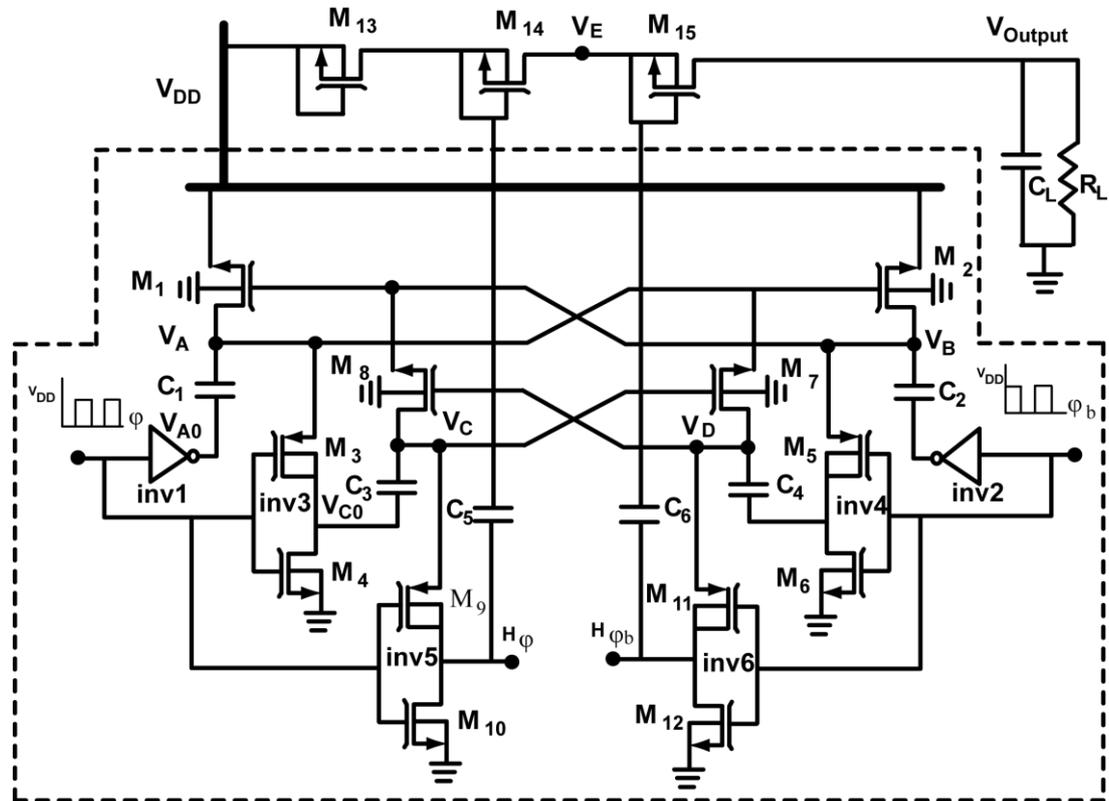
Where,  $R_{on(stage1)}$  is the ON resistance of the high voltage transistors in the first stage and  $R_{on(stage2)}$  is the ON resistance of the high voltage transistors in the first stage of the cascaded high voltage generator.

### 4.2.3 High voltage charge pump for MPPC biasing

In previous sections we have discussed in detail the implementation of the Dickson charge pump and voltage doublers along with the efficiency issue that usually accompany designing any DC-DC converter. It has been seen that a high voltage non-overlapping clock generator is an option for improving the efficiency of the Dickson charge pump. In

this section we will discuss how we can implement an efficient very high voltage charge pump that is capable of biasing the MPPC.

**Figure title: Single cell**



**Figure 4.13** Proposed single cell which produces  $9 V_{DD}$

Up to this point, we have already decided on the topologies of the circuits to be used for our charge pump. The charge pump consists of two main parts; the high voltage clock generator that generates the non-overlapping clocks and Dickson charge pump that is responsible for the transference of the charge to the load. These two parts are connected to form a single unit which can be called a cell for convenience. The single cell is configured as shown in **Figure 4.15** where the outputs of the high voltage generator at nodes  $H_\phi$  and  $H_{\phi_b}$  are connected to the bottom plates of the boosting capacitors  $C_5$  and  $C_6$  of the Dickson charge pump.

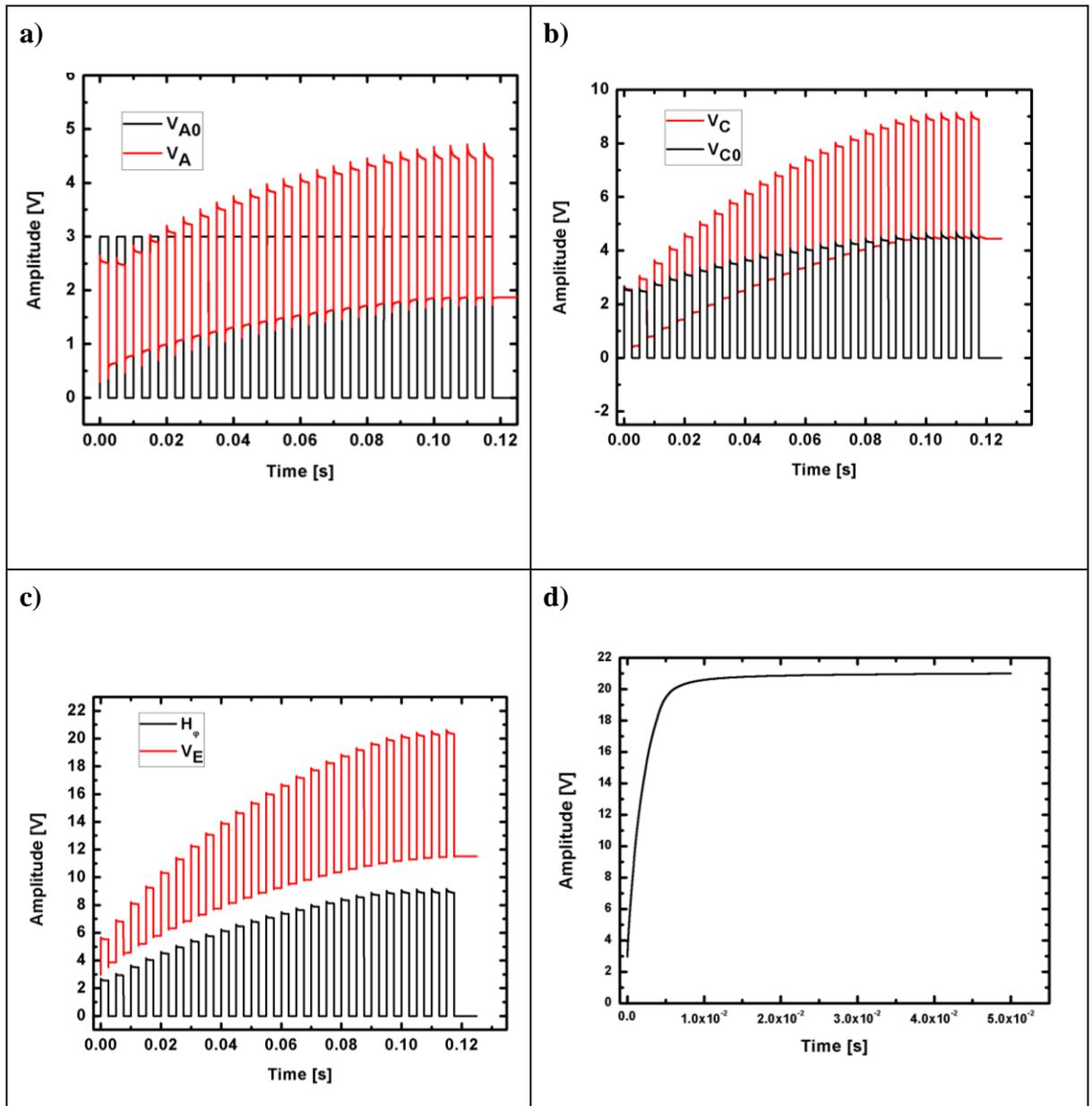
Conventionally, if a voltage doubler is to be used as a charge pump by its own, two PMOS transistors are used to transfer the charge to the load as in **Figure 3.17** [85]. In this work,

a different approach is proposed which uses a Dickson configuration for charge transfer purpose instead of the PMOS transistors. The configuration of this proposed topology is shown in **Figure 4.13**. This configuration has two main advantages over the conventional topology. This configuration offers more than twice the output voltage, ideally  $9 V_{DD}$ . The second advantage is that this configuration offers more than twice the output voltage using almost half the silicon area required if the conventional configuration is adopted. This is because, in order to produce  $8 V_{DD}$ , two cells have to be cascaded in such a way that the output of the first cell is used as a supply source for the second one which consequently doubles the area.

The output of the single cell is given by substituting the output voltage of the high voltage clock generator in **equation 4.12** into **equation 4.6** which yields:

$$V_{out} = V_{DD} - V_D + 2 \times \left( 4 \times V_{DD} - (I_{out} \times R'_s) - V_D - \frac{I_{out}}{(C + C_S)f} - I_{out} \times R_{eq} \right) \quad 4.14$$

The operation principle of the entire proposed charge pump in **Figure 4.13** can be summarised as follows: when  $\phi$  is low,  $M_2$  is on and  $C_2$  is charged to  $V_{DD}$ . Then, when  $\phi$  goes high,  $C_2$  retains some charge and the rest is shared with  $C_4$ . During subsequent cycles, charge is redistributed from  $C_2$  to  $C_4$  and then to  $C_6$ . Eventually, the charge on  $C_2$  builds up and  $V_B$  is elevated to  $2 V_{DD}$ . Then the alternating voltages  $V_{DD}$  and  $2 V_{DD}$  at  $V_A$ . Nodes  $V_A$  and  $V_B$  can be thought of as supplies for the high voltage inverters (inv3) and (inv4). The outputs of these inverters are non-overlapping clocks that swing between 0 and  $2 V_{DD}$ . The same happens with the next voltage doubler. That is when  $\phi$  high and  $\phi_b$  is low, inv4 charges  $C_4$  such that the voltage at node  $V_D$  reaches  $4 V_{DD}$ . The complementary situation arises with the left part of the circuit but is delayed by one half of the clock period as the left hand and right hand outputs and inputs are cross connected. The generated outputs from the high voltage inverters (inv5) and (inv6) are non-overlapping voltages that swing between 0 and  $4 V_{DD}$ . The  $V_{DD}$  connected to  $M_{13}$  will charge  $C_5$  to  $V_{DD}$ . Then when  $H_\phi$  is high, the voltage at  $C_5$  will rise to  $5 V_{DD}$  and be passed by  $M_{14}$  to  $C_6$ . After that, when  $H_{\phi b}$  goes high,  $C_6$  will rise to  $9 V_{DD}$  which will be then passed to  $C_L$  by  $M_{15}$ . The final output then appears at the output node at  $C_L$  and results in a  $9 V_{DD}$ .



**Figure 4.14** Simulated node voltages of single cell charge pump. a. Voltages at nodes  $V_{A0}$  and  $V_A$ . b. Voltages at nodes  $V_C$  and  $V_{C0}$  c. Voltages at nodes  $H_\phi$  and  $V_E$  d. Voltage at output node of the single cell charge pump.

The generated voltages at each node of the cell are simulated and shown in **Figure 4.14**. Because the voltage generator is a symmetrical circuit, only the nodes of the left hand side of the generator are shown. The simulated results are obtained with transistor dimensions as shown as in table 5.1 that lists the transistors along with their maximum operation voltages. At capacitive load  $C_L$  is equal to 6.8 nF and at boosting capacitors  $C$  equal to 2.2 nF each, the generated voltages at node  $V_{A0}$  which alternates between 0 and 3 V is boosted at node  $V_A$  and swings between 1.9 and 4.53 V which is less than  $2V_{DD}$  as in

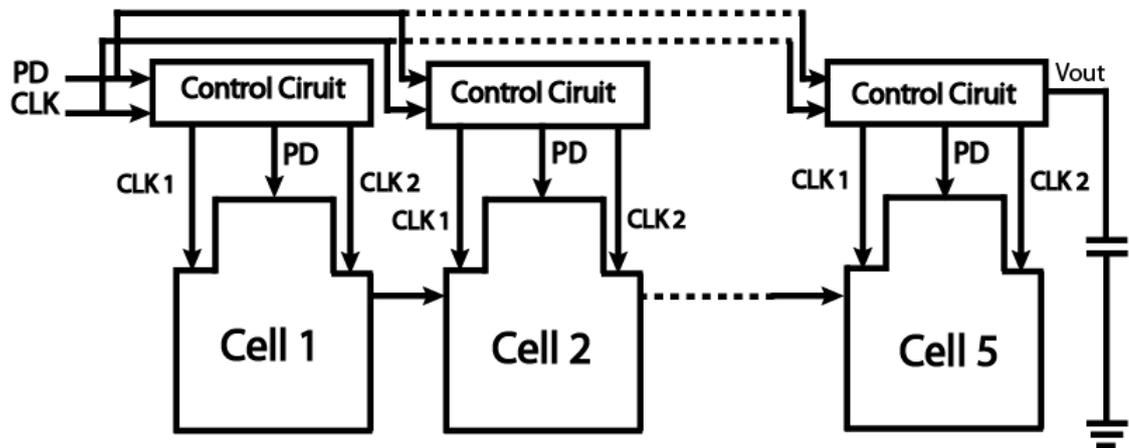
**Figure 4.14.a.** The 1.57 loss is attributed  $R_s$ . Inv.4 make the voltage generated at node  $V_A$ , swings between 0 and 4.63V at node  $V_C$  which is boosted to alternate between 4.53V and 8.56V at node  $V_E$  as shown in part b of **Figure 4.14**. The voltage at  $V_E$  is made to swing between 0 and 8.56V using inv. 6 at node  $V_G$  which passed to node  $V_H$  and boosted to alternate between 10.85V and 20.9V as shown in **Figure 4.14.c**. This voltage is smoothed at the output node and settles at 20.5V as shown in **Figure 4.14.d**.

**Table 4.1 Dimensions of the transistors and the maximum operating voltages.**

Transistor name	Type	Dimensions W ( $\mu\text{m}$ )/L( $\mu\text{m}$ )	Max. VG-SB	Max. VD-S	Max. VD-Psub
$M_1, M_2, M_8, M_7$	NMOS20HS	2000/1.8	20	20	50
$M_4, M_6, M_{10}, M_{12}$	NMOS20HS	500/1.8	20	20	50
$M_3, M_5, M_9, M_{11}$	PMOS20HS	1000/1.2	-20	-20	50
$M_{13}, M_{14}, M_{15}$	NMOSI20	200/0.7	1.2	20	50

So far, the implementation of the two main topologies of charge pumps ( the Dickson charge pump and the voltage doubler) has been discussed. We have also elaborated on the reasons why using a Dickson charge pump or a voltage doubler on their own is not sufficient to deliver the desired high output voltage with a reasonable efficiency. Consequently, an improved design, referred to as a single cell, which is a combination of both and is capable of generating 20.6 V has been discussed. Therefore, in order to generate the 72 V that is needed to bias the MPPC, we have decided to use 5-cells of the proposed single cell and cascaded them as shown in **Figure 4.15**. Here, the output of the first single cell at the drain of the diode-connected transistor is connected to the source-gate node of the diode-connected transistor of the next cell. Unlike the first single cell, the following cascaded cells will contain just two diodes on the charge transfer Dickson part of the charge pump. The 5 cascaded cells, according to simulation results, produces 98.5 V with no resistive load. Though this output voltage is more than what is actually required, nevertheless, the five cells are used so as to leave a margin for error and negate any sources of loss which only become apparent after fabrication.

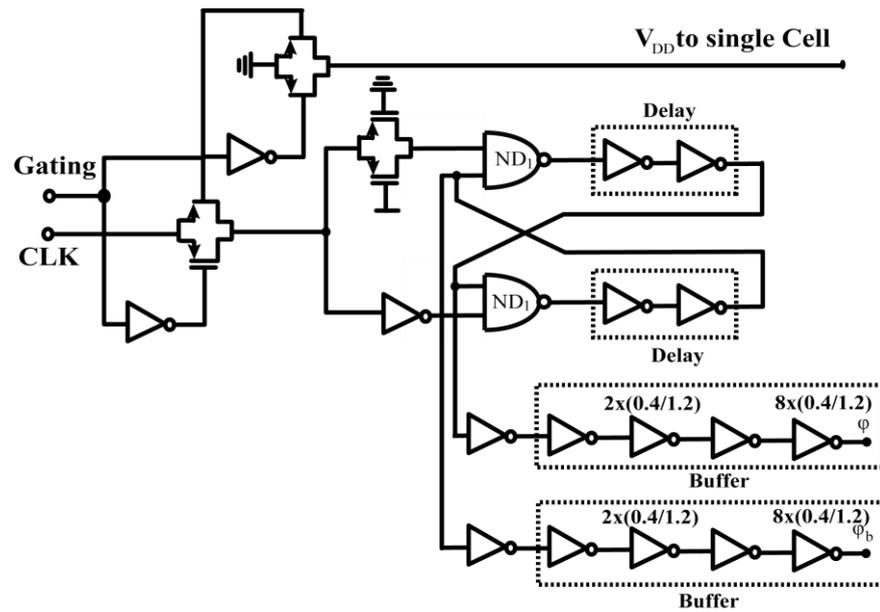
**Figure title: 5- cells charge pump**



**Figure 4.15 Proposed 5-cells charge pump.**

The high voltage charge pump is configured to have a single input clock that is supplied by a microcontroller unit – as discussed in chapter three. Therefore, in order to be able to derive the entire charge pump using a single clock that is generated from a unit that has limited current capability such as microcontroller, each cell was designed to have its own control circuit that incorporates the low voltage non-overlapping generator in **Figure 4.7**. At the output of the clock generator, a chain of inverters forming a signal buffer is added and configured as shown in **Figure 4.16**. This buffer is responsible for driving the thick oxide gates of the high voltage transistors used on the high voltage clock generator. The signal driving buffer consists of four inverters that were scaled up starting with a small size inverter and doubled in size in the next one. Two rows of these buffers are used at each end of the non-overlapping clock generator. The buffer has an even number of inverters. Using the simulator, four inverters were found to be adequate to drive the thick oxide gates and still be capable of generating the required non-overlapping clocks up to 200 kHz. The first inverter of the buffer geometries (W/L) of the NMOS is chosen be (0.4  $\mu\text{m}$  /1.2  $\mu\text{m}$ ), (0.8  $\mu\text{m}$  /2.2  $\mu\text{m}$ ) for the second inverter, (1.6  $\mu\text{m}$  /4.4  $\mu\text{m}$ ) for the third inverter and the final one is (3.2  $\mu\text{m}$  /48  $\mu\text{m}$ ). The PMOS transistor of each inverter has three times the size of NMOS transistors indicated above.

**Figure title: Control circuitry**



**Figure 4.16 Schematic of control circuit used with each single cell of the charge pump.**

The control circuit adds another feature which enables switching on and off the charge pump and can therefore help in the power consumption management. This was achieved by adding a transmission gate which is controlled by a clock signal called the ‘gating signal’. This transmission gate acts as a power switch which incorporates an NMOS and PMOS device. The sizes of these transistors are chosen to be  $(0.5/1500) \mu\text{m}$  and  $(0.5/3000) \mu\text{m}$  respectively. The reason that the size of these transmission gates are so big is that they are responsible for delivering the required current for operating each cell and it also allows for faster switching response, so that the rise and fall time of the overall generated output voltage is only dependent on the internal impedance of the charge pump output rather than the impedance of the power switching circuit. In addition to the main task of the transmission gate, which is to cut-off the power supply from the main body of the single cell, the gating circuitry is configured in such a way that, even if there is still a running input clock at CLK, the signal at (Gating) input will switch off the clock generator, so there is no clock propagating through the rest of the circuit and, therefore, negligible power is consumed.

#### 4.2.4 Layout

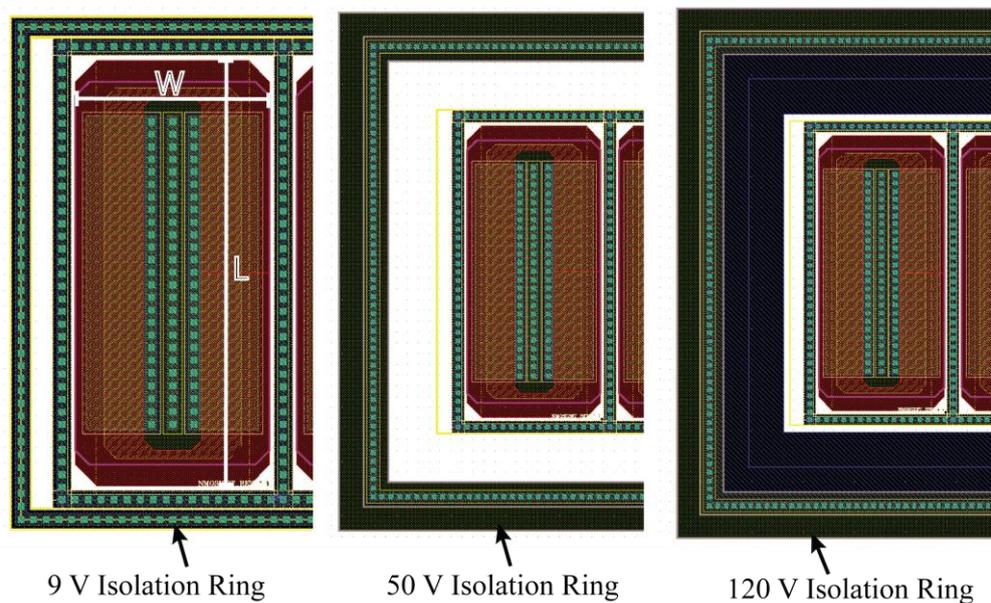
Due to the large size of the power devices and the large number of capacitors which are usually needed to build a high voltage charge pump such as the one we have designed, special consideration has to be given to efficiently using the available silicon area [85, 107]. In our case, 31 capacitors are needed to operate the five cells. The value of these capacitors and therefore their sizes will vary according to the required output current and clock frequency being used. According to simulations, the charge pump can drive an output resistive load equal to  $10\text{ M}\Omega$  and can sustain  $95\text{ V}$  at the output node. This output voltage is achieved by using 31 capacitors of  $2.2\text{ nF}$  each with a clock frequency of  $29\text{ kHz}$ . For two main reasons, laying out these capacitors is impractical. The first reason is that, in order to layout a capacitor using CMOS technology, one has to use either a poly-poly structure or a metal-insulator-metal structure (CMIM). If using a poly-poly, in order to layout a  $2.2\text{ nF}$  capacitor, we need  $2.5\text{ mm}^2$  of silicon area. That is, for 31 capacitors we need a total area of  $79\text{ mm}^2$ . On the other hand, if using the CMIM structure, almost  $4\text{ mm}^2$  is required, which, for a 31 capacitors, equates to  $11.5\text{ mm} \times 11.5\text{ mm}$  of chip area. As previously stated, it is impractical to have a chip of this size because of cost and the restriction imposed by the size of the envisaged capsule. The second reason that on-chip capacitors are not practical is that the operational voltages of these capacitors are limited. For the poly-poly and CMIM capacitors the maximum terminal voltage that these capacitors can tolerate is  $7\text{ V}$  which makes them unsuitable for use in our topology - which in some parts of the circuit needs capacitors that can tolerate up to  $98\text{ V}$ .

Based on the discussion above it was decided to use external capacitors. These capacitors will contribute greatly in minimizing the final size of the chip. Furthermore, having these capacitors as external components will give the additional benefit of allowing variation in the current drivability of the charge pump. Another great advantage that is gained when using external capacitors instead of on-chip capacitors is reducing the effect of the parasitic capacitors  $C_s$  which results in enhancing the overall efficiency of the charge pump. The only thing that can still contribute and can be considered as stray capacitance are the pad plus board wiring capacitances [84].

Another aspect that has to be taken into consideration when laying out the charge pump is the current leakage problem which arises due to the continuous switching nature and the handling of high-voltage swings in the charge pump [77]. In this work the ASIC is

designed to contain other low voltage circuitry such as the front end (to be discussed in the next chapter), any leakage current to the substrate will affect the operation of the circuitry that shares the same substrate. This leakage current is injected to the substrate every time one of the parasitic elements in the high voltage MOS devices is turned on. One of these parasitic elements is the pnp bipolar structure that is formed between DPWELL, DNWELL and PSUB. Due to the high voltage swing, a voltage spike between the rising edges or falling edges of the clocks can turn on the parasitic device and consequently inject current into the substrate. The same thing can happen with the diode parasitic elements in the NMOSHS that is formed between the PSUB and the DNWELL of the drain and the source of the transistor. These diodes inject current into the substrate when forward biased. In order to avoid the effect of these parasitic elements when turned on, each HV transistor has to be enclosed by a RPWELL or PDIFF. This ring has to be as close as possible to the active area of the transistor to ensure a very low substrate resistance that will ensure that the leaked current is collected efficiently by the ring[108, 109].

**Figure title: Guard rings**



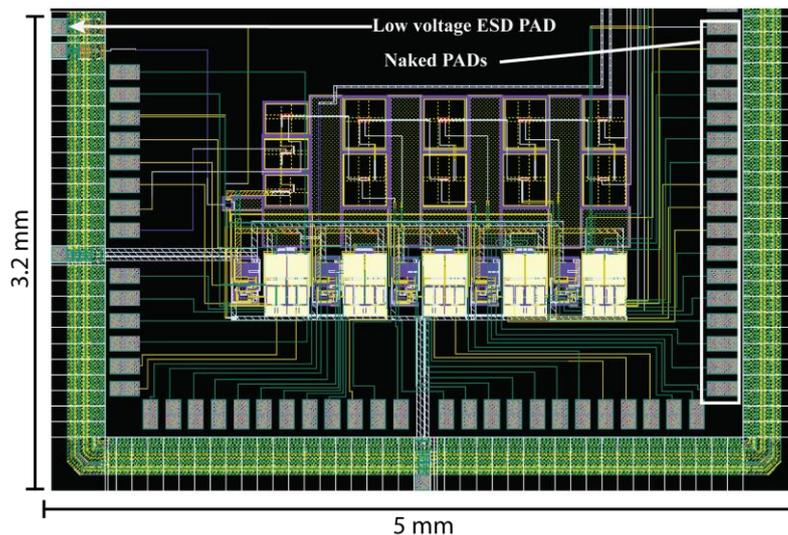
**Figure 4.17 High voltage guard ring available in the H35 process. The width (W) and the length (L) of the transistors is varied according to table 4.1.**

In addition to the use of the guard ring of the high voltage transistor in collecting the leakage current, the guard ring has another more important use. Depending on the type of guard ring being used, the break down voltage limit of  $V_{B-Psub}$  or the  $V_{D-sub}$  can be extended from 9 V up to 120V. Shown in figure 5.1.26 the three guard rings types which are

available with the process. The PDIFF guard ring can support  $V_{B-Psub}$  or  $V_{D-sub}$  up to 9V, RPWELL can support up to 50 V and the final type which is a wide RPWELL guard ring with extended metal one area can support up to 120V.

For our charge pump we have used the 50 V guard ring for all PMOS20HS to extend the  $V_{B-sup}$  and therefore withstand the 4  $V_{DD}$  generated from the high voltage clock generator. However, For the NMOSI20 transistors we have used the 120 V guard ring because at the final stages of the Dickson part of the charge pump,  $V_{D-sub}$  can reach up to 98 V according to the charge pump simulated output results. Based on the fact that  $V_{D-sub}$  maximum limit is 120 V, it can be said that our proposed charge pump configuration is limited to six stages and therefore the 120V is the maximum limit that our charge pump can reach.

**Figure title: Charge pump layout**



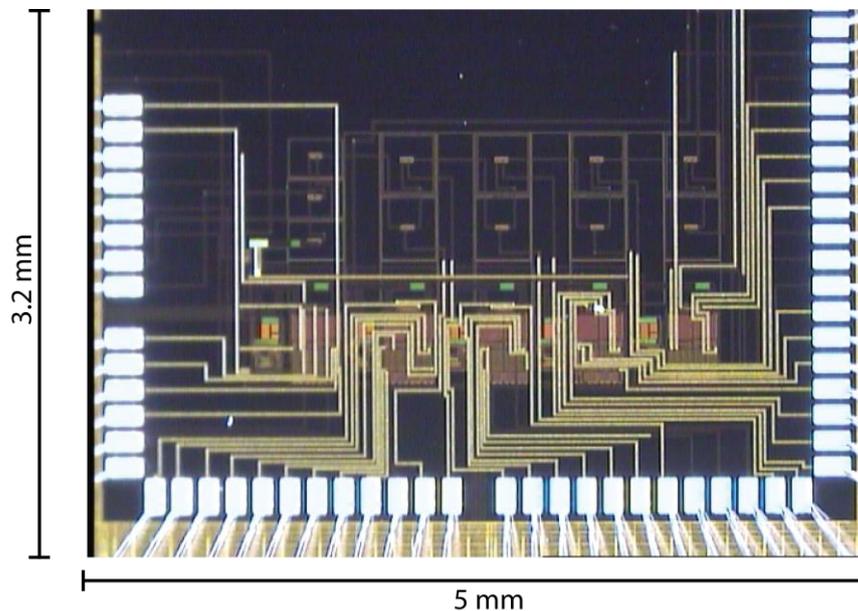
**Figure 4.18 Final layout of the 5-cells charge pump.**

The 5 cell charge pump has been laid out as shown in **Figure 4.18** in a silicon area (5 mm x 3.2 mm) including the pads. For the 31 external capacitors the charge pump needs 62 pads. The AMS library contains ready made pads that are equipped with electro-static discharge (ESD) circuitry. However these pads can only withstand up to 7V. Therefore, it was decided to only use these pads in places where an electrostatic charge can damage the charge pump. The places that are vulnerable to such discharges are the wire paths where it ends up connected to a gate of transistor such as the input gates of the clock generator. The rest of the pads are chosen to be naked pads without any electro-static discharge protection. These pads can withstand up to 120 V between the metal and the substrate.

### 4.3 Measurements

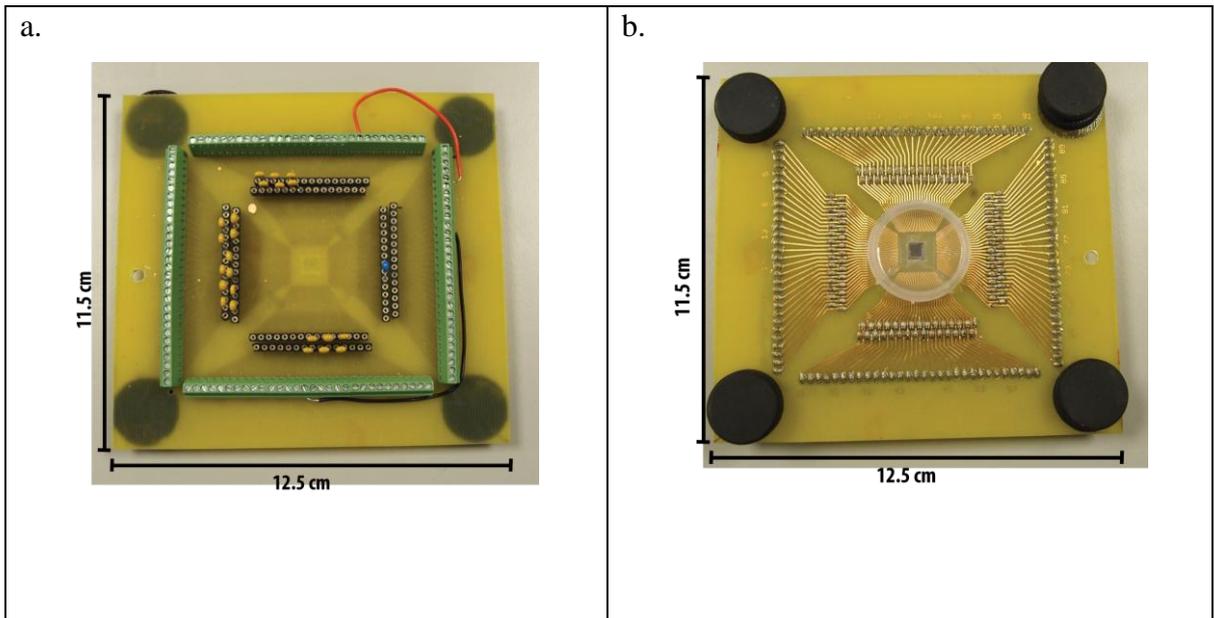
Along with the front end part of the ASIC (which will be discussed in the next chapter), the charge pump layout, which passed the Layout Versus Schematic (LVS) test and the Design Rule Check (DRC) test, was sent for fabrication. A micrograph of a part of the chip which includes the 5-cells charge pump with its control circuitry is shown in **Figure 4.19**. Upon receiving the fabricated chips, the test bench shown in **Figure 4.20** was fabricated in house for testing and evaluating the ASIC. A naked die sample was bonded to copper tracks that were soldered to pin heads used as sockets for capacitors. The use of these pinheads makes the test bench flexible to changes in the capacitor values and, therefore, changes in the current drivability of the charge pump. These tracks are extended and connected to mount terminals that are used as test points so the charge pump and its operation can be checked and debugged at each boosting node of the charge pump.

**Figure title: Charge pump part of the chip**



**Figure 4.19** A micrograph of the 5-cells charge pump with its control circuitry.

**Figure title: Test bench**



**Figure 4.20 A. Front-side of the Test bench used for evaluation of the charge pump**  
**b. back side of the test bench shows the bonded die covered by a plastic led to protect the wire bonding.**

#### 4.3.1.1 Output Voltage

In order to test the charge pump properly, 31 ceramic capacitors of value 2.2 nF are plugged into the allocated pin heads in the test bench one by one so as to make sure that every stage of any single cell is working properly. The non-overlapping clock generator was first constructed and tested. The measured results of the non-overlapping clock generator indicate a 9.8 V peak to peak clock generated out of every high voltage clock generator as show in **Figure 4.21**. The two clocks of each high voltage clock generator were connected to the charge transfer Dickson part of the charge pump. The generated output voltage was measured at the output node of the fifth stage using an oscilloscope with a high voltage probe which has a 2.2 M $\Omega$  input resistance. As shown in **Figure 4.22**, the generated output voltage is 81.9 V at a clock frequency of 37.6 kHz. However, when compared to the simulation results, it is noted that there is more than 16 V difference between the simulated and measured results. This difference is attributed to the load that is imposed by the oscilloscope prop. When measured by a multimeter with a 10 M $\Omega$  load, the charge pump is capable of generating up to 95.5 V. the relationship between the output voltage, delivered current and the resistive load will be explained in detail in the next

section and chapter 6 where we will see how this complex relationship plays a crucial rule in the detection efficiency of the light detector.

**Figure title: High voltage clocks**

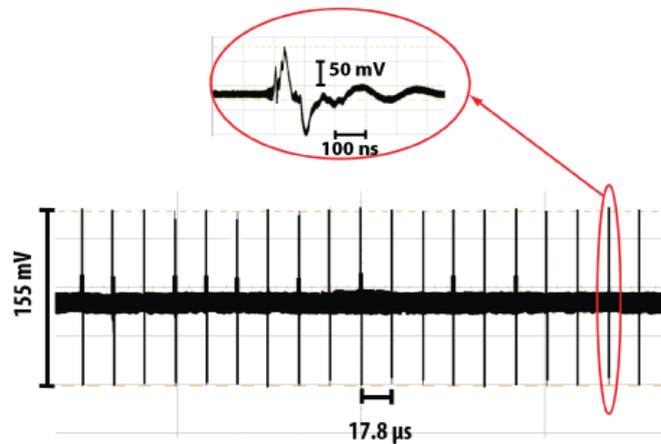


**Figure 4.21 Measured non-overlapping high voltage clocks.**

**Figure title: Output voltage**



**Figure 4.22 Measured output voltage at 37.6 clock frequency, 2.2 MΩ, 2.2 nF boosting capacitors and 6.8 capacitive load.**

**Figure title: Output ripple****Figure 4.23 Measured output ripple voltage at 2.2 MΩ and 6.8 nF load.**

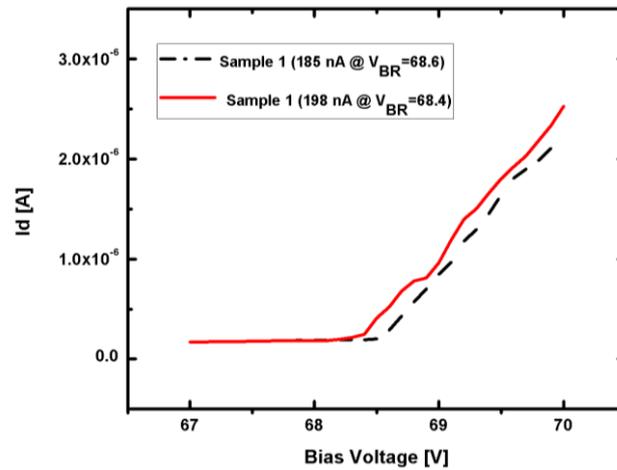
By using a 6.8 nF load capacitor, the charge pump takes 45 ms to settle at 81.9 V. The rise time was captured by the oscilloscope by exploiting the gating feature of the charge pump. The gating clock was set to 0.2 Hz, so the charge pump will be switched off every five seconds which is time enough to enable the capture and, thereafter, the measurement of the rise time of the charge pump output voltage - as shown in **Figure 4.25**. The rise time of the output voltage is a strong function of the capacitor value and can be reduced by reducing the capacitive load. However, in addition to the rise time, when a resistive load is added to the output node, the size of the capacitive load becomes important in determining the amount of ripple voltage that develops at the output. According to **equation 3.14**, the larger the output capacitive load, the smaller the ripple voltage. At 6.8nF capacitive load and 2.2 MΩ resistive load, the output ripple is 155 mV as shown in **Figure 4.23**. The spacing between ripples depends on the clock frequency, that is at 28 kHz, at every 17.8 ns there will a ripple spike. This ripple can be reduced to 60 mV if  $C_L$  is increased to 22 nF which in the other hand will increase the rise time to 64 ms.

#### 4.3.1.2 Delivered current

In order to design a charge pump that is capable of operating the MPPC, some important parameters regarding the MPPC (which will become the loading circuit) have to be determined. An accurate determination of these parameters enables the design of an efficient charge pump that is capable of delivering the required current along with the

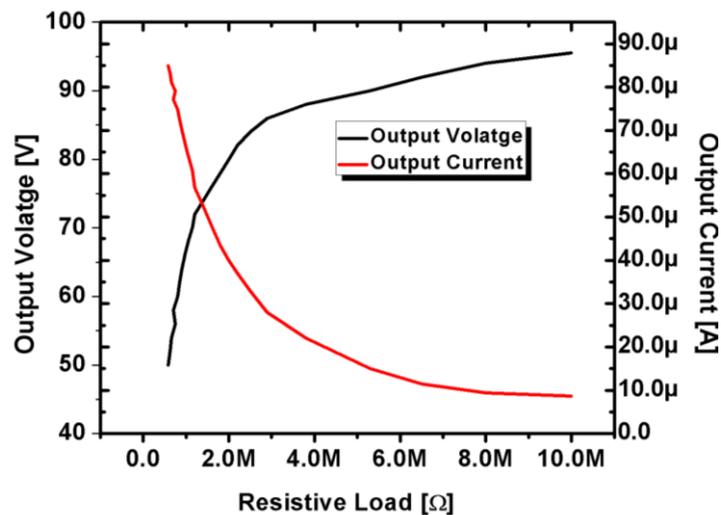
required voltage for our purpose. As we have seen in previous Section, the charge pump was able to generate 95.5 V at 10 M $\Omega$ . The 10 M $\Omega$  value load was derived from the I-V curve of the MPPC shown in **Figure 4.24**. According to this graph, the MPPC can be modelled as resistor that varies depending on the biasing voltage from 370 M $\Omega$  ((68.6 V)/(185 nA)) to 35 M $\Omega$  ((71.1 V)/(1.85  $\mu$ A)). Based on this information, a value of 10 M $\Omega$  was used as a target load for the charge pump at the simulation stage – thus giving a good safety margin.

**Figure title: I-V characteristic**



**Figure 4.24 I-V characteristic curve of the MPPC.**

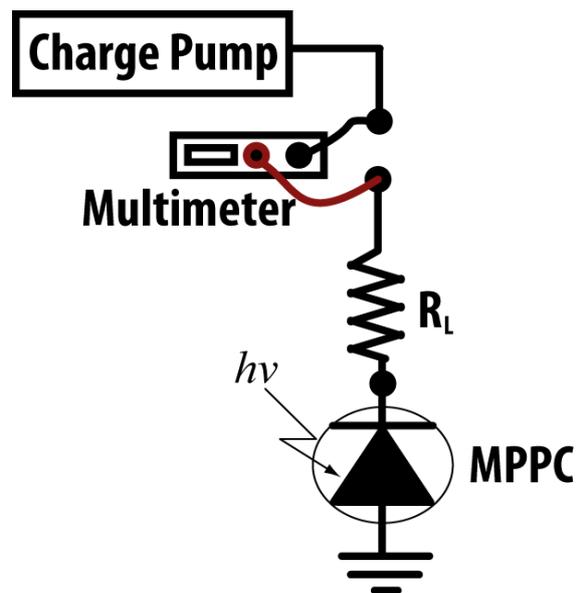
**Figure title: Charge pump characteristic**



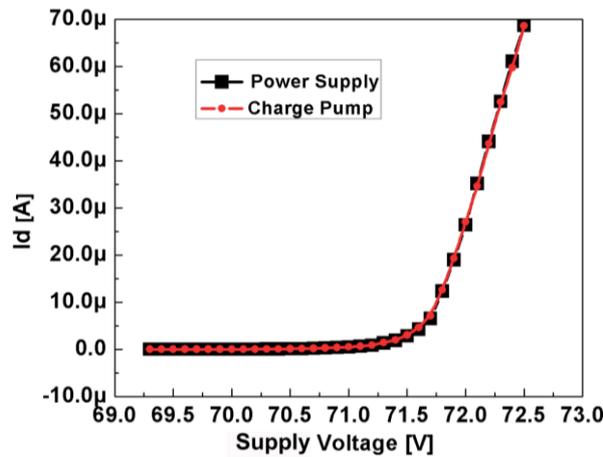
**Figure 4.25 Measured delivered current and voltage capability of the charge pump as function of resistive load.**

According to simulation results and the promising measured results, we can conclude that if the charge pump can drive a  $10\text{ M}\Omega$  while sustaining  $95\text{ V}$  it can certainly drive the  $35\text{ M}\Omega$  load presented by the MPPC at  $72\text{ V}$ . The relationship between the resistive load  $V_s$  current drivability and resistive load  $V_s$  voltage is shown in **Figure 4.25**. This measurement was acquired by sweeping the resistive load from  $500\text{ k}\Omega$  to  $10\text{ M}\Omega$  at fixed clock frequency equal to  $28\text{ kHz}$ . The graph shows how the charge pump generated output voltage is proportional to the value of the resistive load. That is the lower the resistive load value, the lower the generated output voltage. This is can be attributed to the source impedance of the charge pump which is proportional to the delivered current. This means that if the delivered current increases, the output voltage will decrease. From this graph we can note that the MPPC can be driven by the charge pump even if the MPPC terminal resistance reaches as low as  $1\text{ M}\Omega$ . This means that the charge pump can deliver current up to  $75\text{ }\mu\text{A}$  while sustaining  $73\text{ V}$ .

**Figure title: Test setup**



**Figure 4.26 MPPC circuit test configuration.**

**Figure title: MPPC I-V characteristic****Figure 4.27 Measured supply voltage and current by the charge pump to the MPPC.**

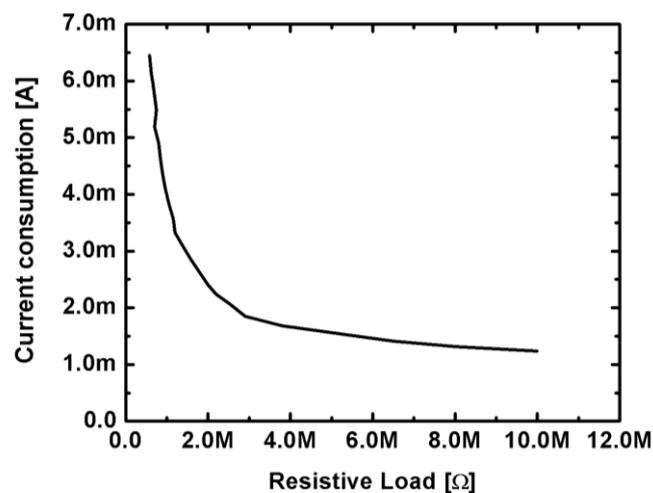
The charge pump capability of biasing the MPPC has been directly tested. The test configuration is as shown in **Figure 4.26**, where an accurate multimeter is placed between the charge pump and the MPPC. The multimeter is used to measure the current delivered to the MPPC and  $R_L$  as well as the capability of the charge pump to supply the MPPC with the required voltage (bias voltage + excess voltage). The generated voltage of the charge pump stepped gradually up to the break down voltage of the MPPC by the means of increasing the clock frequency. In order to probably test the charge pump maximum capability of supplying the MPPC, the MPPC is exposed to high intensity light near to its saturation where the terminal resistor reaches low values. At a clock frequency equal to 18.3 kHz, the charge pump can supply the MPPC by 72.5 V while supplying 68.4  $\mu$ A current. This means, at high intensity light, the terminal resistivity of the MPPC drops to less than about 1.5 M $\Omega$  according to the measurements shown in **Figure 4.25**.

To confirm its operation, the supplied voltage and current was measured at the same light intensity conditions, but this time was reversed biased by a bench-top power supply. The measured results in **Figure 4.27** show that the MPPC gives the same response whether supplied by the charge pump or by a bench-top power supply.

### 4.3.1.3 Power consumption

Power consumption can be categorised into two categories depending on the loading circuit: Capacitive load and resistive load. The charge pump drives the capacitive load until the output voltage is settled and then no dc current is drawn at the output node. If a resistive load is connected to the output node then a dc current is continuously supplied by the charge pump. The value of the supplied current depends on the value of the resistive load which consequently affects the power consumption of the charge pump. The overall power consumption of the charge pump including the control circuits is measured and plotted over a resistive load ranging from 500 k $\Omega$  to 10M $\Omega$  at a fixed clock frequency equal to 28 kHz. The measured results reported in **Figure 4.28** show that the power consumption decreases with an increase in the value of resistive load. With high intensity light, the terminal resistivity of the MPPC reaches about 1.5 M $\Omega$  and the charge pump draws 3.35 mA from the power supply.

**Figure title: Charge pump current consumption**



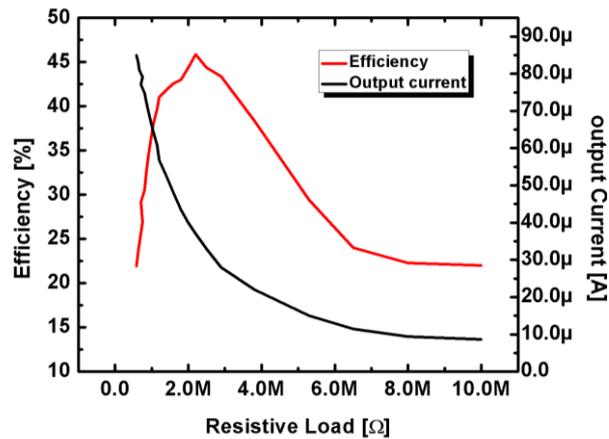
**Figure 4.28 Measured current consumption of the 5-cells charge pump with its control circuits at different resistive load.**

### 4.3.1.4 Power efficiency

The overall efficiency of the charge pump is evaluated and measured in this section. As is the case with the power consumption in the previous section, the efficiency of the charge pump is a function of the resistive load. The efficiency was measured at different resistive

loads using **equation 4.7**. **Figure 4.32** shows the power efficiency along with the current at the output node of the charge pump. The power

**Figure title: Power efficiency**



**Figure 4.29 Measured power efficiency at different resistive load values along with the supplied current.**

efficiency of the charge pump reaches a peak of 46% when resistively loaded at 2.1 MΩ. At this value, it can supply an output current of 37 μA. The efficiency results were obtained at a fixed clock frequency equal 28 kHz in which the charge pump can generate its maximum voltage. At high light intensity, the charge pump efficiency is 37%.

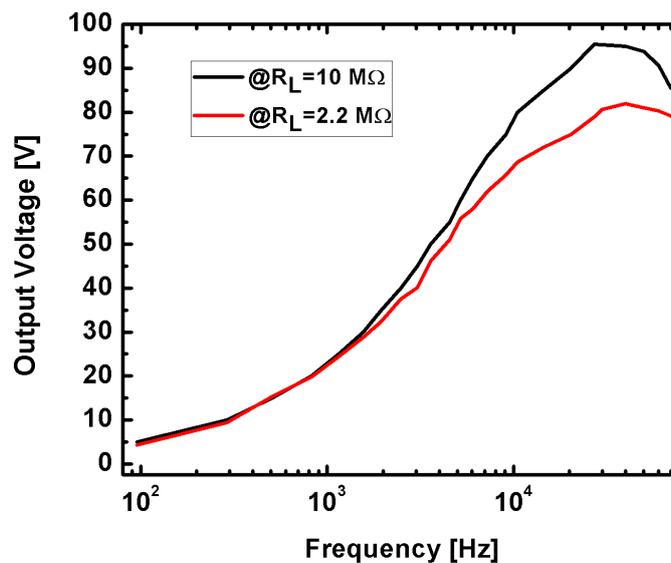
In comparison with the conventional Dickson charge pump and from an efficiency perspective, it is very clear that the proposed charge pump has ramped up the efficiency of the Dickson charge pump from 4% at 69 V, as demonstrated in **section 4.2.1**, to an efficiency equal to 46% at 73 V. It is worth mentioning that this comparison is done between simulated results of the Dickson charge pump and measured results of the proposed charge pump. Due to time constrains it was not possible to do a simulation-simulation comparison in the previous section. That is, in order to simulate the efficiency over the entire range of resistive loads for the charge pump, it may take several weeks to accomplish this operation. Running a single transient simulation for one second for the 5-cell charge pump with their control circuits can take up to two days even when running the simulator in a liberal mode. Due to the Safe Operation Area Check that the high voltage hit kit is equipped with, the simulator has to check and sends warning for every time any of the parasitic devices mentioned in **section 4.2.4** is turned on which dramatically slows

down the simulation time. For this reason it was more convenient to just run the simulations at one resistive load which was chosen to be  $10\text{M}\Omega$ .

### 4.3.1.5 Programmable charge pump

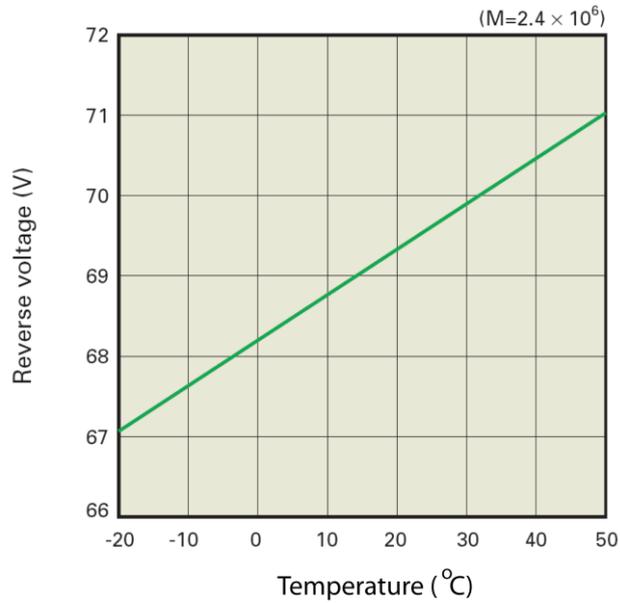
Designing an accurate charge pump that can deliver the exact voltage as intended is a very a difficult task if there is some ambiguity in the losses. Hence, from the design stage, a flexible design strategy was employed in order to allow compensation of any unexpected sources of loss. According to **equation 4.14**, there are three free parameters which can be used to change the output voltage. Under a fixed  $V_{DD}$  value condition, these are boosting capacitors, output current and clock frequency. By fixing the boosting capacitor and the output current (which is determined mainly by the resistive load) the exact value of the desired output voltage can be then solely determined by the clock frequency of the charge pump. The 5-cell charge pump has been designed from the start to have a single input clock which makes it more convenient to change the generated voltage as desired. Without this feature and with fixed output DC-DC converters, the charge pump would need to be followed by Low drop output (LDO) circuit which is used to regulate the generated voltage to the desired voltage [110]. However, the proposed design does not need LDO, and the output voltage is regulated by using the clock frequency.

**Figure title: Output voltage**



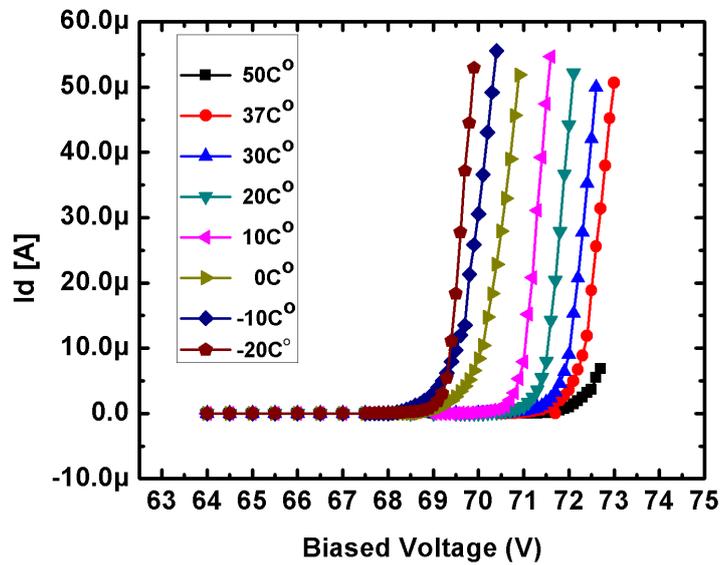
**Figure 4.30 Measured Output voltage as function of clock frequency.**

**Figure title: Bias voltage at different temperature points**



**Figure 4.31 Typical bias voltages of the MPPC device at different temperature points [67].**

**Figure title: Bias voltages at different temperatures**



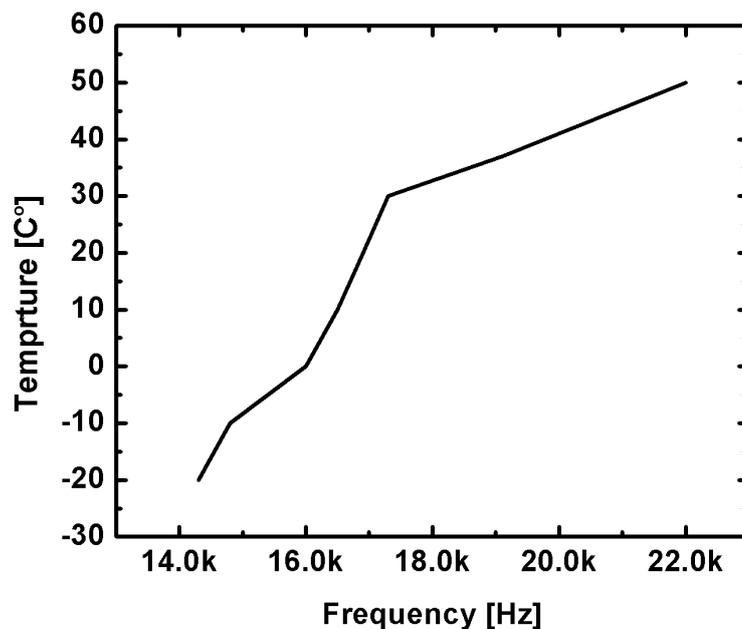
**Figure 4.32 Measured Bias voltages at different temperatures.**

The relationship between the frequency and the output generated voltage is shown in **Figure 4.30**. The charge pump can generate a voltage that varies between 3 V at 95 Hz to 95.5 V at 28 khz when loaded with 10 MΩ. However, when the charge pump is loaded

with  $2.2 \text{ M}\Omega$ , it generates a maximum voltage equal to  $81.9 \text{ V}$  when clock frequency is set to  $37.5 \text{ kHz}$ . Accordingly, the required frequency needed to bias the MPPC at room temperature when exposed to high intensity light is  $18.3 \text{ kHz}$ . This value is extracted from the  $2.2 \text{ M}\Omega$  trace at fig.5.1.40 which is close to the  $2.1 \text{ M}\Omega$  that appears at the MPPC terminals under high intensity light conditions. This relation will be elaborated on in detail in chapter 6.

The ability to control the generated output voltage by changing the clock frequency is exploited in programming the required biasing voltage which changes according to ambient temperature. As is the case with most Avalanche photon detectors, the MPPC breakdown voltage of the device is temperature dependent [111]. Figure 4.31, shows the relationship that describes the typical biasing value for the MPPC at different temperature points. Based on this graph, the MPPC was biased by the charge pump at different temperatures ranging from  $-20 \text{ }^\circ\text{C}$  to  $50 \text{ }^\circ\text{C}$  while exposed to a high intensity light so that the charge pump is evaluated and its performance is tested to its maximum limits. The measured I-V curves of the MPPC at different temperature points are shown in **Figure 4.32** and indicate that the charge pump can efficiently bias the MPPC at different temperatures. However, at  $50 \text{ }^\circ\text{C}$ , the charge pump failed to deliver more than  $10 \text{ }\mu\text{A}$  to the

**Figure title: Clock frequency different temperatures**



**Figure 4.33 Charge pump clock frequency for different temperature points.**

MPPC. This failure is attributed to the dark count pulses of the MPPC that increases dramatically at high temperature which, as a consequence, makes the MPPC require more current. Due to that rapid demand of current from the MPPC, the charge pump tries to compensate for that demand by giving up some of the generated voltage potential which as a result forces the voltage to drop below the brake down voltage every time it tries to do so.

At body temperature (37 ° C), the charge pump is able to deliver the required bias voltage (73 V) and current the required by the MPPC at a clock frequency equal to 19.5 kHz. The data that forms the relationship between the charge pump's clock frequency and the MPPC ambient temperature is plotted in **Figure 4.33**. Using this figure, one can directly extract the clock frequency needed for the charge pump to correctly bias the MPPC at its typical biasing conditions according to the ambient temperature.

#### **4.4 Summary**

This chapter has considered the design and fabrication of a very high voltage charge pump that can generate a variable high voltage greater than 72 V which is required to bias the MPPC device. The charge pump consists of 5-cells where each cell is a combination of a Dickson charge pump and a high voltage clock generator. The 9.8 V high voltage clock generator was employed to increase the efficiency of the Dickson charge pump. The high voltage was achieved by in the Dickson part of the charge pump by configuring the isolated high voltage transistor in a way that it yields a high voltage diode. This configuration of the transistor eliminated the  $V_{GS}$  breakdown limitation of the transistor as well as eliminating the body effect that grows as  $V_{BS}$  increases with each added stage. The charge pump was designed to be controlled by a single input clock which accordingly the generated voltage is varied. The charge pump was characterised and its operation was evaluated and presented. Its capability of delivering the required voltage 72 V at 70  $\mu$ A current to the MPPC was verified by directly biasing the MPPC to the output of the charge pump.

# Chapter 5 Front-end amplifiers

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## **5.1 Introduction**

The Austriamicrosystems AMS H35 process which is compatible with the low voltage process, allows the low voltage circuits as well as the reuse of the IP block provided by AMS to be integrated in the same chip. This compatibility is exploited in the ASIC and allows the integration of the front-end amplifiers with the biasing part of the system into a single chip. This integration contributes greatly in the miniaturization process of the pill. In the previous chapter we have discussed the design and the implementation of the high voltage charge pump which is responsible for providing the required high DC voltage for biasing the MPPC. In this chapter we will discuss the design of the second main block of the ASIC that is responsible for acquiring and then amplifying the pulses from the MPPC. The designed TIA is required to have more than 120 dB $\Omega$  and more than 20 MHz bandwidth to amplify the 10 MHz current pulses.

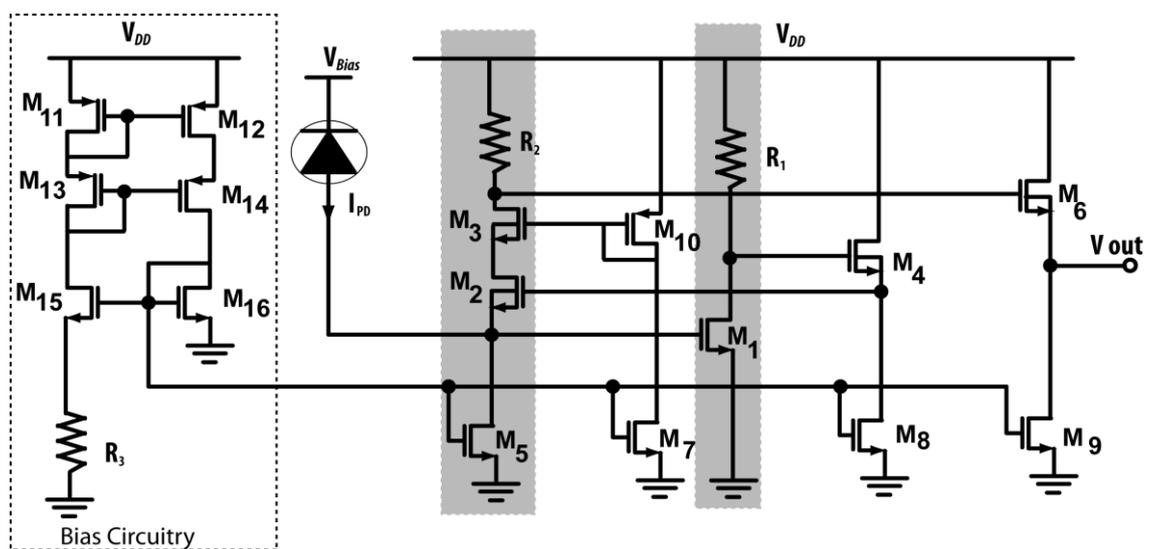
## **5.2 TIA design for MPPC read-out**

As mentioned earlier in **section 3.5.2**, the development of the low impedance, high gain TIA is based on the regulated cascode input stage (RGC) reported in [91]. The advantage in using this configuration is in its ability to ease the effect of the 37 pF terminal capacitance of the MPPC and therefore achieving high impedance, high gain and wide bandwidth. The design of the Proposed TIA shown in **Figure 5.1** is an improved version

of the RGC input stage shown in **Figure 3.19**, where the gain was boosted by adding a cascode stage to the main branch of the RGC and the bandwidth was increased by adding a CS stage between the feedback stage and the main branch.

We will consider the development of the TIA as a sequence of design steps. The proposed TIA shown in **Figure 5.1** is built on a simple Common Source (CS) stage composed of transistor  $M_2$  and a resistive load,  $R_2$ . The simulated open-loop gain of the CS amplifier is 22 dB and the gain-bandwidth product is 4.2 GHz with a phase margin of  $68^\circ$ . At this stage in the design process it is very important that the bandwidth should be kept as wide as possible in order to realise a high speed TIA. A lower gain can therefore be tolerated at this point and will be compensated for as the design is further developed.

**Figure title: Proposed TIA**



**Figure 5.1 Proposed low impedance, high gain TIA. The shaded branches represent the regulated cascode.**

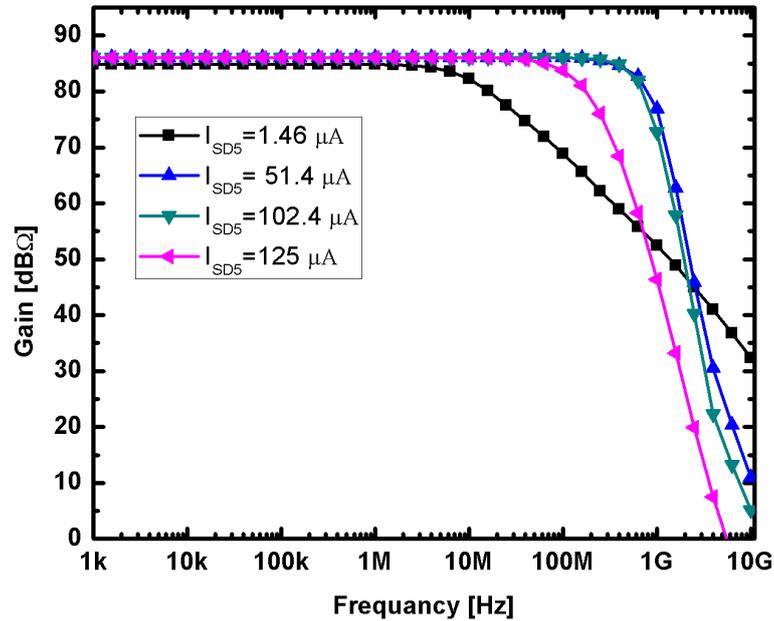
Now that the voltage amplifier is finalised, the TIA is formed by connecting a local feedback consisting of another CS of  $M_1$  and  $R_1$ . These two stages form an RGC similar to that of Figure 3.19 which has an input impedance given by [91]

$$Z_{IN,RCG}(\omega) \approx \frac{R_2}{1 + \left[ j\omega \frac{C_t + C_i}{g_{m2}(1 + g_{m1}R_1)} \right] [1 + j\omega R_2 C_o]} \quad 5.1$$

where  $C_o$  is the sum of the gate-drain capacitance ( $C_{gd2}$ ) and the drain-body capacitance ( $C_{db2}$ ) of  $M_2$ ,  $C_i$  is the sum of the source-body capacitance ( $C_{sb2}$ ) of  $M_2$  and the gate-source capacitance ( $C_{gs1}$ ) of  $M_1$ ,  $C_t$  is the MPPC terminal capacitance,  $g_{m1}$  is the transconductance of  $M_1$  and  $g_{m2}$  is the transconductance of  $M_2$ . Placing a source follower (SF) ( $M_4$ ) between the amplifier stage and the feedback stage will reduce the effect of  $C_{gd2}$  which will result in a lower input impedance. This is realized by connecting the output of the feedback to the input of the SF and then taking the output of the SF to the input gate of the CS amplifier. In order to ensure that the SF has unity gain and therefore avoid degrading the feedback CS gain, the input transistor of the SF is an isolated NMOS transistor (NMOSI). Taking advantage of working in a multi-well process (AMS H35), each of the NMOSI ( $M_4$  and  $M_6$ ) are implemented in their own deep-NWELL. The bulk-connection for these NMOSI is connected to their source to eliminate the body-effect and yield a unity gain SF [112]. In fact this is applied to all other transistors that will be used in building the front end. The use of isolated transistors will add another feature to the design. In addition to reducing the body effect problem, these isolated transistors will ensure that the front end circuit is well isolated and protected against any substrate current that might be injected by the charge pump to the substrate. As mentioned in **section 4.2.4**, due to the switching nature of the charge pump, the parasitic devices in high voltage transistors tend to inject current spikes into the substrate at each switching clock transition edge. These spike currents, especially if they are large in amplitude, can greatly affect the performance of the front end circuit.

One of the consequences of reducing the input impedance, by reducing the effect of  $C_{gd2}$ , is in pushing the dominant pole towards higher frequencies to produce a -3 dB bandwidth which is given by [91]

$$f_{-3dB} \approx \frac{g_{m2}(1 + g_{m1}R_1)}{2\pi(C_t + C_i)} \quad 5.2$$

**Figure title: Gain**

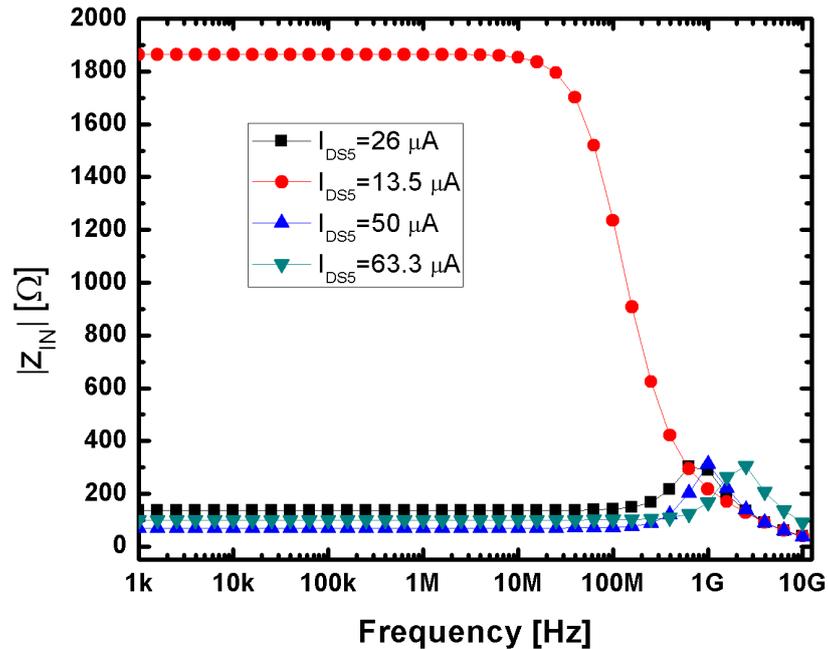
**Figure 5.2 Post-layout simulations of Gain characteristics at different bias currents.**

At this stage of the design, the TIA has a gain of 63 dBΩ and a -3 dB bandwidth equal to 883 MHz. The gain of the TIA can be boosted further by replacing the CS amplifier with a cascode configuration. The cascode configuration provides an extra gain boost to the TIA. Simulations indicate that at the output node of the cascode stage, the total gain of the TIA can reach more than 86 dBΩ. This gain is also maintained and buffered from any capacitive load by connecting the output of the cascode stage at the drain of  $M_3$  to the input of NMOSI SF ( $M_6$ ).

In order to establish more control over the various aspects of the design as we will see later, the source of the cascode amplifier transistor ( $M_2$ ) is connected to the output of the current mirror at the drain of  $M_5$ . The junction between the source of ( $M_2$ ) and the drain of ( $M_5$ ) has two functions. The first is to establish a fixed voltage between the gate and the source ( $V_{gs1}$ ) of  $M_1$  in the CS feedback stage, and the second is to control the bias current  $I_{DS5}$  in the cascode amplifier branch of the TIA. The value of  $I_{DS5}$  in the cascode branch determines the position of the dominant pole of the TIA as illustrated in **Figure 5.2**. The greatest 3 dB bandwidth is achieved for  $I_{DS5} = 55 \mu A$ . More current increases the voltage drop across R2 and consequently lowers  $V_{gs1}$  at the gate of  $M_1$  to beneath the threshold

voltage,  $V_{th}$ . Any reduction of  $V_{gs1}$  below  $V_{th}$  results in current starvation in  $M_1$ , hence reduced bandwidth. Fixing  $V_{gs1}$  to 650 mV, which is slightly more than the  $V_{th}$  of the NMOS transistors in the AMS 0.35  $\mu\text{m}$  CMOS process ( $V_{th} = 0.6$  V), ensures that wide bandwidth and low power consumption is achieved.

**Figure title: Input impedance**

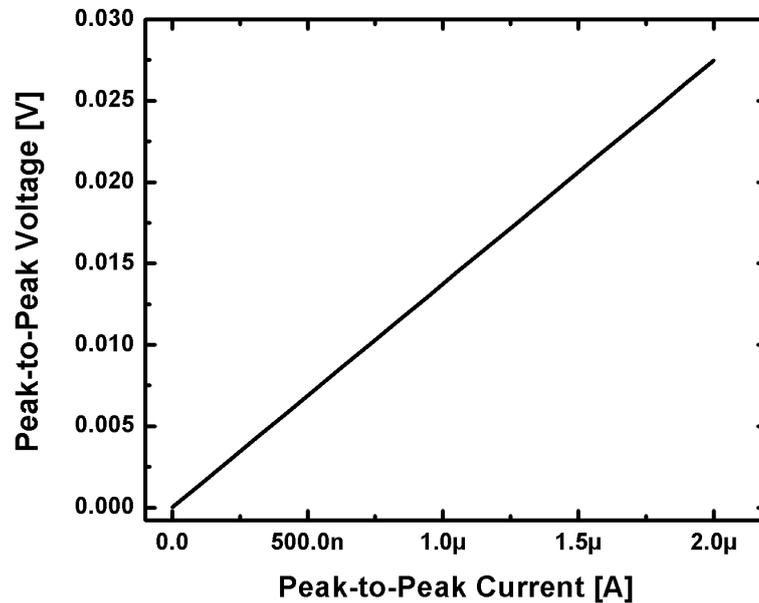


**Figure 5.3 Post-layout simulation of the Input Impedance of the TIA: Input Impedance varies with bias current.**

Another aspect of the design is the trade off between the bandwidth and the input impedance of the TIA that can also be controlled by  $I_{DS5}$ , as illustrated in **Figure 5.3**. The input impedance of the TIA decreases inversely with  $I_{DS5}$ . Thus, decreasing input impedance is achieved by increasing  $I_{DS5}$ . However, this causes the dominant pole to move towards lower frequencies. Therefore, by selecting  $I_{DS5} = 55 \mu\text{A}$ , the dominant pole can be maintained above 618 MHz with a moderately low input impedance of 75  $\Omega$ .

From **Figure 5.3** and **equation 5.2** it can be seen that  $g_{m1}$  and  $g_{m2}$  are the primary factors in determining the input impedance of the TIA especially at low frequencies. The value of  $g_{m2}$  is controlled directly by varying  $I_{DS5}$  and  $g_{m1}$  is varied indirectly via  $V_{gs1}$ .

**Figure title: Linearity**

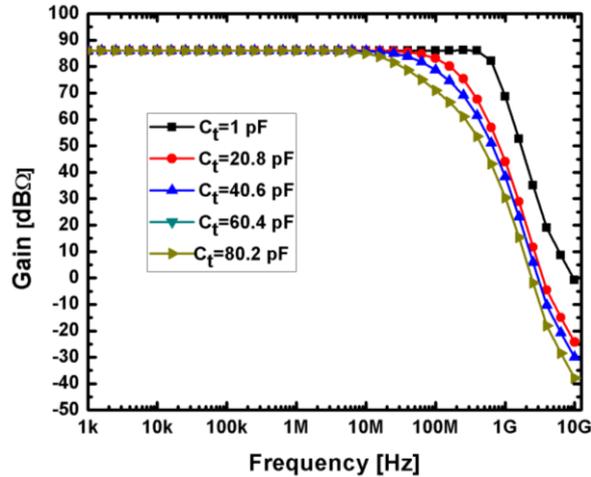


**Figure 5.4** Simulated Input-output characteristic of the TIA shows a linear relationship.

The linearity of the TIA is determined by the  $V_{gs}$  value of the feedback transistor  $M_1$  which is determined by  $I_{DS5}$ . As previously mentioned,  $V_{gs1}$  is fixed at 650 mV which is greater than  $V_{th}$  for the NMOS devices. The relationship between  $V_{gs}$  and  $I_{DS}$  is linear for  $V_{gs1} > V_{th}$ . This relationship manifests itself as a linear relationship between the input current of the TIA and its output voltage. As can be seen in **Figure 5.4**, the expected operation range of the MPPC's pulses (180 nA up to 2  $\mu$ A peak-peak) are linear with the TIA outputs. If desired, the circuit could be modified to give a logarithmic input-output relationship by operating  $M_1$  in the sub-threshold region [89]. This would be done at the expense of both gain and bandwidth.

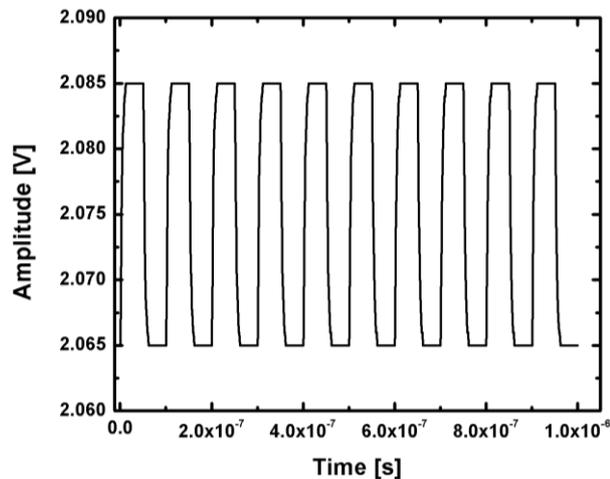
The effect of the terminal capacitance,  $C_t$ , of the SPAD array on the 3 dB bandwidth of the TIA is shown in **Figure 5.5**. When  $C_t = 37$  pF the expected 3 dB bandwidth exceeds 59 MHz. With this wide bandwidth, the TIA is able to capture and amplify the 10 MHz signal produced by the MPPC.

**Figure title: Bandwidth**



**Figure 5.5 Simulated frequency response of the TIA for various terminal capacitances.**

**Figure title: Output pulses**



**Figure 5.6 Post layout simulation of the transient response of the TIA for a 10 MHz current pulse input signal.**

For simulation purposes, the MPPC was replaced by a current source in parallel with a 40 pF input capacitance. The input capacitance represents the 37 pF terminal capacitance plus the pad capacitance which according to AMS documents is equal to 1.5 pF. The addition 1.5 pF represents any stray capacitors that might appear in the wiring and PCB

tracks. The TIA was simulated with and input square pluses at 10 MHz. The current pulses are 1  $\mu\text{A}$  peak to peak which results in an output voltage equal to 20 mV Peak to peak as shown in **Figure 5.6**. It is very important to note that all the simulations regarding the characterisation of the TIA were performed at the post layout stage. At this stage all layout stray capacitors that may affect the speed or the impedance of the TIA are taken into consideration.

**Table 5.1: Optimized component values of the TIA.**

Component lable	Type	Gate dimensions W ( $\mu\text{m}$ )/L ( $\mu\text{m}$ )	Design value
M <sub>1</sub>	NMOSI	250/0.35	
R <sub>1</sub>	Poly2	56/1.05	3.5 k $\Omega$
M <sub>2</sub>	NMOSI	50/0.35	
R <sub>2</sub>	Poly2	320/1.05	20 k $\Omega$
M <sub>3</sub>	NMOSI	30/0.35	
M <sub>4</sub>	NMOSI	10/0.35	
M <sub>5</sub>	NMOSI	27/1.05	
M <sub>6</sub>	NMOSI	150/0.35	
M <sub>7</sub>	NMOSI	9/1.05	
M <sub>8</sub>	NMOSI	15/1.05	
M <sub>9</sub>	NMOSI	4.8/1.05	
M <sub>10</sub>	PMOS	20/0.35	
M <sub>11</sub>	PMOS	5/2	
M <sub>12</sub>	PMOS	5/2	
M <sub>13</sub>	PMOS	5/2	
M <sub>14</sub>	PMOS	5/2	
M <sub>15</sub>	NMOSI	20/2	
M <sub>16</sub>	NMOSI	5/2	
R <sub>2</sub>	Poly2	240/1.05	15 k $\Omega$

The TIA is biased by a transconductance biasing circuitry as shown in **Figure 5.1**. This circuit is used to fixe  $I_{D55}$  at 55  $\mu\text{A}$  and to bias the rest of the TIA branches at (M<sub>7</sub>, M<sub>9</sub> and

$M_8$ ). The transconductance biasing circuit offers a temperature and power-supply independent biasing source. Although temperature dependence is of little effect on the TIA, power supply variation can affect the gain and the bandwidth of the TIA. Post layout simulation of the TIA along with its biasing circuitry shows that the TIA produces almost constant bandwidth and gain at power supply conditions ranging from (2.6 V to 3.3).

Optimised values and dimensions of all the components that were used to design the TIA along with its biasing circuitry are summarised in **Table 3.3**. All the transistors are isolated low voltage devices as we have mentioned previously. All transistors have minimum length of 0.35  $\mu\text{m}$  apart from  $M_5$ ,  $M_7$ ,  $M_9$  and  $M_8$  which have 1.05  $\mu\text{m}$  and  $M_{11}$ ,  $M_{12}$ ,  $M_{13}$ ,  $M_{14}$ ,  $M_{15}$  and  $M_{16}$  of the biasing circuit which are equal to 2  $\mu\text{m}$ . These transistors which are part of the biasing circuitry have wider length in order to offer more stability against temperature and process variations and therefore ensure stable biasing conditions. The width of the transistors and resistors are divided into fingers, so the TIA layout is as compact as possible.

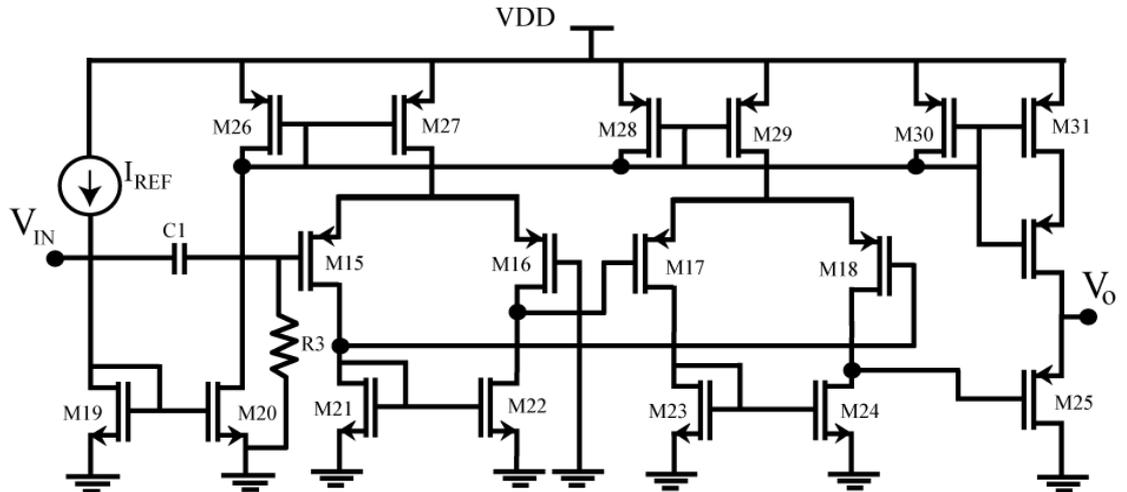
### 5.3 Post-amplifiers design

As is the case with most TIAs, the output swing is very small, especially when amplifying very small current signals such as those produced by the MPPC. A post-amplifier has therefore been employed to give further amplification. The post-amplifier consists of two cascaded differential amplifiers and is shown in **Figure 5.7**. The open loop gains of the differential amplifiers are 27 dB and 32 dB with 3 dB bandwidths of 55 MHz and 47 MHz, respectively. The post amplification process was carried out in two stages in order to maintain a wide bandwidth, which is achieved at the expense of the gain of the two amplifiers[113]. In addition to amplification, the differential amplifiers provide rejection of the common mode noise that might be introduced from the power supply [87].

The input of the post-amplifiers stage was connected to the output of the TIA at the SF stage. In order to avoid the need for any DC biasing circuits at the input stage of the differential amplifier, the post amplifier topology is chosen to have a PMOS input stage rather than a NMOS one. Thus, the output of the TIA is passed via a first order high pass filter consisting of  $C_1$  and  $R_3$ . This filter will remove the DC shift of the amplified signal shown in **Figure 5.6** and will bring it back to operate between 0 and 20 mV rather than being operated between 2.065 V and 2.085 V. The current reference ( $I_{\text{ref}}$ ) for the current

mirrors in the post-amplifiers circuit is a constant-transconductance bias circuit, the same as the one that was used with the TIA.

**Figure title: Post-amplifiers**



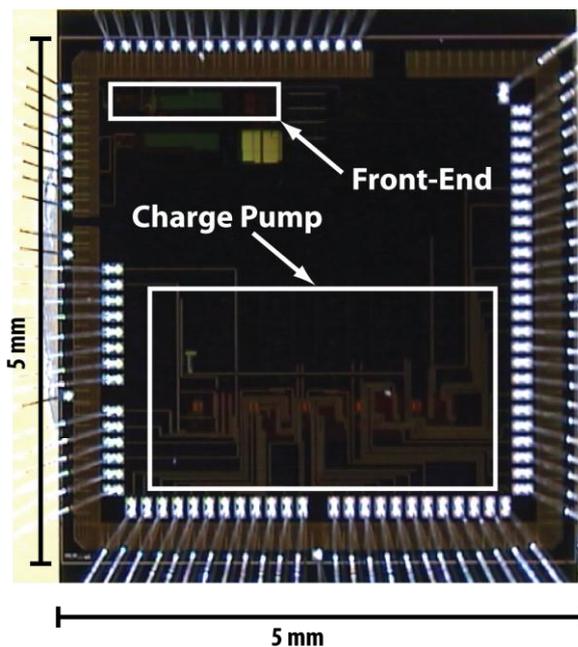
**Figure 5.7 Schematic of the post-amplifiers stage.**

All the components of the front-end, including the TIA and post-amplifiers, were all laid out as a compact single block to avoid any parasitic capacitors that might appear due to long wiring paths and thus preserving the fast performance of the front-end. The front end layout passed the Design Rule Check (DRC) and the Layout Vs Schematic (LVS) test successfully.

#### **5.4 Measurements**

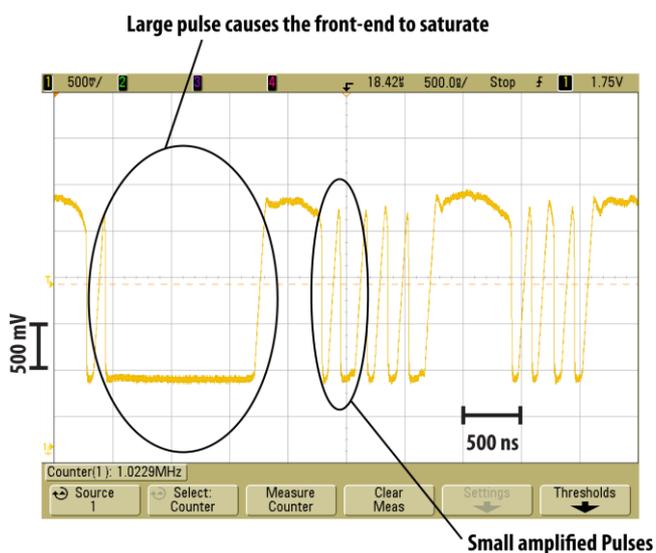
The front-end and the charge pump were fabricated in the same chip using a  $0.35\ \mu\text{m}$  high voltage CMOS (AMS H35) process. **Figure 5.8** shows a microphotograph of the front-end that occupies an area of  $0.6\ \text{mm}^2$  of the ASIC. The front-end has been tested with the MPPC device in order to evaluate its capability to amplify the 10 MHz pulses produced by the MPPC.

**Figure title: Fabricated ASIC**



**Figure 5.8** Microphotograph of the ASIC that includes the 5-cell charge pump block and the front-end block.

**Figure title: Output pulses**



**Figure 5.9** Measured front-end output pulses generated by the MPPC when moderately illuminated by a light source. The large pulse indicates that the MPPC was hit by several photons at the same time causing the TIA to saturate.

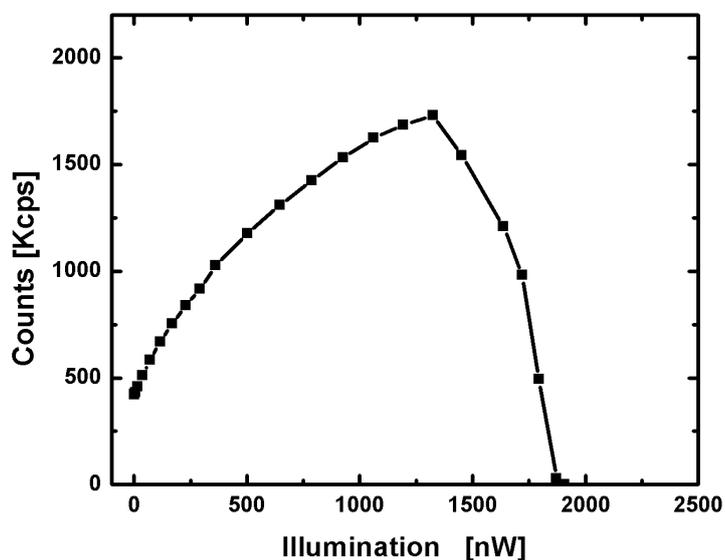
The MPPC is connected to the input port of the front-end and reverse biased by the charge pump at 72.5 V via a 10k $\Omega$  quenching resistor. **Figure 5.9** shows the amplified output waveform generated by the MPPC when all the pixels in the 10 x 10 array are exposed to moderate illumination from a light source. Under these conditions we were able to measure a response time (90 % - 10 %) of 21 ns for a voltage swing of 1.64 V at the output of the post-amplifier. The front-end, which was designed to have separate power pads from the charge pump, is consuming 2.7 mW of power. In terms of speed, the front-end was capable of operating in conjunction with the large terminal capacitance of the MPPC, and was able to capture pulses of ~200ns. By setting the trigger level of the oscilloscope channel to 900mV below the peak voltage of the SPAD, the oscilloscope can be used to count the number of photons detected in a known time.

A green LED was used in a dark room to illuminate different intestines at the MPPC. Theoretically, at high illumination, the oscilloscope counter is expected to count up to 10 Mega count pulse per second (Mcps). Unfortunately, measurements showed that the system failed to achieve this. This failure is attributed to the fact that during the design process we have overestimated the required gain to amplify the pulses produced by the MPPC. As result, the front-end suffers a saturation problem and therefore it was not able to amplify all the pulses generated by the MPPC.

Due to the parallel configuration of the pixel array in the MPPC device, the generated pulse at the output node, is the sum of all pulses generated simultaneously at each pixel [67]. In dark light conditions, the MPPC produces dark pulses of up to 400 Kilo count per second (kcps) where it is very rare that many pixels will generate dark pulse at exactly the same time. However, when the MPPC is exposed to relatively high illumination (greater than 1400 nW) , many pixels will be hit by photons at exactly the same time, this results in a single pulse from every pixel. These pulses are summed at the output node of the MPPC, and give birth to a large current pulse with high amplitude that corresponds to the number of hit pixels. The large pulses cause the front-end to saturate and thus affect its ability to capture the successive pulses. This problem can be seen clearly in **Figure 5.10**. This graph reports the reaction of the front-end and its effect on the final count of pulses when exposed to different light illuminations. At very low illumination (less than 1400 nW), the number of counted pulses increases proportionally with the increase in light intensity. However, when the illumination is increased, the number of large pulses starts to increase, and therefore causes the front end to saturate for several hundreds of nano-seconds. As a

result of this, the number of pulses counted is decreased until the front-end gives a flat response and no more pulses are amplified.

**Figure title: MPPC count rate**



**Figure 5.10 Count rate of the MPPC versus illumination power.**

Despite the saturation problem that arises at high illumination especially above 1400 nW and as will be seen in section 6.5, it can be said that MPPC can operate safely under low illumination such as that produced by autofluorescence. However, it was decided in this project to take the design one further step and integrate a CMOS SPAD in the same chip instead of using the off-chip light detector (MPPC). This integration has several advantages: firstly, CMOS SPADs require low bias voltages less than 30 V which results in a smaller charge pump. Secondly, Integrating the SPAD with the charge pump in the same chip will reduce the size of the pill. Thirdly, the integration can open the opportunity for further development of the pill, so it can be upgraded to perform both steady-state autofluorescence imaging or life-time imaging.

## 5.5 Summary

This chapter has discussed the steps of designing and implementing a front-end that can work in conjunction with the MPPC device that has a very large capacitance of 37 pF. The adaptation of the regulated cascode input stage (RGC) helps to minimize the effect of the input capacitance on the bandwidth and the input impedance of the TIA. It was also shown how the RGC gain was improved by adding a cascode stage and how the bandwidth was improved by adding source followers. The proposed TIA was able to achieve 75  $\Omega$  input impedance, 86 dB  $\Omega$  gain and 3 dB bandwidth equal to 59 MHz. The TIA was cascaded to a post amplifier stage that consisted of two differential amplifiers in order to provide extra amplification. The front-end was fabricated in the same chip with the charge pump designed in chapter 4. Unfortunately, due to overestimating the required gain out of the front-end, it was noticed after testing the MPPC that the front-end was suffering from a saturation problem, especially at relatively high intensity illuminations (greater than 1400 nW). However, under low illumination condition (less than 1400 nW), the MPPC is operating normally and therefore it is expected to cope with the weak autofluorescence emission. In the next chapter, the MPPC is replaced by an SPAD that is integrated with the charge pump which makes the design of the pill more compact and more efficient in terms of power consumption. As it will be seen in next chapter the integrated SPAD does not require a TIA to acquire the current pulses. Furthermore, the integrated SPAD requires only 22 V for biasing instead of the 72 V which is required by the MPPC.

# Chapter 6 Integrated-SPAD pill prototype

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## **6.1 Introduction**

This research project has been focused on the design, implementation, testing and experimental evaluation of an ASIC which was incorporated into a swallowable pill for detection of cancer through autofluorescence. In chapters 4 and 5 we have discussed the design and the implementation of the ASIC which includes a high voltage charge pump  $>72$  V to bias the off chip MPPC and front end circuitry to acquire the pulses produced by the MPPC. In this chapter the miniaturization process is taken a step further by integrating the light detector along with the biasing block and the front-end into a single chip.

This chapter starts with section 6.2 which considers the feasibility integrating a SPAD and charge pump into an ASIC. In section 6.3, the design and implantation of the ASIC is described. This is followed by the measurement section that includes detailed evaluation measurements of the SPAD, charge pump both separately and in combination. The operation of the ASIC is verified using optical measurement and biological measurements with real lamb small intestine that shows the ability of the ASIC to measure autofluorescence.

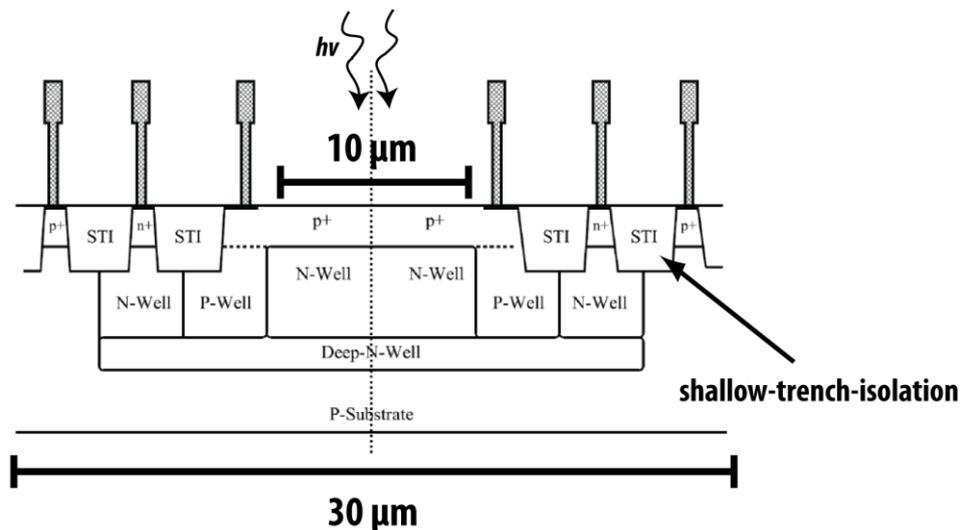
## 6.2 Integration feasibility

In this section as a first stage of developing a more integrated system for the diagnostic pill, the feasibility of using an integrated charge pump to bias a SPAD and the response of the resulting system has been investigated [114]. A CMOS SPAD that has been developed by the research group at the University of Oxford has been tested and with the charge pump whose development is described in chapter 4.

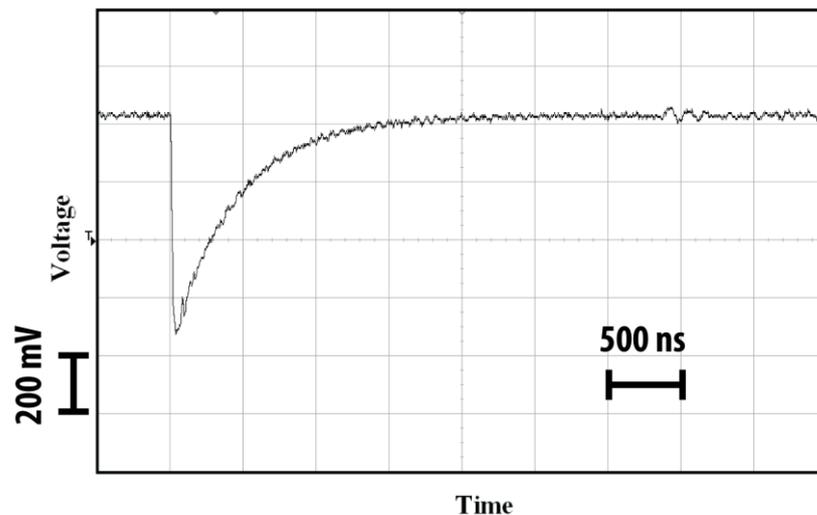
### 6.2.1 CMOS SPAD in UMC 0.18 Process

The SPAD that was developed by the Oxford group was fabricated in a CMOS 0.18 $\mu\text{m}$  triple-well technology. The cross section of the SPAD is shown in **Figure 6.1**. It is a 10 $\mu\text{m}$  diameter P+/N-well junction that forms the active area of the device which is surrounded by a P-Well guard ring. Tests on these devices show that typically they have a breakdown voltage of 10.4V.

**Figure title: SPAD Cross section using UMC technology**



**Figure 6.1** A cross section through the centre of a circular SPAD showing the guard ring of low doped material used to reduce the electric field at the edges and corners. The active area is 10  $\mu\text{m}$  diameter, and the overall SPAD area including guarding is 30 $\mu\text{m}$  diameter.

**Figure title: SPAD response**

**Figure 6.2** The response of the SPAD to a single photon shown on a screen shot of an oscilloscope. Also shown on the left hand axis is a T marking the trigger level.

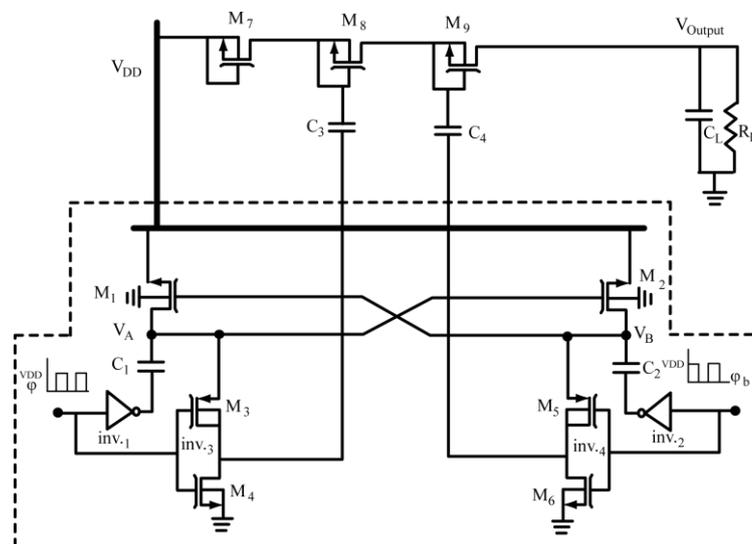
To test the basic operation of the SPAD and its suitability for fluorescence detection, the SPAD was operated in Geiger mode using a 10 k $\Omega$  resistor as a quenching circuit. A green LED was used as light source and a regulated bench power supply was used a voltage source for biasing purposes. The response of the SPAD is shown in **Figure 6.2**. The produced pulses have a width of  $\sim$  400ns and amplitude that can vary according to the supplied over-voltage.

### 6.2.2 Half cell charge pump

As we have seen from measurement results in chapter 4, the 5-cells charge pump can produce up to 98 V. This voltage can be varied and fixed at any desired voltage below the 98 V by changing the frequency of the clock. However, the flexibility of the charge pump design and the use of external capacitors whose values may be changed has enabled us to break down the charge pump into smaller units and therefore generate exactly the required voltage. For the SPAD to be tested, it requires 10.8 V to be biased by 400 mV over voltage. This voltage can be achieved using just half of the cell in **Figure 4.15**. This configuration is a combination of Dickson charge pump and a 6 V non-overlapping clock generator. The schematic of the half cell is shown **Figure 6.3**, where inside the dotted box is the clock voltage generator and the Dickson charge pump is formed by ( $M_{13}$ ,  $M_{14}$  and  $M_{15}$ ).

The basic operation of the charge pump depends on the non-overlapping 3 V peak to peak clocks  $\phi$  and  $\phi_b$ . The clocks charge the capacitors  $C_1$  and  $C_2$  successively to produce a shifted clock alternating between 3 and 6 V at nodes A and B. The two outputs of the voltage doubler are then connected to form the power supply to inverters 3 and 4 in order to create a boosted clock that swings between 0 V and 6 V. The generated high voltage clocks charge the 10 nF capacitors  $C_3$  and  $C_4$  and are then passed by  $M_8$  and  $M_9$  along with  $V_{DD}$  which is passed by  $M_7$  and finally accumulated at 100nF output capacitor  $C_L$ . The measured output voltage of the charge pump when it is unloaded is 11.5 V with a rise time of 90 ms at capacitive load  $C_L=100\text{nF}$ .

**Figure title: Half cell charge pump**

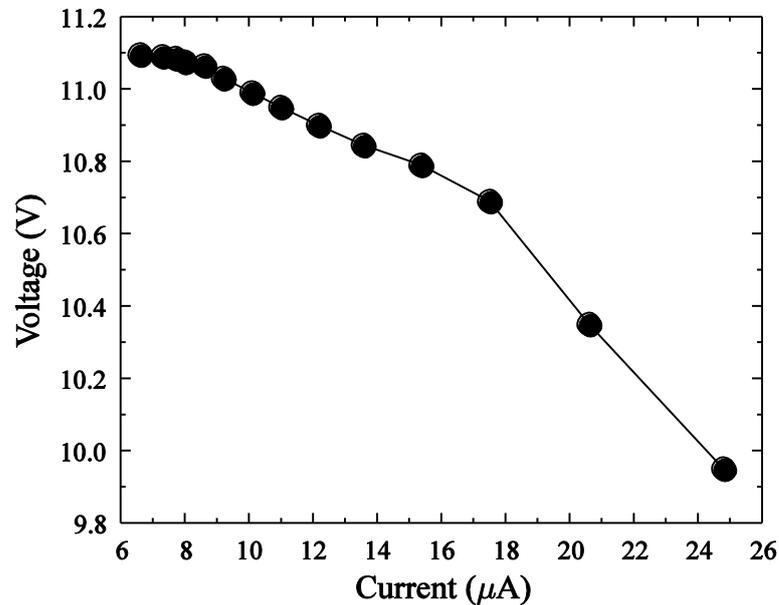


**Figure 6.3 Schematic of half cell high voltage generator.**

The behaviour of the charge pump over the expected region of operation has been investigated. According to the photon detection probability (PDP) measurements conducted with the SPAD it was found that the SPAD is best biased between 10.4 V and 11.4V. Accordingly the charge pump behaviour at this region was investigated by using various load resistors. The measured results reported in **Figure 6.4**, shows that the charge pumps will be able to deliver 6  $\mu\text{A}$  to the SPAD while sustaining 11.1V. However the output voltage will decrease as the resistive load is increased. With this reduction in output voltage, the output current increases up to 24  $\mu\text{A}$ . More importantly, these results

show that this charge pump can generate voltages higher than 10.4 V whilst delivering currents of less than 20 $\mu$ A.

**Figure title: charge pump output voltage and output current.**

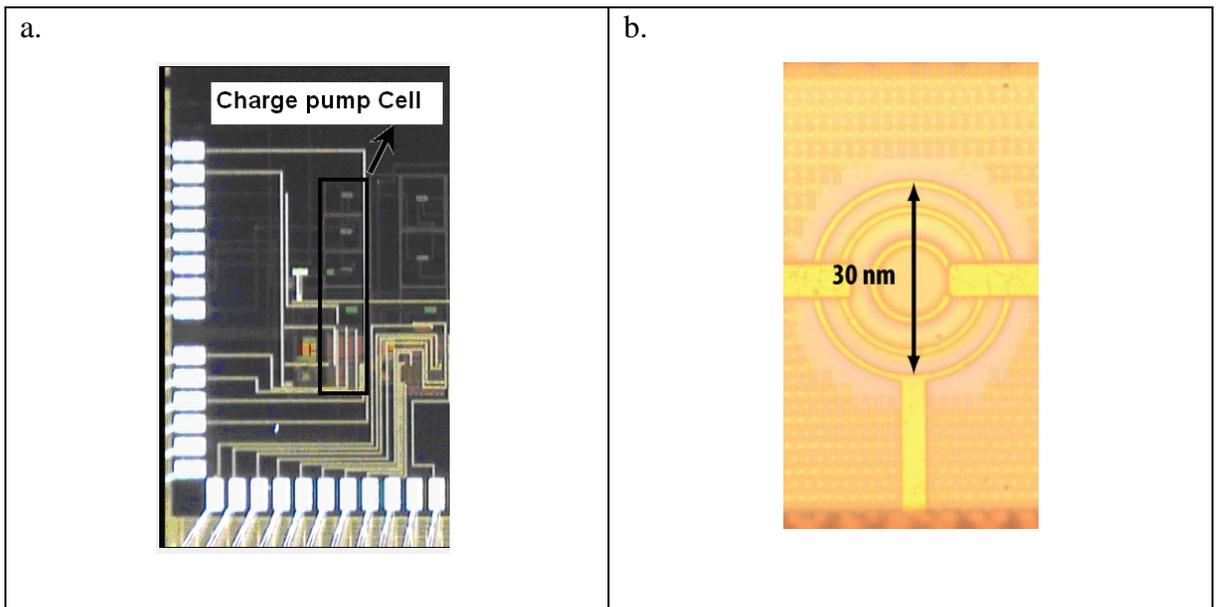


**Figure 6.4 Measured relationship between the output current and output voltage of the charge pump when the clock is 11 kHz.**

### 6.2.3 Combination

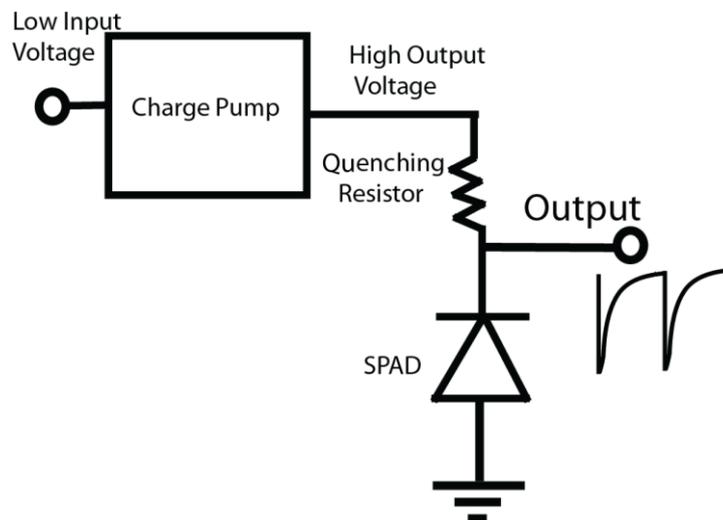
The fabricated charge pump and the SPAD are shown in **Figure 6.5**. The fabricated charge pump has an area of approximately 900 $\mu$ m by 350 $\mu$ m. where the overall diameter of the SPAD is 30  $\mu$ m. The charge pump and the SPAD are configured as in **Figure 6.6** where, the charge pump is used to bias the SPAD via a 10k quenching resistor. The operational behaviour of the combined circuit is investigated using a green LED, with a peak wavelength of 570nm and FWHM (Full Width Half Maximum) of 25nm installed at the entrance port of an integrating sphere to form a uniform illumination at the exit port. The SPAD was placed at the exit port of the integrating sphere.

**Figure title: Fabricated charge pump and SPAD.**



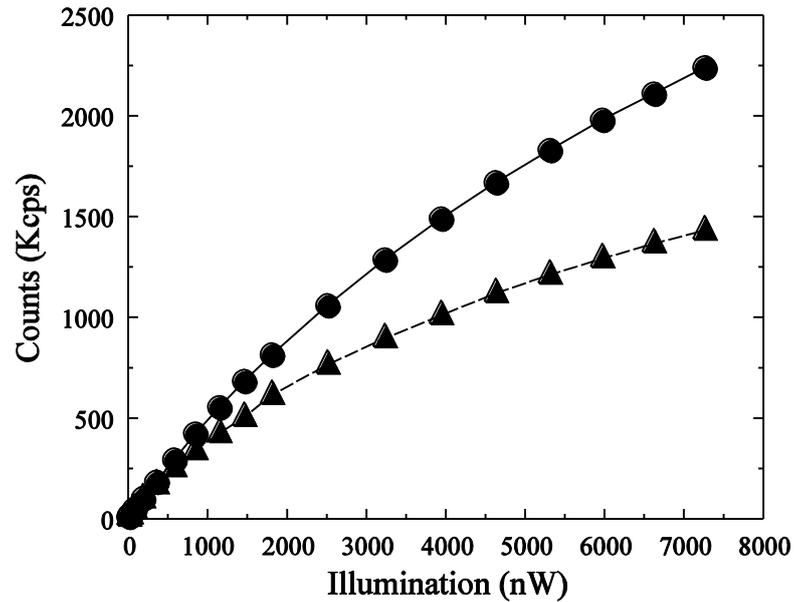
**Figure 6.5 Micrograph of the charge pump cell ( $900\mu \times 350\mu$ ), (B) SPAD  $10\mu\text{m}$  diameter active area and  $30\mu\text{m}$  overall diameter including guard rings.**

**Figure title: Configuration of the charge pump and the SPAD**



**Figure 6.6 Block diagram showing the connection between the charge pump and the SPAD.**

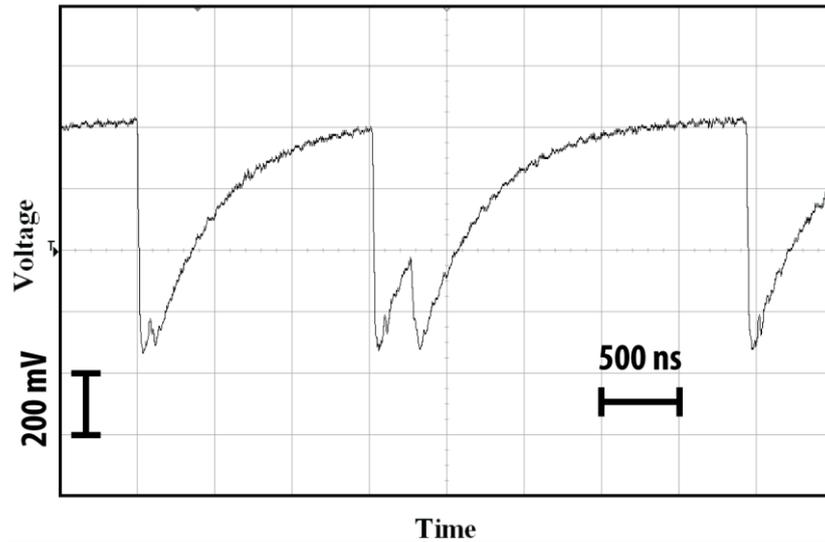
**Figure title: SPAD count rate responses**



**Figure 6.7** The count rate of the SPAD versus illumination power, when the SPAD is biased by either a regulated bench power supply (●) or the charge pump (▲). The overvoltage at low light levels for both sets of data is 0.7V.

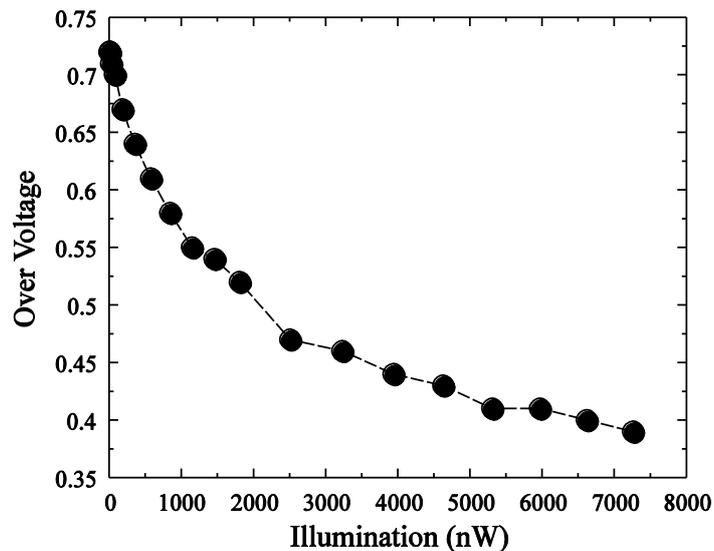
The response of the SPAD to various light intensities has been tested when it is biased either from a regulated bench-top power supply or from the charge pump. In these experiments the illumination intensity was varied. For an ideal photon detector the number of photon counts per second should be proportional to the light intensity. However, the results in **Figure 6.7** show that the SPAD count rate is not proportional to the illumination intensity. The origins of this effect can be understood by examining the temporal response of the SPAD, such as that shown in **Figure 6.8**. A photon is counted when the voltage increases through a trigger level following a sudden decrease caused by a photon. The first pulse in **Figure 6.8** is the response to a single photon, which is counted successfully. However, this response shows that there is a delay of approximately 150ns between the photon and the time at which it is detected. If another photon is detected within this time window then the voltage will only cross the trigger level once and the system will count one rather than two photons.

**Figure title: SPAD generated pulses**



**Figure 6.8** The response of a SPAD at a high illumination intensity shown on a screen shot. Also shown on the left hand axis is a T marking the trigger level.

**Figure title: Over voltage Vs illumination**



**Figure 6.9** The over voltage versus illumination intensity when the SPAD is biased by the charge pump.

In **Figure 6.8** the double peaked response in the centre of the figure corresponds to a situation in which the second photon has arrived before the first photon has been detected and so this first photon has not been counted. This effect explains the non-linear response obtained when the SPAD is biased using a bench top power supply [58, 115].

Another effect of increasing the illumination intensity falling on the SPAD is that since it increases the average count rate it must increase the current flowing through the SPAD. This means that current drawn from the power supply increases when the light intensity increases. This effect is irrelevant when a bench top power supply is used but it is critical to the design of an integrated charge pump. This effect can be attributed to the source impedance of the charge pump and the diode resistance of the SPAD ( $R_d$ ) which decreases inversely with the illumination.

The ability of the charge pump to bias the SPAD whilst supplying the required current was also tested. The results in **Figure 6.9** show that as the illumination intensity increases the increased current drawn from the charge pump causes a reduction in the bias voltage applied to the SPAD.

The effect of the illumination dependant over voltage when using a charge pump can be determined by comparing the responses of the SPAD when it is biased by a bench top supply and by the charge pump. These two responses in **Figure 6.7** show that once the count rate starts to exceed 500 kcps then the current drawn from the charge pump affects the overvoltage and hence the photon detection probability. However, at the low light levels that are relevant for fluorescence detection of cancer the charge pump is as effective as the bench top power supply.

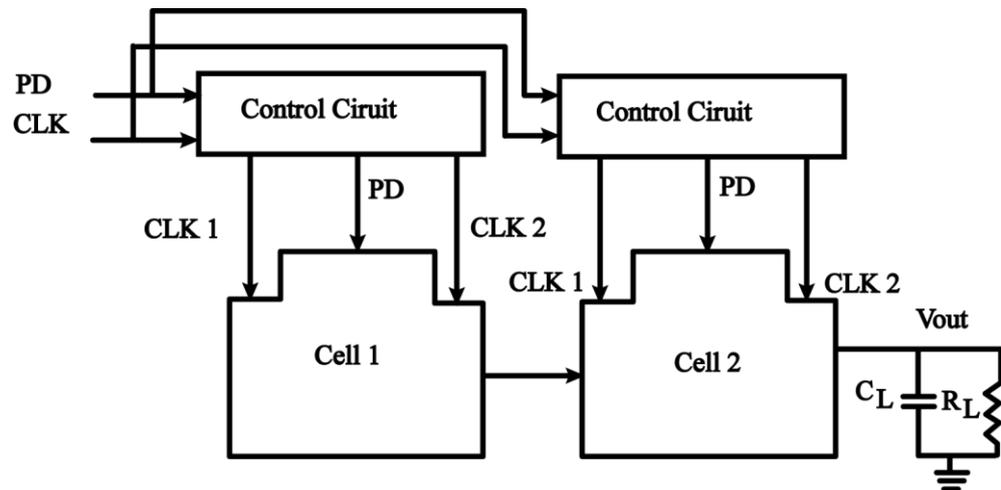
### **6.3 Integrated SPAD chip**

Measurements in previous section have shed light on some design issues that should be taken into consideration when integrating a SPAD with charge pump. Part of the previously designed charge pump was reused in the new ASIC which also incorporates a SPAD with its passive quenching circuitry. Unlike the previous ASIC, the CMOS integrated SPAD does not require any pre-amplification (i.e TIA) and requires lower bias voltage as we will see later in this section. The ASIC has been designed also in the 0.35 $\mu$ m AMS high voltage technology. Though low voltage charge pumps and SPADs can be realized in standard CMOS technologies [116], the AMS H35 technology which is a triple well process has been chosen in order to isolate the SPAD and its circuitry from any substrate noise that can be generated for the high voltage charge pump [77].

### 6.3.1 2-cell Charge pump

Depending on the implementation technology the breakdown voltage of an SPAD can range from 10 to 500 V [58]. However, SPADs realized in advanced CMOS technologies can yield lower breakdown voltages of  $< 20\text{V}$ . Recent literature has reported SPADs exhibiting breakdown at 10.4 V [117], 12.4 V [116], and 17.3 [118] which were fabricated in 90 nm CMOS, 130 nm CMOS, and 0.35  $\mu\text{m}$  CMOS technologies respectively. Indicating that smaller feature size leads to lower breakdown voltage. This is due to the fact that doping concentration is higher in the smaller CMOS technology nodes resulting in a smaller depletion area formed which decreases the breakdown voltage of the SPAD's p-n junction [96, 97]. Based on the breakdown measurements obtained by [118], it was decided to design a charge pump that can produce  $> 25\text{ V}$  for use in the H35 process. This being the sum of the voltage required to reach the breakdown point of the SPAD plus several times the excess voltage  $V_{\text{ex}}$ .

**Figure title: Two cells charge pump**



**Figure 6.10 Block diagram of two cells charge pump.**

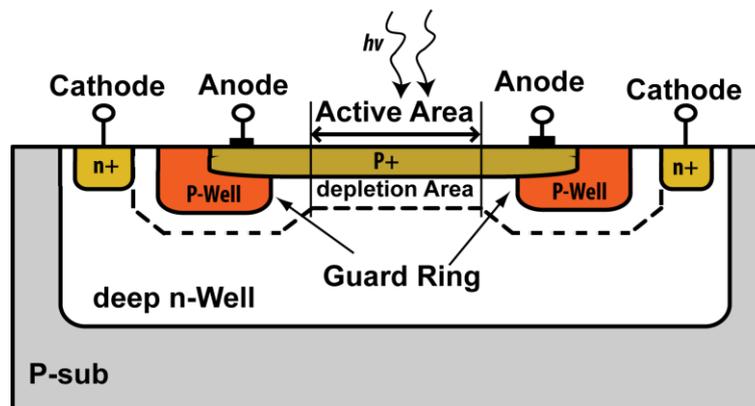
In chapter four, a charge pump which consists of 5 cells was designed and tested. The 5-cell charge pump was able to deliver 95.5 V into a 10 M $\Omega$  load. As we have seen in the previous section this charge pump can be broken down to smaller sections and therefore used to produce lower voltages. According to experimental results in **section 4.2.3**, one single cell (shown in **Figure 4.15**) of this charge pump can produce a maximum of 20.4 V. In order to reach the required 25 V another cell is needed. Thus it was decided to

use two cells as shown in the block diagram in **Figure 6.10**. The charge pump capacitors are located off-chip to allow SPAD drive current to be readily adjusted through component value changes.

### 6.3.2 Passive quenched SPAD

Adjacent to the charge pump on the chip is an SPAD with passive quenching circuitry. The SPAD is the part of the ASIC that has been designed by the group from the University of Oxford and is a diffused guard ring SPAD in a CMOS process. As the CMOS process is a planar fabrication process, a pn junction has small curvature around its edges which results in higher electrical field at the edges of the pn junction than the main active area. As a result, in high electrical fields near to avalanche breakdown, the edges will breakdown at lower voltages than the main area. To avoid this premature breakdown, a guard ring of a lower doped material, the same as the anode, is diffused around the edges of the active area. The lower doped material will reduce the electrical field at the edges hence preventing premature breakdown. Similarly, as the typical layout of a pn junction is rectangular, higher electrical fields occur in the corners. In order to avoid these high electrical in the corners, the SPAD has a circular layout creating a smooth edge hence generating a uniform electrical field across the active area ( **Figure 6.11**).

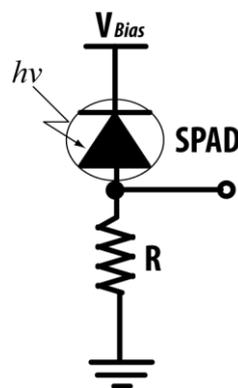
**Figure title: SPAD cross section**



**Figure 6.11** A cross section through the centre of a circular SPAD showing the guard ring of low doped material used to reduce the electric field at the edges and corners. The active area is 10µm diameter, and the overall SPAD area including guarding is 30µm diameter.

As was explained in **section 3.3.3**, in order for the SPAD to be capable of acting as a photon counter, a quenching circuit has to be used. In this ASIC simple passive quenching is adequate for steady-state autofluorescence detection. Therefore, a resistor can be used for this purpose. This resistor could be placed on either the anode or cathode side of the SPAD. Similarly, the sensing node of the SPAD could be on the either side of the SPAD [62]. However, SPADs fabricated in planar technology are not symmetrical (the cathode terminal presents higher parasitic capacitance than the anode terminal of the device) [62]. Thus placing the resistor at the cathode terminal increases the recovery time of the SPAD,s pulses. Furthermore, the generated pulses which are sensed at the cathode terminal will be alternating between  $V_{Bias}$  (i.e. 22 V) and the break down voltage (i.e 19 V). In this case, in order for the generated pulses to be processed by following circuitry, the pulses have to be shifted down to operate between 0 and  $V_{DD}$ . It is therefore more convenient to connect the quenching resistor to anode side. In this case, the resistor is used for two tasks: the first one, the resistor is used for the quenching process. The second task of the resistor is to be used as a current-voltage converter as shown in **Figure 6.12**. Unlike the MPPC which has a very large terminal capacitance ( 37 pF) for the 100 pixel, a single pixel silicon SPAD can have a very small diode capacitance  $C_d$  as low as 200 fF [62]. Small  $C_d$  accompanied by large avalanche current which can go as high as 1 mA makes a small resistor such as (10 k $\Omega$ ) adequate to produce a 1 V voltage pulse. A simple I-V converter can have a bandwidth of  $1/(2\pi RC_d)$  equal to 79.6 MHz. Therefore, unlike the MPPC with the single pixel SPAD there is no need for a Transimpedance amplifier to convert the SPAD anode current to voltage.

**Figure title: Simple I-V converter**



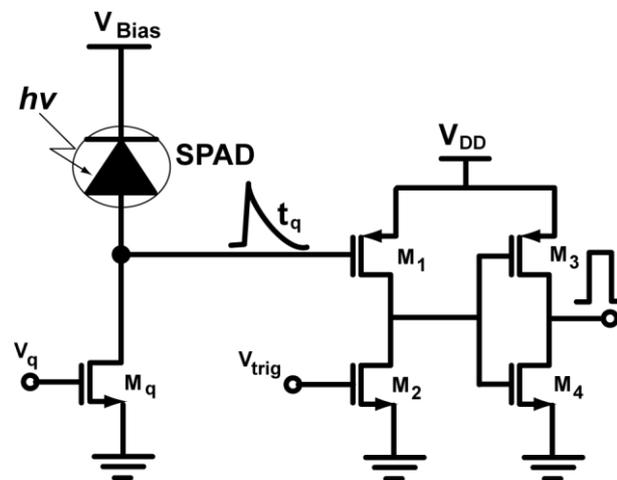
**Figure 6.12 I-V converter that uses resistor to convert the generated current pulses by the SPAD to voltage pulses.**

The quenching resistor can be external or integrated. If an external resistor is used to quench the SPAD, the parasitic capacitance  $C_s$  in parallel with the SPAD's diode capacitance  $C_d$  can be large [119]. The parasitic capacitance has a significant impact on the SPAD operating as  $C_s$  is usually at least an order of magnitude larger than  $C_d$ . When the SPAD is in its idle mode,  $C_d$  is fully charged to the positive bias voltage  $V_{Bias}$ , and  $C_s$  is empty. When an avalanche occurs, in order to quench the SPAD, the anode voltage quickly rises to the excess voltage ( $V_{ex}$ ) hence discharging  $C_d$  to  $(V_{Bias}-V_{ex})$ . This voltage rise will cause  $C_s$  to charge to  $V_{ex}$ , forcing a current through the SPAD. As more electrons flow through the high field region, the probability of trapping high-energy electrons and re-triggering the avalanche will significantly increase. As a result, after-pulses may occur. If the charging current of  $C_s$  is too high and recovery time is too fast, the SPAD may never quench, and a sustained avalanche current will flow through the SPAD. Moreover, as  $C_s$  is much larger than  $C_d$ , the total charge transferred during the quenching and recovery process is equal to

$$Q = (C_d + C_s) \times V_{ex} \quad 6.1$$

where the total capacitance is mostly dominated by  $C_s$ . Therefore, in order to reduce excess power consumption, an internal on-chip quenching circuit is implemented. An integrated quenching resistor can result in a very small parasitic capacitance  $C_s$ , even down to 70fF as reported in [120].

**Figure title: Passive quenching circuit**



**Figure 6.13 Schematic circuit diagram of the Passive quenching circuit.**

Base on the previous discussion, the quenching resistor was decided to be integrated and to be placed at the anode terminal of the SPAD. **Figure 6.13** shows the schematic of the implemented quenching circuit. In this circuit instead of a resistor, an NMOS device  $M_q$ , which is a voltage controlled current source that is used to limit the recharging current hence controlling the speed of the recovery by the means of varying the value of (q Bias). The recovery time is set long enough to ensure that the SPAD is quenched and to minimize the after pulses. The shape of the pulse at the sensing node of the SPAD is similar to a triangular shape due to the very sharp avalanche pulse and the linear discharge by the NMOS device. In order to read out this voltage without interfering with SPAD operation, a high-impedance CMOS buffer with variable threshold level is implemented. This buffer is a two-stage inverter which the first stage is CMOS variable threshold inverting comparator consisting of  $M_1$  and  $M_2$ . The  $V_{trig}$  input to  $M_2$  controls the trigger voltage. The second stage is a CMOS push pull inverter ( $M_3$  and  $M_4$ ) with sufficient current gain to drive the transmission wire and the next stage is a digital output buffer which drives the pad capacitance and the input capacitance of the pulse counter. Although the output buffers consume large amount of power, they are not required if the next stage after the quenching circuit is implanted on the chip.

As each SPADs pulse consumes a fixed amount charge given by equation (6). The SPAD total power consumption is then can be given by

$$P = V_A \times (C_d + C_T) \times V_{ex} \times f \quad (7)$$

where,  $V_A$  is the high positive bias voltage and  $f$  is the count rate per second. Note that  $P$  does not depend on the speed of the recovery unless the count rate changes. In the our present case where steady-state fluorescence measurement is intended, it can be noted that current consumption of the SPAD and therefore the current to be drawn from the charge pump is heavily dependent on the count rate of detected pulses and the dark count rate of the SPAD.

As not all the incident photons will generate a pulse, the ratio of the detected pulses to the incident photons are referred to as Photon Detection Probability (PDP). In the photo detection process, some photons are not absorbed, or if they are absorbed, they do not trigger an avalanche. PDP is product of Quantum Efficiency (QE) of the p-n junction and

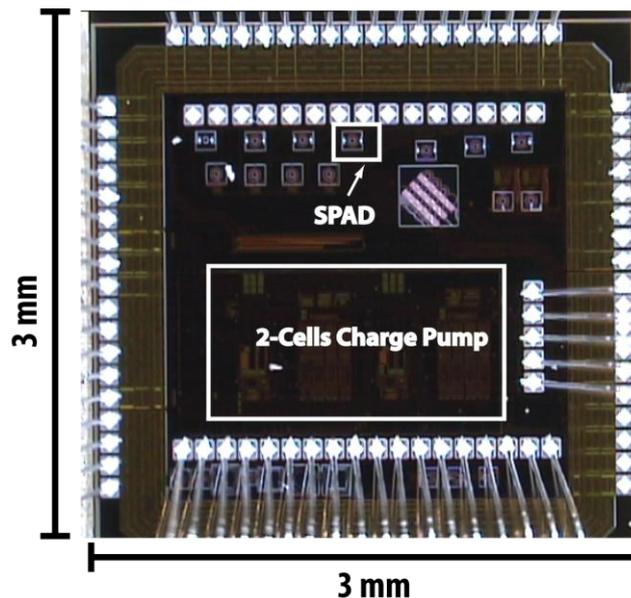
avalanche probability. In the shallow junction CMOS process due to the low depth of the depletion region from the surface of the silicon, the resulting PDE is expected to be higher in shorter wavelengths of the spectrum close to the blue-green region. This characteristic make the CMOS SPAD more suitable for applications such as blue-green fluorescence detection due to the lower cost and availability of the CMOS SPAD compared with SPADs fabricated in dedicated processes.

The SPAD with its circuitry was laid out next to the charge pump. As was the case with the charge pump, all the transistors used in the SPAD circuitry design were isolated transistors, namely NMOSI for MOS transistors and PMOSI for PMOS transistors. The use of isolated transistors gives the SPAD and its circuitry extra immunity against any leakages current injected by the charge pump to the substrate as we have mentioned earlier.

#### 6.4 Measurements

A micrograph of the fabricated ASIC is shown in **Figure 6.14**. The silicon area occupied by the charge pump is  $800\mu\text{m} \times 1570\mu\text{m}$ . Where, the SPAD with its circuitry occupies an area of  $45\mu\text{m} \times 45\mu\text{m}$ . The SPAD and charge pump were evaluated separately and in combination.

**Figure title: Fabricated ASIC**



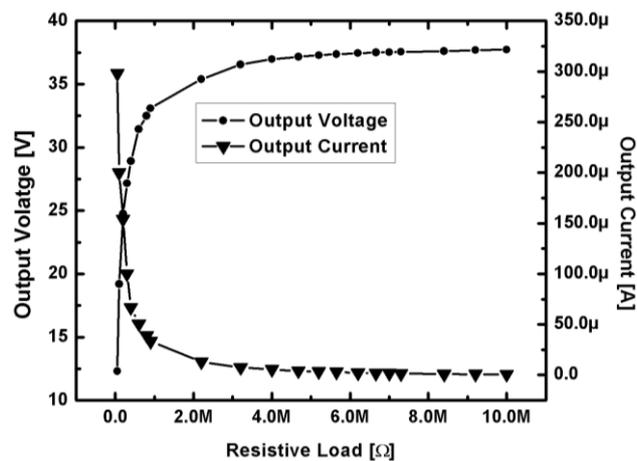
**Figure 6.14** Photograph of the  $3 \times 3 \text{ mm}^2$  application specific integrated circuit chip.

### 6.4.1 Charge pump characterisation

According to measurements, the 2-cell high voltage charge pump is capable of generating up to 37.9 V. At 10 M $\Omega$  resistive load  $R_L$ , 10nF  $R_L$  and 1.430 kHz clock frequency, the charge pump showed minimum ripple of 34 mV, rise time of 19 ms and can deliver 700 nA output current. The overall characterisation of the charge pump voltage generation capability alongside its current drive capability was tested by sweeping  $R_L$  from 10 M $\Omega$  to 50 k $\Omega$ . **Figure 6.15** shows the output current and voltage in response to varying resistive load and the effect of the resistive load on the generated voltage and the delivered current to the output load. At low resistive load value (50 k $\Omega$ ), the charge pump generates only 12.3 V whilst delivering a relatively high current of 298  $\mu$ A. The measured relation between the delivered current and the output voltage of the charge pump can be used to estimate the source impedance ( $R_s$ ) of the charge pump which is according to **Figure 6.16** can be given by

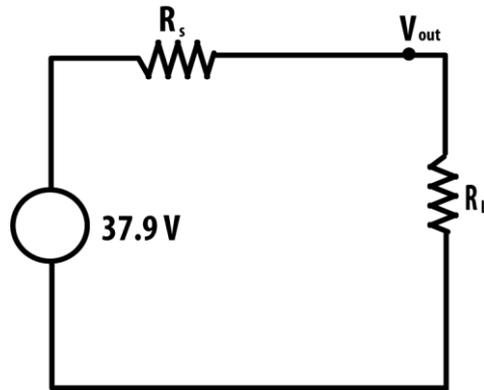
$$R_s = \frac{37.9 \times R_L}{V_{out}} - R_L \quad (8)$$

**Figure title: Current and voltage characteristics of the charge pump**



**Figure 6.15 Measured current driveability and voltage capability of the charge pump as function of resistive load  $R_L$ .**

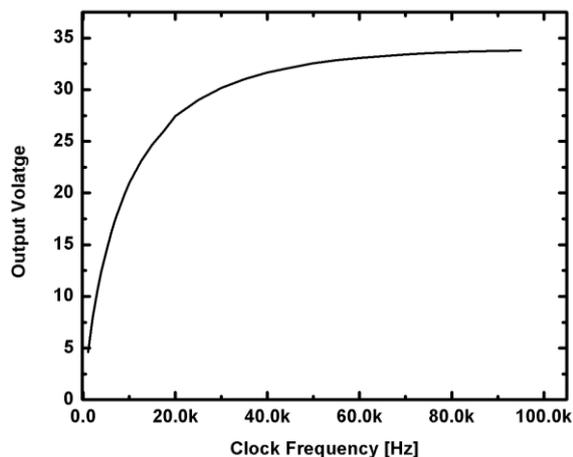
**Figure title: Charge pump equivalent circuit**



**Figure 6.16 Two cells charge pump equivalent circuit**

The variation of output voltage with input clock frequency is shown in **Figure 6.17**. At  $0.9\text{ M}\Omega$  load the maximum output voltage is equal to  $33.2\text{V}$  for a  $95\text{ kHz}$  clock. This curve changes according to the output resistive load value and the clock frequency. Hence the output voltage can be set for a known resistive load value by appropriate adjustment of clock frequency as will be seen in section 6.4.3. This is very important as the SPAD must be biased correctly for optimum photon detection efficiency.

**Figure title: Charge pump output voltage**

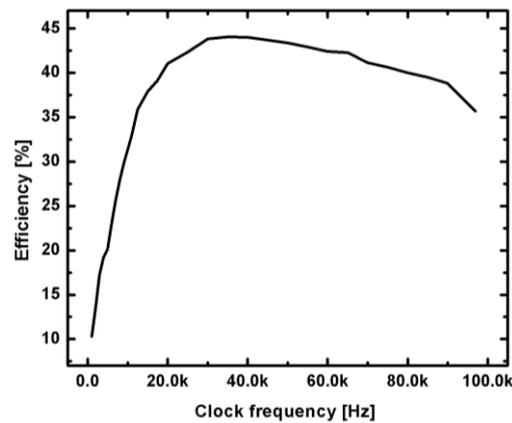


**Figure 6.17 Measured output voltage of the charge pump as function of the clock frequency at resistive load equal to  $0.9\text{ M}\Omega$ .**

The efficiency of the charge pump was measured with respect to frequency. The power efficiency of the charge pump is calculated by dividing the mean value of the output power

by the mean value of the input power consumed by the charge pump [73]. **Figure 6.18** shows, the efficiency with a to 0.9 M $\Omega$  resistive load. The reason that the results in **Figure 6.17** and **Figure 6.18** were obtained at 0.9 M $\Omega$  load is because at this load value, the SPAD showed its best response as we will see in **section 6.4.3** of this section. At this load the charge pump's power efficiency peak is 40.1% for a clock frequency of 35 kHz. (**Figure 6.18**), this mean that at this load the charge pump achieves its highest efficiency when generating 31.6 V.

**Figure title: Charge pump efficiency**



**Figure 6.18 Measured efficiency of the charge pump against clock frequency at resistive load equal to 0.9 M $\Omega$ .**

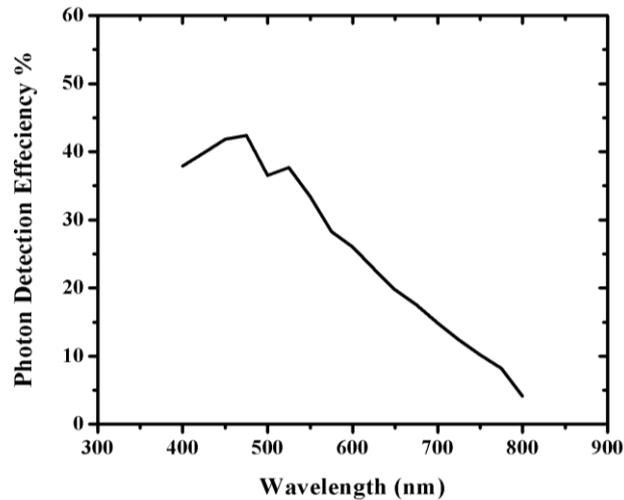
#### 6.4.2 SPAD characterisation

The SPAD was tested independently. The SPAD experienced breakdown at 18.95 V. When biased with excess voltage  $v_{ex}$  equal to 3.1 V over and above the breakdown voltage, the dark count rate (DCR) of the SPAD measures about 4 kilocounts/sec (kcps).

At the same excess voltage the power detection efficiency (PDE) of the SPAD was measured using a white light source attached to an integrating sphere to create a uniform illumination at the exit port of the sphere, where a monochromator was placed to sweep the light wavelength from 400nm to 800nm. The SPAD was placed at the exact centre of the monochromator exit port in order to investigate the count rate against wavelength. Due to the non-uniform spectral distribution of the grating used in the monochromator, the obtained results were then remapped against the spectral response measurement obtained

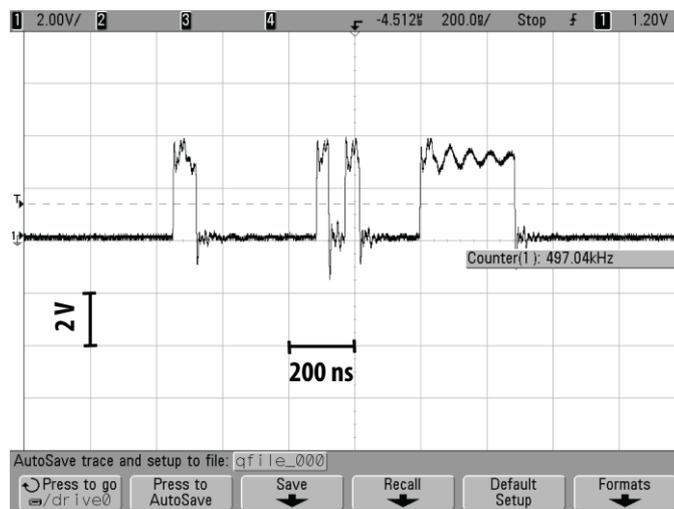
from an off-shelf BX65 photo-diode. The SPAD's PDE shows that it has about 42.4% detection efficiency at 475 nm and 36.6% at 500nm (**Figure 6.19**).

**Figure title: Photon detection efficiency**



**Figure 6.19** Photon detection efficiency of the SPAD peaks at 475nm which is suitable for detection of autofluorescence emission that lies at the end of the blue region and towards the green region.

**Figure title: Output pulses**



**Figure 6.20** The response of a SPAD at the output of the second buffer to moderate light illumination shown on a screen shot of an oscilloscope.

The operation of the SPAD's circuitry including the buffers has been tested as well. The optimum response of the SPAD is achieved when current-sink transistor  $M_q$  is biased at 1.24 V and  $V_{trig}$  is set at 0.95 V. Biasing  $M_q$  at 1.24 V produces a long enough recovery time to ensure that the SPAD is quenched properly and therefore the after pulse effect is low. However setting  $M_q$ 's bias, and the resulting SPAD bias current, too high increases the pulse widths and consequently minimizes the input dynamic range of the SPAD. **Figure 6.20** shows an example of the SPAD pulses generated at the second buffer which contains some narrow pulses and a wide pulse. The square narrow pulses are due to single avalanche pulses. Whereas, the wide square pulse are caused by an avalanche pulse with some after pulsing.

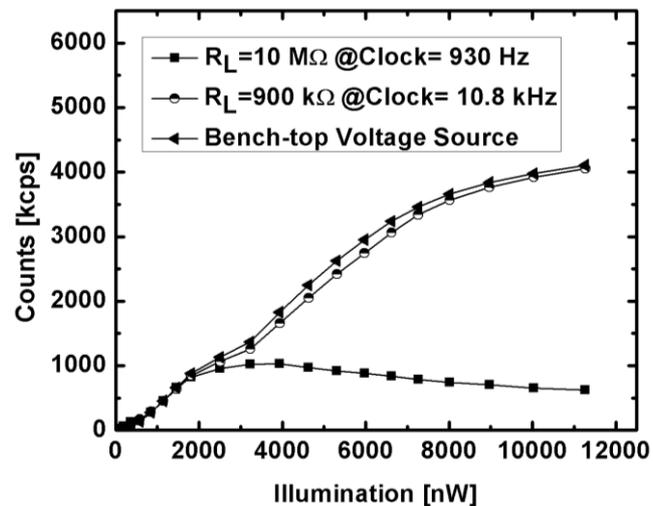
At 3.1 V excess voltage, the threshold voltage of the first buffer at  $V_{trig}$  is set to 0.95 V where the highest pulse count dynamic range is achieved. At high illumination the SPAD can reach up to 4108 kcps which is the highest pulse rate that can be achieved while maintaining relatively low after pulsing. In this work where steady state fluorescence measurement is intended, it is very important to have a wide dynamic range. The transient spectrum of the SPAD should be able to accommodate the DCR, useful pulses count rate (i.e detected autofluorescence emission) and count rates generated from background scattering light originating for the excitation source.

### 6.4.3 ASIC evaluation

The response of the SPAD to various light intensities has been tested when it is biased either from a regulated bench-top power supply or from the charge pump when loaded at different resistive values. The response has been measured using a green LED, with a peak wavelength of 570nm and FWHM (Full Width Half Maximum) of 25nm installed at the entrance port of an integrating sphere to provide uniform illumination at the exit port. The relationship between the voltage applied to the LED and the intensity of the light at the exit port was then determined using an Anritsu optical power meter. The SPAD was first biased using the charge pump at 22 V and clock frequency equal to 10.922kHz. The SPAD response was then measured against varying light intensity. An ideal photon detector's photon counts per second output should be proportional to the light intensity, however this is not the case for the SPAD as when the charge pump is loaded by a high resistance (i.e 10 M $\Omega$ ). This is attributed to the fact that the charge pump is delivering only about 360 nA to the load. At very low intensity the SPAD demands very low current for each pulse generated, however when the light intensity is increased more pulses are generated and

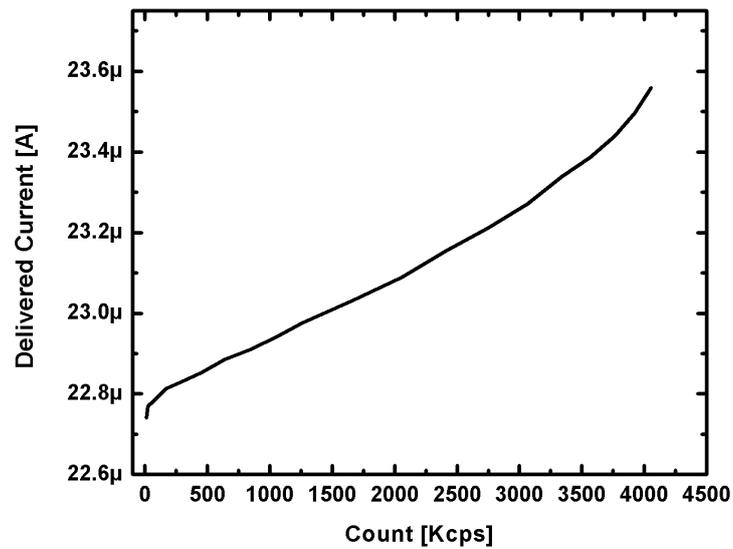
therefore more current is drawn from the charge pump. The charge pump then starts to respond to the high current demands from the SPAD by reducing some of its voltage potential generated at the output. As a result of this, the photon detection efficiency of the SPAD is greatly diminished. This effect is irrelevant when a bench top power supply is used but it is critical the SPAD is biased by a charge pump. Two solutions can be suggested to overcome this problem by: 1) introducing a feedback control unit that senses any drop at the output of the charge pump below the 22 V and then responding by increasing a clock frequency of the charge pump. 2) By directly increasing the amount of current delivered to the output from nano amp scale to several tens of micro amps. The large amount of current ensures that any change in current demand by the SPAD will not cause any significant drop in the excess voltage and therefore maintains the SPAD biased point. Increasing the delivered current to the output node of the charge pump is achieved adding an additional resistive load in parallel with the SPAD -  $R_{\text{regulation}}$  - in order to regulate the delivered output current. According to measurement in **Figure 6.21** this can be achieved by using  $R_{\text{regulation}}$  of 0.9 M $\Omega$ . At this load the SPAD shows a similar response when biased from a bench-top power supply or from the charge pump.

**Figure title: SPAD response at different regulation loads**



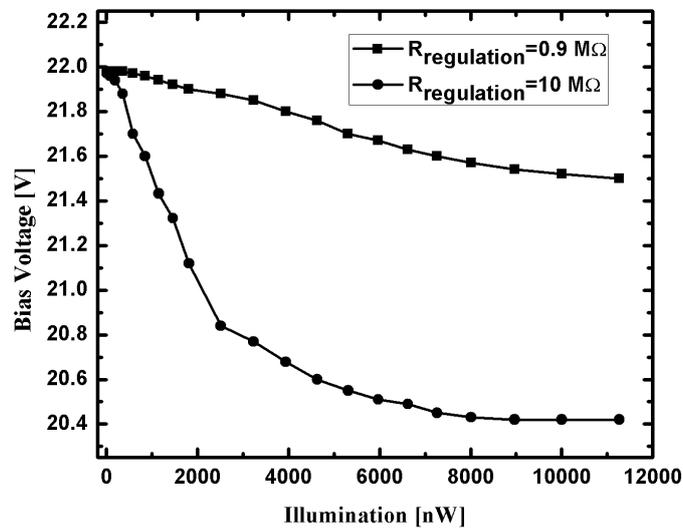
**Figure 6.21** The count rate of the SPAD versus illumination power when biased by the charge pump at different resistive loads values and when biased by a bench-top voltage source. The excess voltage at low light levels for all sets of data is 2.7 V.

**Figure title: Delivered current by the charge pump**



**Figure 6.22 Delivered current by the charge pump as function of light illumination with  $R_{\text{regulation}} = 900 \text{ k}\Omega$ .**

**Figure title: Bias voltage response to illumination**



**Figure 6.23 The bias voltage decreases when illumination intensity is increased by biasing the SPAD with the charge pump. This decrease is changes according to the regulation load used for the charge pump.**

In contrast with the first solution, the second option is very simple to implement. However, in terms of power consumption (and ignoring the power consumption of the feedback

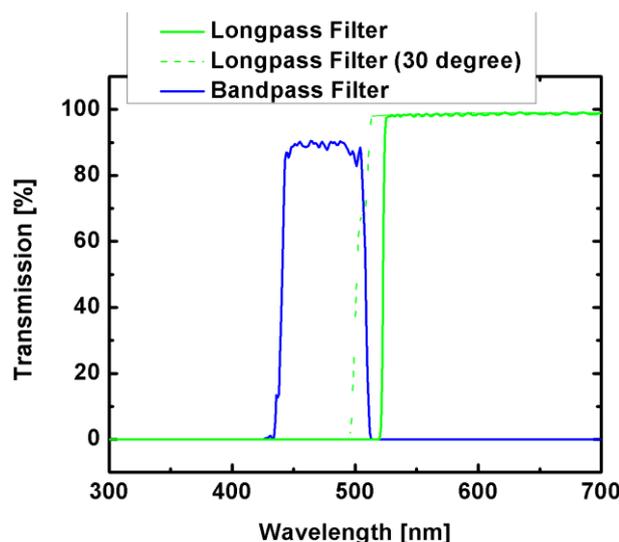
circuit if implemented), using a  $0.9\text{ M}\Omega$   $R_{\text{regulation}}$  increases the current consumption of the charge pump from  $152\ \mu\text{A}$  to  $487\ \mu\text{A}$ . **Figure 6.22** shows the amount of current being delivered to the charge pump when  $0.9\text{ M}\Omega$   $R_{\text{regulation}}$  is used. The actual amount of current that flows through the SPAD changes from  $70\ \text{nA}$  at  $500\ \text{keps}$  to around  $680\ \text{nA}$  at  $4108\ \text{keps}$ . The effect of this change on the bias voltage generated by the charge pump is shown in **Figure 6.23**. It can be seen for this figure that the charge pump can sustain almost  $21.5\ \text{V}$  at high illumination when  $0.9\text{ M}\Omega$   $R_{\text{regulation}}$  is used. However, when higher  $R_{\text{regulation}}$  is used (i.e  $10\text{ M}\Omega$ ) is used, the charge pump voltage output drops from  $22\ \text{V}$  with no illumination to  $20.42\ \text{V}$  at illumination power equal to  $11.27\ \mu\text{W}$ .

## 6.5 Biological measurements

Having evaluated the ASIC performance electrically and optically, in this section the ASIC's ability to measure autofluorescence emitted from living tissues is verified. This measurement was conducted in a small dark room measuring  $80\text{cm}\times 50\text{cm}\times 50\text{cm}$  which isolated the system from ambient light. The ASIC was integrated into a test PCB, placed in the middle of the dark room and aligned next to a blue excitation source. All the evolution experiments in this section were conducted with the SPAD biased by the charge pump and at  $22\ \text{V}$ ,  $0.9\text{ M}\Omega$   $R_{\text{regulation}}$  and  $10.922\text{kHz}$  clock frequency.

It is common for autofluorescence measurements to use white light followed by multi-band optical filters in order to scan the region between  $425\pm 52\text{nm}$  [6, 9, 32]. However, due to capsule size and power constraints a blue LED is used instead. Choice of LED excitation wavelength was based on the findings in [8, 29] which describe the endogenous tissue fluorophores that can be found in human tissues in the upper part of the GI tract. However, as far as we are aware, there is no dedicated study that focuses on finding the exact endogenous fluorophores of the small intestine. Therefore, it was assumed that the GI tract contains more or less the same endogenous tissue fluorophores. By comparing the excitation wave lengths of the endogenous fluorophores and the excitation bands that were used in [6, 9, 32], it can be said that the later studies were targeting mainly Flavins fluorophores which has a peak excitation wave length at  $450\text{nm}$  [8, 29]. Accordingly, the Avago Technologies HSMR-CL25 LED was used as an excitation source. The LED is an 0603-size surface mount device with a peak wavelength of  $465\ \text{nm}$  and (Full Width Half Maximum) FWHM of  $25\text{nm}$ .

**Figure title: Filters characteristics**



**Figure 6.24** The long pass filter has a cut-off wavelength at 515 nm and the band pass filter has a centre wavelength equal to 475nm and FWHM bandwidth equal to 64nm.

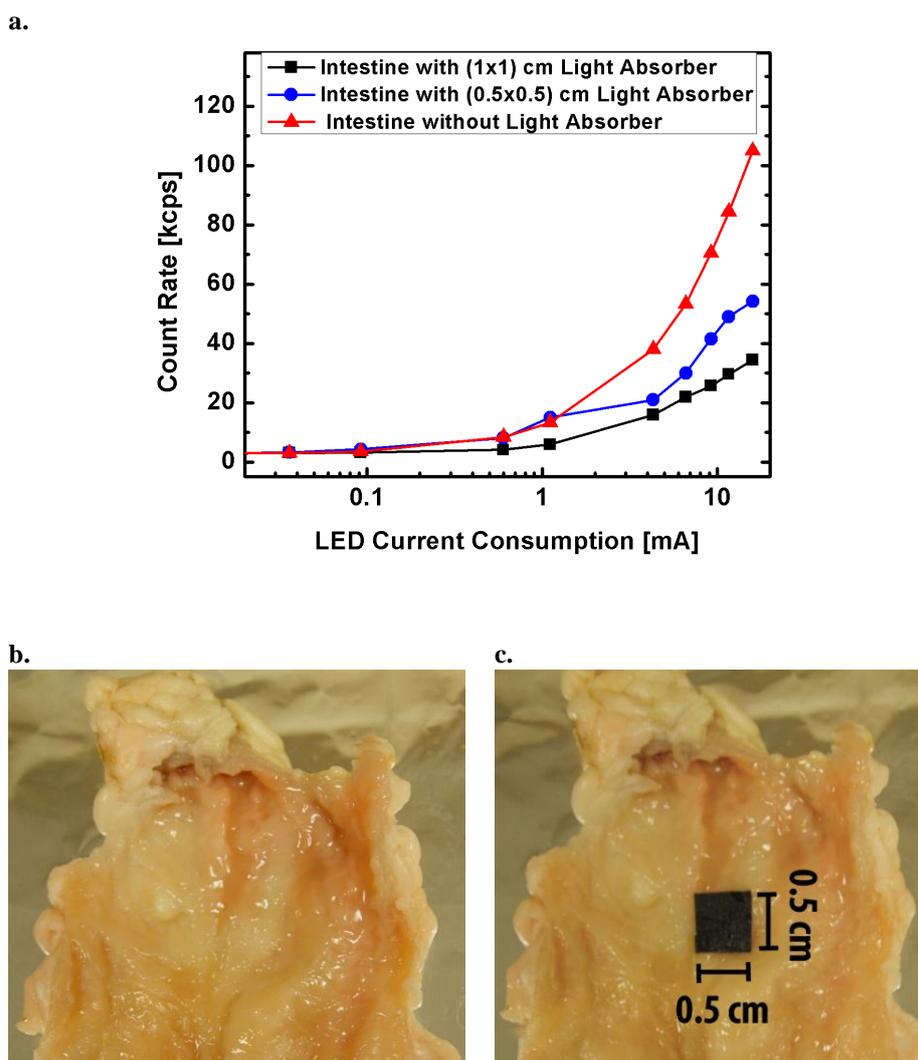
When Flavins fluorophores are excited at 450 nm, they fluoresce at 520nm [8, 29]. Based on this fact, a 4mm x 4mm width, 3.5 mm thickness Semrock long pass filter was placed on top of the SPAD in order to isolate the SPAD for the emission of the excitation source. As the excitation and emission bands are close, a 3mm x 3mm with 3 mm thickness Semrock band pass filter was also used on top of the LED. This filter which has very high optical density (OD) (greater than -7) strongly attenuates the LED's output above 507 nm. The spectrum characteristics of the two optical filters are shown in **Figure 6.24**. The cut-off wavelength of the two filters was chosen to be close to each other to allow as much as possible for a wider excitation band and wider detection band.

In complete darkness, the SPAD generated DRC of~ 4 kcps which is measured using the counter function available in the MSO6104A Agilent oscilloscope. However, when the excitation source is powered on, the SPAD detects photons that are originating from the excitation source with a correspondent count rate reaching up to 8.7 kcps when the LED is biased at 3 V. Count rate increases if a reflective object such as aluminium foil sheet is placed 2cm away from the SPAD in which case it rises up to 23 kcps. Clearly the SPAD optical filter fails to completely attenuate the proportion of photons from the LED which are reflected back from the intestinal wall. This is because the OD of these filters is still not high enough to completely block the blue light and the fact that the cut-offs of the two

filters are close to each other which causes interference between the filters. For incident light at 0 degrees these filters behave according to their measured characteristics and no interference between them is occurring. However, in the case of reflected light having different angles, the cut-off edge of the filter changes accordingly as shown in **Figure 6.24**. It can be seen that when the light angle changes to 30 degree the cut-off wave length moves to lower wave lengths  $<500\text{nm}$  which therefore causes an interference between excitation band and detection band. Minimizing the count rate of the background light can be achieved by: 1) increasing the OD of the band pass filter. 2) using a polarizer on top of the two filters [121]. However, filters with higher OD are too large to fit within the pill. The same can be said about the second option. There is not enough space to add a polarizer. Furthermore, a polarizer will reduce the amount of detected blue light as well as the amount of detected autofluorescence emission. Accordingly it was then decided to deal with any scattered background light as an additive dark count. The measurement conducted using aluminium foil, indicated that the maximum dark count rate is 27 kcps. Therefore, any count readings above this level is considered as autofluorescence emission.

Autofluorescence measurements have been carried out using a piece of lamb small intestine placed 2cm from the SPAD. The intensity of the autofluorescence emission was measured at different excitation blue light intensities (**Figure 6.24.a**). This measurement was first conducted with plain intestine (**Figure 6.24.b**), where its internal side is placed facing the SPAD. The measured autofluorescence count is equal to 53.3 kcps when LED is biased at 3 V (6.6 mA). In order to mimic a cancerous region, a piece of an absorbent optical tape was placed right at the region facing the SPAD. This material mimics a tumour formation in that it absorbs much of the excitation light and emits very weak autofluorescence according to stage and the size of the tumour. The tumour exhibits increased blood flow and correspondingly higher haemoglobin levels. Haemoglobin absorbs incoming photons which will result in substantially reduced autofluorescence which is a characteristic feature of a tumour [122]. When an 0.5cm x 0.5 cm piece of absorbent tape, as shown in **Figure 6.24.c** was used, the SPAD output fell to 30 kcps, and dropped to 21.9 kcps when 1cm x 1cm absorbent tape is used. These results verify that the system is capable of effectively inducing and detecting autofluorescence in mammalian intestinal tissue in spite of the additive noise of dark count and reflection. It can be seen from **Figure 6.24.a** that the difference between autofluorescence measurements diverges as the excitation intensity is increased, hence the higher the excitation intensity the more accuracy is obtained in distinguishing between healthy tissues and non-healthy tissues. However, this issue is a trade-off with the effect of background scattering light. It is thus

**Figure title: Autofluorescence from mammalian tissues**



**Figure 6.25 (a) Autofluorescence emission intensities at different excitation levels. The autofluorescence is measured for a piece of plain lamb intestine as in (b) and for the intestine with light absorbing black-out material as in (c).**

important to note that eliminating the background scattering light effect will allow more accurate readings to take place at lower illumination and therefore reduce the LED power consumption.

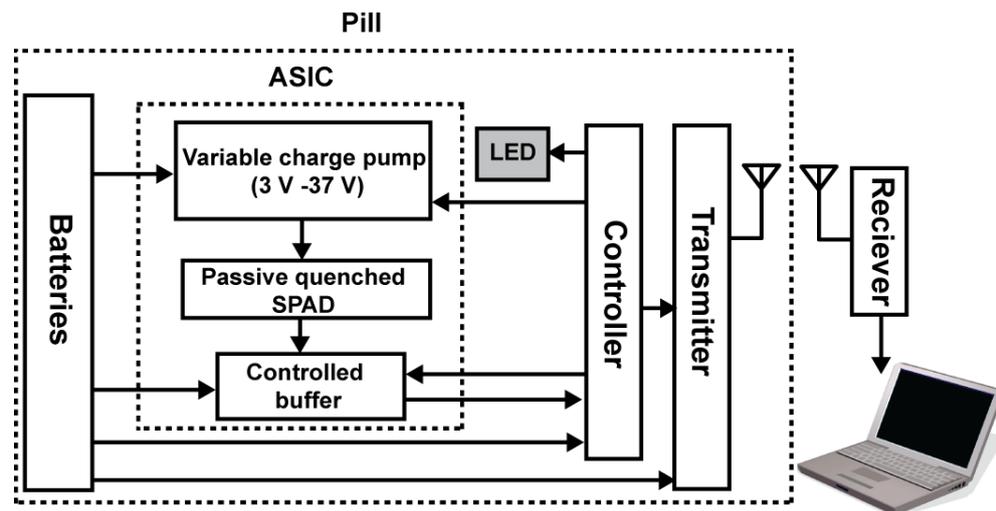
The LED is the main power consumer within the capsule At 3 V which is the highest voltage that can be supplied to the LED using two 1.5 V SR48 battery cells, the LED consumes 19.8 mW, corresponds to 6.6 mA as shown in figure 14.c. In the other hand the ASIC only consumes 1.76 mW, corresponds to 487 $\mu$ A by the charge pump and 85 $\mu$ A by

the SPAD's buffers. The controller and radio link discussed below combined consume an average of 50  $\mu\text{A}$  at 3 V.

## 6.6 Controller & Radio link

After ASIC fabrication and testing the final system was assembled and tested. **Figure 6.26** shows the complete block diagram of the system which consists of a battery pack, ASIC, LED, control unit, radio link and data logging software. The system operates as follows: When the SPAD is biased above its breakdown voltage by the charge pump, it generates pulses that are proportional to the number of detected light photons, these pulses being counted over a fixed period by an off chip counter. An off chip state machine and timer controls the operation of the charge pump, LED and the transmitter. On completion of pulse counting the counter value is transmitted via UHF radio to the external receiver and data logger. This operation is repeated every second until the entire intestine is scanned. At the receiving end, the gathered data is graphed against the travelling time of the capsule.

**Figure title: System block diagram**

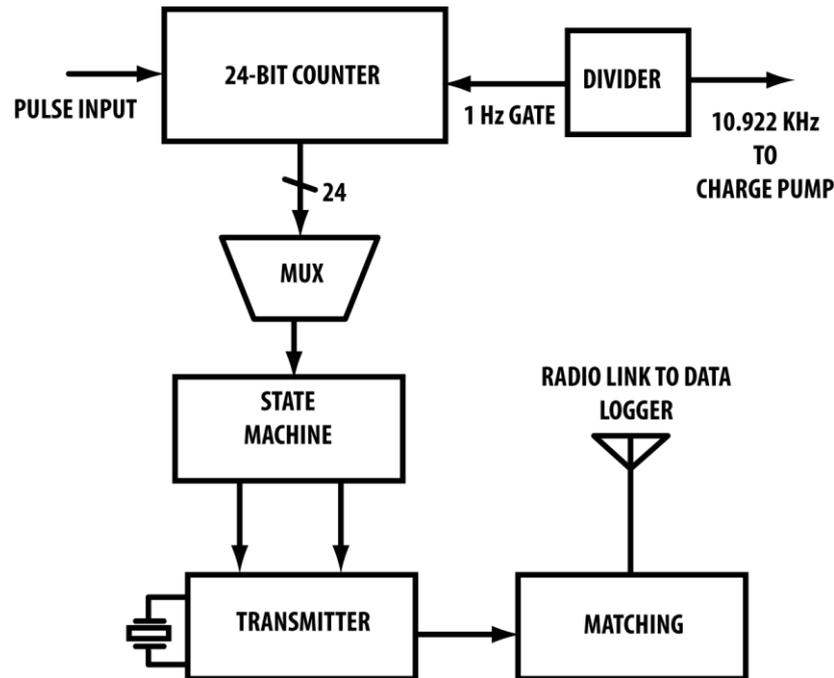


**Figure 6.26 Complete system block diagram illustrating the components of the pill and the radio link to the external base station.**

The radio link, controller and data logger was designed and fabricated by the School of Engineering, Microsystems technology group member, Dr. James Beeley. The design includes a pulse counter which counts pulses generated by the SPAD, controls data

transmission via radio to the external data logger and provides a clock for the SPAD (**Figure 27**). The controller was designed to provide the charge pump with the required clock frequency (10.922 kHz), count incoming pulses for the SPAD (up to 16 Mcps) and control the transmitter part of the pill. The transmitter was designed to send the information acquired by the counter to an external data logger within 1 meter radius.

**Figure title: System block diagram**



**Figure 6.27 Pulse Counter and UHF Data Link.** The counter counts pulses over a 500ms period. The counter value is then read serially by a state machine, which transmits the counter value to an external logger via an 868 MHz ASK transmitter. A divider generates counter gate control and charge pump clock signals.

Incoming pulses from the SPAD increment a 24-bit counter which rolls over to zero on reaching its maximum value of  $2^{24}-1$ . The counter input gate opens for 500ms in every second, the high portion of a 1 Hz 50% duty-cycle clock is used as the counter gate signal. At the end of the sampling period a control state machine activates an 868 MHz amplitude-shift keyed (ASK) radio transmitter. The 24-bit counter value is transmitted serially and asynchronously over the radio link at 32.768 kbaud, and is enclosed by 2 start and 1 stop bits to form a 27-bit data packet. The transmitter requires 1 ms stabilisation time after being powered on, and 823 $\mu$ s to transmit the 27 data bits, and hence is active for only 1.823 ms in every second, thus minimising power use. A UHF receiver passes the

incoming data packet to a microcontroller, in turn transferring the counter value to a PC via USB. PC software uses the two most recent count values to calculate and log the pulse rate per second. As the 24-bit counter gate is open for 500 ms in every second the maximum measurable frequency is 33.5 MHz, and resolution is 2 Hz.

To verify the pill implantation feasibility, an off-the shelf ICs for: counter, controller and transmitter were used. A Xilinx XC2C64 Coolrunner II Complex Programmable Logic Device (CPLD) with 3V I/O and 1.8V core implements the 24-bit counter, the 24-to-1 multiplexer used to read the counter value serially, the control state machine. The CPLD offers far lower power consumption than a Field-Programmable Gate Array (FPGA), and offers far greater pulse counting resolution and precision than a microcontroller. Dividers generating a 10.922 kHz charge pump control clock and a 1 Hz, 50% duty cycle counter gate control signal from the 32.768 kHz system clock are also implemented in this device. The design was specified in VHDL and synthesised and simulated via Xilinx ISE Webpack software. The 6 mm x 6 mm BGA-packaged device was the largest able to fit within the capsule, significant effort being required to fit the required functionality into the 64-macrocell device. The CPLD, 32.768 kHz oscillator and voltage regulator are attached to a 12mm diameter PCB. A tab on the side of the board with an appropriate connector permits in-circuit programming of the CPLD, and is cut off prior to assembly.

An 868.3 MHz radio frequency was selected, this being the only legally permissible frequency within the 450-900 MHz range which finite-element simulations have shown to be effective for radio transmission through the human body [123]. The 433 MHz band, whilst also legally permissible and used in some medical devices, was avoided as it falls outside the optimum range indicated by simulation work and carries a risk of transmission being disrupted by interference as this frequency is also extensively used by car central locking remote control systems and powerful amateur radio and military radio systems [124]. The Melexis TH72035 UHF transmitter IC is active for 1.8235 ms per second in which it generates a 1 mW, 868.3 MHz carrier frequency by multiplying the output of a 27.13438 MHz crystal oscillator via a phase-locked loop and amplifying the resulting signal. The carrier is amplitude-shift keyed - on in response to a logic "1" and off in response to a "0". The RF output drives an omnidirectional helical antenna (Linx JJB) via an LC impedance matching/harmonic suppression network. The ground layer of the 14mm-diameter transmitter PCB doubles as the antenna ground plane.

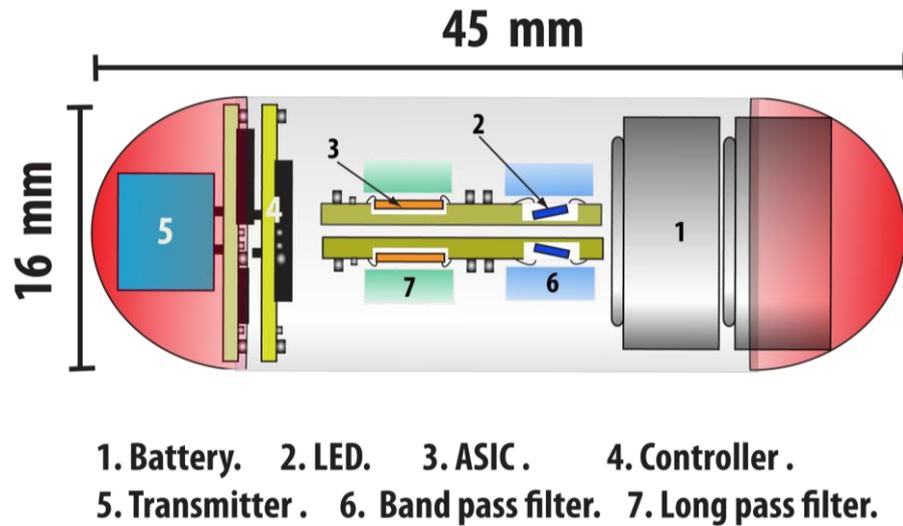
The external data logger's RF section is comprised of a Melexis TH71120 868 MHz receiver board and an end-fed dipole antenna. Incoming data packets from the receiver are fed serially into a Microchip PIC18F14K50 embedded processor. Manufacturers developers boards were used in both cases to minimise design time and cost. The PIC recognises an incoming packet's start-bit pattern and utilises the radio receiver's received signal strength indicator connected to an on-board analogue-digital converter to avoid false triggering on noise in the absence of a transmitted radio signal. PIC code was written in "C" using the MPLAB development system. The received counter value is then passed via USB link to a logging PC running Windows XP. The logging software displays the count value and stores it for later analysis, and communicates with the USB microcontroller via Microchip USB libraries and the LibUSB device driver. The PC software was written in Microsoft Visual C++ 2010.

The operation of the counter and the controller was tested and their operation was verified in conjunction with the ASIC. The implemented counter was able to count and incoming pulses from the SPAD as efficiently as the MSO6104A Agilent oscilloscope. The radio link's performance was also examined. The capsule, whose counter input was driven by a pulse signal generator, was placed against one side of the torso of one of the investigators, and the radio receiver against the other side in a variety of different positions and orientations. In all cases data was received reliably. This experiment was carried out in a radio frequency anechoic chamber, whose walls absorb RF energy and hence eliminate radio propagation by wall reflection. This suggests that the radio link operates reliably through human tissue regardless of the relative position of capsule and receiver and consequent antenna polarisation, and that the communication link would be capable of dependable operation from within a human.

## **6.7 Packaging**

The components that are incorporated into the capsule are arranged in **Figure 6.28**. the capsule is intended to contain two channels, each consisting of an ASIC and an excitation source (LED), such that the entire 360° surface of the intestinal wall is covered by the detection part and the excitation part where in each channel there is an In this work for demonstration purposes a single channel was implemented in a capsule.

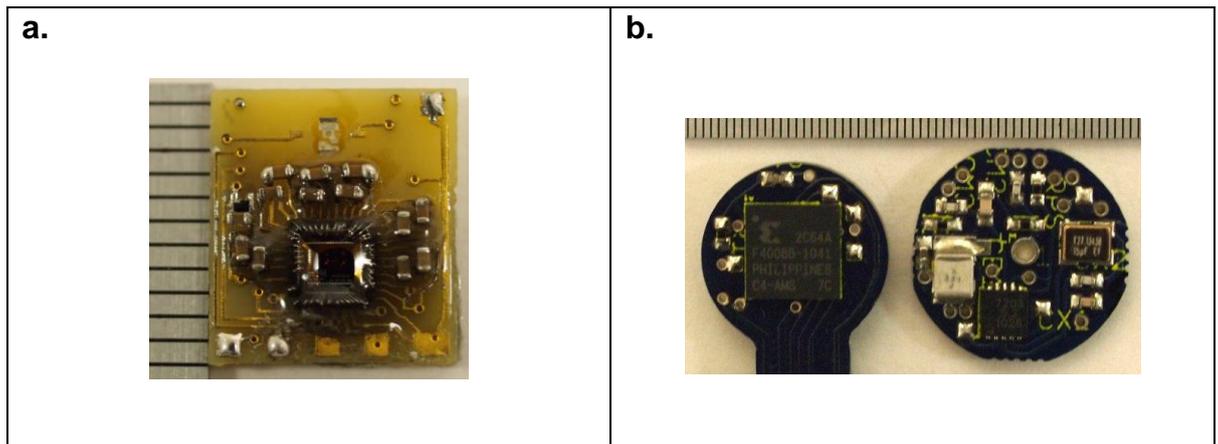
**Figure title: Pill design layout**



**Figure 6.28 Sketch of proposed pill illustration the arrangement of the pill components.**

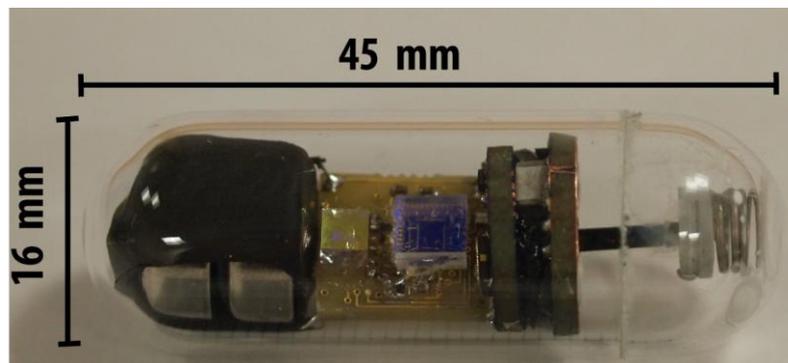
In order to demonstrate the size feasibility of the capsule, a tube made of borosilicate glass which has a visible light transmission  $>92\%$  was used to encase one channel of the system. The design used the following main components: 1) an 11 mm x10mm double-sided PCB board to host the ASIC, LED, optical filters and the charge pump's external capacitors (**Figure 6.29.a**) 2) a double-sided 12 mm diameter round PCB with implementing the counter and control unit and a double-sided 14 mm diameter round with that transmitter PCB (**Figure 6.29.b**). 3) 868 MHz radio transmitter and antenna 4) pack of two (SR48 battery cells). The final assembly of the prototype Pill is illustrated in **Figure 6.30**. The complete prototype was 16 x 45mm in size and weighted 12.01 g including the batteries.

**Figure title: Main PCB , controller and transmitter PCBs**



**Figure 6.29 . a) The 11 mm x10mm double-sided PCB containing the ASIC, LED, the optical filters and the charge pump's external capacitors (1 mm scale). b) The CPLD controller/counter/divider (left) and 868 MHz transmitter (right) boards, scale is 0.5 mm.**

**Figure title: Pill prototype**



**Figure 6.30 Final prototype packaging of the proposed pill. From left to right are the battery pack, LED and ASIC on a horizontal-mounted PCB, vertical controller and transmitter PCBs, and UHF antenna.**

## **6.8 Summary**

This chapter started with a feasibility study of integrating a SPAD with a charge pump into a single chip by testing a SPAD that was designed by The University of Oxford and a component of the charge pump that was discussed in chapter 4. A new ASIC was fabricated using AMS H35 process and contained the charge pump and the SPAD in the same chip. Electrical and optical evaluation measurements have been presented in section 6.4. The measurement section included measurements and evaluation of the SPAD, the charge pump and the two blocks when operating together. The SPAD has high detection efficiency in the green-blue region with a peak of 42.4% achieved at 475 nm and experienced breakdown at 18.95 V. When biased at 22 V the dark count rate of the SPAD measures about 4 kcps. The SPAD was biased at 22 V using the 2-cells charge pump which was regulated by a 0.9 M $\Omega$  resistive load at 10.922 KHz clock frequency in order to overcome the problem introduced by the high source impedance of the charge pump. The resistive load is used to regulate the current delivered to the SPAD and therefore helps the charge pump to sustain the 22 V at high illumination. In order to verify the capability of the ASIC to measure different levels of autofluorescence emissions, biological measurements were conducted using a lamb's small intestines. The measurement verified the operation principle of the system and showed that the fabricated ASIC can detect the changes in the level of the autofluorescence emission produced by the small intestine at different excitation intensities. In section 6.6, the control and radio link part of the capsule was designed, implemented and its operation with ASIC was verified. In the final section, all the implemented components that were designed to be incorporated into the capsules were fitted into a 16 x 45mm glass capsule to demonstrate the size viability.

# Chapter 7 Conclusion and future work

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## 7.1 Conclusion

In this work a prototype of a miniaturised, low-power pill sensor with integrated data transmission capable of detecting autofluorescence from mammalian small intestine tissue has been designed, implemented and characterized. The pill comprises an application specific integrated circuit (ASIC), implementing a single photon avalanche detector (SPAD) and a charge pump enabling the SPAD to operate from a 3V battery. The device also incorporates a digital pulse counter, controller, low power LED, optical filters and a radio transmitter. This offers the potential for automated early detection of cancer and other ailments of the small intestine.

Initial development of the pill used an off chip MPPC device as a light detector. The MPPC is an array of SPADs that has a photon detection efficiency of 60% at 520 nm. In order to operate the MPPC, an ASIC that contains a very high voltage charge pump and front-block was fabricated using the AMS high voltage 0.35 $\mu$ m process. The charge pump, which consists of 5-cells, was capable of delivering the 72 V with 70 $\mu$ A that is required to bias the MPPC. Each cell in the charge pump is constructed using two stages of a Dickson charge pump and a high voltage clock generator which generates 9.8 V non-overlapping clocks. The charge pump output voltage is a function of the clock frequency of the charge pump. This feature was exploited to control the charge pump and deliver the exact desired bias voltage to the MPPC. The front-end part of the ASIC contains a Transimpedance amplifier (TIA) and post amplification stage. The designed TIA has 75  $\Omega$  input impedance, 86 dB  $\Omega$  gain and -3 dB band-width equal to 59 MHz at the input capacitance (37 pF) of the MPPC. The experimental test of the MPPC operating with the TIA showed that the TIA can amplify the generated pulses in response to illumination up to 1400 nW. However, the TIA was suffering from a saturation problem when the MPPC was illuminated with higher light intensities which consequently reduced the input dynamic range of the MPPC. The overall ASIC consumes 9.45 mW. that is a 2.7 mW by the front end and 6.75 mW by the charge pump.

In order to increasing the compactness and reducing the power consumption of the pill, a second ASIC was fabricated and the MPPC was replaced by an integrated light detector (a single SPAD). The new ASIC consists mainly of a two cells charge pump and a SPAD with its passive quenching circuitry. The integrated SPAD reduced the size of the pill by 5 mm which is the size of the MPPC device. Due to the lower breakdown voltages of SPADs fabricated in CMOS technologies, the size of the charge pump was reduced from five cells to two cells and therefore the power consumption of the charge pump was reduced from 6.75 mW to only 1.46 mW. Furthermore, in the new design and due to the low diode capacitance of the SPAD (typically 200fF), no TIA was required to convert the generated current pulses to voltage and an active resistor was used instead. This eliminated the power consumption by the front-end.

Being a multi-well process, the new (3mm x 3mm) ASIC was also fabricated in the AMS high voltage 0.35 $\mu$ m process to provide an isolation between the low voltage SPAD and the charge pump thus eliminating any current leakage which arises due to the continuous switching nature of charge pumps which might affect the performance of the SPAD [77]. Furthermore, designing a SPAD in this process yields lower dark count (DRC) (~ 4 kcps) noise in comparison to smaller nodes processes such as 130nm and 90nm [118] [116, 117].

The 2-cell high voltage charge pump is capable of generating up to 37.9 V. To get this voltage, a 10 M $\Omega$  resistive load, 10 nF capacitive load and 1.430 kHz clock frequency were used. At these conditions the charge pump showed minimum ripple of 34 mV, a start up time of 19 ms and can deliver 700 nA output current. The current delivered by the charge pump is varied according to the resistive loading at the output node of the charge pump. It can also be changed according to the boosting capacitors values, which were chosen to be off-chip. In order to generate the exact required biased voltage to the SPAD, the charge pump was designed to be operated using a single input clock where the output voltage can be varied accordingly. The single input clock feature is critical to deliver the exact desired voltage for biasing the SPAD and therefore eliminates the need for any regulating circuitry.

Regarding to the SPAD operation, obtained experimental results showed that the SPAD has high detection efficiency in the green-blue region with a peak of 42.4% achieved at 475 nm. The SPAD experienced breakdown at 18.95 V. When biased with excess voltage

of 3.05 V on top of the breakdown voltage, the dark count rate of the SPAD measures about 4 kcps.

The SPAD was biased at 22 V using the 2-cells charge pump which is regulated using a 0.9 M $\Omega$  resistive load at 10.922 KHz clock frequency in order to overcome the problem that is introduced by the high source impedance of the charge pump. The resistive load is used to regulate the current delivered to the SPAD and therefore helps the charge pump to sustain the 22 V at high illumination. If no resistive load is used for regulation, the output voltage generated by the charge pump can drop to 20.4 V due to high current demand of the SPAD; such a voltage drop diminishes the SPAD performance. When a regulating load is used the amount of current that is delivered to the output is increased to a point that the current consumption of the SPAD becomes insignificant to the total delivered current. Adopting this technique to regulate the output current of the charge pump however increases the power consumption from 0.48 mW to 1.46 mW when a regulation load is used.

The capability of the ASIC to measure different levels of autofluorescence emission generated by biological tissue was verified using a small intestine of a lamb that was placed inside a dark box in front of the ASIC. The tissue was excited using a surface mount LED with a peak wavelength of 465 nm and full width half maximum (FWHM) of 25 nm. A long pass filter, with a cut-off wavelength equal to 513 nm, was used to block out light coming from the excitation source. Another band pass filter, with a central wavelength equal to 475 nm and FWHM equal to 64nm, was placed on top of the excitation source. Autofluorescence measurements were conducted on healthy lamb intestine in addition to intestine partially covered by light absorbing black-out material to mimic cancerous regions. This material mimics a tumour formation which absorbs much of the excitation light and emits very weak autofluorescence according to stage and the size of the tumour. The tumour exhibits increased blood flow and correspondingly higher haemoglobin levels. Haemoglobin absorbs incoming photons which will result in substantially reduced autofluorescence which is a characteristic feature of a tumour. Obtained pulse counts showed the healthy tissues emitted 53.3 kcps, whereas the tissues that mimicked cancerous regions (1cm x 1cm) emitted only 21.9 kcps, when both were excited by the LED biased at 3 V (6.6 mA). These readings however are not pure autofluorescence. Amongst these count rates are detected photons that originate from light scattering of the excitation source. This is attributed to the fact that the optical density of the filters is not high enough to block out this unwanted light. Reducing such background scattered light will improve the

autofluorescence detection efficiency at even lower excitation levels and therefore can reduce the huge power consumption by the excitation source.

A pill prototype was packaged in a glass tube of borosilicate glass which has a visible light transmission >92%. The design included the following components: an 11mm x10mm double-sided PCB board for the ASIC, LED, optical filters and charge pump capacitors; a double-sided 12mm diameter round PCB implementing the counter and control unit; double-sided 14 mm diameter round transmitter PCB; two SR48 batteries. The complete prototype is 16mm x 45mm in size and weighs 12g including batteries.

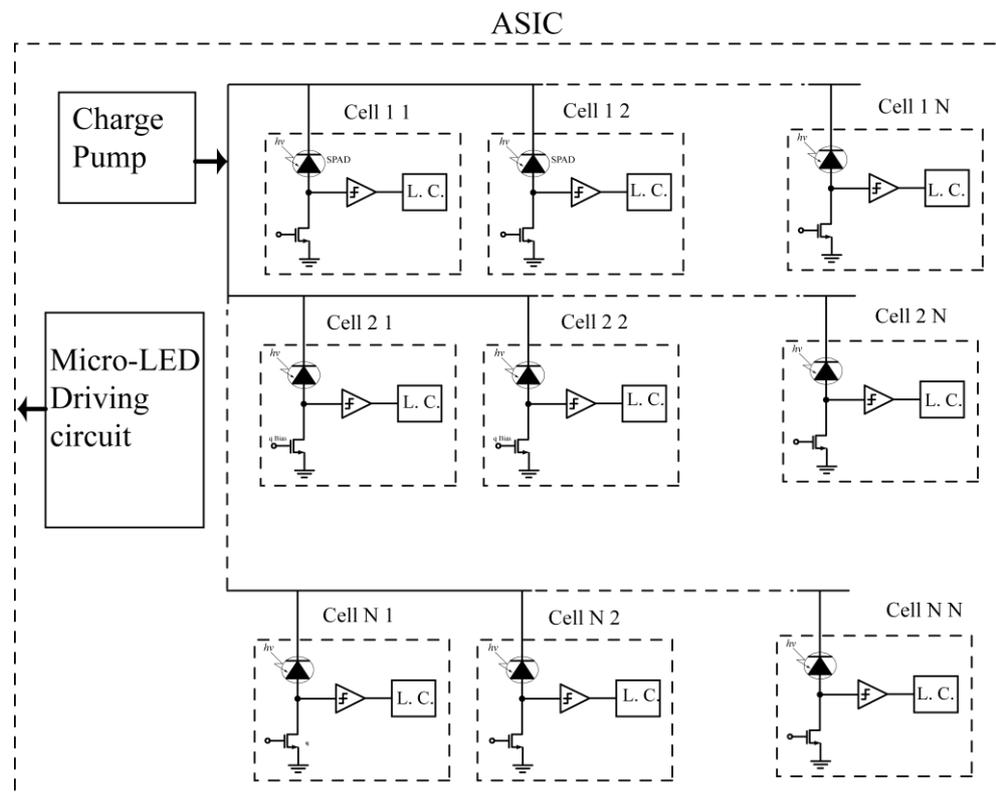
The LED consumes 19.8mW, (6.6mA). The ASIC consumes 1.76mW (487 $\mu$ A) drawn by the charge pump and 255 $\mu$ W (85 $\mu$ A) by the SPAD buffer. The controller and radio link power requirement averages 150 $\mu$ W (50  $\mu$ A). The total average current drawn is 7.137mA, hence the system was capable of operating from 165 mAh SR44 batteries for 23 hours, which is well in excess of the 9 hours typically required to traverse the human intestine. Given the compactness and low power consumption of this technology it is anticipated that it may be readily scaled to make an imaging array for wireless autofluorescence scanning.

## **7.2 Future work**

The LED is the main power consumer in the pill, it consumes 19.8 mW which is almost 10 times more than the power consumed by the rest of the pill including the transmitter. Cutting down the LED power consumption can be achieved by upgrading the existing system so it can perform fluorescence time-resolved measurement instead of steady state measurements. A key component in time resolved measurements is a fast laser excitation source (pico-seconds) [36]. Incorporating a pulsed laser device into the pill is not practical due to their bulky and expensive drive electronics. Recently however micro-LED devices have been demonstrated to produce sub nano-second pulses which are suitable for fluorescence life time measurements [125]

By using a micro-LED as an excitation source performing lifetime measurement in the small intestine is feasible. For this to take place a new ASIC in AMS process can be designed (**Figure 7.1**) and can include the following:

- A charge pump that can produce up to 25 V. Having already designed the SPAD and therefore its exact breakdown voltage is known, the existing charge pump design can be re-customised so it produces the exact voltage and current required.
- A SPAD array cell (i.e 10 x 10) where each cell includes a SPAD, an active quenching circuit, a comparator and local counter (LC).
- A high speed micro-LED driving circuit and time gating circuitry to synchronized the excitation end-up time with the SPAD detection time.



**Figure 7.1 proposed ASIC for time resolved measurement that can be used for cancer detection through autofluorescence life-time measurements.**

The capability of capturing the life time fluorescence decay, which is usually a few hundred nano-seconds, depends on the SPAD ability to count as many photons as possible in this short time. This can be achieved by employing an active quenching circuit which is used to quench the avalanche process of the SPAD and therefore produce ultra short pulses (few nano-seconds). The generated short pulses are passed to the comparator and then to the local counters where the detected photons are counted after each excitation pulse. For example for a 300 ns fluorescence decay, using 2 ns quenched SPAD pulses, an 8-bit local

counter is needed for each cell. The counts of each cell is then passed to a processor where the data is processed and a histogram of the life-time fluorescence can be then obtained.

Further improvement to the ASIC design can be achieved based on the existing measurement data. Having already measured the power consumption of the SPAD at different illuminations, it would be advantageous for the pill miniaturisation to investigate the feasibility of integrating the charge pump's boosting capacitors. It is also important when designing the charge pump to determine roughly the amount of power that will be required by the 100-pixel array. Unlike the steady state measurement, the SPAD is only operated to detect pulses for several hundreds of nano-seconds, which is the decay lifetime of many fluorescent molecules. Pre-estimating the total required current by the array will determine whether it is efficient for the charge pump output current to be regulated by a resistive load or by employing a feedback system that controls the output voltage by setting the charge pump clock frequency.

Based on the previous discussion about the new proposed ASIC, it can be said that the proposed ASIC design in this section is more complicated than the existing ASIC, however many advantages will be gained including:

- With life-time measurements the power consumption of the LED, which is the main power consumer in the pill, will be reduced dramatically due to the ultra short operating periods (sub-nanosecond pulses).
- With life time-measurements there will be no need for optical filters as there is no over-lapping between the excitation time and detection time, thus a smaller size pill can be realised.
- Having already designed and measured the SPAD operating conditions in the AMS high voltage 0.35 $\mu$ m process, redesigning a new ASIC using the same process would allow for more customised design of the charge pump to take place which will consequently improve the system power efficiency.

Whilst lifetime measurements might offer potential advantages in terms of power consumption, the lifetime measurements' capability of distinguishing between cancerous and normal tissues is still not as validated as the steady state measurement is. Therefore, further research is required to be conducted before adopting this technique into the capsule format.

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## Conference:

- Al-Rawhani, M., et al. *Photocurrent dependent response of a SPAD biased by a charge pump*. in *Circuits and Systems (ISCAS), 2011 IEEE International Symposium on*.

## Journal publication (Submitted):

- Mohammed Al-Rawhani, Danial Chitnis, James Beeley, Steve Collins, and David R. S. Cumming., *Implementation of a wireless autofluorescence detection capsule*, IEEE Transactions on Biomedical Circuits and Systems.