

Theory And Applications Of Delta-Sigma Analogue-To-Digital Converters Without Negative Feedback

A Thesis
Presented to
The Academic Faculty

by

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In Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Department of Electronics and Electrical Engineering
University of Glasgow
June 2008

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ACKNOWLEDGEMENTS

I wish to acknowledge all the people who have assisted me in this work and made my experience at Glasgow so enjoyable. First and foremost, I thank my supervisor Bernd Porr for he has given me excellent guidance throughout the years. I would also like to thank Jack Sewell for his assistance in the beginning of my research and Wolfson Microelectronics for their financial and intellectual support.

A huge thank you goes to my office mates Mykhaylo Teplichuk alias Micha, Doyin Thompson alias The Bushwoman, Lynsey McCabe and Colin. They all offered much relief from the tedium of research work through long discussions about life, gossip and Bob The Builder. That in general as well as far too many meal and coffee breaks.

I would like to thank my family, for being very supportive and patiently listening to me trying to explain my research. I am indebted to them for the sacrifices that they made to put me through school as an undergraduate and graduate.

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LIST OF SYMBOLS OR ABBREVIATIONS

A/D	analog-to-digital.
CT	continuous-time.
D/A	digital-to-analog.
DT	discrete-time.
ϵ	quantization error introduced by the qunatizer.
f_{bw}	band-width of interest.
F_{FM}	frequency of the frequency modulated signal.
FIR	finite impulse response.
FM	frequency modulated.
F_c	center frequency fo a voltage controlled oscillator.
F_d	decimated sampling frequency.
F_s	sampling frequency.
F_{se}	elevated sampling frequency.
K_{vco}	gain or sensitivity of a voltage controlled oscillator.
MASH	multi-stage noise shaping.
NTF	noise transfer function.
Nyquist	states that the sampling frequency is twice that of the highest signal frequency of interest.
R	oversampling ratio.
σ_ϵ^2	total noise power.
SNR	signal-to-noise ratio.
STF	signal transfer function.
VLSI	very large-scale integration.

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SUMMARY

Analog-to-digital converters play a crucial role in modern audio and communication design. Conventional Nyquist converters are suitable only for medium resolutions and require analog components that are precise and highly immune to noise and interference. In contrast, oversampling converters can achieve high resolutions (>20 bits) and can be implemented using straightforward, high-tolerance analog components. In conventional oversampled modulators, negative feedback is applied in order to control the dynamic behavior of a system and to realize the attenuation of the quantization noise in the signal band due to noise shaping. However, feedback can also introduce undesirable effects such as limit cycles, jitter problems in continuous-time topologies, and infinite impulse responses. Additionally, it increases the system complexity due to extra circuit components such as nonlinear multi-bit digital-to-analog converters in the feedback path. Moreover, in certain applications such as wireless, biomedical sensory, or microphone implementations feedback cannot be applied. As a result, the main goal of this thesis is to develop sigma-delta data converters without feedback. Various new delta-sigma analog-to-digital converter topologies are explored their mathematical models are presented. Simulations are carried out to validate these models and to show performance results. Specifically, two topologies, a first-order and a second-order oscillator-based delta-sigma modulator without feedback are described in detail. They both can be implemented utilizing VCOs and standard digital gates, thus requiring only few components. As proof of concept, two digital microphones based on these delta-sigma converters without feedback were implemented and experimental results are given. These results show adequate performance and provide a new approach of measuring .

CHAPTER I

INTRODUCTION

1.1 Motivation

The market for personal communication devices is rapidly expanding with the development of new services and applications. Devices such as cordless telephones, cellular telephones, and wireless LANs require low power and low cost solutions. The market for audio applications for automotive, home theater, and personal computer demands cost effective and easy interfacing solutions as well. This range of applications and devices has led to a proliferation of communication standards and modulation schemes. At the same time consumers are demanding low-cost, low-power, and small devices that satisfy these communication requirements. As a result, there has been much effort put into the in the design of integrated circuits for personal communication that can easily be integrated in a low cost technology. The relentless progress in [VLSI](#) silicon technology optimized for digital circuitry generally has made it economically advantageous to trade analog signal processing for digital signal processing. Moving from analog to digital signal processing, however, generally increases the demand on the data converters that provide the interfaces between analog and digital circuits [[Manickavel and Pedar, 1974](#); [Howell and Sander, 1969](#); [Razavi, 1996](#)]. One technique for providing the interface between the analog and the digital circuit is by using delta-sigma [A/D](#) converter. In literature the nomenclature delta-sigma or sigma-delta converters are equally used. However, the original name delta-sigma was coined by the inventors Inose and Yasuda and thus the term delta-sigma will be used in this work [[H. Inose and Marakami, 1962](#)]. While delta-sigma converters have been around for some time [[H. Inose and Marakami, 1962](#)], it is only in the last two decades that they have become more attractive. One reason being is that they are particularly suited for [A/D](#) conversion of narrow band signals used in audio, communication and instrumentation devices. That is, they can achieve

very high resolutions for low-bandwidths. Examples of such applications include digital telephone transmission, wireless phones, audio applications, and medical imaging. This thesis is concerned with the improvement of delta-sigma A/D converters. It is hoped that by using new and modified modulator topologies and digital signal processing the complexity of delta-sigma modulators can be reduced while still obtaining the same performance. Furthermore, as power dissipation is becoming an increasingly important issue in the design of analog to digital converters as signal processing systems move into applications requiring portability, a secondary goal of this thesis is to reduce the analog circuitry improving power dissipation.

1.2 Main Contributions

The main goal of this thesis is to develop delta-sigma data converters with reduced analog complexity and thus to bring the digital domain closer to the analog domain. Simplifications in the analog domain are achieved by removing the negative feedback path from delta-sigma converters while still achieving the desired results. To this extent, analog-to-digital data converters based on voltage-controlled oscillators are explored and developed. As an application, two digital microphones utilizing oscillator based analog-to-digital converters are realized. Undersampling is used as a powerful technique to efficiently deal with very high signal frequencies and thus reduce requirements on sampling and acquisition circuitry. The use of undersampling in conjunction with the use of simplified oscillator-based data converters results in a novel approach to realize digital microphones. Moreover, second-order oscillator based analog-to-digital data converters are developed, resulting in improved performance results compared to their first-order counterparts. In this context, different second-order circuit techniques are explored that result in performance improvements and/or trade-offs. In addition, a more general goal of this thesis is to develop techniques at both the architecture and circuit levels to minimize power dissipation. In the context of these goals, some key research results are summarized below:

- Demonstration of the reduction in circuit complexity of a frequency sigma-delta

modulator by utilizing a D-FF as a quantizer and differentiator.

Soell, S. and Porr, B. (2006) A VCO Based Digital Microphone Utilizing a FIR Sigma Delta Converter. IEEE International Conference on Mixed Design of Integrated Circuits and Systems

- Demonstration of a digital condenser microphone with reduced analog circuitry based on a LC-oscillator and a first-order sigma delta modulator without feedback.

Soell, S. and Porr, B. (2007) An Undersampling Digital Microphone. IEEE International Symposium on Circuits and Systems

- Demonstration of a Schmitt trigger oscillator based digital microphone based on a first-order sigma delta modulator without feedback.

Soell, S. and Porr, B. (2007) An Undersampling Digital Microphone Utilising Second Order Noise Shaping. IEEE International Conference on Mixed Design of Integrated Circuits and Systems

- Demonstration of utilizing undersampling as a technique to efficiently implement an oscillator based digital microphone.

Soell, S. and Porr, B. (2007) An Undersampling Digital Microphone Utilising Second Order Noise Shaping. IEEE International Conference on Mixed Design of Integrated Circuits and Systems

- Demonstration of realizing oscillator-based higher order noise shaping analog-to-digital converters.

Soell, S. and Porr, B. (2007) An Undersampling Digital Microphone Utilising Second Order Noise Shaping. IEEE International Conference on Mixed Design of Integrated Circuits and Systems

1.3 Scope and Structure of the Thesis

This work is divided into six chapters. After this introduction the second chapter introduces the concept of analog-to-digital conversion and discusses methods used to characterize analog-to-digital converters. This includes both Nyquist and oversampling converters. An introduction of the most important analog-to-digital oversampling architectures such as low-pass and band-pass topologies and their performance characterization is given. In this context, essential concepts are reviewed such as decimation, undersampling, and non-idealities in oversampling analog-to-digital converters. Chapter 3 then focuses on a first order delta-sigma analog-to-digital converter without feedback. After a review of existing work, the theory of the modulator topology is explained by revisiting established frequency modulation and de-modulation techniques. New and improved first-order analog-to-digital converters are introduced and a mathematical model for performance evaluation is given. The chapter then verifies obtained results with simulations and concludes with a general discussion. These simulations include both, ideal analog-to-digital converters as well as non-ideal topologies. Subsequently, as a proof-of-concept, the discussed analog-to-digital converter is implemented in a practical application. Chapter 4 covers this. More specifically, two digital oscillator-based microphones are presented based upon analog-to-digital converters without feedback. An LC-oscillator and also a Schmitt-trigger based oscillator are used to realize digital condenser microphones. Both topologies utilize undersampling to deal with high frequency signals. Experimental results are presented and discussed. Chapter 5 then improves the performance of first order analog-to-digital converters by presenting two second-order modulator topologies, also without utilizing feedback and based on oscillators. A mathematical background is established and the topologies are evaluated using simulations. Again, simulation results are presented which also address nonlinearities. Chapter 6 contains a summary of the conclusions of this research and the goals which were achieved, along with a comparison with existing works. This is followed by a proposal for future research, which is given in more detail at the end of Chapter 6.

CHAPTER II

SIGMA-DELTA MODULATORS

2.1 *Nyquist-rate A/D Converters*

Analog-to-digital conversion is the process of encoding an analog signal that is continuous in time and amplitude into a signal that is discrete with respect to time and quantized with respect to amplitude. There are three fundamental operations involved in the conversion process of a general A/D system. These are illustrated in Figure 2.1. The analog input signal, $x(t)$, first passes through a bandlimiting low-pass filter, removing the signal components that lie above one-half of the sampling rate of the subsequent sampler. Otherwise, from the Nyquist sampling theorem [Nyquist, 1928], high frequency components of $x(t)$ would alias into the baseband upon sampling, causing distortion. Following the anti-aliasing filter, the now bandlimited signal, $x_a(t)$, is sampled, thus yielding the discrete-time signal, $x_s(t)$, which is still continuous in amplitude. The sampled-data analog signal is then quantized in amplitude by utilizing a quantizer before being encoded into the digital output data signal, $y[n]$.

2.1.1 Sampling

In the sampling process, a continuous signal is sampled at uniformly spaced time intervals, T_s . The samples $x[n]$, of the continuous time signal, $x(t)$ can be expressed as $x[n] = x(nT_s)$. The process of sampling a continuous-time signal is shown in Figure

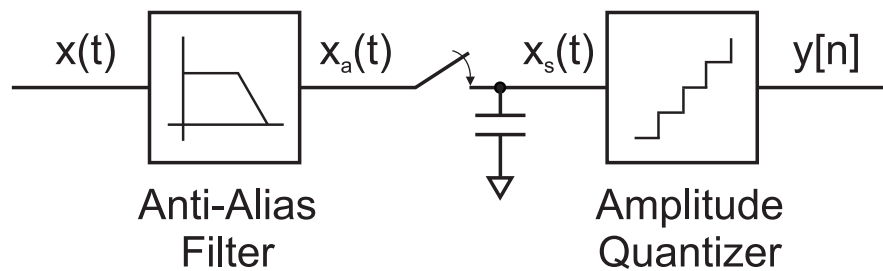


Figure 2.1: Fundamental operations comprising analog-to-digital conversion.

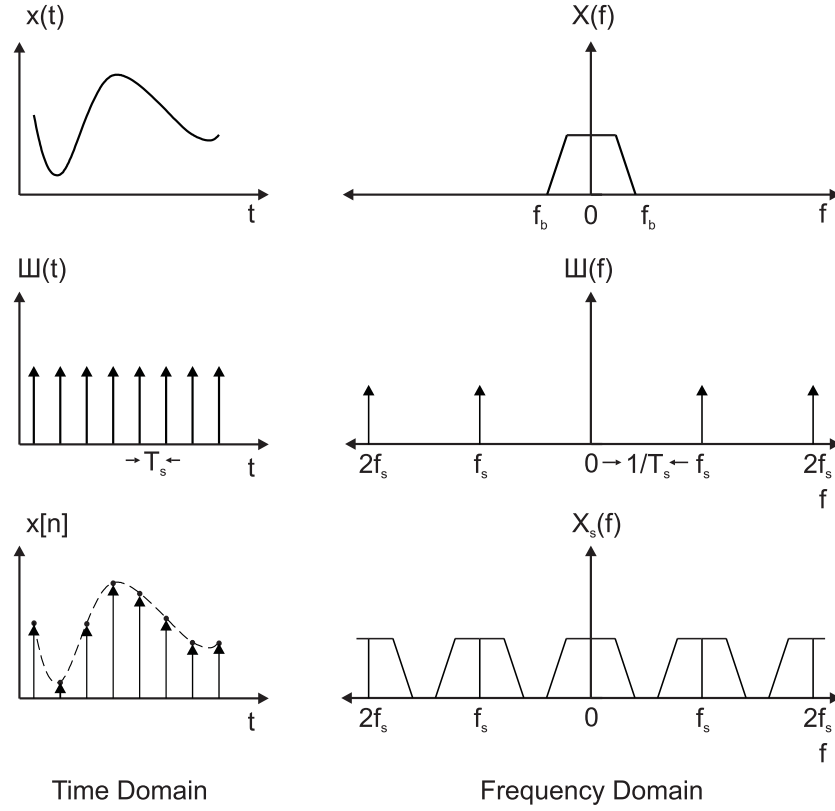


Figure 2.2: Sampling Process of an Analog Signal. On the left side the signals are represented in the time-domain, to the right in the frequency domain.

2.2. In the figure, a continuous signal, $x(t)$, is multiplied by a Dirac comb, often also described as a Shah function, $\text{III}(t)$. The Shah function is a series of Dirac pulses spaced at width T_s [Bracewell, 2000, pp.81ff]:

$$\text{III}(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s). \quad (2.1)$$

The effect, in the frequency domain, of the sampling process is to create periodically repeated versions of the signal spectrum, $X(f)$, at multiples of the sampling frequency $F_s = 1/T_s$. The spectrum of the sampled signal, $X_s(f)$, is depicted in the right hand side of Figure 2.2. In general, the signal, $X_s(f)$, can be reconstructed back to its continuous counterpart, $x(t)$, if the repeated versions of the signal spectrum do not overlap. As a result, the signal must be band limited to half the sampling rate, F_s . In turn, a signal with bandwidth f_b must be sampled at a rate great than twice of its bandwidth, $F_s \geq 2f_b$. This is known as the Nyquist-Shannon sampling theorem [Nyquist, 1928]. An important fact to note is that sampling is a linear operation. Therefore, the effects of sampling amplitude can be divided into two effects: the effect of sampling the original signal,

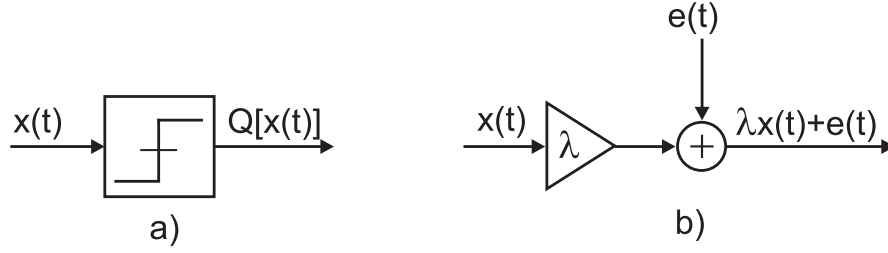


Figure 2.3: Additive Quantizer Model: a) 1-bit quantizer b) noise model including gain variation

and the effect of sampling noise superimposed with the original input. [Nyquist](#) rate converters sample analog signals which have maximum frequencies slightly less than the [Nyquist](#) frequency.

2.1.2 Quantization

Once sampled, the time-discrete signal samples must also be quantized in amplitude to a finite set of output values. Quantization is the process of converting an analog signal into a finite range number system [[Goodall, 1951](#)]. Quantization thus introduces an error signal that depends on how well the signal is being approximated. Unlike sampling, quantization of a signal is a non-reversible operation [[van de Plassche, 2003](#), pp.7ff]. The process of quantization is shown in Figure 2.3 a) where a 1-bit quantizer maps an analog signal into the digital domain by rounding up or down to the nearest step size. Alternatively, an example of multi-level quantization is depicted in figure 2.4 a). The quantization step, q , of a b -bit quantizer is given as:

$$q = \frac{V_{ref}}{2^b}, \quad (2.2)$$

where V_{ref} is a reference signal. Figure 2.3 b) depicts a model for an approximation to the 1-bit quantizer. [[van Engelen and van de Plassche, 1999](#), p.38]. The model includes a time invariant gain λ because adding quantization power to an input signal with variable power would not model the 1-bit quantizer accurately. In case of the 1-bit quantizer the gain can have any value greater than zero. For multi-bit quantizers, the gain would be closer to unity. Assuming a gain of unity, the quantization error is given as the difference between the quantized input, $Q[x(t)]$, and ideal input, $x(t)$:

$$\epsilon(t) = Q[x(t)] - x(t). \quad (2.3)$$

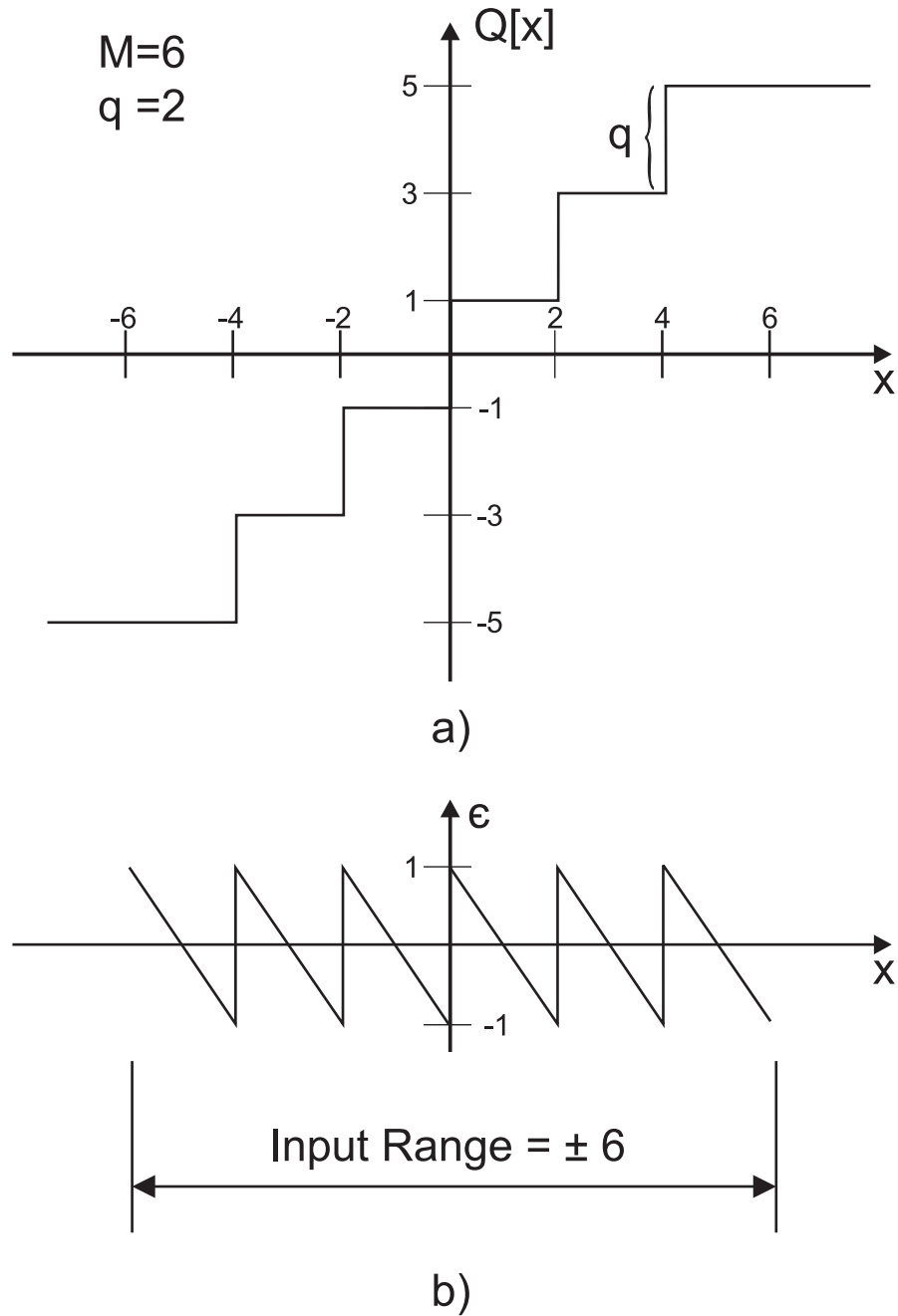


Figure 2.4: Part a) depicts a uniform b-bit quantizer utilizing $M=6$ quantization levels, with a quantization step of $q=2$. Here, the input to the quantizer is a ramp-signal. Part b) shows the introduced error ϵ which is the sawtooth error signal.

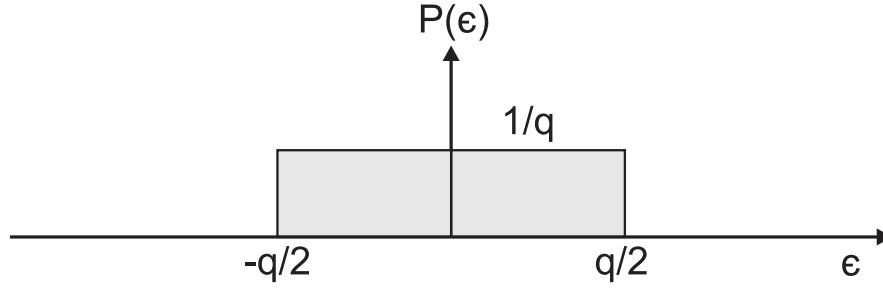


Figure 2.5: Quantization error with a uniform probability density.

The error $\epsilon(t)$ forms a periodic sawtooth waveform in this case as depicted in figure 2.4 b). When expressed as a Fourier series expansion the quantization error $\epsilon(t)$ is given as [van de Plassche, 2003, p.12]:

$$\epsilon(t) = \frac{q}{\pi} \sum_{k=1}^{\infty} \left\{ \frac{1}{k} \sin \left[2\pi k \frac{x(t)}{q} \right] \right\} \quad (2.4)$$

Equation 2.4 illustrates that the quantization error $\epsilon(t)$ due to quantization forms a harmonic series of phase-modulated sinusoids. This can be seen when realizing that the argument of each sine term is a linear function of input $x(t)$. Consequently, phase modulation maps to amplitude quantization [Hawksford, 2002, p.589]. The model in Figure 2.3 b) assumes that the quantization error is largely uncorrelated from sample to sample and has equal probability of lying anywhere in the range of $\pm \frac{q}{2}$ ([van de Plassche, 2003], p.7 ff). This property is illustrated in Figure 2.5. However, for dc-inputs and inputs that change regularly by multiples or sub-multiples of the step size in between sample times, as happens in feedback circuits, the linear noise model does not hold anymore [Norsworthy et al., 1997, p.5]. Under the assumption that the error is uncorrelated to the input signal and has uniform distribution, its total noise power value σ_{ϵ}^2 is given by [Staff, 1982, p.55]:

$$V_{Q_{rms}}^2 = \sigma_{\epsilon}^2 = \int_{-q/2}^{q/2} \epsilon^2 P(\epsilon) d\epsilon = \frac{1}{q} \int_{-q/2}^{q/2} \epsilon^2 d\epsilon = \frac{q^2}{12}. \quad (2.5)$$

The average value of the error is zero with the assumptions made. Since the size of the quantization level q is halved for each additional quantizer bit, equation 2.5 shows that the noise power decreases by 6dB for each additional bit. For a sinusoidal input with peak-to-peak amplitude, V_A , of $2^b q/2$, the *rms* signal value, $V_{A_{rms}}$, is given by $\frac{2^b q}{2\sqrt{2}}$. Then

the signal-to-noise ratio can be calculated:

$$\begin{aligned}
 SNR_{dB} &= 20 \log \left(\frac{V_{A_{rms}}}{V_{Q_{rms}}} \right) \\
 &= 20 \log \left(\frac{2^b q}{\frac{2\sqrt{2}}{\sqrt{12}} q} \right) = 20 \log \left(\sqrt{\frac{3}{2}} 2^b \right) \\
 &= 6.02 b + 1.76 \text{ dB}.
 \end{aligned} \tag{2.6}$$

Equation 2.6 shows that the signal-to-noise ratio of a quantizing system increases by 6 dB when an extra bit is added. It is often useful to express equation 2.5 as a total noise power density per unit bandwidth [van de Plassche, 2003, pp.9ff], $\sigma_\epsilon^2(f)$:

$$\sigma_\epsilon^2(f) = \frac{q^2}{12 f_{bw}} = \frac{q^2}{6 F_s}, \tag{2.7}$$

where f_{bw} is the quantization noise bandwidth and F_s is the sampling frequency. Since the signal-to-noise ratio is calculated over a bandwidth equal to half the sampling frequency we have $f_{bw} = 1/2 F_s$. Thus, for systems that use Nyquist sampling the signal-to-noise ratio as a density can be written as:

$$SNR = 2^{b-1} \sqrt{3 F_s} \tag{2.8}$$

Then the SNR for a system with a bandwidth equal to f_{bw} is found by dividing equation 2.8 by $\sqrt{f_{bw}}$ to give:

$$SNR = 2^{b-1} \sqrt{\frac{3 F_s}{f_{bw}}} \tag{2.9}$$

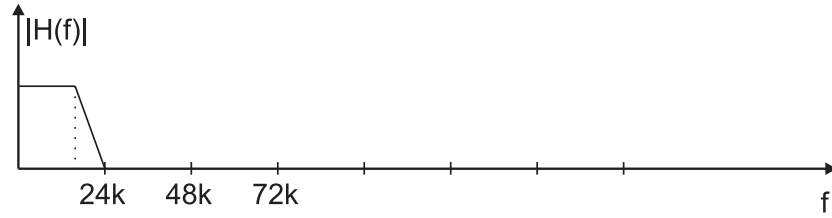
Equation 2.9 is convenient for dynamic range calculations of systems which do not use Nyquist sampling. As will be shown shortly increasing the ratio $\frac{F_s}{f_{bw}}$ reduces the quantization noise density, resulting in higher SNR. Summarizing, if the resolution of an A/D converter is limited by quantization noise, then its dynamic range increases by approximately 6dB with every additional bit of resolution, b . It might be noted that in practical applications sometimes circuit noise, thermal noise, or other non-linearities determine the ultimate resolution of the A/D converter.

2.1.3 Limitations of Nyquist-Rate A/D Converters

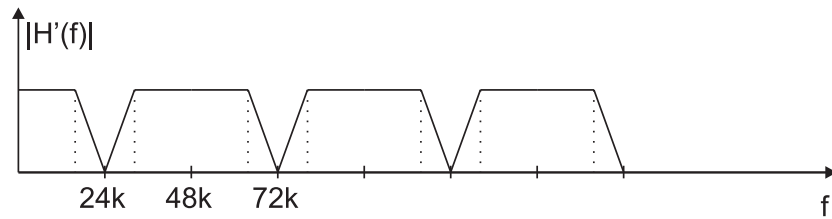
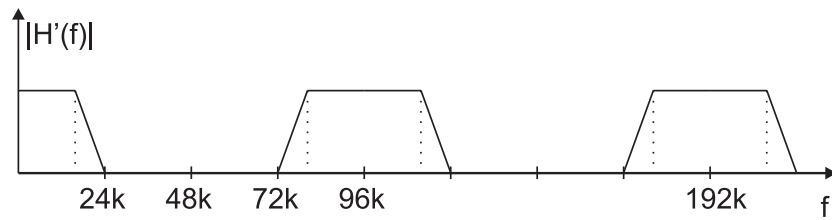
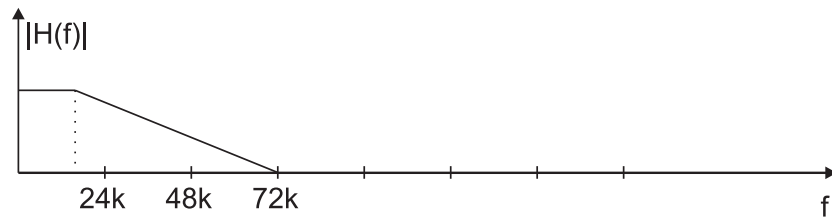
A typical limiting factor in Nyquist-rate architectures is that some operations such as comparison, amplification, or subtraction must be performed to the overall precision of the converter [Aziz et al., 1996, p.64]. This typically translates into the need for precise component matching unless special calibration, error-correction, or trimming techniques are used. A steep anti-aliasing filter must also precede any Nyquist-rate A/D converter. This band-limiting filter rejects frequency components of the signal located above one-half of the sampling frequency in order to prevent aliasing distortion. These anti-aliasing filters are often quite difficult to design to allow for a large signal bandwidth [van de Plassche, 2003, pp.27ff]. In addition, it is still quite difficult to realize precise analog filters to high order in a VLSI technology without resorting to active circuits.

2.2 Over-Sampling A/D Converters

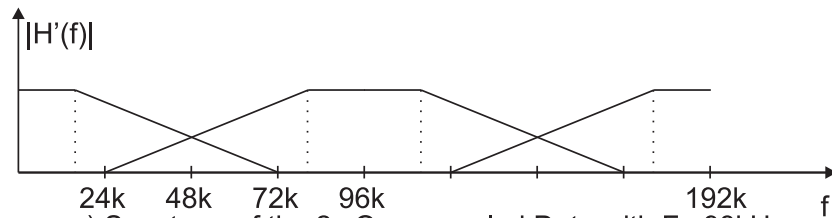
The demands on the circuitry of the A/D converter and their individual required precision can be relaxed by exploiting speed, or oversampling [Walden, 1999]. The use of over-sampling is advantageous as it alleviates the problems mentioned for Nyquist A/D converters above. In particular, Figure 2.6 shows how oversampling can reduce the demands on the aliasing filter. The spectrum of the input signal is shown in 2.6 a) as having a bandwidth of interest of 22kHz. Since the sampling frequency is 48kHz, anything above 24kHz will be aliased into the band of interest. Thus a steep anti-aliasing filter is needed. With such a filter the sampled data has the spectrum as shown in Figure 2.6 b). When oversampling the input signal the anti-aliasing filter can be relaxed. This is illustrated in 2.6 c) and d). It is now sufficient for the filter to attenuate signals above 72kHz without polluting the band of interest with aliased components. In particular, Figure 2.6 d) shows that the band of interest does not contain any aliased components as oversampling was used. Besides reducing the requirements on aliasing filters, the main advantage of oversampling is that it lowers the noise power introduced by quantization in the band of interest. This is because the quantization error is spread out



a) Anti-aliasing Filter Response for a Nyquist Converter

b) Spectrum of the Sampled Data with $F_s = 48$ kHzc) Spectrum of the Sampled Data with $F_s = 98$ kHz

d) Anti-aliasing Filter Response for a 2x Oversampling Converter

e) Spectrum of the 2x Oversampled Data with $F_s = 98$ kHz**Figure 2.6:** Comparison of aliasing filter for Nyquist and oversampling converters.

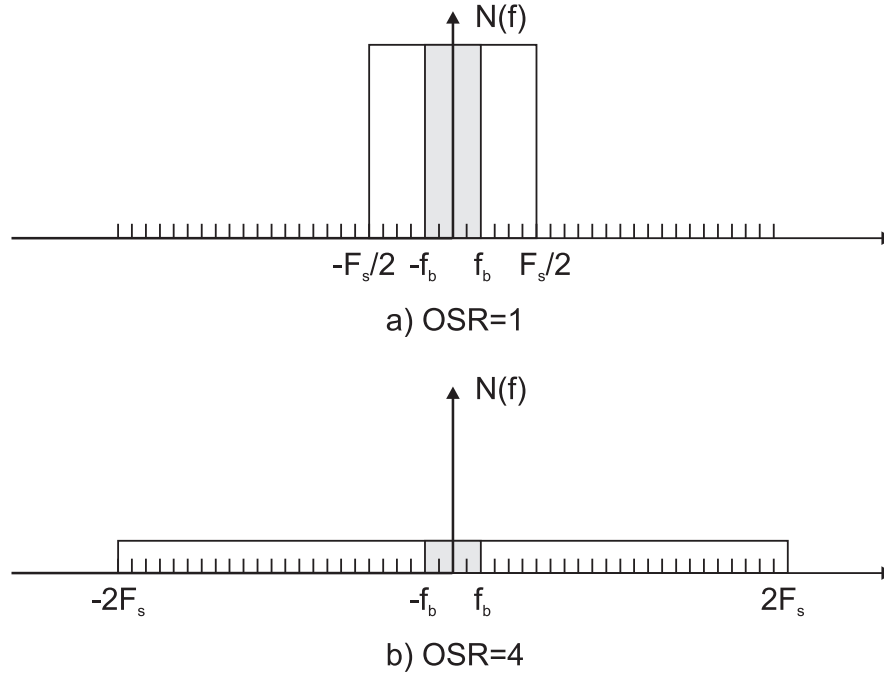


Figure 2.7: Quantization noise power for two oversampling ratios

over a larger frequency band. As a result the error density is reduced and the effective resolution of the converter increases [Cherry and Snelgrove, 1999]. This is depicted in figure 2.7. Figure 2.7 a) shows the quantization noise power for a Nyquist converter. Meanwhile, in Figure 2.7 b) an oversampling factor of 4 reduces the quantization noise power in the band of interest by a factor of 4. Only a relatively small fraction of the total noise power falls within the band of interest and the noise outside the bandwidth can be greatly attenuated by means of digital low-pass filtering. In general, for each doubling of the sampling frequency F_s , 1/2 bit of increase in resolution is achieved [Johns and Martin, 1997, p.535]. The signal-to-noise ratio is then given as:

$$SNR = 2^{b-1} \sqrt{3} \sqrt{R}, \quad (2.10)$$

where, the oversampling ratio, R , is defined as $R = \frac{F_s}{2f_{bw}}$. Converting to decibels gives:

$$SNR_{dB} = 6.02 b - 1.25 + 10 \log(R). \quad (2.11)$$

Again, the total noise power introduced due to quantization is exactly the same as in the case of a Nyquist rate converter, but its frequency distribution is different because of the higher sampling rate.

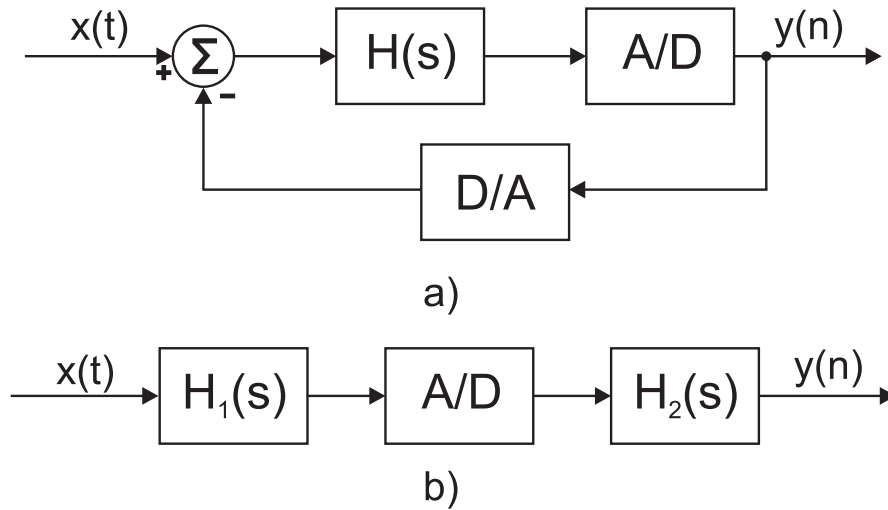


Figure 2.8: First-Order Delta-Sigma Modulator. Figure a) shows the typical implementation of an arbitrary delta-sigma modulator. Part b) depicts the less conventional modulator employing no negative feedback.

2.2.1 The FIR Modulator Principle

The basic thought behind every delta-sigma modulation is the exchange of resolution in time for resolution in amplitude. That is, narrow band signal can be digitized to a very accurate level. As will be shown later, conventional delta-sigma modulators are synonymous with negative feedback; however, they can also be realized without negative feedback. Thus, there are essentially two main implementations for the basic delta-sigma modulator, both of which are depicted in Figure 2.8. Part a) of the figure shows a delta-sigma modulator consisting of a coarse analog-to-digital converter, a digital-to-analog converter, and a loop-filter, $H(s)$, placed within a feedback loop. In this thesis, however, the focus is on delta-sigma converters without feedback. A general principle is depicted in figure 2.8 b). This modulator also consists of a coarse analog-to-digital (A/D) converter and a loop-filter, $H_1(s)$, but lacks the D/A converter in the feedback loop. Instead a second filter, $H_2(s)$, is needed. In the case of the modulator with feedback the input signal, $x(t)$, gets quantized to form a digital signal [Cherry and Snelgrove, 1999, p.2]. The D/A converter converts the digital output back to an analog signal which is then compared to the input signal as depicted in figure 2.8 a). The binary pulses represent the in the integrator accumulated sign of the difference between the input and feedback signals, hence the prefix delta (Δ). The feedback loop causes the

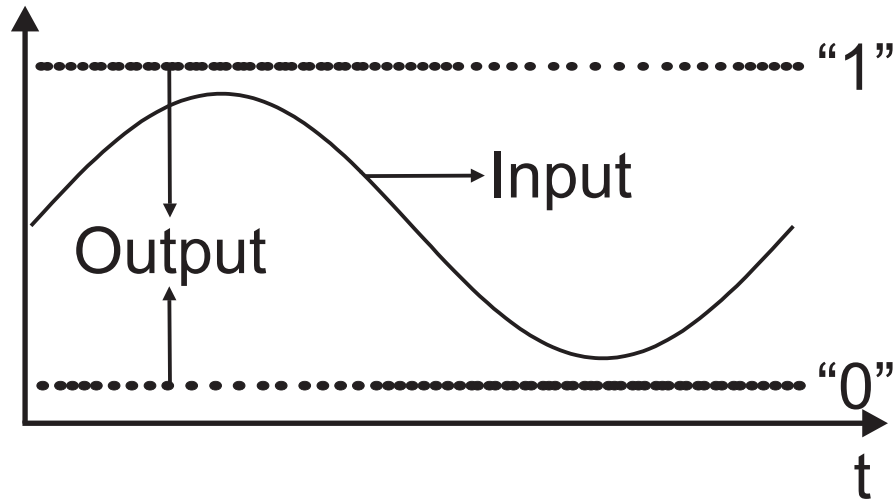


Figure 2.9: Input and output of a first-order delta-sigma modulator.

quantization error to be suppressed for signals falling within the pass-band of the loop filter. The prefix sigma stems from the use of an integrator within the filter (summation = Σ). In the case of the modulator without feedback, the input signal, $x(t)$, gets quantized to form a digital signal also. However, since no feedback loop, the quantization error will be noise shaped by a second filter $H_2(s)$. Consequently, the prefix (Δ) does not apply. However, the prefix Σ from the use of an integrator within the filter $H_1(s)$ can still be used. The notation used to describe the modulator without feedback will be finite impulse response modulator (*FIR modulator*). This is similar to *FIR* filters as they lack a feedback loop also [Chan and Rabiner, 1973]. In either case of modulator, when the sinusoidal input to the two modulator topologies is close to a plus full scale, the digital output is positive during most clock cycles. Similarly, when the input is close to a full negative scale, the digital output is negative during most clock cycles. In both cases, the local average of the digital modulator output tracks the analog input. When the input is near zero, the value of the modulator output varies rapidly between a plus and a minus full scale with approximately zero mean. This is depicted in Figure 2.9. To further analyze the two modulator topologies we need to apply the previously introduced three main principles that make up any sigma-delta modulator and *FIR* modulator. These are *over-sampling*, *quantization*, and *noise shaping*. The properties of quantization outlined in section 2.1.2 apply to the two modulator topologies. As mentioned in section

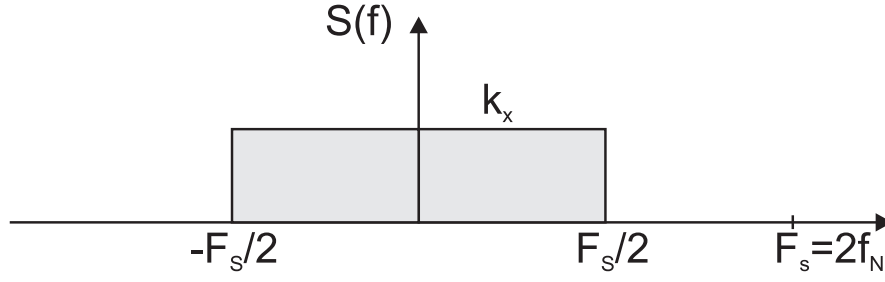


Figure 2.10: Noise spectrum of a Nyquist converter

2.2, specifically equation 2.11 showed that for doubling the sampling frequency a 3dB increase in resolution can be achieved. Delta-sigma and FIR modulators take advantage of this and over-sample to achieve better resolution. The performance modeling criteria designated the introduced quantization noise process as white, which means that the noise power is uniformly distributed between $[-\frac{F_s}{2}, \frac{F_s}{2}]$. This is depicted in figure 2.10. While this is true for delta-sigma modulators, it will be shown later that the quantization noise power might not necessarily be white for FIR modulators. Still, the total noise power is given by $V_{Q_{rms}}^2 = \sigma_\epsilon^2$. The spectral density height, k_x , can then be calculated [Johns and Martin, 1997, p.533]:

$$\int_{-\frac{F_s}{2}}^{\frac{F_s}{2}} S^2(f) df = \int_{-\frac{F_s}{2}}^{\frac{F_s}{2}} k_x^2 df = k_x^2 F_s = \sigma_\epsilon^2. \quad (2.12)$$

Equation 2.12 can be solved for k_x to give:

$$k_x = \sigma_\epsilon \sqrt{\frac{1}{F_s}}. \quad (2.13)$$

Equation 2.13 shows that the total quantization noise power will be reduced by 3dB for doubling the sampling frequency F_s . In addition to this over-sampling advantage, both modulator topologies utilize noise shaping to further attenuate the quantization error.

2.2.2 The Concept of Noise-Shaping

Noise-shaping is generally done by utilizing a high-pass filter to suppress unwanted components in the band of interest. There are two ways to realize a high-pass filter for the introduced quantization noise. Firstly, the in-band quantization noise power can be suppressed with a high-pass dramatically by embedding the quantizer in a feedback loop [Inose et al., 1966]. A filter can then be used to spectrally shape the quantization noise

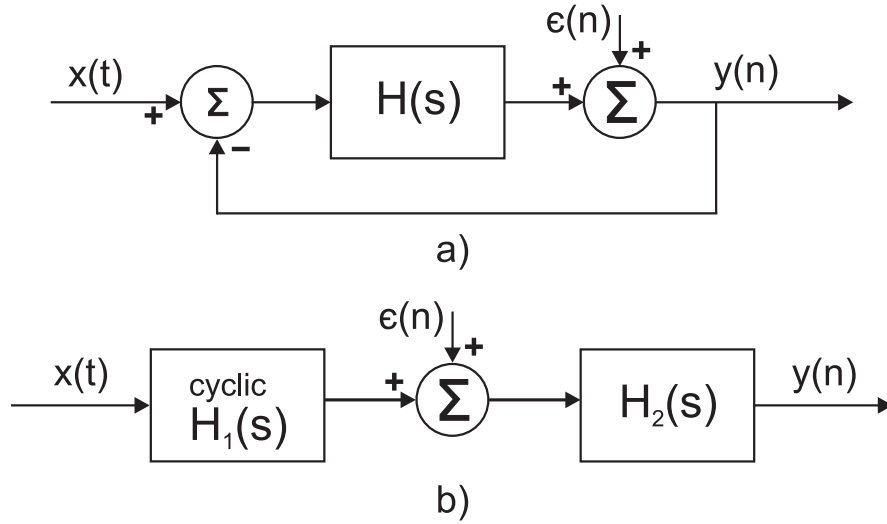


Figure 2.11: First order Delta-Sigma (a) and FIR modulator (b) with an additive noise source for the quantizer.

so that the majority of it is moved out of the signal pass-band. Figure 2.11 a) shows this implementation. Notice that the quantizer was replaced by an additive noise source $\epsilon(n)$. Secondly, a high-pass filter can be implemented by using an explicit filter, such as a differentiator. This is depicted by $H_2(s)$ in figure 2.11 b). For the two modulator topologies two transfer functions can then be written: a signal transfer function from the input to the output (STF), and a noise transfer function (NTF) from the input of the noise to the output. These are given for the delta-sigma modulator as:

$$STF_{DSM}(s) = \frac{y(n)}{x(t)} = \frac{H(s)}{1 + H(s)}, \quad (2.14)$$

$$NTF_{DSM}(s) = \frac{y(n)}{\epsilon(n)} = \frac{1}{1 + H(s)}. \quad (2.15)$$

In the same way we have for the FIR modulator:

$$STF_{FIR}(s) = \frac{y(n)}{x(t)} = H_1(s)H_2(s), \quad (2.16)$$

$$NTF_{FIR}(s) = \frac{y(n)}{\epsilon(n)} = H_2(s). \quad (2.17)$$

Equation 2.15 shows that if the quantization noise is to be suppressed in the baseband, $H(s)$ must have a large gain. As a result Equation 2.14 will become unity and the input signal passes the modulator un-attenuated. Equation 2.15 will then implement a

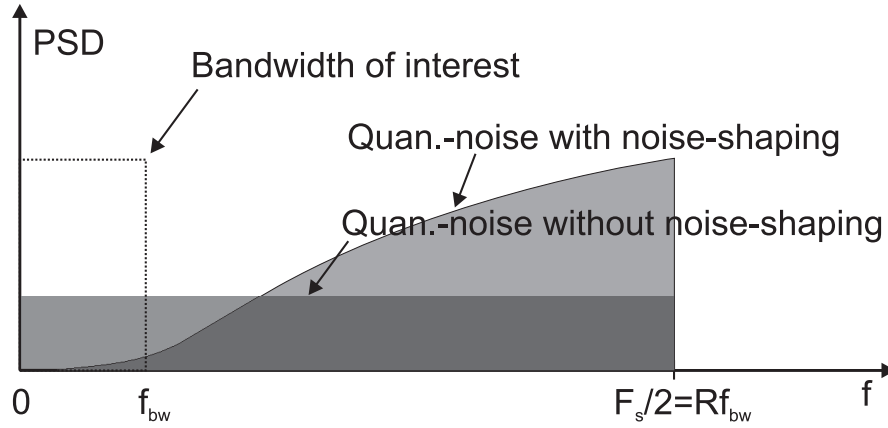


Figure 2.12: Spectrum at the output of an oversampling A/D converter: with and without noise-shaping. Note that the area under both curves is the same.

high-pass filter which shapes the quantization noise introduced by the quantizer. This is depicted in Figure 2.12 which shows that noise shaping can further attenuate the quantization noise in the band of interest, f_{bw} . In the case of the FIR modulator $H_2(s)$ should attenuate the quantization error with a high-pass filter. For the STF to be unity, $H_1(s)$ should ideally be the inverse of $H_2(s)$. It is important to note that the total noise level remains the same; noise shaping only pushes the quantization noise to higher frequencies where they can then be removed by an appropriate filter. There are various transfer functions for $H(s)$ that can realize a high gain in the feed-forward path of figure 2.11 a). One class using an integrator is especially suited for VLSI implementation as the analog circuits required to implement the transfer function are simple and robust. The same applies to the FIR modulator, where $H_1(s)$ is a cyclic continuous-time integrator and $H_2(s)$ a high-pass filter or differentiator. The reason for choosing a cyclic integrator is due to the lack of feedback in the FIR modulator. As will be shown later, a voltage-controlled oscillator can realize such a cyclic integrator.

2.2.3 Limit Cycles and Idle Tones

The performance modeling criteria in section 2.2.1 designated the noise process as white, which means that the noise power is uniformly distributed between $[-\frac{F_s}{2}, \frac{F_s}{2}]$. This is the basis for equation 2.12 which is used to predict the resolution of the various delta-sigma modulator topologies. This assumption is suitable for most busy input signals. However, for dc or slowly varying inputs, the white-noise model is far from

exact as the quantization error will be heavily correlated with the input signal [van Engelen and van de Plassche, 1999, p.8]. When the input signal is dc, the delta-sigma modulator output will bounce between two levels keeping its mean equal to the input signal. For certain dc input values the output sequence will be repetitive [Friedman, 1988]. If the repetition frequency lies in the signal band, the modulation will be noisy, if not, it will be quiet. Repetitive patterns that are present in the output of the modulator under zero input conditions are called idle patters. For example, the periodic pattern of $[1, -1, 1, -1, 1, -1, \dots]$ is defined as a first-order limit cycle [Magrath and Sandler, 1995, p.846]. Idle patterns are a result of limit cycles. These limit cycles create tones in the frequency spectrum. In general, a dc input signal can be expressed as a vulgar fraction, $A_{dc} = \frac{n}{d}$, with $\gcd(n, d) = 1$. Then, the repetition frequency, F_R , for a first-order sigma delta modulator is given by [van Engelen and van de Plassche, 1999, p.46]:

$$F_R = \begin{cases} \left(1 - n\frac{2A_{dc}}{q}\right)\frac{1}{2}F_s & n \text{ odd} \\ \left(n\frac{2A_{dc}}{q}\right)\frac{1}{2}F_s & n \text{ even} \end{cases} \quad (2.18)$$

The low frequency repetitions in the output of a first-order delta-sigma modulator due to small dc-inputs cause a deviation in the signal-to-noise ratio as expressed by equation 2.26. This is due to the repetition frequencies residing within the band of interest, f_{bw} , over which the signal-to-noise ratio is calculated. As a result, for a constant sampling frequency, F_s , the quantization noise power will be a strong function of the power of the input signal. As will become apparent later, FIR modulators experience also idle tones and limit cycles which are equivalent to the idle tones and limit cycles in conventional Delta-Sigma topologies. However, since no feedback is involved in FIR modulators, these FIR topologies have no infinite filter response. Chapter 3 will treat the spectral behavior of FIR modulators in more detail.

2.3 Delta-Sigma Topologies

The two most commonly found delta-sigma modulators implement either a low-pass or a band-pass, depending on the desired application. These two architectures are analyzed in the next two sections. The methods used here are partially applicable to the analysis

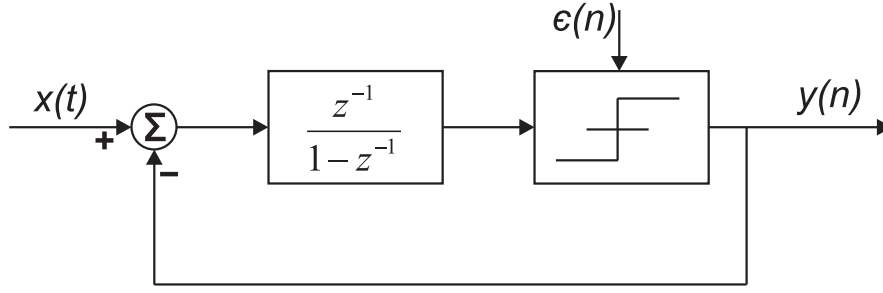


Figure 2.13: First-order low pass delta-sigma modulator with a 1-bit quantizer

of the [FIR](#) modulators which are covered in chapter 3.

2.3.1 Delta-Sigma Low Pass

If the signal of interest extends to dc then a low-pass modulator topology should be utilized. A discrete first-order low-pass delta-sigma modulator is shown in Figure 2.13. The filter $H(z)$ was replaced with a one unit delay discrete-time integrator [[Norsworthy et al., 1997](#), pp.5ff]. For the following analysis the quantizer was replaced with an additive noise source and a gain of unity. More accurate models for a 1-bit quantizer would include not only a time invariant gain λ but also a phase uncertainty. The reader is referred to [[van Engelen and van de Plassche, 1999](#)] which includes both parameters for a stability analysis of delta-sigma converters. By straightforward analysis of the system in Figure 2.13 the following signal and noise transfer functions, $STF(z)$ and $NTF(z)$, are obtained:

$$STF(z) = \frac{y(n)}{x(t)} = z^{-1}, \quad (2.19)$$

$$NTF(z) = \frac{y(n)}{e(n)} = 1 - z^{-1}. \quad (2.20)$$

Clearly, the signal transfer function only introduces a unit delay and leaves the signal unaltered, whereas the noise transfer function high-pass filters the introduced quantization noise. Under the assumption that the quantization noise is white with power $S(f)$, the total noise power in the range of $[0..f_{bw}] = [0..F_s/2R]$ is given as:

$$P_{total} = \int_{-f_{bw}}^{f_{bw}} S^2(f) |NTF(z)|^2 df = \int_{-f_{bw}}^{f_{bw}} \frac{q^2}{12 F_s} |NTF(z)|^2 df. \quad (2.21)$$

Here, F_s is the sampling frequency, f_{bw} the band of interest, and $S(f)$ is the level of the noise power spectral density given by equation 2.13. With the help of equation 2.20, the magnitude squared of an L^{th} noise transfer function is given by:

$$\begin{aligned} |NTF(e^{2\pi jf/F_s})|^{2L} &= |1 - e^{-2\pi jf/F_s}|^{2L} \\ &= \left| \sin\left(\frac{\pi f}{F_s}\right) 2je^{-\pi jf/F_s} \right|^{2L} \\ &= \left[2\sin\left(\frac{\pi f}{F_s}\right) \right]^{2L}. \end{aligned} \quad (2.22)$$

Making the assumption that, $f_{bw} \ll F_s$, one can approximate $\sin(\pi f/F_s)$ with $(\pi f/F_s)$. With this approximation we can re-write the integral in Equation 2.21 as a function of the sampling frequency, F_s , the oversampling ratio, R , and quantizer step, q :

$$\begin{aligned} P_{total} &= \int_{-f_{bw}}^{f_{bw}} \frac{q^2}{12F_s} \left[2\left(\frac{\pi f}{F_s}\right) \right]^{2L} df \\ &= \frac{q^2}{12} \left(\frac{\pi^{2L}}{2L+1} \right) \left(\frac{1}{R^{2L+1}} \right). \end{aligned} \quad (2.23)$$

In the case of a converter with b quantization bits, the *rms*-value of the maximal signal amplitude which does not cause the quantizer to overload is given as:

$$V_{A_{rms}} = 2^b \frac{q}{2\sqrt{2}}. \quad (2.24)$$

For a sinusoidal input signal the input power is then given as:

$$P_{sig} = (V_{A_{rms}})^2 = \frac{q^2 2^{2b}}{8}. \quad (2.25)$$

Utilizing Equation 2.23 and Equation 2.25 the signal-to-noise ratio can be obtained. The signal-to-noise ratio for an L^{th} order low-pass modulator with an oversampling ratio R and an b -bit quantizer is given as the ratio of the signal power and the noise power resulting in:

$$\begin{aligned} SNR_{dB} &= 10\log\left(\frac{P_{sig}}{P_{total}}\right) \\ &= 10\log\left(\frac{q^2 2^{2b}}{8}\right) - 10\log\left(\frac{q^2}{12} \left(\frac{\pi^{2L}}{2L+1}\right) \left(\frac{1}{R^{2L+1}}\right)\right) \\ &= 10\log\left(\frac{3}{2} R^{2L+1} \frac{2L+1}{\pi^{2L}} 2^{2b}\right). \end{aligned} \quad (2.26)$$

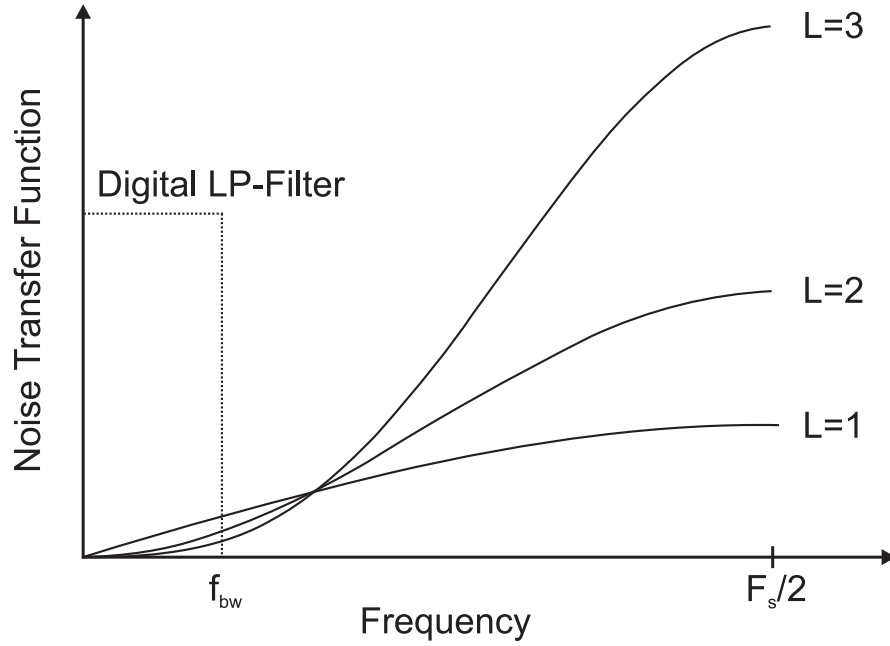


Figure 2.14: First, second, and third order low-pass noise transfer functions.

Equation 2.26 shows that for each doubling of R the signal-to-noise ratio improves by 9dB for a first-order low-pass with 1-bit quantizer. Mainly, 3dB are achieved due to oversampling and 6dB are achieved due to noise shaping. For an order L modulator the noise falls by $3(2L+1)$ dB for every doubling of R . This is depicted in Figure 2.14 which shows the attenuation of the noise in the band of interest which can be achieved for higher order noise transfer functions. Note, that compared to the first order sigma delta noise transfer function, higher order noise transfer functions provide more quantization noise suppression over the low frequency signal band and more amplification of the noise outside the signal band.

2.3.2 Delta-Sigma Band Pass

So far, it was assumed that the sampling frequency, F_s , is much greater than the Nyquist rate. For low-pass signals, the highest frequency component is also the signal bandwidth f_{bw} . If a signal with bandwidth f_{bw} is narrow band but is located at a center frequency of f_c , its highest frequency component is now $f_c + f_b$. If f_c is large, choosing the sampling frequency much greater than the highest frequency component as in the low-pass case will yield unreasonable large sampling frequencies. Therefore, for bandpass modulation the sampling frequency is chosen to be much higher than the bandwidth of the

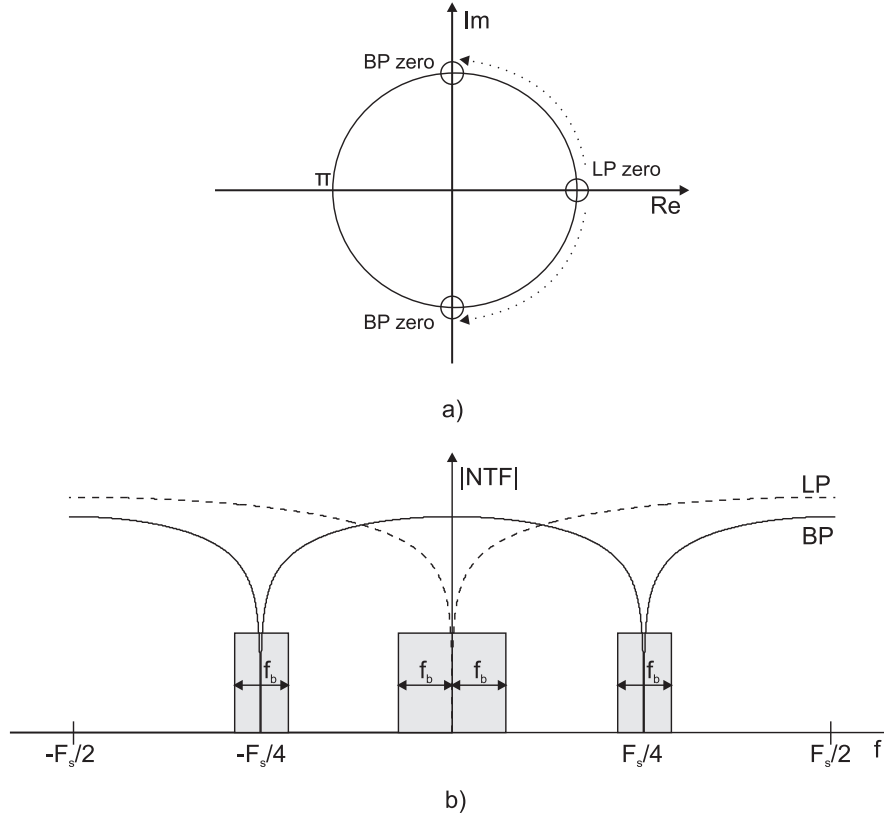


Figure 2.15: Low-pass to band-pass transformation: a) transformation of the NTF zeros b) resulting NTF spectrum

signal, rather than its highest frequency component [Jayaraman et al., 1997; Raghavan et al., 2001b]. The oversampling ratio is then given as $R = \frac{F_s}{2(f_{max} - f_{min})}$ [Norsworthy et al., 1997, p.286]. The simplest way to design a bandpass modulator is to start with a low-pass modulator and apply a lowpass-to-bandpass transformation. For instance, applying the $z^{-1} \rightarrow -z^{-2}$ transformation maps the zeros from dc to $\pi/2$. This transformation is particularly attractive as it does not affect the dynamics of the prototype low-pass modulator [Norsworthy et al., 1997, p.286]. The transformation has effectively doubled the number of zeros of the low-pass noise transfer function and rotated these zeros in the z -plane from $z = 1$ to $z = j$, as depicted in Figure 2.15. In the frequency domain, the noise suppression region has been shifted from dc to $\pm F_s/4$. Another transformation is the $z \rightarrow \frac{z+a}{az+1}$, $-1 \leq a \leq 1$ transformation which gives full control over passband location but does not preserve modulator dynamics [Norsworthy et al., 1997, p.287]. Note that the order of real band-pass modulators refers to the number of poles in the noise transfer function. With this definition, a fourth-order modulator has only two zeros in

the noise transfer function and the quantization noise is only suppressed with a second-order transfer function in the signal passband. Thus, the order of a band-pass modulator is defined as $2L$. The signal-to-noise ratio of a bandpass modulator can be estimated in the same manner as in the case of a low-pass modulator. If the $z^{-1} \rightarrow -z^{-2}$ transformation is extended to the L^{th} order noise-transfer function of a low-pass architecture, the resulting magnitude squared of the noise transfer function is given as:

$$\begin{aligned} |NTF(e^{2\pi jf/F_s})|^{2L} &= |1 + e^{-4\pi jf/F_s}|^{2L} \\ &= \left| \cos\left(2\frac{\pi f}{F_s}\right) 2je^{-2\pi jf/F_s} \right|^{2L} \\ &= \left[2\cos\left(2\frac{\pi f}{F_s}\right) \right]^{2L}. \end{aligned} \quad (2.27)$$

The quantization noise power over the frequency band of $F_s/4 \pm f_{bw}$ is given as:

$$\begin{aligned} P_{total} &= \int_{-\frac{F_s}{4} + \frac{f_{bw}}{2}}^{-\frac{F_s}{4} - \frac{f_{bw}}{2}} N(f) |NTF(z)|^2 df + \int_{\frac{F_s}{4} - \frac{f_{bw}}{2}}^{\frac{F_s}{4} + \frac{f_{bw}}{2}} N(f) |NTF(z)|^2 df \\ &= 2 \int_{\frac{F_s}{4} + \frac{f_{bw}}{2}}^{\frac{F_s}{4} - \frac{f_{bw}}{2}} N(f) |NTF(e^{2\pi jf/F_s})|^2 df \\ &= 2 \int_{\frac{F_s}{4} + \frac{f_{bw}}{2}}^{\frac{F_s}{4} - \frac{f_{bw}}{2}} \frac{q^2}{12F_s} \left[2\cos\left(2\frac{\pi f}{F_s}\right) \right]^{2L} df \end{aligned} \quad (2.28)$$

If it is assumed that $\frac{2f_{bw}}{F_s} \ll 1$ with f_{bw} as defined in Figure 2.15 then Equation 2.28 can be re-written to:

$$\begin{aligned} P_{total} &= 2 \int_{-\frac{f_{bw}}{2}}^{\frac{f_{bw}}{2}} \frac{q^2}{12F_s} \left(2\sin\left(2\frac{\pi f}{F_s}\right) \right)^{2L} df \\ &= 2 \int_{-\frac{f_{bw}}{2}}^{\frac{f_{bw}}{2}} \frac{q^2}{12F_s} \left[2\left(2\frac{\pi f}{F_s}\right) \right]^{2L} df \\ &= \frac{q^2}{12} \left(\frac{\pi^{2L}}{2L+1} \right) \left(\frac{1}{R^{2L+1}} \right). \end{aligned} \quad (2.29)$$

As expected, Equation 2.29 is identical to Equation 2.23 because the noise suppression in a $2L^{th}$ order band-pass modulator is the same as the one in a L^{th} order low-pass modulator. Thus the signal-to-noise ratio in decibels for a $2L^{th}$ band-pass modulator with b-bit quantizer and oversampling ratio R is given as:

$$SNR_{dB} = 10 \log \left(\frac{3}{2} R^{2L+1} \frac{2L+1}{\pi^{2L}} 2^{2b} \right). \quad (2.30)$$

Both modulator topologies, band-pass and low-pass need decimation to lower the frequency and filter out the noise-shaped quantization noise.

2.3.3 The Concept of Decimation

To obtain a high-resolution signal from the low-bit stream from the output of the n -bit quantizer, decimation or averaging is used. Furthermore, decimation is needed to lower the data rate of the oversampled modulator. As was shown in figure 2.12, a key point of a delta-sigma and FIR converters is that the quantization noise spectrum is shaped in such a way as to place most of the noise power outside the signal band. To remove the quantization noise low-pass filters are used. However, appropriate filters tend to be difficult to realize at the elevated sampling rates of the modulator [Norsworthy et al., 1997, p.28]. As a result, decimation is needed to lower the bit rate of sigma delta, modulation and convert it to a form that is more suitable for processing and transmission [Crochiere and Rabiner, 1981]. The factor by which the rate is lowered is the decimation factor R , and is given as:

$$R = \frac{F_s}{F_d}, \quad (2.31)$$

where F_s is the elevated sampling frequency of the sigma delta modulator and F_d is the reduced sampling rate at the output of a decimator as shown in [Norsworthy et al., 1997, p.30]. A convenient filter for decimation is based on the *sinc* function [Presti, 2000]. The transfer function of the filter is given as:

$$H(z) = \frac{1}{R} \sum_{i=0}^{R-1} z^{-i}. \quad (2.32)$$

Conceptually, the filter computes an output by forming the sum of the contents of the registers. Decimators based on *sinc* filters are appropriate for decimating sigma delta modulation down to four times the Nyquist rate [Candy, 1986]. Further decimation usually requires filters that cut off more sharply at the edge of baseband [Candy, 1986]. An efficient way to realize a decimation filter is known as the Hogenauer structure and consist of a series of cascaded accumulators followed by a cascade of differentiator (CIC) [Hogenauer, 1981] as expressed by:

$$H(z) = \left(\frac{1 - z^{-M}}{1 - z^{-1}} \right)^L, \quad (2.33)$$

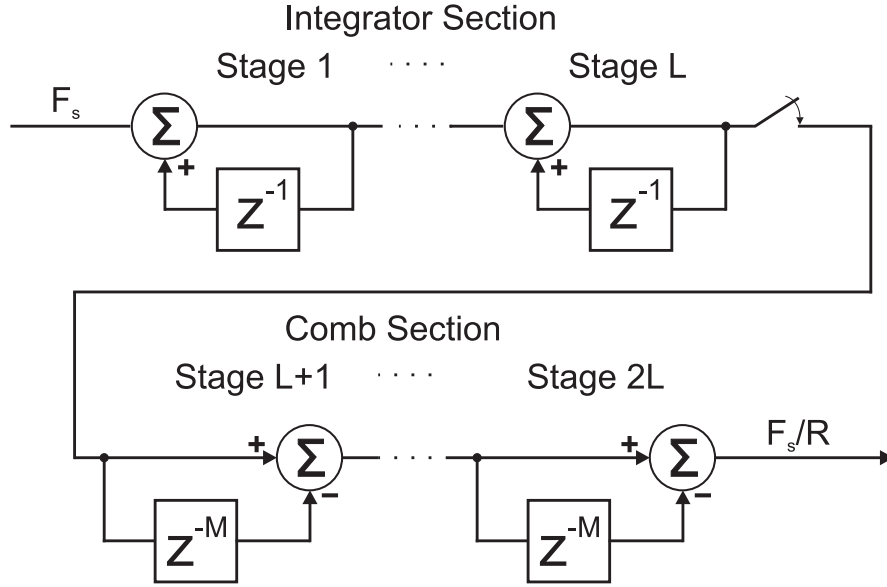


Figure 2.16: CIC decimation filter

where L is the order of the *sinc* filter. The Hogenauer structure is depicted in figure 2.16. With regard to overflow errors in all integrator stages, the two's complement binary format has two attractive characteristics. First, under certain conditions, overflow during the summation of two numbers causes no error. Second, with multiple summations, intermediate overflow errors cause no problems if the final magnitude of the sum of the b -bit two's complement numbers is less than 2^{b-1} ([Lyons, 2004], section 12.1.5). Thus, a composite CIC filter would compute correct filter outputs provided the additions were performed with 2's-complement arithmetic and provided the bit field width of the accumulator exceeded the word width required by the final output sequence. The required bit width is the number of bits in the input data words plus the number of bits required to accommodate the maximum filter gain. Then the most significant bit at the output of the filter is ([Hogenauer, 1981], equation 11):

$$B_{max} = [N \log_2(RM) + B_{in} - 1] \quad (2.34)$$

With a bit width as expressed by equation 2.34, the accumulators can successfully recover from internal overflow.

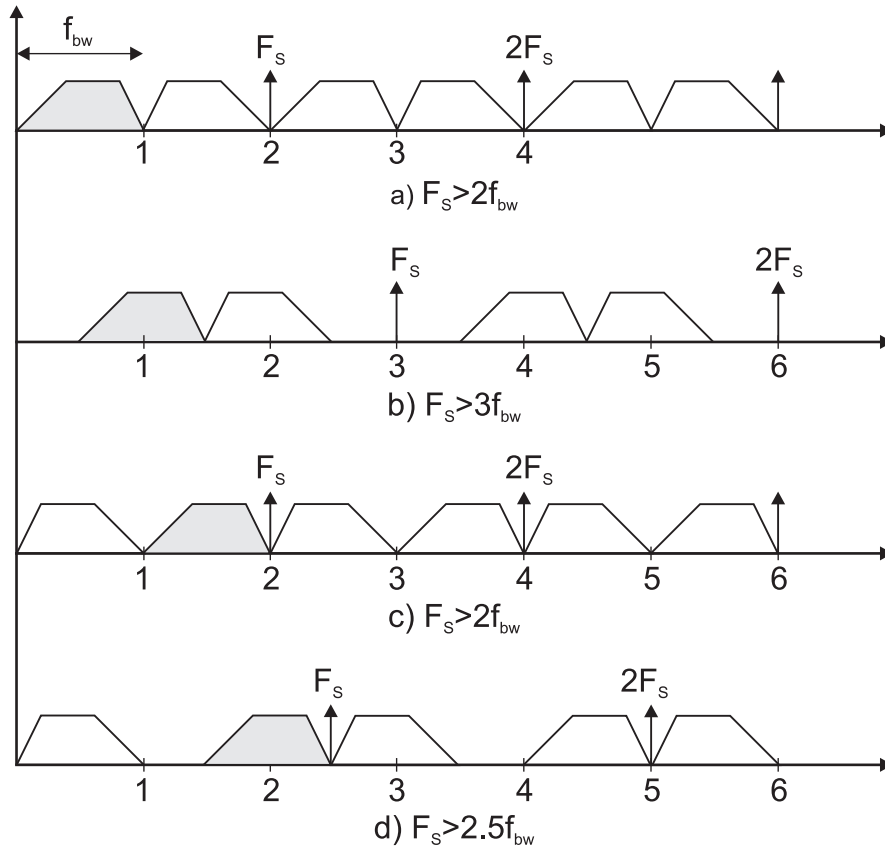


Figure 2.17: Illustration of undersampling various signals with different bands of interest.

2.3.4 The Concept of Undersampling

Undersampling is sampling at a rate below the [Nyquist](#) frequency, which generally implies a loss of information, unless the signal bandwidth, f_{bw} is restricted to less than $F_s/2$. For signals which do not extend to dc, however, the minimum required sampling rate is a function of the bandwidth of the signal, $2f_{bw}$, as well as its position in the frequency spectrum [[Analog Devices, 1998](#)], [[Vaughan et al., 1991a](#)]. When such a signal is undersampled, the aliased products can be used to translate the input signal down to baseband for further processing. The minimum required sampling frequency, F_s , will vary with the signals maximum frequency, F_{max} , and its bandwidth, f_{bw} . This can be illustrated with the help of figure 2.17 [[Analog Devices, 1998](#)]. In part a) of the figure, the signal occupies a band from dc to 1MHz, and therefore must be sampled at greater than 2MSPS. The second case shown in part b) shows a 1MHz signal which

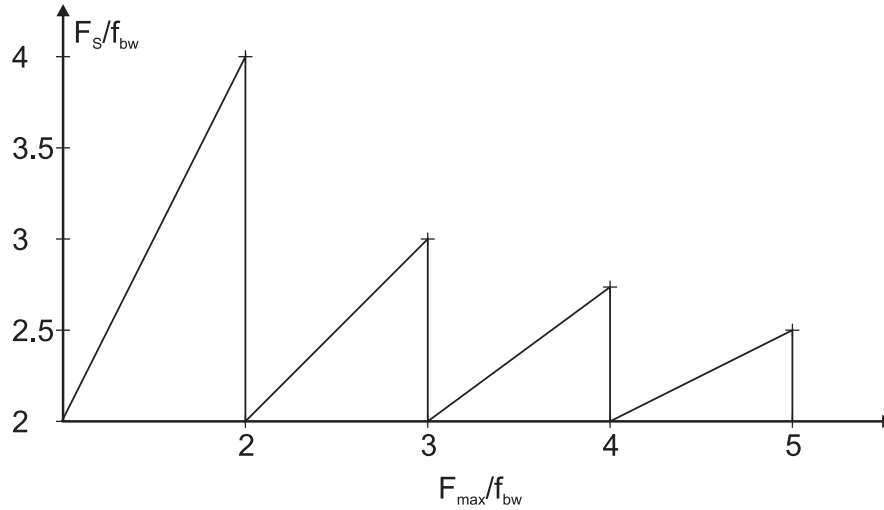


Figure 2.18: Minimum required sampling frequency as a function of the maximum signal frequency.

occupies the band from 0.5 to 1.5MHz. Now this signal must be sampled at a minimum of 3MSPS. In the third case, shown in part c), the signal occupies the band from 1 to 2MHz, and the required sampling rate for no aliasing reduces back to 2MSPS. In part d) of figure 2.17 the signal occupies the band from 1.5 to 2.5MHz. This signal must be sampled at a minimum of 2.5MSPS. Generalizing this analysis will lead to figure 2.18. The actual minimum required sampling rate is a function of the ratio of the highest frequency component, F_{\max} , to the total signal bandwidth, f_{bw} . For large ratios of F_{\max} to the bandwidth, f_{bw} , the minimum required sampling frequency approaches $2f_{bw}$ [Vaughan et al., 1991a]. As a result, undersampling can be used to down-convert a signal residing at a high frequency to baseband where it can be processed further. This methodology will later be used in the FIR analog-to-digital modulator to down-convert a high frequency signal. That is, the narrow-band frequency modulated output of an oscillator is undersampled and digitized directly. A novel scheme will be proposed which reduces the requirements on the sampling circuitry as undersampling is performed, while still not suffering any drawbacks due to undersampling or spectral reversal common to conventional amplitude undersampling applications.

2.4 *Higher Order Delta-Sigma Architectures*

To achieve higher noise shaping of the introduced quantization error in the A/D conversion, higher order noise shaping architectures are utilized along with multi-bit quantization [Chao et al., 1990; Khoini-Poorfard et al., 1997; Kozak et al., 2000]. While there is an abundance of modulator topologies utilizing higher order loop filters [Brandt and Wooley, 1991; Leslie and Singh, 1990; Hairapetian and Temes, 1994], most of them fall into three categories. These are single-loop low order designs, single-loop high order designs or multi-loop designs. A detailed summary outlining the advantages and drawbacks of each topology can be found in [Norsworthy et al., 1997, p.166] and [Ribner, 1991]. As this work is concerned with low-order modulator architectures, the main focus is on multi-loop designs as these are comprised out of multiple low order single-loop topologies. Since FIR modulators do not have a feedback path, a cascaded approach of multiple first-order FIR modulators is a good way to improve noise performance. Cascaded architectures are reviewed next with emphasis on the later presented FIR modulators.

2.4.1 Cascaded

A simple solution to stability problems of higher order single loop topologies was suggested by Hayashi et al. [Hayashi et al., 1986]. In their work they proposed the use of multiple first-order stages instead of a single high order loop filter to reduce quantization errors. This principle is referred to as multi-stage noise shaping (MASH) or a cascaded topology. The principle of cascaded sigma-delta modulation is based on the use of multiple sigma-delta modulator stages in a cascade configuration [Matsuya et al., 1987]. In ideal multi stage architectures, each successive stage accepts the quantization noise of the preceding stage as its input in order to create a digital signal which perfectly cancels out the quantization error introduced in the preceding stage [Longo and Copeland, 1988]. A basic second-order cascaded topology is depicted in figure 2.19. As shown in the figure, two conventional first-order delta-sigma modulators utilizing feedback are utilized to realize a second order structure. Both first-order modulators

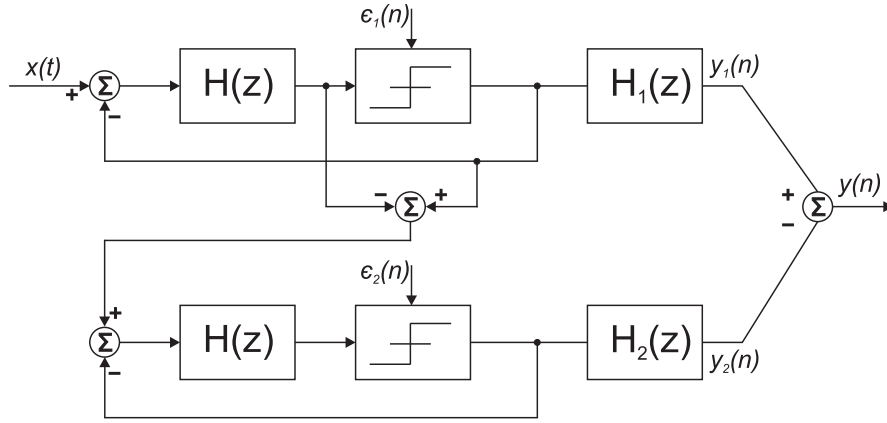


Figure 2.19: Second-order cascaded modulator topology based on two first-order delta-sigma converters.

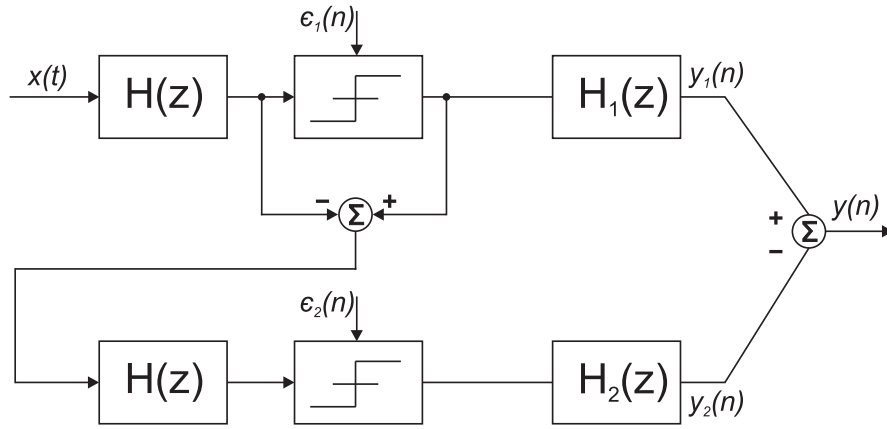


Figure 2.20: Second-order cascaded modulator topology based on two first-order FIR delta-sigma converters.

need negative feedback to shape the quantization noise out of the band of interest. Later it will be shown how a similar second order system can be realized without the need for negative feedback. A simplified version of this scheme of cascaded **FIR** modulators is shown in figure 2.20. A brief analysis of figure 2.19 shows that the output $y(n)$ is given as:

$$Y(z) = [X(z)STF(z) + \epsilon_1(z)NTF(z)]H_1(z) - [\epsilon_1(z)STF(z) + \epsilon_2(z)NTF(z)]H_2(z) \quad (2.35)$$

The goal is to cancel the coarse quantization error ϵ_1 . This occurs when:

$$\epsilon_1(z)NTF(z)H_1(z) = \epsilon_1(z)STF(z)H_2(z). \quad (2.36)$$

The noise-transfer function and the signal transfer functions for $H(z) = \frac{1}{1-z^{-1}}$ were given in section 2.3.1 as $NTF(z) = 1 - z^{-1}$ and $STF = z^{-1}$. Then we can re-write equation

2.36 as:

$$\begin{aligned}\frac{NTF(z)}{STF(z)} &= \frac{H_2(z)}{H_1(z)} \\ \frac{1 - z^{-1}}{z^{-1}} &= \frac{H_2(z)}{H_1(z)}.\end{aligned}\tag{2.37}$$

Thus, choosing $H_1(z) = z^{-1}$ and $H_2(z) = 1 - z^{-1}$ will cancel ϵ_1 and leave the output of:

$$Y(z) = z^{-2}X(z) + \epsilon_2(z)(1 - z^{-1})^2\tag{2.38}$$

As a result, in the MASH topology the quantization error has been improved without increasing the order of the loop filter. However, the topologies are sensitive to the analog accuracy of implementation, typically limiting the resolution of analog-to-digital conversion to less than 14 bits, regardless of the order of the noise shaping [Cauwenberghs and Temes, 2000]. To circumvent this, calibration methods can be applied to in the digital domain to correct for analog imprecision, trading a small increase in the implementation complexity of the digital part for a significant increase in effective analog precision[Cauwenberghs and Temes, 2000; Kiss et al., 2000].

2.5 Summary

This chapter introduced the important concepts forming the foundation for the following chapters. The most vital aspects of every delta-sigma modulator, namely oversampling, quantization, noise shaping, and decimation were reviewed and can now be used to realize different A/D topologies. Also, other well established principles such as under-sampling and higher order delta-sigma topologies were re-introduced, giving the tools needed to fully appreciate the following chapters.

CHAPTER III

FIRST-ORDER FIR SIGMA DELTA MODULATORS

3.1 *Introduction and Review*

While oversampling discrete-time (DT) and continuous-time (CT) analog-to-digital (A/D) modulators have widely been used for high resolution applications, they are almost exclusively synonymous with feedback. Generally, any type of feedback is applied in order to control the dynamic behavior of a system, to ensure stability, improve linearity, and compensate for the effect of disturbances [Franklin et al., 2006]. More importantly, in delta-sigma A/D converters the negative feedback path also realizes the quantization noise suppression in the signal band as shown in section 2.2.2. So why would we want to remove feedback from a system?

- Feedback entails having to deal with undesirable effects such as excess loop delay as in continuous time delta-sigma A/D converter [W. Gao and Snelgrove, 1997]. Ideally, the feedback digital-to-analog converter's currents respond immediately to the quantizer's clock edge, but the non-zero transistor switching time of the latched comparator (quantizer) and the digital-to-analog converter result in a finite delays [J.A. and W.M., 1999]. Excess loop delay will shift the poles of the noise transfer function and will therefore change the characteristic of the noise shaping or make the overall modulator unstable.
- Another problem encountered with multi-bit digital-to-analog converters in the feedback path is their inherent nonlinearity. Non-linearity of the quantizer (A/D) of the modulator in the feed-forward loop is reduced by the gain of the loop. However, non-linearity in the feedback D/A converter is a serious problem since this nonlinearity directly feeds into the input [Wang et al., 2001].
- Limit-cycles, inherent to systems with feedback, might cause instability

[Reefman et al., 2005; Tao et al., 1999a] in the modulator.

- Feedback increases also the system complexity due to extra circuit components such as the digital-to-analog converter in the feedback path [Norsworthy et al., 1997]. Furthermore, in many systems feedback is simply not possible as no path exists.

As a result, delta-sigma converters without feedback are an interesting alternative to conventional topologies. As introduced in Section 2.2.1, delta-sigma A/D converters without feedback are based on frequency modulators followed by frequency-to-digital converters. The work on frequency-to-digital converters for delta sigma converters commenced in the early 90's. However, most of the methods used in these works are based upon well established frequency demodulation techniques. Different research groups have worked on the topic of frequency-to-digital converters since then, realizing different implementations with and without feedback. While there are a wide variety of publications on delta-sigma converters utilizing frequency modulation and demodulation techniques, three university groups have taken interesting yet different approaches to realize these modulators based in some form of frequency modulation and demodulation. One group in particular, is lead by Professor Ian Galton at the University of California, San Diego and includes William Huff, Paolo Carbone, and Eric Siragusa. Their implementation of a second order delta-sigma frequency-to-digital converter is presented in [Ian Galton and Siragusa, 1998]. There, a second-order modulator utilizing feedback is realized. Hence, the previous mentioned comments on using negative feedback apply. This topology which is depicted in Figure 3.1 a) simultaneously performs frequency demodulation and digitization. The topology presented is based on phase-locked loops and uses analog circuitry such as a charge-pump and a digital counter to realize two integrators. Figure 3.1 a) depicts the second-order delta-sigma PLL. As can be seen from the figure, the topology operates on a hard-limited version of the frequency modulated input signal and generates a 2-bit output sequence. Thus, the performance is equivalent to a conventional second order delta-sigma modulator. Note, that the topology requires an already generated frequency modulated input signal, $x(t)_h$. That is, no

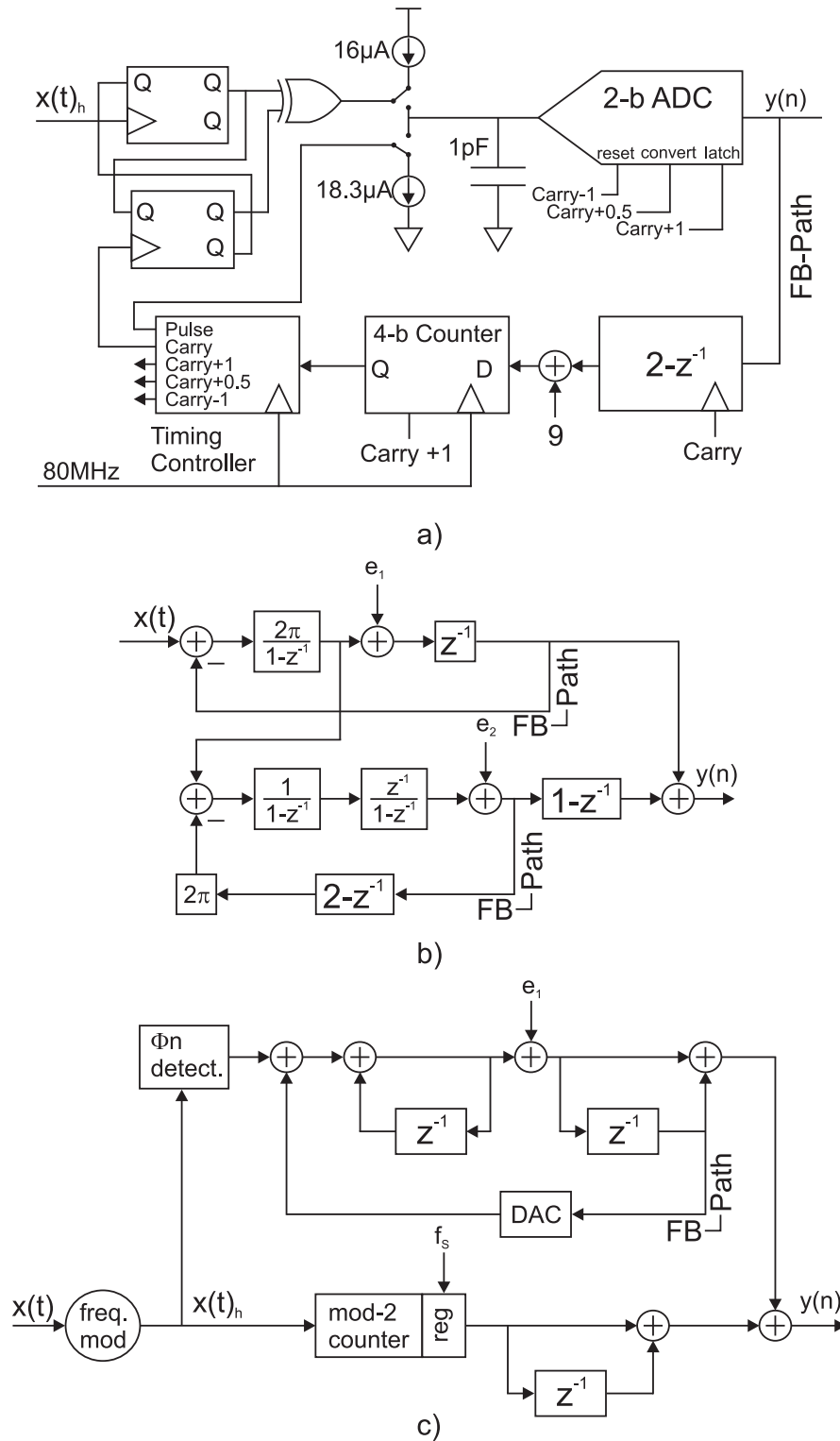


Figure 3.1: The three most important existing topologies. Figure a) shows the works of [Ian Galton and Siragusa, 1998], figure b) the works of [Thomas A. D. Riley and Plett, 1998], and figure c) the works of [Hovin et al., 1997].

frequency modulation is performed by the circuit. While excellent performance results are achieved, the overall complexity of the system is quite high, even more so when including a frequency modulation unit. Furthermore, a non-uniform to uniform decimation filter is required as the overall topology samples the FM signal asynchronously. This decimation filter will increase the complexity of the topology further. Follow-up publications to this work include [Izadi and Leung, 2002] and [Sharifkhani, 2004].

A second research group consists of Walt T. Bax, Thomas A. D. Riley, Miles A. Copeland, Tom A. D. Riley, Norman M. Filiol and Calvin Plett at Carleton University, Ottawa in Canada. Their realization of a delta-sigma frequency-to-digital converter is based on two delta-sigma phase-locked loops as described in [Thomas A. D. Riley and Plett, 1998] and shown in Figure 3.1 b). As can be seen from the figure this topology mimics a 1-2 cascade typically found with conventional delta-sigma converters. The first stage integrates the input signal to convert the frequency content of the FM signal to phase. The signal content and error due to quantization are then fed into the second stage. Both stages need feedback to realize noise-shaping as explained in section 2.2.2 and hence increase circuitry complexity. Furthermore, the topology requires frequency dividers to down-convert the FM input signal to the reference clock. Again, the topology presented performs no frequency modulation. Another implementation utilizing a phase-locked loop and a frequency divider is described in [Riley et al., 1993].

Finally, the research group at the University of Oslo in Norway comprising out of Dag T. Wisland, Mats E. Hovin and Tor S. Lande introduced yet another version of a delta-sigma frequency-to-digital converter [Hovin et al., 1997; Wisland et al., 2002, 2003]. Their implementation is, however, different from the approach the other research groups took as the delta-sigma frequency-to-digital converter is implemented without feedback, thus, resulting in a more efficient modulator implementation. This topology is shown in Figure 3.1 c). Their topology could be realized by utilizing the frequency de-modulation technique patented by Akira Sogo in [Sogo, 1989]. The demodulation scheme provided by Akira Sogo in conjunction with an oscillator approach to perform

frequency modulation and a 1-1 cascade similar to conventional delta-sigma modulators thus realizes an efficient scheme to frequency demodulate and digitize an FM signal. However, as depicted in figure 3.1 c) the second path of the 1-1 cascade still utilizes feedback.

While these are the most important publications there are many others that are utilizing voltage-to-frequency conversion also to realize delta-sigma topologies [Watanabe et al., 2003; Ravinuthula and Harris, 2004; Yang and Sarpeshkar, 2005; Pekau et al., 2006]. However, all of them utilize some sort of feedback to shape out quantization noise.

In this and the following chapters all feedback paths are removed while still realizing the noise-shaping characteristics synonyms to delta-sigma converters. Since these FIR modulators are based on frequency modulation and demodulation techniques, a brief review of these principles and how they can be used is given. Based on these principles various versions of FIR modulator topologies are presented and optimized. An overview of the presented structures and their simplifications is given in figure 3.2. Part a) of the figure shows a first-order FIR modulator where a VCO is used as a frequency modulator followed by an optional hard-limiter to rectify the frequency modulated signal. The frequency de-modulation technique proposed in [Sogo, 1989; Hovin et al., 1997] is given in the shaded region of figure 3.2 a). We simplified this topology by realizing that a simple asynchronous D-FF can realize a quantizer and differentiator at the same time. This simplification is depicted in figure 3.2 b) which shows a resetting D-FF followed by a *sinc* decimation filter. Alternatively, a resetting-counter can be utilized as depicted in figure 3.2 c). Furthermore, the concept of undersampling as introduced in Section 2.3.4 can be used with the counter from figure 3.2 c) or the implementation from figure 3.2 a), which alleviates the need for high clock frequencies. Utilizing a resetting counter in conjunction with undersampling will also eliminate the need for having to choose a certain sampling frequency. This will be outlined in later sections. Usually when utilizing undersampling the sampled signal must not cross an integer multiple of the sampling frequency $F_s/2$. Otherwise aliasing occurs. However, with

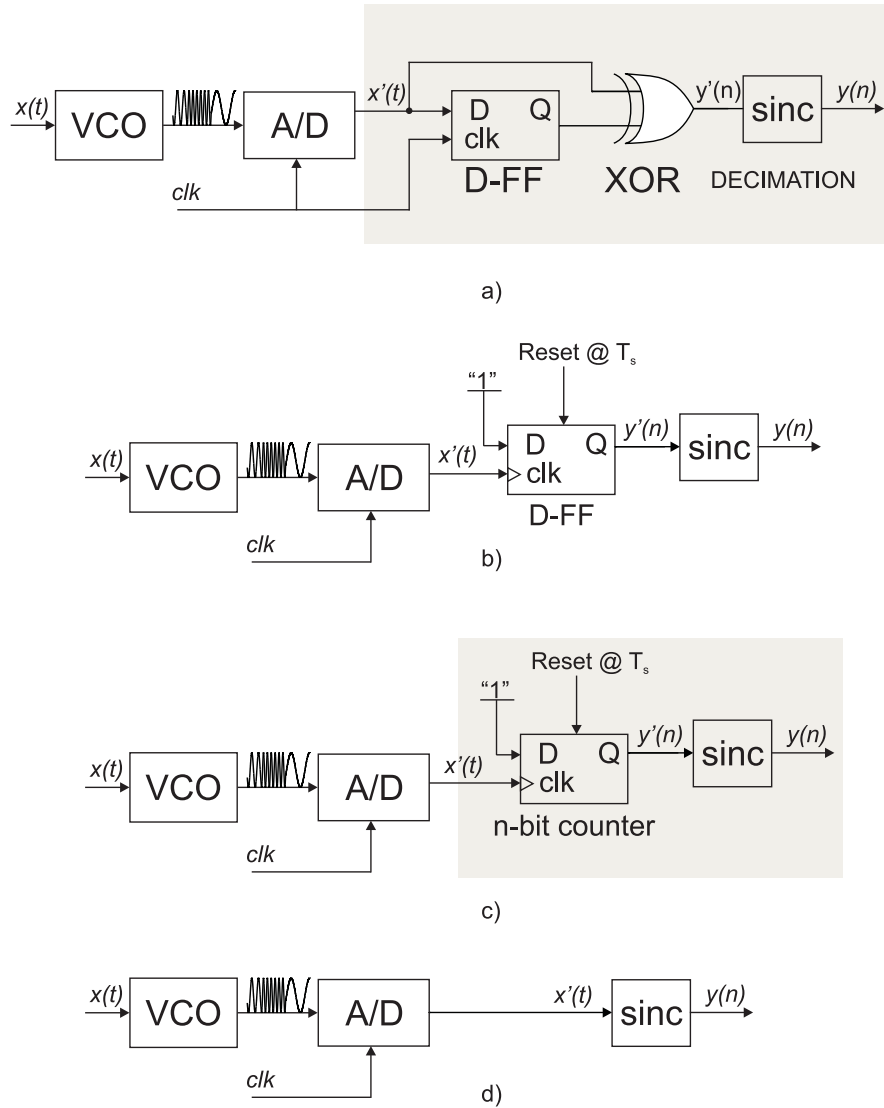


Figure 3.2: Part a) shows the topology adopted by [Hovin et al., 1997]. Part b) shows how we replaced the XOR gate and D-FF by a simple asynchronous D-FF, or more importantly, by a resetting counter as seen in part c). In part d) the counter was moved into the sinc decimation filter.

the counter this is not the case as it captures and retains all the frequency modulated signal edges in between sampling instances. As a result, this first-order topology as depicted in figure 3.2 c) is a marked departure from prior art. To further simplify the FIR modulators the counter from figure 3.2 c) can be absorbed into the decimation filter as shown in figure 3.2 d). However, this can only be done if the decimation filter is based on a cascade of integrators and differentiator. All simplified first-order FIR modulators are then analyzed in terms of non-linearities, phase noise, jitter, and meta-stability. Exact mathematical models are presented describing the noise suppression and hence the signal-to-noise ratio performance. Simulation examples are presented to give proof-of-concept and to discuss performance results. The performance is then compared to the mathematical model.

3.1.1 FIR SDM Principle

The principle behind all sigma delta converters is essentially the same: The analog input signal should pass undisturbed through the system and appear as a digital equivalent at the output. Quantization error introduced should be attenuated in the band of interest. Thus, the signal-transfer function should ideally be unity plus some delay, and the noise-transfer function a variation of an appropriate high pass filter. Conventional delta-sigma modulators, as the ones introduced in section 2.2.1, implement the noise shaping of the quantization error by using negative feedback. The negative feedback, however, is not needed as long as the system realizes a high pass characteristic for the introduced quantization noise, and lets the input signal through without attenuation or distortion. The scheme to realize this task is depicted figure 3.3, which shows the three stages needed: integration, quantization, differentiation. The figure shows that the input signal gets integrated, quantized, and then differentiated to arrive at the output unchanged. The quantization error introduced when quantizing the signal; however, does not experience integration and, therefore, only experiences differentiation, which is a first-order high pass filter as shown in figure 3.3. Thus the error gets noise shaped out

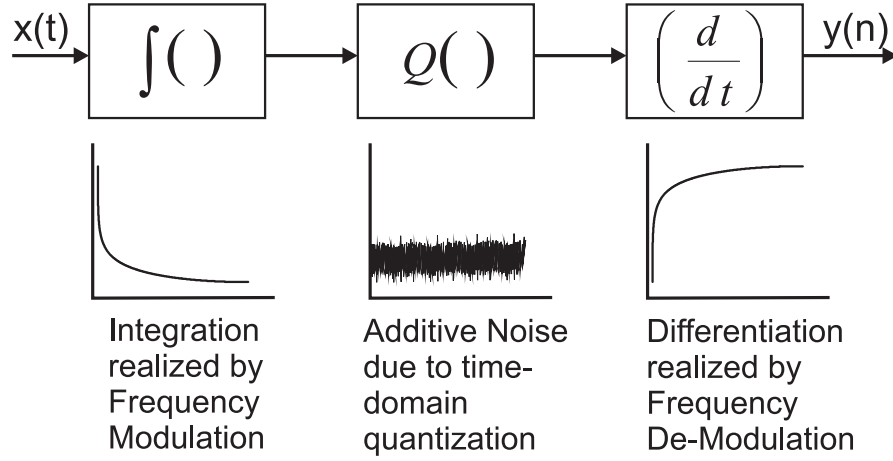


Figure 3.3: The three principal operations synonymous to delta-sigma modulators: integration, quantization which introduced quantization noise as shown, and differentiation proving noise shaping.

of the band of interest as in a conventional sigma delta modulator with negative feedback. To implement the topology shown in figure 3.3 we can borrow methods used from frequency modulators. More specifically, frequency modulation is used to implement integration as seen in figure 3.3. The frequency modulated signal is then time-domain quantized, followed by frequency-demodulation.

Frequency modulation is an important part of the FIR delta-sigma modulator as it performs a translation from the amplitude domain to the frequency domain. By this translation an integration of the modulation signal is performed. Generally, frequency modulation is used to facilitate transmission of information from a transmitter to a receiver [Armstrong, 1936]. In frequency modulation, the frequency of a carrier signal is varied in accordance with a modulating signal which contains the information. A typical frequency modulated signal can be expressed as:

$$y(t) = \cos[2\pi(f_c + kx(t))], \quad (3.1)$$

where $y(t)$ is the frequency modulated signal, f_c is the carrier frequency, k is the modulation index which controls the amount of frequency deviation, and $x(t)$ is the modulating signal. Frequency modulation can be implemented by numerous methods. A common way is to apply the modulating signal, $x(t)$, to a voltage-controlled oscillator. The output

frequency of a voltage-controlled oscillator is governed by:

$$\omega_{out} = \omega_c + K_{vco}x(t), \quad (3.2)$$

where K_{vco} is the gain of the VCO. In particular, since the phase is the integration of the frequency, the sinusoidal output of a VCO can then be expressed as:

$$y(t) = \cos\left(\omega_c t + K_{vco} \int x(t)dt + \phi_o\right). \quad (3.3)$$

Equation (3.3) shows that the voltage controlled oscillator acts as an integrator and that the output frequency of the VCO is a function of the input $x(t)$. The $\cos()$ function in equation (3.3) also shows that the VCO inherently performs a modulo 2π operation and will thus never saturate. The output of the VCO is hence a frequency-modulated signal whose frequency deviation of the carrier, ω_c , is proportional to the modulating input signal $x(t)$. The operation of the voltage controlled oscillator implementing frequency modulation is depicted in figure 3.4. The top part of the figure shows the modulating input signal, $x(t)$, in this case comprising of three different dc-inputs. The middle part of the figure represents the phase. Notice, that the frequency is the slope of the phase, or alternatively, the frequency is the derivative of the phase. The bottom part of the figure represents the output signal $y(t)$. As can be seen from the figure, the higher the input magnitude the faster the frequency at the output as given by equation (3.2). Thus, the information is encoded into the instantaneous frequency of the sinusoid, and more specifically, the zero crossings. The VCO can thus be used as the integrator depicted in figure 3.3. To quantize and differentiate the FM signal we again borrow methods used from FM de-modulators.

One way of demodulating the information is to use a discriminator, which converts the frequency modulation to amplitude modulation, which can be detected using an envelope detector [Chu, 1969]. Alternatively, a phase-locked-loop (PLL) can be used. A more simple solution to demodulate the frequency-modulated signal is to utilize the zero-crossings of the carrier sinusoid and/or the widths of each cycle period [Carlson et al., 2001]. An attractive way to demodulate a frequency modulated signal was first patented by Akira Sogo [Sogo, 1989]. His distinctive way of demodulating consists

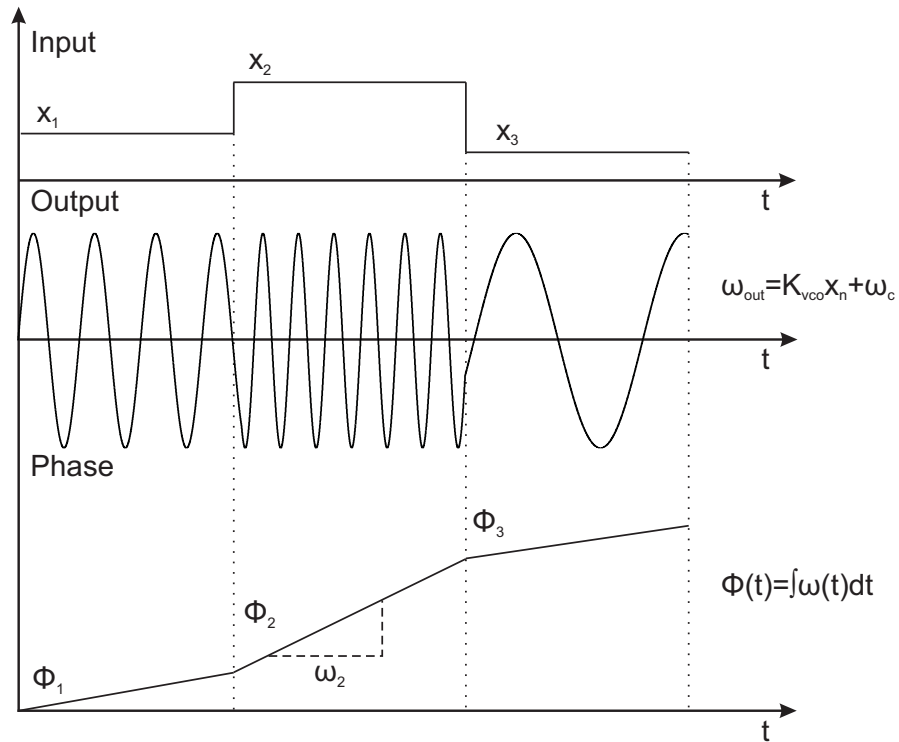


Figure 3.4: Principle of Operation of a VCO. Part a) shows the input the VCO which is for illustrative purposes three different amplitudes. Part b) illustrates how the frequency of oscillation at the output of the VCO depends linearly on the input magnitude. Part c) explains how the frequency of the carrier sinusoid is the derivative of the accumulating phase.

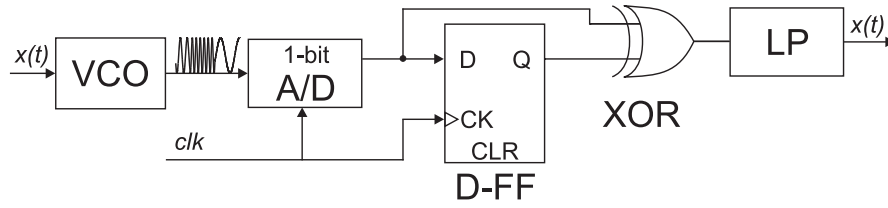


Figure 3.5: Delta-Sigma Modulator by utilizing a VCO as integrator, an A/D converter (hard-limiter), sampling D-FF and XOR to implement differentiation, and a low-pass to obtain back the input signal [Sogo, 1989]

of utilizing a analog-to-digital converter converting the analog FM signal into a digital signal of one bit, an exclusive OR (XOR) circuit performing differentiation of the digital signal, and finally a low-pass filter which is supplied with a pulse train furnished from the exclusive OR circuit. This principle, along with utilizing a VCO for modulation, can then be used to implement a sigma delta modulator without feedback [Hovinn et al., 1997; Sogo, 1989]. The overall scheme is shown in figure 3.5. Note that the D-FF and XOR gate is essentially a phase-detector. The phase detector is essentially a differentiator, $1 - z^{-1}$, which disregards the sign bit by taking the absolute value.

3.2 An FIR Sigma Delta Modulator Utilizing an Asynchronous D-FF

The topology depicted in figure 3.5 can be simplified further by realizing that the phase detector can be replaced by a phase rate monitor which is simply an asynchronous D-FF. This is described next. We essentially combined the D-FF, XOR, and A/D converter into one asynchronous D-FF which is cleared with a one-shot to arrive at the circuit shown in figure 3.6. This simplifies the circuitry as we now have less component count resulting in a more efficient architecture. The principle of operation can be explained as follows. We know from Logan's theorem [Logan, 1977] and other references [Carlson et al., 2001] that if a signal is band-limited then the times or instances of the zero crossings are sufficient to reconstruct the signal to within a constant factor. Since the bandwidth of the modulating signal is limited to only a small fraction of the frequency of the carrier, the information can be determined by the zeros crossings of the carrier sinusoid alone. Positive and negative zero crossings of the signal $y(t)$ occur at a phase change

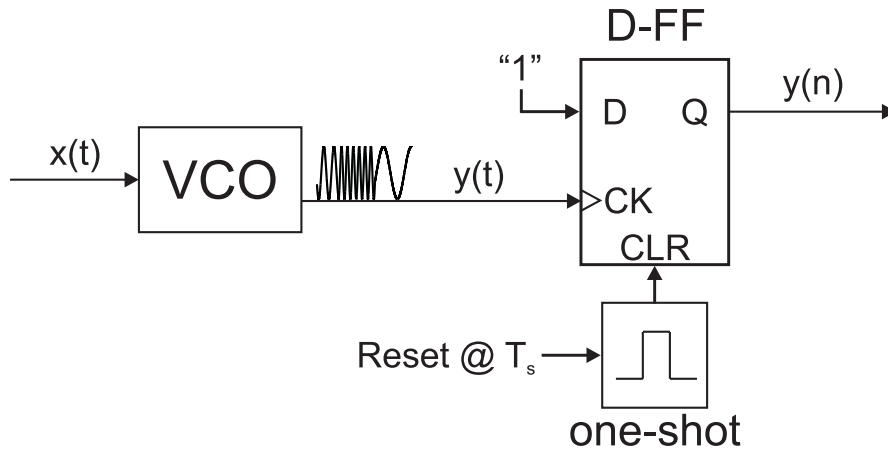


Figure 3.6: Delta-Sigma Modulator by utilizing a VCO as integrator and a D-FF for differentiation. D-FF is cleared with a one-shot.

of π of the carrier sinusoid and contain all the information about the input signal. A D-FF can be used which is clocked by these zero crossings to quantize and differentiate the signal $y(t)$. Essentially, the D-FF acts as a accumulate and dump circuit which is equivalent to a rate monitor. Consequently, the D-FF performs as a phase monitor implementing first-order noise shaping. This is an important point as it simplifies the delta-sigma converter. The entire principle is depicted in Fig. 3.7. The input signal, $x(t)$, generates a linear frequency-modulated signal, $y(t)$, where the frequency of oscillation is proportional to the input amplitude. Reference points are taken at the oscillator output waveform, such as the positive-slope zero crossings which occur when the total phase crosses integer multiples of 2π . Subsequently, these locations are quantized along the time axis by the D-FF using a grid of equally spaced time slots of width T_s as shown in Fig. 3.7. The final output, $y(n)$, can then be read out from a synchronized decimation filter. The exemplary embodiment depicted in figure 3.6 is thus a departed approach from the topology depicted in figure 3.5 [Hovin et al., 1997; Sogo, 1989]. To obtain best performance results, we need to make sure that the D-FF is being reset at a rate greater than the frequency of the carrier sinusoid. This is due to the fact that the D-FF can only recognize one positive zero crossing at a time. If not being reset fast enough, the D-FF might miss zero crossings resulting in a loss of information. Other factors which might limit the performance, but apply to all sigma-delta topologies, include meta-stability, clock jitter, and phase noise from the oscillator [Tao et al., 1999b; Awad,

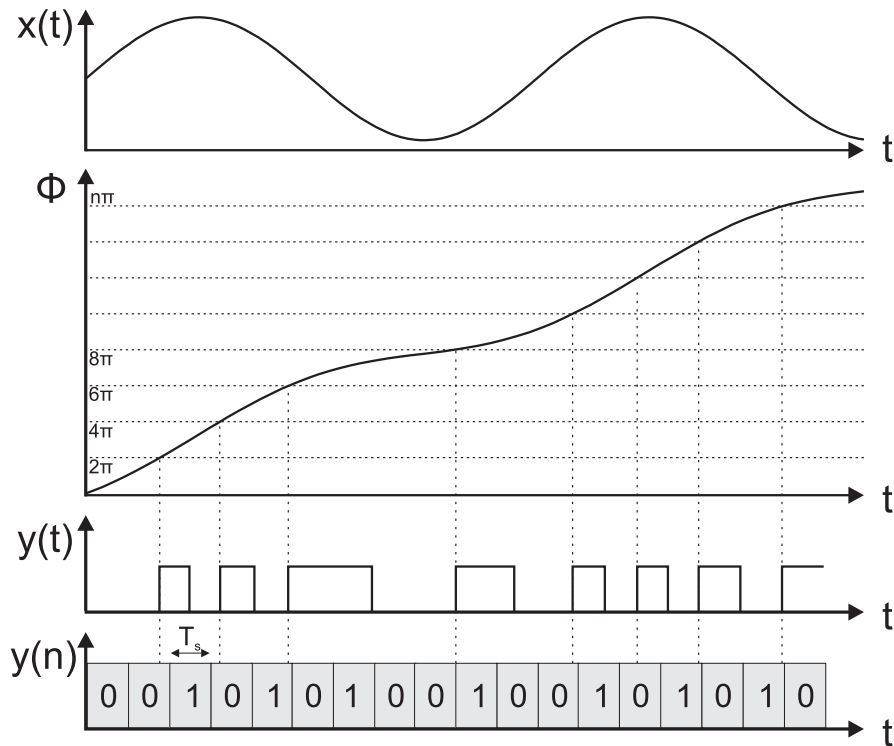


Figure 3.7: The figure shows the modulating signal $x(t)$ and the resulting phase change of the oscillator, $\phi(t)$. The oscillator produces a waveform, $y(t)$, which has zero-crossings for each multiple of 2π . These zero crossings can be time-domain quantized by counting them over a fixed time window, T_s . The introduced quantization noise is differentiated by resetting the count value at the end of each sampling window, thus performing an accumulate and dump function.

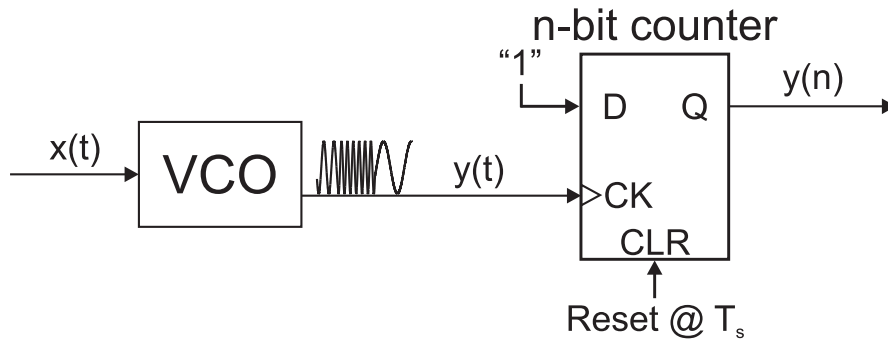


Figure 3.8: Delta-Sigma Modulator by utilizing a VCO as integrator and a resetting counter as quantizer.

1997; Oliaei, 2000]. For example, an error can occur when the D-FF is set to clear while an FM edge is present.

3.3 A FIR Sigma Delta Modulator Utilizing an Asynchronous Counter

Another novel way to replace the D-FF, XOR and A/D converter from figure 3.5 is to utilize a resetting counter. This scheme is depicted in figure 3.8. Similar to the asynchronous D-FF, the resetting counter counts the rising and falling edges of the FM signal over some constant period, T_s , at which, the count value is read out and the counter is reset. Therefore, the counter acts as a quantizer as well as differentiator for the introduced quantization noise. To make sure the counter does not miss any FM edges, the maximum count value of the counter must not be exceeded during the time window T_s . This topology is particularly well suited for utilizing undersampling. In conventional applications where a sample and hold circuit might perform undersampling, the sampling frequency has to be selected very carefully to avoid aliasing. That is, the bandwidth of interest must not cross any integer multiples of $F_s/2$. Furthermore, for certain sampling frequencies, F_s , there will be a spectral reversal in addition to the desired frequency shift. This can be seen with the help of figure 3.9. The figure shows the signal of interest on sheet five. After the undersampling process the signal will fall correctly onto the first sheet. However, when the signal of interest is on sheet four or six, then the final signal after being translated down to sheet one will also experience a spectral reversal, for example. However, when using the resetting counter any undersampling

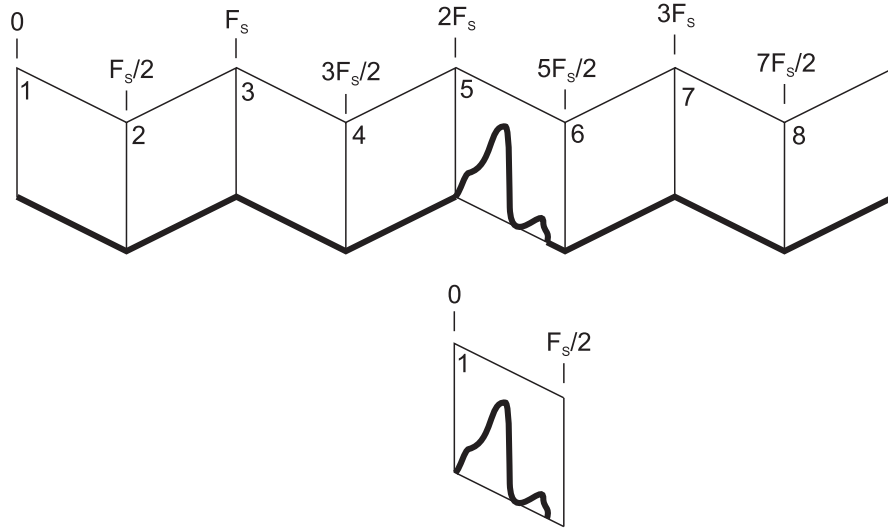


Figure 3.9: Frequency translation due to undersampling and spectral reversal.

frequency will work as long as the counter does not miss any edge crossings in between sampling instances and the sampling frequency satisfies the Nyquist criterium. These two criteria can easily be satisfied. With reference to figure 3.8 we note the combination of integrator and differentiator is similar to a sinc decimation filter, more specifically, similar to Hogenauer decimation filters [Hogenauer, 1981]. An efficient way to realize decimation filters is to utilize a sinc or comb filter. A sinc filter of order L has the transfer function:

$$H(z) = \left(\frac{1 - z^{-R}}{1 - z^{-1}} \right)^L, \quad (3.4)$$

where R is the decimation factor. One implementation of a sinc filter is known as the Hogenauer structure and consists of a series of cascaded accumulators followed by a cascade of differentiators (CIC) [Hogenauer, 1981]. There is a connection of the FIR modulator to the Hogenauer sinc decimation filter. One can re-draw the resetting-counter from figure 3.8 as shown in figure 3.10. The figure shows the resetting counter which, in a first step, is redrawn as an accumulate and dump circuit [Norsworthy et al., 1997, p.33]. The accumulate and dump function performs the same operation as a first-order Hogenauer sinc decimation filter. When omitting the resetting operation from the counter, the differentiation function is removed leaving an accumulator behind. When implemented as a modulo 2^n accumulator we obtain the modulo 2^n accumulator used in the Hogenauer sinc decimation filters. This is depicted in figure 3.10 which implies

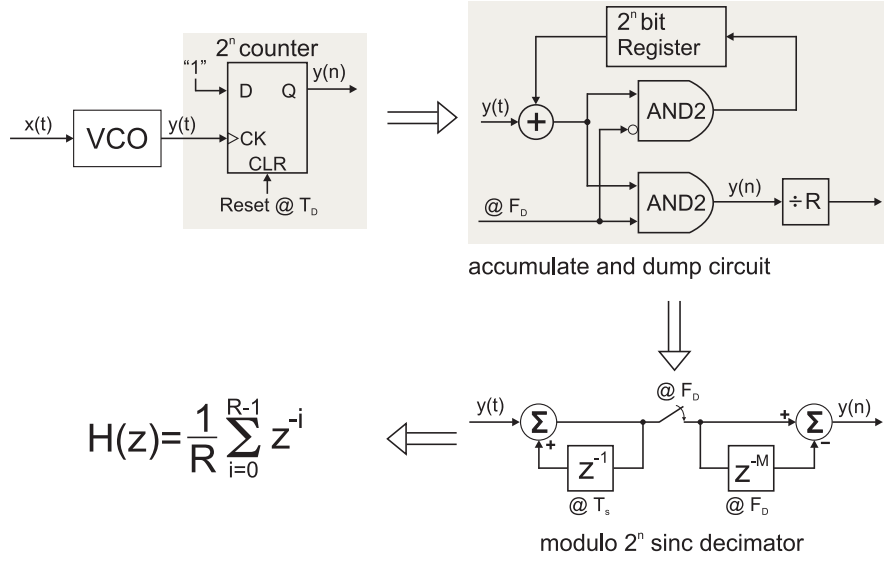


Figure 3.10: The equivalence of the resetting counter to the sinc decimation filter.

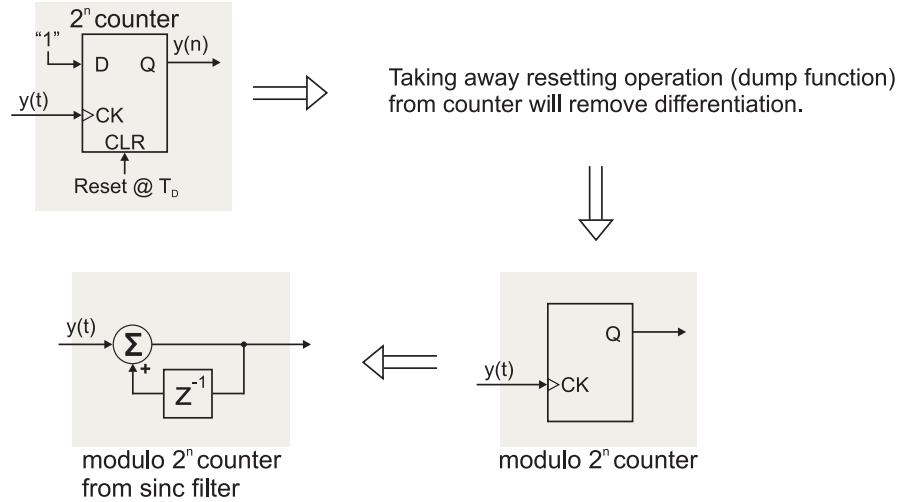


Figure 3.11: The equivalence of the counter to the sinc accumulator.

that the modulo counter can be used in the sinc decimation filter as well as in the FIR modulator. As a result, we can improve the two structures from figures 3.6 and 3.8 by combining the decimation filter with the FIR modulator. This can be achieved by absorbing the accumulating modulo counter from figure 3.11 into the decimation filter. As shown in [Hogenauer, 1981] the order of the decimation filter should be one higher than that of the modulator. Since the FIR modulator is of first-order a second order decimation filter will be used. The FIR modulator, followed by a second order sinc decimation filter based on two accumulators and two differentiators is depicted by the shaded area in

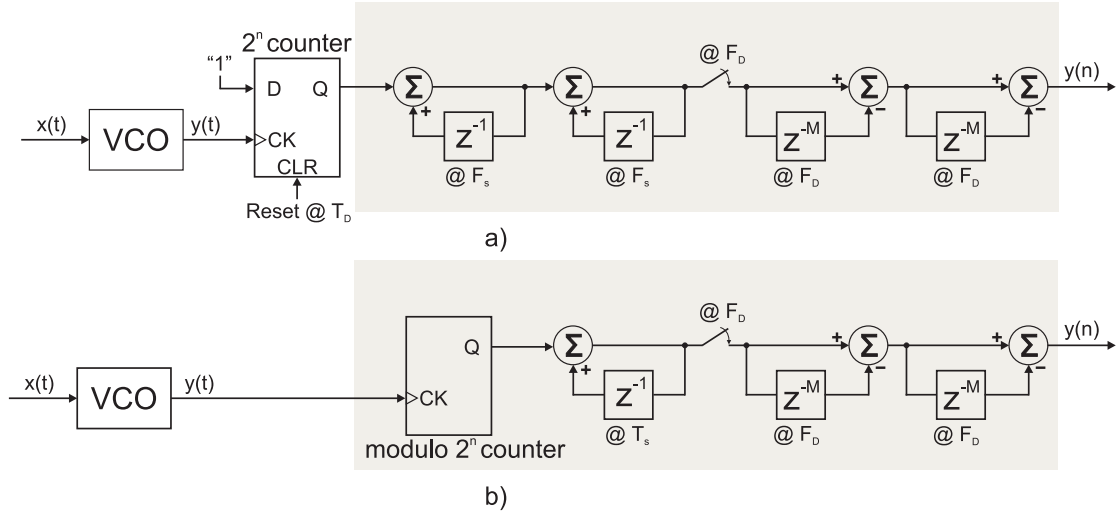


Figure 3.12: FIR modulator with a CIC decimation filter reducing the output rate from F_s to $F_D = \frac{F_s}{R}$. Part a) shows the FIR modulator with the CIC decimation filter connected to its output. Part b) depicts the simplified FIR modulator with the resetting D-FF now absorbed in the decimation filter. All additions are performed in two's complement or modulo 2^n arithmetic with bit width, n , large enough to accommodate the final output magnitude as explained in Section 2.3.3.

figure 3.12 a). Shown in figure 3.12 b) is how the D-FF was absorbed into the decimation filter by utilizing a counter which is clocked by the zero crossings of the frequency modulated signal. This simplification not only reduced digital circuitry, but also rids the topology of the resetting operation. As a result, all the information in the zero crossings of the FM signal is retained regardless of the system clock frequency, F_s . Additionally, a clocking scheme will be easier to implement as there is no explicit sampling of the frequency modulated signal necessary before feeding it into the modulo-counter.

3.4 Theoretical Performance

Having introduced the FIR modulator conceptually, a mathematical model is needed to gain insight into the theoretical performance. This section treats the quantization noise introduced when sampling a frequency modulated signal, i.e. output of a VCO being sampled by a D-FF or counter. As a result, signal-to-noise ratio equations can be derived to give more insight into the modulator. Figure 3.13 depicts the sampling and quantization of the frequency modulated signal, FM , at the output of the oscillator. In part a) of the figure a FM signal from the output of a VCO is shown. The period is

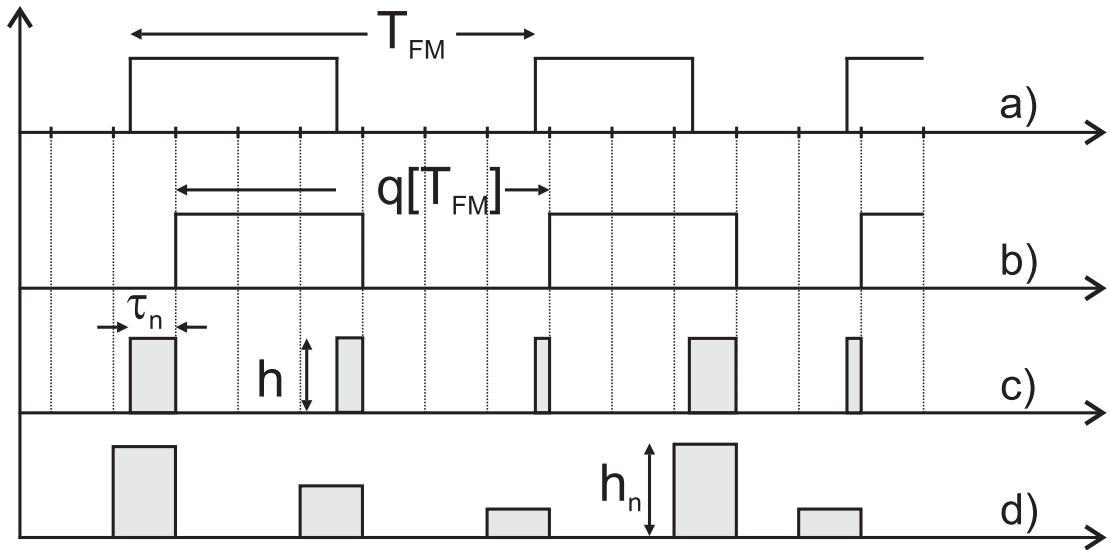


Figure 3.13: Part a) depicts the asynchronous FM signal from the VCO. Part b) shows the now synchronized FM signal. In c) the time-domain quantization error is illustrated, which can be normalized with respect to the sampling time as shown in part d).

denoted by T_{FM} . This signal is sampled, or synchronized with respect to a sampling clock, F_s , resulting in the quantized signal depicted in part b) of the figure. When sampling the FM signal an error is introduced which is a timing error in the positive and negative going edges, as depicted by the shaded area in part c) of Figure 3.13. Each shaded error pulse will have a pulse width τ_n which is anywhere between 0 and T_s . Thus, when normalized with respect to F_s each error pulse will have a height between 0 and 1. This is shown in part d) of Figure 3.13, which shows the normalized error of constant width T_s but variable height, h_n . There are different approaches that can be taken to analyze the performance of the FIR modulator. As cited in [Iwersen, 1969], the spectrum of a pulse sequence can be broken into a factor which contains the information about the pulse shape and a factor which contains the information about the area of each pulse and the periodicity. Following this, [Roza, 1997] assumes the area A_n under each error pulse to be a random quantity and uniformly distributed between 0 and T_s . This assumption presupposes a lack of correlation between the sampling frequency and the modulating frequencies. However, there is a strong correlation between the sampling frequency F_s and the frequency of the FM signal, F_{FM} . Intuitively, the frequency of the FM signal, F_{FM} is quantized or divided by the sampling frequency, F_s . This division can

be expressed as:

$$\frac{T_{FM}}{T_s} = \left\lfloor \frac{T_{FM}}{T_s} \right\rfloor + \left\langle \frac{T_{FM}}{T_s} \right\rangle \quad (3.5)$$

Here, the $\lfloor \cdot \rfloor$ operator expresses the floor operator and $\langle \cdot \rangle$ the fractional part. Thus, the normalized error $\left\langle \frac{T_{FM}}{T_s} \right\rangle$ will be an equidistributed modulo one sequence, uniformly filling the interval $[0..1]$. As a consequence, a different approach must be taken to analyze the quantization error. In [Candy and Benjamin, 1981] Candy models a delta-modulator with an impulse generator which generates a width pulse T_s whenever the asynchronous FM signal goes up or down. These asynchronous pulses can then be sampled by a sampling clock F_s . This is depicted in Figure 7 in [Candy and Benjamin, 1981]. A parallel approach is taken here to find an expression for the error pulse sequence. To do so the square-wave frequency modulated signal is assumed to have a width of α_c and period of T_c . Hence, the duty cycle would be $\frac{\alpha_c}{T_c}$. This signal can then be expressed as the summation of two unit-step functions. Since a step-function is the integral of the Dirac function we can express the frequency modulated signal as:

$$FM(t) = \sum_l \int dt \{ \delta(t - lT_c) - \delta(t - lT_c - \alpha_c) \}. \quad (3.6)$$

The Fourier series of a dirac function is given as:

$$\delta(t - T) = \sum_{l=-\infty}^{\infty} \exp[2\pi j l(t - T)] \quad (3.7)$$

With equation 3.7 equation 3.6 is now given by:

$$\begin{aligned} FM(t) &= \frac{1}{T_c} \sum_l \int dt \left\{ \exp\left(2\pi j \frac{l}{T_c} t\right) - \exp\left(2\pi j \frac{l}{T_c} (t - \alpha_c)\right) \right\} \\ &= \sum_l \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \exp\left(2\pi j \frac{l}{T_c} \left(t - \frac{\alpha_c}{2}\right)\right) \end{aligned} \quad (3.8)$$

Equation 3.8 is the common Fourier series representation of a pulse train with duty cycle $\frac{\alpha_c}{T_c}$. and may be also expressed in a more common form which is given as:

$$FM(t) = \frac{\alpha_c}{T_c} + 2 \sum_{l=1}^{\infty} \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \cos\left(2\pi \frac{l}{T_c} t\right) \quad (3.9)$$

The phase shift of $\frac{\alpha_c}{2}$ is ignored from now on. This FM signal is then sampled by the sampling clock. We can express the sampling clock as a Dirac comb or $\text{III}(t)$ function:

$$\text{III}(t) = \sum_{i=-\infty}^{\infty} \delta(t - iT_s). \quad (3.10)$$

Because the Dirac comb is periodic with period T_s , it can be represented as a Fourier series [Bracewell, 2000; Ortigueira, 2001]:

$$\sum_k \delta(t - kT_s) = \frac{1}{T_s} \sum_k \exp\left(\frac{2\pi jkt}{T_s}\right). \quad (3.11)$$

Thus, when sampling the frequency modulated signal with the clock we can multiply equation 3.8 with equation 3.11 to obtain:

$$FM(t) = \sum_l \sum_k \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \exp\left(2\pi j \left(\frac{l}{T_c} + \frac{k}{T_s}\right)t\right) \quad (3.12)$$

In the last step the phase shift of $\frac{\alpha_c}{2}$ was ignored. Hence, we obtain a signal with spectral lines at $f = \left(\frac{l}{T_c} + \frac{k}{T_s}\right)$ as seen from the exponential expression in equation 3.12. Since we are only interested in the band of $[0..F_s/2]$, or $|f| \leq \frac{F_s}{2}$, the set of frequencies of the $FM(t)$ signal must satisfy:

$$\begin{aligned} \left| \frac{l}{T_c} + kF_s \right| &\leq \frac{F_s}{2} \\ \left| \frac{l}{T_c F_s} + k \right| &\leq \frac{1}{2} \end{aligned} \quad (3.13)$$

This can only be true if $k = -\lfloor \frac{l}{T_c F_s} \rfloor$. Then the set of frequencies of $FM(t)$ is given as $f = \langle \frac{l}{T_c F_s} \rangle F_s$. When inserting this k-value into equation 3.12 we obtain:

$$FM(t) = \sum_l \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \exp\left(2\pi j F_s \left\langle \frac{l}{T_c F_s} \right\rangle t\right) \quad (3.14)$$

Equation 3.14 represents the sampled frequency modulated signal which now includes an error term, which is the quantization error. If the center frequency, F_c , is modulated by a sinusoidal signal, equation 3.14 will be sinusoidal as well. To gain more insight into the why the center frequency F_c does not influence the overall performance of the modulator we can simplify the summation in equation 3.14 by noting that:

$$\sum_{l=-\infty}^{\infty} f(l) = \sum_{l=1}^{\infty} f(l) + \sum_{l=-\infty}^{-1} f(l) + f(0) \quad (3.15)$$

and obtain:

$$FM(t) = \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \Big|_{l=0} + 2 \sum_{l=1}^{\infty} \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \cos\left(2\pi F_s \left\langle \frac{l}{T_c F_s} \right\rangle t\right) \quad (3.16)$$

Equation 3.16 can be further simplified to yield:

$$FM(t) = \underbrace{\frac{\alpha_c}{T_c}}_{S_o} + 2 \underbrace{\sum_{l=1}^{\infty} \frac{\sin\left(\pi l \frac{\alpha_c}{T_c}\right)}{\pi l} \cos\left(2\pi F_s \left\langle \frac{l}{T_c F_s} \right\rangle t\right)}_{S_k} \quad (3.17)$$

Equation 3.17 tells us that we may distinguish between the baseband, S_o , and higher-order bands noise bands, S_k . The baseband is the undisturbed input signal, whereas the higher order bands are the noise components. It can be seen that if $\frac{F_c}{F_s}$ is a rational number the sequence $\langle l \frac{F_c}{F_s} \rangle$ will duplicate as the index takes on all integer values. That is, for a rational number $\frac{F_c}{F_s}$, the sequence $\langle l \frac{F_c}{F_s} \rangle$ is repetitive. The power spectrum of the noise would then be the summation of all amplitude components with $F_s \langle l \frac{F_c}{F_s} \rangle$ giving the desired frequency. It is also clear that when the modulating signal is periodic so is F_c , making the noise component periodic also. Since $\sin(2\pi u)$ is a periodic function and $\alpha_c = T_s$ we may write for the noise component:

$$n(t) = 2 \sum_{l=1}^{\infty} \frac{\sin\left(2\pi \left\langle l \frac{F_c}{2F_s} \right\rangle\right)}{\pi l} \cos\left(2\pi F_s \left\langle l \frac{F_c}{F_s} \right\rangle t\right) \quad (3.18)$$

Here, α_c equals T_s because the pulse width of the error due to sampling the FM signal was in the range $0..T_s$. Assuming an irrational frequency F_c , so that F_c is incommensurate with F_s , will assure the set of frequencies will be unique and the total power will be the summation for each input component. We also realize that for a good design, the center frequency must be high enough to separate the significant noise components from the baseband as also pointed out in [Roza, 1997]. It is important to note that the overall signal in equation 3.17 will be independent of the center frequency of the VCO, F_c . This is because the summation of all amplitude values of the higher order components in equation 3.18 including the base band will be:

$$\frac{F_c}{F_s} + 2 \sum_{l=1}^{\infty} \frac{\sin\left(2\pi \left\langle l \frac{F_c}{2F_s} \right\rangle\right)}{\pi l} = \frac{F_c}{F_s} + 1 - \frac{F_c}{F_s} = 1, \quad (3.19)$$

Hence, the overall output of the FIR modulator will be independent of the center frequency of the VCO, F_c as shown by the simulation results. When increasing the sampling frequency, on the other hand, we will attenuate the noise by 3dB and thus increase the signal-to-noise. This is because of the oversampling effect explained in Section 2.2. Essentially the noise is spread out over more data points, lowering the noise in band. This can also be seen when looking at the set of frequencies, $F_s \langle l \frac{F_c}{F_s} \rangle$, represented in equation 3.18. Since F_c is incommensurate with F_s , the sequence $\langle l \frac{F_c}{F_s} \rangle$ will uniformly fill out the interval $[0..1]$ and be independent of F_s or F_c in the limit $l \rightarrow \infty$. However, due to the multiplication factor of F_s in the term $F_s \langle l \frac{F_c}{F_s} \rangle$, the frequencies are spread out by a factor of two when doubling the sampling frequency F_s . It is also noted that due to the noise shaper $(1 - z^{-1})$ the noise floor will be attenuated by an additional 6dB. At the same time, however, the output signal of the FIR modulator will be attenuated as the VCO gain, K_{vco} , will be independent of the gain of the differentiator. This is easy to realize when considering the signal and noise transfer function of the overall FIR modulator. To start we realize that the signal transfer function (STF) will be the product of a CT integrator and a DT differentiator. To find the frequency response of the STF the CT integrator needs to be transformed into the discrete time domain. To have the FIR SDM produce the same output, the input to the counter needs to be the same for a CT and DT integrator. Thus, the impulse response of the CT integrator and the equivalent discrete time integrator has to be the same as well [Oliaei, 2001]. Therefore,

$$\mathcal{Z}^{-1}\{H(z)\} = \mathcal{L}^{-1}\{H(s)\} |_{t=nT} \quad (3.20)$$

For an ideal VCO the continuous time transfer function can be represented by its discrete time equivalent:

$$H(s) = \frac{K_{vco}}{s} \iff H(z) = K_{vco} \frac{1}{1 - z^{-1}} \quad (3.21)$$

Then the signal transfer function is given as:

$$STF = K_{vco} \frac{1}{1 - z^{-1}} T_s \frac{1 - z^{-1}}{1} = \frac{K_{vco}}{F_s}. \quad (3.22)$$

From equation 3.22 it can be seen that in the ideal case the signal appears scaled by K_{vco}/F_s at the output. Note that, a more realistic model for the VCO will include a

modulation bandwidth, ω_{mod} , which will attenuate signals at high frequencies. Also note that since there is no feedback anymore in the FIR modulator, the overall performance of the system will be only as good as the VCO. Phase noise and jitter effects as well as the non-linear V-F relationship of the VCO will therefore degrade the performance. The resolution of the FIR modulator depends on the sampling frequency F_s of the D-FF/counter and the sensitivity of the VCO K_{vco} . The noise transfer function, which shapes the quantization noise, is simply given as:

$$NTF = 1 - z^{-1}. \quad (3.23)$$

While equation 3.23 gives the correct noise shaping of the quantization noise, it does not show why the center frequency of the VCO does not influence the overall performance as equation 3.19 did. Assuming for the error to have zero mean and to be uncorrelated, the mean square value of the normalized error is given as:

$$V_\epsilon^2 = \sigma_\epsilon^2 = \int_{-1/2}^{1/2} x^2 dx = \frac{1}{12} \quad (3.24)$$

The overall introduced quantization noise power, V_ϵ^2 , is independent of the sampling frequency, similar to conventional delta-sigma modulators, and thus needs a scaling factor of $1/F_s$ as shown in equation 3.24. Intuitively, when F_s is doubled, the normalized error height is doubled as well to keep the area beneath each pulse constant. Thus, the spectral density, $S(f)$, will be:

$$S(f)^2 = \frac{1}{12} \frac{1}{F_s} \quad (3.25)$$

The quantization noise power introduced by the quantizer over the frequency band from 0 to f_b is given as:

$$\begin{aligned} P_e &= \int_{-f_{bw}}^{f_{bw}} S^2(f) |NTF(z)|^2 df = \int_{-f_{bw}}^{f_{bw}} \frac{1}{12} \frac{1}{F_s} |NTF(z)|^2 df \\ &\approx \int_{-f_b}^{f_b} \frac{1}{12} \frac{1}{F_s} \left[2 \left(\frac{\pi f}{F_s} \right) \right]^2 df \\ P_e &= 10 \log \left(\frac{\pi^2}{36 R^3} \right). \end{aligned} \quad (3.26)$$

Thus, with reference to equation 2.23 in Section 2.3.1 equation 3.26 is the same as for the conventional delta-sigma modulators. However, the output signal amplitude for the

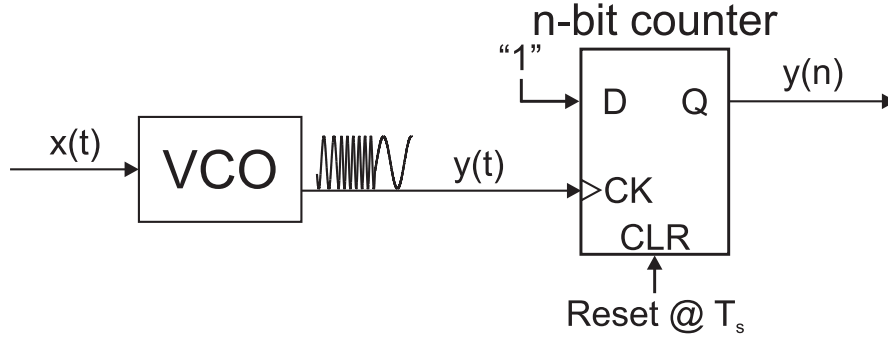


Figure 3.14: Delta-Sigma Modulator by utilizing a VCO as integrator and a resetting counter as quantizer.

FIR modulator is attenuated by 6dB for doubling F_s as already shown with 3.22. Thus the maximum signal-to-noise ratio is given as:

$$SNR \approx 20\log\left(\frac{A_{in}K_{vco}/F_s}{2\sqrt{2}}\right) - 10\log\left(\frac{\pi^2}{36R^3}\right), \quad (3.27)$$

where A_{in} is the input amplitude. This result is the same as the one derived in [Hovin et al., 1997].

3.5 Simulation Results

A first-order FIR modulator was simulated in Spectre using the VerilogA/AMS model as shown in the appendix A.1. The VCO is an ideal oscillator with center frequency, F_c , and VCO gain, K_{vco} . The rectified frequency modulated signal furnishes a resetting-counter which counts the zero-crossings of the FM signal over the sampling time T_s before resetting. The topology was shown in figure 3.8 and is repeated in figure 3.14 for convenience. First, equation 3.27 was compared to the experimental data. This is depicted in Figure 3.15. The figure shows the experimental data points along with a best fit line to illustrate the SNR trend when varying the sampling frequency, F_s . Also shown in figure 3.15 is the SNR predicted by equation 3.27. As can be seen the experimental data does approximate the predicted SNR but rather with slightly higher slope than the expected 3dB slope. Also, the experimental SNR is approximately 3dB higher than predicted by equation 3.27. As will be explained shortly, the SNR is quite dependant on the ratio of the frequency of the VCO, F_{vco} to the sampling frequency, F_s . For certain ratios, the baseband will be noisier than for other ratios. This seems

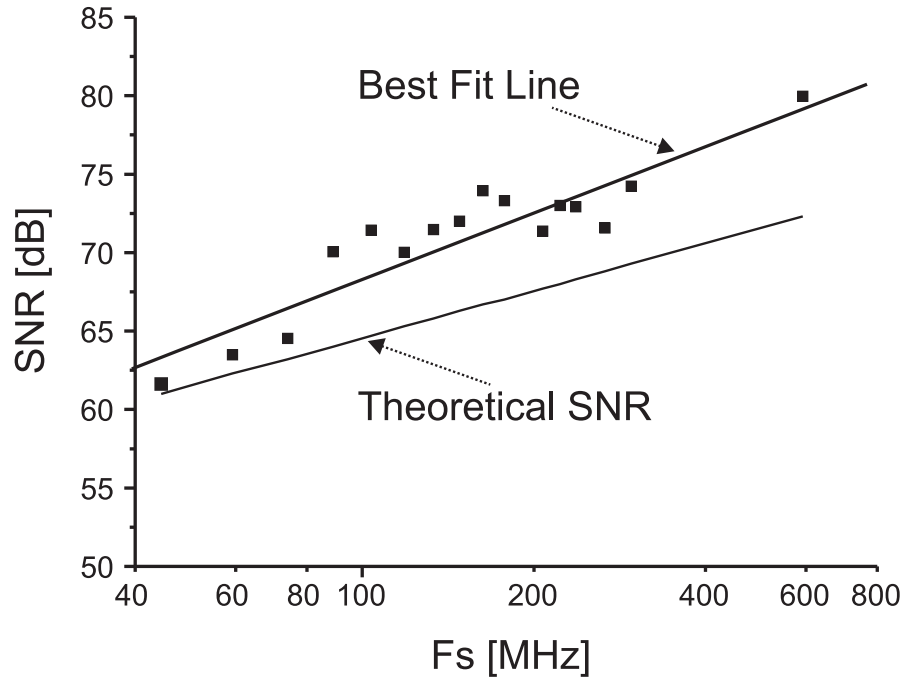


Figure 3.15: SNR results for a 1st order FIR modulator with varying sampling frequency, F_s . The plot shows the obtained data points along with a best fit line. Also shown is the SNR predicted by equation 3.27. Details: $K_{vco} = 0.5\text{MHz}$, $F_{in} = 8.4\text{kHz}$, $BW = 20\text{kHz}$, $F_c = 4.352\text{MHz}$.

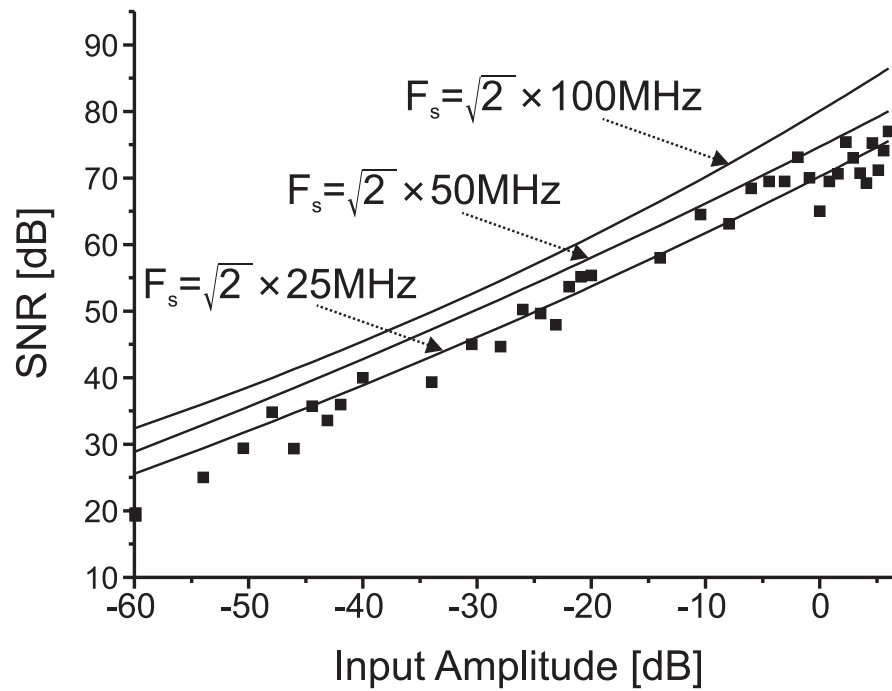


Figure 3.16: SNR results for a 1st order FIR modulator with varying input amplitude for three different sampling frequencies. Details: $K_{vco} = 0.5\text{MHz}$, $F_{in} = 8.4\text{kHz}$, $BW = 20\text{kHz}$, $F_c = 4\text{MHz}$.

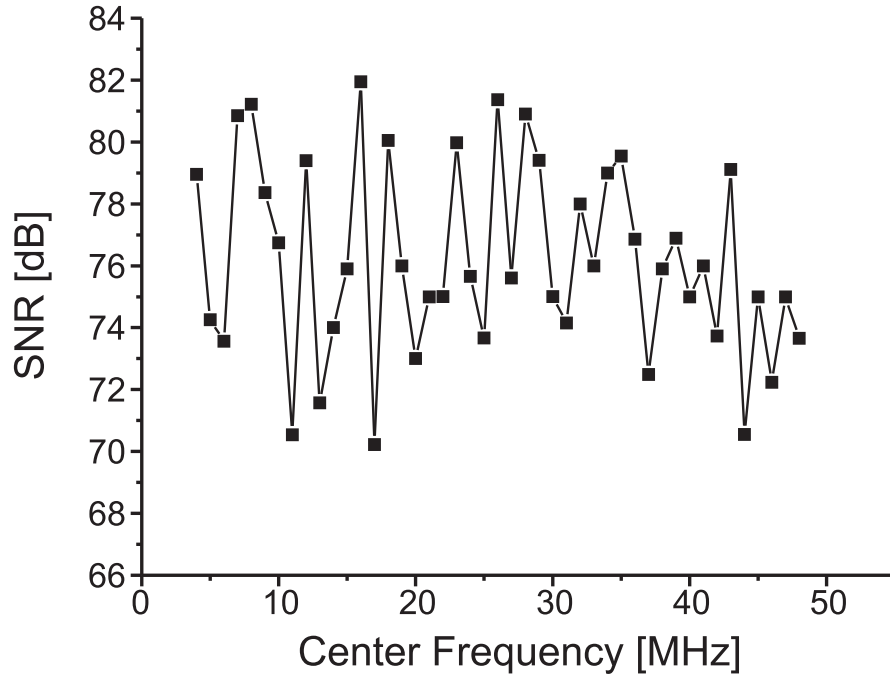


Figure 3.17: SNR results for a 1st order FIR modulator with varying VCO center frequency, F_{vco} . Details: $F_s = \sqrt{2} \times 100\text{MHz}$, $K_{vco} = 0.5\text{MHz}$, $F_{in} = 8.4\text{kHz}$, $BW = 20\text{kHz}$, $A_{in} = 0.5$.

to be the reason for the minor discrepancy of the obtained experimental SNR results to the theoretical SNR as equation 3.27 does not account for the spectral behavior of the quantization noise. Second, the input amplitude to the VCO was varied for three different sampling frequencies, F_s . The results are shown in Figure 3.16. In the figure, the solid lines represent a best-fit curve, approximating the obtained data points. This is to illustrate that for doubling the sampling frequency, F_s , a 3dB signal-to-noise ratio gain is achieved. The dots in figure 3.16 represent the data-points for the best fit line of $F_s = \sqrt{2} \times 25\text{MHz}$ as an example. This is to show that there is a variation in the in-band noise as the spectral components of the noise vary with input amplitude. This is similar to conventional delta-sigma topologies. Note however, that there is no maximum input range for the FIR modulator as the VCO is inherently stable, always producing a limited output signal. Thirdly, in another simulation, the center-frequency of the VCO was changed while keeping all other parameters constant. The results for this simulation are shown in figure 3.17. As expected from theory, the signal-to-noise ratio is independent of the center frequency, F_o . Still, there is a variation in signal-to-noise ratio as some ratios of $\frac{F_c}{F_s}$ will result in a quieter or more noisy base band. To illustrate this point we

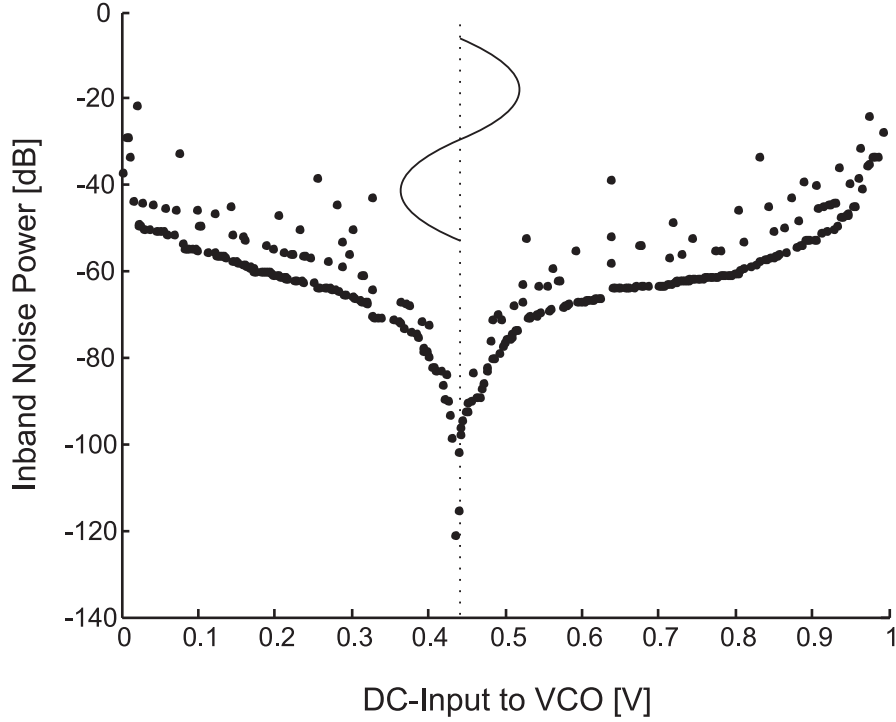


Figure 3.18: Total power of noise components within baseband. Depicted also a small sinusoid centered so as to minimize noise components. $F_s = \sqrt{2} \times 25e6$, $F_c = 8MHz$, $K_{vco} = 0.25MHz$

can utilize equation 3.18 which is repeated here:

$$n(t) = 2 \sum_{l=1}^{\infty} \frac{\sin\left(2\pi \left\langle l \frac{F_c}{2F_s} \right\rangle\right)}{\pi l} \cos\left(2\pi F_s \left\langle l \frac{F_c}{F_s} \right\rangle t\right) \quad (3.28)$$

For certain ratios of $\frac{F_c}{F_s}$ the baseband will be noisier than for other ratios. The set of frequencies is given as $F_s \langle l \frac{F_c}{F_s} \rangle$, and for certain values of l these will fall into baseband, $f \leq BW$. Since the frequency of oscillation of the VCO is given as $F_{vco} = F_c + K_{vco} \times x_{in}$, we can see that a dc-input be directly seen as simply a change in F_c . Thus, the finite set of frequencies of $f(l)_{set} = F_s \langle l \frac{F_c}{F_s} \rangle$ can be obtained and the values of l which cause $f(l)_{set}$ to be $\leq BW$ can be obtained. Each dc-input will produce a distinct set of frequencies and all the powers which fall onto the same frequency can be added. This is illustrated in figure 3.18. The figure plots the simulation results of the total power of the noise components which fall into baseband as a function of various dc-input values. As can be seen, for some inputs there are more noise components which fall into baseband than for other input values. In figure 3.18 one such value is $x_{in} = 0.45$ and it seems a good choice to center a small sinusoid at this value, since the center frequency of the VCO

is usually given. This is indicated by the sine-wave in figure 3.18. It might also be noted that since the introduced quantization noise is not fed back into the modulator as in conventional modulators the noise in the FIR modulator tends to be more correlated.

3.5.1 Non-Linearities

While the FIR modulator is easy to implement and requires only little analog and digital circuitry, it is mainly limited by the noise performance and linearity of the VCO. This is because there is no negative feedback to reduce aforementioned problems common to VCOs. The two main limitations for the analog circuitry are analyzed next. First phase noise which is common to oscillators is observed and its effects on the signal-to-noise ratio. Second, the linearity of the VCO is discussed. The main limitation for the digital circuitry is Jitter of the required sampling clock and meta-stability.

The source of phase noise in an oscillator is due to thermal and flicker noise [Agilent Technologies, 2006]. Jitter in autonomous blocks is almost completely due to the oscillator's phase noise. Phase noise and jitter are also two related quantities. Phase noise is a frequency-domain view of the noise spectrum around the oscillator signal, while jitter is a time-domain measure of the timing accuracy of the oscillator period. Phase noise can thus be related to jitter, but only in the absence of flicker or 1/f noise. Since oscillators translate signals between frequencies, any injected noise at baseband will appear near the carrier and its harmonics. Similarly, noise at the harmonics or carrier will appear in turn at baseband. In [Kundert, 2006] the author relates phase noise of an oscillator to a jitter metric. This relation is expressed in equations 63, 74, and 78 on pages 31 through 33. Then the equivalent jitter can be modeled as a random variation in the frequency of the VCO. Equation 85 on page 38 in [Kundert, 2006] gives the dithered frequency of the VCO including jitter as:

$$f_j = \frac{f_0}{1 + \Delta T_j f_0}, \quad (3.29)$$

where ΔT_j is given as:

$$\Delta T_j = \sqrt{K} J \delta_j \quad (3.30)$$

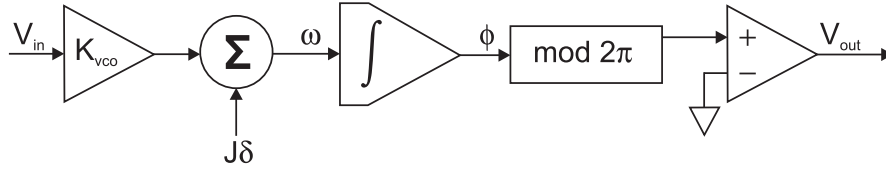


Figure 3.19: Block diagram of the behavioral model of the oscillator used in a first-order FIR modulator which includes jitter [Kundert, 2006].

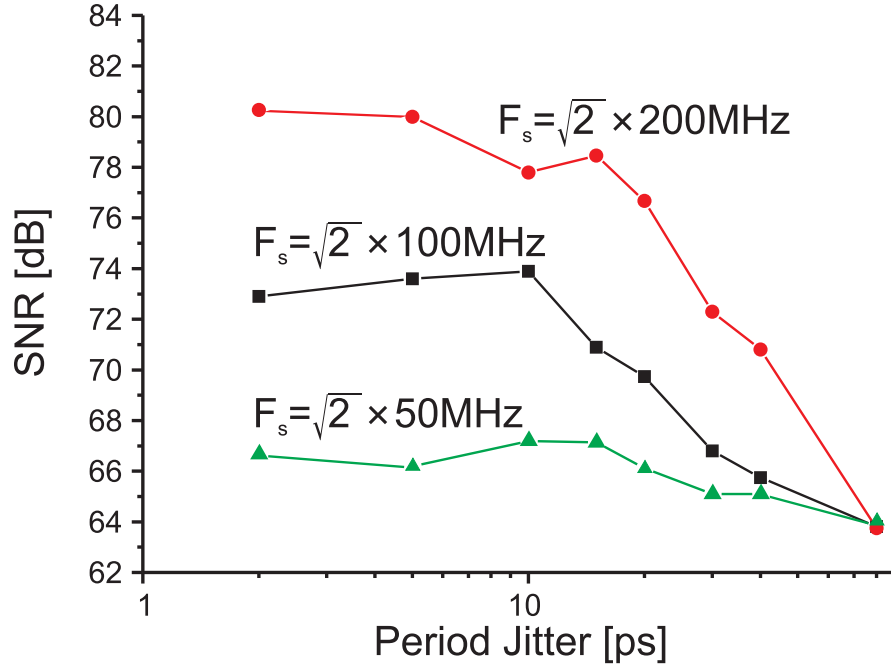


Figure 3.20: SNR results for a 1st order FIR modulator with phase noise related to jitter. Details: $F_s = \sqrt{2} \times 50 \text{ MHz}, 100 \text{ MHz}, 200 \text{ MHz}$, $K_{vco} = 0.5 \text{ MHz}$, $F_{in} = 8.4 \text{ kHz}$, $BW = 20 \text{ kHz}$, $A_{in} = 0.5$, $f_0 = 4.352 \text{ MHz}$.

The term f_0 is the free-running frequency of the VCO, ΔT_j is the random variation in each period of the VCO due to jitter and δ_j is a zero-mean unit-variance Gaussian random process. The factor K in equation 3.30 is the number of jitter updates per period. For a square wave K is 2. This jitter metric based on equation 3.29 can then easily be included into an oscillator VerilogA/AMS model and the FIR modulator can be simulated. By varying the jitter we can thus gain insight into the effects of phase noise of the oscillator on the overall performance of the FIR modulator. Intuitively, since the jitter due to phase noise is quite random, it should act as an equivalent to dither in conventional delta-sigma modulators applied at the input [Chou and Gray, 1991], breaking up idle tones in the output of the modulator to some extent but also increasing the noise floor in baseband. A model for the oscillator VerilogA/AMS model is shown in Figure

3.19. Thus, the period jitter, J , is modeled as a random variation in the frequency of the VCO. Note, that the jitter appears at the input of the VCO and will thus directly add to the output of the FIR modulator. A first-order FIR modulator was simulated for various jitter values and sampling frequencies. The model for the VerilogA/AMS code is given in Appendix A.1. This is the same model as used before for simulating the FIR modulator. This time however, the optional jitter parameter is used, dithering the frequency of the VCO. The obtained results are depicted in Figure 3.20. As can be seen in figure 3.20 for low jitter/phase noise values the SNR does not degrade much, however, at large jitter values and high sampling frequencies the SNR degrades by approximately 3dB per doubling the phase noise. When a low sampling frequency is used, for instance the $\sqrt{2} \times 50\text{MHz}$ plot in figure 3.20 the SNR becomes less dependent on phase noise and thus only degrades a little. In general, low noise oscillators should be used to obtain best performance, however, requirements are less stringent when using a low sampling frequency. For instance, undersampling the output of oscillator is a good way to be less affected by phase noise or jitter. Another non-ideal effect is the non-linearity of the voltage-controlled oscillator. That is, the frequency of the output of the VCO will not be a linear function of the input voltage. This non-linearity of the input-voltage output-frequency relationship will introduce even and odd order harmonics in the output spectrum. To keep these harmonics to a minimum, the oscillator should be operated in the most linear region and the input voltage amplitude should be kept as small as possible. However, performance evaluation and demands entirely depend on the application purpose. In audio applications such as studio microphones certain nonlinearities might be desired. For instance, distortion by-products that lie closer to the excitation are less likely to be perceived [Earl and Lidia, 2003]. Furthermore, non-linearities caused by the oscillator or more importantly by other components such as a condenser microphone for instance will produce a more rich appearing sound to the ear. As will be shown later, we use the oscillator FIR modulator to implement a digital microphone.

Meta-stability in digital systems occurs when two asynchronous signals combine in such a way that their resulting output goes to an indeterminate state [Wellheuser, 1996].

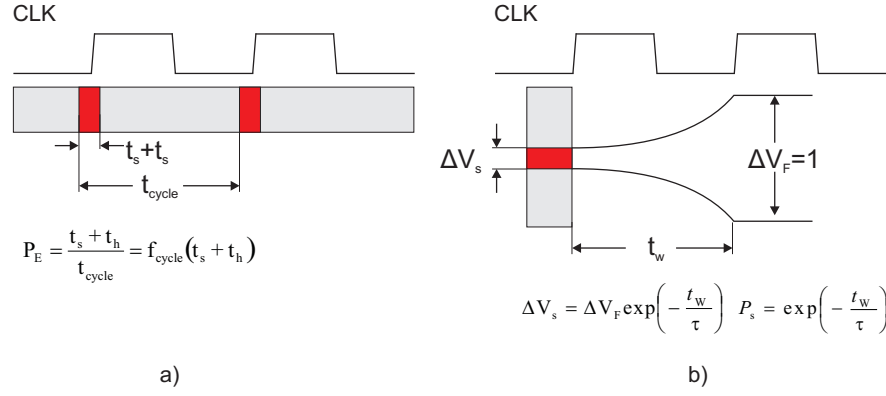


Figure 3.21: Meta-stability: a) Probability to enter a metastable state b) Probability to still be in a metastable state after some time t_w

A common example is the case of data violating the setup, t_s , and hold, t_h , specifications of a latch or a flip-flop. In a synchronous system, the data always has a fixed relationship with respect to the clock. When that relationship obeys the setup and hold requirements for the device, the output goes to a valid state within its specified propagation delay time. However, in an asynchronous system, the relationship between data and clock is not fixed, therefore, occasional violations of setup and hold times can occur. When this happens, the output may go to an intermediate level between its two valid states and remain there for an indefinite amount of time before resolving itself, or it may simply be delayed before making a normal transition. In either case, a metastable event has occurred. Eventually, the output will stabilize at a valid logic level; however, logic circuitry after the flip-flop might fail due to the delay caused by metastability. Thus, it is important to understand when a flip-flop might fail. The probability for a device to fail P_{fail} is given as the product of the probability that the device will enter meta-stability P_e and the probability that the device is still in a metastable state P_s after some time t_w .

$$P_{\text{fail}} = (P_e)(P_s) \quad (3.31)$$

The probabilities P_e and P_s are defined in Figure 3.21. The probability to enter a metastable state is given as the probability of a given transition being in the setup+hold window $t_s + t_h$ which is the fraction of time that is setup and hold window. This is depicted in Figure 3.21a). The device might still be in a metastable state after some time t_w when the starting voltage ΔV_s was too small. The Probability of starting with

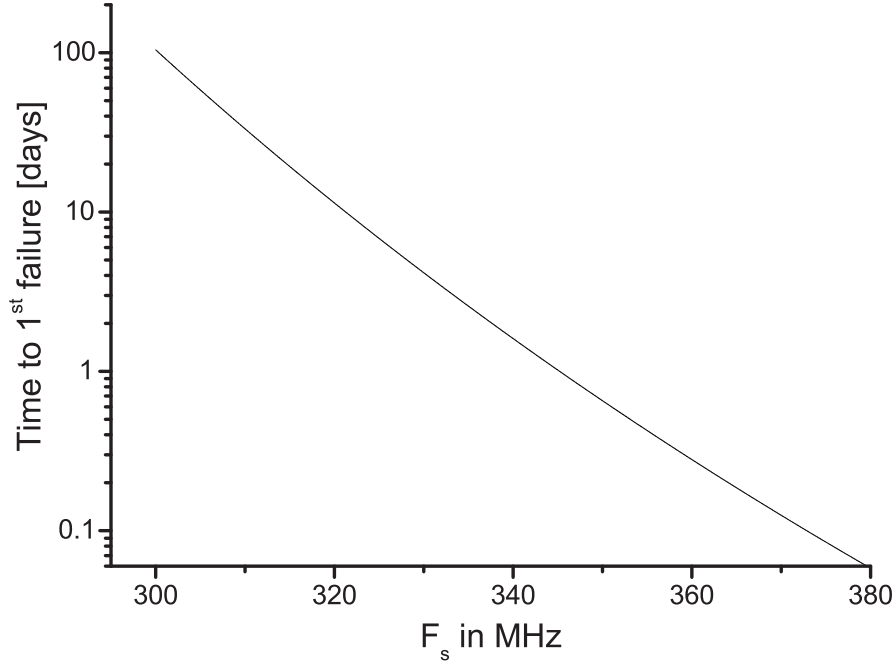


Figure 3.22: Mean time between failures plot.

this voltage is proportion of total voltage range that is too small. This is depicted in Figure 3.21b). As a result the failure probability and error rate are given as:

$$P_{fail} = (P_s)(P_e) = (t_s + t_h) f_{cycle} \exp\left(-\frac{t_w}{\tau}\right) \quad (3.32)$$

$$f_{fail} = (f_{sig})(P_{fail}) = f_{sig} (t_s + t_h) \exp\left(-\frac{t_w}{\tau}\right) \quad (3.33)$$

In Equation 3.33 f_{sig} is the frequency of the signal to be sampled and τ is the circuit time constant (which has also been shown to be inversely proportional to the gain-bandwidth product of the circuit). To see how meta-stability will effect the FIR modulator consider the example given below. Assume a rather large value of $t_h = t_s = \tau = 100ps$ for illustration purposes and assume the maximum FM frequency for a $0.5\sin$ input signal is about $F_s/4$. With this in mind we can plot equations 3.33 to plot the time till the first failure as a function of sampling frequency F_s . Figure 3.22 shows that for high clock frequencies meta-stability becomes an issue. To solve this problem one can easily use a frequency divider before applying the FM signal to the D-FF. However, a better approach is to use under-sampling as a means to keep the sampling frequency at a desired value. This is especially beneficial when the frequencies at the output of the VCO are in the UHF range. As will be shown in an application example, we use undersampling of

the frequency modulated signal to circumvent then otherwise difficult data acquisition at very high frequencies.

3.6 *Discussion and Conclusion*

It was shown that a first-order FIR modulator can be realized by using a VCO to create a frequency modulated signal and sampling D-FF in combination with an XOR gate to reproduce the input signal. This topology was then simplified by combining the XOR gate and D-FF into a single asynchronous D-FF utilizing a one-shot. This simplification was possible by realizing that a resetting D-FF acts as a time-domain quantizer and differentiator at the same time. Additionally, the asynchronous D-FF was replaced by a resetting counter, also acting as a time-domain quantizer and differentiator. The main advantage of using an asynchronous counter is to utilize powerful under-sampling techniques. With oscillators producing often very high frequency signals [Tsai et al., 2005; Li and O, 2005; Bao et al., 2005], it was felt that undersampling is a useful technique to process the FM signal at a much lower frequency. Using a counter in conjunction with undersampling also eases the requirements on the sampling frequency, F_s . Hence, a FIR modulator consisting of a VCO and resetting counter realizes an efficient A/D converter with reduced circuitry, that is very versatile with undersampling techniques, and still gives good performance results. Next, the first-order FIR modulator was analyzed by providing a mathematical model for the introduced quantization noise power, and a signal-to-noise ratio equation was found. This equation was successfully compared to simulation results which were obtained using a VerilogA/AMS model of the first-order FIR modulator. Similar to conventional modulators, the noise floor is reduced by increasing the sampling frequency F_s . When doubling F_s , the noise floor is reduced by 3dB due to the oversampling effect, and 6dB are obtained by attenuating the noise floor in the band of interest by the differentiator. However, since the integrating gain of the VCO, K_{vco} , is independent from the sampling frequency F_s the output signal will be reduced when F_s is increased, resulting in an overall 3dB signal-to-noise ratio improvement per doubling of F_s . Even though the presented FIR modulators used little

circuitry, they are affected by non-idealities such as phase-noise of the oscillator and meta-stability of the digital circuitry. Hence, jitter due to phase noise of the oscillator and its effects on the first-order FIR modulator was investigated. It was found that only large jitter values will degrade the performance. When the jitter is large enough to effect the SNR, then a 3dB decrease per doubling the jitter value was observed. In addition to phase-noise, meta-stability of the digital circuitry was considered also. Since the resetting of the asynchronous D-FF needs to satisfy certain setup and hold requirements, errors might occur when an input is present. As a result, a mean-time between failures figure was produced revealing a strong dependency of the sampling and resetting time, F_s to the failure rate of the device. Hence, it is desired to utilize undersampling to circumvent very high sampling frequencies. A lower sampling time in turn relaxes the requirements on the resetting frequency of the D-FF.

CHAPTER IV

FIR DIGITAL MICROPHONE UTILIZING UNDERSAMPLING

Microphones are usually realized by utilizing a capacitive changing transducer to produce a DC voltage across a high impedance resistor proportional to the impeding sound waves. This voltage drop can then be amplified before it is being converted into the digital domain by a delta-sigma analog-to-digital converter. With the change in capacitance due to the sound waves being quite small, and the high impedance resistor being noisy, a clean and high quality signal is difficult to achieve. A better approach would be to utilize the presented FIR modulator to realize a digital microphone. As will be shown in this section, this approach helps alleviate some of the problems often encountered with conventional microphone implementations. The proposed digital microphone uses minimal circuitry, keeping the component count low, solves the problem with the small capacitance change in the transducer, and uses undersampling as a novel way to directly digitize sound waves. The proposed topology is based on a first-order FIR modulator; and two different oscillators are being used to implement this novel digital microphone. Before delving into details on two different circuit implementations using various oscillator types, conventional microphones are reviewed first.

4.1 Conventional Condenser Microphones

A condenser microphone operates as a variable capacitor formed by a diaphragm and a back electrode [Sinclair, 1998, p.19]. As a result, when the distance between the two electrodes changes due to impeding sound pressure waves, the capacitance varies accordingly. There are two main operating principles to detect this capacitance variation.

- 1) In low-frequency (LF) condenser applications the audio signal can be generated directly as shown in 4.1 a). A battery is connected to the two electrodes of the condenser

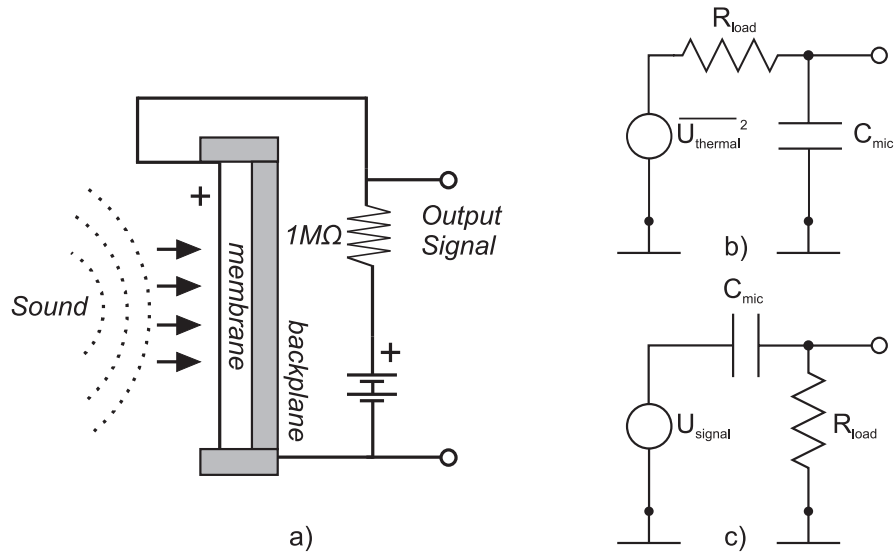


Figure 4.1: Schematic of a typical condenser microphone.

capsule, which produces an electrical potential between them. The amount of charge is determined by the voltage of the battery, the area of the diaphragm and back-plate, and the distance between the two. This distance changes as the diaphragm moves in response to sound. When the distance changes the voltage across a high impedance resistor, R_{Load} , changes accordingly. The signal read across the resistor needs to be amplified before being digitized by a close by A/D converter. Drawbacks of this approach include the noisy high-impedance load resistor which generates large quantities of thermal noise [Brauer et al., 2004]. In combination with the microphone capacitance, the load resistor creates an equivalent circuit of a low-pass filter of first order for the thermal noise (figure 4.1 b)), and the high-pass RC network characteristic prevents measuring low frequency audio signals (figure 4.1 c)). The high source impedance inherent to these LF methods must also be matched to the signal lines requiring amplifiers with very high input impedances [Hibbing, 2004]. 2) On the other hand, RF condenser methods use a high frequency carrier frequency onto which the sound signal is modulated utilizing oscillators. As a result, the audio signal needs to be demodulated thereafter. Even though this approach is more complicated compared to LF methods, it alleviates some of the LF methods drawbacks. The condenser capsule impedance can be decreased by using a high frequency carrier signal as $Z = \frac{1}{2\pi f C_{\text{mic}}}$. Also, the impedance can be kept constant as it is independent of the input sound signal [Hibbing, 2004].

4.2 *RF-Topologies*

There are two basic ways to implement condenser microphones based on RF methods. Either the condenser capsule's capacity is part of an oscillator's resonant circuit, so that the oscillator's frequency is modulated with the audio frequency and can be demodulated with a usual frequency demodulator or discriminator. Or, alternatively, a fixed oscillator generates a fixed frequency and the condenser capsule's capacity is part of the frequency demodulator, so that with the audio frequency it de-tunes the demodulator and thus produces the audio signal [Sennheiser, 1989]. The first approach is adopted here as the FIR sigma delta modulator proposed in section 3 can be used to directly digitize the frequency modulated signal produced by the oscillator. In this chapter, two different oscillator implementation were used to realize the microphone circuit. Firstly, an LC-oscillator where the condenser capsule replaces the varactor in the LC-tank was used to create a frequency modulated signal according to the impeding sound waves. Secondly, connecting a single resistor-capacitor network to an inverting Schmitt trigger will produce an oscillator creating a frequency modulated signal proportional to the modulating sound waves. In both approaches this frequency modulated signal is under-sampled before being digitized by a first order FIR modulator. As will become apparent shortly, the modulation due to a change in the condenser capsule capacity with impeding sound waves is often very small resulting in only minor frequency modulation. This in turn makes it difficult to achieve a high dynamic range in the digital output signal. Employing high frequencies of the oscillator will alleviate this problem as outlined in the following sections but increases requirements on the sampling circuitry responsible for handling the frequency-modulated signal. As a consequence both circuits presented in this chapter utilize undersampling to efficiently handle high frequency signals.

4.2.1 LC-Oscillator based FIR approach

As shown in figure 4.2 a sampling D-FF can be connected to an LC-oscillator where the varactor has been replaced with a transducer. Sound pressure waves will thus create a modulated signal at the output of the LC oscillator prior to digitization with the

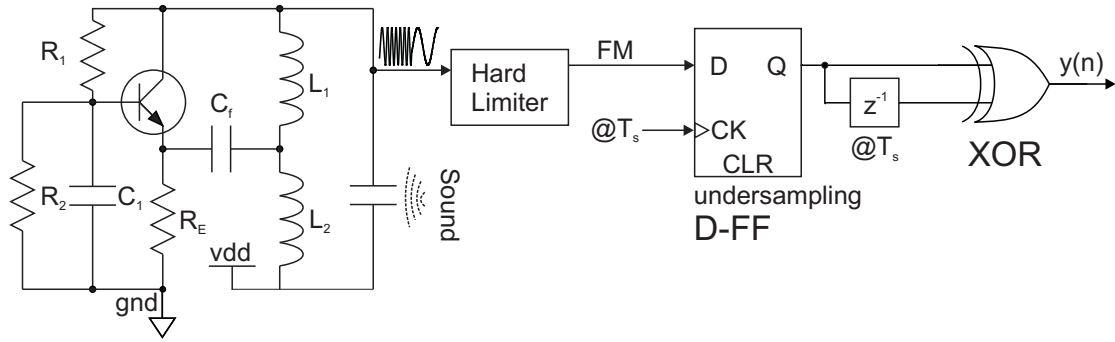


Figure 4.2: Digital microphone based on an LC-oscillator. The LC-Oscillator operates at approximately 9MHz with the sampling frequency, F_s , set to 1.2MHz.

FIR modulator from section 3. The performance of the condenser microphone is then determined mainly by the nonlinearities of the diaphragm, phase noise of the oscillator, and jitter of the sampling clock. The nonlinearity of the diaphragm depends on the diaphragm chosen to the acoustic area of application, the tonal character of the audio to be recorded, and the expectations and requirements with regard to the resulting sound character. For a detailed treatment of the nonlinearities of condenser microphones and how they are perceived by the human ear the reader is referred to [Earl and Lidia, 2003; Peus, 1997]. Since there is no feedback in the FIR modulator, the overall performance of the system will be only as good as the oscillator. Phase noise inherent to autonomous circuits such as oscillators will directly add to the output [Hegazi et al., 2004]. To realize the circuit shown in figure 4.2, a Behringer B1 condenser microphone was obtained and the capsule was extracted. Measurements showed that the center capacitance of the transducer and the approximate capacitance deviation when excited with sound in the case of the Behringer B1 microphone were approximately $60\text{pF} \pm 0.1\text{pF}$. A common-base oscillator approach was adopted for the LC Oscillator to form the frequency modulated signal. For the design process the following approach was adopted.

- The small-signal model of the oscillator is used to analyze and determine all circuit component values.
- The oscillator is simulated in Spectre(RF) to gain insight into tuning sensitivity, non-linearity and noise figures.
- In Spectre, the FIR modulator is then simulated and results are observed

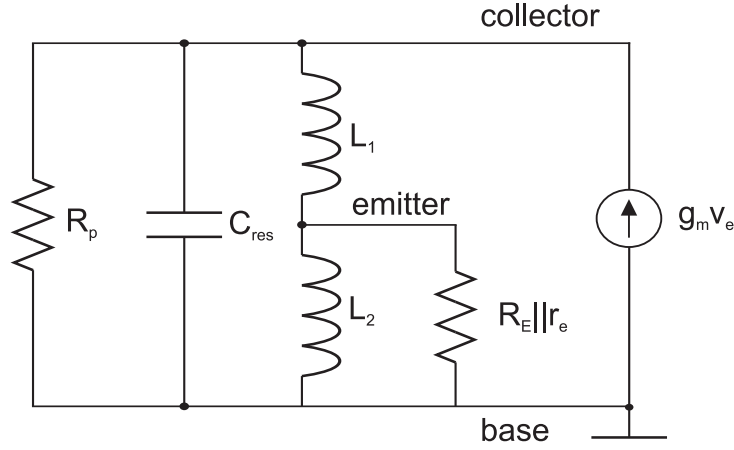


Figure 4.3: Small-signal equivalent circuit of the Hartley common-base circuit.

- A printed-circuit-board implementation of the FIR modulator is realized using discrete SMD components and experimental results are recorded and analyzed.

The small signal model for the common-base Hartley oscillator was thus found first and is given in figure 4.3. Note, that the capacitance C_f was ignored as its reactance is assumed to be negligible to the reactance of L_1 . To design the oscillator, the closed-loop system equations were found by summing the currents at the collector:

$$v_c \left(sC + \frac{1}{R_p} + \frac{1}{sL_1} \right) - v_e \left(gm + \frac{1}{sL_1} \right) = 0 \quad (4.1)$$

At the emitter:

$$v_e \left(\frac{1}{sL_1} + \frac{1}{sL_2} + \frac{1}{R_E} + \frac{1}{r_e} \right) - v_c \left(\frac{1}{sL_1} \right) = 0 \quad (4.2)$$

This can be solved in several ways; however, a matrix expression:

$$[Y][v] = 0 \quad (4.3)$$

will yield:

$$\begin{bmatrix} sC + \frac{1}{R_p} + \frac{1}{sL_1} & -gm - \frac{1}{sL_1} \\ -\frac{1}{sL_1} & \frac{1}{sL_1} + \frac{1}{sL_2} + \frac{1}{R_E} + \frac{1}{r_e} \end{bmatrix} \begin{bmatrix} v_c \\ v_e \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (4.4)$$

The poles will be formed by the determinant of the matrix. To find the conditions for oscillation, we can set the determinant to zero and solve.

$$\left(sC + \frac{1}{R_p} + \frac{1}{sL_1} \right) \left(\frac{1}{sL_1} + \frac{1}{sL_2} + \frac{1}{R_E} + \frac{1}{r_e} \right) - \left(\frac{1}{sL_1} \right) \left(gm + \frac{1}{sL_1} \right) = 0 \quad (4.5)$$

When the substitution is made that $s = j\omega$, even-order terms (s^2 and constant term) will be real, and odd-order terms (s^3 and s) will have a $j\omega$ in them. Thus, when the even-order terms are summed to zero, the result will be an expression for gain. When odd-order terms are summed to zero, the result will be an expression for the frequency. When assuming $R_E = \infty$ then the result for the odd-order terms is:

$$\omega = \frac{1}{\sqrt{C(L_1 + L_2) + \frac{L_1 L_2}{R_p r_e}}}. \quad (4.6)$$

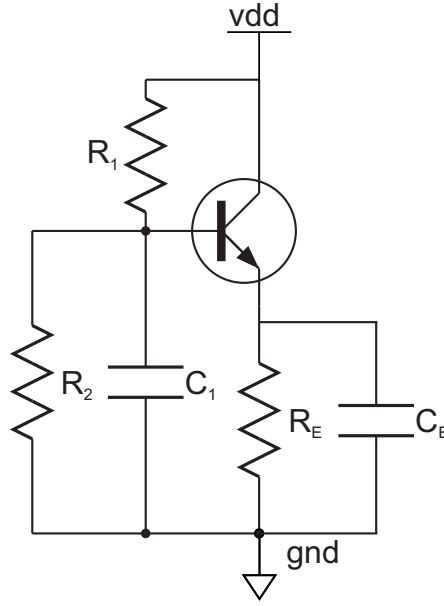
The result for the even-order term:

$$gm = \left(1 + \frac{L_1}{L_2}\right) \frac{1}{R_p} \quad (4.7)$$

Thus, for the oscillator to start oscillating the gm-value has to be greater than $(1 + L_1/L_2)/(R_p)$. The capacitor C_f is to prevent a short circuit from the collector node to the emitter node via L_1 . In order for C_f not to influence the operation of the oscillator, its reactance value should be negligible in comparison with that of inductor L_1 . Then, the node between L_1 and L_2 is directly connected to the emitter. However, it was found that if C_f is made too big the wide band-width of the low-pass feedback network will result in low frequency oscillations. To bias the oscillator a one-battery biasing scheme as shown in figure 4.4 was adopted. The bias-circuit components R_1, R_2, R_E are selected to produce a given current flow under no-signal conditions. The collector current I_c should be set to a value to produce the required output power. With the correct bias-feedback the output power is about 0.25 times of the input power. Thus, divide the desired output power by 0.25 to obtain the needed input power. For a given supply voltage V_{CC} , I_c can then be found by dividing the input power by V_{CC} . The equations given below can then be used to establish the desired collector current I_c and collector-emitter voltage V_{ce} . For $\beta > 1$, $I_c \approx I_e$. It is important that for best stability V_e is normally about 10% – 20% of V_{CC} .

$$R_e = \frac{V_e}{I_c} \quad (4.8)$$

$$V_b = V_e + V_{be} \approx V_e + 0.6 \quad (4.9)$$

**Figure 4.4:** One-battery biasing

Selecting $I_{R2} = 10I_b = 10I_c/\beta$:

$$R_2 = \frac{\beta V_b}{10I_c} \quad (4.10)$$

Finally,

$$R_1 = \frac{\beta(V_{CC} - V_b)}{11I_c} \quad (4.11)$$

When testing the biasing circuit it was validated that V_e is about 10% – 20% of V_{CC} and than V_b is 0.6 V higher than V_e . There are many other biasing schemes each applicable for a certain application. For other biasing schemes the reader is referred to [Rhea, 1995, (pp.133ff)]. The capacitor C_1 and any power supply by-pass capacitors should be such that the reactance is $< 5\Omega$ [Lenk, 1999, pp.59ff]. Capacitors C_1 and a possible capacitor in parallel to R_E must bypass the radio frequency signal, and therefore, should have relatively high values. C_E is selected such that its reactance at the resonance frequency is negligible in comparison with R_E [Misra, 2001, pp.455ff]. Similarly the parallel combination of R_1 and R_2 must be infinitely large in comparison with the reactance of C_1 . This design process for a common-base oscillator is only an initial step. Having done the initial calculations first, Spectre(RF) was used to design and simulate the common-base LC oscillator from figure 4.2. The values for the bias network

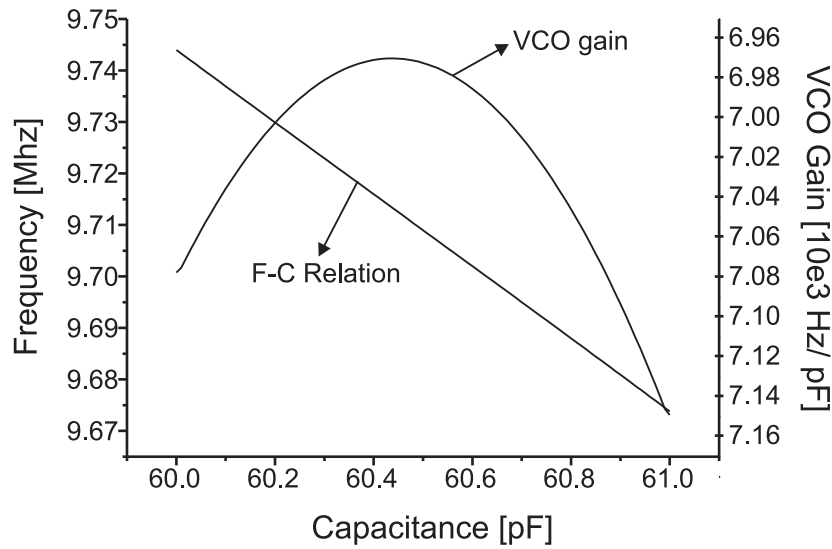


Figure 4.5: Linearity and tuning sensitivity of the LC oscillator.

were set to $R_1 = 10k\Omega$, $R_2 = 20k\Omega$, $R_E = 1k\Omega$, $C_1 = 100pF$, $C_f = 180pF$, $L_1 = 2\mu H$, $L_2 = 2\mu H$, and the capacitance C was varied in accordance with the obtained condenser capsule. Thus, the capacitance was set to $60pF$ and changed by approximately $1pF$. The frequency of the circuit is given by L_1 , L_2 , and C . The total inductance is given by $L_1 + L_2$. Ideally, the capacitance should be 2 pF per meter, where the wavelength in meters is found by $300/\text{frequency}(\text{MHz})$ [Lenk, 1999, p.63]. However, the transducer capacitance was fixed at $60pF$ and could thus not be changed. Alternatively, an inductive reactance between 80Ω and 100Ω at the operating frequency is a good guideline as well. Since the transducer capacitance is rather large two small $2\mu H$ inductors had to be used. Since $v = L \frac{di}{dt}$ and $i = C \frac{dv}{dt}$, reducing the inductors even further, however, will require large currents spikes which the active device might not be able to provide. First, a tuning sensitivity and linearity (Swept PSS) simulation was performed and the results are depicted in Figure 4.5. As can be seen from the figure the frequency of oscillation is around $9.71MHz$ and varies almost linearly with a change in capacitance. The change in capacitance is depicted on the x-axis and is in the range from $60pF$ to $61pF$. Also shown in figure 4.5 is the derivative of the dependency of the frequency of oscillation with respect to a change in capacitance. This derivative, which is also the gain of the oscillator, K_{vco} , gives insight into the linearity. As can be seen there is a small non-linearity associated with the oscillator. This will result in even and odd

order harmonics in the output spectrum as will be shown shortly. Note, that this non-linearity is due to the oscillator and not due to a varactor or transducer, which when implemented, will add a further nonlinearity. In case of a transducer from a condenser microphone, a certain non-linearity is desired as it will make sound be perceived in a more pleasant way [Earl and Lidia, 2003]. In a second simulation step the complete FIR modulator from figure 4.2 was simulated in Spectre. That is, the output of the oscillator was hard-limited and the de-modulation scheme using an XOR gate and D-FF was used to demodulate and digitize the frequency-modulated signal. The capacitance was changed with a sinusoid of frequency 440Hz. Based on the linearity plot shown in figure 4.5 the center capacitance was set to 60.5pF and varied by 0.1pF. Since the change in capacitance is in reality very small also, undersampling the frequency-modulated signal was utilized. That is, the sampling frequency is much lower than the frequency of the oscillator. Undersampling results in a frequency translation and is thus an efficient way to deal with high frequency signals. This undersampling results in reduced component count because a complete analog down-conversion stage is eliminated. As a consequence, care must be taken to choose a sampling frequency F_s . The sampling frequency must be chosen such that there is no overlapping of the aliased components. This means that the sampling frequency must be at least twice the signal bandwidth, and the sampled signal must not cross an integer multiple of $F_s/2$ [Analog Devices, 1998, p.5]. Undersampling eases requirements on the sampling circuitry as lower clock frequencies are needed. Furthermore, as less samples are taken on-line digital signal processing will require less computation effort. Note, that undersampling still satisfies the Nyquist criterium as the sampling frequency is still higher than twice the bandwidth of the signal of interest. The obtained data values were exported to Matlab and the power spectral density obtained. The PSD plot is shown in Figure 4.6. As seen in the figure, the fundamental is at the expected frequency of 440Hz. The quantization noise is nicely shaped out of the band of interest to first order. Having used Spectre to simulate the LC-oscillator FIR modulator the topology from figure 4.2 was implemented.

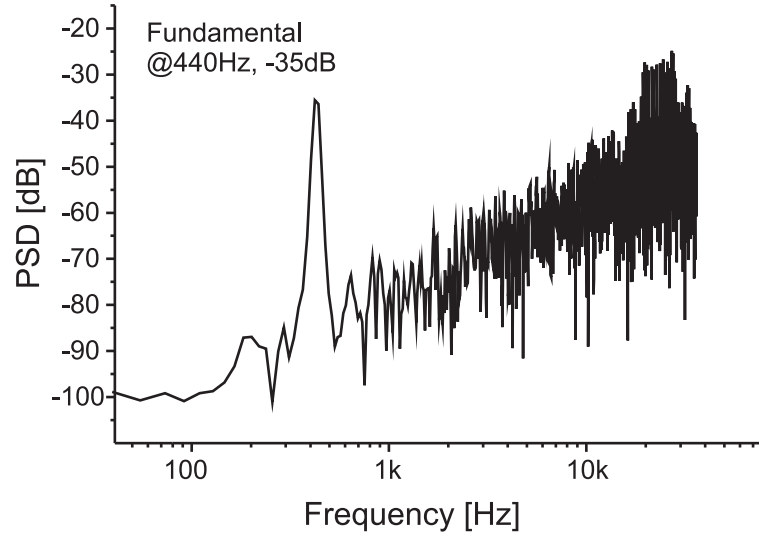


Figure 4.6: PSD plot of the output of a 1st order LC-oscillator FIR modulator simulated in Spectre. Details: $F_{in} = 60.5pF + 0.1pF \times \sin(2\pi 440t)$, $F_s = 1.4142135MHz$.

Even though all design parameters were selected carefully it was found that when implementing the oscillator on a printed circuit board using discrete SMD components the oscillator would often not show the desired results, and a trial-and-error approach was adopted to fine-tune the components values. With the two $2\mu H$ inductors the LC oscillator showed a free running frequency of about 9MHz. With a 0.1pF change of capacitance due to modulation, the anticipated change in frequency was 9kHz, requiring a minimum sampling frequency of $\approx 20kHz$. A hard limiter was used to rectify the FM signal before feeding it into a data-acquisition board. The data-acquisition board essentially performed the sampling operation. The obtained values were exported into Matlab where digital signal processing was done. This entailed delaying each sample and feeding it into a digital XOR gate which demodulated the frequency-modulated signal as depicted in Figure 4.2. The sampling frequency F_s was set to 1.2MHz. This undersampling frequency F_s was well above the anticipated Nyquist frequency. The overall circuit was excited with voice samples ($\approx 88dB$ SPL) as well as pure sine waves at a frequency of 440Hz. The PSD of the modulator output with a 440Hz sine wave at the input is shown in figure 4.7. As seen from figure 4.7 the quantization noise is nicely attenuated at low frequencies while it becomes more dominant at higher frequencies. As shown by the dashed line in figure 4.7, the noise is attenuated sufficiently till about

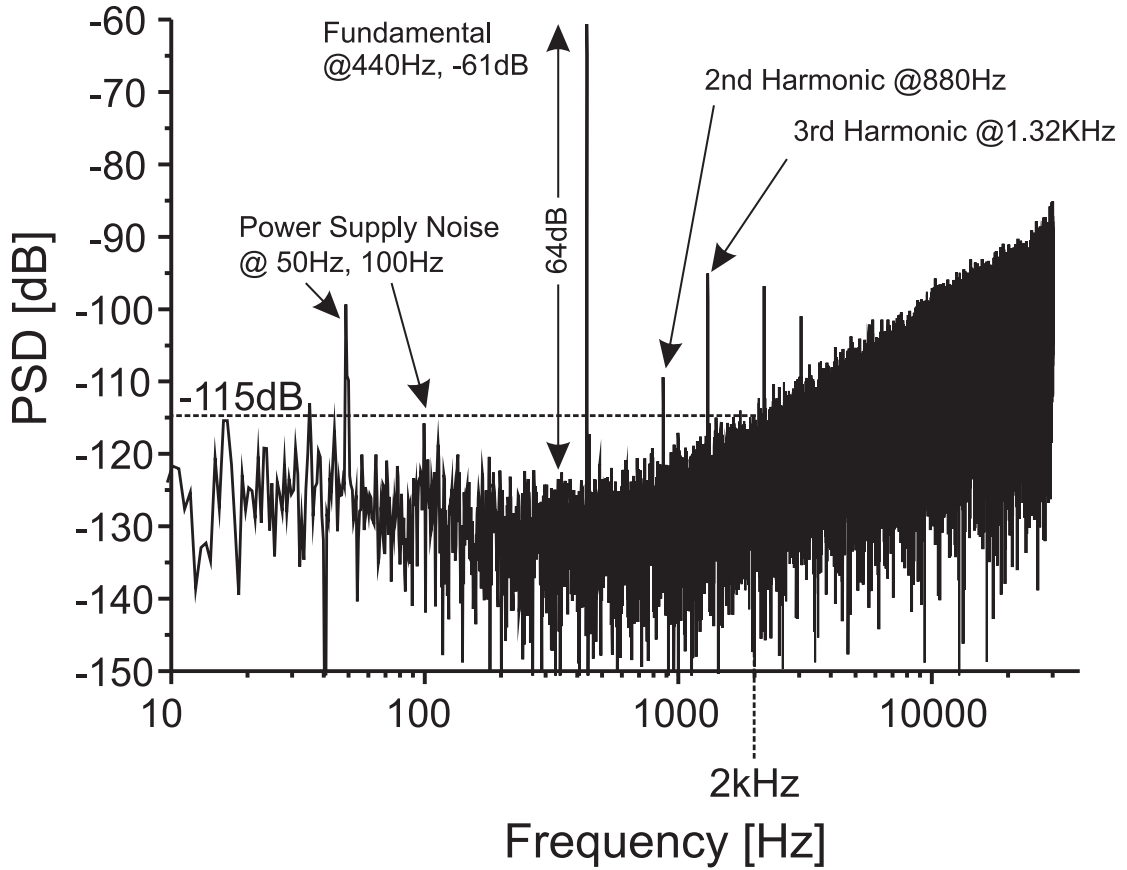
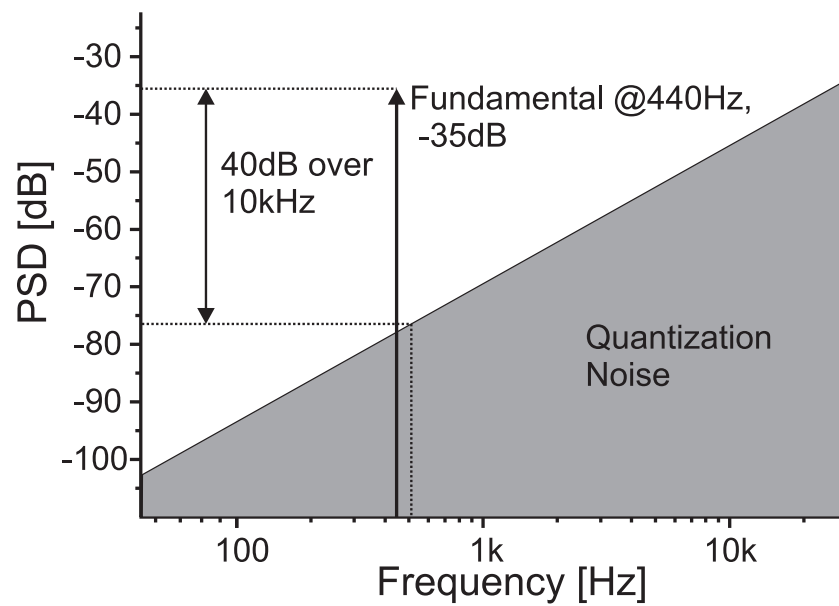
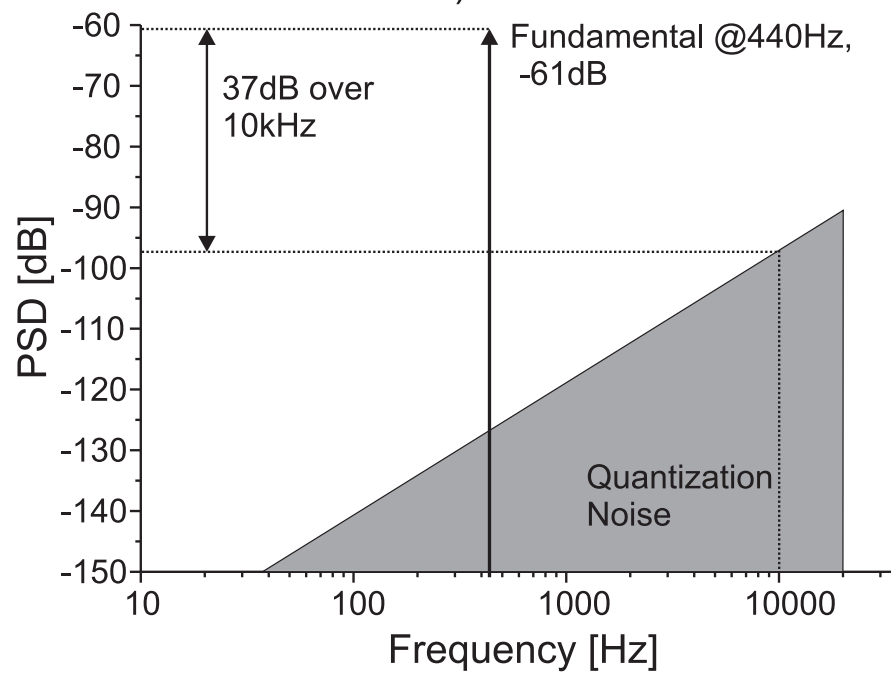


Figure 4.7: Power spectral density plot of the acquired digital output of the digital microphone. The Figure shows the fundamental at 440Hz and its harmonics. The fundamental is at -61dB. Also shown is the power supply noise at multiples of 50Hz. Circuit/Acquisition details: $F_s = 1.2\text{MHz}$, $F_{in} = 440\text{Hz}$, $N = 2^{21}$ samples, $f_c \approx 9\text{MHz}$

2kHz. At this frequency the noise floor rises and will become more audible with respect to the fundamental input signal. Over this frequency range the dynamic range is approximately $115-61=54\text{dB}$. Compared to the Spectre simulation result from figure 4.6 the performance seems not as good, however, when overlaying the two graphs and considering a signal bandwidth of 10kHz for comparison, the dynamic range is almost identical. This can be seen in Figure 4.8. Figure 4.8 a) shows the simplified result of the FIR modulator simulated in Spectre, whereas part b) of the figure shows the simplified result obtained from the implemented FIR modulator on a PCB board. Considering a bandwidth of 10kHz, the simulation results are almost identical. Also note that at low frequencies, the spectrum of the FIR modulator simulated in Spectre is quieter as no power supply noise is present. Additionally, there is no low-frequency contamination due to background noise which was picked up by the condenser capsule. Figure 4.7 also reveals the two main limitations to the performance of the circuit used. Firstly, knowing that the output-amplitude is scaled according to equation 3.27, the signal output level of -61dB suggest a frequency modulation of approximately 1060Hz. This is due to the small capacitance change in the condenser capsule. Thus, it is desirable to use a large diameter condenser capsule resulting in a higher frequency modulation and thus in a higher signal-to-noise ratio. However, a better alternative is to utilize a higher frequency oscillator which will result in more frequency modulation and is a good way to increase performance. Since the frequency of oscillation is determined by $f = \frac{1}{2\pi\sqrt{LC}}$, if the frequency of the oscillator is increased by a factor of M with a fixed transducer, then the modulation is increased by a factor of \sqrt{M} . This approach is especially advantageous when using an integrated circuit approach as the frequencies can be much higher than with the discrete circuit here used. Undersampling the frequency modulated signal will then provide the ideal means to process the very high frequencies which can be achieved by an integrated circuit approach. Also shown in figure 4.7 are the harmonics of the fundamental frequency which are mainly due the characteristic non-linearity of the condenser capsule but also due to the non-linearity of the oscillator. Secondly, as seen in Figure, 4.7, the power supply noise adds to the quantization noise,



a)



b)

Figure 4.8: Figure depicting the comparison between the PSD results of the Spectre simulation to the PSD results from the circuit realization. Part a) shown the results from the Spectre simulation. Part b) depicts the results obtained from the LC-oscillator circuit implementation.

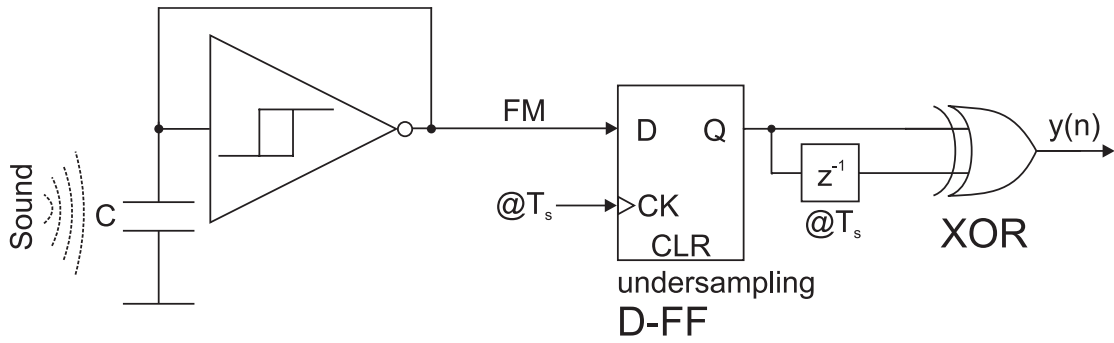


Figure 4.9: Delta sigma modulator utilizing a Schmitt-trigger oscillator as integrator, sampling D-FF and phase detector. Implemented Schmitt-trigger oscillator oscillates at approximately 91MHz. The sampling frequency, F_s , was set to 0.8 MHz.

with the fundamental occurring at 50Hz. Thus, it is important to appropriately decouple the oscillation circuit from the power supplies, or use a battery powered approach. This circuit noise which resides at low frequencies is mixed with low frequency background sound, picked up by the condenser capsule. In conclusion, the LC-oscillator utilized to implement a digital FIR microphone gives a proof of concept for the FIR modulator digital microphone; however, the performance in terms of SNR is rather limited with the circuit used. To improve upon the results obtained, one would have to assemble a more professional circuit, ideally an integrated approach, to reduce circuit noise. This would also result in higher frequencies of oscillation increasing the performance. More specifically, a factor M increase in oscillation frequency of the oscillator will yield a \sqrt{M} factor increase in modulation-width increasing the output amplitude by roughly 3dB for doubling M . Since the experimental circuit uses 1st order noise shaping, a convenient way to further improve the SNR is to extend the topology from figure 4.2 to a second order topology.

4.2.2 Schmitt-Trigger Oscillator FIR approach

As a second implementation, an inverting Schmitt-trigger was used to realize an oscillator as shown in 4.9. This approach was adopted to move towards a more integrated approach by ridding the FIR modulator from the previous section of the undesirable inductor. As seen in figure 4.9, the transducer is now connected to the input of the inverting Schmitt trigger. Thus the RC network consisting out of the transducer and the

high frequency impedance of the feedback wire will change the oscillation proportionally to the impeding sound waves. With the 60pF transducer and no additional resistor in the feedback path, the frequency of the circuit was about 91MHz. This frequency should improve the performance by roughly $\sqrt{10}$ compared to the LC-oscillator approach from the previous section which oscillated at 9MHz. Thus, we expect about 9dB more SNR. With a 0.1pF change of capacitance, the anticipated change in frequency of $f \approx \frac{1}{RC \ln 2.26}$ due to modulation was about 150 kHz. Utilizing a Schmitt trigger, there is no need to use an explicit hard limiter to rectify the FM signal before feeding it into a data-acquisition board. As in the case with the LC oscillator undersampling was used to down-convert the 91MHz signal and thus ease the requirements on the sampling circuitry. The obtained values were exported into Matlab where digital signal processing was done. This included delaying the sampled FM signal and feeding into an XOR gate as depicted in figure 4.9. The sampling time T_s was set to 0.8MHz. This undersampling frequency T_s was well above the anticipated Nyquist frequency of 40kHz. The overall circuit was excited with voice samples (≈ 88 dB SPL) as well as pure sine waves. The PSD of the modulator output with a 1kHz sin-wave at the input is shown in figure 4.10. As seen from figure 4.10 the quantization noise is nicely attenuated at low frequencies. The figure also shows a dashed line indicating that the noise floor is nicely attenuated until about 20kHz. Over this range the dynamic range is approximately 68dB. Comparing this to the results of the LC-oscillator approach shown in Figure 4.7, we obtained more dynamic range over a 10 times higher frequency band by utilizing a more integrated approach. The main limitation of the approach used here is again due to the small capacitance change in the condenser capsule. Even though the frequency of oscillation is higher than in the LC-oscillator case, it is limited by the rather large condenser capacitance of 60pF to about 91MHz. An even higher frequency oscillator would alleviate some of the drawbacks as a higher frequency will result in more frequency modulation and is a good way to increase performance. Thus a completely integrated circuit approach is more appropriate as the frequencies can be even

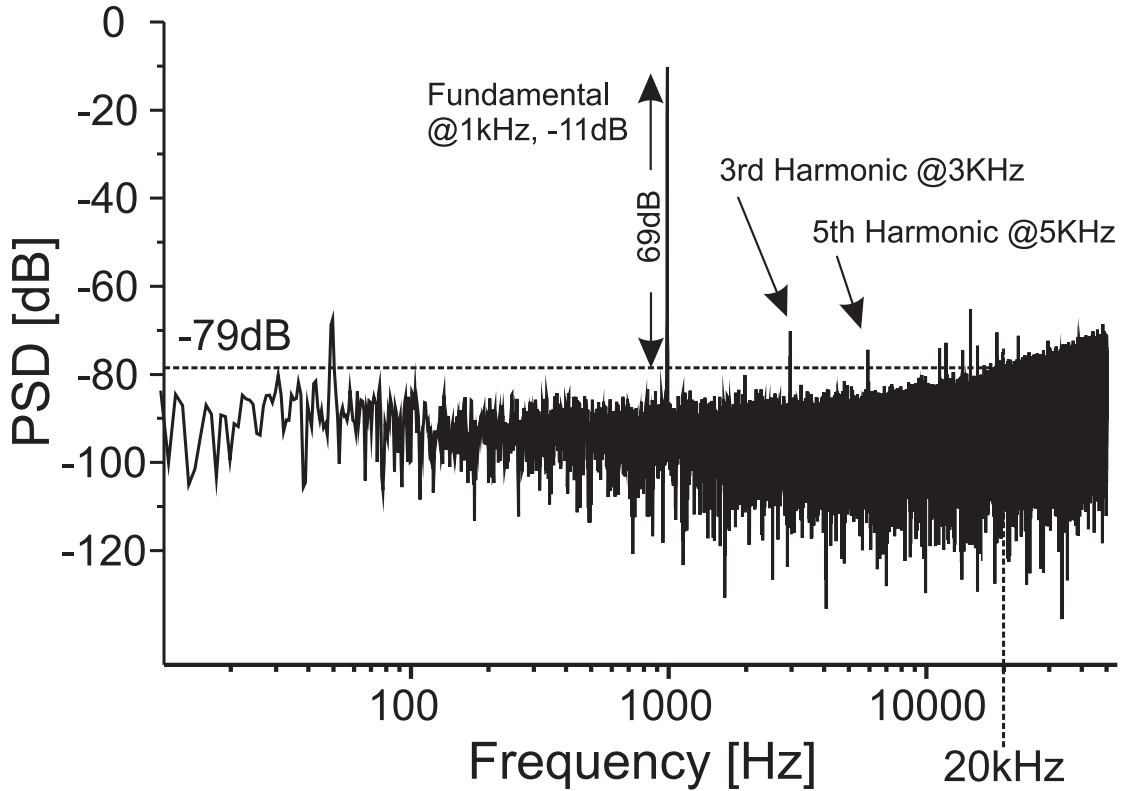


Figure 4.10: Power spectral density plot of the acquired digital output of the digital microphone. The figure shows the fundamental at 1kHz and its harmonics. The fundamental is at -11dB. Also shown are the harmonics at multiples of 1kHz. The dashed lines shows that a slightly higher dynamic range as in the LC oscillator is achieved but over a ten times higher bandwidth. Circuit/Acquisition details: $F_s = 0.8\text{MHz}$, $F_{in} = 1\text{kHz}$, $N = 2^{18}$ samples, $f_c \approx 91\text{MHz}$

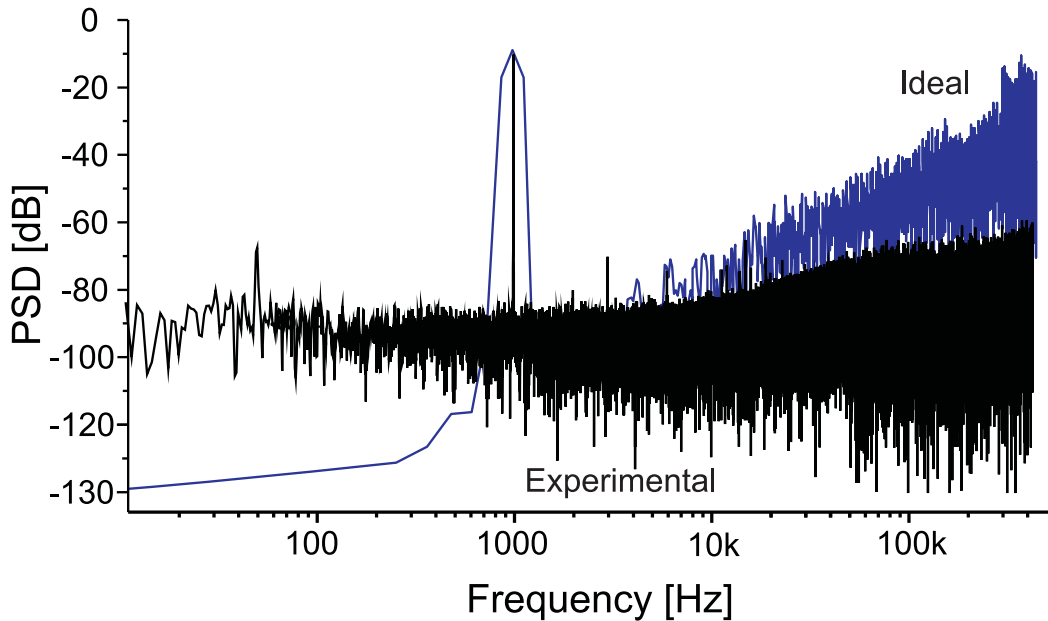


Figure 4.11: Comparison of an ideal first-order modulator simulated in Matlab to the obtained results from the Schmitt-Trigger Based FIR modulator from figure 4.10.

higher than with the discrete circuit used here. Compared to the LC-oscillator the signal is about 69dB above the noise floor whereas in the case of the LC-oscillator it is only 64dB. Thus, there is a 5dB improvement even though the sampling frequency F_s is slightly lower at 0.8MHz. It is also noted that the noise floor is almost constant up until 20KHz resulting in a high dynamic range over the entire audio band. After the 20kHz mark the noise floor starts rising, but still at a lower rate than in the case of the LC-oscillator. In figure 4.11 a comparison is shown to an ideal first-order FIR modulator simulated in Matlab. As seen in the figure the low-frequency noise is much lower in the ideal case as no circuit noise is present. Interestingly, the noise shaping is less pronounced in the experimental setup while the quantization noise of the ideal modulator rises as expected. While the overall performance does not yet compare to commercial products, the Schmitt-trigger implementation shows that an oscillator with a higher frequency will result in better performance as it achieves reasonable resolution over the entire audio band. Also, in contrast to the LC-oscillator circuit, the Schmitt-trigger circuit was powered by a battery, thus reducing power supply noise at multiples of 50Hz. In conclusion, the Schmitt-trigger based FIR digital microphone improves upon the results from the LC-oscillator based approach. A higher dynamic range is achieved by utilizing higher frequencies of the frequency-modulated signal.

4.3 *Conventional Setup*

To compare the obtained results for the LC-oscillator and the relaxation oscillator approach, a condenser microphone was used in a conventional setup. The microphone was setup utilizing a Tascam US-122 USB Audio/MIDI Interface and recordings of two sine waves were done. The resulting plots of the power-spectral densities for a 1kHz and 440Hz sin wave are depicted in Figures 4.12 and 4.13. When observing the two figures and comparing them to the results of the LC-oscillator and Schmitt-trigger setup, one observes a comparable noise floor region towards dc. At higher frequencies the quantization noise floor in the FIR microphone circuits becomes more dominant as it is only noise shaped to first order. The conventional setup on the other hand retains its low

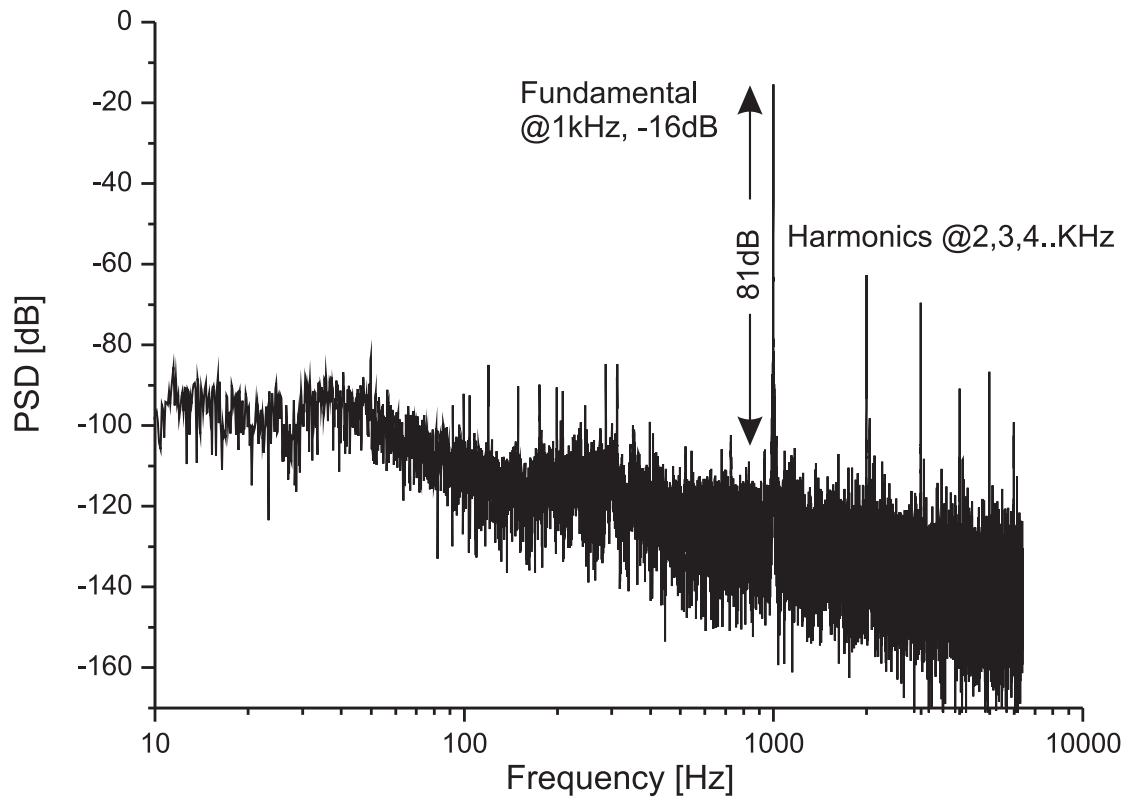


Figure 4.12: Power spectral density plot of the acquired digital output of the conventional condenser microphone setup. The figure shows the fundamental at 1kHz and its harmonics. The fundamental is at -16dB. Also shown are the harmonics at multiples of 1kHz. Circuit/Acquisition details: $F_s = 22\text{kHz}$, $F_{in} = 1\text{kHz}$

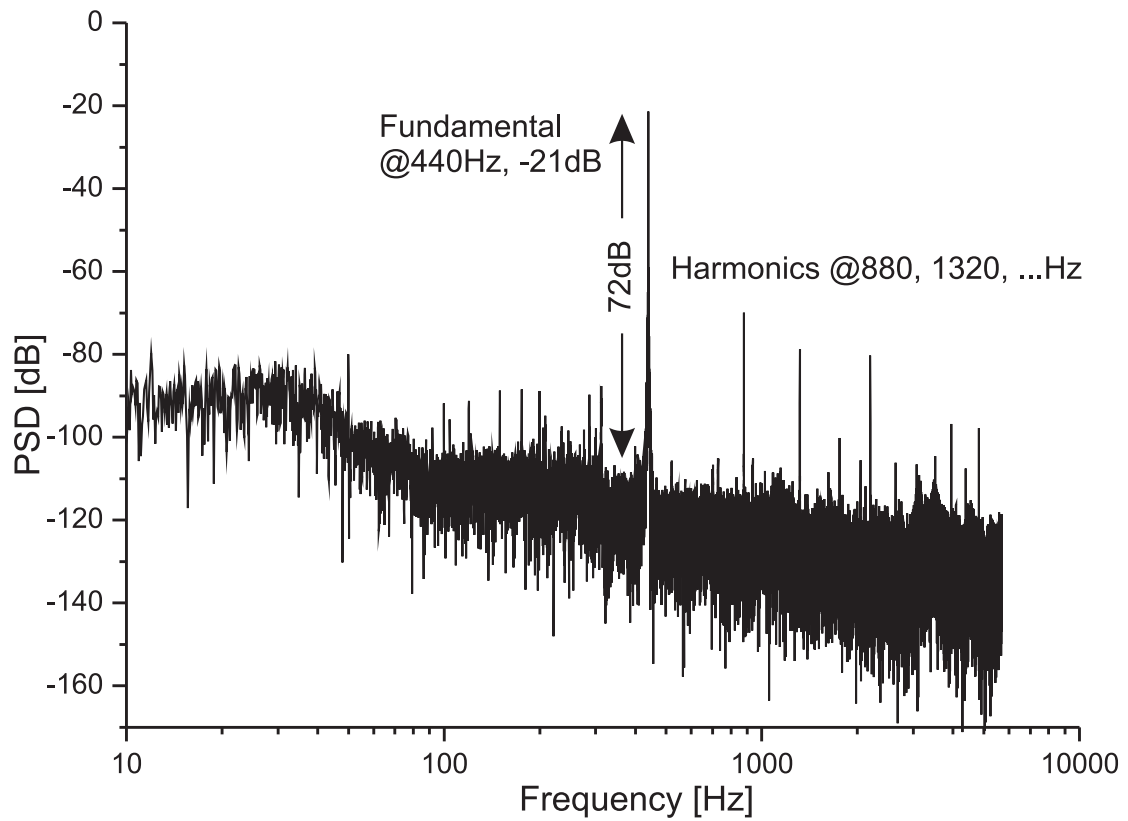


Figure 4.13: Power spectral density plot of the acquired digital output of the conventional condenser microphone setup. The figure shows the fundamental at 440Hz and its harmonics. The fundamental is at -21dB. Also shown are the harmonics at multiples of 440Hz. Circuit/Acquisition details: $F_s = 22\text{kHz}$, $F_{in} = 440\text{Hz}$

noise floor. This is because a higher-order delta-sigma converter capable of converting signals till 96kHz is used in the Tascam Audio/MIDI Interface. In order for the FIR microphone to obtain comparable results, higher order noise shaping would have to be employed as well as moving to an integrated approach.

4.4 Conclusion

In this section it was shown that a digital microphone can be realized by utilizing a first-order FIR delta-sigma modulator. A condenser capsule was used to modulate a carrier frequency utilizing a LC common-base oscillator and a Schmitt-trigger oscillator. The frequency-modulated signal produced was then directly digitized by undersampling it and utilizing a phase detector to demodulate it. Undersampling proofed as a good way to deal with the high frequencies produced by the oscillators, especially the Schmitt-trigger oscillator. Experimental results showed that the Schmitt-trigger approach not only has a higher dynamic range than the LC-oscillator FIR modulator, but also that it keeps this high value over a frequency band of up to 20Khz. This is mainly due to the 10-fold increase in frequency of oscillation, resulting in a more wide-band modulation. Advantages of using an FIR modulator with oscillator to implement digital microphones include the capability of measuring very low-frequency signals. In conventional condenser microphones this is not possible as the change in capacitance of the condenser capsule is read across a noisy high impedance resistor which forms a high-Pass RC network. This high-pass RC network prevents the measurement of low frequency audio signals. Another benefit is that the presented approach is easily expandable to integrated circuits using ring oscillators. As will be proposed later, an N-stage ring-oscillator with the condenser capsule sitting at one (or all) of the inverter output nodes could be used to frequency modulated a voice signal onto a carrier frequency. Considering the high frequencies of an integrated ring-oscillator much better results can be achieved as more modulation-depth is achieved. The increase in dynamic range with a much better circuit noise figure of an integrated approach should result in resolutions that are comparable to that of commercially available product.

CHAPTER V

SECOND-ORDER FIR SIGMA DELTA MODULATORS

5.1 *Introduction*

To achieve better noise shaping of the introduced quantization error, higher order topologies resulting in steeper noise transfer functions have to be utilized. While there are many architectures for implementing high-order noise transfer functions [Norsworthy et al., 1997, p.166], here, a cascade of first-order modulators is used [Matsuya et al., 1987]. This is because two first-order FIR modulators can be used to realize one second-order FIR analog-to-digital converter. The principle of cascaded sigma-delta modulation is based on the use of multiple modulator stages in a cascade configuration [Matsuya et al., 1987]. In ideal multi stage architectures, each successive stage accepts the quantization noise of the preceding stage as its input in order to create a digital signal which, in the ideal case, perfectly cancels out the quantization error introduced in the preceding stage. With a cascade of two modulators we can utilize the already introduced first-order FIR delta-sigma modulator from section 3 to create a second order topology. Then, this second order topology will implement second order noise shaping while still operating without any negative feedback. This chapter introduced various implementations of second order topologies based on a cascade FIR modulators. However, the FIR modulator deployed in the second stage of the cascade will be an all digital implementation as not oscillator is needed to produce a frequency modulated signal. Since a cascade needs the quantization error from the preceding stage, a way to obtain the quantization error is addressed first. There are essentially two cases which need considering for finding the error depending on whether the frequency of the oscillator, F_{vco} is much higher or much less than the sampling frequency, F_s . After the error detection scheme is

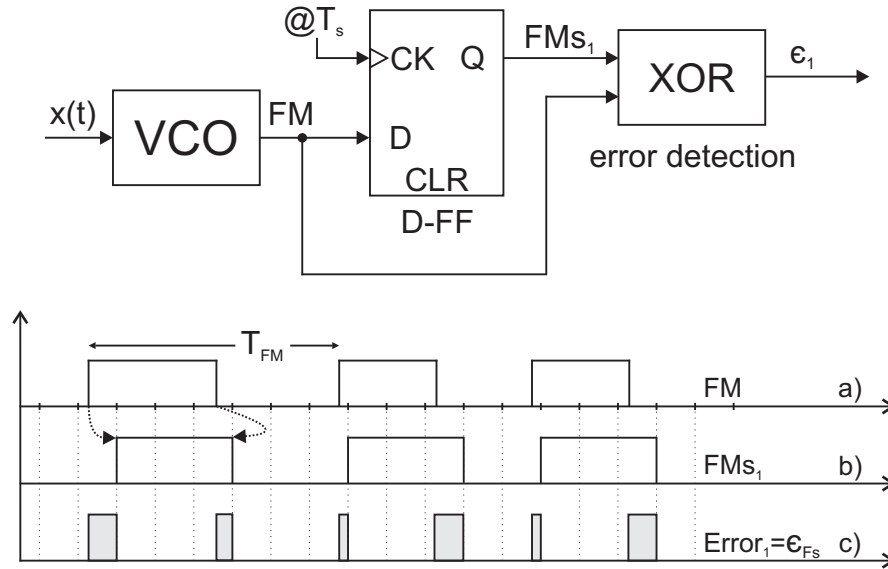


Figure 5.1: The figure shows the error introduced when sampling a frequency modulated signal with a clock frequency greater than the frequency of the VCO. Part a) shows the FM signal. The sampling clock is denoted by the dashed lines. The resulting sampled signal, FMs_1 , is shown in part b). This sampling introduces a timing error in each positive or negative edge which is depicted in part c) as the shaded area.

introduced, the following subchapters then deal with various implementations of second order modulators. These include two versions of cascaded first-order FIR modulators realizing an overall second-order topology. Simulation results are given along with a theoretical analysis. The chapter is concluded with a discussion and comparison of the two proposed topologies.

The basic thought behind a cascade is to feed the quantization error from the first modulator the second modulator. When the frequency modulated signal is sampled by a D-FF, for instance, a timing error is introduced as described in section 3.4. There are two main approaches to finding the quantization error introduced by the sampling D-FF. The easiest would be to utilize a simple XOR gate which gives the difference between the frequency-modulated signal, FM , and the sampled frequency-modulated signal, FMs . This is depicted in figure 5.1. Part a) of the figure shows the FM signal from the VCO being sampled by the clock (D-FF). The sampled signal, FMs_1 , is shown in part b) of the figure. The timing error in the positive and negative edges of FMs_1 is given by the shaded area in part c) of the figure. While using an XOR is certainly the most straightforward way of obtaining the timing error, the sampling frequency F_s has

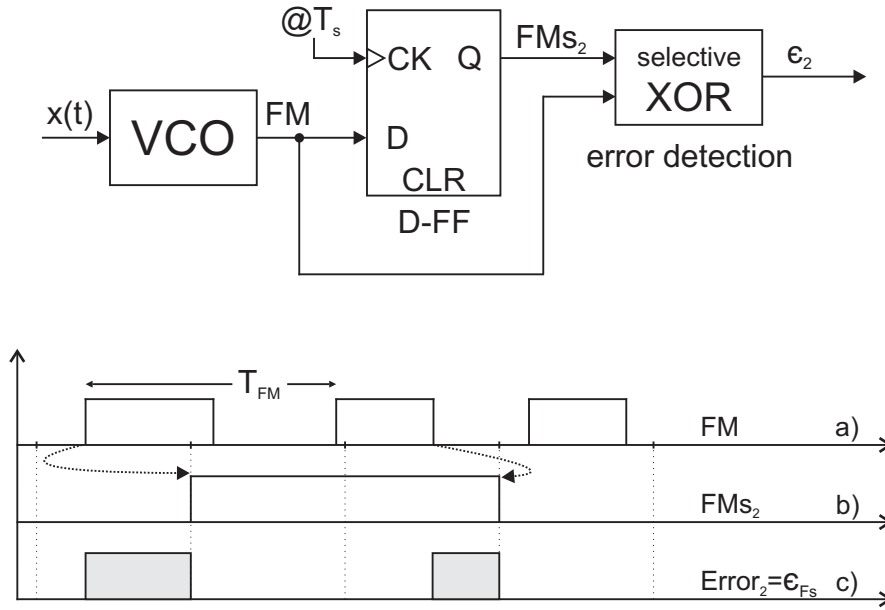


Figure 5.2: The figure shows the error introduced when under-sampling a frequency modulative signal. Part a) shows the FM signal. The sampling clock is denoted by the dashed lines. The resulting sampled signal, FMs_2 , is shown in part b). This sampling introduces a timing error in each positive or negative edge which is depicted in part c).

to be greater than the center frequency of the FM signal, F_c . If the center frequency of the VCO is much greater than the sampling frequency, then a simple XOR gate cannot be used. In the case that the frequency of the VCO is much greater than the sampling frequency, F_s , the timing error is the time from the *last* rising or falling edge of the asynchronous FM signal to the *current* rising or falling edge of the sampled signal, FMs_2 . This can be seen in Figure 5.2 in which the clock frequency F_s is four times slower. Again, the figure shows the asynchronous FM signal in part a) and its quantized equivalent, FMs_2 , in part b). The time-domain quantization error is given in part c) of figure 5.2. A simple XOR gate would in this case not only give the timing error at instances when FMs_2 switches, but also whenever FM is different from FMs_2 . As a result, one would have to make sure to only process the correct error pulses in later stage of the digital circuitry and ignore the non-relevant ones. In figure 5.2 this is indicated by the selective XOR gate. This will be addressed in more detail in the following sections.

With these two error detection schemes in mind, the next sections show various topologies of second order modulators based on a cascade of two first-order FIR modulators. These different versions are divided into architectures using negative feedback

and architectures operating without negative feedback.

5.2 *Second-Order FIR Modulators*

As the emphasis of this work is on delta-sigma modulator topologies utilizing no feedback, the topologies presented in this section are based on two first-order FIR modulator. Two versions of second-order modulators are introduced. First, a topology is devised based on the cascade of two first-order FIR modulators which strongly resembles a conventional cascade of delta-sigma modulators. That is, the second stage uses digital circuit components to realize an integrator and differentiator along with a time-domain quantizer needed to process the quantization error from the preceding stage. This topology is then simulated and performance results are discussed. To reduce circuit component count, the first version is re-designed by exploiting a novel signal processing feature inherent to the functionality of the proposed modulator. Furthermore, this refined version is also suitable for undersampling. Again, a performance evaluation is done and performance results are discussed.

5.2.1 Version I

The principle of cascaded structures was introduced in section 2.4.1 and with reference to figure 2.19 which depicts a cascade of two first-order sigma delta modulators, we can devise a second order modulator using the principle of FIR modulators without negative feedback as depicted in figure 5.3. Figure 5.3 shows a VCO, sampling D-FF and XOR making up a first-order FIR SDM. With the aforementioned limit, the quantization error of the first FIR SDM, ϵ_{Fs} , can easily be found by utilizing a XOR gate. This XOR gate gives the difference between the asynchronous frequency-modulated signal, FM , and the sampled frequency-modulated signal, FM_s . The error ϵ_{Fs} is the time error from each positive or negative pulse edge of the frequency-modulated signal to the positive or negative pulse edge of the sampled frequency-modulated signal. Utilizing an XOR gate is a simple way of obtaining this error, however, the sampling frequency F_s must be greater than the frequency of the oscillator, F_{vco} . When F_s is substantially lower than the frequency-modulated signal frequency, a different error detection scheme should be

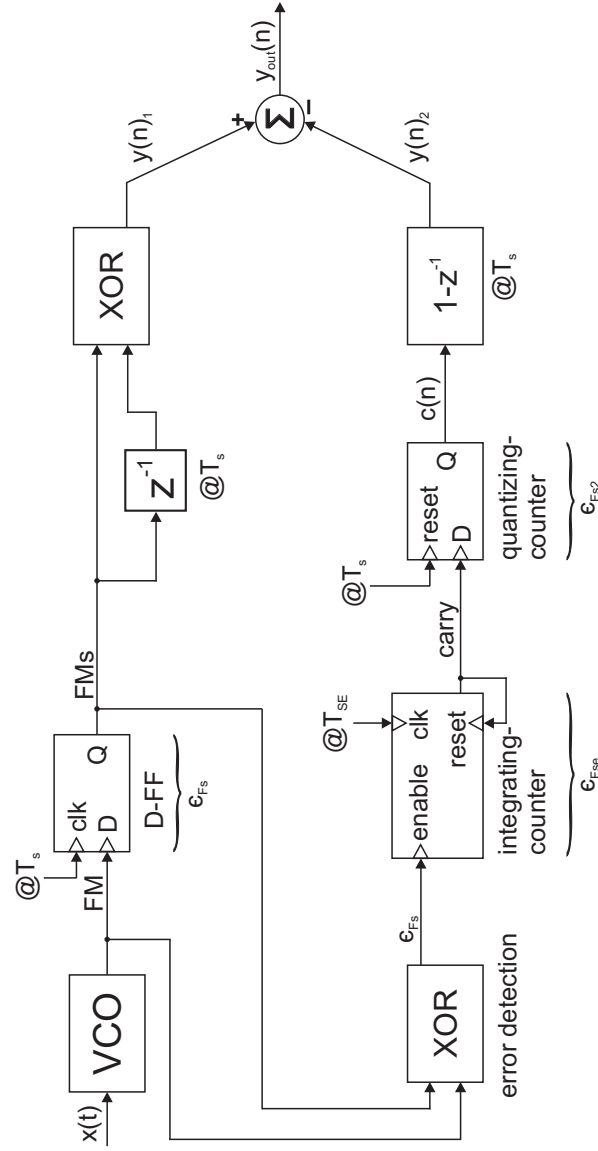


Figure 5.3: Second-order cascaded FIR SDM. An all digital second path is utilized to cancel out the quantization error introduced in the upper FIR SDM. The quantization error introduced in the first stage, ϵ_{Fs} , is found by utilizing a XOR gate. An integrating-counter and differentiating-counter make up the second FIR sigma-delta modulator processing the quantization error, ϵ_{Fs} , such that when the two outputs are combined the error ϵ_{Fs} is cancelled.

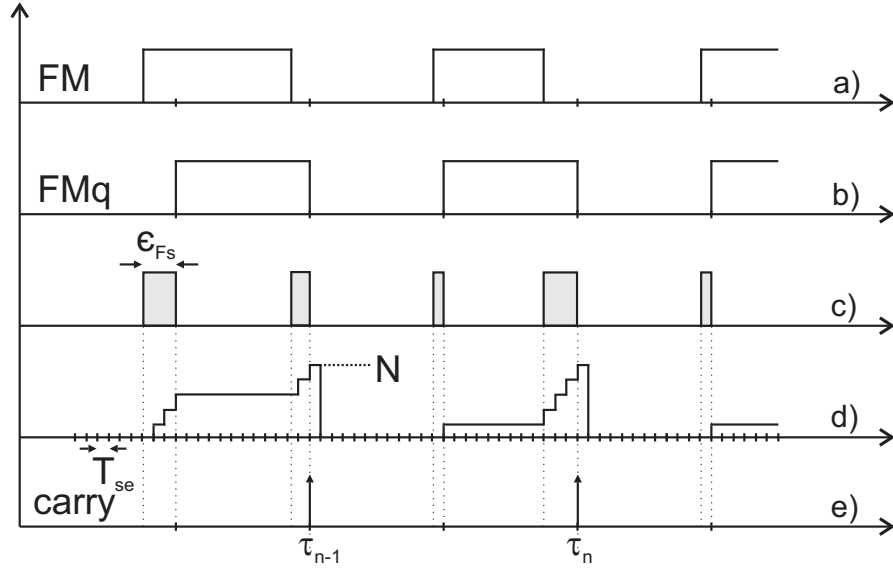


Figure 5.4: a) Asynchronous FM signal b) Sampled FMq signal c) The error signal ϵ_{Fs} as determined by the XOR gate d) The count value of the integrating-counter giving an estimate of the on-time or width of the error pulses e) The carry signal at time instances τ_n when the integrating-counter has reached its final count value N .

utilized. This approach will be outlined in the second version later. In either case, the error ϵ_{Fs} , is proportional to the widths, $\tau_{\epsilon_{Fs}}$, produced by the error detection circuit. Figure 5.4 shows the asynchronous FM signal and the sampled signal, FM_s , in parts a) and b), respectively. The signal produced by the error detection circuit is depicted in figure 5.4 c). To process this error we need to integrate the signal first, quantize, and then differentiate to shape the introduced quantization noise. This is exactly the same principle as in the case of the first-order FIR modulator from section 3.2. First, the error is fed into a first counter, the *integrating-counter* for further processing. The integrating-counter performs the signal processing operation of an integrator, similar to the one performed by the VCO. The heuristics behind this assertion are as follows. The integrating-counter is enabled with each positive going edge of the error signal ϵ_{Fs} . It then keeps counting up with an elevated frequency of F_{se} until it reaches its terminal count-value of N as shown in figure 5.4 d). At this time, τ_n , the carry signal goes high and the counter starts over, thus performing a modulo operation. The carry signal is depicted in figure 5.4 e). Since the counter only counts as long as an error pulse is present we can define the time instances the carry signal occurs as the time from the last

carry signal plus N times the clock time T_{se} :

$$\begin{aligned}\tau(n) &= \tau(n-1) + NT_{se} \epsilon_{Fs} \\ \frac{\tau(n)}{\epsilon_{Fs}} &= \int NT_{se} \iff \frac{\tau(z)}{\epsilon_{Fs}(z)} = \frac{NT_{se}}{1-z^{-1}},\end{aligned}\quad (5.1)$$

where $\epsilon_{Fs} = [0, 1]$. Thus the frequency of occurrence of the carry signal is dependent proportionally on the pulse-width of the error signal, as well as the final count value N . Essentially, the integrating-counter is a time-to-frequency converter, converting the width of the error signal produced by the XOR gate to a pulse frequency-modulated signal. However, since the integrating-counter uses the finite clock F_{se} , there will be an error between the ideal width of each error pulse and the width determined by the integrating-counter, which is a multiple of T_{se} . The normalized width of each error pulse as determined by the integrating-counter is given by an integer multiple of T_{se} and a fractional part:

$$\begin{aligned}\epsilon_{FsN} &= Q \left[\frac{\epsilon_{Fs}}{T_{se}} \right] = \left\lfloor \frac{\epsilon_{Fs}}{T_{se}} \right\rfloor + \underbrace{\left\langle \frac{\epsilon_{Fs}}{T_{se}} \right\rangle}_{\epsilon_{Fse}} \\ &= \lfloor \epsilon_{Fs} \rfloor + \epsilon_{Fse},\end{aligned}\quad (5.2)$$

where ϵ_{Fse} is the new error due to the finite clock of the counter, F_{se} . Thus equation 5.1 is re-written and the output of the integrating-counter is given by:

$$\tau(z) = \lfloor \epsilon_{Fs} \rfloor \frac{NT_{se}}{1-z^{-1}}, \quad (5.3)$$

The output of the integrating-counter is a pulse frequency-modulated signal which is asynchronous with respect to the sampling time, T_s . We can again draw a comparison to the first-order FIR modulator where the output of the VCO was a frequency modulated signal representing the modulating signal at the input of the oscillator. Here, the input signal is $\lfloor \epsilon_{Fs} \rfloor$, and the output of the integrating counter is the new pulse frequency-modulated signal. To synchronize the pulse frequency-modulated carry signal with the sampling clock frequency, F_s , it needs to be time-domain quantized before it can be demodulated. In the previous section this was done with a novel resetting D-FF or resetting counter. As before, this time-quantization will introduce a new error, defined as ϵ_{Fs2}

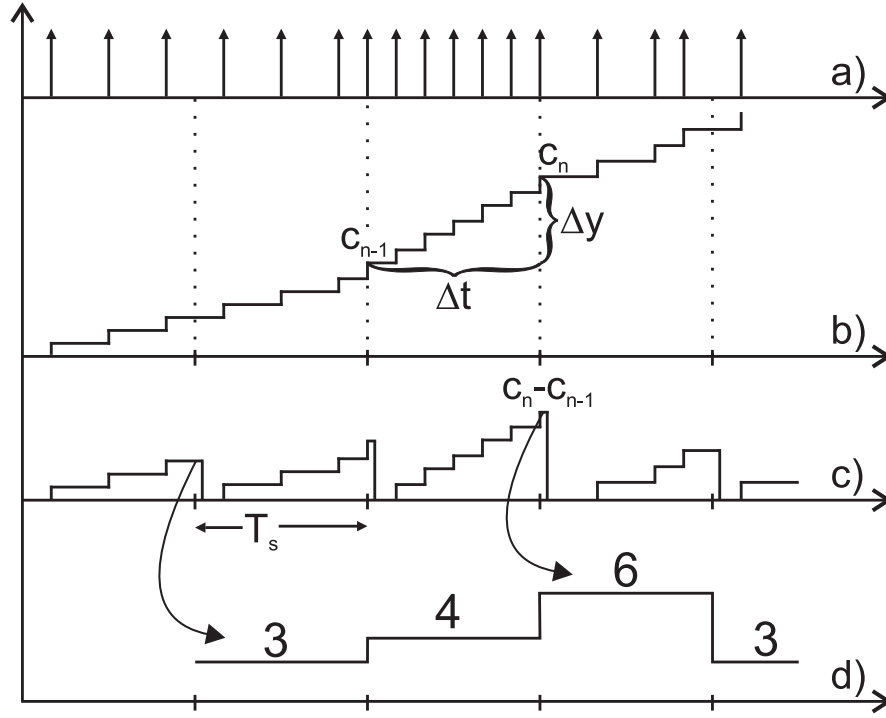


Figure 5.5: a) Carry signal at instances of τ_n as determined by the integrating counter. b) Count signal of the quantizing-counter counting the carry pulses. c) To find the change in the count-value the counter is reset at rate T_s . This makes $c_{n-1} = 0$ and gives the change of the count value as c_n . Furthermore, it guarantees that the differentiating counter will not saturate. d) Quantized output signal $y(n)_2$

here. To time-domain quantize and also shape the introduced quantization error, ϵ_{Fs2} , a second counter is utilized as shown in figure 5.3. This *quantizing-counter* performs time-quantization along with first-order noise shaping of the introduced quantization noise, ϵ_{Fs2} . This can be explained with the help of figure 5.5. Part a) of the figure shows the time-instances of an exemplary carry signal produced by the integrating-counter. These time-instances are being counted by the quantizing-counter as depicted in figure 5.5 b). Discrete-time differentiation with respect to figure 5.5 is defined as:

$$\frac{d}{dt} = \frac{\Delta y}{\Delta t} = \frac{c(n) - c(n-1)}{T_s}, \quad (5.4)$$

where T_s is the simulation's discrete step size, or sampling clock. As a result the transfer function of the resetting quantizing-counter is given as:

$$\frac{y(z)}{c(z)} = \frac{(1 - z^{-1})}{T_s}. \quad (5.5)$$

To find the difference of $c_n - c_{n-1}$ as expressed in equations 5.4 and 5.5, the counter is simply reset at the end of each sampling instance T_s . This is shown in part c) of figure 5.5 which also shows that total change in the counter value, $c_n - c_{n-1}$, is simplify given by c_n owing to the resetting operation. The final output, $y(n)_2$ is the quantized value, just before the resetting as depicted in part d) of figure 5.5. As a result, the quantizing-counter acts as a time-quantizer and differentiator at the same time. Subsequently, the signal transfer function of the second path is given by the product of the discrete integrator and differentiator:

$$\begin{aligned} STF &= \frac{NT_{se}}{1 - z^{-1}} \frac{1 - z^{-1}}{T_s} \\ &= \frac{NT_{se}}{T_s} \end{aligned} \quad (5.6)$$

Hence, it is desired to have the count-value of the integrating counter be the ratio of the elevated clock frequency, F_{se} , to the sampling clock, F_s . Then with $N = F_{se}/F_s$ the STF will be unity. Assuming this N-value of the integrating-counter we can now write the outputs of each first-order modulator, $y(n)_1$ and $y(n)_2$. The output of the first FIR SDM with respect to figure 5.3 is given as:

$$y(z)_1 = \frac{K_{vco}}{F_s} x(t) + (1 - z^{-1}) \epsilon_{Fs} \quad (5.7)$$

The output of the second FIR SDM is given as:

$$\begin{aligned} y(z)_2 &= \left[\frac{\lfloor \epsilon_{Fs} \rfloor}{1 - z^{-1}} + \epsilon_{Fs2} \right] \\ &= \left[\frac{\epsilon_{Fs} - \epsilon_{Fse}}{1 - z^{-1}} + \epsilon_{Fs2} \right] (1 - z^{-1})^2 \end{aligned} \quad (5.8)$$

When the two signals of equation 5.7 and equation 5.8 are subtracted and assuming $NF_s = F_{se}$, one can see that the quantization error ϵ_{Fs} cancels out and only the input signal along with the quantization errors ϵ_{Fse} and ϵ_{Fs2} remain:

$$y_{out}(z) = \frac{K_{vco}}{F_s} x(t) + (1 - z^{-1}) \epsilon_{Fse} + (1 - z^{-1})^2 \epsilon_{Fs2}. \quad (5.9)$$

The error ϵ_{Fse} is determined by the elevated counter clock, F_{se} , as expressed by equation 5.2. Using a finite clock F_{se} to quantize the widths of ϵ_{Fs} introduces the same error as when sampling the input signal at rate F_{se} . As outlined in section 3.4 the

introduced error will be in the range of $[0..T_{se}]$, or $[0..1]$ since the error is in multiples of T_{se} . Assuming no correlation and zero-mean the normalized mean square value is given as:

$$V_{\epsilon_{rms}}^2 = \sigma_{\epsilon}^2 = \int_{-\frac{T_{se}}{2}}^{\frac{T_{se}}{2}} \epsilon^2 P(\epsilon) d\epsilon = \frac{T_s}{T_{se}} \int_{-\frac{T_{se}}{2}}^{\frac{T_{se}}{2}} \epsilon^2 d\epsilon = \frac{F_s^2}{F_{se}^2} \frac{1}{12} = \frac{F_s^2 q^2}{12}. \quad (5.10)$$

The variable q was used in the last equation to show the similarity to conventional delta-sigma converters, where q is often used to represent the quantization step size. Thus, when doubling F_{se} we expect to reduce the noise floor of ϵ_{Fse} by 6dB as q will be halved. As expressed in equation 5.9 the error ϵ_{Fse} is attenuated by a first-order differentiator, $1 - z^{-1}$. Hence, the noise power for ϵ_{Fse} is given as:

$$P_e = \int_{-f_{bw}}^{f_{bw}} S^2(f) |NTF(z)|^2 df = \int_{-f_{bw}}^{f_{bw}} \frac{q^2 F_s^2}{12 F_s} |NTF(z)|^2 df \quad (5.11)$$

Making the assumption that $\sin(\pi f/F_s)$ is approximately $(\pi f/F_s)$, we obtain:

$$\begin{aligned} P_e &\approx \int_{-f_{bw}}^{f_{bw}} \frac{q^2 F_s}{12} \left[2 \left(\frac{\pi f}{F_s} \right) \right]^2 df \\ &= 10 \log \left(\frac{2 \pi^2 f_{bw}^3}{9 F_{se}^2 F_s} \right). \end{aligned} \quad (5.12)$$

As simulation results will later confirm, when doubling the frequency F_{se} while keeping F_s constant, the SNR will improve by 6dB. When doubling the sampling frequency, F_s , the noise floor of ϵ_{Fse} is attenuated by 3dB. Having addressed the error ϵ_{Fse} , the error ϵ_{Fs2} , which is due to the synchronization of the output of the integrating-counter with respect to the sampling frequency F_s , is considered next. Again, assuming no correlation and zero-mean, its normalized variance is given by:

$$V_{\epsilon_{rms}}^2 = \sigma_{\epsilon}^2 = \int_{-\frac{1}{2}}^{\frac{1}{2}} \epsilon^2 P(\epsilon) d\epsilon = \int_{-\frac{1}{2}}^{\frac{1}{2}} \epsilon^2 d\epsilon = \frac{1}{12}. \quad (5.13)$$

As expressed in equation 5.9 this error is attenuated by a second-order differentiator, $(1 - z^{-1})^2$. The noise power for ϵ_{Fs2} is thus given as:

$$P_e = \int_{-f_{bw}}^{f_{bw}} S^2(f) |NTF(z)|^2 df = \int_{-f_{bw}}^{f_{bw}} \frac{1}{12 F_s} |NTF(z)|^2 df \quad (5.14)$$

In equation 5.14 the $1/F_s$ term is due to oversampling as the total introduced noise power is spread out over more samples at higher sampling frequencies, F_s . Making the

assumption that $\sin(\pi f/F_s)$ is approximately $(\pi f/F_s)$, we obtain:

$$\begin{aligned} P_e &\approx \int_{-f_{bw}}^{f_{bw}} \frac{1}{12F_s} \left[2 \left(\frac{\pi f}{F_s} \right) \right]^4 df \\ &= 10 \log \left(\frac{8}{15} \frac{\pi^4 f_{bw}^5}{F_s^5} \right). \end{aligned} \quad (5.15)$$

Equation 5.15 tells us that the error ϵ_{Fs2} is attenuated by 15dB when doubling the sampling frequency, F_s . The total noise of the overall second order FIR modulator is then the sum of the two errors ϵ_{Fse} which is due to the finite clock F_{se} and ϵ_{Fs2} which is due to synchronization with respect to F_s . Hence, the SNR is given as:

$$SNR = 20 \log 10 \left[\frac{2|A_{in}|\Delta f}{F_s} \right] - 10 \log \left(\underbrace{\frac{2}{9} \frac{q^2 \pi^2 f_{bw}^3}{F_{se}^2 F_s}}_{\epsilon_{Fse}} + \underbrace{\frac{8}{15} \frac{\pi^4 f_{bw}^5}{F_s^5}}_{\epsilon_{Fs2}} \right). \quad (5.16)$$

It is easy to see that the dominant error in equation 5.16 is ϵ_{Fse} . Hence, the SNR is determined by ϵ_{Fse} and can be simplified to:

$$SNR \approx 20 \log 10 \left[\frac{2|A_{in}|\Delta f}{F_s} \right] - 10 \log \left(\frac{2}{9} \frac{\pi^2 f_{bw}^3}{F_{se}^2 F_s} \right). \quad (5.17)$$

5.2.2 Simulation Results

To verify the results derived in the previous section, mainly equation 5.16, the second-order FIR modulator from figure 5.3 was simulated. For this a VerilogA/AMS model was written which is included in Appendix A.2. Three different simulation were performed to verify equation 5.16.

- **Utilizing an ideal integrator while changing the frequency of the sampling D-FF, F_s :**

In a first run, the integrating-counter was replaced with an ideal integrator to observe the effects of changing the sampling frequency F_s with which the frequency modulated signal at the output of the VCO is being sampled. An ideal integrator was used because the error ϵ_{Fse} will dominate the noise floor and hence make it difficult to observe how changing circuit parameters will effect the error ϵ_{Fs2} . With an ideal integrator, on the other hand, the error ϵ_{Fse} in equation 5.16 is not present and only ϵ_{Fs2} remains. Hence, for doubling the sampling frequency, F_s ,

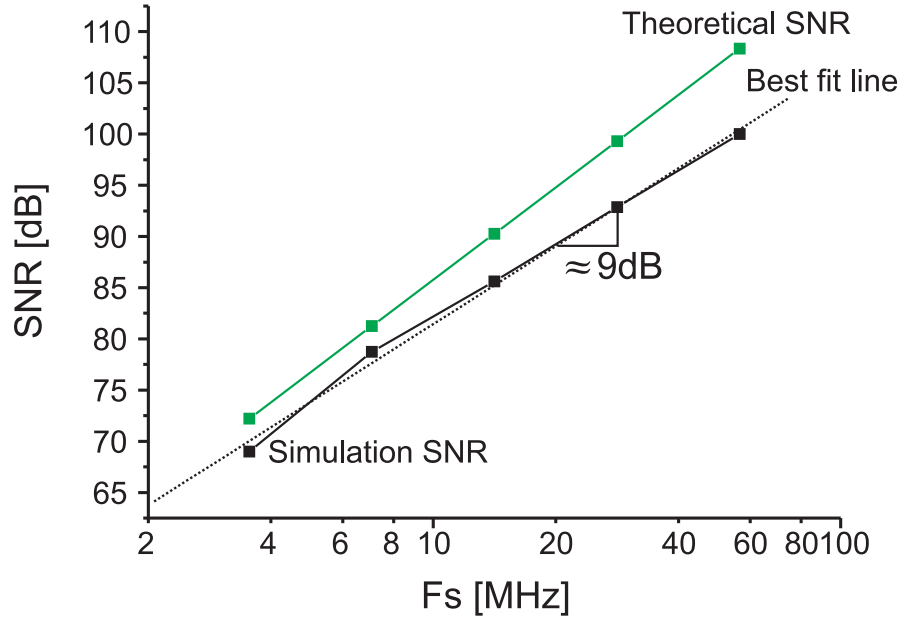


Figure 5.6: Simulation results of the FIR modulator from Figure 5.3. The figure shows the obtained SNR for different sampling frequencies, F_s . The integrating-counter is assumed to be ideal in this simulation, hence no error $\epsilon_{F_{se}}$. Two plots are given. The first plot, indicates the theoretical SNR. The second plot shows the simulation results obtained including a best-fit line to show the expected slope of 9dB for doubling F_s , as expressed in equation 5.16. Circuit/Acquisition Details: $K_{vco}=0.25\text{MHz}$, $f_{bw}=20\text{kHz}$, $F_c=1.07241\text{MHz}$, $f_{in}=8.4\text{kHz}$.

we expect a 9dB increase in SNR. That is, 15dB are gained due to the attenuation of the noise floor and 6dB are lost due to the scaling of the output amplitude. The results of the simulation are given in Figure 5.6. The figure shows the dependency of the SNR on changing the sampling frequency, F_s . With increasing sampling frequency, F_s , the quantization error $\epsilon_{F_{s2}}$ will be attenuated further, resulting in more SNR. Also shown is a best-fit line indicating the average slope, which is 9dB for doubling F_s . To verify the simulation results to the theoretical SNR predictions from equation 5.16 a plot representing the theoretical SNR is depicted also. As can be seen there is a small offset but otherwise the simulation follows the theory.

- **Utilizing a real integrating-counter while changing F_{se} which determines the resolution of the counter:**

Having investigated the dependency of the sampling frequency F_s on $\epsilon_{F_{s2}}$, a non-ideal integrating counter with a finite clock frequency F_{se} was used next. Now,

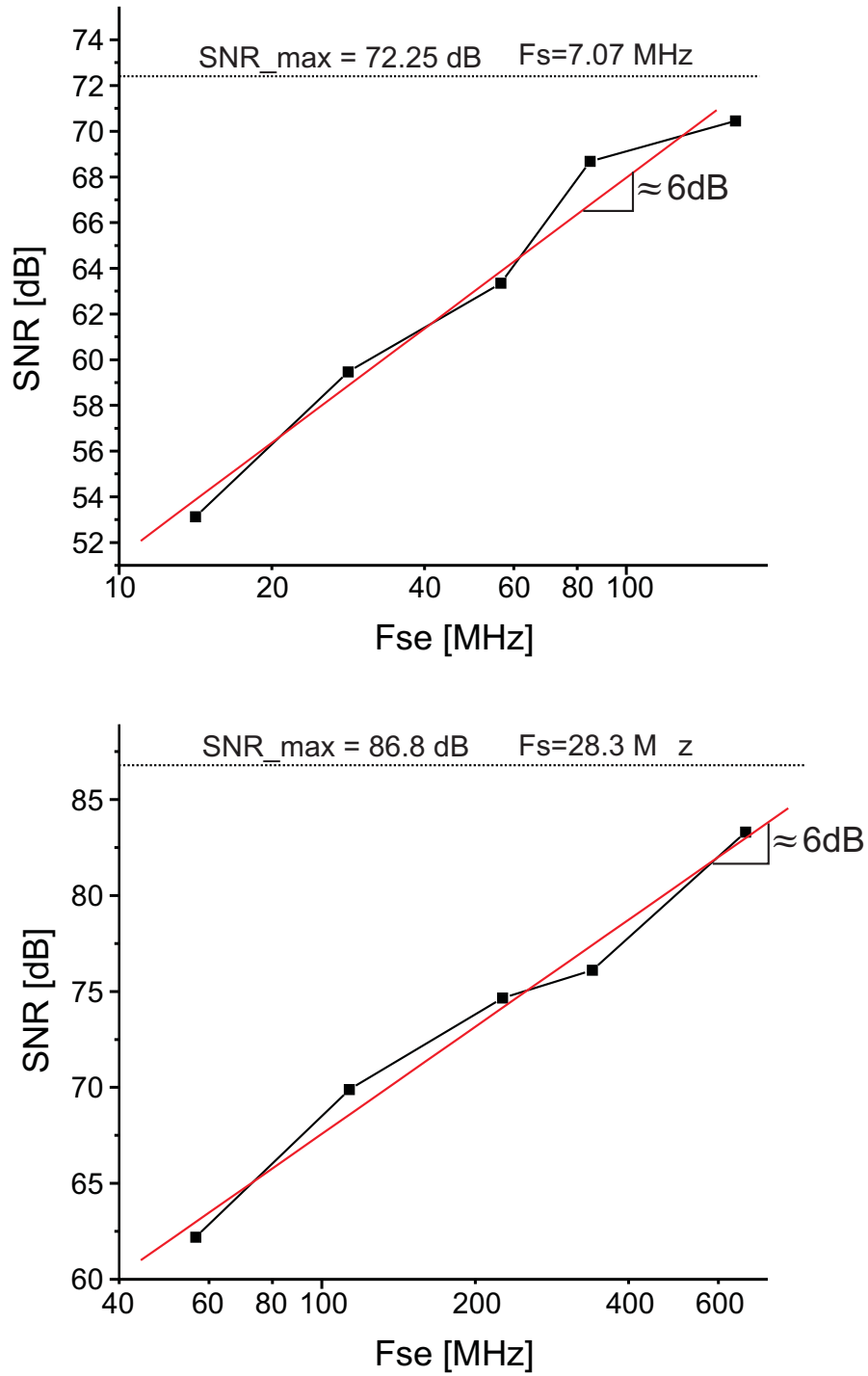


Figure 5.7: Part a) depicts the SNR results for a sampling frequency of $F_s = 7.07$ MHz while increasing the frequency of the integrating-counter, F_{se} . Part b) depicts a similar result for a sampling frequency of $F_s = 28.3$ MHz. Note that for very high frequencies of F_{se} the SNR approaches the values from Figure 5.6. This is indicated by SNR_{max} . The best-fit lines are also shown to confirm the expected increase in SNR of 6dB for doubling F_s , as expressed in equation 5.16. Circuit/Acquisition Details: $F_s = \sqrt{2} \times 5$ MHz and $F_s = \sqrt{2} \times 20$ MHz, $K_{vco} = 0.25$ MHz, $f_{bw} = 20$ kHz, $F_c = 1.07241$ MHz, $f_{in} = 8.4$ kHz.

the error $\epsilon_{F_{se}}$ should dominate the noise floor. With this setup we can observe the effects of changing the clock frequency F_{se} which determines the accuracy of the integrating-counter. At the same time, the sampling frequency F_s is kept constant. When the integrating-counter with its finite clock frequency F_{se} is used, as shown in Figure 5.3, the dominant error $\epsilon_{F_{se}}$ will be added to the error $\epsilon_{F_{s2}}$ and the SNR shown in Figure 5.6 cannot be obtained. This maximum SNR can only be approximated by choosing very high sampling frequencies of F_{se} . From equation 5.12 we expect to increase the SNR by a factor of 6dB per doubling F_{se} . This is depicted for two constant sampling frequencies, F_s , in part a) and b), of figure 5.7, respectively. In part a) the highest SNR with no error $\epsilon_{F_{se}}$ present is 72.25dB, as determined from Figure 5.6. With increasing clock frequency F_{se} this SNR value is approached, but never reached. The same applies for a second sampling frequency, shown in part b) of figure 5.7. The highest SNR value achievable would be 86.8dB. Again, the slope is also depicted to show the expected 20dB per decade slope.

- **Utilizing a real integrating-counter and changing F_{se} and F_s :**

In a final simulation both, the sampling frequency F_s and the frequency of the integrating-counter F_{se} were changed simultaneously. That is, when F_s is increased by a factor of two, F_{se} is increased also by a factor of two. When F_{se} is doubled, the error $\epsilon_{F_{se}}$ will be halved and thus 6dB are gained. Since F_s is doubled also we obtain 6dB more attenuation; however, loose 6dB as the output amplitude will be reduced. Hence, we would expect a total of 6dB increase in SNR. The simulation results depicting the SNR are given in figure 5.8. The figure confirms that for doubling F_s and F_{se} a total of 6dB are gained. Note that even though the error $\epsilon_{F_{s2}}$ is attenuated by 9dB per doubling F_s , the error $\epsilon_{F_{se}}$ dominates the noise floor and we obtain 6dB in total.

In summary, when the sampling frequency F_s is doubled and F_{se} remains constant no SNR improvement is obtained. When both, F_s and F_{se} are doubled, a 6dB improvement is achieved. When F_s remains constant and F_{se} is doubled, a 6dB SNR improvement

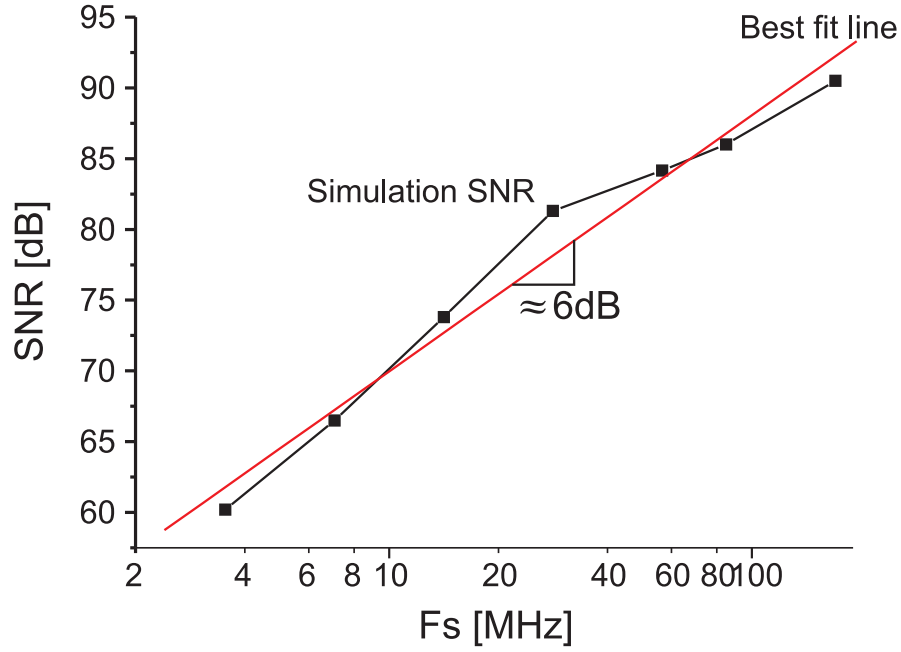


Figure 5.8: Simulation results of the FIR modulator from Figure 5.3. The figure shows the obtained SNR for different sampling frequencies, F_s and $F_{se} = 10F_s$. The dominant error is $\epsilon_{F_{se}}$ and hence a 6dB slope is observed. Circuit/Acquisition Details: $K_{vco}=0.25\text{MHz}$, $f_{bw}=20\text{kHz}$, $F_c=1.07241\text{MHz}$, $f_{in}=8.4\text{kHz}$.

occurs. In all cases the maximum gain in performance is limited to 6dB as the error $\epsilon_{F_{se}}$ which due to F_{se} of the integrating counter dominates the noise floor. As a consequence, the topology could be simplified by ridding it of the quantizing-counter from figure 5.3. This is because $\epsilon_{F_{s2}}$ does not determine the overall SNR and is hence insignificant. In turn, since the quantizing-counter is responsible also for noise-shaping an equivalent would have to be found as the overall topology needs second-order noise-shaping. The next section describes a way to achieve this. A second topology is proposed with simplified circuitry while still giving the same performance than the aforementioned circuit. Furthermore this simplified topology can easily be modified to include undersampling as described below.

5.2.3 Version II

Figure 5.9 shows this simplified 2nd order modulator. As can be seen, it now comprises out of a 1st order FIR modulator in the upper path which again introduces a quantization error, ϵ_1 , when sampling the frequency modulated signal with the D-FF. This quantization error, ϵ_1 , is determined and quantized in the second path to be subtracted from the

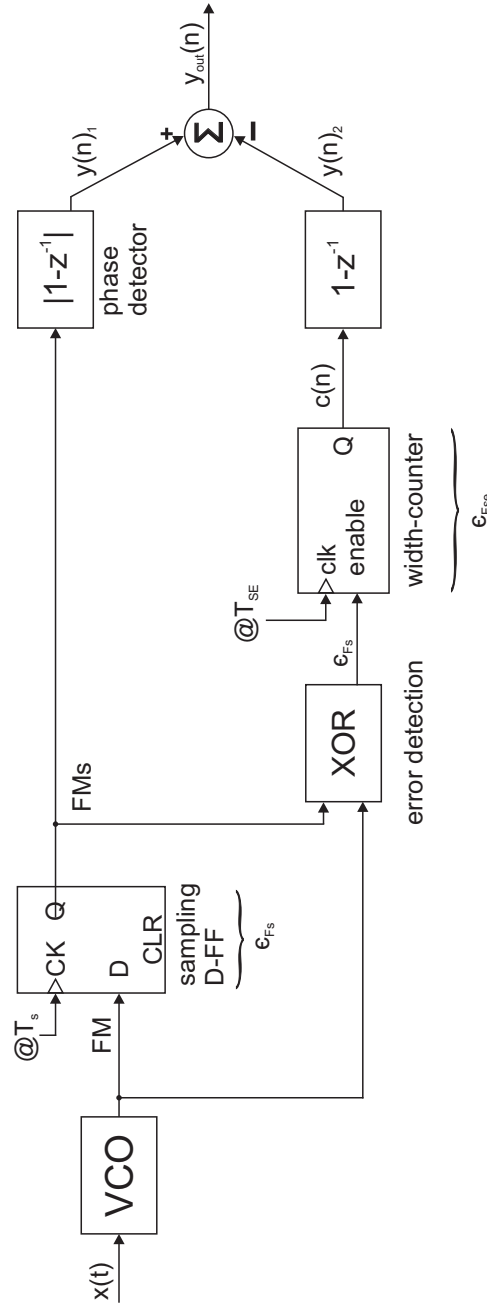


Figure 5.9: Second-order cascaded FIR modulators. Shown is the modulator consisting of a 1st order modulator in the upper path and an all-digital implementation of the second path is used to quantize to cancel out the quantization error introduced in the upper FIR modulator. The quantization error introduced in the first stage, ϵ_1 , is quantized by the width-counter in multiples of T_{se} . At the same time first-order noise shaping on the new error, ϵ_2 , is performed. The estimate determined by the width-counter, $c(n)$, is then representative of the quantization error ϵ_1 and can be used to eliminate ϵ_1 by combining the two signals, $y(n)_1$ and $y(n)_2$.

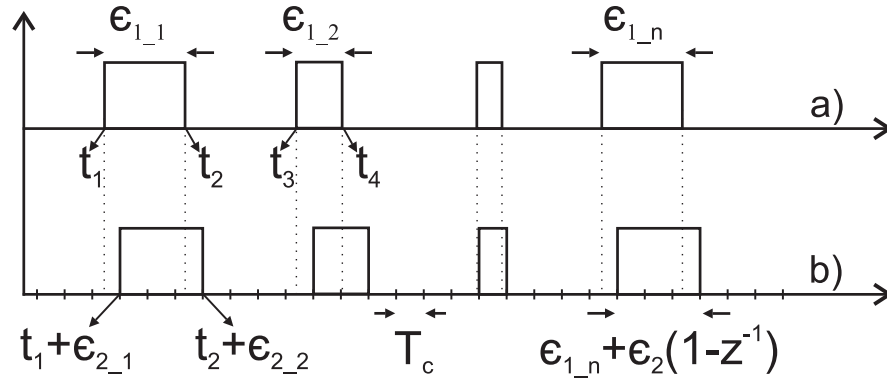


Figure 5.10: Part a) shows a asynchronous signal. Part b) depicts the sampled version, now synchronized with respect to the clock. As shown, the introduced time quantization error will be noise shaped by $1 - z^{-1}$ if the pulse widths are considered.

first stage, thus resulting in improved performance. Since the introduced quantization error as depicted in Figures 5.1 and 5.2 is in the time-domain, a circuit capable of determining the widths of each error pulse could be utilized to quantize this error. Thus, we can replace the *integrating-counter* with a *width-counter*. This is an elegant solution as will become apparent shortly. The quantization error, ϵ_1 , is found first by an XOR gate as explained in section 5. Again, this assumes that the sampling frequency F_s is higher than the frequency at the output of the VCO. This error is then quantized and noise-shaped out of the band of interest by the *same* width-counter, operating at an elevated frequency F_{se} . The heuristics behind this novel assertion are explained with the help of figure 5.10. When sampling the error pulse train signal, ϵ_{1_n} , shown in figure 5.10 a), each rising or falling edge will experience a new time error, ϵ_{2_n} . Shown in figure 5.10 b) is the sampled version of the signal in part a). As can be seen, each positive or negative edge has a new time error ϵ_{2_n} , which is anywhere within the region of the sampling period $[0..T_{se}]$. Also depicted in the figure are the exact pulse widths ϵ_{1_n} which are given by the time difference of the negative and positive edge instances. Mathematically, for instance, the first pulse width, ϵ_{1_1} , is given by the time difference of the rising and falling edge of the first pulse, $t_2 - t_1$. The sampled pulse width is then given as $t_2 + \epsilon_{2_2} - t_1 - \epsilon_{2_1} = \epsilon_{1_1} + \epsilon_2(1 - z^{-1})$. As a result, the new timing error, ϵ_2 , is attenuated by a high-pass filter and thus shaped out of the band of interest, if a width counter is used. Conceptually, whenever the accumulated quantization error exceeds

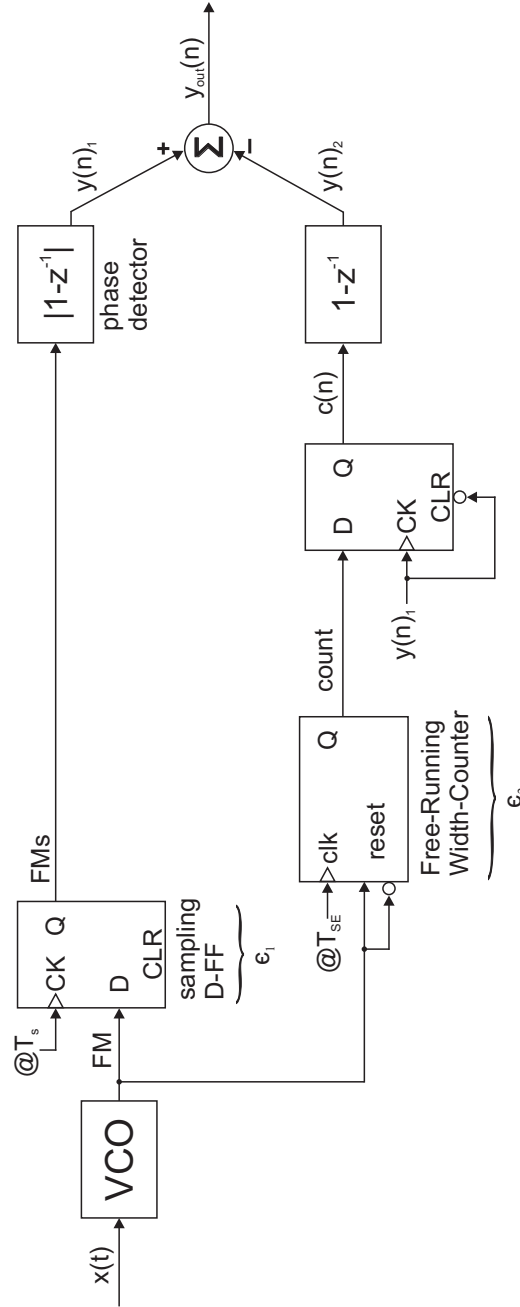


Figure 5.11: Second-order cascaded FIR modulator suitable for undersampling. An all digital second path is utilized to cancel out the quantization error introduced in the upper FIR modulator. The quantization error introduced in the first stage, ϵ_1 , is quantized by the width-counter as multiples of T_{se} . The counter is reset at every positive or negative FM edge. When FM_s switches, the count value is read out by a D-FF. This value is reset to zero when y_1 goes low. The estimate determined by the width-counter, $c(n)$, is then representative of the quantization error ϵ_1 and can be used to eliminate ϵ_1 by combining the two signals, $y(n)_1$ and $y(n)_2$.

a width of T_{se} , the width of the synchronized cycle period is shortened by a length of T_{se} to reflect this error. Thus, the error experiences first-order noise shaping. It might be noted that this elegant principle is identical to amplitude quantization with negative feedback applied. Subsequently, the XOR-gate and the width-counter in Figure 5.9 quantize the error, ϵ_{1_n} , and also noise-shape the quantization error ϵ_{2_n} . In turn, no negative feedback is needed and the overall complexity of the circuit is kept to a minimum. So far it was assumed that the sampling frequency, F_s , is higher than the frequency of the VCO. However, when the VCO frequency, F_{vco} , is much higher than the sampling frequency, F_s , the XOR gate cannot be used to determine the error pulses. This was already indicated in section 5. Instead the topology depicted in figure 5.11 can be used. The topology from figure 5.11 is a modification of the version from figure 5.9 to allow for undersampling. Figure 5.12 gives insight into the general operation of the just introduced topology from Figure 5.9 and also explains how to use sampling frequencies lower than the VCO output for which figure 5.11 is an example. The frequency modulated signal at the output of the VCO is shown in part a) of figure 5.12, and the sampled version in part b). The timing error when sampling the *FM* signal is depicted in figure 5.12 c) by the shaded pulses. Note that the timing error is the time difference from the last rising or falling edge of the *FM* signal to the sampled signal, FM_s . Also note that there is only one timing error per FM_s edge. A counter which counts the width of each *FM* signal pulse can be utilized to provide a quantized value of the error pulses. In order to do so, the counter is simply a free running counter which is simply reset at each positive or negative *FM* edge. This is shown in part d) of figure 5.12. The counter counts up at the elevated frequency, F_{se} . With respect to figure 5.12 c) we see that there is only one error pulse per sampled *FM* edge. Also note that the demodulated output, $y(n)_1$ provides a means to read out the count value since $y(n)_1$ goes high only for each positive or negative *FM* edge. This can be seen when observing parts b) and f) of figure 5.12. Subsequently, the count value can be read out at each positive $y(n)_1$ edge. This value is then held to furnish the following circuitry and then cleared with the negative edge of $y(n)_1$. Subsequently, since the count value is a representative of the quantization error

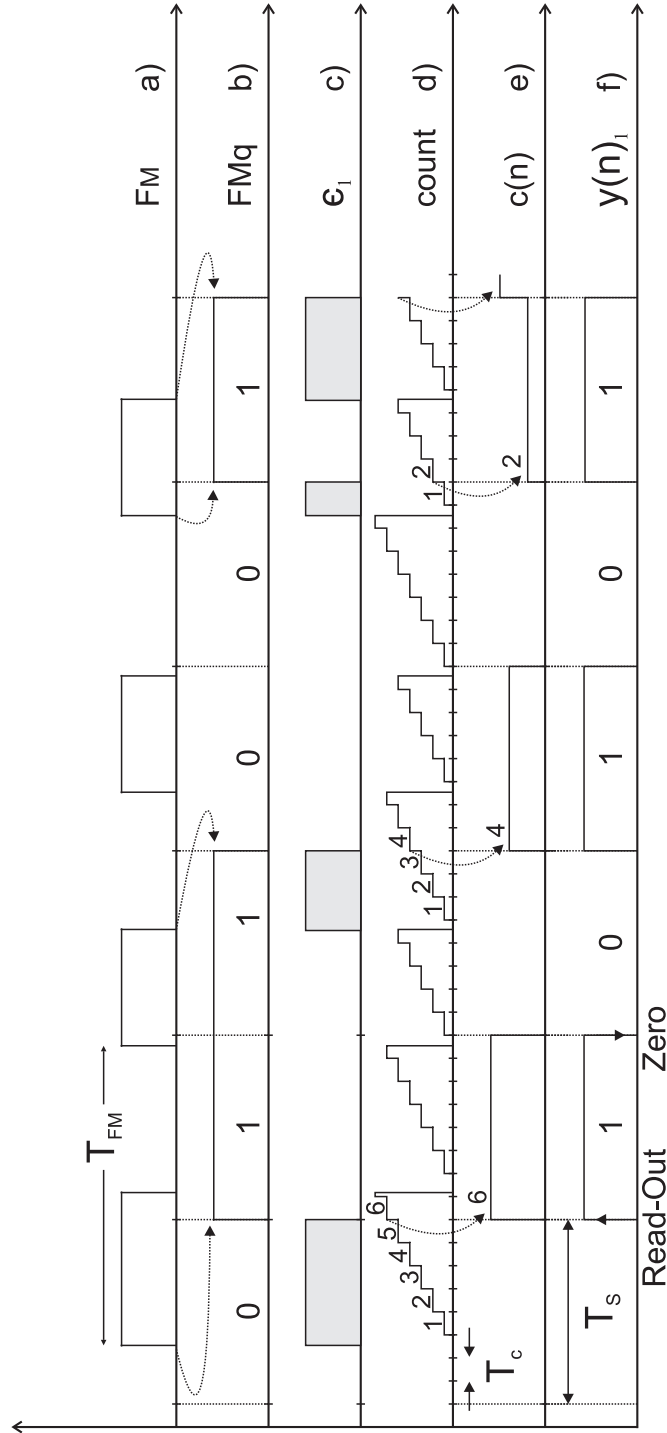


Figure 5.12: Part a) shows the asynchronous FM signal. Part b) is the under-sampled version of that signal, FMq . Part c) depicts the timing error introduced, which is the time from the last rising or falling FM edge to the rising or falling FMq edge. Part d) shows the count signal of the width-counter. The counter is enabled with every positive going FM-edge and reset with every negative going FM-edge. The counter furnishes a D-FF responsible for reading out the count value and holding it till the reset. The D-FF reads out at each positive edge of $y(n)_1$ and resets this value some there thereafter, e.g. with the negative edge of $y(n)_1$. The read-out count value is shown in part e) and the signal $y(n)_1$ in part f).

ϵ_1 introduced in the upper path, it can be differentiated and then combined with the output of the upper path to cancel the quantization error ϵ_1 . It is important to note that the topology depicted in figure 5.11 can be used with undersampling the FM signal or using a sampling frequency that is much higher than the oscillation frequency of the VCO. However, when undersampling we need to make sure that we choose the sampling frequency F_s such that the entire band of the bandpass signal is translated down without crossing any integer multiples of $F_s/2$. Otherwise aliasing or spectral reversal of the signal might occur. The topology from figure 5.11 not only reduces the circuitry when compared to the first version shown in figure 5.3 but also is suitable for undersampling making it a much more versatile topology.

5.2.4 Theoretical Performance

Mathematically, the output of the upper path is given as:

$$y(z)_1 = \frac{K_{vco}}{F_s} x(t) + (1 - z^{-1}) \epsilon_1, \quad (5.18)$$

where the attenuation of the error is done at rate F_s . The pulse widths of the error signal are quantized by the width counter as an integer multiple of T_{se} . As a result the output, $c[n]$, of the counter is given by:

$$\begin{aligned} c(n) &= Q \left[\frac{\tau_\epsilon(n)}{T_{se}} \right] = \left\lfloor \frac{\tau_\epsilon(n)}{T_{se}} \right\rfloor + \left\langle \frac{\tau_\epsilon(n)}{T_{se}} \right\rangle (1 - z^{-1}) \\ &= \epsilon_1 + \epsilon_{Fse} (1 - z^{-1}). \end{aligned} \quad (5.19)$$

In equation 5.19 the $\lfloor \cdot \rfloor$ operator expresses the floor operator and $\langle \cdot \rangle$ the fractional part. The introduced error, ϵ_{Fse} , which is the subtraction of the two errors at each rising and falling edge of ϵ_1 , has a triangular probability distribution. This error is thus being noise shaped by $(1 - z^{-1})$. Thus, the output $y(z)_2$ is given by:

$$y(z)_2 = \left[\epsilon_1 + \epsilon_{Fse} (1 - z^{-1}) \right] (1 - z^{-1}), \quad (5.20)$$

and the overall output as:

$$\begin{aligned} y_{out}(z) &= y(z)_1 - y(z)_2 \\ &= \frac{K_{vco}}{F_s} x(t) + (1 - z^{-1}) (1 - z^{-1}) \epsilon_{Fse}. \end{aligned} \quad (5.21)$$

Thus, in the ideal case the quantization error ϵ_1 is cancelled, and only a scaled version of the input remains along with a second order noise shaped quantization error, $\epsilon_{F_{se}}$. The overall performance of the cascade, more specifically, the cancellation of the quantization error, ϵ_1 , is determined by the clock frequency F_{se} at which the width-counter operates. Also, further attenuation can be achieved when increasing the sampling frequency F_s . Thus, we may distinguish between the two cases:

- **Changing the frequency of the free-running counter, F_{se} :**

Intuitively, the faster the clock F_{se} , the less error is introduced when sampling the error signal, ϵ_1 . This is essentially the same principle as in the case of the first-order modulator where the FM signal was sampled by F_s . Since sampling is done at the elevated clock frequency, F_{se} , it can be seen as an equivalent to multi-bit amplitude quantization in conventional delta-sigma converters. Reducing the quantization step size by a factor of two would then decrease the noise floor by 6dB. This will be confirmed with simulation results shortly. Since the sampling frequency F_s remains unchanged an overall SNR increase of 6dB is expected.

- **Keeping F_{se} constant and changing the sampling frequency of the D-FF, F_s :**

The error from the first modulator, ϵ_1 , is fed into the second stage, sampled, and its width is determined by the width-counter. This width includes the original error ϵ_1 plus the new error $\epsilon_{F_{se}}$ due to the sampling process. Note that this width value is now in the amplitude domain and is also normalized with respect to F_s . Even though the error $\epsilon_{F_{se}}$ is constant as F_{se} is constant, its height doubles when F_s is doubled as it is also normalized with respect to F_s . This will result in an increase of 6dB in the noise floor of the error $\epsilon_{F_{se}}$. On the other hand, due to the second order differentiation the noise floor of $\epsilon_{F_{se}}$ is expected to be attenuated by a total of 12dB for doubling F_s . As a consequence, chaining F_s will have no effect as the net SNR remains constant. This is because 6dB dynamic range are lost as the signal output amplitudes will be reduced by a further 6dB for doubling F_s . Simulation results in the next section confirm this intuitive result.

- **Changing F_{se} and F_s simultaneously:**

Having considered the two previous cases it is clear that doubling F_s as well as F_{se} will result in 6dB increase in SNR

As mentioned, the error ϵ_{Fse} is anywhere in the range of $0..T_{se}$ or $0..1$ in terms of T_{se} . For simplicity the error is assumed to be random with zero mean. The latter assumption is easily justified as any dc-shift is simply a change in the center frequency of the VCO. Then its normalized variance with respect to F_s is given by:

$$V_{\epsilon_{rms}}^2 = \sigma_{\epsilon}^2 = \int_{-\frac{T_{se}}{2T_s}}^{\frac{T_{se}}{2T_s}} \epsilon^2 P(\epsilon) d\epsilon = \frac{T_s}{T_{se}} \int_{-\frac{T_{se}}{2T_s}}^{\frac{T_{se}}{2T_s}} \epsilon^2 d\epsilon = \frac{1}{12} \frac{F_s^2}{F_{se}^2}. \quad (5.22)$$

The width counter will express the time-domain quantized error widths as a count value and also provide noise shaping. With the overall second order noise shaping, the noise within the bandwidth of interest, f_{bw} , is given as:

$$P_e = \int_{-f_{bw}}^{f_{bw}} S^2(f) |NTF(z)|^2 df = \int_{-f_{bw}}^{f_{bw}} \frac{1}{12} \frac{1}{F_s} \frac{F_s^2}{F_{se}^2} |NTF(z)|^2 df \quad (5.23)$$

Making the assumption that $\sin(\pi f/F_s)$ is approximately $(\pi f/F_s)$, we obtain:

$$\begin{aligned} P_e &\approx \int_{-f_b}^{f_b} \frac{1}{12} \frac{1}{F_s} \frac{F_s^2}{F_{se}^2} \left[2 \left(\frac{\pi f}{F_s} \right) \right]^4 df \\ &= 10 \log \left(\frac{8}{15} \frac{\pi^4 f_{bw}^5}{F_s^3 F_{se}^2} \right). \end{aligned} \quad (5.24)$$

Since the signal output has remained the same, the signal-to-noise ratio is given as:

$$SNR = 20 \log 10 \left[\frac{2|A_{in}|\Delta f}{F_s} \right] - 10 \log 10 \left[\frac{8}{15} \frac{\pi^4 f_{bw}^5}{F_{se}^2 F_s^3} \right], \quad (5.25)$$

Thus, for doubling F_{se} we obtain a 6dB decrease in the noise floor.

5.2.5 Simulation Results

The topology in figures 5.9 and 5.12 was simulated for different clock frequencies, F_{se} , and also different sampling and undersampling frequencies, F_s . Appendix A.3 gives the VerilogA/AMS code used to simulate the second order FIR topology. The signal-to-noise ratio was obtained by importing the output into Matlab and calculating the PSD. The results for the simulation of the topology from 5.9 are given in figures 5.13 and

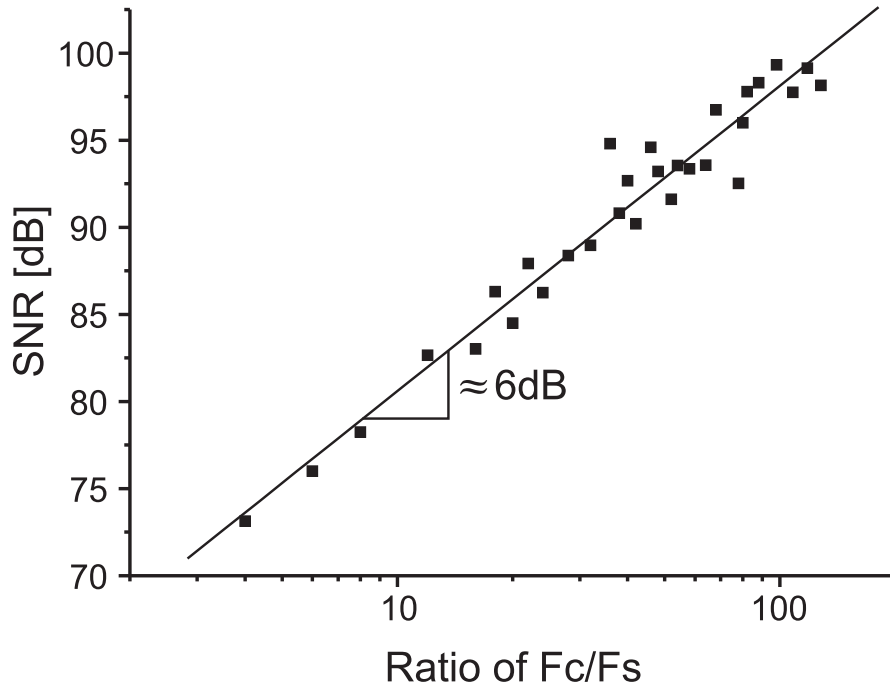


Figure 5.13: SNR plot versus ratio of the elevated clock frequency with which the width-counter is clocked, F_{se} over the sampling frequency $F_s = \text{constant}$. Depicted is the SNR plot for the second order cascade from figure 5.9. As expected, the SNR shows a 20dB per decade characteristic. Circuit/Acquisition Details: $F_s = \sqrt{2} \times 25\text{MHz}$, $K_{vco} = 0.5\text{MHz}$, $f_{bw} = 20\text{kHz}$, $F_c = 4.352\text{MHz}$, $f_{in} = 8.4\text{kHz}$.

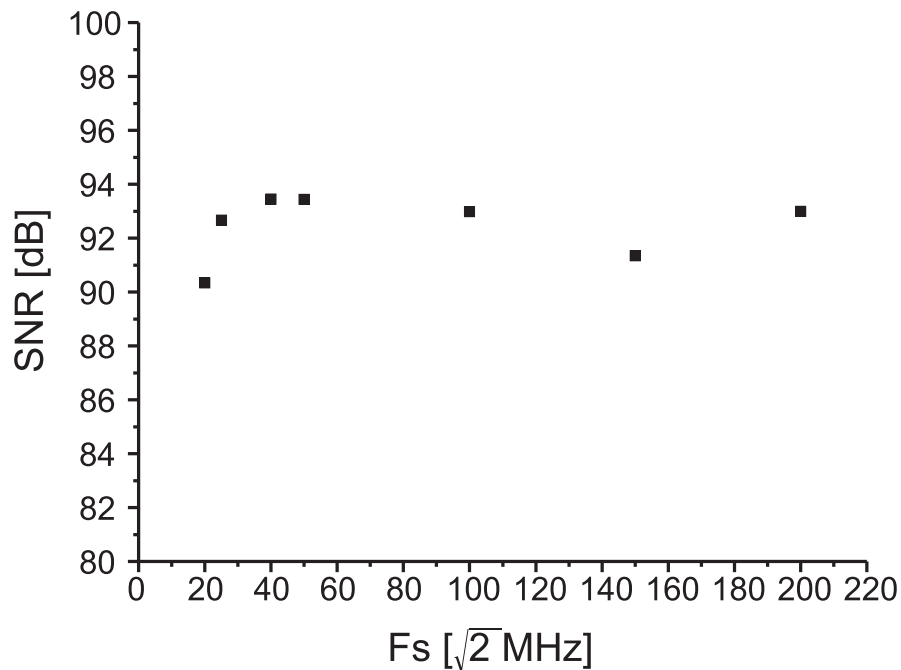


Figure 5.14: SNR plot versus the sampling frequency F_s while keeping F_{se} constant. Depicted is the SNR plot for the second order cascade from figure 5.9. As expected, the SNR shows no improvement. Circuit/Acquisition Details: $F_{se} = \sqrt{2} \times 1\text{GHz}$, $K_{vco} = 0.5\text{MHz}$, $f_{bw} = 20\text{kHz}$, $F_c = 4.352\text{MHz}$, $f_{in} = 8.4\text{kHz}$.

5.14. Figure 5.13 shows the SNR results for keeping the sampling frequency constant while varying the clock frequency of the width-counter, F_{se} . As expected, a 20dB per decade, or, 6dB SNR increase per doubling of F_{se} are achieved. Naturally, with the error still being quite correlated with itself and dependant on the ratio of F_{vco} to F_s as explained in section 3.4, the SNR fluctuates somewhat but on average follows the 20dB per decade slope. Also note that for very low frequencies of F_{se} compared to F_s the width-counter cannot determine an accurate representation of the error ϵ_1 . At these low ratios the 2nd order modulator approaches the result of a 1st order modulator. It was also found that at very high ratios of F_{se} to F_s the SNR levels off which is mainly due to the accuracy of the simulator (Spectre). For example, in VerilogAMS the `@cross` statement used as a trigger for the width-counter, will when the event occurs, temporarily stop the simulator for a very minute amount of time, resulting in a small error. Figure 5.14 shows the obtained SNR when keeping F_{se} constant while changing F_s . As already discussed previously no change in SNR is expected. The results for the simulation of the topology from 5.12 utilizing undersampling frequencies are given in figures

5.3 Comparison To The First-Order Modulator

Having analyzed and discussed the second-order FIR modulators, in this section a comparison is drawn to the first-order FIR modulators from section 3. Specifically, the second-order modulator from figure 5.9 is compared to the first-order modulator from figure 3.6. A direct comparison should show whether there are any benefits to the second-order topology over the simpler first-order modulator.

For a fair comparison, the first-order modulator is clocked at the elevated sampling frequency F_{se} , while the second order modulator utilizes the slow sampling frequency F_s in the upper path, and the elevated sampling frequency F_{se} in the lower path. Figure 5.15 shows the two circuits. Note that most blocks were implemented on transistor level basis using the IBM 130nm Standard Cell Library. The VCO and the counter were implemented as a VerilogA model. Furthermore, it is assumed that both clocks

are derived from the same system clock.

As seen in figure 5.15 the first-order topology shown in part a) has less component count; however, its output rate is $\frac{F_{se}}{F_s}$ higher than the output rate of the second-order topology. As a result, the first-order modulator would require a higher decimation rate to lower the data rate of the oversampled modulator. In addition, the first-order FIR modulator might require output signal amplification as the output amplitude is scaled by a factor of $\frac{K_{vco}}{F_{se}}$ as expressed in equation 3.27. The second-order modulator on the other hand has an output rate which is at the lower frequency F_s . As a result, the decimation filter will be simpler when compared to the first-order FIR modulator.

An important point to recall is that the first-order modulator improves its SNR by approximately 3 dB for doubling the sampling frequency, F_s . This was expressed in equation 3.27. The second order FIR modulator, on the other hand, gains 6dB in SNR for doubling the sampling frequency F_{se} . This was expressed in equation 5.25. Subsequently, one would expect the second-order FIR modulator to outperform the first-order modulator.

Figure 5.16 shows the SNR comparison of the first and second-order FIR modulator for various frequencies, F_s . The first-order modulators sampling frequency was varied from 20MHz to 200MHz. The red graph shows the SNR results obtained. As expected, the slope of the first-order modulator is approximately 3dB. The results of the second order modulator are depicted by the blue line. The second-order modulator was operated at a sampling frequency of 13MHz as depicted in figure 5.15 b). As can be seen the slope of the second-order modulator is higher compared to that of the first-order modulator. At lower frequencies the second-order topology is inferior to the first-order structure. It is believed that this is mainly due to the fact that the width-counter, which is clocked at F_{se} , does not have enough resolution to estimate the error ϵ_1 correctly. Hence, at low frequencies, F_{se} , the with-counter might actually introduce more error than expected. At higher frequencies of F_{se} however, the second-order modulator yields a better signal-to-noise ratio. This is because its SNR increases with a higher slope per doubling F_{se} , and hence the second order modulator outperforms the first-order

topology. Figure 5.17 shows a PSD comparison of the two modulators. As can be seen the output signal amplitude of the first-order modulator is attenuated by approximately -69dB whereas the second-order modulator only attenuates the wanted signal by approximately -48dB. At the same time, due to the second-order noise shaping, the quantization noise is attenuated similar to that of the first-order modulator in the bandwidth of interest resulting in the better SNR. Summarizing, both modulator topologies are useful implementation of delta-sigma A/D converters. In general, the second-order FIR modulator is recommended over the first-order modulator as not only it allows for a simpler decimation filter design, but also outperforms the first-order topology at higher frequencies. In turn, at lower sampling frequencies the first-order topology is beneficial as it has better performance and less component count.

5.4 Discussion and Conclusion

In this chapter two second-order FIR modulators based on oscillators were presented. First, a second order topology was devised utilizing a first-order FIR modulator as described in Chapter 3 and an all digital equivalent utilizing an integrating-counter running on a clock F_{se} to essentially act as a digital voltage-controlled oscillator. The differentiating-counter used realizes time-domain quantization and also noise-shaping of the introduced quantization error ϵ_{Fs2} . The presented topology was analyzed mathematically and equations expressing the three different error sources were given. Furthermore, a signal-to-noise ratio equation was determined. This equation indicated that for doubling the sampling frequency F_s no increase in net SNR is achieved. Also it was shown that increasing the clocking frequency of the counter, F_{se} , would result in an SNR increase of 6dB. These theoretical results were then verified by simulating the aforementioned topology. Various parameters were changed to successfully verify the obtained equations. Since the maximum obtainable SNR increase was limited to 6dB, the topology was in a second circuit variation simplified while still retaining all the characteristics. That is, a novel scheme was proposed which not only gives a digital representation of the quantization error from the first stage, ϵ_1 , but also noise-shapes the

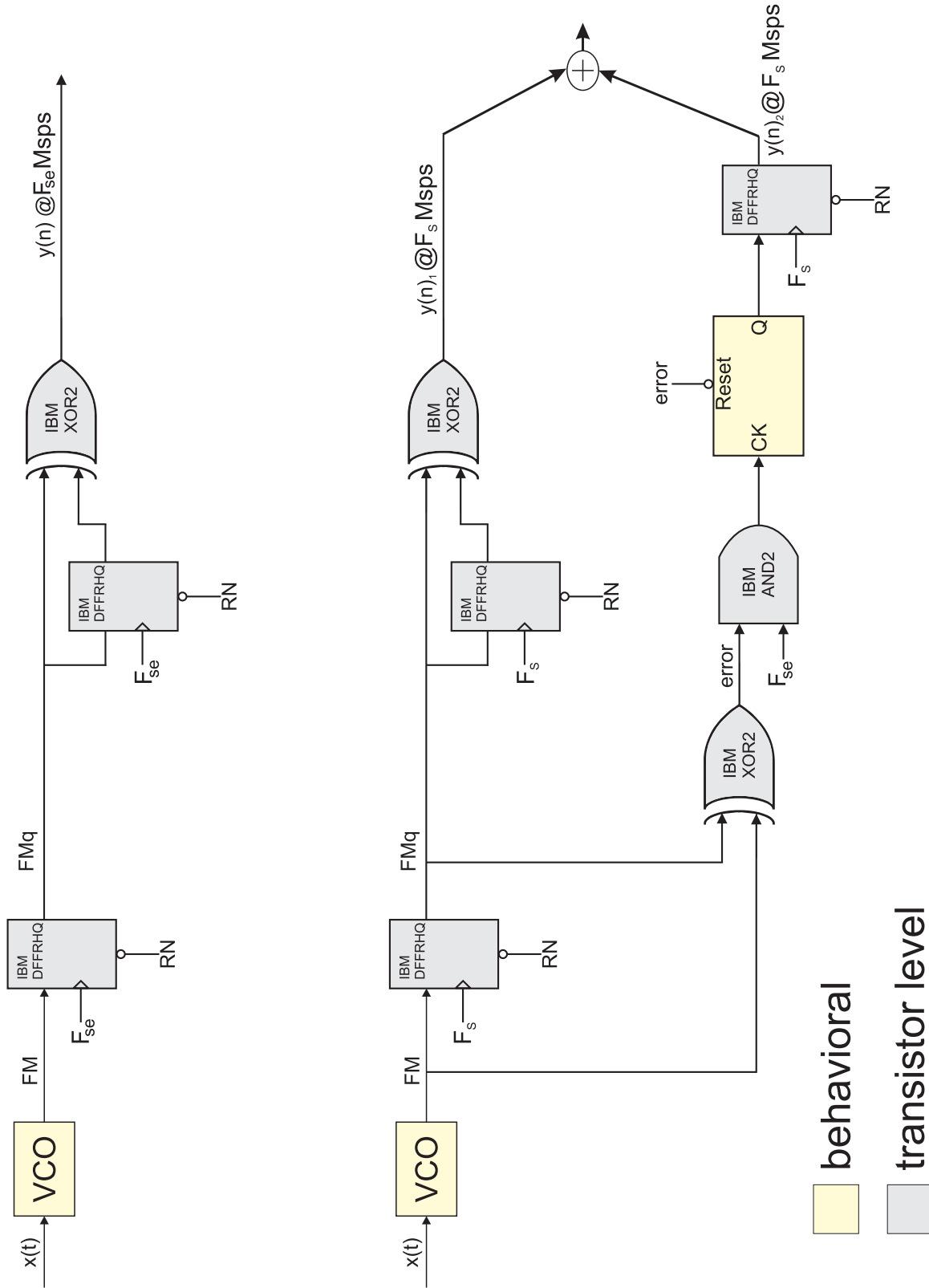


Figure 5.15: Testbench for the comparison of the first-order FIR modulator utilizing the same elevated sampling frequency F_{se} as the second-order modulator shown in the lower part of the figure.

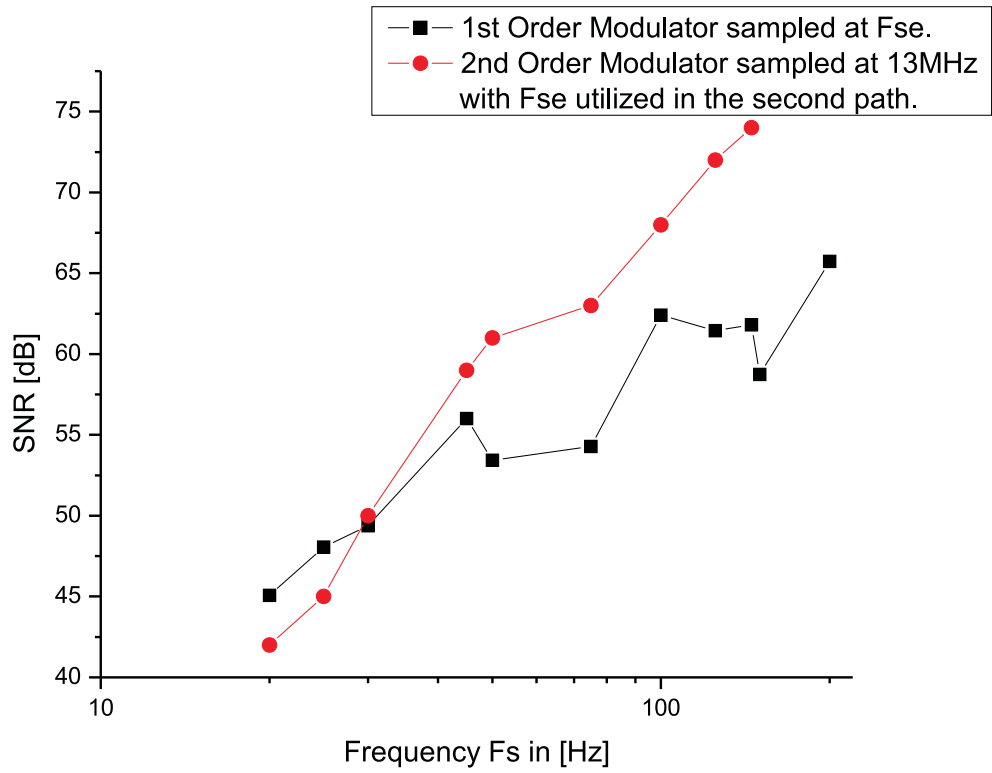


Figure 5.16: The second order modulator's upper path is clocked at F_s and the lower path at the elevated frequency F_{se} . The first-order modulator is clocked at the elevated frequency F_{se} also. Circuit/Acquisition Details: $K_{vco}=100\text{kHz}$, $f_{bw}=20\text{kHz}$, $F_c=4.4\text{MHz}$, $f_{in}=12.41\text{kHz}$, $F_s=13\text{MHz}$.

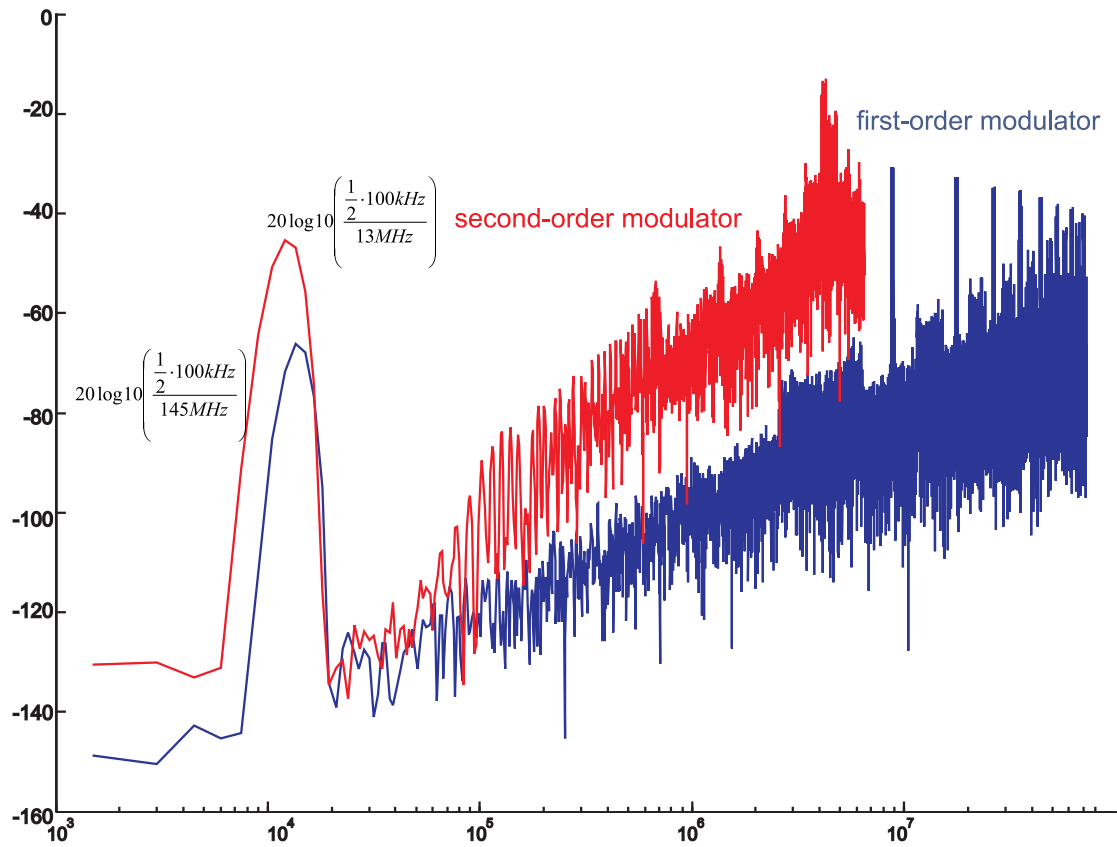


Figure 5.17: Comparison of the PSD plot for the first and second-order modulators. Circuit/Acquisition Details: $K_{vco}=100$ kHz, $f_{bw}=20$ kHz, $F_c=4.4$ MHz, $f_{in}=12.41$ kHz, $F_s=13$ MHz, $F_{se}=145$ MHz.

quantization error $\epsilon_{F_{se}}$ introduced when quantizing ϵ_1 . As a result, this new topology has a significantly reduced circuit count. In a next step, the topology was adapted to make use of the powerful undersampling techniques. Again, a mathematical model was given for the introduced quantization error sources. An signal-to-noise ratio equation was derived, which was then successfully verified by simulating the topology. Simulation results given include both, conventional sampling and undersampling of the frequency modulated signal at the output of the VCO. It was concluded that a major benefit of the last topology is that it can be used for conventional sampling as well as undersampling applications, making it a versatile topology. As in the case of the first version of the second-order modulator, an overall SNR increase of 6dB was achieved for doubling F_{se} even though the circuitry was reduced.

CHAPTER VI

DISCUSSION AND FUTURE WORK

In this thesis, various novel approaches were taken to realize first-order and higher order delta-sigma modulators without feedback. More specifically, two versions of a first-order modulator were proposed and two versions of a second-order modulator were presented. As a practical application, and to show proof-of-concept, a digital microphone was implemented and experimental results obtained.

6.1 First-Order FIR Modulators

These approaches include the realization of first-order modulator topologies utilizing an oscillator as frequency modulator and either an asynchronous D-FF or asynchronous counter for frequency de-modulation and noise shaping of the introduced time-domain quantization noise. It was found that the SNR is proportional to the frequency modulation sensitivity of the oscillator and 6dB of increase in SNR can be achieved for doubling the sensitivity. Since the attenuation of the introduced quantization noise is directly proportional to the sampling frequency, a two-fold increase in F_s will result in slightly more than 3dB of SNR increase. This 3dB increase in SNR for doubling the sampling frequency F_s was also achieved by the first-order topology from [Hovin et al., 1997]. However, the circuit we proposed is simpler as the XOR gate and D-FF as depicted in Figure 3.5 were combined into one asynchronous D-FF as described in section 3.2 and shown in figure 3.6. This asynchronous D-FF performed the simultaneous operation of time-domain quantization and noise-shaping of the quantization noise. Conventional delta-sigma converters (with feedback) are capable of achieving 9dB for doubling the sampling frequency F_s [Norsworthy et al., 1997]. However, it is more difficult to move to high oversampling ratios as the entire system (analog + digital)

needs to be able to support these high frequencies. Hence, continuous time architectures can support much higher speeds [Raghavan et al., 2001a]. In the FIR modulators we presented, only the demodulation part, which is an all digital circuit, has to run at the desired sampling frequency. Hence, the maximum speed is determined by the metastability requirements set by the asynchronous D-FF only.

In a second circuit implementation we replaced the asynchronous D-FF with an asynchronous counter as depicted in figure 3.8. The counter is an ideal way to utilize undersampling as it can be used to reduce the requirements on the demodulation circuitry and help with meta-stability problems as described in section 3.5.1. That is, it is even easier to move to very high frequencies with the oscillator, yielding more frequency modulation and thus more dynamic range, and then using undersampling to de-modulate the signal. When considering conventional undersampling applications such as [Vaughan et al., 1991b; Analog Devices, 1998], it is noted that there are specific requirements on the choosing the sampling frequency F_s , as otherwise spectral reversal might occur, or the desired signal be frequency-translated to above the Nyquist frequency. The asynchronous counter from figure 3.8 circumvents these two problems as it retains all the signal information in between sampling instances, as long as the final count value of the counter is large enough. When comparing our two FIR modulators to the works of [Ian Galton and Siragusa, 1998], the FIR modulator principle presented by us offers mainly simpler circuitry as no feedback path is required. Considering that Galton's work presented [Ian Galton and Siragusa, 1998] does not include frequency modulation, his entire circuit may be replaced by the here presented resetting counter to obtain first-order noise shaping. No additional charge-pumps, phase detectors, S/H circuits and N-bit ADCS are required.

6.2 *Second-Order FIR Modulators*

The second-order realizations which are based upon a cascade of two first-order FIR modulators are distinctive in the way that still no feedback path is needed to realize

the second-order noise shaping. The second path in the cascade is an all digital approach and does not comprise of any analog components. This differs from all the other published second order modulators topologies as they all use negative feedback [Ian Galton and Siragusa, 1998; Izadi and Leung, 2002; Sharifkhani, 2004; Thomas A. D. Riley and Plett, 1998; Riley et al., 1993]. In [Ian Galton and Siragusa, 1998] an analog charge pump and capacitor are needed to implement an integrator. For a good overall performance it is crucial for the current pulses of the charge pump to be produced with a high level of accuracy. This is difficult to achieve in practice, however. The reasons for this are a mismatch in the speed of p-channel and n-channel transistors in the current sources for example [Rhee, 1999]. Furthermore, the switches for switching in the appropriate current pulses will have a finite rise and fall time. Since the pulses operating the switched contain all the information, finite rise and fall time will result in a charge error at the capacitor [Jae-Shin et al., 2000]. Furthermore, this error might be amplified by charge injection. The capacitor needed to realize an integrator in conjunction with the CP is quite area expensive also. While a direct performance comparison between the work of [Ian Galton and Siragusa, 1998] and the second order modulators presented in this work is difficult, it is easy to see that from a circuit point of view the 2nd order FIR modulators seem more beneficial. The second order modulator presented by [Hovin et al., 1997] utilizes two first-order modulators to implement a second order modulator. While the first 1st-order modulator operates without feedback, the second 1st-order modulator uses a negative feedback path. Again, a charge pump is needed to realize an integrator and the aforementioned problems apply here as well. The second version of the 2nd-order modulator shown in figure 5.11 excels in that it uses a novel width-counter to realize one of the differentiators needed. That is, we used the width-value to realize differentiation as described in section 5.2.3. Hence, standard CMOS digital circuitry can be used to extend the performance of a first-order FIR modulator to a second order topology. When comparing our second-order FIR modulator with the work of [Hovin et al., 1997], it is realized that his work still relies on feedback in his cascaded approach. That is, a charge pump is needed as an integrator in conjunction

with negative feedback. Likewise, the third-order modulator of [Thomas A. D. Riley and Plett, 1998] needs a phase detector and charge pump along with a continuous-time operational amplifier to achieve 3rd-order noise shaping. The FIR modulator on the other hand does not need any additional analog components as an all-digital FIR modulator is realized using a novel width counter which is responsible for noise-shaping the introduced quantization noise.

6.3 *Undersampling Digital Microphone*

A digital microphone was realized in two different circuit implementations to show proof-of-concept of the first-order FIR modulator. The two implementations are shown in figures 4.2 and 4.9. Implementing a microphone with a FIR modulator reduces the circuitry as no analog pre-amp is needed to condition the signal for analog-to-digital conversion as it is done in conventional condenser microphones [Pastille, 2000]. Furthermore, the FIR approach does not consist of any noisy high-impedance resistors which, in conventional applications, form a high-pass RC network characteristic preventing measuring low frequency audio signals. In [Brauer et al., 2004] the noise due to resistances was studied in detail. It was found that ideally the resistor value should be decreased to reduce the effects due to noise. But this has an undesired effect as together with the capacitance of the microphone the load resistor forms a high-pass filter with a cut-off frequency in the acoustic band [Brauer et al., 2004]. To alleviate this problem, in a first step, an LC-oscillator was used for generating a frequency-modulated signal which could then be digitized by the FIR modulator. Usually, a high capsule polarization voltage is necessary for the condenser capsule; however, the LC-oscillator condenser microphone uses a comparatively low voltage, generated by the oscillator. Since discrete components were used to realize the LC-oscillator the frequency of oscillation was somewhat limited. This was also due to the large condenser capacitance that had to be used. Experimental results showed a good dynamic range over a somewhat limited bandwidth. It was found that circuit noise and power supply noise were a limiting factor in the performance of the system. Furthermore, due the small change in

capacitance and low frequency of oscillation, only a very narrow band frequency modulation was obtained. As a consequence, a Schmitt-trigger oscillator was used to move to higher frequencies of oscillation and thus obtain a higher sensitivity resulting in more dynamic range. Also, a battery-supplied approach was taken to minimize power supply noise. When testing this circuit, it was found that a higher dynamic range was possible over a ten-fold increase in bandwidth. This showed that moving to higher frequencies, and ridding the circuitry of power supply noise, greatly increased the performance to approximately 11 bits of resolution over a frequency band of 20kHz. While this is still not comparable to the results obtained from a commercial product [Tascam, 2007], it shows that when moving to higher frequencies, and using an integrated approach better performance can be achieved. Ring-oscillators can be implemented as an integrated circuit, and thus the presented FIR modulators could benefit from the lower noise figure associated with an IC approach.

6.4 Future Work: Microphone Utilizing an Integrated Ring Oscillator

It was shown that a first-order SDM can be realized by using an oscillator and a D-FF. This simple approach was then used to realize a digital microphone application. A condenser capsule was used to modulate a carrier frequency utilizing a Schmitt-trigger based oscillator. The advantage of using such a topology to digitize speech is that this approach is capable of measuring low frequency audio signals with a low noise figure. In conventional condenser microphones the change in capacitance is read across a noisy high impedance resistor which forms a high-Pass RC network, preventing the measuring of low frequency audio signals. Additionally, no analog pre-amp is needed to condition the signal for analog-to-digital conversion as is done in conventional setups. Further applications of the presented approach include capacitance-to-digital converters which are coming into widespread use in human-to-machine interfaces [Pratt, 2006]. Another benefit is that the presented circuit is easily expandable to integrated circuits using ring oscillators. When testing the LC and Relaxation oscillator in Section 4, it

was found that better results can be obtained when moving to an integrated approach. For example, consider a N -stage ring oscillator with the condenser capsule sitting at one (or all) of the inverter output nodes as depicted in fig. 6.1 a). The frequency of oscillation is determined by the delay through the inverter and thus by the change in capacitance. The capacitance could be realized by hovering a membrane over the ring oscillator chip. This is depicted in fig. 6.1 b). A change in capacitance is mainly formed by the vibrating membrane and the top metal area of the ring oscillator nodes on the die. Thus this topology could lend itself to be a more attractive integrated solution. Of course this would require the package to be as thin as possible (bare-die is best). Much higher frequencies can be achieved resulting in a better resolution of the circuit. Since a dynamic-range increase of \sqrt{M} can be achieved for an M increase in oscillation frequency, an integrated approach will be capable of producing better resolutions. Also seen in figure 6.1 is a second ring-oscillator with a constant capacitance. This oscillator can be used to generate a clock signal used for resetting the counter. Having this pseudo-differential setup will minimize errors as both oscillators will be affected in the same way. To further improve the performance of such an topology, one can incorporate second order noise shaping techniques presented in section 5 into the integrated approach.

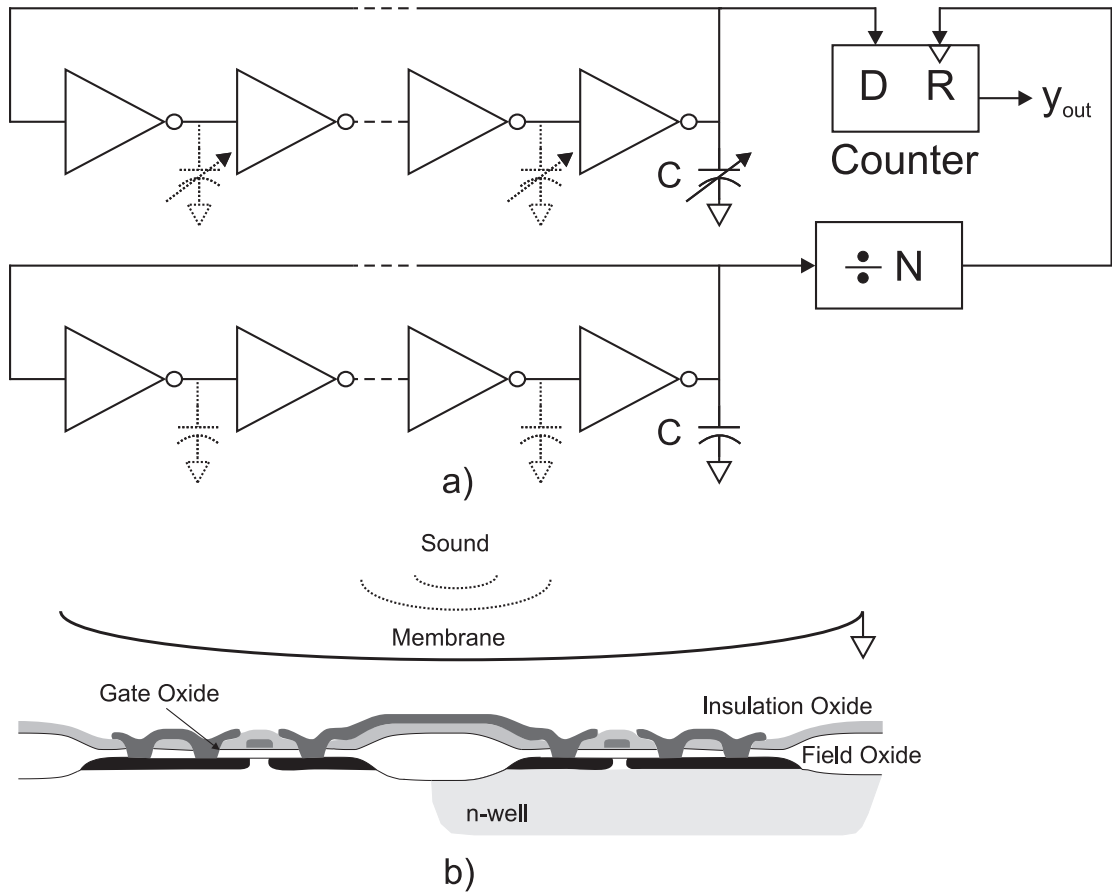


Figure 6.1: a) Alternative circuit using an integrated approach utilizing ring oscillators. The upper ring oscillator is responsible for generating the FM signal which is then quantized and differentiated by the resetting counter. The counter is reset by the lower ring oscillator. b) Simplified inverter cross-section. The change in capacitance is caused by the vibrating membrane over the chip. The capacitance is formed between the grounded membrane and the top metal area of the ring oscillator nodes on the die.

APPENDIX A

VERILOGA/AMS LISTINGS

The VeriloA/AMS models to test and verify the poroposed circuits are given in this section.

A.1 First Order FIR Modulator - Resetting Counter

```

1  'include "disciplines.vams"
    'include "constants.vams"

    module sdvcoct (out, in, clk);

6  input  in, clk; voltage in, clk;
    output out;      voltage out;
    parameter real f0=1e6; // carrier frequency VCO
    parameter real Kvco=50e5; // gain VCO
    parameter real jitter=0; // jitter in seconds
11 real freq, phase, n, count, dT;
    integer x, y, seed, fptr;
    analog begin

        @(initial_step) begin
16          fptr=$fopen("output");
            seed = -561;
        end

        freq = f0+Kvco*V(in);
21      freq = freq/(1 + dT*freq);

        phase = 2*'M_PI*(laplace_nd(freq, {1},{0, 1})↓
→          %1-0.5);
        @(cross(phase+'M_PI/2,+1) or cross(phase-'M_PI↓
→          /2,+1))
        begin
26          dT = 'M_SQRT2*jitter*$dist_normal(seed,0, 1);
            n = (phase >= -'M_PI/2) && (phase < 'M_PI/2);
        end

        @(cross(n - 0.5 ,0)) count=count+1;

```

```

31      @(cross(V(clk) - 0.5,1)) begin
          $fstrobe(fpstr, "%g", count); count=0;
        end

36      @(final_step) $fclose(fpstr);

          V(out) <+ n;

        end
41    endmodule

```

Listing 1: (sdm.va) First Order FIR Modulator in VERILOGA/AMS

A.2 *Second Order FIR Modulator V.I*

```

1  'include "disciplines.vams"
    'include "constants.vams"

4  module sdm (out, in, clk, clk1);

        input in, clk, clk1; voltage in, clk, clk1;
        output out; voltage out;

9  parameter real f0=1e6; // Carrier frequency VCO
    parameter real Kvco=50e5; // Gain VCO
    parameter real period=1/25e6; // Sampling frequency

        integer fptr1, fptr2;
14     real count, FM, errs;
        real freq, phase, n;
        real carry, count1, comb, counte;
        integer s_a, s_b, err;

19    analog begin

        @(initial_step)
            begin
                fptr1=$fopen("/out1");
24                fptr2=$fopen("/out2");
            end

        //***** VCO *****/
        freq = f0+Kvco*V(in);

```



```

29     phase = 2* 'M_PI*(laplace_nd(freq, {1},{0, 1})↓
→       %1-0.5);
       @(cross(phase+'M_PI/2,+1) or cross(phase-'M_PI↓
→       /2,+1))
       begin
           n = (phase >= -'M_PI/2) && (phase < 'M_PI/2)↓
→       ;
       end

34     //***** Upper Path Resetting Counter *****//
       @(cross(n - 0.5,1) or cross(n - 0.5, -1))
       begin
           count=count+1;
39     end

       //***** Sampling FM Signal *****//
       @(cross(V(clk) - 0.5, 1)) FM = n;

44     //***** XOR *****//
       s_a = (n > 0.5)? 1: 0;
       s_b = (FM > 0.5)? 1: 0;
       err = (s_a^s_b);

49     @(cross(V(clk1) - 0.5, 1)) begin errs=err; end
       comb = V(clk1)*errs;

       //***** Integrating Counter *****//
       carry = 0;
54     @(cross(comb - 0.5, 1)) counte=counte+(1/10.0);
       @(cross(counte - 1.0, 1)) begin carry=1; end

       //***** Differentiating Counter *****//
59     @(cross(carry - 0.5,1)) count1=count1+1;
       @(cross(V(clk) - 0.5,1))
       begin
           $fstrobe(fp1r1, "%g", count); count=0;
           $fstrobe(fp1r2, "%g", count1); count1=0;
64     end

       V(out) <+ carry;

end
69 endmodule

```

Listing 2: (2ndVersionI.va) Second Order FIR Modulator V.I in VERILOGA/AMS

A.3 Second Order FIR Modulator V.II - Undersampling

```

1  'include "disciplines.vams"
    'include "constants.vams"

    module sdm (out, in, clk, clk1);

6  input in, clk, clk1; voltage in, clk, clk1;
    output out; voltage out;

    parameter real f0=1e6; // Carrier frequency VCO
    parameter real Kvco=50e5; // Gain VCO
11 parameter real period=1/25e6; // Sampling frequency

    integer fptr1, fptr2;
    real count, count1, FM, y1;
    real freq, phase, n;
16 real err;

    analog begin

        @(initial_step)
21         begin
            fptr1=$fopen("/VCO/out1");
            fptr2=$fopen("/VCO/out2");
            end

26 //***** VCO *****/
        freq = f0+Kvco*V(in);
        phase = 2*'M_PI*(laplace_nd(freq,{1},{0, 1})↓
→         %1-0.5);
        @(cross(phase+'M_PI/2,+1) or cross(phase-'M_PI↓
→         /2,+1))
            begin
31         n = (phase >= -'M_PI/2) && (phase < 'M_PI/2)↓
→         ;
            end

        //***** Sampling FM Signal *****/
        @(cross(V(clk) - 0.5, 1)) FM = n;

36 //***** Generating Y1 (XOR) Signal *****/
        FMd = zi_nd(FM,{1},{1},period);
        y1 = abs(FM-FMd);

41 //***** Freerunning Counter Reset *****/
        @(cross(n - 0.5 ,0))

```

```

        begin
            count1=0;
        end

46
        /** Freerunning Counter Determining Width **/
        @(cross(V(clk1) - 0.5 ,1))
        begin
            count1 = count1+1;
51        end

        /** Freerunning Counter Read Out **/
        @(cross(y1 - 0.5, 1))
        begin
56            err=count1;
        end

        /** Saving Outputs **/
        @(cross(V(clk) - 0.5,1 ))
61        begin
            $fstrobe(fptr1, "%g", y1);
            $fstrobe(fptr2, "%g", err);
            err=0;
        end

66
        /** Closing Files **/
        @(final_step)
        begin
            $fclose(fptr1); $fclose(fptr2);
71        end

        V(out) <+ FM;

    end
76 endmodule

```

Listing 3: (finalLS2under.va) Second Order FIR Modulator V.II - Undersampling in VERILOGA/AMS

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