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# Millimeter-Wave and Terahertz Technology for Integrated Circuits



By

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Submitted in fulfilment of the requirements for the

Degree of Doctor of Philosophy

School of Engineering

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*“What if”*

-David Goggins

# Abstract

In recent years, there has been rapid growth in the use of millimeter-wave or Terahertz-wave frequencies for various applications like communication, imaging, medical sciences and space instrumentation. As the semiconductor processing technologies have enhanced from past years and with state of the art TMIC (Terahertz Monolithic Integrated Circuits) offering increased cut-off frequencies ( $>1$  THz) of HEMT / HBT transistors, these applications have become even more feasible and can now be integrated onto a single chip for low cost and compact production.

The work carried out in this thesis mainly deals with the development of passive structures such as transmission lines, antenna, couplers and power dividers, which are compatible to available TMIC processes using GaN on low resistivity silicon as a substrate. Techniques to reduce ohmic contact resistance for GaN HEMT technology was also investigated. To reduce losses caused by the substrate and to enhance performance of the integrated antenna at THz frequencies, passive structures were shielded using silicon nitride and metal, in addition to a layer of low dielectric material. Transmission lines were designed with operational frequencies up to 1 THz, in order to demonstrate losses presented by several dielectric mediums- air, BCB (Benzocyclobutene) and SiO<sub>2</sub> (Silicon-dioxide). BCB and SiO<sub>2</sub> were also investigated to evaluate antenna performance. For this, various types of antenna were designed - rectangular, circular, three variants of stack antenna (double rectangular, double circular, rectangular-circular), array antenna and stack array antenna. These designs were studied at two different frequencies, 300 and 650 GHz. Both simulated and measured results are presented, which show the importance of using low dielectric materials at THz frequencies. Other passive structures, such as couplers and power dividers were designed using the shielding technique mentioned above. Here, four different hybrid junction couplers (branch line, cascaded branch line, rat race, curved rat race) and one power divider (Wilkinson) were designed at three frequencies: 90, 300, and 650 GHz. The results presented by both antenna and couplers showed the viability of the shielding technique used.

The optimisation of ohmic contact formation on AlGaN/GaN layers on LR Si has been studied by way of etching into the substrate under metal contacts. This investigation compared various etch patterns to standard, unetched, contacts. The depth of these patterns was varied to be above and below the substrates conductive channel and Ti/Al/Ni/Au metal schemes was used. A contact resistance below  $0.3 \Omega \cdot \text{mm}$  was achieved using a grid etch pattern.

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# Publications

## Journal Publications

A. Eblabla; B. Benakaprasad; X. Li; D. J. Wallis; I. Guiney; K. Elgaid, "Low-loss MMICs viable transmission media for GaN-on-low resistivity silicon technology," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 10-12, 2017.

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B. Benakaprasad; A. Eblabla; X. Li; D. J. Wallis; I. Guiney; C. Humphreys; K. Elgaid, "Terahertz microstrip elevated stack antenna technology on GaN-on-low resistivity silicon substrates for TMIC," in *46th European Microwave Conference (EuMC)*, London, UK, 2016.

B. Benakaprasad; A. Eblabla; X. Li; I. Thayne; D. J. Wallis; I. Guiney; C. Humphreys; K. Elgaid, "Terahertz monolithic integrated circuits (TMICs) array antenna technology on GaN-on-Low resistivity silicon substrates," in *41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, Copenhagen, Denmark, 2016.

B. Benakaprasad; A. Eblabla; X. Li; I. Thayne; D. J. Wallis; I. Guiney; C. Humphreys; K. Elgaid, "Terahertz Microstrip Single patch antenna technology on GaN-on-low resistivity silicon substrates for TMIC," in *IET Colloquium on Antennas, Wireless and Electromagnetics*, Glasgow, UK, 26 May 2016.- Unpublished

B. Benakaprasad; A. Eblabla; X. Li; D. J. Wallis; I. Guiney; K. Elgaid, "Design and performance comparison of various terahertz microstrip antennas on GaN-on-low resistivity silicon substrates for TMIC", in *Asian-Pacific Microwave Conference (APMC)*, New-Delhi, India, 2016 .

A. Eblabla; B. Benakaprasad; X. Li; D. J. Wallis; I. Guiney; C. Humphreys; K. Elgaid, "Passive Components Technology for THz-Monolithic Integrated Circuits (THz-MIC)," in *18th International Radar Symposium (IRS)*, Prague, Czech Republic, 28 June 2017.

A. Eblabla; B. Benakaprasad; X. Li; D.J. Wallis; I. Guiney; K. Elgaid, "High Frequency Active and Passives Devices using GaN on Low Resistivity Silicon," in *ARMMS RF & Microwave Society Conference*, Milton Common Nr Thame, UK, 18-19 April 2016. - Unpublished

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## Introduction

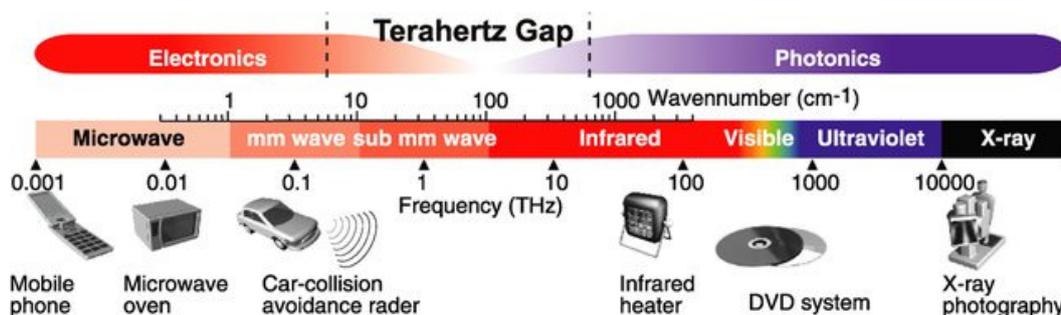
### 1.1 Introduction

The terahertz frequency (THz) band ranges from 0.1 to 10 THz in an electromagnetic spectrum which lies between microwave and infrared optics. Technology which generates or detects terahertz radiation is in its infancy. This has led to the engineering term ‘terahertz gap’, a band of frequencies that has so far not been exploited to its potential. In the last few decades, growth in semiconductor research has driven interest in this area [1.1]. With recent progress in terahertz technology, various potential applications in the field of science and technology has emerged. Applications such as time-domain spectroscopy, medical science, space instrumentation, imaging, sensing and agriculture to name just a few. The broad application of the terahertz spectrum is due to its unique radiation characteristics, such as the ability to penetrate through different materials with different attenuation levels, increased image resolution compared to the microwave regime (due to shorter wavelength), unique terahertz signature for detecting various solid and gaseous materials (spectroscopy) and low ionization [1.2]. In this work, millimeter wave (MM-wave) and terahertz systems are approached for communication applications.

### 1.2 Millimeter-wave and terahertz Communication

Due to ever increasing demands on data and voice communication and an exponential growth of population, the need for high data rate communication systems is also increasing. To bolster data rates, the bandwidth of existing communication systems has to be enhanced or the operational frequencies of these systems needs to increase. As most current systems are designed with narrow bandwidth (in many cases only 10 % of the operating frequency) the latter solution is likely to see greater adoption. Initially, operating frequencies in wireless systems were increased to 60 GHz and 90 GHz. When this became insufficient, the

operational frequency was further increased into the terahertz band [1.1]. As the operational frequency increases, the device design changes and due to its unique position in the electromagnetic spectrum (Fig. 1.1), devices operating in the terahertz band can be designed using both an electronic or photonic approach. The electronic design approach is explored at the lower submillimeter wavelength, while the photonic design approach is explored at far-infrared signals.



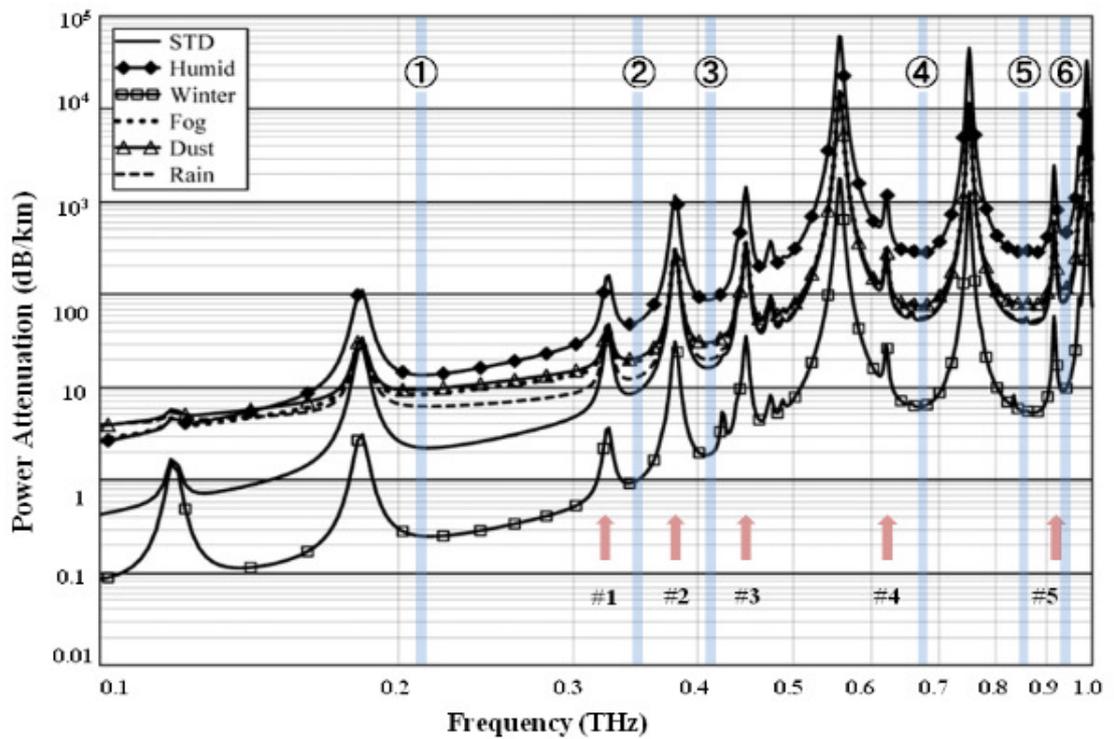
**Fig. 1.1:** Illustration of the terahertz gap [1.3] Copyright © 2010, Springer-Verlag.

There are several reasons that motivate the use of the terahertz band for ultra-broadband communications when compared with the microwave and far-infrared band [1.1] [1.4]:

- (1) The microwave band is already extremely crowded and below 100 GHz cannot support throughput such as Tbps (Terabytes per second). Above 250 GHz, the licenses are free to use.
- (2) THz communications are more directional than microwave or millimeter (MMW) due to less free-space diffraction of the waves. Line of sight detection and point to point communication is required.
- (3) Offers high degree of information security, especially in the spread spectrum.
- (4) Compared to infrared, has low attenuation of signal in certain atmospheric conditions like fog, rain, dust or pollution and low diffusion reflection losses, low misalignment between transmitter and receiver.
- (5) Fiber communication is used to generate and detect optical signals, which are injected into optical front end. These optical systems are typically large, heavy and hinders use for personal and mobile applications.

One of the main limitations in realising terahertz wireless communication compared to mm-wave is the atmospheric path loss. This loss is affected by various atmospheric conditions such as rain, fog and pollution which impede the propagation of electromagnetic waves. Fig. 1.2 shows a plot of attenuation loss (dB/km) over the frequency range 100 GHz to 1000 GHz [1.5]. It can be noted that THz propagation is largely influenced by atmospheric conditions.

The attenuation level increases with changes in weather conditions and height. However, there is less atmospheric attenuation (below 100 dB/km) at certain frequency ranges known as ‘windows’. If a THz communication system is not designed to operate within these windows, it could be confined to indoor communication. Below 1 THz, this window appears around 220 GHz, 300 GHz, 350 GHz, 410 GHz, 650 GHz and 850 GHz [1.6]. These frequency windows can be used for building short-range wireless communication systems (>1 cm). Above a height of 16 km, where moisture is negligible and attenuation is also trivial, inter-satellite communication can be built. In this thesis, device performance are evaluated around these frequency windows.



**Fig. 1.2:** Atmospheric attenuation at sea level for different conditions such as fog, dust, rain [1.5] Copyright © 2011, OSA.

## 1.3 Aims and Objectives

The aim of this work was to develop passive devices for TMIC compatible applications, using GaN on low resistivity silicon substrates. The main focus was on the frequency band 90 - 1000 GHz (especially around low loss windows). In addition, the aim was also to investigate a method to lower contact resistance on AlGaIn/GaN layer. In order to accomplish this, the research was carried out as follows:

- Study existing on-chip antenna at terahertz and design antenna which performs well while also offering lower loss integration to active circuits without any complex micromachining or high temperature fabrication.
- Perform a throw analysis into the performance of potential, antenna, low-loss transmission lines structures, couplers and power dividers suitable for mm-wave and terahertz frequencies (where frequency windows are open, around 300 GHz, 650 GHz, and 1 THz).
- Design novel ideas using a 3D simulator, to verify passive performance and develop methods to fabricate these devices.
- Perform physical measurement and analysis of results, to determine the performance of devices.
- For metal-semiconductor contact, study current methods to lower the contact resistance on other material systems. Fabricate and test structures based on this analysis.

## 1.4 Thesis organisation

This thesis is divided into six chapters. This chapter (Chapter 1) introduce aims and objectives for operating within the terahertz frequency band, and the various applications which can be implemented. Various terahertz source and detectors are discussed, ranging from solid-state electronics to lasers. Review of devices developed for Terahertz Monolithic Integrated Circuits (TMIC) designs to date are presented and discussed.

Chapter 2 discusses fabrication and measurement techniques used in producing antennas, couplers and power dividers and ohmic contacts on GaN-on-LR Si substrates. In addition, the challenges associated with the fabrication of devices on this material system are discussed.

Chapter 3 presents simulation and measurement of fabricated antenna devices. A review of various techniques used to overcome limitations at terahertz frequencies are detailed, such as the shielding technique. Various transmission line, patch and array designs are presented using this shielding technique at frequencies of 300 and 650 GHz. Different dielectrics are used in this design and the need for low-dielectric materials when implementing devices is verified.

Chapter 4 presents the design of various hybrid junction couplers and power dividers at frequencies of 90, 300, and 650 GHz on GaN-on-LR Si. The shielding technique presented in Chapter 3 is used to compare the performance of devices at these frequencies.

Chapter 5 reviews formation of metal to semiconductor contacts on GaN and proposes techniques to reduce ohmic contact resistance. Several strategies of etching the substrate beneath contacts are investigated, as well as different metallisation approaches.

Finally, Chapter 6 provides a summary of research findings and outcomes. Future work for the advancement of THz technology is discussed.

## 1.5 Review of Millimeter-wave and Terahertz Circuit

### Millimeter-wave and terahertz sources and detectors

There is a need to develop new designs for sources and detectors that can efficiently perform at terahertz frequencies. High power, high sensitivity and low noise figure are an additional requirement of existing devices to overcome the losses of atmospheric attenuation [1.4].

There are a wide variety of sources available for terahertz radiation. Vacuum electronic sources are backward wave oscillators (BWO), travelling wave tubes, gyrotrons, magnetrons and klystrons. These sources are bulky and have high power requirements. Solid-state electronic sources include Gunn diodes and high frequency transistors. Frequency multipliers can also be used to shift lower frequency oscillators into the terahertz band. Terahertz direct laser sources include the optically pumped laser and quantum cascaded laser, while laser enabled sources include terahertz parametric oscillators, photo-mixing and time domain systems.

The earliest THz detectors were based on the thermometric property of materials like the bolometer (change in electrical resistance with temperature) and the Golay cell (change in size with temperature) [1.7]. These are uncooled detectors and use an antenna to couple

power with small thermally absorbing regions. Microelectromechanical (MEMS) systems are sophisticated thermal detectors which incorporate sensor arrays for imaging. These devices are still underdeveloped and operate at specific frequencies. In addition, thermo-mechanical detectors are slower compared to solid-state electronic transistors. Electronic sensors, such as like quantum dots and single electron transistors, are typically based on bulk semiconductor materials [1.7].

Depending on the application, certain types of source and detector can be selected. For instance, solid-state electronic sources are better for applications which may require low to medium power, compactness and cost effectiveness (imaging or wireless communication). Since the circuits are implemented on semiconductor chips, one demand from semiconductor technologies is the increase of device speed. Due to this demand, RF electronics appeared in the form of Monolithic Microwave Integrated Circuits (MMIC). Here, both actives and passives are integrated on a small semiconductor chip. As the frequency of operation increased to the terahertz band, there was an emergence of Terahertz Monolithic Integrated Circuits (TMIC) [1.8].

Semiconductor technologies can be mainly divided into two groups: Si based ones and III-V compound based ones. For high frequency applications, III-V technologies based on GaN, GaAs, and InP have been favoured due to the following qualities. Firstly, they present high carrier mobility at relatively low electric field, as well as the distinct ballistic transport found at the boundary of high dielectric field regions. This significantly increases the operational speed of active devices. Secondly, substrate like GaN exhibit large breakdown voltages due to a large bandgap. In addition, resistivity higher than Si substrates are available (High resistivity substrate), which can be used for the design of low loss passives devices like transmission lines and inductors [1.2].

The most popular and efficient III-V devices for high frequency applications today are the High Electron Mobility Transistor (HEMT) and the Heterojunction Bipolar Transistor (HBT). Though both devices have good operational speed, HEMTs provide lower noise characteristics, especially at low temperatures, whereas HBTs tend to exhibit larger current driving capabilities and higher transconductance. Lai *et al.* were the first to drive state of the art HEMT technology to frequencies greater than 1 THz. They achieved an  $f_{max}$  of 1.2 THz with a  $f_T$  of around 385 GHz, based on sub-50 nm InGaAs/InAlAs/InP structures [1.9]. Urteaga *et al.* were the first to drive state of the art HBT technology greater than 1 THz. They achieved an  $f_{max}$  of 1.03 THz with a  $f_T$  of around 430 GHz, based on sub-25 nm InP/InGaAs/InP structures [1.10].

In this thesis, a GaN-on-LR Si substrate has been chosen for designing TMICs. GaN has advantages compared to other semiconductors, including wide bandgap (3.4 eV of GaN), large electric breakdown field strengths ( $\sim 3 \times 10^6$  V/cm) and high saturation electron drift velocity ( $> 2 \times 10^7$  cm/s). Table 1.1 shows the properties of commonly used semiconductors compared to GaN.

Parameters (Units)	Si	GaAs	InP	4H-SiC	GaN (AlGaN/GaN)
Energy bandgap (eV)	1.12	1.43	1.34	3.2	3.4
Relative dielectric constant, $\epsilon_r$	11.9	12.5	12.4	10.0	9.5
Thermal conductivity (W/Kcm)	1.5	0.54	0.67	4	1.3
Breakdown electric field (MV/cm)	0.3	0.4	0.45	3.5	3.3
Saturated electron velocity ( $10^7$ cm/s)	1	1	1	2	2.5
Electron mobility ( $\text{cm}^2/\text{Vs}$ )	1500	8500 (10,000)	5400 (10,000)	700	900 ( $> 2000$ )

**Table 1.1:** Semiconductor properties [1.11] [1.12].

The potential use of GaN HEMTs grown on LR Si for MMICs offers the advantage of cost-effective and large diameter wafers, resulting in manufacturing costs of GaN-on-LR Si becoming potentially competitive with existing high resistivity Si and SiC technologies [1.1].

Heterodyne receivers and transmitters use Local Oscillation (LO) as a source. For imaging and spectroscopy, oscillators can be used directly to generate THz signals. The term oscillations describes the ability for electrons to move back and forth in a transistor. Usually, at terahertz, circuit designers use oscillator harmonics (oscillation signals at multiple frequencies). While this increases the operational frequency, the output power is small compared to the power at a fundamental frequency. As such, effect has been to push fundamental oscillations into the THz band. Various transistors based on conventional oscillator designs, such as the common gate configuration with series feedback, differential series-tuned oscillator topology, triple-push architecture and phase locked loops (PLLs) have been adopted and performed well below 1 THz frequency [1.13]. Above 1 THz, RTD (Resonant Tunnelling Diode) based oscillators have proved effective. RTDs are quantum

effect devices with excellent performance in negative differential conductance (NDC) and show high speed [1.14].

Another key component in terahertz communication systems is the amplifier (low noise amplifier and power amplifier). As the name suggests, amplifiers are used to amplify the power of signal, depending on the application. Amplifier design consideration involves small-signal gain, output power, operational bandwidth, and circuit stability. The main problem is in pushing the operational frequency of these amplifiers above 1 THz. Northrop Grumman Corporation has demonstrated the highest frequency solid-state amplifier, for which they won a world record [1.15]. Their amplifier achieved a gain of 10 dB at a frequency of 1 THz, and 9 dB at 1.3 THz. The circuit was made on an InP substrate with a HEMT design and a 25 nm gate length.

THz receiver systems in the past have implemented SIS (superconductor-insulator-superconductor) mixers or Schottky diodes [1.13]. However, the conversion loss involved with passive devices significantly limited the sensitivity and flexibility of these receivers. In addition, they were found to be difficult to integrate with other circuits on the same die. As the development in high speed transistor technology improved, it became practicable to realize THz integrated transceivers. Many studies were carried out on a single-chip or a multi-chip solution for THz integrated transceivers [1.13]. Complete solid-state receiver systems may consist of LNAs, filters, antennas, detectors, mixers, multipliers and on-chip integration technology.

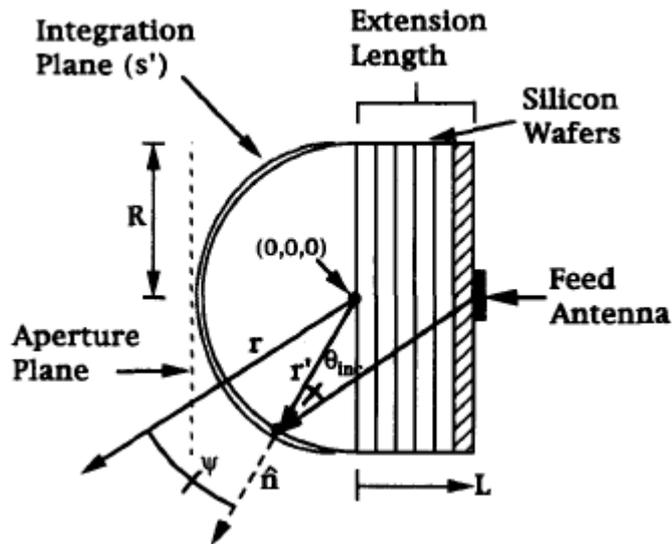
### Millimeter-wave and terahertz antennas

Most of the terahertz applications mentioned above rely on compact, wide bandwidth, electrically large, beamforming antennas. Terahertz antennas can be broadly divided into two different technology areas: antennas used for coupling power from free space into receivers or out of generators like diodes, transistors, photoconductive elements, bolometers, etc. and technology where the antenna beam is shaped or focussed for a variety of applications such as high-resolution imaging and scanning.

A major motivation for realising antennas at terahertz frequencies was in mapping and recording planetary, stellar and galactic spectroscopic emission and absorption lines in radio astronomy [1.16]. Traditional waveguide feedhorn and all planar structures were investigated for both single pixel and multi-element array applications, however constraints of high mechanical tolerances, investigators were forced towards new and simplified waveguide horn designs and towards a large variation of new planar antennas, to take the

advantage of wafer integration. Since waveguide-based antenna are large in size to be placed close enough to comprehend contiguous diffraction limited spots on a scene (in imaging array). In addition, it is also expensive to be implemented, a planar integrated antenna became attractive and practical for the millimeter and submillimeter wave frequency applications which demands smaller, lighter, and cost-effective waveguide receivers [1.16] [1.17].

When designing broadside antenna, like dipoles, slots, log-periodic and patch, on a dielectric substrate, the antenna suffers from power loss due to substrate modes. These modes are exasperated by thick substrates, discussed in Chapter 3. This effect can be severe enough to cause the antenna to radiate more power into the substrate than into free space. One way to eliminate the problem of surface modes is to incorporate a dielectric layer of infinite thickness, i.e., antenna is placed on a semi-infinite dielectric substrate, such as a lens. The planar thick-lens antenna structure was invented by Rutledge *et al.* in the 1980's [1.18]. The primary source is placed at the back of a collimating lens, which increases the gain and directivity of the planar antenna. Here, most of the power is radiated into the substrate with a factor of  $\epsilon_r$  (dipole) and  $\epsilon_r^{3/2}$  (slot) compared to air. Depending on the type of lens used, the lens can bend the rays radiated by the antenna towards the broadside direction, thus sharpening the pattern and successfully increasing the gain of the antenna. Filipovic *et al.* used this lens strategy with a double slot antenna at 246 GHz to achieve a directivity of 29.4 dB  $\pm$  0.3 dB for an extension length of 2700  $\mu\text{m}$  (lens length) [1.19]. Fig. 1.3 shows this. Here, the directivity of the antenna is increased by increasing the extension length and size of the lens, where directivity also depends on the relative permittivity of the lens material. Recently, research at the Jet Propulsion Laboratory (JPL), of the California Institute of Technology, fabricated antenna on a 'leaky-wave' waveguide feed and silicon microlens operating at 1.9 THz. The two antenna realised were a 2.6-mm-diameter microlens antenna with directivity of 33.2 dB and a 6.35-mm-diameter microlens antenna with directivity of 41.2 dB [1.20]. The disadvantages of this technique include multiple reflections at the high dielectric lens-to-air interface, the dielectric loss of the thick lens itself, and the relatively large size of the device [1.16].



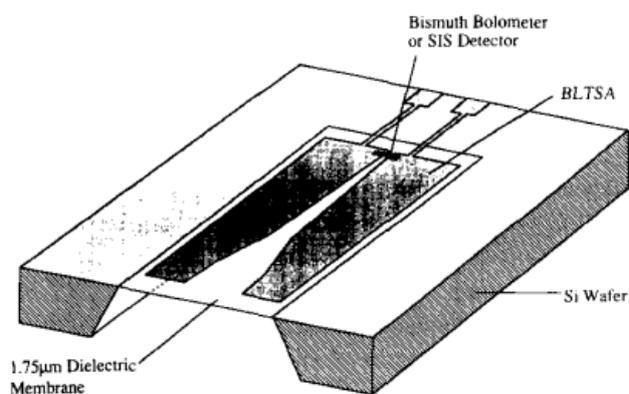
**Fig. 1.3:** Image of extended hemispherical lens integrated with Silicon wafer [1.19]

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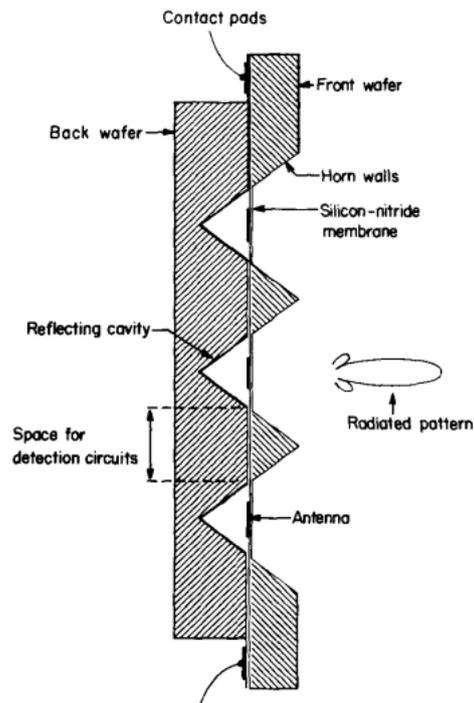
‘End-fire’ is another class of antenna which can be used for millimeter and submillimeter wave integrated circuits. An end-fire antenna usually radiates in the  $+y$  direction, as such the array can be expanded in the  $x$ -direction and  $z$ -direction which will reduce device size compared to broadside antennas. These antenna have wideband input impedance and medium gain patterns. One of the first end-fire antennas was reported by Yih Shiau using dielectric rod antenna and a micromachined  $\text{Al}_2\text{O}_3$  substrate for V-band communication. A V-shaped antenna was used to achieve end-fire radiation patterns in an 85 GHz monolithic receiver, which provided only 35 % efficiency, yet was simple to fabricate and it did not suffer from substrate mode problems [1.21]. End-fire antenna here revolutionised by the design of Vivaldi antenna, Tapered Slot Antenna (TSA), introduced by Gibson [1.22]. The antenna has an exponential tapered slot which can be etched on a metallized dielectric substrate. Gibson reported constant 3 dB beam width between  $30^\circ$  and  $40^\circ$  for two octaves. Over the decades, many studies have been carried out using TSAs due to ease of integration. More recently, two end-fire on-chip antennas were designed at 140 and 320 GHz using ‘quasi-yagi’ antenna with loaded dielectric to reduce the effect of the LR Si substrate. The antenna showed a measured impedance bandwidth of  $> 45\%$  at 140 GHz, with a peak gain of 4.1 dBi at 140 GHz and 3.9 dBi at 320 GHz. The simulated peak radiation efficiency was 83 % and 80 %, respectively [1.23].

Rebeiz and Rutledge introduced a new method to mitigate the substrate mode problem [1.24] [1.25]. They removed the substrate beneath the antenna, which was suspended on a dielectric membrane (Fig. 1.4). Due to the thin membrane, the antenna radiated directly into the free

space. With this, dielectric loss is also eliminated and the design can be easily scaled for different wavelengths. As the antenna is designed on a Si substrate, other components like diodes and matching circuits can be easily designed on the same substrate. Rebeiz *et al.* designed the first antenna using this technique, with a log-periodic antenna backed by an absorbing cavity for wideband applications. A very good cross-polarisation of -20 dB was achieved, from 100 to 700 GHz. Based on dielectric membranes, antenna arrays were designed. Fig. 1.5 shows one of the antenna arrays designed using this technique, the integrated horn antenna, where a dipole feed is integrated on the membrane and other active components are integrated on the back side of the front antenna [1.26]. Other planar or on-chip antenna developed in recent years are further discussed in Chapter 3.

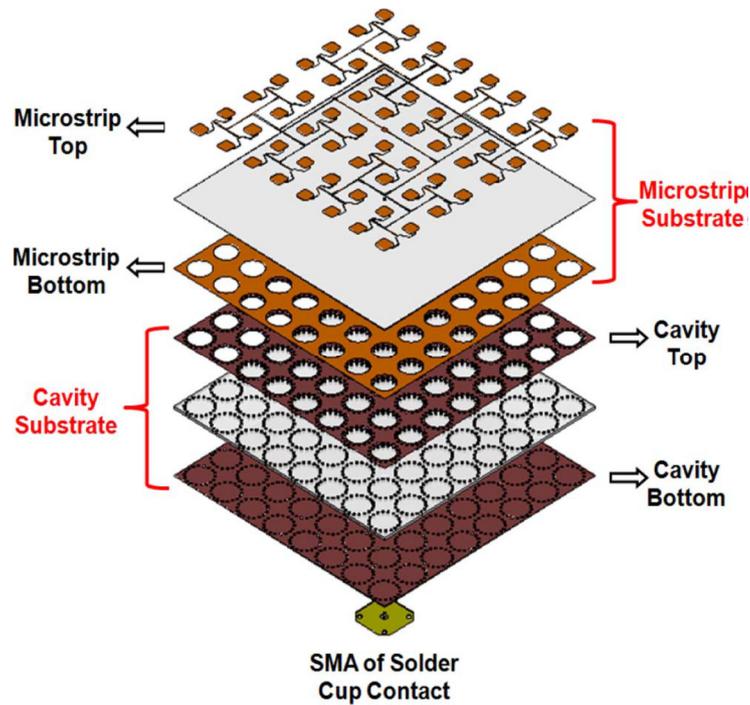


**Fig. 1.4:** LSTA antenna integrated on a thin dielectric membrane [1.17] Copyright © 1992, IEEE.



**Fig. 1.5:** Cross-sectional view of the integrated horn antenna [1.17] Copyright © 1992, IEEE.

Many non-conventional antenna structures have been developed in recent years which further improve upon antenna performance and integration. One such example is substrate-integrated antenna technology. The idea is based on the concept of Substrate-Integrated Circuits (SICs), where the non-planar structures are converted into planar structures, which allows planar fabrication processing of non-planar conformations and 3D structures [1.27]. Some planar processing techniques, such as Low-Temperature Co-fired Ceramic (LTCC) technology and Printed Circuit Board (PCB), are compatible with the transformation from nonplanar structure to planar configuration [1.28]. Over the years, many antennas using this technique have been developed, such as Substrate-Integrate Waveguide (SIW) cavity. This is connected with a patch antenna array to prevent surface waves. Fig. 1.6 shows an example of this. It consists of a stack of two substrates: the top substrate for patch and feed, and the bottom substrate for the SIW cavities [1.29].



**Fig. 1.6:** SIW cavity-backed patch antenna [1.27] Copyright © 2012, IEEE.

3D printed antennas have also been proposed at mm-wave and terahertz frequencies. The first 3D printed antenna consisted of a dual polarized horn design, reported in 2005 [1.30]. It was printed using Emerson and Coming HiK dielectric powder and achieved an averaged gain of 12 dBi over a bandwidth of 34 - 40 GHz. This technique is used only for passive devices, such as lenses, electromagnetic bandgap (EBG) structures, waveguides and horns. This is due to the limited resolution of current 3D printing. Up until now, the 3D horn antenna has achieved 500 GHz operational frequency, limited by roughness of the material and dimensional tolerances [1.31].

In general, the fabrication of antenna at THz frequency is challenging compared to MM-wave. Active research is still ongoing to improve antenna performance and to achieve simple integration with less loss in active circuits. In this thesis, a simple technique known as shielding is implemented using a low loss dielectric and GaN-on-LR Si substrates.

### Other passive components and integration at millimeter-wave and terahertz frequency

To realise complete terahertz circuits, design of passive components such as transmission lines, filters, couplers and power dividers are important. Just like antennas, these components also suffer from high substrate and radiation loss. To overcome this, circuits designed on low dielectric materials, or waveguides, are adopted. Tessmann *et al.* have used airbridge

type transmission line (ABTL) on InP substrate, where the transmission line is elevated in air to form a 500 GHz TMIC amplifier [1.32]. Nagel *et al.* designed a 0.61 THz second-order thin-film microstrip coupled-line band-pass filter on silicon, using BCB dielectric layers [1.33]. Mei *et al.* has designed lines on InP while using SiN as passivation. To overcome substrate mode losses, the substrate has been thinned down to 25  $\mu\text{m}$  [1.34]. Reck *et al.* designed tandem couplers on InP using coplanar waveguides and airbridges [1.35]. High performance waveguides can also be used for designing passive components. The IEEE P1785 working group proposed metallic waveguides that can operate up to 5 THz [1.36]. The University of Birmingham (UK) currently works on replacing bulk micromachining of Si with surface micromachining of SU-8 sacrificial building materials, to demonstrate split block waveguides from 0.5-0.75 THz [1.37]. The main disadvantage of a waveguide approach is the problem of integration. They are not very compact, nor easy to integrate. In this thesis, the same shielding technique used to investigate antenna performance has also been adopted to investigate the losses of the transmission lines, couplers and power dividers.

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## Fabrication

### 2.1 Introduction

Semiconductor fabrication is the process of creating integrated circuits from macro-scale to nano-scale used in electrical and electronic systems. This chapter introduces the details of fabrication processes for producing suspended antennas (stack antenna) using novel air-bridge fabrication, other passive devices (couplers and power dividers and antenna) fabrication using deep SiO<sub>2</sub> etch process and metal contacts on a semiconductor substrate using AlGaN/GaN etch process. The processing techniques and equipment used for achieving this are detailed. All devices produced as part of this work, and shown in Chapters 3, 4 and 5, were made using these fabrication techniques.

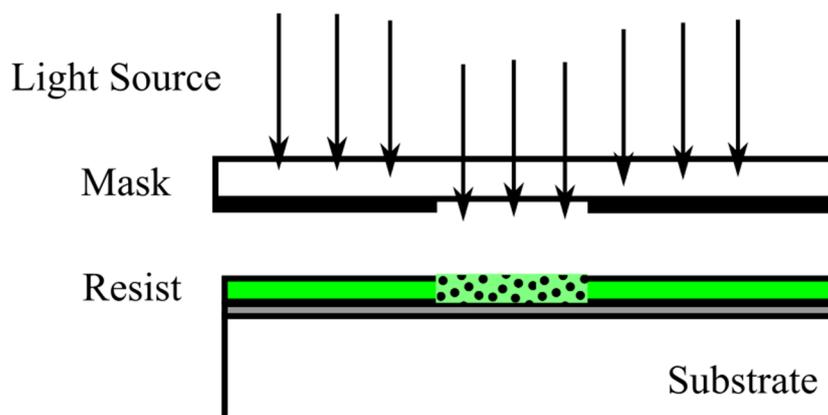
### 2.2 Lithography

Lithography is the process by which a pattern is generated and transferred into the surface of a substrate. The pattern transfer is often achieved either by optical or electron beam (e-beam) lithography, though other techniques also exist.

#### 2.2.1 Optical lithography

Optical lithography or photo-lithography transfers the pattern from a mask plate to the photo-sensitive resist, Fig. 2.1. Patterns used can be for etching, lift-off, or ion implantation process, as discussed later in this chapter. A condenser collects light from the light source and illuminates the mask pattern, passing through the imaging lens to expose the substrate surface. The weakened exposed pattern is selectively removed using a developer solution. Photo resist can be placed in two categories- positive or negative. Positive resist reacts to the light and exposed regions become soluble in the developer solution. The resulting pattern on the substrate is the same pattern as on the mask. Whereas, negative resist reacts to the light and the exposed region solidifies in the developer solution. The pattern on the substrate is

the inverse of the pattern on the mask. Energy ranging from visible to X-ray wavelength can be used when exposing the resist [2.1]. A Karl Suss Mask Aligner 6 (MA6) was used for all of the photo-lithography work performed. This tool can pattern a substrate size of 2" × 2" to 6" × 6" and accommodate a mask plate up to 7" × 7". It uses a UV light of 400 wavelength, supports i- and g- spectral lines (365 and 436 nm respectively) and has an exposure source at 350 watts.



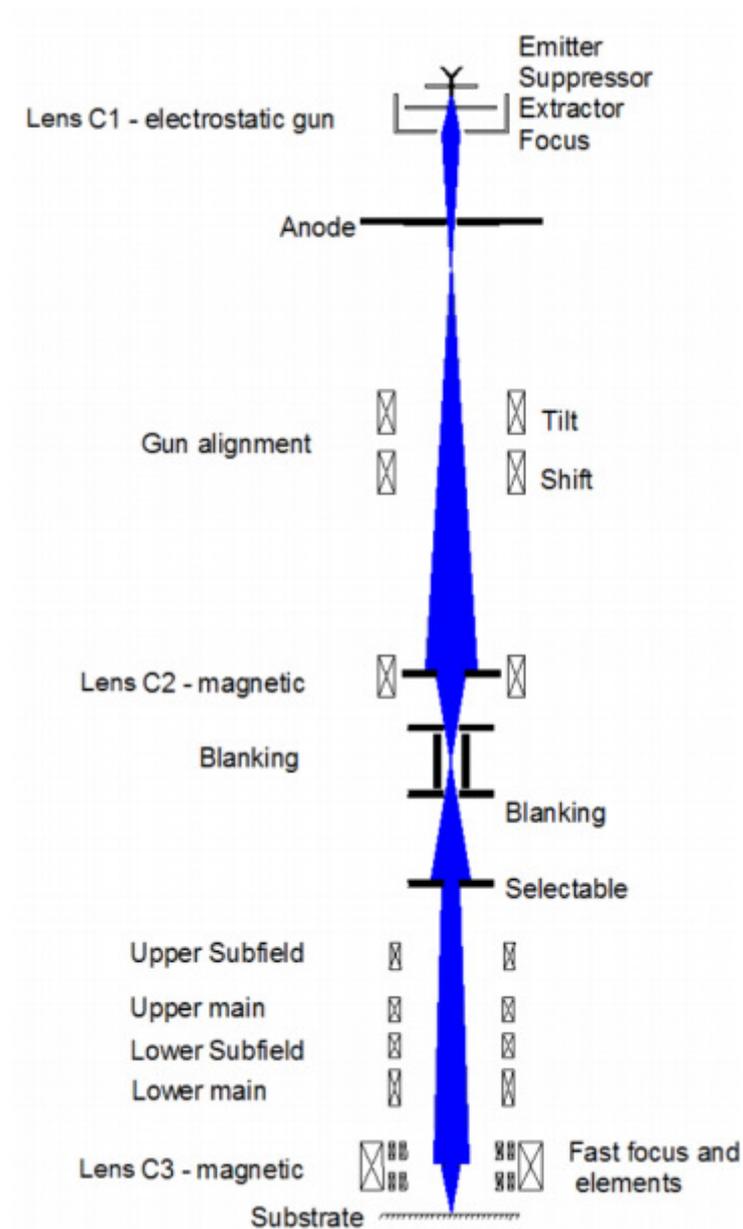
**Fig. 2.1:** Illustration of optical lithography.

### 2.2.2 E-beam lithography

E-beam lithography uses an electron sensitive resist to pattern the substrate. It is a particularly useful technique for patterning features sizes too small to be achieved using photo-lithography ( $< 1 \mu\text{m}$  structures). The e-beam lithography tool used in this work was a Vistec VB6 UHR EWF, the schematic is shown in Fig. 2.2.

There are a number of magnetic and electrostatic lens within the e-beam tool used to focus and confine the electron beam. The lens  $C_1$  is the electrostatic lens which is at the source. The beam is generated by a Schottky field emission gun made up of a tungsten cathode coated with zirconium oxide, heated up to 1800 K. Column height (HT) source biases the cathode at an accelerating voltage of about 100 kV. To ensure that electrons are emitted only from cathode tip, a suppressor electrode is used. The extractor electrodes create a high electric field between them and the cathode. This controls the thermal field emission and the electron acceleration to the extractor electrode. Then, the focus electrode is used to focus the beam before electrons reach the anode. To align the electrons at the anode, gun alignment coils are used which have a number of apertures at several positions in the column. These apertures reduce the deviation of the electron beam for generating spot-size. Further, magnetic lens  $C_2$  adjusts the spot size of beam without tampering with the focus and beam current. Magnetic lens  $C_3$  focuses the beam on the substrate at a given working distance. A

beam blanker is further used to deflect the beam into an aperture to scan x- and y-axes and it contains a number of magnetic coils. There are two deflectors which do this job. The main deflectors are used for large scale movement and subfield deflectors for fine control of the beam. If the feature size is greater than 1.3 mm in either the x or y direction, the sample stage moves as the maximum area covered by the deflector is 1.3 mm. The apertures in the system are used to adjust the beam size and current in the pattern writing process and the largest current and spot sizes are 131 nA and 45 nm, which can be written in short time. The smallest current and spot size are 1 nA and 4 nm, which is used for precision features.



**Fig. 2.2:** Schematic of an e-beam lithography tool [2.2].

## 2.3 Metallisation and lift-off

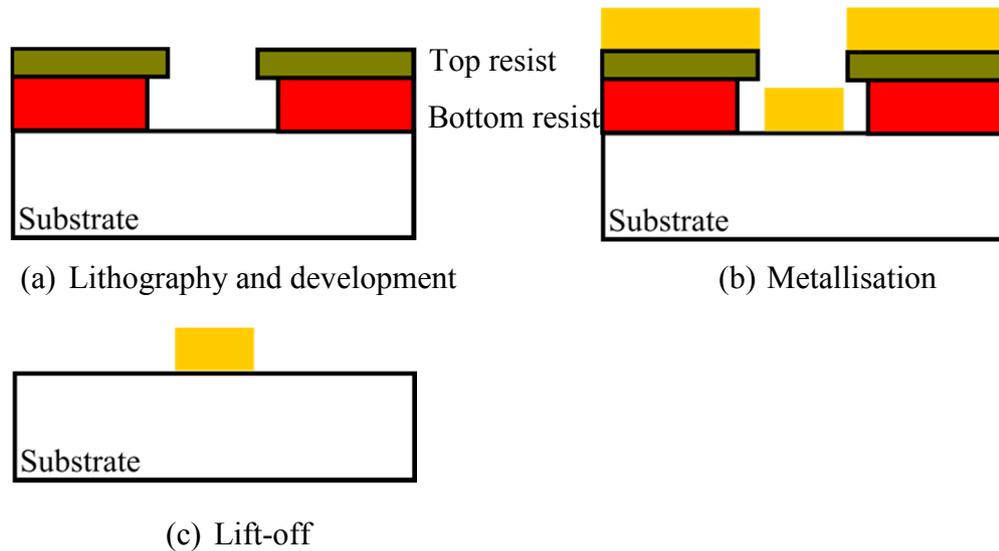
Metallisation is the process of depositing thin films of metal on a sample surface. The metal, for example, is used for establishing interconnections, antennas, ground planes, metal-semiconductor contacts, gate and bondpads or as an alignment marker for aligning to previous layers of lithography.

There are different techniques of metallisation, such as thermal and electron beam metallisation, sputtering and atomic layer deposition (ALD). In this work, most metallisation was carried out using electron beam evaporation tools manufactured by Plassys, models MEB 450 and MEB 550. Some work was carried out using sputtering. For e-beam evaporation, an electron beam is directed at the source material (target metal), causing localised heating of the materials surface which then evaporates onto the desired substrate. Deposition rate varies and is affected by chamber pressure, temperature and the atomic mass of the metal. The chamber where evaporation occurs has a pressure maintained in the order of  $10^{-6}$ - $10^{-7}$  Torr. For depositing multiple layers of material, evaporation takes place sequentially from multiple sources.

Alternative to evaporation, sputtering offers advantages in coverage and conformity. While evaporation is strictly a unidirectional deposition process, sputtering is not. In the case of producing a connection between different layers in a substrate, sputtering provides a better connection when the etched sidewalls are vertical. In this work, a Nordiko RF sputtering tool was used. The substrate is placed in a vacuum chamber with the target metal and an inert gas (argon and nitrogen) is introduced into the chamber at low pressure. The RF sputtering energises the insert gas in the vacuum chamber through changing electrical potential, which is now ionized. The metal is bombarded by these high energy ions, which sputters off metal atoms as a spray covering the substrate. In addition, both the substrate and target metal are placed close to each other in order to reduce the throw distance. Chamber pressure is in the order of 0.1 Torr and the particle energy and deposition rate depends strongly on voltage, substrate bias and pressure used. This is also a more cost-effective and practical means of depositing thicker metal films with good uniformity.

After patterning resist by a lithographic process, metal is often deposited onto the substrate to fill the pattern. The process of removing metal outside of the patterned area is known as lift-off, illustrated in Fig. 2.3. A bi-layer of resist with different sensitivities is used, which forms a tapered lift-off profile after development, e.g. there is a formation of undercut in the bottom resist profile. After metal deposition, the sample is submerged in a solvent to dissolve

the remaining resist, removing metal from the regions around the desired pattern. In this work, both photo-resist and e-beam resist were used for lift-off. The undercut profile helps the side walls of the resist to avoid being coated with metal that has continuity between the substrate metal and the sacrificial metal on top of the resist. This facilitates the lift-off process.



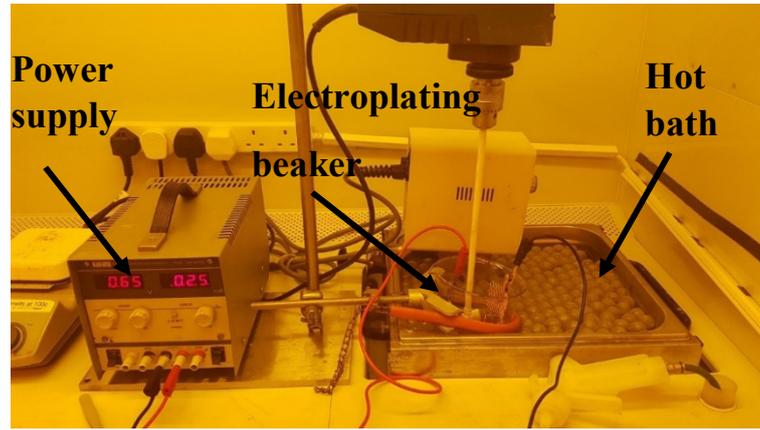
**Fig. 2.3:** Bi-layer lift-off Process.

After lift-off an ashing process is typically carried out in a low power oxygen plasma to remove any organic resist residues remaining on the sample surface, in the patterned area. Sometimes de-oxidation process is performed immediately after the ashing process. This removes any native oxide formed on the substrate surface in the exposed area by dipping the sample in a dilute acid solution (typically HCl) for a brief period and then rinsing with de-ionised water.

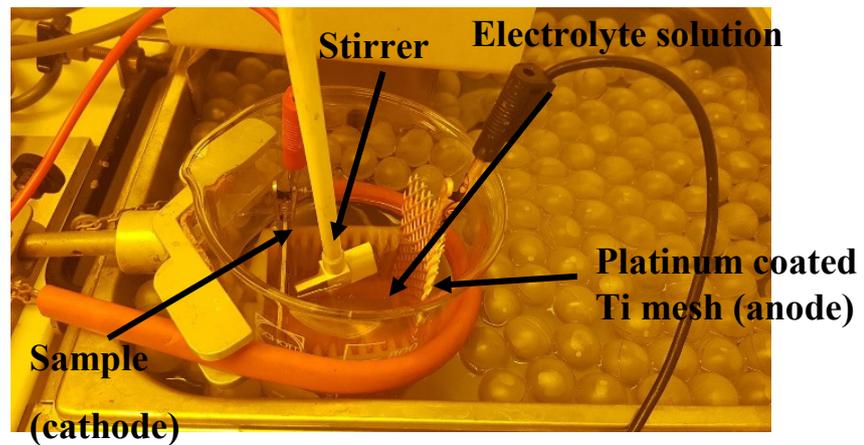
## 2.4 Electroplating

Electroplating is a process used for depositing metal, typically used to achieve thicker films. It involves passing current through a solution called an electrolyte and materials dipped into the solution behave as electrodes-anode electrode (usually same metal rod as electroplated metal) and cathode electrode (sample). These electrodes are connected to an external power supply or battery. When a direct current is applied to the anode, it oxidises the metal atoms and allows them to dissolve into the solution. At the cathode end, the dissolved metal ions in the solution are reduced at the interface between the solution and the cathode, and are plated out on the cathode. The rate at which the anode dissolves is the rate at which the cathode (sample) is being electroplated in addition to the current through the electrolyte solution. Metals which can be electroplated are gold, silver, tin, zinc, copper etc.

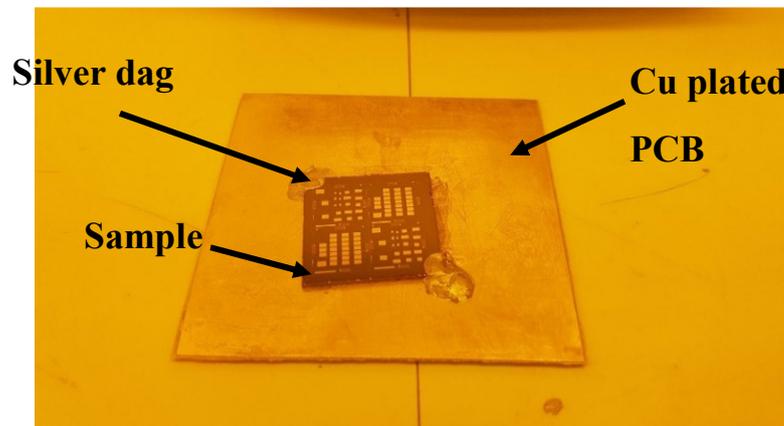
In this work, Au electroplating was used to deposit metal for bond pads and air-bridges of passive devices. Fig. 2.4 shows the operation of electroplating. For Au electroplating, Au electrolyte solution is used. This solution contains four different components, gold sulphite, sodium sulphite and tri-potassium citrate and arsenic. Two electrodes – platinized titanium as an anode and the sample as a cathode are used. Since the sample used was of size 1” inch, it was mounted on a 10 × 10 mm Cu plated PCB (printed circuit board) for better stability and uniform deposition. Wax was used to stick the sample on the PCB board and silver dag for establishing electrical conduction between them. A stirrer was used at 100 rpm to stir the solution for more uniform deposition of Au ions. The whole setup is immersed in a water bath maintained at 50<sup>0</sup> C.



(a)



(b)

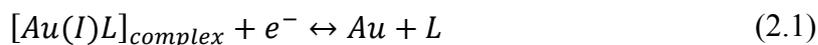


(c)

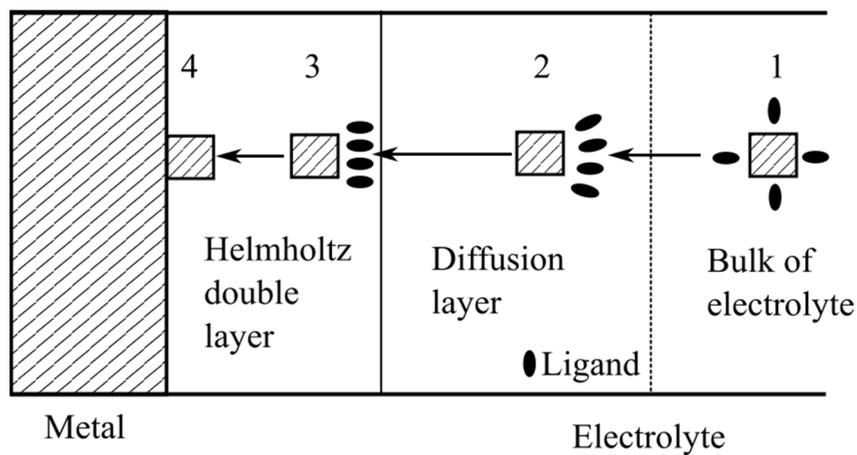
**Fig. 2.4:** Electroplating setup in JWNC (a) complete system (b) Electroplating beaker (c) sample preparation.

Since the anode here is non-soluble in electrolyte, plating salts must be added to the bath to replace the gold content [2.3]. Fig. 2.5 shows the process of electroplating using an electrolyte containing a complex metal ion. Within the Helmholtz double layer, the coordinated positive metal ions are attracted towards the cathode surface. In this region, we observe the distortion of ligands around the metals. At the cathode side, the negatively

charged complex ion becomes polarised by the electric field of cathode, which breaks up the ligand ions and the metal atoms are deposited on the cathode (sample). Equation (2.1) shows the principle reaction for gold electroplating [2.4]:



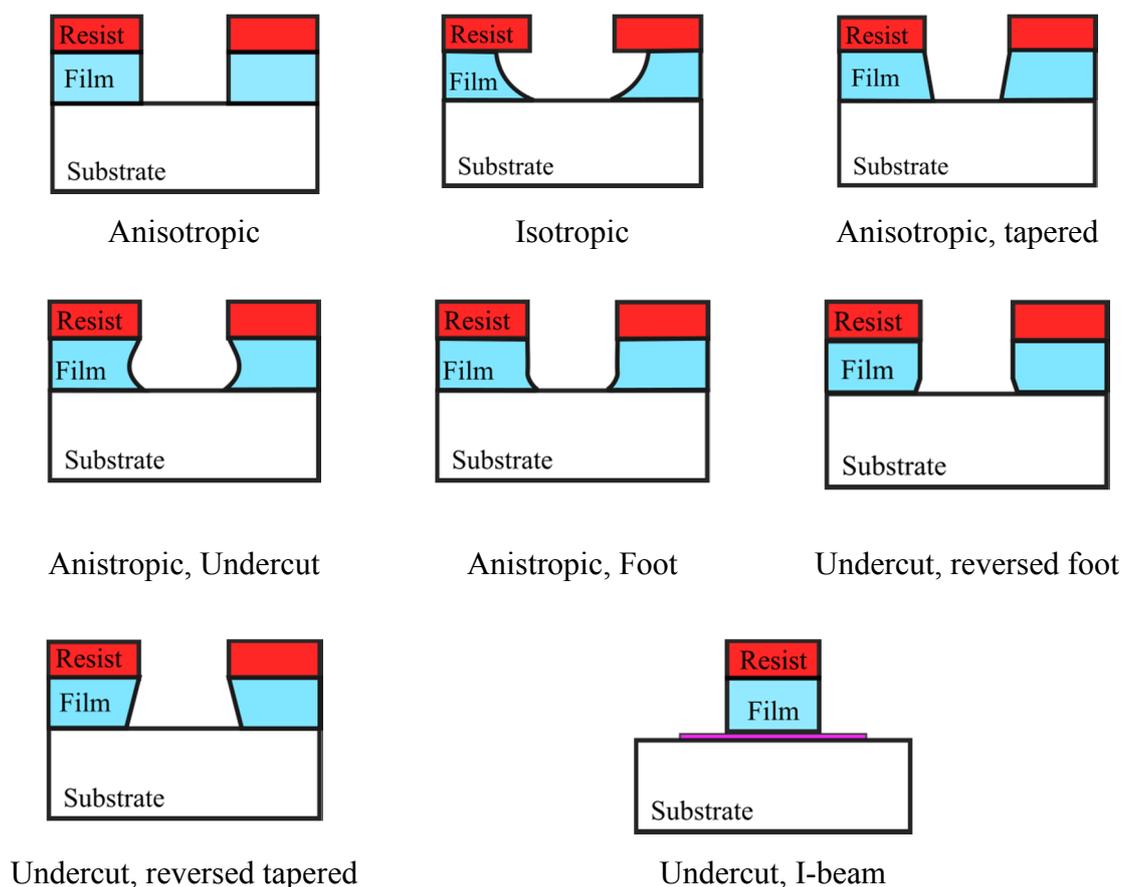
Where, [Au], [complex], and [Au (I) - complex] are the concentrations of gold ion, complex ion and gold complex in the solution.



**Fig. 2.5:** Schematic of gold deposition [2.4].

## 2.5 Etching

Etching is a process of (sometimes selectively) removing material e.g. substrate, dielectric or metals. If a mask is used, this often consists of resist/dielectric material (e.g. SiN or SiO<sub>2</sub>). Two main categories of etching are wet etching and dry etching. The etch creates a cavity, the depth of which is controlled by monitoring the etch rate and time. Etching can also be used without a mask to remove complete top layers of substrates. Often described as the selectivity of a particular etch recipe, this is the ratio of etch rate between the target etch material and other materials such as the mask. High selectivity means the mask is consumed at a much slower rate than the target material being etched. Some etching creates undercut below the masking layer, the distance of undercutting is called bias. Etchants with large bias are isotropic and etches which create sharp, well defined features are anisotropic. Fig. 2.6 shows an example of different etch profiles.



**Fig. 2.6:** Etch profiles [2.5] [2.6].

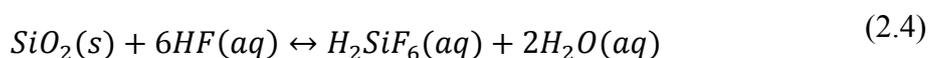
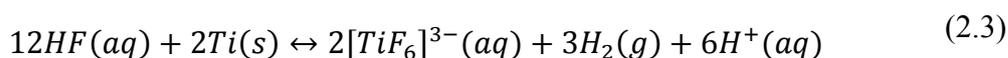
### 2.5.1 Wet etching

Wet etching involves the use of liquid chemicals to etch the target material. The etch rate and uniformity is affected by several factors, such as solution composition, pH value, concentration, temperature and time. Wet etching is a simple technique which often gives a high etch rate and high selectivity, but the etch itself is usually isotropic. This results in the etchant removing material underneath the mask and often requires an excessive amount of solution as the sample is typically immersed [2.7] [2.8].

In this work, wet etching was used for removing the seed layer of electroplating (Ti 50 nm/Au 50 nm). Au wet etching was carried out using a potassium iodide (KI) solution (KI+I<sub>2</sub>+H<sub>2</sub>O). Here, the gold patterning is through an iodide-iodide system. Gold reacts with iodine to form AuI (gold iodide), Equation (2.2) [2.9] and AuI solubility is improved by using KI in the solution. To etch 50 nm Au metal, it takes about 20 secs in this gold etchant solution.

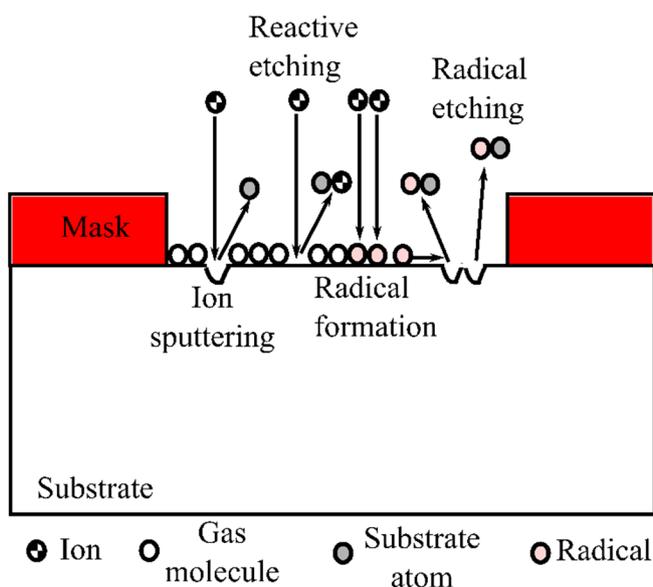


For removing Ti metal, buffered 10:1 HF (hydrofluoric acid) was used as a wet etchant. Equation (2.3) shows the chemical reaction of Ti with HF acid. This is the basic oxidation and reduction process, one reduction of hydrogen to molecular hydrogen and fluoride combines with the metal to form metallic fluoride [2.10]. It takes roughly 20 secs to etch 50 nm of Ti using this solution. HF also etches SiO<sub>2</sub>, Equation (2.4) [2.10] shows the chemical reaction for this.



## 2.5.2 Dry etching

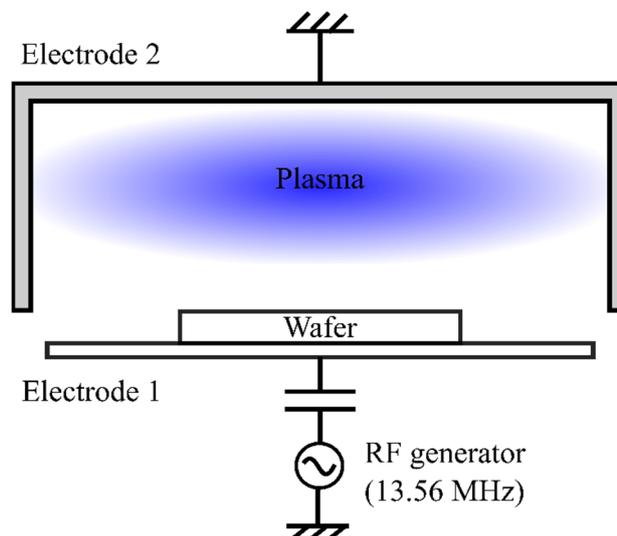
Dry etching (plasma etching) uses plasma or etchant gases to remove the target material. Plasma is an ionized gas, which has enough energy to free electrons from the atoms or molecules of a material and allows both ions and electrons to coexist. Fig. 2.7 shows the role of ions in dry etching. Dry etching is often used over wet etching when high aspect ratio features and precise etching is required. There are three types of dry etching: chemical reaction, physical removal and a combination of physical and chemical removal. Dry etching produces gaseous products which are combined into a large stable gas and is ejected through a vacuum system. Parameters affecting dry etch are etching gas composition, chamber pressure, gas ratio, power levels and temperature of the sample being etched [2.7] [2.11]. Dry etch can be both anisotropic and isotropic depending on the recipe and gas chemistry used. In this work, an Oxford Instruments Plasmalab System 100 RIE and SPTS' Omega® Synapse (APS) system were used for etching AlGaIn/GaN surfaces and 10  $\mu\text{m}$  SiO<sub>2</sub>.



**Fig. 2.7:** Role of ions in plasma dry etching [2.8] [2.12].

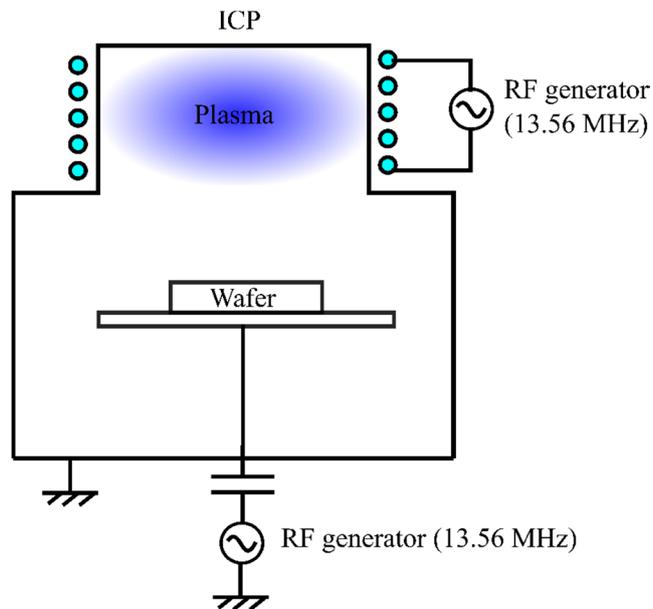
Reactive-ion etching (RIE) uses chemical etching with ion bombardment to remove material. When gases are introduced into the chamber, they are ionised with an RF powered field. The reactive species (ions and electrons) created by the plasma react chemically with the material being etched. In each cycle of the field, the electrons electrically accelerate up and down in the chamber, gets absorbed by the chamber and are also deposited on the sample surface. The stage is electrically isolated from the rest of the chamber, which causes the accelerations of ions towards the stage. Fig. 2.8 shows the diagram of the common RIE setup. The energy released when ions reach the surface greatly enhances the efficiency of the chemical reaction and gives direction to the etching. An important parameter in this process is the generation

of the plasma and the DC bias. Plasma is generated using two parallel plates, which has an advantage depending on the material and since DC bias is applied to the substrate, there is a physical etching aspect to the process. Some materials, like SiO<sub>2</sub>, require higher activation energies compared to Si.



**Fig. 2.8:** Diagram of Reactive Ion etching setup [2.8].

An ICP is a type of plasma source, where energy is generated with a RF powered magnetic field (electromagnetic induction). Fig. 2.9 shows the ICP reactor using planar coil. Here, an RF voltage is applied to the coil, which is on the either side of the dielectric. This coil generates alternating magnetic field and induces RF electric field using Faraday's law. The induced electric field energises electrons in the plasma at low pressure. It's also possible to apply RF bias to the sample holder to control the ion bombardment from the ICP. This gives separate control of plasma density, ion energy, greater process flexibility and profile control, and reduced damage of the sample. As a result, an ICP system can produce very high plasma density ( $>5 \times 10^{11} \text{ cm}^{-3}$ ) compared to conventional RIE ( $10^8\text{-}10^{10} \text{ cm}^{-3}$ ), while maintaining low ion bombardment energy [2.8].



**Fig. 2.9:** Inductive coupled plasma using planar coil [2.13].

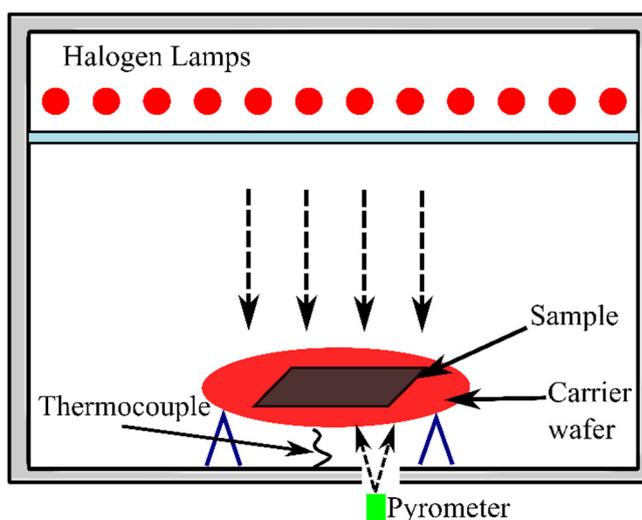
SPTS' Omega® Synapse (APS) system is an ICP-based high density plasma source, designed to etch materials which were difficult to etch using RIE or conventional ICP sources. In high density plasma, ICP is coupled to the sample through CCP (charge coupled plasma) action. Further, there is a multipole magnetic bucket to reduce the electron and ion losses to the chamber, which is heated to additionally reduce radical loss, Fig. 2.10. It is a widely used technique to deliver high etch rates, high selectivity, good directionality and low damage processing. Excellent profiles can also be achieved, as the plasma is maintained at low temperatures [2.14].



**Fig. 2.10:** SPTS APS module [2.15] [2.16] Copyright © 2012, SPTS Technologies.

## 2.6 Rapid Thermal Annealing

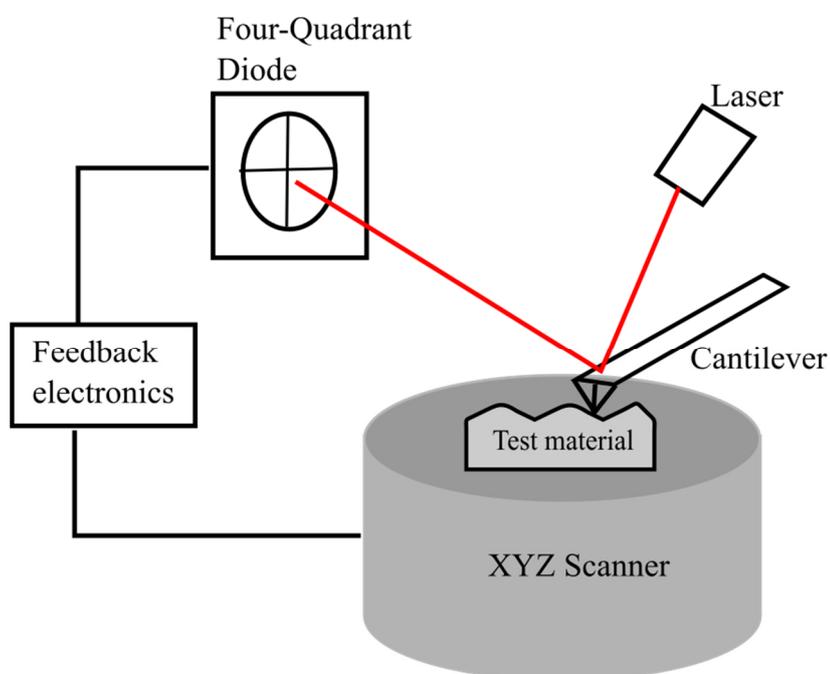
Rapid Thermal Annealing (RTA), as the name suggests, is a process by which a sample can be annealed at relatively high temperatures over a short period of time. As such, this involves the capability to rapidly ramp temperature in a controlled environment. This process is often used in the semiconductor industry for the activation of dopants and for the interfacial reaction of the metal contacts. The operation involves rapidly heating a sample from ambient temperature to around 800-1500 K, along with rapid cooling. As soon the wafer reaches this temperature, it is often seized here for a matter of seconds and then reduced. In this work, a Jipelec JETFIRST RTA system was used. The sample is heated using a halogen lamp with temperature monitored using a pyrometer and thermocouple, Fig. 2.11. RTA can also be used for oxidation, silicide formation and chemical vapour deposition. This can be combined with gases ( $N_2$  or  $O_2$ ) to control the chamber environment. RTA can also be programmed for multi-stage annealing. In this work, RTA was used to anneal metal-semiconductor contacts at elevated temperatures to achieve lower contact resistance on GaN-on-LR Si (Chapter 6).



**Fig. 2.11:** Diagram of RTA chamber [2.17].

## 2.7 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a technique used to measure surface details of a material (contours of the surface, roughness, film thickness etc.) on a sub-nanometre scale at extremely high resolutions. The basic principle of AFM involves a probe kept in close contact with the sample surface with a feedback mechanism as it scans along the surface, carefully maintaining the force between the probe and surface at a low level. The probe is often made of silicon or silicon nitride on the end of a cantilever with a sharp integrated tip and a radius that varies from 5 to 20 nm. The deflection of the cantilever, due to the forces acting on the tip, is measured by a laser focused on the back of the cantilever. This laser is reflected onto a photodiode array and the movement of the laser spot on the photodiode gives precise measurement of the deflection of the probe. This arrangement is known as an optical lever. The deflections of cantilever are sensitive to Angstrom-level movements. There are three types of scanning – contact mode, tapping mode and noncontact mode. In this work, contact mode was used primarily, where the probe remains in contact with the sample as it moves along the surface and this movement is controlled by a XYZ scanner. The surface of the scanner is made of a piezoelectric material, which helps to move probe accurately in all the axes. Since the cantilever acts as a spring, the change in deflection is equal to the sample topography. Fig. 2.12 shows the schematic of the AFM operation.



**Fig. 2.12:** Schematic of AFM operation.

In this work, AFM was used to study the roughness of annealed ohmic metal surfaces and for measuring the etch depth of the AlGaIn/GaN material (Chapter 5). The two main parameters used in AFM for analysing the surface roughness are average roughness ( $R_a$ ), root mean square roughness ( $R_q$ ).

The average roughness ( $R_a$ ) is the arithmetic mean of the absolute values of  $Z(x)$  in a sampling length. The average roughness is described as follows [2.18]:

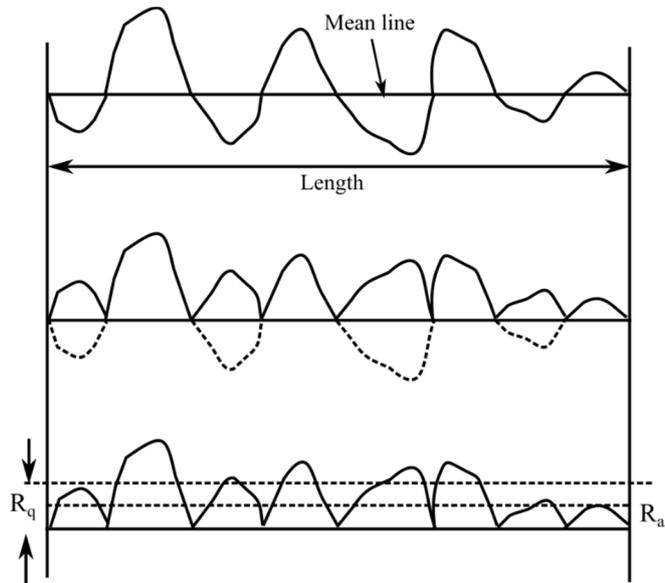
$$R_a = \frac{1}{L} \int_0^L |Z(x)| dx \quad (2.5)$$

Where,  $Z(x)$  is the surface profile value studied in terms of height ( $Z$ ) and position of sample ( $x$ ) over the scanned length ( $L$ ). This is also called as Centre Line Average (CLA) or Arithmetic Average (AA) or Arithmetic Mean Deviation of the profile. A disadvantage of this parameter is, it does not differentiate between peaks and valleys, being the mean absolute profile. As such, it is less useful for differentiating the shape of a surface between samples with similar average roughness.

The root mean square roughness (RMS) is the root mean square of  $Z(x)$  in a sampling length. This is the same as average roughness, except there is mean squared absolute values of the surface roughness profile. The function  $R_q$  is defined as [2.18]:

$$R_q = \sqrt{\frac{1}{L} \int_0^L |Z^2(x)| dx} \quad (2.6)$$

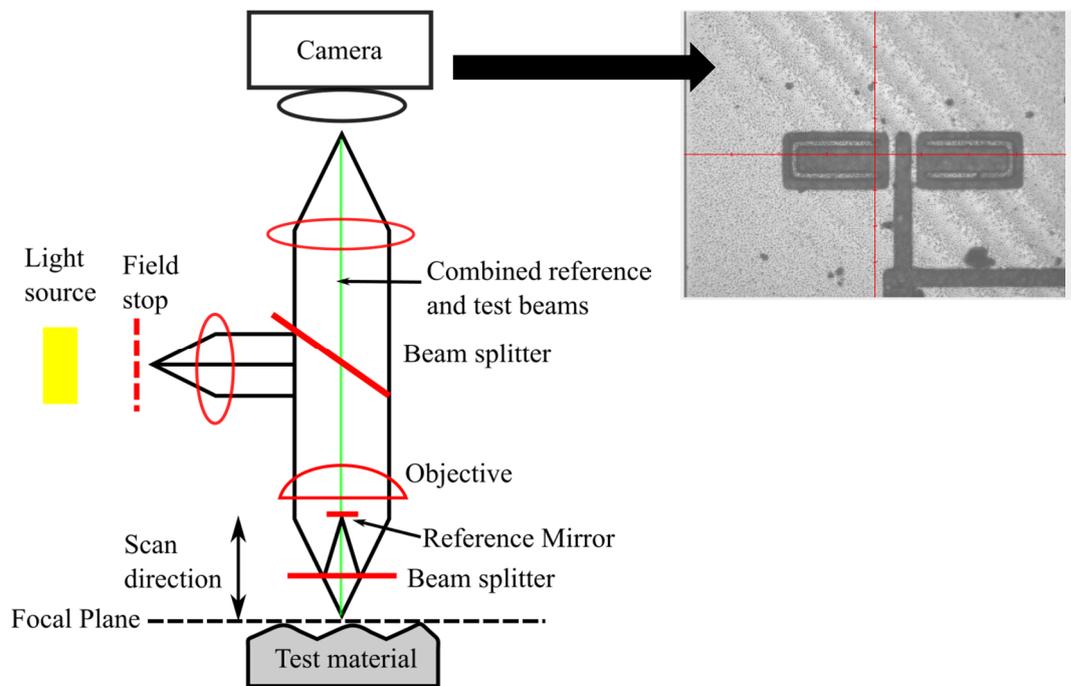
This  $R_q$  is more sensitive to peaks and valleys than the average roughness as the squaring of the amplitude is included in the calculation. Fig. 2.13 shows the graphical representation of both  $R_a$  and  $R_q$ . In this work,  $R_q$  was used analyse the surface roughness of the annealed contact metals and for measuring the etch depth of AlGaIn/GaN material.



**Fig. 2.13:** Graphical derivation of  $R_a$  and  $R_q$  [2.19].

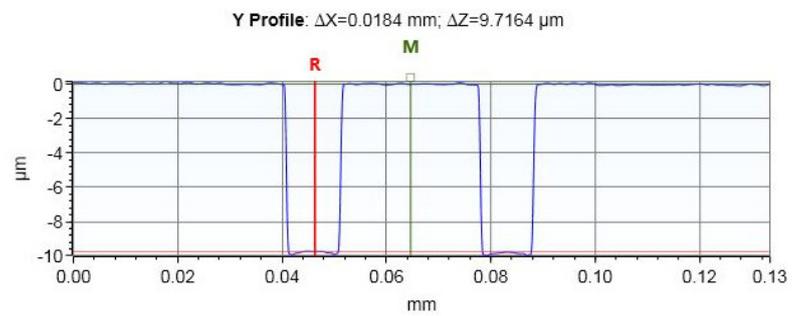
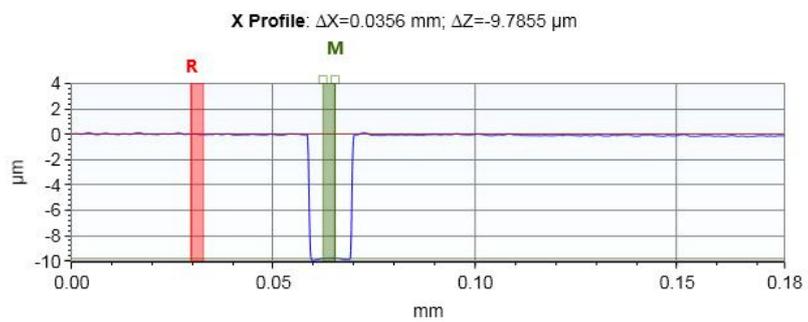
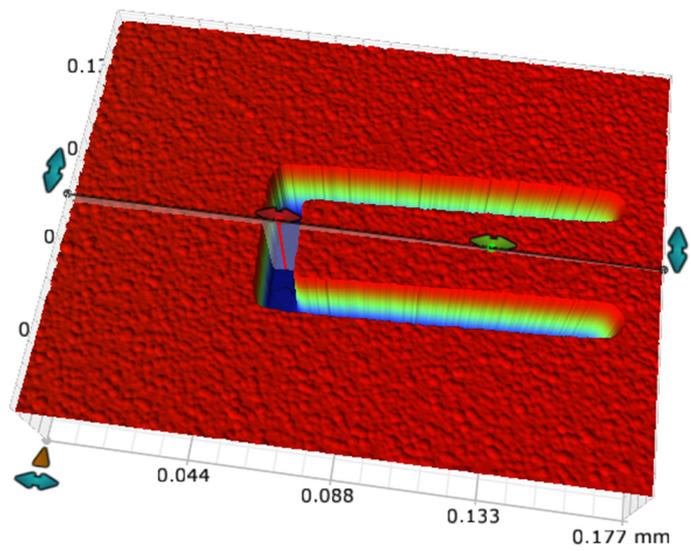
## 2.8 Optical Profilometer

The ContourGT™-X is an optical surface-profiling system used in this work. It measures surface topography of a material using light with high accuracy from the range of a few nm to 10 mm. It can be used to measure particularly deep and narrow features, difficult to measure with AFM due to the limiting dimensions of the probe. Fig. 2.14 shows the schematic of the optical profilometer.



**Fig. 2.14:** Schematic of optical profilometer [2.20].

An optical profiler uses the light wave properties to compare the optical path difference between a test surface and a reference surface. The light beam (mainly white light) is split using a beam splitter, one half the beam is reflected from the test surface passed through a microscope and the other half reflects from the reference mirror. When the distance of the beam splitter from reference mirror is same as the beam splitter distance from the test surface and when these split beams are recombined, constructive and destructive interference occurs in the combined beam when the length of light beams vary. This creates light and dark bands known as interference fringes. Since the reference mirror is close to flat, any difference in height comes from the roughness of the test surface. The interference beam is then sent to a digital camera, where constructive interference areas are lighter and destructive interference areas are darker. In interference, each change from light to dark field is half a wavelength and if the wavelength of the light source is known, calculation of height difference across the surface is fractions of a wave. From these height differences, a surface measurement or 3D surface map can be obtained [2.20]. Fig. 2.15 shows measurement of SiO<sub>2</sub> etch depth from the optical profiler. For this measurement, etch depth was equal to 9.7 μm.



**Fig. 2.15:** 3D image from optical profilometer for measuring etch depth of SiO<sub>2</sub>.

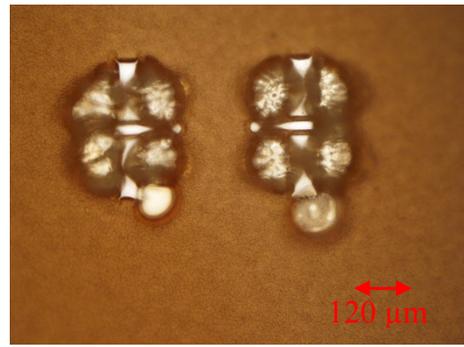
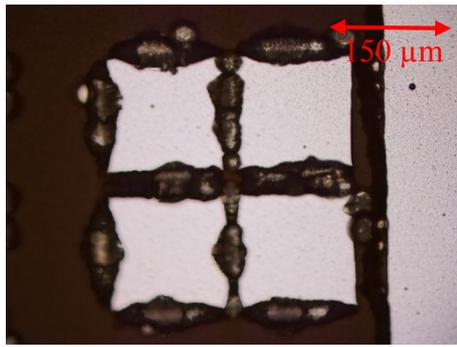
## 2.9 SPTS deep SiO<sub>2</sub> etch fabrication

A SPTS' Omega® Synapse (APS) was used for etching 10 µm SiO<sub>2</sub> dielectric. Due to a high source power (2000 W) and platen power (600 W), this tool is capable of relatively high etch rates compared to other systems. Table 2.1 shows the parameters used for etching SiO<sub>2</sub>. Due to the aggressive parameters being used, the mask material must have the ability to sustain this high-power process. The stage temperature for this process was maintained at -10<sup>0</sup> C to reduce isotropic effects, resulting in a more vertical etch profile. Samples were mounted on a 6-inch Si wafer with a material called cool-grease, which improves the thermal contact between the sample and carrier. The carrier wafer is gripped to a chunk electrostatically and keeps the wafer at constant temperature using Helium back-cooling.

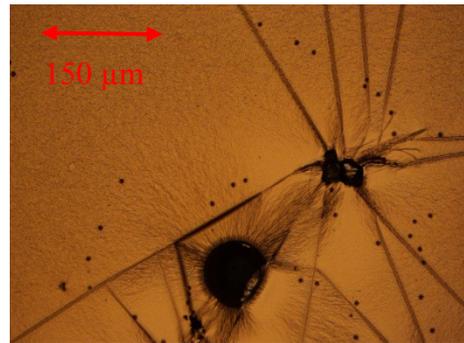
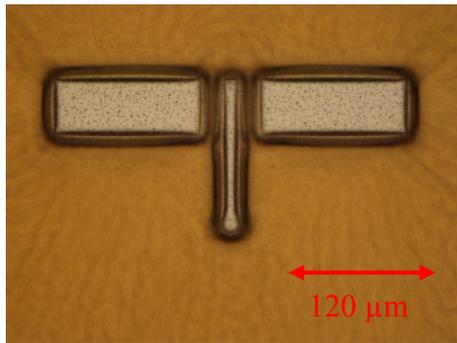
Parameters	Values
Pressure (mTorr)	5
Source power (W)	2000
Platen HF power (W)	600
C <sub>4</sub> F <sub>8</sub> (sccm)	15
CF <sub>4</sub> (sccm)	5
He (sccm)	50
He back-cooling (Torr)	15
Temperature (°C)	-10

**Table 2.1:** Parameters for SPTS deep SiO<sub>2</sub> etching.

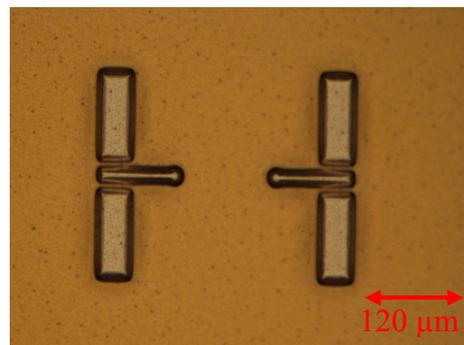
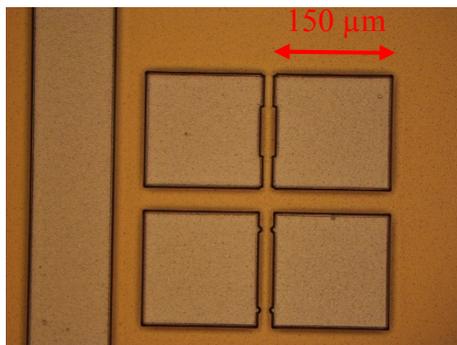
Optical resist AZ4562 was used as an etch mask. Fig. 2.16 (a) shows a sample where AZ was used as a bi-layer with the 1<sup>st</sup> layer baked for 15 mins at 90<sup>0</sup> C and the 2<sup>nd</sup> layer for an hour at 90<sup>0</sup> C. The resist was spun at 4000 rpm. Total resist thickness achieved was 12 µm. After 20 mins of etching, using the above recipe, the resist mask appeared burnt. This is possibly due to the resist not being completely cured or poor thermal exchange between the sample and carrier. Fig. 2.16 (b) shows the AZ bi-layer pre-baked and spun at same time as before and post-baked overnight. After etching for 20 minutes, the resist appeared wrinkled and at the edges of the sample it had fractured. Since a bi-layer was used both times, an etch depth of only 5 µm was achieved, the reason being the aspect ratio (etch depth to etch opening) of 3.14. Here, the etchants have more difficulty passing through the smaller holes and diffusing out etch by-products. Finally, a single layer of AZ4562 resist spun at 4000 rpm (6 µm) was pre-baked for 1 hour and post-baked for 4 hours and showed a more promising result, Fig. 2.16 (c).



(a)



(b)

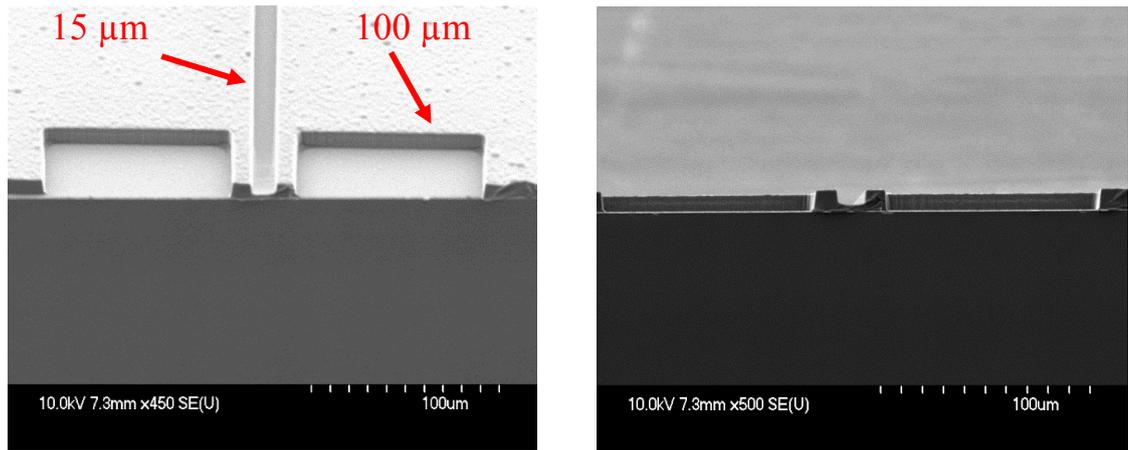


(c)

**Fig. 2.16:** Resist after etching for different post bake time (a) bi-layer resist-Zero post baking (b) bi-layer resist-overnight post baking (c) single layer resist-4 hours post baking.

Another issue that arose when using the SPTS etching tool was micro-loading. Micro-loading is a dry etch effect where smaller features have a lower etch rate compared to larger features. This effect is common for all dry-etch machines and it is suggested to increase etch time 5 to 10 % to compensate for smaller features. However, due to the faster etch rates of the SPTS micro-loading is a particular issue. A combination of feature sizes from 11 μm, 19 μm, and 100 μm can have a huge etch time difference. A 100 μm feature was etched for 5 mins, exposing Al metal underneath. Meanwhile, other smaller features did not reach the Al underlayer, Fig. 2.17. As a result, the size of alignment markers used in this work were made

at 15  $\mu\text{m}$ , which is closer in size to other smaller features that would be needed. Fig. 2.18 shows the difference between small and large features for the same etch time when the bigger features (100  $\mu\text{m}$ ) were removed. As mentioned previously, temperature of the sample can also have a large impact on the etch process. Here, after etching the sample for 5 mins, a 3<sup>o</sup> C change in temperature was observed. In order to maintain a stable temperature of -10<sup>o</sup> C, the etch process was performed in cycles with rest periods of 5 minutes between etches. Final etch rate was optimised to be 0.35  $\mu\text{m}/\text{min}$ .

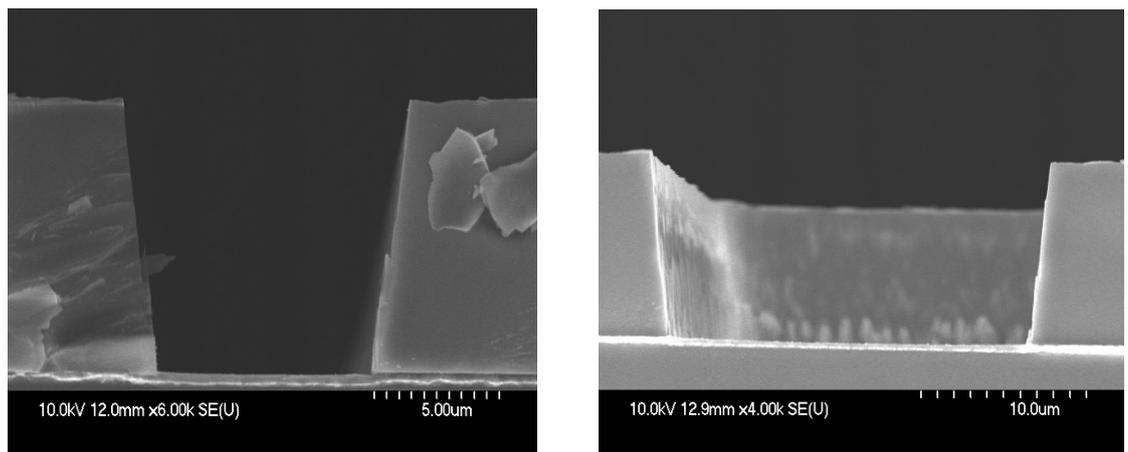


(a)

(b)

**Fig. 2.17:** SEM image of micro loading effect between 15  $\mu\text{m}$  and 100  $\mu\text{m}$  feature size

(a) Top view (b) Side view.



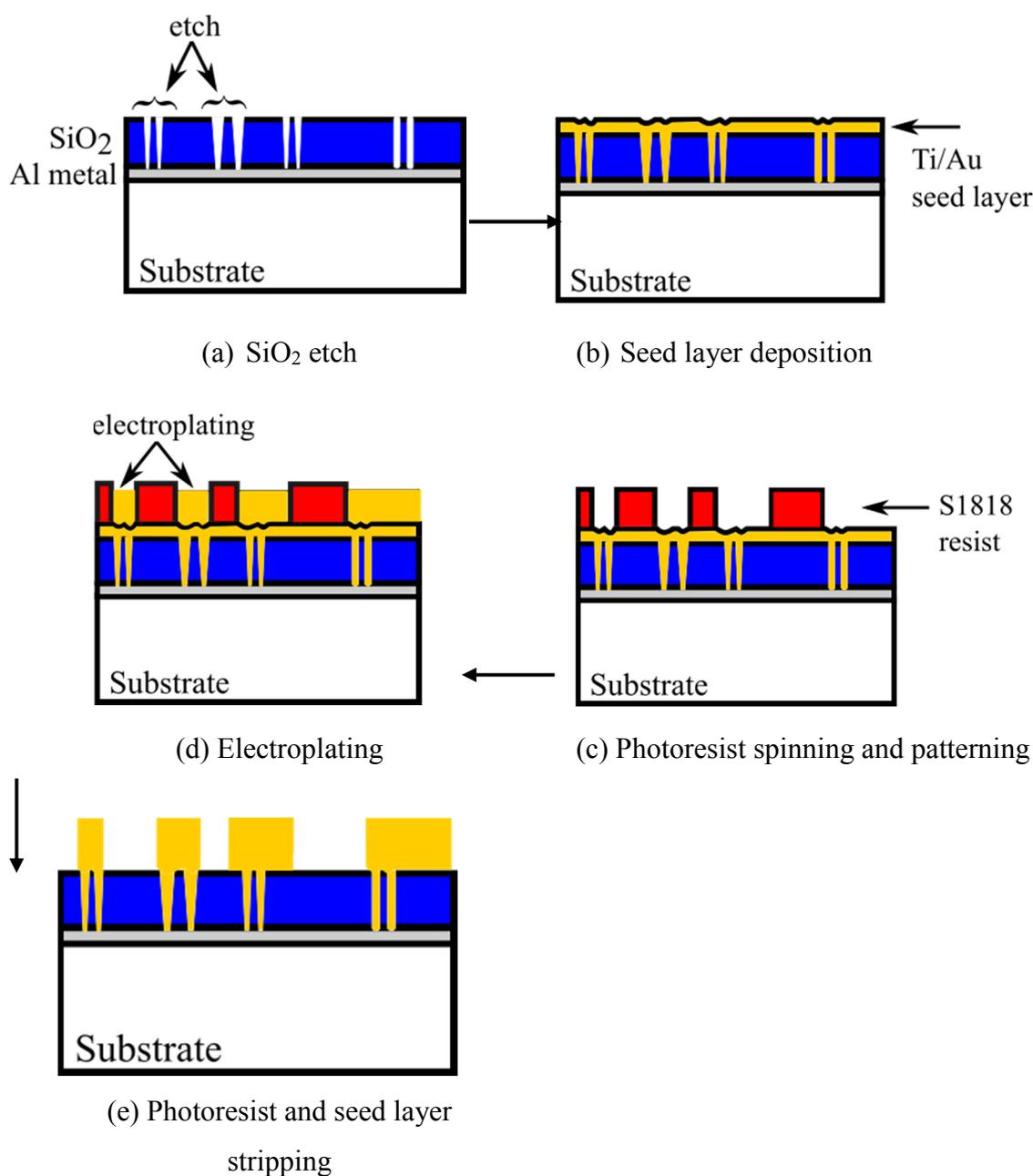
(a)

(b)

**Fig. 2.18:** SEM image of no micro loading effect when bigger features were removed for same etch time (a) 11  $\mu\text{m}$  feature size (b) 25  $\mu\text{m}$  feature size.

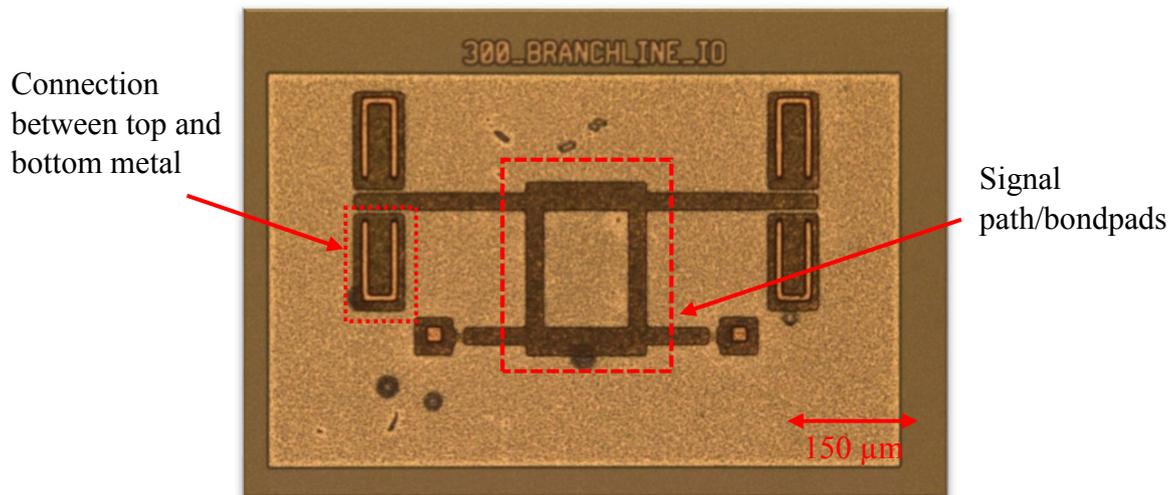
## 2.10 Bondpad and Air-bridge fabrication

Illustration of bondpad fabrication for connecting signal to ground is as shown in the Fig. 2.19. Due to the required thickness of metal, electroplating was used. A seed layer of Ti/Au (50/50 nm) was first deposited using a Plassys e-beam evaporator. Then, using photo-resist S1818, the bondpads were patterned. Here, S1818 was spun at 3000 rpm at 30 seconds and baked using a hotplate at 115<sup>o</sup> C for 3 mins. The delicate part in this process was to develop the correct resist exposure and development time. The SiO<sub>2</sub> dielectric is then dry etched, prior to the electroplating process.

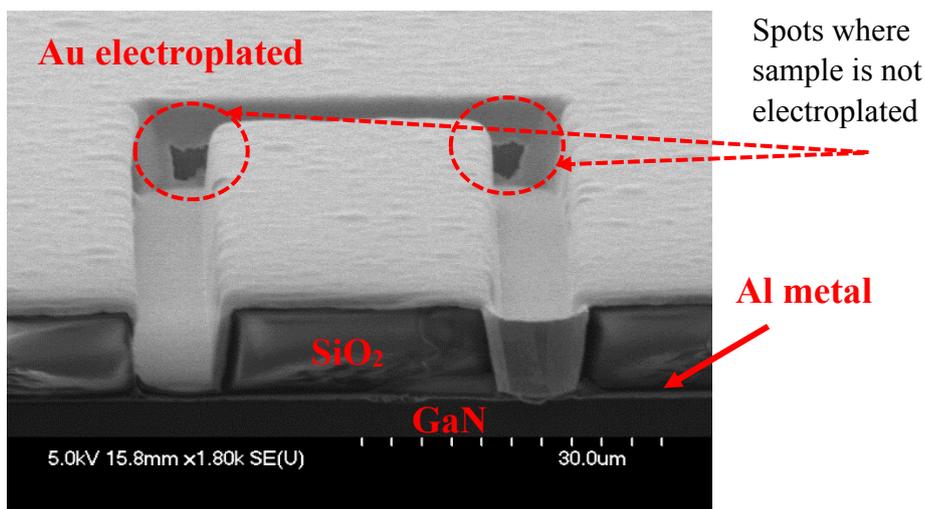


**Fig. 2.19:** Fabrication steps carried out for bondpads.

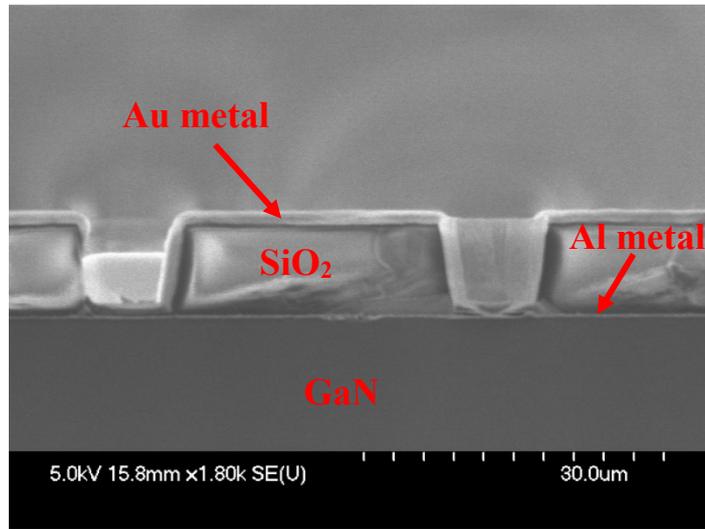
This process connects ground metal to the top metal and establishes the signal path at the top of the dielectric, Fig. 2.20. As a result, it was necessary to clear the photoresist from the bottom metal as well as not to short the top signal line (smallest gap was 7  $\mu\text{m}$ ). Since the bondpads were electroplated, the smallest gap between signal lines was designed to be greater than 3  $\mu\text{m}$  to avoid shorts between lines due to gold ion build up. Resist exposure time was 28 secs and development time was 4 mins. Samples were then plasma ashed for 4 mins and electroplated (Au) for 15 mins to achieve 2  $\mu\text{m}$  thick Au, Fig. 2.21.



**Fig. 2.20:** Branch line coupler circuit (Chapter 4).



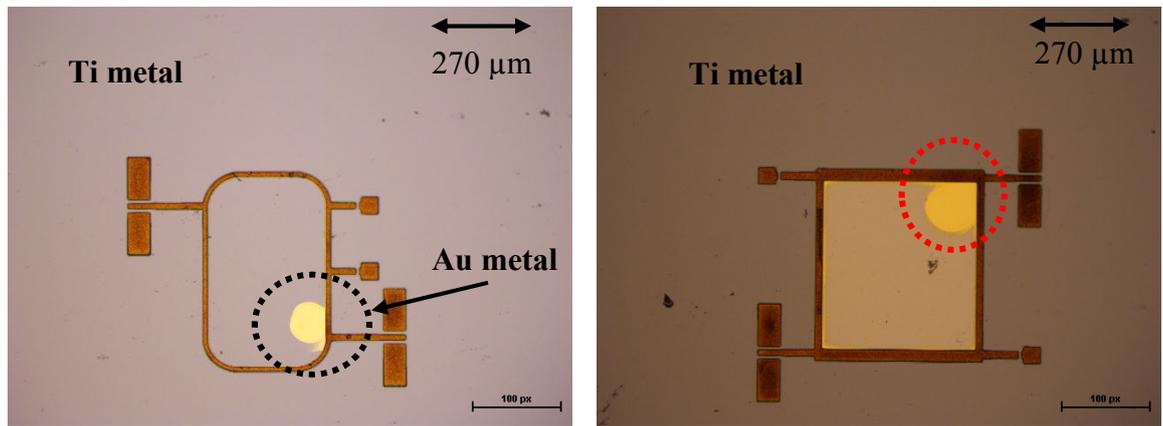
(a)



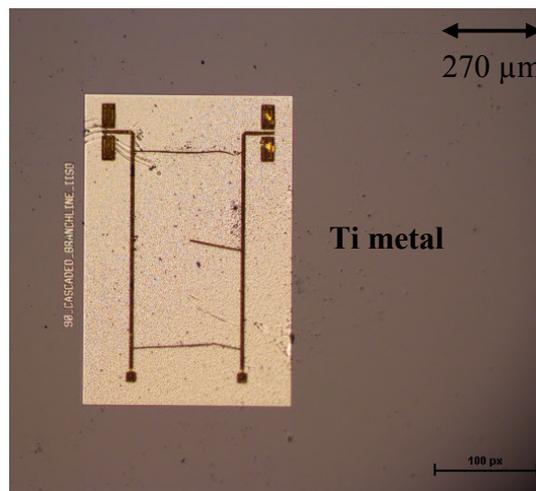
(b)

**Fig. 2.21:** SEM image of bondpads electroplated (a) Top view (b) Cross-sectional view.

Before proceeding to the next lithography step, S1818 resist was removed using acetone, kept at 50<sup>0</sup> C in a hot bath overnight, and the seed layer was removed using wet etchant solutions. The sample was blanked etch to remove Au and Ti using Au etchant (KI solution) and 10:1 buffered HF solution respectively. After exposing the sample to Au etchant for 20 secs, some samples, especially near the bend of signal lines, were observed to have Au which had not etched, Fig. 2.22 (a). Additional exposure time in the wet etch solution could remove these features, yet would result in etching of the metal lines, Fig. 2.22 (b). This extra gold near the bends of signal lines affects the performance of the overall circuit.



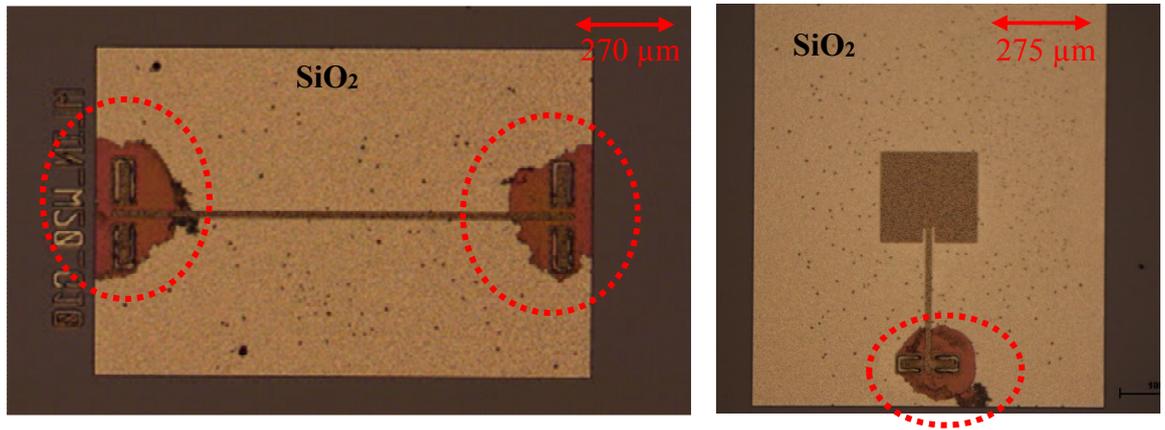
(a)



(b)

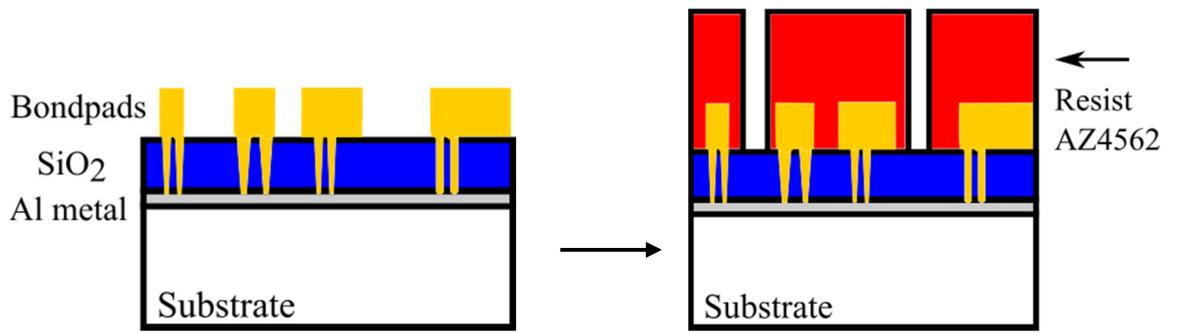
**Fig. 2.22:** (a) Incomplete Au etching (b) Bondpads etched away after excess Au etching.

As such, etch sidewall which has not been successfully electroplated will have exposed  $\text{SiO}_2$ , Fig. 2.21 (a) and Fig. 2.23, which buffered HF etches Other areas (top surface of  $\text{SiO}_2$ ) are initially protected by Ti, however once it is removed the  $\text{SiO}_2$  will be etched if the sample is exposed longer in buffered HF solution. For these reasons, a negative AZ2070 resist was used instead to protect the top metal lines during wet etching. AZ2070 uses the same process step as positive AZ4562 but with an additional bake after exposure, turning the resist negative.



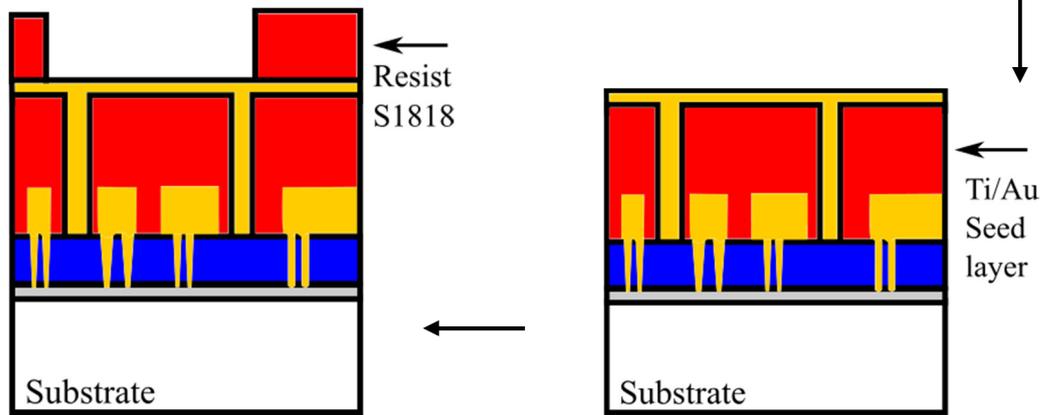
**Fig. 2.23:** Example of where HF etched SiO<sub>2</sub> in the non-electroplated regions.

The next process after depositing bondpads was to create an airbridge. Fig. 2.24 shows an illustration of the airbridge process. Initially, AZ4562 photo-resist was spun at 4000 rpm for 30 secs as a support mask and baked at 90<sup>0</sup> C for 30 secs. Next, a seed layer was deposited Ti/Au (50/ 50 nm) using an e-beam evaporator. For the track layer, photo-resist S1818 was spun at 3000 rpm for 30 secs and baked at 90<sup>0</sup> C for 15 mins. Finally, the sample was ashed and the track layer was Au electroplated for 15 mins to achieve a final thickness of 2 μm. Fig. 2.25 shows the Optical and FEI image of the elevated circular antenna (Chapter 3).



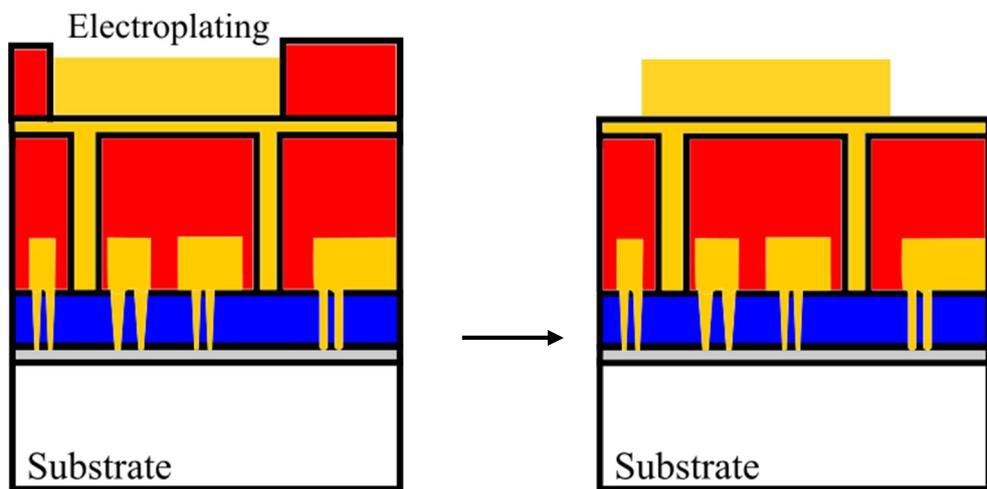
(a) Electroplated bondpads

(b) Photo-resist spinning and patterning for air bridge support



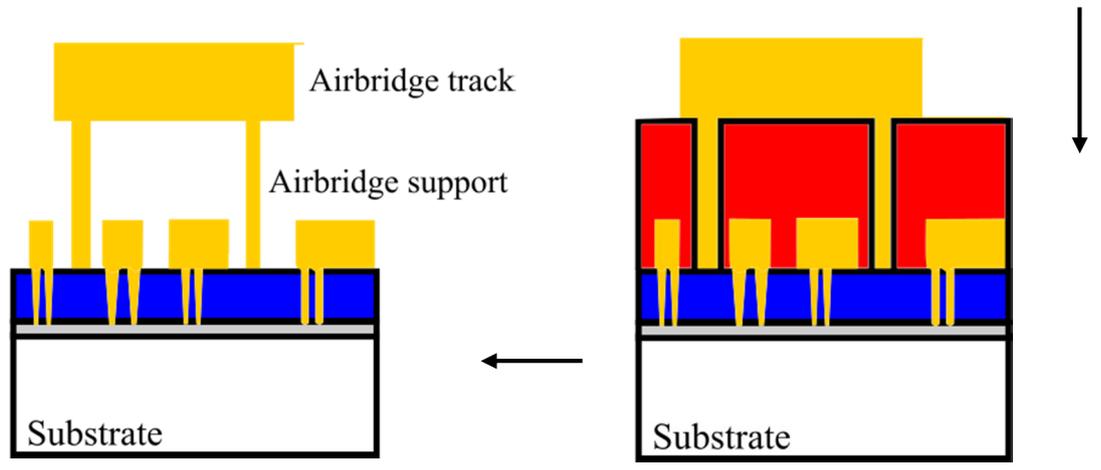
(d) Photo-resist spinning and patterning for air bridge track

(c) Seed layer deposition



(e) Electroplating

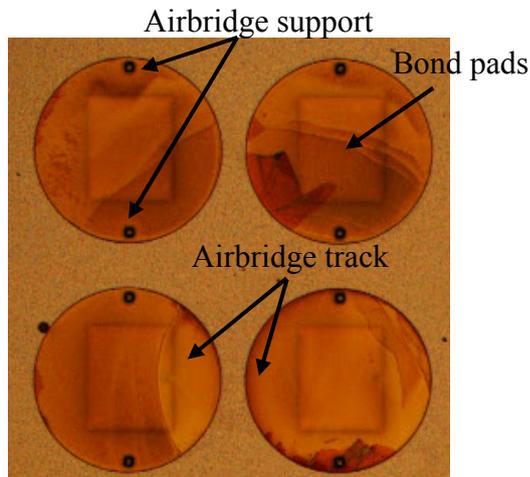
(f) Top layer photo-resist stripping using flood exposure



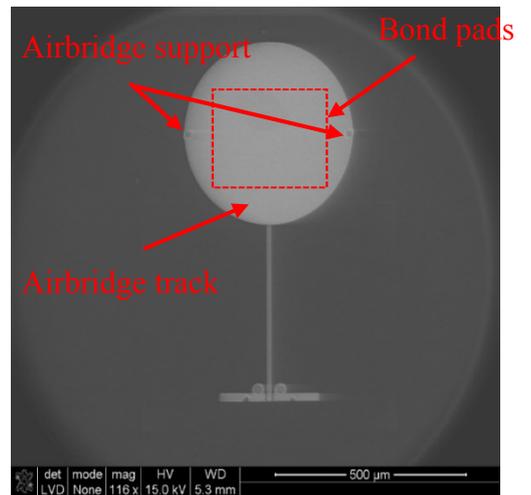
(h) Bottom layer photoresist stripping using flood exposure

(g) Seed layer stripping using wet etching

**Fig. 2.24:** Fabrication steps carried out for air-bridge process.



(a)



(b)

**Fig. 2.25:** Image of air-bridge (a) Optical (b) FEI.

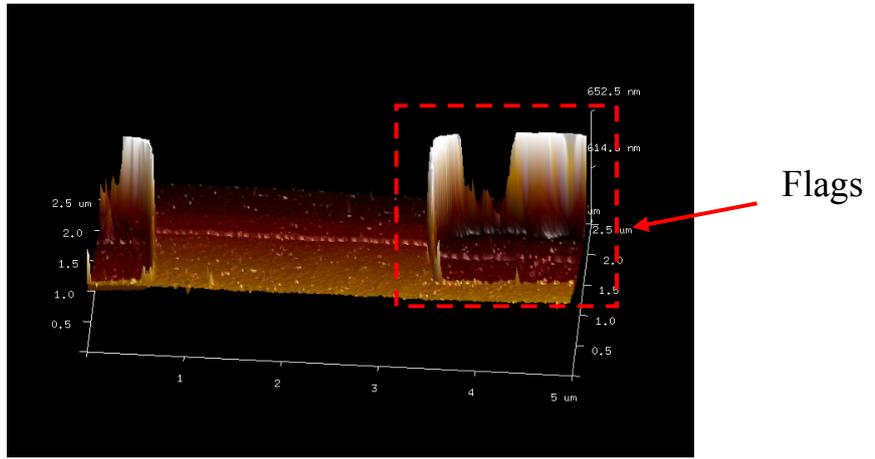
## 2.11 Etching of AlGaIn/GaN using PMMA as etch mask

In this work, AlGaIn/GaN layers were etched using an Oxford PlasmaLab RIE system. This process involved spinning a bi-layer of PMMA resist at 12 % 2010 (700 nm thickness) and 4% 2041 (186 nm thickness) as a mask to etch 50 nm (etch rate = 33 nm/min) of AlGaIn/GaN. A bilayer was chosen, as the metallisation procedure was immediately carried out after etching. Table 2.2 shows the parameters used for etching.

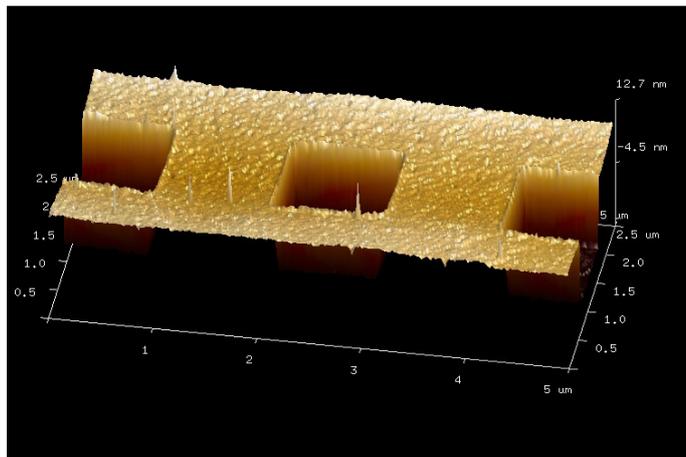
Parameters	Values
Pressure (mTorr)	8
RF platen power (W)	200
SiCl <sub>4</sub> (sccm)	25
Temperature (°C)	22

**Table 2.2:** Parameters for AlGaIn/GaN etching using RIE.

While this process proved effective for removing AlGaIn/GaN material, a common problem known as “flagging” was observed around the etched areas. Fig. 2.26 (a) shows AFM images of the flagging effect. These flags are due to re-deposition of the substrate material around the sidewalls of the mask. The samples were left in resist stripper (1165) at 50° C over 2 days and ashed using O<sub>2</sub> plasma to remove these flags. Flags were reduced, but not entirely removed. As a trial, a thinner resist layer, 12 % 2010 spun at 5000 rpm (550 nm thickness) was used and the process of etching and metallisation was split in two steps. After etching, smaller flag features were observed which was removed using low power O<sub>2</sub> plasma. Fig. 2.26 (b) shows an AFM image with the flags removed using the above process



(a)



(b)

**Fig. 2.26:** AFM image of (a) Flags around etched area (b) No-flags around etched area.

## 2.12 Conclusion

This chapter has provided an overview of fabrication and measurement techniques used in this work. Processes for fabricating antenna and other passive devices, as well as ohmic contacts and the challenges faced while developing these processes were shown. This chapter also discussed deep SiO<sub>2</sub> etching, wet etching of Au and Ti metal and air-bridges fabrication. The airbridge process developed was implemented successfully in terahertz stack antenna design, the deep SiO<sub>2</sub> etch fabrication technique was implemented in both terahertz antenna, couplers and power dividers, and etch of AlGaIn/GaN surface fabrication technique was successfully implemented to achieve low contact resistance on AlGaIn/GaN on LR Si. The following chapters discuss the design theory and results obtained from devices made using these techniques.

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## On-chip Antenna Technology on GaN-on-LR Silicon

### 3.1 Introduction

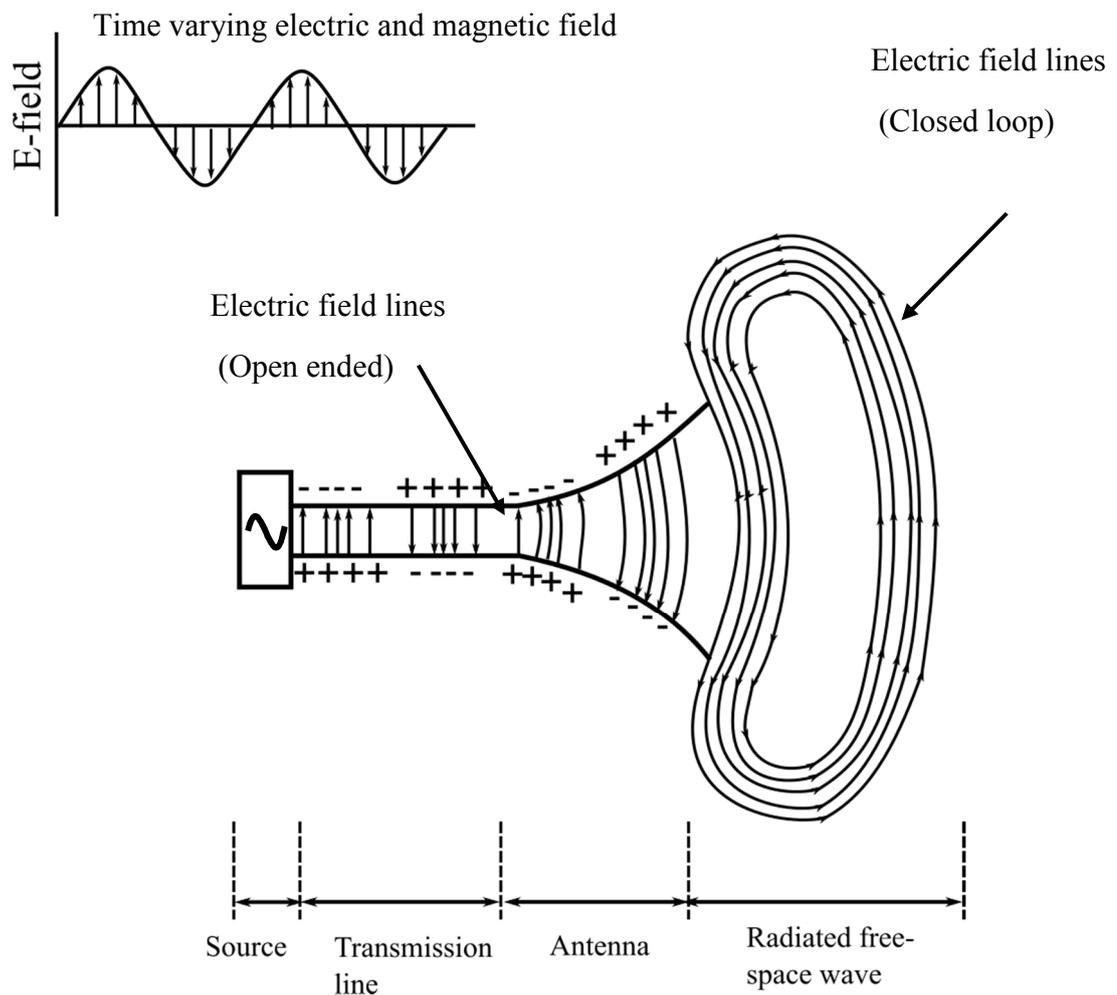
Frequency range up to 1 THz (millimetre and sub-millimetre waves) find applications in imaging, communication (100 Gb/sec), sensing, wireless high definition video streaming and large file transfers [3.1]. Sensing and imaging applications benefit due to the unique properties of Terahertz waves (T-waves) which are better suited to diffusion through fog, rain, snow and other such mediums. The small wavelength and high operating frequency of T-waves also provide the advantage of higher data rates for wireless communication, which reduces size of the components and antennas for airborne systems.

Presently, High Electron Mobility Transistors (HEMTs) are the most advanced devices for next generation TMICs as they deliver high gain at very high frequencies with low noise for an active device [3.2]. III-V materials are well suited for this due to their high-power density and efficiency. The use of GaN HEMTs grown on low resistivity (LR) Si for TMIC circuits has the advantage of low cost and large wafer sizes. For terahertz applications mentioned above, antenna gain (~25 dB), and efficiency (~80 %) are both critical parameters in producing effective isotropic radiated power (EIRP), high spectrum resolution and high sensitivity. For this, integrated antennas are beneficial due to their wide bandwidth and improved beam shaping, combined with lower production cost and smaller form factor. A common means of integration is by design of off-chip antenna on a Printed Circuit Board (PCB), Low Temperature Cofired Ceramic (LTCC) or any low loss material, and then integrating with active devices [3.3]. While this approach can provide an antenna with acceptable efficiency, the overall system efficiency will be reduced by parasitics related to

interconnects like wire bonding and flip-chip bonding. As a result, on-chip antenna (active devices and antenna on same chip/substrate) can be used, which allows integration of devices with a compromise of low efficiency and larger chip size. However, when these antennas are designed on such high-dielectric and thick substrates (e.g. GaN, GaAs, InP...) at millimeter or sub-millimeter wave lengths, this gives rise to total internal reflections within the substrate which produces surface waves [3.4]. This chapter introduces design techniques which are used for antenna at terahertz frequencies to overcome the losses presented by surface modes.

## 3.2 Antenna Theory

The IEEE standard definition defines an antenna as “a means for radiating or receiving radio waves”. It is an intermediate structure between free-space and a guiding device, Fig. 3.1. The guiding device, or transmission lines, is used to transport electromagnetic energy from a source to the antenna, or from the antenna to the receiver. When a voltage is applied across the transmission lines an electric field is formed. This electric field has associated with it “electric lines of force” which are tangential to the field. An electric line of force describes a directional force experienced by a unit charge when placed in the electric field of another charged particle. The direction of this force can be represented by imaginary lines, shown in Fig. 3.1. The magnitude of an electric field can be represented by the concentration of electric lines of force. These electric lines of force act upon the conductor’s free electrons, causing the flow of current, which in turn creates magnetic field intensity (Maxwell’s equation) [3.5].

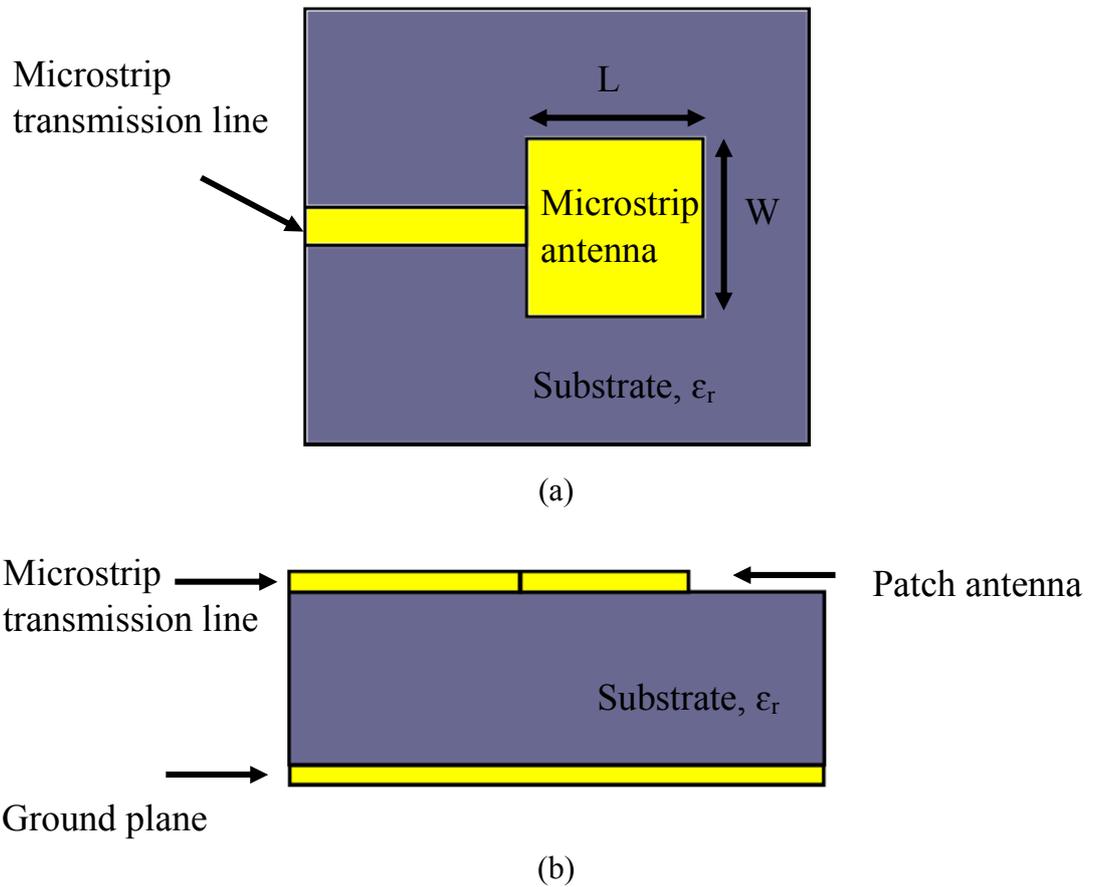


**Fig. 3.1:** Antenna radiation technique [3.5].

The electric field lines start from on positive charge and end on negative charge. They can also start on a positive charge and end at infinity or start at infinity and end on a negative charge, or form closed loops neither starting nor ending on any charge. Whereas magnetic field lines form closed loops encircling the current carrying conductor as physically there is no magnetic charge. The field lines drawn between the conductors in Fig. 3.1 also indicates the distribution of charge. If the source is sinusoidal, the electric field between the conductors is also sinusoidal. The time-varying electric and magnetic field between the conductors creates electromagnetic waves which travel along the transmission lines and enter the antenna along with the respective electric charges and currents. As these waves approach open space, free space waves are formed by connecting the open end of the electric lines. As the source continuously creates the electric disturbance, the electromagnetic waves are created continuously. Inside the transmission line and the antenna, the electromagnetic waves are sustained by the charges, as soon as they enter free space, they form closed loops and are radiated (electrons are not required to sustain the radiation) [3.5].

Since the power needs to be transferred from receiver (the energy contained in voltages and currents) into electromagnetic radiation (energy contained in E and H-fields) travelling away from antenna, the impedance of the antenna needs to be approximately matched to the receiver or transmitter, and the currents or voltages which cause the radiation should add in-phase, rather than cancel each other out. There are many kinds of antenna- wire, aperture, microstrip, array, reflector etc. In this work, both microstrip and array antenna on GaN-on-LR Si at terahertz frequencies are presented.

Cao *et al.* investigated various kinds of waveguides at terahertz using low dielectric material and showed microstrip waveguides as best [3.6]. In this research, antenna or transmission line configuration was optimised to be microstrip configuration. Microstrip antenna became popular in the 1970s for space borne applications [3.5] and are now commonly used for government and commercial applications. A microstrip antenna is generally also referred to as a patch antenna. Microstrip is a configuration, where signal and ground are not on the same plane. Fig. 3.2 shows a diagram of side and top view of a microstrip antenna, fed by a microstrip transmission line. The patch antenna and microstrip transmission line are made from metals with high conductivity, such as Au, Cu and Al. The substrate used may be a III-V material or a printed circuit board (PCB). The performance of the antenna depends of the size of the patch, design of feed, substrate thickness and associated losses. Microstrip antennas are low cost, convenient for planar and non-planar surfaces, simple, easy to fabricate and are compatible with MMIC designs. The following sections below explain more about the patch antenna radiation and figures of merit.



**Fig. 3.2:** 2D image of patch antenna (a) Top view (b) Side view.

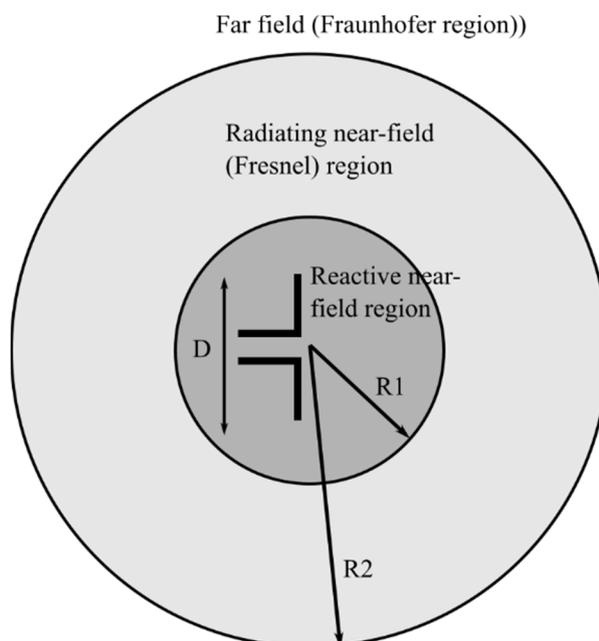
### 3.2.1 Antenna radiation field

The radiation field patterns, associated with an antenna, change with distance and are related to two kinds of energy, reactive and radiating. The reactive field is characterised by standing waves and represents stored energy. The radiating field is characterised by radiating (propagating) waves and represents transmitted energy [3.5]. Thus, the region around an antenna can be split into three regions, Fig. 3.3.

**Reactive near-field region:** The reactive field closely surrounds the antenna, where the reactive field pre-dominates. The range of this field is at a distance,  $R_1 = 0.62[D^3/\lambda]^{1/2}$ , where  $R_1$  is the distance from the antenna surface,  $D$  is the largest dimension of the antenna (radiating part) and  $\lambda$  is the wavelength.

**Radiating near-field region (Fresnel region):** This region lies between the reactive near-field region and far-field region. Here, radiation energy is more dominant than in the reactive field and the angular field distribution is dependent on the distance from the antenna. The range of this field is  $0.62\sqrt{D^3/\lambda} \leq R_2 \leq 2D^2/\lambda$ .

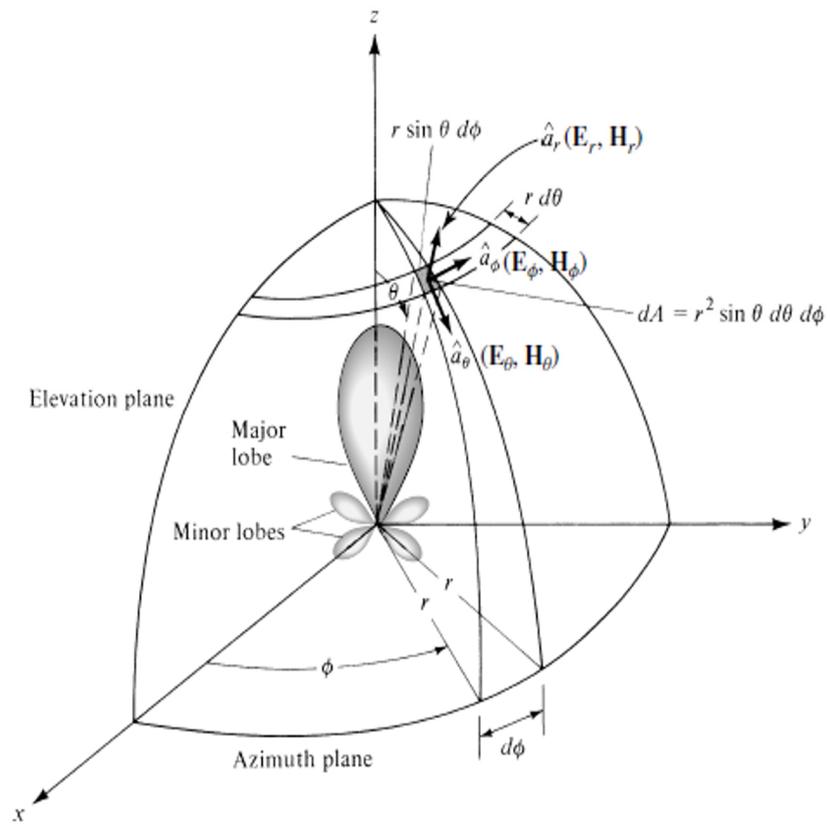
**Far-field region (Fraunhofer region):** The region beyond  $R_2 \geq 2D^2/\lambda$  is the far field region. In this region, reactive energy is absent and only the radiation fields exist. The angular field distribution is not dependent on the distance from the antenna and the power density varies as the inverse square of the radial distance.



**Fig. 3.3:** Field regions of an antenna [3.5].

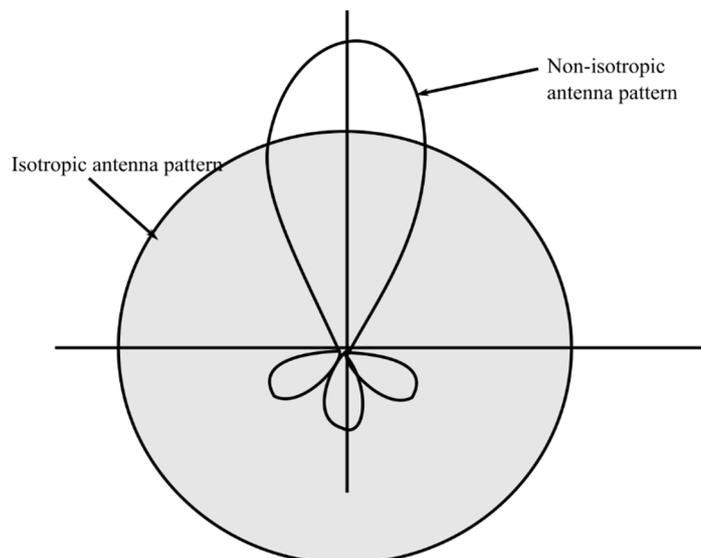
### 3.2.2 Antenna radiation pattern

An antenna radiation pattern is defined as a mathematical function or a graphical representation of the radiation properties of an antenna as a function of space coordinates. In most cases, the radiation pattern is decided in the far-field region and is characterised as a function of the directional coordinates, Fig. 3.4. The radiation properties include power flux density, radiation intensity, field strength, directivity, phase and polarisation. An outline of the received electric field at a constant radius is called the amplitude field pattern and the graph of spatial variation of power density along constant radius is called the amplitude power pattern. Two parameters which can be found from the radiation pattern are Half Power Beam Width (HPBW) and front-to-back ratio [3.7].



**Fig. 3.4:** Antenna radiation pattern [3.5] Copyright © 2005, John Wiley & Sons, Inc.

Radiation patterns can be classified, based on shape, as isotropic, omnidirectional or directional. An isotropic antenna radiates equally in all directions and is used as a reference point to describe real world antennas. An antenna which radiates and receives equally in a single plane is omnidirectional in nature. All physically realizable antennas are directional antennas, they focus energy more in a specific direction rather than in all directions, Fig. 3.5.



**Fig. 3.5:** Directional and isotropic antenna pattern.

### 3.3 Antenna figures of merit

Performance of an antenna can be evaluated by the following parameters- return loss, directivity, gain, efficiency and bandwidth.

#### 3.3.1 Impedance and return loss

Antenna impedance ( $Z=R_A + jX_A \Omega$ ) relates the voltage to the current at the input of an antenna. The “real” part of *antenna impedance* ( $R_A =R_r + R_L$ ) represents the power that is radiated away or absorbed within the antenna. While the imaginary part of the *impedance* ( $X_A$ ) represents power stored in the near field of the antenna (non-radiated power). For an antenna to be resonant, this imaginary value should be zero. The power associated with radiation resistance ( $R_r$ ) is the power radiated by the antenna or is coupled to other modes and power associated with loss resistance is dissipated as heat in the antenna due to dielectric and conduction losses. Equation (3.1) shows the input impedance of antenna and feed line in terms of antenna impedance  $Z_A$ , characteristic impedance  $Z_0$ , length of transmission line  $L$ , and speed of light  $c= 3 \times 10^8$  m/s [3.8].

$$Z_{in} = Z_0 \frac{Z_A + jZ_0 \cdot \tan\left(\frac{2\pi f}{c} L\right)}{Z_0 + jZ_A \cdot \tan\left(\frac{2\pi f}{c} L\right)} \quad (3.1)$$

While designing an antenna, it is matched to the transmission line to deliver maximum power from source to the antenna. Otherwise, the input impedance will vary greatly with the length of the transmission line. If the input impedance is not matched to the source impedance, the power will be lost before being delivered to the antenna and will be reflected. This situation is known as impedance mismatch.

A common way to measure how well an antenna is matched to a transmitter or receiver is a metric called Voltage Standing Wave Ratio (VSWR). If VSWR is equal to 1, there will be no loss due to mismatch. If VSWR is greater than 1 there will be loss. Equation (3.2) shows the VSWR in terms of voltage reflection coefficient [3.8].

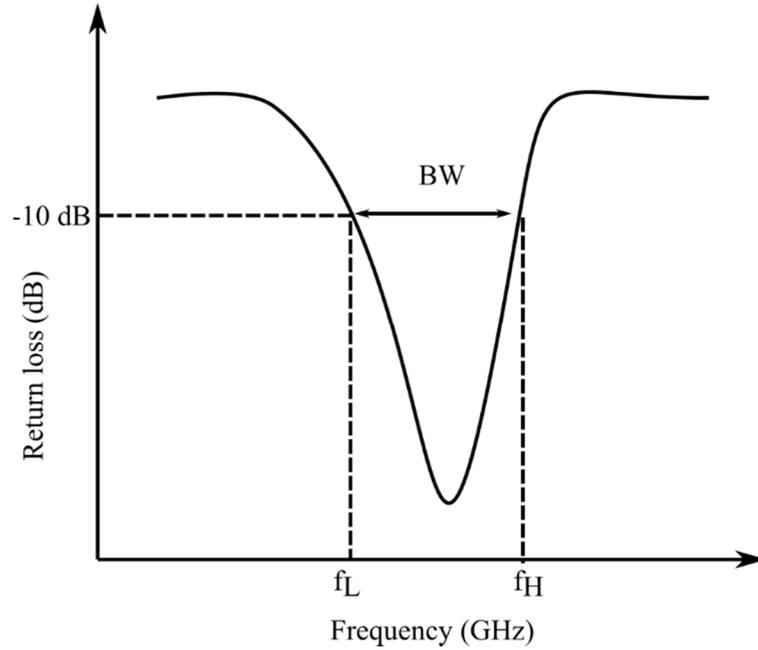
$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1 + \Gamma}{1 - \Gamma} \quad (3.2)$$

Where,

$$\Gamma = \frac{Z_A - Z_0}{Z_A + Z_0} \quad (3.3)$$

Return loss is a parameter which measures how small the reflection is and is defined as the ratio of reflected power to the incident power, Equation (3.4) [3.8]. Lower return loss means that there is less energy being lost in the delivery of power to antenna, Fig. 3.6.

$$RL = \frac{V_i^2 |\Gamma|^2 / Z_0}{V_i^2 / Z_0} = 20 \log_{10} |\Gamma| \text{ dB} \quad (3.4)$$



**Fig. 3.6:** Plot of return loss.

### 3.3.2 Bandwidth

The bandwidth of an antenna is the frequency range in which antenna can properly radiate and receive energy, and where parameters such as gain, directivity and input impedance are within acknowledged values [3.5]. A microstrip patch antenna is a narrow band antenna, where bandwidth is expressed as a percentage indicating frequency difference over the centre frequency of the bandwidth, Fig. 3.6.

$$BW = f_H - f_L \quad (3.5)$$

Where,  $f_H$  = frequency value at which antenna reflection coefficient raises above -10 dB and  $f_L$  = frequency value at which antenna reflection coefficient falls below -10 dB. For a

microstrip patch antenna, the substrate below the antenna predominantly decides the bandwidth. The higher the dielectric constant is, smaller the bandwidth of the patch antenna will be and vice versa.

### 3.3.3 Directivity

Fringing fields within the patch result in the antenna radiating. If the radiated waves favour a certain direction, then the antenna is deemed to have certain directivity. Otherwise, the directivity is said to be equal to 1 or 0 dB (isotropic antenna). In mathematical form, directivity can be written as the ratio of maximum radiation intensity in each direction to the average radiation intensity in all directions as shown in equation below [3.8]:

$$D = \frac{U_{max}}{U_0} = \frac{4\pi U_{max}}{P_{rad}} \quad (3.6)$$

Where  $U_{max}$  = maximum radiation intensity (W/ unit solid angle),

$U_0$  = average radiation intensity =  $\frac{P_{rad}}{4\pi}$  (W/unit solid angle);

$P_{rad}$  = total power radiated (W)

For two radiating slots ( $k_0h \ll 1$ ) (according cavity model), the directivity can be written as:

$$D = \left(\frac{2\pi W}{\lambda_0}\right)^2 \frac{\pi}{I_2} \quad (3.7)$$

Where,  $I_2$

$$= \int_0^\pi \int_0^\pi \left[ \frac{\sin\left(\frac{k_0 W}{2} \cos \theta\right)}{\cos \theta} \right]^2 \sin^3 \theta \cos^2 \left( \frac{k_0 L_e}{2} \sin \theta \sin \varphi \right) d\theta d\varphi \quad (3.8)$$

Where,  $k_0$  is the wavenumber, and  $h$  is the height of the substrate.

### 3.3.4 Gain

Gain of an antenna is defined as “the ratio of the intensity, in a given direction, to the radiation intensity that would be obtained if the power accepted by the antenna were radiated isotropically. The radiation intensity corresponding to the isotropically radiated power is equal to the power accepted (input) by the antenna divided by  $4\pi$ ” [3.8]. It is expressed below:

$$Gain = 4\pi \frac{\text{radiation intensity}}{\text{total accepted power}} = 4\pi \frac{U(\theta, \phi)}{P_{in}} \text{ (dimensionless)} \quad (3.9)$$

Gain which considers the reflection/mismatch losses can be represented as

$$G(\theta, \phi) = \epsilon_R D \text{ (dimensionless)} \quad (3.10)$$

$$G \text{ (dB)} = 10 \log_{10}(\epsilon_R D) \quad (3.11)$$

### 3.3.5 Antenna Efficiency

The efficiency of an antenna can be defined as the ratio of power radiated from an antenna to the power delivered to an antenna. If the efficiency of an antenna is perfect, this would mean that power delivered to the antenna is radiated away into free space with zero loss. In reality, a perfect antenna does not exist. As such, power is lost due to conduction loss, dielectric loss and impedance mismatch loss [3.5].

$$e_0 = \frac{P_{radiated}}{P_{Input}} \quad (3.12)$$

The above equation is referred to as an antenna's radiation efficiency. Total efficiency considers the antenna losses and can be written as [3.5]

$$e_0 = e_r e_c e_d \quad (3.13)$$

Where,  $e_0$  = total efficiency,  $e_r$  = reflection efficiency ( $1 - |\Gamma|^2$ ) (dimensionless),  $e_c$  = conduction efficiency (dimensionless),  $e_d$  = dielectric efficiency (dimensionless),  $\Gamma$  = voltage reflection coefficient at the input antenna terminal.

### 3.3.6 Front-to-Back Ratio and Half power beam-width

The front-to-back ratio is the ratio of the gain in the maximum direction to that in the opposite direction. It's usually expressed in dB and describes the directional radiation pattern of an antenna.

The half power beam-width can be defined as the angle between the two directions in which the radiation power is one-half the maximum value of the main lobe.

### 3.4 Substrate modes in microstrip antenna

The dielectric constant of the semiconductor substrate offers both advantages and disadvantages while designing an on-chip antenna. If it is high, this reduces the size of the antenna as well as makes the antenna more prone to substrate modes. The number of modes -Transverse Electric (TE), Transverse Magnetic (TM), which propagates through the substrate, is governed by the following mathematical expressions [3.9]:

$$f_c = \frac{nc}{4d\sqrt{(\epsilon_r - 1)}} \quad \begin{array}{l} n=0,2,4\dots \text{ for TM modes} \\ n=1,3,5\dots \text{ for TE modes} \end{array} \quad (3.14)$$

Where  $f_c$  = cut-off frequency of the mode,  $c$  = speed of light,  $n$  = an integer,  $\epsilon_r$  = relative dielectric permittivity of the substrate, and  $d$  = thickness of the substrate.

As the substrate thickness increases, the number of modes increases. The total power of these surface waves becomes equal to the sum of the individual surface waves present at that operating frequency. A microstrip antenna always excites some surface waves because a grounded dielectric layer has a zero-cut-off frequency for dominant  $TM_0$  mode. As a result, this launches surface wave modes, in addition to the antenna radiation, into the atmosphere [3.10]. This reduces the radiation efficiency of an antenna (for an infinite substrate) as there is power lost in the initiation of these surface modes. The radiation efficiency of an antenna when other losses are considered zero is given by:

$$\eta = \frac{P_{rad}}{P_{rad} + P_{SW}} \quad (3.15)$$

Where  $\eta$  = radiation efficiency,  $P_{rad}$  = radiation power  $P_{SW}$  = surface wave power radiated into the dielectric.

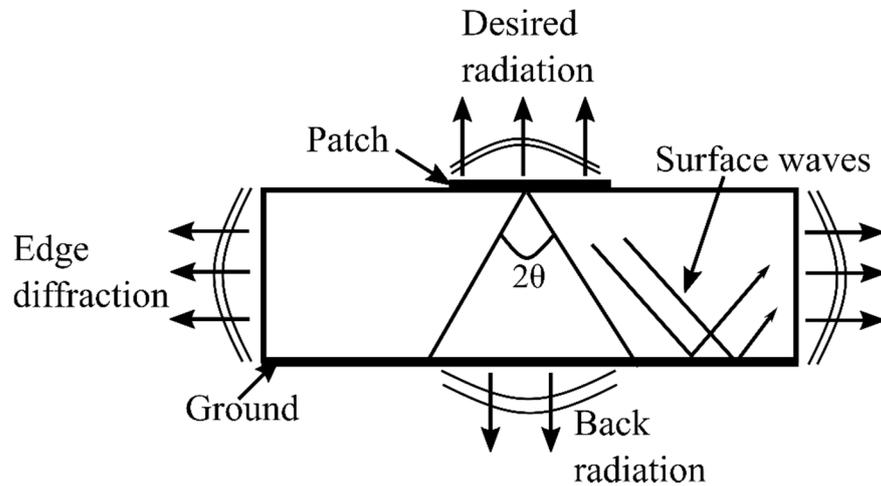
This power loss is smaller when the substrate is thin compared to the free-space wavelength  $\lambda_0$ . Equation (3.16) defines this [3.11]:

$$\frac{d}{\lambda_0} \leq \frac{0.3}{2\pi\sqrt{\epsilon_r}} \quad (3.16)$$

As a result, it is important to avoid any higher order excitations of modes by selecting a thinner substrate and lower dielectric to ensure that the cut-off frequency  $f_c$  for mode  $n = 1$  is above the operating frequency. In the case of thicker substrates with higher dielectric constant, the waves undergo total internal reflection and are diffracted from the edges of the substrate, causing the disruption of the radiation pattern and mutual coupling between the

antennas. Equation (3.17) shows the elevation angle of the wave's incident into the substrate. This is shown in the Fig. 3.7.

$$\frac{\pi}{2} \leq \theta \leq \pi - \sin^{-1}\left(\frac{1}{\sqrt{\epsilon_r}}\right) \quad (3.17)$$



**Fig. 3.7:** Surface waves in thick and high dielectric antenna substrate [3.11].

### 3.5 Methods to improve antenna performance

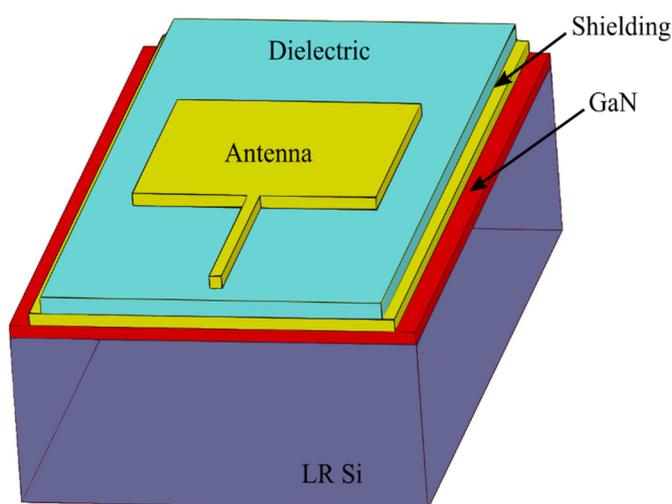
To improve the antenna performance at millimeter and submillimeter wave frequencies, one must reduce the surface losses caused by thick and/or high dielectric constant substrates. There are several ways this can be done: removal of the substrate (micromachining technique), use of a highly resistive substrate, use of thick organic polymers and selection of radiators [3.12]. In a micromachining technique, either the substrate underneath the antenna is removed or the whole substrate thickness is reduced. Naturally, the substrate thickness can only be reduced so far for practical reasons, adding additional complication to how the substrates are handled and processed. On-chip antenna on a high resistivity substrate or semi-insulating substrate can also work within certain frequencies (up to 200 GHz), after which surface modes decrease performance of the antenna.

Novel designs of antenna can improve upon this. A circular patch design with the same radius as that of a magnetic current ring will not excite  $TM_0$  surface waves, using a thin substrate where  $TM_0$  surface wave is above cut-off will not excite surface wave power [3.10]. However, for this radius the antenna will not resonate at the desired frequency. This is solved by increasing radius of the patch while keeping the radiating aperture constant, which makes the size of the antenna larger than desired. Another method to decrease the

high dielectric losses is by separating the substrate from the radiating element using organic polymers like polyimide, BCB, SiO<sub>2</sub> etc., which typically have a lower dielectric constant than that of the substrate material, such as GaN, GaAs or InP. The main disadvantage of this technique is in achieving thick polymer height. Other techniques such as shorted annular structures [3.9], making air-dielectric interface perfect PML (perfect magnetic conductor) [3.9] and multi-layered substrate [3.9] has been investigated for eliminating the surface wave losses. However, these techniques are difficult to employ at terahertz frequencies.

### 3.6 Shielding technique

In this work, a shielding technique has been adopted to design antenna at terahertz frequencies with reduced loss, Fig. 3.8. Previously, this technique has been used for an above Integrated Circuit (IC) process at lower frequencies [3.13]. Typically, a ground plane (Au or Al) is placed between the antenna and a low-resistivity silicon substrate with a low dielectric layer as a separator or as an isolation layer between them.



**Fig. 3.8:** Shielding technique.

P. Abele *et al.* was the first to use this technique to integrate a MMIC differential oscillator with a patch antenna on a SiGe substrate at 24 GHz [3.13]. This integration technique achieved an antenna with radiated power of -4 dBm. From there, a few groups have documented results using this technology. R. Wang *et al.* designed a microstrip patch antenna using Back End Of the Line (BEOL) as the ground plane on SiGe [3.14]. They used a layer of BCB with a thickness of 24  $\mu\text{m}$  and achieved a gain of 3.4 dBi at 122.5 GHz with simulated efficiency of 50%. Tianxi *et al.* was the first to demonstrate microstrip patch antenna integration on lossy silicon [3.15]. They achieved a BCB thickness of 25  $\mu\text{m}$  with 1.67 % impedance bandwidth and no document of gain. Vettikalladi *et al.* showed a

Substrate Integrated Waveguide (SIW) antenna design using multiple thin layers of BCB. Simulated gain and directivity obtained from this design was 8.9 dBi and 10.5 dBi respectively at 60 GHz with 70 % radiation efficiency [3.16]. All the above studies were carried out at lower frequencies (24 -180 GHz) and no reports were made of using other dielectric materials as the isolation layer.

### 3.7 Losses in microstrip transmission line

For any integrated circuit, transmission lines play a significant component to conduct electromagnetic waves in antennas or signals from one place to another between passives and active circuits. Hence, to design a low-loss circuit, three parameters of III-V substrates are significant; loss tangent ( $\delta$ ), relative dielectric permittivity ( $\epsilon_r$ ) and thickness of the material ( $h$ ). In this section, microstrip transmission lines on dielectric substrates at both MM-wave and terahertz frequencies is discussed.

To calculate the losses in a transmission line, we need to know the attenuation constant ( $\alpha_T$ ) which combines three different losses; dielectric loss, conductor loss and radiation loss. The equation below represents this:

$$\alpha_T = \alpha_C + \alpha_D + \alpha_R \quad (3.8)$$

Where,  $\alpha_C$  represents metal conductivity loss,  $\alpha_D$  represents dielectric tangent loss, and  $\alpha_R$  is the loss due to radiation. These losses are frequency dependent. Conduction loss is proportional to the square-root of frequency, while dielectric loss is proportional to frequency. Radiation loss is constant and independent of frequency. The following section discusses these attributes and how they impact performance at terahertz frequencies [3.9] [3.6].

#### 3.7.1 Dielectric loss

Dielectric loss is the dissipation of energy through the movement of charge in a varying electromagnetic field. Dielectric loss for a Quasi-TEM (Transverse Electromagnetic Modes) transmission line can be written as [3.17]:

$$\alpha_D = \frac{27.3\sqrt{\epsilon_r} \tan\delta}{\lambda_0} \text{ (dB/unit length)} \quad (3.9)$$

Where  $\lambda_0$  is the free space wavelength in meters,  $\epsilon_r$  is the relative permittivity of the substrate and  $\tan \delta$  is the loss tangent of the dielectric. The loss tangent is the ratio of imaginary value of the dielectric permittivity to the real value.

Dielectric loss is higher around the resonant frequencies (frequency where device operates) and tends to be higher in materials with higher dielectric constant. Since the dielectric permittivity changes with frequency, loss tangent also changes with frequency. At lower frequencies, the dielectric loss is linear and increases as the frequency increases.

### 3.7.2 Conductor loss

When a microstrip line is designed on a low-loss dielectric substrate, the main cause of losses is from the imperfect conductors (signal and ground metals). Electromagnetic fields from the alternating current (AC) produces voltage across these conductors causing eddy currents to flow through them. These currents increase the conductor loss and operating temperatures. The Skin effect occurs due to opposing eddy currents, induced by changing magnetic field. This effect results in the distribution of current density to gather at the surface of the conductor and decrease moving deeper into bulk. Thus, electric current flows mainly at the skin (beneath the surface, within a region called the skin depth) of the conductor. The skin effect causes the effective resistance of the conductor to increase at higher frequencies, as the skin depth region becomes smaller at these frequencies. Attenuation constant of a wide microstrip line is given by [3.18]:

$$\alpha_c = \frac{8.686R_s}{Z_0 w} \text{ dB/cm} \quad (3.20)$$

Where,  $W$ = width of the conductor and surface skin resistance ( $R_s$ ) is

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}} \quad (3.21)$$

$$R_s = \frac{1}{\delta \sigma} \text{ } \Omega/\text{square} \quad (3.22)$$

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \text{ is the skin depth in cm} \quad (3.23)$$

Where,  $\delta$ =skin depth,  $\mu$  and  $\sigma$  are permeability and the conductivity of metals respectively,  $f$ = frequency.

As seen from Equation (3.21), as frequency increases, the skin resistance  $R_s$  increases, and conductor thickness should be made at least four times higher than  $\delta$  to compensate this. In a microstrip line, current density will not be uniform in the strip and ground plane as it tends to diverse at the strip edges at a rate which causes the skin loss to be infinite. This leads to leakage of the electrical field to the adjacent ground planes [3.19].

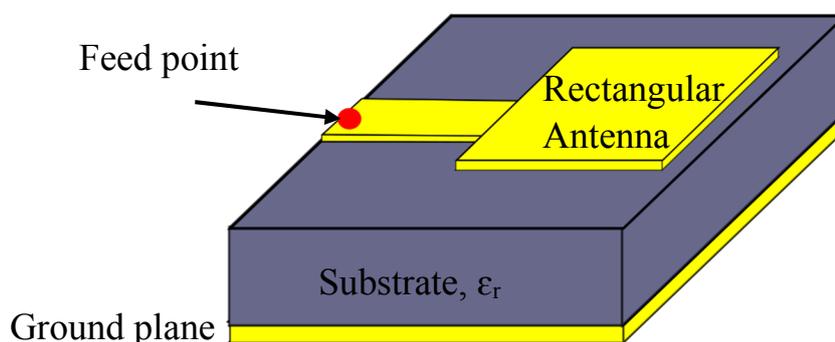
### 3.7.3 Radiation loss

There are two main contributors for radiation losses,  $\alpha_R$ . One is due to surface waves, where excited waves are coupled between the dominant mode and the other parasitic modes, occurring due to substrate thickness. Another is due to shock waves, which is leakage into the substrate and occurs when phase velocity  $V_P$  of the dominant mode is higher than the TEM mode in the dielectric. To address the radiation loss, 3D modelling software such as HFSS and CST can be used. Generally, a thicker substrate produces more radiation loss and bends in the transmission line produces more loss than straight lines.

## 3.8 Design theory of microstrip patch antenna

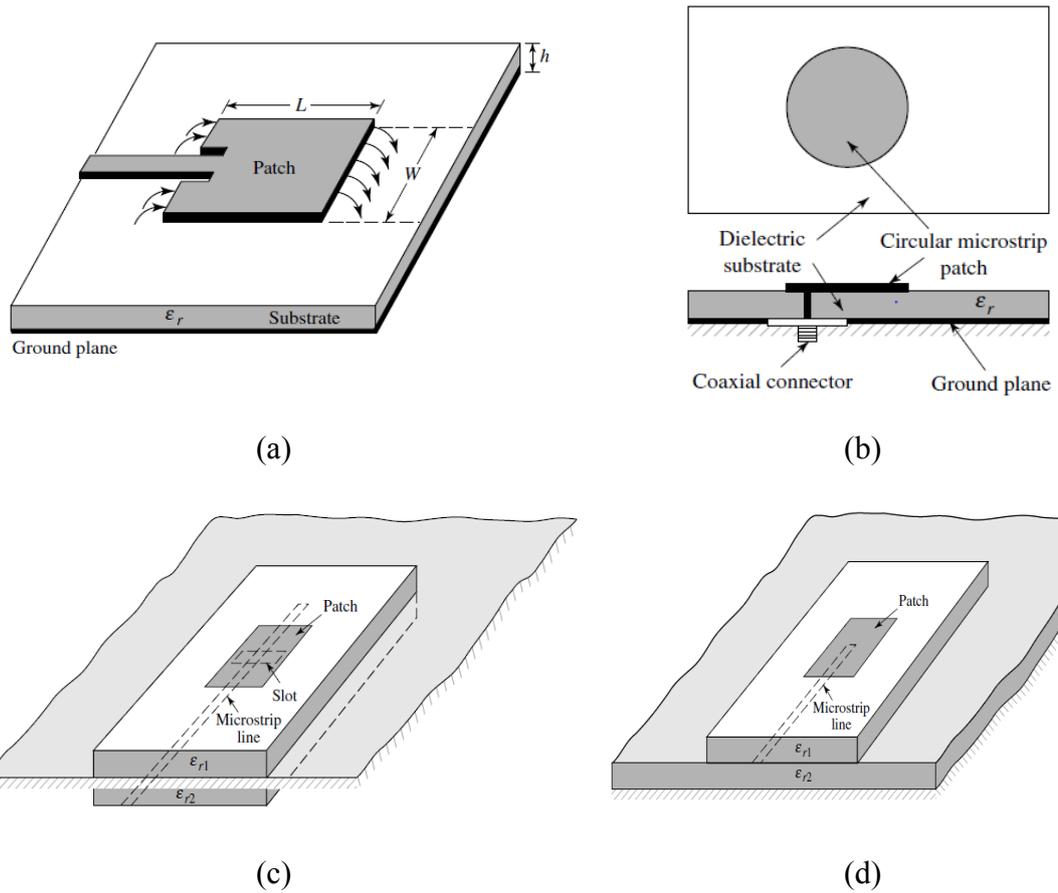
### 3.8.1 Rectangular microstrip antenna

A 3D diagram of a rectangular microstrip patch antenna is illustrated in Fig. 3.9. This is one of the popular shapes of patch used in many antenna applications. The width (W) and length (L) of the patch decides the operational frequency of the antenna. Substrate thickness and dielectric constant determines the efficiency, bandwidth, size and radiation fields of the antenna.



**Fig. 3.9:** 3D diagram of a rectangular microstrip patch antenna.

Microstrip antennas are excited by a feed line and Fig. 3.10 shows four frequently used configurations of the feed (Microstrip line feed, probe fed, aperture-coupled feed, and proximity-coupled feed) [3.5]. Microstrip line feed (Fig. 3.10 (a)) is a conducting strip, which is smaller than the antenna. It is easier to fabricate and simple inset technique (where the antenna is fed closer to the centre, as current is higher nearer to the centre of the antenna, reduces the input impedance) can be used to match the antenna to microstrip line. As the substrate thickness increases, surface waves and spurious feed radiation increases and limits the bandwidth to 2-5 % [3.5].



**Fig. 3.10:** Commonly used feed techniques (a) Microstrip line feed (b) Probe fed (c) Aperture-coupled feed (d) Proximity-coupled feed [3.5] Copyright © 2005, John Wiley & Sons, Inc.

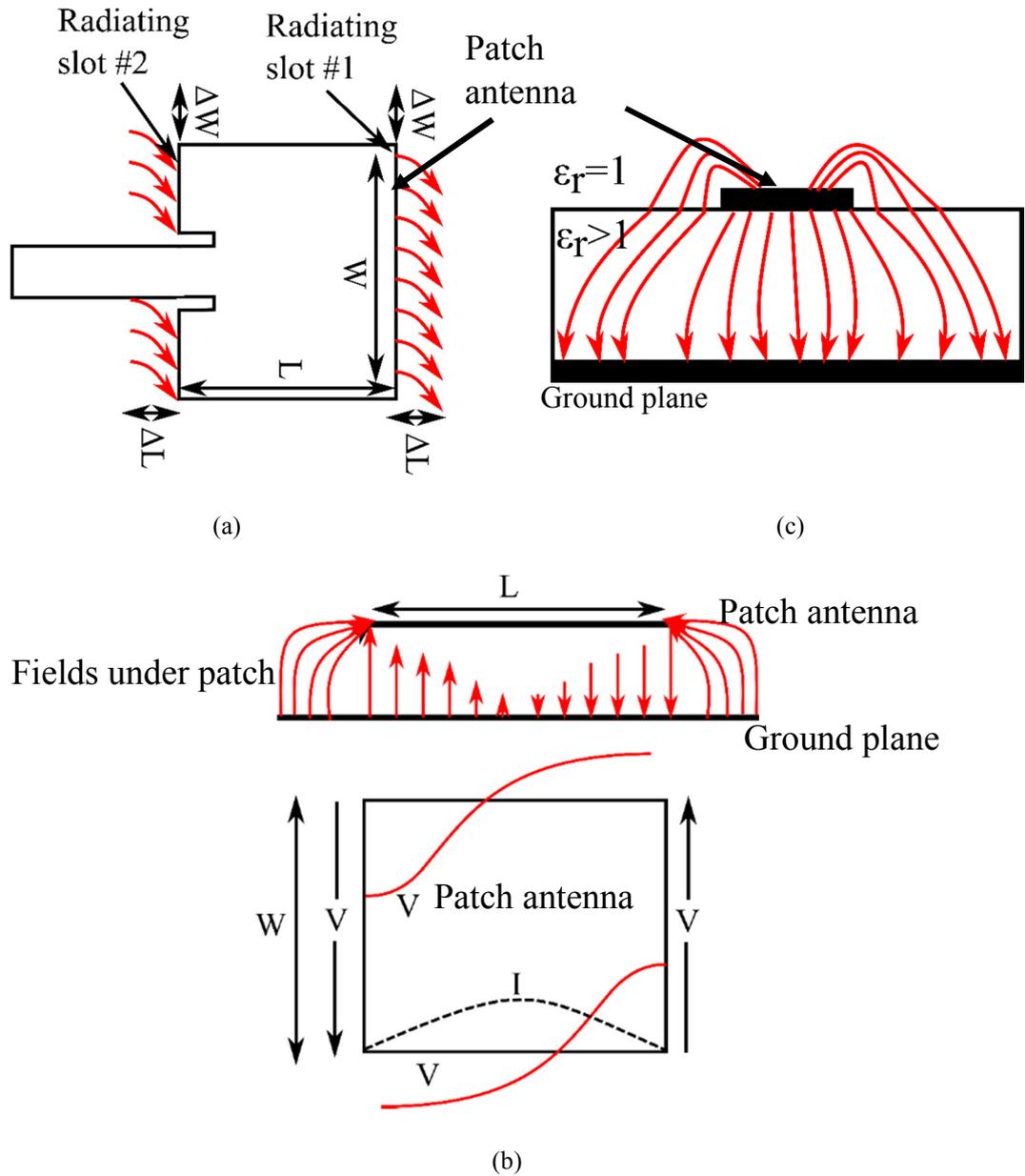
In probe fed (Fig. 3.10 (b)), coaxial conductors are used, where the inner conductor is attached to the patch, while the outer conductor is attached to the ground plane. This technique is used at very low frequencies and produces low spurious radiation. It is also difficult to model, especially for thick substrates ( $h > 0.02\lambda_0$ ).

For both aperture coupled (Fig. 3.10 (c)) and proximity coupled feed (Fig. 3.10 (d)), the feed is placed on a different substrate than the antenna. This configuration can be used to overcome cross-polarised radiation and allows optimisation of the antenna and feed separately. In an aperture-coupled feed, two substrates are separated by a ground plane and energy from the feed is coupled to the patch through a slot in this ground plane. Proximity coupled feed is the most complicated configuration to fabricate. The feed is excited using coaxial conductor and achieves maximum bandwidth and low spurious radiation compared to other configurations.

## Transmission line model for rectangular patch

There are three common ways in which an antenna can be modelled: Transmission line model, cavity model and full wave model. The transmission line model gives good physical understanding of the antenna, but not coupling effects. This is overcome by using the cavity model, which is complex to design. Full wave model, is very accurate and flexible in modelling single elements, stacked elements, finite and infinite arrays, and coupling [3.5].

A rectangular microstrip antenna, using the cavity model, can be denoted as an array of two radiating slots each of width  $W$  and height  $h$ , separated by a distance  $L$  (see Fig. 3.11 (a)). When the system is excited, the patch edges undergo voltage fringing between the patch and the ground plane, as the length and width of the patch are of finite sizes. This fringing effect is the reason why a patch antenna radiates. For  $TM_{10}$  mode, the field varies  $\lambda/2$  cycle along the length and there is no change along the width of an antenna. As the patch antenna can be considered an open circuited transmission line, the voltage reflection coefficient will be equal to 1. When this happens, the voltage and current are out of phase. Thus, voltage is maximum at the end of the patch which causes the beginning of the patch to have minimum voltage due to half wavelength distance. The change in voltage and current in and around the patch is shown in the Fig. 3.11 (b). The fringing field adds up in the positive  $y$  direction. In other words, the phase of the fringes is added to create the radiation of the antenna. There is also the addition of current in the antenna, which is cancelled due to the opposite current in the ground plane. This is what causes an antenna to radiate, but not the microstrip line. For E-plane ( $xy$ -plane), fringing is due to length  $L$  and height  $h$  with a dielectric constant  $\epsilon_r$ . As  $L/h \gg 1$ , fringing is reduced but still considered due to resonant frequency of the antenna. The same applies for the width of the patch.



**Fig. 3.11:** Electromagnetic wave propagation in (a) patch antenna (b) when  $TM_{10}$  mode excited in antenna (c) microstrip transmission line [3.5] [3.20].

For a microstrip line, electric field lines lie in both the substrate and air. As a result, the dielectric constant considered in calculations should be effective dielectric constant (summation of air and substrate dielectric constant), as shown in the Fig. 3.11 (c). If  $W/h \gg 1$  and  $\epsilon_r \gg 1$ , most of the electric field lines are confined to the substrate, causing fringing outwith the physical dimensions of the microstrip line. This effect results in the device appearing electrically larger. The effective dielectric constant is calculated by the Equation (3.24):

$$\epsilon_{reff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[ 1 + 10 \frac{h}{W} \right]^{-1/2}, \text{ for } W/h > 1 \quad (3.24)$$

The fringing field can be considered as the two parallel plate capacitors [3.20]:

$$C = \varepsilon_0 \varepsilon_r \frac{WL}{h} \quad (3.25)$$

If  $\Delta L$  and  $\Delta W$  is the length extended on each side. The effective length and width due to fringing can now be written as

$$L_{eff} = L + 2\Delta L \quad (3.26)$$

$$W_{eff} = W + 2\Delta W \quad (3.27)$$

For regular microstrip antenna, extended length can be written as

$$\Delta L = \frac{h}{\sqrt{\varepsilon_{reff}}} \quad (3.17)$$

As the effective length is equal  $\lambda/2$ , for given resonant frequency ( $f_0$ ) it can be written as

$$L_{eff} = L + 2\Delta L = \frac{\lambda_0}{2\sqrt{\varepsilon_{reff}}} = \frac{c}{2f_0\sqrt{\varepsilon_{reff}}} \quad (3.18)$$

Normally resonant frequency of the uniform patch excited at  $TM_{mn}$  mode ( $m=0, 1, 2, \dots$  and  $n=0, 1, 2, \dots$ ) can be expressed as the following equation:

$$f_0 = \frac{c}{2\sqrt{\varepsilon_{reff}}} \left[ \left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2 \right]^{1/2} \quad (3.19)$$

The width of the patch is responsible for the input impedance. For good radiation efficiency, width should be taken as equal to a half wavelength of two dielectric medium (substrate and air) (Equation 3.31). If the width is smaller, the bandwidth and gain will decrease and if the width is larger, the bandwidth increases due to an increase in radiation fields.

$$W = \frac{c}{2f_r} \sqrt{\frac{2}{\varepsilon_r + 1}} \quad (3.20)$$

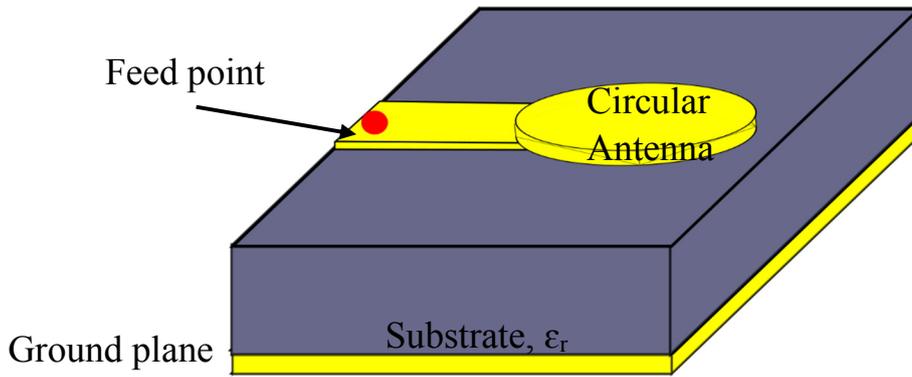
The normalised radiation patterns in the E-plane ( $E_\theta$  in  $\phi=0^\circ$  plane) and the H-plane ( $E_\phi$  in  $\phi=90^\circ$  plane) for the  $TM_{10}$  mode can be calculate using two slots as shown below

$$E_\theta = \frac{\sin\left(\frac{KW \sin \theta \sin \phi}{2}\right)}{\frac{KW \sin \theta \sin \phi}{2}} \cos\left(\frac{KL}{2} \sin \theta \cos \phi\right) \cos \phi \quad (3.32)$$

$$E_{\phi} = -\frac{\sin\left(\frac{KW \sin \theta \sin \phi}{2}\right)}{\frac{KW \sin \theta \sin \phi}{2}} \cos\left(\frac{KL}{2} \sin \theta \cos \phi\right) \cos \theta \sin \phi \quad (3.33)$$

### 3.8.2 Circular microstrip antenna

The next most popular shape for microstrip antenna, other than rectangular antenna, is the circular antenna. Jackson *et al.* showed that using a circular shaped patch could reduce excitation of surface waves [3.10]. Fig. 3.12 shows the geometry of circular microstrip patch antenna. The modes created by the circular antenna can be discovered by treating the patch, ground plane and substrate between the two as a circular cavity. Compared to a rectangular design, the circular patch has only one degree of freedom i.e., the radius of the patch. The mode supported by a circular patch for substrate height ( $H \ll \lambda$ ) is  $TM_{mn0}^Z$ , where Z is taken perpendicular to the patch [3.5].



**Fig. 3.12:** 3D diagram of a circular microstrip patch antenna.

#### Radius calculation of circular patch

The circular patch can be analysed using a cavity model. The resonant frequencies of the dominant mode  $TM_{110}^Z$  are given as [3.5]

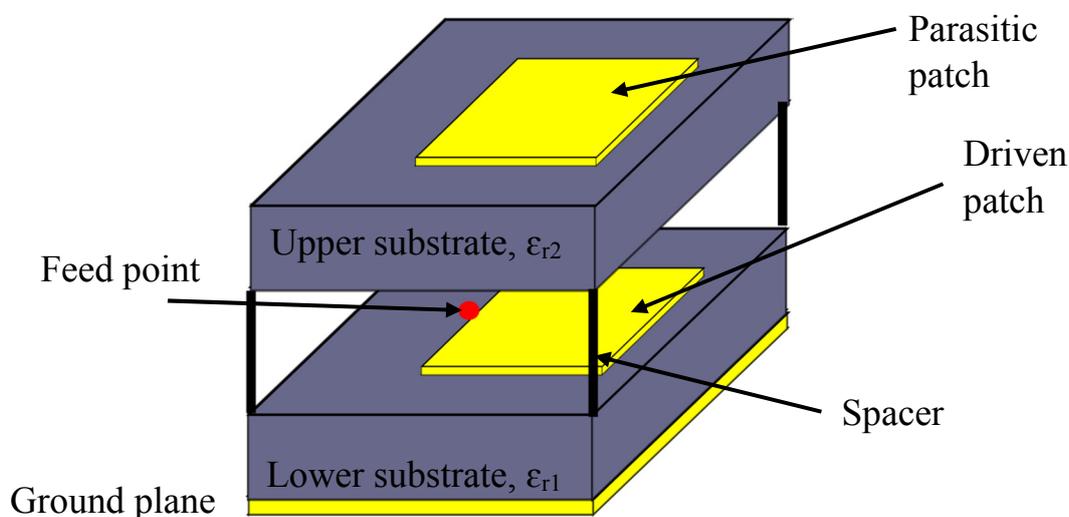
$$(f_r)_{110} = \frac{1.8412}{2\pi a \sqrt{\mu\epsilon}} \quad (3.34)$$

The above equation doesn't consider the fringing effect. Thus, the effective radius  $a_e$  to replace the actual radius  $a$  is given by [3.5]

$$a_e = a \left\{ 1 + \frac{2h}{\pi a \epsilon_r} \left[ \ln\left(\frac{\pi a}{2h}\right) + 1.7726 \right] \right\}^{1/2} \quad (3.35)$$

### 3.8.3 Stack microstrip antenna

Two large disadvantages of the single element microstrip patch antenna are the narrow bandwidth and low gain [3.21]. As a result, Sabban proposed the idea of a multiple-layer antenna, which increased the bandwidth of a single microstrip patch from 2 - 4 % to 9 - 15 % [3.22]. Fig. 3.13 shows the geometry of a two-level stack antenna. The driven patch is fabricated on the bottom substrate (1<sup>st</sup> level) and is excited using one of the feeding techniques mentioned above, whereas the parasitic patch is on the top substrate (2<sup>nd</sup> level), both are separated by a spacer. The spacer material may be air, metal rods or foam [3.21]. Lee *et al.* used this design to study the dependency of substrates on antenna gain and bandwidth and concluded that sizes of parasitic and driven patch have a significant effect on the resonant input resistance and bandwidth [3.21]. Length and width of the parasitic and driven patch is calculated in the same way as a single rectangular patch antenna, but with their respective dielectric properties of the substrates. This design has the capability to create two resonant frequencies and by using different lengths of stacked patches, the input impedance can be increased to create broadband behaviour or may be used to create a dual band antenna (antenna which operates at two different frequencies) [3.23].



**Fig. 3.13:** 3D diagram of a stack microstrip patch antenna.

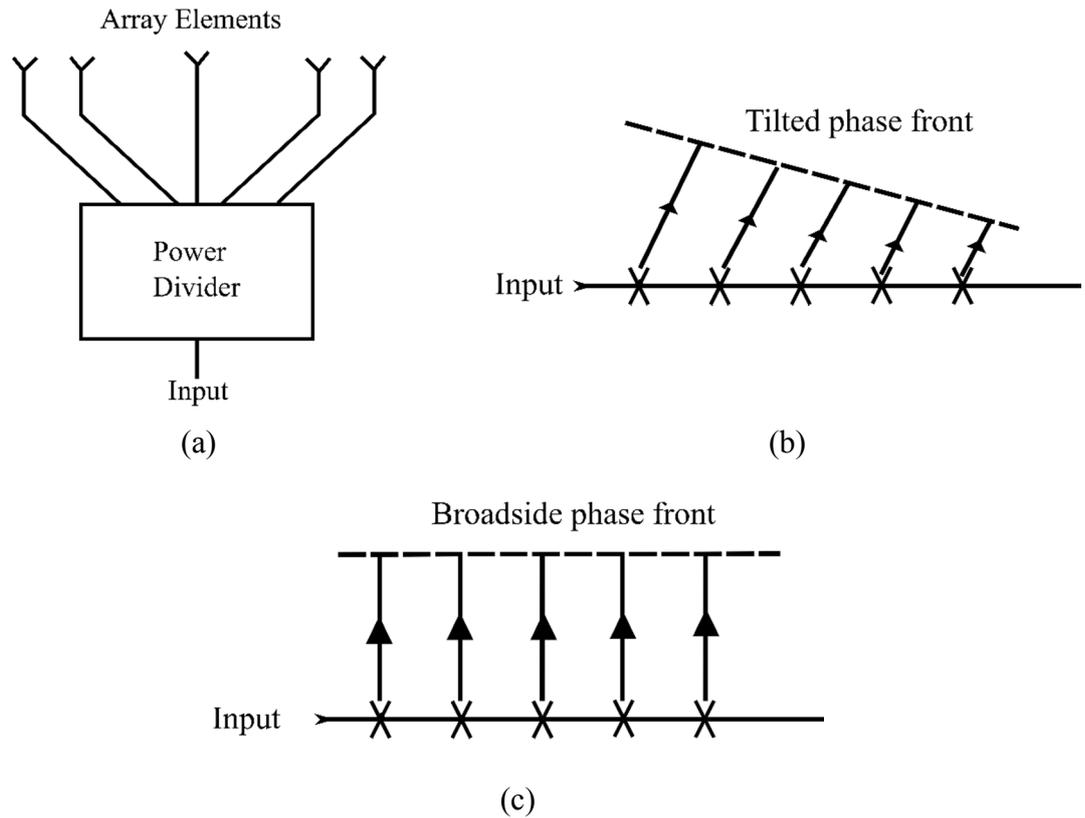
### 3.8.4 Array microstrip Antenna

Microstrip antennas can be used in arrays (multiple patches) to enhance the gain, directivity and to steer the antenna radiation in a communication system. There are two ways the antenna patches can be arranged – linear or planar. Linear arrays are used for fan-shaped analysis and can also be the building block of planar antenna. There are three main feeding methods used in this: corporate, travelling wave, and resonant feeds. Fig. 3.14 shows this.

Fig. 3.14 (a) shows the corporate feed technique, where linear antennas are fed using a simple T-power divider or the Wilkinson power divider. This feed occupies a large chip area, but it also has the advantage of broadband coverage. The most popular application of a corporate feed is in phased arrays where phase shifters are inserted in the transmission line to steer the main beam direction.

Fig. 3.14 (b) shows the travelling wave feeding method. Here, all the patches are attached to a single transmission line and signal decays along the length of the line. The main beam is tilted from the broadside as the reflections from the radiators tend to have different phase than the feed input (radiator spacing is not half a wavelength) and bandwidth is limited due to the allowed beam pointing change.

Fig. 3.14 (c) shows the resonant feed method. Unlike a travelling wave feed, patches in the resonant feed method are spaced half a wavelength, which creates a broadside pointing beam. Here, the matching between the antenna and feed limits the bandwidth of the array.



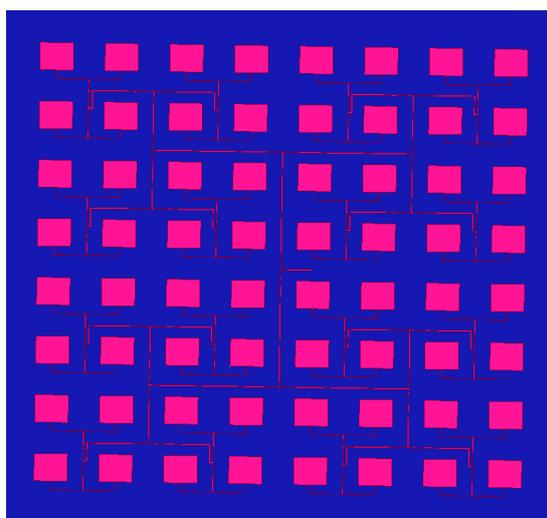
**Fig. 3.14:** Linear array feeds: (a) corporate (b) travelling wave (c) resonant feeds [3.24].

Planar microstrip arrays are used to form pencil beams and they are fed in the same way as the linear microstrip array. Fig. 3.15 (a) shows a parallel feeding, also known as binary feeding or corporate feeding array antenna. Here, two antennas are fed at the same time either using a simple T-power divider or a Wilkinson power divider. The feed lines are designed to be of similar length, so that the beam pointing is broadside to the array at all frequencies. Here, bandwidth is limited to individual patches and since the feed lines are longer, this causes spurious radiation at the bends and junctions which decreases the efficiency of the overall antenna performance. At terahertz, the number of patches that can be implemented using this technique is limited as after a certain number of arrays the efficiency and gain decrease drastically.

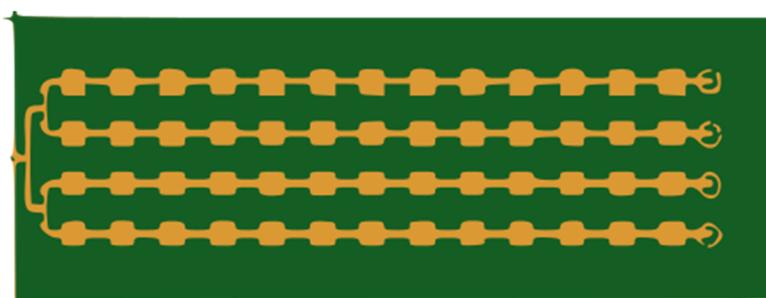
Fig. 3.15 (b) shows several linear arrays, fed using a corporate feed. This uses linear travelling wave arrays as described previously. The corporate feed here is very lossy, which makes the overall radiation efficiency  $\sim 40\%$ .

Fig. 3.15 (c) shows a planar resonant feed. It consists of a lattice of hexagons, squares or equilateral triangles. The line lengths are one-half wavelength in the medium and a voltage introduced at the feed is repeated at each line intersection. The antenna is very compact and the whole area acts as the radiating structure. The radiation efficiency is high (62%)

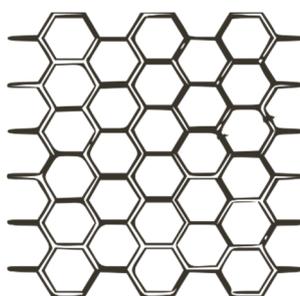
compared to planar travelling wave feed, however it is suitable only for narrow band applications.



(a)



(b)



(c)

**Fig. 3.15:** Planar array feeds: (a) corporate (b) travelling wave (c) resonant feeds [3.24]

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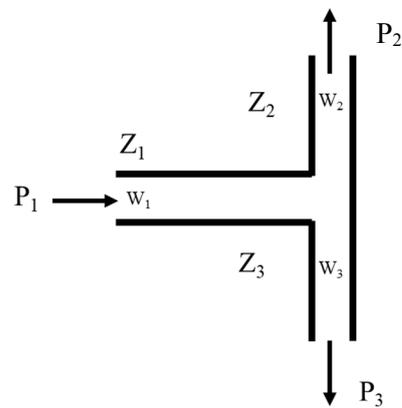
In this work, both linear corporate fed array antenna and planar corporate fed array antenna were designed, see Section 3.9.2 (Page 89) and 3.9.3 (Page 110) Fig. 3.16 shows the standard T-junction power divider.  $P_1$  is the input power to the divider and  $P_2$  and  $P_3$  are the output power. The impedance of the microstrip line which divides the power equally between two branches is calculated as follows [3.25]:

$$Z_1 = \frac{Z_2 \times Z_3}{Z_2 + Z_3} \quad (3.36)$$

$$P_2 = \frac{Z_1}{Z_2} \times P_1 \quad (3.37)$$

$$P_3 = \frac{Z_1}{Z_3} \times P_1 \quad (3.38)$$

Thus, from the above equations  $Z_2=Z_3=2 \times Z_1$ . The two impedances simulated for design are  $50 \Omega$  and  $100 \Omega$  (for fabrication easiness). The design was carried out in ADS software, see Section 3.9.2 (Page 89) and 3.9.3 (Page 110).

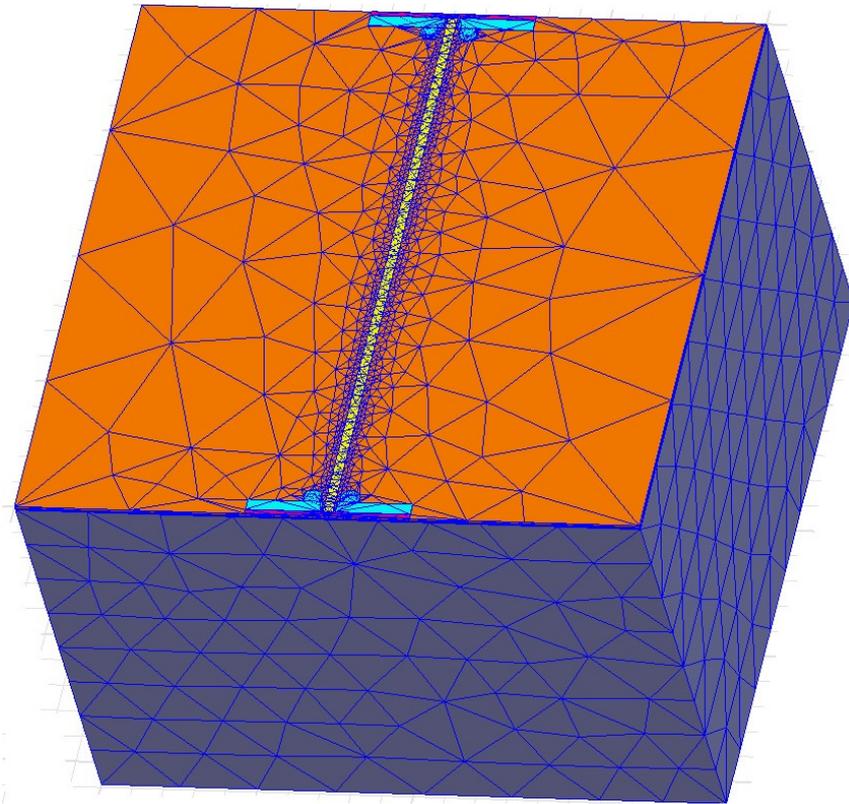


**Fig. 3.16:** Simple T-junction power divider circuit.

### 3.9 Simulation of devices

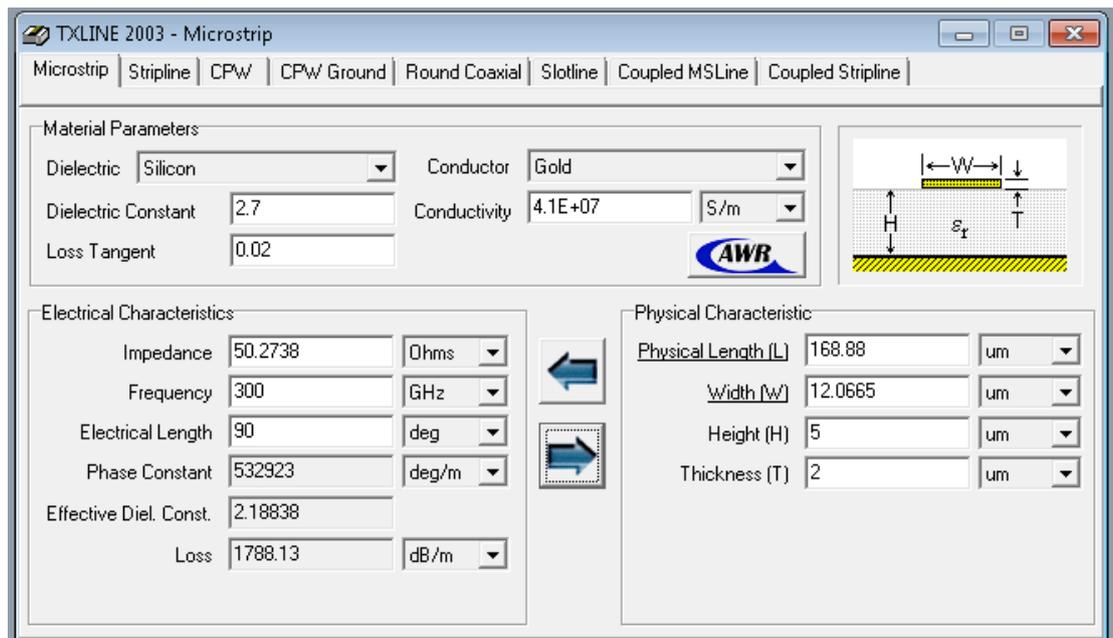
Simulation is an important stage in designing antennas since it determines the physical dimension of a device at a given resonant frequency, as well as the performance of the circuit before fabrication. There are several software packages that can be used for this purpose, such as FEKO, CST, HFSS, IE3D and ADS momentum. These use the 2D or 3D geometry of a desired design to determine the performance. As each software package uses different numerical techniques in the time or frequency domain to simulate, each is relatively suited to various passive circuit geometries. In the research presented here, HFSS software has been used to determine electromagnetic performance of an antenna, arrays and passive devices for an ideal balance between simulation time and to bridge the gap between measured and simulated results.

HFSS software employs the Finite Element Method (FEM), adaptive meshing and intense graphics to provide performance and insight into 3D EM problems. It takes advantage of the Microsoft windows graphical user interface [3.26]. For a passive device, HFSS can be used to calculate parameters such as S-parameters, resonant frequency and E- and H- fields. The 2D or 3D geometry and materials used for passive devices are designed and assigned in HFSS. Parameters such as the physical dimension of a device, loss tangent and dielectric constant of the materials being used. For these parameters, boundaries and excitations are assigned. There are two types of boundaries and excitation- radiation boundaries and Perfectly Matched Layers (PML), wave port and lumped port excitation respectively. To solve this 3D geometry, HFSS uses a meshing technique, where complex curves and shapes are divided into large tetrahedral elements. Each tetrahedron is made up of four triangular face and together this collection of tetrahedron forms a finite element mesh. In 2D, field points are calculated using 6 points (3 corners and 3 midpoints) and in 3D using 10 points. Vertices of the triangle store the components of a field that are tangential to the edges of an element and the midpoint of the selected edges store the component of field that are tangential to the face of an element and normal to an edge. Using these stored values, H-field and E-field are calculated inside each tetrahedron. A first order basis function is used to perform the interpolation. Further, by using Maxwell's equation the field quantities are later transformed into matrix equations which are solved using traditional numerical methods. Fig. 3.17 shows the finite element mesh for a  $50 \Omega$  transmission line on BCB ( $W=13.2 \mu\text{m}$ ,  $L=1 \text{ mm}$ - Section 3.9.1).



**Fig. 3.17:** Finite mesh created by HFSS software for 50  $\Omega$  transmission line.

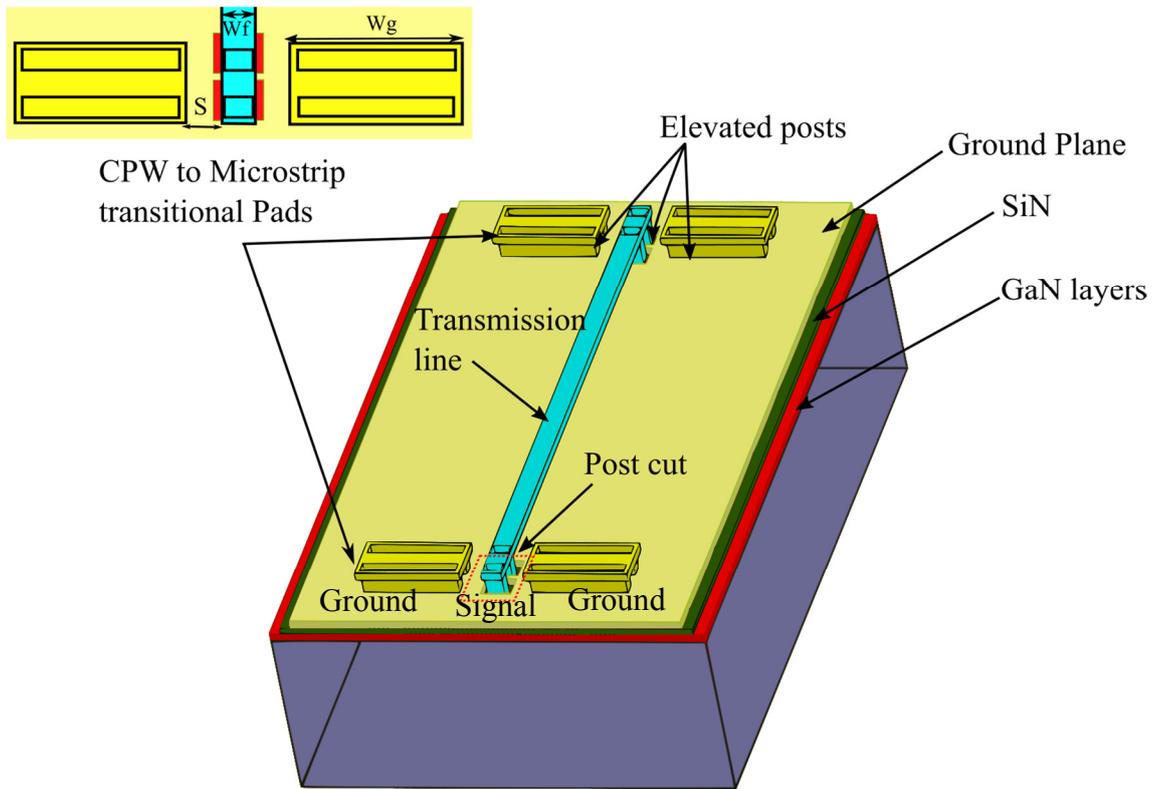
Additionally, a tool kit named TXLINE from AWR software was used to give initial dimensions of a transmission line using the substrate dielectric constant, loss tangent and thickness. Fig. 3.18 shows the calculation for a 50  $\Omega$  transmission line on BCB dielectric at 300 GHz using this tool.



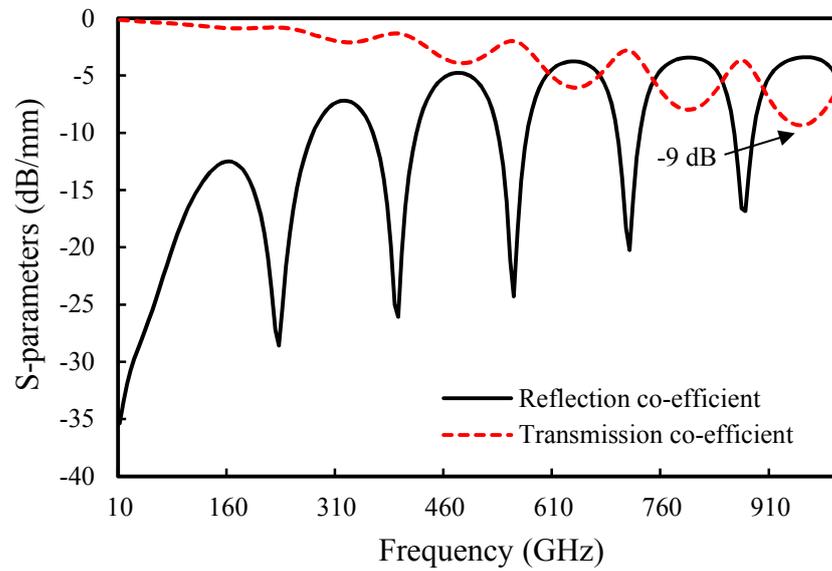
**Fig. 3.18:** AWR tool kit to calculate width and length of transmission lines and antennas.

### 3.9.1 Simulation of Microstrip transmission line using shielding technique

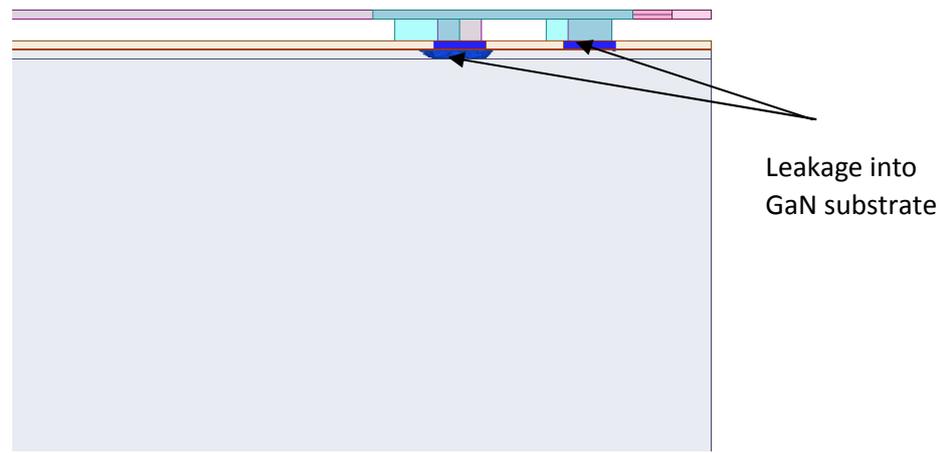
In this section, simulation of microstrip transmission line up to terahertz frequencies (10 GHz – 1 THz) using different dielectric materials (Air, BCB, SiO<sub>2</sub>) is presented. These dielectric materials have lower loss tangent and dielectric constant at terahertz frequencies and are relatively easy to fabricate. Fig. 3.19 (a) shows a 3D model of a 50  $\Omega$ -1mm length elevated microstrip transmission line using air as a dielectric. The dielectric constant and loss tangent used for this simulation was 1 and 0 respectively. This is the lowest dielectric constant and almost zero loss one can use as a dielectric material in RF designs. Width of the signal line was calculated using the Line-calc tool of ADS software to achieve 50  $\Omega$ . Here, the 50  $\Omega$  signal line with 50  $\Omega$  CPW transition is elevated in air using gold posts. The width of the signal line was simulated to be 20  $\mu\text{m}$  (Wf), the distance between CPW ground and signal line was 9  $\mu\text{m}$  (s), and width of the CPW ground was 120  $\mu\text{m}$  (Wg). Mismatch between the signal line and CPW transition is reduced by matching them to 50  $\Omega$  separately. A small window is opened in the ground plane so that the signal post does not short with the ground plane. Fig. 3.19 (b) shows the plot of transmission and reflection coefficient of the elevated microstrip line. As can be seen, a transmission of -9.5 dB and reflection coefficient of -3 dB was achieved at 1 THz. In addition, the transmission coefficient shows some leakage due to the opening in the shielding ground plane, see Fig. 3.19 (c). Thus, we can say elevation works at lower GHz frequencies (-0.36 dB transmission co-efficient at 67 GHz), but as the frequency increases there is more leakage of current through the window. Eblabla *et al.* [3.27] have used BCB under Ground plane (shielding) to overcome this problem.



(a)



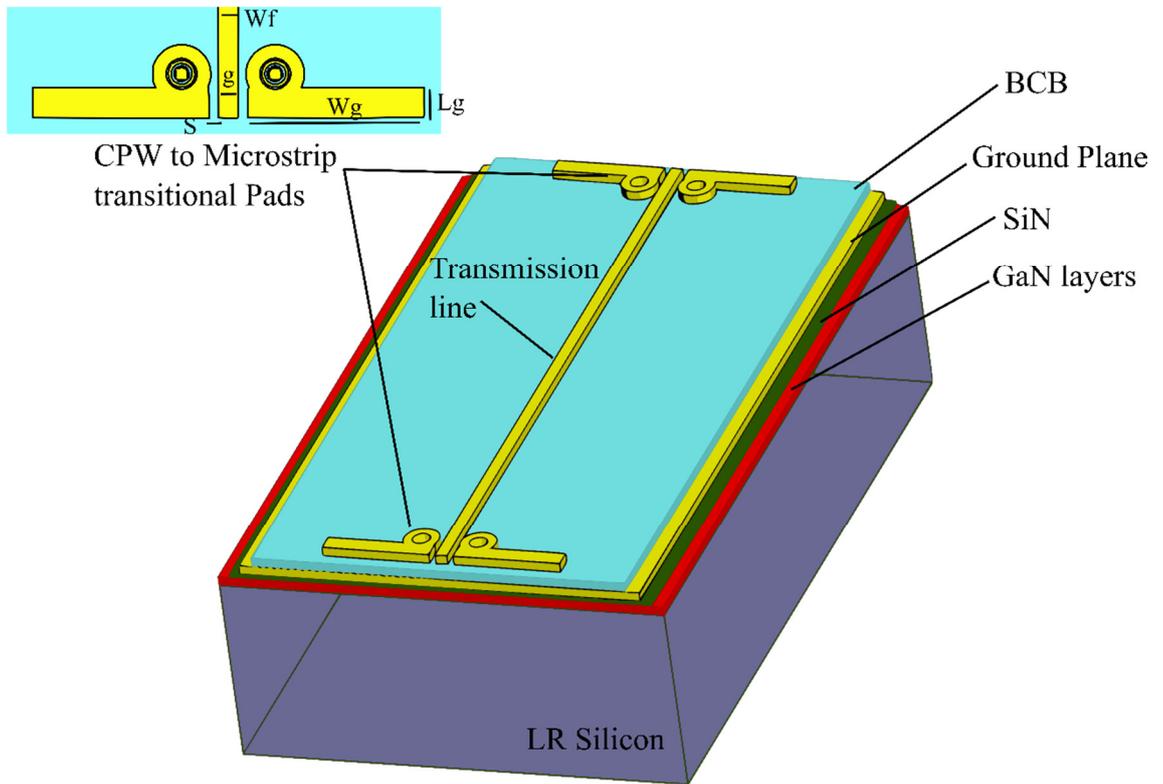
(b)



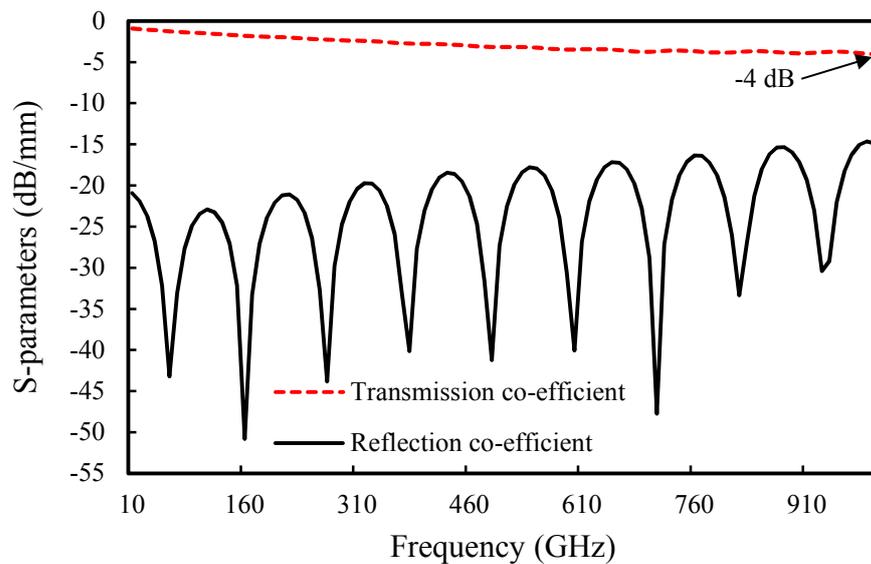
(c)

**Fig. 3.19:** 50  $\Omega$ -1mm transmission line on Air (a) 3D diagram (b) plot of transmission and reflection co-efficient (c) leakage of current into GaN substrate through post cut.

Fig. 3.20 (a), shows a 3D model of a 50  $\Omega$ -1mm length microstrip transmission line on BCB with a circular via-hole transition. The dielectric constant and loss tangent of BCB used in this simulation was 2.7 and 0.02 respectively, which is higher than that of air as dielectric. A thickness of 5  $\mu\text{m}$  was used for the transmission line. The width of the transmission line was 13.2  $\mu\text{m}$  ( $W_f$  and  $g$ ), the distance between CPW ground and signal line was 3.9  $\mu\text{m}$  ( $s$ ), and the dimensions of the CPW ground pads were 120  $\mu\text{m} \times 20 \mu\text{m}$  ( $W_g \times L_g$ ). Mismatch between the signal line and CPW transition is reduced by matching them to 50  $\Omega$  separately. Fig. 3.20 (b) shows a plot of transmission and reflection coefficient of the microstrip transmission line. A transmission coefficient of -4 dB and reflection co-efficient of less than -14 dB was achieved. There was no indication of leakage in the transmission coefficient (in contrast to the previous simulation) as there was no current leakage into the Si substrate.



(a)



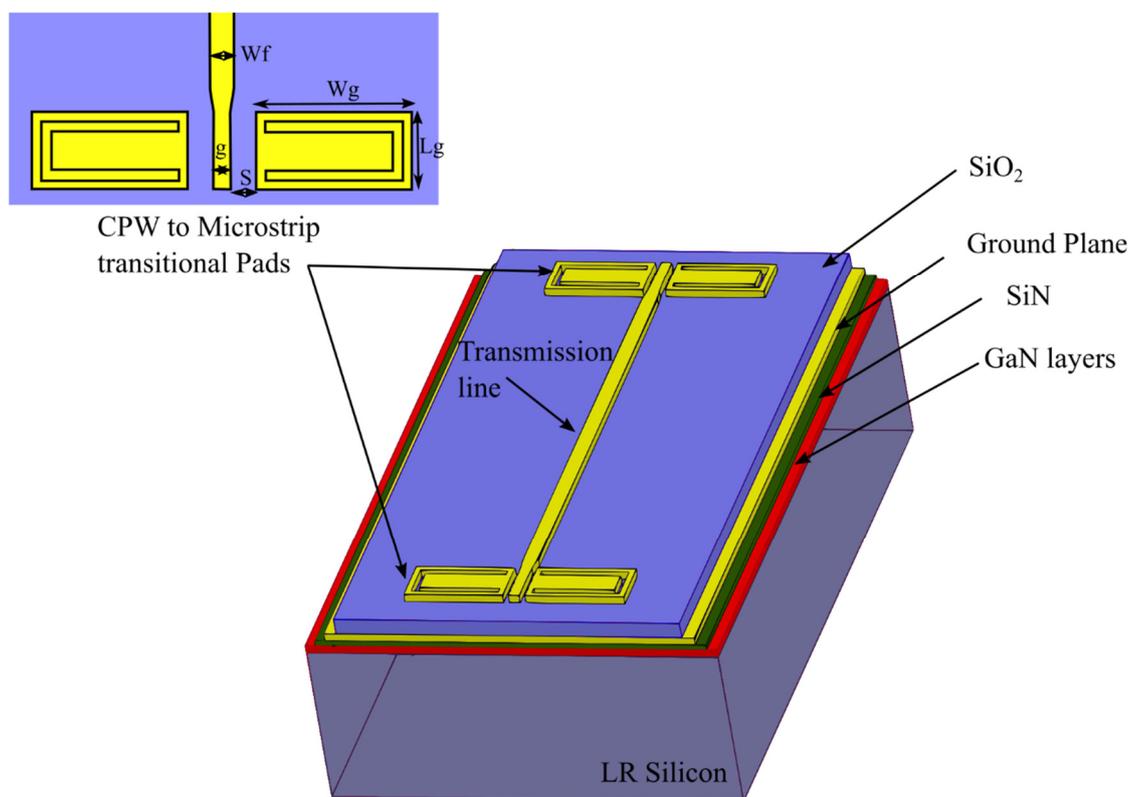
(b)

**Fig. 3.20:** 50  $\Omega$ -1mm transmission line on BCB (a) 3D diagram (b) plot of transmission and reflection co-efficient [3.28].

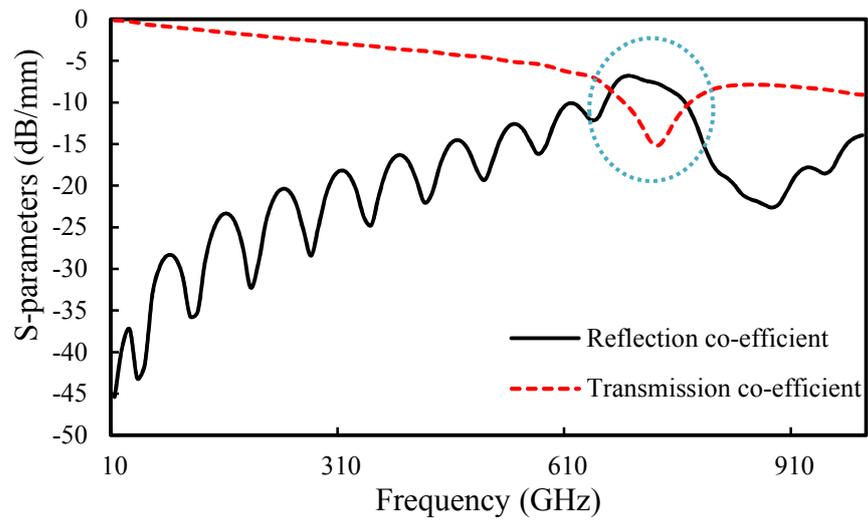
Fig. 3.21 (a), shows a 3D model of a 50  $\Omega$ -1mm length microstrip transmission line on SiO<sub>2</sub> with a rectangular via-hole transition. The dielectric constant and loss tangent of SiO<sub>2</sub> used in simulation was 4 and 0.04 respectively. This material is lossier due to higher dielectric constant and loss tangent compared to the other two simulated materials (air and BCB). SiO<sub>2</sub> thickness used for this simulation was 10  $\mu\text{m}$ . The shape of the via-hole transition was altered

from the BCB design (circular) to a square one due to fabrication flexibility (square etching is comparatively easier than circular). Fig. 3.21 (b) shows the plot of transmission and reflection co-efficient when the via-hole shape was changed from circular to square. As it can be seen, there is a resonance at certain frequencies as the square via-hole acted more like an inductor. To reduce this inductance, the via-hole was etched all around the CPW pads (rectangular via-hole). The width of the transmission line simulated was  $19\ \mu\text{m}$  ( $W_f$ ), the distance between CPW ground and signal line ( $S$ ) was  $5\ \mu\text{m}$ , the dimensions of the CPW ground pads were  $120\ \mu\text{m} \times 20\ \mu\text{m}$  ( $W_g \times L_g$ ), and the width of signal pad ( $g$ ) was  $13.2\ \mu\text{m}$ . Mismatch between the signal line and CPW transition is reduced by matching them to  $50\ \Omega$  separately. Fig. 3.21 (c) shows the plot of transmission and reflection co-efficient of the rectangular via-hole around the CPW pads. Transmission coefficient of  $-6.3\ \text{dB}$  and reflection coefficient below  $-12\ \text{dB}$  at  $1\ \text{THz}$  was achieved.

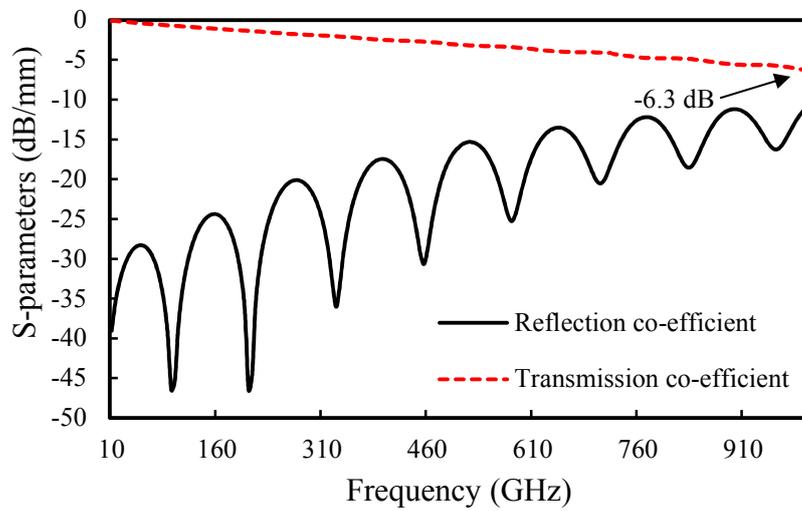
Comparing all three transmission line designs, BCB material offered lower transmission co-efficient at terahertz frequencies. Since all the transmission line designs are run from  $10\ \text{GHz}$  to  $1\ \text{THz}$ , the matching at  $1\ \text{THz}$  may not be as good compared to lower frequencies. Values of transmission coefficient might vary by  $\pm 0.5\ \text{dB}$  from the plots shown, whereas values of reflection efficient may vary by  $\pm 10\ \text{dB}$ .



(a)



(b)



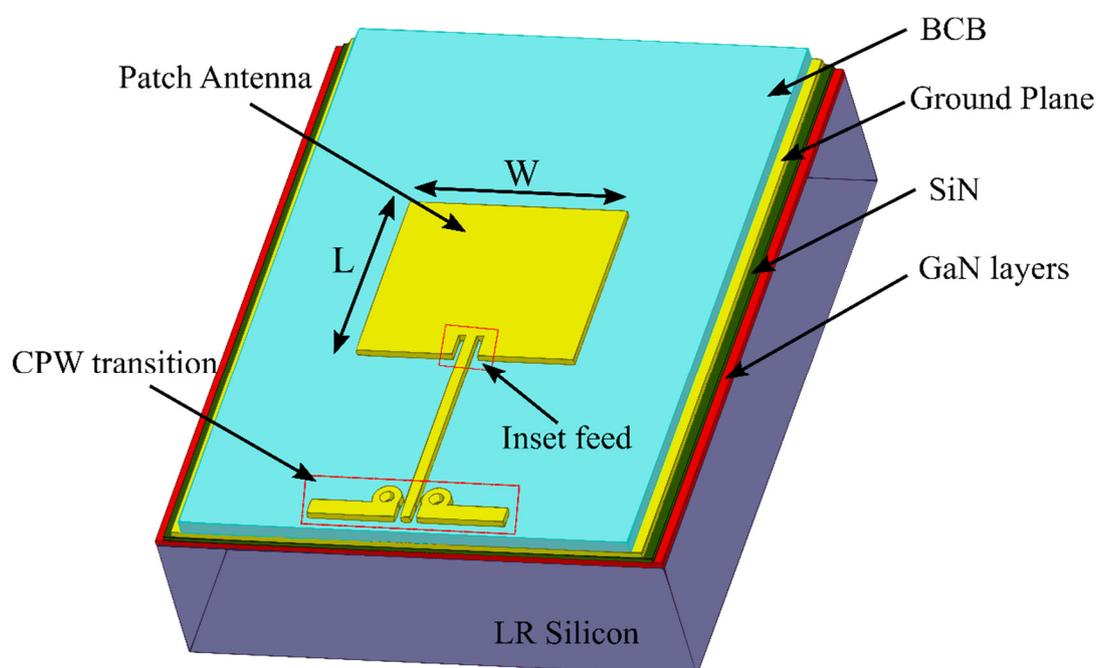
(c)

**Fig. 3.21:** 50  $\Omega$ -1mm transmission line on SiO<sub>2</sub> (a) 3D diagram (b) plot of transmission and reflection co-efficient of square via-hole (c) plot of transmission and reflection co-efficient of new rectangular via-hole.

### 3.9.2 Simulation of Microstrip antenna using BCB

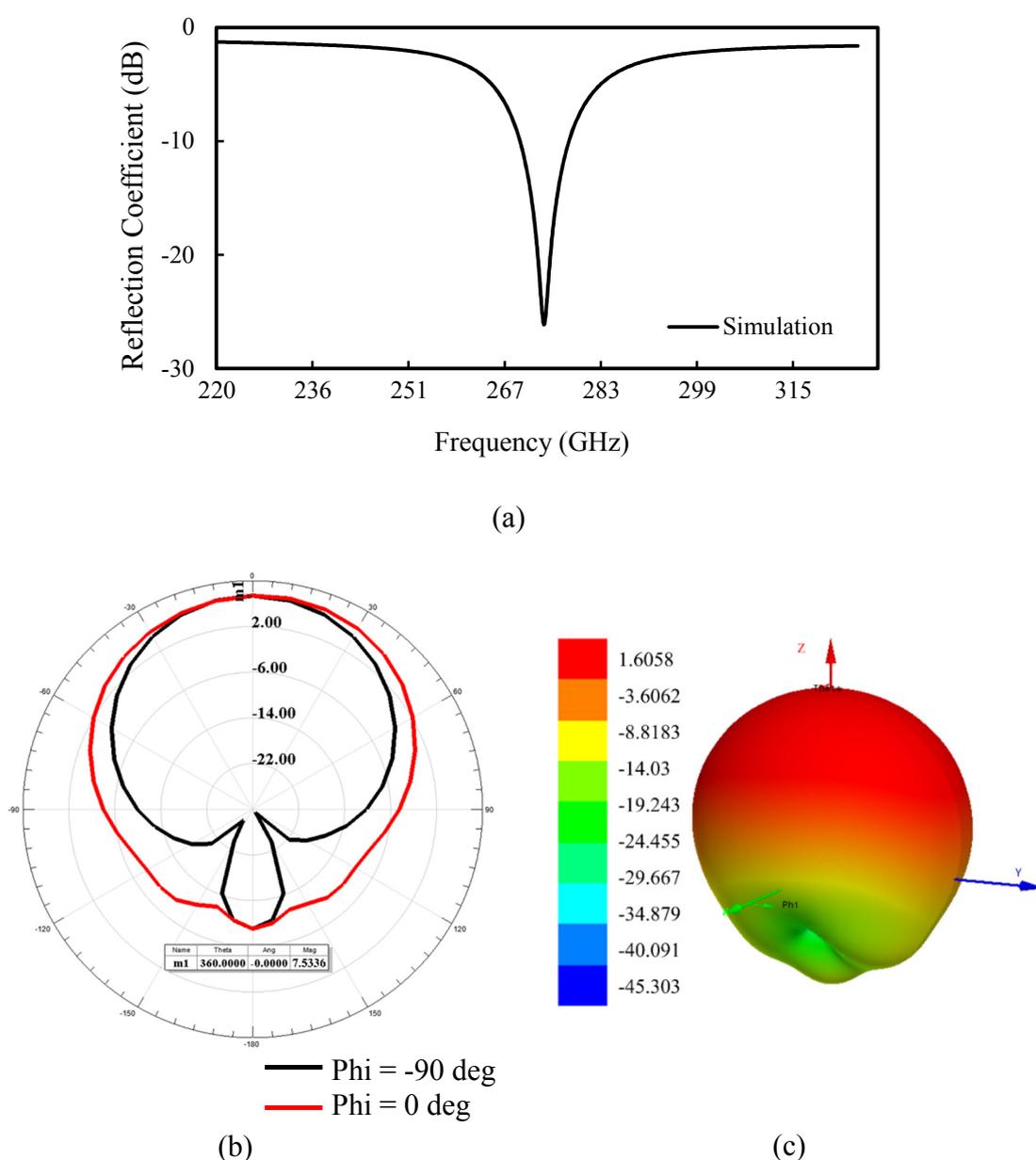
#### Rectangular patch antenna

The 3D model of a single rectangular patch antenna on GaN-on-LR Si using the shielding technique is shown in Fig. 3.22. As mentioned earlier, the LR Si is shielded with SiN and a metal ground plane (Au). A BCB layer is used as a dielectric spacer between the patch and the ground plane. Design of the antenna was carried out in HFSS software, for which, width (W) and length (L) of the antenna was derived using the transmission line model (Section 3.8.1, Page 70). A dielectric height of 5  $\mu\text{m}$ , loss tangent of 0.02 and dielectric constant of 2.7 at 270 GHz (frequency window around 300 GHz) were the parameters used in the simulation of this antenna. Final length (L) and width (W) of the rectangular patch antenna was optimised to be 372  $\mu\text{m}$  and 333  $\mu\text{m}$  respectively, to make the antenna resonate at 270 GHz. The patch is fed through a 50  $\Omega$  feed line and the inset feed technique was used to match the edge of the antenna to it, Section 3.8.1, Page 70. A 50  $\Omega$  CPW to microstrip transition was added at the end of the feed line for measurement purpose. The dimensions of the CPW pads and feed line used were the same as the dimensions used in the design of previous 50  $\Omega$  BCB transmission line. Width and length of the inset feed was simulated to be 7  $\mu\text{m}$  and 15  $\mu\text{m}$  for better matching at 270 GHz.



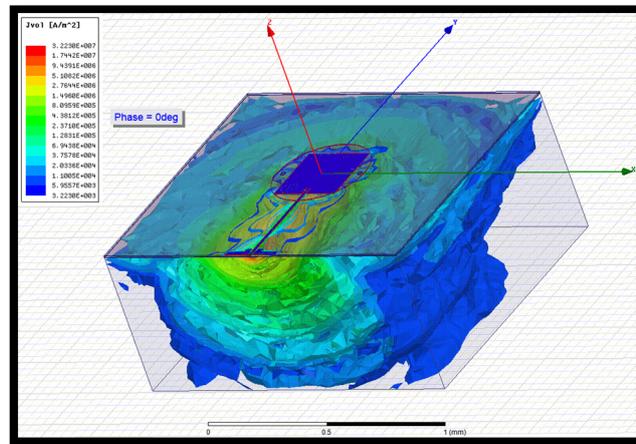
**Fig. 3.22:** 3D model of a rectangular patch antenna on BCB dielectric using shielding technique.

Fig. 3.23 (a) shows the simulated reflection coefficient of the rectangular patch antenna. A simulated reflection coefficient as low as -26 dB was achieved at 273 GHz. A bandwidth of 7 GHz ( $|S_{11}| < -11$  dB including insertion loss of the transmission line) was noted from the plot. Fig. 3.23 (b) and (c) shows the directivity and gain plot of the antenna. All values are obtained at resonant frequency. Maximum directivity at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  achieved was 7.5 dB, and maximum  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  gain reached was 1.6 dB. In addition, radiation efficiency and front to back ratio of the antenna was determined using HFSS software. An efficiency of 24 % was achieved with front to back ratio of 17.8 dB. The performance demonstrated by the antenna is comparable with the performance of patch antenna simulated on a Roger substrate [3.29].

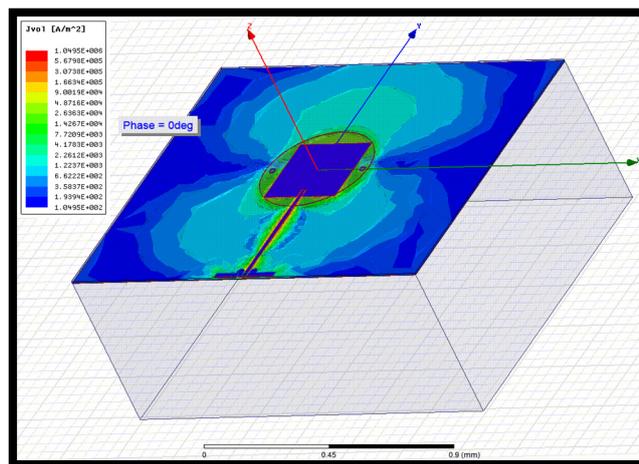


**Fig. 3.23:** Performance plot of single rectangular stack (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain [3.30] Copyright © 2016, IEEE.

Fig. 3.24 shows the electromagnetic simulation of volume current in the entire circuit with and without shielding at 273 GHz. As can be seen, with shielding, no current is lost in the dielectric substrate (LR Si). Whereas, without shielding there is a significant loss in current. This shows the viability of this technology at terahertz frequencies.



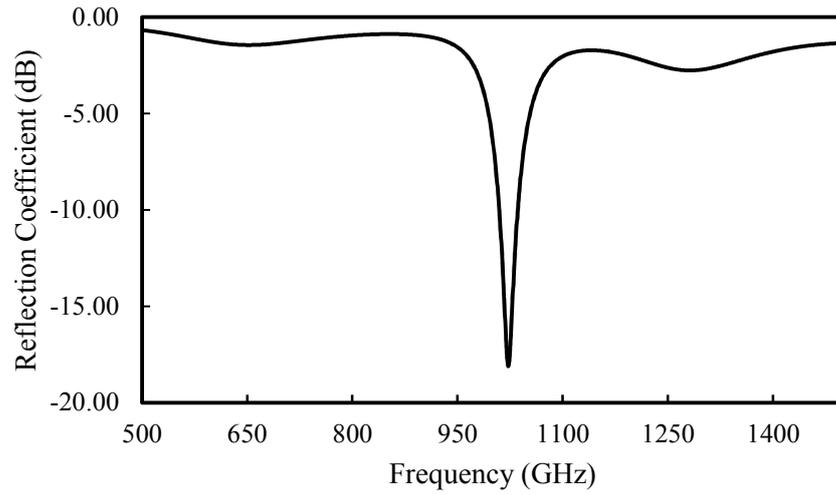
(a)



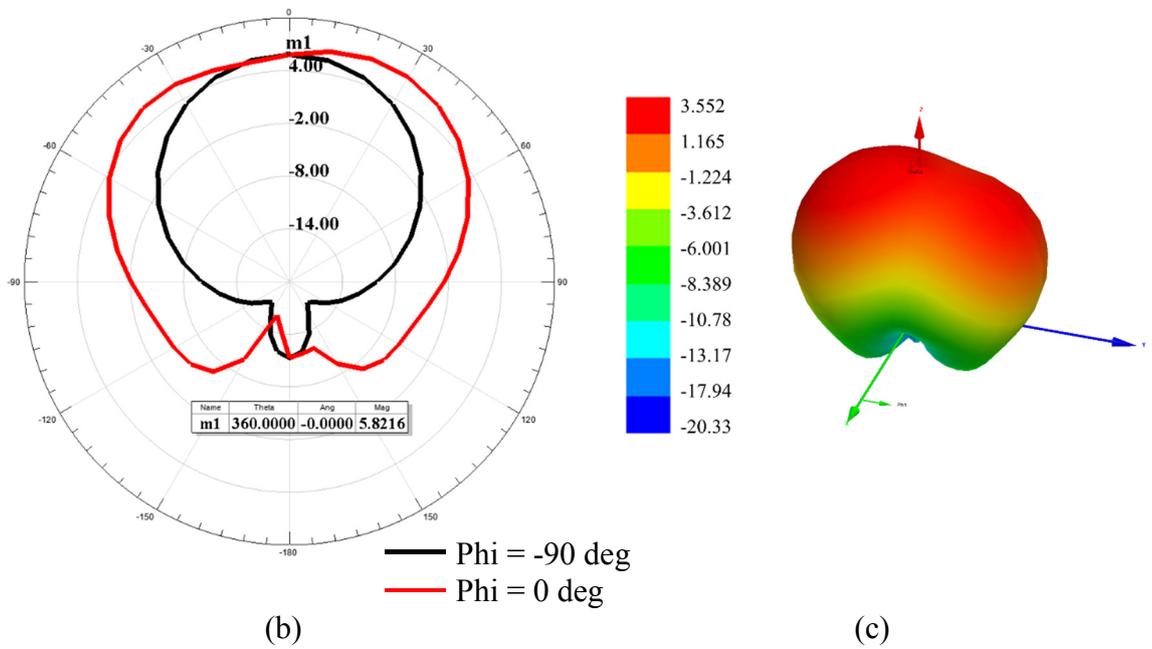
(b)

**Fig. 3.24:** Volumetric current in the substrate (a) without shielding (b) with shielding [3.30] [3.4] Copyright © 2016, IEEE.

Since BCB as a dielectric material performed very well at 270 GHz, it was further simulated in a 1 THz frequency patch to verify the performance of the antenna. The length and width of the antenna was simulated to be 92  $\mu\text{m}$  and 112  $\mu\text{m}$  respectively, and width and length of the inset feed was 5  $\mu\text{m}$  and 20  $\mu\text{m}$  respectively. Fig. 3.25 shows the performance of a 1 THz patch antenna on a BCB dielectric. A reflection coefficient as low as -17 dB was achieved. Directivity, gain, radiation efficiency and front to back ratio as high as 5.8 dB, 3.5 dB, 45 %, 22.9 dB was reached separately at  $0^0 < \theta < 360^0$  and  $\phi = -90^0$  and  $0^0$ .



(a)



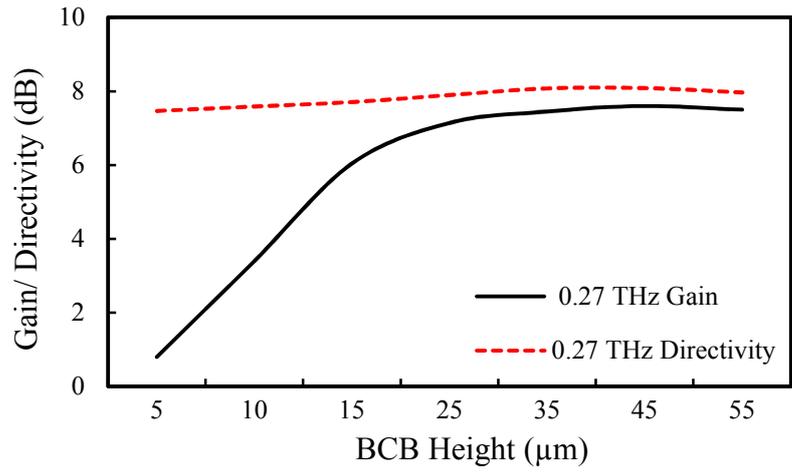
**Fig. 3.25:** Performance plot of 1 THz rectangular antenna (a) simulated and measured reflection coefficient (b) simulated directivity (c) simulated gain.

Table 3.1 shows a summary of antenna performance at both 270 GHz and 1 THz frequencies. Gain and radiation efficiency of 1 THz patch antenna increased twice compared to 270 GHz patch, whereas directivity decreased by 2 dB. The overall improved performance is explained below by the dependency of patch performance at certain operating frequency on the dielectric height.

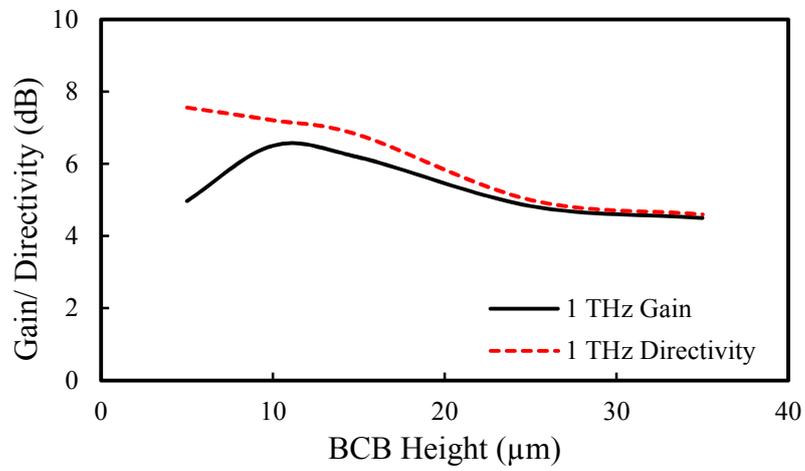
	270 GHz	1000 GHz
Reflection Coefficient (dB)	-26	-17
Bandwidth (GHz) ( $ S_{11}  < -10$ )	7	24
Directivity (dB)	7.5	5.8
Gain (dB)	1.6	3.5
Radiation Efficiency (%)	24	45
Front to back ratio (dB)	17.8	22.9

**Table 3.1:** Simulated performance of a 270 GHz and 1 THz rectangular patch antenna.

Fig. 3.26 shows a study of change in directivity and gain with BCB height for a 270 GHz and 1 THz frequency patch. To achieve a gain of 7.5 dB at 270 GHz, the BCB thickness required was 35  $\mu\text{m}$ , whereas at 1 THz this gain is achieved with a BCB thickness of 10  $\mu\text{m}$ . Unfortunately, the 1 THz design was not fabricated due to the repeatability issues in the fabrication process and difficulty in achieving a BCB thickness of more than 5  $\mu\text{m}$ .



(a)

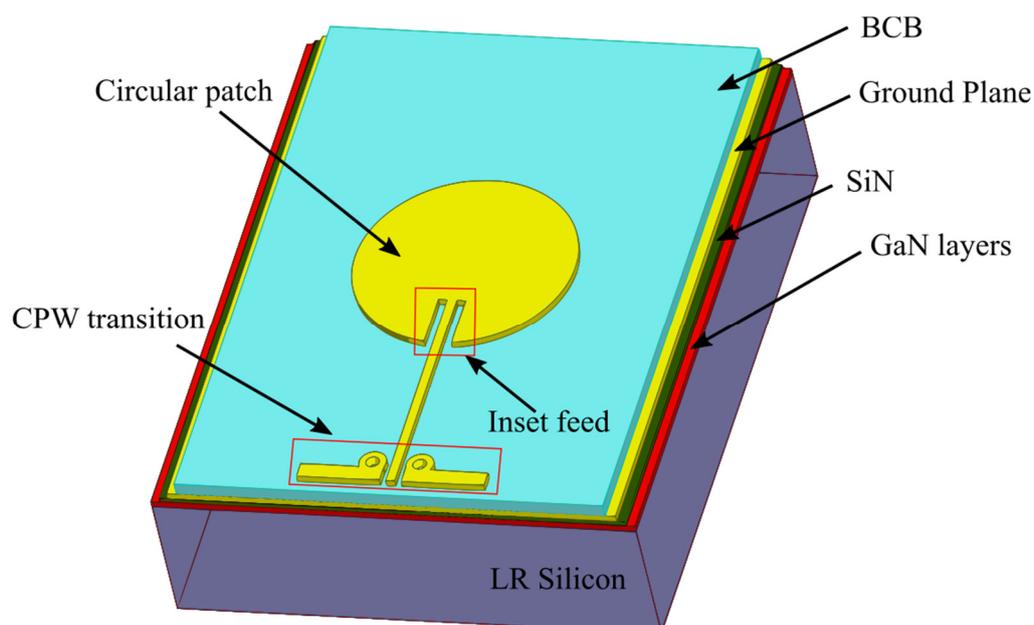


(b)

**Fig. 3.26:** Plot of change in gain/directivity with BCB height (a) At 270 GHz (b) At 1 THz [3.30] Copyright © 2016, IEEE.

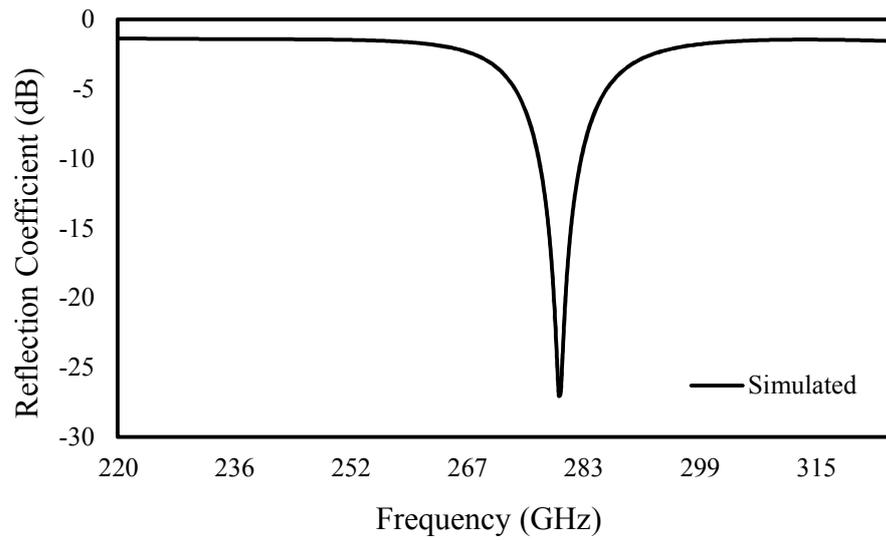
## Circular patch antenna

The 3D model of the circular patch antenna on the BCB is shown in the Fig. 3.27. Radius of the circular patch was calculated using equations in Section 3.8.2, Page 75 and optimised using HFSS software to be 200  $\mu\text{m}$ , for achieving resonance at 270 GHz (frequency window around 300 GHz). The inset feed width and length was simulated to be 13  $\mu\text{m}$  and 85  $\mu\text{m}$ , respectively. The dimensions of CPW pads and feed line is the same as the prior BCB transmission line design.

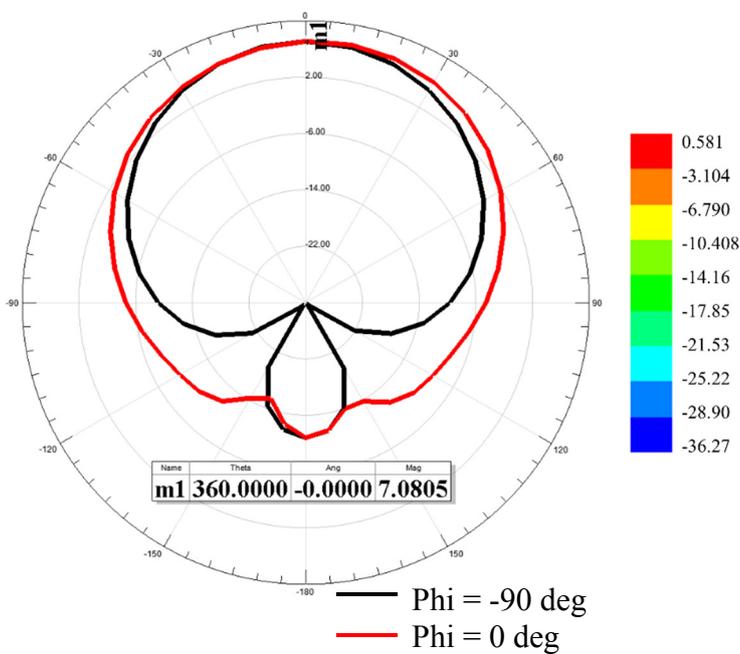


**Fig. 3.27:** 3D model of a circular patch antenna on GaN-on LR Si using shielding technique.

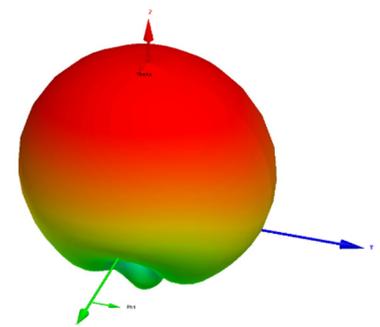
Fig. 3.28 shows the performance of the circular patch antenna. A simulated reflection coefficient as low as -27 dB was achieved. Maximum directivity of 7 dB and gain of 0.58 dB at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  was reached at resonant frequency. Radiation efficiency and front to back ratio presented by the devices was 22 % and 19.65 dB respectively. Table 3.2 shows the summary of circular antenna performance. Since the performance of circular patch was not good at 270 GHz, it was not simulated further at 1 THz.



(a)



(b)



(c)

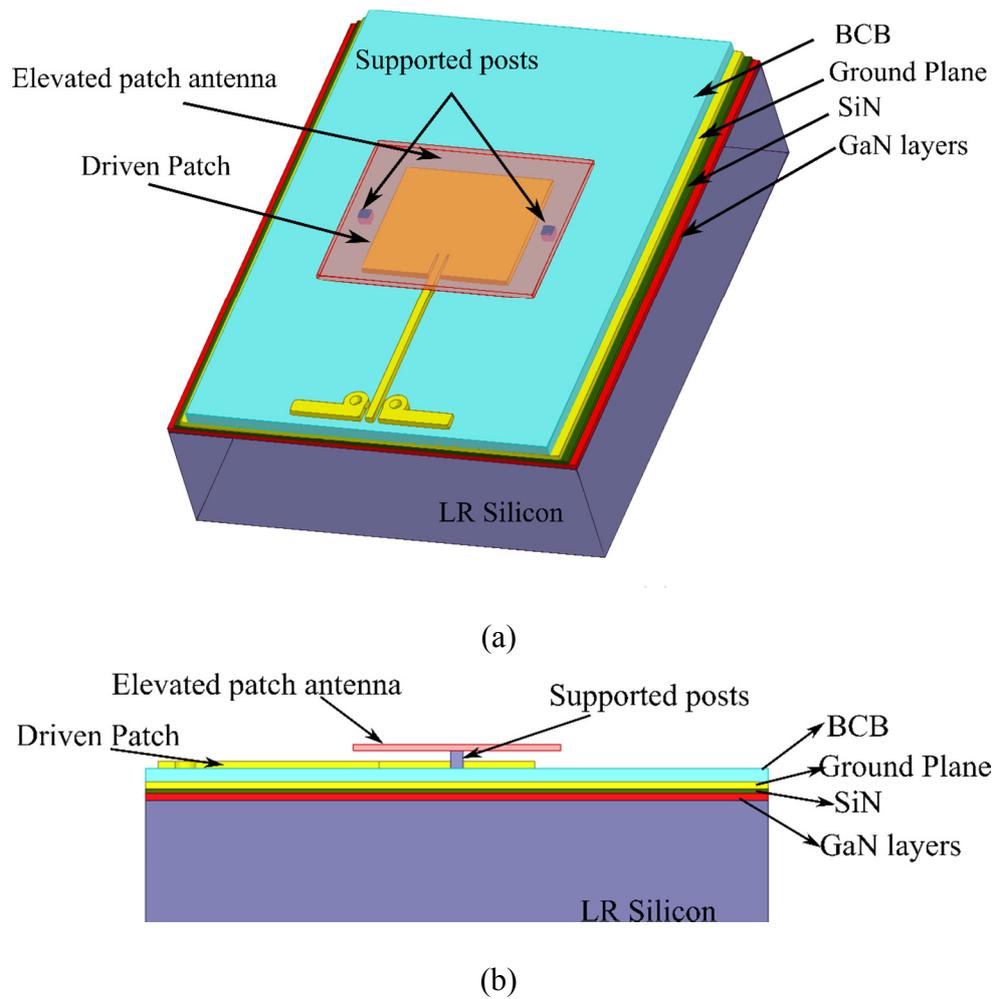
**Fig. 3.28:** Performance plot of circular patch (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

	270 GHz
Reflection Coefficient (dB)	-24
Bandwidth (GHz) ( $ S_{11}  < -10$ )	5
Directivity (dB)	7
Gain (dB)	0.58
Radiation Efficiency (%)	22
Front to back ratio (dB)	19.65

**Table 3.2:** Simulated performance of a 270 GHz circular patch antenna.

### Stack Antenna

In this work, three variants of stack antenna (Double rectangular stack, double circular stack and rectangular-circular stack antenna) were designed and compared. A 3D plot of a double rectangular stack antenna is shown in the Fig. 3.29. The driven patch is designed on a BCB, whereas the elevated (parasitic) patch is raised in air about 6  $\mu\text{m}$  (fabrication tolerances) above the substrate using two square 19  $\mu\text{m} \times 19 \mu\text{m}$  gold posts at each end of the patch. Dimensions of the driven patch and elevated patch were calculated using equations in Section 3.8.1 (Page 70) and Section 3.8.2 (Page 75) by parameters of the BCB dielectric ( $\epsilon_r=2.6$ ,  $\delta=0.02$ ) and air dielectric ( $\epsilon_r=1$ ,  $\delta=0$ ) separately for stack simulation. The sizes were then optimised using HFSS software to alter the resonant frequency of antenna at 270 GHz (frequency window around 300 GHz), Table 3.3 shows this. Dimensions of the CPW pads and microstrip feed line were the same as those for the BCB transmission line design. This is the first time such a configuration has been studied at terahertz frequencies on GaN-on-LR Si.



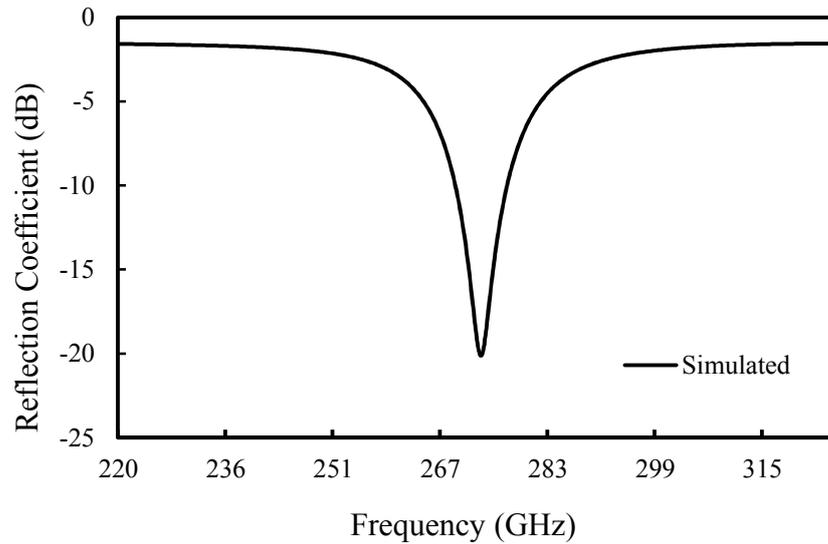
**Fig. 3.29:** 3D model of double rectangle stack antenna (a) Top view (b) Side view [3.4]

Copyright © 2016, IEEE.

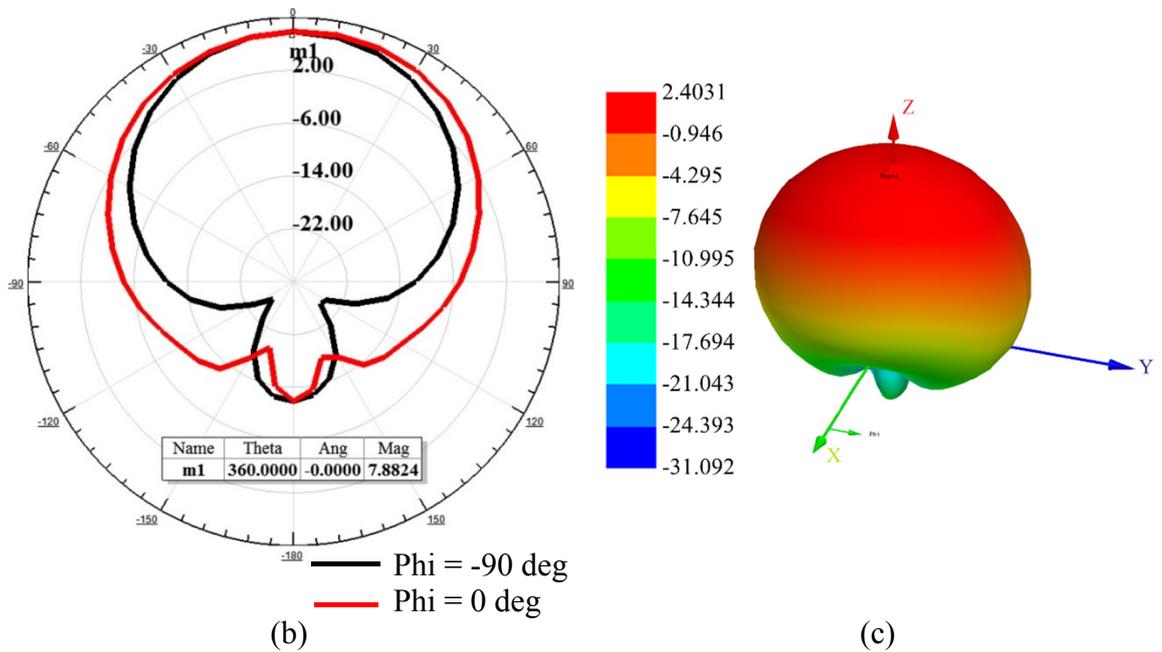
Antenna type	Driven patch	Parasitic patch	Inset feed
Double Rectangular	$373 \times 308 \mu\text{m}$ (W×L)	$500 \times 308 \mu\text{m}$ (W×L)	$4 \times 45 \mu\text{m}$ (W×L)

**Table 3.3:** Simulated dimensions for double rectangular stack antenna.

The simulated performance of the double rectangular stack antenna is shown in Fig. 3.30. The antenna resonated at 273 GHz with a return loss as low as -20.1 dB. Antenna radiation performance, directivity of 7.8 dB and gain of 2.4 dB at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  was achieved at resonant frequency. Further, radiation efficiency of 29 %, and front to back ratio of 20 dB was observed.

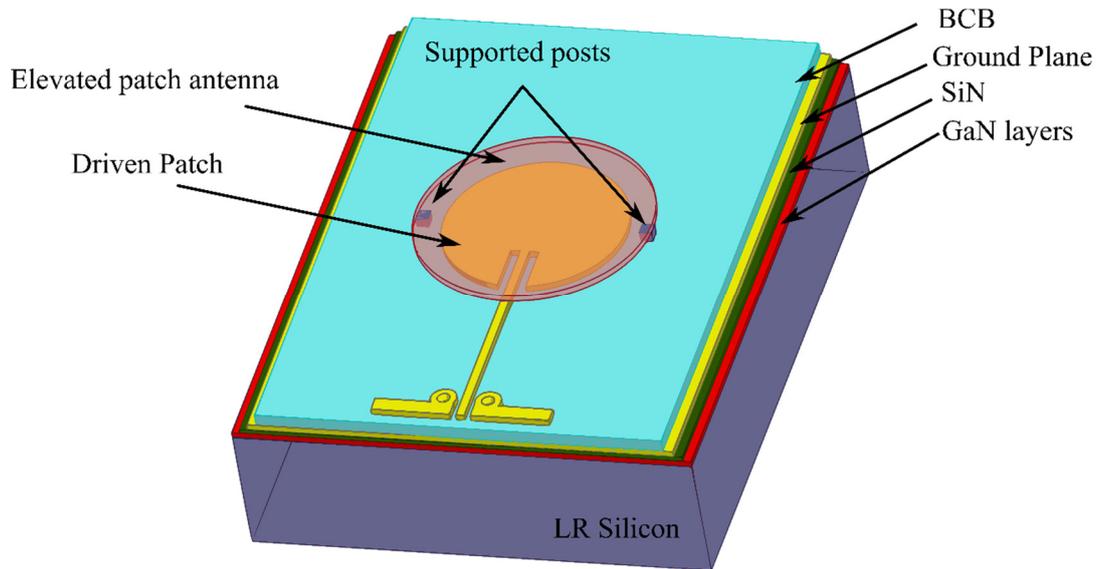


(a)



**Fig. 3.30:** Performance plot of double rectangular stack (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain [3.30] Copyright © 2016, IEEE.

The 3D model for a second variant of stack antenna is displayed in Fig. 3.31. The driven patch and elevated patch are both circular in shape and radius of each was calculated using equations in Section 3.8.2, Page 75 by parameters of BCB dielectric ( $\epsilon_r=2.6$ ,  $\delta=0.02$ ) and air dielectric ( $\epsilon_r=1$ ,  $\delta=0$ ) respectively. The elevated antenna was supported by two square  $19 \mu\text{m} \times 19 \mu\text{m}$  gold posts at each end of the patch to achieve an elevation height of  $6 \mu\text{m}$ . Table 3.4 shows the dimensions used for resonating the double circular stack antenna at 270 GHz. Dimensions of the CPW pads and microstrip line used for simulation were the same as the dimensions of the prior BCB transmission line design.

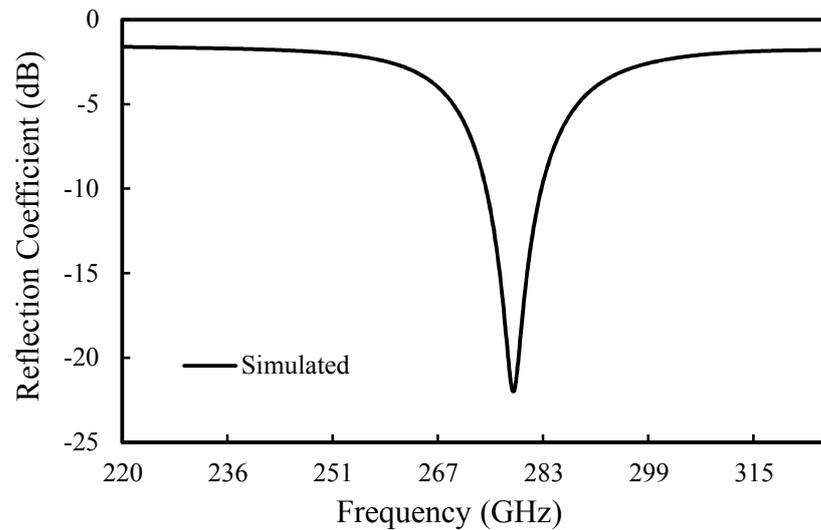


**Fig. 3.31:** 3D model of double circular stack antenna [3.30] Copyright © 2016, IEEE.

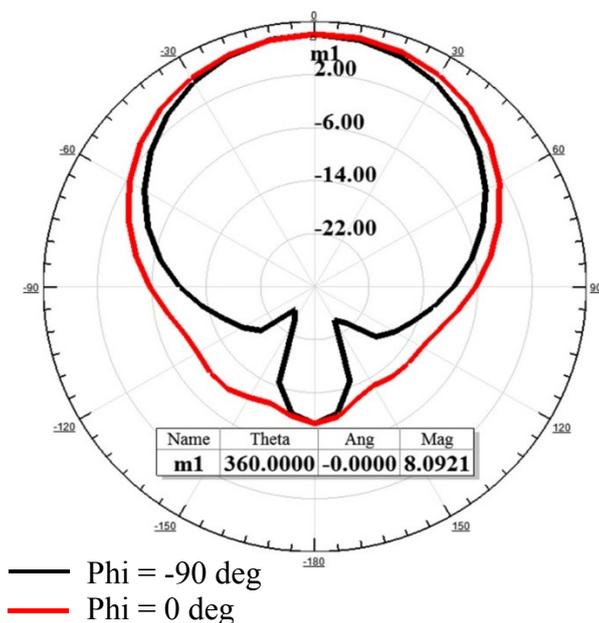
Antenna type	Driven patch	Parasitic patch	Inset feed
Double Circular	182 $\mu\text{m}$ (radius)	220 $\mu\text{m}$ (radius)	5 $\times$ 45 $\mu\text{m}$ (W $\times$ L)

**Table 3.4:** Simulated dimensions for double circular stack antenna.

Fig. 3.32 shows the performance of the double circular antenna stack. The resonance of the antenna was achieved at 279 GHz with reflection coefficient as low as -21.95 dB. Maximum directivity and gain reached at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  using this antenna variant was 8.1 dB and 2.5 dB at resonant frequency. The radiation efficiency and front to back ratio observed was 30 % and 18 dB.

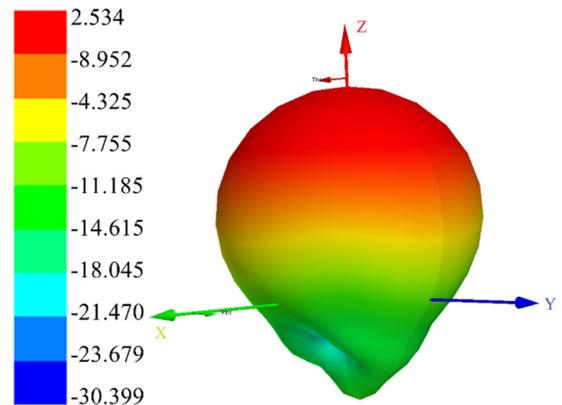


(a)



— Phi = -90 deg  
 — Phi = 0 deg

(b)

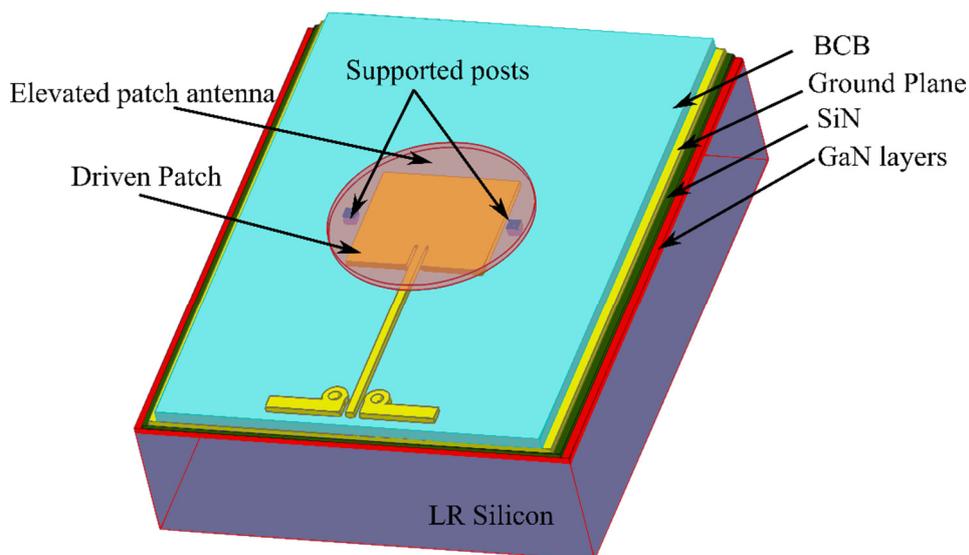


(c)

**Fig. 3.32:** Performance plot of double circular stack (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain [3.30] Copyright © 2016, IEEE.

The 3D diagram of a third variant, rectangular-circular stack antenna is shown in Fig. 3.33. The driven patch is rectangular, whereas the elevated patch is circular in shape. The length and width of the driven patch was calculated using equations in Section 3.8.1, Page 70 by parameters of the BCB dielectric ( $\epsilon_r=2.6$ ,  $\delta=0.02$ ), and radius of the elevated patch was calculated using equations in Section 3.8.2, Page 75 by parameters of air dielectric ( $\epsilon_r=1$ ,  $\delta=0$ ). The elevated antenna was supported by two square  $19 \mu\text{m} \times 19 \mu\text{m}$  gold posts at each end of the patch to achieve an elevation height of  $6 \mu\text{m}$ . Table 3.5 shows the dimensions used for resonating the rectangular-circular stack antenna at 270 GHz. Dimensions of the

CPW pads and microstrip line used for simulation were the same as the dimensions of the prior BCB transmission line design.

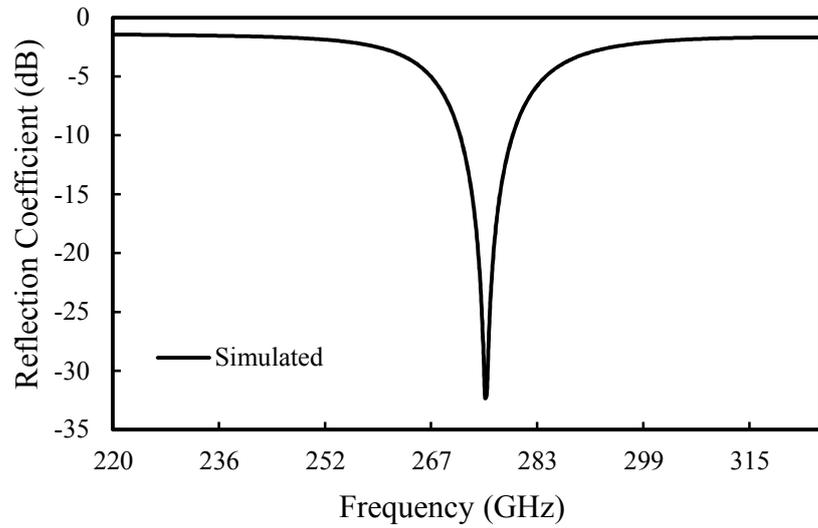


**Fig. 3.33:** 3D model of rectangular-circular stack antenna.

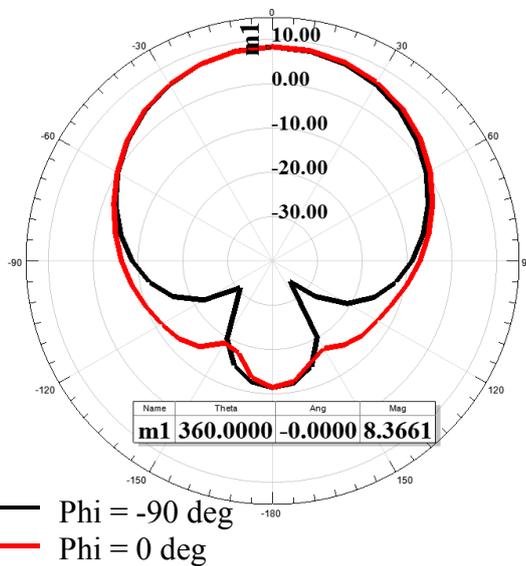
Antenna type	Driven patch	Parasitic patch	Inset feed
Rectangular-Circular	$310 \times 320 \mu\text{m}$ (W×L)	$225 \mu\text{m}$	$4 \times 75 \mu\text{m}$ (W×L)

**Table 3.5:** Simulated dimensions for rectangular-circular stack antenna.

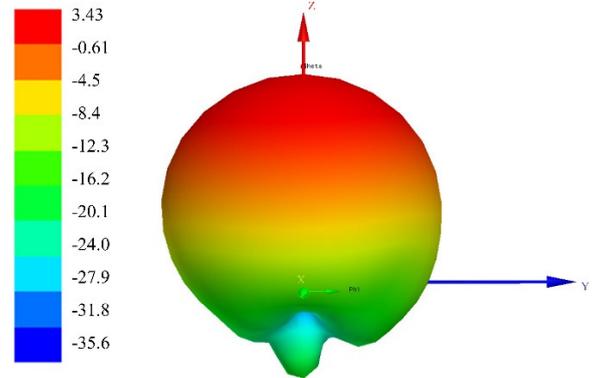
The simulated performance of the rectangular-circular stack antenna is shown in Fig. 3.34. The antenna resonated at 275 GHz with return loss as low as -32.3 dB. Antenna radiation performance, directivity of 8.3 dB and gain of 3.4 dB at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  was achieved at resonant frequency. Further, radiation efficiency of 32 %, and front to back ratio of 21 dB was observed for the rectangular-circular stack antenna.



(a)



(b)



(c)

**Fig. 3.34:** Performance plot of rectangular- circular stack (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain [3.30] [3.4].

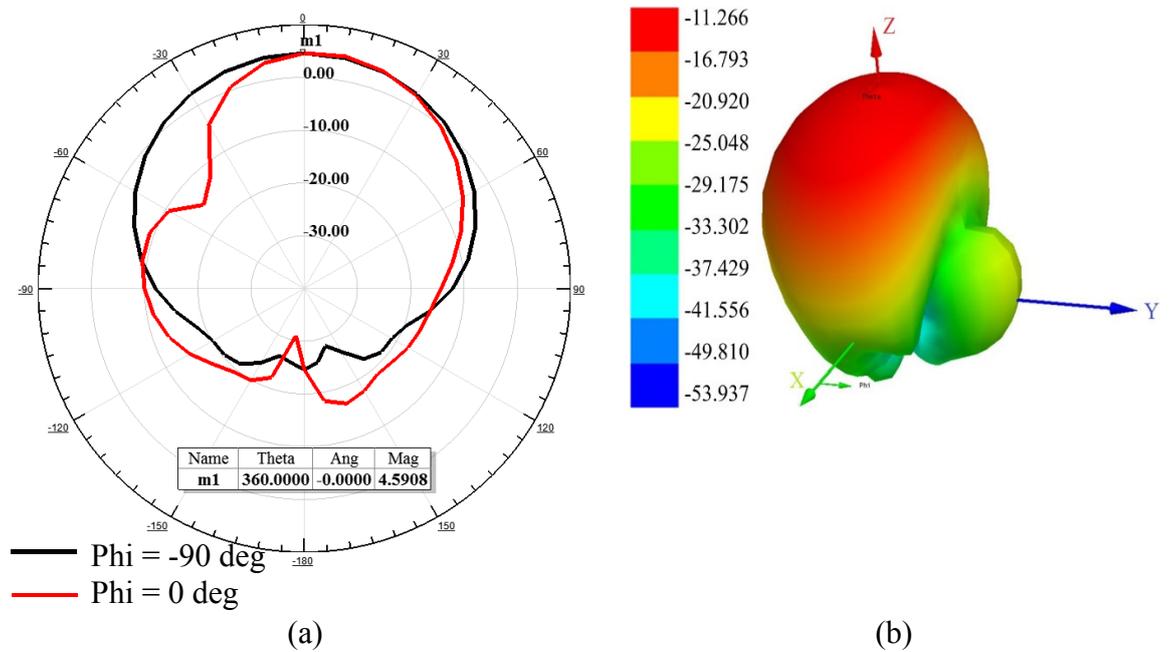
Table 3.6 shows a summary of the stack antenna performance, comparing each with a single rectangular antenna at 270 GHz. By comparison, the rectangular-circular stack performed better due to better coupling between the driven patch and parasitic patch and there was a good improvement of about 51.4 % in the gain and 33.3 % in the radiation efficiency over a single microstrip antenna, which achieved 1.6 dB and 24 %. The increase in performance is due to the use of air as a second dielectric, which provides zero loss to overall performance. Comparing design flexibility and ease of optimization, rectangular-circular stack antenna was easier to design as it had three degree of freedom- length and width of driven patch and radius of the parasitic patch for the optimisation. The other two stack variants had (width

and length or radius) one of the parameters for optimization. Further, bandwidth achieved by the stack configurations was almost same as the single rectangular antenna, since resonant frequency of both driven and parasitic patch was designed to resonate at same frequency.

	Single rectangular antenna	Double rectangle stack antenna	Double circular stack antenna	Rectangle circular stack antenna
Reflection Coefficient (dB)	-26	-20.1	-21.95	-32.3
Bandwidth (GHz) ( $ S_{11}  < -11$ )	7	6	7	7
Directivity (dB)	7.5	7.8	8.1	8.3
Gain (dB)	1.6	2.4	2.5	3.4
Radiation Efficiency (%)	24	29	30	32
Front to back ratio (dB)	17.8	20	18	21

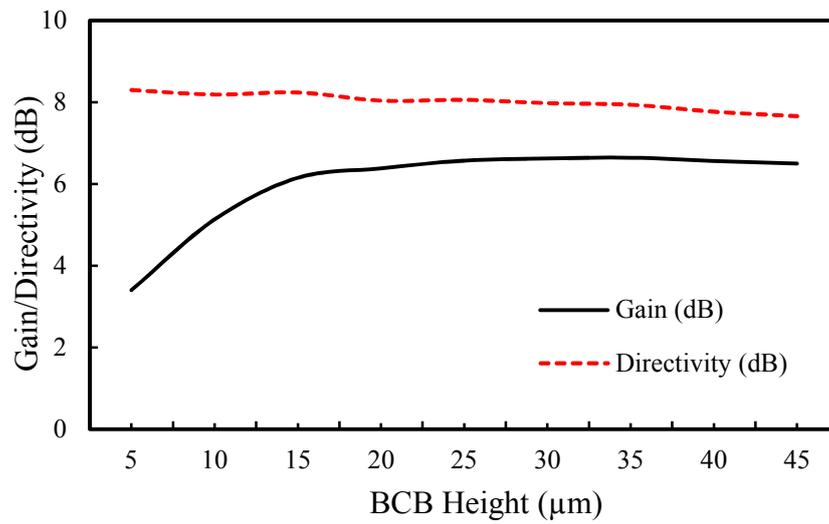
**Table 3.6:** Performance summary of all three stack antennas.

To evaluate the importance of using a low loss dielectric material for elevated patch, a double rectangular stack antenna was simulated using BCB as a second dielectric material in place of air. Fig. 3.35 shows the radiation performance of the antenna. Directivity of 4.5 dB and gain of -11.26 dB was achieved using this design. Reduction in the performance of the stack antenna design compared to the previous design was may be due to the charge degradation at the surface of the driven patch and relatively low mutual coupling between the first and second patch [3.31].

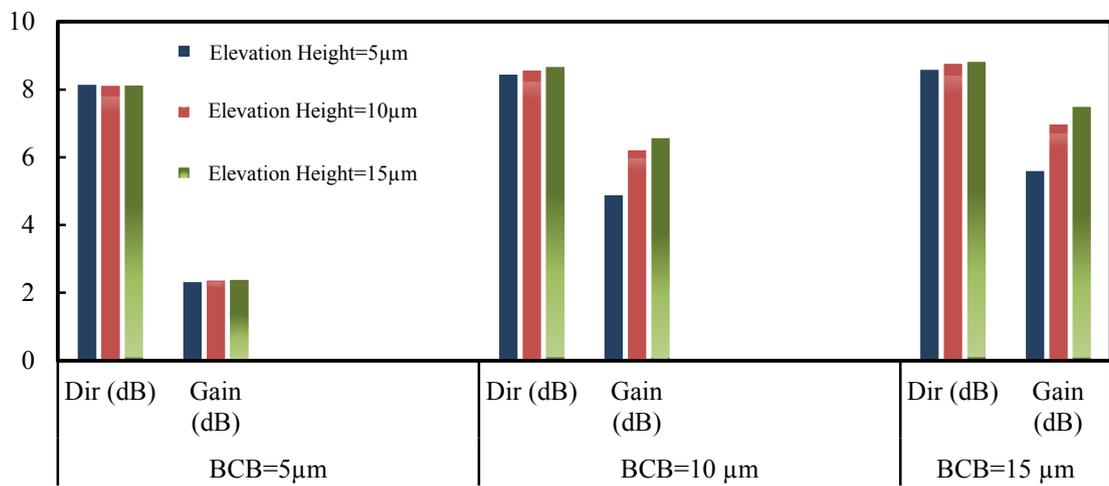


**Fig. 3.35:** Performance of BCB as second dielectric/elevated dielectric material (a) Directivity (b) Gain [3.30] Copyright © 2016, IEEE.

To estimate the effect of variation in thicknesses of the two dielectric materials used on the performance of the stack antenna, double-rectangular stack antenna were simulated by changing the BCB height while fixing the air height and vice versa. Fig. 3.36 (a) shows the change in gain and directivity when the BCB height is varied and stack height is fixed at 6  $\mu\text{m}$ . It can be observed that as the BCB height changes, the directivity is maintained within  $\pm 0.5$  dB. However, gain increased by 50 % at 30  $\mu\text{m}$  height (6.7 dB). Fig. 3.36 (b) shows the change in gain and directivity for fixed values of BCB height (5, 10, 15  $\mu\text{m}$ ) and varied elevated distance. Directivity did not change significantly yet gain increased promptly from 5  $\mu\text{m}$  BCB and elevation height (2 dB) to 15  $\mu\text{m}$  BCB and elevation height (8 dB) due to better coupling between the patch and the ground plane. A final height of 5  $\mu\text{m}$  (minimum height) was chosen for simulation of the BCB dielectric as a trade-off between antenna performance, realisable CPW pad size and microstrip feed line size for measurement, within fabrication tolerances. For elevation, the height was limited to 6  $\mu\text{m}$  due of the issue of support posts collapsing.



(a)



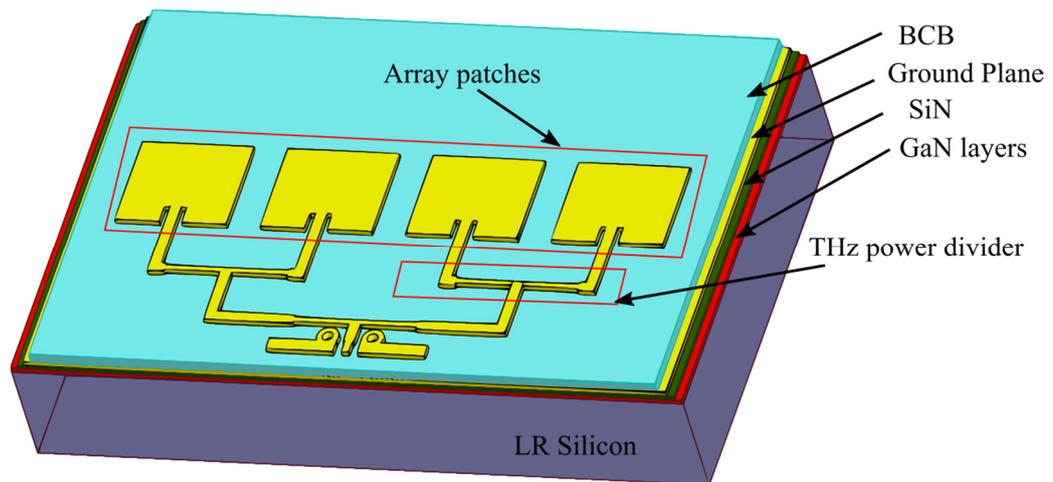
(b)

**Fig. 3.36:** Plot of change in gain/directivity of double-rectangular (a) with BCB height having elevation fixed at 6 μm (b) with fixed BCB heights and changing elevation height

[3.30] Copyright © 2016, IEEE.

## Array antenna

A 3D diagram of a 4×1 array antenna on BCB is shown in Fig. 3.37. Design of this antenna followed the theory of array antenna as discussed in Section 3.8.3, Page 76. Length and width of individual patches was simulated to be 372 by 333  $\mu\text{m}$  (W×L) with 64  $\mu\text{m}$  spacing between. The inter-element spacing between patches was simulated to be  $0.13 \lambda_0$  to avoid spurious radiation (grating lobes) in any direction other than the broadside direction i.e.  $\beta=0$ . This spurious radiation is caused by spacing antennas more than  $\lambda/2$  [3.5]. In this design, array patches are excited using a corporate feed network. This corporate feed network uses simple T-junction power dividers, discussed in Section 3.8.3, Page 76. The input impedance of the antenna was aimed to be 50  $\Omega$  and since, the power splitting was done in parallel, the characteristic impedance of the transmission line was 100  $\Omega$ . A quarter wavelength impedance transformer with 70.7  $\Omega$  characteristic impedance was used to convert back to 50  $\Omega$ . Table 3.7 shows the physical length and width of the different impedance transmission line used in the corporate feed network.



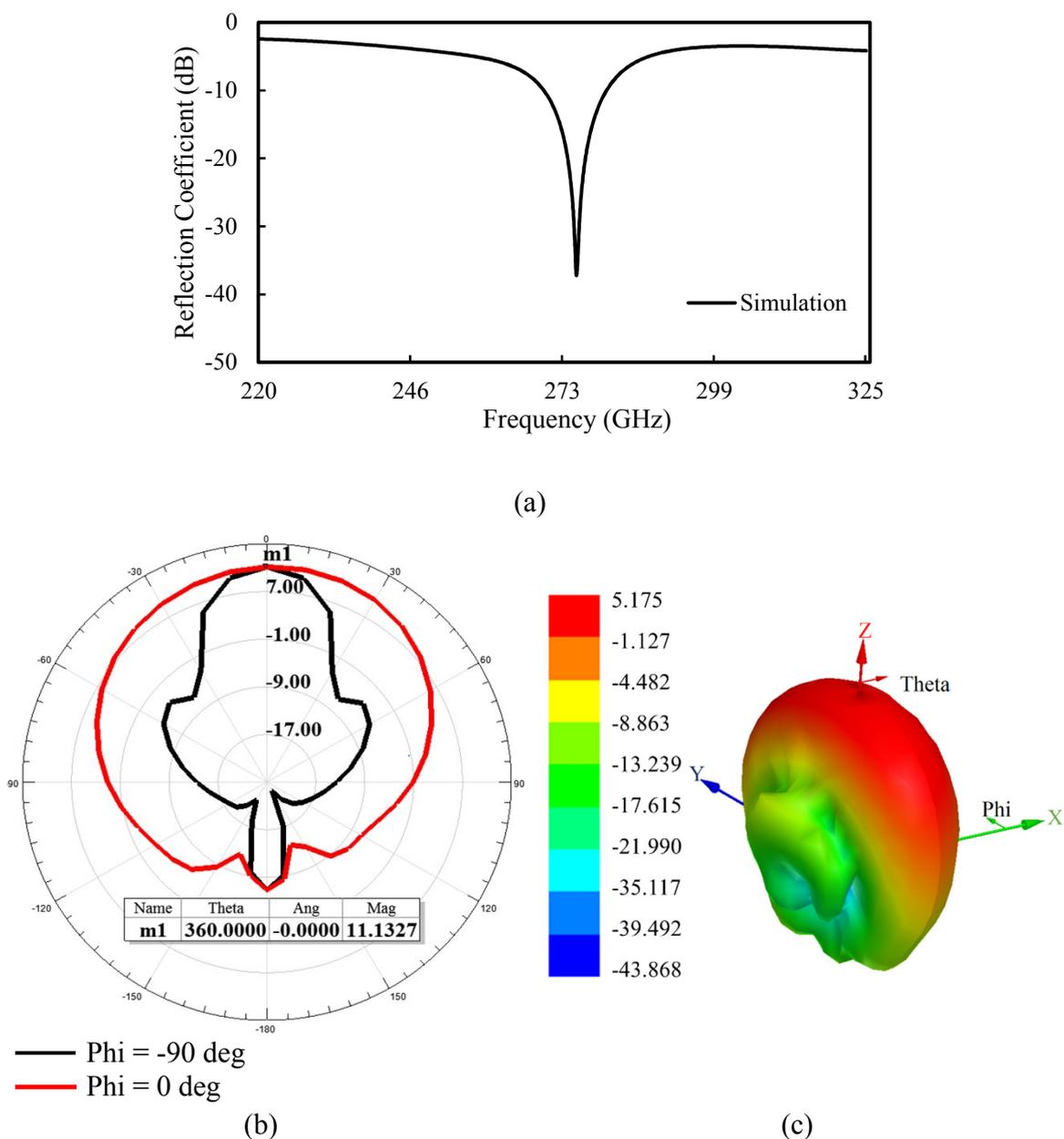
**Fig. 3.37:** 3D model of 4×1 array antenna.

Impedance ( $\Omega$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
50	14	172.4
70.71	7.5	177

**Table 3.7:** Width and length of different impedances transmission lines in power divider.

Fig. 3.38 shows the performance of this 4×1 array antenna. Simulation reflection coefficient as low as -37 dB was achieved at 275 GHz. The simulated return loss showed a bandwidth

of 9 GHz ( $S_{11} < -12$  dB including insertion loss of the transmission line), calculated from 270 GHz to 279 GHz. The directivity and gain of the simulated  $4 \times 1$  array were as high as 11.2 dB and 5.2 dB at  $0^\circ < \theta < 360^\circ$  and  $\phi = -90^\circ$  and  $0^\circ$  at resonant frequency (Table 3.8). In addition, radiation efficiency of 74 % was noted. Comparing to the radiation performance achieved by single rectangular antenna design (Section 3.9.2, Page 89), performance was doubled by the array configuration, due to mutual coupling of the patches.



**Fig. 3.38:** Performance plot of rectangular-circular stack (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain [3.32] Copyright © 2016, IEEE.

	4 × 1 array antenna
Reflection Coefficient (dB)	-37
Bandwidth (GHz) ( $ S_{11}  < -12$ )	9
Directivity (dB)	11.2
Gain (dB)	5.2
Radiation Efficiency (%)	74
Front to back ratio (dB)	23.32

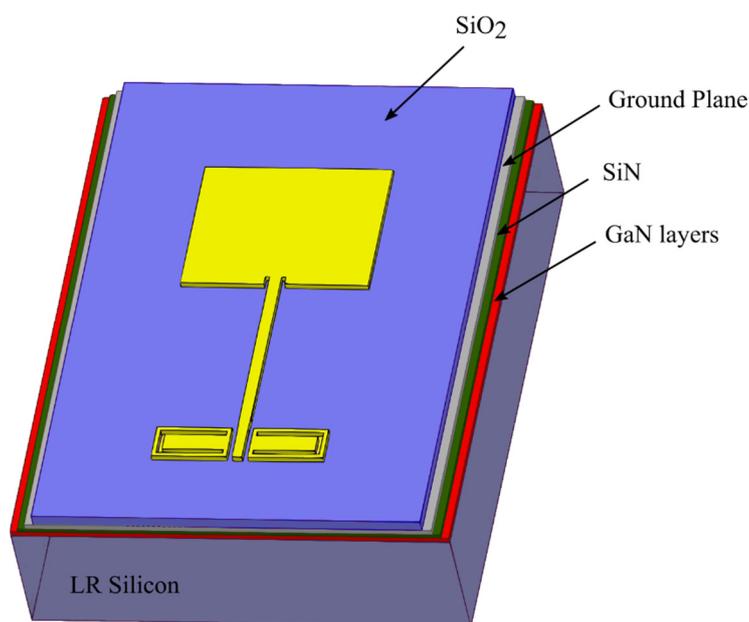
**Table 3.8:** Performance summary of the 4 × 1 array antenna.

Further simulation of the array configuration revealed that as the number of elements in the array increased (greater than 64 elements), the losses from the microstrip feed lines exceeded the antenna gain, resulting in diminishing returns. Applications which requires higher directivity and low gain at terahertz can benefit from this array technology.

### 3.9.3 Simulation of antenna on SiO<sub>2</sub>

#### Rectangular patch

The 3D diagram of a single rectangular antenna on GaN-on-LR Si using a shielding technique and SiO<sub>2</sub> as the dielectric is shown in Fig. 3.39. In this, the LR Si substrate is shielded with SiN and an Al ground plane. A SiO<sub>2</sub> dielectric spacer was used to separate the distance between the patch and the ground plane. Simulations were carried out in HFSS software, for which, width and length of the patch antenna was calculated using equations in Section 3.8.1, Page 70. A dielectric height of 10  $\mu\text{m}$ , dielectric constant of 4, and loss tangent of 0.04 at 300 GHz was used for the simulation of the antenna. Final width and length of the antenna was optimised to be 300 and 240  $\mu\text{m}$  respectively. The antenna was fed using a 50  $\Omega$  microstrip line and the inset feed technique was used to match this with a 50  $\Omega$  transmission line. For measurement purpose, GSG (Ground-Signal-Ground) pads were required, which was designed using a 50  $\Omega$  via-hole CPW to microstrip transitional pad. Table 3.9 shows the dimensions of the antenna, line, and GSG pads.

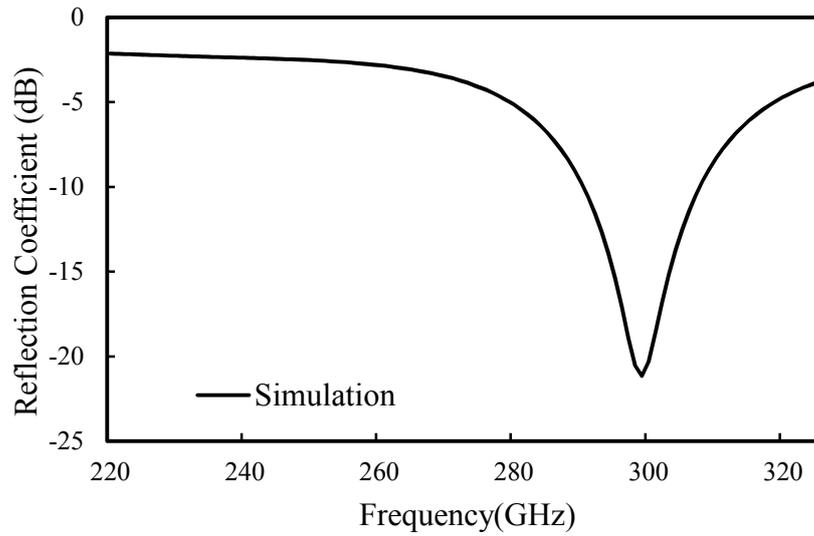


**Fig. 3.39:** 3D diagram of the 300 GHz rectangular patch antenna on SiO<sub>2</sub>.

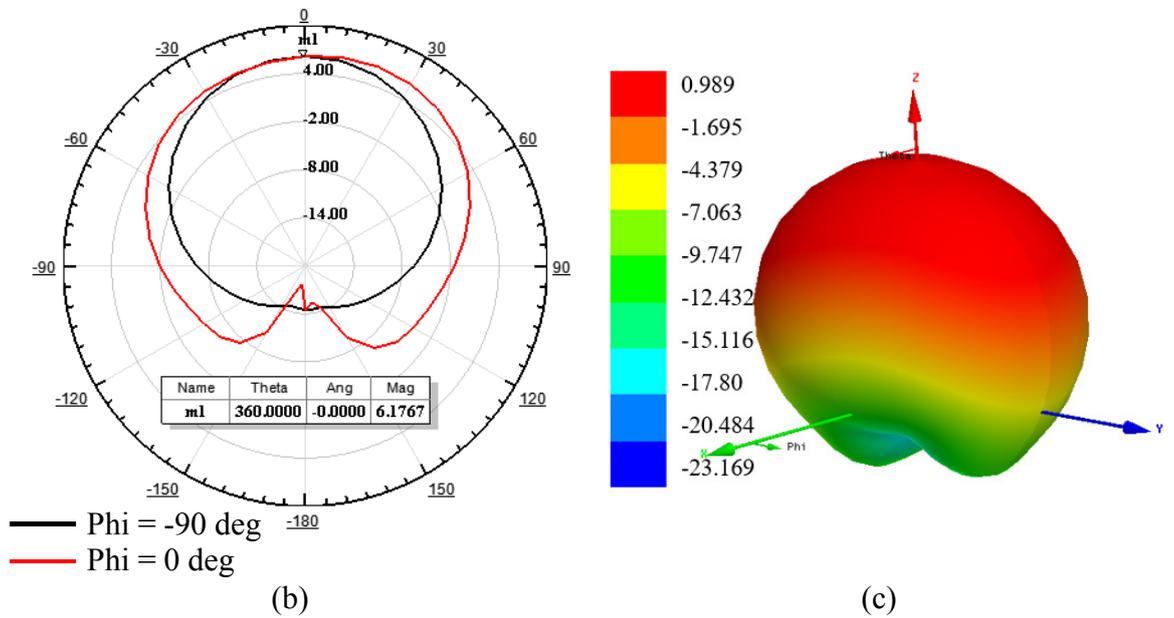
	Dimensions
Antenna	$300 \times 240 \mu\text{m}$ (W×L)
Inset feed	$7 \times 15 \mu\text{m}$ (W×L)
Microstrip line	$19 \times 300 \mu\text{m}$ (W×L)
CPW pads (GSG)	$120, 16, 120 \mu\text{m}$ (Gap- $9\mu\text{m}$ ) $\times 60 \mu\text{m}$ (W×L)

**Table 3.9:** Dimensions used for the simulation of the 300 GHz rectangular patch antenna.

Fig. 3.40 (a) shows the simulated reflection coefficient of the rectangular patch antenna. Simulated reflection coefficient as low as -21.1 dB was achieved at 300 GHz. A bandwidth of 12 GHz ( $|S_{11}| < -12$  dB including insertion loss of the transmission line) was noted from the plot. Fig. 3.40 (b) and (c) shows the directivity and gain radiation pattern at  $0^\circ < \theta < 360^\circ$  and  $\phi = -90^\circ$  and  $0^\circ$  at 300 GHz respectively. Maximum directivity achieved was 6.17 dB and maximum gain reached was 0.98 dB at resonant frequency. In addition, an efficiency of 28.51 % was achieved and front to back ratio of 17.8 dB.



(a)



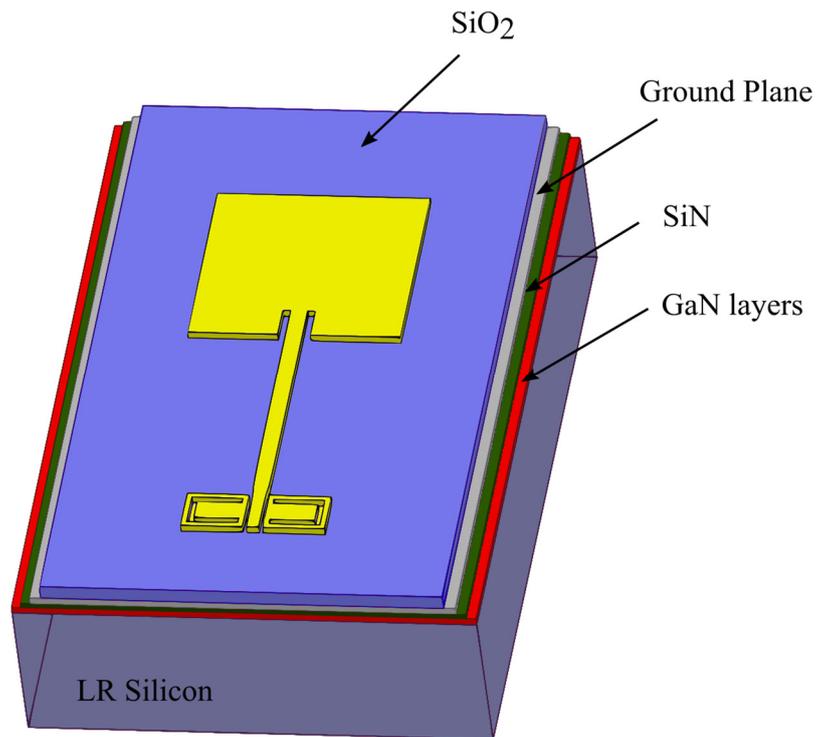
**Fig. 3.40:** Performance plot of 300 GHz single rectangular patch (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

Table 3.10 shows a comparison between a single rectangular antenna on BCB and on SiO<sub>2</sub>. Radiation (directivity and gain) performance of the rectangular antenna on BCB achieved was much better than on SiO<sub>2</sub>, this is due to the higher loss tangent presented by the SiO<sub>2</sub> at 300 GHz. However, parameters like bandwidth, front to back ratio, and radiation efficiency achieved by antenna on SiO<sub>2</sub> was higher than on BCB due to the tightly bound fields created by higher dielectric constant. In addition, it can be observed that the back lobe in Fig. 3.40 is almost null compared to Fig. 3.23, Page 90, for the same reason and thicker dielectric material.

	BCB	SiO <sub>2</sub>
Reflection Coefficient (dB)	-26	-21.1
Bandwidth (GHz) ( $ S_{11}  < -11$ )	7	12
Directivity (dB)	7.5	6.17
Gain (dB)	1.6	0.98
Radiation Efficiency (%)	24	28.51
Front to back ratio (dB)	17.8	22.86

**Table 3.10:** Comparison table for performance of simulated rectangular patch antenna on BCB with SiO<sub>2</sub> dielectric.

The rectangular antenna was also simulated at 650 GHz to evaluate the antenna performance. Fig. 3.41 shows the 3D model of this. Dimensions of the design are listed in Table 3.11.

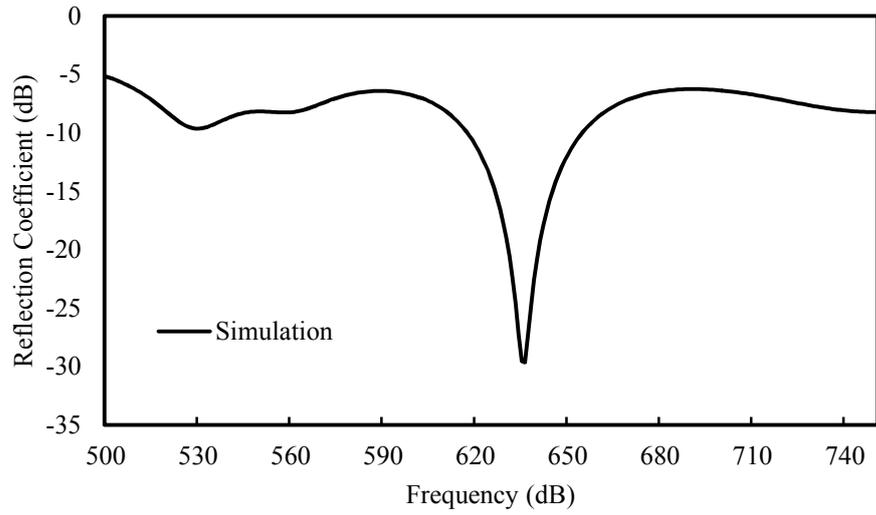


**Fig. 3.41:** 3D diagram of the 650 GHz rectangular patch antenna on SiO<sub>2</sub>.

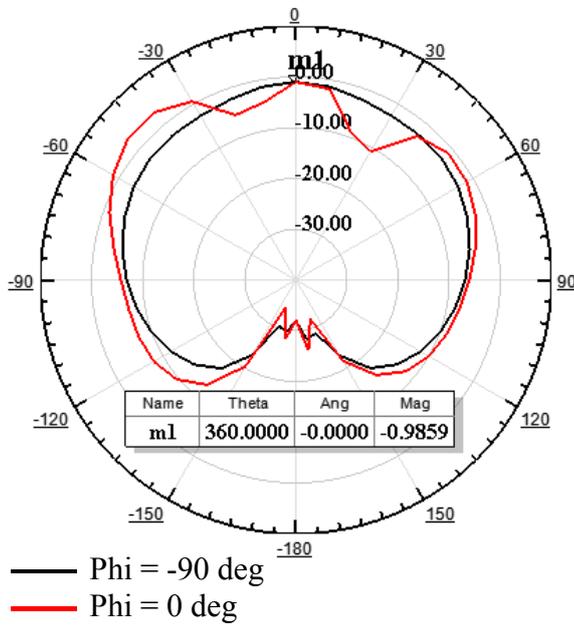
	Dimensions
Antenna	275 × 260 μm (W×L)
Inset feed	10 × 45 μm (W×L)
Microstrip line	22 × 300 μm (W×L)
CPW pads (GSG)	80, 16, 80 μm (Gap-5μm) × 60 μm (W×L)

**Table 3.11:** Dimensions used for the simulation of the 650 GHz rectangular patch antenna.

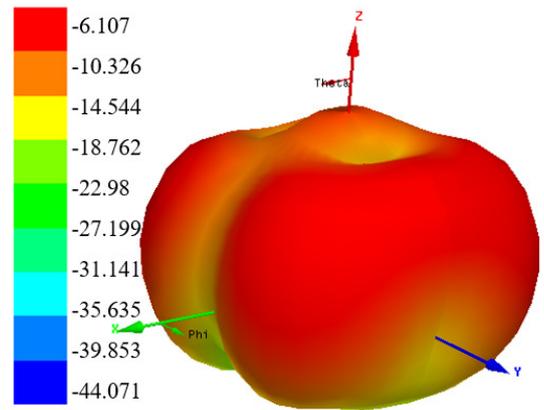
Fig. 3.42 shows the performance of the 650 GHz rectangular patch antenna. Simulation reflection coefficient as low as -29.5 dB was achieved. Maximum directivity of -0.98 dB and gain of -6.10 dB was reached at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$ . Radiation efficiency and front to back ratio presented by the devices were 10 % and 9.84 dB respectively. Table 3.12 shows the summary of rectangular antenna performance. Simulated results show that shielding technology using SiO<sub>2</sub> as a dielectric combined with a microstrip rectangular antenna design at 650 GHz is very lossy. In addition, the antenna insertion loss is quite high due to the SiO<sub>2</sub> transmission line loss at 650 GHz, Section 3.9.1, Page 83.



(a)



(b)



(c)

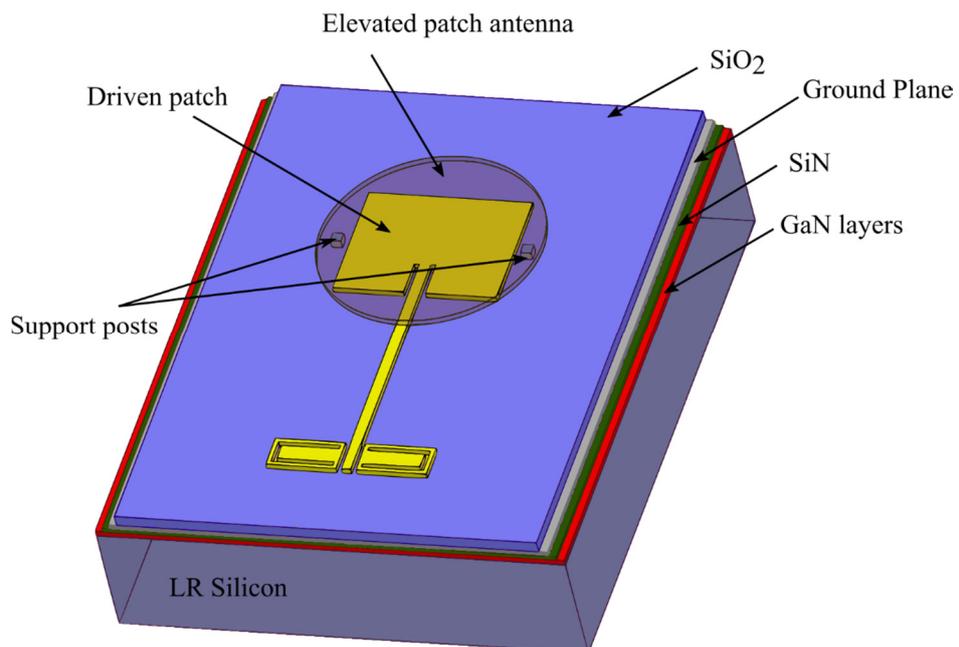
**Fig. 3.42:** Performance plot of 650 GHz single rectangular patch (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

	650 GHz
Reflection Coefficient (dB)	-29.5
Bandwidth (GHz) ( $ S_{11}  < -15$ )	17
Directivity (dB)	-0.98
Gain (dB)	-6.1
Radiation Efficiency (%)	10
Front to back ratio (dB)	9.84

**Table 3.12:** Performance summary of 650 GHz rectangular patch antenna.

### Stack antenna

A rectangular-circular stack configuration was simulated to evaluate the performance of the antenna (this variant of stack was simulated as it performed better compared to other two on BCB dielectric). Fig. 3.43 shows the model of this. The driven patch is designed on a SiO<sub>2</sub> dielectric, whereas the elevated (parasitic) patch is raised in air roughly 6 μm (fabrication tolerance) above the substrate using two square 19 μm × 19 μm gold posts at each end of the patch. Dimensions of the driven patch and elevated patches were calculated using equations in Section 3.8.1 (Page 70) and 3.8.2 (Page 75), by parameters of the SiO<sub>2</sub> dielectric ( $\epsilon_r=4$ ,  $\delta=0.04$ ) and air dielectric ( $\epsilon_r=1$ ,  $\delta=0$ ) separately. The sizes were then optimised using HFSS software to alter the resonant frequency of the antenna at 300 GHz, Table 3.13 shows this.

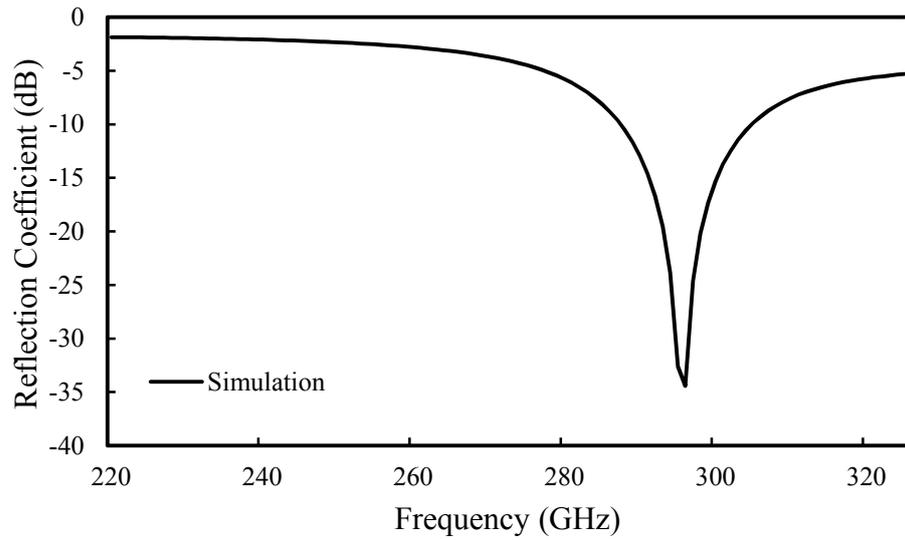


**Fig. 3.43:** 3D diagram of the 300 GHz rectangular-circular patch antenna.

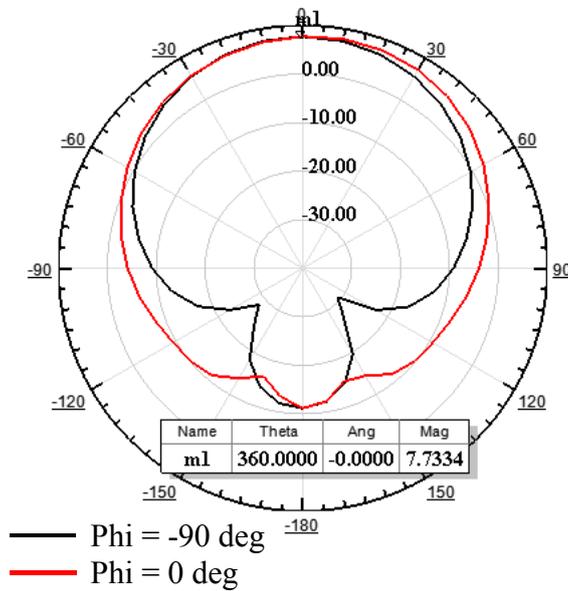
	Dimensions
Driven patch	$280 \times 270 \mu\text{m}$ (W×L)
Elevated patch	$190 \mu\text{m}$ (radius)
Inset feed	$9 \times 65 \mu\text{m}$ (W×L)
Microstrip line	$19 \times 350 \mu\text{m}$ (W×L)
CPW pads (GSG)	$120, 16, 120 \mu\text{m}$ (Gap- $9\mu\text{m}$ ) $\times 60 \mu\text{m}$ (W×L)

**Table 3.13:** Dimensions used for the simulation of the rectangular-circular stack antenna.

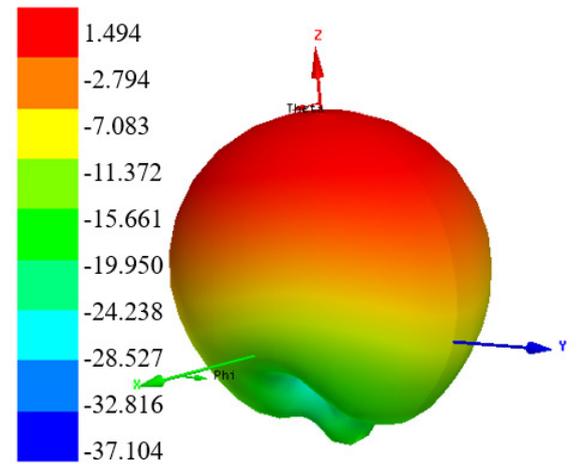
The simulated performance of the rectangular-circular stack antenna is as shown in Fig. 3.44. The antenna resonated at 296 GHz, with return loss as low as -34.42 dB. Antenna radiation performance directivity of 7.73 dB and gain of 1.5 dB at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  was achieved at resonant frequency. Further, radiation efficiency of 22 %, and front to back ratio of 21.11 dB was presented by this antenna.



(a)



(b)



(c)

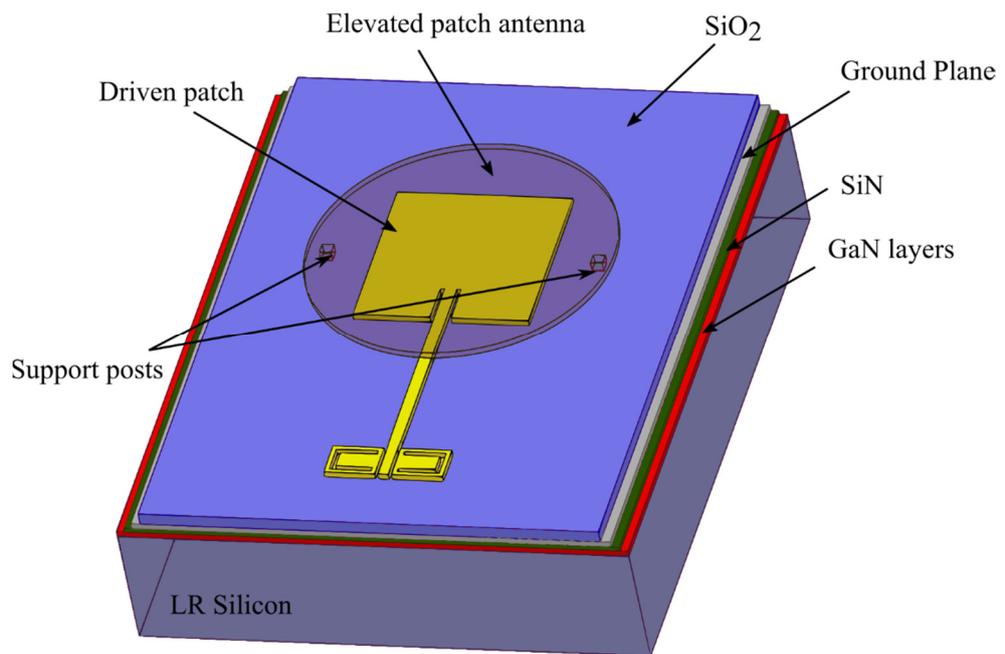
**Fig. 3.44:** Performance plot of 300 GHz stack antenna (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

Comparing the above simulated results with BCB dielectric, gain achieved by SiO<sub>2</sub> dielectric was ~ 2 dB lower, and efficiency roughly 9 % lower (Table 3.14). However, bandwidth achieved was 7 GHz higher than for BCB dielectric. Lower performance of stack antenna on SiO<sub>2</sub> was due to the higher loss tangent and dielectric constant compared to BCB. Further, comparing stack on SiO<sub>2</sub> with SiO<sub>2</sub> single element, directivity increased by ~ 1.5 dB, gain by 0.52 dB and matching was improved due to the stack configuration.

	BCB (stack)	SiO <sub>2</sub> (stack)	SiO <sub>2</sub> (single)
Reflection Coefficient (dB)	-32.3	-34.42	-21.1
Bandwidth (GHz) ( $ S_{11}  < -10$ )	7	14	12
Directivity (dB)	8.3	7.73	6.17
Gain (dB)	3.4	1.5	0.98
Radiation Efficiency (%)	32	22.8	28.51
Front to back ratio (dB)	21	21.11	22.86

**Table 3.14:** Comparison table for performance of simulated stack antenna on BCB with SiO<sub>2</sub> dielectric and single rectangular antenna on SiO<sub>2</sub> dielectric.

A similar stack configuration was designed at 650 GHz to test the performance improvement from a single rectangular antenna. Fig. 3.45 shows the 3D diagram of this. Dimensions used for the simulation of this design are shown in Table 3.15.

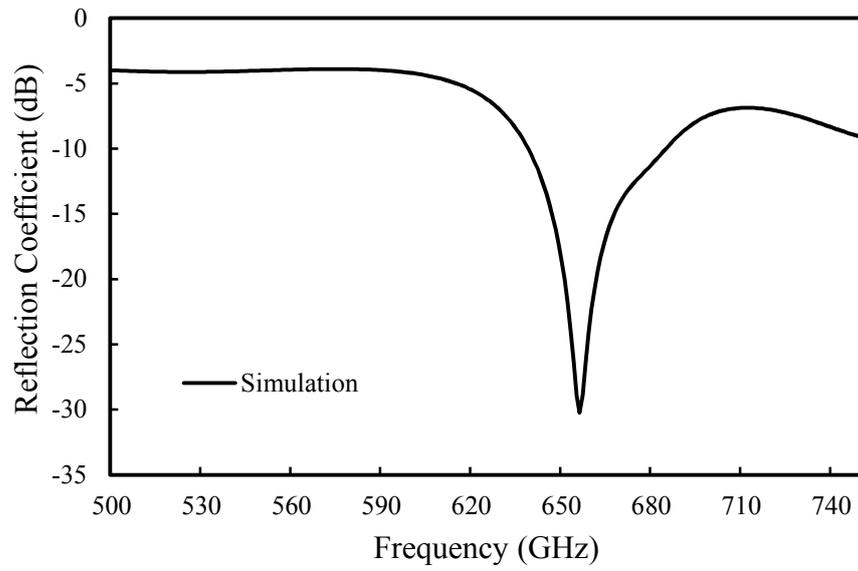


**Fig. 3.45:** 3D diagram of the 650 GHz rectangular-circular patch antenna.

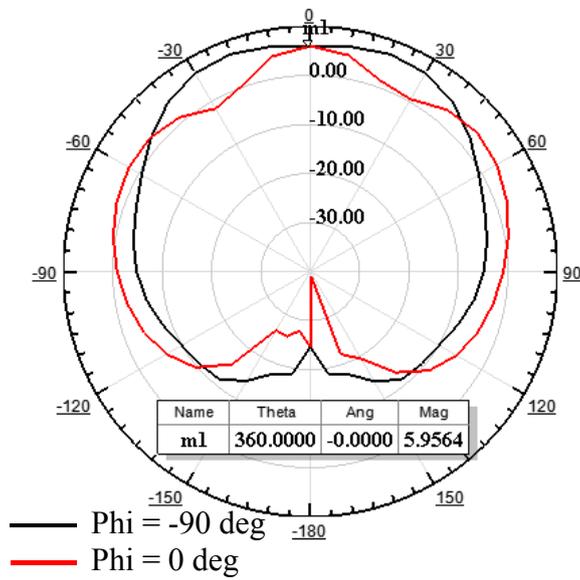
	Dimensions
Driven patch	275 × 280 μm (W×L)
Elevated patch	240 μm (radius)
Inset feed	7 × 65 μm (W×L)
Microstrip line	19 × 300 μm (W×L)
CPW pads (GSG)	120, 16, 120 μm (Gap - 5μm) × 60 μm (W×L)

**Table 3.15:** Dimensions used for the simulation of the rectangular-circular stack antenna.

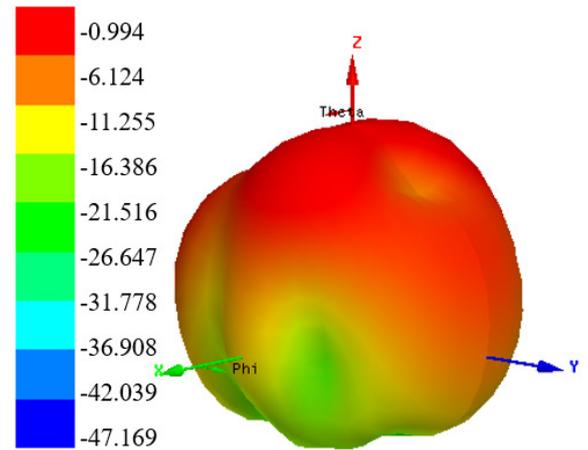
Fig. 3.46 (a) shows the simulated reflection coefficient of the 650 GHz rectangular-circular patch antenna. Simulated reflection coefficient as low as -29.95 dB was achieved at 655.8 GHz. A bandwidth of 25 GHz ( $|S_{11}| < -13$  dB including insertion loss of the transmission line) was noted from the plot. Fig. 3.46 (b) and (c) shows the directivity and gain plot of the antenna at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$ . Maximum directivity achieved was 5.95 dB and maximum gain reached was -0.994 dB at resonant frequency. In addition, radiation efficiency and front to back ratio of the antenna was determined using HFSS software. An efficiency of 26.19 % was achieved and front to back ratio of 15.15 dB. The stack configuration is lossy due to the high dielectric properties of SiO<sub>2</sub> at 650 GHz. Table 3.16 shows a summary of the results. Compared to a single element, the stack improved overall the performance of the antenna.



(a)



(b)



(c)

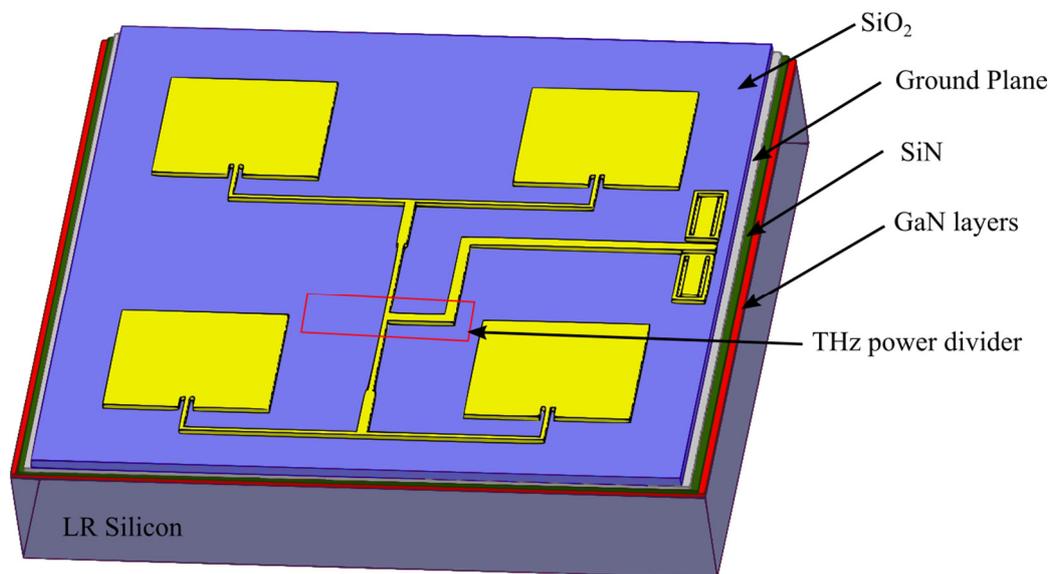
**Fig. 3.46:** Performance plot of 650 GHz stack antenna (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

	Single element	Stack
Reflection Coefficient (dB)	-29.5	-29.95
Bandwidth (GHz) ( $ S_{11}  < -10$ )	17	25
Directivity (dB)	-0.98	5.95
Gain (dB)	-6.1	-0.994
Radiation Efficiency (%)	10	26.19
Front to back ratio (dB)	9.84	15.15

**Table 3.16:** Performance summary of 650 GHz rectangular-circular stack antenna.

### Array antenna

The 3D model of a 300 GHz  $2 \times 2$  array patch antenna on GaN-on-LR Si using the shielding technique is shown in Fig. 3.47. The LR Si is shielded with SiN and an Al ground plane. SiO<sub>2</sub> is used as a dielectric spacer between the patch and the ground plane. Design of the antenna was carried out in HFSS software, for which, width and length of the antenna was derived using the transmission line model (Section 3.8.1, Page 70). In this design, array patches are excited using a corporate feed network. This corporate feed network uses simple T-junction power dividers, see Section 3.8.4, Page 77 for design details. A dielectric height of 10  $\mu\text{m}$ , loss tangent of 0.04 and dielectric constant of 4 at 300 GHz were the parameters used in the simulation of the antenna. Dimensions used for the design of this array antenna is shown in the Table 3.17.

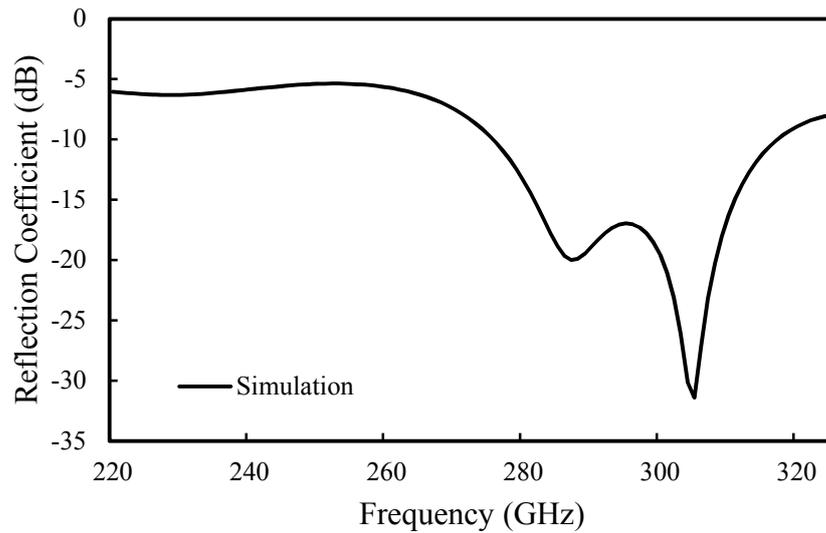


**Fig. 3.47:** 3D model of the  $2 \times 2$  array patch antenna.

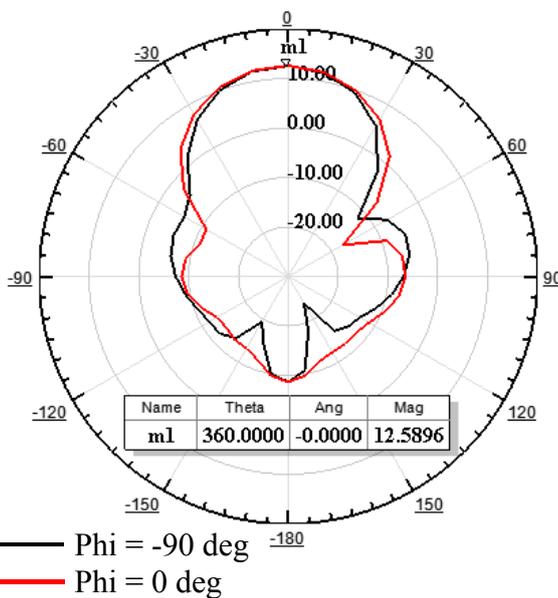
	Dimensions
Antenna	$300 \times 240 \mu\text{m}$ (W×L)
50 $\Omega$ microstrip line	$19 \times 100 \mu\text{m}$ (W×L)
70 $\Omega$ microstrip line	$9 \times 373 \mu\text{m}$ (W×L)
100 $\Omega$ microstrip line	$3 \times 50 \mu\text{m}$ (W×L)
CPW pads (GSG)	$120, 16, 120 \mu\text{m}$ (Gap - $9\mu\text{m}$ ) $\times 60 \mu\text{m}$ (W×L)

**Table 3.17:** Dimensions used for the simulation of the 2×2 array patch antenna.

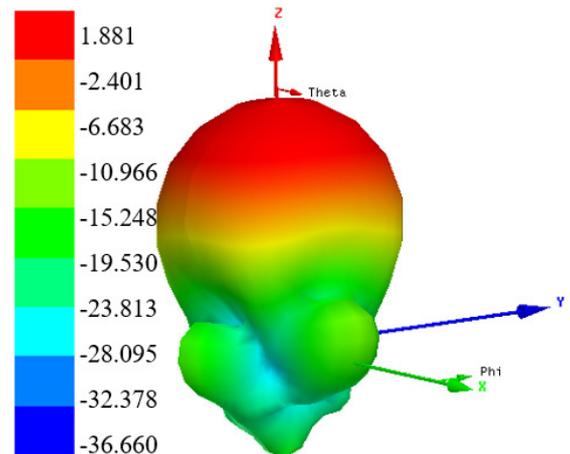
Fig. 3.48 shows the performance of a 300 GHz 2×2 array patch antenna on a SiO<sub>2</sub> dielectric. A reflection coefficient as low as -31.28 dB was achieved. A bandwidth of 27 GHz ( $|S_{11}| < -16$  dB including insertion loss of the transmission line) was noted from the plot. Directivity, gain, radiation efficiency, and front to back ratio as high as 12.58 dB, 1.88 dB, 8.5 %, 21.25 dB at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$  was reached separately at resonant frequency.



(a)



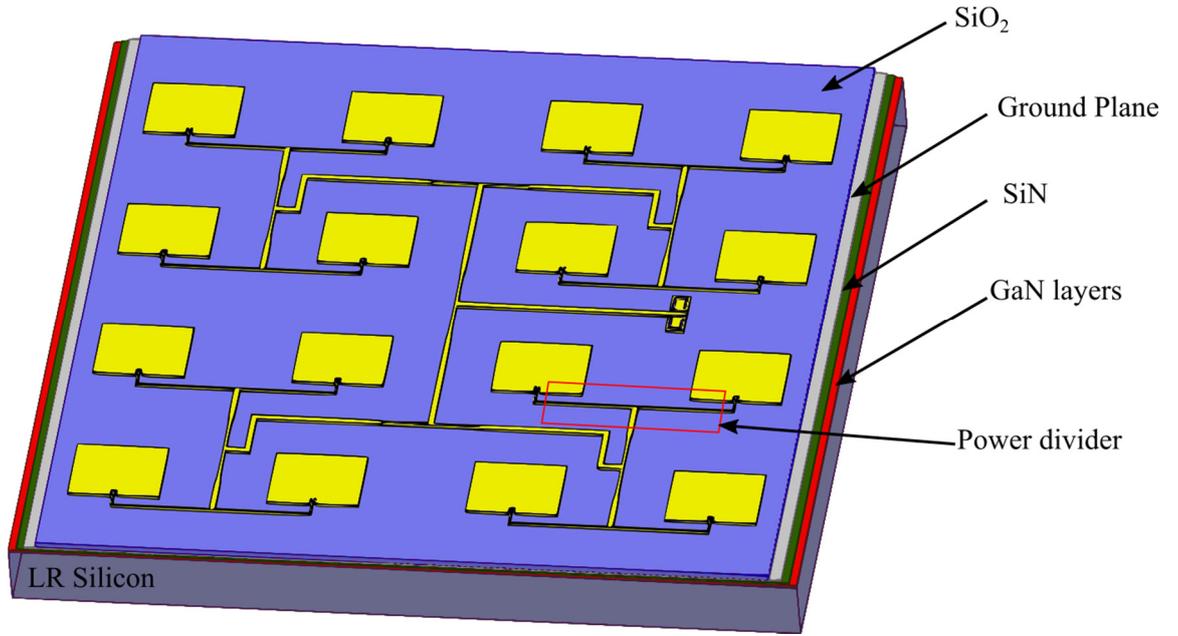
(b)



(c)

**Fig. 3.48:** Performance plot of  $2 \times 2$  array antenna (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

A 3D diagram of a  $4 \times 4$  array antenna on  $\text{SiO}_2$  dielectric is as shown in the Fig. 3.49. Design of this antenna followed the theory of an array antenna discussed in Section 3.8.3, Page 76. Array patches are excited using a corporate feed network and this corporate feed network uses simple T-junction power dividers, see Section 3.8.3, Page 76 for design details. Table 3.18 shows the details of the design.

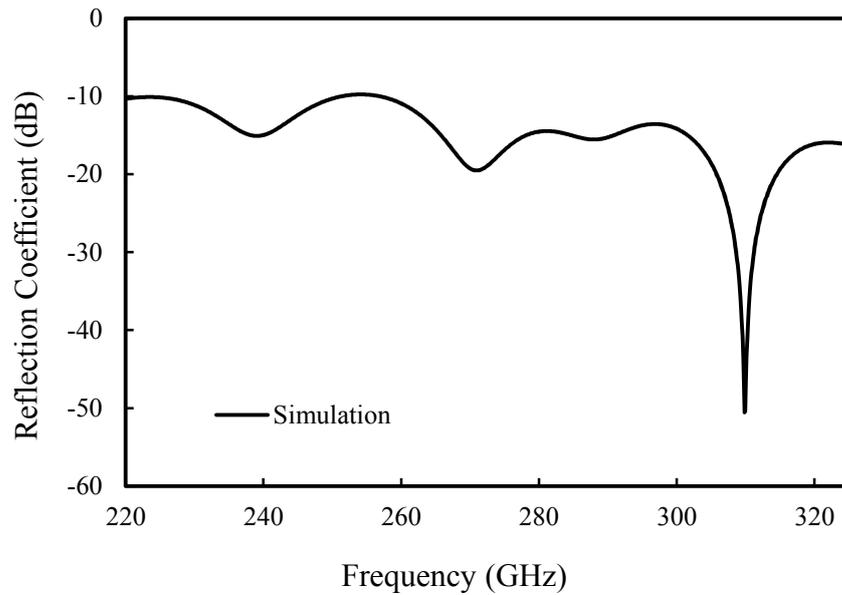


**Fig. 3.49:** 3D model of the 4×4 array patch antenna.

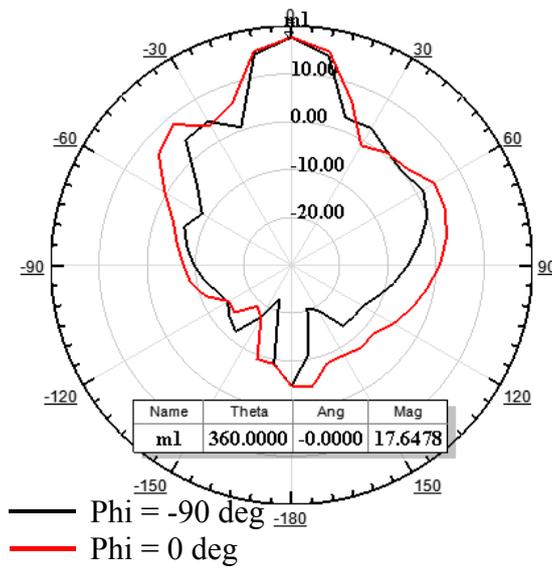
	Dimensions
Antenna	$300 \times 240 \mu\text{m}$ (W×L)
50 $\Omega$ microstrip line	$19 \times 439.5 \mu\text{m}$ (W×L)
70 $\Omega$ microstrip line	$9 \times 150 \mu\text{m}$ (W×L)
100 $\Omega$ microstrip line	$3 \times 50 \mu\text{m}$ (W×L)
CPW pads (GSG)	$120, 16, 120 \mu\text{m}$ (Gap - $9\mu\text{m}$ ) $\times 60 \mu\text{m}$ (W×L)

**Table 3.18:** Dimensions used for the simulation of the 4×4 array patch antenna.

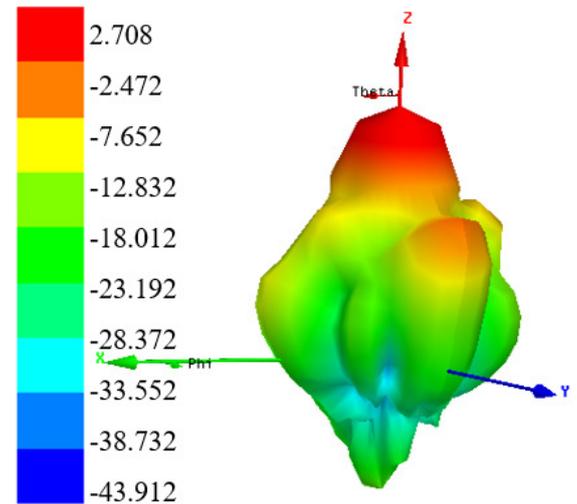
Fig. 3.50 (a) shows the simulated reflection coefficient of the 300 GHz 4×4 array antenna. Simulated reflection coefficient as low as -50.56 dB was achieved at 309.8 GHz. A bandwidth of 9 GHz ( $|S_{11}| < -20$  dB including insertion loss of the transmission line) was noted from the plot. Fig. 3.50 (b) and (c) shows the directivity and gain plot of the antenna at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$ . Maximum directivity achieved was 17.64 dB and maximum gain reached was 2.7 dB at resonant frequency. In addition, radiation efficiency and front to back ratio of the antenna was determined using HFSS software. An efficiency of 3.2 % was achieved and front to back ratio of 22.33 dB.



(a)



(b)



(c)

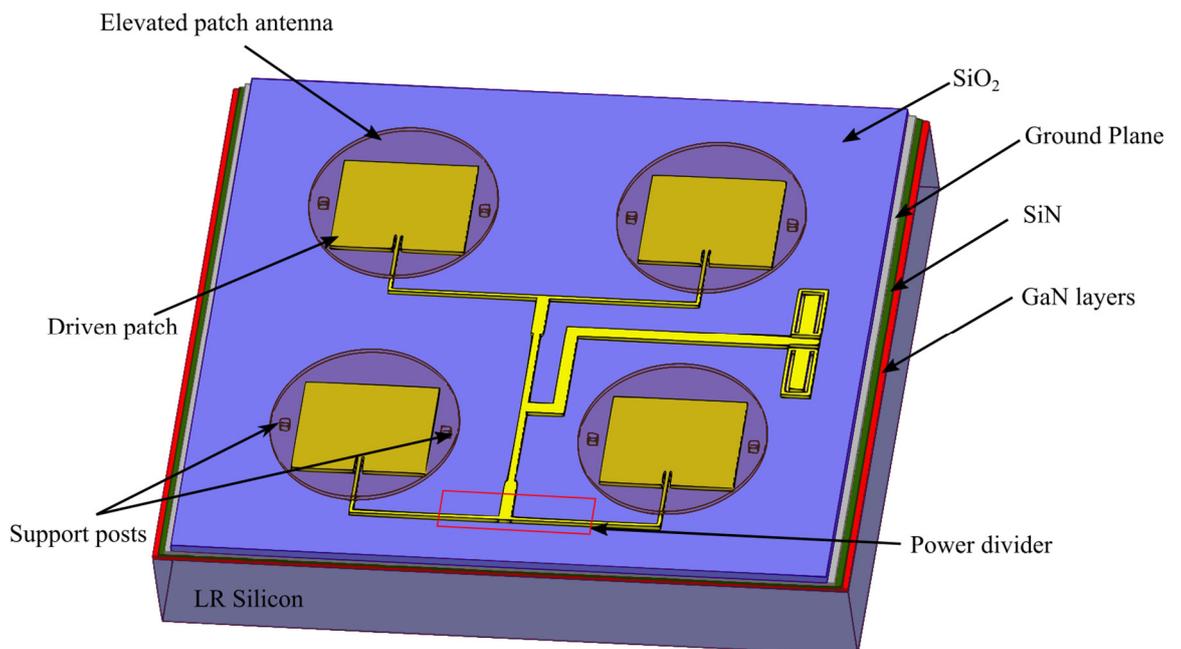
**Fig. 3.50:** Performance plot of 4×4 array antenna (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

Table 3.19 shows the summary of 2×2 array and 4×4 array antenna. Gain, radiation efficiency, and bandwidth achieved by both antenna was very low due to losses from the transmission lines, whereas directivity achieved was better than 10 dB. Improving the feeding technique or possibly reducing the losses in the dielectric material using EBG structures may further improve the antenna efficiency. 2×2 array and 4×4 array antenna on BCB was never simulated as the fabrication of BCB was not consistent.

	2×2 array	4×4 array
Reflection Coefficient (dB)	-31.28	-50.56
Bandwidth (GHz) ( $ S_{11}  < -16$ )	27	9
Directivity (dB)	12.58	17.64
Gain (dB)	1.88	2.70
Radiation Efficiency (%)	8.5	3.2
Front to back ratio (dB)	21.25	22.33

**Table 3.19:** Comparison table for performance of simulated rectangular patch antenna using BCB and SiO<sub>2</sub> dielectric.

Using the array designs above, a stack configuration for both  $2 \times 2$  and  $4 \times 4$  array was designed. Fig. 3.51 shows the 3D model for the 300 GHz  $2 \times 2$  stack array antenna. The driven patch is designed on a SiO<sub>2</sub> dielectric, whereas the elevated (parasitic) patch is raised in air  $\sim 6 \mu\text{m}$  above the substrate (fabrication tolerances) using two square  $19 \mu\text{m} \times 19 \mu\text{m}$  gold posts at each end of the patch. Dimensions of the driven patch and elevated patches were calculated using equations in Section 3.8.1 (Page 70) and 3.8.2 (Page 75), by parameters of the SiO<sub>2</sub> dielectric ( $\epsilon_r=4$ ,  $\delta=0.04$ ) and air dielectric ( $\epsilon_r=1$ ,  $\delta=0$ ) separately. The sizes were then optimised using HFSS software to alter the resonant frequency of antenna at 300 GHz, Table 3.20 shows this.

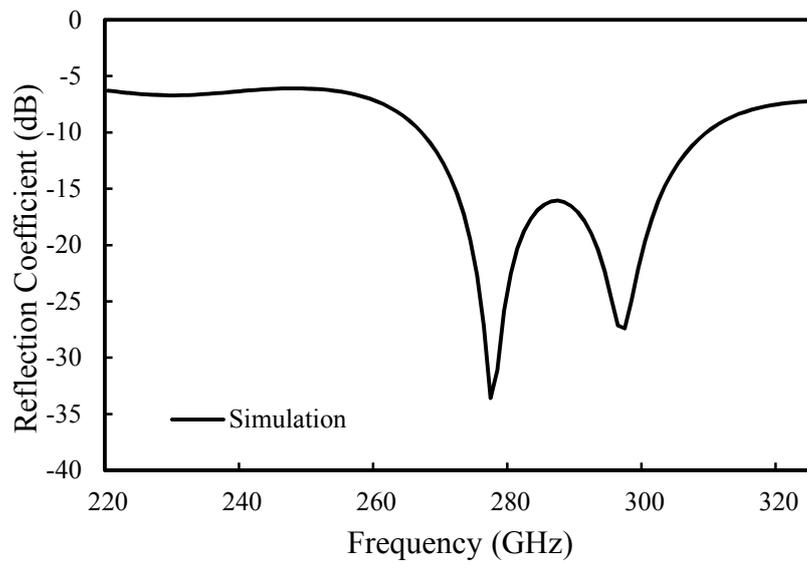


**Fig. 3.51:** 3D model of the  $2 \times 2$  stack array patch antenna.

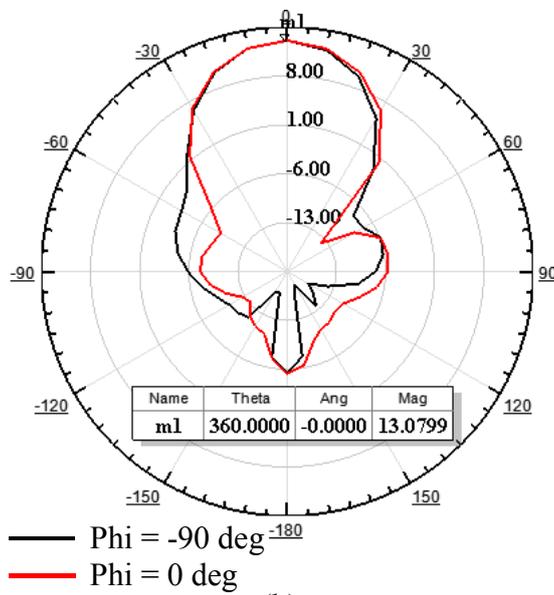
	Dimensions
Driven antenna	$270 \times 220 \mu\text{m}$ (W×L)
Elevated antenna	$190 \mu\text{m}$ (radius)
$50 \Omega$ microstrip line	$19 \times 100 \mu\text{m}$ (W×L)
$70 \Omega$ microstrip line	$7.5 \times 373 \mu\text{m}$ (W×L)
$100 \Omega$ microstrip line	$3 \times 100 \mu\text{m}$ (W×L)
CPW pads (GSG)	$120, 16, 120 \mu\text{m}$ (Gap - $9 \mu\text{m}$ ) $\times 60 \mu\text{m}$ (W×L)

**Table 3.20:** Dimensions used for the simulation of the 2×2 stack array patch antenna.

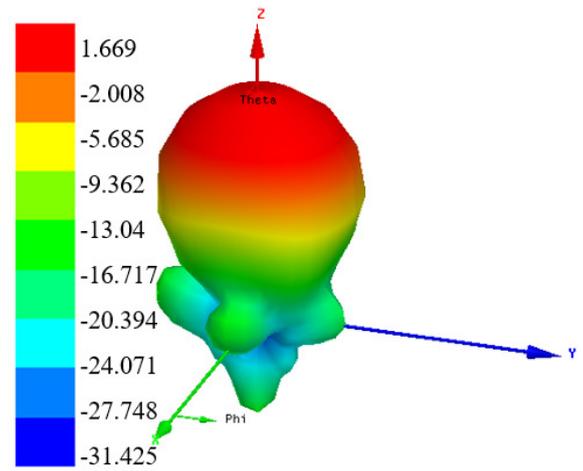
Fig. 3.52 (a) shows the simulated reflection coefficient of the 300 GHz rectangular-circular patch antenna. Simulated reflection coefficient as low as -32.85 dB was achieved at 277.3 GHz. A bandwidth of 30 GHz ( $|S_{11}| < -16$  dB) was noted from the plot. Fig. 3.52 (b) and (c) shows the directivity and gain plot of the antenna at  $0^\circ < \theta < 360^\circ$  and  $\varphi = -90^\circ$  and  $0^\circ$ . Maximum directivity achieved was 13.08 dB and maximum gain reached was 1.67 dB. In addition, radiation efficiency and front to back ratio of the antenna was determined using HFSS software. An efficiency of 7.2 % was achieved and front to back ratio of 18.5 dB.



(a)



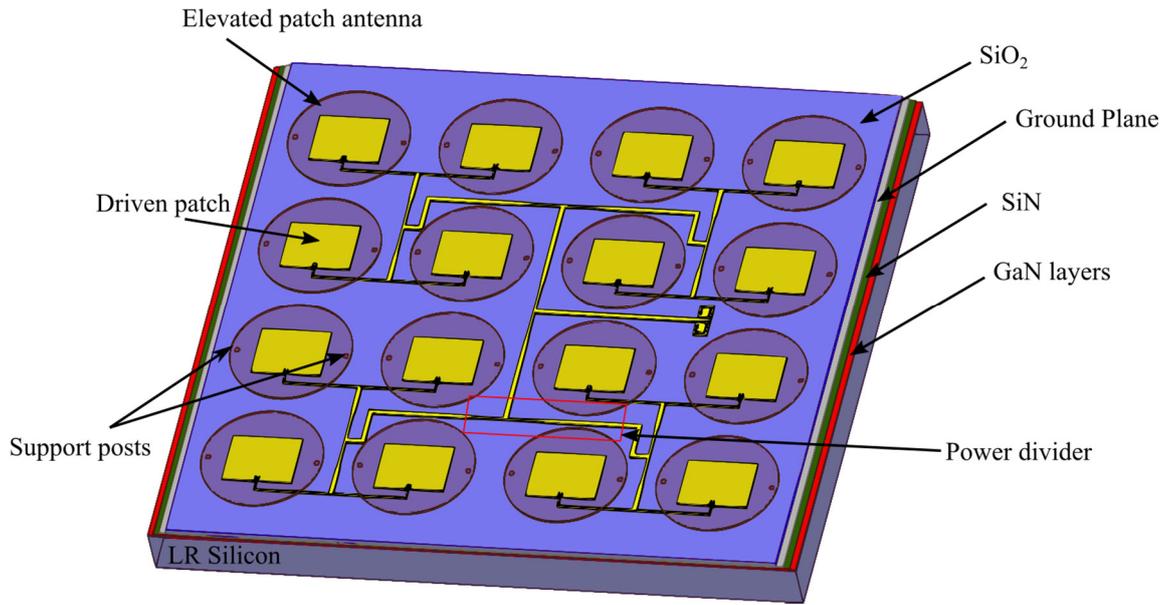
(b)



(c)

**Fig. 3.52:** Performance plot of 2×2 stack array antenna (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

Fig. 3.53 shows the 3D model for the 300 GHz  $4 \times 4$  stack array antenna. Dimensions used for the simulation are shown in the Table 3.21.



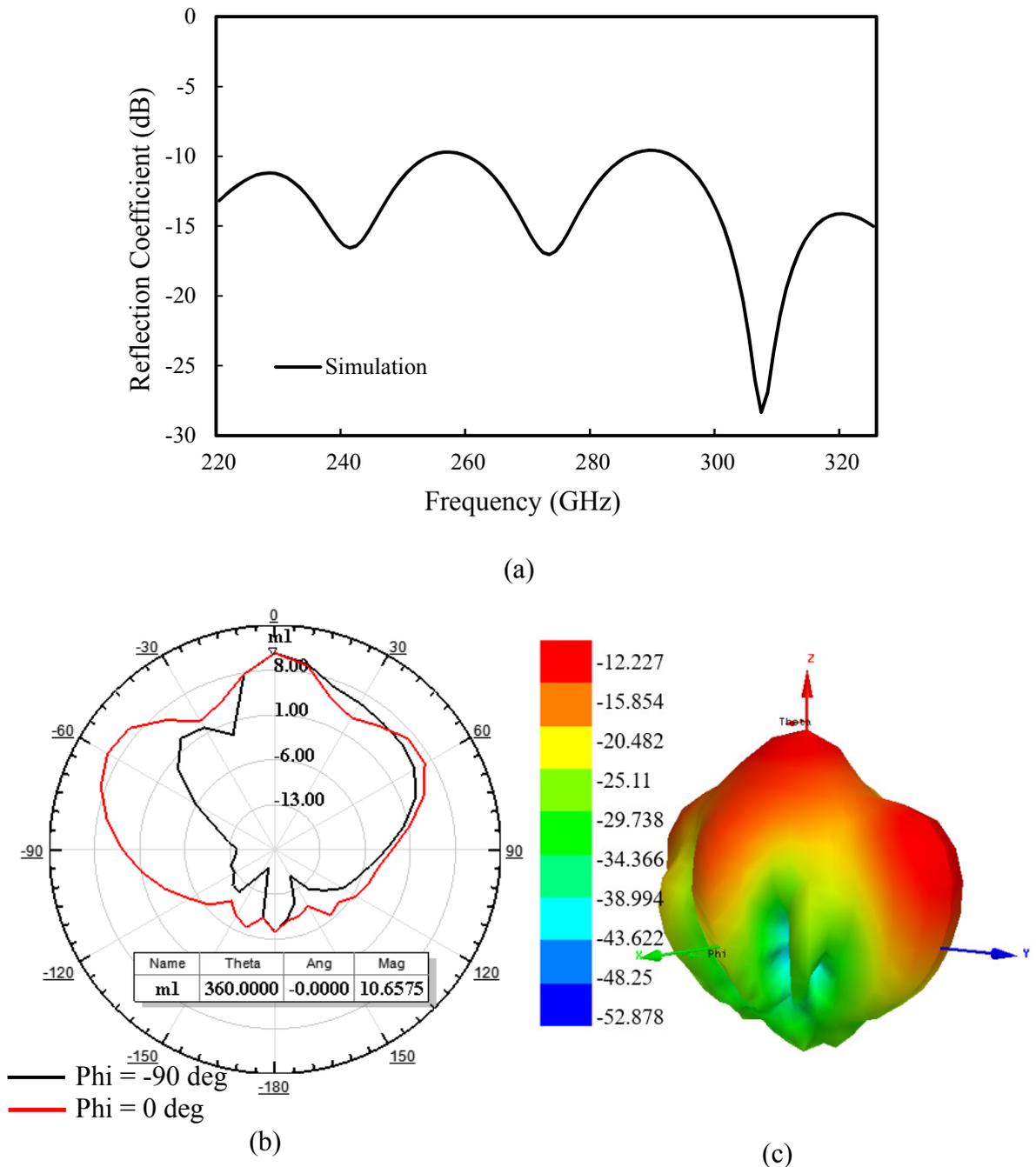
**Fig. 3.53:** 3D model of the  $4 \times 4$  stack array patch antenna.

	Dimensions
Driven antenna	$300 \times 240 \mu\text{m}$ (W×L)
Elevation height (fabrication tolerances)	$6 \mu\text{m}$
Elevated antenna	$260 \mu\text{m}$ (radius)
$50 \Omega$ microstrip line	$19 \times 439.5 \mu\text{m}$ (W×L)
$70 \Omega$ microstrip line	$9 \times 150 \mu\text{m}$ (W×L)
$100 \Omega$ microstrip line	$3 \times 50 \mu\text{m}$ (W×L)
CPW pads (GSG)	$120, 16, 120 \mu\text{m}$ (Gap - $9 \mu\text{m}$ ) $\times 60 \mu\text{m}$ (W×L)

**Table 3.21:** Dimensions used for the simulation of the  $4 \times 4$  stack array patch antenna.

Fig. 3.54 (a) shows the simulated reflection coefficient of the 300 GHz  $4 \times 4$  stack rectangular-circular patch antenna. Simulated reflection coefficient as low as  $-28.34$  dB was achieved at 293 GHz. A bandwidth of 5 GHz ( $|S_{11}| < -23$  dB including insertion loss of the transmission line) was noted from the plot. Fig. 3.54 (b) and (c) shows the directivity and gain plot of the antenna at  $0^\circ < \theta < 360^\circ$  and  $\phi = -90^\circ$  and  $0^\circ$ . Maximum directivity achieved

was 10.65 dB, and maximum gain reached was -12.22 dB. An efficiency of 0.6 % was achieved and front to back ratio of 17.71 dB.



**Fig. 3.54:** Performance plot of 4×4 stack array antenna (a) simulated reflection coefficient (b) simulated directivity (c) simulated gain.

Table 3.22 shows a summary of the 2×2 and 4×4 stack array antenna. Directivity achieved by both the antenna was low compared to the non-stack antenna configuration due to the radiation loss through side lobes. Gain and radiation efficiency achieved were worse than any of the previous designs. It may be due to improper matching between stack and driven

patch and losses from the microstrip line. Changing the feeding technique and reducing dielectric loss of the material may further improve the performance.

	2×2 stack array	4×4 stack array
Reflection Coefficient (dB)	-32.85	-28.34
Bandwidth (GHz) ( $ S_{11}  < -10$ )	30	5
Directivity (dB)	13.08	10.65
Gain (dB)	1.67	-12.22
Radiation Efficiency (%)	7.2	0.6
Front to back ratio (dB)	18.5	17.71

**Table 3.22:** Comparison table for performance of  $2 \times 2$  and  $4 \times 4$  stack array antenna.

In general, comparing antenna on BCB to  $\text{SiO}_2$ , BCB performed much better in terms of gain and radiation efficiency, which showed the necessity of lower dielectric constant and loss tangent material at terahertz frequency. However, very good directivity (17.64 dB) was achieved by  $4 \times 4$  array element on  $\text{SiO}_2$ . Further optimization of stack, stack array on  $\text{SiO}_2$  might improve the radiation performance of antenna, which can be comparable to antenna on BCB.

## 3.10 Measurement of fabricated devices

### 3.10.1 Fabrication

Devices fabricated in this chapter were formed using the techniques outlined in Chapter 2. The fabrication process for the antenna on BCB dielectric was started by depositing a 200 nm  $\text{Si}_3\text{Ni}_4$  on GaN-on-LR Si using ICP-CVD deposition tool. A Ti/Au metal of thickness 50/600 nm was deposited using e-beam evaporation to form the ground plane (shielding). Next, a BCB layer was spun and fully cured in an oven to achieve a thickness of 5  $\mu\text{m}$ . To make the via-hole CPW pads, BCB was etched down to ground metal using plasma RIE and then Ti/Au of the same thickness was evaporated to form the antenna (top metal) or driven patch in case of the stack antenna. Finally, a standard III-V MMIC air-bridge process mentioned in Chapter 2 was used to create support posts and the elevated patch together. All simulated antenna on BCB reported in this chapter were fabricated with the exception of the 1 THz patch antenna.

The fabrication process of the antenna on  $\text{SiO}_2$  dielectric was started by depositing a 200 nm  $\text{Si}_3\text{Ni}_4$  on GaN-on-LR Si using ICP-CVD deposition tool. Then 1  $\mu\text{m}$  of Al metal was deposited using e-beam evaporator as ground plane or shielding. A 10  $\mu\text{m}$  thick  $\text{SiO}_2$  was deposited using PECVD. To create via-hole CPW pads,  $\text{SiO}_2$  was etched to ground plane using the SPTS etcher (Chapter 2 for details) and then evaporated to form the antenna (top metal) or driven patch in case of stack. Same air-bridge process as mentioned in BCB fabrication was used. All the simulated antenna on  $\text{SiO}_2$  reported in Section 3.9.3 have been fabricated.

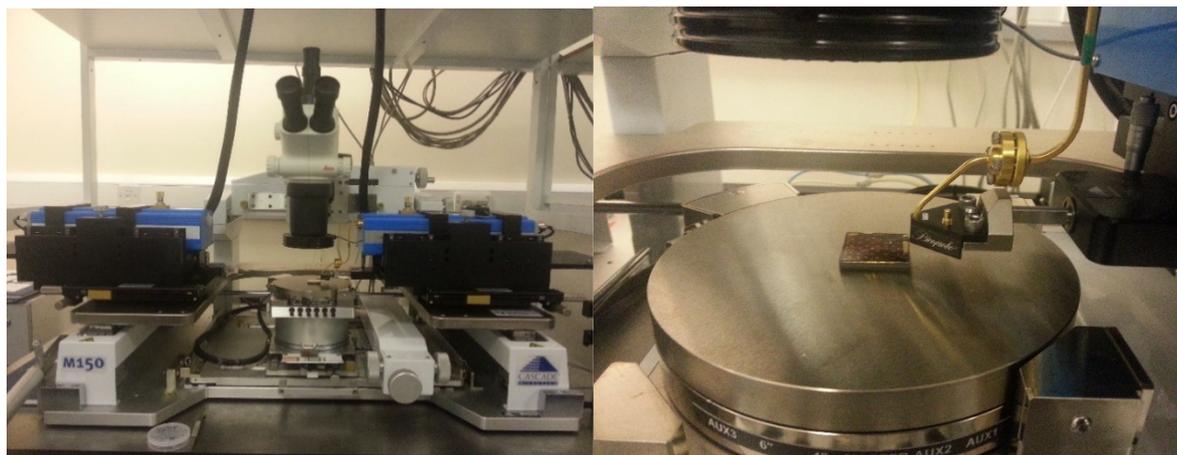
### 3.10.2 Measurement

Accurate measurement of passive devices at millimetre-wave and terahertz frequencies is challenging. For evaluating antenna performance, both S-parameters (return loss) and radiation pattern are measured. Return loss of the antenna determines the frequency of operation, bandwidth and how well the antenna is matched to the 50  $\Omega$  for the measurement system, whereas the radiation pattern determines the efficiency, directivity and losses of the antenna. In this work, only return loss of the antenna was measured, as the system used to measure a 3D pattern was not available at The University of Glasgow.

Return loss measurements of the fabricated antenna were performed using an Agilent PNA Vector Network Analyser with 220-325 GHz OML probes. An ISS standard substrate was used to calibrate the PNA using the LRRM technique (Line-Reflect-reflect-match) and

antenna were probed using 50  $\mu\text{m}$  pitch Pico-probes. Fig. 3.55 shows the measurement setup. All devices above 325 GHz were sent to the Fraunhofer Institute in Germany for measuring purpose.

Reflection and transmission coefficient of transmission lines was measured using the same setup as above. The only difference was that transmission lines are a 2-probe measurement and antenna are a single probe measurement. Calibration of the probes prior to measuring transmission lines was performed.



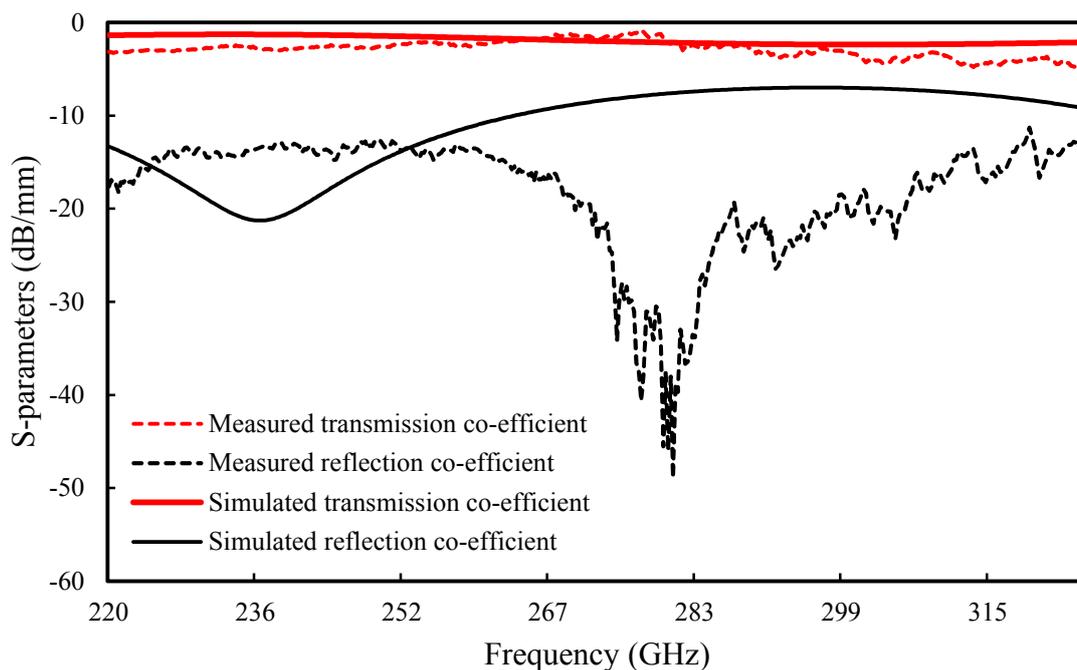
**Fig. 3.55:** Measurement setup at The University of Glasgow.

### 3.10.3 Measured results and discussion

In this section, measured results using BCB as a dielectric are reported. However, while devices using SiO<sub>2</sub> as a dielectric were fabricated, results for these devices are not shown due to measurement delays out with the author's control.

#### Microstrip transmission line

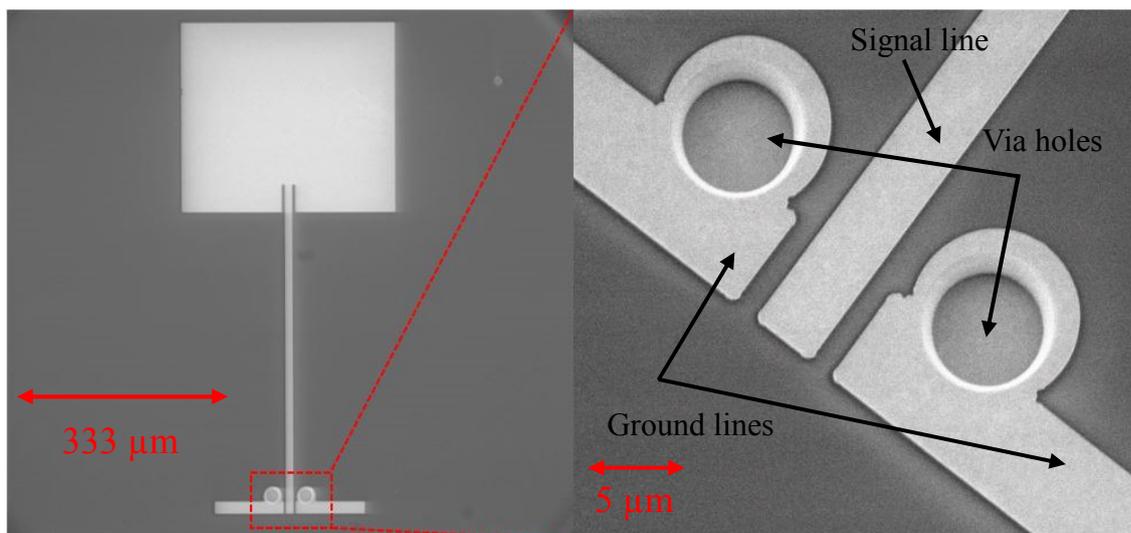
A 50  $\Omega$  transmission line on BCB dielectric reported in Section 3.9.1, Page 83 has been measured at three different frequency intervals (0.1-67 GHz, 220-325 GHz, and 500-750 GHz) as the equipment required to measure from GHz to THz is not available in The University of Glasgow. Fig. 3.56 shows the plot of simulated and measured transmission and reflection co-efficient from 220 to 325 GHz. This frequency is of particular interest, as most of the antenna reported in this thesis were designed at this frequency interval. A transmission loss of 2.5 dB/mm at 325 GHz was measured with matching better than -15 dB across the full measurement band. Further, a transmission loss of 0.9 dB/mm at 67 GHz [3.28], transmission co-efficient of 3 dB/mm at 750 was observed [3.33].



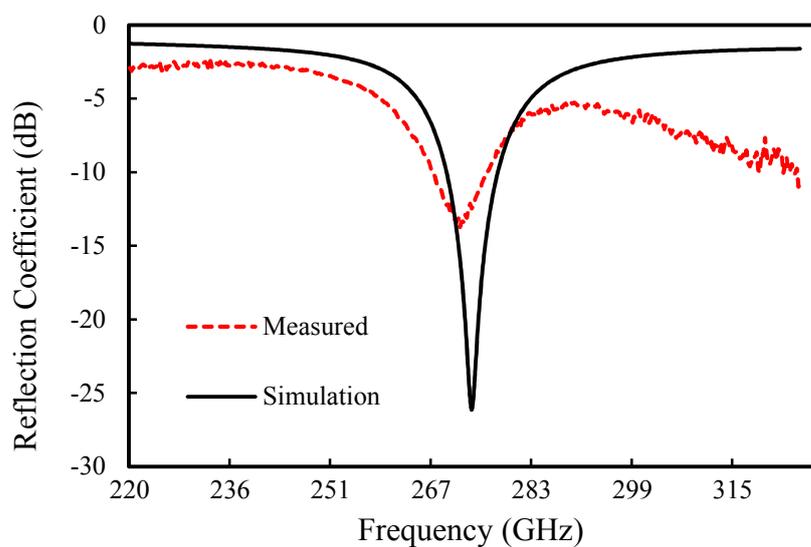
**Fig. 3.56:** Measured and simulated S-parameter results for BCB transmission lines.

## Rectangular patch antenna

A SEM image of the fabricated 270 GHz rectangular patch antenna on BCB discussed in Section 3.9.2, Page 89 is shown in Fig. 3.57 (a). Fig. 3.57 (b) shows the simulated and measured reflection coefficient for this device. Simulated reflection coefficient was as low as -26 dB, while a measured value of -13 dB was observed. The measured bandwidth was 9 GHz and simulated bandwidth was 3 GHz ( $|S_{11}| < -13$  dB including insertion loss of the transmission line).



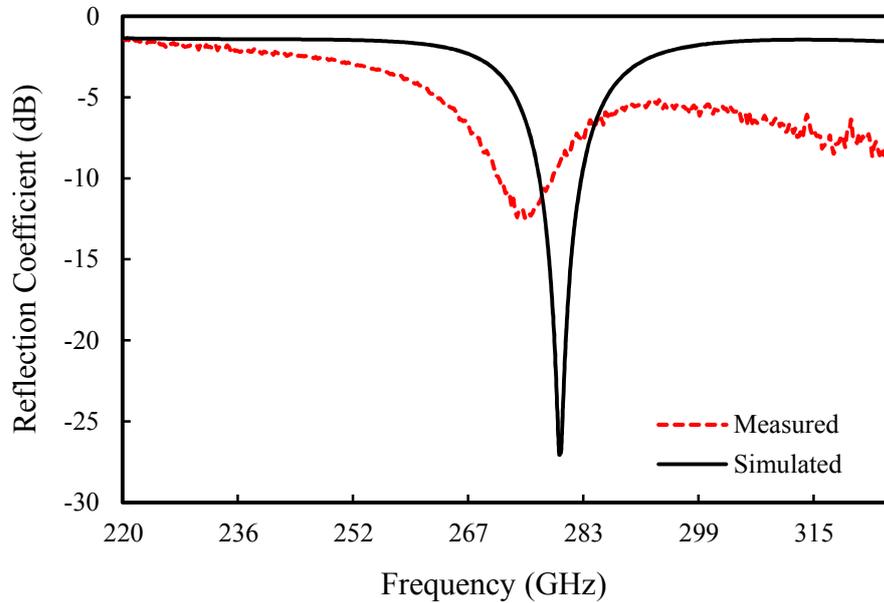
(a)



(b)

**Fig. 3.57:** 270 GHz rectangular patch antenna (a) SEM image (b) Measured and simulated reflection coefficient [3.30] Copyright © 2016, IEEE.

Fig. 3.58 shows the simulated and measured reflection coefficient of the 270 GHz circular patch antenna on BCB (discussed in Section 3.9.2, Page 89). The simulated and measured reflection coefficient achieved was as low as -24 dB and -12.4 dB, respectively, and the measured bandwidth was 4 GHz ( $|S_{11}| < -11$  dB) was attained.



**Fig. 3.58:** Measured and simulated reflection coefficient of the 300 GHz circular patch antenna.

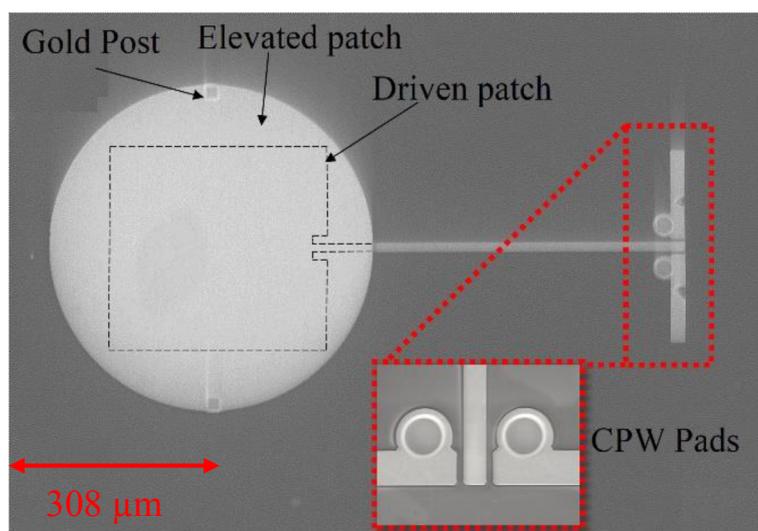
Table 3.23 shows a summary of both rectangular and circular patch antenna at 270 GHz. Measured reflection co-efficient achieved by both antenna was lower than -15 dB due to mismatch loss, and the bandwidth achieved was 2 - 3 GHz lower than the simulated results. The mismatch loss may be due to initial assumption of loss tangent value to be  $\delta=0.002$ , while the actual value was measured was  $\delta=0.02$ . In addition, final thickness achieved for the BCB layer was only 4.4  $\mu\text{m}$  while simulated thickness was 5  $\mu\text{m}$ .

	Rectangular patch	Circular patch
Simulated reflection Coefficient (dB)	-26 @ 274 GHz	-24 @ 280 GHz
Measured reflection Coefficient (dB)	-13 @ 271 GHz	-12.4 @ 276 GHz
Simulated bandwidth (GHz) ( $ S_{11}  < -10$ )	7	5
Measured bandwidth (GHz) ( $ S_{11}  < -10$ )	3	4

**Table 3.23:** Measured and simulated results of rectangular and circular antenna.

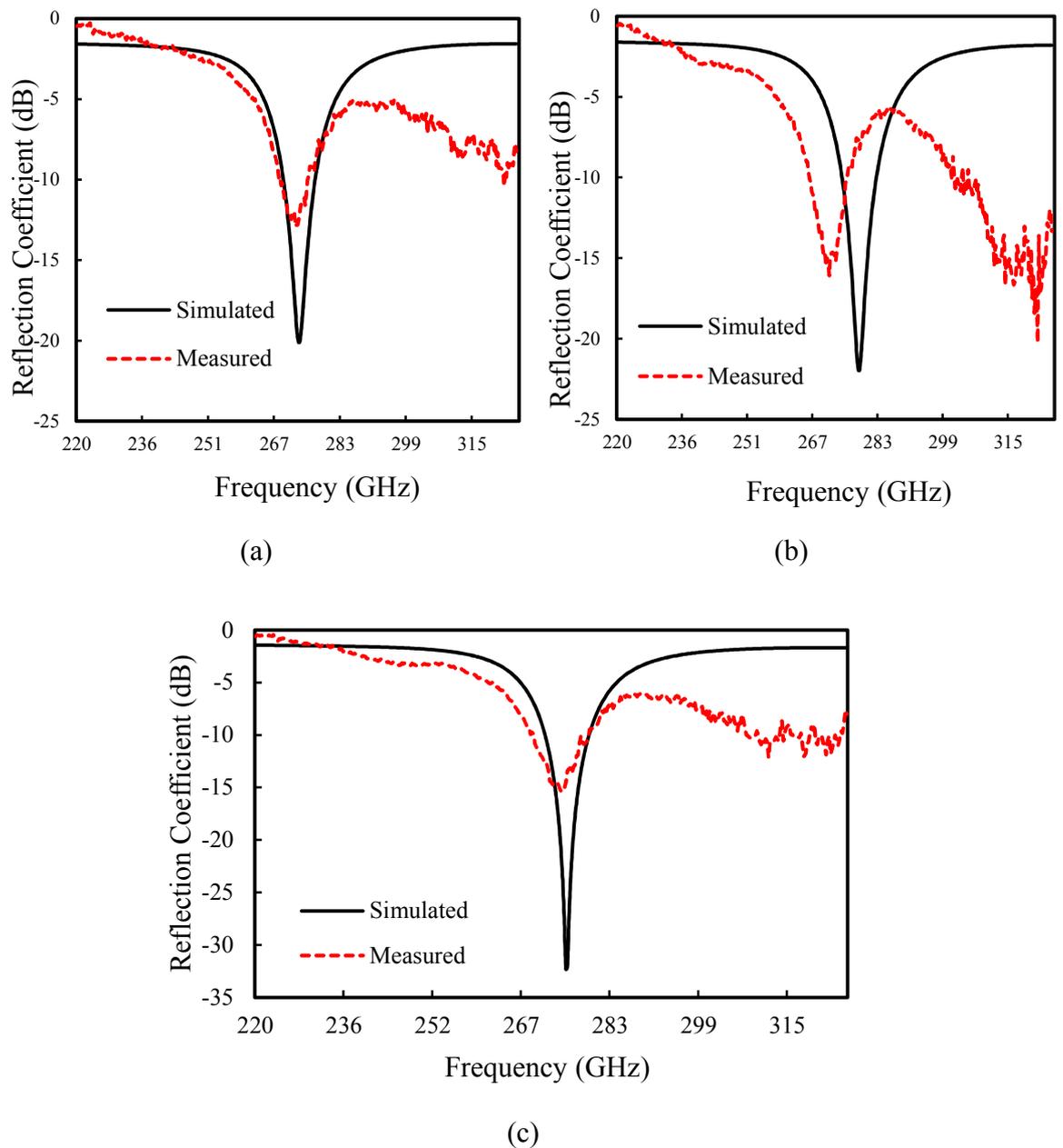
## Stack antenna

All three variants of the stack antenna mention in Section 3.9.2, Page 89 were fabricated and measured. Fig. 3.59 shows the SEM image of the fabricated rectangular-circular patch antenna. Fig. 3.60 shows the measured and simulated reflection co-efficient plot for all three variants. A good agreement between the measured and simulated results was observed. The simulated reflection coefficient attained was as low as -20.1 dB, -21.95 dB, and -32.3 dB for double-rectangular, double-circular and rectangular-circular, respectively, and a measured bandwidth of ( $|S_{11}| < -10$  dB) 6 GHz, 8 GHz, and 9 GHz was achieved.



**Fig. 3.59:** SEM image of the fabricated rectangular-circular stack antenna [3.4]

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**Fig. 3.60:** Measured and simulated reflection coefficient of (a) Double rectangular stack antenna (b) Double circular stack antenna (c) Rectangular-circular stack antenna [3.4] [3.30] Copyright © 2016, IEEE.

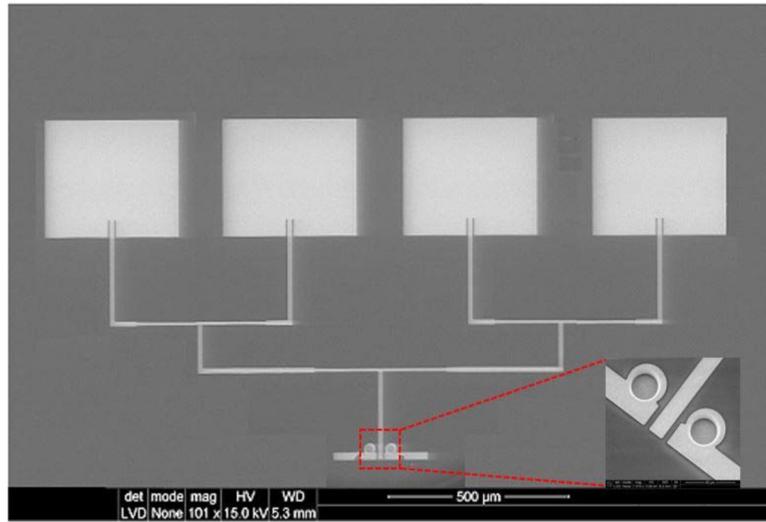
Table 3.24 shows a summary of the measured and simulated results for each of the three variants of stack antenna. The rectangular-circular stack antenna showed better matching and wider bandwidth, both in simulation and measurement, than the other two configurations. The worse mismatch was demonstrated by the double circular stack antenna. This may be due to BCB loss tangent being assumed as lower than it actually was, resulting in an unoptimized design.

	Double rectangular stack	Double circular stack	Rectangular-circular stack
Simulated reflection Coefficient (dB)	-20.1 @ 273 GHz	-21.95 @ 278 GHz	-32.3 @ 275 GHz
Measured reflection Coefficient (dB)	-13 @ 272 GHz	-16 @ 271 GHz	-18 @ 274 GHz
Simulated bandwidth (GHz) ( $ S_{11}  < -11$ )	6	7	7
Measured bandwidth (GHz) ( $ S_{11}  < -10$ )	6	8	9

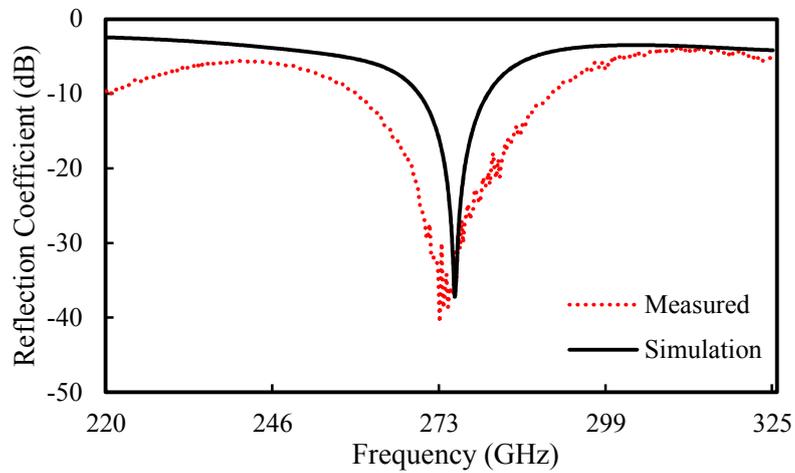
**Table 3.24:** Measured and simulated results of double rectangular stack, double circular stack and rectangular-circular stack antenna [3.30] [3.4] Copyright © 2016, IEEE.

### Array antenna

A SEM image of the fabricated  $4 \times 1$  array patch antenna on BCB discussed in Section 3.9.2, Page 89 is shown in Fig. 3.61 (a). Fig. 3.61 (b) shows the simulated and measured reflection coefficient for this device. A good agreement between the measured and simulation results was observed. The simulated and measured reflection coefficient achieved was as low as -37 dB and -41 dB, respectively, due to better matching obtained by the array patch and power divider. Simulated and measured bandwidth of 9 GHz and 20 GHz ( $|S_{11}| < -16$  dB including insertion loss of the transmission line) was calculated from the plot, this was highest bandwidth achieved compared to previous design due to array configuration, which can be used for transceiver applications. Table 3.25 show a summary of this. Good performances of the antenna suggest that the good reliability of the shielding technique at THz frequencies.



(a)



(b)

**Fig. 3.61:**  $4 \times 1$  array antenna (a) SEM image (b) Measured and simulated reflection coefficient [3.32] Copyright © 2016, IEEE.

	4×1 array antenna
Simulated reflection Coefficient (dB)	-37 @ 275 GHz
Measured reflection Coefficient (dB)	-41 @ 273 GHz
Simulated bandwidth (GHz) ( $ S_{11}  < -12$ )	9
Measured bandwidth (GHz) ( $ S_{11}  < -10$ )	20

**Table 3.25:** Measured and simulated results of  $4 \times 1$  array antenna.

### 3.11 Conclusion

Performance of the microstrip transmission line and microstrip patch antenna on the different dielectrics (air, BCB, and SiO<sub>2</sub>) using a shielding technique has been investigated using GaN-on-LR Si as a substrate material. The problems presented by the thick and high dielectric material (LR Si) at terahertz frequencies, such as surface waves which diminish antenna performance, have been mitigated. For this, various configurations of patch antenna were designed- single rectangular, circular patch, three variants of stack antenna using air as second dielectrics (double rectangular, double circular, rectangular-circular), array antenna, stack array antenna at frequency windows 300 GHz, 650 GHz and 1 THz have been studied. GSG pads were also optimised using via-hole CPW to microstrip transition for measurement purposes. Further, designs were fabricated and measured for validation of the technology. Both simulated and measured results showed the importance of using a dielectric material with lower dielectric constant and lower loss tangent at terahertz frequencies. BCB, in general, performed much better than SiO<sub>2</sub> as a dielectric material due to its lower dielectric loss. This is the first time such a technology has been studied on GaN-on-LR Si for TMIC compatible applications. In addition, this technology can be used for newly emerging high-speed electronics on GaN-on-LR Si without any micromachining or use of high temperature fabrication. As a result, this approach is more cost effective, can be mass produced, is relatively compact and suitable for portable TMICs wireless communication and spectroscopy imaging.

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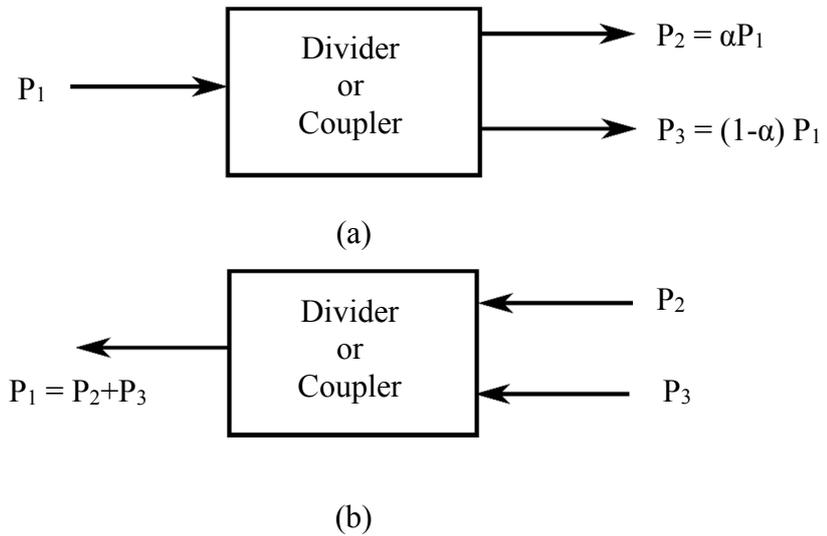
## Couplers and Power dividers on GaN-on-LR Silicon

### 4.1 Introduction

The ability to distribute and combine power signals is a very important and fundamental requirement in many RF systems. It is mostly useful if it can be done over a wide range of frequencies and with phase shifted signals. Power couplers and dividers are essential passive components used in RF systems like mixers, modulators, and antenna beam-forming networks. At terahertz frequencies, these devices become extremely challenging for integration. In this chapter, passive circuits such as hybrid junction couplers and Wilkinson power dividers are designed on GaN-on-LR Si using a shielding technique. The circuits are designed at three different frequencies (90, 300, and 650 GHz) to compare the performance of the devices.

### 4.2 Basic properties of couplers and power dividers

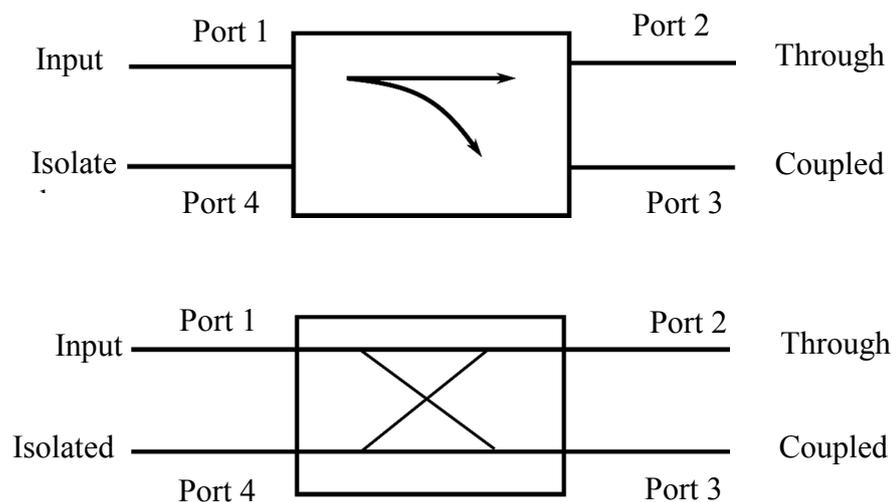
Couplers and power dividers are passive components used for combining or splitting signals, as shown in Fig. 4.1, where  $\alpha$  is the amount of power division. In power splitting, the input signal is divided into two or more weaker signals of lesser power by the passive device and in power combining two or more signals are combined into one stronger signal by the passive device. Power dividers are usually three-port networks, where power division can be of equal or unequal ratios. Couplers are usually four port networks, where directional couplers can be designed for arbitrary power division and hybrid junctions for equal power division with either  $90^\circ$  (quadrature) or  $180^\circ$  (magic-T) phase shift between output ports [4.1].



**Fig. 4.1:** Schematic of (a) Power division (b) Power combining [4.1].

### 4.2.1 Directional couplers

Common symbols used for directional couplers are as shown in the Fig. 4.2. Power is supplied to Port 1, which is then coupled to Port 3, with a coupling factor of  $\beta^2$ . The rest of the input power is delivered to Port 2 with the coefficient  $\alpha^2 = 1 - \beta^2$ . In an ideal case, no power is delivered to Port 4 (which is isolated). Common parameters desired from all directional couplers are high directivity, wide operational bandwidth, and a good impedance match at all ports. Some of these parameters are discussed below.



**Fig. 4.2:** Symbols used for representing directional couplers [4.1].

### Coupling factor:

The coupling factor specifies the fraction of the input signal being coupled to the output port. This is defined as [4.1]:

$$C = 10 \log \frac{P_1}{P_3} = -20 \log \beta \text{ dB} \quad (4.1)$$

Where,  $P_1$  is the power at Port 1 and  $P_3$  is the power at coupled output Port 3. Coupling factor is a negative quantity and it doesn't exceed 0 dB ( $P_1 \neq P_3$ ), and it changes with frequency.

### Loss:

In a directional coupler, insertion loss is a combination of coupling loss, dielectric loss, and mismatch loss. Insertion loss between Port 1 and Port 2 is given as [4.1]:

$$L_{i2,1} = -10 \log \left( \frac{P_2}{P_1} \right) \text{ dB} \quad (4.2)$$

Coupling loss is the power lost when part of it goes to the coupled port. It is given by [4.1]:

$$L_{c2,1} = -10 \log \left( 1 - \frac{P_3}{P_1} \right) \text{ dB} \quad (4.3)$$

### Isolation:

Isolation is the difference in signal levels (dB) between the input port (Port 1) and the isolated port (Port 4) when the other ports are terminated by matched loads. It can also be defined between output ports (Port 2 & 3) by terminating the input and isolation ports by matched loads. It is described as [4.1]:

$$I_{4,1} = -10 \log \left( \frac{P_4}{P_1} \right) = -20 \log |S_{14}| \text{ dB} \quad (4.4)$$

$$I_{3,2} = -10 \log \left( \frac{P_3}{P_2} \right) \text{ dB} \quad (4.5)$$

The higher the isolation, the better the coupler performance will be.

### Directivity:

Directivity is the measure of a coupler's ability to isolate forward and backward waves. It is directly related to isolation by [4.1]

$$I = D + C \text{ dB} \quad (4.6)$$

$$D_{3,4} = 10 \log \left( \frac{P_3}{P_4} \right) = 20 \log \frac{\beta}{|S_{14}|} \text{ dB} \quad (4.7)$$

For an ideal coupler, directivity is infinite, and isolation is zero. For a lossy coupler directivity should be as high as possible, which is a frequency dependent parameter as it depends on the revocation of the two wave components. Equation (4.7) can be used to calculate directivity of any coupler.

### S-parameters:

The scattering parameters are used to derive the basic properties (isolation, coupling, matching, phase difference etc.) of three-port and four-port networks [4.1]. The scattering matrix for a three-port and four-port network has nine and sixteen independent elements, as shown in Equation (4.8) and (4.9).

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \quad (4.8)$$

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \quad (4.9)$$

If ports 1 and 2 are matched in a three-port network, then  $S_{ii}=0$ , and if the network is reciprocal ( $S_{21} = S_{12}$ ,  $S_{13} = S_{31}$ , etc.), the scattering matrix can be written as:

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{21} & 0 & S_{23} \\ S_{31} & S_{32} & 0 \end{bmatrix} \quad (4.10)$$

For a four-port symmetrical coupler, the scattering matrix has the following form:

$$[S] = \begin{bmatrix} 0 & \alpha & j\beta & 0 \\ \alpha & 0 & 0 & j\beta \\ j\beta & 0 & 0 & \alpha \\ 0 & j\beta & \alpha & 0 \end{bmatrix} \quad (4.11)$$

The phases of the terms having amplitude  $\beta$  are chosen equal. For a four-port anti-symmetrical coupler, the scattering matrix has the following form:

$$[S] = \begin{bmatrix} 0 & \alpha & \beta & 0 \\ \alpha & 0 & 0 & -\beta \\ \beta & 0 & 0 & \alpha \\ 0 & -\beta & \alpha & 0 \end{bmatrix} \quad (4.12)$$

The phases of the terms having amplitude  $\beta$  are chosen to be  $180^\circ$  apart. Also, the amplitudes  $\alpha$  and  $\beta$  are not independent, as

$$\alpha^2 + \beta^2 = 1 \quad (4.13)$$

### **Amplitude balance:**

Amplitude balance is the power difference in dB between two output ports (Ports 2 & 3). In an ideal coupler, the amplitude difference should be 0 dB. However, in practice the device amplitude difference is frequency dependent and deviates from 0 dB difference [4.2] [4.3].

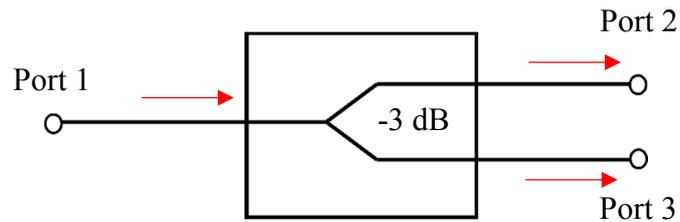
### **Phase balance:**

Like amplitude balance, phase balance is the difference of phase between two output ports [4.2] [4.3]. For a hybrid coupler, phase difference can be  $0^\circ$ ,  $90^\circ$  or  $180^\circ$  depending on the type designed. Phase balance is sensitive to input frequency and can vary by few degrees.

In this work, a special case of directional couplers known as hybrid junctions were designed. They have a coupling factor of 3 dB (equal split) with  $90^\circ$  (quadrature hybrid) or  $180^\circ$  (magic-T or rat race hybrid) phase difference between the output ports. The following sections explain the design of hybrid junctions.

## 4.2.2 Power dividers

The symbol used for a power divider is shown in Fig. 4.3. Power dividers and directional couplers fall within the same group of devices. Directional couplers are four-port devices, where only a small fraction of the input power appears at the coupled port. However, power dividers are dedicated for power splitting, where there is tight coupling between the output ports [4.1]. The most common power dividers are T-junction and Wilkinson power dividers. The following section below explains the design of a Wilkinson power divider.



**Fig. 4.3:** Symbol for power divider [4.1].

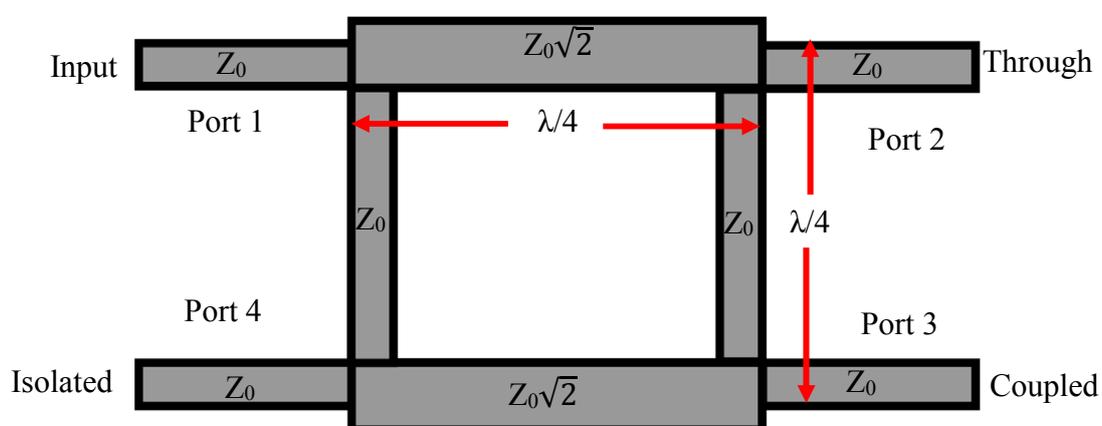
## 4.3 Coupler and Power divider circuit designs

### 4.3.1 The branch line coupler

The branch line coupler is a quadrature hybrid with 3 dB coupling factor and  $90^\circ$  phase difference in the output ports. Fig. 4.4 shows the geometry of a branch-line coupler. When all the ports are matched, the power entering port 1 will be split equally between Port 2 and 3, with a phase difference of  $90^\circ$  between them and no power enters through the isolated Port 4. The S-matrix of a branch line will have the following form [4.1]:

$$[S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \quad (4.14)$$

Since the design of branch line couplers have a high degree of symmetry, any port can be used as an input port and opposite ports will be output ports with the isolation port being on the same side as the input port. This is reflected in the S-matrix, where each row is the transposition of the first row.

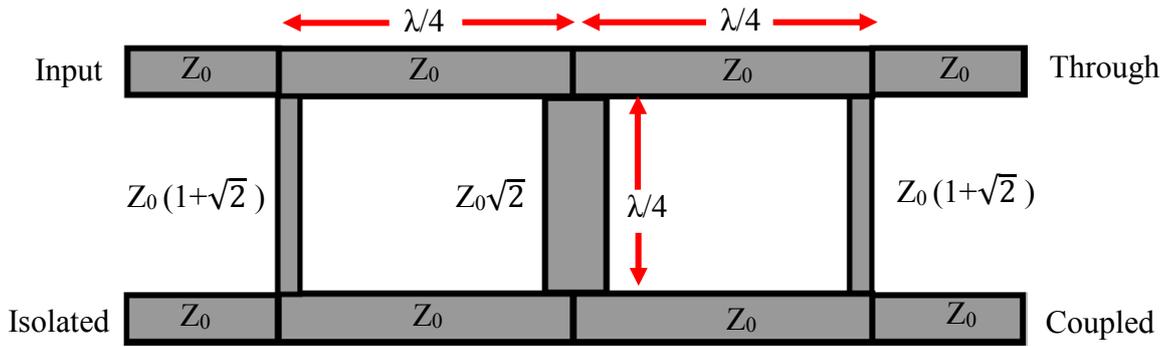


**Fig. 4.4:** Geometry of branch line coupler [4.4].

As the circuit uses quarter wavelength transmission lines, the bandwidth of the branch-line hybrid is limited to 10-20 %. For improving the bandwidth, multiple sections of the branch line in cascade form can be used. Further, by altering the arm's characteristic impedance and/or length, it is possible to divide power between the output ports unequally.

### 4.3.2 The cascaded branch line coupler

The cascaded branch line coupler is a multi-section design of the basic branch line coupler in cascade form, as shown in Fig. 4.5. The idea of this design is to improve the bandwidth of the branch line coupler. The branch lines are spaced  $\lambda/4$  distance apart and the coupled line is  $\sqrt{2}$  of the system impedance. High impedance lines have narrow tracks, which limits the design to three sections due to fabrication tolerances [4.5].

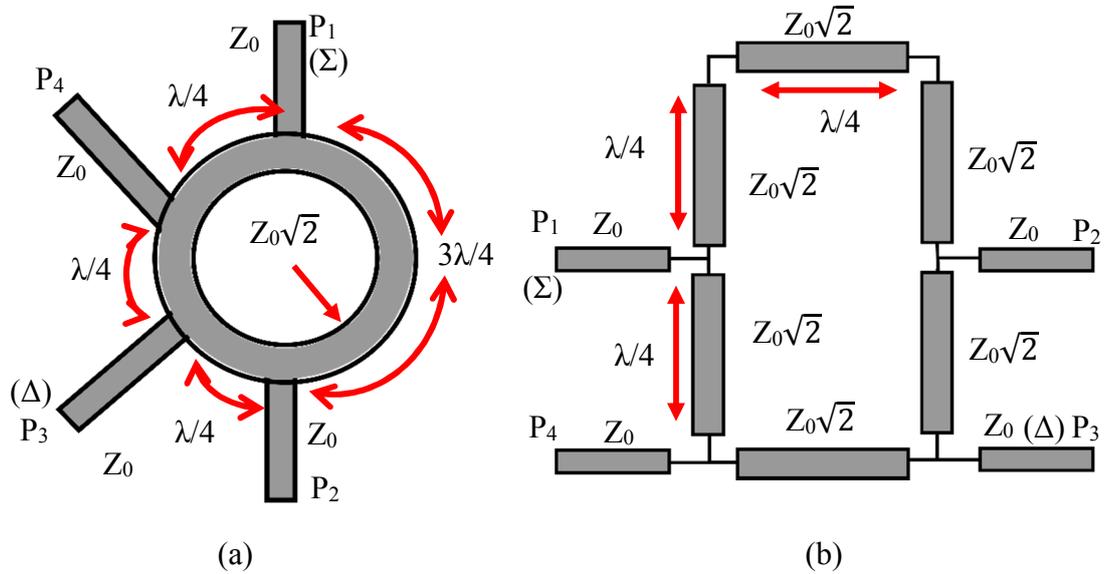


**Fig. 4.5:** Geometry of cascaded branch line coupler [4.6].

### 4.3.3 The rat race coupler

The rat race coupler is an  $180^\circ$  hybrid four-port network. Fig. 4.6 shows the  $180^\circ$  hybrid junction in ring and rectangle form. When all the ports are matched, the signal from Port 1 splits equally into two in-phase components at Ports 2 and 4, while Port 3 is isolated. Due to symmetry, Ports 1 and 3 can be interchanged for the input port and isolated port. The rat race coupler, when operated as a combiner, has input signals applied to Ports 2 and 4. The sum of these inputs will appear at Port 1, while the difference of the input will appear at Port 3. Thus, Ports 1 and 3 are denoted as the sum and difference ports, respectively. In this work, the rectangle form of rat race coupler was used for design, as the ring formation occupies more space by comparison. The ring design in Fig. 4.6 (a) is composed of three-quarter wave ( $\lambda/4$ ) transmission line and one  $3\lambda/4$  transmission line. This  $3\lambda/4$  transmission line is decomposed into three sections to make a square configuration instead of circular. The S-matrix of the rat race coupler thus has the following form [4.1]:

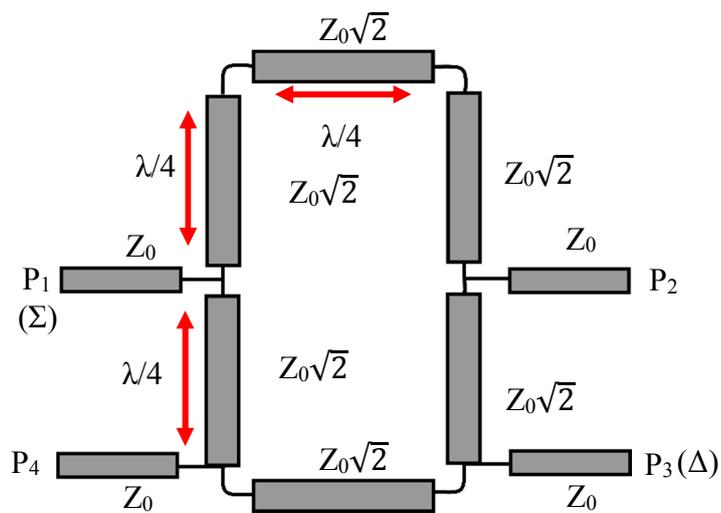
$$[S] = \frac{-j}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & -1 \\ 1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \end{bmatrix} \quad (4.15)$$



**Fig. 4.6:** Geometry of rat race coupler (a) ring form (b) rectangle form [4.4] [4.7].

The bandwidth of the rat race hybrid is 20-30 % and is usually limited by the frequency dependency of the arm's length [4.1].

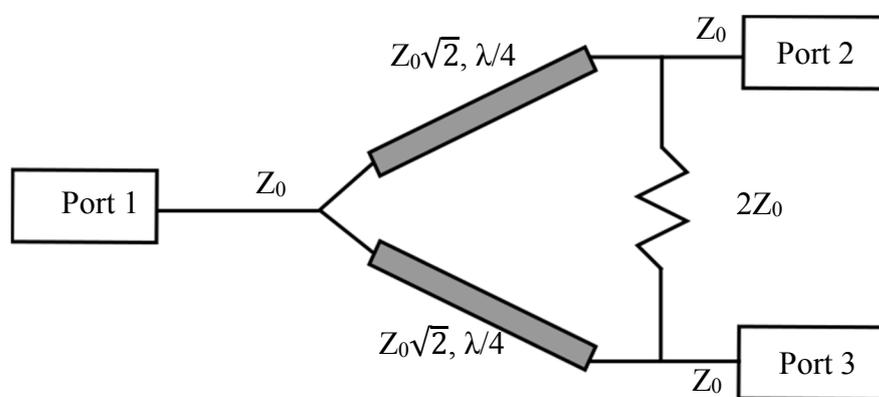
The rectangular rat race coupler discussed above has 90° bend or discontinuities which is undesirable at the terahertz frequencies. Discontinuities in microstrip is caused by an abrupt change in the geometry of the conductor [4.8]. To remove these discontinuities the edges of the rectangle rat race coupler is made curved. The radius of the curve is adjusted to make the circuit to resonant at the desired frequency. Fig. 4.7 shows the circuit diagram of the curved rat race coupler.



**Fig. 4.7:** Circuit diagram of the curved rat race coupler.

#### 4.3.4 The Wilkinson power divider

The lossless T-junction power divider used in designing array antennas (discussed in Section 3.8.4, Chapter 3, Page 77) experiences problems due to the ports being unmatched, due to the absence of isolation between output ports. The Wilkinson power divider is such a network, which is lossless when the output ports are matched, and isolation exists at the output ports [4.1]. Fig. 4.8 shows the circuit diagram of an equal split Wilkinson power divider. Here the input signal is split equally between the two output, in both phase and amplitude. The two arms are quarter wavelength with impedance  $1.414 \times Z_0$  and resistor ( $2Z_0$ ) between the two arms is used to isolate Port 2 and Port 3 at the resonant frequency. Arbitrary power division can also be achieved by designing the arm of higher impedance or by loading arms with short or open stub [4.9].



**Fig. 4.8:** Geometry of Wilkinson power divider [4.5].

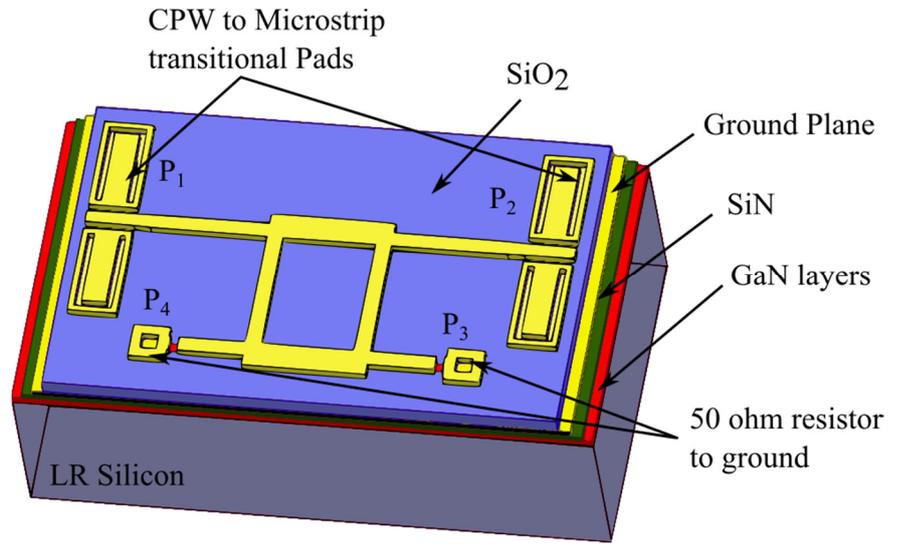
The Wilkinson power divider can also be used to generate an N-way divider or combiner. However, for fabricating planar devices of  $N \geq 3$ , this is more complicated due to the divider resistor crossovers [4.1].

## 4.4 Simulation

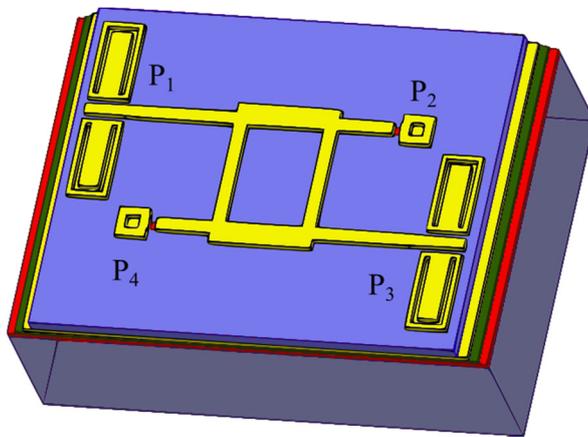
Simulation of couplers and power dividers discussed so far were carried out using Ansys HFSS software. Prior to using HFSS, another software packaged named ADS was used to find the approximate dimensions of the transmission lines in the making of the passive devices. The devices were simulated at three different frequencies (90 GHz, 300 GHz and 650 GHz) on SiO<sub>2</sub> dielectric. The same shielding technique as used in the antenna design in the Chapter 3 was adopted. A dielectric constant of 4 and loss tangent of 0.04 was used for simulating passive devices at these frequencies on SiO<sub>2</sub>. Further, widths and lengths of transmission lines used were also tabulated.

### 4.4.1 The branch line coupler

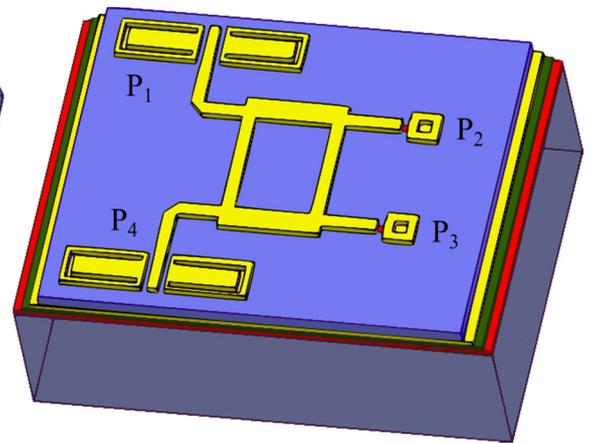
The 3D diagram of a branch line coupler is shown in the Fig. 4.9. The couplers were designed to fit two-port pair measurement and the other two ports were terminated with 50  $\Omega$  resistors. In this way, three sets of measurements ( $S_{11}$ ,  $S_{21}$ ), ( $S_{11}$ ,  $S_{31}$ ), ( $S_{11}$ ,  $S_{41}$ ) were carried out which describes the overall performance of the coupler [4.10]. A 50  $\Omega$  CPW to microstrip via-hole transition was attached at the end of transmission line for measurement compatibility. The widths and lengths for designing branch line couplers at the three different frequencies were calculated based on the different transmission line's characteristic impedances and lengths, shown in Fig. 4.4, Page 154 and is tabulated in Table 4.1.



(a)



(b)



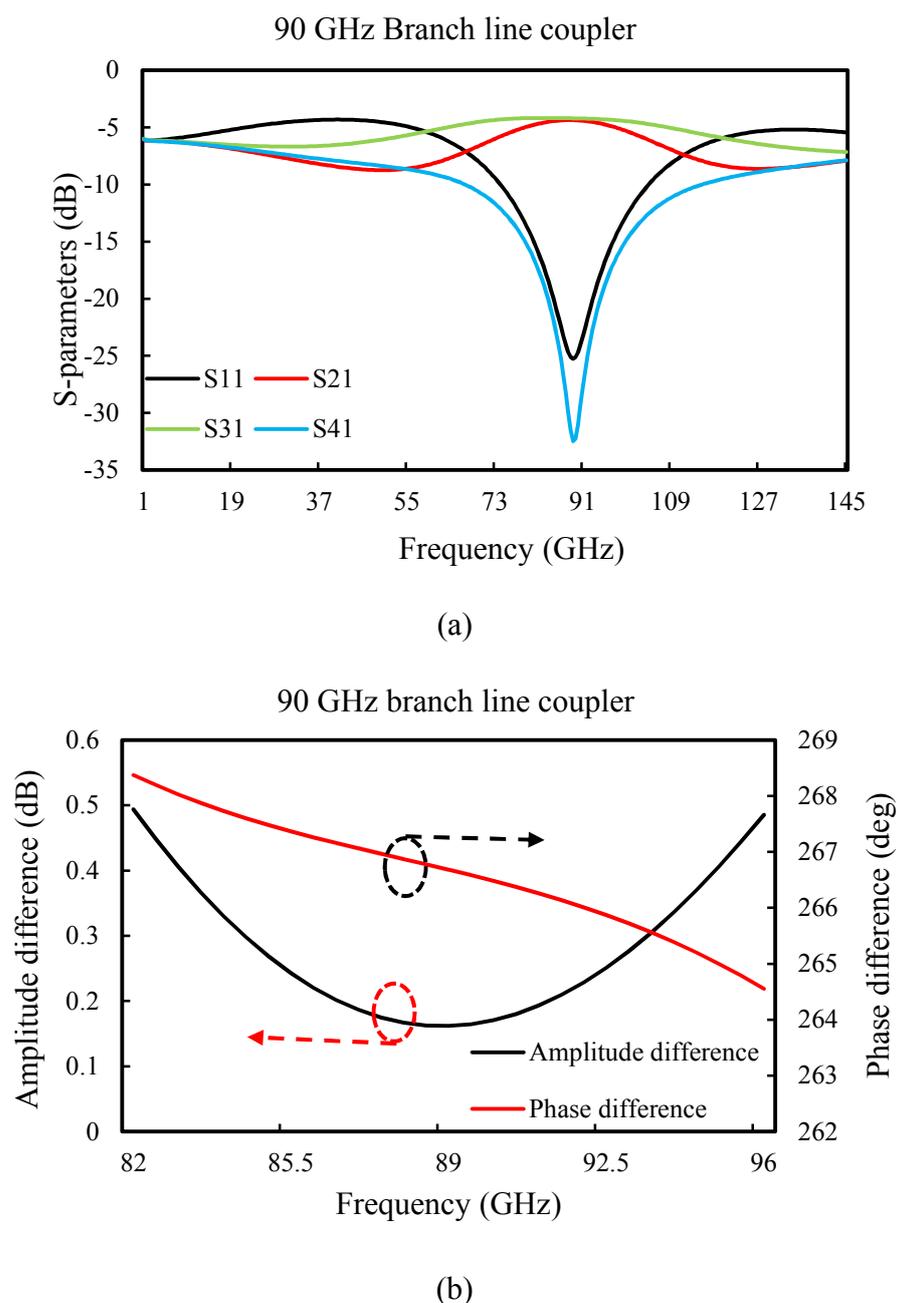
(c)

**Fig. 4.9:** 3D images of branch line coupler simulated for final two-port measurements  
 (a) P<sub>1</sub> and P<sub>2</sub> measured (b) P<sub>1</sub> and P<sub>3</sub> measured (c) P<sub>1</sub> and P<sub>4</sub> measured.

Frequency (GHz)	70.71 $\Omega$ , $\lambda/4$		50 $\Omega$ , $\lambda/4$		50 $\Omega$ , $\lambda/2$	
	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
90	33.7	464	19	478	19	100
300	33	150	19	154	19	80
650	28	70	19	65	19	50

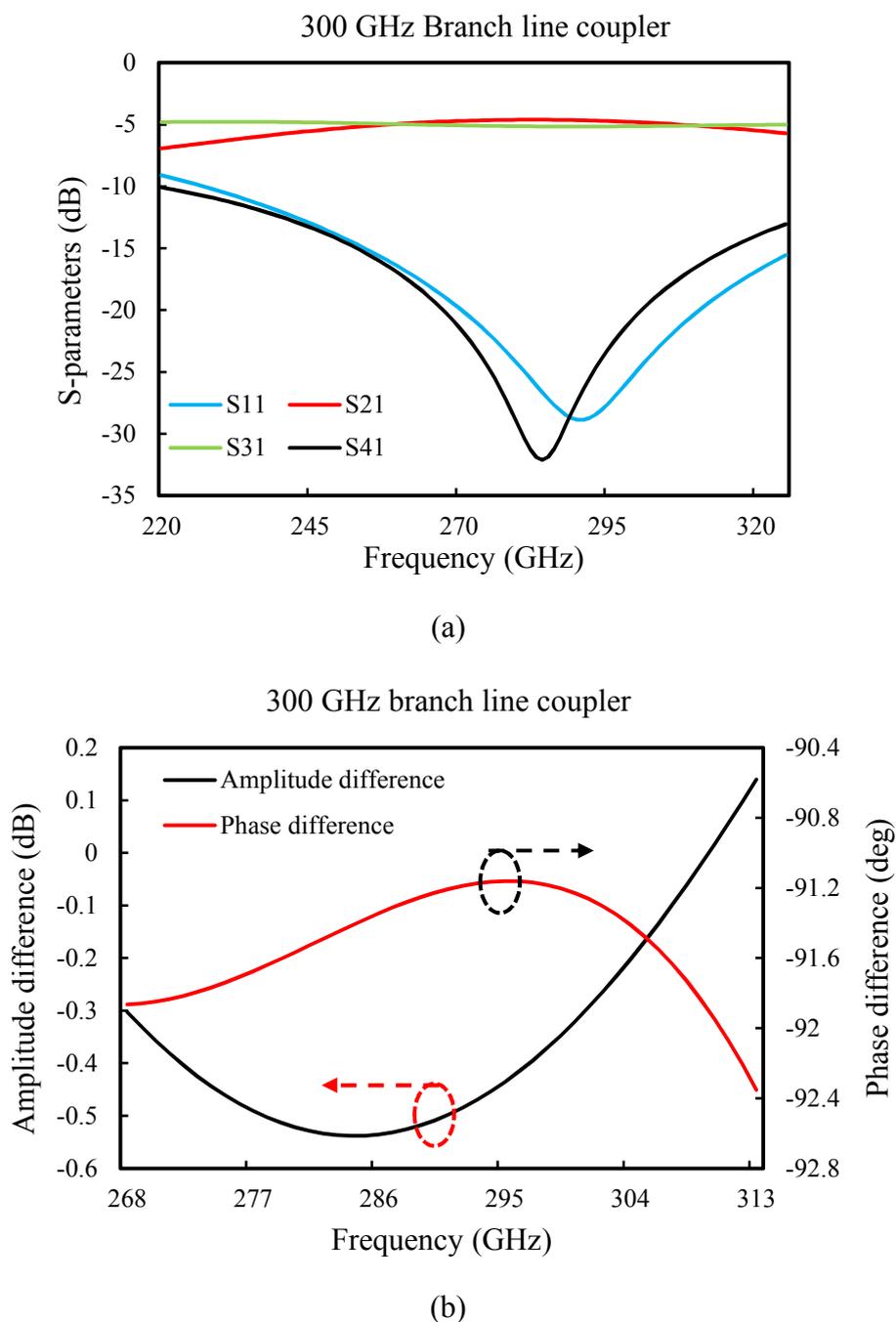
**Table 4.1:** Dimensions used for designing branch line coupler.

The simulated S-parameters of the 90 GHz branch line coupler is shown in the Fig. 4.10 (a). The coupling factor ( $|S_{31}|$ ) and through ( $|S_{21}|$ ) of -4.18 dB and -4.36 dB was achieved respectively. Return loss ( $|S_{11}|$ ) as low as -25 dB, and isolation ( $|S_{41}|$ ) as low as -32 dB was reached. A 15-dB (including insertion loss of transmission line) percentage bandwidth was about 15.77%. The amplitude ( $|S_{31} - S_{21}|$ ) and phase difference ( $\angle S_{31} - \angle S_{21}$ ) between two output ports are plotted in Fig. 4.10 (b). The amplitude difference was less than 0.5 dB between 82 and 96 GHz and the phase shift between outputs were  $90^\circ$  with  $178^\circ$  phase difference.



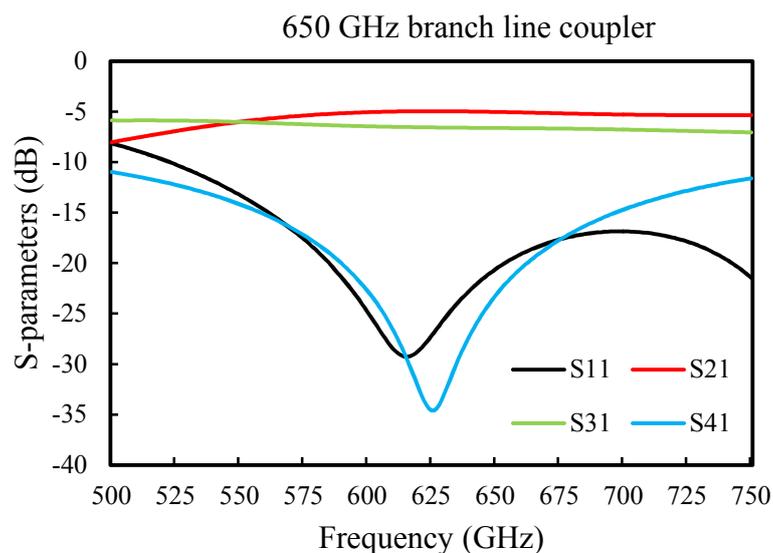
**Fig. 4.10:** Simulated performance of the 90 GHz branch line couplers (a) S-parameters (b) Amplitude and phase difference.

The simulated S-parameters results for a 300 GHz branch line coupler is shown in the Fig. 4.11 (a). Amplitude and phase difference between outputs ports are shown in Fig. 4.11 (b). The coupling ( $|S_{31}|$ ) and through ( $|S_{21}|$ ) achieved were -5.12 dB and -4.64 dB respectively with amplitude imbalance ( $|S_{31} - S_{21}|$ ) less than  $\pm 0.5$  dB. The return ( $|S_{11}|$ ) and isolation ( $|S_{41}|$ ) loss of -28.86 dB and -32.10 dB was noted separately with 19-dB percentage bandwidth (including insertion loss of transmission line) of 15.53 %. The output phase of  $90^\circ$  was obtained with a phase difference ( $\angle S_{31} - \angle S_{21}$ ) less than  $2^\circ$ .

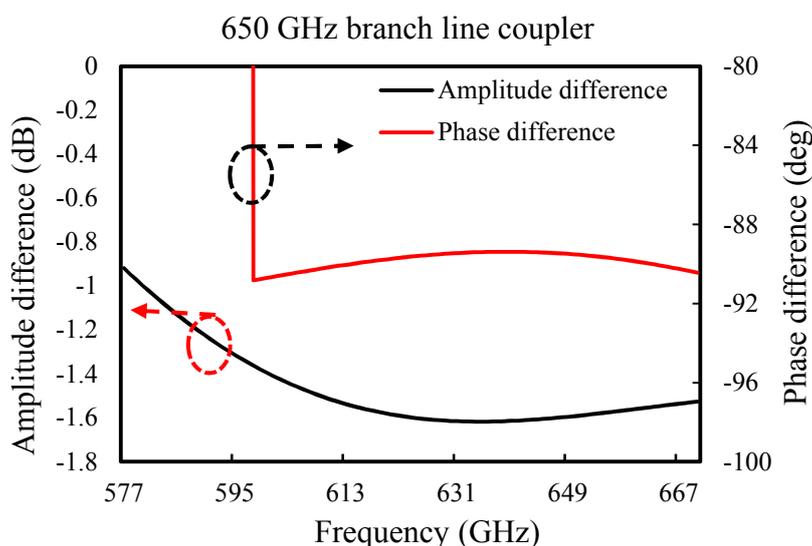


**Fig. 4.11:** Simulated performance of the 300 GHz branch line couplers (a) S-parameters (b) Amplitude and phase difference.

The simulated S-parameters results for a 650 GHz branch line coupler is shown in the Fig. 4.12 (a). The simulated return loss ( $|S_{11}|$ ) was lower than -25 dB from 577 to 670 GHz with a 14.95 % relative bandwidth, while isolation ( $|S_{41}|$ ) achieved was better than -30 dB for this circuit. The simulated transmission coefficients,  $|S_{21}|$  and  $|S_{31}|$  were -4.99 dB and -6.60 dB respectively. Fig. 4.12 (b) shows the simulated amplitude imbalance and 90° out-of-phase difference of 650 GHz branch line coupler. The amplitude ( $|S_{31} - S_{21}|$ ) of less than 2 dB from 600 to 670 GHz with phase difference ( $\angle S_{31} - \angle S_{21}$ ) of  $\pm 1^\circ$  was simulated.



(a)



(b)

**Fig. 4.12:** Simulated performance of the 650 GHz branch line couplers (a) S-parameters (b) Amplitude and phase difference.

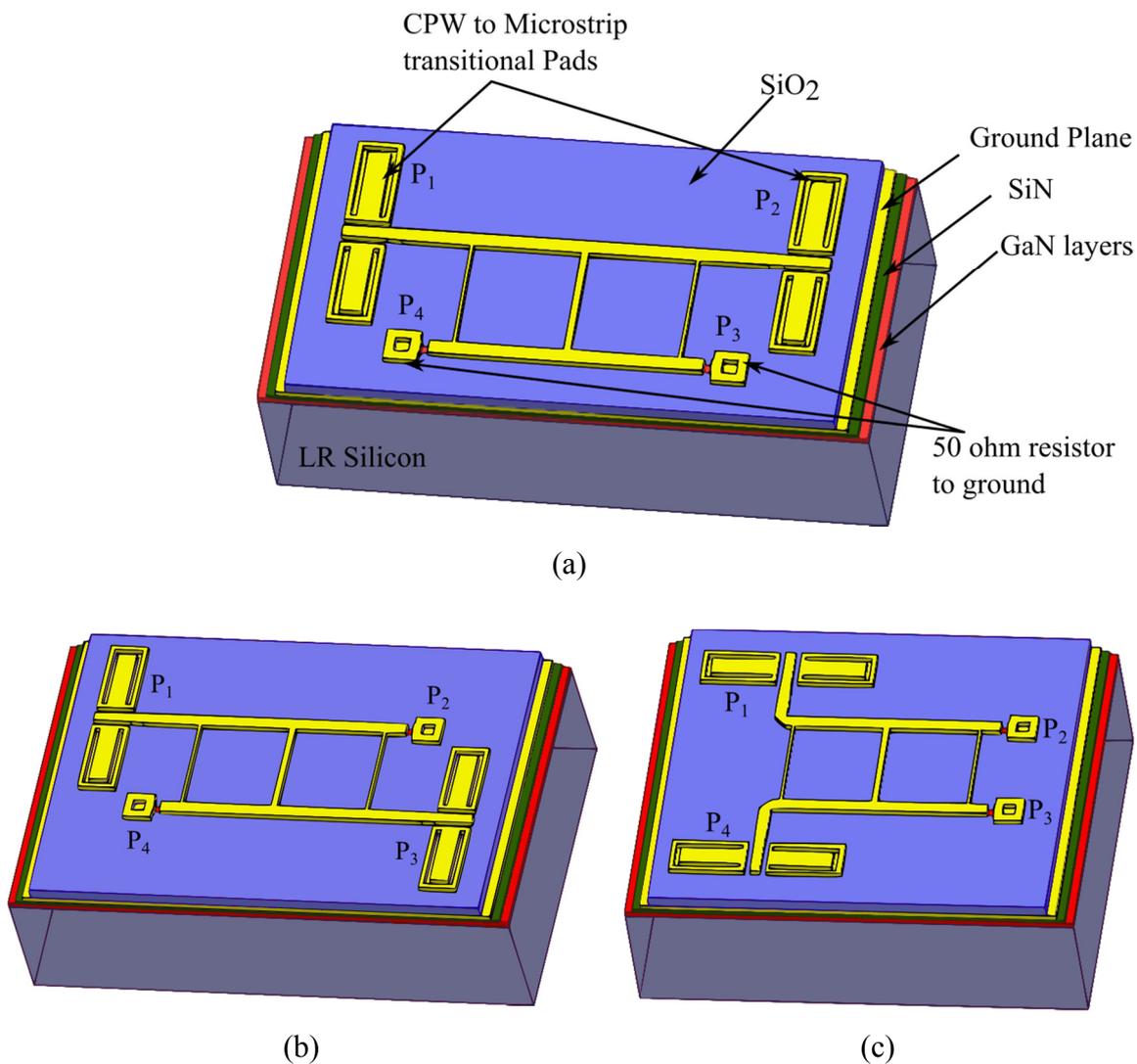
A summary of simulated results of the branch line coupler at each frequency is displayed in Table 4.2. The transmission coefficient ( $|S_{21}|$  and  $|S_{31}|$ ) achieved at 90 GHz were almost equal. However, as the operational frequency increased, there was an observation of signal loss in the coupled port ( $|S_{31}|$ ). This might have been due to dielectric loss. Return loss ( $|S_{11}|$ ) and isolation ( $|S_{41}|$ ) achieved at all three frequencies were better than -25 dB, but the phase difference ( $\angle S_{31} - \angle S_{21}$ ) presented by the devices at 90 GHz were higher compared to 300 GHz and 650 GHz, due to the length of the transmission line simulated different from  $\lambda/4$  at resonant frequency. Amplitude difference was higher in 650 GHz branch line coupler due to dielectric loss of SiO<sub>2</sub> being higher at those frequencies.

Coupler Parameters	Frequency (GHz)		
	90 GHz	300 GHz	650 GHz
Frequency (GHz)	82-96	268-313	577-670
Bandwidth (%)	15.77	15.53	14.95
Through, $ S_{21} $ (dB)	-4.36	-4.64	-4.99
Coupled, $ S_{31} $ (dB)	-4.18	-5.12	-6.60
Return loss, $ S_{11} $ (dB)	-25.25	-28.86	-29.27
Isolation, $ S_{41} $ (dB)	-32.48	-32.10	-34.58
Amplitude imbalance, $ S_{31}-S_{21} $ (dB)	< 0.5	< $\pm 0.5$	< $\pm 2$
Phase difference, $\angle S_{31} -$ $\angle S_{21}$ (deg)	178	< 2	< 1

**Table 4.2:** Summarized results of branch line coupler at each frequency.

#### 4.4.2 Cascaded branch line coupler

The 3D schematic of a cascaded branch line coupler is as shown in the Fig. 4.13. The circuit was divided in three ways to accommodate two-probe measurements. Two ports are measured each time ( $S_{11}$ ,  $S_{21}$ ), ( $S_{11}$ ,  $S_{31}$ ), ( $S_{11}$ ,  $S_{41}$ ) while the other two ports are terminated in  $50 \Omega$  resistors. A  $50 \Omega$  CPW to microstrip via-hole transition was attached at the end of transmission line for measurement compatibility. Table 4.3 shows the dimensions used for designing the cascaded branch line coupler at each frequency.

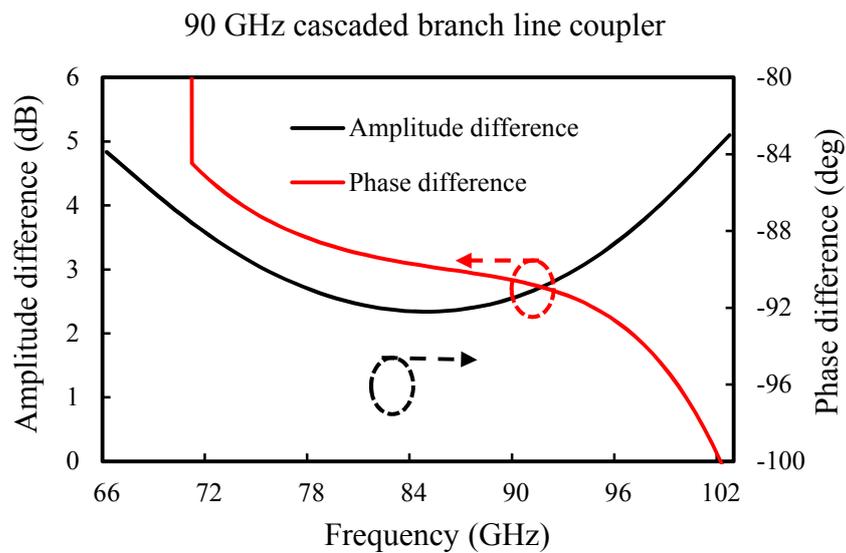
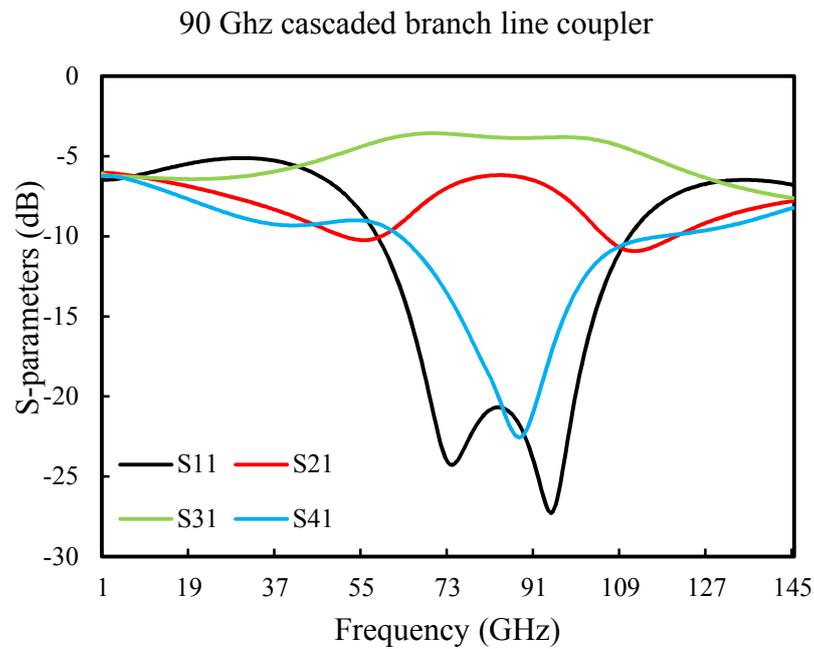


**Fig. 4.13:** 3D images of cascaded branch line coupler simulated for final two-port measurements (a) P<sub>1</sub> and P<sub>2</sub> measured (b) P<sub>1</sub> and P<sub>3</sub> measured (c) P<sub>1</sub> and P<sub>4</sub> measured.

Frequency (GHz)	50 $\Omega$ , $\lambda/4$		120.7 $\Omega$ , $\lambda/4$		70.71 $\Omega$ , $\lambda/4$		50 $\Omega$ , $\lambda/2$	
	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
90	19	478	1.6	521	9.7	521	19	100
300	19	150	2	149	9.5	149	19	80
650	37	60	3	60	37	60	19	40

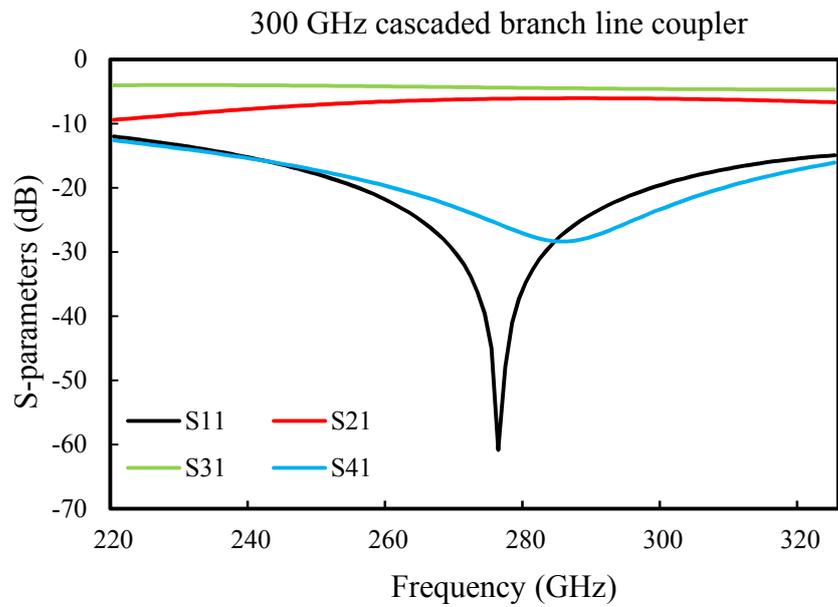
**Table 4.3:** Dimensions used for designing cascaded branch line coupler.

The simulated S-parameter results, amplitude and phase imbalance for a 90 GHz cascaded branch line coupler are shown in the Fig. 4.14. The coupled ( $|S_{31}|$ ) and through ( $|S_{21}|$ ) achieved was -3.82 and -6.19 dB respectively, with amplitude difference ( $|S_{31} - S_{21}|$ ) of 5 dB between them. Return loss ( $|S_{11}|$ ) and isolation ( $|S_{41}|$ ) loss as high as -27.28 and -22.56 was simulated. Bandwidth of 44.37 % was observed from 66 GHz to 102.5 GHz. The phase of the output ports ( $\angle S_{31} - \angle S_{21}$ ) was  $90^\circ$  with a difference of  $\pm 5^\circ$  between 75 GHz to 95 GHz.

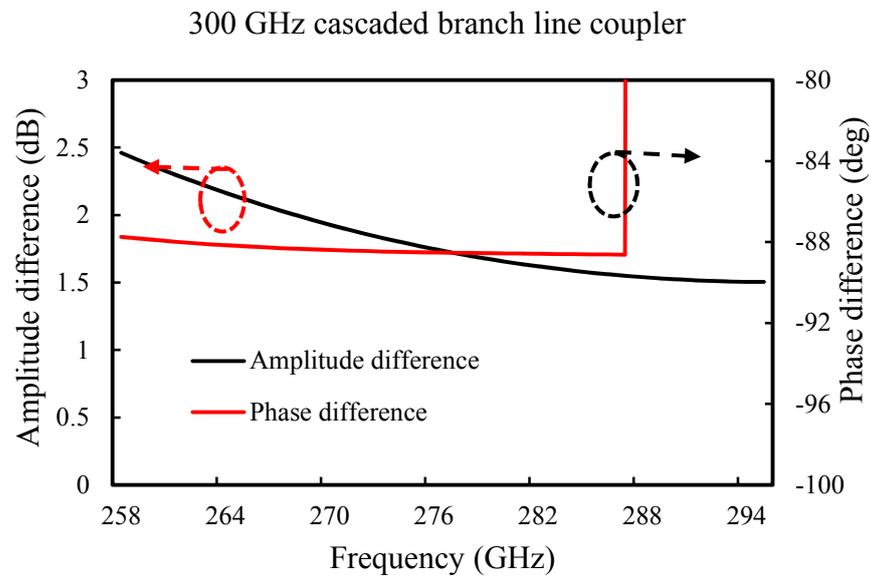


**Fig. 4.14:** Simulated performance of the 90 GHz cascaded branch line couplers (a) S-parameters (b) Amplitude and phase difference.

The simulated outcome of a 300 GHz cascaded branch line coupler is plotted in the Fig. 4.15. A return loss ( $|S_{11}|$ ) and isolation ( $|S_{41}|$ ) loss of -60.82 and -28.32 was reached separately. From frequency 220 to 325 GHz, the 21-dB bandwidth (including insertion loss of transmission line) achieved was 13.41 % and a transmission co-efficient ( $|S_{21}|$  and  $|S_{31}|$ ) of -6.16 and -4.30 dB was attained with amplitude difference ( $|S_{31} - S_{21}|$ ) of  $\pm 2.5$  dB. The phase ( $\angle S_{31} - \angle S_{21}$ ) achieved at two output ports was  $6^\circ$  between 258 GHz to 285 GHz.



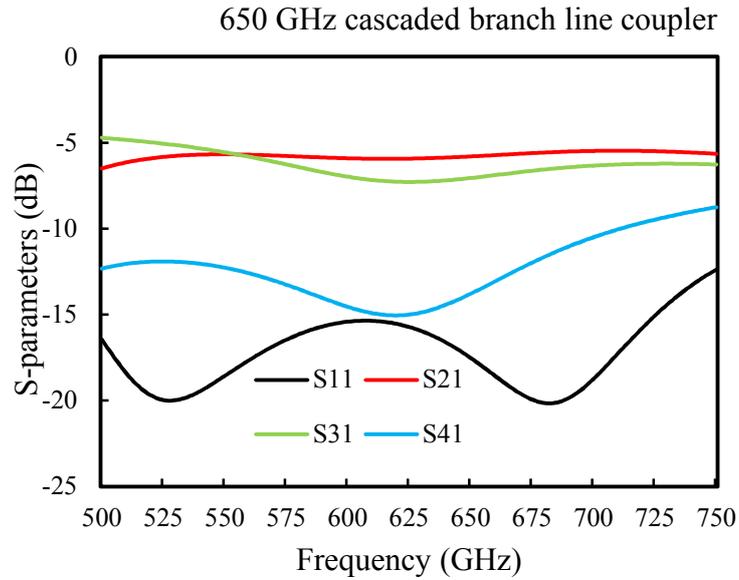
(a)



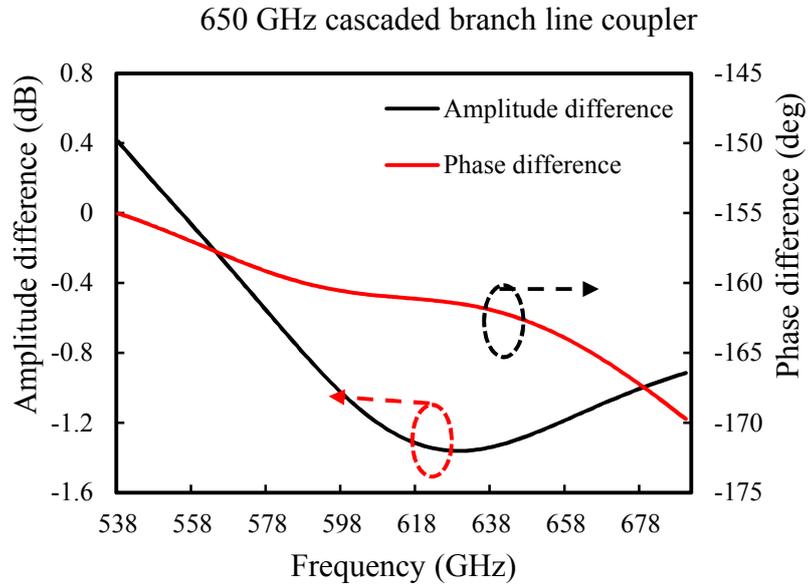
(b)

**Fig. 4.15:** Simulated performance of the 300 GHz cascaded branch line couplers (a) S-parameters (b) Amplitude and phase difference.

The simulated S-parameter result of a 650 GHz cascaded branch line coupler is as shown in the Fig. 4.16 (a). A 24.94 % fractional bandwidth was achieved from frequency 538 to 690 GHz, with -5.92 dB ( $|S_{21}|$ ) and -7.02 dB ( $|S_{31}|$ ) at the output ports. The return ( $|S_{11}|$ ) and isolation ( $|S_{41}|$ ) loss as high as -20.15 dB and -15.04 dB were reached. Fig. 4.16 (b) shows the amplitude ( $|S_{31} - S_{21}|$ ) and phase difference ( $\angle S_{31} - \angle S_{21}$ ) between two output ports. Maximum swing of amplitude values between the output ports was about  $\pm 1$  dB and phase of  $180^\circ$  was achieved with a difference of  $\pm 60^\circ$ .



(a)



(b)

**Fig. 4.16:** Simulated performance of the 650 GHz cascaded branch line couplers (a) S-parameters (b) Amplitude and phase difference.

A summary of simulated results for the cascaded branch line coupler at each frequency is arranged in the Table 4.4. The transmission co-efficient achieved ( $|S_{21}|$  and  $|S_{31}|$ ) at each frequency were not equal, possibly due to the losses in the dielectric or coupling loss. Since the design is cascade, the bandwidth realised is higher than in the single branch line coupler except for 300 GHz cascaded branch line coupler. The signal loss at the isolation port ( $|S_{41}|$ ) was lower at 650 GHz compared to other frequencies as the impedance of the transmission line was not achieved properly, but reflection coefficient achieved ( $|S_{11}|$ ) at these frequencies

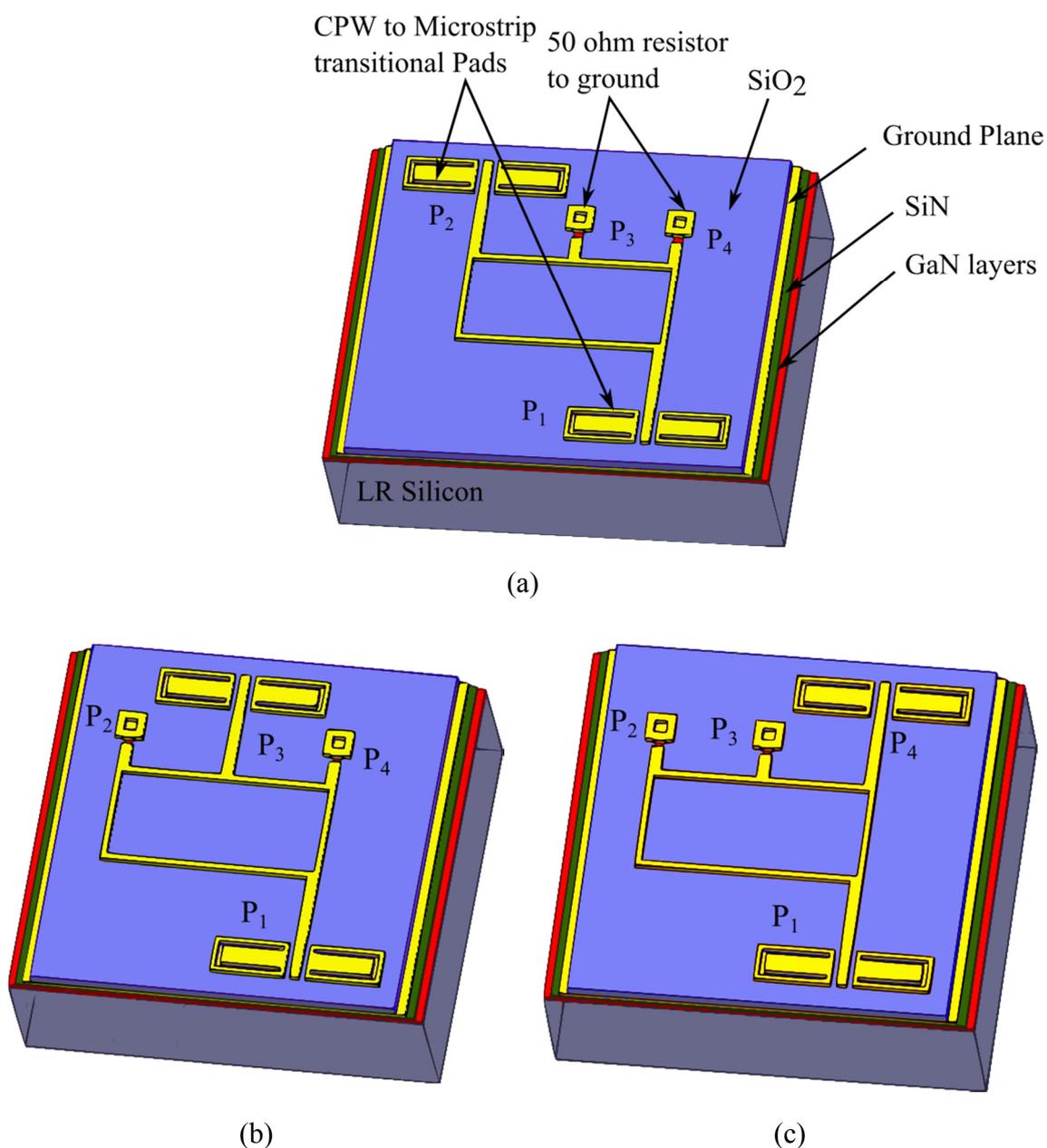
was better than -20 dB. Amplitude difference is higher at 90 GHz due to higher through port loss, and phase difference was higher at 650 GHz as the simulated length of the transmission line was different from  $\lambda/4$  at resonant frequency

Coupler Parameters	Frequency (GHz)		
	90 GHz	300 GHz	650 GHz
Frequency (GHz)	66-102.5	258-295	538-690
Bandwidth (%)	44.37	13.41	24.94
Through, $ S_{21} $ (dB)	-6.19	-6.16	-5.92
Coupled, $ S_{31} $ (dB)	-3.82	-4.30	-7.02
Return loss, $ S_{11} $ (dB)	-27.28	-60.82	-20.15
Isolation, $ S_{41} $ (dB)	-22.56	-28.36	-15.04
Amplitude imbalance, $ S_{31}-S_{21} $ (dB)	< 5	< 2.5	< $\pm 1$
Phase difference, $\angle S_{31} - \angle S_{21}$ (deg)	5	6	$\pm 25$

**Table 4.4:** Summarized results of cascaded branch line coupler at each frequency.

### 4.4.3 Rat race coupler

The 3D diagram of a rat race coupler is as shown in the Fig. 4.17. The coupler was designed for two-port measurements, where two ports are terminated with  $50\ \Omega$  resistors. A  $50\ \Omega$  CPW to microstrip via-hole transition was attached at the end of transmission line for measurement compatibility. The dimensions of transmission lines used for simulating the rat race coupler is summarised in Table 4.5.

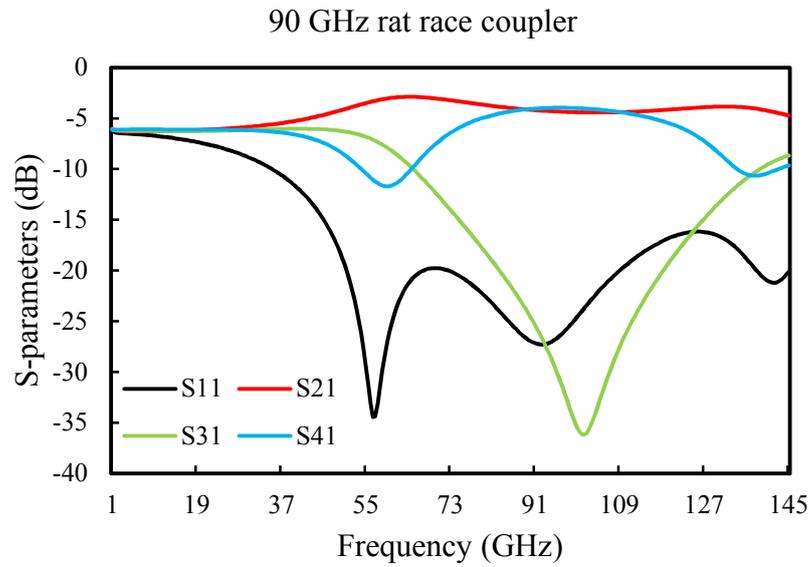


**Fig. 4.17:** 3D images of rat race coupler simulated for final two-port measurements (a) P<sub>1</sub> and P<sub>2</sub> measured (b) P<sub>1</sub> and P<sub>3</sub> measured (c) P<sub>1</sub> and P<sub>4</sub> measured.

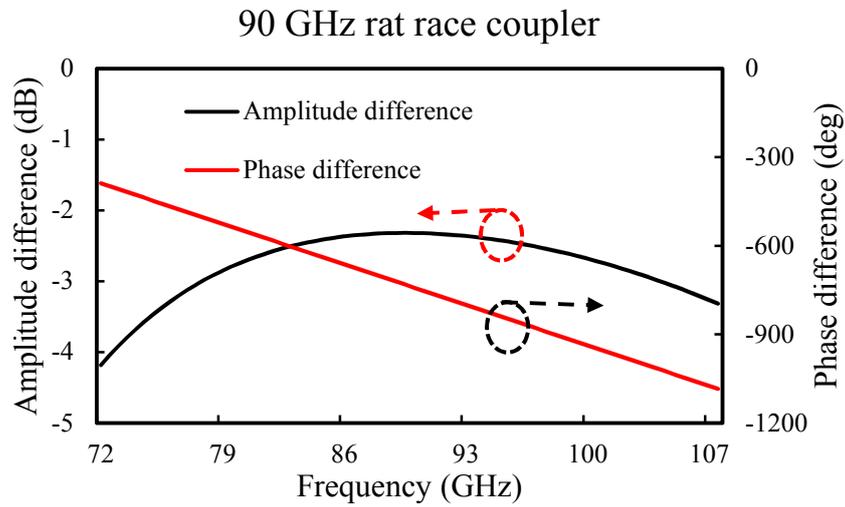
Frequency (GHz)	70.71 $\Omega$ , $\lambda/4$		70.71 $\Omega$ , $3\lambda/4$			50 $\Omega$ , $\lambda/2$	
	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Radius ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
90	5	240	5	240	100	19	100
300	9.5	165	9.5	149	85	19	80
650	9.5	60	9.5	60	50	19	40

**Table 4.5:** Dimensions used for implementing a rat race coupler.

The simulated outcome of the 90 GHz rat race coupler is shown in the Fig. 4.18. The transmission coefficient ( $|S_{21}|$  and  $|S_{41}|$ ) attained were about -3.75 and -4 dB separately, with a 16dB fractional bandwidth (including transmission line insertion loss) of 101.02%. The return loss ( $|S_{11}|$ ) and isolation ( $|S_{31}|$ ) loss at Port 1 and 3 were -27.27 and -36.18 dB respectively. The amplitude ( $|S_{41} - S_{21}|$ ) and phase difference ( $\angle S_{31} - \angle S_{11}$ ) between the two output ports achieved correspondingly was 4.5 dB and  $1000^\circ$  between 72 GHz and 108 GHz.



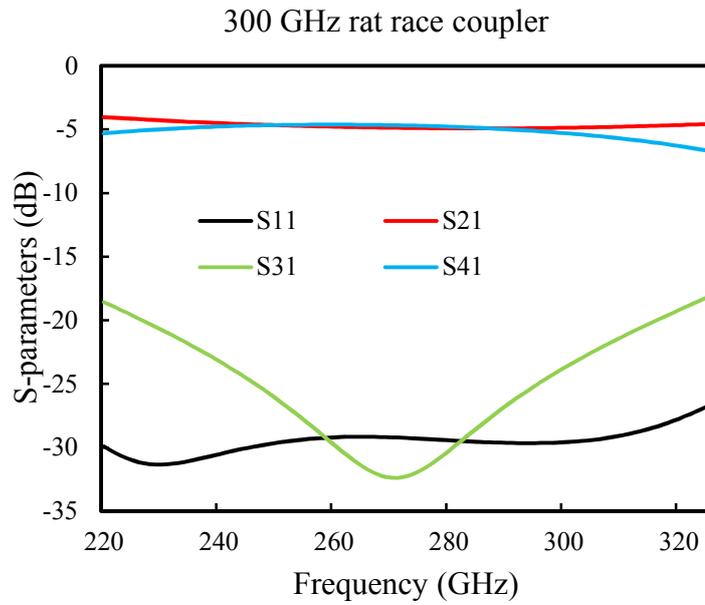
(a)



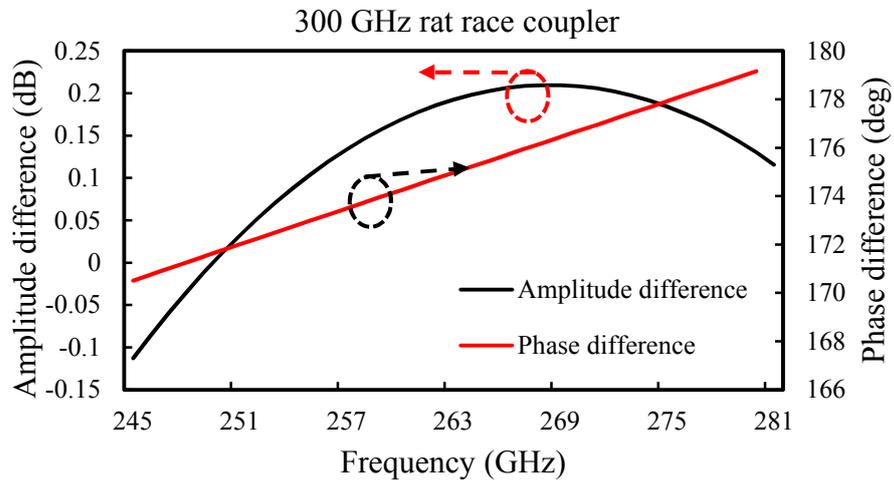
(b)

**Fig. 4.18:** Simulated performance of the 90 GHz rat race couplers (a) S-parameters (b) Amplitude and phase difference.

The S-parameter plot of a simulated 300 GHz rat race coupler is shown in the Fig. 4.19, along with a plot of amplitude and phase difference between two output ports. The ( $|S_{21}|$  and  $|S_{41}|$ ) transmission coefficient ( $|S_{21}|$  and  $|S_{41}|$ ) achieved was similar at -4 dB, with amplitude difference ( $|S_{41} - S_{21}|$ ) of  $\pm 2$  dB between them. The reflection co-efficient ( $|S_{11}|$  and  $|S_{31}|$ ) noted were as low as -29.15 dB and -32.38 dB respectively with fractional bandwidth of 13.72 %. The phase ( $\angle S_{31} - \angle S_{41}$ ) achieved was  $180^\circ$  with  $8^\circ$  variation in the output ports between 245 GHz and 281 GHz.



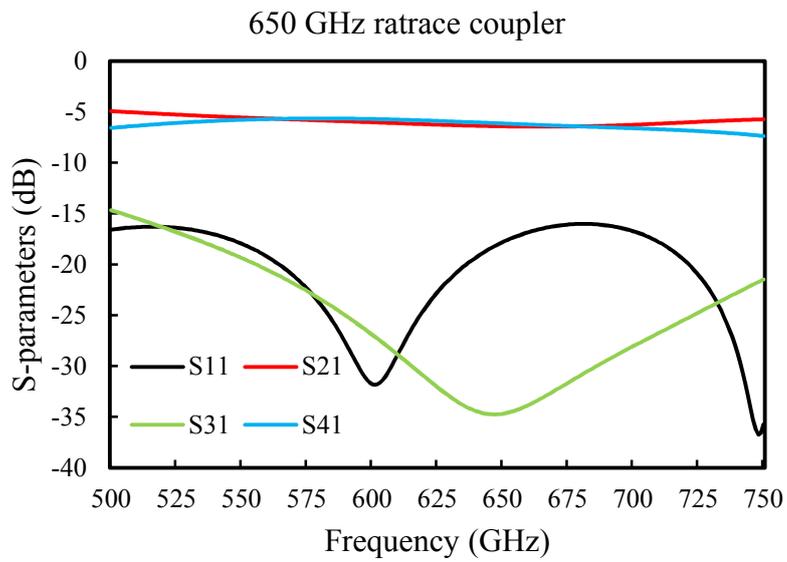
(a)



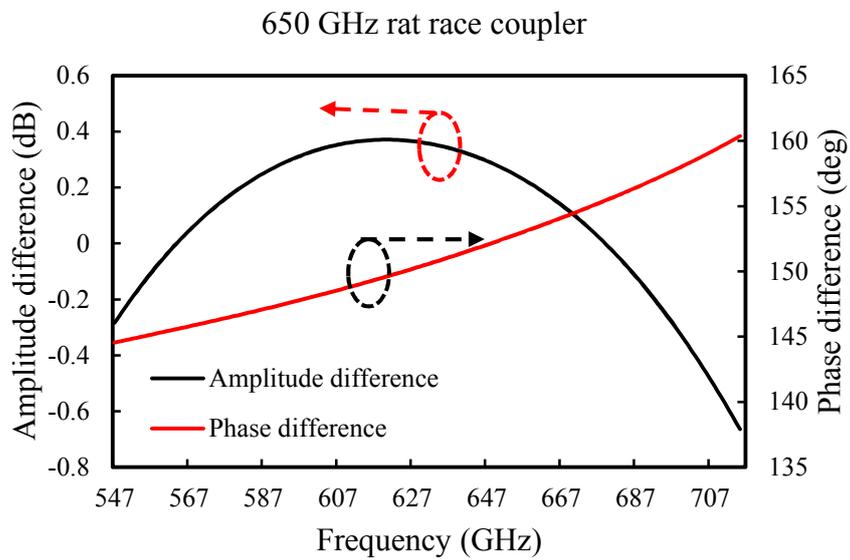
(b)

**Fig. 4.19:** Simulated performance of the 300 GHz rat race couplers (a) S-parameters (b) Amplitude and phase difference.

The S-parameter plot of a simulated 650 GHz rat race coupler is shown in Fig. 4.20. The transmission co-efficient ( $|S_{21}|$  and  $|S_{41}|$ ) simulated was -6.29 and -5.68 dB respectively. Fractional bandwidth of 26.86 % was achieved between frequencies 547 to 715 GHz with reflection co-efficient ( $|S_{11}|$  and  $|S_{31}|$ ) as low as -31.83 and -34.73 dB. The amplitude ( $|S_{41} - S_{21}|$ ) and phase ( $\angle S_{31} - \angle S_{11}$ ) difference observed individually between output ports were as small as  $\pm 0.7$  dB and  $\pm 40^\circ$ .



(a)



(b)

**Fig. 4.20:** Simulated performance of the 650 GHz rat race couplers (a) S-parameters (b) Amplitude and phase difference.

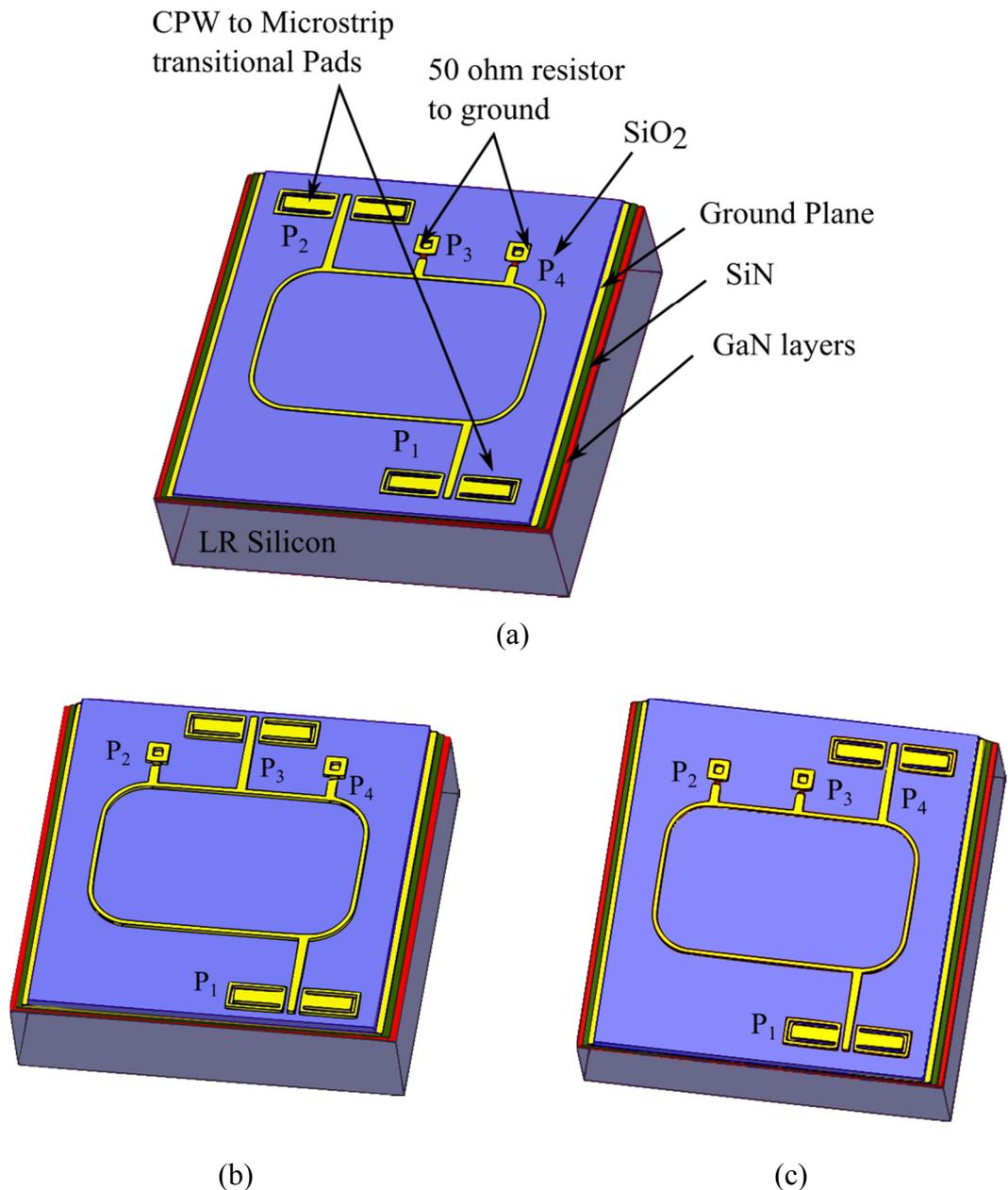
Summarized outcome of the rat race coupler at each frequency is shown in Table 4.6. Power achieved at the two output ports ( $|S_{21}|$  and  $|S_{41}|$ ) was almost equal but the loss increased with frequencies due to dielectric loss, and loss from  $90^\circ$  bend at the corners and matching at Port 1 ( $|S_{11}|$ ) and isolation at Port 3 ( $|S_{31}|$ ) were below -27 dB at all frequencies. Simulated bandwidth achieved at 90 GHz was higher compared to 300 GHz and 650 GHz. In addition, phase difference at 90 GHz was higher compared with other frequencies as the simulated length of transmission line was different from  $\lambda/4$  at resonant frequency.

Coupler Parameters	Frequency (GHz)		
	90 GHz	300 GHz	650 GHz
Frequency (GHz)	47.5-125.5	245-281	547-715
Bandwidth (%)	101.02	13.72	26.86
Transmission, $ S_{21} $ (dB)	-3.75	-4.87	-6.29
Transmission, $ S_{41} $ (dB)	-4	-4.62	-5.68
Return loss, $ S_{11} $ (dB)	-27.27	-29.15	-31.83
Isolation, $ S_{31} $ (dB)	-36.18	-32.38	-34.73
Amplitude imbalance, $ S_{41}-S_{21} $ (dB)	< 4.5	< $\pm 2$	< $\pm 0.7$
Phase difference, $\angle S_{41} -$ $\angle S_{21}$ (deg)	1000	8	40

**Table 4.6:** Summarized results of rat race coupler at each frequency.

#### 4.4.4 Curved rat race coupler

To avoid the losses from the sudden bend ( $90^\circ$  bend) of the rat race couplers, curved rat race couplers were designed. Fig. 4.21 shows the 3D diagram of a curved rat race coupler fit for 2 probe measurements where two-ports are terminated in  $50\ \Omega$  resistors. A  $50\ \Omega$  CPW to microstrip via-hole transition was attached at the end of transmission line for measurement compatibility. Table 4.7 shows the dimensions of transmission lines used in the design of the curved rat race coupler.

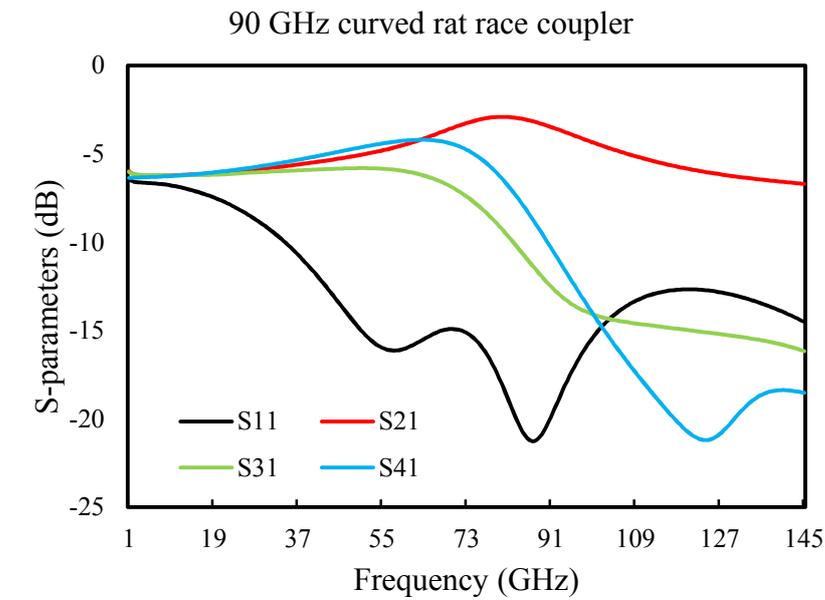


**Fig. 4.21:** 3D images of curved rat race coupler simulated for final two-port measurements (a) P<sub>1</sub> and P<sub>2</sub> measured (b) P<sub>1</sub> and P<sub>3</sub> measured (c) P<sub>1</sub> and P<sub>4</sub> measured.

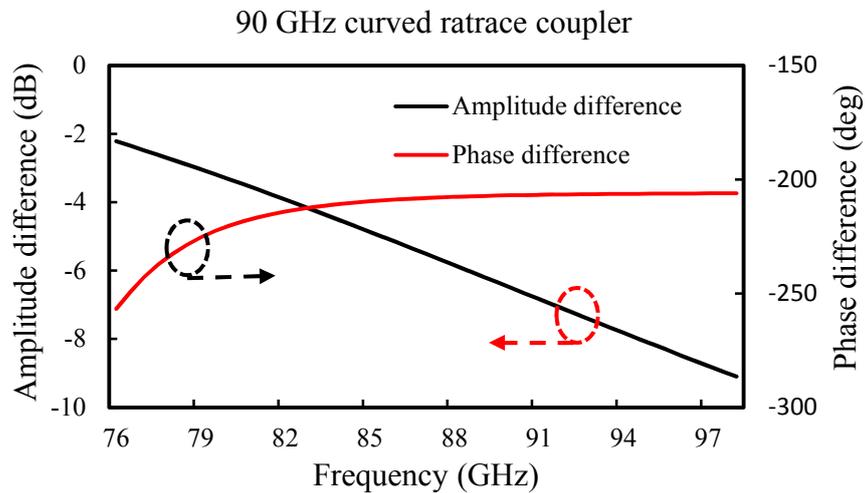
Frequency (GHz)	70.71 $\Omega$ , $\lambda/4$		70.71 $\Omega$ , $3\lambda/4$		50 $\Omega$ , $\lambda/2$	
	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
90	5	425	5	1275	19	100
300	9.5	149	9.5	447	19	80
650	10	55	10	165	19	70

**Table 4.7:** Dimensions used for designing curved rat race coupler.

The simulated output results of the 90 GHz curved rat race coupler are shown in the Fig. 4.22. The transmission co-efficient ( $|S_{21}|$  and  $|S_{41}|$ ) achieved were -2.91 and -4.21 dB respectively, with amplitude difference ( $|S_{21}| - |S_{41}|$ ) between them of 8 dB. A return loss ( $|S_{11}|$ ) of -21.24 and isolation loss ( $|S_{31}|$ ) of -15 dB were simulated and fractional bandwidth demonstrated was 25.49 % from frequency range of 34.5 to 145 GHz. The output phase difference ( $\angle S_{41} - \angle S_{21}$ ) achieved was  $\pm 10^0$  in this design between 76 GHz and 98 GHz.



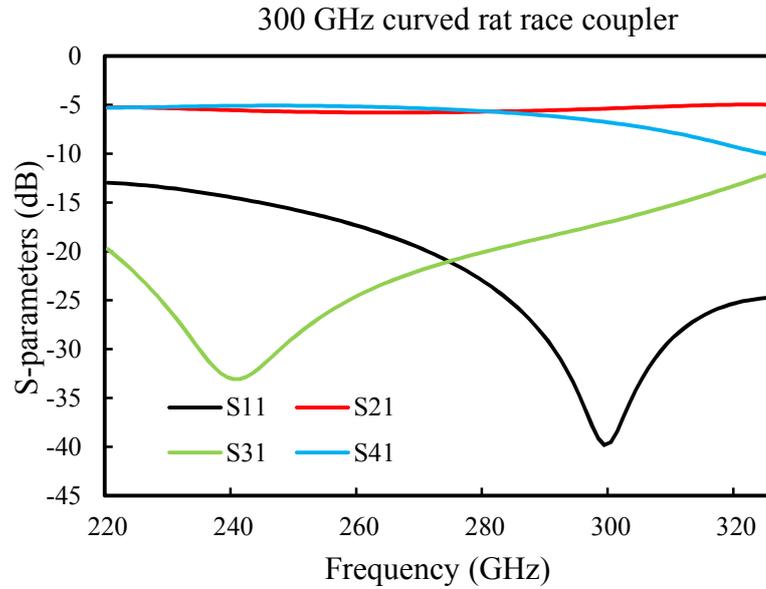
(a)



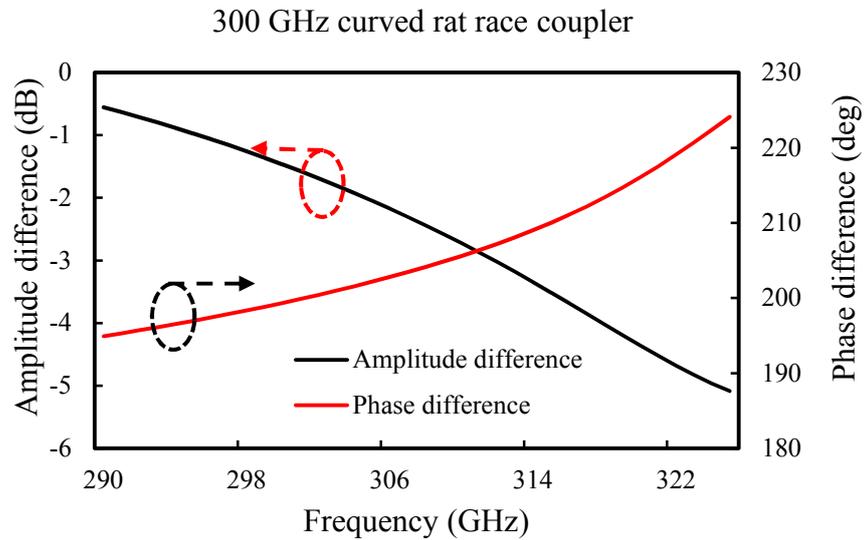
(b)

**Fig. 4.22:** Simulated performance of the 90 GHz curved rat race couplers (a) S-parameters (b) Amplitude and phase difference.

The output plot of the 300 GHz curved rat race coupler is shown in Fig. 4.23 (a). The power transmission ( $|S_{21}|$  and  $|S_{41}|$ ) achieved were similar at -5 dB. Fractional bandwidth of 11.4 % was observed between frequency 290 to 325 GHz. Return loss of -40 dB ( $|S_{11}|$ ) and isolation loss ( $|S_{31}|$ ) of -33.08 dB was reached using this design. The amplitude ( $|S_{41}| - |S_{21}|$ ) and phase imbalance ( $\angle S_{41} - \angle S_{21}$ ) between two output ports are plotted in Fig. 4.23 (b). Amplitude difference as low as 5 dB was attained and phase difference of  $\pm 40^\circ$  was noted in this design.



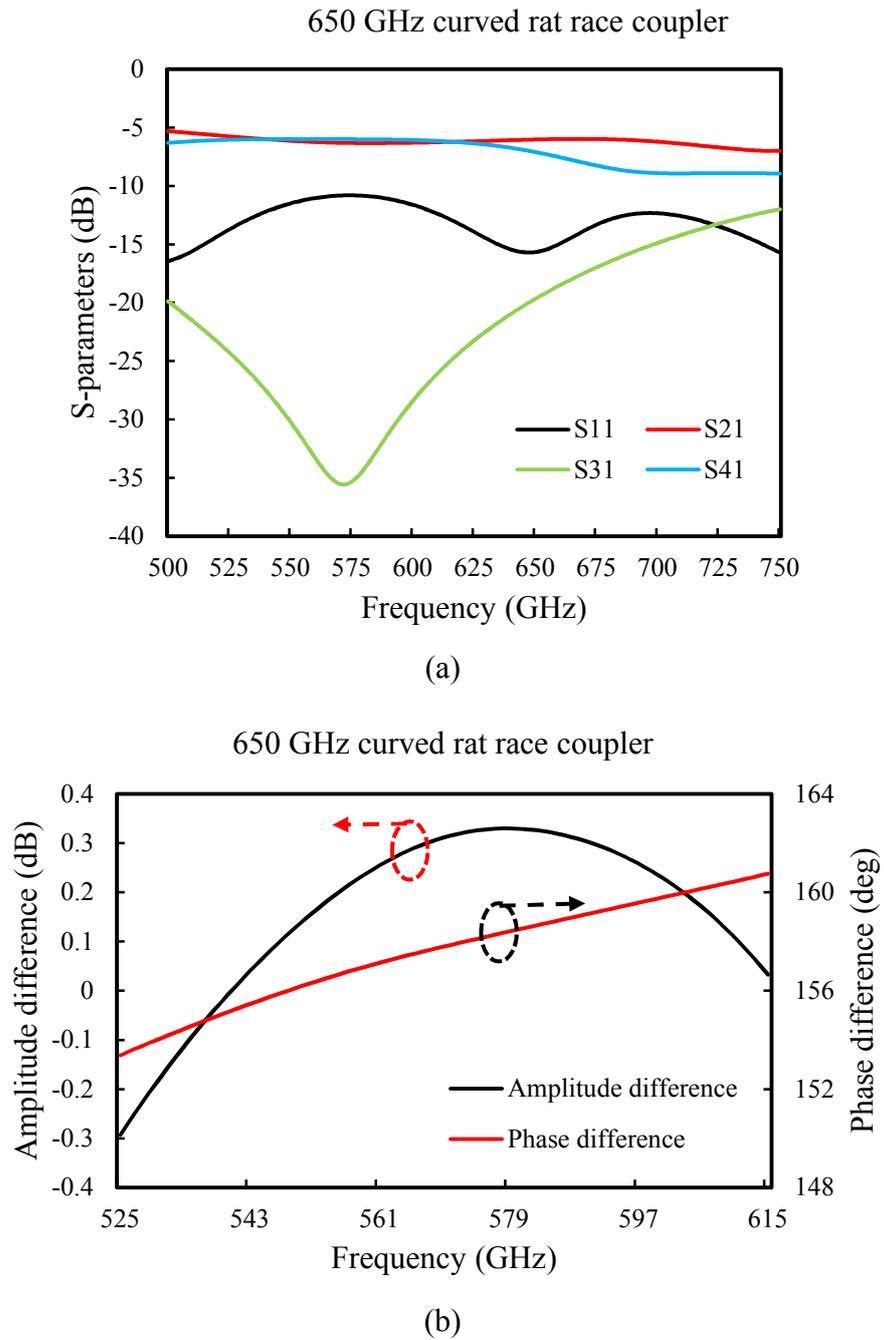
(a)



(b)

**Fig. 4.23:** Simulated performance of the 300 GHz curved rat race couplers (a) S-parameters (b) Amplitude and phase difference.

The simulated S-parameter results of a 650 GHz curved rat race coupler is shown in Fig. 4.24 (a). A 15.83% fractional bandwidth was achieved using this design from frequency 525-615 GHz. A -6.11 dB and -5.99 dB transmission coefficient ( $|S_{21}|$  and  $|S_{41}|$ ) was reached with -15 dB return loss ( $|S_{11}|$ ) and -11 dB isolation loss ( $|S_{31}|$ ). The data of amplitude ( $|S_{41}| - |S_{21}|$ ) and phase difference ( $\angle S_{41} - \angle S_{21}$ ) between the output ports are plotted in Fig. 4.24 (b). A  $\pm 0.3$  dB and  $\pm 20^\circ$  amplitude and phase difference respectively were noted in this design.



**Fig. 4.24:** Simulated performance of the 650 GHz curved rat race couplers (a) S-parameters (b) Amplitude and phase difference.

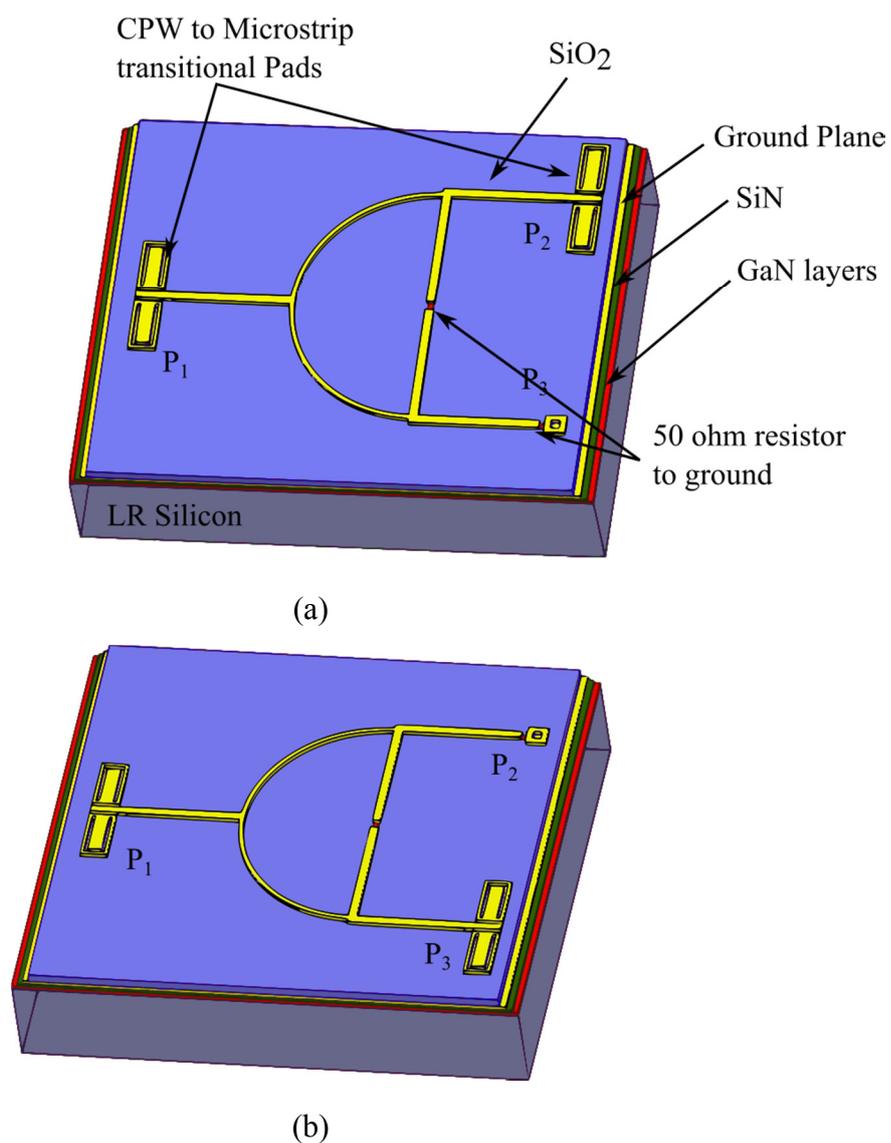
The overall results achieved for the curved rat race coupler at each frequency is shown in Table 4.8. In general, curved rat race simulation performed worse compared to the rat race coupler. While the use of a curved configuration was meant to improve performance, the simulation showed deteriorated results due to the geometry of the bend being poorly optimised. Further study is required to determine the effect of angle and radius of the bend on the performance of the circuit at these frequencies.

Coupler Parameters	Frequency (GHz)		
	90 GHz	300 GHz	650 GHz
Frequency (GHz)	76-98	290-325	525-615
Bandwidth (%)	25.49	11.4	15.83
Transmission, $ S_{21} $ (dB)	-2.91	-5.40	-6.11
Transmission, $ S_{41} $ (dB)	-4.21	-5.07	-5.99
Return loss, $ S_{11} $ (dB)	-21.24	-40	-15.70
Isolation, $ S_{31} $ (dB)	-15	-33.08	-11
Amplitude imbalance, $ S_{41}-S_{21} $ (dB)	8	5	$\pm 0.3$
Phase difference, $\angle S_{41} -$ $\angle S_{21}$ (deg)	$\pm 10$	40	20

**Table 4.8:** Summarized results of curved rat race coupler at each frequency.

#### 4.4.5 Wilkinson power divider

The 3D diagram of a Wilkinson power divider is depicted in Fig. 4.25. The circuit is meant for two-port measurement, where the third port is terminated in a  $50\ \Omega$  resistor. A  $50\ \Omega$  CPW to microstrip via-hole transition was attached at the end of transmission line for measurement compatibility. The dimensions of the transmission lines used for the design of this circuit are shown in Table 4.9.

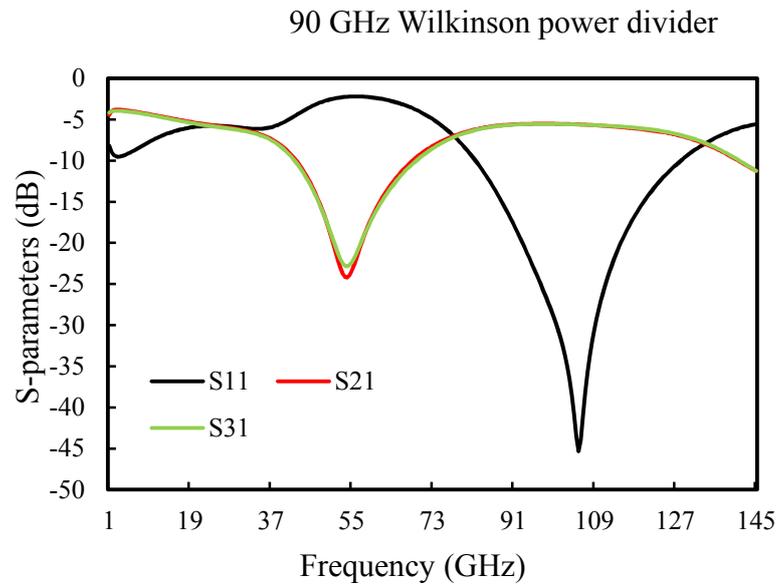


**Fig. 4.25:** 3D images of Wilkinson power divider simulated for final two-port measurements (a) P<sub>1</sub> and P<sub>2</sub> measured (b) P<sub>1</sub> and P<sub>3</sub> measured.

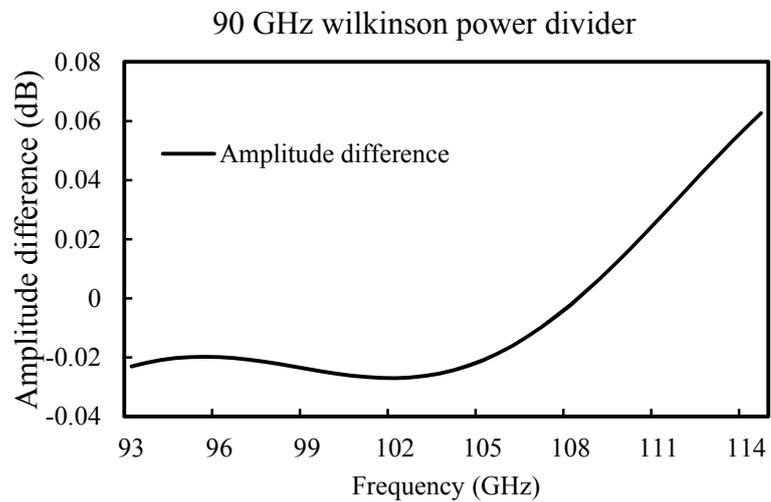
Frequency (GHz)	70.71 $\Omega$ , $\lambda/4$		50 $\Omega$ , $\lambda/2$	
	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )	Width ( $\mu\text{m}$ )	Length ( $\mu\text{m}$ )
90	10	775	19	300
300	9.5	280	19	280
650	9.5	115	19	115

**Table 4.9:** Dimensions used for designing Wilkinson power divider.

The simulated S-parameter results for a 90 GHz Wilkinson power divider are plotted in Fig. 4.26 (a). A bandwidth of 20.83 % was noted between 93 GHz to 114.5 GHz (20-dB bandwidth). The power through coupled ( $|S_{31}|$ ) and through ( $|S_{21}|$ ) achieved was equal to -5.6 dB and return loss ( $|S_{11}|$ ) achieved was as low as -45.32 dB. The amplitude difference ( $|S_{31}| - |S_{21}|$ ) between the output ports is plotted in Fig. 4.26 (b) with  $\pm 0.06$  dB achieved for this design.



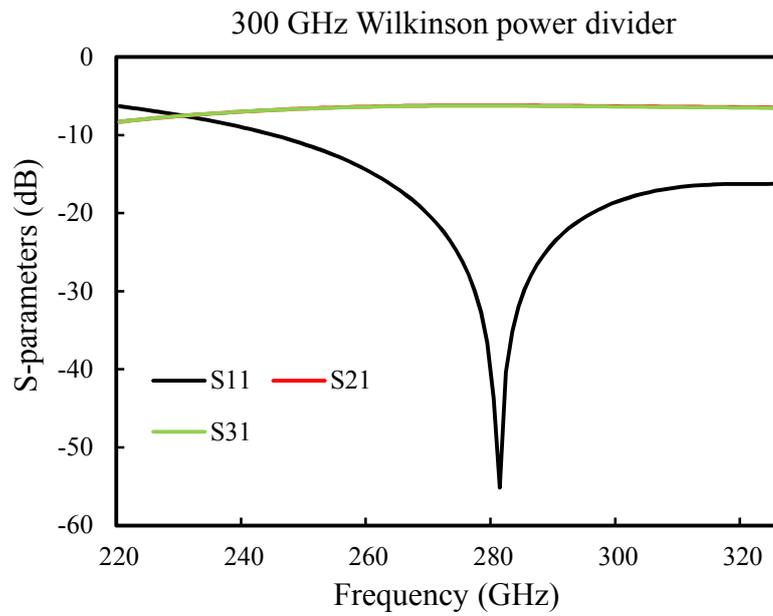
(a)



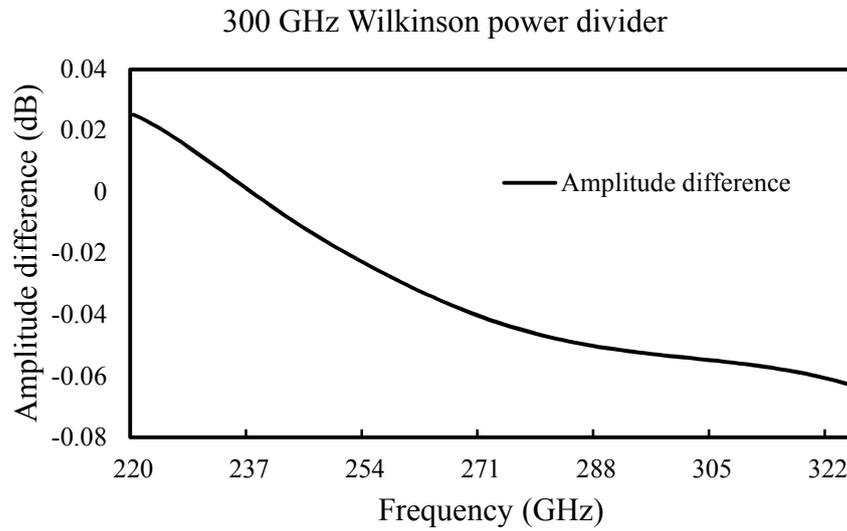
(b)

**Fig. 4.26:** Simulated performance of the 90 GHz Wilkinson power divider (a) S-parameters (b) Amplitude and phase difference.

The output results for a 300 GHz Wilkinson power divider are shown in Fig. 4.27. A transmission coefficient ( $|S_{21}|$  and  $|S_{31}|$ ) of -6 dB and return loss ( $|S_{11}|$ ) of -55.13 dB was achieved. A 16-dB fractional bandwidth of 21.20% was observed between frequencies 263 to 325 GHz. An amplitude difference ( $|S_{31}| - |S_{31}|$ ) of  $\pm 0.06$  dB was noted between the output arms.



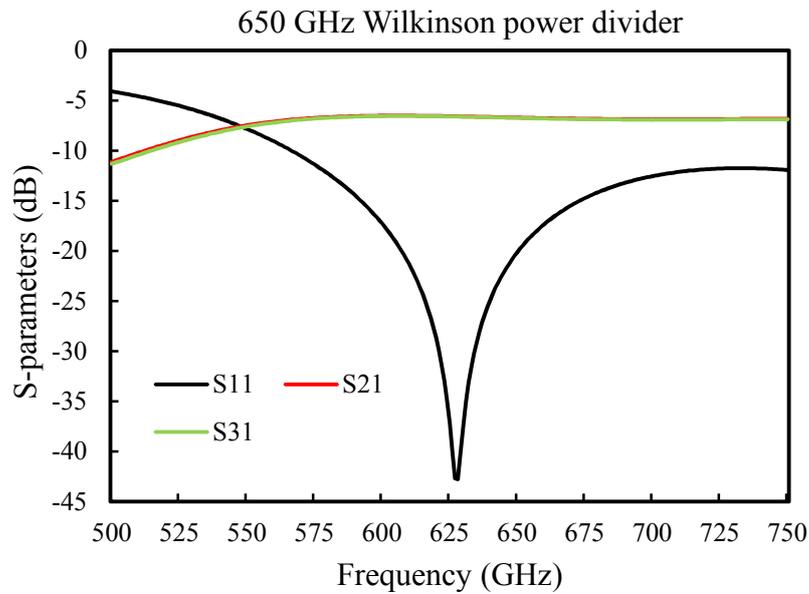
(a)



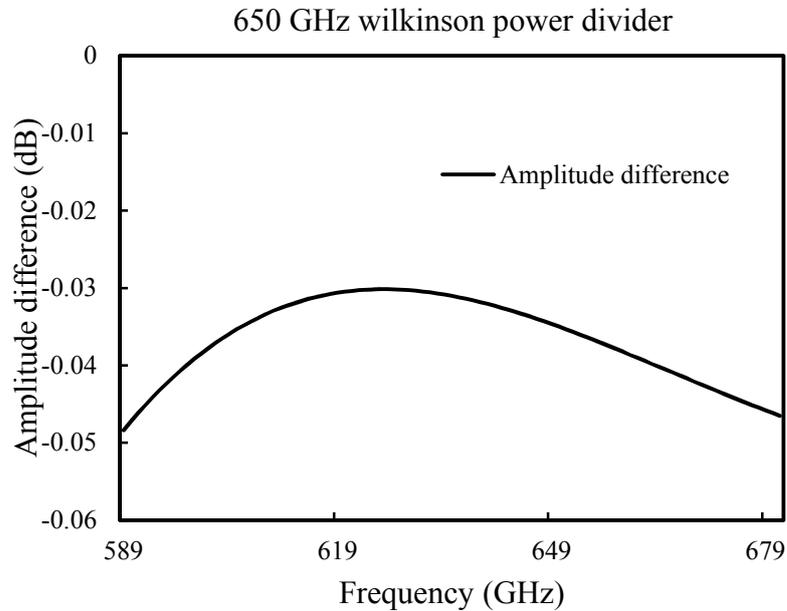
(b)

**Fig. 4.27:** Simulated performance of the 300 GHz Wilkinson power divider (a) S-parameters (b) Amplitude and phase difference.

The simulated output plots for 650 GHz are shown in the Fig. 4.28. The coupled and through port ( $|S_{31}|$  and  $|S_{21}|$ ) achieved was -6 dB. Return loss ( $|S_{11}|$ ) as low as -42.77 dB with 14-dB bandwidth (including transmission line insertion line) of 14.52 % was simulated between 589 and 681 GHz. An amplitude difference ( $|S_{31}| - |S_{31}|$ ) of 0.05 dB was observed between the two output ports in this design.



(a)



(b)

**Fig. 4.28:** Simulated performance of the 650 GHz Wilkinson power divider (a) S-parameters (b) Amplitude and phase difference.

A summary of results for the Wilkinson power divider are shown in Table 4.10. In general, the matching achieved at Port 1 ( $|S_{11}|$ ) was lower than -42 dB and the power ( $|S_{21}| - |S_{31}|$ ) between output ports was divided equally at each frequency. Comparing transmission coefficient ( $|S_{21}|$  and  $|S_{31}|$ ) with respect to frequency, there is a notable loss as the frequency increases. This may be due to an increase in dielectric loss of  $\text{SiO}_2$  at higher frequencies.

Coupler Parameters	Frequency (GHz)		
	90 GHz	300 GHz	650 GHz
Frequency (GHz)	93-114.5	263-325	589-681
Bandwidth (%)	20.83	21.20	14.52
Through, $ S_{21} $ (dB)	-5.62	-6.19	-6.58
Coupled, $ S_{31} $ (dB)	-5.60	-6.24	-6.64
Return loss, $ S_{11} $ (dB)	-45.32	-55.13	-42.77
Amplitude imbalance, $ S_{31}-S_{21} $ (dB)	$\pm 0.06$	$\pm 0.06$	0.05

**Table 4.10:** Summarized results of Wilkinson power divider at each frequency.

## 4.5 Fabrication

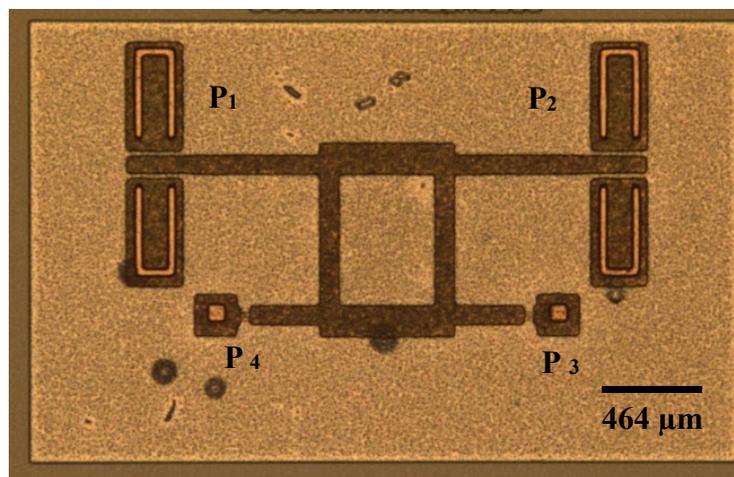
The devices simulated in this chapter thus far were fabricated using techniques outlined in Chapter 2. The fabrication process started with the deposition of Al metal (1  $\mu\text{m}$ ) using an e-beam evaporator (ground plane or shielding) on GaN-on LR Silicon. Then, 10  $\mu\text{m}$   $\text{SiO}_2$  dielectric was deposited using a PECVD process. Next, via-holes for connecting ground metal to the circuit was defined using photolithography and etched using the SPTS etch tool. NiCr (100 nm) metal was deposited using a standard lift-off process to define the 50  $\Omega$  resistor features. Finally, the top metal layer (signal tracks) were electroplated and patterned using a standard lift-off process with Ti/Au (50/2000 nm).

## 4.6 Measurement and results discussion

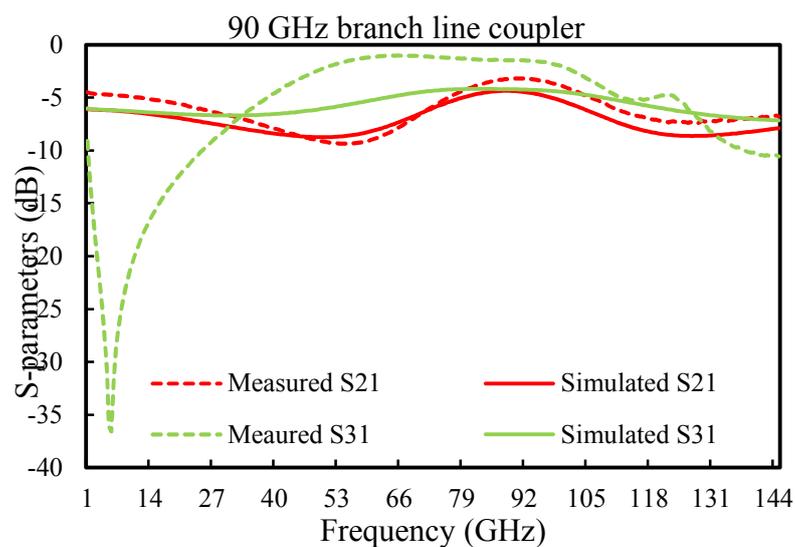
On-wafer measurements of small signal S-parameters were performed using an Agilent PNA network analyser over the frequency ranges 1 - 145 GHz, 220 - 325 GHz, and 500 - 750 GHz. The system was calibrated using the LRRM (line-reflect-reflect-match) calibration technique based on an off-chip ISS impedance standard. 50  $\mu\text{m}$  pitch Picoprobes were used for probing the via-hole CPW to microstrip transition pads and the samples were placed on a thick quartz spacer to eliminate any possible parasitic substrate modes caused by the metal chuck. The couplers were designed to fit two-port pair measurement and the other two ports were terminated with 50  $\Omega$  resistors. In this way, three sets of measurements ( $S_{11}$ ,  $S_{21}$ ), ( $S_{11}$ ,  $S_{31}$ ), ( $S_{11}$ ,  $S_{41}$ ) were carried out which describes the overall performance of the coupler. Samples were sent for measurement at the Fraunhofer institute in Germany. Due to a delay in measurement, only two devices (90 GHz branch line and cascaded branch line coupler) are presented here.

### 4.6.1 90 GHz Branch line coupler

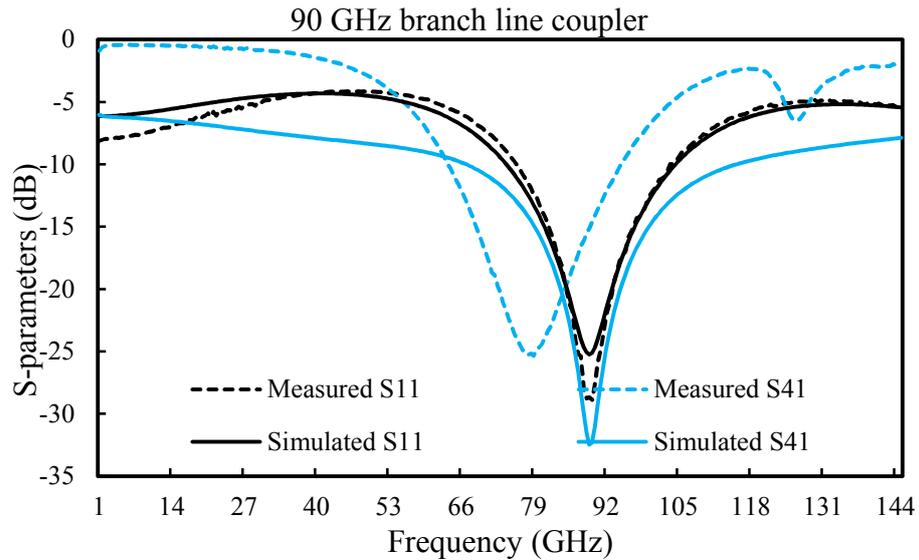
Optical images of fabricated branch line couplers are shown in the Fig. 4.29. The parameters used for fabrication were same as the simulated parameters detailed in Section 4.4.1, Page 158. The measured and simulated S-parameters result is plotted in Fig. 4.30 and Fig. 4.31. The measured transmission coefficient ( $|S_{21}|$  and  $|S_{31}|$ -dotted lines) achieved were -3.17 and -1 dB respectively, with amplitude difference ( $|S_{21}| - |S_{31}|$ ) between them being  $\pm 7$  dB. The return loss ( $|S_{11}|$ -black dotted line) of -28.8 dB and isolation ( $|S_{41}|$ -blue dotted line) of -24.8 dB were measured. In addition, fractional bandwidth demonstrated was 23.27 % from frequency range 76.5 to 96.5 GHz (18 dB bandwidth including transmission line insertion loss).



**Fig. 4.29:** Optical images of fabricated branch line coupler.



**Fig. 4.30:** Measured and simulated  $S_{21}$  and  $S_{31}$  parameters results for the 90 GHz branch line coupler.



**Fig. 4.31:** Measured and simulated  $S_{11}$  and  $S_{41}$  parameters results for the 90 GHz branch line coupler.

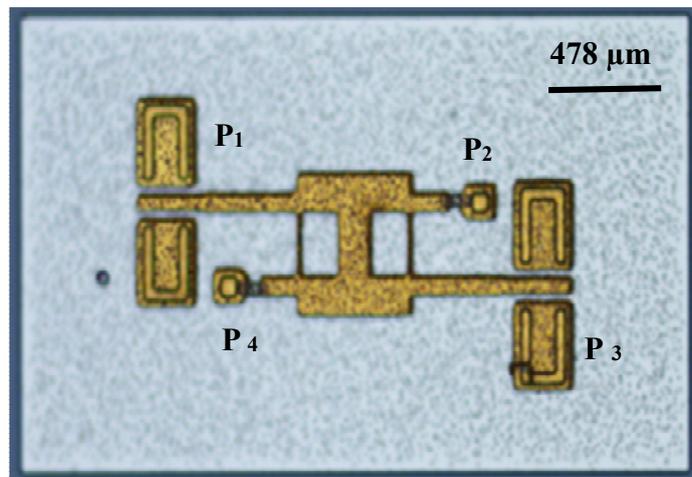
Table 4.11 shows a summary of simulated and measured results for the 90 GHz branch line coupler. Both return loss ( $|S_{11}|$ ) and isolation loss ( $|S_{41}|$ ) achieved in the measured results show good agreement with the simulated values. The power at coupled port ( $|S_{31}|$ ) was measured at -3.17 dB, whereas at the through port ( $|S_{21}|$ ) it was -1 dB. The higher power at through port might be due to a coupling issue in the circuit. Coupled port showed resonance at lower frequency due to the length of the transmission line, impedance of the quarter wavelength transmission line not achieving  $Z_0\sqrt{2}$  at resonant frequency. The fractional bandwidth demonstrated by the measured result was in close agreement with the simulated result, and the measured phase difference was  $18^\circ$  higher than the simulated value as the device didn't achieve  $\lambda/4$  length at resonant frequency.

Couplers Parameters	Simulated	Measured
Frequency (GHz)	82-96	84-94
Bandwidth (%)	15.77	11.25
Through, $ S_{21} $ (dB)	-4.36	-3.17
Coupled, $ S_{31} $ (dB)	-4.18	-1
Return loss, $ S_{11} $ (dB)	-25.25	-28.8
Isolation, $ S_{41} $ (dB)	-32.48	-24.8
Amplitude imbalance, $ S_{31} - S_{21} $ (dB)	< 0.5	$\pm 7$
Phase difference, $\angle S_{31} - \angle S_{21}$ (deg)	$90 \pm 178$	$90 \pm 196$

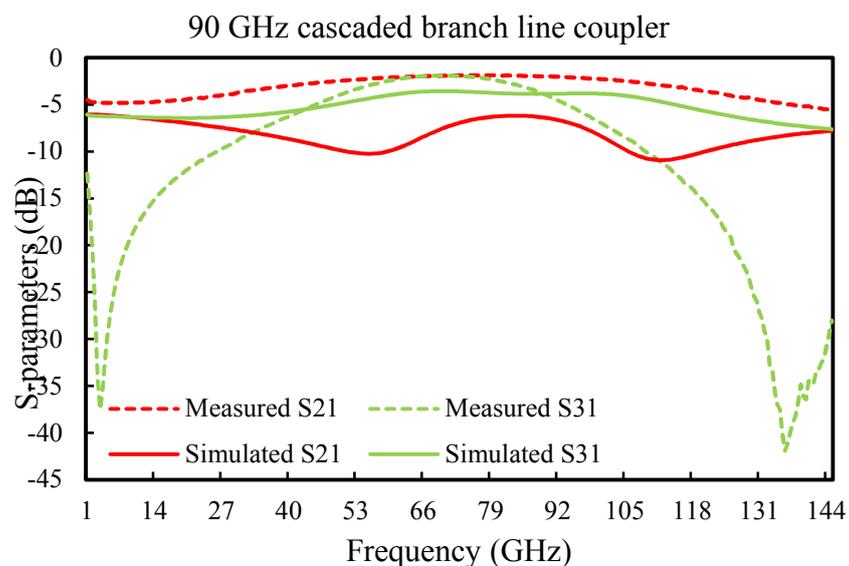
**Table 4.11:** Summarised measured and simulated S-parameters result of the 90 GHz branch line coupler.

#### 4.6.2 90 GHz Cascaded branch line coupler

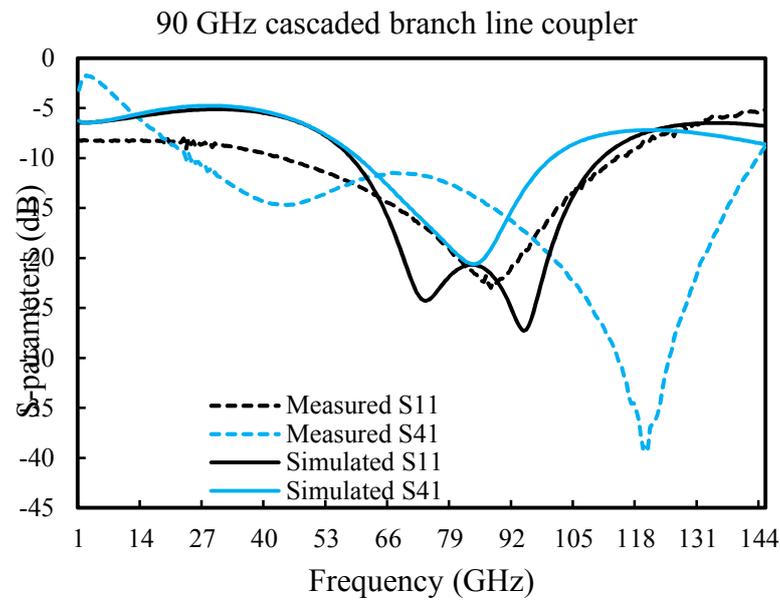
Optical images of fabricated cascaded branch line couplers are shown in the Fig. 4.32. The parameters used for fabrication were same as the simulated parameters detailed in Section 4.4.2, Page 164. The measured and simulated S-parameter results for the cascaded branch line coupler are plotted in Fig. 4.33 and Fig. 34. The coupling ( $|S_{31}|$ ) and through ( $|S_{21}|$ ) achieved were -1.85 dB and -1.88 dB respectively, with amplitude imbalance ( $|S_{31} - S_{21}|$ ) of  $\pm 1$  dB. The return loss ( $|S_{11}|$ ) and isolation loss ( $|S_{41}|$ ) of -22.96 dB and -17.48 dB was noted separately with 10 dB percentage bandwidth of 98.34 %.



**Fig. 4.32:** Optical images of fabricated cascaded branch line coupler.



**Fig. 4.33:** Measured and simulated  $S_{21}$  and  $S_{31}$  parameters results for the 90 GHz cascaded branch line coupler.



**Fig. 4.34:** Measured and simulated  $S_{11}$  and  $S_{41}$  parameters results for the 90 GHz cascaded branch line coupler.

Table 4.12 shows a summary of simulated and measured results for the 90 GHz cascaded branch line coupler. There was reasonable agreement between the simulated and measured results. The power at coupled port ( $|S_{21}|$ ) measured was -1.85 dB, while at the through port ( $|S_{31}|$ ) it was -1.88 dB. The higher power at both the ports might be due to the coupling issue between the arms, impedance of the quarter wavelength transmission line not achieving  $Z_0\sqrt{2}$  at resonant frequency. The fractional bandwidth demonstrated by the simulated result was higher than the measured results and higher than the measured 90 GHz branch line coupler and the measured phase difference was higher than simulated by  $135^\circ$ , as the device didn't achieve  $\lambda/4$  length at resonant frequency.

Couplers Parameters	Simulated	Measured
Frequency (GHz)	62-102.5	76.5-96.5
Bandwidth (%)	44.37	23.27
Coupled, $ S_{21} $ (dB)	-6.19	-1.85
Through, $ S_{31} $ (dB)	-3.82	-1.88
Return loss, $ S_{11} $ (dB)	-27.28	-22.96
Isolation, $ S_{41} $ (dB)	-22.56	-17.48
Amplitude imbalance, $ S_{31} - S_{21} $ (dB)	< 5	$\pm 1$
Phase difference, $\angle S_{31} - \angle S_{21}$ (deg)	$90 \pm 5$	$90 \pm 140$

**Table 4.12:** Summarised measured and simulated S-parameter results for the 90 GHz cascaded branch line coupler.

## 4.7 Conclusion

Four different hybrid junction couplers (branch line, cascaded branch line, rat race, curved rat race) and one power divider (Wilkinson) were designed and simulated at three frequencies (90, 300, 650 GHz) on GaN-on-LR Si using a shielding technique. Only the 90 GHz branch line and 90 GHz cascaded branch line coupler were measured, and the results reported here due to delays out with the author's control. Both measured circuits showed very good agreement with the simulated results, with respect to matching and isolation. However, power at the output ports seemed to have experienced coupling loss, which has resulted in an increase of power division at the output port. Bandwidth achieved by cascaded branch line was twice the single branch line coupler. Both simulated and measured results of these circuits show the viability of the shielding technique and SiO<sub>2</sub> as the dielectric material.

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## Study of Ohmic Contacts Formation on AlGaN/GaN layers on LR Silicon

### 5.1 Introduction

Active devices such as transistors play a major part in determining the performance of sensors and circuits. At terahertz frequencies, transistors with high unity-current-gain-cut-off ( $f_T$ ) and maximum oscillation ( $f_{max}$ ) frequencies are key factors to determine the speed and maximum frequency of circuit operation. To maximise the use of GaN materials at terahertz frequencies, ohmic contact resistance should be as low as possible. This chapter provides an overview of metal to semiconductor contact formation for AlGaN/ GaN HEMTs. The Transmission Line Model (TLM) for characterising ohmic contact resistance and Atomic Force Microscopy (AFM) for surface analysis will be described and discussed.

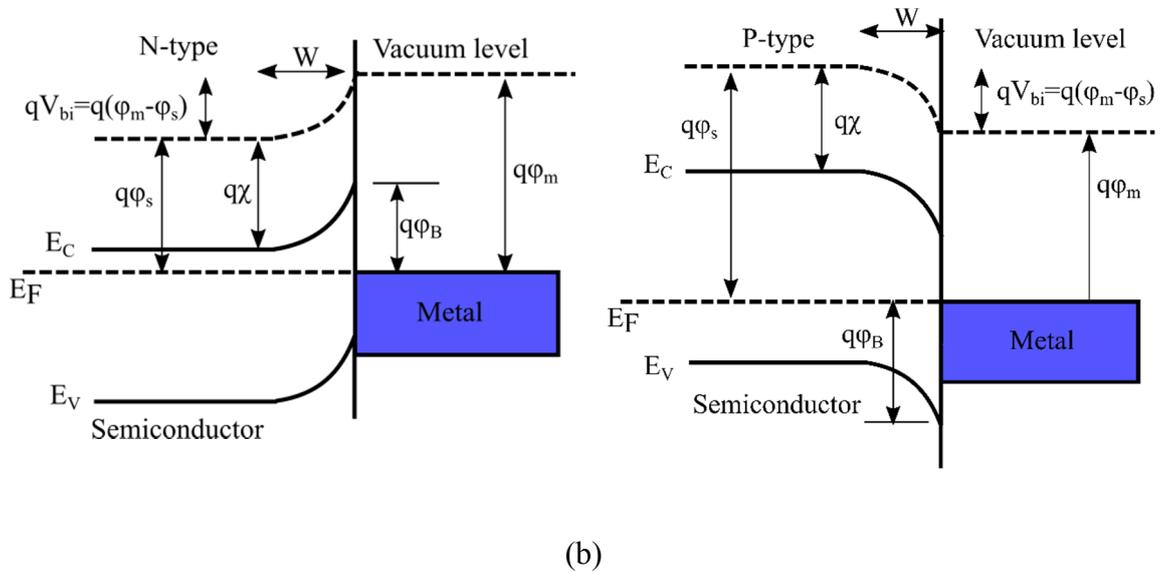
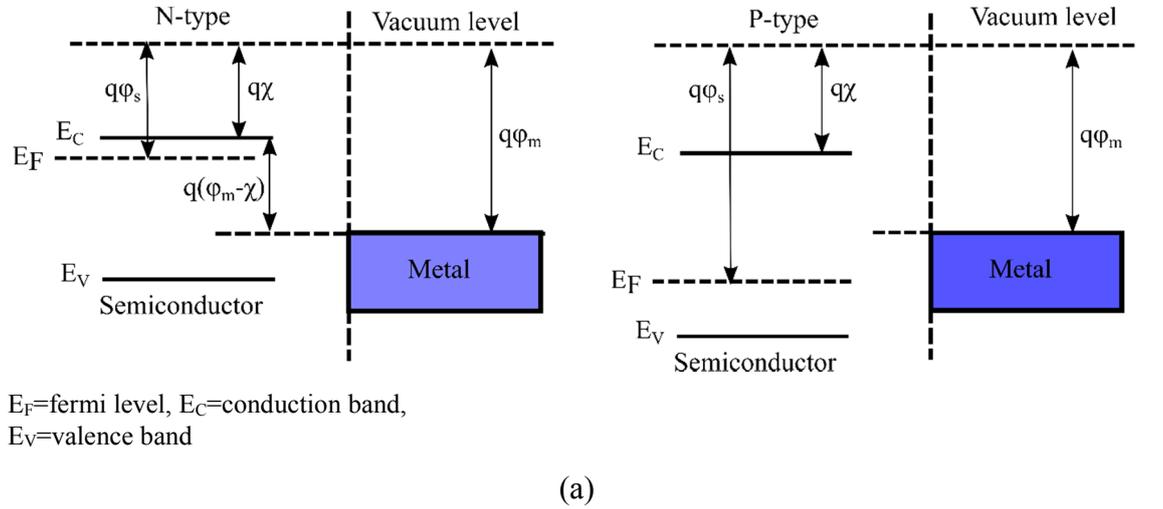
### 5.2 Metal-semiconductor contact

A metal-semiconductor contact can be described as Schottky or ohmic in nature, dependent upon the height of the Schottky barrier formed. A Schottky contact is a rectifying junction that conducts current only in the forward bias state. Whereas, an ohmic contact conducts current in both directions (forward and reverse bias). An ohmic contact follows Ohm's laws, where current is a linear function of the applied voltage. Whether the given junction is ohmic or Schottky, depends on the Schottky barrier height ( $\phi_B$ ) of the junction. The section below explains the physics of Schottky and ohmic contacts on both n- and p-type semiconductors.

Schottky barrier is formed when the metal is sputtered or evaporated onto a semiconductor surface. Fig. 5.1 shows the band bending in both n- and p-type semiconductors when a Schottky barrier is formed. Here  $\phi_B$  is the barrier height, defined as the potential difference between the Fermi level of the metal and the band edge where the majority carrier is present. For an n-type semiconductor, the barrier height is

$$\phi_{Bn} = \phi_m - \chi_s \quad (5.1)$$

Where  $q\phi_m$  is the metal work function,  $q\phi_s$  is the semiconductor work function and  $q\chi_s$  is the semiconductor electron affinity. In this case,  $q\phi_m > q\phi_s$  and electrons flow from semiconductor to the lower work function metal until thermal equilibrium is achieved [5.1].



**Fig. 5.1:** Ideal band diagram of metal-semiconductor: (a) before contact (b) after contact [5.2].

For a p-type semiconductor, the barrier height is the difference between valence band edge to the Fermi level in the metal and electron flows from the metal to semiconductor until equilibrium is obtained [5.1].

$$\phi_{Bp} = \frac{E_g}{q} + \chi - \phi_m \quad (5.2)$$

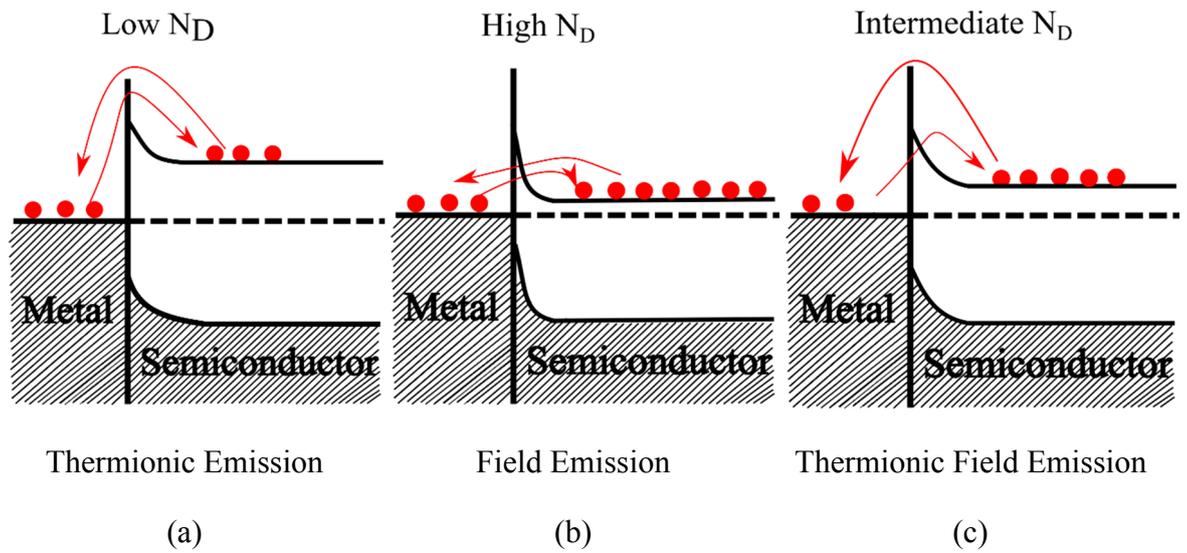
To form an ohmic contact at the metal-semiconductor interface, lower Schottky barrier height ( $\phi_B$ ) should be achieved, where there is no depletion region in the semiconductor. This is the basic requirement for any semiconductor devices for an electrical charge to be conducted between the active region of a transistor and the external circuitry.

Specific contact resistance is the figure-of-merit for ohmic contacts [5.2], and is defined as

$$\rho_c = \left( \frac{\partial J}{\partial V} \right)_{V=0}^{-1} \Omega \cdot \text{cm}^2 \quad (5.3)$$

Depending on the semiconductor doping level ( $N_D$ ) and the different thickness of the space charge region  $W$  (width of barrier) formed at the interface, there are three different conduction mechanisms (Fig. 5.2) [5.3]:

1. **Thermionic emission (TE)** - carriers have sufficient energy to overcome the barrier height. This mechanism typically dominates carrier transport in low doped semiconductor ( $N_D < 1 \times 10^{17} \text{ cm}^{-3}$ ) where the barrier width is larger.
2. **Field emission (FE)** - carrier passes through the barrier, based on the theory of quantum mechanical tunnelling. Tunnelling probability depends on both barrier height and barrier width ( $N_D > 1 \times 10^{19} \text{ cm}^{-3}$ ).
3. **Thermionic field emission (TFE)** - is the combination of both thermionic emission and field emission. If the barrier is narrow and height is small (or if they have sufficient energy), then both will occur ( $N_D$  between  $1 \times 10^{17} - 1 \times 10^{19} \text{ cm}^{-3}$ ).



**Fig. 5.2:** Schematics of different carrier transport mechanisms through metal/semiconductor barrier for different doping level  $N_D$  [5.3].

Thus, we can say that for a constant value of the Schottky barrier height ( $\phi_B$ ) and carrier concentration  $N_D$ , the temperature  $T$  defines the carrier transport mechanism through the metal/semiconductor interface. If thermal energy ( $kT$ ) is lower than characteristic energy  $E_{00}$  ( $kT \ll E_{00}$ ), the tunnelling by FE mechanism is predominant. If thermal energy is comparable with characteristic energy ( $kT \approx E_{00}$ ), TFE mechanism is predominant, and if thermal energy is much greater than characteristic energy thermionic emission becomes main for carrier transport ( $kT \gg E_{00}$ ). Considering all the above conditions, a narrower Schottky barrier height is needed to achieve lower contact resistance  $\rho_c$  [5.3].

## 5.3 Measurement techniques

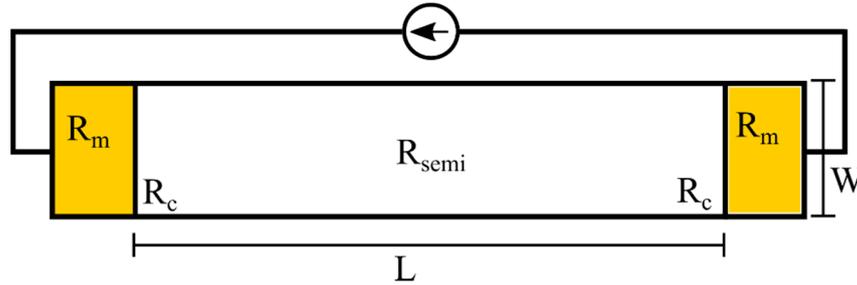
There are several methods to measure contact resistance ( $R_c$ ). In this work, the Transmission Line Method (TLM) is used to determine contact resistance and sheet resistance of the material. Further, four-point probe or the van der Pauw method are used to also determine sheet resistance.

### 5.3.1 Transmission line model

Transmission line model is the measure of several resistors of different lengths while retaining all other parameters as constant. Consider the simple resistor geometry shown in the Fig. 5.3. Two contacts are placed at the ends of the semiconductor bar with contact area  $A_c$ . The total measured resistance of all the components are:

$$R_T(\Omega) = 2R_m + 2R_c + R_{semi} \quad (5.4)$$

Where  $R_m$  is the resistance of the metal,  $R_c$  is the contact resistance associated with metal/semiconductor interface, and  $R_{semi}$  is the semiconductor resistance.



**Fig. 5.3:** Diagram of simple resistor using semiconductor and metal contacts.

Since the resistance of the interface is much higher than metal interface,  $R_m$  can be neglected from above equation, and the semiconductor resistance is given by

$$R_{semi}(\Omega) = R_S \frac{L}{W} \quad (5.5)$$

Where  $R_S$  is the sheet resistance of the semiconductor,  $W$  and  $L$  is the width and length of semiconductor respectively.

Therefore, the resistance in Equation (5.4) can be written as

$$R_T(\Omega) = \frac{R_S}{W} L + 2R_c \quad (5.6)$$

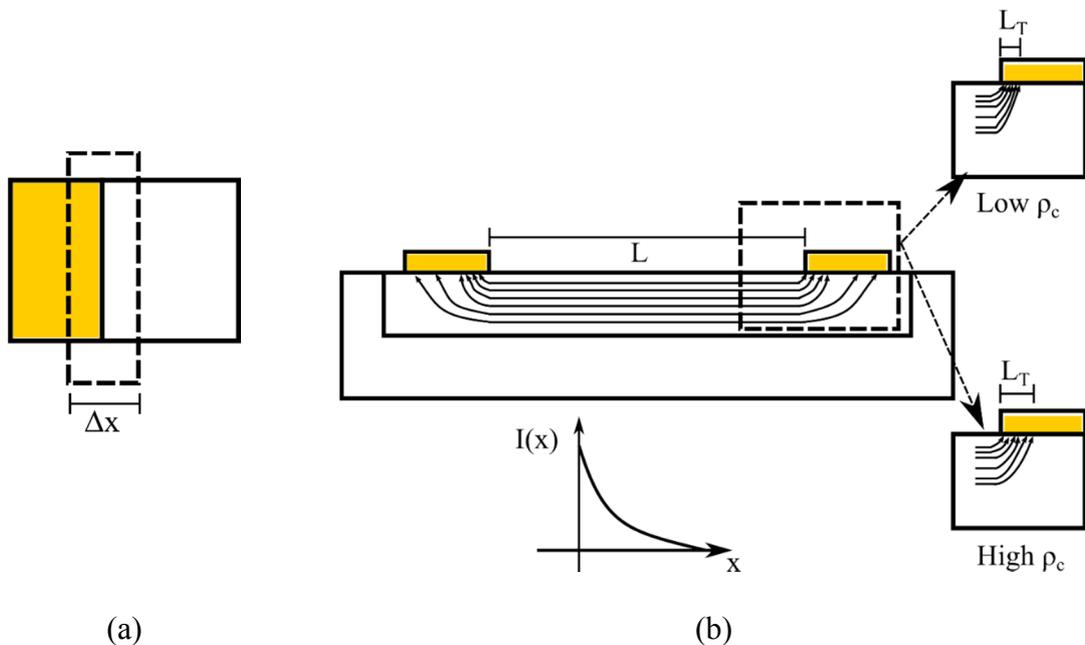
This equation shows a way to calculate contact resistance/total resistance at different lengths. The contact resistance is the total resistance of the metal/semiconductor junction, and hence it depends on the size of the contact, specific contact resistance  $\rho_c$  is used more as a physical parameter for describing the performance of the ohmic contact. Specific contact resistance doesn't depend on the size of the contact and is calculated as follows.

Consider small area around the contact  $\Delta x$ , as shown in Fig. 5.4 (a) [5.4].

$$R_C = \rho' \frac{\Delta x}{A_C} \quad (5.7)$$

Where  $A_C$  is the area of contact.

$$\rho_c = \lim_{\Delta x \rightarrow 0} (\rho' \Delta x) = R_C A_C \quad \Omega \cdot \text{cm}^2 \quad (5.8)$$



**Fig. 5.4:** (a) Contact area around metal-semiconductor interface (b) current crowding inside the semiconductor.

The calculation of contact area  $A_C$  ( $W \times L$ ) holds well if the current flowing into the contact is uniform (Fig. 5.4 (b)) but only the current flow in semiconductor is uniform. As a result, instead of physical length, characteristic length known as transfer length ( $L_T$ ) is used ( $A_C = W \times L_T$ ). As we can see from Fig. 5.4 (b) the current flowing in or out of the contact is higher near the semiconductor side and it drops at the far edge. This is known as current crowding and it exponentially decays with transfer length.

$$L_T = \sqrt{\frac{\rho_c}{R_S}} \quad (5.9)$$

Transfer length is the average distance that an electron (hole) travels in the semiconductor below the contact before it enters the contact pad. So effective area of contact is  $L_T W$ .

From Equation (5.8) and Equation (5.9), contact resistance is:

$$R_C = \frac{\rho_c}{L_T W} = \frac{R_S L_T}{W} \quad (5.10)$$

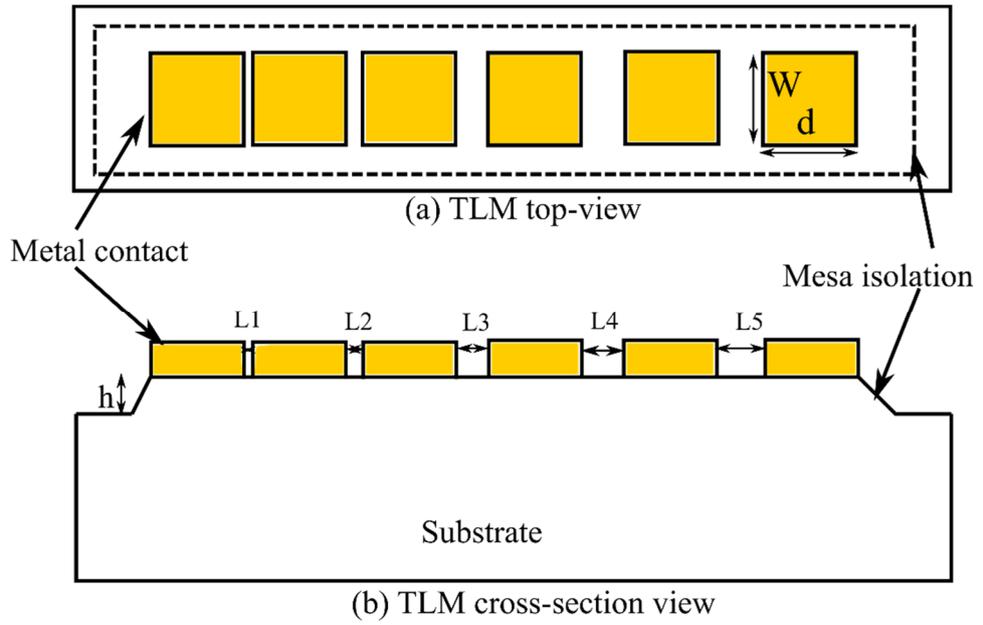
Applying Equation (5.5) and Equation (5.10) into Equation (5.4):

$$R_T = R_{semi} + 2R_C \quad (5.11)$$

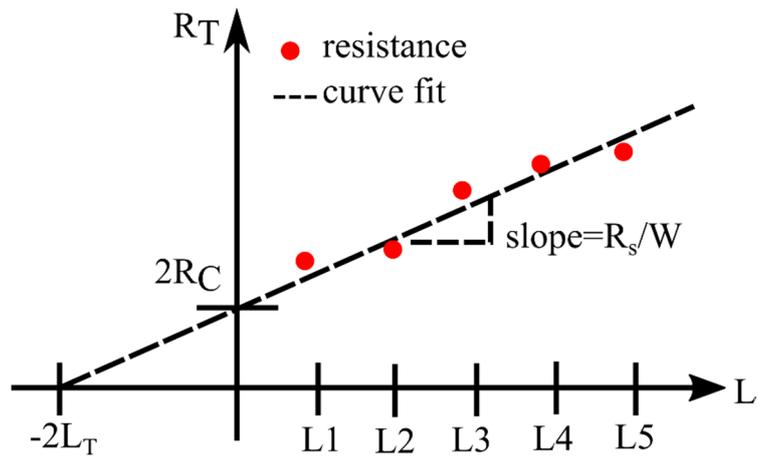
$$= R_S \frac{L}{W} + 2 \frac{R_S L_T}{W} \quad (5.12)$$

$$R_T = \frac{R_S}{W} (L + 2L_T) \quad (5.13)$$

From single resistor geometry, TLM test structures can be deduced Fig. 5.5 shows the schematic diagram of the array of rectangular ohmic contact pads with width  $W$  and length  $d$ , spacing between them  $L$ , and mesa height  $h$ . Measurements of contact pads are carried out by applying voltage across each gap and measuring the current. Fig. 5.6 shows the plot of total resistance of each gap. For each gap, the total resistance is of the contacts plus gap. At the y-intercept where the gap is equal to zero, the resistance is  $2R_C$ . The slope of the graph gives the sheet resistance of the semiconductor. The Graph can also give transfer length by extrapolating back to the horizontal axis, where the intercept =  $-2L_T$  [5.5] [5.6].



**Fig. 5.5:** Schematic of TLM test structure.



**Fig. 5.6:** Plot of  $R_T$  vs resistor length of TLMs.

### 5.3.2 Van der Pauw method

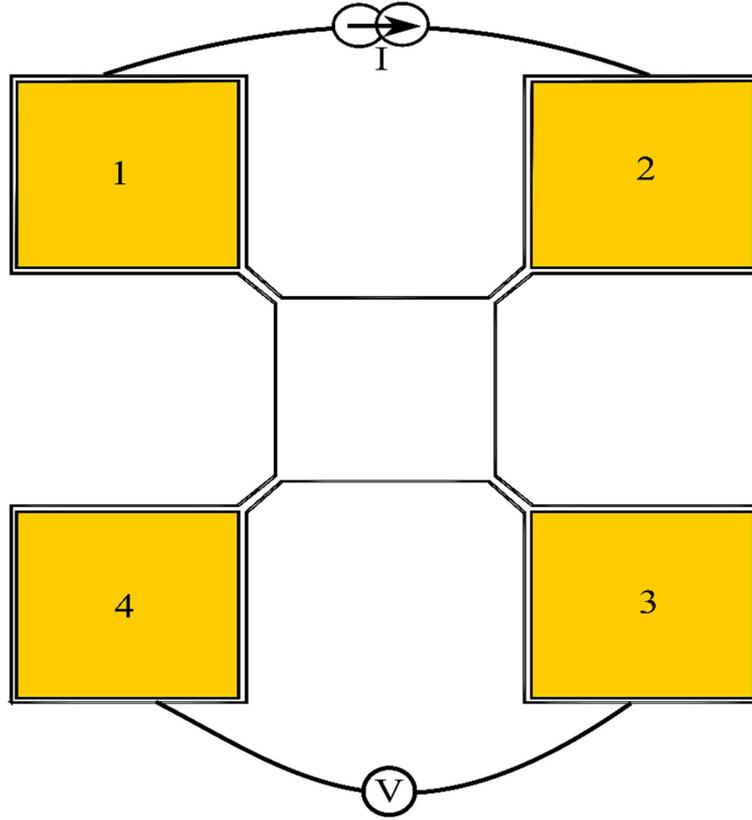
The van der Pauw method (VDP) is a technique used to determine the resistivity and Hall coefficient of a semiconductor material of arbitrary shape. This method uses four contacts placed around the periphery of the conducting region to measure voltage by applying a current. Using this structure, four properties of a material are calculated: resistivity, doping type (n- or p-type material), sheet carrier density and mobility of majority carrier. Below section details the procedure to calculate these parameters [5.7] [5.8] [5.9] [5.10].

Fig. 5.7 shows the VDP structure used in this experiment. Here, contact pads are numbered 1-4. The current  $I_{12}$  is a positive DC current applied to contact 1 and measured from contact 2. The voltage  $V_{43}$  is a DC voltage measured between contacts 4 and 3 with no external magnetic field applied. The current is applied along one edge of the sample  $I_{12}$  and voltage is measured across the opposite edge  $V_{43}$ . According to Ohms law, the resistance is calculated as below

$$R_{12,43} = \frac{V_4 - V_3}{I_{12}} \quad (5.14)$$

Likewise, another resistance is calculated by measuring along horizontal edge,  $R_{23,14}$ . The average resistivity of any sample is given by

$$\rho = R_S \cdot t \quad (5.15)$$



**Fig. 5.7:** VDP structure.

From which actual sheet resistance is calculated using the above resistances by the van der Pauw formula [5.7]

$$e^{-\pi t R_{12,43}/R_S} + e^{-\pi t R_{23,14}/R_S} = 1 \quad (5.16)$$

To obtain value for sheet resistances per unit area, the measurement is taken on all the sides of the structure and it should obey reciprocity theorem. Therefore, measurement taken along  $R_{12,43}$  should be same as  $R_{43,12}$ . Further, to improve the accuracy, the reverse polarity measurement is also done. Where, the measurements are repeated after switching polarities of both current source and voltage source. Now, the VDP formula in Equation (5.16) can be changed into

$$e^{-\pi t R_{vertical}/R_S} + e^{-\pi t R_{horizontal}/R_S} = 1 \quad (5.17)$$

Where,

$$R_{vertical} = \frac{R_{12,34} + R_{43,12} + R_{21,34} + R_{34,21}}{4} \quad (5.18)$$

$$R_{horizontal} = \frac{R_{14,23} + R_{23,14} + R_{41,32} + R_{32,41}}{4} \quad (5.19)$$

The error associated with measurement of  $R_{\text{vertical}}$  and  $R_{\text{horizontal}}$  should be within 3-5%. Otherwise, it suggests sample non-homogeneity, anisotropy, problems in sample's contacts or instruments.

If samples and the position of contacts are symmetrical, then  $R_{\text{vertical}} = R_{\text{horizontal}}$  and sheet resistance can be computed as

$$R_S = \frac{-\pi t R_{\text{vertical}}}{\ln(2)} \quad (5.20)$$

If the symmetry is not perfect, and  $R_{\text{vertical}} \sim R_{\text{horizontal}}$ , the sheet resistance is calculated as the average between the two resistances in the above equation. If they are totally different, the sheet resistance calculation is done using Equation (5.17). As result, VDP structures are simple squares and circles.

Hall measurement is based on the principle of Hall Effect. When a charged particle is placed in a magnetic field, it experiences a Lorentz force proportional to the strength of the magnetic field and the velocity at which carriers are moving through it [5.11] [5.12] [5.1].

$$F_y = qv_{D,x}B_z \quad (5.21)$$

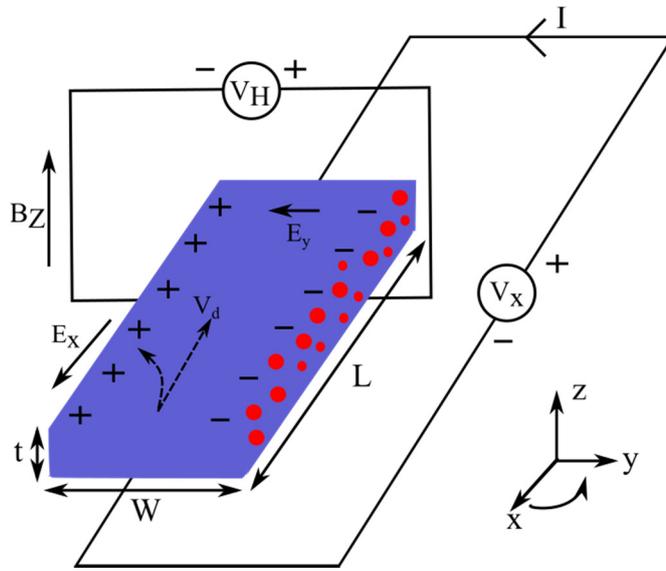
Where,  $q$  is the charge on particles (C),  $v$  the velocity at which carriers are travelling (cm/s), and  $B$  the strength of magnetic field (Wb/cm<sup>2</sup>). The velocity at which carriers travel when a current is applied to a piece of semiconductor material is,

$$v = \frac{I}{nAq} \quad (5.22)$$

In this,  $n$  is the electron density,  $A$  is the cross-sectional area of the material and  $q$  the elementary charge ( $1.602 \times 10^{-19}$  coulombs).

When an external magnetic field is applied perpendicular to the direction of current flow (Fig. 5.8), the resulting Lorentz force will cause the electrons to accumulate at one end of the sample and holes on the other end until the balance is reached. These accumulated electrons will create potential difference across the sample, known as the Hall voltage  $V_H$ . As the current flows along the material constantly, the force on the electrons due to electric field balances the Lorentz force. The force on an electron due to electric field  $\epsilon$  is  $q\epsilon$ , combining Equation (5.21) & (5.22), strength of electric field is

$$\varepsilon = \frac{IB}{qnA} \quad (5.23)$$



**Fig. 5.8:** Hall effect measurement of electrons [5.13].

The magnitude of Hall voltage is simply the strength of the electric field multiplied by the width of the material,

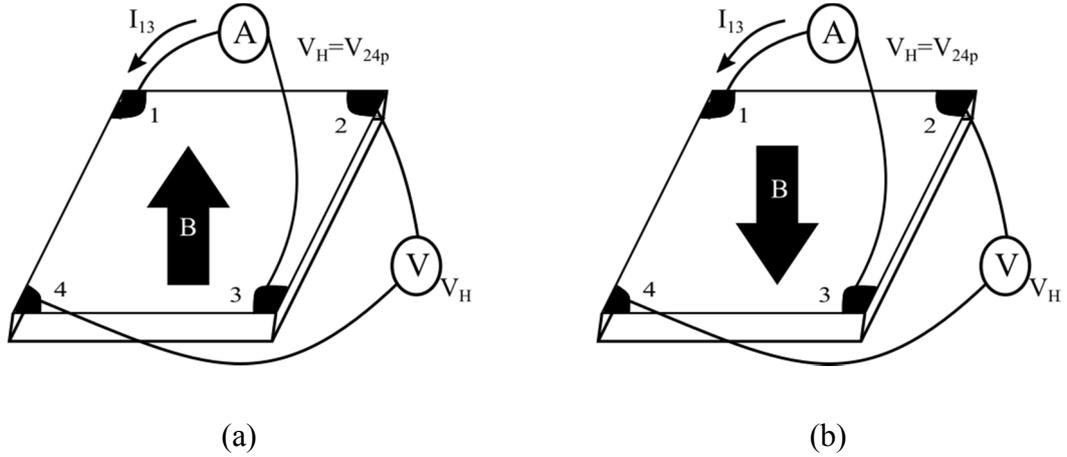
$$V_H = w\varepsilon = \frac{wIB}{qnA} = \frac{IB}{qnt} \quad (5.24)$$

Where  $t$  is the thickness of the sample. Since the sheet density  $n_s$  is defined as the density of electrons multiplied by the thickness of the material, Hall voltage in terms of sheet density is,

$$V_H = \frac{IB}{qn_s} \quad (5.25)$$

Fig. 5.9 shows the method to measure VDP structures to determine Hall voltage. Two sets of measurements are done- one with a magnetic field in the positive  $Z$ -direction, and one with the negative  $Z$ -direction with same magnitude of injected current and same magnitude of magnetic field in both the cases, to improve accuracy of the measurement. Unlike resistivity measurement, current is applied diagonally to contacts  $I_{24}$  and voltage  $V_{13,P}$  is recorded, same is repeated with  $I_{13}$  and  $V_{24}$ . Similar measurements are done with reversing the current direction as before to check the accuracy. Further, negative magnetic field is applied instead of positive one and the procedure is repeated  $I_{24}$  and  $V_{13,N}$ . Thus,

$$\begin{aligned}
V_{13} &= V_{13,P} - V_{13,N} \\
V_{24} &= V_{24,P} - V_{24,N} \\
V_{31} &= V_{31,P} - V_{31,N} \\
V_{42} &= V_{42,P} - V_{42,N}
\end{aligned}
\tag{5.26}$$



**Fig. 5.9:** Hall measurement using VDP with (a) positive magnetic field (b) negative magnetic field.

The overall Hall Voltage then is

$$V_H = \frac{V_{13} + V_{24} + V_{31} + V_{42}}{8}
\tag{5.27}$$

The polarity of the Hall voltage determines which type of material it is. If its positive voltage, the material is P-type, and if it's negative voltage, the material is N-type. After knowing Hall voltage, by rearranging Equation (5.25), we can find sheet carrier density

$$n_s = \frac{IB}{q|V_H|} \text{ cm}^{-2}
\tag{5.28}$$

From the sheet density, mobility of charge carrier can be further calculated. The resistivity of a semiconductor material can be calculated using

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)}
\tag{5.29}$$

Where n and p are the concentration of electron and hole respectively in the material, and  $\mu_n$  and  $\mu_p$  are the mobility of the electrons and holes respectively. If the material is doped with either holes or electron, the other can be neglected in the equation

$$\rho = \frac{1}{qn_m\mu_m} \quad (5.30)$$

Where  $n_m$  and  $\mu_m$  are the doping level and mobility of majority charge carriers in a material respectively. The bulk carrier density can be determined if the conducting layer thickness  $t$  is known for a sample:

$$\begin{aligned} n_m &= n_s \times t \\ R_S &= \rho_s/t \end{aligned} \quad (5.31)$$

Replacing above in Equation (5.30), we can calculate sheet resistance  $R_S$

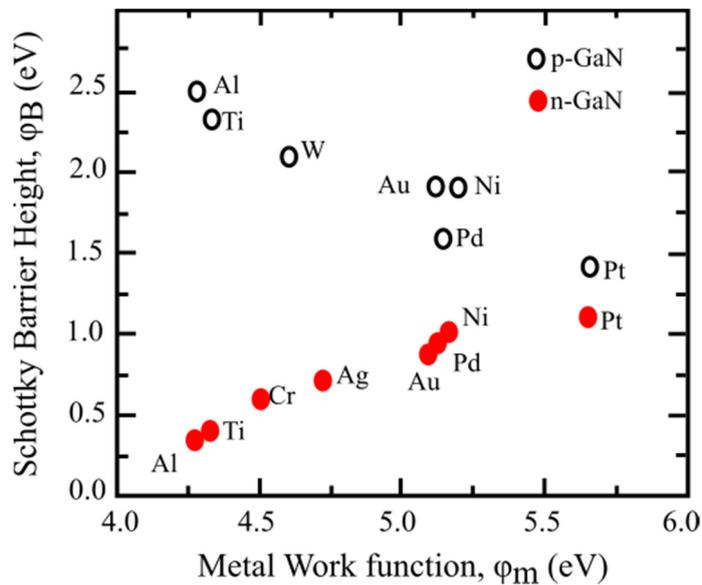
$$R_S(\Omega\Box) = \frac{1}{qn_s\mu_m} \quad (5.32)$$

Rearranging this the mobility of majority carriers in terms of sheet density and sheet resistivity is given as

$$\mu_m(cm^2/V.s) = \frac{1}{qn_sR_S} \quad (5.33)$$

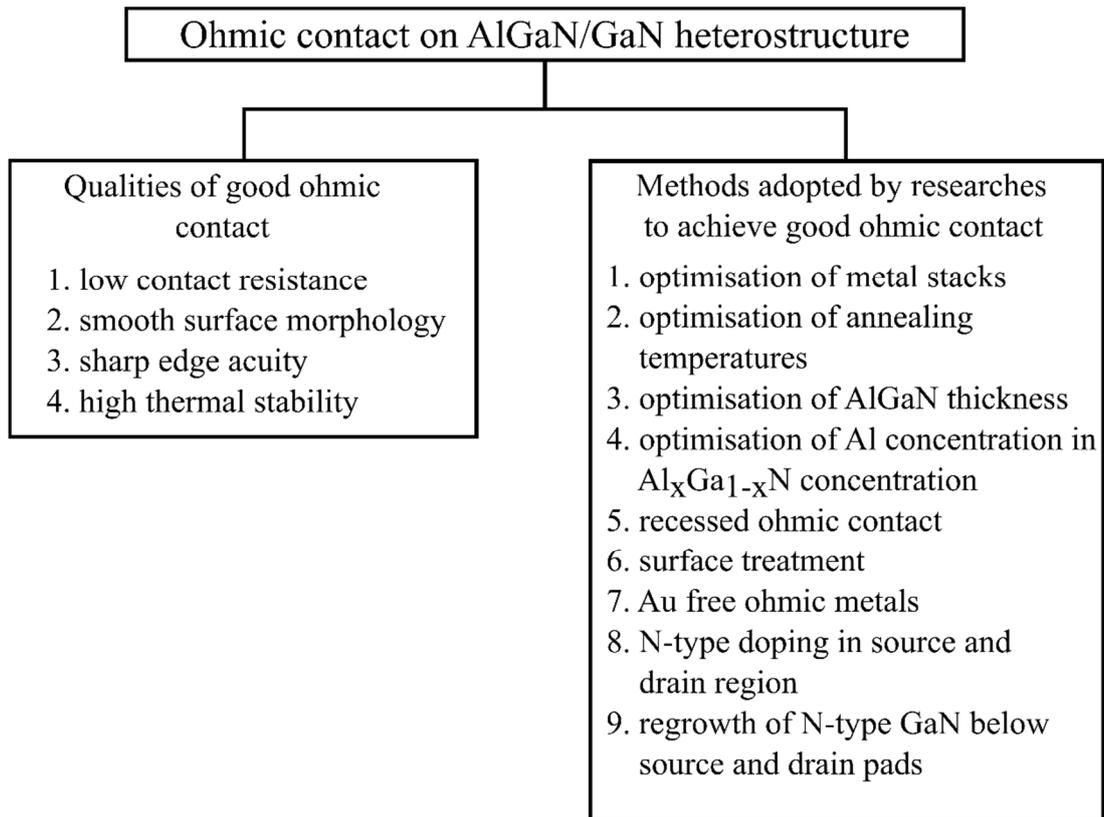
## 5.4 Review of ohmic contact on AlGaN/GaN HEMT

The AlGaN/GaN heterostructure plays a significant role in GaN-materials and device technology, especially for the fabrication of High Electron Mobility Transistors (HEMT). It generates a two-dimensional electron gas (2DEG) at the interface by the piezoelectric polarization gradient, which provides a low channel resistance compared to Si and SiC devices [5.14]. For a standard HEMTs, the current flows between the source and drain in the 2DEG channel and Schottky metal gate modulates this flow. Fig. 5.10 shows the values of Schottky barrier height as a function of metal work function for different metals, which could be used for the formation of HEMTs devices [5.3].



**Fig. 5.10:** Review of literature of Schottky barrier height  $\phi_B$  values as a function of the metal work function  $\phi_m$  for different metals on both n-type and p-type GaN [5.3].

Initially, for the development of source-drain ohmic contacts in AlGaN HEMTs, metal stacks used for n-type GaN were studied. However, the AlGaN barrier has larger bandgap (depending on the Al concentration of layer) than n-GaN, making the ohmic contact essentially more difficult. AlGaN/GaN heterostructure are made from undoped layers for limiting scattering phenomena and enhancing mobility of the 2DEG. The current conduction in AlGaN is through the high sheet carrier density of the 2DEG located at the AlGaN/GaN interface [5.3]. Hence, more investigation was needed to optimise the ohmic contact on AlGaN/GaN heterostructure than simple n-type GaN material.



**Fig. 5.11:** Merits of good ohmic contact and techniques researchers have adopted to solve it.

Fig. 5.11 shows the potentials required to achieve a good ohmic contact on AlGaIn/GaN and methods researchers have adopted to achieve these. Most studies used Ti/Al/X/Au (X=Ni, Ti, Ta, Mo, Pt ...) metal stack combination which was proposed by Mohammed *et al.* for n-GaN to achieve lower ohmic contact resistances. Here, each metal stack has their own role for optimising the ohmic contact [5.15] [5.16] [5.17]:

**Titanium:** Reacts with N in AlGaIn to form TiN, lowering SBH (Schottky barrier height). It creates N vacancies which helps for tunnelling of electrons by creating a highly n-doped layer underneath the ohmics. TiN formed here has a low work function < 4 eV.

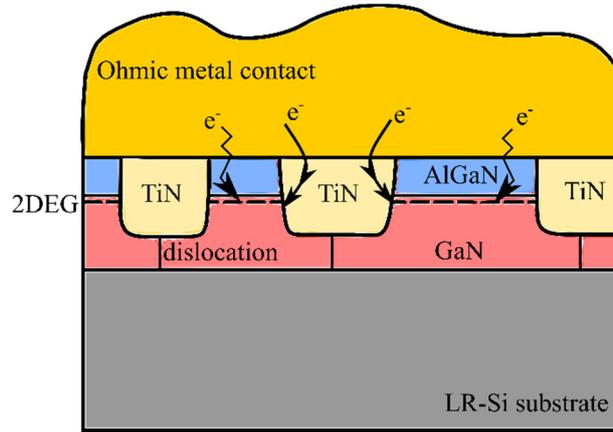
**Aluminium:** Reacts with Ti to form Ti-Al phase (Al<sub>3</sub>Ti layer) which prevents Ti from oxidation. Further it reacts with AlGaIn to form AlN and N vacancies underneath the ohmics enabling electrons tunnelling easily to the 2DEG channel.

**Pt, Ni, Ti, or Mo:** These metal layers prevent the in-diffusion of Au and out-diffusion of Al, thus preventing Al and Au metal mixing with each other. It's responsible for formation of good contact resistance as well as good surface morphology of the ohmics after being annealed at higher temperatures.

**Gold:** This metal layer prevents oxidation of Ti and Al metals at higher annealing temperatures and to improve ohmic contacts conductivity (by reducing sheet resistance).

#### 5.4.1 Carrier transport mechanisms in AlGaIn/GaN HEMTs

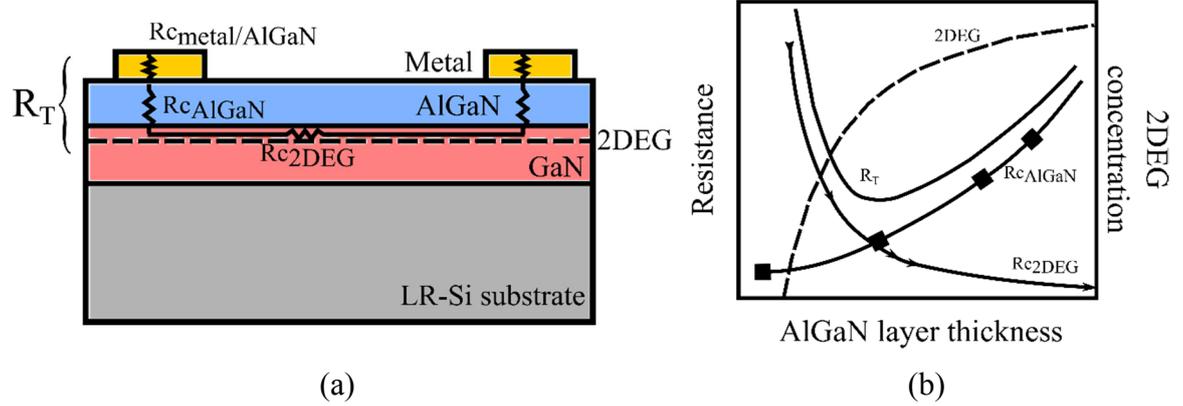
For an AlGaIn/GaN heterostructure, two mechanisms were initially reported based on the displacement reaction between Ti and AlGaIn, producing tunnelling and low-barrier Schottky contacts. The first mechanism occurs through out-diffusion of N, as N-vacancies are created in the AlGaIn layer they act as an n-type dopant and thus create a highly doped region at the surface of semiconductor which leads to increased band bending. This reduces the depletion region width and facilitates carrier transport via tunnelling [5.15]. The low Schottky barrier height requires formation of intermediate band-gap compounds and nitride compounds. Since TiN has higher electrical conductivity and lower work function (3.74 eV) than Ti (4.33 eV), this leads to a reduced barrier height and thus a higher possibility of carriers transport [5.18]. Fay *et al.* observed TiN inclusions at the dislocations of an AlGaIn/GaN interface by using Ti/Al/Ni/Au contacts annealed at 950<sup>o</sup> C. This led to the discovery of another mechanism called direct electron path or “spike” contact [5.19]. Further research by Wang *et al.* demonstrated that after high temperature annealing of a Ti/Al/Mo/Au stack, they observed the formation of TiN in two ways. The first observation was of TiN islands, which formed along threading dislocations with incorporation of Au, another at the metal/AlGaIn interface. They also claim that these TiN protrusions were not observed in Ta/Al/Mo/Au stacks [5.20]. Fig. 5.12 shows the schematic of the spike mechanism for carrier injection. In this, there are two ways for electrons to be transported, one from the 2DEG to metal contact through AlGaIn, another through TiN protrusions surrounded by Au shell. Here, contact properties are determined by the nature of 2DEG channel and TiN protrusions [5.20].



**Fig. 5.12:** Schematic of the spike mechanism for carrier injection [5.20].

#### 5.4.2 Effect of AlGaN thickness on ohmic contact

In this section, we will discuss the effect of AlGaN thickness on the contact resistance and 2DEG concentration of a device. Fig. 5.13 (a) shows a model of contact resistance on AlGaN/GaN HEMT structure. Since current paths need to be formed through AlGaN layer, it can be seen that there are three resistance involved in transport of current through the structure. These three components are the resistance at the metal/AlGaN interface ( $R_{c_{\text{Metal/AlGaN}}}$ ), the resistance to current flow through the AlGaN layer ( $R_{c_{\text{AlGaN}}}$ ), and resistance to the connection with the 2DEG ( $R_{c_{\text{2DEG}}}$ )-sheet resistance. Fig. 5.13 (b) shows the dependency of contact resistance and the 2DEG concentration on the AlGaN layer thickness. For thinner AlGaN layers, there is a depletion of the 2DEG concentration, induced by the large piezoelectric polarization in the AlGaN layer. These properties lead to trade-off involving AlGaN layer thickness and contact resistance. Thinner AlGaN layer reduces AlGaN resistance, 2DEG concentration and increases 2DEG resistance. For thicker layers,  $R_{c_{\text{AlGaN}}}$  resistance increases while 2DEG contact resistance is kept low. As a result, overall resistance ( $R_T$ ) will have to be lower. Since  $R_{c_{\text{AlGaN}}}$  and  $R_{c_{\text{2DEG}}}$  have opposite dependence on AlGaN thickness, which makes it tricky to reduce the overall resistance [5.21] [5.22].



**Fig. 5.13:** (a) model of contact resistance on AlGaN/GaN heterostructure (b) dependency of contact resistance and 2DEG concentration on AlGaN thickness [5.21].

### 5.4.3 Literature

#### Standard ohmic method

Table 5.1 shows a review of metals commonly used for optimising the ohmic contact on AlGaN/GaN heterostructure. The typical values of the contact resistance from the table are in the range of 0.1 to 4  $\Omega$ .mm for annealing temperatures of 400<sup>0</sup> to 900<sup>0</sup> C. Initially, Ti/Al/X/Au metal stack, where X being metals like Ni, Mo, Ti etc., was commonly used as ohmic metal for AlGaN/GaN heterostructure. Kong *et al.* [5.23] have claimed the importance of Ti/Al ratio in the metal structure. They have changed the ratio of Ti to Al in Ti/Al/Ni/Au with low (20/180 nm) and suitable (20/120 nm) relative thickness and fixed Ni/Au thickness to be 55/45 nm. Ti/Al of thickness 20/180 nm (sample A) showed non-linear response and contact resistance of 3.2  $\Omega$ .mm with rough surface. In addition, Ti/Al of thickness 20/120 nm (sample B) demonstrated contact resistance of 0.239  $\Omega$ .mm and very smooth contact surface. Further, research using STEM HAADF and EDX showed sample A conduction using electron tunnelling and sample B conduction using both electron tunnelling and spike mechanism, which showed the influence of Ti/Al relative thickness on the different ohmic formation mechanism. Maeta *et al.* and Wang *et al.* have studied the dependence of contact resistance on various annealing temperatures (400<sup>0</sup> C to 950<sup>0</sup> C) using Ti/Al/Ni/Au and Ti/Al/Mo/Au metal and have achieved lower contact resistance at higher temperatures (850<sup>0</sup> C to 900<sup>0</sup> C) with better surface morphology using Mo as diffusion layer than Ni [5.24] [5.15]. Another researcher, Feng *et al.* demonstrated the advantage of using multi-step annealing, however it is not clear how much the contact resistance was reduced [5.25]. Further, some researchers have changed the metal stack from norm (Ti/Al/X/Au) to achieve low contact resistance, smooth surface morphology, and edge acuity [5.17] [5.25-5.32]. One of the interesting suggestions to vary from norm was the use of Si in the metal stack.

Mohammed *et al.*, compared Ti/Al/Mo/Au with Ti/Si/Al/Si/Mo/Au, and achieved the lowest ohmic contact through tunnelling mechanism on undoped AlGaIn/GaN (0.12  $\Omega$ .mm) to date [5.16]. Since smooth surface morphology is necessary key for improving reliability and reproducibility of the AlGaIn/GaN HEMTs as it affects the process yield of the devices. Many researchers investigated to improve the surface morphology of the ohmic contact. Gong *et al.*, claimed that probable reason for the roughness on Ti/Al/Ni/Au metal scheme was due to non-uniform precipitation of Al-Ni in the Al-Au matrix and ratio of Ti/Al and Ni/Au is important factor in this [5.26]. Au-free metal schemes like Ti/Al/Cr/Mo/Au, Ti/Al/Ti/Ni/Au or Al-free metallisation or Ti-based contacts containing Mo has been proposed to solve this issue [5.27]. Based on the literature reported, there is a need for more research to determine the mechanism occurring under varied anneal conditions and the influence of dislocations and epitaxial material on the recognition of Ti/Al relative thickness or different metal stacks thickness.

<b>Metal layers (nm)</b>	<b>d<sub>AlGaIn</sub> (nm)</b>	<b>X<sub>Al</sub> (%)</b>	<b>Annealing conditions</b>	<b>R<sub>c</sub> (<math>\Omega</math>.mm)</b>	<b><math>\rho_c</math> <math>\Omega</math>.cm<sup>2</sup></b>	<b>Ref.</b>
Ti/Al/Ni/Au (15/60/35/50 nm)	25 nm	25 %	900 °C for 30s in N <sub>2</sub>	0.44	----	[5.24]
Ti/Al/Mo/Au (15/60/35/50 nm)	25 nm	25 %	850 °C for 30s in N <sub>2</sub>	0.28	----	[5.24]
Ti/Al/Ni/Au (20/160/50/100 nm)	25 nm	25 %	900 °C for 30s in N <sub>2</sub>	----	----	[5.26]
Ti/Al/Mo/Au (15/60/35/50 nm)	25 nm (n-type)	20 %	800 °C for 30s in N <sub>2</sub>	0.38	3×10 <sup>-6</sup>	[5.28]
Mo/Al/Mo/Au (15/60/35/50 nm)	25 nm (n-type)	20 %	650 to 800 °C for 30s in N <sub>2</sub>	0.22	9×10 <sup>-7</sup>	[5.28]
V/Al/Mo/Au (15/60/35/50 nm)	25 nm (n-type)	20 %	700 °C for 30s in N <sub>2</sub>	0.35	2.7×10 <sup>-6</sup>	[5.28]
Ti/Al	27 nm	25 %	500 °C	1.75	4.7×10 <sup>-5</sup>	[5.29]
Ti/Al/Ni/Au	27 nm	25 %	700 °C	0.49	6.5×10 <sup>-6</sup>	[5.29]
Ta/Ti/Al/Ni/Au (10/30/120/40/50 nm)	27 nm	25 %	700 °C for 1 min	0.21	7.5×10 <sup>-7</sup>	[5.29]
Ti/Al/Ti/Au/WSiN <sub>x</sub> (10/50/20/30/140 nm)	----	----	830 <sup>0</sup> C for 15s	0.51	----	[5.17]
Ti/Al/Mo/Au (10/50/20/30 nm)	----	----	830 <sup>0</sup> C for 15s	0.429	----	[5.17]
Ti/Al/Ti/Au (10/50/20/30 nm)	----	----	830 <sup>0</sup> C for 15s	0.502	----	[5.17]
Ti/Al/Ni/Au (10/50/20/30 nm)	----	----	830 <sup>0</sup> C for 15s	0.371	----	[5.17]
Ti/Al/Pt/Au (10/50/20/30 nm)	----	----	830 <sup>0</sup> C for 15s	0.41	----	[5.17]

<b>Metal layers (nm)</b>	<b>d<sub>AlGaN</sub> (nm)</b>	<b>X<sub>Al</sub> (%)</b>	<b>Annealing conditions</b>	<b>R<sub>c</sub> (Ω.mm)</b>	<b>ρ<sub>c</sub> Ω.cm<sup>2</sup></b>	<b>Ref.</b>
Ti/Al/Ni/Au	21 nm	28 %	750 °C for 30s in N <sub>2</sub>	0.2	----	[5.30]
Ti/Al/Ni/Au (20/90/55/45 nm)	25 nm (Si-doped)	30 %	400 °C-3min 700 °C-20 s 830 °C-30 s	----	----	[5.25]
Ti/Al/Ni/Au (20/120/55/45 nm)	25 nm (Si-doped)	30 %	400 °C-3min 700 °C-20 s 830 °C-30 s	----	4-3×10 <sup>-6</sup>	[5.25]
Ti/Al/Ni/Au (20/150/55/45 nm)	25 nm (Si-doped)	30%	400 °C-3min 700 °C-20 s 830 °C-30 s	----	----	[5.25]
Ti/Al/Ni/Au (20/180/55/45 nm)	22 nm	21.5 %	870 °C for 50s in N <sub>2</sub>	3.2	2.13×10 <sup>-4</sup>	[5.23]
Ti/Al/Ni/Au (20/120/55/45 nm)	22 nm	21.5 %	870 °C for 50s in N <sub>2</sub>	0.239	9.7×10 <sup>-7</sup>	[5.23]
Ti/Al/Mo/Au (15/60/35/50 nm)	20 nm (1 nm AlN)	28 %	850 °C for 30s	0.41	4.78×10 <sup>-6</sup>	[5.31]
Ti/Si/Al/Si/Mo/Au (15/15/60/15/35/50 nm)	20 nm (1 nm AlN)	28 %	850 °C for 30s	0.12	3.87×10 <sup>-7</sup>	[5.31]
Ti/Si/Al/Si/Mo/Au (15/30/60/30/35/50 nm)	20 nm (1 nm AlN)	28 %	900 °C for 30s	0.56	7.83×10 <sup>-6</sup>	[5.31]
Ti/Al/Ni/Au (20/120/40/50 nm)	20 nm	25 %	850 °C for 30s	----	6.4×10 <sup>-6</sup>	[5.32]
V- Ti/Al/Ni/Au (10/20/120/40/50 nm)	20 nm	25 %	850 °C for 30s	----	2.3×10 <sup>-6</sup>	[5.32]
Ti/Al/Mo/Au (15/60/35/50 nm)	21 nm (n-type)	28 %	850 °C for 30s in N <sub>2</sub>	0.176	2.96×10 <sup>-7</sup>	[5.15]
Ti/Al/Ni/Au (12/200/40/100 nm)	30 nm (Al <sub>2</sub> O <sub>3</sub> )	27 %	900 °C for 30s in N <sub>2</sub>	0.17	7.7×10 <sup>-8</sup>	[5.33]
Ti/Al/Ni/Au (12/200/40/100 nm)	26 nm (Si and SiC)	27%	900 °C for 30s in N <sub>2</sub>	No contacts		[5.33]

**Table 5.1:** Review of standard ohmic contacts on AlGaIn/GaN heterostructure.

## Recessed ohmic technique

A method to establish direct contact with the 2DEG channel has been explored by several groups. This technique is known as pre-ohmic recess or recessed ohmic contact, where the substrate is etched down to expose the 2DEG channel. The main advantage of a recessed ohmic contact is the reduction in required annealing temperatures (improves surface morphology) and contact resistance when compared to thick barrier AlGa<sub>N</sub>. Table 5.2 shows a literature review of recessed ohmic contacts on AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure. The most common gases for etching Ga<sub>N</sub> cap or AlGa<sub>N</sub> are chlorine-based gases such as SiCl<sub>4</sub>, Cl<sub>2</sub>/BCl<sub>3</sub> and Ar/CCl<sub>2</sub>F<sub>2</sub>/O<sub>2</sub>, using in ICP or RIE, ECR (electron cyclotron resonance) dry-etch tool. Three studies Hajlasz *et al.*, Wang *et al.*, and Lau *et al.* used Ti/Al based ohmic recess. They compared non-etched samples with different etch depth and optimised the performance of recessed ohmic contact [5.34] [5.35] [5.36]. Hajlasz *et al.* achieved 0.18 Ω.mm for 10 nm etch depth while, Liang wang *et al.* achieved 0.26 Ω.mm when the 2DEG channel was completely removed, and Lau *et al.* achieved 3.2 Ω.mm for 100 nm etch depth. Further, Zhang *et al.* and Lee *et al.* used Au-free ohmic contact and demonstrated higher ohmic contact compared to non-recessed Au based ohmic contact [5.37] [5.38]. Since very small number of researchers have studied the recessed ohmic contact, there is no clarity which etch depth or annealing temperatures or ohmic metal is better to achieve lower contact resistance than standard non-recessed contacts.

Since the 2DEG sheet carrier concentration depends on the AlGa<sub>N</sub> thickness and Al concentration. Pre-ohmic recess might deplete the 2DEG under the contact metals, which increases the overall contact resistance. As a result, Takei *et al.*, proposed patterned etching under ohmic metal [5.21]. The reason is, the three resistances as discussed before  $R_{c2DEG}$ ,  $R_{cMetal/AlGaN}$ ,  $R_{cAlGaN}$ , which contributes towards total contact resistance  $R_T$  has a dependency on AlGa<sub>N</sub> thickness, which makes  $R_T$  not to be reduced lower than the minimum value. Previous contact formation techniques used non-uniform alloying by means of Au contained metals and trading dislocation to establish localised current paths to evade trade-off limits. These techniques are difficult to use if the contact formation requires higher process controllability and Au-free process [5.22].

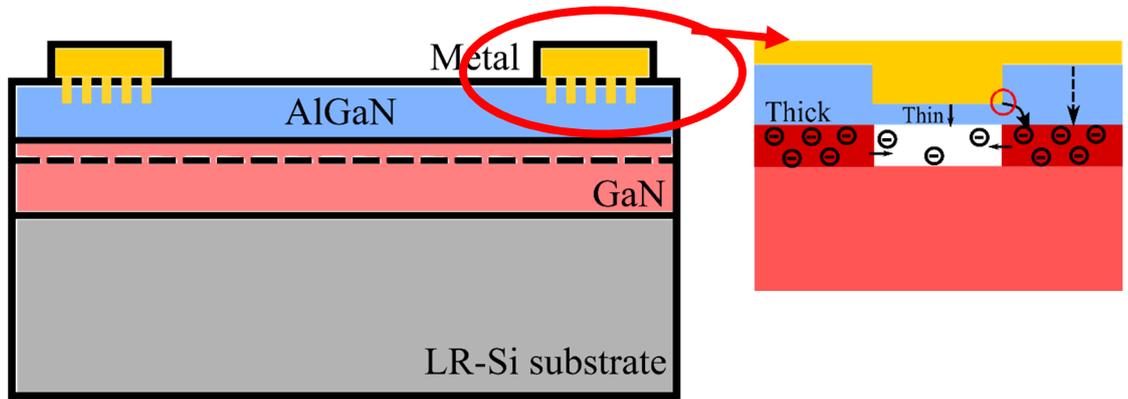
<b>Metal layers (nm)</b>	<b>d<sub>AlGaN</sub> (nm)</b>	<b>X<sub>Al</sub> (%)</b>	<b>Etch depth (nm)</b>	<b>Annealing conditions</b>	<b>R<sub>c</sub> (Ω.mm)</b>	<b>ρ<sub>c</sub> Ω.cm<sup>2</sup></b>	<b>Ref.</b>
Ti/Al	20 nm (3 nm GaN cap)	20%	0 nm	875 <sup>0</sup> C	0.3	5×10 <sup>-6</sup>	[5.34]
Ti/Al	20 nm (3 nm GaN cap)	20%	10 nm	875 <sup>0</sup> C	0.18	5×10 <sup>-6</sup>	[5.34]
Ti/Al	20 nm (3 nm GaN cap)	20%	26 nm	875 <sup>0</sup> C	7.5	4.5×10 <sup>-5</sup>	[5.34]
Ti/Al/Mo/Au (15/60/35/50 nm)	23 nm (10 nm GaN cap)	30 %	35 nm (3.5 mins)	850 <sup>0</sup> C for 30s in N <sub>2</sub>	0.31	3.1×10 <sup>-6</sup>	[5.35]
Ti/Al/Mo/Au (15/60/35/50 nm)	23 nm	30 %	30 nm (3 mins)	850 <sup>0</sup> C for 30s in N <sub>2</sub>	0.41	5.8×10 <sup>-6</sup>	[5.35]
Ti/Al/Mo/Au (15/60/35/50 nm)	20 nm	30 %	30 nm (3 mins)	850 <sup>0</sup> C for 30s in N <sub>2</sub>	0.26	1.7×10 <sup>-6</sup>	[5.35]
Ti/Al/Ti/W (20/120/20/30 nm)	22 nm	25 %	10 nm (60 secs)	600 <sup>0</sup> C for 120s in N <sub>2</sub>	No ohmic contact		[5.37]
Ti/Al/Ti/W (20/120/20/30 nm)	22 nm	25 %	20 nm (120 secs)	600 <sup>0</sup> C for 120s in N <sub>2</sub>	1.12	2.77×10 <sup>-6</sup>	[5.37]
Ti/Al/Ti/W (20/120/20/30 nm)	22 nm	25 %	25 nm (150 secs)	600 <sup>0</sup> C for 120s in N <sub>2</sub>	4.10	3.17×10 <sup>-6</sup>	[5.37]
Ti/Al/Ti/W (20/120/20/30 nm)	22 nm	25 %	30 nm (180 secs)	600 <sup>0</sup> C for 120s in N <sub>2</sub>	3.17	2.14×10 <sup>-6</sup>	[5.37]
Ti/Al/Ni/Au (20/120/55/45 nm)	22 nm	25 %	0 nm	850 <sup>0</sup> C for 50s in N <sub>2</sub>	0.5	5.43×10 <sup>-6</sup>	[5.37]
Ti/Al/Ti/Au	30 nm	----	0 nm	500 <sup>0</sup> C for 120s in N <sub>2</sub>	5.7	----	[5.36]
Ti/Al/Ti/Au	30 nm	----	100 nm	500 <sup>0</sup> C for 120s in N <sub>2</sub>	3.2	----	[5.36]
Ti/Al/W (60/100/30 nm)	17.5 nm (2 nm GaN cap)	26 %	0 nm	950 <sup>0</sup> C for 30s	2.1	8.7×10 <sup>-6</sup>	[5.38]
Ti/Al/W (60/100/30 nm)	17.5 nm (2 nm GaN cap)	26 %	15 nm	870 <sup>0</sup> C for 30s	1.71	----	[5.38]
Ti/Al/W (60/100/30 nm)	17.5 nm (2 nm GaN cap)	26 %	30 nm	870 <sup>0</sup> C for 30s	0.49	6.5×10 <sup>-6</sup>	[5.38]

<b>Metal layers (nm)</b>	<b>d<sub>AlGaN</sub> (nm)</b>	<b>X<sub>Al</sub> (%)</b>	<b>Etch depth (nm)</b>	<b>Annealing conditions</b>	<b>R<sub>c</sub> (Ω.mm)</b>	<b>ρ<sub>c</sub> Ω.cm<sup>2</sup></b>	<b>Ref.</b>
Ti/Al/Ni/Au	17.5 nm (2 nm GaN cap)	26 %	0 nm	870 <sup>0</sup> C for 30s	0.38	3.1×10 <sup>-6</sup>	[5.38]
TiN/TiSi <sub>2</sub> (30/50 nm)	10 nm	25 %	5 nm (patterned etching)	1000 <sup>0</sup> C	4.5	----	[5.21]
TiN/TiSi <sub>2</sub> (30/50 nm)	10 nm	25 %	5 nm (patterned etching)	1000 <sup>0</sup> C	4.5	---	[5.22]
Mo/Ti/Al (35/60/60 nm)	10 nm	25 %	5 nm (patterned etching)	900 <sup>0</sup> C	0.24	---	[5.22]
Ti/Al/Ni/Au (20/140/55/45 nm)	20 nm	27 %	0 nm	830 <sup>0</sup> C for 30s	0.46	---	[5.39]
Ti/Al/Ni/Au (20/140/55/45 nm)	20 nm	27 %		830 <sup>0</sup> C for 30s	0.35	---	[5.39]
Ti/Al/Ni/Au (20/140/55/45 nm)	20 nm	27 %	(patterned etching)	830 <sup>0</sup> C for 30s	0.18	---	[5.39]
Ti/Al/Ni/Au (15/80/20/100 nm)	20 nm	25 %	15 nm (patterned etching)	800 <sup>0</sup> C for 15s	0.2	8.4×10 <sup>-7</sup>	[5.40]
Ti/Al/Ni/Au (Ti filled in vias)	20 nm	----	10 nm (hole etching)	830 <sup>0</sup> C for 30s	0.1	----	[5.41]

**Table 5.2:** Review of recessed and patterned ohmic contact on AlGa<sub>N</sub>/Ga<sub>N</sub> heterostructure.

## Patterned recess technique

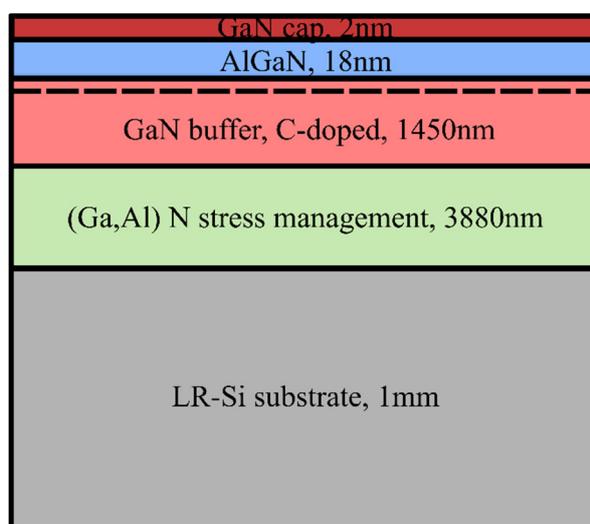
The concept of fabricating an uneven surface underneath the ohmic contact is shown in the Fig. 5.14. The area where the AlGa<sub>N</sub> layer is etched will have a depleted 2DEG and region where the AlGa<sub>N</sub> is not etched will have a higher-density 2DEG. The concept is to extend from the high-density 2DEG region to the thinner AlGa<sub>N</sub> material. In doing so, a fringing effect is produced where the metals and 2DEG with sufficient concentration come within a very small distance of each other. This distance would be unachievable in standard structures with uniform AlGa<sub>N</sub> layers and will reduce the overall contact resistance  $R_C$ , if optimised. Takei *et al.* simulated models of uneven AlGa<sub>N</sub> layers (rectangular, triangular, domed structures) to find the lateral distribution of carrier concentration and to verify experimentally, they fabricated different lateral etch patterns (hole, vertical and horizontal lines) using TiN/TiSi<sub>2</sub> metals. They confirmed the fringing effect, where carrier concentration near the edge in regions of thin AlGa<sub>N</sub> layer increased compared to flat AlGa<sub>N</sub> and found triangular and domed structures were more effective than rectangular structures. The experimental patterns achieved a contact resistance of 4.5  $\Omega$ .mm at 1000<sup>o</sup>C for horizontal lines (10 nm AlGa<sub>N</sub> etch depth) [5.21]. Kazuo Tsutsui repeated the same experiment and tested horizontal etch (parallel to current flow) patterns with different pattern width from 0.4  $\mu$ m to 5  $\mu$ m using Mo/Ti/Al metal. They found that the smaller size pattern (0.4  $\mu$ m width) reduced the ohmic contact further and achieved nearly 0.2  $\Omega$ .mm  $R_C$  at 900<sup>o</sup>C [5.22]. Chong *et al.* investigated pattern etching with single-recessed etching (whole) and no etching for comparison [5.39]. They demonstrated 0.18  $\Omega$ .mm  $R_C$  for patterned etching width of 0.8  $\Omega$ .mm, 0.35  $\Omega$ .mm for single-recess (whole) and 0.46  $\Omega$ .mm for no etching, which proved the concept of Takei *et al.* Further, they commented on the surface roughness of the contact. Single recess showed the lowest RMS value of surface roughness 19.84 nm, whereas standard and patterned showed 39.25 nm and 43 nm respectively. Kefeng Han included hole recess only half the ohmic pad nearer to the gaps of the TLM lines and achieved 0.2  $\Omega$ .mm at 800<sup>o</sup>C [5.40]. They observed reduction of irregular metal particles and metal bumps after annealing and a relatively straight metal edge, which suggests improved surface morphology of the contacts. The lowest contact resistance of 0.1  $\Omega$ .mm was achieved by Wang *et al.*, using the technique detailed here [5.41]. They filled the etched holes with Ti metal, which generated additional N vacancies during annealing and thus reduced the contact resistance further. To determine optimal technique for achieving lower contact resistance on AlGa<sub>N</sub>/Ga<sub>N</sub> on LR Si substrate, I have experimented from standard methods to single recessed to patterned recessed. The next section deals with performance of the ohmic contact on Ga<sub>N</sub>-on-LR Si substrate.



**Fig. 5.14:** Observed fringing effect when the AlGaN/GaN heterostructure below ohmic contact is etched uneven [5.21].

## 5.5 Results and Discussion

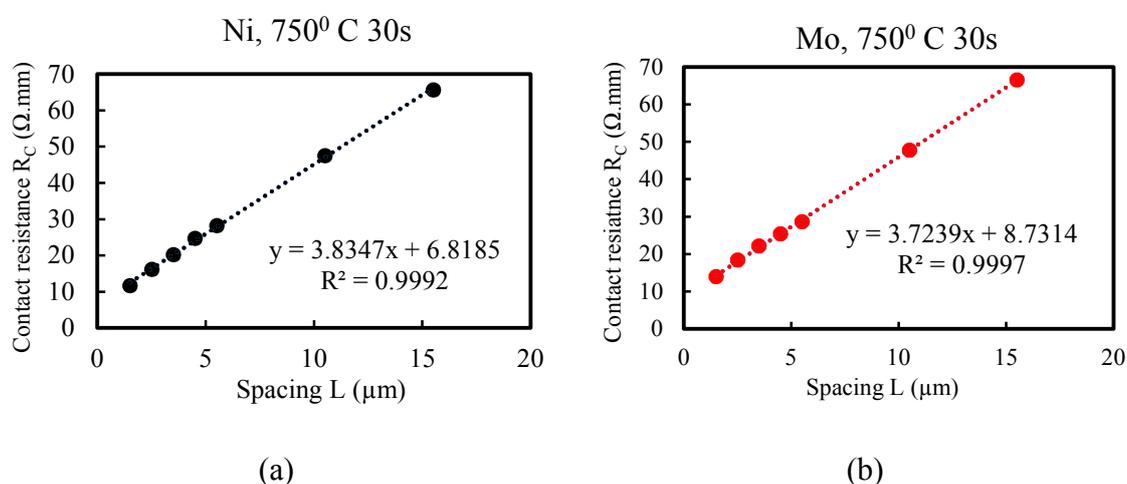
The epitaxial layer structure used for optimising ohmic contact resistance on GaN-on-LR Si is as shown in the Fig. 5.15. This material was purchased from IQE U.S and growth of AlGa<sub>N</sub>/Ga<sub>N</sub> was done on a 1 mm thick silicon substrate by metal organic chemical vapour deposition (MOCVD). The process starts with the growth of a Ga<sub>N</sub> stress management layer of 3880 nm, followed by a carbon doped buffer layer of 1450 nm and the formation of an 18 nm Al<sub>x</sub>Ga<sub>1-x</sub>N (X=0.26) and 2 nm Ga<sub>N</sub> cap layer. We started out by using standard ohmic metals such as Ti/Al/Ni/Au and Ti/Al/Mo/Au. Later, patterned substrate etching under the ohmic contacts is investigated.



**Fig. 5.15:** Schematic of the AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT on LR Si silicon (111).

### 5.5.1 Standard ohmic contact on AlGaIn/GaN

Fabrication of ohmic contacts on GaN-on-LR Si is explained in Chapter 2. Two different standard ohmic metal stacks- Ti/Al/Ni/Au and Ti/Al/Mo/Au were used for comparison at various annealing temperatures. Two samples of size 1×1 inch was processed in parallel using e-beam lithography. After two lithography steps, defining the ohmics and mesa etch, each sample was cleaved into 12 sets which were then annealed at 12 different temperatures from 750<sup>0</sup> to 860<sup>0</sup> C with a difference of 10<sup>0</sup> C between samples for 30 s. Fig. 5.16 shows the plot of contact resistance R<sub>C</sub> extracted from TLMs as a function of TLM spacing at 750<sup>0</sup> C annealing temperatures for both Ni and Mo metal stacks. Details of TLM measurements and sheet resistance at various annealing temperatures are given in Table 5.3.



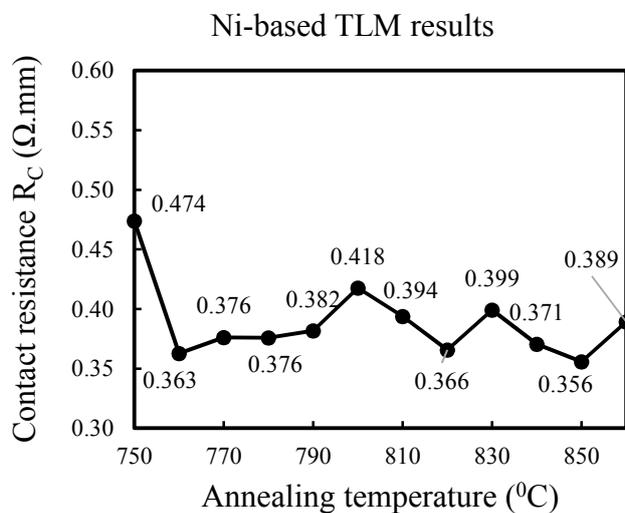
**Fig. 5.16:** Extracted  $R_C$  values from TLMs annealed at 750<sup>0</sup> C for 30s (a) Ni as barrier (b) Mo as barrier.

Annealing temperature (°C)	Contact resistance (Ω.mm)		Correlation		Sheet resistance Ω/□	
	Ni	Mo	Ni	Mo	Ni	Mo
750°C for 30s	0.474	0.655	0.9997	0.9998	583.5	558.59
760°C for 30s	0.363	0.668	0.9998	0.9999	604.1	578.40
770°C for 30s	0.376	0.575	0.9998	0.9998	597.4	580.61
780°C for 30s	0.376	0.561	0.9999	0.9998	622.8	575.48
790°C for 30s	0.382	0.508	0.9996	0.9998	569.6	562.38
800°C for 30s	0.418	0.534	0.9998	0.9997	555.3	563.43
810°C for 30s	0.394	0.516	0.9995	0.9998	632.2	569.67
820°C for 30s	0.366	0.500	0.9999	0.9999	580.0	576.27
830°C for 30s	0.399	0.541	0.9999	0.9999	588.2	523.80
840°C for 30s	0.371	0.507	0.9999	0.9992	590.6	536.49
850°C for 30s	0.356	0.583	0.9998	0.9998	609.2	558.83
860°C for 30s	0.389	0.620	0.9999	0.9999	599.6	526.85

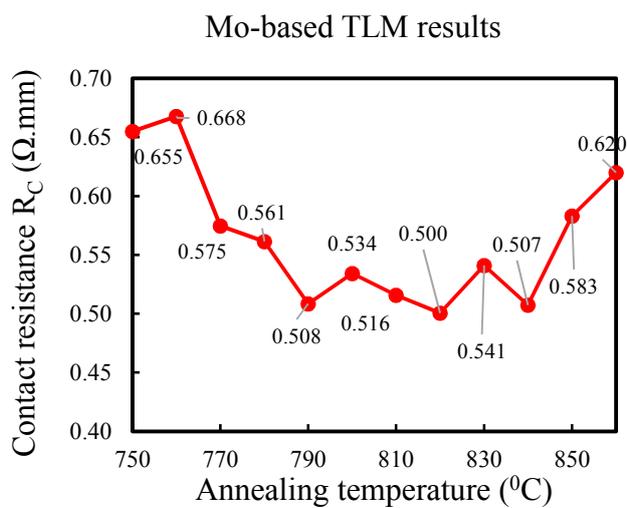
**Table 5.3:** Details of TLMs for Ni and Mo as barrier layer at various annealing temperatures.

Fig. 5.17 (a) shows the summarised contact resistance for various annealing temperatures of the Ni metal stack. The contact resistance decreased from 0.474 to 0.376 Ω.mm between 750<sup>0</sup> to 790<sup>0</sup>C and then there was a sudden increase in contact resistance at 800<sup>0</sup> to 810<sup>0</sup> C and again a rise at 830<sup>0</sup> and 860<sup>0</sup> C. The data points didn't follow any particular trend as expected (higher contact resistance at ends of annealing temperatures and lower in middle). The lowest contact resistance achieved was 0.356 Ω.mm at 850<sup>0</sup> C and highest was 0.474 Ω.mm at 750<sup>0</sup> C. As all samples were fabricated in parallel, there should be minimal fabrication difference between them. As such, the difference in R<sub>C</sub> is primarily related to the anneal temperature and the way the ohmic metal is formed. Fig. 5.17 (b) shows the contact resistance for various annealing temperatures for the Mo metal stack. The contact resistance decreases from temperature 770<sup>0</sup> C and again increases at 860<sup>0</sup> C. The data points were more parabolic trend compared to Ti/Al/Ni/Au, this may be due to the several factors like metals not being deposited under good vacuum or difference in annealing environment. The highest contact resistance achieved was 0.668 Ω.mm at 760<sup>0</sup> C and lowest was 0.5 Ω.mm at 820<sup>0</sup> C. The lowest contact resistance may be due to the formation of TiN island at this temperature, as explained in Section 5.4.1 [5.15]. The standard deviation for TLMs measurement was

calculated to be between  $\pm 0.18 \Omega.\text{mm}$  and  $\pm 1 \Omega.\text{mm}$  (average from 3 TLMs data), which is low to be represented in the graph. The average correlation achieved was 0.999, which shows good homogeneity of the ohmic contact annealed and the average sheet resistance was  $571.6 \pm 20.7 \Omega/\square$  between various temperatures and samples.



(a)

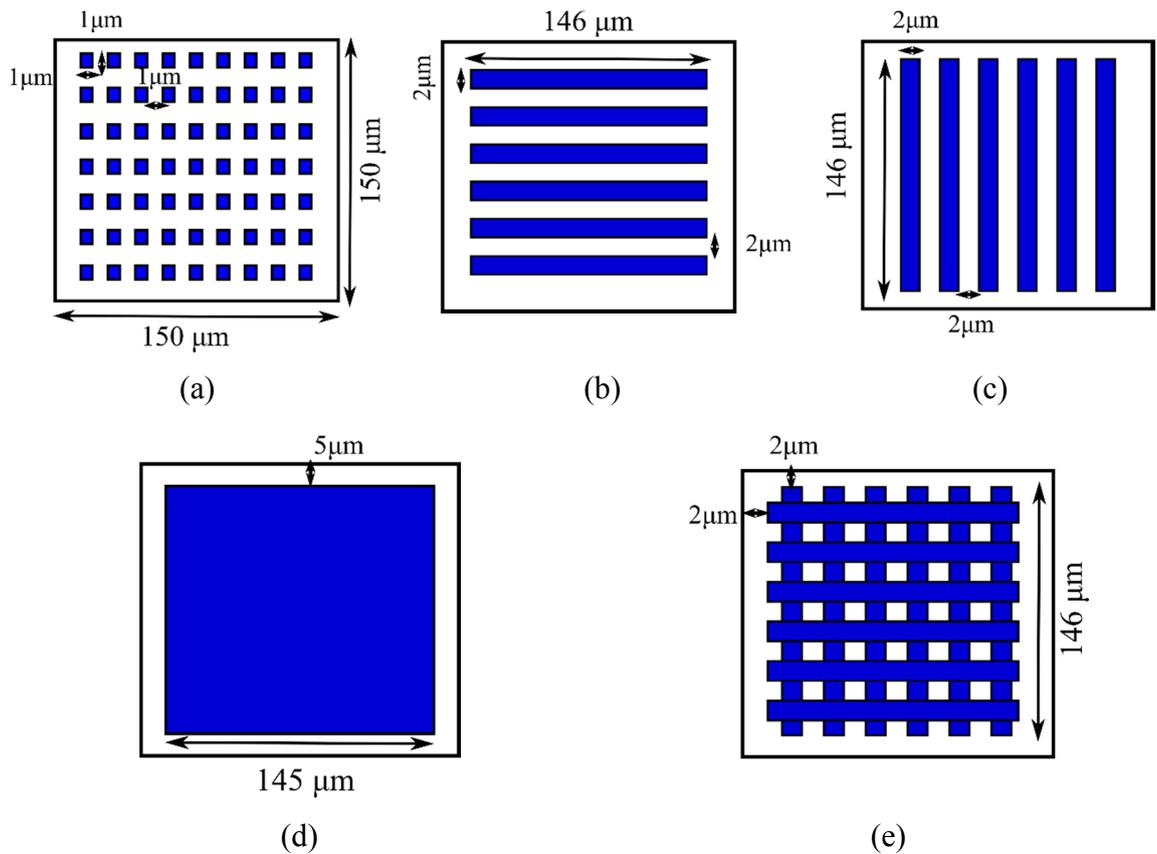


(b)

**Fig. 5.17:** Summaried contact resistance (a) Ni (b) Mo at various annealing temperature.

### 5.5.2 Patterned and whole etching on AlGaN/GaN

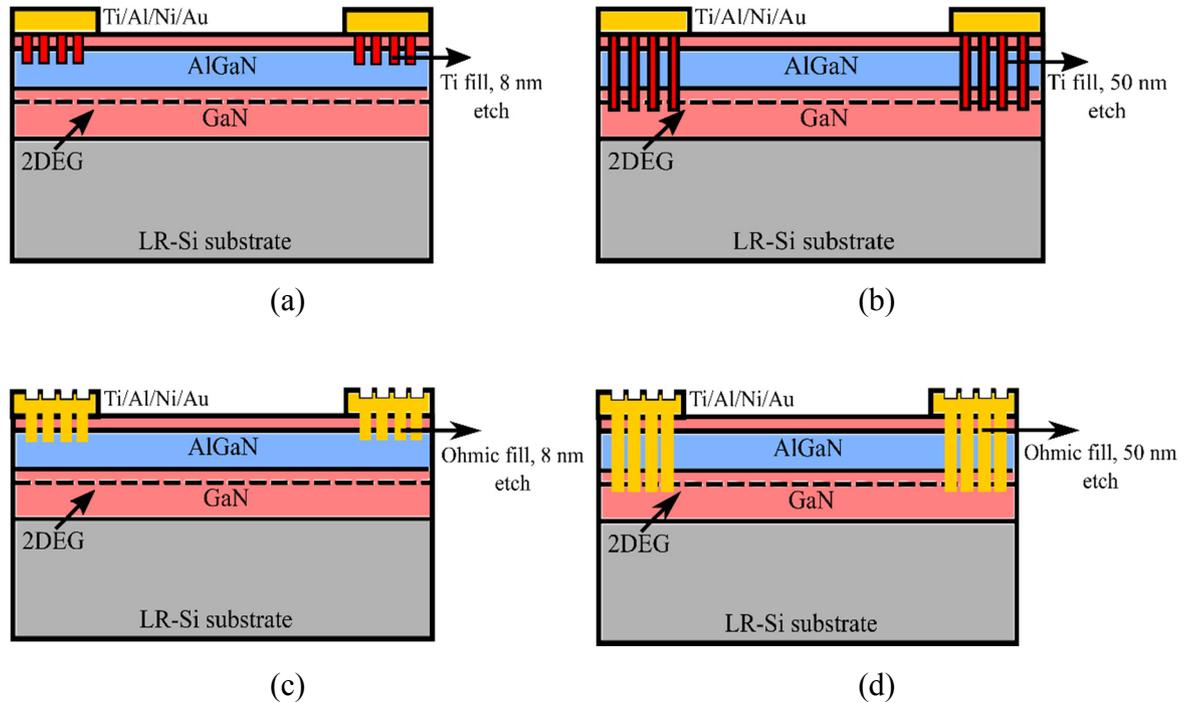
Fig. 5.18 shows the different pattern etching used for this experiment. The first pattern (a) is a hole array of size  $1 \times 1 \mu\text{m}$  rectangles with  $1 \mu\text{m}$  separation. Second (b) is a horizontal line array (parallel to current flow) of size  $2 \times 146 \mu\text{m}$  lines separated by  $2 \mu\text{m}$ . Third (c) is a vertical line pattern of the same geometry perpendicular to direction of current flow. Next (d) is a whole area etch of size  $145 \times 145 \mu\text{m}$  and lastly (e) a combination of both vertical and horizontal etch called grid etch. A control pattern with no etching was included for comparison.



**Fig. 5.18:** Etch patterns of uneven AlGaN/GaN structures used in this experiment (a) hole (b) horizontal (c) vertical (d) whole recessed (e) grid.

Fig. 5.19 shows the cross-section schematic of the sample sets prepared for this experiment. Samples were divided into four different sets, set I and III were etched above the 2DEG channel, while set II and IV were etched below the 2DEG channel. In addition, experiments were designed using planar and non-planar ohmic surface i.e. the top surface of the contact would be uniform or non-uniform. Set I and II were fabricated by filling the etched pattern with an appropriate thickness of Ti metal (planar ohmic pads) and for set III and IV there was no additional metal fill (non-planar ohmic pads). Ti/Al/Ni/Au was used as the ohmic

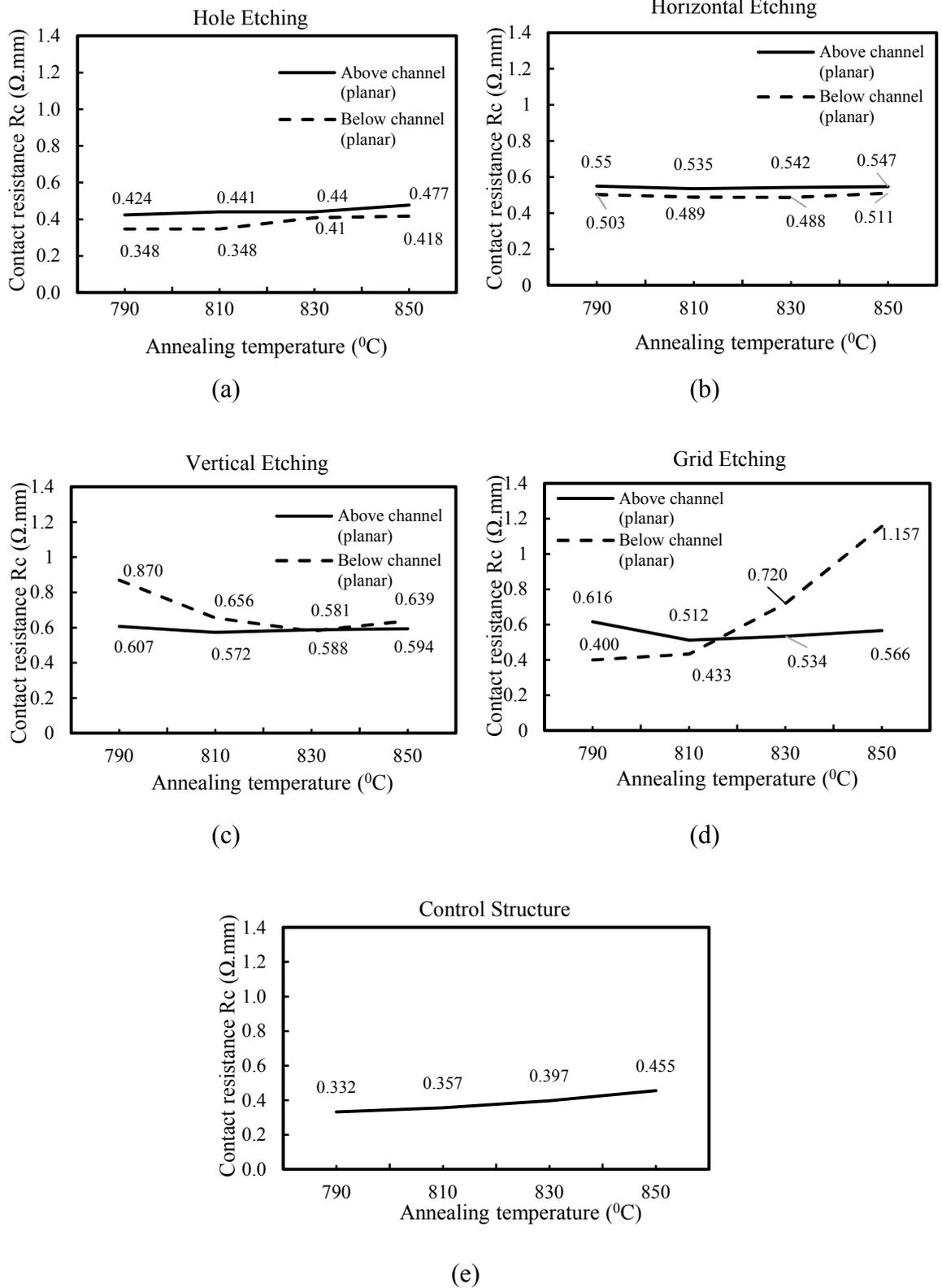
metal stack for all the patterns and gaps of TLMs were same as those made previously. Each set had four samples for four annealing temperatures (790, 810, 830, 850 °C) and each sample had all five etch patterns, a control pattern of no etch and three VDP structures for Hall measurement purposes. The fabrication of these patterns is explained in the Chapter 2.



**Fig. 5.19:** Cross-section schematic of etch patterns (a) above etch, planar ohmic surface (b) below etch, planar ohmic surface (c) above etch, non-planar ohmic surface (d) below etch, non-planar ohmic surface.

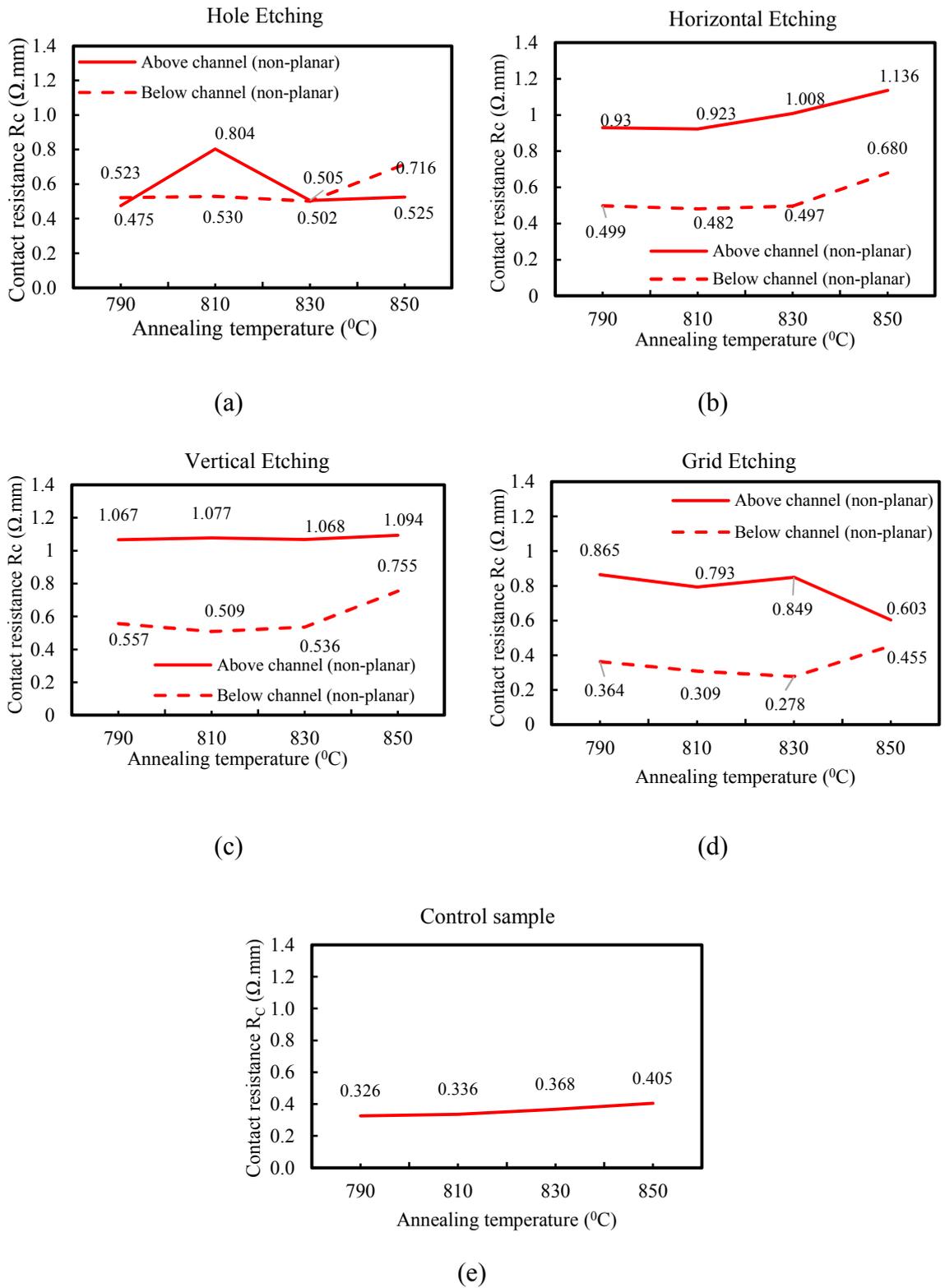
Fig. 5.20 shows the measurement of contact resistance with annealing temperature for different etch depths, etch patterns, planar contacts and the control design. Above channel etching is represented by a black solid line, and below channel etching is represented by black dashed line. Above channel etching showed greater contact resistance (0.424 - 0.616  $\Omega$ .mm) in general compared to below channel etching (0.348 - 1.157  $\Omega$ .mm), except in the grid and vertical etch pattern designs. Single recess exhibited very high contact resistance or high sheet resistance for both planar and non-planar ohmic surface, and above and below etching ohmic contact. For a TLM gap of 1.5  $\mu$ m, a 300  $\Omega$  resistance was measured. This high contact resistance was an anomaly may be due to the defect of the material. Below channel etching for both vertical and grid patterns showed some unusual behaviour. For vertical etching there was a sudden dip in the contact resistance at 810<sup>0</sup> C and for grid etching there was a sudden rise in contact resistance at 810<sup>0</sup> C. These anomalies might be due to ohmic roughness or impurities in GaN which contribute towards contact resistance.

Comparing all above channel etching, the hole pattern exhibited a lower contact resistance in general (0.424 - 0.477  $\Omega$ .mm) compared to horizontal (0.535 - 0.555  $\Omega$ .mm), vertical (0.572 - 0.607  $\Omega$ .mm) and grid etching patterns (0.512 - 0.616  $\Omega$ .mm). For below channel etching patterns, hole etching exhibited lower contact resistance (0.348-0.418  $\Omega$ .mm) in general compared to horizontal (0.488-0.511  $\Omega$ .mm), vertical (0.581-0.870  $\Omega$ .mm), and grid (0.4 - 1.157  $\Omega$ .mm). Comparing this to the control sample, a contact resistance of 0.332 - 0.455  $\Omega$ .mm was achieved, which showed better performance than above or below etching with planar ohmic surfaces.



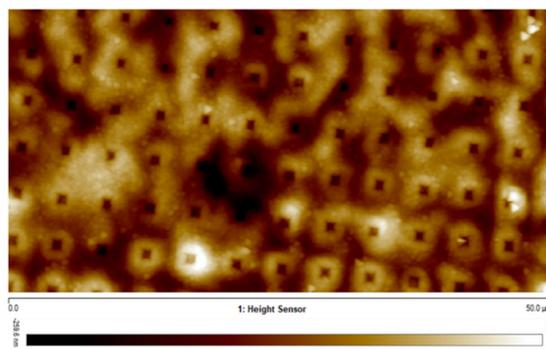
**Fig. 5.20:** Plot of contact resistance vs annealing temperatures for various etch pattern for planar ohmic surface (a) hole (b) horizontal (c) vertical (d) grid (e) control sample.

Fig. 5.21 shows the measurement of contact resistance with annealing for the non-planar samples. Above channel etching is represented by a red solid line and data of below etching is represented by a red dashed line. Above channel etching showed higher ohmic contact resistance (0.475 - 1.136  $\Omega$ .mm) compared to below channel for non-planar ohmic surfaces (0.278 - 0.755  $\Omega$ .mm). Comparing to other above channel etching, hole etching (0.475 - 0.804  $\Omega$ .mm) performed better in general than horizontal etching (0.93 - 1.136  $\Omega$ .mm), vertical (1.077 - 1.094  $\Omega$ .mm) and grid etching (0.603 - 0.865  $\Omega$ .mm), despite the unusual spike at 810<sup>0</sup>C. Below channel etching with a grid design (0.278-0.455  $\Omega$ .mm) performed better than hole (0.502 - 0.716  $\Omega$ .mm), horizontal (0.482 - 0.68  $\Omega$ .mm) and vertical etching (0.509 - 0.755  $\Omega$ .mm). Relating these results to the control sample, an average contact resistance of 0.35 to 0.41  $\Omega$ .mm was achieved. A contact resistance of 0.27  $\Omega$ .mm was observed for a grid patterned ohmic contact employing below channel etching and an anneal temperature of 830<sup>0</sup>C. By comparison, the lowest contact resistance measured for TLM's without etching was 0.32  $\Omega$ .mm, annealed at 790<sup>0</sup> C. Since the annealing temperature only differed by 20<sup>0</sup>C, it is possible that a contact resistance of less than 0.27  $\Omega$ .mm was achieved between the annealing temperatures of 810 and 850<sup>0</sup> C.

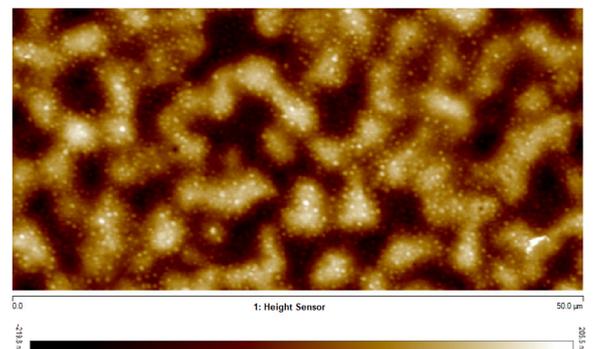


**Fig. 5.21:** Plot of contact resistance vs annealing temperatures for various etch pattern for non-planar ohmic surface (a) hole (b) horizontal (c) vertical (d) grid (e) control sample.

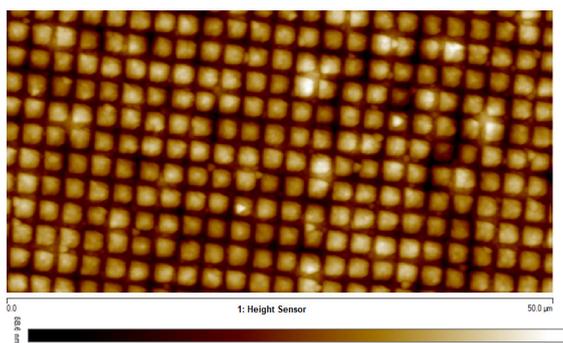
Fig. 5.22 shows AFM roughness scans for planar and non-planar ohmic contact surfaces for each etch pattern annealed at 790<sup>0</sup>C. Comparing the non-planar surface with planar, the etch pattern is clearly visible in the non-planar design. Whereas for the planar design, with etched regions filled with Ti metal, the pattern is far less visible. Since there are 80 TLM structures to be presented, Table 5.4 shows the summarised AFM roughness scan for planar/non-planar surfaces with above and below channel etching patterns. A large scan size of 50  $\mu\text{m}$  was used due to the spacing of the etch pattern features. AFM roughness for all contacts increased with annealing temperature, interestingly roughness was similar for all contacts. This suggest that Au reflowed for non-planar contacts. Comparing etch patterns with the control structure, the non-etched contacts exhibited very similar roughness to the etch patterns and some areas of the ohmic pads showed bulges. The possible reason behind higher roughness is the Ni as barrier layer, during rapid annealing it forms Ni-Al alloy aggregation in some areas [5.26]. This may be solved using Mo metal as the barrier rather than Ni [5.42].



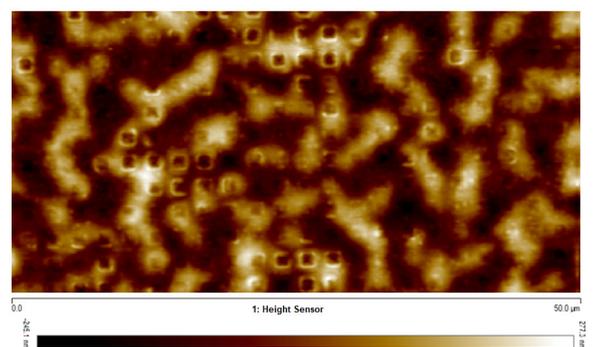
(a) Grid-non-planar ohmic surface



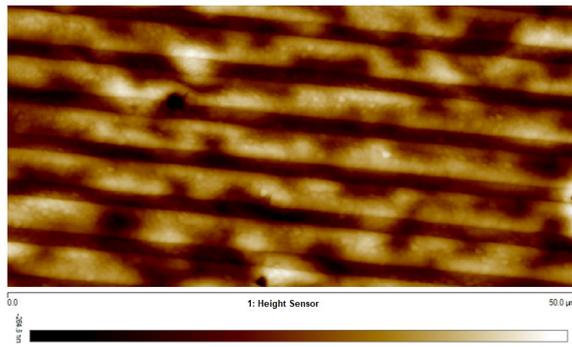
(b) Grid-planar ohmic surface



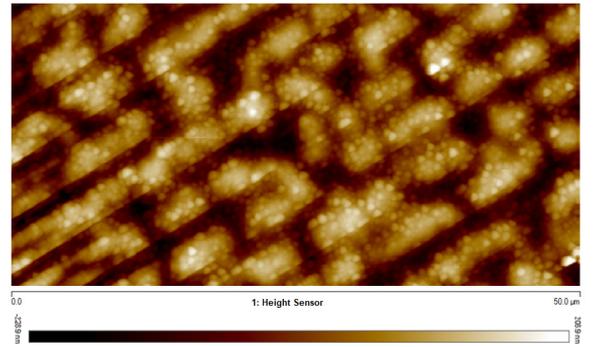
(c) Hole-non-planar ohmic surface



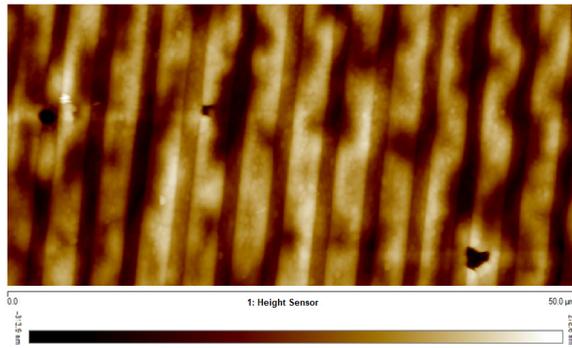
(d) Hole-planar ohmic surface



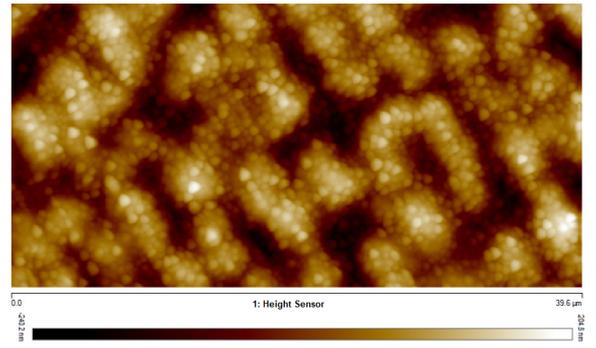
(e) Horizontal-non-planar ohmic surface



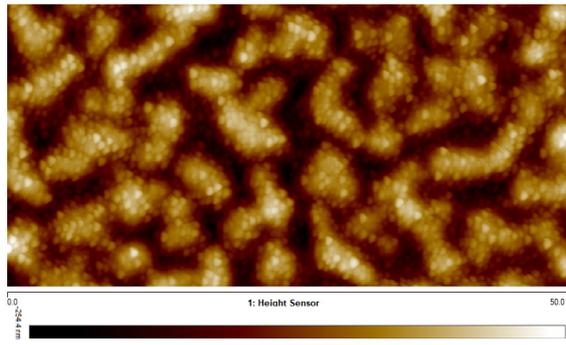
(f) Horizontal-planar ohmic surface



(g) Vertical-non-planar ohmic surface



(h) Vertical-planar ohmic surface



(i) Standard ohmic surface

**Fig. 5.22:** AFM scans for analysing roughness for patterned etch and standard sample at 790°C annealing temperature.

Sample set	Etch Pattern	AFM Roughness by annealed temperatures (RMS nm)			
		790°C	810°C	830°C	850°C
Set I (Ti fill, 8nm etch)	No etch (control structure)	75.4	88.9	92	101
	Holes	64.2	91.8	68.7	65.5
	Horizontal	73.7	92.5	91	103
	Vertical	69.3	85.4	100	98.6
	Grid	70.7	86.2	93	95.8
Set II (Ti fill, 50nm etch)	No etch (control structure)	N/A			
	Holes	88.7	97.2	97	106
	Horizontal	87.6	84.9	95.2	103
	Vertical	93.9	94.6	101	101
	Grid	94.8	101	104	115
Set III (ohmic fill, 8nm etch)	No etch (control structure)	81	97.5	103	112
	Holes	61.3	72.4	82.9	73.4
	Horizontal	87	105	80.6	100
	Vertical	91.2	108	102	105
	Grid	69.4	88.1	79.3	71.1
Set IV (ohmic fill, 50nm etch)	No etch (control structure)	N/A			
	Holes	56.7	61.9	87.6	110
	Horizontal	82.3	99.1	105	105
	Vertical	102	106	70.4	103
	Grid	92.5	92.2	88.7	108

**Table 5.4:** AFM roughness scan for patterned etch and control structure at various annealing temperatures.

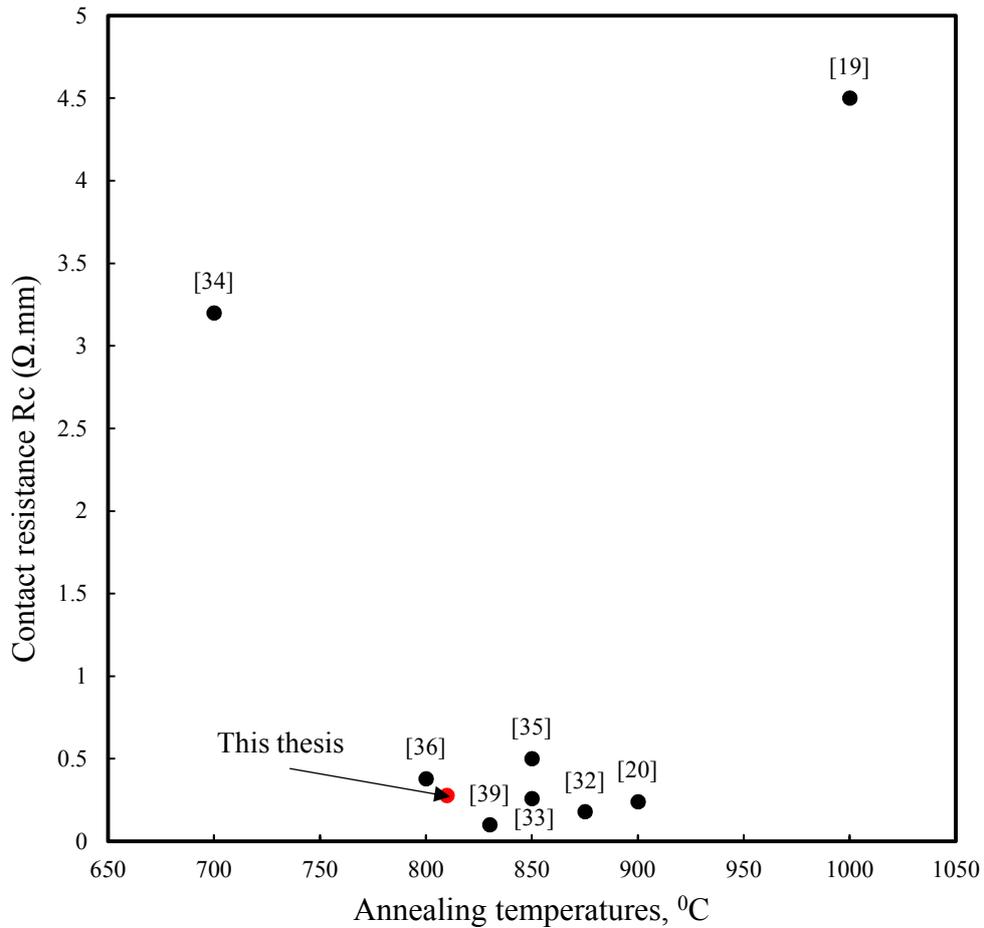
In conclusion, the concept of an irregular AlGa<sub>N</sub> layer underneath the ohmic metal was proposed to reduce ohmic contact resistance. This method improves access to the 2DEG by creating fringes near the edges of the etched AlGa<sub>N</sub> and high-density 2DEG located just outside these regions [5.21] [5.41]. With this, a plasma etching process creates N vacancies at the surface of the AlGa<sub>N</sub> and the formation of TiN in the ohmic metal after annealing further lowers contact resistance. The improved tunnelling effect through N vacancies can be explained through equations detailed below [5.39]. N vacancies are created at the surface of AlGa<sub>N</sub> [5.41] [5.39], which increases the donor doping concentration  $N_d$  and electric field  $E_{00}$ , Equation (5.41). Thus, increasing the tunnel current  $J_t$  and reducing the contact resistance  $R_C$ , Equation (5.39) & (5.41).

$$R_c = \left( \frac{\partial J}{\partial V} \right)^{-1} \Big|_{V=0} \Omega.cm^2 \quad (5.34)$$

$$J_t \propto \exp\left(\frac{-e\phi_{Bn}}{E_{00}}\right) \quad (5.35)$$

$$E_{00} = \frac{e\hbar}{2} \sqrt{\frac{N_d}{\epsilon_s m_n^*}} \quad (5.36)$$

Above channel etching for both planar and non-planar surfaces demonstrated higher ohmic contact resistance compared to below channel etching. This may be due the barrier height still present, requiring electron tunnelling between the ohmic metal and 2DEG channel. Comparing above channel non-planar ohmic surface to planar ohmic surface, filling the trenches with metal had a large impact on reduction of contact resistance. In below channel etching, we find that non-planar ohmic surfaces performed much better than the planar surface, indicating the extra filling of Ti metal in the etched area did not make any significant improvement to contact resistance. Previous research [5.34] [5.37] has shown etching below the 2DEG channel in the case of single recess ohmic contacts exhibited high contact resistance. Even though the barrier height is low, absence of a 2DEG channel underneath causes tunnelling to occur at a very small area around the sidewall of the recessed barrier. In our case, since several small areas are etched underneath the ohmics, tunnelling may occur around the sidewall of the etched region, achieving lower contact resistance. Overall, below channel etch patterns and increased sidewall exposure exhibited lower contact resistance which was lower than the contact resistance of non-etched contacts, thus making this technique viable. A comparison between the measured contact resistances  $R_C$ , which was obtained in this work, with other published work on AlGa<sub>N</sub>/Ga<sub>N</sub>-based devices is shown in the Fig. 5.23.



**Fig. 5.23:** Comparison of  $R_c$  as a function of annealing temperatures on AlGaIn/GaN HEMT structures for recessed structures from various publications.

## 5.6 Conclusion

In this chapter, the optimisation of ohmic contact formation on AlGaIn/GaN HEMT structures on LR Si has been discussed. Initially, a non-etch approach was adopted to achieve contact resistance less than  $0.4 \Omega \cdot \text{mm}$ . Here, Ti/Al/Ni/Au and Ti/Al/Mo/Au metal schemes were explored, where contact resistance of  $0.356 \Omega \cdot \text{mm}$  at  $850^\circ \text{C}$  and  $0.5 \Omega \cdot \text{mm}$  at  $820^\circ \text{C}$  respectively was achieved. Patterned etching of the substrate surface under the ohmic contact was introduced to further reduce the contact resistance. A grid pattern etched below channel achieved a lower contact resistance ( $0.278 \Omega \cdot \text{mm}$ ) compared to the non-etched control structures ( $0.35 \Omega \cdot \text{mm}$ ). Using a grid pattern produces increased exposed sidewall area and is most likely the cause of reduced contact resistance. Below channel etching also exhibited lower contact resistance compared to above channel etching. Further, use of extra Ti metal in the etched trenches to produce a planar surface showed a reduction in contact resistance for above channel etching compared to below channel etching. This fabrication method is a

simple and cost-effective way to further reduce ohmic contact resistance, which will benefit RF and power devices based on GaN-on-LR Si.

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## Conclusions and Future work

With the recent progress in semiconductor technologies and state of the art TMIC offering increased cut-off frequencies of HEMT/HBT ( $> 1$  THz), the demand for improved integration and passive devices has increased. III-V materials are well suited for this, as they offer high power and low noise for an active device. The use of GaN HEMTs, grown on low resistivity (LR) Si, for TMIC circuits also has an advantage of low cost and large wafer sizes.

The integration of efficient high frequency planar antenna is a fundamental task for the realisation of high-speed communication and sensing instruments. However, when placed on a GaN-on-LR silicon substrate, due to the high dielectric constant and thickness of the substrate, the antenna experiences high losses. These issues become especially problematic at terahertz frequencies, as power generated by the amplifier is relatively low. In this thesis, we have introduced a state of the art shielding technique, where the antenna is shielded from the substrate using silicon nitride and ground metal, with low dielectric material as an isolation layer between them. Antenna design began by evaluating microstrip transmission lines up to 1 THz using this shielding technique. The dielectric materials investigated for this were air, BCB (Benzocyclobutene), and SiO<sub>2</sub> (silicon-dioxide). Simulated air dielectric performed well up to 200 GHz, however at higher frequencies leakage became apparent due to an opening in the shielding ground plane. Simulated BCB dielectric presented -4 dB transmission co-efficient at 1 THz and simulated SiO<sub>2</sub> resulted in -6.3 dB transmission co-efficient at 1 THz. Informed by the simulated data, antenna were designed using BCB and SiO<sub>2</sub> at 270 GHz. First, a single element rectangular and circular patch was designed using BCB, which presented directivity around 7 dB and gain around 1 dB. To improve this single element performance, a stack antenna was designed where the first patch was designed on BCB and the second patch was elevated in air. Three variants of stack antenna (double rectangular, double circular, and rectangular-circular) was designed to evaluate each configuration. The rectangular-circular stack antenna performed well with a 51.4 % increase

in gain and a 33.3 % increase in the radiation efficiency over a single microstrip antenna. Simulations were carried out to find the optimum performance of the antenna with respect to dielectric height. In addition, a  $4 \times 1$  array antenna was designed to evaluate the array configuration using the shielding technique. A directivity of 11.2 dB and gain of 5.2 dB was achieved. These results show the viability of shielding technology using BCB as a dielectric. Similar antenna configurations were also designed using SiO<sub>2</sub> as the dielectric. Performance of these antenna were lower compared to BCB, but directivity achieved by a  $4 \times 4$  array antenna on SiO<sub>2</sub> was higher than any planar antenna reported in this thesis. All simulated devices were fabricated, however only devices incorporating BCB were physically measured for reflection co-efficient. Measured reflection co-efficient agreed well with simulated values at 270 GHz.

The shielding technique, which proved to be effective, was also used to develop couplers (branch line, cascaded branch line, rat race, and curved rat race) and power dividers (Wilkinson power divider) at three frequencies (90, 300, and 650 GHz) using SiO<sub>2</sub> on GaN-on-LR Si to compare performance. The power division at 90 GHz was almost equal. However, as the frequency increased there was an observation of signal loss at the one of the output ports due to high dielectric constant and coupling loss between the arms. The curved rat race coupler performed worst of all, as further optimization of the bend angle and radius was likely required. All simulated devices were fabricated, however only the 90 GHz branch line and 90 GHz cascaded branch line coupler were measured due to time constraints. Both measured circuits showed very good agreement with simulated results, with respect to matching and isolation. However, power at the output ports appeared to have experienced coupling loss, which has resulted in an increase of power division at the output port. Both simulated and measured results for these circuits show the viability of the shielding technique and SiO<sub>2</sub> as the dielectric material. This is the first time such a technology has been studied for TMIC compatible applications. In addition, this technology can be used for newly emerging high-speed electronics on GaN-on-LR Si, without any micromachining or use of high temperature fabrication. As a result, this approach is more cost effective, can be mass produced, and is relatively compact and suitable for portable TMICs wireless communication and spectroscopy imaging.

With the continued scaling of transistors to obtain increased bandwidth, speed of operation and packing density, achieving lower metal-semiconductor contact resistance (below 0.4  $\Omega$ .mm) becomes crucial. Optimisation of ohmic contact formation on AlGaIn/GaN HEMT structures, on LR Si, has been presented. Various etch patterns (holes, grid, vertical,

horizontal, single-recess) under metal contacts were investigated to reduce contact resistance. Two etch depths- above and below the conducting channel, and metal schemes Ti/Al/Ni/Au were used. The effect of planar and non-planar metal, as well as anneal temperature, was also investigated. For each type of metal contact formed, a non-etched contact was also fabricated for direct comparison. A contact resistance of  $0.356 \Omega \cdot \text{mm}$  at  $850^{\circ} \text{C}$  and a resistance of  $0.5 \Omega \cdot \text{mm}$  at  $820^{\circ} \text{C}$  was achieved for Ti/Al/Ni/Au and Ti/Al/Mo/Au. A grid pattern, etched below the conducting channel, exhibited the lowest contact resistance at  $0.278 \Omega \cdot \text{mm}$ . This fabrication method is a simple and cost-effective way to further reduce ohmic contact resistance, which will benefit RF and power devices based on GaN on LR Si.

Building upon the work shown in this thesis, an end fire antenna (Vivaldi antenna) using the shielding technique shown could produce advanced antenna performance. EBG (Electromagnetic bandgap) structures could also be implemented to reduce the dielectric loss of  $\text{SiO}_2$ . Further, examination of the SIW antenna (Substrate Integrated waveguides) structures to improve the antenna efficiency. These designs could then be integrated with RTDs (Resonant tunnelling diode) or Schottky diodes for power radiation and detection. Depending on coupler performance, implementing different coupler configurations to reduce the coupling effect from the output arm would also benefit this technology. The etching strategy for reducing contact resistance can also now be integrated into the fabrication of RF HEMT transistors on AlGaN/GaN.