Germanium on Silicon Single Photon Avalanche Detectors

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Abstract

In recent years there has been an increased demand in both the civilian and military sectors for high performance single photon detectors. With potential uses in LIDAR technologies, quantum key distribution and remote gas sensing, various single-photon detection techniques have been developed. There has been a significant lack of technologies, however, that would cover a demand for low cost, robust, eye safe, short-wave infrared region (SWIR) sensitive devices. Wavelengths between 1310 nm and 1550 nm are especially interesting for the quantum communications and rangefinding. The lower photon energy at these wavelengths compared to the visible enable a twenty-fold increase in laser source power while still remaining eye safe. Additionally, operating at wavelengths close to 1550 nm provides the best atmospheric penetration length in various hostile environmental conditions, including rain, snow, fog, smoke and haze (1)(2). Such detectors could prove crucial for realizing concepts like self-driving cars and autonomous vehicles and are essential for quantum communications and SWIR quantum optics applications. Cryogenic operating temperatures, high rates of afterpulsing, and high manufacturing prices are among many other obstacles preventing existing technologies from mass market penetration.

In this thesis I will present single photon avalanche detectors (SPADs) operating with a separate Ge absorber and a Si multiplication structure fabricated using a CMOS process. This structure was chosen in order to utilize Ge absorption at wavelengths up to 1600 nm at 300 K (3) and the ability to grow high quality Si multiplication region with few trap states. The present devices demonstrate an order of magnitude higher single photon detection efficiency (SPDE) and 3 orders of magnitude lower dark count rates (DCR) than previously reported Ge on Si SPAD devices (4) (5) and can still provide Geiger mode single photon detection up to 175 K.

"It means your future hasn't been written yet, no one's has. Your future is whatever you make it, so make it a good one."

— Doc Brown

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Introduction

1.1 Brief historical background

For a long time people did not seem to be that interested in investigating the nature of light. The earliest records of people trying to understand this phenomenon come from V B.C. The first person who tried to understand more about its nature was a Greek Philosopher Empedocles, who thought that light must be comprised of rays which are emitted from the human eye, allowing him to perceive the world around. This was a recognized theory until Euclid wrote his classic work "Optica". In this book about the propagation of light, he proposed that light rays must not be emitted by the human eye, but rather an external source. However, his theory had no scientific background until the works of Ibn al-Haytham in the 1000 A.D. In his "Book of Optics" he used the basic principles of experimentation and conducting experiments (that he developed and were a progenitor to the modern scientific method), to show with usage of lenses, mirrors, effects of refraction and reflection that (as he theorized) light travels in straight perpendicular lines to reach a human eye. The next major breakthrough occurred in the 17th century where Descartes proposed his view of light being a "pressure" that is transmitted from source to a detector, a theory later improved on by Huygens and Hooke around 1670. Newton opposed Descartes view of light, with his theory on light being a particle. This was a highly regarded theory in the scientific community thanks to Newton's well established position as a scientist. In 1800 Young's and later in 1816 Fresnel's experiments seemed to vote in favor of a wave-like description of light. This wave-like description was further cemented by the elegance and deep meaning of

Maxwell's equations. Since the beginning of 20th century our understanding of the nature of light has changed dramatically. The revolution started in 1909 with Planck, who proposed a novel way of explaining one of the big mysteries of that time - black body radiation spectrum, with a quantized electromagnetic radiation (6), (7). Only five years later Einstein used this formalism, considered at that time to be a a mathematical oddity without real-life sense, to explain the effect which would later grant him a Nobel prize on the photoelectric effect (8). This was followed by the work of Compton in 1923 regarding the wavelength shift of scattered x-rays (9). Compton's works allowed de Brogile in 1924 to form his hypothesis about both light and matter displaying wave-like properties (10). Even though these theories gained in popularity, it wasn't until 1926 when G. N. Lewis coined the term "photon" for the particle displaying particle, and wave like properties (11). The event which sealed this new formalism in the scientific community, was performed in 1927 by Dirac - quantisation of light (12).

As the understanding of light as a phenomenon rose so did the ways of capturing it. Some of the most interesting examples of devices created to utilize the properties of light (specifically camera obscura) include its use to create paintings or its use by charlatans to convince the populous that they possess supernatural powers or had connection to gods (13). Evidences of these simple devices consisting of a darkened box with a tiny hole on one side and a screen that was either intentionally built or occurring naturally in cave systems were appearing as far back as the paleolithic era. The first written evidence of the camera obscura-like device appeared circa 470 BCE with it being more precisely described as a means of creating pictures in the before mentioned Ibn al-Haytham "Book of Optics" in the 1000 A.D. This little box, continued to be used all the way to the advent of photography, when British inventor Thomas Wedgwood made the first documented attempt to produce a picture with it combining it with a photosensitive material. This process was then greatly improved upon by Louis Daguerre and proceeded an era of photography.

Great advancement on the way light is detected especially for the dim light (that led to creation of apparatus more similar to what we are used to in modern times) came from an unlikely marriage of discovery of an effect of electron multiplication in vacuum tubes, photons generating and aiding electron generation, and a great drive to realize

the theoretical concept of a fully electronic television system.
The effect that for the first time allowed for the transformation of light into an electric signal was first demonstrated in 1887 by Heinrich Hertz where, via experimentation, he observed that a presence of UV radiation increased the electric response in his setup. In 1899 an effect in which electrons while in the vacuum tube striking an electrode would cause emission of additional electrons was presented by Paul Ulrich Villard and dubbed a secondary emission. Explanation of this mysterious photoelectric effect, was what granted Einstein his Nobel prize in 1921.

The modern television on the other hand was made possible thanks to the ideas and experiments on deflecting, modulating and accelerating cathode (electron) rays that were performed by an English physicist J. J. Thomson. In 1897 Ferdinand Braun was able to create the first phosphor-coated screen and thus a CRT screen was born. Experiments in 1907 by Boris Rosing where he used CRT as a mean of receiving and displaying an image, led to publication of a Nature paper in 1908 where Alan Archibald Campbell-Swinton theorized on the possibility of using this to create a fully electronic television. Two decades of intensive research have led to the creation of Iconoscope that was the first practical photo detector that was then used in the creation of television cameras. But most importantly it also resulted in great advancements in the creation of vacuum tubes and systems for the purposes of accelerating electrons.

A combination of these advancements led to the development of photomultiplier tubes. In 1934 the first device combining a photoelectric-effect cathode with a secondary emission amplification stage encompassed in a vacuum tube was presented by Harrison, NJ. Harley Iams and Bernard Salzberg. Even though displaying only an eight fold gain of the current, this was a monumental discovery that sparked research on the creation of devices capable of achieving much higher gains and detecting ever smaller amounts of light down to a single quanta of light-photon.

With that the interest in single photon detection and understanding of its potential benefits rose steadily. Increased investments from government and private sector have lead to a significant improvements to the existing technologies making them more viable for the bread market and out of lab applications.

1.2 Light detection in IR

In the recent years there has been a significant growth in the interest of implementing quantum technology based systems into market ready applications. This interest was explicitly shown by a UK government that announced in 2013 an investment of £270 million for a National Quantum Technologies Programme, over five years, to accelerate implementation of quantum technologies into private sector and military applications. A large part of that programme was directed towards sensing and single photon applications. Such detectors could then be used for many applications, for example quantum key distribution, time-correlated photon counting, Light Detection And Ranging (LIDAR) within the remote gas sensing and smart phone industry. This is especially true for the LIDAR technologies with specific applications in autonomous vehicles for both public and military applications. With over US$800 million being invested in LIDAR companies over past two years and expected growth of the market to a value of US$28 billion within the automotive sector until 2032 (as stated by the Yole development) there is a clear marked demand for such technologies. However, there has been a significant lack of technologies, that would cover a demand for low cost, robust, eye safe, short-wave infrared region (SWIR) sensitive devices for potential use in LIDAR systems. There have been some developments from companies like Velodyne and Innoviz but their technologies are only capable of operating at around 905nm and 940nm. This leaves a huge window of opportunity for technologies capable of producing devices operating at wavelengths between 1310nm and 1550nm which would be more suitable for the LIDAR applications in addition to quantum communications and range finding. The wavelengths between 1310nm and 1550nm are of interest due to the capability of low loss optical fiber light transport at these wavelengths in addition to a fact that operating at wavelengths close to 1550nm would provide the best achievable atmospheric penetration length in various hostile environmental conditions, including rain, snow, fog, smoke (1), haze (2) and considerably reduced snow spectral albedo (14). It is especially important to take into account rainy conditions when considering autonomous/automotive vehicle applications. To do so rain droplets can be approximated as perfect spheres and the Mie solution (which describes the scattering of an electromagnetic plane wave by a homogeneous sphere) can be utilized to solve the Maxwell equation. As was presented in the (15), the minimum of the scattering

for the average rain droplet size has a minimum around 1600nm allowing for the best measurement lengths for the LIDAR systems. Another important factor to be taken into account is the Solar radiation that would act as a background signal introducing noise into the measurement. Luckily this background noise (although still present) has a significantly reduced value at around 1550nm wavelength (16). The final thing to consider is eye safety, particularly if these systems are to be used in the public space. Since LIDAR utilizes a laser as a source of light for it to be allowed for the public use, its power and wavelength should be within the eye safety norms as presented in IEC-60825-1 standard where for the wavelenghts between 1400nm and 1550nm maximum permissible exposure (MPE) at the cornea for direct exposure to laser radiation is $10^3 Jm^{-2}$ for times less than 0.35s. The human eye, since being mostly comprised of water, heavily absorbs incoming light at these wavelengths and although it would cause a slight increase in the eye temperature, this would not cause permanent damage (as shown in the IEC-60825-1 standard). The eye-safe wavelengths prevent more problematic interactions from occurring with the more light-sensitive retina, that could cause significant damage to it if it wasn't for most of the incoming radiation being absorbed in the vitreous humor. This absorbing effect is so strong for the 1550nm wavelength that the power of the laser used in such systems could be increased by a factor of 20 over visible wavelengths, significantly increasing with it the signal to noise ratio and allowing the laser to operate at much better capacity.

With all these advantages it is no surprise, that single photon detection at wavelengths between 1310nm and 1550nm is a technology that is highly sought after. The most commonly used devices are based on Silicon complementary metal oxide semiconductor technology (Si - CMOS) Single Photon Avalanche Detectors (SPAD) which provide the advantage of being cheap to produce on large scale and being readily available on the market. However they are only capable of operating at the visible wavelength range up to 940nm. At this wavelength there is a strong absorption due to the atmospheric conditions, significantly reducing possible range of detection. The SPAD devices can be utilized for the LIDAR systems using the photon time of flight method for the ranging purposes (17). With the single photon detection efficiencies below 10%, which is a relatively low value if these devices were to be used reliably, that

makes them not viable option for LIDAR implementation for autonomous vehicles.

The two other major technologies that operate at 1310nm and 1550nm wavelengths are : superconducting nanowires and InGaAs/InP SPAD, with a third emergent technology (presented in this thesis) Ge on Si SPAD.

1.2.1 Superconducting nanowire single photon detector

A superconducting nanowire single photon detector (SNSPD) is defined as structure that possess width and thickness of size tens of nanometers or less and an unconstrained longitudinal size cooled down to temperatures below the temperatures required for the superconductivity to occur and typically around 4K (18). While in the mode of operation, SNSPDs are being biased just below a critical current density of the nanowire. The working principle of such a device is presented in Fig.1.1. Firstly, the incoming

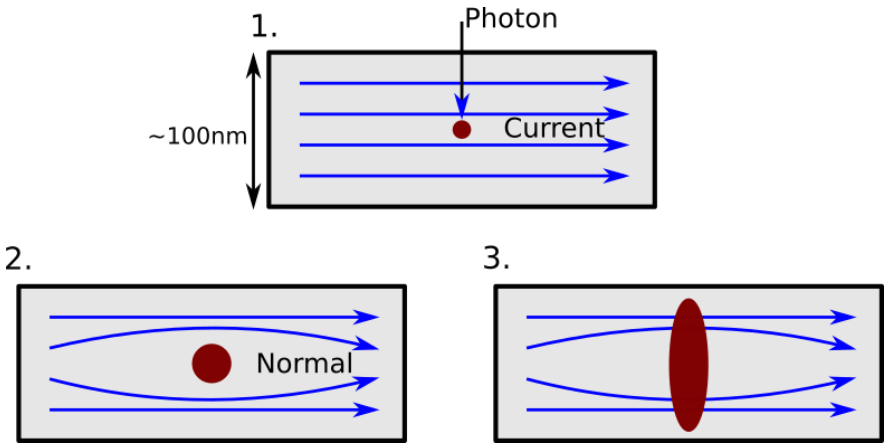

Figure 1.1: Diagram depicting process of Single photon detection in a nanowire.

photon is being absorbed by the nanowire which causes breakage of the Cooper Pairs (which are responsible for the superconductivity) at the point of the photon absorption 1.1 1). This leads to this area starting to exhibit a finite resistance. This in turn leads to the current flowing around that point as presented in 1.1 2). Increased current flow at this small area is effectively equal to the local increase of the current densities around the resistant spot. This increased current leads to the current in these regions 1.1 3) exceeding the critical current bias which results in the whole nanowire entering a

normal resistance mode. With this increase a measurable spike in voltage occurs that is high enough for the confirmation of photon absorption. The reported single photon detection efficiencies for devices working on this basic principle are 93% for 1550nm (19) and 75% for 1310nm (20) with low dark count rates and small jitter. They also do not exhibit afterpulsing effects, although they can stagger causing the device to stay in the normal resistance mode, with a necessity to reduce current flow to bring the device back to the initial state. The performance achieved by the SNSPD is the most impressive out of all of the single photon detectors, sadly they are not suitable for mass consumer applications. The very demanding and costly fabrication process combined with required readout apparatus and the necessity to operate them at temperatures of a few Kelvins, raising operation costs above all other factors, inhibit their suitability for mass production of a small size, robust and, most importantly, cheap device of this type.

1.2.2 P-I-N photodiode

The next type of devices that are capable of single photon detection at SWIR wavelengths are Single Photon Avalanche Detectors (SPAD). Before we investigate specific architectures for this design, the general ideas behind their working principals we will presented. To understand the mode of operation for this kind of design a basic introduction to the physics behind the p-n diode, its more complicated form in the p-i-n diode and the working principles of the avalanche process. This will relate to the devices based on ideas like InGaAs and presented in this thesis Ge-on-Si SPAD.

A p-n semiconductor diode is created by joining a layer of p-type semiconductor, with a layer of n-type, where p and n type are extrinsic semiconductors that are doped with electron acceptor atoms and electron donor atoms which respectively share their electrons and accept electrons with and from the crystalline lattice. The two layers can be described with their acceptor (N_a) and donor (N_d) concentrations for p and n respectively. For a better understanding of the effects taking place inside of the diode it is important however to consider their states before the connection and general concept of a Fermi level. In the broadest sense Fermi level is a value determining the electrical properties of the medium. In more detail, it corresponds to the assumed electron energy level, which at the thermodynamic equilibrium would have a 50% chance of

being occupied. In the p- type semiconductor, introduction of the acceptor impurities creates hole levels (virtual empty states above the valence band) in the band gap. With these empty states present, electrons can be easily excited from the valence band to occupy some of them. This leaves a virtual positive particle (hole) in the valence band, that can participate in charge movement. Let's consider initially a case where no voltage is applied to the junction and there is no associated current flow. This state is known as the state of thermal equilibrium.

$$J_{n,p} = 0 = \mu_{n,p} n, p \frac{dE_F}{dx} \tag{1.1}$$

Therefore, from the requirement of no hole or electron drift in the state of equilibrium one can see that the Energy at which the Fermi level is located should remain constant across the area of the device. In this type of semiconductor the holes are known as the majority carriers, as they are accommodating charge movement. In the case of the n type semiconductor the situation is similar, but the donor states are located just below the conduction band. Electrons located there, if given enough energy from the applied voltage can be promoted to the conduction band and participate in the charge movement. In the n-type semiconductor, electrons are the majority carriers and the Fermi level is located in the valence band between the donor level and the conduction band. Both of these cases are presented in the Fig.1.2 1) and Fig.1.2 2) .

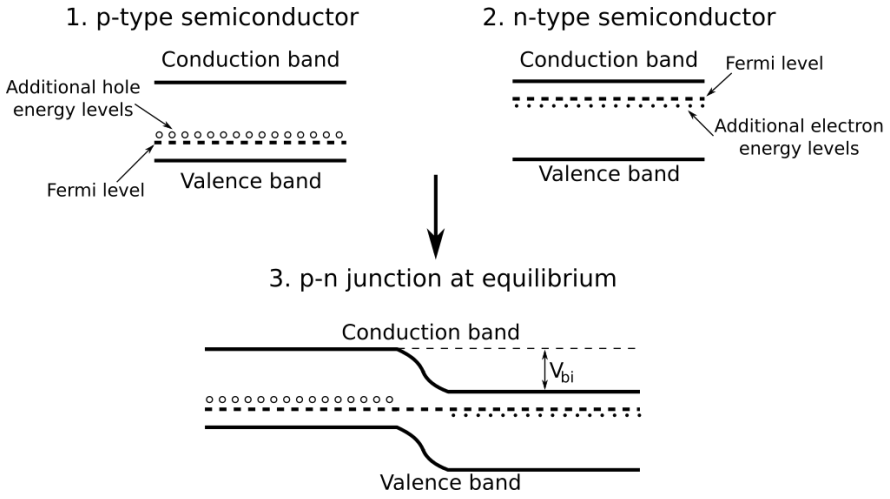

Figure 1.2: Diagram depicting p and n type semiconductors energy bands on their own and after connecting to create p-n junction.

After making the connection, in order to accommodate the correct positioning of the electron and hole states (and more precisely to ensure that in equilibrium state the drift-diffusion current has a spatially continuous Fermi level), the Fermi level has to stay constant. But since the Fermi level is located at different places in p and n type semiconductor, to maintain its flatness requirement in the equilibrium, the band bending must occur at the interface of the two semiconductors. The contact potential of these bend bands can be expressed with equation:

$$V_{bi} = \frac{k_b T}{q} ln \left(\frac{N_a N_d}{n_i^2} \right) \tag{1.2}$$

where k_b is the Boltzmann constant, T is the temperature, q is the magnitude of the electrical charge of an electron, N_a is the doping concentration in the p-type region,N_d is the doping concentration in the n-type region and n_i is the intrinsic carrier concentration. In the equilibrium state because of the strong difference of doping concentrations, some of the free electrons from the n-type region which have reached the conduction band would drift into the p-type region to recombine with the holes present near the interface. This process can be understood in respect to the p-type semiconductor, as virtual hole particles drifting to the n-type to recombine with the electrons located near their interface. Therefore, near the interface negative charged ions in the p-type are being created from filling the vacancies in it. In the n-type positive charged ions are being created from electrons leaving positively charged hole as they diffuse to p-type . This process leads to the creation (at the interface) of a charged region (depletion region) that results in an electric field gradient in that region. In the equilibrium state, Coulomb force prevents additional electrons from migrating from n-type to p-type.

Firstly let's consider situations in which either a positive or a negative bias (V_f, V_r) is applied onto the p-n junction. The first case of positive bias being applied (positive on the p-side and negative on the n-side). This applied voltage results in the separation between bulk Fermi levels in p and n semiconductors which results in the step between band levels within the p-n junction to be reduced by the applied voltage $(V_{bi} - V_f)$. This forward applied voltage assists the electrons to cross through the Coulomb that was preventing them from movement in the case of equilibrium. These electrons can then flow in the direction indicated by the field with little resistance therefore carrying

out current conduction.

Let's consider the case of reverse bias being applied (negative on the p-side and positive on the n-side). While this is still true that in bulk, the Fermi level remains appropriate for a given semiconductor, in this case the potential step in the band between the p and n gets increased by the value of the applied field ($V_{bi} + V_r$). Additionally, the applied field would interact with the holes and electrons in the depletion regions for the p- and n-type semiconductors respectively, causing them to be attracted and move away from their current position near the junction region, therefore leading to the creation of wider spread areas of negative and positive regions translating to the widening of the of the depletion region on both p-side and n-side. This leads to an effective increase of the resistivity of the junction. However, there is a small amount of current that still flows through the junction due to two mechanisms. This current is called a reverse current or leakage current and is important to consider as it is a main contributor to the dark current that negatively contributes to a performance of the photo detector(21). This will be considered while discussing avalanche photo-diodes in the following section. There will be a small thermal generation of electron-hole pairs inside the depletion layer, these carriers will be separated by an internal field and drift towards the neutral regions, therefore creating a small current flow. Another mechanism supporting a small current density is related to the diffusion lengths of the holes and electrons on the distance of the junction being described by the equation:

$$J_s = q\left(\frac{D_e}{L_e N_a} + \frac{D_h}{L_h N_d}\right) n_i^2 \tag{1.3}$$

where the D_e is a diffusion coefficient for the electrons, and D_h is the diffusion coefficient for the holes.

Other components that contribute to a reverse current (leakage current) including tunneling effects and components from the potential surface leakage paths. However these mechanism extend past the basic mechanisms of the p-n diode and therefore will not be discussed here.

A diode like the one presented above would be capable of the detection of incoming photons, assuming that their energy is above the energy of the bandgap. This causes

the electron to be promoted from the valence band into the conduction band leaving an unoccupied positive charge in the valence band (hole) creating an electron-hole pair (EHP). The electric field present in the depletion region causes the EHP to drift towards the neutral regions of the p and n semiconductor, giving rise to the photo generated current. The generation rate of these EHP pairs can be expressed as:

$$G = \frac{\alpha P_{inc}}{Ah\nu} \tag{1.4}$$

where α is the absorption coefficient of the material that makes up the diode, P_{inc} is the incoming optical power, A is the area of the junction and $h\nu$ is an energy of the photon. With the generation rate at hand, one can express the overall photo current as:

$$I_{photo} = q\frac{(1-R)P_{inc}}{h\nu}\left(1 - e^{-\alpha W}\right) \tag{1.5}$$

where R is the reflectivity at the surface of the semiconductor and W is the width of depletion region. This equation is accurate for the depletion region. Photons absorbed in the neutral regions of the p-n diode would lead to the creation of current as well, although this process is much smaller than the one occurring at the junction due to recombination and will be therefore omitted.

Although photodetection can happen in the p-n type diode, the fact that it would happen predominantly in the small region in the p-n junction, as the photons absorbed in the neutral region give a much smaller response, it does not make them a good candidate for direct radiation detection applications. Additionally, the diffusion based electric transport, which is a slow process, results in the whole photo response of the p-n diode to be slow.

As an alternative to this a p-i-n type diode, where the regions of the p -type and the n-type heavily doped semiconductor are spaced by an intrinsic undoped spacer. A general overview of such a device with an avalanche capability (which will be explained later in this chapter) is presented in Fig.1.3.

In a p-i-n type of device, the addition of the i-layer results in an increased area of the depletion region, therefore increasing the overall absorption region for photo detection. The detection levels are also enhanced in this region due to its relatively

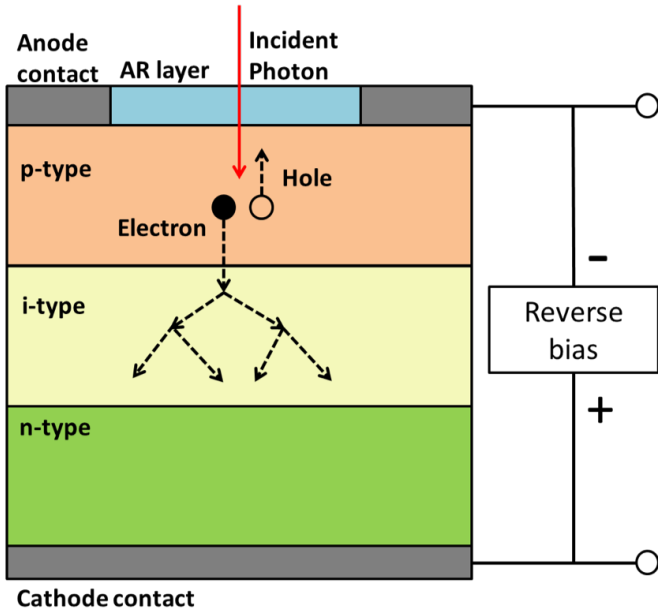

Figure 1.3: Diagram depicting a p-i-n photodiode fabricated to operate as a single photon avalanche detector.

low doping (22). Due to the electrons and holes merging in the i-region, this region contains no carriers, therefore exhibiting insulator-like high resistivity that causes the entire voltage drop to happen on that layer. This promotes the creation of a high field in the i-layer that is beneficial for the photo detection. Additionally this structure can be created in a way where the i-layer is much thicker than the p-layer and additional n-layer . This would make it more viable to compare to the p-n diode, as in this case the the charge mobility would be accommodated by a much faster drift component.

1.2.3 Avalanche diode

An avalanche photo diode is a specific type of photo detector that utilizes a similar design to a p-i-n diode but with a significant improvement for the photon detection coming from the internal gain mechanism based on the impact ionization by electrons (23). This in turn provides with a strong, easy to register output signal. Devices of this type were first investigated and created by R. H. Haitz and his associates in the 1960's (24) (25) who for the first time observed their capability to detect single photons. In order for the carrier multiplication to take place a photo generated charge carrier must

enter a high field region in which it would be sped up and gain kinetic energy. After it reaches sufficient levels of energy there is a finite probability of it impacting another electron in the valence band with the impact providing enough energy to promote it into the conduction band. This leaves a positively charged hole in the valence band and two electrons (the original one and the newly ionized one) being sped up in the electric field. After these two electrons reach sufficient energy they can both partake in the impact ionization process, promoting even more electrons to the conduction band. The sequence of events continues with the number of electrons greatly increasing with each iteration. This process is called an avalanche effect and can be observed in the Fig.1.3. While traveling through the avalanche region, in addition to ionization, electrons can interact with the phonons (virtual particles representing vibration of the crystalline lattice) either by gaining some energy (phonon absorption) or by losing some energy to lattice vibrations (phonon emission).

The way to quantify the impact ionization can be achieved with the usage of impact ionization coefficients α_p and α_n for holes and electrons respectively (26). These coefficients describe the number of new EHP per unit distance traveled by the given solitary carrier between collisions and can be defined as:

$$\alpha_{p,n} = \frac{1}{nv_{p,n}} \frac{d(p,n)}{dt} \tag{1.6}$$

where $v_{p,n}$ is the velocity of the carrier, n is the concentration of carriers and $d(p,n)/dt$ is the carrier generation rate. In general, the coefficients increase with the field applied, as higher values of the electric field would cause the carriers to travel at greater speeds. This allows for the carrier to undergo impact ionization at a shorter travel distance. To fully utilize the avalanche process, the SPAD is operated at voltages just below the breakdown and taken above it with the application of the timed gate. This allows for much higher efficiency of photon detection as compared to the basic p-i-n diodes as every absorbed photon that creates EHP leads to a greater multiplication of the carriers, whereas in the non-avalanche design it remains as a singular carrier. This mode of operation (with the applied gate) is called a Geiger mode as it bares resemblance to the Geiger-Muller type devices (27). However, due to the stochastic nature of the multiplication of EHP in the avalanche process there is a large variation in the resulting amount of ionized electrons therefore resulting in varying values of the current being

generated for the same input which results in an increased measurement noise in the devices (28).

A figure of merit that describes the general APD performance according to the local field model is an intrinsic material parameter κ such that when $\alpha_p < \alpha_n$ parameter $\kappa = \alpha_p/\alpha_n$ and for $\alpha_n < \alpha_p$ parameter $\kappa = \alpha_n/\alpha_p$. This parameter is tied with the excess noise factor F(M)through the equation:

$$F(M) = \kappa M + (1 - \kappa)\left(2 - \frac{1}{M}\right) \tag{1.7}$$

where M is an avalanche ionization gain expressed as

$$M = \frac{i_{photo} - i_{dark}}{i_{primary,photo} - i_{primary,dark}} \tag{1.8}$$

where i_{photo} is a multiplied photo current, i_{dark} is a multiplied dark current, $i_{primary,photo}$ is a photo current generated in the device before the multiplication occurs and $i_{primary,dark}$ is a dark photo current generated prior to the avalanche process.

The value of κ approaches 1 as the field across the device is increased. With that, the requirement arises that for a thinner multiplication layer an increase in the electric field applied would be necessary, to achieve the same gain value as for the devices with thicker multiplication layers. However, an opposite relation has been observed in the experiment (29). This discrepancy could be explained when taking into account the behaviour of an electron before it creates other impact ionized carrier. As stated earlier, either when the carrier is just generated by absorption of a photon or by being promoted to the conduction band by a highly energetic electron traveling through the multiplication region, it begins to be accelerated by the field as it does not have sufficient energy itself to immediately cause another electron to become impact ionized. Initially it has to travel for some distance in the multiplication layer while being sped up by the electric field to achieve high enough energy, to be able to participate in the impact ionization. The amount of semiconductor traveled while the electron gains sufficient energy is called the dead space (30). It stands to reason that for the devices with a different thicknesses of the multiplication region, the overall dead space distance contribution (which is dependent on the voltage applied), would be a larger contributing factor for the devices with thinner multiplication layers. This is especially

true for the devices with multiplication layers of thicknesses comparable to the dead space distance. This dead space influence on the thin devices would in turn result in the multiplication process to be more deterministic, as the actual avalanche would only be possible at the part of the device at which electrons reach energy levels high enough to participate in the impact ionization. With the number of electrons participating and being created in the avalanche ionization events being kept more consistent, the excess noise resulting from the stochastic nature of that process gets reduced (31). Therefore, a thinner multiplication layer would be advisable in order to be able to manufacture devices performing with lower noise levels.

Lastly, since the traveling carrier can interact with phonons in the semiconductor it stands to reason that the overall temperature at which the APD device operates would influence its performance (21). With an increasing temperature the lattice would possess a higher vibrational energy. This energy could either be partially transferred to the free electron, increasing its energy by the process of phonon absorption, or more likely it would result in part of the electron energy being transferred to the lattice in the phonon creation process. Another possible outcome is for the lattice to provide carrier with enough energy to promote it into the conduction band, therefore creating a free electron that could potentially trigger an avalanche event. When the APD acts as if it absorbed an incoming photon, but the avalanche is coming from a carrier promoted to a conduction band by some other means is called a dark count. In contrast, for the case of low temperature of measurement, the crystalline lattice of a semiconductor would possess less energy, meaning less vibrations and less interaction with phonons by carriers. Since the α_p, α_n are exhibiting a temperature dependency, the breakdown voltage of the APD should also be dependent on temperature (32) in a correlation represented by the equation:

$$\Delta V_{BD} = \gamma \Delta T V_{BD,RT} \tag{1.9}$$

where γ is a coefficient tied to the material of the APD, ΔT is the temperature change and $V_{BD,RT}$ is a breakdown voltage at the room temperature. This dependency was also observed empirically in this thesis and is presented in the Fig.5.12.

As mentioned previously, especially in the cases of high temperature, some of the carriers that can start the avalanche event can come from other sources than photon absorption. These mainly originate either in the bulk of the semiconductor, as random thermally generated carriers or from the lattice defects that can act as traps for charges that when released in the device operation mode can start the avalanche process as they would follow the same kinetic energy increase by field and impact ionization principles as their photo generated counterparts. The dark current consisting of carries with such origins is referred to as a bulk dark current and the square mean value of it can be expressed as:

$$\langle i_{DB} \rangle = 2qI_D M^2 F(M) B \tag{1.10}$$

where I_D is the non-multiplied current in the device and B is the operation bandwidth. Another component of the total dark current arises from the interaction with the surface. In real applications there will always be a need for an exposed surface, either by the etch to define its area or just as a top surface. When there is a breakage in the lattice due to the existence of the exposed surface, bonds that in the normal condition would be connected to the next crystalline lattice are left dangling, not passivated. They will either connect to one another recombining the surface or they will connect to appropriate chemical elements in their surroundings to try to achieve an energetic minimum. That process however is heavily random if left to its own devices and results in the creation of a poor quality surface that can either possess trapping centers as in the case of device bulk or create leakage paths-energetically preferential routes for the carrier that exclude them from the avalanche process inside the semiconductor by being directly swept to the contact. With that, the surface of the device also contributes as well to the dark current as:

$$\langle i_{DS} \rangle = 2qI_L B \tag{1.11}$$

where I_L is the surface leakage current.

However, even though dark currents can be a serious detriment to the device's performance, the SPAD ability to create an enormous multiplication of the photon-generated carrier, makes it a more viable structure than a regular p-i-n diode.

1.2.4 Separate absorption, charge and multiplication

Separate absorption, charge and multiplication (SACM) type architecture, refers to a range of modified p-i-n type structures where every layer is performing a separate function. This provides more precise control over parameter for each layer (33) (34) (35). As the name suggests, the absorption layer is the layer where photon absorption occurs, the multiplication layer accommodates the avalanche multiplication process and the charge layer is a doped region that is responsible for precise control of the electric field levels in the previous two layers. For the purposes of radiation detection, usage of a semiconductor with a narrower band gap than the multiplication region is required in order for the radiation to be absorbed

. To enable a carrier multiplication a semiconductor with a wider band gap is more desirable in order to decrease the multiplication noise. The values of the electric field in the absorber correspond to its internal performance and have to be carefully designed to be at a high enough level so that the photo generated carriers are given enough energy to be transported into the multiplication region. Alternatively, the value of electric field has to be kept at a low enough level so as not to promote random carrier generations and be kept below values that would cause an avalanche breakdown in this layer. However, the multiplication layer must be above the breakdown voltage to accommodate carrier multiplication but not too high so as not to promote multiplication noise. A doped charge sheet is placed between these two layers to allow control of the field. The appropriate values for the charge sheet are investigated in more detail in the Simulation chapter 4.

In addition to the value of the electric field, the geometry of a SACM device (including the thicknesses of the absorption and the multiplication regions), would influence the overall performance of the device (35) (36).
Two types of devices that follow the SACM type of device are Ge-on-Si SPADs (that are the main focus of this thesis) and InGaAs (37) (38) devices. The InGaAs/InP devices are biggest competitor to our technology. They have been investigated and improved upon in the recent years, providing transferrable knowledge on how to adapt SACM structures into Ge-on-Si platform (4).

1.3 Competing technologies

In this section some technologies which directly compete with the devices proposed in this thesis due to their similar applications will be discussed.

Firstly, Si SPAD devices are considered. Even though these do not comply to the operating wavelength requirements it would be easy and cheap to manufacture on a mass scale (39) with the use of "IMG175" technology node (40) which is a European Union set of requirements for the emitters to be considered eye-safe. Current Si SPAD device design is presented in (41) (42) (43). the are made utilizing 40nm technology with a filing factor $> 70\%$ and all the logic implemented on a dedicated layer. Although impressive as an achievement on its own these devices, however, are incapable of light detection at longer wavelengths. The single photon detection efficiency drops to $< 10\%$ at about 940nm and steadily declines at longer wavelengths. This is no surprise since the absorption coefficient of Si, which is used for photon detection in these devices, begins to decline at a wavelength of about 1000nm.

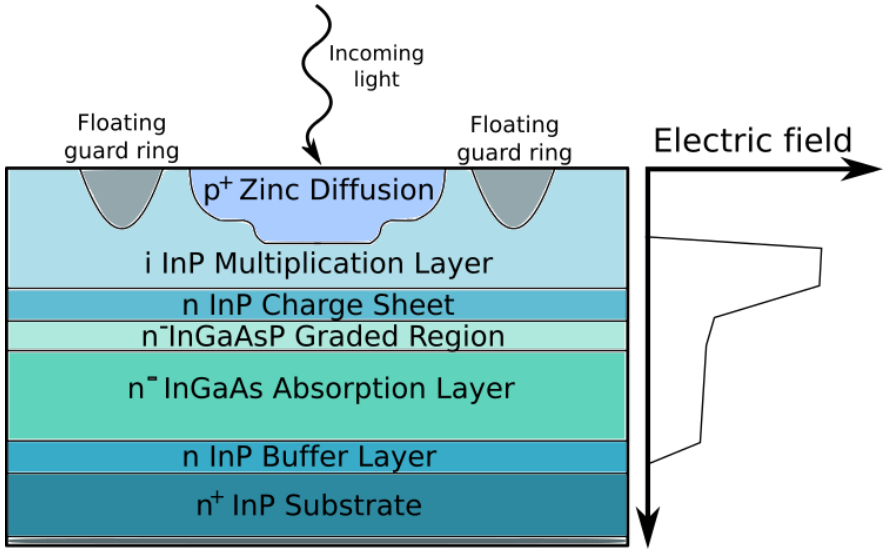

Figure 1.4: Diagram depicting InGaAs/InP based single photon avalanche detector with an explanatory graph showing electric field profile in the device.

At present, only devices that are commercially available and can be used for an out of lab single photon detection purposes (at desired wavelengths) are SPADS based on

the InGaAs/InP architecture. There has been a significant push towards the development of these devices ever since it was shown in the 1970's that they could potentially be of high performance and low jitter while being able to register light wavelengths between 1000nm and 1550nm (44) (45) (46). Devices of this type, as well as the devices presented in this thesis, are based on the SACM structure. This type of structure for the InGaAs/InP structures is presented in Fig.1.4. InGaAs in this structure acts as an absorption layer for incoming radiation, with its small energy gap providing good detection efficiency, and where the high energy gap i-InP is acting as a multiplication layer and the n-InP as a charge sheet layer. This charge sheet layer provides control over the electric field distribution between the i-inP and the InGaAs layer. The field is sufficiently high to allow for an avalanche event to happen in the i-InP, and low enough in the InGaAs absorption layer to prevent excess carriers tunneling and triggering the dark counts. Additionally, an InP buffer layer is deployed between InGaAs and the substrate to reduce discontinuity in the band structures at the interface of the two layers. This in turn reduces the carrier trapping, the release of which could later contribute to an increased dark current. As an additional means of field control inside of the device a p+ Zinc diffusion region with floating guard rings at the periphery is incorporated allowing for a better confined diffusion region inside the device (33) (47) (48). The active area of such a device can also be defined by utilizing an etched mesa structure (49) (50). However this architecture is not very popular as the discontinuity introduced to the semiconductor structure at the device side wall could potentially lead to the creation of surface trap states.

InGaAs/InP SPAD pose a good candidate for LIDAR applications, these were shown to achieve high values of SPDE of about 25% and were utilized recently for LIDAR depth profiling purposes with high quality results at kilometer-scale ranges(51) (52). To achieve low dark count rates however they must be operated at low temperatures. This is required to reduce the dark count rates that the device experiences. It is important as well to consider the high costs of materials and fabrication of these devices , coupled with low fabrication yield that make them a poor choice for mass scale applications. However this is still a leading technology especially since it is commercially available as an off the shelve component from providers like Princeton Lightwave and ID Quantique priced at about £20k per pixel. Another big drawback of this technology is that it is covered by International Traffic in Arms Regulations (ITAR) regulatory

regime. ITAR is a set of rules, regulations and restrictions issued by the United States government that are designed to restrict the export and usage of military and defense related technologies to protect the interests, security and military dominance of the United States of America. These rules are far reaching and encompass any components that have potential military uses, with LIDAR capable technologies having a high potential for military ranging purposes. Under these rules the United Kingdom military would be forbidden from using InGaAs/InP technology as a component in a larger ranging system. This also affects the public sector as InGaAs/InP devices, even if used in civilian semi autonomous vehicles, would fall under the same embargo since the technology only needs to possess a potential usage for military and defense purposes to be put restricted by ITAR.

To address the issues with the above mentioned technologies, SPAD devices based on Ge-on-Si architecture are being pursued with the first instance of such device that would be able to perform in the single photon regime at 1210nm wavelength being reported in 2002 by Loudon et al. (53) where the detection was performed utilizing Ge/Si quantum wells. However, performance of this device was limited by low quality fabrication and a lack of techniques available for the growth of thicker layers of Ge on top of the Si layer. This prove-of-concept device created greater interest in the following decade in the possibilities of this type of a structure and the development of more advanced Ge on Si epitaxial growth techniques allowing for thicker Ge layers. Progress has been marked by Kang et al. (54) DeRose et al. (55) and Martinez et al.(56) who have developed better quality and CMOS compatible structures for the new era of Ge-on-Si photodetectors, culminating in a high performing Ge-on-Si SPAD operating in Geiger mode presented by Warburton et al. (4) which was used as a starting point for the devices developed throughout the course of this research. However, even with better quality growth methods available, current Ge-on-Si SPAD devices were still not able to reach the levels of detection efficiencies comparable to these achievable in the InGaAs/InP architecture. This is due to different challenges posed by these structures. One of these challenges is related to the different lattice constants of Germanium and Silicon (with Ge having the lattice constant of 5.658 A and Si having a lattice constant of 5.431 A). During the Ge on Si growth, due to Ge possessing larger lattice constance, it experiences compressive strain at the interface

with Si. This strain causes an appearance of discontinuities in the crystalline lattice of Ge. These dislocations can then act as trapping centers for generated carriers. This in turn can lead to decreased photon detection efficiency if a photo generated carriers were to be trapped at the Ge and Si interface and not initiate an avalanche multiplication process. As stated earlier the charge sheet is crucial in the SACM type structures as it allows for the control of the electric field distributions in the absorption and multiplication regions. However, this is more difficult to achieve, as the values of electric field at which the tunneling current in Ge would be greatly reduced are less precisely known than in InGaAs/InP (35). As a rule of thumb however, it is reasonable to aim for the electric field value in Si to be around 300kV/cm and for the Ge of about 100kV/cm allowing for high electric field in Si accommodating multiplication while the lower electric field in Ge provides photogenerated carriers with enough energy to cross into the Si layer while not significantly increasing the tunneling current. Appropriate values for the charge sheet doping concentration (N) that would produce the required fields can be achieved by solving the Poisson equation:

$$\frac{dE}{dx} = \frac{qN}{\epsilon_{Si}\epsilon_0} \tag{1.12}$$

which would be dependent on the thickness of the Si multiplication region. Results of these numerical calculations are presented in the Simulations chapter 4 of this thesis. Performance of the devices is also dependent on the Ge thickness and growing a thick layers of Ge on Si without increased dislocations is a technology that is not very well established. Another challenge is posed by the Ge-on-Si devices being predominantly developed to be normal incidence radiation mesa structures. This architecture choice is necessary as a means of defining an active area of the device but brings with it many challenges connected to the exposed side wall which can be detrimental to the performance of the device.

The previously published results (4) were based on the design where the active are was defined by the cylindrical mesa etch. As it was suspected at the time and confirmed in the course of this PhD project, this kind of design would display a high interaction of the electrical field of the active area with the side wall states. If the surface is not perfectly passivated, the dangling bonds could lead to creation of dark counts (due to the release of carriers from trap states) and potential leakage path alongside the mesa

surface (that would result in lack of multiplication of the absorbed photon). In this thesis I will present the first Ge-on-Si SPAD in the planar geometry which was fabricated to negate the issues with the side wall interaction.

The first high performance device with normal incidence radiation detection in the planar geometry with significantly increased performance will be presented in this thesis. Development of the fabrication processes are on par with novel design choices that allowed us to fabricate a device that not only outperforms any published to date Ge-on-Si type devices Tab.6.2 but also reaches efficiencies that make it a promising, low cost technology for the single photon detectors operating in the SWIR.

2

Methods and techniques

This chapter provides an overview of the fabrication methods used throught this thesis. The techniques explained herein are kept largely to be compatible with CMOS production line for Si and Ge processing because one of the main drivers of this project is the development of a device that can be cheaply and easily incorporated into existing industry lines for mass production. More specific fabrication steps for particular devices are covered in the Chapter 3 - Fabrication.

2.1 Facilities

The majority of the fabrication work through this PhD project was performed in the James Watt Nanofabrication Center (JWNC). The JWNC is a state of the art cleanroom facility spanning 1350m^2 with over £35M of nano fabrication tools which are used for the purposes of dry and wet etching, metalization, photo and e-beam lithography, and various metrology and imaging. This facility is run in a pseudo industrial operation regime, meaning that certain pieces of equipment that require specific safety and operational training as well as maintaining safety and cleanliness of the facilities is performed by specially selected 22 technicians and research technologists. Specifically, dry etch tools and atomic layer deposition tools are only run and maintained by qualified staff members, with the specific run parameters being designed and requested by users. This way it can be ensured that this important equipment can be properly maintained and nullifies risk of it becoming damaged by imperfectly trained users.

Fabrication at the nano scale is a very precise process requiring reliable and exact control over the environment properties inside the facilities. Therefore, the whole facility is under constant environment control, retaining precise values of pressure, humidity, and temperature thought the facility. It is also important to control the atmospheric composition inside not only for safety purposes, with gas detectors monitoring air composition, but with precise control of the airborne particles too. This is because the presence of large amounts of dust in the ambient environment would result in its deposition on top of the fabricated sample and would prevent manufacturing on the nano scales. To prevent that, clean room has as well monitored particle count which is reflected in the value of clean room class which reflects how many particles of diameter larger than $0.5\mu m$ would be present per cubic foot volume of the air. The JWNC facility has rooms with classes of 1000, 100 and 10. To additionally prevent contamination, the rooms in the JWNC are held at slightly higher pressure than the connecting corridors (which have lower class), preventing particles from traveling inside. Additionally to prevent the build up of dangerous airborne chemicals and dust contaminants the cleanroom has gas detectors and precise control of airborne particles, through a well monitored particle counter that tracks the presence of particles with a diameter greater than $0.5\mu m$ percent per cubic foot volume of air.

2.2 Cleaving

In this work, we begun with designing structure of the wafer, but to use it for device fabrication it is necessary to cleave it into smaller chips making it easier to handle with tweezers and in order to be able to utilize majority of the clean room dish ware. Size typically chosen for that is 1cm^2, which is small enough for the ease of managing, but provides sufficient amount of material for incorporating different structures on it. Since the required precision of the cleave and relative thickness of the substrate ($525\mu m$ of Si (001) wafer), cleaving has to be done with usage of the automated diamond saw. Wafer is first covered with a polymer in order to protect the sample surface from the airborne debris from sawing and wafer is glued on top of a sheet to maintain the positioning of separate chips after sawing. Various positioning marker are then located in order to precisely make the cut in the required places. After cleaving, separate chips were then

unglued from the sheet, and the polymer was removed from their surface.

Another type of cleaving that was necessary in this thesis is cleaving with diamond tip cleaver. At the end of processing, cheeps need to be connected for measurements to the header package which has a window for placing samples that is $3mm^2$. In order to be able to have a margin of error, samples have to be cleaved into chips of $2.8mm^2$ or smaller. To do so, sample is covered in polymer as for the wafer cleaving process, and moved to the diamond tipped hand cleaver. There, using the microscope and the guidelines on the sample surface, a cut is being made along the required line. This scratch however is only a surface damage and is not enough to cut the chip, therefore additional processing is required. Sample is then placed on top of a specially mounted thin bladed razor aligning (with a help of the microscope) scratched line with the razor blade and pinpoint pressure at the edges of the cut is applied by hand with a help of thin tipped lab tweezers. High eye hand coordination is required for this step, as wrongly applied scratch or pinpoint pressure can lead to the processed sample cracking in a hard to predict fashion, in most cases deeming it unusable.

2.3 Cleaning of Ge on Si samples

The standard cleaning procedure for Si wafers involves ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) which is commonly referred to as RCA1 clean and RCA2 clean which consists of Nitrogen tetrachloride NCL_4 and (H_2O_2). These cleans, however should be avoided with Ge present on the surface, as these chemicals can etch Ge at an significant rate (58). Whenever a Si surface clean is required it is recommended that a cyclic hydrofluoric acid (HF) and reverse osmosis (RO) H_2O clean be performed instead because it strips native oxide from from the Ge surface while leaving it temporarily hydrogen terminated.

After cleaving wafers into $1cm^2$ samples a main body of sample processing begins. In between of these processing steps, samples were cleaned for 5 minutes in acetone and then isopropyl alcohol (IPA) ultrasonic baths. These two chemicals were selected because acetone is good at removing organic residues (grease), and IPA acts mainly as a chemical to remove acetone from sample surface because drying acetone leaves residue on the sample surface. Typically an IPA clean is followed by a reverse osmosis water

(RO) rinse, but this was avoided for our samples because the water can potentially roughen the Ge surface by creating and removing the oxidized layer on top of it (59). Sample were then blow dried with a nitrogen blow gun. After nanofabrication steps were performed, ultrasonic agitation should not be used as it could lead to damaging more delicate structures on the sample surface. Instead a gentle rinse is recommended. If sample would require more of agitation, usage of a clean pipette to create a jet of liquid in the beaker would be advised.

2.4 Lithography

Lithography, originally meant process in which a pattern was transferred from a stone or a metal plate to obtain a print. In the modern times this definition relates to various processes in which a pattern in transferred into a medium, either with usage of a mask, or by a computer programmed pattern being written into a sample with a ray of electrons. Substrates onto which the pattern is transferred include various mediums with semiconductors being the most prominent ones. Instead of oil of fat as a transferring substance various organic compounds (photoresist) deposited on the sample surface are used as the intermediaries onto which a pattern from mask is transferred. Following an exposure either to UV or ionizing radiation photoresist changes its reactivity to the certain group of chemicals called developers allowing for parts of the photoresist to be selectively removed. This then can be followed either by an etch or metalization. Main two types of that process utilizing UV radiation (photolithography) and beam of electrons (e-beam lithography) are presented below.

2.4.1 Photolithography

Photolithography is a process that uses UV light to transfer patterns from a metal mask onto a sample. An overview of this process is shown in Fig.2.1. To achieve such light assisted transfer, a light sensitive polymer (called photoresist) is required. Photoresists react in a very specific way with the incoming light either cross-linking or breaking the cross-links in the polymer, making them way more or way less susceptible to interact with a counterpart group of chemicals known as developers. This photoresist can be then utilized as a masking material for an etch or for a metal lift off process that will

be explained in the later part of this chapter.

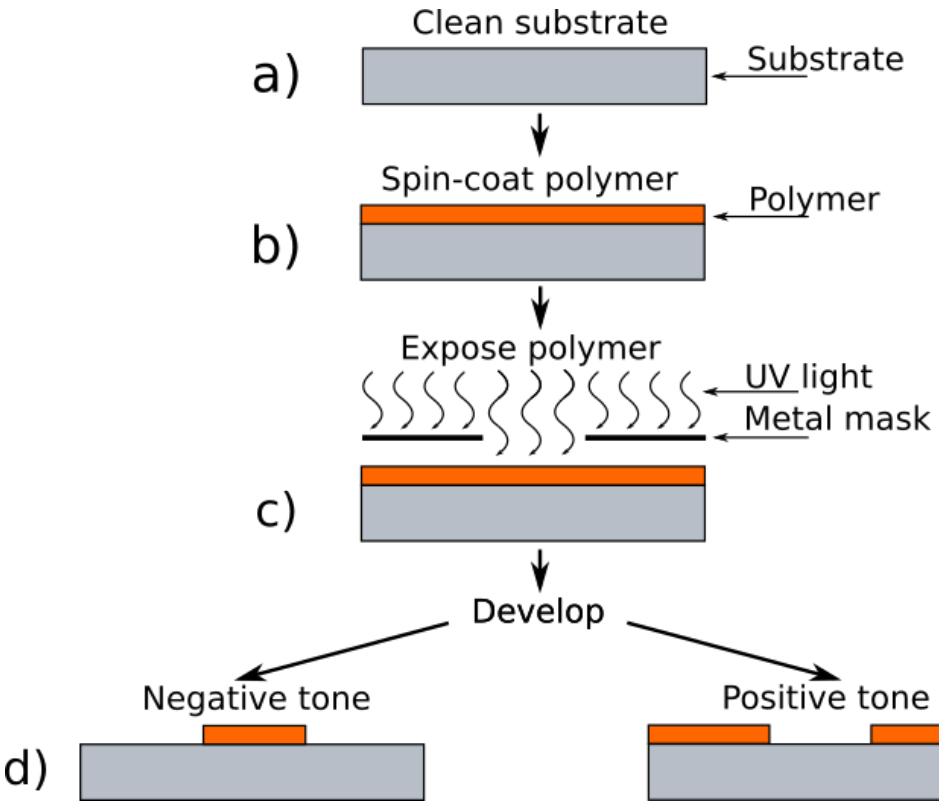

Figure 2.1: Diagram of a photolitography process for photoresist of negative and positive tone

Starting at the top of Fig.2.1 a) a cleaned surface is dehydration baked at $120°C$ in a convection oven for 10min in order to remove any moisture from the sample surface, which promotes the adhesion of photoresist. Once cooled the sample is placed on a spinner and a photoresist is spun on the surface Fig.2.1 b).

All the spinning jobs are confined in a specifically designated room for two reasons: (1) to prevent contamination at this crucial step by moving processing into the room with lower particle count and (2) to reduce exposure to the photoresist as it has a strongly negative influence on the human body increasing probability of decreased fertility and spontaneous abortion (60). The spinning cabinets have a vacuum capable chucks with programmable control of spin parameters. The rotational spin speed,

ramp speed, overall time of the spin, deceleration speed are programmed depending on the resist used. One of the most standard recipes used during processing of samples presented in this thesis is a recipe for spinning Shipley Microposit S1818 photoresist, which requires a spin of 4000rpm for 30s. This results in the final resist thickness on top of the substrate of $1.8\mu m$. The resulting resist thickness can be as well calculated before-hand utilizing following equation:

$$t = \frac{kp^2}{\sqrt{w}} \tag{2.1}$$

where t is the resulting thickness, k is the spinner constant, p is the resist solid content in percent, and w is the rotational spinner speed.

After the spin, a soft bake is performed to evaporate the solvent in the resist and prepare it for exposure. For S1818 photoresist, this is done on the hotplate set for the $120°C$ for 2min. It is important to note that this hotplate is placed under the fume extraction unit as evaporated solvent has a negative impact on health too.

The next step of the photolithography process, presented in Fig.2.1 c), is the exposure step, where the pattern transfer into the photoresist happens, using a Karl Suss Microtech MA6 mask aligner/exposure tool (MA6). An ultraviolate lamp provides the radiation that then passes through the collimating lens onto our device. Interaction of the light with the chemical structure of photoresist causes it to exhibit a new property that is dependent on its tone. There are two tones of the photoresist; positive and negative. In case of the positive tone, the area that has been exposed to UV light becomes soluble in the developer chemical. In the case of negative tone, the area that is exposed to UV light becomes hardened, resulting in these areas remaining on top of the substrate while all the areas that have not been exposed are removed by the developer. In other words, in order to transfer any kind of pattern on top of the substrate surface it is necessary to use a mask that allows only the desired areas of the resist to be exposed to the UV light. A chromium coated quartz is used as the mask, with quartz allowing the passage of UV light and chromium blocking it. This kind of mask acts in a similar fashion to a negative in a process of making traditional black and white photos. Photolithography masks are fabricated by a Compugraphics company that uses our design specification. The mask design is created in L-edit Tanner EDA

software. With many photolithography processing steps, it is important to create a system where, subsequent layers can be related and aligned with the already processed layers on the sample surface. This is made possible by a long focus field microscope that allows to simultaneously focus on the markers on the photolithography mask and on the features on the sample surface. For alignment, the MA6 possesses three manually adjusted degrees of movement freedom x, y and θ.

These correspond to translation in the XY plane as well as rotation of the sample. After loading, the sample it is held in position by vacuum seal (which is a rubber ring that comes in contact with sample, with a vacuum pump removing air from it's inside, providing enough suction to ensure that sample won't be moved from it's position). The photolithography mask is then lowered to contact the sample in order to perform a wedge error correction, which makes parallel the loaded sample and the mask. The mask is then lifted to a required height (dictated by the thickness of loaded sample) and the sample can be aligned using a micrometer screw that controls the x, y and θ movement directions with $1\mu m$ of precision. To be able to perform a meaningful alignment, a sets of photolithography markers have to be created. The design utilized for the alignment markers is presented in Fig.2.2.

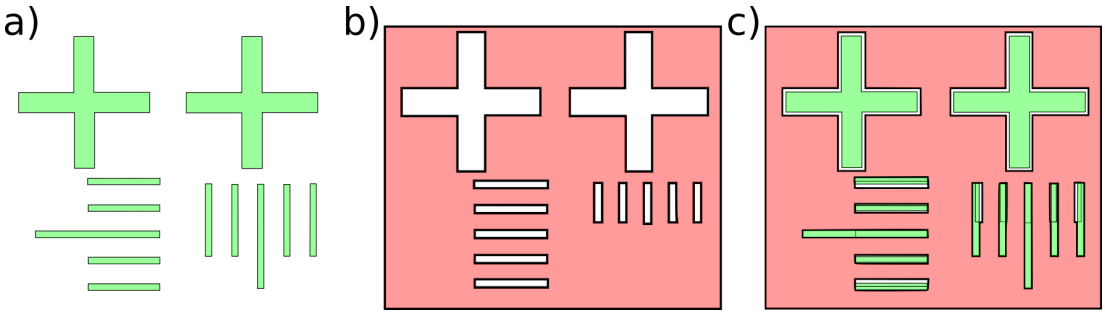

Figure 2.2: Diagram of a markers that were being used for the photolithography alignment purposes. a) presents marker on the sample surface, b) markers on the mask, c) example of the markers alignment

Figure 2.2 a) represents the markers that are transferred on top of the sample surface. This can be done either by etching or metal lift off. In most of the cases placement of these alignment markers is the first step on which all subsequent stages are build upon. Since it is the first step of the processing exact positioning of these is not essential as long as they are all fit on top of the sample. Four copies of all the markers for the

photolithography processing are transferred into the sample with each of them placed symmetrically to their copy at the 4 borders of the sample. Figure 2.2 b) represents the way the marker outline is present on the surface of the photolithography mask that are placed with the same separation distances and symmetries as corresponding markers at the sample surface. Alignment process itself consists of correctly positioning the alignment markers on the samples in relation to the outline markers on the mask with using micrometer screws as can be seen in Fig.2.2 c). In addition to the standard alignment crosses that allow for precision of $5\mu m$ a set of horizontal and vertical vernier markers is utilized to achieve fine precision of $0.5\mu m$ (61) in the x and y directions. Copies of the markers placed at the chip extremities are used for the angular alignment purposes. By aligning markers on one side, the microscope is moved to the other side of the chip, if the markers are misaligned it means that sample requires angular position adjustment. After rotating the sample by the required amount the microscope is moved to the first position to check the markers alignment, if they are misaligned an x, y correction is performed. The microscope is then moved to the other side to check if sample requires angular readjustment. This back and forth process is repeated until markers are in alignment on all the samples' extremities. The maximum angular misalignment can be calculated using following equation:

$$\phi = \frac{\delta y_1 + \delta y_2}{\Delta x} \tag{2.2}$$

where $\delta y_{1,2}$ is the maximum error in the alignment in the $y_{1,2}$ and Δx is the distance between two markers. This means that easiest way to increase the angular alignment precision is to increase a distance between two markers. After achieving alignment like presented in Fig.2.2 c), the sample is brought to contact the chromium coated mask and is exposed with UV light for a specific time that depends on the used photoresist as well as its desired profile to be achieved. In the most standard S1818 process timing of the exposure is 4.4s.

With the exposure finished, if the photoresist used was that of negative tone an additional hot plate bake must be performed in order to harden the exposed resist preventing it from being developed away. For the positive tone photoresist no hot plate is required after the exposure and the exposed resist becomes soluble and removed in the developer. After that negative tone photoresist is being processed the same way as

its positive counterpart.

Removal of the corresponding parts of the resist is performed in the chemical known as developer which dissolves parts of the photoresist. Timing of this process depends on the type of the photoresist and in the case of S1818 photoresist consists of 75s, 1:1 Microposit developer:RO bath with gentle agitation followed by the RO water rinse.

With that a pattern is transferred on top of the substrate surface in the photoresist.

2.4.2 Electron beam lithography

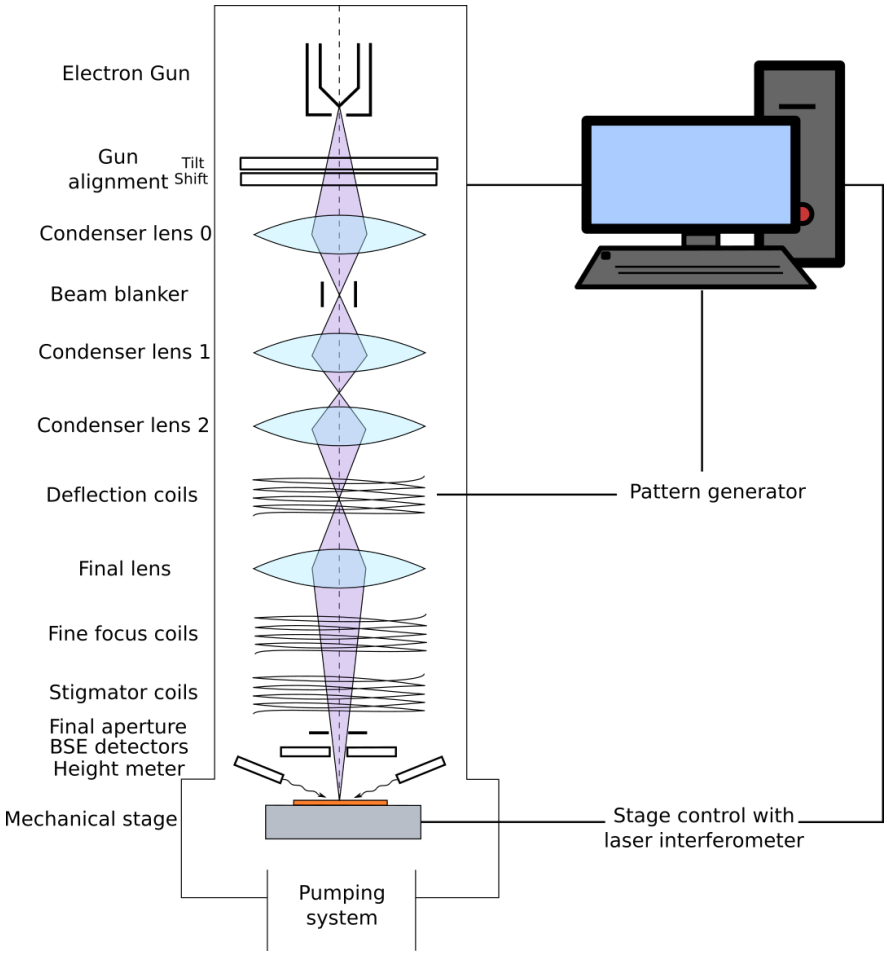

Figure 2.3: Diagram of the beam column of the EBPG5 HR100 beamwriter used for electron beam lithography

Electron beam lithography (e-beam) as the name suggests, is a process of patterning specific resist with usage of directed beam of electrons. This type of resist reacts significantly less with UV or other types of electromagnetic radiation making it easier to process and fabricate. This technique has several advantages over regular photolithography process shown previously. Tool that is capable of performing the e-beam lithography at the JWNC clean room is a Vistec VB6 UHR EWF (62) which shematic is presented in the Fig.2.3. This type of lithography has an advantage over the photolithography as there is no need for mask development every time a new design is required. The writing process itself however can be quite time consuming (compared to photolithography) as the electron beam has to slowly scan over every area to be patterned. Additionally e-beam tools have higher running and maintenance cost than photolithography exposure tools. However the e-beam can pattern features much smaller than these achievable with standard photolithography where the feature size is theoretically limited by the diffraction limit of the UV light. Where UV light wavelength is placed around $10^{-12}m$ an electron wavelength is only that of $10^{-17}m$ allowing patterning features so small that their size is no longer governed by the theoretical diffraction limit of light, but rather by the capabilities of resist used. For a high quality polymers it has been demonstrated that feature sizes of 5nm are achievable (63). For e-beam patterns that require alignment, the tool has an automated self alignment feature with a fidelity of about 50nm, which is much better than that of standard photolithography tool.

The e-beam works in the following way. Firstly an electric current is applied to a zirconium oxide-coated tungsten tip, heating it up to 1800K. This which causes it to release electrons in accordance to the operating principle of a field emission gun, (64) with the capability to accelerate electrons up to 100keV. The high acceleration results in production of a nanometer-scale writing spot. A condenser lens focuses the beam onto the beam blanker. The beam blanker is moved in and out of the beam path to allow for quick switching between on and off states without having to start the ramping up process for the electron gun anew. Two additional lenses are used to control a resulting spot radius on the substrate surface. A deflection coil, directly controlled by a computer with the selected design for patterning, deflects the beam within a $1.3mm^2$

area creating what is called a single field. If a design exceeds this value, the mechanical stage on top of which sample is being placed has to be moved. This movement has to be performed precisely, otherwise the system might loose track of the actual positioning at which two fields connect, overwriting or leaving spacings between fields resulting in so called stitching errors that result in the necessity to repeat the whole process of e-beam lithography again. A final lens along with fine focus coils are used to focus the beam on the sample surface. This allows for a slight corrections to the beam positioning and takes into account possible slight variations of the sample thickness. The stigmator coils ensure that planar components of the electron beam have the same foci. This e-beam system is also fitted with detectors that collect backscattered electrons from which a sample image can be recreated (similar to a electron microscope). Lastly, e-beam column is fitted with a height detector to make sure that the sample remains flat on the surface. The whole system is operated under a high vacuum.

Before putting it into the e-beam system, the substrate is prepared utilizing a similar technique as that for a photolithography - the sample is cleaned and a resist is spun onto its surface. The two most popular e-beam photoresist that are in use in the JWNC clean room are polymethyl methacrylate (PMMA) and Hydrogen silsesquioxane (HSQ), which are positive and negative tone, respectively. A standard recipe for PMMA calls for a spin 5000 rpm for 60 s with an after bake performed at $154°C$ for 120s followed by an exposure by e-beam and development in the 1:1 solution of IPA and methyl isobutyl ketone (MIBK) for 60s followed by a rinse in IPA. HSQ, on the other hand, is a negative tone resist that requires a spin of 3000rpm for 60s followed by a $90°C$ hotplate bake for two minutes, exposure by e-beam and development in a 25% concentration tetra-methyl- ammonium hydroxide (TMAH) for 30 s. What is especially interesting about HSQ, from the fabrication utility point of view, is that after exposure to high temperatures it transformed into a glass like state. This can be especially useful for usage as a masking material for etching.

For e-beam lithography, there are three major effects that should be taken into account that can have detrimental effect on the overall exposure resolution: forward scattering, back scattering, and resulting proximity effects (65) which are represented in a Fig.2.4.

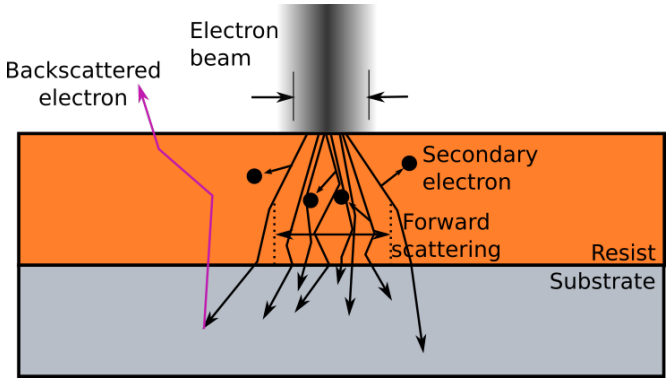

Figure 2.4: Schematic representation of the major effects limiting the exposure resolution

With the high energies, the incoming electrons from the beam mostly travel through the resist without being absorbed. While passing through the resist, some of these electrons produce secondary electrons caused by inelastic electron to electron interactions. The inelastic interaction can be understood ass a type of scattering in which an electron can either gain or loose some of it's energy to another electron (as opposed to elastic interaction where no energy transfer would occur). These secondary electrons possess only a fraction of the energy that the electrons that created them had. Therefore they are only able to travel a short distance in the resist before being absorbed and exposing the resist. This short traveling distance causes a broadening of the effective exposed area in relation to the area under the direct exposure from the electron beam. This mechanism is known as the forward scattering. (66) Backscattering occurs due to the incoming electron interaction with the atomic nucleus either in the resist or substrate that contributes to enlarging of the exposed area on a much larger scale than that of forward scattering. These particles would travel at longer horizontal distances before being reabsorbed and exposing the resist. In the densely patterned structures this can cause a reduction of contrast and altering the sizes and shapes of the features. Both of these effects can be predicted, via simulation , and therefore to a large extent be mitigated. This calculation is done in a separate program before sending the pattern files to the e-beam computer and involves manipulating the dose that the sample receives at the contingency points such as sharp corners and patterns placed closely to each other.

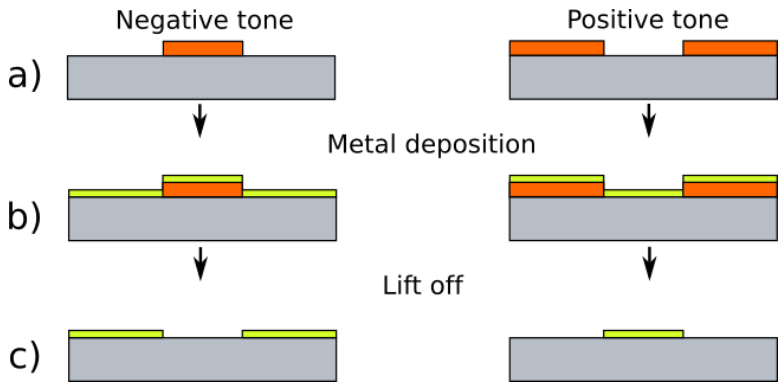

Figure 2.5: Diagram depicting metal contact deposition for positive and negative tone photoresist

2.5 Metal deposition

To achieve an electrical connection allowing for feeding current through fabricated Ge on Si devices, it is crucial to have deposited metallic contacts. The most common techniques for the metal contact deposition are electro plating, electron beam evaporation, and plasma sputtering. Metal deposited with the electro plating process tends to be of thicknesses above $1\mu m$, which is too thick for the applications in this thesis and this process deposits metals with too low of resolution for our purposes. The sputtering method would cause too much damage for the structures that we are trying to achieve. There can be a point made about potential usage for good metalization over the edges with sputtering since it provides a high conformality metal coverage. However the designs presented here have a planar like structure and conformal deposition is not a necessity for creating good working contacts. Therefore, in the course of this PhD only the electron beam evaporation was utilized.

A diagram of the electron beam evaporation system can be seen in Fig.2.6. The JWNC equipment that are capable of performing this type of evaporation are Plassys II and Plassys IV. For example, while using electron beam evaporation to deposit metal on the surface of the sample with an etched free standing mesa, the metal would cover the area around the mesa and its top surface, but without being sputtered at the mesa side walls.

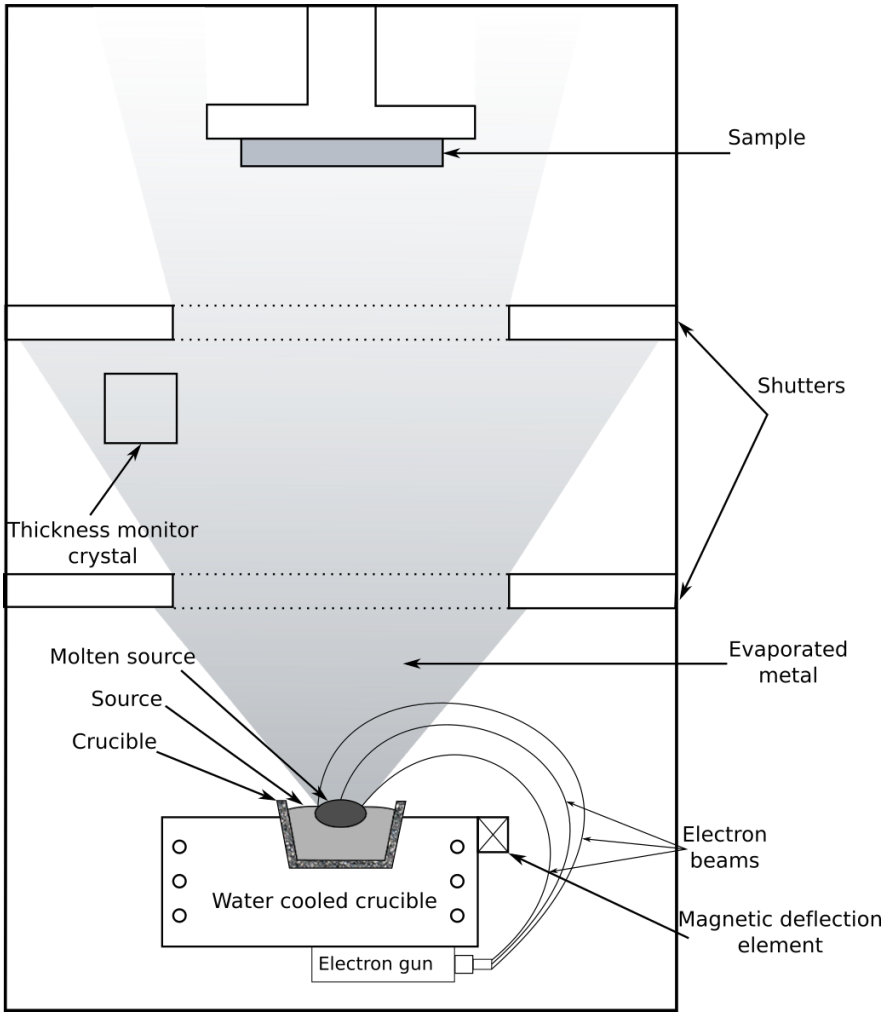

Figure 2.6: Diagram of the electron beam assisted metal deposition tool

Electron beam metal evaporation works as follows. Initially, the prepared sample is loaded into a load lock chamber which possess vacuum capabilities but is disconnected from the other parts of the evaporation tool. It is a necessity as to allow loading while keeping essential parts of evaporation system under the vacuum condition. This minimizes its interaction with the environment and reduces a need for maintenance, as well as significantly decreasing the time needed for pump down (since only a small load lock needs to be evacuated).

Evaporation itself happens after reaching a sufficient level of vacuum inside the

chamber. An electron gun is ramped up to a high voltage and current, reaching a stable power level. The electrons produced by it are then curved by a magnetic deflector and directed onto a metal source placed in a crucible containing metal to be evaporated. Constant barrage of electrons causes some of material in the crucible to melt and eventually reach a point at which it starts evaporating from the surface. During that process the crucible is constantly cooled utilizing a water based cooling system. Ability to use such a simple cooling for the crucible is a result of ability to highly localized the stream of electrons on a small spot within, additionally preventing from extreme raise in the temperature of the crucible. That also allows for very little contamination and high metal quality during the run. As can be seen in the Fig2.6, there are two shutters separating loadlock with a sample in it from a crucible. As the process starts, both of them are closed. After achieving evaporation the first shutter opens. A quartz crystal evaporation thickness monitor is located in the second chamber. With the shutter open, metal starts covering the inside of the second chamber, including depositing the material on the crystal. Oscillation of this crystal is monitored through the process and reduces when additional layers of metal are being deposited on it. By observing the crystal oscillation rate and how it reduces throught the deposition, rate of the metal deposition can be deduced. With that information the electron gun output power can then be adjusted to change the metal deposition rate to a required one. During the evaporation, a specific rate is desired for achieving best quality layers, this rate is manipulated by changing the e-gun output. After achieving the desired, constant rate of deposition, second shutter is opened, and metal is deposited on top of the sample. When the desired thickness of metal has been achieved both shutters close, the load lock is vented, and the sample can be removed from the chamber.

2.5.1 Lift off

After removing sample from the metalization chamber a lift off process is performed. Lift off process is being used in most of the metal deposition cases for this sample fabrication. Its basic principle follows the standard photolithography process and can be seen as a two last steps in the Fig.2.5. After patterning the photoresist in a specific way the metal is being uniformly deposited on top of the sample surface. Some of the metal, therefore, will be deposited directly on the sample surface and some on top

of the photoresist. Following the metal deposition sample is placed in $50°C$ acetone bath in which the photoresist gets dissolved. The metal that was deposited on top of it gets removed from the sample in that process, therefore resulting of only the metal deposited directly on the sample surface remaining.

2.6 Etching

Etching is a process used to perform material removal, either to define the device, provide with isolation or open a via hole for contact deposition. In all of these cases however, parts of the material are masked (usually with photoresist or metal masks)to achieve etching in designated areas only. Etching types can be divided into two broad categories: 1) dry etching - where the material removal is plasma assisted and 2) wet etching - where the material removal is achieved via chemical reaction in solution (which is more physical in nature).

2.6.1 Dry etching

Dry etch is a preferred method of etching if it is required to achieve vertical side walls, precise control over the etch depth or achieving definition less or close to $1\mu m$. This type etch is carried out in a high performance equipment with capabilities for exact control over etch parameters like plasma power, dc bias, temperature, gas flow rates. That in turn allows us to achieve high precision manufacturing.

The two types of dry etching used in this thesis are inductively coupled plasma etching (ICP) and reactive ion etching (RIE).

In, ICP quick etch rates are achieved with low surface damage to the sample. In the most typical ICP systems there is a coil located on the outside of a tool that inductively creates electric field inside the chamber. This field couples to an RF antenna, located inside the chamber, which energizes electrons creating high densities of plasma. To allow for an independent control of the pressure inside the processing chamber and pressure of plasma, this method is combined with a RIE technique.

For RIE, plasma is achieved by generating an AC electric field between two parallel electrode plates. Since the plasma contains a mix of light electrons and heavy

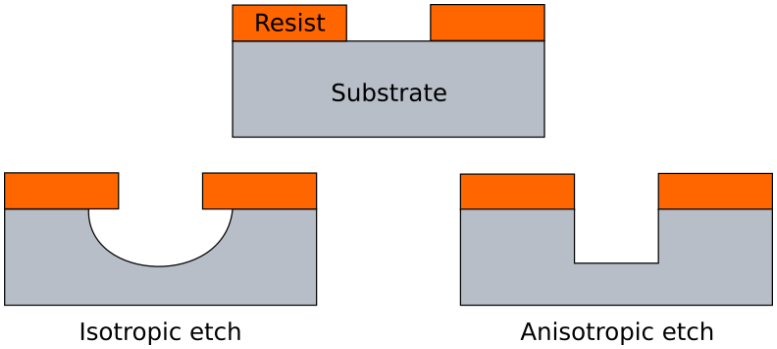

Figure 2.7: Schematic cross section illustrating difference between isotropic and anisotropic types of etch.

ions, the accelerating voltage has a much larger effect of the electrons which reach the plate where the sample is located much quicker. This causes a negative charge build up, and the ions accelerate towards the plate, bombarding the sample in a mixture of physical damage (where the ions dislodge parts of the substrate from the bulk with their kinetic energy) and chemical reaction of ions with the substrate. This chemical etch could potentially cause for an isotropic type of etch which etches horizontally as well as vertically into surface of the substrate just like the wet etches presented below. The difference between wet and dry etch is shown in Fig.2.7. In order to create anisotropic etch profile, after a step of etching a step of surface passivation is performed. In this context passivation means uniformly depositing specific type of layer on top of the sample surface to prevent it from chemically interacting with etching gas. This layer is then stripped by the heavy ion bombardment in the physical part of subsequent etching. Heavy ions travel parallel onto the sample surface therefore interacting only with the bottom of an etched area while leaving the passivated side wall intact. This results with the the side wall surface to interact chemically with ions (rather than via physical bombardment) and since the side wall surface is passivated to prevent such type of interaction it results in the anisotropic etching to occur. After subsequent steps of etching and passivation, the resulting side wall would be vertical in respect to the sample surface and therefore highly anisotropic. Etch rates, profiles and side wall roughness can be controlled by varying plasma densities, DC biases, and flow rate of the gas into the chamber. However, plasma density and bias to the sample plate cannot be independently controlled like in the ICP case. If an increase of etch

rate is desired, an increase of plasma power is necessary. This, in turn, increases the kinetic energy of the ions resulting on a more physical etch, that can cause the resulting surface to have a poor quality because of high about of physical damage by the ions.

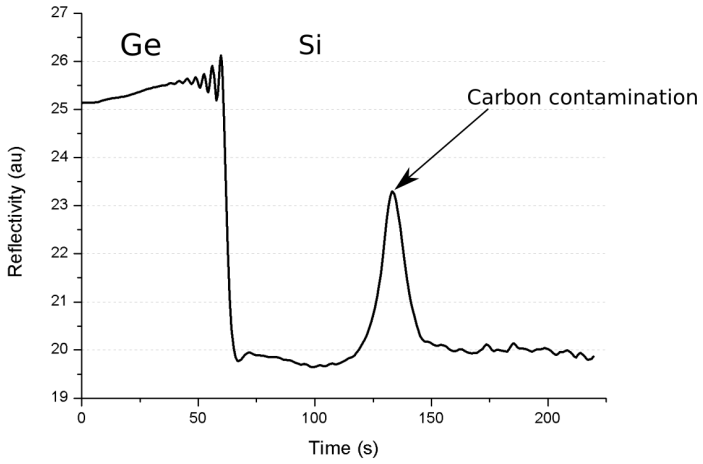

Figure 2.8: Reflectometry data obtained from the in-situ interferometer during an etch through $1\mu m$ of Ge layer into Si layer

With many variables coming into play like loading effects (where the etch rate would be influenced by the shear area exposed to etch) to slight tweaks to the equipment after maintenance. Assessing an exact time needed to obtain given etch depth can sometimes be challenging. In a situation where a high precision of an etch is required and materials etched have distinctively different refractive indexes usage of an in situ interferometer is required. The interferometer (632.8nm laser spot) is focused on the sample. During an etch, a sample surface is removed which causes an interference of the reflected signal that results in an oscillation in the measured power. This in turn ties with the etch depth and can be represented by an equation:

$$d = \frac{\lambda}{2n} \tag{2.3}$$

where λ is the wavelength of the interferometer laser (632.8nm) and n is an refractive index of the material being etched. The material that is being mostly etched is Ge which at this wavelength has a refractive index of 5.47 which corresponds to an oscil-

lation every 58nm (67).

An example of a reflectivity graph taken during the etch of a Ge on Si sample can be seen in Fig.2.8. The initial high value represents etching through the thick Ge layer (total thickness of Ge layer in this case was $1\mu m$). During the etch, the layer of Ge becomes thinner and the interference pattern starts to appear signifying approaching a change of the refractive index. A sudden drop of the reflectivity signifies that medium being etched changed from Ge to Si. For a mesa etch (which is a standard etch for defining the area of the device), the etch would be stopped at this time. However in this instance, the etch was continued to investigate poor single photon detection efficiencies achieved from this wafer. Around 125s there can be seen a spike in reflectivity, since the wafer composition was supposed to be only Ge on Si, this was an unexpected result. However, this led to more in depth investigation that revealed a presence of a contaminating layer of carbon inside the Si layer that resulted in devices produced from that wafer being nonoperational. This example shows an instance where the interferometer tool was useful for more than just determining the etch depth.

2.6.2 Wet etching

Wet etching utilizes chemical reactions between liquid etchant solution and the substrate to achieve desired removal of material. Through this PhD project it was mostly used for uniform etching but selectivity can be achieved if an appropriate material for the specific echant chemistry is used for masking purposes. This etch profile is mostly isotropic due to the purely chemical nature of it (although for some cases it can be purely anisotropic as the chemicals would attack substrate only at the specific lattice plane). The speed of the etch and its profile can be controlled by dilution and temperature of the solvent. The most commonly used etching chemicals in this work were tetramethylammonium hydroxide (TMAH) (for etching away aluminum oxide) and hydrofluoric acid (HF) (for etching native Ge oxide) . HF was especially useful because it doesn't damage Ge and leaves its surface hydrogen passivated allowing for better quality oxide growth. For the less common etches (like silicone nitride and titanium) papers (68) and (69) were used as a reference.

2.7 Limited area growth

One of the issues preventing a quick development of the Ge-on-Si SPAD devices arises from the large lattice mismatch (of 4.2%) between these two elements. This leads to significant threading dislocations on the order of $10^8 - 10^9 cm^{-2}$ which is preventing production of a high performance devices. To try to overcome this difficulty we have looked into a method of growing Ge in a confined area. Proposed by E.A. Fitzgerald (70) and then further developed by J.S. Park (71) and M. Kim (72) the method focuses on growing germanium inside SiO_2 trenches, and provides a reduction of threading dislocations to $\backsim 2x10^6 cm^{-2}$. This level of reduction and the following improvement of device performance might be beneficial even though we will have to face additional challenges connected with this type of processing, which are not present in the simple process of growing blanket Ge. Providing an extremely clean Si surface, and finding parameters for non faceted and completely uniform Ge growth inside the oxide trenches will have to be found alongside with development of an optical mask for the full wafer processing.

An overview of the process is as follows. First the silicon wafer is cleaned to achieve an ultra clean Si surface. The trenches are then etched into the wafer surface. Silicon oxide is then grown inside of the trenches, followed by the two step Ge growth. Firstly at low temperature to achieve a smooth Ge film followed by an increased temperature providing an increased growth rate while maintaining a high quality Ge. Some of the optimisation parameters for the growth will be taken from (72) to reduce germanium faceting, hole filling and good selectivity of germanium on silicon. This will be followed by a cyclic anneal in a furnace to reduce dislocations even further (due to thermal excitation more of the threads would move towards the surface where they can be terminated). 2.9

This process should potentially provide us with minimal threading dislocations within the Ge. In the further work this process could be combined with the previously mentioned guard ring approach (which would be performed before the germanium growth) , providing not only low number of threading dislocations but as well making need for side wall passivation obsolete. Both of these approaches would require further

investigation and process development, but could provide significantly improved device performance.

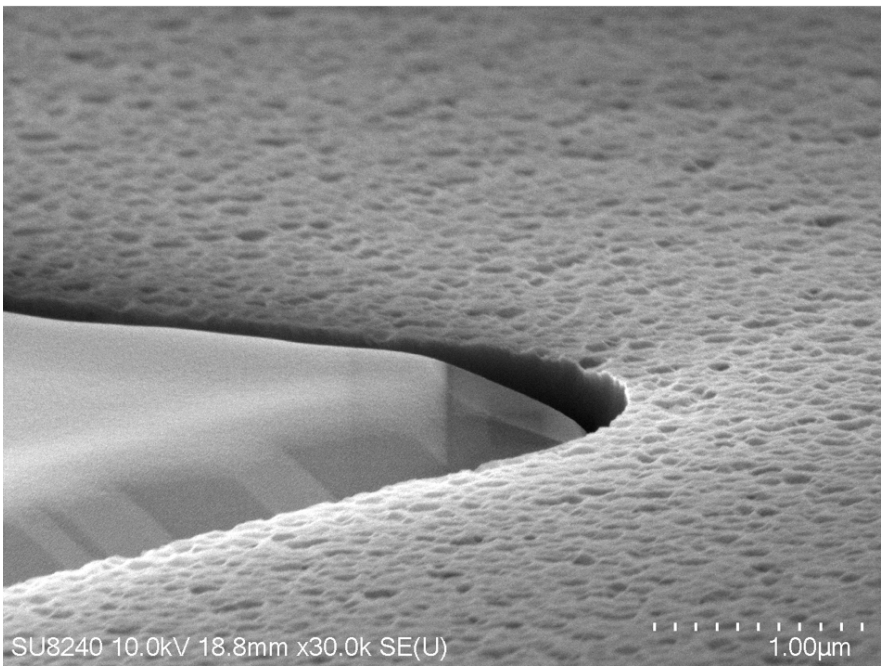

Figure 2.9: Sem picture of epitaxially grown Ge inside of a SiO well.

2.8 Single photon characterization

In order to obtain results on single photon detection efficiency (SPDE), dark count rates(DCR), jitter and noise eqivalent power (which are important metrics of the SPAD performance that will be explained in more detail in the measurement section of this thesis) an experimental setup as presented in a diagram Fig.2.10 was used.

Cleaved devices were connected and wire bonded to a header package which was subsequently mounted on a cold finger of a Oxford Instruments liquid nitrogen dewar cryostat which enables measurements at an accurately controlled temperatures between 77K and 175K. Two pulsed picosecond lasers : PicoQuant and a Supercontinuum NKT tunable laser, were used for delivering illumination onto our devices at 1310nm and in a continuum between 1310nm and 1550nm respectively. Output radiation from these lasers was coupled into Single Mode Fibre (SMF - 28) and then transferred into a

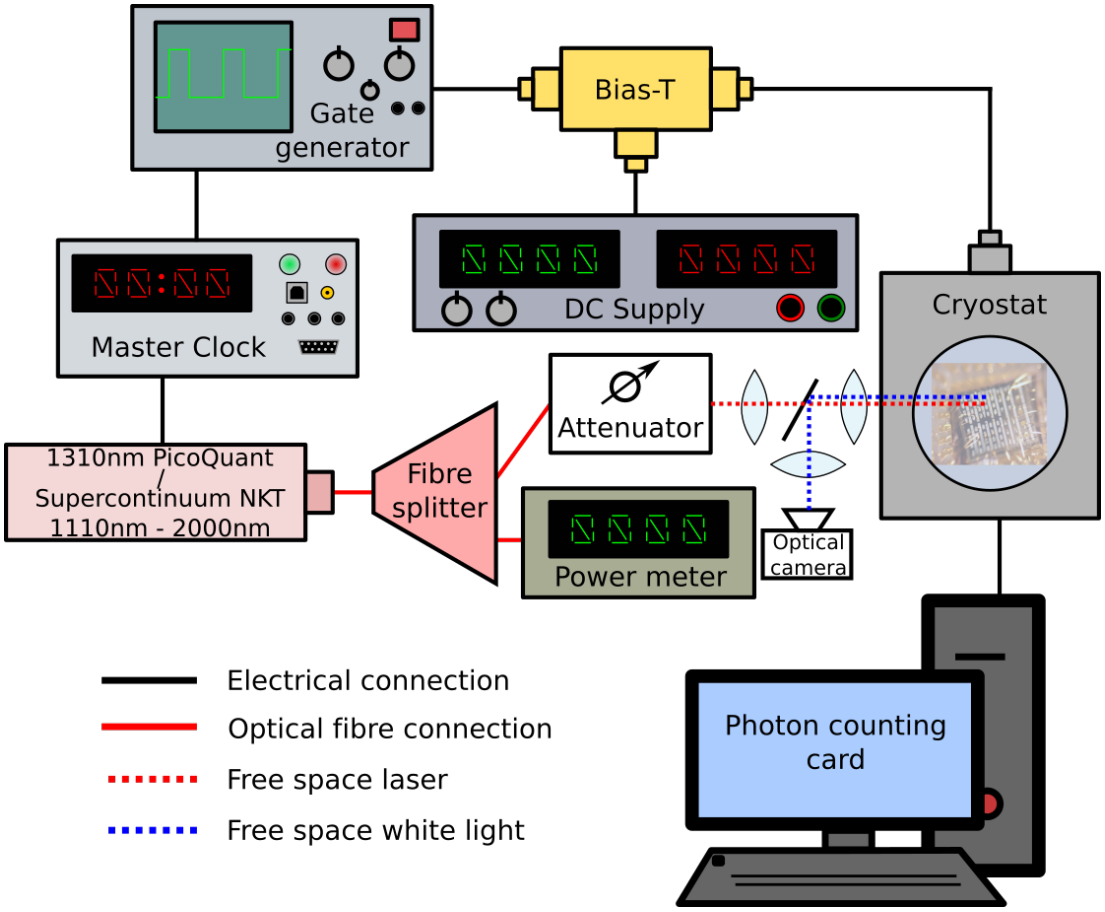

Figure 2.10: Diagram of a single photon characterization setup.

50/50 splitter. Half of the beam is then directed into a power meter to acquire an accurate reading of an outgoing laser power during the measurement. Second half was directed to a calibrated programmable optical attenuator, with attenuation capability of up to 100dB. Before continuing with measurements the output from the attenuator and past the collimator lenses was carefully measured and controlled to assure that during the optical measurements and average flux of photons would be kept below 0.1 per pulse. Distribution of photons in the pulse follows a Poisson distribution and an average number of photons in the pulse can be calculated utilizing following equation:

$$n = \frac{P}{h\nu f} \tag{2.4}$$

where P is the optical power, h is a Planck constant, ν is a frequency of incoming radiation and f is the laser repetition rate. With that, if the photon per pulse rate is

kept at 0.1 per pulse there is a 10% chance of having a photon in a single pulse with a probability of having 2 photons in a pulse is less than 0.5%. Since the photon number is a probabilistic function however there is still chance of having more than one photon per pulse, that is why, to significantly reduce chance of this happening, for an accurate measurement the number of photons per pulse has to be kept below 0.1 per pulse.

Output from the attenuator was then in free space collimated with lenses and focused on a sample surface. Additionally the sample was monitored with an outside camera capable of detecting short wavelength infrared radiation to accurately position the laser spot on detector's optical window. Electrical connection to the sample was carried by GHz bandwidth miniature coax cable to prevent deterioration of electric pulse signals incoming to device and signal outgoing from it. During measurements samples were operated in the gated mode (73) where a bias few volts below the breakdown voltage was applied to the device followed by a regulated electric pulse being superimposed with usage of Tektronix 5530 Bias-T onto the applied bias to bring the device above its breakdown voltage. A figure of merit describing the excess bias above the breakdown voltage is known as the excess bias and can be calculated from a following equation:

$$V_{ex}(\%) = \frac{V_{DC} + V_{gate} - V_{BD}}{V_{BD}} \times 100 \tag{2.5}$$

where V_{DC} is a constant DC bias applied onto the device, V_{gate} is the voltage from the gated pulse and V_{BD} is a breakdown voltage of the device. Device was then brought into an avalanching state either by a dark count or by an incoming photon. Timing of the incoming photons were precisely controlled by a master clock connected to a pulse laser trigger to insure that the timing of illumination would coincide with the applied gate. Outgoing electric signal from the device during the gate event was then directed and measured by a Edinburgh Instruments TCC900 photon counting card. The gate length for the measurements described in this thesis was set up to be 50ns. Avalanche event was continuing until the end of applied gate voltage from the gate generator. An important part of enabling properly timed measurements was utilization of various delays to the gates and laser pulses to ensure that these events would occur at the same time on the device even while taking into account electric signals traveling at finite speeds through the cables and incoming photon traveling through the free space and lenses. This mode of operation is also known in the literature as a Geiger mode.

Photon counting histograms were created for the conditions of illuminated device and a state with no illumination and were used to extract values of SPDE, DCR and jitter.

3

Simulations

In this chapter a discussion of the various simulations that were performed will be discussed with an aim of designing better performing devices. The simulations focus on two main aspects of the device; the charge sheet doping, to allow for the correct electric field profile and the geometry of a pseudo-planar device to minimize the effect of etched side walls and the electric field hot spots.

For the former, the correct doping would provide correct electric field screening between the Ge and Si layers that would provide high enough field in the Si layer to accommodate the avalanche process while being low enough in the Ge layer to not increase dark counts. However, the uniform charge sheet going all the way to the mesa side wall was discovered to result in the non-zero electric field at the side wall, which resulted in the increased dark count rates in previous devices. To solve that issue, a novel planar geometry was proposed. This is based upon the selective implantation of a charge sheet layer, to confine the electric field of the device locally. The simulations here focus on the relative size of this charge sheet and the top contact layer, and also considers an isolation etch (which physically removes material between the devices preventing current flow between them), which is required due to finite background doping in the Ge that acts as a leakage path.

The basic design of the devices, that are the main focus of this thesis, is based on a working principle of Separate Absorption Charge and Multiplication (SACM) avalanche photo diode where the absorption of incoming photons occurs in the Ge and an avalanche multiplication of the photo-generated carriers occurs in the Si. The initial design of the device bares resemblance to an Avalanche Photo Diode (APD) idea

presented in (54), although in order to achieve a single photon detection, some steps had to be taken to greatly increase the performance of the device. However, recently there have been some significant developments in the available techniques allowing for the introduction of changes to the design that would increase device performance. Thanks to the recent developments in epitaxial growing techniques, it would be possible to achieve a thickness of Ge on top of Si greater than $1\mu m$ for much higher incoming light absorption. An increased size of an Si layer in the multiplication area of the device to $2\mu m$ could be used as well in order to increase the ability for registering incoming single photons by allowing for a higher degree of avalanche multiplication. An increased thickness of this layer also contributes to an enhanced voltage distance between Si breakdown and the Ge punch-through, which in return allows for a lower temperature of operation. We have decided to perform a set of simulations of Ge on Si structures with these advancements being included. The appropriate design of the electric field distribution in the device allows for operation in single photon regime. Its influence, modeling and application are discussed below.

3.1 Charge sheet doping

In this section I am going to discuss simulations performed with the Nextano software in order to determine the doping of a charge sheet that would be implanted in the new batch of SPAD wafers. The simulations were performed at 95% of the breakdown voltages, with the bias applied at the top contact area of the device. A diagram of the structure used for the simulations in this section is presented in the 3.1. The charge sheet in presented devices is a layer of p+ doped Si region on the border between Si and Ge. This is one of the crucial components that influences the overall performance, by regulating the electric field distribution across the device. This stems from the very separate requirements of high performance for absorption and multiplication regions.

For the highest possible amplification of a photo-generated carrier, it is important to keep the field inside the multiplication region high, to make achievement of avalanche breakdown possible. The field inside Si should be high enough to accommodate a breakdown across the $1\mu m$ Si multiplication region. The field above 300 kV/cm would be suitable for that purpose. At the same time, the electric field in the Ge absorption layer must be kept below its breakdown (which is at 100kV/cm) but above zero. This

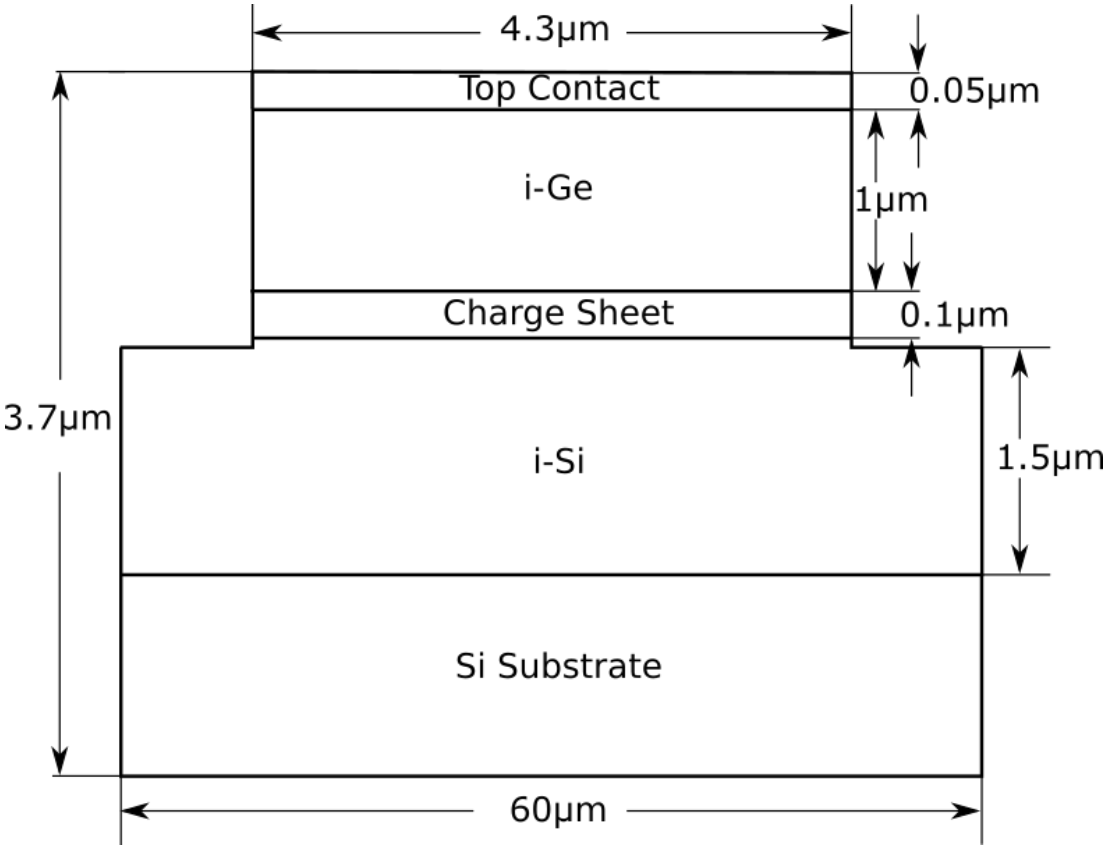

Figure 3.1: Diagram depicting composition and dimensions of the structure used in the simulations presented in this section.

is in order to provide a photo-generated carrier with enough energy to make it more likely to pass into the Si multiplication layer. At the same time the electric field has to be kept low enough to prevent random generation of carriers in Ge, that would in turn trigger avalanche breakdown in the multiplication region leading to an increase in the false (dark) counts. The electric field in the Ge absorption layer should moreover be kept below 100kV/cm to prevent it from reaching breakdown and creating an avalanche current within itself. As a rule of thumb, in order to fulfill above mentioned requirements, the electric field value inside the Si should be three times greater than that within Ge. The horizontal size of the device used in the simulations was scaled down from the size of device that will be subsequently fabricated in order to significantly reduce the computational resources necessary for the simulations. This will, however, still provide a valuable insight into the workings of the larger devices.

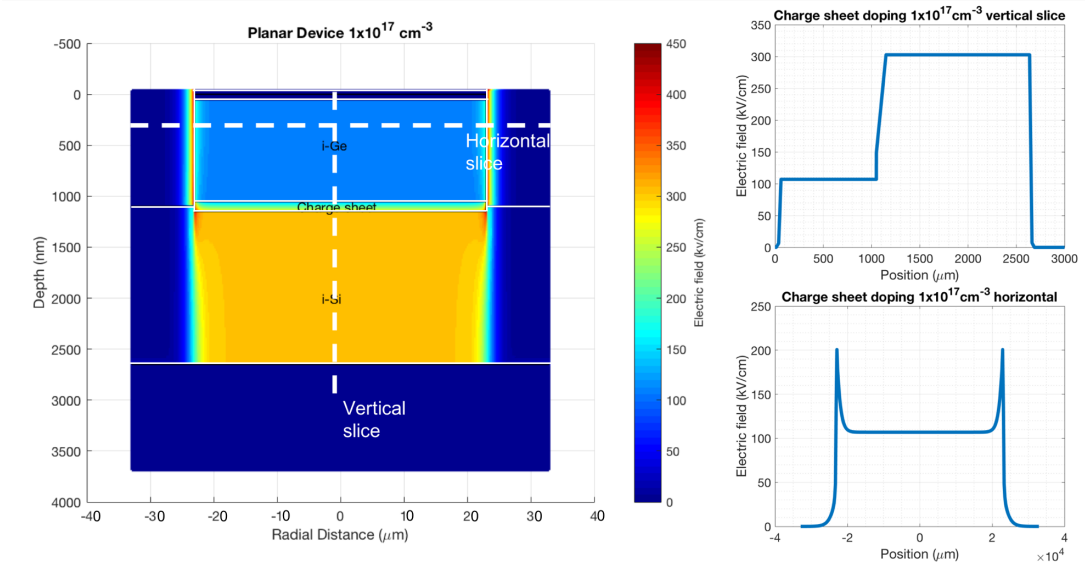

Figure 3.2: Left - electric field distribution within etched mesa device for the $1 \times 10^{17} cm^{-3}$ charge sheet doping. Right - vertical and horizontal cross sections of that field distribution , taken respectively through center and right below the contact area.

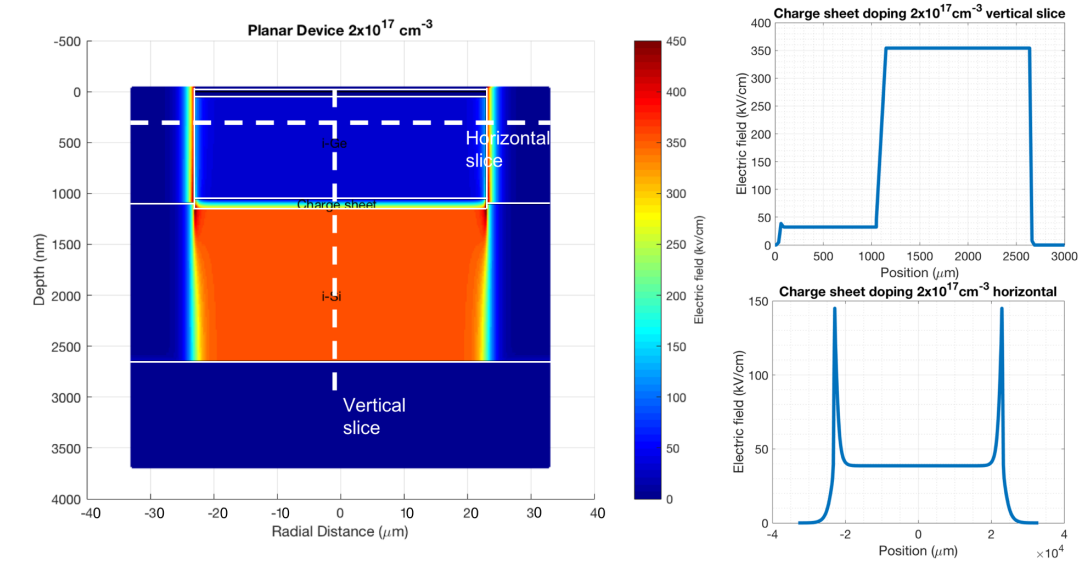

Figure 3.3: Left - electric field distribution within etched mesa device for the $2 \times 10^{17} cm^{-3}$ charge sheet doping.Right - vertical and horizontal cross sections of that field distribution , taken respectively through center and right below the contact area.

It was necessary to run computer simulations of the devices in order to find the

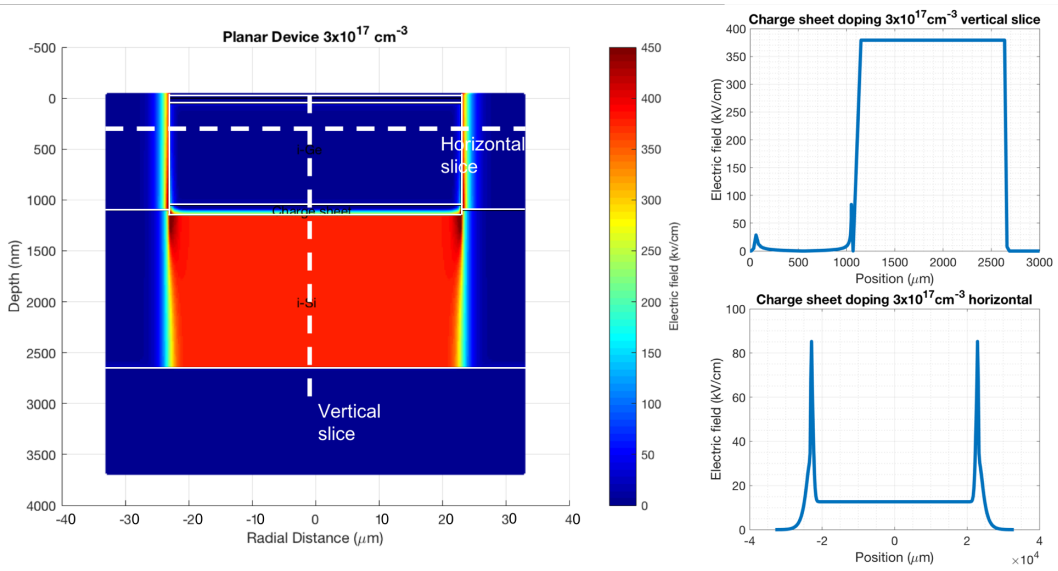

Figure 3.4: Left - electric field distribution within etched mesa device for the $3\times10^{17}cm^{-3}$ charge sheet doping.Right - vertical and horizontal cross sections of the field distribution , taken respectively through center and right below the contact area.

appropriate value for the charge sheet doping. The device geometry, that was selected for the boundary condition, is a free standing, etched cylindrical mesa of the $23\mu m$ radius, etched past the Ge layer and 50nm into the i-Si layer. In the implantation process the exact thickness of the charge sheet can vary slightly, but for the sake of simplicity a charge sheet of a precise thickness of 100nm is assumed in the simulation. The initial simulations in 1D for the Ge on Si SACM device were described in (4) and used for the first set of devices. A deeper investigation of the electric field in the case of a $1.5\mu m$ layer of Si was required. The simulations were performed with a 2D approach to better understand the electric field distribution near the exposed mesa side wall, potentially increasing our understanding of the side wall passivation influence on the overall performance. The values of the charge sheet doping, centering around previous results were used as a starting point for this investigation. The voltage applied at the top contact of the devices was -58V.

In the figures from Fig.3.2 to 3.6 the results of these simulations for dopings of $1\times10^{17}cm^{-3}$, $2\times10^{17}cm^{-3}$, $3\times10^{17}cm^{-3}$, $4\times10^{17}cm^{-3}$ and $5\times10^{17}cm^{-3}$ respectively are shown. The large heat map on the left hand side represents 2D map of the electric

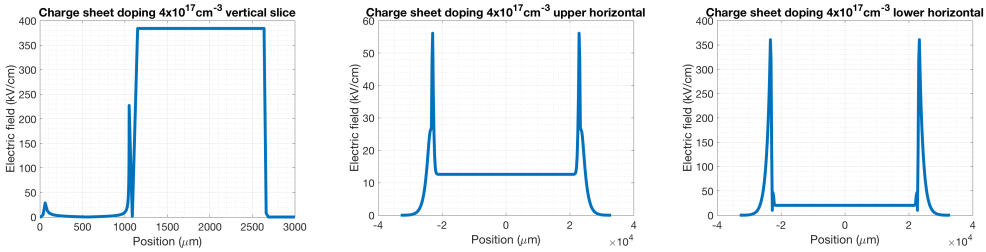

Figure 3.5: Vertical and two horizontal cross sections of the field distribution simulation for $4 \times 10^{17} cm^{-3}$ charge sheet doping, taken respectively through center, right below the contact area and right above the charge sheet area.

field for the selected value of the charge sheet doping. On the right hand side vertical and two horizontal cross-sections are shown. The vertical cross-section was taken through the middle of device and horizontal ones were taken at the top of the device and right above the charge sheet respectively.

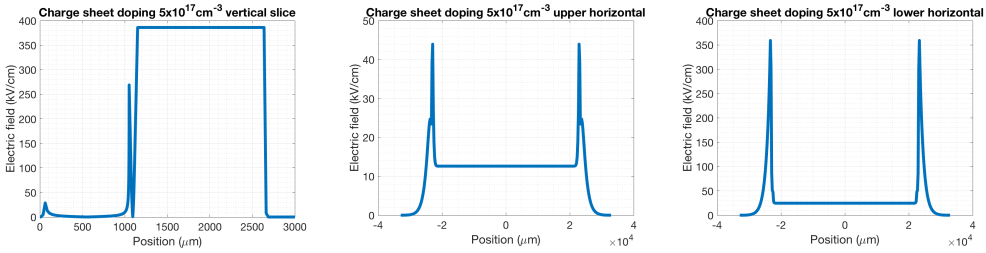

Figure 3.6: Vertical and two horizontal cross sections of the field distribution simulation for $5 \times 10^{17} cm^{-3}$ charge sheet doping, taken respectively through center, right below the contact area and right above the charge sheet area.

After initial simulations it was observed that devices with a charge sheet $1 \times 10^{17} cm^{-3}$ do not fulfill the requirements stated earlier for the values of the electric field. As can be seen in Fig.3.2, even though the electric field in the Si multiplication layer reaches a required minimum of 300kV/cm, the field in Ge is higher than 100kV/cm. This could potentially lead to a great number of dark counts originating in the Ge. This suggests that the charge sheet doping is too low and doesn't screen electric field in the Ge sufficiently. Simulation for the charge sheet doping of $2 \times 10^{17} cm^{-3}$, is presented in Fig.3.3. For this value of charge sheet doping it can be observed that the field in Ge is screened to a greater extend than in the previous example. Even though

only reaching 32kV/cm it is high enough to make the SPAD device operational. The electric field inside of Si on the other hand is higher than in the previous case reaching 350kv/cm, which is within an expected working range. This result strongly suggests that this value of the charge sheet doping might be the one to produce best working SPAD device.

The electric field profiles for the device with charge sheet doping $3 \times 10^{17} cm^{-3}$ is presented in Fig.3.4. As shown on the 2D heat map and especially on the cross-sections, a device with this charge sheet doping would be unlikely to perform as a SPAD device. This is mostly due to the electric field not being able to punch through into the Ge layer, causing any carriers generated within it to remain largely stationary. This is due to the high doping of the charge sheet. It is possible to achieve the field extension into Ge by increasing the applied voltage that would fully deplete the charge sheet. Even though this would create the desired field in the Ge, it would cause values in the Si multiplication layer to increase as well. Simulations were run at the higher voltages in order to investigate that condition. It was observed, that by increasing the value of applied voltage to a point in which the electric field punches into Ge, the electric field in Si increases to an amount high enough to cause it to have a really high DCR, negating this devices ability to detect photo generated carriers.

Simulations of the $4 \times 10^{17} cm^{-3}$ and $5 \times 10^{17} cm^{-3}$ charge sheet doping were displaying behavior similar to the $3 \times 10^{17} cm^{-3}$, where increased value of the charge sheet doping causes more extreme screening of the electric field into Ge. These simulations are therefore only presented in the form of cross-sections as seen in Fig.3.5 and Fig.3.6. Thanks to the results presented in this section it was decided to proceed with development of the new batch of wafers with values of the charge sheet doping centered around $2 \times 10^{17} cm^{-3}$, as this was displaying the most desirable characteristics.

3.2 Charge sheet implantation

One of the major issues diminishing the overall quality of a SPAD device is a sidewall current caused by poorly passivated mesa structures. This, in addition to the fabrication difficulties of performing an active area defining etch, being one of the expected

performance limiting factors was a motivation for an investigation of new methods of device design and the way in which an active area is defined. Since the structures proposed as the aim of this project is similar to the single photon detectors based on InGaAs/InP it was decided to investigate the methods which were used during the development of these devices and assess if any of them could be used in Ge-on-Si devices. One of the methods found this way was development of a localized doped area (75) (76) (77). The idea of guard rings, to create such an area, for use in InGaAs/InP photodetectors was adapted from the initial work considering an increase in the surface breakdown voltage of a planar junction (78) and p-i-n diodes (79) which saw a later development into a numerical design method for the optimum ring spacing (80). In the InGaAs/InP devices it is essential to have an electric field high enough to cause avalanche multiplication in the InP but not too high, because a high field would significantly increase tunneling in the absorption InGaAs layer (81). This would present similar challenges to appropriate charge sheet. Extensive amounts of work were put into the development of suitable ways of applying this approach (82).

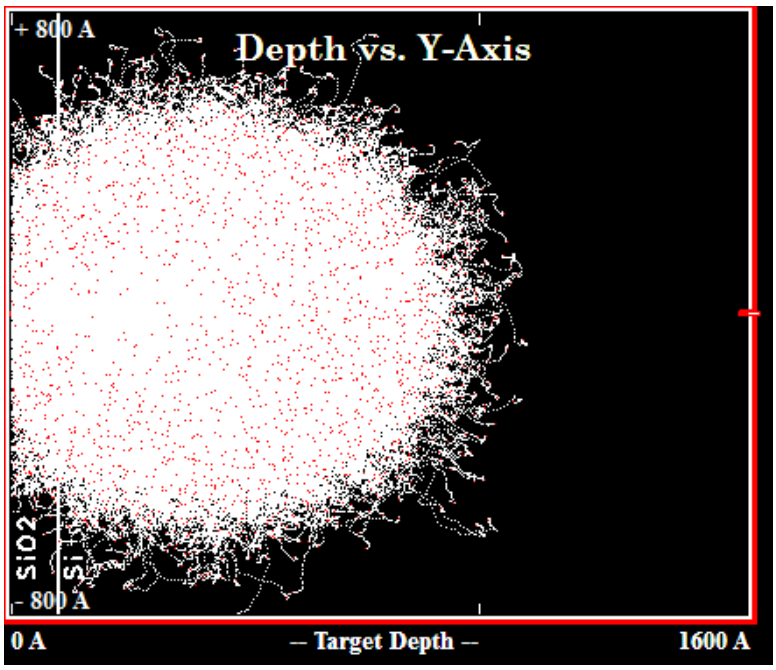

Figure 3.7: Simulation of the ion penetration paths for $10keV$

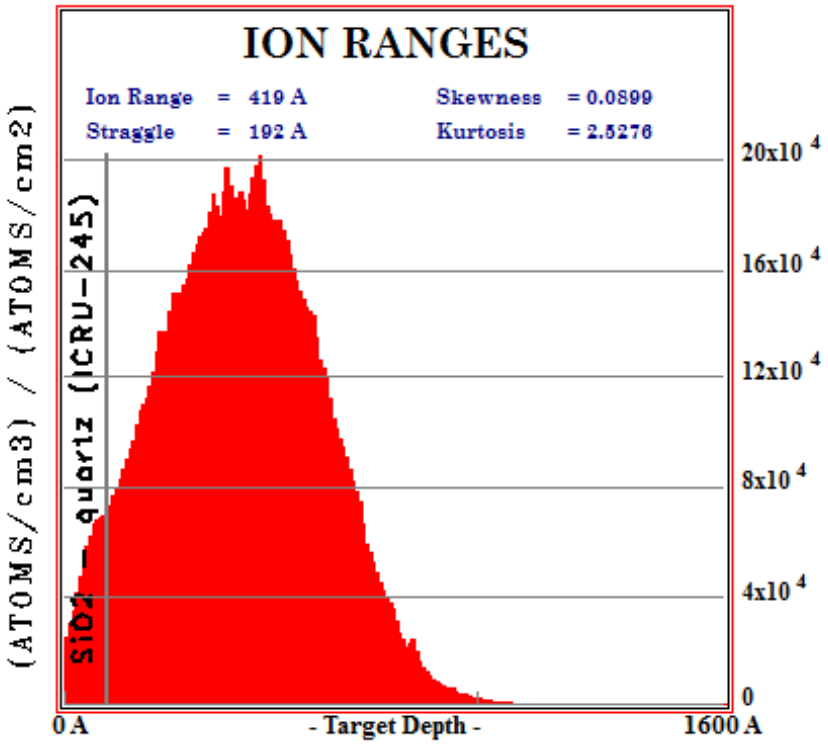

Figure 3.8: Distribution of ions in the material for $10keV$

In the case of Ge-on-Si SPADs, design of the structure is different than in the case of InGaAs/InP but some of the experience gained in process development of guard rings for these devices could be used. A major issue in our devices is control of the electric field in both the Ge absorption region and the Si multiplication region. This field is controlled using a heavily doped Si charge sheet which separates Ge and Si regions.

During processing one of the initial steps is defining devices by etching through the Ge and the charge sheet. This confinement of the charge sheet provides well defined devices. Unfortunately, sidewalls are created by etching which then require passivation. This difficulty could be overcome by defining structures using a locally doped charge sheet. This would prevent current spreading without creating side walls that would later require passivation. The initial plan for this would be to acquire material after growth of the Si layers. This material could be covered with photolithography resist, patterned and developed providing well defined places that would be doped for the

purpose of creating the guard ring. After doping implantation, the wafer could be sent back to the grower for completion of the Ge growth.

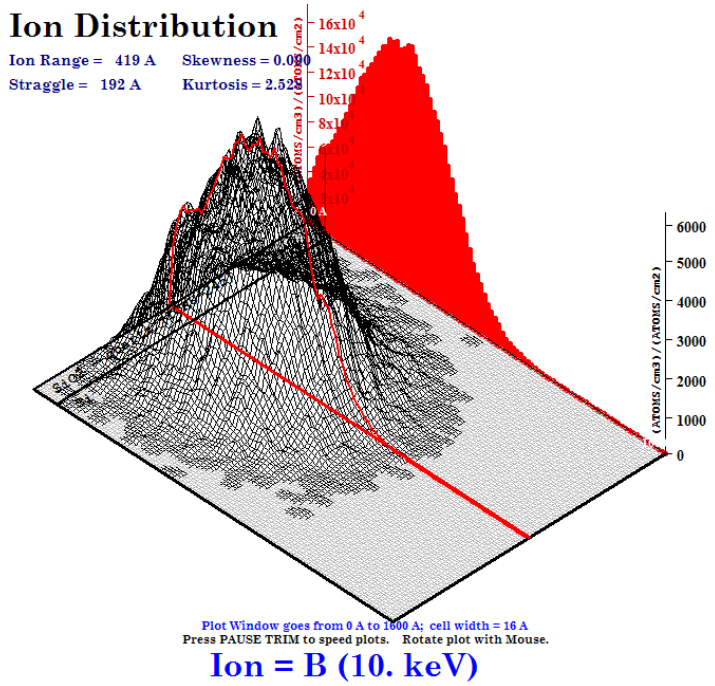

Figure 3.9: 3D ion distribution for $10keV$

Achievement of such a structure would require designing photolithography for the whole wafer at once as well as investigation of the proper parameters for doping. For now, focus was put on modeling of the doping parameters. For this it was decided to use SRIM, a software package which provides programs allowing for calculation of the distribution of ions in various substrates using a Monte Carlo method for the random ion impacts. The first thing that needs to be simulated with the program would be a table of the ion energies and the correlated projected range, longitudinal and lateral straggling. Wafers prepared for doping are covered in SiO_2 to minimize some of the entry point damage caused by incoming ions, this also reduces the chance of an ion traveling alongside the Si lattice greatly increasing the maximum ion depth. It is also important to have taken into consideration that after the implantation process during removal of the SiO_2 layer, some of the underlying Si might get stripped or damaged. Therefore, the ion energy has to be selected in such a way so that it would provide 90%

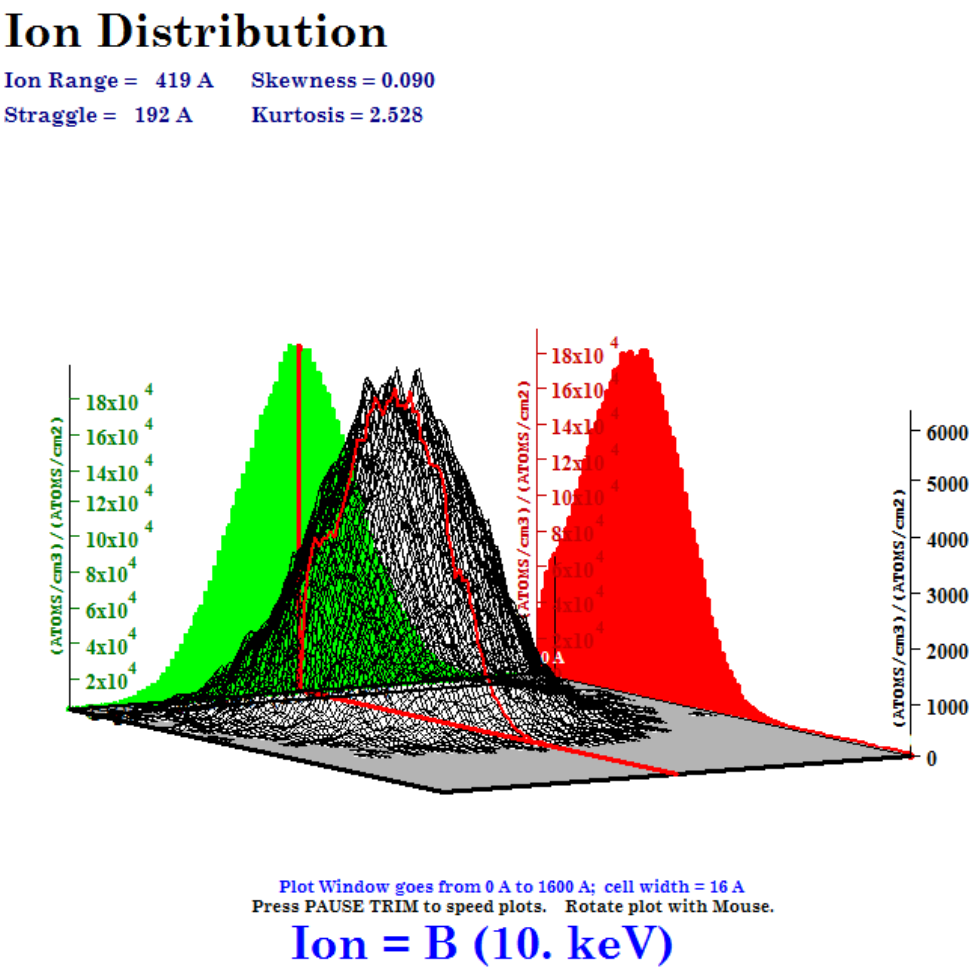

Figure 3.10: 3D ion distribution for $10keV$

of the ions getting trapped in the first $100nm$ of Si (which is simulated in the thickness of the charge sheet for these devices) but not too high in order not to penetrate masking material. Relatively high concentration of ions getting trapped is also required since not all of them will become active after the activation process. Based on this it was possible to select ion energies for the collision simulation. Ion penetration is a random process which can be simulated, and for the large numbers of ions used in simulation it should give a rough estimate to show if the selected ion energy would be sufficient.

In the figures from Fig.3.7 to 3.11 one can see the results of such simulations. Based on these, an energy of $10keV$ was selected as the most promising one for the actual

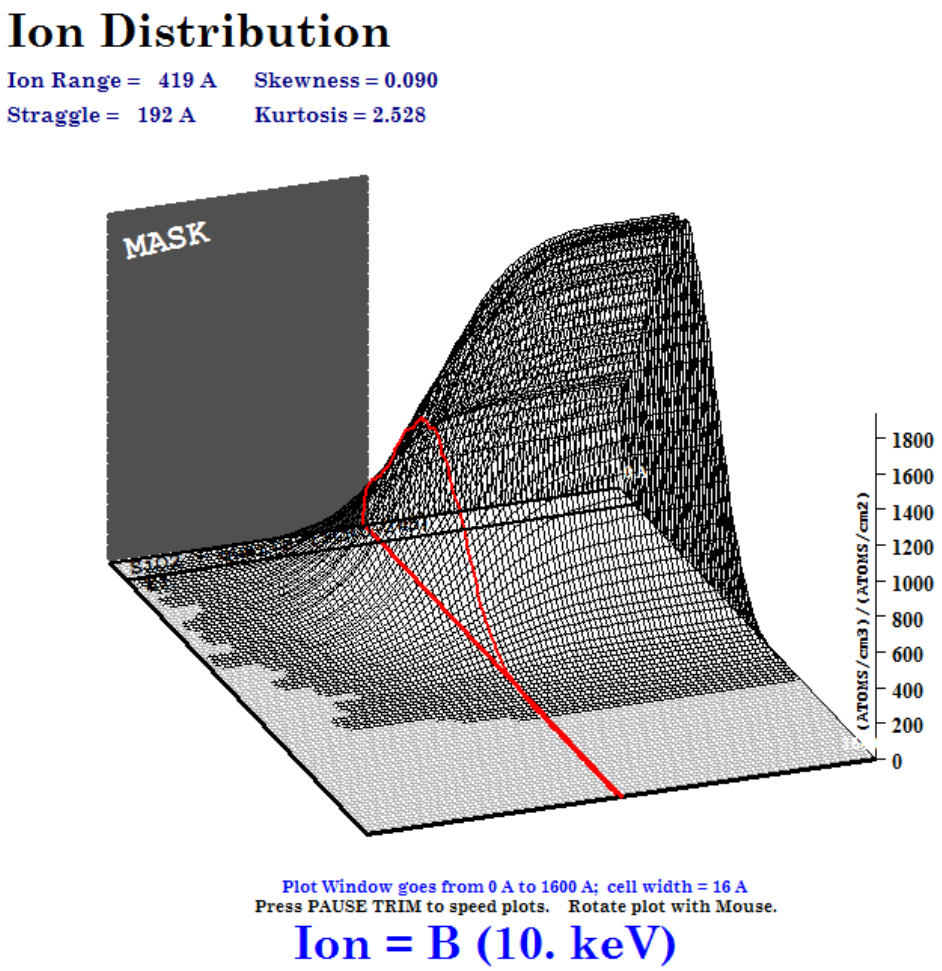

Figure 3.11: Effects on ion distribution in a situation of part of the material being masked. Result for $10keV$ ion energy

doping test. It can be seen from the pictures that this energy provides us with sufficient amounts of ions getting past the SiO_2 layer and into Si. It can be seen in Fig.3.7 that most of the ions are stopping within 100nm of the Si, therefore providing the earlier stated size of the charge sheet. No ions (from the 50000 used in the simulation) managed to pass through the i-Si layer. Even though straggling of ions underneath the mask was observed (Fig.3.11) this should be low enough not to cause any concerns for the final device confinement and would be impossible to prevent.

It is worth noting that for the production test a couple of different ion densities,

around the one selected for the simulation, should be used. This is because of the hard to predict nature of ion activation which might result in higher or lower than expected activated doping densities. Based on the earlier assumptions 5 different dopings ($1 \times 10^{17}cm^{-3}$, $2 \times 10^{17}cm^{-3}$, $3 \times 10^{17}cm^{-3}$, $4 \times 10^{17}cm^{-3}$ and $5 \times 10^{17}cm^{-3}$) in the charge sheet were selected. Even though it is predicted that a doping density of $2 \times 10^{17}cm^{-3}$ would produce wafers with the highest performance it is important to include a wider range for tests. This is because of the doping activation and lack of relevant information on Ge, especially when compared to Si . For the wafer implantation an energy of $10keV$ will be used for all the different doses.

3.3 Selectively implanted charge sheet

Significant changes have been made to the fabrication and the design of the SPAD devices since first presented in the (4). The more in depth analysis of the oxidation methods, uniform planarization and better etch processes have been developed, but improvement of the overall performance of the devices seemed to only be incremental. It became apparent that the reason for the lack of significant improvement might lie in the most basic assumption about devices' design. In this section we are going to discuss some of the electric field simulations that were performed in order to pinpoint required design changes that would increase performance of the devices. A diagram of the structure used for the simulations in this section is presented in 3.12.

All of the simulations presented in this chapter are performed for the charge sheet doping density of $2 \times 10^{17}cm^{-3}$ which was determined to produce best results in the previous section 3.1.

We begin our investigation with a device bearing resemblance to the previous designs. The charge sheet here is a $100nm$ thick layer uniformly stretching over the whole wafer. The active area is defined by the etch going through the charge sheet into the Si multiplication layer. The radius of the mesa created by this etch is $23\mu m$. The top contact area in this device was etched as well, stopping at the Ge absorption region. Radius of that p++ Ge etch was selected to be $15.5\mu m$. The simulation was performed for two cases of uniform charge sheet and selectively doped charge sheet. The size of

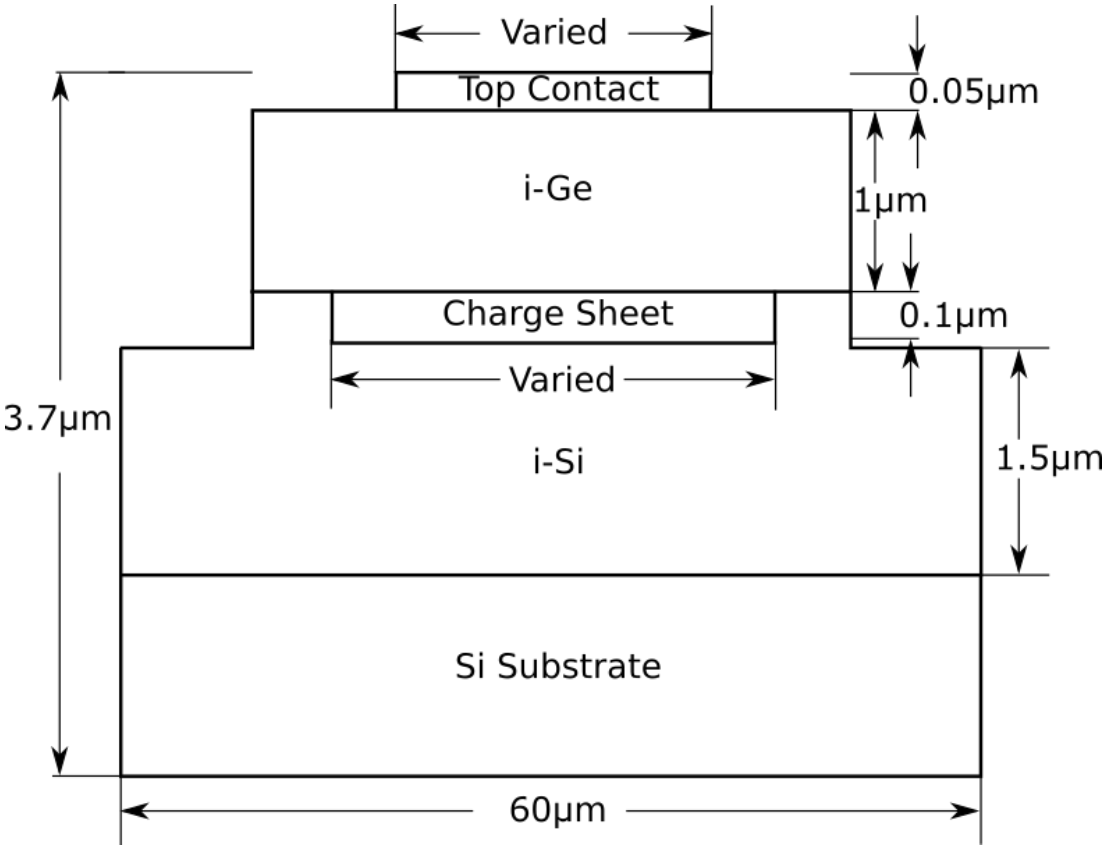

Figure 3.12: Diagram depicting composition and dimensions of the structure used in the simulations presented in this section.

the selectively doped charge sheet was constant for all of the subsequent simulations and was selected to be $13\mu m$ in radius. Because of that, the main purpose of these simulations is an investigation of the influence of relative top contact etch size to the size of underlying charge sheet.

As can be seen in the first simulation Fig.3.13 top, where the top contact radius was defined by the etch greater than the lateral charge sheet size, the top contact influences field distribution inside Si. The field in Si spreads to the limits defined by mesa even though exibiting slightly more confinement in the area directly below the etch. Difference the top contact etch makes can be seen exceptionally well when comparing etched top contact in Fig.3.13 to the device with full top contact in Fig.3.3. That dependency could have a positive effect on the overall device performance, even though

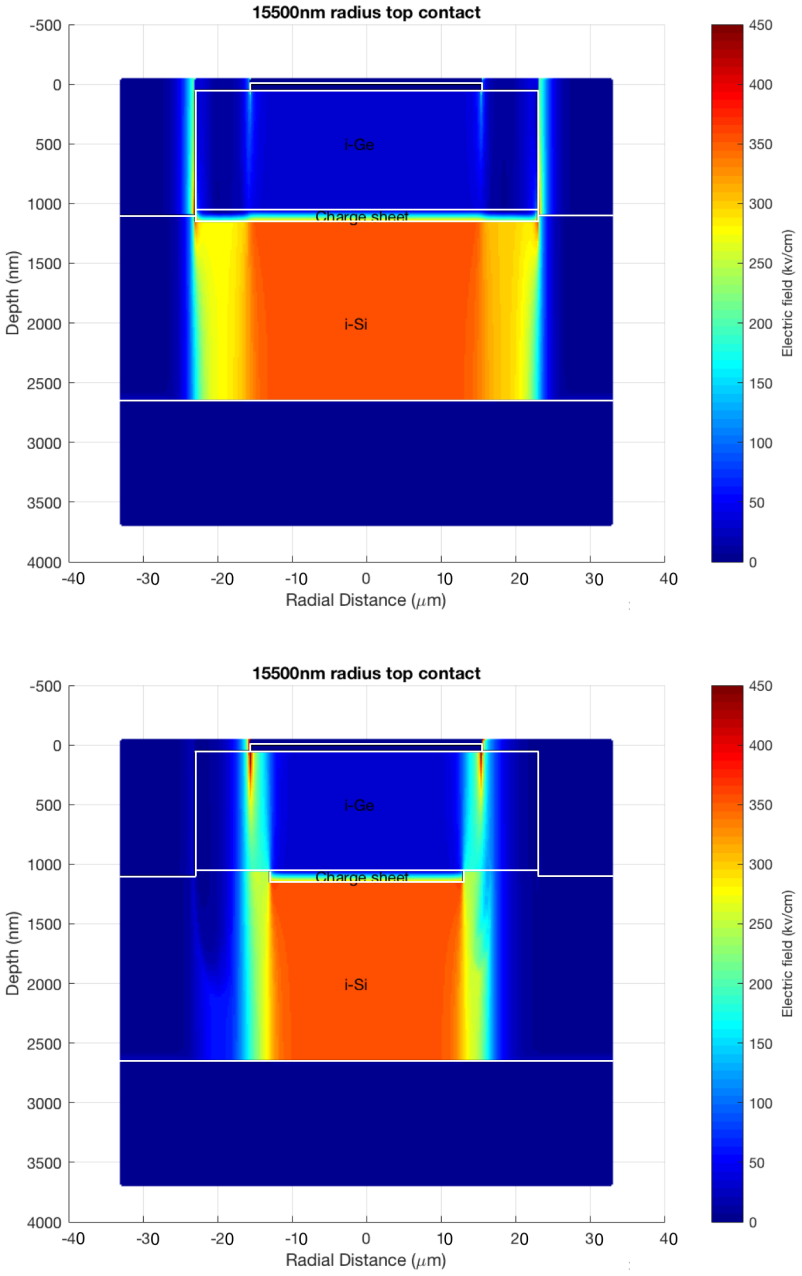

Figure 3.13: Electric field distribution within etched mesa device with $2 \times 10^{17} cm^{-3}$ charge sheet doping and $23\mu m$ mesa radius. Top - design with uniform charge sheet and etched $15.5\mu m$ radius top contact. Bottom - design with selectively doped $13\mu m$ radius charge sheet and etched $15.5\mu m$ radius top contact.

it still exhibits some field at the side wall.

Bottom figure in the Fig.3.13 represents a device with the top contact defined by the etch with $15.5\mu m$ radius and selectively doped $13\mu m$ radius charge sheet. The etched top contact in the case of a full charge sheet exhibits a small level of field confinement, however, this effect becomes especially pronounced in the case of selectively doped charge sheet. The biggest difference lies in the way field is being distributed inside Si multiplication layer. While preserving the electric field value in the center of mesa with values same as for the case of simple design for $2 \times 10^{17} cm^{-3}$ charge sheet doping device, it rapidly drops as it gets past the areas defined by charge sheet position and reaches 0 kV/cm outside of the top contact etch area. This suggests that this device possess a more beneficial field distribution in the Ge absorption layer than the design above. The active area of this device effectively becomes smaller, by confining field in Si multiplication layer to a smaller area, therefore creating another potential benefit for the overall SPAD performance.

With the active area serving as a de facto device itself, we arrive at a situation where (while maintaining easier to fabricate larger mesa sizes) the active are of the device itself would be smaller than a size of the mesa.

This could potentially lead to the decreased amount of dark counts originating from the bulk of Ge allowing for operation at higher temperatures or larger mesa sizes.

Biggest issue in this case is the region between areas defined by the p++ Ge etch and the placement of the charge sheet. In this area it can be observed that the electric field in Ge absorption region exceeds value for which avalanche current would occur in Ge. This is especially problematic in the area near the ends of etched top contact where the electric field reaches 450 kV/cm, leading to a device being largely nonoperational or exhibiting difficult to predict characteristics that could be influenced by the positioning of metal contacts in the final, fabricated chip. It can be also observed that near the bottom of the device in the Si multiplication area, some of the electric field extends past the charge sheet area and reaches etched area of the mesa. This effect, however is largely an artifact of the way the simulation is being run, either due to the meshing error near this area or not sufficient number of iterations. We can say for sure that this feature is just a software artifact because of the circular symmetry of our design, as it is not appearing on the right hand side of the device in the same region.

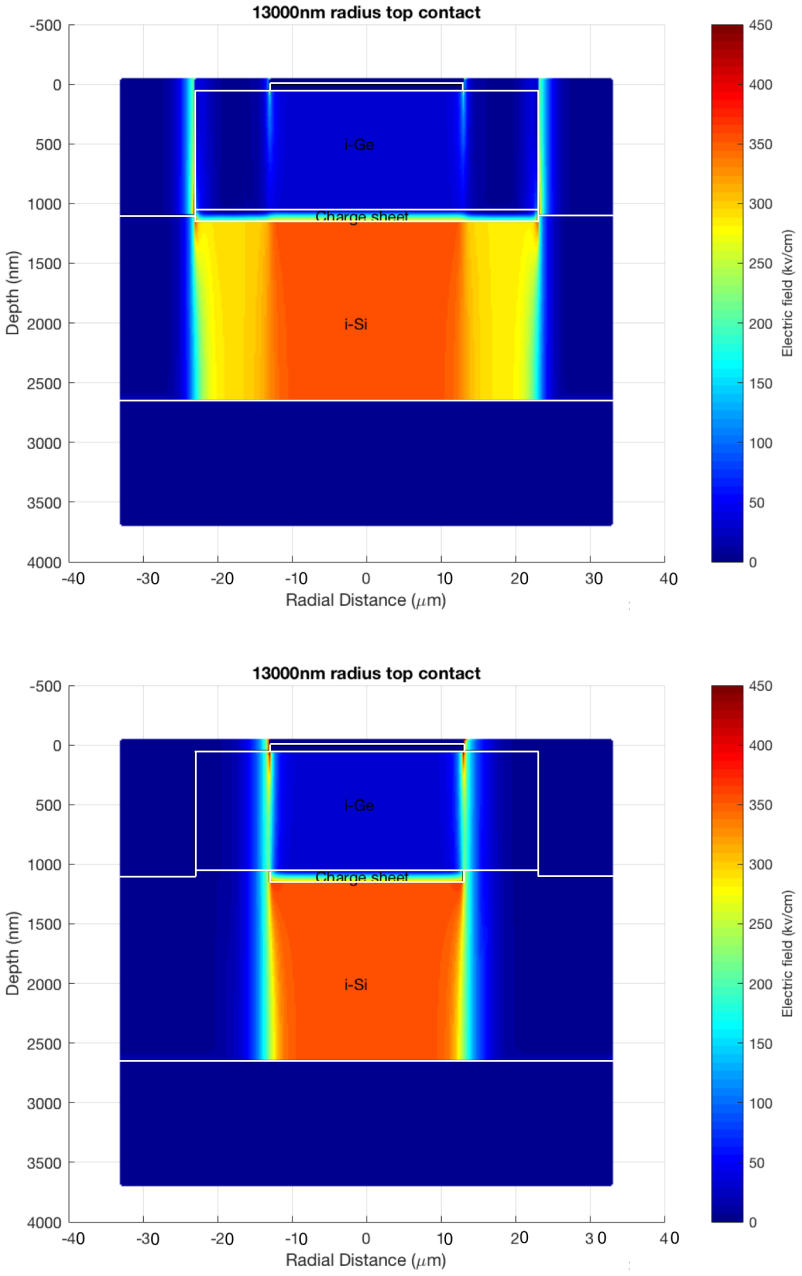

Figure 3.14: Electric field distribution within etched mesa device with $2 \times 10^{17} cm^{-3}$ charge sheet doping and $23\mu m$ mesa radius. Top - design with uniform charge sheet and etched $13\mu m$ radius top contact. Bottom - design with selectively doped $13\mu m$ radius charge sheet and etched $13\mu m$ radius top contact. (TC=)

These results were interesting and encouraged us to pursue some additional modeling for both the uniform and selectively doped charge sheet with etch defined top contact.

Acquiring this positive result we have decided to perform the electric field simulations on the design proposed earlier. The sizes of the etched mesa ($23\mu m$) and implanted charge sheet ($13\mu m$) were kept the same through the simulations.

It was decided to investigate three additional cases for both embedded and uniform charge sheet designs:

- Top contact of the same radius as implanted charge sheet ($13\mu m$ and $13\mu m$). For the future purposes this design will be abbreviated as: TC=
- Top contact of radius smaller than implanted charge sheet ($10.5\mu m$ and $13\mu m$). For the future purposes this design will be abbreviated as: TC-
- Top contact of radius much smaller than implanted charge sheet ($5.5\mu m$ and $13\mu m$). For the future purposes this design will be abbreviated as: TC+

These three cases are represented in Fig.3.14, Fig.3.15 and Fig.3.16 respectively.
The varying sizes of the top contact etch result in the different outcomes for the devices with full and selectively implanted charge sheet. With that we will discuss these two cases separately, bringing them together at the end of this section.

For a device with the uniform charge sheet and varying top contact it can be seen that the outcome of simulations follows a trend suggested by the initial assessment for case presented in Fig.3.13. The non zero electric field area inside the Ge absorption layer is dictated by the size of the top contact etch. The same holds true for the high field area in the Si multiplication layer. Even though the active size of the area gets smaller inside the Ge, the electric field spreads up to the edge of the mesa in multiplication layer, and it does not decrease in value as the top contact etch gets smaller but rather continuously spreads out. In turn, this causes a creation of hot spots at the bottom corner of the etched mesa in which electric field reaches values above the breakdown in the Si layer. It should be noted, that for all these cases there is also an electric field of values above the Ge breakdown that is spread across the mesa side wall surface, amplitude of which remains unchanged while decreasing the

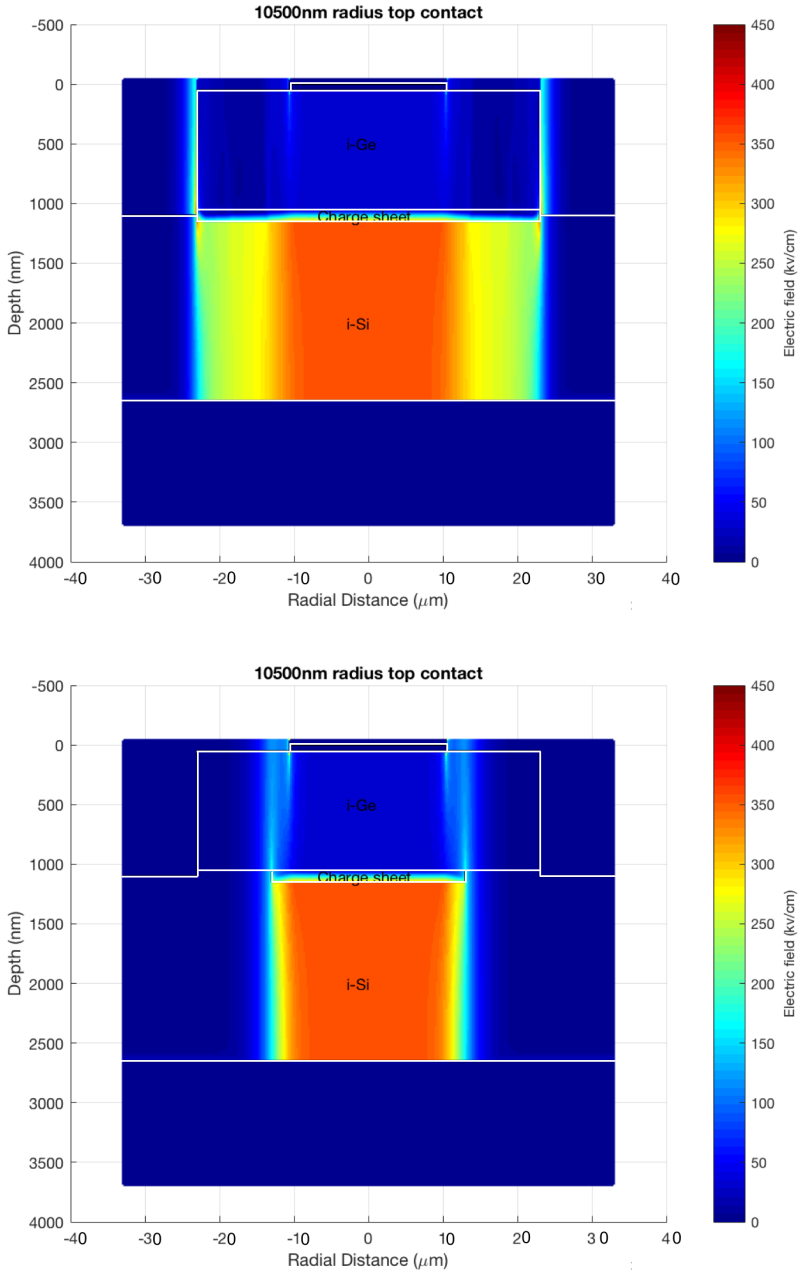

Figure 3.15: Electric field distribution within etched mesa device with $2 \times 10^{17} cm^{-3}$ charge sheet doping and $23\mu m$ mesa radius. Top - design with uniform charge sheet and etched $10.5\mu m$ radius top contact. Bottom - design with selectively doped $13\mu m$ radius charge sheet and etched $10.5\mu m$ radius top contact. (TC-)

top contact etch radius. This combined with the hot spots at bottom corner of the mesa, could lead to a decreased device performance. The lacking surface passivation combined with the electric field at the mesa side wall could lead to the creation of the leakage paths. In these, generated carrier in the high field region would be given enough energy to travel into the Si multiplication region,where it causes a dark count. These are all serious issues suggesting that even though the initial idea of decreasing the size of the top contact etch for the uniform charge sheet seemingly benefited the field distribution inside the mesa, this benefit was not significant enough to outweigh the problems with that design. It was therefore decided to investigate in more detail an idea of the selectively doped charge sheet that was suggested earlier.

Let us begin investigation of the different relative top contact etch sizes with a case of TC= in Fig.3.14, we can immediately observe a difference in the electric field distribution to a case with the larger top contact. The high field area in the Ge absorption region became much smaller with the hot spots at the edges of top contact becoming visibly reduced. This confinement of the electric field can also be seen in the Si multiplication region, where the high electric field (allowing for the avalanche process) becomes reduced to an area defined by the charge sheet. This is in stark contrast to a field distribution for the uniform charge sheet case where the field in multiplication region stretches to the edge of the mesa. With such a confinement of the electric field, we can reason that the active area of the device is largely defined, in the case of selectively implanted charge sheet, by the sizes of top contact etch and charge sheet effectively causing the device to perform as if it was of a smaller size than suggested by the mesa etch radius. Additionally in comparison with the uniform charge sheet case, there is a lack of increased electric field areas at the mesa side wall for the device with the embedded charge sheet, therefore decreasing the role a mesa side wall would have on the overall device performance.

The results from this case were really promising, therefore design TC- (with dimensions as listed before) was investigated. As can be observed in the Fig.3.15 and Fig.3.16, there is indeed a beneficial change in the electric field distribution for these two cases. It can be observed that the hot spots present previously at the edges of the etched top contact have greatly diminished in size, causing the electric field in these regions to reach values between 100 and 150 kV/cm, which are just above the desired value in the Ge absorption region. Operating the devices at lower biases, however,

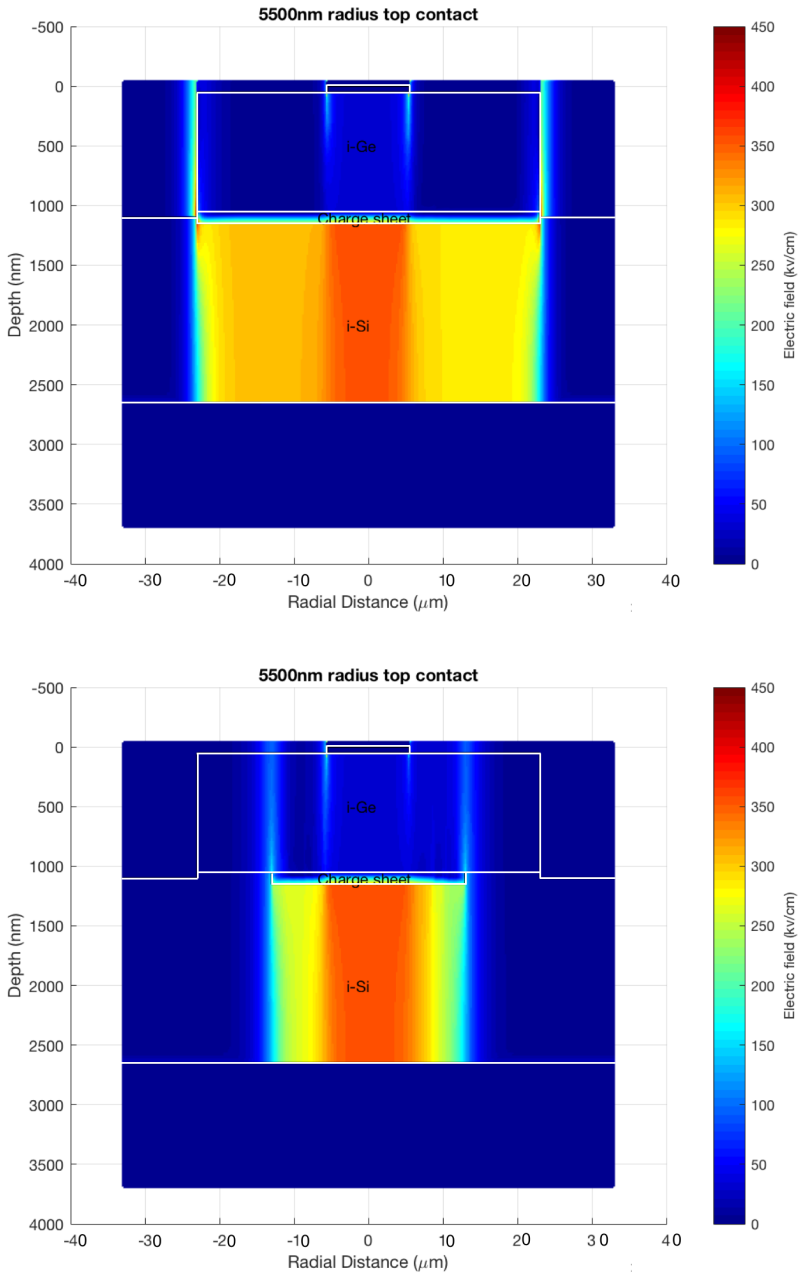

Figure 3.16: Electric field distribution within etched mesa device with $2 \times 10^{17} cm^{-3}$ charge sheet doping and $23\mu m$ mesa radius. Top - design with uniform charge sheet and etched $5.5\mu m$ radius top contact. Bottom - design with selectively doped $13\mu m$ radius charge sheet and etched $5.5\mu m$ radius top contact. (TC+)

should result in the Ge not reaching its breakdown with a current value of the charge sheet doping. In the case with $5.5\mu m$ etched top contact it can be seen that these hot spots continue horizontally down to the charge sheet, where as in the case of $10.5\mu m$ etched top contact, the field of top contact hot spots merges with hot spots originating at the edges of the charge sheet effectively creating a larger area of higher electrical field. As expected decreasing the radius of top contact etch kept the electric field at the mesa side wall at 0 kV/cm as in previously discussed case. Field distribution in the Si multiplication layer remained largely the same for cases of $13\mu m$ and $10.5\mu m$ etched top contact, suggesting that the size of implanted charge sheet exerts stronger influence on its field distribution. For TC-, however, it can be observed that the field distribution on Si multiplication layer is different than for the cases of larger etched top contacts. While the electric field still remains high in the region defined by the charge sheet radius, it can be observed that it remains at highest value in the region directly under the etched top contact. This suggest that the relative size of these two layers interplays in creation of the field distribution inside the Si. Even though it is not fully confined within the area encompassed with top contact etch to a degree where we could define this active area as of that of a smaller device, this could still prove beneficial for the overall performance. This is because of the electric field not being high enough at the boundaries to allow for triggering of the avalanche event in the Si to be caused by bulk Ge generated carriers.

With these simulations at hand it is concluded that the design with implanted charge sheet would exhibit the best performance. Therefore all wafers used for the device generations in this thesis were fabricated with that design in mind. Additionally, since they were displaying characteristics with a potential to increase the performance even further, it was decided to incorporate device designs with varying size of the top contact etch radius with a future processing steps. Since the simulations presented here were done for the scaled down version of a mesa structure, and no interaction with surface states was modeled, final sizes in the processed devices will be different to incorporate other effects that could potentially come into play changing their behavior from the simulated one.

4

Fabrication

As shown in the previous chapter, there were certain design choices that were displaying promising properties. In this chapter I will present the fabrication steps and methods, that allowed for their implementation in the live devices of generations 12 and 13. The following chapter will present results for the devices from generation 12 as the generation 13 devices are still not finalized as of writing this PhD thesis. However, the initial results on the devices from generation 13 will be presented in the Conclusions chapter 6.

There were many attempts in the early stages of this PhD, to achieve high performing SPAD device but to no avail. Work was started as a continuation of the devices presented in (4) and expanded upon in an attempt to try and achieve better performance. Wafers with different characteristics and designs were investigated along with incremental changes to the published design although the best performance achieved in the current study were very close to already published results. Therefore, a new approach was necessary at either the wafer or device design level. These changes were implemented in the devices of generations 12 and 13 and resulted in a great increase in the SPAD performance for the first case with second still being under investigation as of the time of writing this thesis. The results of generation 12 will be presented in the measurements chapter 5 and the initial assessment of devices from generation 13 will be presented in the conclusions chapter.

As a basis for device fabrication a range of wafers with selectively implanted charge sheet dopings of $1 \times 10^{17} cm^{-3}$, $2 \times 10^{17} cm^{-3}$, $3 \times 10^{17} cm^{-3}$, $4 \times 10^{17} cm^{-3}$ and $5 \times$

$10^{17} cm^{-3}$ were used. Simulated behavior and arguments for using these specific values are presented in the simulations chapter 4. Fabrication of the wafers with these charge sheets are presented in the fabrication section of Gen12 below. Some of the techniques that were developed to successfully fabricate the working devices will be presented in the fabrication section below. If a technique required longer development process or went through multiple iterations to achieve the desired properties it will be described in detail in the methods chapter 2. A description of the design choices for the devices of generation 12 will be provided in the following sections, along with the motivation behind and fabrication of these. Additionally/Finally a description of the design choices and the fabrication of generation 13 devices is given.

4.1 Generation 12 device design description

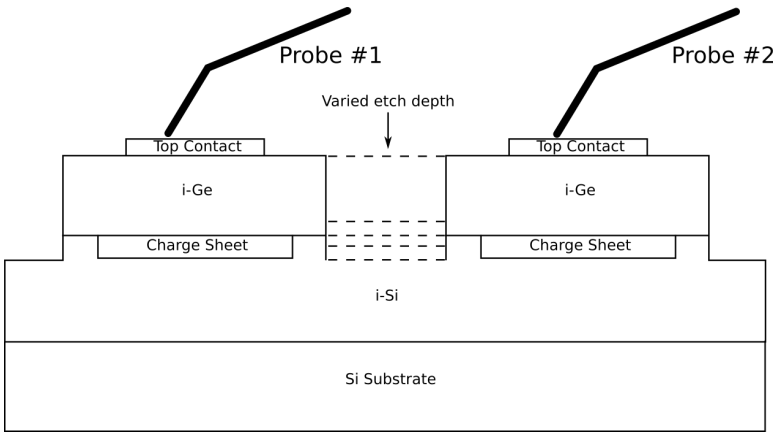

Figure 4.1: Diagram representing a measurement of leakage between two devices.

Initially devices in generation 12 were predicted to perform as full planar devices with only a shallow mesa etch to define the contact area in the p++ Ge, based on the results of the electric field simulations (presented in the simulations chapter 3). These suggested that for the cases of a selectively doped charge sheet and etched top contact of a radius similar to that of the charge sheet, the electric field would be confined to the area defined by them. That would allow for a fabrication of devices in which only a top contact etch is required to confine the field. After initial tests, however, the devices with only a top contact etch were performing poorly. More in depth investigation revealed that there exists a non-zero current between devices on the chip as seen in

Fig.4.2 this current is called a leakage current.

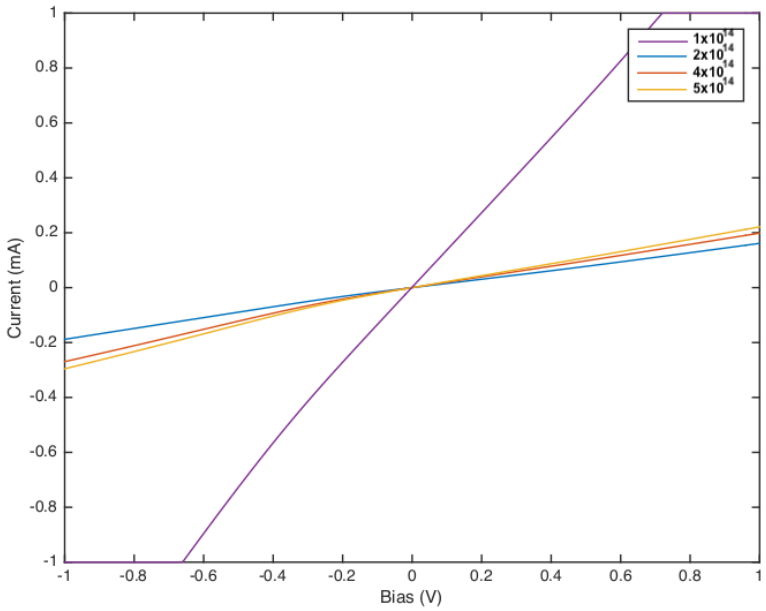

Figure 4.2: Leakage current between devices for wafers of different charge sheet dopings.

The investigated chips were fabricated from the same wafers. The wafer consists of a $550\mu m$ thick n++ Si (100) substrate with a $1.5\mu m$ i-Si avalanche region epitaxially grown on top of it, in which there are selectively doped charge sheets with dopings of $1 \times 10^{17} cm^{-3}$, $2 \times 10^{17} cm^{-3}$, $3 \times 10^{17} cm^{-3}$, $4 \times 10^{17} cm^{-3}$ and $5 \times 10^{17} cm^{-3}$. On top of a i-Si these wafers have epitaxially grown $1\mu m$ i-Ge absorption region with an $50nm$ p++ Ge contact layer grown on top in-situ. These wafers will be denoted as SPAD1, SPAD2,SPAD3, SPAD4 and SPAD5 depending on their charge sheet dopings respectively. Measurement was done as depicted on the diagram 4.1. Two probes used to drive the current between the devices were placed on top of the etched top contacts of both of those devices.

It can be observed for all the cases, except SPAD1, there is a leakage current passes between devices on the same chip. For the SPAD1 this current is much larger than for the other cases, this is most likely due to a shorter top contact etch time on the chip of that wafer. Even thought the etch was measured to be around 50nm seemingly not all of the p++ Ge was removed from the top surface. This could be due to the

uncertainty of the resulting thickness after the p++ Ge doping or a measurement error in the stylus profilometer (Dektak) top contact etch depth acquisition. In order to exclude the possibility of the etches not fully removing the p++ Ge layer for the cases of SPAD2, SPAD4 and SPAD5 resulting in leakage current between devices, deeper etches were performed. After a series of different etch depths and acquisition of the corresponding current measurements between devices, it was discovered that the leakage current stops only after etching past the Ge absorption layer into the Si multiplication region as depicted by dashed line in diagram 4.1. Contradictory to the simulations that suggest there is a non-zero electrical field spanning at the distances from one device to another which is localized entirely inside a Ge absorption layer. Simulations that were performed for the wafers did not suggest the existence of such a effect (since the lateral spread of the electric field terminated in the area dictated by the size of the top contact and charge sheet), but it might have been caused by the simulations being performed only individual device. With these results it became clear that an isolation etch of sorts would be necessary to prevent a leakage current between devices. The mesa etch performed for the previous generations of devices was decided upon as it would provide device-to-device isolation (if performed deeper than the Ge absorption layer) as well as being developed already for the previous device generations. Therefore, the general

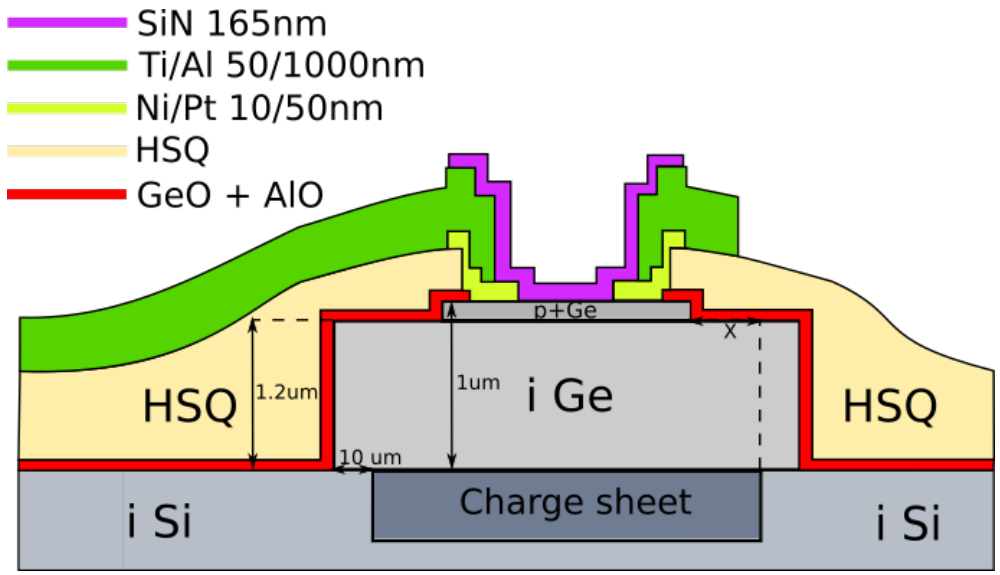

Figure 4.3: Cross section view of the fully processed Gen12 device (picture not up to scale)

design presented in the Fig.4.3, which is a cross section side view diagram of the Gen12 device, was decided upon. In this design the devices are etched just past the $1\mu m$ i-Ge layer, and $0.2\mu m$ into the i-Si, which is deep enough to go past the charge sheet. The etch itself is kept at a lateral distance from the charge sheet at $10\mu m$, this value was selected in order to combine the benefit of electrical isolation between different devices simultaneously keeping the side wall surface far enough from the active area to reduce its influence on the device performance with simulations suggesting that this distance is far enough that the device would get the benefit of a planar like design. A p++ Ge contact etch was performed to define an active area of the device, its lateral distance from the charge sheet being varied and presented in Fig.4.4.

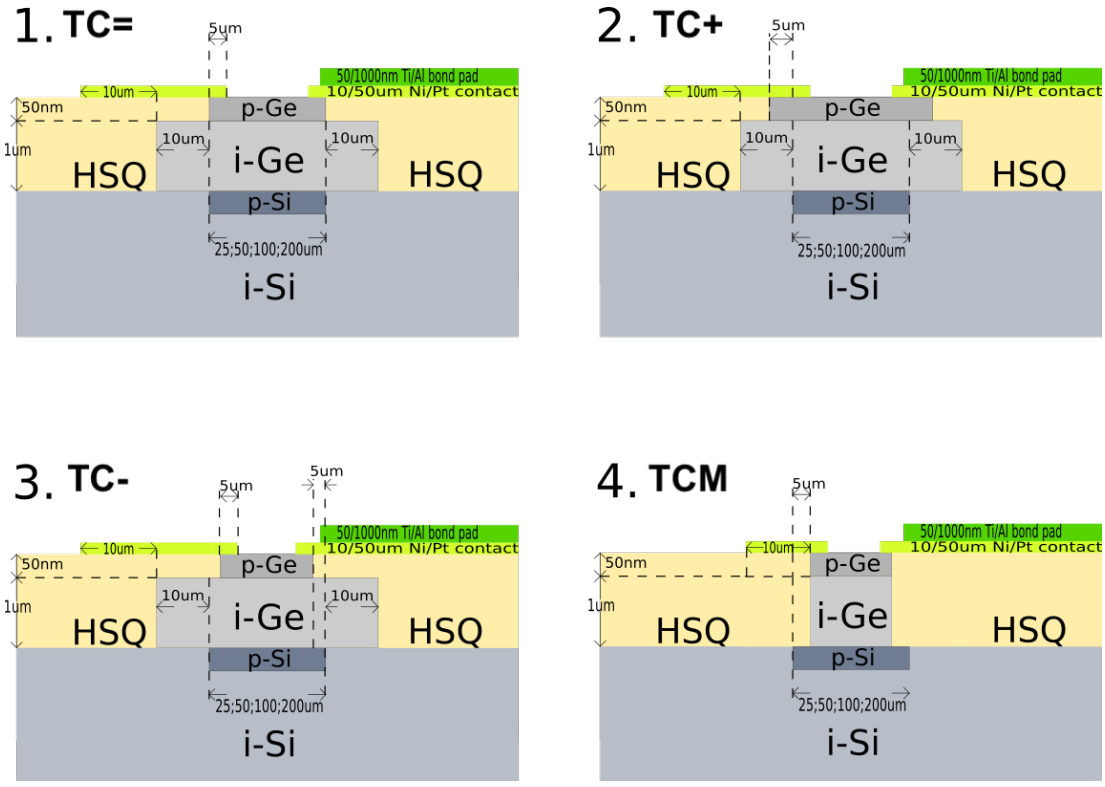

Figure 4.4: Presentation of four different designs located on separate quarters of the chip

Before fabrication on the chip-scale, the full wafer is diced up into $1cm^2$ chips for greater ease of handling. At the end of the processing the chips are diced into four $2.8mm^2$ quarters, whose size is dictated by the available size inside the header package upon which the samples are attached for further measurements. It is then reasonable to

put different designs on each of the quarters. This provides an opportunity to compare the effect of different design choices without having to take into consideration the small changes that occur during fabrication, as it can be assumed that processing is the same within chips of the same size. Differences between quarters are presented in Fig.4.4, and are kept consistent for all the charge sheet sizes within each quarter. The design choices are mainly connected to the size of the p++ Ge top contact etch and are as follows:

- Quarter 1 - radius of the p++ Ge etch of the same size as the underlying charge sheet (referred to as TC=).
- Quarter 2 - radius of the p++ Ge etch larger by $5\mu m$ than the underlying charge sheet (referred to as TC+).
- Quarter 3 - radius of the p++ Ge etch smaller by $5\mu m$ than the underlying charge sheet (referred to as TC-).
- Quarter 4 - radius of the p++ Ge etch smaller by $5\mu m$ than the underlying charge sheet with the overall mesa radius being the same size as p++ Ge etch (referred to as TCM).

For the quarters 1,2,3 all the other distances are kept the same. Quarter 4 presents a case of a mesa being fully confined on top of the charge sheet. This last design was incorporated to mirror the design of the previous generations of devices, where the charge sheet is uniform across the wafer and therefore extends past the radius of the mesa. This would provide an unique ability to directly compare previous generations to the current one without having to take into account any differences in processing.

Although it should not have a large effect on the device performance, a devices side walls and top surface are then passivated with a thermally grown GeO and capped with AlO as described earlier in the methods chapter 2.

Similarly, to the previous generations a surface planarisation was performed for the ease of lift off processes and to provide an electrical isolation of the bond pad from the bulk Si. Previously this was performed with SU-8 photoresist which was replaced in this design with HSQ which provides the ability to process samples at higher temperatures without having to worry about thermal cracking of the planarization layer. After performing a high temperature bake HSQ transforms into silicone oxide providing high

electric isolation from the surface. The HSQ has an expansion coefficient much closer to Si and Ge therefore reducing thermally induced stress in the temperature dependent measurements.

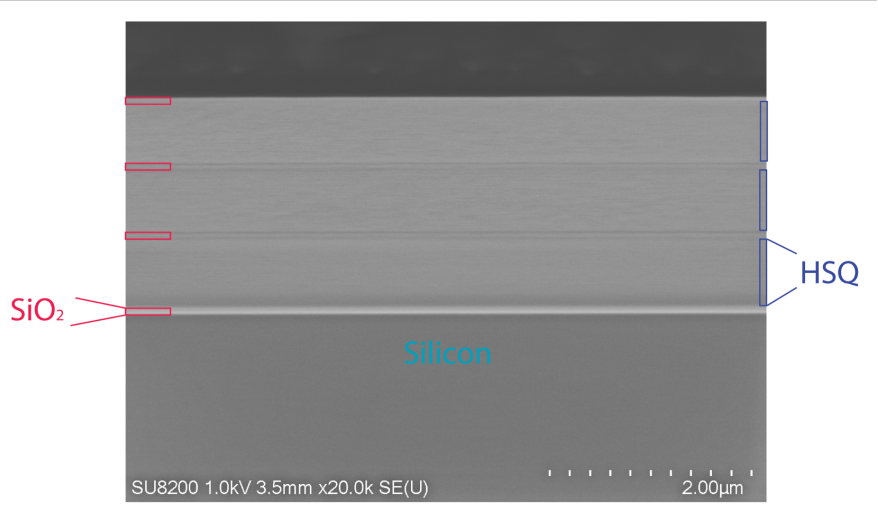

Figure 4.5: SEM pictures of three layers of HSQ separated by thin layers of deposited SiO_2

In Fig.4.6 one can see an SEM image of a cross section through the test samples used for the investigation of the HSQ planarisation process. A test sample comprised of mesa type structures with varying radii of 5,10 and 25μm and covered with two layers of HSQ as described in the following section. The border between two separate spins can be observed on these SEM images as a line creating an increase in contrast. This layer represents a layer of SiO_2 deposited on top of the first layer of HSQ. Its deposition not only provides a distinction between separate HSQ layers but it is also crucial for achieving multi layer deposition. In the investigated cases without this protective layer it was observed that the resulting thickness of HSQ layers after spinning it on two or more times, was significantly less than the sum of thicknesses of singular depositions. After depositing the first layer of HSQ the solvent, present in it and diluting the chemical to a point at which it can be spun, is evaporated from the surface with a high temperature bake. Solvent present in HSQ, that is being spun as second and subsequent layers, absorbs into previous layers causing them to partially reflow and combine with material being spun. This causes the thickness of the following layers

to increase only marginally. This can be prevented by the deposition of intermediary layers between subsequent HSQ spins, that would prevent solvent reabsorption in the previous layers. SiO_2 was decided upon for the separation layer as it is easy to deposit and since it is structurally similar to the hard baked HSQ preventing potential issues that could emerge from different temperature expansion coefficients in the repeating sequence of layers. Results of this approach can be seen in the SEM cross section of three layers of HSQ separated by a thin layer of SiO_2 in the Fig.4.5.

On the left of Fig.4.6, one can see zoomed out SEM pictures showing whole device and on the right a zoom in on the devices corner with thickness measurements presented. The depth of etch in these devices was setup for $2.5\mu m$ in order to investigate a more challenging case for planarisation. As can be seen the best results are achieved for the samples with the smallest radius meaning that the lowest amount of HSQ is still being left on top of the mesa after spin. This amount grows steadily as the radius of the device increases, for example as presented in Fig.4.6 the thickness of HSQ in the middle of the device reaches $518nm$ in the center of the $10\mu m$ radius device, while for the $25\mu m$ device this value reaches $1.2\mu m$. This build-up of HSQ increases with increasing size of the mesa and decreasing depth of an etch. As for the overall quality of planarisation for leveling purposes it can be observed in Fig.4.6 (right), that even though HSQ reaches the mesa height providing a smooth lead up to its top surface, creating a gentle plane on which it would be easy to deposit a continuous layer of metal, in the region distant from the mesa it only reaches $1.22\mu m$ which is only half of the mesa height. This could prove a challenging issue if a Radio Frequency (RF) optimized ground-signal-ground architecture was incorporated in future designs as the top contact should be positioned at the same level as the top contact of the device.

In order to mitigate some of these issues an etch of $1.2\mu m$ depth was used for the devices in Gen12. This would result in the slight increase of the material build up on the mesa surface, but in return it results in the thickness of HSQ being more uniform across the entire sample in the areas in between devices as well as an ability to achieve an acceptable quality of planarisation with just one layer of HSQ providing a significant decrease in the time required for processing. A shallower etch also leads to less exposed surface on the sides of the mesa, therefore decreasing the influence of side wall passivation on the overall device performance.

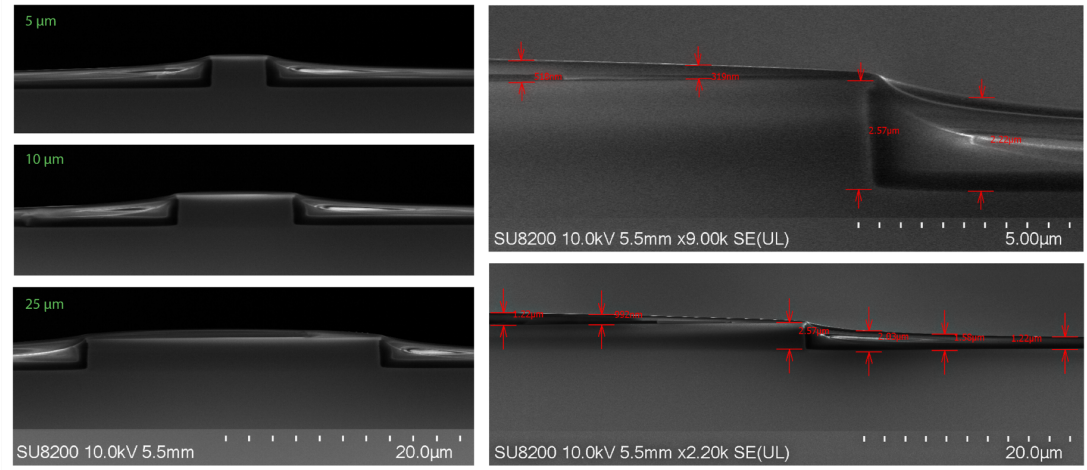

Figure 4.6: SEM pictures of two layers of HSQ spun on top of test structures. On the left - comparison of spin on 5, 10 and 25μm devices. On the right a zoom in on the corners of 10 and 25μm devices.

A via-hole in the HSQ and passivation is then opened where the metal contact is deposited. A bond pad connecting the contact area and providing it with an area large enough for probing and bonding is then metalized.

The optically active area of the device is then capped with a 165nm of silicon nitride, that would serve as an anti-reflection coating since for this thickness it would prevent reflection of more than 90% of incoming light at wavelengths of 1310nm and 1550nm which will be predominantly used in the optical measurement.

Lastly a metal contact is deposited at the bottom of the chip, providing an electrical connection to the header package after the sample is mounted on top of it for measurements.

4.2 Fabrication of Generation 12 devices

Details of the fabrication steps for a device from Generation 12 will be described in this section.

Processing for the Gen12 devices begun with preparation of wafers. Since a localized charge sheet design was chosen the wafers required various preparation steps. Processing begins with a highly n doped 550μm Si (100) 6" wafer with a 1.5μm thick layer of i-Si epitaxially grown on top. The first step of processing is the creation of align-

ment markers. This has not been a problem in the wafers up to this point, since the charge sheet was uniform across the wafer, the actual positioning of the etch layer did not matter as long as the alignment was being kept with that layer. In the case of a selectively doped charge sheet, it was imperative to have a mask incorporating the alignment markers from the very beginning. In later stages, these markers were the only way to judge the positioning of the specific doped areas. The markers have to be visible and precise on the wafer surface even after subsequent deposition and cleaning steps. For the later simplicity of use for the chips, sets of photo lithography markers were fabricated for the wafer size processing (like markers for the wafer size charge sheet doping photolithography) and the photo lithography processing. These markers were positioned both in the $1cm^2$ chips themselves in addition to general markers for the wafer in order to achieve the best possible alignment for the processing. Additionally, on a chip scale sets of markers were placed for positioning and alignment for E-beam processing in case such processing would be required to increase flexibility of the chips as a potential base material for incorporating future designs.

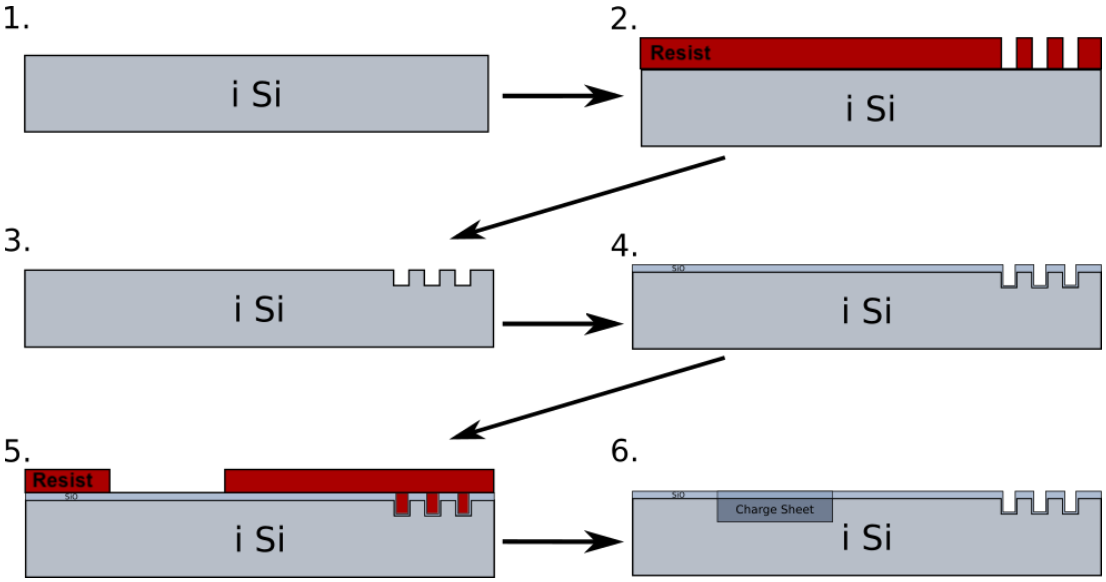

Figure 4.7: Schematics representing processing done on the Si wafer with selectively doped charge sheet.

Firstly, the wafer was cleaned in acetone and IPA followed by the SPR220 photoresist being spun in an automated spinner with a $10mm$ Edge Bead Removal (EBR). EBR guarantees that there is no build up of material at the edges of the wafer providing

that it will be in full contact with the photolithography mask at the later stage. A 10min wait is incorporated to allow for the resist to settle, before a 90s bake on the $118°C$ automated hotplate. The wafer is then exposed with Suss MA8 mask aligner at 440 mJ/cm^2 proceeded by 45min wait. Another bake on the $118°C$ automated hotplate for 90s is performed next and followed by 10min wait. Lastly photoresist is developed at the automated developer with a CD26 photoresist developer. For the first 60s the wafer spins with continuous flow of the CD26 on top of it . A fresh resist developer is then put on top of the wafer and it stays stationary for 30s with only a small agitation, the developer stays on top of the wafer during this step. The wafer is then spun at high speed removing the used developer from the surface of the wafer. This 30s subprocess is then repeated 2 more times. Both gentle agitation, which has been programmed into an automated developer as slow short spins with a change of direction, and additional developments were added as a measure of improving the overall development quality. Development problems for wafers without these steps can be attributed to the resist developer locally, chemically combining with photoresist which greatly diminishes its ability to interact with the exposed area (which is mitigated by introducing fresh developer at every step), and not being able to penetrate small features (which is being resolved by agitation). To remove developer from the wafer surface and stop its further interaction with the photo resist this was followed by a deionized (D.I.) water rinse that is also performed inside the automated spinner. In order to clear out any resist residue potentially left after development, the wafer was ashed in RIE80+ at 20sccm of O_2, 150W and 20mT for 10min. Markers are then etched in PlasmaPro 100 Estrelas with SF6/C4F8 = 50/50 sccm, Coil/Platen = 600/10 W (LF), 11 mTorr at $5°C$. The wafer is then ashed using the same RIE80+ recipe as described above. Though initially thought of as a high-quality process, the markers etched with it were of poor quality. This made performing alignment on later stages challenging. It is believed that this problem with an etch arose because of machine failure that resulted in the full shutdown after performing etcher. Leftover photoresist is then removed, first in the Acetone followed by IPA ultrasonic bath and then (to achieve best possible clean) in the Solar Semi cleaning cabinet with a solution of H_2SO_4 and H_2O_2 commonly referred to as a Piranha clean.

With markers in place one can proceed with selectively doping areas that would serve as a charge sheet in the full device. In order to achieve a selectively doped charge sheet, areas around it have to be masked to prevent ions from penetrating. Additionally a thin layer of SiO_2 would have to be deposited directly on Si surface to protect the Si proper from the impact damage of the ions. This idea along with the selection appropriate values for doping are explained deeper in the simulations chapter 4. The 10nm of SiO_2 were deposited with a plasma-enhanced chemical vapor deposition tool (PECVD) with a 3s of SiO_2 recipe proceeded with standard Acetone/IPA clean. After that a photolithography process using SPR220 photoresist was conducted as described in the previous paragraph but utilizing a different photolithography mask. During this process, photoresist is developed out from the areas where the charge sheet will be located, this allows for selectivity of the doped area since thick photoresist like the one used here would prevent any incoming ions from penetrating into the Si. Next, the wafer is then ashed in RIE80+ as described in the paragraph above and sent to the Ion Beam Services for doping implantation.

After successful doping the layer of the photoresist that acted as a mask for the implantation is removed with a regular Acetone/IPA clean. To insure cleanliness this was followed by the Piranha clean in the Solar Semi. The wafer was then forwarded for the activation anneal in the Rapid Thermal Annealer for a 30s bake at $950°C$. This process is often referred to as Ion Implantation Damage Annealing and is performed to recrystallize the amorphization damage from the implantation process. Also due to high temperature of the anneal process and movement caused by it, within the substrate vacancies are generated which, enables movement of the doped implants from interstitial to substitutional lattice sites. This results in ions releasing carriers into the valence band or conduction band, therefore making ions electrically active, which changes the properties of the implanted region. The random nature of the annealing process causes a varying number of implants to be active as well as making an accurate prediction on the final doping of the selected area impossible. To insure that a value close to the preferred doping is achieved a range of wafers with planned dopings of $1 \times 10^{17} cm^{-3}$, $2 \times 10^{17} cm^{-3}$, $3 \times 10^{17} cm^{-3}$, $4 \times 10^{17} cm^{-3}$ and $5 \times 10^{17} cm^{-3}$ were processed. More information on doping calculations can be found in the simulation chapter 4 of this thesis.

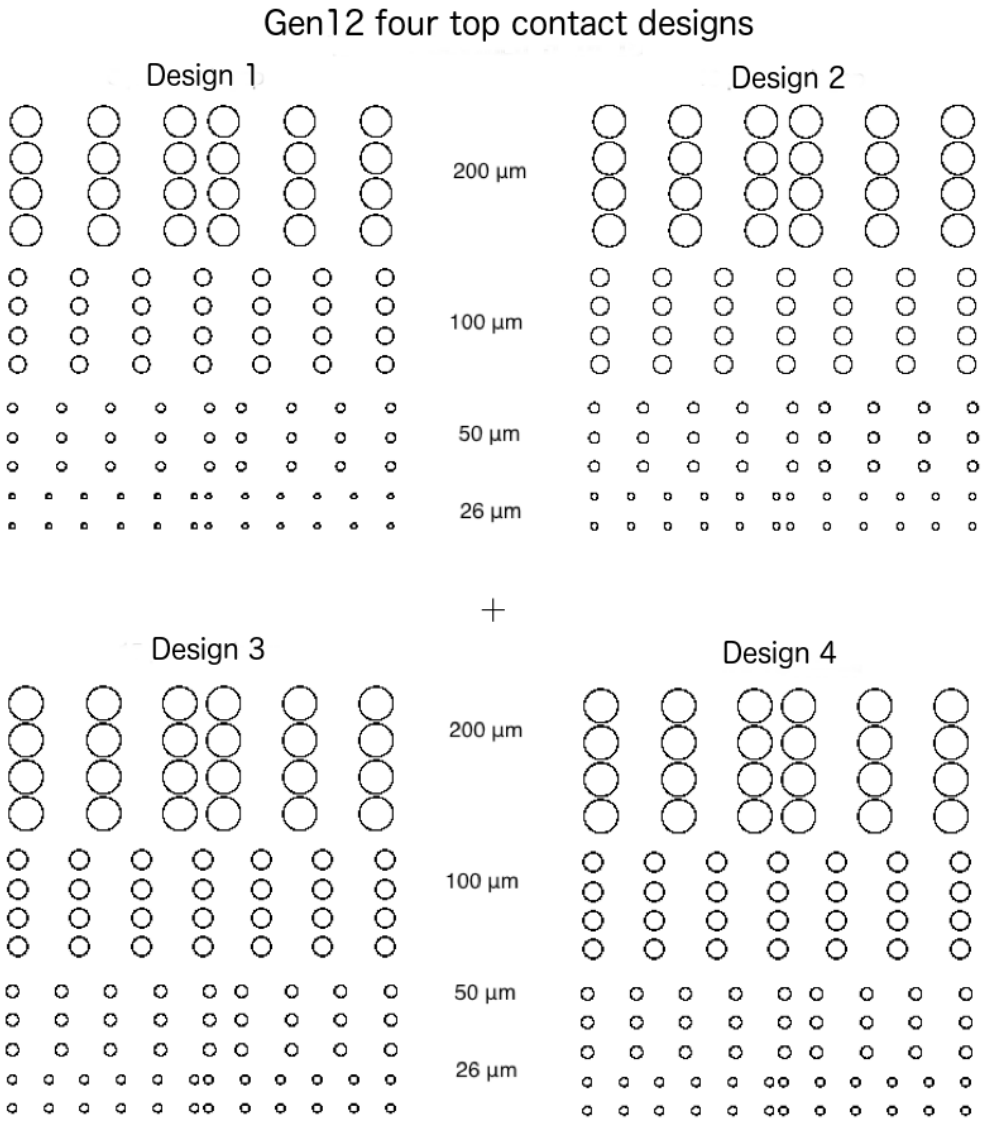

Figure 4.8: Differences between quarters in a Gen12 chip

After dopant activation the protective layer of SiO_2 is stripped from the surface in the Solar Semi with RCA1 and RCA2 cleans. The wafer is then sent to the semiconductor company IQE which performs Ge growth on top of the wafers with a selectively doped charge sheet as well as in-situ doping of the topmost layer of Ge as grown to exhibit a heavy p++ doping for improving ohmic contact between it and a metal con-

tact layer. With Ge growth completed, the wafer is then coated in a protective layer of photoresist and sent to be diced with a diamond saw into $1cm^2$ pieces, that will be used as a base for chip-scale processing. Markers that were etched earlier act as guidelines for the sawing process.

Fabrication on the chip-scale begins with defining the top contact etch into the thin p++ Ge layer on the very top of a wafer. As stated in the simulations chapter, this is carried out in a separate step (as opposed to being performed at the same time as an mesa etch for previous generations of devices) to achieve the defined top contact etch as described in the simulation chapter. Firstly, the sample is cleaned with subsequent acetone and IPA ultrasonic baths for 5min each and dried using a nitrogen blow gun after which it is transported to a $120°C$ oven for a 10min dehydration bake. After that a S1818 resist is spun on top of the sample at 4000rpm, 20000 ramp for 30s. A hotplate bake was then performed, which consists of placing the chip on top of a hotplate designated for a given resist, used resist side up, and leaving the chip on top of it for a given amount of time. This so called soft baked was carried out on an $85°C$ hotplate in the spinning room thermal processing area for 2 min. It was then exposed for 4.4s with a MA6 photolithography tool and developed for 75s in MIF319 developer with a 75s RO water rinse afterwards. An optical microscope is then incorporated for a preview of the development quality. If iremoval of the resist in the acetone bath was not satisfactory then the whole process is repeated. If the resist developed correctly then the sample is ashed in the TEPLA microwave asher for 2min at 150W of power. Next, the chip is submitted to the STS dry etch machine for 26s of MMmetal recipe. This etch had to be carefully investigated in advance to ensure that it was consistent enough to be able precise knowledge of how deep it is going to be at a given time. Because of the top contact in this design it is important to etch past it to prevent the electric field from spreading to the edges of the mesa. We also do not want to etch too much into the Ge as it would cause the appearance of a free standing mesa on top of our device. All of this combined with a p++ Ge layer being only 50nm thick results in the necessity for the etch process to be precisely controllable and slow. In this case 26s MMmetal etch results in an etch depth of around 70nm, which was decided upon as a precaution measure to ensure that we are always etching p++Ge away as well as taking into account the fact that due to the probabilistic nature of doping p++Ge

layer might be slightly thicker than the requested 50nm. After that the etch depth is measured in Dektak and the chip is ashed in the TEPLA asher at 600W for 2min to prevent any hard-baked resist from remaining on the surface.

The next step of chip fabrication is the mesa etch. Starting with a 5min acetone/IPA ultrasonic bath and proceeded with the same photolithography process as for the Ge top contact etch. After an ash in the TEPLA microwave asher at 150W for 2min the sample is submitted for for dry etch in the STS. This recipe utilized SF6 and C4F8 gases at 30 and 90 sccm respectively with Coil and Platen at 600/12 W, pressure of 10 mTorr and temperature of $20°C$ for about 4min 20s. For this etch it is required to use a reflectometer which while pointed at the etched surface measures reflectivity of the surface and produces an interference pattern indicative of the medium being etched, allowing an easy way to terminate the etch without having to rely on timing itself. Stopping 40s after crossing from etching Ge to Si results in the total etch depth of $1.2\mu m$ which means that etching past the Ge layer into the Si for $0.2\mu m$. This relatively shallow etch is utilized in order not to expose too much of the Si side wall surface that could potentially require separate passivation process and make it easier for planarisation. It was also confirmed that, with proper side wall passivation, a varying etch depth into Si doesn't significantly influence the overall device performance. The chip is then ashed with the TEPLA microwave asher at 600W for 2min.

A mesa etch is followed by a surface oxidation, the development for which was presented in the methods chapter 2. One minute of acetone/IPA ultrasonic clean is run before proceeding with the main processing steps. This is followed by the cyclic Hydrofluoric acid (HF) oxide removal. Acid is firstly diluted to a 50:1 concentration, the chip is then dipped inside of this solution for 10s while agitating it up and down. The chip is then placed for 30s in RO water with an up and down agitation. This process is repeated two more times finishing with a 45s RO water dip. After that the chip is immediately transported for oxide growth. This step has to be performed without delays as the native oxide growth on top of the Ge surface happens rapidly under atmospheric conditions, the upper time limit being about 30min. The chip is placed inside a preheated to $550°C$ oxidation tube for 25 min with oxygen flow of 240 l/h at 2Bar. Because of the rapid etching of GeO etching in water, exposure to atmospheric conditions can be quite detrimental to the surface oxide quality, it is therefore important to quickly cap this newly grown oxide with a protective layer. For

this purpose 7nm of AlO_2 was grown on top of GeO_2 in the Atomic Layer Deposition tool at $200°C$. In order to increase the quality of the oxide, a forming gas anneal (5% H_2, 95%N_2) at $350°C$ for 30min was performed.

The next step in processing is surface planarisation, where the regions between the devices are filled with a medium to create a surface of consistent elevation across the chip. Creating such a surface allows for deposition of better quality contacts that will not break because of the high steps between low and high points in the device, as well as the medium serving as a dielectric isolating contacts from the exposed Si surface. Firstly, we begin with a uniform deposition of SiO_2 of 25nm on top of the chip. Neat Hydrogen silsesquioxane (HSQ) is then spun on top of the sample surface at 2000rpm proceeded by a 2min bake on a $90°C$ hotplate. Following that a carbolite furnace is preheated to $100°C$ with a N_2 flow of 50l/h. The HSQ covered chip is then loaded into the furnace and the temperature is ramped up to $400°C$ with a N_2 flow of 150l/h at 2Bar. After reaching the desired temperature the sample is baked for 30min. The N_2 flow rate is then decreased to 50l/h and the temperature controller turned off. After the furnace reaches $200°C$ the sample is unloaded. To achieve better leveling of the surface it is advised to repeat this process once more starting with SiO_2 deposition. After the second run, the sample is coated once more with 25nm of SiO_2.

In order to reach Ge surface for the purpose of contact deposition it is necessary to perform an etch. This etch has to remove layers of Ge oxide, Al oxide and HSQ, from the area where the contacts would be deposited. To do so a passivation etch is required. This processing step follows all the steps for S1818 based photolithography as described above. After ash in TEPLA microwave asher for 2min at 150W, the chip is submitted for the dry etch in the Oxford Instruments PlasmaPro 80 + reactive ion etch system where the removal of HSQ layer is performed. The recipe used for this is the CHF3/AR at 25/18 sccm etch with 200W of power at 30mTorr for 15min. This etch is timed rather than being reliant on interferometry because of the difficulty to place the laser spot on the small area that is being etched as well as AlO_2 acting as a stopping layer for that etch. This means that the chemistry involved in the etch does not interact with the AlO_2 layer therefore, not progressing past this layer. A time of 15min is selected as it guarantees (for the given thickness of HSQ after spin), that all of the HSQ would be removed from the etched area. The chip is then transported to the Oxford Instruments Plasmalab System 100 ICP-RIE (T-gate) to remove the AlO_2

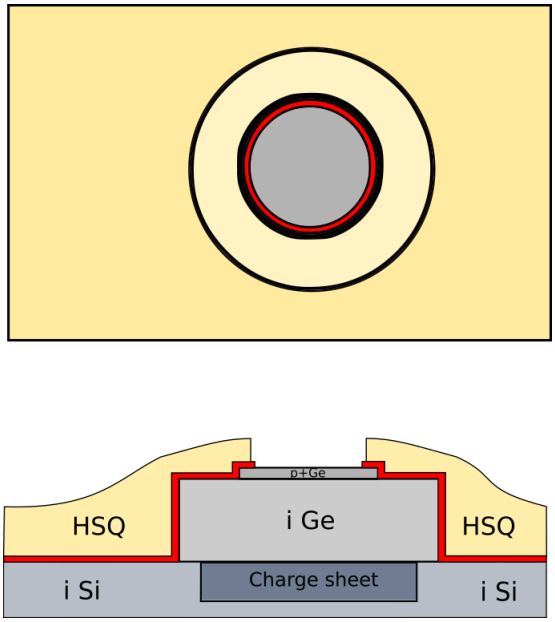

Figure 4.9: Schematic cross section and a top view of a chip after opening via hole down to the p++ Ge region (not up to scale).

layer. An etch utilizing silicon tetrachloride ($SiCl_4$) at 25sccm at 50W, 8mTorr for 10min is performed. After this etch the last thing to be removed from the contact area is a layer of GeO, which is done with a 30s dip in the 50:1 RO water:HF followed by 60s rinse in RO water.

As the path through the passivation layer down to the Ge p++ is opened, we can continue processing with the metal contact and bond pads deposition. First a photolithography process for the metal contact is performed utilizing S1818 photolithography process as described above. Since GeO forms spontaneously on the exposed Ge surface in atmospheric conditions, it is important to perform a native oxide removal before proceeding with a metal contact deposition. This is carried out after the TEPLA ash. A 30s dip in the 100:1 RO:HF solution followed by a 30s rinse in RO water is performed, before immidiately transporting the chip into a vacuum environment of the metalization tool to prevent atmospheric native oxide creation. Metals used for the contact are 10nm of Ni followed by 50nm of Pt deposited in the PLASSYS II thin film deposition tool. Nickel is chosen to create a good ohmic contact with p++ Ge and a layer of Pt serves as a hard metal layer preventing Ni from being damage. Platinum is a good choice as well, because it will not form a native oxide layer on its surface,

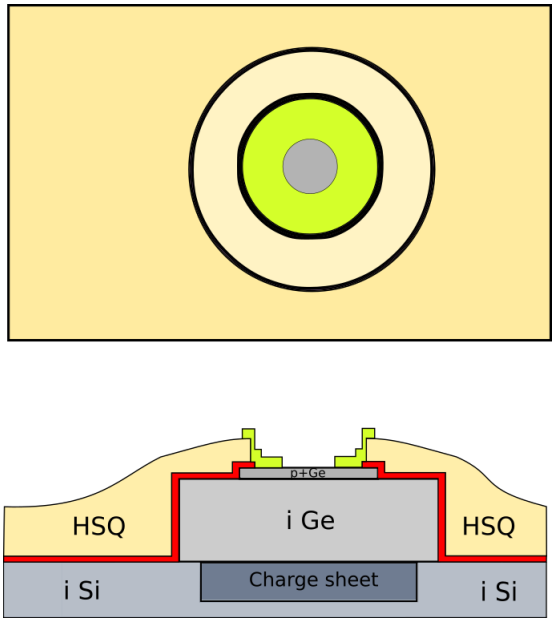

Figure 4.10: Schematic cross section and a top view of a chip after deposition of the top contact(not up to scale).

removing the need for another oxide removal step. Optionally a layer of Pd can be used instead of Pt. After this the oxidation chip is transported to a $50°C$ acetone bath, where it will stay for 1 hour for a liftoff process after which it is gently rinsed in IPA and blow dried after. Usually after metal deposition on the surface a contact anneal is performed to create an ohmic contact, although in the case of wafers used for these chips it is not necessary as the heavy doping of the p++ Ge layer guarantees a high quality of contact without need for an anneal.

After inspection of the top contact fabrication step with a microscope and Dektak we proceed with bond pad deposition. Bond pads are a large, thick layer of metal that provides a means of electrically contacting the sample. Since the top contact is a thin ring structure, entirely located on top of the mesa, it would be extremely difficult to drive a current directly through it even with use of thin tungsten tipped probes in the probe station. To make this possible a larger area is deposited to connect with a top contact ring providing with easier electrical access. Additionally, since a bond pad provides a thick large area of metal, bonds connecting the fabricated chip with a cryostat suitable header package can be easily attached onto it. Processing begins with a 5min clean in the Acetone bath and 5min in the IPA bath with gentle side to

side agitation followed by a nitrogen blow dry and 10min dehydration bake at 120°C oven and an required amount of AZ2070 photoresist is pipetted from the bottle in the fridge and allowed to rise to the room temperature. To promote adhesion of the photoresist firstly a spin of the HDMS primer is performed. The chip is coated with 80:20 HDMS primer and allowed to sit in the spinning cabinet for 20s after which a spin of 4000rpm for 5s is performed. Room temperature AZ2070 photoresist is then deposited on top of the chip and spun for 60s at 4000rpm with a 20000 ramp. This is proceeded with a hotplate bake of 90s at 110°C. After that the chip is exposed with MA6 photolithography tool at the vacuum program setting for 20s. The chip is then post baked on the 110°C hot plate for 60s and developed in the MIF319 developer for 70s with a RO water rinse and nitrogen blow dry. Development is then inspected under the microscope and the photolithography process is repeated if the alignment or development quality is not satisfactory. If the process was successful, barrel ash at 100W for 60s is performed and the chip is placed in the vacuum chamber of the PLASSYS III tool, ready for bond pad evaporation. A 50nm of Ti which serves as a sticky layer promoting bond pad adhesion to the surface and 1000nm of Al forming the bond pad proper. To achieve these thicknesses, Ti is evaporated for 20min at 1A and Al is evaporated for 90min at 1.5A. After evaporation the liftoff process is performed similarly to the contact step but with an acetone bath time increased to 2 hours.

For the devices of this design, a finished chip is mounted on top of the header package with silver paste and the bond pads on its surface are connected with gold wire bonds. The header package is then used for various characterization steps and data acquisition with a driving voltage is applied to the top of the device via a wire bond and the backside of the chip serving as a common ground for all of the devices. For this reason it is important to deposit a contact on the backside of the chip as well. In order not to damage a chip surface, it is coated with a S1828 spun at 4000rpm for 30s and baked for 2min on the 90°C hotplate. To create a good quality contact with a heavily doped backside of the chip a native oxide is removed from it with a 30s 10:1 RO:HF dip followed by 30s RO rinse. The chip is then transported to the PLASSYS IV vacuum chamber for a 150nm Al back contact deposition. Since it is a uniform metal layer the lift off process is not necessary with the sample only require an acetone bath followed by a IPA bath with gentle agitation to remove protective layer of resist.

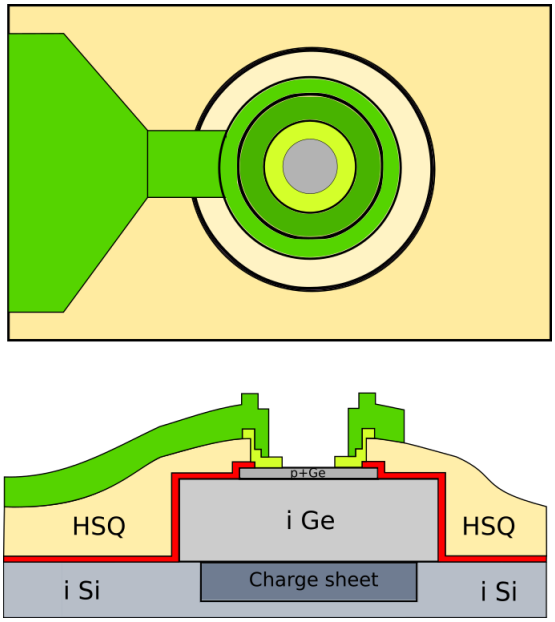

Figure 4.11: Schematic cross section and a top view of a chip after deposition of the bond pads(not up to scale).

The final step of fabrication involves deposition of anti-reflection coating. Firstly the chip is cleaned and prepared with acetone and IPA bath as in previous steps, this is followed with deposition, exposure and development of AZ2070 photoresist. The chip is then ashed in the barrel asher at 100W for 60s followed with a 165nm of SiN deposited in ICP-SiN deposition tool. It is then lifted in a same fashion as for the top contact processing step.

With that the sample is ready to be attached to the header package with silver paste, bonded with gold wire. The initial measurements are performed and after that it is transported to the Heriot-Watt university for the single photon measurements.

4.3 Generation 13 device design description

In this section the general aims and design choices for the Gen13 devices will be discussed. The general approach to the Gen13 was to improve upon the successful devices from Gen12 in the hopes of achieving another breakthrough in the Ge on Si SPAD's performance, although some of the device choices were dictated by equipment availability during the fabrication process.

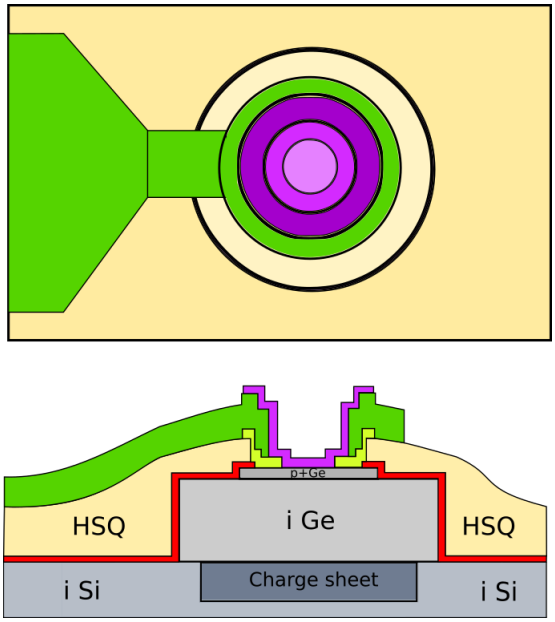

Figure 4.12: Schematic cross section and a top view of a chip after Anti reflection coating lift off process(not up to scale).

One of the biggest unresolved challenges in Gen12, was the poor quality contacts go-

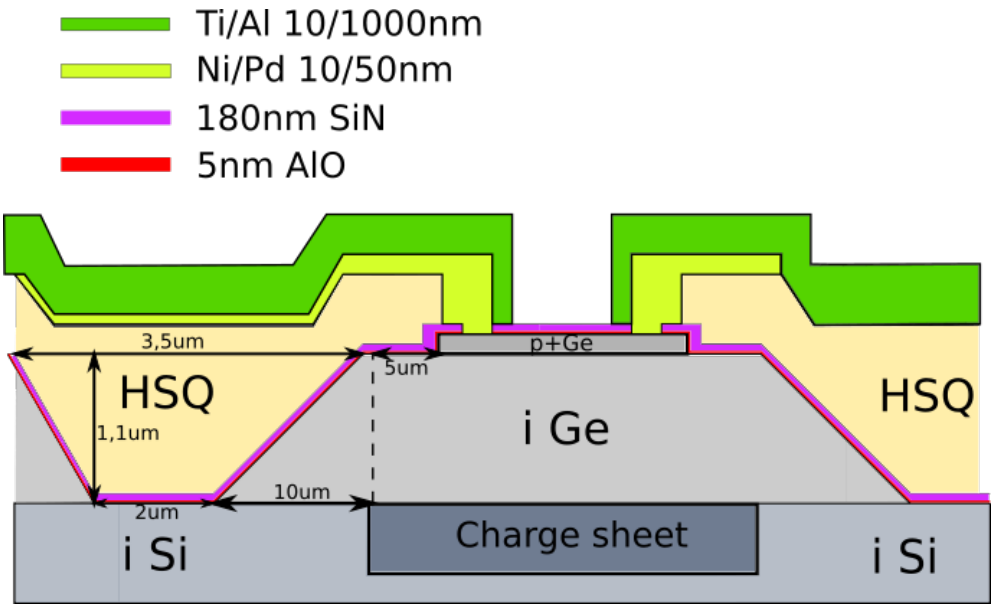

Figure 4.13: Cross section view of the fully processed Gen13 device

ing down to the 25μm and some of the 50μm devices. After performing some tests on

these, it became apparent that the problem arose from the HSQ planarization process. As mentioned in the previous section on Gen12 fabrication, after SiO_2 deposition, HSQ was spun on top of the devices. However, due to the viscosity of HSQ the spin did not form a uniform layer over the whole surface, but rather caused a build-up on top of the mesa and dipped into canyons around it as seen in cross-section in Fig.4.14. This effect was discovered to be dependent on the size of the single pixel mesa. Build-up became thicker as the mesa radius was decreased. This became particularly problematic after the HSQ removal from the active area of a mesa. As shown in Fig.4.14 where the lighter area symbolizes part of the HSQ that is being removed in the via hole etch process. After the HSQ removal, a sharp edge is created going down from the planarization layer to the device. The size of this step is dependant on the device radius and it increases with decreasing device radius. The size of this step was estimated to be 450nm for the $25\mu m$ devices.

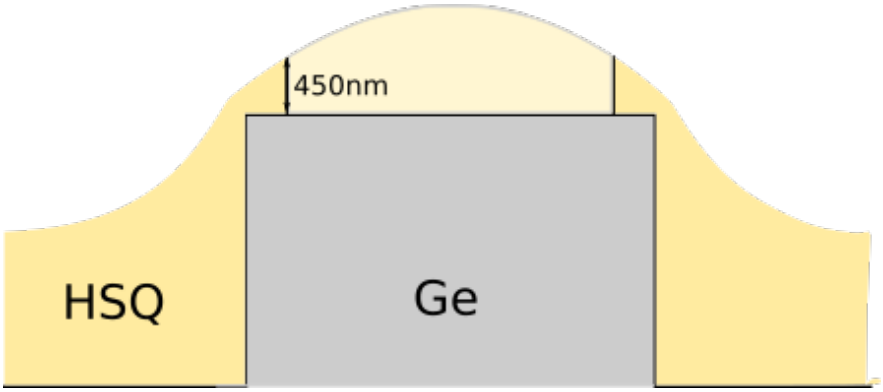

Figure 4.14: Cross section view of the Gen12 device after spinning HSQ on top. Brighter area corresponds with an area where HSQ will be removed in the via hole etch.

If a thin metal contact layer was deposited over such a step, metal layer would break its continuity while going from the top of the step to its bottom due to the steepness and size of the step. Such a break occurring during metalization was the most likely cause of failure for the smallest devices, especially since these were mostly displaying open circuit-like behavior in their IV characteristics. Since the smallest devices bear a high likelihood of much higher performance than their larger counterparts, this problem had to be addressed with high priority. It was decided to try to eliminate this problem by creating a chip design that would not require surface planarization. A long-term

solution for the selected area growth of Ge in SiO wells was suggested, though since putting it to life would require a significant amount of process development another approach (with usage of SPAD3 wafers from Gen12) was created. As stated in the device description section for the Gen12 above, it was not possible to achieve fully planar devices because of device-to-device leakage current, therefore an etched mesa approach from previous designs was adopted. However, mesa isolation could be, achieved without the need for a full etch. A way to electrically isolate neighboring devices is required to prevent the leakage currents. Therefore it was decided that an approach involving an isolation etch should be implemented. This etch would create a trench encircling the mesa in a way that the full etch would, cutting into the Si layer and therefore providing a device-to-device isolation, as shown in Fig.4.13. To decrease the chance of the deposited layers continuity and potential spikes of E-field at the corners of the mesa, a sloped-wall variation of the trench etch was developed. A description of this process and its development is presented in detail in the methods chapter 2 of this thesis. To improve the continuity of bond pads and to have an additional dielectric layer underneath it, a HSQ trench filling process was developed.
The next variation to the Gen12 processing was removal of the SiN liftoff process. Regardless of the generally good results it was producing, it was observed that the anti-reflection coating deposited in such a way tended to be irregular in thickness, resulting in some regions on the mesa device having a less effective anti-reflection coating. This process could be considered as a non-standard approach, and since aim of this project is the development of a process that could be easily adapted for the CMOS production line, therefore this had to be significantly modified. A layer of SiN of correct thickness for the anti-reflection coating purposes for wavelengths between 1310nm and 1550nm could be uniformly deposited on the sample surface. Initial tests on this uniform SiN layer were carried out before the sloped process for the trench side wall was finalized. There are two points in the fabrication process where the uniform SiN layer could be incorporated, either after Ge passivation and capping or after the HSQ trench filling process.

Focusing on the first case, it was speculated that for narrow enough trenches, a uniformly deposited layer of SiN would run smoothly above the trench without breaking. Trenches of thicknesses ranging between $300nm$ and $5\mu m$ were investigated. After taking a cross-section of the test structures and inspecting them under the SEM, it

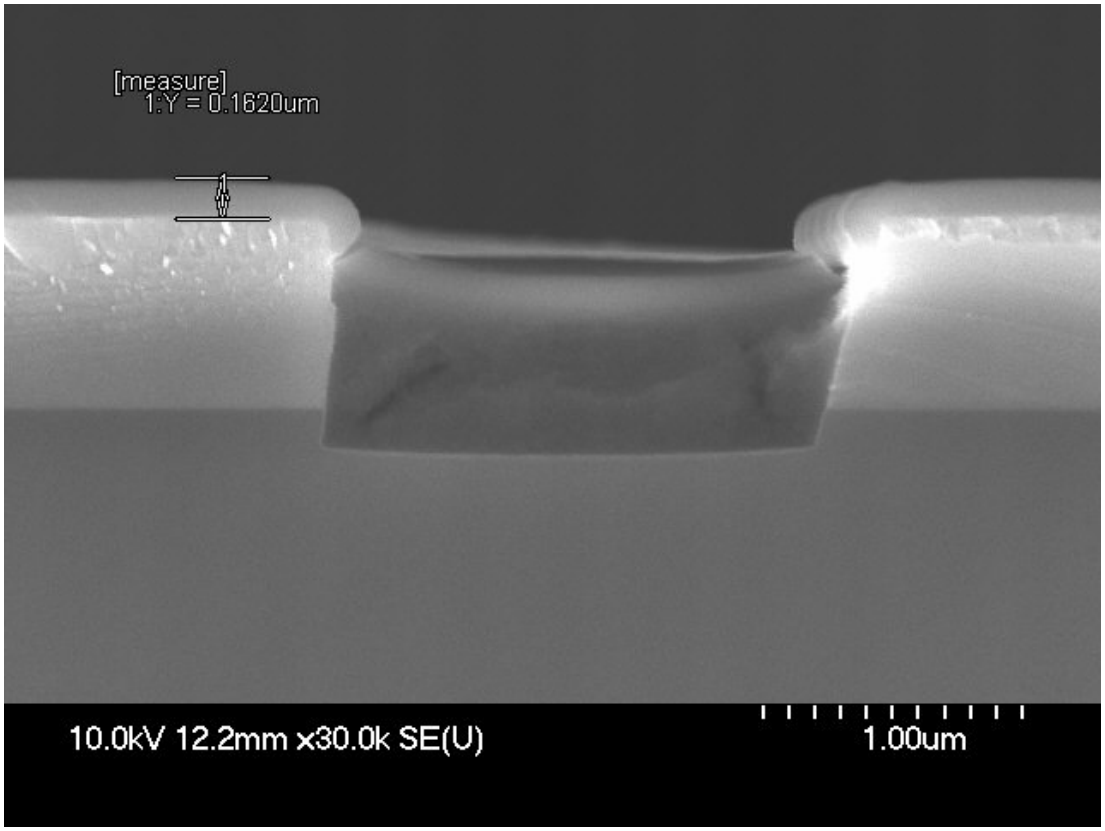

Figure 4.15: Cross section view of the uniform SiN deposition, after the HSQ trench filling.

was observed that regardless of the trench wideness, a uniformly deposited SiN layer would break while going from one edge of trench to another therefore not connecting them. Instead the part that was expected to be a connector between two edges of the trench was deposited at the bottom of that trench. This layer was also not continuous on the trench side wall. The second approach, of depositing SiN after HSQ trench fill and etch back was then investigated. This approach did not result in success either. As shown in Fig.4.15 despite the good uniformity along the surface of Ge and HSQ filling the trench and providing a good support for the SiN layer, it is not continuous. It can be seen that near the edges,the layer of SiN curls up to the sides creating a "beaking" effect. It was therefore decided to retry the first method but with a sloped side wall as development was entering its last stage. Again, the uniform SiN layer was deposited on top of the Ge oxidation layer and capping, but in this case the side wall of the trench

was at an angle.

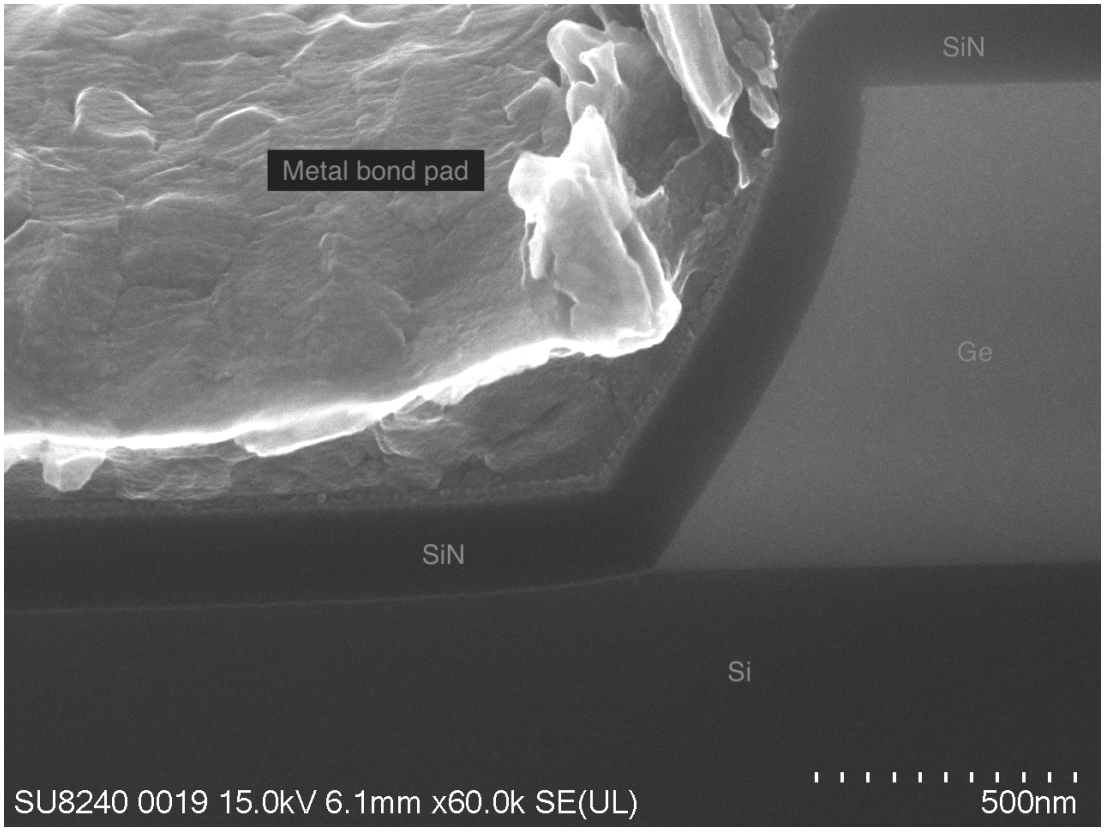

Figure 4.16: Cross section view of the uniform SiN deposition on the sloped side wall of the isolation trench.

Figure Fig.4.16 shows that the SiN layer, even though a bit thinner than on the horizontal surfaces, remains continuous across the sloped wall of a trench. This method, being CMOS compatible also provided an additional dielectric isolation in the regions where bond pads would be located and was therefore implemented for devices in Gen13. The last difference to the Gen12 design were different uses of the 4 quarters in a chip. Quarters 1, 2 and 3 contain a design with different sizes of the spacer between a charge sheet and a trench. It was suggested in simulations that a $3\mu m$ wide spacer should be enough to keep the Ge sidewall far enough to diminish its influence on the device performance. Variation in the size of the spacer would provide information about the real influence of the sidewalls on the overall device performance. Additionally this could potentially provide information of the contributions to the dark counts from the

Ge bulk. If the contribution is significant then future designs should incorporate a spacer of this minimum width to reduce the overall bulk size of the device. If, on the other hand, this contribution is either minimal or reaches a plateau after a certain size then this would allow for fabrication of a fully planar device with only the isolation etch at its extremities in the next generation. This in turn would significantly reduce the time required for full processing, and increase devices robustness.

4.3.1 HSQ trench filling

In this section I am going to discuss development and reasons behind design decisions for trenches etching and filling. Design of a circular trench that cuts through Ge and into the Si was decided upon while developing devices from Gen12 that were produced with locally doped charge sheet. There was a need for creating an isolation around the device to prevent leakage of electric current with its neighbors. More in dept analysis of that will be presented in the design section for the Gen12 devices.

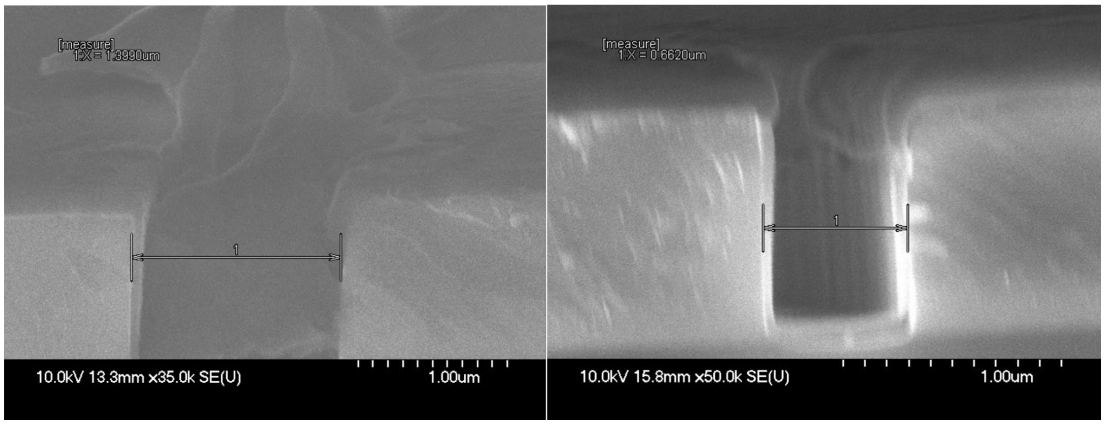

Figure 4.17: SEM image of a cross section through the trenches of widths $1.3\mu m$ and $0.6\mu m$ after the SiN deposition

A range of test samples with dry etched trenches with widths ranging from $0.4\mu m$ to $5\mu m$ were produced (with lower limit being dictated by a resolution of photoresist used and upper limit dictated by a distance at which we were sure no bridging would occur). Since these were one time use test samples e-beam lithography was utilized. Trench widths below $0.4\mu m$ were attempted but their they did not met fabrication requirements. Since to etch through Ge an etch of at least $1.1\mu m$ would be required,

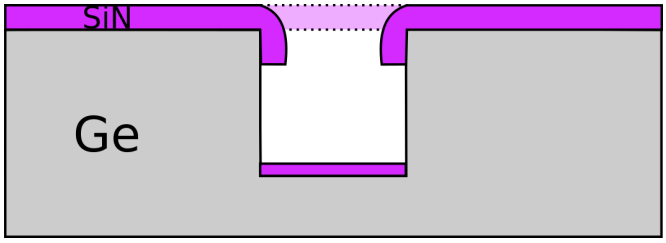

Figure 4.18: Diagram explaining the images above. Solid line representing the actual profile fo SiN and dotted line presenting and expected bridging effect

a thick enough layer of resist would be necessary for the etch. With increasing the thickness of the resist, however, a feature resolution decreases, meaning that very small elements of the design, like trenches below $0.4\mu m$ would not be possible to achieve.

These samples were then used for range of tests, first of them involving silicon nitride deposition for the purposes of bridging the trench. Since the devices have to be isolated, and we do not want to increase the surface around active area too much to avoid contributions to the dark currents from the Ge bulk the region between active part and the trench cannon be made large enough to incorporate the bond pad. This means that the bond pad would have to be entirely located after the trench, and connecting to the and the mesa area by passing it. If we were to deposit the metal with a trench left without any processing a metal would be deposited inside the trench, filling it, and connecting its inner and outer parts, leading again to the appearance of leakage current between devices.

To avoid this issue a method of trench bridging was though upon. It was initially assumed, taking into consideration known properties of deposited layers of silicone nitride, that during the deposition it should create a bridge between two edges of a trench allowing for the subsequent layer of metal to run on top of it without electrically connecting the surface. This desired effect is presented in Fig.4.18 with dotted line and lighter color. Sadly this effect did not occur. Instead during the deposition silicone nitride broke while crossing the trench creating small beaks covering corners of the trench and small amount of it being deposited at its bottom which can be also seen in Fig.4.18 represented with solid line and darker color. This occurred regardless of the trench thickness as can be seen in SEM cross section images Fig.4.17 where on the left

is presented a trench of $1.3\mu m$ in width and on the right 0.6μ wide trench. It was clear that a different approach would be necessary.

It was decided that instead of trying to bridge the trenches one should attempt to fill them. A suitable chemical for that should be a dielectric to provide isolation for the high current transferring bond pads, have a low surface tension during the spin to allow for the trench filling, known process turning it a solid to prevent leaking from the trenches, being relatively easy to remove providing access to the top surface, not deteriorate in the ambient atmosphere and posses similar thermal expansion coefficient to both Si and Ge to prevent cracking and tension during the thermally dependent measurements. A chemical filling most of these requirements was found out to be hydrogen silsesquioxane (HSQ) an e-beam lithography resist.

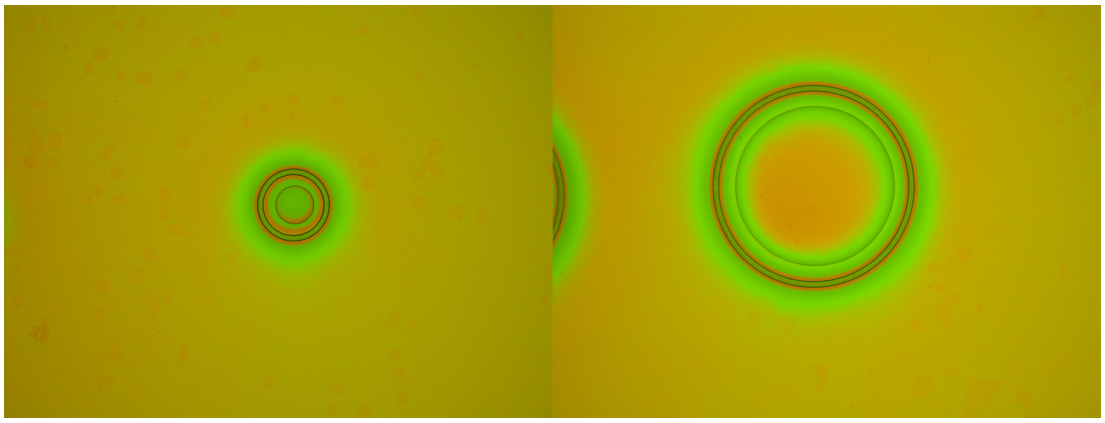

Figure 4.19: Top view microscope image of two samples after Ge P+ and trench etches after spinning the HSQ, but before the reflow process. On the left device $26\mu m$ in diameter and on the right device $50\mu m$ in diameter.

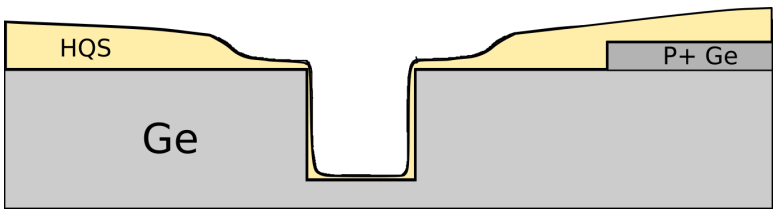

Figure 4.20: A non up to scale diagram showing a cross section through the trench and part of the P+ etch after spinning HSQ

A series of tests were performed on the trench filling with HSQ and previously prepared samples with different trench thickness, spin speeds, and HSQ dilutions. In all the cases a behavior was observed as can be seen in the microscope picture and corresponding diagrams in 4.19 of $26\mu m$ and $50\mu m$ in diameter devices with a $1\mu m$ deep $2\mu m$ thick ring like trench. This has also been represented in a cross section diagram form in the 4.20. As HSQ is spun on top of the sample, it mostly gathers at the top surface with only a small portion of it resulting at the bottom of the trench. Presented samples had a $50\mu m$ deep P+ Ge etch in the middle of a circular trench and it was observed with a stylus profilometer measurement of the sample surface that the HSQ creates a build up of a material in a dome form on top of the P+ etch surface as presented on the diagram in 4.20. This build up varies with a P+ etch - increasing with increasing diameter of the etch. An area around the trench from which HSQ was pulled to fill it can be seen as a green halo. This behavior remained largely unchanged with varying HSQ parameters and the trench thicknesses although it was observed that the trench filling was of a slightly better quality for the thicker HSQ and narrower trenches. A sudden change in color on top of an area of the trench suggest that a layer of HSQ in it is indeed really thin, which was confirmed with a more detailed Dektak investigation. It was apparent that there was a need for investigating a different type of a chemical, or introducing some intermediate steps that would improve the trench filling.

A process that promotes HSQ trench filling has been developed with a main principle behind it being promoting HSQ flow. Here we will focus on the general principles of that process with a description of implementation in the following fabrication chapter. Initially an effort to promote flow was attempted at the spinning stage, with dilutions of HSQ, sadly it did not produce a desired effect as for high dilutions a majority of HSQ would be removed from the sample surface during the spin, resulting in not enough of the material left to fill in the trench. An approach with the HSQ flow promotion was then attempted after HSQ was already spun on the sample surface and then it was quickly dipped in methyl isobutyl ketone (MIBK) which is a chemical used for diluting HSQ. This resulted in a very non uniform behavior of the HSQ on the sample surface that was impossible to exert control over. Lastly a more gentle variant of that process was being attempted, where the HSQ covered sample would be introduced into the MIBK rich atmosphere in hopes of a more gentle flow promotion. After a wait of

couple of hours there was no extreme changes to the trench filling but it was observed that seemingly some small amount of the HSQ did indeed flow to the bottom of the trench. It was decided to perform that test again leaving the sample for an over night reflow in the MIBK rich atmosphere.

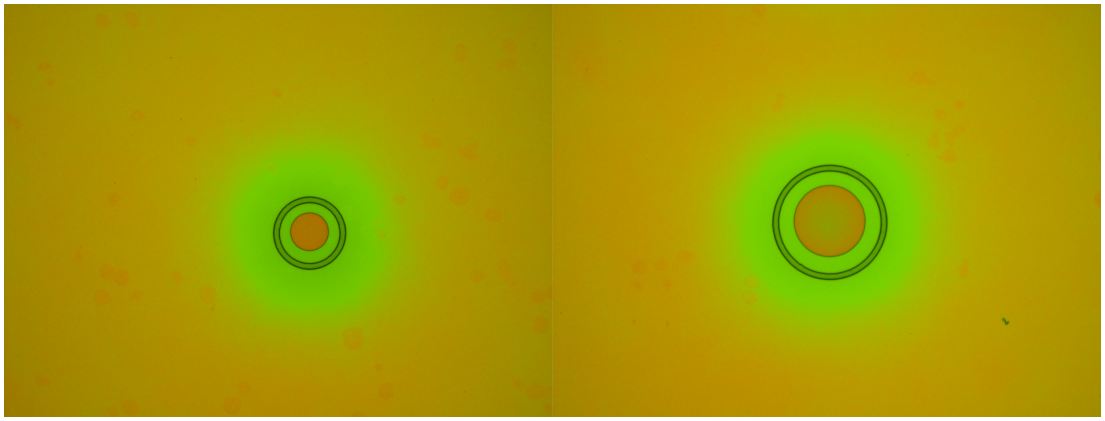

Figure 4.21: Above - top down microscope image of two samples after Ge P+ and trench etches after spinning the HSQ, and after the reflow process. On the left device $26\mu m$ in diameter and on the right device $50\mu m$ in diameter.

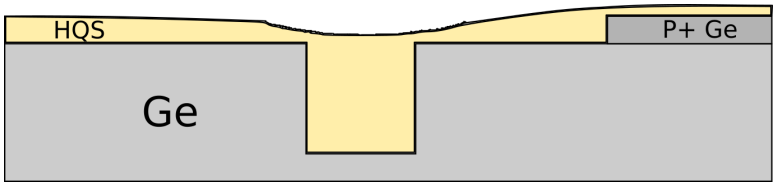

Figure 4.22: A non up to scale diagram showing a cross section through the trench and part of the P+ etch after spinning HSQ and performing a reflow process

Long reflow time allowed for the HSQ to reabsorb greater amount of MIBK therefore promoting its flow. As can be seen in the microscope picture of the same devices taken after the night of a reflow presented in the Fig.4.21. It can be observed that the discoloration present on top of the trench has been smoothed out to create a layer of comparable thickness above Ge surface to the HSQ outside of it. An increased size of a green halo on the outside of the trench this indicates an increased radius at which HSQ gradient has been affected pulling material into the trench. Top of the P+Ge has been positively affected as well, as can be seen from the color change in respect to the

before reflow microscope image. For cases of devices of various radii a doming effect on top of the Ge P+ etch was reduced creating largely flat surface across the circle. This was especially dramatic change for the smallest devices on top of which layer of HSQ was much thinner than in other cases, presumably due to lot of the material from that dome being redeposited into the trench.

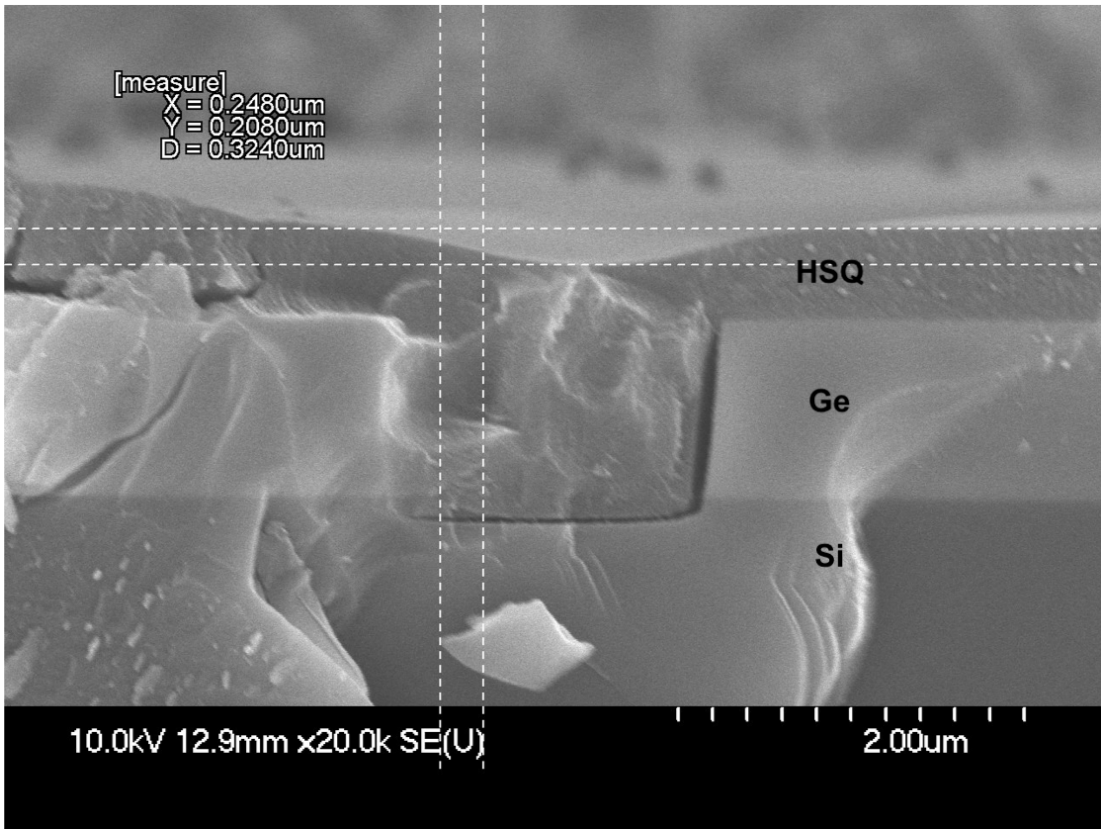

Figure 4.23: Sem picture of a cross section of a trench after HSQ filling and reflow.

A cross section of the trench was taken and imaged as can be seen in the Fig.4.23. Trench presented in here was $2\mu m$ wide. The roughness of the surface of the cut is due to a bad quality of a cleave rather than material itself displaying roughness. It can be seen that even though the HSQ surface still exhibits a dip in a place where the trench is located, it is significantly smaller than in case of a sample without reflow exhibiting an exact property that was aimed to achieve. Thinning of HSQ layer on top of the P+ Ge etch is beneficial as well as it would result in a smaller drop after etching a via

hole for the contact, therefore improving their quality which is an important quality especially for the devices of smaller diameters.

Various test samples were produced in order to achieve best possible quality of the trench fill. Firstly different times for the reflow were investigated. It was observed that after 6 hours HSQ exhibits the same properties as after a full over night reflow. For the fabrication purposes, however, an overnight process is more convenient as with it we are not spending a whole day of the clean room processing on just waiting for the reflow process to finish. Different chemicals to create flow promoting atmosphere, starting with acetone, IPA, TMAH and CD26 with varying temperatures of the process for acetone and CD26, were investigated. None of these chemicals, however, managed to reproduce the trench refill to a quality achievable in the MIBK rich atmosphere.

Varying trench widths were investigated as well. With its width increased in increments from $0.6\mu m$ to $6\mu m$, one observed that increasing the width above $3.5\mu m$ had a diminishing effect on the trench filling, causing the resulting dip of HSQ on top of the region where the trench was located to drop below the top surface of Ge. With decreasing trench width the surface dip of HQS above trench location seemed to decrease causing it to become fully planar for the trench widths just below $1\mu m$. With that information at hand, it was decided that the width of the trench for the final design should be placed at $2\mu m$ as seen in Fig.4.23. Even though at this width the HSQ surface still exhibits a dip above trench location this dip is small enough not to cause problems during processing, moreover this size of a trench allows for utilization of photolithography process for its creation (as any smaller size would be below this processes' achievable resolution for such a deep etch), decreasing significantly time and cost of the subsequently produced live devices.

Lastly different HSQ thicknesses were investigated. For various dilution during, even though initially they perform better than their neat counterpart and produce less material on top of the Ge P+ surface the resulting layers are too thin, not providing enough of the material to fill the trench, resulting in the area around the trench where all of the HSQ was redeposited into the trench leaving nothing on the top surface. This is not a desirable effect since resulting filling is not fully capping the trench and HSQ

depleted area would not provide an electric isolation from the Ge surface for the bond pads. For the neat HSQ thicknesses between 360 and 600nm were explored with 360nm case presented in the above Sem image Fig.4.23. With increasing HSQ thickness dip above trench was diminishing, achieving fully planar profile at 600nm thick spin. This however has resulted in the really thick layer on top of the Ge P+ etch. This could lead to a significant hight drop for the contacts inside etched via hole decreasing their quality. Therefore a spin thickness of HSQ of 360nm was decided upon as together with $2\mu m$ wide trench it was located in the middle of all the filling requirements without creating additional fabrication issues.

4.3.2 Sloped trench

Devices in generation 12 were created on a premise of trying to create a smooth planar like structure with uniform covering of silicone nitride on top of the germanium passivation layer that would serve as capping for Ge oxide, dielectric providing electric separation for the bond pads, sticky layer promoting bond pads adhesion and anti reflection coating. This design choice was decided upon in order to avoid non CMOS standard processes of SiN lift off and HSQ reflow in addition to reducing the overall number of fabrication steps and therefore time required for full device processing.

However, as was seen in the previous section on effort to create bridging over the trench, in the case of vertical etch, SiN layer was not providing a uniform surface coverage breaking on the side wall. E-beam evaporated metal layers for contact and bond pads would result in such a breaking as well. In order to achieve a continuous layers over all of the trench surfaces it was agreed that a trench etch where the side walls would be at an angle was necessary.

Initially a possibility of an wet etch was investigated, bearing in mind that its isotropic profile might serve as a way to provide an angle to the side wall surface (84) (85). Hydrogen Peroxide H_2O_2 was utilized for these etching attempts as it would utilize underlying Si layer as an etch stop providing a required etch depth. This is because of Si not being etched by H_2O_2. This however did not produce required effects. Since this is not a uniform etch, masking of Ge is required and in the time required to achieve a desired depth of etch all of the tested photoresists were removed therefore

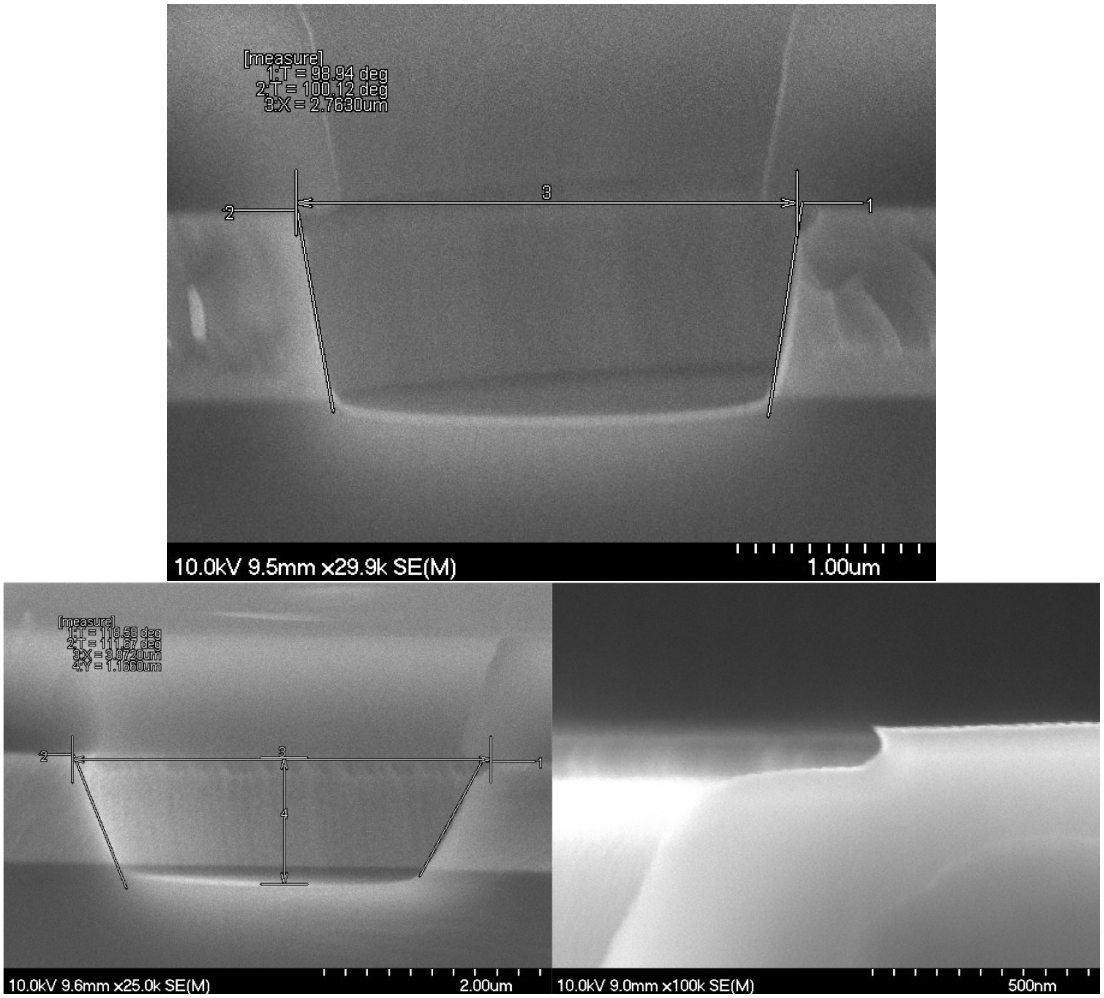

Figure 4.24: Sem image of slope trench etch test with 115sccm (top) and 100sccm (bottom) of C4F8 in the STS ICP dry etch tool.

exposing all of the Ge surface to the etch. A possibility of utilizing a metal mask was considered, but it was dropped since the trench profile in that etch ended up producing an "overhang" in Ge that would result in the deposited layer continuity being broken. With that investigative focus was shifted towards possibility of dry etches.

Achieving sloped surface with the dry etching techniques is challenging since they are usually developed do perform anisotropic etches. If however, an etch removes material in a preferential way to a certain crystallographic direction, that could be used to recreate sloped side wall. Etch like that was already developed for etching SiGe

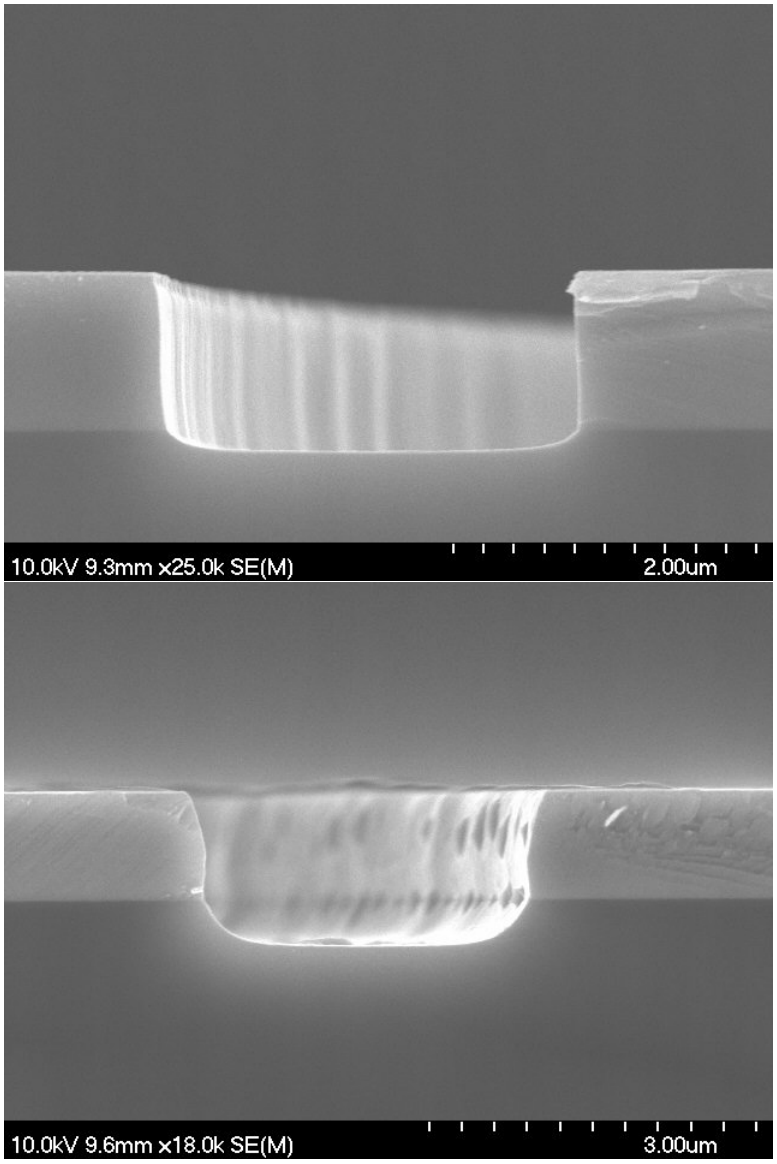

Figure 4.25: Sem image of slope trench etch test with 50sccm (top) and 100sccm (bottom) of CF4 in the RIE80+ dry etch tool.

superlattices with 85% Ge content, that was producing side wall of 80° with an etch rate of 1.03μm/min, and was decided upon as a starting point for investigation of more sloped etches. Exact recipe of that etch consisted of gases C4F8/SF6 with flows 90/130, platen power 12W, ICP Power 600W and Pressure 15mT. Upon using that exact recipe however, no sloping was achieved while etching trench inside of Ge. This could be a

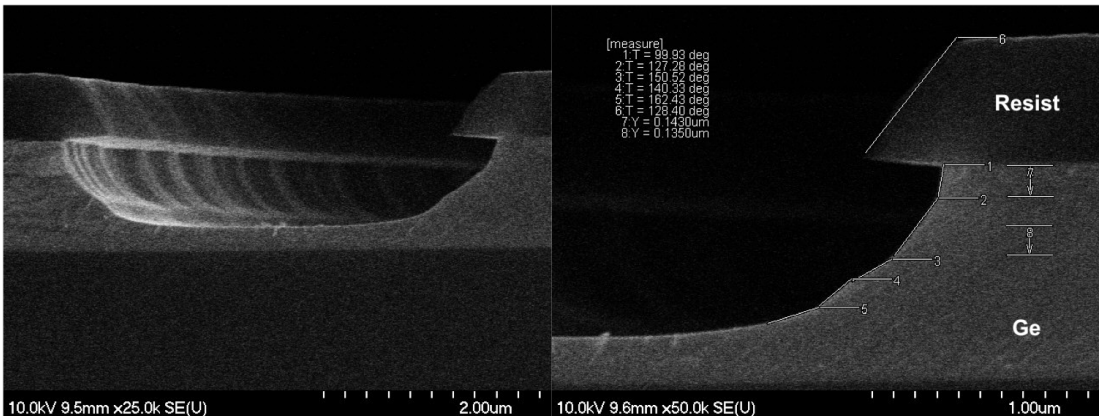

Figure 4.26: Sem picture of a sloped trench etched with SF6O2 and a resist profile stopped before reaching Si layer.

due to the different material composition or type of proximity effect due to etching in a trench rather than open architecture as for the case in which the etch was investigated for. It was decided that a range of changes in this etch should be investigated, setting up appropriate parameters for our case with a primary focus put on changing flow rates of the C4F8 (which is used as a surface passivating chemical during the etch). This is because of this gas serving as a passivation during the etch process, with a slight sloping already present in the basic etch and increased value of surface passivation the passivation build up should slow down the vertical component of the etch, allowing for it to consume more material on the side walls therefore resulting in more prominent sloping. Flows of C4F8 in range between 115 and 90 with an decrement of 5 were investigated utilizing a range of test samples with $2\mu m$ wide trenches fabricated with a photolithography processing. Sem images of cross sections through the trench for the cases of 115 and 100sccm of C4F8 are presented in Fig.4.24.

As can be seen on the top picture representing highest value of the C4F8 flow selected for this investigation the sloping does not exceed initially achieved value of around 80°. It has been observed however that around the flow of 100sccm C4F8, there was a local maximum of the sloping, resulting in the 70° side walls with the value of sloping dropping while moving to either lower or higher values. Even though this value is still far from the best possible case of side walls sloped at 45° this could potentially be enough to achieve desired continuous layer deposition. However, after stripping resist

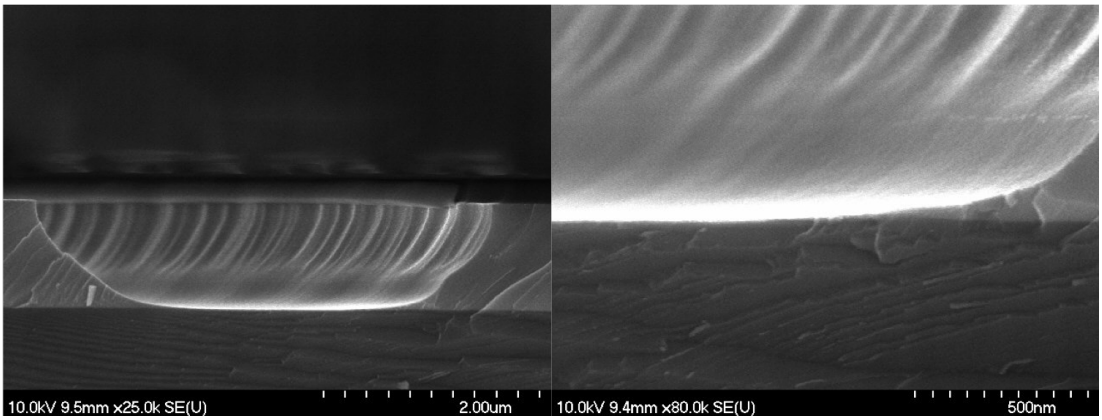

Figure 4.27: Sem picture of a sloped trench etched with SF6O2.

after etch, it was discovered, that this etch was displaying an unwanted characteristic as can be seen in the bottom right close up of the trench top in Fig.4.24. There can be observed an overhang in the Ge top surface close to the trench edge. This could lead to breaking of the deposited layers, especially while taking measurements in extreme temperatures in addition to potential creation of hot spots in electric field. That combined with not achieving required amount of side walls sloping lead us to investigate different etch chemistries.

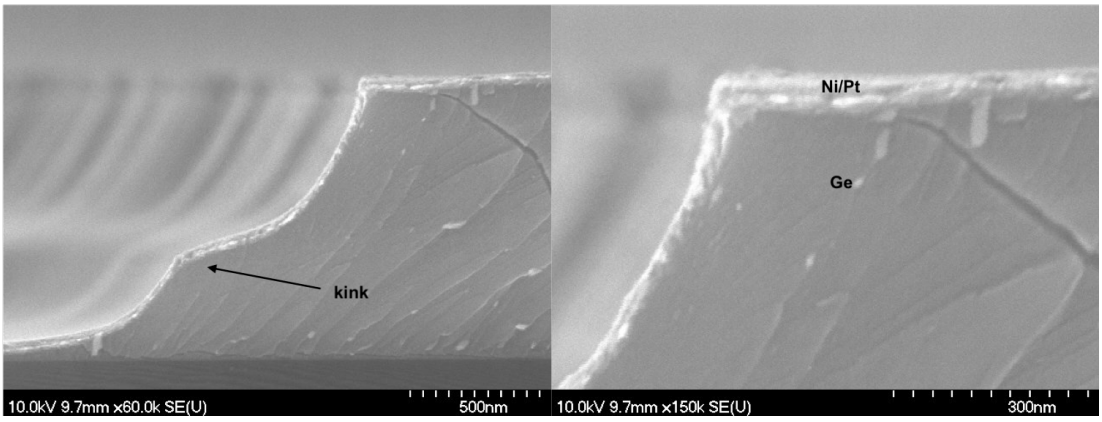

Figure 4.28: Sem picture of a sloped trench cross section with a uniform 10/50nm Ni/Pt metal layer coverage.

Following the suggestions in (86) and (87) etches using combination of CF_4 and O_2 were investigated. To achieve isotropy for the CF4 etch chemistry pressure was kept at

20mT and values of CF_4 and O_2 flow rates as well as the ICP power were investigated. Sem images of the trench cross sections for the etch with 50sccm and 100sccm of CF_4 can be seen in the Fig.4.25. However, only sloping in the Si layer was achieved for this etch chemistry, therefore not making it a viable etch method.

Last etching chemistry investigated was a known Ge etching method utilizing Sulfur hexafluoride (SF_6) and O_2. Values of pressure, and flow were changed to investigate potential change in the etch profile. At the 9/21 sccm of SF_6 and O_2 with 100 W power and 20 mTorr pressure a significant sloping was observed. Due to extended etch time in comparison to the standard recipe,initially sample was removed from an etch before reaching Si layer. This can be observed in the Fig.4.26 presenting a cross section through the trench with a resist used for the etch still intact. It can be seen that the really mild angles were achieved with resist profile being affected and sloped as well and displaying an "overhang" characteristic for the isotropic etches. Sample was then put for another longer etch. It became apparent that although the etch creates a desired sloping effect in the Ge side walls, it does not have a very good selectivity. While the next sample was etched to a depth of $1.3\mu m$ all of the resist from the surface was removed, causing significant damage to the top Ge surface. Sadly the easiest option of addressing that issue - using thicker resist was not viable in this case as the thickest possible resist layer at which it was still possible to achieve $2\mu m$ resolution for the trench width, was already used. To combat that, etch rate was investigated in depth to achieve etching past the Ge layer without total removal of the resist. We were able to time the etch precisely, etching just past the Ge layer without stripping the resist which result is presented in Fig.4.27. Sloping presented here was the best achieved in the Ge medium, and is the best candidate for the sloped trench architecture, even though the trenches width gets expanded by that etch to about $3\mu m$. The kink appearing in the middle depth of the trench was investigated, although its origin was not fully understood. Overall slope angle becomes more mellow while approaching bottom of the trench. These angles were measured and presented in the close up in Fig.4.26.

To further asses the application value of this trench a test was devised in which on the sample surface a thin layer of metal (10nm of Ni and 50nm of Pt) was deposited utilizing e-beam metal deposition tool. With a e-beam deposited metal being very

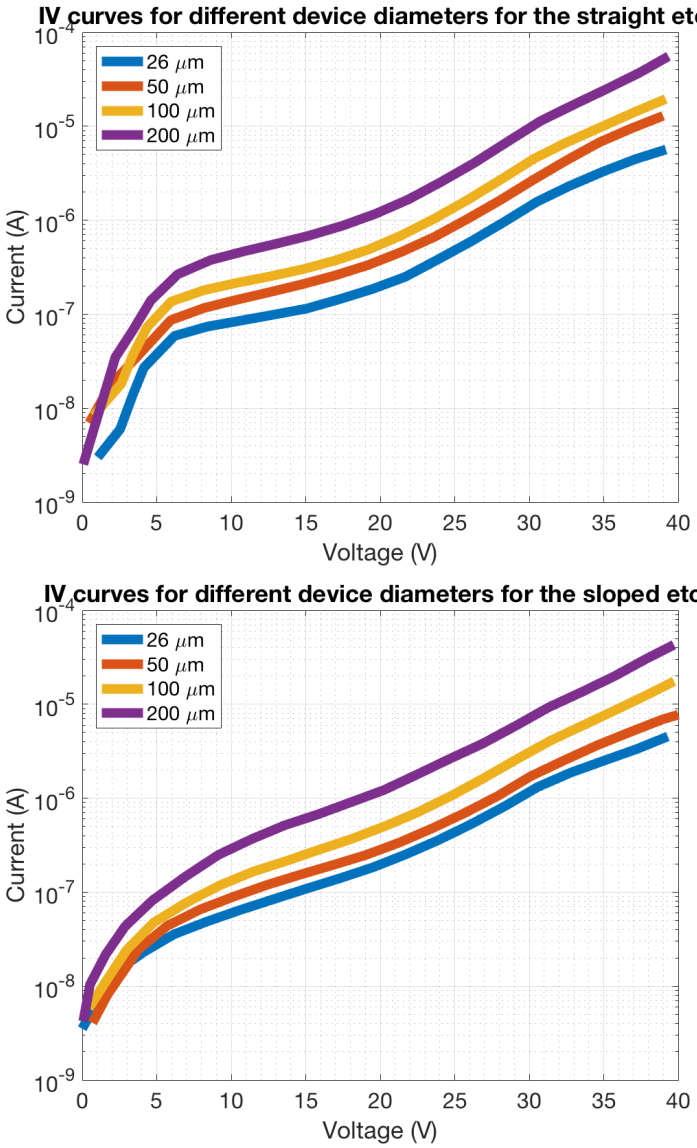

Figure 4.29: Voltage - Current characteristic for different device sizes for straight and sloped trench etches. Top - straight side wall etch. Bottom - sloped side wall etch.

directional, and a thinness of its layer it would be prone to discontinuities if the side wall area was not smooth enough. This would be especially true near the top of the trench where the slope is closest to 90°. However, as can be seen in the Sem trench cross sections in Fig.4.28 the thin layer of metal remains continuous on the side wall. Electrical connection was also performed to cross check the metal continuity at the

inside and outside of the trench. With that test being a positive result, it was decided that an trench etch with above mentioned recipe would be utilized in the generation 13 fabrication.

Lastly, to gain better understanding of a potential trench profile influence on the sample performance, two chips were fabricated, with the same defined P+ etch and straight trench side wall for one and sloped for the other. These test samples were produced using SPAD wafer 2. The current - Voltage (IV) characteristics were then taken for different device diameter for both of these cases and are presented in Fig.4.29. As can be seen although IV's stay the same above 25V there is a slight difference below that value. For the sample with a straight side wall a voltage value near 0V is lower, and rise in current is less smooth than for the sloped one . The biggest indicator of the device performance would be sharpness of change and the value of current before the breakdown. Since these devices were not taken to the breakdown voltage it is difficult to judge if the side wall profile would have an influence (either positive or negative) on the overall performance. It is worth noting however that difference in these two cases goes against initial assumption that the side wall is located far enough from the active area to have any influence on the devices. Since the trenches were located $10\mu m$ away laterally from the embedded charge sheet, it was expected that the confined electric field would not interact with a side wall surface, therefore these two characteristics should have been the same. The fact that side wall does in fact influence IV curves suggests that there is some sort of interaction with the side wall indeed, and is influenced on the side wall profile (since it is the only difference between these two devices measured). We will try to understand the origin of that phenomenon and explain it in detail in the future work.

4.4 Fabrication of Gen13 devices

In this section all of the fabrication steps of Gen13 devices will be discussed in detail.

Firstly, chip fabrication begins with dicing of the water into $1cm^2$ chips with a diamond saw. Each of the chips has designated quarters as seen in Fig.4.30.

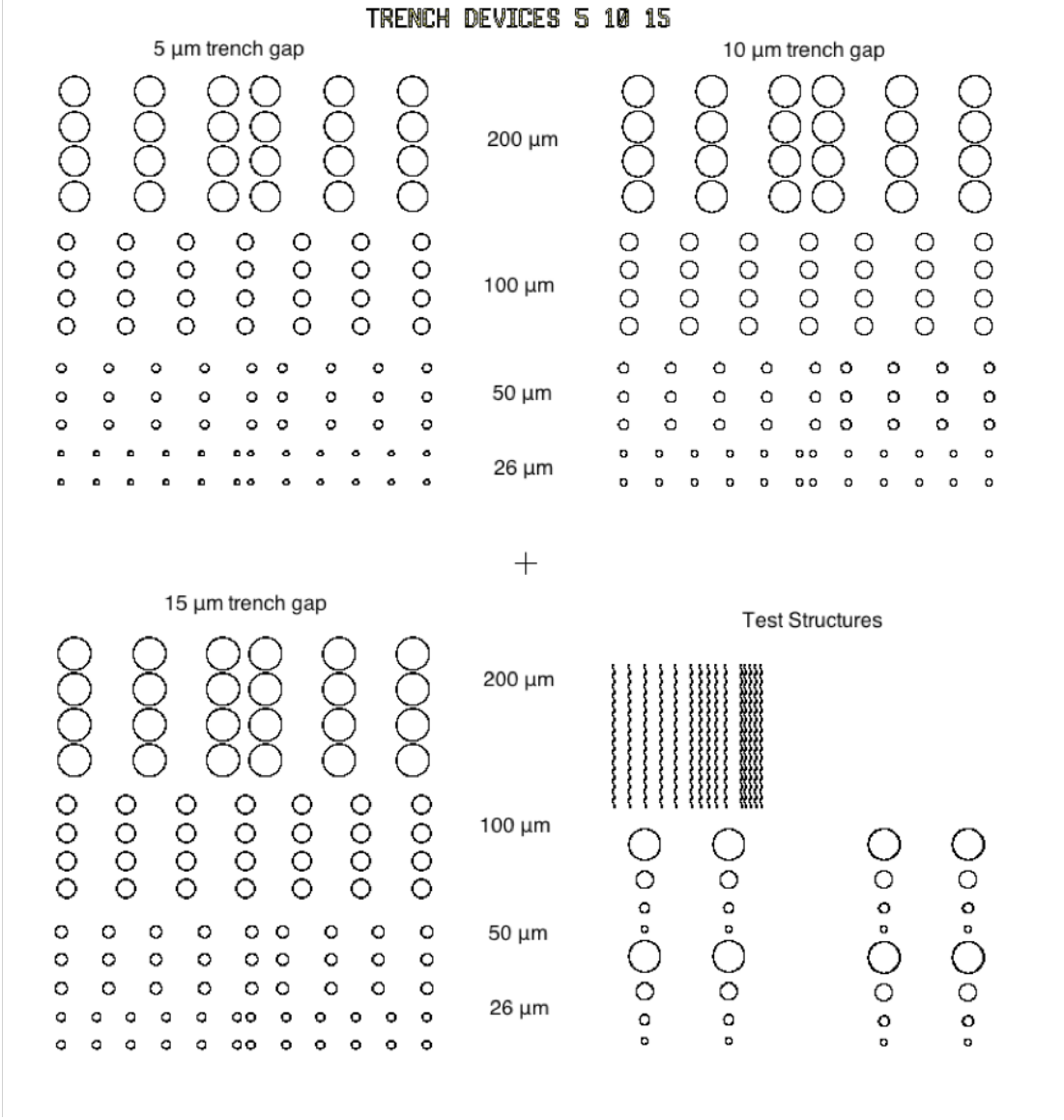

Figure 4.30: Differences between quarters in a Gen13 chip

Three quarters that are present on the chip, have the same processing with a differences in the distance of trench etch from the charge sheet. These are as follows:

- Quarter 1 - lateral distance of $5\mu m$ from the charge sheet (trench gap).
- Quarter 2 - lateral distance of $10\mu m$ from the charge sheet (trench gap).

- Quarter 3 - lateral distance of $15\mu m$ from the charge sheet (trench gap).

Quarter 4 is filled with test structures for quantifying the effectiveness of trench filling, continuity of the contact and electrical connectedness of the bond pad. Additionally, this quarter is used for placement of the interferometer for various steps that require cross referencing during etches and depositions.

Processing begins with removal of the photoresist that was deposited on top of the device as a protective measure from the airborne debris produced during dicing. This is achieved with an ultrasonic bath dip of 5min in acetone proceeded with 5min in IPA. It was observed that this cleaning was insufficient as some resist residue remained on the sample surface. Therefore, additional clean of 1.5min in the Metal Ion Free 319 (MF319) developer with RO water rinse afterwards is recommended to achieve the cleanest surface. The chip is then put in the $120°C$ oven for 10min dehydration bake. Photoresist S1818 is then spun on the sample at $4000RPM$ for 30s. The backside of the chip is then cleaned with an acetone dipped cotton bud. This backside clean is then performed after every spinning step afterwards. The chip is then placed on a $85°C$ hotplate for 2min to bake the resist. Using a MA6 photolitography tool our chip was exposed for $4.4s$ with an ultraviolet light, at the vacuum setting, with a pattern for the p-Ge etch.

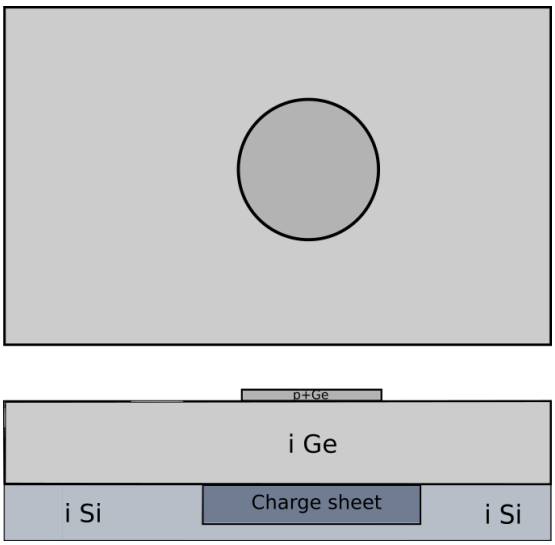

Figure 4.31: Top and cross section view of the Gen13 depice after performing P Ge etch.

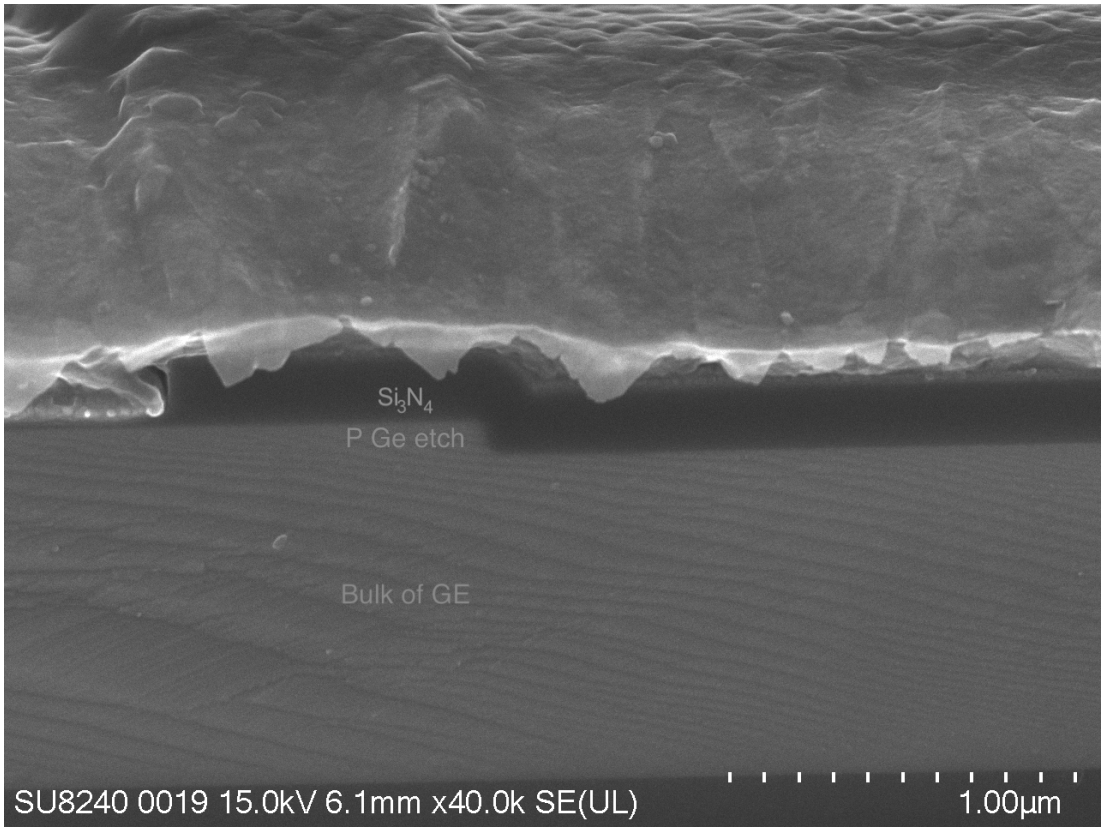

Figure 4.32: SEM image of a cross section through the P Ge etch on a test device covered in Al bond pad for electrical testing.

After the exposure, the chip was developed in MF319 for 75s and rinsed in RO water for 75s. After the visual quality control of the development under a microscope the sample was submitted for the etch with Oxford Plasmalab 80 Plus RIE using 50sccm of Tetrafluoromethane (CF_4) with RF power of 200W, pressure 55mT at 22°C for 45s. This etch provides consistent etch depth of around 80nm. With the doped p++ contact on top of the Ge surface of around 50nm, this proves to be a reliable etch depth providing electrical isolation of the top contact. A cross-section SEM image of the p++ etch on the test sample is provided in Fig.4.32.

The next step of the processing is an etch of the thin trenches surrounding the device. This step has proven to be a necessity due to the presence of the leakage current observed between different devices when the device was not isolated from the bulk of Ge. A thin trench isolation etch past the thickness of Ge has proven to be the best

solution allowing for preservation of the planar type of device while solving the issue of isolating devices from each other. A width of $2\mu m$ was selected for the trench for the reasons explained in the methods chapter 2 of this thesis. Another requirement for increasing the performance of this type of design was that it required a highly sloped etch, to allow for the continuous deposition of the SiN and metals along the side of the trench. In depth analysis of that process and its development is included in the methods chapter 2 of this thesis.

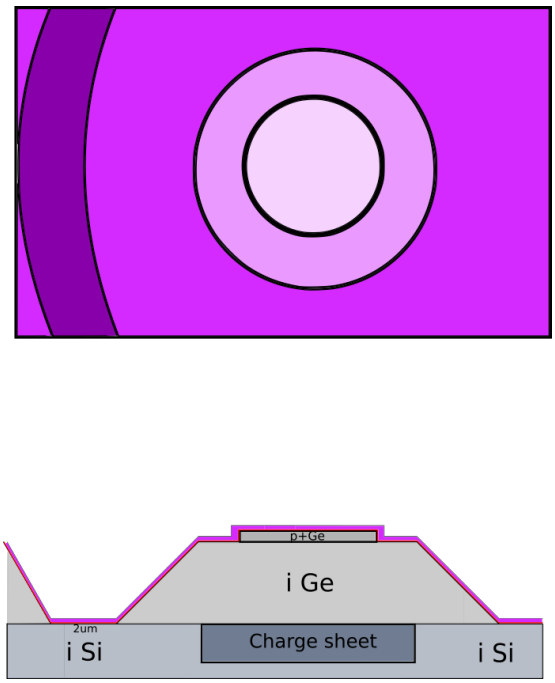

Figure 4.33: Top and cross section view of the Gen13 device after performing isolation trench etch, followed by surface passivation and capping with Si_3N_4.

The sample was cleaned using the standard process of 5min in an ultrasonic bath in Acetone proceeded with 5min in IPA. After blow drying the chip was placed in the $120°C$ oven for a dehydration bake. The S1818 resist was then spun at 10 000RPM for 30s followed by a hotplate bake at $85°C$ for 2min. The sample was then exposed for 4.4s in the MA6 photolithography tool at a low vacuum setting followed by being developed in MF319 for 75s proceeded with a 75s RO water rinse. After a visual inspection of the development under a microscope the sample was submitted for an etch

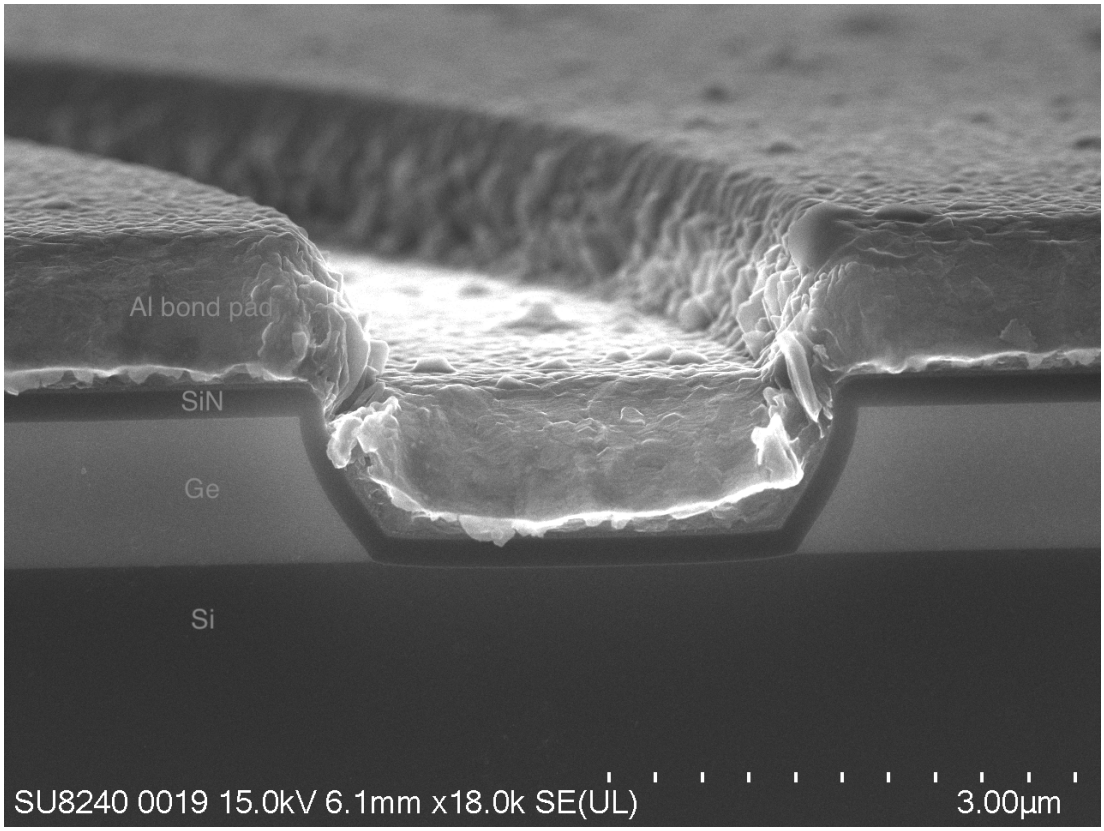

Figure 4.34: SEM image of a cross section through the test structure, sloped, circular trench with Al bond pad.

in a RIE80+. The etch was performed with Sulfur hexafluoride (SF_6) and O_2 with 9/21 sccm respectively, RF power of 100W, pressure of 20mT for 8min in 20°. An SEM image of a cross-section of the resulting sloped trench in a test device can be seen in Fig.4.34. The bottom part of the trench lies between 150nm and 200nm below level of the Ge providing sufficient isolation between devices.

Trench etch is followed by surface passivation and capping. Because of an oxidation furnace malfunction during the development of devices in Gen13, the suboptimal method of passivation under the ALD layer had to be used (as described in section 5.1). However, although according to electrical field simulations this should not pose an excessively detrimental effect on device performance since the side walls are being kept at a sufficient distance from the active area of the device. The chip is then

cleaned with a standard 5min Acetone and 5min IPA in an ultrasonic bath. Before the surface passivation it is important to strip any native oxides that have formed on the Ge surface. This is done with a cyclic Hydrofluoric (HF) acid dip. HF was chosen for its ability to remove native oxides without damaging the Ge surface. HF etching also leads to a better prepared Ge surface than in the case of HCl which, even though not resulting in a damage to Ge surface, leaves a Cl residue as stated in (74). A dip of 30s in a 10:1 HF solution was performed next, followed by 30s in the RO water. This process was repeated 2 more times (to improve the sample surface quality) before blow drying the sample. Due to the rapid formation of the native oxide on the Ge surface in the atmosphere the chip must be transported into a vacuum environment immediately after the HF clean. A vacuum environment is provided inside of the ALD cluster tool where the passivation of Ge and capping of its oxide can be performed. Capping of Ge oxide is crucial as a way of protecting it from the atmosphere as it is highly water soluble. The method used here was Oxygen plasma passivation under a thin layer of Al_20_3 as described in detail in section 5.1. The recipe used for this was 10 cycles of Ch3 Al_20_3 at $290°C$ followed by 5min of 0_2 plasma, capped with 40 cycles of Ch3 Al_20_3 at $290°C$. This process results in a total thickness of Al_20_3 of about 5nm.

The chip was then sent for uniform PECVD Si_3N_4 deposition. This layer is used for two separate functions: 1) It serves as a anti reflection coating for the optical measurements performed in the wavelengths between 1310 nm and 1550 nm and 2) provides isolation as a dielectric layer between metal contact and Ge surface. The sample is then sent for 180 nm PECVD Si_3N_4 deposition immediately after the ALD processing. As observed in Fig.4.35, the layer of Si_3N_4 remains continuous on the side wall thanks to the high quality of deposition and a sloped side wall.

After the Si_3N_4 the next step in processing is trench filling with Hydrogen silsesquioxane (HSQ). A precise description of the process development for this step can be found in the section 4.3.1. The chip is subsequently cleaned by gentle agitation in an Acetone filled beaker followed by gentle agitation in an IPA filled beaker. The sample is then placed in the $120°C$ oven for 10min dehydration bake. Neat HSQ is then spun on the chip at 6000 RPM for 60s. No after bake is performed on that chip, instead it is being placed inside of a specially prepared Methyl Isobutyl Ketone (MIBK) rich environment

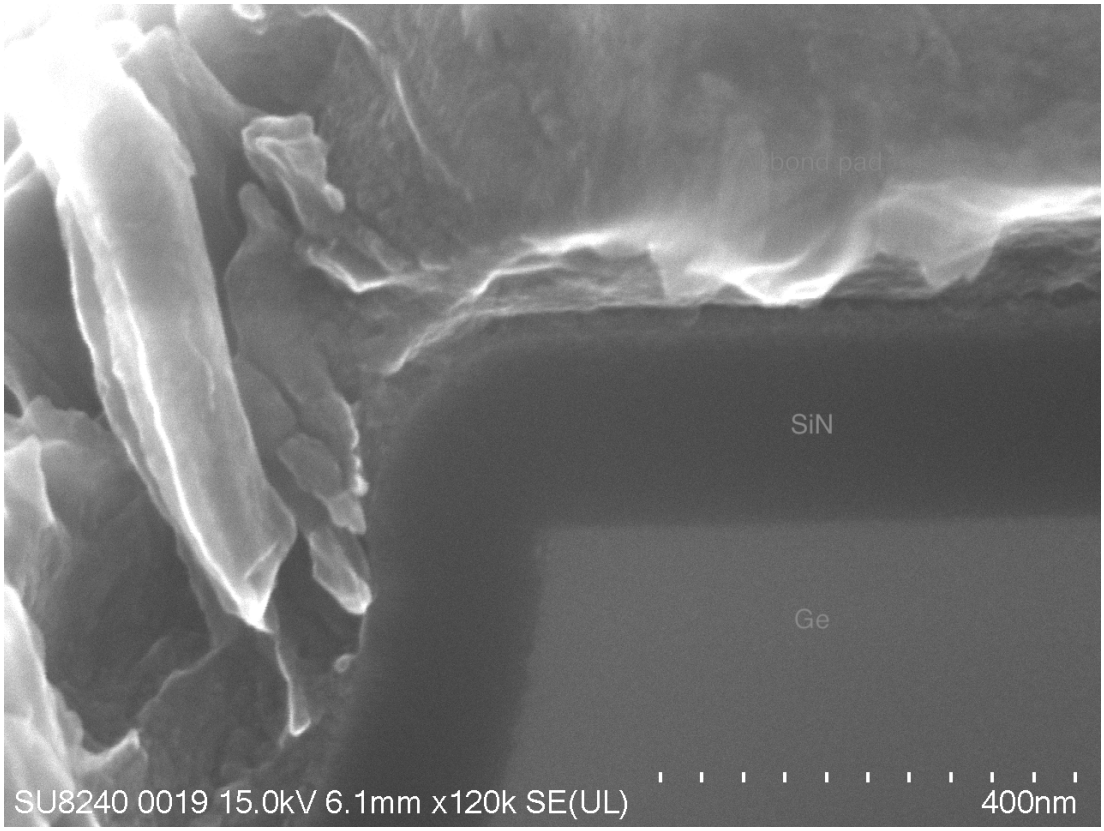

Figure 4.35: SEM image of a cross section through the test structure with zoom in on a side wall of a trench.

as shown in a Fig.4.36. Two petri dishes are utilized with a smaller one placed inside the larger one. The spacing between the petri dishes is then filled with MIBK. The chip is then placed in the smaller dish with the utmost precision so as not to allow for direct contact of chip with MIBK. A watch glass is then placed on top of the petri dishes to allow for creation of highly MIBK rich atmosphere via its evaporation. The sample is then left overnight in a designated fume cabinet to allow for the HSQ to flow from the high points on the chip to fill in the trenches surrounding active areas. After the overnight reflow in order to evaporate an excess of MIBK from the sample surface a 2min bake on top of a $90°C$ hotplate is performed.

In order to create a connection and optical access, it is imperative to open via holes on top of the active areas of the chip. Firstly, the HSQ is removed via dry etch. The

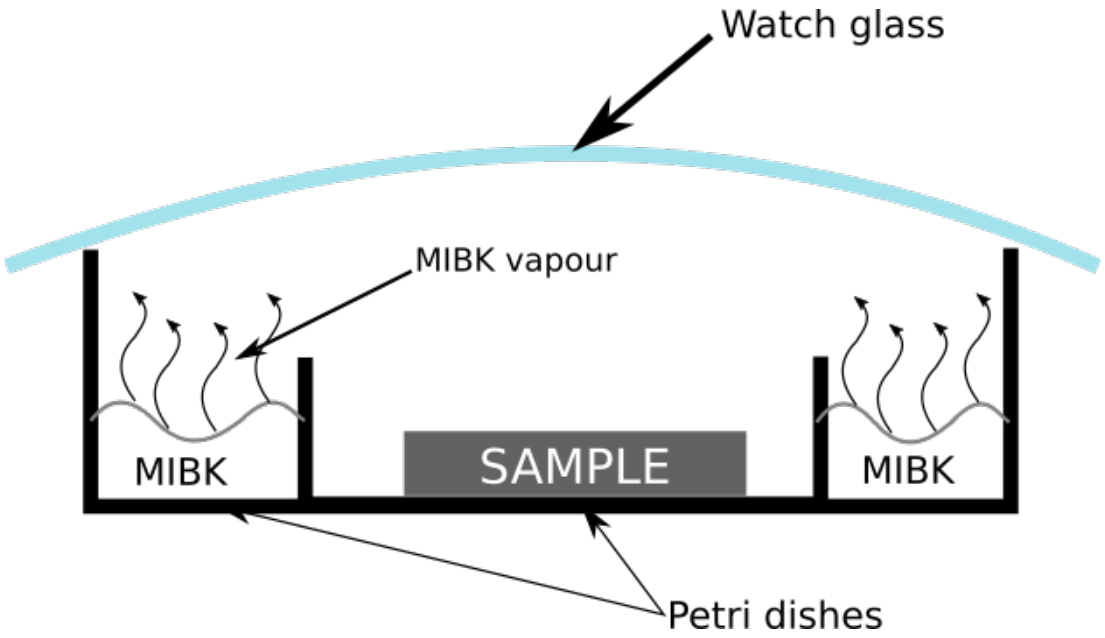

Figure 4.36: Diagram of a setup used for performing of the HSQ reflow.

via hole is opened as seen in Fig.4.37. This step is performed to open up access to the active area and allow for contact deposition. However, this can not be performed as a uniform layer removal. Patterning a specific area on top of the device rather than removing the material from all of the surface preserves a layer of HSQ in the areas outside of the active area. This layer in turn, provides additional isolation preventing electric contact in areas other than the active area. It is especially important for the thick bond pads (deposited in later steps) that, if such an isolating layer was not in place, could cause a current to pass through the bulk of the material.

Before etching, the sample is treated with a gentle agitation clean in Acetone and IPA for 5min. The chip is then put in the $120°C$ oven for 10min dehydration bake. S1818 photoresist is spun at 4000 RPM for 30s after which the sample is put on a $85°C$ hotplate for 2min. Exposure is carried out with a MA6 photolitography tool for 4,4s on a Vacuum program. After the exposure, the chip was developed in a 1:1 solution of Microposit Developer Concentrate and RO water for 75s and rinsed in RO water for 75s. Microposit Developer concentrate is used from this point on to develop photoresists from S18 series as it does not attack HSQ or SiN. Additionally, resist is removed from the test quarter chip with an acetone dipped cotton bud. After a visual inspection

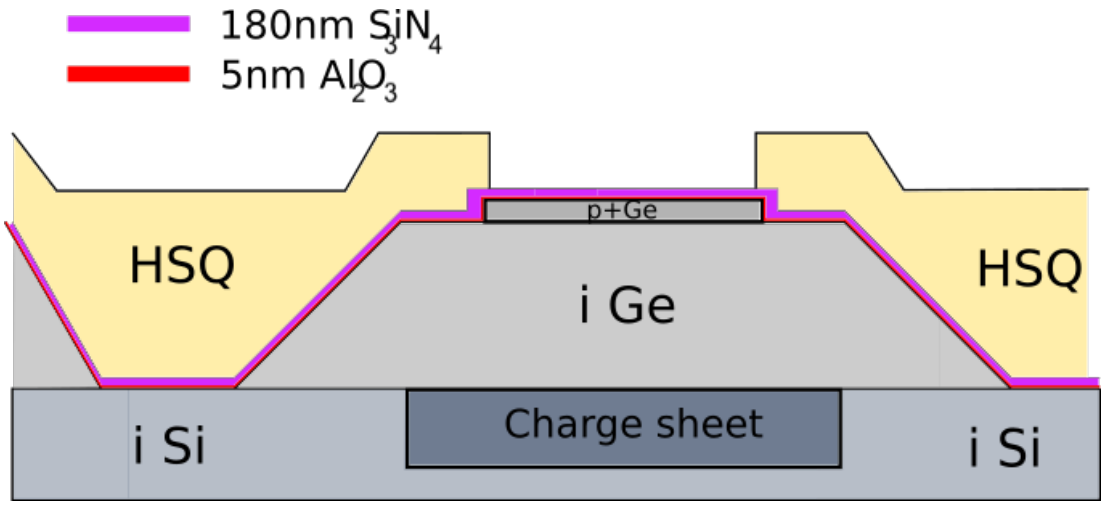

Figure 4.37: Schematic cross section of a chip after opening via hole in the HSQ (not up to scale).

under the microscope, the sample is ashed in the microwave asher at 150 W for 2.5min on the "descum" program (which is a setting providing good quality sample surface clean after the photoresist development). RIE 80+ is used for etching the via hole with Fluoroform (CHF_3) and Argon at 25/18 sccm, with RF power of 200W, pressure 30mT at 20°C. For this process it was necessary to use an interferometer aimed at the top of the device. This is because of potential non-uniformities of the HSQ thickness after the reflow. Usage of the interferometer allows to stop processing when the signal indicates that the HSQ has been removed. Because of having to stop precisely before the antireflection coating begins to etch, the recipe was selected so that it would have slower etch rate in Si_3N_4.

Following this, it is necessary to open via holes in the Si_3N_4 without removing it from the center of the device. The sample is cleaned with a gentle agitation for 5min in Acetone followed by 5min in IPA and blow dried, it is then placed in 120°C oven for a 10min dehydration bake. After that the S1818 resit is spun at 10 000RPM for 30s and the sample is baked at 85°C hotplate for 2min. Resist exposure is performed at MA6 photolitography tool for 4.4s at a low vacuum setting. The sample is then developed in 1:1 Microposit developer concentrate and RO water solution for 75s and rinsed in RO water for 75s after which it is ashed in a microwave asher at 150W for

2.5min at the "descum" recipe. RIE 80+ is then used for opening via holes in Si_3N_4. The recipe used is CHF_3/O_2 at 50/5 sccm, RF power of 150W, pressure 55mT at $20°C$. The interferometer is also required for judging the depth of the etch, it is placed on top of one of the test structures that were opened up in the previous step. Resist is then removed from the sample surface with a gentle Acetone/IPA clean as in previous steps.

The last step before depositing the metal contacts requires opening up the via holes through the Al_20_3. In order not to damage the chip during the wet etch it is imperative to perform a hardening anneal for HSQ on the sample. This is performed at the Rapid Thermal Annealer (RTA) at $450°C$ with 60s ramp up for 10min. This process results in the HSQ becoming much less susceptible for the Tetramethylammonium hydroxide (TMAH) wet etch later. It was observed that usage of the furnace for that step might be beneficial albeit being slower than RTA process. This is because the quick ramp of the temperature in RTA can lead, in some cases to the creation of cracks on the HSQ surface. After the HSQ hardening the sample is placed in the $50°C$, 25% TMAH for 2min and this is proceeded with RO water rinse. This wet etch is carried out to remove the Al_20_3 in the via holes going through Si_3N_4 .

The next step involves deposition of the metal contact. The process for S1818 lithography at 4000RPM is then repeated starting with a gentle Acetone/IPA clean, development with Microposit Concentrate and finishing with 150W, 2.5min ash. The sample is placed in the Plassys IV metalization unit for metal contact evaporation. In order to prevent potential damage to the sample surface, HF removal of the Ge oxide was abandoned in favor of performing the Ar sputtering of the sample at the Plassys IV right before the metalization. With that method, the sample stays in a high vacuum environment after oxide removal, preventing spontaneous native oxide creation. After this 10nm of Ni followed by 50 nm of Pd are deposited. The sample is then placed in the $50°C$ Acetone bath for the liftoff of excessive metal for 30min. The quality of liftoff is then investigated with the long focusing range microscope. In some cases there might be parts of the metal that did not lift in the acetone bath, therefore a two step process is recommended for their removal. Firstly, while keeping the sample in the acetone beaker a plastic pipette is filled with fresh acetone and submerged. By squeezing the pipette and directing it on top of a sample, a rapid stream of acetone is

created promoting liftoff. If after microscope inspection the liftoff is not completed it is recommended to perform a short ultrasonic bath of couple of seconds. This is however very aggressive on the sample, potentially reducing its quality and should therefore be used with utmost precaution and only if the removal with pipette did not produce satisfactory results. After that sample is rinsed in IPA and blow dried with a Nitrogen gun.

The sample is then placed in the $120°C$ oven for a 10min dehydration bake as a preparation for the bond pad stage of the processing. Before proceeding with this part of the process it is advised to pipette the required amount of the AZ2070 photoresist to allow it to gently rise to ambient room temperature. Initially the sample is covered with 80:20 HDMS primer, after a wait of 20s it is spun at 4000RPM for 5s. If the AZ2070 has risen to room temperature it is deposited on the chip and then spun at 4000RPM with 20 000 ramp for 60s. After cleaning the chip's back, it is placed on the $110°C$ hot plate for 90s. It is then exposed with MA6 photolitography tool for 20s with the vacuum program setting. After that a post bake of 60s on $110°C$ hotplate must be performed. Next, the chip is developed for 70s in MF319 developer, followed by RO water rinse. After visual inspection under microscope the chip is ashed in microwave asher at 150W for 2.5min on a "descum" setting. The chip is then placed in the Plassys IV metalization tool for bond pad deposition. Metals deposited are 10nm of Ti, that acts as a sticky layer promoting general adhesion of the bond pad, and 1000nm Al being bond pad proper. Lift off should be carried out in the same way as in the case of metal contact deposition finishing with an IPA rinse and drying with Nitrogen blow gun.

The final step of the fabrication is deposition of a back contact for the chip. The top of the sample should be covered in S1828 photo resit and spun at 4000RPM for 60s, the back side is cleaned with an acetone dipped cotton bud and finished with a 2min post bake on a $85°C$ hot plate. After that a quick HF clean is performed on the back surface of the chip. It is recommended to use 10:1 HF for no more than 15s to prevent any potential attack of the chip from its sides. Immediately after the HF clean the sample should be put into the vacuum environment of the metalization unit, then 10nm of Ni and 50nm of Pd are evaporated on the backside of the sample.

This concludes the fabrication steps of the Gen13 devices. It is recommended to leave the resist on top of the sample after metal deposition on the back side. This not only protects the sample surface during transportation, but also provides a protective layer for the subsequent diamond saw dicing, which is performed for fitting separate quarters of the device on the header package on which most of the optical measurements are subsequently being performed.

5

Measurements and results

In this chapter I will present the results for the devices from generation 12. The initial fabrication steps on the generation 13 devices were carried out, however these devices are still not finalized as of writing this PhD thesis. The initial results obtained for the generation 13 will be presented in the Conclusions chapter 6.

Let's begin with measurements performed on the test samples fabricated using the batch of wafers with selectively doped charge sheets of $1 \times 10^{17} cm^{-3}$, $2 \times 10^{17} cm^{-3}$, $3 \times 10^{17} cm^{-3}$, $4 \times 10^{17} cm^{-3}$ and $5 \times 10^{17} cm^{-3}$ which from now on will be referred to as SPAD1, SPAD2, SPAD3, SPAD4 and SPAD5. As established in the simulations chapter wafer SPAD2 is expected to produce devices of the highest performance based on the modeled electric field distribution. The test devices utilized were single etch mesa structures with diameters of $50\mu m$, $100\mu m$, $200\mu m$, $300\mu m$, $500\mu m$ and $1mm$ with full top metal contacts allowing for an easier direct probing.

Firstly current - voltage (IV) characteristics were taken for $200\mu m$, $300\mu m$ and $500\mu m$ diameter devices fabricated from different wafers. These are presented in Fig.5.1. Measurements were performed between 0 and 40V in reverse bias. Parts of the curves near 0V are missing because of the recorded current being below the noise floor of the setup used to perform these measurements. As can be seen in Fig.5.1, SPAD1 is an outlier for which the values of current are high, indicating a potential poor performance of the devices fabricated from that wafer. This is caused by the lowest charge sheet doping in that wafer. For a case where charge sheet doping is too low,

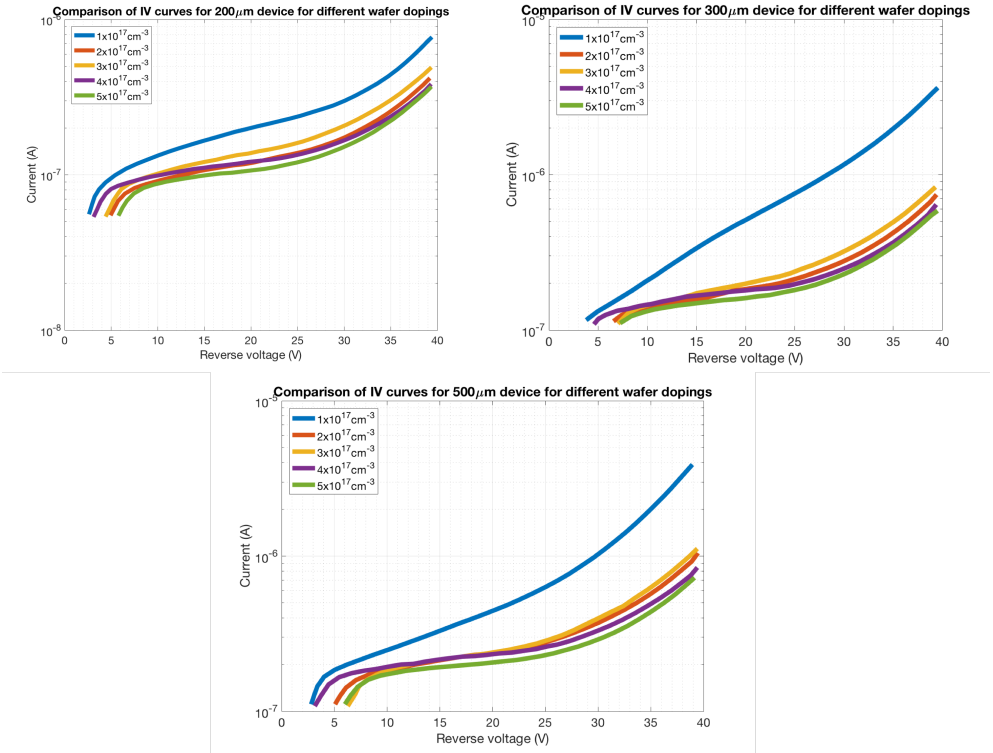

Figure 5.1: Comparison of Current - Voltage characteristics for different charge sheet dopings and a given device size.

value of the electric field inside the Ge absorption layer is increased which leads to an increase in the tunneling current from Ge absorption to Si multiplication layer resulting in higher values of the dark current. It can be also seen that although IV's for other wafers are of similar value there is an interesting behavior present (especially visible for the $500\mu m$ device) where the wafers SPAD2 and SPAD3 display a similar values of a current to each other, and wafers SPAD4 and SPAD5 are alike as well. For the wafers SPAD3 and SPAD5 the current stays below the noise floor level of the setup at the highest voltage. To obtain a better understanding of the effect of doping density a series of measurements for different device diameters were performed for a given wafer doping, Fig.5.2. Consistent with the previous observations, wafer SPAD1 displays the highest values of dark currents. For the other device diameters the measurement are similar across the wafer doping with exception of $50\mu m$ and $1mm$ diameter devices. For the first case this lack of uniformity was most likely caused by the difficulty of placing probes with large tip sizes on top of these devices. As for the largest device, wafer

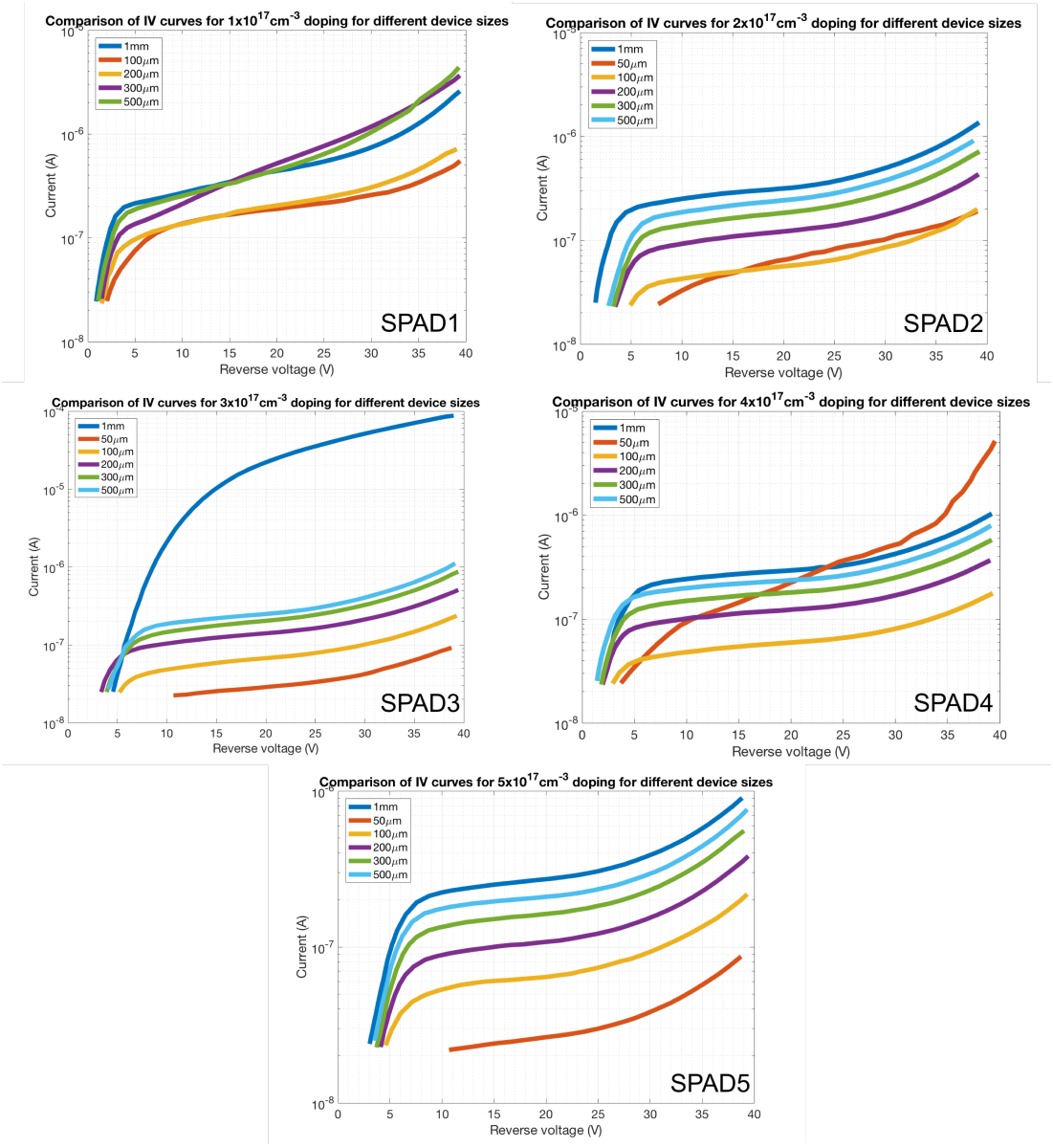

Figure 5.2: Comparison of Current - Voltage characteristics for different device sizes and a given charge sheet doping.

SPAD 3 seems to be an outlier with a really high values of current out of all the other wafers especially when considering device of 1mm diameter for which dark current was two orders of magnitude higher than in the case of other wafers. This is surprising as it was expected for other wafers to exhibit similar behaviors, since such a large device would posses significant surface area, contributing to a high values of carrier

generations. It is not surprising however that the most promising wafers SPAD2 and SPAD4 are centered around the wafer SPAD3 and its the result of the doping activation process. As discussed in the earlier sections after the implantation the ions require a temperature anneal to become electrically activated within the doped medium. This process however is probabilistic in nature, resulting with actual value of doping most likely to be lower than a perfect scenario in which all of the dopants become activated. This in turn would result in a wafer of nominally higher implanted doping possessing characteristics of a lower doped wafer.

In this case, wafer SPAD3 has a nominally higher doping density than the most optimal value obtained in the simulations, however while taking into account that not every dopant would become active therefore decreasing an actual doping value. Therefore it becomes understandable why wafer with a value slightly higher than the optimal value after the dopant activation would end up with doping value closer to the optimal one.

More measurements were carried out on the most promising wafers SPAD2,SPAD3 and SPAD4 using a more advanced measurement setup that allowed for biasing devices at increased voltage allowing for reaching the breakdown, with and without illumination, trying to asses which of these wafer would be the best one to continue fabrication with. Although displaying similar properties in these measurements, wafer SPAD3 seemed to be a best suited one. It was displaying the lowest current value right before breakdown - which is a good indicator of high performance as suggested by a TCAD-simulations of single-photon avalanche diodes is (83), allowing for better differentiating between states with an without photon registration Fig.5.3.

With these results it was decided that the wafer SPAD3 was the best candidate to fabricate the devices from. As an additional mean of comparison some devices were fabricated from the SPAD2 and SPAD4 wafers as well but since they did not meet the performance expectations they will not be presented in the further part of this results chapter.

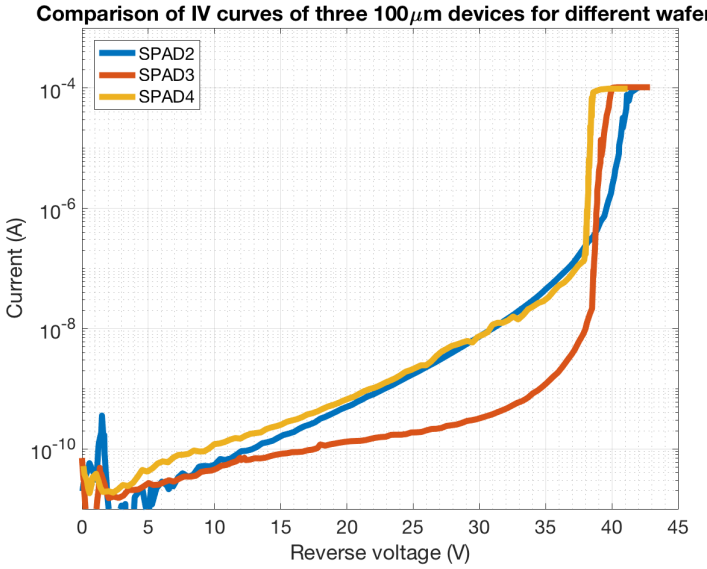

Figure 5.3: Comparison of Current - Voltage characteristics for $100\mu m$ diameter devices for wafers SPAD2, SPAD3 and SPAD4 while taking the devices to the breakdown voltage.

5.1 Ge passivation for the Ge-on-Si SPADs

One of the most critical issues that limits the performance of single photon avalanche diode (SPAD) detectors based on Ge-on-Si mesa epitaxial structure is the lack of good surface passivation. This leads to the deleterious effects from high surface density of states at interface (D_{it}) resulting in higher dark count rates (DCR). Hence, in order to lower these rates and be able to register some real counts, one needs to lower the operating temperature between $100K - 150K$ to limit DCR resulting from thermal excitations (4). To improve the Ge interface, interfacial control layers such as germanium oxides (GeO_2) and germanium nitrides (Ge_3N_4), which significantly lower the Dit_{it}, have been investigated and developed (88)(89). However the literature and our own investigation suggests that GeO_2 delivers lower D_{it} values than Ge_3N_4. In the literature, thermal oxidation (90) and plasma oxidation (91) methods are predominately used to produce high quality GeO_2/Ge interfaces, among which thermal oxidation provided the lowest to date D_{it} values - below $8x10^{10}cm^{-2}eV^{-1}$ (90). In this section, a plasma oxidation method has been investigated to grow ultra-thin GeO_x on epitaxially grown Ge-on-Si substrates, where the resistivity of Ge layer is $2.5\Omega \cdot cm$. The process flow is illustrated in figure 5.4. The substrate is initially pre-treated with cyclic buffered HF $(50:1)$ and

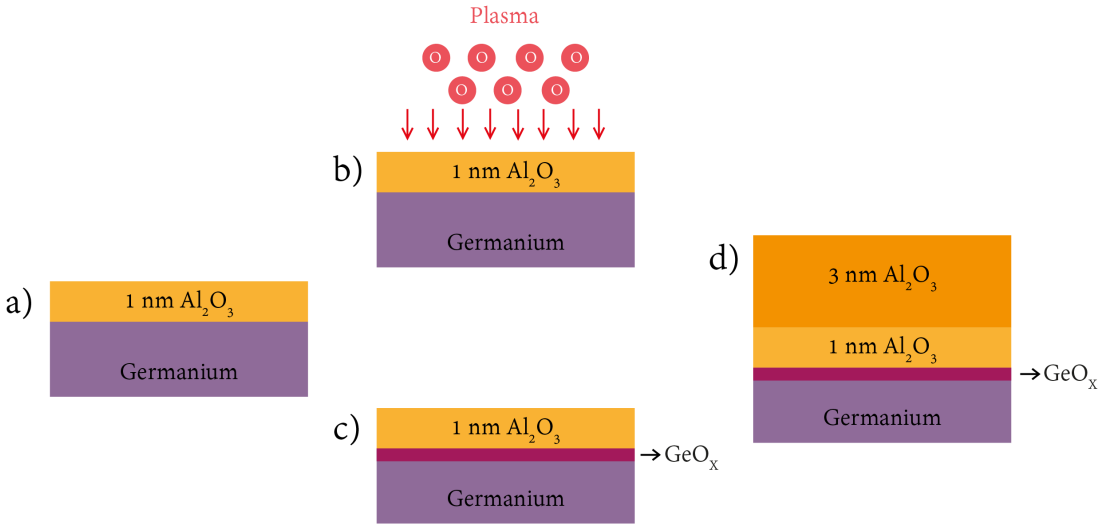

Figure 5.4: Illustration of plasma oxidation process to grow ultra-thin GeO_X

deionized (DI) water dips, before being loaded into Oxford Instruments atomic layer deposition (ALD) FlexAl cluster tool. The tool remotely generates the plasma to enable low temperature and low damage deposition of high-k dielectric materials. At first, $1nm$ thick Al_2O_3 is deposited at $0.13nm/cycle$ rate, using trimethylaluminum (TMA) as metal precursor and H_2O as oxidant at $200°C$. The substrate is then irradiated with inductively coupled plasma (ICP) oxygen plasma at $500W$, $100sccm$ and $50mTorr$ at $300°C$ between $1-10$ minutes. The oxygen atoms disperse through $1nm$ Al_2O_3 layer and react with Ge surface, to form ultra-thin GeO_X. Finally, $3nm$ Al_2O_3 is deposited as a cap layer to restrict the diffusion of GeO_X due to the presence of moisture in the atmosphere. All the above steps were performed in-situ taking advantage of the capabilities of the cluster tool. The quality of the deposited layers has been evaluated from circular MOS capacitors, fabricated using shadow masks which physically contact the surface of the sample allowing metal evaporation only in designed areas. Hence no resists or lithography steps were involved, reducing significantly the time needed for their development. Aluminium (Al) is used for both top and back gate contacts. At the end of the process the MOS capacitors were annealed in forming gas (FG) $(5\%H_2, 95\%N_2)$ at $350°C$ for 30 minutes to remove dangling bonds and trap charges from the Ge interface. The MOS capacitors were measured on Agilent B1500 semiconductor parameter analyser, equipped with multi frequency AC impedance measurement capability for

capacitance voltage (CV) measurement with frequency range between $1kHz - 5MHz$.

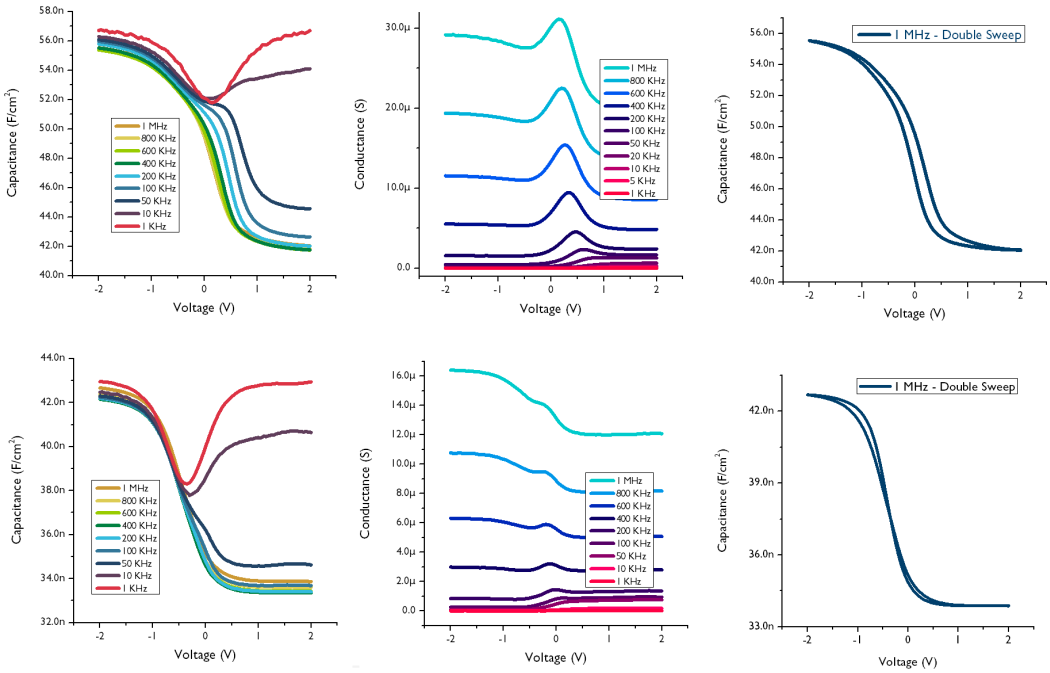

Figure 5.5: Capacitance and conductance measurements of a p-Ge MOS capacitor fabricated using plasma oxidation method. Figures on top are without and below are with FG treatment

Figure 5.5 shows the capacitance, conductance and hysteresis measurements of a p-Ge-MOS capacitor fabricated using the plasma oxidation method illustrated in figure 5.4. In the example discussed in the figure, the oxidation time was 5 minutes. Without the FG treatment, C-V measurements revealed a significant shift of over $2V$ in the depletion region as function of frequency, indicated the presence of large number of surface states which became dominant below $400kHz$. The minority carrier (electrons) response is clear in terms of the large dispersion in the accumulation region below $100kHz$. Moreover a hysteresis of $250mV$ has been observed at $1MHz$ indicating the presence of interface trap charges. After the FG annealing, a majority of these trap charges became neutral from hydrogen passivation, and thus improved C-V characteristics has been observed. A small shift in the depletion region, a deeper depletion region for low frequency C-V curves and negligible hysteresis at $1MHz$ means there

has been significant reduction of surface states. Moreover it has been observed that 5 minutes is the optimum oxidation time to grow GeO_X. C-V measurements from the MOS capacitors exposed to shorter (1 min) and longer duration (10 min) oxidation times revealed high frequency dispersion and large shifts in flatband voltage, possibly because shorter duration is not enough to grow sufficient interfacial layer of GeO_X to passivate the Ge surface, and longer duration has potentially removed the initial $1nm$ Al_2O_3 layer due to high ICP power.

Our Ge-on-Si SPAD detectors are mesa etched, therefore the passivation for Si-charge sheet and multiplication layer is equally important. MOS capacitors were fabricated on p-Si substrate using a thick $9nm$ Al_2O_3 dielectric layer. C-V measurements are shown in figure 5.6, where after FG treatment almost no frequency dispersion has been observed, moreover there is a negligible hysteresis seen at $1MHz$, indicating that the passivation is fully optimized to apply over the SPAD detectors.

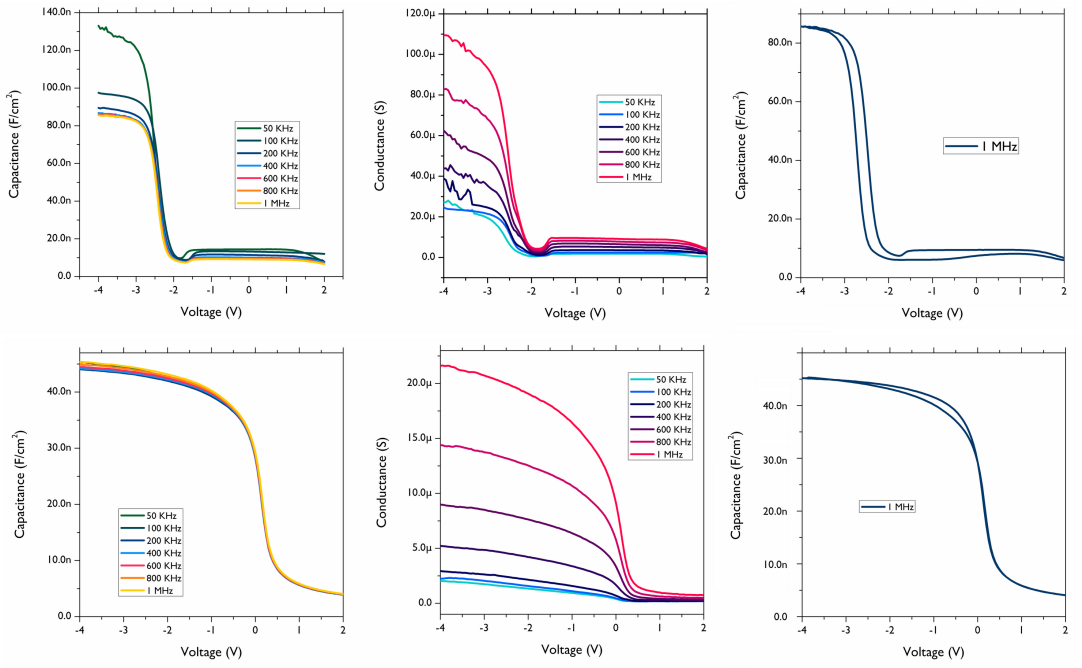

Figure 5.6: Capacitance and conductance measurements of a p-Si MOS capacitor fabricated using $9nm$ Al_2O_3 dialectic layer. Figures on top are without and below are with FG treatment.

Another method investigated for the passivation purposes was growing a thick layer of GeO_X in the oxidation furnace and then transporting it to the cluster tool where the cap layer of Al_2O_3 would be grown on top of it. Initial preparation of the surface and FG anneal post Al_2O_3 cap growth, were kept the same as in the case of plasma oxidation. Oxidation furnace was located outside of the designated clean area in another building which resulted in risk of exposure to the outside contamination and possible formation of native oxides during the transportation from the clean room. After growing the oxides, samples had to be transported back to the clean room for the ALD cap growth in cluster tool. Moisture in the atmosphere could potentially result in etching away oxides grown on the surface and replacing them with native oxide with much worse properties. Transportation was performed with the usage of the dehydrated vacuum box and went without any major issues. After performing capacitance measurements

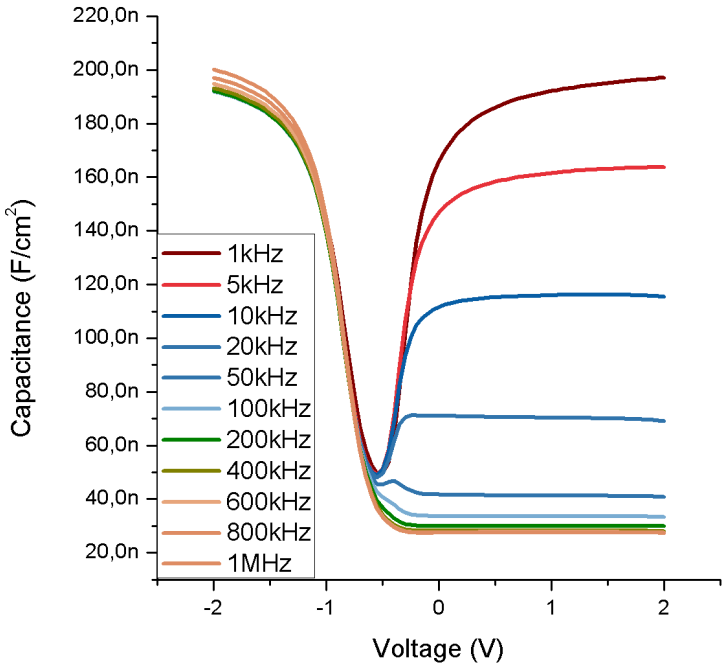

Figure 5.7: Capacitance measurement of a p-Ge MOS capacitor fabricated using furnace oxidation capped by Al_2O_3 dialectic layer. Figure represents sample with FG treatment

on the Ge sample prepared in the above ways it was observed that the quality of sur-

face passivation was much better than mentioned earlier method of plasma oxidation (Fig.5.7). This might be due to the quality and thickness of the oxide grown using the oxidation furnace. Therefore this method will be the primary method of passivation on which our future efforts will be focused.

Even though passivation using silicon nitride was proven in the literature not to be the one which produces the most outstanding results, a couple of samples will be developed using this method. This is mainly because of the relative quickness in relation to the other methods.

In the very first devices developed our dominant method of passivation was depositing SU8 on the sample surface, which was also serving as the planarisation method. Further studies on these samples suggested that the side surfaces of the samples were rather just locked from the influence of the environment rather than being properly passivised. It was also observed that samples were displaying better performance after the etch process but before performing any further production steps. This is because during the etch process side walls of the samples are undergoing simple passivation which is used during the etch process as a mean of achieving better verticallity of the etch. It stresses the importance of a post-etch ash which would strip this layer from the sample side walls. If this layer remains it would significantly inhibit ability of growing a good quality passivation layer.

Many different variations on initial cleaning, times and temperatures of growth and oxidation, temperatures and thicknesses of the initial Al_2O_3 layer, parameters for the plasma oxidation, length and temperature of the FG anneal were chosen after many trials. Results obtained from measurements performed on these MOS capacitors will provide the basis for production of a proper passivation layer on the side walls of SPAD devices for both Si and Ge regions of the side wall. Some samples were already produced and their quality will soon be investigated using Single Photon Detection Efficiency optical measurements.

5.2 Generation 12 Results

In this section I am going to present and discuss results obtained for the devices from generation 12. Chips in this generation are $1cm^2$ samples with different designs on each quarter. The differences are mainly confined to the relative size of the p++Ge top contact etch in relation to the underlying selectively implanted charge sheet. Design1 has a p++Ge of a smaller lateral size than charge sheet, Design 2 larger, Design 3 smaller and Design 4 is a full mesa etch reflecting previous design choices. These differences are explained in more detail in fabrication chapter and are presented graphically in Fig.4.4. Measurements presented in this section were taken at the Heriot-Watt University in collaboration with Peter Vines and Kateryna Kuzmenko.

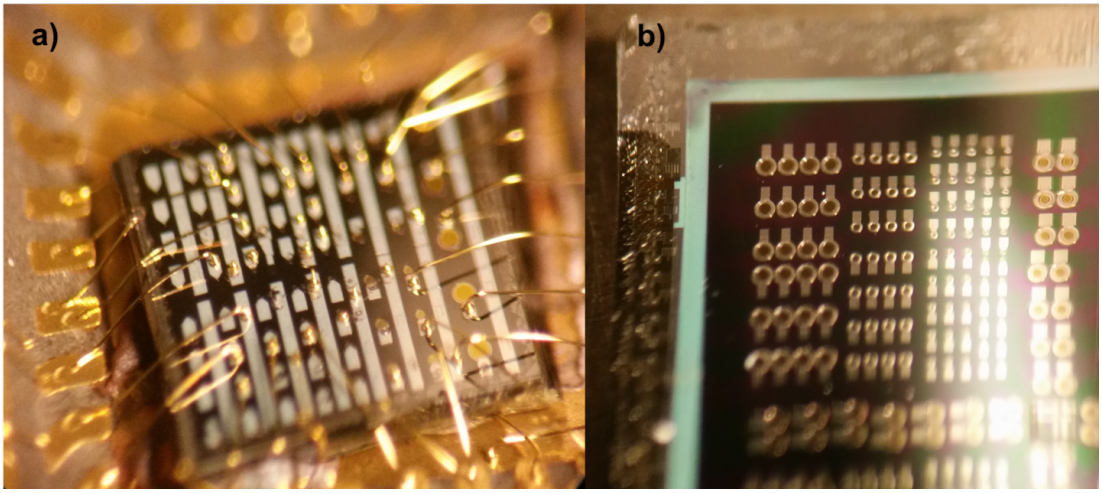

Figure 5.8: Microscope images of Gen12 device after and before cleaving and wire bonding.

A range of devices were fabricated in accordance to the design and fabrication details presented in the Fabrication chapter. Some of the chips in this series were fabricated with small changes to the overall process either due to time restrictions or to be able to focus on just one aspect of the device. As an example the first chip produced was only consisting of a mesa etch with a fully metal covered Ge p++ etch. Although not allowing for optical measurements, this variant was useful for a quick IV testing in the probe station, because of fully covered top contact allowing for direct probing without need for cleaving and binding, indicating if the design choices in this generation were

amounting to the devices different performance.

In the image Fig.5.8 b) one can see a microscope zoom in on one of the quarters on a fully processed $1cm^2$ chip before cleaving and mounting. In Fig.5.8 a) the microscope picture presents a zoom in on a $3mm^2$ opening in the header package that is used for electrical measurements inside the cryostat. The sample presented is a cleaved and fully bonded quarter of a chip.

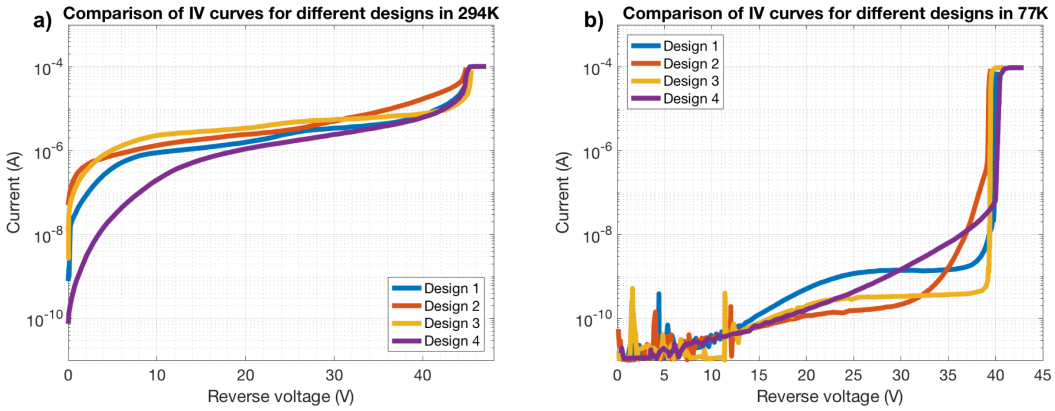

Figure 5.9: Comparison of Current - Voltage characteristics for different designs at temperatures of 294K and 77K.

Initial assessment of the sample quality was performed with running a simple IV characteristics in a cryogenic probe station, starting with testing $100\mu m$ in diameter devices for different designs. The results of these measurements are presented in the Fig.5.9. First IV characteristics were taken at the room temperature of 294K and are presented in the graph Fig.5.9 a). However, differences between the designs in this measurement were not immediately clear therefore it was decided to repeat this measurement at the liquid nitrogen cryogenic temperature of 77K (as presented on the graph Fig.5.9 b)). In this case differences between designs are amplified and first attempts at understanding the meaning of this data could be carried out. It can be observed that like in case of measurement in the 294K, IV curves of Design1 and Design3 are the most similar while Design2 and Design4 are the outliers. This can be explained as the Design4 is a mirror design of a previous generations of devices akin to one presented in (4), with the uniform rise in the reverse current before reaching breakdown. In the

Design2 the reverse current remains largely stable until rapidly increasing at around $30V$ and continuing to rise until reaching the breakdown voltage. For the Design1 and Design3 the reverse current remains stable up until reaching the voltage breakdown at which point it rapidly increases, with the current before breakdown being lower in the case of design 3. This clearly shows an influence of the relative lateral size of the p++Ge top contact etch relative to the selectively implanted charge sheet having a large influence on the overall device performance. As expected from the results in the simulation chapter a design where the top contact is smaller than the charge sheet is exhibiting the best IV characteristics due to the electrical field distribution being largely confined inside the mesa, keeping it from interacting with side walls of the device. This distribution is similar to the design with top contact of the same size as the charge sheet. This is reflected in the IV's with Design1 being the one most closely resembling Design3. The shape of the IV curve of the Design3 can be predicted to have a high performance because of its low dark current in the lead up to the breakdown, its low value before the breakdown, and sharpness at the breakdown which are good performance indicators as stated in (83).

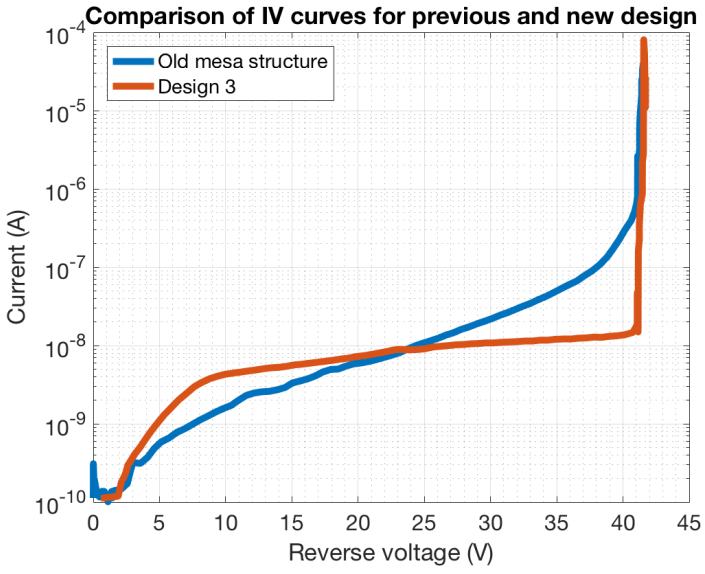

Figure 5.10: Comparison of Current - Voltage characteristics for two $100\mu m$ devices from a previous mesa design and current design 3 at 77K.

With that it was decided to focus testing on the Design3 as the most promising

one. Later on SPDE measurements were attempted for the other designs but the DCR inside of them was found out to be too high to allow for any SPDE measurements. Additionally in the Fig.5.10 one can see a direct comparison of the IV's for a $100\mu m$ diameter device form the Design3 and the old design performed in the 78K with a new design clearly possessing much lower reverse current in the lead up, lower current before and much sharper breakdown. This sharp breakdown can in turn be related to the lesser influence of the mesa surface on the electric field inside the active area as explained in (92) which is reasonable as for the Design3 electric field was intentionally kept away from the side wall unlike for the previous mesa designs.

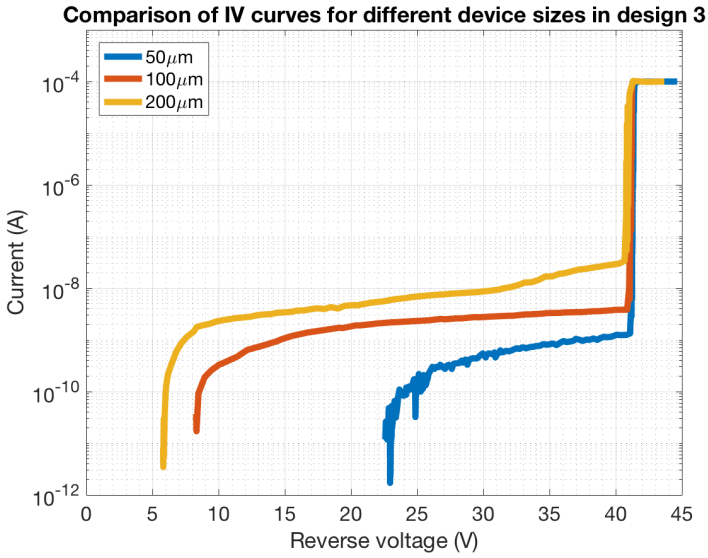

Figure 5.11: Comparison of Current - Voltage characteristics for three different device diameters from design 3 at 78K.

Measurements for different Design3 device sizes were performed. All of the measured ones displayed a trend presented in the Fig.5.11 with devices $50\mu m$, $100\mu m$ and $200\mu m$ in diameter measured at 78K. As can be seen, with decreasing device radius the current before breakdown decreases as well. Dark current before the breakdown decreases with decreasing device radius as well. As seen in the Fig.5.11 the IV curves for the devices shift towards the higher voltages with decreasing device size, because of the dark current being below the noise floor of the setup used for the measurements. The noise floor was removed from this figure for the sake of clarity so the point at which

the IV curve "begins" is in fact a point at which the current reaches values above the noise limit. It is no surprise that the devices of smaller sizes are displaying better IV characteristics since the overall generation of random carriers is proportional to the bulk volume of Ge. The low value of current before the breakdown voltage, coupled with a sharp breakdown is a good indicator that the devices would display lower dark count rates in the following measurements(92).

Although fabricated, $25\mu m$ in diameter devices are not presented in this work. Most of them either displayer an open circuit behavior or broke after few runs resulting in no devices left for the proper characterization. The reason for such a bad yield was deduced to be a poor quality metal contact deposition and it is explained in more detail in fabrication section. This problem, although on a smaller scale was also present in the $50\mu m$ diameter devices, making them unsuitable for consistent repeatable measurements, therefore our focus was largely directed towards the $100\mu m$ diameter devices. As explained above, devices with the smaller diameters are expected to posses much lower dark count rates allowing for higher temperature of operation and higher detection efficiencies than their larger counterparts, therefore it can be expected that better SPDE and afterpulsing for this design are achievable with an increased yield of the $25\mu m$ and $50\mu m$ devices.

We begin a closer examination of the samples with temperature dependent IV measurements for the $100\mu m$ diameter devices presented in Fig.5.12. A number of trends are observed in these IV's with decreasing temperature. This includes a minute decreased breakdown voltage, increased sharpness at which breakdown occurs and lowered dark current in the whole measured region. These features can be connected with lower amount of thermally generated carriers at the lower temperatures leading to less tunneling current resulting in device approaching a ideal IV curve for the reverse biased diode. Additionally at around 21V a bump in the current appears, that in the higher temperatures is largely obscured by the high dark currents. This bump is a so called "punch thorough" and it happens at the voltage at which electric field extends into the i-Ge region, sweeping the carriers generated in the Ge past the charge sheet into the Si therefore being registered as an increase of current in the IV characteristic. This is a key indicator of a device that would be able to perform light sensing since that requires

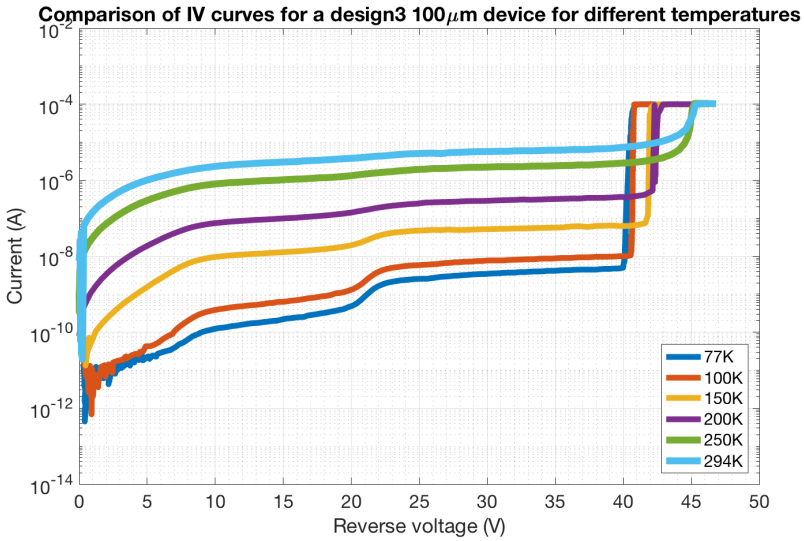

Figure 5.12: Comparison of Current - Voltage characteristics fora 100μm diameter device from design 3 at varying temperatures.

sweeping photo generated electrons into Si layer for multiplication.

All of the devices of the 100μm diameter were measured and it was found out that about 90% of all the devices that size were working and demonstrated very similar IV curves. That indicates both a uniformity of fabrication and uniformity of the material growth for larger devices and is especially encouraging if development of large arrays or a mass fabrication with such devices was ever attempted.

Following the fabrication the photocurrent of the devices was measured with 1310nm laser. A focused spot of 15μm was used, leaving some room for aligning the laser as the optical window diameter in the middle of the top contact was between 18μm for the 26μm diameter device up to above 100μm for the 200μm in diameter device. A sample connected to the header package was placed in the cryostat with an optical window and connected electrically. Although the illumination setup on top of the optical bench was set to be rigid, the positioning of the laser spot was possible by moving the sample inside of the cryostat under the laser spot position which was observed with a long focus range microscope focused on the sample surface. A more in depth description of the setup used for optical measurement is presented in the methods section. The chip

can be aligned relative to the laser allowing for the light to be moved across its surface.

While moving the laser spot across the optical window it was observed that the anti reflection coating layer was displaying slight thickness non uniformities. This could have been observed because of the anti reflection coating being fine tuned for the 1310nm wavelength, therefore making laser spot disappear from sigh for the correct thickness and appearing as a slight reflection in the case of being positioned on top of a thinner anti reflection coating region. The majority of the optical window however was possessing the right thickness allowing for least amount of reflection from the surface resulting in higher performance.

It was observed as well that, while moving the laser spot across the inner circumference of the top contact, there has been an increase in the resulting reverse current in comparison to laser spot being placed in the center of the active area. This phenomenon is most likely caused by the creation of local hot spots at the metal discontinuity area. A similar effect was observed with hot spots appearing in the simulation under the metal's only discontinuity at its outer circumference. It can be therefore deduced that such localized hot spots would appear at any metal discontinuity or like in this case on the inner circumference. To achieve more certainty a simulation would have to be performed on a 3D structure with a metal ring on top, since 2D simulation would result in a different kind of symmetry of the hot spot. This however is beyond the resources available for such a minute issue.

IV measurements with a flood illumination with a 1310nm laser were performed to confirm that devices fabricated are acting as photo detectors. In the Fig.5.13 the photocurrent of a $100\mu m$ diameter device at 78K is compared to the dark current. A clear difference between light and dark conditions can be seen, indicating that the device is indeed acting as a photo detector. Especially prominent in the IV curve for the illuminated condition is the presence of punch through (described earlier) positioned at around 20V. This really high response is a result of photo generated carriers being swept from the Ge absorption region into the Si, which in turn is a result of the electric field extending past the charge sheet into Ge. This photo response was uniform across all working devices of this diameter as well as larger devices. In previous generation

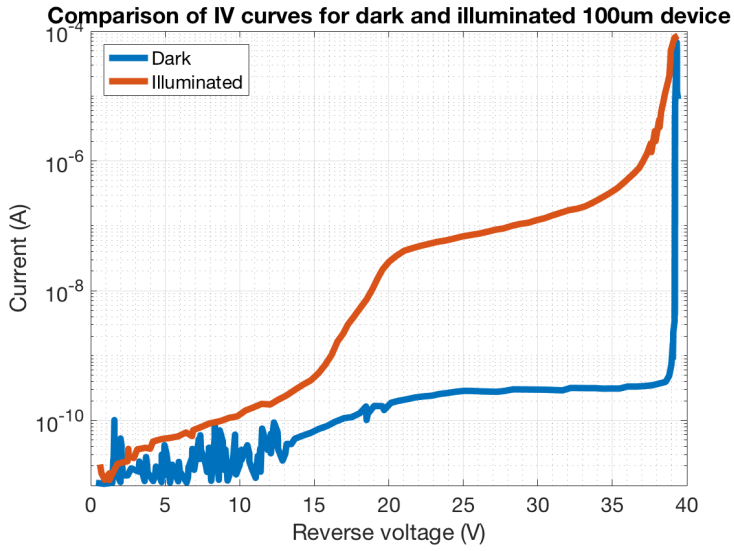

Figure 5.13: Comparison of Current - Voltage characteristics for the 100μm diameter device at 78K while in absence of light and illuminated with 1310nm laser.

devices this response was much weaker, indicating that they were less light sensitive and that this generation should exhibit a high single photon detection (4). With that in mind single photon detection efficiency and dark count rate measurements were attempted on the selected best performing 100μm in diameter devices.

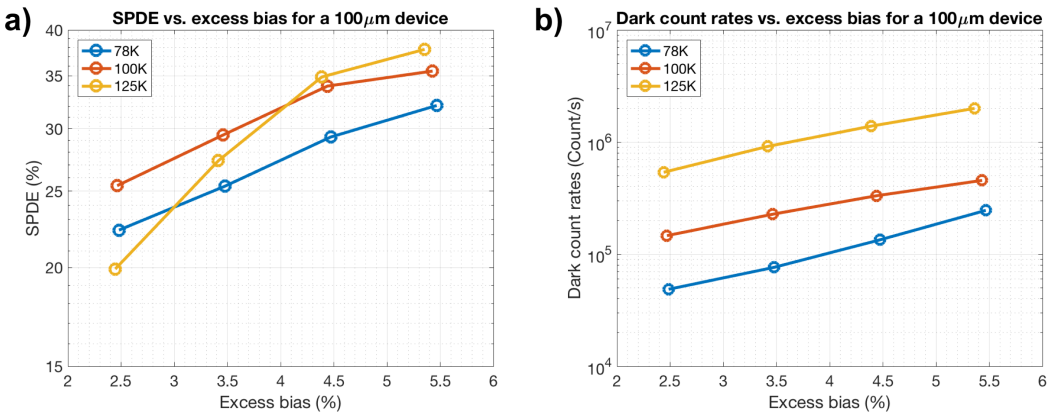

Figure 5.14: Single Photon Detection Efficiency (left) and Dark Count Rate (right) vs excess bias for a 100μm diameter device for different temperatures while illuminated with a 1310 nm laser at a repetition rate of 1 kHz.

In the figure Fig.5.14 a) I present results of the Single Photon Detection Efficiency (SPAD) and Dark Count Rates (DCR) in the figure Fig.5.14 b).
The dark count rate is defined as the number of times device registers a count in a given time period. In this case count refers to a an event where an excited carrier triggers an avalanche in the absence of light. This can happen due to the random carrier generation inside the device, either due to the thermal excitations or trap states being vacated.

As can be seen inf Fig.5.14 b) DCR decreases with decreasing temperatures. This corresponds to a decreased carrier generation due to the thermally assisted lattice vibrations. At low temperatures they are less likely to provide enough energy for an electron to be excited to a higher energy band and potentially being swept into Si and partake in the current generation.

On the other hand one can see that for a given temperature DCR increases with increasing excess voltage bias. Excess voltage bias is a proportional value of amount of voltage that the device is biased at in proportion to the breakdown voltage bias. Increasing this value result in the increased DCR due to the higher probability of tunneling which is being known to cause high DCR at higher excess biases (93). In general DCR can be understood in relation to the dark count probability and expressed as:

$$DCR = -\frac{ln(1 - P_d)}{\tau_e} \tag{5.1}$$

where $\tau_e = \tau_p - t_d$ is the effective pulse width and τ_p is a width of a given pulse and t_d is the difference between the with of the pulse being applied and the with of an effective pulse and P_d is a dark count probability .

Single Photon Detection Efficiency presented in figure Fig.5.14 a) is a value describing how likely is our device to detect a single photon and can be understood in the form of an equation as:

$$SPDE = \frac{1}{n} ln\left(\frac{1 - P_d}{1 - P_t}\right) \tag{5.2}$$

where n is the average number of photon per pulse and P_t is the total probability of triggering an avalanche event. For the single photon measurements average number of photons per pulse is kept below 0.1 photons per pulse reaching top of the device.

As can be seen in figure Fig.5.14 a), SPDE increases with increasing excess bias, thanks to more of the photo generated carriers having enough energy to cross into the Si and higher probability of triggering an avalanche event. It also increases with temperature up to 38% at 5.3% excess bias. This is an unprecedented value, higher than anything previously recorded for a Ge-on-Si SPAD architecture (94) (54) (4) (5). These are also first Ge-on-Si devices to achieve a comparable efficiencies to these registered to InGaAs/InP (95) (96) (97) type devices at comparable running conditions as presented in the 6.1 . This excessively good performance can be attributed to the new design choices described in the earlier section reducing DCR significantly as well as a good quality 1.5μm of Si multiplication layer being thick enough to ensure that the photo generated carriers that cross charge sheet can travel far enough to create additional carriers through the impact ionization mechanism and therefore become multiplied to a point at which their effect can be registered. Measurements were attempted at higher temperatures to achieve even higher SPDE rates, but they were unsuccessful due to very high DCR. This could hovewer be overcome in the next batch of devices that would have working devices of smaller diameters which would have lower DCR allowing for higher temperature operation.

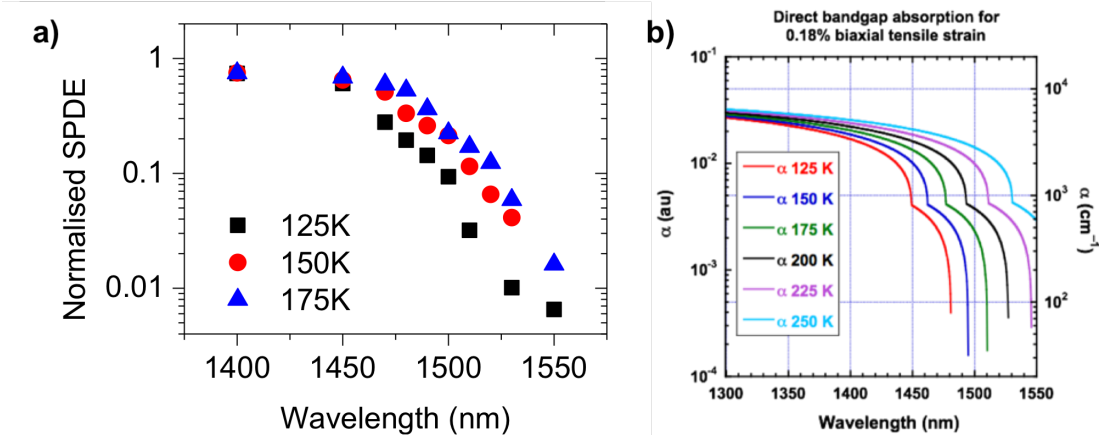

Figure 5.15: On the left - Normalised Single Photon Detection Efficiency vs. the incident wavelength for the 100μm diameter device in three different temperatures. On the right - Simulated spectra of the Ge absorption coefficient at different temperatures, with a residual biaxial tensile strain of 0.18% of Ge layers grown directly on Si considered.

For the temperature of 125K it can be observed that there is quite a significant

change in the way SPDE changes with excess bias starting with values lower at the low excess bias and reaching values higher than for any other temperature at higher excess bias. Although it might be challenging to pinpoint an exact cause for this behavior, the most likely candidate is a shifting Ge absorption curve with changing temperatures. To help with visualizing that, measurements of SPDE were conducted at varying wavelengths from 1310nm to 1550nm using tunable NKT Supercontinuum laser at temperatures of 125K, 150K 175K results of which are presented in Fig.5.15 a). Since the part to be investigated is an absolute shape of the SPDE curve results for these 3 temperatures were normalized. It is known that the Ge band gap responsible for absorption in this region would change for different temperatures therefore a simulation was performed of temperature dependency curves for Ge with a residual biaxial tensile strain of 0.18% of Ge layers grown directly on Si (98) to use as a reference. Results of these simulations are presented in Fig.5.15 b). Measured data matches the trend of relative curve and changes to a satisfying extent, which could partially explain unexpected behavior of SPDE vs Excess Bias values for temperature of 125K. This however would require a lot more of in depth investigation to confirm. However, if the trend where SPDE increases with increasing temperatures would continue that could potentially lead to an interesting feature. The increase of operational temperature would cause a shift of Ge absorption curve towards longer wavelengths, increasing significantly absorption coefficient at wavelengths close to 1550nm. This could potentially lead to an increase of the SPDE at lower wavelengths. Higher operation temperature would also simplify and reduce the cost of packaging required, as devices could be operated on top of a Peltier cooler rather than cryostat, significantly reducing the manufacturing price. However DCR at higher temperatures would have to be reduced first so the single photon operating mode would be possible. This could be achieved by reducing overall size of the device which would be discussed in the later section.

As a way of further investigation cut-off wavelengths for different Ge thicknesses were calculated utilizing the Varshni parameters (99) (these are the parameters that allow for calculation of the temperature dependence of the band gap energy in semiconductors). In this case cut-off wavelengths were defined as the wavelengths at which the detector's SPDE is 50% of the SPDE at 100K for 1450nm wavelength. Wavelength of 1450nm was selected as it is a wavelength which is at the end of the flat part of

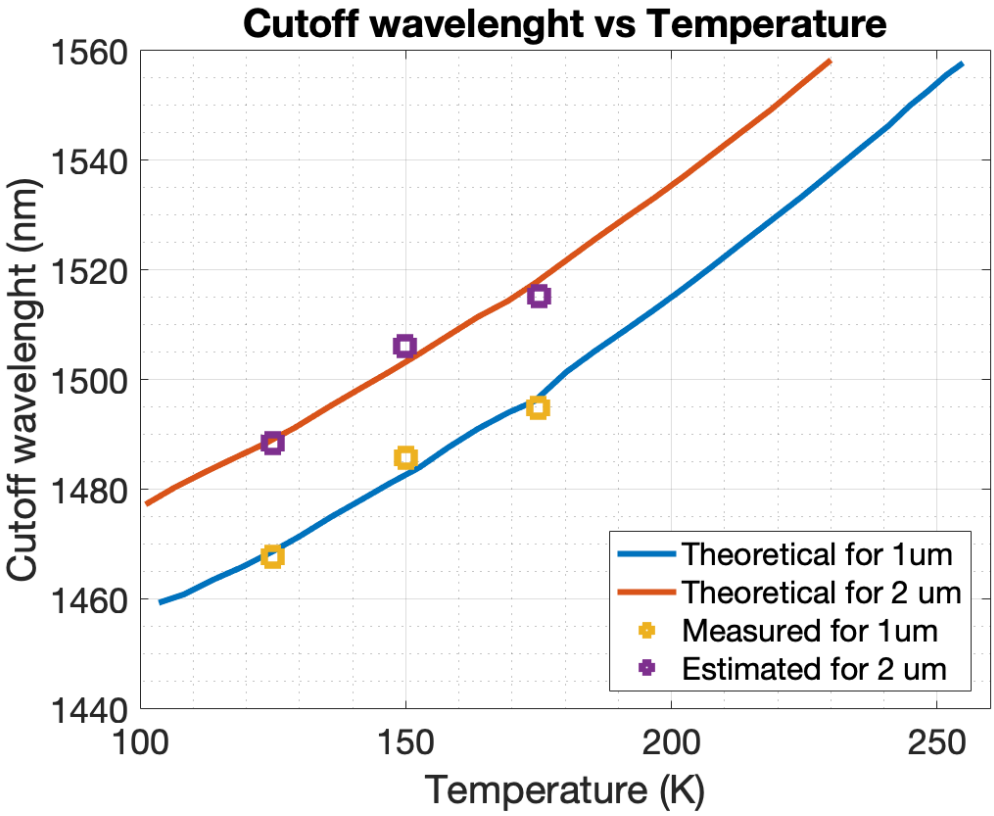

Figure 5.16: Cut-Off wavelenghths as a finction of temperature for $1\mu m$ and $2\mu m$ thicknesses of Ge absorption region.

absorption coefficient curve. Results of this investigation are presented in the Fig.5.16 where the theoretically obtained curve is compared to the measured results. As can be seen measured values are in good alignment with theory, suggesting that this curve could be used for predicting values of cut off for higher temperatures. From it one can read that the cutoff wavelength would move to the desired 1550nm at the temperature of 245K, which is a temperature that might prove difficult to achieve even with the smaller devices in this design available. However this would require more data to confirm it. Another possibility to reach sufficient absorption coefficient at 1550nm was therefore investigated. On the right hand side of Fig.5.16 are presented simulated curves and predicted values for the devices of our current design if the thickness of the Ge absorption layer was increased to $2\mu m$. As one can see this results in lowering the required temperature to achieve cut-off wavelenght at 1550nm to about 220K which

is a much easier to achieve temperature. Additionally, increasing the Ge absorption layer thickness would greatly increase the absorption probability of incoming photon potentially resulting in devices of much better SPDE. For the Ge thickness of $1\mu m$ used in current devices it can be calculated from the single crystal Ge absorption coefficients (3) that less than 50% of the incoming radiation actually gets absorbed. As calculated from Beer's law a $2\mu m$ thick Ge would result in an absorption of over 70%. This would in turn result in the increased SPDE to potentially above 55% while at the same conditions as current devices, resulting in a better detection efficiency than that obtained by InGaAs/InP SPADs (95) (96) (97). The downside of this increased thickness lies in difficulty to grow thick Ge with sufficiently low dislocations on top of Si, this however could be overcome by incorporating the selective area Ge growth as explained in the methods section. Even thicker Ge absorption regions would result in the further increase in the efficiency, but fabrication of such layers would require waveguide style approach. In this approach the absorber region could be a Ge waveguide on top of Si, which would allow for much longer travel distances inside the Ge of incoming photons.

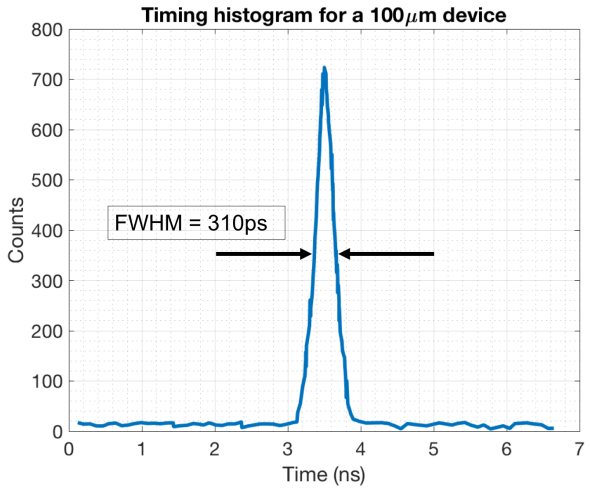

Figure 5.17: The jitter diagram for a $100\mu m$ diameter device at 78K, excess bias of 5.4%while illuminated by a 1310nm laser. The full width at half maximum (FWHM) being 310ps.

Another important characteristic quantifying performance of the photo detector is timing jitter. In the case of photo detector jitter is defined as a Full Width at Half

Maximum (FWHM) of the SPAD timing response. In a broadest sense it represents a precision with which we can determine the arrival time of the photon onto a device. Timing jitter in the presented case would consist of combined variations of the laser pulse width, contribution from the rest of the system including electric components and a variation in timing response of the detector itself. The fact that the peak of counts on the background of dark counts can be observed is a proof for the single photon detection operation mode (since the device is illuminated on average with less than 0.1 photon per pulse). It can be measured utilizing time-correlated single photon counting (TCSPC) (100) setup when the detector is illuminated with a highly attenuated pulsed laser (on average less than 0.1 photon per pulse) with short pulse duration. Its overall value is heavily influenced by the thickness of multiplication region, since a thicker multiplication region results in a more carriers being generated in the avalanche event increasing the overall time needed for it to subside. Another contributing factor is a variation of a laser pulse itself, which can differ up to 50ps As can be seen in Fig.5.17 which was taken for $100\mu m$ device at 78K, 5.5% excess bias and illuminated by a 1310nm laser its value for our devices is at 310ps. This is a value comparable to the ones presented in the literature (34) (101). Like in previous characteristics of our SPAD device this figure is expected to exhibit better properties for the smaller devices (102) as well as with improved connection to the header package and better voltage delivery and readout systems.

Noise Equivalent Power (NEP) is a figure of merit for the SPAD which allows for better comparison between SPADs of different designs. The NEP is defined as the signal power required to attain a unity signal to noise ratio within a 1-s integration time and can be expressed as:

$$NEP = \frac{h\nu}{SPDE}\sqrt{2DCR} \tag{5.3}$$

where h is a Planck constant and ν is a frequency of radiation used for illumination. This value was calculated to be $1.9 \times 10^{-16} WHz^{\frac{1}{2}}$ which is a fifty fold improvement as compared to the previous bes performing Ge-on-Si SPAD of $3 \times 10^{-16} WHz^{\frac{1}{2}}$ and $7 \times 10^{-16} WHz^{\frac{1}{2}}$ for temperatures of 100K and 125K (4). It is also comparable to the commercially available InGaAs/InP detectors as shown in 6.1.

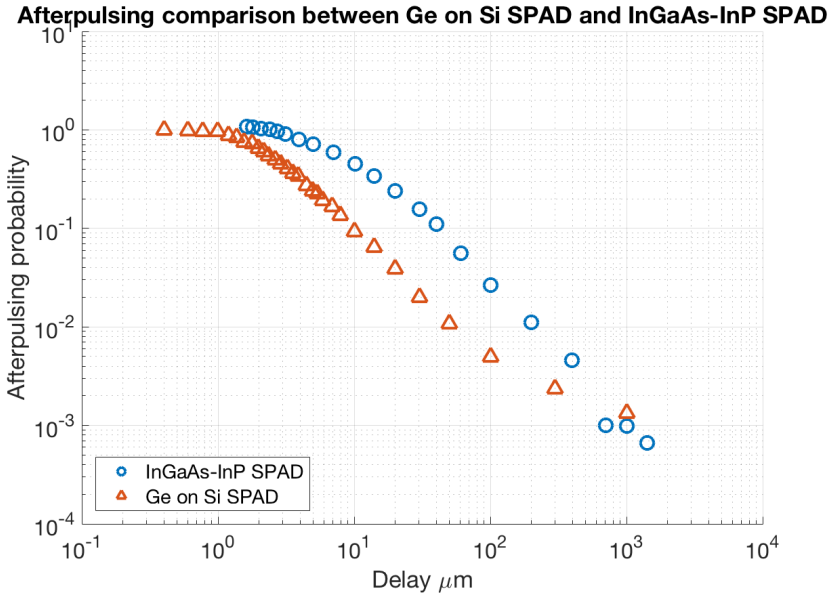

Figure 5.18: The afterpulsing probability for a 100μm device compared with a commercially - available InGaAs/InP Single Photon Detector when measured at 1310 nm wavelength and operated at a SPDE of 17% and a temperature of 125 K.

An investigation of afterpulsing has followed. This phenomenon is related to the carrier traps in the crystal that are created by the impurities (or discontinuities) of the crystalline lattice. During the avalanche event (triggered either by incoming photon or a thermal carrier generation while device is biased above the breakdown) a large amount of carriers travels through the device. Some of these carriers can become trapped in the trapping centers. After device is quenched causing the avalanche current to subside these trapping centers start releasing carriers. These released carriers can then cause an avalanche effect if the device was to be brought above breakdown voltage in the time of their release. Since these trapping centers would naturally depopulate with time, longer the delay between gate that populated them and a new gate, the lower chance of these centers still being populated and releasing carriers. Therefore longer delay between gates would lower the chance of a dark count caused by carrier being released from a trapping center. Therefore afterpulsing is a value that measures a probability of another avalanche trigger happening after the photon detection due to release of carriers in the trapping centers causing another avalanche event. It can be easily mitigated by extending time between measurements to allow all of the trapped

carriers to be swept before proceeding with next measurements. However, this would result in a significant decrease of possible rate of detection which would be a great hindrance for achieving a high rate photo detector. This rate is heavily influenced by the quality of multiplication region, which because of an ability to grow really high quality Si multiplication layers for our devices is significantly better than in case of InGaAs/InP where high trapping density of InP is know to heavily influence that rate (103) (104) (105).

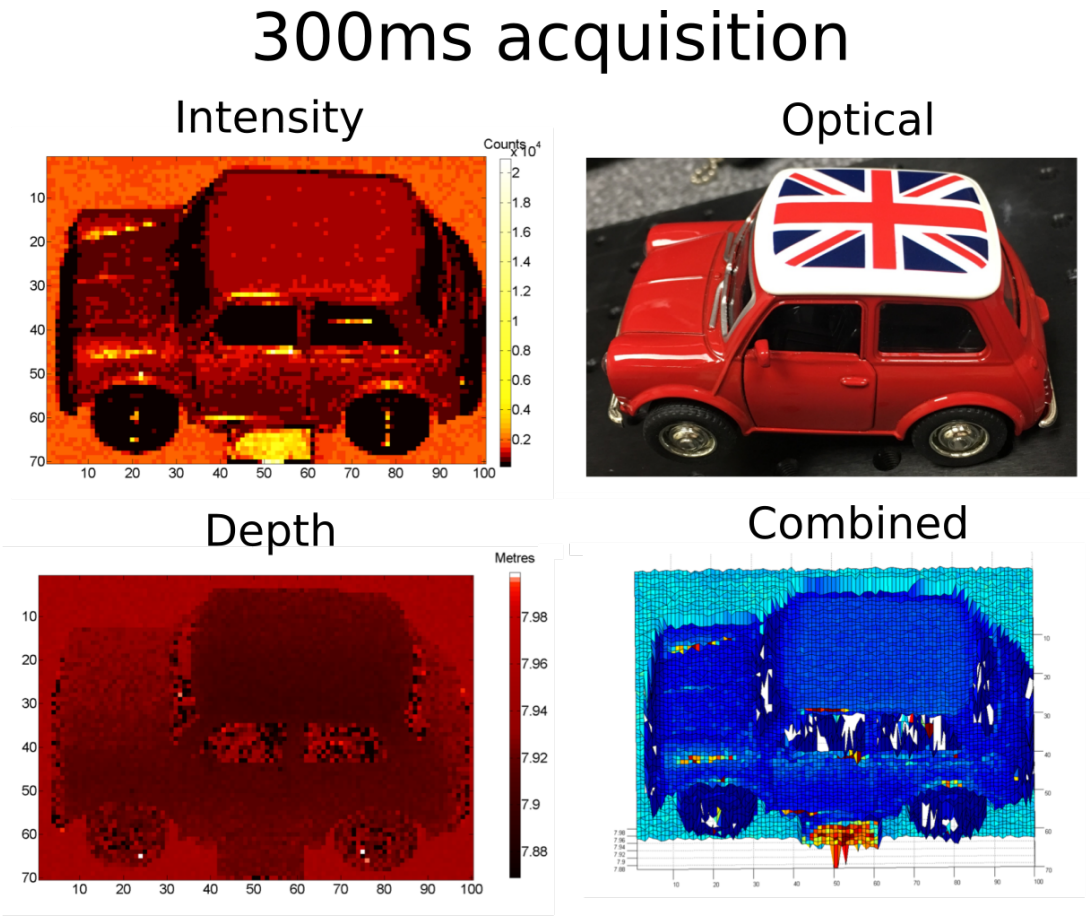

Figure 5.19: Proof of concept in lab LIDAR measurement performed with 100μm diameter Ge-on-Si SPAD device.

The values presented in Fig.5.18 were obtained by causing a photon induced avalanche event on a 100μm device at 125K with 1310nm illumination, after waiting for a certain delay time the device was brought up to the excess bias again without illumination.

Instances in which another avalanche event occurred were counted to extract the afterpulsing probability for a given hold-off time. As one can see, Ge-on-Si devices exhibit smaller afterpulsing probability therefore allowing for faster repetition rates than InGaAs/InP based technologies reaching 80% faster possible rate at 10μs delay time making it a much more viable technology for high repetition rate applications such as LIDAR.

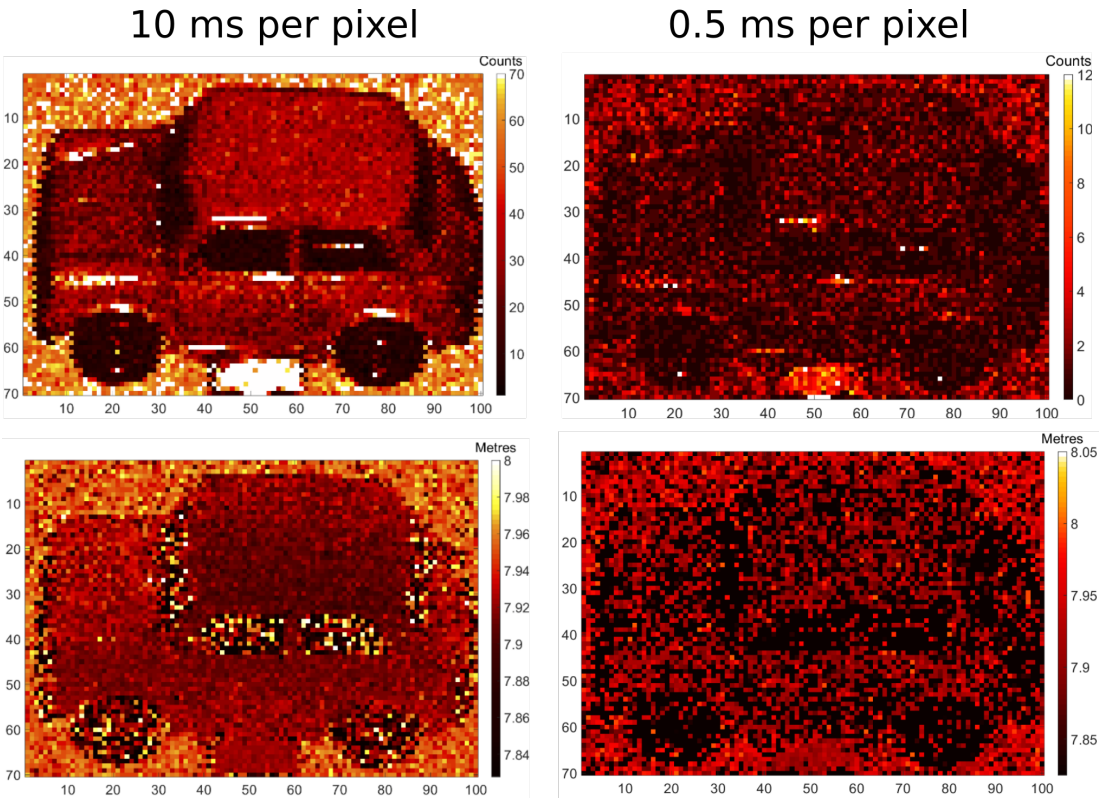

Figure 5.20: Intensity (top) and depth (bottom) measurements for the single pixel 100μm diameter Ge-on-Si SPAD device for acquisition time of 10ms and 0.5ms per pixel.

Lastly a proof of concept LIDAR measurement was attempted utilizing our device. Presented in the Fig.5.19 is a LIDAR image of a toy car with approximate size of 9.5cm x 6cm x 4.5cm(L x W x H) performed with a 100μm in diameter single pixel device at 100K, repetition rate of 104Hz,1450nm laser with 912 pW, spending 300ms per pixel. The picture consists of 100x70pixels and since the sample in the cryostat cannot be moved to a great extend, imaging was performed by mounting a toy car on top of a

optical stage and moving it to a new position for each pixel. Combined readings of intensity (top right figure) and depth (bottom left figure) were used to create a LIDAR image (bottom right figure).

We have then proceeded with acquisition of more intensity and depth measurements of an object with reduced time of acquisition per pixel. This was done in order to asses how long of an acquisition time (for these $100\mu m$ in diameter devices) would be required in order to still obtain decipherable images. As can be seen in the Fig.5.20 reducing the acquisition time to 10ms acquisition time per pixel still yielded an image where one could easily see an outline of the object. While reducing the time to 0.5ms however, the images loose most of their resolution making it hard to see outline of the object.

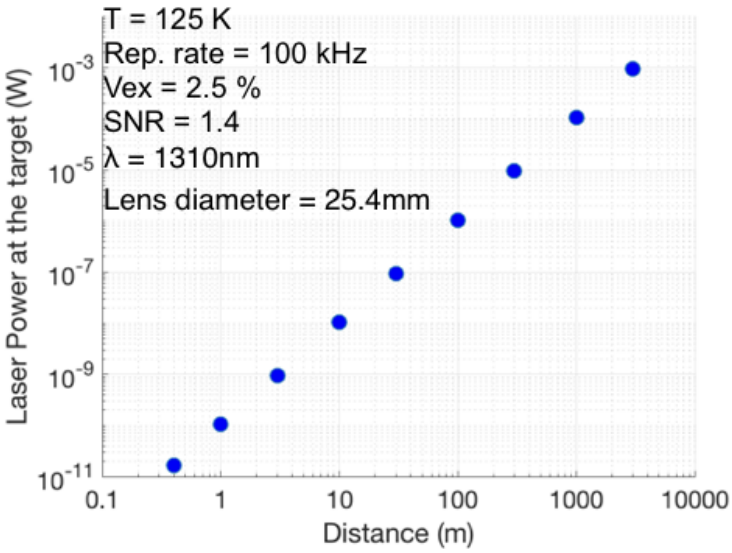

Figure 5.21: Extrapolation of the laser power required for the outside of lab LIDAR measurements for 10ms acquisition time.

With the information about LIDAR capabilities of our $100\mu m$ device we have proceeded with extracting information about the potential device performance in the outside of lab ranging applications. The Fig.5.21 is a graph representing required laser power to achieve LIDAR ranging at given distance with acquisition time of 10ms and while illuminated with 1310nm laser. As one can see, to achieve highly sought for by industry 1km ranging laser power required would only be around 10^{-4}W. This required

power is still below the eye safe threshold limit making it a very promising technology for the automotive/autonomous vehicle LIDAR applications. It is important to note as well that this device was relatively large in size, which resulted in high DCR. For devices of smaller sizes performance of the device would be much higher. This device was as well not optimize for these sort of measurements (since it was a first generation device) and with improvements to the bonding and contact optimization one would expect further increase in the ranging capabilities.

All the results presented above indicate that the change in a design have resulted in the significant increase in the overall performance, highlighting that Ge-on-Si technology has potential to be a suitable competitor of a InGaAs/InP technology especially while taking into consideration potentially much lower costs of the Ge-on-Si technology and reduced rate of afterpulsing. If the high SPDE at 1550nm were achieved this could lead to even further applications in QKD. To even further increase their performance an effort has been made to improve upon this design with a special focus on manufacturing robust small devices.

6

Conclusion and future work

In this thesis I have discussed the motivations, design and results of a novel approach towards Ge on Si separate absorption charge multiplication (SACM) single photon avalanche detector (SPAD) architecture. In the following Conclusions section I am going to present an abbreviated version of the discussion present in the main body of this work while giving an emphasis on major points in the chapters. The future work section will include an short outline of ideas and improvements that could be incorporated in the upcoming designs of the Ge on Si SPAD with potential benefits arising from these changes.

6.1 Conclusion

In recent years there has been a significant growth in interest in single photon detection in the infra red wavelengths. With a myriad of applications in quantum technologies such as quantum key distribution, quantum computing, security sensors, ghost imaging and LIDAR applications. With so many potential applications for both private and military sectors, it is not surprising that the UK government has announced in 2013 a £270M program for accelerated implementation of quantum technologies in private and military sectors. The current lack of technologies that could fulfill all the requirements for applicable automotive LIDAR makes the development of technologies in this niche especially tempting. Especially while taking onto consideration over US$800M being invested in the LIDAR companies over the past two years and a predicted market

Technology	**ID Quantique ID230**	**MPD**	**Current result**
Material	InGaAs/InP	InGaAs/InP	Ge/Si
SPDE	25%	25%	38%
NEP(W/$\sqrt{Hz}$)	7.2×10^{-18}	1.6×10^{-16}	2.0×10^{-16}
DCR(Hz)	200	5×10^{4}	2×10^{4}
Timing jitter (ps)	200	200	310
ITAR	US Source	US+EC Source	UK Source
Relative cost	$ 24k	$ 20k	Research

Table 6.1: Comparison of the commercially available InGaAs/InP type devices with a Ge-on-Si SPAD presented in this thesis.

growth of US$28 billion in automotive LIDAR applications until 2032.

Wavelengths between 1310nm and 1550nm are the most interesting range for automotive applications. Utilizing these wavelengths would provide the best possible penetration length for the laser because the atmospheric absorption is heavily decreased in this range, for various environmental conditions like snow, rain, fog and haze. These wavelengths allow as well for low operational power below the eye safe threshold limit A wavelength of 1550nm being of particular interest because around this wavelength the influence of background solar radiation is significantly reduces providing device operation without excessive environmental noise. In this thesis is presented a new device that fulfills these requirements. This is a new class of Ge-on-Si devices that could allow for a low cost IR SPADs capable of being mass produced at a fraction of the cost of the current state-of-the-art InGaAs/InP SPAD.

A single photon detector based on the superconducting nanowires is a technology that exhibits the highest SPDE in the SWIR region. These devices display very high SPDE's up to 90% and average values of afterpulsing in a wide range of wavelenghts. However, requirements to operate at cryogenic temperatures, poor scaling and high manufacturing costs make them unusable for the mass scale out of lab applications.

Currently the only SPAD architecture present on the market that fulfills some of the requirements for automotive ranging in based on SACM InGaAs/InP. These de-

vices, however, present many issues that make them unlikely candidates for massive adaptation in autonomous vehicles. They display a high rate of afterpulsing that significantly reduces their detection rate capabilities. They are also costly to produce, with the elements used being of high price due to the high cost of the wafers that are 500-1000times more costly than Si wafers, in addition to difficult and costly fabrication processes particularly while considering large arrays of devices. Commercially available arrays consist of 32x32 devices and are priced at about £120K. Additionally, the process required for their fabrication is not compatible with the CMOS production lines, therefore it is unlikely that their prices would drop below the current prices of £20k per package detector anytime soon. Since this technology is ITAR protected as well it becomes unusable for certain applications, with military applications being these most sought for.

As an alternative to InGaAs/InP devices we present a Ge on Si SACM SPAD device. One advantage of this technology is that Ge and Si are cheaper to produce and process than InGaAs and some of the Si CMOS production lines already utilize Ge in them, making both fabrication and modifications to the CMOS lines to achieve mass production of devices much cheaper. Additionally, usage of Si as a multiplication region allows the devices to achieve lower afterpulsing probabilities that would result in the ability to perform measurements at higher rate than the InGaAs/InP devices.

The SACM type structure represents a basic overall design architecture of our devices, where i-Ge acts as an absorption layer, p+ Si the layer acts as a charge layer and layer of i-Si acts as a multiplication layer. This structure accommodates for the avalanche operation mode.

Potentially, manufacturing of a Ge on Si SPAD device could be as easy as adding an additional Ge epitaxial growth step at the end of the Si photodetector production line. This would therefore extend its detection range to 1550nm. This advantage alongside a massive reduction to production costs makes Ge on Si type SPADs great fit for the purposes of automotive/autonomous vehicle LIDAR applications.

	DCR Density $[counts/s/\mu m^2]$		**SPDE** [%]		**DCR** $[kHz]$		**Temperature** $[K]$		**Device area** $[\mu m^2]$
This work	6.37	18.3	22	26	50	140	78	100	7850
Warburton(4)	11200		4		5500		100		490
Martinez(5)	31400		5		500		80		15.9

Table 6.2: Comparison of the recently developed Ge-on-Si SPAD devices with the device presented in this thesis. Measurements of our device presented here were performed in the similar conditions as the devices from other groups in order to make more accurate comparison possible.

6.1.1 Results

Devices presented in this thesis were produced in the James Watt Nanofabrication Center which is a 1350m^2 state of the art cleanroom facility with over £35M of nanofabrication tools for the purposes of dry and wet etching, metalization, photo and e-beam lithography and various metrology and imaging tools. Fabrication at the nano-scale is a challenging process that requires a lot of process development and a deep understanding of the processes and surface chemistry of the used materials. Some parts of the fabrication process are simplified by the most difficult equipment being operated by a qualified technical stuff where there is only the need to submit a set of process parameters for a given fabrication step. This semi industrial mode of operation significantly reduces the time necessary for some of the processing steps.

To achieve devices capable of high single photon detection efficiencies, there was a need for a number of specific designs to be simulated before wafer production could begin. Using a Poisson solver, a required value of the charge sheet doping was determined to be $2 \times 10^{17} cm^{-3}$. The charge sheet of this doping would ensure that field distribution inside of the device would be such, that when Si multiplication layer is at the breakdown, there is only a small electrical field in the Ge absorption region.

Initially a mesa etch type design was attempted, however this resulted in low values of SPDE of 4%. It became apparent that a new approach to the overall design was required in order to achieve an increase in single photon detection efficiency and a reduction of dark count rates. Interaction of the electric field with the side wall of a mesa

etch was hypothesized to cause an increase in the dark count rates. Having an exposed side wall also meant that it was necessary to perform a challenging passivation process. After deeper investigation it was decided that a planar structure akin to the ones prevalent in the design of InGaAs/InP devices should be incorporated in order to nullify the challenges associated with the side walls. To achieve this a design of wafers with an embedded charge sheet was investigated. Such an embedded charge sheet would act to define an active area of the device without the necessity of performing a side wall etch, therefore resulting in a fully planar structure. However, due to the finite background doping, a current leakage between devices was observed.

To solve the problem with leakage current between devices it was decided to perform an isolation etch. The isolation etch was performed at a distance (spacer) from the active area of the device with an additional top contact etch. This top contact etch is relative in size to the underlying selectively doped charge sheet. From these investigations it became apparent that a design with an etched top contact (with a lateral size smaller than underlying charge sheet) and an isolation etch at a certain lateral distance from the embedded charge sheet, was the most promising design to continue to the fabrication stage with. For this design the embedded charge sheet prevents the electric field spreading to the edges of the device, therefore, reducing interaction of the electric field with the side walls. Additionally, the smaller etched top contact keeps the field in the Ge more localized within the active area and also reduces the hot spots created at its etch edges.

Devices were fabricated in the cleanroom with photolithography processes. A dry etch was utilized for deep etches and wet etches for surface preparation. Metalization was carried out in the e-beam metal deposition tool.

Optical measurements on the devices were performed with illumination with < 0.1 photon per pulse on average. This guaranteed that there would be either no photons or at most 1 photon in a pulse, with a negligible probability of 2 photons. This ensured that we were operating in the single photon regime. The devices were characterized with a time correlated single photon counting technique. Gated measurements were performed to switch the detector to above avalanche breakdown with a gate length of

50ns in synchronization with the arriving photon. This type of measurement was used to generate the timing histogram, allowing the determination of the difference between dark counts and photon counts. The Full Width Half Maxima was measured to be 310ps at 78K for a $100\mu m$ diameter device. The peak in the timing histogram with single photon illumination above the dark current, is evidence that the single photon counting does happen in the device. In this case this value would be largely influenced by the lack of optimization of the packaging and contacts and is expected to be decreased in the next generations of the devices. Following this we acquired values for the single photon detection efficiency (SPDE) and dark count rates (DCR) vs. excess bias at different temperatures while illuminated by a 1310nm laser with < 0.1 photon per pulse on average. We have observed that SPDE increases with temperature and excess bias, reaching a record breaking 38% SPDE at 125K in 5.5% excess bias (compared to previously reported 5.27% (5)). A limiting factor on the temperature of operation were dark count rates that increase with temperature and excess bias. DCR at the 125K in 5.5% excess bias were recorded to be $18.3 counts/s/\mu m^2$ (which is still 3 orders of magnitude lower than previously reported $11200 counts/s/\mu m^2$ (4)). By reducing the DCR we would be able to operate our devices at higher temperatures and higher excess bias achieving even higher SPDE. Since the DCR is related to the thermal carrier generation in the semiconductor, it also increases with the device size. As stated earlier the devices that were used for these measurements were large $100\mu m$ in diameter devices. By decreasing the device size we would observe a substantial decrease in the DCR. Even still, the values achieved of DCR for a Ge-on-Si SPAD are record breaking when compared to the ones previously reported in the literature (between 2 and 4 orders of magnitude lower while accounting for device size). A Noise Equivalent Power (which is a figure of merit used for comparing different SPAD devices) for the record breaking device was a record breaking $1.9 \times 10^{-16} WHz^{-1/2}$ at 78K which is a fifty-fold improvement over previously reported Ge-on-Si SPADs at 1310nm(5). However at the temperatures where the record SPDE was achieved for 1310nm there was only a minimal SPDE for 1550nm wavelength.

To understand this small absorption at 1550nm a simulation of a 0.18% biaxial tensile strain (due to the lattice constant mismatch between Ge and Si) Ge direct band

gap absorption curve for different temperatures was performed. From it one could observe that increasing the temperature of device operation would result in a substantial increase in the Ge absorption coefficient at wavelengths close to 1550nm. This trend (presented in the simulation) was then confirmed by acquiring and normalizing SPDE vs different wavelengths for different temperatures.

The investigation of the afterpulsing using time-correlated carrier counting method was carried afterwards. We registered an afterpulsing probability of a $100\mu m$ device in 100K and compared it with the afterpulsing probability of a commercially available state of the art InGaAs/InP SPAD. Our Ge-on-Si SPADs exhibit lower afterpulsing probabilities than commercially available state of the art InGaAs/InP SPAD in nominally identical conditions. For instance, using a hold off time of $10\mu s$, the Ge-on-Si SPAD exhibits 20% of the afterpulsing probability of the InGaAs/InP SPAD detector. These initial results demonstrate a very encouraging trend implying that the Ge-on-Si SPADs could potentially be operated at a much faster rate. Further investigation would be required to more precisely asses their potential for commercial applications.

Lastly in-lab LIDAR measurements were performed with a single pixel $100\mu m$ device by scanning it across an object. Measurements were performed in 100K for an acquisition time of 10ms. LIDAR measurement was successful resulting in depth and intensity images clearly representing the scanned object. Additionally, a set of LIDAR measurements were performed with shorter acquisition times as a proof of concept on the shortest time necessary to obtain meaningful picture. The lower limit of acquisition time was observed to be 0.5ms. From these measurements it was possible to extrapolate the laser power necessary the outside of the lab applications. To achieve a 1km ranging in 1310nm a laser power of only 10^{-4}W would be required, this is below the eye safe threshold limit, suggesting that this device would perform well in real life automotive LIDAR applications. Our devices could be potentially operated at near room temperatures (with Peltier cooling) which additionally reduces the costs of packaging and makes the devices more robust and viable for commercial applications.

6.2 Future work

As discussed in the previous section, there are a number of details to be optimized in order to achieve higher values of SPDE and lower DCR. Since DCR is known to be related to the overall area of the device the initial focus was put into achieving working devices of $50\mu m$ and $26\mu m$ diameter. Additionally, a more planar structure was investigated to achieve easier to fabricate and more robust devices. These new designs were implemented into the fabrication process and initial testing was performed. This new generation of devices is referred to as generation 13. A chip from generation 13 was designed to have 3 quarters with spacers (lateral distance between charge sheet and etch) of $5\mu m$, $10\mu m$ and $15\mu m$ in order to investigate the influence of a spacer on the DCR as well as a quarter 4 with test structures for fabrication purposes. Changes in the fabrication of these devices consisted of utilizing a thin sloped trench etch around the device to electrically isolate it from its neighbors (instead of uniform material removal around it). This was done in order to increase the yield of the contacts going down on top of the smaller devices. There were two variants of this design, one with the trenches being filled with dielectric and one with uniform layers going across the trench (using the fact that the side wall slope would prevent thin layers from having discontinuities at the edge). Devices with the latter design were found to display an open circuit behaviour, most likely due to an insufficient passivation etch that prevented the bond pad from having an electrical contact with the top of the sample. As for the devices with filled trenches a novel process was developed allowing for the HSQ to reflow from the higher surfaces of the sample into the trenches creating more uniform surface was developed. This process was proven to create uniform surfaces with the trenches being filled with HSQ. However, this process still requires some adjustments and improvements for the fabrication step and are still being investigated at the time of writing this thesis. I will therefore present the results achieved so far and draw conclusions on what other improvements need to be implemented.

6.2.1 Generation 13 results

In this section I am going to present some initial results achieved on the generation 13 devices. For these devices the main design difference was a varying spacer, which is the

lateral distance between the charge sheet end and the side wall of the mesa presented in the Fig.6.1 in addition to some fabrication decisions considering the trench separation of the devices and sloped side walls of these trenches.

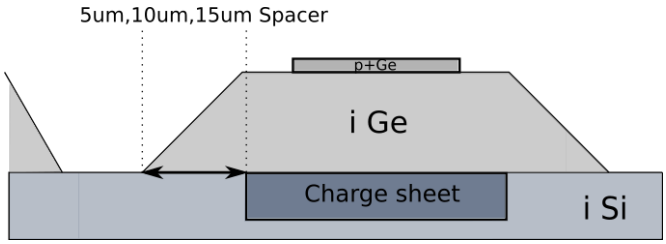

Figure 6.1: Diagram showing positioning of the spacer being varied in the Gen13 design.

Devices were produced in accordance to the fabrication techniques presented in the fabrication chapter 3. There were two sets of devices, one following all of the fabrication steps of the gen13 processing and another without the HSQ spin and reflow. This second set of devices was fabricated in order to asses if the SiN on itself provides adequate dielectric isolation. Additionally it was investigated if the layer deposition being continuous along the sloped trench would allow for skipping the HSQ deposition for increased robustness of devices and decreased time of fabrication.

Before proceeding with live devices however, a set of test devices were fabricated to assess the overall viability of differentiating spacer distances. To investigate this a set of simple devices were produced with only a trench etch and Ge p++ etch. Due to the high doping of the top layer and high doping of the substrate it was possible to perform IV measurements without the need for depositing metal. Even though the obtained results are expected to be of a lower quality than these with a deposited metal contacts an overall observed trend in the IVs would still be a good indicator of the possible performance of the devices.

In Fig.6.2 I present the collected IV's for different device sizes with varying spacer size. It can be seen, that with increased spacer size, the current passing through the device increases as well, however it is still not known how this would influence the DCR and SPDE values. In addition, differences in the overall current for different spacers

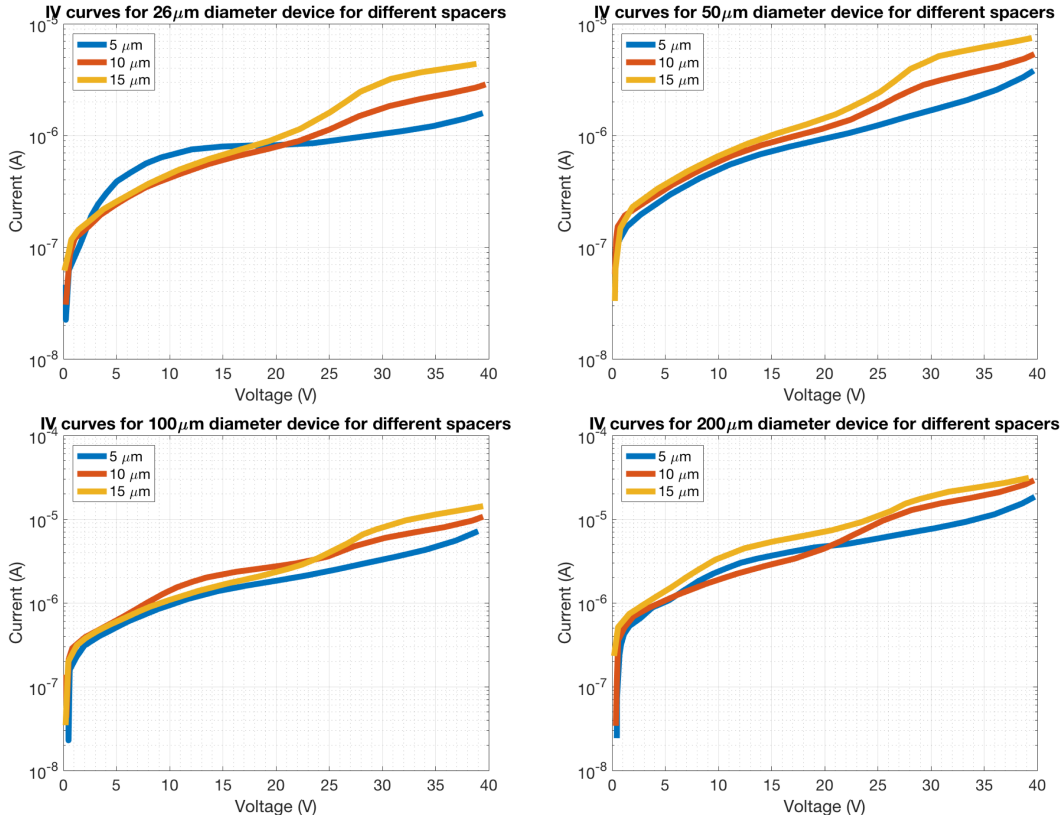

Figure 6.2: Current-Voltage characteristics for different spacer sizes and given device diameter.

are largest for the device of the smallest diameter with this difference decreasing as the device diameter gets larger. The more in-depth investigation would need to be carried out in order to asses the magnitude of the spacer size influence on the DCR. However, the fact that the current does not significantly increase with the larger spacer is really encouraging for the potential performance of this design.

With these results at hand full fabrication of chips was begun. In Fig.6.3 a SEM image shows a cross-section through the middle of a fully fabricated $26\mu m$ diameter device from such a chip. The chips were then diced into quarters and IV measurements were performed as a first quality check measure. However, the acquired characteristics were different than expected, mainly all of the devices, regardless of their size, exhibited the same extremely high IV profile. After some investigation it was observed that

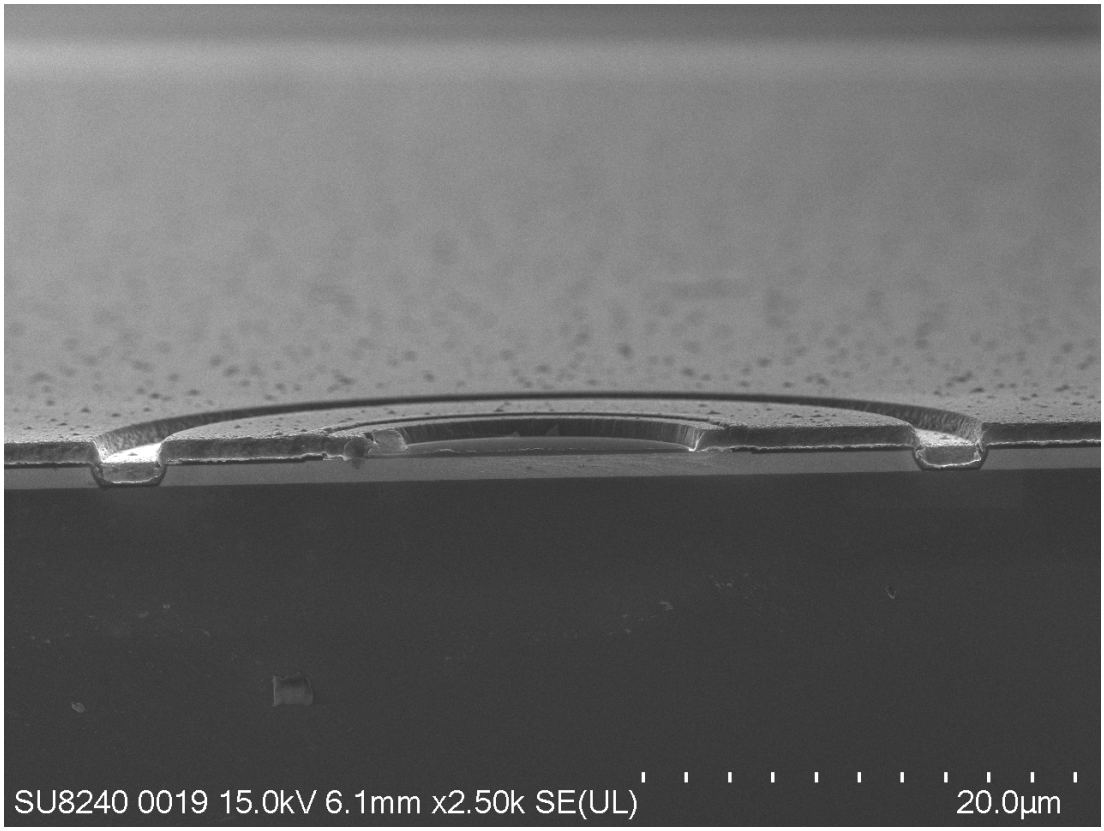

Figure 6.3: SEM picture of a cross section through fully processed Gen13 device without trench filling

this profile was similar to the IV that were taken on the test devices with a diameter of 1mm, which displayed a bulk behavior. This suggested that there was no contact on top of the device, but rather that contacting was happening either below the bond pad or inside the trench. In addition, cleaves were performed for SEM investigation of the contact region and it was observed that the silicon nitride layer in the via hole was not fully etched, therefore preventing the top of the device from being contacted. This insufficient etch was likely due to some changes in the etching apparatus slowing down the etch rates of silicone nitride. That, in addition to the potential problem with SiN breaking either under the bond pad or in the trench led to these devices begin non-operational and led us to consider fabricating more devices with a HSQ trench fill. The design presented here should be revisited in future work in attempt with trying to achieve more precise SiN deposition and etching.

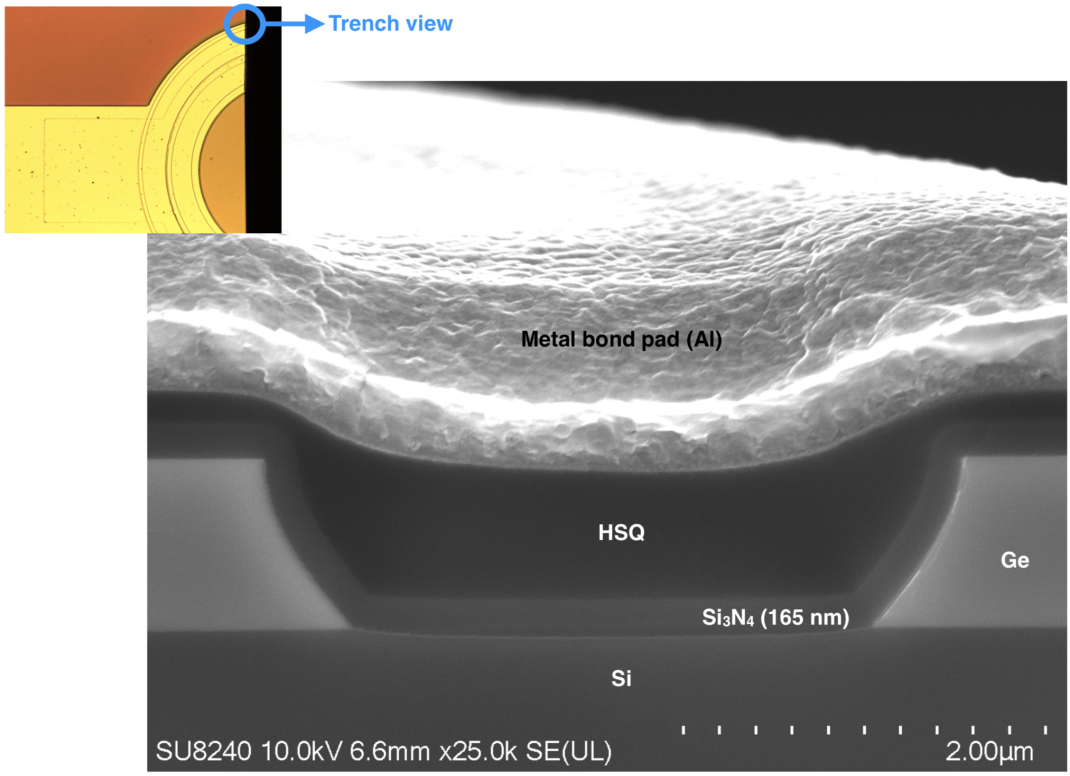

Figure 6.4: SEM picture of a cross section through fully processed Gen13 device with HSQ trench filling and reflow process

Lastly a set of generation 13 chips with a HSQ trench fill were fabricated. In Fig.6.4 an SEM picture showing the cross-section of a trench with HSQ filling and reflow, with a metal bond pad running over it is presented. Additionally a microscope view of the SEM imaged spot is provided in the inset of Fig.6.4. Chips were cleaved into quarters and initial IV characteristics were performed.

The comparison of the IV characteristics for the devices with isolation trench either with or without HSQ filling is shown in Fig.6.5. The measurements were performed for the $25\mu m$, $50\mu m$ and $100\mu m$ radius devices. As can be seen in Fig.6.5, devices with HSQ filed isolation etch show dark currents two orders of magnitude lower than the devices without HSQ filling. Additionally,for the devices of different sizes in the case of no trench filling, there is very little difference between the dark currents . In

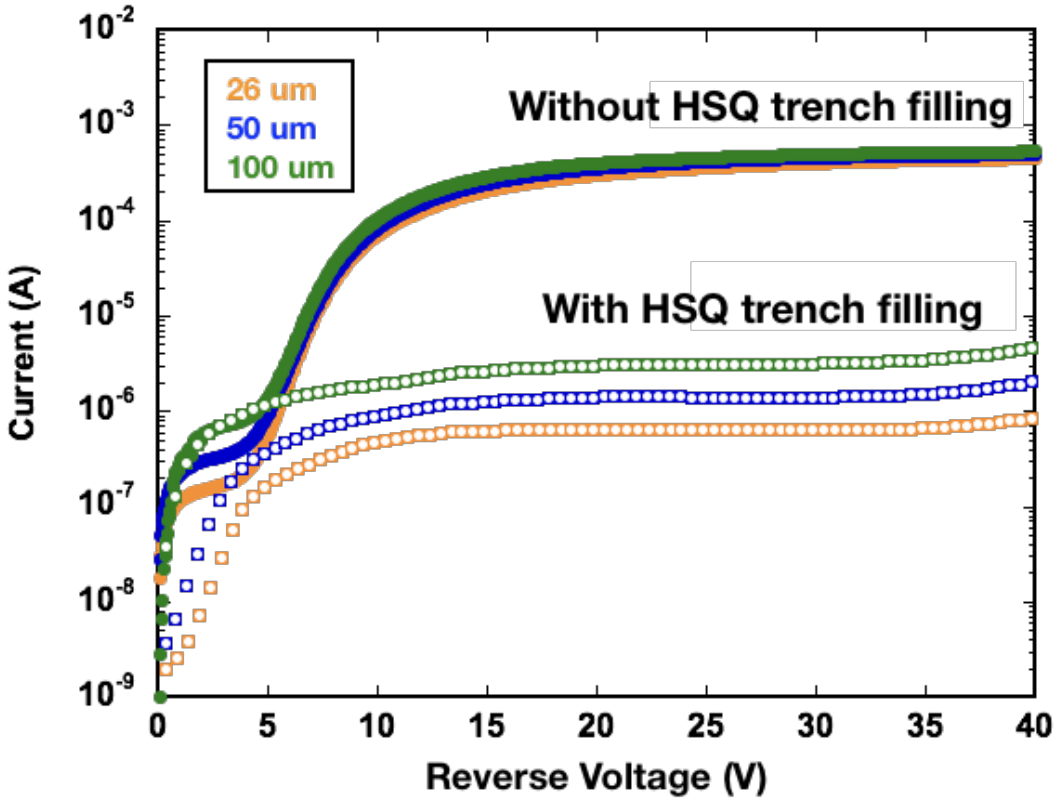

Figure 6.5: The Current-Voltage characteristics of $25\mu m$, $50\mu m$ and $100\mu m$ radius devices for the cases with and without HSQ filling of the isolation trench.

the case of the devices with the HSQ trench filling there are clear differences between IV's of different size devices in addition to the low dark current. These are promising characteristics suggesting that the devices with the HSQ filled trench would be a better candidate for a high performing Ge-on-Si SPAD. However determine the origin of the differences between those two designs additional investigation should be carried out.

To summarize, future work should be focused on devices with this design, building on the initial results presented in this section.

6.3 Further Developments

In this section I am going to discuss some of the ideas concerning design and fabrication that could be implemented in the future designs in order to improve the device's yield, SPDE, DCR and jitter.

6.3.1 Small diameter devices

In this subsection I am going to focus primarily on the benefits of, and potential changes to the design for the development of devices with diameters below $100\mu m$.

Fabrication of the devices with diameters below $100\mu m$ is an important step forward in the Ge-on-Si SPAD development that could prove important in increasing the performance of our devices. There are two types of advantages arising from such devices. Firstly, smaller devices would require less space on the chip, meaning that more of them could be placed on a $1cm^2$ chip that are currently being used for development. With larger arrays it would be possible to manufacture a detection matrix therefore increasing detection capabilities and bringing our chips closer to the requirements of mass produced SPAD LIDAR cameras. Currently (as shown in the measurement chapter 5) LIDAR measurements were only possible with a single pixel being scanned across the object which would not be very useful for the out of lab type measurements. Additionally, with large numbers of devices of the same size, it would be easier to determine how uniform their performance is. If larger discrepancies are discovered it would be easier to investigate what mechanisms would influence their performance the most. One of the mechanisms that would potentially cause large differences between devices is the creation and propagation of threading dislocations. Threading dislocations are discontinuities in the crystalline lattice which in the case of Ge being grown on top of Si is caused by the lattice mismatch between the two, and the tensile strain originating from it. These dislocations created at the interface propagate through the Ge creating "thread" that can act as trapping centers for the carriers, potentially contributing to the dark counts in the device operation mode. Their creation is a probabilistic process as well, meaning that within a certain area there is a chance that they might occur. For devices of larger diameters this means that the amount of threads per device would be approximately the same. For really small devices however, there is a better chance

that a device would be located in an area with a lesser amount of dislocations, that could potentially lead to much better performance. However, this can lead to some devices containing more threading dislocations than their neighbors, therefore hindering its performance.

With a large amount of devices test measurements could be performed to investigate the threading dislocation influence on the SPDE and DCR. If this contributes significantly to lower performances then different methods for reducing threading dislocatios could be investigated and attempted.

Dark count rates are known to be proportional to the size of the devices and it is expected that they would be reduced with smaller areas of the devices as previously reported for all Si SPADS (92). This is a second significant motivation for the fabrication of smaller devices. DCR also increases with temperature and applied excess bias, so that at higher temperatures or biases it makes single photon detection impossible. However, with smaller DCR originating from the bulk Ge in the case of devices with smaller diameters, DCR would stay lower at higher temperatures and excess biases allowing for single photon detection. The ability to operate the devices at higher temperatures and higher biases will in turn (as the trend observed in SPDE suggests so far) result in achieving higher SPDE. If the operational temperature of about 200K was reached it could be of great benefit as the devices could be operated on a triple Peltier cooling stage instead of cryostat. That would not only make measurements less demanding to perform but would also make up for much more viable devices for wide-spread consumer applications.

Additionally, a change in operating temperature would lead to a change of the Ge direct absorption band. As shown on the simulated absorption spectra of tensile strain of Ge on Si (due to the lattice mismatch) the absorption coefficient curve would shift towards longer wavelengths causing a great increase of the absorption coefficient of wavelengths around 1550nm. This is especially interesting due to the decreased background Sun noise at these wavelengths which would be problematic while considering outside of lab applications and potential QKD applications . Therefore, creating smaller devices would in turn result in the ability to reach high SPDE at 1550nm wavelength.

Several problems have been identified as potentially resulting in the smallest devices from previous generations not working during this PhD research. These problems include: layer misalignment, poor contact deposition and planarization issues. Firstly, misalignment issues should be addressed as they would have to be incorporated into fabrication first. To start with, the size of a device could be increased to incorporate larger margins of error for the photolithography steps. This however would only be applicable to the devices fabricated from the current wafers as they only have smallest charge sheets $25\mu m$ in diameter, which is too small to incorporate margin of error necessary for the photolithography processing. However, this approach would not work while considering fabrication of new wafers and potential devices of sizes $10\mu m$ and below. Alignment in this case would have to be performed by the e-beam system replacing the photolithography processes used so far. An e-beam approach was not widely utilized in present samples to solve alignment issues due to the poor quality of e-beam alignment markers. During the etch processes of these markers the Estrelas etch tool developed some issues that resulted in an isotropic etch profile which made it difficult for the e-beam system to properly register. Therefore a big part of the alignment problems for the future samples could be solved by investigating different etch processes that could allow for a much more anisotropic etch for the e-beam markers that would be easier for the e-beam systems to register.

Alignment issues could be tackled as well by utilizing the self-alignment method. As an example let's consider the etches performed on top of the active area to remove excess HSQ and create a via hole through SiN and AlO to reach the p++Ge for contact deposition. Currently each of these etches is performed with different chemistry and requires separate photolithography steps. A self-alignment method in this case would mean that there is only one photolithography step before all of the etches are carried out, this is used as a protective layer for all of the etches. This completely negates the problem of misalignment between photolithography steps between etches as they could be performed all together utilizing only one photolithography layer. This method, however, poses some different challenges that would need to be addressed and solved if it is going to be applied to real devices. Currently between the etches a sets of cleans are performed to remove the side wall passivation chemical that can be deposited during

the etch and clean off the remaining resist from the surface. In the case of a self-aligned method, no cleaning steps would be performed between etched as they could potentially damage the resist, causing following etches not to preserve a developed out shape. Necessity for the cleaning steps could however be diminished by performing all the subsequent etches without removing the sample from the etching equipment and potentially exposing it to contamination. Chemicals used for the etches would have to be carefully selected in between the etches to prevent a potential interaction with the previous passivation layer that could influence the etch profile of a subsequent layer. However, the most challenging part of this method to develop, would be selection of the photoresist and spinning method utilized. During the etch, the resist layer acts as a mask for the material underneath preventing any damage to it, this resist layer however is also being damaged by the etching chemicals during the etch, reducing its thickness which (for the longer and more aggressive etches) can lead to a full resist removal from the sample surface therefore leading to damage of regions that should be protected. This could be prevented by using thicker resist, although this can pose an issue while etching out material on smaller devices. For smaller devices, the contact area that is to be exposed would have to be relatively thin so as to leave enough room on top of the device for feeding light. With thicker resist, that could potentially survive subsequent etch steps, achieving such small features would be difficult if not impossible. This poses the main challenge in this approach. Self-aligned etches would require a completely new approach towards the resist masking, that would provide protection for the regions that should remain unaffected and at the same time provide a small resolution of features necessary for small devices. This could be achieved either by considering usage of different photoresist (that won't be heavily affected by the etch chemistry and therefore allow for thinner layers) or a change to the etch chemistry (reducing the rate at which it is removing the photoresist while maintaining etching speeds in the materials to be removed). These two approaches would require a significant amount of tests to achieve a satisfactory middle ground but could prove extremely beneficial for the overall alignment of the device.

This process if developed correctly could prove beneficial for more precise metal contact deposition. In the contact deposition process the sample is covered in photoresist, with areas where, according to the design, metal should remain being developed

out, metal is then uniformly evaporated on the sample surface. After that the sample is put in an acetone bath in which the resist with metal on top is being removed (liftoff process) leaving only the areas that were previously developed out covered in metal. In the via hole opening process the areas that are being etched out are largely the same as the areas that would have been developed out in the liftoff process. This means that if after the etch remaining resist layer is thick enough it could be used as a mask for the metal contact deposition process. This would not only lead to the contacts being perfectly aligned with the areas where the etch was performed but could also lead to a significant decrease in the time necessary for the processing. Hence, even though it would be challenging to develop a suitable process like this, it would be worthwhile time spent developing it.

Another issue related to metal contacts and especially bond pads deposition, which is present while utilizing a many layer approach for the via hole etch, is the metal continuity at the top of device. Utilizing many photolithography steps can lead to misalignment, this can then cause (in a spot where misaligned layers would at one spot end up on top of each other) an appearance of a larger step between the top of the device and the bottom of the via hole. This large step, after covering it with metal, was observed to cause open circuit behavior. As the devices are thermally cycled strain, due to different thermal expansion coefficients, is introduced to the metal layer. With the large step to be covered the metal layer is thinner at the side wall of the step, making it more prone to breaking when additional strain is applied. This behavior was observed in some cases of the small devices as they seemed to work initially but were displaying open circuit behavior after a few IV cycles. Another solution (in addition to the alignment improving methods mentioned earlier) would be the introduction of thicker metal. With the thickness of the metal layer larger than the step it has to cover, it would likely be much more robust and less prone to breaking. This thicker metal deposition could be easily implemented although some investigation of its properties would still be needed as thick metal layer might be prone to cracking if deposited by e-beam methods.

6.3.2 Further improvements

One of the layers that influence the step height, mentioned in the previous section, is the HSQ planarization layer. The misalignment of the photolithography layer used for the etch, can lead to creation of a step of about $300\mu m$ (which was partially solved by the reflow process). Etching of this layer can also be challenging as the chemistry used for this would attack the underlying SiN antireflection coating as well. Even with the usage of a reflectometer during the etch, the transition between these two chemicals can be challenging to distinguish, further adding to the potential of damaging the SiN. One of the ways that could be used to address the uncertainty of the etch would involve developing out the HSQ instead of etching. The HSQ in addition to being a spin on glass material that can be readily used for planarization it is a negative tone resist. It can be patterned with an e-beam exposure. Exposed areas then become insoluble in the developer that does not interact with the SiN layer underneath. If incorporated, this process would provide an easy and consistent method for removing HSQ from the active area without risking damage to the underlying layer. A big issue for this method (if the samples were developed from the current batch of wafers) is the ambiguity of e-beam alignment markers as this via hole step would require a high level of alignment. This method however might leave a small HSQ step behind that could add to the aforementioned metal contact breakage. Another method to remove excess HSQ from the surface while leveling the surface is polishing. After the HSQ spin and reflow, HSQ still remains as a thicker layer on the highest points of the device which in this case are the tops of the active areas. Polishing is a process in which a planar rough surface coplanar to the sample is brought into contact with it and it mechanically remove the material that is at higher elevations than the rest of the surface. This would allow one to polish the tops of the active areas down to the level of SiN creating a perfectly smooth surface that would prevent any potential in between layer steps from appearing and prevent the problem of metal discontinuity. However, even though potentially allowing for high improvements to the sample robustness its application would be challenging. To begin with the surface quality after the polishing should be considered. Since this involves a mechanical removal of the material, it can lead to highly increased surface roughness. Although this would not matter for the planar areas around the active area it can prove to be a significant problem for the antireflection coating which would be

a stopping layer of the polishing, since the high roughness of the surface would lead to increased reflectivity therefore diminishing the coating's ability to perform its major function. Another big challenge in developing this process would be related to timing of the process. Since only the removal of the HSQ is required, one would have to stop precisely at the interface with SiN or slightly before that and timing of when to abort the polishing could prove extremely difficult since the layer thicknesses are in ranges of $300nm$. However, If this process was developed it could prove extremely useful for the purposes of fabricating planar, robust devices.

If the development of planarization via polishing was successful, this could lead the way towards replacing the spin on HSQ as a chemical used for planarization with deposited SiN. Currently, samples require a process in which an isolation trench is filled and has an insulation layer under the contacts to prevent from current flow in the regions outside of the active area. HSQ, even though it has proven itself to be useful and provides a good planarization after the reflow process, won't even provide uniformity of the deposited layers. In order to improve the surface uniformity an approach utilizing SiN deposition could be attempted. Using plasma enhanced chemical vapor deposition layers of SiN exceeding a thickness of $2\mu m$ could be grown on top of the sample surface. This process would not create a planar surface, but rather transfer surface profile $2\mu m$ higher. However, with a developed polishing process, this uneven surface profile could be polished down to a level at which only $165nm$ of SiN is left on top of the active area of the devices to serve as an antireflection coating. This would create a perfectly even surface that would be difficult to achieve in any other way. Selecting the thickness of the grown SiN to be above $2\mu m$ would guarantee that the lowest point of the translated up surface (which would be at the bottom of the isolation trench $1.3\mu m$ below the top of the active area) would be higher than the top of the active area after the polishing. This would ensure that a perfectly flat surface across the whole chip would be achieved after polishing.

If this process proves to be successful another improvement to the device fabrication that could reduce the fabrication time required and overall processing complexity could be attempted. Since its heavily water soluble, grown GeO_2 has to be protected from the ambient atmosphere. A capping layer of Al_2O_3 , isolating it from the ambient

atmosphere is currently utilized, it is also used as an additional measure to electrically isolate the Ge surface from the deposited contacts. However, Al_2O_3 has proven to cause some issues during both deposition, as it is difficult to achieve the same deposited thickness every time, and removal for example when performing the via hole etch to contact the p++ Ge. Instead, an approach with SiN serving as such a layer could be attempted. Deposited layers of SiN are known to have pinholes in them, that for the thinner layers could lead to the metal contact layer spiking through them and forming an electrical contact with the Ge underneath. However, growing a thick layer of SiN should prevent this. The main problem with such a layer in previous designs was that it creates non-uniformities at the sample surface. However, with the developed polish off planarization process this should not be an issue. Therefore development of a polish off process for the SiN could make it possible to replace the Al_2O_3 cap with much easier and faster SiN capping and planarization process.

Another improvement that could be developed in future generations of devices would be the implementation of the Radio Frequency (RF) techniques for current delivery. Currently contacts and connections used as a mean of current delivery are not optimized, which results in increased values of jitter. Although smaller than in the case of InGaAs/InP type SPADs, the afterpulsing of our devices could be reduced even further allowing for much faster operation rates. All of these benefits could be achieved by developing RF optimized contacts that could largely suppress the electronic interference by influencing the way that the device is gated. Firstly, it is important to note that the afterpulsing effects are related to charges that are being trapped during the avalanche process and then if released during the subsequent gating event they could cause a false count. This could be tackled either by extending the time between gates (as the trap states will depopulate probabilistically with time) or reduce the overall amount of carriers that are being created during the avalanche process. There are two main ways that one could reduce a number of carriers created in the avalanche, one method is the reduction of excess bias and another is reduction of the time that the gate is applied. Since it was observed that for higher excess biases the devices in this thesis were reaching higher SPDE it would be more beneficial to try to implement shorter gate times. Shortening of the pulse could be achieved by utilizing a radio-frequency generator as a source of the gate. This pulse would be constructed of multiple synchronized harmonics

that would allow for shortening of the gate time. To achieve this a careful investigation of the electrical interference in the system would have to be carried out in order to be able to devise a secondary, opposite signal which (while superimposed on the first one) would allow for the initial one to be canceled out leaving only the avalanche signal to be detected. This would also allow to operation of the devices at higher bias voltages with decreased noise allowing them to achieve higher values of SPDE. Additional investigation should be carried out on the amplitudes and phases of the interference signals in order to make this mode of operation possible. This would also be related to the geometry that is being used to contact the devices. Additionally with development of low noise RF contacts a fabrication of large arrays of devices, akin to the Si detector arrays could be attempted.

One change to the fabrication process that is known to have to been applied in order to make the design RF ready is a correct positioning of the bottom contact. Currently the bottom contact is a deposited metal layer on the back of the chip (which is a heavily doped n+ Si allowing for direct ohmic contact deposition). in the current generation of devices all the devices on the chip have a common back contact. This works for current first investigation purposes as the devices are only ever addressed one at a time. If the devices were to be operated in the RF mode, the bottom contact should be developed to address only one device and preferably be on the same level as the top contact. This could be achieved by performing a deep etch, that would reach down past the i-Si and into the n+ Si in the half moon type of structure (ground-signal-ground), that could then be filled with metal and act as a direct bottom contact. Such a processing step, although challenging could be achieved based on experience with trying to develop a sloped etch for the Ge isolation trench. With it the contacts could be run continuously without breaking on the sloped surface and without having to deposit metal layers $3\mu m$ thick. However some additional development would be required so as to make sure that the sloped etch would also perform well in the Si.

Another thing to consider, especially while growing the next batch of wafers is the thickness of the Ge absorber used. In the current design, the Ge absorber layer is of $1\mu m$ thick to ensure easier processing and trench filling. However, this is not the optimal thickness as $1\mu m$ of Ge would only absorb about 50% of the incoming radiation

between 1310nm and 1550nm. The thickness of Ge was kept at this level in order to make the processing and etches easier to perform. With some additional improvements to the processes of trench isolation etch and planarization, Ge absorber thickness could be increased in the subsequent wafers therefore increasing the amount of light that gets absorbed, which in turn would increase the overall SPDE of our devices.

As mentioned in the methods chapter 2 a technique for selectively growing Ge inside the SiO_2 wells is now under development for future wafers. Currently the development was performed up to a stage at which the SiO_2 wells can be manufactured and testing of growing the required amounts of Ge inside of them will commence in the near future.

Another design change that could make testing of the devices easier and more in line with commercial requirements would be the development of new ways for the samples to be connected to the header package, and header package to the cryostat. Currently the header package used has to be soldered to the contacts in the cryostat to create the electric connection. However, with modifications to the header package and cryostat the connection could be established by utilizing a plug in header package and cryostat connection. Removing the soldering step in favor of using the plug in component could reduce the troubleshooting required for achieving a high quality connection. Similarly current generation of devices requires bonding to the header package in order to establish the connection with top contact. If the bond pads were developed to be more uniform (giving up some of the flexibility of the test devices) a bonding step could be largely automated significantly reducing the time required and variation from the manual bonding (arising from the differences between the quality of the bonds).

In addition to the design and fabrication changes new properties of Ge on Si SPADs could be investigated. An in depth study presenting the relation between DCR and dark current in the Ge on Si SPAD (which was not presented in the literature so far) could be performed. This could be done by investigating dark currents and DCR for a larger range of device sizes. If the range of the temperatures at which one can obtain meaningful SPDE was expanded, an investigation of the Ge absorption coefficient for different wavelength vs temperature could be performed to better support the theoretical calculations presented in the main body of this thesis. Study, that would be

especially interesting from the commercial application perspective, could be carried out on the outside of lab LIDAR measurements in various atmospheric conditions and various acquisition times.

Lastly let's discuss potential changes to the design and fabrication of the generation 13 devices, based on the data achieved from them so far. Just like the chips from generation 12, chips from generation 13 have on them three separate designs. The main goal of these is to determine which is the best performing design to be incorporated in the next batches. In this case, the design differences that were being investigated are related to the spacer size, where the spacer is a lateral distance between isolation trench etch and the charge sheet. After extracting the SPDE values for all currently incorporated designs, the next samples could be produced that only have the spacer sizes that provided best results in DCR and SPDE. With the most optimal spacer size determined another design choice could be investigated. The most interesting one to be determined next would be the lateral distance between the edge of p++ Ge etch and the charge sheet. It was determined previously in this thesis that the best performing devices are the ones with the p++ Ge etch being laterally confined within the charge sheet but the exact distance required for the best performance is unknown. Next samples could have a range of p++ Ge etches that are all enclosed within the lateral extremities of the charge sheet with the value of their separation changed by $5\mu m$ for different designs to hopefully determine either the best separation distance or if even larger separation would yield better results.

Applying all the changes presented in this section would require a lot of time consuming development and fabrication. However, I am confident that the current azimuth of investigation would produce devices of higher yields and even higher performances than the devices that were fabricated so far during this PhD, making them the most promising technology for applications in the automotive/autonomous LIDAR sector.

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