Enhancement of hydrogen terminated diamond FET performance through integration of electron acceptor oxides

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Abstract

This work reports on the improvement to the performance of hydrogen terminated diamond field effect transistors (FETs) by replacing surface adsorbed atmospheric species with transition metal oxides MoO_3 and V_2O_5, and the implementation of a pre-deposition vacuum anneal at 400°C which is required to maintain the stability of the doping within the devices.

MESFET structures incorporating a metal/H-diamond gate contact were observed to be irreversibly damaged by exposure to the 400°C pre deposition vacuum annealing prior to deposition of MoO_3 or V_2O_5. Therefore preliminary investigation of devices including the MoO_3 or V_2O_5 without pre annealing was carried out. An increase in maximum drain current of up to 50% was observed when comparing output characteristics before and after deposition of MoO_3 or V_2O_5 without the 400°C pre anneal.

Following this, investigation of the inclusion of Al_2O_3 into the FET structure as a gate dielectric was explored in order to increase the thermal robustness of the gate and allow inclusion of the pre deposition vacuum annealing at 400°C. It was shown that FETs fabricated using Al_2O_3 as a gate dielectric maintained transistor operation after vacuum annealing at 400°C and deposition of 10nm of MoO_3 or V_2O_5. FETs were characterized after exposure to atmospheric adsorbates, and after deposition of 10nm of MoO_3 or V_2O_5 and pre deposition 400°C vacuum anneal. FETs with Al_2O_3 gate dielectric using V_2O_5 and pre deposition annealing showed an increase in drain current of up to 276%. The V_2O_5 FETs using Al_2O_3 as a gate dielectric showed maximum drain currents of -376mA/mm, extrinsic transconductances of 97mS/mm, and on resistances as low as 17Ω.mm. These are important parameters for assessing the performance of power FETs.

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Associated Publications

Journal Entries

D. A. Macdonald, K. G. Crawford, A. Tallaire, R. Issaoui, and D. A. J. Moran, "Performance enhancement of Al_2O_3/H-diamond MOSFETs utilizing vacuum annealing and V_2O_5 as a surface electron acceptor," *IEEE Electron Device Letters,* pp. 1-1, 2018.

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Conferences

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Contents

1. Introduction

The field effect transistor (FET) is one of the most important technological advances of the last century. The FET forms an electronic switch which can be turned on or off using just a small electronic voltage. Perhaps the best known implementation of FETs, and where they have had the greatest impact, is in logic circuits; every day we use microprocessors formed by cascading logic circuits in our phones and computers etc. Logic circuits operate at low voltages using small currents. However, there is also a need for switching higher powers at high frequencies as efficiently as possible for applications such as radar and satellite communications, FETs are suitable for this task too.

High power FETs, as their name would suggest, are used as high-power switches. Ideally when “on” they allow large currents to flow through the circuit with minimal electrical resistance; when “off” they block all current flow through a circuit and drop all voltage across the FET. In order to be as efficient as possible, high power FETs must consume as little power as possible. This means minimizing conduction loses when “on” and minimizing leakage current when “off”. Banks of silicon based devices have previously been used for high power applications. However this is non-ideal as many devices must be used to allow high currents and block high voltages. This is both expensive and inefficient due to the poor thermal performance of silicon and the need for a large amount of die space. Thus there has been much interest in alternative materials which could surpass silicon in regards to current transport, high voltage breakdown and thermal management. The main competitors in this respect are the wide bandgap materials, GaN, SiC and diamond, as they have many desirable properties for high power operation.

	Si	*CVD Diamond*	*GaN*	*4H-SiC*
Bandgap (eV)	*1.1*	*5.47*	*3.44*	*3.2*
Breakdown Field ($MVcm^{-1}$)	*0.3*	*10*	*5*	*3*
Electron Saturation Velocity ($x10^7 cms^{-1}$)	*0.86*	*2*	*2.5*	*3*
Hole Saturation Velocity ($x10^7 cms^{-1}$)	*1*	*0.8*	*n/a*	*n/a*
Electron Mobility ($cm^2V^{-1}s^{-1}$)	*1450*	*4500*	*440*	*900*
Hole Mobility ($cm^2V^{-1}s^{-1}$)	*480*	*3800*	*200*	*120*
Thermal Conductivity ($Wcm^{-1}K^{-1}$)	*1.5*	*24*	*1.3*	*5*
Johnson's FOM	*1*	*8200*	*280*	*410*
Baliga's FOM	*1*	*17200*	*910*	*290*

Table 1.1 - Intrinsic properties of Diamond and its main competitors for high power performance GaN and SiC compared with Si, figures from [1.1].

Due to its large bandgap diamond has a very high theoretical breakdown voltage of >10$MVcm^{-1}$ [1.2]. High breakdown voltage means that diamond is suited for high power operations as it can be operated under strong electric fields before ionisation, avalanche or another breakdown mechanism occurs. Intrinsic diamond has very high intrinsic electron and hole mobility (4500$cm^2V^{-1}s^{-1}$ and 3800 $cm^2V^{-1}s^{-1}$ respectively) [1.3] which contributes to current transfer in low fields. Diamond also has high electron and hole saturation velocities at $2x10^7cms^{-1}$ and $0.8x10^7cms^{-1}$ [1.4] respectively contributing to high current transfer in high field and high frequency performance. The saturation velocity can also be reached well before breakdown occurs. Diamond also has very high thermal conductivity at 24$Wcm^{-1}K^{-1}$ [1.5] allowing for effective heat dissipation from high power operation and therefore low thermal losses. Diamond is radiation resistant due to its very large band gap of 5.5eV resulting in very high ionisation energy needed to excite electrons from the valence band into the conduction band. Its bandgap also contributes to its ability to operate at higher temperatures without excess thermal excitation of electrons into the conduction band.

Mechanical toughness is perhaps diamond's most well-known attribute. Its toughness is due to the short bond length of 1.54Å of carbon to carbon bonds and the diamond lattice.

As can be seen from the figures discussed and shown in *table 1.1* diamond excels in every metric for high power performance, theoretically outperforming both GaN and SiC as assessed by properties important for high power operation. High power and high frequency performance potential can be roughly represented by Johnson's Figure of Merit (JFOM). This is determined by the breakdown field and the saturation velocity of the material. Baliga's Figure of Merit (BFOM) describes the power loss at low frequency of a material. It presumes that all loss is due to the on resistance of a power FET and is determined by the dielectric constant, mobility and bandgap of a material [1.6].

Despite diamond's superior intrinsic properties, at present high quality diamond substrates are smaller area and more expensive to produce compared to GaN and SiC, which are more mature and have been demonstrated more extensively. GaN and SiC have seen successful high-power FETs make it to market. Diamond may therefore never be a direct replacement for GaN and SiC unless substantial progress in upscaling wafers is established. However diamond's intrinsic properties such as high thermal conductivity and radiation resistance may allow it to operate in extreme environments where GaN and SiC would see degradation of performance, and hence may form a more "niche" technology for military, space, aerospace, and oil and gas applications.

Although diamond grown using Chemical Vapor Deposition (CVD) has many properties which makes it an excellent candidate for the development of future high power electronic devices, natural diamond found in the earth's crust tends to have too many impurities and crystal defects to make it a good candidate for use in semiconductor devices as well as being prohibitively expensive.

Diamond, however is intrinsically an insulator. It is very challenging to substitutional dope due to the close spacing of the carbon atoms in the lattice resulting in few impurities being able to fit without distorting the lattice. It is further complicated by the high activation energies of potential dopants [1.7]. Substitutional doping of boron has been used to create conductive diamond with some success, although the high activation energy means that large concentrations of impurities must be incorporated resulting in low mobilities [1.8]. A technique known as "delta doping" has also been explored using boron in an effort to provide charge transfer layers with higher mobility [1.9]. A newer and more novel technique known as "surface transfer doping" has also been explored in diamond. Surface transfer doping relies on hydrogen termination of the diamond surface which results in a negative electron

affinity at the surface of the diamond. This allows electrons to leave the surface if a suitable "acceptor" material is in contact, the holes "left behind" form a 2 dimensional hole gas (2DHG) below the surface of the diamond [1.10]. So far surface transfer doping has been the most effective method for producing high power FETs on diamond; Achieving maximum breakdown voltages above 1500V [1.11] and -1.3A/mm maximum output current [1.12]. Therefore, the surface transfer doping technique and its application forms the focus of this thesis work.

The main body of this thesis focuses on overcoming the challenges of integrating the alternative surface electron acceptor materials on diamond such as molybdenum trioxide (MoO_3) and vanadium pentoxide (V_2O_5) into the fabrication of hydrogen terminated diamond FETs with a view towards stable and high power device operation. The integration of MoO_3 and V_2O_5 into H-diamond FETs is envisioned to improve important parameters for high power performance such as; maximum drain current, peak transconductance, and on-resistance. Aluminium oxide (Al_2O_3) has been included in the gate stack in an effort to create a more thermally robust structure and to improve off-state breakdown characteristics.

The following chapter addresses the background of the diamond material system, surface transfer doping of hydrogen terminated diamond and the underlying semiconductor physics of device operation. Chapter 3 explores relevant literature on surface transfer doping of hydrogen terminated diamond and diamond FETs, detailing the development of the technology as well as the potential which has been shown for the technology thus far. Chapter 4 details the equipment and fabrication techniques used throughout the project in order to produce hydrogen terminated diamond FETs. Chapter 5 addresses the electrical characterization techniques used to assess material and FET performance. Chapters 6 details the initial efforts to include MoO_3 and V_2O_5 into the H-diamond MESFET architecture. This chapter revealed that pre-annealing the diamond surface prior to the deposition of MoO_3 or V_2O_5 resulted in degraded transistor performance. Chapter 7 details the inclusion of Al_2O_3 as a gate dielectric into hydrogen terminated diamond FETs in order to produce a more thermally robust gate structure. The performance of the fabricated MOSFETs using atmospheric adsorbates to induce surface transfer doping and after pre deposition annealing and deposition of MoO_3 or V_2O_5 is compared. Chapter 8 closes the thesis by discussing and summarizing what has been achieved through this research and details potential further work.

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2. Background: Diamond as an electronic material

Diamond has many properties which make it an interesting candidate for electronic applications. This work will focus more specifically on the properties which make it an interesting candidate for high-power, robust electronic applications.

This chapter focuses on the physics behind diamond as a potential electronic material. It begins with the structure of the carbon atom and diamond crystal, and how these give rise to diamond's attractive properties for electronic applications. A brief introduction to the growth of synthetic diamond is included. Succeeding this is a discussion of the physics and challenges of doping diamond to achieve an extrinsic semiconductor with a special focus on the method of surface transfer doping, which is the doping method employed in this work. Following this is discussion of carrier transport in a semiconductor and the key parameters for assessing the performance of high power FETs. Finally the chapter covers metal-semiconductor and metal-oxide-semiconductor interfaces which will be used to produce the FETs in this work.

2.1. Diamond Structure

What we call "Diamond" is an allotrope of carbon, other allotropes being graphite and graphene. Which of these forms carbon takes is determined by how the individual carbon atoms are bonded to their neighbors. The carbon atom has electrons in a $(1s)^2(2s)^2(2p)^2$ orbital configuration and can have up to 4 covalent bonds [2.1].

Sp^2 bonding of carbon atoms gives rise to graphene formation, where each carbon atom is bound to its 3 nearest neighbors. Graphene is conductive as it has one remaining electron which does not take part in bonding to other carbon atoms. Graphene is a 2 dimensional material and when many "sheets" of graphene are attracted to one another by a weak Van der Walls force it forms graphite [2.2]. Sp^3 bonded carbon forms a diamond lattice configuration. As can be seen from *figure 2.1.1,* the configuration can be viewed as each carbon atom forming tetrahedral covalent bonds to each of its 4 nearest neighbors[2.3].

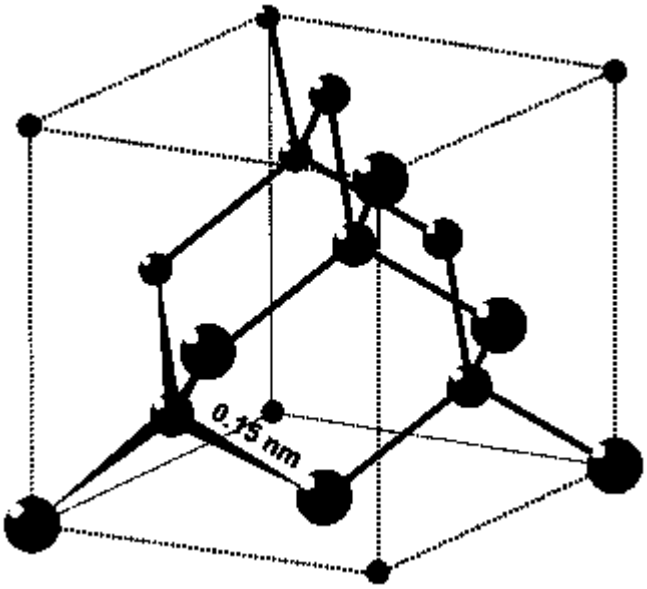

Figure 2.1.1 Diamond lattice showing the unit cell of diamond formed by sp3 bonded carbon from [2.4].

Diamond's crystal structure is what gives rise to many of the properties for which it is well known. The atoms in the diamond lattice are close together as carbon has few "shells" available for covalent bonding, meaning electrons are pulled closer to the nuclei of the atom. The extreme physical robustness arises from the strength of these covalent bonds [2.4].

Diamond has very low phonon scattering due to the stiffness of the lattice, and a short bond length, which along with the periodicity of the diamond lattice contribute to fast transfer of phonons through the material. This results in diamond having the highest thermal conductivity of any 3 dimensional material of up to $24 Wcm^{-1}K^{-1}$ [2.5], which allows for effective heat dissipation during device operation.

A large amount of energy is required to move an electron from the valence band of diamond into the conduction band due to the large energy difference between carbon atoms bonding and anti-bonding orbitals [2.3]. This gives rise to diamond's large band gap of 5.47eV, which makes diamond a wide band gap semiconductor. Diamond's wide band gap is important for power electronic applications as it leads to a very high theoretical breakdown voltage of $10 MVcm^{-1}$ before avalanche breakdown [2.6].

In high electric fields carriers rapidly lose energy to the crystal lattice by emission of optical phonons as well as other scattering events, which limits the maximum velocity carriers can achieve in a material. Therefore, the optical phonon energy in a material can play a large role in determining the saturation velocity of charge carriers; and diamond possesses the largest optical phonon energy of any semiconductor [2.7]. Due to this, diamond has high velocity saturation for mobile charge which can be reached well before the electric field

breakdown, this is important for achieving high currents when operating at high electric field.

As will be discussed later in this chapter, the mobility of a semiconductor is determined by the effective mass and mean time between collisions of carriers[2.8]. As intrinsic diamond offers few scattering mechanisms to charge carriers (as will also be discussed in more detail later in this chapter) intrinsic diamond achieves a high mobility for both electrons and holes [2.9]. Mobility is an important metric as it determines how quickly carriers reach their saturation velocity.

The key figures discussed above are outlined below in *table 2.1.1* compared with values for Si and GaN.

Property	*Si*	*GaN*	*CVD Diamond*
Bandgap (eV)	*1.1*	*3.44*	*5.47*
Breakdown field $MVcm^{-1}$	*0.3*	*5*	*10*
Electron saturation Velocity $x10^7$ cms^{-1}	*0.86*	*2.5*	*2*
Hole Saturation velocity $x10^7$ cms^{-1}	*1*	*n/a*	*0.8*
Electron mobility $cm^2V^{-1}s^{-1}$	*1450*	*440*	*4500*
Hole mobility $cm^2V^{-1}s^{-1}$	*480*	*200*	*3800*
Thermal Conductivity $Wcm^{-1}K^{-1}$	*1.5*	*1.3*	*24*

Table 2.1.1. – Comparison between semiconductor properties for diamond and other semiconductor materials Si, and GaN, figures from [2.6].

There are a number of figures of merit which can be used to assess how material qualities can translate into real electronic device performance. For this work Johnson's figure of merit, Keye's figure of Merit and Baliga's figure of merit are of importance.

Johnson's figure of merit is defined as follows:

$$JFOM = \frac{E_c * v_s}{2\pi} \qquad \textit{equation 2.1.1}$$

where E_c is the critical electric field for breakdown and v_s is the saturated drift velocity. This figure defines the power-frequency product [2.10].

Keye's figure of merit is defined as follows:

$$KFOM = \lambda \left[2.\frac{c * v_s}{4\pi\varepsilon}\right]^{1/2} \qquad \textit{equation 2.1.2}$$

where λ is the thermal conductivity, c is the speed of light, ε is the dielectric constant and v_s is the saturated drift velocity. KFOM provides a thermal limitation to the switching behavior of a transistor [2.11].

Baligas figure of merit is defined as follows:

$$BFOM = \varepsilon * \mu * E_g^3 \qquad \textit{equation 2.1.3}$$

Where ε is the dielectric constant, μ is is the mobility and E_g is the band gap. BFOM defines switching losses in power FETs assuming that the power losses are solely due to the power loss in the on-state current flow through the on resistance of an FET [2.12].

	Si	*GaN*	*CVD Diamond*
JFOM	*1*	*280*	*8200*
KFOM	*1*	*1.8*	*32*
BFOM	*1*	*910*	*17200*

Table 2.1.2 – Outlines Figures of merit values discussed in this body of work for Silicon, GaN and CVD diamond[2.6].

As can be seen from the above *table 2.1.2* Diamond's properties give rise to high values for the outlined figures of merit. This means that diamond is a very attractive candidate for high-power, high-frequency devices. Although these figures of merit provide a comparison between

2.2 Synthetic Diamond growth

Although diamond possesses many qualities which make it an interesting electronic material, these properties are not found consistently in natural diamond due to the inclusion of impurities or non-diamond carbon in the lattice. However, diamonds which possesses all these qualities can be produced synthetically.

The first diamonds grown synthetically were reported by General Electric in 1955 using the process of High Pressure High Temperature (HPHT). Essentially graphite was placed under immense pressures at high temperatures in an attempt to mimic the thermodynamic conditions of the earth's natural creation of diamonds [2.13]. Following this, groups also explored "detonation diamond" whereby immense temperatures and pressures are applied to graphite by close proximity to an explosive device[2.14]. Both of these techniques showed successful diamond growth, however each has its draw backs. HPHT diamond requires a large amount of energy, which increases exponentially with increased area. Detonation

diamond can only yield miniscule “seeds” of diamond, of little use for electronic device applications.

Chemical Vapour Deposition (CVD) growth is the main method used for the production of high quality, electronic grade diamond material today. CVD growth produces diamonds by heating a hydrocarbon gas in a low pressure (vacuum) environment. Typically the growth will nucleate on diamond already in the chamber, such as “seed” material grown using another method (HPHT or detonation). In the chamber some of the hydrocarbon gas is converted into atomic hydrogen and carbon usually by microwave plasma or by passing the gas over a hot filament. It is energetically favorable for the free carbon to form diamond in this environment. Graphite and non-diamond carbon react with the atomic hydrogen and evaporate into a newly formed gas phase[2.15].

During CVD diamond synthesis, where the growth ends the carbon is typically terminated with hydrogen atoms[2.16]. Hydrogen termination is typically stable at room temperature in normal atmopsheric conditions, however the hydrogen termination can be removed by strong acids or by exposing the surface to high temperatures (above 230°C) in normal atmosphere. In these cases the hydrogen is usually replaced with oxygen from the atmosphere leading to an oxygen terminated surface. If the hydrogen or oxygen terminated diamond surface is annealed at around 1000°C in Ultra High vacuum (UHV) the surface carbon atoms “reconstruct” leading to a clean surface[2.17].

2.3 Doping of Diamond

In order to increase the mobile charge carrier density in semiconducting material, doping is employed. By this method additional carriers are introduced into the lattice of a material typically by introduction of impurity atoms which either offer an additional electron to the lattice (n-type doping) or accept an electron from the lattice introducing an additional mobile vacancy (hole) (p-type doping). These impurity atoms will usually take the place of an intrinsic atom (substitutional doping)[2.18].

The main methods of introducing additional impurity dopant atoms into a semiconducting material is by diffusion, ion implantation and during growth[2.19]. During diffusion implantation atoms are placed on or near the surface of a semiconductor at elevated temperatures. These atoms migrate through the semiconducting material. The doping concentration is concentrated at the surface as the dopant must diffuse through the material from the surface. During ion implantation dopant atoms are accelerated to high velocities incident on the surface, becoming embedded in the lattice of the material. During growth

impurity atoms can be included in the gas or liquid phase of semiconductor material production and become included in the lattice.

For diamond there are few elements which can be used for this purpose, and they face a number of problems. If a large atom is implanted into the material it could disrupt the lattice, due to this only a few smaller atoms such as boron, nitrogen and phosphorus are options for incorporating into diamond. The tight spacing of the diamond lattice can make diffusion of impurities through the lattice very difficult [2.20], therefore diffusion implantation is not particularly desirable. Ion implantation can cause large amounts of damage to the lattice due to the high velocity ions colliding with atoms in the lattice. In order to reduce this damage in most semiconducting materials the material is annealed after implantation which reconstructs some of the damaged bonds in the material. However, in diamond high temperature annealing required to reform the bonds can also cause graphitization of the diamond (at around 1500K) [2.21]. Therefore the most common, and successful way of including impurities in diamond is to introduce them during the growth process.

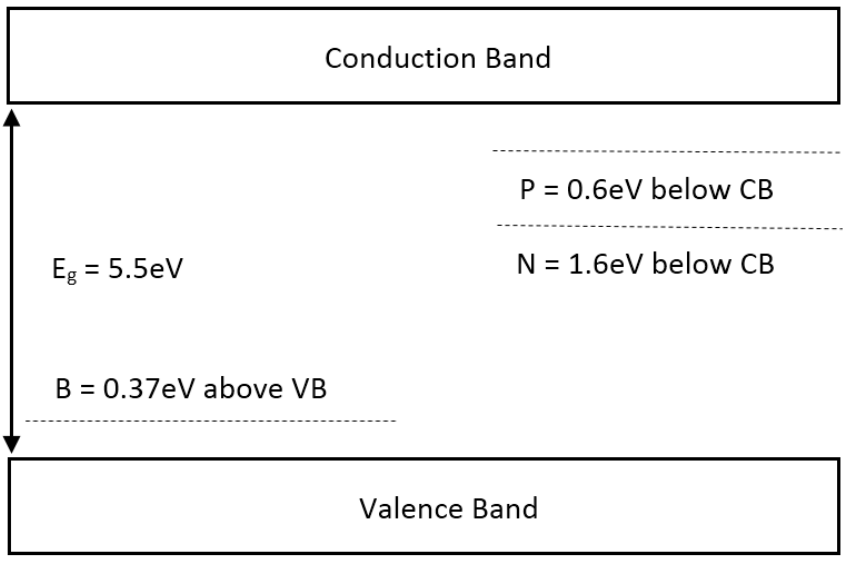

Figure 2.3.1 - Energy levels of impurity atoms suitable for implantation in diamond.

The few elements suitable for doping diamond due to their small size also have other draw backs. For n-type dopants phosphorus and nitrogen the activation energies are 0.6eV[2.22]and 1.6eV[2.23] respectively. This is very high when compared with other semiconductors (activation energies for arsenic and boron in silicon are 0.049eV and 0.045eV respectively [2.24]) and results in low carrier concentrations at room temperature which is not ideal. The activation energy for boron is lower at 0.37eV[2.25], but still results

in low activation of carriers at room temperature. In *figure 2.3.1* the activation energies of these impurity atoms can be seen in reference to either the conduction band or valence band. Boron doping can result in increased conductivity at room temperature but only in very high doping concentrations in order to offset the low number of carriers active at room temperature.

Diamond can be bulk doped by impurity atoms such as boron during CVD growth by introducing the impurities in the gas phase [2.26]. However this is not particularly controllable on the nanometer scale. As impurity concentrations in semiconductors are increased, the mobility of charge carriers can decrease due to increased impurity scattering events. As bulk boron doping in diamond requires a high concentration of boron in order to achieve appreciable carriers at room temperature this leads to low carrier mobility. In order to reduce the detrimental effect on mobility of incorporating large quantities of boron into diamond, the method of delta doping can be employed. Delta doping is a technique whereby a thin layer of doped diamond is grown during CVD growth including impurity atoms[2.27]. This thin layer is sandwiched between the intrinsic bulk of the diamond and a layer of intrinsic diamond grown on top of the doped layer. In theory this can result in a large density of charge being confined to a few atomic layers of doped diamond to act as a charge transfer layer. The wave functions of the carriers should extend into the intrinsic areas of the diamond reducing the scattering events as there are much fewer impurities in the intrinsic region. Carrier concentrations in the region of $10^{15}/cm^2$ have been reported at room temperature for delta doped layers, however this layer had a mobility of just 2.9 cm^2/Vs [2.28], showing that delta doping still requires substantial progress to be made.

2.4 Surface transfer doping of diamond

As discussed previously, diamond produced by CVD growth typically results in films with hydrogen terminated surfaces. This is not the only option regarding the satisfaction of dangling bonds on the surface of diamond. Other alternative elements can terminate diamond satisfying the “dangling” bonds. In this work the terminations of interest are hydrogen and oxygen.

An “unterminated” diamond interface has an ionization potential (IP) (which is the energy required to excite an electron from the valence band to the vacuum level) of 5.9eV. This is due to the electron affinity (which is the energy required to move an electron from the conduction band minimum of a material to the vacuum level) being 0.4eV and the band gap being 5.5eV. Oxygen termination increases the electron affinity of the diamond surface to

1.7eV. This results in an ionization potential of oxygen terminated diamond of 7.2eV. Hydrogen termination results in the electron affinity of the diamond decreasing to -1.3eV. Thus the ionization potential of hydrogen terminated diamond at the surface is 4.2eV[2.29], the lowest of any semiconductor.

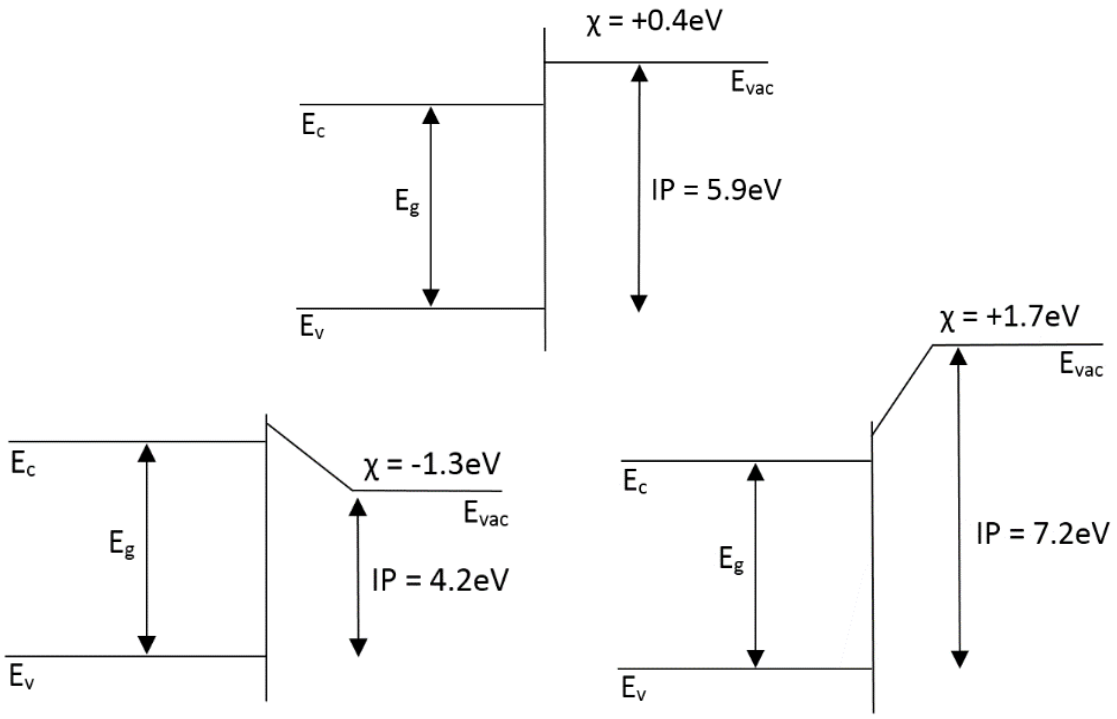

Fig 2.4.1 – Band alignment of unterminated diamond (top) Hydrogen terminated diamond (bottom left) and oxygen terminated diamond (bottom right).

The negative electron affinity of hydrogen terminated diamond is caused by the negative surface dipole which arises from the hydrogen-carbon bonds at the surface. The surface dipole pulls the vacuum level of the diamond surface below the conduction band maximum (CBM) by 1.3eV and reduces the ionization potential to 4.2eV. This means that if a suitable acceptor medium is near the surface of hydrogen-terminated diamond, it will become energetically favorable for electrons to leave the valence band of the diamond leaving behind free holes. These holes accumulate near the surface of the hydrogen terminated diamond and can be modeled as a 2 dimensional hole gas (2DHG).

For a material to be a suitable surface acceptor it must have available energy levels close to or below the valence band maximum of hydrogen terminated diamond to make electron transfer energetically favorable[2.30]. Hydrogen terminated diamond in intimate contact with a suitable accepter layer before and after equilibrium can be seen in *figure 2.4.2*. For organic materials this means their lowest unoccupied molecular orbit (LUMO) must be greater than 4.2eV. For non-organic materials this means that the electron affinity must be more than 4.2eV. If a material has a LUMO or electron affinity much greater than 4.2eV

there is a greater level of transfer between the hydrogen terminated diamond and the material, leading to a greater concentration of electrons that can leave the diamond prior to equilibrium and therefore a larger concentration of holes accumulated at the surface.

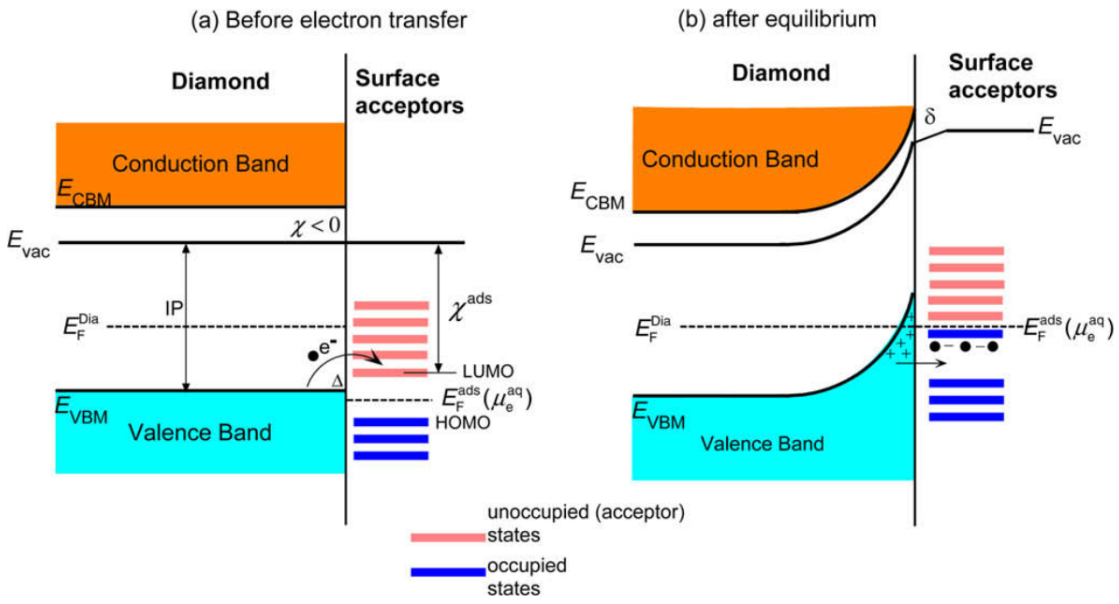

Fig 2.4.2 – Shows band alignment of hydrogen terminated diamond before and after equilibrium with a suitable surface transfer doping material[2.30].

Whereas hydrogen termination results in a 2DHG forming near the surface of the material, oxygen termination does not. In this way oxygen termination of the surface can be used to "Isolate" conductivity and confine it only to desired areas (active device regions) in order to eliminate parasitic conductive paths. In alternative material systems such as HEMTs this same effect is typically achieved by a "Mesa" etch through the active, conduction layer in order to remove the two dimensional electron gas (2DEG).

2.5 Carrier transport in a Semiconductor

To understand the performance of field effect transistors it is important to understand the transport of electrons and holes in a semiconductor.

The mobility of an electron or hole can be defined as follows[2.8]:

$$\mu = \frac{q\tau_c}{m^*} \qquad \textit{equation 2.5.1}$$

where q is the unit charge, τ_c is the mean time between scattering events and $m*$ is the effective mass of the carrier.

We can see in *equation 2.5.1* that the mobility is highly dependent on the mean time between scattering events of charge carriers. Carrier scattering mechanisms lead to large variation in mobility of electrons and holes as it can drastically increase the mean time between collisions. Some of the main scattering mechanisms in semiconductors are phonon scattering, surface roughness scattering, carrier-carrier scattering and coulomb scattering [2.8].

Arguably the two most important scattering mechanisms in hydrogen terminated diamond are coulomb scattering, and surface roughness scattering[2.31]. Coulomb scattering occurs when carriers have their paths deflected by the influence of charge in the lattice, be that ionized impurities or some other charge in proximity to the carriers. The proximity of the 2DHG to the surface of the hydrogen terminated diamond means that surface roughness scattering can also play a large role in the mobility of the 2DHG.

Under an electric field, carriers are accelerated by the field during their motion between scattering events [2.8]. This is known as the drift velocity, which can be seen in *equation 2.5.2*.

$$v = \mu E \qquad \textit{equation 2.5.2}$$

where E is the electric field strength and v is the drift velocity.

As the distance between scattering events is not changed, the application of an electric field reduces the time between such events. As more scattering events occur with unit time more energy is lost to them. The result of this is that electrons and holes cannot be accelerated continuously and reach a saturation velocity.

2.6 Field Effect Transistor operation and figures of merit

For discrete high-power field effect transistors (FETs), the most important parameters are maximum on state drain current, off state breakdown voltage, transconductance and on-resistance (R_{on}). R_{on} is important to minimize on state power loss (switching losses are more important for RF operation which is not discussed in detail in this work).

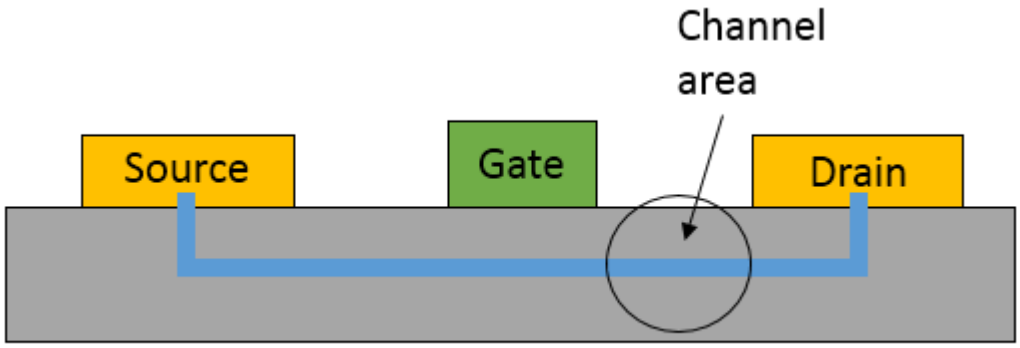

Figure – 2.6.1 – Simplified FET model showing source, drain and gate contacts.

An FET consists of 2 ohmic contacts (source and drain) and a gate, fabricated on a semiconducting material. By applying a potential difference between the source and drain contacts (V_{ds}) of an FET, current will flow between the source and drain, under the gate (assuming the gate is "on" as will be discussed shortly). This potential is typically applied between the source and drain contacts with the source grounded. In p-type electronics, as shown in this work, a negative potential is applied between the source and drain, allowing holes to flow from the source to the drain. In n-type electronics, a positive potential is applied for electrons flow from the source to the drain. As the potential is increased, the current through the FET increases due to the increasing velocity of the charge carriers in the channel. This is called the linear region as can be seen in *figure 2.6.2*. The velocity of the charge carriers will eventually saturate with increased electric field in the semiconductor, this, and pinch-off in the channel under the gate at increased drain potential, causes the current to saturate. This is called the saturation region as can be seen in *figure 2.6.2* If the potential is continually increased, eventually the FETs will be damaged due to the large electric field between the source and drain, and gate and drain, causing impact ionization in the material [2.32] or different breakdown mechanism at the metal-semiconductor interfaces.

A FET effectively operates as a switch, with the gate voltage (V_{gs}) determining whether the FET is "off" or "on". This potential is applied between the source and gate contacts with the source grounded. In the p-type electronics shown in this work, when a positive voltage is applied to the gate holes are depleted away from the area under the gate, decreasing the concentration of carriers under the gate. When there is sufficiently low carriers the FET will be "off" as there should be no, or very little current flow. When a negative voltage is applied to the gate, holes are accumulated under the gate increasing the number of charge carriers and turning the FETs "on". As the voltage is pushed more negative, the concentration of carriers under the gate increases, resulting in larger current flow. If the gate voltage is pushed too negative however, the gate leakage currents will increase (as will be discussed in chapter

2.7), which is undesirable and can damage the gate-semiconductor interface. In n-type electronics, as a positive voltage is applied to the gate, electrons are depleted away from the gate interface, reducing the concentration of charge in the channel under the gate, impeding charge flow between the source and drain, turning the FETs "off". If a positive voltage is applied, the concentration of electrons under the gate increases, allowing current to flow between the source and drain, turning the FETs "on".

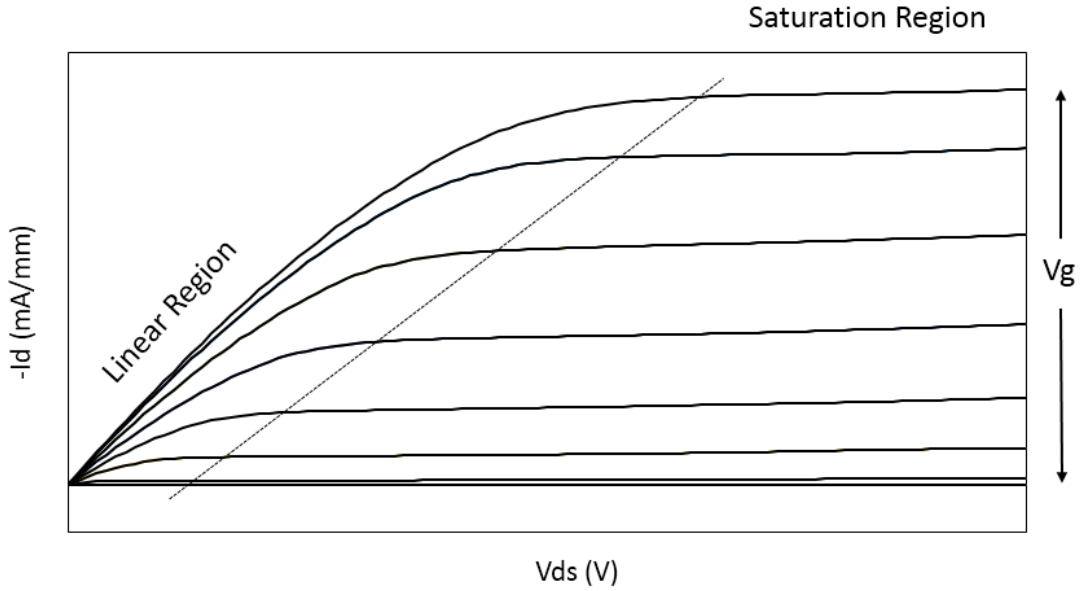

Figure 2.6.2 – Example output characteristic of p-type FETs characterized in this work.

A power FET should block high voltages when it is "off" and allow large current flows through the FET when it is "on". It must do this with minimal power losses.

A FET can be visualised as a simple series resistor network when operating in the linear region. As with a real series resistor network the current path will be dominated by the largest resistances, thus it is important to minimise the resistance in each region of the device. As can be observed in the simplified FET model in *figure 2.6.3*, R_c is the contact resistance and is determined by the "ohmic" contact made to the device channel. R_a is the "access" or "channel" resistance, which is determined by the resistance of the intrinsic charge layer in the FET, $R_{under\ gate}$ is determined by the gate contact. For a p-type semiconductor, when a metal with a low work function comes into contact with the substrate a depletion region is formed (assuming the semiconductor is sensitive to metal work function, as hydrogen terminated diamond is) whereby holes are depleted away from the gate. When the gate contact is biased with a negative voltage holes accumulate at the surface of the diamond forming a channel for current to flow between the source and drain. Thusly the resistance under the gate is determined by the ability of the gate contact to accumulate and deplete charge beneath the gate.

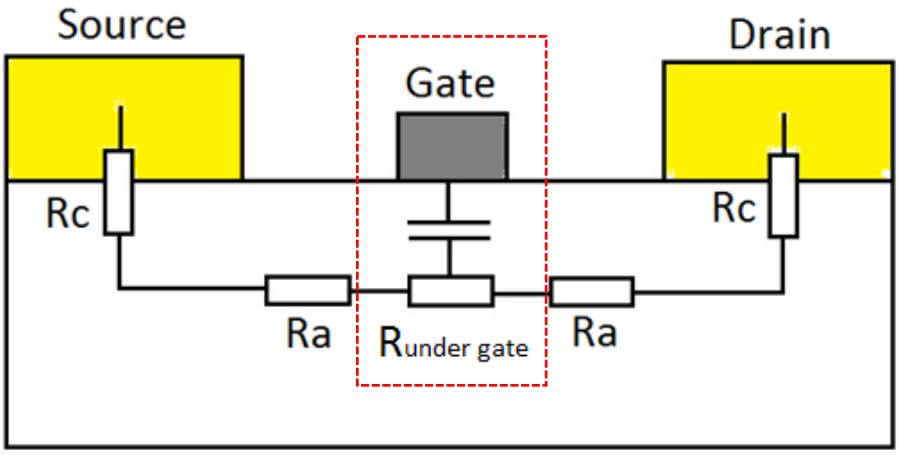

Fig 2.6.3 – Simplified model of FET showing intrinsic area within red square.

$$R_{on} = 2R_c + 2R_a + R_{under\ gate} \qquad equation\ 2.6.1$$

When an FET is operating at high drain bias, the maximum current can be defined as[2.33]:

$$I = Wvnq \qquad equation\ 2.6.2$$

where W is the channel width, v the carrier saturation velocity, n is concentration of charge in the channel, and q is the unit charge.

It can be seen from *equation 2.6.3* the maximum current through an FET is heavily dependent on both the carrier density and carrier saturation velocity in the channel. These are both intrinsic to the semiconductor material in the channel areas, and dependent on the performance of the gate contact under the gate. Diamond has the potential for extremely high values for both carrier density and carrier saturation velocity. One of the key aspects of this work has been to increase the carrier concentration in the channel by including surface transfer doping oxides in the "access" regions of FETs.

As mentioned previously, the concentration of carriers under the gate also heavily contributes to the maximum current as the carriers must pass under the gate, and the carrier concentration under the gate is dependent upon the voltage applied to the gate contact. Therefore, how well the gate can accumulate charge is important to understand. This can be assessed by the transconductance of the FETs. Intrinsic transconductance (g_m^*) is defined as the rate of change of drain-source current with respect to gate-source voltage for a constant drain-source bias as can be seen from *equation 2.8.3*[2.34].

$$g_m^* = \left(\frac{dI_{ds}}{dV_{gs}}\right)_{V_{ds}} \qquad \textit{equation 2.6.3}$$

The intrinsic transconductance (gm^*) only applies to the gate contact and does not take into account the voltage drop between the source and gate contacts. The extrinsic transconductance (g_m) which includes the source resistances, R_s (which is equal to R_c+R_a) can be defined as follows in *equation 2.6.4* [2.35]:

$$g_m = \frac{g_m^*}{1+ g_m^* R_s} \qquad \textit{equation 2.6.4}$$

2.7 Metal Semiconductor interfaces

To utilize a semiconductor material in electronic device applications, there is a need to inject and eject charge from the material via ohmic contacts. To do this we must understand how the semiconducting material interfaces with metals. The gates of the FETs made in this work are produced by Schottky, or Metal Oxide Semiconductor (MOS) contacts which are used to accumulate or deplete charge under the gate. As this work relates to hydrogen terminated diamond which is a p-type semiconductor, only p-type interfaces will be discussed.

Due to the low density of pinning states at the surface, hydrogen terminated diamond obeys the Schottky- Mott rule and has an un-pinned fermi level allowing the fermi level of the diamond to align with metal it comes into contact with [2.36].

The work function of a metal ($Ø_m$) or semiconductor ($Ø_s$) is the energy required to remove an electron from the fermi level of the material to the vacuum level. If a metal and semiconductor with differing work functions come into intimate contact, charge transfer occurs until the fermi levels align at equilibrium by diffusion of electrons across the interface[2.37].

Ohmic Contacts

An ideal ohmic contact results in no barrier for carriers at the interface between the semiconductor and metal and provides a linear current response with applied voltage. Ohmic contacts are used in this work to form the source and drain contacts of the fabricated FETs.

To form a p-type ohmic contact, the work function of the metal must be greater than the work function of the semiconductor. This case can be seen in *figure 2.7.1*. As discussed previously, charge transfer occurs at the interface until equilibrium is reached. In this case,

electrons flow from the semiconductor to the metal, bending the bands downwards. After equilibrium holes flowing from the semiconductor to the metal see no barrier as can be seen in *figure 2.7.2*.

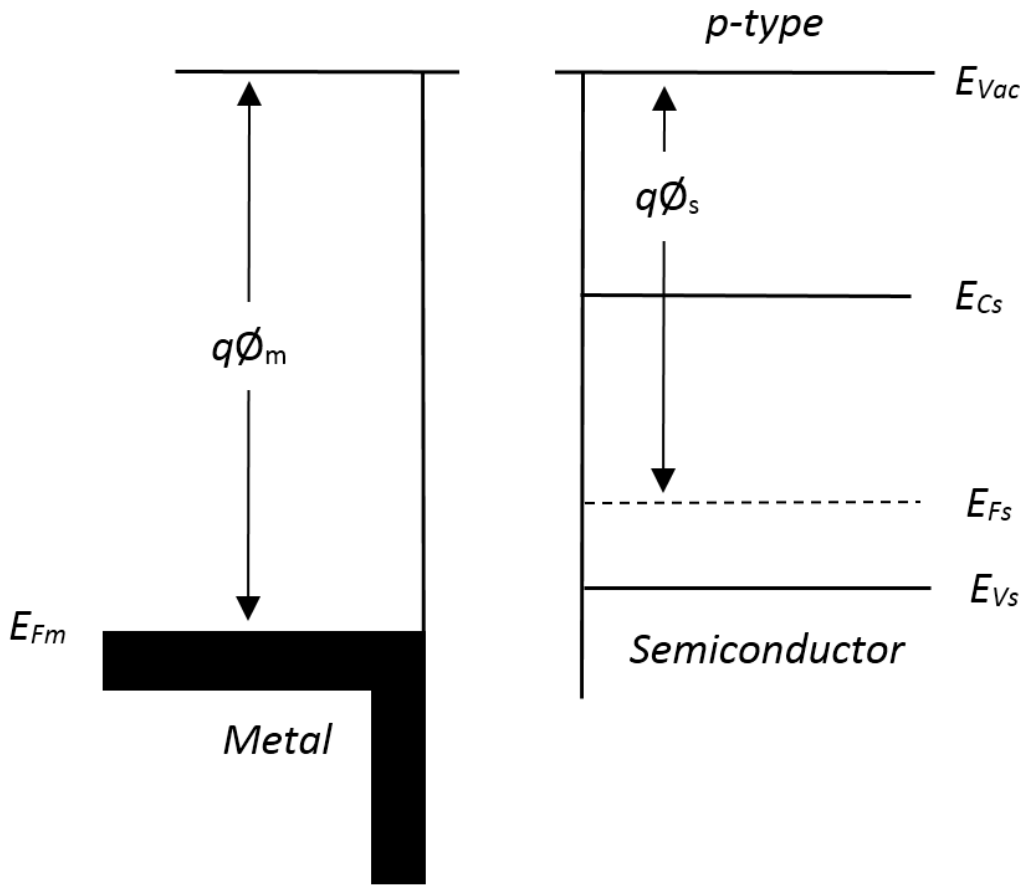

Fig 2.7.1– Metal with work function greater than p-type semiconductor prior to equilibrium.

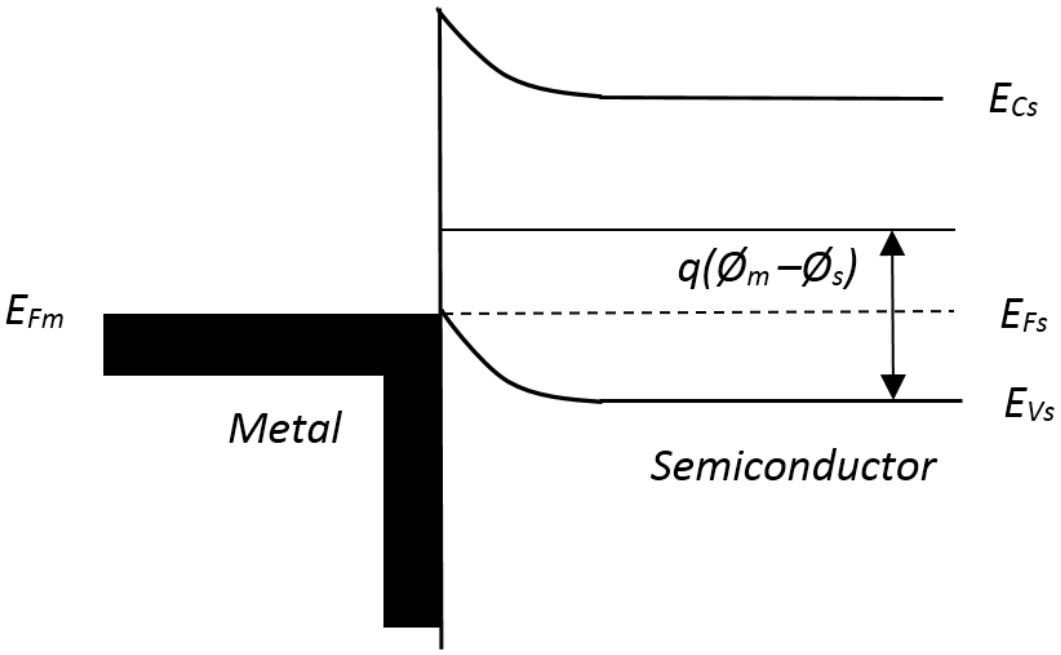

Fig 2.7.2 - Metal with work function greater than p-type semiconductor after equilibrium.

Schottky contacts

To form a Schottky contact on a p-type semiconductor the work function of the metal must be less than the work function of the semiconductor. Shottky contacts are used in this work to form the gates in a MESFET configuration.

As discussed previously charge transfer occurs between the metal and semiconductor until the fermi levels align at equilibrium. For equilibrium to be reached electrons must transfer between the metal and semiconductor, which causes a build-up of charge at the interface and bends the semiconductor bands upwards, forming a depletion region on the semiconductor side of the interface (*W*) as seen in *figure 2.7.4.* After equilibrium the barrier to hole flow from the semiconductor to the metal is shown in *figure 2.7.4* as $qV_{bi.}$

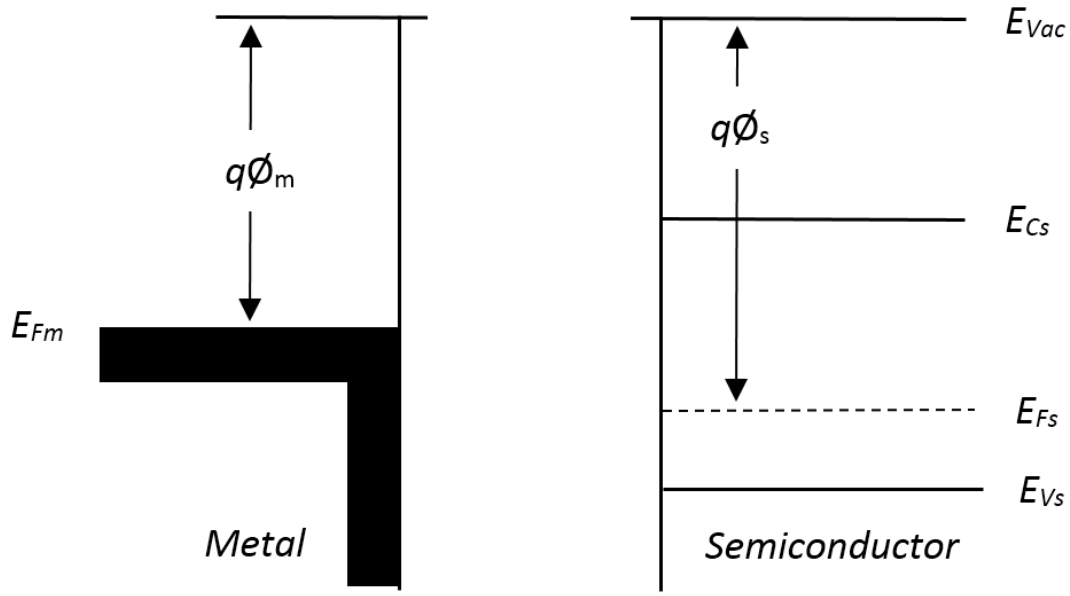

Fig 2.7.3 – Metal with work function less than p-type semiconductor prior to equilibirum.

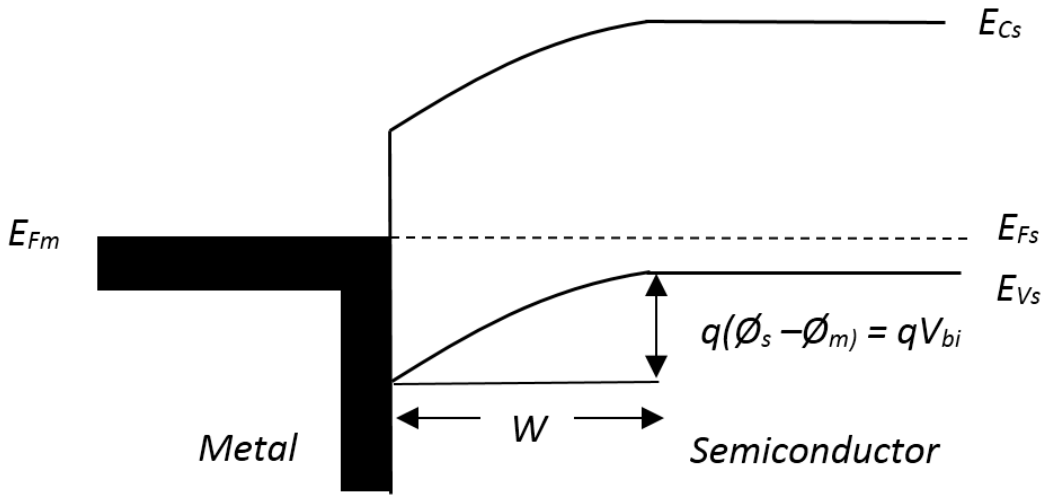

Fig 2.7.4 – Metal with work function less than p-type semiconductor after equilibrium, showing potential barrier V_{bi} and depletion region W.

For charge to flow through a Schotty-semiconductor interface charge must find a way to overcome the potential barrier. The main ways carriers can do this is through Thermionic emission (TE), Field emission (FE). Thermionic emission is when a carrier has sufficient thermal energy to overcome the barrier height in the semiconductor-metal interface and is thus highly reliant on temperature. Field emission occurs when carrier's tunnel through the barrier, it is highly dependent on the "tunneling" probability, which is itself highly dependent on the concentration of carriers at the interface and the width of the potential barrier [2.38].

As mentioned previously, Schottky contacts have been used to create the gate contact of FET structures in a Metal-Semiconductor FET (MESFET) configuration in this work. When a positive voltage is applied to the metal contact, (as can be seen in *figure 2.7.5*) this results in a larger barrier to holes. This also depletes holes on the semiconductor side of the interface, leading to a lower concentration of carriers on the semiconductor side of the interface. In this work this is used to turn the FETs "off". When a negative voltage is applied to the metal side of the interface, this results in a lower barrier for holes (as seen in *figure 2.7.6*), which causes an accumulation of mobile holes on the semiconductor side of the interface if there are available mobile holes. In this work this is used to turn the FETs "on" and provide a charge transfer layer under the gate. At sufficiently negative voltage the schottky barrier height will be reduced enough that holes can flow easily from the semiconductor to the metal, resulting in gate leakage current.

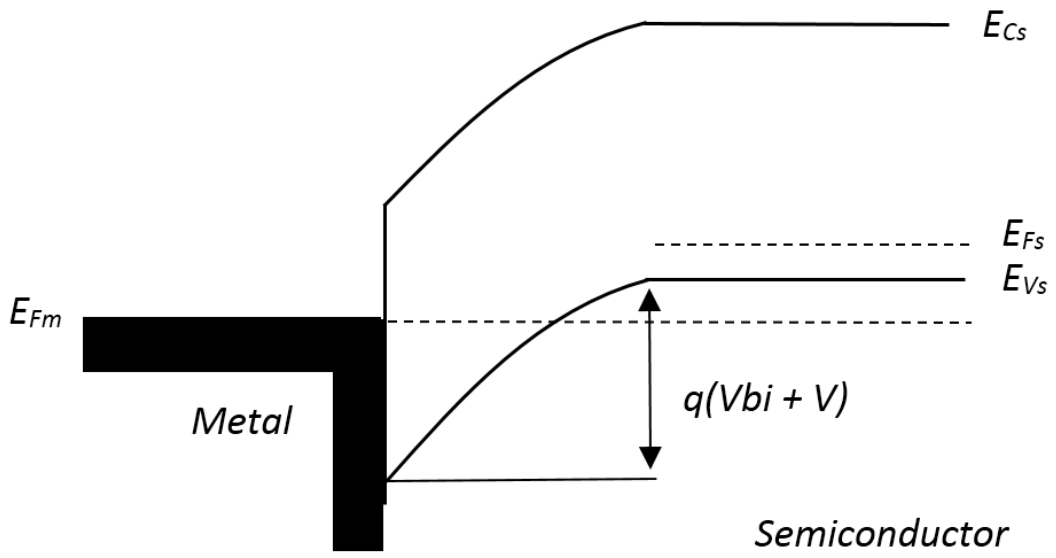

Fig 2.7.5 – Shows p-type semiconductor Schottky contact under positive voltage resulting in increased potential barrier height.

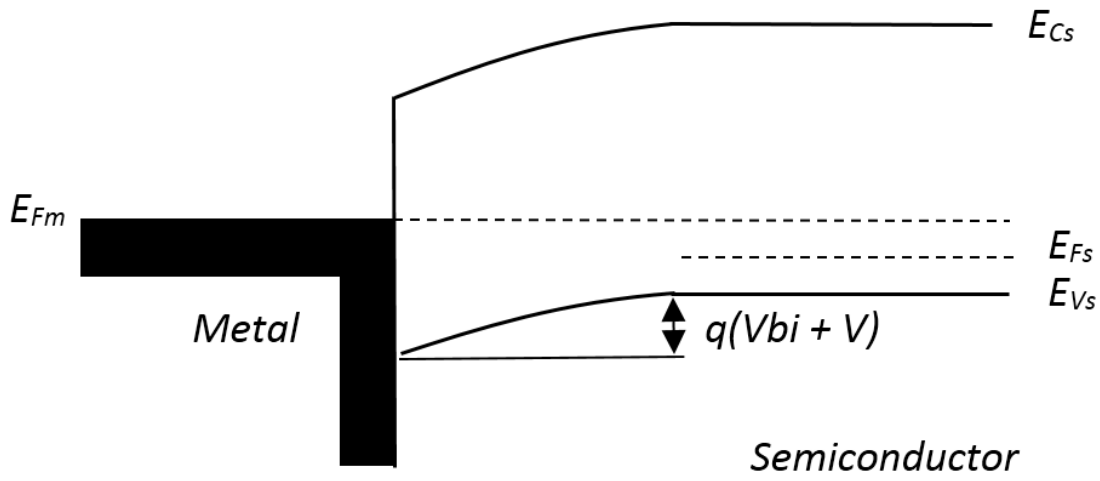

Fig 2.7.6 – Shows p-type semiconductor Schottky contact under negative voltage resulting in decreased potential barrier height.

MOS interface

A special mention must be given to the Metal-Oxide-Semiconductor (MOS) interface as this is used to create the gate contacts in a MOSFET configuration later in this work. The ideal MOS interface can be modeled as a parallel plate capacitor, with the gate metal acting as one plate and the semiconductor as the other[2.39]. For the discussion here of an ideal MOS interface we assume that the semiconductor and metal have the same work function.

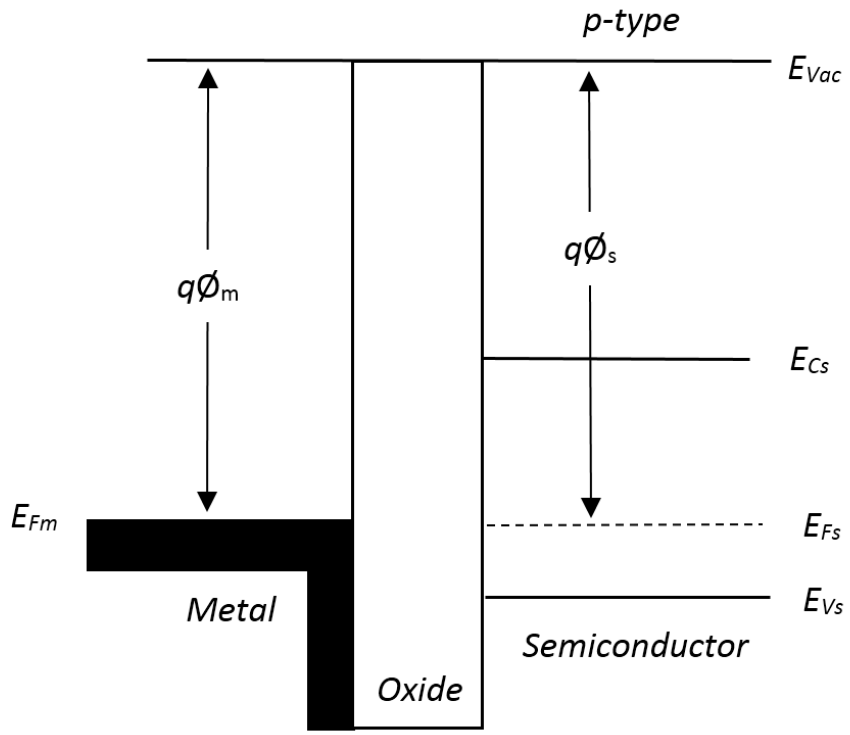

Fig 2.7.8– Metal Oxide Semiconductor interface band diagram of a p-type semiconductor at V = 0.

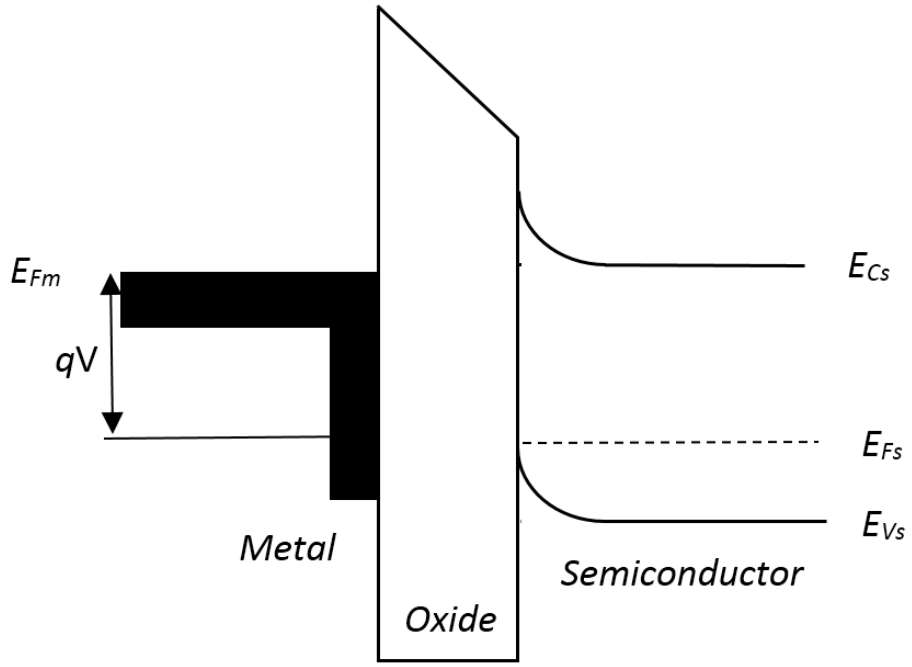

Fig 2.7.9 – Metal Oxide Semiconductor interface band diagram of a p-type semiconductor with voltage <0 applied to the gate metal.

When a negative voltage is applied to the metal contact, there is an accumulation of positive charge (mobile holes) on the semiconductor side of the oxide due to the negative charge on

the metal side as can be seen in *figure 2.7.9*. In this work this has been used to turn the FETs "on" by increasing the concentration of mobile holes beneath the gate contact.

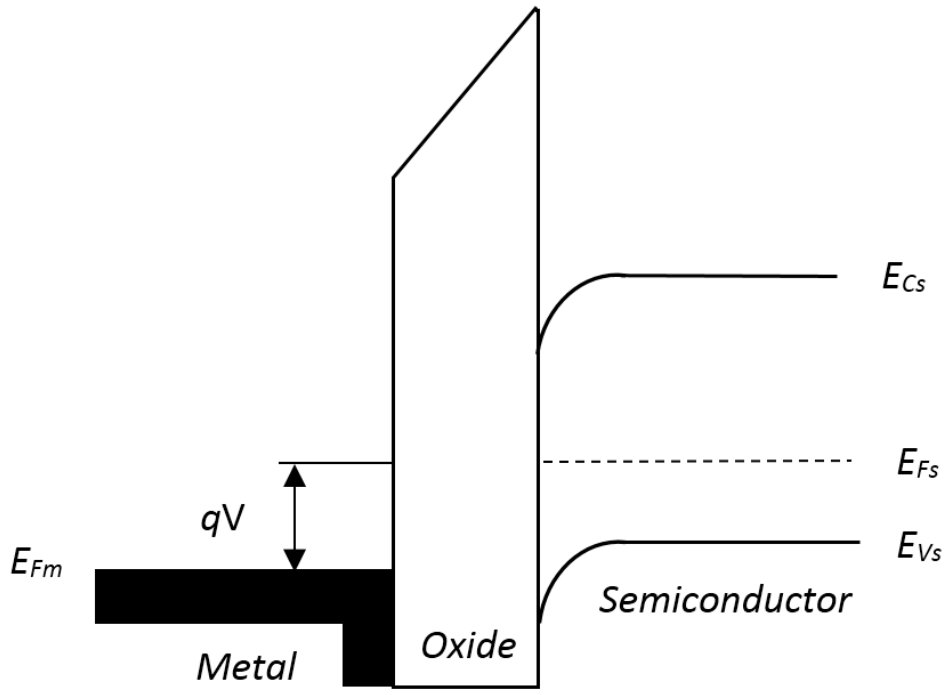

Fig 2.7.10– Metal Oxide Semiconductor interface band diagram of a p-type semiconductor with voltage >0 applied to the gate metal.

When a positive voltage is applied to the metal contact, there is an accumulation of negative charge at the semiconductor side of the interface due to the positive charge on the metal side as seen in *figure 2.7.10*. In this work this has been used to turn the FETs "off" by depleting the positive charge carriers (holes) away from the region under the gate contact, reducing the concentration of carriers under the gate.

As voltages become sufficiently large, tunneling currents through the oxide become increased. This can lead to permanent dielectric breakdown [2.40].

Chapter Summary

This chapter has addresed the theory behind diamond as an electronic material, beginning by discussing the structure of the carbon atom and the diamond lattice, and how these give rise to the impressive intrinsic properties of diamond which could prove useful for electronic applications. Following this, the chapter discussed the growth of synthetic diamond for electronic applications. The chapter has also addressed the challenges of substitutionally doping diamond and the novel doping method of surface transfer doping which is utilised in the FETs in this work. Finally the chapter has discussed semicondutor physics, addressing

current transport through a semiconductor, the basic figures of merit for FET operation with respect to high power applications, metal-semiconductor interfaces, and metal-oxide-semiconductor interfaces which will be used to produce the FETs reported in this work.

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3. Literature review

This chapter begins by outlining the development of the model used to understand the surface conductivity of hydrogen terminated diamond. The first sub chapter also explores what has been achieved in the realm of improving the sheet resistance and high temperature stability of the 2DHG of hydrogen terminated diamond by investigating alternative surface electron acceptor materials.

The second sub-chapter follows the development of hydrogen-terminated diamond FETs, detailing the different surface materials used to control the surface transfer doping process which have been used to increase the performance of the FETs, as well as what has been achieved using surface transfer doping diamond FETs in the high power operating space, with particular focus placed on maximum drain current, extrinsic transconductance, off-state breakdown voltage, and stability of performance at elevated temperatures.

Finally, the chapter briefly explores what has been achieved in the development of boron doped diamond FETs.

3.1 Surface transfer doping

As discussed in chapter 2, surface transfer doping is the process which allows the creation of a two-dimensional hole gas (2DHG) by transfer of electrons across the hydrogen terminated diamond to acceptor materials on the surface, which leave behind mobile holes which can be used as a charge transfer layer. In this work the 2DHG is utilized to create FETs on hydrogen terminated diamond.

In 1989 M. Landstrass and K. Ravi observed that diamond grown by CVD growth terminated with hydrogen showed high surface conductivity. This effect was reported to be removed by heating the diamond films in atmosphere. At the time of the publication of this work the conductivity was thought to be due to hydrogen passivation of traps in the diamond films, which could be reversed by removal of the hydrogen termination by a high temperature anneal [3.1]. After a re-introduction to hydrogen plasma the conductivity was again observed, confirming that hydrogenation of the diamond surface played a key part in the observed conductivity.

It was not until the year 2000 that the now widely accepted model for conductivity of hydrogen terminated diamond was published by F. Maier *et al*. [3.2]. It was shown that the surface conductivity could be removed by annealing in ultra-high vacuum. This effect could

be reversed and the conductivity restored by re-exposure to normal atmosphere. If annealed above 230°C in atmosphere the effect of reducing the conductivity is irreversible. This was reported to be due to the removal of hydrogen termination of the surface and replacement with oxygen. This showed that the surface conductivity was due to both the hydrogen termination of the surface and it's interaction with atmospheric exposure. In this work a model for surface transfer doping was developed. It was proposed that due to the negative electron affinity of hydrogen terminated diamond electrons will readily leave the surface of the diamond. This negative electron affinity and it's properties of allowing unbound electrons to leave the diamond surface have been extensively explored in the past [3.3, 3.4]. If a material with an electron affinity or chemical potential larger than 4.2eV interfaces with the hydrogen terminated diamond surface electrons will leave the valence band of the diamond and leave behind holes which form a two dimensional hole gas (2DHG) near the surface of the diamond. This effect can be seen below in *fig 3.1.1*. It was calculated that a thin "water layer" which forms on all surfaces exposed to atmosphere would provide a layer with a chemical potential of around 4.4eV, placing it's Lowest Unoccupied Molecular Orbit (LUMO) below the valence band of hydrogen terminated diamond.

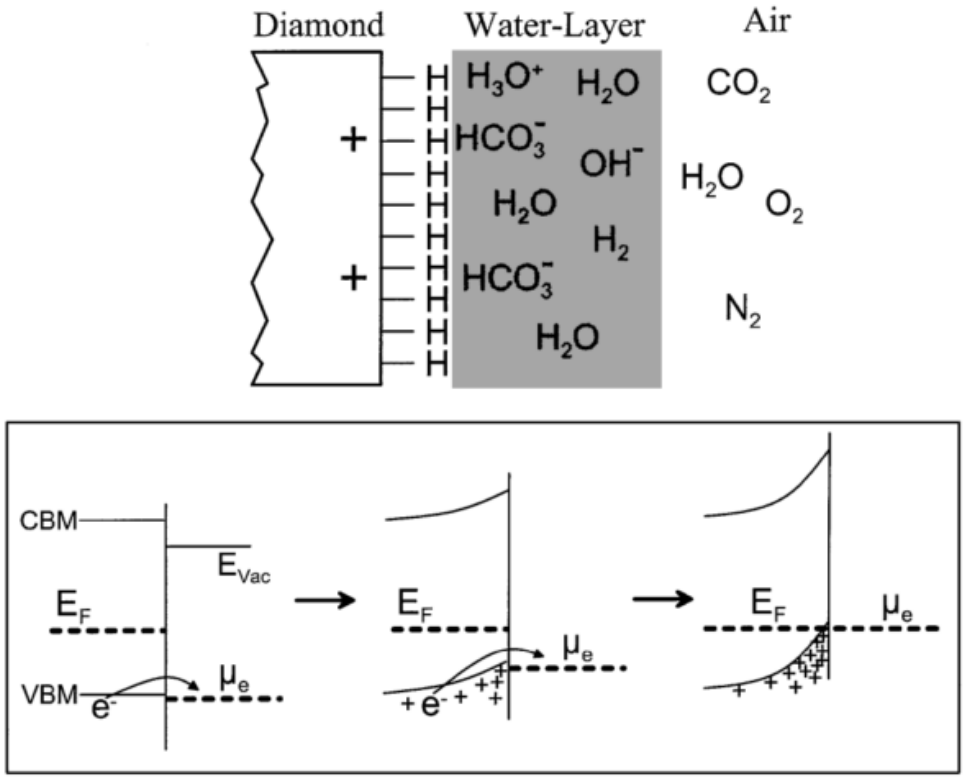

Fig 3.1.1 – Surface bending and accumulation of holes due to "water layer" on h-diamond surface proposed by F. Maier et al [3.2].

Following the publication of the model proposed by F. Maier *et al*, J. Goss *et al* reported simulations from first principles of various adsorbate layers with electron affinities close to or above 4.2eV such as NO_2 and C_{60} [3.5]. In this publication Goss *et al* used local density functions to calculate the electron affinities of the adsorbate clusters. Of most interest from this paper was the demonstration of charge transfer between hydrogen terminated diamond and C_{60} fullerenes.

In the succeeding years the hypothesis of atmospheric adsorbates and hydrogen termination giving rise to surface conductivity, and the mechanism of hole transfer from diamond into the atmospheric adsorbates was investigated by M. Kubovic *et al*. The first effort was to expose hydrogen terminated diamond to NO_2 vapour, oxygen, and argon [3.6] and compare the sheet carrier concentration induced in each case. In this publication it was observed that exposure to NO_2 increased the carrier concentration in the 2DHG and exposure to oxygen and argon has little effect on the carrier concentration. It was also observed that increasing the concentration of NO_2 gas resulted in an increase in 2D carrier concentration up to $2.3x10^{14}$ /cm^2. However the concentration of carriers decreased exponentially when the diamond was exposed to normal atmospheric conditions, emphasizing the need for passivation of the H-diamond/NO_2 material system in order to maintain the increased carrier concentration.

Y. Takagi *et al* [3.7] isolated the chemical composition of the previously vaguely described "atmospheric adsorbates" and calculated the LUMO and Highest Occupied Molecular Orbit (HOMO) of each. In *figure 3.1.2* it can be seen the LUMO and HOMO of various atmospheric species as well as that of hydrogen terminated diamond of each orientation (100, 110, 111). It was experimentally demonstrated that NO_2, O_3, SO_2 and NO demonstrate surface transfer doping. However, H_2O, N_2O and CO_2 show no surface transfer doping. This further promotes the hypothesis reached by Maier *et al.* It was also shown that the concentration of carriers in the diamond is dependent upon the energy level difference between the LUMO of the atmospheric adsorbate and VBM of hydrogen terminated diamond. The larger the energy difference, the more electrons are able to leave the surface of the hydrogen terminated diamond prior to equilibrium.

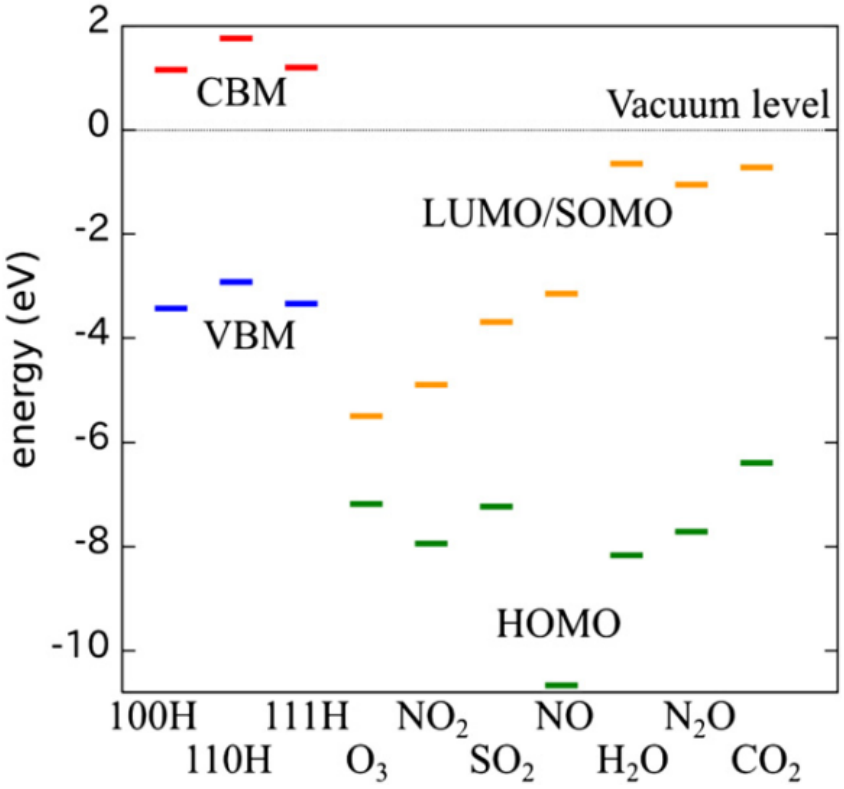

Fig 3.1.2 – Energy levels of hydrogen terminated diamond of orientations 100, 110 and 111 and the LUMO and HOMO levels of chemical components of atmospheric adsorbate layer from [3.7].

Following this, research groups investigated alternative materials with LUMOs lying below the valence band of hydrogen terminated diamond. Initially P. Strobel *et al*. showed success in utilizing fullerenes C_{60} and $C_{60}F_{48}$ [3.8] to induce surface transfer doping, achieving carrier concentrations of $10^{12}/cm^2$ for C_{60} and $10^{13}/cm^2$ for $C_{60}F_{48}$, exceeding what had been shown with "atmospheric adsorbates". Following this it was also reported that without encapsulation these materials sublimate from the diamond surface at 200°C[3.9]. This work was followed by demonstration of the material "tetrafluoro-tetracyanoquinodimethane" (F_4-TCNQ) by D. Qi *et al*, which showed a similar sheet hole density to what was achieved using $C_{60}F_{48}$ [3.10]. These publications confirmed the simulations performed by Goss *et al* with regards to the surface transfer doping of C_{60}, and that alternative organic materials could be used to replace "atmospheric adsorbates" for the purpose of surface transfer doping hydrogen terminated diamond.

Although the demonstration of organic films was encouraging, it was also shown that they did not perform adequately at elevated temperatures without encapsulation. It was theorized that inorganic layers with electron affinities higher than 4.2eV could also be used as more thermally robust surface transfer doping layers. To this end it was demonstrated by S. Russel

et al [3.11] that the material molybdenum trioxide (MoO_3) could be utilized to surface transfer dope H-diamond. It was shown that the increased electron affinity in comparison to the potential energy of atmospheric adsorbates lead to greatly increased carrier concentration. It was reported that the carrier concentration of the sample in this work increased from $1x10^{13}$ with atmospheric adsorbates, to $2.16x10^{13}$ after deposition of MoO_3. Although there was also decrease in mobility, this corresponded to a change in sheet resistance from 9.1kΩ/□to 5.6kΩ/□. In order to demonstrate that the MoO_3 is responsible for the surface transfer doping the surface of the diamond was annealed at 400 °C for 1 hour in order to remove all atmospheric adsorbates and ensure surface transfer doping was due only to the MoO_3.

Following this work, M. Tordjman *et al* expanded on the demonstration of MoO_3 by showing that H-diamond using MoO_3 layers could maintain stable carrier concentrations at temperatures in excess of 300°C [3.12].

Following the publication of MoO_3 as a surface transfer doping medium, K. Crawford *et al* showed the surface transfer doping potential of another high electron affinity material vanadium pentoxide (V_2O_5) [3.13]. V_2O_5 showed an increase in carrier concentration to $1.8x10^{13}$ compared to a carrier concentration of $3x10^{12}$ for atmospheric adsorbates and increased stability at elevated temperatures, with V_2O_5 surface transfer doping remaining stable up to 250 °C.

After the demonstration of high electron affinity inorganic layers as surface transfer dopants C. Verona *et al* demonstrated a comparison between MoO_3, V_2O_5 tungsten oxide (WO_3), niobium oxide (NbO_5), and aluminium oxide (Al_2O_3) deposited by electron beam evaporation [3.14]. All of these materials exhibited surface transfer doping other than Al_2O_3 which exhibited a higher sheet resistance than the control sample using atmospheric adsorbates after deposition. Al_2O_3 has a low electron affinity and therefore should not induce surface transfer doping. It may be that any conductivity can attributed to atmospheric adsorbates encapsulated by the Al_2O_3 deposition. This paper also shows a correlation between the work function of the surface transfer doping layer and the carrier concentration in the 2DHG as shown in *figure 3.1.3*. It was also reported that the mobility of charge decreases as the concentration of charge increases in the 2DHG for each of the demonstrated oxides.

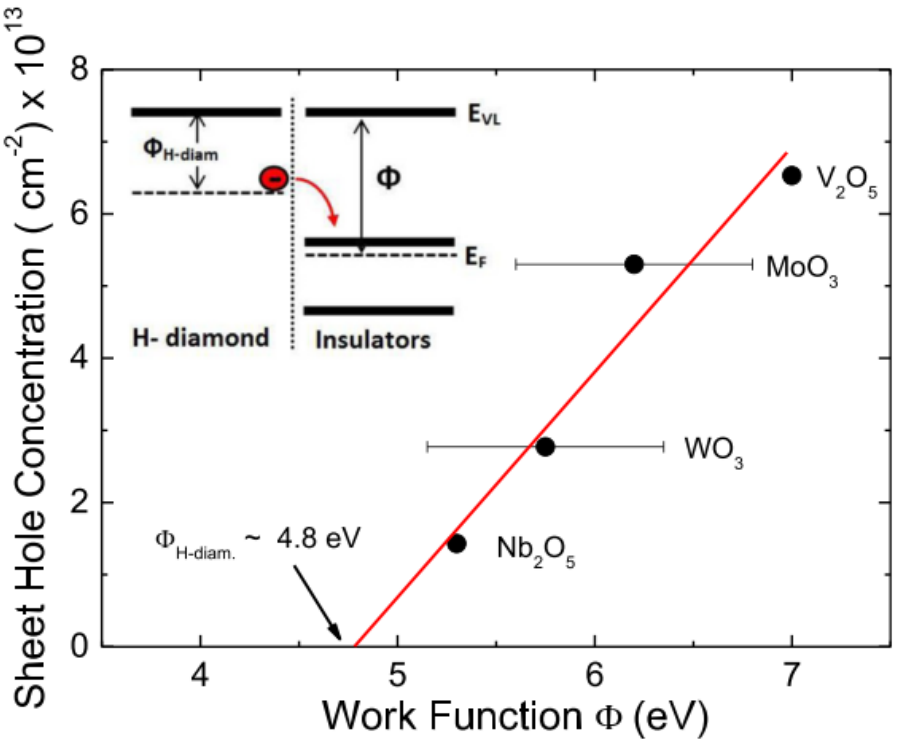

Fig 3.1.3. - Relationship between the work function of some surface transfer layers and carrier concentration in diamond using these layers as shown by C. Verona et al [3.14].

Following this work, M. Tordjman *et al* further showed the potential of WO_3 as a surface transfer doping oxide and introduced another potential surface transfer doping material in rhenium oxide (ReO_3). In this publication it was shown that *Rafi et al* had achieved the highest reported carrier concentration in the 2DHG with WO_3, reporting a carrier concentration of 4.78×10^{14} /cm^2. ReO_3 showed stable performance up to 450 °C in atmospheric conditions, the highest operational temperature demonstrated for surface transfer doping oxides [3.15].

As other research groups focused on inorganic alternatives to "atmospheric adsorbates", groups in Japan concurrently worked on the passivation of atmospheric adsorbate layers on the diamond surface. To this end A. Daicho *et al* showed that the sheet resistivity of hydrogen terminated diamond films can be maintained by deposition of thin films of Al_2O_3 by "low temperature" ALD on the hydrogen terminated diamonds surface [3.16]. In this publication the Al_2O_3 was reported to "passivate" the atmospheric adsorbates on the surface prior to Al_2O_3 growth. Al_2O_3 has a small electron affinity (1eV) which should not allow transfer of electrons from the valence band of the diamond to the Al_2O_3 as proposed by the surface transfer doping model. However H. Kawarada *et al* showed that the ALD Al_2O_3 deposited at higher temperatures could perform adequate surface transfer doping after atmospheric adsorbates have been removed from the surface and proposed a model whereby surface

transfer doping can be achieved using Al_2O_3 due to fixed charge in the Al_2O_3 layer acting as an acceptor layer. There has also been some discussion that the surface conductivity shown by ALD Al_2O_3 may be due to the ALD precursors forming an adsorbate layer [3.17].

Following the demonstration of ALD Al_2O_3 inducing surface transfer doping, D. Kueck *et al* began to explore AlN films grown on hydrogen terminated surface by ALD. The deposition temperatures were above 370°C which was intended to remove adsorbates from the diamond surface. FETs were fabricated, and the output characteristics measured using atmospheric adsorbates, they were then passivated using AlN and their output characteristics measured again. The un-passivated FETs showed a maximum drain current of -160mA/mm and the passivated FETs showed a maximum drain current of -100mA/mm. Although the reduction in maximum drain current is disappointing, it is hoped the passivation would provide a more thermally robust surface transfer doping layer. Keuck *et al* surmised that the exhibited surface transfer doping may be due to polarization of charge due to the AlN layer [3.18]. Whether the surface transfer doping was due to residual adsorbates, ALD precursors or another mechanism remains unclear.

In relation to this work C. Pietzka *et al* showed hydrogen terminated diamond could show surface conductivity after removal of atmospheric adsorbates and growth of AlN films by Metal-Organic Chemical Vapour Deposition (MOCVD) leading to 2DHG formation [3.19]. A substrate was hydrogen terminated and showed a sheet resistance of 7kΩ/□ in atmosphere. After growth of AlN by MOCVD the sheet resistance of the diamond increased to 10kΩ/□. Although the sheet resistance of the sample had degraded, the temperatures at which the MOCVD growth takes place should remove residual atmospheric adosbrates from the H-diamond surface. Little explanation of the mechanism of surface transfer doping after MOCVD growth are explored. Following this, in another publication M. Imura *et al* demonstrated that a pretreatment of H_2 + NH_3 prior to MOCVD deposition of AlN [3.20] could lead to decreased sheet resistance of the hydrogen terminated diamond surface. After the pretreatment the 2DHG layer showed deceased sheet resistance in comparison with atmospheric adsorbates from 6.82kΩ/□ to 2.62kΩ/□. However, after AlN deposition the sheet resistance degraded substantially to 10.3kΩ/□. This may support the argument that AlN growth passivates a surface transfer doping mechanism rather than being a surface transfer doping medium itself.

Kasu *et al* continued their work with NO_2, moving on to show that the surface adsorbed NO_2 could be encapsulated using Al_2O_3 grown on the diamond surface by ALD in order to maintain the surface transfer doping of NO_2 over time and at elevated temperatures.

Passivation of NO_2 with Al_2O_3 provided a stable carrier concentration in vacuum at 150°C[3.21]. The NO_2 exposure and subsequent encapsulation using Al_2O_3 was used to produce FETs which showed the highest recorded drain current to date of -1.3A/mm due to the decreased sheet resistance of the surface in areas exposed to NO_2 [3.22].

The examples explored here show that there is still some contention among the diamond community as to what gives rise to the surface conductivity in hydrogen terminated diamond surfaces. For the purpose of this work the surface transfer doping model proposed by Maier *et al is* used to understand the mechanism of formation of the 2DHG.

The discussed publications have also shown that many alternatives are available for replacing atmospheric adsorbates in hydrogen terminated diamond in order to improve the concentration of carriers in the 2DHG and increase the stability at elevated temperature. For ease of reference, some important parameters for assessing alternative surface transfer dopants can be seen in *table 3.1.1* below. It has been shown that these alternatives offer increased carrier concentration in the material and the ability to engineer the sheet resistance to lower levels than previously observed. The thermal stability of these alternative surface transfer doping layers has far surpassed that offered by atmospheric adsorbates.

The surface transfer doping mechanism and materials discussed can be utilized to produce FETs as will be discussed in detail in the following chapter.

Material	*Electron affinity (eV)*	*Carrier concentration (/cm²)*	*Mobility (cm²/Vs)*	*Sheet resistance (kΩ/□)*	*Max stable temperature in atmosphere (°C)*	*Reference*
"Atmospheric adsorbates"	*≈ 4.2*	*≈ 1x10¹³*	*≈ 30-100*	*≈ 10*	*≈ 60*	*[3.2]*
NO_2	*≈ 5*	*2.3x10¹⁴*	*≈ 50*	*n/a*	*200 (encapsulated with Al_2O_3)*	*[3.6, 3.21]*
C60	*4.1*	*1x10¹²*	*n/a*	*n/a*	*150*	*[3.9]*
C60F48	*4.06*	*1x10¹³*	*n/a*	*n/a*	*150*	*[3.9]*
F4-TCNQ	*5.24*	*1.6x10¹³*	*n/a*	*n/a*	*n/a*	*[3.10]*
MoO_3	*6.7*	*2.16x10¹³*	*51.2*	*5.6*	*200*	*[3.11, 3.12]*
V_2O_5	*7.2*	*6.55x10¹³*	*38*	*2.6*	*250*	*[3.13, 3.14]*
WO_3	*6.4*	*4.78x10¹⁴*	*≈ 50*	*n/a*	*250*	*[3.14, 3.15]*
ReO_3	*6.7*	*3.12x10¹³*	*≈ 50*	*n/a*	*400*	*[3.15]*
Al_2O_3	*1*	*2.82x10¹²*	*89*	*38.6*	*n/a*	*[3.14]*
AlN (H_2+ NO_3 pretreatment)	*1.5*	*1x10¹⁴*	*6*	*10*	*n/a*	*[3.20]*

Table 3.1.1- Surface transfer doping "materials" and corresponding figures of merit for 2DHG.

3.2 – Surface transfer doping FETs state of the art

After the discovery of surface conductivity in diamond in 1989 it was not long before this method of charge conduction was utilised to produce FETs. H. Kawarada *et al* were the first to utilise the surface conductivity of H-diamond to fabricate diamond FETs in 1994 [3.23]. H. Kawarada *et al* took advantage of hydrogen terminated diamond's sensitivity to metal work function at the surface in order to produce Ohmic and Schottky contacts. In this publication it was detailed that a large work function metal such as gold could be used to form an Ohmic contact and a low work function metal such as aluminium can be used to from a Schottky contact on the same substrate without the requirement for contact annealing.

The resulting FETs showed good transistor action but very modest drain drain currents in the order of -2mA/mm and transconductance of 0.2mS/mm.

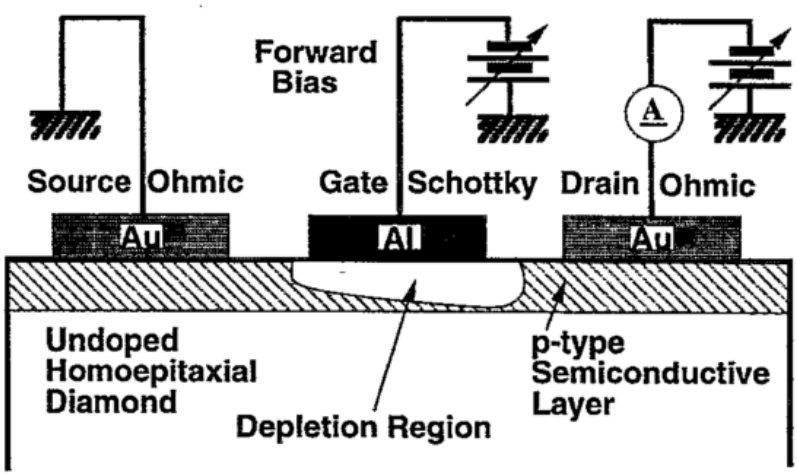

Figure 3.2.1 – Shows the structure of the first surface transfer doped H-diamond FET produced by Kawarada et al in 1994 [3.23].

Soon after the first diamond FETs were reported, K. Tsugawa *et al* demonstrated MESFET devices using Pb as a gate metal and also included a gate dielectric for the first time in a surface transfer doped diamond FET by including SiO_2 in the gate stack[3.24]. The Pb gated MESFET showed enhancement mode operation, maximum drain currents of -14mA/mm, and transconductance of 9mS/mm. Pb gated MOSFET using SiO_2 as a gate dielectric showed depletion mode operation, maximum drain currents of 18mA/mm, and a transconductance of 14mS/mm. This showed that both enhancement mode and depletion mode FETs could be realized on the same hydrogen terminated diamond substrate.

Following these initial publications, M. Kubovi and E. Kohn *et al* developed an alternative fabrication technique for hydrogen terminated diamond. In this method the surface would be blanket coated with metal (in this case gold) to form the ohmic contacts, and this would be etched to form the source drain gap with gate metallization deposited between the contacts. This served to protect the hydrogen termination of the surface during processing and solved some of the stability issues plaguing diamond FETs prior to this development, and resulted in higher maximum drain currents, reporting a maximum drain current of -48mA/mm [3.25]. This process would prove to be one of the most influential in the fabrication of diamond FETs and remains the most common route to fabricating FETs on hydrogen terminated diamond.

Continuing this work P. Gluche and E. Kohn *et al* showed breakdown of almost 200V for an FET with a large source-drain gap of 8.5µm. Showing that the breakdown is heavily dependent upon the source drain gap as would be expected [3.26]. The FETs showed low maximum drain currents of -22mA/mm. A drain current of -90mA/mm was obtained for a smaller gate length of 3µm. unfortunately breakdown data for the 3µm gate length FETs was not reported.

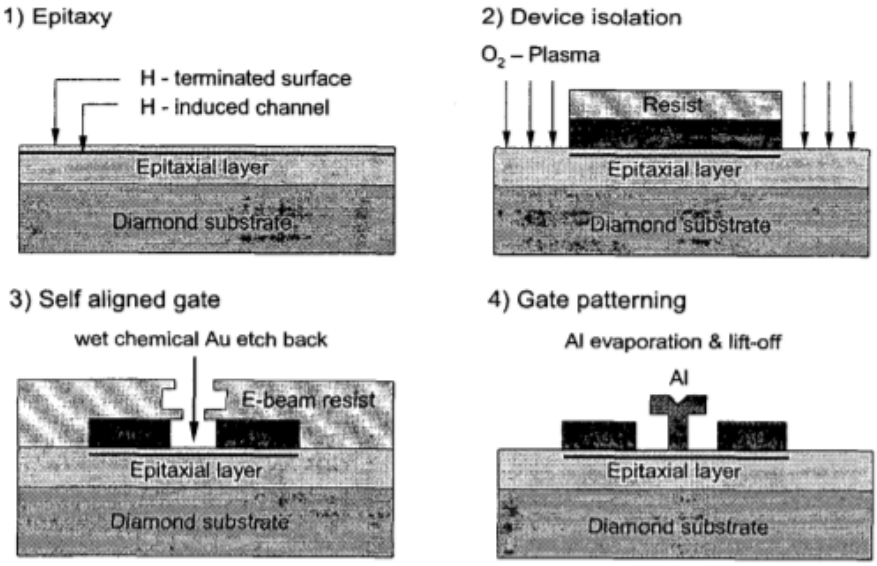

Fig. 4. Processing sequence of self aligned gate of diamond Schottky-gate FET technology.

Figure 3.2.2 – Shows "Self-aligned" gate process by wet etch of ohmic metal and deposition of gate metal as shown by M. Kubovi et al [3.25].

For the previously outlined FETs made on diamond larger gate lengths of around 3-10µm were used. The gate length was engineered down to 1µm by U. Hitoshi *et al* [3.27] who demonstrated FETs with drain currents of up to -150mA/mm and extrinsic transconductance of 110mS/mm, which would be expected due to the decreased gate length of the fabricated FETs. It was also proposed that gate lengths of 0.2µm could yield extrinsic transconductances in excess of 500mS/mm using this technology.

Following this A. Aleskov *et al* demonstrated FETs utilizing 0.2µm gates, achieving a maximum drain current of -360mA/mm, as well as an extrinsic transconductance of 148mS/mm [3.28]. This publication also included high voltage measurements showing device operation in the off state up to 68V before destructive breakdown occurred. Interestingly the paper also reports substantial degradation in maximum drain current

achieved for repeated large signal measurements, a 5µm gate length FET which showed a maximum drain current of -24mA/mm degraded to -5mA/mm after 10 repeated measurements. This work also reported a maximum oscillation frequency (f_{max}) of 40GHz and a cut-off frequency (f_t) of 11.7GHz.

Following this K. Ueda *et al* demonstrated 100nm gate length FETs which achieved an f_{max} of 120 GHz [3.29]. This was closely followed by Russel et al. demonstrating 50nm gate length devices which showed cut off frequency f_t of 53GHz [3.30]. These publications remain the best RF performance from diamond technology with respect to f_{max} and f_t to date and show what can be achieved with the diamond material system.

M. Kasu *et al* began investigating the performance of hydrogen terminated diamond for microwave power applications and showed power output density of over 2W/mm at 1GHz for an FET with gate length 0.1µm and width of 100µm [3.31]. Emphasis in this publication was placed on the very small temperature increase of 0.5°C after operation, which was attributed to diamonds extremely high thermal conductivity allowing for effective heat dissipation.

Many groups moved on to further investigate the inclusion of alternative dielectric layers in the gate structure. To this end Koide *et al* investigated a number of alternative gate dielectrics, successfully demonstrating Hf_2O_3 as a gate dielectric [3.32], followed by ZrO_2 [3.33], TiO_2 and Y_2O_5 [3.34]. K. Hirama *et al* also succeeded in demonstration of Al_2O_3 as a gate dielectric[3.35].

At this time, work was well underway to replace the atmospheric adsorbate layer in diamond FETs. To this end M. Kubovic *et al* had shown that the adsorbates could be replaced with NO_2 resulting in greatly reduced sheet resistance of hydrogen terminated diamond [3.6] showing a comparison between an air exposed diamond FET and an NO_2 gas exposed diamond FET. An air exposed FET showed a maximum drain current of -235mA/mm, and after exposure to NO_2 this increased in magnitude to -425mA/mm. It was also reported that the on resistance decreased 1.7 fold and the extrinsic transconductance increased 1.5 fold. The effect of NO_2 exposure was quickly lost after re-exposure to normal atmospheric conditions, emphasizing the need for passivation of the H-diamond NO_2 material system.

Following this, K. Hirama *et al* demonstrated FETs based on exposing the H-diamond surface to NO_2 gas and encapsulating with Al_2O_3. In this publication maximum drain current of -1.3A/mm and intrinsic transconductance above 200mS/mm were reported for FET with gate length 0.4µm [3.22], the highest drain current and transconductance reported in diamond FETs to date. In this publication K. Hirama *et al* state that parasitic source and

drain resistances are not negligible and begin to dominate as the sheet resistance of the source-drain gap decreases, and these resistances dominate for source-drain gaps less than 2µm.

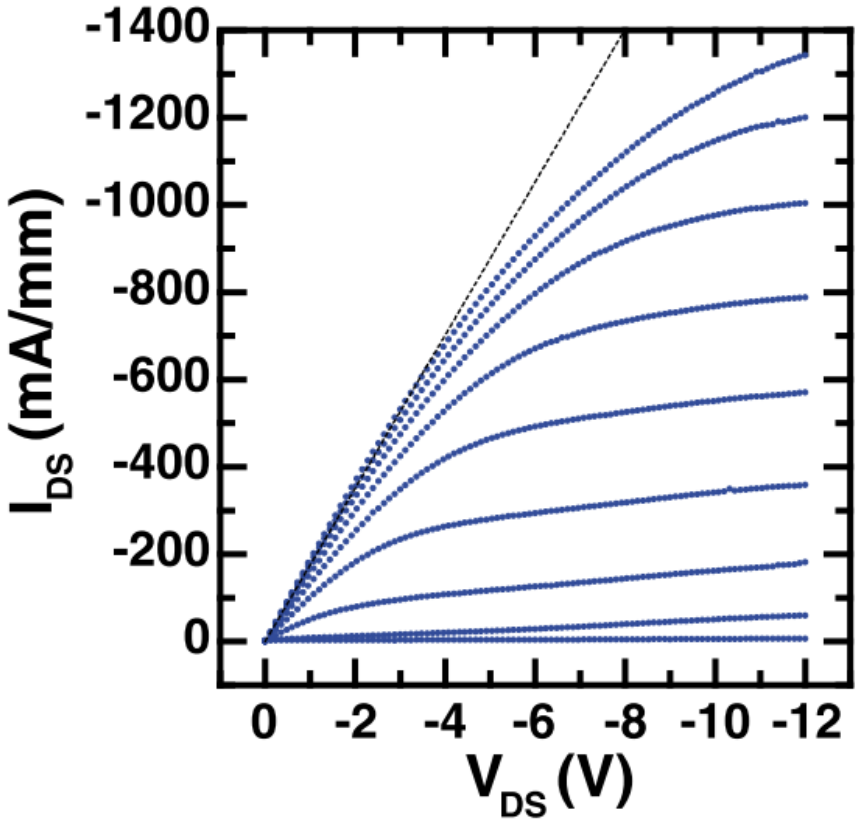

Figure 3.2.3 – Maximum drain current achieved for diamond FET by K. Hirama *et al. using encapsulated NO2 as surface transfer doping medium [3.22].*

A. Vardi *et al* showed the first FET results using a high electron affinity electron acceptor oxide material in the form of MoO_3 in a MISFET structure [3.36]. Very small drain current of -1.6mA/mm was achieved in this work, although this is likely due to the source and drain contacts being deposited on top of the surface transfer doping oxide leading to poor access to the 2DHG as can be observed *figure 3.2.4.*

Following this, MISFETs exhibiting much better DC characteristics using MoO_3 were reported by Z. Ren et al and Z. Jin-feng *et al* [3.37] [3.38]. Z Ren *et al* reported maximum drain currents of -100mA/mm, extrinsic transconductance of 35mS/mm and on resistance of 76.5Ω.mm, and also succeeded in showing that the MoO_3 FETs continued to perform at temperatures up to 200°C, showing an increase in drain current at 200°C compared to room temperature, however the FETs permanently failed at 250°C.

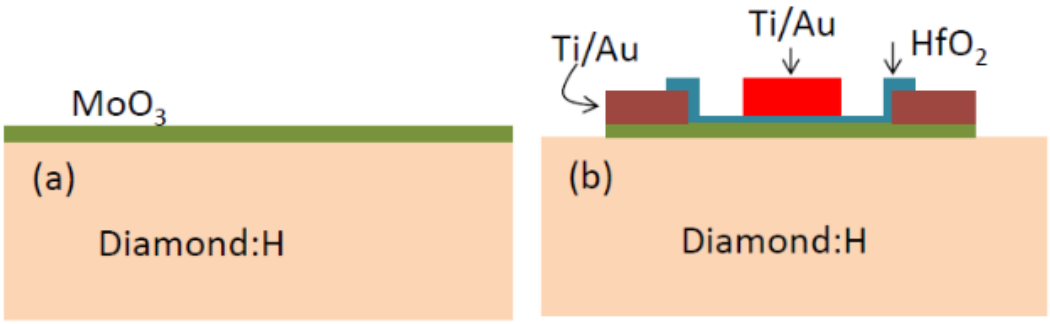

Figure 3.2.4 – First surface transfer doping oxide FET reported by A. Vardi *et al. Of note is the MoO_3 deposited under the source and drain contacts resulting in poor access to the 2DHG.*

Following publication of FETs utilizing MoO_3, C. Verona et al. succeeded in fabricating and demonstrating diamond MISFETs using the alternative surface transfer doping oxide V_2O_5 [3.39]. V_2O_5 was deposited between the source drain-gap under the gates of FETs as can be observed in *figure 3.2.5*. This publication included the highest drain current recorded at the time of publication for a surface transfer doping oxide FET at -275mA/mm with a transconductance of 80mS/mm. Atmospheric adsorbate MESFETs were also fabricated in this publication for comparison with V_2O_5 MISFETs of the same dimensions, comparison between the output characteristics can be seen in *figure 3.2.6*. This publication also detailed a reduction in maximum drain current of 11% after the FETs were heated above 130 °C.

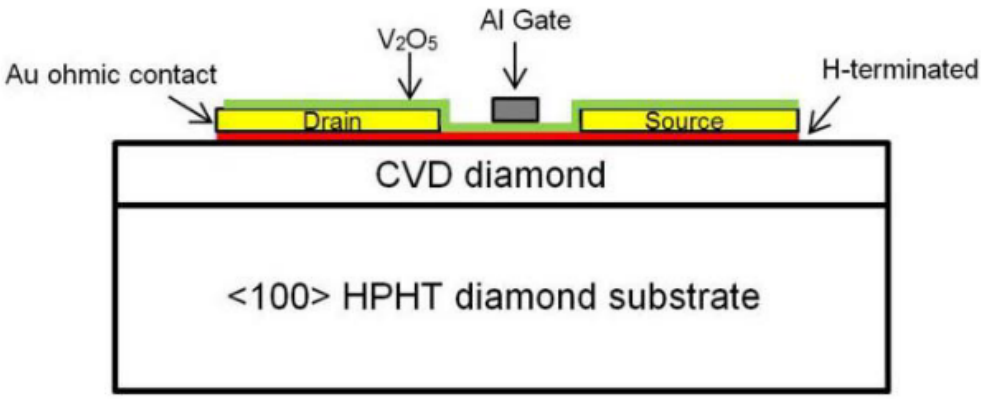

Figure 3.2.5 – MISFETs reported by C. Verona et al. The V_2O_5 has been deposited over the entire source-drain gap including under the gate.

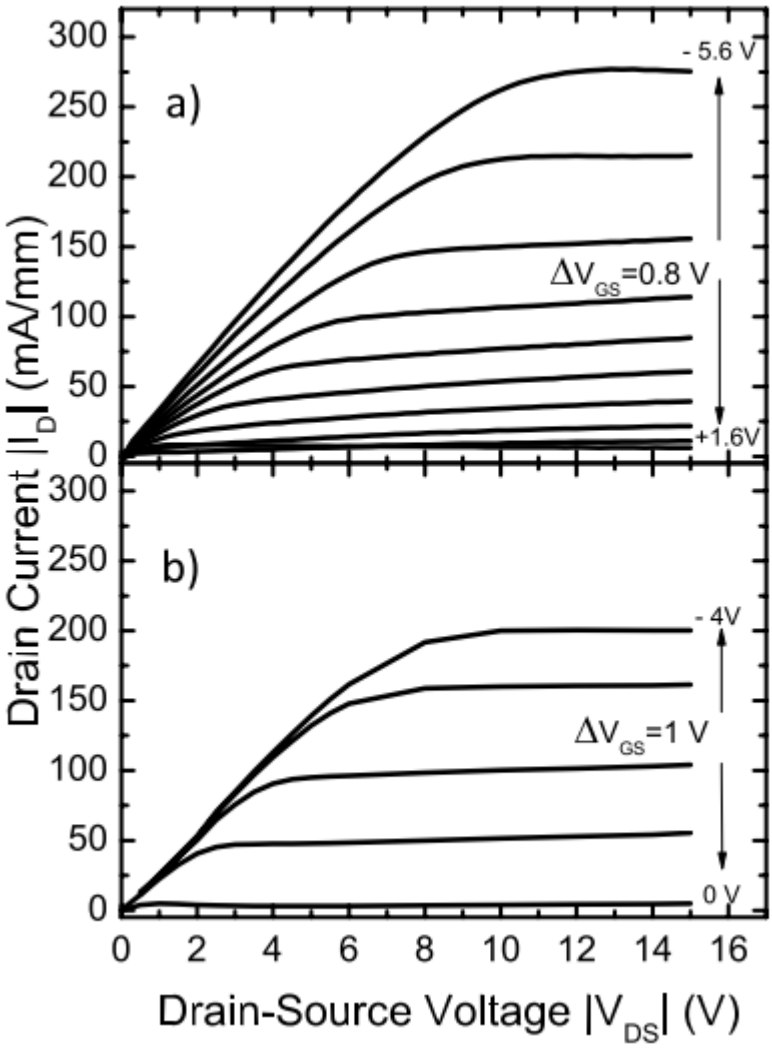

Figure 3.2.6 – Highest drain current achieved for surface transfer doping oxide FET (Top) compared to atmospheric adsorbate FET (Bottom)reported by Verona et al. using V2O5 as surface transfer doping medium [3.40] .

H. Umewaza *et al* showed over 1.5kV breakdown voltage by extending the gate drain gap of diamond FETs up to 40µm with a 20µm gate length using atmospheric adsorbates and Schottky gates formed using platinum metallization[3.41]. The breakdown field between the gate and drain was calculated to be 2.15 MV/cm, much less than the theoretical limit of 10 MV/cm for intrinsic diamond. This demonstrates that the diamond material itself is most likely not responsible for the breakdown mechanism, and emphasizes the need for engineering of the gate and ohmic metallization and interface with the diamond to maximize the breakdown voltage.

H. Kawarada *et al* also pursued Al_2O_3 deposition on hydrogen terminated diamond by ALD whereby Al_2O_3 was grown across the entire source drain gap of FETs and gate metal deposited on top [3.17]. Kawarada *et al* also included titanium carbide (TiC) ohmic contacts

in the published FET in an effort to reduce the ohmic contact resistance of diamond FETs. This work also succeeded in demonstrating a “hydrogen termination last” approach whereby the surface of the diamond is hydrogen terminated after the fabrication of the ohmic contacts. This allows the hydrogen termination to be unaffected by the processing of the ohmic contacts, an alternative to the “sacrificial” Au layer method used by competing research groups. Using Al_2O_3 as a passivation layer and to protect the p-type surface conductivity high temperature performance up to 400 °C was recorded. Very high breakdown voltage of above 600V with a gate drain gap of 7µm was also recorded with an Al_2O_3 gate oxide thickness of 200nm.

Following this H. Kawarada *et al* published another FET using ALD Al_2O_3 with a larger gate to drain distance of 9µm and achieved a breakdown of over 1000V[3.42], calculated as a breakdown field of 2MV/cm, comparable to the 2.15MV/cm previously reported by Umewaza *et al* These FETs were also operated between -263 °C and 400 °C showing a deviation in maximum drain current of 50% for a given gate voltage. The FETs in these publications showed poor on state performance with drain currents around 80mA/mm, lower than what has typically been reported for atmospheric adsorbate FETs.

From the discussed literature it is clear that substantial progress has been made in regards to realizing the potential of hydrogen terminated diamond FETs for high-power and high-frequency performance. This work explores hydrogen terminated diamond FETs using transition metal oxides MoO_3 and V_2O_5 to induce surface transfer dopants as these have shown potential for high maximum drain currents and transconductances. MoO_3 and V_2O_5 have also shown good stability at elevated temperatures. If these parameters could be improved, and combined with the high temperature and high voltage operation shown by FETs using ALD Al_2O_3, this could lead to exemplary high power performance and achieve high maximum drain currents, extrinsic transconductances, low on-resistances, high breakdown voltages, and good operation at elevated temperatures in the same FET.

For ease of reference a table showing the highest reported values for key figures in regards to high-power and high-frequency performance has been shown below in *table 3.2.1.*

Parameter (reported)	*Value*	*Surface transfer doping medium*	*Reference*
Highest I_{dmax}	*-1.3A/mm*	*NO_2 encapsulated with ALD Al_2O_3*	*[3.22]*
Highest g_m	*200mS/mm*	*NO_2 encapsulated with ALD Al_2O_3*	*[3.22]*
Lowest R_{on}	*4.4Ω.mm*	*NO_2 encapsulated with ALD Al_2O_3*	*[3.22]*
Highest breakdown voltage	*1.5kV (2.15MV/cm)*	*Atmospheric adsorbates*	*[3.41]*
Highest temperature performance	*400°C*	*ALD Al_2O_3*	*[3.17, 3.42]*
Highest f_T	*53GHz*	*Atmospheric adsorbates*	*[3.30]*
Highest f_{max}	*120GHz*	*Atmospheric adsorbates*	*[3.29]*

Table 3.2.1 – Highest reported values for key parameters in regards to high-power and high-frequency performance.

3.3 Boron Doped diamond FETs

Although the focus of this work is surface transfer doped diamond FETs it would be useful to compare the results achieved using atmospheric adsobates to those achieved by the competing diamond FET technologies for the high power high frequency space. Therefore, the current state of the art of boron doped diamond FETs will briefly be discussed.

The first demonstration of FETs utilising a boron growth layer was reported by Fujimori *et al* [3.43] who achieved limited drain current modulation and a maximum drain current of -150uA/mm at room temperature.

The highest drain current achieved for diamond FETs utilising boron delta doped layers was achieved by A. Aleskov *et al* who reported an FET with maximum drain current of -115mA/mm at -20V at 250°C[3.44]. As can be observed in *figure 3.3.1,* The FETs showed weak modulation of drain current at room temperature due to low boron activation as would be expected. The currents achieved are low compared to what has been achieved using

surface transfer doping hydrogen terminated diamond and the magnitudes of gate voltage required in order to turn the FETs off (30V) is very high.

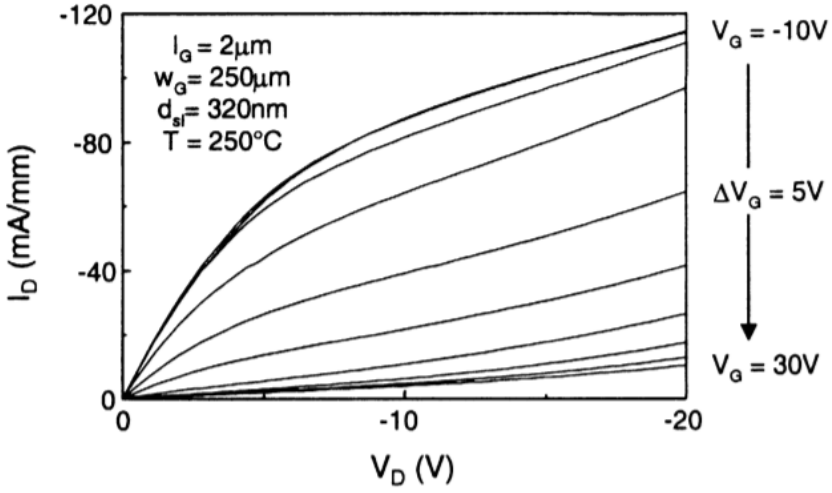

Figure 3.3.1 – Output characteristics of delta-doped boron FET reported by A. Aleskov et al at operating at 250°C.

The highest currents achieved at room temperature was achieved by E. Hajj *et al* using a recessed gate structure (which can be seen in *figure 3.2.2*) in order to gain better control of the delta doped layer. A current of -35mA/mm was achieved [3.45].

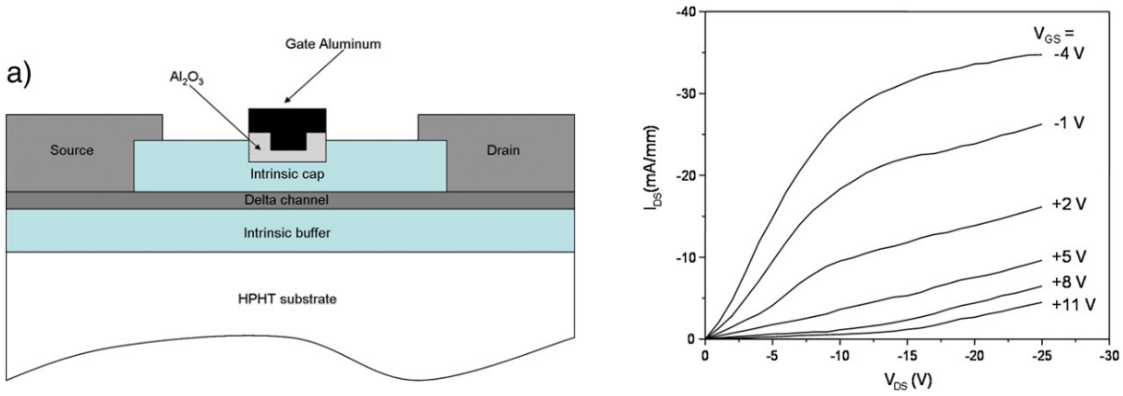

Figure 3.3.2 – FET structure (left) and output characteristics (right) of delta-doped boron FET reported by E. Haji et al.

The results discussed above for boron doped diamond FETs are encouraging for the exploration of the technology, however they pale in comparison to what has been achieved for hydrogen terminated diamond surface transfer doped FETs.

3.4 Chapter Summary

This chapter has explored the development of the surface transfer doping model and compared the results reported for various materials which can be used as a surface electron

acceptor material on H-diamond for transfer doping. From the discussed literature it has been shown that surface transfer doping oxides, MoO_3, V_2O_5, WO_3, ReO_3 and encapsulated NO_2 provide the most promising routes for increasing the carrier concentration and high temperature stability of the 2DHG in H-diamond.

From the literature reported in the second sub chapter it can be seen that hydrogen terminated diamond based FETs have shown good characteristics for both power and RF devices. The maximum breakdown field achieved so far is 2.15MV/cm, although not yet approaching the intrinsic breakdown voltage of diamond (10MV/cm), this is encouraging. Maximum output current of -1.3mA/mm, and transconductance of above 200mS/mm has also been reported and far surpasses what has been achieved in delta doped diamond FETs. This technology has also shown promising high frequency performance of f_T of 120GHz and f_{max} of 53GHz. Operation at elevated temperatures has also been reported with small deviation in maximum drain current observed in FETs at temperatures up to 400°C for Al_2O_3 MOSFETs. These characteristics demonstrate the potential diamond has for operating in the high power space at elevated temperatures.

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4. Fabrication and process flow

Fabricating small scale electronic devices on hydrogen terminated diamond can be a challenging endeavor due to the sensitivity of the hydrogen terminated diamond surface. As discussed in chapter 2, the mechanism which is taken advantage of in this work as a charge transfer layer is hydrogen terminated diamond's 2DHG. As this 2DHG relies on the surface hydrogen termination and its interface with acceptor materials, the surface is very sensitive to fabrication processes.

The main fabrication techniques employed in nanofabrication for defining patterns on a substrate surface are photolithography, electron beam lithography (EBL) and nanoimprint lithography (NIL). In this work photolithography and EBL have been used exclusively so only these will be discussed.

In photolithography, a geometrical pattern is transferred onto a light sensitive polymer or "photoresist" by passing usually UV light through a photomask. The advantage of photolithography is that it is highly repeatable in short timescales, as once the mask is manufactured it takes a short amount of time to spin resist, expose and develop the resist. However the drawback of photolithography is the in-flexibility of the design once the mask is manufactured. The minimum feature size of patterns fabricated through photolithography available to the author is around 1 micrometer and is determined by a number of factors as will be discussed in this chapter.

During EBL a pattern is transferred onto resist by a beam of electrons incident on the EBL resist affecting the resist structure. The electron bombardment affects the polymer bonds, transferring a pattern onto the resist. EBLs main advantages are that it is highly flexible and has a much smaller minimum feature size compared to photolithography allowing for fabrication of smaller features. It is however more time consuming and expensive to perform alignment and exposure.

The processes for spinning and developing photoresists and EBL resists are de-facto identical so will be covered as one. The process of exposure differs and will be covered separately.

Resists can be either positive or negative. In a positive resist once it has been "exposed" the polymer chains are broken, this means a weak solvent can wash away the resist in exposed area with a minimal effect on the non-exposed regions. This works in the opposite manner for negative resists, where the bonds are strengthened by exposure and the exposed areas

remain after development. For this work only positive resists have been used and thus only positive resists shall be discussed in this chapter.

Although this chapter provides an explanation of each processing method used in this work, the full processing details and process sheets can be found in appendix A.

4.1 Substrate preparation

In order to provide a pristine surface for hydrogenation, and to remove any non-diamond graphic carbon from the surface of the diamond, a two-step acid clean in employed. The first step of the process is to submerge diamond samples for 10 minutes in a boiling 1:1 mix of Nitric Acid (HNO_3) and Hydrochloric acid (HCl). This step is intended to remove surface contamination and graphic non-diamond carbon from the surface of the material. The next step is to ensure the surface is fully oxygen terminated, to achieve this the diamond sample is submerged for a further 10 minutes in a boiling 3:1 mix of Sulphuric Acid (H_2SO_4) and Nitric Acid (HNO_3).

4.2 Hydrogen termination

As discussed previously, for the formation of a 2DHG one must have a hydrogen terminated diamond surface to create a negative electron affinity allowing electrons to leave the diamond surface if a suitable “acceptor” layer is available.

In this work a high power hydrogen termination process was used which was developed in collaboration with, and carried out by, colleagues at the Université Paris 13 as reported in [4.1]. In order to replace the oxygen termination of the diamond surface with hydrogen, the diamond surface is treated with a 2.6KW hydrogen microwave plasma under ultra-high vacuum (UHV) and the substrate is heated to 650°C. This temperature is required to break the oxygen-carbon bonds of an oxygen terminated diamond surface. Once these bonds are broken it becomes energetically favorable for the “dangling” carbon bonds to be satisfied by atomic hydrogen generated by the hydrogen plasma.

4.3 Substrate cleaning

The first step in any fabrication process is to ensure you have a clean surface on which to fabricate. This is a simple process which involves placing a substrate into a beaker of acetone and placing this into an ultrasonic water bath. The acetone acts to remove any grease or particulate adsorbed to the surface of the substrate. The ultrasonic water bath aids in this process by mechanically agitating the substrate. After this the substrate is thoroughly rinsed

in Isopropyl Alcohol (IPA) to remove any residual acetone. Care must be taken to ensure the substrate does not dry with any acetone on the surface as this can be hard to remove and impede later fabrication processes.

4.4 Resist spinning

Resist spinning is the process of spreading a uniform thin layer of resist across a substrate for later exposure and development. After the resist is placed on the surface of the substrate by pipette, the substrate is spun at high speeds and the centrifugal force spreads a small amount of the viscous material evenly across the surface of the substrate. The resist simultaneously begins to evaporate its solvent component and flies from the edge of the substrate. The thickness of the film is dependent on the speed at which the substrate is spun and the viscosity of the resist. After spinning the resist is "baked" either on a hotplate or in an oven in order to evaporate the remaining solvent from the resist. For this work all EBL resist was baked at 120°C in an oven, and photolithography resists S1805 and LOR5A were baked on hotplates at 115°C and 150°C respectively.

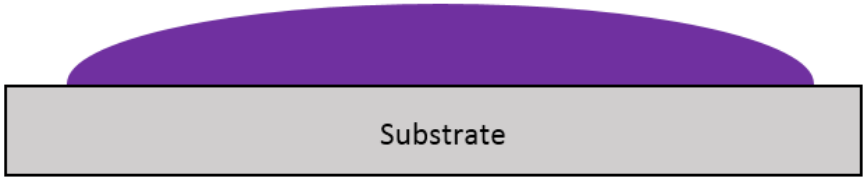

Fig 4.4.1 – Substrate after resist is deposited on surface of substrate.

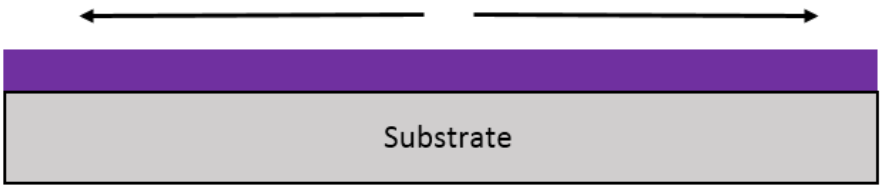

Fig 4.4.2 – Substrate and resist after spinning showing planarization of resist on substrate.

A single layer of resist can be used as a mask for etching. However, if one desires to deposit another material on top of the substrate it is advantageous to use a bi-layer of resist in a process known as "lift-off" which will be discussed in detail later in this chapter.

4.5 Photolithography exposure

Photoresist is usually a long chain polymer which can be affected by UV light. For positive photoresists the polymer is weakened by exposure to the UV light and the exposed areas can be removed by a weak solvent. The wavelength of the light used must be correct for absorption by the resist. Below in *figure 4.5.1* a photolithography mask schematically shown in contact with a substrate including resist spun into the surface. It can be seen that in this case the mask is in direct contact with the resist layer. The wavelength of the light source will primarily determine the minimum critical feature size during photolithographic development. Minimum critical feature size can also be affected by any gap between the resist and photomask as well as exposure dose (too low a dose leads to greater development time and therefore the "dark erosion" of the resist during development), as well as diffraction of light through the mask under the "dark" areas. In the semiconductor industry greatly smaller feature sizes than reported in this work, down to 10s of nanometers, can be achieved using processes such as projection lithography and extreme UV lithography [4.2].

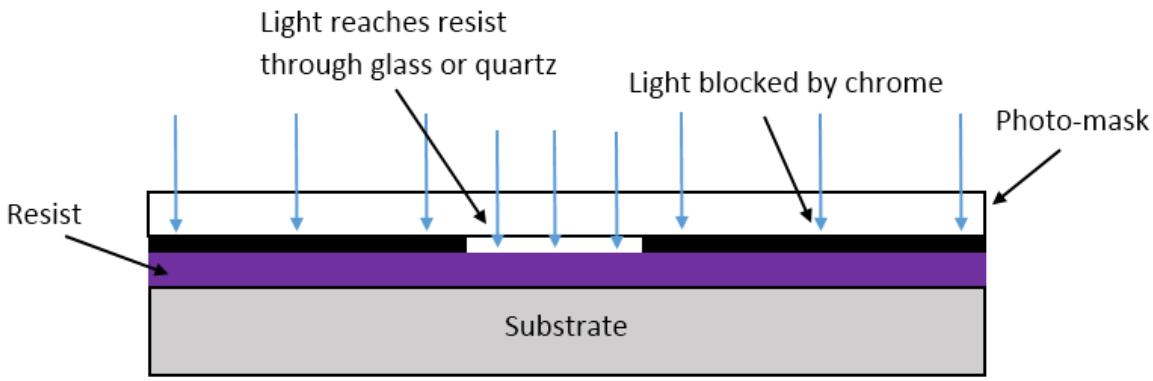

Fig 4.5.1 – Photomask in contact with resist during UV exposure. UV radiation reaches resist through glass area and is blocked by chrome areas.

Photolithographic exposure reported in this work was performed using a SUSS MICROtech Mask Aligner 6 (MA6).

4.6 EBL exposure

In regards to electron beam lithography the resist is affected by incident electrons which weaken or strengthen polymer bonds dependent on whether the resist is negative or positive.

In order to produce patterns, a thermally assisted field emission source is used to produce an electron beam which is accelerated by the anode. The beam emerges from the electron gun and passes through two sets of magnetic deflection coils which can tilt and shift the

alignment incident on the substrate. The divergence of the resulting beam is limited by the apertures present in the column, these can be changed and a range of different available apertures allow the spot size and current density to be optimized for different patterns. The final pattern is defined by the main and subfield deflection coils. The pattern generator generates analogue drive signals which deflects the electron beam in order to produce the pattern defined by the user. The beam can be switched on and off by the beam blanker within the coil.

For EBL the minimum feature size is primarily determined by the minimum "spot" size the electron gun can produce, which is in turn determined by the wavelength of electrons emitted. It is also determined by the amount of electron backscatter, which is itself dependent on the accelerating voltage.

When performing EBL it is important to account for the conductivity of the substrate. An insulating substrate can lead to a build-up of charge on the surface as an EBL pattern is written. This may lead to the beam being deflected by the charge build up and features not writing correctly. In this work the bulk of diamond substrates used are highly insulating, thus a layer of 10nm of aluminium was deposited on top of spun resist to act as a charge depletion layer (CDL)[4.3]. Although this layer may result in marginally increased beam dispersion it is not thought to have an effect on the size of features achieved in this body of work.

EBL reported in this work was performed using the University of Glasgow's Vistec VB6, a simplified representation of which can be seen in *figure 4.6.1.*

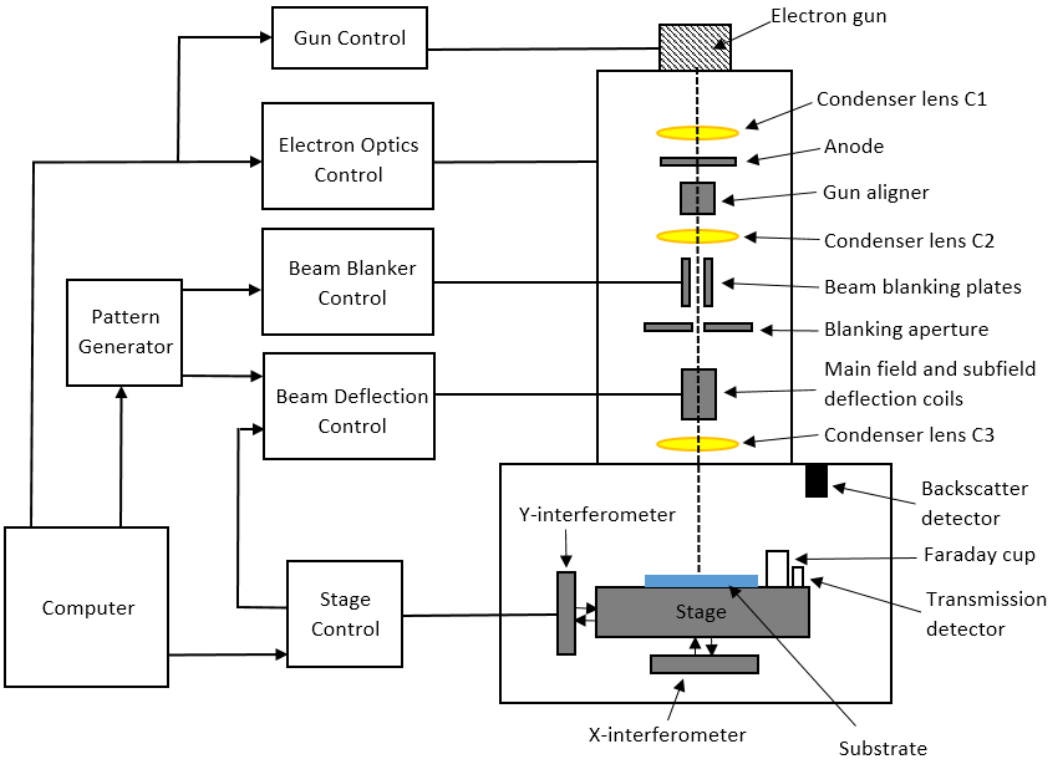

Fig 4.6.1 – Simplified representation of Vistec VB6. Information from [4.4].

4.7 Alignment

In order to form multiple patterns for different fabrication steps on the same substrate alignment of lithography layers must be employed. For photolithography this takes the form of optical alignment, whereby shapes present on the substrate surface are optically "aligned" with matching shapes on the mask in order to ensure the layers are aligned properly.

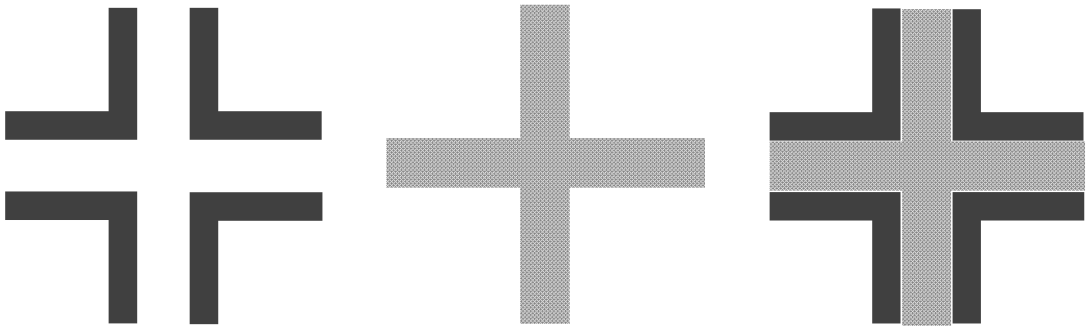

Fig 4.7.1 – Example of photolithography alignment, feature on photomask (left), feature on substrate (center), features after optical alignment (right).

With regards to EBL alignment is handled by the controlling computer. The VB6 scans the surface with a marker location algorithm and detects backscattered electrons. The VB6 can detect the signal from the markers as they are defined either by etching or deposition of reflective metals on the substrate surface. The VB6 uses these markers as reference points for ensuring the different layers are written with the correct alignment. Typically "global" markers can be sufficient for smaller patterns, however for large patterns more markers can be added to smaller divisions of the pattern called cells ensuring that each cell is correctly aligned.

4.8 Resist development

After exposure, resist can be developed in a solvent. In the case of positive resist this results in the regions which were exposed being removed. In an ideal case, resist development should be binary, meaning the exposed regions should be completely cleared away after development and the non-exposed regions should be completely intact. This is in reality impossible to achieve as the development solution will usually have a small effect on unexposed areas, and the solvent will not usually remove all of the resist in the exposed areas.

The development time will be determined by a number of factors, including the concentration and temperature of the development solution, dose delivered during exposure, and thickness of the resist.

Resist left behind after development in the exposed area is known as "resist residue". This residue can cause issues such as metallization failing to adhere to the substrates surface or poor access to underlying material for etch processes. This residue can be removed after development by a low power oxygen plasma or "ash"[4.5]. Care must be taken to not allow the oxygen plasma to come into direct contact with the surface of the hydrogen terminated diamond as this can remove the hydrogen termination.

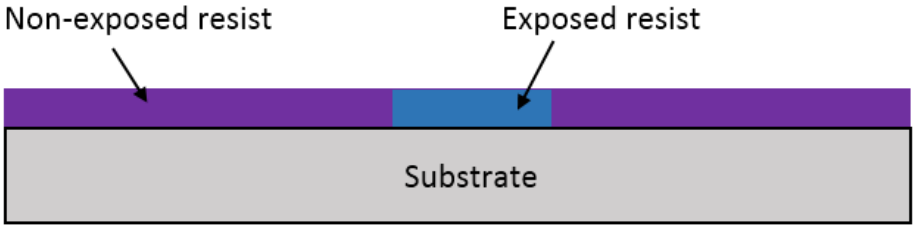

Fig 4.8.1 – Positive resist after exposure to radiation.

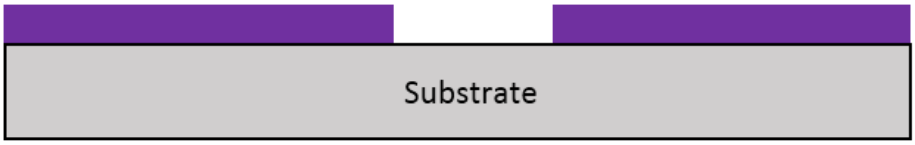

Fig 4.8.2 – Positive resist after exposure and subsequent development.

4.9 Lift-off metallization

In order to form metal contacts on a semiconducting substrate the method of lift-off can be employed. To this end 2 resist layers must be spun and are referred to as a "bi-layer". In order to do this one layer is spun onto the substrate and baked in order to remove solvents, before the second layer is spun onto the substrate and baked in order to remove solvent. The full photolithography lift-off process can be seen below in *figures 4.9.1 – 4.9.5.*

When applied to photolithography a special lift-off resist (LOR) can be used in a bi-layer with conventional photoresist. The photoresist is exposed and developed as usual, this development does not affect the lift off resist underneath. After this another developer (which has no effect on the conventional resist) is used to develop the LOR and produce un "undercut" beneath the conventional resist as can be seen below in *figure 4.9.3*. This undercut means that the metallization layer is non-continuous and a solvent or stripper can access the resist underneath the metallization in order to dissolve it.

A bi-layer of E-beam resist is created in a slightly different manner. The bi-layer consists of 2 different concentrations of resist with different molecular weights. The bottom layer is more sensitive to electron beam exposure, this results in a larger feature size being developed compared to the top layer producing a similar "overhang" as seen the in photolithographic processing detailed below.

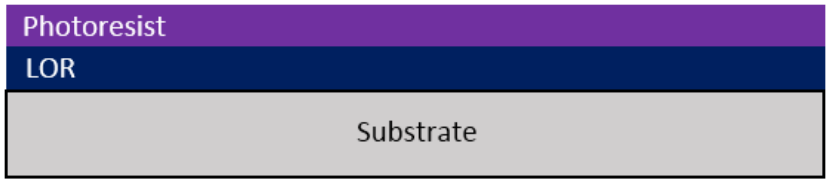

Fig 4.9.1 - Resist "bi-layer" after spinning and baking onto substrate.

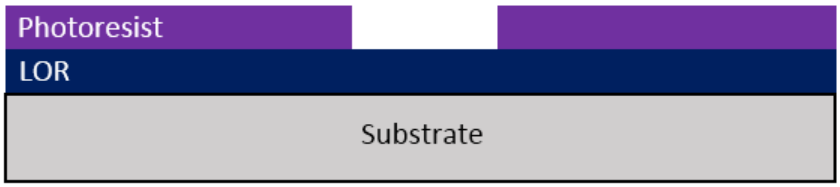

Fig 4.9.2 - Resist "bi-layer" after exposure and development of top layer.

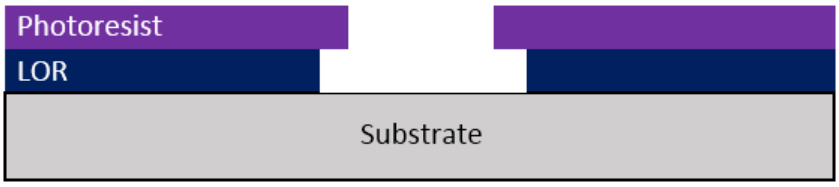

Fig 4.9.3 - Resist "bi-layer" after exposure and development of top and bottom layers.

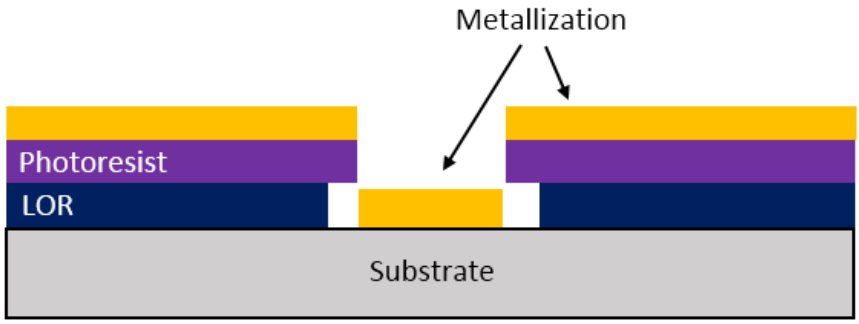

Fig 4.9.4 - Resist "bi-layer" after deposition of metal.

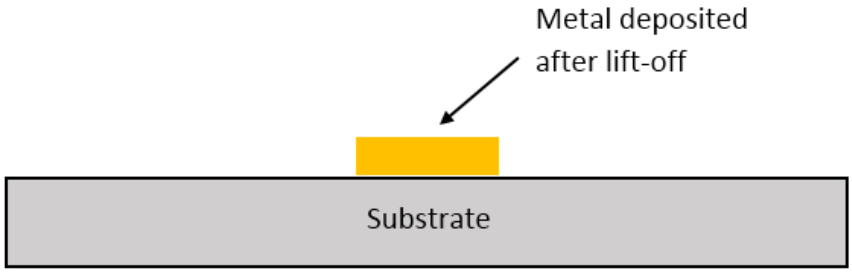

Fig 4.9.5 - Metal remains on substrate after resist stripped from substrate surface.

4.10 Etching

In order to remove materials from the substrate surface etching must be employed. In an etch process a chemical reaction occurs with the material to be removed and the material is removed with the resulting reactant. The two types of etching are "dry" and "wet" etching.

In a wet etching process a "wet" chemical solution is allowed to make contact with the material to be removed. In this way a reaction can occur between the solution and the material to be removed and the resulting reactant is transported from the substrate surface.

Wet etching can be highly selective and is usually isotropic depending on the crystallinity of the material being etched and the etch chemistry. Potassium iodide (KI_2) has been used in this work as a "wet etch" to remove gold.

In the process known as "dry" etching the material to be removed is exposed to a bombardment of ions (usually a plasma of reactive gases) that removes portions of the exposed material. The resulting reactant is pumped out of the chamber by vacuum. Dry etching is particularly useful for removing materials which are non-reactive to wet etchants. Dry etching is more repeatable than wet etching and can be controlled more easily, however dry etching is less selective and can lead to damage to areas where removal is not intended. Dry etching can also be anisotropic which can be very useful for producing high aspect ratio features. Cl_2+Ar and O_2+Ar chemistries have been used in this work to etch the surface of the diamond prior to hydrogen termination in order to remove sub surface damage and produce a smooth surface[4.1]. Low power oxygen etching has also been used to remove resist residue from the surface during processing in a process known as "ashing".

4.11 Pattern Generation

In order to produce a pattern which is to be transferred onto the substrate it initially must be designed in computer aided design (CAD) software. Tanner Layout's L-edit software was used to produce the lithography designs in this body of work.

For photolithographic processing the produced design was provided to an external company in the form of a GDSII file who produced a photomask to the specifications provided.

For EBL, the GDSII file is exported locally to "BEAMER" software which interprets the file and produces a pattern in .vep format. BEAMER fractures the design into geometric shapes which can be interpreted by the pattern generator of the VB6. After this the .vep is transferred to the "Belle" software which allows the user to determine the spot size, dose and beam step size as well as the alignment of multiple layers of EBL patterns.

4.12 Physical Vapour Deposition

Physical Vapour Deposition (PVD) is a vacuum deposition technique whereby a thin film of material can be deposited onto a substrate. These processes involve a solid phase material being converted into vapour phase and then condensed back into a solid thin film deposited on the desired surface. For this work the primary technique was evaporation deposition, and of this category two subsets were used; electron beam evaporation and thermal evaporation.

The quality of vacuum is very important in these processes as any excess gaseous specimen in the chamber can lead to non-uniform or contaminated films.

In both of these systems the deposition is monitored using a Quartz Crystal Microbalance (QCM). The microbalance has a resonant frequency which is monitored by the deposition system. When material is deposited on the crystal its resonant frequency is dampened due to the increase in mass. Sensitivities to changes in mass in the range of 10^{-8} g/cm^2 can typically be achieved[4.6]. This change in mass can be used to calculate the thickness of material deposited and the rate of deposition on the known area of the QCM. This is very important as the rate of deposition can affect the material properties of deposited films and controlled thickness of deposition is important for fabrication.

Thermal Evaporation deposition

As can be observed in the diagram in *figure 4.12.1*, during thermal evaporation the target material is heated until vaporization of the material occurs and it deposits on the substrate located above the vaporized material. The target material is usually located in a resistive element "boat" which is heated by current passing through it. The magnitude of current can determine the temperature of the material to be deposited and hence the deposition rate. For this work thermal evaporation was used for deposition of surface transfer doping oxides on the surface of diamond substrates.

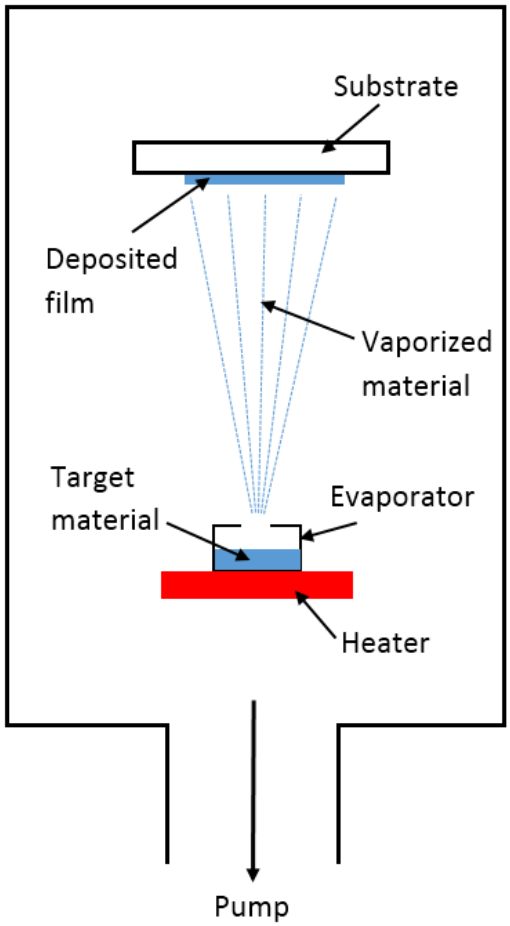

Figure 4.12.1 – Thermal evaporation system.

Electron Beam Evaporation deposition.

As can be observed below in *figure 4.12.2*, during electron beam evaporation electrons are accelerated towards the target material, on contact with the material the kinetic energy of the electrons is lost and becomes thermal energy. Once the target material is at sufficient temperature the material will enter the vapour phase and can coat the substrate located above the target. For this body of work e-beam evaporation was primarily used for deposition of metals and alumina.

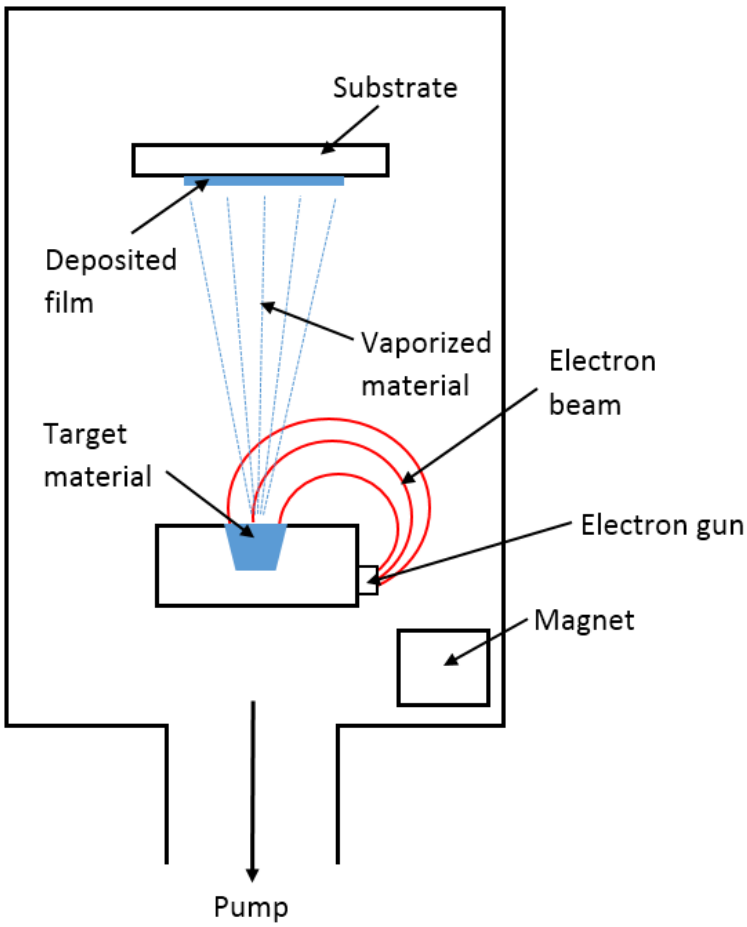

Figure 4.12.2 – Electron beam evaporation system.

4.13 Physical characterization

When fabricating microelectronics it is important to have the capability to characterize and inspect the physical material qualities and the devices at each stage of fabrication. These tools are indispensable during process development.

Optical microscopy

Optical microscopy is a form of conventional microscopy whereby a real image is magnified by lenses to appear larger to the eye. This is useful for inspecting devices made in the dimension of 10s or 100s of micrometers. The resolution of optical microscopy is limited by the diffraction limit of the microscope system. Therefore, if there is a requirement to investigate features smaller than the micrometer scale an alternative method must be employed. Typically optical microscopy has been used in this work in order to inspect the substrate during fabrication steps.

Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) is a technique which allows imaging by bombarding a surface with a "scanning" electron beam. A detection signal is produced which can provide information about surface morphology and topography. The accelerated electrons incident on the surface dissipates energy as a variety of signals, such as secondary electrons which can be used to create SEM images, and photons which can be used for XPS analysis. SEM is very useful for characterizing 2 dimensional structures made in the nanometer scale as it has very good spatial resolution down to 10s of nanometers. The spatial resolution of an SEM is limited by the electron beam spot size which itself is reliant on the wavelength of electrons produced by the electron beam source.

As in EBL exposure, an insulating substrate can cause issues with charge build up when using SEM resulting in disturbed signals and imaging. In order to reduce charge build up the substrate can be coated in a thin layer of metal, typically 5-10 nanometers thick. Due to the insulating nature of the substrates used in this work, and concerns regarding the effect of electron beam exposure to the hydrogen termination of the diamond surface, SEM imaging would usually only be performed at the end of a substrates life. In this work the SEM used is a Hitachi SU8240.

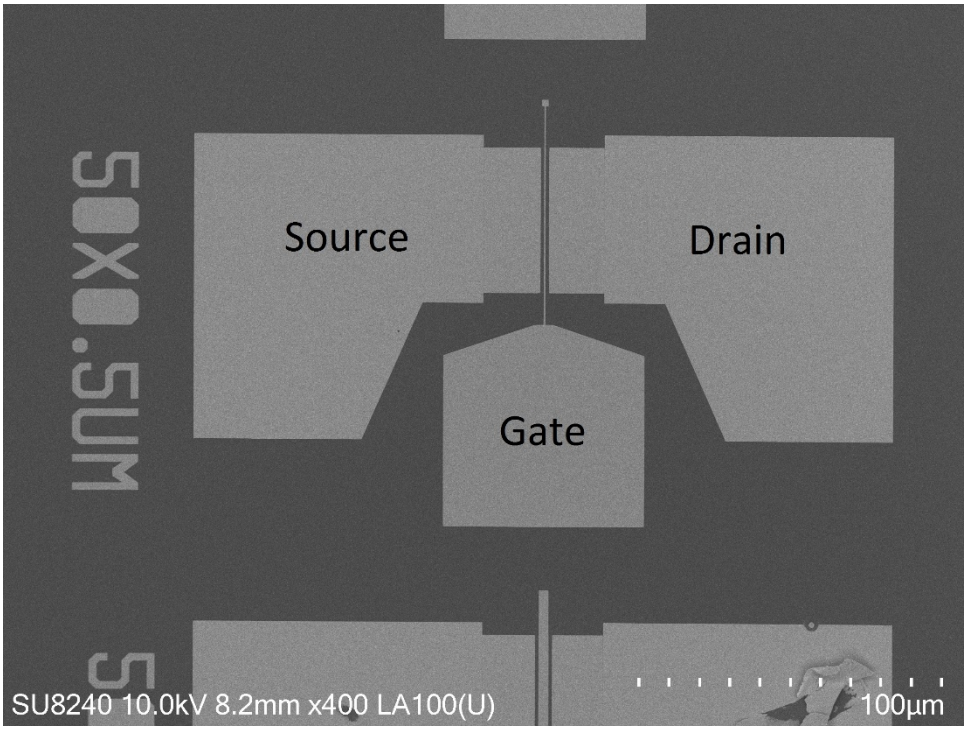

Figure 4.13.1 - Example SEM image of a single finger DC FET fabricated in this work.

Stylus Profilometer

Stylus profilometers work by dragging a stylus or tip across the surface of a material, giving the ability to measure surface roughness and thin film thickness. This can be a very useful tool for determining the thickness of spun resist films or confirming thicknesses of deposited thin films of metals or oxides. Profilometers have good vertical resolution however lack spatial resolution of an SEM, or the greater vertical resolution of an AFM. Due to this stylus profilometers are useful for quick measurements of larger feature sizes. (100s of nanometers in depth). Typically the Dektak has been used in this work to verify resist thicknesses. The stylus profilometer used in this work is the Bruker Dektak XT.

Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a physical characterization method whereby a probe is scanned across the surface of a material or substrate which provides detailed topographical information. The tip applies a small force to the material to remain in intimate contact and follow the topography of the material. As the tip is displaced the vertical movement is tracked by a laser and photodiode to provide a signal which can be interpreted as a topographical 3D map of the surface. AFMs have submicron resolution and are not subject to an optical diffraction limit. AFMs are not useful for measuring deep trenches as the small cantilever size means the tip cannot reach into a high aspect ratio trench. Typically, in this body of work the AFM has been used to verify the thickness of deposited metals and the roughness of the diamond surface. The AFM used in this work is the Bruker Dimension Icon AFM.

4.14 Hydrogen terminated diamond FET Process Flow

For this work there have been 6 main steps in completion of FETs after the hydrogen termination of the substrates performed by our collaborators in Paris. Up to step five, which can be seen outlined below in *figure 4.14.1*, results in the production of an atmospheric adsorbate doped FET. An additional step is shown in *figure 4.14.2*, which shows the deposition of a surface transfer doping oxide over the completed FET. Each fabrication step is covered in detail in this subchapter, and uses techniques explored in the previous subchapters. The inclusion of surface transfer doping oxides into hydrogen terminated diamond FET technology is the main focus of this body of work. The full process sheets for the processes are shown in appendix A.

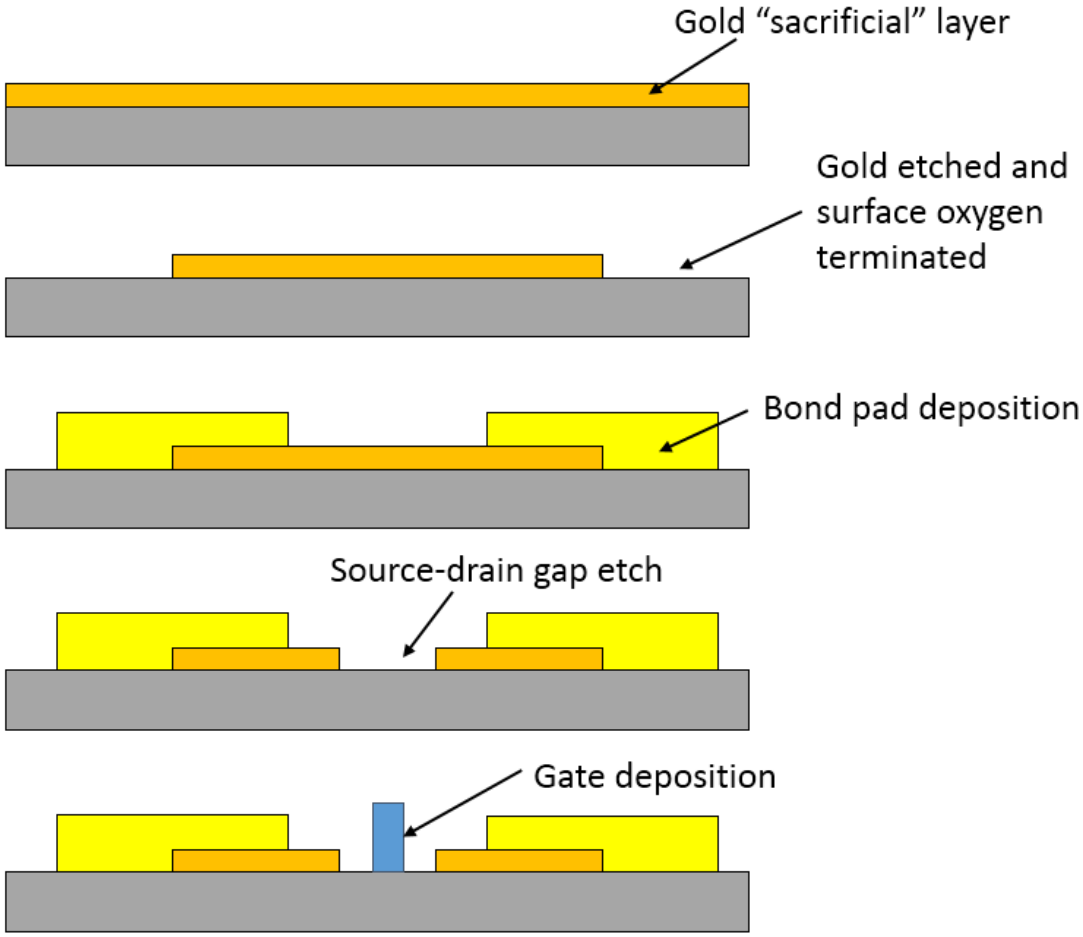

Fig 4.14.1 – Shows standard process flow used in this work to produce FETs up to “atmospheric” FET level.

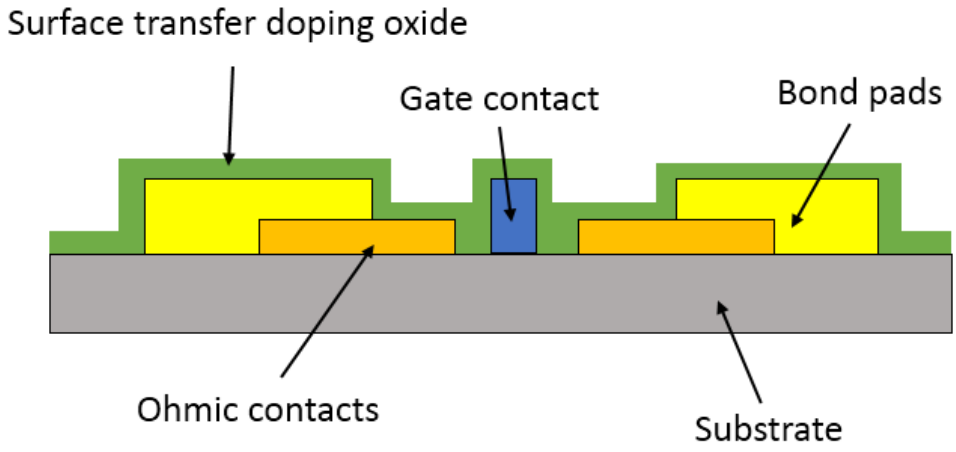

Fig 4.14.2 – Example FET after surface transfer doping oxide deposition with key elements highlighted.

Substrate preparation

As outlined in the previous subchapters, before fabrication the diamond substrates are submerged in a 2-stage acid boil before being hydrogen terminated by exposure to a high power microwave hydrogen plasma. Following this the substrate is cleaned in solvents to remove any residue or grease build up.

Gold Sacrificial layer deposition

The first step in hydrogen terminated diamond FET fabrication is to deposit a gold "sacrificial layer" which will later form the ohmic contacts of fabricated devices. The layer also serves to protect the hydrogen termination of the diamond surface during fabrication and is carried out as soon as possible after hydrogen termination This layer is formed by depositing 80nm of gold by electron beam evaporation through a shadow mask using a Plassys MEB400 electron beam evaporation system.

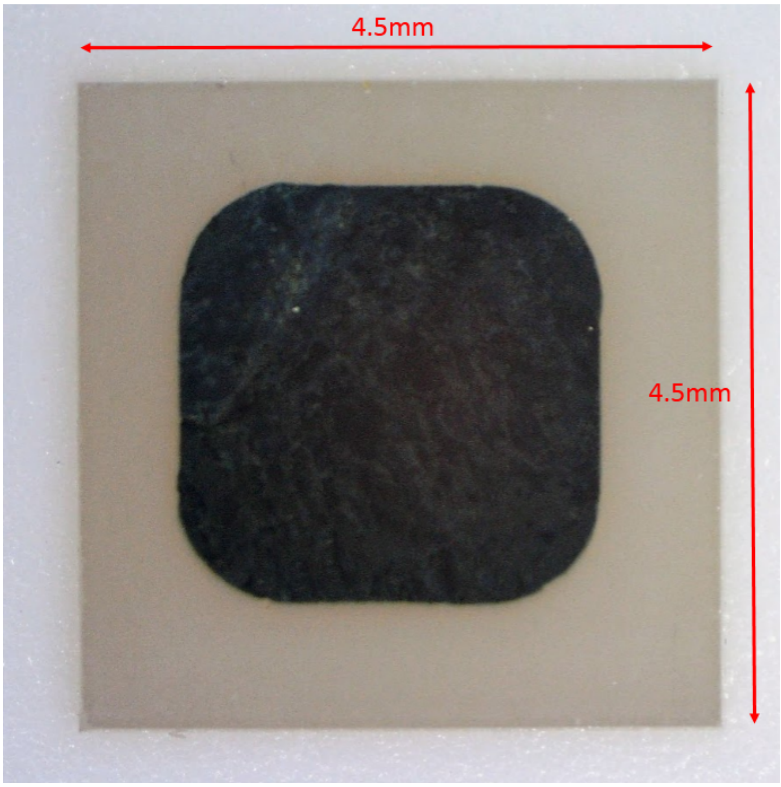

Fig 4.14.3 – Gold sacrificial layer deposited on hydrogen terminated diamond substrate showing dimensions of typical substrate.

Markers

In order for multiple layers of lithographic processing to take place on one sample, alignment is needed. For this purpose metal "markers" are deposited on the diamond surface using electron beam lithography and a metal lift-off processes. A bi-layer of poly methylacrylate

(PMMA) is used to lift off then metallization to define markers. The metallization for markers used in this work is 20nm of Titanium and 80nm of Gold. Titanium allows the marker layer to adhere better to the diamond surface, and the golds high reflectivity allows the VB6 or MA6 operator to find the markers more easily for aligning later layers.

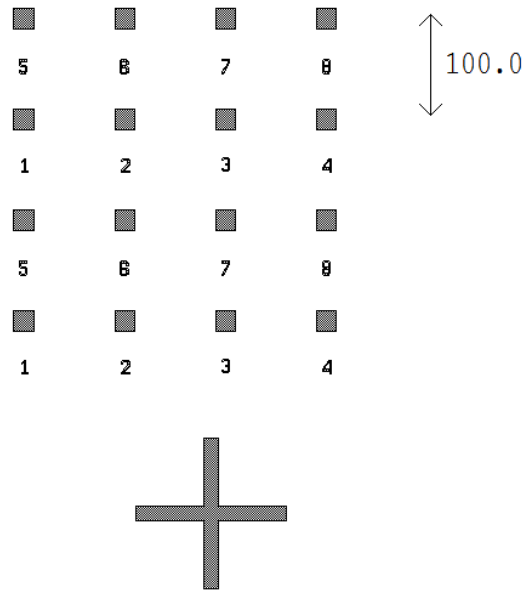

Fig 4.14.4 – EBL markers and cross for reference and alignment in L-edit software. Scale indicates 100µm.

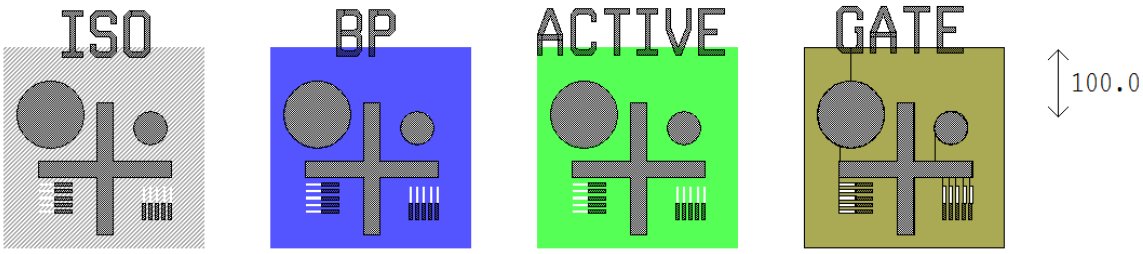

Fig 4.14.5 - Photolithography markers in L-edit software (Dark Grey), other layers for alignments are coloured. Scale indicates 100µm.

Isolation

The next step of diamond device fabrication is to "Isolate" each device individually so current is confined to the channel of each device. In order to achieve this the 2DHG must be removed in areas it is not desired. The previously deposited sacrificial layer forms the ohmic contact regions of the devices after a wet etch defined by photolithography and the etched area is referred to as the "Isolation" region. After the gold etch the diamond surface is

exposed to a low power oxygen plasma which removes the hydrogen termination on the exposed surface leaving it oxygen terminated. This can be seen in *figure 4.14.6* where the hydrogen termination is maintained under the remaining gold and the exposed areas are oxygen terminated. The oxygen termination results in no formation of a 2DHG isolating each device.

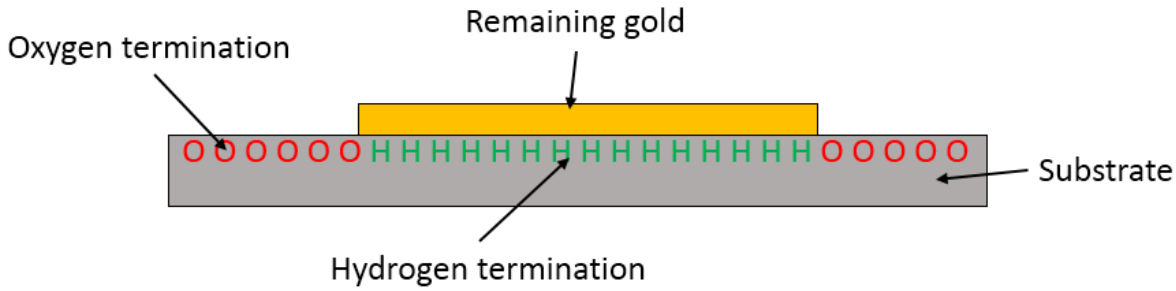

Figure 4.14.6 – Shows gold remaining after etch of sacrificial layer, H-termination maintained under remaining gold after oxygen etching, whereas etched areas exposed to oxygen plasma are now oxygen terminated.

For this process S1805 is spun onto the substrate and given a soft bake on a hotplate to remove solvent. After the exposure of the correct pattern using MA6 the resist is developed and the area is exposed to an oxygen plasma to remove all resist residue. The gold etch is then performed. The areas which were exposed and developed now have exposed gold, the substrate is placed into a beaker containing a solution of 1:4 Potassium iodide (KI_2) gold etch and reverse osmosis (RO) water for 30seconds. This removes the gold and undercuts the resist by approximately 1 micrometer. After this stage the substrate can be exposed to oxygen plasma to remove the hydrogenation of the surface effectively isolating each structure on the substrate.

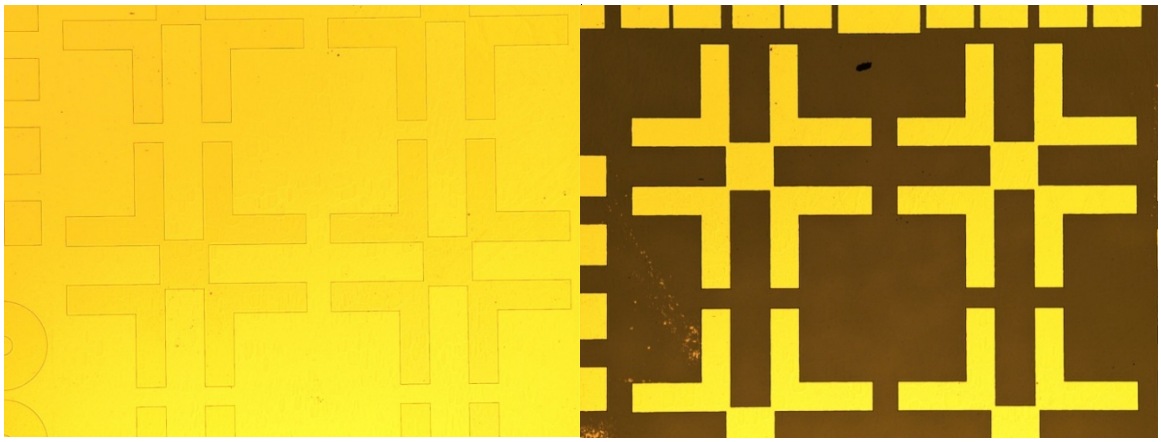

Figure 4.14.7 – Isolation lithography (left) and after KI_2:RO etch (right)

Bond pads

Although the gold "sacrificial" layer forms the ohmic contact regions of the devices, this layer can easily delaminate from the diamond surface. In order to form more robust contacts larger pads formed of 20nm of Titanium and 200nm or Gold are lifted off which ride up onto the ohmic gold. The majority of the bond pads are deposited on oxygen terminated areas of the diamond surface, which also improves the adhesion of the metal to the diamond surface. The titanium is much more robust than the gold and promotes adhesion of the metallization on the diamonds surface. The thicker layer of gold provides another more robust region to probe minimizing damage to the contact metal.

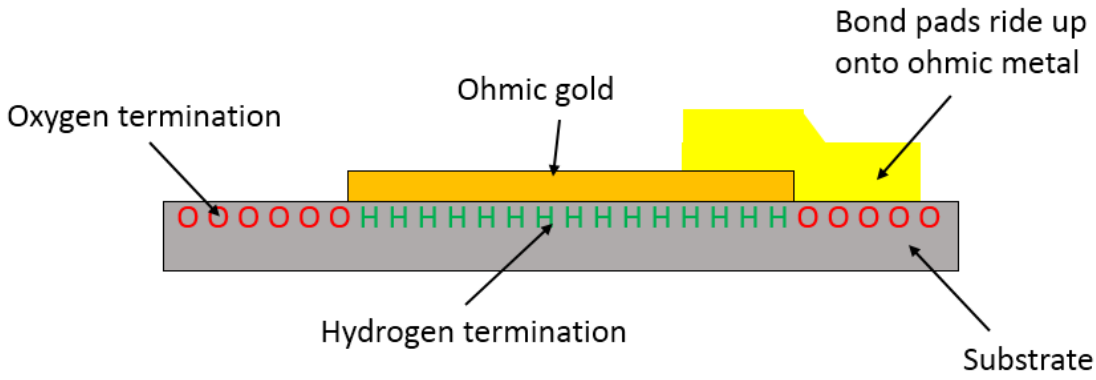

Figure 4.14.8 – Representation of bond pad metal riding up onto ohmic gold metal, showing hydrogen and oxygen terminated areas.

This process consists of a bi-layer of S1805 resist on top of LOR5A "lift-off" resist. After the resist has been patterned using the MA6 it is developed, producing an undercut bi-layer of resist. Following an oxygen ash to remove resist residue, 20nm of Titanium and 200nm of Gold is deposited by electron beam vapour deposition and lifted-off.

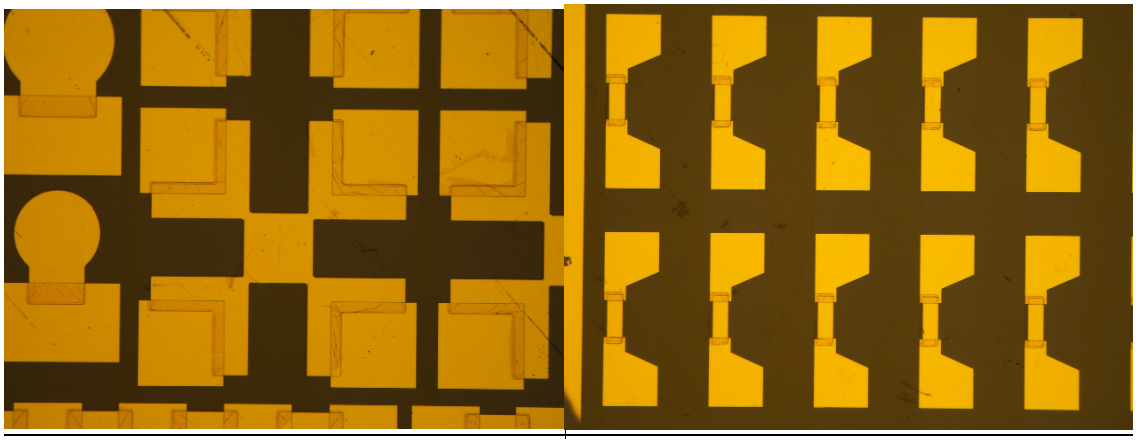

Figure 4.14.9 – Bond pads after lift-off, VDP structures (left) and FETs (right).

"Active" device region

As well as forming the ohmic contact regions of the devices the gold sacrificial layer serves to protect the diamond surface during fabrication. In order to fabricate non-FET test structures such as TLM and VDP structures, regions of gold must be etched to expose the hydrogen terminated diamond surface and form the separated ohmic contacts for these structures.

For this process S1805 is spun onto the substrates and given a soft bake to remove solvent. After being exposed to a pattern using the Mask Aligner 6 (MA6) the resist is developed. The resist in the area to be exposed to oxygen plasma is removed by the exposure and development. The gold etch is performed. This etch is a wet etch process. The areas which were exposed now have exposed gold, the substrate is placed into a beaker containing a solution of 1:10 KI_2 gold etch and RO water which is heated to 60°C on a hotplate. The etchant does not react with the hydrogen termination of the surface, leaving it intact. The etch is performed for 10 seconds as this has been calibrated to clear out the exposed areas while providing an undercut of 100-200nm. Geometry of VDP structures and the dimensions of TLM structures are very important, thus a larger undercut could compromise the electrical characterization of these structures.

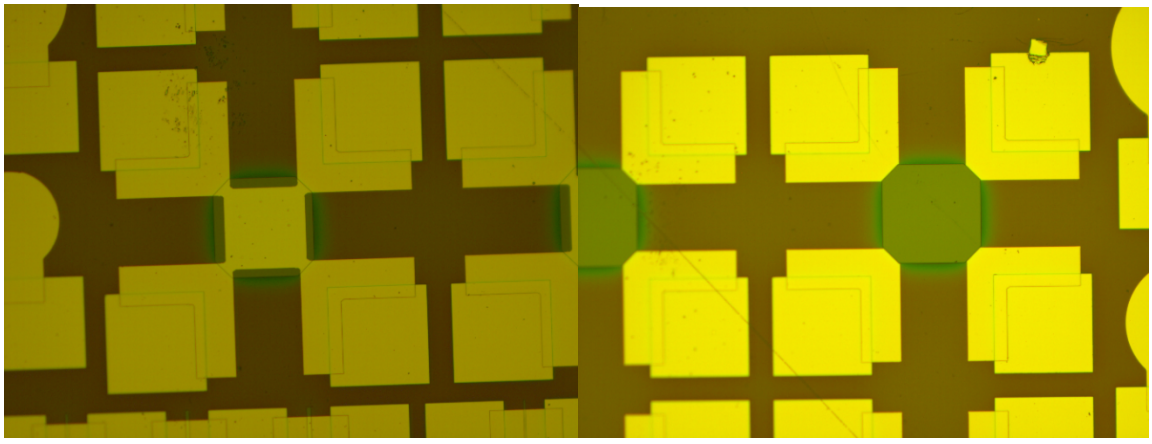

Figure 4.14.10 – "Active" lithography of VDP structure (left) and VDP structure after "Active" etch

Gate lithography, etch and metallization

In order to fabricate gates on hydrogen terminated diamond a self-aligned etch and deposition process is used. In a similar fashion to that previously applied for etching of the "active" regions of the test structures the source drain gap of the FETs must also be etched, and then gates deposited in the middle. For MESFET devices this process can be seen below in *figure 4.14.11* whereby the same resist profile is used to etch the source-drain gap and lift

off the gate metal. In this work, EBL has been used to define gate lengths of 250nm, 500nm and 2µm.

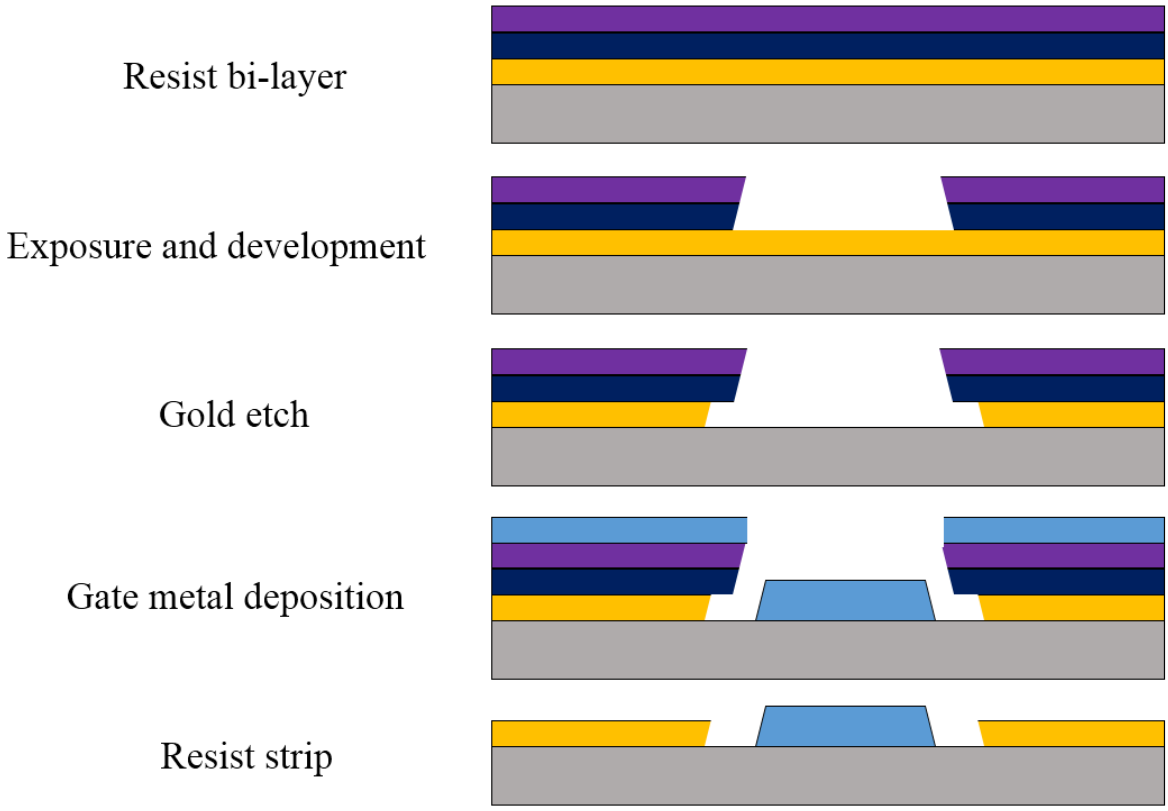

Figure 4.14.11 – Process of defining gate in diamond MESFET process.

To begin the gate fabrication process, a bi-layer of PMMA is spun onto the substrate and baked in an oven at 120°C to remove solvents. Following this a charge depletion layer of 10nm of aluminium is deposited on top of the resist. Following EBL exposure, charge depletion layer removal, and development of the resist, the source-drain gap is etched. This etch is performed using a KI_2:RO water solution in a 1:10 ratio heated to 60°C. The sample is etched for 15 seconds in order to provide an undercut of ~1µm to either side of the gate lithography. In the case of the 500nm gate shown *in figure 4.14.12* the total distance between the source and drain is around 3µm. Following the gold etch, the gate metallization can be deposited. After this the resist is stripped and the metal deposited in the middle of the source drain gap will remain as the defined gate contact.

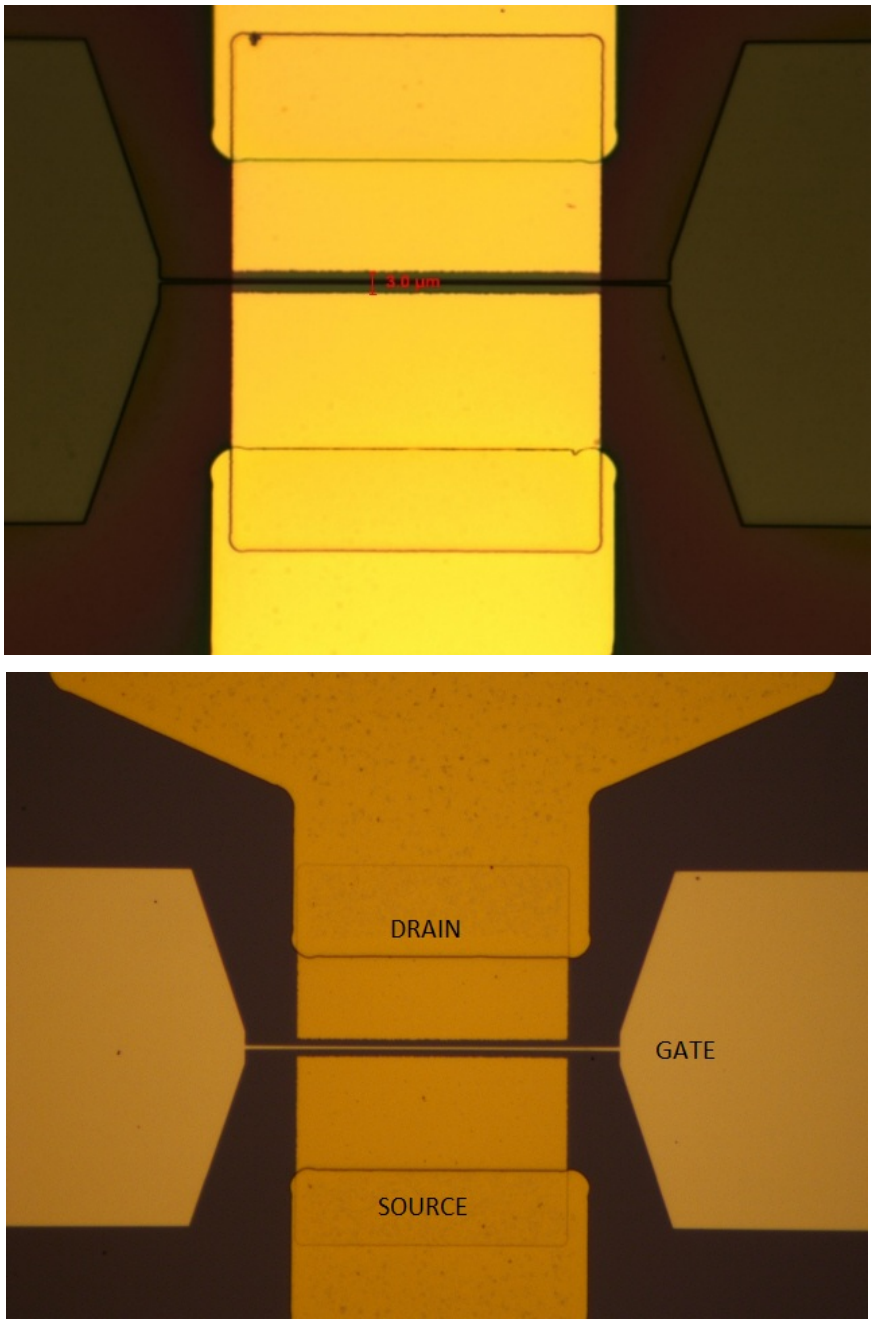

Figure 4.14.12 – Optical images of gate lithography and gold etch (Top) and after gate metal deposition and resist removal (Bottom). Gate length is 500nm.

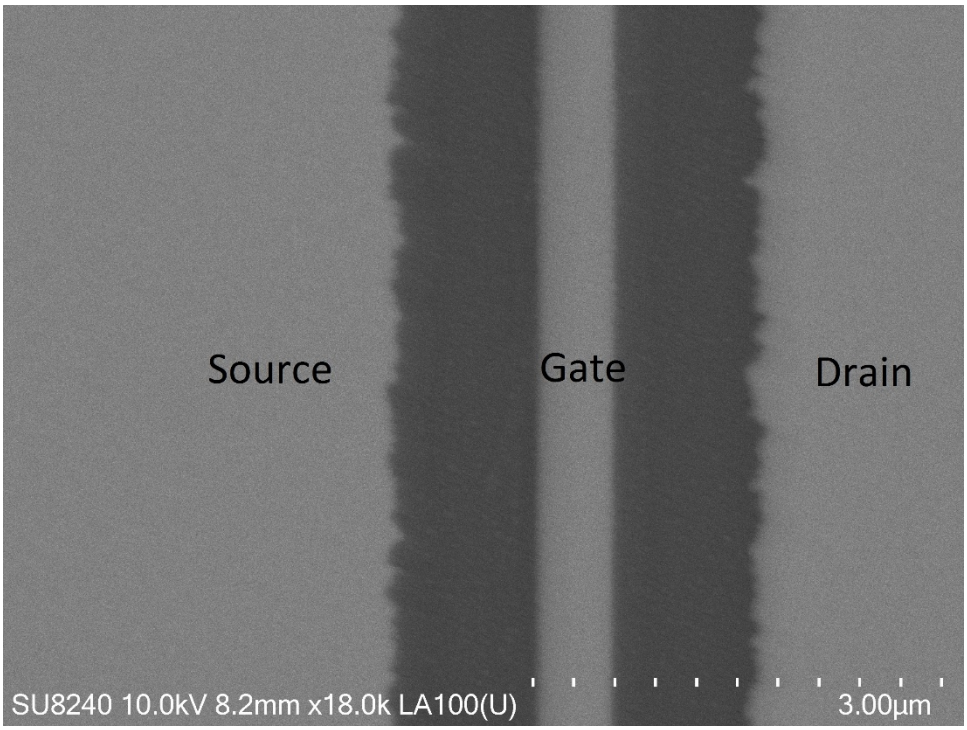

Figure 4.14.13 – SEM image of a 500nm gate after deposition showing source-drain gap and metal deposition in the middle.

Gate metallization of a tri-layer of 20nm aluminium, 20nm of platinum and 40nm of gold as seen on the left of *figure 4.14.14* was primarily used for this work. Aluminium was included as the contact metal as the low work function provides a Schottky barrier when in contact with the hydrogen terminated diamond surface[4.7], suitable for MESFET configuration. Platinum was included in the gate metallization in order to provide a diffusion barrier to impede the aluminium and gold layers intermixing when the gate is exposed to high temperatures during vacuum annealing required prior to surface transfer doping oxide deposition. Gold was included as the gate metal "cap" as it is a noble metal and does not oxidize when exposed to atmospheric conditions. Having a thicker gate metallization also increases the robustness of the gate stack allowing for repeated probing.

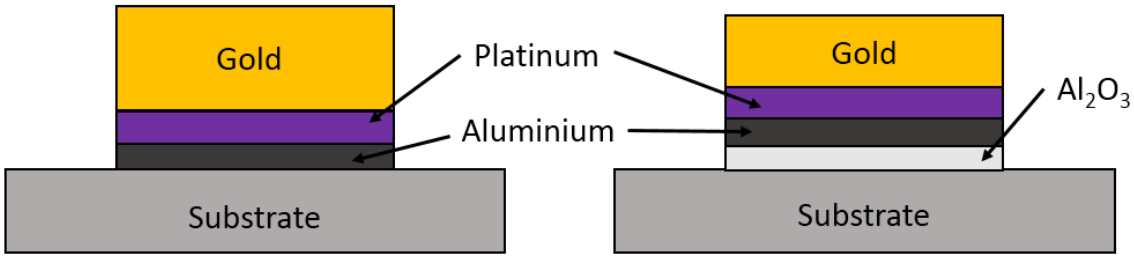

Figure 4.14.14 – Gate metallization explored in this body of work.

This work also reports gates including aluminium oxide (Al_2O_3) deposited by electron beam evaporation (as can be seen on the right of *figure 4.14.14*) as a gate dielectric in an attempt

to further increase the robustness of the gate stack at elevated temperatures and reduce gate leakage currents.

Surface transfer doping oxide deposition

The key development in diamond FET fabrication reported in this body of work is the incorporation of surface transfer doping oxides into the hydrogen terminated diamond FET structure. In order to achieve this surface transfer doping oxides are blanket deposited over the surface of the fabricated FETs as shown in *figure 4.14.15* in order to affect the "channel" areas. This deposition was performed in a Plassys MEB400 system which has both a thermal and electron beam evaporation source. All surface transfer doping oxide deposition reported in this work was performed by thermal evaporation using MoO_3 and V_2O_5 sources. Deposition is performed at a vacuum pressure of x10-^{6} mbar.

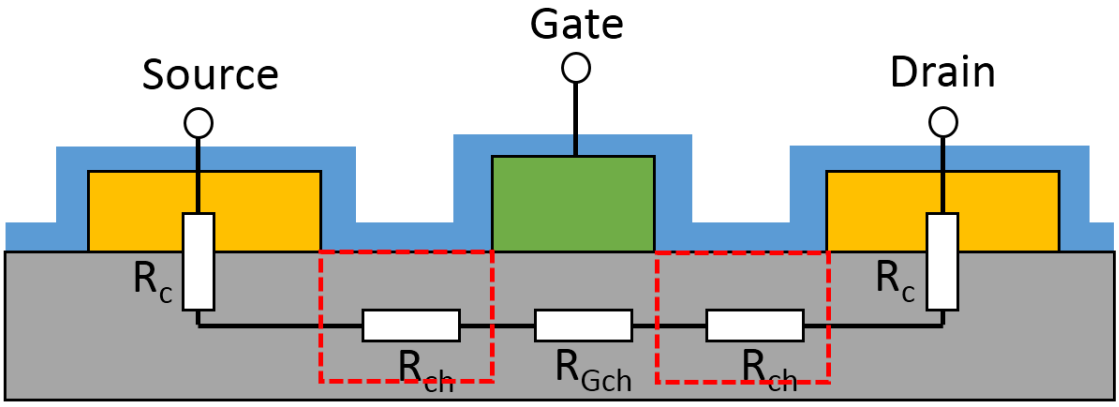

Figure 4.14.15 – Surface transfer doping oxide in light blue, showing effect on resistance of channel of FETs.

It is required to include a high temperature vacuum anneal of 400°C for 1 hour prior to in situ deposition of surface transfer doping oxides in order to remove residual atmospheric adsorbates and improve the stability of the 2DHG [4.8]. Heating the diamond to 400°C in vacuum has not been shown to degrade the hydrogen termination of the diamond surface. The Plassys MEB400 has the capability to heat the stage to up to 400°C for this purpose. This vacuum anneal has no adverse effect on the hydrogen termination of the diamond's surface.

4.14 Chapter Summary

This chapter has explored the individual fabrication processes of acid cleaning, hydrogen termination, surface preparation, photolithography and electron beam lithography (resist spinning, exposure and development), physical vapour deposition and etching (wet and dry).

These processes are used in this work in order to produce FETs which will be characterized in the following chapters. The chapter has also covered optical microscopy, SEM, AFM, and stylus profilometry which have been used to physically characterize the fabricated FETs in this work. Finally, the chapter explored how the previously explained fabrication processes have been utilized to produce FETs by detailing the full process flow. More detailed process flows can be found in appendix A.

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[4.8] K. G. Crawford, D. Qi, J. McGlynn, T. G. Ivanov, P. B. Shah, J. Weil*, et al.*, "Thermally stable, high performance transfer doping of diamond using transition metal oxides," *Scientific Reports,* vol. 8, p. 3342, 2018/02/20 2018.

5. Electrical characterization methods

In order to assess the performance of the devices created in this work, various electrical characterization techniques are employed. This is split into two distinct areas. The first is material characterization, whereby the material can be assessed using techniques such as transmission line measurement (TLM) and Van der Pauw measurements (VDP). The next is device measurement, whereby the performance of full FET structures can be assessed by measuring their DC IV output and transfer characteristics. These techniques will be explored in detail in this chapter.

5.1 Material Characterization

In order to fully understand the electrical performance of a semiconducting material the techniques of Transmission line measurement (TLM) and Van der Pauw measurements (VDP) can be utilized.

5.1.1 Transmission Line Measurement (TLM)

Transmission Line Measurement (TLM) is a method of characterizing semiconducting material to calculate the sheet resistance and the contact resistance between a semiconducting material and a metal contact.

A potential difference is applied across 2 ohmic contacts with a gap of a known distance. The current flowing between the 2 contacts is measured and the resistance can be calculated using ohms law, which is shown in *equation 5.1.1.1*

$$R = V/I \qquad \textit{equation. 5.1.1.1}$$

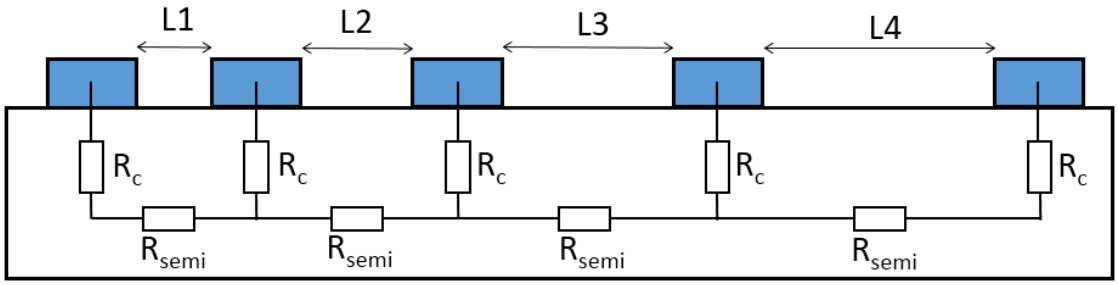

Figure 5.1.1.1 – TLM structure modeled as a resistor network, showing increasing gaps between ohmic contacts.

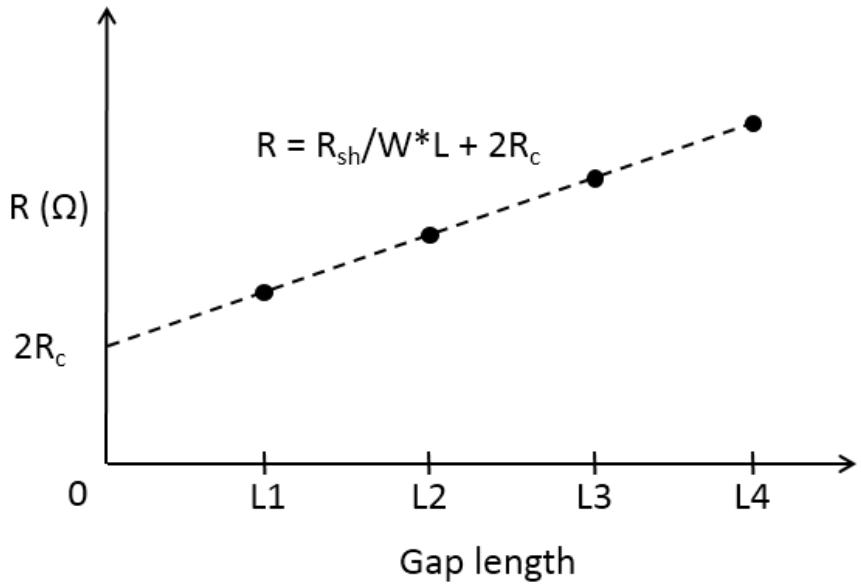

Figure 5.1.1.2 –Ideal plot of measured resistance against gap lengths of TLM structure.

This operation is performed for a series of distances increasing linearly. If the measured resistances are plotted against distance between contacts the resulting plot should appear linear. A line can be fitted and traced back to 0 distance, this would be the theoretical situation of zero distance between 2 ohmic contacts. Thus the resistance value at the intercept can be expressed as 2 times the contact resistance shown as $2R_c$ in *figure 5.1.1.1*. For this work the ohmic contact resistance is normalized to the width of the ohmic contact (Ω.mm). Although in technologies such as silicon the contact resistance is normalized by the area of the contact, this assumes that the sheet resistance of the material is constant under the ohmic contact. As the hydrogen terminated diamond relies on surface conductivity it cannot be assumed that this is true.

The sheet resistance of the material can be calculated using the gradient of the fitted line using the equation shown in *equation 5.1.1.2*, where W is the width of the TLM structure.

$$Rsh = gradient*W \qquad \text{equation. 5.1.1.2}$$

5.1.2 Van Der Pauw measurements (VDP)

Van der Pauw (VDP) measurement is a useful and widely used tool for assessing the properties of materials of interest to semiconductor technologies such as carrier concentration, sheet resistance and carrier mobility.

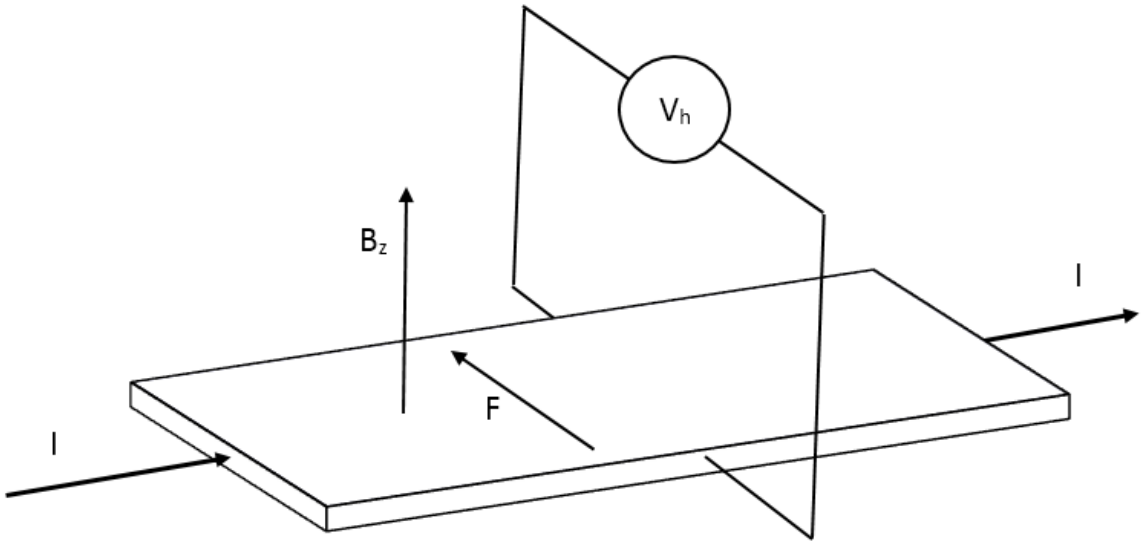

Figure 5.1.2.1 – Hall Effect example showing magnetic field direction B_z, Hall voltage V_h, direction of current flow I, and direction of force on majority carriers F.

If current is passed through a piece of material, an applied magnetic field "B_z" deflects charge from its straight path causing a build-up of charge at the edges of the material. Enough charge will eventually be present that the current flow returns to its straight path. The difference in potential due to this charge between the two sides of the material is called the "Hall voltage" or "V_h".

In this work The Hall Effect is utilised to perform VDP measurements using the "Nanometrics 550 Hall Kit", a 4 probe Hall measurement system which can be seen in *figure 5.1.2.2*. Van der Pauw (VDP) structures (an example of which can be seen in *figure 5.1.2.4*) were fabricated on all samples.

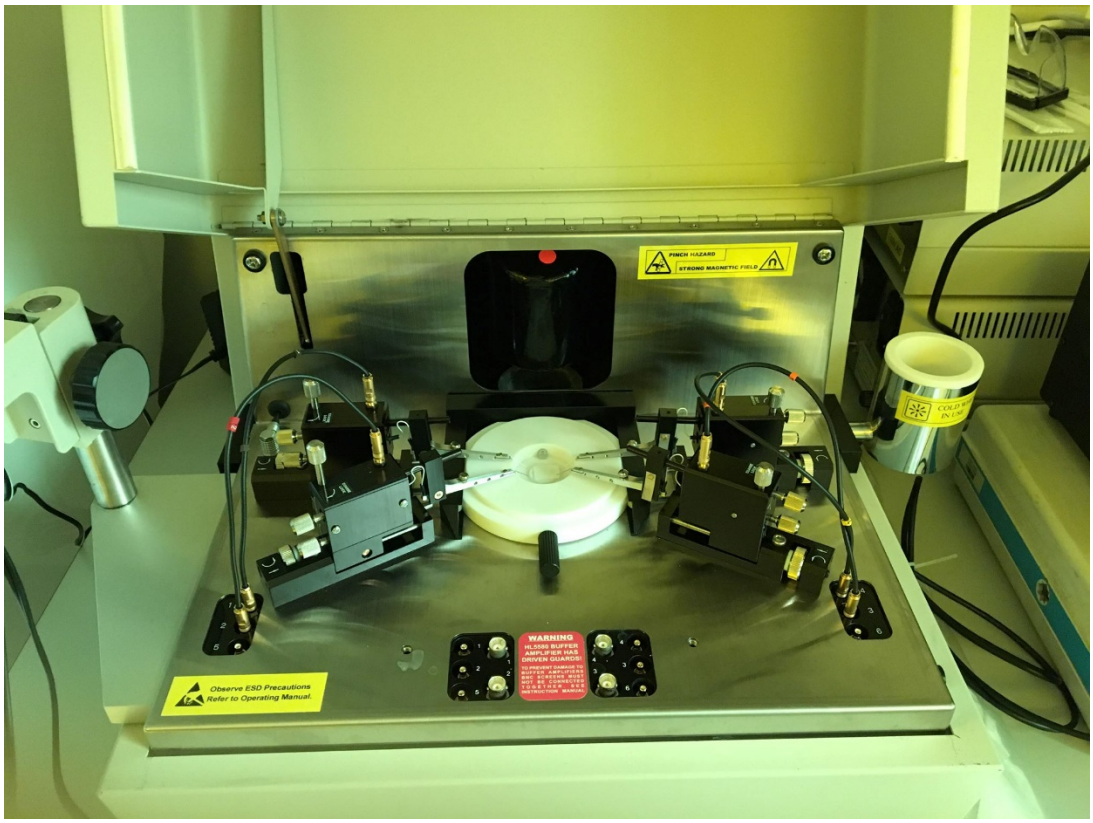

Figure 5.1.2.2 - Nanometrics 550 Hall Kit 4 probe hall measurement system used in this work.

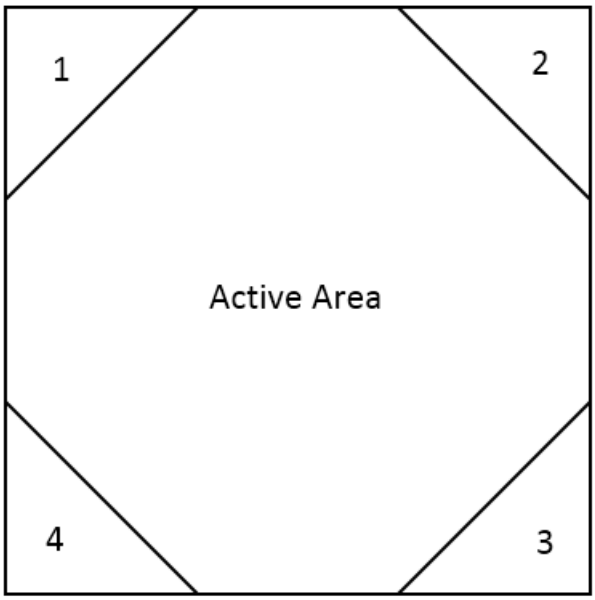

Figure 5.1.2.3 - Simplified VDP structure showing ohmic contacts numbered 1 to 4.

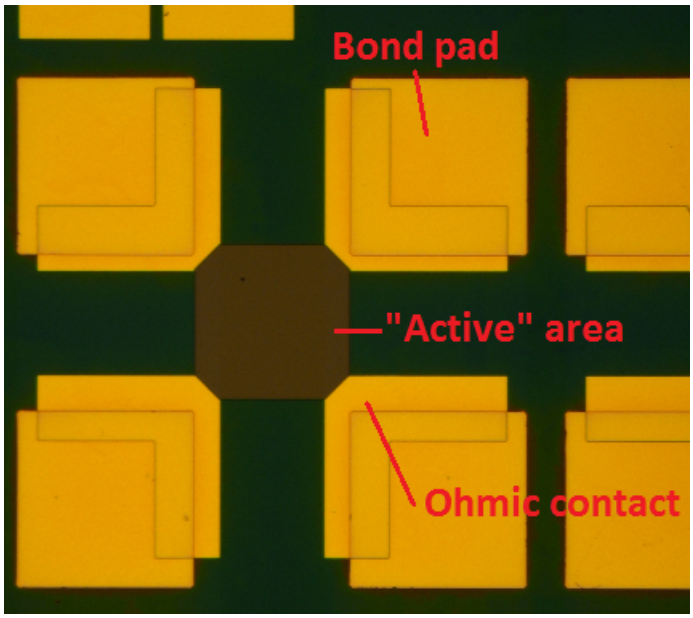

Figure 5.1.2.4 – Fabricated VDP structure showing bond pads, ohmic contacts, and "active" area after etching prior to resist stripping.

A current can be injected between 2 contacts on the structure, which will give rise to a corresponding voltage across the 2 other contacts. Using Ohm's law a resistance can be calculated. For instance if current is injected between contacts 1 and 2, a corresponding voltage can be measured between contacts 3 and 4. Leo Van der Pauw showed that the sheet resistance of a material could be calculated using two such measurements, one vertical and one horizontal[5.1]. If the resistances measured are the same, the formula below in *equation. 5.1.2.1* can be used to calculate the sheet resistance, where Rs is sheet resistance, and R is the measured resistance.

$$R_s = \frac{\pi R}{ln2} \qquad \textit{equation. 5.1.2.1}$$

After calculating the sheet resistance the VDP method can also be used to calculate the Hall coefficient, carrier concentration and mobility of the material. Current can be injected between two contacts with a positive magnetic field applied to the substrate. The voltage can be measured at the other 2 contacts. This is repeated for a negative magnetic field. The difference in the measured voltages is the hall voltage. The sign of the hall voltage determines whether the majority carriers are electrons (n-type) or holes (p-type). The hall voltage can be used to calculate the sheet carrier concentration. The hall coefficient can be calculated using the known values of the current, magnetic field and hall voltage as seen in *equation 5.1.2.2*, where R_H is the hall coefficient, V_h is the hall voltage, I is the current, and B is the electric field.

$$R_H = \frac{V_h}{IB} \qquad \textit{equation. 5.1.2.2}$$

The carrier concentration of the material can be calculated using the hall coefficient using the formula in *equation 5.1.2.3*, where n_s is the carrier concentration, and q is the unit charge.

$$n_s = \frac{1}{qR_H} \qquad \textit{equation. 5.1.2.3}$$

Using the previously calculated sheet resistances and hall coefficient, one can calculate the mobility of the carriers using *equation 5.1.2.4*, where μ is the mobility of charge carriers.

$$\mu = \frac{R_H}{R_s} \qquad \textit{equation. 5.1.2.4}$$

The VDP technique is important for characterising a material as the current a semiconductor is able to transfer is determined by the amount of charge passing through an area per unit time. Thus the amount of charge carriers is an important metric to understand. As noted below, minimising the sheet resistivity of a material is also important. Mobility is also important to understand for electronics operating under low electric fields.

5.2 Field Effect Transistor (FET) characterisation

Although the previously explored methods of TLM and VDP measurements allow us to form a picture of the material qualities of a semiconductor, in order to understand the operation of a field effect transistor (FET) there are 2 main DC IV measurement techniques which can be employed; Transfer characteristics measurement (I_dV_g) and Output Characteristics measurement (I_dV_d).

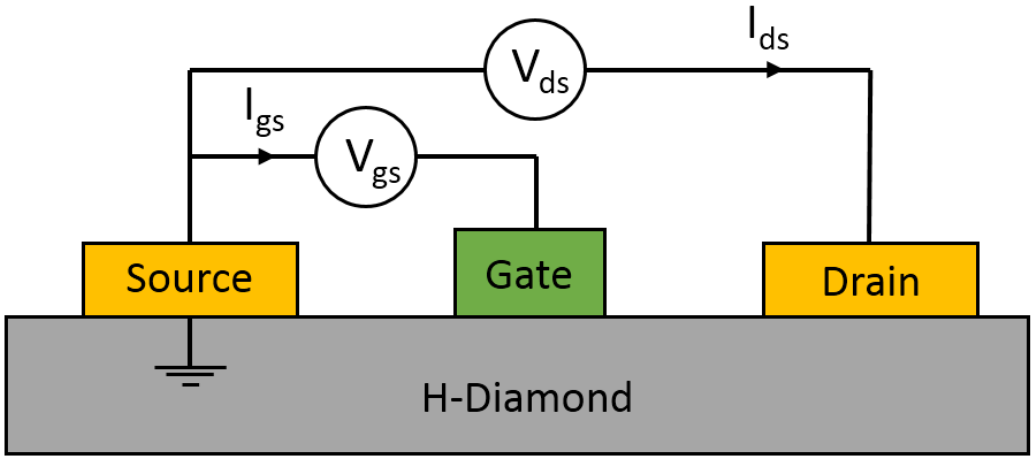

Figure 5.2.1 – Simplified FET model showing applied potentials V_{gs} and V_{ds}, and measured currents I_{ds} and I_{gs}.

For DC FET measurements 3 probes are used. 1 in contact with each of the gate, drain and source contacts. The current is measured at each contact. For this work DC measurement was performed with an Agilent B1500a Semiconductor device analyser. The probes are Source Measurement Units (SMU), which are capable of simultaneously acting as a current source and measurement unit.

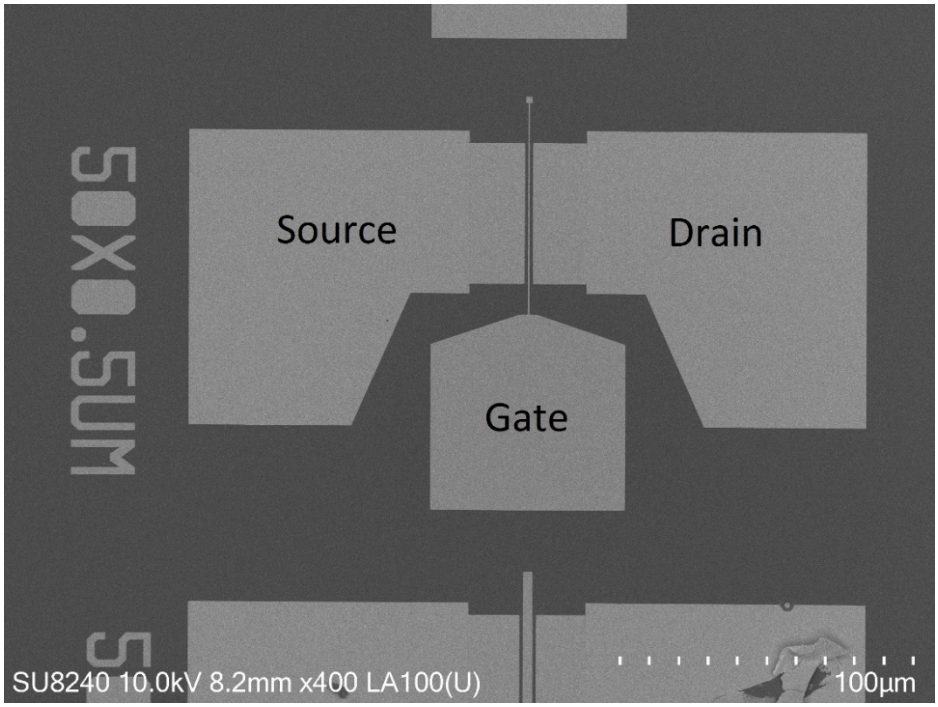

Figure 5.2.2 – "Single finger" DC FET fabricated throughout this work.

5.2.1 Output Characteristics

Output characteristics refers to the technique used to assess the "output" of fabricated FETs, mainly the drain or "output" current. In order to assess the output characteristics (also

referred to as I_dV_d) of a FET, the source contact is kept grounded and the drain voltage is swept, the gate voltage is stepped after each sweep of the drain voltage. Output characteristics are useful for ascertaining the maximum drain current of fabricated FETs (I_{dmax}), as well as the on resistance (R_{on}), which are both important metrics for high power FETs.

The output characteristics can be split into 2 distinct regions of operation. The first is the "Linear" region; where the FET acts as a voltage dependent resistor, with the resistance dependent on the voltage applied to the gate contact. As the potential between the source and drain increases in the linear region the charge carriers accelerate due to the increasing electric field, resulting in a higher drain current. The rate at which the carriers accelerate is dependent on the mobility of the charge carriers in the channel. The second region is the "Saturation" region, which occurs where the drain current saturates with increasing drain voltage for a constant gate voltage. As the electric field at the drain increases, eventually the velocity of charge carriers will saturate, resulting in saturation of the drain current. As the gate voltage is stepped, the concentration of charge in the channel under the gate increases, or decreases dependent on the potential applied, which will result in either a higher or lower drain current. Although this cannot continue into perpetuity as the gate contact can only deplete or accumulate a finite amount of charge. The transitional area between the linear region and the saturation region is referred to as the "knee" region.

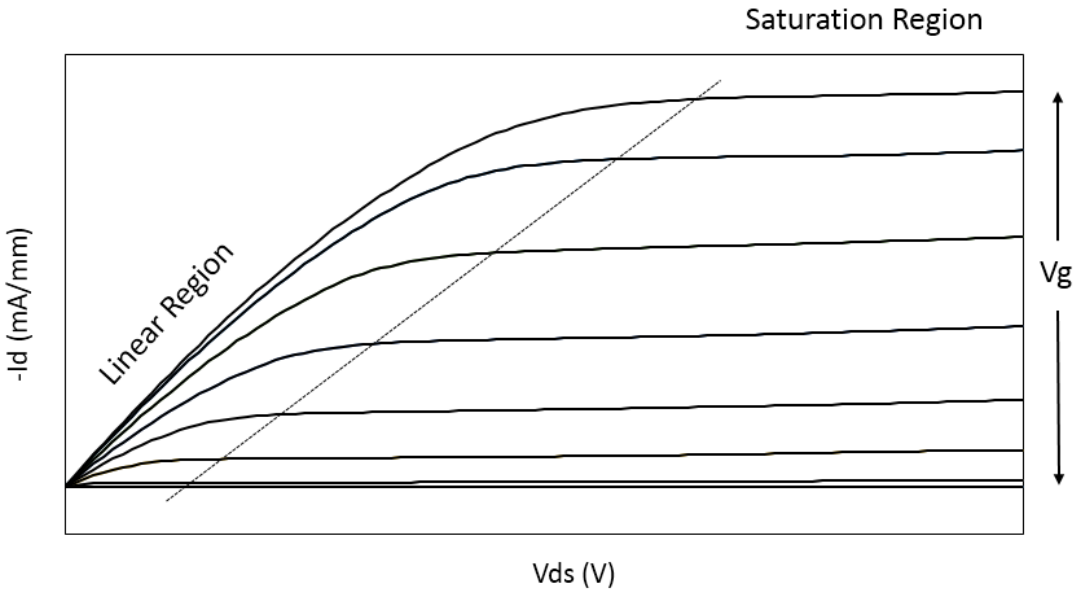

Figure 5.2.1.1 - Ideal Output characteristic measurement for a MOSFET or MESFET structure showing drain current in solid blue.

As mentioned above, the output characteristics are also useful for measuring the static "on state resistance" (R_{on}) of fabricated FETs. In the linear region, where the FET acts like a

resistor, ohms law tells us that the gradient of the linear region is equal to $1/R_{on}$. Below in *figure 5.2.2.2* one can see a simplified model of the series resistances which make up R_{on}.

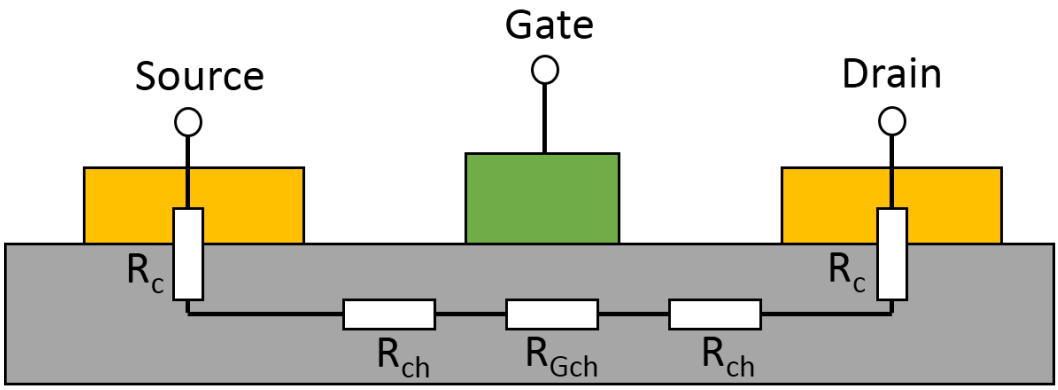

Figure 5.2.1.2 – Simplified model of an FET during linear region operation showing constituent resistances which make up "R_{on}".

TLM measurements can provide us with measured values for the resistance of the contacts (R_c). The sheet resistance measured by VDP or TLM can be used to calculate the resistance in the channel areas of the FETs (R_{ch}). The only resistance which makes up R_{on} which is difficult to extract directly is the resistance under the gate of the FET. Therefore we can measure R_{on}, R_c and R_{ch} and use this to calculate the resistance under the gate contact.

$$R_{ON} = 2R_C + 2R_{CH} + R_{GCH} \qquad \textit{equation. 5.2.1.1}$$

The output characteristics will also be used to assess the off state performance of the fabricated FETs. In this case the gate voltage will be held constant in the "off" state, and the drain voltage will be swept to high voltages in order to assess at what drain voltage the FETs "breakdown", or the current increases above the previously defined threshold current. As will be discussed in the following sub-chapter, the "on" current for this work will be defined as -0.1mA/mm. Therefore the "breakdown voltage" has been defined as the drain voltage at which the drain current surpasses -0.1mA/mm when the gate is "off". The drain current is plotted in the log scale so one can more easily observe the changes in order of magnitude of the drain current. Below in *figure 5.2.2.3* you can observe an example off state output plot for a 250nm gate length MOSFET at 2V gate voltage.

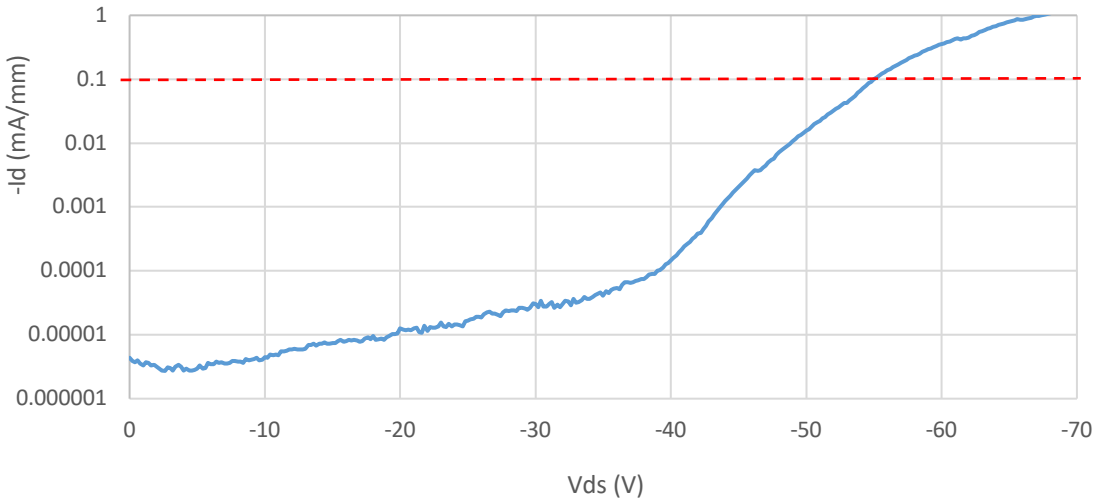

Figure 5.2.1.3 – Exemplar plot of off state performance output characteristics. Red line shows the "threshold current".

5.2.2 Transfer Characteristics

Transfer characteristics (also referred to as I_dV_g) are obtained by sweeping the voltage between the gate and source (V_{gs}) at a given bias between the drain and source (V_{ds}) and stepping the drain-source bias after each sweep. The extrinsic transconductance can be calculated from the transfer characteristics as the rate of change of drain current with respect to gate voltage. Transconductance is an important metric for FET characterisation. Transfer characteristics are also useful for determining the threshold voltage of a FET. Threshold voltage is the point at which the device can said to turn "on" as the gate has accumulated enough charge for substantial current to flow between the source and drain contacts. The most common method of defining threshold voltage is using the constant current method, where by the threshold voltage is defined as the point at which the normalised drain current (I_{ds}) reaches a certain magnitude. Threshold voltage can be defined somewhat arbitrarily[5.2]. In this body of work -0.1 mA/mm has been chosen as the "on" current as this is around 0.1% of the magnitude of the typical maximum drain current for atmospheric adsorbate FETs fabricated in this work. Transistor operation falls into two categories. Depletion mode (normally on) and enhancement mode (normally off). In depletion mode a gate voltage is needed to switch the FET "off", by pushing the current below the threshold and in enhancement mode a gate voltage is required to switch the device "on", by pulling the current above the threshold.

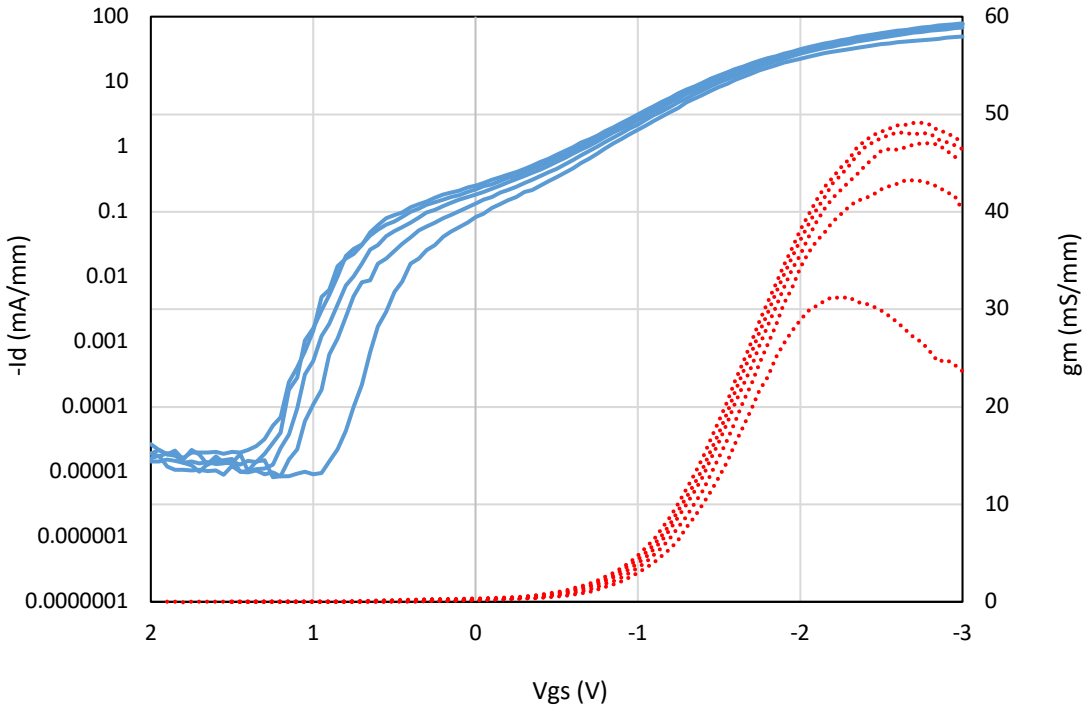

Figure 5.2.2.1– Exemplar Transfer characteristics of 250nm gate length depletion mode FET in this work. Drain current is plotted in blue plotted on a log scale. Extrinsic transconductance is plotted as a red dashed line.

As discussed previously in chapter 2, transconductance is the rate of change of drain current with respect to gate voltage for a constant drain voltage. This is essentially a measure of how efficiently the gate contact can change the drain current beneath it for each step in gate voltage. In contrast to extrinsic transconductance, the intrinsic transconductance describes the efficiency of this process without the impact of parasitic resistances[5.3].

$$g_m^* = \left(\frac{dI_{ds}}{dV_{gs}}\right)_{V_{ds}} \qquad \textit{equation 5.2.2.1}$$

The intrinsic transconductance (g_m^*) only applies to the gate contact assuming that it is an ideal parallel plate capacitor and does not take into account the voltage drop between the source and gate contacts. Extrinsic transconductance can also be calculated as the rate of change of measured drain current with respect to the applied gate voltage for a constant drain bias, which can be seen plotted in orange in *figure 5.2.1.1*. Extrinsic transconductance (g_m) which includes the source resistances, is defined as follows:

$$g_m = \frac{g_m^*}{1 + g_m^* R_s} \qquad \textit{equation 5.2.2.2}$$

The source resistance (R_s) term takes into account the voltage drop between the source and gate contacts. R_s is a combination of the sheet resistance in the channel R_{ch} and the contact resistance R_c ($R_s = R_{ch}\ R_c$) as can be seen in *figure 5.2.2.2*.

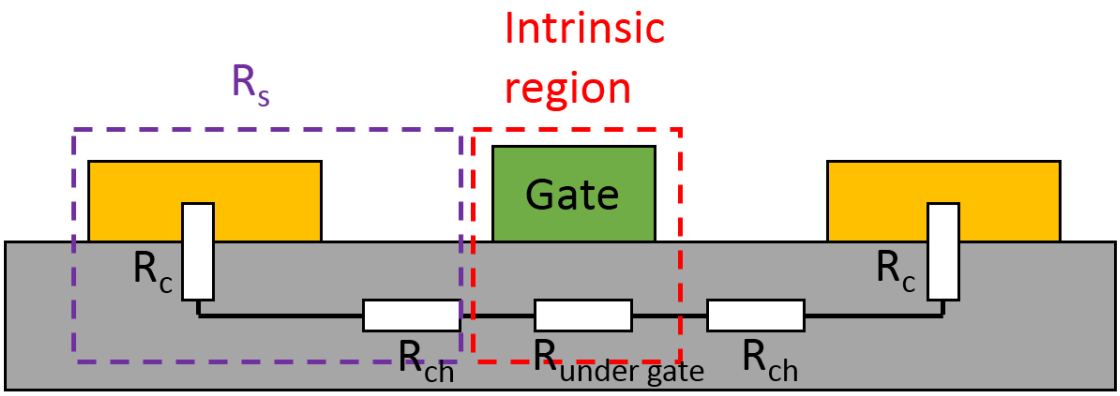

Figure 5.2.2.2 – Simplified FET model showing "intrinsic" region in red, and access resistances R_s in purple.

The measured values for extrinsic transonconductance, channel resistance (R_{ch}) and contact resistance (R_c) have been used to calculate the intrinsic transconductance in this work using the formula below:

$$g_m^* = \frac{g_m}{1 - g_m R_s} \qquad \textit{equation 5.2.2.3}$$

5.3 Chapter Summary

This chapter has detailed the material characterisation techniques of TLM and VDP measurements which were used to assess the quality of substrate surface preperation used to fabricate FETs in the following chapters. This chapter has also outlined the FET characterisation techniques utilised in subsequent chapters to assess the performance of fabricated FETs. Output characteristic measurement is used to assess the maximum drain currents, on resistance, and breakdown voltage. Transfer characteristic measurement is used to examine the extrinsic tranconductance, and threshold voltages. These parameters are important to understand in order to analyse the improvement to the performance of the fabricated FETs.

References

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6. Hydrogen terminated diamond MESFETs

Hydrogen terminated diamond MESFETs using atmospheric adsorbate doping have proven to be promising in the high-power high-frequency operating space [6.1, 6.2]. However atmospheric adsorbates provide inconsistent performance and begin to sublimate from the surface of the diamond at temperatures as low as 60°C[6.3]. Due to the nature of the adsorbates, device high temperature operation and long term stability of performance is poor. Alternative surface transfer doping materials such as V_2O_5 and MoO_3 have recently been investigated as alternative surface acceptors in order to increase the high temperature stability, carrier concentration and long term stability of hydrogen terminated diamond FETs [6.4, 6.5]. Although the results shown so far have been promising the full potential of these materials when incorporated into the architecture of diamond FETs has been hampered by the difficulties of integrating the materials into the FET structure.

This chapter begins by investigating the effects of deposition of MoO_3 and a pre deposition vacuum anneal at 400°C on VDP and TLM structures. Following this the chapter outlines the initial challenges and results of including the surface transfer doping oxides MoO_3 and V_2O_5 into hydrogen terminated diamond MESFETs.

One of the challenges of working with a material in its early developmental stages such as hydrogen terminated diamond is the inconsistency of acquired results. Therefore the results shown should be taken as a representation of the potential of the technology.

The focus of this work has been engineering hydrogen terminated diamond FETs to achieve the best results in regards to maximum drain current, peak transconductance, lowest on resistance and off state breakdown voltage. These characteristics are important to the operation of high power FETs as outlined in chapter 5.

The fabrication processes used in this chapter are outlined in chapter 4, and in further detail in appendix A. The electrical characterization methods used are outlined in chapter 5.

6.1 Hydrogen termination

The hydrogen termination and surface preparation of the material shown is outlined in chapter 4. In the beginning of this research project the hydrogen termination available to the author resulted in high sheet resistances when the diamond surface was exposed to atmosphere. There was also no “new” material available for the outlined work. Therefore recycling of existing diamond material was undertaken. To this end the material was acid

boiled to remove surface contamination as described in appendix A, and the material hydrogen terminated by collaborators at Unversitie Paris 13. However this non-optimised hydrogen termination processes provided poor results with sheet resistances as high as 170kΩ/□, possibly resulting from incomplete termination of the surface. Typically sheet resistances of 10-20kΩ/□ are reported in literature [6.6, 6.7].

As the quality of hydrogen terminated diamond was not consistent, it was initially decided that recycled material would have an epitaxial layer of CVD diamond grown on the surface which would be hydrogen terminated in-situ at the end of the growth by the author's collaborators at Universtie Paris 13. This process resulted in more consistent sheet resistances, ranging from 23.5 to 33.4 kΩ/□. However there were some issues regarding the epitaxial CVD layer growth and suspected boron contamination as discussed later in this chapter.

Towards the end of this research, work was undertaken to improve the quality of the hydrogen termination by the author's colleague and fellow PhD student Kevin Crawford. The work reports sheet resistances as low as 4.1kΩ/□after deposition of MoO_3 by etching the diamond surface with a tailored Cl_2 +A_r and O_2 + Ar chemistry to remove surface and sub-surface damage, and exposing the surface to a 2.6kW power density hydrogen plasma [6.8]. Using this new process to hydrogen terminate as purchased CVD material sourced from Element Six the last few samples shown in this work provided consistently lower sheet resistances of 20-7kΩ/□ using atmospheric adsorbates as surface acceptors.

Below in *table 6.1.1* is a summary of the properties of the material used for fabrication in this chapter and the following chapter with the H-diamond surface exposed to air.

Sample	*Hydrogen termination*	*Mobility* (cm^2/Vs)	*Sheet resistance* $(k\Omega/\square)$	*Carrier concentration* $(/cm^2)$
Sample A	*CVD epitaxial layer in situ 2kW PD*	*51*	*23.5*	$5x10^{12}$
Sample B	*CVD epitaxial layer in situ 2kW PD*	*41*	*33.4*	$4.49x10^{12}$
Sample C	*2kW PD*	*201*	*170*	$1.8x1x10^{11}$
Sample D	*2.6kW PD*	*208*	*20.6*	$1.45x10^{12}$
Sample E	*2.6kW PD*	*79.5*	*7.2*	$1x10^{13}$
Sample F	*CVD epitaxial layer in situ 2kW PD*	*n/a*	*20.8*	*n/a*
Sample G	*2.6kW PD*	*103*	*7.2*	$8.39x10^{12}$

Table 6.1.1 – Hydrogen termination processes of material fabricated in chapters 6 and 7 (PD = Power density of the hydrogen plasma).

6.2 - VDP and TLM structures with vacuum annealing and MoO_3 deposition - Sample A

The effect of deposition of surface transfer doping oxides such as MoO_3 and V_2O_5 combined with the use of a 400°C pre-anneal in order to remove residual atmospheric adosbrates has already been demonstrated by Van Der Pauw measurement in a number of publications [6.9-11]. However, the impact of application of these materials and anneal stage on the ohmic contact resistance has not yet been reported. Therefore an experiment was designed to assess the effect of MoO_3 on both the sheet resistance and contact resistances of diamond substrate using VDP and TLM structures.

A sample was overgrown with a 5µm CVD diamond layer by collaborators at Universite Paris 13 with a surface roughness of 0.6nm Ra measured by AFM. This sample was fabricated with TLM and VDP structures using the processes outlined in chapter 4. Following the etching of the gold to form the "active" areas of the TLMs and VDPs the

sample was left for 2 days in order to accumulate atmospheric adsorbates in the etched areas to induce surface transfer doping. The TLM and VDP structures were then measured.

Measurement Method	*Sheet resistance (kΩ/□)*	*Contact Resistance (Ω.mm)*	*Mobility (cm^2/Vs)*	*Carrier Concentration ($/cm^2$)*
TLM	*26.9*	*30.1*	*n/a*	*n/a*
VDP	*23.5*	*n/a*	*51*	*$5x10^{12}$*

Table 6.2.1 – Results from TLM and VDP structures with atmospheric adsorbate induced surface transfer doping.

The sheet resistance of 23.5k Ω/□ with atmospheric induced surface transfer doping is close to what has been reported in literature, typically 10-20kΩ/□ [6.6, 6.7]. However the contact resistance of 30.1 Ω.mm is higher than has been reported in the literature for gold ohmic contacts on hydrogen terminated diamond, typically 4-5 Ω.mm [6.12, 6.13].

Following TLM and VDP measurements the substrate was annealed at 400 °C at a vacuum pressure of $2x10^{-6}$ mbar for one hour in a Plassys MEB400 system. Following this 30nm of the surface transfer doping material MoO_3 was deposited by thermal evaporation in-situ without breaking vacuum after the substrate was cooled to room temperature.

Measurement Method	*Sheet resistance (kΩ/□)*	*Contact Resistance (Ω.mm)*	*Mobility (cm^2/Vs)*	*Carrier Concentration ($/cm^2$)*
TLM	*18.4*	*11.8*	*n/a*	*n/a*
VDP	*18.68*	*n/a*	*41*	*$8.12x10^{12}$*

Table 6.2.2 – Results from TLM and VDP structures after vacuum annealing at 400°C for one hour and deposition of 30nm MoO_3.

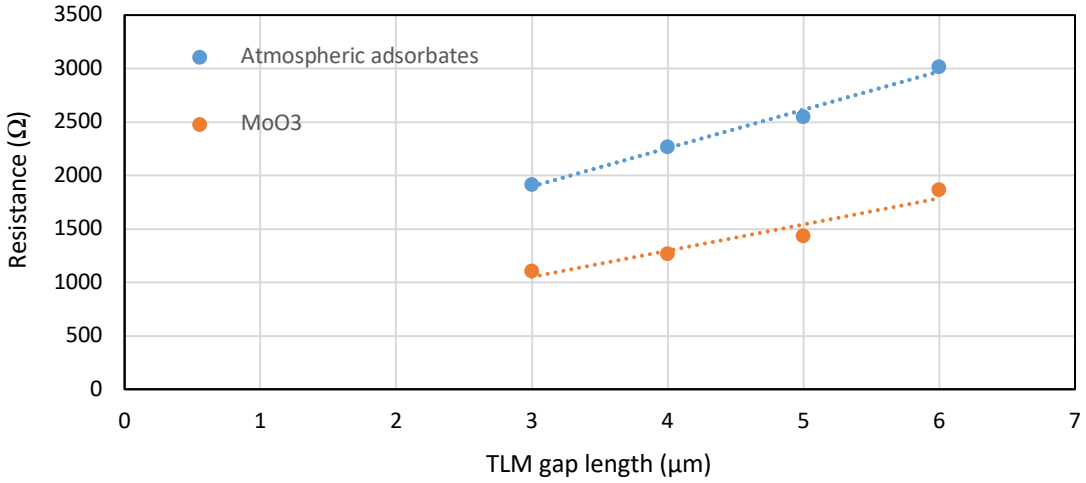

Figure 6.2.1 - TLM measurements from atmospheric adsorbates (Blue) and after annealing and in-situ MoO_3 deposition (Orange) from the same TLM structure.

There is substantial variation in the results acquired from different TLMs on the substrate. This could be indicative of poor consistency of the hydrogen termination of the substrate leading to varying current paths. As VDP measurements are taken over a larger geometric area, it is assumed that the VDP measurements are more representative of the general material qualities. The TLM chosen to represent the substrate shown in *figure 6.2.1* has a sheet resistance close to what has been measured from the VDP structures.

The results shown are indicative of the effects of deposition of the surface transfer doping oxide MoO_3 after an in-situ vacuum anneal in order to improve the long term operational stability of the surface transfer doping oxide. As would be expected there has been a decrease in sheet resistance observed by VDP results from 23.5kΩ/□to 18.68kΩ/□. The decrease is due to an increase in the carrier concentration, accompanied by a small decrease in mobility in the 2DHG, which is consistent with results reported in literature for deposition of MoO_3 [6.9, 6.10].

The TLM results also show there has been a substantial and unexpected decrease in the contact resistance of the TLM structures from 30.1Ω.mm to 11.8Ω.mm. The mechanism behind this reduction in contact resistance in unclear. One would not expect the gold to react with the diamond surface to form a carbide, or diffuse into diamond at annealing temperatures of 400°C [6.14]. It may be argued that the gold contacts have migrated slightly from the original location into the channel area, allowing better contact to the 2DHG. Another theory is that atmospheric adsorbates below the gold contact have diffused through the gold and left the substrate surface, resulting in an improved interface between the ohmic contact and diamond surface. Which, if any of these mechanisms is responsible for the

reduced ohmic contact resistance is not clear and unfortunately the timescales for this research did not allow for this to be pursued.

If the reduction in contact resistance is consistent across diamond material of different growth methods, and quality of hydrogen termination this process could prove very positive for FET production. Improving the contact resistance of FETs could be another method to further reduce the total on resistance of FETs fabricated on hydrogen terminated diamond. Combining both in-situ vacuum annealing and deposition of surface transfer doping oxides could lead to reduced channel and contact resistances in hydrogen terminated diamond FETs.

6.3 - MESFET with vacuum annealing and MoO_3 deposition – Sample B

The results in section 6.2 show that incorporating the surface transfer doping oxide MoO_3 can have positive impacts on both the channel sheet resistance and the contact resistance of TLM structures. The most straight forward method of incorporating these materials into hydrogen terminated diamond FETs is to blanket deposit them across the surface of the completed device. Therefore this is what was attempted first. To achieve this a series of FETs were fabricated on CVD material which was overgrown with a 5µm layer of CVD diamond with surface roughness of around 0.5nm Ra which was hydrogen terminated at 2kW plasma power density in situ at the end of growth. Growth and hydrogen termination were carried out by collaborators at Universite Paris 13.

Material	*Hydrogen termination*	*Sheet Resistance on arrival (in air)*
CVD substrate with epitaxial CVD overgrowth.	*2kW in situ after growth of 5µm CVD layer.*	*33.4kΩ/□*

Table 6.3.1– Material preparation prior to fabrication.

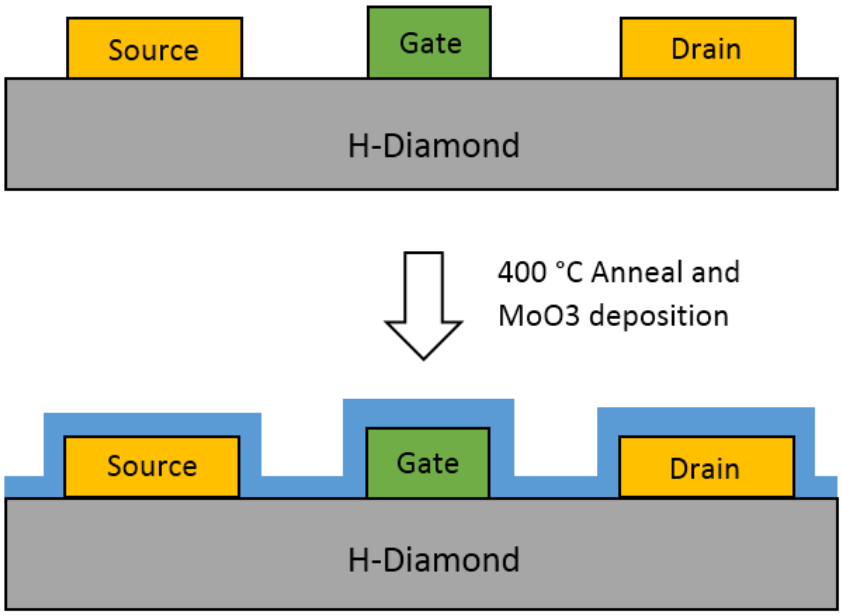

Figure 6.3.1 – FET structure with atmospheric adsorbates (top) and after anneal and 30nm MoO_3 deposition (bottom).

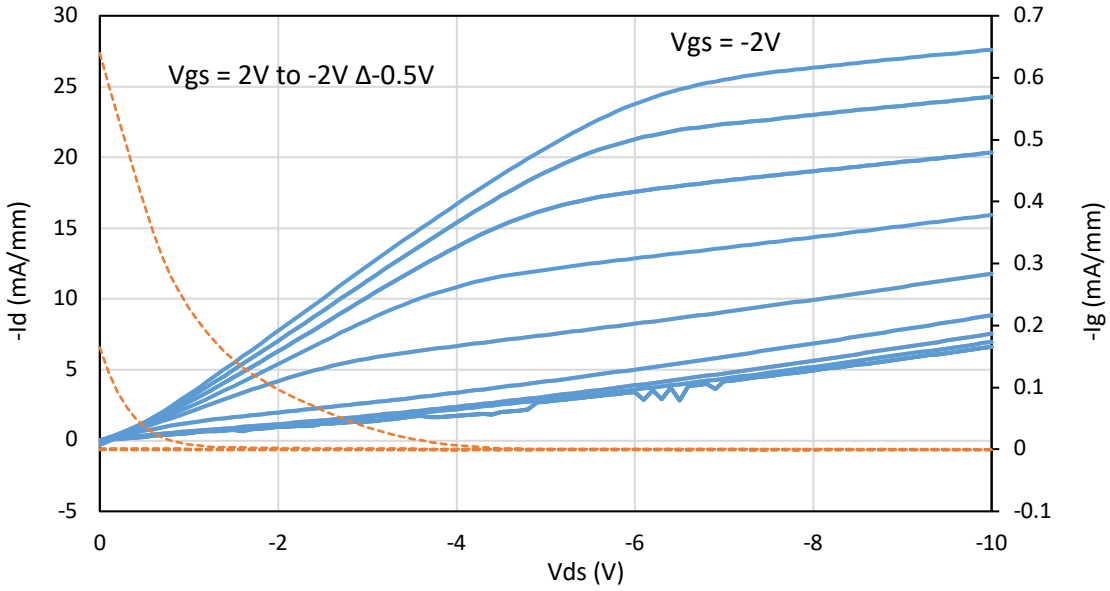

Figure 6.3.2 – Output characteristics for MESFET with atmospheric adsorbates fabricated on overgrown CVD layer, representative for FETs fabricated on sample A. Drain current is shown in blue, and gate leakage current is shown in orange.

It can be observed in the acquired output characteristics in *figure 6.3.2* that for positive gate voltages the FETs could not be turned "off". This is thought to be due to poorly isolated FETs, where current can flow outside the defined area of the FET controlled by the gate. The layout for all samples fabricated include "Isolation" test structures in order to assess

whether the isolation stage had worked sufficiently. The structures consist of 2 ohmic contacts 5µm apart. After 2 oxygen "ashes" to remove the hydrogen termination between the contacts of these test structures, the current continued to flow between the isolation structures as can be observed in *figure 6.3.3*. Below, *figure 6.3.4* shows a comparison between the results from this substrate, and the results from a well isolated substrate measured later in the course of the author's PhD. As the current could not be removed by repeated exposure to oxygen plasma it is thought that there are possible boron impurities in the epitaxial CVD layer which act as a low-level p-type doping.

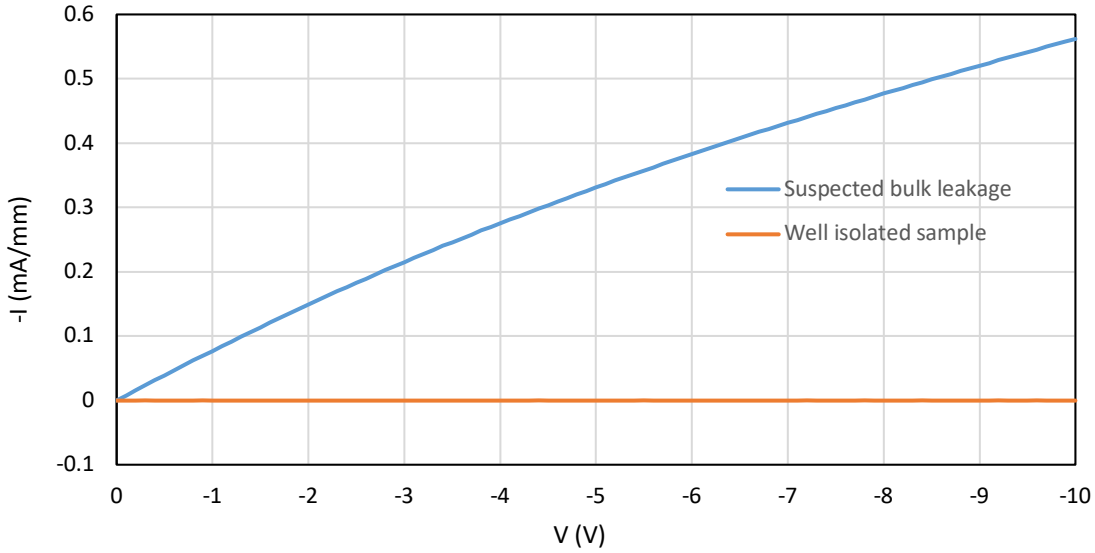

Figure 6.3.3 – Current across a 5um gap isolation structure after 2 oxygen ashes.

The measured FET drain current does not fully saturate at -10V V_d although this is most likely due to the suspected bulk leakage resulting in current paths through the diamond substrate which cannot be controlled by the gate, and continue to increase as the drain bias is increased. These current paths would either be in the bulk of the substrate or around the periphery of the gate structure.

The maximum drain currents measured of around -28 mA/mm in *figure 6.3.2* is poor compared to what has typically been reported for atmospheric diamond MESFETs, where groups have reported maximum drain currents typically between -100 and -300mA/mm [6.15, 6.16]. However, this was not unexpected for the high sheet resistance of the sample of around 33.4kΩ/□, whereas the reported literature shows material with sheet resistances of around 10-20kΩ/□ [6.6, 6.7].

It can be observed in *figure 6.3.2* that the gate leakage current begins to increase exponentially as the gate voltage is reduced to -2V. If the gate voltage is taken higher the

gate leakage would begin to dominate the drain current and could degrade the performance of the FETs.

Following demonstration of the atmospheric adsorbate FETs, the substrate was annealed in a vacuum of $2x10^{-6}$ mbar at 400°C for 1 hour prior to deposition of 30nm of the surface transfer doping oxide MoO_3 in order to remove residual atmospheric adsorbates from the surface as can be seen in *figure 6.3.1*. 400°C was chosen as this has been shown previously in literature to be sufficient to remove atmospheric adsorbates from the diamond surface prior to the deposition of surface transfer doping oxides. The deposition of MoO_3 was undertaken in order to improve the sheet resistance in the channel areas of the FETs.

After in-situ annealing and deposition of MoO_3 the sheet resistance as measured by VDP remained at around 34k Ω/□. This is not consistent with what has been reported in literature, however the carrier concentration has increased from $4.49x10^{12}/cm^2$ to $8.95x10^{12}/cm^2$ but there has also been a substantial decrease in mobility from 41 cm^2/Vs to 20 cm^2/Vs which has resulted in the sheet resistance remaining constant.

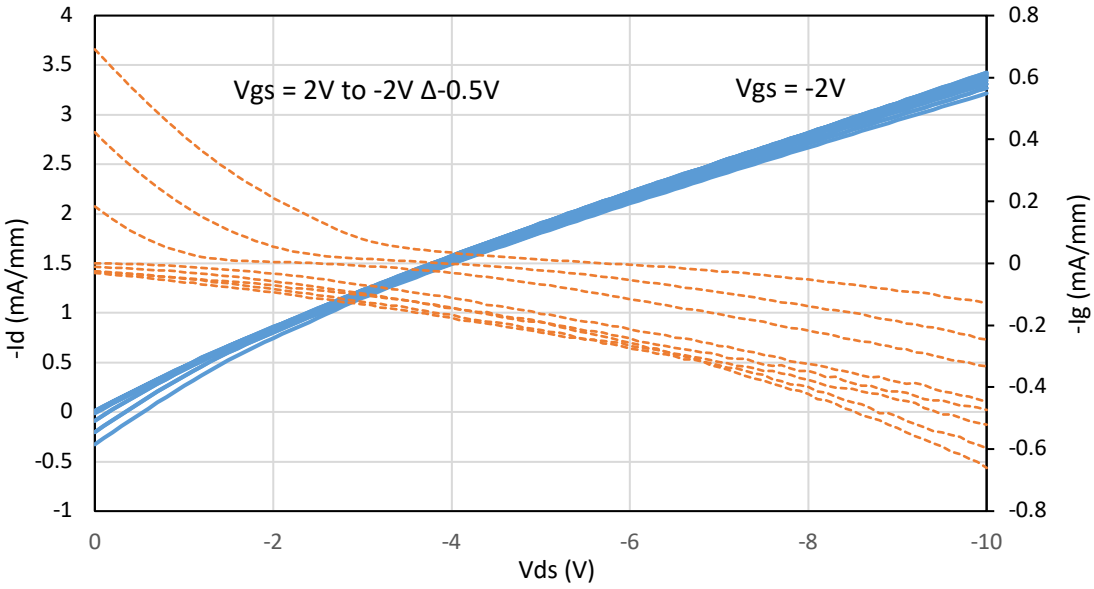

Figure 6.3.4 – FET operation after 400°C vacuum annealing and 30nm of MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

After annealing and MoO_3 deposition the performance of the FETs appeared to be irreversibly damaged. It can be observed in *figure 6.3.4* that the magnitude of the drain current has substantially degraded to -3.5mA/mm from -28mA/mm before annealing and MoO_3 deposition. The gate voltage also has little or no effect on the current flow between the source and drain contacts.

Comparing *figures 6.3.2* and *6.3.4* it can be observed that the magnitude of the gate leakage current has not changed by an appreciable amount from a maximum of -0.6mA/mm after in situ vacuum annealing and MoO_3 deposition. However there is significant gate leakage when a positive gate voltage is applied which was not present before annealing and deposition of MoO_3, this could be indicative of a change in the barrier of the Schottky gate contact.

From this initial experimentation it was unclear whether the FETs had been damaged by vacuum annealing at high temperatures, or the deposition of the surface transfer doping oxide MoO_3. Therefore another experiment was designed in order to assess which processing stage was responsible for the degradation in the FET performance.

6.4 MESFET with V_2O_5, and vacuum annealing with V_2O_5 – Sample C

Due to the unexpected results from the first produced MESFET it was decided to design an experiment to determine whether the degradation of device performance was due to the deposition of MoO_3, or the annealing of the surface prior to oxide deposition. To this end a series of MESFETs were be fabricated on a substrate using atmospheric adsorbates as a surface transfer doping medium and would be characterized. Following this half of the substrate would be masked by a shadow mask and 10nm of V_2O_5 deposited over half the substrate. V_2O_5 was chosen to be used in this case as literature suggests that without pre deposition annealing of the diamond surface V_2O_5 should provide more stable results than MoO_3, and provide the same surface transfer doping effects[6.17]. Following this the whole sample was vacuum annealed at 400°C and 10nm of V_2O_5 deposited across the entire sample. 10nm was chosen as there was occasionally difficulty making contact to the ohmic contacts through the 30nm of MoO_3 used previously. This experiment provides comparison of 3 situations, un-encapsulated and un-annealed FETs, encapsulated un-annealed FETs and encapsulated and annealed FETs.

Material	*Hydrogen termination*	*Sheet Resistance on arrival (in air)*
CVD	*2kW*	*170kΩ/□*

Table 6.4.1 – Material preparation prior to fabrication.

Measurement Method	*Sheet resistance (kΩ/□)*	*Mobility (cm^2/Vs)*	*Carrier Concentration /cm^2*
VDP	*170*	*201*	*$1.8x10^{11}$*

Table 6.4.2 – VDP results from substrate with atmospheric adsorbates

As mentioned previously, at the early stages of this research the author had access to little material for experimentation in terms of low sheet resistances (R_{sh} < 15kΩ/□) substrates. This substrate was optical grade CVD diamond sourced from element six and hydrogen terminated at a power density of 2kW by collaborators at Universite Paris 13, as opposed to the previous experiment in chapter 6.3 where there was an epitaxial layer grown on the substrate. This was to try to avoid the large background leakage observed in the previous experiment devices believed to be due to high levels of boron in the epitaxially grown layer. The VDP results showed an extraordinarily high sheet resistance of 170kΩ/□ and TLM results showed a non-ohmic response, and therefore the contact resistance could not be extracted. These values are likely indicative of the non-optimized hydrogen termination process used, which was improved later in the research.

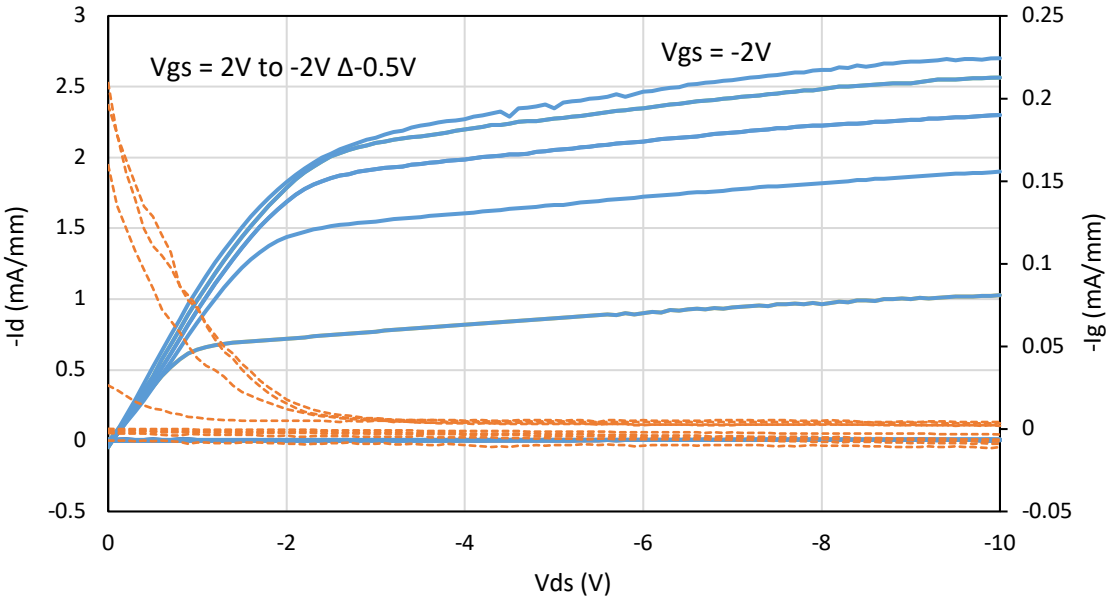

Figure 6.4.1 – 250nm gate length FET output characteristics after exposure to atmospheric adsorbates. Drain current is shown in blue, and gate leakage current is shown in orange.

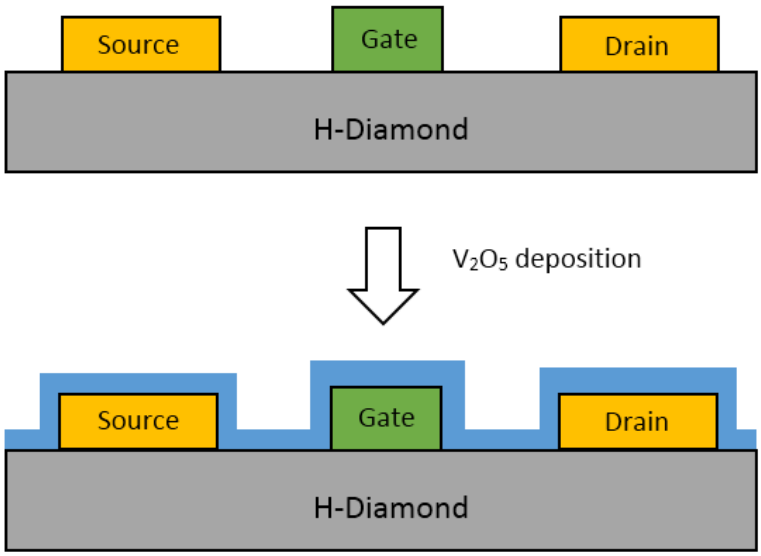

Figure 6.4.2– FET structure with atmospheric adsorbates (top) and after 10nm V_2O_5 deposition (bottom).

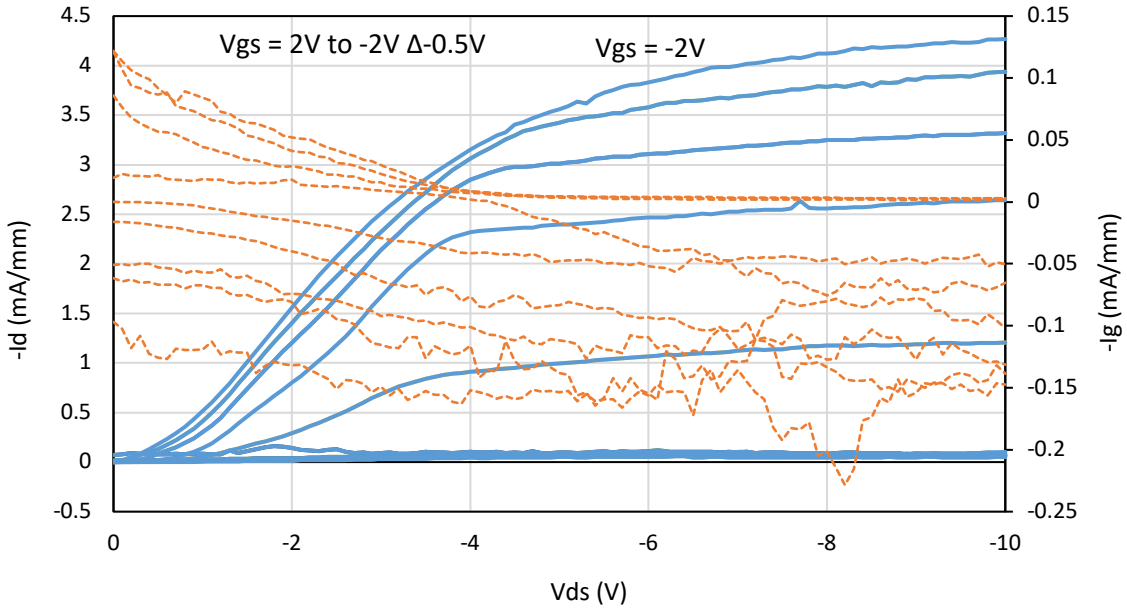

Figure 6.4.3 – 250nm gate length FET output characteristics after deposition of 10nm of surface transfer doping oxide V_2O_5 with no anneal. Drain current is shown in blue, and gate leakage current is shown in orange.

Measurement Method	*Sheet resistance (kΩ/□)*	*Mobility (cm^2/Vs)*	*Carrier Concentration /cm^2*
VDP	*37*	*93*	*$1.8x10^{12}$*

Table 6.4.3 – VDP results after 10nm of V_2O_5 deposition.

The above results provide an insight into "replacing" the atmospheric adsorbates with the surface transfer doping oxide V_2O_5 in a hydrogen terminated diamond FET. Unfortunately the quality of the hydrogen termination of this sample resulted in extremely high sheet resistance compared to what is typically reported in literature. Using atmospheric adsorbate doping the VDP structures had a sheet resistance of 170kΩ/□ as shown in *table 6.4.2*, this is higher than what has typically been reported in literature (10-20kΩ/□). This is thought to be due to the non-optimized hydrogen termination process used at this stage of the work, resulting in the surface of the diamond only being partially hydrogen terminated. Following deposition of 10nm of V_2O_5, the sheet resistance has reduced to 37kΩ/□ as shown in *table 6.4.3*. Although this is higher than what has been reported in literature, it is still encouraging as it emphasizes the improvement to the sheet resistance of the 2DHG associated with deposition of V_2O_5 on H:diamond surface.

The deposition of 10nm of the surface transfer doping oxide V_2O_5 on the substrate as shown in *figure 6.4.2* has had the immediate effect of increasing the magnitude of the maximum drain current of the FETs from -2.7mA/mm to -4.3mA/mm as can be observed by comparing *figures 6.4.1* and *6.4.3*, this would be expected from the increased concentration of carriers in the channel area of the FETs. Unfortunately, the low-field "linear" region in the IV response after oxide deposition shown in *figure 6.4.3* displays a non-ohmic response at the very low drain voltages (sub -1V), and thus on resistances could not be compared before and after oxide deposition. The gate leakage currents shown do not differ in orders of magnitude, although there is a marked increase in the gate current at high drain bias when the gate voltage is more positive.

After this preliminary comparison the entire substrate was annealed at 400°C in vacuum at a pressure of $2x10^{-6}$ mbar for one hour and 10nm of V_2O_5 was deposited in situ as shown in *figure 6.4.4*. This then allowed investigation into the effects of annealing and V_2O_5 deposition on the half of the substrate which was masked during the initial V_2O_5 deposition.

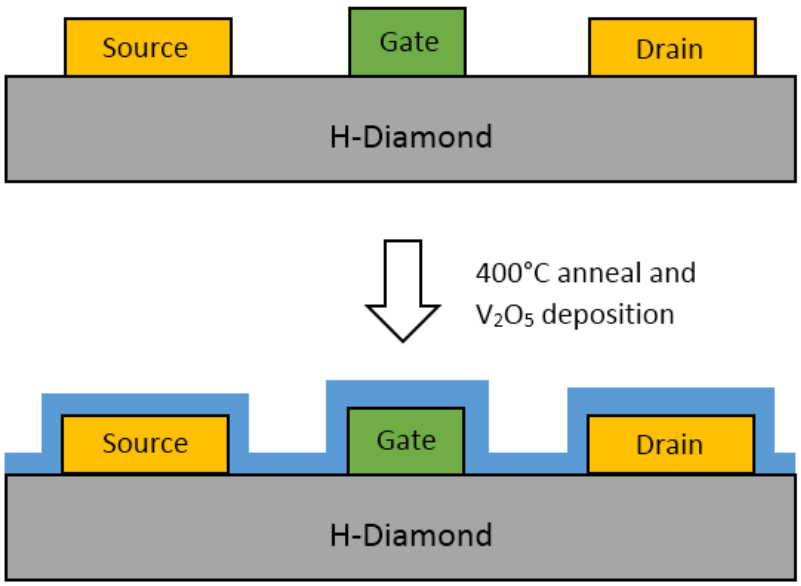

Figure 6.4.4 – FET structure with atmospheric adsorbates (top) and after anneal and 10nm V_2O_5 deposition (bottom).

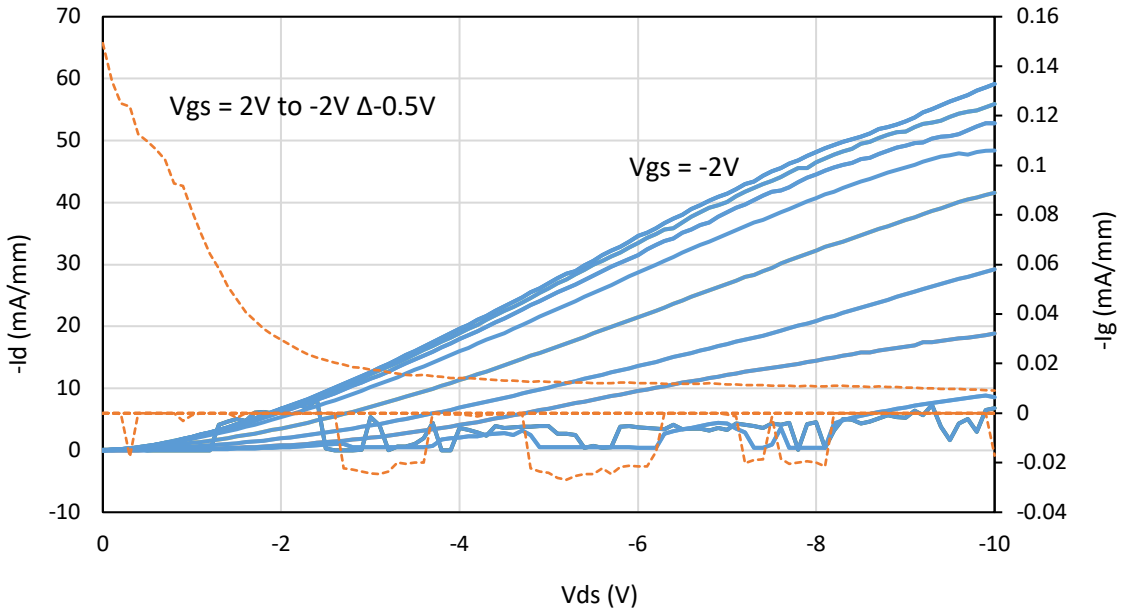

Figure 6.4.5 - 250nm gate length FET output characteristic measurement after annealing and 10nm V_2O_5 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

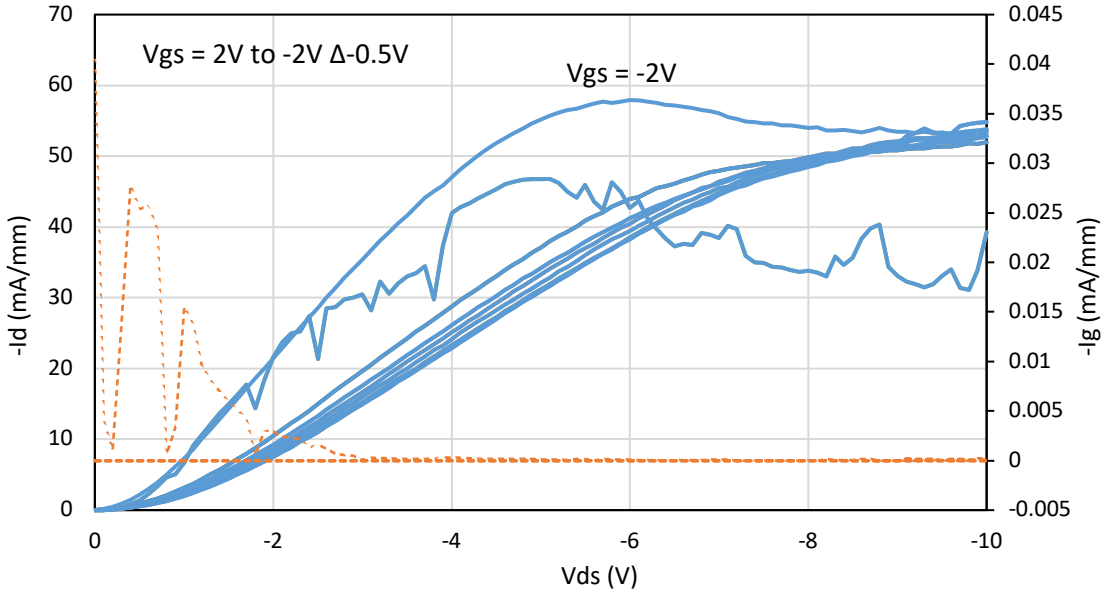

Figure 6.4.6 – 250nm gate length FET second output characteristic measurement after annealing and 10nm of V_2O_5 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

The results in *figures 6.4.5* and *6.4.6* provide an insight into the operation of diamond MESFETs using V_2O_5 and pre deposition annealing at 400°C. Unfortunately due to the method of masking the substrate the VDP data for this fabrication stage in unavailable.

It can be observed when comparing *figures 6.4.1* and *6.4.5* that the maximum drain current achieved has increased in magnitude from -2.5mA/mm to -60mA/mm. The increase is encouraging, and it is unfortunate that VDP and TLM results are not available to further investigate the increase in this case. The increase is more dramatic than what was observed when there was no anneal prior to deposition. This may imply the annealing stage is also contributing to improving the maximum drain current. This may be due to the annealing removing residual atmospheric adsorbates allowing the V_2O_5 to make full contact to the diamond surface channel.

The first output characteristic measurement after annealing and V_2O_5 deposition in *figure 6.4.5* showed transistor characteristics with maximum drain current changing for different gate voltages for the same drain voltage. However, as shown in *figure 6.4.6*, after repeating the output characteristic measurement the devices were damaged irreversibly and there is little or no change in drain current with different gate voltages at the same drain voltages. The output characteristics shown are representative for devices measured after annealing and show that the gates lose control over the channel after 1 output characteristic measurement.

The gate leakage current appears to decreases by an order of magnitude after annealing and the gate appears to have very limited control over the magnitude of current flowing between the source and drain. It is clear that the gate contact is not sufficiently engineered in order to survive the 400°C vacuum anneal required to maintain the stability of the 2DHG and improve the contact resistance and noted previously.

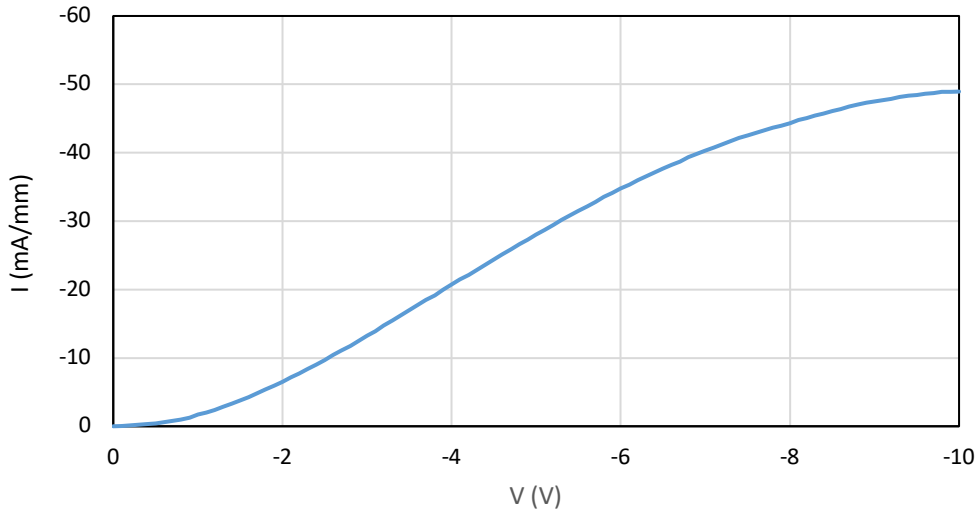

Figure 6.4.7 – 3µm TLM gap after annealing and 10nm of V_2O_5 deposition.

After annealing and V_2O_5 deposition the FET shown in *figure 6.4.6* seems to be stuck "on". The magnitude of the current of the 250nm gate length FET shown in *figure 6.5.5* is around 60mA/mm, which is very similar to the current of -50mA/mm acquired from a TLM with a gap size of approximately 3µm shown in *figure 6.4.7*. This is interesting as the total source drain gap of the 250nm FET shown should be approximately 2.25µm. This could imply that the gate is having little to no effect on the current flowing between the source-drain gap.

It is not presumed that an explanation for the mechanism of gate damage can be explained in this body of work and would require a great amount more investigation. Therefore it was decided the best course of continuing to research the full potential of integrating surface transfer doping oxides into hydrogen terminated diamond FETs was engineering the gate to maintain operation after high temperature vacuum annealing.

6.5 MESFETs with MoO_3 – Sample D

Although the comparison acquired from the previous sample in chapter 6.4 provided some insight into the effects of depositing surface transfer doping oxides on hydrogen terminated diamond FETs, it was unfortunate that the sheet resistance of the sample was extraordinarily high resulting in low currents prior to V_2O_5 deposition, and after. It was decided to

investigate how MoO_3 could be implemented into FETs without including annealing prior to surface transfer doping in order to ensure the maintained operation of the FET gate after surface transfer doping deposition. To this end after atmospheric adsorbate FETs have been characterized, 30nm of MoO_3 was deposited on top of the completed devices. 30nm was chosen as it has been suggested from preliminary work carried out by the author's colleague that thinner films provide less stable results without inclusion of a pre deposition 400°C vacuum anneal.

This substrate was optical grade CVD diamond sourced from Element Six. The diamond surface was etched with a tailored $Cl_2 + A_r$ and O_2 + Ar chemistry to remove surface and sub-surface damage, and then exposed to 2.6kW power density hydrogen plasma by collaborators at Universite Paris 13 after a two step-acid boil. This processes was developed in order to improve the quality of hydrogen termination.

Material	*Hydrogen termination*	*Sheet Resistance on arrival (in air)*
CVD Element six	*2.6kW power density.*	*20.6kΩ/□*

Table 6.5.1 – Material preparation prior to fabrication.

Measurement Method	*Sheet resistance kΩ/□*	*Contact Resistance (Ω.mm)*	*Mobility cm^2/Vs*	*Carrier Concentration $/cm^2$*
TLM	*19.7*	*7.8*	*n/a*	*n/a*
VDP	*20.6*	*n/a*	*208*	*$1.45x10^{12}$*

Table 6.5.2 – TLM and VDP results prior to MoO_3 deposition.

Measurement Method	*Sheet resistance kΩ/□*	*Contact Resistance (Ω.mm)*	*Mobility cm^2/Vs*	*Carrier Concentration $/cm^2$*
TLM	*n/a*	*n/a*	*n/a*	*n/a*
VDP	*13.5*	*n/a*	*152*	*$3x10^{12}$*

Table 6.5.3 – TLM and VDP results following 30nm MoO_3 deposition.

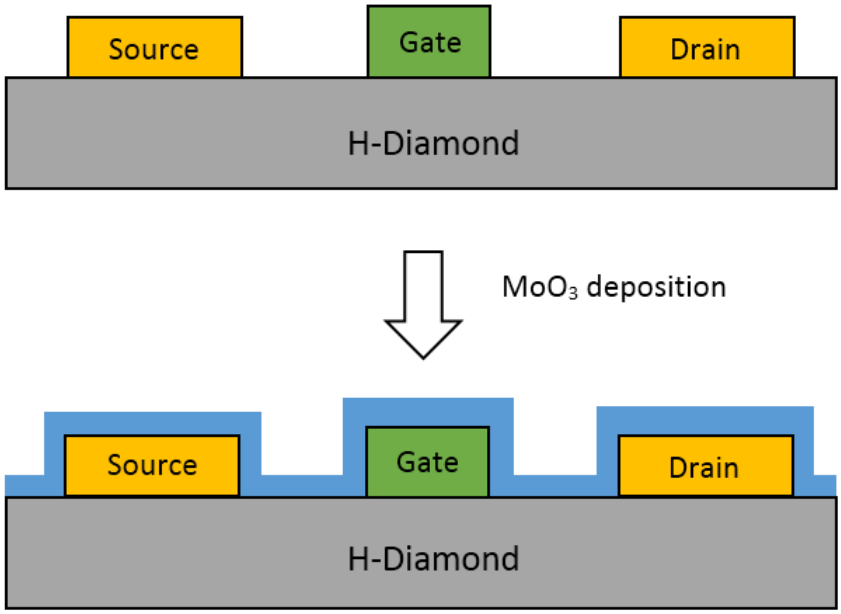

Figure 6.5.1 – FET structure with atmospheric adsorbates (top) and after anneal and 30nm MoO3 deposition (bottom).

During fabrication the isolation structures were tested as part of the processing. After an initial gold etch and oxygen etch it was observed that there was 0.12mA/mm of current flowing between the two isolation "pads" 5µm apart at -10V (*figure 6.5.2*).

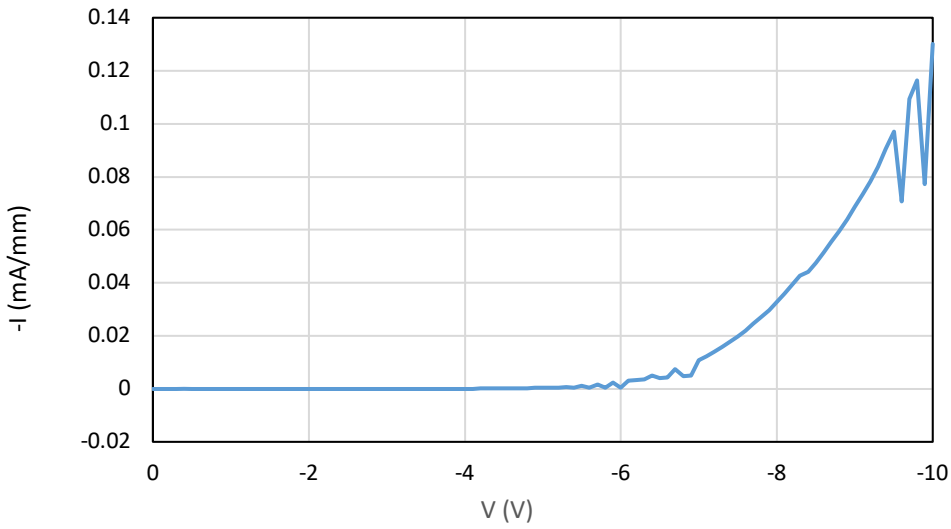

Figure 6.5.2 – Current flowing between isolation structures after first gold etch and oxygen ash.

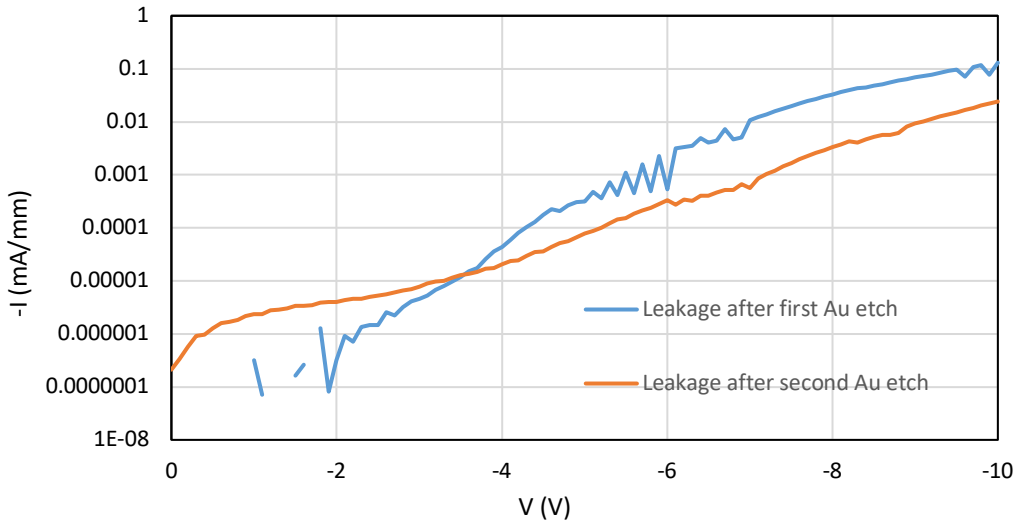

Figure 6.5.3 – Current flowing between isolation structures after first gold etch and oxygen ash (Blue) and after repeating the process (Orange).

In an attempt to improve the isolation of the structures the gold etch lithography and oxygen etch was repeated, with the time of gold etch increased from 40 seconds to 60 seconds to ensure all gold had been removed. The oxygen etch was also performed for 4 minutes increased from the normal 2 minute etch. After this there has been a decrease in the magnitude of the leakage current at -10V from -0.12mA/mm to -0.02mA/mm. At this point it was thought that the magnitude of the leakage would be low compared to the measured currents, and the main aim of this substrate was to investigate the effects of deposition of MoO_3 on the maximum drain currents and transconductance of the FETs. Therefore it was decided to continue with the fabrication of these FETs despite the high leakage current.

TLM, VDP and FETs were fabricated on the substrate and characterized electrically as discussed in chapters 4 and 5 using atmospheric adsorbates. Following this, 30nm of MoO_3 was deposited across the completed devices as shown in *figure 6.5.1*, which were then electrically characterized.

The VDP results in *table 6.5.2* showed a sheet resistance of 20.6kΩ/□ in air, which is better than what was achieved previously in this work and is closer to the values reported in literature of 10-20kΩ/□. This is due to the new optimized process of etching the diamond surface and using a 2.6kW power density hydrogen plasma for hydrogen termination as discussed in [6.8].

Comparing VDP results in *tables 6.5.2* and *6.5.3* shows a decrease in sheet resistance from 20.6kΩ/□ to 13.5kΩ/□ as would be expected after deposition of 30nm of MoO_3. Unfortunately, the TLM results obtained after deposition of 30nm of MoO_3 appear to be

non-ohmic in the low voltage regions of the current-voltage measurements. The sheet resistance and contact resistances cannot reliably be obtained from the non-ohmic TLM measurements after MoO_3 deposition and no comparison could be made.

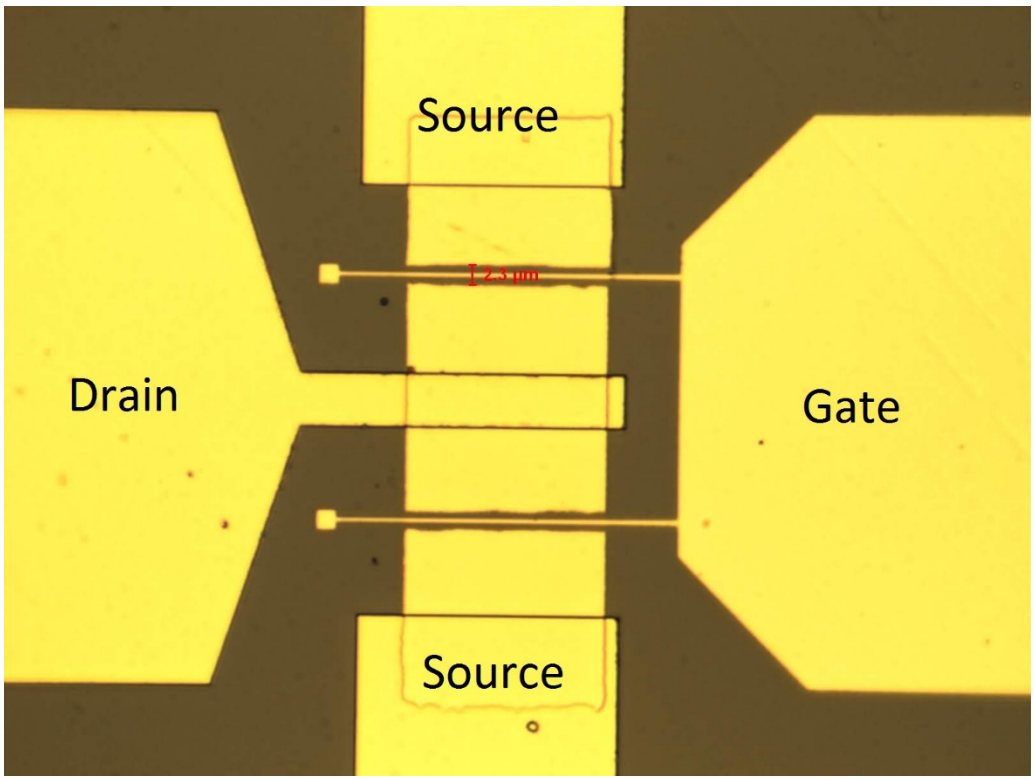

Figure 6.5.4 – Optical image of 250nm gate showing 2.3µm source-drain gap.

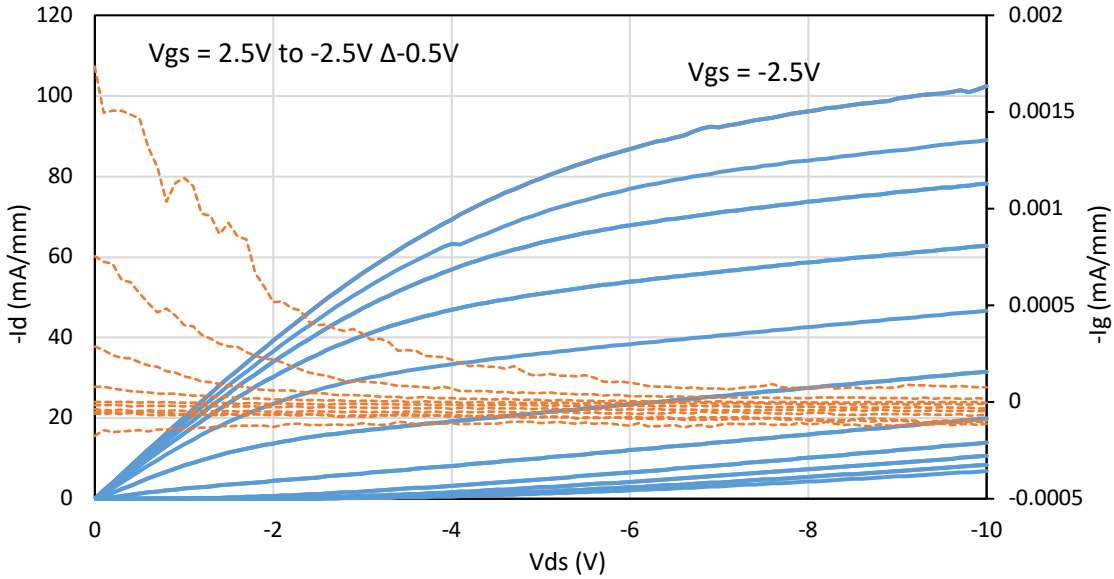

Figure 6.5.5 – Output characteristics of 250nm gate length prior to MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

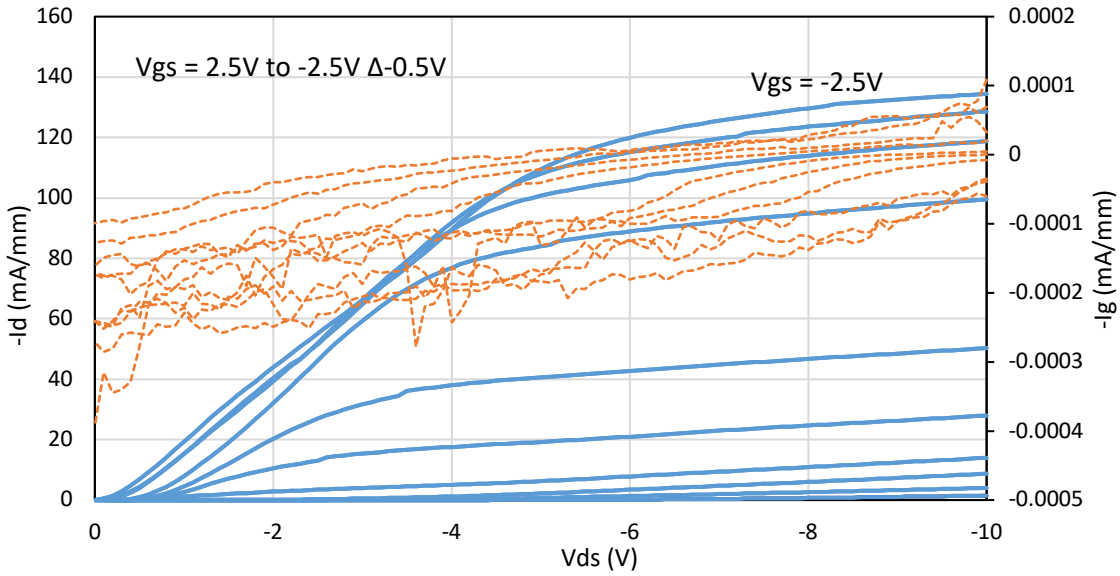

Figure 6.5.6 – Output characteristics of 250nm gate length after MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

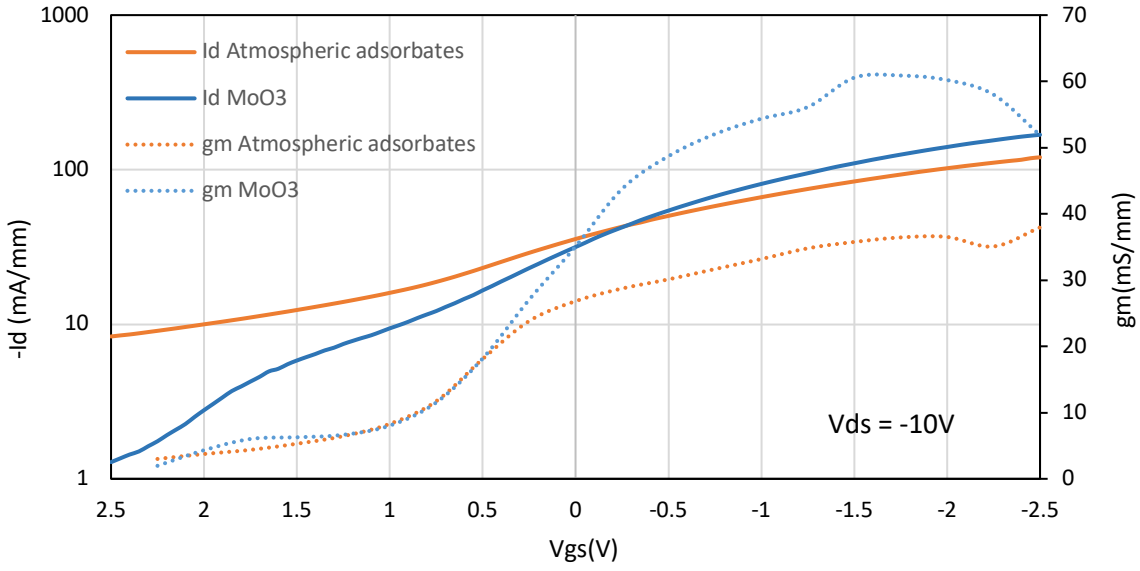

Figure 6.5.7 – Transfer characteristics and transconductance of 250nm gate length FET before and after MoO_3 deposition.

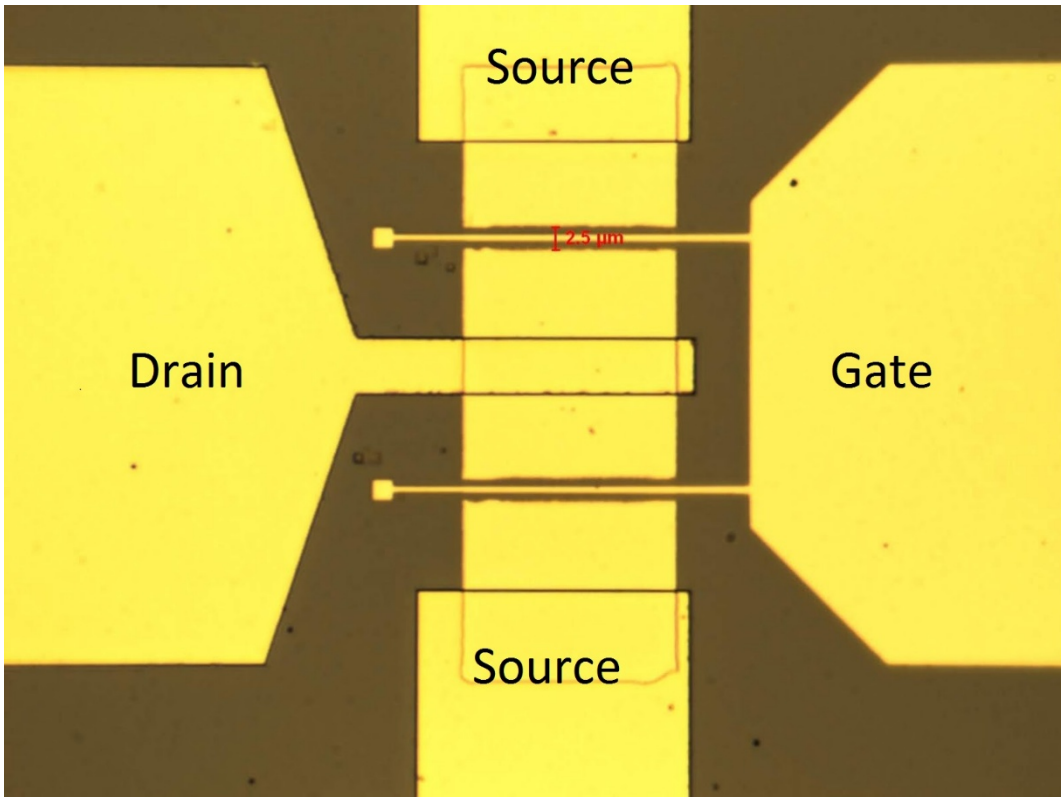

Figure 6.5.8 – Optical image of 500nm gate showing 2.5µm source-drain gap.

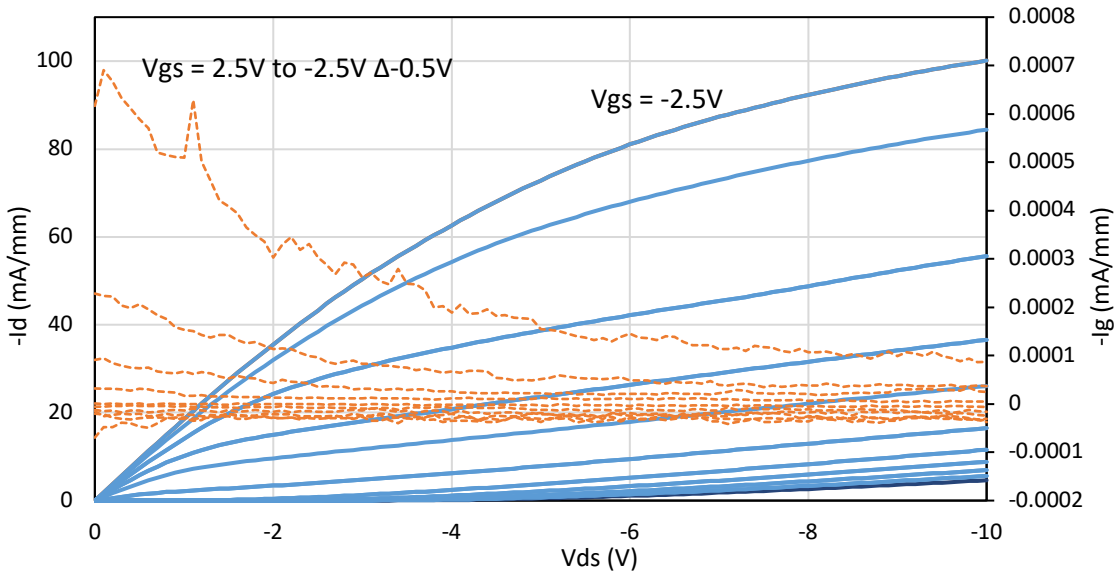

Figure 6.5.9 – Output characteristics for 500nm gate length FET prior to MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

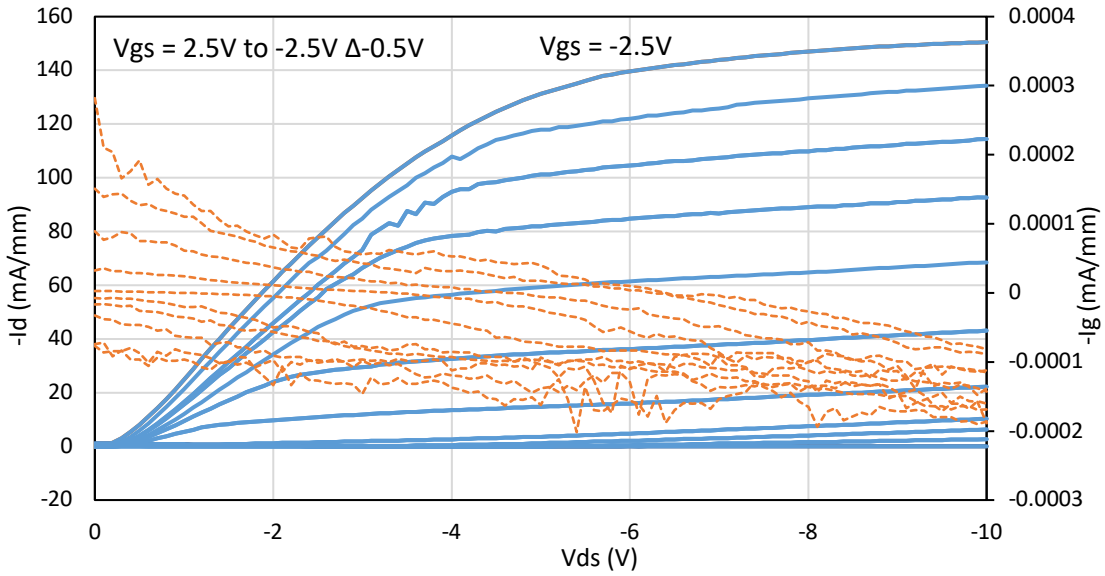

Figure 6.5.10 - Output characteristics for 500nm gate length FET after 30nm MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

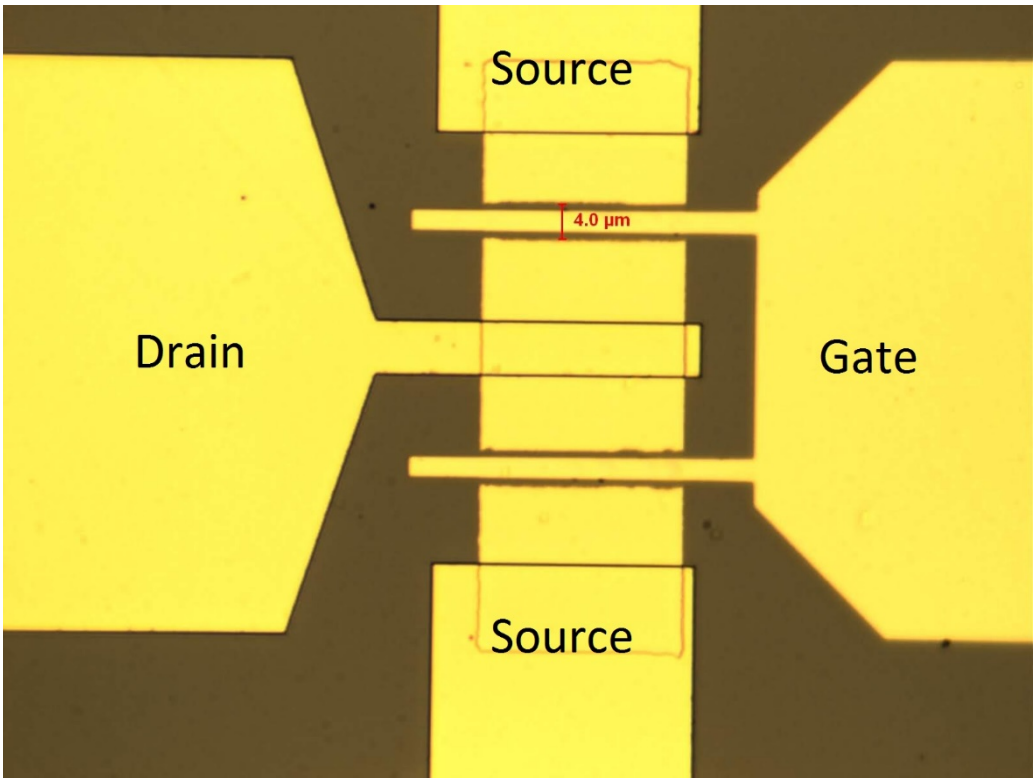

Figure 6.5.11 – Optical image of 2µm gate showing 4µm source-drain gap.

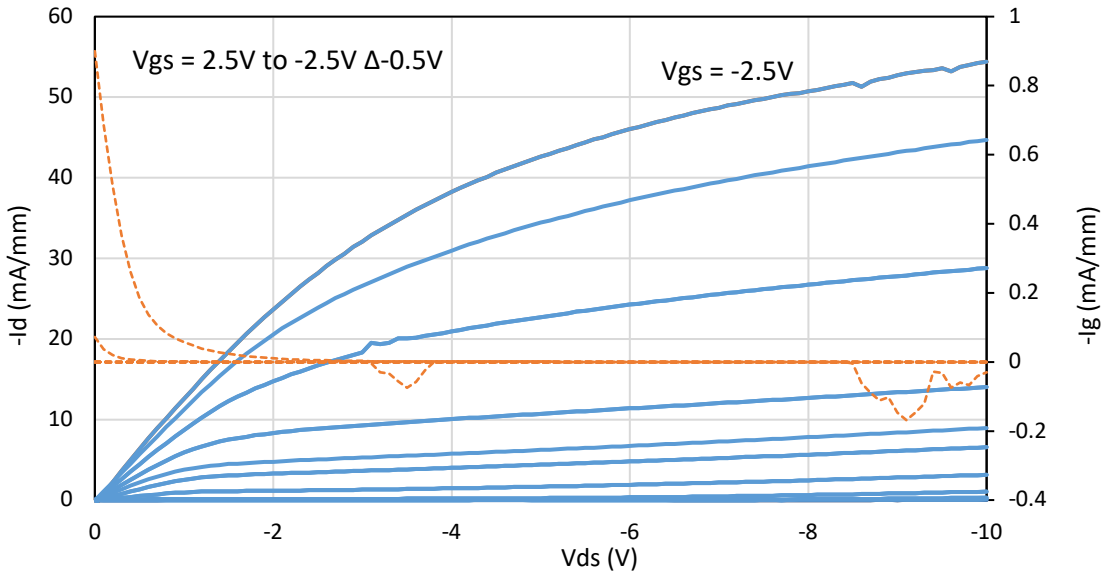

Figure 6.5.12 – Output characteristics for 2µm gate length FET prior to MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

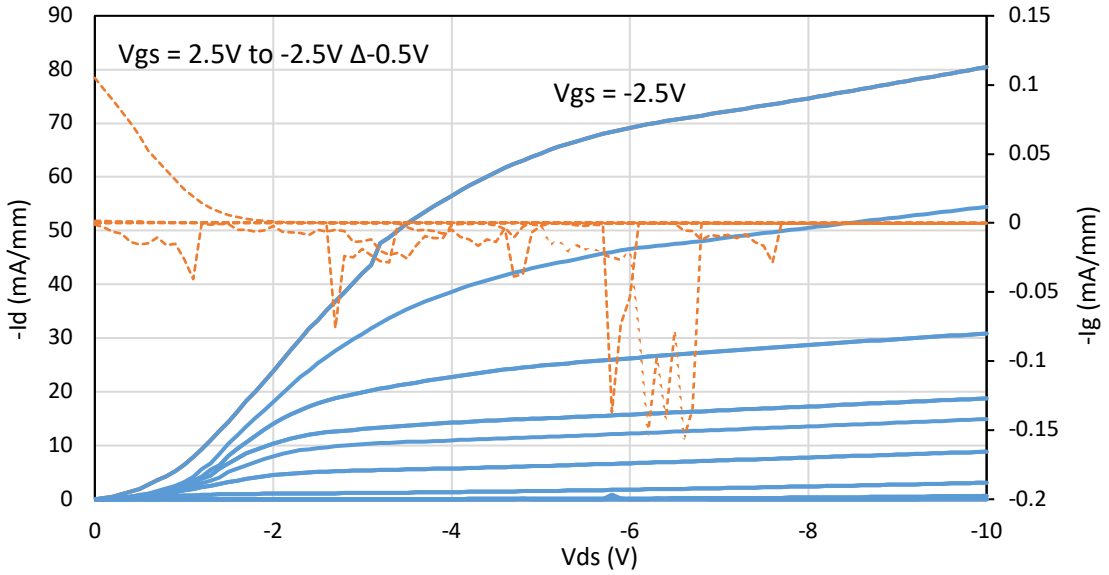

Figure 6.5.13- Output characteristics for 2µm gate length FET after to MoO_3 deposition. Drain current is shown in blue, and gate leakage current is shown in orange.

Gate length	*Source-Drain gap*	*Idmax pre MoO_3 (mA/mm)*	*Gm pre MoO_3 (mS/mm)*	*Idmax Post MoO_3 (mA/mm)*	*Gm Post MoO_3 (mS/mm)*	*R_{on} Pre MoO_3 (Ω.mm)*
0.25µm	*2.3µm*	*-102*	*35*	*-134*	*61*	*49.9*
0.5µm	*2.5µm*	*-100*	*32*	*-151*	*60*	*55.4*
2µm	*4µm*	*-54*	*16*	*-80*	*20*	*75.5*

Table 6.5.4 – Results of FETs measured before and after deposition of 30nm of MoO_3.

Unfortunately, the FETs could not be properly isolated by oxygen plasma so the off state performance could not be fully explored. This also resulted in the on/off ratio of the drain current being small at just 1-2 orders of magnitude. Usually the author would extract the threshold voltage at 0.1mA/mm as discussed in chapter 5, however as the currents could not be suppressed below this value the threshold voltage could not be extracted reliably.

From *figures 6.5.5* and *6.4.9*, it can be observed that prior to deposition of MoO_3 a 250nm gate length FET yielded a maximum drain current of -102mA/mm and a 500nm gate length FET showed a maximum drain current of -100mA/mm. This is lower than what has been reported for atmospheric MESFETs of similar dimensions shown in literature which have exhibited maximum drain currents as high as -360mA/mm, on material with a sheet resistance of 6.5kΩ/□ [6.16], which is lower than the sheet resistance of this sample where VDP measurements yielded a value of 20.6kΩ/□.

From *figures 6.5.6* and *6.4.10*, it can be observed that the magnitude of the maximum drain currents have increased to -134mA/mm for a 250nm FET and -151mA/mm for a 500nm FET after MoO_3 deposition. Although this does not reach the heights of what has been previously shown on hydrogen terminated diamond the improvement when compared to the same material prior to deposition is encouraging as it emphasizes how deposition of MoO_3 without pre-annealing can be used to increase the maximum drain current of hydrogen terminated diamond FETs.

The extrinsic transconductances for atmospheric adsorbate FETs were 35mS/mm for a 250nm FET and 32mS/mm for a 500nm FET as can be seen in *table 6.5.4*. This is lower than what has been reported for some of the best atmospheric adsorbate FETs of similar dimensions shown in literature which reach as high as 137mS/mm and 150mS/mm [6.2, 6.16]. However, this may be explained by the fact that extrinsic transcondtance is heavily

reliant on the channel and contact resistances of an FET. The values reported in literature are from substrates with sheet resistances of 11kΩ/□ and 6.5kΩ/□ and contact resistance as low as 5Ω.mm. Compared to the sheet resistance of 20.6kΩ/□ and contact resistance of 7.8Ω.mm for the substrate shown here.

From the figures in *table 6.5.4*, it can be observed that the extrinsic transconductance has increased to 61mS/mm for a 250nm FET and to 60mS/mm for a 500nm FET after deposition of MoO_3. Although these results do not surpass what has been shown for atmospheric adsorbate FETs it can be observed that including MoO_3 in the channel regions of FETs leads to increased extrinsic transconductance by reducing the sheet resistance in the channel area.

Although the on resistance could be extracted prior to the deposition of MoO_3, it could not reliably be extracted for comparison after deposition of MoO_3 due to the non-linear response in the low drain field region.

Although the results shown here do not exceed what has been achieved in the best FETs using atmospheric adsorbates as a surface transfer doping medium, the maximum drain current of -151mA/mm and transcondutances of around 60mS/mm acquired for these FETs after deposition of MoO_3 are higher than what has been reported for MoO_3 encapsulated MOSFETs in literature, which reported -100mA/mm maximum drain current and a peak transconductance of 35mS/mm. [6.4, 6.18].

By comparing figures *6.5.12* and *6.5.13*, it can be observed that for a 2µm gate length FET the maximum drain current magnitude has increased from -54mA/mm to -80mA/mm after deposition of MoO_3. The extrinsic transconductance has also increased from 16mS/mm to 20mS/mm as can be observed in *table 6.5.4*.

There is an evident trend that can be seen in that the "shorter" gate lengths (250nm and 500nm) provide the highest drain currents and highest extrinsic transconductances which can be observed by comparing figures in *table 6.5.4*. Due to the self-aligned gate process used in this work the source-gate and drain-gate separation should always be approximately 1µm. As the gate size increases the source-drain gap must also increase as can be seen from the optical images for the FETs in *figures 6.5.4*, *6.5.8* and *6.5.11*. For the "longer" gate length the improvement in the maximum drain current and transconductance is also reduced to only 26mA/mm and 4mS/mm respectively. This is most likely due to the MoO_3 deposition having no effect on the channel under the gate, which may become the dominant contributor to maximum drain current and extrinsic transconductance as the gate length increases.

The effect of deposition of the MoO_3 on the surface of the hydrogen terminated diamond without performing a pre-anneal is not always consistent. This may be due to a number of factors. One factor could be that if the hydrogen termination is not complete (some sites being oxygen terminated) there will be areas where surface transfer doping does not occur, and thus deposition of MoO_3 on these areas will have no effect. Another factor is that without performing an anneal on the surface of the diamond prior to deposition there will most likely be remaining atmospheric adsorbates on the surface which may be trapped at the interface between the hydrogen terminated diamond surface and MoO_3. This could inhibit the surface transfer doping between the diamond and MoO_3.

Although the FETs fabricated could not be fully explored due to the issues regarding contact to the channel in the low field regions, and the inability to isolate the sample by use of oxygen plasma to remove hydrogen termination, this set of FETs served to show the potential of depositing surface transfer doping oxide MoO_3 onto hydrogen terminated diamond FETs in order to improve the maximum drain current and transconductance of the fabricated FETs.

6.6 MESFET with V_2O_5 – Sample E

Material	*Hydrogen termination*	*Sheet Resistance on arrival (in air)*
CVD Element six	*2.6kW Power density*	*18kΩ/□*

Table 6.6.1 – Material preparation prior to fabrication.

The previously outlined attempts to include surface transfer doping oxides into hydrogen terminated diamond FETs showed the potential for including MoO_3 and V_2O_5 in the FET structure. However the results for V_2O_5 were acquired on a substrate with a high sheet resistance of 33.4 kΩ/□ and did not show the full potential for improvement of the 2DHG. Off-state characteristics which are important for high power applications could not be explored on the sample including MoO_3 due to the inability to isolate the material and therefore another experiment was undertaken in order to show the potential of V_2O_5 as a surface transfer doping oxide and to assess the effects of the deposition of surface transfer doping oxides may have on the off-state performance of the fabricated FETs. To this end, another set of FETs was fabricated and characterized using atmospheric adsorbates. Following this, the completed devices were encapsulated with 10nm of V_2O_5 with no pre deposition anneal.

This substrate was optical grade CVD diamond sourced from Element Six. The diamond surface was etched with a tailored $Cl_2 + A_r$ and O_2 + Ar chemistry to remove surface and sub-

surface damage, and then exposed to 2.6kW power density hydrogen plasma by collaborators at Universite Paris 13 after a two step-acid boil.

6.6.1 - DC Characteristics of Sample E

	Sheet resistance (kΩ/□)	*Contact Resistance (Ω.mm)*	*Carrier Concentration*	*Mobility*
Atmospheric Adsorbates	*7.2*	*4.7*	*$1x10^{13}$*	*79.5*
10nm V_2O_5	*5.2*	*3.7*	*$2x10^{13}$*	*59.9*

Table 6.6.1.1 – TLM and VDP results after fabrication to active level using atmospheric adsorbates, and after deposition of 10nm of V_2O_5.

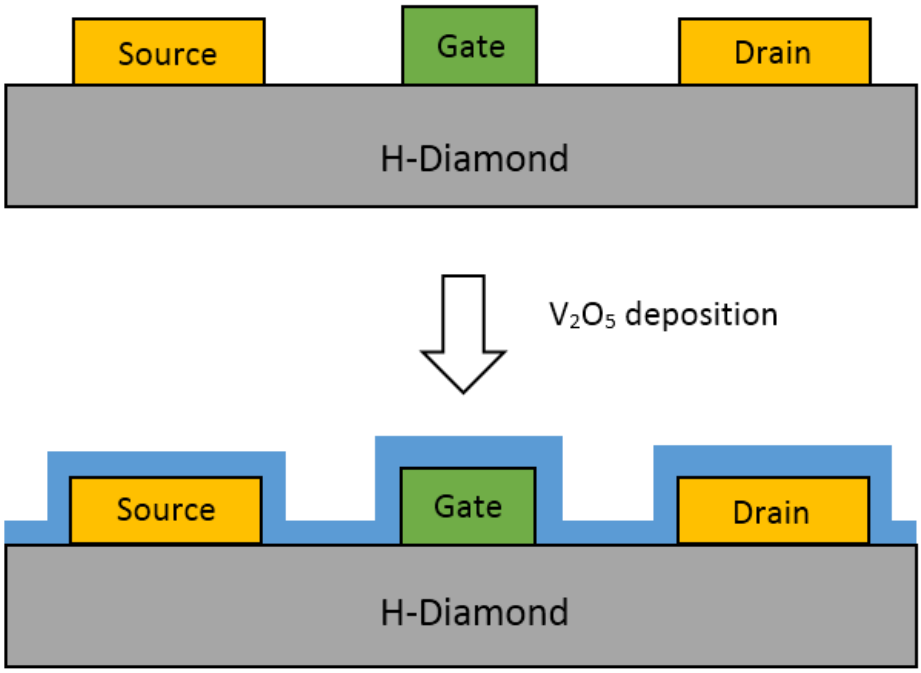

Figure 6.6.1.1– FET structure with atmospheric adsorbates (top) and after anneal and V_2O_5 deposition (bottom).

The sheet resistance measured by the Hall Effect prior to any fabrication was around 18KΩ/□. Which is close to what was observed for previous material prior to fabrication which showed sheet resistances between 20-30kΩ/□. However, from the fabricated VDP structures it can be seen in *table 6.6.1.1* that the measured sheet resistance is around 7.2kΩ/□ using atmospheric adsorbates. This may be due to the simple way in which the measurements are taken prior to fabrication, with the probes placed on the corners of the sample with no ohmic contacts providing an unreliable measurement compared to fabricated VDP structures, as the probes may not form a good ohmic contact.

As can be observed in *table 6.6.1.1*, after deposition of 10nm of V_2O_5 the sheet resistance has improved from 7.2kΩ/□ to 5.2kΩ/□. The contact resistances from TLMs shown in *table 6.6.1.1* also show a decrease in the contact resistance from 4.7Ω.mm to 3.7Ω.mm after deposition of 10nm of V_2O_5. The reduction in contact resistance of 1Ω.mm is a much smaller change than has been observed after annealing of the ohmic contacts previously where the contact resistance reduced from 30Ω.mm to 11.8Ω.mm in chapter 6.2. This is interesting as previous attempts to deposit the surface transfer doping oxides without annealing of the substrate surface showed non-linear TLM contacts at low voltages which was not observed here.

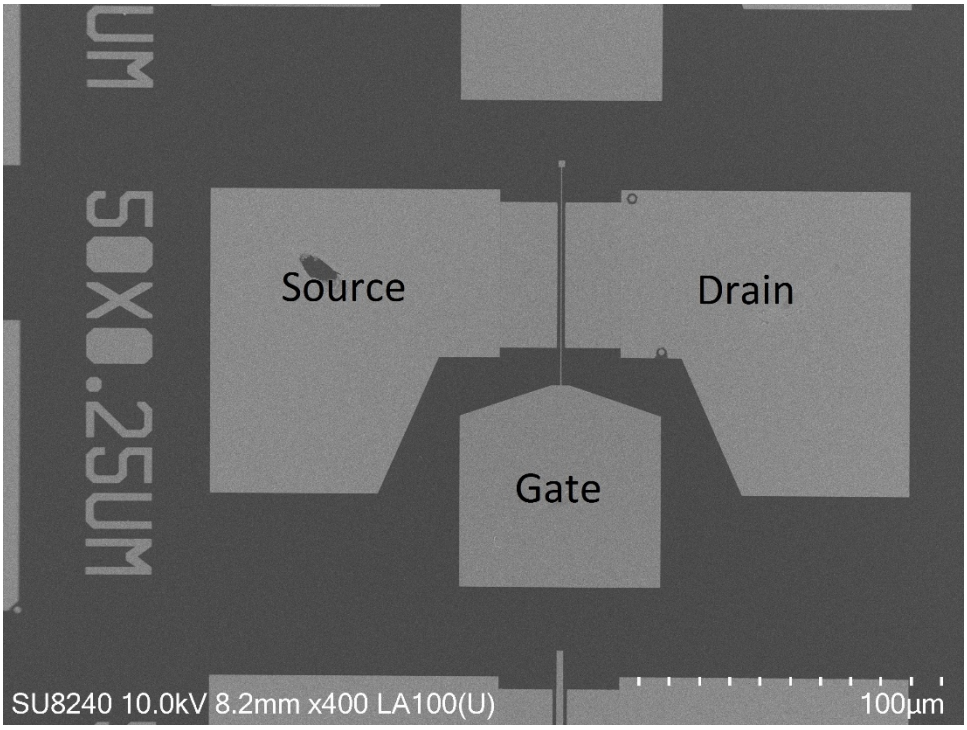

Figure 6.6.1.2 – SEM image showing complete 0.25µm gate length FET

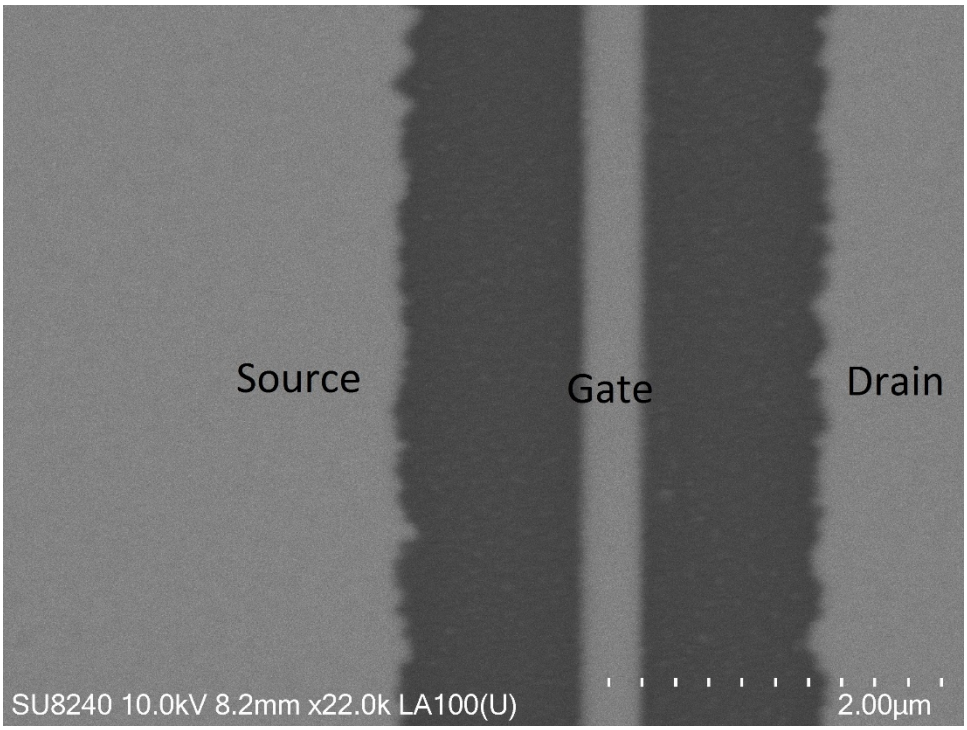

Figure 6.6.1.3 – SEM image showing source-drain gap of approximately 2.25µm and gate in the middle of approximately 250nm.

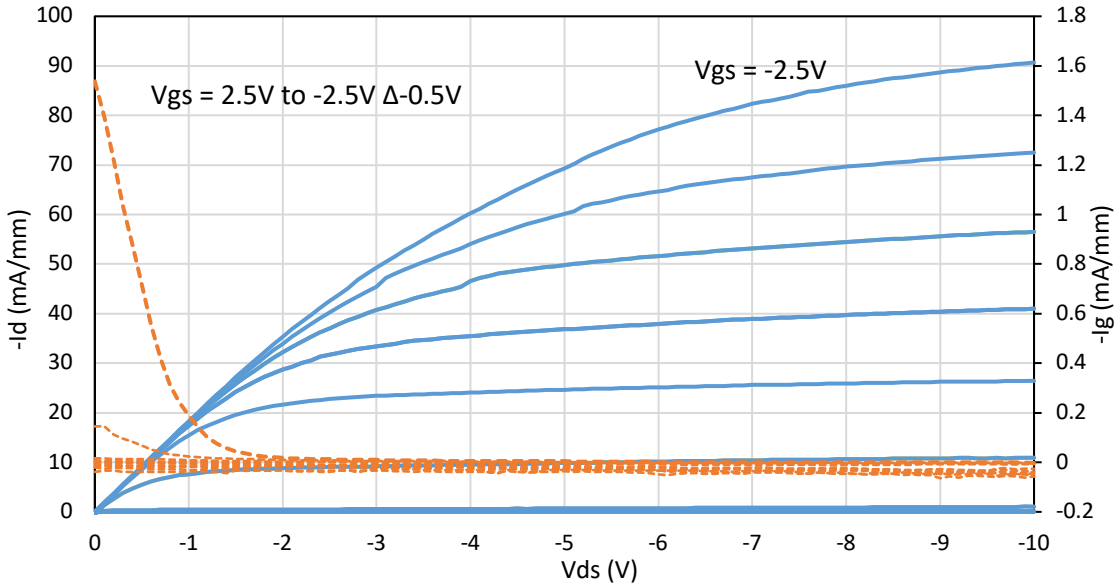

Figure 6.6.1.4- Output characteristics of 250nm gate length FET acquired using atmospheric adsorbate induced 2DHG. Drain current is shown in blue, and gate leakage current is shown in orange.

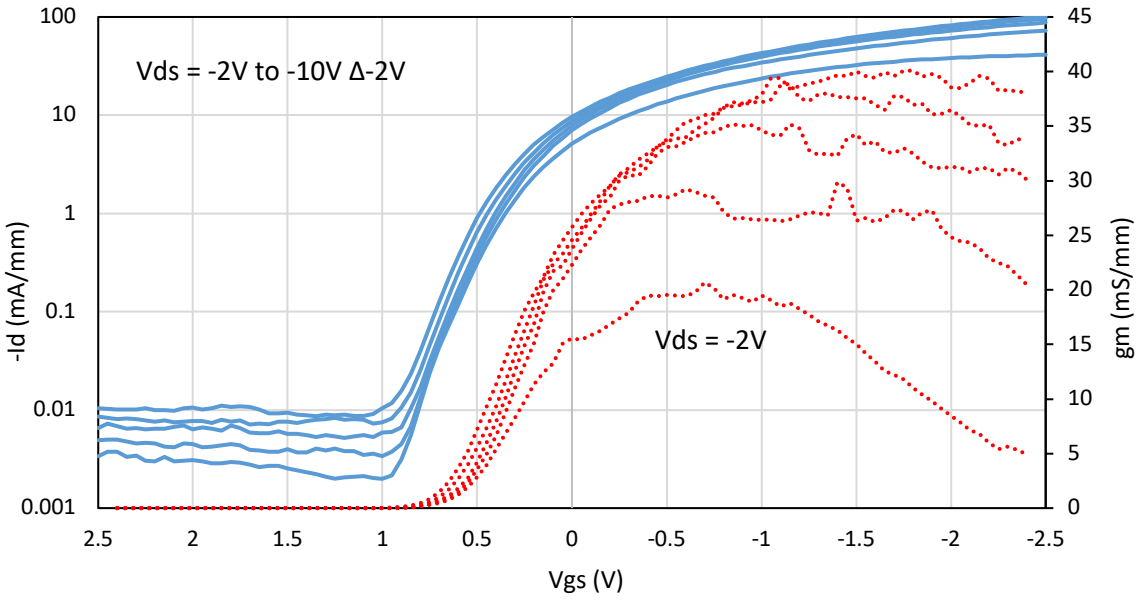

Figure 6.6.1.5– Transfer characteristics and transconductance acquired from 250nm gate length FET using atmospheric adsorbates as surface transfer doping medium. Drain current is shown in blue, and extrinsic transconductance is shown in dashed red.

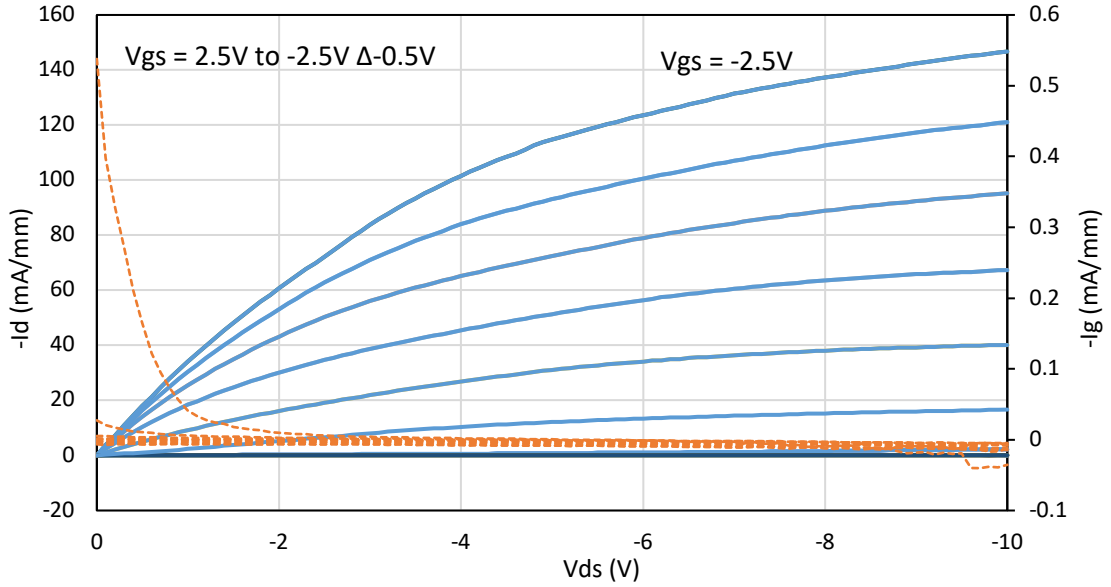

Figure 6.6.1.6 – Output characteristics acquired from 250nm gate length FET using 10nm of V_2O_5 as surface transfer doping medium. Drain current is shown in blue, and gate leakage current is shown in orange.

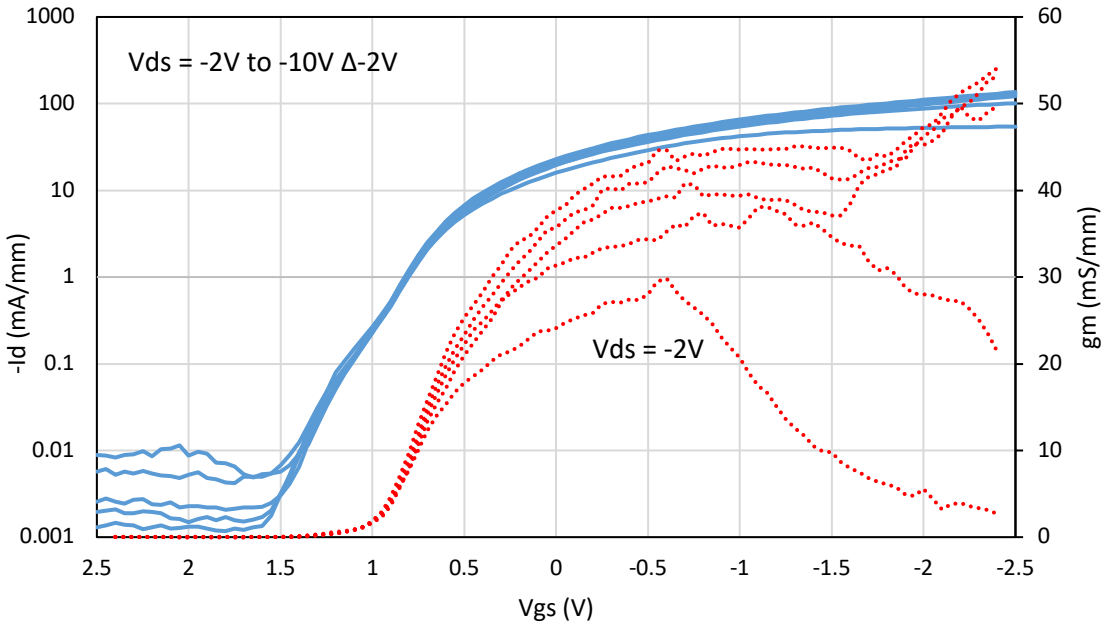

Figure 6.6.1.7 – Transfer characteristics and transconductance acquired from 250nm gate length FET using 10nm of V_2O_5 as surface transfer doping medium. Drain current is shown in blue, and extrinsic transconductance is shown in dashed red.

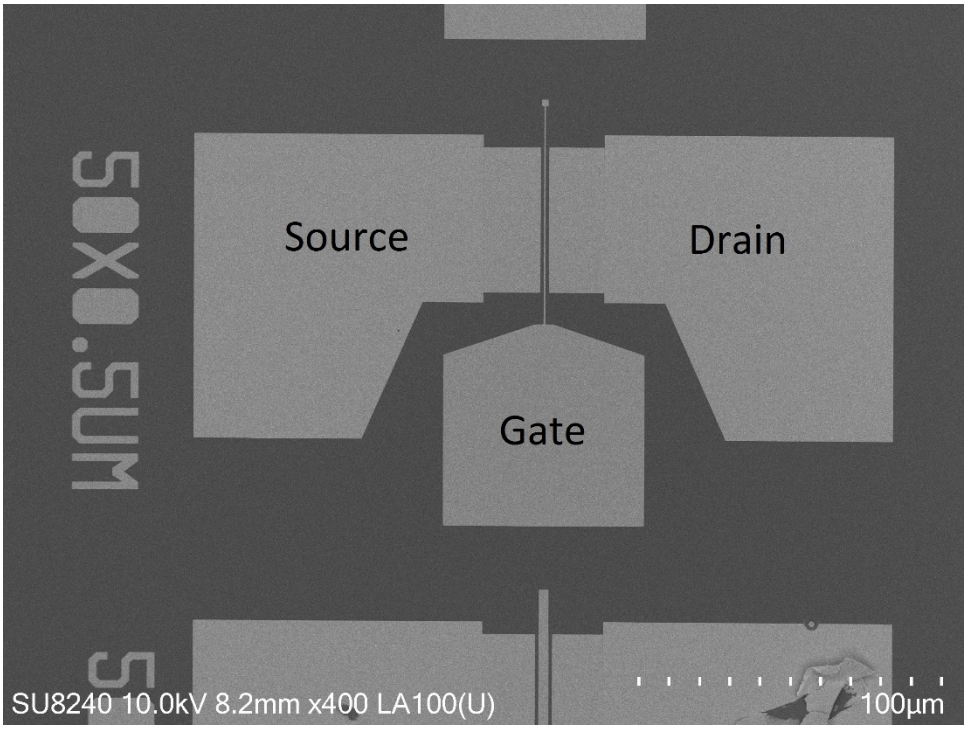

Figure 6.6.1.8 – SEM image showing complete 0.5µm gate length FET

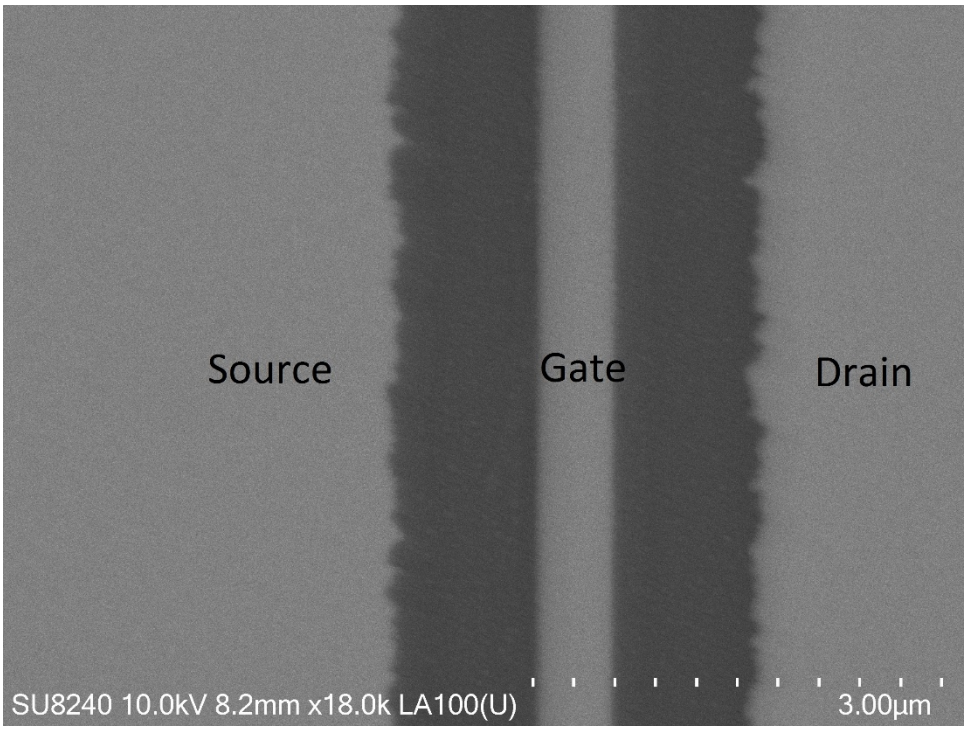

Figure 6.6.1.9 – SEM image showing source-drain gap of approximately 2.5µm and gate in the middle of approximately 500nm.

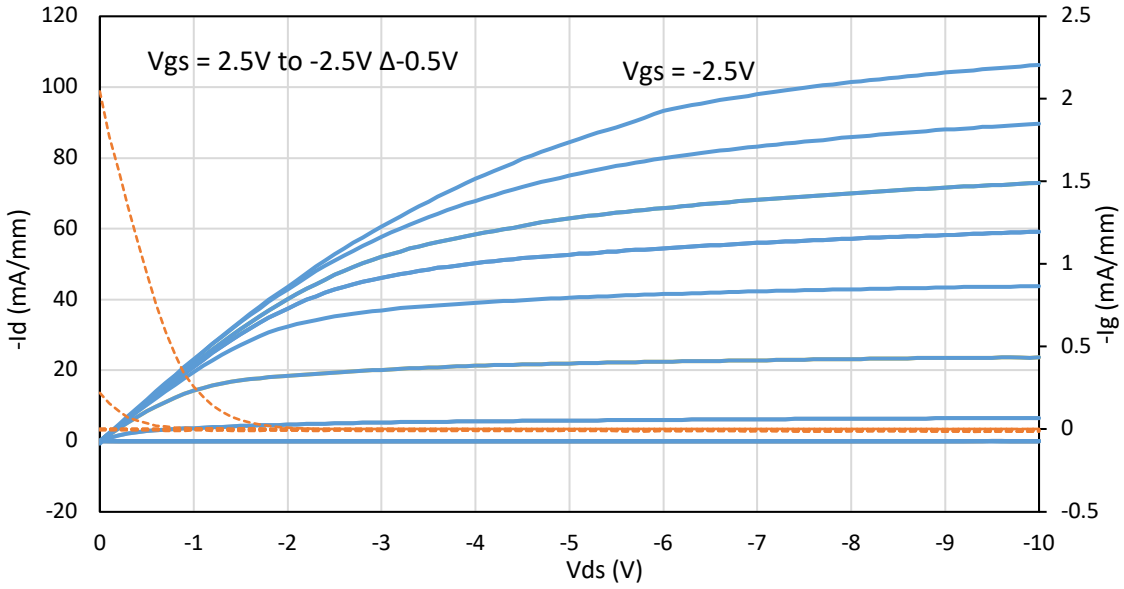

Figure 6.6.1.10 – Output characteristics of 500nm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and gate leakage current is shown in orange.

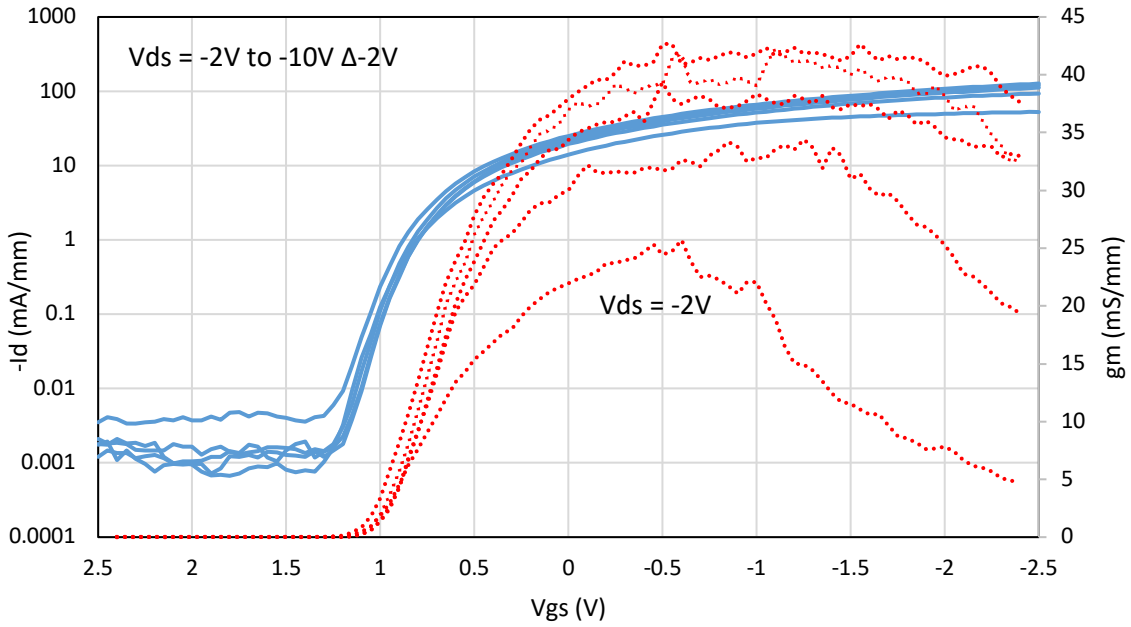

Figure 6.6.1.11 – Transfer characteristics of 500nm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and extrinsic transconductance is shown in dashed red.

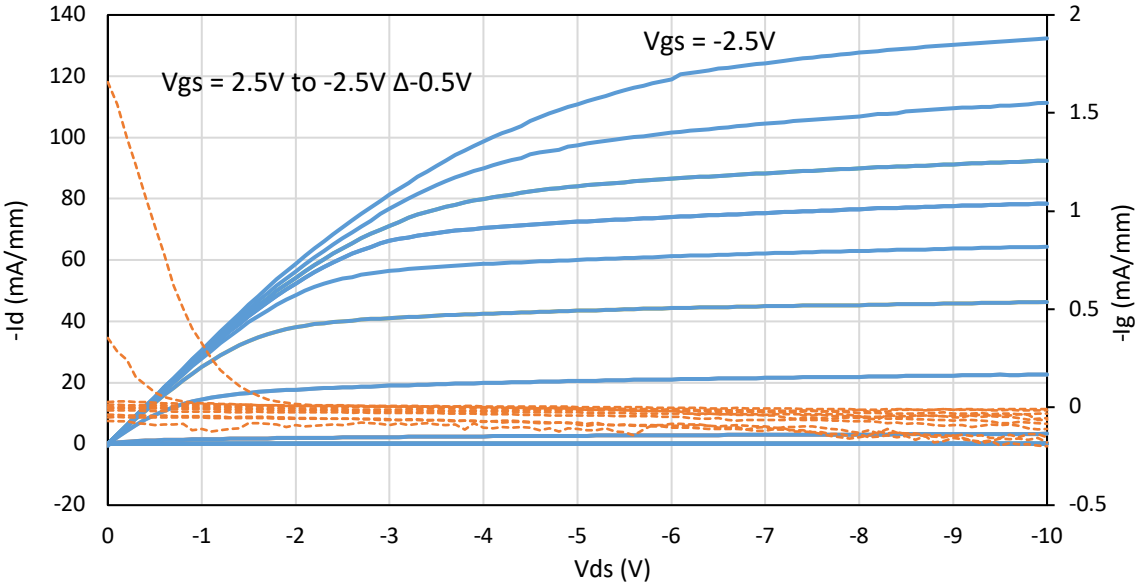

Figure 6.6.1.12 – Output characteristics of 500nm gate length FET after deposition of 10nm of V_2O_5. Drain current is shown in blue, and gate leakage current is shown in orange.

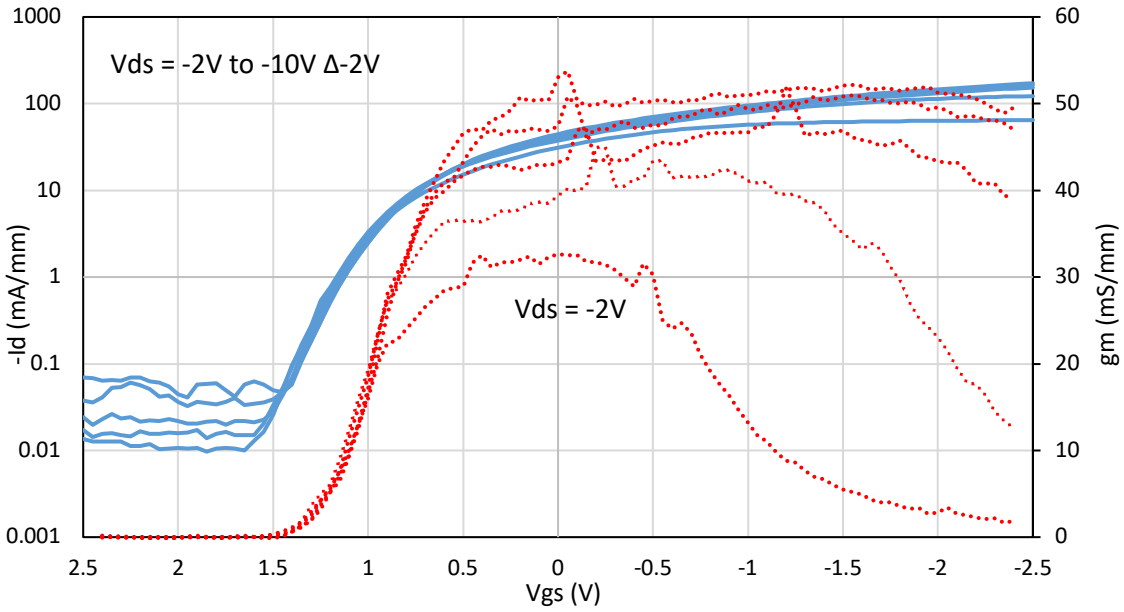

Figure 6.6.1.13 – Transfer characteristics of 500nm gate length FET after deposition of 10nm of V_2O_5. Drain current is shown in blue, and extrinsic transconductance is shown in dashed red.

In order to provide an overview of the acquired results from this experimentation tables *6.6.1.3* and *6.6.1.4* have been provided in order to show representative examples of some of the key parameters measured for FETs on this substrate before and after oxide deposition.

	Ron Ω.mm	*R_C Ω.mm*	*R_{CH} Ω.mm*	*R_{GCH} Ω.mm*	*R_s Ω/□*	*Idmax (mA/mm)*	*Igmax (mA/mm)*	*gm*	*gm **	*Vth (V)*	*Ion /Ioff*
Atmospheric adsorbates	*53*	*4.7*	*7.2*	*29.2*	*7200*	*-90*	*1.6*	*40*	*76*	*0.75*	*10^4*
V_2O_5	*39*	*3.7*	*5.2*	*21.2*	*5200*	*-135*	*0.5*	*45*	*73*	*1.25*	*10^4*

Table 6.6.1.3 – Key figures before V_2O_5 deposition for FETs with gate length 250nm.

	Ron Ω.mm	R_C *Ω.mm*	R_{CH} *Ω.mm*	R_{GCH} *Ω.mm*	R_s *Ω/□*	*Idmax (mA/mm)*	*Igmax (mA/mm)*	*gm*	*gm ∗*	*Vth (V)*	*Ion/Ioff*
Atmospheric adsorbates	*43*	*4.7*	*7.2*	*19.2*	*7200*	*-106*	*2*	*42*	*84*	*1*	10^4
V_2O5	*32*	*3.7*	*5.2*	*14.2*	*5200*	*-132*	*1.6*	*52*	*95*	*1.25*	10^3

Table 6.6.1.4 – Key figures after V_2O_5 deposition for FETs with gate length 500nm.

The calculated values in the tables above rely on two assumptions. That the contact resistances on the source and drain contacts are equal. And that the source-gate and drain-gate resistances are equal due to the symmetrical gate etch.

As can be observed in *figures 6.6.1.4* and *6.6.1.10*, prior to the deposition of V_2O_5 the maximum drain currents achieved were -90mA/mm for a 250nm gate length of FET and -106mA/mm for a 500nm gate length FET. This is comparable to what was achieved in the previous sub chapter for atmospheric adsorbate FETs which showed maximum drain currents of around -100mA/mm. This is lower than, but comparable to atmospheric adsorbate FETs reported elsewhere with a gate length of 200nm which showed maximum drain currents as high as -360mA/mm [6.16]. The sheet resistances of the material shown here (7.2KΩ/□) is similar to what was reported in the literature for an FET of -360mA/mm maximum drain current (6.5KΩ/□). This shows that the maximum drain current is heavily dependent upon the performance of the gate contact and not only the channel and contacts.

After deposition of V_2O_5, it can be observed from *figures 6.6.1.6* and *6.6.1.12* that the drain currents have increased in magnitude to -135mA/mm for a 250nm FET and -132mA/mm for a 500nm FET. These results are comparable to what was achieved for FETs of the same dimensions in the previous sub chapter using MoO_3 which showed maximum drain currents of -130 to -150mA/mm. This is another promising result showing that including V_2O_5 into hydrogen terminated diamond FETs can increase maximum drain current by increasing the carrier concentration in the channel. Again it should be noted that no pre-anneal was performed on these devices, the impact of which may further improve the doping performance of the V_2O_5 layer and associated device drain current.

The peak transconductance achieved prior to deposition was measured to be 40mS/mm for a 250nm FET and 42mS/mm for a 500nm FET. After V_2O_5 deposition this was marginally increased to 45mS/mm for a 250nm FET and 52mS/mm for a 500nm FET. Although these

results are lower than has been reported for hydrogen terminated diamond FETs of these dimensions, where values of 150mS/mm have been reported [6.16], the increase in these FETs after the deposition of V_2O_5 is encouraging.

The maximum drain currents of around -130mA/mm and peak extrinsic transconductances of 45-52mS/mm are lower than what has been reported for hydrogen terminated diamond FETs with V_2O_5 encapsulation in literature where a maximum drain current of -280mA/mm, and a peak extrinsic transconductance of 80mS/mm has been achieved [6.5]. This may be explained by the carrier concentration of the substrate in the reported literature being $6.8x10^{13}$ compared to $2x10^{13}$ achieved in this work. The higher value for extrinsic transconductance may also be explained by the reduced sheet resistance in the channel, with the reported literature showing a sheet resistance of 2.8kΩ/□ compared to 5.2kΩ/□ measured in this body of work. However the FET reported in literature also included V_2O_5 under the gate as a dielectric, which may have had the effect of drastically reducing the sheet resistance under the gate of the FETs. The inclusion of V_2O_5 under the gate also results in the gate voltage being able to be taken as far as -5.6V in the on state without significant gate leakage. This further emphasizes the need to engineer the gate of the FET structures further in order to improve high power performance.

After deposition of V_2O_5 on this substrate the sheet resistance and the contact resistances were 5.2KΩ/□ and 3.7Ω.mm respectively. This is better than the material demonstrated in chapter 6.5 by deposition of MoO_3, which had a sheet resistance and contact resistance of 13.5K Ω/□ and 7.8Ω.mm respectively. However the maximum drain currents achieved were in the region of 130mA/mm for the V_2O_5 sample and 130-150mA/mm for the MoO_3 sample. This further emphasizes that the maximum drain currents are dependent on the performance of the gate contact, not only the channel area.

As can be observed from *tables 6.6.1.3* and *6.6.1.4*, prior to oxide deposition the threshold voltages of the FETs were consistently around 0.75V-1V, however after deposition there has been a shift to around 1.25V for both the 300 and 500nm gate length FETs measured. The fabricated FETs are therefore depletion mode prior to, and after deposition of V_2O_5. As discussed in chapter 5, the threshold voltage has been defined as the gate voltage at which the drain current exceeds -0.1mA/mm at -10V drain bias. As the V_2O_5 was deposited on top of the gate it was not thought it would have any effect on the gate's ability to accumulate charge at the interface.

As has been discussed previously in chapter 5, the "static" on resistance is the inverse of the gradient of the drain current in the linear region of the output characteristics. The resistances

which constitute R_{on} can be seen in *figure 6.6.1.14*. The on resistance could not be calculated for the previously fabricated MESFETs after deposition of 30nm of MoO_3 due to the non-linear response of the output characteristics in the low field region. The response of the FETs shown here after 10nm of V_2O_5 has remained linear in the low field regions, thus a comparison can be made for the on resistance of the FETs before and after deposition of 10nm of V_2O_5.

$$R_{ON} = 2R_C + 2R_{CH} + R_{GCH} \qquad \textit{equation. 6.6.1.1}$$

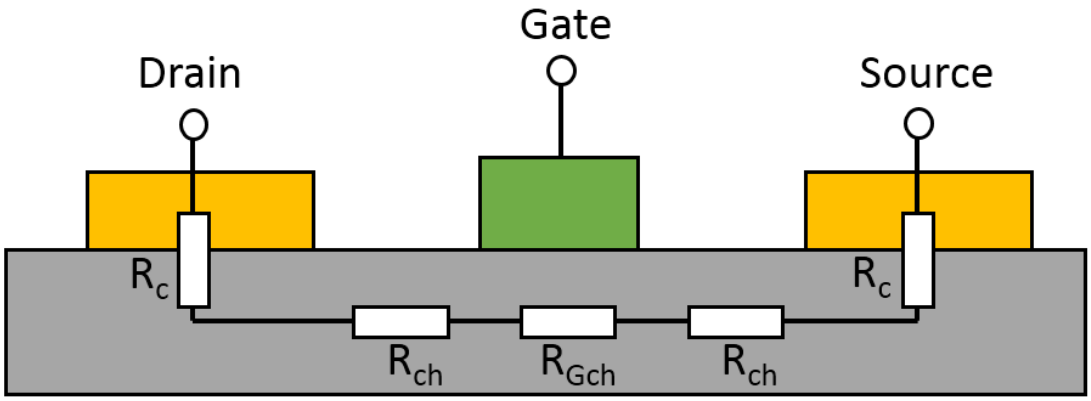

Figure 6.6.1.14 – Simplified FET model showing series resistances R_c, R_{ch}, and R_{Gch} in the linear operation region which make up R_{on}.

The total on resistance prior to deposition was 53Ω.mm and 43Ω.mm for the 250nm FET and 500nm FET respectively. Contact resistances and channel resistances should be identical for both gate lengths due to the self-aligned gate process. After deposition of 10nm of V_2O_5 it was measured that a 250nm FET had an on resistance of 39Ω.mm and a 500nm FET had an on resistance of 32Ω.mm. It can be seen that the on resistances of the FETs has consistently reduced after deposition of V_2O_5 as would be expected for the reduction in resistance in the channel area.

The contact resistance has reduced from 4.7Ω.mm to 3.7Ω.mm by deposition of V_2O_5 as calculated from TLM results, therefore the change in total on resistance should be mostly attributed to the reduced resistance in the channel areas, which has reduced from 7.2Ω.mm to 5.2Ω.mm. However this does not appear to be the case from the calculated values where the reduction in resistance under the channel has been calculated using *equation 6.6.1.1* as 8Ω.mm for a 250nm FET and 5Ω.mm for a 500nm FET. The V_2O_5 was deposited across the top of the gate and should have no effect on the gate-hydrogen terminated diamond interface, and the sheet resistance under the gate. This observed reduction may be due to a number of

factors such as; varying gate performance between FETs or changes due to repeated measurements on devices as will be discussed in the following subchapter.

Intrinsic and extrinsic transconductance are both important metrics for high power FETs. The extrinsic transconductance can be calculated as the rate of change of drain current with respect to gate voltage from the measured transfer characteristics. Intrinsic transconductance can be calculated using the equation below.

$$g_m^* = \frac{g_m}{1 - g_m R_{ch} R_c} \qquad \textit{equation. 6.6.1.2}$$

The intrinsic transconductances have been calculated using *equation 6.6.1.2*. With atmospheric adsorbates the intrinsic transconductance was calculated to be 76mS/mm for a 250nm FET and 84mS/mm for a 500nm FET. This decreased to 73mS/mm for a 250nm FET and increased to 95mS/mm for a 500nm FET after deposition of V_2O_5. As discussed in chapter 2 the intrinsic transconductance should only account for the area under the gate as it excludes the contributions from the contact and channel resistances. Therefore the intrinsic transcondutance should not be affected by the deposition of the surface transfer doping oxide V_2O_5. For the 250nm FET shown here there is only a difference of 3mS/mm between the intrinsic transconductance for an atmospheric adsorbate FET and V_2O_5 FET. For a 500nm FET there is a larger difference of 11mS/mm for an atmospheric adsorbate and V_2O_5 FET. There is most likely variation between FETs and due to degradation from repeated measurement which will be discussed in more detail in chapter 6.6.2.

The peak intrinsic transconductance is calculated to be 76mS/mm for a 250nm FET prior to deposition of V_2O_5. This is lower than, but close to the peak intrinsic transconductance of a 250nm MESFET reported in literature of 97mS/mm [6.12]. This may imply that the gate contact on this substrate is not optimal and could be further engineered by investigating using alternative fabrication methods and materials in the future to provide better performance.

Due to the variable nature of the FETs utilizing surface transfer doping it is therefore difficult to draw an exact story of what is happening with regards to the improvement of the FETs. However from the results it can be seen that there is a clear trend of decreased on resistance, increased maximum drain current and increased transcondutance after V_2O_5 deposition when compared to the results acquired from atmospheric adsorbates. These results further emphasize the potential of incorporating surface transfer doping oxides into hydrogen terminated diamond FET technology.

6.6.2 - Repeated measurements on Sample E

As one of the main drawbacks of the atmospheric adsorbates is the associated instability, replacing the atmospheric adsorbates with a surface transfer doping oxide was envisioned to improve operational stability.

In order to assess this change, first a number of atmospheric adsorbate FETs had their full output characteristics measured 5 times to assess any change in the drain current and on resistance. Below in *figure 6.6.2.1* each sweep of the drain voltage with -2.5V applied to the gate can be seen.

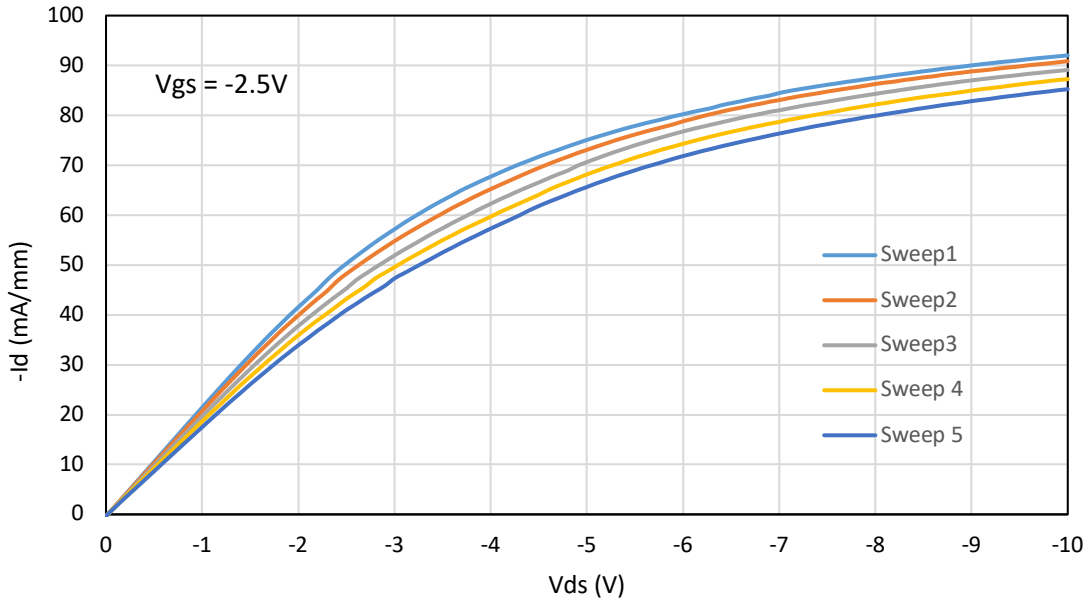

Figure 6.6.2.1 – Output characteristics at -2.5Vg repeated. 8% reduction for a 250nm gate length FET using atmospheric adsorbates.

Following this, the output repeated characteristic measurements were performed on an FET of the same gate length after deposition of 10nm of V_2O_5 without pre deposition annealing and the results are shown in *figure 6.6.2.2*.

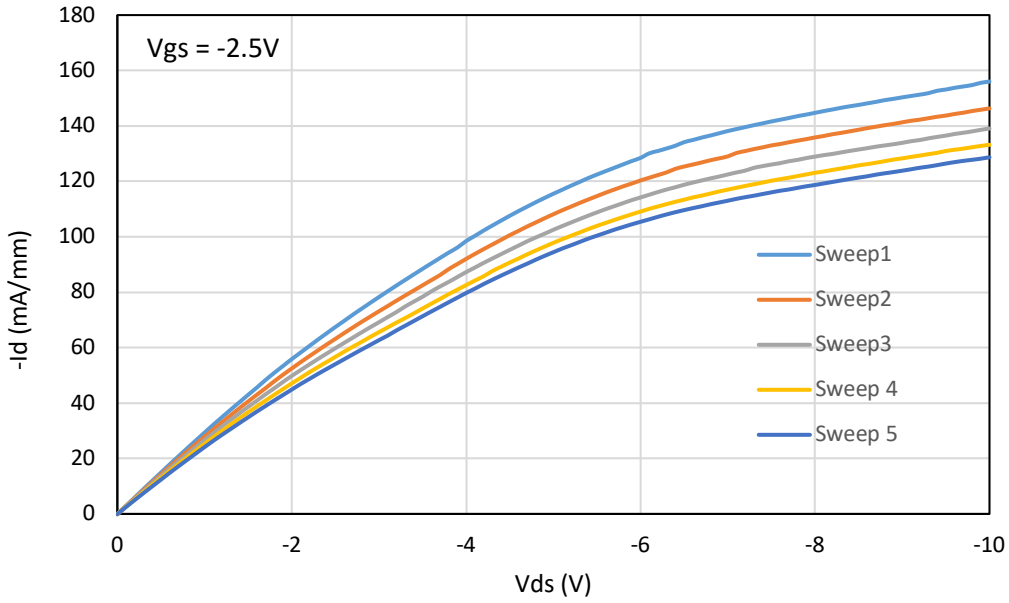

Figure 6.6.2.2 – Output characteristics at -2.5Vg repeated. 17% reduction for a 250nm gate length FET after deposition of 10nm of V_2O_5 with no anneal.

For the atmospheric adsorbate FET shown in *figure 6.6.2.1* the on resistance increases from 45Ω.mm to 56Ω.mm after 5 measurements. An increase of 11Ω.mm. For the V_2O_5 encapsulated FET shown in figure *6.6.2.2* the on resistance is increased from 33Ω.mm to 41Ω.mm after 5 measurements, an increase of 8Ω.mm. For both of these cases this is an increase in on resistance of around 24%. This is interesting as it may imply that the mechanism of reduction in the on resistance is the same for FETs using atmospheric adsorbates and V_2O_5. Therefore it may be that the increase takes place under the gate as this should be same for both atmospheric and V_2O_5 FETs. The maximum drain current has decreased in magnitude from -92mA/mm to -85mA/mm for an atmospheric adsorbate FET in *figure 6.6.2.1* after 5 repeated measurements, a reduction of 8%. The V_2O_5 encapsulated FET shown in *figure 6.6.2.2* exhibited a current decrease in magnitude from -156mA/mm to -126mA/mm after 5 repeated measurements, a decrease of 17%. In the literature MoO_3 FETs were swept 3 times in a similar manner to what is reported here and a reduction of only 3.3 % maximum drain current was observed [6.18]. Although in this case the MoO_3 was also under the gate of the fabricated FETs. So it is not clear whether the degradation can be attributed to the V_2O_5 passivation or whether the degradation may be due to a poor gate-diamond interface leading to large numbers of traps. Although the gate should remain unchanged after oxide deposition for the FETs shown here.

6.6.3 - Sweep Direction on Sample E

As repeated output sweeps have shown a decrease in the maximum drain currents and an increase in the on resistance of the fabricated FETs, preliminary investigation was undertaken to explore if the direction of the sweep in regards to the gate voltage has an effect on the maximum drain current and on resistance.

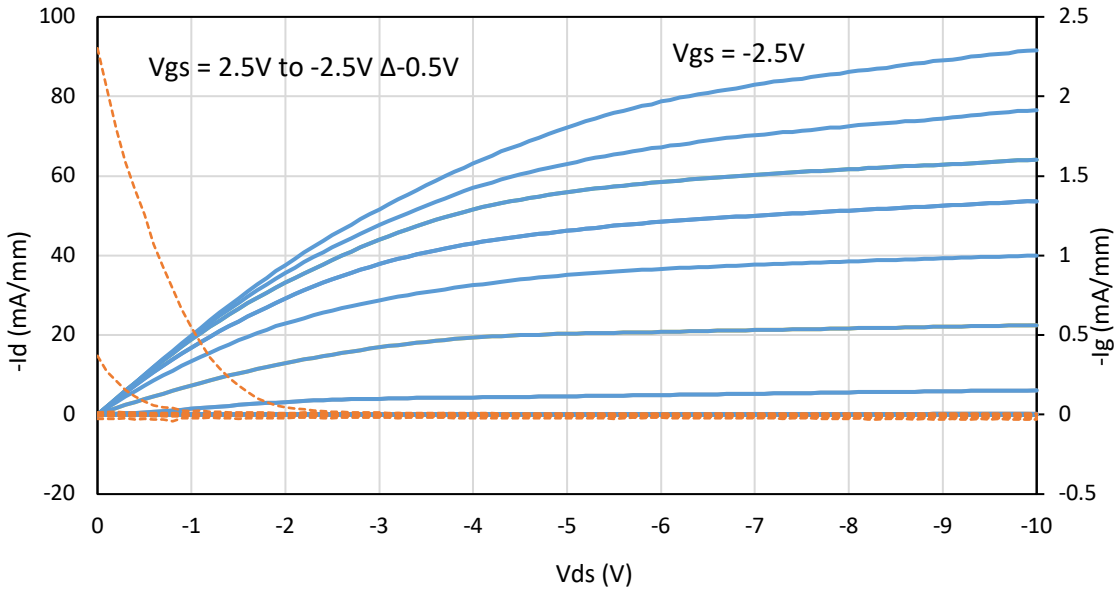

Figure 6.6.3.1 – Output characteristic swept from 2.5Vg to -2.5Vg for a 250nm gate length atmospheric adsorbate FET.

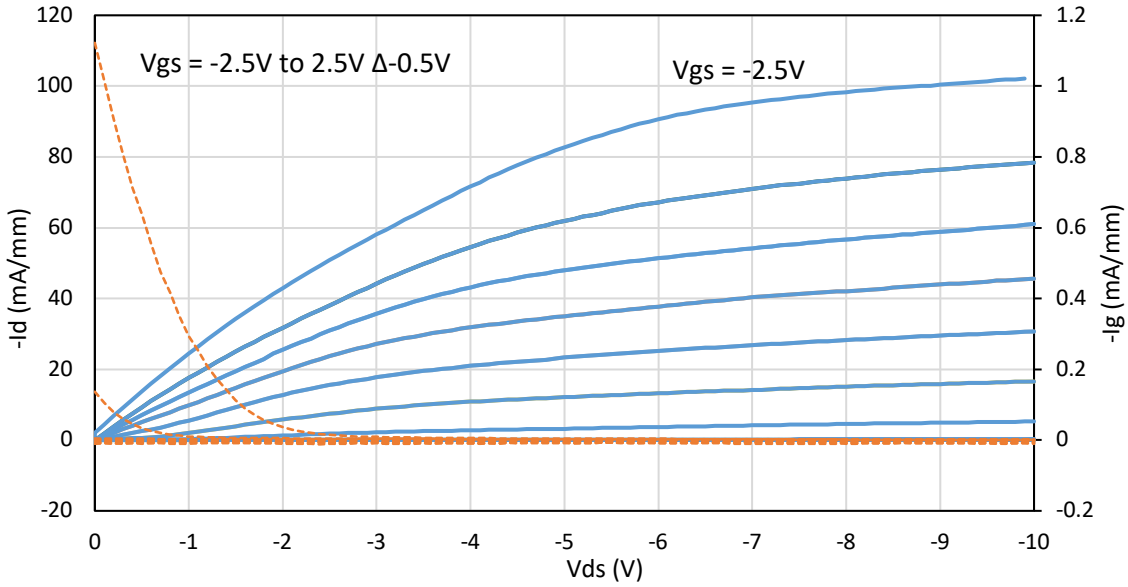

Fig 6.6.3.2 – Output characteristic swept from -2.5Vg to 2.5Vg for a 250nm gate length atmospheric adsorbate FET.

Figure 6.6.3.2 shows an output characteristic swept from the "off" state at 2.5V to the "on" state at -2.5V, *figure 6.6.3.1* is for comparison a sweep from the "on" state at -2.5V to the "off" state at 2.5V performed immediately after *figure 6.6.3.2*. It can be seen that the maximum drain current achieved has been increased in magnitude from -90mA/mm to -100mA/mm.

In p-type technology as an FET is swept from "off" to "on" initially electrons are brought close to the interface, and are pushed away from the interface as the voltage is pushed more negative. If the FET is swept from "on" to "off" electrons are initially pushed away from the interface and do not begin close to the interface as these FETs are "normally on". This may explain why a sweep from on to off results in a higher maximum drain current and lower on resistance as it should be less likely that electrons are trapped at the interface suppressing the drain current or increasing the resistance under the channel. This may emphasize the need to optimize the H-diamond:gate interface.

6.6.4 - Off State Breakdown measurements on Sample E

One of the key parameters for assessing the performance of high power FETs is the off state breakdown voltage. Thus far hydrogen terminated diamond MESFETs have been poorly explored with regards to the off state breakdown voltage and the mechanism. Therefore it was decided to undertake a preliminary investigation of the breakdown characteristics of hydrogen terminated diamond MESFETs with atmospheric doping and after deposition of V_2O_5 to explore whether the deposition of surface transfer doping oxides has an effect on these characteristics.

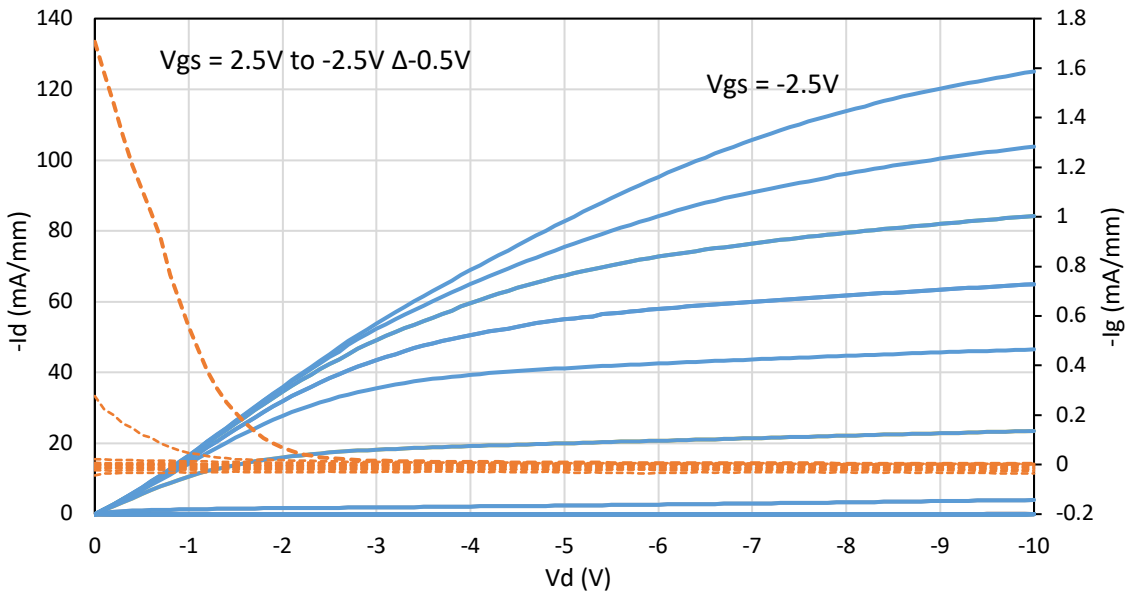

Figure 6.6.4.1 – Output characteristic measurement prior to high voltage measurement for a 250nm gate length FET using atmospheric adsorbates.

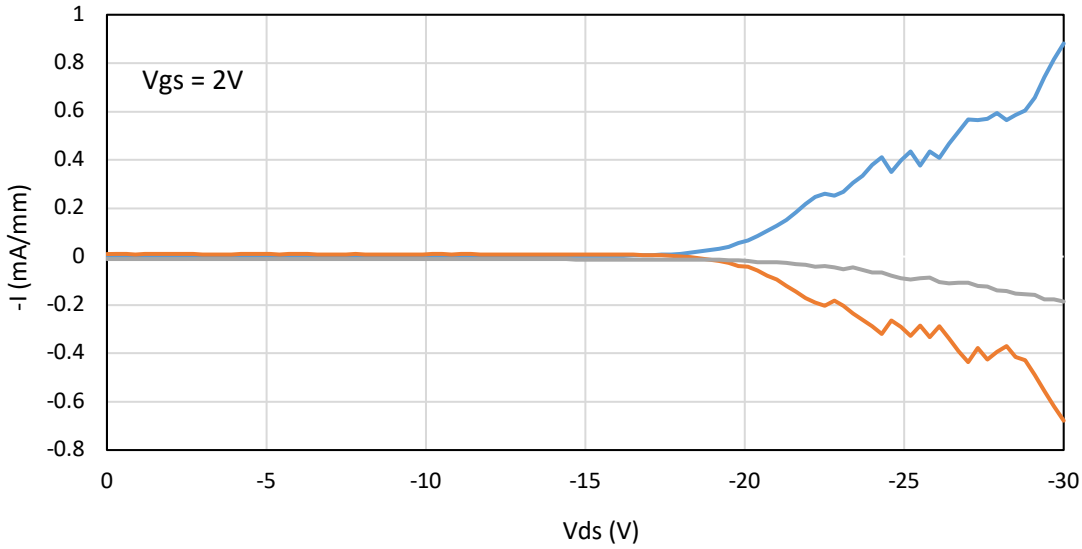

Figure 6.6.4.2 – Drain current (Blue), Source current (Orange), and Gate leakage current (Grey) at 2V Vg for "high" drain voltages for a 250nm gate length atmospheric adsorbate FET.

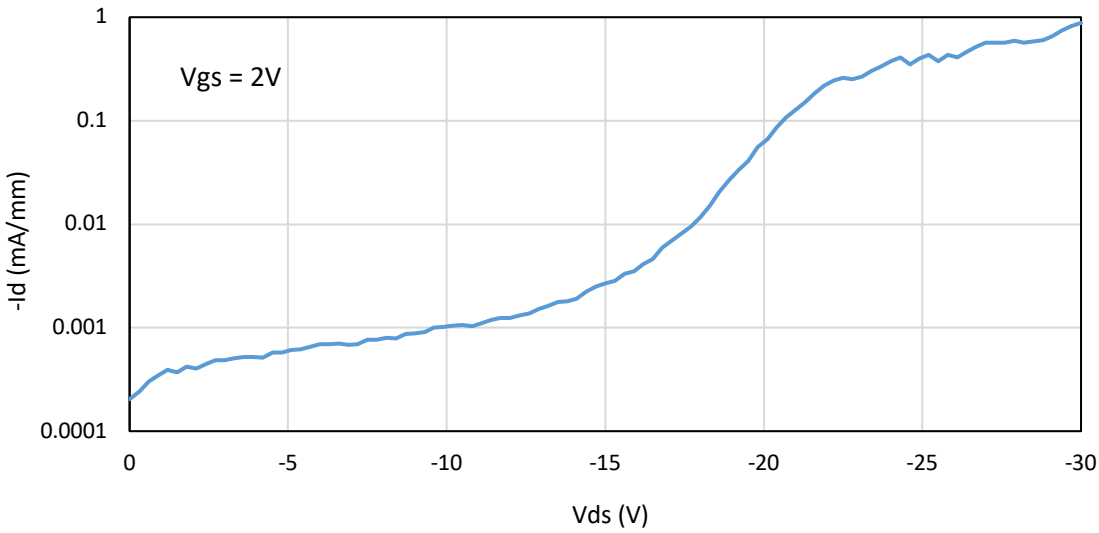

Figure 6.6.4.3 – Drain current plotted on log scale at 2V Vg for "high" drain voltages for a 250nm gate length atmospheric adsorbate FET.

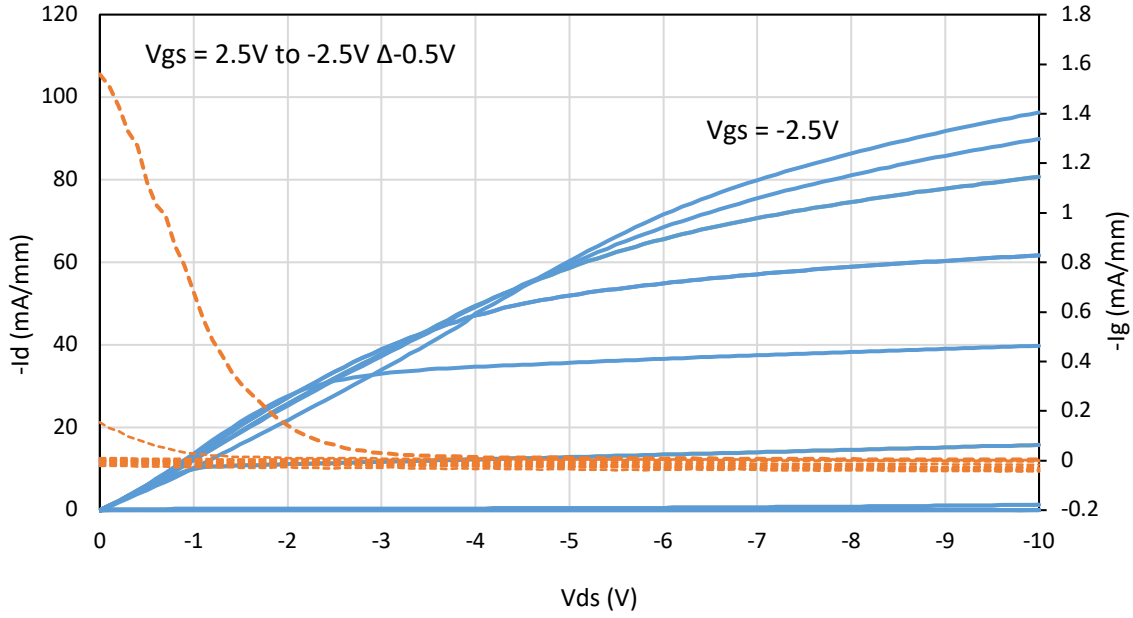

Figure 6.6.4.4 – Output characteristic measurement after high voltage measurement for a 250nm gate length FET using atmospheric adsorbates.

As can be observed in *figure 6.6.4.2*, the increase in drain current with increased drain bias is not wholly attributable to the gate leakage in this case. A substantial amount of the drain leakage current is coming from the source contact, this may imply there must be current flow around the periphery of the gate contact or through the bulk at increased drain bias. From

the log plot of drain current in *figure 6.6.4.3* it can be seen that the increase in drain current increases dramatically after -10V. It can also be observed that the increase in drain current is gradual until -10V drain bias at which point the current increases drastically by 2 orders of magnitude at -20V. As the threshold voltage in this work is defined as 0.1mA/mm (as discussed in chapter 5) the FET at -20V would be considered "on" as the drain current has not been sufficiently suppressed.

The output characteristics (*figures 6.6.4.1 and 6.6.4.4*) when compared before and after show that the FET has been damaged irreversibly leading to reduced drain current from a magnitude of -124mA/mm to -96mA/mm.

The breakdown characteristics are not consistent between FETs. Some FETs show increased drain currents due to gate leakage currents, whereas other FETs of the same dimensions on the same substrate show that the drain currents are not solely attributable to the gate leakage current with the majority of current flowing through the gate contact and little flowing from the source contact.

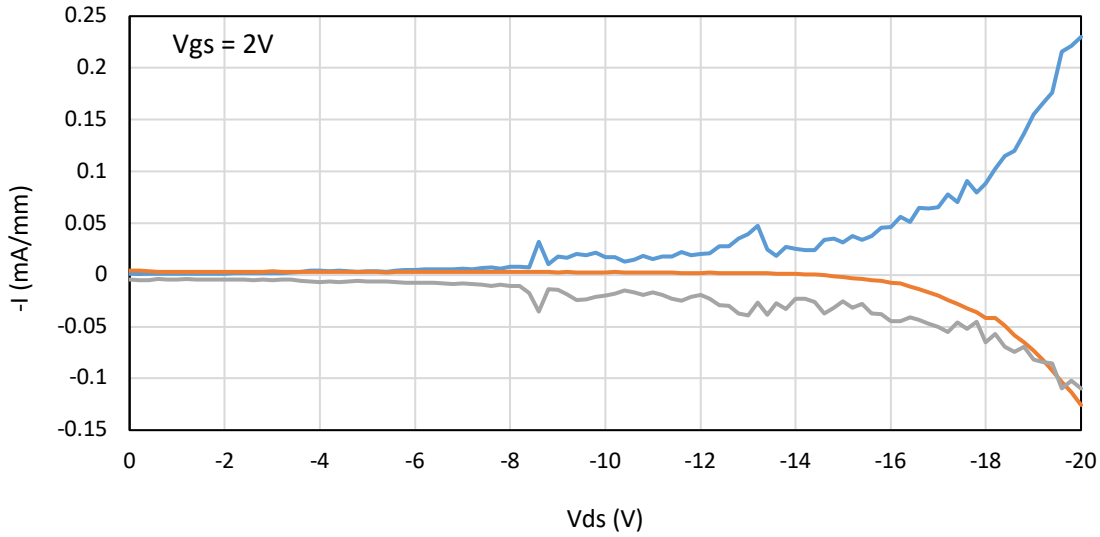

Figure 6.6.4.5 – Drain current (Blue), Source current (Orange), and Gate leakage current (Grey) at 2V Vg for "high" drain voltages for a 250nm gate length V_2O_5 encapsulated FET.

As can be seen in this example of another FET in *figure 6.6.4.5*, the gate and source currents at -20V are around 0.1mA/mm, and the drain current is -0.2mA/mm as the currents from the gate and source flow into the drain. Below in *figure 6.6.4.6* we can observe as the voltage is taken higher to -40V there is complete failure of the gate to suppress the current and the drain current rises to almost -250mA/mm, it is closely mirrored by the source current as the

FET breaks down. It appears that the source-drain leakage becomes the dominant leakage path after -30V in this case. There is no evidence of any mechanical damage to any of the contacts after high voltage measurement.

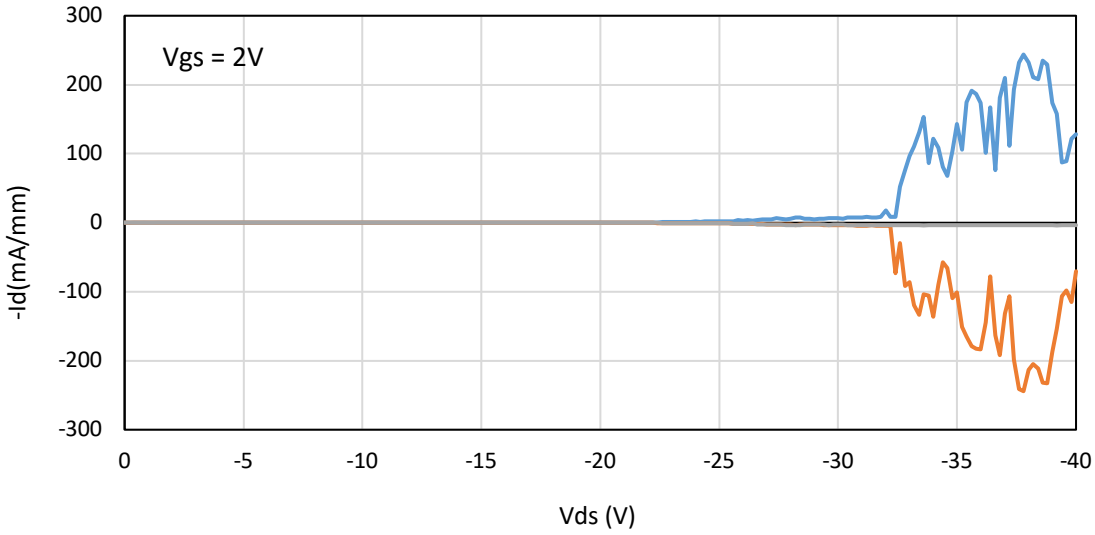

Figure 6.6.4.6 – Drain current (Blue), Source current (Orange), and Gate leakage current (Grey) at 2V Vg for "high" drain voltages for a 250nm gate length V_2O_5 encapsulated FET.

As the main focus of this work is to investigate integration of the surface transfer doping oxide into hydrogen terminated diamond FETs it is not presumed that this work can fully explore the breakdown mechanism of hydrogen terminated diamond FETs. The FET results do however show that the FETs can consistently not be brought below -30V without catastrophic failure.

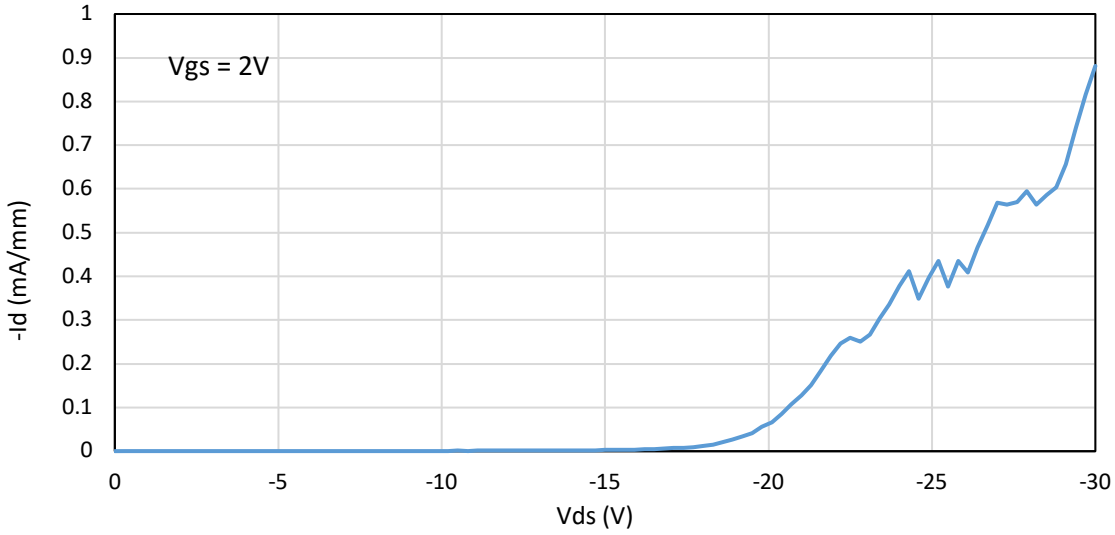

Figure 6.6.4.7 – Off-state breakdown of FET of a 250nm gate length for atmospheric adsorbates.

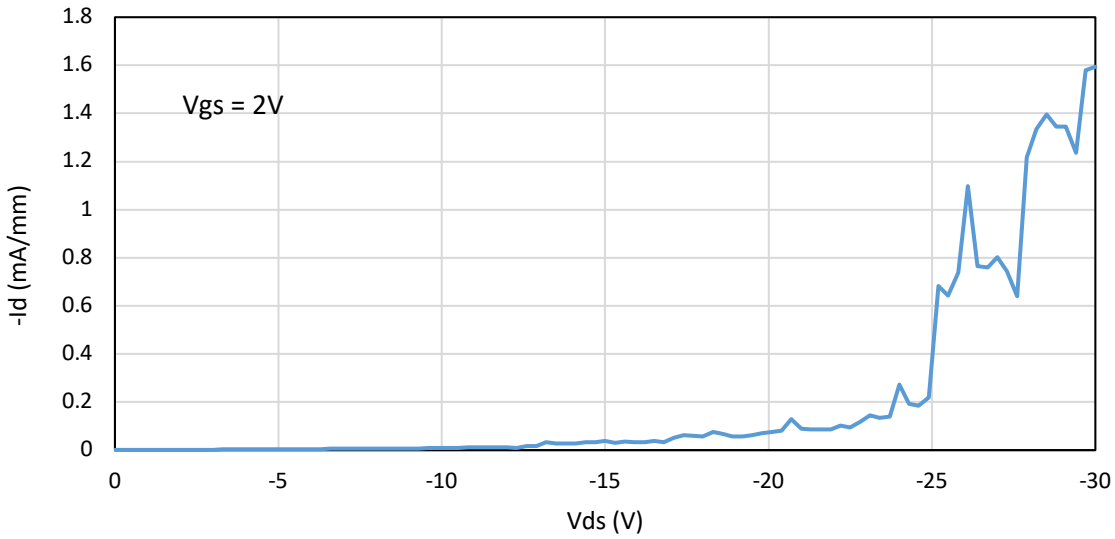

Figure 6.6.4.8 – Off-state breakdown of a 250nm gate length FET after 10nm of V_2O_5 deposition with no pre-deposition anneal.

The results in *figures 6.6.4.7 and 6.6.4.8* show that the V_2O_5 has had little appreciable effect on the breakdown voltage of the fabricated FETs. An atmospheric adsorbate FET reaches a current of -0.9mA/mm at -30V and a V_2O_5 encapsulated FET reaches a current of -1.6mA/mm at -30V. This is promising with regards to integrating surface transfer doping oxides such as V_2O_5 and MoO_3 into high power diamond FETs as it shows that the deposition

of 10nm of V_2O_5 without pre deposition annealing does not degrade the observed breakdown voltage.

These exploratory results suggest that the breakdown mechanism for hydrogen terminated diamond FETs is somewhat inconsistent. With some FETs breakdown is more gate dependent than other FETs of the same dimensions. What is clear is that the drain voltages reached here are low, and substantial engineering of the hydrogen terminated diamond FET system must be undertaken in order to improve off state breakdown. These preliminary results provide baseline for the exploration of hydrogen terminated diamond MOSFET structures fabricated on near identical material in the following chapter.

6.5 - Chapter Summary

The results shown in this chapter demonstrate the improvement of DC characteristics associated with including surface transfer doping oxides MoO_3 and V_2O_5 into hydrogen terminated diamond MESFET technology. The inclusion of surface transfer doping oxides has shown to result in higher maximum drain currents, increased extrinsic transconductance and a reduced on-resistance.

The 400°C vacuum annealing shown to be required to improve long term stability of the 2DHG after surface transfer doping oxide deposition reported in literature has been demonstrated to damage MESFET gate structures fabricated on hydrogen terminated diamond. It has however also been shown to reduce the contact resistance of gold ohmic contacts on hydrogen terminated diamond. Therefore it would be beneficial for long term stability of the 2DHG, and to improve ohmic contact resistance to engineer the robustness of the gate in order to maintain operation after high temperature vacuum annealing. By engineering the gate contact one can also hope to demonstrate FETs with greater off state breakdown performance, another important metric for high power FETs.

The following chapter will explore the fabrication of MOSFETs fabricated on hydrogen terminated diamond using Al_2O_3 as a gate dielectric in order to provide a more robust gate structure. This structure is envisioned to improve the performance of hydrogen terminated diamond FETs by allowing the inclusion of the pre surface transfer doping oxide deposition anneal and utilize surface transfer doping oxides to their full potential.

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7. Hydrogen terminated diamond MOSFETs

The preceding chapter has outlined the success of including surface transfer doping oxides V_2O_5 and MoO_3 into hydrogen terminated diamond MESFETs. The results are encouraging, although limited, showing that including MoO_3 and V_2O_5 layers without pre-deposition annealing can yield greater maximum drain currents, higher peak extrinsic transconductance and reduced on resistance compared to the same FETs using atmospheric adsorbates.

However it was also demonstrated that the existing MESFET gate structures did not operate consistently after 400°C vacuum annealing and MoO_3 and V_2O_5 deposition. Pre deposition annealing should result in improved stability of the 2DHG than deposition of surface transfer doping oxides without annealing as reported in literature[7.1]. As demonstrated in the work described in the previous chapter, annealing also appears to lower the contact resistance of gold ohmic contacts on hydrogen terminated diamond.

This chapter follows the investigation of inclusion of Al_2O_3 as a gate dielectric into the hydrogen terminated diamond FET gate stack in order to produce a more thermally robust gate structure that may tolerate the 400°C anneal. Firstly, this chapter explores the deposition of Al_2O_3 films by electron beam evaporation and confirmation that the full gate structure (combining Al_2O_3 and typical gate metal layers) can be deposited using a lift-off process. Following this is investigation into the electrical performance of MOSFETs that include Al_2O_3 as a gate dielectric using atmospheric adsorbates to induce surface transfer doping before performing a 400°C vacuum anneal and in situ deposition of MoO_3 or V_2O_5 layers.

7.1 Al_2O_3 deposition

As discussed in the previous chapter there is a desire to include a vacuum anneal prior to the deposition of surface transfer dopants in order to ensure that: a) the long term stability of the 2DHG is maintained as reported in literature[7.1], and b) to take advantage of the reduced ohmic contact resistance after 400°C vacuum annealing. It was demonstrated in the previous chapter that vacuum annealing at 400°C prior to deposition of MoO_3 or V_2O_5 proved to be incompatible with the existing diamond MESFET process.

As it was not clear what the mechanism of degradation of the gate structures during high temperatures annealing was, it was decided to investigate including a dielectric in the gate stack at the hydrogen terminated diamond – gate interface in order to provide a gate structure that is more robust to high temperatures.

There is also a desire to improve the off-state performance of the fabricated diamond FETs. Al_2O_3 as a gate dielectric has been proven in the literature to provide extremely high breakdown voltages on hydrogen terminated diamond FETs. Breakdown voltages of between 500V and 1.5KV have been reported for inclusion of Al_2O_3 into hydrogen terminated diamond FETs, Although the architectures are much larger than that reported in this work, and the typically very thick layers of Al_2O_3 used (>100nm) result in poor on state characteristics such as maximum drain current, on resistance and peak extrinsic transconductance, it is promising to see the potential of increasing the off state breakdown voltage by including gate dielectrics such as Al_2O_3 [7.2, 7.3].

It was first considered to include Al_2O_3 grown by atomic layer deposition as this would provide a well characterized and optimized dielectric layer as has been shown on diamond previously[7.4]. However the process of ALD growth can only be done in a conformal manner, meaning a lift-off resist process cannot be utilized to define the gate contact. Thus the Al_2O_3 would have to be grown across the whole surface of the devices and then etched where it is not required in order to deposit either MoO_3 or V_2O_5 in the access regions. The etching processes which were readily available for Al_2O_3 could damage the hydrogen termination of the diamond's surface which would degrade, or entirely eliminate the 2DHG.

Another option considered was to anneal aluminium deposited by electron beam evaporation in an oxygen rich environment as has been shown previously in literature [7.5, 7.6]. However it was not clear what the effect on the hydrogen termination of the diamond surface would be when exposed to elevated temperatures in an oxygen rich environment.

The option finally settled on was electron beam evaporation of Al_2O_3, as electron beam evaporation would allow the use of a lift-off process to define the gate contact and the diamond surface would not be exposed to anything which could damage the hydrogen termination.

Al_2O_3 deposited by electron beam evaporation was deposited on silicon substrates with native silicon oxide in order to assess the quality of the Al_2O_3 films by ellipsometry. All deposition of Al_2O_3 was carried out at $2x10^{-6}$ mbar using a 10kV electron beam source manufactured by Telemark in a Plassys MEB400 vacuum system.

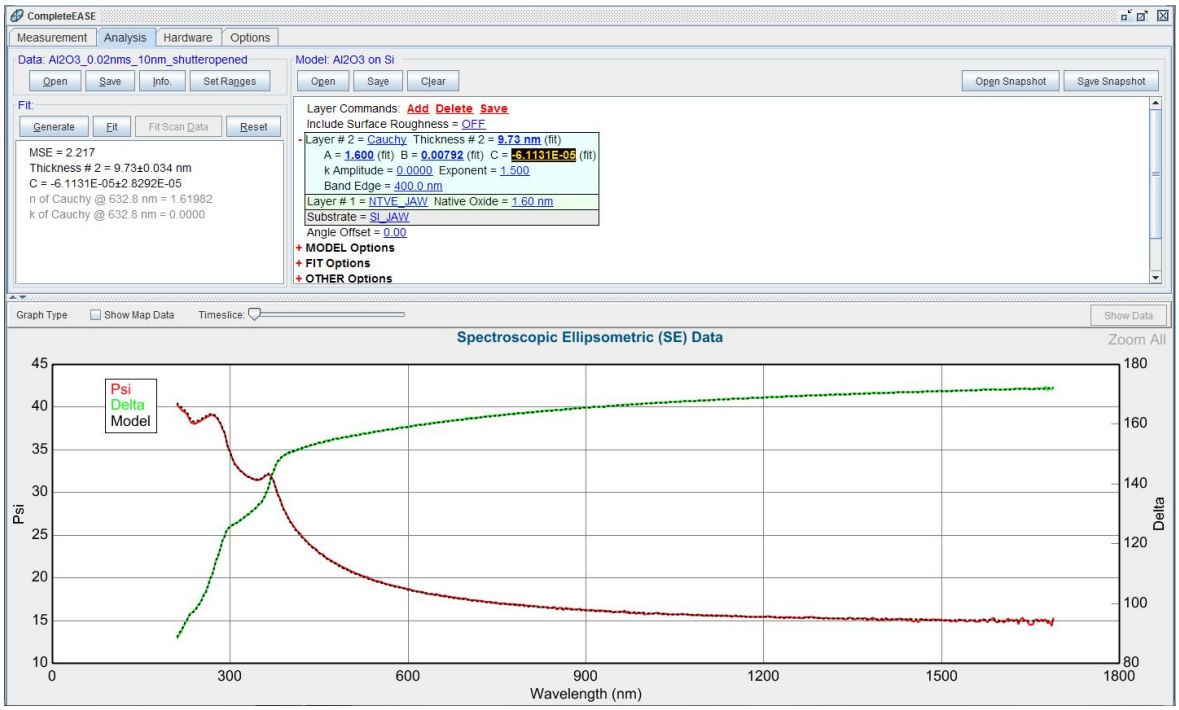

Figure 7.1.1 – Screenshot of ellipsometry data for 10nm of Al_2O_3 deposited on 500µm thick Si wafer with native SiO_2.

The ellipsometry data in *figure 7.1.1* shows the acquired data plotted fitted with the Cauchy model for 10nm Al_2O_3 deposited on top of a silicon substrate with native SiO_2 and shows a close match to the theoretical curve. We can see that the refractive index is measured to be around 1.62, which is somewhat lower than the textbook value for Al_2O_3 films of 1.7[7.7]. However it is very close to what has been reported for Al_2O_3 films grown by electron beam deposition elsewhere, where refractive indexes between 1.58 and 1.63 are reported [7.8]. This is not unexpected as electron beam deposition of oxide layers is thought to lead to poor quality, oxygen deficient films. Although the application of the Al_2O_3 would not be for optical applications it was thought that the refractive index could be a good indicator of the quality of the films.

Following confirmation that the deposited films were Al_2O_3 the lift-off of Al_2O_3 was tested mechanically on an oxygen terminated diamond substrate. The standard process of etching the source drain gap and depositing the gate between the source and drain contacts followed to ensure that the full process would work.

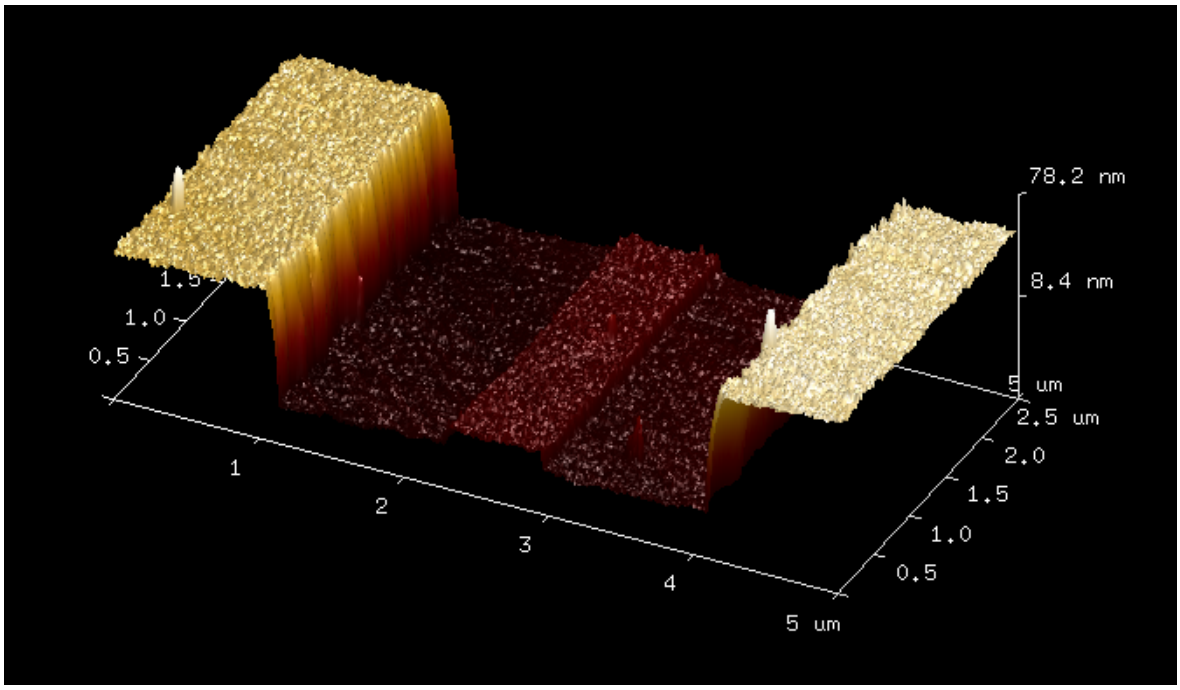

Figure 7.1.2 – 3D image created from AFM scan of source-drain gap with 10nm of Al_2O_3 deposition in the middle of the source-drain gap.

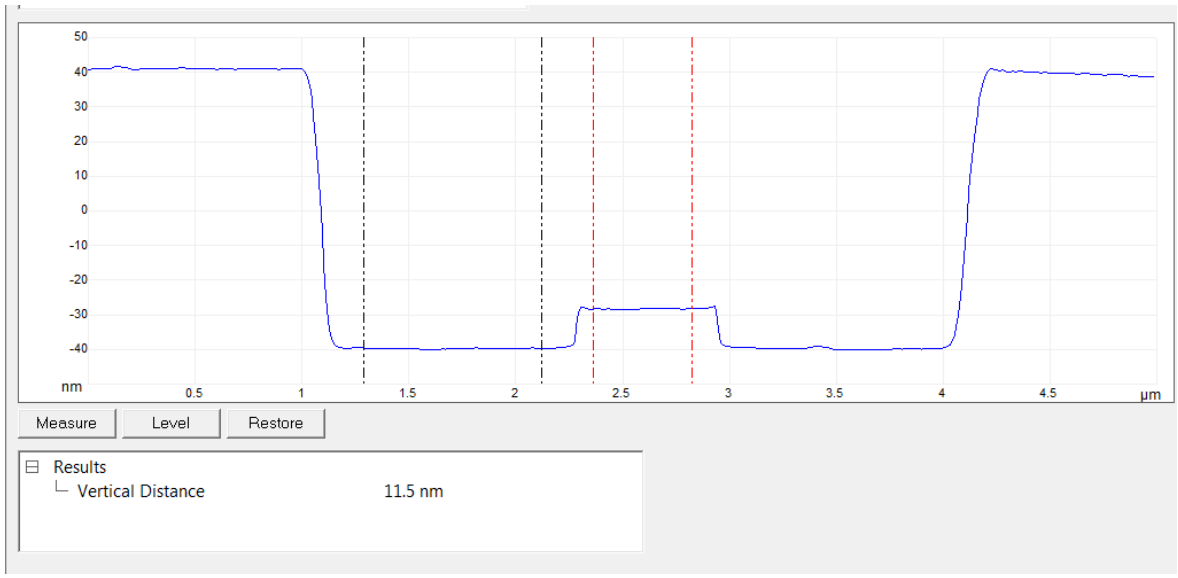

Figure 7.1.3 – AFM scan of source-drain gap with 10nm of Al_2O_3 deposition in the middle of the source drain gap.

As can be observed in *figures 7.1.2* and *7.1.3* the Al_2O_3 deposition has successfully lifted off and the thickness of the deposition is within 15% of the intended thickness of 10nm. The ohmic contacts can be observed on the right and left of the AFM scan.

After confirmation that the Al_2O_3 layer would lift off successfully using the established gate process, the full gate stack was tested in order to ensure full lift off of the gate structure. The full gate stack with thicknesses of each metal layer can be seen in figure 7.1.4.

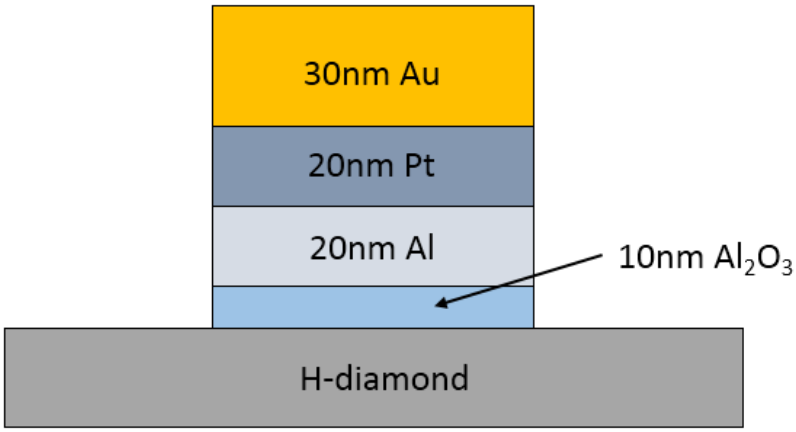

Figure 7.1.4 – Gate stack used throughout this chapter of 10nm of AL_2O_3/20nm of Al/20nm of Pt/30nm.

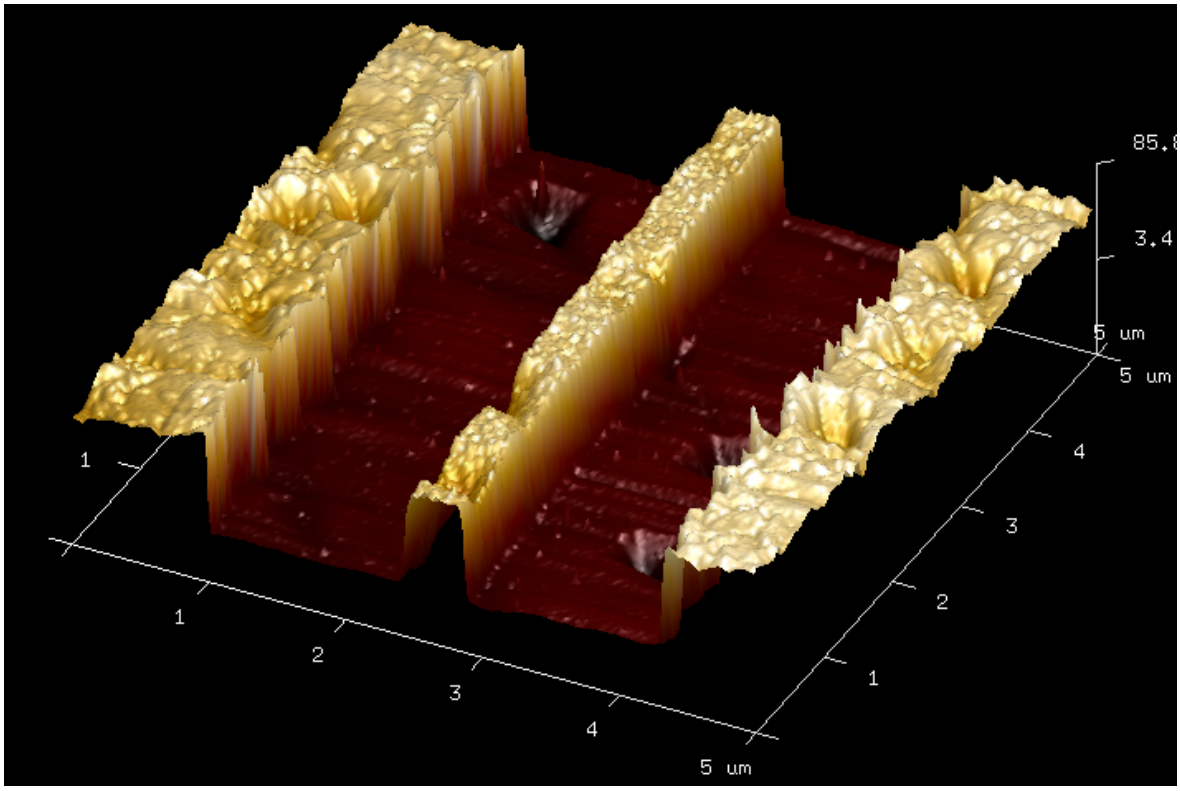

Figure 7.1.5 – 3D image created from AFM scan of source-drain gap with 10nm of Al_2O_3 deposition and 10nmAl/10nmPt/30nmAu in the middle of source-drain gap.

In *figure 7.1.5* it can be observed that the full gate structure of 10nm of Al_2O_3/20nm of Al/20nm of Pt/30nm of Au has lifted off successfully. The AFM scan shows a height of 81.3nm. Which is close to the total intended height of 80nm.

After confirmation of the mechanical lift-off of the gate stack, next it would be required to assess the electrical performance of the gate structures for fabricated MOSFETs with

atmospheric adsorbates, and then after 400°C vacuum annealing and in situ surface transfer doping oxide deposition.

7.2 Al_2O_3 MOSFET with 400°C vacuum annealing and 10nm MoO_3 deposition – Sample F

After the demonstration of the deposition of Al_2O_3 films by electron beam deposition, and successful lift off technique of the Al_2O_3/Al/Pt/Au gate structure it was decided to test the electrical performance of the gate contact including Al_2O_3 gate dielectric by fabricating a series of FETs. Following this the completed FETs were exposed to 400°C vacuum annealing at a pressure of $2x10^{-6}$ mbar for 1 hour, prior to in situ deposition of 10nm of MoO_3 as shown in *figure 7.2.1*. The performance of the FETs would then be assessed again to ascertain the effect of the annealing and MoO_3 deposition on the FETs.

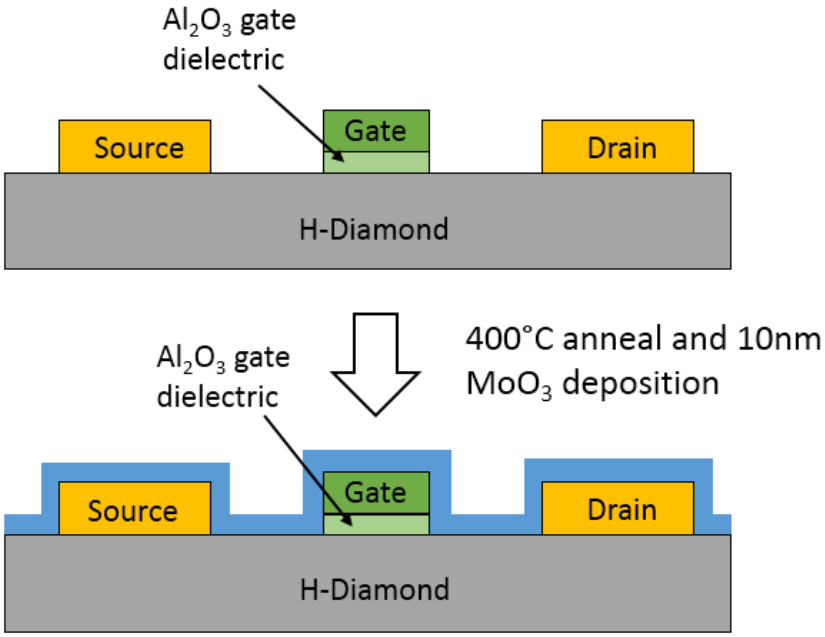

Figure 7.2.1 - FET structure with atmospheric adsorbates (top) and after 400°C vacuum anneal and 10nm of MoO_3 deposition (bottom).

The fabrication of a series of MOSFETs to atmospheric adsorbate level was carried out on CVD material which was overgrown with a 5µm layer of CVD diamond with surface roughness of around 0.5nm Ra which was hydrogen terminated at 2kW plasma power density after growth. Hydrogen termination and growth was carried out by collaborators at Universite Paris 13. The full fabrication methods and processes are outlined in chapter 4 and the process sheets can be found in appendix A. The performance of the fabricated MOSFETs was assessed by electrical measurement of the output characteristics and transfer

characteristics as discussed in chapter 5. After this the substrate was annealed at 400 °C at a vacuum pressure of $2x10^{-6}$ mbar and MoO_3 was deposited across the completed devices. Following this the MOSFETs were electrically characterized again for comparison with atmospheric adsorbates.

Material	*Hydrogen termination*	*Sheet Resistance on arrival (in air)*
CVD substrate with epitaxial CVD overgrowth.	*2kW in situ after growth of 5µm CVD layer.*	*20.8k (Ω/□)*

Table 7.2.2 - Material preparation prior to fabrication.

During fabrication it was observed that the conductivity of the material could not be fully eliminated by exposure of the surface to oxygen plasma. After repeated oxygen etches current continued to flow between the isolation test structures which can be observed in *figure 7.2.2*. This material was part of the same batch of material overgrown with a layer of CVD diamond in shown in chapter 6.3 which showed the same response after multiple oxygen ashes.

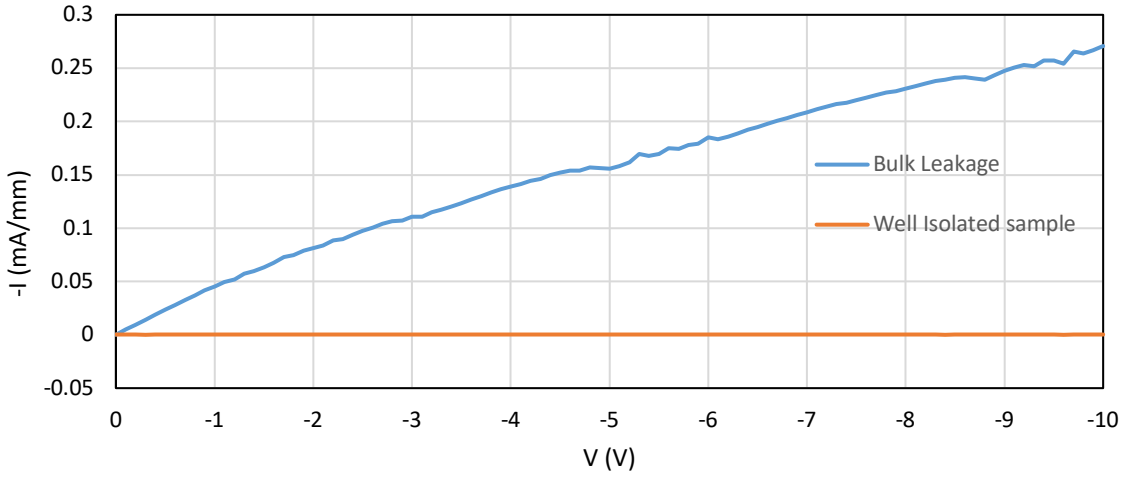

Figure 7.2.2 – Current across a 5um gap isolation structure after 2 oxygen ashes

In addition, the gold to be etched from the test structures as part of the "active" level did not etch correctly and thus unfortunately the TLM and VDP data could not be extracted for this substrate. It is thought that the lithography for this layer did not develop correctly, and after etching there are islands of gold left where the etchant could not fully access the gold in the TLM gaps and VDP active areas as can be seen in the optical image in *figure 7.2.3*.

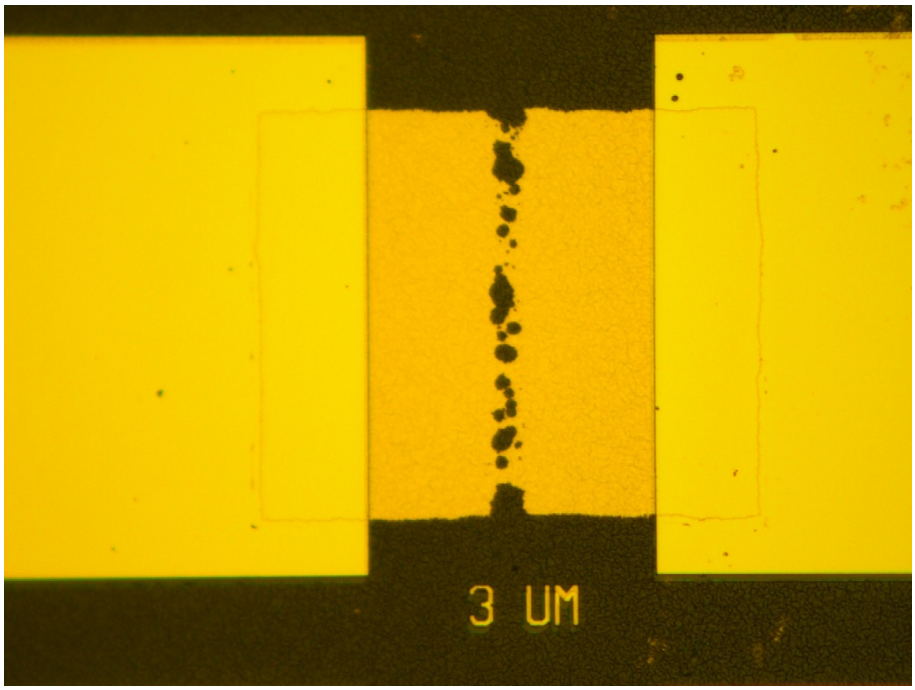

Figure 7.2.3 – Optical image of one TLM gap showing poor gold etching on this substrate.

Following the failed etching of the TLM and VDP area, fortunately the gate etch worked as intended and the source-drain gap fully etched as can be seen from the optical microscope image in *figure 7.3.4.*

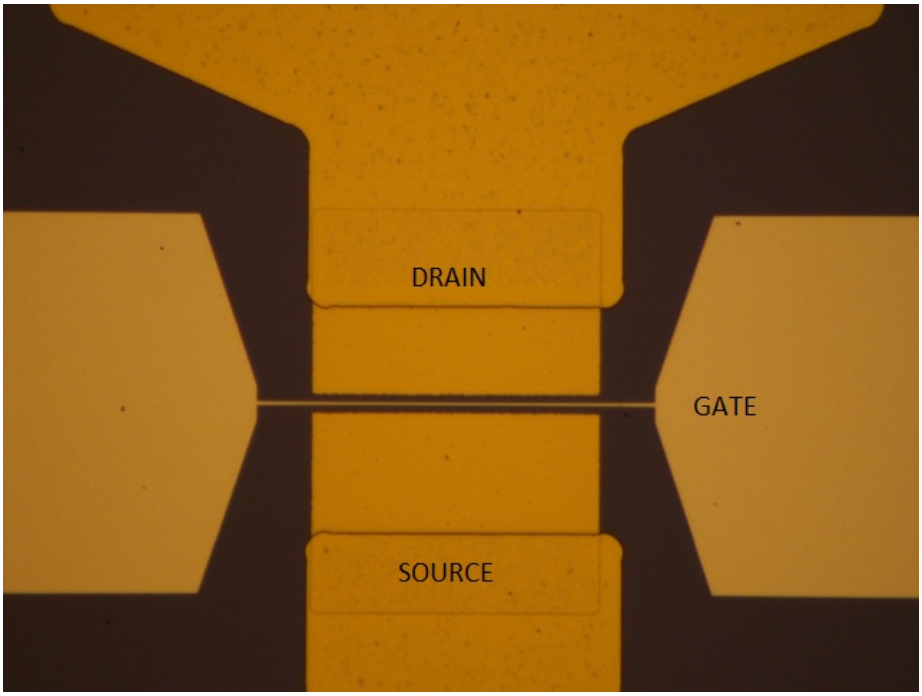

Figure 7.2.4 – Optical image showing successful etching of the source-drain gap and deposition of the gate contact.

The FETs were fabricated up to gate level and the output and transfer characteristics were measured with the diamond surface exposed to air. Following this the substrate was annealed

at 400°C and 10nm of MoO_3 was deposited across the whole substrate. The output characteristics and transfer characteristics before and after annealing and MoO_3 deposition are shown below in *figures 7.2.5-7.2.12*

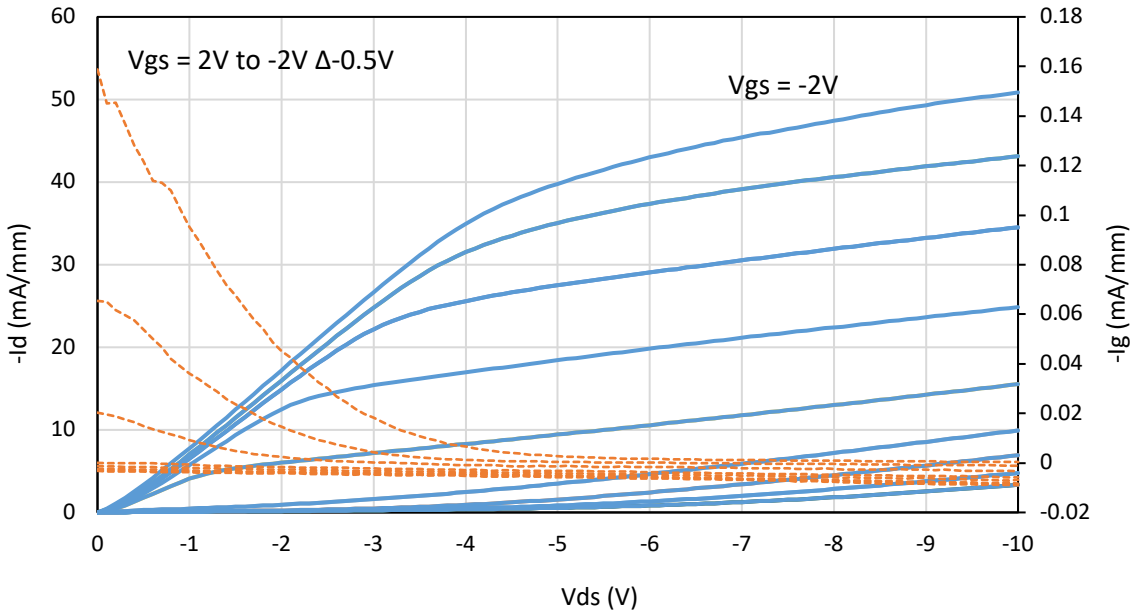

Figure 7.2.5 - Output characteristics for 0.25µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and gate leakage current is shown in orange.

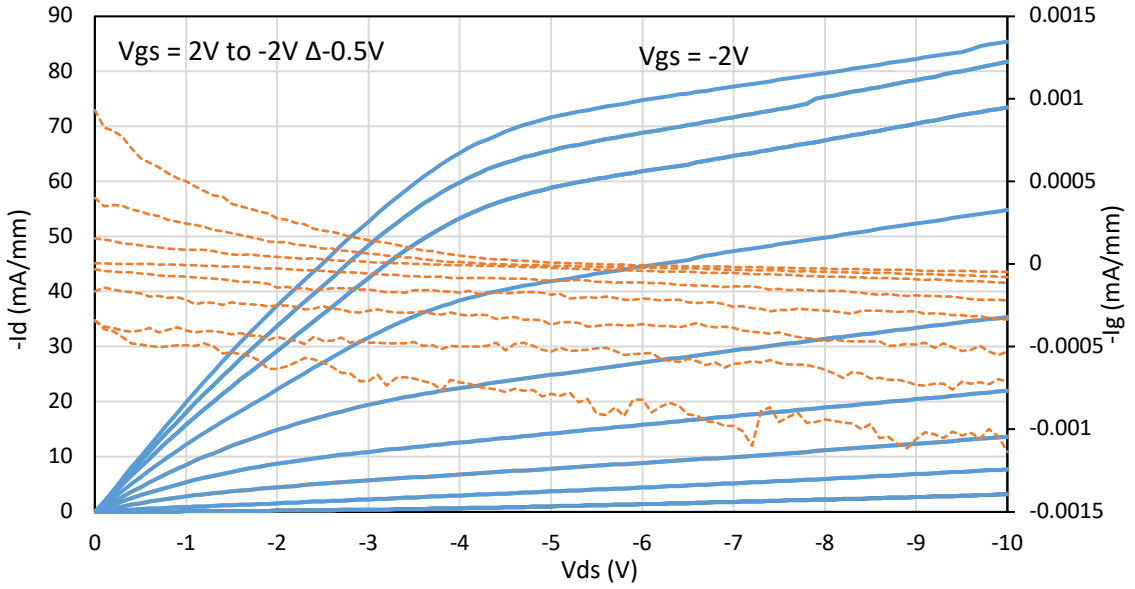

Figure 7.2.6 - Output characteristics for 0.25µm gate length FET with 10nm of MoO_3 deposited in situ after 400°C vacuum annealing. Drain current is shown in blue, and gate leakage current is shown in orange.

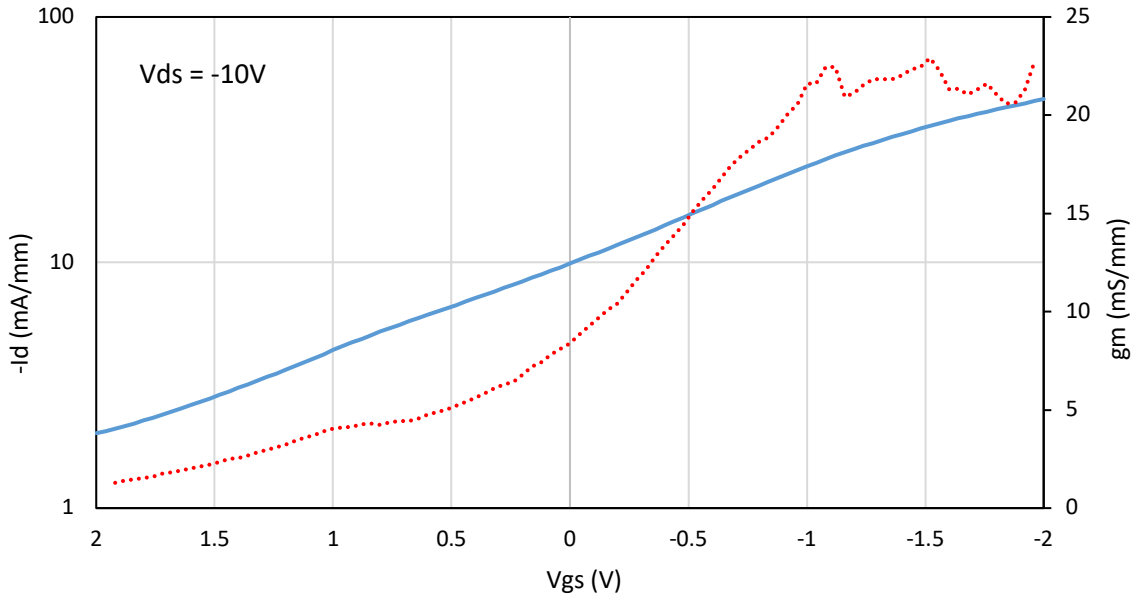

Figure 7.2.7 - Transfer characteristics for 0.25µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

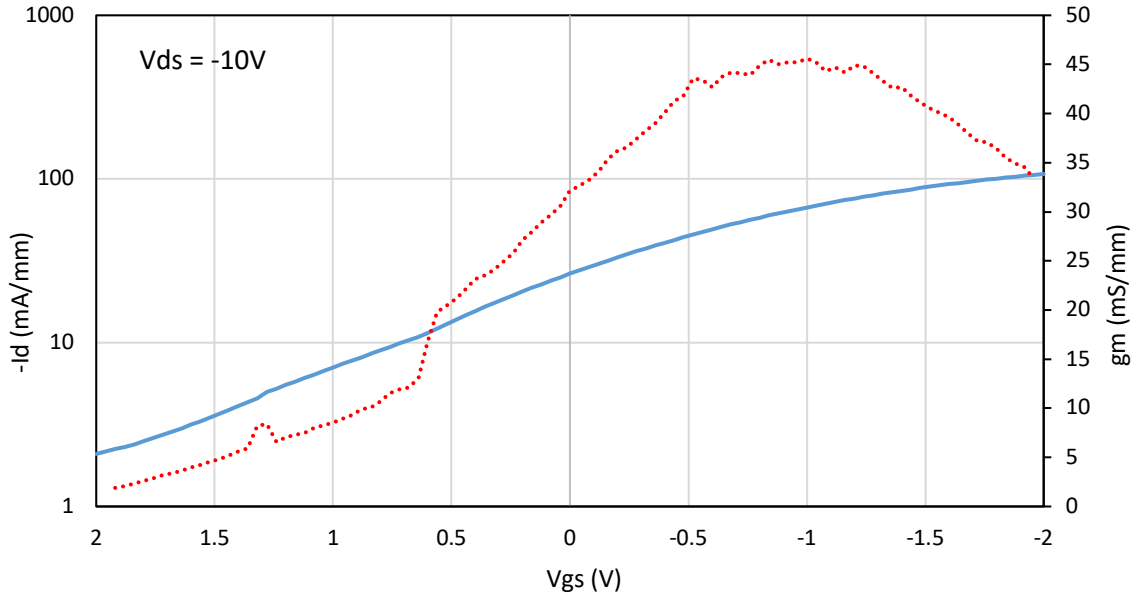

Figure 7.2.8 - Transfer characteristics for 0.25µm gate length FET with 10nm of MoO_3 deposited in situ after 400°C vacuum annealing. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

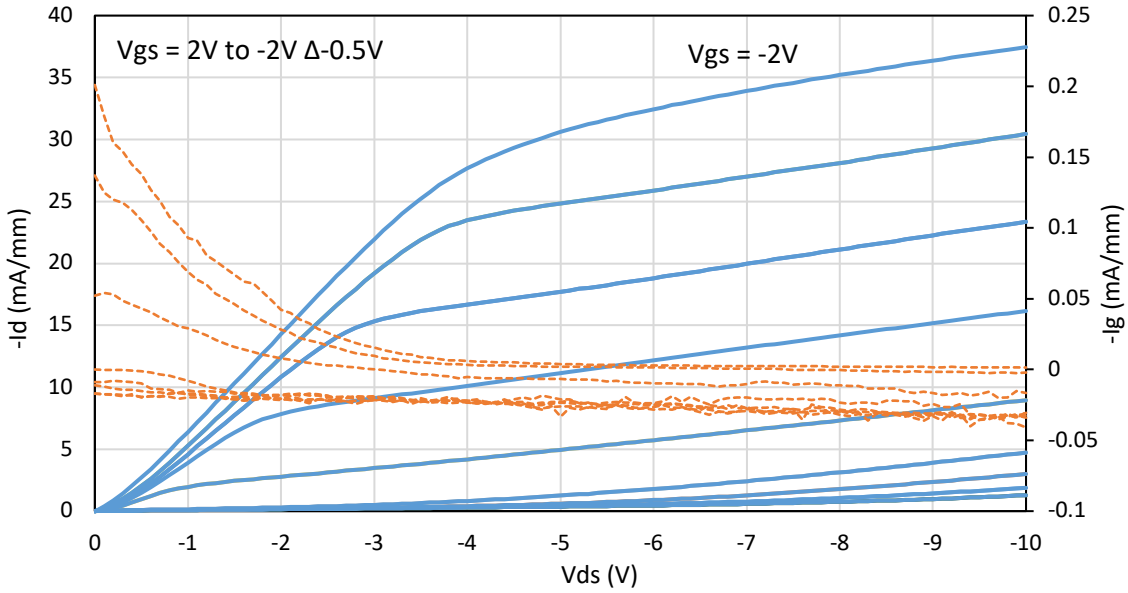

Figure 7.2.9 - Output characteristics for 0.5µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and gate leakage current is shown in orange.

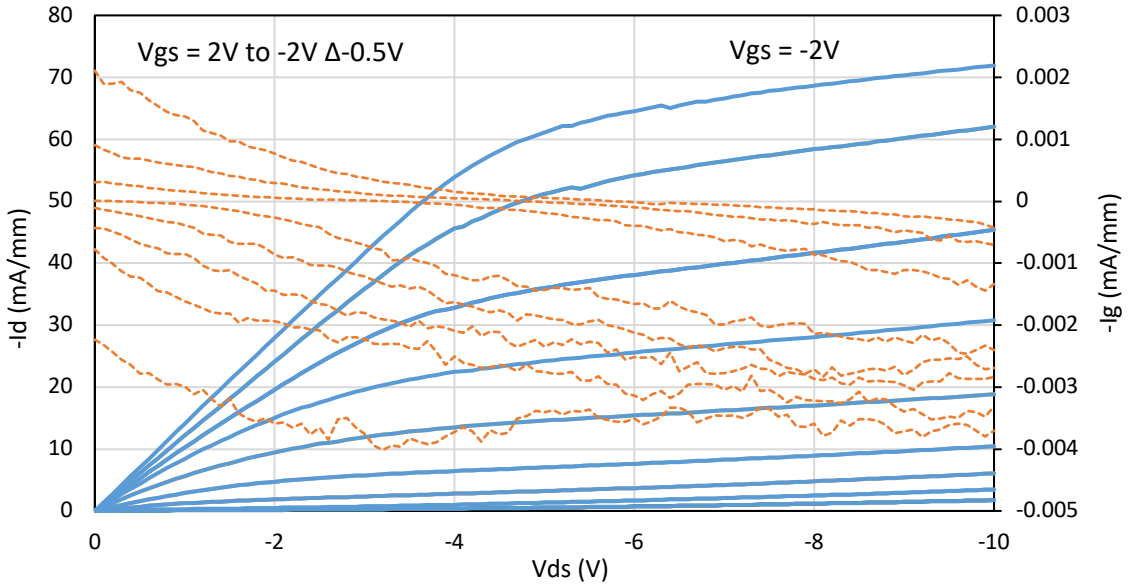

Figure 7.2.10 - Output characteristics for 0.5µm gate length FET with 10nm of MoO_3 deposited in situ after 400°C vacuum annealing. Drain current is shown in blue, and gate leakage current is shown in orange.

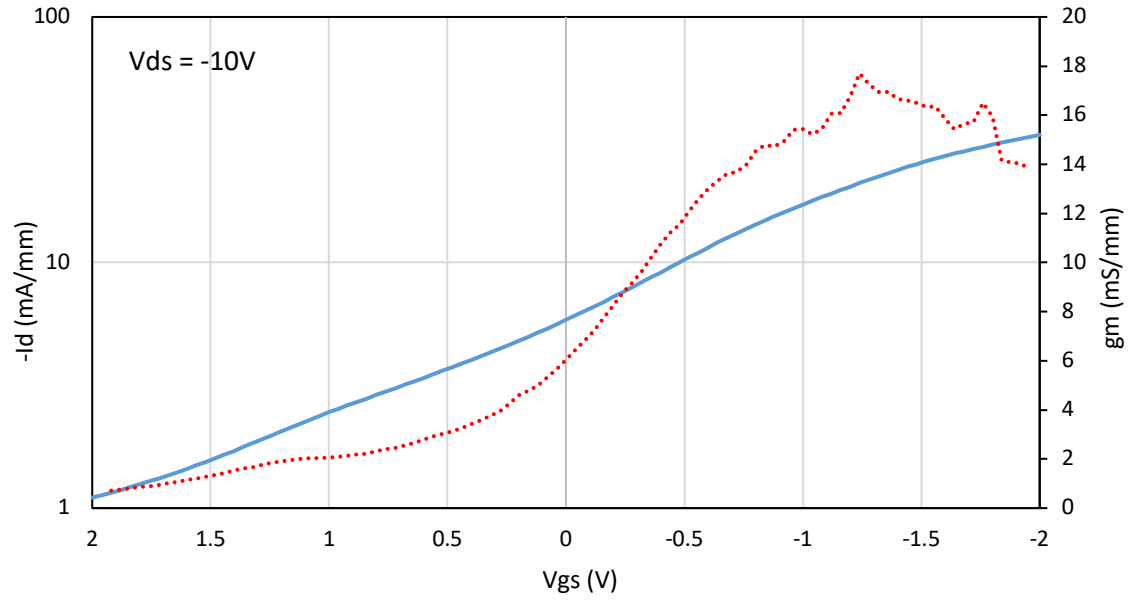

Figure 7.2.11 - Transfer characteristics for 0.5µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

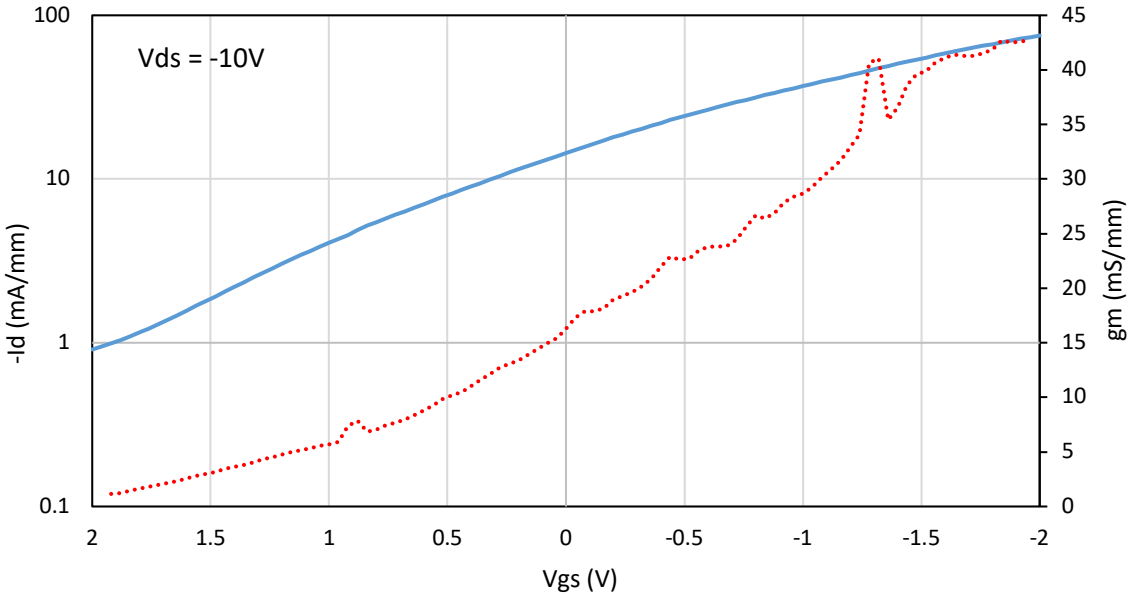

Figure 7.2.12 - Transfer characteristics for 0.5µm gate length FET with 10nm of MoO_3 deposited in situ after 400°C vacuum annealing. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

Gate Length (μm)	*Idmax Atmo (mA/mm)*	*Peak gm Atmo (mS/mm)*	*Ron Atmo (Ω.mm)*	*Idmax MoO_3 (mA/mm)*	*Peak gm MoO_3 (mS/mm)*	*Ron MoO_3 (Ω.mm)*
0.25	*-50.8*	*23*	*105*	*-85.4*	*45*	*53*
0.5	*-37.5*	*17*	*126*	*-71.8*	*43*	*72*

Table 7.2.2 – Key DC parameters measured for FETs with atmospheric adsorbates, and after 400°C vacuum annealing and MoO_3 deposition.

Due to the inability to isolate the material the threshold voltage could not be measured for comparison with other fabricated FETs as the currents could not be pushed below -0.1mA/mm. Unfortunately, this has also led to a poor "on/off ratio" at just $1.5x10^1$.

The maximum drain current achieved for a 250nm gate length FET was -50.8mA/mm and -37.5mA/mm for a 500nm gate length FET for atmospheric adsorbate FETs as can be observed in *figures 7.2.5* and *7.2.9*. After vacuum annealing at 400°C for 1 hour and in situ MoO_3 deposition this has increased in magnitude to -85.4mA/mm for a 250nm FET and -71.8mA/mm for a 500nm FET as can be observed in *figures 7.2.6* and *7.2.10*. This increase is expected due to the increased carrier concentration in the channel area. It can be observed that the gate structures maintain transistor operation after 400°C vacuum annealing and MoO_3 deposition.

The on resistances with the diamond surface exposed to atmosphere are calculated to be 105Ω.mm for a 250nm FET and 126Ω.mm for a 500nm FET as shown in *table 7.2.2*. After 400°C vacuum annealing and in situ deposition of MoO_3 the on resistances have reduced to 53Ω.mm for a 250nm FET and 72Ω.mm for a 500nm FET. This reduction in sheet resistance is consistent with the reduction in channel resistance and contact resistance as has been observed previously after vacuum annealing and MoO_3 deposition. This is encouraging as it implies that the vacuum annealing prior to deposition of MoO_3 has not had a negative effect on the resistance under the gate of the FETs.

After annealing and oxide deposition it appears that there has been a decrease in the gate leakage currents of around 2 orders of magnitude for these MOSFET devices, from a peak of 0.2mA/mm to 0.002mA/mm. Whether this is due to the annealing of the Al_2O_3 layer, or the deposition of MoO_3 is unclear. It may be that the annealing is having the effect of passivating trapping states in the Al_2O_3 layer resulting in less leakage current.

For the FETs exposed to atmospheric adsorbates a peak extrinsic transconductance of 23mS/mm for a 250nm FET and 17mS/mm for a 500nm FET was measured as can be observed in *figures 7.2.7* and *7.2.11*. After vacuum annealing at 400°C for 1 hour and in situ

deposition of 10nm MoO_3 the peak extrinsic transconductance has increased to 45mS/mm for a 250nm gate length FET and 43mS/mm for a 500nm gate length FET as can be observed in *figures 7.2.8* and *7.2.12*. This is an expected, though still encouraging improvement attributable to the reduced sheet resistance in the channel area and the presumed reduction in contact resistance from annealing the ohmic contacts (although the TLMs could not be used to measure the contact resistances for this substrate, it is assumed there will be a reduction in contact resistance after 400°C vacuum annealing and MoO_3 deposition as observed previously in chapter 6).

Although the data which could be gathered from this set of FETs was limited due to the large off-state leakage and incomplete TLM and VDP structures it is encouraging as it shows that the inclusion of Al_2O_3 as a gate dielectric results in maintained transistor operation (after high temperature vacuum annealing and surface transfer doping oxide deposition. It also further emphasizes the increased DC performance of FETs associated with deposition of MoO_3.

7.3 Al_2O_3 MOSFET with 400°C vacuum annealing and V_2O_5 deposition- Sample G

Material	*Hydrogen termination*	*Sheet Resistance on arrival (in air)*
CVD Element six	*2.6kW Power density*	*16k Ω/□*

Table 7.3.1 – Material preparation prior to fabrication

Although the results from the sample shown in chapter 7.2 are encouraging, showing that the gate structure including AL_2O_3 gate dielectric remains operational after 400°C vacuum annealing and in situ deposition of MoO_3, it is unfortunate that the material characterization structures (TLM and VDPs) were unusable and the performance of the FETs was limited by the large off-state leakage currents.

It was therefore decided to repeat the experimentation with the same gate structure on material which did not exhibit the same inability to isolate the FETs. The FETs would similarly be characterized in air and after the deposition of 10nm of V_2O_5 following a 400°C vacuum anneal in order to investigate if including the deposition of V_2O_5 and pre deposition anneal would have the same beneficial effects on DC performance as observed for MoO_3 and pre deposition annealing. Using material which can be properly isolated would also allow investigation of the off state performance of the FETs in air and after V_2O_5 deposition

and pre deposition annealing. Literature also suggests that V_2O_5 should provide higher carrier concentration, and a more thermally robust 2DHG in comparison to MoO_3[7.1].

This substrate was optical grade CVD diamond sourced from Element Six. The diamond surface was etched with a tailored Cl_2 +Ar and O_2 + Ar chemistry to remove surface and sub-surface damage, and then exposed to 2.6kW a power density hydrogen plasma by collaborators at Universite Paris 13 after a two step-acid boil. After hydrogen termination this material had a surface roughness measured by AFM of 0.3nm Ra.

7.3.1 DC Measurements of Sample G

TLMs, VDPs and FETs were fabricated on the substrate using the processes described in chapter 4 and electrically characterized using the techniques discussed in chapter 5 after exposure to atmospheric adsorbates. Following this, the substrate was annealed at 400°C under a vacuum of $2x10^{-6}$ for 1 hour prior to the in situ deposition of 10nm of V_2O_5 as shown in *figure 7.3.1.1* and electrical characterization was repeated.

The sheet resistance in air measured by the Hall Effect prior to any fabrication was around 16kΩ/□. This is close to what was observed for previous material prior to fabrication which showed sheet resistances between 20-30kΩ/□. However, from the TLM and VDP structures fabricated on this sample and shown in *table 7.3.1.1* it can be seen that the measured sheet resistance is 7.2kΩ/□. This effect was previously noted for the substrate in chapter 6.6.

The VDP structures fabricated on this substrate show that after 400°C vacuum annealing and in situ deposition of 10nm of V_2O_5 the sheet resistance has improved from 7.2kΩ/□ to 4.2kΩ/□. In chapter 6.6 the sheet resistance of the sample reduced to 5.2kΩ/□ from 7.2 kΩ/□ after deposition of 10nm of V_2O_5 with no deposition annealing. The improved reduction here to 4.2KΩ/□ from 7.2kΩ/□ may show an added benefit to the inclusion of 400°C vacuum annealing prior to deposition of V_2O_5. The contact resistances from TLMs show a decrease in the contact resistance from 9Ω.mm to 3Ω.mm after 400°C vacuum annealing and in situ deposition of 10nm of V_2O_5.

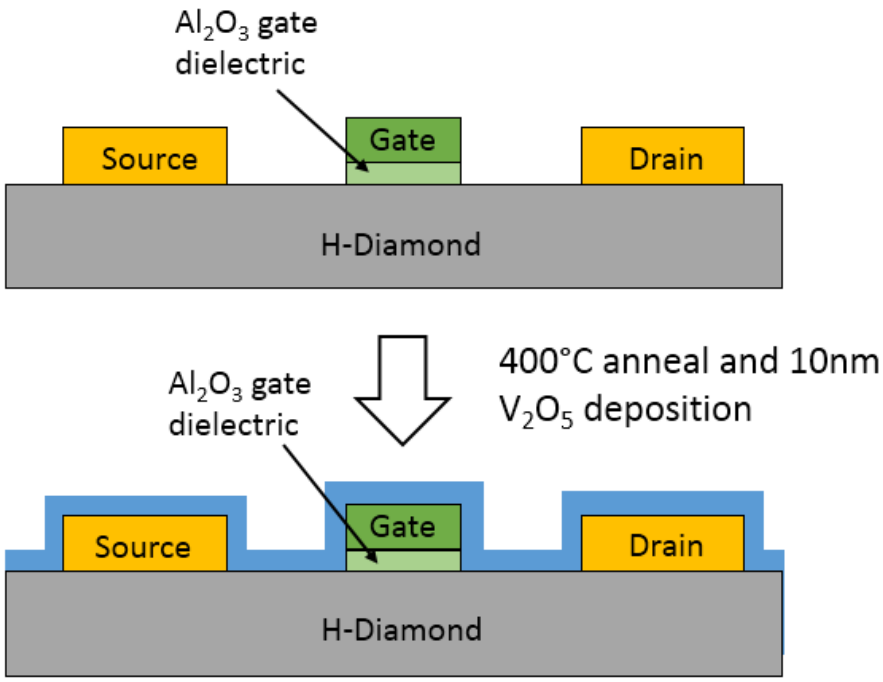

Figure 7.3.1.1 - FET structure with atmospheric adsorbates (top) and after 400°C vacuum anneal and V_2O_5 deposition (bottom).

	Sheet resistance (kΩ/□)	*Contact Resistance (Ω.mm)*	*Carrier Concentration (/cm²)*	*Mobility (cm²/Vs)*
Atmospheric Adsorbates	*7.2*	*9*	*$8.39x10^{12}$*	*103*
400°C vacuum annealing and in situ 10nm V_2O_5	*4.2*	*3*	*$3.1x10^{13}$*	*55*

Table 7.3.1.1 - TLM and VDP results after fabrication to active level using atmospheric adsorbates, and after 400°C vacuum annealing and in situ deposition of 10nm of V_2O_5.

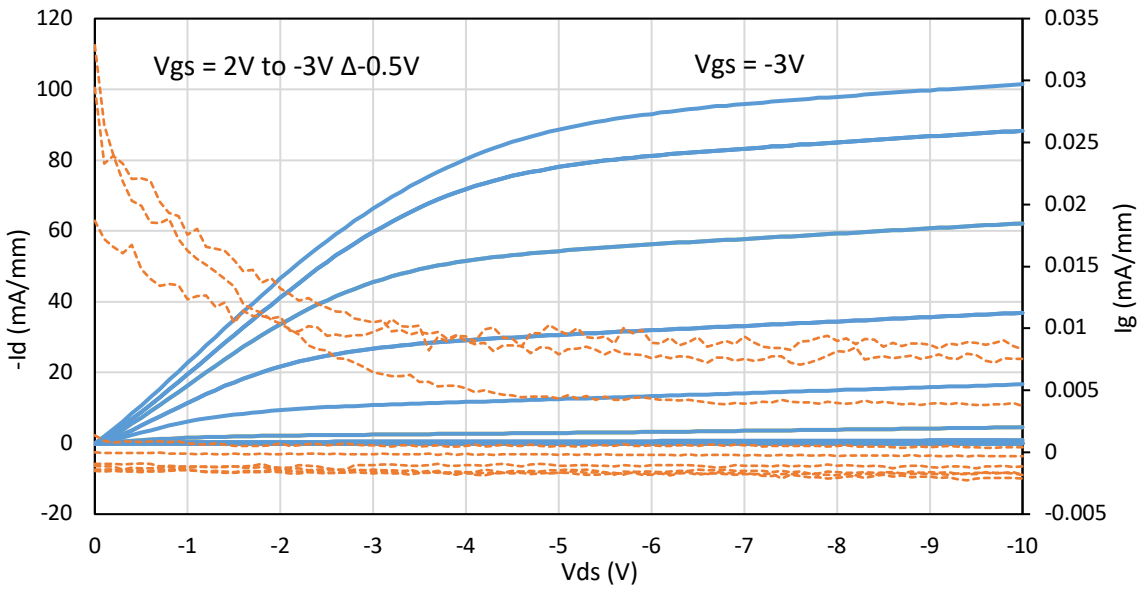

Figure 7.3.1.2- Output characteristics for 0.25µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and gate leakage current is shown in orange.

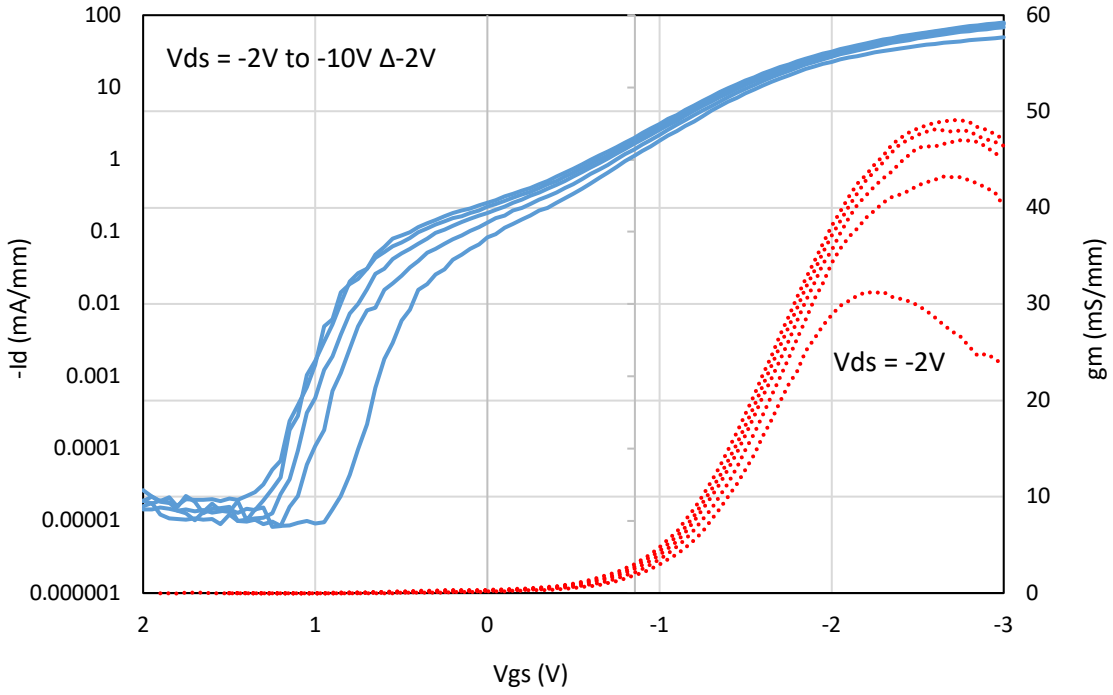

Figure 7.3.1.3 - Transfer characteristics for a 0.25µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

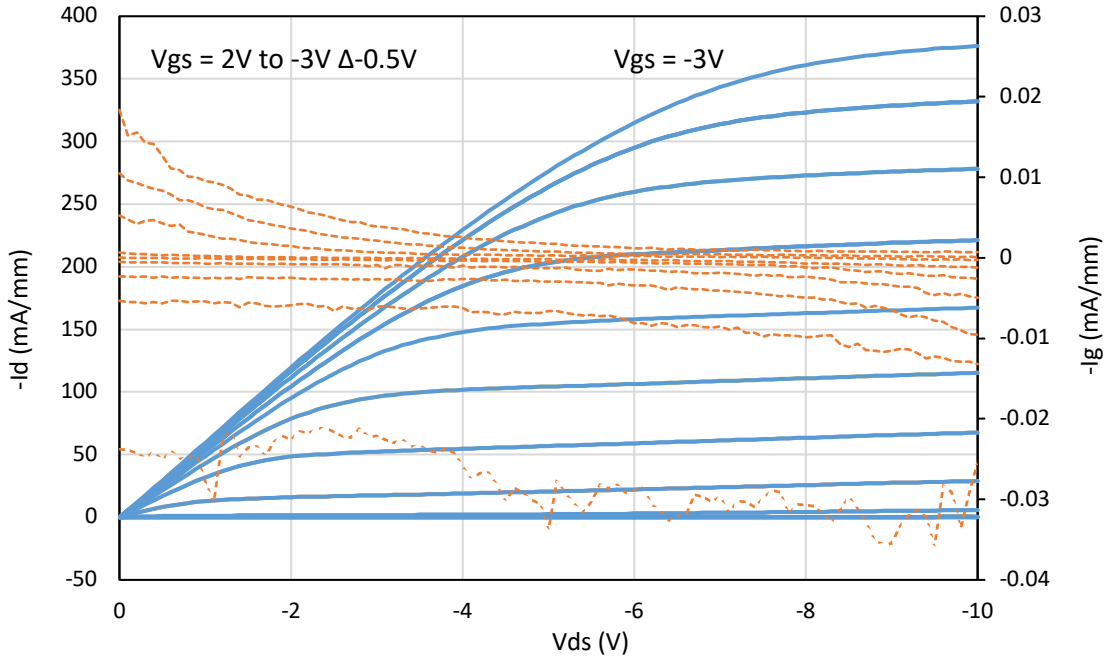

Figure 7.3.1.4 - Output characteristics for a 0.25µm gate length FET with V_2O_5 after in situ 400°C vacuum annealing. Drain current is shown in blue, and gate leakage current is shown in orange.

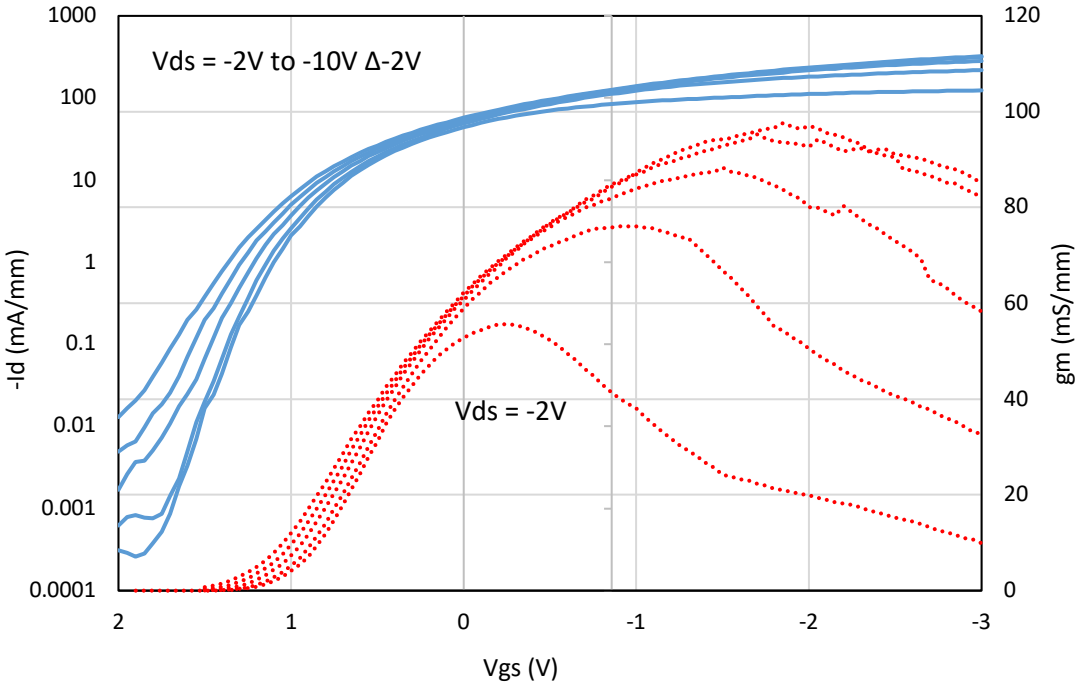

Figure 7.3.1.5 - Transfer characteristics for a 0.25µm gate length FET with V_2O_5 after in situ 400°C vacuum annealing. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

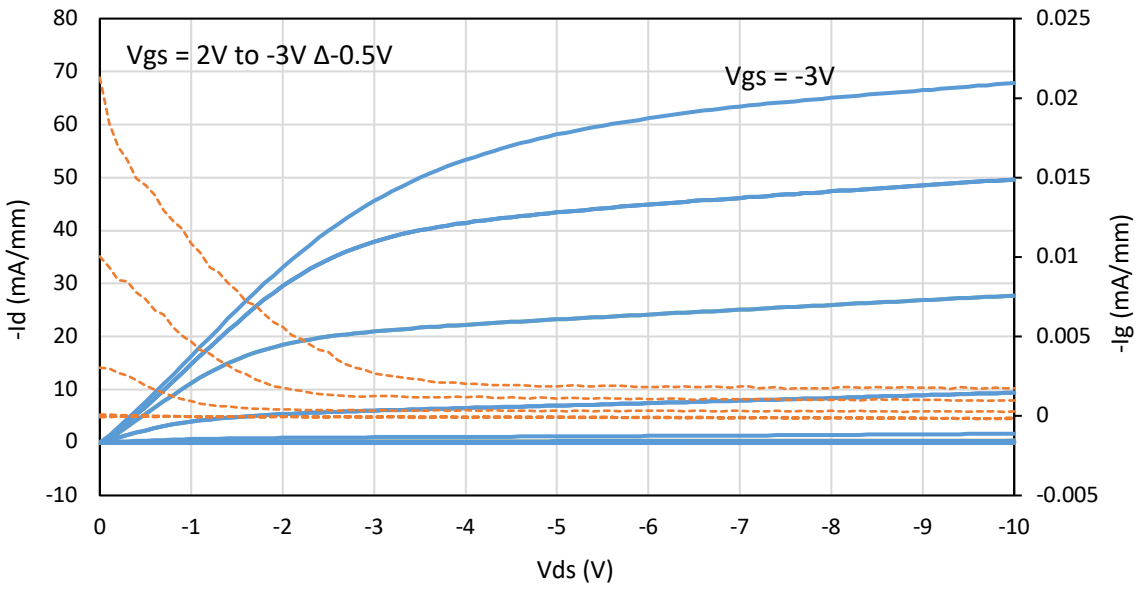

Figure 7.3.1.6 - Output characteristics for a 0.5µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and gate leakage current is shown in orange.

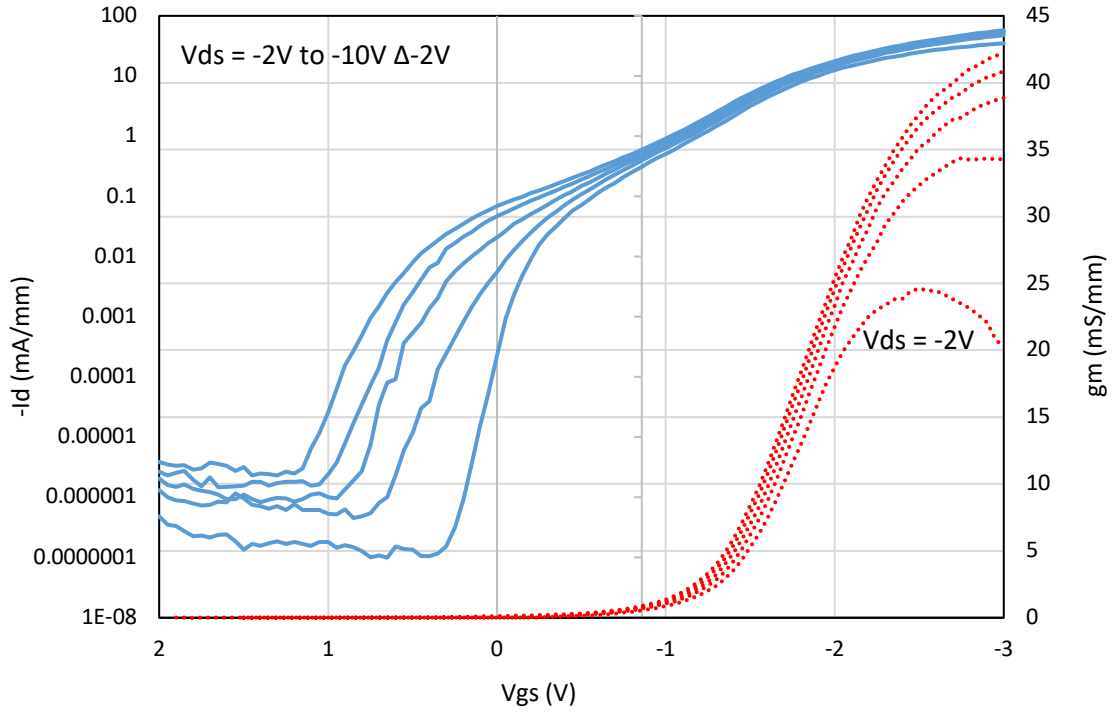

Figure 7.3.1.7 - Transfer characteristics for a 0.5µm gate length FET with atmospheric adsorbates. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

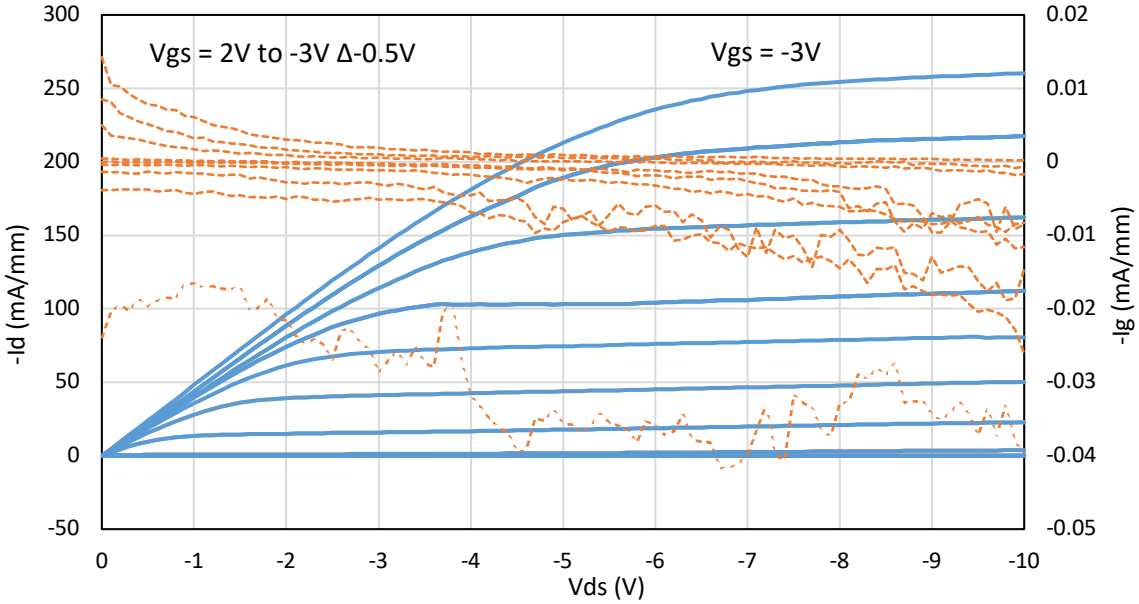

Figure 7.3.1.8 - Output characteristics for a 0.5µm gate length FET with 10nm of V_2O_5 after in situ 400°C vacuum annealing. Drain current is shown in blue, and gate leakage current is shown in orange.

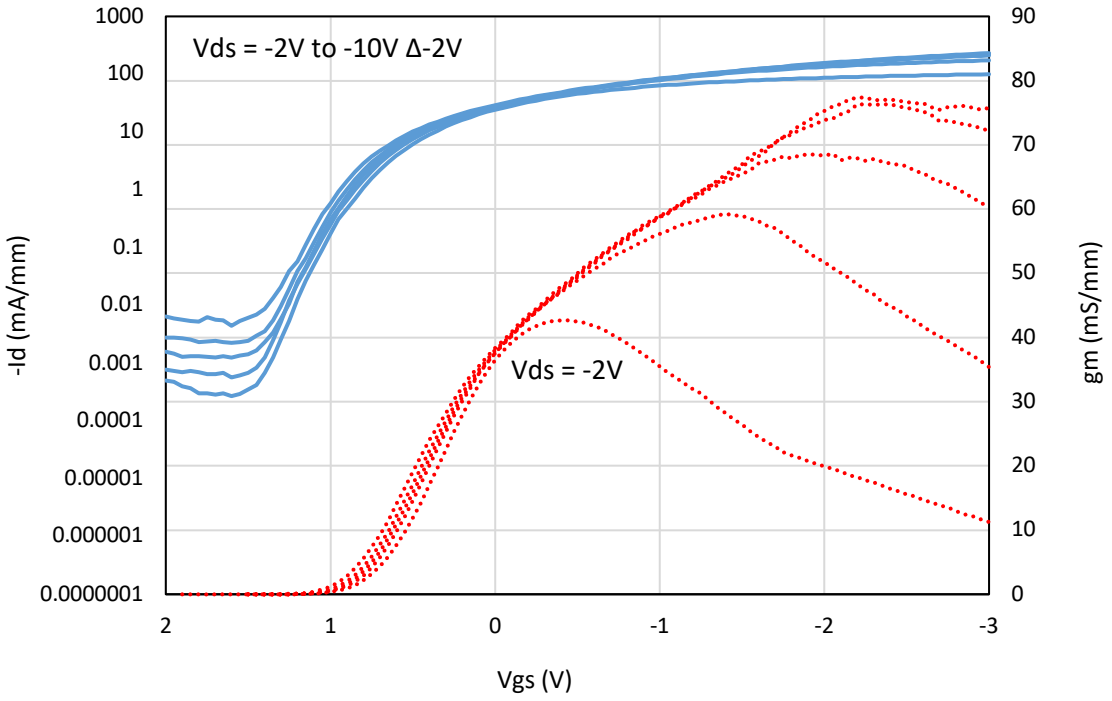

Figure 7.3.1.9 - Transfer characteristics for a 0.5µm gate length FET with 10nm of V_2O_5 after in situ 400°C vacuum annealing. Drain current is shown in blue, and extrinsic transconductance is shown in red dashed.

	Ron Ω.*mm*	R_C Ω.*mm*	R_{CH} Ω.*mm*	R_{GCH} Ω.*mm*	R_s Ω/□	*Idmax (mA/mm)*	*Igmax (mA/mm)*	*gm*	*gm**	*Vth (V)*	I_{on}/I_{off}
Pre anneal and V_2O_5	*44*	*9*	*7*	*10*	*7000*	*-101*	*0.035*	*49*	*287*	*0.45*	10^5
Post anneal and V_2O_5	*17*	*3*	*4.2*	*2.5*	*3700*	*-376*	*0.03*	*97*	*325*	*1.65*	10^3

Table 7.3.1.2 – Key DC figures for a 0.25µm gate length FET with atmospheric adsorbates and after 400°C vacuum annealing and 10nm of V_2O_5 deposition.

	Ron Ω.*mm*	R_C Ω.*mm*	R_{CH} Ω.*mm*	R_{GCH} Ω.*mm*	R_s Ω/□	*Idmax (mA/mm)*	*Igmax (mA/mm)*	*gm*	*gm**	*Vth (V)*	I_{on}/I_{off}
Pre anneal and V_2O_5	*59*	*9*	*7*	*27*	*7000*	*-68*	*0.022*	*43*	*137*	*0.5*	10^6
Post anneal and V_2O_5	*20*	*3*	*4.2*	*5.6*	*3700*	*-260*	*0.04*	*80*	*189*	*1.4*	10^4

Table 7.3.1.3 – Key DC figures for a 0.5µm gate length FET with atmospheric adsorbates and after 400°C vacuum annealing and 10nm of V_2O_5 deposition.

The techniques used to analyse and calculate the results in *Tables 7.3.1.3* and *7.3.1.4* have been discussed in detail in chapter 5.

The threshold voltages for 250nm and 500 FETs were measured to be 0.4V and 0.5V before annealing and V_2O_5 deposition as shown in *tables 7.3.1.2* and *7.3.1.3*. The FETs can be said to be depletion mode as they are "on" at 0V. The MESFET structures shown in chapter 6 demonstrated threshold voltages between 0.75V and 1V for similar gate lengths. The difference is not unexpected as the interface between the Al_2O_3-H-diamond will inevitably be different from the Al-H-Diamond interface of the MESFET structures. The threshold voltage for the MOSFET structures has shifted to 1.65V for a 250nm FET and 1.4V for a 500nm FET after 400°C vacuum annealing and 10nm V_2O_5 deposition. This means the FETs have become more depletion mode. This may imply that the annealing is having a substantial effect on fixed charge at the gate-hydrogen terminated diamond interface. What this effect is remains unclear and could be the subject of further investigation.

It can be seen from the shown output characteristics that the FETs have maintained good transistor action after 400°C vacuum annealing and V_2O_5 deposition.

From *figures 7.3.1.2* and *7.3.1.6*, it can be observed that the maximum drain currents prior to anneal and V_2O_5 deposition are -101mA/mm for a 250nm FET and -68mA/mm for a 500nm FET. After 400°C vacuum annealing and deposition of 10nm of V_2O_5 there has been a dramatic increase in the measured drain currents as can be observed from *figures 7.3.1.4* and *7.3.1.8*. For a 250nm gate length FET a maximum drain current of -376mA/mm and -260mA/mm for a 500nm FET has been measured. The increases in maximum drain current shown here is 275mA/mm for a 250nm FET and 192mA/mm for a 500nm FET. This increase is larger than that reported in chapter 6.6, where a 250nm FET increased by 45mA/mm and a 500nm FET increased by 26mA/mm after 10nm of V_2O_5 deposition and no annealing. This shows that there is most likely an added benefit of including vacuum annealing of the surface prior to 10nm of V_2O_5 deposition in terms of improving device drain current. This may be due to the high temperature annealing desorbing atmospheric species from the surface, improving the interface between the H-diamond and V_2O_5 layer. The MOSFET substrate showed a carrier concentration of $3.1x10^{13}$ and the MESFET substrate in chapter 6.6 showed a carrier concentration of $2x10^{13}$. As these concentrations are similar this may suggest that the dramatic difference in current is due not entirely to variation in the carrier concentration in the channel areas. This may indicate that a substantial amount of the improved performance is due to the effect of the vacuum annealing on the gate structure, rather than any difference in the concentration of carriers in the channel areas of the FETs.

-376mA/mm FET is the highest recorded drain current for an FET on hydrogen terminated diamond using a surface transfer doping oxide such as V_2O_5 and MoO_3 as a surface accepter. This result can be compared to what has been achieved using V_2O_5 as a surface acceptor previously, where a maximum drain current of -280mA/mm was reported for a 2µm gate length MISFET with V_2O_5 as both gate dielectric and surface transfer doping layer[7.9].

The substantial reduction in gate leakage currents observed after annealing and MoO_3 deposition in chapter 7.2 is not observed in this case. Although there has been an increase in gate leakage currents when the gate is "off" from around 0.001mA/mm to 0.03 and 0.04 for a 250nm and 500nm gate length FET respectively after annealing and 10nm of V_2O_5 deposition. This shows that the effects of annealing the Al_2O_3 gate contact are not always consistent, emphasizing the need for further optimization of the gate contact.

As has been discussed previously in 5, the "static" on resistance is the inverse of the gradient of the drain current in the linear region of the output characteristics. The constituent

resistances which make up the "on" resistance can be seen in *equation 7.3.1.1* and *figure 7.3.1.10*.

$$R_{ON} = 2R_C + 2R_{CH} + R_{GCH} \qquad \textit{equation. 7.3.1.1}$$

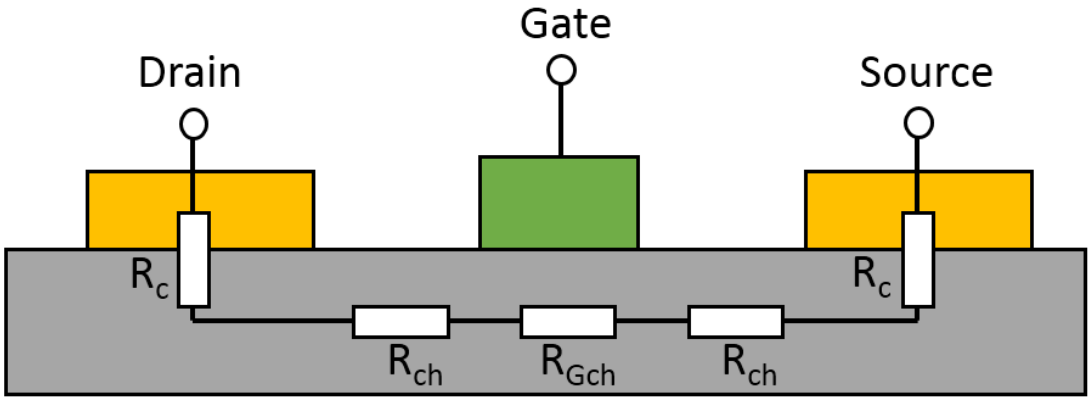

Figure 7.3.1.10 – Simplified FET model showing series resistances in the linear operation region which make up R_{on}.

The on resistances measured from *figures 7.3.1.2* and *7.3.1.6* for the atmospheric adsorbate MOSFETs is 43Ω.mm for a 250nm FET and 59Ω.mm for a 500nm FET. This is comparable to what was reported in chapter 6 for atmospheric MESFETs where a 250nm FET has an on resistance of 54Ω.mm and a 500nm FET had an on resistance of 43Ω.mm. After 400°C vacuum annealing and deposition of 10nm of V_2O_5 the on resistance has decreased to 17Ω.mm for a 250nm FET and 20Ω.mm for a 500nm FET as measured from *figures 7.3.1.4* and *7.3.1.8*. Although a reduction in on resistance after deposition and annealing is expected for the reduction in contact resistance and channel resistance, this does not account for the entire reduction. Inspection of each of the resistances that contribute to R_{on} seems to indicate that the sheet resistances under the gate have also reduced from 10Ω.mm to 2.5Ω.mm for a 250nm FET and from 27Ω.mm to 5.6Ω.mm for a 500nm FET after the anneal and deposition of V_2O_5. This shows that a substantial amount of the reduction in total on resistance is taking place under the gate. The deposition of V_2O_5 should arguably have no effect on the resistance under the gate, and thus it can be proposed that the pre-deposition vacuum annealing at 400°C has had the effect of reducing the sheet resistance under the gate of the MOSFETs.

What mechanisms could cause the observed sheet resistance reduction under the gate is unclear. The Al_2O_3 gate dielectric is deposited prior to annealing of the surface, and thus there may be residual atmospheric adsorbates between the dielectric and the hydrogen terminated diamond surface. The high temperature vacuum annealing may displace the adsorbates at the interface by diffusion through the Al_2O_3 layer, improving the ability of the

gate to accumulate charge at the interface. Clearly this warrants substantial further investigation.

For a 250nm FET the extrinsic transconductance has increased from 49mS/mm to 97mS/mm after vacuum annealing and V_2O_5 deposition as can observed from comparing *figures 7.3.1.3* and *7.3.1.5*. For a 500nm FET there has been an increase in extrinsic transconductance from 43mS/mm to 80mS/mm as can be observed by comparing *figures 7.3.1.7* and *7.3.1.9.* This substantial increase for both 250nm and 500nm FETs shows the benefits of the reduced sheet resistance in the channel and contact resistances after annealing and V_2O_5 deposition. 97mS/mm is higher than the reported peak extrinsic transconductance in literature for V_2O_5 MISFET structures where 80mS/mm was reported[7.9].

Intrinsic transconductances were calculated as 287mS/mm and 137mS/mm for a 250nm FET and 500nm FET respectively with atmospheric adsorbates as can be observed in *tables 7.3.1.2* and *7.3.1.3*. After 400°C vacuum annealing and in situ deposition of 10nm of V_2O_5 the intrinsic transconductances have increased to 325mS/mm and 187mS/mm for a 250nm FET and 500nm FET respectively. This is an increase of 38mS/mm for a 250nm FET and 50mS/mm for a 500nm FET respectively. This again implies that the performance of the gate contact with regards to accumulating charge has been improved by high temperature vacuum annealing and V_2O_5 deposition as the intrinsic transconductance should only account for the area under the gate contact.

Comparing the results in *tables 7.3.1.2* and *7.3.1.3*, it can also be observed that the on/off ratio of the FETs has diminished substantially by 1 order of magnitude from around $1.5x10^5$ to $1.5x10^4$ after 400°C vacuum annealing and 10nm of V_2O_5 deposition. From the displayed output characteristics it would appear that the gate structures' on state performance has increased after annealing, resulting in higher maximum drain currents, and that it's off state performance has been degraded somewhat, resulting in higher off state drain currents. This may indicate that there is more charge under the gate, and a larger voltage is needed fully to deplete the charge away from the interface after 400°C vacuum annealing.

There has not been a substantial decrease in the gate leakage currents as observed for the previous MOSFET structure in chapter 7.1. This could be indicative of the poor optimization of the Al_2O_3 layer resulting in variation in performance between different films deposited on different substrates.

The results shown and discussed here demonstrate the extremely beneficial effects of including V_2O_5 and an in situ pre deposition surface annealing on the DC performance of hydrogen terminated diamond FETs. There has been a recorded increase in maximum drain

current and extrinsic transconductance to the highest values reported for hydrogen terminated diamond FETs using surface transfer doping oxides of 376mA/mm, and 97mS/mm respectively. There has also been a reduction in the total on resistance of the FETs down to 17Ω.mm.

7.3.2 Repeated Measurement on Sample E

As one of the main drawbacks of the atmospheric adsorbates is the associated instability, replacing the atmospheric adsorbates with a surface transfer doping oxide was envisioned to improve operational stability. The previous MESFETs demonstrated in chapter 6.6.2 showed a degradation in maximum drain current of around 8% prior to V_2O_5 deposition with repeated measurements, and a degradation of around 17% after V_2O_5 deposition with no annealing. It is not clear whether the degradation was due to the gate structures, or the surface transfer doping in the channel areas. For comparison, preliminary measurements were taken on the MOSFET structures before and after 400°C vacuum annealing and in situ deposition of 10nm of V_2O_5 in order to assess what effect repeated measurement has on the performance of the MOSFETs. Full output characteristic sweeps were performed 5 times on FETs with gate lengths of 250nm. One FET was chosen to represent the MOSFETs with atmospheric adosrbates, and another to represent the MOSFETs after pre annealing and deposition of 10nm of V_2O_5.

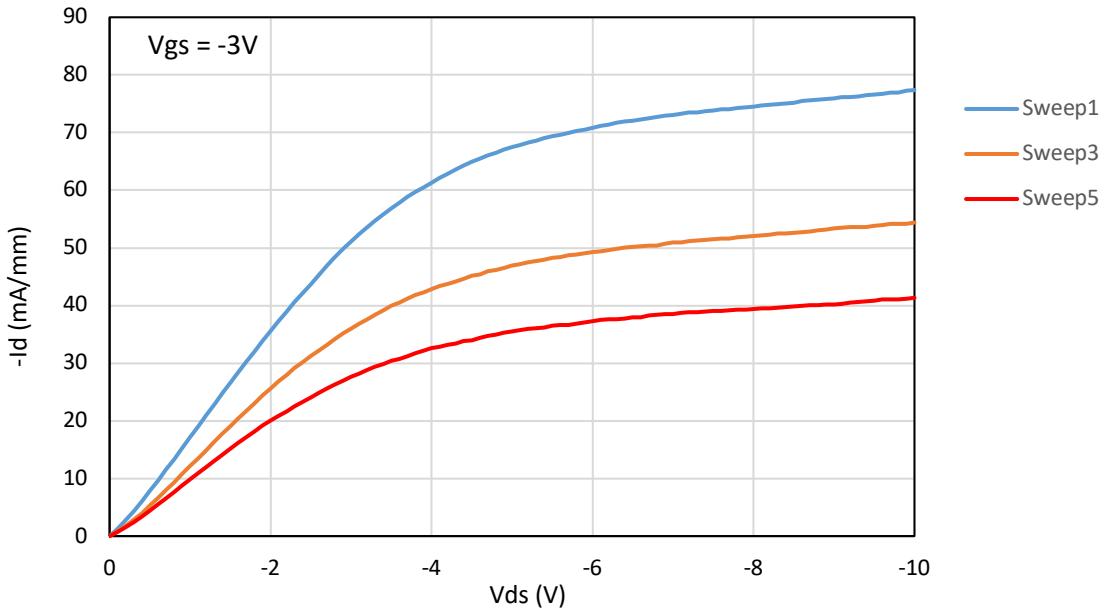

Figure 7.3.2.1 - Output characteristics at Vgs = -3V repeated for a 250nm gate length atmospheric adsorbate FET.

For the MOSFET shown in *figure 7.3.2.1*, after exposure to atmospheric adsorbates there is a decrease in maximum drain current of close to 50% after 5 output characteristic measurements, and the on resistance has increased from 58Ω.mm to 98Ω.mm after 5 measurements. This is a much more dramatic decrease in performance than was observed in the previous MESFET samples. A reduction of this magnitude was not observed for MESFET structures of the same gate size after exposure to atmospheric adsorbates. This may indicate this degradation in performance has been caused by increased trapping from repeated measurements in the Al_2O_3 gate dielectric layer.

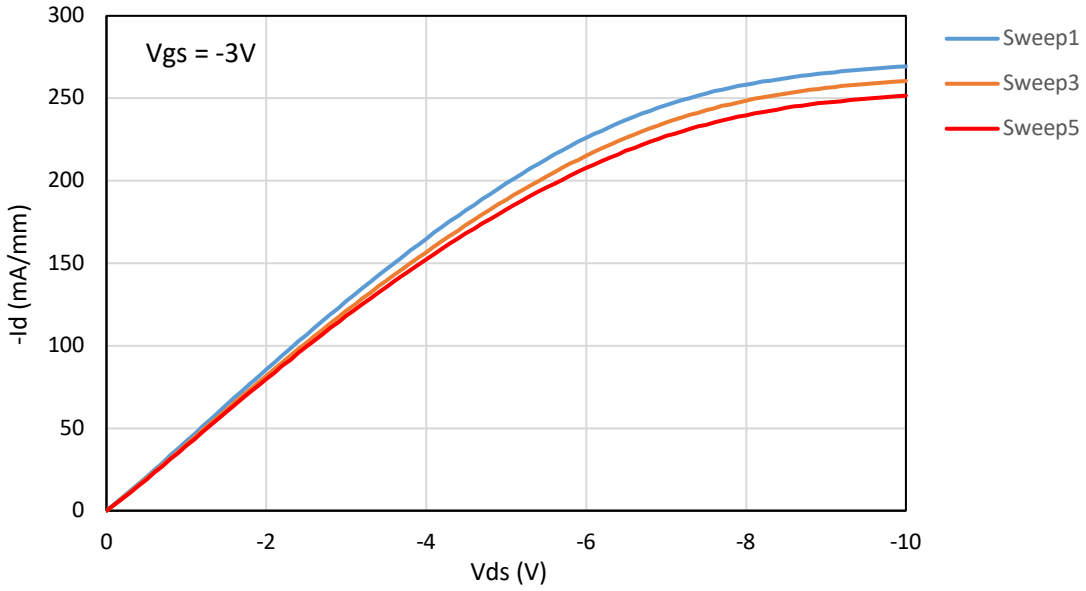

Figure 7.3.2.2 - Output characteristics at Vgs = -3V repeated for a 250nm gate length FET after 400°C vacuum annealing and V_2O_5 deposition.

After annealing and deposition of the surface transfer doping oxide V_2O_5, it can be observed in *figure 7.3.2.2* that the reduction in maximum drain current and sheet resistance is much less dramatic than was observed prior to annealing and V_2O_5 deposition. The reduction in maximum drain current is only around 5% after 5 output characteristic measurements. This comparable to what has been reported in literature for repeated measurement of FETs where MoO_3 passivated FETs with MoO_3 as a gate dielectric showed a reduction of 3% maximum drain current after 3 measurements [7.10]. The on resistance measured in *figure 7.3.2.2* increased from 23Ω.mm to 25Ω.mm after 5 measurements, a change of just 2Ω.mm. The MESFETs shown in chapter 6.6.2 showed an increase of 8Ω.mm after 5 measurements after deposition of V_2O_5 with no pre-deposition annealing. The results here may indicate that the annealing of the Al_2O_3 gate contact has improved the performance with regards to repeated measurement.

The difference between the repeated measurements before and after high temperature vacuum annealing and V_2O_5 deposition is dramatic. Whether the improvement is due to the annealing of the FET structures, or the deposition of V_2O_5 requires further investigation. The 400°C vacuum annealing may have had an effect of passivating or moving trapping states away from the interface resulting in less trapping events from repeated measurement in the Al_2O_3 gate dielectric.

7.3.3 Off-state breakdown measurements on Sample G

The previously demonstrated MESFET structures in chapter 6.6.4 showed poor off state performance, with "breakdown" occurring at voltages of around -20V (as discussed in chapter 5 breakdown has been defined for this work as the drain voltage at which the drain current exceeds 0.1mA/mm) which can be observed in *figure 7.3.3.1*. It was decided to continue preliminary investigation of the breakdown of the fabricated FETs by measuring the breakdown voltages of fabricated MOSFETs before and after 400°C vacuum annealing and in situ V_2O_5 deposition compare with the results acquired for MESFET structures fabricated and discussed in chapter 6.6.4.

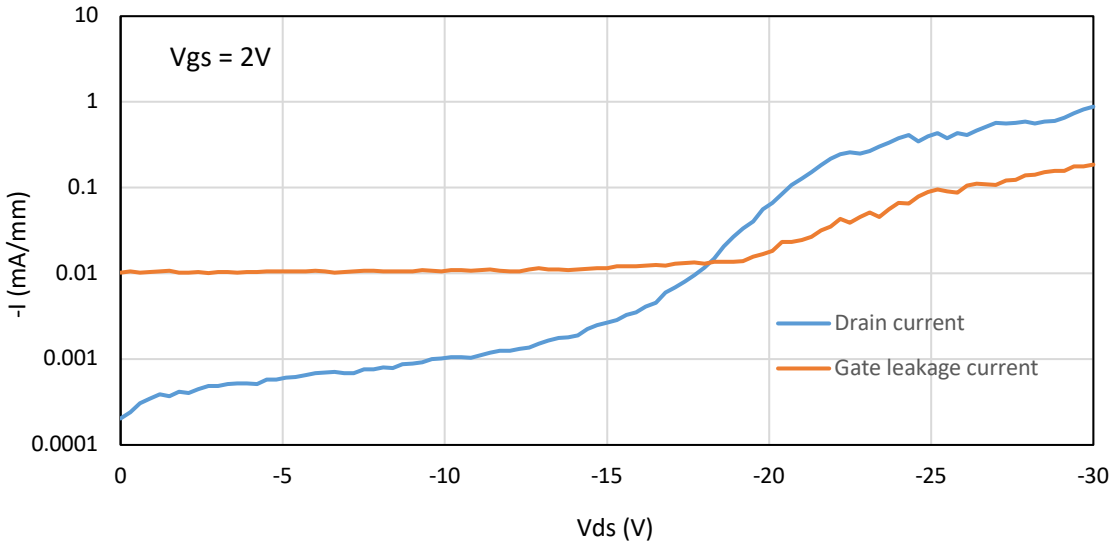

Figure 7.3.3.1 – Shows off state drain current with Vgs = 2V for MESFET with 250nm gate length with atmospheric adsorbates.

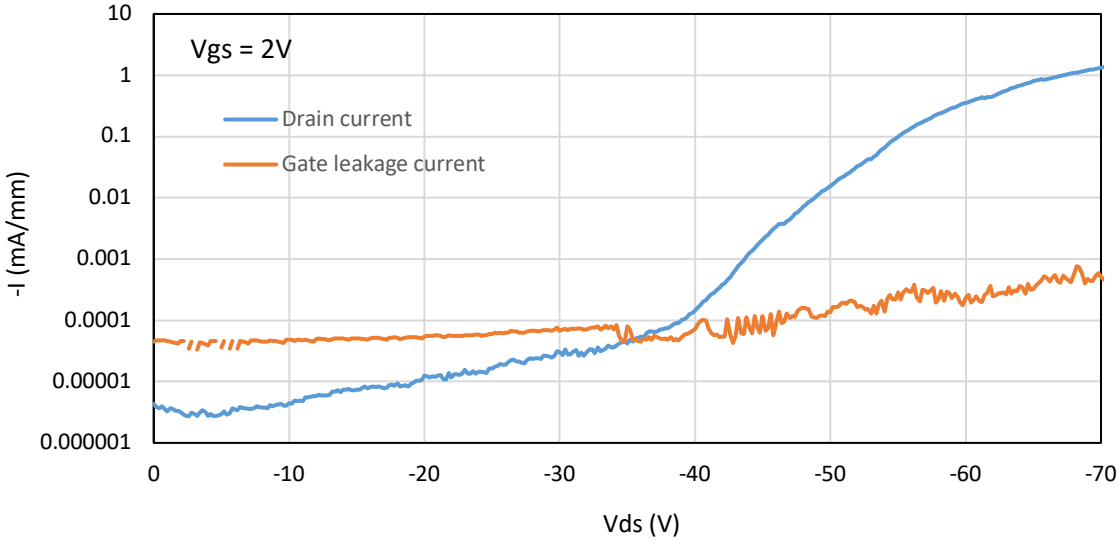

Figure 7.3.3.2 – Shows off state drain current with Vgs = 2V for MOSFET with 250nm gate length with atmospheric adsorbates.

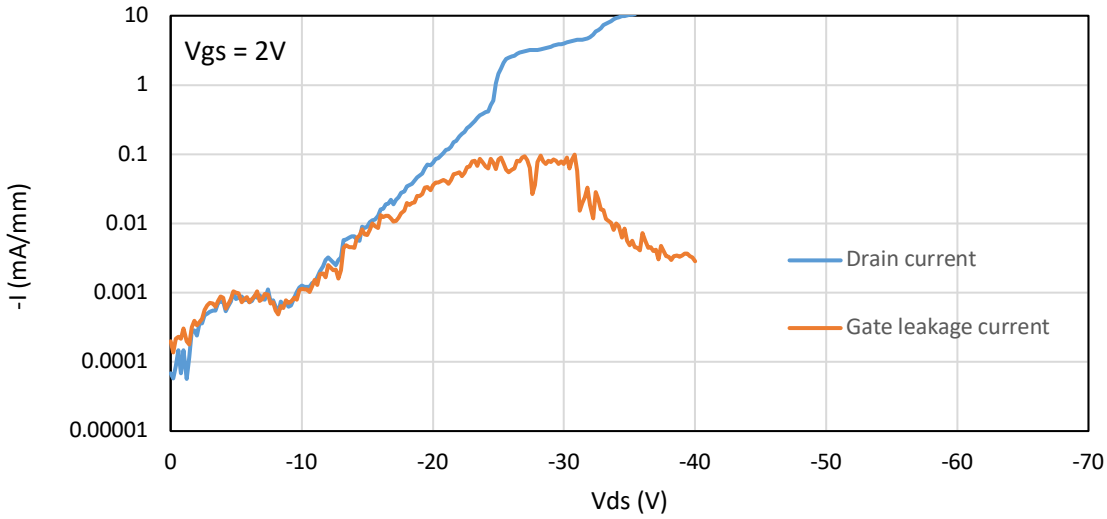

Figure 7.3.3.3 – Shows off state drain current with Vgs = 2V for MOSFET with 250nm gate length after 400°C vacuum annealing and in situ 10nm of V_2O_5 deposition.

From *figures 7.3.3.1* and *7.3.3.2* the difference in breakdown voltage between the MESFET structures and MOSFET structures of the same gate length can be observed. Prior to annealing and V_2O_5 deposition, the inclusion of the Al_2O_3 dielectric layer appears to have increased the breakdown voltage of the structures significantly from around -20V to almost -55V for a 250nm gate length FET. The gate leakage does not appear to be the dominant breakdown mechanism in the devices with Al_2O_3 as a gate dielectric as the gate leakage current does not increase as drastically as the drain current after -50V. The majority of the

off state leakage after -40V can be attributed to source-drain leakage. Similarly to what was noted in chapter 6.6.4, after high voltage measurement there is no evidence of mechanical damage to any of the contacts.

After 400°C annealing and deposition of V_2O_5 into MOSFET structures there has been a reduction in the off state breakdown voltage from -50V to around -20V which can be observed by comparing *figures 7.3.3.2* and *7.3.3.3.* The magnitude of the gate leakage current has increased dramatically, and matches the drain current until around -20V drain bias. After this point the source-drain leakage current begins to dominate.

Although the preliminary results show that the off state performance can be improved by incorporating the dielectric Al_2O_3 in the gate structure of hydrogen terminated diamond FETs, it is unfortunate that the 400°C vacuum annealing appears to reduce the off state breakdown predominantly through increased gate leakage. This provides further evidence that the Al_2O_3 gate dielectric is being modified substantially by the anneal and V_2O_5 deposition. It is clear that the breakdown mechanisms require substantial further investigation and that the gate structures still require substantial optimization in order to maintain the high breakdown voltage of the MOSFET structures after 400°C vacuum annealing and V_2O_5 deposition.

7.4 Conclusions

The inclusion of surface transfer doping oxides and pre deposition surface annealing has successfully shown improved MOSFET performance in terms of drain current, transconductance and on resistance. The results acquired from these MOSFETs show the best DC characteristics reported for hydrogen terminated diamond FETs using surface transfer doping oxides V_2O_5 and MoO_3.

The highest maximum drain current of 376mA/mm, extrinsic transconductance of 97mS/mm and lowest on resistance of 17Ω.mm for hydrogen terminated diamond using surface transfer doping oxides has been achieved in this work and reported in IEEE EDL [7.11]. Although the results are not yet as impressive in comparison to that achieved using NO_2 encapsulated with Al_2O_3 where 1.3A/mm maximum drain current [7.12] has been achieved it is still very promising that there are alternative routes to demonstrating the potential of hydrogen terminated diamond FETs.

Although the demonstrated on state characteristics have been impressive. Preliminary measurements have shown a degradation of the Al_2O_3 gate dielectric in regards to breakdown voltage from -55V to -20V after high temperature vacuum annealing and V_2O_5 deposition.

Preliminary results also suggest that the off state currents have increased by an order of magnitude after vacuum annealing and deposition of V_2O_5.

Although the on state DC results are encouraging, there is still substantial engineering of the gate contact required in order to provide the best results in both the on and off state, which are both important operating regions for high power FETs.

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8 Conclusions and further work

8.1 Conclusions

Diamond has the potential to deliver excellent FET performance in terms of high power and high frequency performance, and operation at high temperatures due to its intrinsic material properties as discussed in detail in previous chapters. Hydrogen-terminated diamond FETs have sought to take advantage of these intrinsic properties and have shown some success in regards to both high frequency performance, where a maximum oscillation frequency (f_{max}) of 120 GHz[8.1] and cut off frequency (f_T) of 53GHz have been achieved [8.2], and high power performance, where a power output density of over 2W/mm at 1GHz has been achieved[8.3]. However the reliance on surface atmospheric adsorbates for doping has limited the exploration of hydrogen terminated FETs as they provide inconsistent performance due to their unstable nature and the adsorbates begin to sublimate from the surface of the diamond at temperatures as low as 60°C[8.4].

Replacing atmospheric adsorbates with alternative surface transfer doping materials such as MoO_3 and V_2O_5 has been shown to lead to higher carrier concentration in the 2DHG, and more consistent performance at elevated temperatures[8.5]. Thus far, integration of these alternative surface transfer doping materials into hydrogen terminated diamond FETs has proved challenging, and the FETs fabricated have yielded maximum drain currents and extrinsic transconductances lower than anticipated [8.6-8].

This thesis set out to investigate new strategies for the incorporation of MoO_3 and V_2O_5 into hydrogen terminated diamond FETs, and the potential improvement to important parameters for high performance FETs; maximum drain current, peak transconductance, and on resistance.

It was discussed in chapter 6 that 400°C vacuum annealing prior to the deposition of either MoO_3 or V_2O_5 layers is required in order to maximize the stability of the 2DHG over time[8.5]. The incorporation of this anneal stage in a FET production process flow was also observed to substantially decrease ohmic contact resistance but resulted in the degradation in the operation of MESFET devices. Which was attributed to thermal-induced damage to the gate metal:H-diamond contact. Following this, MESFET devices that incorporated MoO_3 and V_2O_5 without annealing of the surface prior to deposition was explored by comparing electrical characterization acquired with atmospheric adsorbates and after deposition of 10nm of MoO_3 or V_2O_5 layers. This demonstrated that the maximum drain current, peak

transconductance and on resistance of hydrogen terminated diamond FETs could be improved by deposition of MoO_3 or V_2O_5 without pre deposition annealing and suggested that the anneal stage was indeed degrading the MESFET structure.

Following this, the fabrication of MOSFET structures including Al_2O_3 as a gate dielectric was explored in chapter 7. This was intended to improve the thermal robustness of the gate contact to allow inclusion of the pre deposition 400°C vacuum annealing of the diamond surface prior to deposition of MoO_3 or V_2O_5 without degrading device performance. The inclusion of 10nm of MoO_3 or V_2O_5 with pre deposition 400°C vacuum annealing on the MOSFET structures resulted in greatly improved DC performance compared the results measured using atmospheric adsorbates. MOSFETs including V_2O_5 showed the best DC performance recorded for hydrogen terminated diamond FETs using surface transfer doping oxides at the time of writing. The largest maximum drain current of -376mA/mm, extrinsic transconductance of 97mS/mm and lowest on resistance of 17Ω.mm for hydrogen terminated diamond using surface transfer doping oxides has been recorded in this work.

Preliminary comparisons between the breakdown voltages and breakdown characteristics for MESFET and MOSFET structures has also been carried out in chapters 6 and 7. For 250nm gate length FETs with a gate-drain gap of approximately 1µm a -20V breakdown was measured for MESFET structures, and a -50V breakdown was observed for MOSFET structures prior to annealing and V_2O_5 deposition. Although this increase in breakdown voltage is encouraging, 400°C vacuum annealing of the MOSFETS with Al_2O_3 as a gate dielectric reduced the breakdown voltage to -20V. It is clear that the gate dielectric requires substantial further optimization in order to take full advantage of the effects of the 400°C vacuum annealing prior to V_2O_5 or MoO_3 deposition.

8.2 Further Work

Although the results explored in this thesis have been encouraging, there is still a wealth of research to be undertaken with regards to improving the high power performance, and high temperature operation of hydrogen terminated diamond FETs.

It has been observed in chapters 6 and 7 that 400°C vacuum annealing of the completed devices prior to the deposition of MoO_3 or V_2O_5 resulted in reduced ohmic contact resistance. The mechanism which results in reduced ohmic contact resistance is not clear at this time and warrants further and much more detailed investigation. The improved contact resistances measured in this work are at the lowest 3Ω.mm. This is still considerably large when compared to reported values for other materials such as GaN where contact resistances

as low as 0.1Ω.mm have been demonstrated [8.9]. It would be imperative for high power FET performance to further investigate minimizing the contact resistance of hydrogen terminated diamond FETs in order to minimize the total on resistance. As there is, at the time of writing, a lack of systematic investigation into the operation of the ohmic contacts on hydrogen terminated diamond, this would allow for a methodical investigation into alternative materials or fabrication methods of the ohmic contacts. Titanium carbide (TiC) contacts have been demonstrated successfully, however the high temperatures (600°C) required to form the TiC contact necessitate a "hydrogen termination last" approach, which requires substantial reworking of the existing H-diamond fabrication processes[8.10].

Furthermore, the quality of the gate dielectric could be improved in order to further reduce gate leakage currents by using different methods of fabricating gate dielectrics such as Atomic Layer Deposition (ALD). Alternative dielectrics could also be explored to this end. Alternative gate dielectrics such as HfO_2 [8.11] and TiO_2 [8.12] and Y_2O_3[8.13] have previously shown success on hydrogen terminated diamond. The observed adverse effect of 400°C vacuum annealing on the breakdown voltage of MOSFETs using Al_2O_3 as a gate dielectric observed in this work may be avoided by using a more robust gate dielectric. It was observed that annealing of the gate oxide shifted the threshold voltages of the fabricated FETs using Al_2O_3 as a gate dielectric. If annealing, or the use of different gate metals, or dielectrics could shift the threshold voltage to become enhancement mode FETs this could be very useful as it is desirable to have both enhancement and depletion mode FETs on the same substrate. It is also desirable for high power applications to have normally-off devices [8.14]. Enhancement mode operation of H-diamond FETs has been demonstrated using Y_2O_3 as a gate dielectric [8.13]. A systematic study of the operation of the gate contact and its operation would be beneficial in order to further understand how it can be improved.

High temperature applications for diamond FETs are key targets for this technology. High temperature performance of FETs fabricated on hydrogen terminated diamond using atmospheric adsorbates has so far been unable to take advantage of this. Utilizing surface transfer doping oxides such as V_2O_5 and MoO_3 is hoped to provide better stability of operation at elevated temperatures. If time allowed, the performance of the fabricated FETs would have been assessed at temperatures from room temperature to 300°C in this work. Literature suggests that V_2O_5 and MoO_3 should maintain the stability of the 2DHG at temperatures above 200°C [8.5]. The operational temperature could be further improved by exploring alternative surface transfer doping oxides or exploring encapsulation of the surface transfer doping oxides with more robust passivation such as Al_2O_3 or silicon nitride (SiN).

MOSFET operation up to 400°C has been demonstrated using Al_2O_3 as a gate dielectric and surface passivation [8.15].

The most prevalent and successful method of fabricating hydrogen terminated diamond FETs has thus far relied on a symmetrical undercut etch of the "sacrificial Au layer" to form the source-drain gap and ohmic contacts, followed by deposition of the gate contact in the middle. A non-self-aligned gate process could provide more flexibility for increasing off state breakdown voltages by allowing increased distance between the gate and drain contacts, reducing the concentration of the electric field. However this would require substantial reworking of the existing technology. The gold "sacrificial" layer also serves to protect the hydrogen termination of the diamond during fabrication. The thermal budget of fabrication processes is reduced by the efforts to preserve the hydrogen termination of the surface, as it can be removed from the surface at temperatures above 230°C under normal environmental conditions[8.16]. A hydrogen termination last approach has been demonstrated successfully[8.10], this could open the exploration of alternative fabrication processes requiring increased thermal budget, or chemical processes which would otherwise damage the hydrogen termination in existing FET processing.

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Appendix A – Process sheets

Marker Deposition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C - IPA rinse - Blow dry with N2 gun
Resist Spin:	- 12% 2010 PMMA spun at 5k RPM for 60 s - 120° C bake for 20 min - 4% 2041 PMMA spun at 5k RPM for 60 s - 120° C bake for 20 min
Metallisation:	- Deposit 20 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 700 μCcm-2, 64 nA beam spot size, VRU 40
Metal Etch:	- MF CD-26 soak for 2 minutes - RO water rinse - Blow dry with N2 gun
Development:	- MIBK:IPA (1:1) soak for 30 s at 23° C - IPA rinse - Blow dry with N2 gun
Resist Ash:	- O2 plasma at 80 W for 2 minutes
Metallisation :	- 20nm Titanium followed by 80nm Gold
Lift-Off:	- 2 hour soak in acetone at 50° C - IPA rinse - Blow dry with N2 gun

Isolation

Substrate Cleaning:	- 20 minute soak in acetone at 50° C

	- IPA rinse
	- Blow dry with N2 gun
Resist Spin:	- S1805 spun at 4000k RPM for 30s
	- 115°C hotplate bake for 3 minutes
Isolation:	- Alignment gap 50um, Hard contact, 2.3s exposure
Development:	- 1:1 Microposit concentrate:RO 75s
	- RO water rinse
Resist Ash:	- O2 Plasma 100W for 3 minutes
Gold Etch:	- 1:4 Au etch (clean room bottle): RO water etch for 20s
	- Rinse in RO water
Isolation:	- O2 Plasma 80W for 3 minutes
Isolation test:	- IV on isolation test structures

Bond pads

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N2 gun
Pre bake (Dehydration):	- 180°C degrees for 5 minutes
Resist Spin:	- LOR 5A spun at 3000k RPM for 45 seconds
	- 180C hotplate bake for 5 minutes
	- Allow 5 minutes for resist to cool after bake
	- S1805 spun at 4000k RPM for 30s
	- 115°C hotplate bake for 3 minutes
Bond pads:	- Alignment gap 50um, Hard contact, 2.3s exposure

Development:	- 1:1 Microposit concentrate:RO 75s - RO water rinse - 5 mins 100W ash - Cure resist 120 degrees oven bake 30 minutes - MF-CD26 60s - Ro water rinse
Resist Ash:	- O2 Plasma 80W for 2 minutes
Metallisation:	- 20nm Titanium followed by 200nm Gold
Lift-off:	- SVC-14 overnight - IPA rinse

"Active" level

Substrate Cleaning:	- 20 minute soak in acetone at 50° C - IPA rinse - Blow dry with N2 gun
Resist Spin:	- S1805 spun at 4000k RPM for 30s - 115°C hotplate bake for 3 minutes
Active:	- Alignment gap 50um, Hard contact, 2.3s exposure
Development:	- 1:1 Microposit concentrate:RO 75s - RO water rinse
Resist Ash:	- O2 Plasma 100W for 3 minutes
Gold Etch:	- 1:10 Au etch (clean room bottle): RO water etch for 15s at 60°C - Rinse in RO water

Gate etch and deposition (MESFET)

Substrate Cleaning:	- 20 minute soak in acetone at 50° C

	- IPA rinse - Blow dry with N2 gun
Resist Spin:	- 12% 2010 PMMA spun at 5k RPM for 60 s - 120° C bake for 20 min - 4% 2041 PMMA spun at 5k RPM for 60 s - 120° C bake for 20 min
Metallisation:	- Deposit 20 nm Al via e-beam evaporation
Electron Beam Lithography:	- Gate dose 2100 μCcm-2, 8 nA beam spot size, VRU 10 - Gate pad dose 1500 μCcm-2, 32 nA beam spot size, VRU 32
Metal Etch:	- MF CD-26 soak for 2 minutes - RO water rinse - Blow dry with N2 gun
Development:	- MIBK:IPA (1:1) soak for 30 s at 23° C - IPA rinse - Blow dry with N2 gun
Resist Ash:	- O2 plasma at 80 W for 60 s
Metal Etch:	- 1:10 Au etch (clean room bottle): RO water etch for 15s at 60°C - Rinse in RO water
Metal deposition:	- 20nm Aluminium, 20nm Platinum, 40nm Gold
Lift-Off:	- 2 hour soak in acetone at 50° C - IPA rinse - Blow dry with N2 gun

Gate etch and deposition (MOSFET)

Substrate Cleaning:	- 20 minute soak in acetone at 50° C - IPA rinse - Blow dry with N2 gun
Resist Spin:	- 12% 2010 PMMA spun at 5k RPM for 60 s - 120° C bake for 20 min - 4% 2041 PMMA spun at 5k RPM for 60 s - 120° C bake for 20 min
Metallisation:	- Deposit 20 nm Al via e-beam evaporation
Electron Beam Lithography:	- Gate dose 2100 μCcm-2, 8 nA beam spot size, VRU 10 - Gate pad dose 1500 μCcm-2, 32 nA beam spot size, VRU 32
Metal Etch:	- MF CD-26 soak for 2 minutes - RO water rinse - Blow dry with N2 gun
Development:	- MIBK:IPA (1:1) soak for 30 s at 23° C - IPA rinse - Blow dry with N2 gun
Resist Ash:	- O2 plasma at 80 W for 60 s
Metal Etch:	- 1:10 Au etch (clean room bottle): RO water etch for 15s at 60°C - Rinse in RO water
Dielectric deposition:	- 10nm Alumina
Metal deposition:	- 20nm Aluminium, 20nm Platinum, 30nm Gold
Lift-Off:	- 2 hour soak in acetone at 50° C - IPA rinse - Blow dry with N2 gun