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Fabrication and Characterisation of InP/InGaAs Heterojunction Bipolar Transistors

By
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(by dissertation)

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Supervisor: Dr. Edward Wasige
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Abstract

Heterojunction bipolar transistors (HBTs) have well established themselves since the invention of modern day epitaxial growth technology in nearly all areas of electronic integrated circuits varying from high speed Indium Phosphide (InP) based devices through to future high-power gallium nitride (GaN) applications.

This thesis begins with a review of the current state of the art HBT devices, along with comparison between different materials used within such devices. A large portion of the work covers the fabrication process of an Indium Phosphide/ Indium Gallium Arsenide (InP/InGaAs) based Single-HBT (SHBT) using only wet etching, along with the comparison between different techniques involved. RF and DC measurements for the fabricated devices are also reported of HBTs with emitter size $16\mu\text{m} \times 8\mu\text{m}$ with achieving speeds of F_{MAX} and F_{T} being, 3.5GHz and 9GHz respectively.

Finally, being that the accurate extraction of the small-signal equivalent circuit is a crucial part in the process development and optimisation of HBTs, the investigation and development of an accurate small signal device modelling technique was evaluated and developed this project.

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List of Symbols and Acronyms

ρ	The net charge density
β	DC current gain
τ_b	Base transit time
τ_c	Collector charging time
τ_e	Emitter charging time
ϵ_r	Relative permittivity of the dielectric (F/m)
τ_{sc}	Space-charge transit time
ΔE_g	Total band gap discontinuity difference
ΔE_v	Valence band discontinuity at the base-emitter hetero-interface
ΔE_v	Discontinuity in the valence band
A	Degree of isotropy
AC	Alternating current
Al	Aluminium
AlGaAs	Aluminium gallium arsenide
Au	Gold
B	Base
BJT	Bipolar junction transistor
C	Collector
C_{BC}	Total base-collector capacitance
C_{BCI}	Intrinsic base-collector capacitance
C_{BCX}	Extrinsic base-collector capacitance
C_{BE}	Base-emitter capacitance
C_{pbc}	Parasitic base-collector capacitance
C_{pbe}	Parasitic base-emitter capacitance
C_{pce}	Parasitic collector-emitter capacitance
Cr	Chrome
DC	Direct current
DHBT	Double heterojunction bipolar transistor
D_{nB}	Minority electron diffusion in the base
D_{nB}	Minority electron diffusion in the base
D_{pE}	Minority hole diffusions coefficient in emitter
DuT	Device-under-test
E	Emitter
E_{BI}	Electron back injection
E_{CE}	Emitter conduction band level

E_{FB}	Base fermi level
E_{FE}	Emitter fermi level
E_g	Band gap (in eV)
E_{gB}	Base band gap in eV
E_{gE}	Emitter band gap in eV
E_{VB}	Base Valence band level
f	Frequency
FET	Field-effect transistors
F_{MAX}	Unity power gain
F_T	Unity current gain
GaAs	Gallium arsenide
GaN	Gallium nitride
Ge	Germanium
H ₂ O	Water
H ₂ O ₂	Hydrogen peroxide
H ₃ PO ₄	Phosphoric acid
H _{BI}	Home back injection
HBT	Heterojunction bipolar transistor
HCL	Hydrochloric acid
HEMT	High electron mobility transistor
I_B	Base current
I_C	Collector current
I_E	Emitter current
InAlAs	Indium aluminium arsenide
InGaAs	Indium gallium arsenide
InGaP	Indium gallium phosphide
InP	Indium phosphide
IV	Current-Voltage
JWNC	James Watt Nanofabrication Centre
k	Boltzmann's constant
L_b	Extrinsic base inductance
L_c	Extrinsic collector inductance
L_e	Extrinsic emitter inductance
LNA	Low noise amplifiers
LPE	Liquid phase epitaxy
MBE	Molecular beam epitaxy
Mn	Manganese

MOCVD	Metal organic chemical vapour deposition
MS D-FF	Master slave D-type flip flop
N_B	Base doping
N_B	Base doping density
N_{dopant}	Dopant levels
N_E	Emitter doping
N_E	Emitter doping density
Ni	Nickel
Pd	Palladium
Pt	Platinum
q	Electric charge
$R_{b,\text{cont}}$	Base contact resistance
$R_{b,\text{spread}}$	Base spreading resistance
R_{BB}	Total base resistance
$R_{b\text{gap}}$	Base-emitter gap resistance
R_c	Collector resistance
R_{con}	Contact resistance
R_e	Emitter resistance
RF	Radio frequency
R_L	is the lateral etch rate
R_{total}	Total resistance
R_V	is the vertical etch rate
SHBT	Single heterojunction bipolar transistor
Si	Silicon
SiGe	Silicon germanium
t	Thickness of dielectric (metres)
T	Temperature in Kelvin
T_B	Base thickness
T_{dep}	Base-collector depletion region thickness
T_{dep}	Depletion region thickness
T_E	Emitter thickness
Ti	Titanium
TiW	Titanium Tungsten
TLM	Transmission line measurement
UV	Ultraviolet
V_{BC}	Base-collector voltage
V_{BE}	Base-emitter voltage

V_{bi}	Built in potential voltage
V_{BV}	Breakdown voltage
V_N	Potential difference between the conduction band and fermi level in the emitter
V_P	Potential difference between the fermi level and the valence band in the base
V_{sat}	Saturation voltage
V_T	Threshold voltage
W	Tungsten
W_{dep}	depletion width
X_s	Electron affinity of the semiconductor
ΔE_C	Discontinuity in the conductance band
ϵ_0	Permittivity of free space(F/m)
T_b	Base transit-time
Φ_{Bn}	Barrier heights of n-type material
Φ_{Bp}	Barrier heights of p-type material
Φ_m	Work function of the metal
χ^B	Electron affinities of the base
χ^E	Electron affinities of the emitter

1. Introduction

Since the 1970's with the fabrication of the first heterojunction bipolar transistor (HBT), the technology has successfully established itself in current day commercial applications. This is due to the higher performance offered by HBTs in comparison to other devices such as field-effect transistors (FET) and/or high electron mobility transistors (HEMTs) due to their strong linearity, low $1/f$ noise characteristic with high frequency and high speed performance.

1.1. History

The history behind HBTs started with Thomas Edison who first discovered the theoretical principle of a basic diode [1], the testing of which led to the description of the process being known as the Edison effect. It was in 1906 however, when John Fleming followed on with Edison's work and developed a vacuum diode [2] that it became accepted as the start of the electronics journey to its current widespread application use of today. This diode used thermionic emission to form a one-way valve for electrical current which allowed the conversion of alternating current (AC) to direct current (DC) and the processing of high frequency signals

In 1906 Lee De Forrest expanded on Fleming's work by incorporating a third electrode into the vacuum diode to form a triode [3]. This new vacuum tube triode was an improvement on the Fleming's diode as it not only rectified the AC signal but also boosted it, this making it the first amplifier. It was this triode that was developed as a radio detector and resulted in the triode being a key component in electronic systems until the 1940's with the invention of the first transistors.

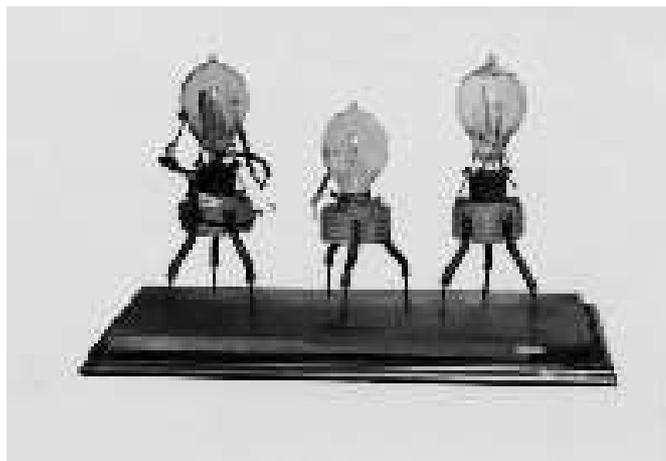


Figure 1-1: Fleming's first vacuum diodes [4]

In 1947, with the invention of the first Germanium based solid state transistor [5] by J. Bardeen and W. Brattain that the next evolution step occurred. Up until then, virtually all electronics circuits were made up from valves which were unreliable and cumbersome. As the transistor was considerably more reliable than valve technology, it also offered other key advantages of longer life time, less power consumption and smaller device dimensions. It was these key attributes that resulted in invention of the first integrated circuit by J. Kilby [6]. Within the next 10 years, the transistor had rendered valve technology all but obsolete.



Figure 1-2: First transistor from Bell laboratories (1947) [7]

At the same time that the transistor was invented, the theory behind HBT came to light. This technology described the effect of incorporating a wider band gap material for the emitter in the transistor, which became known as “the heterojunction concept” [8]. It was not until the 1970s, with the advent of modern epitaxial growth techniques, that the ability to grow complex, latticed matched layer structure, enabled the fabrication of HBT devices.

Initially, gallium arsenide (GaAs) / indium gallium arsenide (InGaAs) based devices were grown using liquid phase epitaxy (LPE) [9,10] due to the low density of interface recombination made it the ideal material for HBT. Since the introduction of LPE, the advent of molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD) resulted in the focus of research into this area to increase drastically [11], with MOCVD grown HBTs being reported in 1979 [12]. This work looked into finding the optimal alloys and materials, and to find out the properties of these materials such as the carrier motilities and high-field velocities [13].

1.2. Literature Review

Research of HBTs can be broken down and characterised into different family types of heterostructures which are used in their construction. These include gallium arsenide (GaAs), silicon (Si), gallium nitride (GaN), and indium phosphide (InP) based devices.

GaAs-based HBTs, such as aluminium gallium arsenide (AlGaAs)/GaAs and indium gallium arsenide (InGaAs)/GaAs devices were, as previously mentioned, the first heterostructure used in HBTs. The selection of these heterojunctions is down to the different layer structures having very similar lattice constants and thermal coefficients. GaAs based devices are used for high-power applications due to higher breakdown voltages [14].

Si-based HBTs (Si/SiGe) are not as competitive in comparison to other HBT heterojunction materials in the sense of achieving high speed or high power capability's. However, Si has some considerable advantages over the other families of HBTs being that it is well established, cheaper and has the ability to be integrate RF, analog and digital functions on a single substrate. Si HBTs still offer advantages over bipolar junction transistors (BJTs) equivalent devices such as higher frequency operation, better gain performance and higher power efficiency due to the advantages of HBTs (this will be discussed in the following chapter). SiGe based devices are typically used for low noise applications such as low noise amplifiers (LNAs) due to their enhanced noise behaviour [15].

GaN-based HBTs are strong devices that offer excellent performance in power electronics due to their ability to perform under high power, high temperature and high frequency conditions [16]. GaN devices however are more limited due to having relatively low current gain, low maximum current density and high offset voltage.

InP-based HBTs, such as InP/InGaAs have shown considerable performance at high speed [17]. This is largely due to the low-contact resistance of InGaAs, high mobility and lower surface recombination of the material. These advantages, combined with the low turn-on voltages of InP-based HBTs, allow the use of InP based devices for high-speed, low-powered applications. InP based technology, while still being relatively new compared to the established Si and GaAs based heterostructures tends to be more expensive.

With the aim of achieving high speed devices, particularly in InP based HBTs, both the unity current gain (F_T) and the unity power gain (F_{max}) are key RF characteristics of the device. Principally with F_T , the increasing of the bandwidth requires the vertical and lateral scaling of the device, which has led to the development of scaling laws [18-22], with scaling laws for InP based devices being indicated in table 1.1:

In scaling, the aim being to improve the target bandwidth and speed of a circuit that uses transistors, such as master-slave D flip-flop (MS-DFF) circuits or amplifiers circuit by a factor of

γ :1. So with the target aim to increase the speed, (whether it be F_T , F_{MAX} or the speed of a MS-DFF circuit) of a device by $\gamma = \sqrt{2}$. Then the need to reduce the physical parameters of the devices, such as the widths and thicknesses of the emitter, base and collectors regions but also the element characteristic resistivity of the regions.

Parameter	scaling law	Gen. 2 (512 nm)	Gen. 3 (256 nm)	Gen. 4 (128 nm)	Gen 5 (64 nm)
MS-DFF speed	γ^1	150 GHz	240 GHz	330 GHz	480 GHz
Amplifier center frequency	γ^1	245 GHz	430 GHz	660 GHz	1.0 THz
Emitter Width	$1/\gamma^2$	512 nm	256 nm	128 nm	64 nm
Resistivity	$1/\gamma^2$	16 $\Omega\text{-}\mu\text{m}^2$	8 $\Omega\text{-}\mu\text{m}^2$	4 $\Omega\text{-}\mu\text{m}^2$	2 $\Omega\text{-}\mu\text{m}^2$
Base Thickness	$1/\gamma^{1/2}$	300 Å	250 Å	212 Å	180 Å
Contact width	$1/\gamma^2$	300 nm	175 nm	120 nm	60 nm
Doping	γ^0	7 10^{19} /cm ²	7 10^{19} /cm ²	7 10^{19} /cm ²	7 10^{19} /cm ²
Sheet resistance	$\gamma^{1/2}$	500 Ω	600 Ω	708 Ω	830 Ω
Contact ρ	$1/\gamma^2$	20 $\Omega\text{-}\mu\text{m}^2$	10 $\Omega\text{-}\mu\text{m}^2$	5 $\Omega\text{-}\mu\text{m}^2$	2.5 $\Omega\text{-}\mu\text{m}^2$
Collector Width	$1/\gamma^2$	1.2 μm	0.60 μm	0.36 μm	0.18 μm
Thickness	$1/\gamma$	1500 Å	1060 Å	750 Å	530 Å
Current Density	γ^2	4.5 mA/ μm^2	9 mA/ μm^2	18 mA/ μm^2	36 mA/ μm^2
$A_{\text{collector}}/A_{\text{emitter}}$	γ^0	2.4	2.4	2.9	2.8
f_r	γ^1	370 GHz	520 GHz	730 GHz	1.0 THz
f_{max}	γ^1	490 GHz	850 GHz	1.30 THz	2.0 THz
$V_{BR,CEO}$		4.9 V	4.0 V	3.3 V	2.75 V
ΔT		39 K	50 K	61 K	72 K
I_E / L_E	γ^0	2.3 mA/ μm	2.3 mA/ μm	2.3 mA/ μm	2.3 mA/ μm
τ_f	$1/\gamma$	340 fs	240 fs	180 fs	130 fs
C_{cb}/I_c	$1/\gamma$	400 fs/V	280 fs/V	240 fs/V	170 fs/V
$C_{cb}(\Delta V_{\text{logic}}/I_c)$	$1/\gamma$	120 fs	85 fs	74 fs	52 fs
$R_{bb}/(\Delta V_{\text{logic}}/I_c)$	γ^0	0.76	0.47	0.34	0.26
$C_{je}(\Delta V_{\text{logic}}/I_c)$	$1/\gamma^{3/2}$	380 fs	180 fs	94 fs	50 fs
$R_{ex}/(\Delta V_{\text{logic}}/I_c)$	γ^0	0.24	0.24	0.24	0.24

Table 1-1: Scaling laws for InP-based HBTs [22].

There is the constant drive to increase the speed of devices, in the form of F_{MAX} and F_T , which is largely dependent on reducing parasitic elements device. For F_{MAX} , the reduction of the base resistance (R_{BB}) and the base-collector capacitance (C_{BC}); being that F_{MAX} is inversely proportional to these values (to be discussed in chapter two). Reducing R_{BB} and C_{BC} can be achieved by increased doping in the base and reducing the base-collector mesa structure. In conventional emitter-up structures, C_{BC} provides a considerable restriction on F_{max} . As illustrated in Fig 1.3, C_{BC} consists of both the intrinsic (C_{BCi}) and extrinsic (C_{BCx}) elements. As the extrinsic element provides no purpose in the operation of the device, then its removal would be beneficial in the increase of F_{max} .

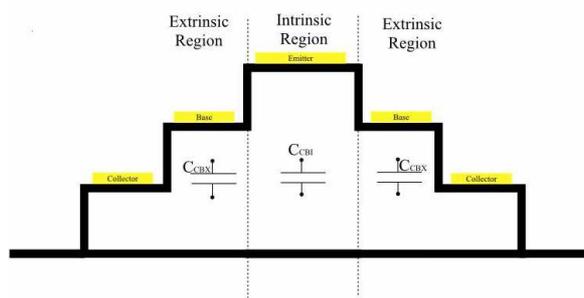


Figure 1-3: C_{BCI} and C_{BCX} elements of an HBT

Various techniques, as illustrated in Fig 1.4 that target the reduction, or even the removal of C_{BCX} have been investigated. This includes techniques such as emitter-up devices with re-grown emitter-base junctions [23], base with sidewall contacts [24], undercut technique [25] collector-up devices with implanted extrinsic emitter-base regions [26] and transferred substrate devices [27].

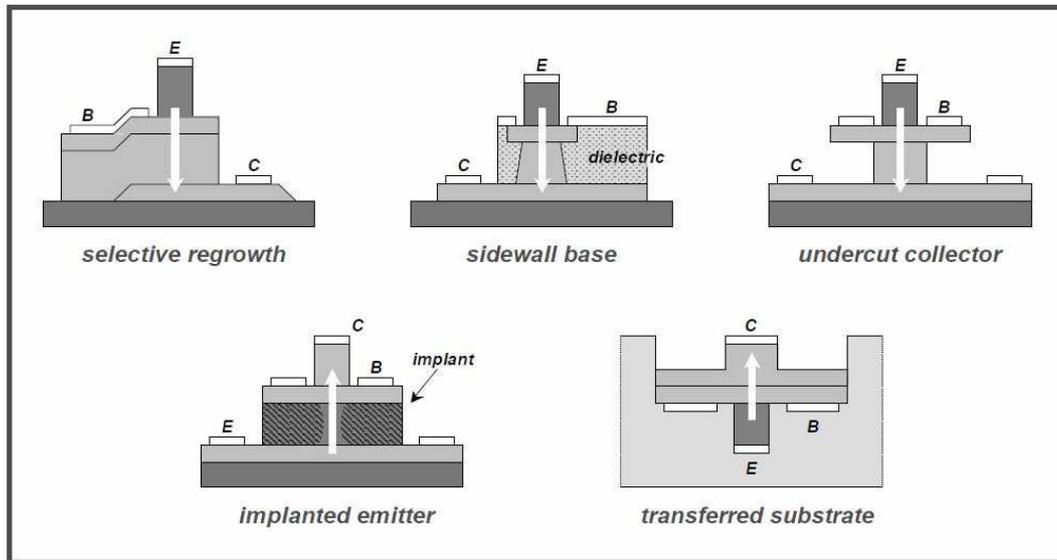


Figure 1-4: Various methods used to reduce the base-collector capacitance of a HBT. [28]

In the last few years, Indium Phosphide based HBTs have achieved high reported transistor bandwidths, with power gain cut-off frequencies (F_{MAX}) approaching and even exceeding 1 THz [17,29,30].

1.3. Aims and objectives

The primary objective of this work is the development of a reliable process for the fabrication InP/In_{0.53}Ga_{0.47}As based Single-HBT. The establishment of a reliable fabrication process of HBT devices is crucial in obtaining a high yield for working devices. During this process the evaluation and testing of the Ohmic contacts and etching techniques will investigated and evaluated.

Following the completion of the device fabrication, the next objective is the establishment and evaluation of an accurate small-signal model of a HBT. The accurate characterisation of HBTs is a crucial part in the process and development of devices, as it allows for improved device characterisation and evaluation.

1.4. Summary and layout of the Thesis

This thesis is broken down into 6 chapters and will be structured as follows:

Chapter 2 :

This outlines the detail relating to the theory of HBT device operation, including the heterostructure concept that makes HBT different from bipolar junction transistors (BJTs). Alongside this, the key characteristic attributes that define the performance of a device such as the DC and RF properties are described.

Chapter 3:

Presented in chapter three is the fabrication technique that is used in the project to develop and fabricate a HBT. In addition, the evaluation and testing of different Ohmic contacts and etching are undertaken along with the discussion about the different possible fabrication techniques available.

Chapter 4:

The RF and DC extracted results, such as F_{\max} , F_T and the current gain (β) of the devices are presented here.

Chapter 5:

This chapter explains the design and implementation of an accurate small signal equivalent circuit HBT model. In addition the background principle of small signal techniques and the evaluation of the equivalent circuit will be discussed.

Chapter 6:

The final chapter summarizes the results achieved within the thesis as a whole along with the outlook for potential future research that could follow on from this work.

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2. Heterojunction Bipolar Transistor Theory

The drive to achieve higher speeds in integrated circuit design has resulted in considerable work in transistor research to push the limit on the capabilities of these devices. This has helped HBTs to establish themselves in circuit design due to the advantages of incorporating a heterojunction in a bipolar junction transistor (BJT). Since the BJT (and as a consequence HBTs) is formed up of two p-n junctions that are connected back to back then the operation of these transistors devices depends on the effects and properties at the p- and n- type boundary.

2.1. Semiconductor Diode

A semiconductor diode is achieved by combining two adjacent regions of the same continues crystal lattice with different carriers, as depicted in fig 2-1. With sufficient doping of donor impurities to a region of semiconductor material results in extra electrons being available within the crystal structure and the region becomes termed as “n-type”. Within this region, electrons become the majority charge carriers. Whereas with sufficient doping of acceptor impurities would result in extra holes being available in the crystal lattice of the region and is termed to be “p-type. The impurity atoms added to the crystal lattice to form the p-type region accepts the electrons of the semiconductor material and adds a hole in the covalent bond. Within the p-type region, holes become the majority charge carriers.

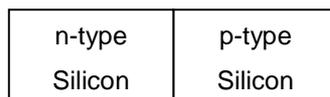


Figure 2-1: pn semiconductor diode

2.1.1. Unbiased

As soon as the pn junction is formed, as represented in Fig 2-2 (a), free electrons and holes close to the boundary diffuse across the junction from their respective regions and recombine with each other. This results in the n-type region near to the junction to becomes positively charged and the p-type region to become negatively charged (both having been previously neutral). This exchange of majority charge carriers between the two regions stops because the positive charge region in the n-type region opposes the flow of holes into the p-type material. As well as this, the negative charge region in the p-type region opposes the flow of electrons into the n-type material. This depletion region becomes free of majority charge carriers due to the recombination that has occurred, as illustrated in Fig 2-2 (b). This region is known as the depletion region. The newly

formed depletion region acts as if there was a built in junction voltage, acting from n- to p-type region.

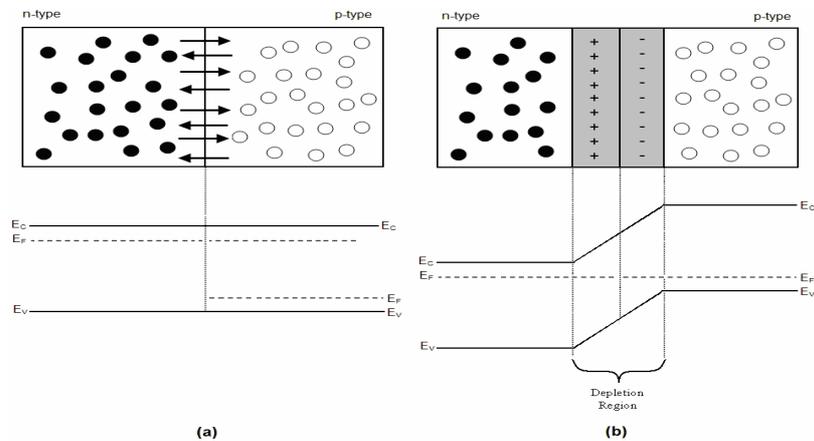


Figure 2-2: Formation of a pn diode

During this formation, in view of the need for the Fermi level of adjacent band gap to be aligned, this results in the valence and conduction bands shift to allow for this, as indicated in the band diagram in Fig 2-2 (b).

2.1.2. Forward Bias

Forward bias condition is obtained with the application of a positive voltage source to the p-type region a negative voltage being applied to the n-type region (as shown in Fig 2-3 (a)). This applied voltage results in the decrease in width of the depletion region and the junction voltage. When the applied voltage exceeds the junction voltage of the depletion region, electrons are then able to flow across the pn boundary towards the positive terminal of the battery. While the holes, which give the impression of flowing towers the negative terminal. Holes do not flow themselves, but the electrons that possessed by the holes gain sufficient kinetic energy to break the covalent bond and fill up the hole [1].

2.1.3. Reverse Bias

With the application of the power source in reverse bias mode by applying the positive terminal to the n-type material and negative terminal to the p-terminal (as depicted in fig 2-3 (b)), the excess electrons in the n-type region are attracted away from the depletion region, and towards the positive terminal of the external power source. This results in an increased build up of minority carriers at the pn boundary. Whereas in the p-type region, any electrons (minority carriers) are repelled and the holes appear to be attracted to the negative terminal of the power source. This

results in the increased width of the depletion region. Only a few minority carriers cross the junction and a small current, known as a “leakage voltage” flows.

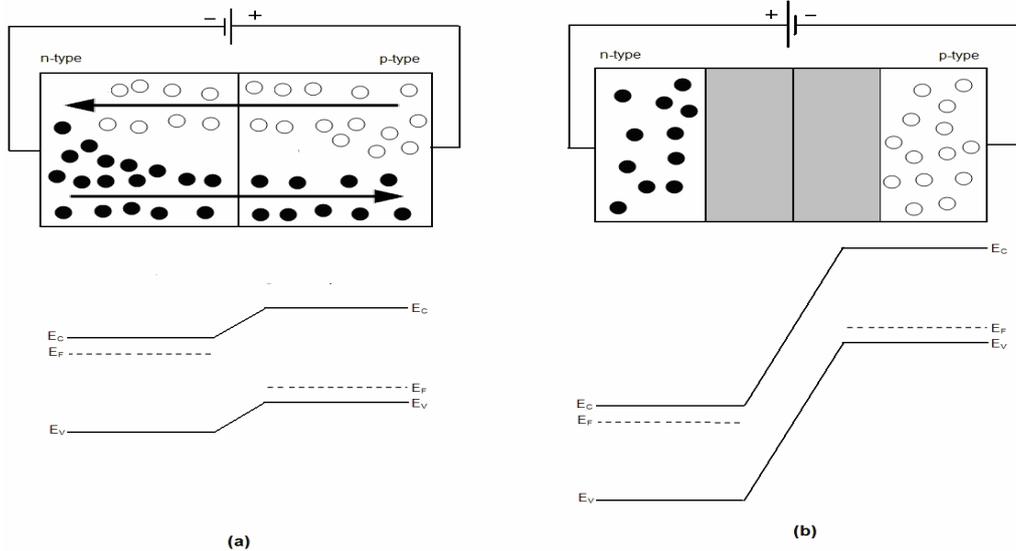


Figure 2-3: Band gap of a pn junction under (a) forward bias and (b) reverse bias.

2.1.4. Diode I-V Characteristic

The typical IV characteristic graph for a pn junction is shown Fig 2-4. The two key values for a pn junction are the threshold voltage (V_T) and the breakdown voltage (V_{BV}). The threshold voltage occurs due to the fact that even though the device is under forward bias, a small voltage is initially required to overcome the depletion region to allow the flow of current between the two terminals of the device.

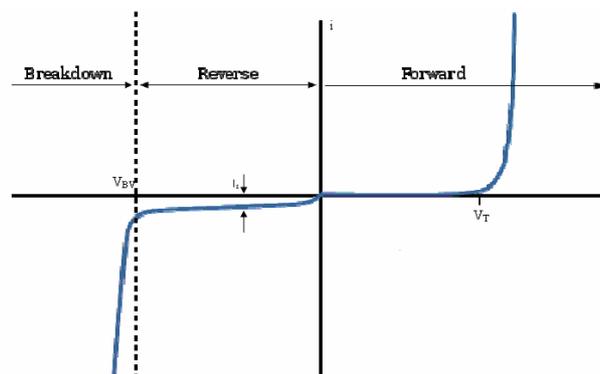


Figure 2-4: IV characteristic graph of diode

If the diode is reverse biased, the breakdown voltage occurs when the material stops operating as a diode, i.e. it stops blocking current flow between the contacts but instead allows large current

flow (avalanche breakdown). The relationship between the applied voltage V , and the current I is exponential and is expressed as [2]:

$$I = I_s \left(e^{\frac{qV}{kT}} - 1 \right) \quad (1)$$

where:

- I = The forward bias current
- I_s = The leakage current
- q = The charge of an electron
- V = The forward bias voltage
- k = is Boltzmann's constant
- T = Temperature

2.2. BJT and HBT Layer Structure

HBTs, like BJTs, are made up of three main regions, as indicated in Fig 2-5, being the collector (C), base (B) and emitter (E). These layers form two pn junctions connected in a back to back configuration. Typically it is the form of an npn transistor where the base is p-type and the emitter and collector are n-type. The device can be in the form of a pnp transistor. As the electron mobility is typically higher than the hole mobility for all semiconductor materials, a given npn structure tends to be faster, thus they are generally preferred for circuit applications.

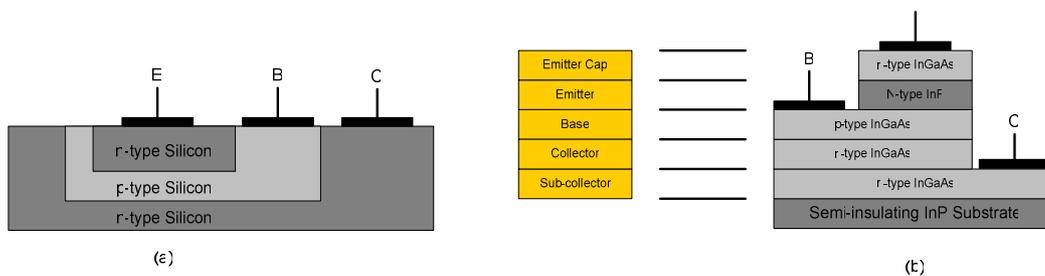


Figure 2-5: Typical layer structure of (a) silicon BJT and (b) InP/InGaAs HBT Transistor

The principle difference between a BJT and HBT is the introduction of a heterojunction at the emitter-base interface in a HBT device. As depicted in Fig 2-5 with an npn BJT being formed out of silicon and the emitter and collector regions of which being implanted with donors. For an InP-based HBT, narrower bandgap InGaAs (an alloy lattice-matched to InP) is used for the collector and the base, with the emitter being made out of a wider bandgap material in the form of InP.

The incorporation of a wide band-band gap material for the emitter region, and the resulting heterojunction means that at the boundary between the emitter and base result in a spike in the conductance band due to the discontinuity of the band gap. This spike in turn reduces the back injection of electrons into the base is reduced considerably compared to the BJT equivalent device. This results in, not only an improved efficiency of the HBT in comparison to BJT, but an improvement in the DC current gain (β) of the device. As well as this, the incorporation of a wider bandgap material in the emitter means that there is less of a requirement for higher doping concentration within the region to limit the back injection, but allows for design in the doping levels with the intention to minimise parasitic elements of the device, which, as will get discussed later in this chapter, results in the improved device speeds. Table 2.1 below shows some typical HBT layer structures.

Substrate	Emitter	Base	Collector	Type
GaAs	AlGaAs	GaAs	GaAs	SHBT
			AlGaAs	DHBT
	InGaP	GaAs	GaAs	SHBT
			InGaP	DHBT
InP	InP	InGaAs	InGaAs	SHBT
			InP	DHBT
	InAlAs	InGaAs	InGaAs	SHBT
			InP	DHBT
	InP	GaAsb	InP	DHBT

Table 2-1: Types with different material systems [3]

GaAs is the most mature of the substrates materials used as well as being the cheaper option when compared to InP based structures. Although InP has some attractive advantages in comparison, the main one being that its energy band gap corresponds with that used with optical communication, or more accurately with lasers working at 1.36 and 1.55 μ m wavelengths, this makes them an ideal choice for optical communication circuits [42]. In addition, InP is lattice matched with InGaAs, which has a higher electron mobility than GaAs.

2.3. Heterostructure Concepts

This heterostructure concept, mentioned above, expands upon the theory and concept of a pn junction. Unlike a homojunction pn junction where the material is made out of the same material and each adjacent region being doped to form a PN junction, a heterojunction, while still doping both the p and n region of the junction, incorporates two different semiconductor materials to form a PN junction.

2.3.1. Band Discontinuities

With the introduction of a heterojunction between the emitter and base, we find the electron affinities of these materials, χ^E and χ^B respectively are different, which results in a discontinuity in the conduction band, which can be expressed as:

$$\Delta E_C = \chi^B - \chi^E \quad (2)$$

A discontinuity in the valence band (ΔE_V) is also introduced due to the band gap energies being different in the two regions. The total band gap discontinuity difference, ΔE_G , of the emitter and base, E_{gE} and E_{gB} respectively, is the combined discontinuities in both the valence and conduction bands:

$$\Delta E_G = \Delta E_C + \Delta E_V \quad (3)$$

The difference in the band gap, ΔE_G , between the two materials is resolved at the junction by the introduction of discontinuities in both the valence and conduction bands. As shown in Fig 2-6, HBTs with abrupt emitter-base junction leads to a spike, ΔE_C , in the conduction band, and a step ΔE_V , in the valence band.

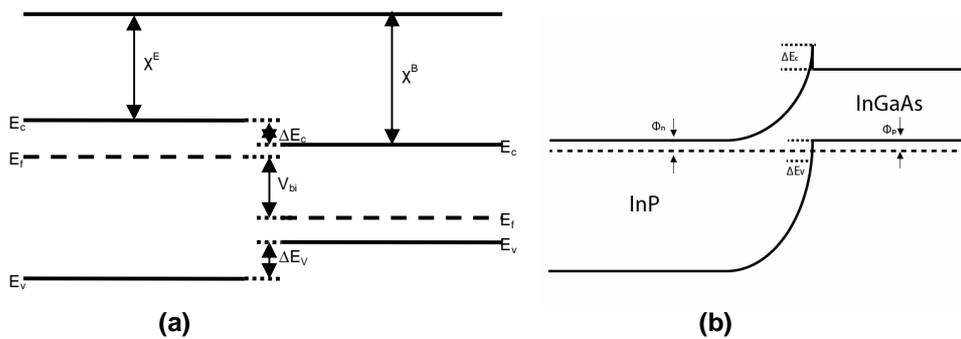


Figure 2-6: Energy band gap diagram of a N-type wide gap emitter and P-type base at equilibrium both (a) before and (b) after formation.

The key advantage of this incorporation of a heterojunction bipolar transistor does mean the back injection of electrons into the base is reduced considerably compared to the homojunction deployed in a BJT. However the introduction of this band spike in the conduction band, ΔE_C , does mean that the forward flow of electrons from the wide band-gap emitter into the base is restricted due to the need to burrow (tunnel) through the spike (barrier).

In the valence band a combination of a large ΔE_v as well as the incorporation of a wider band-gap material in the emitter restricts the minority-carrier back flow from the emitter into the base. The reduction in both the back injections of the holes and electrons, is expressed as $H_{BI} = e^{-\frac{\Delta E_g}{kT}}$ and $E_{BI} = -e^{-\frac{\Delta E_c}{kT}}$ respectively [5]. Considering the difference between ΔE_c is less than ΔE_g , while under forward bias the reduction of hole back injection H_{BI} is reduced by a greater amount than that of electron back injection (E_{BI}). This results in several advantages in the incorporation of a heterojunction in a HBT device that include:

- The reduction the minority carrier charge stored in the emitter under forward bias, which accounts for the reduction in emitter-base capacitance (C_{BE}). As a result this improves the high-speed and high frequency of the device.
- An improvement in the electron injection efficiency which impacts directly and favourably on the DC gain (β) of the device.

If the reduction in hole flow is large enough, then the emitter doping density, N_E , can be decreased, and the base doping density, N_B , can be increased while still maintaining a high β . The advantages include:

- A further reduction in C_{BE} (due to the reduced in N_E)
- A reduction in base resistance, R_{BB} , which in-turn improves:
- Maximum oscillation frequency of the device (F_{MAX})
- Noise performance by reducing thermal noise in the base

With the goal to meet a required R_{BB} value, a narrower base can be achieved; this results in a shorter base transit-time (τ_b) which improves the current gain cut-of frequency (F_T).

2.3.2. Built-In Potential

For a heterostructure PN structure, the built-in potential, (V_{bi}), as indicated in Fig 2.6 (a), can be expressed as:

$$E_{gE} - V_N = \Delta E_v + V_p + V_{bi} \quad (4)$$

where:

E_{gE} = Emitter band gap in eV

V_N = Potential difference between the conduction band and Fermi level in the emitter

V_p = Potential difference between the Fermi level and the valence band in the base

If we then express V_N and V_P in terms of the emitter and base doping levels, N_{DE} and N_{AB} respectively, and the respective density of states in Emitter conduction band and base valence band, N_{CE} and N_{VB} , the following is obtained:

$$V_N = (E_{CE} - E_{FE}) = -(kT/q) \ln(N_{DE}/N_{CE}) \quad (5)$$

and,

$$V_P = (E_{FB} - E_{VB}) = -(kT/q) \ln(N_{AB}/N_{VB}) \quad (6)$$

By combining equations (2) through (5):

$$V_{bi} = E_{gE} + (kT/q) \ln(N_{DE}/N_{CE}) + (kT/q) \ln(N_{AB}/N_{VB}) + \Delta E_C - \Delta E_G \quad (7)$$

Although, since ΔE_g is defined as:

$$\Delta E_G = E_{gE} - E_{gB} \quad (8)$$

Equation (6) can now be updated to the following:

$$V_{bi} = E_{gB} + \Delta E_C + (kT/q) \ln\left(\frac{N_{DE} \cdot N_{AB}}{N_{CE} \cdot N_{VB}}\right) \quad (9)$$

2.3.3. Emitter-Base Interface

With the introduction of a wide-bandgap material in the emitter to form a HBT, this allows a wider variety of options and flexibility in the design process depending on the exact design requirements. Typical design parameters which, when taken into account when deciding on the emitter material includes:

- Low-turn voltage (V_T), which is a key requirement for low power consumption circuit.
- Increased electron flow across the junction, allows in more electrons to flow into the collector. As a result, improves the dc gain (β) of the device.

The key properties that affect these design parameters of the different materials in Table 2-1 are listed below in Table 2-2.

Heterojunction Material	E_G , Emitter (eV)	E_G , Base (eV)	ΔE_C (eV)	ΔE_V (eV)
InP/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	1.35	0.76	0.25	0.34
$\text{In}_{0.52}\text{Al}_{0.48}\text{As} / \text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	1.48	0.76	0.48	0.24
$\text{Al}_{0.30}\text{Ga}_{0.70}\text{As}/\text{GaAs}$	1.86	1.42	0.28	0.15
$\text{In}_{0.49}\text{Ga}_{0.51}\text{P}/\text{GaAs}$	1.92	1.42	0.12	0.38

Table 2-2: Band Gap details of emitter-base materials [3]

Fig 2.7a illustrates a typical E-B wide bandgap emitter heterojunction which results in a discontinuity in both the conduction and valence bands, ΔE_c and ΔE_v . Provided that the emitter is made up of a wide bandgap alloy, then the composition can be graded over a short distance at the junction to allow the removal of the discontinuity. An example would be the emitter was made up of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and the fraction x being varied from 0.3 to 0 over a short distance to a GaAs base. By incorporating a graded junction at the emitter-base junction (as depicted in fig 2-7b) allows for improved V_T performance and increased electron flows as previously mentioned. Although a downside of reducing ΔE_c is that the back injection of electrons enter the emitter from the base is increased due to the low barrier.

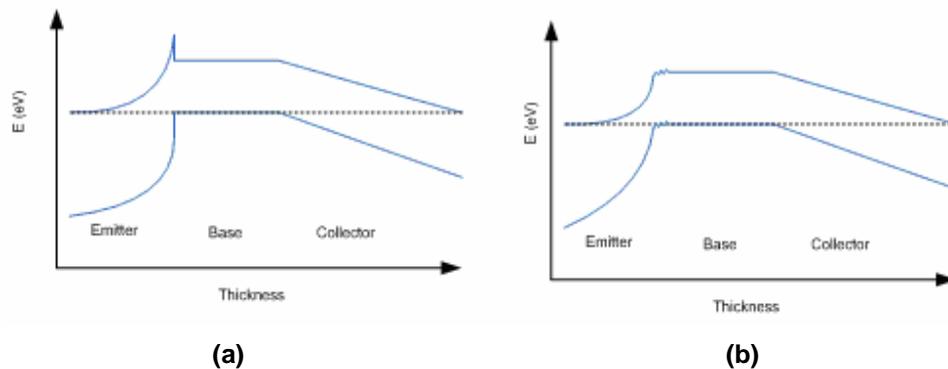


Figure 2-7: Band diagram of a NPN HBT with (a) abrupt junction and (b) graded junction at the emitter-base junction.

2.3.4. Base-Collector Interface

Typically HBTs come in the form of Single-HBT (SHBT) where there is only a single heterojunction between the emitter and base region. However it is not uncommon to incorporate a heterojunction between the base and collector to form a Double-HBT (DHBT). The band diagram of both a SHBT and DHBT being depicted in Fig 2-8. There are several considerations in the design of the collector region mesa structure and the final design of this is dependent on the application of the device. An example of this is illustrated by the thicker the collector region the higher the breakdown voltage [4], with the incorporation of a wider bandgap material in the collector increases the breakdown voltage of the device, this is particularly useful for high power devices. In contrast, a thinner collector results in a higher F_T but an increase C_{BC} .

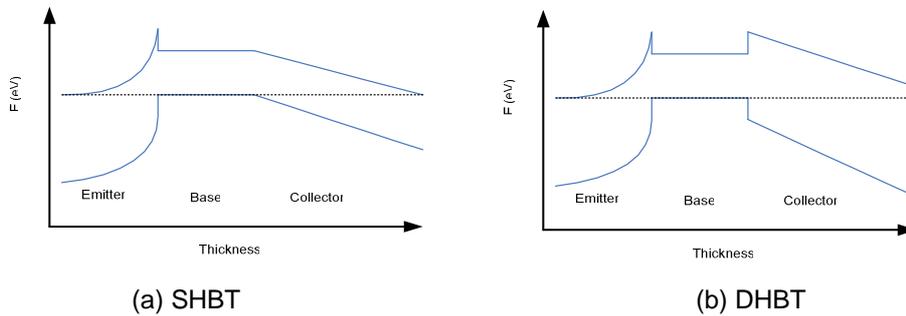


Figure 2-8: NPN Band diagrams illustrating the difference between a SHBT and DHBT

Although, the ΔE_c brought in by incorporating a heterojunction between the base and collector will decrease the electron flow into the collector, which will drastically reduce device performance [5], particularly β . The removal of the discontinuity between the two regions can be overcome by incorporating grading into the base-collector interface as depicted in Fig 2-9. This is achieved by incorporating a number of intermediate epitaxial layers between the two regions.

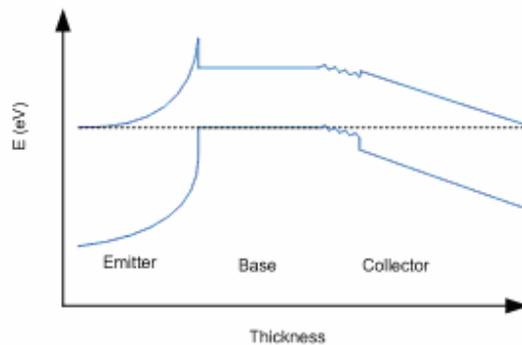


Figure 2-9: Band diagram of the base – collector grading for a NPN DHBT.

2.4. DC Characteristics

For DC characterisation, Fig 2.10 shows the standard output characteristics, where, at a given V_{CE} , varying I_B has a similar effect on the collector current output (I_c). Except with a gain of β , which is dependant upon the physical properties of the device.

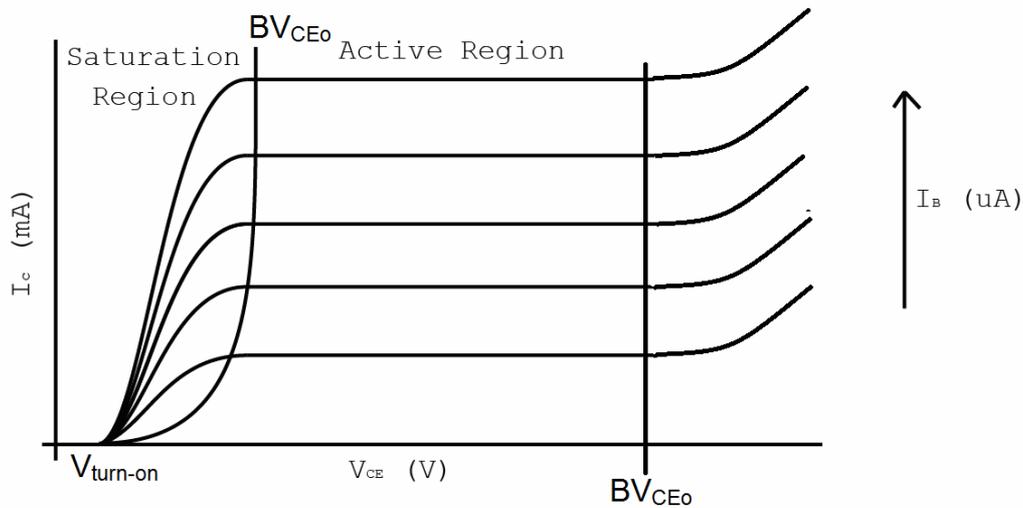


Figure 2-10: Common DC output emitter characteristics

With two pn junction diodes being connected back to back to each other 3 distinctive regions are obtained which, as illustrated in figure 2-10; include the saturation region, active region and finally the cut-off region. The basic diode operation for the transistor is described below:

To begin with in the saturation region:

- The base-emitter diode is forward biased $V_{BE} > 0V$ and
- The base-collector diode is forward biased $V_{BC} > 0V$

Under normal operating conditions (active region):

- The base-emitter diode is Forward Biased $V_{BE} > 0V$ and
- The base-collector diode is Reversed Biased $V_{BC} < 0V$

In the cut-off region:

- The base-emitter diode is reversed biased $V_{BE} < 0V$ and
- The base-collector diode is reversed biased $V_{BC} < 0V$

2.4.1. DC current gain

In the common emitter output characteristics shown above in figure 2.10 if the output collector current (I_C) is divided by the input base current (I_B) at a certain bias point the DC current gain can be calculated for a given bias point. The equation of this DC current gain (β) is [8]:

$$\beta = \frac{I_C}{I_B} = \frac{N_E T_E D_{nB}}{N_B T_B D_{pE}} \cdot \exp\left(\frac{\Delta E_V}{kT}\right) \quad (10)$$

where:

N_E = Emitter doping

N_B = Base doping

T_E = Emitter thickness

T_B = Base thickness

D_{pE} = Minority hole diffusions coefficient in emitter

D_{nB} = Minority electron diffusion in the base

ΔE_v = Valence band discontinuity at the base-emitter hetero-interface

Due to the valence band discontinuity brought on by the heterojunction at the emitter-base connection results in the reduction of the hole transfer from the base to the emitter, thus keeping the base current lower and leading to a higher DC gain.

2.5. RF Characterisation

For RF characterisation of a HBT there are two key figures of merit that are used, the current gain cut-off frequency (F_T) and the maximum oscillation frequency (F_{max}).

2.5.1. The Current Gain Cut-off Frequency (F_T)

The current gain cut-off frequency (F_T) is the frequency at which point the magnitude of the AC current gain has been decreased down to 1. This cut-off frequency is determined mostly by the physical vertical structure of the device [8]. The cut-off frequency can be calculated by using equation (10) below:

$$F_T = \frac{1}{2\pi\tau_{total}} \quad (11)$$

where:

$$\tau_{total} = \tau_e + \tau_b + \tau_{sc} + \tau_c \quad (12)$$

this equation can be further broken down with the following equations:

$$\tau_e = \frac{kT}{qI_c} (C_{BE} + C_{BCI}) \quad (13)$$

where τ_e is known as the emitter charging time, C_{BCI} is defined as the intrinsic base–collector junction capacitance and C_{BE} is known as defined as the base–emitter junction capacitance.

$$\tau_b = \frac{T_B^2}{2D_{nB}} \quad (14)$$

τ_b is the base transit time and D_{nB} being the minority electron diffusion in the base

$$\tau_{sc} = \frac{T_{dep}}{2V_{sat}} \quad (15)$$

τ_{sc} = space-charge transit time which is the time for the carriers to cross through the depletion region of the base-collector junction.

$$\tau_c = (R_e + R_c) \cdot C_{BCI} \quad (16)$$

τ_c = the collector charging time. When substituting equations 12 to 16 back into equation 11 this results F_T to be rewritten as:

$$\frac{1}{2\pi F_T} = \frac{kT}{qI_c} (C_{BE} + C_{BCI}) + \frac{T_B^2}{2D_{nB}} + \frac{T_{dep}}{2V_{sat}} + (R_e + R_c) C_{BCI} \quad (17)$$

From which, the cut-off frequency is written by:

$$F_T = \frac{1}{2\pi \left(\frac{kT}{qI_c} (C_{BE} + C_{BCI}) + \frac{T_B^2}{2D_{nB}} + \frac{T_{dep}}{2V_{sat}} + (R_e + R_c) C_{BCI} \right)} \quad (18)$$

From equation (17), it is clear that the intrinsic base–collector junction capacitance (C_{BCI}) has a large effect on F_T and there is currently a lot of work being undertaken into minimizing this [8-9].

2.5.2. Maximum oscillation Frequency (F_{max})

The maximum oscillation frequency is defined as the frequency at which the maximum available power gain deliverable by the transistor equals unity. This can be expressed as [9]:

$$F_{MAX} \approx \sqrt{\frac{F_T}{8\pi R_{BB} C_{BC}}} \quad (19)$$

where R_{BB} is the total base resistance and C_{BC} is the combined total base-collector capacitance of both the intrinsic (C_{BCI}) and extrinsic (C_{BCX}) values:

$$R_{BB} = R_{b,cont} + R_{b,gap} + R_{b,spread} \quad (20)$$

$$C_{BC} = C_{BCI} + C_{BCX} \quad (21)$$

where:

$R_{b,cont}$ = Base contact resistance

$R_{b,gap}$ = Base-emitter gap resistance

$R_{b,spread}$ = Base spreading resistance

The parameters are illustrated in Fig 2.11 as a visual representation of the parameters as part of the triple mesa structure of a HBT.

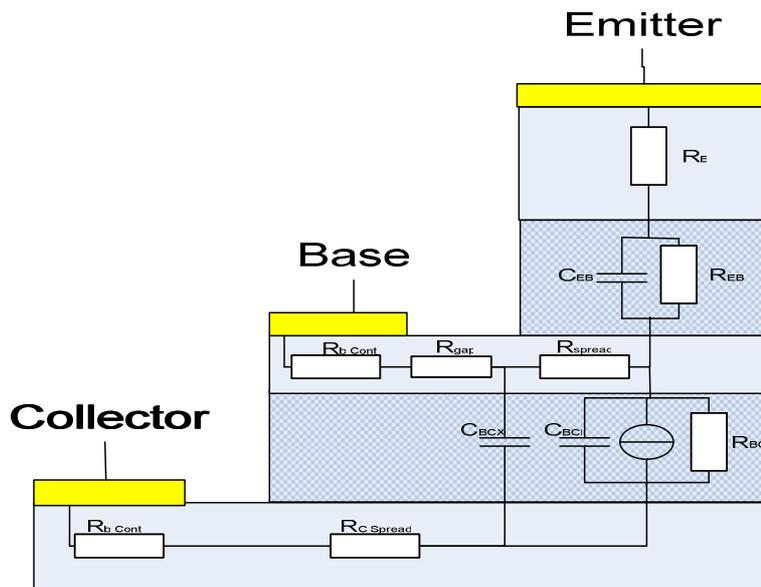


Figure 2-11: Triple mesa HBT structure with small-signal model used in the equations.

2.6. References

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3. HBT Fabrication

In this chapter, the techniques used in the fabrication of HBTs are discussed along with comparisons of the different processing techniques available. The processing of HBTs presented here is performed in a clean room environment, the University of Glasgow's James Watt Nanofabrication Centre (JWNC).

3.1. *Processing Steps*

The fabrication of HBTs used in this work, being of a triple mesa design structure, requires 8 separate processing steps. These consist of 3 etching steps, 4 metallization steps and a device isolation step, all of which are discussed here.

3.1.1. Lithography

Lithography is a crucial part of the fabrication process, as even though it is not a step in itself, it is used in every step. It can be defined as the process used to define the required pattern layout design from the mask plate onto the resist layer on the wafer surface. There are two forms of photolithography; electron-beam lithography (e-beam lithography) and photolithography.

Photolithography uses ultraviolet (UV) to transfer the layer on the mask to be imprinted onto the photo-resist, whereas e-beam lithography, which as the name suggests, involves exposing the resist to the electron beam via a mask plate which transfers the layer design onto the wafer. In comparison to photolithography, e-beam is capable of defining structures in the nanometre scale with good tolerances, although does require considerably more time to write the patterns. For our process, photolithography using a SÜSS MA6 mask aligner is used which provides a high precision alignment accuracy of as low as $\pm 0.5\mu\text{m}$.

The initial step with photolithography is the application of photo-resist onto the wafer which is used to define the mask layer in. There are several considerations to be aware of with the use of photo-resist. These include the required thickness, which is dependant of the speed and duration of the application of the photo-resist, and the choice of using either negative or positive resist depending on the application of the process. The difference between the two types is that with the exposure of positive photo-resist to UV light, results in the weakening of the chemical structure and becomes soluble in the developer solution. Whereas with negative photo resist, the exposure of these resist to UV light strengthens the bonds and becomes insoluble in the developer solution. The illustration of the outcome of using different outcome of using positive or negative resist is shown in Fig 3-1. There are a number of different resists and techniques used within the JWNC, although the process used within this project is the use of S1818 photo-resist.

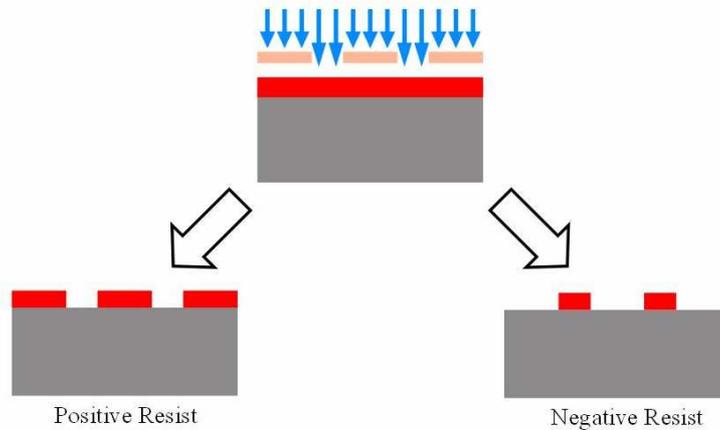


Figure 3-1: Comparison between positive and negative resist

The masks used in the creation of the HBT structures were themselves made using the electron beam technology. The mask itself is of glass material that has been coated with chrome on one surface. Resist is covered on top of the chrome, exposed with e-beam lithography and the exposed chrome is etched away using wet etch technique. The mask used in this project consists of eight 10mm² layers, one for each of the 8 steps involved in this work, as described later in this chapter in section 3.2.

3.1.2. Ashering

After the development of the resist once it has been exposed on the MA6, a sub-step of placing the sample into an oxygen plasma chamber may be required. This would be used to remove any remaining unwanted resist that might have been left after development. It is required to make sure there is no resist remaining because if this were the case, it would prevent a successful etch or the application of good Ohmic contacts. This ashing is processed at 80W for 4 minutes during this fabrication process.

3.1.3. Etching

Etching is defined as the removal of a required material on the wafer to a required depth. This can be achieved by using either wet etching or dry etching. Wet etching uses chemicals that interact with the material to etch to the required depth. Dry etching typically uses the bombardment of ions to etch away the material. There are a number of different requirements of etching, depending on the application and layer structure of the devices being developed. These requirements include: etch rate, uniformity, selectivity, and anisotropy:

Uniformity is the deviation of the etch rate across the whole wafer. Having a high uniformity is required with the aim to have consistently reliable devices that all contain similar properties.

Having a high selectivity means that if one etches down through one layer structure then when a different material is reached, it stops. Isotropic etching occurrence is only a problem in wet etching, as dry etch has a virtually perfect anisotropic etching effect on the sample.

An/Isotropy is the etch rate difference between vertical and horizontal etching for different crystallographic directions. Isotropic etching is where the etching in both the horizontal and vertical direction are the same, as illustrated in Fig 3-2 (c). Anisotropic Etching rate is where the etch rates are different in the horizontal and vertical direction, Fig 3-2 (b), and lateral etch.

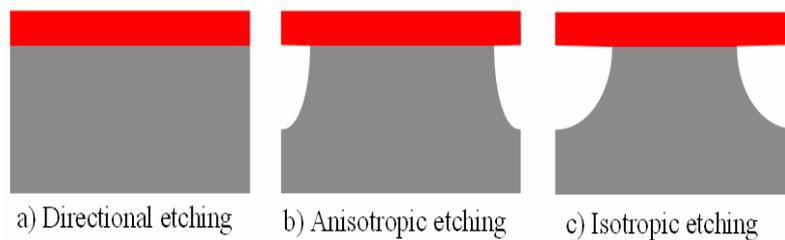


Figure 3-2: Etching comparison

The degree of isotropy, A , is depicted as:

$$A = \frac{R_L}{R_v} \quad (22)$$

where:

R_L is the lateral etch rate

R_v is the vertical etch rate

Therefore when $A = 0$, then the etch characteristic is known as directional etching, as depicted in Fig 3-2 (a), and reversely, when $A = 1$ then the etch is known as Isotropic. Any variation in between these extreme is referred to as having an anisotropic etch characteristic.

In comparison wet etching offers high etching rate and greater etch selectivity to that of dry etching, although in contrast, dry etching has the advantage of being capable of defining small feature sizes.

3.1.4. Forming of Contacts

The forming of metal contacts onto a semiconductor layer allows for the direct accessing of the device in question, whether this is for testing of the device characteristics or for connection to

other devices in a circuit. These contacts, in an ideal world would not add any resistance to the flow of current, however, in reality this is not the case and a small resistance is added. The base contact is important in the development for high speed HBT devices. The introduction of this junction creates a contact resistance which will cause the voltage to drop and with this will affect the key merits of the device, F_T and F_{MAX} , as discussed in the previous chapter. There are two types of contacts that can be applied, namely Ohmic and Schottky. Ohmic contacts provide symmetric and linear current-voltage (IV) curve (as shown in Fig 3-3 a), while a Schottky contact provides asymmetric and non-linear behaviour (as shown in Fig 3-3 b)

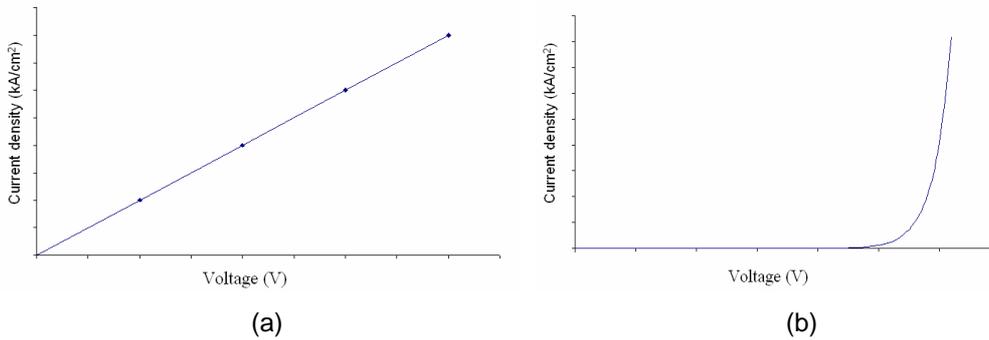


Figure 3-3: Comparison between (a) Ohmic and (b) Schottky contact.

In a semiconductor contact, depending on the requirements of the semiconductor material, it will be implanted with either acceptors or donors. This results in them having different Fermi levels (Fig 3-4 (a) and Fig 3-5 (b)). On joining the semiconductor material to the metal contact the free electrons and holes diffuse across the junction so that the Fermi levels align [Fig 3-4 (b) and Fig 3-5 (b)].

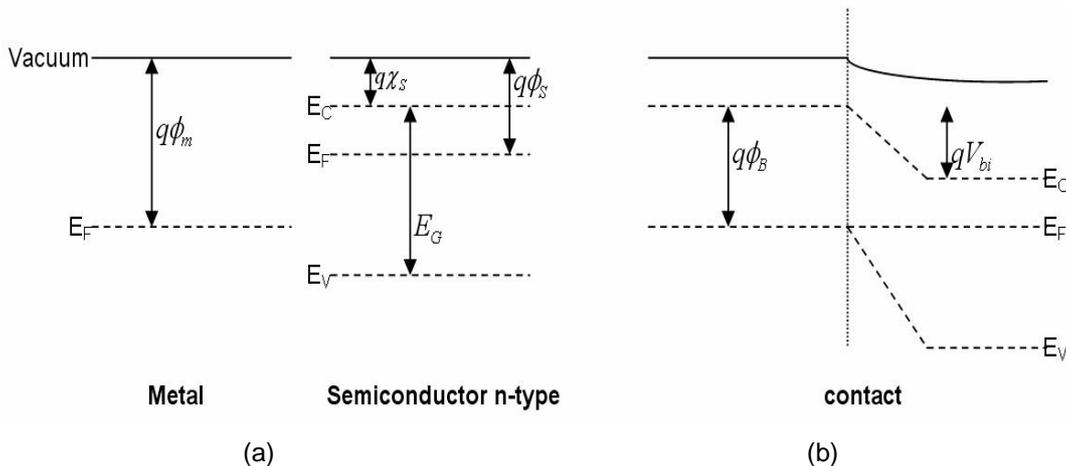


Figure 3-4: Band diagram for a metal/n-semiconductor junction.

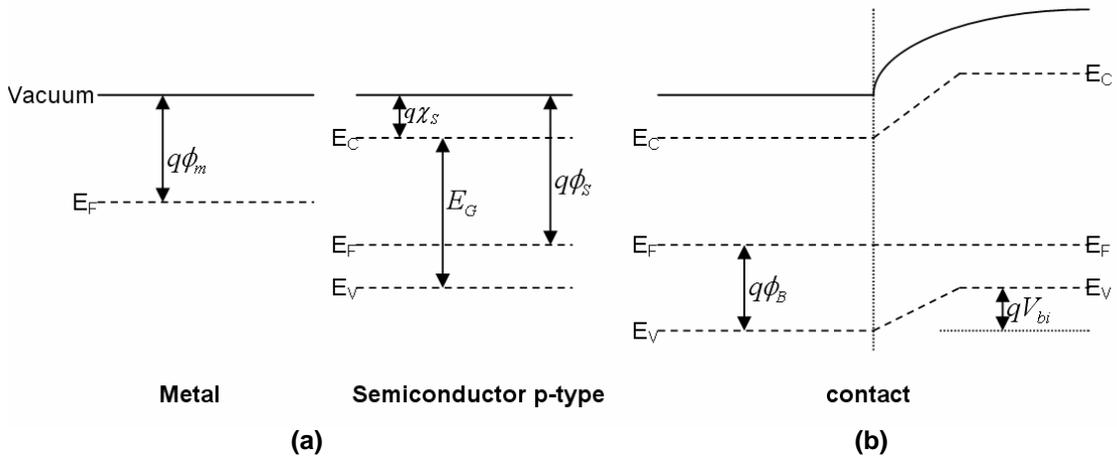


Figure 3-5: Band diagram for a metal/p-semiconductor junction.

There are two methods by which carriers flow across the metal/semiconductor interface. “Thermionic emission” occurs if the doping level in the semiconductor material is low. In this scenario the carriers flow over the barrier by thermal energy. In contrast for highly-doped semiconductor material, the depletion region becomes narrower. This narrow region can be penetrated by the carriers by quantum effect, or more commonly known as “tunnelling”. For Ohmic contacts, tunnelling is preferred as it allows for greater linearity and as a result, high doping is employed. The depletion width (W_{dep}) within the metal/semiconductor interface can be derived by solving the Poisson’s equation:

$$\nabla^2 V = \frac{\rho}{\epsilon} \quad (23)$$

where:

ρ is the net charge density

ϵ is the dielectric constant

After evaluating this, we are able to define the depletion region as [1]:

$$W_{dep} = \sqrt{\frac{2\epsilon V_{bi}}{\rho}} = \sqrt{\frac{2\epsilon V_{bi}}{q \cdot N_{dopant}}} \quad (24)$$

where:

q = Electric charge

V_{bi} = Built in Potential

N_{dopant} = Dopant levels

As indicated in equation (24) the depletion thickness is inversely proportional to the doping of the semiconductor material, so for Ohmic contacts, tunnelling is preferred as it allows for greater

linearity. As a result of these properties high doping is employed in this project. For semiconductors that are highly doped, the barrier heights can be defined as [1]:

$$q\phi_{Bn} = q\phi_m - qX_s \quad (25)$$

$$q\phi_{Bp} = E_g - q(\phi_m - X_s) \quad (26)$$

where:

Φ_{Bn} = Barrier heights of n-type material

Φ_m = Work function of the metal

X_s = Electron affinity of the semiconductor

Φ_{Bp} = Barrier heights of p-type material

E_g = Band gap (in eV)

3.1.5. Device Planarization

Due to the need of applying Ohmic contacts that are designed to enable the direct access of the device, the active/actual transistor is required to be isolated from these contacts. This is to prevent the bond pads from touching active multiple device regions (Emitter, base and collector). Polyimide PI-2545 is used to enable thick application onto the substrate to cover the vertical mesa structure of the device and the etching of the polyimide enables vias to be applied to directly access the emitter, base and collector regions of the device, as depicted in Fig 3.6. At which point the Ohmic contacts used for device testing can be applied the characteristics of the HBT can be successfully extracted, as shown later in this chapter. Individual devices are isolated from each other by etching the epitaxial layers around the transistors down to the semi-insulating InP substrate.

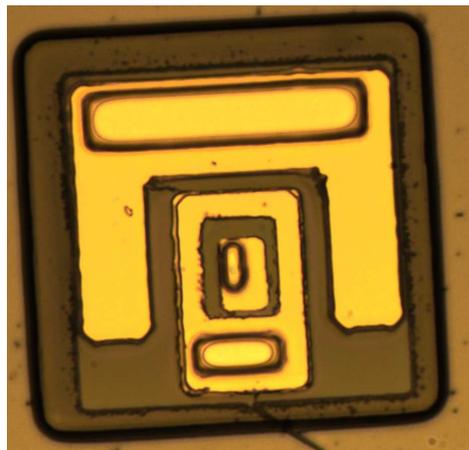


Figure 3-6: Successful application and development of polyimide

3.1.6. Details of a typical processing step

There are two key processing steps used within the development and fabrication of devices. This includes in the depositing of metal contacts, known as a metallization step and etch step. The initial steps, steps a-c in fig 3-7 for both processes are the same. Initially, the sample wafer is cleaned in Acetone, followed by Methanol and IPA for 5minutes in each while in an ultrasonic bath. This removes any loose organic or resist on the wafer. Once this has been completed, S1818 is spun onto the wafer (step a) and baked. The sample is then exposed with UV light and the mask layer is imprinted into the resist, which is then developed to expose the mask design. It is at this step where the processing steps between metallisation and etch processes divide with the deposition on metal or the etching of the wafer structure. Once this has been completed, the sample is placed into acetone for an hour in a warm bath (50°C) to remove the resist.

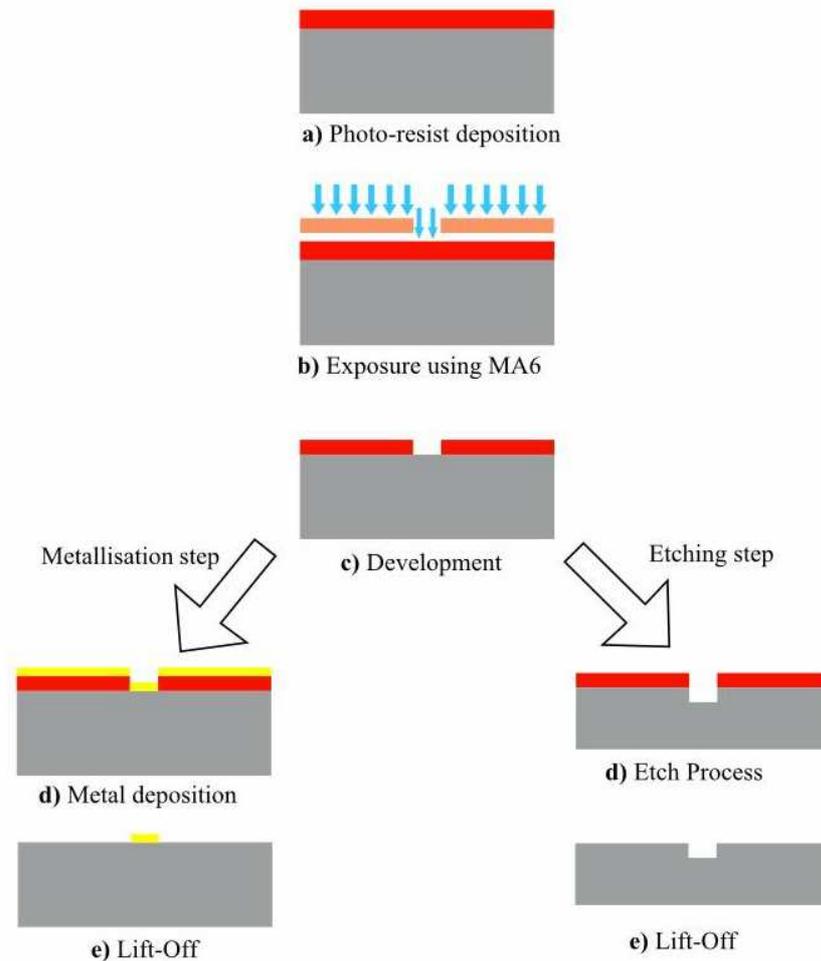
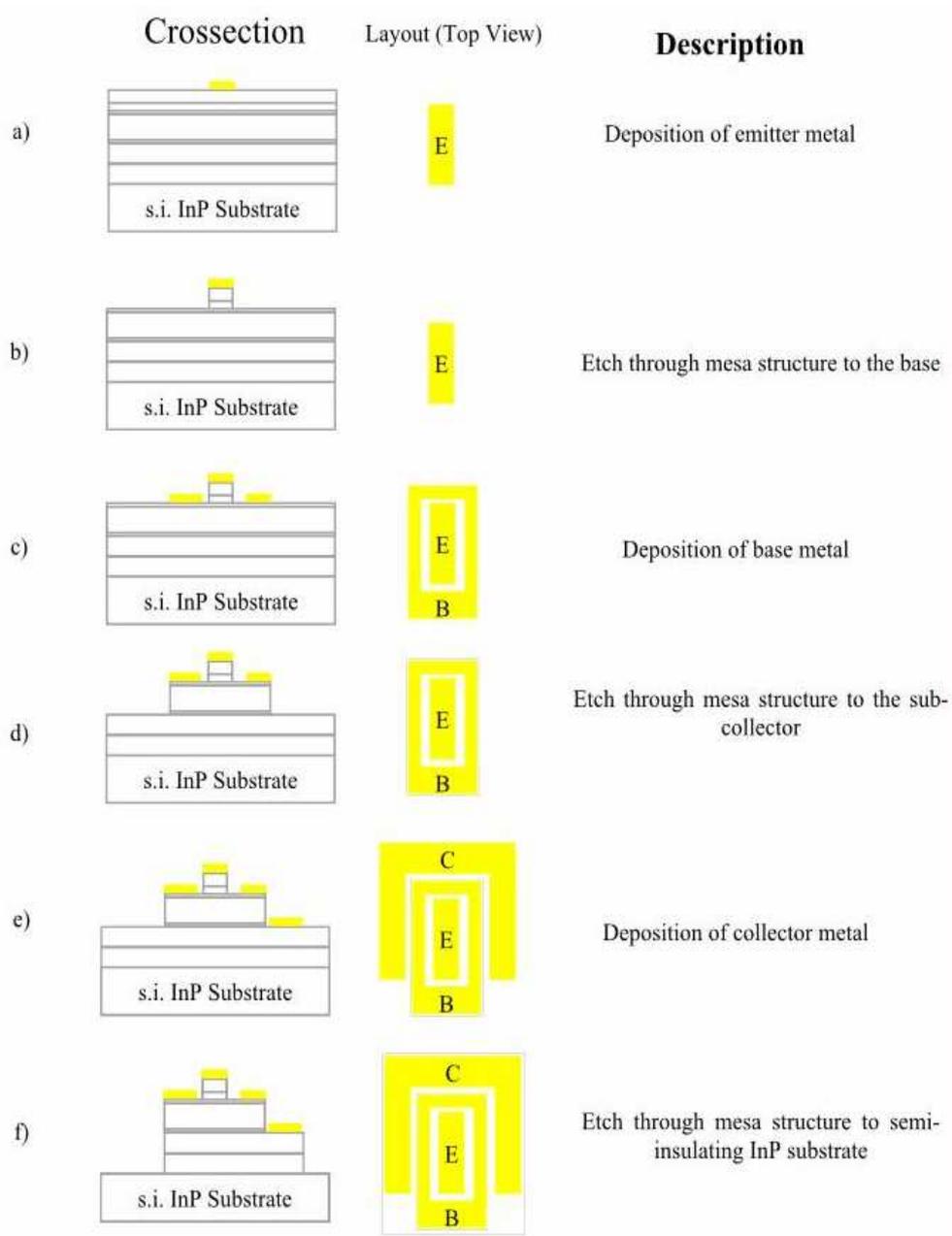


Figure 3-7: Individual processing step flow diagram.

3.2. Processing of InP/InGaAs SHBT

As previously outlined the process of the fabrication of a single heterojunction bipolar transistor (SHBT) in this project consists of eight steps, with each step having a respective layer in the mask. The following flow diagram gives an overview of the fabrication steps used in this project as a whole and their specific order. A more detailed description of the fabrication process can be found in the Appendix A.



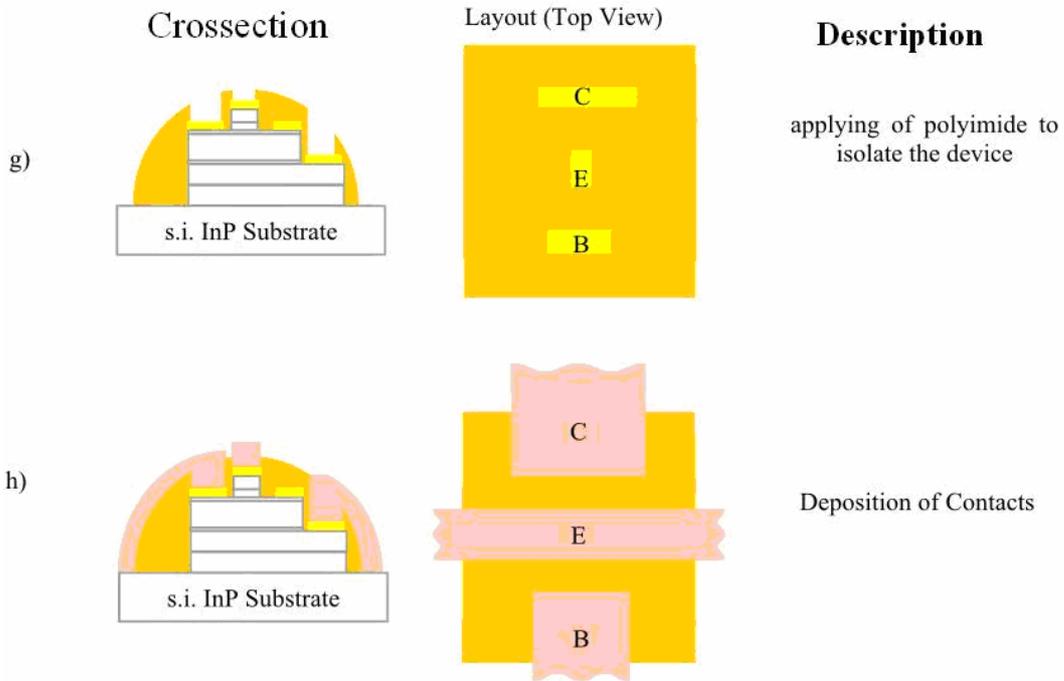


Figure 3-8: Processing of InP/InGaAs SHBT.

The development and deposition of the contacts in step h results in the deposition of the bond pads as shown 3.9. This allows the access of both the DC and RF probes to reach the device as the actual devices are too small to be probed directly.

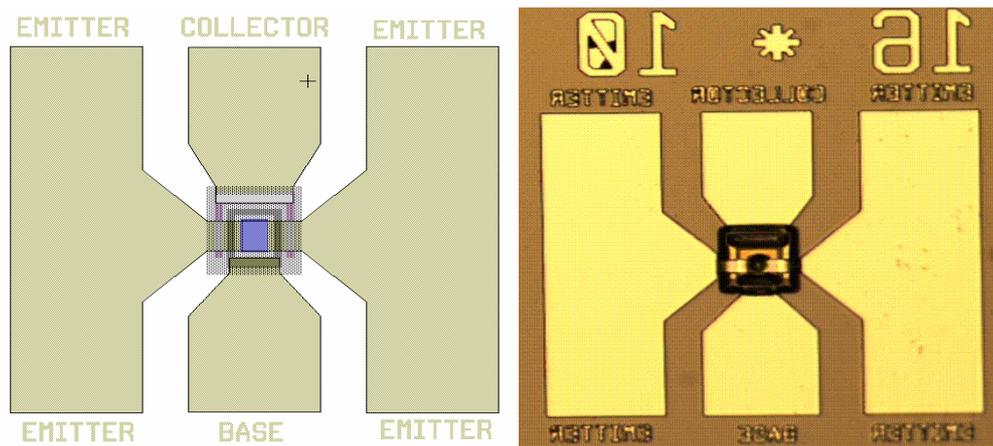


Figure 3-9: Final layout design and a picture of a fabricated dummy device (top down views).

3.3. Etching

With the use of wet etching technique in this project to etch through InP and InGaAs, the use of two highly selective solutions were used to accomplish this.

- The solution used to etch through the InP layers of the wafer uses a solution with a mixture of orthophosphoric acid (H_3PO_4) and hydrochloric acid (HCL) at a ratio of 9:1 respectively. This resulted in an etch rate of $\approx 400\text{nm/min}$ [2]
- While the solution used to etch the InGaAs layers, a solution with the combination of hydrogen peroxide (H_2O_2), orthophosphoric acid (H_3PO_4) and water (H_2O) with a ratio of 1:1:38 respectively. This solution at the stated ratio resulted in an etch rate of $\approx 92\text{nm/min}$ [3]

Both solutions have been found to be highly selective in relation to the semiconductor material they were not desired to etch, be it InGaAs or InP [4].

3.4. Ohmic Contacts

The depositing of metal onto the semiconductor wafers in this project was carried out with the use of electron beam evaporation with the Plassys MEB 450 Electron Beam Evaporator (Plassys I) and Plassys MEB 550S (Plassys II). The process involves first placing the sample, which has been appropriately processed onto a holder, which then is loaded into a vented loadlock and is pumped down to the required pressure. At which point the desired metal structure that has been selected on the computer software is selected, and then the respective layers are evaporated and condenses onto the wafer. After the deposition of the contacts have been applied, the pressure within the loadlock returns up to atmospheric pressure and the sample is withdrawn from the loadlock. At this point the sample is placed into a beaker of Acetone and placed into a warm bath 50°C to remove the S1818 resist along with the unwanted metal that has been deposited on top of the resist, leaving the required metal on the wafer. The metals that were available to be deposited by evaporation were Al, Au, Ge, Pd, Pt, Ti and NiCr.

3.4.1. Ohmic Comparison

Since the development of different epitaxial growth techniques, research has been undertaken into the investigation of metal contacts with various semiconductor materials [5-9]. Tables 3-1 and 3-2 show some of the common metal schemes over the last decades by various groups for both n and p type materials on InGaAs.

Metal Scheme	Specific Contact Resistance [$\Omega \cdot \text{cm}^2$]	Reference
Ti/Pd/Au	$0.73 \pm 0.44 \times 10^{-9}$	[6]
TiW/Ti/Ni	$0.84 \pm 0.48 \times 10^{-9}$	[6]
Ti/Pt/Au	2×10^{-7}	[7]
Ni/Ge/Au	3.5×10^{-7}	[7]
Pd/Ge/Pd/Ti/Au	1.1×10^{-6}	[9]
Pd/Ge/Ti/Pt	3.8×10^{-6}	[9]

Table 3-1: n-type InGaAs contacts.

Metal Scheme	Specific Contact Resistance [$\Omega \cdot \text{cm}^2$]	Reference
Ti/Pd/Au	2×10^{-4}	[10]
Ti/Pt/Au	5.7×10^{-5}	[11]

Table 3-2: : p-type InGaAs contacts.

3.4.2. TLM Theory

It is with the use of the transmission line measurement (TLM) that the quality of the Ohmic contact can be evaluated [12]. This is achieved when two adjacent pads are deposited on a semiconductor material and an applied electron current and voltage is forced through the interface, as shown in Fig 3.10.

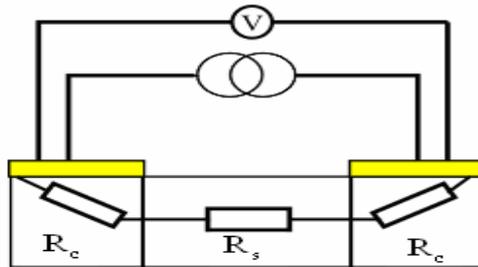


Figure 3-10: TLM characterisation set up.

The current experiences a resistance of both the semiconductor material resistance (R_s) and a contact resistance (R_c) that is brought about by the infusion of holes and electrons between the contact and semiconductor material. The symbols 'W', 'S' and 'd' are the width and length of the metal contact pads and mesa height respectively and are located at a gap spacing of a linearly increasing gap spacing (L) with $L_1 < L_2 < L_3$.

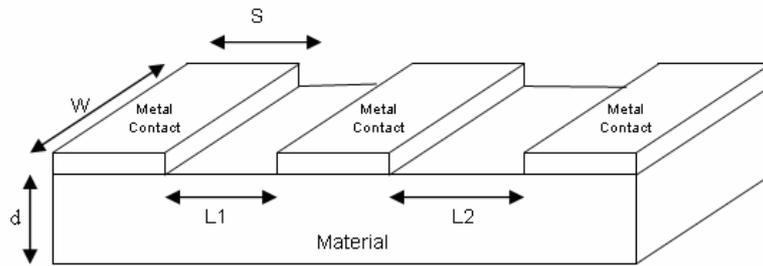


Figure 3-11: Overall TLM cross section.

The measurement of the total resistance drop (R_{total}) for various gap spacing lengths can be obtained and a R_{total} is plotted on a linear graph as a function of pad spacing, an example of which is shown in fig 3.12

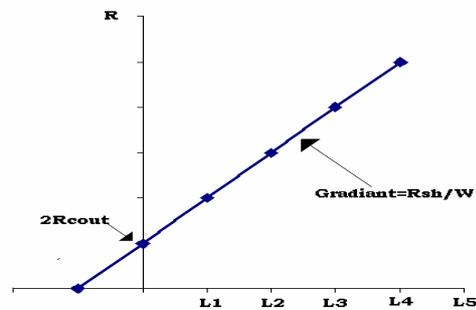


Figure 3-12: Example of R_{total} Vs TLM pad spacing.

From Fig 3.12, it can be extracted that the total resistance R_{total} between the two adjacent pads, can be expressed as:

$$R_{total} = 2R_{con} + R_s \quad (27)$$

Considering R_s and R_{sh} can be expressed as:

$$R_s = \frac{\rho L_x}{dw} \quad (28)$$

$$R_{sh} = \frac{\rho}{d} \quad (29)$$

where:

ρ = resistivity of the semiconductor material

R_{sh} = sheet resistance

L_x = length

When rearranging equations (28) and (29) back into (27) we get:

$$R_{total} = 2R_{con} + R_{sh} \left(\frac{L_x}{w} \right) \quad (30)$$

Thus, giving us a gradient of (R_{sheet}/W) and the x-y intercept points at L_x and $2R_c$. It has been shown that R_{con} and L_T can be expressed as [9]:

$$2R_{con} = \frac{2R_{sk}L_T}{w} \quad (31)$$

where:

R_{sk} = the modified sheet resistance of the semiconductor material directly under the pads

L_T = The transfer length, being the distance that is required for the current to flow in or out of the Ohmic contact.

3.4.3. TLM Evaluation

TLM tests were carried out not only to confirm that the contacts had made good connections to the devices but also as a comparison to the published data from other laboratories. Ohmic contacts used within the research group being 10nm Au / 10nm Ge / 10nm Au / 10nm Ge / 20nm Au / 11nm Ni / 80nm Au and 20nm Ti/ 30nm Pd/ 80nm Au for n-type and p-type contacts, respectively. A summary of the extracted figures of merit for the contacts are shown in Tables 3-3 to 3-5 below. The complete comparison between all the elements of both metal structures for emitter, base and collector, along with all measured data are listed in the Appendix B through to D.

Metal Structure	$R_{con} (\Omega)$	$R_{sh}(\Omega/\square)$	$L_T(\mu m)$
Au/Ge/Au/Ge/Au/Ni/Au	0.31	14.7	3.19
Ti/Pd/Au	0.23	16.51	2.14

Table 3-3: Emitter TLM comparison

With the emitter metal, Ti/Pd/Au metal scheme was used due to its improved contact resistance. Being that this metal contact lays directly on top of the vertical active region of the device the sheet resistance of the layer is not as important when deciding on this Ohmic contact.

Metal Structure	$R_{con} (\Omega)$	$R_{sh}(\Omega/\square)$	$L_T(\mu m)$
Ti/Pt/Au	0.28	646.4	0.31
Ti/Pd/Au	2.75	377.55	1.09

Table 3-4: Base TLM Comparison

Metal Structure	$R_{con} (\Omega)$	$R_{sh} (\Omega/\square)$	$L_T (\mu m)$
Au/Ge/Au/Ge/Au/Ni/Au	0.33	10.87	13.15
Ti/Pd/Au	0.14	2.88	7.5

Table 3-5: Collector TLM Comparison

3.5. Preliminary device evaluation

As it is not possible to evaluate the devices themselves until after the development of bond pads contacts, a few large devices have been placed on the sample to allow direct access by the DC probes to enable the evaluation of the structure. It is from these large devices that the DC characteristic can be extracted after the base and collector contacts have been deposited in Fig 3-13

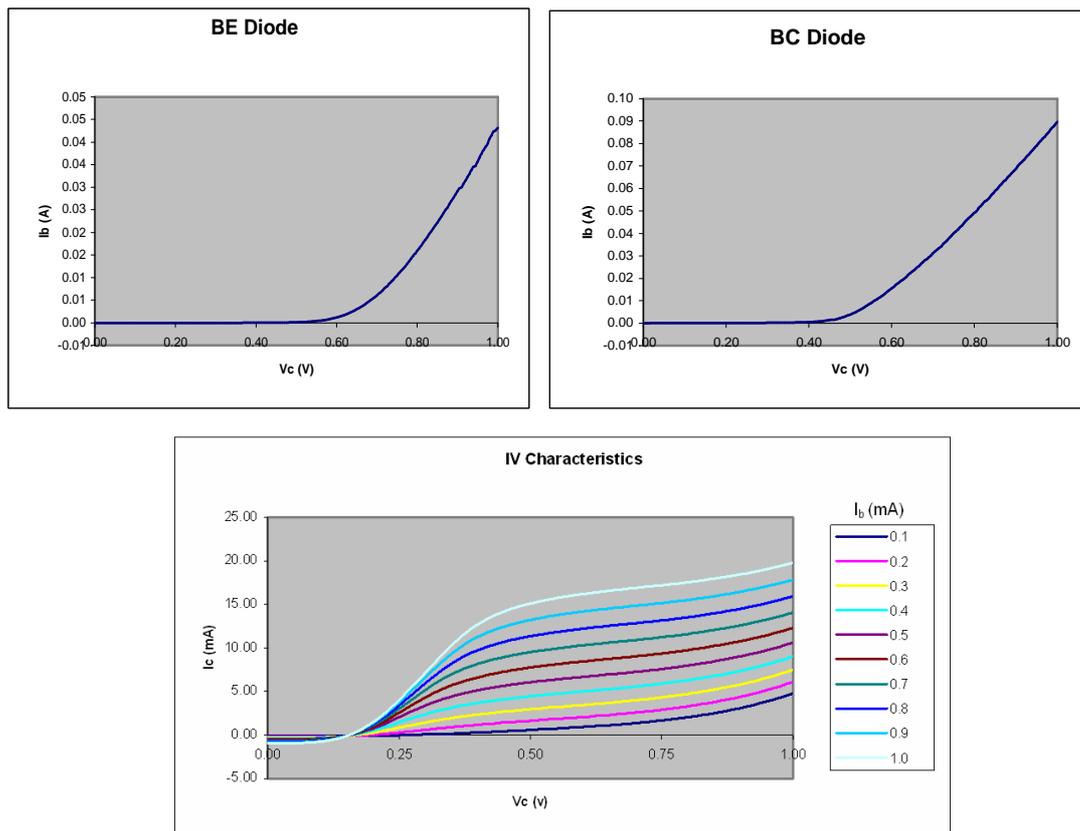


Figure 3-13: Preliminary device evaluation

These large devices as well as the TLM measurements in the evaluation of the Ohmic contacts enable the evaluation of the sample after each step in the processing. This enables the identification and isolation issues in the processing and update the fabrication technique if required.

3.6. HBT structure

The epilayer structure for the wafer used in this project is of a single heterojunction bipolar transistor (HBT) made up of an Npn InP/InGaAs material, as seen below in table 3-6.

Layer No	Layer	Dopent Concentration /cm ⁻³	Thickness (nm)	Type
1	In _{0.53} Ga _{0.47} As	3×10 ¹⁹ :Si	40	Emitter Cap
2	InP	3×10 ¹⁹ :Si	80	Emitter Cap
3	InP	8×10 ¹⁷ :Si	10	Emitter
4	InP	3×10 ¹⁷ :Si	40	Emitter
5	In _{0.53} Ga _{0.47} As	6×10 ¹⁹ :C	40	Base
6	In _{0.53} Ga _{0.47} As	2×10 ¹⁶ :Si	400	Collector
7	InP	1×10 ¹⁹ :Si	10	Etch Stop
8	In _{0.53} Ga _{0.47} As	3×10 ¹⁹ :Si	200	Sub Collector
9	InP	2×10 ¹⁹ :Si	200	Buffer
	Si : InP	Si : InP	Substrate	

Table 3-6: Layer Structure currently being used in this project.

The emitter cap (layer 1+2) are the top most layers in the structure. Due to InGaAs having a smaller band gap than InP it makes it easier to create a good Ohmic contact on InGaAs. The InP emitter cap is used to create a step between the highly doped InGaAs cap and the InP emitter layer.

The emitter is split into two different layers, which includes a highly doped InP to provide electrons for injection into the base. This is on top of another InP less doped layer which is used to reduce the base-emitter junction capacitance as discussed in section 2.2.

The base layer, as discussed earlier in this chapter is the most important layer in a HBT. There are two key things for the base, being the thickness and the doping level. The thinner the base, the shorter the transit time, which increases the cut-off frequency, as well as having a greater DC gain (β). The thinner the base however, the greater the base resistance, to overcome this the base needs to be as highly doped as possible, hence this is why the layer has a dopant concentration of $6 \times 10^{19} \text{ cm}^{-3}$.

The doping level in the collector is lower in comparison to the layers adjacent to it as a high doping is not required here. A low doping level also minimises the base-collector capacitance.

The etch stop layer, like the name indicates, is used primarily used as an etch stop. The sub-collector layer, like the emitter cap, is highly doped to make a good Ohmic contact. All these layers are grown on top of a 200nm InP buffer layer to improve the quality of the device. Below in Fig 3-14 gives the band line-up of the emitter, base and collector region while under equilibrium of the HBT used in this project. It was generated by a programme designed for calculating energy band gap known as 1D Poisson [13].

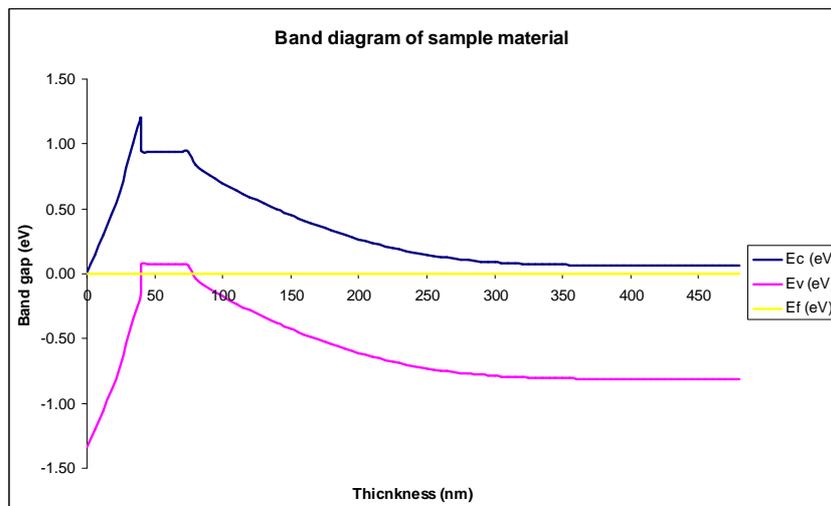


Figure 3-14: Band line-up of emitter, base and collector region of the HBT used in this project while under equilibrium.

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4. Device Characterisation

This chapter presents the DC and RF results obtained from the fabricated devices. The results described here are of an HBT that has an emitter size of $16\mu\text{m}\times 10\mu\text{m}$.

4.1. 4.1 DC Measurements

With the completion of the fabrication of the devices, preliminary tests were performed on the devices in the form of the emitter-base and base-collector diode I-V characteristic. These diode tests are the first chance to test the devices themselves because the bond pads are fabricated last. The testing of the diode I-V characteristic this way enables the isolation of any issues. Figure 4.1 illustrates the forward emitter-base junction from which it is possible to conclude that the turn on voltage is 0.6V

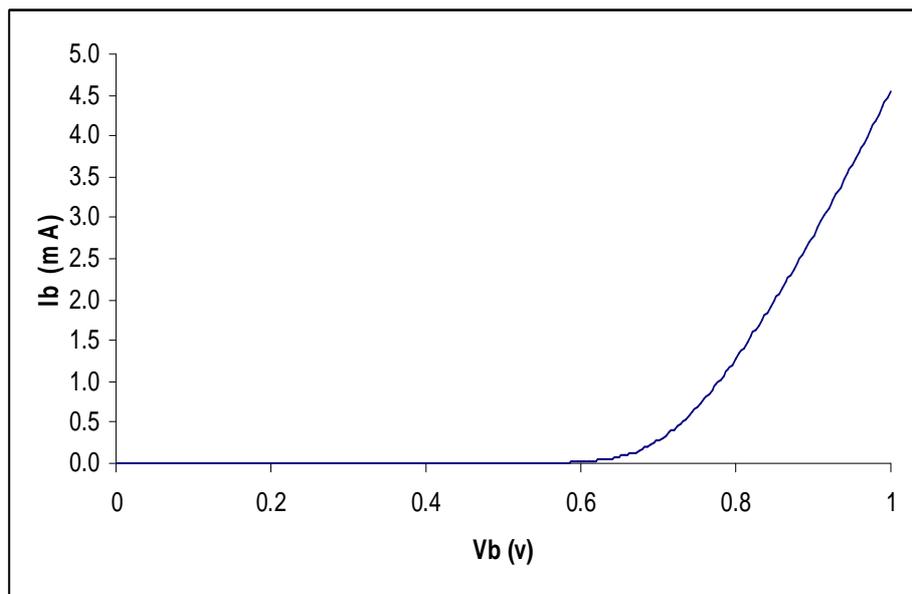


Figure 4-1: Forward biased base-emitter emitter junction diode I-V characteristic.

Next the base-collector diode characteristic is tested from which the turn on voltage is extracted as approx 0.4V

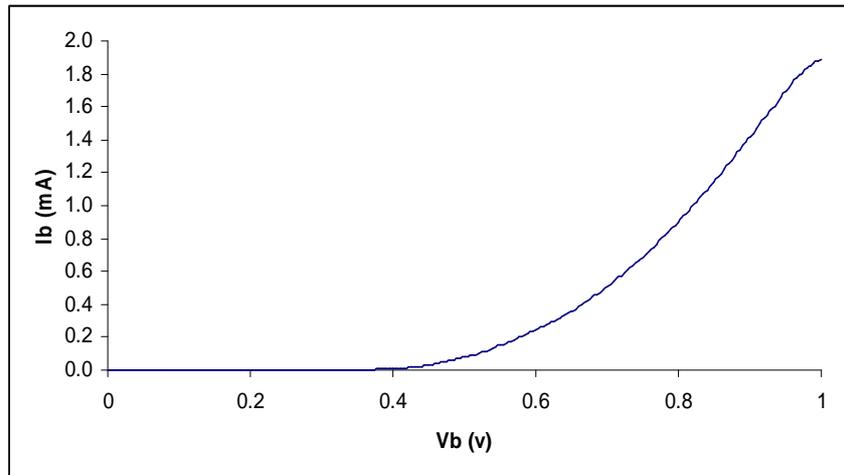


Figure 4-2: Forward biased base-collector junction diode I-V characteristic.

With the completion of the preliminary testing, the DC characteristics can be measured. On setting up the probe station to undertake a DC sweep from 0 to operate 2V for variable base currents (I_B) of $1\mu\text{A}$ to $10\mu\text{A}$ with intervals of $1\mu\text{A}$. This gives us the common emitter output I-V characteristics as shown in figure 4.3.

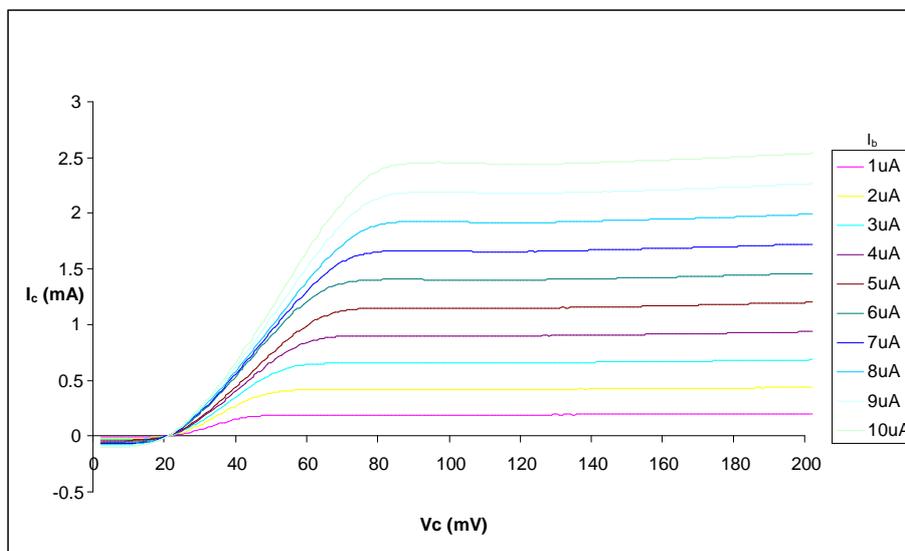


Figure 4-3: Common emitter HBT output I-V characteristics for devices with $16\mu\text{m} \times 10\mu\text{m}$ emitter dimensions.

The DC current gain (β) of the device can be observed from the measured Gummel plot as shown in figure 4.4, for this device, β is extracted as 25.

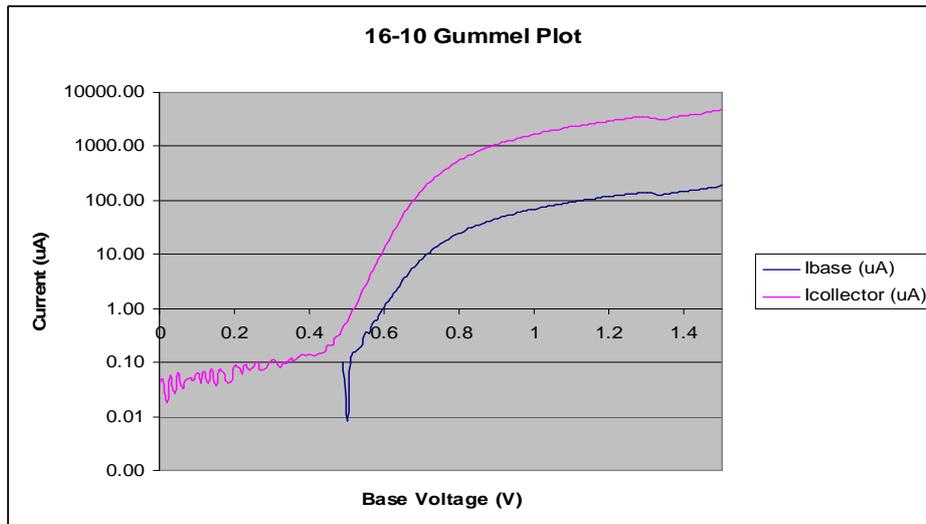


Figure 4-4: Gummel plot of 16 μ m \times 10 μ m HBT.

4.2. RF Characterisation

The measurement of the RF characteristics of a device requires a different technique than that of measuring of DC characteristic. This is due to the difficulties encountered in measuring voltages and currents at microwave frequencies. In contrast, waves are more easily measured in a microwave device. One way of measuring the behaviour of a device is through the incident and reflected waves, this being described by scattering parameters (S-parameters). The basic theory of S-parameters is outlined in the following sub-section.

4.2.1. Scattering Parameters (S-Parameters)

A two-port network that is described by S-parameters is shown in Fig 4-5. This is with the incident power waves a_1 and a_2 , as well as the reflected power waves b_1 and b_2 .

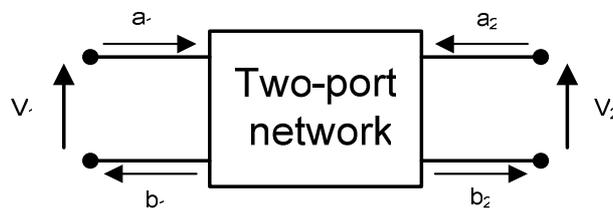


Figure 4-5: Two-port network for S-parameter network

These four waves (a_1 , a_2 , b_1 and b_2) are related by the use of scattering matrix:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (32)$$

The introduction of a source generator whose source impedance matches the line characteristic impedance is connected to the device-under-test (DuT), in the case of $a_1 = 0$ then [2]:

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad (33)$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \quad (34)$$

and when the load is matched, i.e $a_2 = 0$

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad (35)$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad (36)$$

with:

S_{11} = Input port voltage reflection coefficient

S_{12} = The reverse gain ratio of the device

S_{21} = The forward gain ratio of the device

S_{22} = Output port voltage reflection coefficient

4.2.2. RF Calibration Technique

The measurement of S-parameters uses a vector network analyzer (VNA) and it is important to explain the calibration procedure. When measuring with a VNA, imperfections and errors can affect the final results. These errors can be broken down into three different types [1] which include systematic, random and drift errors.

- **Systematic errors** are caused by imperfections brought in by the VNA and cables this includes errors from crosstalk, source and load impedance mismatch as well as frequency response errors caused by reflection. These errors however, can be removed mathematically through calibration.
- **Random errors** occur due to instrumental noise, repeatability of switches, connectors and cables. Even though random errors can be defined, they do however vary with time which makes them unpredictable. As a result they cannot be removed through calibration.

- **Drift Errors** occurs after the initial calibration has been performed due to the changes in VNA performance from variation in ambient temperature. Even though drift error cannot be accounted for with the initial calibration of the VNA, additional calibration techniques can be performed during the data extraction to limit this error.

Calibration of the network analyser is required to be carried out to eliminate errors that would otherwise be introduced to the device by the test station, probes and the cables. The process used in this work for calibration is known as SOLT, and provides a broadband calibration that provides testing over the whole frequency range that is required. SOLT stands for known Short circuit load, Open circuit load, Load ($50\ \Omega$) structure and Thru (transmission line) structure tests and once they have been measured, the results are used to remove errors from the measured S-parameters.

4.2.3. RF Results

With the completion of the calibration of the VNA, measurements of S-parameters at desired bias points can be taken. Figure 4.6 shows the measured S-parameters of the device at 2V and $I_b=50\ \mu\text{A}$ bias point:

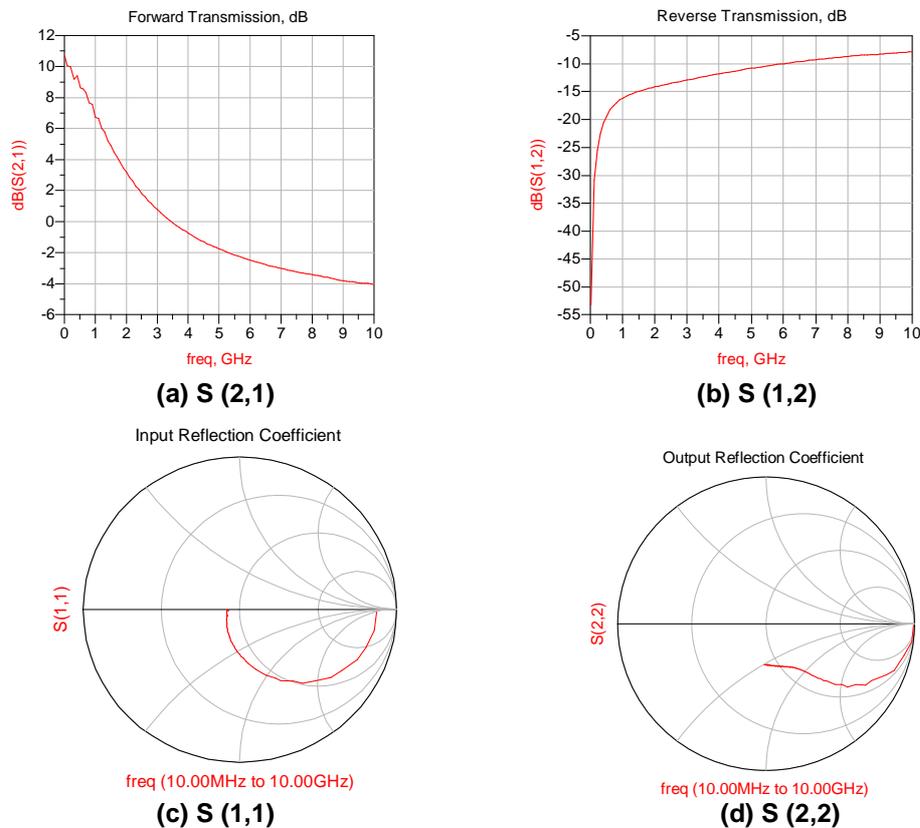


Figure 4-6: Extracted S-Parameters at bias voltage of 2V and bias current of $50\ \mu\text{A}$

S-parameter measurements were carried out over a range of frequencies up to 10 GHz. It is the use of these S-parameters that the F_{MAX} and F_T can be extracted as indicated in fig 4-7. F_T is extracted from h-parameters at indicated in equation (37), while F_{MAX} is defined and extracted as the S_{21} .

$$h_{21e} = \left. \frac{i_2}{i_1} \right|_{v_2=0} = \left. \frac{i_c}{i_b} \right|_{v_{ce}=0} \quad (37)$$

where:

- i_2 = Output applied current
- i_1 = Input applied current
- v_2 = Applied voltage at the input
- i_c = Collector current
- i_b = Base current
- V_{ce} = Collector-emitter voltage

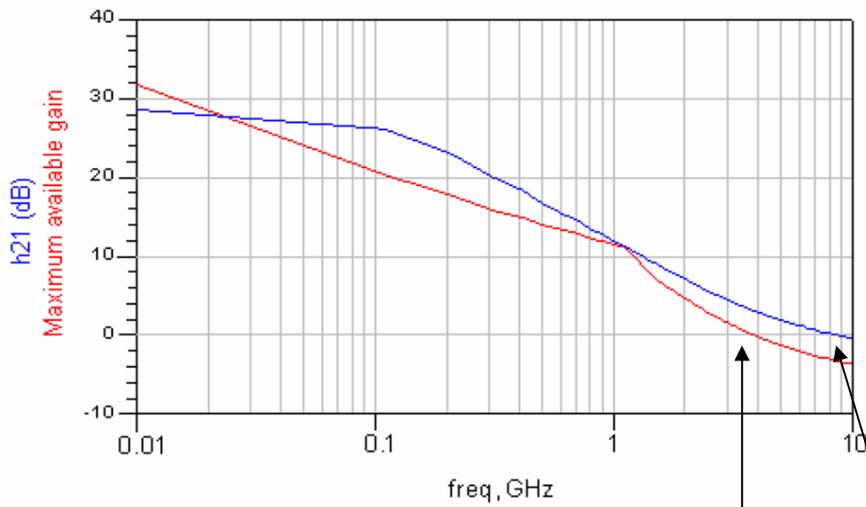


Figure 4-7: F_T and F_{MAX} extraction.

$$f_{max} = 3.5 \text{ GHz} \quad f_T = 9 \text{ GHz}$$

4.3. References

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5. Device Modelling

Accurate extraction of the small-signal equivalent circuit is a crucial part in the process and development of HBTs as it allows for improved device evaluation and modelling. There has been extensive research into this subject area over the last few decades [1-5] in order to improve the accuracy of modelling, with approaches varying from optimisation to purely analytical techniques. Small signal modelling involves a trade-off between the optimisation techniques and the more accurate and simpler technique of direct extraction techniques.

5.1. Analysis

The method adopted here follows on and further improves on the work involved by Sheinman et al. [2], as well as the modelling technique used on HEMTs by MacFarlane et al. [6] which combines the approach of estimating the extrinsic components of the device capacitance and inductances with the use of 3D electromagnetic numerical simulation. The extrinsic resistances are estimated from the geometry of the device and the transmission line method (TLM) test structures. Knowing these extrinsic elements values, these are de-embedded from the S-parameters and the remaining intrinsic values are then estimated analytically. Due to these estimates being highly accurate and close in value to the actual results, optimisation of the whole circuit against measured S-parameters results in a quick convergence to the final values.

The model shown in Figure 5-1 is used as the basis of the small-signal model used in this parameter extraction. With the extrinsic parasitic components, capacitance, Inductance and resistance brought in by the bond pads, while the intrinsic model being marked within the dash line and is based on the typical bias dependent T-model of HBTs [7]. The element values can be extracted from measured data, both from the final S-parameters as well as from the TLM test structures as discussed below.

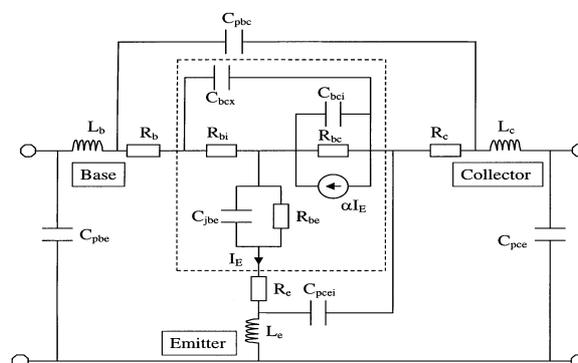


Figure 5-1: Small-signal equivalent circuit of an HBT.

5.1.1. Pad Capacitances-

The extrinsic base-collector, base-emitter and collector-emitter capacitances (C_{pbc} , C_{pbe} and C_{pce} respectively) are simulated in Agilent's Momentum software, which is a 3D electromagnetic simulator. Once the bond pads of the device have been drawn in (as seen below in Fig. 5-2a) with the accurate dimensions, along with the relative dielectric constants of the substrate, the software applies a technique "method of moments" to Maxwell's electromagnetic equations to analyse the structure. The result of the simulations produces S-parameters which are then converted into Y-parameters, and it is from these parameters (equations 38-40 below) that the extrinsic capacitances, as shown in Fig.5-2b, can be calculated and evaluated

$$Y_{11} = j\omega.(C_{pbe} + C_{pbc}) \quad (38)$$

$$Y_{12} = Y_{21} = -j\omega.C_{pbc} \quad (39)$$

$$Y_{22} = j\omega.(C_{bc} + C_{pbc}) \quad (40)$$

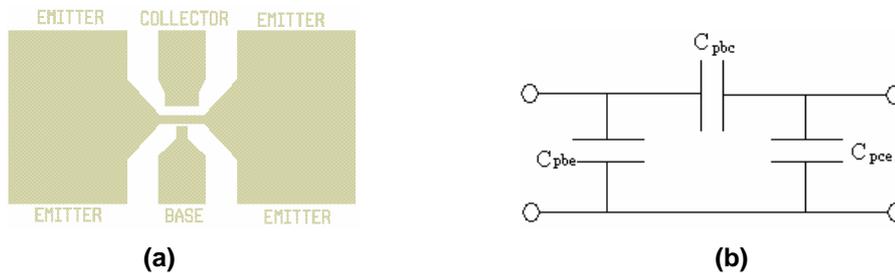


Figure 5-2: a) Layout of open-circuited bond pads (b) Electrical equivalent circuit for the pads

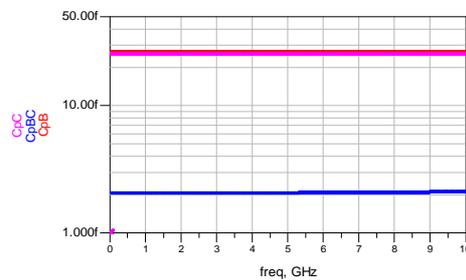


Figure 5-3: Extracted pad capacitances.

5.1.2. Pad Inductances

The extrinsic emitter, base and collector Inductances (L_e , L_b and L_c respectively) are simulated in a similar method to those of the pad capacitances mentioned above, except a short circuit is placed where the transistor would sit (Fig 5-4a below). Agilent's Momentum software, simulates the S-parameters from the test structure, from which the Z-parameters are extracted and the inductances are calculated from these, using equations (41-43) which results in pad Inductances equivalent circuit (Fig. 5-4b below). This results of which is shown in fig 5-5.

$$Z_{11} = j\omega.(L_b + L_e) \quad (41)$$

$$Z_{12} = j\omega.L_e \quad (42)$$

$$Z_{22} = j\omega.(L_c + L_e) \quad (43)$$

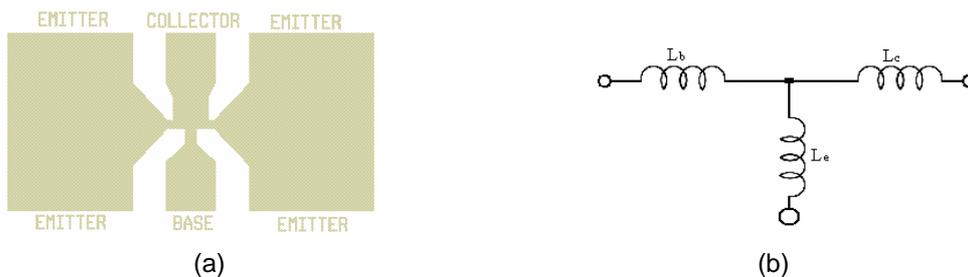


Figure 5-4: a) Layout of short-circuited bond pads, (b) Electrical equivalent circuit for the pads.

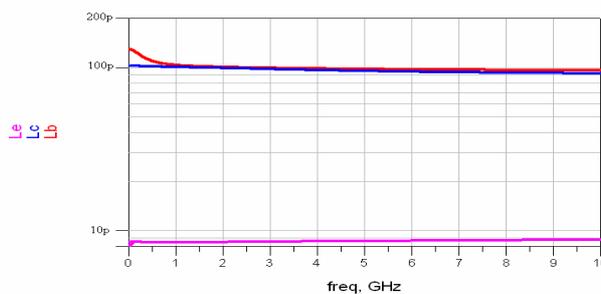


Figure 5-5: Extracted pad inductances.

5.1.3. Contact and Access Resistances

The extrinsic emitter (R_e), base (R_b) and collector (R_c) resistances are calculated from the extracted sheet resistance and contact resistances from the transmission line measurements (TLM) test structures that are carried out at each of the three metallisation steps (emitter, base and collector). Once the values for R_{sh} and R_c have been acquired, the access resistance is calculated through combining the known geometry (In the case of the base, the four gray regions

highlighted in Fig.5-6 below) of the access region of the device (highlighted by the arrows in Fig. 5-7), with the sheet resistance (R_{sh}) and the addition of the contact resistance (R_{sh}). The results are set out below in Table 1 using (20 nm)Ti / (30 nm) Pd / (80 nm) Au Ohmic contacts.

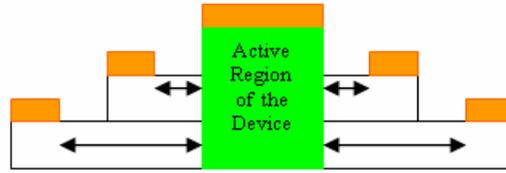


Figure 5-6: Active Region and access region of device

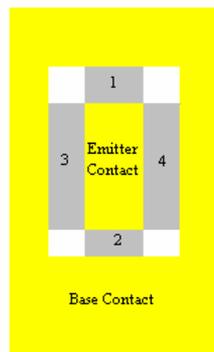


Figure 5-7: Known geometry of device

	Layer	Doping (cm^{-3})	$R_{con}(\Omega)$	$R_{sh}(\Omega/\square)$
Emitter Cap	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	3×10^{19} : Si	0.22	16.51
Base	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	6×10^{19} : C	2.75	377.55
Sub-Collector	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	3×10^{19} : Si	0.15	2.88

Table 5-1: Sheet (R_{sh}) and contact (R_{sh}) Ohmic contact resistances.

5.1.4. Intrinsic Elements

The intrinsic and extrinsic base-collector capacitances (C_{bcx} and C_{bci}) were estimated as they are area dependent. They are able to be estimated with the use of equation (44) below.

$$C = \frac{\epsilon_r \cdot \epsilon_0 \cdot A}{t} \quad (44)$$

where:

A_r = Cross-section area of metallic contact (m^2)

ϵ_r = Relative permittivity of the dielectric (F/m)

ϵ_0 = Permittivity of free space (F/m)

t = Thickness of dielectric (metres)

The intrinsic and extrinsic base-collector capacitances can be calculated this way because of the high dopant concentrations of the base and sub-collector. As they are separated by a lightly doped collector layer then this acts like a plate capacitor which is area dependant. Since all the extrinsic components have been estimated, we then de-embedded these values from the original S-parameters results, the remaining elements can all be expressed in the form of Z-parameters as follows [4]:

$$[Z_{\text{int}}] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} R_{bi} + \frac{1}{Y_{be}} & \frac{1}{Y_{be}} \\ \frac{1}{Y_{be}} - \frac{\alpha}{Y_{bc}} & \frac{1}{Y_{be}} + \frac{1}{Y_{bc}}(1 - \alpha) \end{bmatrix} \quad (45)$$

where:

$$Y_{be} = \frac{1}{R_{be}} + j\omega C_{be} \quad (46)$$

$$Y_{bc} = \frac{1}{R_{bc}} + j\omega C_{bci} \quad (47)$$

From (44-46) gives us:

$$R_{bi} = Z_{11} - Z_{12} \quad (48)$$

$$R_{be} = \frac{1}{\text{Re}\left(\frac{1}{Z_{12}}\right)} \quad (49)$$

$$R_{bc} = \frac{1}{\text{Re}\left(\frac{1}{Z_{22} - Z_{21}}\right)} \quad (50)$$

and

$$\alpha = \frac{Z_{12} - Z_{21}}{Z_{22} - Z_{21}} \quad (51)$$

where:

α being the common-base high frequency current gain

Since all the intrinsic components of the small-signal model are now known, the result can be compared and optimised using a multi-variable optimisation technique in Agilent's Advanced Design Systems to provide the best fit of the measured and modelled S-parameters. The

importance of the need to optimise these values is due to the fabrication process would have a small effect, although, as discussed previously, the estimation and data extraction are highly accurate estimates so only a brief convergence to the final values is required.

5.2. Results

The measured S-parameters for a $16\mu\text{m}\times 10\mu\text{m}$ HBT device biased at $V_{CE} = 2\text{V}$ and $I_B = 50\mu\text{A}$ are shown figures 5-8 and 5-9:

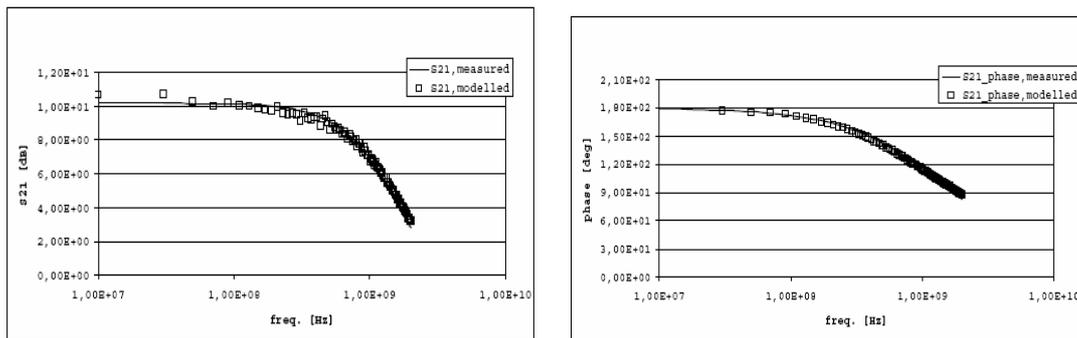


Figure 5-8: Frequency plots of the measured and modelled S_{21} .

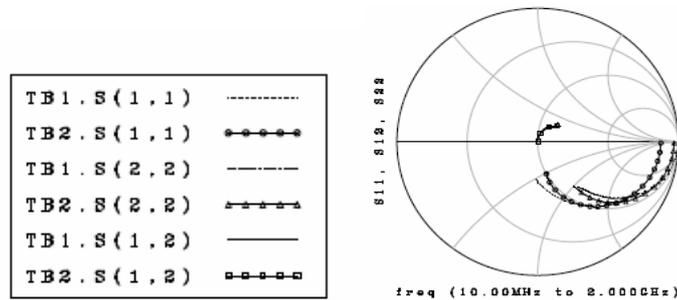


Figure 5-9: Comparison between modelled and measured S-parameters.

The estimated and optimised small-signal equivalent circuit element values are shown below in Tables 5-2 and 5-3.

	R_e	R_c	R_b	L_e	L_c	R_b	C_{pbc}	C_{pce}	C_{pbe}
	Ω	Ω	Ω	pH	pH	Ph	fF	fF	fF
Est.	0.4	1.91	28.14	8.4	110	100	2.060	25.48	26.31
Opt.	0.39	2.18	20	8.14	113	96.9	2.25	28.3	27.8

Table 5-2: Comparison between estimated and optimised parasitic components.

	α	R_{be}	R_{bi}	R_{bc}	C_{be}	C_{bcx}	C_{bci}
	-	Ω	Ω	k Ω	pF	fF	fF
Est.	0.964	30	147	22	4.5	440	40
Opt.	0.966	23.2	100	20.9	3.82	450	31

Table 5-3: Comparison between extracted and optimised Parasitic Components.

5.3. References

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6. Conclusion

The aim of the work described in this dissertation was the development and fabrication of an InP/InGaAs based SHBT using wet etching technique. The fabrication of a InP/InGaAs based SHBT with emitter dimensions of $16\mu\text{m}\times 10\mu\text{m}$ was successfully accomplished and this was characterised both at DC and RF. The project completed with the successful extraction of the small-signal RF model for the HBT. Using an extraction methodology in which the extrinsic parasitic transistor elements were estimated from the device geometry and the TLM measurements and the intrinsic elements were extracted from the s-parameters.

Future Work

- Fabricate smaller device sizes with the use of wet etch due to its high selectivity capability. For sub-micron devices, the use of e-beam lithography would be required due to its high accuracy in the defining of structures in the nanometre scale.
- Evaluate of the small-signal equivalent circuit model for high speed devices.

Appendices

Appendix A: Accurate Fabrication Process Overview

Initial Sample Cleaning

5mins in Acetone in ultrasonic bath

5mins in Methanol in ultrasonic bath

5mins in IPA in ultrasonic bath

Rinse in RO water

Blow dry with N₂ gas

Metallisation

Spin S1818 resist at 4,000rpm for 120s

Bake on hot plate at between 60°C and 65 °C

Place in developer solution and RO water at a ratio of 1:1 for 1min

Expose on MA6 for 5secs

Place in developer solution and RO water at a ratio of 1:1 for 75secs

Check under microscope

Ashering in O₂ plasma for 80 Watts for 3mins

De-oxidise sample for 60secs

Rinse in RO water

Blow dry with N₂ gas

Place sample into Plassys and deposit the metal

Place sample into warm bath (50°C) for 3 hours

Place sample into IPA solution and then ultrasonic bath for 3minutes

Rinse in RO water

Blow dry

Etching Process

Spin S1818 resist at 4,000rpm for 120s

Bake on hot plate at between 60°C and 65 °C

Expose on MA6 for 5secs

Place in developer solution and RO water at a ratio of 1:1 for 80secs

Inspect under microscope

De-oxidise sample for 60secs

Rinse in RO water

Blow dry
Etch InGaAs layer using in $\text{H}_2\text{O}_2:\text{H}_3\text{PO}_4:\text{H}_2\text{O}$ on a 1:1:38 ratio
Rinse in RO water
Etch InP layer using $\text{H}_3\text{PO}_4:\text{HCl}$ on a 9:1 ratio
Rinse in RO water
Blow dry
Place into acetone and then into the warm bath (50°C) for an hour
Check height measurements under Dektak

Polyimide

Mix polyimide Polymer with RO on a 5:1000 ratio
Put solution onto sample and wait 20secs
Spin on recipe 9 (5Secs at 4,000rpm)
Bake on hot plate @ 120 °C for 1min
Put polyimide onto sample
Spin on recipe 6 for 5 Secs
Spin on recipe 1
Bake on hot plate at 140°C for 20minutes
Spin on S1818 on recipe 1
Bake for 90 secs at 115°C
Expose on MA6 for 11 secs and Gap of 50µm
Place in CD-26 for 20s
Rinse in RO water
Check under microscope
Place in Acetone and then into warm bath for 30mins
Bake sample for 5mins at 140°C
Bake sample in oven (180°C) for 20mins

Bond Pads

Spin LOR 10A at 3,000rpm for 45Secs
Bake at 150°C for 5mins
Spin S1818 resist for 30s at 4,000rpm
Bake at 115°C for 1min
Expose S1818 for 5.0s on MA6
Place in developer solution and RO water at a ratio of 1:1 for 75secs
Bake in oven at 120 °C for 20mins
Develop LOR10a and S1818 using LDD-26W solution for 1min

Rinse in RO water

Blow dry

Metal deposition using either Plassys machines

Immerse samples in SVC-14 positive stripper

Rinse with RO Water

Check under microscope

Appendix B: Emitter TLM results

20Ti/30Pd/80Au

	1	2	3	4	6	7	8	9	OVERAL
3	0.80183	0.78202	0.81288	0.80345	0.71111	0.68695	0.87176	0.82859	0.787
5	1.02519	1.01189	1.00947	1.03443	0.95674	0.94218	1.08749	1.04291	1.014
7	1.23754	1.28238	1.23869	1.26523	1.20477	1.17321	1.24817	1.28347	1.242
9	1.41274	1.45558	1.42238	1.4764	1.44162	1.41803	1.44919	1.48625	1.445
CORR	0.999	0.997	0.999	1.000	1.000	1.000	0.999	1.000	0.999
Rsh/Wpad [$\Omega/\mu\text{m}$]	0.1023	0.1146	0.1029	0.1125	0.1220	0.1212	0.0946	0.1107	0.110
2Rcont [Ω]	0.5058	0.4456	0.5035	0.4700	0.3467	0.3278	0.5963	0.4962	0.461
Rsh [Ω/\square]	15.34	17.18	15.43	16.87	18.30	18.18	14.20	16.60	16.513
Rcont [Ω]	0.25	0.22	0.25	0.23	0.17	0.16	0.30	0.25	0.231
L _T [μm]	2.47	1.94	2.45	2.09	1.42	1.35	3.15	2.24	2.140
Sp.Rcont [$\Omega*\mu\text{m}^2$]	94	65	92	74	37	33	141	83	77.422

10Au/10Ge/10Au/10Ge/20Au/11Ni/80Au

	1	2	3	4	5	6	Average
3	1.0905	1.0578	0.897	0.906	0.88532	0.8424056	0.947
5	1.2708	1.2454	1	1.08	1.0323	1.03251	1.110
7	1.4933	1.4414	1.3792	0.7565	1.2549	1.25629	1.264
9	1.6729	1.6394	1.9605	1.195	1.39694	1.43963	1.551
CORR	0.999	1.000	0.958	0.364	0.996	0.999	0.988
Rsh/Wpad [$\Omega/\mu\text{m}$]	0.0985	0.0971	0.1785	0.0272	0.0879	0.1008	0.0983
2Rcont [Ω]	0.7910	0.7637	0.2383	0.8213	0.6151	0.5381	0.6279
Rsh [Ω/\square]	14.8	14.6	26.8	4.1	13.2	15.1	14.7
Rcont [Ω]	0.40	0.38	0.12	0.41	0.31	0.27	0.31
L _T [μm]	4.02	3.93	0.67	15.11	3.50	2.67	3.19
Sp.Rcont [$\Omega*\mu\text{m}^2$]	238	225	12	931	161	108	150

Annealing: Au/Ge/Au/Ge/Au/Ni/Au - 380°C for 1min
Ti/Pd/Au - None

Appendix C: Base TLM Results

20Ti/30Pt/80Au

Sample:	Base 1		Base 2		Base 3		Average
Spacing	1	2	3	4	5	6	
3	10.2178	10.1988	0.712	29.3			8.405
5	16.2255	16.2959	38.7	40.3	16.2959	16.2716	24.015
7	21.7541	22.1319	50.5	49.4	22.1317	22.1319	31.342
9	27.2642	27.3116	59.3	61.3	27.3116	27.3868	38.312
CORR	1.000	0.999	0.938	0.999	0.999	1.000	0.989
Rsh/Wpad [W/mm]	2.8334	2.8587	9.3782	5.2550	2.7539	2.7788	4.310
2Rcont [W]	1.8651	1.8322	-18.9662	13.5450	2.6356	2.4785	0.565
Rsh [W/°]	425.0	428.8	1406.7	788.3	413.1	416.8	646.451
Rcont [W]	0.93	0.92	-9.48	6.77	1.32	1.24	0.283
L _T [mm]	0.33	0.32	-1.01	1.29	0.48	0.45	0.309
Sp.Rcont [W*mm ²]	46	44	1438	1309	95	83	502.528

20Ti/30Pd/80Au

Sample:	1-1				Average	1-2				Average	OVERAL
Spacing	1	2	3	4		6	7	8	9		
3	12.9703	15.58	12.749	12.5985	13.47443		12.4864	12.4739	12.5435	12.50127	12.988
5	18.4862	17.353	18.1083	18.127	18.01855	18.2161	18.0835	18.7626	18.0731	18.28383	18.151
7	23.2513	22.004	23.3428	23.3377	22.98398	23.3371	23.4125	23.2835	23.4258	23.36473	23.174
9	28.0433	26.127	28.0988	28.6556	27.73125	27.7256	28.9535	28.2905	28.8526	28.45555	28.093
CORR	0.99936	0.98543	0.99963	0.99993	0.99987	0.99901	0.99996	0.99755	0.99998	0.99948	0.99994
Rsh/Wpad [$\Omega/\mu\text{m}$]	2.4992	1.8147	2.5642	2.6691	2.3868	2.3774	2.7365	2.5985	2.7140	2.6472	2.517
2Rcont [Ω]	5.6925	9.3779	5.1896	4.6651	6.2313	6.4513	4.3149	5.1114	4.4398	4.7682	5.500
Rsh [Ω/\square]	374.88	272.20	384.63	400.37	358.02	356.61	410.48	389.78	407.10	397.08	377.549
Rcont [Ω]	2.85	4.69	2.59	2.33	3.12	3.23	2.16	2.56	2.22	2.38	2.750
L _T [μm]	1.14	2.58	1.01	0.87	1.31	1.36	0.79	0.98	0.82	0.90	1.09
Sp.Rcont [$\Omega*\mu\text{m}^2$]	486	1817	394	306	610	656	255	377	272	322	451

Appendix C: Collector TLM Results

20Ti/30Pd/80Au

Sample:	1-1				Average	1-2				Average	OVERAL
Spacing	1	2	3	4		6	7	8	9		
3	0.35031	<i>0.3433</i>	0.33675	0.341846	0.343041	0.341144	<i>0.349427</i>	0.36271	0.35498	0.352064	0.348
5	0.38021	<i>0.3743</i>	0.383998	0.380851	0.37985	0.373329	<i>0.396658</i>	0.40261	0.391282	0.39097	0.385
7	0.42107	<i>0.4105</i>	0.414634	0.416743	0.415729	0.416957	<i>0.414992</i>	0.42955	0.435683	0.424296	0.420
9	0.45033	<i>0.4505</i>	0.452877	0.466561	0.45506	0.48365	<i>0.456123</i>	0.46873	0.485097	0.473401	0.464
CORR	0.99781	0.99844	0.99657	0.99741	0.99982	0.98656	0.98775	0.99733	0.99771	0.99692	0.99876
Rsh/Wpad [$\Omega/\mu\text{m}$]	0.0170	0.0179	0.0190	0.0205	0.0186	0.0236	0.0169	0.0173	0.0217	0.0199	0.0192
2Rcont [Ω]	0.2982	0.2873	0.2834	0.2785	0.2868	0.2624	0.3028	0.3124	0.2863	0.2910	0.2889
Rsh [Ω/\square]	2.56	2.68	2.84	3.08	2.79	3.53	2.54	2.59	3.26	2.98	2.88
Rcont [Ω]	0.15	0.14	0.14	0.14	0.14	0.13	0.15	0.16	0.14	0.15	0.14
L_T [μm]	8.75	8.03	7.48	6.79	7.71	5.57	8.95	9.05	6.59	7.32	7.51
Sp.Rcont [$\Omega*\mu\text{m}^2$]	196	173	159	142	166	110	203	212	141	160	163

Sample:	Collector 1		Collector 2		Collector 3		Average
Spacing	1	2	3	4	5	6	
3	0.7487	0.704883	<i>0.652</i>	<i>0.7752</i>	0.712275	0.720708	0.719
5	0.7796	0.754119	<i>1.8977</i>	<i>2.4987</i>	0.756446	0.779645	1.244
7	0.8059	0.797957	<i>2.002</i>	<i>2.269</i>	0.803177	0.805862	1.247
9	0.8304	0.834927	<i>1.97</i>	<i>1.9</i>	0.839975	0.831541	1.201
CORR	0.99857	0.99800	0.80143	0.53100	0.99884	0.97542	0.884
Rsh/Wpad [W/mm]	0.0136	0.0217	0.2029	0.1572	0.0215	0.0179	0.072
2Rcont [W]	0.7098	0.6428	0.4129	0.9173	0.6490	0.6768	0.668
Rsh [W/ \square]	2.03	3.25	30.44	23.59	3.22	2.69	10.871
Rcont [W]	0.35	0.32	0.21	0.46	0.32	0.34	0.334
L_T [mm]	26.17	14.81	1.02	2.92	15.10	18.87	13.147
Sp.Rcont [W*mm ²]	1393	714	32	201	735	958	671.994

Annealing: Au/Ge/Au/Ge/Au/Ni/Au - 380°C for 1min

Ti/Pd/Au - None

Appendix D: TLM Comparison

Spacing	Emitter			Base			Collector		
	Original	New	Difference	Original	New	Difference	Original	New	Difference
3	0.947	0.787	0.159	8.405	12.988	-4.583	0.719	0.348	0.371
5	1.110	1.014	0.096	24.015	18.151	5.864	1.244	0.385	0.859
7	1.264	1.242	0.022	31.342	23.174	8.167	1.247	0.420	0.827
9	1.551	1.445	0.105	38.312	28.093	10.219	1.201	0.464	0.737
CORR	0.988	1.000	-0.012	0.989	1.000	-0.011	0.884	0.999	-0.115
Rsh/Wpad [$\Omega/\mu\text{m}$]	0.098	0.110	-0.012	4.310	2.517	1.793	0.072	0.019	0.053
2Rcont [Ω]	0.628	0.461	0.166	0.565	5.500	-4.935	0.668	0.289	0.379
Rsh [Ω/\square]	14.746	16.513	-1.767	646.451	377.549	268.902	10.871	2.885	7.986
Rcont [Ω]	0.314	0.231	0.083	0.283	2.750	-2.467	0.334	0.144	0.190
L _T [μm]	3.194	2.096	1.098	0.309	1.093	-0.784	13.147	7.511	5.635
Sp.Rcont [$\Omega*\mu\text{m}^2$]	150.398	72.547	77.850	502.528	450.646	51.883	671.994	162.757	509.238