Scaling and Variability in Ultra Thin Body Silicon on Insulator (UTB SOI) MOSFETs

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Dedication

"*So, verily, with every difficulty, there is relief. Verily, with every difficulty there is relief.*" (Al-Inshirah: 5-6)

To my husband, Nurulfajar Abd Manap – for his love, passion and fortitude
my solehah princess, Nur Najla Alia – for her pure affection and sacrifice
my dearest parents & families – for their endless *dua'* and supports

And my late son, Amir Yusuf – who has taught me the true meaning of patience, humble, perseverance, life and hope.

"With you, it wasn't long enough together, but it was long enough to last forever."

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Abstract

The main objective of this thesis is to perform a comprehensive simulation study of the statistical variability in well scaled fully depleted ultra thin body silicon on insulator (FD-UTB SOI) at nanometer regime. It describes the design procedure for template FD-UTB SOI transistor scaling and the impacts of statistical variability and reliability the scaled template transistor.

The starting point of this study is a systematic simulation analysis based on a well-designed 32nm thin body SOI template transistor provided by the FP7 project PULLNANO. The 32nm template transistor is consistent with the International Technology Roadmap for Semiconductor (ITRS) 2009 specifications. The well-established 3D 'atomistic' simulator GARAND has been employed in the designing of the scaled transistors and to carry out the statistical variability simulations. Following the foundation work in characterizing and optimizing the template 32 nm gate length transistor, the scaling proceeds down to 22 nm, 16 nm and 11 nm gate lengths using typically 0.7 scaling factor in respect of the horizontal and vertical transistor dimensions. The device design process is targeted for low power applications with a careful consideration of the impacts of the design parameters choice including buried oxide thickness (T_{BOX}), source/drain doping abruptness (σ) and spacer length (L_{spa}). In order to determine the values of T_{BOX}, σ, and L_{spa}, it is important to analyze simulation results, carefully assessing the impact on manufacturability and to consider the corresponding trade-off between short channel effects and on-current performance. Considering the above factors, T_{BOX} = 10nm, σ = 2nm/dec and L_{spa} = 7nm have been adopted as optimum values respectively.

The statistical variability of the transistor characteristics due to intrinsic parameter fluctuation (IPF) in well-scaled FD-UTB SOI devices is systematically studied for the first time. The impact of random dopant fluctuation (RDF), line edge roughness (LER) and metal gate granularity (MGG) on threshold voltage (V_{th}), on-current (I_{on}) and drain induced barrier lowering (DIBL) are analysed. Each principal sources of variability is treated individually and in combination with other variability sources in the simulation of large ensembles of microscopically different devices. The introduction of high-k/metal gate stack has improved the electrostatic integrity and enhanced the overall device performance. However, in the case of fully depleted channel transistors, MGG has become a dominant variability factor for all critical electrical parameters at gate first technology. For instance, σV_{th} due to MGG increased to 41.9 mV at 11nm gate length compared to 26.0 mV at 22nm gate length. Similar trend has also been observed in σI_{on}, increasing from 0.065 up to 0.174 mA/μm when the gate length is reduced from 22 nm down to 11 nm. Both RDF and LER have significant role in the intrinsic parameter fluctuations and therefore, none of these sources should be overlooked in the simulations.

Finally, the impact of different variability sources in combination with positive bias temperature instability (PBTI) degradation on V_{th}, I_{on} and DIBL of the scaled nMOSFETs is investigated. Our study indicates that BTI induced charge trapping is a crucial reliability problem for the FD-UTB SOI transistors operation. Its impact not only introduces a significant degradation of transistor performance, but also accelerates the statistical variability. For example, the effect of a late degradation stage (at trap density of 1e12/cm^2) in the presence of RDF, LER and MGG results in σV_{th} increase to 36.9 mV, 45.0 mV and 58.3 mV for 22 nm, 16 nm and 11 nm respectively from the original 29.0 mV, 37.9 mV and 50.4 mV values in the fresh transistors.

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Publications

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Nomenclatures

Acronyms

1D	One dimension
2D	Two dimensions
3D	Three dimensions
BOX	Buried Oxide
BTI	Bias Temperature Instability
CIC	Cloud In Cell
CMOS	Complementary Metal Oxide Semiconductor
DD	Drift-Diffusion
DG	Density Gradient
DI	Dielectric Isolation
DIBL	Drain Induced Barrier Lowering
EOT	Equivalent Oxide Thickness
ESD	Elevated Source Drain
FD-UTB SOI	Fully Depleted Ultra Thin Body Silicon on Insulator
FinFET	Fin Field Effect Transistor
FIPOS	Full Isolation Porous Oxidized Silicon
GAA	Gate All Around
GIDL	Gate Induced Drain Leakage

GSS	Gold Standard Simulations
IC	Integrated Circuit
IPF	Intrinsic Parameter Fluctuation
ITRS	International Technology Roadmap for Semiconductors
LER	Line Edge Roughness
LOP	Low Operating Power
LTTV	Layer Total Thickness Variation
MC	Monte Carlo
MGG	Metal Gate Granularity
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability
NTRS	National Technology Roadmap for Semiconductors
OTV	Oxide Thickness Variations
PBTI	Positive Bias Temperature Instability
RDF	Random Dopant Fluctuation
SCE	Short Channel Effect
S/D	Source/Drain
SIA	Semiconductor Industry Association
SIMOX	Separation Implantation of OXygen
SNM	Static Noise Margins
SOS	Silicon on Sapphire
SRAM	Static Random Access Memory
SS	Sub-threshold Slope
TB SOI	Thin Body Silicon on Insulator

TCAD	Technology Computer Aided Design
UTB SOI	Ultra Thin Body Silicon on Insulator

Symbols

A_{vt}	Pelgrom coefficient/ mismatch coefficient
I_{on}	On-current
I_{off}	Leakage current
k	Boltzmann's constant
L_g	Gate length
L_{spa}	Spacer length
N_a	Doping concentration
N_{it}	Trapped charge density
N_{sub}	Substrate doping
R_{SD}	Access resistance
Si	Silicon
SiO_2	Silicon dioxide
SiON	Silicon oxynitride
t_{ox}	Gate dielectric thickness
T	Temperature
T_{BOX}	Buried oxide thickness
TiN	Titanium nitride
T_{Si}	Silicon body thickness
V_b	Substrate bias

V_{dd}	Supply voltage
V_{ds}	Drain voltage
V_{th}	Threshold voltage
w_f	Work function
X_j	Junction depth
α	Scaling factor
ε	Electric field
σ	Source/Drain doping abruptness
μ	Carrier mobility
Δ	RMS amplitude
Λ	Correlation length
$\varnothing$	Grain diameter
σV_{th}	Threshold voltage standard deviation
σI_{on}	On-current standard deviation
σDIBL	DIBL standard deviation
$<V_{th}>$	Average threshold voltage
$<I_{on}>$	Average on-current
<DIBL>	Average DIBL

CHAPTER 1

Introduction

1.1 Motivation

The inventions of first transistor and integrated circuit (IC) have opened up a successful path for a broad range of micro and nano electronic applications. Until now, the technology scaling captured by the famous Moore's law has been the drive force behind the enormous success of the semiconductor industry. The planar bulk CMOS technology has been the work-horse of the semiconductor industry for over 40 years. However, the conventional planar bulk MOSFET is approaching the limits of scaling. Among the critical problems of conventional bulk-MOSFET scaling are the short channel effect (SCE). Very high channel doping concentration and extremely thin gate oxide are needed to control electrostatic integrity, which results in the degradation on channel mobility and gate leakage performance. In the same time, further transistor scaling dramatically increases the statistical variability resulting from the discreteness of charge and granularity nature of matter. The dominant source of statistical variability

are the random discrete dopants from heavily doped channel region, which unavoidably introduce huge variation in the bulk transistor electrical characteristics.

The high statistical variability introduces significant complications in the design of circuit and system, limiting the overall yield and performance in nanoscale CMOS applications. Since the planar bulk-MOSFET scaling may not deliver the expected benefits beyond the 28nm CMOS, new device architectures are needed in order to enable the benefits of scaling for future generations. Significant efforts have been invested in inventing and developing new device structures to overcome the limitations of planar bulk technology scaling. It is expected by the International Technology Roadmap Semiconductor (ITRS) that bulk-MOSFET will be succeeded by Ultra Thin Body Silicon on Insulator (UTB SOI) transistors. This is due to the fact that, the UTBSOI architectures can tolerate very low channel doping concentration due to much improved electrostatic integrity, and as a result, the variability that originates from random dopants (RDF) could be dramatically reduced. In addition, simultaneously the buried oxide in the SOI substrate can reduce the junction capacitance, which results in faster switching and signal propagation. However, there are other variability sources that are becoming important in UTB SOI devices including the line edge roughness (LER) and the metal gate granularity (MGG). Therefore it is very urgent to investigate the impact of different variability sources on the characteristics of properly scaled UTB SOI transistors. Throughout this study, fully depleted ultra thin body silicon on insulator (FD-UTB SOI) transistors are designed on the impact of the statistical variability thoroughly investigated.

1.2 Aim and Objectives

The aim of this research is to study the realistic scaling of advanced fully depleted ultra thin body silicon on insulator (FD-UTB SOI) MOSFETs and their statistical variability and reliability. This aim can be accomplished by the following objectives:

1. To design realistic highly scaled FD-UTB SOI transistors corresponding to advanced technology generations.

    - Design study of 22 nm FD-UTB SOI MOSFET
        - device structure design based on ITRS specification.
        - buried oxide (BOX) design, thick or thin BOX?
        - source/drain doping abruptness design : 2.0, 2.5 and 3.0 nm/dec.
        - spacer length design : simulation study of spacer length selection, trade-off/compromise between I_{on}, I_{off}, DIBL and SS for low power devices.
        - investigate the impact of substrate bias effects on device behaviour.

    - Scaling of single gate FD-UTB SOI MOSFET down to 16 nm and 11 nm gate lengths, follow the trends from design template of 22 nm technology generation.

2. To perform physical simulation with different sources of statistical variability such as RDF, LER, MGG; investigate the impact of statistical variability on threshold voltage (V_{th}), on-current (I_{on}) and drain induced barrier lowering (DIBL). The impact is analysed both individually and in combined sources.

    - RDF
    - LER – 2nm
    - MGG – average grain size is 5 nm

3. To carry out statistical reliability simulation on the designed devices. This includes the impact of trapped charge as a result of positive bias temperature instability (PBTI) of n-type FD-UTB SOI MOSFET.

    - Simulation with combined variability sources at different degradation levels '***without***' MGG. The trapped charge density are 1e 11 cm^{-2}, 5e 11 cm^{-2} and 1e 12 cm^{-2}.
    - Simulation with combined variability sources at different degradation levels '***with***' MGG. The same trapped charge density are employed, 1e 11 cm^{-2}, 5e 11 cm^{-2} and 1e 12 cm^{-2}.

1.3 Thesis Organization

This PhD thesis consists of seven chapters, and is organized as follows:

Chapter 1 describes the motivation, the aim and objectives of this PhD study, as well as thesis organization.

Chapter 2 begins with the scaling of conventional bulk-MOSFET, Moore's law and the ITRS. It describes the scaling concept of bulk-MOSFET such as constant field scaling and generalized field scaling rules. Several scaling challenges in terms of variability are also discussed in detail. The discussion expands to new device architectures that can replace the conventional bulk transistor. Finally, it reviews the ITRS projection in respect of FD-UTB SOI for next generations to look at possible future direction of this technology.

Chapter 3 focuses mainly on the simulation tools and methods used in this research. This includes the description of the 3D 'atomistic' device simulator GARAND, carrier transport, mobility models and finally the 'atomistic' simulation techniques.

Chapter 4 presents the scaling study of single gate FD-UTB SOI n-type MOSFET. It starts with the vigilant design exercise of 32nm thin body SOI MOSFET in the FP7 project PULLNANO. This starting device is then scaled down to 22nm gate length. Certain device parameters such as buried oxide thickness, source/drain doping abruptness and spacer length are optimized to achieve the performance according to the ITRS goals. Later, the scaling proceeds further to 16nm and 11nm physical gate lengths by following the same design procedures as for the 22nm template device.

Chapter 5 presents the predictive simulation study of statistical variability in the scaled FD-UTB SOI MOSFETs. The impact of the principle variability sources such as RDF, LER and MGG on V_{th}, I_{on} and DIBL for three technology generations is investigated. All variability sources are treated individually and in combination.

Chapter 6 presents the simulation study of statistical reliability in scaled FD-UTB SOI devices for 22 nm, 16 nm and 11 nm technology generations. The PBTI variability associated with trapped charge is simulated in conjunction with other variability sources (RDF,LER and MGG). The impact of combined variability sources at different trapped charge levels on V_{th}, I_{on} and DIBL is analysed. Under this study, two scenarios are considered; combined variability sources at different degradations '***without***' and '***with***' MGG.

Chapter 7 draws the conclusion of this research and outlines some directions for future research.

Figure 1.1 illustrates the main part of thesis contents, it covers from chapter 2 up to chapter 6. Chapter 1 and 7 comprise of introduction and conclusion respectively, which is not describe in this figure.

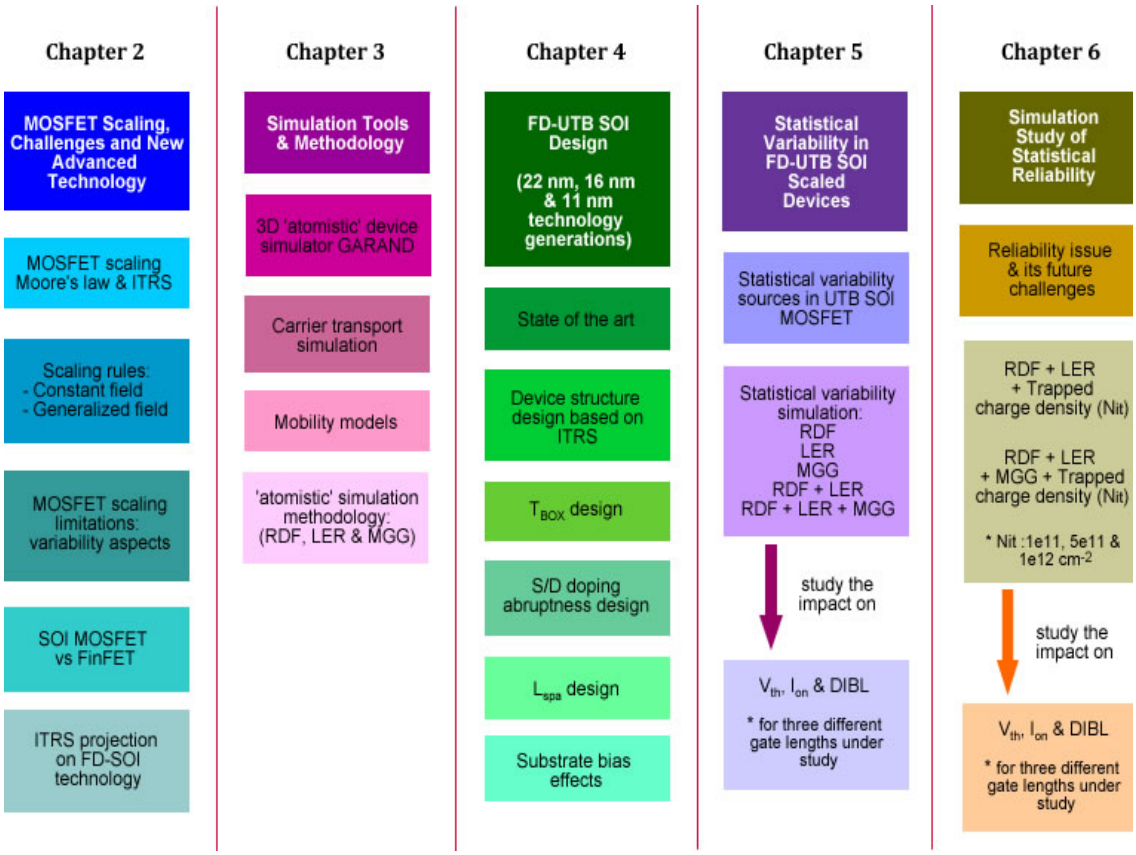


Figure 1.1: Main part of thesis organization

CHAPTER 2

MOSFET Scaling, Challenges and New Advanced Technology

2.1 Introduction

Since the beginning of the integrated circuit (IC) technology in 1959, the minimum feature gate length has been continuously reduced and the expectation is that the scaling of feature length will be continued in the foreseeable future. The reduction of device dimensions can increase the chip's density, lower the manufacturing cost, speed up the performance and lower the power consumption per functionality. As the metal oxide semiconductor field effect transistor (MOSFET) dimensions are reduced, the transistors need to be designed properly in order to reduce short channel effect (SCE) and to improve performance. Researchers in the semiconductor sector and academia race to propose new device architectures assisted by ITRS (International Technology Roadmap for Semiconductors) guidance in order to improve MOSFET scalability and performance and to allow the Moore's predictions to become a reality.

Moore's law describes a long-term trend in the history of the semiconductor industry in which the number of transistors that can be placed on an integrated circuit are increased exponentially doubling every year [1], resulting in more compact integration, upgraded performance and decreased cost per transistor. The law is named after Intel co-founder Gordon E. Moore, who introduced the concept in 1965. The Moore's law survived more than 40 years and has become the central driving force of semiconductor industry growth for a long period of time. This law has a significant impact on the electronics industry as a whole and continuously improves user applications in terms of increasing performance and functionality, as well as decreasing cost of the electronic devices.

In order to sustain the semiconductor industry growth, in 1992, the Semiconductor Industry Association (SIA) produced a document called the National Technology Roadmap for Semiconductors (NTRS) to provide 15 years outlook of semiconductor industry trends that provides guidelines in terms of equipment, material and provided clear target for research and technology development. After 7 years, in 1999, the first International Technology Roadmap for Semiconductors (ITRS) was born after a comprehensive revision of NTRS 1997, including a set of latest technology requirements, potential transitions and timing for semiconductor industry [2]. The purpose of the ITRS is to ensure advancements in the performance of integrated circuits and to remove any barriers to the continuation of Moore's Law journey. The ITRS efforts and assessment is a joint venture of global industry manufacturers and suppliers, government organizations, consortia and universities. They work together to ensure that the Moore's law remains alive. Every year, the ITRS identifies the technological challenges and needs facing the semiconductor industry over the next 15 - 16 years. The latest edition (ITRS 2011)[ø] shows the targets and requirements as a challenge to the CMOS technology in maintaining the Moore's law. In fact, the Moore's law and the ITRS strongly complement each other.

[ø] The ITRS 2011 has been published during the '**end**' of this study

2.2 Past Scaling Trends and Rules

The integrated circuits miniaturization is referred to as scaling down of the transistor size, aiming to achieve high speed, high density and multi functionality. The best possible scenario to the device scaling is to reduce all device dimensions and supply voltage while maintaining constant internal electric field. This requirement is very important to avoid SCE. Device scaling not only involves geometry parameter reduction, but also significantly influences the device electrical characteristics. Therefore appropriate scaling rules must be employed in order to mitigate SCE that degrade the transistor performance. Figure 2.1 illustrates the scaling concept of MOSFET transistor. They are two basic sets of scaling rules; the constant field scaling rule and the generalised scaling rule. Each of them will be discussed in the next sub-section.

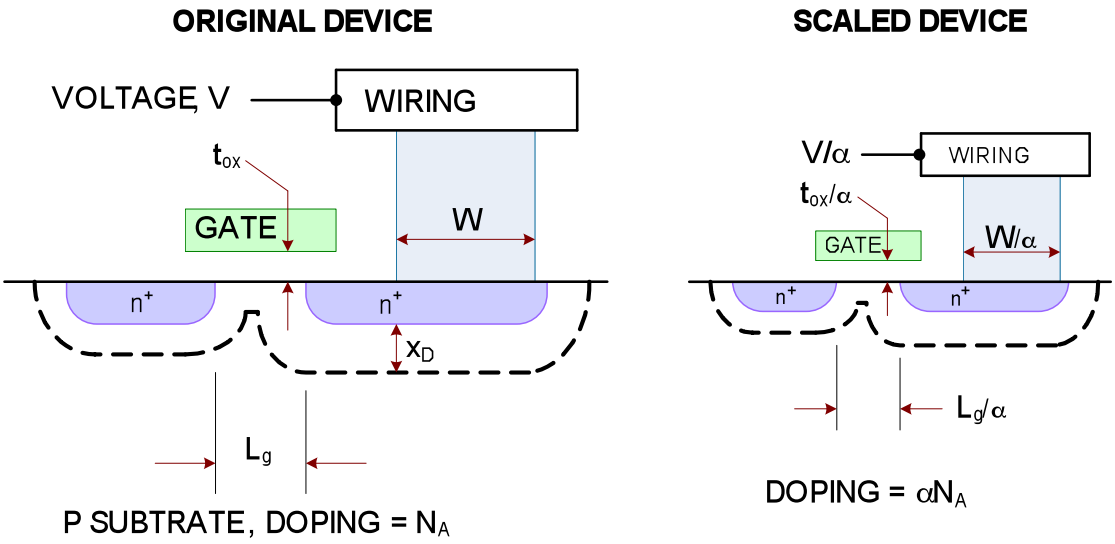


Figure 2.1: Illustration of past scaling concept of bulk-MOSFET transistor by a factor α. Redraw from [3].

2.2.1 Constant field scaling rule

The simple principles of scaling of a MOS transistor formulated by R.H. Dennard [4, 5] and aiming to enhance the performance of MOSFET, stipulate that the supply voltage and the transistor size must be reduced linearly. In the same time the doping concentration needs to be increased to allow the electric field to remain constant. This method should preserve the field in the transistor unchanged. The design parameters of the device will be scaled by the same scaling factor, α. The scaled down device will have a reduced supply voltage (V_{dd}/α), gate length or horizontal dimension (L_g/α), vertical dimensions (oxide thickness, t_{ox}/α and junction depth, X_j/α) and an increased doping concentration (αN_a). Since the dimensions and supply voltage are scaled by the same ratio, the intensity of the electric field remain unchanged and assures that the reliability of new scaled device is not worse than the original device.

2.2.2 Generalized field scaling rule

Due to the non-scaling effect of sub-threshold slope, the supply voltage can hardly be scaled in proportion to the channel length, and as a result, the electric field in the transistor has been increasing during the scaling down of the transistors over the years. In order to allow both vertical and lateral electric fields to change with the same multiplication factor so that the shape of electric pattern is preserved, a generalized scaling rule was proposed by Baccarani *et* al. [6] in 1984. In the generalized scaling rule, the physical dimensions of the transistor are still reduced by a factor α but the supply voltage and the doping concentration are scaled by ε/α and $\varepsilon\alpha$ respectively. The critical issue arises in the generalized scaling approach is the increase of the power density (Power/Area) by a factor of ε^2. This leads to challenges related to packaging and cooling in order to cope with the increasing power dissipation by the transistors on a chip. The list of physical parameters and scaling rules are presented in Table 2.1.

Table 2.1 : Device parameters and scaling rules [3].

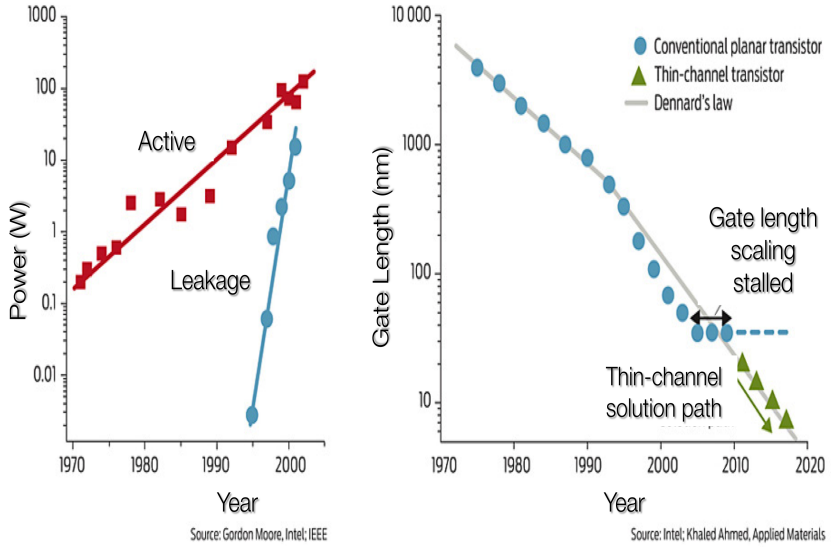
Physical parameters	***Constant*** field scaling rule	***Generalized*** field scaling rule	***Generalized selective*** scaling rule
Channel length, Insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
On-current per device	$1/\alpha$	ε/α	ε/α_w
Doping	α	$\varepsilon\alpha$	$\varepsilon\alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^2$
Capacity	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\alpha_w\alpha_d$
Power density (Power/Area)	**1**	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

* α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_d & α_w are separate dimensional scaling parameters for the selective issue. The α_d is applied to the device vertical dimensions and gate length, meanwhile the α_w applies to the device width and the wiring.

2.3 Limitations of MOSFET Scaling

The key driver of the enormous success of complementary metal oxide semiconductor (CMOS) technology is due to the scalability of the MOSFET transistor. However, when the CMOS technology entered deep submicron regime, the era of 'happy scaling' ended due to physical and technological limitations [7, 8]. The conventional scaling method to shrink horizontal (gate length) and vertical (gate dielectric thickness) device parameters as well as increase channel doping concentration are no longer practical and achievable. In addition, basic physical parameter such as kT and the related sub-threshold slope cannot be scaled. Scaling associated power crisis is becoming a major challenge for sustainability of the Moore's law. According to Figure 2.2 [9], the transistor leakage power that is approaching the active power required for switching the transistor state and carrying out digital computations, which is highly undesirable. This is eventually retarding already the transistors scaling pace, necessitating a solution to offer a second life to Moore's law. Therefore, new technology boosters including the channel and gate stack materials and new device architecture needed to achieve the performance requirements of the future CMOS technology generations, in association with device dimensions scaling have been adopted or are actively pursued in research [10].

Before we focus on the new possible alternative devices, it is imperative to identify the main obstacles affecting MOSFET scaling. The most critical issue that becomes a major focus of the MOSFET scaling is the short channel effect (SCE) due to the charge sharing in the channel of the short channel devices. When the gate length shrinks, there is a competition between the gate and source/drain regions over the control of the channel depletion region and the inversion layer charge due to the fact that the electrostatic control of source/drain regions has increased. An early description of the SCE and the charge sharing model can be found in [11].



(a) *(b)*

Figure 2.2 : Power crisis as the downsizing of transistor gate length.

a) The leakage power during off state quick approaching the active power for switching the transistor to the on state.
b) The leakage problem slow down the transistor scaling pace, thus alternative architectures are required.

The SCE leads to device degradation and reliability concern such as;

- Threshold voltage (V_{th}) roll-off - the dependence of V_{th} upon gate length, L_g.
- Increase of leakage current (I_{off}) and degradation of sub-threshold slope (SS) due to the loss control of the gate bias on the drain current.
- Drain induced barrier lowering (DIBL) due to the modulation of source/channel potential barrier by the drain voltage, where the V_{th} decreased with the increasing drain voltage.

In order to retain the strong gate control over the channel, further technological improvements are very important to ensure continuing benefits from device miniaturization. In MOSFET transistor, gate dielectric thickness (t_{ox}) is the most critical parameter and has been aggressively scaled until recently. The thin gate oxide can preserve good switching characteristics and can provide higher drive current at reduced

supply voltage, thus preventing the negative impact of the SCE. However, the aggressive scaling of the gate oxide has now reached fundamental physical limitation (1nm ≈ 4 atomic layer), due to the direct quantum mechanical gate tunneling between the gate electrode and channel. The parasitic leakage current due to gate tunneling can significantly contribute to the total leakage current and standby power dissipation [3, 12]. Therefore, the use of high-dielectric constant (high-k) gate dielectric in combination with metal gate electrode has been introduced as a promising option to boost the performance and sustain the scaling from 45 nm to 32 nm technology generation.

Figure 2.3 shows the gate dielectric transition from silicon dioxide (SiO_2) to high-k stack for different technology generations. The introduction of a high-k/metal gate stack at 45nm technology node [13] has resulted in a significant improvement in performance, reduction of leakage and variability [14, 15]. Figure 2.4 illustrates the migration from Poly/SiON to metal gate/high-k gate stack and the dependence of gate dielectric thickness and gate leakage on technology scaling.

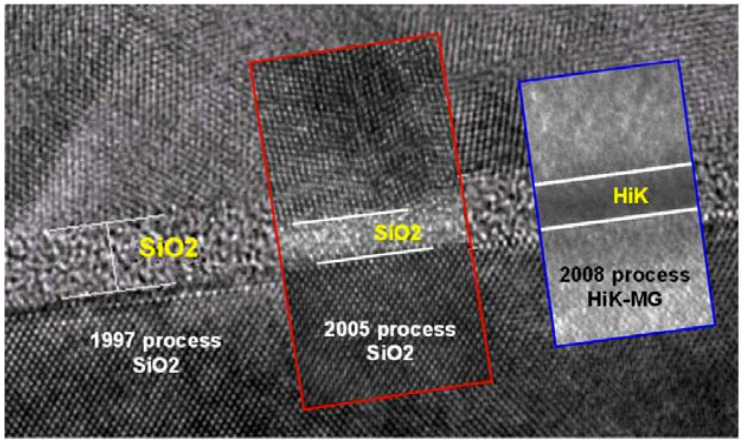


Figure 2.3 : Transition of gate dielectric material from SiO_2 to high-k for three different device gate length [16].

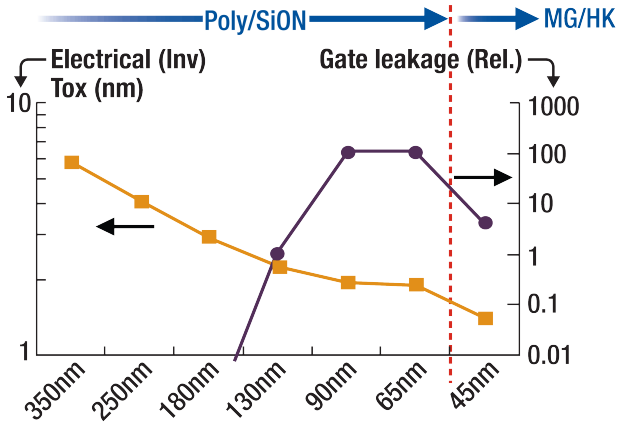


Figure 2.4 : Migration from Poly/SiON (Poly/Silicon Oxynitride) to metal gate/high-k (MG/HK) and the dependence of gate dielectric thickness and gate leakage on technology scaling [13].

Another issue related to MOSFET scaling is the very high channel doping concentration needed for controlling of SCE. The moderated doping density of approximately 2.5e16 cm^{-3} at Lg = 1 μm [4] has been increased to more than 2e18 cm^{-3} at Lg = 35 nm [17]. The reduction of gate length without heavy channel doping will result in accute threshold voltage roll-off and punch-through between source and drain. For sub-100 nm devices, halo/pocket implants and shallow source/drain junctions are used to block lateral field penetration (punch-through) and minimized the SCE without affecting the threshold voltage [18]. However, high channel doping concentration reduces carrier mobility due to impurity scattering [17], increases the sub-threshold slope and also introduces band-to-band tunneling.

On the top of SCE and leakage current limitations, the most challenging problems associated with scaling are the increasing statistical variations due to discreteness of charge and granularity of matter [19-21]. The main sources of intrinsic parameter fluctuation are random dopant fluctuation (RDF) [20, 21], line edge roughness of the gate (LER) [22, 23], metal gate granularity (MGG) [24, 25] and oxide thickness variations (OTV) [26]. It has been proven experimentally that the further scaling of bulk-MOSFET will introduce intolerable drain current and threshold voltage fluctuations and will dramatically degrade the circuit performance [27]. In the next section, the factors that impede the scaling of bulk-MOSFET in term of variability will be discussed.

2.4 Factors Impede the Scaling of Traditional Bulk MOSFET : Variability Aspects

In modern CMOS technology, the semiconductor industry aims to produce a high speed and low cost integrated circuits by shrinking the size of each transistor on a single chip. However, several limitations to scaling mark the end of 'happy scaling' era. These include the intrinsic parameter fluctuations (random dopant fluctuation-RDF, gate line edge roughness-LER, metal gate granularity-MGG and oxide thickness variation), the quantum mechanical effects (band to band tunnelling, direct gate oxide tunnelling and source to drain tunnelling), the degradation of carrier mobility, and the ever-increasing power dissipation. All the limitations and constraints are becoming more severe especially variability, and force the industry to shift the paradigm to new transistor structures and fabrication technologies which hopefully may tackle the limitations. Figure 2.5 shows the major challenges facing by the semiconductor industry in the 'late CMOS' phase, where new CMOS transistor architectures will be needed.

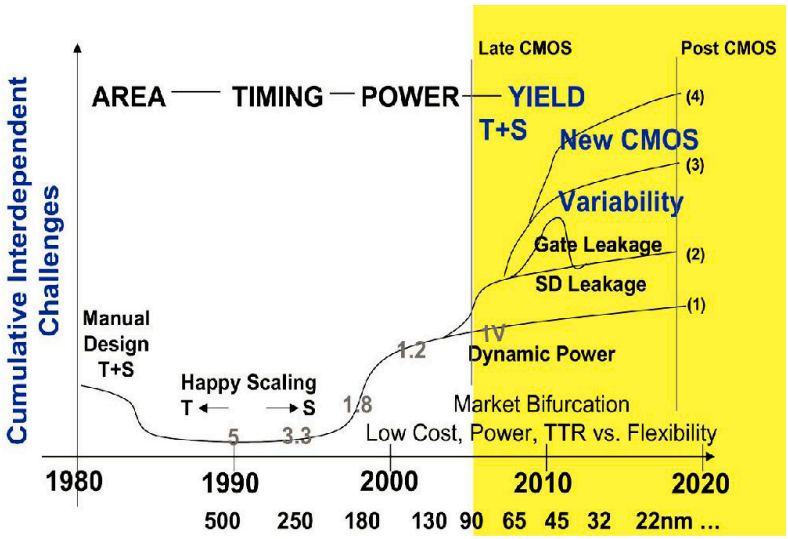
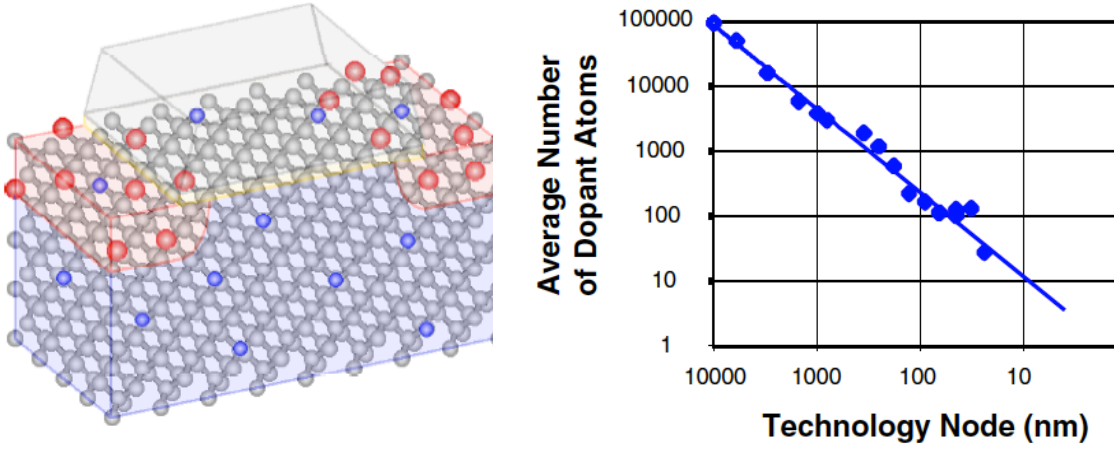


Figure 2.5 : Major challenges as a function of time and technology nodes [28].

It widely accepted that the statistical variability is a major concern for nanoscale CMOS technologies, hindering further device scaling and integration [14, 15, 29, 30]. Statistical variability is introduced by discreteness of charge and granularity of matter, which lead to significant fluctuations in the device characteristics.

Random dopant fluctuations (RDF) introduced by the ion implantation process and consequent activation and diffusion have became a dominant source of statistical variability in modern MOSFET technology [21, 31, 32]. During ion implantation process, the impurity atoms are implanted into the silicon with an adequate energy and activated using annealing in order to allow the impurity atoms to replace the silicon atoms in the lattice and to become activated. The combination of ion implantation and annealing causes random dopant distribution in every single device, leaving no two devices the same. RDF causes threshold voltage fluctuations due to the variation in dopant number and location [20, 21, 33, 34]. The magnitude of threshold voltage fluctuation becomes more pronounced in smaller gate length device due to the reduction in the number of discrete random dopants. This point is illustrated in Figure 2.6.



(a) (b)

Figure 2.6 : (a) Schematic of 4.2 nm MOSFET under the influence of RDF. Red/blue dots represent donor/acceptor dopants, while the grey dots are silicon crystalline lattice [35], (b) average number of dopant atoms versus technology generation [36].

Another important source of intrinsic parameter fluctuation (IPF) is LER, which related to the patterning of the gate edge by using photolithography. The LER is due to the variations of the molecular structure of the resist polymer material, resulting in non-uniformities of the resist edge. In the past, the LER impact was negligible because the transistor gate length and width are much bigger than the roughness, however, as the devices shrinks, the LER causes appreciable fluctuation in the local length of the channel along the width of the transistor [37]. Figure 2.7 illustrates an example of polymer aggregates for negative/positive resists, where the unexposed/exposed regions are removed.

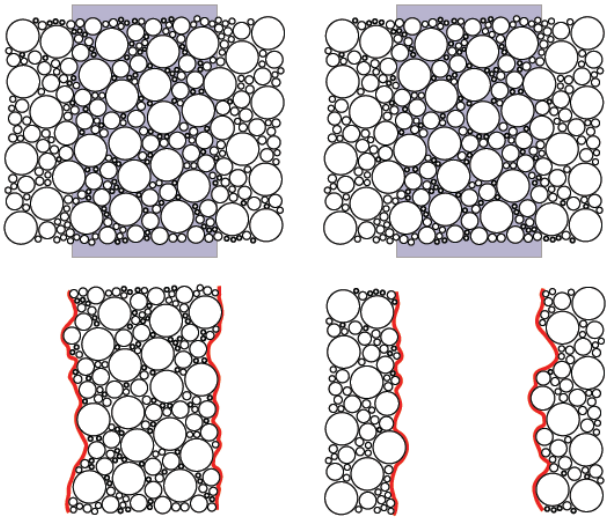


Figure 2.7 : Typical LER in photoresist when negative/positive resists are used [35].

Other possible statistical variability source is the metal gate granularity, which has been introduced when the technology moved to the higk-k gate dielectric materials at 45nm technology generation. The MGG is introduced by crystallization of the metal gate material during the high temperature annealing process leading to variation in the work function of the crystal grains in the metal gate [38]. This has became one of the major variability sources, affecting the transistor parameters distributions [15, 24, 25, 39, 40]. Figure 2.8 shows a typical metal grain pattern in a 35 nm gate length MOSFET with an average grain diameter of 10 nm and two different grain orientations.

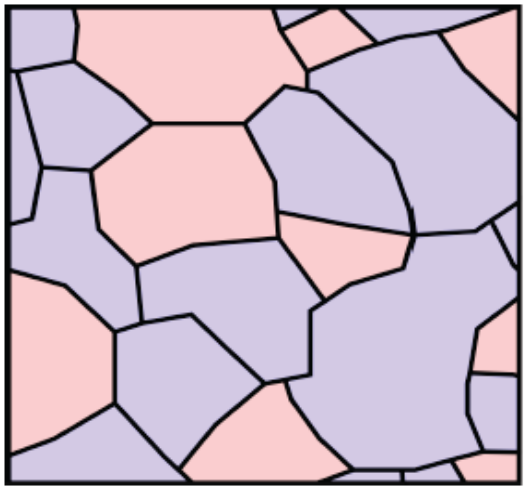


Figure 2.8 : Metal grain pattern of 35x35 nm gate with an average grain diameter of 10 nm [40].

Additionally, oxide thickness variations (OTV) is another source of IPF associated with the silicon/silicon dioxide surface roughness at the interface between silicon, silicon dioxide and poly gate in MOSFET transistor. Such atomic scale roughness causes potential variation across the channel and leads to threshold voltage fluctuation [26, 41, 42]. The effect is more severe in scaled devices. Apart from threshold voltage variation, fluctuation in gate tunnelling current [43] and mobility are also affected by OTV since each individual device microscopically has dissimilar surface roughness and oxide thickness pattern as shown in Figure 2.9.

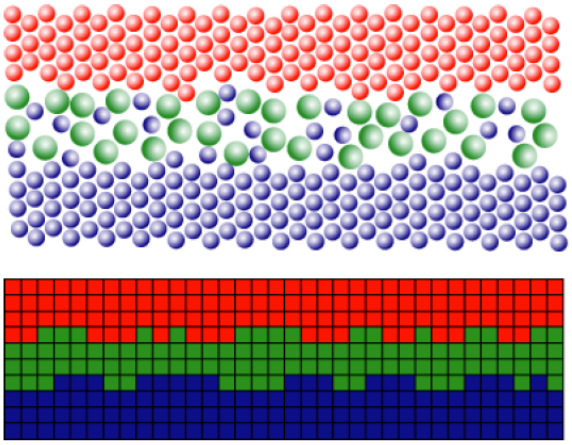


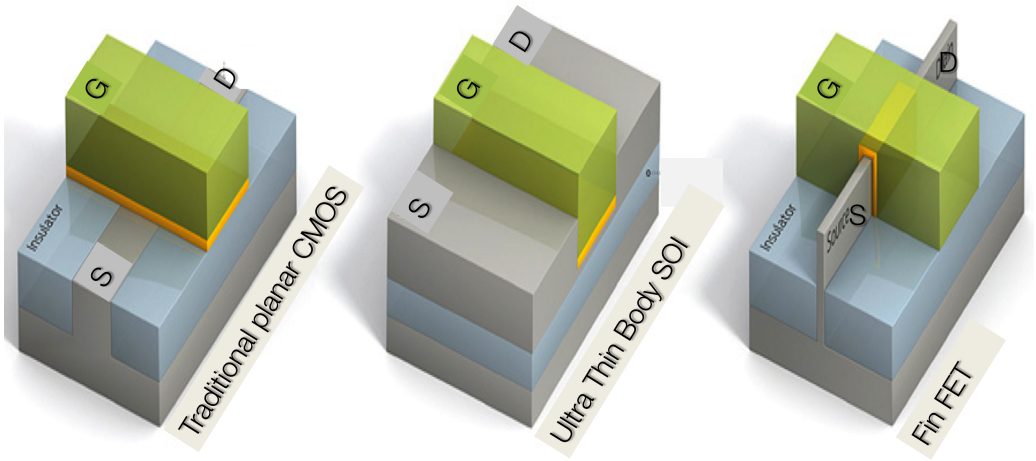
Figure 2.9 : Illustration of OTV impact at the interface of silicon/silicon dioxide and silicon dioxide/poly-si gate [35]. The Red, green and blue colors signify poly-si gate, silicon dioxide and silicon respectively.

Before the introduction of high-k/metal gate stack at 45 nm technology node, polycrystalline-silicon (poly-si) was used as the gate material. The poly-si granularity can result in large threshold voltage due to Fermi-level pinning at the grain boundaries at the poly-si/gate oxide interface [44] due to the high defect state densities [45].

All the principle sources of statistical variability described above can widen the threshold voltage distribution and degrading circuit and system performances of traditional bulk-MOSFET. This is related to the fact that, the progressive scaling of bulk-MOSFET needs a very high channel doping concentration to control SCE, leading to unacceptable high variability in threshold voltage due to the RDF [15, 46]. In this respect, new device architectures, materials and process steps should be introduced to allow further transistor miniaturization and mitigating the statistical variability introduced by RDF, although some of the other variability sources could still exist in new device architectures.

2.5 New Device Architectures: SOI MOSFET vs FinFETs

Scaling of traditional planar bulk-MOSFET is becoming more and more difficult in following the Moore's law in advanced technology nodes. The main detrimental effects are the difficult to control SCE and the increasing variability in the device characteristics. Therefore, there is a consensus among the semiconductor industry experts that introduction of new device architectures at nonometer regime is mandatory. The essence behind the invention of novel device structure is to maximize the control of gate terminal over the channel and minimize the impact of statistical variability on the device characteristics. Figure 2.10 shows an evolution of transistor structures that enable the continuing scaling down to a shorter gate length. A migration from conventional bulk-MOSFET to planar ultra thin body SOI (UTB SOI) and tri-dimensional FinFET is envisaged. The concept of both new structures is to improve the gate control and reduce the statistical variability.



(a) (b) (c)

Figure 2.10 : Transition of field effect transistor (FET) transistor to proceed further scaling, (a) bulk-MOSFET, (b) ultra thin body silicon on insulator (UTB SOI) and (c) FinFET [9].

2.5.1 FD-UTB SOI

From a design point of view, the fully-depleted UTB SOI [47] (FD-UTB SOI) and FinFET [48] are very different device architectures. The planar FD-UTB SOI is built with a thin layer of crystalline silicon on top of an insulating layer (BOX). In FD-UTB SOI device, the SCEs are controlled by the silicon body thickness [49]. To acquire high performance, low sub-threshold slope and acceptable DIBL, the SCE can be controlled by the ratio of the gate length to the body thickness which should remain larger than four, $L_{gate}/T_{Si} \geq 4$ [50].

The FD-UTB SOI transistors have demonstrated promising device performance, well controlled access resistance and significant reduction in statistical variability that originates from random dopant fluctuation (RDF), allowing the implementation of undoped channel. This leads to excellent matching performance [14, 51] and boosts carrier mobility. In addition, to excellent electrostatic integrity, improved scalability, and reduced DIBL, the UTB SOI also eliminates submerged leakage paths due to its ultra thin body structure. Since the manufacturing of the FD-UTB SOI transistors is relatively simple compared to the manufacturing of non-planar device, FD-UTB SOI offers advantages in terms of compatibility with planar CMOS processing and integration. As a result, the corresponding circuits can reach the market faster.

Another feature that makes planar device more attractive are the back-biasing capabilities [52-55]. This attribute is very useful for low power and low standby power applications. With the application of back-bias, the threshold voltage (multiple V_{th}) and on/off current are easily tuned to meet design target [52, 56]. Simultaneously, performance enhancement can be achieved by applying forward back gate bias.

Simultaneously the optimization the '*SmartCut*' SOI wafer technology (pioneered by Soitec) was able to provide the wafer uniformity LTTV (layer total thickness variation) of +/- 0.5nm, which is in accordance with the FD-UTB SOI technology requirement [57]. Besides, most of the mobility enhancement technique can be applied to FD-UTB SOI to boost an extra performance [58, 59]. This is very important since the externally induced-stress (tensile/compressive liners; *t-CESL*/*c-CESL*) will be reduced with the reduction of the gate pitch as the gate length shrinks [60]. Furthermore, it has been

reported that FD-UTB SOI delivers currently the smallest V_{th} variation (A_{vt} -Pelgrom coefficient) [51, 61, 62] compared to the other devices with the same gate length.

2.5.2 FinFET

In the FinFETs the thin silicon channel is turned by 90° out of the flat surface creating a '*fin*' [63]. The FinFET's gate wraps the channel on all three sides of the fin. As a result, the gate have improved control over the channel, leading to superior SCE control and better sub-threshold slope. The relatively large channel volume gives major advantage to FinFET in carrying high current density. In the FinFET structure, the fin width is the most critical parameter because it determines the SCE. As the fin width increased, the leakage current also dramatically increased due to the poor gate control over the channel [49]. It is imperative to achieve good control of the fin width since it also affecting other critical parameters such as threshold voltage [64-66] and mobility [67]. A key design guidelines for FinFET, allowing adequate reduction of the SCE, the fin width should be approximately one half of the gate length [48, 49].

It is widely accepted that the FinFET is the best structure for improving electrostatic integrity, achieving higher drive current and speed, small DIBL [68] and ideal sub-threshold slope (~ 60 mV/dec). Intel been first in introducing 3D Tri-Gate FinFET technology at 22 nm CMOS technology in their high end microprocessor *Ivy Bridge* with high volume of production starting in June 2012 [69]. However, from manufacturing standpoint, the FinFET is quite complicated and challenging because the fin definition must be narrow and uniform, with uniform gate dielectric on all sides and at the corners. In the FinFET manufacturing, all sources of process induced variations should be under control (on the few atomic layer scale) in order to achieve the promised benefit of the FinFETs. Furthermore, the FinFETs are very sensitive to fin line width and line edge roughness, which leads to threshold voltage fluctuation [64, 70]. In principle, the essential FinFET geometry introduces many edges and boundaries, therefore it unavoidably susceptible to extra parasitic coupling and substantial variations.

It is early to anticipate which device will be a winner in future applications with both FD-SOI MOSFETs and FinFETs having specific advantages and disadvantages. Certainly, both have the potential of taking over the bulk-MOSFET dominant position in future technology generations. Those in needs of high speed and high performance transistors nominate FinFET, meanwhile, others who are interested in low power mobile applications will find the FD-UTB SOI most desirable. On the whole, planar FD-UTB SOI has the potential of keeping the Moore's alive in low power and hand-held applications.

2.6 ITRS Projection on Fully Depleted SOI for Next Generation

Due to the physical limitations of the traditional planar bulk-MOSFET scaling, several options have been brought forward in the ITRS to extend the life of the transistor scaling. The emerging device technology has been added in the ITRS in order to improve device performance and replace the existing bulk-MOSFET via the introduction of multiple gates FET (e.g., FinFET) and SOI MOSFET (e.g., UTB-FD). It is foreseen by the ITRS that bulk-MOSFET will be superseded by UTB-FD at 22 nm gate length, while the multiple gate is expected to be introduced at 17 nm gate length, targeting low operating power technology [12].

This work concentrates on planar SOI MOSFET technology and is based on the ITRS 2009 edition. Therefore in Table 2.2 we present the ITRS 2009 projection for certain critical parameters relevant to UTB-FD MOSFETs for low power operation.

Table 2.2 : The long term year (2010-2024) projections of some critical parameters for UTB-FD, low power operation [12].

(Extracted from process integration, devices and structures (PIDS) document)

Year of Production	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024
Lg: Physical Lg for LOP logic (nm)	**29**	**27**	**24**	**22**	**18**	**17**	**15.3**	**14**	**12.8**	**11.7**	**10.7**	**9.7**	**8.9**	**8.1**	**7.4**
Equivalent Oxide Thickness, EOT (nm)				**0.9**	**0.85**	**0.8**	**0.75**	**0.7**							
Body Thickness, Tsi (nm)				**7**	**6.2**	**6.0**	**5.1**	**4.7**							
Power Supply Voltage, Vdd (V)	**0.95**	**0.85**	**0.85**	**0.8**	**0.8**	**0.75**	**0.75**	**0.7**	**0.7**	**0.65**	**0.65**	**0.6**	**0.6**	**0.6**	**0.6**
Saturation Threshold Voltage, $V_{t,sat}$ (mV)				**311**	**317**	**320**	**323**	**327**							

Legends :

	Manufacturable solutions exist, and are being optimized
	Manufacturable solutions are known
	Manufacturable solutions are NOT known
	Delineate one of two time periods; before initial production of UTB-FD or MG MOSFETs, or when planar bulk or UTB-FD MOSFETs have reached the limits of scaling.

Table 2.2 summarised physical gate length, equivalent oxide thickness (EOT), body thickness, power supply voltage and saturation threshold voltage of the future generations UTB-FD SOI MOSFETs. A manifestation of the tough challenges due to the scaling is the gate length reduction has been slowed down of 1-3 years compared to the previous roadmap predictions. Parallel to the diversification of the device scaling, the gate stack engineering including combination of metal gate electrode and high-k gate insulator has been applied in recent technology generation for suppressing direct tunnelling current through ultra thin gate oxides (atomic layer scale), increasing the gate capacitance and scaling down the equivalent oxide thickness (EOT). The gate stack normally includes an interfacial layer (SiO_2) between high-k dielectric and silicon material in order to achieve better interface quality and attain higher mobility. The ratio of high-k and silicon dioxide thickness need to be seriously considered to avoid reliability and mobility degradation problems.

The body thickness parameter has been added in ITRS 2009 in line with the introduction of new device structures to replace bulk-MOSFET at 22nm gate length and beyond. The body thickness in UTB-FD transistor is an important design parameter controlling the short channel effects. This parameter becomes more critical below 10 nm, therefore the effect of surface scattering and quantum confinement need to be well understood because the electrical performances of these devices are immensely sensitive to the body thickness variations.

The increase of the static leakage power is one of the main power constraints in the nano scale transistors. The static power dissipation grows due to the significant increase in the leakage current as the gate length shrinks down. When dealing with the power to achieve scaling is more difficult compared to the other parameters because the supply voltage cannot be reduced as easy as other device dimensions due to the non-scaling properties of threshold voltage and sub-threshold slope. As scaling continues beyond 22 nm technology, the power supply voltage scaling has practically slowed, with the saturation threshold voltage about 0.3V. Therefore, managing the power dissipation while maintaining the device performance is extremely important even though it is truly complicated.

2.7 Summary

This chapter presents the challenges in the scaling of the traditional MOSFETs and the corresponding technology innovations. It also describes how the MOSFET scaling, Moore's law and ITRS are closely interrelated. Two types of scaling rule including constant field and generalized field were explained clearly. The factors that restrict the bulk-MOSFET scaling have been discussed in depth. Since statistical variability is becoming one of the crucial scaling limitation factors, the factors that introduce statistical variability have been elaborated. Two novel device architectures; UTB-FD SOI MOSFET and FinFET are introduced and discussed in detail in terms of future technology and circuit applications. Finally, the ITRS projection for UTB-FD SOI MOSFETs for the next technology generations was discussed. UTB-FD SOI MOSFETs that offer record reduction of the statistical variability have been selected as a subject of further scaling and variability studies in this thesis.

CHAPTER 3

Simulation Tools and Methodology

3.1 Introduction

Microelectronics industry has grown rapidly and played a crucial role in the advancement of the semiconductor technology to its present stage. New product development and design of advanced technologies needs state of the art TCAD tools. With technology nodes entering into sub-20nm regime, traditional bulk planar device scaling increasingly faces fundamental limitations more than ever as discussed in chapter 2. One of the major concerns among these limitations is the impact of statistical variability, arising from the discreteness of charge and matter, on device characteristics and electronics systems operation. This particular challenge requires variability resilient device architectures in order to keep the Moore's law going for few more technology generations. Moreover, an enormous amount of strategic design decisions are needed before a mature technology data are available for production. Therefore, the use of TCAD device simulation is essential at early technology development stage in order to

obtain accurate assessment of performance and practical advantage that the new device architectures can offer.

This chapter will discuss the main simulation tools and methodology adopted in this work, including a brief introduction to 'atomistic' device simulator GARAND and detail descriptions of related simulation technologies.

3.2 Device Simulation Techniques

Modelling and simulating of physical behavior and electrical characteristics of semiconductor devices are very crucial for in-depth understanding and exploration of device design and operations. Moreover, they allow reliable evaluation of important physical parameters and their potential impacts on device functionality during the design and optimization process of modern CMOS technologies.

As device geometry continues to shrink, the 3D nature of device structure associated with the complex physics mechanism that governing nanoscale device operation makes it's difficult to assess device performance based on back-of-the-envelope analysis approach. The 3D TCAD device simulation is necessary to correctly understand the device operation. There are various useful numerical models and simulation tools, which have been utilized to analyze device behaviour in contemporary CMOS technologies. For example the drift-diffusion (DD) approach [71], the Hydrodynamic model [72], and the Monte-Carlo method [73] [74] [75] are the some of the major semiconductor device simulation techniques, which have been developed and evolved over the years. It is worth mentioning that some of the advanced simulation techniques are computational expensive and can overestimate or underestimate some important device parameters, for example drive current. Therefore the selection of appropriate technique is important based on the appreciation of its boundary and validity. In this study, DD approach is employed due to its' computational efficiency and flexibility in respect of current calibration.

3.2.1 The DD simulation approach

Since the 1970s, DD model have been instrumental in understanding and analyzing of semiconductor devices due to its efficiency in computing the current voltage characteristics of semiconductor devices.

There are three basic equations that are solved self-consistently in DD simulation in order to capture the behavior of the carrier transport in semiconductor devices. The Poisson's equation which characterizes the relationship between the electrostatic potential and the space charge, the current continuity equation encapsulating the charge conservation principle and the drift-diffusion current relation that takes into account both the drift and diffusion components of electron and hole flux density.

The classical Poisson's equation [76] [77] is formulated as follows;

$$\nabla\cdot\left(\nabla\psi\right)=-\frac{\rho}{\varepsilon_{si}} \tag{3.1}$$

where ε_{si} is the permittivity, ψ is the electrostatic potential and ρ is the charge density. The charge density ρ can further be expressed in terms of mobile and fixed charges as follows;

$$\nabla\cdot\left(\nabla\psi\right)=-\frac{q}{\varepsilon_{si}}\left[p-N_a^-+N_d^+-n\right] \tag{3.2}$$

where q is the charge, n and p are electron and hole concentrations, N_d^+ and N_a^- are density of ionized donors and acceptors respectively.

The second fundamental semiconductor equation is the current continuity equation that can be derived from the Maxwell's equations. It deals the charge conservation and with the time-dependent: generation and recombination mechanisms of electrons and holes. The current continuity equation is given by

$$\frac{\partial n}{\partial t}=\frac{1}{q}\nabla J_n-R_n+G_n \tag{3.3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla J_p - R_p + G_p \tag{3.4}$$

where R_n R_p are electron and hole recombination rates and G_n G_p are electron and hole generation rates respectively, whereas J_n and J_p are electron and hole current density terms combining drift current generated by the electric field and diffusion current due to the concentration gradients of the carriers. The J_n and J_p are the current density and can be expressed as in (3.5) and (3.6) below.

$$J_n = -qn\mu_n \nabla\psi + qD_n \nabla n \tag{3.5}$$

$$J_p = -qp\mu_p \nabla\psi - qD_p \nabla p \tag{3.6}$$

The μ_n and μ_p are electron and hole mobility, while D_n and D_p are the corresponding diffusion coefficients. The carrier diffusion coefficient and the mobility are connected through the Einstein relation when the system is close to thermal equilibrium or for non-degenerate semiconductors, $D = \mu\frac{kT}{q}$, where k, T and q are Boltzmann's constant, absolute temperature and single electron charge respectively. In summary, the Poisson's current continuity and drift-diffusion equations form a complete system of equations that describes the electrical behavior of a semiconductor device.

In the drift-diffusion simulation, the impact of statistical variability on carrier transport is not fully captured. In respect of threshold voltage, sub-threshold slope and DIBL variability, the selection of mobility model would not have a big influence on final simulation results, all extracted in the sub-threshold region of operation where the electrostatic impact of the variability sources dominate. In order to accurately capture the device on-current variation, Monte Carlo device simulation are needed, and the mobility parameters need to be calibrated against Monte Carlo simulation, as demonstrated in [78]. The approach in [78] could be adopted in future research to accurately capture the on-current variation in nano-scale FD-UTB SOI devices.

Quantum confinement becomes important in nano-scale device due to the thin EOT. There are two frequently used methods for including quantum correction in classical DD device simulation are the Density Gradient (DG) approach and the Effective Potential approach [79] [80]. In this work, the density gradient method is employed in DD simulation and further explanations can be found in [81].

3.2.2 Mobility models

Carrier mobility (μ) is one of the important parameters in semiconductor device that determine the device performance. High mobility leads to high drive current. Mobility in semiconductor devices is influenced by scattering mechanisms including ionized impurity scattering, lattice or phonon scattering and surface roughness scattering. Therefore, considering the major sources of scattering are essential, in order to achieve accurate estimation of carriers mobility. In the presence of multiple scattering mechanism the Mathiessen's rule [82] can be employed.

$$\frac{1}{\mu} = \frac{1}{\mu_{b1}} + \frac{1}{\mu_{b2}} + \ldots + \frac{1}{\mu_{s1}} + \frac{1}{\mu_{s2}} + \ldots \tag{3.7}$$

where (μ_{b1}, μ_{b2} , …) and (μ_{s1}, μ_{s2} , …) are different bulk and surface mobility contributions respectively.

The lattice or phonon scattering depends on the lattice temperature. At high temperature, phonon scattering increases resulting in carrier mobility degradation. In an undoped semiconductor, phonons associated with the vibrations of atoms in the crystal dominate the scattering and determine the mobility. The phonon scattering related mobility model is often presented in the form

$$\mu_{const} = \mu_L \left(\frac{T}{300K} \right)^{-\xi} \tag{3.8}$$

where μ_L is the mobility due to bulk phonon scattering and its value together with the exponent (ξ) are listed in Table 3.1.

Table 3.1 : Default values of phonon related constant mobility model for Silicon (Si).

Symbol (Unit)	Electrons	Holes
μ_L (cm^2/Vs)	1417	470.5
(1)	2.5	2.2

In doped semiconductors, ionized impurity scattering, from ionized donors and acceptors also degrades the carrier mobility. There are two main models, which are frequently deployed to simulate doping-dependent carriers mobility: the Masetti and Arora models. The Masetti model was proposed by Masetti et al. [83] and is expressed as

$$\mu_{dop} = \mu_{\min 1} \exp\left(-\frac{P_c}{N_{A,0}+N_{D,0}}\right) + \frac{\mu_{const} - \mu_{\min 2}}{1+\left(\left(N_{A,0}+N_{D,0}\right)/C_r\right)^{\alpha}} - \frac{\mu_1}{1+\left(C_s/\left(N_{A,0}+N_{D,0}\right)\right)^{\beta}} \qquad (3.9)$$

Typical values, which are used as a reference doping mobility (μ_{min1}, μ_{min2} and μ_1), doping concentrations (P_c, C_r and C_s) and exponential coefficients (α and β) are given in Table 3.2. The total acceptor and donor concentrations are assigned as $N_{A,0} + N_{D,0}$.

Table 3.2 : Masetti mobility model default parameters for silicon.

Symbol (Unit)	Electrons	Holes
μ_{min1} (cm^2/Vs)	52.2	44.9
μ_{min2} (cm^2/Vs)	52.2	0
μ_1 (cm^2/Vs)	43.4	29.0
P_c (cm^{-3})	0	9.23×10^{16}
C_r (cm^{-3})	9.68×10^{16}	2.23×10^{17}
C_s (cm^{-3})	3.34×10^{20}	6.10×10^{20}
α (1)	0.68	0.719
β (1)	2	2

A different doping-dependent mobility model was suggested by Arora et al. [84] and expressed as

$$\mu_{dop} = \mu_{\min} + \frac{\mu_d}{1+\left(\left(N_{A,0} + N_{D,0}\right)/N_0\right)^{A^*}} \tag{3.10}$$

where,

$$\mu_{\min} = A_{\min} \cdot \left(\frac{T}{300K}\right)^{\alpha_m} \quad , \quad \mu_d = A_d \cdot \left(\frac{T}{300K}\right)^{\alpha_d}$$

$$N_0 = A_N \cdot \left(\frac{T}{300K}\right)^{\alpha_N} \quad , \quad A^* = A_a \cdot \left(\frac{T}{300K}\right)^{\alpha_a}$$

Selected Arora model default parameters and coefficients for silicon are listed in Table 3.3.

Table 3.3 : Default values of Arora mobility model for silicon.

Symbol (Unit)	Electrons	Holes
A_{min} (cm^2/Vs)	88	54.3
α_m (1)	-0.57	-0.57
A_d (cm^2/Vs)	1252	407
α_d (1)	-2.33	-2.23
A_N (cm^{-3})	1.25×10^{17}	2.35×10^{17}
α_N (1)	2.4	2.4
A_a (1)	0.88	0.88
α_a (1)	-0.146	-0.146

In addition to mobility degradation in bulk, carrier mobility can be significantly affected at the interface regions due to the acoustic surface phonon scattering and surface roughness (interfacial defect) phenomena. These effects are related to the high perpendicular electric field in the channel region pushing carriers to interact intensely with the silicon-insulator interface. One of the models describing both type of mobility degradation is the enhanced Lombardi model which first proposed by Lombardi et al. [85] and for acoustic phonon scattering is formulated as

$$\mu_{ac} = \frac{B}{F_{\perp}} + \frac{C\left(\left(N_{A,0} + N_{D,0}\right)/N_0\right)^{\lambda}}{F_{\perp}^{1/3}\left(T/300K\right)^{k}} \tag{3.11}$$

For surface roughness scattering the formulation is

$$\mu_{sr} = \left(\frac{\left(F_{\perp}/F_{ref}\right)^{A^*}}{\delta} + \frac{F_{\perp}^{3}}{\eta} \right)^{-1} \tag{3.12}$$

where F_{ref} is a reference field of 1V/cm and $F_{\perp}$ is a perpendicular electric field normal to silicon-insulator interface. The exponent A^* is defined in [85] equal to 2 although , later works by Darwish et al. [86] has suggested an empirical formula for calculating the exponent A^* as in (3.13);

$$A^* = A + \frac{\alpha_{\perp}\left(n+p\right)N_{ref}^{v}}{\left(N_{A,0} + N_{D,0} + N_1\right)^{v}} \tag{3.13}$$

here, n and p are electron and hole concentrations respectively. The term N_{ref} denotes reference-doping concentration of 1 cm^{-3}.

Finally, all the scattering effects (surface mobility and bulk mobility) are incorporated by Mathiessen's rule as expressed in equation (3.7) and summarized as

$$\frac{1}{\mu} = \frac{1}{\mu_b} + \frac{D}{\mu_{ac}} + \frac{D}{\mu_{sr}} \qquad with, \quad D = \exp\frac{-x}{l_{crit}} \tag{3.14}$$

where x is defined as a distance from the interface and l_{crit} is a fitting parameter. The respective default values of Lombardi surface mobility model for silicon is shown in Table 3.4.

Table 3.4 : Default parameter values in Lombardi mobility model for silicon.

Symbol (Unit)	Electrons	Holes
B (cm/s)	4.75×10^{7}	9.925×10^{6}
C ($cm^{5/3}V^{-2/3}s^{-1}$)	5.80×10^{2}	2.947×10^{3}
N_0 (cm^{-3})	1	1
λ (1)	0.1250	0.0317
K (1)	1	1
δ (cm^2/Vs)	5.82×10^{14}	2.0546×10^{14}
A (1)	2	2
$\alpha_{\perp}$ (cm^3)	0	0
N_1 (cm^{-3})	1	1
v (1)	1	1
η ($V^2cm^{-1}s^{-1}$)	5.82×10^{30}	2.0546×10^{30}
l_{crit} (cm)	1×10^{-6}	1×10^{-6}

In the cases of high electric fields and velocity saturation, one has to take into account the high-field velocity saturation model which can employ different driving force model. Canali et al. proposed a model, which integrates temperature-dependent parameters [87] based on the Caughey-Thomas mobility model[88] to capture the velocity saturation effects. The proposed Canali model is given by the following equation;

$$\mu(F) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1+\left(\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{3.15}$$

where μ_{low} is the low field mobility and the exponent β is temperature-dependent term, which is defined as $\beta = \beta_0 \left(\frac{T}{300K}\right)^{\beta_{\exp}}$. The velocity saturation (v_{sat}) and the driving force (F_{hfs}) are given in equation (3.16) and (3.17) respectively.

$$v_{sat} = v_{sat,0}\left(\frac{300K}{T}\right)^{v_{sat,\exp}} \tag{3.16}$$

$$F_{hfs,\,n/p} = \left|\nabla \Phi_{n/p}\right| \tag{3.17}$$

where $\Phi_{n/p}$ represent electron and hole quasi-Fermi potential. The details of default coefficients of Canali model for silicon material is listed in Table 3.5.

Table 3.5 : Default parameters of Canali model for silicon (high-field mobility).

Symbol (Unit)	Electrons	Holes
β_0 (1)	1.109	1.213
β_{exp} (1)	0.66	0.17
α (1)	0	0
$v_{sat,\,0}$ (cm/s)	$1.07\text{x}10^7$	$8.37\text{x}10^6$
$v_{sat,\,exp}$ (1)	0.87	0.52

3.3 The 3D 'Atomistic' Simulator, GARAND

The 3D 'atomistic' device simulator, GARAND, has been developed over the years in the Device Modelling Group at the University of Glasgow. It is well calibrated against the experimental data and commercial CAD tools as extensively discussed in [89], [90]. It has been used as a vital tool to perform research studies producing numerous scientific publications [21, 31, 33]. This well-established simulator [91] is based on the drift diffusion approach to solve self-consistently the Poisson and the current continuity equations with a density gradient quantum corrections.

GARAND has been employed extensively to explore the impact of intrinsic parameter fluctuations (IPF) [34] [92] [93] on wide range of devices, spanning from traditional bulk-MOSFET to alternative device architectures, such as SOI and FinFET. In this research, three main sources of IPF are considered, namely random dopant fluctuation (RDF), gate line edge roughness (LER) and metal gate granularity (MGG). Statistics based predictive analysis of these sources of variability and their adverse impact on the transistor parameters is of great importance from both device and circuit design perspective. In order to analyze the impact of individual sources of variability, and their combined effect on device characteristics, all sources should be properly introduced into the device simulator. Without going into detail, the simulation methodology for each variability source is briefly discussed in the next sub-sections.

3.3.1 Random Dopant Fluctuation (RDF)

The Random Dopant Fluctuation (RDF) is associated with the discrete nature of the dopant atoms and their position in the crystal lattice. The doping profiles in modern CMOS technology are increasingly complicated. The impurity atoms are introduced using an ion implantation process by applying an adequate energy to penetrate into the silicon substrate to form the required region type or profile. The annealing process is used to allow the implanted atoms to replace silicon atom in the silicon lattice in order to become active. During the process of introducing doping atoms, a series of random collisions occur until they will come to rest state, thus resulting in random positions of

the individual discrete dopants in the active region of the device. The granularity of charge and the stochastic nature of discrete dopants adversely affect the electrical characteristics from one device to another, thus ultimately introducing significant variability in the device performance.

In ultra thin body silicon on insulator (UTB SOI) device, the RDF impact is reduced due to very low doping concentration in the channel compared to the conventional bulk-MOSFETs. However, the presence of random discrete dopants in the source and drain regions still result in effective channel length variation as well as in changes of the access resistance, both leading to drive current fluctuations.

The most realistic method of introducing the random doping distribution into an "atomistic" simulator would be the output from a Monte Carlo process simulation [89]. However this would be forbiddingly computational expensive for large scale statistical study. In this work RDF is implemented using a rejection technique, where the dopants are placed randomly in the source/drain and in the channel regions based on the initial continuous doping distribution obtained from continous process simulation. In this technique, the probability that there is dopant in a given discretization cell of the 3D simulation domain is computed according to equation (3.18);

$$\rho = \left(dx * dy * dz\right) N_D \tag{3.18}$$

here, ρ is the probability of charge being assigned, dx,dy and dz are the x, y and z components of the mesh cell respectively and N_D is the local doping concentration associated with the mesh node. If the generated random number is less than the calculated probability from equation (3.18), then the dopant would be allocated in the lattice site. This method is simple and widely used especially to introduce RDF into semiconductor device models for simulation of statistical variability effects in nano-scale MOSFETs. [21, 32].

Figure 3.1 presents the full 3D view of the electrostatic potential due to random dopant fluctuation in 22nm FD-UTB SOI transistor.

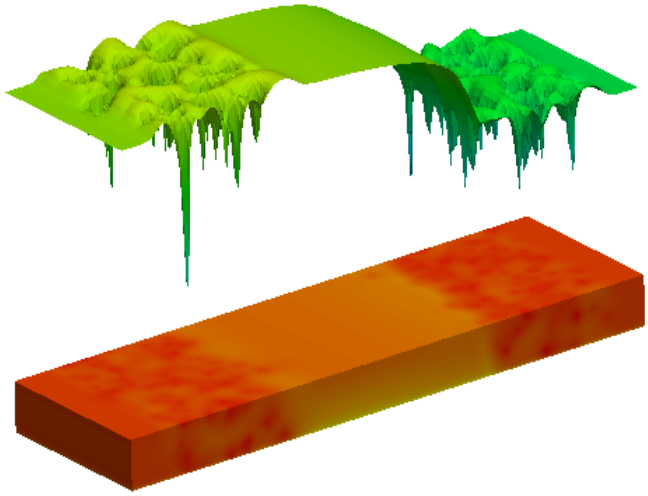


Figure 3.1 : The electron distribution in the silicon body subjected to RDF in 22nm FD-UTB SOI nMOSFET with the surface potential shown above.

3.3.2 Line Edge Roughness (LER)

Gate Line Edge Roughness (LER) is one of the undesirable random variations that becomes more severe as the device dimensions are scaled below 50nm [94], resulting in effective channel length variation. This phenomenon cannot be understated as it leads to serious device parameter fluctuations. As a result, LER has to be analyzed in order to evaluate the impact of LER on device performance, specifically on drive current and threshold voltage fluctuations, which are strongly influenced by LER as the gate length shrinks. Figure 3.2 (a) and (b) illustrate the line edge roughness effect due to polymer aggregate that develop within the resist material.

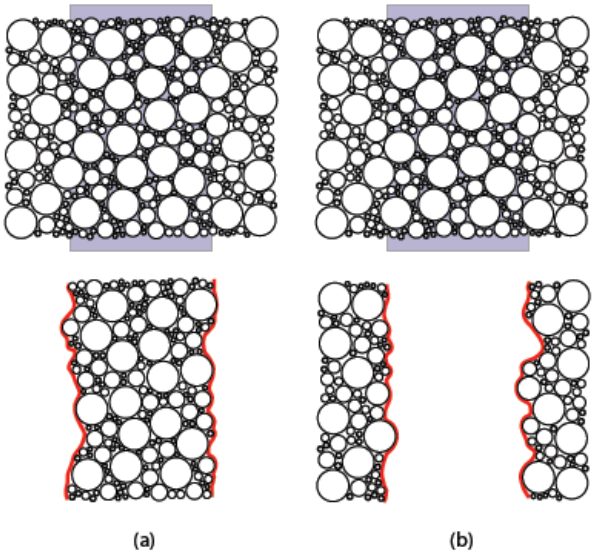


Figure 3.2 : The impact of line edge under different resist flavors (a) the effect of a negative resist removing the region that is unexposed and (b) the effect of a positive resist where the exposed region is removed away [35].

LER is characterized by two important parameters called rms amplitude (Δ) and correlation length (Λ). To implement LER into the device simulator, the gate edge is generated based on 1D Fourier synthesis method corresponding to power spectrum of a Gaussian or exponential autocorrelation functions. Details analysis on how LER is implemented into atomistic device simulator can be found in [94, 95]. The power spectra for Gaussian and exponential autocorrelation functions are based on the following equations and determine the amplitude of complex array;

$$S_G(k) = \sqrt{\pi}\ \Delta^2\ \Lambda e^{-\left(k^2\Lambda^2/4\right)} \tag{3.19}$$

$$S_E(k) = \frac{2\Delta^2\Lambda}{1+k^2\Lambda^2} \tag{3.20}$$

where $k = i\left(2\pi/N\,dx\right)$, dx is the discrete spacing used for the line and $0 \le i \le N/2$. Note that, the value quoted as LER is customarily defined to be 3 times the *rms* amplitude or $3\,\Delta$. Lines generated from Gaussian autocorrelation function are smoother than the lines

generated by exponential one. This is mainly due to the lack of high frequency components that are characteristic of the corresponding exponential power spectrum.

In Figure 3.3, the impact of LER on one of the simulated SOI devices is shown clearly, by considering 3σ = 2nm and the correlation length (Λ) of 25nm.

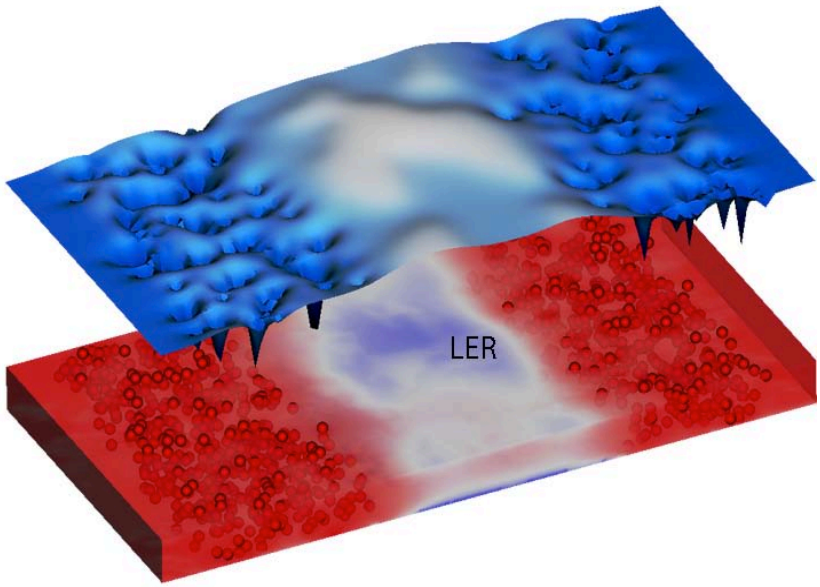


Figure 3.3 : The electron distribution in the silicon body showing the impact of LER (2nm) in 22nm FD-UTB SOI nMOSFET with the surface potential shown above.

3.3.3 Metal Gate Granularity (MGG)

The metal gate has become an important asset for the advanced technology nodes in order to realize 'small and yet efficient' transistor. The world's largest semiconductor chips maker, Intel announced the use of high-k technology at 45nm technology generation [13]. The introduction of high-k/metal gate stack is considered as remedy to reduce the gate leakage due to direct tunneling through silicon/silicon dioxide (Si/SiO_2) interface. In addition to this advantage, the use of metal gate eliminates the poly-silicon gate depletion effect, resulting in the reduction of the equivalent oxide thickness, hence helps to partially suppress the variability [13]. However, polycrystalline nature of metal gate materials introduces a new source of statistical variability [96, 97], known as metal gate granularity (MGG).

The method used to introduce a random grain pattern into the gate of the simulated device is similar to the procedure used by previously to the study the effects of poly-silicon granularity. The method is described in detail in [24]. An image of grain patterns in a large area is used as a template and small portion of this image is chosen randomly and transferred to the corresponding device gate area. Then, each grain is identified and work-function (W_f) is assigned according to the probability of each possible grain orientation for a given material.

Table 3.6 presents the summary of grain orientation, probability of occurrence and corresponding W_f [97]. For this work TiN is considered as a gate material. As described in Table 3.6, TiN has two grain orientations with a probability of 60% and 40% having the W_f of 4.6 eV and 4.4 eV respectively. This will give the W_f difference of TiN metal gate of 0.2 eV between the two orientations. A typical electrostatic potential profile of TB SOI device with MGG as the variability source is illustrated in Figure 3.4. The average grain diameter (∅) of 5nm is considered for this particular simulation. Figure 3.5, on the other hand, illustrates the electrostatic potential profile of a device with combined variability sources - RDF, LER and MGG.

Table 3.6 : Grain orientations with corresponding probability and work-function for TiN.

Orientation	Probability	W_f (eV)
⟨200⟩	60%	4.6
⟨111⟩	40%	4.4

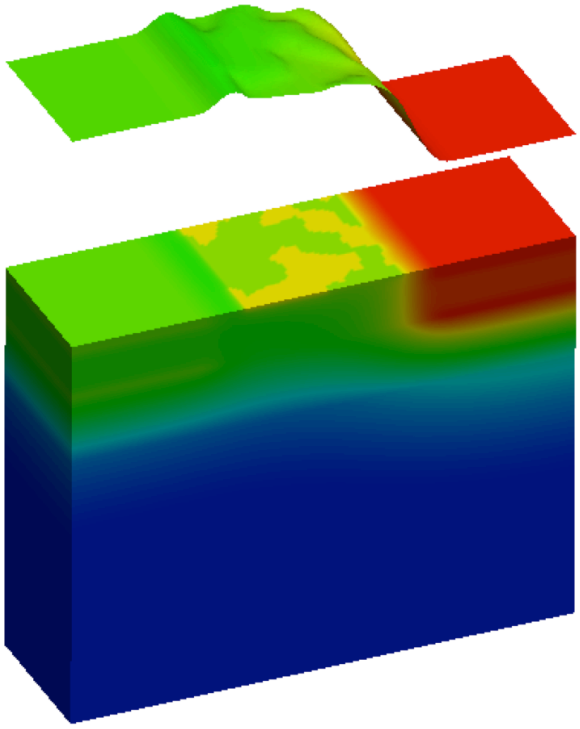


Figure 3.4 : The electrostatic potential in a generic 22nm FD-UTB SOI nMOSFET with the surface potential shown above. The average grain diameter (∅) is 5nm.

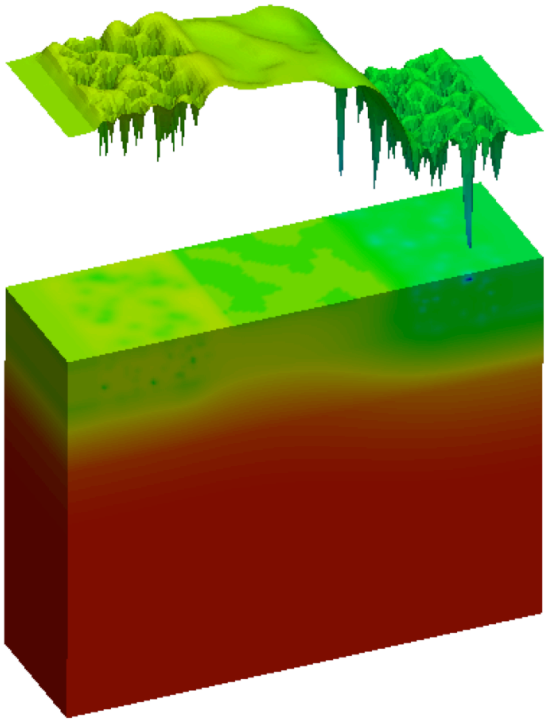


Figure 3.5 : Electrostatic potential for combined variability sources : RDF, LER and MGG for 22nm FD-UTB SOI device.

3.4 Summary

Simulation tools and methodology employed in this research study has been described in detail. The 3D 'Atomistic' drift-diffusion simulator, GARAND, is employed in this study. A very brief introduction of drift diffusion technology is presented, followed by the general description of major statistical variability sources: RDF, LER and MGG, and the corresponding implementation in GARAND. Simulation of large ensembles of devices is necessary in order to understand the statistical behavior of advanced technology nodes. GARAND is a powerful tool for this task and is extensively employed in chapter 5 and chapter 6 of this thesis, where used to investigate the random nature of the variability sources such as RDF, LER and MGG and the statistical analysis of device characteristics.

CHAPTER 4

Fully Depleted Ultra Thin Body Silicon on Insulator (FD-UTB SOI) Design

4.1 Introduction

The performance improvement deriving from the transistor scaling has fueled for the enormous successes of semiconductor industry. Until now, the device miniaturization has been the main driving force for the advancement of semiconductor technology [98]. However, due to the unacceptable level of statistical variability in bulk planar technologies [99], new variability-resilient device architectures are needed in sub-20nm technology nodes. According to ITRS, Fully Depleted Ultra Thin Body Silicon on Insulator (FD-UTB SOI) transistor is among the most promising candidates. Although in theory, UTB SOI transistors should have superior immunity to statistical variability due to the much reduced channel doping level, the statistical variability is not completely eliminated. It is therefore important for semiconductor industry to have an accurate quantitative understanding of the statistical variability behavior of UTB SOI

transistors at the early technology development stage. There is no mature statistical variability data available for UTB SOI MOSFET technology. Therefore, it is extremely important to develop realistic UTB SOI '*template*' scaled transistors for exploring accurately the statistical variability in future scaled UTB SOI technologies.

In this chapter a template 22nm FD-UTB SOI MOSFET designed for low operating power (LOP) application is presented. The drain leakage current is targeted at 5 nA/μm for low power application [12]. The device design study includes transistor design parameters selection and screening. Special attention is focused on the source/drain (S/D) doping profile including the optimization of the spacer between the gate and the source/drain contact regions, which plays a pivotal role in determining the corresponding transistor performance. Starting from the 22nm template transistor, the FD-UTB SOI architecture is further scaled down according to the requirements for the 16nm and 11nm technology generations.

4.2 SOI Technology Review

Over the last twenty years, transistor scaling had been the driving force of the CMOS technology revolution [100, 101]. As the technology nodes approach the decananometer range, the classical scaling may not be able to follow the Moore's law due to intrinsic limitations [3, 102, 103]. In order to keep Moore's law alive, modifications of traditional bulk MOSFET become a necessity, thus leading to novel transistor architectures incorporating new materials [61, 104, 105]. Several decades ago, SOI wafers had been utilized as an integrated circuit substrate especially for space applications. The earliest SOI devices were invented in 1960s for satellite and space exploration programs. The primary advantage of utilising SOI wafers for such applications was its excellent resilience to harsh radiation environment in space. SOI technology has undergone many improvements to reach today's remarkable accomplishment. The progresses include new technologies for SOI wafer fabrication and the invention of new SOI transistor architectures [102, 106].

In terms of SOI substrate development, the researchers and technologists have spent years to deliver reliable techniques to produce high quality and low cost SOI wafers. Silicon on sapphire (SOS) [107] and dielectric isolation (DI) [108] are typical SOI wafer technologies of the early years. The SOI wafer also can be produced by the full isolation of silicon film using porous silicon (FIPOS) or separation by implanted oxygen (SIMOX), where a thin silicon layer is isolated from the substrate through formation and oxidation of porous silicon or through ion beam synthesis of a buried insulator respectively [102]. For modern Fully Depleted (FD) SOI technology, the uniformity of silicon film thickness, including on-wafer uniformity and wafer to wafer uniformity, is one of main requirements on SOI wafer quality control. The main reason for this is that the thickness uniformity is very important for controlling the SCE and the threshold voltage variations [62, 109] of FD SOI transistors. The most promising SOI wafer technology for modern SOI IC is the smart-cut technology. This is a process using deep implantation of hydrogen that allows a thin, well controlled layer from the top of the wafer to be separated naturally according to the location of hydrogen after the bonding of the wafer on top of the Si/SiO_2 substrate [110] [111].

In order to maintain the benefits of scaling, a move from highly doped channel in traditional bulk MOSFET device to lightly doped or undoped fully-depleted channel in new device architectures has been adopted as a semiconductor industry consensus [112-114]. The possible candidates include single gate FD-SOI MOSFET and multiple gate MOSFETs including double gate (DG) [115], triple gate (TriGate) [116] and gate all around (GAA) [117] architectures. By increasing the number of gates, the device performance is improved due to the increased electrostatic control over the device channel by gates [118] [119] [120].

4.3 22nm FD-UTB SOI Transistor Design

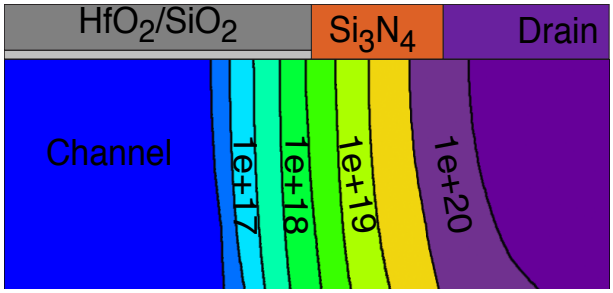
TCAD based design of conventional MOSFET and new device architecture is not an easy task particularly at the sub 100nm channel length regime. Many factors should be taken into account including the device structure, doping distribution, strain, variability, fabrication techniques, and reliability. The predictive simulation on FD-UTB SOI in this chapter aims to deliver a set of well-scaled template devices in order to investigate the level of statistical variability in the forthcoming technology generations with device physical gate length at 22nm, 16nm and 11nm.

4.3.1 Device structure design based on ITRS specifications

A well designed 32nm template thin body SOI (TB SOI) MOSFET for low power application provided by PULLNANO consortium [121] is served as the starting point of this research study. The work starts with a careful re-design of the 32nm TB SOI PULLNANO template transistor using the well-established 3D drift-diffusion simulator, GARAND [122] utilizing density gradient quantum corrections. The design replicates the physical dimensions, doping profiles and the current-voltage characteristics of the PULLNANO transistor [121]. Then, comprehensive simulations are carried out varying important device parameters such as the silicon substrate concentration, equivalent oxide thickness (EOT), buried oxide thickness (T_{BOX}) and silicon body thickness (T_{si}), to understand the impact of the device design parameters on device performance. This understanding serves as a solid ground for future scaling based on the requirements of upcoming technology generations. Figure 4.1 presents the physical dimensions of re-design 32nm TB SOI PULLNANO and its doping profiles. The device transfer characteristics are also presented in Figure 4.2, both linear and logarithmic scales, biased at high and low drain voltage. The results have shown good agreement with the PULLNANO template device.

LOP / Technology Parameter	32 nm
T_{Si} (nm)	7.0
T_{BOX}(nm)	20.0
T_{poly} (nm)	50.0
T_{Tin} (nm)	10.0
T_{HfO_2}(nm)	2.3
T_{SiO_2}(nm)	0.8
L_{spa} (nm)	10.0
N_{bulk} (cm^{-3})	1e18

(a)



(b)

Figure 4.1 : Redesign of 32nm TB SOI PULLNANO, (a) physical dimensions and (b) device structure and its doping profiles.

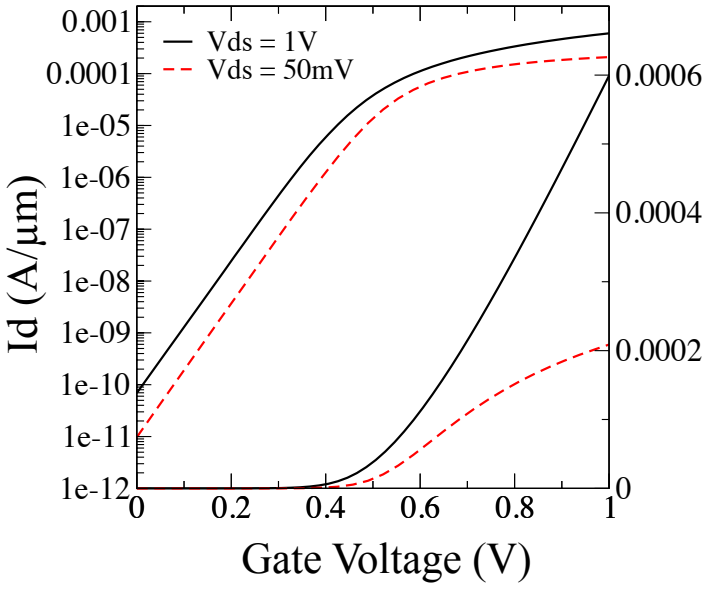


Figure 4.2 : I_dV_g for 32nm gate length TB SOI PULLNANO, biased at high and low drain voltage, in linear and logarithmic scales.

After a successful reproduction and analysis of the 32nm TB SOI transistor, the main task begins with scaling of vertical and horizontal device dimensions by κ=0.7 to realize 22nm technology generation. The design recommendations of the 2009 edition of the ITRS is used as design guidelines [12].

The cross section of the generic structure of 22nm single gate FD-UTB SOI n-type MOSFET is illustrated in Figure 4.3. The adopted supply voltage (V_{dd}) of this transistor is 0.8V and S/D leakage current is fixed at 5nA/μm as suggested in ITRS for low operating power technology requirements. The designed template transistor features titanium nitride (TiN) metal gate, hafnium oxide (HfO_2) high-k dielectric stack with a thin SiO_x interfacial layer ($TiN/HfO_2/SiO_x$). The channel and S/D extensions are doped at $1.2x10^{15}$ cm^{-3} and $2.0x10^{20}$ cm^{-3} respectively. The fixed and the varied device parameters used as design reference are listed in Table 4.1. The impact of device design parameters, such as BOX, EOT, Tsi, on device performance are discussed in detail in the following sections.

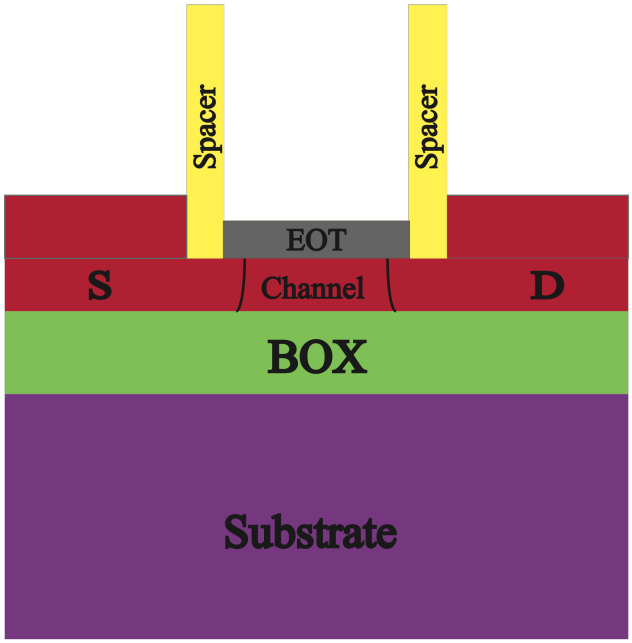


Figure 4.3 : General structure of 22nm single gate FD-UTB SOI n-type MOSFET.

Table 4.1 : Physical device parameters considered for 22nm device.

Design device parameters (unit)	Fixed/Varied device parameters	Value
Physical gate length, L*g* (nm)	Fixed	22
Equivalent oxide thickness, EOT (nm)	Varied	0.8-1.2
Body thickness, T*si* (nm)	Varied	5-10
Buried oxide thickness, T_{BOX} (nm)	Varied	15-60
Spacer length, L*spa* (nm)	Fixed	6
Channel doping concentration (cm^{-3})	Fixed	$1.2x10^{15}$
S/D doping concentration (cm^{-3})	Fixed	$2.0x10^{20}$
Substrate doping concentration (cm^{-3})	Fixed	$1.0x10^{16}$ - $1.0x10^{18}$

4.3.2 Impact of the BOX thickness

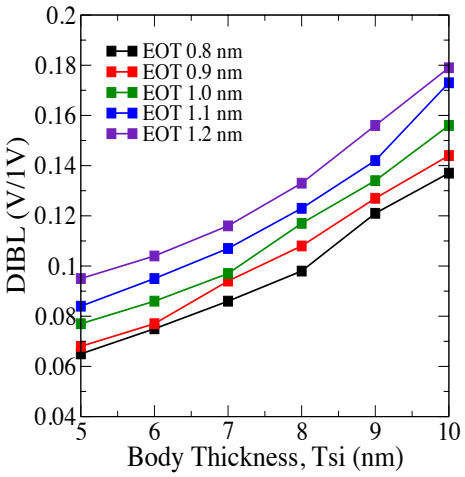
The thicknesses of the buried oxide (BOX) can have significant impact on SCE performance. In this section of the design study, the impact of BOX thickness variations upon device performance is highlighted. A design of experiment simulation environments have been set-up to investigate the influence of three crucial transistor parameters including EOT, T*si* and BOX on the FD-SOI transistor figures of merit for two BOX designs namely thick and thin BOX. Important device figure of merits such as drain induced barrier lowering (DIBL) and sub-threshold slope (SS) have been monitored in this study. Table 4.2 shows the simulation study set-up for 22nm gate length transistor based on thick and thin BOX SOI technologies.

Table 4.2 : Simulation environment for Thick and Thin BOX scenarios.

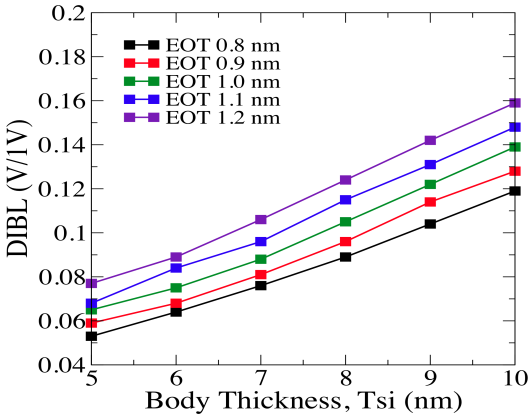
EOT (nm)	Tsi (nm)	BOX (nm) **THICK**	Nbulk (cm^{-3}) **THICK**	BOX (nm) **THIN**	Nbulk (cm^{-3}) **THIN**	Vds (V)
0.8	5,6,7,8 9&10	40,50 &60	1.0e+16	15, 20 & 25	1.0e+16 1.0e+17 1.0e+18	0.8 0.05
0.9	5,6,7,8 9&10	40,50 &60	1.0e+16	15, 20 & 25	1.0e+16 1.0e+17 1.0e+18	0.8 0.05
1.0	5,6,7,8 9&10	40,50 &60	1.0e+16	15, 20 & 25	1.0e+16 1.0e+17 1.0e+18	0.8 0.05
1.1	5,6,7,8 9&10	40,50 &60	1.0e+16	15, 20 & 25	1.0e+16 1.0e+17 1.0e+18	0.8 0.05
1.2	5,6,7,8 9&10	40,50 &60	1.0e+16	15, 20 & 25	1.0e+16 1.0e+17 1.0e+18	0.8 0.05

According to Table 4.2, the thickness of the thick BOX are 40nm, 50nm and 60nm with substrate doping (N_{sub}) fixed at $1.0x10^{16}$ cm^{-3}, while the thicknesses of the thin BOX are 15nm, 20nm, and 25nm, and three different substrate doping concentrations of $1.0x10^{16}$ cm^{-3}, $1.0x10^{17}$ cm^{-3}, and $1.0x10^{18}$ cm^{-3} are considered.

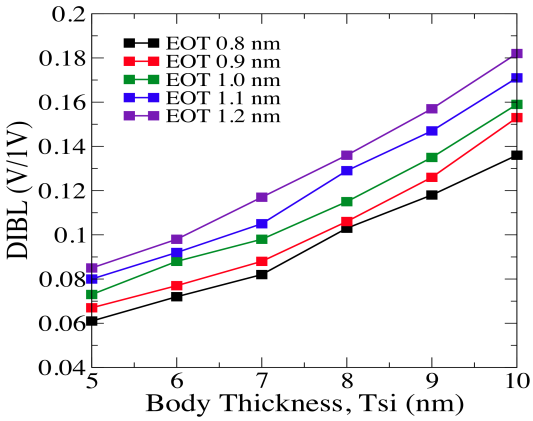
In the comparison study between thick and thin BOX design scenarios, the substrate doping (N_{sub}) is fixed at $1.0x10^{16}$ cm^{-3}. Figure 4.4 and 4.5 illustrate the behavior of DIBL and SS in the case of thick and thin BOX. Figure 4.4 (a)-(f) and Figure 4.5 (a)-(f) show the impact of EOT and T*si* on DIBL and SS respectively for thick and thin BOX scenarios. The sub-threshold slope is evaluated at high drain voltage (V_{ds}) of 0.8V. The results demonstrate that both DIBL and SS increase with the increase of EOT and T*si* . As expected, the devices with smaller EOT and reduced T*si* have better electrostatic control of the gate over the channel and capable to hold back the lateral electrostatic coupling from the drain in controlling the DIBL, SS and thus the leakage current (I_{off}). Nevertheless, compared to the devices with thick BOX, EOT and T*si* have less impact on DIBL and SS for the transistors featured with thin BOX .



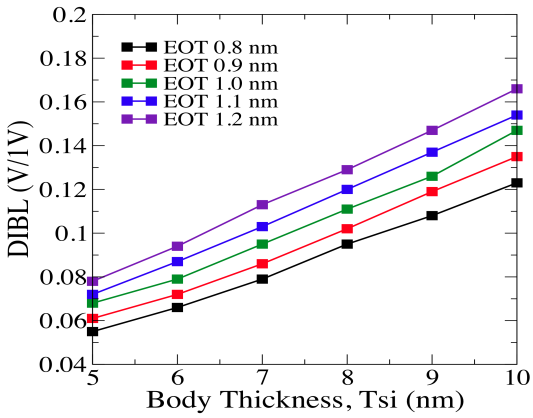
(a) Thick BOX = 40nm



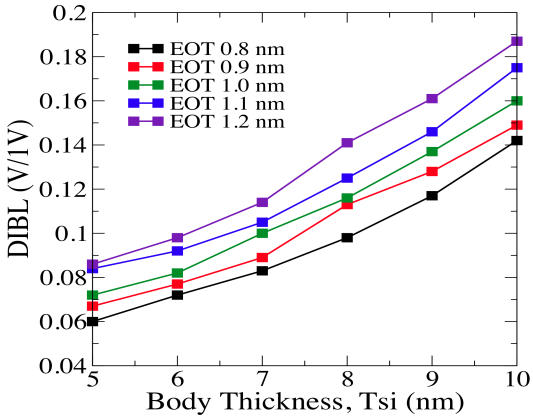
(d) Thin BOX = 15nm



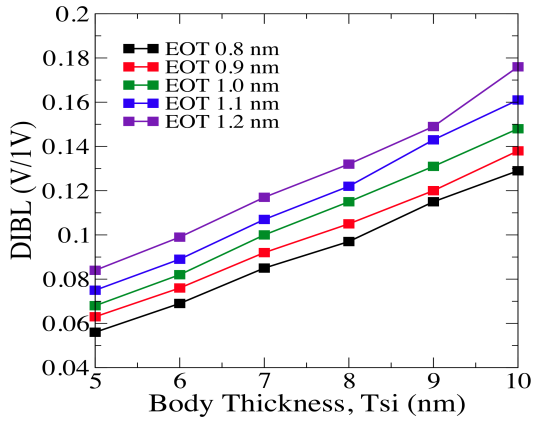
(b) Thick BOX = 50nm



(e) Thin BOX = 20nm

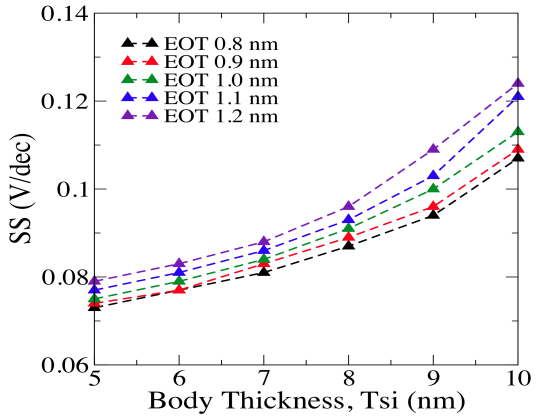


(c) Thick BOX = 60nm

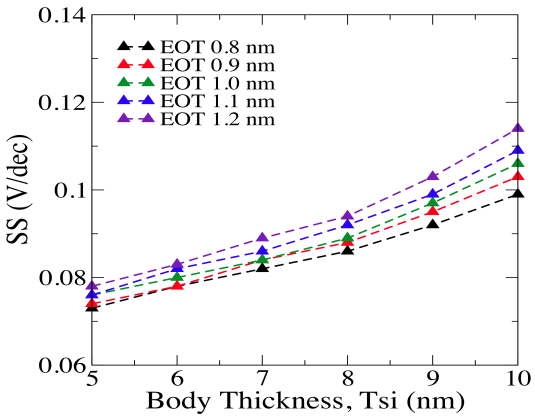


(f) Thin BOX = 25nm

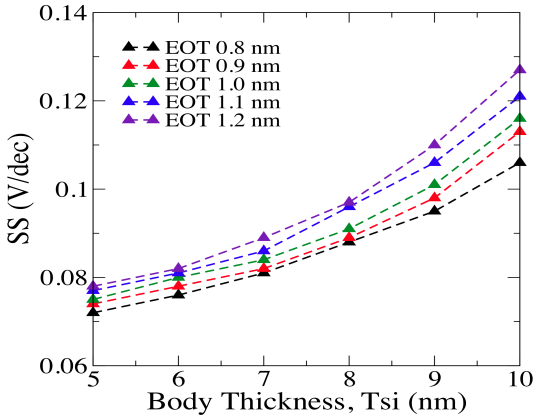
Figure 4.4 : Impact of global variation of EOT and Tsi on DIBL for thick and thin BOX scenarios at high drain voltage (V_{ds}= 0.8V) with N_{sub} = 1.0x10^{16} cm^{-3}.



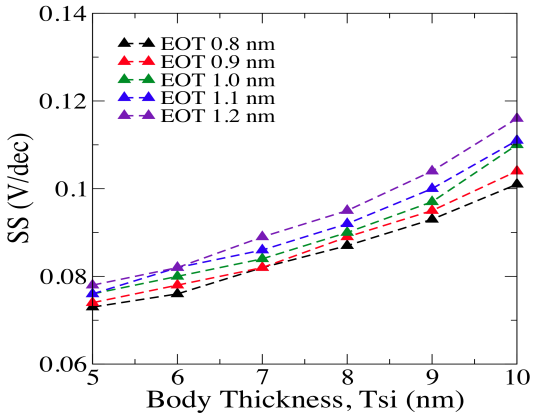
(a) Thick BOX = 40nm



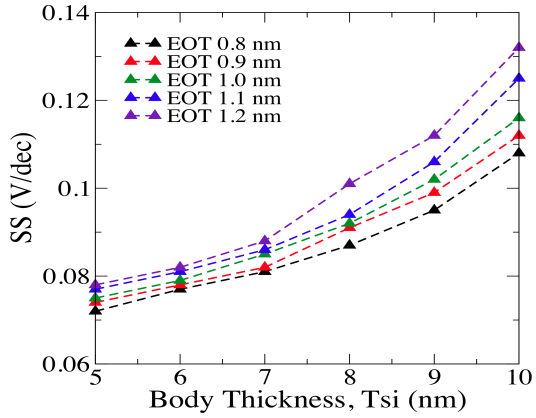
(d) Thin BOX = 15nm



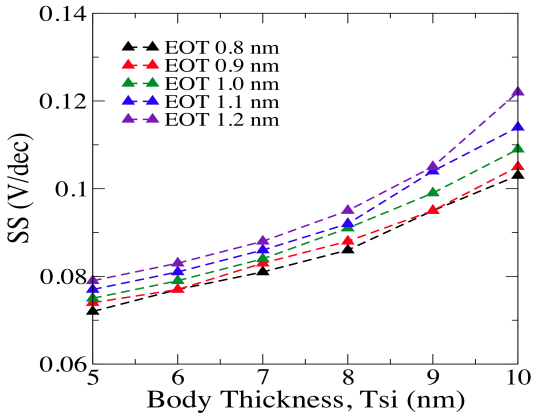
(b) Thick BOX = 50nm



(e) Thin BOX = 20nm



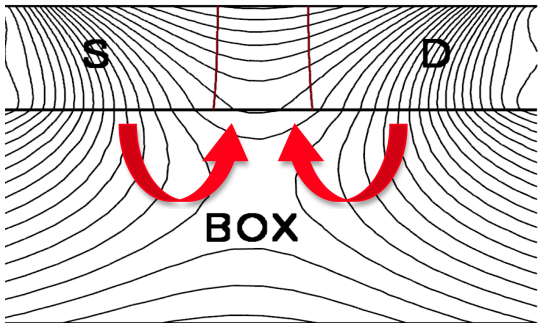
(c) Thick BOX = 60nm



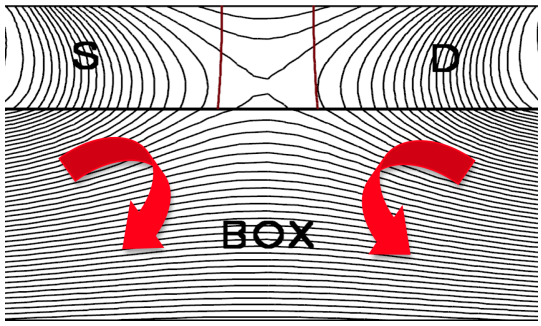
(f) Thin BOX = 25nm

Figure 4.5 : Impact of global variation of EOT and Tsi on SS for thick and thin BOX scenarios at high drain voltage (V_{ds}= 0.8V) with N_{sub} = 1.0x10^{16} cm^{-3}.

Reducing the thickness of the BOX facilitates the suppression of the drain fringing field effect [123], resulting in lower DIBL and SS. The two-dimension (2D) fringing effect present in the thick BOX case, thus result in high leakage current particularly present in thick 60nm BOX. Figure 4.6 illustrates the electrostatic potential distribution in both cases under low drain bias condition. It clearly demonstrates that for thick BOX device, the electric field in BOX that originate from S/D regions tends to terminate in the channel also called active region, resulting in strong BOX field-fringing effect. Meanwhile, for the thin BOX counterpart, the electric field originating from S/D regions tends to terminate in the substrate, leading to a much reduced BOX field-fringing effect. Consequently the electrostatic integrity depends strongly on the thickness of the BOX, and the impact of T*si* and EOT variations on the device characteristics can be substantially different for devices with different BOX thickness, as illustrated in Fig. 4.4 and 4.5.



(a) Thick BOX



(b) Thin BOX

Figure 4.6 : Electrostatic potential contours for thick and thin BOX at V_{ds} = 0.05V indicating 2D coupling through the BOX.

Figure 4.7 further highlight the influence of BOX thickness on T*si* and EOT sensitivity on DIBL and SS. In this simulation experiment setup, a thick BOX of 60nm and a thin BOX of 15nm are considered with a fixed substrate doping concentration of $1.0x10^{18}$ cm^{-3}. The nominal values of T*si* and EOT are 7nm and 0.9 nm respectively, and each individual parameter is treated separately. In order to explore a broad design space, the T*si* value is varied from 5nm to 9nm, and EOT value is varied from 0.7nm to 1.1nm. The T*si* value is fixed at 7nm in the EOT variation study, while EOT is fixed at 0.9nm in T*si* variation study.

When T*si* varies from 7nm to 5nm, similar DIBL and SS improvement can be achieved for both the thick and the thin BOX transistors. However, when T*si* increases from 7nm to 9nm, the device with thin BOX maintains strong resilience to the degradation of DIBL and SS, yielding 52 mV/1V degradation of DIBL and 20 mV/dec degradation of SS respectively. For the thick BOX device, the corresponding values are 77 mV/1V and 51mV/dec respectively. In general, devices with thick BOX are more sensitive to variation on T*si*.

With EOT varied from 0.9nm to 0.7nm, for the transistors with thick BOX of 60nm, the DIBL is reduced from 141 mV/1V to120 mV/1V, and the SS is improved from 95 mV/dec to 89 mV/dec. Similar degrees of improvement is obtained for the transistors with thin BOX of 15nm, with DIBL decreasing from 118 mV/1V to 97 mV/1V, and SS reduced from 92 mV/dec to 86 mV/dec. When EOT is increased from 0.9 nm to 1.1nm, for both the thick and the thin BOX transistors, the amount degradations of DIBL is similar, around 30 mV/1V. However, in respect of SS, the device with thin BOX is more resilient yielding degradation of 4mV/dec compared to 10mV/dec in the thick BOX counterpart.

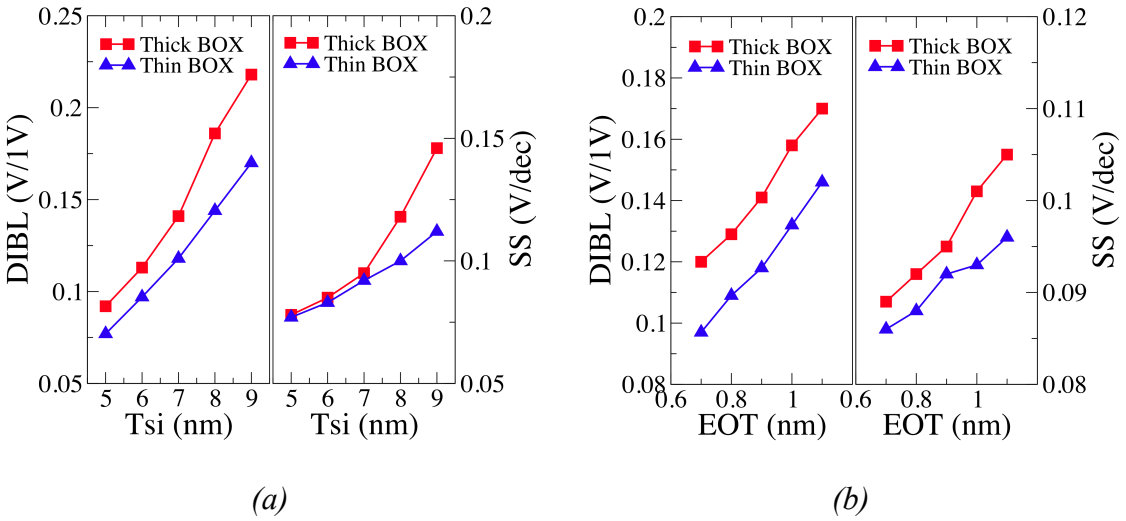


Figure 4.7 : Trend of DIBL and SS against variation of (a) Tsi and (b) EOT for 60nm thick BOX and 15nm thin BOX.

It is also worth studying the impact of the doping concentration beneath the BOX since it will influence the potential distribution and the magnitude of the fringing effects. The impact of the substrate doping concentration on DIBL and SS is illustrated in Figure 4.8, for the devices with the thin BOX, EOT and T_{si} being 15nm, 0.9nm and 7nm respectively. The substrate doping has beneficial impact on DIBL or SS for doping concentrations higher than $1.0x10^{17}$ cm^{-3}.

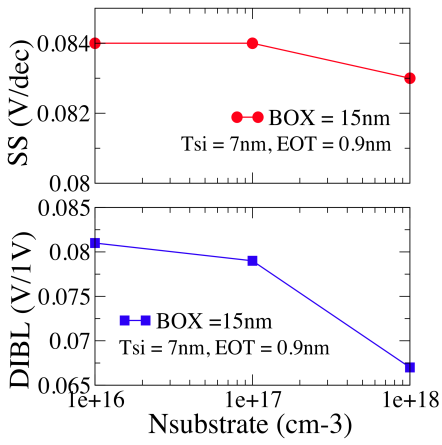


Figure 4.8 : Impact of different substrate doping concentration on SS and DIBL for the thin BOX device of 15nm, Tsi of 7nm and EOT of 0.9nm.

Based on the above results, it is clear that the device with thin BOX and high substrate doping concentration not only offer better control of short channel effect, but simultaneously have better variability performance in respect of global variations of T*si* and EOT. In FD-SOI technology, Process Integration, Devices and Structures (PIDS) technology requirements have introduced buried oxide thickness as a new design parameter in ITRS 2011. In this ITRS edition, the physical gate lengths of 21nm, 16nm and 11.9nm stipulate buried oxide thickness of 18nm, 14nm and 11nm respectively. Recently, the use of ultra thin BOX down to 10nm is also utilized as an approach to allow back-bias control of the threshold voltage [112, 124, 125]. Therefore, due to superior electrostatic integrity and considering its manufacturability, the thickness of BOX layer in our 22nm FD-UTB SOI design is chosen to be 10nm and it remains fixed at the next stage of device parameter optimizations.

4.3.3 Impact of the Source/Drain doping abruptness

Even though the silicon body in UTB SOI can control SCEs, the further scaling of silicon body thickness can result in drive current degradation due to the increased S/D access resistance. One of the major factors influence the access resistance is the doping profile. It has been suggested that elevated S/D (ESD) structure can be used to minimize this access resistance [126, 127].

In designing UTB SOI transistors, one of the significant design challenges is the trade-off between access resistance of the S/D regions and the device electrostatic integrity. As a result, it has to be approached carefully in order to achieve high overall device performance. Although the UTB SOI could tolerate low channel doping which enhances the channel mobility and reduces dopant-induced V_{th} fluctuation [21], there is still a room for punch-through when the S/D extensions are heavily doped in order to reduce the access resistance. Therefore, the focus at this stage of the design is the lateral doping profile in the S/D extension regions. The impact of the S/D profile abruptness (σ) on the access resistance is studied systematically in an attempt to provide a guideline for the realistic UTB SOI device design. For simplicity, an analytical doping profile based on the Gaussian distribution is used in this study as illustrated in Figure 4.9.

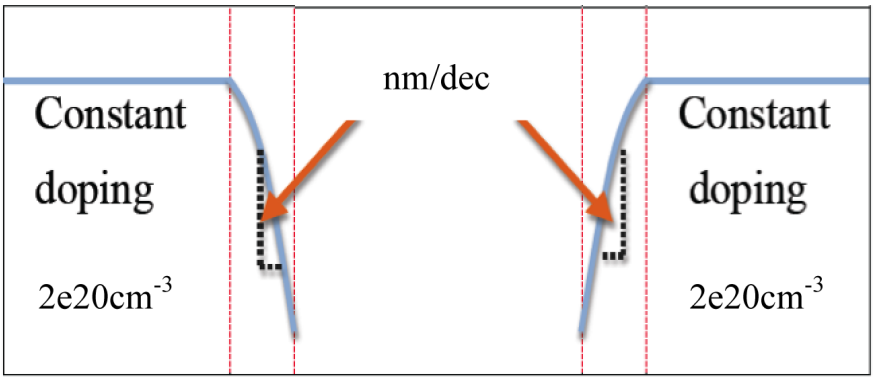


Figure 4.9 : Doping abruptness (nm/dec) under the spacer and doping profile based on Gaussian function.

The lateral distribution of the S/D doping profile is given by equation (4.1),

$$N = N_{peak} \exp\left[-(x - x_{space})^2 / 2\sigma^2\right] \qquad x \geq x_{space}$$
$$N = N_{peak} \qquad x < x_{space} \tag{4.1}$$

where x_{space} is determined by spacer length (L_{spa}) , σ is determined by the abruptness of the doping profile, measured in nm/dec. At this design stage, the spacer length is fixed at a typical value of 6nm. Based on the ITRS recommendation for the abruptness of S/D junction profiles for advanced technology nodes, three different abruptness values are selected : 2.0, 2.5 and 3.0 nm/dec. According to ITRS requirement, drain leakage current of 5nA/μm under high drain bias condition is the maximum tolerated leakage current for LOP application. In order to have a fair comparison, the gate work-function (W_f) has been adjusted for each design scenario, so that the high drain bias leakage current is fixed at 5nA/μm. In all designs, the doping distributions are symmetrical in source and drain regions decaying according to the Gaussian distribution in the channel region. Figure 4.10 shows the Gaussian S/D doping profiles with different doping gradients.

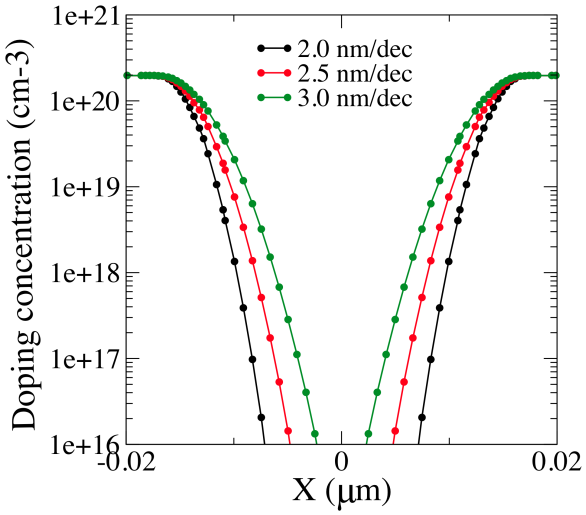


Figure 4.10 : Illustration of various lateral S/D doping abruptness along the channel; 2.0, 2.5 and 3.0 nm/dec, with L_{spa} of 6nm.

The underlap S/D profiles are designed such that the extension region doping does not exceed beyond the gate edge. The device transfer characteristics are presented in Figure 4.11 (a) and (b) using both linear and logarithmic scales, the gate work-function is tuned to make sure that the high drain bias leakage current remains fixed at 5 nA/μm. The simulated results show that, the S/D doping abruptness has a significant impact on drive current and the electrostatic integrity. Although the higher σ value results in lower the S/D access resistance, the electrostatic integrity plays a more important role here. The transistor with abrupt S/D doping profile of 2.0 nm/dec delivers the best results including better control of the sub-threshold slope, DIBL and I_{on} performance. When analyzing the device performance in terms of spacer thickness to doping abruptness ratio (L_{spa} / σ) [128], the L_{spa} / σ ratio is 3, 2.4 and 2 for σ of 2, 2.5 and 3 nm/dec respectively, where the L_{spa} is 6nm. In addition, the dependency of L_{eff} on L_{spa} / σ is clearly observed in [129], where the effective channel length (L_{eff}) increases linearly with L_{spa} / σ. The higher the L_{spa} / σ, the longer the L_{eff} is, resulting in device with better short channel effects.

In the next stage of the design experiment study, the source/drain doping abruptness is fixed at 2.0 nm/dec, due to the observed superiority in terms of electrostatic integrity and performance.

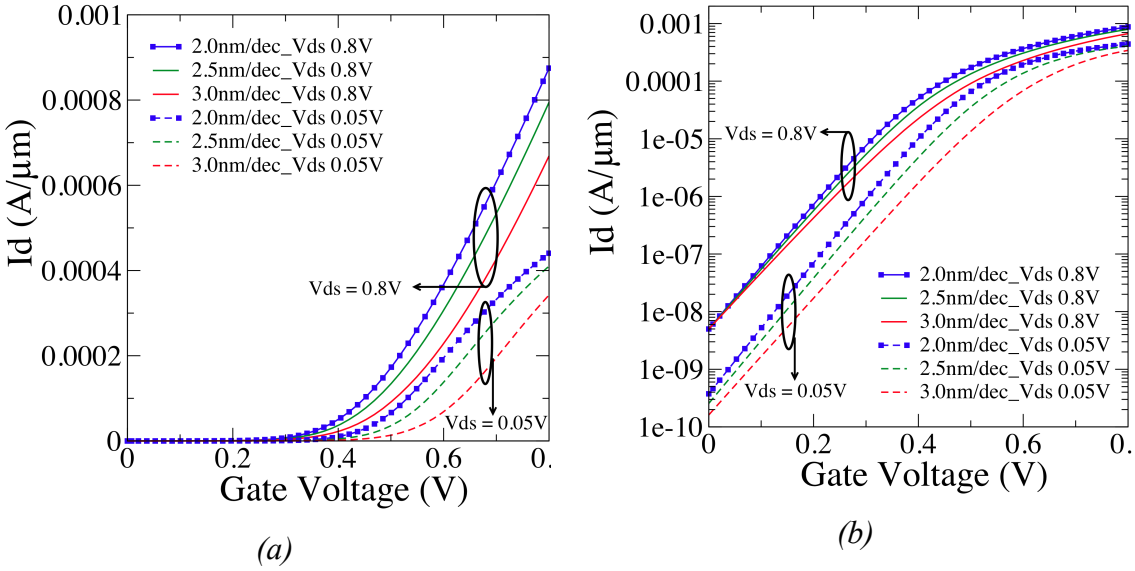


Figure 4.11 : I_dV_g for three different σ (nm/dec), biased at high and low drain voltage; (a) linear and (b) logarithmic scales.

4.3.4 Spacer length optimization

At the previous stage of this design study, the BOX thickness and doping gradient abruptness have been investigated meticulously. From the comprehensive simulated results of the 22nm FD-UTB SOI transistor, the thin BOX of 10nm and doping gradient abruptness,σ of 2.0 nm/dec are the most suitable design for the 22nm device. These device parameters will be fixed in the following spacer length optimization study.

At this design stage, while σ is fixed at 2.0 nm/dec, the spacer length, L_{spa} is varied from 4nm to 9.8nm. From S/D access resistance design point of view, a short spacer length would deliver lower access resistance, while from electrostatic integrity point of view, the longer the spacer length will reduce the short channel effects. Similar to the previous design procedure, the gate work-function is tuned to make sure that the high drain bias leakage current remains fixed at 5 nA/µm. The results are presented in Figure 4.12 (a) and (b). For better understanding, the impact of spacer variation against DIBL and SS is illustrated in Figure 4.13.

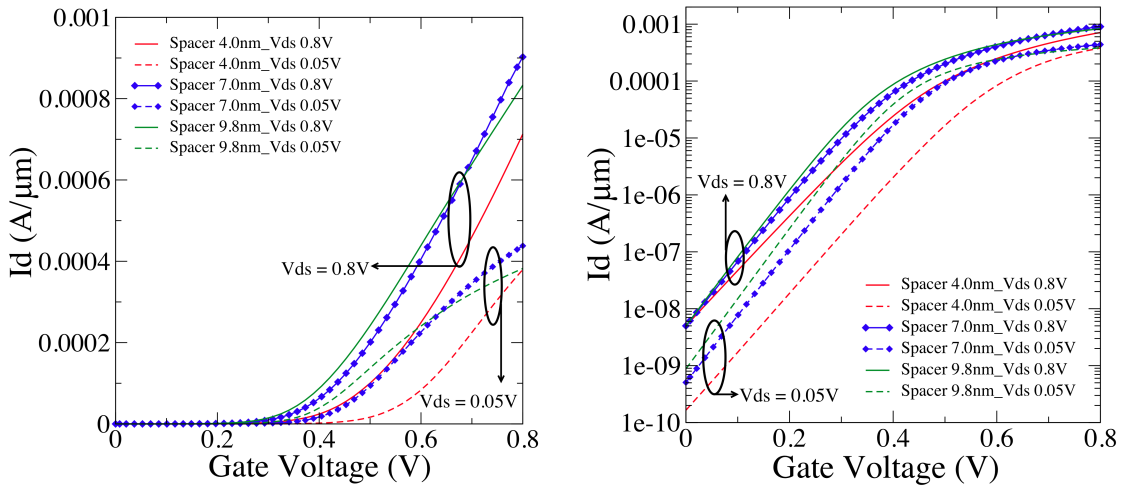


Figure 4.12 : I_dV_g for 22nm at dissimilar spacer lengths , biased at high and low drain voltage; (a) linear and (b) logarithmic scales.

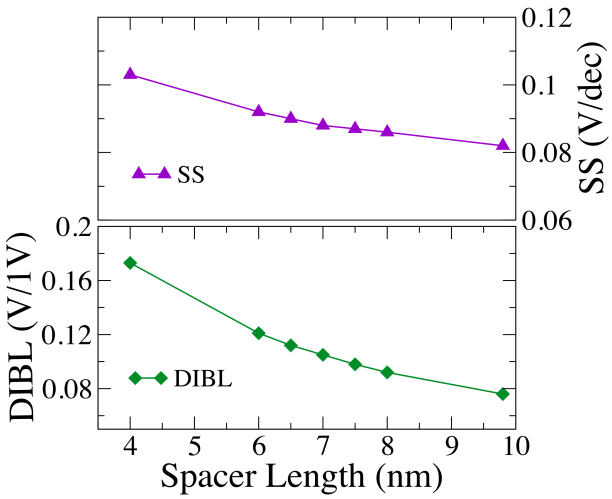


Figure 4.13 : Impact of spacer length variation on DIBL and SS.

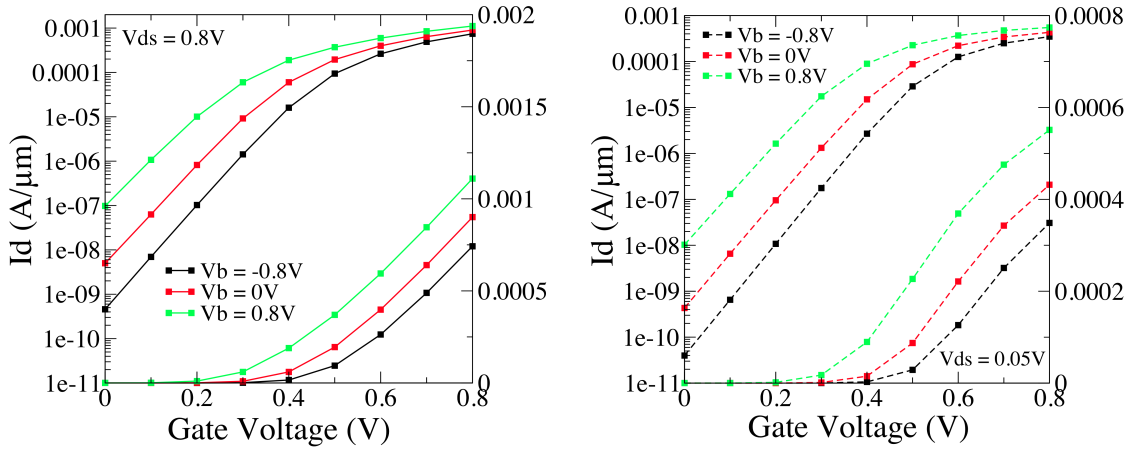
Although the smaller spacer length of 4nm offers the smaller access resistance, it leads to not only an increased gate to S/D parasitic capacitance, but also results in a significant degradation of the DIBL. In turn, the device at spacer length of 9.8nm deliver best sub-threshold slope and DIBL, but the drive current is slightly below the design requirement. The device with a spacer length of 7nm provides the best overall results; high drive current with acceptable DIBL and SS performance. In traditional transistor design, the sub-threshold slope and DIBL are among the most important

figures of merit as device with better sub-threshold slope and DIBL performances normally deliver greater drive current. However, with the increase of S/D access resistance in UTB SOI transistors, the sub-threshold slope and drive current is not well correlated and careful design trade-off is necessary in order to achieve particular design specification.

4.3.5 Substrate bias effects

Apart from having high immunity to statistical variability, better scalability and improved electrostatic integrity, another merit of FD-UTB SOI is the broad range of back bias control. The back gate bias (also known as substrate bias, V_b) effect is very useful in low power and high performance applications [112, 130]. The substrate bias is beneficial not only for increasing the drive current but could be also used to reduce the leakage current by orders of magnitude. These can be achieved by controlling dynamically the threshold voltage by applying substrate bias which is very effective for FD SOI transistors with thin BOX.

Figure 4.14 (a) and (b) show the current-voltage characteristics of FD-UTB SOI transistors with BOX thickness of 10nm, silicon body doping of 1.2×10^{15} cm^{-3} and substrate doping of 1.0×10^{18} cm^{-3} in saturation and linear modes of operation respectively. The substrate biases are -0.8V, 0V and 0.8V. The application of negative bias of V_b = -0.8V increases the threshold voltage, reducing the leakage current significantly. The application of forward substrate bias decreases the threshold voltage and hence increases the drive current. However, the leakage current also increases. This behavior is pertinent to both saturation and linear modes.



(a) *(b)*

Figure 4.14 : I_dV_g for different substrate bias, V_b = -0.8V, 0V and 0.8V in linear and logarithmic scales, (a) saturation and (b) linear modes.

Therefore, FD-UTB SOI transistors offer interesting opportunities of efficient power management in low power handheld applications. In addition, an improvement of gate induced drain leakage (GIDL) in ultra thin body and BOX devices also have been reported [130]. Meanwhile, studies in [52, 131] have showed that static noise margins (SNM) of six-transistors static random access memory (6T-SRAM) cells can be improved via substrate bias effect.

4.4 Design of 16nm and 11nm Technology Generations FD-UTB SOI Transistors

The previous sections described the design of the template 22nm gate length FD-UTB SOI n-MOSFET which will be used to study the corresponding statistical variability effects in chapter 5 of this thesis. In this section, the design procedures and device characteristics of scaled device down to 16nm and 11nm technology generations are presented. According to ITRS 2009, the 16nm and 11nm technology generations are expected to be in mass production in year 2016 and 2020 respectively. For that reason, it is crucial to access the statistical variability of the FD SOI transistor corresponding to these technology generations.

The FD-UTB SOI transistor with 16nm and 11nm gate length also feature metal gate and high-k dielectric stack similar to the 22nm template device. Prior studies indicate that thin BOX will be favorable due to better electrostatic control and reduced self-heating. The thickness of the BOX has been fixed to 10nm for all technology generations considering the manufacturability of the thin BOX SOI wafer. The high substrate doping of $1.0x10^{18}$ cm^{-3} and channel doping of $1.2x10^{15}$ cm^{-3} were implemented. The value of EOT and T_{si} are selected according to ITRS recommendation. For the 16nm gate length template transistor, they are 0.75nm and 5.1nm respectively. Meanwhile, for 11nm gate length, the EOT is 0.6nm and Tsi is 4nm. Both technology generations operate at same supply voltage of 0.75V. The leakage current is set at 5nA/μm regardless of technology generation, which is in line with the ITRS requirements of low power application.

Based on the results of S/D doping abruptness and spacer length optimization, the final decisions have been made. The S/D doping roll-off is fixed at 2nm/dec, while the spacer length is set at 7nm due to the trade off between DIBL and on-current. The device design parameters of 22nm, 16nm and 11nm are summarized in Table 4.3.

Table 4.3 : Device parameters for three technology generations.

Technology (nm) / Device parameters	22	16	11
EOT (nm)	0.9	0.75	0.6
Body thickness, T_{si} (nm)	7	5.1	4.0
Buried oxide thickness, T_{BOX} (nm)	10	10	10
Spacer length, L_{spa} (nm)	7	7	7
S/D doping abruptness, σ (nm/dec)	2	2	2
S/D doping concentration (cm^{-3})	$2.0x10^{20}$	$2.0x10^{20}$	$2.0x10^{20}$
Substrate doping concentration, N_{sub} (cm^{-3})	$1.0x10^{18}$	$1.0x10^{18}$	$1.0x10^{18}$
Channel doping concentration (cm^{-3})	$1.2x10^{15}$	$1.2x10^{15}$	$1.2x10^{15}$
Supply Voltage, V_{dd} (V)	0.8	0.75	0.75

The simulated current-voltage characteristics for the 16nm channel length transistor are shown in Figure 4.15. Drive currents of 1177 μA/μm is obtained at 5nA/μm leakage current. SS and DIBL are 86 mV/dec and 111 mV/1V respectively. The SS is improved by 2.27% and the DIBL is slightly increased by 1.83% compared to 22nm technology generation.

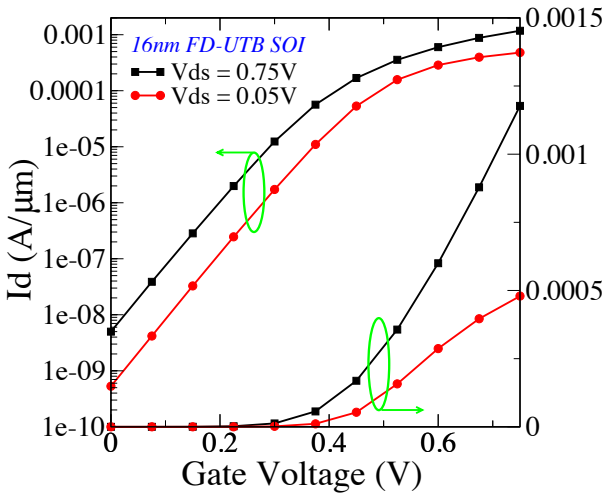


Figure 4.15 : I_dV_g characteristics in linear and logarithmic scales for 16nm FD-UTBSOI MOSFET.

The I_dV_g characteristics of the 11nm FD-UTB SOI transistor are illustrated in Figure 4.16. The supply voltage is 0.75V similarly to the 16nm technology. There is an enhancement of the drive current when the device is scaled down. The saturation drive current of 1213 µA/µm at 5 nA/µm leakage current. Meanwhile the SS and DIBL are 87 mV/dec and 121 mV/1V respectively. A summary of the performance of the template n-channel FD-UTB SOI MOSFETs with gate length of 22, 16 and 11nm is presented in Table 4.4.

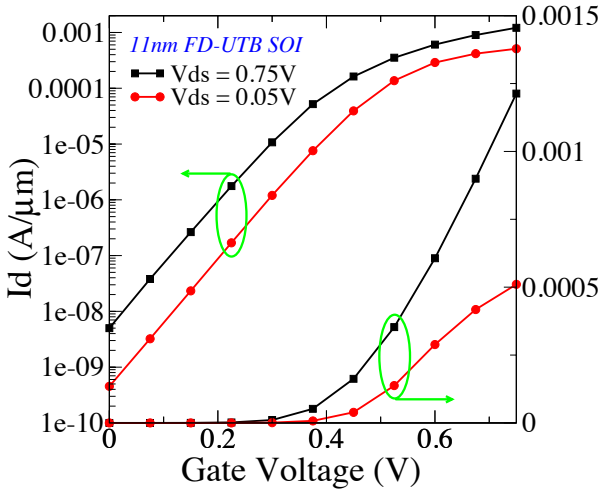


Figure 4.16 : I_dV_g characteristics in linear and logarithmic scales for 11nm FD-UTBSOI MOSFET.

Table 4.4 : Key electrical parameters of the device templates for 3 technology generations.

Gate length (nm)	V_{ds} (V)	V_{th} (mV)	I_{on} (µA/µm)	SS (mV/dec)	DIBL (mV/1V)
22	0.8	205	900	88	109
	0.05	287	432	85	
16	0.75	199	1177	86	111
	0.05	277	479	83	
11	0.75	203	1213	87	121
	0.05	288	510	86	

4.5 Summary

In this chapter, the design of FD-UTB SOI n-channel MOSFET corresponding to the 22nm, 16nm and 11nm technology generations is reported. A 32 nm template transistor provided by PULLNANO project is the starting point at this scaling study. The device design is target at low power application. The simulations are carried out using the 3D drift-diffusion simulator, GARAND. The aim was to deliver a set of well-scaled template devices in order to investigate the statistical variability in the forthcoming technology generations.

The simulation study first focused on the design of 22nm gate length transistor exploring the impact of the BOX thickness. The impact of thick and thin BOX on key figures of merit was investigated. The impact of global variations of EOT and T_{si} on device performance was also investigated in detail for the two BOX design scenarios. The results indicate that the device with thin BOX not only has improved short channel effect, but also has better resistance to global variation of EOT and T_{si}. Consequently, a BOX thickness 10nm was chosen. The next step was S/D doping abruptness and spacer length optimization. Although the higher σ value of the Gaussian S/D doping profile provides lower S/D access resistance, the electrostatic integrity plays a more important role here. The transistor with 2 nm/dec doping steepness delivers the best overall performance for SS, DIBL and drive current. In respect of the spacer length, the transistor with spacer length of 7nm delivers the superior overall performance. Excellent back-bias control increasing the drive current, reducing the leakage current by order of magnitude was demonstrated in 22nm gate length transistor design.

Based on the 22nm template UTB SOI transistor, 16nm and 11nm template devices were designed by adopting realistic physical scaling scenarios for UTB SOI technology. Regardless of technology generations, the BOX, σ and L_{spa} are fixed at 10nm, 2 nm/dec and 7nm respectively. The simulation based design has delivered three technology generations of UTB SOI template transistors that meet the ITRS performance targets.

CHAPTER 5

Statistical Variability in FD-UTB SOI Scaled Devices

5.1 Introduction

"Small is beautiful". That is what can describe the development of today's semiconductor technology. The great triumph of the semiconductor industry is based on the technology scaling that provides increased functionality and chip compactness while reducing the cost. However, scaling pace is now hitting a breaking point where hard technological and physical challenges start to emerge. Among other difficulties, intrinsic parameter fluctuation due to discreteness of charge and granularity of matter, which are essentially unavoidable, are becoming serious concerns for device integration, and circuits and systems performance and yield. These become more critical when the characteristic size of material grains and roughness in device definition become comparable to the transistor dimensions. The statistical variability has been identified as a critical challenge in CMOS scaling, in many reports and publications [28,

30]. It has far reaching impact on semiconductor memory circuits, including SRAM (static random access memory), where careful consideration and balance at device level is needed [132]. Due to the statistical nature of the device variation, the circuit and system design methodology is shifting from deterministic approach to probabilistic approach; consequently, the statistical variability study is becoming not only an important research field but also a practical necessity for the semiconductor industry [30, 133].

This chapter presents a comprehensive study of statistical variability in scaled transistors that has been discussed already in Chapter 4. FD-UTB SOI template of 22nm, 16nm and 11nm technology generation devices for low power (LOP) applications. The impact of random dopant fluctuation (RDF), line edge roughness (LER) and metal gate granularity (MGG) on threshold voltage (V_{th}), on-current (I_{on}) and drain induced barrier lowering (DIBL) variability are analysed in details. Each one of the variability sources studied are treated individually and also in combination.

5.2 Impact of Statistical Variability in FD-UTB SOI Scaled Devices

Novel device technology and architecture have been introduced to allow further device scaling while mitigating variability. The UTB SOI transistors can tolerate very low channel doping concentration due to much improved electrostatic integrity, and as a result, the variability from random dopant fluctuation is dramatically reduced. However, other sources of variability remain pertinent including line edge roughness [15, 96] and metal gate granularity leading to work-function (W_f) variation which critically affect the threshold voltage of the devices. The dissimilar nature of RDF, LER and MGG variability sources influence the dispersion of threshold voltage, on-current and DIBL in different ways. Those variability sources are explored in order to evaluate their impacts on device and circuit design performance.

For each technology generation, simulations of statistical variability on 1000 device ensembles of microscopically different transistors are performed, by using the very well-established 3D density-gradient quantum-corrected drift-diffusion simulator GARAND [91]. In this simulation study, the relevant modelling parameters for LER are 3σ = 2nm and a correlation length, λ = 25nm [134]. Meanwhile, inrelation to MGG, TiN introduces two metal grain orientations with a probability of 0.4/0.6. The work-function (W_f) difference between these two types of grain is 0.2eV, and for our particular device technology, they are 4.4/4.6 eV respectively. In this study, an average grain size diameter of ∅= 5nm is assumed for 22nm, 16nm and 11nm technology generations because it agrees with observations for TiN in a gate-first process [96, 97]. The threshold voltage is extracted from I_d-V_g characteristics by using current criteria. Each of the simulated sources of statistical variability has a different impact on the device behavior. All these will be explained qualitatively and quantitatively in the following sub-sections.

5.2.1 Random Dopant Fluctuation (RDF) : 22nm, 16nm and 11nm

The impact of random dopant fluctuation (RDF) on V_{th}, I_{on} and DIBL in the three different gate length devices: corresponding to 22nm, 16nm and 11nm technologies are presented in this section. Simulations of statistical ensemble of 1000 microscopically different FD-UTB SOI devices are carried out for RDF induced variability. Figure 5.1 shows the microscopic effects inside the device due to RDF. In this figure, the electron potential landscape and electron concentration surface in the body of the FD-UTB SOI transistor subjected to the influence of RDF are illustrated.

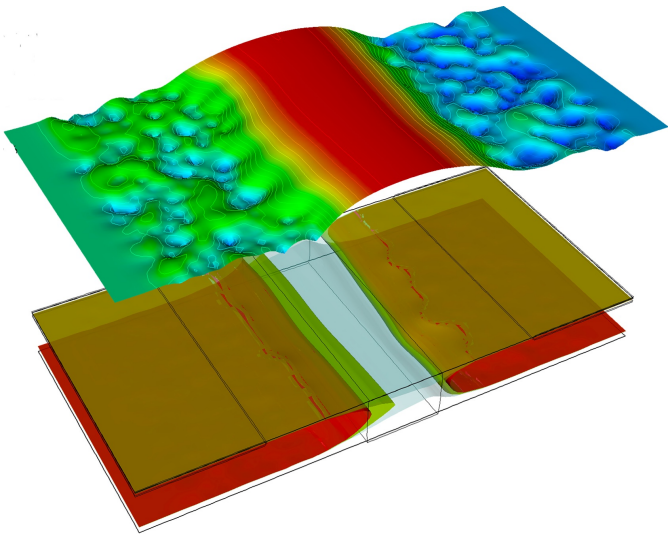


Figure 5.1 : Electron potential landscape and electron concentration surface in the body of the device in the presence of RDF.

In the case of RDF referring to Figure 5.1, the potential in the channel is smooth since there are no ionized acceptors in the undoped body. Therefore RDF-induced V_{th} fluctuations are well suppressed. However, potential fluctuations due to donors in the source and drain extensions (S/D-RDF) lead to large fluctuations in the source/drain access resistance, resulting in an increase in the on-current variability. This has been recently reported theoretically and experimentally in [135, 136]. In addition, the S/D-RDF results in a local modulation of the channel length, and therefore introduces RDF influences on the DIBL fluctuations as well. The complete ensemble of 1000 gate transfer characteristics in saturation and linear regimes for 22nm, 16nm and 11nm gate length, subjected purely to RDF are illustrated in Figure 5.2 (a)-(c) and Figure 5.3 (a)-(c) respectively. Noticed that, the I-V dispersion is relatively small in the sub-threshold region. This is the reason why FD-UTB SOI devices have low mismatch coefficient (A_{vt}) [14, 51, 137]. Now ever with the scaling, the on-current dispersion increases dramatically. Additionally, further elucidating the importance of RDF and access resistance (R_{SD}) variation as evidenced by some current-voltage (I-V) curve crossing at high gate voltage in linear regime. This phenomenon is more clearer for small scaled transistor.

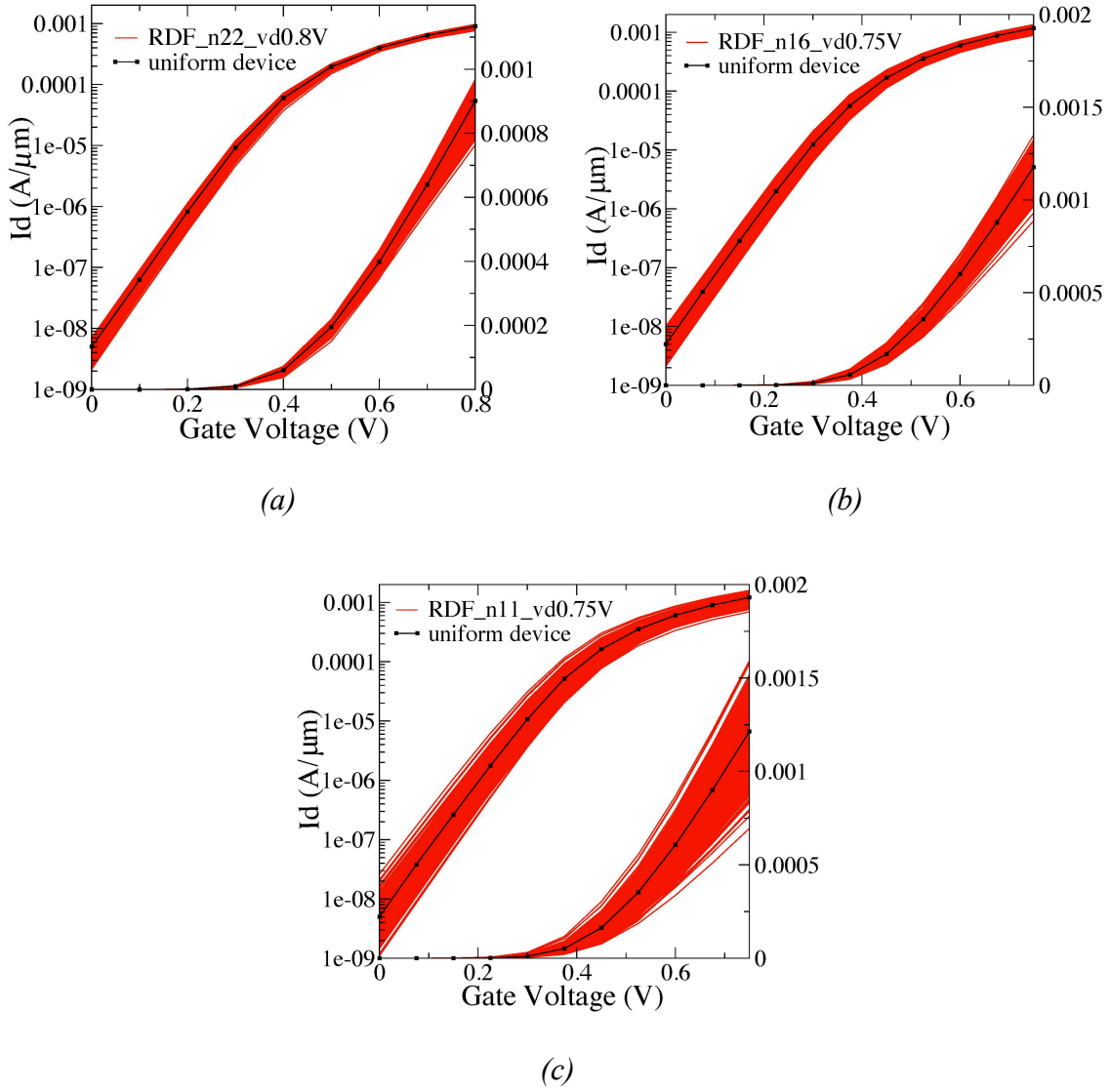
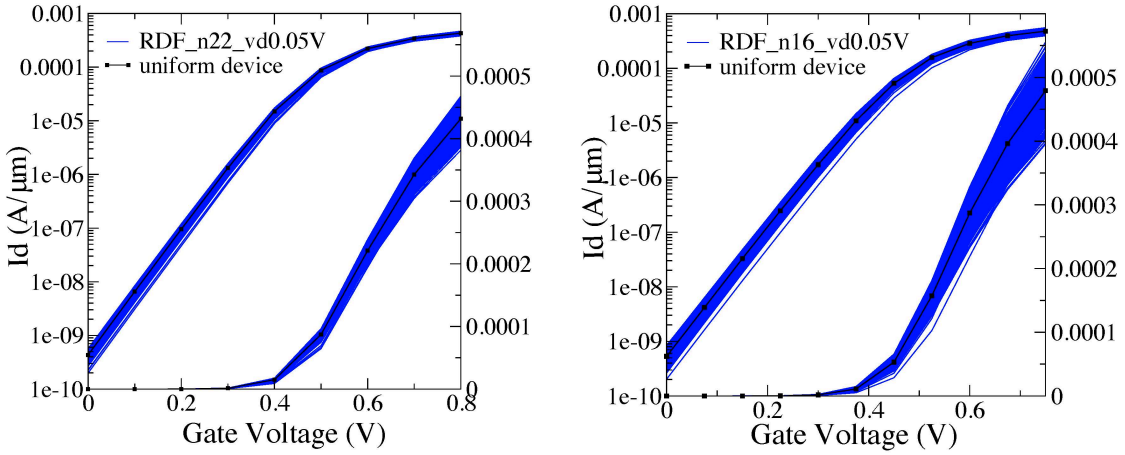
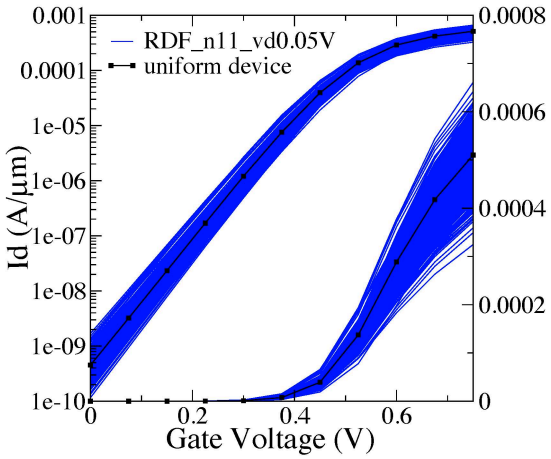


Figure 5.2 : Saturation transfer characteristics of (a) 22nm, (b) 16nm and (c) 11nm device ensembles under influence of RDF.



(a)

(b)



(c)

Figure 5.3 : Linear transfer characteristics of (a) 22nm, (b) 16nm and (c) 11nm device ensembles under influence of RDF.

The distributions of threshold voltage, on-current and DIBL due to RDF in three generations of FD-UTB SOI with gate lengths of 22nm, 16nm and 11nm are presented in Figure 5.4 (a)-(c). The threshold voltage standard deviation (σV_{th}) in Figure 5.4 (a) are 5mV, 7.97mV and 12.6mV for 22nm, 16nm and 11nm gate lengths respectively. These values are small and indicate the V_{th} fluctuations are well suppressed, attributing to the undoped channel and typically, there are no ionized impurities under the gate. Meanwhile, the on-current variations in Figure 5.4 (b) have on-current standard deviation (σI_{on}) which slightly prominent, they are 0.029 mA/μm, 0.066 mA/μm and 0.135 mA/μm for 22nm, 16nm and 11nm technology generations respectively. This was expected due to the donors in the S/D extensions that lead to huge fluctuations in S/D access resistance thus rendering significant increase in the on-current variability with scaling. Note that, with respect to DIBL, RDF also affects DIBL fluctuations in consequence of channel length modulation, and can be seen in Figure 5.4 (c). The reduction in the gate length results increase in the RDF-induced variability.

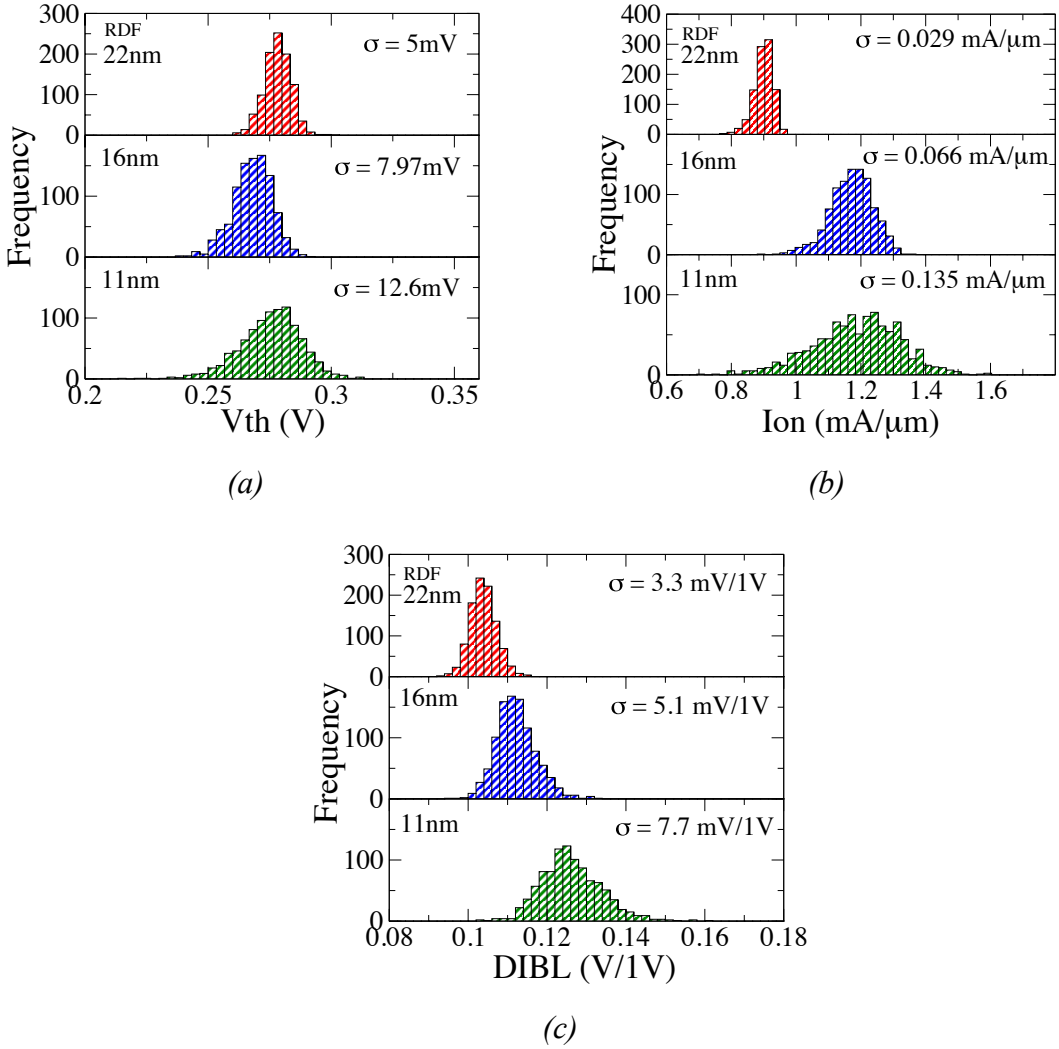


Figure 5.4 : Histograms of the impact of RDF-induced fluctuations on (a) V_{th}, (b) I_{on} and (c) DIBL for 22nm, 16nm and 11nm devices.

5.2.2 Line Edge Roughness (LER) : 22nm, 16nm and 11nm

The line edge roughness (LER) is another statistical variability contributor associated with the lithographic process. The impact of LER on V_{th}, I_{on} and DIBL for three gate lengths of 22nm, 16nm and 11nm is discussed in this section. The impact of LER on the potential and the electron concentration landscapes is shown in Figure 5.5.

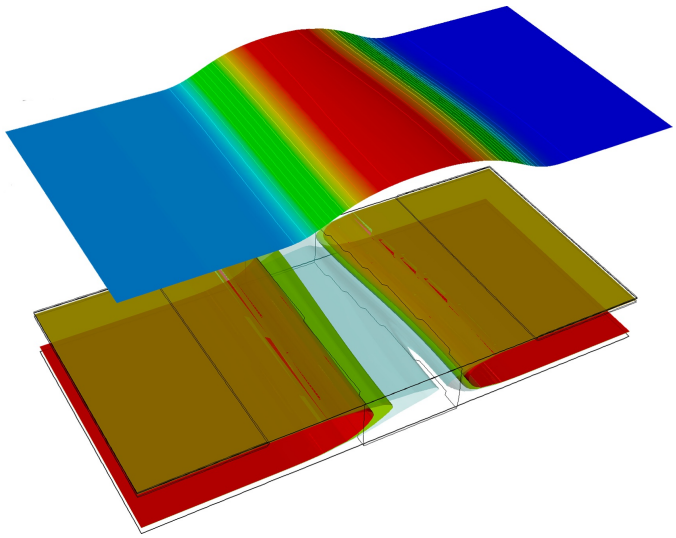


Figure 5.5 : Electron potential landscape and electron concentration surface in the body of the device in the existence of LER.

In the case of LER, the smoothness of the potential landscape is not affected, but there is variation in the shape of the potential barrier across the width of the device. In this particular case, one side of channel appears longer, which results in a reduction of electron concentration. At the other side of channel, the locally shorter channel provides a leakage path due to short channel effects. Therefore, LER principally affects the leakage and the DIBL of the transistor, through channel length variation and the corresponding short channel effects. It is worth noting that the variation of the gate edge position induced by LER has much larger length scale compared to the local modulation in the effective channel length due to redistribution of S/D-RDF as discussed in previous section. As a result, the impact of LER on DIBL should be more noticeable.

Figure 5.6 (a)-(c) illustrates the variation in gate transfer characteristics due to LER compared to the characteristics of an uniform transistor at 22nm, 16nm and 11nm gate length and under high drain bias condition. Large ensembles of 1000 devices are used to minimize statistical error. LER has a relatively mild impact on on-current variation, but has a substantial impact on the subthreshold region where the variation in the leakage current rapidly increases with scaling. This is complemented by increasing variations in the subthreshold slope.

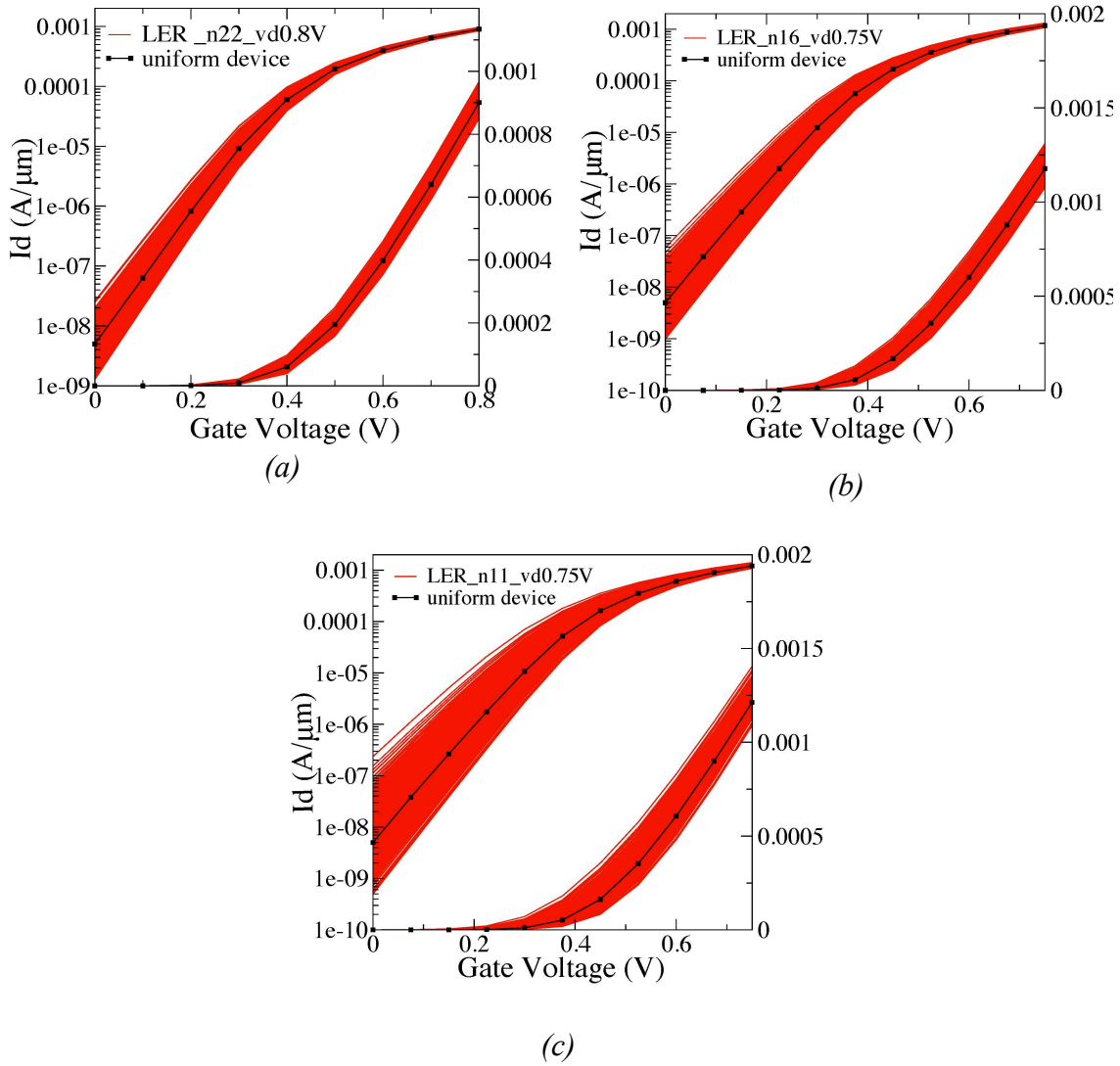


Figure 5.6 : Saturation transfer characteristics of (a) 22nm, (b) 16nm and (c) 11nm device ensembles under influence of LER.

LER affects the distributions of V_{th}, I_{on} and DIBL. The corresponding results are presented in the Figure 5.7 (a)-(c) for the transistors with three scaled: 22nm, 16nm and 11nm gate lengths. From the histograms, is clear that in the presence of LER the V_{th} and DIBL fluctuations are larger when comparing with RDF-induced variability due to the channel length variation across the width of the transistor. As expected, the distributions of V_{th}, I_{on} and DIBL become broader and the variability becomes substantial with the reduction of the device dimensions.

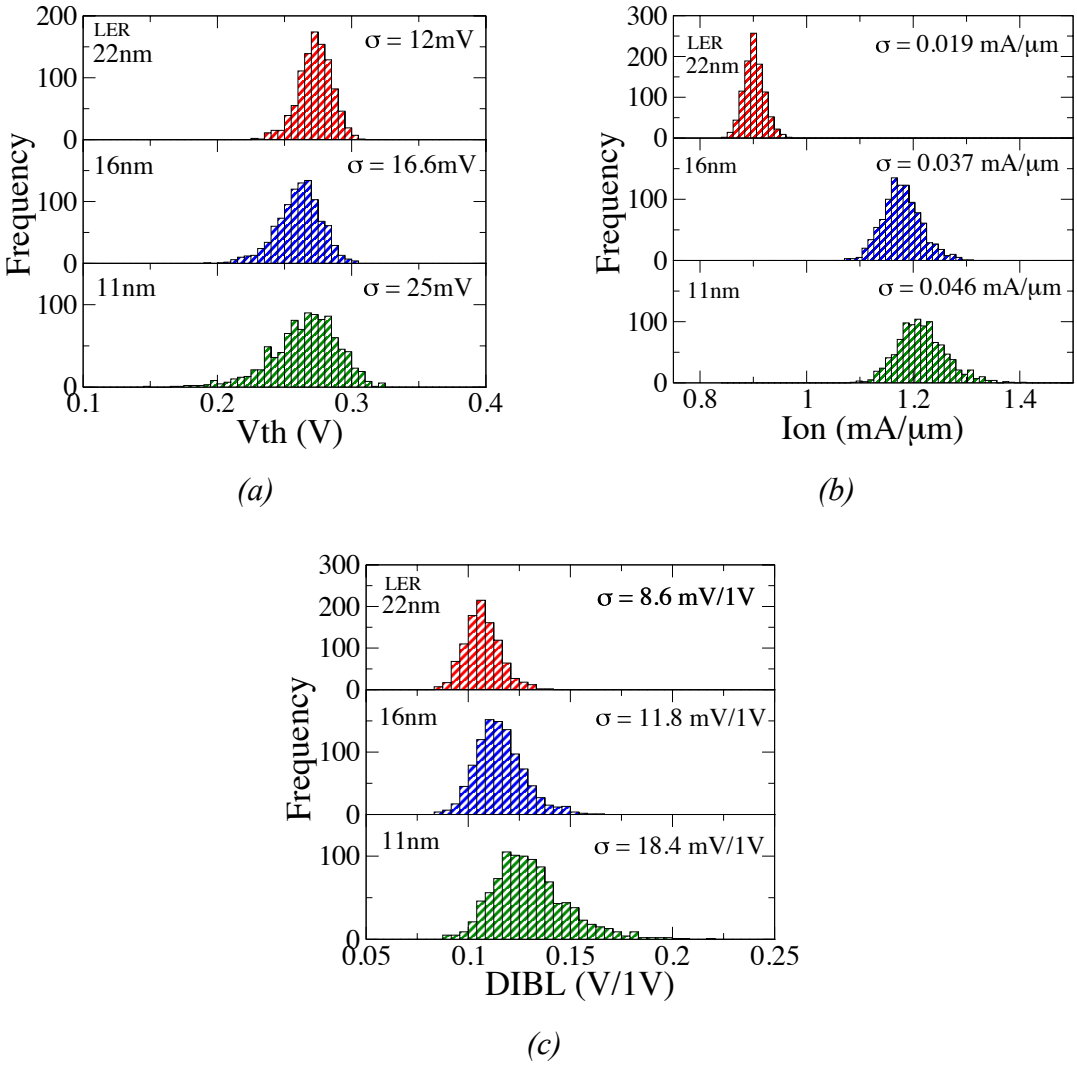


Figure 5.7 : Histograms of the impact of LER-induced fluctuations on (a) V_{th}, (b) I_{on} and (c) DIBL for 22nm, 16nm and 11nm devices.

5.2.3 Metal Gate Granularity (MGG) : 22nm, 16nm and 11nm

The introduction of high-k/metal gate stack allows further scaling of equivalent oxide thickness (EOT) without compromising the gate leakage performance [138], and thus directly improves the gate control over the channel. The transition from poly-silicon gate to metal gate has a favorable impact, significantly reducing the gate leakage, improving in the meantime the drive current. Nevertheless, from variability point of view, the presence of a metal gate can introduce a new variability source, the so called metal gate granularity (MGG). Figure 5.8 illustrates the electron potential landscape and the electron equi-concentration surface in the body of FD-UTB SOI transistor subjected to MGG. Here, the potential fluctuations due to grains of different work-functions affect the free carrier distribution in the entire depth of the silicon body of the transistor due to the thin silicon body. In particular, for a nMOSFET, a grain with a higher work-function blocks the formation of a channel under the gate, while a grain with lower work-function leads to the formation of a channel underneath, well before the nominal threshold condition for a uniform device. This results in both V_{th} and I_{on} variability introduced by MGG.

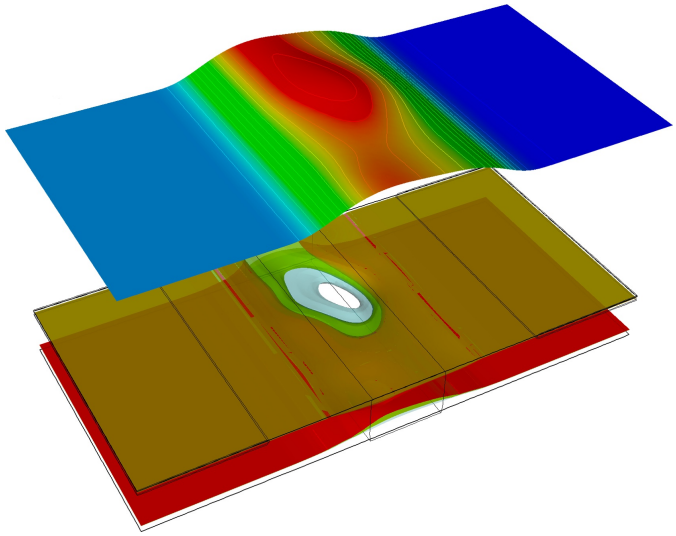


Figure 5.8 : Electron potential landscape and electron concentration surface in the body of the device in the presence of MGG.

The statistical simulations are carried out for an ensemble of 1000 microscopically different FD-UTB SOI transistors in order to study the impact of MGG on V_{th}, I_{on} and DIBL. Transistors corresponding to three different technology generations: 22nm, 16nm and 11nm were simulated. The full I_d-V_g characteristics of the corresponding transistors are presented in the Figure 5.9 (a)-(c). The impact of the work function variability is significant leading to a wider dispersions in the characteristics compared to the previously studied variability sources (RDF and LER). As usual, the degree of dispersion increases with smaller technology generation. An interesting feature is the almost parallel shift in the current-voltage characteristics of the statistical ensemble.

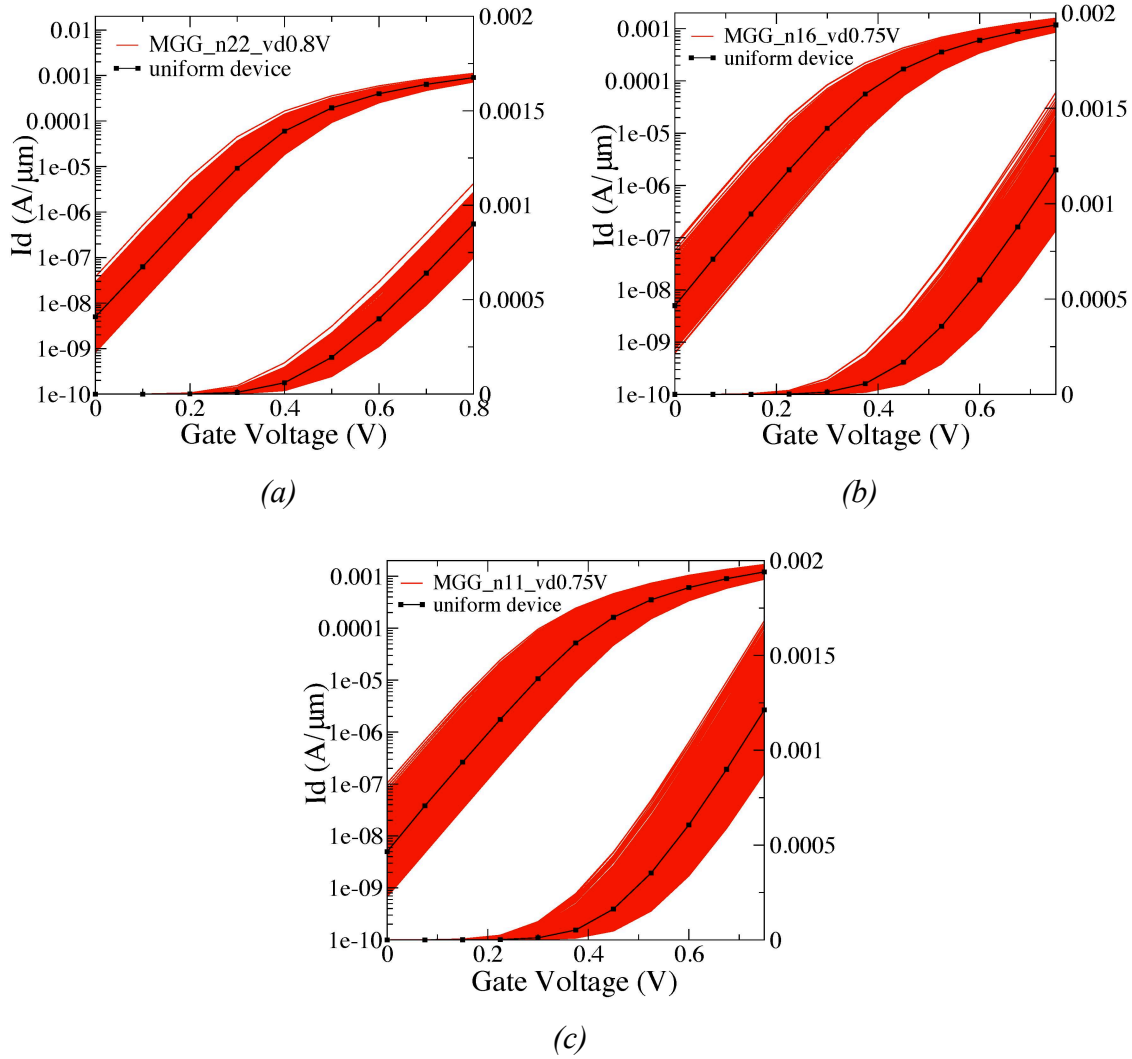


Figure 5.9 : Saturation transfer characteristics of (a) 22nm, (b) 16nm and (c) 11nm device ensembles under influence of MGG.

The statistical distributions of V_{th}, I_{on} and DIBL due to MGG as a single source of variability are presented in Figure 5.10 (a)-(c). As in the previous sections, three technology generations considered, with 22nm, 16nm and 11nm gate length devices. In general, the MGG on its own dominates the variation of V_{th}, I_{on} and DIBL compared to the other main variability including RDF and LER discussed previously. With the reduction of the gate length, the magnitudes of σV_{th}, σI_{on} and σDIBL increase.

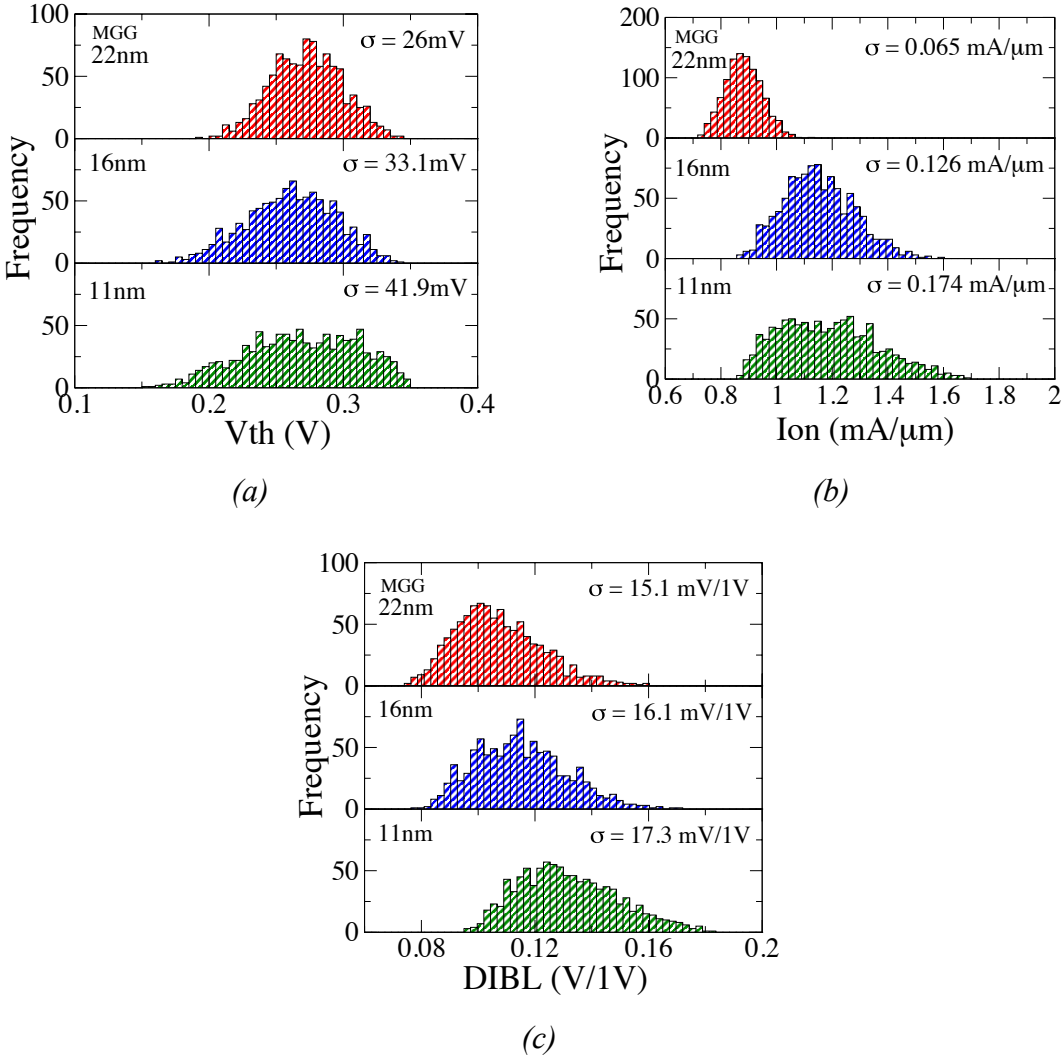


Figure 5.10 : Histograms of the impact of MGG-induced fluctuations on (a) Vth, (b) Ion and (c) DIBL for 22nm, 16nm and 11nm devices.

5.2.4 Combined variability sources WITHOUT MGG: 22nm,16nm and 11nm

In the previous sections, the impact of RDF, LER and MGG on V_{th}, I_{on} and DIBL are explored in the presence of individual variability sources. In this sub-section, the impact of combined effect of RDF and LER is investigates in the absence of MGG. This simulation case is important because the MGG is the metal gate granularity formed by high temperature annealing, which increases the statistical variability. In the gate-first process, metal gate will undergo the source/drain high temperature annealing, leading to MGG. Contrarily, in the gate-last process, the metal gate is formed after source/drain annealing, which can reduce significantly the MGG effects. These two gate processes co-exist, and the simulation without MGG is relevant to the gate-last process.

The devices under study are the 22nm, 16nm and 11nm gate lengths UTB SOI MOSFETs. The statistical simulations ensembles of 1000 of microscopically different transistor are performed. The complete transfer characteristics for three technology generations including the characteristics of the uniform device are shown in Figure 5.11 (a)-(c). The spread of the current voltage characteristics in Figure 5.11 (a)-(c) for the combined effect of RDF and LER is similar to the individual LER in Figure 5.6 (a)-(c) for three technology generations at subthreshold region, while at on-current region, RDF is the dominant variability source. It can be assumed that the combination of variability sources could markedly enhance the effect of a single variability source. For instance, when combining RDF and LER, LER have more prominent impact on V_{th} and DIBL compared to the RDF effect. The RDF effects are more pronounced in the case of I_{on}. The histograms in Figure 5.12 (a)-(c) show the distributions of V_{th}, I_{on} and DIBL resulting from the combined impact of RDF and LER. For all set of devices, the standard deviations of V_{th}, I_{on} and DIBL increase with reduction of the channel length. The increase in the statistical parameter fluctuations in the scaled devices impose increasing limitations on the device performance with scaling.

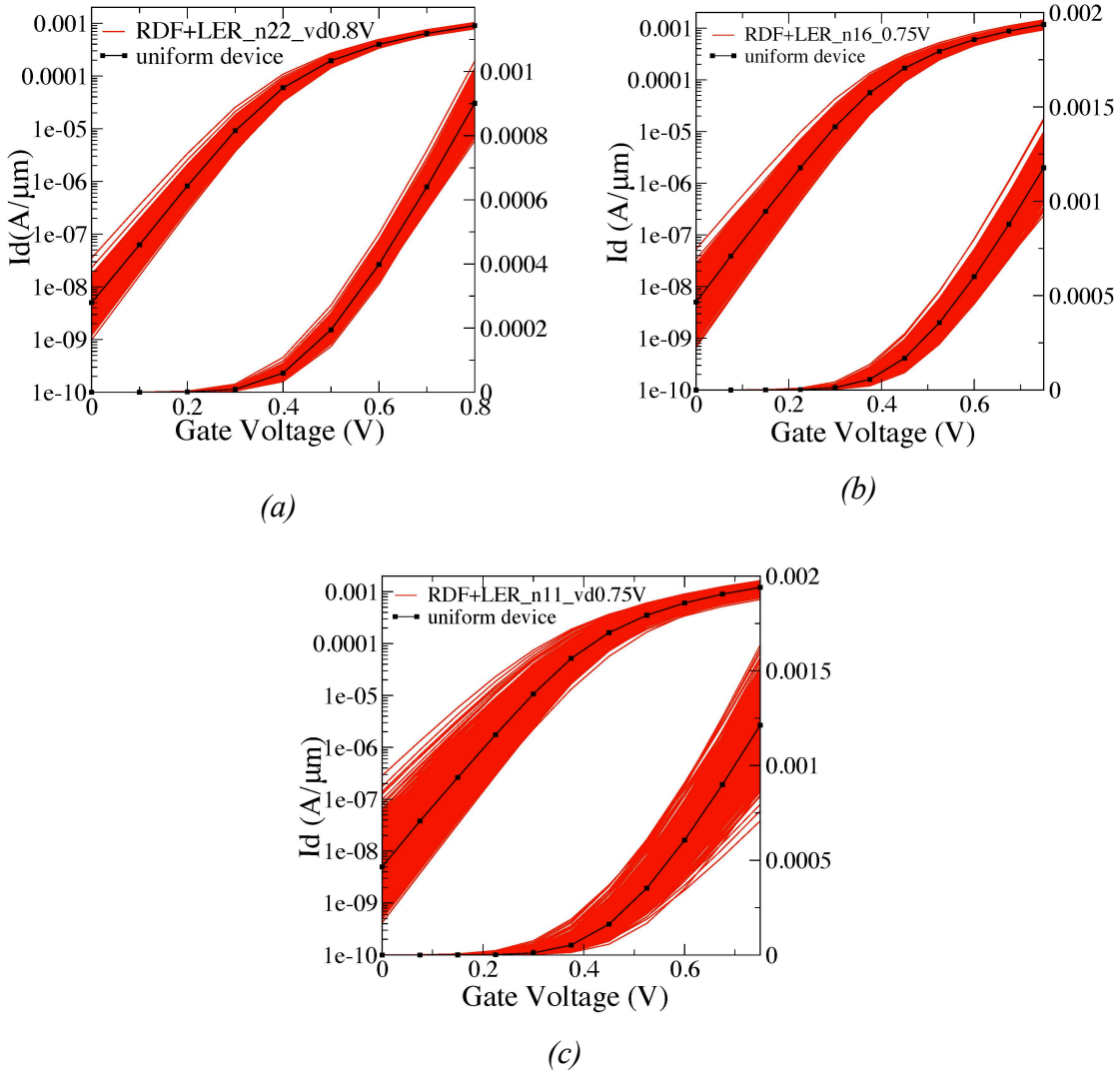


Figure 5.11 : Saturation transfer characteristics of (a) 22nm, (b) 16nm and (c) 11nm device ensembles under influence of combined variability sources; RDF+LER.

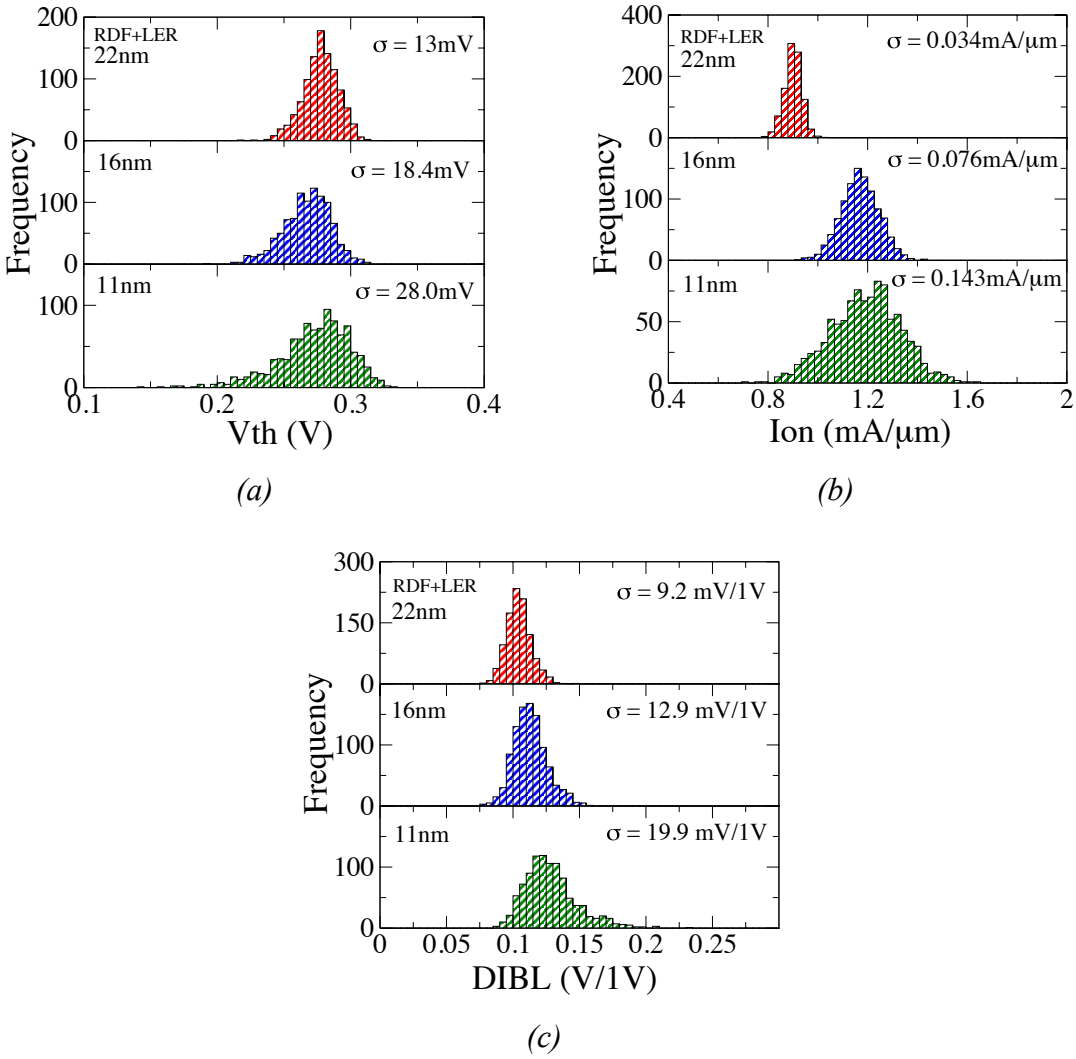


Figure 5.12 : Histograms of the impact of RDF+LER-induced fluctuations on (a) V_{th}, (b) I_{on} and (c) DIBL for 22nm, 16nm and 11nm devices.

The scatter plots of V_{th} versus I_{on} for 22nm, 16nm and 11nm gate lengths transistors under the influence of RDF, LER individually and in combination are shown in Figure 5.13 (a)-(c). There is almost perfect correlation between V_{th} and I_{on} in the case of LER, but its interplay with RDF significantly broadens the cloud particularly at high threshold voltage. Meanwhile, S/D-RDF significantly weakens the correlation between both variables. The spreading of the cloud at high threshold voltage in the presence of RDF is caused by two different phenomena that may work against each other. The first reason is high access resistance due to S/D-RDF and the second reason is high threshold voltage due to spurious acceptors in the channel [139].

Generally, the correlation trend for each technology generation is almost similar, except for combined of RDF and LER at 11nm gate length, where the V_{th} and I_{on} are less correlated (ρ = -0.64) compared to (ρ = -0.76) for both 22nm and 16nm gate lengths. This is due to the dramatically reduced transistor size.

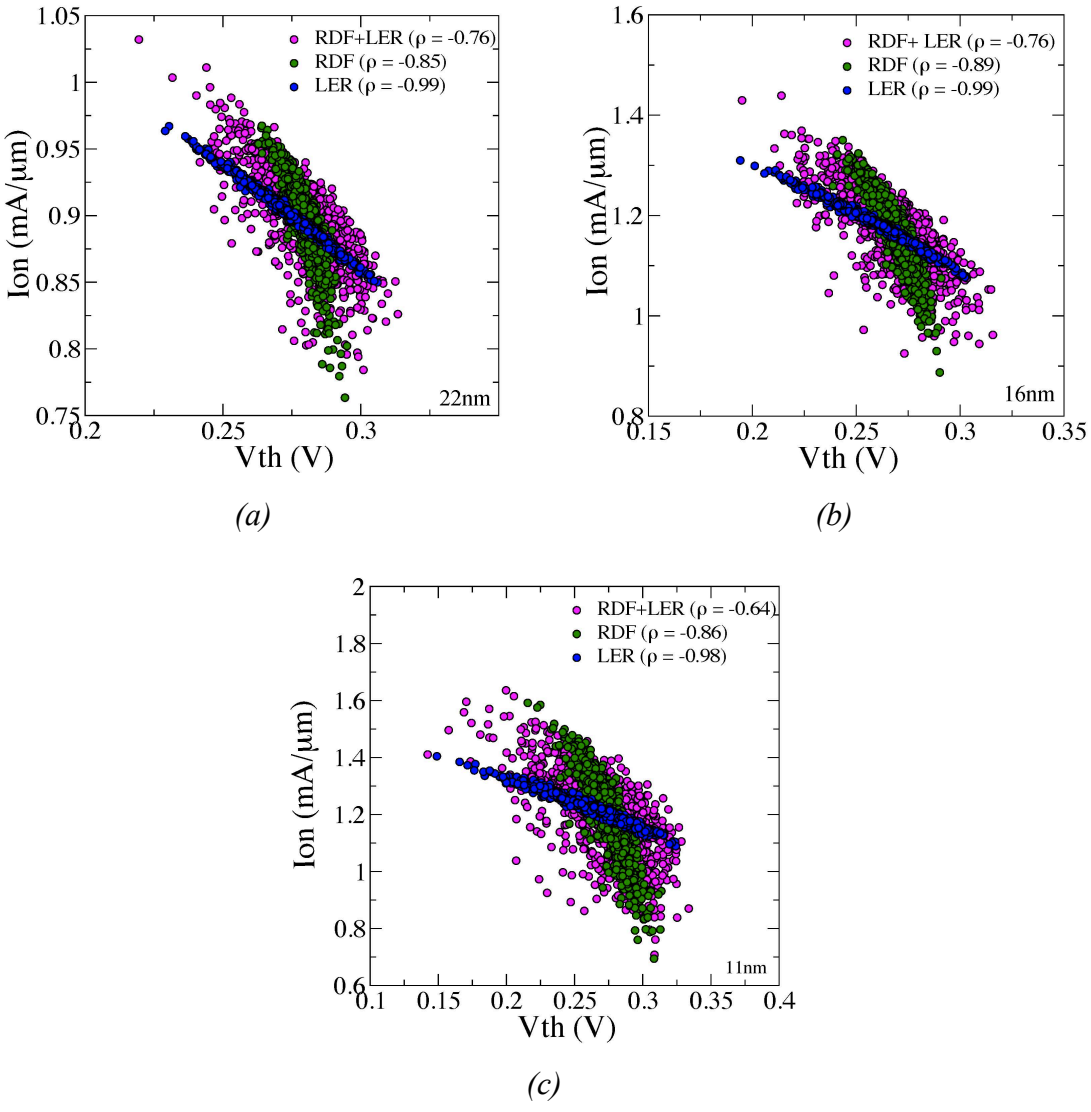


Figure 5.13 : Scatter plots of I_{on} versus V_{th} at saturation for the device ensembles with RDF, LER and RDF + LER for (a) 22nm, (b) 16nm and (c) 11nm devices.

5.2.5 Combined variability sources WITH MGG: 22nm,16nm and 11nm

Finally, the impact of the all combined variability sources (RDF, LER and MGG) on V_{th}, I_{on} and DIBL is analysed in this sub-section, where the device with gate lengths of 22nm, 16nm and 11nm are considered as usual. Figure 5.14 shows the combined effect of the three main sources of statistical variability. For reference, the same LER (3σ = 2nm, λ = 25nm) and MGG (grain size, $\varnothing$ = 5nm) patterns are used as in the previous sections (5.2.2 and 5.2.3). However, in combination, they have complex impact on the potential landscape and the carrier distribution.

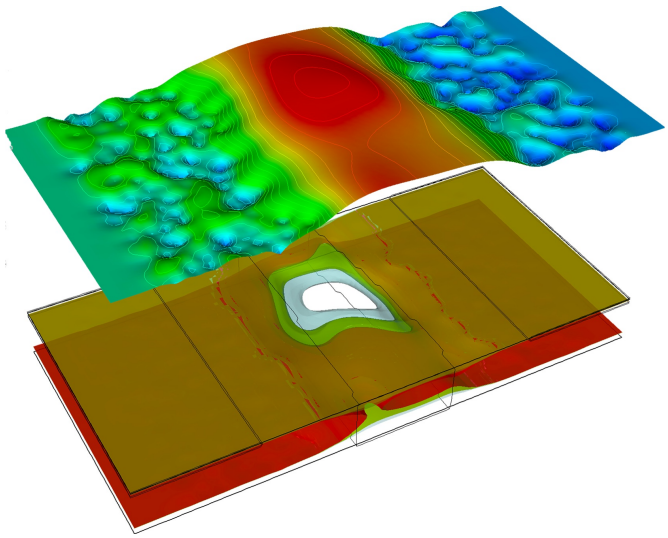


Figure 5.14: Electron potential landscape and electron concentration surface in the body of the device in the presence of combined variability sources; RDF+LER+MGG.

The results of this simulations are presented in Figure 5.15 (a)-(c) showing an ensemble of 1000 simulated I_d-V_g characteristics of 22nm, 16nm and 11nm gate lengths transistors in saturation region, subjected to combined variability sources (RDF, LER and MGG).

It can be observed that the variation of the leakage current becomes larger as the device dimensions are scaled down. For example, the variation in leakage current has spanned four orders of magnitude for 11nm gate length, compared to two orders of magnitude for 22nm and three orders of magnitude of 16nm gate lengths. The wide range of distribution of the I_d-V_g characteristics indicates that the influence of statistical variability becomes more dramatic when MGG is taken into account.

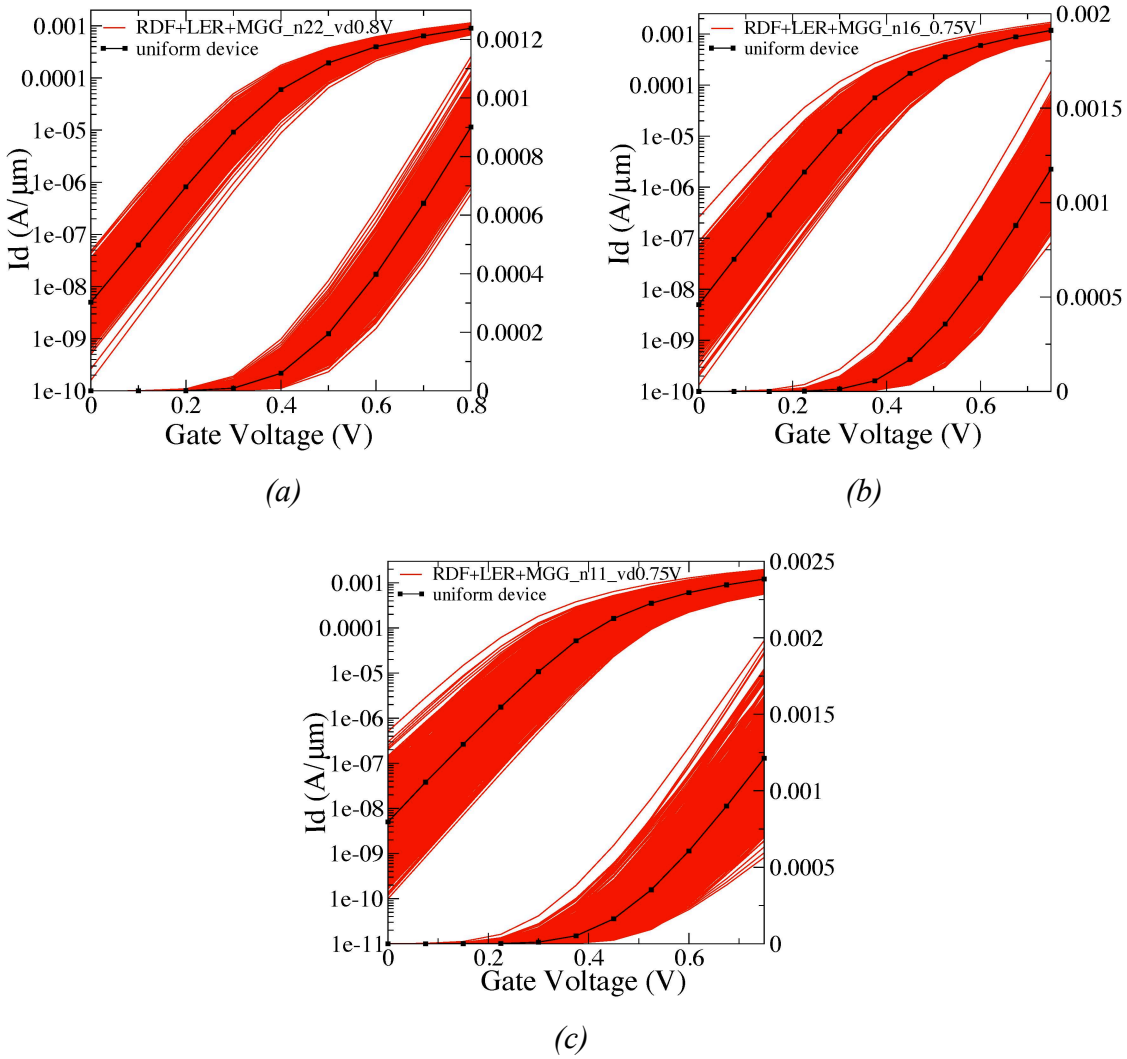


Figure 5.15 : Saturation transfer characteristics of (a) 22nm, (b) 16nm and (c) 11nm device ensembles under influence of combined variability sources; RDF+LER+MGG

The statistical distributions of V_{th}, I_{on} and DIBL for 22nm, 16nm and 11nm FD-UTB SOI devices under the combined impact of all the variability sources are presented in Figure 5.16 (a)-(c). As expected, the standard deviations of V_{th}, I_{on} and DIBL escalate with the reduction in the gate length. Please also note that, MGG is by far the most dominant factor for V_{th}, I_{on} and DIBL fluctuations. In spite of this, other sources of variability cannot be underestimated and ignored.

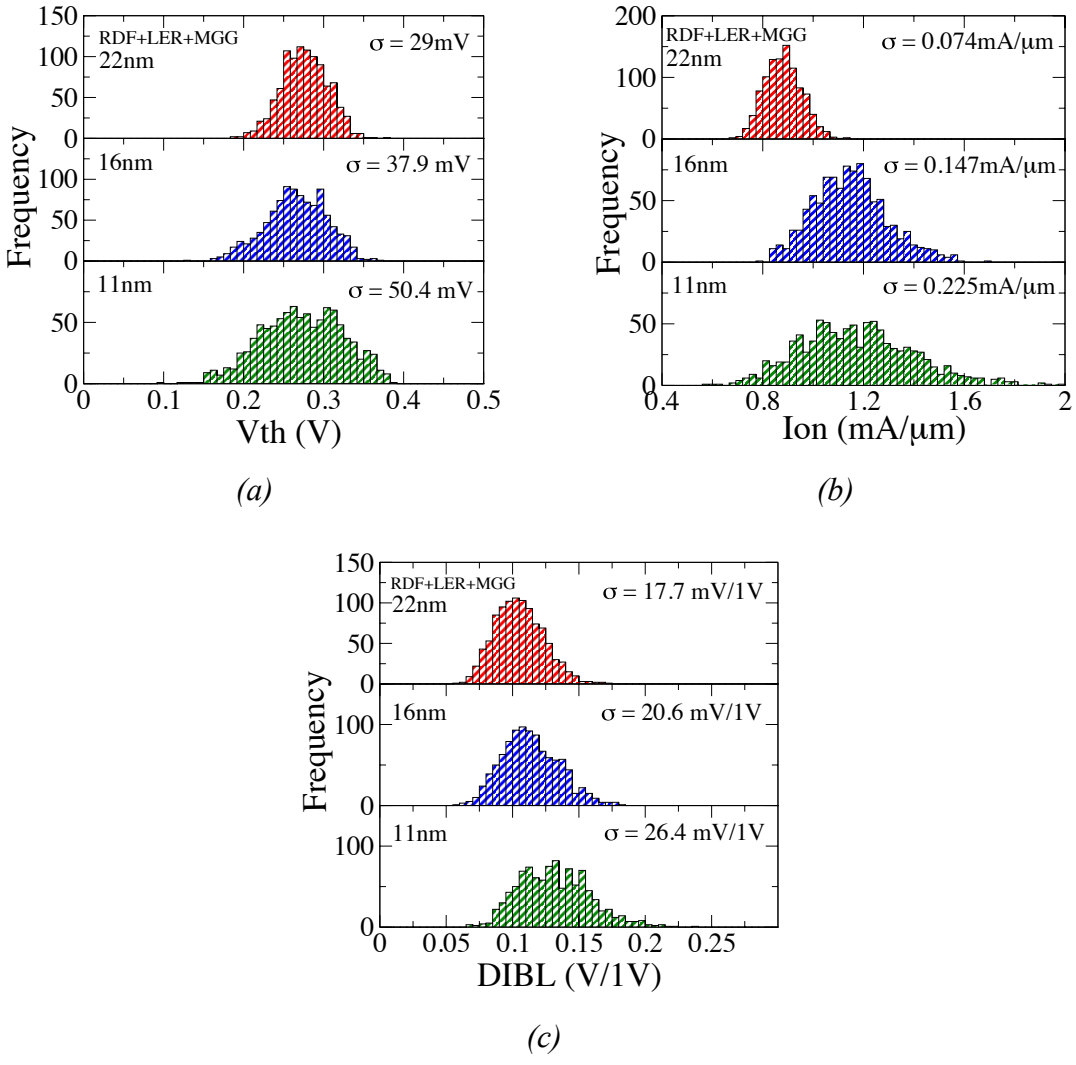


Figure 5.16 : Histograms of the impact of RDF+LER+MGG-induced fluctuations on (a) V_{th}, (b) I_{on} and (c) DIBL for 22nm, 16nm and 11nm devices.

In order to provide a better understanding, Figure 5.17 (a)-(c) illustrate the scatter plot of I_{on} versus V_{th} for the simulated devices with different combination of variability sources. The correlation coefficients are reported in the legend. The scatter plot of I_{on} versus V_{th} includes of 22nm, 16nm and 11nm gate length devices. Because of MGG dominates the variability of I_{on} and V_{th}, it appears that it increases the correlation between the two variables, compared to the correlation observed in the ensemble for combination of RDF and LER only. In addition, due to the dominant impact of MGG on I_{on} and V_{th} , it shows that the MGG restores the correlation between both variables. This trend applies to all technology generations under study.

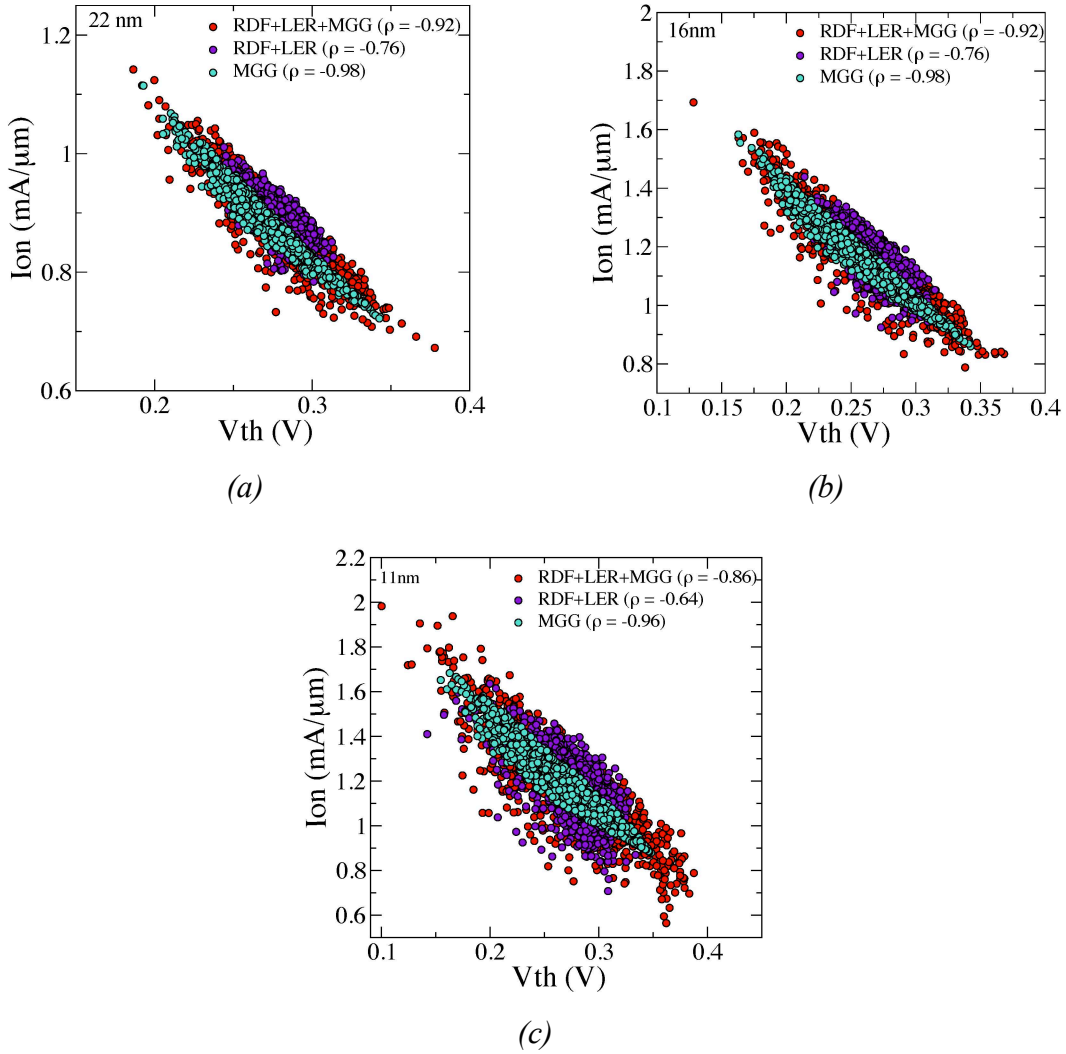


Figure 5.17 : Scatter plots of I_{on} versus V_{th} at saturation for the device ensembles with MGG, RDF+LER and RDF+LER+MGG for (a) 22nm, (b) 16nm and (c) 11nm devices.

For a clearer overall information, Figure 5.18 (a)-(c) and Table 5.1 have summarized the gate length dependence of σV_{th}, σI_{on} and σDIBL for different variability sources, treated as single source and also in combination.

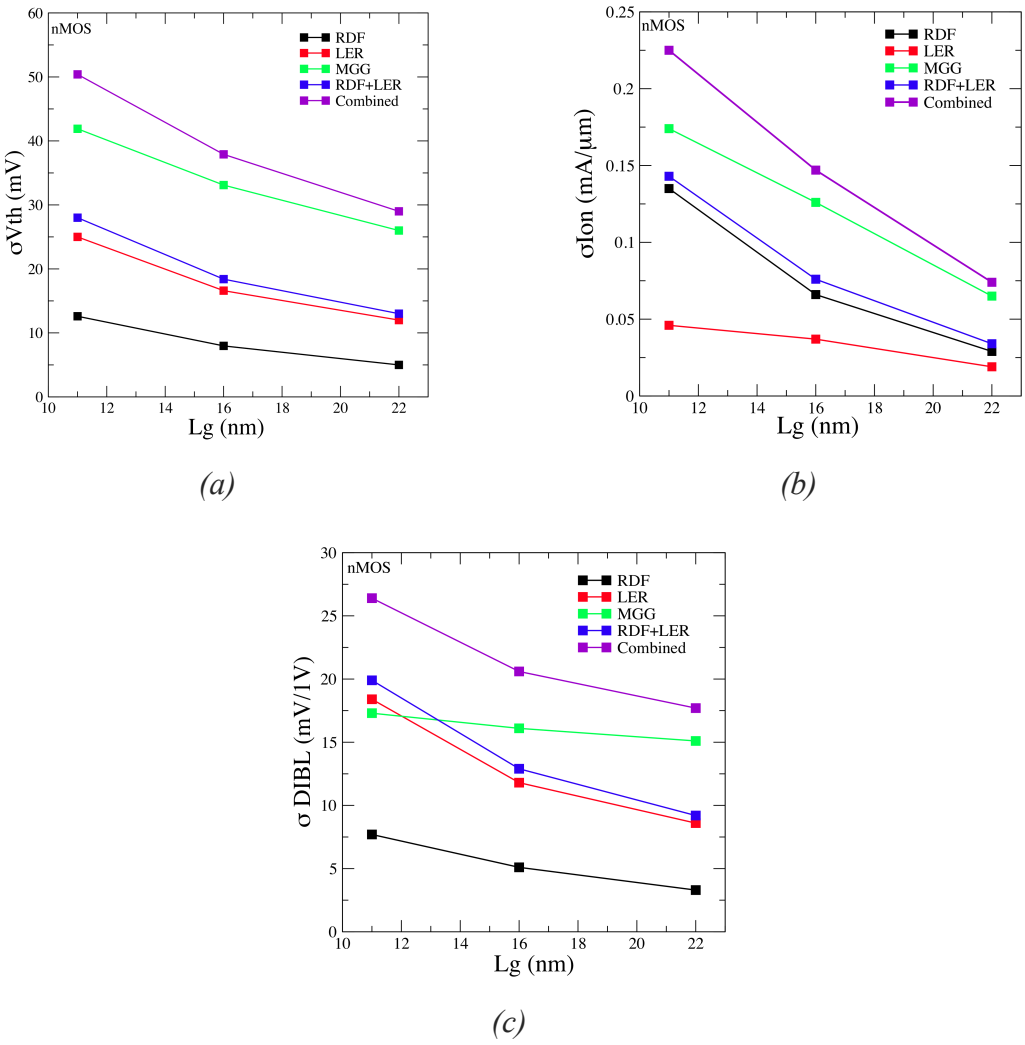


Figure 5.18 : The gate length dependence of σV_{th}, σI_{on} and σDIBL for different variability sources in saturation mode.

Table 5.1 : Variability in performance of 22nm, 16nm and 11nm FD-UTB SOI devices.

Parameters	σV_{th} (mV)			σI_{on} (mA/μm)			σDIBL (mV/1V)		
Ensemble	22nm	16nm	11nm	22nm	16nm	11nm	22nm	16nm	11nm
RDF	5	7.97	12.6	0.029	0.066	0.135	3.3	5.1	7.7
LER	12	16.6	25.0	0.019	0.037	0.046	8.6	11.8	18.4
MGG	26	33.1	41.9	0.065	0.126	0.174	15.1	16.1	17.3
RDF + LER	13	17.6	27.3	0.034	0.076	0.141	9.1	12.6	19.8
RDF + LER + MGG	28	37.9	51.3	0.073	0.146	0.226	18.3	21.4	26.6

5.3 Summary

This chapter describes a comprehensive simulation study of the statistical variability of scaled FD-UTB SOI devices with the gate lengths of 22nm, 16nm and 11nm. The impact of RDF, LER and MGG on V_{th}, I_{on} and DIBL are analysed individually as well as in combination. Results reveal that MGG is the dominant variability factor for all critical electrical parameters of all channel lengths if a gate first process is considered. For instance, in the shortest gate length transistor, the MGG on its own dominates the V_{th} and I_{on} variations by 53% and 23% more variability when compared to the RDF leading to LER respectively. With the reduction of the gate length the magnitudes of σV_{th}, σI_{on} and σDIBL increase. As an example, σV_{th} due to MGG increases from 26.0 to 41.9 mV with the reduction of the gate lengths from 22nm to 11nm respectively. However, both RDF and LER have important role in determining the fluctuations of I_{on} and DIBL respectively. Therefore, none of these sources of statistical variability can be neglected for low power, high performance FD-UTB SOI transistors and the corresponding circuit design.

CHAPTER 6

Simulation Study of Statistical Reliability

6.1 Introduction

"*Is future CMOS technology still reliable with scaling?"*. Companied with the excitement of reducing the transistor size in order to improve performance, enlarge the chip integration capacity and minimize power consumption, a variety of challenges arise in horizon. Apart from the increasing importance of statistical variability issues, the generation of defect states at the channel interface or in the gate stack dielectric is becoming a serious concern especially for the lifespan of nanoscale devices [36, 140, 141]. The trapping of individual or multiple charges on defect states results in a degradation of transistors performance figures of merit and, in turn, introduces severe reliability problems in SRAM [142], Flash memories [143] and analog basic blocks [144].

In this chapter, by using the 3D density-gradient (DG) quantum-corrected 'atomistic' drift-diffusion (DD) simulator GARAND [91], we study the impact of dominant variability sources in combination with reliability issues associated with positive bias temperature instability (PBTI) in n-channel FD-UTB SOI scaled devices. In order to evaluate the trends of variability and reliability with scaling, we carry out our simulation study on three devices featuring a gate length of 22nm, 16nm and 11nm (designed aspects have been discussed thoroughly in Chapter 4). We take into account RDF, LER and MGG as main sources of statistical variability (implementation details have been described in Chapter 5). Large ensembles of 1000 FD-UTB SOI n-channel transistors are used in order to improve the statistical accuracy. Three degradation levels are explored, considering progressively increasing trapped charge densities of 1e11cm^{-2}, 5e11 cm^{-2} and 1e12 cm^{-2} of the gate oxide interface that represent early, medium and late degradation stages. The impact of combined variability sources on the transistor threshold voltage (V_{th}), on-current (I_{on}) and drain induced barrier lowering (DIBL) is evaluated for each degradation level. The simulations are carried out in the contact of two possible scaling scenarios, differentiated by the presence or absence of MGG as a variability source in future CMOS technology.

6.2 Reliability Issues and Future Challenges

With the physical gate length of the contemporary CMOS transistors entering nanometer scale, fundamental physical limitations start to influence the operation of the transistors [145]. The crucial issues affecting contemporary transistors are the intrinsic statistical variability that has been discussed in previous chapters and performance degradation due stress [146] [147]. Over a period of time, the stress related device performance deterioration causes reliability problems.

Reliability is becoming a hot subject to chip designers in present and emerging technology generations, where the reliability issues should be verified and tackled early in the design process. An accurate knowledge of the statistical reliability issues is necessary and important in order to predict circuit performance degradation during its

lifetime. A common type of degradation is related to defect states at the Si/SiO_2 interface or in the dielectric stack resulting in Bias Temperature Instability (BTI) [148] [149]. Depending on the operation conditions, these defect states can trap charge carriers above the channel, introducing progressive changes in the transistor's electrical characteristics which influence its operational lifetime. For instance, a 3D simulation [150] and experimental studies [143] have shown that the trapping of a single charge carrier in a short channel transistor can cause substantial changes in the transistor's characteristics. It was reported in [151] that threshold voltage shifts as large as 0.5V can be observed in flash memories. Apart from that, the charge trapping occurs mainly because of an electron injection into the insulator as a result of applied electrical stress to the device. The trapped charge build up as far as the stress condition is present leading to critical parameter drift and potential yield loss [152]. On the other hand when the BTI conditions are removed, significant fraction of the trapped charges can be emitted leading to BTI relaxation leaving relatively small permanent trapped charge level as illustrated in Figure 6.1 at the end of the BTI relaxation [153], [154].

The adoption of high-k/metal gate stack in contemporary CMOS technology has resulted in remarkable improvements in terms of electrostatic integrity, variability and device performance [15, 34, 133, 138]. The high-k dielectrics allow to increase the physical thickness of the gate stack at particular EOT, and hence to reduce significantly the gate leakage [155] [156]. This however can be complemented by a reduction of the channel mobility, and fixed charge and trapping-induced instability, which have to be understood and characterized [157] [158].

The BTI degradation can be observed in both p-channel and n-channel transistors with high-k gate stacks. Charge trapping under positive bias stress is associated with electron trapping in n-channel MOSFET, and is called PBTI. Meanwhile, for p-channel MOSFET, the degradation happens when the transistor is stressed with negative gate voltages, and is called negative bias temperature instability (NBTI). The temperature condition at which a particular device is stressed for NBTI measurements depends on the transistor type and application. BTI experiments have been performed under a wide range of temperature conditions (25 – 200^{o}C) as presented in [159], [153], [160].

Despite constant improvements on the quality of the high-k gate dielectric, the higher trap density still results in a significant charge trapping [161] [162].

Due to the discrete charge trapping associated with the PBTI/NBTI degradation, there is additional variation in the transistor figures of merit such as the threshold voltage [163] and the on-current [164]. In addition, the impact of a particular trapped charge distribution on the transistor behavior will be influenced by the presence of other underlying variability sources. Therefore, considering together the static and the dynamic statistical variability is very important when studying fluctuation-resilient FDSOI transistors in this thesis.

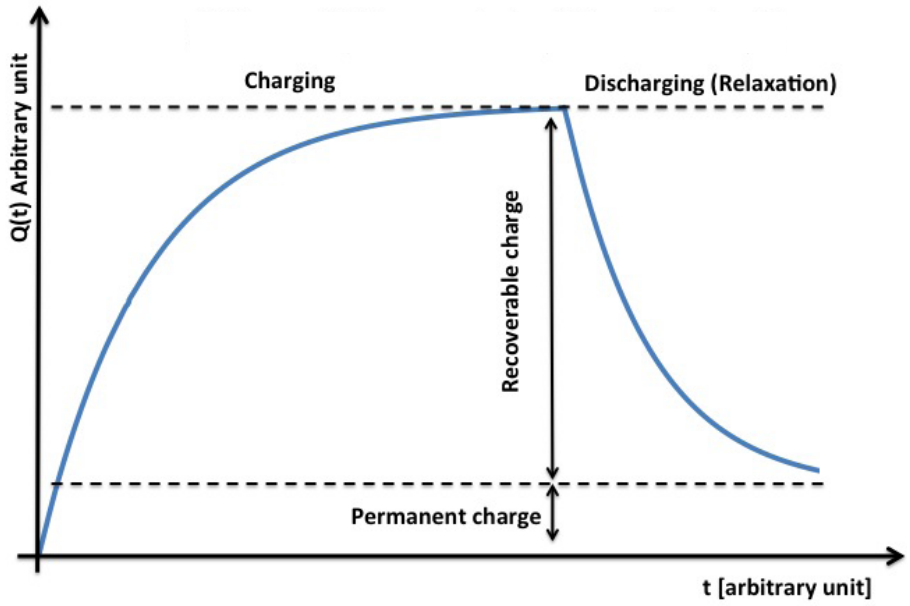


Figure 6.1 :Schematic dependence of the trapped charge density as a function of time during the degradation and relaxation BTI stages.

6.3 Statistical Reliability Simulations in the Absence of MGG

This section reports the simulation results of PBTI variability associated with fixed/trapped random negative charges in concert with RDF and LER. The impact of MGG is excluded in this section, assuming a metal gate-last technology which can result in an amorphous metal gate [165]. Random trapped charges are introduced to the ensemble of 1000 'fresh' microscopically different transistors with 22nm, 16nm and 11nm gate lengths. Three different levels of PBTI degradation are investigated corresponding to interface trapped electron charge densities of:

- 1e11 cm^{-2} - early degradation
- 5e11 cm^{-2} - intermediate degradation
- 1e12 cm^{-2} - late degradation

The PBTI degradation progresses by trapping of electrons on pre-existing defect states and the generation of new defect states. Here, we consider frozen in time simulations, corresponding to the above three levels of degradation.

We assume that the charges are trapped at the silicon/silicon dioxide (Si/SiO_2) interface. In order to generate random number and positions of the trapped charges a fine auxiliary two-dimensional (2D) mesh is imposed at the interface. Both the number of trapped charges and their individual positions are randomly assigned from device to device, according to the average trapped charge density. For this purpose, a rejection technique is used at every node of the auxiliary mesh to determine if a single negative charge is located at that node or not based on the charge density. If it is determined that a single charge should be placed there, then its electronic charge is assigned to the surrounding nodes of the 3D discretization mesh using a cloud in cell (CIC) charge assignment scheme [166].

Figure 6.2 illustrates the simulation of one particular random configuration of charges in an n-channel FD-UTB SOI in presence of RDF and LER. Note that, the spikes at the site of trapped charges reduce the local carrier concentrations and thus cause the local current reduction.

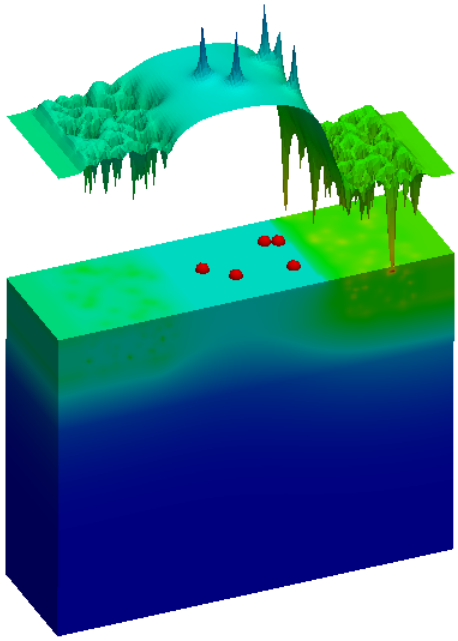


Figure 6.2 : The electrostatic potential of 22nm FD-UTB SOI nMOSFET that includes RDF and LER at interface-trapped charge density of 1e12 cm^{-2}. The trapped charges are shown in red colour. (W/L=1)

Simulation results of the impact of an increasing trapped charge density (N_{it}) in the presence of RDF and LER are presented. Figures 6.3 to Figure 6.5 illustrate the gate transfer characteristics at high drain bias for the ensemble of transistors with 22nm, 16nm and 11nm gate lengths respectively, with combined RDF, LER variability sources at different level of BTI degradation stages. All I_dV_g are presented in linear and logarithmic scales, to demonstrate the impact of BTI at both sub-threshold and on-current regions.

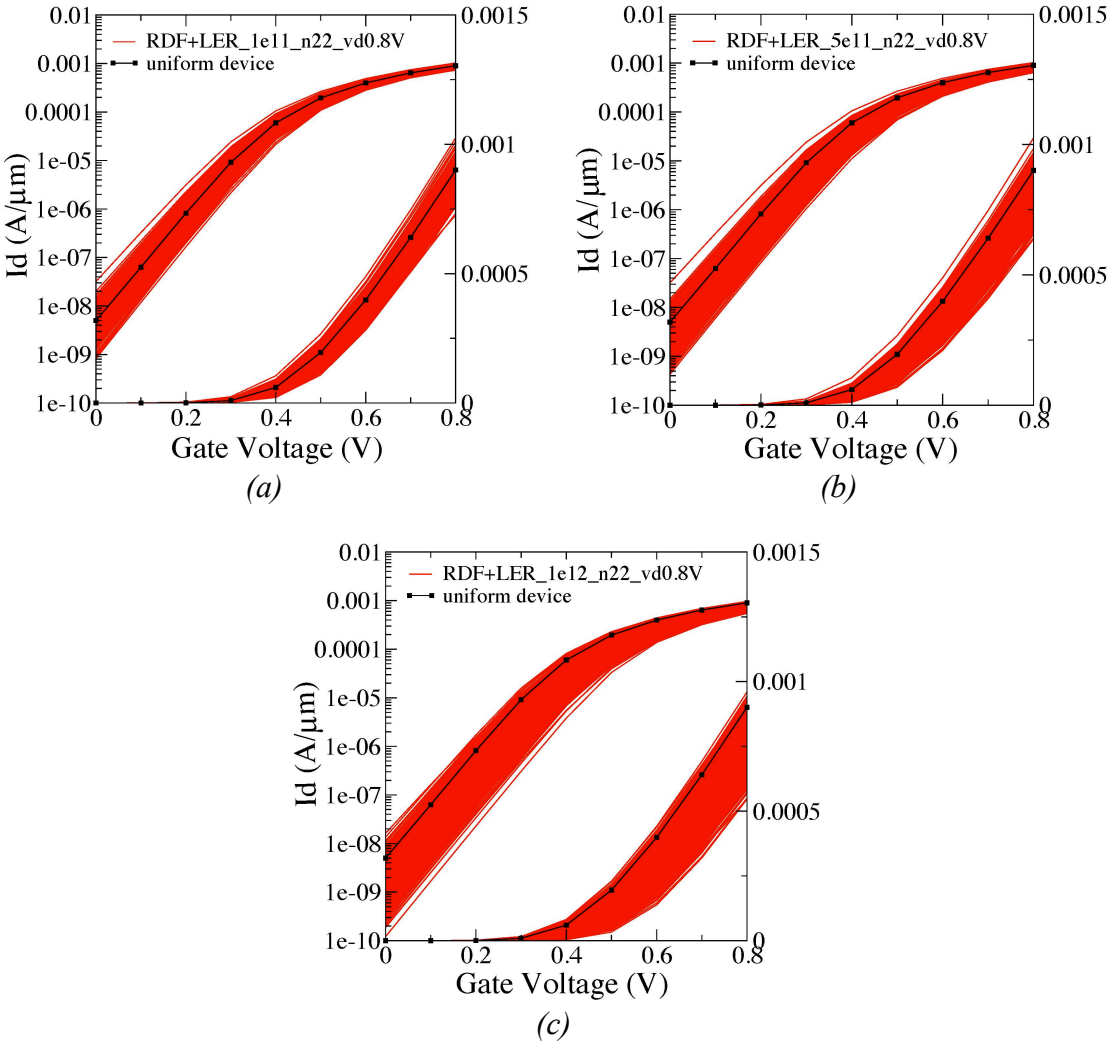


Figure 6.3 : I_dV_g of 1000 devices with RDF, LER and increase of PBTI degradations (a) 1e11cm^{-2} (b) 5e11cm^{-2} and (c) 1e12cm^{-2} for 22nm gate length.

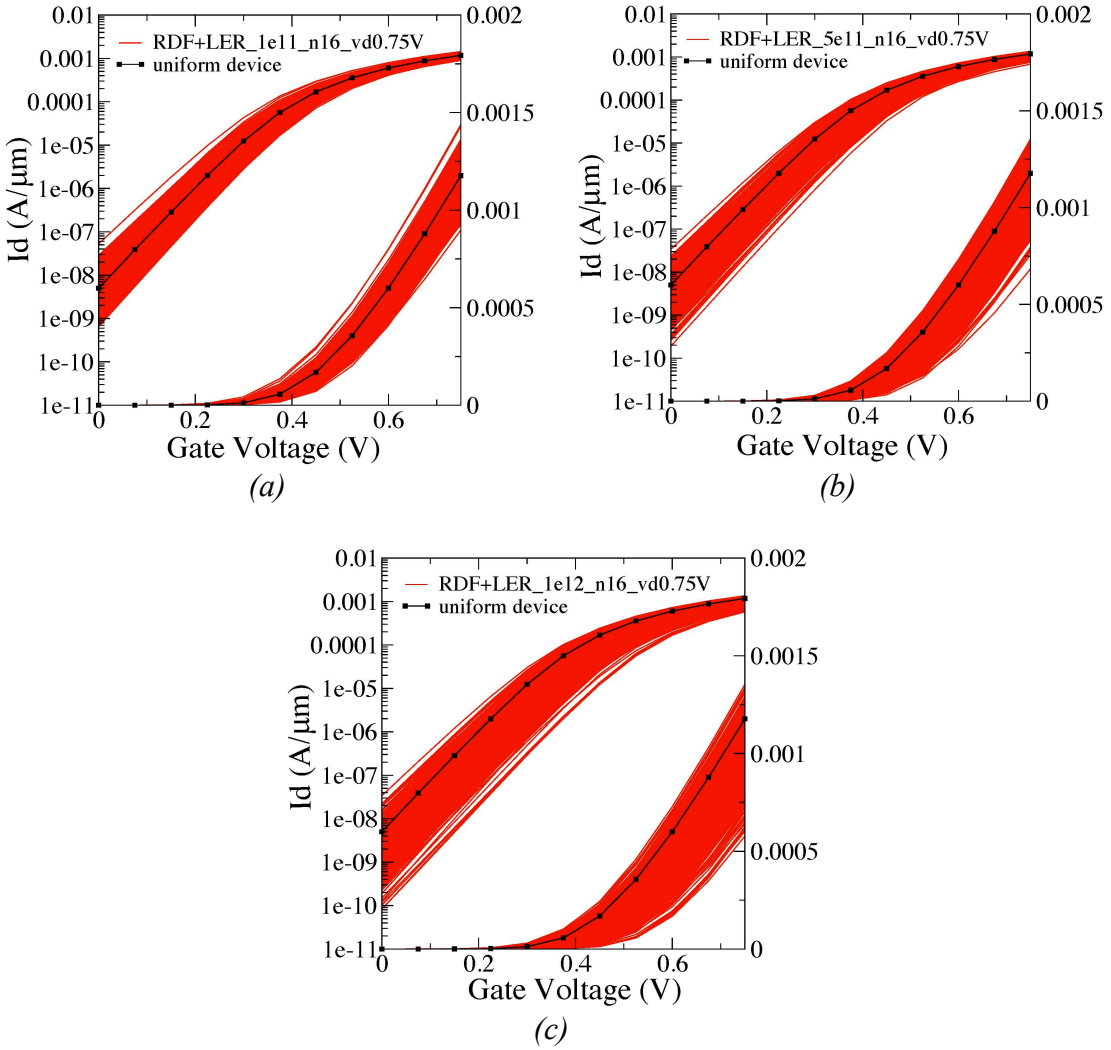


Figure 6.4 : I_dV_g of 1000 devices with RDF, LER and increase of PBTI degradations (a) 1e11cm^{-2} (b) 5e11cm^{-2} and (c) 1e12cm^{-2} for 16nm gate length.

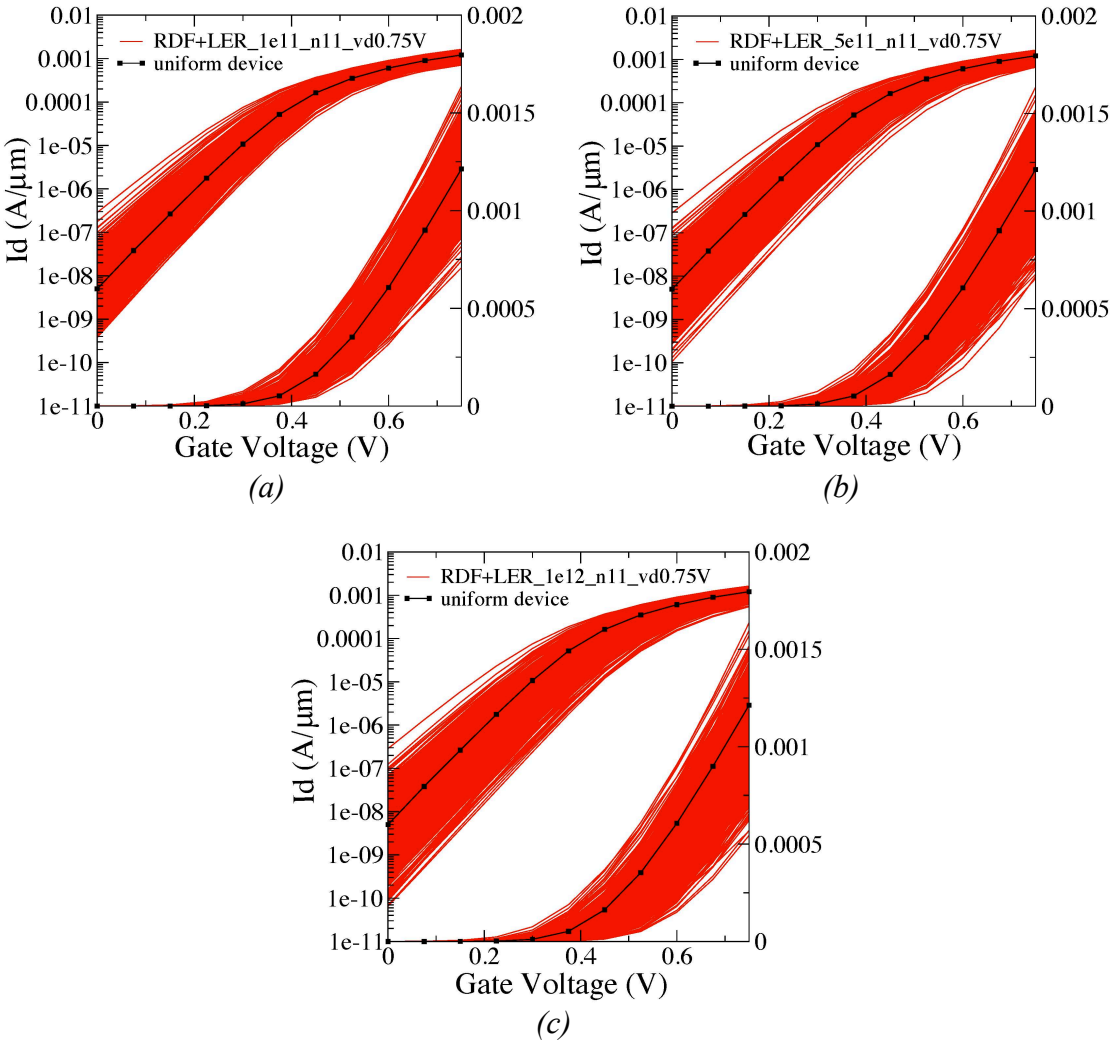


Figure 6.5 : I_dV_g of 1000 devices with RDF, LER and increase of PBTI degradations (a) 1e11cm^{-2} (b) 5e11cm^{-2} and (c) 1e12cm^{-2} for 11nm gate length.

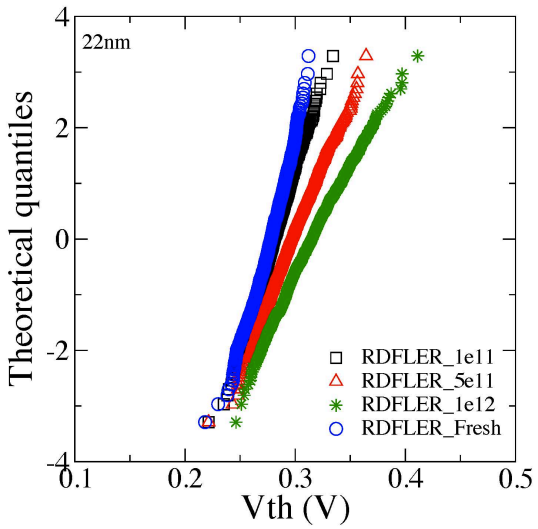
Figures 6.3-6.5 clearly show that both the gate length scaling and degradation broaden the dispersion in the I_dV_g characteristics. The maximum on-current is three times larger than minimum on-current in the 11nm transistor at high degradation level, which could lead to serious timing issue in digital application.

For a better understanding of the impact of PBTI on the transistor characteristics, Figures 6.6 to Figure 6.8 show the normal QQ-plots of the V_{th}, I_{on} and DIBL distributions for the three technology generations FD-UTB SOI transistors subjected to the various levels of trapped charge in concert with the presence of RDF and LER.

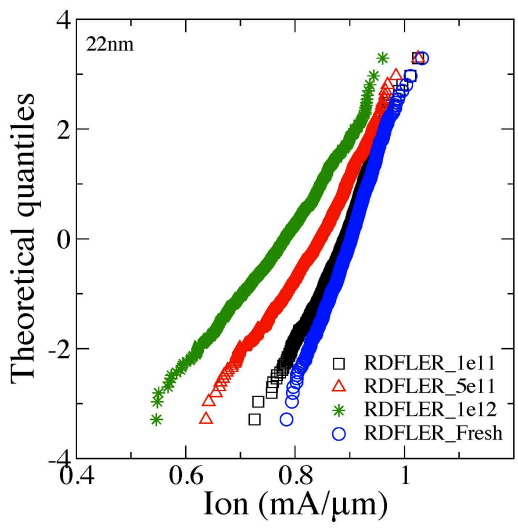
In the case of the V_{th} distributions, a clear change in the slope of the distribution is observed, highlighting an increase in the dispersion with the increase in trapped charge density. As expected, the distributions shift with the increase of trap charge density due to the PBTI degradation induced average threshold voltage increase. Note that, the upper tail of threshold voltage distribution at the late degradation stage (1e12 cm^{-2}) deviates from normal distribution due to the interaction of multiple trapped charges.

The effect of the trapped charge is further illustrated in respect of the I_{on} degradation. The I_{on} distributions are skewed to the left with a prolonged lower tail, which is in agreement with the V_{th} skewness. This indicates that the current amplitude decrease with the increase in the degradation level. The trapped charge blocks the current conduction paths effectively increasing the threshold voltage, and hence reduce the amount of current flow.

Apart from V_{th} and I_{on} shift due to PBTI degradation, the DIBL is also affected by the trapped charge induced degradation. The QQ-plots for DIBL reveal that although the mean value of DIBL is almost unchanged, the distribution becomes wider.



(a)



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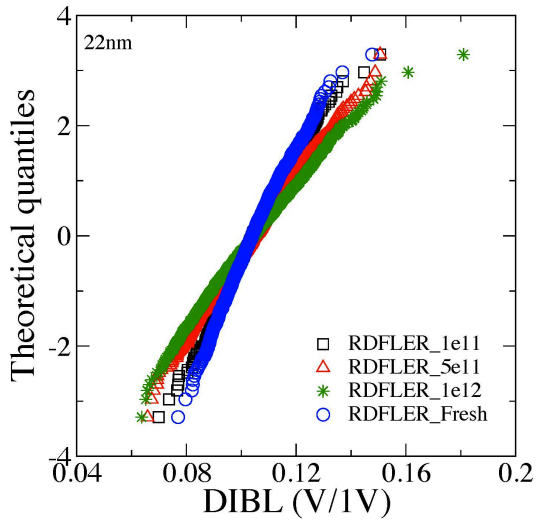
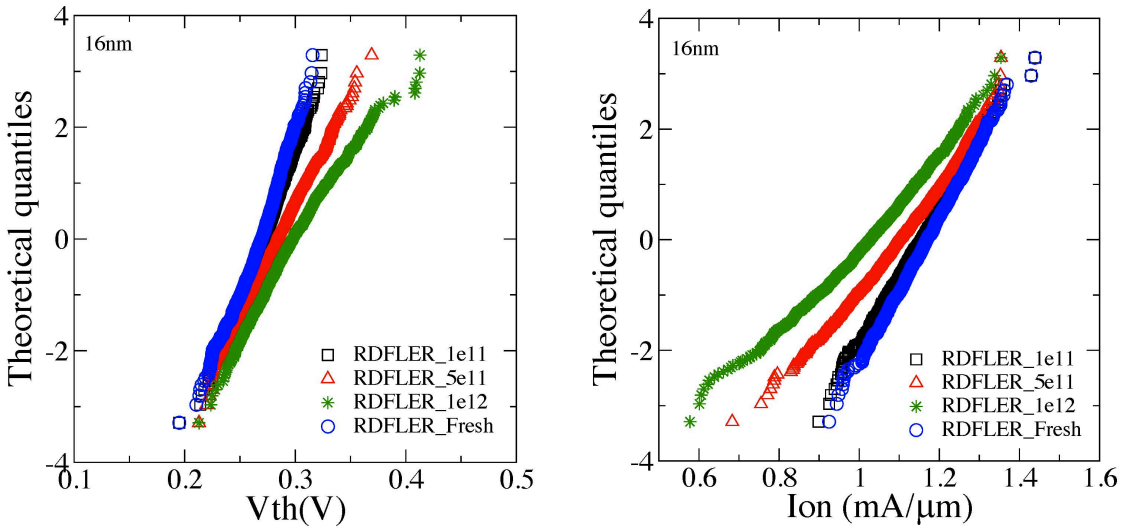


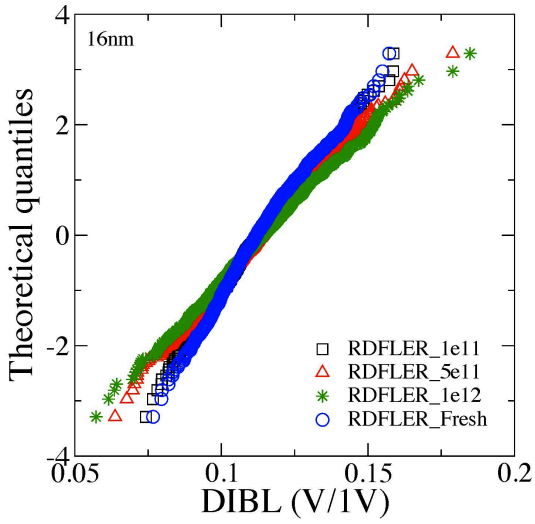
(c)

Figure 6.6 : Normal probability QQ-plots for (a) V_{th}, (b) I_{on} and (c) DIBL due to combinations of RDF and LER at different level of degradations, subjected to 22nm gate length technology.



(a)

(b)



(c)

Figure 6.7 : Normal probability QQ-plots for (a) V_{th}, (b) I_{on} and (c) DIBL due to combinations of RDF and LER at different level of degradations, subjected to 16nm gate length technology.

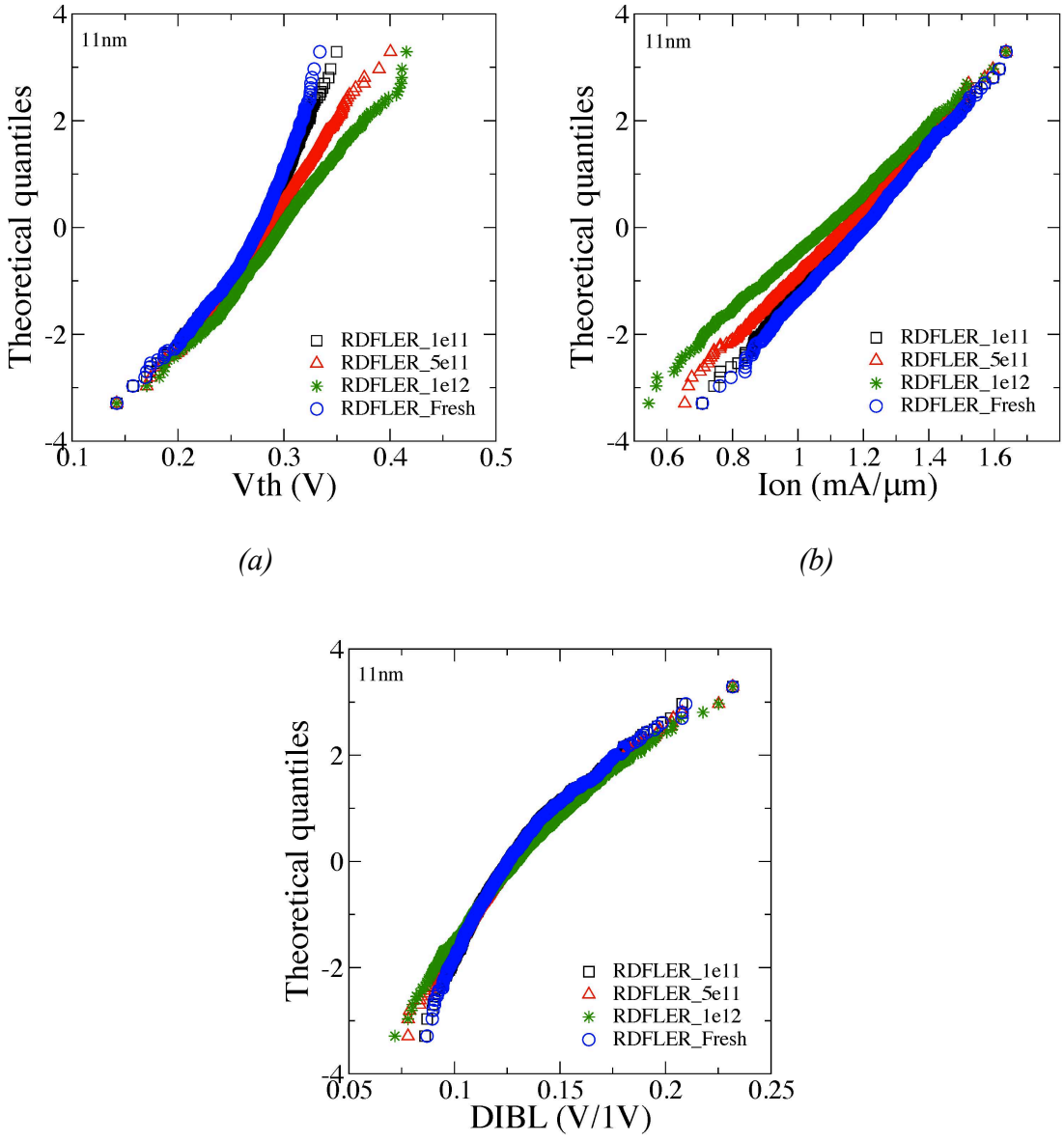


Figure 6.8 : Normal probability QQ-plots for (a) V_{th}, (b) I_{on} and (c) DIBL due to combinations of RDF and LER at different level of degradations, subjected to 11nm gate length technology.

For further highlight the scaling effects, Figure 6.9 to Figure 6.11 provide normal quantile-quantile (QQ) plots of V_{th}, I_{on} and DIBL respectively, comparing the three different gate length transistors in the same figure. In these figures, the three different stages of degradation: 1e11 cm^{-2}, 5e11 cm^{-2} and 1e12 cm^{-2} are individually considered.

The initial V_{th} variability is dominated by LER as previously discussed in Chapter 5, which is dominated by threshold voltage variations due to the effective gate length change introduced by LER [39]. At the high degradation stage, the BTI induced additional threshold voltage shift tends to merge the upper tail end of V_{th} distributions together for the three different technology generations.

The impact of additional PBTI-induced interface charges on drive current for the three different gate lengths is also presented. Similar to the V_{th} variation, from the scaling prospective, the BTI induced drive current degradation merges the lower tail of the on-current distributions of different technology generations together, which to some extent limits the benefits of scaling on the performance improvement.

In general terms, the impact of the BTI degradation on the transistors short channel behavior is not as strong as for the threshold voltage since the first order impact of BTI is to shift the device characteristics. DIBL is an important device figure of merit describing device short channel effects. From the scaling point of view, the BTI-induced degradation does not have a big impact on the DIBL distribution pattern at different gate lengths. However, as demonstrated in Figure 6.6-6.8, the magnitude of DIBL variation increases with the increase of the degradation level.

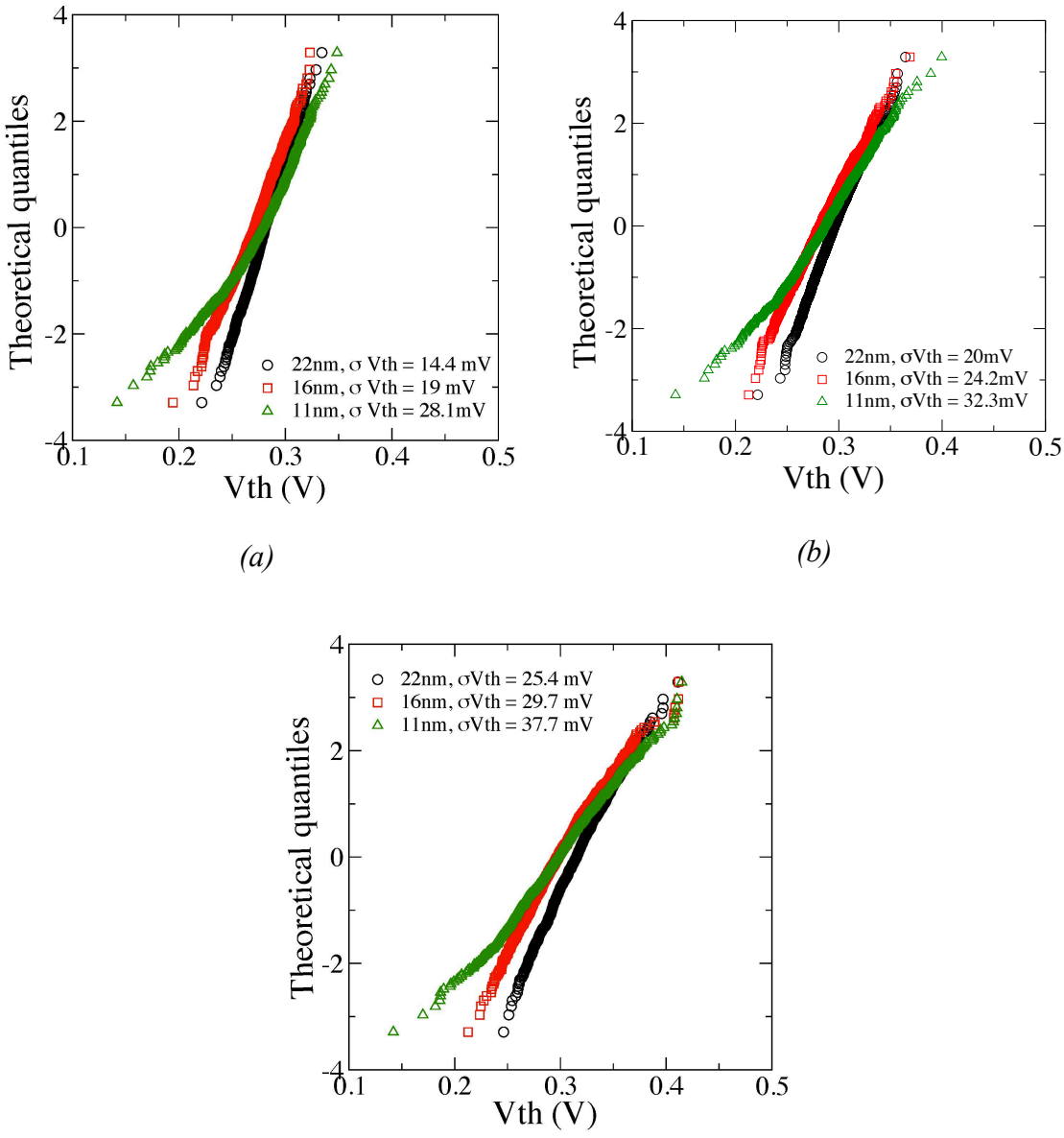
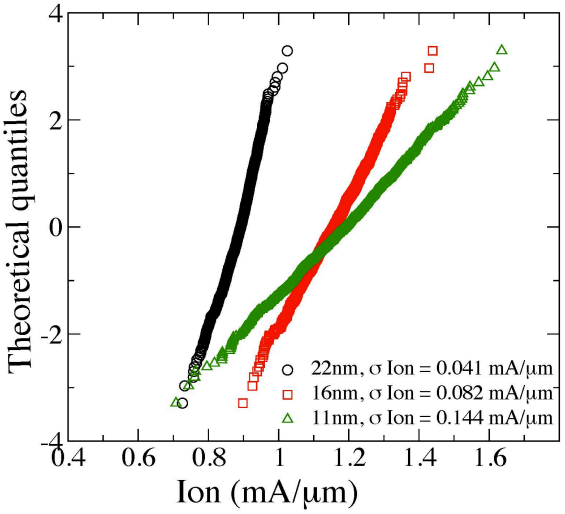
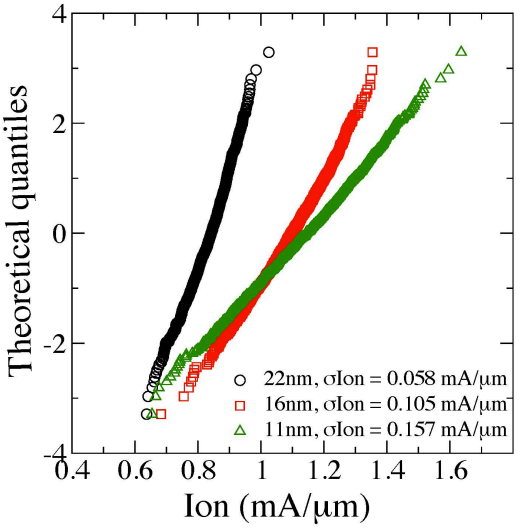


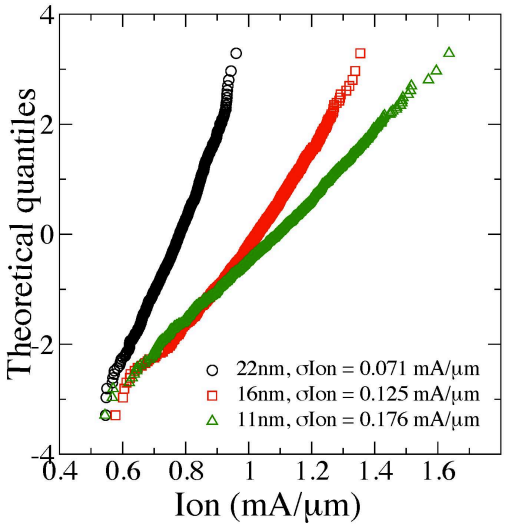
Figure 6.9 : Normal probability QQ-plots for V_{th} distributions due to combinations of RDF, LER and N_{it} at (a) 1e11 cm $^{-2}$ (b) 5e11 cm $^{-2}$ (c) 1e12 cm $^{-2}$, comparing three different gate lengths.



(a)



(b)



(c)

Figure 6.10 : Normal probability QQ-plots for I_{on} distributions due to combinations of RDF, LER and N_{it} at (a) 1e11 cm $^{-2}$ (b) 5e11 cm $^{-2}$ (c) 1e12 cm $^{-2}$, comparing three different gate lengths.

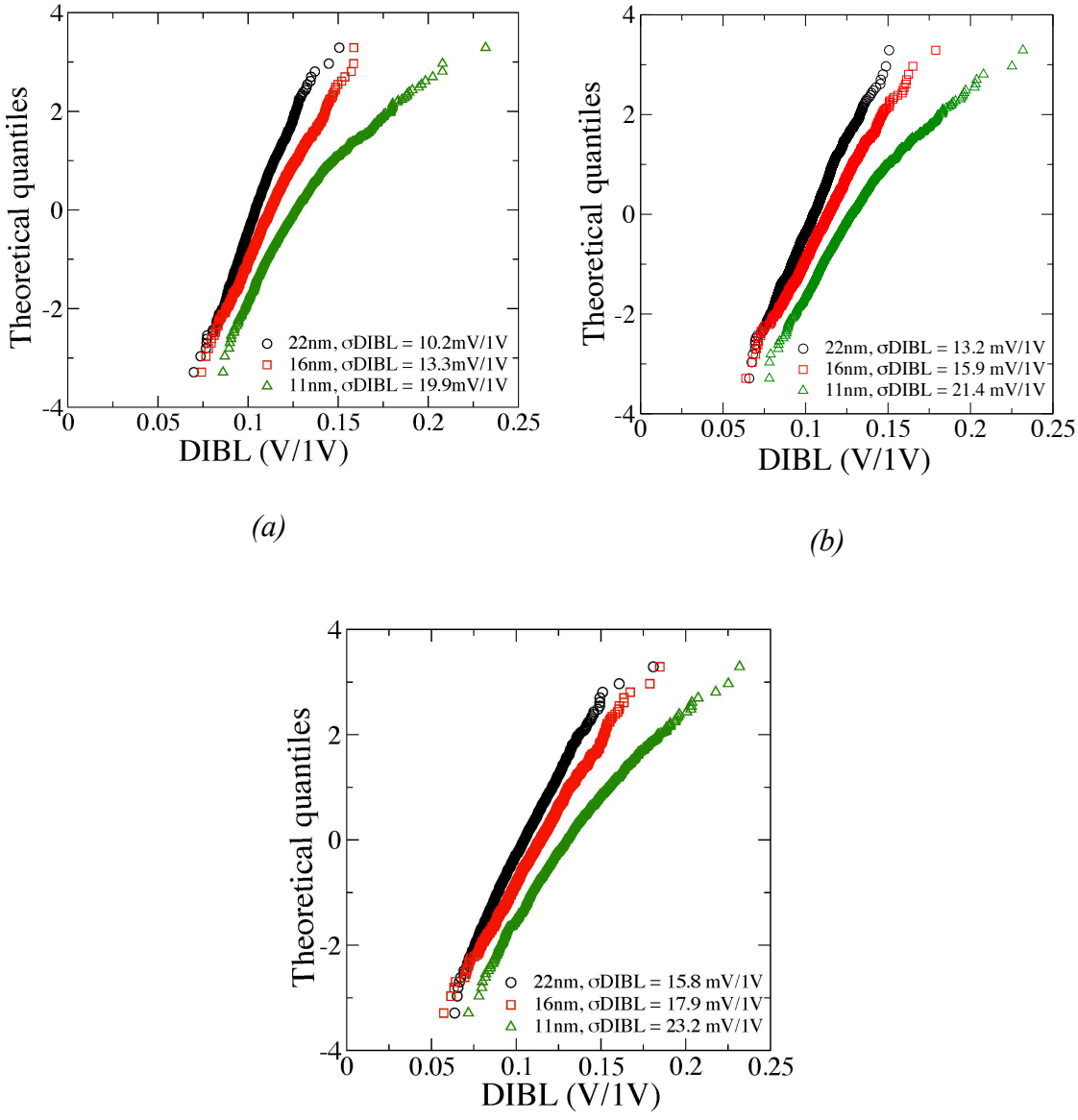


Figure 6.11 : Normal probability QQ-plots for DIBL distributions due to combinations of RDF, LER and N_{it} at (a) 1e11 cm $^{-2}$ (b) 5e11 cm $^{-2}$ (c) 1e12 cm $^{-2}$, comparing three different gate lengths.

The average values of V_{th}, I_{on} and DIBL as a function of the trapped charge density for the three different gate length transistors are presented in Figure 6.12. As expected, the average V_{th} ($<V_{th}>$) increases linearly with the progressive degradation and this is true for all gate lengths. As a result, the average I_{on} ($<I_{on}>$) decreases with the increase in trap density. This illustrates the anti-correlation dependence between V_{th} and I_{on}. This is related to the fact that a trapped charge blocks locally the current conduction giving also rise to an increase in V_{th} and a decrease in the magnitude of the drive current. As discussed in Figure 6.11, BTI only has a weak influence on the average DIBL (<DIBL>) value.

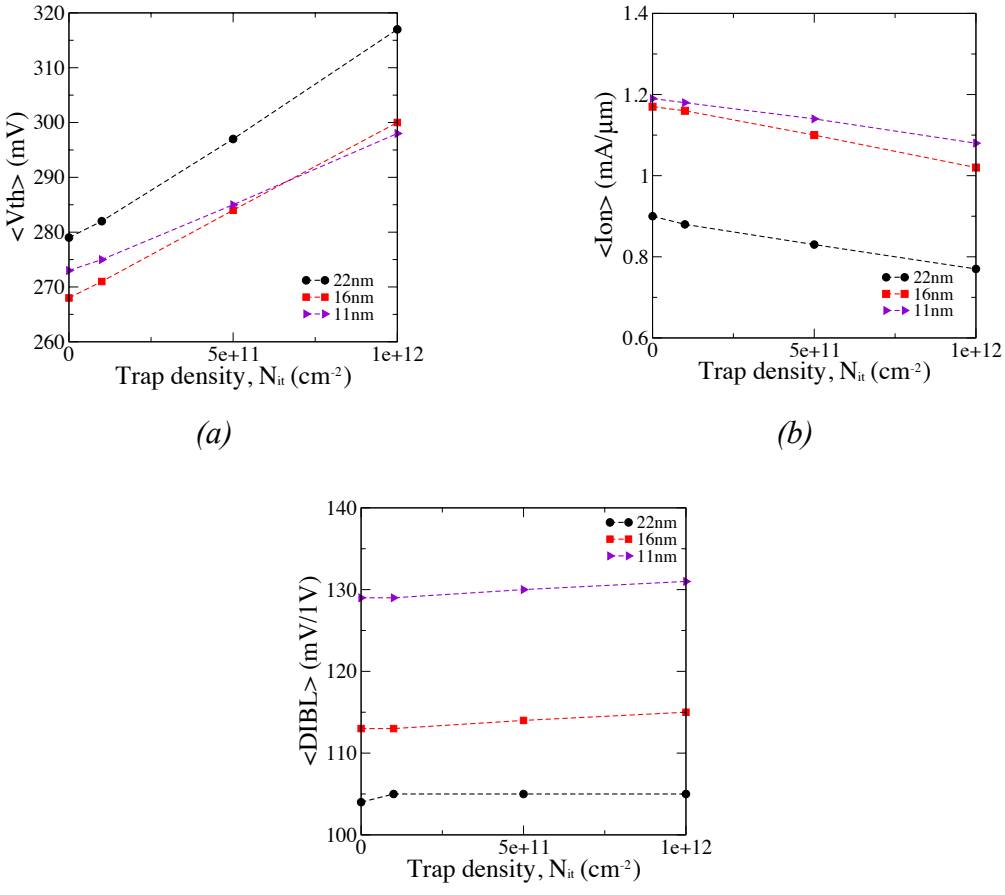


Figure 6.12 : Mean of V_{th}, I_{on} and DIBL versus trap density with the inclusion of static statistical variability sources of RDF and LER.

Figure 6.13 reports the standard deviation of V_{th}, I_{on} and DIBL as a function of the interface trap density for three different technology generations at high drain bias. A complete summary of the standard deviation of V_{th}, I_{on} and DIBL for different trapped charge densities in the presence of RDF and LER for the three simulated gate lengths is also presented in Table 6.1. The results clearly demonstrate a linear increase in σV_{th}, σI_{on} and σDIBL with the progressive degradation of all technology generations. The BTI degradation enhances the statistical variability, brings a time-dependent variability issues to the device and circuit operation.

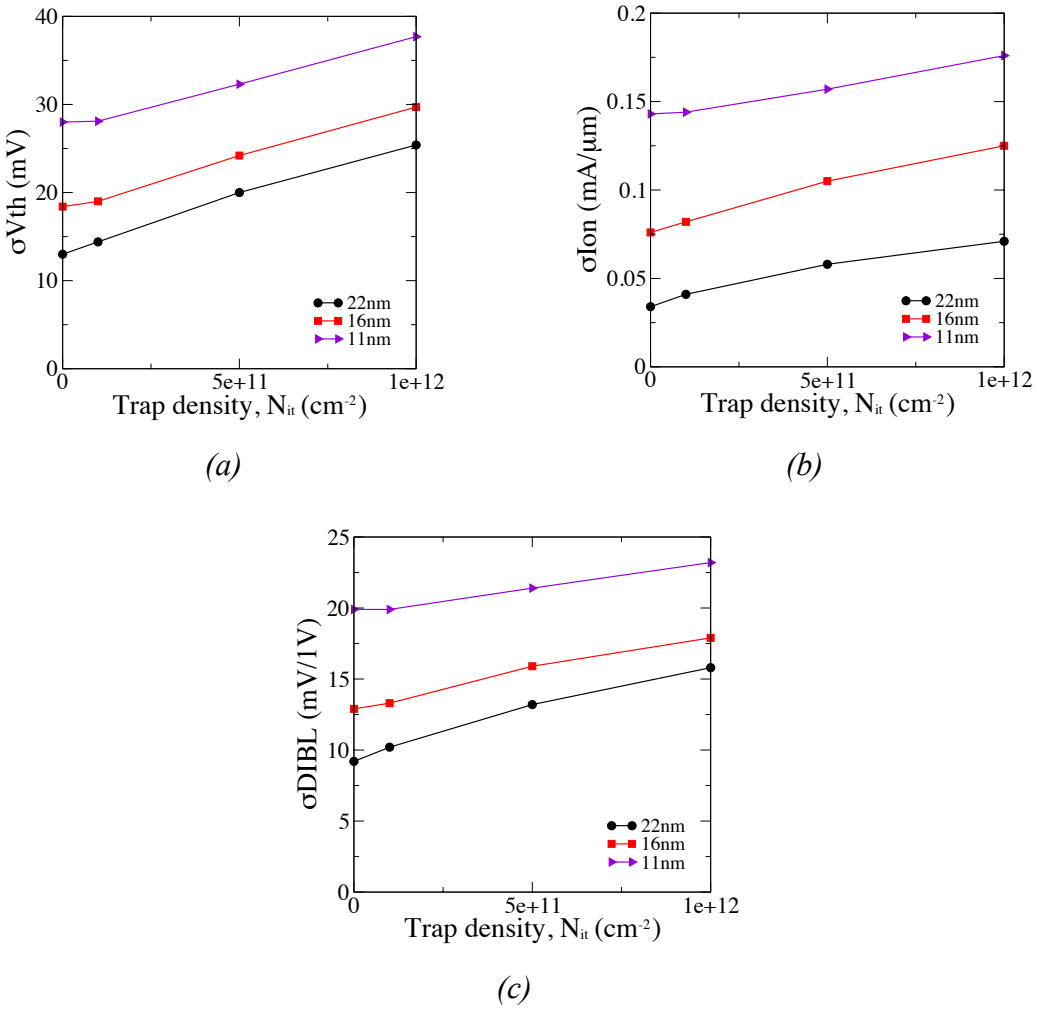


Figure 6.13 : Standard deviation of V_{th}, I_{on} and DIBL versus trap density with the inclusion of static statistical variability sources of RDF and LER.

Table 6.1 : Effect of interface trapped charge density on V_{th}, I_{on} and DIBL distributions in the background of RDF and LER for three different gate lengths.

22nm gate length	σV_{th} (mV)	σI_{on} (mA/μm)	σDIBL (mV/1V)
RDF+LER (Fresh device)	13.0	0.034	9.2
RDF+LER+Nit 1e11	14.4	0.041	10.2
RDF+LER+Nit 5e11	20.0	0.058	13.2
RDF+LER+Nit 1e12	25.4	0.071	15.8
16 nm gate length	σV_{th} (mV)	σI_{on} (mA/μm)	σDIBL (mV/1V)
RDF+LER (Fresh device)	18.4	0.076	12.9
RDF+LER+Nit 1e11	19.0	0.082	13.3
RDF+LER+Nit 5e11	24.2	0.105	15.9
RDF+LER+Nit 1e12	29.7	0.125	17.9
11nm gate length	σV_{th} (mV)	σI_{on} (mA/μm)	σDIBL (mV/1V)
RDF+LER (Fresh device)	28.0	0.143	19.9
RDF+LER+Nit 1e11	28.1	0.144	19.9
RDF+LER+Nit 5e11	32.3	0.157	21.4
RDF+LER+Nit 1e12	37.7	0.176	23.2

6.4 Statistical Reliability Simulations in the Presence of MGG

This section presents the simulation results of PBTI degradation in n-channel FD-UTBSOI transistors featuring 22nm, 16nm and 11nm gate lengths and considering the metal gate-first technology. Apart from RDF and LER, MGG is also included in this case as a statistical variability source in the fresh transistors. Similar to section 6.3, three degradation levels with average interface trapped charge sheet densities of 1e11cm^{-2}, 5e11 cm^{-2} and 1e12 cm^{-2} are considered in this study. As an example, a typical potential profile corresponding to the trap charge sheet density of 1e12 cm^{-2} in the presence of combined RDF, LER and MGG variability sources is shown in Figure 6.14. The spikes at the sites of trapped charges reduce the local carrier concentrations and thus cause local and global current reduction.

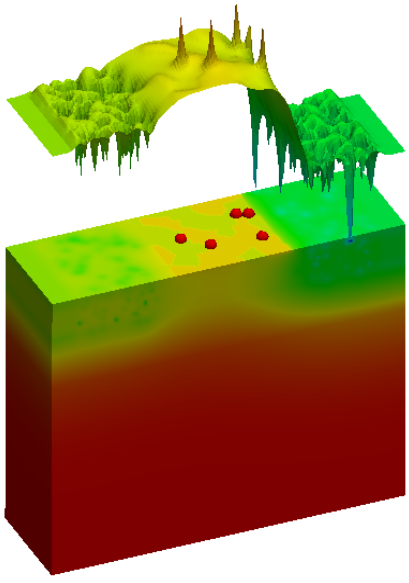


Figure 6.14 : The electrostatic potential of 22nm FD-UTB SOI nMOSFET that includes RDF, LER and MGG at interface-trapped charge density of 1e12 cm^{-2}. The trapped charges are shown in red colour. (W/L=1)

First we present the results of the impact of additional trapped charges on the transistor characteristics in the presence of RDF, LER and MGG. Figures 6.15 - 6.17 show the transfer characteristics of the 22nm, 16nm and 11nm gate lengths FD-UTB SOI devices at high drain bias for ensembles of 1000 transistors with an increasing level of degradation and in the presence of RDF, LER and MGG. All I_dV_g characteristics are presented in linear and logarithmic scales to demonstrate the impact of PBTI in both sub-threshold and on-current regions.

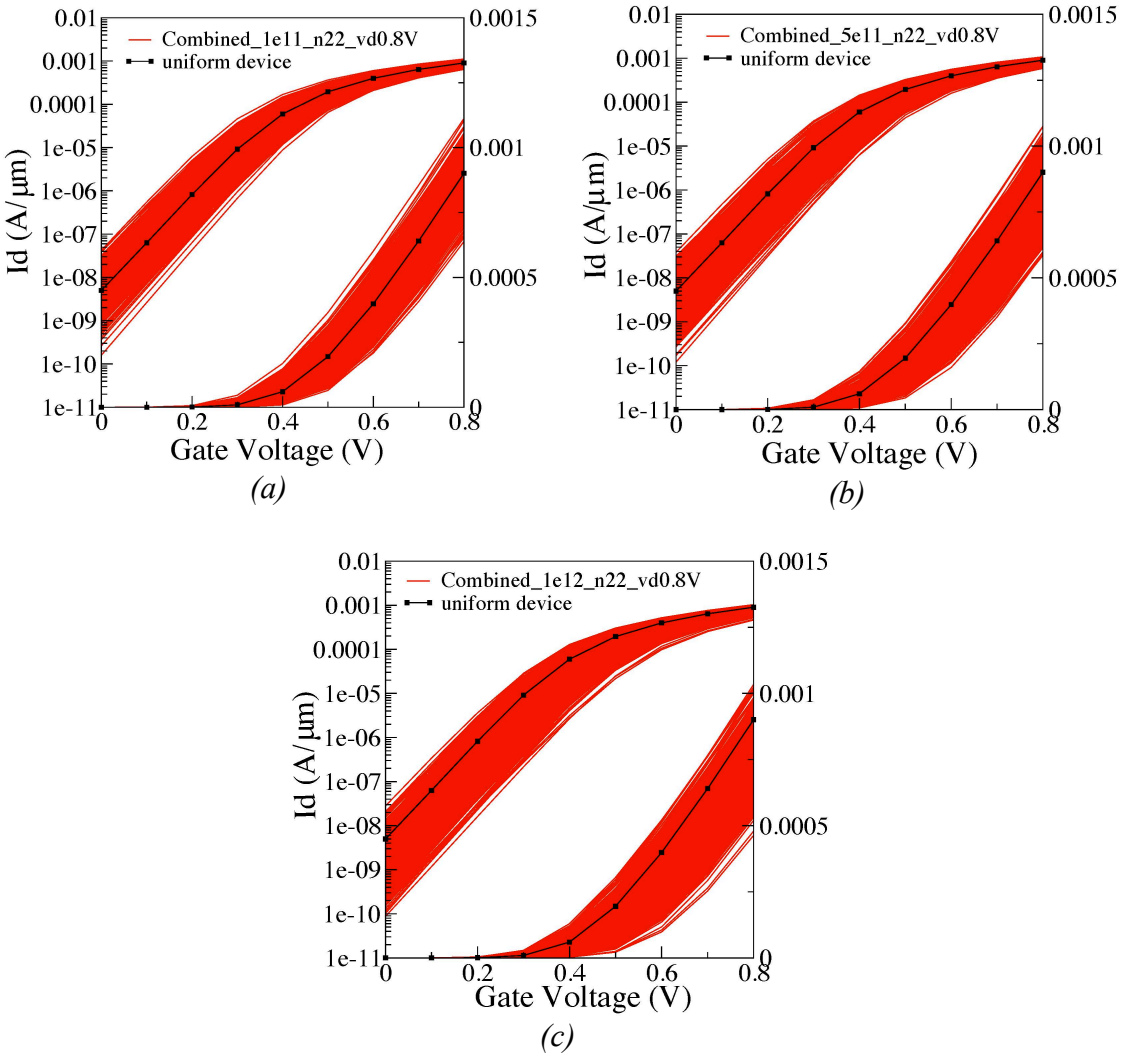


Figure 6.15 : I_dV_g of 1000 devices with RDF, LER, MGG and increase of PBTI degradations (a) 1e11cm^{-2} (b) 5e11cm^{-2} and (c) 1e12cm^{-2} for 22nm gate length.

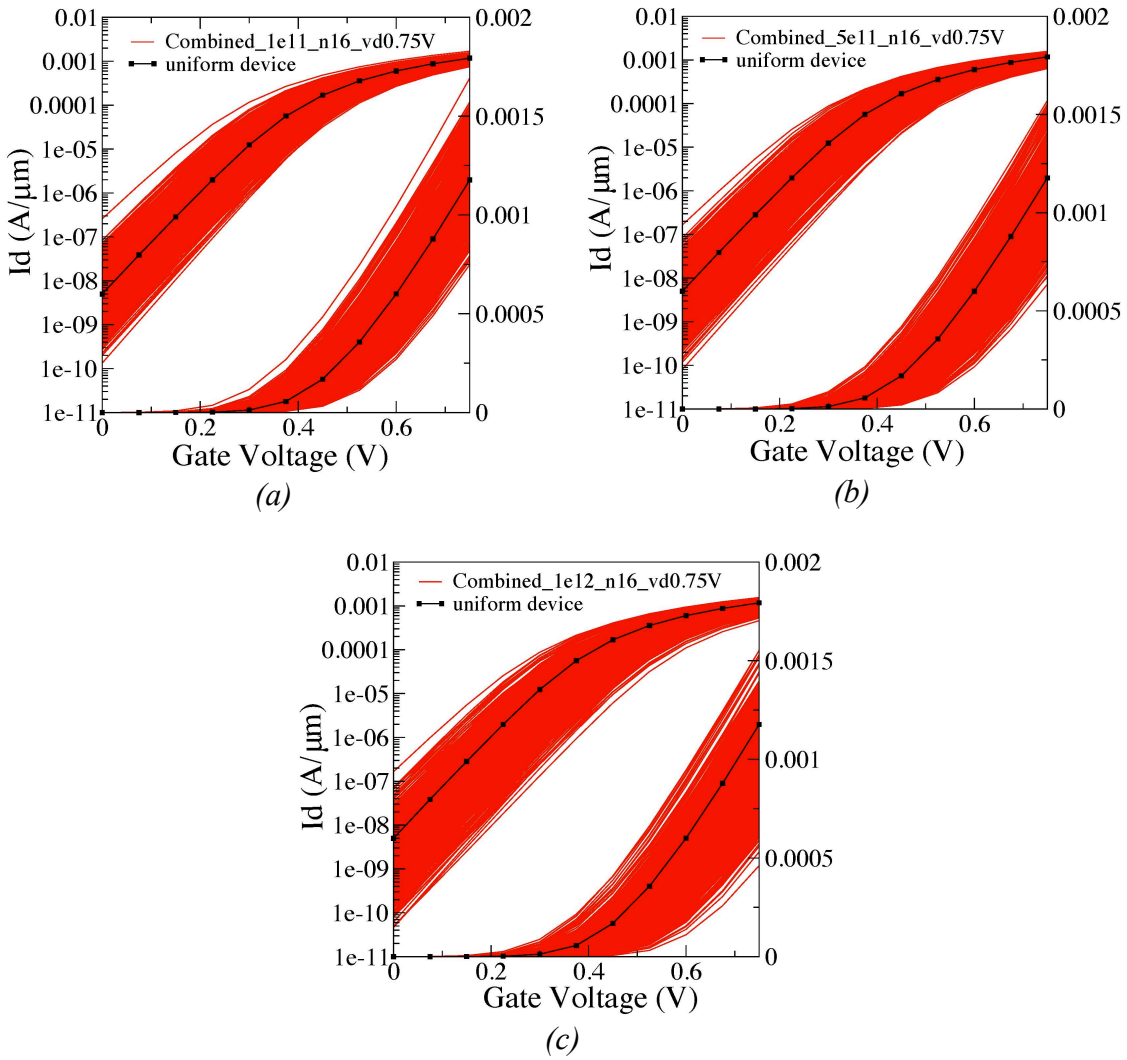


Figure 6.16 : I_dV_g of 1000 devices with RDF, LER, MGG and increase of PBTI degradations (a) 1e11cm^{-2} (b) 5e11cm^{-2} and (c) 1e12cm^{-2} for 16nm gate length.

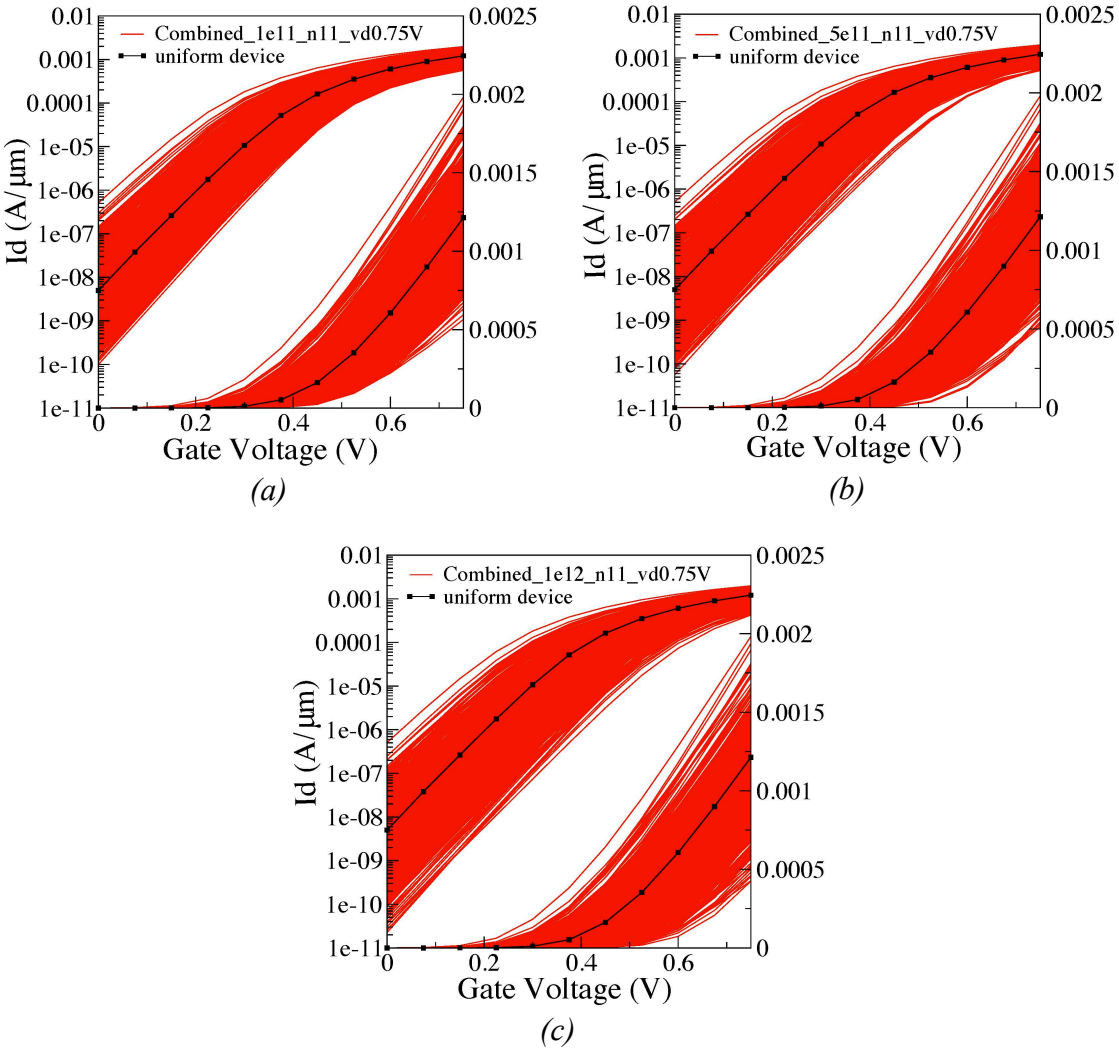


Figure 6.17 : I_dV_g of 1000 devices with RDF, LER, MGG and increase of PBTI degradations (a) 1e11cm^{-2} (b) 5e11cm^{-2} and (c) 1e12cm^{-2} for 11nm gate length.

Figure 6.15 - 6.17 clearly show that the additional impact of MGG on device characteristics. The maximum on-current can be more than four times larger than minimum on-current in the 11nm devices at high degradation stage, compared to the three time difference where MGG is not presented.

The QQ plots of V_{th}, I_{on} and DIBL distributions in the presence of RDF, LER and MGG at the three different level of degradation for the three technology generations are presented in Figure 6.18- 6.20. Similar trends of degradation can be observed as in the Figure 6.6 – 6.8 where MGG was not presented. However, due to the increased initial statistical variation introduced by MGG, the relative impact of BTI on the magnitude of device variation is reduced. For instance, in the 11nm gate length transistor, a trap charge sheet density of 1e12cm^{-2}, which corresponds to a late BTI degradation stage, introduces a further 16% degradation on σV_{th} , while the same amount of trap charge sheet density can introduce a further 35% degradation for the counterpart transistor simulations without MGG.

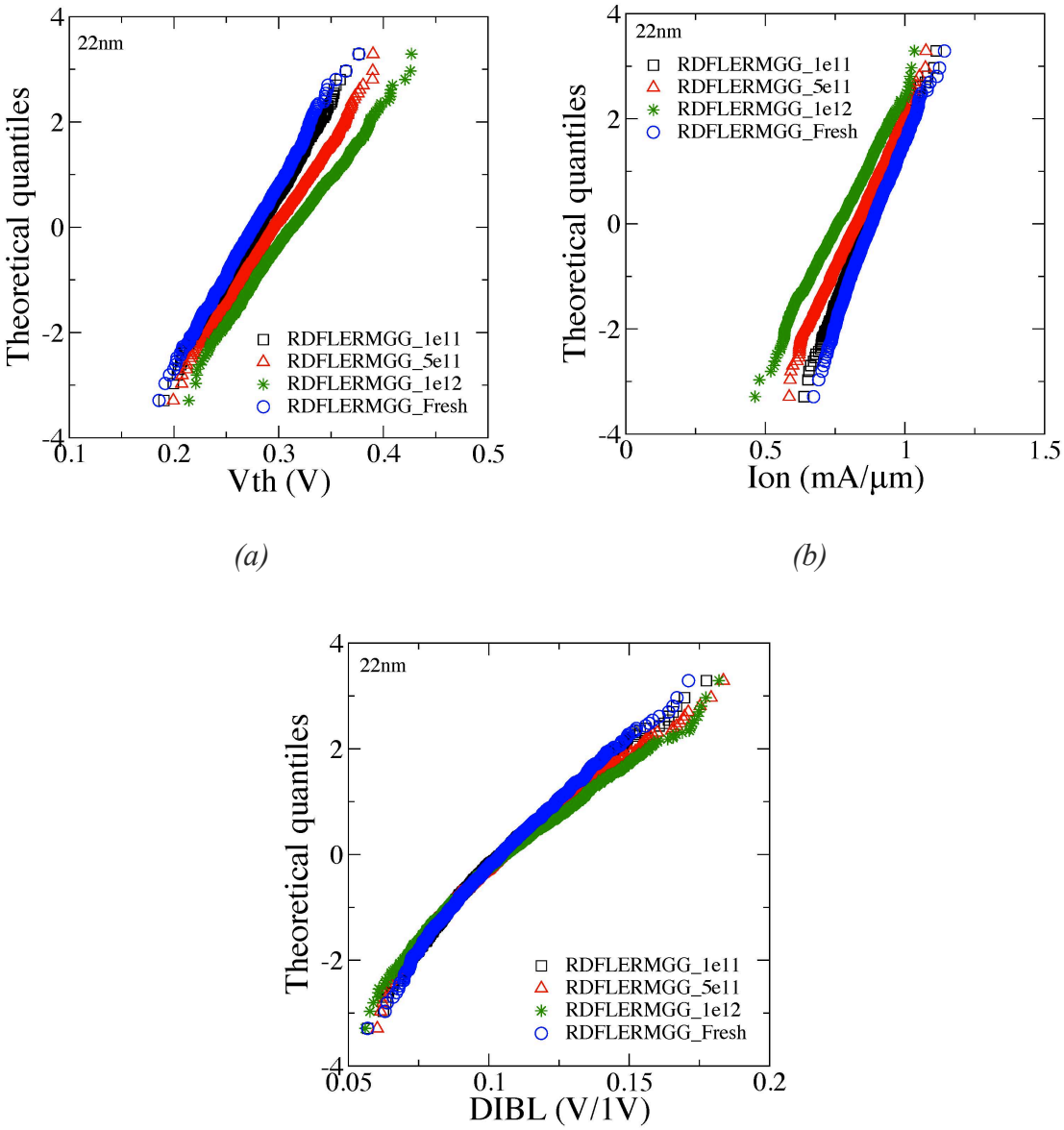


Figure 6.18 : Normal probability QQ-plots for (a) V_{th}, (b) I_{on} and (c) DIBL due to combinations of RDF, LER and MGG at different level of degradations, subjected to 22nm gate length technology.

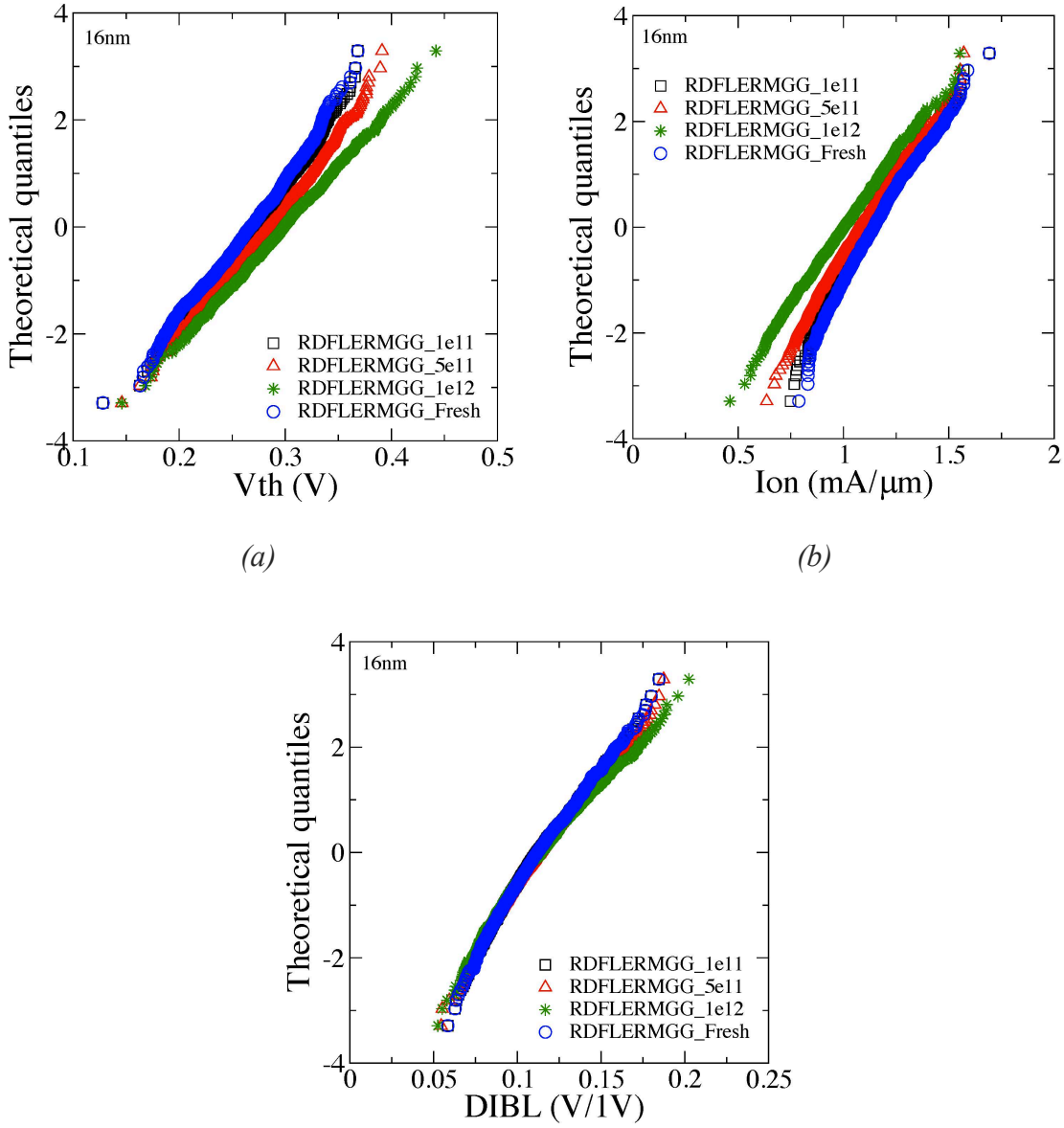
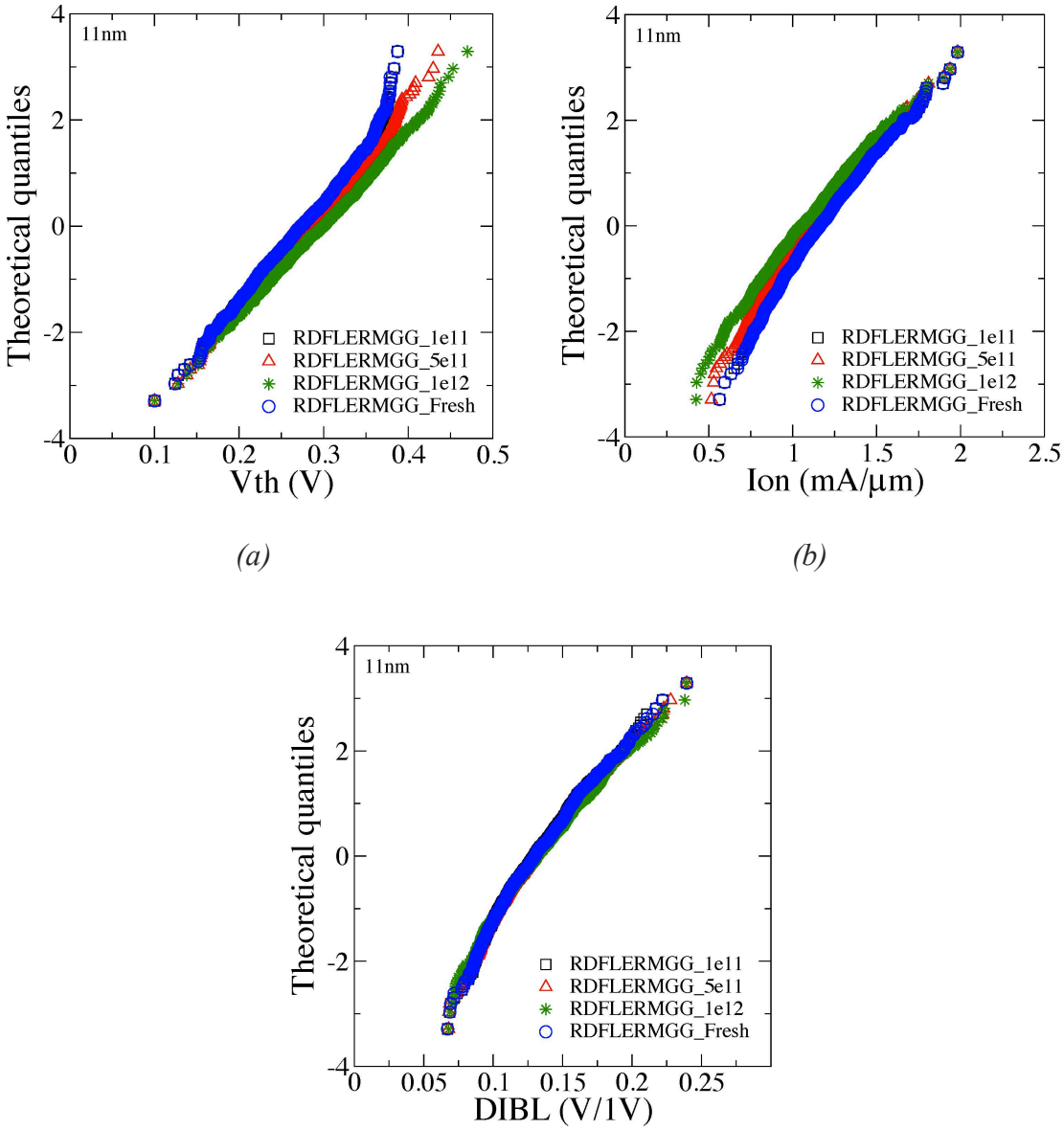


Figure 6.19 : Normal probability QQ-plots for (a) V_{th}, (b) I_{on} and (c) DIBL due to combinations of RDF, LER and MGG at different level of degradations, subjected to 16nm gate length technology.



(a) *(b)*

(c)

Figure 6.20 : Normal probability QQ-plots for (a) V_{th}, (b) I_{on} and (c) DIBL due to combinations of RDF, LER and MGG at different level of degradations, subjected to 11nm gate length technology.

To further highlight the effects associated with the scaling, Figure 6.21 to Figure 6.23 present normal QQ plots of V_{th}, I_{on} and DIBL respectively, with the three transistors with different gate length in the same figure. In each one of these figures, the different stages of degradation: $1e11cm^{-2}$, $5e11cm^{-2}$ and $1e12cm^{-2}$ are applied.

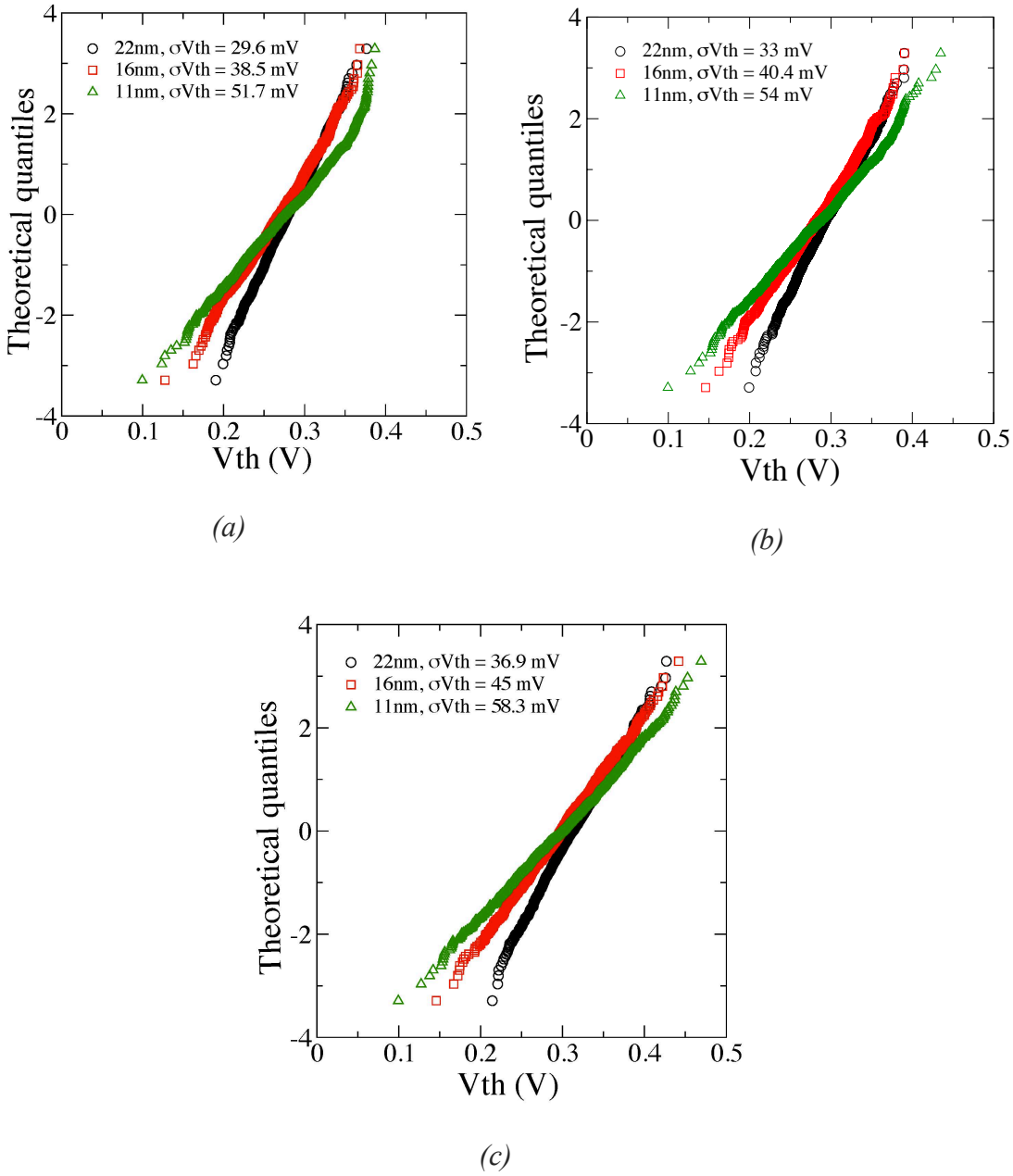


Figure 6.21 : Normal probability QQ-plots for V_{th}, distributions due to combinations of RDF, LER, MGG and N_{it} at (a) 1e11 cm $^{-2}$ (b) 5e11 cm $^{-2}$ (c) 1e12 cm $^{-2}$, comparing three different gate lengths.

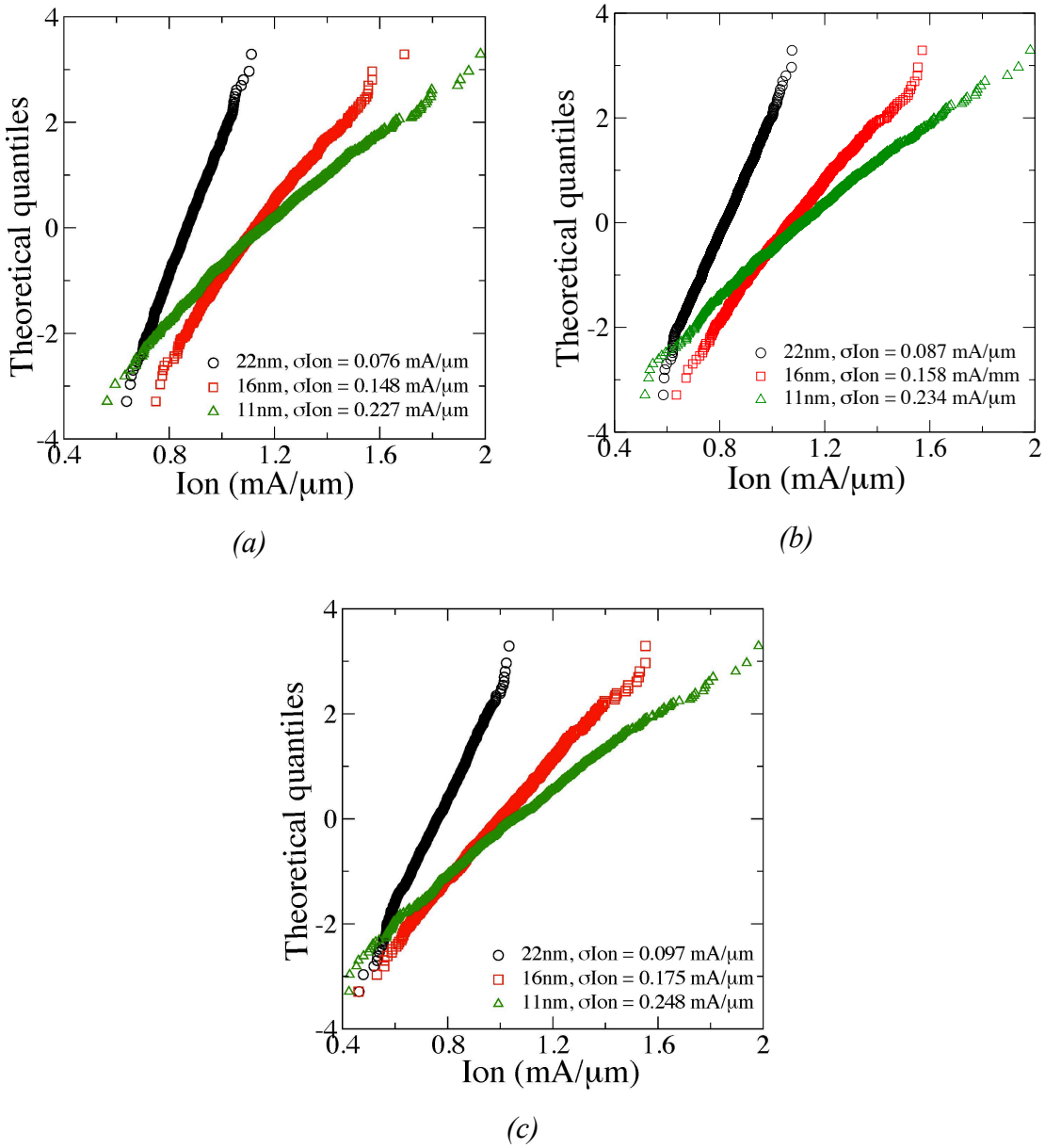


Figure 6.22 : Normal probability QQ-plots for I_{on} distributions due to combinations of RDF, LER, MGG and N_{it} at (a) 1e11 cm $^{-2}$ (b) 5e11 cm $^{-2}$ (c) 1e12 cm $^{-2}$, comparing three different gate lengths.

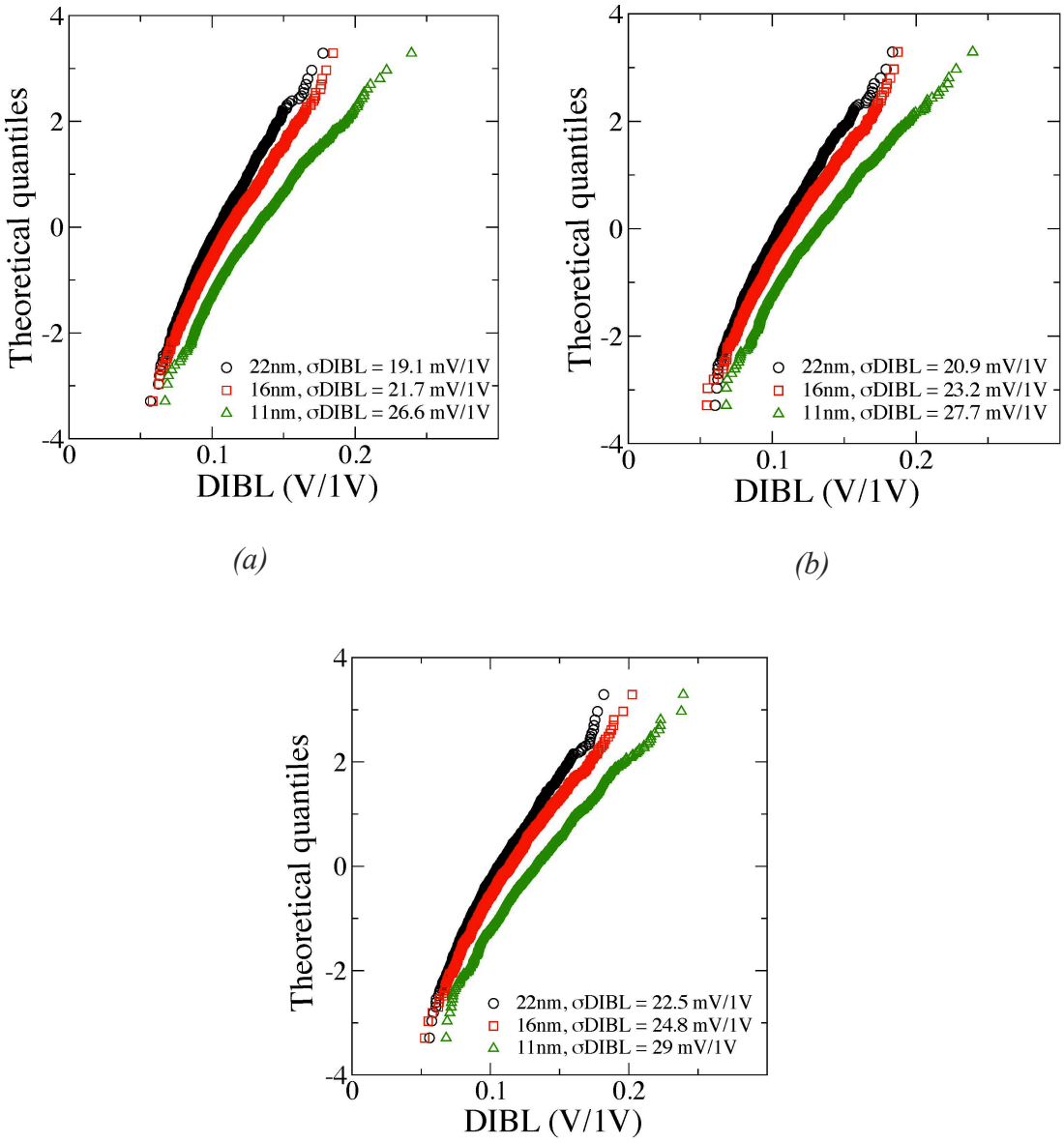


Figure 6.23 : Normal probability QQ-plots for DIBL distributions due to combinations of RDF, LER, MGG and N_{it} at (a) 1e11 cm $^{-2}$ (b) 5e11 cm $^{-2}$ (c) 1e12 cm $^{-2}$, comparing three different gate lengths.

As reported in Chapter 5, MGG has a dominant contribution to the dispersion of both V_{th} and I_{on} compared to the RDF and LER. In the case of additional trapped charge incorporated with the rest of the variability sources, MGG is still the dominant variability source. The V_{th} distributions clearly show that the upper tail of distribution for 11nm gate length is highly skewed at the lower end of the distribution. This is due to the fact that the average grain size is of the same order as the gate area. However, the additional trap charges introduced by BTI fundamentally change the upper tail of the V_{th} distribution compared to the initial impact of MGG. In the case of I_{on}, the BTI induced drive current degradation merges together the lower tail of the on-current distributions of the different technology generations. This to some extent limits the benefits of scaling on the performance improvement. Finally, for the DIBL distribution, as discussed in section 6.3, the BTI-induced degradation does not have a big influence on the distribution pattern of different gate lengths, apart from the fact that the magnitude of the DIBL variation increases with the increase of the degradation level.

The dependence of the average V_{th}, I_{on} and DIBL values as a function of the trapped charge density for three different gate length transistors are presented in Figure 6.24, all in the presence of RDF, LER and MGG. The $<V_{th}>$ increases linearly as a function of the trapped charge sheet density for all transistors with different gate lengths. As a result, the average I_{on} ($<I_{on}>$) decreases with the increase in the trapped charge density. As expected, BTI only have a mild influence on <DIBL> behavior.

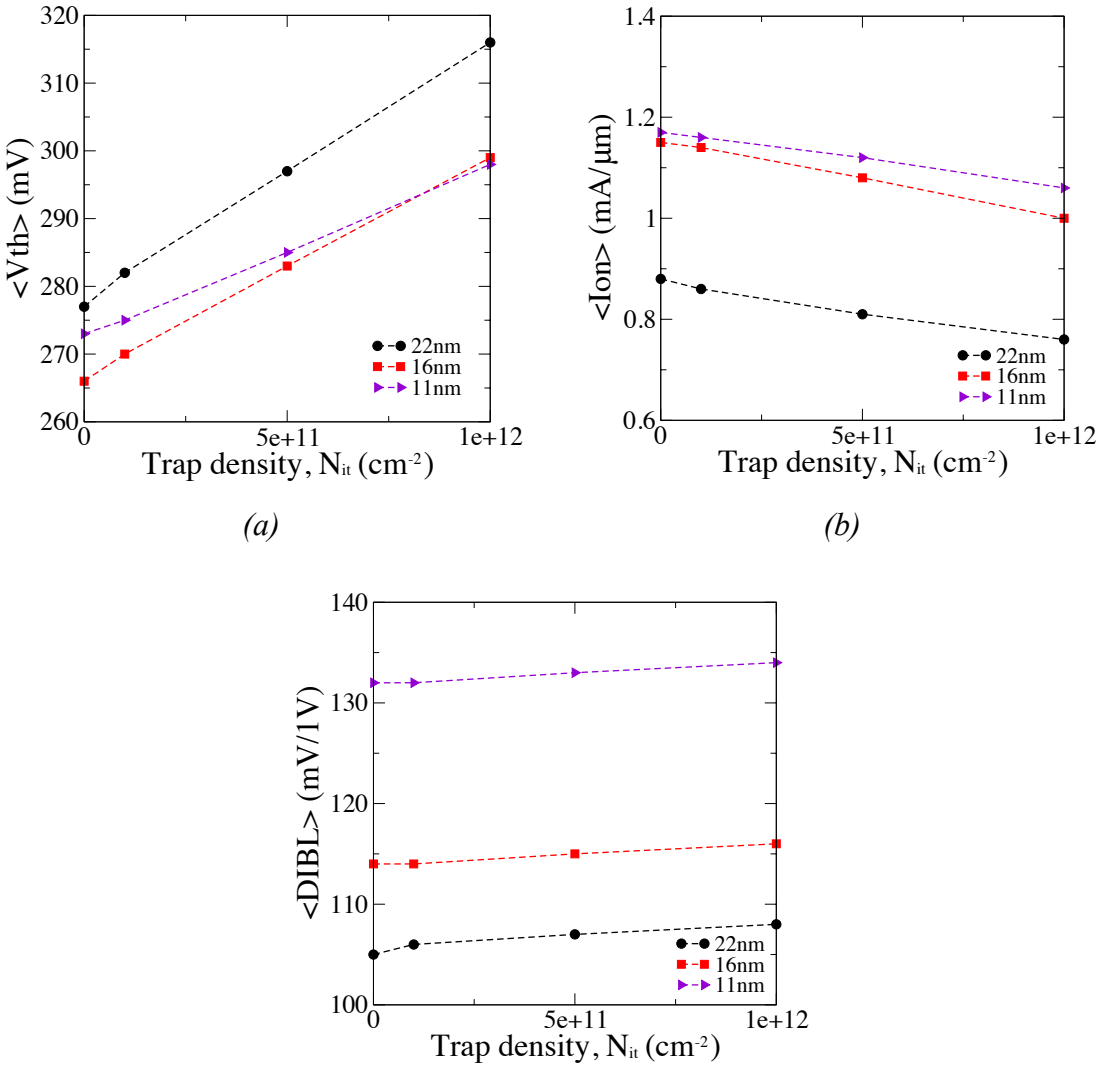


Figure 6.24 : Mean of V_{th}, I_{on} and DIBL versus trap density with the inclusion of static variability sources of RDF, LER and MGG.

Figure 6.25 depicts the standard deviation of V_{th}, I_{on} and DIBL as a function of interface trapped charge density for three different technology generations at high drain bias. A complete summary of the standard deviation of V_{th}, I_{on} and DIBL for different trapped charge densities in the presence of RDF, LER and MGG, and for three simulated gate lengths is also presented in Table 6.2. The results clearly demonstrate a linear increase in σV_{th}, σI_{on} and σDIBL with the progressive degradation for all technology generations.

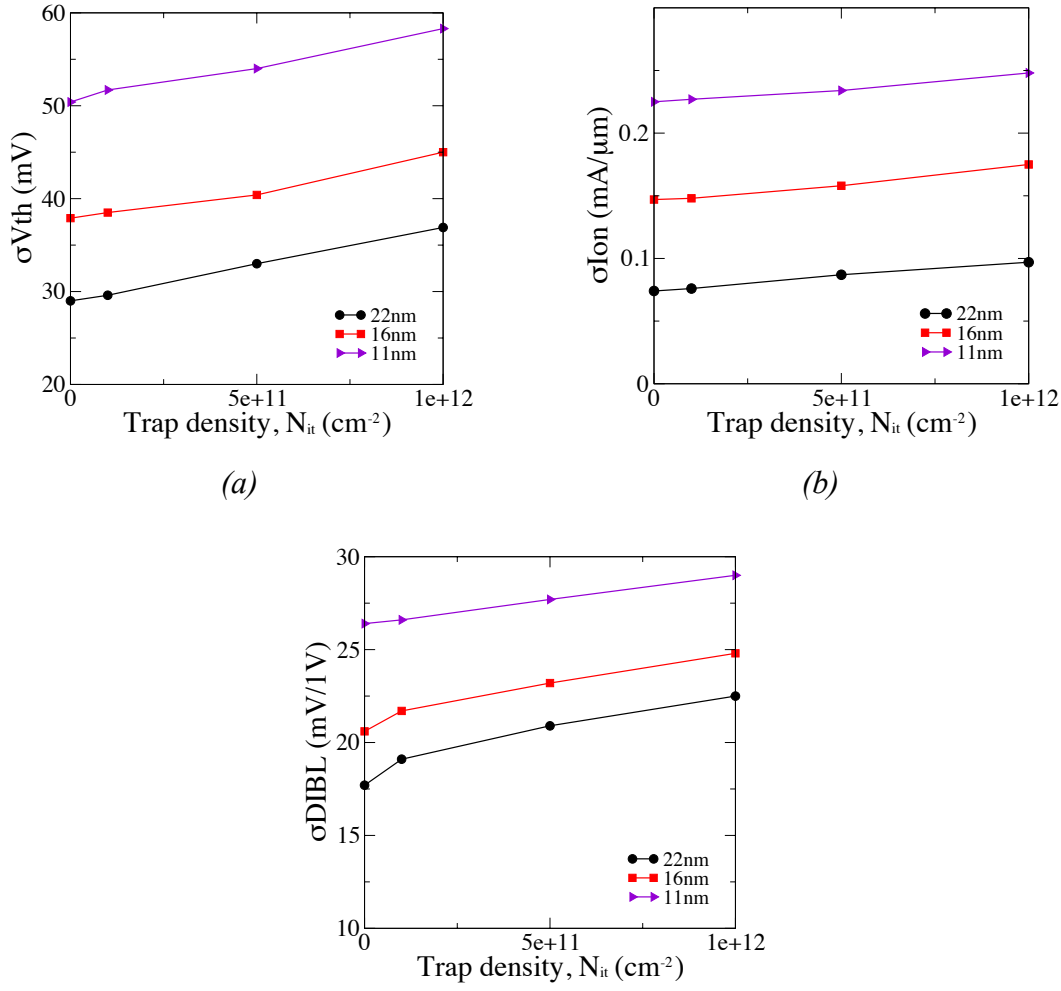


Figure 6.25 : Standard deviation of V_{th}, I_{on} and DIBL versus trap density with the inclusion of static variability sources of RDF, LER and MGG.

Table 6.2 : Effect of interface trapped charge density on V_{th}, I_{on} and DIBL distributions in the background of RDF, LER and MGG for three different gate lengths.

22nm gate length	σV_{th} (mV)	σI_{on} (mA/μm)	σDIBL (mV/1V)
RDF+LER+MGG (Fresh device)	29.0	0.074	17.7
RDF+LER+MGG+Nit 1e11	29.6	0.076	19.1
RDF+LER+MGG+Nit 5e11	33.0	0.087	20.9
RDF+LER+MGG+Nit 1e12	36.9	0.097	22.5
16nm gate length	σV_{th} (mV)	σI_{on} (mA/μm)	σDIBL (mV/1V)
RDF+LER+MGG (Fresh device)	37.9	0.147	20.6
RDF+LER+MGG+Nit 1e11	38.5	0.148	21.7
RDF+LER+MGG+Nit 5e11	40.4	0.158	23.2
RDF+LER+MGG+Nit 1e12	45.0	0.175	24.8
11nm gate length	σV_{th} (mV)	σI_{on} (mA/μm)	σDIBL (mV/1V)
RDF+LER+MGG (Fresh device)	50.4	0.225	26.4
RDF+LER+MGG+Nit 1e11	51.7	0.227	26.6
RDF+LER+MGG+Nit 5e11	54.0	0.234	27.7
RDF+LER+MGG+Nit 1e12	58.3	0.248	29.0

6.5 Summary

This chapter presents a comprehensive 3D simulation study of the statistical reliability in scaled FD-UTB SOI n-type MOSFET with physical gate lengths of 22nm, 16nm and 11nm. The GSS 'atomistic' simulator GARAND has been employed to investigate the impact of PBTI on the device electrical characteristics in concert with combined static variability sources. Two simulation scenarios have been considered here for the static variability sources present in the fresh devices. In the first scenario only RDF and LER corresponding to gate-last technology have been considered. In the second scenario, RDF, LER and MGG have been considered, corresponding to a gate-first technology. Large ensembles of 1000 microscopically different transistors are simulated for each scenario with three degradation levels: 1e11 cm^{-2} (early degradation), 5e11 cm^{-2} (intermediate degradation) and 1e12 cm^{-2} (late degradation).

The simulation results show that the average V_{th} and DIBL increase and the average I_{on} decreases linearly with the increased trapped charge density. BTI degradation has also a significant impact on the transistor variability. The results clearly indicate that BTI has stronger impact on the gate-last compared to gate-first technology due to less native variability in the former. For instance, in the 11nm gate length metal gate- last transistor, there is 34% increase in V_{th} variation compared to the fresh device while in the gate-first technology the increase in the variability after degradations is 15% compared to the corresponding fresh device. However, due to the larger magnitude of initial variation introduced by MGG at the gate-first process, from variability point of view, the gate-last approach is still a preferred technology even when considering the impact of BTI.

Figure 6.26 illustrates the trend of gate length dependence of V_{th}, I_{on} and DIBL for combined variability sources at different trapped charge degradations under two separated scenarios; the absence and presence of MGG.

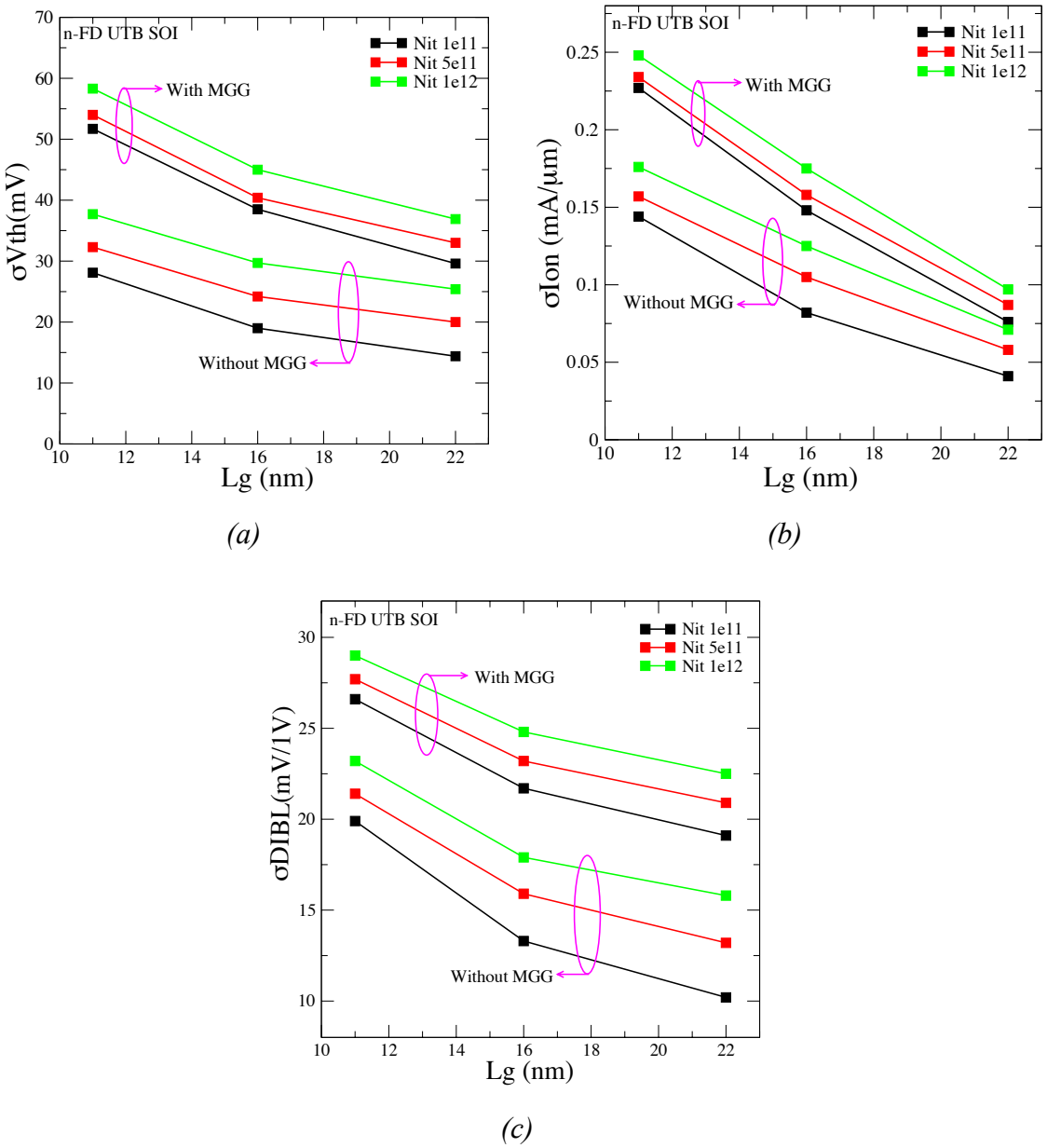


Figure 6.26 : V_{th}, I_{on} and DIBL variations due to combined variability sources at different trapped charge density, without and with MGG.

CHAPTER 7

Conclusions and Outlook

7.1 Conclusions

The ultimate goals of this PhD work were to design a set of realistically scaled single gate FD-UTB SOI transistors and to investigate the corresponding statistical variability and reliability introduced by the discreteness of charge and granularity of matter. Three major steps have carefully followed in order to accomplish this research and achieve its goal. The first step is the design of realistically scaled devices that meet the IRTS technology roadmap specifications at physical gate length of 22nm, 16nm and 11nm. The second step is to perform comprehensive device simulation by incorporating the relevant sources of intrinsic parameter fluctuations such as RDF, LER and MGG. The adverse impact of RDF, LER and MGG on important device figure of merits like V_{th}, I_{on} and DIBL were analysed by taking into account their individual and combined effects. The final aspect of this research is the statistical reliability simulation on scaled

devices, where the impact of combined variability sources at different degradation levels were analysed.

A thorough study of bulk-MOSFET scaling, challenges and new advanced technologies is presented in Chapter 2. At the beginning of this chapter, the relation between scaling of bulk-MOSFET, the Moore's law and the ITRS were discussed. These 'entitles' are strongly interrelated and have impacted tremendous of the great history in the semiconductor industry. At the same time, the scaling limitation of traditional bulk-MOSFET, as well as the general rules of constant field scaling and generalized scaling were described. Since the statistical variability is a major subject of this research, the factors that affect the bulk-MOSFET scaling from variability point of view were discussed in depth. Due to the scaling constraints faced by the bulk-MOSFET, the semiconductor industry is migrating to novel device architectures such as SOI MOSFET and FinFET. Various aspects of both of them were discussed and compared. Finally, the ITRS projection in respect of fully depleted SOI for next technology generations was presented. This chapter highlights the fundamental limitations of the bulk-MOSFET scaling that triggered the introduction of new transistor architectures and the corresponding technologies.

The simulation tools and methodology employed to design the scaled FD-UTB SOI template transistors and to perform the statistical simulations were discussed in Chapter 3. The main simulation tool used in this research is the GSS 3D 'atomistic' drift-diffusion simulator GARAND which employs accurate density-gradient quantum corrections. This well-established simulator was described in detail including the basic equations used in the drift-diffusion equations and the density gradient quantum corrections. The selected mobility models for instance ionized impurity scattering, lattice or phonon scattering, surface roughness scattering and high electric field effects were also presented. Finally, the methods applied to simulate the principle sources of statistical variability (RDF, LER and MGG) were also presented.

In Chapter 4, the designs of template FD-UTB SOI transistor for three different technology generations were presented. Chapter 4 begins with the review of SOI technology, followed by the comprehensive design study of the 22nm gate length FD-UTB SOI transistor, where the design follows the projections from the 2009 edition of

the ITRS as design guidelines. The impact of key design parameters including the BOX thickness, S/D doping abruptness and spacer thickness optimization were investigated in details. The impact of substrate bias in FD-UTB SOI device is also carefully taken into account. The design proceeds further to 16nm and 11nm gate lengths transistors and the full electrical results for these technology generations were presented. Based on the simulated results, the scaled FD-UTB SOI devices achieved the performance targeted by the ITRS.

A comprehensive study of statistical variability in scaled FD-UTB SOI n-channel MOSFET with a physical gate lengths of 22nm, 16nm and 11nm is reported in Chapter 5. The impact of intrinsic parameter fluctuations such as RDF, LER and MGG on V_{th}, I_{on} and DIBL were analysed extensively, both individually and in combination. The results of statistical simulations on 1000 ensembles of microscopically different transistors were simulated using GARAND and the results were presented in this chapter. According to the presented results, even though MGG remained the dominant variability factor for all critical device figures of merits, other variability sources such as RDF and LER also contribute substantially to I_{on} and DIBL fluctuations respectively. None of these variability sources can be ignored for low power circuit design in FD-UTB SOI devices.

The simulation study of statistical reliability in scaled FD-UTB SOI MOSFET was presented in Chapter 6. The reliability issue and its future challenges were reviewed. Then, the effects of combined variability sources at different level of degradations 'without' and 'with' MGG contribution were explored. The distributions of V_{th}, I_{on} and DIBL for three different technology nodes were presented and analysed. In addition, the average of V_{th}, I_{on} and DIBL were also considered and presented at various trapped charge densities. It was found that, the dynamic statistical variability (PBTI degradation) significantly increases the initial 'fresh' variability that originated from RDF, LER and MGG. The trapped charge due to degradation increase the fluctuations in threshold voltage, I_{on} and DIBL.

And finally, the following are the important contributions of this PhD research work:

1) A set of well-scaled realistic FD-UTB SOI transistors for 22nm, 16nm and 11nm has been designed. Based on the simulated results, the scaled FD-UTB SOI transistors achieved the performance targeted by the ITRS.

2) For the first time, systematical physical simulation of intrinsic parameter fluctuations in the well-scaled FD-UTB SOI transistors are conducted on large statistical scale. The impact of RDF, LER and MGG upon threshold voltage, on-current and DIBL are comprehensively analyzed.

3) This research has contributed to the study and understanding of the FD- UTB SOI reliability by carrying out statistical reliability simulation on the previously designed FD-UTB SOI transistors. The impact of trapped charge originated from BTI on threshold voltage shift, on-current degradation and DIBL of the scaled FD-UTB SOI transistors in conjunction with other variability sources have been studied and investigated for the first time.

7.2 Outlook

This PhD research concentrated on the design of realistic highly scaled FD-UTB SOI MOSFET corresponding to advanced technology generations and study of statistical variability and reliability in advanced FD-UTB SOI devices.

There are several possible future research directions stemming from this work. The extraction of statistical compact models that captures both statistical variability and reliability could be one of the first areas of extending the research presented in this thesis. This will be useful to assist the variability aware circuit design into taking into account the impacts of both statistical variability and reliability at the early design stage. In addition, the understanding of the statistical behaviour of the extracted set of device parameters can facilitate the development of statistical parameter generation strategies. This creates an opportunity of collaboration with industry and research groups enabling the development of advanced circuit simulation tools that takes into account the aspects of variability and reliability in future technologies nodes.

The other possibility that could be considered based on this study is extending the device results to the circuit simulation including SRAM yield analysis and statistical standard cell characterization in the presence of statistical variability and reliability. This could provide the designer with useful information on performance and yield distributions after manufactured and aging. Moreover, the information can be obtained using simulations during the early design stages, leading to a significant reduction in development time and considerable cost benefits.

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