High Performance Hydrogen-Terminated Diamond Field Effect Transistors

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Dedicated to the memory of Joyce Powell

“Everything you've learned in school as ‘obvious’ becomes less and less obvious as you begin to study the Universe. For example, there are no solids in the Universe. There's not even a suggestion of a solid. There are no absolute continuums. There are no surfaces. There are no straight lines…”

R. Buckminster Fuller

“Science is the belief in the ignorance of experts”

Richard Feynman

Abstract

Diamond provides extreme properties which make it suitable as a new substrate material for high performance electronics. It has the potential to provide both high frequency and high power performance while operating in extreme environments such as elevated temperature or exposed to corrosive chemicals or radiation. Research to date has shown the potential of diamond for this purpose with hydrogen-terminated diamond surface channel transistors already showing promise in terms of high frequency operation. The inherent instability of using atmospheric molecules to induce a p-type doping at this hydrogen-terminated diamond surface has so far limited power performance and robustness of operation.

This work reports upon the scaling of surface channel hydrogen-terminated transistors with FET gate lengths of 250 nm and 120 nm showing performance comparable to other devices published to date. The gate length was then scaled for the first time to sub-100 nm dimensions with a 50 nm gate length FET fabricated giving record high-frequency performance with a f_T of 53 GHz. An adapted fabrication procedure was developed for this project with special attention paid to the volatility of the particles upon the diamond surface. Equivalent RF circuit models were extracted for each gate length and analysed in detail.

Work was then undertaken to investigate a more stable alternative to the atmospheric induced doping effect with alternative electron accepting materials being deposited upon the hydrogen-terminated diamond surface. The as yet untested organic material $F_{16}CuPc$ was deposited on to hydrogen-terminated diamond and demonstrated its ability to encapsulate and preserve the atmospheric induced sub-surface conductivity at room temperature.

For the first time an inorganic material was also investigated as a potential encapsulation for the hydrogen-terminated diamond surface, MoO_3 was chosen due to its high electron affinity and like $F_{16}CuPc$ also showed the ability to preserve and even slightly enhance the sub-surface conductivity. A second experiment was performed using photoelectron spectroscopy to analyse in-situ deposition of MoO_3 which indicated this material has the ability to induce surface transfer doping by itself without the aid of atmospheric particles.

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Associated Publications

Journals:

- S. A. O. Russell, S. Sharabi, A. Tallaire and D. A. J. Moran, "Hydrogen-terminated diamond field effect transistors with cut-off frequency of 53 GHz," *IEEE Electron Device Letters* vol. 33, pp. 1471-1473, 2012
- D. A. J. Moran, O. J. L. Fox, H. McLelland, S. Russell and P. May, "Scaling of hydrogen-terminated diamond FETs to sub-100-nm gate dimensions," *IEEE Electron Device Letters* vol. 32, pp. 599-601, 2011

Conferences:

- S. A. O. Russell, S. Gupta, H. Gleskova, A. Tallaire and D. A. J. Moran, "The impact of processing on hydrogen-terminated diamond TLM structures exposed to atmosphere and coated with F_{16}CuPc," Hasselt Diamond Workshop SBDD XVIII, Hasselt, Belgium, 2013
- D. A. J. Moran, S. A. O. Russell, S. Sharabi and A. Tallaire, "High frequency hydrogen-terminated diamond field effect transistor technology," *12th IEEE Conference on Nanotechnology (IEEE-NANO)*, Birmingham, UK, 2012
- S. A. O. Russell, S. Sharabi, A. Tallaire and D. A. J. Moran, "Diamond field effect transistors," *ARMMS RF & Microwave Society April 2012 Meeting*, Oxfordshire, UK, 2012
- S. A. O. Russell, S. Sharabi, A. Tallaire, H. McLelland and D. A. J. Moran, "Scaling of diamond FET RF performance, including a cut-off frequency of 53 GHz," 11th *NPL Millimetre-Wave Users Group Meeting*, Luton, UK, 2012
- S. A. O. Russell, S. Sharabi, D. Macfarlane, R. Caterino, J. Garrido and D.A.J. Moran, "A comparison between de-embedding strategies for the extraction of the RF performance of hydrogen-terminated diamond FETs," *Hasselt Diamond Workshop SBDD XVII*, Hasselt, Belgium, 2012
- D. A. J. Moran, O. J. L. Fox, H. McLelland, S. Russell and P. W. May, "Inspection of intrinsic operation and DC performance of 50 nm gate length hydrogen-terminated diamond field effect transistors using an optimised fabrication process," *Hasselt Diamond Workshop SBDD XVI*, Hasselt, Belgium, 2011

Contents

1. Introduction

The invention of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) using silicon in 1960 made possible modern electronics which over the second half of the 20th century progressed rapidly and revolutionised almost every aspect of our lives [1.1]. Prior to this, electronics was a very manual process as individual switches required human input to control them. Now thanks to the FET billions of switches on one processor can be automatically switched on and off with precisely controlled electronic voltages. The electronics industry today is still vastly dominated by silicon devices from calculators to personal computers to satellites. It has been known for many years that there is a limit to silicon's capabilities and today more than ever we need to investigate alternative technological solutions to keep up with increasing demand. This demand is not only for smaller, faster chips as famously discussed by Gordon Moore, but also for other requirements such as high power operation and heat dissipation which are intrinsically limited by the material properties of silicon [1.2].

Over the last three decades, demand for higher frequency operation, high power and the need to operate devices in more extreme conditions has led to research in alternative materials. The 1980s saw research begin into the High Electron Mobility Transistor (HEMT) using alloys of group III and V materials from the periodic table (silicon and germanium being in group IV) [1.3]. For example, gallium arsenide and aluminium gallium arsenide may be used to create heterojunctions which separate charge carriers from their dopants to give a two dimensional electron gas (2DEG) with very high mobility. This has been taken even further in recent years with advances in molecular beam epitaxy (MBE) allowing for more exotic structures to be grown so that lattices may be matched exactly, reducing defects and hence reducing traps to give extremely fast electronic carrier transport. These can typically take the form of pseudomorphic HEMTs (pHEMTs) where a very thin layer of one material is used so the lattice may be stretched or compressed to fit

the lattice parameter of an adjacent material or metamorphic HEMTs (mHEMTs) where a graded composition buffer layer containing a third material is used. While GaAs and InP based structures may be adopted for high frequency applications we need to turn to wide bandgap materials such as GaN and SiC for power. Of these GaN has seen the most success so far achieving over 10 $W.mm^{-1}$ output power density at ~ 2 GHz on a silicon substrate and over 40 $W.mm^{-1}$ output power density at ~ 4 GHz on a silicon carbide substrate [1.4-5]. Performance is still currently limited by its poor thermal management.

In addition to these, diamond has often been described as the ultimate material for power electronics as it has the most extreme properties of the wide bandgap semiconductors. Figure 1.1 illustrates diamond's extreme material properties in comparison to other semiconductor materials. Its wide bandgap gives devices a high electric field breakdown and hence the ability to use high operating voltages much like GaN. Diamond however has a thermal conductivity (in excess of 22 $W.cm^{-1}.K^{-1}$ at room temperature), five times greater than copper, making it ideal to spread heat generated away from devices [1.6]. Intrinsic carrier mobility and high saturation velocity also give diamond a competitive frequency performance, while its robustness makes it favourable for operation in 'extreme' environments.

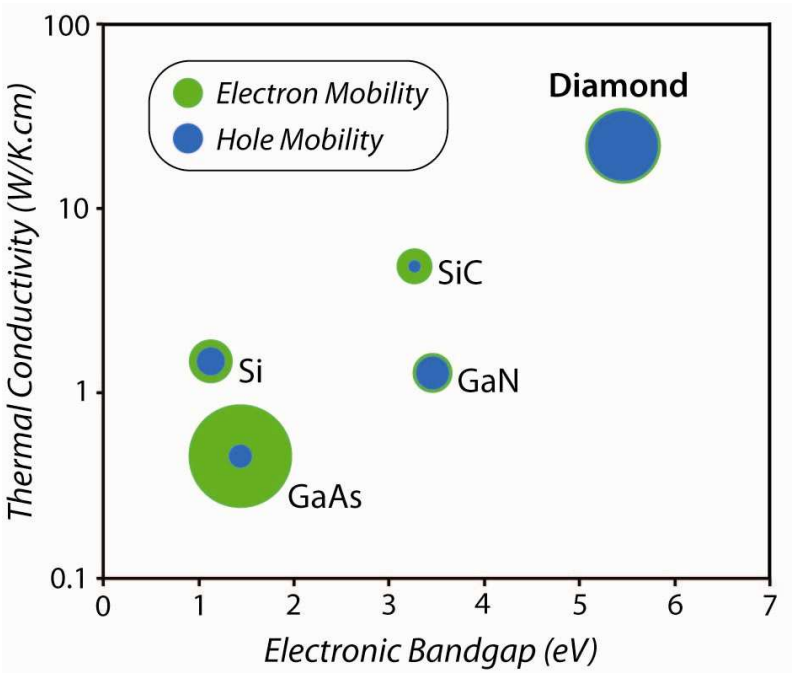


Figure 1.1: Comparison of the material properties of diamond against other semiconductor materials

Due to the large bandgap of diamond (5.47 eV), it is essentially classified as an insulator in its intrinsic form. It is possible albeit challenging to dope and hence making it semiconducting. Some success has been achieved using boron doping and indeed FETs have been demonstrated using this technology [1.7]. Another method is based on an effect known as 'surface transfer doping'. In 1989 M. I. Landstrass and K. V. Ravi found that the resistivity of diamond films significantly lowered when grown in a hydrogen atmosphere and hence given a hydrogen surface termination [1.8]. This was later shown to be due to a unique form of doping involving adsorbed molecules from the atmosphere and again people have demonstrated FETs using this effect [1.9-10]. Both techniques have their limitations. With boron doped devices it is difficult to contact the channel (which is typically formed by a delta-doped boron layer) as a substantial barrier of intrinsic diamond impedes the ohmic contact as well as limiting the gates ability to control the carrier density beneath it. In addition, FETs using the hydrogen-terminated surface have been plagued by instability issues and reduced maximum power operation. Doping and ensuring these dopants become active and stable at room and ideally elevated temperatures remains the greatest challenge with diamond electronics today.

Because of the challenges associated with doping and access to synthetic material, diamond has not yet bettered GaN electronics and reached its full potential. It is unlikely to ever compete with silicon due to the cost involved with growth and processing but specific markets for its application exist similar to GaN such as in radar, satellite communications or where high-performance electronics are required to operate in extreme environments. This project aimed to advance this emerging technology by scaling the already promising performance of hydrogen-terminated diamond surface channel FETs to sub-100-nm dimensions to see just how much frequency performance may be improved and generate greater understanding of the scaling limitations of these devices. This has required the development of an adapted fabrication processes to improve upon performance. In addition to this scaling study, methods to produce more stable devices via deposition of materials onto the hydrogen-terminated diamond surface were also briefly investigated, so diamond may eventually fulfil its high power and stable operation potential.

The bulk of this thesis begins with Chapter 2 which introduces the diamond FET and the theory of its operation. Chapter 3 and Chapter 4 discuss the fabrication and characterisation

techniques respectively involved in this project. Chapter 5 reviews the current literature on diamond electronics, focussing on diamond FETs. Chapter 6 presents the bulk of the results from this work, showing the scaling of diamond FETs to sub-100-nm dimensions and presenting detailed measurements of scaled devices. Chapter 7 investigates several ideas to further adapt the FET device fabrication procedure and material deposition with the aim of fabricating more stable diamond FETs. Finally Chapter 8 concludes the thesis and presents some ideas for future work into this area of research.

References

[1.1] C-T. Sah, "Evolution of the MOS transistor – from conception to VLSI," *Proceedings of the IEEE*, vol. 76, no. 10, pp. 1280-1326, 1988

[1.2] G. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, 1965.

[1.3] T. Mimura, "The early history of the high electron mobility transistor (HEMT)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 780-782, 2002

[1.4] S. Hoshi, M. Itoh, T. Marui, H. Okita, Y. Morino, I. Tamai, F. Toda, S. Seki and T. Egawa, "12.88W/mm GaN high electron mobility transistor on silicon substrate for high voltage operation," *Applied Physics Express*, vol. 2, pp. 061001-1-061001-3, 2009

[1.5] Y-F. Wu, M. Moore, A. Saxler, T. Wisleder and P. Parikh, "40-W/mm double field-plated GaN HEMTs" *Proceedings of IEEE Device Research Conference*, pp. 151-152, 2006

[1.6] C. J. H. Wort and R. S. Balmer, "Diamond as an electronic material," *Materials Today*, vol. 11, no. 1-2, pp. 22-28, 2008

[1.7] H. El-Hajj, A. Denisenko, A. Kaiser, R. S. Blalmer and E. Kohn, "Diamond MISFET based on boron delta-doped channel," *Diamond and Related Materials*, vol. 17, no. 7- 10, pp. 1259-1263, 2008

[1.8] M. I. Landstrass and K. V. Ravi, "Resistivity of chemical vapor deposited diamond films," *Applied Physics Letters*, vol. 55, no. 10, pp. 975-977, 1989

[1.9] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook, and S. E. Coe, "Diamond FET using high-quality polycrystalline diamond with f_T of 45 GHz and f_{MAX} of 120 GHz," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 570–572, 2006.

[1.10] K. Hirama, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Umezawa and H. Kawarada, “High-performance p-channel diamond MOSFETs with alumina gate insulator,” *IEDM Technical Digest*, pp. 873–876, 2007.

2. Diamond Field Effect Transistors (Theory)

The type of diamond FET discussed in the bulk of this work is known as a 'surface channel' or ‘hydrogen-terminated’ diamond FET. Atmospheric particles will readily adsorb on to a hydrogen-terminated diamond surface and initiate a transfer of charge due to the negative electron affinity (NEA) given to the diamond by hydrogen-termination [2.1]. This produces a shallow sub-surface p-type doped layer where electrons are displaced from the diamond to the atmospheric molecules, which may be used to create FETs [2.2]. Aside from this novel doping mechanism these devices function in much the same way as a standard Metal-Semiconductor FET (MESFET), using a gate deposited directly on to the diamond surface to control charge and hence current flow within the channel between source and drain ohmic contacts.

This chapter begins by discussing how synthetic diamond is synthetically ‘grown’ and the extreme material properties it possesses, followed by an in depth look at the surface transfer doping model as well as a brief look at other routes to doping diamond. Surface transfer doping is not limited to just atmospheric adsorbate molecules. Theoretically any molecule with a high enough electron affinity and available energy states should allow this charge transfer to happen, hence alternative electron accepting materials are also discussed [2.3]. To fully understand the operation of these surface channel FETs it is important to look at some basic semiconductor theory and how it relates to device operation i.e. how charge moves within a semiconductor and across metal-semiconductor interfaces. Finally once diamond FETs have been fabricated it is important to understand various figures of merit to assess how well they perform and to accurately understand their operation.

2.1 Synthetic Diamond

Carbon can manifest itself in several different forms or 'allotropes' due to the difference in bonding between the individual carbon atoms. There are six electrons present in each atom in the configuration $(1s)^2(2s)^2(2p)^2$. One would assume the two electrons in the 2p outer shell are the only ones capable of bonding however orbital hybridisation of the 2s and 2p orbitals may occur as the energy difference between the 2s and 2p state is small enough a tiny perturbation such as a nearby atom will excite an electron from the 2s to the 2p state. This gives several possibilities for carbon bonding with sp, sp^2, sp^3 and even combinations of s, p and d orbitals possible [2.4]. The sp^2 and sp^3 configurations are shown in Figure 2.1.1. It is energetically favourable for carbon to bond together in the sp^2 configuration which most often gives the material commonly known as graphite.

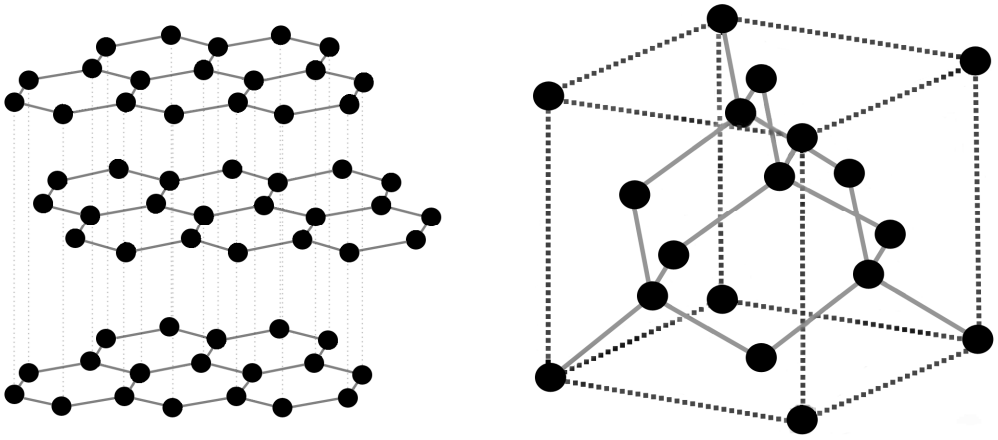


Figure 2.1.1: Carbon bonded in the graphite sp^2 configuration (left) and diamond sp^3 configuration (right, dotted line represents unit cell)

Graphite consists of a continuously repeating hexagonal sheet of carbon atoms stacked on top of each other and weakly bonded together by Van der Waals forces. Other related forms of sp^2 carbon are a single sheet of graphite known as graphene or carbon nanotubes which are essentially a layer of graphene rolled up to form a tube. One of the characteristic properties of this form of carbon is it is incredibly strong in the horizontal plane (stronger than diamond even) but very weak in the vertical plane and layers will readily peel apart with little applied force.

Diamond is an allotrope of carbon that occurs naturally as a mineral and can be found in many locations throughout the world. To form, it usually requires conditions of both high pressure and high temperature. Diamond bonds in an sp3 configuration with its lattice identical to that of silicon or germanium (face centred cubic lattice with a second identical set of atoms shifted by ¼ of the width of the unit cell as seen in Figure 2.1.1) however diamond is much stronger due to the covalent bond length between atoms being much shorter. This is due to fewer electron shells being present in carbon than silicon or germanium meaning electrons are drawn closer to the positively charged atomic nuclei. The lattice constant has been empirically measured to be 0.357 nm whereas in silicon it is 0.564 nm and germanium 0.543 nm [2.5]. The bonding angle of all three structures is 109.5 degrees thus unlike graphite diamond is strong in all directions.

Over the last half century it has become possible to replicate the conditions under which diamond forms in a laboratory environment. Originally, natural diamond stones were tested for their electronic properties [2.6] but it is unlikely all the properties we desire will be found in a single stone. Synthetic growth however can tailor a 'stone' for the required purpose. Today there are three well recognised routes to growing diamond. The first synthetically created diamonds came in 1954 when H. T. Hall of General Electric utilised apparatus in the form of a press and created high pressure high temperature (HPHT) synthesis involving a graphite sample and transition metal solvent catalyst compressed under ~8.4 GPa pressure for one hour [2.7]. In 1962, Yevgeny Zababakhin and a team of scientists involved in nuclear weapons design in the Soviet Union experimented with TNT/RDX explosives in a closed chamber [2.8]. The blast turned the carbon in the explosives into nanodiamond dust. This mixture is also rich in non-diamond carbon so the product is too small and contaminated to be useful for devices.

Chemical Vapour Deposition (CVD) is currently the most effective method for systematically producing relatively defect free diamond. It can be performed at comparatively low pressures and relies on decomposition of a carbon containing gas compound via DC arc jet discharge, hot filament or microwave plasma [2.9-11]. Microwave plasma enhanced CVD (PECVD) is most used today due to the precise controllability of plasma, relatively high growth rate and the lack of necessity for extreme pressure and temperature apparatus hence relatively low cost. The carbon containing gas (methane is standard) is diluted with atomic hydrogen which helps to stabilise diamond

growth as C-H bonds prevent formation of other non-diamond carbon contaminants. This leaves the as grown diamond crystal hydrogen-terminated at the crystal edges (and semiconducting in atmosphere). This occurs as dangling carbon bonds require another atom at the surface to become energetically stable. Hydrogen is suitable for this purpose and the hydrogen rich growth conditions coupled with being allowed to cool in a pure hydrogen atmosphere give rise to this surface termination. This termination will change to oxygen (insulating) when subjected to an acid clean used to remove non-diamond contaminants e.g. H_2SO_4/HNO_3 or exposure to oxygen plasma. From this CVD method it is possible to replicate and in some cases even improve on the extreme properties of natural diamond.

As previously mentioned diamond has a very large bandgap for a semiconductor and it could almost be considered an insulator. Instead however it falls in to the category of wide bandgap semiconductor. When discussing electronic properties any material can generally be classified in one of three categories: conductor, insulator or semiconductor. If many atoms are bought closely together to form solid crystals we can describe them via band theory.

Quantum mechanics suggests every atom has a series of allowed energy states and when bought together to form a solid these will become allowed energy bands (there are still individual allowed energies but they are so close together they resemble continuous bands). The lower bands are known as valence bands (E_V) where electrons are tightly bound to the atomic nuclei, the upper band is known as the conduction band (E_C) which as the name suggests involves electronic conduction throughout the material. The valence bands and conduction bands are separated by an energy bandgap (E_G). The Fermi level (E_F) is the energy where the probability of an energy state being filled is half, which for an intrinsic (pure semiconductor with no impurities or 'dopants') semiconductor will be in the middle of the bandgap. Insulators have a full valence band and empty conduction band with a large bandgap, semiconductors have an almost full valence band and almost empty conduction band with a relatively small bandgap and conductors have lots of states filled in the conduction band and there is no bandgap with the conduction and valence bands effectively overlapping. Figure 2.1.2 shows an illustration of these bands and how they may be occupied.

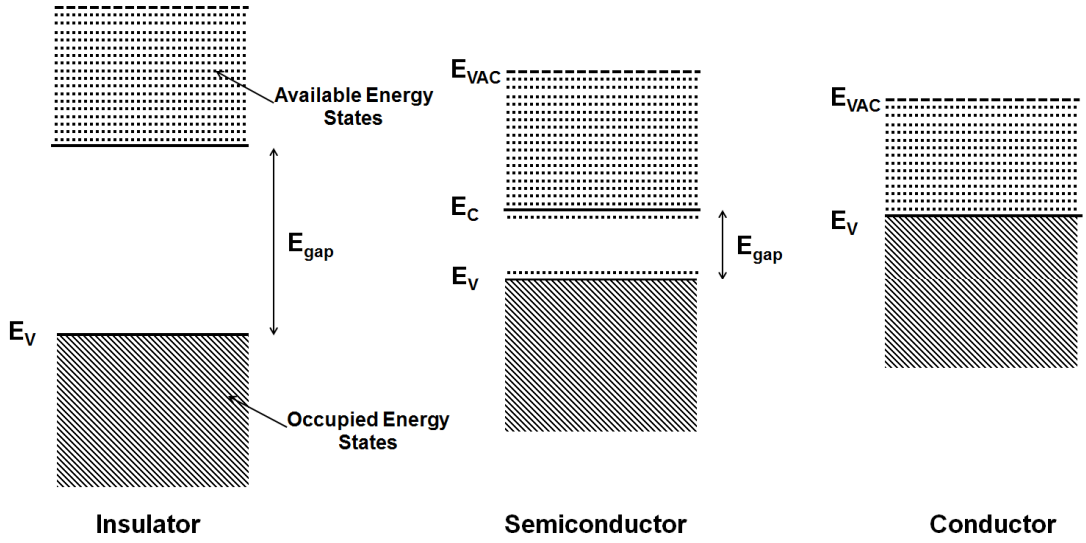


Figure 2.1.2: Band makeup and occupation in insulators, semiconductors and conductors

Table 2.1.1 shows that for material properties directly related to high power electronics, diamond surpasses all of its competitors while also having competitive properties for high frequency operation.

	Si	**GaAs**	**4H:SiC**	**GaN**	**Natural Diamond**	***CVD Diamond***
Bandgap	1.12	1.43	3.26	3.45	5.47	5.47
Electric Breakdown Field ($MV.cm^{-1}$)	0.3	0.4	3	5	10	10
Intrinsic Electron Mobility ($cm^2.V^{-1}.s^{-1}$)	1450	8500	900	440	200-2800	4500
Intrinsic Hole Mobility ($cm^2.V^{-1}.s^{-1}$)	480	400	120	200	1800-2100	3800
Saturation Velocity (Electrons) ($x10^7$ $cm.s^{-1}$)	1	1	3	2.5	2	2
Saturation Velocity (Holes) ($x10^7$ $cm.s^{-1}$)	0.6	1	1	-	0.8	0.8
Thermal Conductivity ($W.cm^{-1}.K^{-1}$)	1.6	0.46	5	1.3	22	24

Table 2.1.1: Intrinsic material properties of diamond compared to other semiconductors [2.12-14]. Note that 4H:SiC values are quoted as it is the form of silicon carbide shown to have highest mobility [2.15]

The thermal conductivity of 24 $W.cm^{-1}.K^{-1}$ at room temperature for diamond is perhaps one of the most attractive features which again stems from the tightly packed lattice structure which transmits lattice vibrations (or phonons) efficiently. This thermal conductivity is almost five times larger than SiC and almost twenty times larger than GaN. Diamond's intrinsic low-field mobility is also much larger than its competitors which is important to produce low resistance access regions and fast acceleration to saturation velocity in a device. Although mobility is traditionally linked to high frequency operation, transistors are typically operated at high-field so we also care about saturation velocity and this too has a competitive value. Velocity saturation data for holes in GaN is not presented as p-type doping is still difficult to achieve with good activation [2.16]. SiC saturates near its breakdown field making velocity saturation difficult to achieve in reality [2.13]. Diamond saturation velocity is not only high but it saturates at an electric field of ~10 $kV.cm^{-1}$ - well below the breakdown field giving it lots of potential for high power operation [2.13]. Aside from these device related properties diamond has other features that make it desirable such as a low dielectric constant of 5.7 in comparison to 9.7 for GaN. This makes it desirable for RF electronics as a lower dielectric constant can give lower loss to the substrate making circuit elements such as transmission lines perform better [2.17-18]. Diamond is also transparent from the far infra-red to deep ultra-violet part of the electromagnetic spectrum making it suitable for many optical applications [2.13]. Finally diamond is famously renowned for its mechanical strength which comes from its bonding and structure as discussed previously making it robust and inert in terms of both chemistry and radiation. This structural strength unfortunately hinders diamond when it comes to doping for electronic applications however as we shall see in the next section. These fantastic properties are not all possible in natural stones, for example defects will hinder carrier transport and lower intrinsic mobility [2.13].

There are several straightforward expressions devised to directly compare semiconductor materials for purpose. Johnson's figure of merit is shown in equation 2.1.1 and shows the power-frequency product for high frequency and high power transistor operation where E_B is the breakdown field and v_s the saturation velocity [2.19]. Keye's figure of merit is shown in equation 2.1.2 and describes the thermal limit of the frequency performance where χ is the thermal conductivity, c the speed of light and and ε_0 the dielectric constant of the semiconductor [2.20]. Finally Baliga's figure of merit is shown in equation 2.1.3 and describes material parameters to show the conduction loss in power FETs at low frequency

where conduction loss dominates (higher frequencies need to account for switching losses) μ represents mobility and E_G the bandgap of the semiconductor [2.21].

$$JFoM = \frac{E_B^2 v_s^2}{4\pi^2} \quad \textbf{2.1.1}$$

$$KFoM = \chi \sqrt{\frac{c v_s}{4\pi\varepsilon_0}} \quad \textbf{2.1.2}$$

$$BFoM = \varepsilon_0 \mu E_G^3 \quad \textbf{2.1.3}$$

Table 2.1.2 shows a normalised comparison (silicon being set to 1) of these figures of merits again for SiC, GaN and diamond and it is clear diamond can exceed all its competitors. Figure 2.1.3 shows a single crystal CVD diamond sample to scale grown from an HPHT seed and the grains visible in a polycrystalline diamond sample also grown via CVD but without a diamond seed.

	4H:SiC	**GaN**	**Natural Diamond**	***CVD Diamond***
Johnson's FoM	410	280	8200	8200
Keye's FoM	5.1	1.8	32	32
Baliga's FoM	290	910	882	17200

Table 2.1.2: Comparison of wide bandgap semiconductors in terms of power device figures of merit (normalised to silicon being 1) [2.13]

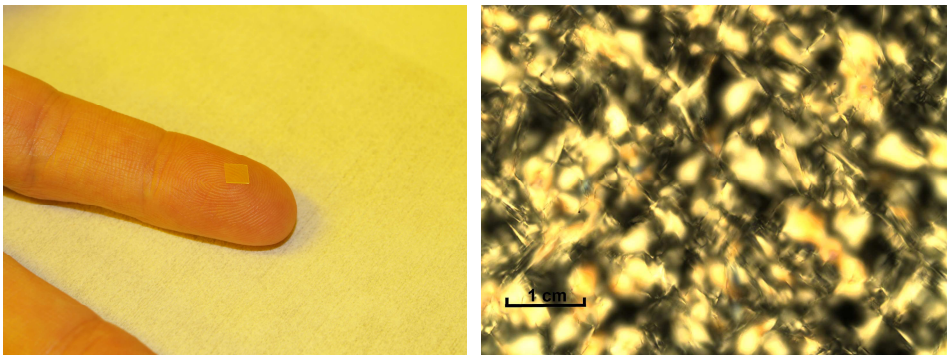


Figure 2.1.3: Single crystal diamond sample showing scale (left), polycrystalline diamond grains seen via dark field microscopy at 5x magnification (right)

The major challenges left in synthetic diamond growth today are reducing its cost to make it a more competitive technology as well as the ability to produce large area single crystal material. This is difficult as the CVD process requires a natural diamond seed (usually from costly HPHT synthesised material). There is an alternative lower cost solution, polycrystalline diamond can be grown heteroepitaxially on many substrates and has already found uses in coatings for cutting tools among other mechanical functions. 1 inch diameter wafers grown on silicon substrates have been demonstrated and the diamond itself is of a high quality although it is found in grains of a few nm to ~100 μm [2.22]. It is possible to fabricate individual electronic devices within these grains but it would seem unsuitable for amplifier or circuit fabrication as between the diamond grains are boundaries containing conductive graphite and amorphous carbon. More research needs to be done but it has been suggested these boundaries inhibit diamond's superb thermal conductivity and may do the same electrically.

2.2 Doping Diamond

Doping a semiconducting material traditionally involves introducing impurity atoms in to a solid with either donor atoms, which contain an excess of electrons compared to the intrinsic material for n-type doping (shifting E_F towards the conduction band), or acceptor atoms which have a deficiency of electrons and accept electrons from the original lattice creating positively charged holes for p-type conduction (shifting E_F towards the valence band). As carbon is in group IV of the periodic table group III elements would be natural acceptors and group V elements donors. Doping of diamond in a conventional manner has proved extremely difficult to date due to the strong bonds and short inter-atomic spacing that gives diamond its immense mechanical strength [2.13]. Ideally, when attempting to dope a semiconductor the aim is to achieve substitutional doping where an atom of the original lattice (in this case carbon) is replaced or 'substituted' by a dopant atom. Another possibility is interstitial doping where dopant atoms lay between the original lattice atoms. If an attempt is made to insert a relatively large atom such as arsenic in to the diamond structure, it will disrupt the lattice, diminishing the desirable properties that were there in the first place. So this limits doping candidates to smaller sized atoms such as boron, nitrogen and phosphorous. It would take very large temperatures to achieve diffusion of dopant atoms in diamond (~1500° C for nitrogen) and in any case these temperatures would cause graphitisation of the diamond [2.23]. Ion implantation requires a post-implant anneal to ‘heal’ lattice defects which again would lead to graphitic growth or amorphous

carbon regions which compensate the charge carriers from doping and also places strain on the lattice.

One idea is to include dopant materials in the original diamond growth i.e. inserting boron gas during CVD. Boron is a common impurity found in natural diamonds and gives them a blue colour [2.24]. It is the shallowest acceptor currently known for diamond with activation energy of 0.37 eV. This is too large to be useful for room temperature operation unless heavily doped (> 10^{18} cm^{-3}), at this point hopping conduction between impurity atoms occurs rather than conventional band conduction [2.25]. Boron doped diamond can also be made semi-metallic if doped to concentrations > 10^{20} cm^{-3} [2.25]. As illustrated in Figure 2.2.1 the lower the activation energy the closer the dopant energy state to either the valence (p-type) or conduction (n-type) band, 0.37 eV is over a third of the bandgap of silicon and requires a large amount of thermal energy to activate.

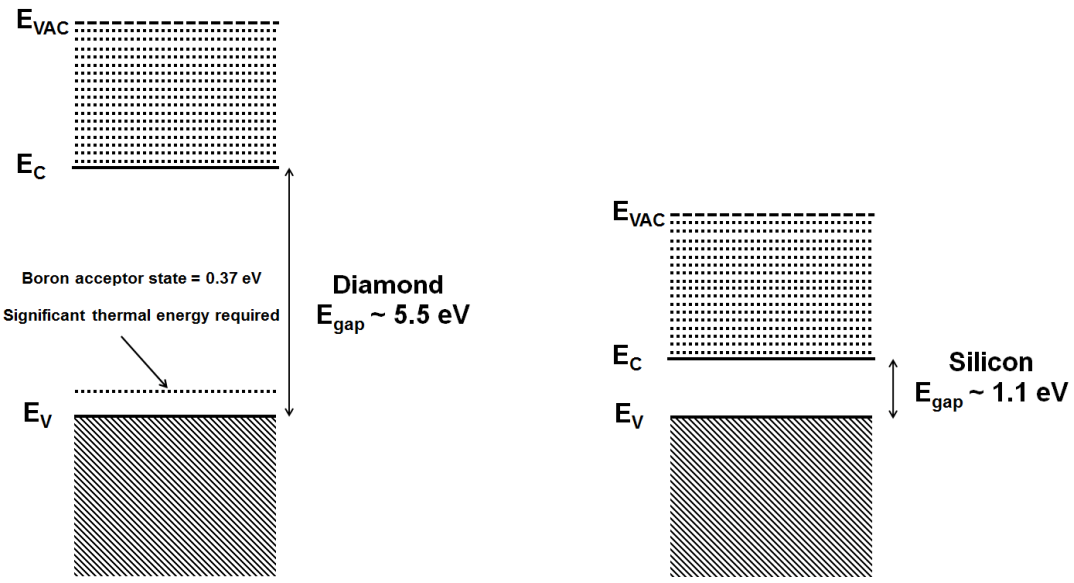


Figure 2.2.1: Boron activation in diamond

N-type doping has even tougher challenges to overcome with nitrogen having a donor activation energy of 1.7 eV [2.13]. Phosphorous is lower but still challenging at 0.6 eV [2.13]. Sulphur is a potential candidate which is still under some debate, being a group VI element it has the potential to be a 'double donor' although practical experiments have yet to produce conclusive proof of theoretical predictions [2.26]. Similarly arsenic has predicted activation energy of 0.4 eV but there is little empirical evidence to confirm this

to date and antimony is predicted to be 0.3 eV but the antimony atom is much larger than the carbon atom it is trying to displace and as such is not suitable [2.26]. Aluminium is also predicted to be an electron acceptor at 1 eV but again is a relatively large atom with higher activation energy than boron [2.27]. Impurity complexes such as an individual nitrogen atom bonded to four silicon atoms or nitrogen-hydrogen-nitrogen have also been suggested from theoretical modelling with donor energies as low as 0.09 eV but again there is little to no proof of any experimental success and it is possible these complexes are insoluble in diamond [2.28-29]. There have also been some controversial results involving boron-deuterium complexes which are as yet not widely accepted [2.30].

Boron remains the shallowest conventional dopant in diamond but the need for high doping concentrations hampers the carrier mobility. A solution which has seen success in III-V FET structures is 'delta-doping' and the natural candidate in diamond would be boron. The principle involves a thin (ideally one atom thick) layer of boron atoms grown in the diamond so the wave function of the charge carriers overlap in to the intrinsic diamond and hence a large percentage of charge is physically separated from the boron atoms and moved into the intrinsic diamond as seen in Figure 2.2.2. However in reality, doping profiles are currently around 1 nm wide and while Hall mobility of 900 $cm^2.V^{-1}.s^{-1}$ has been observed room temperature conductivity mobility and field effect mobility is only 1-4 $cm^2.V^{-1}.s^{-1}$ seriously hampering the potential of devices using this technique [2.31].

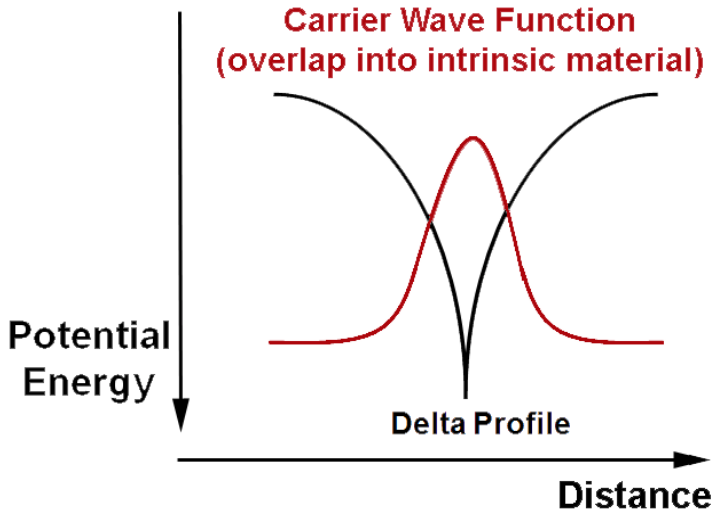


Figure 2.2.2: Delta-doping profile

As grown surface termination of CVD diamond tends to be hydrogen-terminated but may easily become oxygen-terminated after being subjected to an acid surface clean [2.32]. This oxygen-termination is stable with regards to elevated temperature or chemical exposure and is typically used for delta-doped devices. The hydrogen-termination is also relatively stable and will remain unless heated to > 800˚ C or subjected to oxygen plasma [2.32]. A clean non-terminated diamond surface in vacuum has an ionisation potential (IP) of 5.9 eV, this being the energy required to remove an electron from the valence shell of an atom and ionise it. Its electron affinity (χ) is 0.4 eV, this being the energy required to remove one electron from the conduction band and ionise it [2.33]. This is illustrated diagrammatically in Figure 2.2.3.

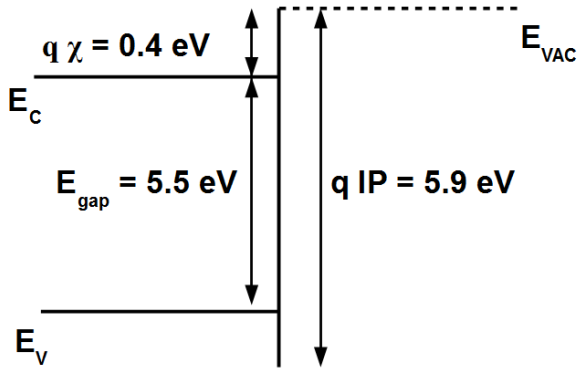


Figure 2.2.3: Energy band diagram of clean diamond surface

Oxygen-termination of the diamond surface raises its ionisation potential to 7.2 eV with χ of 1.7 eV [2.33]. Hydrogen-termination however lowers the ionisation potential to 4.2 eV resulting in a negative χ (NEA) of -1.3 eV [2.33]. This implies the vacuum level (an energy level defined somewhere outside the material where potential to confine electrons has become effectively zero so they have become ionised) actually lies below the conduction band energy, meaning electrons near the surface will readily leave or at least no substantial barrier impedes them from doing so. The energy band diagrams for oxygen and hydrogen-terminated diamond are shown in Figure 2.2.4.

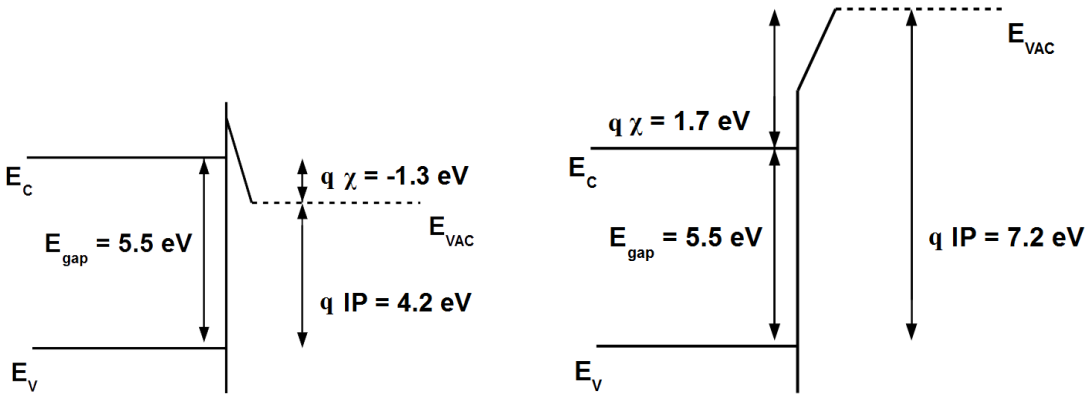


Figure 2.2.4: Energy band diagram of H-terminated (left) and O-terminated (right) diamond surface

This has shown promise in the potential use of hydrogen-terminated diamond as a cold cathode electron emitter but may also find use in active electronic devices. A form of doping using this effect known as 'surface transfer doping' is currently a popular topic of research and the focus of the devices presented in this thesis. Diamond is unique in that changing its surface termination can alter χ by up to 3 eV. Normally H-termination raises IP in semiconductors, hydrogen-terminated diamond has the lowest IP of any semiconductor as shown in Figure 2.2.5 [2.33].

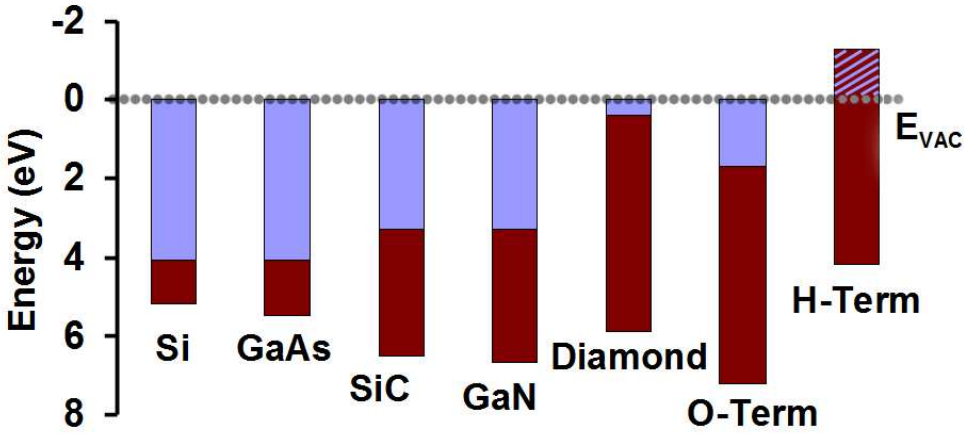


Figure 2.2.5: Comparison of semiconductor electron affinities (blue) and bandgaps (red)

2.3 Surface Transfer Doping

The NEA found in hydrogen-terminated diamond can be utilised as a doping mechanism with the aid of suitable electron accepting materials with high electron affinities. These materials will accept electrons from the surface much like a conventional p-type dopant would from a bulk material leaving behind a thin layer of holes ~ 10 nm below the diamond surface [2.34]. This layer is so thin it behaves as a quasi-two-dimensional hole gas (2DHG) similar to the two dimensional electron gas (2DEG) found in modulation doped III-V heterostructures. The best FET performance seen in diamond so far has been achieved using the surface transfer doping method [2.35].

The initial discovery of surface transfer doping was somewhat unexpected. Researchers Ravi and Landstrass reported seeing the conductivity of diamond raise by ten orders of magnitude when exposed to hydrogen plasma and subsequently exposed to atmospheric conditions, but this leap in conductivity could be reversed by a mild anneal of ~300º C [2.36]. It has since been proven that atmospheric molecules will adsorb on to the hydrogen-terminated diamond surface and instigate surface transfer doping as seen in Figure 2.3.1 [2.1]. At this point it is important to note hydrogen-termination alone is not enough for surface transfer doping and that a suitable surface acceptor material must be present for the diamond valence band electrons to transfer to.

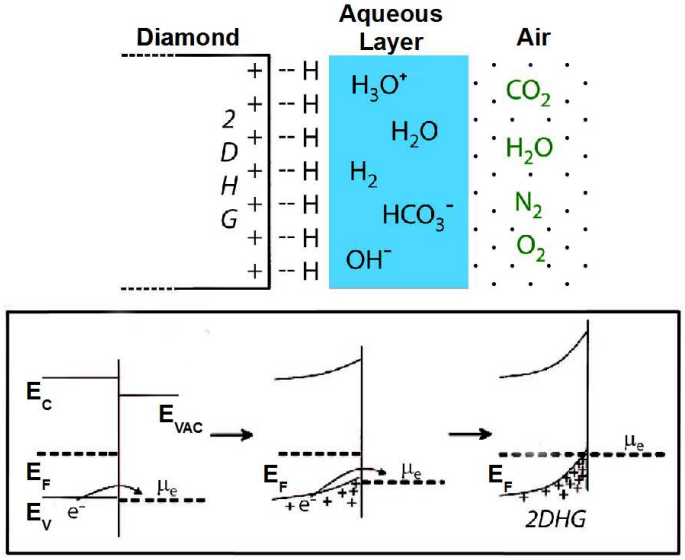


Figure 2.3.1: Illustrated charge transfer from diamond to aqueous layer with associated band diagrams

Although today it is widely accepted that atmospheric particles play the role of electron acceptors in this surface transfer doping process it is still not entirely clear how. The low ionisation potential of hydrogen-terminated diamond still requires electron acceptors to have electron affinities > 4.2 eV so that the lowest unoccupied molecular orbital (LUMO) aligns close to or below the diamond's valence band instigating conditions suitable for electron transfer. No commonly found atmospheric particle has anything close to this figure, in fact most are below 2.3 eV [2.1].

Rather than a simple electron transfer from diamond surface to adsorbate an electrochemical interaction is thought to be at work. F. Maier *et al* have suggested a thin aqueous wetting layer of various atmospheric particles forms on the surface and redox reactions between this and the diamond surface give rise to the electron transfer mechanism as shown in equation 2.3.1. [2.1]

$$diamond + \ 2H_3O^+ \longleftrightarrow diamond^{2+} + H_2 + 2H_2O \qquad \textbf{2.3.1}$$

Further calculations by Maier involving the Nernst equation have shown the chemical potential of this hydronium redox couple to be between -4.2 and -4.3 eV assuming the aqueous layer pH is between 5 and 7 [2.1]. This chemical potential (μ_e) lies slightly below the valence band of hydrogen-terminated diamond allowing electrons to leave the diamond to balance energy until charge neutrality is reached and the chemical potential and diamond Fermi level align as pictured in Figure 2.3.1. This gives spatially separated holes and electrons and an electrostatic potential between them and band bending occurs at the hydrogen-terminated diamond surface. It is possible even for the Fermi level to dip below valence band leaving a degenerate semiconductor and the quasi-2DHG if the surface transfer doping is particularly efficient and produces a high enough hole concentration.

At this point it may be pertinent to ask again why this happen in only hydrogen-terminated diamond and no other semiconductor materials. Looking back at figure 2.2.5 no other candidate has the suitable valence band maximum to align with this μ_e. Even so hydrogen-terminated diamond has an unpinned Fermi Level due to dangling bonds being reduced to such a level that surface states are low enough they are below the Mott-Schottky limit, this allows for surface band bending and charge transfer at the interface [2.2]. Although currently the best description for the interaction between atmospheric adsorbate molecules

and hydrogen-terminated diamond this model is far from complete. Other atmospheric molecules such as hydroxyl ions and ozone have also been suggested as candidates for similar aqueous redox reactions [2.37].

The sub-surface conductivity of surface transfer doped diamond samples measured by F. Maier *et al* are similar to those originally measured by Ravi and Landstrass ~ 10^{-4}–10^{-6} $S.m^{-1}$ (up ten orders of magnitude from ~ 10^{-16} $S.m^{-1}$ for insulating oxygen-terminated diamond surfaces) at room temperature [2.36]. Surface sheet carrier concentration typically ranges from 10^{12}-10^{13} cm^{-2} depending on efficiency of the doping [2.38] and these carriers tend to have a mobility between 30-70 $cm^2.V^{-1}.s^{-1}$ depending on material quality but can reach over 100 $cm^2.V^{-1}.s^{-1}$ [2.39]. This mobility value is significantly lower than the 3800 $cm^2.V^{-1}.s^{-1}$ quoted for holes in intrinsic diamond and is still a topic for debate. It is possible that the electrostatic potential initiated by surface transfer doping pulls the holes very close to the surface where they are subject to scattering and trapping processes. The sheet resistance of the 2DHG is typically found to be between 10 - 15 kΩ. The highest mobility recorded in a surface transfer doped sample to date is 335 $cm^2.V^{-1}.s^{-1}$ with a carrier concentration of only 7 x 10^{11} cm^{-2} suggesting there may be a trade-off between the two values [2.40]. In principle, electrons transferred to the adsorbate molecules will also have a contribution to the conductivity but their mobility through the adsorbate layer will determine if this contribution may be neglected or not. Surface transfer doping is fundamentally linked to the amount of charge carriers available at the surface which in turn relies on the surface orientation of diamond samples as a higher concentration of surface atoms gives rise to more potential charge carriers. The most common form of single crystal diamond synthetically grown is (001) which is the orientation used in this project primarily because it is the easiest to grow. Others are possible however such as (111) which due to its crystal orientation provides a higher density of carbon atoms at the surface meaning potential for more carriers. These orientations are more susceptible to stacking faults and the creation of twin crystals during growth which are detrimental to carrier transport [2.41].

The main drawback and perhaps the main factor limiting transfer doped diamond becoming commercially viable for devices presently is its inherent instability. Adsorbate particles will desorb from the surface at > 250º C and although they will eventually return when re-exposed to the atmosphere there is an urgent need for a suitable ‘passivation’

process to encapsulate the diamond surface to prevent degradation during operation [2.1]. This is especially true as diamond is considered a promising candidate for high power electronics and operation in extreme environments both of which are not possible with this current atmosphere dependent process. An alternative is the use of suitably high χ materials for electron accepting as a replacement for the atmospheric molecules route, this could perhaps be used in conjunction with an encapsulation layer.

2.4 Alternative Electron Acceptors and Dielectric Coatings

As touched upon in the previous section surface transfer doping does not necessarily have to rely upon a chemical reaction at the diamond surface. The basic principle is more straightforward in that because hydrogen-terminated diamond has a uniquely low ionisation potential and minimal interface state density, it is possible to match it to a material with $\chi \geq 4.2$ eV and instigate electron transfer to the materials lowest unoccupied molecular orbital (LUMO) or conduction band minimum as seen in Figure 2.4.1 [2.3].

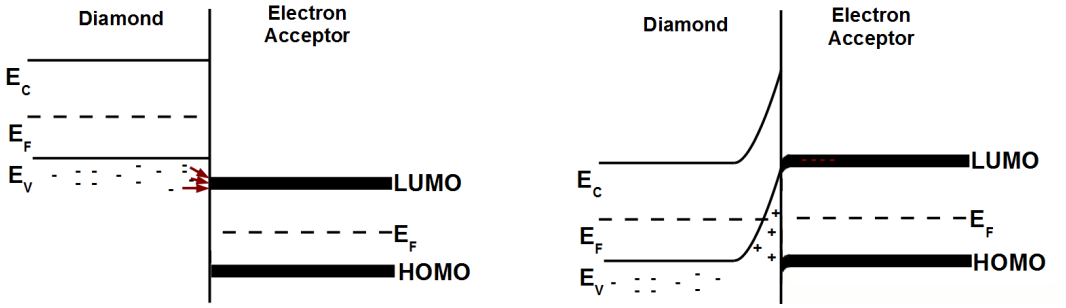


Figure 2.4.1: Band diagrams of charge transfer from diamond to an organic electron accepting material

This is a recent development in diamond electronics research and the only materials to see any substantial investigation thus far have been fullerenes [2.3]. These are another allotrope of carbon featuring carbon atoms arranged in the sp^2 configuration like graphite but instead of being in stacked sheets they are arranged in a spherical structure as shown in Figure 2.4.2.

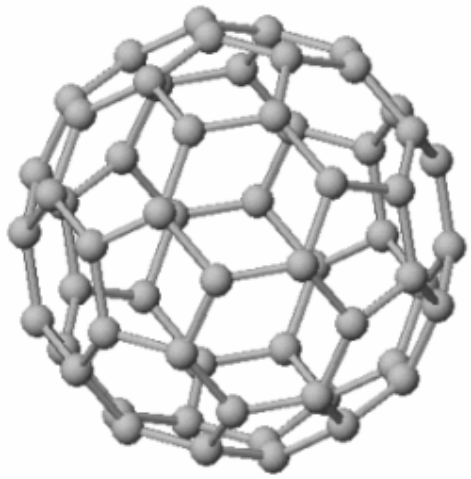


Figure 2.4.2: A C_{60} molecule of the carbon allotrope fullerene, other examples exist such as C_{70}

Fullerenes have already seen success as electron accepting materials when employed in organic electronic polymer structures for applications such as polymer solar cells [2.42]. In terms of chemistry they are strongly oxidising which would imply they have a high χ [2.42]. There is some debate as to the exact value for χ for a C_{60} molecule. Values have been quoted in the range 2.7 - 3.3 eV but even for the upper bound this is still well below the 4.2 eV threshold. It is however generally accepted that when combined into a solid (fullerite) the value for χ raises by ~ 1.3 eV making it viable at high levels of coverage [2.33].

As well as pure carbon fullerenes it is also possible to fluorinate these molecules (adding fluorine atoms on to the basic C_{60} sphere) to varying degrees. The more fluorine atoms that are added the greater the χ becomes due to the high χ of fluorine. $C_{60}F_{48}$ is the most highly fluorinated form of an individual C_{60} molecule that has been synthesized thus far [2.43]. This has χ of ~ 4 eV (increasing to ~5 eV when combined in to solid fullerite) and can instigate surface transfer doping on roughly a 1:1 basis i.e. each $C_{60}F_{48}$ molecule accepts an electron until saturation which is reached with a single mono-layer coverage of $C_{60}F_{48}$ giving sheet carrier concentrations in excess of 10^{13} cm^{-2}[2.43].

Some investigation into other organic materials using photoelectron spectroscopy (PES) has begun with a recent review by W. Chen *et al* detailing preliminary results for

pthalocyanine (CuPc), 2,3,5,6-tetrafluoro-7,7,8,8-tetracyanoquinodimethane (F_4-TCNQ) and 7,7,8,8-tetracyanoquinodimethane (TCNQ) molecules with χ of 2.7, 5.24 and 4 eV respectively [2.44]. As expected F_4-TCNQ and TCNQ instigated surface transfer doping whereas CuPc does not. This leaves a tantalisingly vast array of possibilities to be explored with plenty of other high χ organic and potential inorganic materials yet to be investigated. The only caveats are the material needs to possess sufficiently high χ, have enough states in its LUMO or valence band to accept carriers, be non-conducting in isolation and be stable in atmosphere. There are however other factors to be considered in practice as different interfaces may lead to different levels of charge trapping and reliability however the potential is clear.

Although these alternative electron accepting materials have seen success in replicating the surface transfer doping process, stability of conduction through the 2DHG still remains an issue for investigation. Fullerenes are arguably no more stable than atmospheric particles on the diamond surface once the surface is heated > 250º C [2.45]. They will sublimate at only a few hundred degrees centigrade (even lower for the more highly fluorinated case) and are as yet untested in terms of electronic device characterisation, it is still unknown if these molecules will leave the sub-surface holes mobile enough to produce currents suitable for FET devices. An inorganic material may be a better choice in terms of stability and if an organic (or atmospheric) molecule is still deemed best it would be prudent to find a suitable dielectric material to encapsulate this to ensure stability of device performance. So far no conclusive evidence has been found to suggest any dielectric alone can preserve the surface conductivity sufficiently. The problem lies in the fact that deposition temperatures for potential encapsulation materials are generally high (~800º C for a technique such as metal organic chemical vapour deposition (MOCVD)) so preliminary research in to AlN was limited [2.46]. However recent research in to low temperature atomic layer deposition (ALD) of aluminium oxide (Al_2O_3) has shown some promise [2.47].

2.5 Semiconductor Theory

As surface transfer doping initiates a p-type doping in diamond, this section and beyond will attempt to address mainly hole rather than electron transport in semiconductors although in some cases it is far more intuitive to derive expressions using the electron. A hole behaves like a missing electron and can be modelled simply as an electron with

positive charge. The mass of an electron in free space (m_0) = 9.11 x 10^{-31} kg but this is not quite the case in a semiconductor crystal as both electrons and holes are not 'free', they are confined by a potential arising from the atomic nuclei. When confined in a crystal lattice, carriers can be modelled semi-classically to behave like a free electron but with an altered mass depending on the carrier's position within the conduction or valence band. Holes are of course imaginary. It is just simpler to model the lack of a single electron (hole) in the valence band rather than the movement of electrons but when discussing the effective mass of a hole we are in fact talking about the acceleration of a hole related to the imaginary force on it from the effective mass. Effective mass (m*) can be shown to be [2.48]:

$$m^* = \hbar^2 \left(\frac{d^2 E}{dk^2} \right)^{-1} \qquad \textbf{2.5.1}$$

Where ħ is the reduced Planck constant, E energy and k wave number (which is momentum divided by ħ. This does in general give a positive effective mass for holes with effective mass increasing far from the band edge as it relies on the curvature of the band. Effective mass can be graphed as a parabola remembering this is a basic picture as it makes some assumptions. For example it ignores anisotropy in the crystal and assumes all carriers are towards the bottom of the conduction band or top of the valence band.

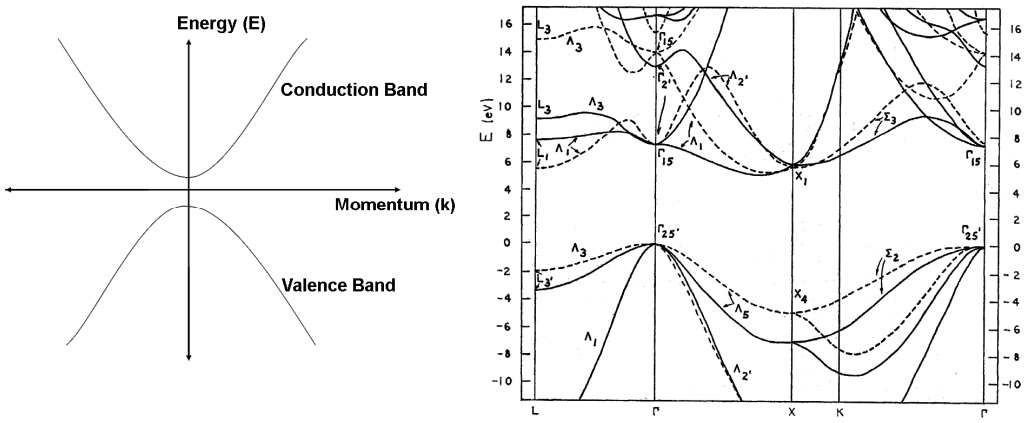


Figure 2.5.1: Energy bands from modelling effective mass (left) and in pure diamond (right) [2.49]

The two mechanisms through which a hole may travel through a semiconductor are labelled diffusion and drift. Diffusion arises from thermal energy which allows carriers to

travel in any direction, however they will tend to diffuse from densely populated regions to those of lower population density as thermodynamics dictates; this will produce a small diffusion current.

Drift involves charge carriers moving under the influence of an electric field such as that applied between the terminals of an electronic device. Holes will move in the same direction as the field (towards the negative terminal) whereas an electron would travel against it producing a total drift current. When this external electric field is applied each individual hole experiences a force (F) due to it. The hole will travel through the semiconductor until it comes under the influence of a scattering mechanism. The average distance the hole will travel before being scattered is known as its mean-free path (λ) and the average time between scattering events is the mean free time (τ_c). Scattering can be due to many factors which can be hard to discern from each other as they will be occurring all at once hence why a mean free time for all scattering events is used.

Some of the more important scattering mechanisms are defect scattering, surface scattering, ionised impurity scattering and phonon scattering from lattice vibrations (any lattice above absolute zero will vibrate to a certain extent just from thermal energy). Surface scattering will be particularly relevant for surface transfer doped diamond and especially so in an FET device where carriers are confined to a narrow channel close to the surface. Low frequency phonons are known as ‘acoustic phonons’ and high frequency are ‘optical phonons’. From this knowledge carrier effective mass may now be related to the velocity at which carriers may travel through that crystal (v) this is given by [2.50]:

$$v = \frac{q\tau_c E}{m^*} \qquad \textbf{2.5.2}$$

Where q is the elementary charge, E is now the electric field strength and τ_c the combined momentum relaxation time for all scattering processes. Again this velocity is positive due to holes travelling with the field. The ratio of the drift velocity to the electric field is known as the carrier mobility i.e. how velocity of carriers changes with electric field strength (under low electric fields).

$$\mu = \frac{q\tau_c}{m^*} \qquad \textbf{2.5.3}$$

It is worth noting that holes have lower mobility than electrons in general as they relate to carriers confined to the valence band hence subject to more obstruction from lattice vibration and attraction to atomic nuclei. This is also why hole effective masses tend to be higher. So when possible it is always desirable to use electrons as charge carriers in unipolar electronic devices.

Although mobility is a useful figure in general to describe the transport of charge, for devices driven at higher bias and hence high electric field, the velocity saturation mechanism for charge limits its usefulness in predicting device performance, which is more related to saturation velocity. In fact it is necessary for the field to be as high as is possible without impacting device reliability for high power applications. The above is satisfactory to describe the region of operation where velocity increases linearly with field (known as the linear region of operation in a transistor) however as field increases so does the amount of scattering. Optical phonons occur more often at high fields as carriers now contain enough energy to instigate lattice vibrations themselves. This begins to severely hamper charge transport as phonons travel with high momentum and reduce carrier velocity greatly meaning there is no longer a linear velocity increase with field and hence velocity becomes independent of mobility. Eventually this leads to impact ionisation where charge carriers can collide with impurities and other lattice atoms with enough energy to ionise carriers and cause breakdown although fortunately in diamond this does not occur until 10 $MV.cm^{-1}$ in theory.

Velocity saturation can be modelled as a result of the energy loss to the optical phonons. This is a complex interaction but can be shown if accounting for only optical phonon emission to be [2.51]:

$$v_s = \sqrt{\frac{8E_{op}}{3\pi m^*}\tanh\left(\frac{E_{op}}{2k_BT}\right)} \qquad \textbf{2.5.4}$$

Where E_{op} is the optical phonon energy, k_B the Boltzmann constant and T being absolute temperature. In diamond carrier velocity saturates at 2 x 10^7 and 0.8 x 10^7 $cm.s^{-1}$ for electrons and holes respectively. These are relatively high values due to a very high E_{op}

(163 meV) [2.51] arising from the strong bonding and low atomic mass of carbon also a low effective mass for carriers.

As charge carriers move temporarily into a region of different electric field (i.e. beneath a gate contact) then an effect known as velocity overshoot may also occur where the charge carrier's momentum relaxation rate is slower than its energy relaxation rate [2.52]. This effect allows for charge carriers to temporarily exceed the saturation velocity in the material. It is feasible that this phenomenon could occur in the short gate length devices presented in this work as carriers reaching the gate region will already have a substantial velocity [2.52].

2.6 Metal-Semiconductor Interfaces

In semiconductor devices, charge is also required to cross over interfaces between the semiconductor and metals in the form of an ohmic contact or leave the surface of the semiconductor completely and in to free space becoming ionised. It is also possible to accumulate or deplete regions of charge in the semiconductor with Schottky barrier contacts, giving us the ability to control the magnitude of current through devices leading to the field effect devices that have revolutionised electronics.

When charge carriers reach such interfaces, they encounter many differences to the bulk material such as non-periodicity, contamination and imperfections which lead to surface states different to the bulk lattice. As discussed in Section 2.3 hydrogen-termination of a diamond surface leaves the Fermi level unpinned, this means surface states are reduced to the point that allows the bands to bend so the semiconductor Fermi level will match the metal work function (assuming thermal equilibrium). This simplifies current transport across metal-semiconductor interfaces a great deal. If there is a substantial difference between metal work function φ_M and that of the semiconductor φ_S before contact is made a Schottky barrier (φ_B) is formed as electrons diffuse from the metal into the semiconductor setting up an electrostatic potential which prevents further flow similar to the potential ensuing from surface transfer doping as seen in Equation 2.6.1 where E_c is conduction band energy, q the elemental charge and χ the electron affinity [2.53]:

$$\varphi_B = \frac{E_G}{q} + \chi - \varphi_M \qquad \textbf{2.6.1}$$

The band bending experienced by a p-type semiconductor when metal and p-type semiconductor are brought in to intimate contact can be seen in Figure 2.6.1

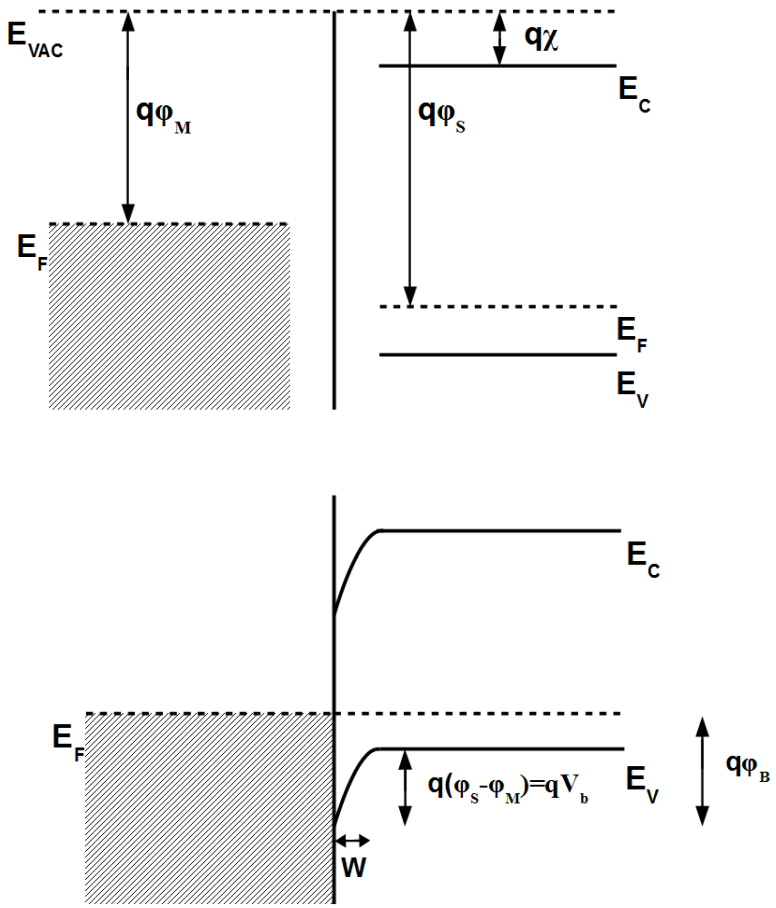


Figure 2.6.1: Metal-Semiconductor (p-type) energy band diagrams in isolation (above) and after contact and barrier formation (below)

This can be seen in terms of hole transport as holes drifting deeper in to the semiconductor material which leaves behind ionised acceptor atoms (a surplus of negative charge) and forms a depletion region (lack of majority carriers in this case holes) near the interface in the semiconductor. The built in potential (V_b) is then the amount of band bending instigated by contact shown in Equation 2.6.2 [2.53]:

$$V_b = \varphi_S - \varphi_M \qquad \textbf{2.6.2}$$

There is of course a small volume of electrons transferred from the metal to semiconductor during the diffusion and instigation of V_b, but compared to the density of charge carriers

present in a typical metal this is negligible in terms of the energy band diagram. The depletion width into the semiconductor is represented by W which is intrinsically related to the doping concentration in the semiconductor and the built in potential [2.53]:

$$W = \left(\frac{2\varepsilon_{SC}}{qN_d} V_b \right)^{\frac{1}{2}} \qquad \textbf{2.6.3}$$

Where ε_{SC} is the semiconductor permittivity and N_d the doping concentration. This contact is commonly known as a Schottky contact and is used in a FET to deplete/accumulate charge depending on the bias conditions. If a positive potential (V_{ap}) is applied to the metal with respect to the semiconductor (reverse bias) the bands are pulled further upwards and the barrier will increase as the depletion width is extended and holes are pushed further in to the semiconductor leaving more ionised acceptors as shown in Figure 2.6.2.

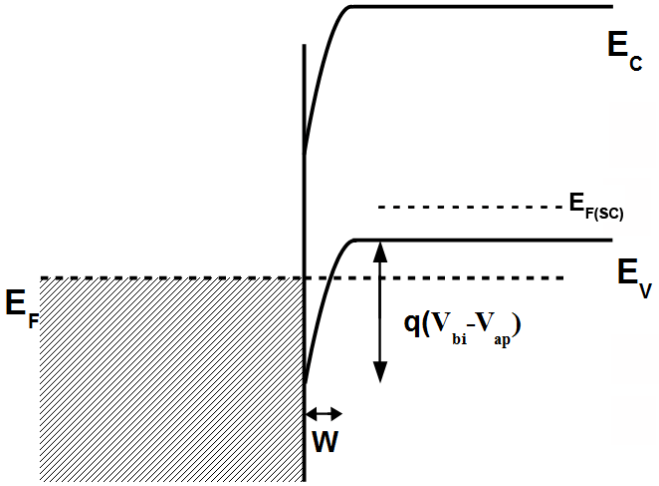


Figure 2.6.2: Metal-Semiconductor energy band diagram in reverse bias

If a negative V_{ap} is applied (forward bias) this pulls the bands down which acts to lower the barrier and accumulate holes towards the interface as shown in Figure 2.6.3. It is worth noting here this is a simplification of what is seen in the FETs discussed in this work as the situation is complicated somewhat by the interface arising from the adsorbed atmospheric layer.

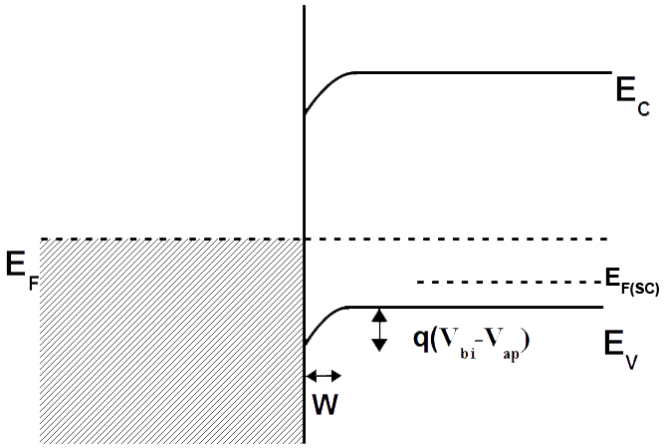


Figure 2.6.3: Metal-Semiconductor energy band diagram in forward bias (below)

If charge is to travel across the metal-semiconductor interface to give a net flow of holes moving from semiconductor to metal (or analogously electrons from metal to semiconductor) and hence current is to flow, the carriers need to overcome the Schottky barrier somehow. There are three methods of achieving this: thermionic emission, field emission and thermionic field emission and while these often occur somewhat in unison, they are more or less likely depending on the barrier heights and widths. These are shown in Figure 2.6.4.

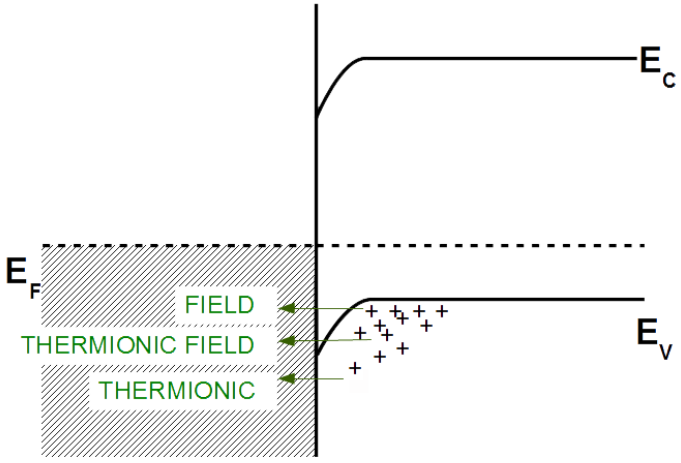


Figure 2.6.4: Methods of transport across a p-type Schottky barrier

Thermionic emission involves charge which has enough thermal energy to pass over the top of the Schottky barrier so $k_BT \geq q\varphi_B$. The thermionic emission current density across the barrier at any specific bias can be shown as an Arrhenius relationship [2.54]:

$$J_{TE} \propto \exp\left(-\frac{q\varphi_B}{k_BT}\right) \qquad \textbf{2.6.4}$$

Hence thermionic emission increases exponentially with temperature or with lower barrier height. Conversely field emission occurs if the Schottky barrier is thin enough so that quantum mechanical tunnelling of carriers through the barrier may take place. The thermal energy of carriers is not relevant in these circumstances and a tunnelling probability (E_{00}) is defined which is strongly depends on barrier width [2.54].

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_d}{m^*\varepsilon_S}} \qquad \textbf{2.6.5}$$

N_d being dopant density and ε_S semiconductor permittivity. The dependence on N means this phenomenon is found in more highly doped structures making this more likely to occur in a highly doped contact region. With the tunnelling current density being [2.54]:

$$J_{FE} \propto \exp\left(-\frac{q\varphi_B}{E_{00}}\right) \qquad \textbf{2.6.6}$$

Finally thermionic field emission is a combination of the two previous transport methods. It is found where a barrier is too high for thermionic emission and too wide for field emission yet carriers may on occasion obtain enough thermal energy to reach a point where they can tunnel through the barrier. The thermionic field emission current density can be shown to be [2.55]:

$$J_{TFE} \propto \exp\left(-\frac{q\varphi_B}{E_{00}\coth\left(\frac{E_{00}}{k_BT}\right)}\right) \qquad \textbf{2.6.7}$$

The total current density across the Schottky barrier takes the same form as a diode [2.54]:

$$J = J_0\left[\exp\left(\frac{qV}{\eta k_B T}\right) - 1\right] \qquad \textbf{2.6.8}$$

With η being the diode ideality factor and J_0 the saturation current density. So long as k_BT is >> E_{00} thermionic emission dominates but if $k_BT \sim E_{00}$ thermionic field emission needs to be accounted for and when $k_BT << E_{00}$ field emission becomes the dominant mode of transport across the barrier with the precise details of this mechanism becoming quite complex and beyond the scope of this thesis.

Ohmic Contacts take their name from Ohm's law and they are so named as the current response between semiconductor and metal is linear with applied voltage. This means strictly speaking they should not involve thermionic emission as it is a non-linear process. So in general ohmic contacts tend to be made on very highly doped regions of semiconductor where the Schottky barrier has become so thin as to allow for field emission to occur in both directions between metal and semiconductor. Hydrogen-terminated diamond however has low enough surface states to avoid Fermi level pinning so choosing a high work function metal will produce an ohmic contact [2.2].

2.7 MESFET Operation

MESFETs fabricated on surface transfer doped hydrogen-terminated diamond constitute the bulk of the work presented in this thesis. As seen in Figure 2.7.1 the design of a MESFET device utilising the hydrogen-terminated diamond surface is in principle conveniently simple. From the knowledge of carrier transport obtained in sections 2.5 and 2.6 as well as the surface transfer doping phenomenon described in section 2.3 it is now possible to build up a picture of how this device functions.

The MESFET has two ohmic contacts labelled source and drain between which a bias is applied to move charge from the source to the drain. There is a Schottky contact placed between these labelled the ‘gate’ which is used to modulate current transport within the FET.

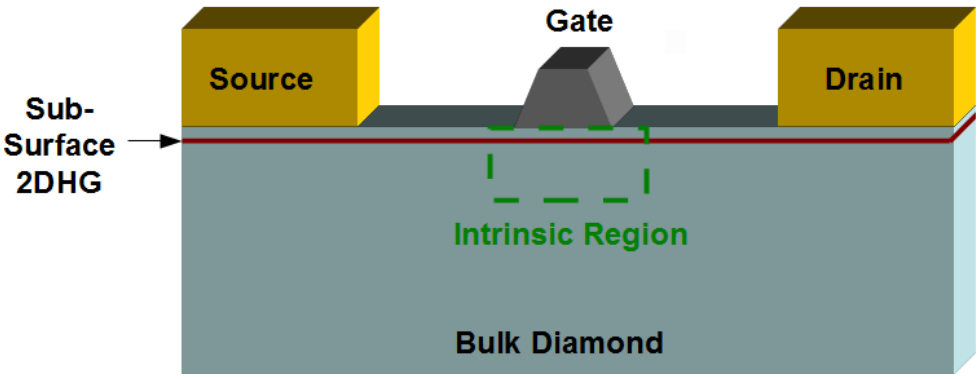


Figure 2.7.1: Layout of hydrogen-terminated diamond MESFET

There are several reasons for using a MESFET design, originating from both design specifications and material limitations. For example, diamond has no native oxide making traditional metal-oxide-semiconductor field effect transistors (MOSFETs) impossible. It is thus necessary to ensure current can be controlled within the device but without significant charge leaking through the gate metal contact. As touched upon when discussing metal-semiconductor interfaces, because hydrogen-terminated diamond falls below the Mott-Schottky limit with respect to interface state density, it is possible to tailor metals for purpose depending on their work function. Hence a gate contact may be achieved by using a low work function metal such as aluminium (4.26 eV) which will create a significant Schottky barrier and allow for current modulation without significant leakage current. Also, an ohmic contact may be achieved by choosing a high work function metal such as gold (5.1 eV) with contact resistance typically between 2-5 Ω.mm [2.2].

Current modulation between source and drain is achieved by applying a voltage between the gate and the source contacts. Upon gate contact deposition, the energy bands in the diamond are raised due to a built in potential between metal and semiconductor. This causes a depletion region the size of which for reduced gate lengths is somewhat dependent on the size of the contact. For the relatively small gate lengths seen in this work the contact does not tend to fully deplete the channel hence current will still flow at zero gate bias making these ‘depletion mode’ devices. Due to the p-type nature of the channel, a negative gate bias will cause the accumulation of charge at the surface and allowing for more current flow as the source contact is earthed and negative bias is applied to the drain

contact. A positive gate bias will deplete holes away from the interface and lead eventually to no current flow. The gate voltage at which drain current is reduced to a small enough value to define the device as 'off' is known as the pinch-off voltage (V_P) (or threshold voltage in traditional silicon CMOS devices). In effect the gate acts as one side of a parallel plate capacitor to accumulate or deplete charge on the other side (the semiconductor) to either increase or decrease the resistance of the channel region beneath it. Figure 2.7.2 shows how current in the FET channel responds to this modulation in an idealised case.

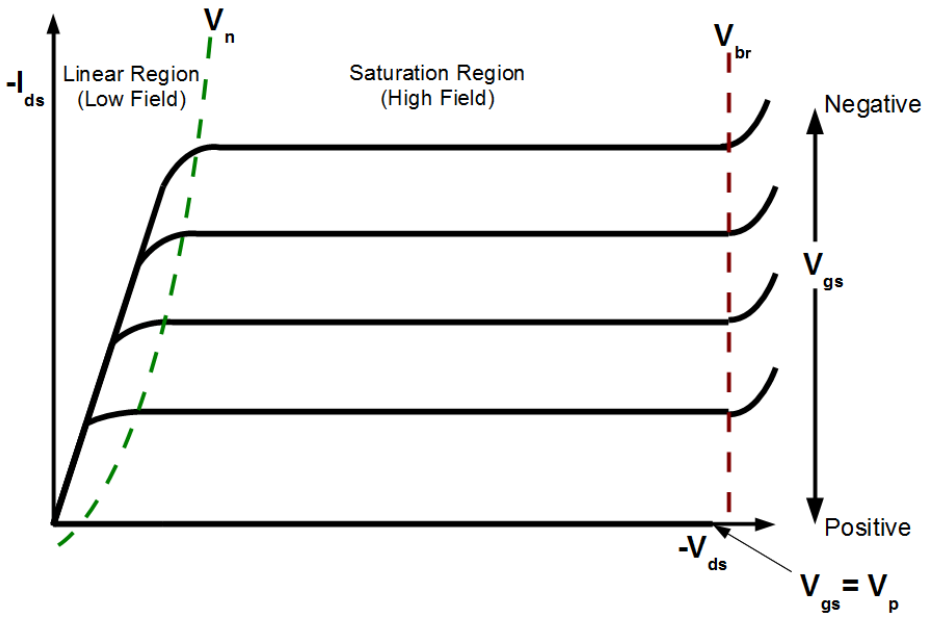


Figure 2.7.2: Ideal I_{ds}-V_{ds} characteristics for p-type MESFET

The linear region can be seen to the left where velocity of charge is still linearly increased with applied electric field. This continues until the knee voltage (V_n) is reached and the characteristics become saturated due to velocity saturation. Current then remains constant with respect to increased source-drain voltage until breakdown (V_{br}) is reached and the device becomes irreversibly damaged from impact ionisation or another method of breakdown. For example in surface channel MESFETs utilising atmospheric adsorbate molecules, their instability upon the surface may lead to premature breakdown before impact ionisation occurs within the intrinsic diamond.

There are several reasons why FET I_{ds}-V_{ds} data from real devices may differ from the ideal case presented in Figure 2.7.2. For example gate current leakage through the Schottky barrier will significantly distort the results around the origin i.e. significant current is still flowing even at V_{ds} = 0 but between the gate and channel. If this becomes a critical problem it may be worth considering the deposition of a dielectric material between metal and semiconductor to create a metal-insulator-semiconductor FET (MISFET). There is currently some debate as to the existence of an interfacial layer between the aluminium gate metal and semiconductor surface in surface transfer doped diamond FETs [2.56]. In addition it is unclear if the aqueous atmospheric layer remains during the deposition process and hence forms an interfacial layer with different properties to pure aluminium.

Another issue is the existence of higher electric field towards the drain side of the FET. This arises from a large potential difference between the gate and drain terminals and can lead to the possibility of buffer leakage through small amounts of residual boron in bulk diamond or at least the trapping of charge [2.57]. This can also cause premature breakdown at applied fields much lower than the intrinsic material breakdown field. Because of localised increases in electric field, carrier concentration becomes non-uniform and carriers can reach very large velocities in certain regions. It is worth noting in regards to breakdown that these surface transfer doped FETs depend intimately on the adsorbate layer which is far more likely to impact device operation before breakdown of the bulk diamond is reached.

When designing short gate length devices there will at some point be a limit at which the gate can no longer fully deplete the channel with an applied bias and hence pinch-off cannot be reached. This results in what is known as short channel effects. It is also true that the effective channel length (the region of influence the gate has over the semiconductor) is different to the physical length of metal deposited it can differ by potentially tens of nanometres giving a larger (or even smaller if the aluminium gate contact becomes oxidised) depletion region than expected.

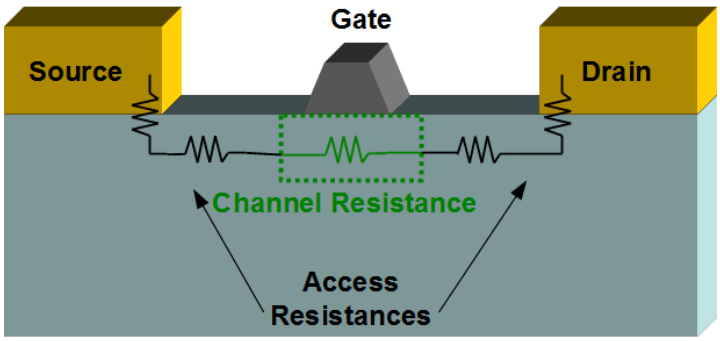


Figure 2.7.3: R_{ON} in MESFET

The slope in the linear region of the I_{ds}-V_{ds} characteristics may be used to extract on resistance (R_{ON}). This comprises a combination of resistances throughout the device as shown in Figure 2.7.3. The resistance of the channel directly beneath the gate in what is known as the intrinsic part of the device combined with the sum of contact and sheet resistance through the contact and semiconductor material respectively (collectively termed access resistance) present in what is described as the extrinsic region of the device make up R_{ON}. It is important when discussing the merits of device performance to distinguish between intrinsic and extrinsic device figures of merit.

2.8 DC Figures of Merit

After fabrication of FET devices is complete there needs to be a method of judging exactly how well they perform. This can be split in to two sections - the DC figures of merit and the RF figures of merit (to be presented in the following section).

An important metric of DC performance is the total drive current that can be passed through the device between source and drain terminals. The total current beneath the gate contact can be related to the two dimensional charge density present in the device channel (n), the charge velocity (v) and the device width (W_G):

$$I = W_g vnq \qquad \textbf{2.8.1}$$

As has been discussed, v varies with field up until saturation so the saturation current varies depending on the amount of charge and the device dimensions. With the ability to

accumulate and deplete charge it is important to know just how well the device is able to do this which can be defined via a quantity known as transconductance. Transconductance is defined as the rate of change of drain current (I_{ds}) with applied gate voltage (V_{gs}) at constant source drain voltage (V_{ds}). There are two measures of this: Intrinsic transconductance (g_m^*) involving the charge accumulation in the gate region just considering gate voltage between gate and channel and extrinsic transconductance (g_m) accounting for the applied gate voltage between source and gate contact which is subject to a voltage drop in the source access region.

$$g_m^* = \left(\frac{dI_{ds}}{dV_{gs}} \right)_{V_{ds}} \qquad \textbf{2.8.2}$$

Treating the gate contact and the channel as an idealised parallel plate capacitor i.e. no charge leaks across the barrier and permittivity does not change and assuming again a simplified two-dimensional model the intrinsic transconductance can be expressed as [2.58]:

$$g_m^* = \frac{\varepsilon W_g v}{h} \qquad \textbf{2.8.3}$$

Where h is the spacing between gate and channel charge and v is carrier velocity at the source end of the gate. Hence critical to achieving high transconductance is high velocity of carriers beneath the gate and low gate-channel separation. When considering the entire device, the total source access resistance becomes crucial as charge carriers will pass through this region introducing a drop in voltage before reaching the charge modulation region beneath the gate. Extrinsic transconductance (g_m) after accounting for this can then be shown to be [2.59]:

$$g_m = \frac{g_m^*}{1 + g_m^* R_S} \qquad \textbf{2.8.4}$$

High transconductance can be observed graphically as the differential of the I_{ds}-V_{gs} response as shown in Figure 2.8.1.

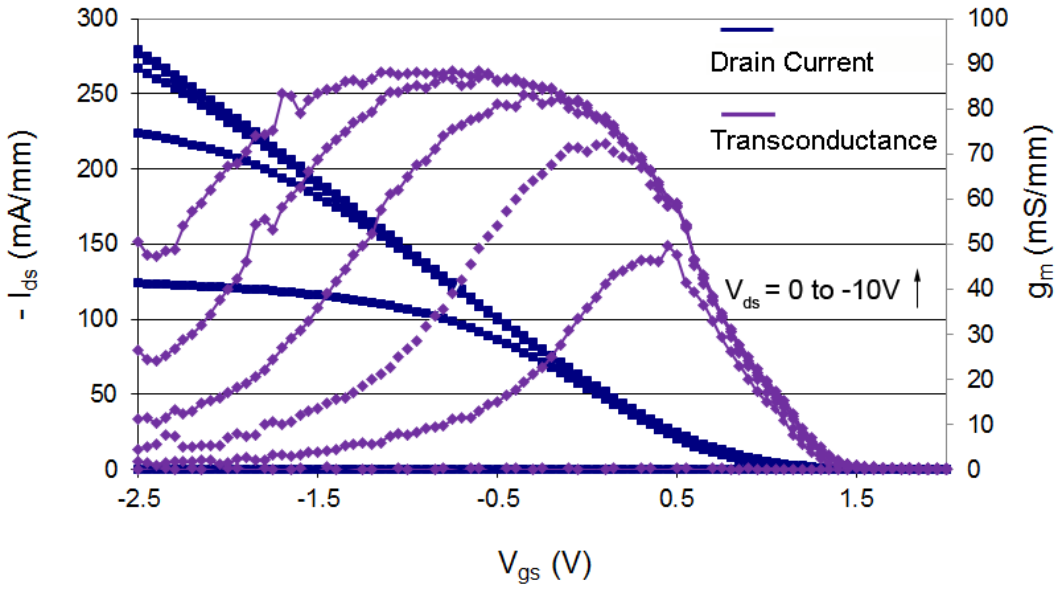


Figure 2.8.1: Changing transconductance as seen on an I_{ds}-V_{gs} plot for 250 nm FET

Continued increase in drain current even after saturation due to effects such as buffer leakage are seen graphically as a sloped rather than horizontal saturation current as seen in Figure 2.8.2. This slope still relates to the resistance of the device but is now dominated by the resistance in the channel or alternatively its reciprocal termed the output conductance (g_{ds}) which is the rate of change of the drain current with respect to drain voltage at a constant gate voltage within the 'saturation' region:

$$g_{ds} = \left(\frac{dI_{ds}}{dV_{ds}} \right)_{V_{gs}} \qquad \textbf{2.8.5}$$

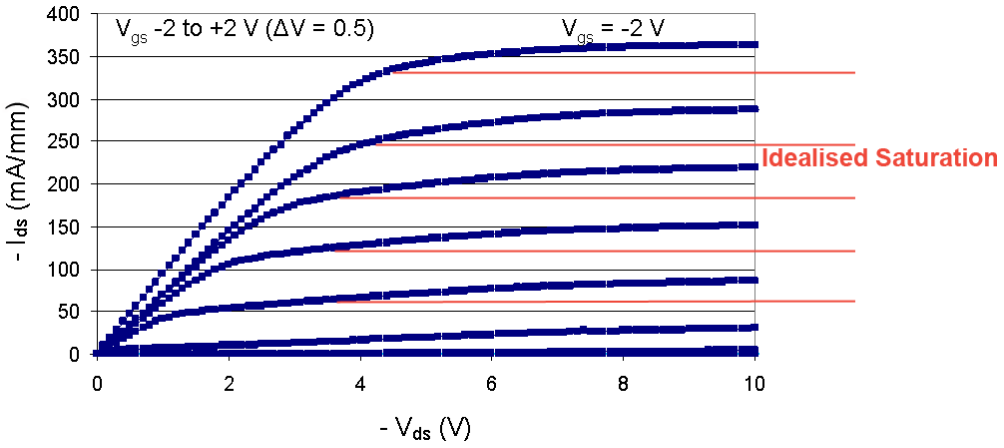


Figure 2.8.2: Output conductance seen graphically

2.9 RF Figures of Merit and the Small Signal Equivalent Circuit

It is possible to better understand FET operation by modelling each parameter of the devices as individual lumped circuit elements which combined provide an equivalent circuit of FET behaviour for small signals at RF frequencies.

At low frequency, DC characterisation techniques may provide a realistic view of FET operation. However modelling the equivalent circuit tells us more about the extrinsic device parts and how performance alters particularly at higher frequencies. It is then possible to determine exactly how each element contributes to overall performance and scale the device parameters suitably to improve FET figures of merit. An example of the RF equivalent circuit for a diamond MESFET is presented in Figure 2.9.1 with the individual elements described in Table 2.9.1 [2.58]:

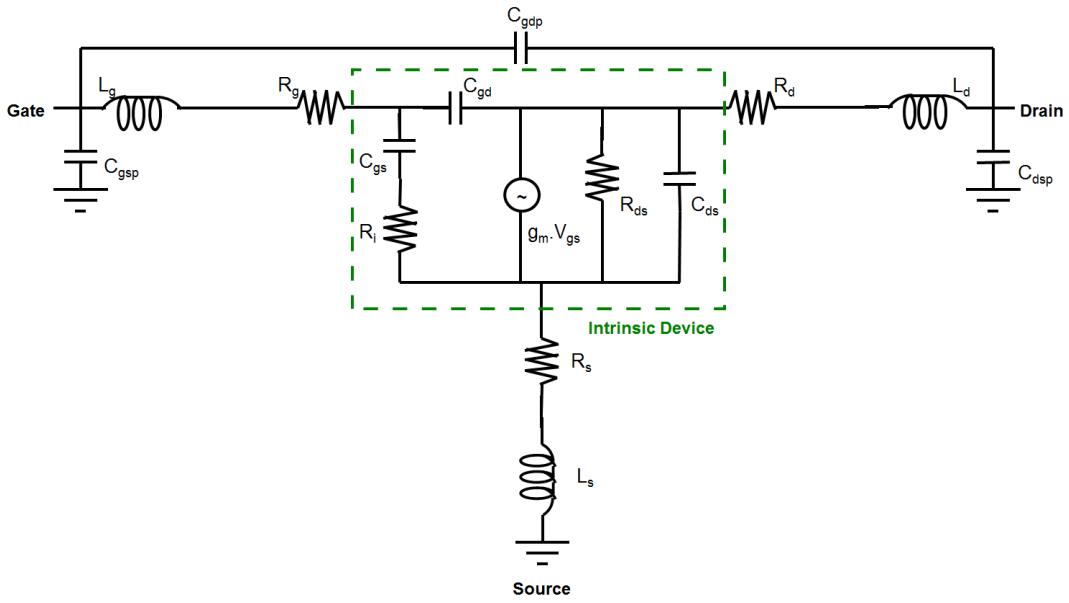


Figure 2.9.1: Extrinsic diamond MESFET equivalent circuit with intrinsic region highlighted

Circuit Element	Description
Current Source ($g_m^*.V_{gs}$)	Model for the source-drain current modulation (intrinsic transconductance) controlled by voltage across gate capacitor.
Source-Drain Resistance (R_{ds})	The source-drain resistance of the intrinsic device
Intrinsic Channel Resistance (R_i)	Finite channel resistance through the distributed capacitance of C_{gs}
Gate-Source Capacitance (C_{gs})	Gate capacitive coupling to channel distributed to the source side of the gate
Gate-Drain Capacitance (C_{gd})	Gate capacitive coupling to channel distributed to the drain side of the gate
Drain-Source Capacitance (C_{ds})	Capacitance along channel due to varying charge carrier density
Gate Resistance (R_g)	Resistance associated with gate contact
Gate Inductance (L_g)	Inductance associated with gate contact
Source Resistance (R_s)	Resistance associated with source contact
Source Inductance (L_s)	Inductance associated with source contact
Drain Resistance (R_d)	Resistance associated with drain contact
Drain Inductance (L_d)	Inductance associated with drain contact
Gate-Source Pad Capacitance (C_{gsp})	Capacitance between gate and source contacts
Gate-Drain Pad Capacitance (C_{gdp})	Capacitance between gate and drain contacts
Drain-Source Pad Capacitance (C_{dsp})	Capacitance between drain and source contacts

Table 2.9.1: Description of equivalent circuit elements

To maximise FET performance it is essential for extrinsic and external elements that act to impede charge flow to be as low as possible. For example to minimise extrinsic resistances thick layers of metal are normally deposited. However there is a trade-off between lowering the resistance and raising other important parasitics such as capacitance which will allow signal to travel between the gate and other parts of the device outside the gate region. In terms of the gate, multiple gate fingers can be used to reduce the total R_g (additional gate fingers will act as resistors in parallel, meaning the total R_g is the sum of the reciprocal of each finger's resistance). This will also increase the width of the channel to increase maximum drive current. To further reduce R_g a T-shaped gate may be employed to increase cross sectional area (reducing resistance) without increasing the gate length as seen in Figure 2.9.2. It should also be noted that RF gate resistance as seen in the equivalent circuit is roughly one third of the value for DC characterisation [2.60].

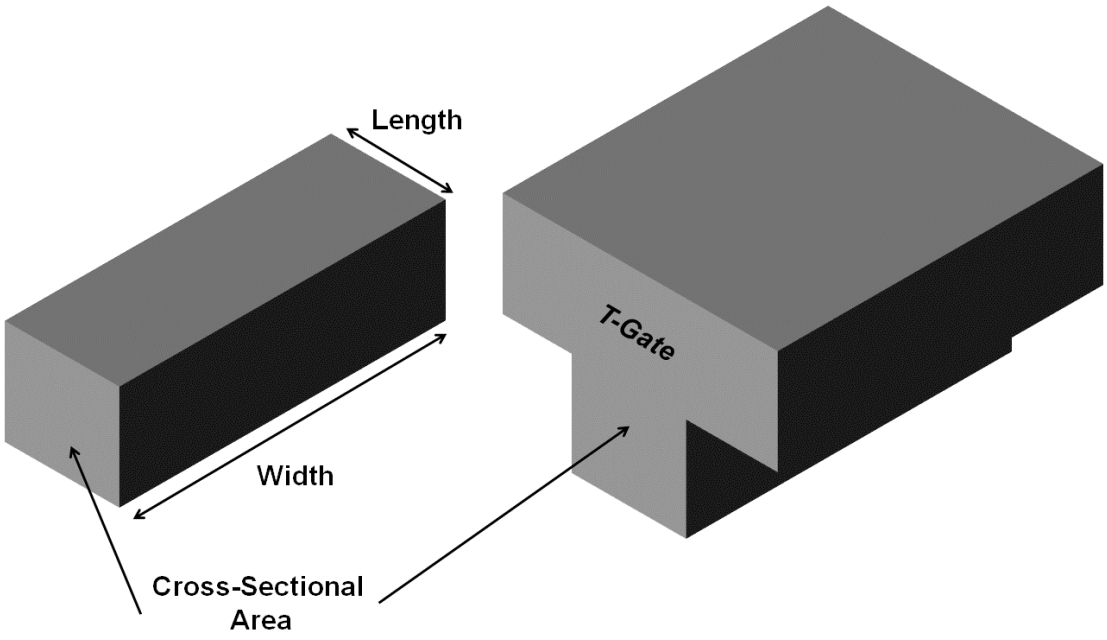


Figure 2.9.2: Increase in cross-sectional gate area benefitting from a T-shaped gate structure

For RF operation it is desirable for an FET to exhibit gain in terms of both current and power. The gain a device provides tends to decrease with frequency until a point where no more is given by the device. The frequency at which current gain reaches unity (ie: where $I_{in} = I_{out}$) is known as the 'Cut-Off Frequency (f_T)' the maximum frequency at which the

device exhibits current gain. The difference between intrinsic and extrinsic performance has been touched upon already and again for RF measurement access resistances along with other parasitic elements will be detrimental to performance. In the case of f_T particularly, access resistances can play a large role, so intrinsic and extrinsic f_T can vary substantially. For the case of intrinsic f_T the magnitude of the current signal input to the device (I_{in}) will be:

$$\left|I_{in}\right| = V_{C_g} 2\pi f\left(C_g\right) \qquad \textbf{2.9.1}$$

Where C_g is the total gate capacitance (i.e. $C_{gs} + C_{gd}$). The current signal flowing out of the device (I_{out}) becomes:

$$I_{out} = g_m^* V_{C_g} \qquad \textbf{2.9.2}$$

Hence when $I_{in} = I_{out}$ intrinsic f_T is given by:

$$f_T^{\text{int}} = \frac{g_m^*}{2\pi.C_g} = \frac{v}{2\pi.L_g} \qquad \textbf{2.9.3}$$

It may be also written in terms of the average velocity of carriers under the gate and gate length (L_g) as shown. Hence intrinsic transconductance, gate length and total gate capacitance are crucial to f_T and as L_g is the easiest to scale during fabrication it is easy to see why FET gate length is so aggressively scaled. When accounting for how parasitic elements can affect this frequency performance the result may be seen below for the extrinsic f_T [2.59]:

$$f_T^{ext} = \frac{\frac{g_m}{2\pi}}{\left[C_{gs} + C_{gd}\right]\left[1 + \frac{\left(R_s + R_d\right)}{R_{ds}}\right] + C_{gd}.g_m.\left(R_s + R_d\right)} \qquad \textbf{2.9.4}$$

This is the value as measured for the entire device. It is clear that if ($R_s + R_d$) is large and R_{ds} is small then the extrinsic f_T will be much reduced from the intrinsic value. It is likely

that as gate dimension is reduced, R_{ds} will also be reduced as the output conductance increases due to potential short channel effects.

The second important figure of merit for RF performance detailed here is f_{MAX} which is defined as the point where there is unity power gain ($P_{in} = P_{out}$). Access resistances will still have a negative influence over f_{MAX} including the gate resistance, R_g. The equation below describes the intrinsic expression for f_{MAX} [2.60]:

$$f_{\max}^{\text{int}} = \frac{f_T^{\text{int}}}{2}\left(\frac{R_{ds}}{R_g + R_i}\right)^{1/2} \qquad \textbf{2.9.5}$$

As (R_g + R_i) becomes larger and R_{ds} smaller then the smaller f_{MAX} will become. As discussed previously a common method used to lower R_g and increase f_{MAX} is employing a T-shaped gate feature (Figure 2.9.2). This maximises the cross-sectional area of the gate and hence lowers its cross-sectional resistance. When extrinsic components are accounted for f_{MAX} can be shown to be [2.61]:

$$f_{\max}^{ext} = \frac{f_T^{\text{int}}}{2.\left(\frac{R_g + R_i + R_s}{R_{ds}} + 2\pi . f_T^{\text{int}} . R_g . C_{gd}\right)^{1/2}} \qquad \textbf{2.9.6}$$

Again while other extrinsic factors play a role as with f_T, R_g is perhaps the most important component affecting the extrinsic f_{MAX} figure. Also this equation is only valid for certain approximations. – Namely $R_s g_{ds} << 1$, $C_{gd} << C_{gs}$ and $R_s g_m^* << 1$ [2.58].

So scaling FET devices is very much a trade-off between achieving the smallest possible dimensions fabrication processes will allow and ensuring extrinsic components do not dominate the DC and RF performance. There are other RF figures applicable to high power measurement and although this is the ultimate goal with diamond these cannot be considered seriously until areas such as repeatability and stability of FETs have been addressed.

2.10 Summary

This chapter has provided a brief background on synthetic diamond and why it is an attractive material for high performance electronics. The challenges in doping have been

summarised with a promising solution known as surface transfer doping discussed. Having addressed the theoretical and basic principles of diamond FET operation in Chapter 2, the physical fabrication processes used to produce these devices are presented in Chapter 3.

References

[2.1] F. Maier, M. Riedel, B. Mantel, J. Ristein, and L. Ley, "Origin of surface conductivity in diamond," *Physical Review Letters*, vol. 85, no. 16, pp. 3472-3475, 2000

[2.2] H. Kawarada, M. Aoki and M. Ito, "Enhancement mode metal-semiconductor field effect transistors using homoepitaxial diamonds," *Applied Physics Letters*, vol. 65, no. 12, pp. 1563-1565, 1994

[2.3] P. Strobel, M. Riedel, J. Ristein and L. Ley, "Surface transfer doping of diamond," *Nature*, vol. 430, no. 6998, pp. 439-441, 2004

[2.4] J. Clayden, N. Greeves, S. Warren and P. Wothers, Organic Chemistry, Oxford University Publishing, pp. 105-110, 2001

[2.5] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd Edition, John Wiley & Sons Inc, p. 789, 2007

[2.6] C. R. Zeisse, C. A. Hewett, R. Nguyen, J. R. Zeidler and R. G. Wilson, "An ion-implanted diamond metal-insulator-semiconductor field-effect transistor," *IEEE Electron Device Letters*, vol. 12, no. 11, pp. 602-604, 1991

[2.7] H. T. Hall, "Ultrahigh-pressure research: At ultrahigh pressures new and sometimes unexpected chemical and physical events occur," *Science*, Vol. 128, no. 3322, pp. 445-449, 1958

[2.8] O. A. Shenderova and D. M. Gruen, Ultananocrystalline diamond: Syntheses, properties and applications, 2nd Edition, William Andrew p. 135, 2012

[2.9] F.X. Lu, W.Z. Tang, T.B. Huang, J.M. Liu, J.H. Song, W.X. Yu and Y.M. Tong, "Large area high quality diamond film deposition by high power DC arc plasma jet operating at gas recycling mode," *Diamond and Related Materials*, vol. 10, no. 9-10 pp. 1551-1558, 2001

[2.10] R. Haubner and B. Lux, "Diamond growth by hot-filament chemical vapor deposition: State of the art," *Diamond and Related Materials*, vol. 2, no. 9, pp. 1277-1294, 1993

[2.11] C-S. Yan, Y. K. Vohra, H-K. Mao, and R. J. Hemley, “Very high growth rate chemical vapor deposition of single-crystal diamond,” *Proceedings of the National Academy of Sciences*, vol. 99, no. 20, pp. 12523-12525, 2002

[2.12] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, p. 790, 2007

[2.13] C. J. H. Wort and R. S. Balmer, “Diamond as an electronic material,” *Materials Today*, vol. 11, no. 1-2, pp. 22-28, 2008

[2.14] A. Akturk, N. Goldsman, S. Potbhare, A. Lelis, “High field density-functional-theory based Monte Carlo 4H:SiC impact ionization and velocity saturation,” *Journal of Applied Physics*, vol. 105, no. 3, pp. 033703-1-033703-7, 2009

[2.15] J. B. Casady and R.W. Johnson, “Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review,” *Solid State Electronics.*, vol. 39, no. 10, pp. 1409–1422, 1996

[2.16] C. Bayram, J. L. Pau, R. McClintock, and M. Razeghi, “Delta-doping optimization for high quality *p*-type GaN,” *Journal of Applied Physics*, vol. 104, no. 8, pp 083512-1-083512-5, 2008

[2.17] S. Bhagavantam, “Dielectric constant of diamond,” *Nature*, vol. 161, no. 4097, p. 729, 1948

[2.18] H. Morkoç, Handbook of Nitride Semiconductors and Devices. Vol. 1, John Wiley & Sons Inc, p. 21, 2008

[2.19] A. Johnson, “Physical limitations on frequency and power parameters of transistors,” *RCA Review*, vol. 26, pp. 163-177, 1965

[2.20] R. W. Keyes, "Figure of merit for semiconductors for high speed switches," *Proceedings of the IEEE*, vol. 60, no. 2, pp. 225-232, 1972

[2.21] B. J. Baliga, “Power semiconductor device figure of merit for high-frequency applications,” *Electron Device Letters*, vol. 10, no. 10, pp. 455-457, 1989

[2.22] A. Aleksov , M. Kubovic, N. Kaeb, U. Spitzberga A. Bergmaier, G. Dollinger, T. Bauer, M. Schreck, B. Stritzker and E. Kohn, “Diamond field effect transistors-concepts and challenges,” *Diamond and Related Materials*, vol. 12, no. 3-7, pp. 391-398, 2003

[2.23] C. Saguy, E. Baskin and R. Kalish, “Electrical properties of undoped and ion-implanted type IIa diamonds measured by photo-Hall,” *Diamond and Related Materials*, vol. 14, no. 3-7, pp. 344-349, 2005

[2.24] E. Gaillou, J. E. Post, D. Rost and J. E. Butler, "Boron in natural type IIb blue diamonds: Chemical and spectroscopic measurements," *American Mineralogist*, vol. 97, pp. 1-18, 2012

[2.25] B. Massarani and J. C. Bourgoin, "Hopping conduction in semiconducting diamond," *Physical Review B*, vol. 17, no. 4, pp. 1758-1769, 1978

[2.26] J. P. Goss, P. R. Briddon, R. Jones and S. Sque, "Donor and acceptor states in diamond," *Diamond and Related Materials*, vol. 13, no. 4-8, pp. 684-690, 2004

[2.27] E. B. Lombardi and A. Mainwood, "A first principles study of lithium, sodium and aluminium in diamond," *Diamond and Related Materials*, vol. 17, no. 7-10, pp. 1349-1352, 2008

[2.28] D. Segev and S. H. Wei, "Design of shallow donor levels in diamond by isovalent-donor coupling," *Physical Review Letters*, vol. 91, no. 12, pp. 126406-1-126406-3, 2003

[2.29] T. Miyazaki and S. Yamasaki, "Efficiency of multiple atom doping in wide band gap semiconductors," *Applied Physics Letters*, vol. 86, no. 26, pp. 261910-1-261910-1, 2005

[2.30] Z. Teukam, J. Chevallier, C. Saguy, R. Kalish, D. Ballutaud, M. Barbé, F. Jomard, A. Tromson-Carli, C. Cytermann, J. E. Butler, M. Bernard, C. Baron and A. Deneuville, "Shallow donors with high n-type electrical conductivity in homoepitaxial deuterated boron-doped diamond layers," *Nature Materials*, vol. 2, no. 7, pp. 482-386, 2003

[2.31] R. S. Balmer, I. Friel, S. Hepplestone, J. Isberg, M. J. Uren, M. L. Markham, N. L. Palmer, J. Pilkington, P. Huggett, S. Majdi and R. Lang, "Transport behaviour of holes in boron delta-doped diamond structures," *Journal of Applied Physics*, vol. 113, no. 3, pp. 033702-01-033702-10, 2013

[2.32] P. W. May, J. C. Stone, M. N. R. Ashfold, K. R. Hallam, W. N. Wang and N. A. Fox, "The effect of diamond surface termination species upon filed emission properties," *Diamond and Related Materials*, vol. 7, no. 2-5, pp. 671-676, 1998

[2.33] J. Ristein, "Diamond surfaces: familiar and amazing," *Applied Physics A*, vol. 82, no. 3, pp. 377-384, 2006

[2.34] J. A. Garrido, C. E. Nebel and M. Stutzmann, "Capacitance-voltage studies of Al-Schottky contacts on hydrogen-terminated diamond," *Applied Physics Letters*, Vol. 81, no. 4, pp.637-639, 2002

[2.35] S. A. O. Russell, S. Sharabi, A. Tallaire and D. A. J. Moran, "Hydrogen-Terminated Diamond Field Effect Transistors with Cut-Off Frequency of 53 GHz", *IEEE Electron Device Letters* vol. 33, no. 10, pp. 1471-1473, 2012.

[2.36] M. I. Landstrass and K. V. Ravi, "Hydrogen passivation of electrically active defects in diamond," *Applied Physics Letters*, vol. 55, no. 14, pp. 1391-1393, 1989

[2.37] J. S. Foord, C. H. Lau, M. Hiramatsu, R. B. Jackman, C. E. Nebel and P. Bergonzo, "Influence of the environment on the surface conductivity of chemical vapour deposition diamond," *Diamond and Related Materials*, vol. 11, no. 3-6, pp. 856-860, 2002

[2.38] K. Hayashi, S. Yamanaka, H. Watanabe, T. Sekiguchi, H. Okushi and K. Kajimura, "Investigation of the effect of hydrogen on electrical and optical properties in chemical vapour deposition on homoepitaxial diamond films," *Journal of Applied Physics*, vo. 81, no. 2, pp. 744-753, 1997

[2.39] H. J. Looi, R. B. Jackman and J. S. Foord, "High carrier mobility in polycrystalline thin film diamond," *Applied Physics Letters*, vol. 72, no. 3, pp. 353-355, 1998

[2.40] B. Rezek, H. Watanabe, D. Shin, T. Yamamoto and C. E. Nebel, "Ion-sensitive field effect transistor on hydrogenated diamond," *Diamond and Related Materials*, vol. 15, no. 4-8, pp. 673-677, 2006

[2.41] K. Hirama, K. Tsuge, S. Sato, T. Tsuno, Y. Jingu, S. Yamauchi, and H. Kawarada, "High-performance p-channel diamond metal–oxide–semiconductor field-effect transistors on H-terminated (111) surface," *Applied Physics Express*, vol. 3, no. 4, pp. 044001-1-044001-3, 2010

[2.42] G. Dennler, M. C. Scharber and C. J. Brabec, "Polymer-fullerene bulk heterojunction solar cells," *Advanced Materials*, vol. 21, no. 13, pp. 1323-1338, 2010

[2.43] L. Ley, J. Ristein, F. Meier, M. Riedel and P. Strobel, "Surface conductivity of the diamond: A novel transfer doping mechanism," *Physica B*, vol. 376-377, pp. 262-267, 2006

[2.44] W. Chen, D. Qi, X. Gao and A. T. S. Wee, "Surface transfer doping of semiconductors," *Progress in Surface Science*, vol. 84, no. 9-10, pp. 279-321, 2009

[2.45] P. Strobel, J. Ristein, L. Ley, K. Seppelt, I. V. Goldt and O. Boltalina, "Surface conductivity induced by fullerenes on diamond: Passivation and thermal stability," *Diamond and Related Materials*, vol. 15, no. 4-8, pp. 720-724, 2005

[2.46] D. Kueck, P. Leber, A. Schmidt, G. Speranza and E. Kohn, "AlN as passivation for surface channel FETs on diamond," *Diamond and Related Materials*, vol. 19, no. 7-9, pp. 932-935, 2010

[2.47] K. Hirama, H. Sato, Y. Harada, H. Yamamoto and M. Kasu, "Thermally stable operation of H-terminated diamond FETs by NO_2 adsorption and Al_2O_3 Passivation," *IEEE Electron Device Letters*, vol. 33, no. 8, pp. 1111-1113, 2012

[2.48] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, pp. 12-14, 2007

[2.49] L. R. Saravia and D. Brust, "Band structure and interband optical absorption in diamond," *Physical Review*, vol. 170, no. 3, pp. 683-686, 1968

[2.50] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, p. 28, 2007

[2.51] R. S. Sussmann, CVD Diamond for electronic devices and sensors, John Wiley & Sons Inc, p. 40 2009

[2.52] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, p. 37, 2007

[2.53] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, pp. 136-137, 2007

[2.54] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, pp. 153-165, 2007

[2.55] S. Tiwari, Compound Semiconductor Device Physics, Academic Press, pp. 214-219, 1992

[2.56] M. Kasu, K. Ueda, H. Kageshima and Y. Yamauchi, "Gate interfacial layer in hydrogen-terminated diamond field-effect transistors," *Diamond and Related Materials*, vol. 17, no. 4-5, pp. 741-744, 2008

[2.57] M. Kasu, M. Kubovic, A. Aleksov, N. Teofilov, Y. Taniyasu, R. Sauer, E. Kohn, T. Makimoto and N. Kobayashi, "Influence of epitaxy on the surface conduction of diamond film," *Diamond and Related Materials*, vol. 13, no. 2, pp. 226-232, 2004

[2.58] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, p. 309, 2007

[2.59] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, pp. 347-348, 2007

[2.60] B. Razavi, R-H. Yan and K. F. Lee, "Impact of distributed gate resistance on the performance of MOS devices," *IEEE Transactions on Circuits and Systems – I: Fundamental Theory and Applications*, vol. 41, no. 11, pp. 750-754, 1994

[2.61] P. Wolf, "Microwave properties of schottky-barrier field effect transistors," *IBM Journal of Research and Development*, vol. 14, no. 2, pp. 125-141, 1970

3. Fabrication

The scaling of electronic devices to nanometre dimensions naturally leads to the need for ever more advanced fabrication techniques and this becomes even more apparent when working with a material as challenging to process as diamond. This chapter details some standard tools and procedures and how they may be adapted for diamond FET fabrication, allowing for the production of the devices characterised in later chapters of this thesis.

First there is a brief look at sample preparation and hydrogen-termination procedures, then electron beam lithography is investigated as an alternative to optical UV lithography for reasons such as minimum feature size amongst others. Techniques to metallise samples are discussed and how these can be adapted to create the best quality contacts to the surface transfer doped diamond material. Intimately linked to this is the sensitivity of the hydrogen-terminated diamond surface and how this needs to be accounted for in the form of metal sacrificial layers (which will also need specialised etching techniques to be selectively removed) amongst other processing considerations. Then after all the tools necessary to produce a diamond MESFET are presented the ‘standard’ process flow for these devices is reviewed and the best way to effectively scale gate geometry is discussed. Finally there is a brief discussion of some alternative fabrication techniques that were investigated over the course of this research and their relative merits.

3.1 Hydrogen-Termination and Sample Preparation

As with all nanoscale fabrication a clean uncontaminated surface is essential and this is particularly true for this research with its strong dependence on the quality of the diamond surface. Ideally the hydrogen-terminated diamond surface would be atomically smooth so as to minimise trapped charge and scattering in the surface channel FETs [3.1]. It has been shown that one of the best possible ways to produce a smooth clean diamond surface with little in the way of contamination from non-diamond carbon is to expose the diamond to hydrogen plasma at the end of growth [3.2]. This is beneficial for this research for another reason in that the samples are required to be hydrogen-terminated for surface transfer doping to occur. While it is also true that strongly acidic solutions such as aqua regia or combinations of sulphuric and nitric acids will remove graphitic contaminants these cleans will also oxidise the diamond surface leaving the need for a subsequent hydrogen-termination process anyway [3.1].

Hydrogen-termination was typically performed by collaborators at Université Paris 13 before arrival at Glasgow which involved a high power hydrogen plasma performed at a temperature of 580° C for 30 minutes. Upon arrival at Glasgow the samples should be relatively clean of non-diamond carbons but a simple de-grease was performed to remove any mild organic contamination from transit. This involved a 2 hour soak in acetone in a 50° C water bath followed by isopropyl alcohol (IPA) rinse and blow dry with pure nitrogen (N_2). These have no known detrimental effect on the hydrogen-termination however it is good practice to leave the diamond sample for 24 hours before commencing further fabrication to allow for atmospheric adsorbate molecules to fully maximise the surface transfer doping effect [3.3].

3.2 Electron Beam Lithography

Lithography is perhaps the most crucial tool involved in this research and semiconductor device fabrication in general. It allows for the definition of patterns of any shape down to the nanometre scale and encompasses optical lithography which is the most commonly used lithography method in the semiconductor industry through to electron beam (e-beam) lithography and even lithography via imprint techniques. Both optical and e-beam techniques derive from the same principle, the modification of a thin radiation sensitive coating known as resist and selective removal of this after exposure.

All fabrication carried out in this research used e-beam rather than optical lithography as the FETs fabricated all contain nanometre sized gate features and while modern optical lithography techniques are capable of these dimensions [3.4], ever changing patterns from sample to sample would be an uneconomical usage of lithography masks. E-beam lithography may be slower and costlier but it is better adapted for research due to the versatility with changing devices (e-beam patterns can be altered electronically as they are electronically stored and the pattern is directly written with no need for a mask).The e-beam lithography process is shown in Figure 3.2.1 and described below.

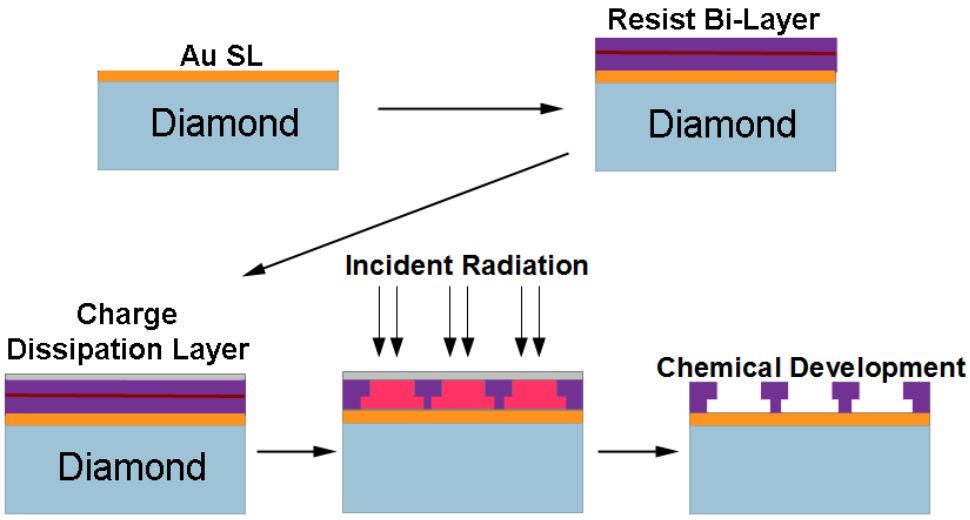


Figure 3.2.1: Lithography procedure involving a positive resist

First the clean diamond sample is coated with a thin sacrificial layer (SL) of Au which is a special requirement of the hydrogen-terminated diamond to protect it from subsequent processing. Au is used as it can be etched with an acid which does not cause any detriment to the atmospheric induced sub-surface conductivity [3.3]. The substrate is then coated in a polymer (dissolved into the solvent oxylene) resist using a spin-coating technique. This is performed at high RPM (typically around 5k) to give total uniform sample coverage apart from narrow edge beading towards the edge of the sample. Adapting the RPM as well as the ratio of polymer to solvent can very accurately control the thickness of resist coating down to nanometre scales. Once coated the sample is baked with all bakes undertaken during this research at a relatively low 120° C to attempt to minimise any potential damage

to the surface adsorbate layer from baking while still suitable to evaporate the solvent and leave just the desired polymer coating. All fabrication in this project involved the use of the positive e-beam resist poly(methyl methacrylate) (PMMA) in different concentrations. Being a positive resist, when exposed to a significant dose of electrons the exposed area will de-polymerise and become easier to dissolve in a suitable chemical developer. To aid metal lift-off a bi-layer of resist is spun on to the sample with different molecular weights, this will be discussed in detail later.

The inverse process is possible using a negative resist such as hydrogen silsesquioxane (HSQ) where during exposure more cross-linking of the polymer chains will occur making it denser and less easily dissolved in developer. Negative resist tends to be used for etching small features from a substrate i.e. 'subtractive' processes and is not utilised in this work. Instead positive resist is used to define small scale features for metal deposition on to the substrate, an 'additive' process.

The final step before submission to the e-beam lithography tool is the deposition of a thin charge dissipation layer (CDL). This is necessary as the insulating diamond substrate will quickly become charged under e-beam exposure becoming a problem when the charge build up begins to deflect the incident electron beam and hence distorts the pattern being written. The CDL needs to be thick enough to provide electrons with a fast path to ground but not too thick so as to impede electrons penetrating it and expose the resist. In this work 15 nm of Al is used as it is relatively cheap and can be easily removed using MF-CD26 developer with no detriment to the resist below [3.5].

The James Watt Nano-fabrication Centre (JWNC) at the University of Glasgow is equipped with a Vistec Vector Beam 6 Ultra-High Resolution Extremely-Wide Field (VB6 UHR EWF) lithography tool capable of ~ 3 nm beam size, 50 MHz writing speed and 1.3 mm field at 100 kV acceleration voltage along with the capability for lower 50 kV acceleration. The VB6 is displayed in a diagrammatic representation in Figure 3.2.2. It contains a thermionic field emission tungsten tip with a zirconium oxide (ZrO) bead which can emit a beam of electrons in a similar manner described in section 2.7. This beam is then focused and aligned by a series of coils and magnetic lenses along the column and then either blanked or deflected as required by the pattern. The Faraday cup is placed on the stage to monitor the beam current and the sample may be loaded under vacuum via the

load-lock with the stage also capable of movement under the beam to produce the desired pattern.

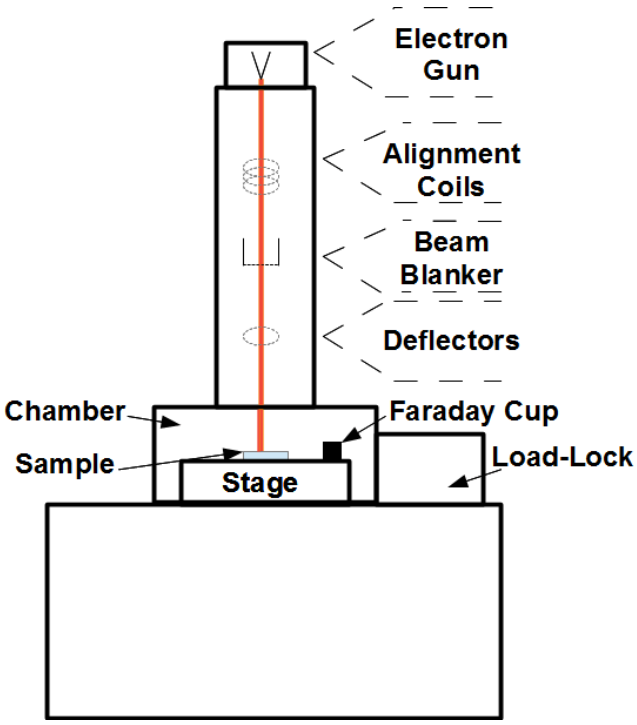


Figure 3.2.2: Simplified schematic of VB6 e-beam lithography tool

To create the pattern a computer aided design (CAD) package may be used for multi-layer GDSII file creation, although as the VB6 has a maximum field of 1.3 mm this needs to be fractured via a computer aided transcription system (CATS) in to sub-fields and written as CFLT files. The pattern is fractured as standard in to 1200 x 1200 μm blocks and stitched together with accuracy of within 10 nm. These files are finally converted to IWFL files that are readable by the VB6 hardware via in house software called 'Belle'. Once the pattern is read by the software the beam is blanked and the stage moved beneath it to each determined exposure. For the general set-up there are a total of 2^{20} exposure sub fields along each axis giving a resolution of:

$$\frac{1.31072\ \ mm}{2^{20}} = 1.25\ \ nm \qquad \textbf{3.2.1}$$

Parameters input by the user may then further affect pattern and exposure for example the amount the beam moves between each exposure is its step size which is equal to the resolution multiplied by a term known as variable resolution unit (VRU). It is sensible to choose a step size equal to the minimum required feature size divided by ~ 5 to give well defined spot features if it is too large lines may become tapered, too large and over-exposure may occur. The length of time (T) the beam dwells on each sub-field is determined by an input known as dose. This is related by:

$$\frac{DA}{I} = T \qquad \textbf{3.2.2}$$

Where D is the dose parameter, A the sub-field area and I beam current. Other factors to consider in pattern creation are electron forward and back scattering. This is where the resist alters an incident electron's velocity and direction slightly exposing more resist than specified (forward scattering) or the substrate atoms deflect electrons greater than 90° and hence back through the resist again exposing more resist than desired (back scattering). In extreme cases patterns need to be altered with proximity corrections to account for this however this tends to be needed only for small structures close together such as gratings and the fact high accelerating voltages (100 kV) are used in this work also lessens scattering and reduces the need for this.

Once the pattern has been written, the resist can then be ‘developed’. The CDL is removed first with a soak in MF-CD26 developer. The resist beneath can be developed in a solution of methyl isobutyl ketone (MIBK) diluted with IPA to specific concentrations and submerged at specific temperatures depending on the feature size required.

Many of the devices fabricated in this research require multi-layer patterns which require accurate alignment between them by a technique known as registration. When required, an extra lithography step is therefore performed prior to device fabrication to create small metallic markers to give the e-beam a reference to align later lithography levels to.

3.3 Selective Etching of Metals

Apart from a mild plasma etch used for removal of resist residue from samples, no other dry etches were used in this project due to the potential damage to the hydrogen-terminated

diamond surface. Instead wet etches were undertaken with samples submerged in a potassium iodide (KI/I_2) solution used to selectively etch the Au SL via the reaction [3.6]:

$$2Au + I_2 \longrightarrow 2AuI_2 \qquad \textbf{3.3.1}$$

This is chosen as it does not oxidise the diamond surface. Other acids may etch gold but will leave the surface oxygen-terminated and hence insulating [3.3]. Not much more is known about the interaction between KI/I_2 and hydrogen-terminated diamond beyond the fact it does not seem to damage the surface conductivity. To achieve a sensible etch rate, the Au etch solution is diluted with reverse osmosis (RO) water by a ratio of RO water 10:1 Au etch. Unfortunately although this form of etching has its benefits in protecting the surface termination it leads to a rough Au etch and is unrepeatable. It is used to create the source-drain gap in FETs by etching through the Au SL and undercutting beneath the resist layer to leave a gap as shown in Figure 3.3.1. This leaves the ohmic contact edges rough and the source-drain gap unpredictable as seen in Figure 3.3.2. Other pitfalls include the re-deposition of Au residue from the etch solution onto the diamond surface even after the sample is thoroughly rinsed in RO water.

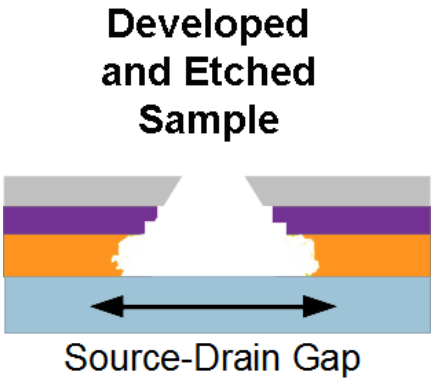


Figure 3.3.1: Approximate source-drain gap formed by Au etch

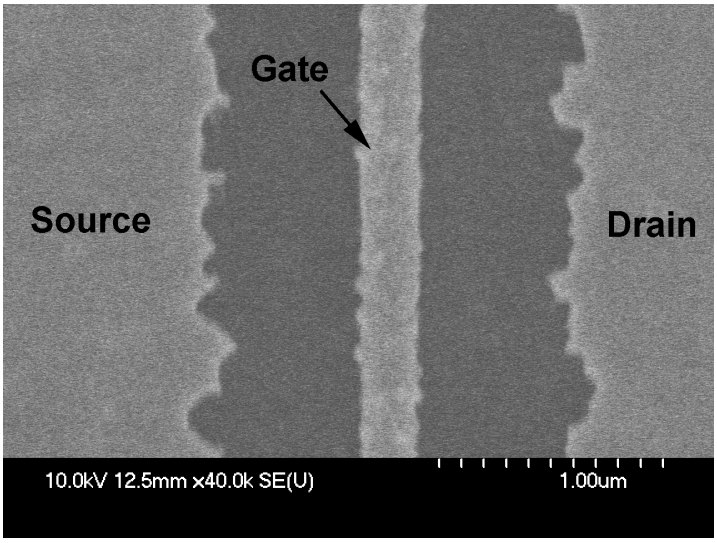


Figure 3.3.2: SEM image of diamond MESFET gate with rough ohmic contact edges visible

3.4 Metallisation Deposition, Ashing and Lift-Off Techniques

Metal can be deposited in the exposed and developed regions of the sample and then 'lifted-off' where not required by soaking in warm acetone for 2 hours which is enough to dissolve and strip the PMMA from the sample. To aid this process it is beneficial to spin on a bi-layer of resist with the bottom layer being a lower molecular weight and hence more sensitive to e-beam exposure than the top layer. Development will then produce an undercut profile which aids the lift-off process as it creates a clean break between the metal in contact with the semiconductor and that on top of the resist as shown in Figure 3.4.1:

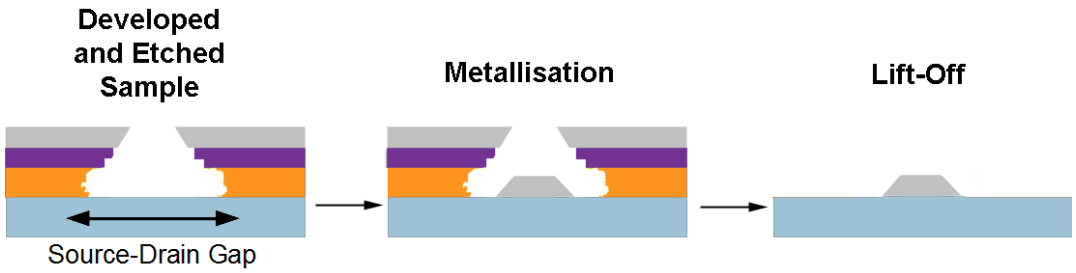


Figure 3.4.1: Metallisation and lift-off with the aid of bi-layer resist

Prior to etching the Au SL it is necessary to perform a low power oxygen plasma 'ash' to remove resist residue which is always present even after development and resembles granules of a few nanometres in size [3.7]. Plasma etching is a process whereby a high electric field ionises electrons from their atoms (in this case oxygen) giving radical species which will react with the resist and the products of this reaction are removed with the gas flow. The SL is used to provide protection to the hydrogen-terminated diamond surface from this process but nevertheless care is taken to ensure preservation of surface conductivity so the power is kept down to a relatively low 40 watts and only performed for 1 minute. This same oxygen based ash process may be used to provide electronic isolation around the outside of individual devices by selectively removing the hydrogen-termination from the diamond surface. In FET processing, typically a mesa-etch is required for electronic isolation, however here a weak oxygen plasma is sufficient to provide insulating regions. As diamond does not grow a native oxide after development and etching the sample may be left in atmosphere until metal deposition with no de-oxidisation step required. Metal may then be deposited via a number of evaporation or sputtering methods. The majority of metal deposition in this work utilised a Plassys MEB 550S e-beam evaporation tool as shown in Figure 3.4.2.

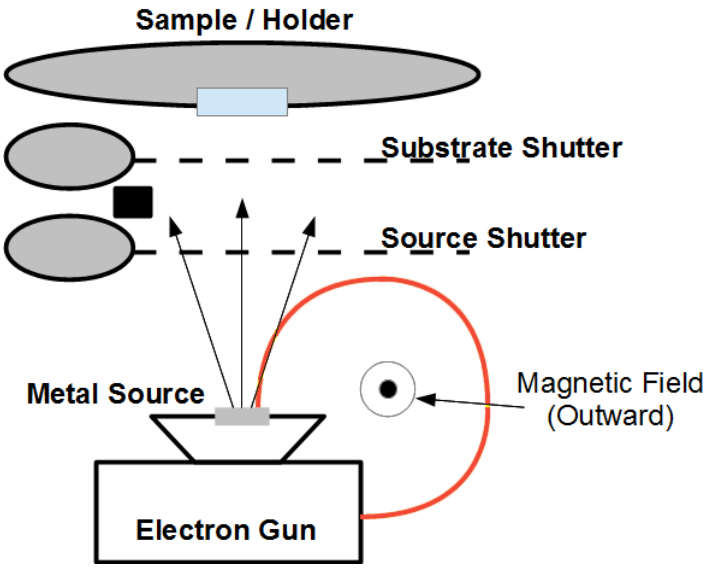


Figure 3.4.2: Simplified schematic of Plassys e-beam metal evaporation tool

This tool contains an electron gun operating similarly to the VB6 but using lower accelerating voltages (<50 kV) creating a beam which is magnetically focused on to an ingot of the required source metal to locally heat up and eventually sublimate specific regions of this metal yielding very high purity coatings over the sample. A quartz crystal is used to monitor the deposition rate, which is set to oscillate at a resonant frequency so as evaporated material hits the crystal it alters this frequency. With typical evaporation pressures being at 10^{-7} Torr the metal will travel unimpeded towards the sample giving a non-conformal, directional coating.

The e-beam lithography CDL is an example of metallisation with aluminium used as it can be completely removed via a short submersion in MF CD-26 with this developer not having any adverse effect on the resist beneath. This Al layer is kept at 15 nm for reasons discussed earlier although instead of being deposited at a standard Plassys deposition rate of 0.3 $nm.s^{-1}$ a much slower rate of 0.05 $nm.s^{-1}$ is used to keep stress on the resist and SL below to a minimum and prevent damage.

As mentioned in section 2.3 the hydrogen-terminated diamond surface leaves the Fermi level unpinned hence the metal-diamond interface can be tailored depending upon work function to give ohmic or Schottky contacts. For the FET gates aluminium is chosen as it has a low work function creating a Schottky barrier between diamond surface and metal. Gold is chosen for the ohmic contacts due to its high work function and the ability to selectively etch the Au SL to give ready-made ohmic contacts and minimise fabrication steps.

3.5 Standard Diamond MESFET Process Flow

The design of FETs for RF measurement is slightly more complex than for purely DC measurement (which will be shown in Section 4.4). Coplanar waveguides need to be incorporated into the device structure to land the three-armed RF probes on with a ground-signal-ground set-up to transmit the RF signal. In more conventional FET fabrication these waveguides would be deposited as bond pads to the main device in the final fabrication step but for this technology some essential alterations need to be made. Since a final additional layer of lithography (resist spin, bake and e-beam exposure) may well damage the surface conductivity of the exposed gate region, the waveguides here are incorporated in to the device structure partly in to the ohmic contact Au SL etch as extension of source

and drain contact pads and partly in to the gate deposition as an extension of the gate contact pad. Although this method works in as much as successful measurements can be obtained it leaves several non-ideal scenarios. The RF FET design can be seen in Figure 3.5.1.

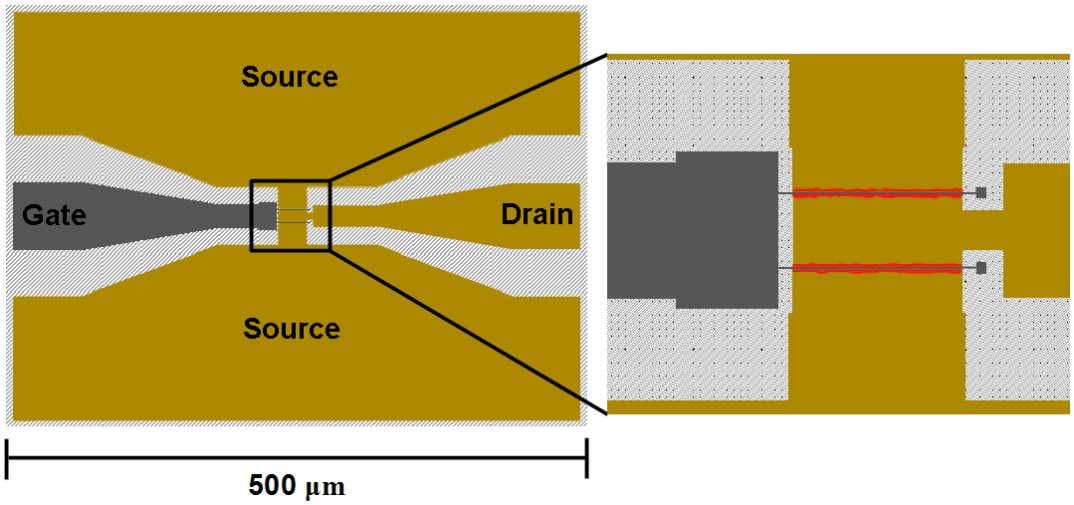


Figure 3.5.1: Layout of an RF FET with zoomed in view of device which utilises two gate fingers

The waveguide metal tends to be much thinner than is normal for such structures meaning these contacts are more resistive than would be desired and they will scratch off from the surface very easily usually after a single measurement making re-measurement difficult if not impossible. This also gives the undesirable situation of the waveguides being partly on insulating (gate pad) and partly on conducting (source and drain pads) material. Ideally these would all be on insulating material so as to minimise interaction between the metal and charge present in the substrate.

As the FETs are scaled to sub-100-nm dimensions the device yield becomes far less due to a higher probability of damage to the gate from more challenging lithography. With coplanar waveguides added to FET devices the total device size now takes up a significant amount of the usable surface area (each single crystal diamond sample is only 4.7 x 4.7 mm). So with a lower yield and only ~ 20 RF devices present on each sample measurement becomes extremely challenging and is compounded by device degradation from repeat measurement as will be discussed in the results section of this thesis.

The extra metal associated with the waveguides will bring additional resistance, capacitance and inductance which although not part of the device itself act as external parasitic components to degrade RF performance. Hence these need to be subtracted to give an accurate picture of the actual device operation especially as the source and drain RF pads are placed on non-insulating material.

The most straightforward way of doing this is creating two extra structures (a short and open) and measure and subtract the RF response of these from the overall measurements the process of which will be described in more detail in section 4.6. These on-wafer de-embedding structures can be seen in Figure 3.5.2. The open structure can be fabricated alongside the rest of the RF FETs with an extended isolation etch. However the short will require an extra fabrication step to deposit the extended gate pad and overlap the existing metal.

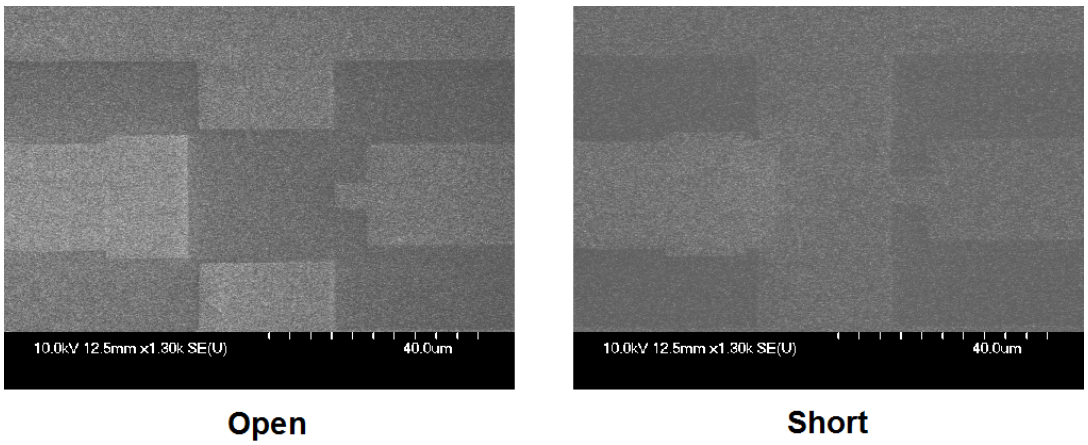


Figure 3.5.2: SEM images of on-wafer de-embedding structures

With this in mind the process flow by which the diamond MESFETs fabricated in this project follow can be categorised as seen in Table 3.5.1. With a summary of the gate contact deposition and source-drain gap definition also shown in Figure 3.5.3.

Step	Description
1	Sacrificial layer deposition
2	Marker deposition
3	Isolation/ohmic contact definition (plus waveguide)
4	De-embedding structure ‘gate pad’ deposition
5	Gate contact deposition (plus waveguide)
6	*Acceptor material deposition (not required for devices but investigated as a potential final step to provide stability)*

Table 3.5.1: Process flow for diamond MESFET fabrication

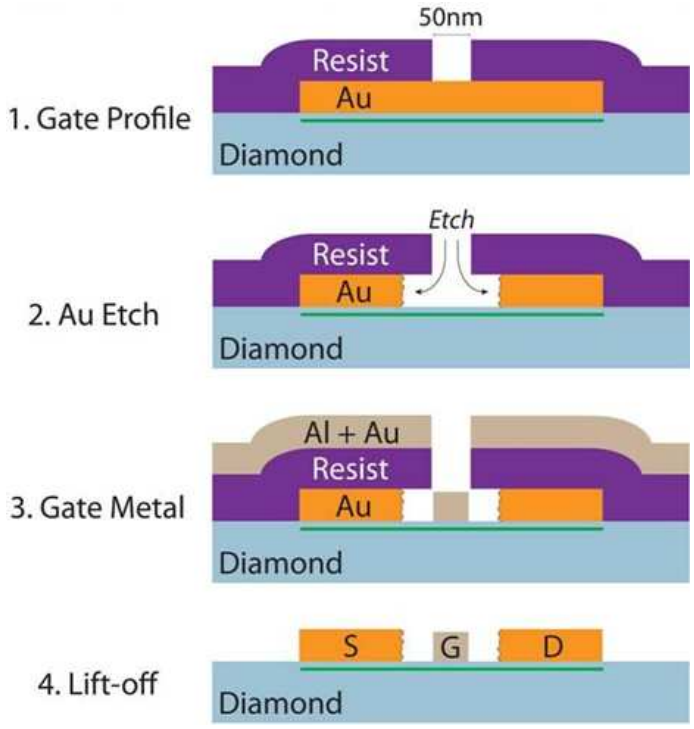


Figure 3.5.3: Gate contact deposition and source-drain gap definition

Note that the order of these steps is crucial and it is essential that the gate is deposited after the previous fabrication steps to ensure the exposed surface region may receive minimum exposure to high energy electrons and resist coating. In the case of acceptor material deposition it is particularly important that the exposed surface region does not have other contaminants such as resist residue prior to deposition. The details for each of these steps is described below with full details for each individual process being given in Appendix A.

1. *Sacrificial Layer Deposition:*

After the Hydrogen-terminated diamond sample is cleaned and ready for use an 80 nm Au SL is deposited to protect the hydrogen-terminated diamond surface from potentially damaging fabrication processes such as e-beam exposure or oxygen plasma [3.8]. Gold is chosen due to the ability to etch it with a chemical wet etch and the process of doing so not having a negative impact on the surface conductivity. There is however a significant challenge in using gold for this layer in that it adheres poorly to hydrogen-terminated diamond, so badly so in fact that a tiny scratch in the SL will cause the entire layer to buckle and begin peeling off when next exposed to vacuum (see Figure 3.5.4). Similarly if deposited all the way towards the edge of the sample, gold will begin peeling away from the edges due to this poor adhesion.

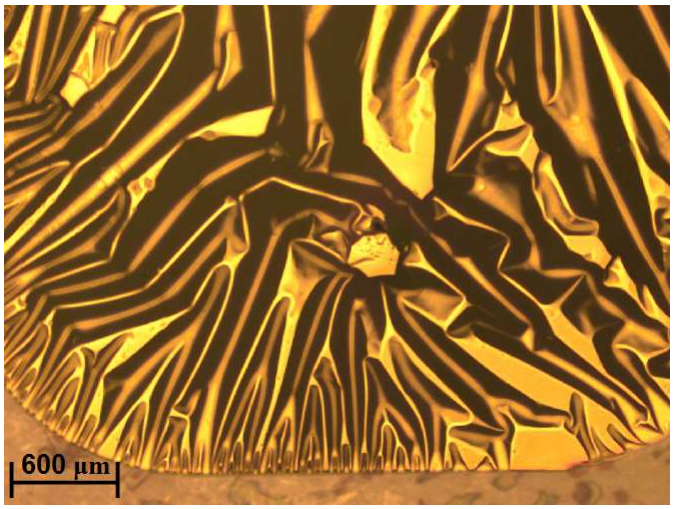


Figure 3.5.4: Au SL adhesion issues imaged via optical microscope

A specialised holder was therefore designed as shown in Figure 3.5.5 and used for the SL deposition where the sample sits in a shallow recess the same dimensions as itself (typically 4 x 4 x 0.5 mm for single crystal material and 10 x 10 x 0.5 mm for polycrystalline) and is clamped securely from behind with the front containing a rounded window slightly smaller than the sample to allow for SL deposition up to almost the edge of the sample leaving ~ 500 μm around the edges which can be used for e-beam alignment markers.

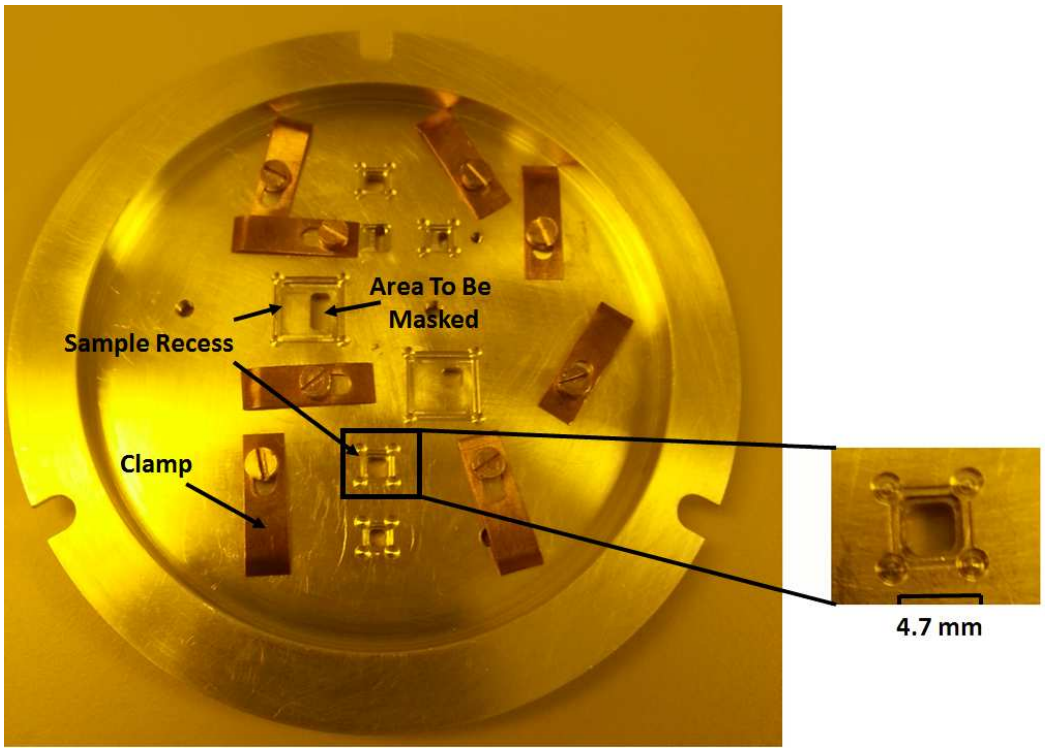


Figure 3.5.5: Specialised holder created for Au SL deposition

2. *Marker Deposition:*

As device fabrication requires several individual layers of lithography, it is essential to align each layer to the previous one accurately. Since this involves aligning the gate contacts to sub-μm accuracy it needs to be done by the e-beam tool and would be unrealistic to do by hand. Hence the first layer of e-beam lithography defines small arrays of metallic markers between the Au SL and the edge of the sample with several 20 x 20 μm squares in each along with a row of 150 x 150 μm crosses along the bottom edge of the sample as pictured in Figure 3.5.6.

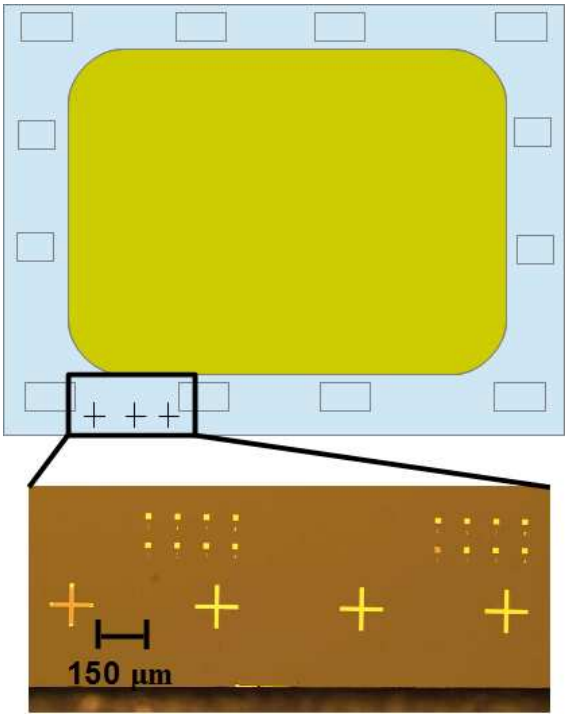


Figure 3.5.6: Marker and cross layout on typical diamond sample

The e-beam prior to performing lithography can then detect these markers. To ensure this can be done accurately a metallisation is used for the marker layer (20 nm Ti to promote adhesion to the diamond substrate topped with 100 nm Au) where the contrast between this and the substrate is clear from the backscattered electron intensity. It is important to have several markers in each array as this process of exposure can deform markers especially if subjected to an Au etch processing step. In performing alignment for a subsequent lithography level (referred to as a registration level) the beam begins by locating the bottom left hand corner of the sample and then measures the distance from here to the cross specified for use by the user. This determines accurately any difference between the pattern distance and the physical distance which may have arisen in deposition of the markers. Next the e-beam will attempt to locate ideally four markers around the edges of the sample (ideally in the corners) to produce accurate reference points across the substrate from which transformations can be made to write the substrate pattern exactly where required.

Due to the small size of the diamond samples another specialised holder needed to be created for the purposes of e-beam lithography as shown in Figure 3.5.7. This was necessary for the purposes of alignment.

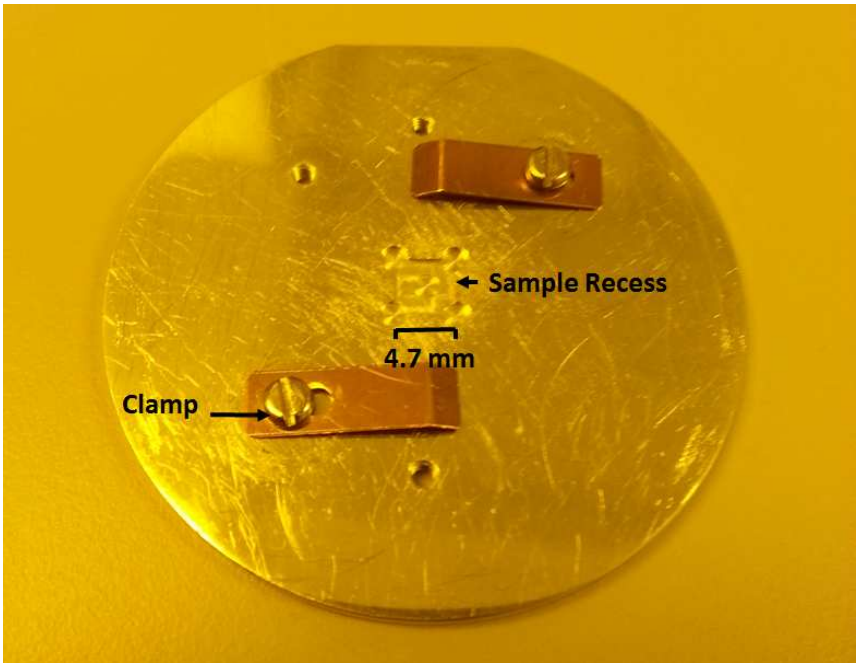


Figure 3.5.7: Specialised holder created for e-beam lithography

3. *Isolation/Ohmic Contact Definition (Plus Waveguide):*

Following the marker layer deposition, the Au SL may now be selectively etched to form the outer edge of source and drain ohmic contacts as well as the extended waveguides required for RF measurement. The exposed hydrogen-terminated diamond surface post-etch is then subjected to a brief oxygen plasma to electrically isolate individual devices, the recipe of which is the same as the resist ash although here the oxygen plasma interacts directly with the exposed hydrogen-terminated diamond surface leaving it oxygen-terminated and insulating [3.8]. The region intended for gate deposition at this point remains encapsulated by the Au SL and ready to be etched after further lithography. A device after isolation can be seen in Figure 3.5.8.

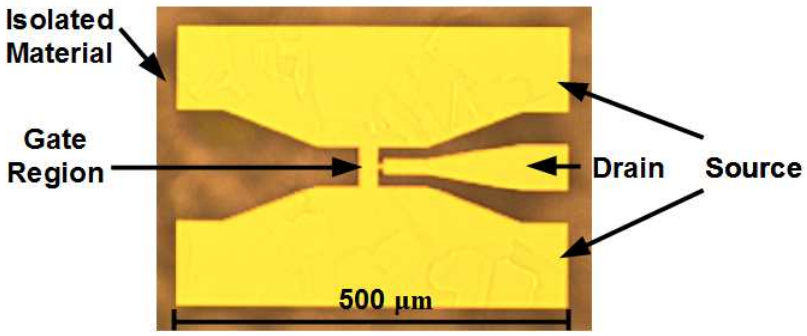


Figure 3.5.8: Isolated RF diamond MESFET

4. *De-Embedding Structure 'Gate Pad' Deposition:*

At this point an extra stage of lithography is used to deposit an extended gate pad for the short de-embedding structure. This cannot be incorporated in with the regular gate lithography level as it involves etching to remove and undercut the metal which would leave the short structure disconnected. Al is deposited for an extended gate pad which overlaps the device region creating an effective short. It is clearer now how some of the pads are on conductive material and some not, as the gate pad region will have received the oxygen isolation treatment prior to deposition. However the source and drain pads as well as device region will be protected by Au SL and will have conductive material underneath, making de-embedding the pad contributions from measurement all the more essential for accurate results.

5. *Gate Contact Deposition (Plus Waveguide):*

This is the most crucial step of the fabrication procedure as it defines the FET intrinsic properties and to a large extent the overall device performance. Simple rectangular gates were fabricated here using a much thinner bi-layer coating of PMMA than would be utilised for markers/isolation along with higher e-beam dose and lower VRU. Development is undertaken in a more highly diluted solution of MIBK for longer along with a standard ash, then as touched upon in section 3.3 a wet etch through the SL is performed with an undercut to create the source-drain gap. Gate metallisation takes place on top of the exposed diamond surface with a standard deposition of 25 nm Al / 25 nm Au employed. The height being low so as to maximise lift-off success, it is generally recommended that the maximum deposition height should be 1.5x feature length as above this in-fill will occur where the metal on the surface of resist overlaps the gap completely and blocks any

further deposition. Longer gate lengths could employ thicker metallisations but when scaled down to 50 nm thin metal layers are essential. Although T-gates would be desirable for lower gate resistance and hence better f_{MAX} performance this process is as yet unrefined and will take some additional research to incorporate into the Au SL process. The in-fill problem is illustrated in Figure 3.5.9.

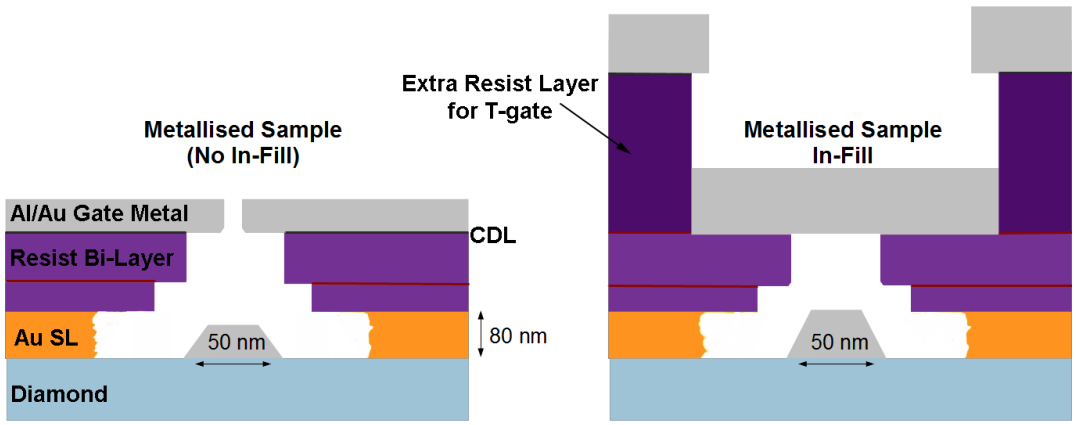


Figure 3.5.9: 50 nm length gates are limited to ~ 80 nm high metallisations

Al is chosen for its low work function and creates the necessary Schottky barrier between gate and diamond. As Al readily oxidises in atmosphere, an Au cap is deposited while still under vacuum to minimise this although oxidation may still take place around the sides and minimise the effective gate length. The gate 'feed' is formed as a large square feature at the end of the gate on oxygen-terminated material to aid adhesion to the substrate and again maximise lift-off success which is achieved as standard by a 2 hour strip submerged in 50° C acetone. Full realisation of 50 nm gates will be discussed in greater depth in Chapter 6 along with optimisation of other components such as the waveguides. A completed RF device is shown in Figure 3.5.10 along with the two finger gate region in Figure 3.5.11. Note that two gate fingers are used to enable the coplanar waveguide configuration but also increase gate width to increase drive current through the device.

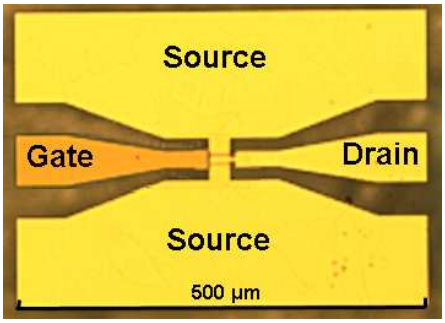


Figure 3.5.10: Completed RF device

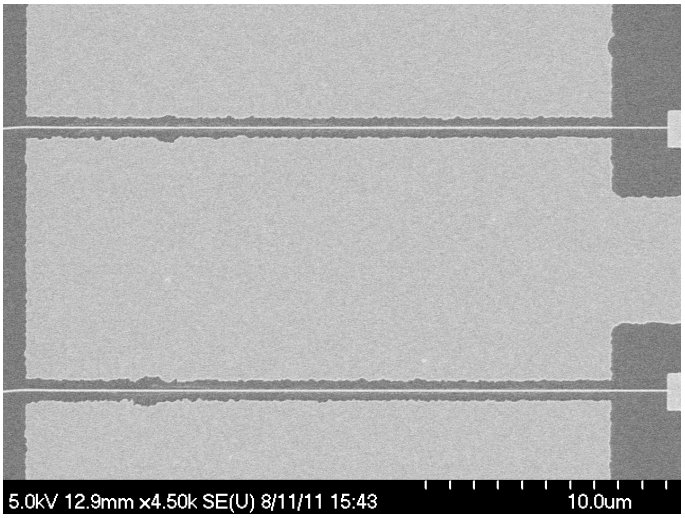


Figure 3.5.11: SEM image of two completed gate fingers

6. *Acceptor Material Deposition:*

Deposition of alternative acceptor materials was undertaken at the National University of Singapore and at Glasgow. Both $F_{16}CuPc$ and MoO_3 materials were deposited via resistive (thermal) evaporation. This being a similar process to that described for e-beam metallisation however instead of heating via an electron beam the sample holder itself is heated to temperatures hot enough to sublimate the material to be deposited. There is also the capability to heat the substrate holder and potentially drive off adsorbed atmospheric particles from the surface prior to deposition. Detailed results from these procedures are given in sections 7.2 and 7.3

3.6 Alternative Fabrication Procedures

An attempt was made to fabricate bond pad structures by a slightly modified fabrication procedure, instead of isolating the Au as seen in Figure 3.5.8. Instead just a small square was isolated as seen in Figure 3.6.1.

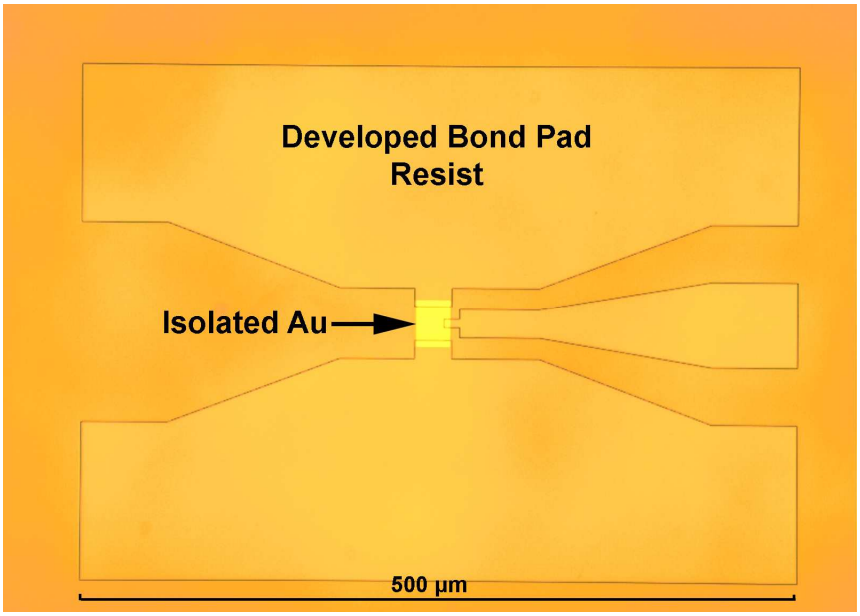


Figure 3.6.1: Isolated Au SL prior to bond pad deposition

A thick Au layer of 300 nm could then be deposited (with the bonus of being upon oxygen-terminated and hence insulating material), then gate lithography was undertaken as normal. Unfortunately this resulted in a very poor lift-off after gate lithography as seen in Figure 3.6.2, thought to be due to the thin resist bi-layer used for gate lithography not fully overlapping the thick bond pads hence not allowing acetone to reach and lift-off the gate metal.

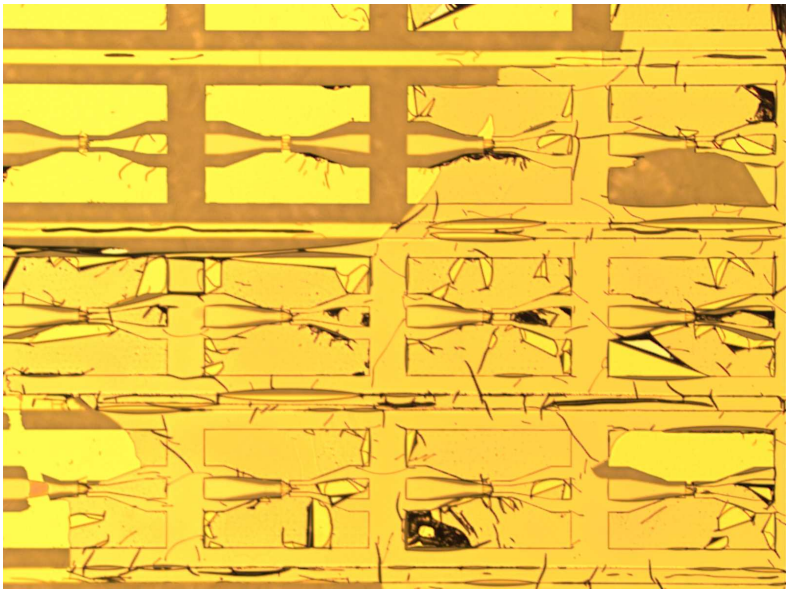


Figure 3.6.2: Poor gate lift-off due to thick bond pads

Alternatives to the standard fabrication procedure were investigated over the course of this work to try and replace the non-ideal Au SL process. For example an Al SL was implemented as an inverse process with the idea being that Au ohmic contacts could be deposited after an Al etch with MF CD26. The benefit being these ohmic contacts would be perfectly smooth as defined by the lift-off process. Other variations included an alternative ash process using SF6 gas rather than oxygen for the plasma. Metallisation via thermal evaporator deposition and also standard thick waveguides were also attempted to try and maximise stability and repeatability of device measurement. Results of these processes can be seen in section 7.1

3.7 Summary

This chapter has outlined the fabrication techniques used for diamond MESFETs giving processing details as well as the equipment used for fabrication. Most of these are based on standard semiconductor fabrication techniques yet almost all have needed some adaptation to ensure preservation of diamond sub-surface conductivity. Particular attention has been paid to successful fabrication of an RF device layout and the challenges in scaling to sub-100-nm gate lengths as well as potential techniques for enhancing and stabilising the surface conductivity.

The following chapter continues with details of how to characterise these devices to determine the figures of merit for measuring device performance.

References

[3.1] C. E. Nebel, C. Sauerer, F. Ertl and M. Stutzmann, "Hydrogen-induced transport properties of holes in diamond," *Applied Physics Letters*, vol. 79, no. 27, 4541-4543, 2001

[3.2] B. Baral, S. S. M. Chan and R. B. Jackmnan, "Cleaning thin-film diamond surfaces for device fabrication: An auger electron spectroscopic study," *Journal of Vacuum Science and Technology A*, vol. 14, no. 4, pp. 2303-2307, 1996

[3.3] J.J. Mareš, P. Hubík, J. Krištofik, J. Ristein, P. Strobel and L. Ley, "Influence of ambient humidity on the surface conductivity of hydrogen terminated diamond," *Diamond and Related Materials*, vol. 17, nos. 7-10, pp. 1356-1361, 2008

[3.4] F. Schellenberg, "A little light magic," *IEEE Spectrum*, vol. 40, no. 9, pp. 34-39, 2003

[3.5] A. I. M. Greer and D. A. J. Moran, "Charge dissipation layer optimisation for nano-scale electron-beam lithography pattern definition on diamond," *Diamond and Related Materials*, vol. 29, pp. 13-17, 2012

[3.6] K. R. Williams, K. Gupta and M. Wasilik, "Etch rates for micromachining processing – part II," *Journal of Microelectromechanical Systems*, vol. 12, no. 6, pp. 761-778, 2003

[3.7] D. S. Macintyre, O. Ignatova, S. Thoms and I. G. Thayne, "Resist residues and transistor gate fabrication," *Journal of Vacuum Science and Technology B*, vol. 27, no. 6, pp. 2597-2601, 2009

[3.8] M. Kubovic, A. Aleksov, A. Denisenko and E. Kohn, "Advances in diamond surface channel FET technology with focus on large signal properties," *Proceedings of IEEE Lester Eastman Conference on High Performance Devices*, pp. 90-99, 2002

4. Characterisation and Metrology

To fully understand device operation and to be able to compare their relative performance, accurate characterisation techniques are crucial. This encompasses not only device figures of merit but also material properties with particular focus on surfaces for this research. Knowledge of both the material and device allows further refinements which can then be made to fabrication procedures discussed in Chapter 3 to produce improved devices in the future.

This chapter details all forms of characterisation undertaken during this project. The Van der Pauw (VDP) method, which is used to extract the amount of charge present in the diamond material and its mobility, is initially discussed. This is complemented by transmission line method (TLM) measurements which assess parasitic resistances from ohmic contact structures. Capacitance-voltage measurement gives insight into the performance of the gate contact, while current-voltage measurements help analyse gate leakage. MESFET device characterisation follows with both DC and RF measurements discussed and the extraction of various figures of merit for the extrinsic and intrinsic device. Surface profiling is touched upon with atomic force (AFM) microscopy and scanning electron microscopy (SEM) used to investigate sample properties such as surface roughness as well as mechanical yield of devices. Finally photoelectron spectroscopy (PES) shows accurate material composition during in-situ growth with insight into any impurity incorporation and can also monitor any energy shifts during acceptor material deposition.

4.1 Material Characterisation

To achieve competitive device performance it is crucial to ensure material quality is exceptional with as few defects or impurities as possible to hinder movement of charge. It is also imperative the hydrogen-termination processing of diamond samples is a high quality again with little in the way of impurities as this contributes greatly to the surface structure as well as the ability to accumulate charge. As seen in Section 2.8 the amount of charge directly influences the drain current in an FET. Low-field mobility can tell us about device performance as it will have an effect on the R_{ON} of an FET it can also shed some light on the nature of charge transport through the diamond and if it is significantly impeded. All these factors are crucial for devices to realise their full potential.

The Hall effect utilises an external magnetic field transverse to a sample to exert a Lorentz force on the charge moving within it. The charge is then deflected perpendicular to the magnetic field (B_z) and its direction of motion as seen in Figure 4.1.1 resulting in an electric field (E_y) between the difference in charge across the sample opposing the Lorentz force which continues until equilibrium is reached. This potential difference is known as the Hall voltage (V_H) which is equal to E_y multiplied by the width of the sample (w) [4.1].

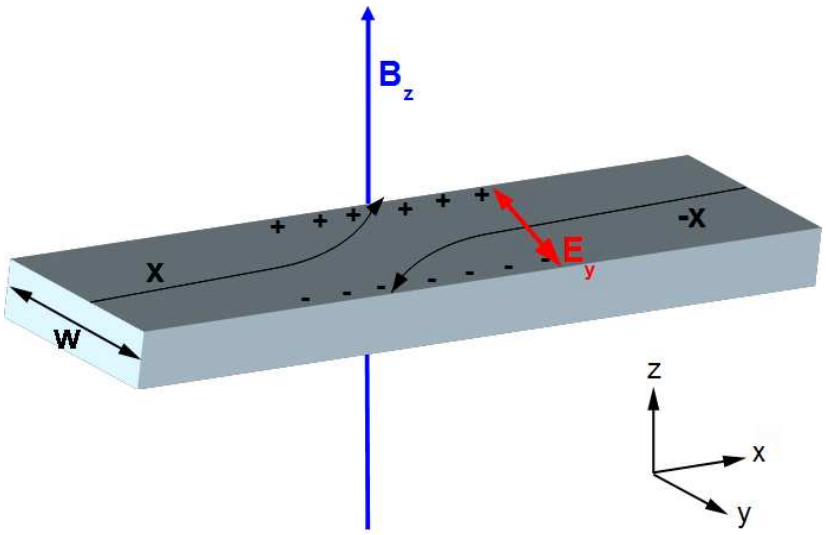


Figure 4.1.1: Deflection of charge carriers via the Hall Effect

The Hall Effect may be applied to a semiconductor material such as diamond via four ohmic contacts in a technique invented by Leo Van Der Pauw. As long as the sample is flat, relatively two-dimensional and homogeneous, measurement using this technique is independent of sample geometry [4.2]. A VDP structure fabricated on a diamond sample is shown in Figure 4.1.2. The Au SL layer is etched in a similar manner to that during device fabrication. Firstly isolation is performed using the same oxygen plasma as during MESFET fabrication around the edges of the VDP structure as seen on the left of Figure 4.1.2. An active region is fabricated in the centre again using the Au SL etch but without the plasma isolation.

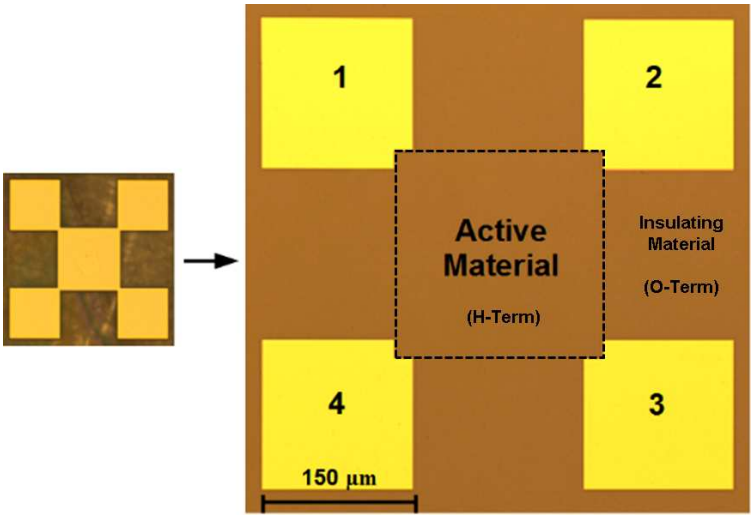


Figure 4.1.2: Van der Pauw structure as fabricated on diamond
(isolated structure on the left, finished VDP on the right)

As this structure is symmetrical, we can write:

$$\frac{V_{12}}{I_{34}} = \frac{V_{23}}{I_{14}} = R \qquad \textbf{4.1.1}$$

Meaning if a current is made to flow between two contacts i.e. 3 & 4 then the voltage measured across the opposite side (1 & 2) gives rise to a resistance that is symmetrical around the whole sample. Van der Pauw then showed that [4.2]:

$$\exp\left(-\pi\frac{t}{\rho}R\right)=\frac{1}{2} \qquad \textbf{4.1.2}$$

Where t is the thickness of the sample and ρ its resistivity which can be simplified to:

$$\rho=\frac{\pi t}{\ln 2}R \qquad \textbf{4.1.3}$$

Sheet resistance, R_{sh} is a material's resistivity divided by its thickness and can be used to simplify the above expressions further as well as providing a useful, easily measurable figure of merit for characterising the sample surface.

$$R_{sh}=\frac{\rho}{t}=\frac{\pi R}{\ln 2} \qquad \textbf{4.1.4}$$

R_{sh} can be measured from four point current-voltage probing of the pads without an external magnetic field. Mobility and carrier concentration however requires the magnetic field to instigate the Hall Effect. So if for example a small voltage (so that transport is linear and not saturated) is applied between pads 1 and 3 (V_{13}) and a transverse magnetic field is applied, the current flow will become deflected and charge will begin to accumulate at pads 2 and 4 building up an electric field between them (E_{24}). This continues until equilibrium is reached and no more charge flows where an expression can be stated for the forces in equilibrium [4.1]:

$$qE_{24}=qv_{13}B_z \qquad \textbf{4.1.5}$$

Where $qv_{13}B_z$ is the Lorentz force felt by charge carriers with v_{13} being the drift velocity and qE_{24} being the force opposing movement built up by the electric field E_{24}. Voltage can be measured between pads 2 and 4 and is equivalent to the Hall voltage (V_H) which may be related to the sheet carrier concentration (n_{sh}) by [4.1]:

$$n_{sh}=\frac{I_{13}B_z}{q|V_H|} \qquad \textbf{4.1.6}$$

The mobility may then be determined from [4.1]:

$$\mu = \frac{1}{qn_{sh}R_{sh}} \qquad \textbf{4.1.7}$$

Further measurements may then be taken between each of the diagonal contacts in both directions with a total averaged value for a more accurate measurement.

This technique is useful for characterising material properties such as carrier concentration and mobility which can vary significantly due to impurities such as boron contamination or poor quality hydrogen-termination. This should be easy to discern from Van der Pauw measurements as carrier concentration would be lower than expected due to less free charge being present. Mobility may be lower or higher than expected depending on trapping within the crystal structure and scattering mechanisms. Unfortunately if there are similar amounts of holes and electrons it is not possible to discern the two using this technique. The Hall voltage accounts for the overall charge difference between pads and hence it is more suitable for use on samples where the carrier concentration for one charge carrier is orders of magnitude higher than the other. This should be true of hydrogen-terminated diamond. However in diamond structures using electron acceptor materials on the diamond surface there may be two effective channels with opposite charge carriers in each. This will need to be carefully considered upon deposition of these materials.

4.2 – Ohmic Contact/Sheet Resistance Measurement

In FET devices to maximise performance, extrinsic resistance needs to be kept as low as possible, especially as dimensions are scaled to the nanometre scale. Creating transmission line model (TLM) structures allows the determination of these resistances as they essentially resemble FET devices minus the gate which allows for the accurate measurement of the extrinsic parasitic resistances that contribute to R_{ON}. Looking back again at Figure 2.7.4 we can see the elements that contribute to R_{ON} in a MESFET. Several gaps of differing separation are required to determine a trend. Fabricated TLM test structures may be seen in Figure 4.2.1.

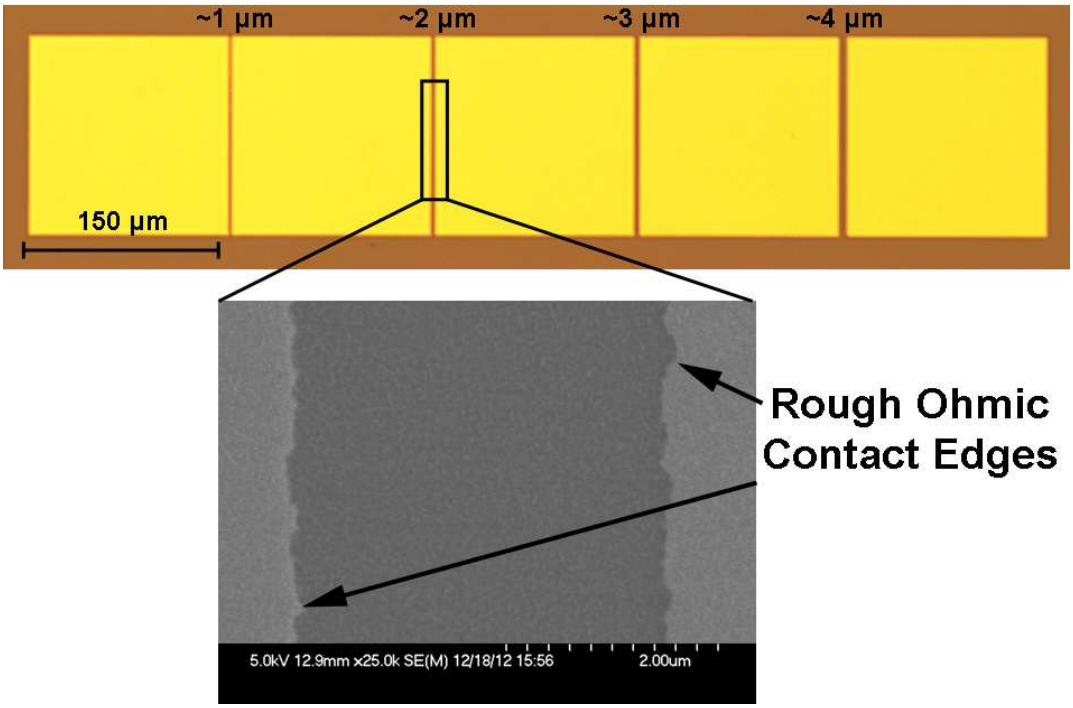


Figure 4.2.1: Fabricated TLM structure with approximate gap distances and SEM image of the 2 µm gap (actual gap distance of 3.5 µm)

The sheet resistance is assumed to be the same in each hence the resistance measured should increase proportionally to gap separation which may be plotted as in Figure 4.2.2 [4.3].

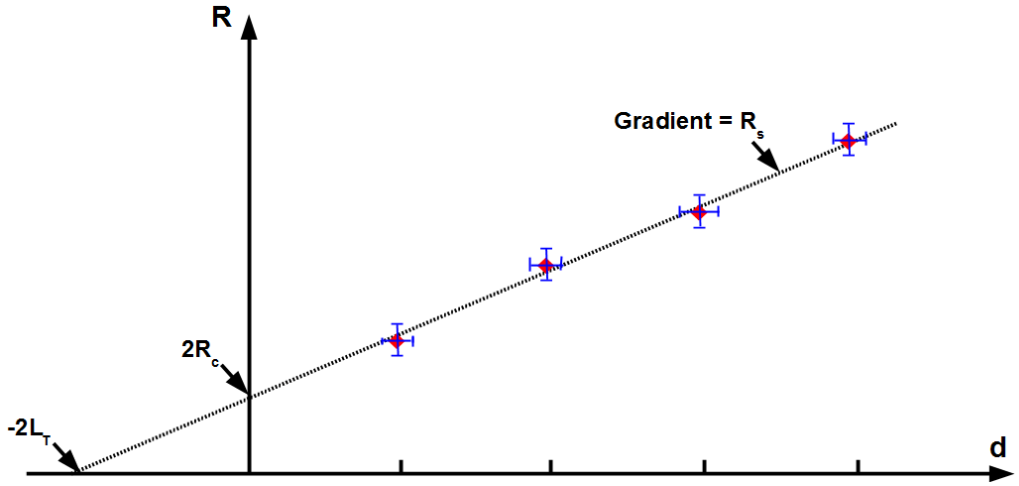


Figure 4.2.2: Plot of resistance with varying gap separation as seen in a TLM structure

The total contact resistance for both ohmic contacts ($2R_c$) may be extracted by extrapolating the trend backwards to zero contact separation whilst the gradient of the line gives the sheet resistance (R_s) divided by the contact width (W). L_T is known as the transfer length and gives the minimum contact length necessary for a contact to display ohmic type behaviour.

There are two conventions for quoting contact resistance: That normalised to the width of the device (Ω.mm) or that normalised to the area of the contact that contributes to current flow ($\Omega.cm^2$). The second, which is also referred to as the specific contact resistance, is useful as it takes in to account L_T and hence current crowding where a non-uniform current density is present through a contact. However this process assumes that the sheet resistance under the contact is equal to the sheet resistance of the material between the contacts, thus potentially giving an inaccurate value due to the inaccurate value extracted for L_T. Due to difficulty in determining an accurate vale for R_{SH} beneath the ohmic contact Ω.mm is quoted in this work.

Structures were designed to have 150 x 150 μm ohmic pads with separations of 1, 2, 3 and 4 microns although as the Au etch process is used to fabricate these gaps they may vary substantially from these designed values. It was therefore important to observe each under a microscope to determine the exact separation which will still involve a large margin for error due to the rough contact edges formed by the etch.

The outside of each rectangular structure is isolated with an oxygen plasma to remove the hydrogen-termination and oxygen-terminate the surface in these areas. This acts to isolate the TLMs electrically and prevent any fringing current around the edges of each gap, ensuring an accurate measurement.

4.3 - CV Measurement

As well as testing the quality of the ohmic contacts it is also important to characterise the gate contact so the full picture of device operation may be broken down in to its component parts. To do this, diode structures are fabricated with a circular aluminium gate contact surrounded by an Au ohmic as pictured in Figure 4.3.1.

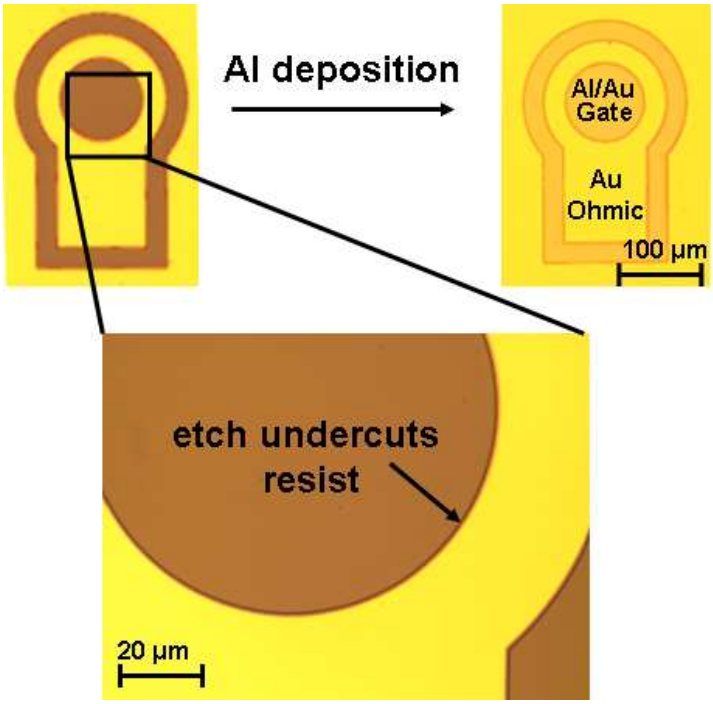


Figure 4.3.1: CV structure during fabrication with Au etch undercutting resist (top left) to leave a gap between Al and Au post deposition

This diode structure serves several purposes with the first being the ability to demonstrate accumulation and depletion beneath the gate contact by measuring capacitance with respect to voltage as well as shedding some light on trapping mechanisms between the material and gate contact. This is seen in hysteresis of capacitance sweeps by measuring both from off to on and on to off voltages while the inability to maintain accumulated charge may indicate leakage. Sweeps may be performed at different frequencies with lower frequencies more likely to reveal trapping as a higher frequency sweep will move charge faster than the time constant of most trapping mechanisms. This structure also gives the potential to test for gate leakage current by measuring current with respect to voltage.

Figure 4.3.2 shows a typical capacitance-voltage sweep with capacitance normalised to the area of the Al gate contact and both forward and reverse sweeps present showing some hysteresis between the two.

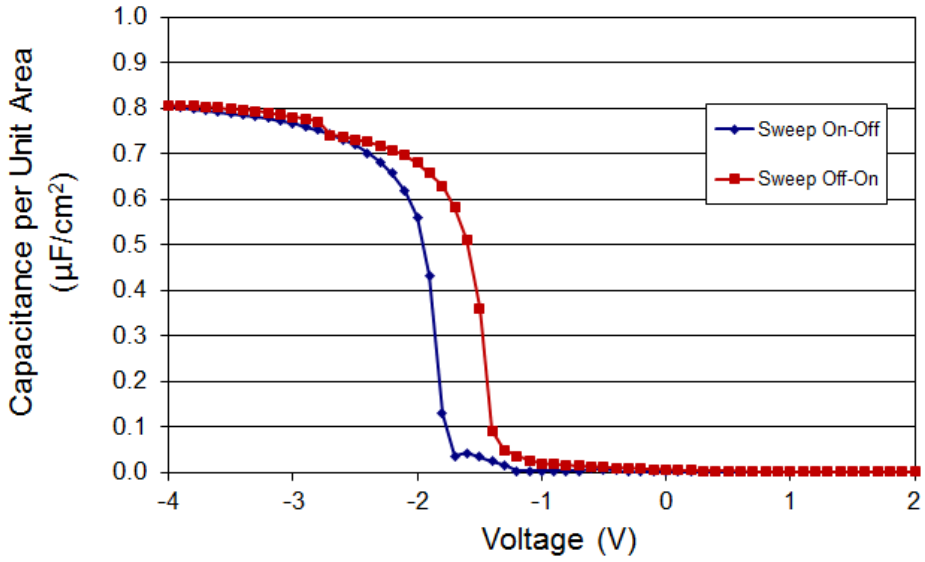


Figure 4.3.2: CV sweep for 100 µm diameter diode structure on hydrogen-terminated diamond at 1 MHz

4.4 - DC Device Characterisation

The RF device setup as discussed in Chapter 3 is used for the majority of measurements in this work however some more basic preliminary FETs are also discussed which employ just a single finger gate and small pads for DC measurement. This allows FET characterisation via standard DC probes without the need to fabricate more complex waveguide structures. FET characterisation as well as TLM and CV measurement was performed using an Agilent B1500 semiconductor parameter analyser (SPA) running Agilent's EasyEXPERT measurement software. The DC FET structures are shown in Figure 4.4.1

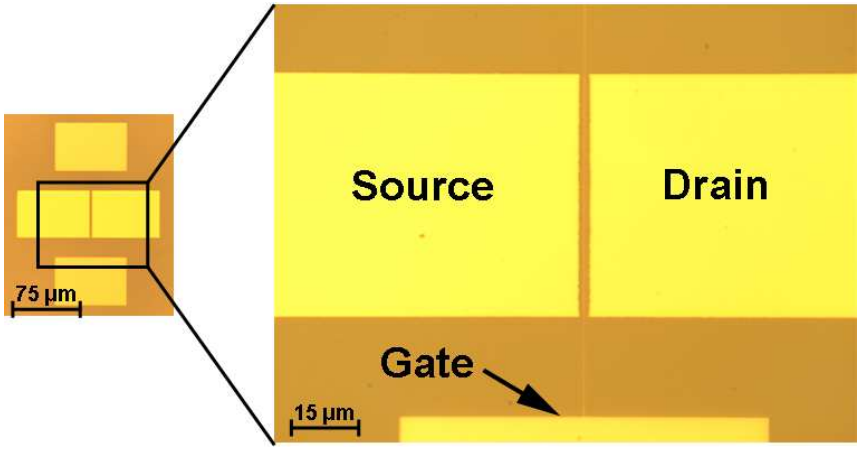


Figure 4.4.1: Fabricated DC FET structure utilising single finger gate and basic probe pads

To measure the drain current characteristics of an FET device, the source is kept at ground while the drain voltage is swept across the desired range. This may be repeated several times with varying gate voltages to give full I_{ds}-V_{ds} characteristics, an example of which may be seen in Figure 4.4.2. These are known as the output characteristics with the current conventionally normalised to gate width i.e. $mA.mm^{-1}$.

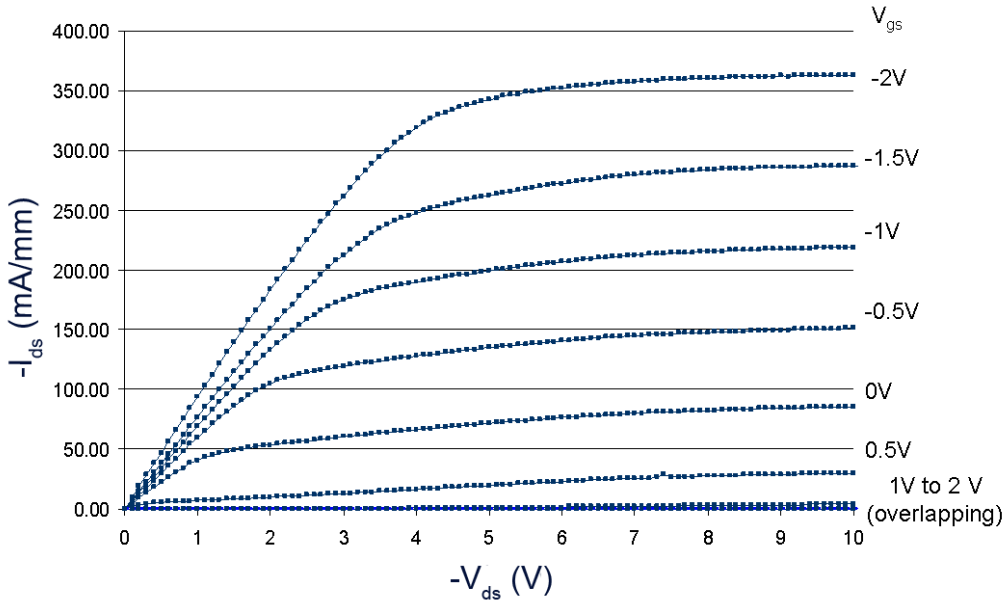


Figure 4.4.2: Output characteristics for 100 nm gate FET

To measure transconductance, a similar process is performed but instead gate voltage is swept while the drain voltage is incrementally stepped to give an I_{ds}-V_{gs} plot. This is known as the FET transfer characteristics. The change in the drain current with respect to gate voltage may then be plotted to give transconductance as seen in Figure 4.4.3 and as discussed previously in Section 2.8. These measurements yield the important DC figures of merit also discussed in Section 2.8. Finally gate leakage may also be monitored for different gate or drain voltages by measuring gate current with respect to either drain or gate voltage.

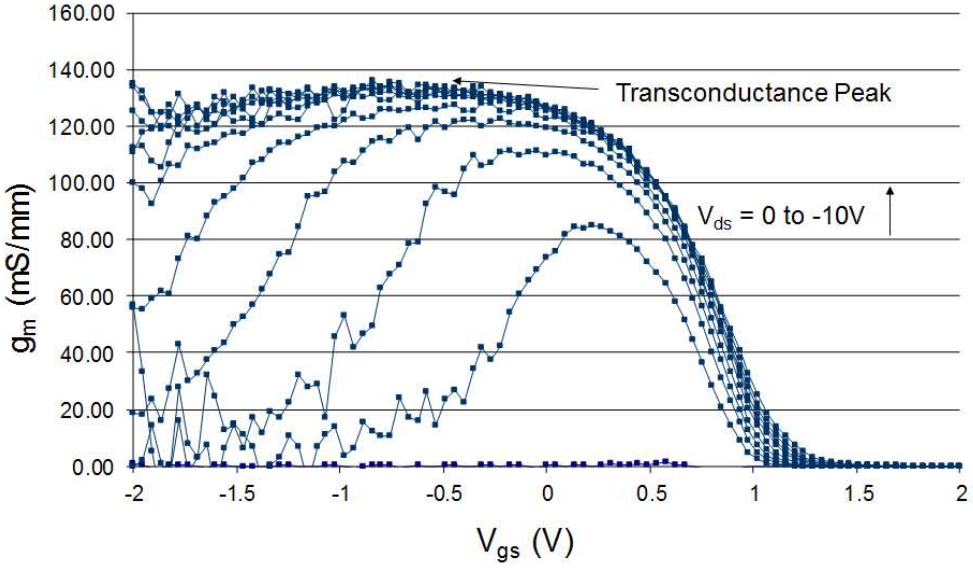


Figure 4.4.3: Transconductance for 120 nm gate FET

4.5 - RF Characterisation

For DC characterisation relevant performance metrics can be related to static currents and voltages. However as measurements move to higher frequency, small signal parameters (S-parameters) become more relevant. These describe the amount of RF signal transmitted and reflected through a device at a given frequency and hence vary with both frequency and bias. It is possible to model a diamond MESFET as a 2-port network for this purpose as shown in Figure 4.5.1. A signal is sent in to both ports and four s-parameters describe the resulting signal as described in Table 4.5.1.

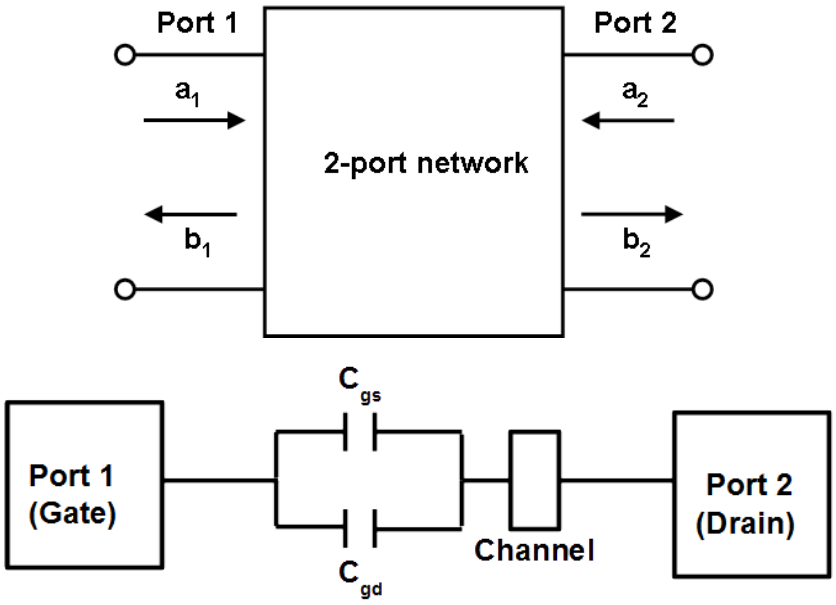


Figure 4.5.1: 2-port network including input and output signals (above).
Visual representation of MESFET 2-port network (below)

S-Parameter	Description
S_{11}	Input Reflection Coefficient
S_{22}	Output Reflection Coefficient
S_{12}	Reverse Gain
S_{21}	Forward Gain

Table 4.5.1: S-parameters and their meaning

In this work there is a particular interest in S_{21} as this can be converted to the H-parameter H_{21} which represents the current gain of the device. To visualise the complex impedance response with frequency of the MESFET device a Smith chart is plotted as shown in Figure 4.5.2 where all S-parameters may be plotted simultaneously.

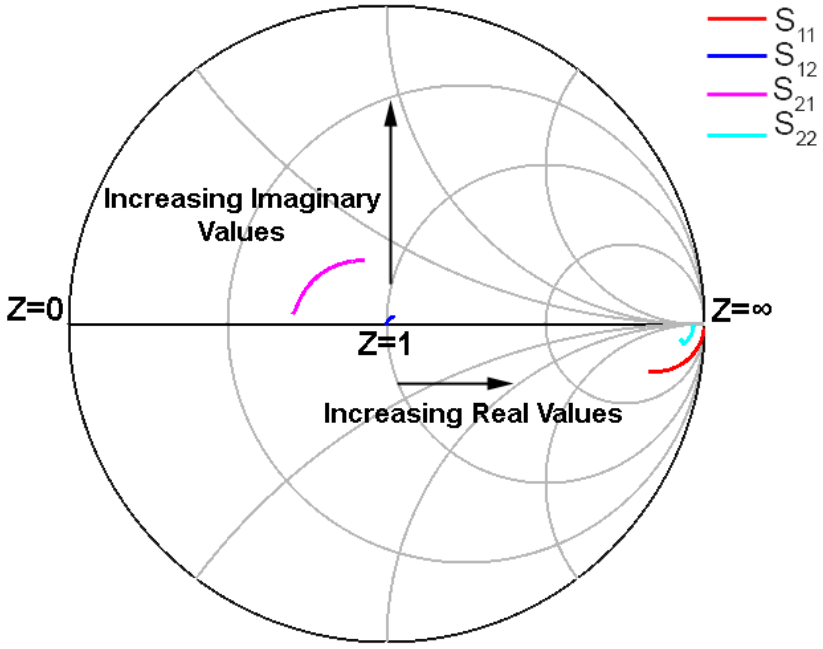


Figure 4.5.2: Example Smith chart

The horizontal axis represents the real part from zero at the left hand side to 1 in the centre and infinity at the right hand side with circles representing constant real values. The complex part of the impedance is represented vertically being zero at the centre, positive (or inductive) in the top half and negative (or capacitive) in the bottom half of the chart. The curved lines represent constant imaginary values. The Smith charts shown in this work are normalised to a characteristic impedance of 50 Ω, so the centre where Z = 1 represents a 50 Ω load.

RF characterisation in this project was carried out with the SPA with Picoprobe probes replacing the standard DC probes as these are capable of both DC and RF measurement. These are connected via Agilent frequency extender arms to an Agilent E8361A PNA network analyser. As touched upon in Section 2.9 when it comes to RF measurement the FET needs to be treated as a two-port device so a signal may be sent into each port and the fraction of reflected and transmitted signal is measured by scattering parameters (S-parameters) which describe both magnitude and phase of these signals across a specified frequency range and bias conditions. The diamond MESFET can be treated as such with

port 1 being the gate, port 2 drain and the source as earth as seen in with the input (a_1 and a_2) and output (b_1 and b_2) signal contributions also shown.

The signals are related to each other in a matrix format and it is not only S-parameters which may be used to describe the action of the network on these signals, there are also H, Y and Z parameters although S-parameters are the most straightforward to obtain with two simple expressions relating them to the signals at each port:

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad \textbf{4.5.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad \textbf{4.5.2}$$

If the 2-port network is modified so that a_2 or $a_1 = 0$ by creating a signal source at port 1 and terminating port 2 with a 50 Ω load to ensure no reflection making a_2 negligible or vice versa making a_1 negligible then the S-parameters are related as so:

$$S_{11} = \frac{b_1}{a_1}, \quad S_{21} = \frac{b_2}{a_1}, \quad S_{12} = \frac{b_1}{a_2}, \quad S_{22} = \frac{b_2}{a_2}$$

Calibration of the measurement apparatus is required to obtain accurate S-parameter measurements. This effectively removes the contribution of the probes, cables and the actual network analyser system itself from measurement data. Several structures with a known signal response may be used to calibrate the system. These are taken from a Cascade Microtech Impedance standard substrate (ISS). Standard short, open, load, thru (SOLT) calibration was utilised in measurements for this research where an open circuit is created by simply raising the probes from the substrate. The short, load and thru are fabricated on the ISS where the short resembles two strips of metal to short circuit the three tips on each probe together, thru is a strip of metal for each tip between ports 1 and 2 and finally line consists of two 100 Ω resistors in parallel between the tips on each probe to give in total a 50 Ω characteristic impedance. These structures are shown in Figure 4.5.3.

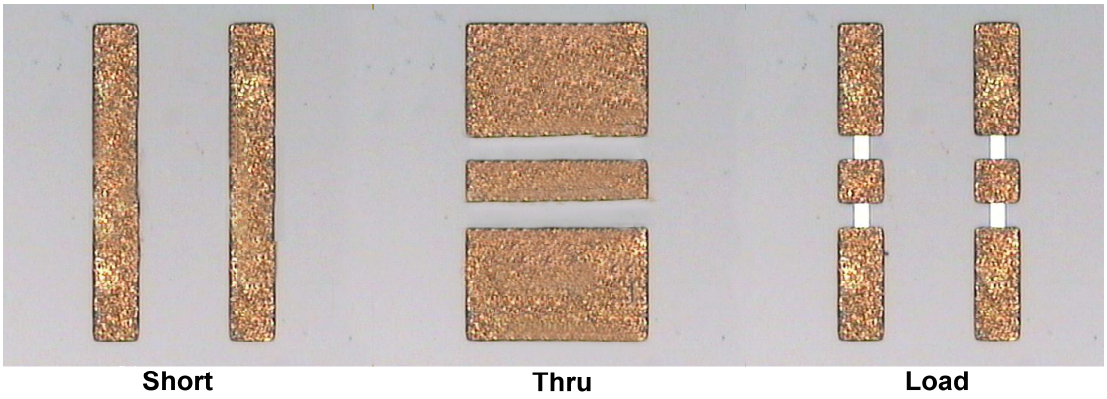


Figure 4.5.3: Short, through and line calibration structures

Although this allows for accurate RF measurement there is still a significant contribution to the S-parameters present from the on-wafer coplanar waveguides connecting the probes to the device. To accurately measure the FET response it is important to de-embed the effects of these and be left with the extrinsic device performance as this is how the device would appear in a potential integrated circuit (IC) i.e. the waveguides are purely to enable RF measurement. There are two methods of achieving this: - they may be modelled as part of the equivalent circuit if enough is known about their precise dimensions and interaction with the substrate. However the situation is complicated here in that the waveguides sit on both insulating and semiconducting material giving complex interactions which are extremely challenging to model. Hence the on-wafer de-embedding structures as discussed in Section 3.5 were employed with their S-parameters independently measured and then their contributions subsequently removed. This was done via a two-step de-embedding procedure on each device removing the parallel and series parasitic elements of the waveguides leaving just the device under test (DUT) [4.4]. The parallel elements are obtained by converting S-parameters of the open structure to Y-parameters while the series elements are obtained from the Z-parameters of the short structure.

Getting from device S-parameters to RF figures of merit still requires some manipulation. To obtain cut-off frequency (f_T) S-parameters may be converted in to H-parameters as shown in equation 4.5.3 with H_{21} giving the current gain of the FET [4.5].

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+(S_{12}S_{21})} \qquad \textbf{4.5.3}$$

If this is then plotted against frequency the point where H_{21} reaches unity gives the value for f_T. Current gain decreases at a rate of -20 dB/decade if the cut-off frequency occurs higher than the upper limit of the measurement frequency this line may be extrapolated to give an accurate value. In terms of power gain and extracting f_{MAX} the process becomes more complex and it becomes necessary to deal with Maximum Stable Gain (MSG) and Maximum Available Gain (MAG). MSG is simply defined as [4.6]:

$$MSG = \frac{|S_{21}|}{|S_{12}|} \qquad \textbf{4.5.4}$$

This applies to the region of operation where the FET is described as 'conditionally stable' as it could potentially oscillate under certain load impedances. This region can be defined by Rollet's stability factor (K) [4.6]:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}S_{12}|} \qquad \textbf{4.5.5}$$

When K < 1 the device obeys the MSG regime above, if however K > 1 the device becomes 'unconditionally stable' where the power gain now follows MAG [4.6]:

$$MAG = \frac{S_{21}}{S_{12}}\left[K + \left(K^2 - 1\right)^{\frac{1}{2}}\right] \qquad \textbf{4.5.6}$$

The second important RF figure of merit f_{MAX} can then be extracted at the frequency at which the power gain becomes zero. The method of extracting f_{MAX} here is graphically and is the method employed throughout this work and can be seen in Figure 4.5.4.

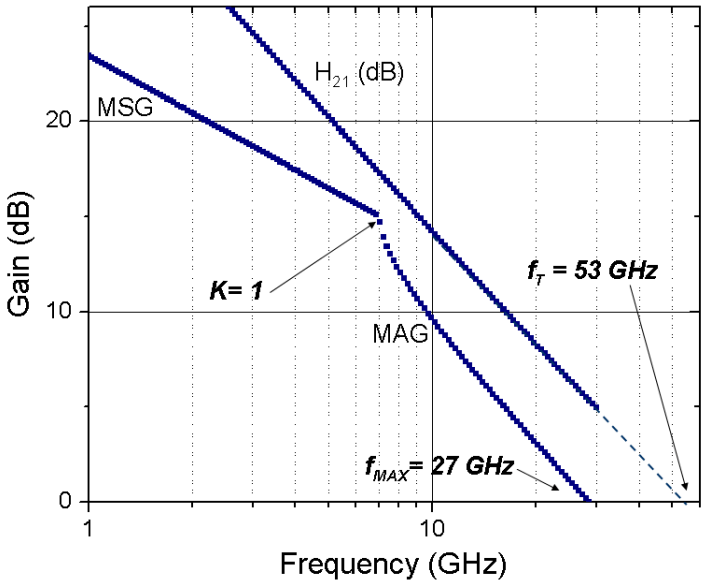


Figure 4.5.4: Example plots of H21, MSG and MAG with extraction of figures of merit taken from 50 nm gate length FET

Unfortunately due to the thin poorly adhering waveguide metal used to fabricate the FETs in this work, it is difficult to characterise RF devices more than once and even so repeat measurements are seen to reduce the DC current performance slightly each time most likely due to instabilities in the adsorbate layer. Fresh devices for each measurement are therefore desirable, although limited structures are available per 4.7 x 4.7 mm single crystal diamond sample which presents difficulties in obtaining large systematic volumes of data as well as making measurement of multiple bias points unrealistic for this work.

4.6 - Surface Profiling

In addition to device electrical characterisation there are some tools which further detail device structure along with material quality and can shed light on issues with device yield. The Atomic Force Microscopy (AFM) technique uses a silicon cantilever with a sharp tip of the order of a few nm across which is scanned via a piezoelectric scanner. This moves across the specified sample area and the vertical deflection of the tip by sample features is measured by a laser providing feedback to the AFM software which produces a topographical map of the area scanned. All AFM work undertaken in this project used a

Veeco Dimension 3100 SPM. There are many different operating modes available however only contact mode was used for this work as features are not so fragile the tip would cause them damage.

The AFM allows accurate measurement of surface roughness of the diamond sample before any fabrication takes place. For device fabrication, samples should be as smooth as possible (ideally sub-nm) to produce less scattering mechanisms at the surface which could heavily impact device performance. The AFM may also confirm metallisation thicknesses or resist profiles although it is somewhat less adept at lateral measurement due to the limitations associated with the dimensions and geometry of the AFM tip. The tip is only capable of measuring features larger than its own dimensions i.e. for a trench that is smaller than the size of the tip accurate measurement is impossible. Other features such as an overhang would also be difficult to measure with AFM.

Scanning Electron Microscopy (SEM) may be used for assessing features that are too small for optical microscopy and will readily pick up small surface features as well as giving very accurate lateral measurements. Operation is very similar to the electron beam lithography set up described in Section 3.2 although the accelerating voltage is either 10 or 20 kV, so much lower than for lithography purposes. This project's work was carried out with a Hitachi S4700 Field emission SEM and relies on the measurement of the emission of secondary electrons from a sample. This is useful in observing features such as the source-drain gap of a finished FET or an Au etched TLM. It can also shed light on fabrication errors such as broken or discontinuous gates and residue from the Au etch.

4.7 Photoelectron Spectroscopy (PES)

X-ray photoelectron spectroscopy (XPS) is a technique which enables characterisation of the composition of materials and their electronic states. Relying on the photoelectric effect the sample is exposed to x-ray radiation and a specialised synchrotron facility is required to produce the high energy x-rays used in this work and hence XPS characterisation was performed by collaborators at the National University of Singapore. Lower energy ultra violet radiation was also used for UVPES. Due to surface contamination post atmospheric exposure it is desirable to measure in-situ during or immediately after growth.

The binding energy (E_B) of an electron emitted via the XPS process is given by [4.7]:

$$E_B = E_\gamma - \left(E_{K.E.} + \phi\right) \qquad \textbf{4.7.1}$$

With Eγ being the x-ray photon energy, $E_{K.E.}$ the emitted electron's kinetic energy and ϕ the work function of the spectrometer. From measurement E_B may be accurately worked out and a plot may be produced as shown in Figure 4.7.1.

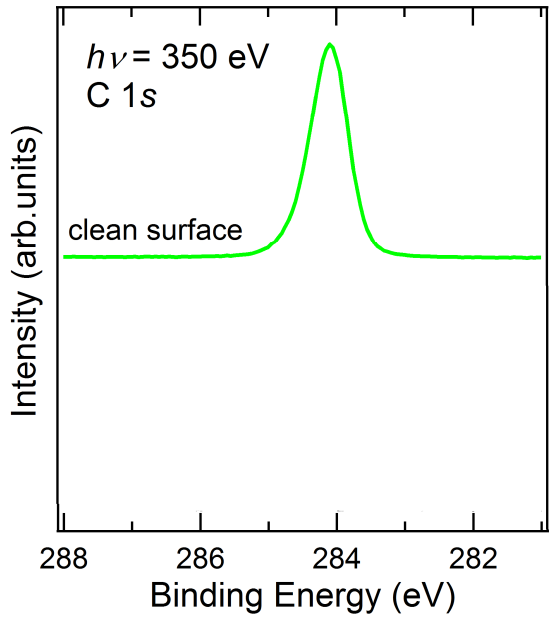


Figure 4.7.1: XPS plot showing the C1s peak characteristic of a clean diamond surface (irradiated with 350 eV x-ray synchrotron radiation)

Each element has a characteristic XPS peak and the number of counts for each binding energy is directly related to the amount of that element present within the surface of that sample hence an accurate picture of sample composition may be obtained including any potential contamination i.e. residual boron or nitrogen within diamond.

4.8 Summary

The various techniques used to characterise the diamond material and devices fabricated upon it have been summarised in this chapter. It is crucial to fully understand these

methods their calibration and application to be able to produce accurate measurements as well as de-embedding external measurement data from actual devices.

Particularly important is the Hall effect which can show to an extent material purity and doping while TLM and device measurement allow accurate device modelling and extraction of figures of merit to assess overall performance. PES is used to monitor the composition of the diamond surface during acceptor material deposition. Before discussing the results of this research the next Chapter briefly summarises the very latest developments in diamond FET technology.

References:

[4.1] S. M. Sze and K. K. Ng, Physics of semiconductor devices, 3rd Edition, John Wiley & Sons Inc, pp. 30-35, 2007

[4.2] L. J. Van der Pauw, "A method of measuring specific resistivity and Hall effect of disc of arbitrary shape," *Philips Research Report*, vol. 13, p. 1, 1958

[4.3] G. K. Reeves, H. B. Harrison, "Obtaining the specific contact resistance from transmission line model measurements," *IEEE Electron Device Letters*, vol. 3, no. 5, pp. 111-113, 1982

[4.4] T. Ytterdal, Y. Cheng, and T. A. Fjeldy, Device modelling for analog and RF CMOS circuit design, Wiley, p. 101, 2003

[4.5] D. A. Frickley, "Conversions between S, Z, Y, H, ABCD and T parameters which are valid for complex source and load impedances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205-211, 1994

[4.6] S. J. Orfanidis, Electromagnetic waves and antennas, Rutgers, pp. 535-545, 2010

[4.7] D. Briggs, Surface analysis of polymers by XPS and static SIMS, Cambridge University Press, p. 7, 1998

5. Current Technology Review

In this chapter, the current state of the art in diamond FET technology is discussed. Compiling the latest developments in surface transfer doping of diamond, device fabrication and performance a benchmark can be set out to compare the results in the following chapters to as well as giving insights into new routes to repeatability and eventual commercialisation of this technology.

Other routes to diamond FET fabrication are also discussed such as, boron delta-doping of diamond which has yielded some preliminary device data although the performance of these FETs has some way to go to match surface channel FETs.

5.1 Surface Transfer Doping

Since the surface transfer doping model for atmosphere exposed hydrogen-terminated diamond was proposed by F. Maier *et al* in 2000, the development in understanding of the interaction between atmospheric particles and the diamond surface has slowly developed with much still to be explained about this interaction [5.1]. It is however the most widely accepted theory for the p-type doping at the hydrogen-terminated diamond surface and is gaining more support such as work by V. Chakrapani *et al* who performed a detailed investigation into the redox reactions at the surface while attempting to explain issues such as how an aqueous layer adsorbs on to what is essentially a hydrophobic surface [5.2].

Meanwhile separate research has confirmed just how attractive intrinsic diamond is as an electronic material with proof of intrinsic high mobility (4500 $cm^2.V^{-1}.s^{-1}$ for electrons and 3800 $cm^2.V^{-1}.s^{-1}$ for holes) by J. Isberg *et al* encouraging further research into diamond electronics [5.3]. Significant progress has been made in the search for alternative acceptor materials to replace atmospheric particles at the diamond surface with a more stable solution. P. Strobel *et al* demonstrated from photoyield spectra in 2004 that C_{60} molecules could produce the same sub-surface p-type doping effect and fluorinating these molecules enhances their doping efficiency [5.4-5]. After annealing at 400° C, enough to remove atmospheric particles but not damage the hydrogen-termination of the diamond surface, they deposited C_{60} and $C_{60}F_{48}$ molecules. With electrical characterisation performed in-situ saw an increase in conductivity from 10^{-12} S to 10^{-6} S for C_{60} and 10^{-5} for $C_{60}F_{48}$ in the case of $C_{60}F_{48}$ they predict a 1:1 doping for each fullerene molecule with sheet hole density induced in the diamond above 10^{13} cm^{-2}.

This has led others such as W. Chen *et al* to search out other organic molecules to provide stable doping alternatives with surface transfer doping also observed using a covering of F_4-TCNQ [5.6]. D. P. Langley *et al* have demonstrated doping via a molecular heterojunction of ZnTPP and $C_{60}F_{48}$ with the ZnTPP layer acting to prevent atmospheric doping while allowing fullerene induced doping [5.7]. To the authors knowledge there has yet to be any research into inorganic surface coatings with the aim of replacing the electron accepting layer by using a dielectric with electron affinity > 4.2 eV. To date, dielectrics have only been utilised as encapsulation layers to try and preserve surface transfer doping instigated by atmospheric particles. It seems the best route forward would be to employ a high electron affinity dielectric for the purpose of electron accepting rather than purely

encapsulation as they will tend to be far more stable on the diamond surface assuming a low stress conformal film can be successfully deposited. Figure 5.1.1 shows the relative band energy levels of semiconductors and some candidate surface acceptor materials as speculated by W. Chen et al [5.6]. A preliminary investigation into alternative surface acceptor materials is presented in Chapter 7 of this thesis.

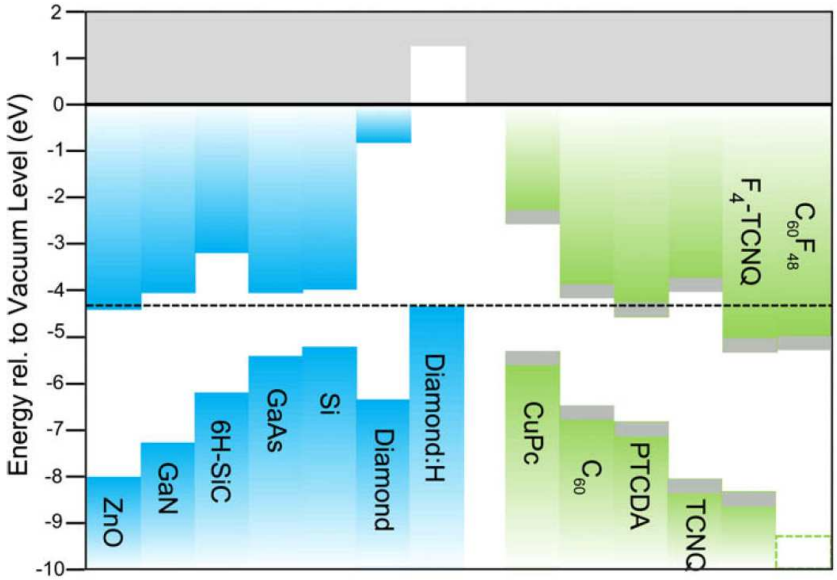


Figure 5.1.1: Relative band energies of semiconductors and various organic acceptor material candidates [5.6]

5.2 Surface Channel Diamond Transistors

It is widely accepted that minimisation of FET gate length improves its frequency performance and this is no different in diamond FETs which employ surface transfer doping. Over the past decade, diamond FET gate length has been gradually reduced from ~2.5 μm to 100 nm, with the expected enhancement in frequency performance observed. Beginning with H. Taniuchi et al in 2001 and the first reported microwave measurements using a 2-3 μm gate, an f_T of 2.2 GHz and f_{MAX} of 7 GHz was obtained from a hydrogen-terminated diamond FET [5.8]. Since this initial demonstration, two independent groups had reported the highest microwave performance to date for diamond FETs using a T-shaped gate. Firstly K. Ueda *et al* in 2006 where f_T of 45 GHz and f_{MAX} of 120 GHz were

observed for two separate MESFET devices optimised with different gate widths and gate length of 100 nm as seen in Figure 5.2.1 [5.9].

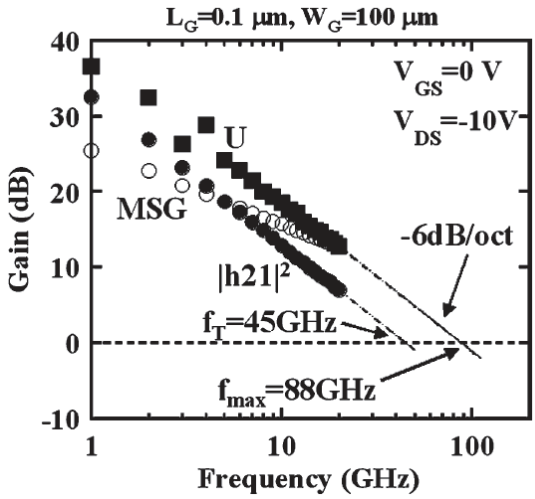


Figure 5.2.1: RF measurement for diamond MESFET [5.9]

K. Hirama *et al* replicated similar results with an experiment instead using a 3 nm dielectric layer of Al_2O_3 beneath the gate to create a MISFET device and a 150 nm gate length. Both authors used polycrystalline diamond in their respective research [5.10].

Power measurement for surface channel FETs is still in its infancy as degradation and repeatability is currently a huge challenge with this technology. However K. Hirama *et al* managed to produce 2.14 $W.mm^{-1}$ output power with a power added efficiency (PAE) of 42% from a surface channel MISFET with gate length of 300 nm and unquoted gate width operating at 1 GHz [5.10]. M. Kasu *et al* again achieved very similar results 2.1 W.mm-1 output power, maximum power gain of 10.9 dB and PAE of 31.8% from a surface channel MESFET with gate length of 100 nm and gate width of 100 μm operating at 1 GHz as shown in Figure 5.2.2 [5.11].

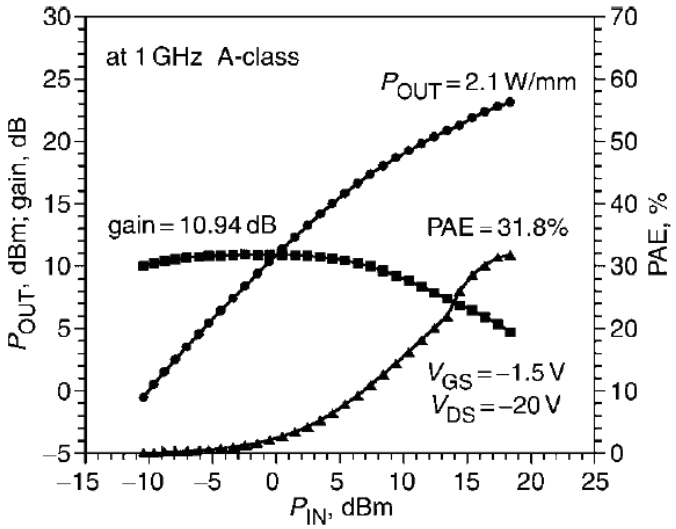


Figure 5.2.2: Power measurement for diamond MESFET [5.11]

P. Gluche *et al* have performed some preliminary investigation in to high voltage operation for a device with 3 μm gate length, 100 μm gate width and 12 μm source-drain spacing. They obtained a maximum drain-source voltage of 200 V prior to breakdown [5.12]. Other research groups have attempted power measurements of these types of devices, most notably in Italy where attempts have also been made to model the large-signal equivalent circuit although their performance is as yet not as competitive as that described above [5.13]. Prior to this project, no research has been reported on the operation of sub-100 nm diamond FETs where parasitic resistances need to be seriously considered in scaling to keep improving device performance. Results of this work are presented in the following Chapter.

As well as the search for alternative electron accepting materials effort has been made to provide passivation for the exposed region of atmospheric FET devices. Attempts to grow AlN via MOCVD on top of existing devices would seem fundamentally flawed due to the high deposition of > 800° C potentially removing the hydrogen-termination yet some success has been observed and put down to the spontaneous polarisation of AlN films instigating some charge transfer [5.14]. More success seen with atomic layer deposition (ALD), D. Kueck *et al* report maintaining 65% of the original device current from this method even with a deposition temperature of 370° C, which is high enough to remove

atmospheric adsorbates [5.15]. Other dielectrics that have been investigated as potential gate insulating materials in MISFET devices include SiO_2 and CaF, but have not yet been investigated for passivation of the active device regions exposed between source and gate and gate and drain contacts.

Makoto Kasu's research group at NTT in Japan have tried various experiments involving gas exposure of devices to individual constituents of the atmosphere. They have observed particular success when exposing devices to NO_2 gas and recently combined this process with an ALD Al_2O_3 layer recording record output current density of 1.3 $A.mm^{-1}$ from a diamond MESFET [5.16]. However the ALD deposition temperature (< 150° C) is below that at which atmospheric particles desorb from the hydrogen-terminated diamond surface, raising the issue of whether this process modifies and encapsulates the atmospheric adsorbate molecules rather than replacing them.

Hiroshi Kawarada's group at Waseda University in Japan have also attempted various other alternative fabrication procedures for surface channel diamond FETs. A recent paper describes a 'hydrogenation last' process where robust titanium carbide contacts are initially made to an oxygen-terminated diamond surface known to provide an ohmic contact which is far more strongly bonded to the diamond surface than the standard Au process [5.17]. This is followed by selective hydrogen-termination of the active regions with their standard gate process. Although this procedure is yet to produce competitive device results it is foreseeable that its refinement, possibly incorporating another electron accepting material, could be a potential route to more stable diamond FETs. They have also experimented with different crystal orientations of diamond to produce more carriers for devices theorising that more exposed dangling bonds given by a (111) surface termination gives the potential for a greater electron transfer [5.18].

Device Instability

All surface channel FETs to date have demonstrated an inherent instability with repeat measurement leading to seriously degraded drain currents. Ever since the first surface channel transistor reported by H. Kawarada *et al* in 1994 these problems have persisted with little discussion in the literature addressing these issues. In one publication it was noted that the FETs were only stable up to 200° C in air, far lower than would be hoped for with diamond technology [5.19]. M. Kubovic *et al* reported in 2002 that fabricating surface

channel FETs by conventional lift-off lithography was detrimental to the atmospheric adsorbate layer and suggested that the now widely used Au SL and etch technique has a 'slightly passivating' effect on the surface due to the KI/I_2 based etch [5.20]. Little more is known about this interaction apart from the fact is does not lead to oxygen-termination of diamond.

A thorough report investigating degradation due to repeat measurement is to the author's knowledge as yet unpublished. However there have been plenty of anecdotal mentions of this phenomenon [5.20-22]. M. Kasu *et al* investigated a device close to breakdown with source-drain voltage pushed to -100 V at which point they saw bubbles forming on their ohmic contacts. These are suggested to be hydrogen bubbles evaporating from the diamond surface due to high energy carriers breaking the C-H bond. They believe this to be the cause for premature breakdown in surface channel FETs as it is a function of the surface and not the intrinsic diamond itself. This theory is yet to garner wide scale acceptance and the debate over degradation and premature breakdown continues.

K. Hirama *et al* recently reported their Al_2O_3 encapsulation layer combined with a pre-deposition exposure to NO_2 gas is sufficient to prevent degradation due to repeat measurement in their FETs however there does still appear to be ~ 12.5% drain current degradation after 250 measurements [5.23]

Another theory is the Schottky barrier between diamond and gate metal contact is not sufficient to prevent significant gate leakage in MESFET devices hence why some groups employ MISFET devices instead [5.10]. These do not however show vastly improved performance compared to their MESFET counterparts [5.9]. Another controversial theory by J. A. Garrido *et al* suggests the gate does not in fact accumulate charge beneath it at all instead they describe an 'in-plane' capacitance at the edge of the gate contact as capacitance does not scale with gate area but with the periphery [5.24].

Although device performance is being improved upon there is still much to understand about the hydrogen-terminated diamond surface and its properties.

5.3 Boron Delta-Doped Diamond Transistors

The delta-doping of diamond with boron has been presented as a potential competitor to the hydrogen-terminated surface channel FET discussed in this project. It has the benefit of being stable due to an oxygen-terminated surface being employed and all conduction taking place within the bulk diamond. However in the FET devices fabricated so far via this method the gates ability to control the channel has been poor meaning full pinch-off is difficult to achieve [5.25].

A gate recess is a potential solution to bring the gate closer to the delta layer as seen in Figure 5.3.1.

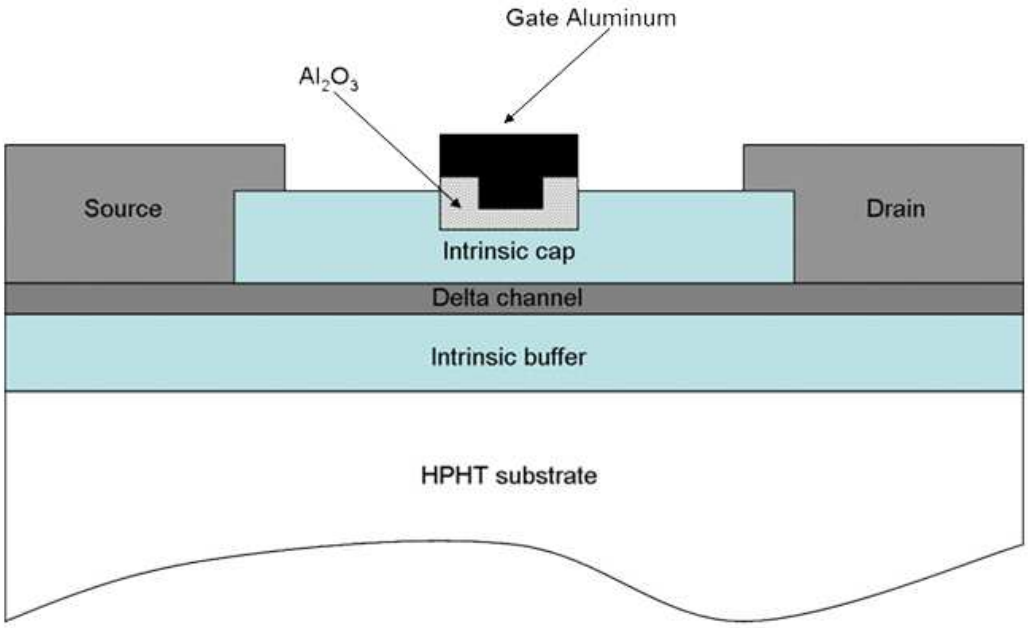


Figure 5.3.1: Boron delta-doped diamond FET design [5.25]

High power dry etches involving bombardment with large ions such as an argon plasma are required to etch diamond. This leads to damage and graphitisation of the diamond surface and give the need for another acid etch clean, so this quickly becomes a complex fabrication processes [5.26]. Even if this is all successful a dielectric is then required to prevent gate leakage and buffer leakage from residual boron doping is also an issue [5.25]. Finally there is a need for highly doped regions to create ohmic contacts and provide low

resistance access to the channel. Even with the latest structures channel mobility is still only ~20 $cm^2V^{-1}s^{-1}$ as limited by the doping profile [5.25].

5.4 Summary

This chapter has summarised the current state of diamond surface channel FET technology which although in its infancy has seen plenty of encouraging results including a vast potential of materials which could provide a route to stable devices along with some already very promising device results.

The following chapter now deals with this project's contribution to diamond FET scaling to below 100 nm gate dimensions and the improved frequency performance achieved with this study. Chapter 7 then contributes to further understanding of electron accepting materials on diamond with two alternative electron accepting materials that to the author's knowledge have not yet been investigated as a surface acceptor on diamond. These results include the first example of a potential inorganic electron accepting material.

References:

[5.1] F. Maier, M. Riedel, B. Mantel, J. Ristein, and L. Ley, "Origin of surface conductivity in diamond," *Physical Review Letters*, vol. 85, no. 16, pp. 3472-3475, 2000

[5.2] V. Chakrapani, J. C. Angus, A. B. Anderson, S. D. Wolter, B. S. Stoner and G. U. Sumanasekera, "Charge transfer equilibria between diamond and an aqueous oxygen electrochemical redox couple," *Science*, vol. 318, no. 5855, pp. 1424-1430, 2007

[5.3] J. Isberg, J. Hammersberg, E. Johansson, T. Wikström, D. J. Twitchen, A. J. Whitehead, S. E. Coe and G. E. Scarsbrook, "High carrier mobility in single-crystal plasma-deposited diamond," *Science*, vol. 297, no. 5587, pp. 1670-1672, 2002

[5.4] P. Strobel, M. Riedel, J. Ristein and L. Ley, "Surface transfer doping of diamond," *Nature*, vol. 430, no. 6998, pp. 439-441, 2004

[5.5] L. Ley, J. Ristein, F. Meier, M. Riedel and P. Strobel, "Surface conductivity of the diamond: A novel transfer doping mechanism," *Physica B*, vol. 376-377, pp. 262-267, 2006

[5.6] W. Chen, D. Qi, X. Gao and A. T. S. Wee, "Surface transfer doping of semiconductors," *Progress in Surface Science*, vol. 84, no. 9-10, pp. 279-321, 2009

[5.7] D. P. Langley, Y. Smets, C. B. Stark, M. T. Edmonds, A. Tadich, K. J. Rietwyk, A. Schenk, M. Wanke, Q. H. Wu, P. J. Barnard, L. Ley and C. I. Pakes, "Surface transfer doping of diamond with a molecular heterojunction," *Applied Physics Letters*, vol. 100, no. 3, pp. 032103-1-032103-4, 2012

[5.8] H. Taniuchi, H. Umezawa, T. Arima, M. Tachiki and H. Kawarada, "High frequency performance of diamond field-effect transistor," *IEEE Electron Device Letters*, vol. 22, no. 8, pp. 390-392, 2001

[5.9] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook and S. E. Coe, "Diamond FET using polycrystalline diamond with f_T of 45 GHz and f_{MAX} of 120 GHz," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 570-572, 2006

[5.10] K. Hirama, H. Takayanagi, Y. Yamauchi, Y. Jingu, H. Umezawa and H. Kawarada, "High-performance p-channel diamond MOSFETs with alumina gate insulator," *IEDM Technical Digest*, pp. 873–876, 2007

[5.11] M. Kasu, K. Ueda, H. Ye, Y. Yamauchi, S. Sasaki and T, Makimoto, "2 W/mm output power density at 1 GHz for diamond FETs," *Electronics Letters*, vol. 41, no. 22, pp. 1249-1250, 2005

[5.12] P. Gluche, A. Aleksov, A. Vescan, W. Ebert and E. Kohn, "Diamond surface-channel FET structure with 200 V breakdown voltage," *IEEE Electron Device Letters*, vol. 18, no. 11, pp. 547-549, 1997

[5.13] V. Camarchia, F. Cappelluti, G. Ghione, M. Pirola, G. Conte, B. Pasciuto, E. Limit and E. Giovine, "Accurate large-signal equivalent circuit of surface channel diamond FETs based on the Chalmers model," *Diamond and Related Materials*, vol. 26, pp. 15-19, 2012

[5.14] D. Kueck, J. Scharpf, W. Ebert, M. Fikry, F. Scholz and E. Kohn, "Passivation of H-terminated diamond with MOCVD-aluminium nitride – a key to understand and stabilize its surface conductivity," *Physica Status Solidi (a)*, vol. 207, no. 9, pp. 2035-2039, 2010

[5.15] D. Kueck, P. Leber, A. Schmidt, G. Speranza and E. Kohn, "AlN as passivation for surface channel FETs on H-terminated diamond," *Diamond and Related Materials*, vol. 19, no. 7-9, pp. 932-935, 2010

[5.16] K. Hirama, H. Sato, Y. Harada, H. Yamamoto and M. Kasu, "Diamond field-effect transistors with 1.3 A/mm drain current density by Al_2O_3 passivation layer," *Japanese Journal of Applied Physics*, vol. 51, no. 9, pp. 090112-1-090112-5, 2012

[5.17] Y. Jingu, K. Hirama and H. Kawarada, "Ultrashallow TiC source/drain contacts in diamond MOSFETs formed by hydrogenation-last approach," *IEEE Transactions on Electron Devices*, vol. 57, no. 5, pp. 966-972, 2010

[5.18] K. Hirama, K, Tsuge, S. Sato, T. Tsuno, Y. Jingu, S. Yamauchi and H. Kawarada, “High-performance p-channel diamond metal-oxide-semiconductor field-effect transistors on H-terminated (111) surface,” *Applied Physics Express*, vol. 3, no. 4, pp. 044001-1-044001-3, 2010

[5.19] H. Kawarada, M. Aoki and M. Ito, “Enhancement mode metal-semiconductor field effect transistors using homoepitaxial diamonds,” *Applied Physics Letters*, vol. 65, no. 12, pp. 1563-1565, 1994

[5.20] M. Kubovic, A. Aleksov, A. Denisenko and E. Kohn, “Advances in diamond surface channel FET technology with focus on large signal properties,” *Proceedings of IEEE Lester Eastman Conference on High Performance Devices*, pp. 90-99, 2002

[5.21] A. Aleksov, M. Kubovic, M. Kasu, P. Schmid, D. Grobe, S. Ertl, M. Schreck, B. Stritzker and E. Kohn, “Diamond-based electronics for RF applications,” *Diamond and Related Materials*, vol. 13, no. 2, pp. 233-240, 2004

[5.22] M. Kasu, K. Ueda, Y. Yamauchi, A. Tallaire and T. Makimoto, “Diamond-based RF power transistors: Fundamentals and applications,” *Diamond and Related Materials*, vol. 16, no. 4-7, pp. 1010-1015, 2007

[5.23] M. Kasu, H. Sato and K. Hirama, “Thermal stabilization of hole channel on H-terminated diamond surface by using atomic-layer-deposited Al_2O_3 overlayer and its electric properties,” *Applied Physics Express*, vol. 5, pp. 025701-1-025701-3, 2012

[5.24] J. A. Garrido, C. E. Nebel and M. Stutzmann, “Capacitance-voltage studies of Al-Schottky contacts on hydrogen-terminated diamond,” Applied Physics Letters, vol. 81, no. 4, pp. 637-639, 2002

[5.25] H. El-Hajj, A. Denisenko, A. Kaiser, R. S. Balmer and E. Kohn, “Diamond MISFET based on boron delta-doped channel,” *Diamond and Related Materials*, vol. 17, no’s. 7-10, pp. 1259-1263, July-October 2008

[5.26] A. Denisenko, A. Romanyuk, C. Pietzka, J. Scharpf and E. Kohn, “Surface damages in diamond by Ar/O_2 plasma and their effect on the electrical and electrochemical characteristics of boron-doped layers,” *Journal of Applied Physics*, vol. 108, pp. 074901-1-074901-7, 2010

6. Device Results - Scaling Diamond FETs to Sub-100 nm Gate Length

Previous chapters have outlined the basics of FET operation while showing how important scaling the physical dimensions of the gate can be in relation to improving the intrinsic performance of a device. The current technology review chapter discussed how various groups have already worked to reduce the dimensions of diamond FET gate lengths to sub-micron dimensions with significant success but as yet no research has been published on sub-100 nm gate length devices. This chapter details work done throughout this project with this goal in mind.

Prior chapters have also shown it is sensible to isolate the individual components comprising the FET to assess and improve these individually before combining them to make a device. So this chapter begins with the analysis of basic material and contact properties from VDP, TLM and CV measurements. Then moving on to DC and RF characterisation of RF FET structures with gate lengths of 250, 150 and 50 nm to produce a full picture of the effects of scaling on diamond FETs and the potential limiting factors involved in terms of their operation and peak performance.

Finally there is a brief investigation in to the effect of measurement and how it can lead to degradation of the drain current in a surface channel FET and what may be the underlying cause of this phenomenon.

6.1 VDP and TLM Measurements

Several single crystal and polycrystalline diamond samples were used throughout the course of this research all of which were sourced from Element Six Ltd and Diamond Microwave Devices Ltd. Hydrogen-termination procedures on the other hand evolved over the course of this research to produce cleaner, more repeatable and improved processes at several facilities outside of Glasgow.

To begin with, experimental work was undertaken using polycrystalline samples as they are slightly larger (10 x 10 mm) compared to the single crystal (4.7 x 4.7 mm) and hence are easier to handle and process, along with having more space on each sample to create structures. The vast majority of surface channel FET devices reported to date have been fabricated on polycrystalline material so it is also a useful comparison to have.

To assess material quality, VDP measurements were performed on the electron beam defined structures described in Section 4.1 with Table 6.1.1 showing a comparison between an early polycrystalline sample at the beginning of the hydrogen-termination process development and the single crystal material used later to fabricate RF devices.

	Early Polycrystalline Sample	**Single Crystal Sample Used for Device Fabrication**
Carrier Concentration (cm^{-2})	5.51×10^{11}	5.55×10^{12}
Sheet Resistance (kΩ/□)	46.7	11.3
Mobility ($cm^2.V^{-1}.s^{-1}$)	211	90

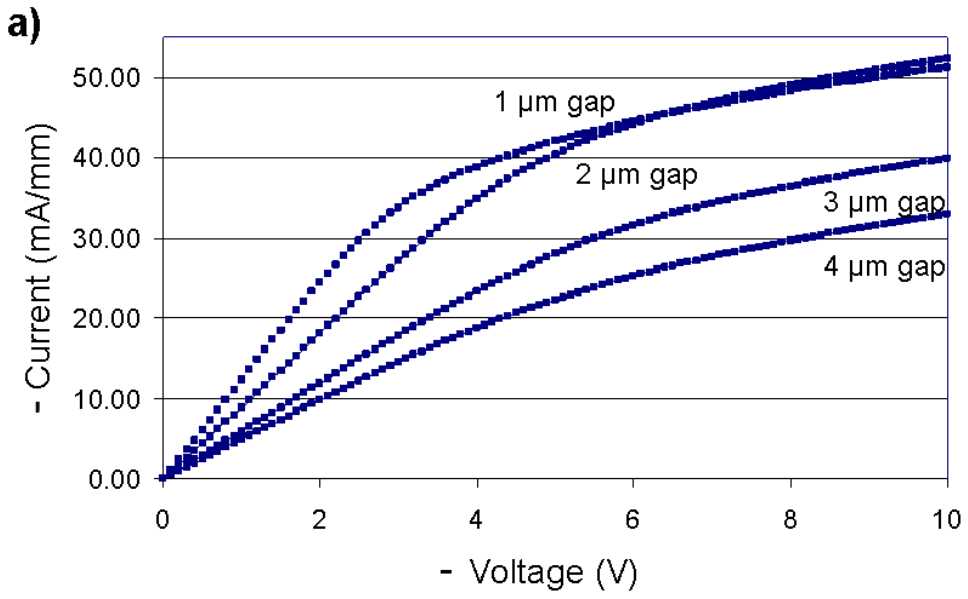
Table 6.1.1: Comparison of VDP measurement

It is clear these values differ greatly and there are two possible explanations for this. Firstly the difference in quality between polycrystalline and single crystal diamond. The grain boundaries present in the polycrystalline material may perhaps impede the charge transport although this does not fit with the results seen here since mobility is in fact higher on the polycrystalline sample. There have also been previous reports of VDP measurements on diamond which are comparable to those obtained on the single crystal sample here [6.1]. Instead it is speculated that the difference observed here is due to the hydrogen-termination

procedure. The values for the single crystal sample are close to what has been previously reported with perhaps just a slightly low value for the sheet carrier concentration.

The hydrogen-termination for the early experimental work undertaken here was performed in an old hot filament system at Heriot-Watt University which has been used for many different experiments including doping with boron which is known to contaminate chambers and be extremely difficult to remove hence subsequently contaminating other substrates [6.2]. The sheet carrier concentration is an order of magnitude lower than may be expected. This would suggest possible contamination of the hydrogen-terminated diamond surface with impurities which impede the surface transfer doping mechanism, giving less active carriers and also leading to a higher sheet resistance. The mobility is higher than anticipated which may be explained by less scattering mechanisms present, for example if the surface transfer doping mechanism is impeded the charge may not be drawn as close to the surface as would normally be the case.

TLM measurements were then performed to confirm the sheet resistance seen in VDP measurements and to also obtain the contact resistance between the Au ohmic metal and diamond. This was undertaken on electron beam defined structures as described in Section 4.2. Figure 6.1.1 shows current voltage sweeps for four separate TLM gaps on the polycrystalline sample along with an average graph combining four TLM structures.



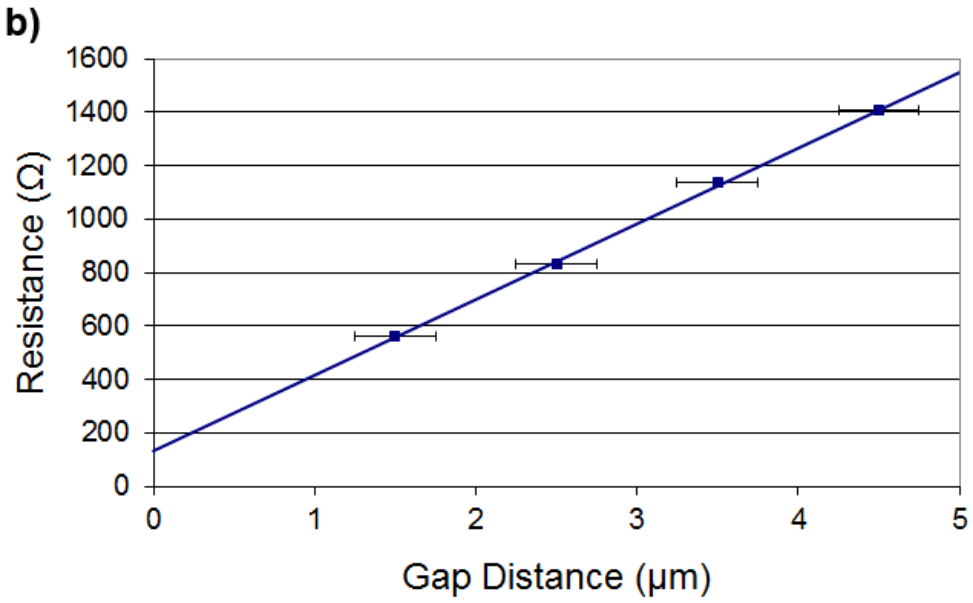


Figure 6.1.1: a) TLM measurements for polycrystalline sample with possible boron contamination, b) average graph

The sweeps were performed between 0 and -10 V with the individual sweeps not quite saturating before the -10 V final measurement value. It is important to only extract the resistance where the current-voltage plot is linear and hence ohmic prior to saturation. The gradient of each sweep up to -3 V gives resistance which is averaged over four TLM structures to give the average plot. It is important to note that even though the gaps are designed to be 1, 2, 3 and 4 μm respectively this is not actually the real physical separation as previously mentioned in section 4.2 so before plotting the resistance against gap distance it is crucial to observe the structures under the SEM. Even for a short 1 minute Au etch used as standard there can be significant variation in etch distances between samples, especially for larger gaps. E.g. the 4 μm polycrystalline sample is actually ~ 4.5 μm whereas on the single crystal sample the gap is actually ~ 5.5 μm.

The TLM plots for the single crystal sample can be seen in Figure 6.1.2. This hydrogen-termination procedure took place at Université Paris 13, it involved a pre-clean with H_2SO_4/HNO_3 to remove any graphitic contaminants on the diamond surface as well as leaving it oxygen-terminated. Subsequently the sample was loaded in to a CVD reactor and exposed to high power hydrogen plasma for 30 minutes at 580° C.

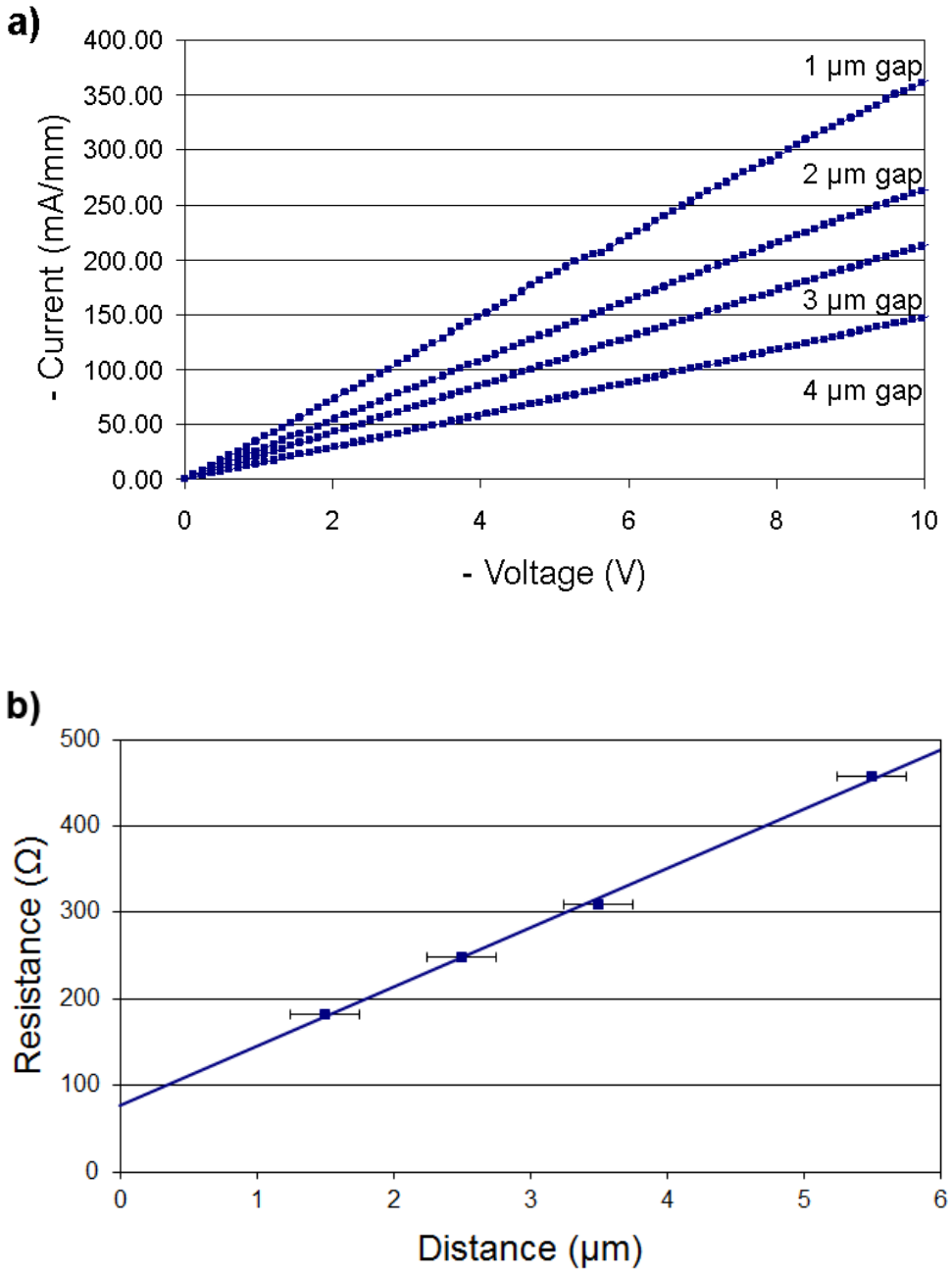


Figure 6.1.2: a) TLM measurements for single crystal sample with hydrogen-termination used later in the project, b) average graph

From observing the plots we see an order of magnitude difference in carrier concentration between the two samples gives rise to a much larger current in the TLM structure on the single crystal sample. For the single crystal sample the TLM sweeps have not fully

saturated by -10 V but it is still a sufficient range to obtain an average TLM plot as shown. The error in resistance measurement is relatively low as long as the gradient of the plots is averaged over a wide range of linear behaviour and over several TLM structures. This can be attributed to errors in the measurement apparatus and is small enough that the error bars are not visible on the average TLM plot. The error in gap distance however is a different matter. As can be seen in Figure 6.1.3 the actual ohmic contact edge can be difficult to define. In this instance the variation can be said to be ~ 250 nm. This introduces an error of 500 nm in the ohmic contact spacing. The extracted TLM results are summarised in Table 6.1.2.

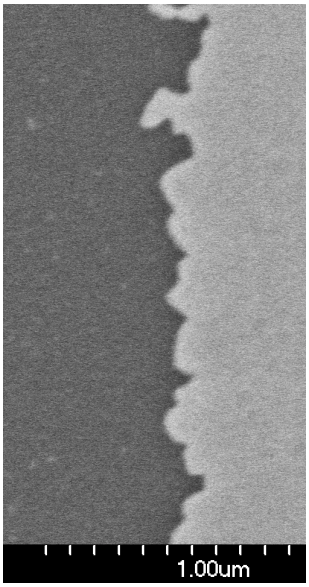


Figure 6.1.3: Ohmic contact edge roughness due to Au etch

	Polycrystalline Sample	**Single Crystal**
Contact Resistance (Ω.mm)	10.1 (± 5.3)	5.7 (± 1.3)
Sheet Resistance (kΩ/□)	42.5 (± 6.0)	10.3 (± 2.0)

Table 6.1.2: Comparison of TLM measurement

The 42.5 kΩ/□ value for sheet resistance for the polycrystalline sample agrees within error with the value obtained from Hall measurement. As does 10.3 kΩ/□ for the single crystal sample. The margin for error is more significant in terms of contact resistance as the large

error in gap distance (the x-axis) will significantly shift the y-intercept whereas the gradient is not as substantially affected. A sheet resistance of 10.3 kΩ/□ is comparable to sheet resistances obtained by other groups [6.3] while 42.5 kΩ/□ again suggests an un-optimised hydrogen-termination procedure.

As for contact resistance, 5.70 Ω.mm is perhaps a little high but still comparable to work done by other groups [6.3] and although both sheet and contact resistance are very high compared to a more mature material technology such as silicon, competitive device performance has still been achieved with similar values and work can be undertaken to improve this although it is not currently a priority.

The hydrogen-termination process successfully employed for the single crystal sample was then used for all subsequent samples to obtain a good quality sub-surface hole accumulation layer for device fabrication. Also due to a lack of polycrystalline material as well as an interest to produce FETs on single crystal material to compare the performance, the rest of this work involves single crystal diamond.

6.2 CV Results

Following material quality analysis by VDP and having achieved a competitive ohmic contact resistance it was important to analyse the gate contact employed by the FET device. This was done using CV measurement as discussed in Section 4.3 with electron beam defined diode structures as discussed previously. These measurements took place on a single crystal sample.

Sweeps can be performed at a range of frequencies to show data relating to trapping at the surface which while interesting would be difficult to discern correctly from just this measurement as the knowledge of the surface transfer doping process is still in its infancy. Here data for just 1 MHz is presented at which traps should be less noticeable due to the charge being shifted faster so some basic information about the sub-surface hole accumulation layer may be deciphered. Sweeping the voltage across the gate from +2 to -4 V allows for both depletion and accumulation beneath the gate contact, with sweep performed in both directions to show any hysteresis. The results can be seen in Figure 6.2.1.

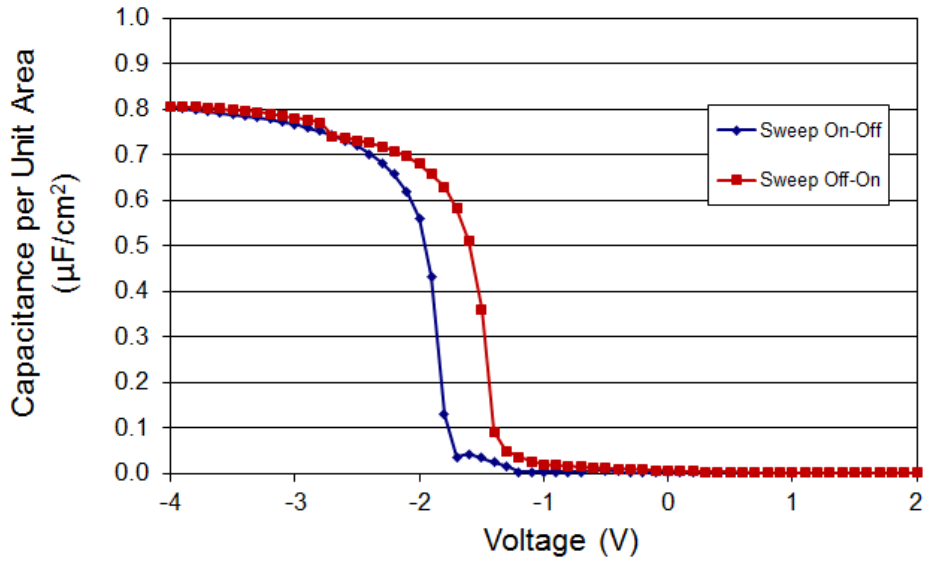


Figure 6.2.1: CV sweep at 1 MHz on single crystal diamond sample

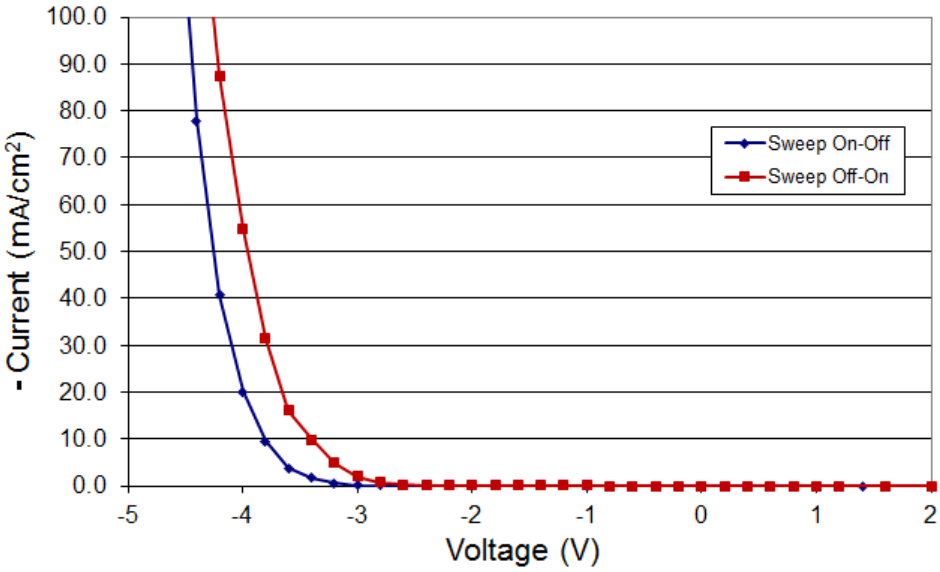


Figure 6.2.2: IV sweep for gate contact

The sweep shows clear accumulation underneath the gate which tends to disagree with the theory of in-plane capacitance suggested by J. A. Garrido *et al.* The saturated capacitance extracted from the graph can be related to a parallel plate capacitor to get an idea of how deep the sub-surface hole layer is below the diamond surface [6.4].

The parallel plate capacitor equation is as follows:

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \qquad \textbf{6.2.1}$$

Where C represents the capacitance, ε_r the relative dielectric constant of the medium between the parallel plates, ε_0 the permittivity of free space, A the area of the parallel plates and d the distance between the plates. The dielectric constant for diamond is known to be 5.7 while the permittivity of free space is 8.85 x 10^{-12} $F.m^{-1}$. The radius of the fabricated gate contact is 50 μm giving a plate area of 7855 μm^2 (± 157). Extracting the capacitance per unit area from the graph in Figure 6.2.1 which saturates at ~ 0.8 $\mu F.cm^{-2}$ and then dividing the relative permittivity by this should yield the spacing between gate contact and hole accumulation layer (which acts as the second plate) in the diamond.

The distance in this instance is found to be 6.31 nm which seems to fit with the figure generally quoted of 5 - 15 nm although there are several factors which may introduce error into this result [6.3, 6.5]. The area of the gate contact is unlikely to be exact especially as the contact is aluminium which readily oxidizes upon exposure to the atmosphere so the effective area of the gate contact may be reduced. With the area of the gate contact being large in relation to possible nanometre scale oxidation around the edge however, this should not have a large impact upon the overall gate area. It is also possible and has been speculated by M. Kasu *et al* that upon Al deposition on to an atmospherically surface transfer doped diamond surface a thin intermediate layer may form [6.6]. This is most likely a form of aluminium oxide formed at the diamond surface. If indeed this is the case then ε_r may become significantly different.

The current-voltage sweep shown in Figure 6.2.2 gives an insight into gate leakage through the Al gate contact which acts as a Schottky diode structure due to the Al forming a Schottky contact to hydrogen-terminated diamond. Current through the structure is negligible up to ~ -4 V (in both sweep directions) although beyond this current readily flows and increases rapidly. It should be noted that this will not be identical for FET gates as they are used to modulate the current between source and drain rather than purely for accumulation. It does however give an insight into the behaviour of this gate metallisation on hydrogen-terminated diamond.

6.3 Original 150nm DC Transistor Measurement and 50 nm Gate Length Realisation

Although the polycrystalline material was shown to be less suitable for high quality device performance, it still proved a useful starting point for developing the fabrication procedures previously discussed on a relatively large area substrate. As seen in Section 6.1, although the current achieved is comparatively low with few carriers there are still enough to create a functioning device. This substrate also proved useful in scaling the fabrication procedures for the gate contact down to 50 nm. Before scaling, an array of forty DC designed FETs (as seen in Section 4.4) with 150 nm gate lengths were fabricated to assess yield as well as device performance. The yield of working FETs i.e. produced a drain current in the region of hundreds of mA and containing a gate capable of modulating this current worked out to be ~ 50% and presented in Figure 6.3.1 is the output characteristics for one of these devices.

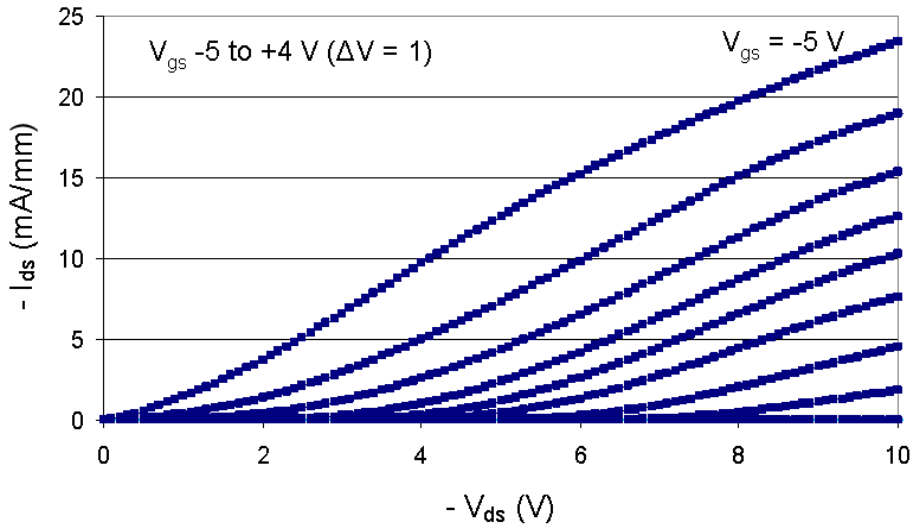


Figure 6.3.1: Output characteristics for 150 nm L_g FET

Each device is characterised over a range of drain (0 to -10 V) and gate (-5 to +4 V) voltages and exhibits transistor behaviour in as much as the gate contact is able to control the amount of current between source and drain contacts and the device can be fully pinched off at V_{gs} = +3 V. The device never fully saturates within this voltage range which would suggest a large value for R_{ON}. This agrees with the results previously seen in

Section 6.1 where the TLM structures showed large values for sheet and contact resistance speculated to be due to sample contamination.

Looking next at the transfer characteristics as shown in Figure 6.3.2, there are a few points worth noting. The threshold voltage is not clear from the plot of transfer characteristics it appears to change with V_{ds}. It is also important to note that the total drain current found at V_{gs} = -5 V and V_{ds} = - 10 V which reaches only -13 mA.mm^{-1}. This is less than two thirds of the original current measured at the same bias points for the I_{ds}-V_{ds} measurement and suggests significant drain current degradation for repeat measurement.

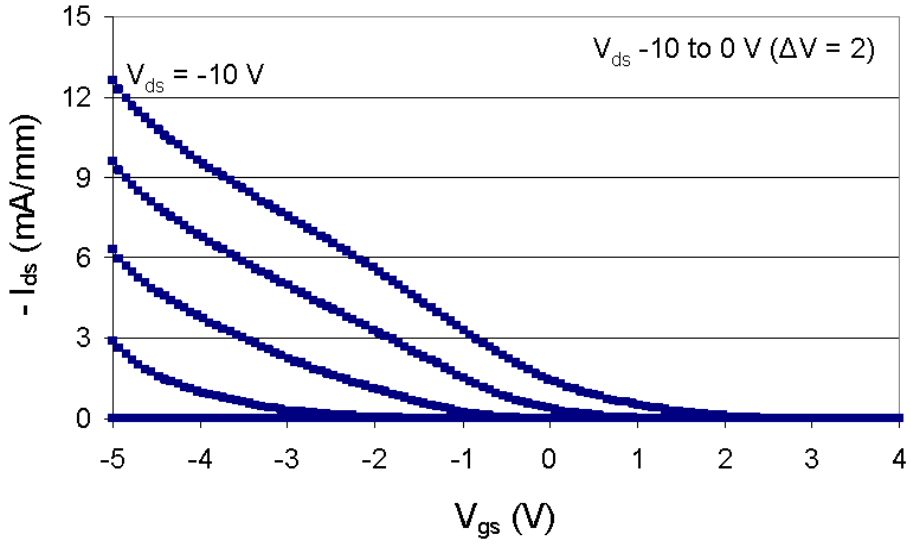


Figure 6.3.2: Transfer characteristics for 150 nm L_g FET

Figure 6.3.3 shows a transconductance plot for varying gate and drain voltages which as may be expected presents low values with peak transconductance of 5 mS.mm^{-1} at V_{gs} = -5 V and V_{ds} = -10 V although it is not saturated and appears as if it is still increasing beyond these bias points so further measurements were taken to attempt to push this value higher.

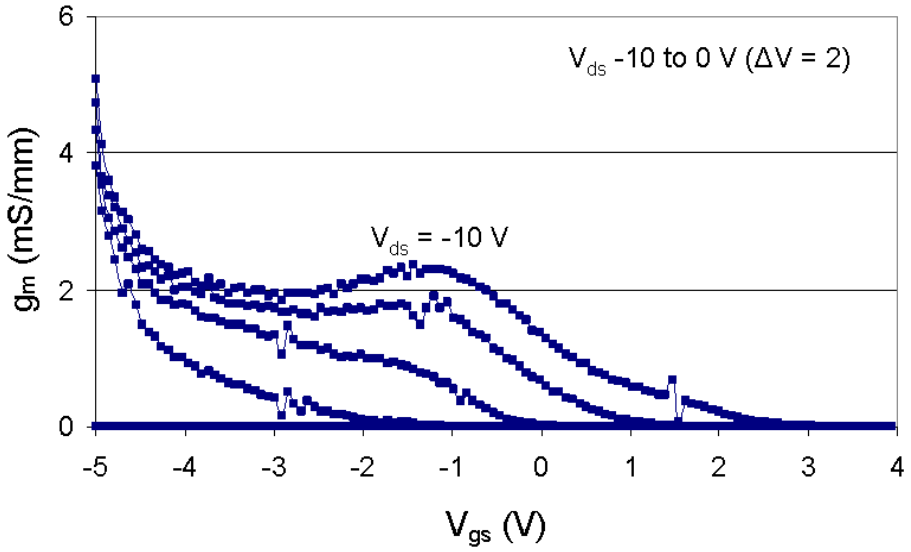


Figure 6.3.3: Transconductance plot for 150 nm L_g FET

Figure 6.3.4 shows the FET re-measured but pushed to a V_{ds} of -20 V and the device still does not quite saturate. The current now reached -27 mA.mm^{-1} for V_{gs} = -5 V although at V_{ds} = -10 V it remains degraded at -13 mA.mm^{-1}.

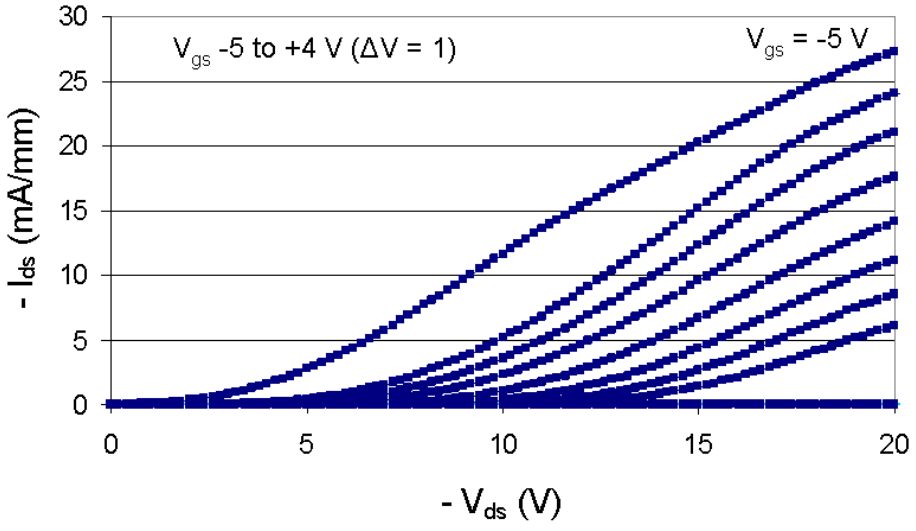


Figure 6.3.4: Output characteristics for 150 nm L_g FET up to 20 V V_{ds}

Pushing V_{gs} higher lead to failure in the device gate so if transconductance could be increased it is not physically possible to reach in this device. Although the measurement of these 150 nm gate length devices did not yield the best performance in comparison with that reported elsewhere, they do demonstrate the viability of the fabrication procedure so the rest of the polycrystalline material was then used for 50 nm gate realisation. This involved the use of a much thinner resist and higher electron beam dose for pattern definition with the full details of the process being stated in Appendix A.

As has previously been discussed, the fabrication procedure contains various elements such as the Au etch procedure that are difficult to control and are inherently low yield. A combination of repeat experiments with tweaks to the procedure eventually yielded working 50 nm gate length FETs but several generations of devices were required to reach this point.

Figure 6.3.5 shows an early experiment with the Au etch recipe demonstrating the unreliable nature of this process. Of the two separate etches performed (isolation first around the active area of the device then etching of the source-drain gap prior to gate deposition) the procedure and etch time is kept constant yet producing radically different results. For a reason that wasn't fully determined the isolation etch has only partially removed the Au metal leaving the devices with poor isolation.

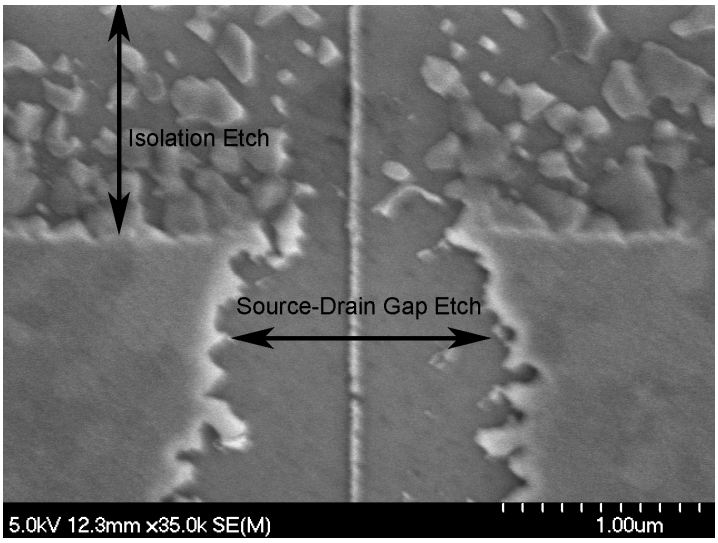


Figure 6.3.5: SEM image showing poor isolation from Au etch

Another pitfall in this process can be seen in Figure 6.3.6 where residue can be clearly seen within the source-drain gap thought to be re-deposited by the Au etch solution. To try and minimise this effect subsequent etches employed a rigorous 1 minute rinse in RO water along with sample agitation. The extra care in rinsing is necessary due to the Au etch solution doing most of its work beneath the undercut of the resist layer as shown in Figure 6.3.7, hence a quick rinse is not sufficient to remove all the Au etch solution.

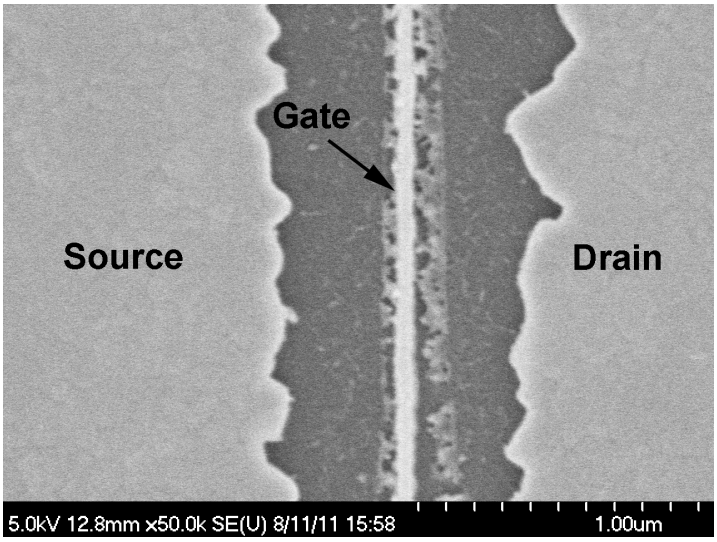


Figure 6.3.6: SEM image showing re-deposition of Au from etchings solution

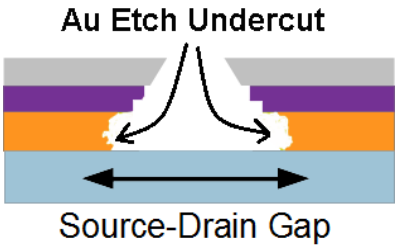


Figure 6.3.7: Au etch producing an undercut profile

Figure 6.3.8 shows that even when thoroughly rinsed and the etch residue removed as much as possible, other factors may still impede the etch. Two things should be noted from this image. Firstly the ohmic contact edge is particularly rough and secondly the gate is patchy and not fully deposited. It is believed that this is related to poor development of the

gate resist profile hence impeding the effectiveness of the Au etch with residue in the gate region and also producing a poor lift off profile for the gate contact.

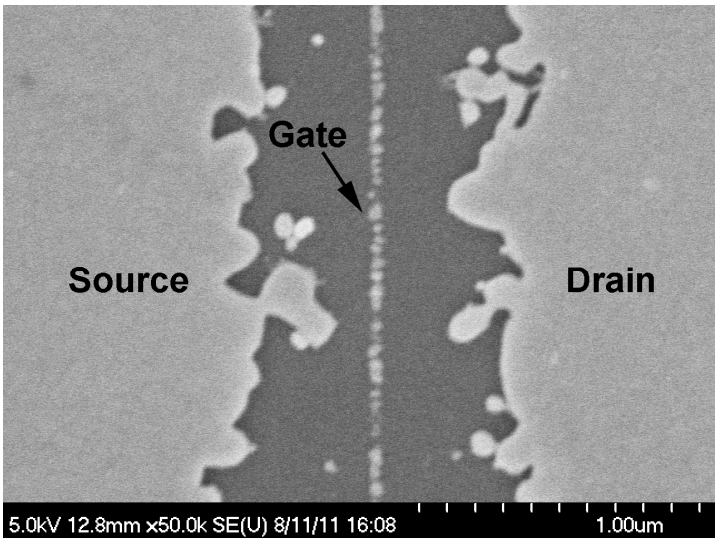


Figure 6.3.8: SEM image showing poor Au etch due to poor resist development

Figure 6.3.9 shows that even with a thorough rinse and reasonable Au etch profile the very nature of the small gate contact can cause problems with lift-off of the gate metals. Although the gate is complete it can be seen the Au metal appears poorly adhered to the underlying Al with parts clearly flaking off.

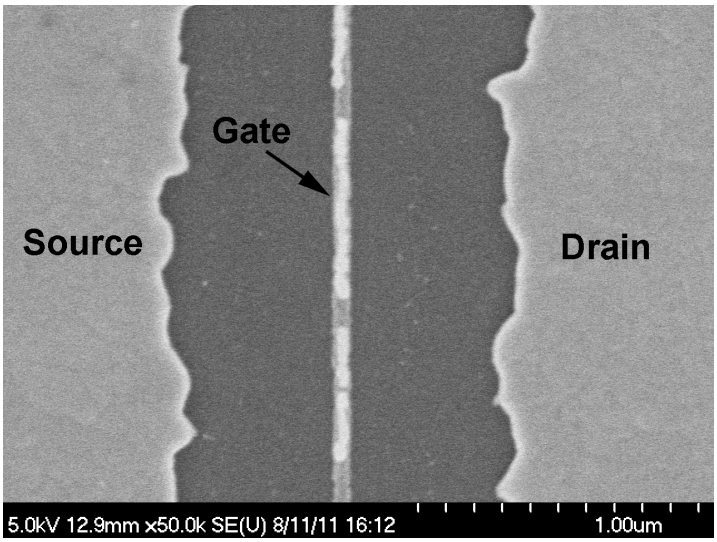


Figure 6.3.9: SEM image showing poor gate metal adhesion

Finally Figure 6.3.10 shows when the procedure is successful with a 50 nm gate length FET produced.

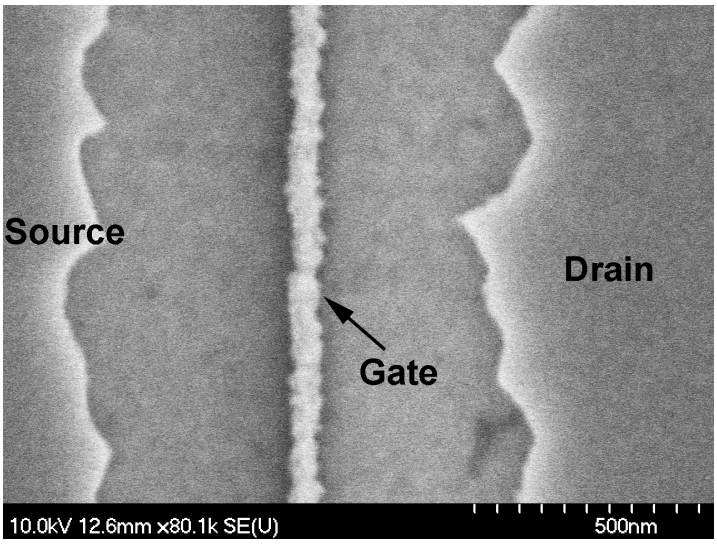


Figure 6.3.10: SEM image of 50 nm gate

6.4 DC Measurement for 250, 120 and 50nm Devices

With a sufficiently optimised hydrogenation process achieved and an improved lithography procedure allowing for gate feature definition down to at least 50 nm (as seen in Figure 6.3.5) research then shifted to producing high performance devices. To give a comparison to previous work and also a deeper insight in to the scaling of these devices three gate nodes were investigated with gate lengths of 250, 120 and 50 nm. All these devices were fabricated on the same single crystal sample to maintain continuity between the material properties for each device. This sample had the same hydrogenation procedure applied to it as the single crystal sample in Section 6.1 and hence possessed very similar material properties. Each device was designed to have two gate fingers each with a width of 25 μm to give a total device gate width of 50 μm.

First the 250 nm gate length devices are discussed, an SEM image of one can be seen in Figure 6.4.1. The DC output characteristics are shown in Figure 6.4.2 and transfer characteristics in Figure 6.4.3 with a transconductance plot for this device given in Figure 6.4.4.

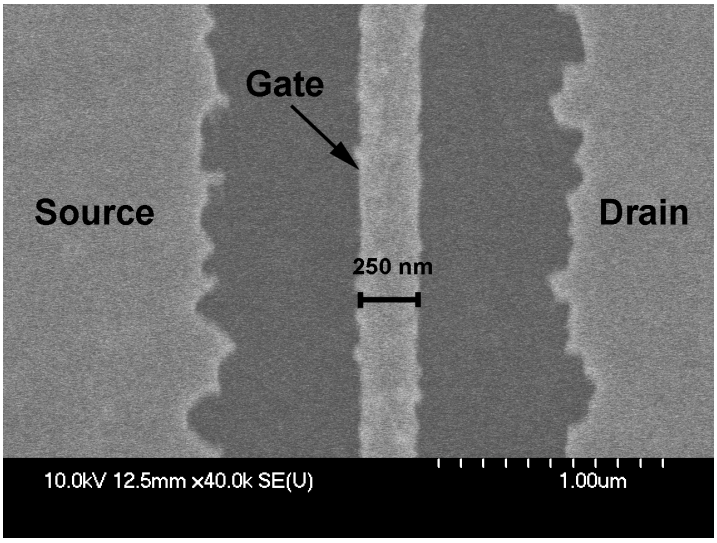


Figure 6.4.1: SEM of 250 nm FET

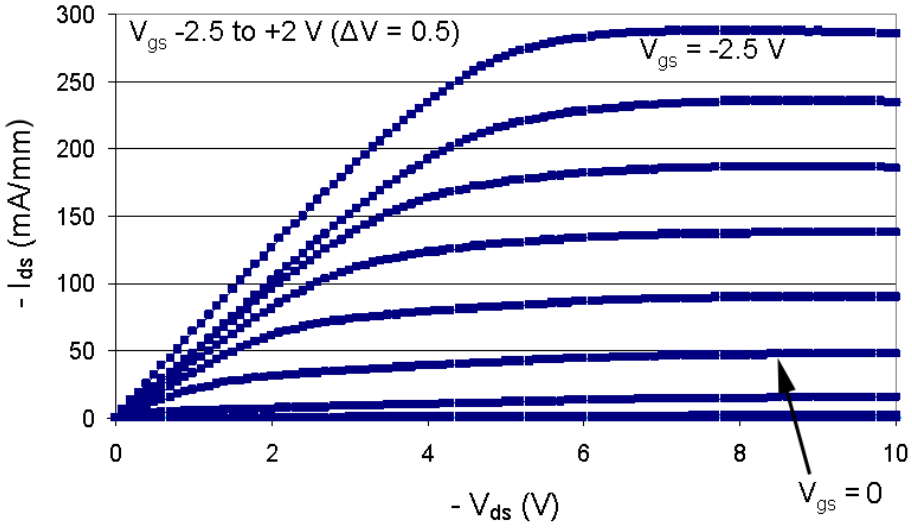


Figure 6.4.2: Output characteristics for 250 nm L_g FET

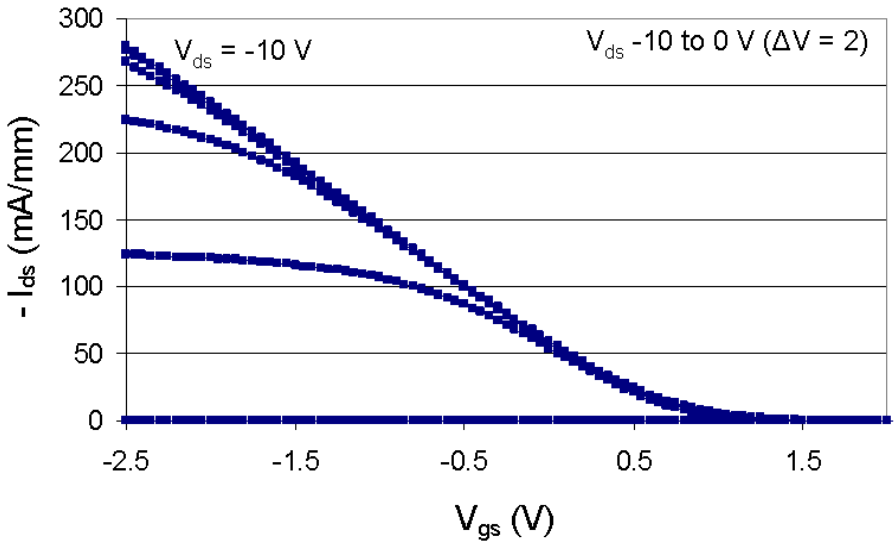


Figure 6.4.3: Transfer characteristics for 250 nm L_g FET

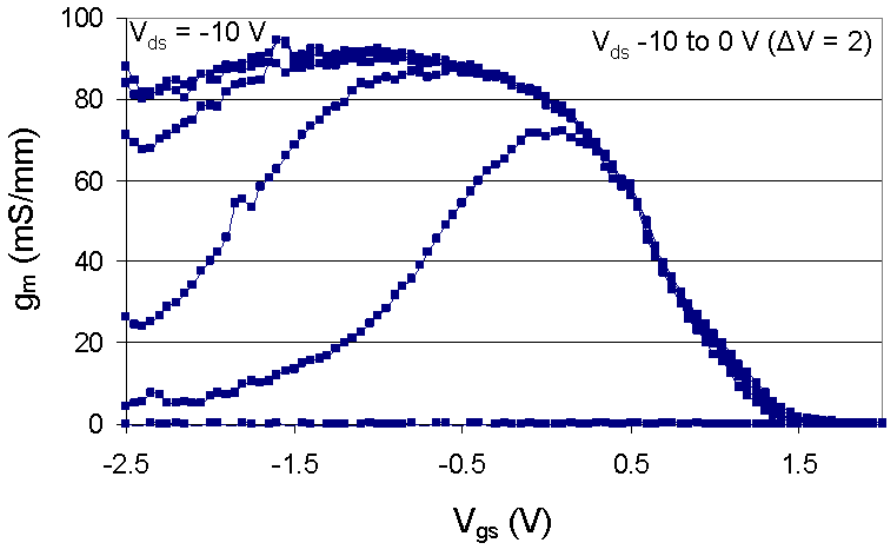


Figure 6.4.4: Transconductance plot for 250 nm L_g FET

The output characteristics at this gate length fully saturate at around V_{ds} = -5 V so although this still represents a substantial R_{ON} it is reasonable for this technology and a vast improvement on the preliminary devices seen in Section 6.3. The drain current saturates at

-280 mA.mm^{-1} for a gate voltage of -2.5 V and the device channel becomes depleted of carriers to the point there is negligible current present at a V_{gs} of +1 V. The gate voltage was not pushed to beyond -2.5 V due to concerns over drain current degradation and looking at the next measurement of the transfer characteristics this seems to have sustained the same saturation current confirming that a high gate voltage is intimately related to this phenomenon. Extracting linearly from the transfer characteristics graph the threshold voltage for this device is at V_{gs} ~ +0.75 V with a peak transconductance extracted from Figure 6.4.4 of 92 mS.mm^{-1} with a plateau between a V_{ds} of -7 and -10 V and a V_{gs} of -1 to -2 V.

The gate leakage observed in this device was so small that it was below the noise floor of the measurement system. It can be seen plotted in Figure 6.4.5 on a logarithmic scale.

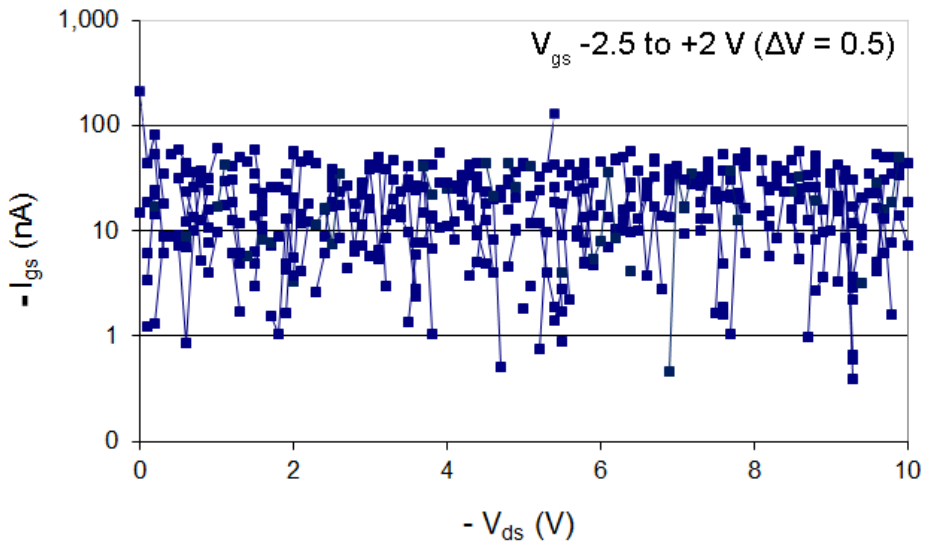


Figure 6.4.5: Gate leakage plot for 250 nm L_g FET

Moving on to the 120 nm gate length device as seen in Figure 6.4.6 with the plot of output characteristics in Figure 6.4.7, transfer characteristics in Figure 6.4.8 and transconductance displayed in Figure 6.4.9.

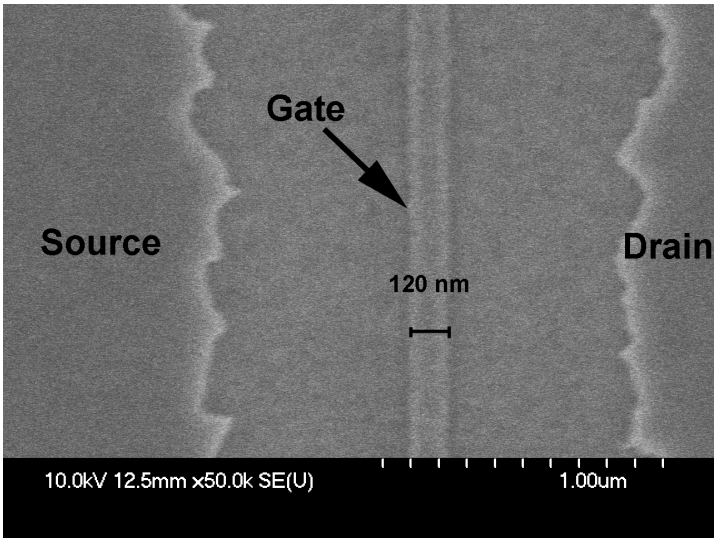


Figure 6.4.6: SEM of 120 nm FET

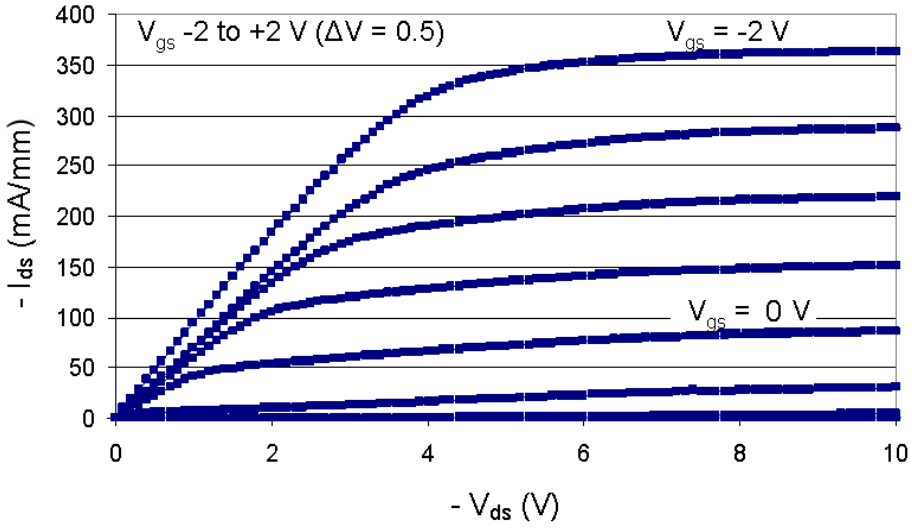


Figure 6.4.7: Output characteristics for 120 nm L_g FET

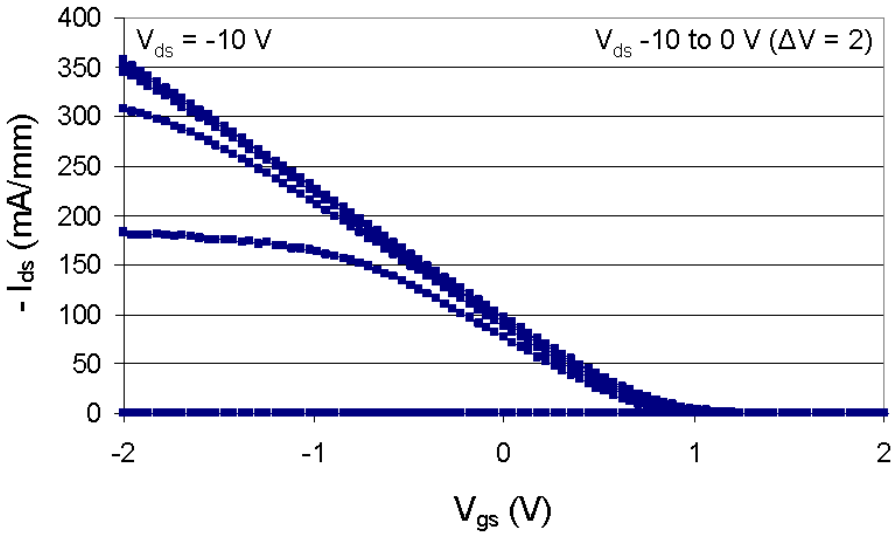


Figure 6.4.8: Transfer characteristics for 120 nm L_g FET

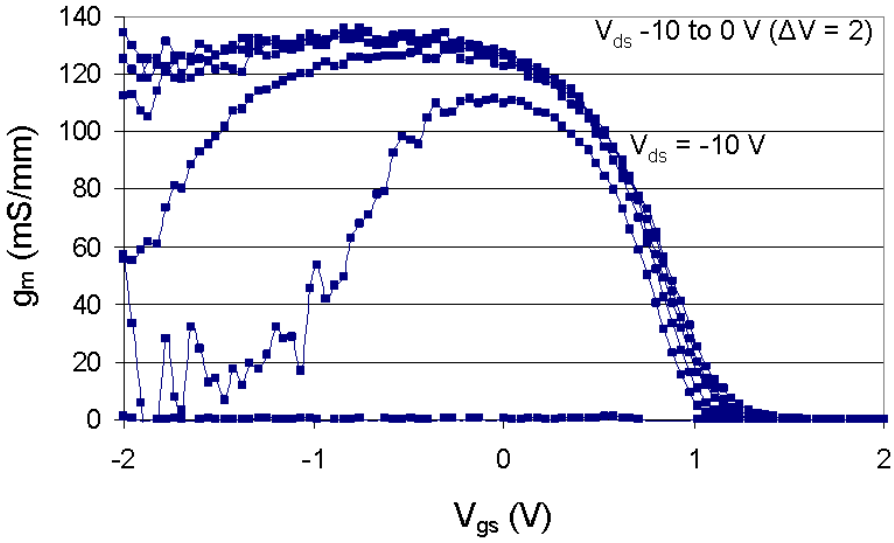


Figure 6.4.9: Transconductance plot for 120 nm L_g FET

To again try and maintain the drain current with minimal degradation care was taken to not apply too high a negative gate voltage to the device. This is because degradation appears to occur when charge is brought close to the surface. This time V_{gs} was taken between -2 and + 2 V with 0.5 V intervals and again the device becomes depleted of carriers so as to give

no substantial current at around V_{gs} = +1 V. Saturation appears to occur at reduced V_{ds} than for the 250 nm L_g FET which would suggest a slightly lower R_{ON} most likely attributed to a smaller source-drain gap from the variable Au etch. The two SEM plots images (Figure 6.4.1 and 6.4.5) however show similar spacing although the 120 nm device has marginally smoother ohmic contact edges. The maximum drain current here is higher than the 250 nm gate length device, reaching -360 mA.mm^{-1} at V_{gs} = -2 V. The transfer characteristics seen in Figure 6.4.7 confirm the threshold voltage again to be at V_{gs} ~ +0.75 V and again maintaining the same maximum drain current as from the output characteristics measurement. A peak transconductance of 137 mS.mm^{-1} is extracted from Figure 6.4.6 and again the transconductance plateaus between V_{ds} of -7 and -10 V with V_{gs} between -0.5 and -1.5 V.

Again the gate leakage observed in this device was below the noise floor of the measurement system.

Finally the 50 nm gate length FET was characterised (the device is shown previously in Figure 6.3.10). The output characteristics are shown in Figure 6.4.10, transfer characteristics in Figure 6.4.11 and transconductance in Figure 6.4.12. Extra care was once again taken to not push the gate voltage too high in the negative direction initially, hence due to the reduced gate length measurements were only taken between V_{gs} of -1 and +2 V.

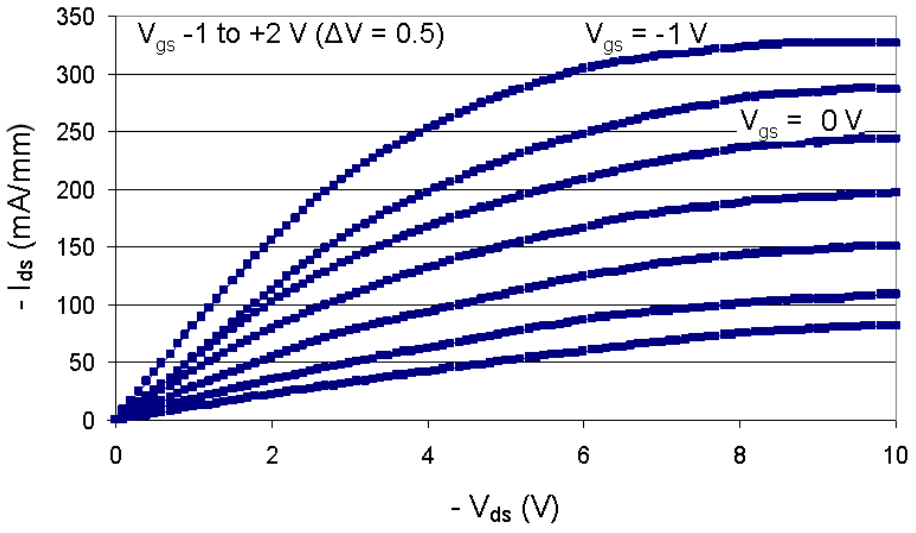


Figure 6.4.10: Output characteristics for 50 nm L_g FET

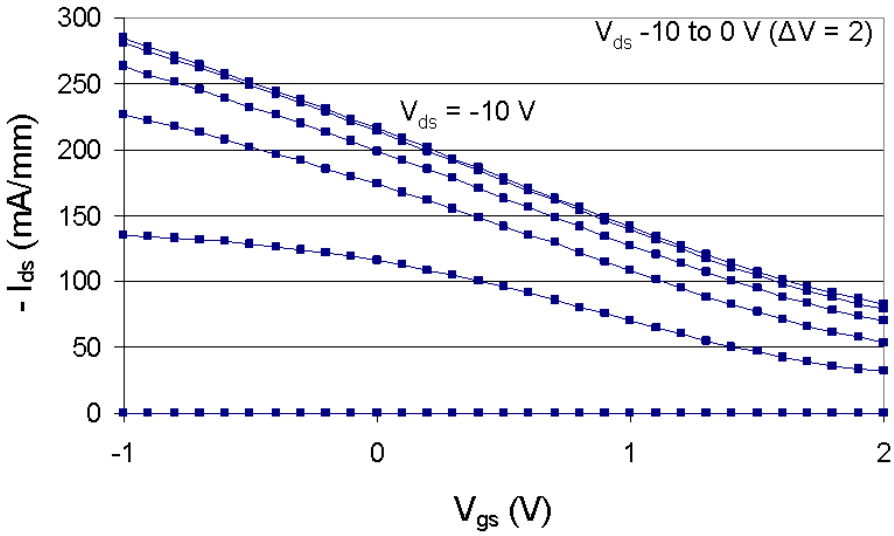


Figure 6.4.11: Transfer characteristics for 50 nm L_g FET

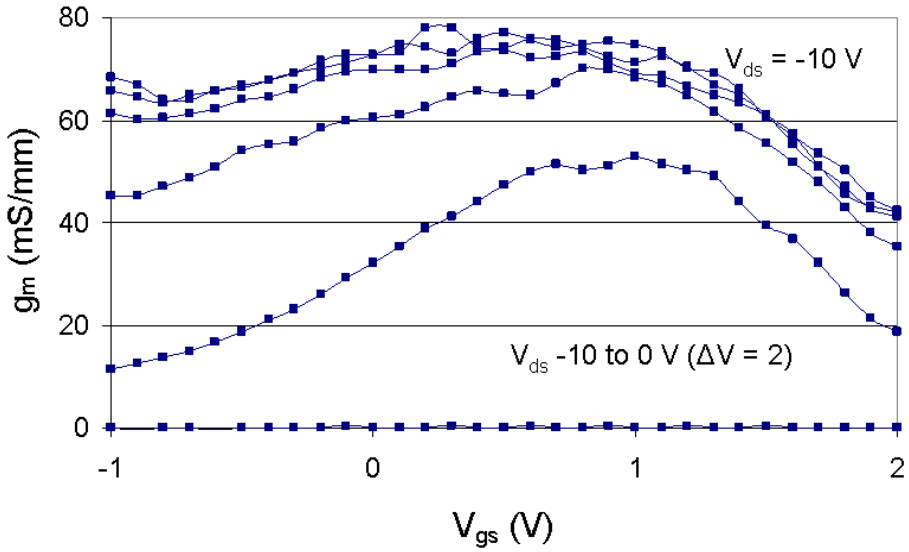


Figure 6.4.12: Transconductance plot for 50 nm L_g FET

The maximum drain current is still high with -325 mA.mm^{-1} achieved at a V_{gs} of -1 V although the devices take a large drain voltage to saturate fully requiring a V_{ds} ~ -8 V.

Even at a V_{gs} of + 2 V the channel is still showing significant drain current at this smaller gate dimension. An attempt was made to deplete the channel further but not until after the transfer characteristics were taken. Even though extra care was taken not too push the gate voltage too negative current degradation was still observed. The peak transconductance is extracted from Figure 6.4.13 to be just 78 $mS.mm^{-1}$ again with a plateau between a V_{ds} of -7 to -10 V and a V_{gs} of -0.5 to +1 V.

As for the prior devices with longer gate lengths the gate leakage observed in this device was below the noise floor of the measurement system.

Figure 6.4.13 shows a repeat measurement of the output characteristics between a V_{gs} of -2 and +4 V. The drain current is once again degraded overall giving credit to the theory this is intimately linked to the gate bias perhaps due to stronger negative gate voltages bringing charge closer to the surface and populating traps. This measurement also shows it was possible to deplete the channel of this device however not until a gate bias of +4 V.

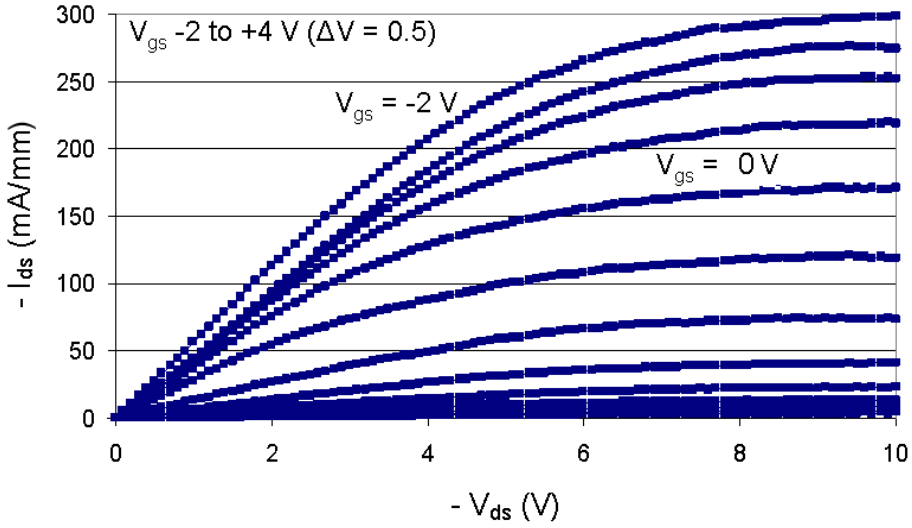


Figure 6.4.13: Output characteristics for 50 nm L_g FET with increased range of gate bias

This is the first time any characterisation has been reported on sub 100 nm gate length diamond FETs and has yielded some interesting results with the details published in relevant scientific literature [6.7]. There appears to be a gradual shift in the threshold voltage linked to the scaling of the gate suggesting it becomes more and more difficult to

deplete the channel at these reduced gate lengths. It is thought any further reduction of the gate length would likely lead to these effects becoming even more apparent. A reduced extrinsic transconductance compared to the previous trend of increase with reduction of gate length appears to suggest further evidence that at this gate length the gate is losing the ability to control the channel as well as before. Or there is increased access resistance present although from the SEM image the source-drain gap appears smaller than for the other devices suggesting the total access resistance should be smaller. Nevertheless, competitive drain current is still observed with the following sub-section detailing successful RF measurement and further information on the make-up of these devices as well as trying to build up an accurate model of their operation.

The DC figures of merit for these three devices are summarised in Table 6.4.1.

	250 nm Device	**120 nm Device**	**50 nm Device**
Peak Drain Saturation Current ($ma.mm^{-1}$)	-280 (at -2.5 V_{gs})	-360 (at -2 V_{gs})	-325 (at -1 V_{gs})
Threshold Voltage (V)	+1	+1	+4
Extrinsic Transconductance ($mS.mm^{-1}$)	92	137	78

Table 6.4.1: Summary of DC figures of merit for scaling study

6.5 250 nm RF Transistor Measurement

Along with obtaining results for DC measurement of each of the three device gate lengths RF characterisation was undertaken. As mentioned in Chapter 3 and expanded upon in Section 6.8, concerns regarding possible drain current degradation led to the use of a 'fresh' FET structure for RF measurement. Since device yield is low and there are a limited number of devices on each small diamond substrate, this leaves few attempts for successful RF measurements after DC characterisation. The best results are discussed here with S-parameter measurements taken from 1 to 20 GHz (as these were the only probes available

for the network analyser at the time) at the DC bias points at which peak DC transconductance was observed to ensure that the highest possible RF figures of merit may be extracted.

The de-embedded S-parameter measurements (i.e. the contribution of the co-planar waveguides having been removed) for a 250 nm L_g diamond FET at a bias of V_{ds} = -8 V and V_{gs} = -1 V are shown in Figure 6.5.1 plotted using Agilent's Advanced Design System (ADS) software and displayed in the Smith chart format for ease of visualisation.

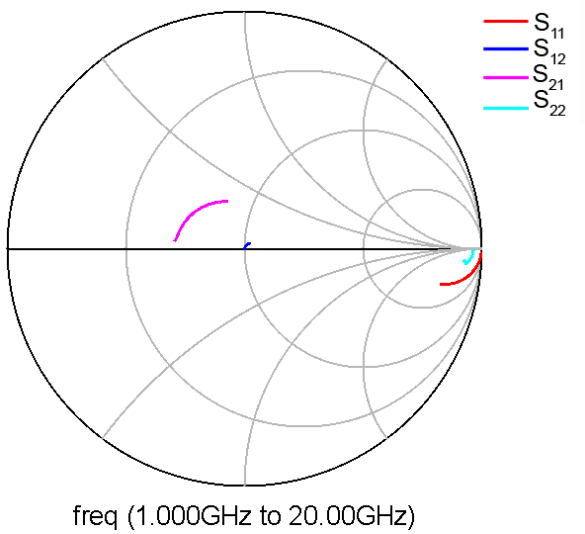


Figure 6.5.1: S-Parameter data for 250 nm L_g FET

From these measurements, a small signal equivalent circuit model at this bias point was extracted as discussed in Section 2.9. As can be seen from Figure 6.5.2 a reasonable model was achieved for the 250 nm device with only slight discrepancies present.

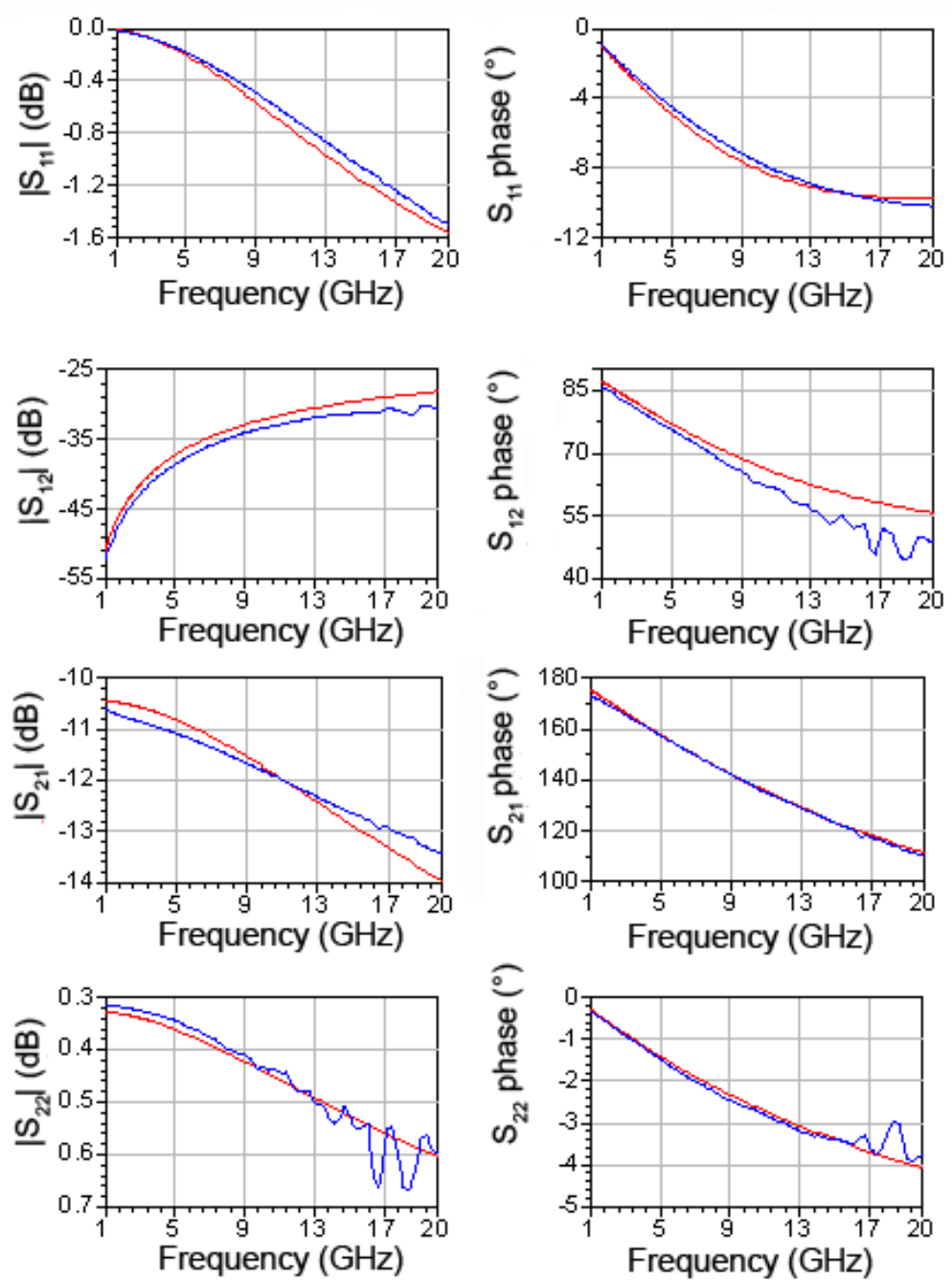


Figure 6.5.2: S-Parameter matching between measured data (blue) and modelled (red) for 250 nm L_g FET

Starting from a rough knowledge of the individual parameters as extracted from DC device and test structure measurement a range for each parameter can be assigned, then tuning may be performed in the ADS software to create an accurate model for the device at this

bias point and frequency range. E.g. TLM measurement gives us contact and sheet resistances and although R_s and R_d cannot be explicitly calculated from this measurement (due to different ohmic contact spacing amongst other factors such as variable ohmic edge roughness) a reasonable range within which the component value lies can be expressed nonetheless.

The magnitude and phase plots for each of the S-parameters show the matching in more detail. The Smith chart displays the complex impedance response of the FET with varying frequency, but the magnitude of each parameter can tell us how much of the respective signal is being reflected or transmitted through the device while the phase describes any delay in the signal. Due to the mismatch in input and output impedances S_{21} is in fact less than zero although gain is still present in the device [6.8]. Precise matching is challenging due to the model being dependent on a large range of values a large range of values. Traditional parameter extraction techniques such as 'cold FET' measurement were not possible here again due to repeat measurement leading to current degradation as mentioned previously which would lead to inaccurate parameter values. Extracted equivalent circuit values for the 250 nm device are presented in Table 6.5.1.

Circuit Element	Value	Circuit Element	Value
g_m^*	6.82 mS	R_d	144.60 Ω
R_{ds}	1.60 kΩ	L_g	0.13 fH
R_i	14.12 Ω	L_s	0.26 pH
C_{gs}	45.06 fF	L_d	0.13 pH
C_{gd}	2.35 fF	C_{gsp}	0.18 fF
C_{ds}	3.89 fF	C_{gdp}	0.56 aF
R_g	184.01 Ω	C_{dsp}	1.55 aF
R_s	144.13 Ω		

Table 6.5.1: Extracted equivalent circuit elements for 250 nm device

There is some margin for error associated with the equivalent circuit extraction and there are numerous reasons why the values may differ as detailed below.

Beginning with transconductance which is not quite as high as one would expect from the extracted DC intrinsic value, although it is not too far off if compared to the value extracted from the DC plot of 92 $mS.mm^{-1}$ in Figure 6.4.3. If this is converted from intrinsic to extrinsic transconductance as seen in Equation 2.8.4 we obtain 69 $mS.mm^{-1}$ (normalizing to a gate width of 50 μm). The fabrication procedure for creating the gate on the Au etched diamond surface is not well understood and although it was rinsed thoroughly there will still inevitably be residue present as has been seen in SEM pictures in this chapter. This could lead to surface states and traps which vary with frequency and affect the RF transconductance more than for the DC measurement. These traps may indeed be present even if deposition was possible straight on to the diamond without the Au etch process as unfortunately knowledge of this contact is still minimal. Finally there may even be traps present along the exposed surface regions. Source-drain resistance (R_{ds}) is of a reasonably high value as would be expected at this gate length, there is no noticeable slope observed in the saturation current in the output characteristics as seen in Figure 6.4.2 and hence low output conductance.

The total gate capacitance ($C_{gs} + C_{gd}$) is smaller than may be expected when modeling the gate and channel as a parallel plate capacitor which for a 10 nm separation between gate contact and device channel gives 63 fF. The equivalent circuit suggests it to be 47 fF, so only 75% of the parallel plate capacitor model's value. It is thought that since the gate metal is aluminium which oxidizes easily in air, there may be significant oxidation at the gate edges, reducing the effective gate area as well as the effective gate length. Also if an interfacial layer is present between Al and diamond this may well have a different dielectric constant. Finally the separation between gate and channel is also far from certain.

Gate resistance (R_g) is high but this is to be expected from a non-optimised gate design rather than employing a T-shape. Oxidation of the gate metal would also play a role with the gate stack consisting of just 25 nm Al topped with 25 nm Au. The source and drain access resistance are a reasonable value (both being 144 Ω) given the contact and sheet resistance values mentioned previously. The inductance/capacitances are small in value compared to the rest of the device elements hence having little effect on device performance.

Using the equations discussed in Section 4.5, extrinsic f_T and f_{MAX} were extracted as shown in Figure 6.5.3. With f_T = 19 GHz and f_{MAX} = 18GHz, these results are comparable to those obtained by M. Kubovic *et al* for a 200 nm gate length device [6.3].

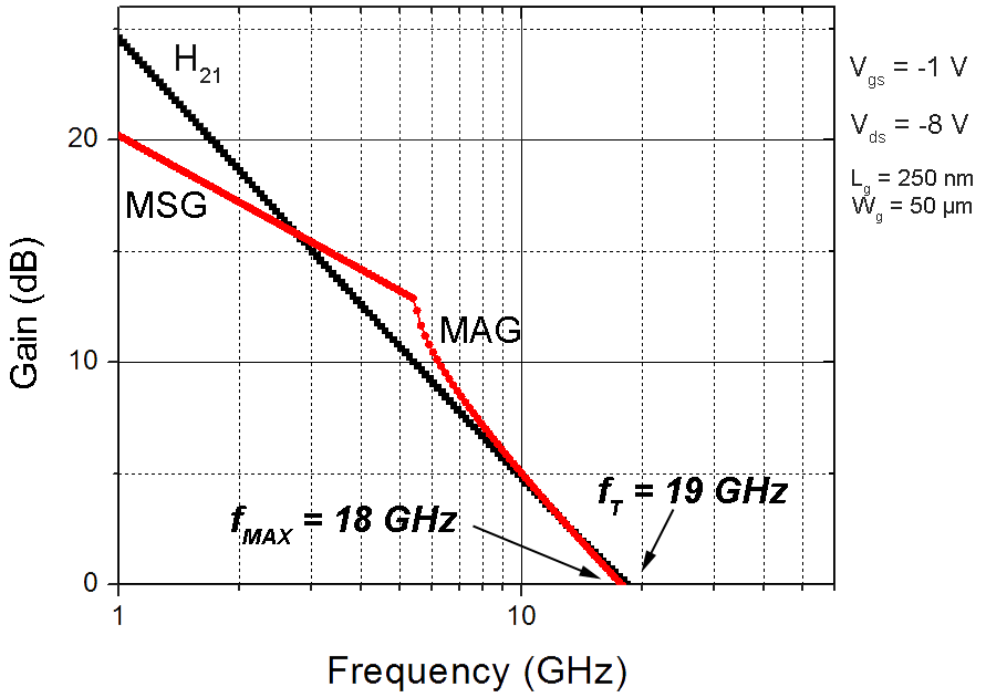


Figure 6.5.3: Extracted values for extrinsic f_T and f_{MAX} for 250 nm gate length FET

Using the equations given in Section 2.9 and considering the equivalent circuit values established from the device RF model, it is possible to calculate a value for intrinsic f_T and f_{MAX} and to compare these with the extrinsic values. The intrinsic value for f_T is calculated to be 23 GHz in comparison with an extrinsic value of 19 GHz. For f_{MAX} an intrinsic value of 27 GHz was calculated compared to the extracted value of 18 GHz. Hence it is clear that access resistances don't have a significantly detrimental effect on the value of f_T at this gate length and output conductance is still low enough to not impact the performance with f_T reaching 83 % of its potential and f_{MAX} 67 % (again both intrinsic and extrinsic f_{MAX} could be increased further by minimising R_g with a T-shaped gate structure).

As shown in Section 2.9 intrinsic f_T may also be related to velocity of carriers beneath the gate region. Using the value of 23 GHz extracted here gives an average velocity of 0.36 x

10^7 cm.s^{-1}. This value lies well below the saturation velocity of holes in intrinsic diamond (0.8 x 10^7 cm.s^{-1}) and suggests velocity overshoot does not occur at this gate length agreeing with the value observed by H. Matsudaira *et al* for a 200 nm FET [6.3].

6.6 120 nm RF Transistor Measurement

Moving to the 120 nm gate length device, biased at the same values as the 250 nm device, a V_{ds} of -8 V and a V_{gs} of -1 V, the S-parameter plot is noticeably different as shown in Figure 6.6.1. The impedance response of S_{21} appears to vary with frequency more than the 250 nm device besides which the other parameter responses appear similar.

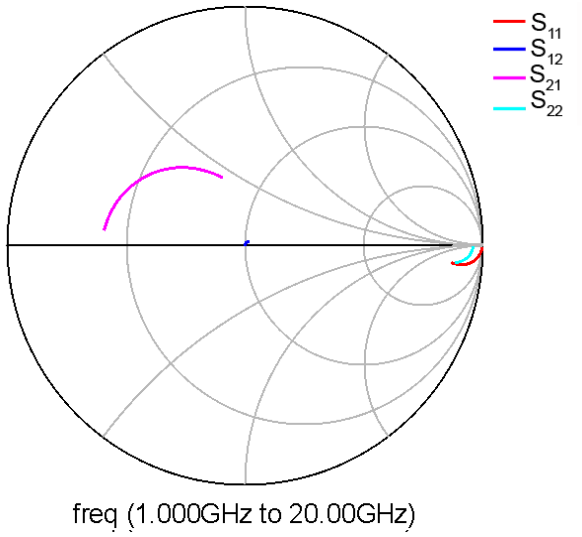


Figure 6.6.1: S-Parameter data for 120 nm L_g FET

In creating the extracted equivalent circuit model, S-parameter magnitude and phase were again matched as closely as possible and tuned to the measured values. The measured signal response is again plotted against the equivalent circuit response as pictured in Figure 6.6.2

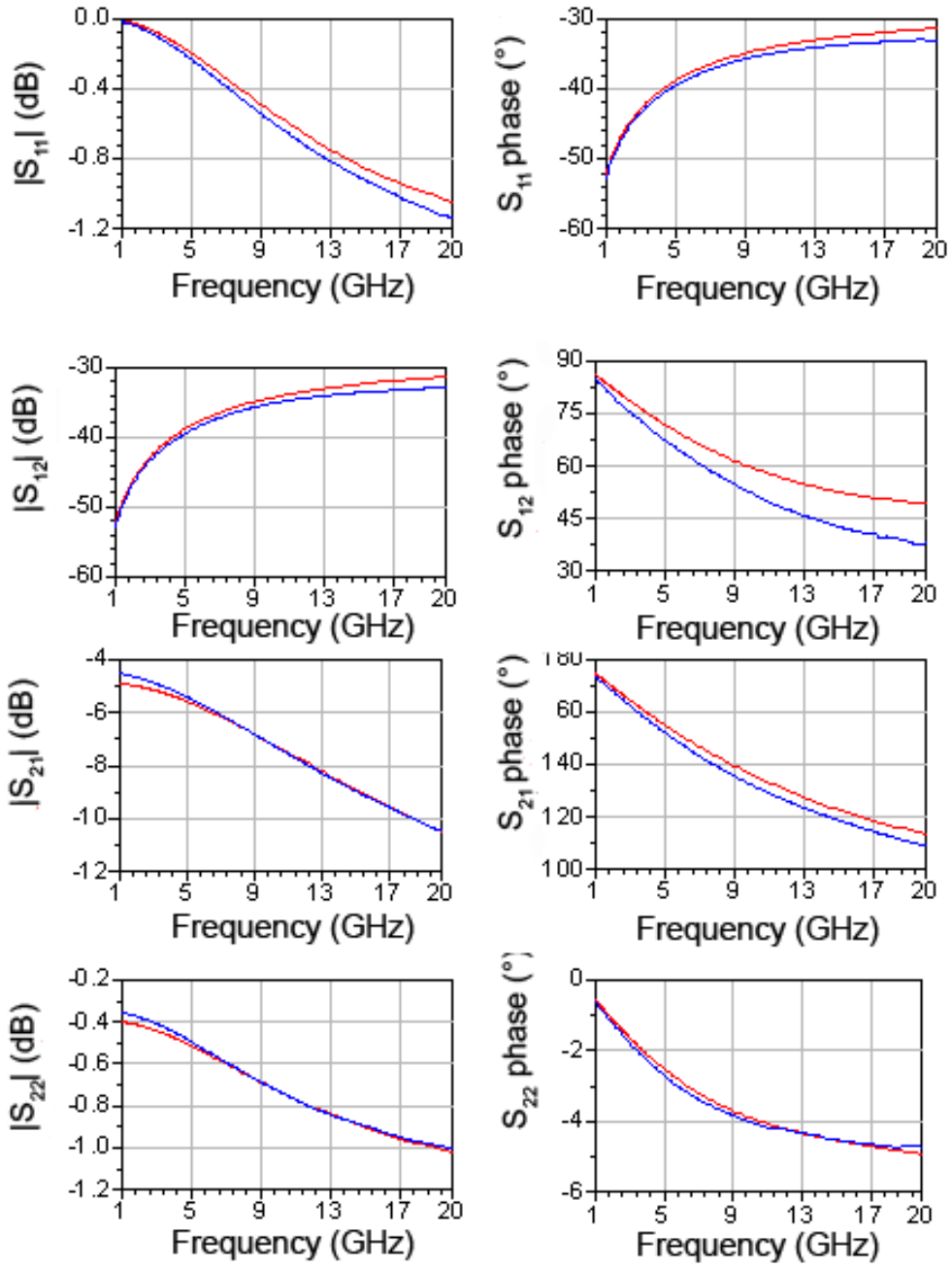


Figure 6.6.2: S-Parameter matching between measured data (blue) and modelled (red) for 120 nm L_g FET

Extracted equivalent circuit values are presented in Table 6.6.1 and would seem to obey the scaling trend as observed in the DC measurements. Beginning with intrinsic transconductance, this is as expected from the DC measurement higher than for the 250 nm device. Once again when converting and normalising by the gate width 128 $mS.mm^{-1}$ does

not quite match the value from the extrinsic DC transconductance measurement of 137 $mS.mm^{-1}$.

Circuit Element	Value	Circuit Element	Value
g_m^*	17.00 mS	R_d	97.30 Ω
R_{ds}	0.90 kΩ	L_g	3.22 pH
R_i	16.09 Ω	L_s	9.54 pH
C_{gs}	39.76 fF	L_d	1.52 pH
C_{gd}	1.80 fF	C_{gsp}	4.90 aF
C_{ds}	3.10 fF	C_{gdp}	0.56 fF
R_g	508.00 Ω	C_{dsp}	0.01 fF
R_s	97.30 Ω		

Table 6.6.1: Extracted equivalent circuit elements for 120 nm device

Output resistance is slightly lower here at 0.9 kΩ compared to 1.6 kΩ for the 250 nm gate length. This may be expected due to the gate having slightly less control of the channel but not to the point where short channel effects are significantly hampering device performance.

Total gate capacitance is lower than for the previous device but only by ~5 fF to 42 fF suggesting that capacitance of the gate contact does not necessarily scale with gate length as we would expect. A gate capacitance of 30 fF is found from the parallel plate approximation which is smaller than the equivalent circuit value. Perhaps the oxidation speculated for the previous device gate is not as prevalent here, the intermediate layer may be larger or the different gate lengths draw the charge to slightly different distances beneath the diamond surface as they apply different electric fields accounting for why this value is in fact larger than predicted. It should also be reinforced at this point the values extracted from the equivalent circuit are only accurate for this bias point. It is clear the parallel plate approximation is not entirely suitable here. Although the transconductance is significantly improved at this gate length capacitance still ultimately limits the performance. Access resistances are lower with both R_s and R_d = 97 Ω which is in agreement with the lower R_{ON} seen for the DC measurement even though there is no

discernable difference in the ohmic contact spacing between SEM images of the 250 nm and 120 nm devices (seen in Figures 6.4.1 and 6.4.5 respectively) although this R_{ON} value also accounts for the resistance beneath the gate which as stated above is lower than for the 250 nm device.

One anomalous value in this model is the gate resistance. In comparison with the 250 nm gate, one would expect this to increase purely due to the smaller cross-sectional gate area. However the increase here is fairly substantial from 184 to 508 Ω. A crude calculation taking the average resistivity of Al and Au to be 2.63×10^{-8} yields a predicted resistance of 105 Ω for the 250 nm gate and 219 Ω for the 120 nm gate. It could be suggested that oxidation of the gate metal could account for this however that would also affect other parameters such as gate capacitance and transconductance. Other causes could be defects in the gate structure - for example regions where the gate has been unusually constricted or deformed due to lithographic defects (an example can be seen in Figure 6.6.3) or perhaps even when metal has been deposited especially as the gate is topped with Au this layer may not contact the Al producing a much thinner deposition than expected.

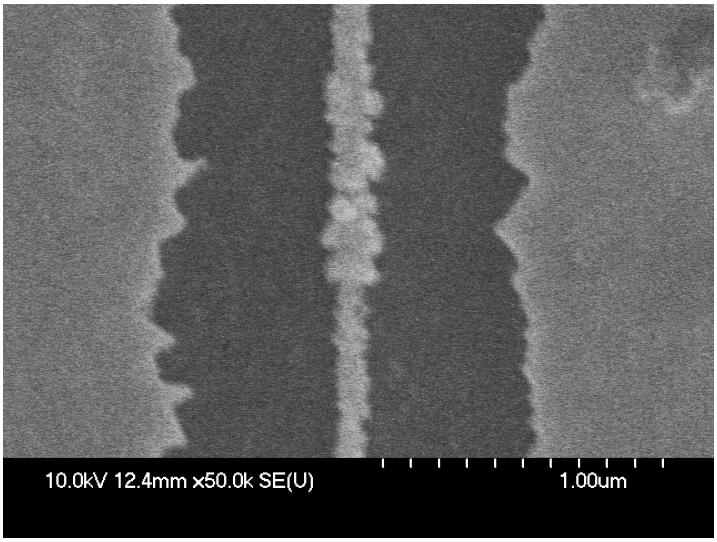


Figure 6.6.3: Deformation of gate due to lithographic deffect

Values for f_T and f_{MAX} were again extracted as seen in Figure 6.6.4, although this time a small amount of extrapolation is required as both values lie above the maximum measured frequency of 20 GHz. The f_T value of 45 GHz is a significant result, as it matches the values obtained by both K. Ueda *et al* and K. Hirama *et al* although with some differences

in device design [6.9-10]. The result obtained by Ueda was from a 100 nm device while Hirama's was 150 nm and utilised a gate insulator of Al_2O_3, while both devices used polycrystalline material. This is by far the best result obtained to date on single crystal diamond proving it is just as viable for producing FET devices as polycrystalline material. Again the 25 GHz value for f_{MAX} is not as high as could be achieved with an optimised T-gate design.

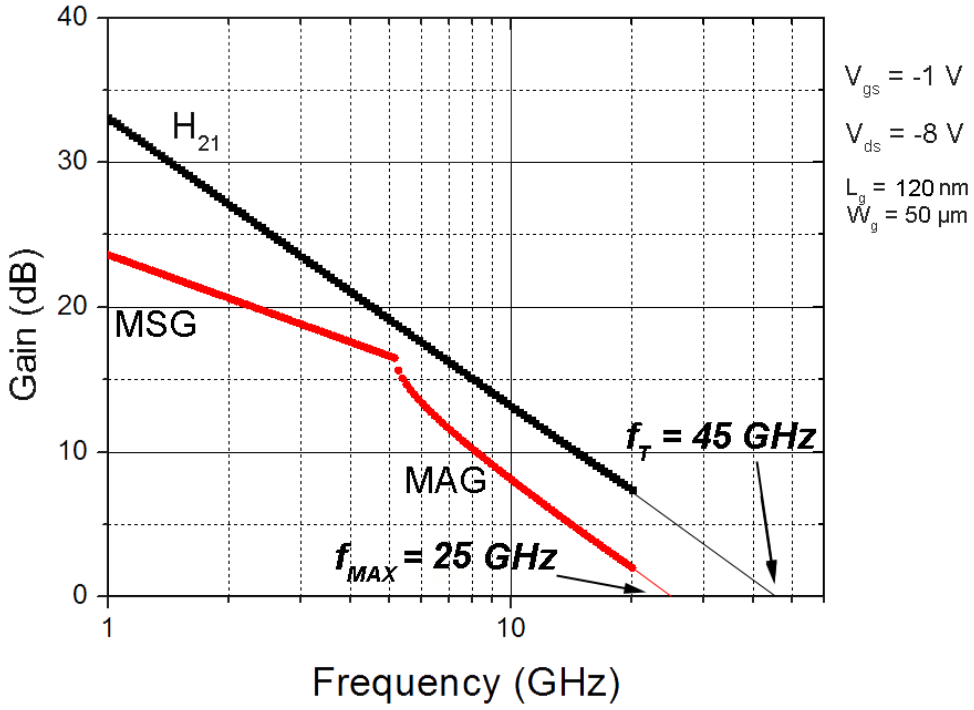


Figure 6.6.4: Extracted values for extrinsic f_T and f_{MAX} for 120 nm FET

Calculating the intrinsic values yields f_T = 65 GHz and f_{MAX} = 42 GHz with the extrinsic f_T now 69 % of the intrinsic value and the extrinsic f_{MAX} just 60 % of the intrinsic value showing that as these devices are scaled the parasitic effect of access resistance becomes more pronounced as well as an increased output conductance. It should be noted the figure for f_{MAX} may have the potential to be higher due to the unusually large and perhaps anomalous R_g for this device.

Relating intrinsic fT to the carrier velocity beneath the gate as done for the previous device using the value of 65 GHz extracted here gives an average velocity of 0.49 x 10^7 $cm.s^{-1}$.

This value albeit faster again lies below the saturation velocity of holes in intrinsic diamond and suggests velocity overshoot does not occur at this gate length.

6.7 50 nm RF Transistor Measurement

The Smith chart for the 50 nm devices (biased at V_{ds} = -8 V and V_{gs} = -0.4 V) is noticeably different to the other two devices as seen in Figure 6.7.1.

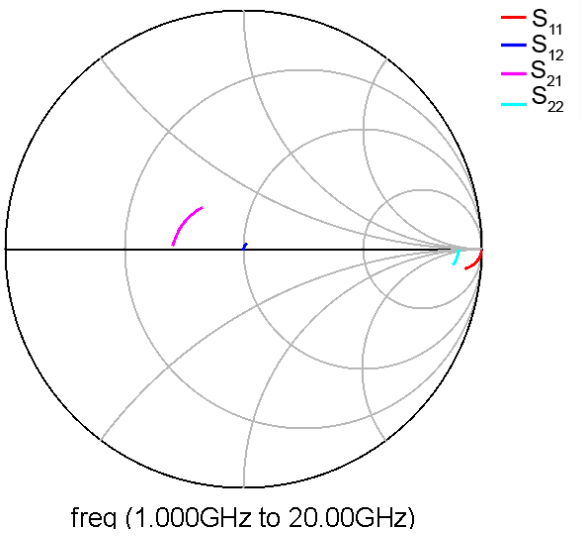


Figure 6.7.1: S-Parameters for 50 nm L_g FET

All parameters are once again matched to the equivalent circuit model with the matching plots picture in Figure 6.7.2. The matching achieved was worse than for the larger gate length devices although this may be expected considering the relative magnitude of the S-parameters here are much smaller than for previous devices.

The equivalent circuit values are displayed in Table 6.7.1 and seem to agree with the trends observed in DC device measurement. The intrinsic transconductance is smaller than for the 120 nm FET but larger than the 250 nm device and converting to extrinsic transconductance then comparing to the extracted DC value this time it roughly matches at 84 $mS.mm^{-1}$. Although this transconductance value is significantly smaller than for the 120

nm FET the intrinsic gate capacitances have also scaled so as not to fundamentally limit the RF performance.

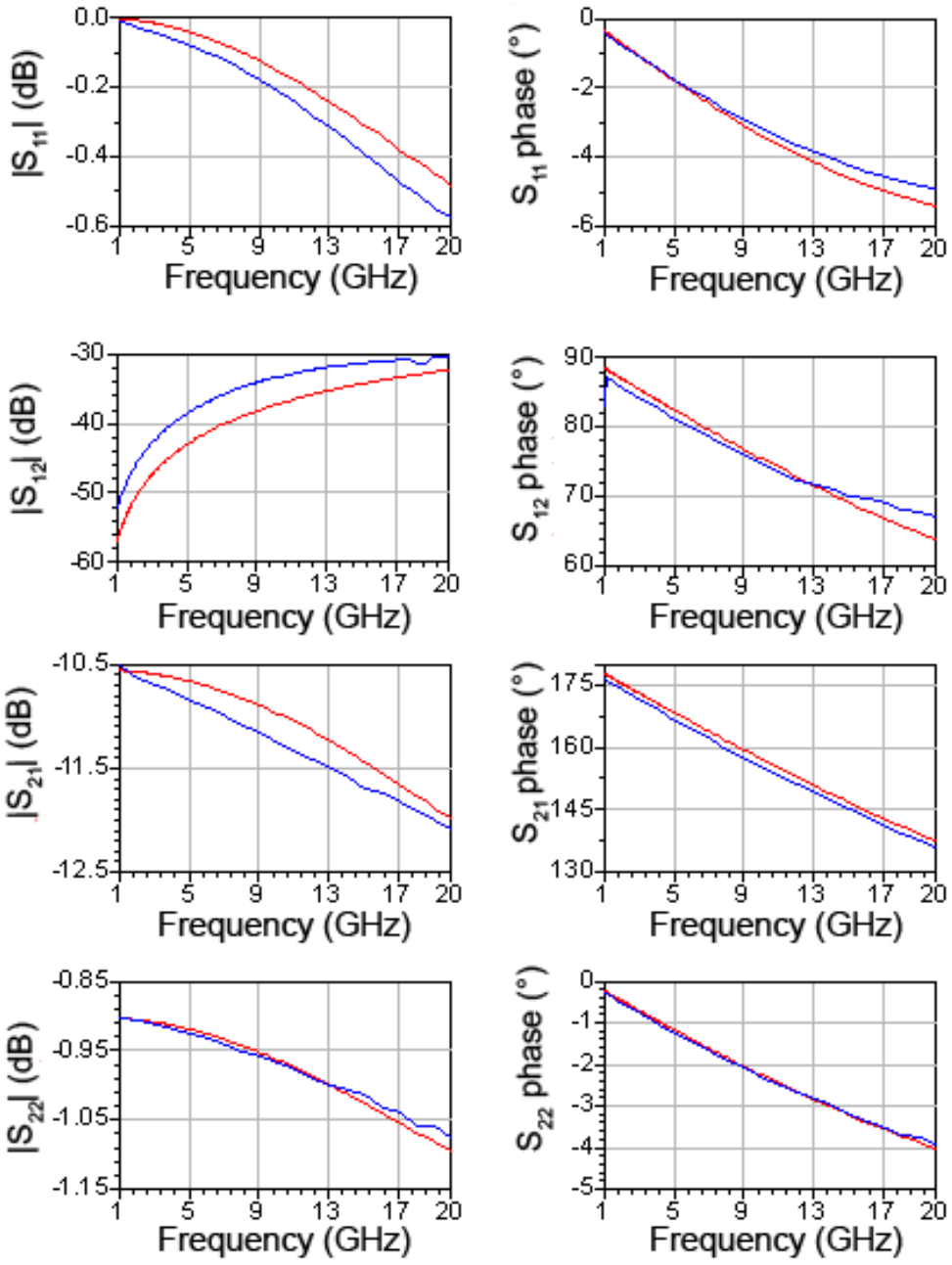


Figure 6.7.2: S-Parameter matching between measured data (blue) and modelled (red) for 50 nm L_g FET

Circuit Element	Value	Circuit Element	Value
g_m^*	8.75 mS	R_d	119.00 Ω
R_{ds}	0.37 kΩ	L_g	0.70 pH
R_i	27.20 Ω	L_s	1.80 pH
C_{gs}	15.20 fF	L_d	1.44 pH
C_{gd}	0.30 fF	C_{gsp}	1.15 aF
C_{ds}	5.02 fF	C_{gdp}	0.17 fF
R_g	370.40 Ω	C_{dsp}	0.89 fF
R_s	125.00 Ω		

Table 6.7.1: Extracted equivalent circuit elements for 50 nm device

Other circuit values have also changed at this gate length however and will have an impact on the RF figures of merit. Output resistance is less than half the value of the 120 nm FET at 0.37 kΩ rather than 0.9 kΩ and a quarter of that of the 250 nm (1.6 kΩ) FET. This suggests that short channel effects although not crucially diminishing device performance, are becoming important as has been noted in the DC characterisation. Where a V_{gs} of +2 V would be sufficient to pinch off the larger gate length devices there is still drain current present here and takes a V_{gs} of +4 V to fully achieve pinch off.

Total gate capacitance is smaller at 16 fF than 42 fF for 120 nm gate length device and 37 fF for the 250 nm gate length device. The parallel plate capacitor model suggests a total gate capacitance of 12.6 fF for 50 nm gate length which is close to this result.

The gate resistance is larger at 370 Ω than for the 250 nm FET (184 Ω) but smaller than for 120 nm (508 Ω). This is unexpected but this increased resistance would seem reasonable for this gate length due to the smaller cross-sectional gate area (which from a crude resistivity calculation yields 526 Ω). This also suggests that the high R_g value seen for the 120 nm gate may indeed be anomalous. Both access resistances R_s and R_d at 125 Ω and 119 Ω respectively again seem reasonable considering the range of values possible from variable source-drain gap spacing and contact edge roughness.

Extrapolation of the data seen in Figure 6.7.3 was again necessary to find the RF figures of merit with f_T = 53 GHz and f_{MAX} = 27 GHz being observed. This is the largest f_T value yet reported from a diamond FET as well as being the first RF data reported from a sub-100 nm diamond FET. [6.11]

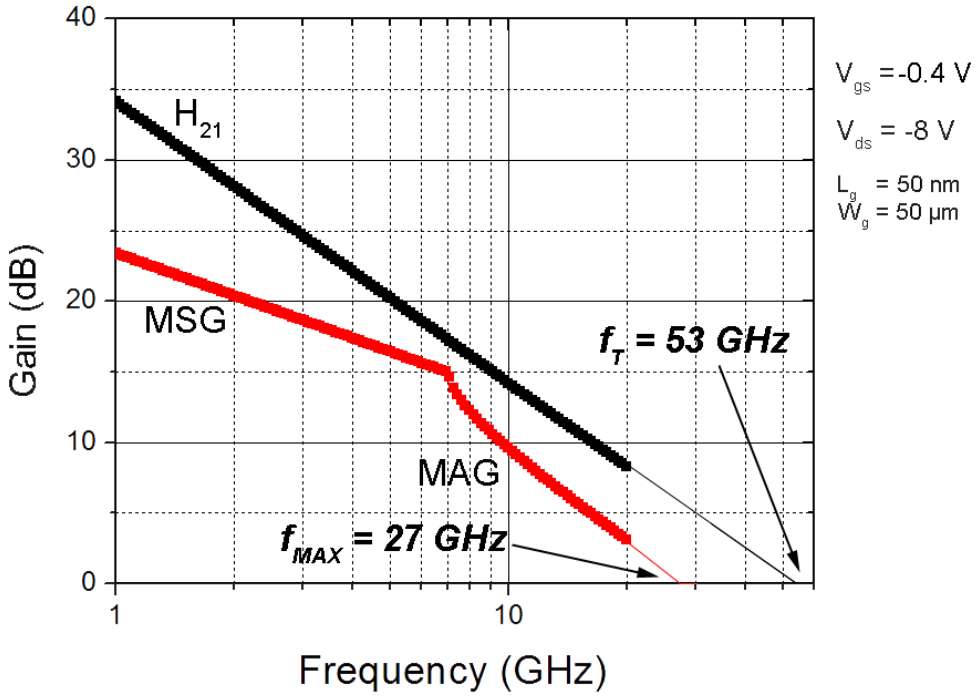


Figure 6.7.3: Extracted values for extrinsic f_T and f_{MAX} for 50 nm FET

Although this is the highest f_T value yet reported and it is an improvement upon the 45 GHz observed for the 120 nm FET it is not as significant an improvement as was seen moving from 250 to 120 nm where f_T more than doubled. Again looking at the intrinsic values for f_T and f_{MAX}, intrinsic f_T = 90 GHz and intrinsic f_{MAX} = 43 GHz for this 50 nm device. So extrinsic f_T is now just 59 % of the intrinsic value with f_{MAX} being 63 %.

Relating intrinsic fT to the carrier velocity beneath the gate as done for the previous device using the value of 90 GHz extracted here yields an average velocity of 0.28 x 10^7 $cm.s^{-1}$ for carriers beneath the gate. This value is slower than for both the 250 nm and 120 nm devices, once again lying below the saturation velocity of holes in intrinsic diamond and suggests velocity overshoot does not occur even at this gate length.

Hence the effect of access resistance along with the output conductance becomes significantly more prominent as is common when scaling devices to shorter gate lengths. This trend as seen in Figure 6.7.4 indicating it is unlikely that further scaling of the gate length geometry would lead to a large improvement in the f_T of these devices.

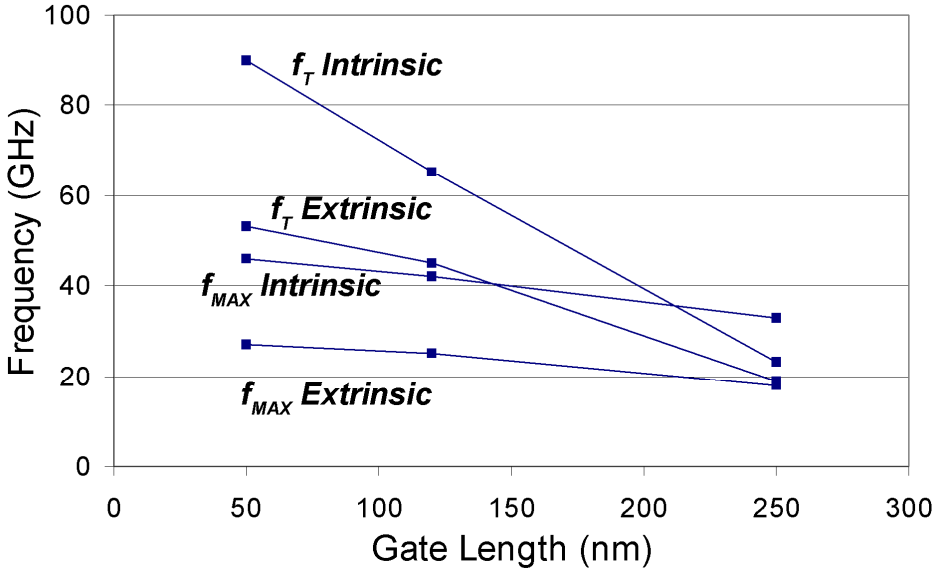


Figure 6.7.4: Plot comparing extrinsic and intrinsic f_T and f_{MAX} for each device gate length

This trend may also be seen in Table 6.7.2 which summarises the performance of each device gate length and highlighting the effect of scaling on equivalent circuit elements important to the value of f_T. It shows that instead of further gate length scaling focus now needs to be shifted in to minimising the extrinsic elements that limit the potential RF performance and/or if possible increasing the output resistance at reduced gate lengths.

	250 nm L_g	**120 nm L_g**	**50 nm L_g**
f_T Extrinsic	19 GHz	45 GHz	53 GHz
f_T Intrinsic	23 GHz	65 GHz	90 GHz
Extrinsic Percentage of Intrinsic Value	83 %	69 %	59 %
f_{MAX} Extrinsic	18 GHz	25 GHz	27 GHz
f_{MAX} Intrinsic	27 GHz	42 GHz	43 GHz
Extrinsic Percentage of Intrinsic Value	67 %	60 %	63 %
Extracted Carrier Velocity Beneath Gate	0.36×10^7 cm.s^{-1}	0.49×10^7 cm.s^{-1}	0.28×10^7 cm.s^{-1}
g_m^*	6.82 mS	17 mS	8.75 mS
Total C_g ($C_{gs} + C_{gd}$)	47.41 fF	41.56 fF	15.5 fF
Access Resistance ($R_s + R_d$)	288.73 Ω	194.6 Ω	246 Ω
R_{ds}	1.6 kΩ	0.9 kΩ	0.37 kΩ

Table 6.7.2: Comparison of device performance with gate length and effect of scaling on important equivalent circuit values

6.8 Degradation

As has already been mentioned repeat measurements at a high negative gate bias leads to drain current degradation in these surface channel FETs. It is thought that this phenomenon is intimately linked to the gate contact as repeat measurement at low gate voltages or on TLM structures does not appear to noticeably degrade the current and the smaller the gate length the less gate bias will cause degradation i.e. for a 50 nm device no greater than a V_{gs} of -1 should be applied. However as shown there is no significant gate leakage in these devices, hence it is thought a trapping mechanism involving the gate contact may be responsible.

To try to provide some insight as to why this happens, DC current-voltage measurements at a constant bias were taken for various periods of time using the 50 nm gate length FET as well as a 1 μm TLM gap for a comparison. Interestingly every single measurement showed a change in the measured current with respect to time. Beginning with the 1 μm TLM gap, Figures 6.8.1 and 6.8.2 show measurement of current at -5 and -20 V respectively for a time of 30 seconds.

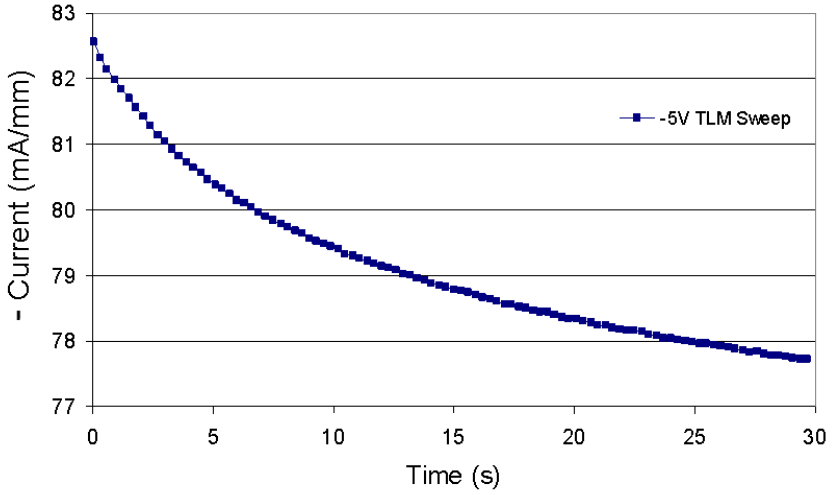


Figure 6.8.1: 1 μm TLM gap timed 30 s measurement for -5 V

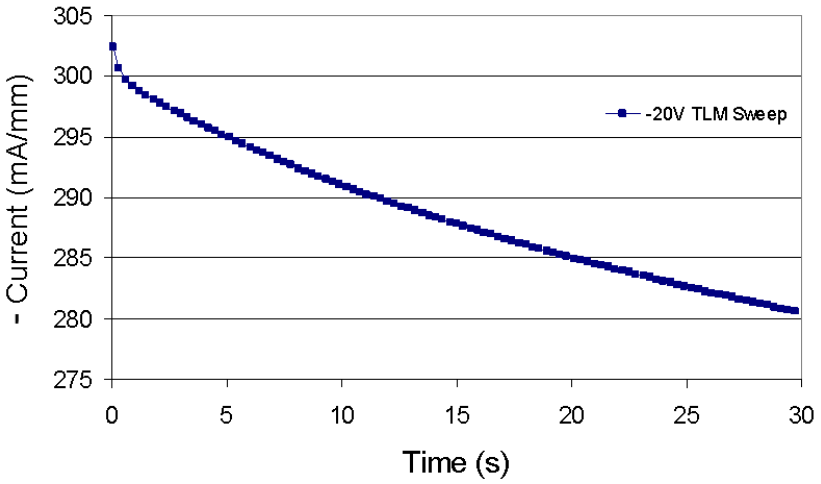


Figure 6.8.2: 1 μm TLM gap timed 30 s measurement for -20 V

In this timeframe, in the case of the -5 V sweep, the current degrades by ~ 6% of its original value by the end of the measurement with the -20 V measurement also degrading by ~6%. When the next measurements were taken however the current had fully recovered

at time = 0 s, (see Figures 6.8.3 and 6.8.4) which suggests degradation of current in the TLM structure i.e. without a gate is only temporary and recovers very quickly when biasing is removed. Figures 6.8.3 and 6.8.4 demonstrate this degradation across a shorter scan of just 1 second. Degradation is again observed although this time much more so for the -20 V bias which loses ~ 1% of its current compared to ~0.3% for the -5V scan.

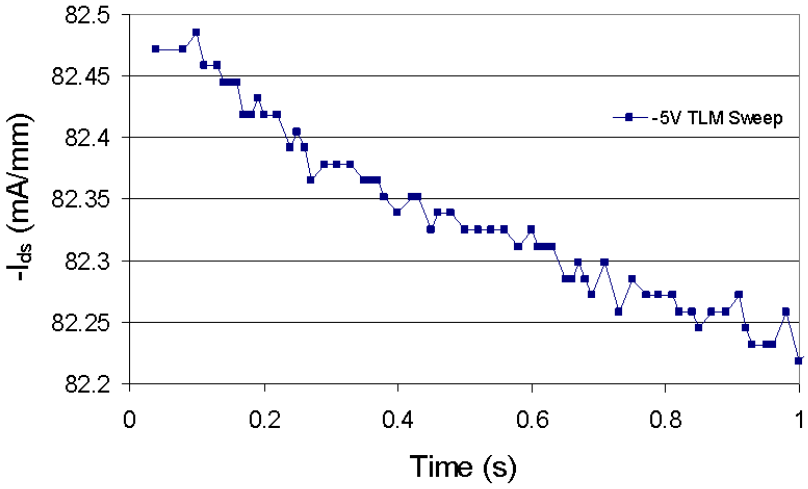


Figure 6.8.3: 1 μm TLM gap timed 1 s measurement for -5 V

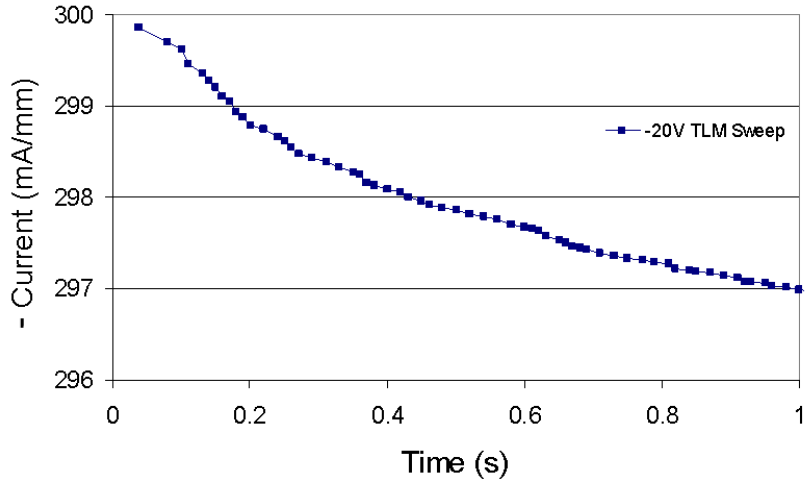


Figure 6.8.4: 1 μm TLM gap timed 1 s measurement for -20 V

A final set of measurements can be observed in Figures 6.8.5 and 6.8.6 showing the same bias points again for the 1 μm TLM gap, only this time over 3 minutes. The original current is again fully recovered from the last scan at time = 0 s and over the course of the 3 minutes the -5 V bias scan shows a current loss of ~8% as opposed to 16% for -20 V.

Hence it appears the larger the bias the faster degradation ensues. Also in Figure 6.8.5 the loss of current appears to be beginning to saturate by 3 minutes whereas in Figure 6.8.6 degradation continues.

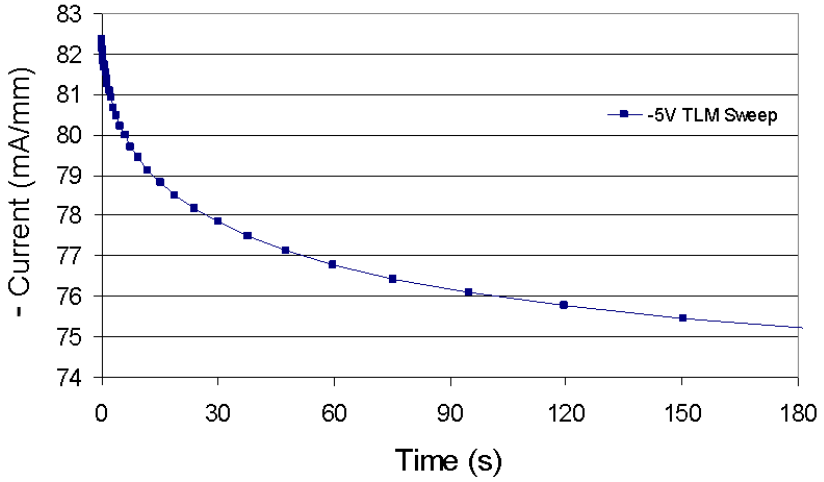


Figure 6.8.5: 1 μm TLM gap timed 3 mins measurement for -5 V

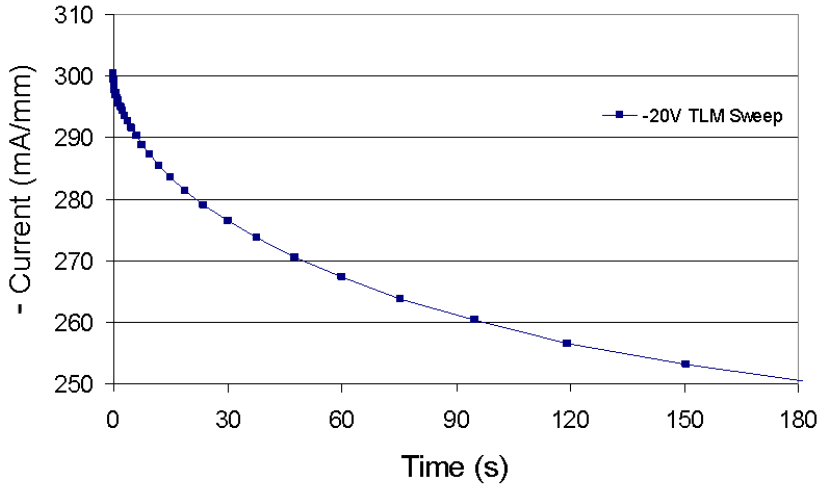


Figure 6.8.6: 1 μm TLM gap timed 3 mins measurement for -20 V

Moving to the 50 nm gate length device, a gate bias of V_{gs} = 0 V was inspected to give a contrast to the TLM measurements, although they cannot be compared directly as the built in voltage the gate provides makes these structures incomparable. A measurement at a V_{ds} of -1 V which is within the linear operating regime of this device is shown in Figure 6.8.7. A loss of ~ 3% in current is seen over a 30 second measurement and in contrast to the

TLM structure, the current does not fully recover between each of the following measurements, but instead decreases slightly for each. When measured at a V_{ds} of -10 V as shown in Figure 6.8.8 a ~ 36% drop can be seen in the current over 30 seconds suggesting that whatever mechanism degrades the current the presence of the gate contact certainly appears to accentuate it.

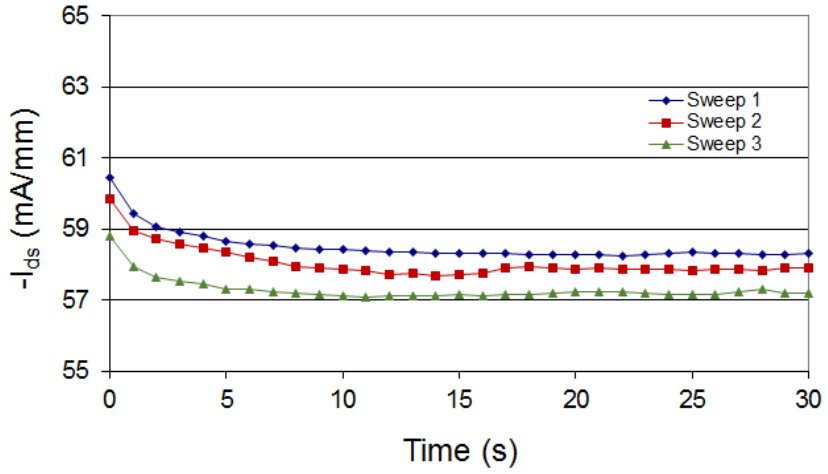


Figure 6.8.7: 50 nm FET timed measurement, 30 seconds -1 V V_{ds}, 0 V_{gs}

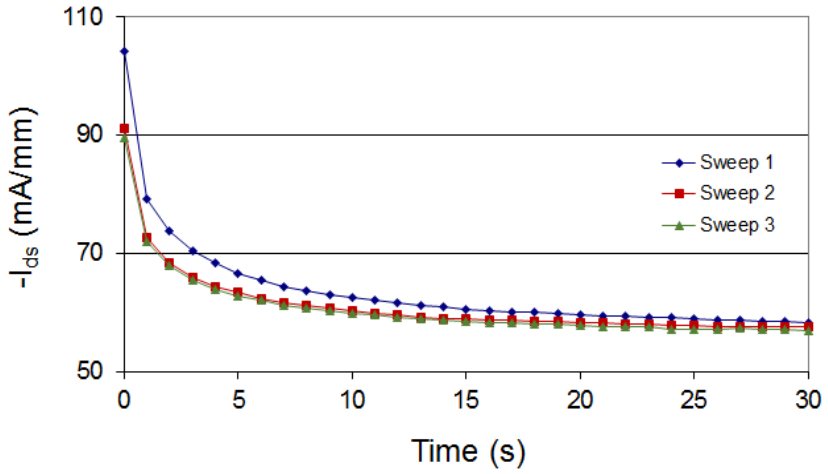


Figure 6.8.8: 50 nm FET timed measurement, 30 seconds -10 V V_{ds}, 0 V_{gs}

Two final graphs in Figure 6.8.9 and 6.8.10 show the same measurement of the 50 nm device but with a V_{gs} of -4 V applied. In contrast to the previous measurements, current actually increases here with time. This suggests the mechanism involved is detrimental due to its instability and is indeed intimately linked to the gate contact although it does not necessarily involve a decrease or 'degradation' in current.

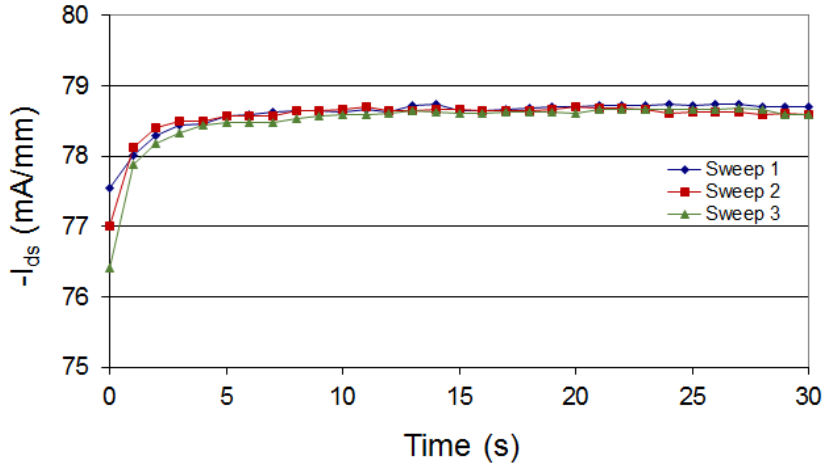


Figure 6.8.9: 50 nm FET timed measurement, 30 seconds -1 V V_{ds}, -4 V V_{gs}

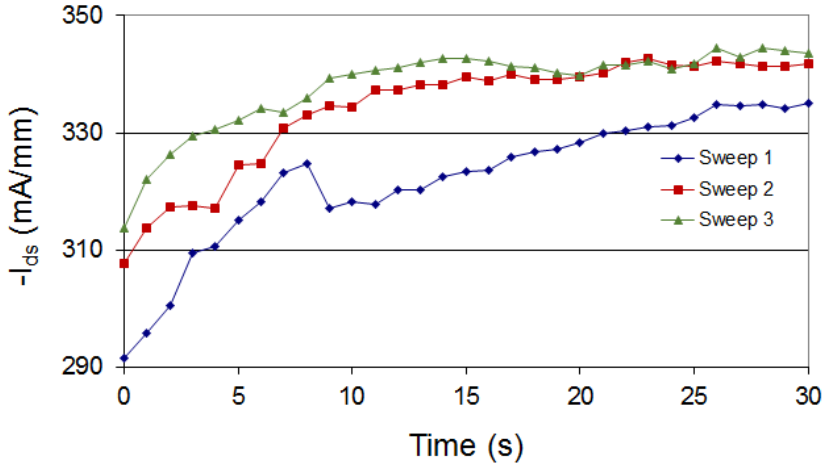


Figure 6.8.10: 50 nm FET timed measurement, 30 seconds -10 V V_{ds}, -4 V V_{gs}

Tables 6.8.1 and 6.8.2 provides a summary of the measurements undertaken in this section for ease of comparison.

	-5 V	-20 V
Original Current	-82.5 mA.mm^{-1}	-300 mA.mm^{-1}
After 1 second bias	-82.2 mA.mm^{-1}	-297 mA.mm^{-1}
Percentage Change	-0.3 %	-1 %
Original Current	-82.5 mA.mm^{-1}	-300 mA.mm^{-1}
After 30 second bias	-77.8 mA.mm^{-1}	-281 mA.mm^{-1}
Percentage Change	-6 %	-6 %
Original Current	-82.5 mA.mm^{-1}	-300 mA.mm^{-1}
After 3 minutes bias	-75.5 mA.mm^{-1}	-250 mA.mm^{-1}
Percentage Change	-8 %	-16 %

Table 6.8.1: Summary of current degradation for a 1 μm TLM gap

	Sweep 1	Sweep 2	Sweep 3
Original Current	-60.5 mA.mm^{-1}	-60.0 mA.mm^{-1}	-58.8 mA.mm^{-1}
After Bias (V_{ds} = -1 V, V_{gs} = 0 V)	-58.3 mA.mm^{-1}	-57.9 mA.mm^{-1}	-57.2 mA.mm^{-1}
Percentage Change	-3.6 %	-3.5 %	-2.7 %
Original Current	-104 mA.mm^{-1}	-91.1 mA.mm^{-1}	-89.6 mA.mm^{-1}
After Bias (V_{ds} = -10 V, V_{gs} = 0 V)	-58.3 mA.mm^{-1}	-57.5 mA.mm^{-1}	-57.0 mA.mm^{-1}
Percentage Change	-43.9 %	-36.8 %	-36.4 %
Original Current	-76.4 mA.mm^{-1}	-77.0 mA.mm^{-1}	-77.5 mA.mm^{-1}
After Bias (V_{ds} = -1 V, V_{gs} = -4 V)	-78.6 mA.mm^{-1}	-78.6 mA.mm^{-1}	-78.7 mA.mm^{-1}
Percentage Change	+2.9 %	+2.1 %	+1.5 %
Original Current	-292 mA.mm^{-1}	-308 mA.mm^{-1}	-314 mA.mm^{-1}
After Bias (V_{ds} = -10 V, V_{gs} = -4 V)	-335 mA.mm^{-1}	-342 mA.mm^{-1}	-344 mA.mm^{-1}
Percentage Change	+14.7 %	+11.0 %	+9.6 %

Table 6.8.2: Summary of current degradation for 50 nm gate length FET

Conclusive explanations for the mechanism behind this degradation/instability remain unclear. In terms of surface quality, all samples even after hydrogen-termination exhibit a very smooth surface as shown by an AFM scan for this sample in Figure 6.8.11 where an RMS roughness of 0.31 nm was measured.

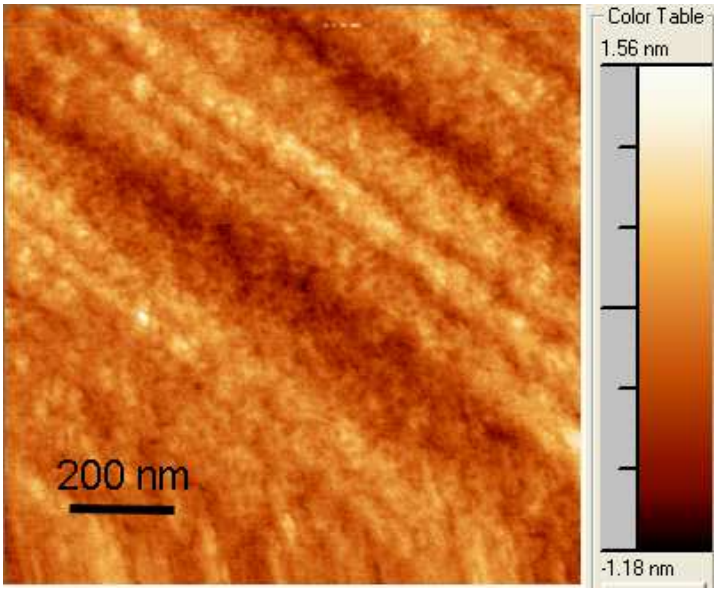


Figure 6.8.11: AFM surface roughness scan on sample post-hydrogenation

The explanation may be associated with the atmospheric adsorbate particles be it that they move during measurement as has been suggested by M. Kasu *et al* [6.12], the hydrogen itself evaporates beneath the contacts [6.12], or even a simpler charge trapping mechanism at the diamond adsorbate interface. This final explanation seems to be the most likely especially as slight degradation still appears even in recently fabricated devices encapsulated by Al_2O_3 [6.13]. An effect known as 'current collapse' is seen in GaN FETs where charge may populate surface traps causing a 'virtual gate' to deplete the channel and degrade the current and it is possible a similar situation occurs here especially as the degradation appears to be linked to the gate bias and will even act to increase the current at certain biases [6.14].

It would appear this effect is related to the exposed regions between source and gate and gate and drain as well as the gate contact itself. Instead of being charged by a virtual gate it is possible the relative electric field across the sample acts to further trap charge or remove

it from surface traps upon the diamond surface. This is the only explanation which fits with the measurements taken here and emphasises the need to pursue a suitable electron accepting layer with minimal charge trapping. Further work also needs to be done on understanding the gate contact.

6.9 Summary

This chapter has summarised the FET device results obtained during this research. It has built on work done by previous groups in realising the high frequency potential of diamond transistors and provided a comparison between different gate length devices as they are scaled. For the first time, a sub-100 nm diamond FET has been realised and rigorously characterised. The data shows improvement upon previous FETs in the literature with the highest f_T obtained to date.

These results have also indicated the limitations associated with scaling and that for further significant improvement new fabrication techniques need to be implemented. It emphasises the need to replace the atmospheric dopant molecules with a more robust solution and degradation measurements also highlight this need as well as the potential need for a passivation layer.

References:

[6.1] M. Kasu, K. Ueda, Y. Yamauchi, A. Tallaire and T. Makimoto, "Diamond-based RF power transistors: Fundamentals and applications," *Diamond and Related Materials*, vol. 16, no. 4-7, pp. 1010-1015, 2007

[6.2] J. A. Garrido, C. E. Nebel, M. Stutzmann, E. Gheeraert, N. Cassanova and E. Bustarret, "Electrical and optical measurements of CVD diamond doped with sulphur," *Physical Review B*, vol. 65, no. 16, pp. 165409-1-165409-6, 2002

[6.3] H. Matsudaira, S. Miyamoto, H. Ishizaka, H. Umezawa and H. Kawarada, "Over 20-GHz cutoff frequency submicrometer-gate diamond MISFETs," *IEEE Electron Device Letters*, vol. 25, no. 7, pp. 480-482, 2004

[6.4] J. A. Garrido, C. E. Nebel and M. Stutzmann, "Capacitance-voltage studies of Al-Schottky contacts on hydrogen-terminated diamond," *Applied Physics Letters*, vol. 81, no. 4, pp. 637-639, 2002

[6.5] M. Kubovic, M. Kasu, Y. Yamauchi, K. Ueda and H. Kageshima, "Structural and electrical properties of H-terminated diamond field-effect-transistor," *Diamond and Related Materials*, vol. 18, no. 5-8, pp. 796-799, 2009

[6.6] M. Kasu, K. Ueda, H. Kageshima and Y. Yamauchi, "Gate interfacial layer in hydrogen-terminated diamond field-effect transistors," *Diamond and Related Materials*, vol. 17, no. 4-5, pp. 741-744, 2008

[6.7] D. A. J. Moran, O. J. L. Fox, H. McLelland, S. Russell and P. W. May, "Scaling of hydrogen-terminated diamond FETs to sub-100-nm gate dimensions," *IEEE Electron Device Letters* vol. 32, no. 5, pp. 599-601, 2011

[6.8] B. Pasciuto, W. Ciccognani, E. Limiti, P. Calvani, M. C. Rossi and G. Conte, "Modelling of metal-semiconductor field-effect-transistor on H-terminated pollycrystalline diamond," *10th International Conference on Ultimate Integration of Silicon*, pp. 261-264, 18-20th March 2009

[6.9] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook and S. E. Coe, "Diamond FET using polycrystalline diamond with f_T of 45 GHz and f_{MAX} of 120 GHz," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 570-572, 2006

[6.10] K. Hirama, H. Takayanagi, Y. Yamauchi, Y. Jingu, H. Umezawa and H. Kawarada, "High-performance p-channel diamond MOSFETs with alumina gate insulator," *IEDM Technical. Digest*, pp. 873–876, 2007

[6.11] S. A. O. Russell, S. Sharabi, A. Tallaire and D. A. J. Moran, "Hydrogen-terminated diamond field effect transistors with cut-off frequency of 53 GHz", *IEEE Electron Device Letters* vol. 33, no. 10, pp. 1471-1473, 2012

[6.12] M. Kasu, K. Ueda, Y. Yamauchi, A. Tallaire and T. Makimoto, "Diamond-based RF power transistors: Fundamentals and applications," *Diamond and Related Materials*, vol. 16, no. 4-7, pp. 1010-1015, 2007

[6.13] M. Kasu, H. Sato and K. Hirama, "Thermal stabilization of hole channel on H-terminated diamond surface by using atomic-layer-deposited Al_2O_3 overlayer and its electric properties," *Applied Physics Express*, vol. 5, pp. 025701-1-025701-3, 2012

[6.14] T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto and K. Maezawa, "A study on current collapse in AlGaN/GaN HEMTs induced by bias stress," *IEEE Transactions on Electron Devices*, vol. 50, no. 10, pp. 2015-2020, 2003

7. Preliminary Investigations into Alternative Device Design

The research shown so far throughout this thesis highlights the potential of diamond as an electronic material. Although some of the best device results yet seen for diamond have been shown in this work, the need for an alternative fabrication method to the conventional atmosphere exposed surface channel FET has also been consistently highlighted. This will lead to a more stable, repeatable and perhaps one day commercial set of devices as well as to fulfil diamond's potential as a substrate for high power electronic devices.

The greatest fabrication challenge in this work comes from the Au etch process used to create ohmic contacts. It is necessary to protect the hydrogen-termination beneath, however the etch is far from ideal and Au does not adhere to hydrogen-terminated diamond at all well so the most obvious route to improving the repeatability of these devices is to eliminate this Au etch process. Attempts at this were made and are presented in this chapter including the use of an 'inverse process' with an Al sacrificial layer and using an alternative ash with a non-oxygen containing SF_6 gas mixture.

The atmosphere exposed diamond surface itself is also non-ideal and a big factor in the instability of FETs. Two routes to encapsulating this were attempted both with moderate success as well as trying to find an alternative electron accepting material to replace the atmospheric particles all together which has shown substantial promise.

7.1 Alternative Fabrication Procedures

When investigating an alternative to the traditional Au sacrificial layer with its subsequent etch to produce ohmic contacts, one place to begin is attempting an inverse process whereby an Al sacrificial layer is deposited first to protect the surface and subsequently etched back in the same manner although to produce gate features instead of the ohmic contact as seen in Figure 7.1.1.

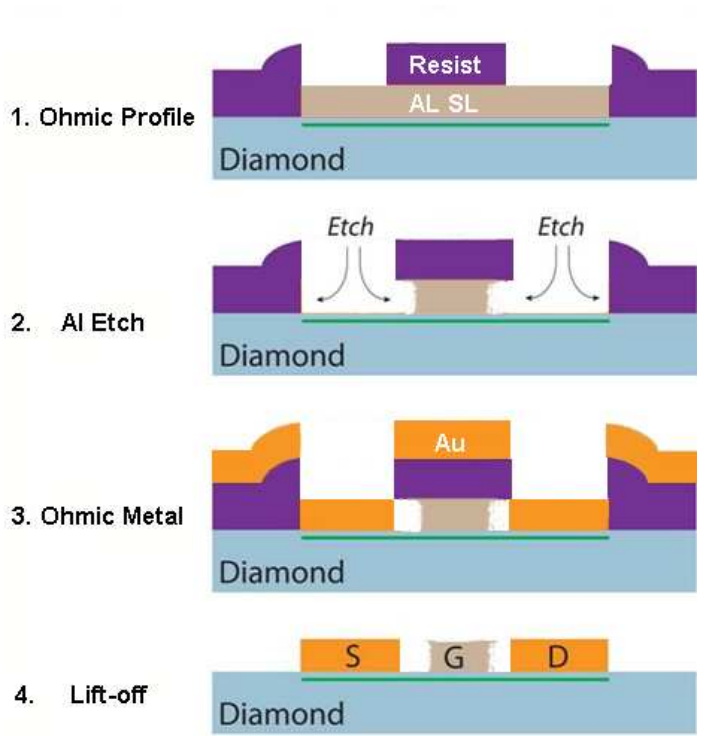


Figure 7.1.1: Inverse Al SL process

The success of this method relies on a number of factors, namely the ability to produce a lower roughness contact edge than is possible with Au, especially as small gate features are desirable. The nature of the Al etch and if it adversely affects the sub-surface conductivity will also be crucial.

The Al etch was performed using the same MF CD-26 developing solution as is used to remove the Al charge dissipation layer subsequent to electron beam lithography. An initial investigation was undertaken with a 1 minute etch on a CV structure as this has a relatively

large gate area. Etching showed that although the edge roughness may be slightly smoother than its Au counterpart it is not significantly so. It can be seen via inspection of the SEM images in Figures 7.1.2 and 7.1.3 that metal edge roughness is still present and of the order of ~100 nm. It should also be noted this etch appears to leave significant re-deposition of material even with a thorough rinse with RO water. Hence with any improvement over the Au etch being marginal at best along with the process seeming to complicate rather than simplify matters it was quickly discarded.

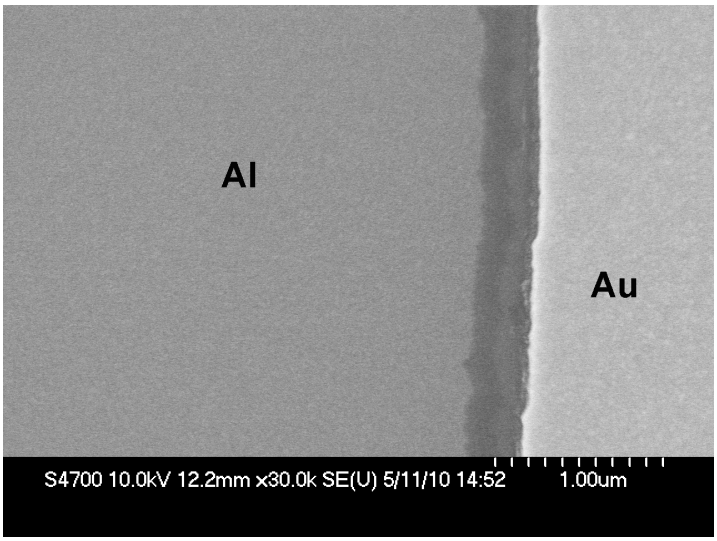


Figure 7.1.2: Al etch on diamond with re-deposition clearly visible

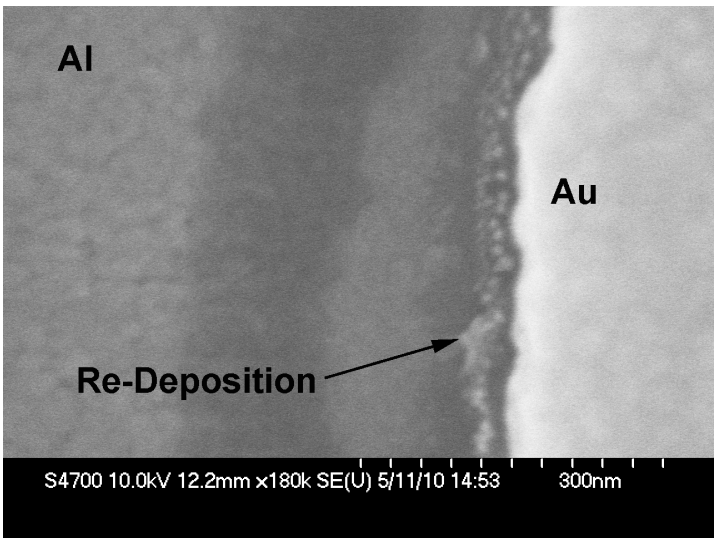


Figure 7.1.3: Zoomed in Al etch on diamond with re-deposition clearly visible

One method of potentially achieving reduced roughness and anisotropic metal etch profiles is by using a dry etch technique. This raises the question is there a gas chemistry which will produce the desired result of etching the Al without damaging the hydrogen-termination of the diamond and degrading the sub-surface conductivity? This to the author's knowledge has yet to be discovered.

Another potential route to avoid the use of an Au sacrificial layer is to use an alternative plasma ashing technique to the process mentioned in Section 3.4, which does not contain oxygen as this would remove the necessity to etch any metals. Instead resist could be spun directly on to the diamond surface, developed and ashed with this gas prior to metal deposition assuming that no significant damage is caused by high energy electrons to the surface termination during lithography. This potential process is illustrated in Figure 7.1.4.

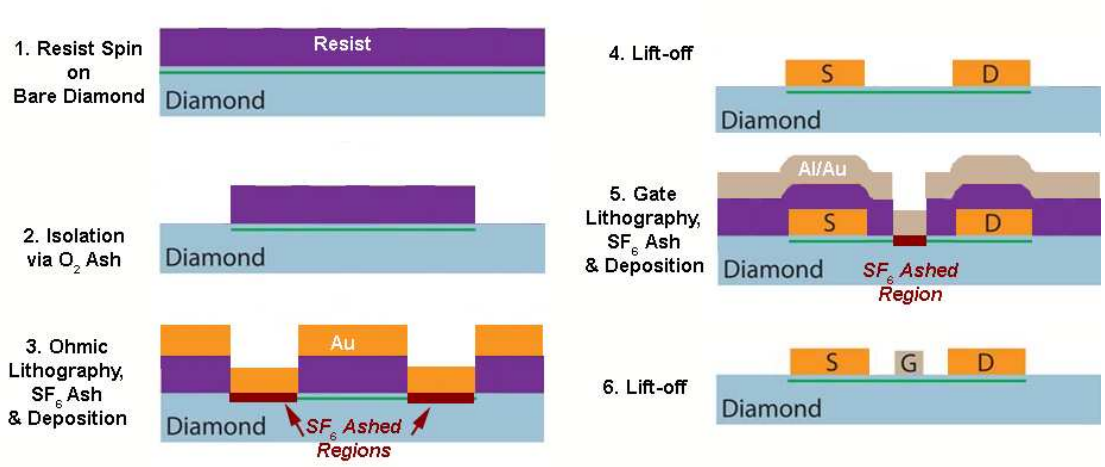


Figure 7.1.4: Alternative ash process

A possibility is to use sulphur hexafluoride (SF_6) as it is a mild etch used in silicon processing to give anisotropic profiles at relatively low temperature and pressures [7.1]. It does not contain oxygen so should not lead to oxygen-termination of the diamond surface. To test this ashing technique some TLM structures were fabricated on the bare hydrogen-terminated diamond surface (i.e. without an Au sacrificial layer) using an SF_6 ash and standard lift-off to produce smooth ohmic contact edges. The parameters for the SF6 ash were unchanged from the standard low power oxygen ash (1 minute at 40 Watts) so as to give a comparison between the two.

Figure 7.1.5 shows the results of DC measurement of these SF_6 ashed TLMs. There is clearly very little current present and where we would usually expect to see hundreds of mA instead there is only a fraction of a μA so something in this method has almost completely destroyed the sub-surface conductivity or somehow left the charge carriers immobile. This highlights just how delicate this surface transfer doping effect is. It is impossible to decouple whether the conductivity is destroyed due to a reaction between the diamond surface and the gas mixture (it is possible fluorination of the diamond surface may have occurred which although still under debate is believed to give the surface a positive electron affinity much like oxygen-termination), coating the bare diamond with resist or electron beam damage [7.2]. Further experiments should look in to decoupling these as although unsuccessful, this method with a suitable gas mixture may provide an efficient method of improving the yield of the fabrication process and would address many of the issues currently associated with fabricating surface channel diamond FETs.

Due to the limited amount of diamond material available for experimentation, other parameter SF_6 ashes were not attempted here, as the initial results of this experiment were particularly damaging to the sub-surface conductivity it was decided a method of encapsulation was a sensible way forward.

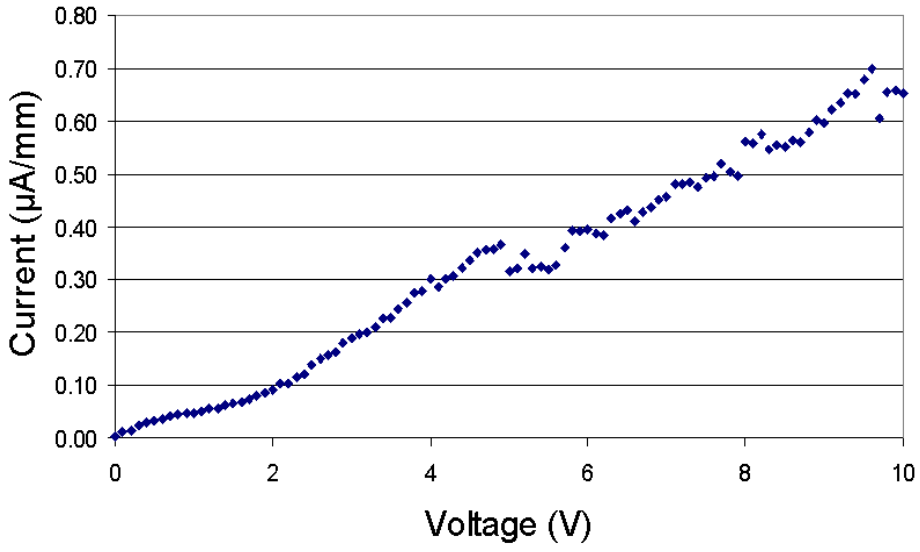


Figure 7.1.5: TLM measurement for 1 μm gap after SF6 Ash for 1 minute at 40 Watts

7.2 Organic Coating

There is an obvious need for a passivation layer to encapsulate finished diamond devices to try and prevent performance degradation. In recent years there has been a growing consensus that organic materials such as C_{60}, $C_{60}F_{48}$ and F_4-TCNQ may induce sub-surface conductivity as well as or even better than the traditional atmospheric particle method and may also be more stable [7.3-7.4]. Some preliminary research was thus performed to investigate these claims further as so far published data focuses on purely simulations, material characterisation, spectroscopic data and in-situ conductivity measurements with little in the literature to date in regards to organic surface accepting materials and their incorporation into devices.

An organic material worth consideration that is overlooked yet already universally used to coat diamond for processing is electron beam resist. Following from the alternative SF_6 ash experiment, poly(methyl methacrylate) (PMMA) electron beam resist (which is used for electron-beam lithography pattern transfer throughout this work) was spin-coated over an already fabricated TLM and any degradation of the current through it was measured to decouple one variable from the many discussed in the previous section as well as finding out if it can in fact provide a stable encapsulation to the surface. Three TLM measurements were taken on previously fabricated and atmosphere exposed structures initially to check the resistance values were stable as 6 months had passed since the previous measurement. Measurement was then taken immediately after coating the TLM structure with resist by probing through the resist layer. A following measurement was performed after the resist was removed with a warm acetone soak and the TLMs left to acclimatise in atmosphere for 24 hours. Figure 7.2.1 displays these measurements graphically while the sheet and contact resistances for each measurement with associated errors can be seen in Table 7.2.1. It should be noted the sample was baked to 120° C after each resist layer deposition to mimic the standard process, this should be considered when analysing the results.

	Sheet Resistance (kΩ/□)	Contact Resistance (Ω.mm)
Original	10.3 (± 2.0)	5.7 (± 1.3)
After 6 Months	14.4 (± 0.40)	6.38 (± 0.71)
With PMMA Coating	24.5 (± 1.80)	9.00 (± 3.26)
After PMMA Removal	16.0 (± 1.20)	2.22 (± 1.22)
Two Days After Removal	16.0 (± 1.20)	2.22 (± 1.22)

Table 7.2.1: TLM resist measurement summary

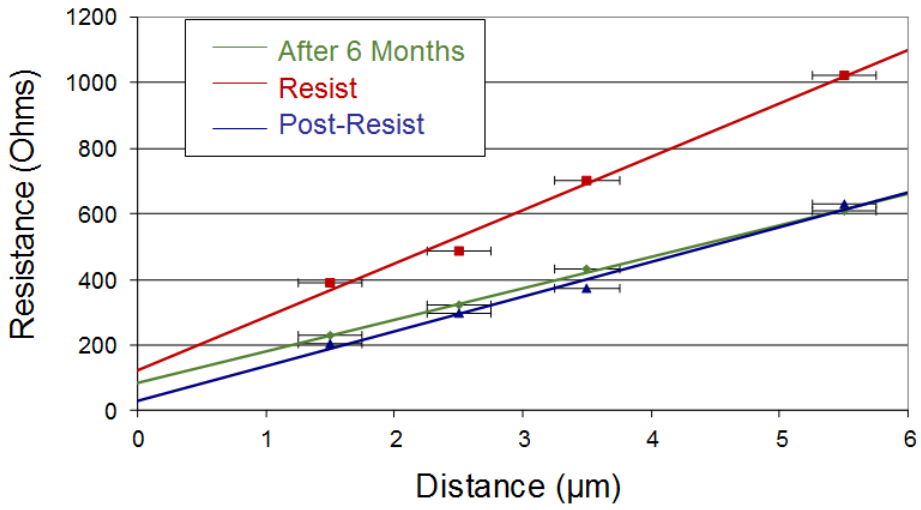


Figure 7.2.1: TLM resist comparison measurements

The results show an increased sheet resistance from 10.3 kΩ/□ obtained 6 months previously to 14.4 kΩ/□. The contact resistance also sees some slight increase. There is some debate over the degradation with time of atmospheric induced sub-surface conductivity. Popular consensus appears to suggest that there is no degradation of the sub-surface conductivity with time [7.5]. Although some believe there is slight degradation thought to be due to partial oxidation of the diamond surface with time [7.6]. This result appears to support the latter observation.

The PMMA resist bi-layer coating along with subsequent bake clearly has an impact with the sheet resistance almost doubling and contact resistance also seeing significant increase.

The change in contact resistance should only be attributed to the resist bake as the PMMA should not interact with the region beneath the contact. The increase in sheet resistance however is likely related to the coating of the exposed areas and shows that although surface transfer doping still exists in some reduced form, this organic coating clearly hampers its efficiency. Even after being left for two days to recover from the bake the TLM measurements yielded the same results.

Once the PMMA is removed, the sheet resistance almost fully recovers showing that the atmospheric adsorbate molecules are able to re-attach although perhaps to a slightly lesser extent due to potential resist residue still being present. The large decrease in contact resistance is unexplained however it should be noted these measurements are susceptible to large errors as seen in Table 7.2.1 and discussed previously.

Copper Phtalocyanine Electron Acceptors

Recent experiments using copper phtalocyanine (CuPc) have shown its inability to induce surface transfer doping on a hydrogen-terminated diamond surface due to having too low an electron affinity (2.7 – 2.9 eV) [7.4]. Much like C_{60}, a fluorinated form of this material exists known as copper hexadecafluorophtalocyanine (F_{16}CuPc) which possesses a higher electron affinity than CuPc. Due to its higher electron affinity (4.7 – 5.0 eV), F_{16}CuPc is more likely to be more efficient than CuPc at inducing the sub-surface conductivity and has already seen success in organic electronics [7.7]. The chemical structure of both these organic compounds is shown in Figure 7.2.2.

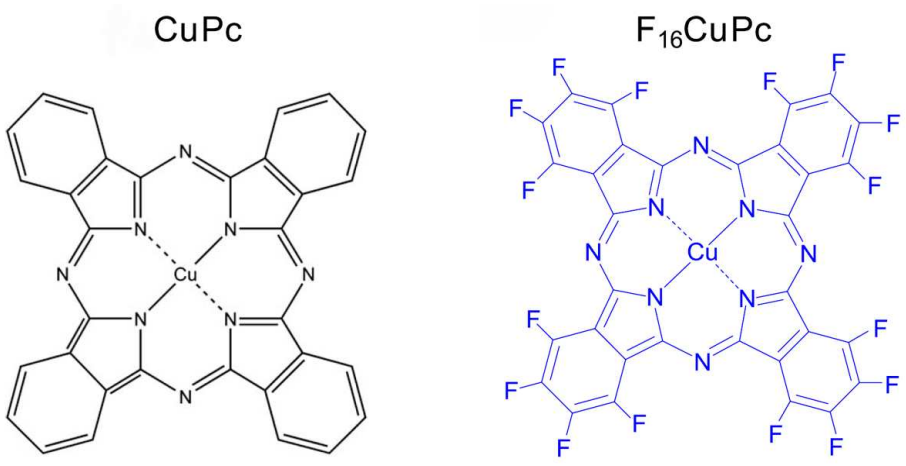


Figure 7.2.2: Chemical structure of CuPc and its fluorinated counterpart F_{16}CuPc

Similar to coating the already fabricated TLM structures with PMMA resist, 100 nm of F_{16}CuPc was deposited on to some 'fresh' TLM structures (i.e. no resist history) on a sample via thermal evaporation with the substrate not intentionally heated although somewhat susceptible to the temperature change in the evaporation chamber (~200° C). Several TLM measurements from these structures are summarised below in Figure 7.2.3 as well as resistance values presented in Table 7.2.2, all measurements were performed on the same apparatus.

	Sheet Resistance (kΩ/□)	**Contact Resistance (Ω.mm)**	**Time Since Deposition**
Before Deposition	12.2 (± 0.85)	9.12 (± 1.69)	0
After Deposition	16.9 (± 1.08)	10.50 (± 2.15)	30 minutes
After Recovery	13.9 (± 0.77)	8.17 (± 1.53)	2 days
Before Bake	13.9 (± 0.77)	8.17 (± 1.53)	7 days
After Bake	31.9 (± 0.80)	10.20 (± 1.59)	7 days
After Recovery	21.8 (± 1.00)	8.36 (± 1.96)	9 days

Table 7.2.2: TLM F_{16}CuPc measurement summary

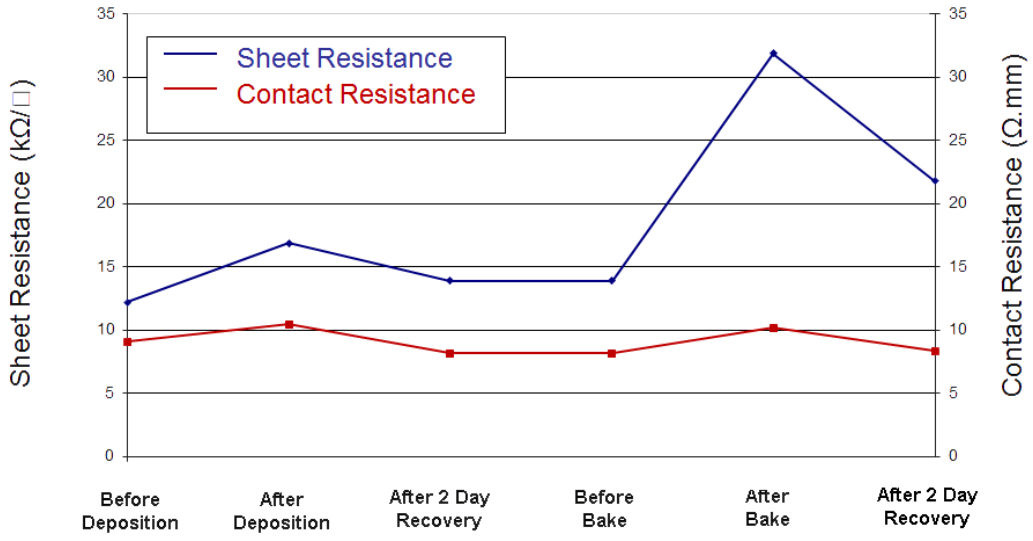


Figure 7.2.3: Access resistances for TLM encapsulated with F_{16}CuPc after various processing conditions

Prior to F_{16}CuPc deposition, the original TLM measurement gave a sheet resistance of 12.2 kΩ/□ although contact resistance is relatively high at 9.12 Ω.mm which should be kept in mind for the following results. After F_{16}CuPc deposition the sample was removed from the deposition chamber and the TLMs were re-measured (within 30 minutes after deposition) giving an increased sheet resistance of 16.9 kΩ/□ and increased contact resistance of 10.5 Ω.mm. Although no intentional substrate heating took place during the deposition it is likely that unintentional heating occurred due to the heat of the thermal evaporation up to 200° C. Two days later another measurement was performed this time yielding sheet resistance of 13.9 kΩ/□ and contact resistance 8.17 Ω.mm. These figures do not quite match the original measurements but do suggest a slight recovery of the sub-surface conductivity does occur.

This result is similar to that seen with PMMA deposition where surface transfer doping is diminished by its initial encapsulation although not to the same extent here as with the PMMA. There are two possibilities here: either the F_{16}CuPc is instigating surface transfer doping in combination with the residual atmospheric particles present on the surface or at the very least it is encapsulating the atmospheric adsorbate molecules in a far more efficient manner than PMMA.

A week after the deposition another measurement was taken which confirmed identical results to the previous measurement taken two days after F_{16}CuPc deposition suggesting a stabilization of the TLM characteristics. Immediately after this the sample was baked on a 180° C hot plate and immediately re-measured with the sheet resistance more than doubling to 31.9 kΩ/□ and contact resistance also increasing to 10.2 Ω.mm. Even after a two day recovery period following heating of the sample, the sheet resistance did reduce but still remained relatively high at 21.8 kΩ/□ with contact resistance reducing slightly to 8.36 Ω.mm.

This suggests that if the F_{16}CuPc is indeed instigating surface transfer doping then it is not stable on the surface and hence is not necessarily any more worthwhile a pursuit than the atmospheric adsorbate molecules. There are some positives to note in these results however. The initial deposition clearly did not impede the sub-surface conductivity to an extent that it would be unfeasible to incorporate this process in to FET devices. It may be possible to encapsulate the F_{16}CuPc layer with another material so surface transfer doping

is preserved by the 100 nm $F_{16}CuPc$ coating which is in turn encapsulated by a suitable dielectric although this thick multi-layer stack may prove problematic if an FET gate was intended to be placed on top.

Future work in this area should look into deposition of the $F_{16}CuPc$ material on to hydrogen-terminated diamond surface baked to above 300° C and kept under vacuum to ensure all the atmospheric particles are removed from the surface prior to deposition and then see if it is capable of inducing surface transfer doping by itself [7.8]. Unfortunately this substrate heating capability was not available on the thermal evaporator used for this $F_{16}CuPc$ work. It is possible that the $F_{16}CuPc$ just acted to encapsulate the atmospheric particles already present on the surface or even that the $F_{16}CuPc$ layer is porous to these atmospheric particles. This may explain the lack of a full recovery in the sheet resistance after heating.

7.3 Transition Metal Oxide Coating

Although various inorganic coatings have been deposited on to hydrogen-terminated diamond in an attempt to stabilise their conductivity they have as yet involved relatively low electron affinity materials such as AlN and Al_2O_3 [7.9-7.10].

As explained in Section 2.4 it is thought that an inorganic material with a high enough electron affinity material could induce surface transfer doping at the hydrogen-terminated diamond surface in the same way various organics have been shown to with the added benefit that inorganic materials tend to be far less volatile in atmosphere. There are many candidate materials which may be tried such as but not exclusively CrO_3, V_2O_5, WO_3, TiO_2 etc. The energy band levels of some of these candidates is illustrated in Figure 7.3.1. Here we have opted for MoO_3 due to its high electron affinity, low reactivity, ease of deposition (via thermal evaporation) and knowledge of prior success as an electron acceptor material in organic electronic systems [7.11].

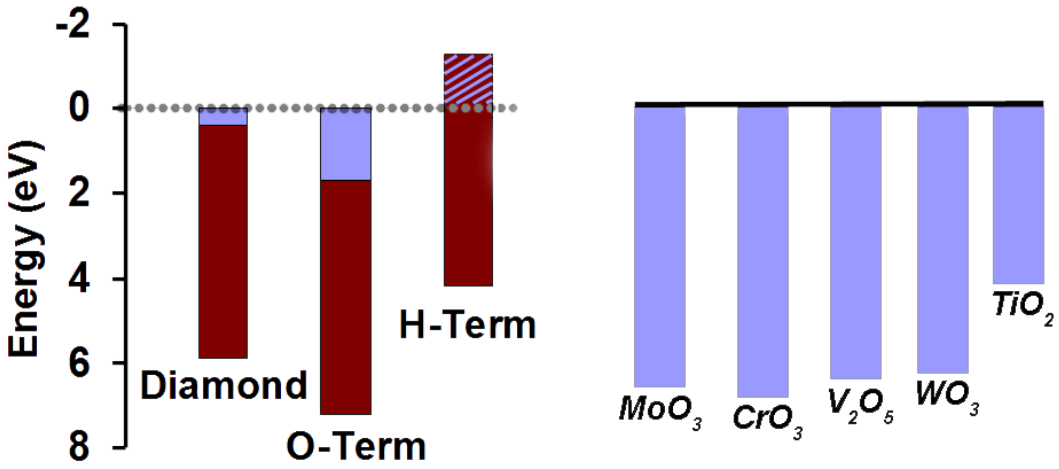


Figure 7.3.1: Comparison of transition metal oxide electron affinities (right) with diamond energy band levels as seen in Section 2.2 [7.12]

A similar experiment to that using $F_{16}CuPc$ was performed with deposition of 100 nm of MoO_3 on to readily fabricated fresh TLM and VDP structures on a single crystal sample. Again no intentional substrate heating was performed so possible encapsulation of atmospheric particles may have occurred.

A second single crystal sample was prepared at a later date and sent to the National University of Singapore to gain insight through both high energy x-ray photoelectron spectroscopy (XPS) and lower energy ultraviolet light (UPS) into in-situ surface transfer doping using MoO_3. It had a 1 μm thick epitaxial layer grown on top by collaborators at Université Paris 13, lightly doped with boron to enable the XPS measurement before subsequent acid clean and hydrogen-termination procedures as discussed in Section 3.1. In contrast to the electrical test sample, this sample was annealed at a temperature ~ 437° C in vacuum immediately prior to MoO_3 deposition to ensure removal of any residual atmospheric material. Both are shown in Figure 7.3.2.

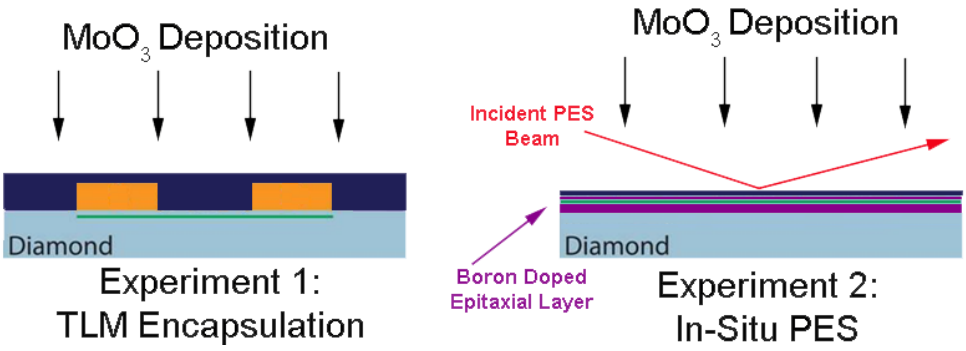


Figure 7.3.2: Dual MoO_3 Experiments

The TLM encapsulation experiment much like the $F_{16}CuPc$ deposition showed promising results as summarised in Table 7.3.1 and presented in Figure 7.3.3.

	Sheet Resistance (kΩ/□)	**Contact Resistance (Ω.mm)**
Before Deposition	15.8 (± 0.12)	8.21 (± 0.23)
After Deposition	11.3 (± 0.27)	5.86 (± 0.49)
After 1 Day Recovery	11.7 (± 0.49)	6.43 (± 0.87)

Table 7.3.1: TLM MoO_3 measurement summary

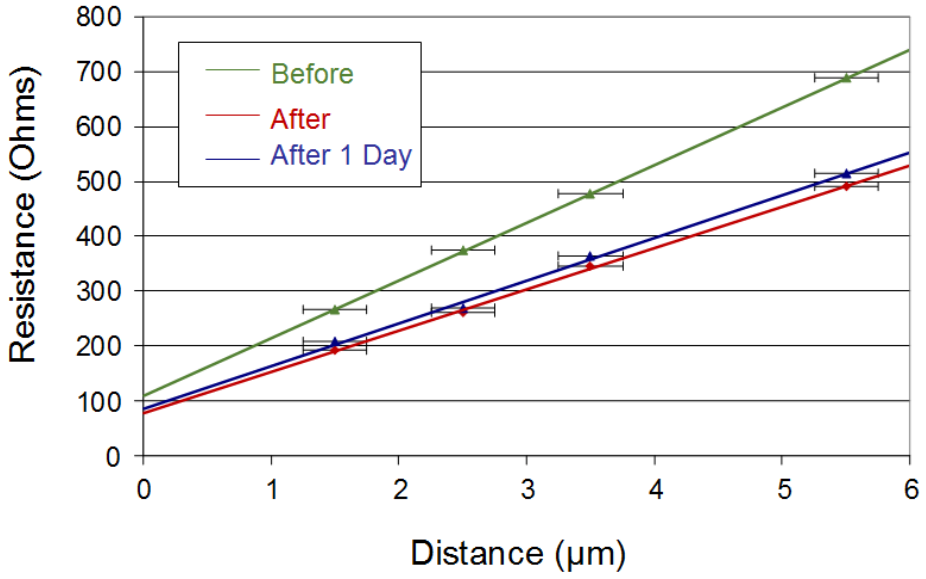


Figure 7.3.3: TLM MoO_3 comparison measurements

An original sheet resistance value of 15.8 kΩ/□ was measured and improved to 11.3 kΩ/□ after deposition of MoO_3 along with a somewhat unexplained reduction of the contact resistance from 8.21 Ω.mm to 5.86 Ω.mm. The improvement in sheet resistance is still clearly visible after 1 day so this does indeed seem to be promoting surface transfer doping very well. However after a day the current-voltage characteristics became slightly more Schottky in nature making TLM measurements unreliable and suggesting a significant increase in the sheet resistance (assuming the contact resistance didn't change over time) possibly due to a gradual interaction between atmospheric particles under the coating and the MoO_3 itself.

Again with future experiments it will be essential to instigate a pre-deposition bake in vacuum of at least over 300° C for similar TLM encapsulation experiments to decouple whether the MoO_3 is indeed inducing surface transfer doping by itself. In this preliminary experiment, it was unknown as to whether the Au ohmic contacts would be degraded by this high temperature anneal, which was therefore avoided at this stage.

The VDP characterisation done in parallel with TLM measurements can perhaps shed some light on how this degradation manifests. Table 7.3.2 summarises VDP measurements taken over the course of 4 weeks along with Figure 7.3.4 presenting this in graphical form.

	Carrier Concentration ($x\ 10^{12}\ cm^{-2}$)	**Sheet Resistance (kΩ/□)**	**Mobility ($cm^2/V.s$)**
Before Deposition	3.63	13.5	130
After Deposition	9.88	9.75	63.2
1 Day After Deposition	7.66	10.0	81.6
4 Days After Deposition	8.64	10.1	71.2
1 Week After Deposition	7.36	9.42	90.2
2 Weeks After Deposition	5.15	14.2	85.1
1 Month After Deposition	3.29	15.5	123

Table 7.3.2: VDP MoO_3 measurement summary

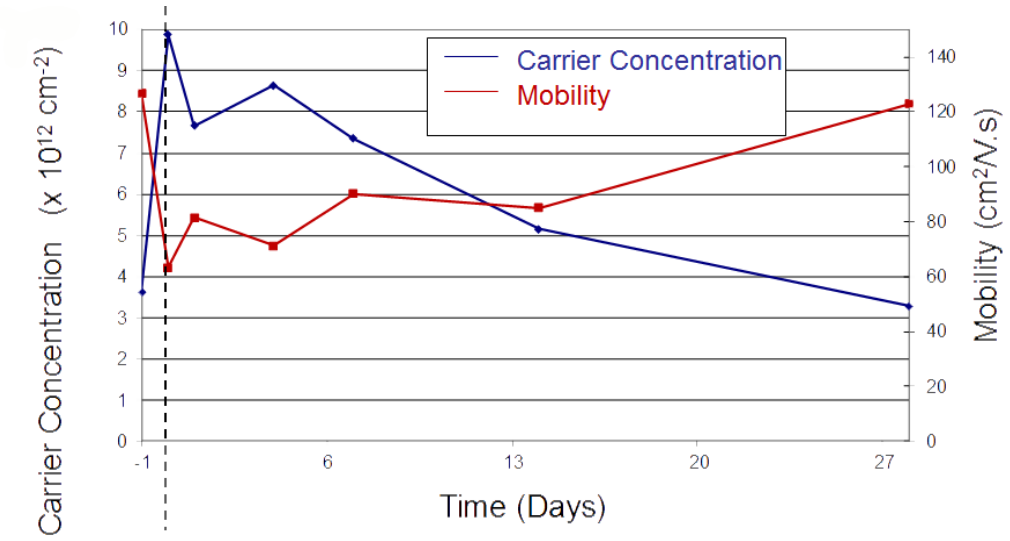


Figure 7.3.4: VDP MoO_3 comparison measurements

It is clear that deposition of the MoO_3 lead to a significant increase in carrier concentration with the figure almost trebling from 3.63 x 10^{12} to 9.88 x 10^{12} cm^{-2} leading to a reduced sheet resistance and mobility. This strongly suggests that MoO_3 is increasing the efficiency of surface transfer doping even if it is impossible to separate its contribution conclusively from the atmospherically induced process in this experiment which does not include a pre-deposition bake. To ensure parallel conduction was not occurring through the MoO_3 a sample of silicon dioxide (SiO_2) was used to also deposit 100 nm of MoO_3 onto and measured simultaneously via two probes placed within a few µm. This registered no current, just noise suggesting no conduction through the MoO_3. Over the course of the next month further measurements were taken and the three measured values gradually returned to approximately their pre-MoO_3 values over this time, suggesting once again either a slow reaction between adsorbate molecules and MoO_3 takes place or the MoO_3 is porous to the atmospheric molecules gradually reducing the values back to an equilibrium. The likelihood of this process could be further investigated by depositing an additional capping layer material onto the MoO_3.

The second sample used for XPS involved deposition of MoO_3 after a 437° C pre-deposition bake was performed in vacuum so as to remove any atmospheric particles from the surface and attempt to induce surface transfer doping by the MoO_3 alone. The substrate

was then cooled to room temperature and then kept there during deposition so as to avoid stress on the MoO_3 film upon cooling. Figure 7.3.5 shows the C 1s carbon binding energy peak as measured by XPS in Singapore for the clean diamond surface with a sharp characteristic sp^3 peak visible at 284.2 eV for an incident photon energy of 350 eV. This can be seen to significantly shift the binding energy (BE) upon deposition of MoO_3 by ~ 1 eV until it is no longer visible after 3.2 nm film coverage due to the XPS only capable of measuring the surface of a sample and the MoO_3 masking the diamond by this point. The 1 eV shift seen in the C 1s peak is indicative of band bending at the diamond surface associated with transfer of electrons as part of the surface transfer doping process.

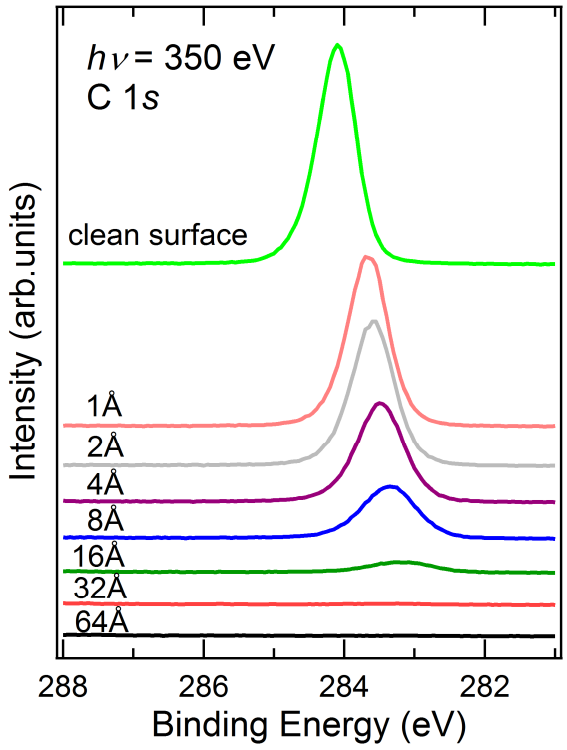


Figure 7.3.5: C 1s binding energy peak shift as measured by XPS during MoO_3 deposition

Figure 7.3.6 shows the Mo 3d binding energy peaks (two are visible due to spin-orbit coupling associated with the d core level) and the relative intensity upon increasing deposition of MoO_3 material. Note there is an increase in intensity but no significant shift suggesting no substantial band bending in the MoO_3 surface layer. It should also be noted XPS shows relative amounts of atoms not absolute values and is not entirely conclusive as it is unable to detect small atoms such as H via the system although it can give a good idea

of the relative composition of the surface. This is why the y-axis is arbitrary units and not an absolute value.

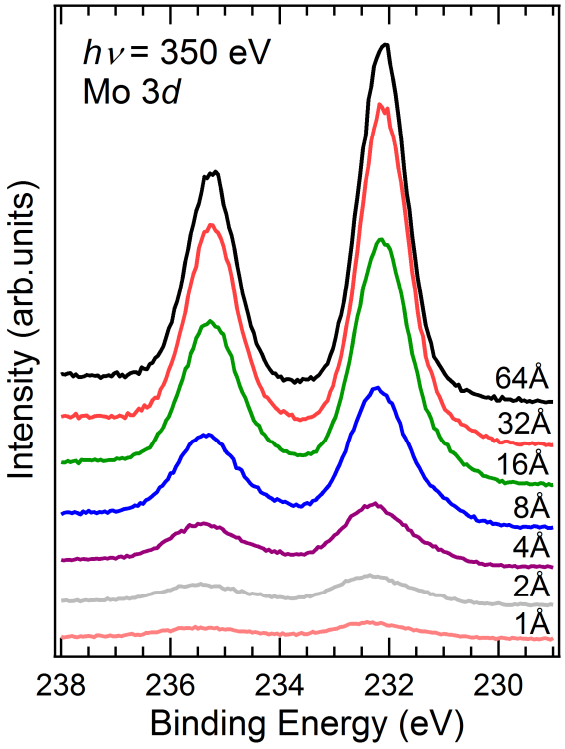


Figure 7.3.6: Mo 3d binding energy peak as measured by XPS during MoO3 deposition

Figure 7.3.7 shows UPS spectra with incident radiation of 60 eV allowing the valence level to be probed and the low kinetic energy (KE) part of the spectra displayed. The low energy cut-off for the KE shows the vacuum level position or in this case where the energy scale is referenced to the Fermi Level the work function of the diamond surface. Before MoO_3 deposition the work function is ~ 4 eV as should be expected from a hydrogen-terminated diamond surface with a sharp emission peak present due to the surface NEA. Upon deposition the work function increases rapidly until ~ 1.6 nm is deposited and a shift of ~ 3 eV has occurred. This shift is related to the interface dipole initiated by charge separation along with band bending at the diamond surface.

The work function shift can be seen more clearly in Figure 7.3.8 along with the shift in BE from the C 1s core spectra associated with upwards band bending due to hole accumulation in the diamond at the interface.

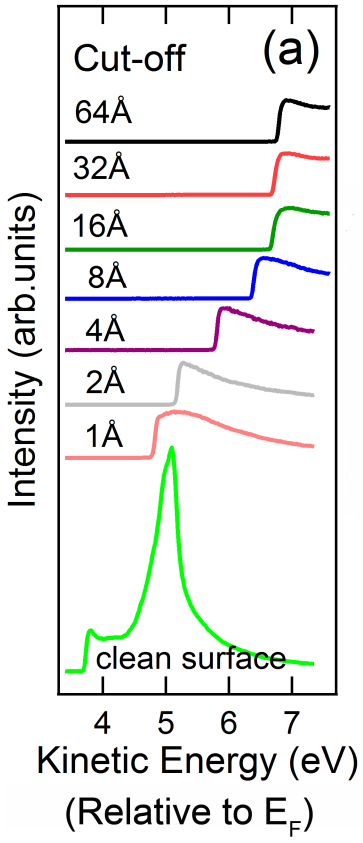


Figure 7.3.7: Low Energy UPS spectra showing K.E. spectra during MoO_3 deposition

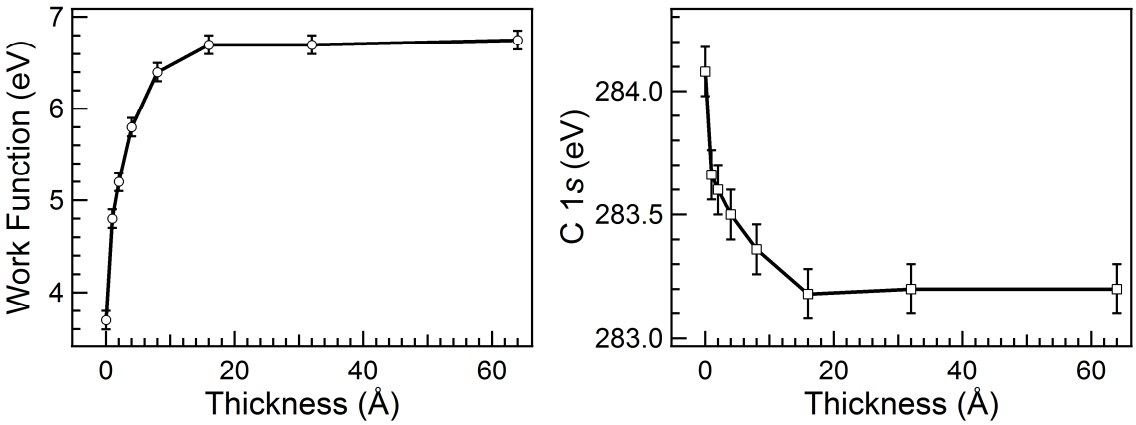


Figure 7.3.8: Shift in work function and C 1s associated with MoO3 deposition

This data shows that MoO_3 is sufficient alone to induce surface transfer doping in diamond and while further research will need to be done to ensure this provides a suitable and stable alternative to the atmospheric process all signs thus far are positive. While we cannot draw definitive conclusions from the VDP measurements as it is possible that atmospheric particles remain on the surface along with MoO_3. We can conclude that the MoO_3 deposition certainly does not hinder carrier transport but in fact it acts to improve it, at least temporarily as observed in this as yet unoptimised experiment. With the significant shift seen in the XPS and UPS spectra it is plausible MoO_3 could cause accumulation layers of concentrations ~ 1 x 10^{14} which is comparable to the best values achieved for hydrogen-terminated diamond to date [7.9]. Again to fully verify this electrically, TLM/VDP measurements should be performed after deposition of a MoO_3 layer following a high temperature anneal to ensure removal of any atmospheric based residue.

Another positive to note from this process is the shifts in XPS and UPS spectra all appear to saturate by 1.6 nm of deposition which is very beneficial if FET devices are to be eventually made from this technology, as an extra 1.6 nm spacing between gate contact and drain should not diminish the transconductance of devices a great deal.

7.4 Summary

Following on from the device results of the last chapter and the need for a paradigm shift in diamond FET fabrication to continue to improve device figures of merit, an initial investigation was undertaken to this end.

Beginning by trying the same basic principles of fabrication on the volatile surface but substituting conventional fabrication techniques with other alternative methods little progress was made. However when it came to trying to change the surface and maximise its potential via incorporation of new materials, some very promising initial results were achieved. Several as before untested materials were deposited on to the diamond surface, both organic and inorganic in nature. Again a fluorinated molecule ($F_{16}CuPc$) shows the potential to electrically match other proven materials such as $C_{60}F_{48}$ and F_4-TCNQ along with an inorganic material in the form of MoO_3 being electrically and spectrographically tested for the first time.

The crucial next stage in development of this technology will be to electrically characterise TLM and VDP structures which have had a pre-deposition anneal to drive off atmospheric molecules prior to electron acceptor material deposition. This will reveal critical information on the potential to integrate these materials into FET devices.

References:

[7.1] R. Legtenberg, H. Jansen, M. De Boer and M. Elwenspoek, "Anisotropic reactive ion etching of silicon using $SF_6/O_2/CHF_3$ gas mixtures," *Journal of the Electrochemical Society*, vol. 142, no. 6, pp. 2020-2028, 1995

[7.2] K. J. Rietwyk, S. L. Wong, L. Cao, K. M. O'Donnell, L. Ley, A. T. S. Wee and C. Pakes, "Work function and electron affinity of the fluorine terminated (100) diamond surfaces," *Applied Physics Letters*, vol. 102, no. 9, pp. 091604-1-091604-3, 2013

[7.3] L. Ley, J. Ristein, F. Meier, M. Riedel and P. Strobel, "Surface conductivity of the diamond: A novel transfer doping mechanism," *Physica B*, vol. 376-377, pp. 262-267, 2006

[7.4] W. Chen, D. Qi, X. Gao and A. T. S. Wee, "Surface transfer doping of semiconductors," *Progress in Surface Science*, vol. 84, no. 9-10, pp. 279-321, 2009

[7.5] K-S. Song and H. Kawarada, "Characteristics of diamond electrolyte solution-gate FETs (SGFETs) and applications to biosensor," *New Diamond and Frontier Carbon Technology*, vol. 15, no. 6, pp. 325-335, 2005

[7.6] G. R. Salazar-Banda, L. S. Andrade, P. A. P. Nascente, P. S. Pizani, R. C. Rocha-Filho and L. A. Avaca, "On the changing electrochemical behaviour of boron-doped diamond surfaces with time after cathodic pre-treatments," *Electrochemical Acta*, vol. 51, no. 22, pp. 4612-4619, 2006

[7.7] J. L. Yang, S. Schumann, R. A. Hatton and T. S. Jones, "Copper hexadecafluorophtalocyanine (F_{16}CuPc) as an electron accepting material in bilayer small molecule organic photovoltaic cells)," *Organic Electronics*, vol 11, no. 8, pp. 1399-1402, 2010

[7.8] F. Maier, M. Riedel, B. Mantel, J. Ristein, and L. Ley, "Origin of surface conductivity in diamond," *Physical Review Letters*, vol. 85, no. 16, pp. 3472-3475, 2000

[7.9] D. Kueck, P. Leber, A. Schmidt, G. Speranza and E. Kohn, "AlN as passivation for surface channel FETs on H-terminated diamond," *Diamond and Related Materials*, vol. 19, no. 7-9, pp. 932-935, 2010

[7.10] K. Hirama, H. Sato, Y. Harada, H. Yamamoto and M. Kasu, “Diamond field-effect transistors with 1.3 A/mm drain current density by Al_2O_3 passivation layer,” *Japanese Journal of Applied Physics*, vol. 51, no. 9, pp. 090112-1-090112-5, 2012

[7.11] M. Kröger, S. Hamwi, J. Meyer, T. Riedl, W. Kowalsky and A. Kahn, “P-type doping of organic wide band gap materials by transition metal oxides: A case-study on molybdenum trioxide,” *Organic Electronics*, vol. 10, no. 5, pp. 932-938, 2010

[7.12] M. T. Grenier, M. G. Helander, W-M. Tang, Z-B. Wang, J. Qiu and Z-H. Lu, “Universal energy-level alignment of molecules on metal oxides,” *Nature Materials*, vol. 11. Pp. 76-81, 2012

8. Conclusions and Future Work

The potential of diamond as an electronic material has been well known for over fifty years. However it is only over the last two decades it has begun to be exploited in the form of active electronic components. Initial progress in FET design was very encouraging but has somewhat stalled in recent years due to the lack of an efficient and stable doping process, with the only real success being seen from the quasi-doping effect bought about by hydrogen-termination of the diamond surface to give it NEA and subsequent exposure to a suitably high electron affinity material.

These FET devices have to date displayed high operating frequencies with a record f_T = 45 GHz and f_{MAX} = 120 GHz being seen in devices with 100 nm gate length [8.1]. Unfortunately due to the instability associated with the surface transfer doping effect due to its use of atmospheric particles, in most cases diamond is yet to reach its potential as a suitable platform for high power and high temperature electronics.

The two main aims of this research were to improve upon the already impressive frequency performance of surface channel diamond FETs (and in turn investigate their scaling potential) and to look into methods of producing a stable alternative to the atmospheric induced sub-surface conductivity. Much more has been learnt regarding the nature of surface channel FETs and the surface transfer doping effect.

Device scaling was focused upon to see if this frequency performance could be improved further. Three different gate length RF geometry FETs were produced on a single diamond sample, 250 nm and 120 nm to try and repeat and confirm previous results and then continued scaling to sub-100 nm dimensions with FET gate lengths of 50 nm being fabricated on diamond for the first time. These produced a new record f_T of 53 GHz

although f_{MAX} did not reach the same record breaking levels. One reason for this is the gate design did not involve a T-shape due to fabrication challenges.

The larger gate length devices (250 nm) produced similar results to those achieved by H. Matsudaira et *al* [8.2]. The 120 nm gate length device matched results achieved by both K. Ueda *et al* and K. Hirama *et al* for 100 nm and 150 nm respectively proving the fabrication process developed throughout this project worked and could match the very best diamond FETs produced to date [8.1, 8.3].

Although the 50 nm device did achieve unique RF performance it also showed perhaps for the first time the limits of this technology. As shown in the extracted equivalent circuit for the 50 nm device the gate capacitance and transconductance have scaled to allow for improved intrinsic frequency performance, extrinsic factors such as source and drain resistances remain the same (within error associated with the unrepeatable nature of the Au ohmic contact etch). This combined with an increase in output conductance means although the intrinsic f_T of this device has increased substantially to 90 GHz the extrinsic value of 53 GHz is only 59% of this potential value. It is expected then that further reduction of gate length would only lead to a similar marginal improvement.

All of this coupled with the instability associated with atmospheric surface transfer doping leads to the need to investigate alternative methods of fabrication to further improve upon repeatability and perhaps increase the device performance further. Some attempt was made to improve the stability of these devices during this research by modifying the fabrication procedure slightly while sticking with the atmospheric induced sub-surface conductivity. It quickly became evident that this task was not straightforward and the volatile nature of the atmospheric particles on the diamond surface and sensitivity of the hydrogen-termination leaves very little room for alternative fabrication techniques, hence the motivation for the incorporation of the Au sacrificial layer technique in the first place.

To truly improve upon the stability of this technology a different, more stable electron accepting material needs to be successfully incorporated in to the fabrication of hydrogen-terminated diamond surface channel transistors. This research took the initial work done by various groups and extended the scope of organic materials looked at so far to include both

PMMA and F_{16}CuPc. Coating TLM structures with both these organic materials managed to preserve the sub-surface conductivity to different extents [8.4-8.6].

In the case of PMMA, not known for having a high electron affinity the sheet resistance almost doubled upon deposition from 14.4 kΩ/□ to 25.5 kΩ/□ making it impractical as an encapsulation layer for diamond surface channel FETs. F_{16}CuPc on the other hand which is known to have a high electron affinity ~ 5 eV encapsulates the TLM structures leading to no significant degradation of the sheet resistance [8.7]. However upon heating to just 180° C the sheet resistance does almost treble from 13.9 kΩ/□ to 31.9 kΩ/□ and never fully recovers suggesting it is just as volatile upon the diamond surface as the atmospheric particles.

Towards the end of this project it was suggested that the search for alternative acceptor materials should be extended further to include non-organic materials of suitable electron affinity (> 4.2 eV) as they should perform the same task as their organic counterparts but with the prospect of also being relatively stable upon the diamond surface. Some preliminary tests at encapsulating TLM structures with MoO_3 which has an electron affinity of 6.7 eV have proved very promising as it not only preserved sub-surface conductivity but initially at least lead to a decrease in the sheet resistance from 15.8 kΩ/□ to 11.3 kΩ/□ [8.8].

A separate sample used for photoelectron spectroscopy to measure the energy make-up of the sample surface in-situ during MoO_3 deposition after a 400° C pre-bake to remove atmospheric particles showed all the characteristics associated with the valence band bending upward due to an accumulation of holes on the diamond side of the interface and an increase in work function. This suggests that it is highly probable MoO_3 and other inorganic materials of suitable electron affinity will instigate surface transfer doping at the hydrogen-terminated diamond surface on their own and at a very low coverage of just 1.6 nm.

Future Work

Although this research has succeeded in its two main aims it has also raised many questions for the future but fortunately there are numerous exciting routes left to explore to enhance this emerging technology. The main task still remains to completely stabilise the

hydrogen-terminated diamond surface and while using atmospheric particles for FETs appears ultimately doomed because of the inherent instability associated with them there are still other fabrication techniques which may be employed to try and improve the performance of FETs fabricated in this manner. An alternative ashing method was attempted in this research with SF_6 employed as it is a non-oxygen containing compound. Although this was unsuccessful it is feasible there is another gas mixture that could successfully remove resist particles from the diamond surface without hampering the surface transfer doping effect. If this can be found then there would be no need for an Au sacrificial layer to be employed making ohmic contacts far more controllable and repeatable along with the source-drain gap spacing.

It is clear however that ultimately Au is a fairly poor ohmic contact to use for hydrogen-terminated diamond FETs as contact resistance is at best 2 Ω.mm and can reach as high as 10 Ω.mm. There has been various research already by other groups showing the potential of carbide based contacts on diamond such as TiC or TaC to have a far lower contact resistance [8.9]. However this would involve a high temperature anneal hence requiring a whole new method of fabrication.

A host of organic materials have already been deposited on to hydrogen-terminated diamond with encouraging results yet there still remain many more to try and with inorganic materials of high enough electron affinity also now showing promise there is surely a material capable of preserving the sub-surface conductivity associated with hydrogen-terminated diamond if not enhancing it even [8.5]. This may finally let diamond truly realise its potential as an electronic material with high temperature, voltage and power operation within reach.

It is still feasible that gate length could be scaled even further below 50 nm once other issues with this technology have been resolved. Electron beam lithography at the University of Glasgow has demonstrated line features of just 3 nm and recently sub-10 nm silicon nanowires incorporating electron beam lithography and a dry etch process to give an aspect ratio ~ 50:1 [8.10-11]. Although this is by no means straightforward it just shows that the potential for further high frequency enhancement via lithographical techniques is there.

The thermal properties of diamond are well known so in terms of the maximum temperature a diamond device could eventually operate at, it is really in fact dependent on how high a temperature the acceptor material and the surface transfer doping process could cope with.

As for diamond's high power operation potential, once the surface is stable and repeat measurement of FETs can be done with ease there will be a far clearer picture of its ultimate potential.

Several groups have already performed power measurement on non-encapsulated hydrogen-terminated diamond FETs with 2 $W.mm^{-1}$ being the record output power seen to date. One prediction has suggested that diamond could eventually reach 75 $W.mm^{-1}$ although this has been suggested for boron delta-doping employing a field plate the potential of hydrogen-terminated diamond could certainly reach this and could well exceed the potential of any other wide bandgap material currently under development [8.12].

References:

[8.1] K. Ueda, M. Kasu, Y. Yamauchi, T. Makimoto, M. Schwitters, D. J. Twitchen, G. A. Scarsbrook and S. E. Coe, "Diamond FET using polycrystalline diamond with f_T of 45 GHz and f_{MAX} of 120 GHz," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 570-572, 2006

[8.2] H. Matsudaira, S. Miyamoto, H. Ishizaka, H. Umezawa and H. Kawarada, "Over 20-GHz cutoff frequency submicrometer-gate diamond MISFETs," *IEEE Electron Device Letters*, vol. 25, no. 7, pp. 480-482, 2004

[8.3] K. Hirama, H. Takayanagi, Y. Yamauchi, Y. Jingu, H. Umezawa and H. Kawarada, "High-performance p-channel diamond MOSFETs with alumina gate insulator," *IEDM Technical. Digest*, pp. 873–876, December 2007

[8.4] P. Strobel, M. Riedel, J. Ristein and L. Ley, "Surface transfer doping of diamond," *Nature*, vol. 430, no. 6998, pp. 439-441, 2004

[8.5] W. Chen, D. Qi, X. Gao and A. T. S. Wee, "Surface transfer doping of semiconductors," *Progress in Surface Science*, vol. 84, no. 9-10, pp. 279-321, 2009

[8.6] D. P. Langley, Y. Smets, C. B. Stark, M. T. Edmonds, A. Tadich, K. J. Rietwyk, A. Schenk, M. Wanke, Q. H. Wu, P. J. Barnard, L. Ley and C. I. Pakes, "Surface transfer doping of diamond with a molecular heterojunction," *Applied Physics Letters*, vol. 100, no. 3, pp. 032103-1-032103-4, 2012

[8.7] G. Shen and A. Kahn, "Role of metal-molecule chemistry and interdiffusion on the electrical properties of an organic interface: The Al-F_{16}CuPc case," *Journal of Applied Physics*, vol. 90, no. 12, pp. 6236-6242, 2001

[8.8] M. Kröger, S. Hamwi, J. Meyer, T. Riedl, W. Kowalsky and A. Kahn, "Role of the deep-lying electronic states of MoO_3 in the enhancement of hole-injection in organic thin films," *Applied Physics Letters*, vol. 95, no. 12, pp. 123301-1-123301-3, 2009

[8.9] H. J. Looi, L. Y. S. Pang, M. D. Whitfield, J. S. Foord and R. B. Jackman, "Engineering low resistance contacts on p-type hydrogenated diamond surfaces," *Diamond and Related Materials*, vol. 9, no. 3-6, pp. 975-981, 2000

[8.10] D. R. S. Cumming, S. Thoms, S. P. Beaumont and J. M. R. Weaver, "Fabrication of 3nm wires using 100 keV electron beam lithography and poly(methyl methacrylate) resist," *Applied Physics Letters*, vol. 68. No. 3, pp. 322-324, 1996

[8.11] M. M. Mirza, H. Zhou, P. Velha, X. Li, K. E. Docherty, A. Samarelli, G. Ternent and D. J. Paul, "Nanofabrication of high aspect ratio (~50:1) sub-10 nm silicon nanowires using inductively coupled plasma etching," *Journal of Vacuum Science and Technology B*, vol. 30, no. 6, pp. 06FF02-1-06FF02-7, 2012

[8.12] A. Denisenko and E. Kohn, "Diamond power devices. Concepts and limits," *Diamond and Related Materials*, vol. 14, no. 3-7, pp. 491-498, 2005

Appendix A. Fabrication Procedures

Sample Pre-Treatment/Protection via Sacrificial Layer Deposition

Substrate Cleaning:	- 5 min soak in acetone in ultrasonic bath
	- 5 min soak in IPA in ultrasonic bath
	- Blow dry with N_2 gun
Sacrificial Layer Deposition:	- Deposit 80 nm Au via e-beam evaporation

Standard Marker Deposition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Spin:	- 12% 2010 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
	- 4% 2041 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
Metallisation:	- Deposit 15 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 700 μCcm^{-2}, 64 nA beam spot size, VRU 40
Metal Etch:	- MF CD-26 soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Development:	- MIBK:IPA (1:1) soak for 30 s at 23° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Ash:	- O_2 plasma at 40 W for 60 s

Metallisation:	- Deposit 20 nm Ti/100 nm Au via e-beam evaporation
Lift-Off:	- 2 hour soak in acetone at 50° C
	- IPA rinse
	- N_2 dry

Standard Isolation/Ohmic Contact Definition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Spin:	- 12% 2010 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
	- 4% 2041 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
Metallisation:	- Deposit 15 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 700 μCcm^{-2}, 64 nA beam spot size, VRU 40
Metal Etch:	- MF CD-26 soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Development:	- MIBK:IPA (1:1) soak for 30 s at 23° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Ash:	- O_2 plasma at 40 W for 60 s
Metal Etch:	- KI_2:RO water (1:10) soak for 60 s
	- RO water rinse
	- N_2 dry
Plasma Induced Isolation:	- O_2 plasma at 40 W for 60 s
Lift-Off:	- 2 hour soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun

De-Embedding Structure Gate Pad Definition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse

	- Blow dry with N_2 gun
Resist Spin:	- 12% 2010 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
	- 4% 2041 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
Metallisation:	- Deposit 15 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 700 μCcm^{-2}, 64 nA beam spot size, VRU 40
Metal Etch:	- MF CD-26 soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Development:	- MIBK:IPA (1:1) soak for 30 s at 23° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Ash:	- O_2 plasma at 40 W for 60 s
Metallisation:	- Deposit 25 nm Al/25 nm Au via e-beam evaporation
Lift-Off:	- 2 hour soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun

250 nm Gate Contact Definition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Spin:	- 4% 2010 PMMA spun at 3k RPM for 60 s
	- 120° C bake for 20 min
	- 2.5% 2041 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
Metallisation:	- Deposit 15 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 2500 μCcm^{-2}, 8 nA beam spot size, VRU 18 (For Gate Line) - Dose 1800 μCcm^{-2}, 32 nA beam spot size, VRU 32 (For Gate Feed)
Metal Etch:	- MF CD-26 soak for 60 s
	- RO water rinse

	- Blow dry with N_2 gun
Development:	- MIBK:IPA (1:2.5) soak for 1 min at 23° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Ash:	- O_2 plasma at 40 W for 60 s
Metal Etch:	- KI_2:RO water (1:10) soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Metallisation:	- Deposit 25 nm Al/25 nm Au via e-beam evaporation
Lift-Off:	- 2 hour soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun

120 nm Gate Contact Definition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Spin:	- 4% 2010 PMMA spun at 3k RPM for 60 s
	- 120° C bake for 20 min
	- 2.5% 2041 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
Metallisation:	- Deposit 15 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 2500 μCcm^{-2}, 2 nA beam spot size, VRU 8 (For Gate Line) - Dose 1800 μCcm^{-2}, 32 nA beam spot size, VRU 32 (For Gate Feed)
Metal Etch:	- MF CD-26 soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Development:	- MIBK:IPA (1:2.5) soak for 1 min at 23° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Ash:	- O_2 plasma at 40 W for 60 s
Metal Etch:	- KI_2:RO water (1:10) soak for 60 s

	- RO water rinse
	- Blow dry with N_2 gun
Metallisation:	- Deposit 25 nm Al/25 nm Au via e-beam evaporation
Lift-Off:	- 2 hour soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun

50 nm Gate Contact Definition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Spin:	- 4% 2010 PMMA spun at 3k RPM for 60 s
	- 120° C bake for 20 min
	- 2.5% 2041 PMMA spun at 5k RPM for 60 s
	- 120° C bake for 20 min
Metallisation:	- Deposit 15 nm Al via e-beam evaporation
Electron Beam Lithography:	- Dose 2500 μCcm^{-2}, 1 nA beam spot size, VRU 5 (For Gate Line)
	- Dose 1800 μCcm^{-2}, 32 nA beam spot size, VRU 32 (For Gate Feed)
Metal Etch:	- MF CD-26 soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Development:	- MIBK:IPA (1:2.5) soak for 1 min at 23° C
	- IPA rinse
	- Blow dry with N_2 gun
Resist Ash:	- O_2 plasma at 40 W for 60 s
Metal Etch:	- KI_2:RO water (1:10) soak for 60 s
	- RO water rinse
	- Blow dry with N_2 gun
Metallisation:	- Deposit 25 nm Al/25 nm Au via e-beam evaporation
Lift-Off:	- 2 hour soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun

Acceptor Material Deposition

Substrate Cleaning:	- 20 minute soak in acetone at 50° C
	- IPA rinse
	- Blow dry with N_2 gun
Sacrificial Layer Deposition:	- Deposit 100 nm $F_{16}CuPc$ or MoO_3 via thermal evaporation