Low Power RF Transceivers

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Abstract

This thesis details the analysis and design of ultra-low power radio transceivers operating at microwave frequencies. Hybrid prototypes and Monolithic Microwave Integrated Circuits (MMICs) which achieve power consumptions of less than 1 mW and theoretical operating ranges of over 10 m are described.

The motivation behind the design of circuits exhibiting ultra low power consumption and, in the case of the MMICs**,** small size is the emerging technology of Wireless Sensor Networks (WSN). WSNs consist of spatially distributed 'nodes' or 'specks' each with their own renewable energy source, one or more sensors, limited memory, processing capability and radio or optical link. The idea is that specks within a 'speckzone' cooperate and share computational resources to perform complex tasks such as monitoring fire hazards, radiation levels or for motion tracking. The radio section must be ultra low power e.g. sub 1 mW in order not to drain the limited battery capacity. The radio must also be small in size e.g. less than 5 x 5 mm so that the overall speck size is small. Also, the radio must still be able to operate over a range of at least a metre so as to allow radio contact between, for example, rooms or relatively distant specks.

The unsuitability of conventional homodyne topologies to WSNs is discussed and more efficient methods of modulation (On-Off Keying) and demodulation (non-coherent) are presented. Furthermore, it is shown how Super-Regenerative Receivers (SRR) can be used to achieve relatively large output voltages for small input powers. This is important because baseband Op-Amps connected at the RF receiver output generally cannot amplify small signals at the input without the output being saturated in noise (10mV is the smallest measured input for 741 Op-Amp). Instrumentation amplifiers are used in this work as they can amplify signals below 1mV.

The thesis details the analysis and design of basic RF building blocks: amplifiers, oscillators, switches and detectors. It also details how the circuits can be put together to make transceivers as well as describing various strategies to lower power consumption. In addition, novel techniques in both circuit and system design are presented which allow the power consumption of the radio to be reduced by as much as 97% whilst still retaining adequate performance. These techniques are based on duty cycling the transmitter and receiver and are possible because of the discontinuous nature of the On-

Off Keying signal. In order to ease the sensitivity requirements of the baseband receive amplifier a design methodology for large output voltage receivers is presented. The designed receiver is measured to give a 5 mV output for an input power of -90 dBm and yet consumes less than 0.7 mW.

There is also an appendix on the non linear modelling of the Glasgow University 50nm InP meta-morphic High Electron Mobility Transistor (50nm mHEMT) and one on the non linear modelling of a commercial Step Recovery diode (SRD). Models for the 50 nm mHEMT and the SRD are useful in the analysis, simulation and design of oscillators and pulse generators respectively.

Acknowledgements

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Publications

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- McGregor, I.; Wasige, E.; and Thayne, I.; 'Sub-50μW, 2.4 GHz Super-Regenerative Transceiver with Ultra Low Duty Cycle and a 675μW High Impedance Super-Regenerative Receiver', 37th European Microwave Conference, Page(s) 1322-1325, 8-12th Oct., 2007.

- McGregor, I.; Wasige, E.; and Thayne, I.; 'Sub Milli-Watt, 2.4 GHz, Super-Regenerative Transceiver with Ultra Low Duty Cycle', Asia-Pacific Microwave Conference Proceedings, Volume 1, Page(s): 484 - 487, 12-15 Dec. 2006.

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Chapter 5

List of Abbreviations

AGC – Automatic Gain Control

AM – Amplitude Modulation

BPSK – Binary Phase Shift Keying

CMOS – Complimentary Metal Oxide Semiconductor

CPW – Co Planar Waveguide

FET – Field Effect Transistor

HEMT – High Electron Mobility Transistor

IF – Intermediate Frequency

LO – Local Oscillator

mHEMT – metamorphic High Electron Mobility Transistor

MMIC – Monolithic Microwave Integrated Circuit

OOK – On Off Keying

PLL – Phase Locked Loop

PN – Pseudo Noise (code)

PSK – Phase Shift Keying

RD – Return Difference

RF – Radio Frequency

RR – Return Ratio

Rx – Receiver

SRD – Step Recovery Diode

SRO – Super Regenerative Oscillator

SRR – Super Regenerative Receiver

Tx – Transmitter

UWB – UltraWideBand

VCO – Voltage Controlled Oscillator

WSN – Wireless Sensor Network

Chapter 1

Introduction

This thesis details the analysis, design, implementation and measurement of microwave frequency radio transceivers. The designed transceivers are intended to be used in Wireless Sensor Network (WSN) applications. WSN ‘nodes’ or ‘specks’ must be physically small. This requirement imposes severe limitations on the power consumption of the radio as the battery, being physically small, has limited capacity. The small dimensions of the speck necessitate the use of relatively high carrier frequencies as the antenna and circuit dimensions decrease as the operating frequency increases. Therefore, the main aims of this thesis are to design microwave frequency transceiver topologies which allow the power consumption to be made as small as possible. All the models of electronic components and the designs for circuits are the work of the author. The hybrid prototypes were kindly fabricated by Stuart Fairbairn and were soldered by the author. All MMIC fabrication was kindly performed by technical staff. Credit is given throughout the thesis to those who contributed to the work .

Chapter 2 introduces the concept of WSNs and discusses the ‘traditional’ radio solution i.e. homodyne schemes. Furthermore, Chapter 2 discusses the drawbacks of homodyne schemes from the point of view of power consumption and presents topologies for non-coherent On-Off Keying (OOK), Super-Regenerative transceivers which are shown, in Chapter 4, to exhibit very low power consumption. Chapter 2 then discusses the choice of operating frequency with regard to path loss and circuit/antenna size. Chapter 2 finishes by reviewing the various work published in the literature on Super-Regenerative receivers.

Chapter 3 gives equations and procedures for designing basic RF building blocks: amplifiers, oscillators, detectors and switches. Knowledge of these building blocks is necessary for the discussion in Chapter 4 on complete transceivers.

Chapter 4 is dedicated to complete OOK transceivers which incorporate a Super-Regenerative Receiver (SRR). It begins with an introduction to super-regeneration and then presents a mathematical analysis of a simplified equivalent circuit. Next, a

complete hybrid prototype transceiver is presented along with measured results. Chapter 4 continues with the novel concept of duty cycling the whole transceiver to reduce the power consumption of first the transmitter and, secondly, the receiver. It is shown that, with the addition of some baseband processing, the original input waveform can be reconstructed at the receiver with a reduction in RF transceiver power consumption of approximately 95 %. Some measured results are then presented and finally the Chapter ends with a discussion of the advantages and disadvantages of the implemented systems.

Chapter 5 details the design and implementation of a MMIC solution to the design problem. It begins with a brief discussion of the technology process used. Next, an illustration of the layout and performance of MMIC capacitors and inductors is provided. EM simulation and measured data are shown to agree closely. If the passive networks (mainly inductors and capacitors) of designed MMIC circuits can be modelled with precision and if the active devices can be characterised accurately then the overall performance of MMIC circuits such as amplifiers and oscillators can be predicted with confidence. Chapter 5 continues with some simulated results and layouts for switches, amplifiers, oscillators and super-regenerative detectors. A design for a compact MMIC antenna is also presented. Finally, the layout for a complete transceiver/antenna MMIC is presented. Chapter 5 ends with a discussion of the simulated results.

Appendix A gives a more detailed derivation of the equations used for the analysis of the super-regenerative receiver in Chapter 4. Appendix B presents a step by step guide to the extraction and implementation of a table-based non-linear model of the 50 nm mHEMT used in the MMIC designs in Chapter 5. The model is useful for predicting the performance of circuits such as oscillators. Appendix C discusses a novel non linear model of a Step Recovery Diode (SRD). The model is shown to be accurate in terms of both small signal a.c. and time domain behaviour. The model is useful for predicting the performance of pulse generators. These circuits have applications in UWB systems. UWB systems are attractive solutions to the WSN design problem because they potentially offer very low power consumption. This is because the duty cycles of UWB systems can be extremely low as the RF signal widths are typically measured in pico seconds.

Chapter 6 assesses the contribution of this thesis to the development of ultra low power radio transceivers and discusses future work and improvements to the circuits and systems developed during the preparation of this thesis.

Chapter 2

Literature Review

2.1 Wireless Sensor Networks

Wireless sensor networks (WSN) [1] are emerging technologies and are attracting a lot of interest amongst the research community [2-7] and in industry [8]. SpeckNet, for whom this research is conducted, envisage a ubiquitous computing system consisting of a number of 'specks' whose size is anticipated, in the long term, to be less than 1 mm^2. SpeckNet is an inter-University collaborative project between Edinburgh, Glasgow, Strathclyde, Napier and St. Andrews Universities with Glasgow University responsible for the radio circuitry. The radically new aim of SpeckNet is to allow for programmable computational networks enabling data sensing and information processing to 'disappear' into everyday objects such as surfaces, smart cards, clothes and walls. In this scenario, objects are 'speckled' and the specks automatically create an ad-hoc sensing and processing network.

WSN consist of a number of 'nodes' or 'specks' working cooperatively to perform some complex task such as monitoring the environment for temperature, sound, vibration, motion, radioactivity etc. They are especially well suited to tasks where the use of wired sensors is prohibitively high in cost or impractical. Wireless sensor network specks are equipped with wireless communication capability – optical or radio – to enable communication and sharing of collected data. Each speck or node, in addition to wireless communication, is equipped with a battery and/or renewable energy source, a limited amount of memory, sensor(s) and processing capability – usually some small microprocessor running a specially designed operating system [9]. This thesis is concerned with electronic circuits and radio topologies operating at low microwave frequencies which are suitable for use in WSNs.

There are two distinct approaches to the problem of communication between specks: each speck can be allocated a channel (a frequency band or time slot) or the specks can share one channel – in the former case more than one speck can 'talk' at a time whereas

in the latter case sophisticated techniques and algorithms have to be used to allow the sharing of the channel. Colleagues working at Edinburgh University have determined that the sharing of one channel is possible [10]. Also, the physical size, complexity and power consumption of a multi-frequency RF transceiver are probably prohibitively large – as will be discussed later. The problem with dividing specks into time slots is that some sort of 'mother' speck is required in order to synchronise the network but this is judged to violate the principle of having a truly distributed, ubiquitous, ad-hoc network. Therefore, to reiterate, the decision is made to use one channel and to use collision avoidance algorithms to allow the sharing of the channel between specks.

Current SpeckNet specifications require that, because of the limited power available from the battery, the radio must consume extremely low amounts of power e.g. less than 1 mW and, because of the intended unobtrusiveness of the specks, the radio must also be small e.g. less than 5 x 5 mm. The radio must also be able to operate effectively over a distance of at least a metre to enable communication between relatively distant specks.

2.2 Conventional Homodyne Radios

In order to highlight the unsuitability of conventional homodyne radio topologies to WSNs and to prepare the ground for future chapters, some measured results and technical concepts will now be described.

The traditional approach to modulating a high frequency carrier with a data signal is to multiply the baseband binary data with a Local Oscillator (LO) signal. This multiplication is achieved using a mixer and has the effect of moving the baseband data spectrum to a higher frequency – one which can be more conveniently transmitted through a free space link.

A mixer is a three port device: LO, RF (Radio Frequency) and IF (Intermediate Frequency) ports. The LO is connected to the LO port of the mixer and the baseband data is connected to the RF port. The resulting output at the IF port is an AM (Amplitude Modulated) signal. If the baseband signal is sinusoidal the output spectrum is a carrier with sidebands the same frequency from the carrier as the baseband frequency is from 0 Hz. The problems associated with this form of modulation include:

the carrier is attenuated between the input LO and output IF port and there is a loss in power between the baseband signal at the RF port and the sidebands of the output signal i.e. conversion loss. Figure 2.1 shows the idealised input baseband spectrum, the LO signal and the (filtered) output spectrum of a mixer in up-conversion mode.

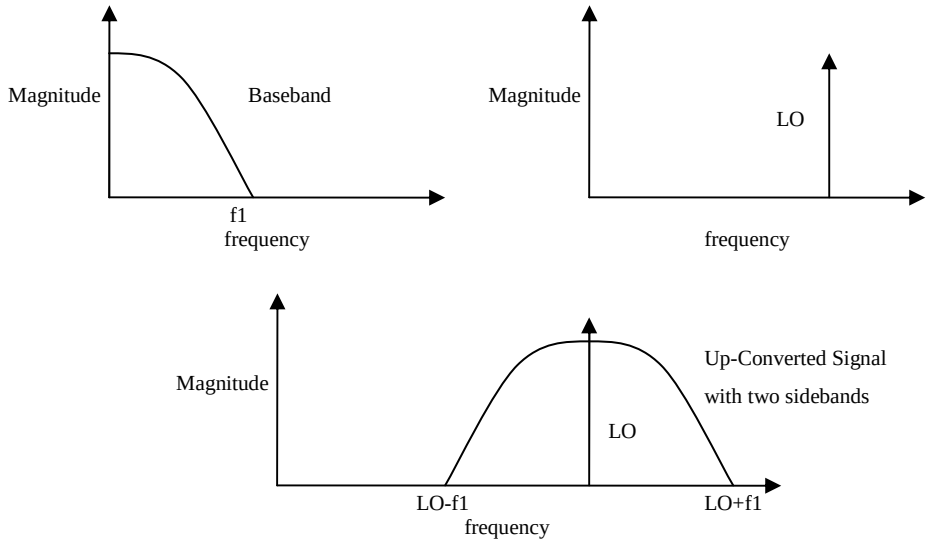


Figure 2.1 – Idealised LO, baseband and up-converted output signal of a mixer

The figure shows that the baseband data has significant low frequency components. The high frequency content depends on the rise and fall time of the input waveform and the data rate. The baseband spectrum is up converted to the carrier frequency by frequency multiplication. In practice the mixer output will contain baseband and higher frequency components but these can be filtered out and are omitted for clarity. Figure 2.2 shows the spectrum of the input RF signal, the LO signal at the receiver and the output baseband data of a mixer in down conversion mode.

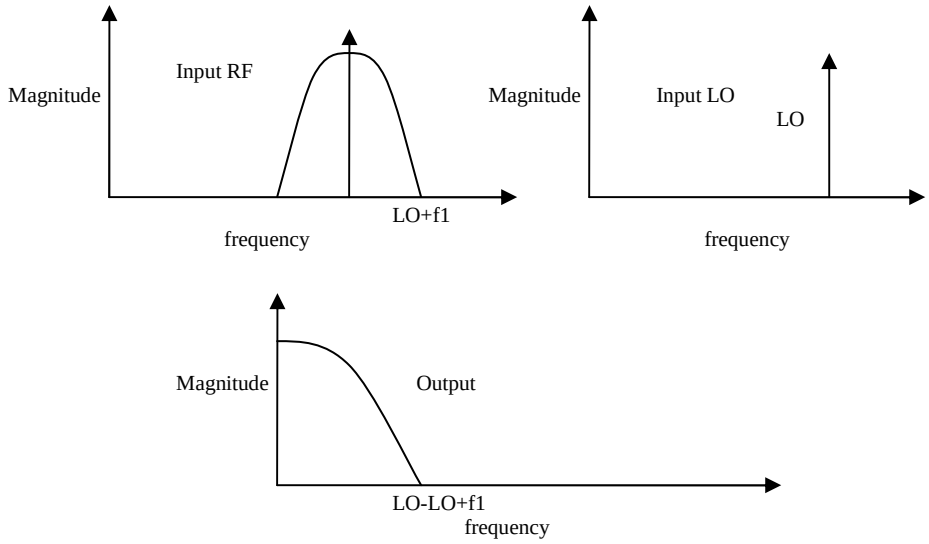


Figure 2.2 – Idealised LO, input RF and down converted output signal of a mixer

It can be seen that the effect of multiplying the received RF AM signal with an LO at the same frequency as the input carrier is to move the spectrum back down to d.c. thus reproducing the original baseband data.

Microwave engineers usually quote power in terms of dBm. Eq. 2.1 shows how the power in dBm is calculated.

$$PdBm = 10Log\left(\frac{Power}{0.001}\right) \tag{2.1}$$

Conversion loss is defined as the baseband power in dBs minus the power in one sideband of the output spectrum. Fig. 2.3 shows a photograph of a mixer operating at 2.45 GHz and fabricated on microstrip using diodes from Metelics (SMSD3012).

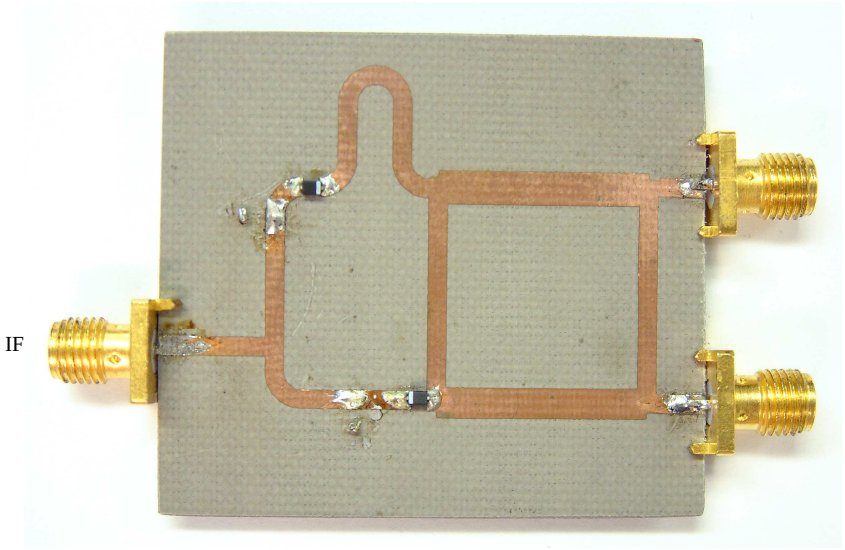


Figure 2.3 – Photograph of designed mixer operating at 2.45 GHz.

The measured conversion loss for varying LO power and a fixed RF signal power of -6dBm at 10 MHz is shown in fig. 2.4. These values are related to up-conversion or modulation of the carrier. It is clear from the graph that the conversion loss is relatively large (9 dB or 1/8th of the power) for an LO power of 0 dBm. If we assume a value of LO power equal to -10 dBm then the oscillator d.c. power consumption is likely to be 400 μW (this will be detailed in section 3.3) and the conversion loss is 20 dB. The conversion loss exhibited by the mixer is typical for passive mixers. However, active mixers can exhibit negative conversion loss i.e. they have conversion gain. Active mixers, however, tend to consume relatively large amounts of power [11-13] e.g. 50 mW for 15 dB gain, 7 mW for 6.5 dB gain and 2 mW for -0.5 dB gain.

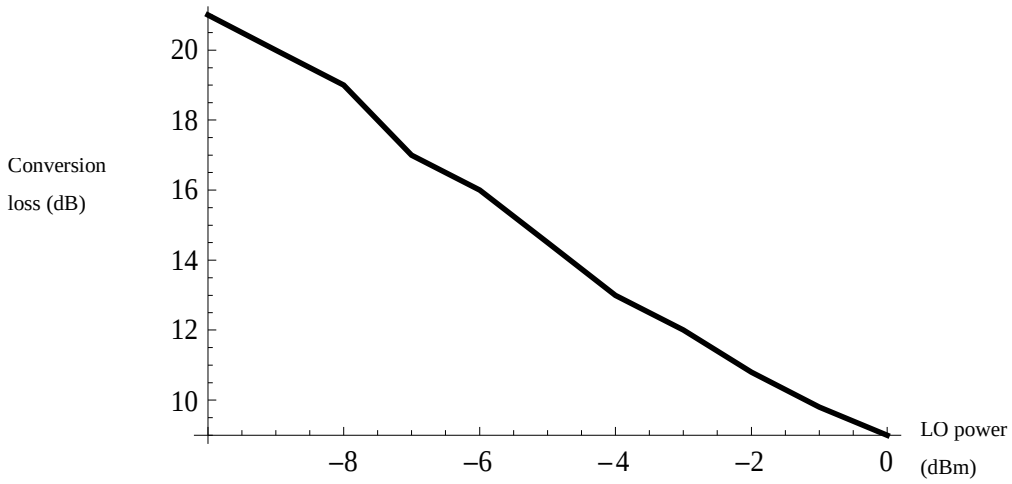


Figure 2.4 – Measured conversion loss for designed mixer
RF power=-6 dBm (0.25 mW), varying LO power

A more efficient way of modulating a carrier with a binary data signal is to use an oscillator and turn it ON and OFF with a control voltage. Using this arrangement the oscillator is only ON approximately half of the time and so approximately half the power is saved compared with using an oscillator which is always ON in conjunction with a switch to route the oscillator output to the antenna when there is a data ‘1’ or to ground when there is a data ‘0’.

Another parameter of interest is the output voltage of the mixer when down converting a signal. Fig. 2.5 shows some measured results for varying LO power and two fixed values of input power: -30dBm and -40 dBm. The output of the mixer is connected to a 1MΩ load to simulate the high input impedance of the baseband amplifier connected to the receiver (Rx) output in the full transceiver. Again we see the same trend: at high (0dBm) powers the output is relatively high but at small powers (-9dBm) the output is seriously degraded. It will be shown in later chapters how the output voltage can be maximised by using a super-regenerative receiver.

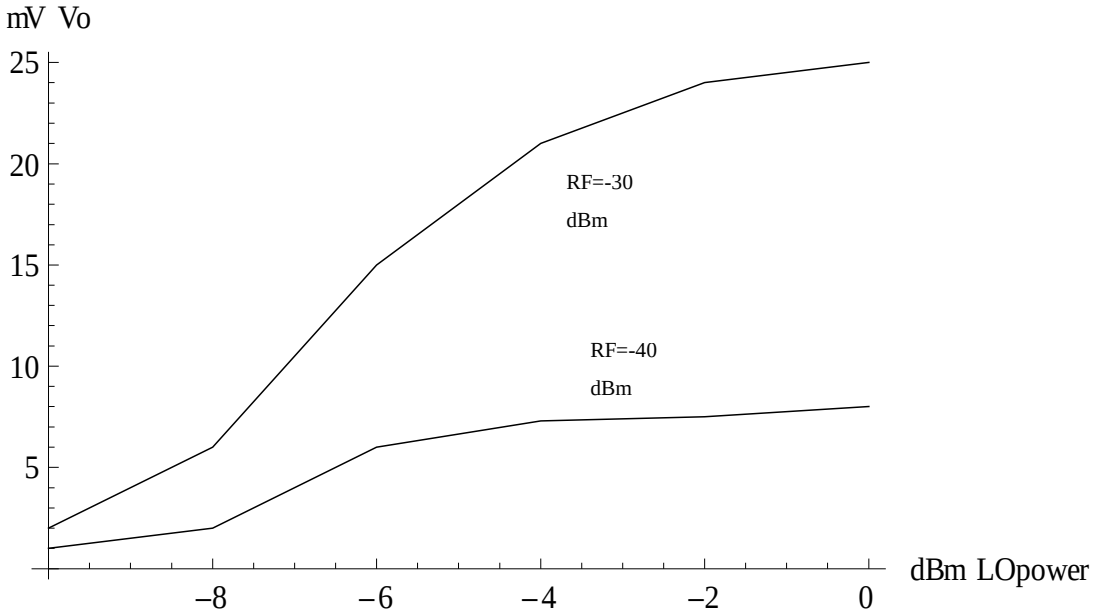


Figure 2.5 – Graph of mixer output voltage vs. LO power
For RF Power = -30 dBm and -40 dBm

The traditional approach to demodulating an AM wave is to down-convert the signal by using a mixer. Down-converting radios are called homodyne when the RF signal is directly converted to baseband or superheterodyne receivers when the RF signal is down converted to an Intermediate frequency and then down converted again to

baseband. Both approaches are popular because of their high sensitivity (lowest input power which produces acceptable output SNR: e.g. –117dBm [13]) and high selectivity i.e. resistance to signals adjacent in frequency to the input carrier frequency.

In this case the input signal is connected to the RF port, the LO to the LO port and the output is taken from the IF port. Again we have the same problems outlined earlier (losses) but on top of this we need to synchronise the receiver LO to the carrier. This is performed by a Phase Locked Loop (PLL) or, if the input signal is carrier suppressed as in Phase Shift Keying (PSK), a Costas Loop. Fig. 2.6 shows a block diagram of a PLL.

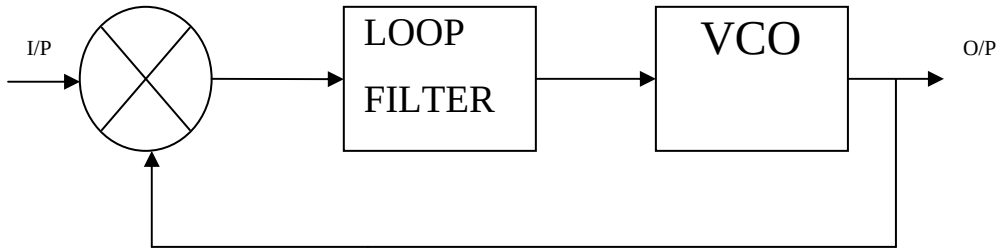


Figure 2.6 – Block diagram of a PLL

The input RF signal is multiplied with the VCO output and the mixer, or phase detector, produces an output at the difference frequency which causes the VCO frequency to deviate from its starting value. When the VCO frequency matches the input frequency the circuit will ‘lock’. The disadvantage of the PLL is that a VCO is required and this needs to output a relatively high power in order to ‘pump’ the mixer – as explained in the earlier discussion on conversion loss. An example of a PLL operating at microwave frequencies (1.1 GHz) is provided by ref. [14]. The power consumption in this case is 6.3 mW and the RF input sensitivity is only -17 dBm.

Fig. 2.7 shows a block diagram of a Costas Loop [15].

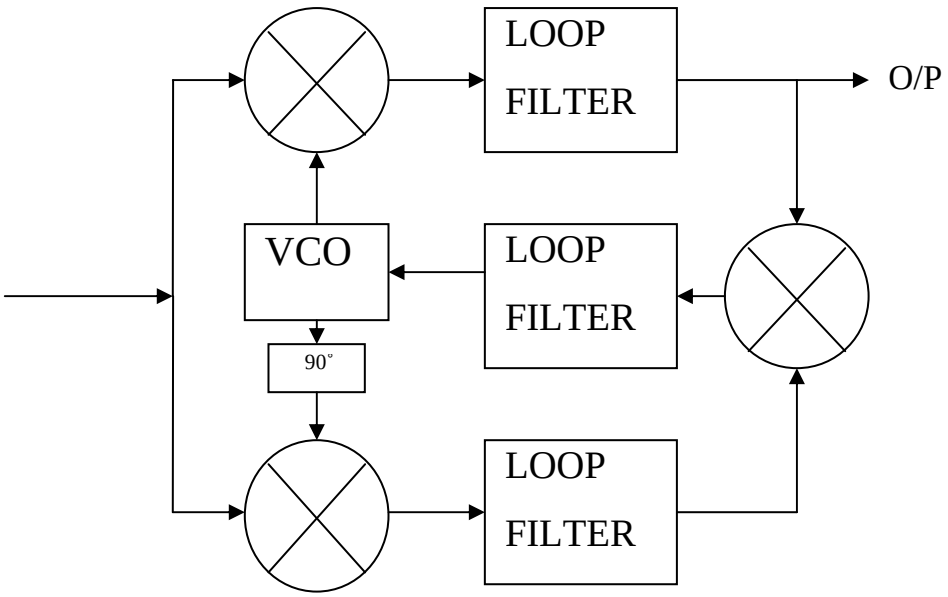


Figure 2.7 – Block diagram of Costas loop

The Costas loop is useful for tracking the input frequency of a signal with discontinuous phase e.g. a Phase Shift Keying (PSK) waveform. A PSK waveform can be generated by switching between two near identical carriers which are 180˚ (or some other value) out of phase with each other. The disadvantages of the Costas Loop are the same as mentioned for the PLL but on top of this the physical size of the circuit will be larger than the PLL as there are more components in the Costas Loop as can be seen from fig. 2.7. Also, half the power is lost at the input as the signal is split between the two mixers. Half the power is also lost from the VCO as the power is split between the direct path to the mixer and the path via the 90 deg phase shifter. The advantages of a Costas loop are that a signal with discontinuous phase can be tracked. In other words, the Costas loop is a generalised PLL.

A Costas Loop was implemented at 2.45 GHz using hybrid technology. Microstrip was used for all transmission lines and the mixers were those already shown in fig. 2.3. The 90˚ phase shift was implemented by a length of transmission line. The oscillator's frequency is tuned by the gate voltage which is fed by a CMOS baseband frequency multiplier. The output power of the oscillator was -10 dBm. The loop filters have a cut off frequency of approximately 10 MHz. The circuit tracked the input frequency but only for powers above -13dBm which is insufficient sensitivity if powers as low as, for example, -85 dBm are to be tracked and received. The circuit was fabricated using

microstrip and discrete diode technology (hybrid). The power consumption was 0.4 mW but this figure does not include the power consumption of an amplifier – used to amplify the input signal and isolate the receiver LO signal from the antenna.

2.3 Evolution of Radio from Homodyne to Super Regenerative OOK

The synchronisation problem (matching the LO to the input carrier frequency) can be negated if we replace the receive mixer with an envelope detector. The simplest envelope detectors consist of a d.c. return, a diode and an RC load (as will be detailed in section 3.5). The envelope detector is so called because it converts the envelope of the input carrier to a corresponding baseband signal. The advantages of using an envelope detector are that no LO is required and that no synchronisation circuitry is required – saving power and real estate. The disadvantage is that sensitivity is reduced: for example to –69dBm at 0.915GHz [16]. We are now faced with the problem of increasing sensitivity and also with the problem of increasing the output voltage of the RF front end as the envelope detector's output voltage is relatively small for a given input power (as will be detailed in section 4.3). One way to do this is to place an oscillator before the detector. By quenching (turning on and off) the oscillator at a rate of at least twice the maximum baseband frequency the oscillator acts like a high gain amplifier. The addition of a Super-Regenerative Oscillator (SRO) increases the sensitivity- a typical figure is –83 dBm [17]. Great savings in power are also made as the power consumption of an amplifier which provides equivalent gain is much larger than that of the SRO - for example the SRO in section 4.3 provides the equivalent of approximately 20 dB of gain. For the same transistor (NE76038) to provide this amount of gain in a single stage amplifier circuit, simulations show that it would need to be biased such that it consumed approximately 90 mW. This is compared to 300 μW for the SRO – see section 4.3 for more details. Collecting all this information together with the information in section 2.2 on directly modulated carriers we can draw four diagrams showing the evolution of the system from Homodyne (fig. 2.8), to an On-Off Keying (OOK) Tx (fig. 2.9), to an envelope detector Rx (fig. 2.10), and finally to a system with a super-regenerative receiver (fig. 2.11).

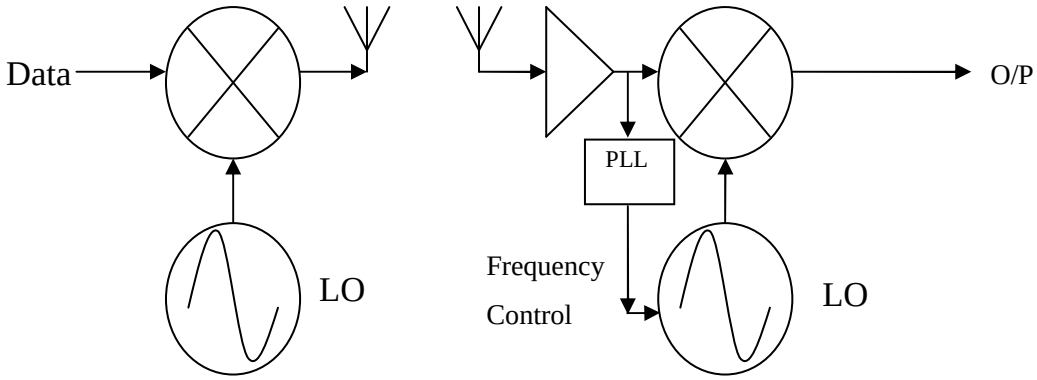


Figure 2.8 – Homodyne block diagram

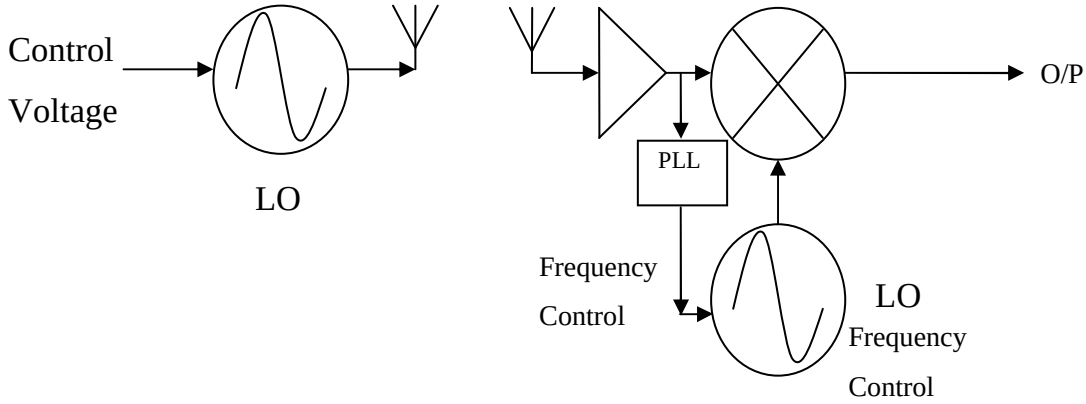


Figure 2.9 – OOK Tx with Homodyne Rx block diagram

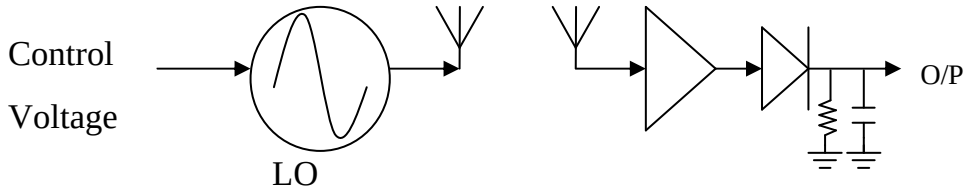


Figure 2.10 – OOK Tx with envelope detector Rx block diagram

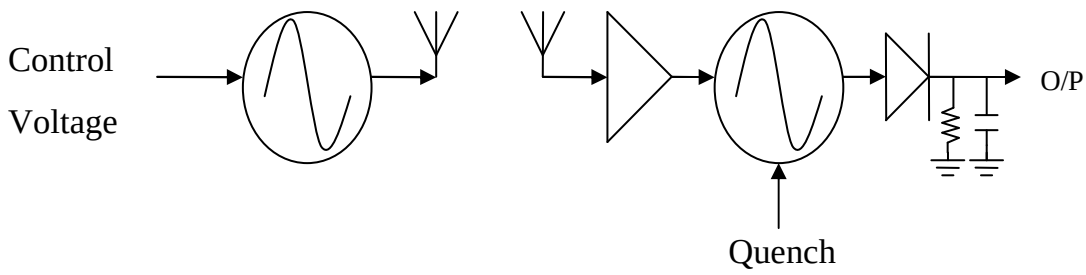


Figure 2.11 - OOK Tx with super-regenerative Rx block diagram

From the preceding discussion on mixers, conversion loss, PLLs, envelope detectors and SROs it follows that a promising circuit topology for WSNs in terms of power consumption, output voltage and operating range is a super-regenerative, directly modulated transceiver as shown in fig. 2.11. This is because mixers require relatively large LO powers if they are to exhibit acceptable conversion loss. If the mixers are active the published research in the literature indicates that they will consume more than 1 mW. PLLs are also likely to consume large amounts of power because they use a mixer and an LO. Envelope detectors are attractive because they are passive but the sensitivity is reduced compared with direct down conversion. Also, the output voltage of envelope detectors can be relatively small and can therefore place stringent demands on the baseband amplifier connected to the RF transceiver output. Super-Regenerative Receivers offer low power consumption, good sensitivity and higher output voltages than envelope detectors and are therefore the option which will be pursued in the remainder of this thesis.

2.4 Friis's Free Space Equation

Friis's equation [18], eq. 2.2, relates the power received at a point (P_{rx}) a certain distance away (d) from a transmitter with a certain output power (P_{tx}) using antennas with a certain gain (G_{tx} and G_{rx}) operating at a given wavelength λ

$$P_{rx} = P_{tx} + G_{tx} + G_{rx} - 20Log\left(\frac{4\pi d}{\lambda}\right) \tag{2.2}$$

where P_{tx}, G_{tx} and G_{rx} are in dBs. The last term of the equation is called the 'free space loss' and represents the attenuation of a radio wave between two points a distance, d, apart. Equation 2.2 assumes an ideal Line Of Sight (LOS) link. The loss is proportional to $(4\pi d)^2$. This results from the fact that the radio wave propagates out from a point as a sphere and so the energy is spread out in proportion to the surface area of the sphere. The free space loss according to eq. 2.2 is inversely proportional to the square of the wavelength. In other words the loss increases as the frequency increases or the wavelength gets shorter. The reason is that as the wavelength gets shorter so does the effective collecting area of the antenna [19].

The implications of Friis's free space equation are that in order to increase radio range, the operating frequency must be as low as possible. However, low operating

frequencies conflict with the requirement for small size because the lower the operating frequency the larger the antenna. Another factor to be considered is that a transistor's gain falls of with frequency so that more power has to be consumed to maintain the same performance as the frequency increases.

Another implication of Friis's equation is that to maximise received power the antenna gain must be high. But as the antenna gain is increased so does the directionality of the radiation pattern so that the radio range is drastically reduced if the Rx and Tx antennas are misaligned. Fig. 2.12 shows the free space loss as a function of distance where the operating frequency is 2.4 GHz, 5.8 GHz, 14 GHz and 24 GHz.

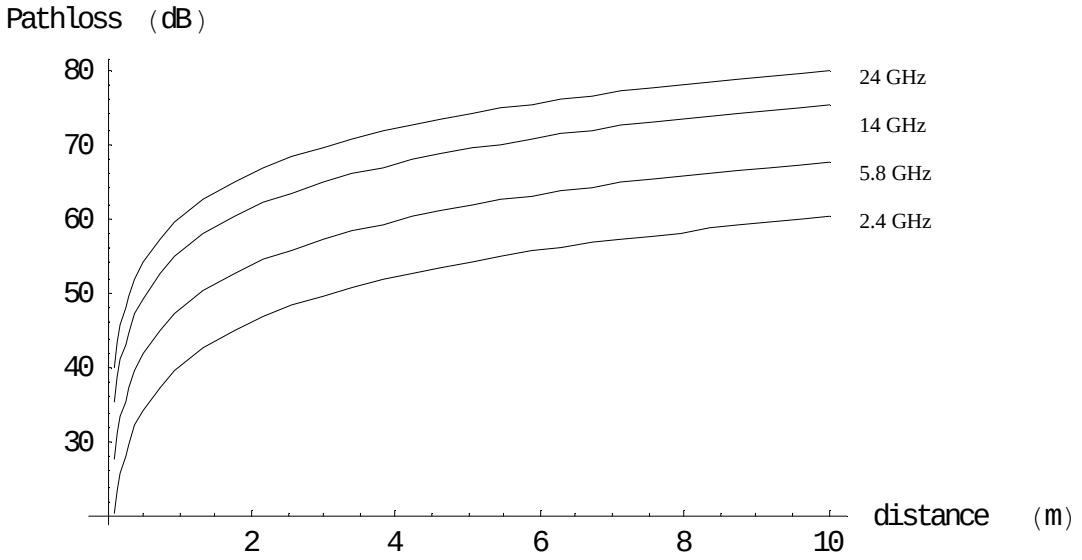


Figure 2.12 – Graph of pathloss vs. distance for different values of frequency

The free space loss increases by 6 dB as the distance doubles. Fig. 2.13 shows the dependence of the free space loss on frequency for a given distance (1m).

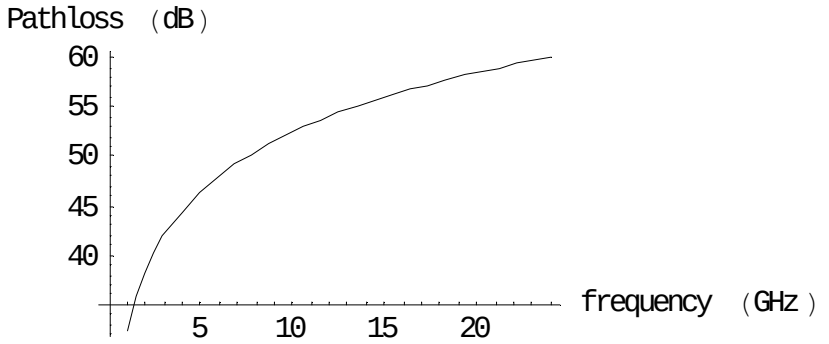


Figure 2.13 – Plot of pathloss vs. frequency for d=1 m

Fig. 2.14 shows the approximate antenna size for varying frequency. These figures are based on the wavelength in Co-Planar Waveguide (CPW) on GaAs substrate with a permittivity of 12.9 (ε_r=12.9). The wavelength is given approximately by:

$$\lambda = \frac{c}{f \cdot \sqrt{\frac{\varepsilon_r + 1}{2}}} \tag{2.9}$$

where c is the speed of light in a vacuum and f is the operating frequency. The term $\frac{\varepsilon_r + 1}{2}$ refers to the effective dielectric constant. In CPW half of the electric field is in the air and the other half in the dielectric so that the effective dielectric constant is the average of the two.

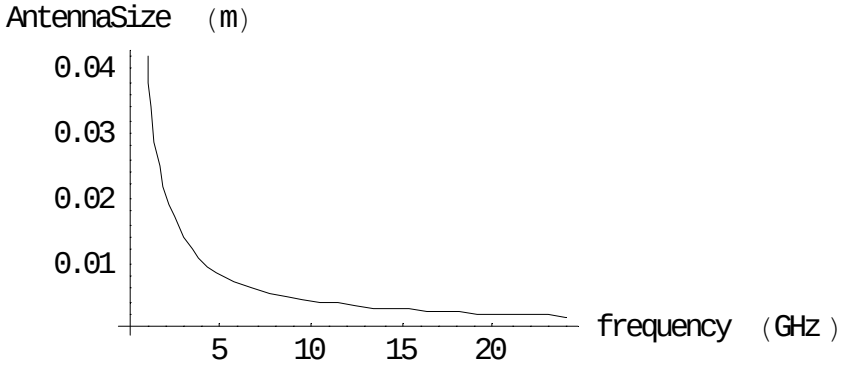


Figure 2.14 – Approximate antenna size vs. frequency

What is not clear from fig. 2.14 is that the antenna needn't be the full size predicted by eq. 2.9. For example, if a dipole or monopole is used the transmission line forming the antenna can be meandered or bent (see section 5.8).

If we assume a transmitter (Tx) power of -10 dBm and a receiver sensitivity of -80 dBm then from fig. 2.13 it is clear that an operating frequency of 2.45 GHz would provide a range of well over 10 m. However, from fig. 2.14 this results in antenna size of approximately 1.6 cm – to big for our requirements. If we increase the frequency to 6 GHz then the corresponding range is again over 10 m but the antenna size is reduced to approximately 7.2 mm. With some folding or meandering this antenna should fit into 5 x 5 mm (although we can expect a slight reduction in antenna efficiency). If we move to 24 GHz the antenna will fit into 5 x 5 mm without any difficulty but the radio range is reduced to about 3 m. This short analysis excludes the reduced sensitivity which results

from moving to a higher carrier frequency. The reduced sensitivity is a consequence of the receiver bandwidth being wider. Assuming the percentage bandwidth of the receiver is constant, the higher the frequency, the higher the noise bandwidth and the lower the SNR.

2.5 Conclusions

From the preceding arguments we can conclude that the traditional homodyne topology is in general unsuitable for WSNs – at least until ultra low power mixers with low conversion loss and ultra low power PLLs with high sensitivity can be designed. This is because of the high LO powers needed and because of the need to synchronise the LO with the input carrier frequency. We can also conclude that an OOK system with a passive envelope detector and a super regenerative oscillator is a promising choice as this maximises the receive sensitivity compared with a detector-only receiver and yet consumes relatively low amounts of power. The arguments presented in section 2.4 suggest that in order to maximise radio range whilst still maintaining a small antenna size an operating frequency of around 6 GHz is a good choice.

2.6 Discussion of Previously Reported Work on Super-Regenerative Receivers

From the arguments presented in the previous chapter, a major problem with down converting an OOK signal using a mixer is the need to synchronise the LO to the input frequency. Another problem is the relatively low output voltage. By quenching (turning on and off) an oscillator at a rate of at least twice the maximum baseband data rate the oscillator can be made to act like a high gain amplifier when an OOK signal is applied to the gate port of the oscillator. The addition of a Super-Regenerative Oscillator (SRO) increases the sensitivity of a receiver and maximises the output voltage. Only a few super-regenerative detectors, receivers and transceivers have been reported in the

literature - all employing OOK. In order to put the work contained in this thesis into context the various papers will now be described.

A 34 GHz super-regenerative detector [20] has been described. The detector consists of a 6 x 15 μm PHEMT (Pseudo-morphic High Electron Mobility Transistor) with the input RF injected into the gate port. The quench signal is also applied to the gate circuit – this time through the biasing circuitry. The transistor is configured as a negative resistance oscillator using transmission lines. The measured sensitivity for 12dB SNR is -61 dBm at a baseband rate of 1 KHz. The quench signal is a 500 KHz sine wave. The measured sensitivity is relatively poor and confirms what was outlined at the end of section 2.4 about the percentage bandwidth and hence the noise increasing as the operating frequency rises.

The same authors of [20] also report a 7.5 GHz super-regenerative detector [21] using hybrid microstrip technology and an ATF2884 transistor. This circuit achieves a good sensitivity of -83 dBm but consumes 100 mW. This power consumption is more than 100 times higher than the consumption of the receivers detailed in this thesis. The quench frequency in this case is a 600 KHz sine wave. This paper is notable for its claim that the optimum detection frequency (7.5GHz) is significantly lower than the free running oscillation frequency (8.366GHz). In both of the papers discussed so far the demodulated signal is recovered from the drain current i.e. a demodulated voltage is produced across a 100 Ohm resistor in the drain bias circuit.

A 1.2mW super-regenerative receiver operating at 1GHz and from a 1.5 V supply is described in [22]. The circuit uses a 0.35 μm CMOS process and achieves a sensitivity of -97 dBm. The circuit includes an AGC (Automatic Gain Control) and a baseband amplifier. The quench frequency is 100 KHz and the data rate is <18 KBit/s. CMOS circuits have the major advantage of potentially being integrated with the digital logic, memory, microprocessor and DSP of the speck or node and so the overall die size and cost is reduced. However, the power consumption of high frequency CMOS radios will tend to be higher than that of compound semiconductor (III-IV) solutions due to the higher transistor gains, lower noise figure and lower substrate loss of GaAs/InP.

A super-regenerative CMOS receiver operating in the ISM (Industrial, Scientific and Medical) band at 2.4 GHz is detailed in [23]. The receiver works from a 1.2 V supply and draws 3 mA i.e. power consumption is 3.6 mW. The sensitivity was measured to be -80 dBm for a relatively high data rate of 500 KBit/s but the most notable feature of the receiver is that it incorporates a feedback control loop to allow

channel selection by altering the operating frequency of the super-regenerative oscillator. The power consumption exhibited by this receiver is too high for the purposes of this research but represents a possible solution to the sharing of the channel by multiple specks i.e. Frequency Division Multiplexing (FDM). The transmitter could be implemented with a VCO.

A super-regenerative receiver operating at 1 GHz is reported in [24, 25]. The receiver is constructed in 0.8 μm CMOS and operates from a 2 V supply. The current consumption is 600 μA and the power is therefore 1.2 mW. The measured sensitivity is a very low -98 dBm whilst the data rate is a relatively high 100 KBit/s. The receiver has an extremely wide operating range of 0.3 GHz to 1.5 GHz. The quenching frequency is 1 MHz and the chip size is extremely small at less than 1 mm^2. Despite the extremely small size of the chip a very large antenna would be required if the circuit were used as an RF transceiver as it would have to operate at low GHz frequencies.

The transceiver described in [26] by Otis probably represents the apex of low power super-regenerative transceiver design. The receiver consumes only 400 μW and yet displays a sensitivity of -100 dBm at a BER (Bit Error Rate) of 0.001 when the data rate is 5 KBit/s. The transmitter consists of a highly stable BAW (Bulk Acoustic Wave) based oscillator coupled with a low power amplifier. Modulation is achieved by cycling the whole Tx circuit. The Tx consumes 1.6 mW and achieves a d.c./a.c. efficiency of 25%. This implies that the output power is 0.4 mW or -4 dBm. The overall chip size is very small at less than 1mm^2. Whilst the receive power consumption is very low, the Tx is too high for the specifications required by SpeckNet. The work in [26] has the major advantage over III-IV solutions in that the circuit can be implemented on the same silicon wafer as the other circuits comprising the speck. However, it has the disadvantage in that a relatively large antenna would be required. Solutions operating at 5.8 GHz, taking up less than 6 x 6 mm in area and consuming less than 1 mW are described in chapter 4.

Ayers [27] shows that low power super-regenerative receivers can be modified to demodulate FSK signals. In this paper a 1 mW Tx/ 0.28 mW Rx transceiver in 0.25 um CMOS is described. The data rate is 250 Kbit/s and the operating frequency is 900 MHz. The results in this paper may indicate a way to couple the low power consumption of the super-regenerative receiver with a modulation scheme more resistant to noise and interference than OOK.

Moncunill [28, 29] increases the functionality of super-regenerative receivers by describing two different spread spectrum architectures. Using spread spectrum techniques different users can share the same frequency band at the same time. The sharing of the channel is achieved by allocating different codes to different users and correlation is used at the receiver to 'de-spread' the RF signal i.e. the RF signal is demodulated by using the same code at the receiver as the transmitter uses to spread the original baseband data. The receivers achieve an extremely large output voltage of 1 V for the 'periodic quench' receiver and 0.55 V for the 'PN quench' (Pseudo Noise code Quench) receiver when the input power is -60 dBm. The term 'PN quench' refers to the quench signal being the output of an AND gate whose inputs are a clock signal and a PN de-spreading code. The power consumption is 4 mW and 2.75 mW respectively. In both cases the demodulated signal is recovered from the Collector/Emitter current i.e. no envelope detector is placed at the output of the super-regenerative oscillator.

The results of the papers discussed so far are summarised in table 2.1

Ref. No.	Operating Frequency (GHz)	Power consumption of Receiver (mW)	Technology	Sensitivity (dBm)
20	34	-	PHEMT	-61
21	7.5	100	MESFET	-83
22	1	1.2	CMOS	-97
23	2.4	3.6	CMOS	-80
24,25	1	1.2	CMOS	-98
26	1.9	0.4	CMOS	-100
27	0.9 GHz	0.28	CMOS	____

Table 2.1- Summary of the results in the literature

It can be seen from the table that the only super-regenerative detectors to have been implemented in GaAs have either very high (100 mW) power consumption or else their consumption is not stated. The only low power transceivers reported have all been in CMOS and have an operating frequency no higher than 2.4 GHz. This thesis will present full transceivers implemented with GaAs or InP transistors whose power consumption is less than any of the results discussed and whose operating frequency is 2.4 GHz or above. It will also describe techniques to lower the power consumption of

the standard super regenerative transceiver topology. Compared with silicon, GaAs transistors have the advantage of lower power consumption and smaller Noise Factors: ref [30] shows that at 24 GHz the lowest noise factor is 0.7 dB compared to 5 dB with 180 nm CMOS technology at the same frequency [31].

Chapter 3

Basic RF Building Blocks

3.1 Introduction

Before a full RF transceiver can be discussed it is necessary to detail the RF building blocks of which the transceiver is composed. The circuits needed are as follows:

- Amplifiers – used to boost the received signal and to isolate the receiver oscillator from the antenna
- Oscillators – used to generate the carrier when there is a data '1' and to amplify the received signal when used as a super-regenerative oscillator/detector
- Detectors – used to demodulate the receive signal to baseband data
- Switches – A switch allows the antenna to be shared between the receiver and transmitter

3.2 Amplifiers

The amplifier performs the most basic of functions within an RF transceiver by boosting the received power at the receiver input. In the case of a super-regenerative receiver the amplifier also prevents re-radiation by isolating the Super-Regenerative Oscillator (SRO) from the antenna i.e. the only coupling is via the S_{12} parameter of the amplifier. S_{12} should be as low as possible but a figure of -15 dB is acceptable as the re-radiated power for an SRO power of -10 dBm is -26 dBm (including 1 dB switch loss) which is equivalent to saying that 3 % of the power of the SRO is re-radiated.

Since it is determined that no amplifier is necessary in the transmit path (the transmit oscillator is directly connected to the antenna) the only amplifier needed is the receive amplifier – no power amplifier is needed for the transmitter. This is because the

necessary output power is more efficiently achieved by an oscillator-only implementation; the addition of an amplifier would reduce the overall efficiency of the transmitter.

Fig. 3.1 shows a general 2-port network consisting of a two port representing the transistor and a 2-port on either side representing the matching networks. The transistor is represented by an S-Parameter matrix while Γ_s represents the reflection coefficient looking into the source matching network and Γ_L represents the reflection coefficient looking into the load matching network.

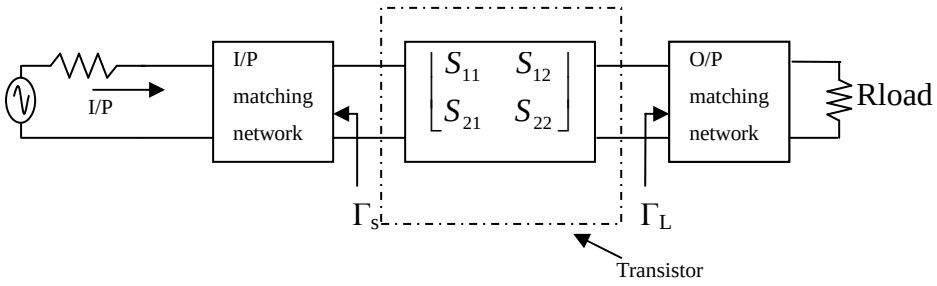


Figure 3.1 – General 2-port network

Rollet's number, k, is a measure of the stability of a transistor and is given by eq. 3.1 [1].

$$k = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} \tag{3.1}$$

where Δ is given by

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{3.2}$$

If k is greater than 1 and Δ is less than 1 then any passive impedance can be presented to either port and the circuit will be stable. If k is less than 1 then some portion of the smith chart will represent unstable impedances. If the transistor is unconditionally stable it can be 'conjugately' matched. Fig. 3.2 shows the simulated k number and Δ for the NE76038 transistor. It can be seen that k is less than 1 at low frequencies and that Δ is less than 1. If the transistor has k<1 at the desired operating frequency then it can be resistively loaded. This can be achieved by inserting a small (typically 50 – 150 Ω) resistor in series with the gate or drain circuit. The better choice is to place the resistor at the drain side as this produces lower Noise Factor (NF). The equation for the noise factor of two cascaded stages is given by eq. 3.3 [1].

$$NFtotal = F_1 + \frac{F_2 - 1}{G_1} \tag{3.3}$$

Eq. 3.3 shows that the NF of two stages (resistor and transistor) cascaded depends most critically on the noise factor of the first stage (F_1) and that the contribution of the second stage (F_2) is reduced by the gain (G_1) of the first stage.

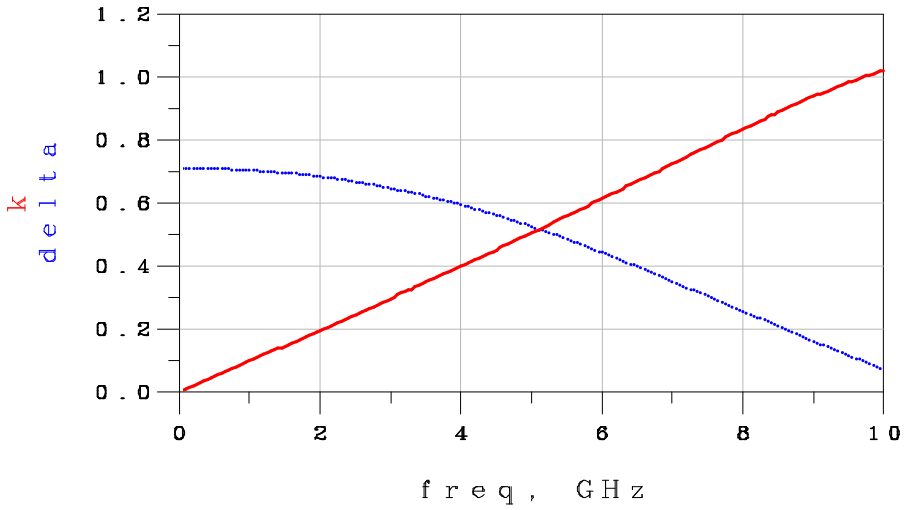


Figure 3.2 – k and Δ for NE76038 transistor

Fig. 3.3 shows k and Δ for the same transistor with resistive loading at the drain (80Ω)

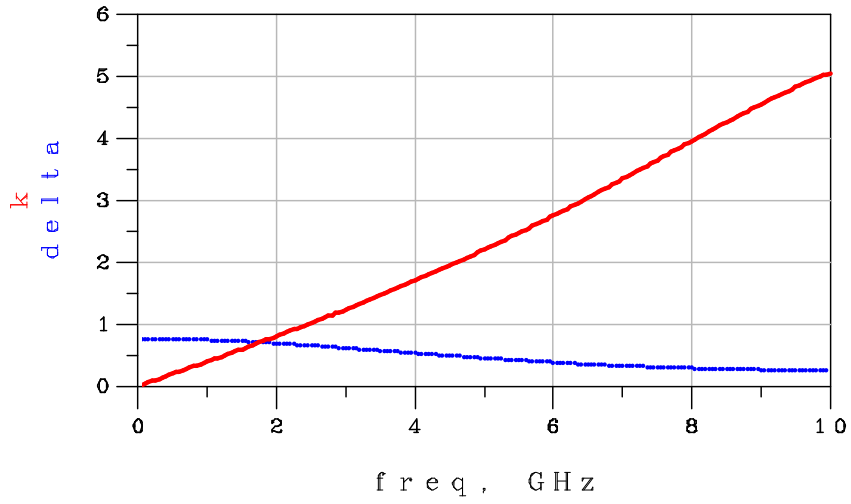


Figure 3.3 - k and Δ for NE76038 transistor with resistive loading

Fig. 3.4 shows the source and load stability circle before and after resistive loading at 2.45 GHz. In both cases it can be seen that the effect of the resistor is to move the stability circles outside the passive smith chart.

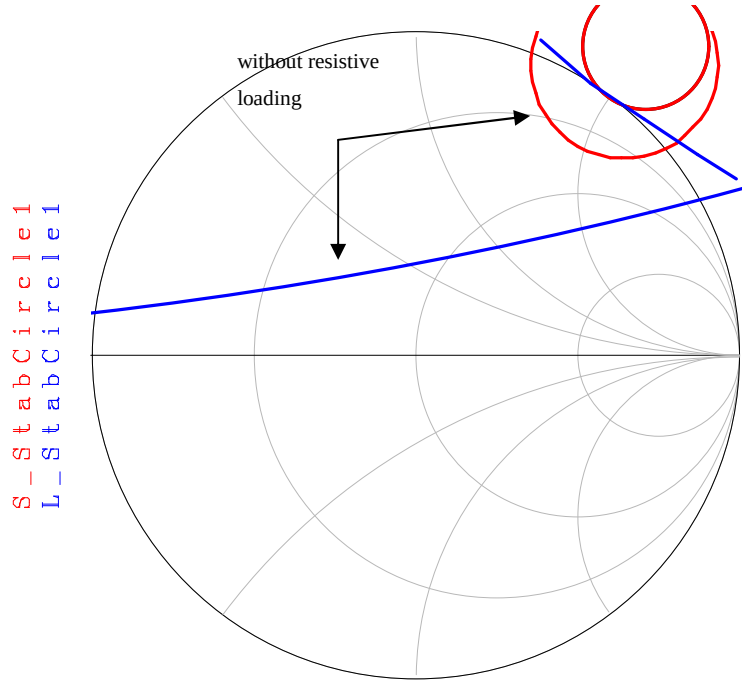


Figure 3.4 – Source (red) and load (blue) stability circles before and after resistive loading

Because k is now greater than 1, the magnitude of S_{11} and S_{22} are less than 1 and the stability circles lie outside the passive smith chart the transistor can be conjugately matched.

The relevant equations are given below.

$$\Gamma_s = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \tag{3.4}$$

$$\Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \tag{3.5}$$

Where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \tag{3.6}$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \tag{3.7}$$

$$C_1 = S_{11} - \Delta(S_{22})^* \tag{3.8}$$

$$C_2 = S_{22} - \Delta(S_{11})^* \tag{3.9}$$

Fig. 3.5 shows an example of an ADS schematic for a resistively loaded, conjugately matched amplifier. The two bias voltages are applied through two large

valued inductors. The reactance must be at least ten times the normalising impedance (50 Ω) so that the RF is isolated from the a.c. grounds of the power supplies. A large valued capacitor on either side of the circuit prevents d.c. current from flowing in either the source or load resistances. The matching networks are realised using ideal lumped components.

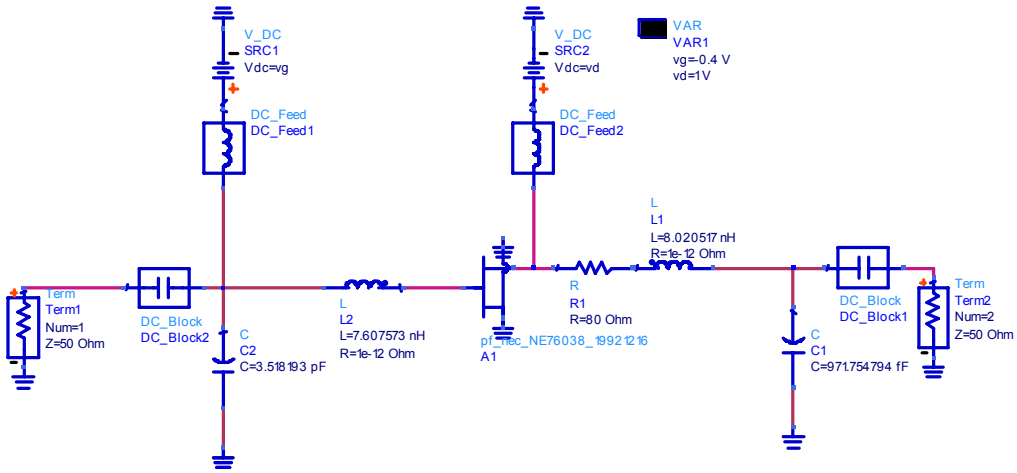


Figure 3.5 – Example of conjugately matched amplifier

Fig. 3.6 shows the simulated input and output reflection coefficient for the circuit in fig. 3.5. The deep troughs indicate a near perfect match to 50 Ω for both the input and output at the centre frequency of 2.45 GHz.

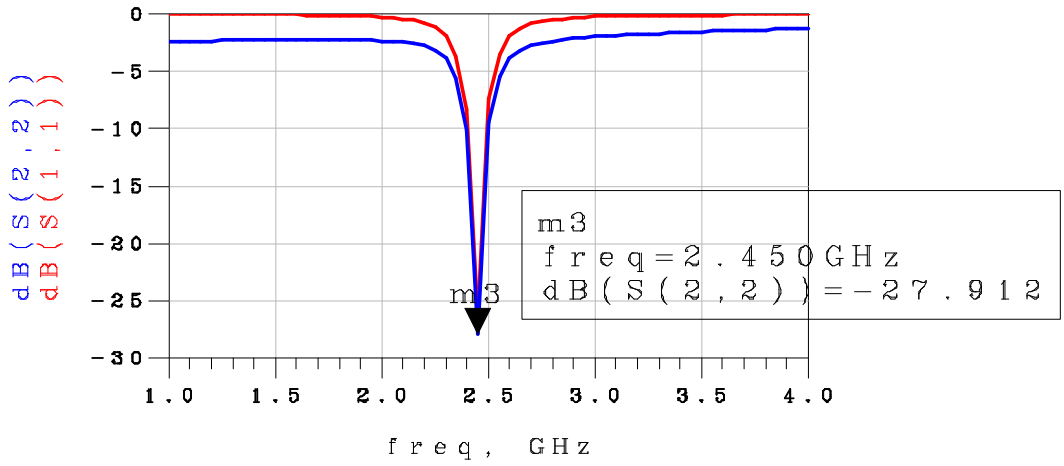


Figure 3.6 – Input and output reflection coefficient for the circuit in fig. 3.5

Fig.s 3.7 and 3.8 show the simulated forward power gain and reverse transmission respectively. The gain is at a peak at the centre frequency whilst the reverse transmission is –17.5 dB at 2.45 GHz.

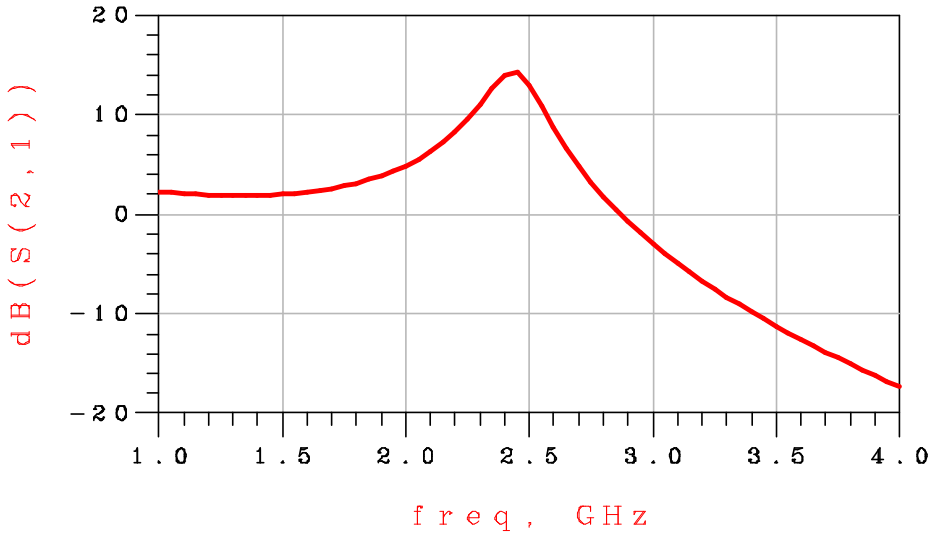


Figure 3.7 – Simulated power gain for the circuit in fig. 3.5

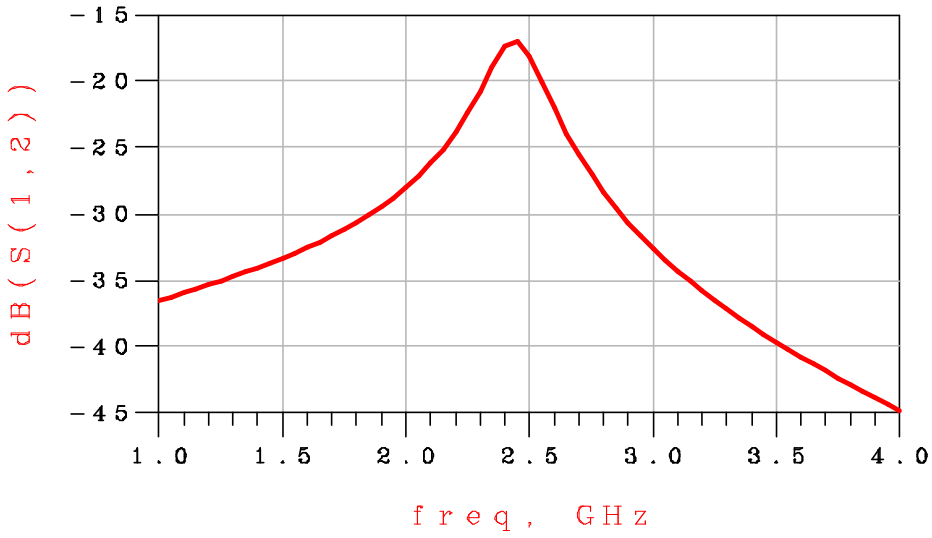


Figure 3.8 – Simulated reverse transmission for the circuit in fig. 3.5

3.3 Negative Resistance Oscillators

Oscillators are used to generate carriers (Local Oscillator) and also as an effective high gain amplifier when used in Super-Regenerative receivers. They convert d.c. power into a.c. power with an efficiency η.

$$\eta = \frac{fundamental power}{d.c. power} \tag{3.10}$$

Typically η is 20 to 30% for the NE76038 at 2.45 GHz. Hence, if we fix the output power at -10 dBm we can expect the power consumption of the Tx oscillator to be 400 μW assuming η=25%. There are many configurations for oscillators (e.g. Colpitt's, Hartely's and others) but the most convenient type to implement at microwave frequencies are negative resistance oscillators. They are the most convenient to design as they are the easiest to predict the behaviour of and to design. Fig. 3.9 shows a block diagram of a 2-port network oscillator.

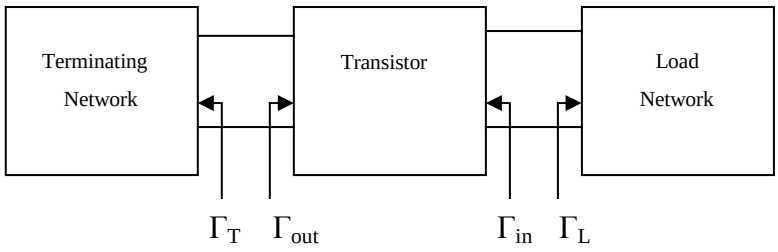


Figure 3.9 – Block diagram of 2-port negative resistance oscillator

To design a negative resistance oscillator we use a potentially unstable transistor (k<1) and choose a terminal impedance, Γ_T, to lie in the unstable region of the smith chart. This produces a negative resistance or, equivalently, a reflection coefficient at the other port, Γ_{in}, greater than 1. The output matching network is designed according to eq. 3.11 [1].

$$Z_L = \frac{-\mathrm{Re}(Z_{in})}{3} - j(\mathrm{Im}(Z_{in}) \tag{3.11}$$

The terminal impedance is that presented to the gate circuit and the input reflection coefficient, Γ_{in}, is associated with the drain side of the transistor for a common source configuration.

Any small perturbation (i.e. noise) at the oscillator output frequency is amplified and fed back to the gate port and amplified again etc until a steady state – governed by the non-linearity's of the transistor - is reached.

The harmonic content of the output waveform is important because the designer wants as much of the power in the fundamental as possible and also because spurious

RF emissions need to be limited in most cases. Therefore, from these considerations it is desirable to have as little power in the harmonics as possible.

3.4 Oscillators: Return Ratio Method

As an alternative to the negative resistance method described in the previous section this section describes how Return Ratios (RR) can be used to design microwave frequency oscillators with decreased start up time, improved spectral purity, and increased efficiency.

Any three terminal transistor can be modelled by an equivalent circuit [2] consisting of three frequency dependent admittances (*a*, *b* and *c*), a frequency dependent controlled source, or transconductance, (*m*) and two terminating admittances, L and G, as shown in fig 3.10.

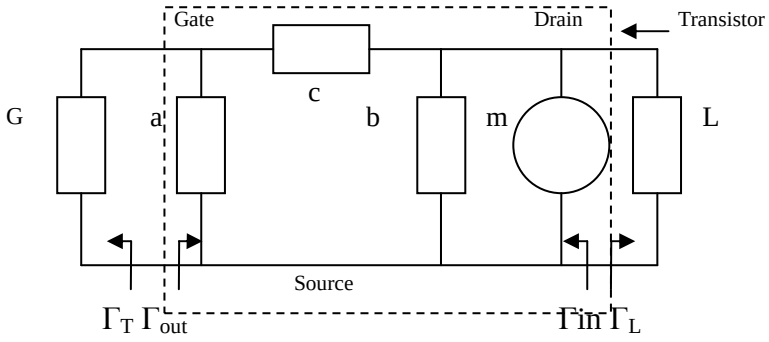


Figure 3.10 - Equivalent circuit of transistor with terminations for analysis purposes

Using standard two-port analysis the admittance matrix is found to be

$$[Y]=\begin{bmatrix} a+c+G & -c \\ m-c & b+c+L \end{bmatrix}=\begin{bmatrix} Y_{11}+G & Y_{12} \\ Y_{21} & Y_{22}+L \end{bmatrix} \tag{3.12}$$

Y_{11}, Y_{12}, Y_{21}, and Y_{22} can be converted from measured S – Parameters using standard formulae.

The RR, as defined by Bode [3], is given by

$$RR=1-\frac{\Delta}{\Delta(m=0)} \tag{3.13}$$

where Δ is the determinant of eq. 3.12 and Δ(*m*=0) is the determinant with *m* set equal to zero. From Nyquist's real frequency test [4], a doubly terminated transistor is unstable if the RR encircles the point -1+j0 in a clockwise sense with increasing frequency.

To develop a synthesis procedure using RRs, from eq.s 3.12 and 3.13,

$$RR = \frac{mc}{(ab+(a+b)c)+GL+(b+c)G+(a+c)L} \tag{3.14}$$

where G and L are the generator and load admittances respectively,
and *a*, *b*, *c* and *m* are the branch admittances of the equivalent circuit
Setting eq. 3.14 equal to -n+j0 and rearranging we get

$$L = \frac{mc + n((ab + (a+b)c) + (b+c)G)}{-n(G + a + c)} \tag{3.15}$$

where *n* is the desired magnitude of RR at 180 deg. Varying the value at which the RR passes through the 180 deg point is found to have a profound influence on oscillator start up time, output wave-shape and magnitude. In order to investigate the effect, several oscillators were designed for 2.45GHz in the following manner:

(i) The input stability circle is drawn and a value for Γ_T which results in a maximum negative real part of Z_{in} (this usually corresponds to choosing the magnitude of Γ_T to be a maximum, i.e. 1, since it is associated with a reactive impedance and choosing the angle such that a straight line drawn from the origin of the Smith chart to Γ_T passes right through the centre of the source stability circle) is chosen in the unstable region

(ii) The generator admittance, G, is calculated and the terminating network designed using the smith chart tool in ADS

(iii) Eq. 3.15 is used to determine L and the output matching network designed

(iv) Several different values of RR from 1 to 2 are chosen

(v) The circuits are simulated in Agilent's ADS software using a vendor supplied non linear model

(vi) The circuits were built on Rogers high frequency laminate with h=0.762mm and a relative permittivity of 3.48. The boards were fabricated by Stuart Fairbairn and the boards were soldered by the author. Also, an oscillator was designed using the standard design procedure [1] with one exception: The point inside the source stability circle was not arbitrarily chosen, instead it was chosen to make the negative real part of Z_{in} a maximum.

In order to evaluate the RR using ADS, two Y-Parameter Touchstone™ files are created. The first, called RTR (Reciprocal Transmission), comprises $\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{12} & Y_{22} \end{bmatrix}$. The second file, Ym, consists of the entries $\begin{bmatrix} 0 & 0 \\ Y_{21} - Y_{12} & 0 \end{bmatrix}$. The Y-Parameters are found from de-embedded small signal S-Parameter measurements of the transistor.

In order to calculate the RR as a voltage ratio [5], all independent sources are set to zero, the control voltage for the dependent current generator is transferred from branch '*a*' to an isolated independent excitation v_1. All feedback paths between the dependent generator and its controlling branch voltage are thus broken. This approach is slightly different from [5] in that the feedback loop is broken at the opposite side of the controlled source and the returned voltage is taken as the voltage across branch '*a*' instead of across the dependent generator. However, the two methods yield identical results. Fig. 3.11 shows how ADS is used to calculate the RR for the circuit.

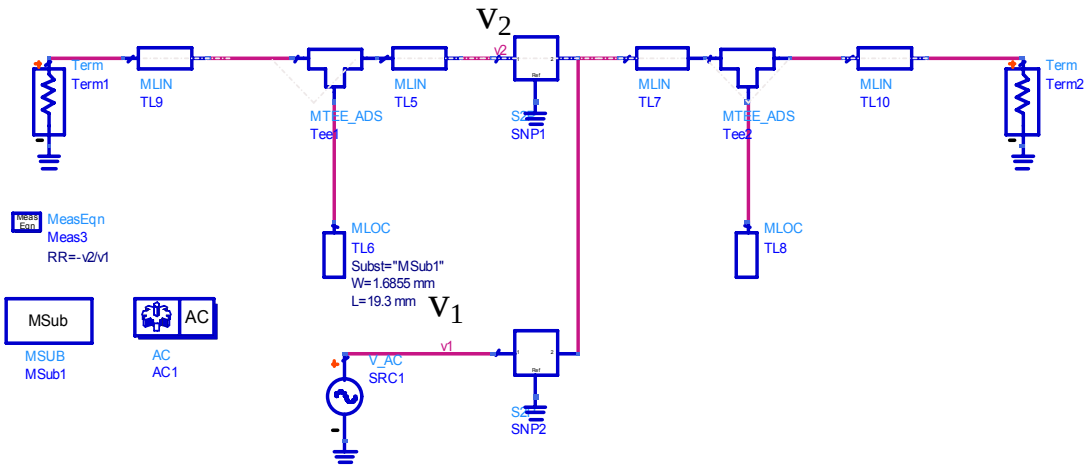


Figure 3.11 – ADS schematic showing how the Return Ratio is calculated

The upper 2-Port is the reciprocal network RTR and the lower is the 2–Port Ym. The RR is calculated as the negative of the voltage returned to port 1 of RTR, V_2, to the applied test voltage, V_1. Fig. 3.12 shows the RR- in this case the RR is designed to be 1.08 at 180 degrees.

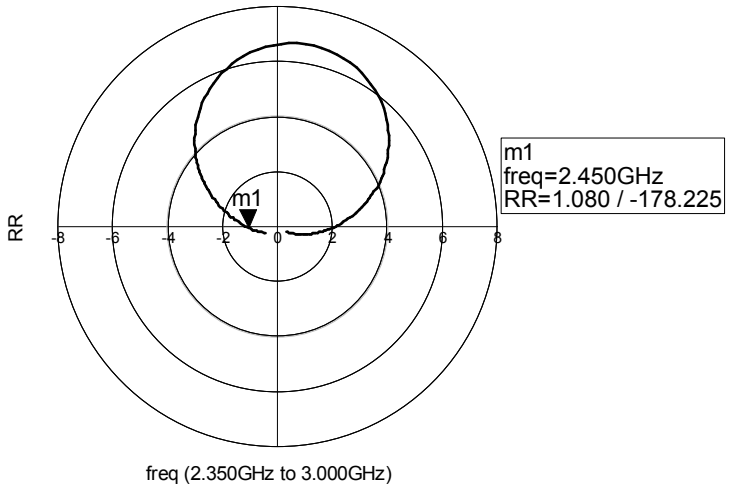


Figure 3.12 – Return Ratio of circuit in fig.3.11

The RR crosses the 180 deg line, indicating oscillations, at 2.45 GHz. The measured results for the circuits are summarised in table 3.1.

RR	Transistor	dc power consumption (mW)	Frequency of Oscillation (GHz)	O/p Power of Fundamental (dBm)	Power of 2 nd Harmonic (dBm)	ac/dc Efficiency (%)
Conventional Circuit	NEC76038	6.2	2.41	-1	-14	12.8
1.08	NEC76038	6.2	2.325	+2.5	-16	26.2
1.2	NEC3210S01	20	2.42	+5.8	-21	19
1.26	NEC76038	6.2	2.35	+3	-15	29.3
1.35	NEC3210S01	20	2.41	+0.5	-17	5.6
1.9	NEC3210S01	15	2.55	-10	-8	0.5
2	NEC76038	6.2	2.325	-3	-5	7.4

Table 3.1 –Summary of experimental results

The results show that for spectral purity the RR should be as low as possible. However, this tends to result in decreased efficiency so for a practical design a value of around 1.25 is recommended. This value results in high efficiency and, as will be discussed later, fast start up time. Also, if the circuit is designed for RR=1 there is a risk that the circuit will not oscillate. It can be seen from the table that there are large variations in efficiency between circuits. This is explained by the fact that different bias

points were chosen and two different transistors were used. However, for a d.c. power consumption of 6.2 mW using the NE76038 it can be seen that maximum efficiency occurs when the RR is equal to 1.26. In the circuits that use the NE3210S01 the maximum efficiency occurs when the RR is approximately equal to 1.2. The results also show that the actual frequency of oscillation is somewhat lower than the designed value. This is explained by the fact that that as the signal level increases the S-Parameters of the device change. Large signal S-Parameters may give a more accurate picture. Alternatively the circuit can be designed for a higher frequency than required. Note that no tuning of the circuit via power supplies or stub length was used for the results summarised in table 3.1.

It can also be shown that designing for RR=1 at 180 deg phase shift and then dividing the real part by three corresponds exactly to the common method for oscillator design proposed in [1].

Simulated results suggest a strong correlation between increased RR and decreased start up time. This can be explained by the fact that as the RR is large the returned voltage is also large and hence the oscillations build up more quickly. This is shown in fig. 3.13 with three plots of the start up transient envelope. It cannot be seen from the plot but the three traces consist of approximate sine waves.

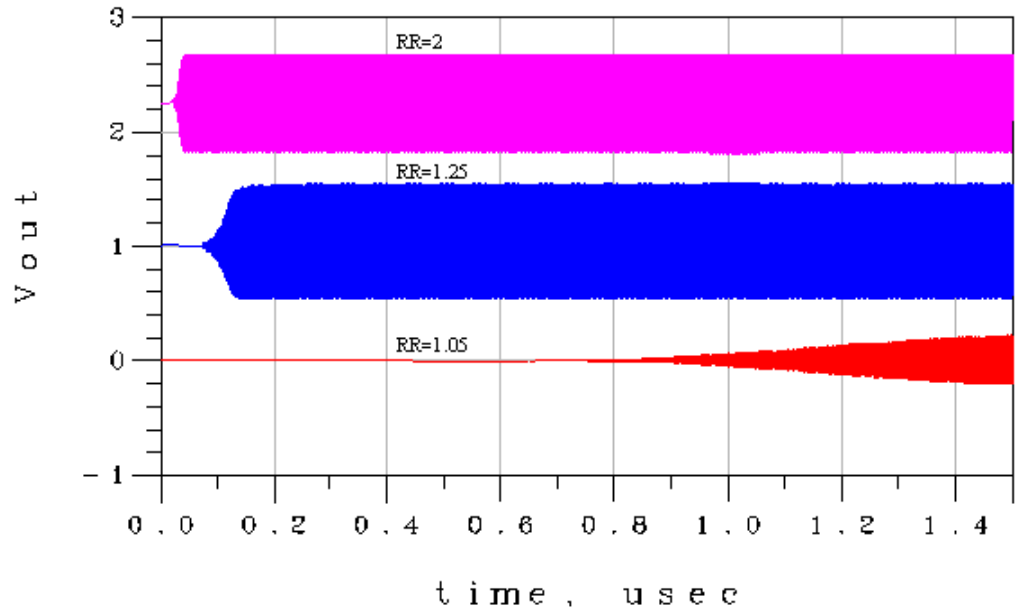


Figure 3.13 – Start up transient for circuits with RR=2, 1.25 and 1.05

It has been shown that, by using the new design method, an oscillator circuit can be optimised for output power or start up time by designing for RR>1 at 180 deg phase

shift whilst keeping the oscillator operating frequency constant. The connection between better spectral purity and lower values of RR has also been demonstrated.

3.5 RF Detectors

RF Detectors [6] are used to demodulate or rectify the input of an AM or OOK RF signal. Generally speaking, detectors convert input powers to output voltages when properly configured with an input matching network (usually to 50 Ω), a d.c. return and an output RC network. This arrangement is shown in fig. 3.14.

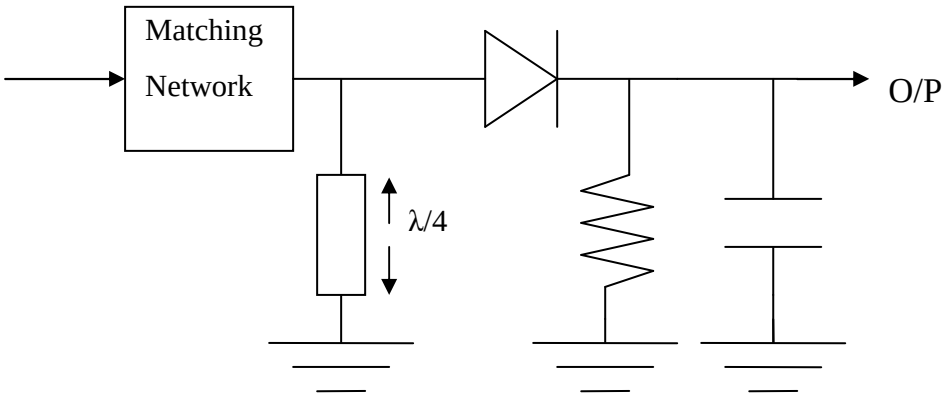


Figure 3.14 - General diode envelope detector

As already mentioned, the matching network transforms the relatively high input impedance of the diode to, usually, 50 Ohms whilst the d.c. return is a short circuit (at d.c. but not at RF) at the input side. The quarter wavelength transmission line transforms the short circuit into an open circuit at the carrier frequency. The d.c. return is necessary to complete the circuit between the output and ground otherwise no current would flow through the diode and so no voltage would be produced across the diode. If no d.c. return is used the output waveform exhibits a high pass shape characteristic. This is due to a.c. current flowing through the junction capacitance of the diode. The d.c. return can be incorporated into the matching network by using an inductor to ground. The RC network performs two functions: it provides a load resistance so a voltage can be developed and it filters out any of the RF signal present at the output. The presence

of this signal is due to the parallel capacitance in the diode model providing an a.c. path for the input signal.

The design procedure used for the detectors in this thesis is as follows:

- From the baseband frequency required and the RF frequency used, estimate the values for the RC network. The capacitance should be sufficiently high to short out the RF carrier. The RC product should be sufficiently low so as not to distort the output waveform but on the other hand R should be high so as to maximise the output voltage
- Measure/Simulate the input impedance of the diode with the RC network attached
- Use the smith chart tool in ADS to synthesise a matching network consisting of a series inductor and parallel inductor to ground

Fig. 3.15 shows an ADS schematic of a diode detector designed as outlined above.

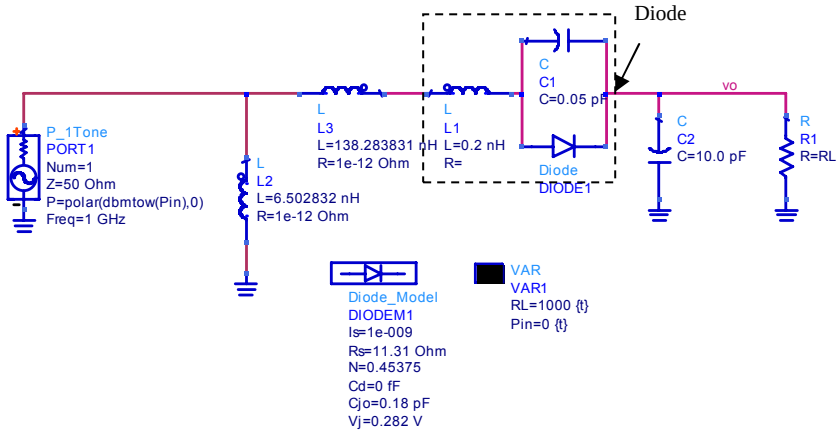


Figure 3.15 – ADS schematic of a matched diode with RC output network

A Harmonic Balance (HB) simulation is carried out at 1 GHz to find the Vo vs. Pin relationship. This is shown in Fig. 3.16 for different load resistors: 1K, 3K, 5K, 7K, 9K and 11K Ohms. It can be seen that at -25 dBm the output voltage increases with increasing load resistance but at higher input powers the output voltages converge.

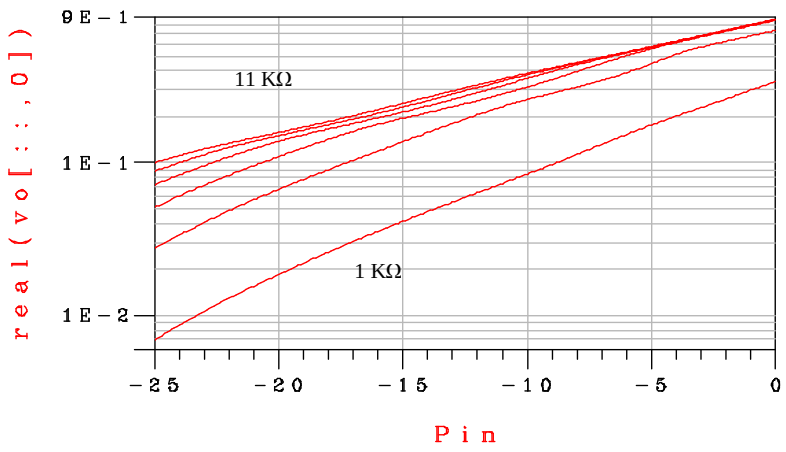


Figure 3.16 – Plot of output voltage vs. input power for different load resistances

The higher the load resistance, the higher is the RC time constant of the output network. This means that the baseband frequency is limited by the value of load resistance i.e. there is a trade off between output voltage and maximum data rate. Fig. 3.17 shows the simulated output waveforms for a data rate of 4Mbit/s for different load resistors: 1K, 11K and 21K Ohms.

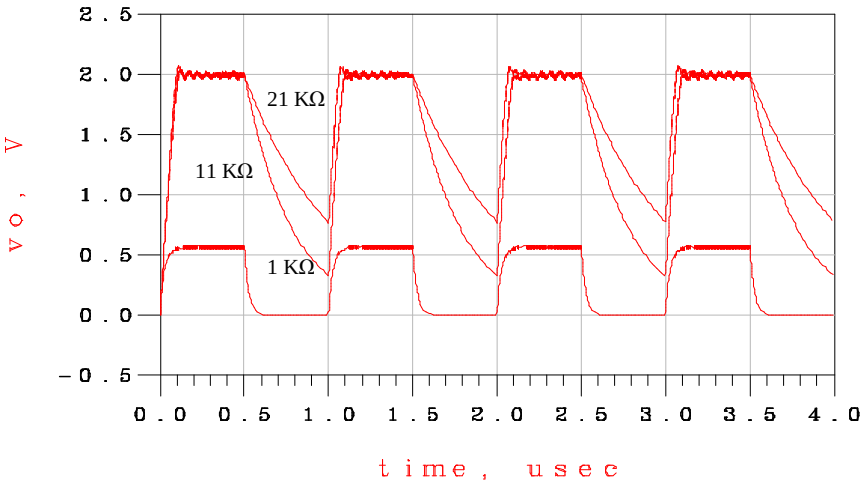


Figure 3.17 – Simulated waveforms for detector with R_L=1 KΩ, 11 KΩ and 21 KΩ

3.6 Switches

The antenna needs to be shared between the receiver and transmitter otherwise two antennas are required and in this case the circuit real estate will be greatly

increased. Instead, a two way switch can be used [7]. A switch can be constructed from a GaAs FET by connecting a control voltage to the gate and arranging the signal path to flow from the drain to source or vice versa. Fig. 3.18 shows the circuit model of a FET.

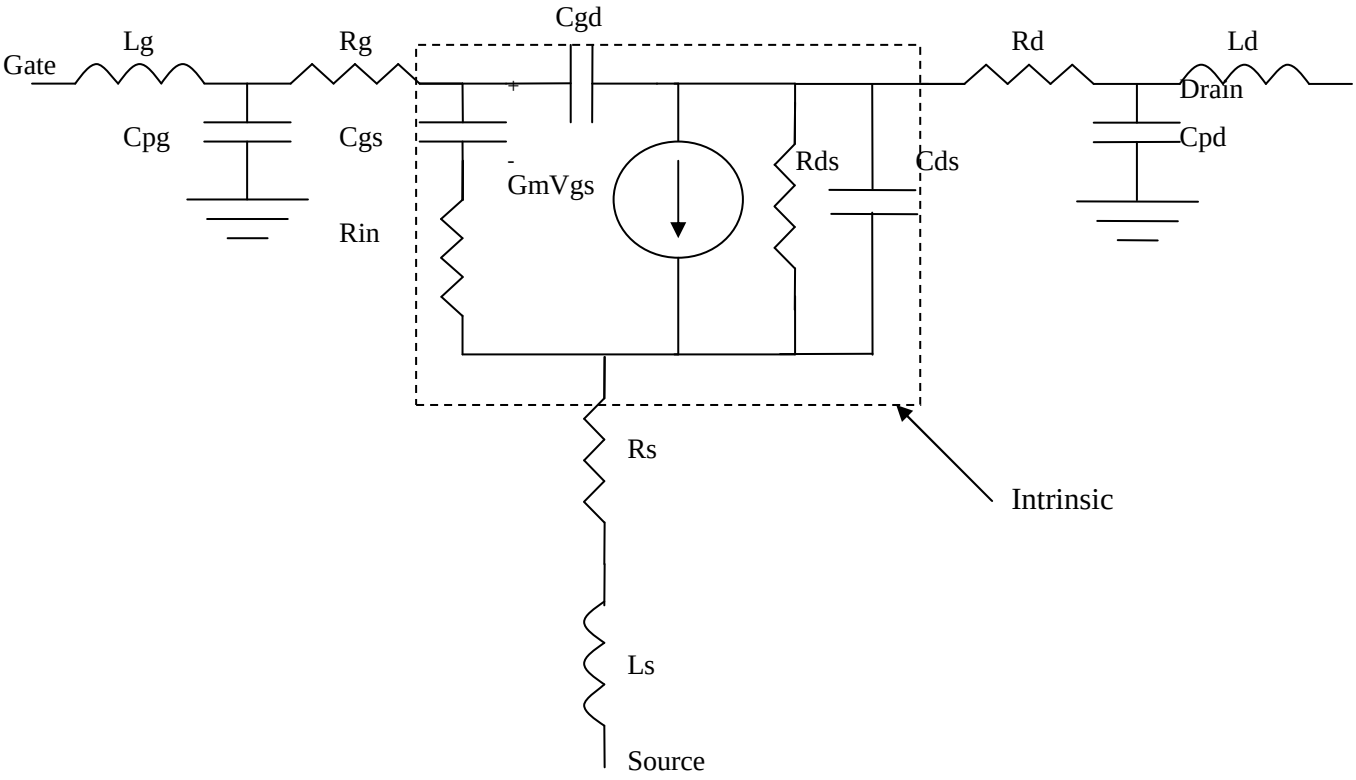


Figure 3.18 – Circuit model of a FET

When the control voltage applied to the gate is at pinch off or below R_{ds} is high and the drain is isolated from the source (see Appendix B) – the only connection beeing through C_{ds}. Conversely, when the gate voltage is zero R_{ds} is very low and there is an effective short circuit between the source and drain. In other words the FET acts like a voltage controlled resistor. In all cases the gate is isolated from the signal path: the only connection being through Cgd. Virtually no power is consumed by using a FET in this way as the gate is an effective open circuit. A two way switch can be constructed from two FETs as shown in fig. 3.19.

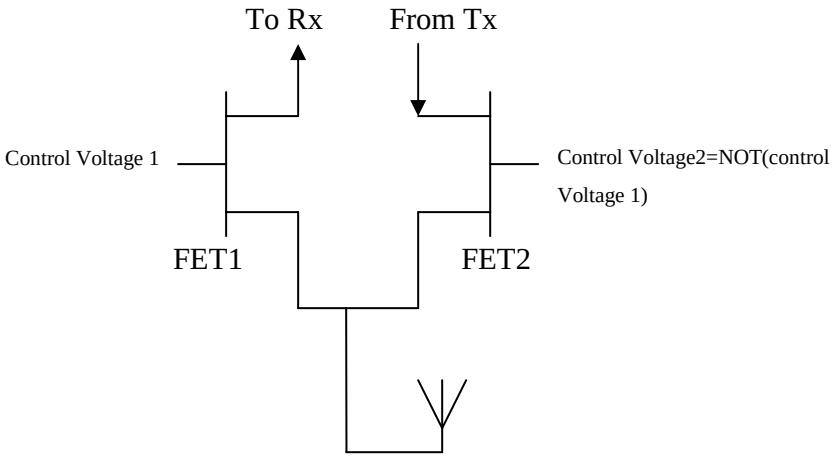


Figure 3.19 – Configuration of two way switch to allow antenna sharing

The two control voltages are the inverse of each other so that when FET1 is turned on, FET 2 is turned off and vice versa. When control voltage 1 is zero and control voltage 2 is at pinch off, the antenna signal is routed to the receive circuitry since there is a short circuit between the antenna and the Rx and an open circuit between the Tx output and the Rx. When the control voltage 2 is zero and control voltage 1 is at pinch off, the Tx output is routed to the antenna. Fig. 3.20 shows the simulated insertion loss for a two way switch using NE76038 transistors and fig. 3.21 shows the simulated isolation.

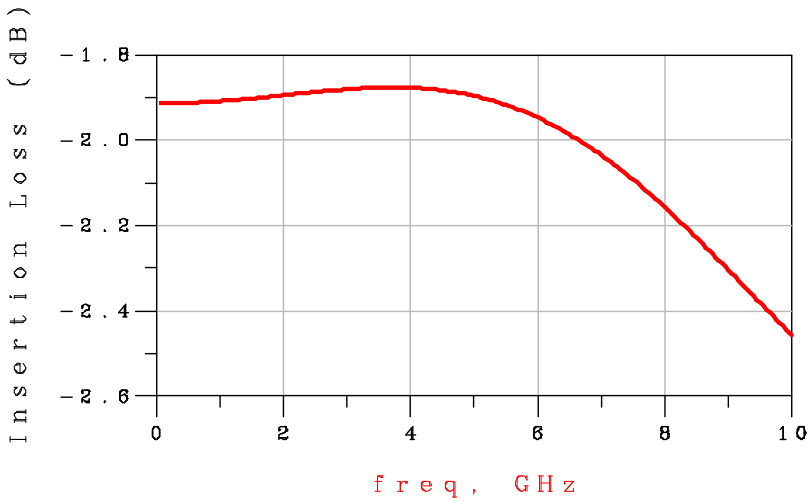


Figure 3.20 – Simulated insertion loss for two way switch using NE76038

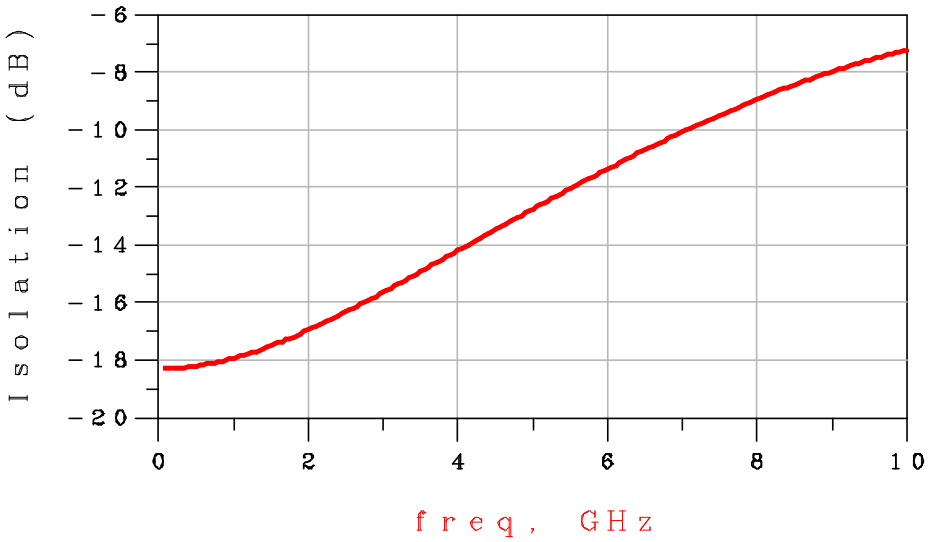


Figure 3.21 – Simulated isolation for two way switch using NE76038

A two way switch constructed on microstrip using two NE76038 transistors is measured to have an insertion loss of approximately 1 dB at 2.45 GHz whilst the isolation is measured to be approximately 12 dB.

3.7 Conclusions

This chapter has discussed the function each building block performs in a full transceiver. Also, a design procedure for each of the building blocks has been presented. Amplifiers using resistively loaded transistors have been used as these offer the best input and output match – thus making the whole transceiver more likely to work when it is assembled from the basic RF building blocks.

Negative resistance oscillators have been chosen as these are the most simple to implement at microwave frequencies and their performance is more easily predicted than feedback or dielectric resonator oscillators. These properties are due to the small number and simplicity of the passive components in the matching networks. A design procedure for negative resistance oscillators using the concept of the Return Ratio (RR) has been detailed. Measured results showed that the a.c./d.c. efficiency can be improved from 12.8 % for the standard oscillator to 29.3% for the oscillator designed for the RR equal to 1.26 at the operating frequency. It has also been shown that the start up time

and the relative level of the harmonics present in the oscillator output can both be changed as a function of the value of RR at the operating frequency.

Envelope detectors or simply detectors have also been discussed in this chapter. It has been shown that there exists a trade off between output voltage and the maximum data rate which can be detected. It has also been shown that the matching network and d.c. return can be incorporated into the same circuit by using a shunt and series inductance – thus reducing the number of components needed.

It has been shown how two transistors can be configured to form a SPDT switch. The switch works by using the two transistors as voltage controlled resistances: when the gate voltage is 0 there exists an effective short circuit between drain and source and when the gate voltage is at pinch off there exists an effective open circuit between drain and source. Configured in this way the power consumption of the switch is the voltage at the gate times the gate current. Since the gate current is of the order of 10 to 50 μA, the power consumption is negligible.

In conclusion, the proposed transceiver (see fig. 2.11) consists of a transmit oscillator with an a.c./d.c. efficiency of around 25 %. The receive circuitry consists of an amplifier with certain gain and isolation, an SRO and an envelope detector. The isolation of the amplifier must be as high as possible to reduce leakage of the SRO signal from the antenna. The amplifier must have good input and output matching in order to ensure maximum power transfer between each transceiver sub-circuit and also to ensure that the transceiver as a whole works. The amplifier will also add noise to the signal. This is kept relatively low by placing the loading resistor at the drain side rather than at the gate side. The amplifier passes the received signal to the SRO which is essentially the same as the transmit oscillator. The SRO output is passed to the detector which demodulates the received signal to baseband data. The antenna is shared by means of a SPDT switch.

Chapter 4

Super-Regenerative Transceivers

4.1 Introduction

As mentioned in Chapter 2, Super-Regenerative Receivers (SRRs) use a quenched oscillator as an effective high gain amplifier. The quench rate (ON/OFF rate) must be at least twice the data rate. In practice it is many times higher because in this case the quench component present at the output can be removed using a low order filter.

The oscillator is inserted between the receive amplifier and envelope detector as shown in fig.4.1.

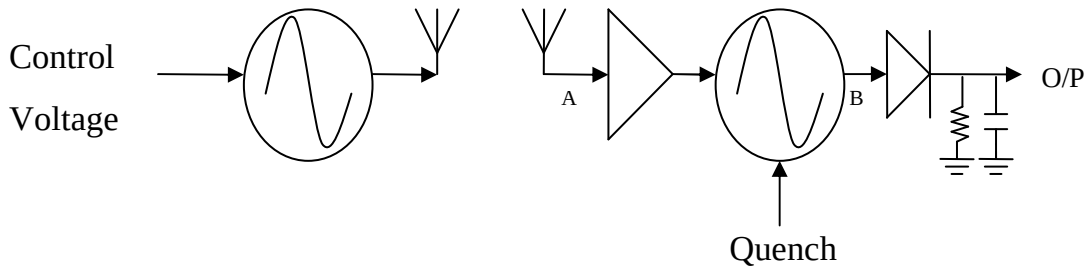


Figure 4.1 Block Diagram of a Super-Regenerative Transceiver

The amplifier in this case performs the dual function of boosting the antenna output and of isolating the receive oscillator signal from the antenna i.e. re-radiation.

Fig. 4.2 illustrates the principle of 'linear mode' super-regeneration. The linear mode differs from the logarithmic mode in that the input RF input causes the amplitude of the oscillations to increase whereas in the logarithmic mode the duration of the oscillation period increases when an RF signal is present.

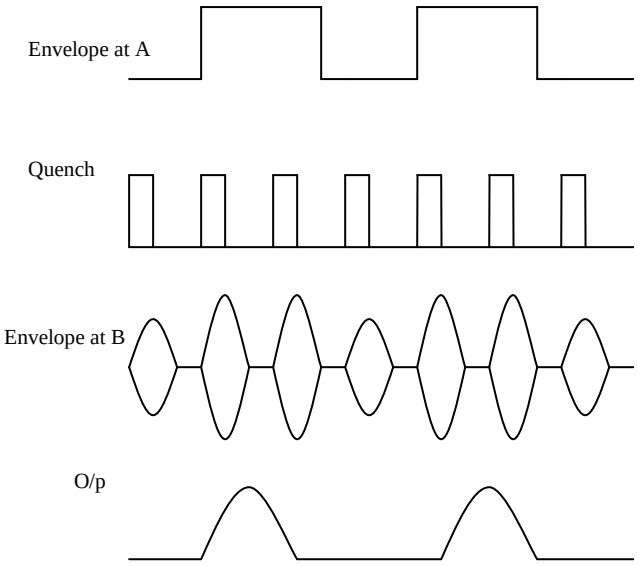


Figure 4.2 – Diagram showing the super-regenerative linear mode of operation

The amplitude of the waveform which builds up from noise in the presence of the quench signal is increased when an OOK wave is applied to the gate circuit side of the Super-Regenerative Oscillator (SRO). When the SRO output is detected or rectified, the quench component can be filtered out - leaving the baseband data.

4.2 Mathematical Analysis

Frink [1] presents an analysis of the super-regenerative detector in which the RF signal is represented by an a.c. voltage source and the effect of the quench signal by a switch which is assumed to open and close in accordance with the quench waveform. The impedance seen at the output of the oscillator is represented by a tuned series LC circuit and the negative resistance of the oscillator is represented by a negative valued resistor. This is shown in fig. 4.3.

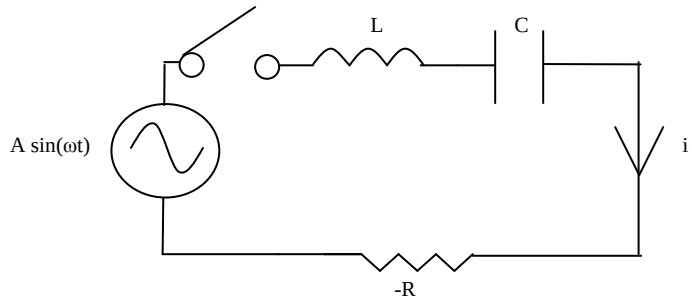


Figure 4.3 – Simplified equivalent circuit of super-regenerative receiver for analysis purposes

When the switch is closed, the voltage equation of the circuit can be written as:

$$A\sin(\omega t) = L\frac{di}{dt} - Ri + \frac{1}{C}\int i \cdot dt \tag{4.1}$$

Solving this equation (for details see Appendix A) we arrive at eq. 4.2

$$i = \frac{A\omega_r e^{\frac{R}{2L}t}}{\beta R}\sin(\beta t) - \frac{A\sin(\omega_r t)}{R} \tag{4.2}$$

The second term in eq. 4.2 represents a steady state sinusoidal current but the first term represents an oscillation which increases exponentially with time. This term is plotted in fig. 4.4. The frequency of the tuned circuit is 2.45 GHz, R is -10 Ω and the amplitude of the input signal, A, is 1. Fig. 4.5 shows the same function but with A=10. It can be seen that the oscillatory current reaches higher amplitude for a given period of time. Fig. 4.6 shows a plot where the conditions are the same as in fig.4 but the negative resistance is doubled to -20. It can be seen that the oscillations build up more quickly and reaches higher amplitude for a given period of time.

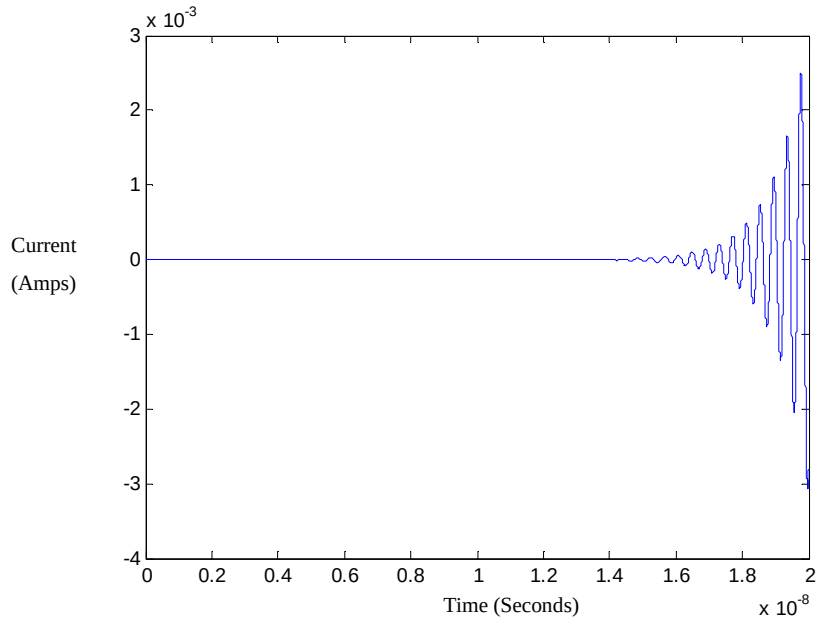


Figure 4.4 – Graph of the first term in eq. 4.2 with f=2.45GHz, A=1, R=-10 Ω

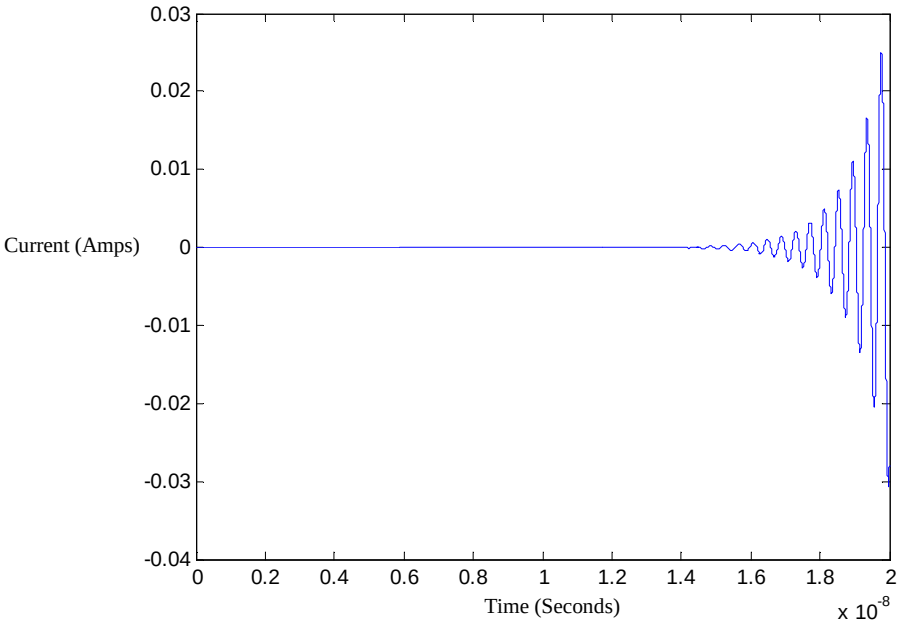


Figure 4.5 – Graph of the first term in eq. 4.2 with f=2.45GHz, A=10, R=-10 Ω

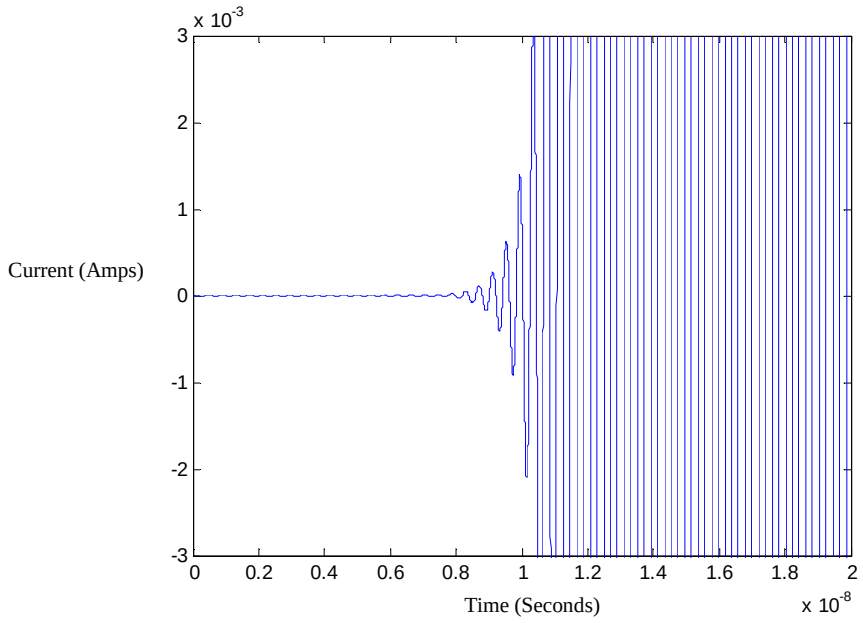


Figure 4.6 – Graph of the first term in eq. 4.2 with f=2.45GHz, A=1, R=-20 Ω, the scale is the same as fig. 4.5

These results indicate that for maximum output voltage the negative resistance of the oscillator should be high.

A problem with eq. 4.2 is that no limiting value is reached. Instead the oscillatory current increases exponentially with time. This problem can be overcome by adding a tanh function to the exponential term. X is an arbitrary constant which sets the limiting value of the amplitude:

$$i = \frac{A\omega_r e^{x\tanh\left(\frac{R}{2L}t\right)}}{\beta R}\sin(\beta t) \qquad (4.3)$$

Fig. 4.7 shows a graph of this function. It can be seen that the amplitude of the sine wave initially increases exponentially and then reaches a limiting value.

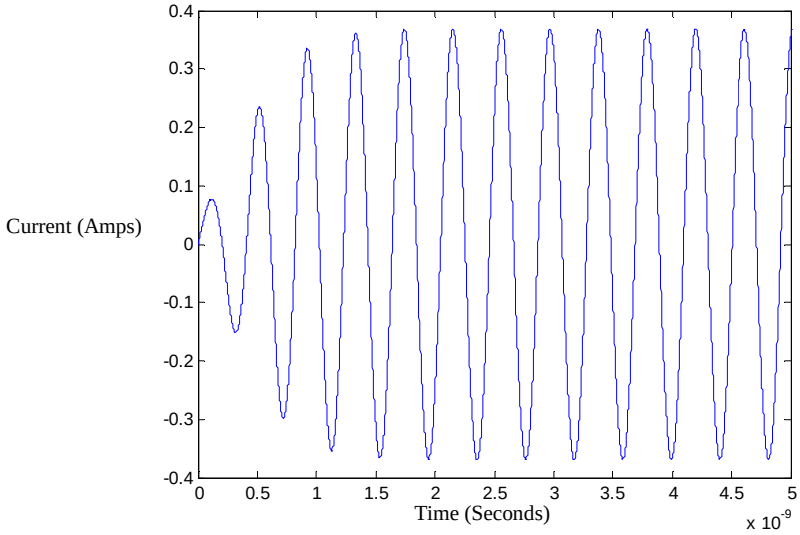


Figure 4.7 – Graph of eq. 4.3 with x=2

A delayed version of eq. 4.3 can be expressed as:

$$i = \frac{A\omega_r \left(e^{x\tanh\left(\frac{R}{2L}t - p\right)} - e^{x\tanh\left(\frac{-pR}{2L}\right)} \right)}{\beta R} \sin(\beta t) \tag{4.4}$$

p represents the quench period and the second exponential term ensures that the waveform equals zero before the exponential increase in oscillatory current.

The sum of successive quench cycles can be expressed as:

$$i = \frac{A\omega_r e^{x\tanh\left(\frac{R}{2L}t\right)}}{\beta R} \sin(\beta t) + \sum_{n=1}^{\infty} \frac{A\omega_r \left(e^{x\tanh\left(\frac{R}{2L}t - np\right)} - e^{x\tanh\left(\frac{-npR}{2L}\right)} \right)}{\beta R} \sin(\beta t) \tag{4.5}$$

This equation is plotted in fig. 4.8

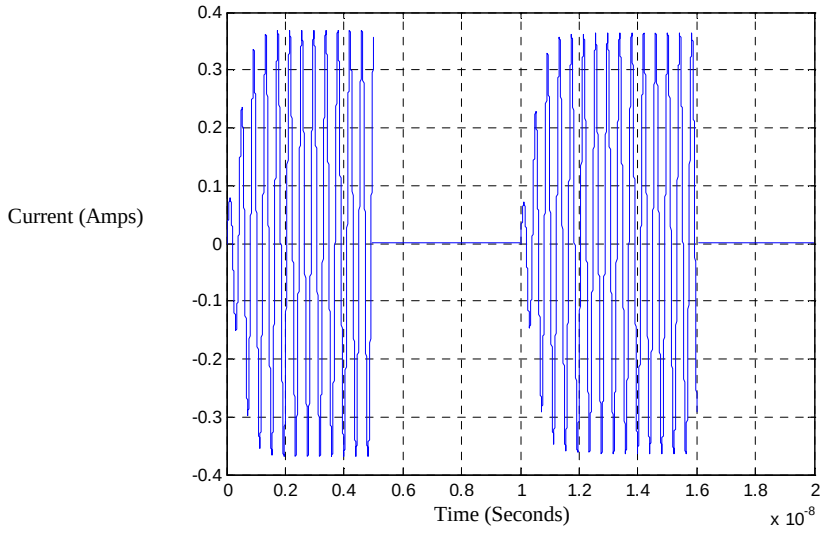


Figure 4.8 – Plot of eq. 4.5

4.3 Implementation of Super-Regenerative Transceiver

Putting the circuits discussed so far – amplifiers, oscillators, detectors and switches- together with the principles of super-regeneration we obtain a block diagram of a complete transceiver as shown in fig. 4.9. The bit slicer is a comparator with hysteresis which converts the two valued, noisy baseband output to logic levels e.g. 0 and 5 V.

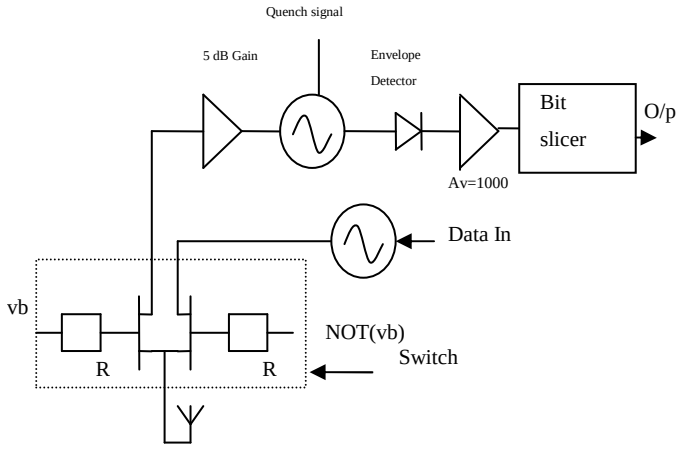


Figure 4.9 - Block diagram of complete super-regenerative transceiver

The circuit uses a simple architecture to lower the active component count and hence the power consumption. Previous GaAs based super-regenerative detectors [2, 3] recover the data by 'tapping off' the drain current via a load resistor. This realisation was tried but measurements indicated that this approach to introduce too much noise to the base-band signal. Instead, it is found that the addition of an envelope detector results in much better noise performance. In fact the received signal appears largely noise free on an oscilloscope.

The receiver consists of a low noise, low gain (5dB) amplifier, a super – regenerative oscillator and passive envelope detector which includes a 2nd order, Butterworth, RC low pass filter to filter out the carrier and quench signals. The circuit is designed as follows:

- The amplifier uses a transistor with resistive loading at the drain and is conjugately matched. The matching networks are realised using microstrip transmission lines. The noise factor is measured to be less than 3 dB.
- The receive oscillator and transmit oscillator use transmission lines and have a return ratio equal to 1.25 at the operating frequency
- The detector is matched to 50 Ω using series and shunt lumped inductances
- The switch is designed as detailed in section 3.6

The amplifier conducts 0.6mA and the super-regenerative oscillator conducts 1.3 mA. The supply voltage is 0.2 V. The overall power consumption is therefore 0.38 mW. The amplifier isolates the super regenerative oscillator signal from the antenna and hence prevents transmission during reception – i.e. re-radiation. The amplified OOK signal is applied to the gate port of the oscillator and the quenching signal is applied through a bias inductor to the gate port. Because the output resistance of the amplifier is 50 Ω, the oscillation frequency of the SRO is the same as in normal operation. The regenerated signal is then detected and is ready for base-band amplification and bit slicing. Bit slicing uses a comparator with hysteresis (op-amp with positive feedback) to convert the received signal to a clean, two valued, digital signal. The total number of transistors used in the transceiver is five – three of which consume power if we ignore the gate current flowing in the switching transistors. The base-band amplifier is an instrumentation amplifier from Analog Devices and the bit slicer is built around a standard LF353 op-amp.

All transistors are NE76038 and the diode (SMSD3012) is from Aeroflex-Metelics. The measured IV curve for the NE76038 transistor is shown in fig. 4.10. Also shown is the region where the amplifier and oscillator are biased.

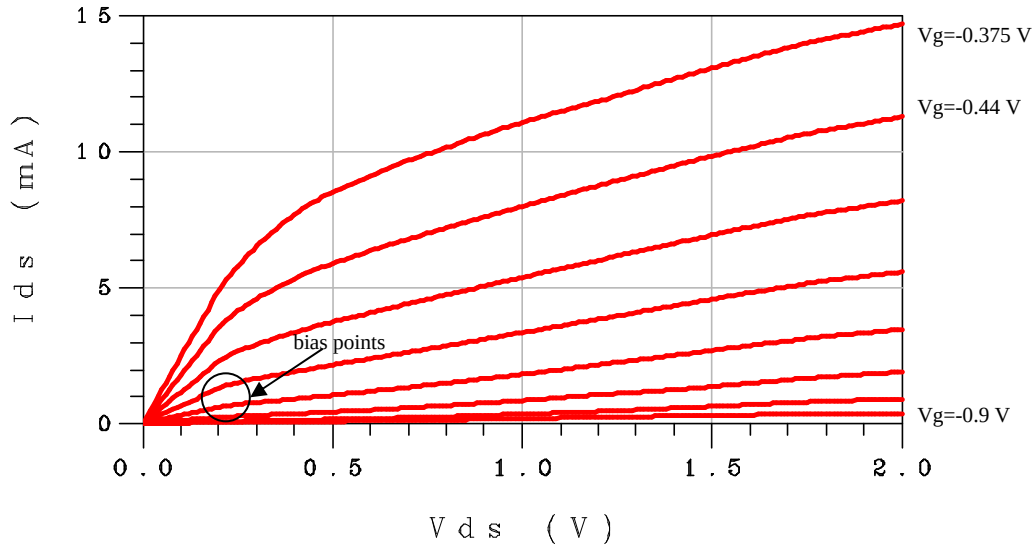


Figure 4.10 – Measured IV curve for NE76038

The circuit board has a dielectric constant of 3.48 and a thickness of 0.762mm. The matching networks and bias circuitry are realised using a mixture of lumped components from ATC and meandered transmission lines. The two switches are approximately passive and allow the antenna to be shared and have an insertion loss of 1dB. The switch is turned off by bringing the gate voltage to below pinch off (-0.9 V) and presents a low impedance path when the gate voltage is zero. Fig.4.11 shows a photograph of the circuit.

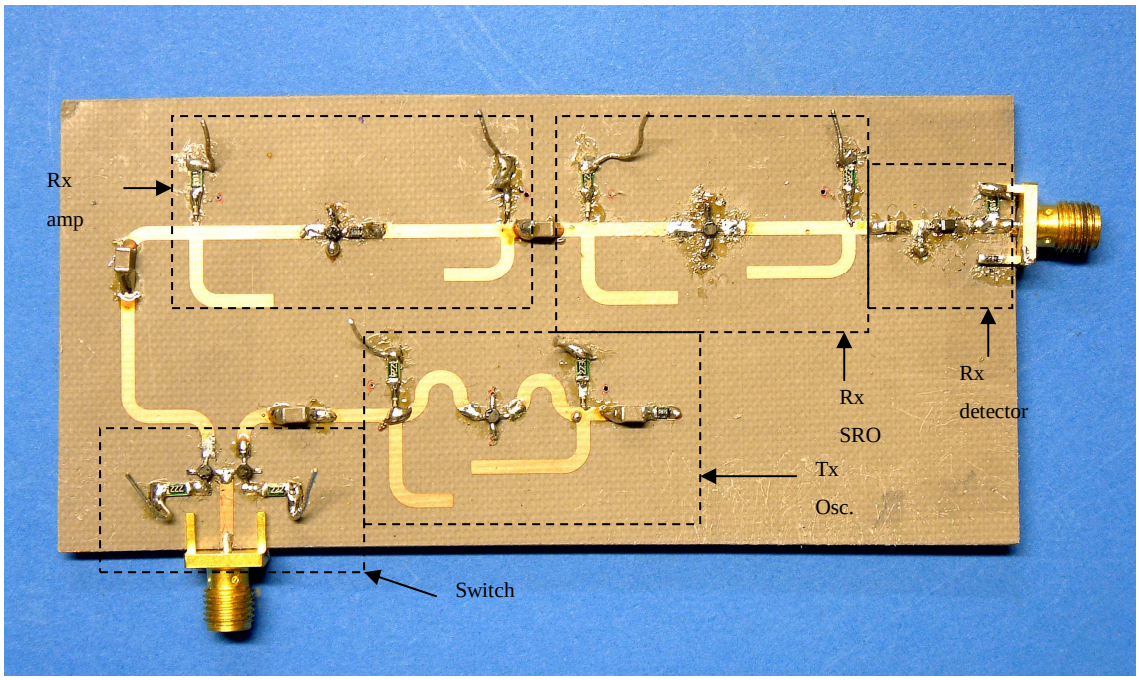


Figure 4.11 – Photograph of the designed super-regenerative transceiver

The transmitter is an oscillator operating at 2.48 GHz with an output power of -10 dBm. The base-band data is given a negative offset and is applied to the gate. The oscillator produces the carrier when there is a '1' and is pinched–off when there is a '0'. In this way data rates of plus 500Kbit/s can be achieved. Fig. 4.12 shows the variation in transmit oscillator output frequency as a function of gate bias.

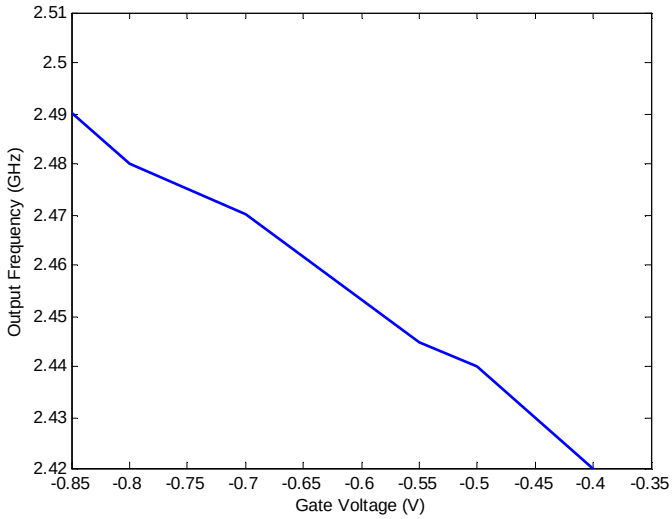


Figure 4.12 – Variation in transmit oscillator output frequency as a function of gate voltage

The main reason why the oscillation frequency varies with gate bias is the non-linearity of Cgs in the circuit model. From Fig. 4.12 it is clear that a variation in gate voltage of approximately 10% results in a frequency shift of 10 MHz. A tolerance of less than 10% in the power supply is not unrealistic and, moreover, if the Tx oscillator varies by ± 10% it will still be detected by the super-regenerative receiver – see fig. 4.14.

It was found that an input power as low as -85dBm was sufficient to produce a clean bit sliced output. This compares well with published results - see table 2.1 - although this result was measured with an instrumentation amplifier (AD620) connected at the output of the detector. Instrumentation amplifiers are specially designed so they are able to amplify extremely low level signals. The power consumption of the instrumentation amplifier is 6.5 mW. It is expected that a custom design using a short gate length CMOS process will lower this figure considerably as the shorter the gate length the lower the power consumption tends to be for a given circuit function.

Fig. 4.13 shows a plot of the a.c. detector output voltage versus input power at the switch. These results were obtained by injecting the signal from a signal source modulated by a baseband signal via an RF switch. The modulated signal was fed through a pair of antennas in order that there was no leakage of the baseband signal through the switch or power supplies. The path loss was measured with a Spectrum Analyser and then subtracted from the output power of the signal source in order to find the actual RF input power. Also plotted is the detector output voltage with a 5dB gain amplifier in front. It can be seen that the output voltage of the receiver is much larger than the amplifier plus detector – especially at low input powers. The super regenerative architecture ensures large output voltages for small input powers but also introduces noise to the signal. The noise of the receiver is also plotted. These results were estimated from an oscilloscope.

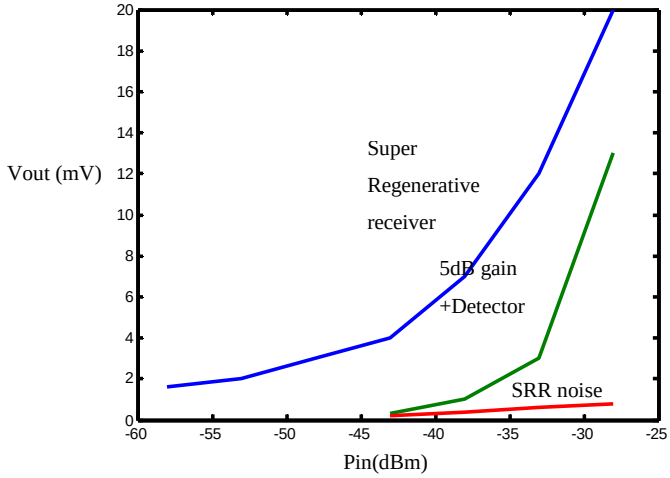


Figure 4.13 – Output voltage vs. input power for super-regenerative receiver

Fig. 4.14 shows the output voltage versus the RF input frequency for a fixed input power (-20 dBm). It can be seen that the bandwidth is approximately 20 MHz and that the output voltage falls off rapidly above 2.5 GHz.

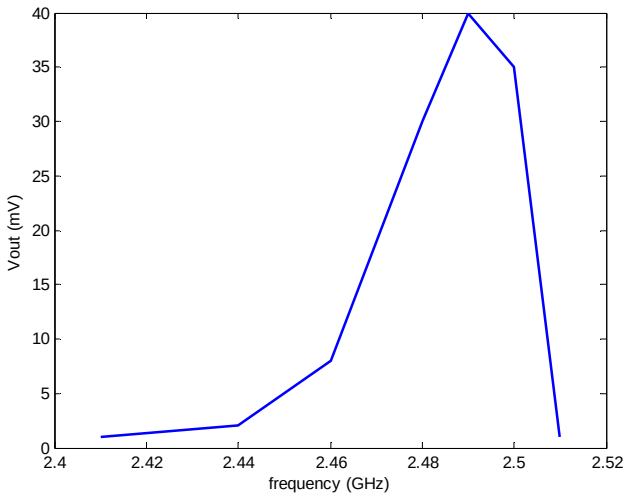


Figure 4.14 - Output voltage vs. input frequency for super-regenerative receiver

Every circuit in the transceiver described is matched to 50 Ω. Virtually all test equipment has 50 Ω output and inputs therefore it is normal practice to match all circuits to 50 Ω. A receiver with a higher (1000 Ω) normalising impedance is presented in section 4.6.

A complete super-regenerative, sub-milliwatt, transceiver using GaAs transistors has been designed and tested for the first time. Results indicate that ultra low power transceivers can be designed which produce useful signal levels for small input powers.

4.4 Super-Regenerative Transceiver with Low Transmitter Duty Cycle

If the transmit oscillator is only ON for a very short period of time relative to the length of a data ‘1’ then obviously the power consumed is lower than if the oscillator is ON for the same period of time as the data is at a ‘1’. This fact can be exploited to reduce the power consumption of the transmitter by duty cycling the transmit oscillator to a number lower than 50 %.

In order to operate with extremely low duty cycles, the binary data waveform is high pass filtered via a capacitor to produce a series of spikes which are related to the rise and fall of the data waveform as shown in Fig. 4.15. These spikes are used to trigger an oscillator via the bias network. Instead of high pass filtering the data waveform and using the resulting spikes to trigger an oscillator, a dedicated pulse generator may be used as a trigger.

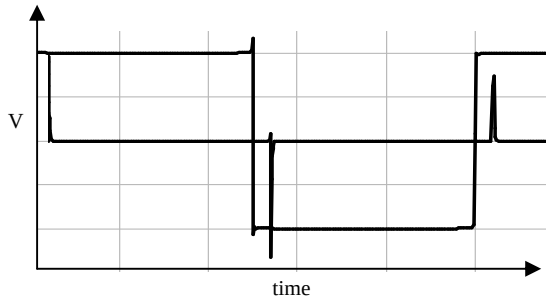


Figure 4.15 – Illustrative plot of input (data) and high pass filtered waveforms

If the spikes are given a negative offset and are applied to the gate of the oscillating transistor via the bias network then the circuit will oscillate during the narrow positive going spike and will be pinched off otherwise. The negative offset is necessary for depletion mode FETs as the transistor needs to be pinched off (i.e. drawing no current) when the circuit is not oscillating. The data waveform can be attenuated by voltage

division before being passed to the gate of the transistor via the bias network capacitor. Fig. 4.16 shows an ADS schematic of an oscillator with a capacitor in the bias network. The capacitor is used to high pass filter the binary data in order that a pulse - modulated carrier is produced at the output.

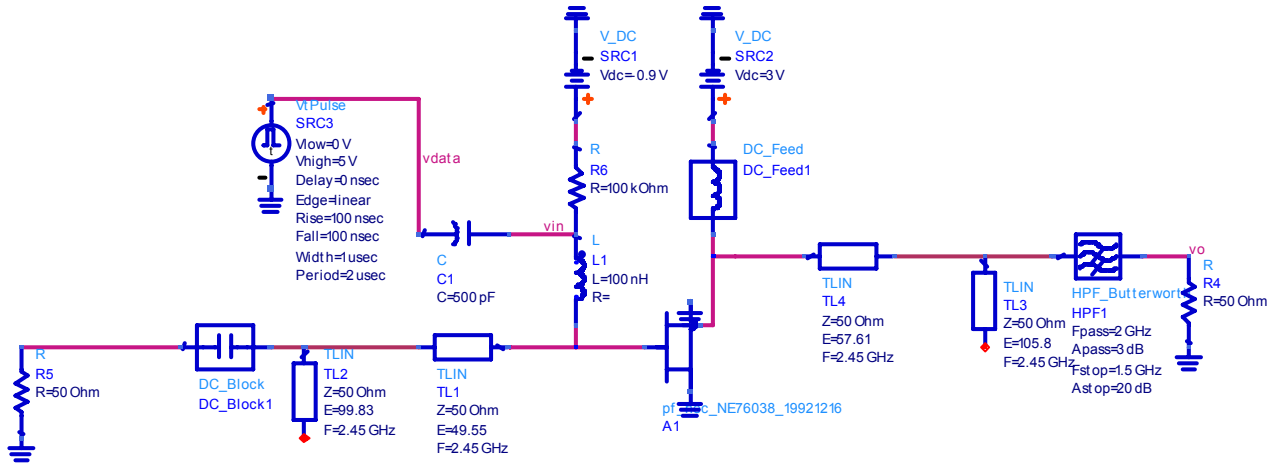


Figure 4.16 – ADS schematic of a pulsed oscillator

The data waveform is high pass filtered via a capacitor and then added to a d.c. offset of -0.9 V through a resistance of 100 kΩ. The composite waveform is applied through an RF choke inductor and is used to bring a transmission line oscillator in and out of oscillation. The output RF waveform is high pass filtered to remove the data pulses. In practice the spectra of the input pulses and the output RF pulses are far enough apart that a simple capacitor can be used. Fig. 4.17 shows the simulated transient waveforms for the circuit.

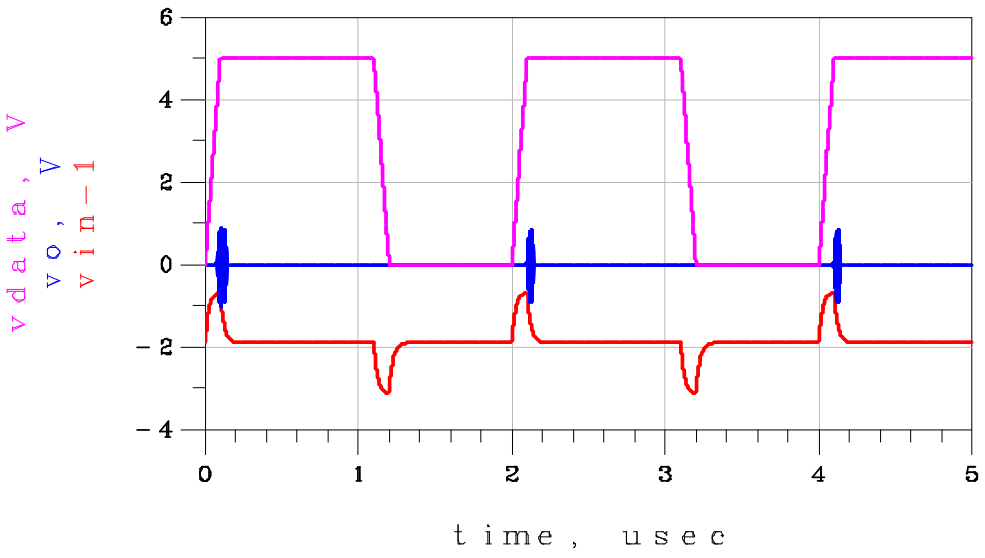


Figure 4.17 – Simulated data (pink), filtered (red) and output RF pulses (blue) for circuit in Fig. 4.16

The width of the pulse is controlled by the value of capacitance and the rise and fall time of the data waveform. When the triggering voltage rises from transistor pinch off to its maximum value the oscillator begins to oscillate and stops oscillating when the triggering waveform falls back to pinch off. During the negative going portion of the data waveform the transistor is still pinched off so the circuit does not oscillate.

A problem arises with the architecture described so far if two or more consecutive 1's occur. In this case, only one logic 1 is transmitted because there will be only one positive going spike triggering the oscillator. This problem can be resolved by clocking the data and then performing a Boolean AND operation on the clock and the data. This ensures that a number of negative to positive transitions occur equal to the number of data 1's. At the receiver, the narrow RF pulses are amplified, regenerated and envelope detected. Then the baseband data are amplified and subsequently bit sliced (bit slicing converts a two valued waveform with noise to a clean output with two logic values e.g. 0 and 5V). The output at this point consists of a series of narrow pulses with 0V representing logic 0 and 5 V representing logic 1. In order to recover the missing portions of the 1's a mono-stable circuit with a time constant dependent on an external resistor and capacitor is used. The mono-stable will output a 1 when it is input a 1 but will hold this level for a time dependent on the external resistor and capacitor.

This approach works in that a 50 % duty cycle can be reproduced for the baseband output but a drawback is that a fixed data rate must be used. In order to accommodate

varying data rates a bank of switch-able resistors or a voltage controlled resistor in the monostable circuit could be used.

Fig. 4.18 shows the measurement set up used to test the concept. The oscillator works at a drain voltage of 0.56 V but conducts less than 50 μA. This is a power consumption of less than 30 μW. The oscillator considered in this section operates at 2.48 GHz with a drain bias of 0.56 V and conducts 0.7 mA under normal operating conditions. The output power is -10dBm. This is an a.c./d.c. efficiency of 25.5%. Note that the super-regenerative receiver includes the base-band amplifier and bit slicer. The Pseudo-Noise (PN) code sequence generator was used to simulate a bit sequence and the antennas ensure no leakage of the baseband signal from input to output. The bias inductor should be large enough at the operating frequency to be an effective open circuit. The bias capacitor should be chosen to provide output pulses of the required width. The system works as well as the basic super-regenerative transceiver as the peak output voltage of the Tx oscillator remains constant if the pulse width does not exceed 10 μS (for this particular circuit) and the Rx output remains constant if the input RF pulses do not exceed the bandwidth of the receiver. The pulse width used is 25 μS and the bit rate is 7 kbit/S. Higher data rates could be used but the duty cycle (the pulse width remaining constant) and hence the power consumption will increase.

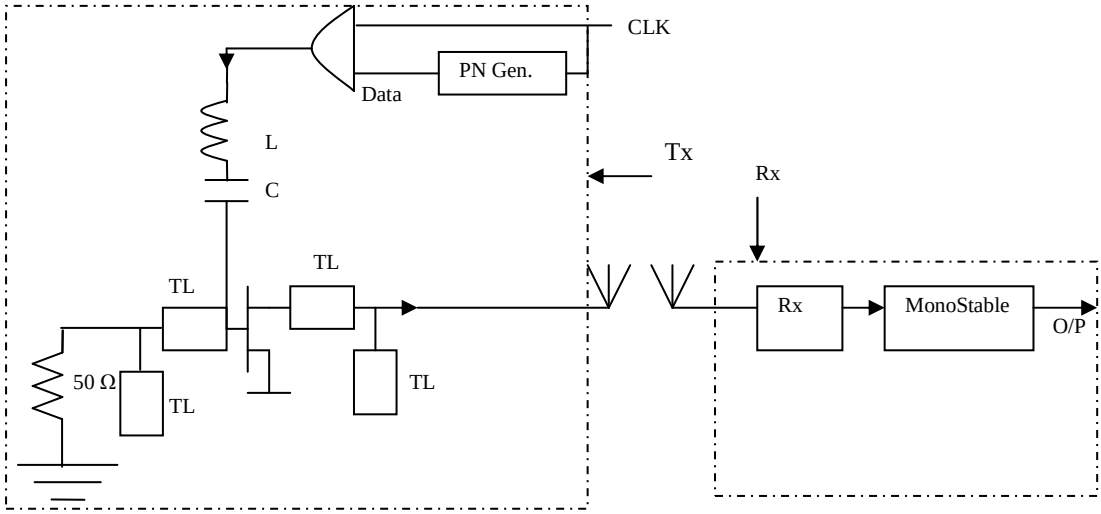


Figure 4.18 – Measurement set-up to test low duty cycle transmitter

Fig. 4.19 shows the waveforms at various points in the system. Note that the result of ANDing the clock and the data produces a waveform with the number of positive going transitions equal to the number of data 1's.

A low pass RC filter is connected to the output of the monostable and has a pass band high enough to allow the data waveform to pass through but low enough to remove any narrow glitches which may be present. At this point the signal can be bit sliced again if the effect of the low pass filter is to introduce an unacceptable degree of rounding to the transitions. All logic was implemented using the CMOS 4000 series.

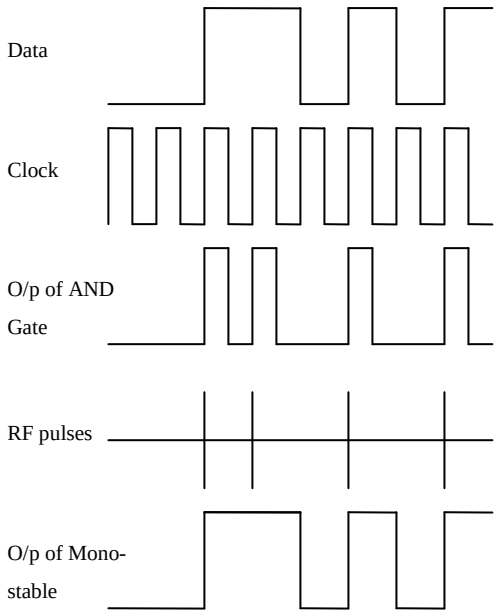


Figure 4.19 – Waveforms at various points in the low duty cycle transmitter system

Fig. 4.20 shows an example of measured RF pulses.

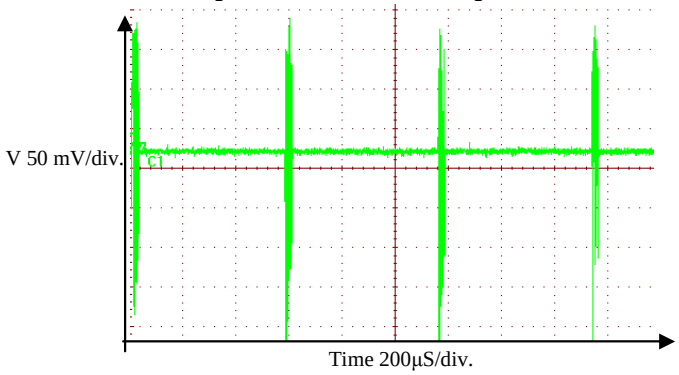


Figure 4.20 – Measured RF pulses

The smallest achievable output RF pulse width is around 10µS. Below this the peak voltage of the RF pulse decreases. In order to overcome this problem, two circuits for obtaining shorter RF pulses were devised. The first is shown in Fig. 4.21. This is a

standard transmission line RF oscillator designed as detailed in Chapter 3.3. Bias circuits are omitted for clarity.

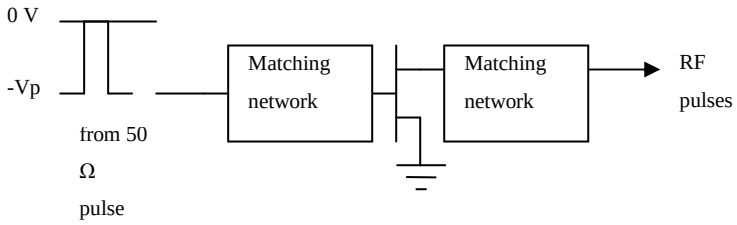


Figure 4.21 – Circuit for obtaining short RF pulse

The circuit is biased at pinch off (-0.9 V) with some positive value on the drain (0.56 V). The input baseband pulse results in a change of operating point and the circuit oscillates during the positive portion of the input pulse. The smallest RF pulse width achieved before degradation in output voltage was 1 μS. The circuit achieves smaller pulse widths than the standard circuit because the bias resistor, inductor and bypass capacitor of the circuit previously described limit the high frequency response.

The second circuit for obtaining narrow RF pulses is shown in Fig. 4.22.

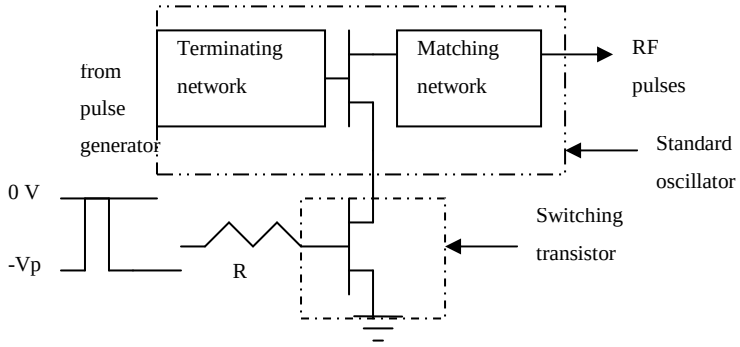


Figure 4.22 – Second Circuit for obtaining short RF pulse

Again the circuit uses a standard RF oscillator (with RR=1.25 at the operating frequency) but this time modulation is achieved via the switching transistor in the source circuit of the oscillating transistor. When a negative voltage below pinch off is applied through the resistor to the gate of the switch transistor there is, in effect, an open circuit between the drain of the oscillating transistor and ground. When the gate of the switch is brought up to 0V by the data waveform current flows and the circuit oscillates.

The shortest RF pulse width achievable before loss of output voltage was 0.5 μS for this circuit. The experimental results just described from these two circuits indicate that extremely low duty cycles can be achieved.

4.5 Super-Regenerative Transceiver with Low Receiver Duty Cycle

The same principle of turning the circuit ON for a period considerably less than the bit period described in the previous section can be applied to the receive circuitry. In this case an input composed of short RF pulses is applied to the receiver. A quench signal synchronised to the input data and with a pulse width greater than the RF input pulse width (2x in this particular case) is given a negative offset and applied to the gates of the amplifying and oscillating (super-regenerative) transistors. In this way the receive amplifier and oscillator are turned on only when a '1' or a '0' is 'expected'. Fig. 4.23 shows the measurement set up used to test the concept.

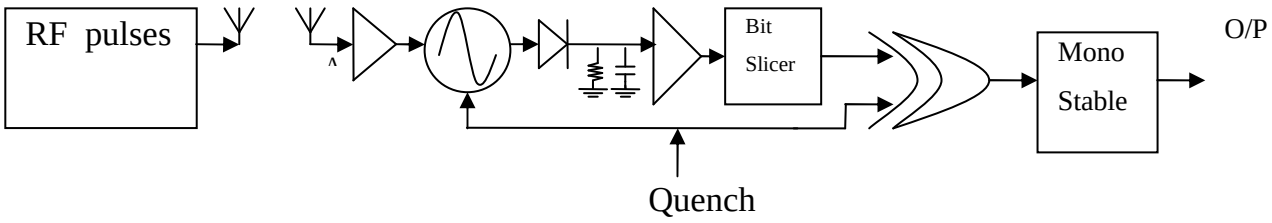


Figure 4.23 – Measurement set up to test low duty cycle Rx concept

Fig. 4.24 shows the waveforms at various points in the system. It can be seen that the RF output contains the quench signal as well as the data. Usually the quench period is at least twice the frequency of the input data and can therefore be filtered out. In this case however the quench signal is the same as the data period. It can be seen from fig. 4.24 that the data can be recovered by exclusive Or–ing the Rx output with the quench signal. This leaves a series of short pulses related to the data 1's. The missing portions of the data can be recovered in exactly the same way as in the previous section i.e. with

a monostable. The quench waveform in fig. 4.24 is shown to be much wider than the RF pulses for clarity - in practice it is twice the width.

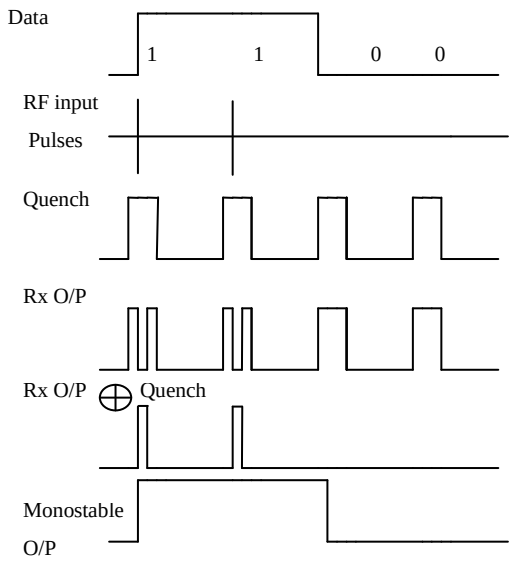


Figure 4.24 – Waveforms for low duty cycle receiver

The hybrid prototype detailed in section 4.4 is used for the RF part. The additional baseband circuitry (logic and monostable) is realised using the CMOS 4000 series. Fig. 4.25 shows the ac, pk-pk, output voltage of the RF part of the receiver.

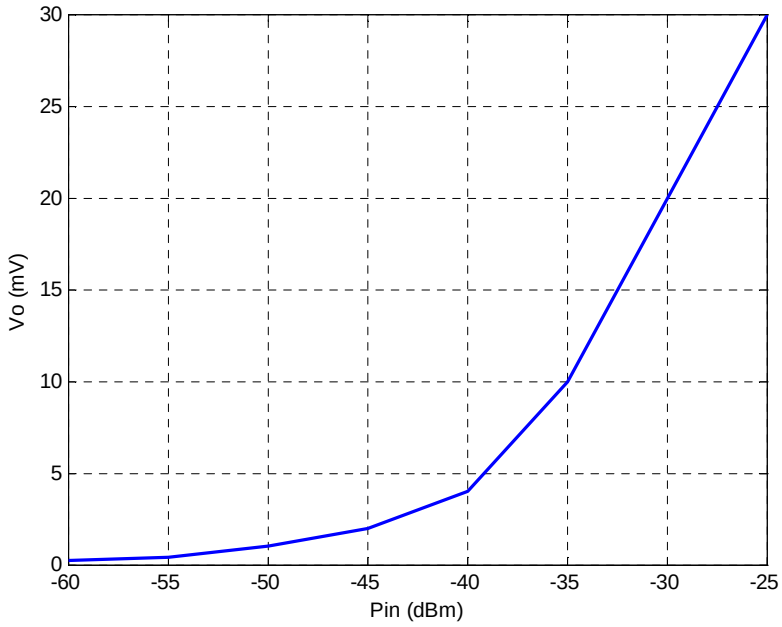


Figure 4.25 – Output voltage vs. input power for low duty cycle receiver

The receiver achieves an output of 1 mV for an input of -50 dBm. This is many times larger than the output of the amplifier cascaded with the detector (see section 4.4) and yet consumes only 10 μW – a 97.5% reduction in power over the basic super-regenerative receiver which is turned ON all of the time.

As with the transmit circuitry, if the data rate is increased then so does the duty cycle (the pulse width remaining constant) and the power consumption. The measured results in Table 4.1 illustrate this effect.

Data Rate	Quench pulse width	Duty Cycle	Power consumption
800 bit/S	50μS	2%	10μW
50 kbit/S	10μS	25 %	100μW

Table 4.1 – A comparison between Rx data rate and power consumption

In order for the duty cycled receiver to work the quench waveform needs to be synchronised to the input RF pulses. Synchronisation can be achieved by using a stable frequency source matched to the input data and by varying the position of the quench pulses in time until a lock is achieved. Two 555 timers and an inverter can be used to achieve an output of narrow pulses whose position in time can be altered as a function of a control voltage. Fig. 4.26 shows an example of a monostable-connected 555 timer circuit. Two such circuits are connected in cascade via an inverter. The control voltage is applied to pin 6 of the first monostable and the pin 3 output of the first monostable is fed through an inverter to pin 2 (trigger) of the second monostable.

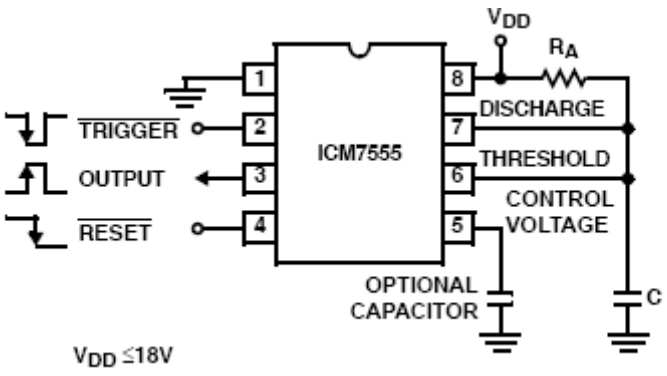


Figure 4.26 – Monostable connected 555 timer circuit

Fig. 4.27 shows the relevant waveforms. The two timers are connected as monostables. The first timer's output duty cycle can be altered as a function of the applied control voltage. The output is inverted and then used to trigger the second monostable. In this way variations in duty cycle are translated into varying delays.

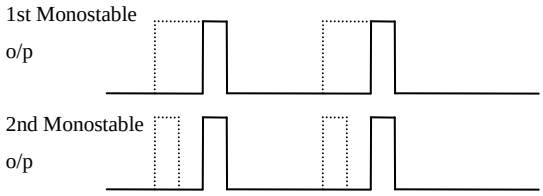


Fig. 4.27 Synchronisation of quench waveform by translating variation in duty cycle into variations in delay

The extra power consumption of the synchronisation circuit is 600 μW. Again, custom design should allow this figure to be drastically reduced.

It has been shown that, by duty cycling the receiver, the power consumption of the RF circuitry can be reduced to 10 μW. Duty cycling the receiver does lead to some degradation in performance because only one sample is taken per bit period. This is contrast to normal operation where at least two samples are taken. However, the performance is still much better than that provided by an amplifier and envelope detector. The reduction in power arises because the receive circuitry is turned ON for a short period of time compared to the bit period. The low duty cycle receiver may find application in short range, low data rate links where ultra low power consumption is required for example the SpeckNet project.

4.6 High Impedance Transceiver

The circuits described in the previous sections (4.3 – 4.5) are based on circuitry designed in a 50 Ω environment. In this section, a receiver is discussed which is designed to have a normalising impedance of 1000 Ω. It will be shown that this maximises the output voltage of the receiver and therefore relaxes the specifications of the baseband amplifier.

Ref [4] describes a high data rate (10 Mbit/s) super-regenerative receiver. The circuit achieves this high data rate by synchronising the quench waveform with the

input data but it is the detector in [4] that is of most interest here. The detector in [4] converts a modulated voltage into a demodulated voltage. This is in distinction to the detectors previously described in this work. They operated as power in/voltage out demodulators. The common drain detector schematic is shown in fig. 4.28.

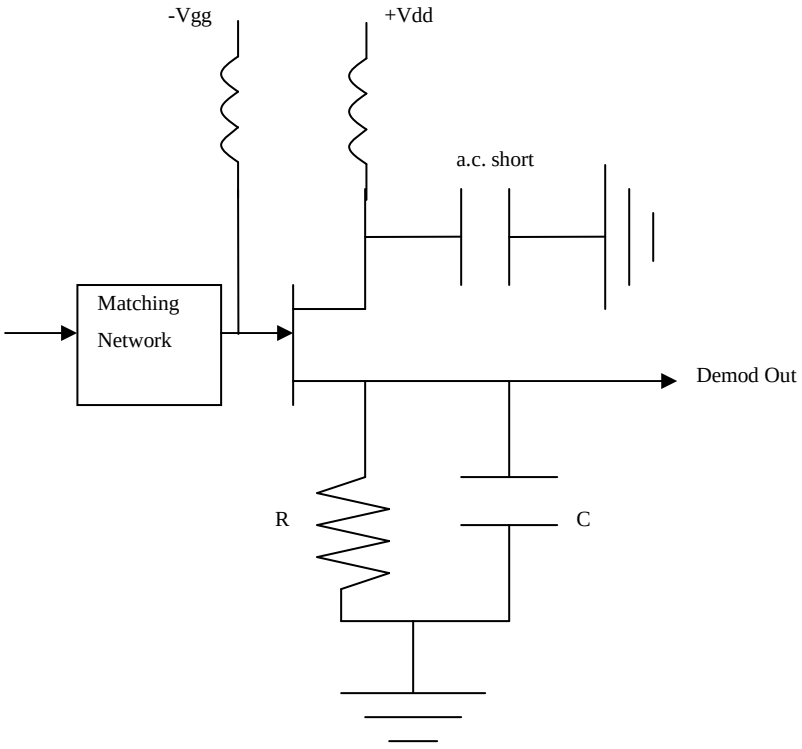


Figure 4.28 – Schematic of common drain detector

Use of the common drain envelope detector allows the designer to maximise the voltage at the input to the detector, and hence the system output voltage, by using a higher normalising resistance to match the receive amplifier output (the receive amplifier input is still matched to 50 Ω), the input and output resistance of the super-regenerative oscillator and the input resistance of the detector. The reason the output voltage is maximised is that, for a given power, the relation

$$Power = \frac{V^2}{R} \tag{4.6}$$

shows that the voltage will be larger for a larger resistance i.e. for a doubling of resistance the voltage will increase by $\sqrt{2}$. This is a refinement of the techniques described in [4] in that, previously, a high impedance load was presented to the output of each stage rather than individually matching the relative input and outputs to a

certain normalising resistance. Using the current technique reflections are minimised and maximum power is transferred between each stage.

The high normalising resistance precludes the use of the kind of negative resistance oscillator previously described. Instead a feedback circuit based on a modified Colpitt's oscillator is used. Fig. 4.29 shows a schematic diagram of the circuit.

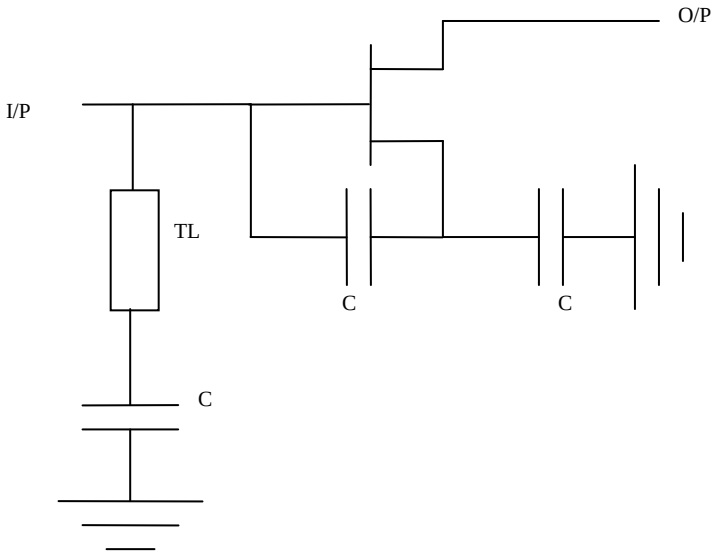


Figure 4.29 – Schematic of modified Colpitt's oscillator (bias circuit not included)

A circuit consisting of a 50 Ω input and high output impedance amplifier, a high impedance oscillator and detector, 50 Ω transmit oscillator and a two way switch was designed. The designed circuit was realised using microstrip transmission lines on a substrate with a dielectric constant of 3.48 and a thickness of 0.762 mm. Lumped inductors and capacitors from ATC were used for the matching networks. The transistor is the NE76038. The supply voltage is 0.75 V. The current drawn by the amplifier is 0.2 mA and the current drawn by the super-regenerative oscillator is 0.7 mA. The detector consumes less than 50 μW so the total power consumption of the receiver is approximately 675 μW.

To summarise:

- The amplifier is designed to have a a 50 Ω input impedance and a 1000 Ω output resistance
- The oscillator is based on a modified Colpitt's configuration with a capacitive feedback network and a meandered transmission line/ capacitive resonator

- The detector converts an RF voltage to a demodulated voltage and uses a common drain configured transistor. An LC matching network provides a 1000 Ω input impedance
- The transmit oscillator is a standard 50 Ω negative resistance oscillator designed to have a RR equal to 1.25 at the operating frequency.
- The antenna is shared via a switch as outlined in Chapter 3.6

Fig. 4.30 shows the measured input match to the transceiver i.e. looking into the switch when the receiver is turned on. It can be seen that the return loss is approximately 30 dB at 2.47 GHz and 15 dB at the receiver operating frequency of 2.5 GHz.

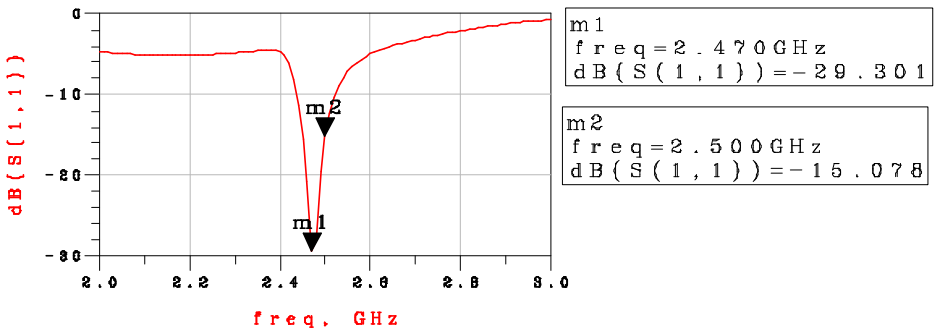


Figure 4.30 – Input match of the high impedance receiver

Fig. 4.31 shows the measured a.c. output voltage versus the input power for a quench rate of 10 MHz and a data rate of 10 KBit/s. These results were obtained by injecting an RF pulse train at varying powers into the receiver and measuring the peak to peak voltage of the RF output on an oscilloscope with an input impedance of 1 MΩ and a shunt capacitance of 20 pF.

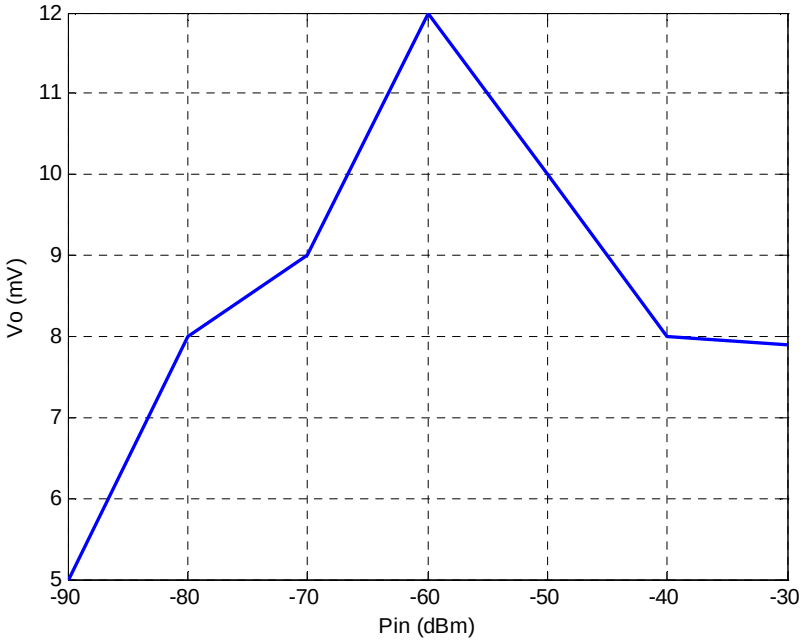


Figure 4.31 – Output voltage vs. input power of high impedance receiver

It can be seen from fig. 4.31 that the output voltage is still at a usable level of 5 mV for an input power of -90 dBm and rises to a peak voltage of 12mV for Pin=-60 dBm. The circuit exhibits a sort of AGC since the variations in output voltage are very small. In fact the output voltage drops when the input power increases above -60 dBm. An input power of -90 dBm is equivalent to a transmitter with an output power of -10 dBm over 60 m distant from the receiver assuming 0 dB gain antennas and an operating frequency of 2.5 GHz. Fig. 4.32 shows the frequency response of the high impedance receiver.

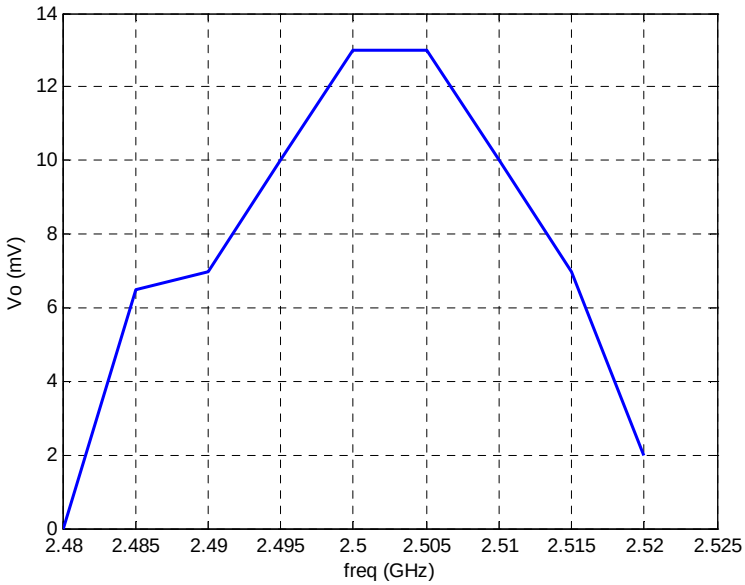


Figure 4.32 – Output voltage vs. input frequency of the high impedance receiver

It can be seen from fig. 4.32 that the centre frequency is 2.5 to 2.505 GHz and that the 0.707 bandwidth is approximately 15 MHz. This obviously reflects poor selectivity and is a well known problem with super-regenerative receivers. However, this feature can be regarded as positive as it accommodates varying input frequencies i.e. it allows for variations in the transmit frequencies of communicating specks.

4.7 Conclusions

This chapter has introduced the reader to the concept of super-regeneration: an oscillator which is quenched such that oscillations periodically build up, reach a steady state and then die out acts as a high gain amplifier. Thus, an OOK signal which is applied to the gate port of an oscillator is sampled at a rate of at least twice the input data rate and appears at the drain port of the oscillator with greater amplitude. The output signal also contains also contains an RF signal modulated at the quench frequency. When the RF signal is demodulated the quench component can be filtered out with a low pass filter. The higher the quench component is relative to the data rate the more precisely the quench component can be removed.

A mathematical analysis of an SRR has also been presented. The analysis can be reduced to the statement that the greater the negative resistance of the oscillator the larger is the effective amplification of the SRO. The reader is referred to appendix A for a more detailed treatment of the analysis. It has also been shown that the equation describing the output of the SRR can be modified such that successive quench cycles as well as a limiting value for the oscillator output are included.

The chapter continues with a detailed description of the implementation of an OOK, super-regenerative, hybrid prototype transceiver operating at 2.4 GHz and with a data rate of 200 kBit/s. The transmitter consists of directly modulated negative resistance oscillator designed using the RR method described in section 3.4. The oscillator is biased such that consumes 400 μW and achieves an efficiency of around 25 % i.e. the output power is 100 μW or -10 dBm. Modulation is achieved by biasing the oscillator at positive drain voltage and the gate at pinch off. A data '1' is produced by raising the gate voltage above pinch off and then bringing the voltage back to pinch off. In this way a burst of RF carrier is generated when there is data '1' and the transistor is pinched off and draws no current during data '0's. Using this arrangement virtually no power is consumed during data '0's and so a saving of at least 50 % is achieved over using a switch to modulate the output of an LO. The receiver consists of an isolation amplifier, SRO and detector. In total the receiver consumes 380 μW and generates an output voltage of 2 mV for an input power of – 55 dBm. If we assume antennas with 0 dB gain and a baseband amplifier with an ability to amplify signals as low as 1 mV this translates into a maximum operating range of 4 m.

In section 4.4 the novel concept of duty cycling the transmitter is detailed. The basic concept is to utilise the discontinuous nature of OOK signals to reduce the power consumption of the transmit circuitry. Instead of transmitting a burst of carrier for the total time the data is at a high logical level, the transmitter only generates a burst of carrier for a short period of time relative to the time the baseband binary signal is high. The correct duty cycle is then reproduced by additional baseband circuitry connected at the RF receiver output. It is shown that the RF circuit power consumption can be reduced by 97 % with no loss in performance as long as the RF pulses do not exceed the bandwidth of receiver.

Section 4.5 applies the same concept described in section 4.4 to the receiver. In this case narrow quench pulses are used to cycle the whole receiver i.e. the amplifier and the SRO. The reduction in power consumption relative to the static d.c. power

consumption is always less than the reduction for the duty cycled transmitter as the pulse width of the quench signal must be wider than the input RF pulses for successful operation. Despite this a reduction in power consumption of 95 % was achieved. The major drawback of the technique is that the quench signal must be synchronised to the input RF pulses although a synchronisation mechanism based on monostables is discussed in which the position of the narrow quench pulses can be shifted back and forth in time as a function of a control voltage. It is envisaged that a training sequence can be used so that a control loop is used to vary the control voltage until a 'lock' is achieved.

In section 4.6 a design methodology for receivers with increased output voltage is presented. It is important to maximise the output voltage of the RF receiver as this relaxes the specifications of the receive baseband amplifier thus reducing overall power consumption. Maximising the output voltage of the receiver will also increase the operating range of the transceiver.

In conclusion, this chapter has provided a description of the operation of super-regenerative receivers and has provided an equation to describe the output waveform of a quenched oscillator. An implementation of a super regenerative transceiver has been described and measured results have been presented. It has been shown that the power consumption of a standard transceiver can be as low as 400 μW for both transmit and receive circuitry. In addition, it has been shown that the power consumption of the transceiver can be reduced by approximately 95 % by duty cycling both the transmitter and receiver circuits. Also, it has been shown how the output voltage and hence operating range of the complete transceiver can be greatly increased by using a larger normalising impedance for the receiver.

Future work should concentrate on designing a complete control loop to synchronise the receiver quench pulses to the input data pulses. Another important piece of work to be followed up is to design a high impedance, low duty cycle receiver. The result thus obtained should couple extremely low power consumption with large output voltages. The experiment was tried but it was found that, for reasons which remain unclear, the high impedance receiver proved resistant to duty cycling: it was found that the circuit produced the correct output but was extremely sensitive to the bias voltage on the gate of the SRO – too sensitive for reliable operation.

Chapter 5

Monolithic Microwave Integrated Circuits

5.1 Introduction

So far, the circuits described are realised in hybrid form – i.e. using discrete transistors, inductors and capacitors – and as such are very large compared with the requirements of specks (i.e. less than 5 x 5 mm). Circuits can be made smaller if the transistors, lumped components and transmission lines are realised in Integrated Circuit (I.C.) form or, in the case of microwave frequency circuits, as Monolithic Microwave I.C.s or MMICs. The reduction in size is partly due to the high permittivity substrate of 12.9 for GaAs (smaller wavelength) and the lack of interconnects, soldering pads etc which are necessary when a hybrid circuit is fabricated. The physical size of the lumped components, especially the capacitors (due to thinness of the dielectric between the plates – yielding higher capacitance per unit area), also contributes to the smaller size. The absence of solder joints also greatly increases the reliability of the circuit. The disadvantage of MMICs, are the greater care required when designing the circuits and the lack of any tuning facility.

The methodology used in the design of MMICs is as follows:

- The transistors are measured on-wafer in a Co-Planar Waveguide (CPW) configuration
- Electro-Magnetic (EM) simulations are performed on the CPW waveguide structure connecting the transistor to the on-wafer probes and are compared with measurements
- The transistors are de-embedded using the ElectroMagnetic simulation data for the CPW interconnects
- EM simulations are performed on a number of capacitors, inductors and resistors

- The EM data for the lumped components are compared with measured results
- A library of S-Parameter files for the lumped components is created
- An EM-based library of T-Junctions and cross junctions is created
- Oscillators, Super Regenerative Detectors (SRD), amplifiers and switches are designed using S-Parameter files for the transistor, lumped components, interconnects and junctions.

This methodology ensures that the performance of the final circuits and transceiver are predicted with accuracy. The models for the passives were obtained using Agilent's Momentum planar EM solver. Use of EM data negates the need to measure and extract models for a large number of passive structures. If several passive components are shown to agree with simulation, the performance of any passive geometry of similar size can be predicted with confidence. The MMIC process technology will now be described and will be followed by a discussion of the design of lumped components, sub circuits, transceiver, antenna and finally the complete integrated antenna/transceiver.

5.2 MMIC Process

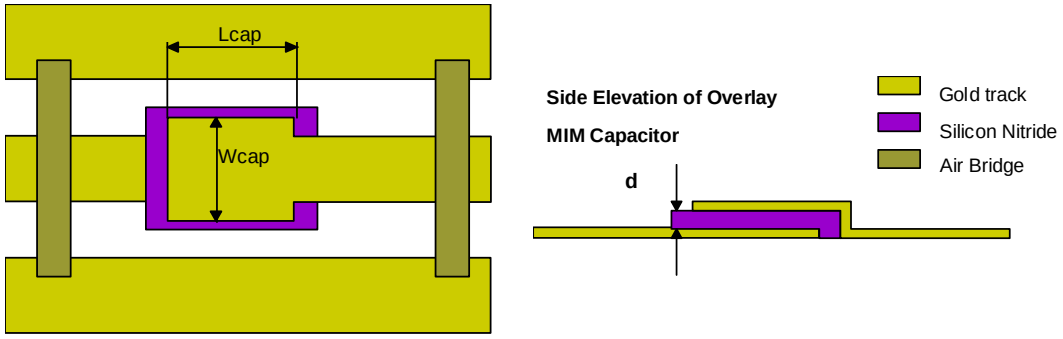
The MMIC process at Glasgow University is an advanced III-V process based on 3 inch GaAs substrates. The standard devices are depletion mode, 2 x 50 μm gate width, 50 nm gate length, mHEMTs with a composite InP/GaAs channel. The breakdown voltage is approximately 1.3 V and Idss is in the region of 70 mA. The circuit interconnects are realised in CPW form. Compared to microstrip, CPW offers reduced fabrication complexity as no vias or backside processing are required. CPW is also superior to microstrip in terms of microwave performance as CPW transmission lines are less dispersive: in microstrip, thin substrates are required in order to eliminate higher order substrate modes whereas in CPW relatively thick substrates can be used without the introduction of higher order modes as long as airbridges are used to suppress the higher order slot-line mode. Ft for the devices is approximately 270 GHz. The MMICs fabricated as part of this work were fabricated by Harold Chong, Susan Ferguson, Helen McLelland and others and not by the author.

A MMIC wafer involves many process steps - a brief description of which is given below:

- A first gold metal layer, 1.2 μm thick, is deposited on the substrate and is used for text, the bottom plate of the MIM capacitors and for finely detailed structures
- A 150 nm thick SiN layer is deposited using a dry etch technique. This is used for MIM capacitors and for passivation.
- Next, ohmic contacts are fabricated
- A MESA isolation layer, 60 nm thick, for the active devices is deposited
- The recessed T-gates of the transistors are then fabricated with a thickness of approximately 70 nm
- Next, a 150nm thick, 50 Ohm/square, NiCr layer is deposited. This is used for resistors and is realized using an e-beam evaporation and the lift-off technique
- The penultimate stage is to deposit the 1.2 μm thick gold layer used for the CPW transmission lines
- Finally the airbridges are added to tie the two ground planes together and so eliminate any higher order modes which may otherwise propagate

5.3 MMIC Capacitors

Fig. 5.1 shows the top and side view of a series connected Metal Insulator Metal (MIM) capacitor used in MMIC design.



top view side view

Figure 5.1 – Layout of series MIM capacitor

Fig. 5.2 shows a shunt connected MIM capacitor.

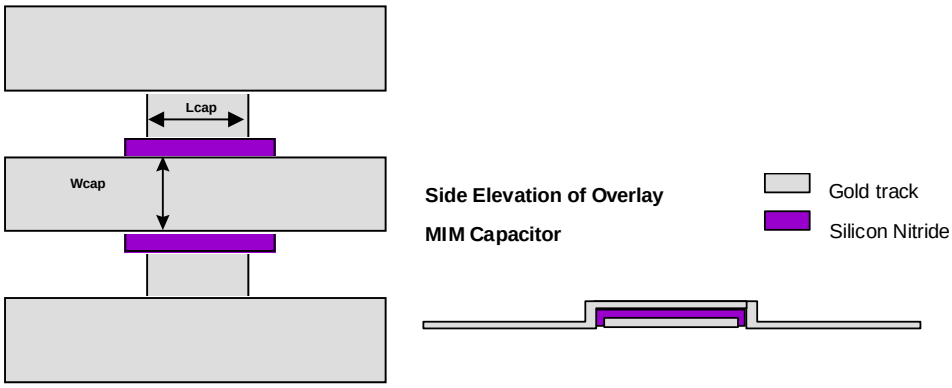


Figure 5.2 – Layout of shunt MIM capacitor

In the series connection there is dielectric filled gap between the gold signal tracks whereas in the shunt connected track there is a direct connection between input and output port and there is gold track beneath the signal line and dielectric which is connected to ground.

The dielectric thickness is 150 nm and has a permittivity of approximately 6.7 yielding a typical capacitance of 0.4 fF per μm^2. A number of capacitor structures with varying length and width were simulated and then fabricated and measured. Fig.s 5.3 and 5.4 shows the measured and simulated reflection parameters for a two port shunt capacitor which is 60 μm in length and 20 μm in width. ADS/Momentum was used to simulate the structure and the measurement was performed on-wafer using Cascade probes and an Anritsu network analyser. Similarly good agreement is obtained for other capacitors both series and shunt.

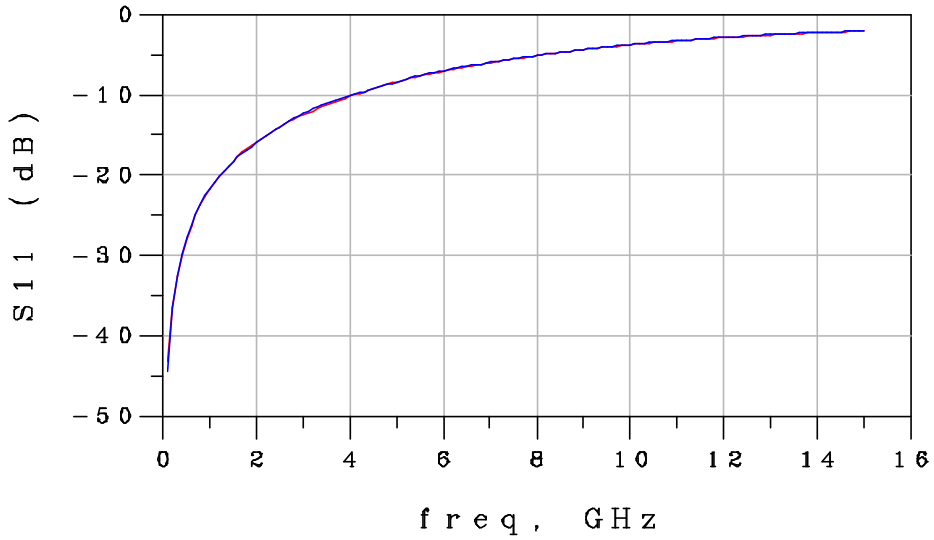


Figure 5.3 – Measured (red) and simulated (blue) S_{11} magnitude for 20x60 μm shunt capacitor

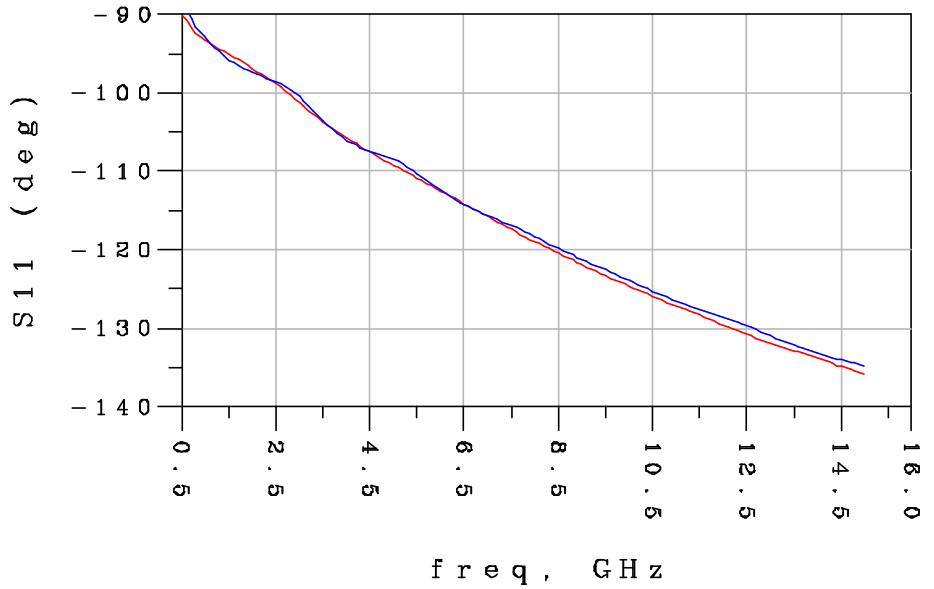


Figure 5.4 – Measured (red) and simulated (blue) S_{11} phase for 20x60 μm shunt capacitor

As a rough approximation the capacitance of a MIM structure is given by eq. 5.1

$$Cideal = \varepsilon_0 \varepsilon_r \frac{w \cdot l}{h} \tag{5.1}$$

where ε_0 is the permittivity of free space, ε_r is the dielectric permittivity, w is the plate width, l is the plate length and h is the height of the dielectric or the distance between the plates. To this, a term for the fringing capacitance must be added. By comparing the

measured and ideal capacitance a term for the fringing capacitance per μm of edge can be derived. The empirically derived formula for the corrected capacitance including fringing term is given by eq. 5.2

$$Ccorr = \varepsilon_0 \varepsilon_r \frac{w \cdot l}{h} + 7.8 \cdot 10^{-5} w \cdot l \qquad (5.2)$$

Some indicative results for capacitance against frequency for different areas are shown in fig. 5.5

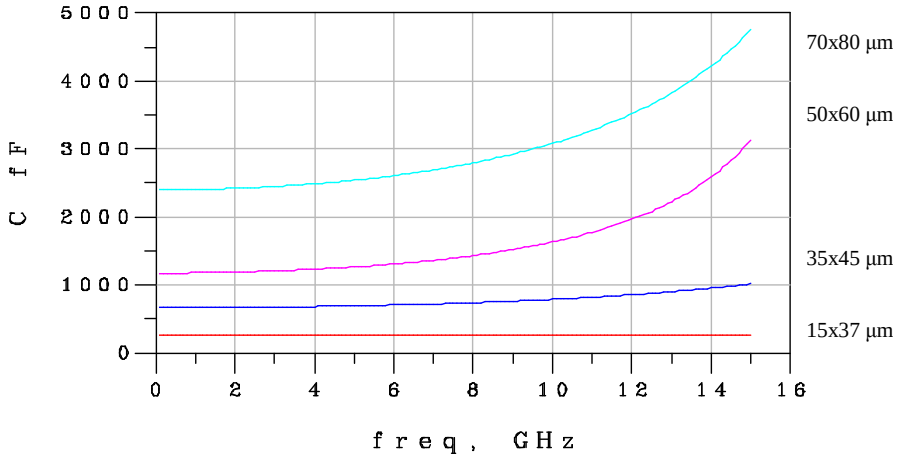


Figure 5.5 – Illustrative capacitance vs. frequency curves for different areas

5.4 MMIC Inductors

The layout of a general Co-Planar Waveguide (CPW) MMIC inductor is shown in fig. 5.6. The airbridges connecting the two grounds eliminate modes other than the quasi-TEM mode from propagating and the long airbridge ensures a series connection between the input, central inductive track and the output. The number of turns in this particular case is four. The width of the central track is 10 μm and the spacing of the track is also 10 μm. The Overall Dimension (OD) is the length and width of the inductor.

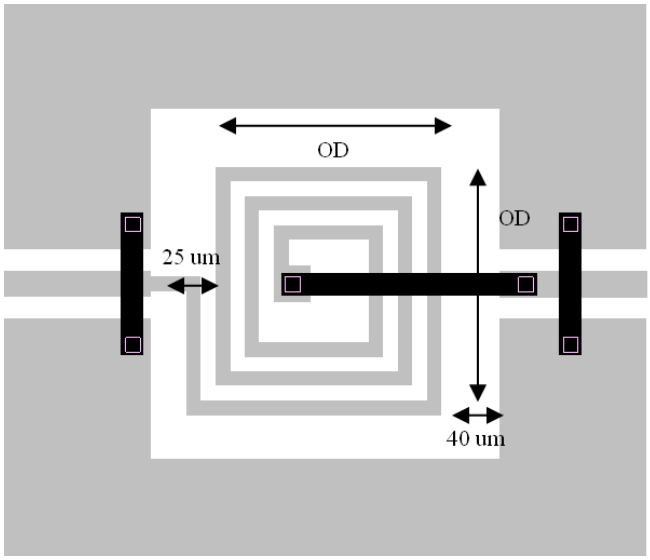


Figure 5.6 – General Layout for MMIC inductor

A number of test inductors were fabricated, measured and compared with simulation results. Figs. 5.7 and 5.8 show a comparison of the simulated and measured S_{21} parameters. Similar agreement is obtained for larger and smaller inductors.

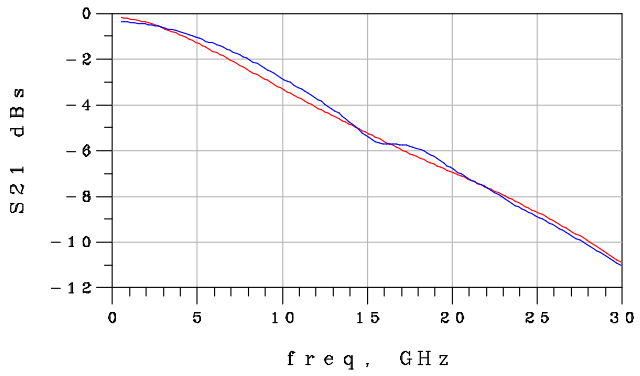


Figure 5.7 – Comparison between measured and modelled S_{21} magnitude for inductor

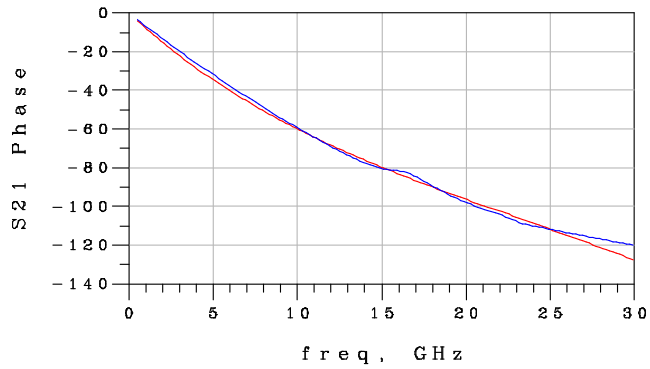


Figure 5.8 – Comparison between measured and modelled S_{21} phase for inductor

Fig. 5.9 shows some illustrative inductances for different geometries.

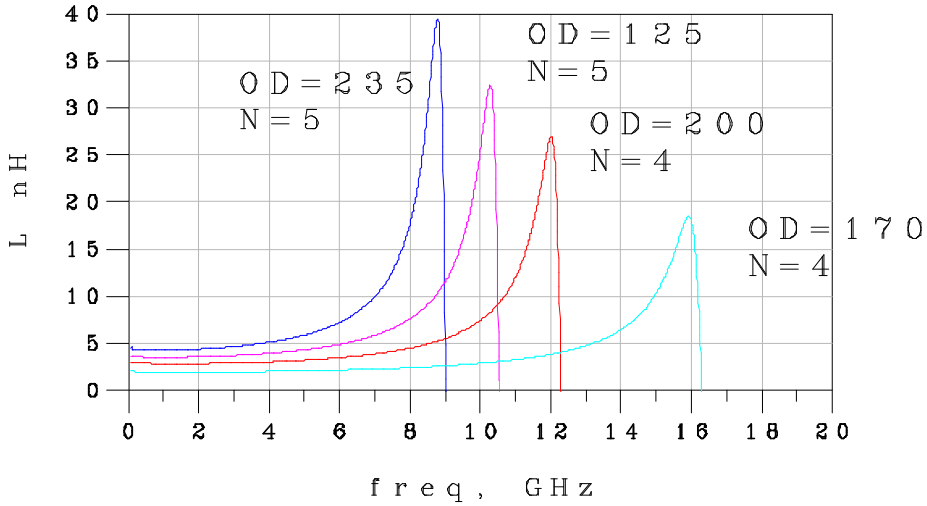


Figure 5.9 – Illustrative inductances for various geometries

5.5 MMIC Two Way Switch

Fig. 5.10 shows the layout of a switch designed as in section 3.6 (see fig. 3.19). The two sources are connected to each other and the output/input transmission line whilst the two drains are connected to either the receive amplifier or the transmit oscillator. The two control voltages are connected via isolation resistors to the two gates. This arrangement is equivalent to the schematic shown in fig. 3.19.

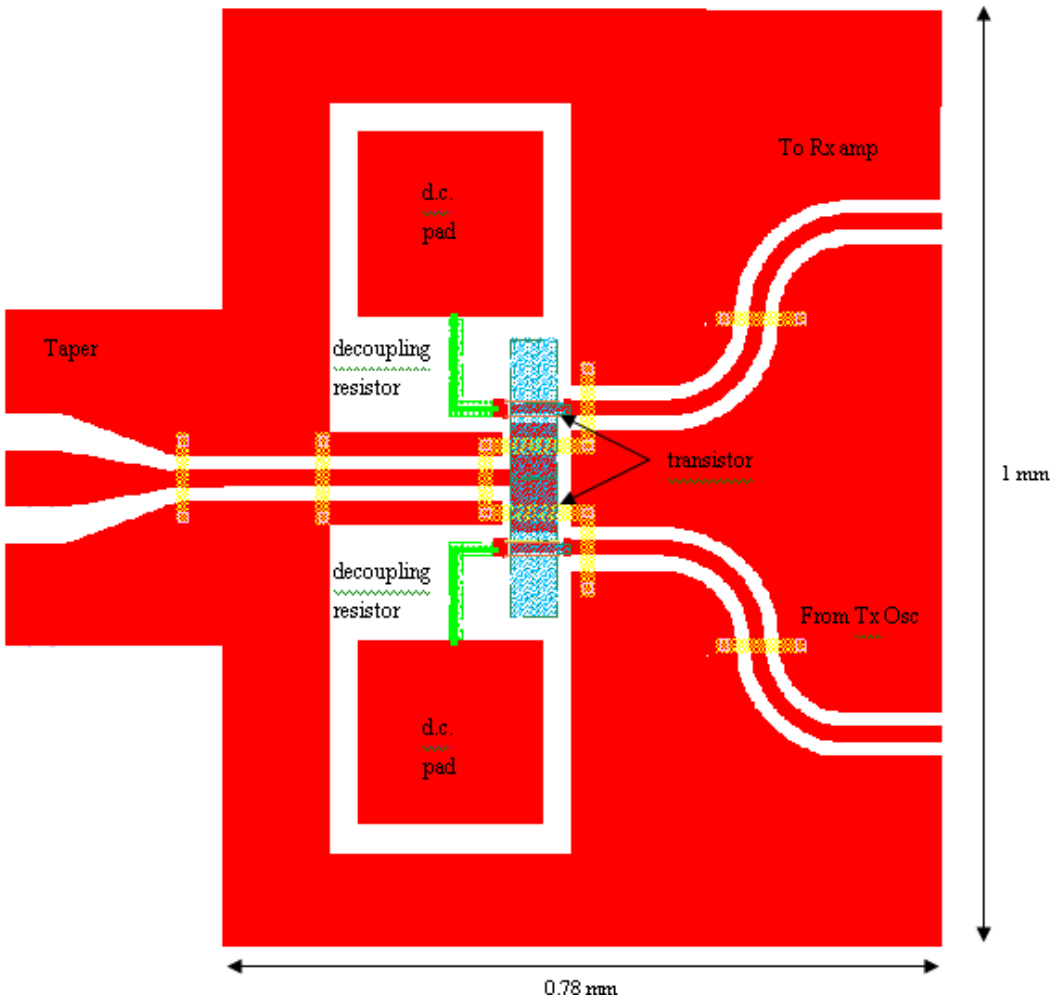


Figure 5.10 – Layout of two way switch

The taper at the input allows on-wafer probing and the two rectangular pads allow d.c. probing. The d.c. supply is decoupled from the circuit by two 1 KΩ resistors. Two of the sources are grounded whilst two are left floating (future designs will strap the sources together using airbridges). Two CPW curves at the right hand side allow for connection to the receive amplifier and transmit oscillator. The transistors used are 50 nm mHEMTs and have a pinch off voltage of approximately -1.45 V. Idss on this particular wafer is in excess of 100 mA and could not be measured directly because the Semiconductor Parameter Analyser used has an output limit of 100 mA. For more details on the transistor see Appendix B.

The circuit was fabricated and tested. Fig. 5.11 shows the simulated (red) and measured (blue) insertion loss between the taper and one of the ports when the switch is ON (gate voltage of 0 V). It can be seen that the insertion loss is approximately 1 dB at 6 GHz. This figure is acceptable but may be improved by optimising the layout and by

strapping the transistor sources together. Fig. 5.12 shows the modelled (red) and measured (blue) input match to the switch in the ON state. It can be seen that the match is good (< 10 dB) up to 10 GHz. Fig. 13 shows the insertion loss when the switch is in the OFF (gate voltage of -1.45 V) state. Isolation of 23 dB is achieved around 6 GHz. Finally, Fig. 5.14 shows the match of the switch in the OFF state. The switch is effectively an open circuit in this state.

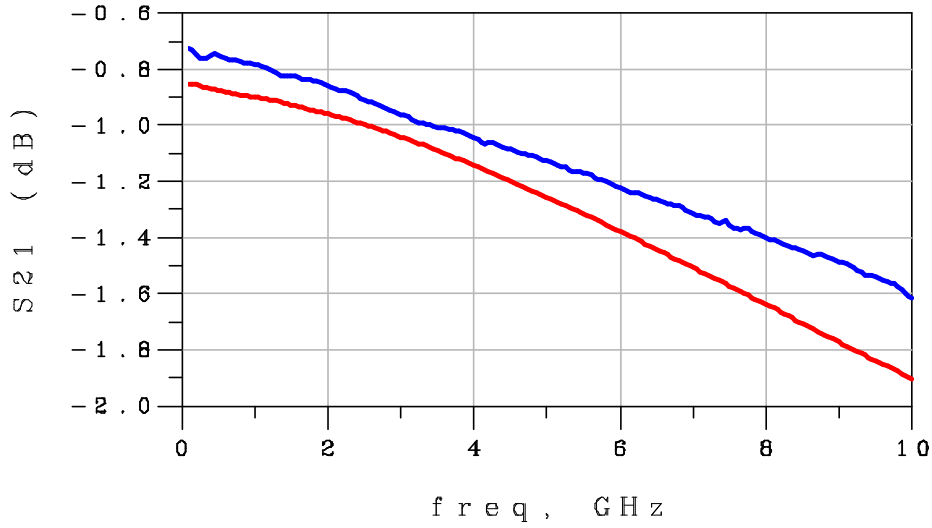


Figure 5.11 – Measured (blue) and modelled (red) insertion loss of the switch

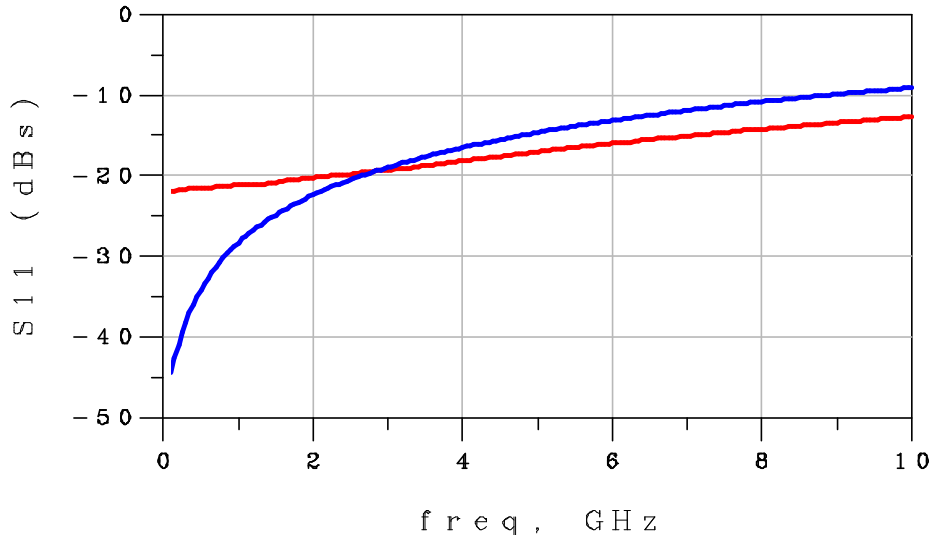


Figure 5.12 – Measured (blue) and modelled (red) input match of the switch in ON (Vgs=0 V) state

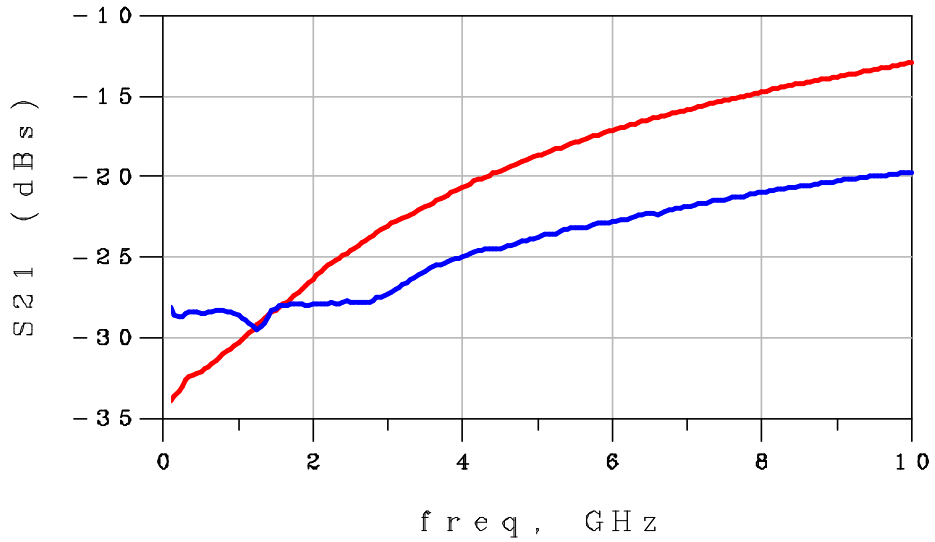


Figure 5.13 – Measured (blue) and modelled (red) insertion loss of the switch in OFF (Vgs=-1.45 V) state

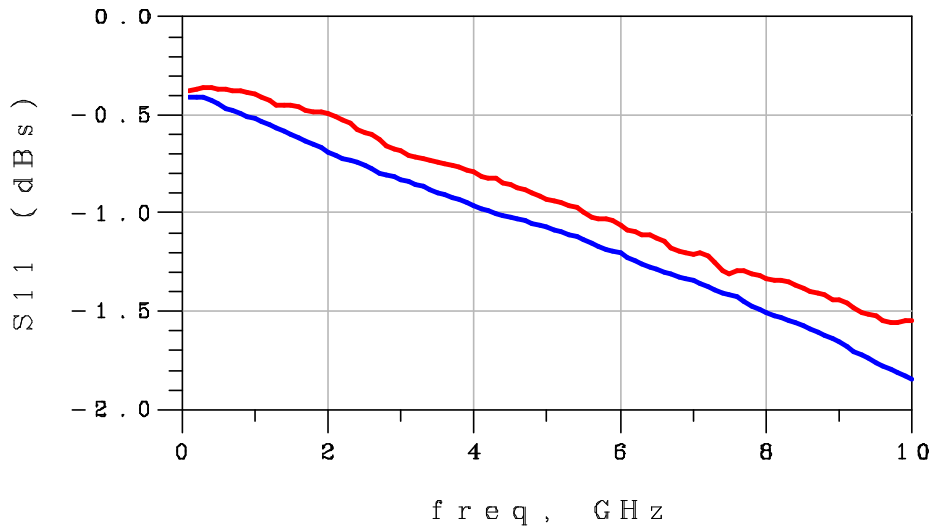


Figure 5.14 – Measured (blue) and modelled (red) input match of the switch in OFF state

The discrepancy between modelled and measured parameters is attributable to the imprecise EM modelling of the passive structure connecting the transistors to the external circuitry. The transistor was modelled by S-Parameter files.

5.6 MMIC Amplifier

The receiver amplifier must be low noise (<2dB), have good input match (<12 dB) and high isolation (>20 dB) whilst the amount of forward gain is not as important but must be greater than 0 dB. The amplifier must be low noise in order to ensure good receiver sensitivity. It must also have good matching to 50 Ω to ensure maximum power is transferred from the antenna. The isolation must be high in order that excessive amounts of re-radiation are avoided. Finally, the amplifier must provide some gain to the received signal in order to boost the signal fed to the SRO and also to reduce the noise of the second stage SRO (see eq.3.3). A trade off exists between gain and power consumption. Fig. 5.15 shows the layout of a designed MMIC amplifier. The transistor is resistively loaded at the drain side and is then conjugately matched. The gate bias is fed through a 1 KΩ resistor, shunt decoupling capacitor (1 pF) and a large inductance (15 nH). The drain bias is fed through a low valued resistor (20 Ω), shunt decoupling capacitor (1 pF) and a large inductance (15 nH). A d.c. blocking capacitor (2 pF) is placed at the input and output port. A 50 Ω resistor is placed at the drain to ensure unconditional stability. The use of resistors in the drain circuit mean that the final circuit will have to be biased at a slightly higher drain voltage than the measured S-Parameters on which the circuit is based. This is due to the voltage drop across the resistors. The matching networks are realised using shunt capacitors and series inductors. The total chip size is 1.4 x 2 mm and the power consumption is 0.45 mW. The transistor is

biased at 0.3 Vds and draws a current of 1.5 mA.

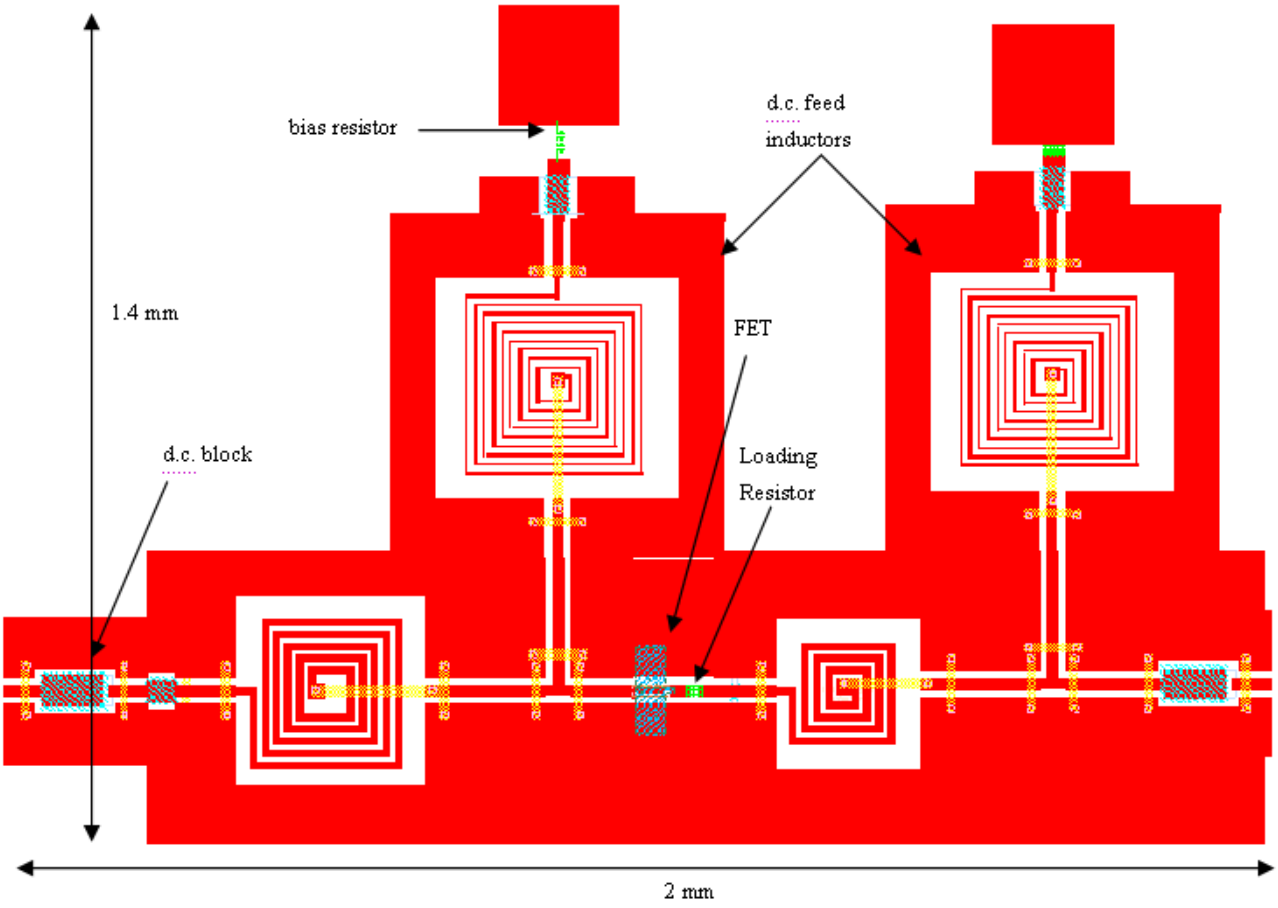


Figure 5.15 – Layout of MMIC amplifier

Fig. 5.16 shows the simulated input and output reflection coefficient magnitude in dBs. The return loss at both ports is better than 14 dB at 5.6 GHz.

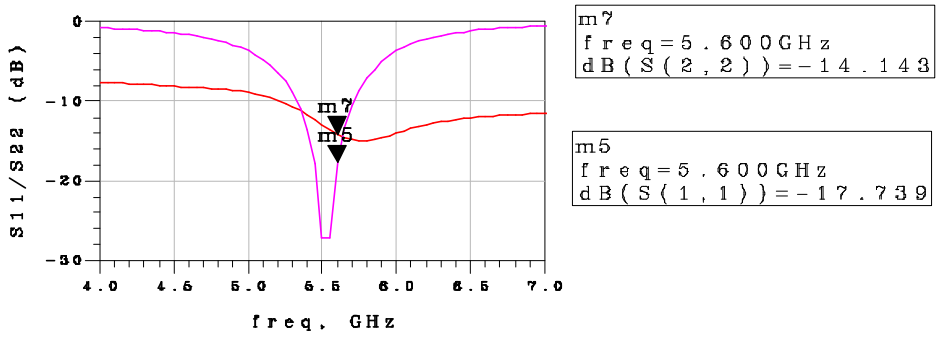


Figure 5.16 – Simulated input and output reflection coefficient gain for MMIC amplifier

Figure 5.17 – Simulated power gain for MMIC amp

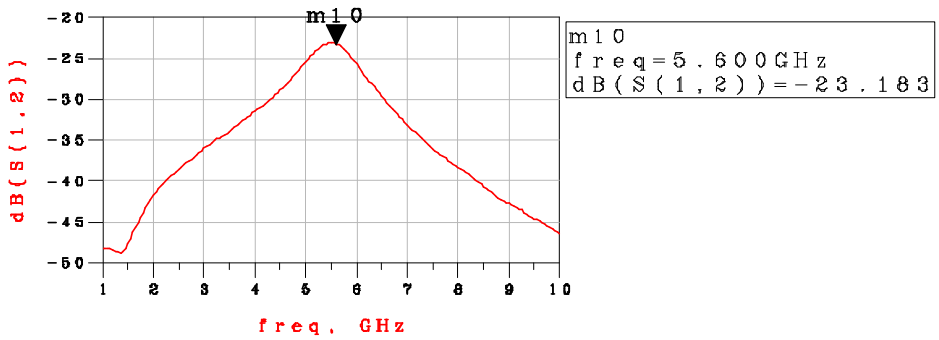


Figure 5.18 – Simulated reverse transmission for MMIC amp

Fig. 5.17 shows that the power gain of the amplifier is 7 dB at the centre frequency. Fig. 5.18 shows that the isolation is better than 23 dB. These figures indicate a useful amount of gain coupled with acceptable isolation.

5.7 MMIC Oscillators/Super-Regenerative Detectors

Fig. 5.19 shows the layout of a MMIC oscillator. The biasing arrangement is similar to that of the amplifier previously described. A feedback capacitor connected between drain and gate increases the portion of the smith chart representing unstable impedances. This makes it easier to match for negative resistance using low Q components. A negative resistance at the drain port is created by suitably matching the gate circuit so that the reflection coefficient lies in the unstable region of the smith chart. The negative resistance is then increased in value by the output matching network. As a final check the Return Ratio is calculated to ensure oscillations. The

overall dimensions of the circuit are 1x2.2 mm. The power consumption is 0.6 mW. The transistor is biased at 0.3 Vds and 2 mA.

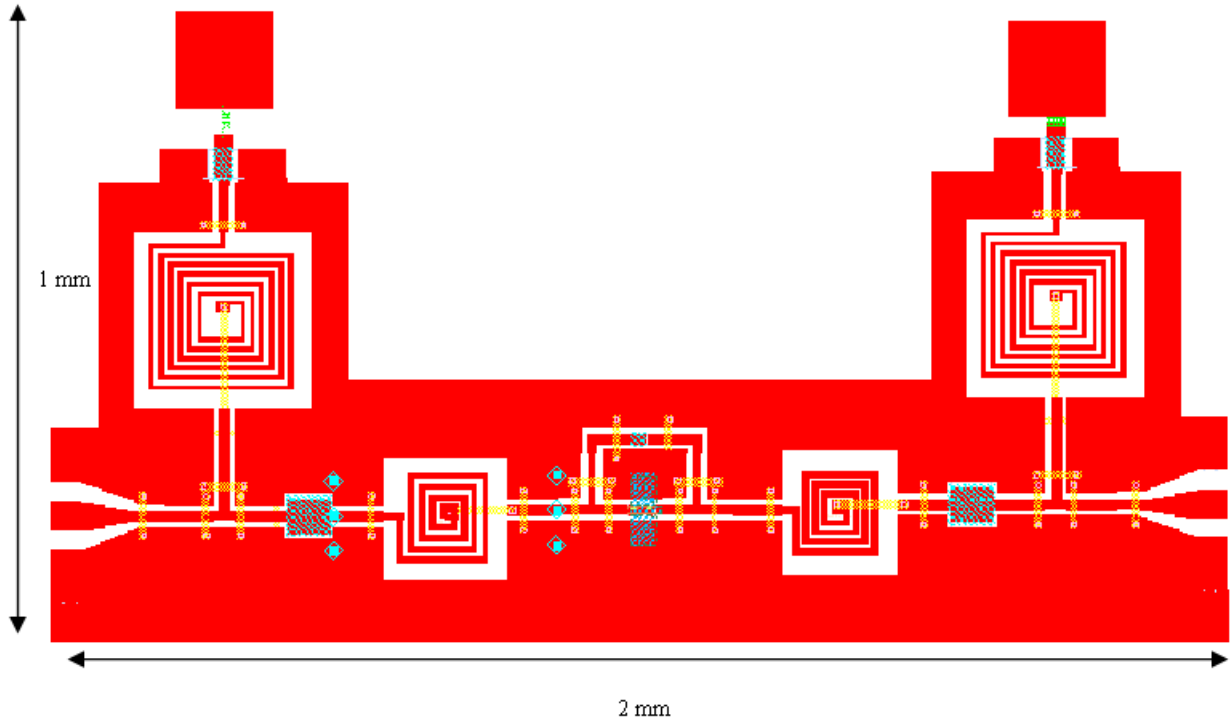


Figure 5.19 – Layout of MMIC oscillator

Fig. 5.20 shows the simulated Return Ratio (RR). It can be seen that the RR encircles the point -1+j0 in a clockwise fashion and that it crosses the 180 deg point at 5.6 GHz indicating oscillations at this frequency.

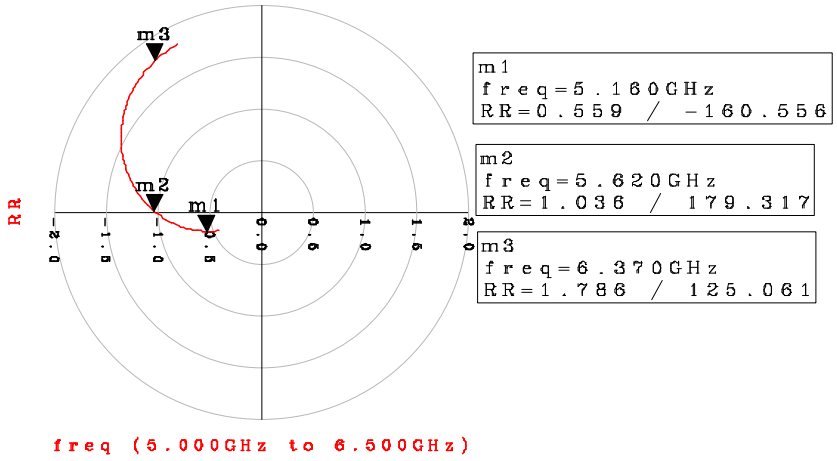


Figure 5.20 – Simulated MMIC oscillator Return Ratio

In Chapter 4 it was stated that the addition of a detector at the output of the Super-Regenerative Oscillator (SRO) improved the receiver performance. However, a transistor based common drain detector was designed and measured and despite the good input match failed to generate useful output voltages. The reason for this remains unclear. For this reason it was decided to use the SRO as a Super-Regenerative Detector by placing a resistance in the drain bias circuit and using the voltage developed across the resistor to recover the demodulated signal.

The same oscillator just described can be configured to act as a Super-Regenerative Detector by inserting a load resistor in the drain bias circuit, a d.c. block and load at the drain side port and by adding a taper for probing the signal developed across the drain load resistor. The layout for this circuit is shown in fig. 5.21.

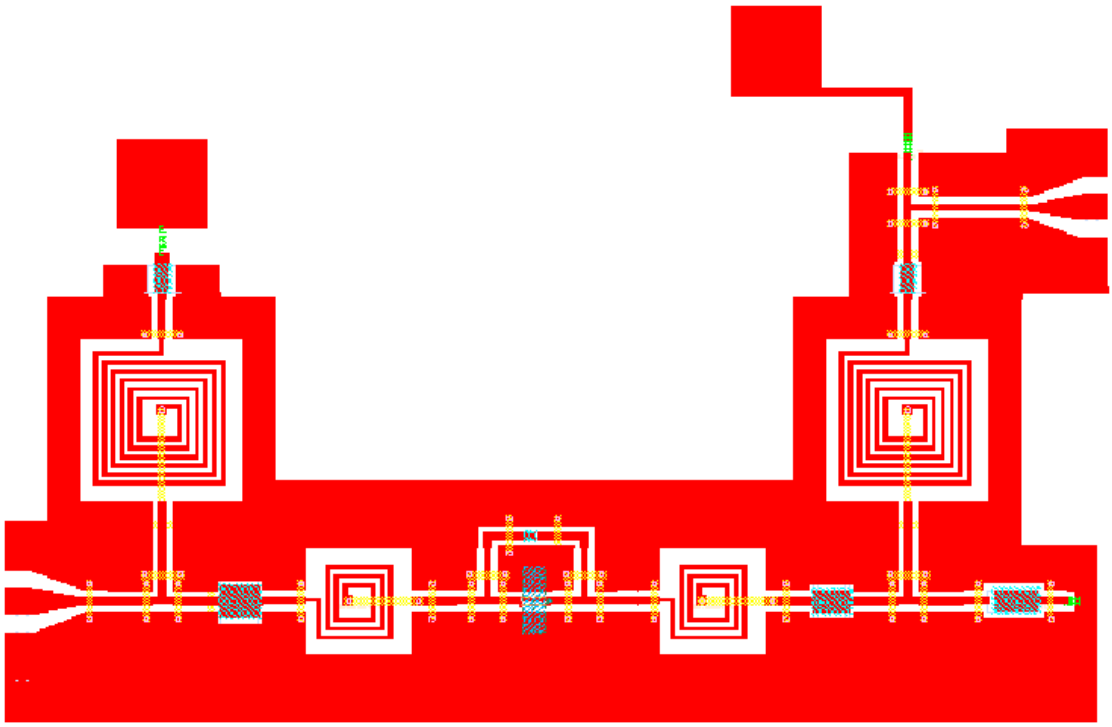


Figure 5.21 – Oscillator in fig. 5.20 adapted to become a Super- Regenerative Detector

5.8 Complete Transceiver MMIC

Now that all of the necessary sub circuits have been designed they can be put together to form a complete transceiver. The layout is shown in fig. 5.21. The total chip

size is 2.5x4.9 mm. The power consumption is approximately 1 mW receive and 0.6 mW transmit. The area and power consumption are both within specifications.

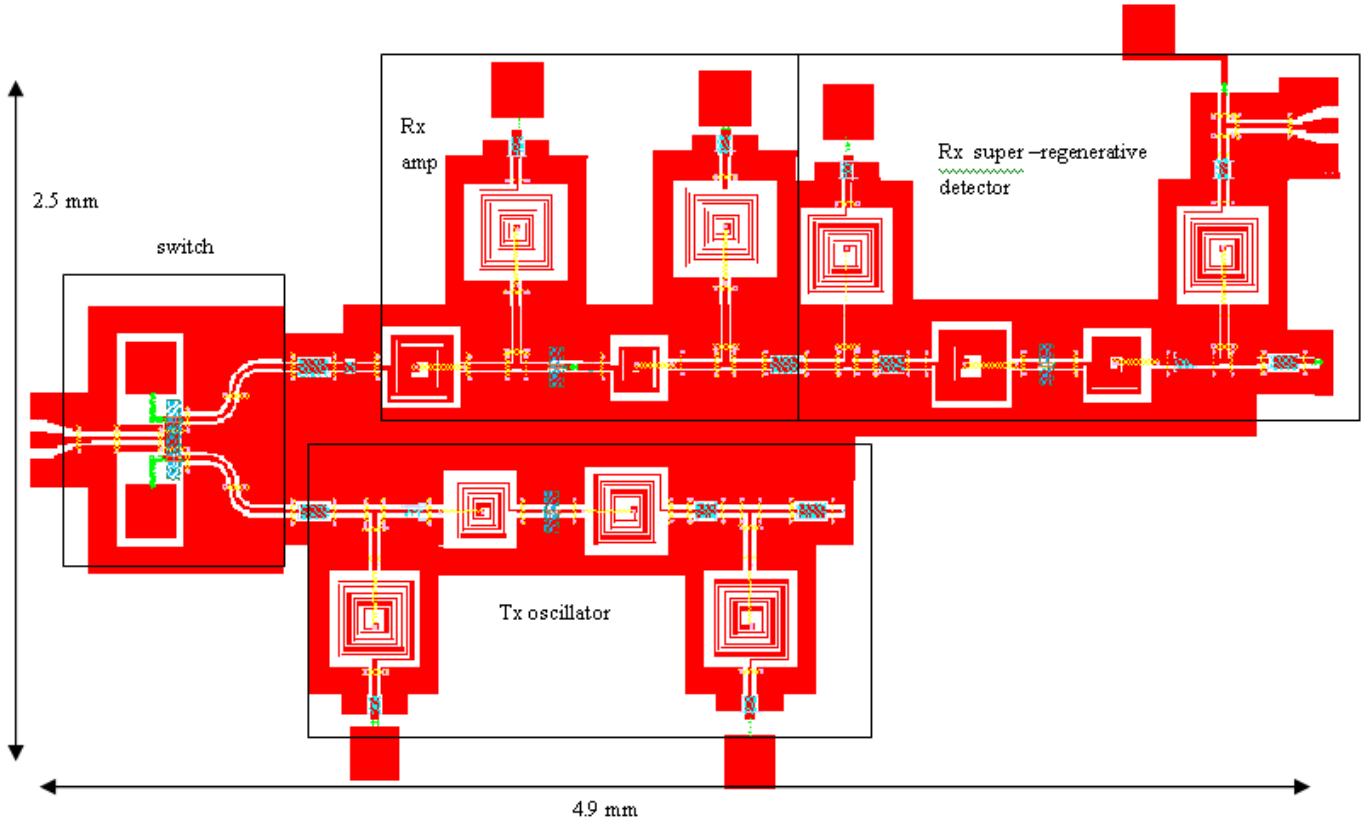


Figure 5.22 – Layout of complete MMIC transceiver

5.9 Antenna

A wire loop antenna was designed for 5.6 GHz. The antenna was designed by first starting with a half wave length wire loop and then the loop track width was adjusted to maximise gain. Next, the loop was meandered to reduce its size and finally the geometry of the feed was optimised to achieve a good input match. The ADS/Momentum layout of the simulated antenna is shown in fig. 5.23. The transceiver was approximated by a conductive metal polygon. The total area taken up is 6.8 x 6.3 mm which is slightly larger than SpeckNet requirements (5 x 5 mm). Simulations show that a 7 GHz antenna will fit into into 5x5 mm. The track width is 0.25 mm and the gap between the CPW feed and the loop is 0.1 mm. Fig. 5.24 shows a close up of the feed. The signal track of the CPW feed line is connected to one

end of the loop whilst the other end of the loop is connected to one of the CPW grounds.

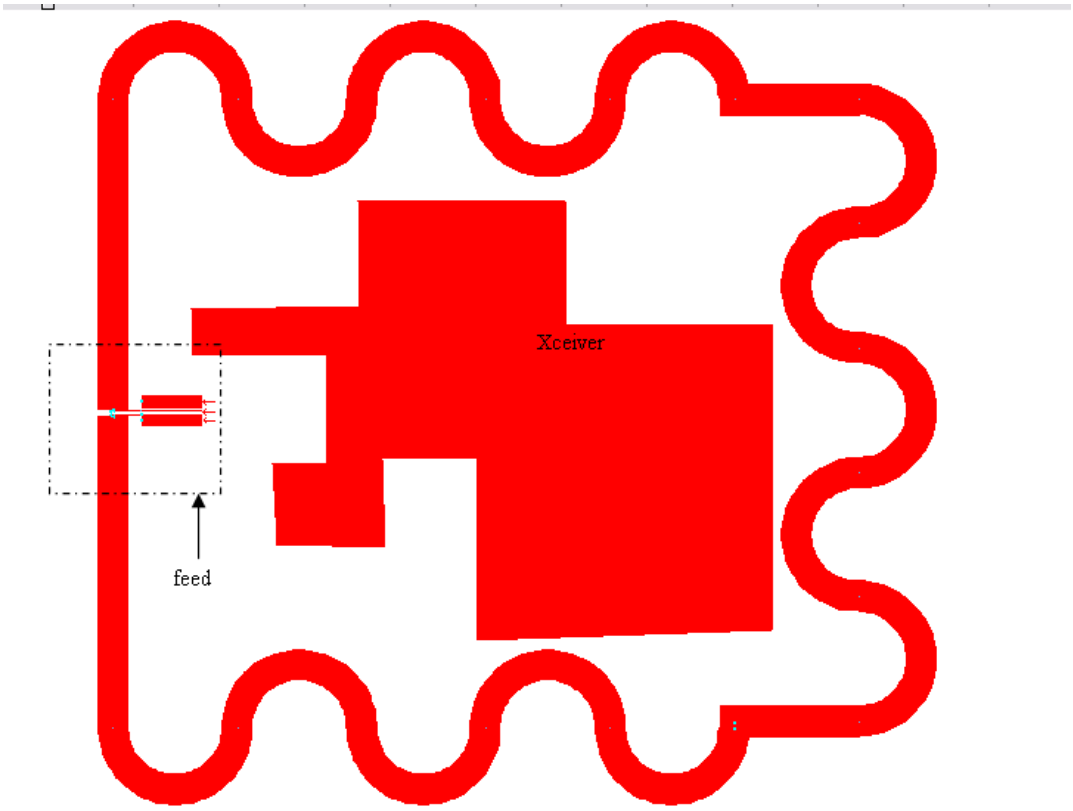


Figure 5.23 – ADS layout of the wire loop antenna with a metal polygon representing the transceiver

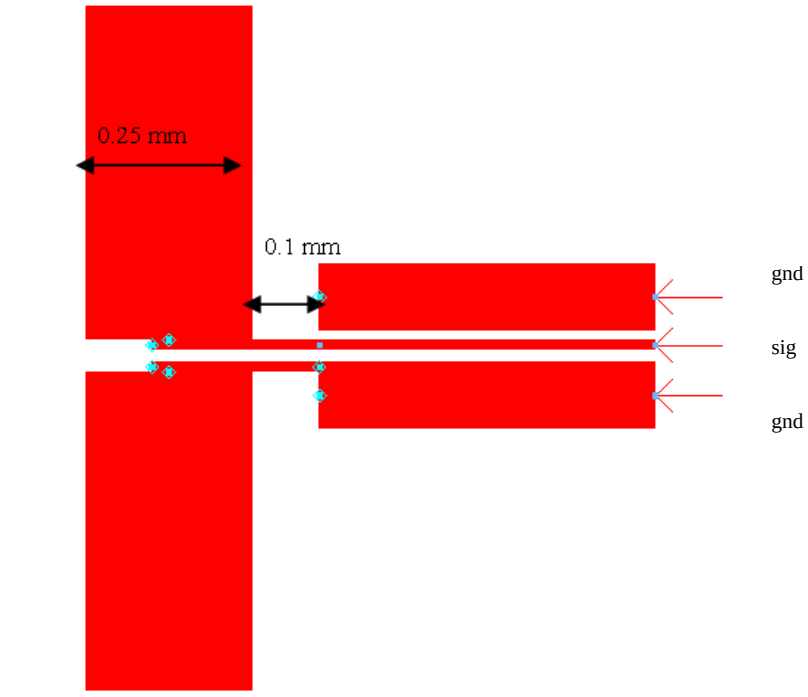


Figure 5.24 – Close up of the antenna feed

Fig. 5.25 shows the radiation pattern of the antenna. It shows a dipole – like omni-directional radiation pattern. The simulated gain is -1.06 dB. The radiation pattern and relatively high gain make it ideally suited to WSN applications with the high gain allowing for low path-loss radio links and the omni-directional response allowing for communication between specks orientated in different directions.

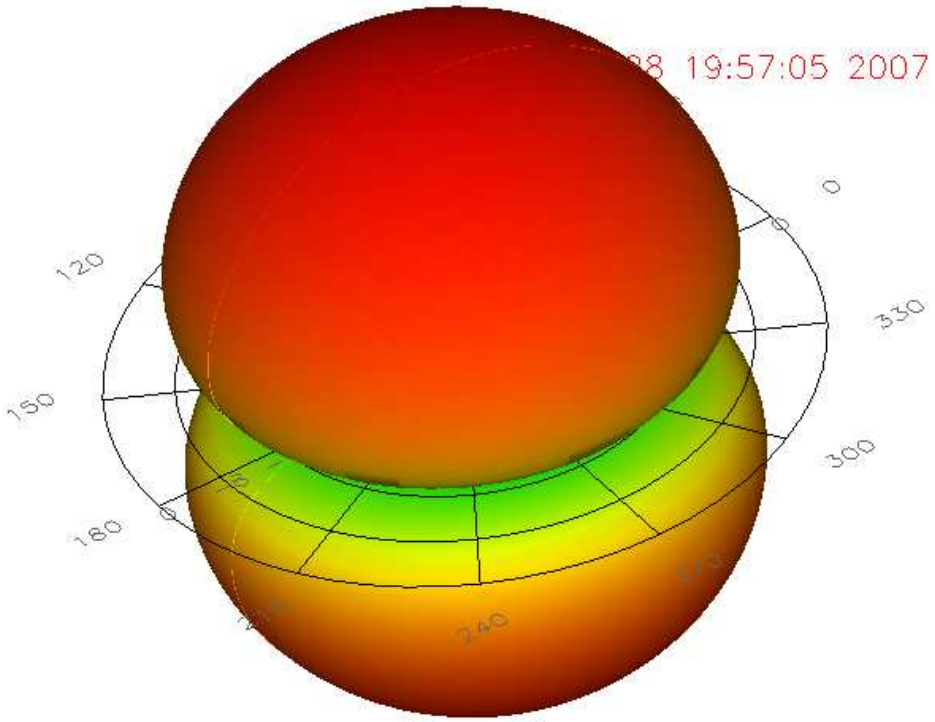


Figure 5.25 – Radiation pattern of the antenna

Fig. 5.26 shows the input reflection coefficient of the antenna. It can be seen that the return loss at 5.6 GHz is 27 dB – indicating an almost perfect match to 50 Ω. However, on the negative side, the 10 dB bandwidth is approximately 0.6 GHz. The large bandwidth will increase the noise floor of the receiver as out of band noise will be input to the receiver. However, the bandwidth of the receiver amplifier and the band pass like response of the SRD should filter out some unwanted noise.

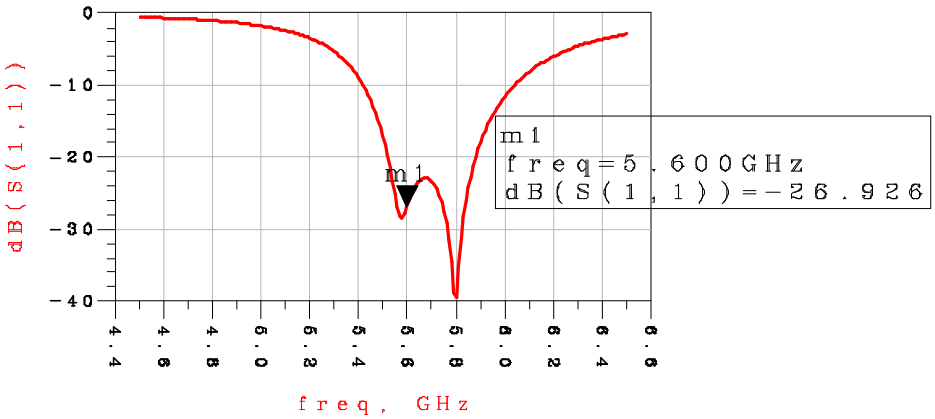


Figure 5.26 – Input reflection coefficient of the antenna

5.10 Integrated Antenna/Transceiver MMIC

Fig. 5.27 shows the layout of the final antenna integrated with the transceiver. The Super-Regenerative Detector (SRD) has been rotated by 90 ˚ to make more efficient use of the available space. The final dimensions are 6.8 x 6.3 mm. This is slightly larger than SpeckNet requirements but simulations show that a transceiver operating at 7 GHz would fit into 5 x 5 mm.

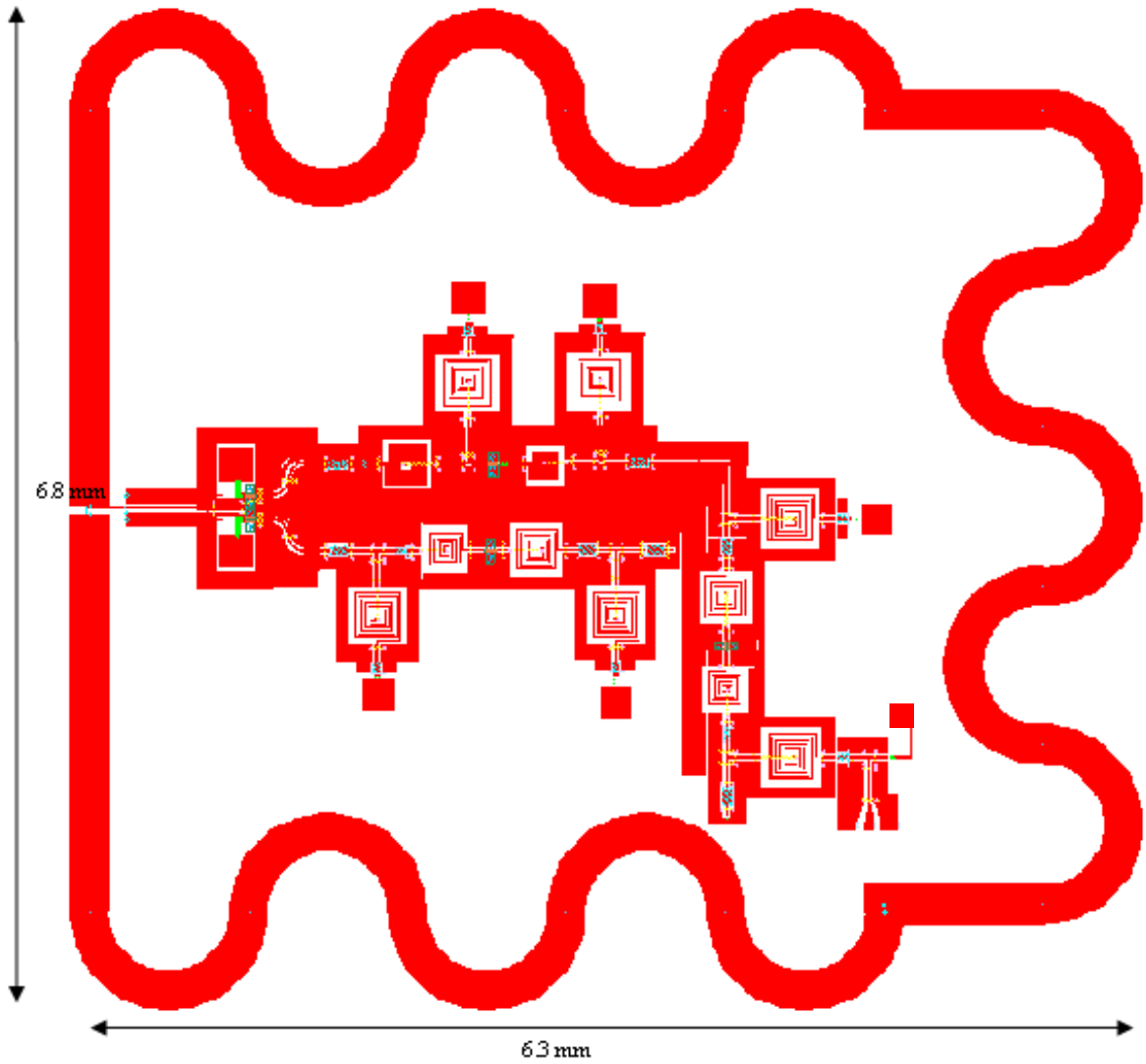


Figure 5.27 – Final integrated transceiver/antenna MMIC

5.11 Conclusions

This chapter has presented a design methodology for MMIC transceivers based on EM data for the lumped components, junctions and interconnects and S-Parameter files for the active devices. The accuracy of the EM data has been confirmed for both capacitors and inductors by a comparison between measured and modelled S-Parameters. This close agreement ensures the performance of complete circuits can be predicted with confidence. An overview of the fabrication steps used in the advanced III-V in-house technology has been given and the simulated performance of low power MMIC circuits has also been given.

The layout of MIM series and shunt capacitors and typical performance data has been presented. It has been shown that excellent agreement is obtained between measured and modelled S-Parameters for shunt capacitors. Use of MIM shunt capacitors greatly reduces the circuit real estate compared with open circuit stubs - especially at relatively low microwave frequencies. Series capacitors are essential for d.c. blocks – excellent agreement between measured and modelled parameters for series capacitors is obtained.

Lumped inductances are preferred to lengths of transmission lines at low microwave frequencies as they take up considerably less circuit real estate. Accurate models are required and excellent agreement is achieved between measured and modelled S-Parameters using EM data – see figures 5.3 and 5.4.

With close agreement between measured and modelled responses for capacitors and inductors for a number of given geometries a library of components can be created. Powerful additions to the library include EM data for interconnects and for T/Cross junctions. The data for the passive components when coupled with accurate de-embedded measured data for the transistors provides a sound basis for the design of complete circuits and, ultimately, complete transceivers.

Measured data for a two way switch is given. The insertion loss in the ON state is 1.1 dB at 6 GHz and the isolation in the OFF state is 17 dB whilst the return loss is better than 10 dB. The switch layout should be optimised to better the input match and decrease the insertion loss. The switch design is compact and measures 0.78 mm x 1 mm. The switch is effectively passive as the gate current is of the order of tens of μAs.

A design for a linear amplifier with a centre frequency of 5.8 GHz is shown in fig.5.15 the circuit exhibits 7 dB gain with 23 dB isolation and consumes 0.45 mW.

A design for an oscillator intended for use as both a transmit oscillator and a receive SRO is given. The predicted output frequency is 5.8 GHz and the predicted output power is -10 dBm. The power consumption is 0.45 mW. The circuit was designed using Return Ratios.

As discussed earlier in the chapter, a common drain detector was designed and measured but it was found that, despite a good input match, the output voltage was very low. The reason for this is still under investigation. It was therefore decided that a resistor would be placed in the drain bias circuit of the SRO to convert the circuit into a Super-Regenerative Detector.

A design for a compact wire loop antenna operating at 5.8 GHz is given in section 5.9. The antenna exhibits an omni-directional response with satisfactory gain of -1 dB. The antenna is therefore suited to use in WSNs as its radiation pattern allows for misaligned specs to communicate with each other and its high gain reduces the path loss and hence increases the distance over which specks can communicate.

Finally the layout for an integrated transceiver/antenna is given in fig. 5.27. The overall chip size at 6.8 mm x 6.3 mm is slightly large compared with the specification of 5 x 5 mm. The operating frequency of 5.8 GHz is in an unlicensed ISM band but if it were possible to move to the slightly higher frequency of 7 GHz simulations show that the complete transceiver would fit into 5 x 5mm.

Chapter 6

Conclusions

6.1 Discussion of Results

The focus of this thesis has been to design radio transceivers which exhibit ultra low power consumption, small size and are suitable for use in WSNs. The radio must exhibit small size as the overall ‘speck’ size must be small. The battery capacity is therefore severely limited. Another, conflicting, requirement is that the radio must be able to operate over a distance of at least a metre. This implies radios with high sensitivity but again this requirement is in conflict with the demand that the radio exhibit low power consumption. However, the radio is only required to handle relatively low data rates. This latter fact facilitates the design of a radio solution which satisfies the specifications: this thesis has demonstrated that for ultra low power consumption, low data rate (<200 kBit/s) applications the super-regenerative receiver coupled with a directly modulated transmit oscillator provides satisfactory performance with respect to output voltage and operating range. Measured results on hybrid prototypes described in this thesis confirm this assertion.

Chapter 2 discussed the unsuitability of ‘conventional’ homodyne transceivers to the design problem. This is mainly due to the relatively high LO powers required to ‘pump’ the mixers and the power hungry PLL. Chapter 2 also discussed the choice of operating frequency in terms of physical size, power consumption and operating range: the circuitry requires low frequencies as the gain of amplifiers and the output power of oscillators can be higher at low frequencies. Also, the insertion loss of switches and the path loss of LOS links are lower at low frequencies. On the other hand, in terms of physical size the operating frequency must be as high as possible as this allows the antenna, lumped components and transmission lines to be made extremely small. There thus exists a trade off between physical size, operating range and power consumption. For this particular application the optimum operating frequency is judged to be between 5 and 10 GHz for a physical circuit size of around 5 mm x 5 mm.

Chapter 3 described the function of each RF sub-circuit or building block. Design procedures for all the circuits required for super-regenerative transceivers:

amplifiers, oscillators, detectors and switches were presented. The amplifier uses resistive loading at the drain side and conjugate matching to achieve as close a match to 50 Ω as possible. A novel oscillator design method (section 3.4) which allows the designer to optimise the circuit for either spectral purity, start up time or a.c./d.c. efficiency was also detailed. The efficiency can be made twice as high as the efficiency obtained with the standard design technique. Also, the designer may want to decrease the start up time of their circuit when, for example, they are designing quenched transmit oscillators for carrier-UWB applications. Section 3.5 discussed the design procedure for envelope detectors. It was shown that there exists a trade off between output voltage and the highest possible data rate. However, for low data rate applications an output RC network with a high time constant (and load resistance) can be used - therefore maximising output voltage. Section 3.6 described how two FETs can be connected together to form a SPDT switch. The switch is important because it allows the antenna to be shared between the receiver and transmitter. Switch insertion losses of around 1 to 1.5 dB at low microwave frequencies can be achieved.

The standard transceiver operating at 2.48 GHz described in section 4.3 achieves an output voltage of 2mV for an input power of -55 dBm. Extrapolating to lower powers and assuming that the baseband amplifier can amplify a signal as small as 1mV then with an -11 dBm Tx output power the transceiver can work over a distance of 4 m assuming antennas with 0 dB gain. The power consumption of the receiver is 0.38 mW and the transmitter consumes 0.4 mW. These important results indicate that a transceiver can be designed using GaAs FETs, operating at low microwave frequencies and built from standard circuits that operates over a metre and yet consumes less than a milliwatt.

Sections 4.4 and 4.5 described how the transmitter and receiver circuits can be duty cycled to reduce power consumption by as much as 97.5%. The principle underlying the duty cycling technique is simple: rather than sending a burst of carrier for the same length of time as the data is at a high logical level, instead send a much shorter pulse to signal a ‘1’. If the transmitter is only ON when there is a short burst of carrier then the power consumed will be less than if a ‘long’ burst of carrier is sent. The same principle can be applied to the receiver: it only turned ON when a 0 or a 1 is ‘expected’. The technique of duty cycling the transmitter requires the addition of a capacitor and an AND gate at the transmit side and a monostable with an RC timing network at the receive side. These simple additions can reduce the d.c. power consumption of the

transmitter by as much as 97.5 % and yet the performance is the same as that of the standard transceiver – as long as the bandwidth of the transit RF pulses do not exceed the bandwidth of the receiver. As the radios considered in this thesis all operate at low data rates the bandwidth of the receiver (approximately 15 MHz) is always large enough. Duty cycling the receiver is more complex than duty cycling the transmitter but can potentially reduce the power consumption by 95 %. Duty cycling of the receiver requires a high pass filter and an Ex-OR gate as well as the additional circuitry required to duty cycle the transmitter. Moreover, a control loop is required to synchronise the receiver pulses with the input RF pulses. An important step towards this goal has been achieved: a circuit has been designed using an inverter and two monostables whose output consists of narrow pulses whose position in time can altered by a control voltage. Thus a control voltage can be varied electronically until a 'lock' is achieved. Unlike duty cycling the transmitter, duty cycling the receiver leads to a reduction of output voltage by approximately half. This is due to less samples being taken than in the normal case (>2 per bit).

It was shown in section 4.6 that by using a high normalising impedance 2.45 GHz transceivers can be designed to work over 10 m with a power consumption of 0.675 mW. The increased operating range compared with the standard transceiver described in section 4.3 is a direct consequence of the high normalising resistance: the envelope detector operates as RF voltage in/baseband voltage out detector having a gain of slightly less than 1. Therefore anything that can be done to maximise the input voltage to the detector will also increase the output voltage. This can be achieved by using a higher normalising resistance since, for the same power, as the normalising resistance increases by 2 the associated voltage increases by 1.414. The receiver works by matching the input of the amplifier to 50 Ω, the output to 1000 Ω, the input and output of the oscillator to 1000 Ω and the input of the detector to 1000 Ω. This ensures maximum power transfer between each stage.

Chapter 5 presented simulated results for a MMIC transceiver operating at 5.6 GHz. The simulated results for each sub circuit were based on measurements for the transistor and EM data which has been compared with measurements for the lumped components and junctions. Excellent agreement between the measured and modelled response for inductors and capacitors was obtained. If the transistor is characterised accurately this design methodology allows the designer to predict the final performance of the transceiver with confidence. Unfortunately, due to external circumstances associated

with the in-house foundry, the circuit could not be fabricated in time for final measurements. The predicted power consumption is 1 mW receive and 0.45 mW transmit. The overall chip size is 2.5 x 4.9 mm. Furthermore, it was shown that the transceiver can be integrated with an antenna and fit into 6.8 x 6.3 mm. The antenna exhibits -1.06 dB gain and an omni-directional radiation pattern. Simulations show that moving to an operating frequency of 7 GHz will shrink the overall chip size to less than 5 x 5 mm. These results for the MMIC coupled with performance of the transceivers detailed in Chapter 4 indicate that a transceiver operating at low microwave frequencies can be designed which works over a metre and yet consumes less than 1 mW and, moreover, fits into size comparable with the specification of 5 x 5 mm. The performance of the MMIC should be superior to that of the transceiver described in Chapter 4 as the shorter gate length of the transistors used provides greater transconductance for a given power consumption and the parasitic components are less significant than in the packaged devices used in Chapter 4. Also, the noise performance of the 50 nm devices is approximately 2 dB better than the packaged devices used in Chapter 4. In conclusion, practical measured results in Chapter 4 coupled with the rigorously obtained simulation results for MMICs described in Chapter 5 demonstrate the feasibility of sub-milliwatt, III-IV radios suitable for Wireless Sensor Networking.

Crucial to the successful prediction of the behaviour of non linear circuits such as pulse generators and oscillators is the accurate modelling of semiconductor devices such as transistors and diodes. Appendices B and C provide details of accurate non linear models of transistors and step recovery diodes respectively. Both models use look up tables in order to closely model complex behaviour without recourse to two dimensional curve fitting.

Appendix B details an accurate non linear model of a 50nm mHEMT. The model is assembled from small signal data and stored in 2D data files. The model is proved to accurately predict, d.c., small signal and gain compression characteristics of the transistor. The model can also be used to predict the output power of simple oscillator circuits. However, simulations do not converge for circuits with S-Parameter files for the cross junctions, inductors, capacitors etc. Simulations only converge for circuits containing simple lumped components and transmission lines with or without Q factor information. Future work should include increasing the robustness of the model perhaps by extending the valid bias range.

Appendix C describes an accurate table based non linear model of a Step Recovery Diode (SRD). The efficacy of the model is demonstrated in a comparison between measured and simulated output waveforms for a novel Bi-Phase Wavelet generator. The model is useful for low power designs as UWB can be considered to be OOK with an extremely low duty cycle: similar to the circuits detailed in sections 4.4 and 4.5.

6.2 Future Work

From the discussion in Chapter 2, research should be carried out to reduce the power consumption of active mixers which exhibit good conversion loss. This may include exploring new FET-based circuit topologies as well as the optimum layout of the FETs in order to reduce the LO power needed to attain good conversion loss. The new mixer circuits thus obtained may form the basis for PLLs/Costas Loops which exhibit low power consumption and high RF sensitivity. With mixers and frequency control loops suitable for low power implementation, transceivers using more sophisticated forms of modulation than OOK can be designed. This may allow for Orthogonal Frequency Division Multiplexing or Code Division Multiplexing systems to be used thus alleviating the problem of scheduling transmissions to avoid multi-user interference. Coherent demodulation will also improve the sensitivity of the receiver and the resistance to interference. Another feature which would improve the sensitivity of the receiver would be a narrowband, low loss, band pass filter. This work may involve the design of high Q MMIC spiral inductors perhaps by suspending the structure in air using airbridges.

Research should also be conducted into extending the design methodology using RRs to include transistors which are unconditionally stable. In Chapter 3 and in Chapters 4 and 5 all of the designs used transistors which are potentially unstable at low frequencies and unconditionally stable at some higher frequency and above. The new methodology may include the use of a feedback capacitance and inductance to make the transistor exhibit negative resistances at both ports over some narrow frequency range. Transmission lines can then be used to tune the final operating frequency. Investigations have already begun but it has been found that the operating frequency is very sensitive – especially to slightly differing transistor characteristics such as are found from device to device. Another improvement to be made is to increase the frequency stability of the

oscillators especially with respect to the variations in transistor performance from batch to batch or even from individual device to device. This may involve the use of some external frequency determining component such as a crystal, dielectric resonator or SAW (Surface Acoustic Wave) element. Such frequency determining elements tend to be large and are usually placed off chip and are connected with wire bonds. The switch designs presented in this thesis are very basic and can have their isolation improved by the use of more transistor stages.

Radios with higher data rates than those presented in chapter 4 should be considered. The power consumption of radios increase with higher data rates but on the other hand it takes less time to send a message of fixed size using high data rates than low data rates so the total energy consumed whilst transmitting and receiving a packet may actually be less.

The duty cycled designs presented in Chapter 4 would benefit from an all-digital logic device to reproduce the correct duty cycle of the signal at the bit slicer (comparator) output. Currently, a monostable is used which is a quasi analog-digital device and depends on an RC network to determine its time constant. A sequential logic state machine which when input a logical ‘1’ outputs a ‘1’ for a given number of clock cycles would ensure that a perfect 50 % duty cycle would be reproduced without any narrow glitches – thus negating the need for low pass filtering and a subsequent stage of bit slicing.

Another important piece of future work is the design of a complete synchronisation loop for the duty cycled receiver. As outlined in Chapter 4 a circuit has been devised which outputs a series of narrow pulses whose position in time can be shifted back and forward as a function of a control voltage. This circuit can be used as the basis of a process which uses an incoming signal incorporating a training sequence - for example, a long sequence of alternating 1s and 0s. A DAC could step the control voltage until the output of a sequence generator (10101etc) is correlated with the input signal over a given number of clock cycles. This correlation could be achieved with an Ex-OR gate. The gate would output 0 constantly if the input and output code were perfectly aligned. If this output were 0 over a given number of clock cycles a state machine could then be used to signal to the DAC to stop ramping the control voltage and hold the output at its current value. The trade off to be evaluated is the greater power consumption of the increasingly complex baseband circuitry and the decreased power consumption of the RF circuitry. Another important poinis that, for low power consumption, emphasis

should be placed on RF/baseband co-design: the baseband and RF parts can not be designed separately if optimum performance is required.

The work on the MMICs can also be much advanced. The improvements can equally be made on the devices and components as on the circuits and transceivers. For the transistors, modifications should be made to the device to increase the transconductance of the device when it is biased at low voltages and currents. This may include producing devices with decreased gate width and/or shorter gate length. Lower-loss passive components can be designed by increasing the thickness of the gold layer from 1.2 μm to, for example, 2.5 μm. The price paid is an increase in fabrication cost and time but the advantages are higher Q components and hence higher gain amplifiers and higher efficiency oscillators. In terms of circuit design, the performance of the switch can be improved by optimising the layout or increasing the number of stages. The circuit layout of the transceiver can also be optimised to reduce circuit real estate. The use of a MMIC process with the capability of high frequency performance can be used to explore the performance of a high frequency (+60 GHz) transceiver with much smaller dimensions than currently envisaged. The antenna size may be so small that arrays of electronically switch-able antennas could be used to form beam steering systems. In such a system an extremely narrow, high gain, LOS link would be formed automatically by the speck to mitigate the increased path loss incurred by the higher carrier frequency. Use of such highly focused beams of electromagnetic energy would also allow frequency reuse – thus accommodating multiple users without any frequency, code or time division multiplexing. Use of a much higher carrier frequency would also facilitate high data rate links.

Future work should also include the design and measurement of a carrier-UWB transceiver as the theoretical power consumption can be very low. This is a consequence of the fact that the circuitry only needs to be ON for hundreds of picoseconds at a time. Thus, if the data rate is relatively low, the transceivers can be made to operate with extremely low duty cycles and hence the power consumption can be made correspondingly low. Use of a carrier frequency over ‘traditional’ impulse radio implementations allows the antenna to be made small.

In conclusion, this work has demonstrated that microwave frequency radio transceivers exhibiting ultra low power consumptions can be designed (<0.1 mW) but the designed transceivers are all low data rate (<200 kBit/s) and use OOK and are therefore susceptible to interference and rely on multiple access techniques to

accommodate more than two users. The transceivers are also large (approximately 6 x 6 mm for the MMICs). Therefore, the improvements to be made and the focus of future work should be on improving the functionality of the radio, the resistance to interference, increasing the data rate and on reducing its physical size.

APPENDIX A: Mathematical Analysis of Super-Regenerative Receiver

A model of a super-regenerative receiver was described in Chapter 4, section 2. A detailed mathematical analysis is given here for completeness. When the switch is closed (see section 4.2 – fig.4.3), the voltage equation of the circuit can be written as:

$$A\sin(\omega t) = L\frac{di}{dt} - Ri + \frac{1}{C}\int i \cdot dt \tag{A.1}$$

differentiating with respect to *t* gives:

$$A\omega \cdot \cos(\omega t) = L\frac{d^2 i}{dt^2} - R\frac{di}{dt} + \frac{i}{C} \tag{A.2}$$

Solving this equation we obtain:

$$\begin{aligned} i &= K_1 e^{(a+b)t} + K_2 e^{(a-b)t} - \frac{R}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} A\sin(\omega t) - \frac{\left(\omega L - \frac{1}{\omega C}\right)}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} A\cos(\omega t) \\ &= K_1 e^{(a+b)t} + K_2 e^{(a-b)t} - \frac{A\sin(\omega t + \phi)}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}} \end{aligned} \tag{A.3}$$

where

$$a = \frac{R}{2L} \tag{A.4}$$

$$b = \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}} \tag{A.5}$$

and

$$\phi = \tan^{-1}\frac{\left(\omega L - \frac{1}{\omega C}\right)}{R} \tag{A.6}$$

and K_1 and K_2 are arbitrary constants

Assuming that at *t=0, i* is 0 and therefore from eq.1

$$A\sin(\omega t) = 0 = L\frac{di}{dt} \tag{A.7}$$

We can evaluate the constants of integration, K_1 and K_2. First we substitute eq. A.3 with *t* set equal to zero into eq. A.7 to obtain:

$$K_1 + K_2 - \frac{A\left(\omega L - \frac{1}{\omega C}\right)}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} = 0 \tag{A.8}$$

And differentiating eq. A.3 with respect to *t* then setting *t=0* gives:

$$K_1(a+b) + K_2(a-b) - \frac{AR\omega}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} = 0 \tag{A.9}$$

Also:

$$K_1 = -K_2 + \frac{A\left(\omega L - \frac{1}{\omega C}\right)}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} = -\frac{AR\omega}{(a-b)\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)}$$

$$+ \frac{K_1(a+b)}{(a-b)} + \frac{A\left(\omega L - \frac{1}{\omega C}\right)}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \tag{A.10}$$

$$K_1((a-b)-(a+b)) = \frac{A\left(R\omega + \left(\omega L - \frac{1}{\omega C}\right)(a-b)\right)}{\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} \tag{A.11}$$

$$K_1 = \frac{A\left(R\omega + \left(\omega L - \frac{1}{\omega C}\right)(a-b)\right)}{-2b\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} \tag{A.12}$$

Similarly,

$$K_2 = \frac{A\left(R\omega + \left(\omega L - \frac{1}{\omega C}\right)(a+b)\right)}{-2b\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} \tag{A.13}$$

Substituting eq.s A.12 and A.13 into eq. A.3 gives:

$$i = \frac{A\left(R\omega - \left(\omega L - \frac{1}{\omega C}\right)(a-b)\right)}{2b\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} e^{(a+b)t} - \frac{A\left(R\omega - \left(\omega L - \frac{1}{\omega C}\right)(a+b)\right)}{2b\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} e^{(a-b)t}$$
$$- \frac{A\sin(\omega t + \phi)}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}} \qquad \text{(A.14)}$$

If b is an imaginary quantity the first and second term can be transformed into oscillatory cos and sin functions. The third term represents a sine wave component the same frequency as the applied RF voltage. Making the substitution $b=-j\beta$ into eq. A.14 where,

$$\beta = \sqrt{-\frac{R^2}{4L^2} + \frac{1}{LC}} \qquad \text{(A.15)}$$

we obtain:

$$i = \frac{A\left(R\omega - \left(\omega L - \frac{1}{\omega C}\right)(a-j\beta)\right)}{j2\beta\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} e^{(a+j\beta)t} - \frac{A\left(R\omega - \left(\omega L - \frac{1}{\omega C}\right)(a+j\beta)\right)}{j2\beta\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} e^{(a-j\beta)t}$$
$$- \frac{A\sin(\omega t + \phi)}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}} \qquad \text{(A.16)}$$

expressing (A.16) in terms of sine and cosines,

$$i = \frac{A\left(R\omega - \left(\omega L - \frac{1}{\omega C}\right)(a-j\beta)\right)}{j\beta\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} e^{at}\left(\cos(\beta t) + j\sin(\beta t)\right) -$$
$$\frac{A\left(R\omega - \left(\omega L - \frac{1}{\omega C}\right)(a+j\beta)\right)}{j2\beta\left(R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2\right)} e^{at}\left(\cos(\beta t) - j\sin(\beta t)\right) - \frac{A\sin(\omega t + \phi)}{\sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}} \qquad \text{(A.17)}$$

If we consider only the case where the input frequency is the same as the LC resonant frequency then we have

$$\omega L - \frac{1}{\omega C} = 0 \tag{A.18}$$

Substituting (A.18) into (A.17) we get:

$$i = \frac{A\omega_r e^{at}}{j2\beta R}\left(\cos(\beta t) + j\sin(\beta t)\right) - \frac{A\omega_r e^{at}}{j2\beta R}\left(\cos(\beta t) - j\sin(\beta t)\right) - \frac{A\sin(\omega_r t)}{R} \tag{A.19}$$

Alternatively,

$$i = \frac{A\omega_r e^{\frac{R}{2L}t}}{\beta R}\sin(\beta t) - \frac{A\sin(\omega_r t)}{R} \tag{A.20}$$

The second term in eq. A.20 represents a steady state sinusoidal current but the first term represents an oscillation which increases exponentially with time.

APPENDIX B: Non-Linear Model of 50nm mHEMT

B.1 Introduction

This appendix describes the development of an accurate table-based non linear model of a 50 nm GaAs/InP mHEMT fabricated using in house technology at Glasgow University. This transistor is used in all the MMICs described in this work.

The process of non linear modelling consists of two stages. The first stage is to determine the small signal model for multiple bias points and the second stage is to combine the small signal models with the IV curves to make a bias and signal - level dependent model. The basic assumption made is that the transistor's non linear behaviour (bias dependence, harmonics, IV curve, gain compression etc) can be approximated by extracting the small signal models at multiple bias points and then combining them into one model. The validity of this assumption can then be tested by comparing the measured and modelled IV curves, S-Parameters, gain compression characteristic and output harmonics due to a single input tone. Another good test is to use the model in a HB/transient oscillator simulation. The output frequency, power and harmonics can then be compared with measurements if available.

First, an 'average' transistor was identified. Then ninety measurements were made at different bias points: from Vds=0 to 0.9 V in 0.1 steps and Vgs =-1.45 to -1.05 in 0.05 V steps and, in addition, two 'cold' bias points were measured i.e. forward biased gate and 0 V on the drain and the gate pinched off with 0 V on the drain. The current range is from 0 to 26 mA. Fig. B.1 shows the measured IV curves the gate voltage increases in steps of 0.05 V.

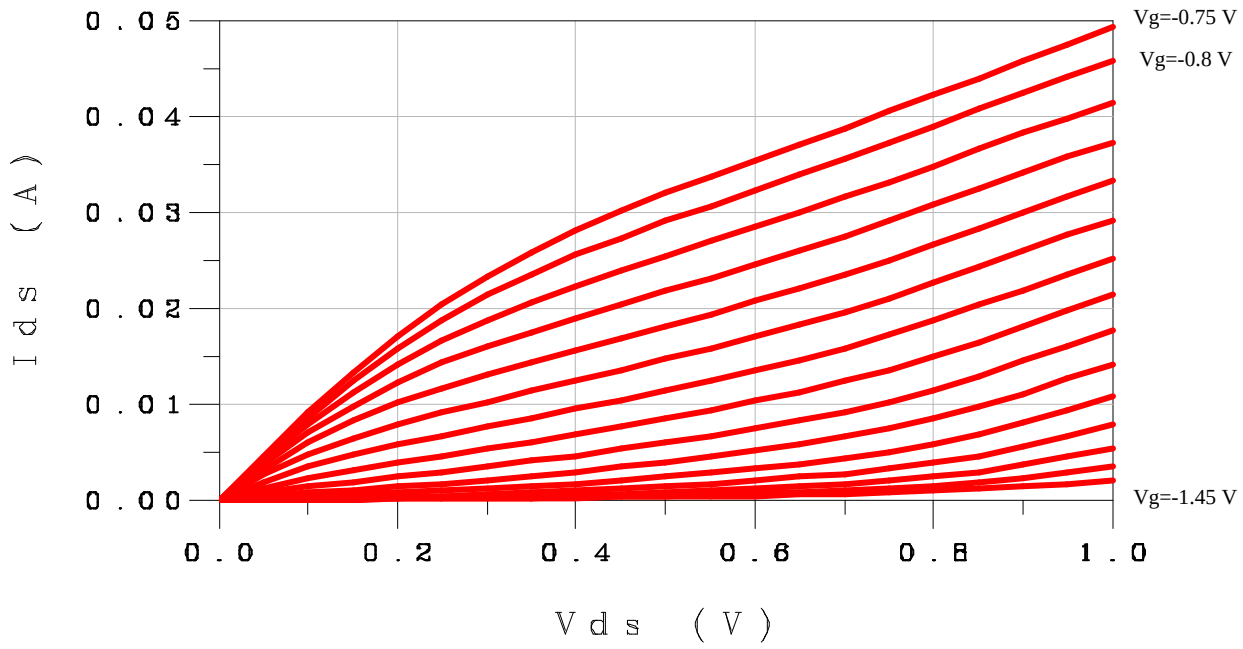


Figure B.1 – Measured IV curves for 50 nm mHEMT

The first stage of non linear modelling, the extraction of the small signal models, can be divided into another two stages: the extraction of the extrinsic components and the extraction of the intrinsic components. The extrinsic or ‘parasitic’ components should not vary with bias i.e. they are linear whilst the intrinsic components do vary with bias and are thus non-linear. The location of these components within the small signal model used in this chapter is shown in fig. B.2

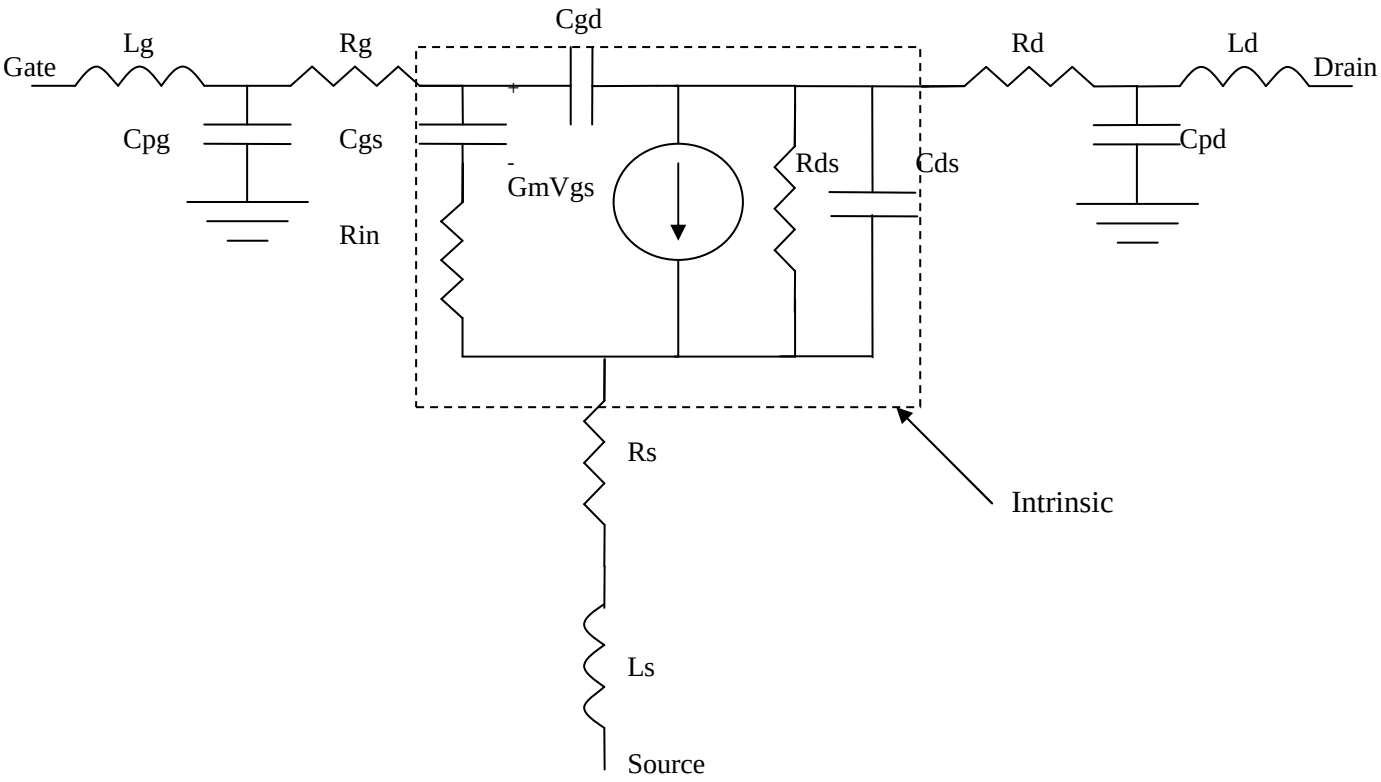


Figure B.2 – Equivalent circuit of a FET showing intrinsic and extrinsic components

The method due to Dambrine [1] for extracting the extrinsic components is used. For the intrinsic components, Berroth's method is used. As will be seen, the values yielded by Dambrine's method require some 'tuning' to achieve a good match between measured and modelled parameters when extracting the intrinsic components. Some tuning is necessary for the extrinsic components whereas *no* tuning is necessary for the intrinsic components. This latter fact considerably speeds up the modelling process.

B.2 Extraction of Extrinsic Components

In Dambrine's method the transistor is biased with 0V on the drain and some positive value on the gate. The gate voltage should be such that the gate-source diode shorts out C_{gs}. The equivalent circuit under these conditions is shown in fig. B.3.

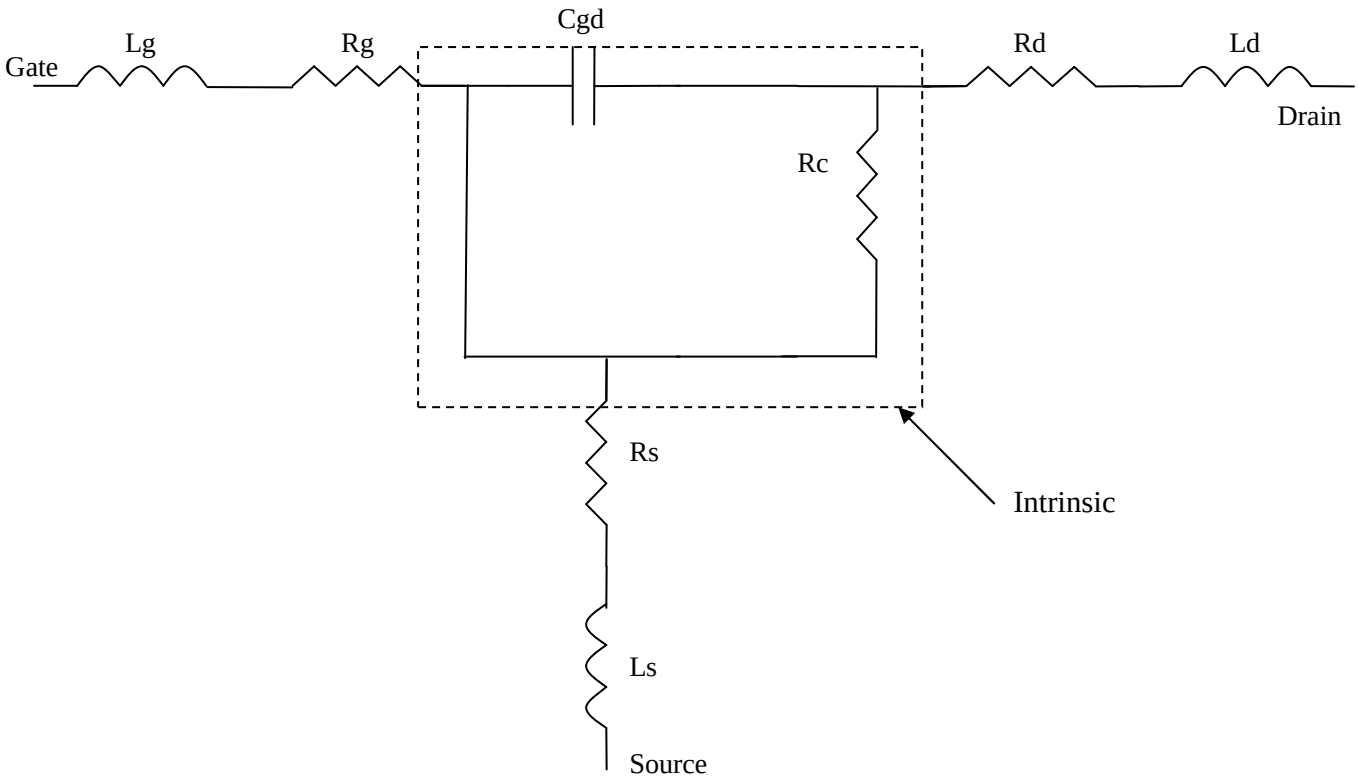


Figure B.3 – Equivalent circuit of FET when gate is forward biased and drain voltage is 0 V

The input reactance obtained should therefore be inductive (i.e. lies in the top half of the Smith Chart). From the measured S-Parameters the extrinsic components L_g, R_g, L_s, R_s, R_d and L_d can be found after de-embedding the CPW lines which allow connection of the device to the on-wafer probes. Forward biasing the device in this manner is likely either to damage the device or modify the characteristics such that S-Parameters measured at the same bias point before and after shorting out the gate-source junction will differ so it is advisable to have two or more transistors with similar characteristics. The next stage is to pinch off the gate by applying a negative gate voltage. This has the effect of making the reflection coefficients purely capacitive. The equivalent circuit under these conditions is shown in fig. B.4.

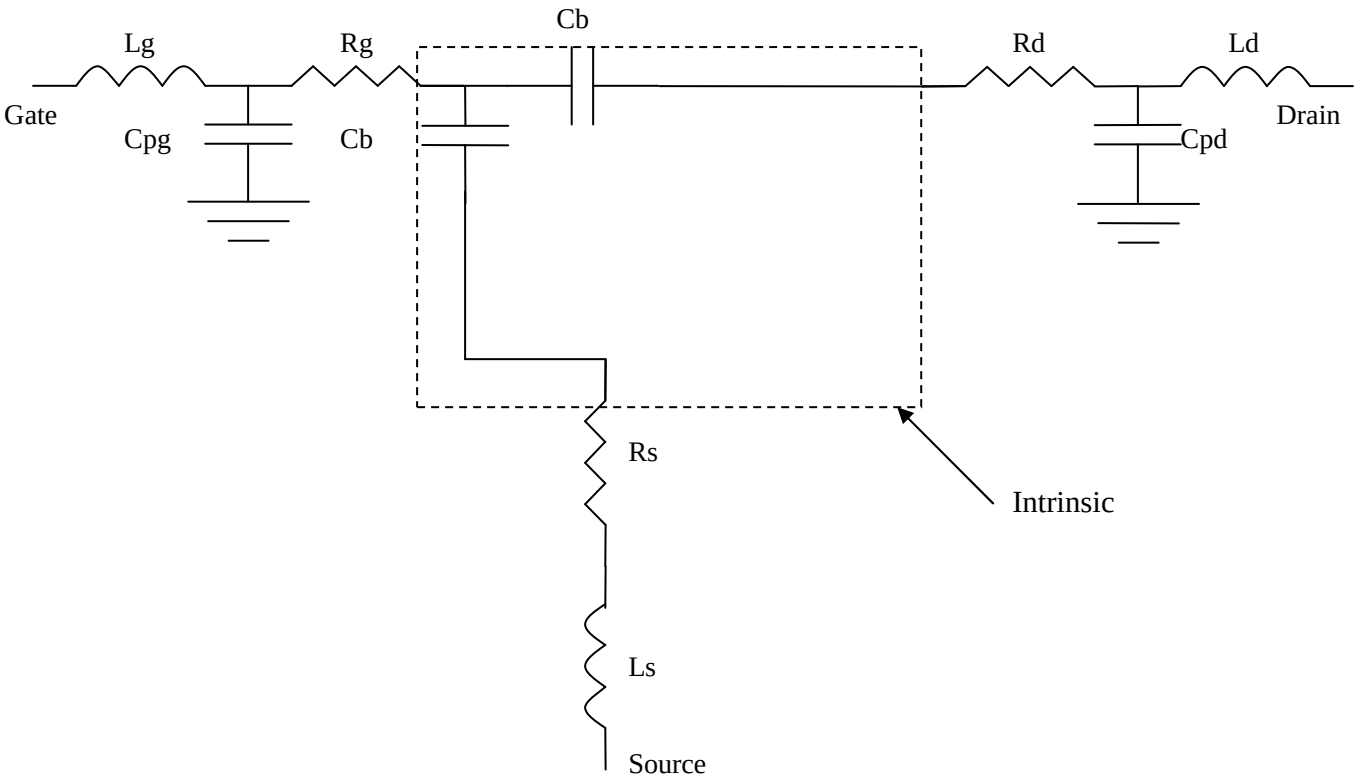


Figure B.4 – Equivalent circuit of FET when gate is pinched off and drain=0 V

The measured S-Parameters can be used to find the extrinsic capacitances C_{pg} and C_{pd}. Now that the extrinsic components are known they can be de-embedded from the measured S-Parameters at a particular bias point to obtain the intrinsic model only. Equations can then be used to obtain values for the intrinsic components.

To reiterate, the gate is pinched off and the drain is at 0V. First a value for R_s is assumed. The actual value can be calculated if the channel resistance is known. However, the channel resistance is not known so a value for R_s is assumed then the extraction is performed. If the curves of the other extrinsic components are not independent of frequency then the value of R_s is changed. In this way, R_s is found iteratively. Before the extrinsic components can be found the S-Parameters are converted to Z-Parameters using standard formulae. Once the value for R_s is found the following equation is used to determine the source inductance, L_s.

$$L_s = \mathrm{Im}\left(\frac{Z_{12}}{2\pi f}\right) \qquad \text{(B.1)}$$

Equations B.2 and B.3 are now used to determine the other parasitic inductances: L_d and L_g:

$$L_g = \mathrm{Im}\left(\frac{Z_{11}}{2\pi f}\right) - L_s \tag{B.2}$$

$$L_d = \mathrm{Im}\left(\frac{Z_{22}}{2\pi f}\right) - L_s \tag{B.3}$$

A new variable R_c is defined as

$$R_c = 2\left(\mathrm{Re}(Z_{12}) - R_s\right) \tag{B.4}$$

also we define the variable '*a*' as:

$$a = \frac{0.026}{Ig} \tag{B.5}$$

where Ig is the gate current. We can now find R_g and R_d from the following:

$$R_g = \mathrm{Re}(Z_{11}) - R_s - \frac{R_c}{3} - a \tag{B.6}$$

$$R_d = \mathrm{Re}(Z_{22}) - R_s - R_c \tag{B.7}$$

Fig. B.5 shows an example of the frequency dependence of the extrinsic inductances. It can be seen that the inductances are relatively independent of frequency so we know that the assumptions made regarding the bias conditions and corresponding simplified equivalent circuit are valid. Fig. B.6 shows the parasitic resistances versus frequency. Again it can be seen that the slope is very close to horizontal.

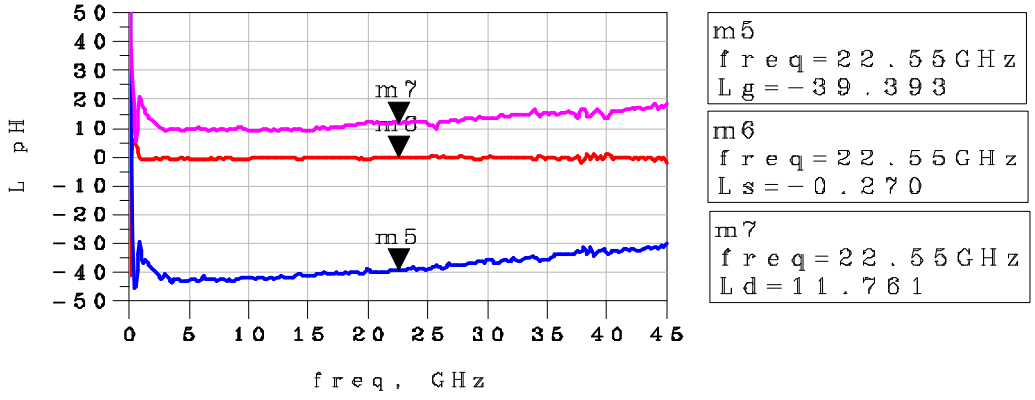


Figure B.5 – Parasitic inductances versus frequency

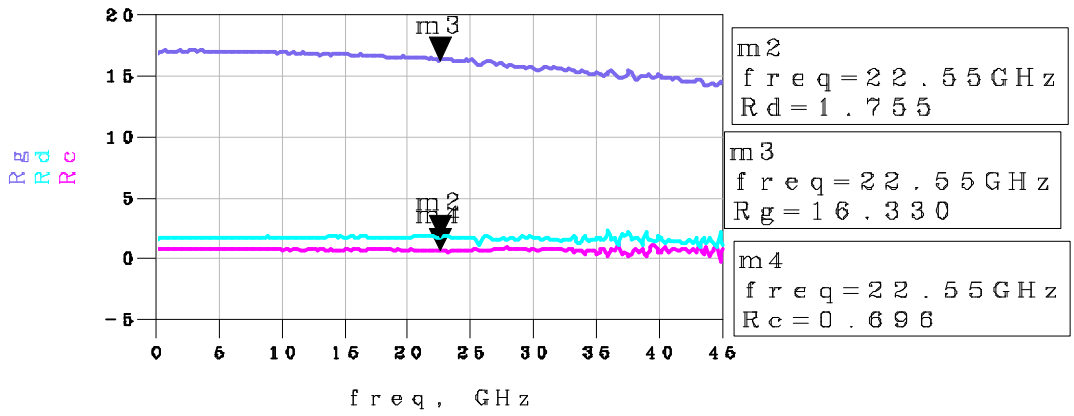


Figure B.6 – Parasitic resistances versus frequency

In order that the remaining extrinsic components can be found the S-Parameters are converted to Y-Parameters using standard formulae. To find the parasitic pad capacitances bias the gate at pinch off and keep Vds at 0 V. First we define a variable, Cb, as:

$$Cb = -\mathrm{Im}\left(\frac{Y_{12}}{2\pi f}\right) \tag{B.8}$$

We can now find C_{pd} and C_{pg} from:

$$C_{pd} = \mathrm{Im}\left(\frac{Y_{22}}{2\pi f}\right) - Cb \tag{B.9}$$

$$C_{pg} = \mathrm{Im}\left(\frac{Y_{11}}{2\pi f}\right) - 2Cb \tag{B.10}$$

Fig. B.7 shows the pad capacitances versus frequency

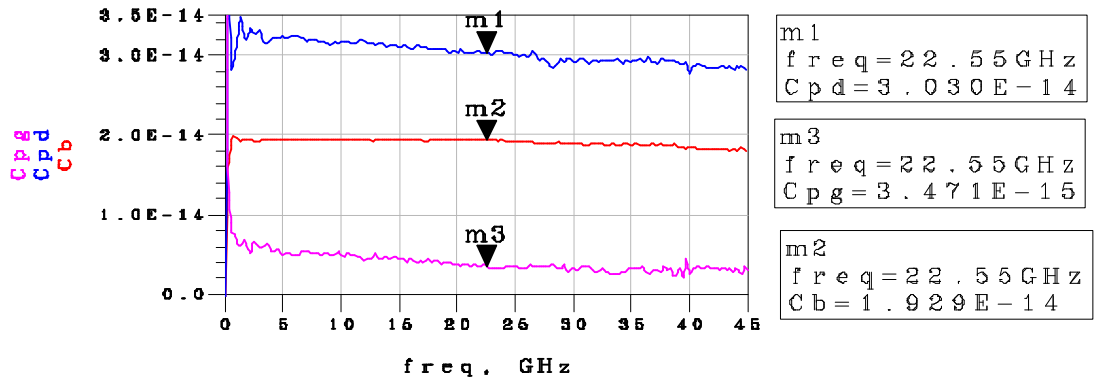


Figure B.7 – Parasitic capacitances versus frequency

Table B.1 shows the extracted values and the optimised (tuned) values used to de-embed the transistor in order to find the intrinsic components. The optimisation goal is to achieve a horizontal characteristic with respect to frequency.

Component	Extracted Value	Optimised value
L_g	-40 pH	0 pH
C_{pg}	3.5 fF	0 fF
R_g	16 Ω	6.16 Ω
L_s	-0.27 pH	0 pH
R_s	1.5 Ω	1.5 Ω
R_d	1.75 Ω	1.5 Ω
C_{pd}	30 fF	15 fF
L_d	11.8 pH	4 pH

Table B.1 – Comparison between extracted and tuned values

It can be seen from Table B.1 that most of the components differ from their extracted values considerably. Note in particular that L_g and L_d are extracted as negative values. This is clearly un-physical and suggests uncertainty in the position of the reference planes e.g. through not placing the probes at the optimum positions during calibration.

B.3 Extraction of Intrinsic Components

Now that the extrinsic components are known, they can be de-embedded from S-Parameter measurements performed at a particular bias point. Berroth's method can now be used to find the intrinsic components. The equations are:

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \tag{B.11}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11}) - \omega C_{gd}}{\omega} \cdot \left(1 + \frac{\left(\mathrm{Re}(Y_{11})\right)^2}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2}\right) \tag{B.12}$$

$$R_{in} = \frac{\mathrm{Re}(Y_{11})}{\left(\mathrm{Im}(Y_{11}) - \omega C_{gd}\right)^2 + \left(\mathrm{Re}(Y_{11})\right)^2} \tag{B.13}$$

$$g_m = \sqrt{\left(\left(\mathrm{Re}(Y_{21})\right)^2 + \left(\mathrm{Im}(Y_{21}) + \omega C_{gd}\right)\right)\left(1 + \omega^2 {C_{gs}}^2 {R_{in}}^2\right)} \tag{B.14}$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22}) - \omega C_{gd}}{\omega} \tag{B.15}$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{22})} \tag{B.16}$$

Figures B.8 to B.11 show examples of the frequency dependence of the extracted intrinsic components. In this case this value of Vgs is -1.25 V and the drain voltage is 0.5 V. It can be seen that the graphs are fairly flat with frequency thus validating the equations used to derive the values. R_{in} is a strong function of frequency but fortunately the overall S-Parameters of the transistor do not vary much with the value of R_{in}.

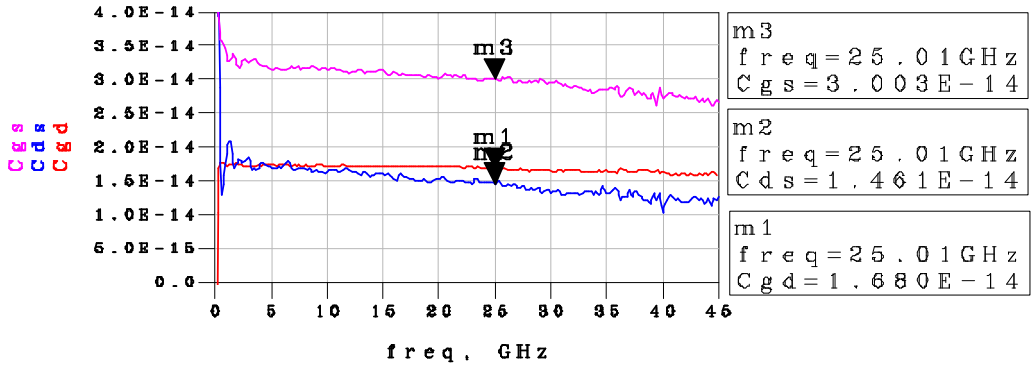


Figure B.8 – Intrinsic capacitances vs frequency at Vds = 0.5 V and Vgs =-1.25 V

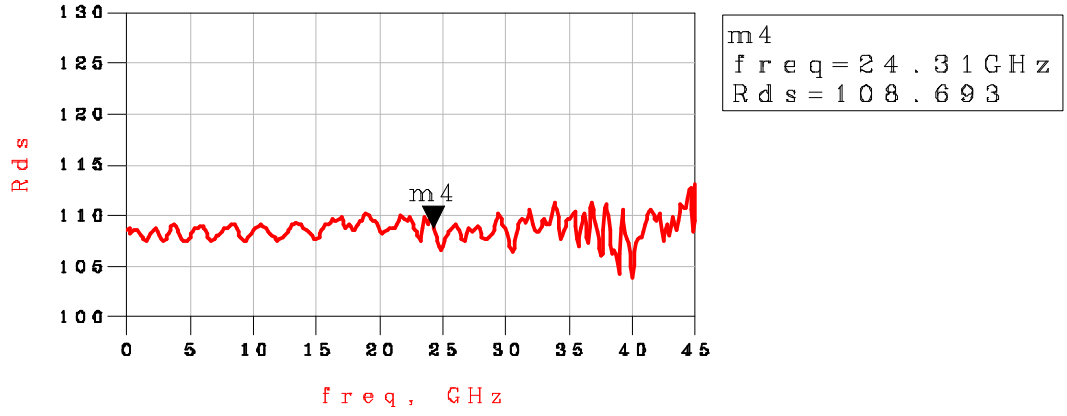


Figure B.9 –Drain-source resistance vs frequency at Vds = 0.5 V and Vgs =-1.25 V

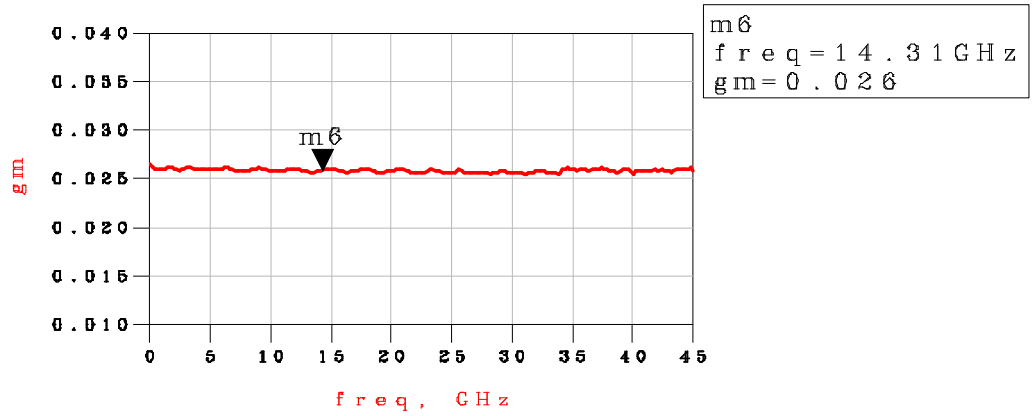


Figure B.10 – Transconductance vs. frequency at Vds = 0.5 V and Vgs =-1.25 V

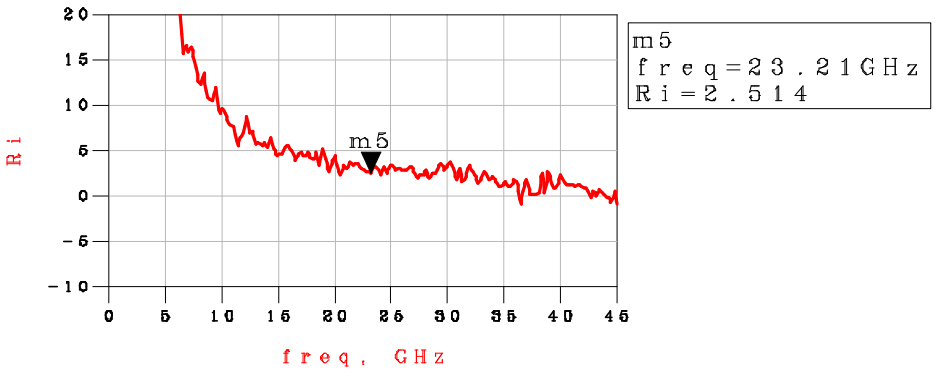


Figure B.11 – Intrinsic resistance vs. frequency at Vds = 0.5 V and Vgs =-1.25 V

Fig.s B.12 through B.16 show the dependence of g_m, R_{ds}, R_{in}, C_{gs}, C_{gd} and C_{ds} respectively on the drain and gate voltages. There are some curious non linear effects particularly around 0.9 Vds but the general trends are as follows:

- G_m is very small for all values of Vds when Vgs is near pinch off. Gm increases as Vgs becomes less negative and Vds becomes more positive.
- R_{ds} is very high when the gate voltage is close to pinch off and Vds is close to zero. R_{ds} decreases when Vgs becomes less negative and also when Vds becomes more positive.
- R_{in} varies little with gate voltage and is negative over most of the range of bias points. R_{in} becomes more positive as the drain voltage is increased.
- C_{gs} increases very smoothly as Vds increases and also as Vgs becomes less negative.

- The influence of the gate voltage on C_{gd} is weak but C_{gd} decreases as the drain voltage is increased.
- C_{ds} decreases as the gate voltage becomes less negative and decreases as the drain voltage is increased.

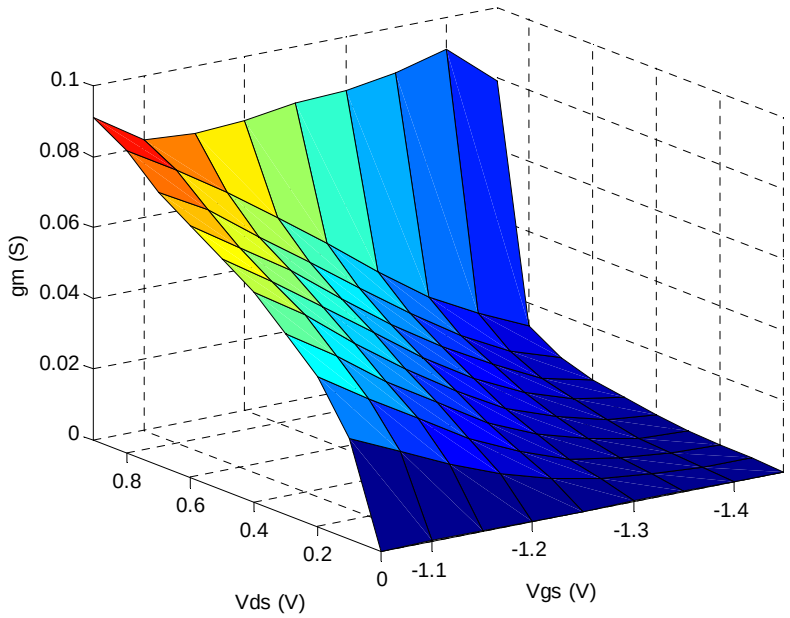


Figure B.12 – Transconductance as a function of Vds and Vgs

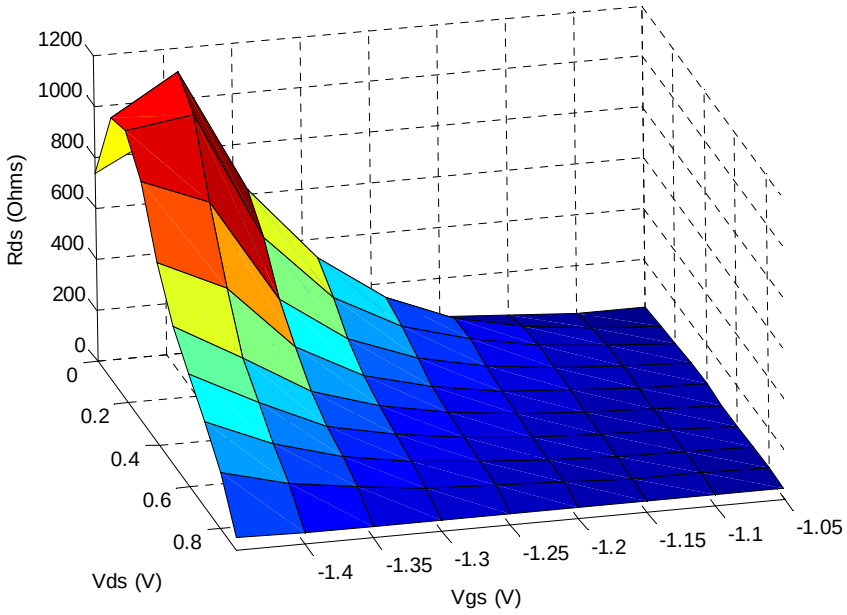


Figure B.13 – Output resistance as a function of Vds and Vgs

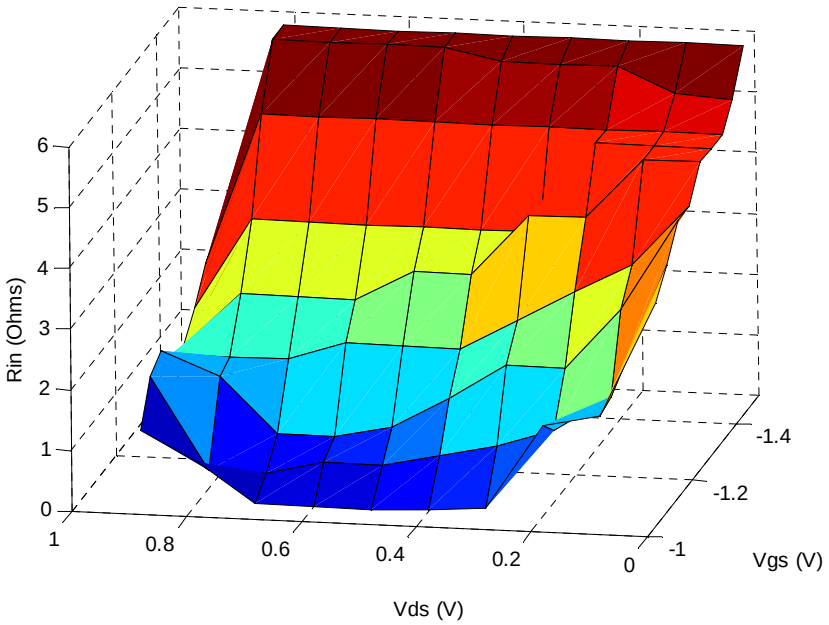


Figure B.14 – Intrinsic resistance as a function of Vds and Vgs

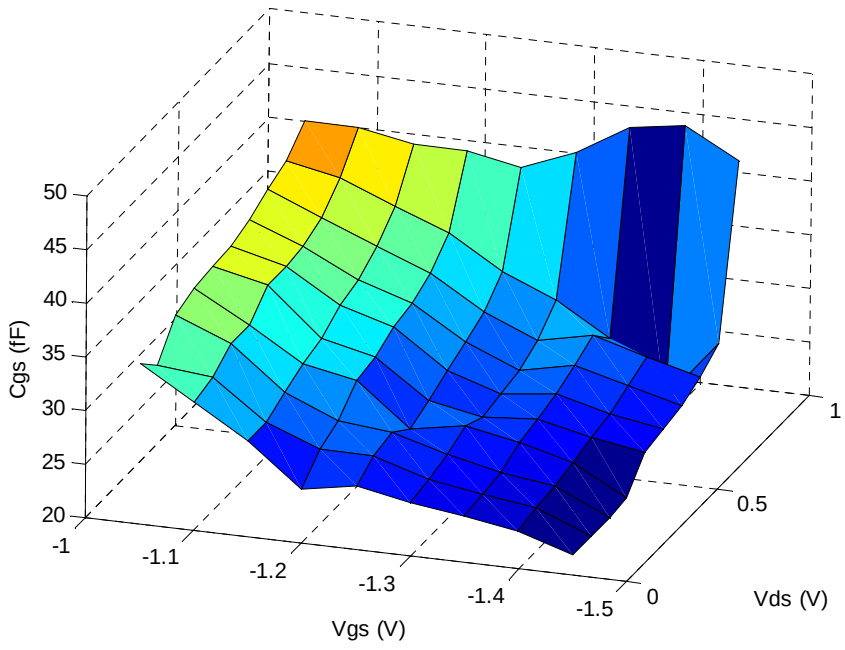


Figure B.15 – Gate-source capacitance as a function of Vds and Vgs

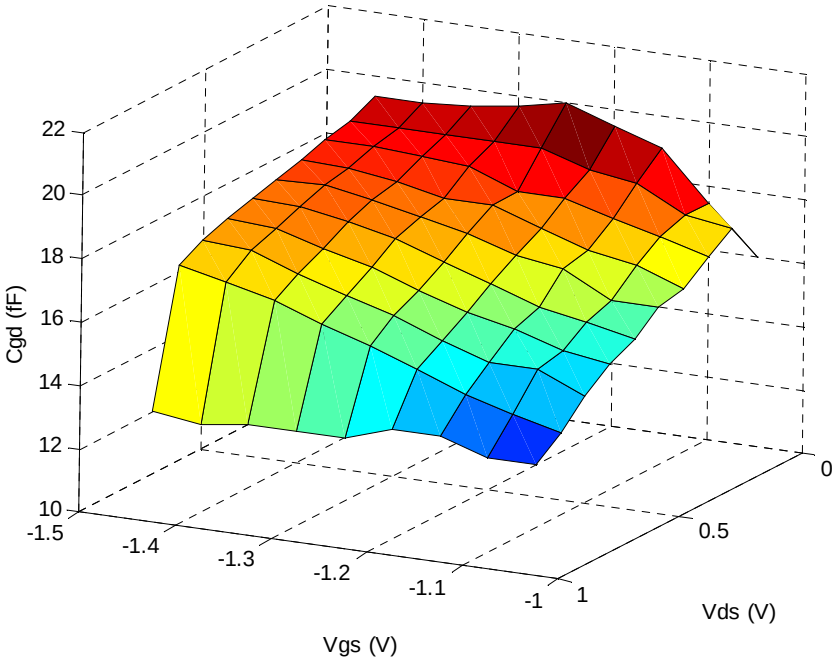


Figure B.16 – Gate-drain capacitance as a function of Vds and Vgs

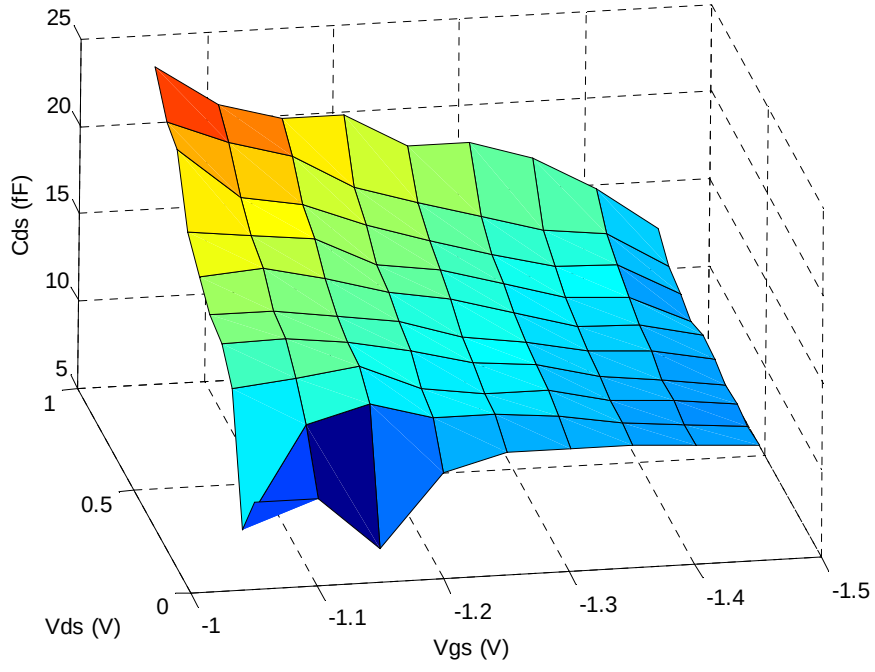


Figure B.17 – Drain-source capacitance as a function of Vds and Vgs

B.4 SDD Implementation of Non Linear Model

Now that the values of the components comprising the model are known for the various bias conditions, they can be combined to produce an SDD (Symbolically Defined Device) non-linear model. This model can be based on curve fitted equations or, as in this thesis, can be linked via a DAC (Data Access Component) to a file containing tables of bias points and corresponding component values. Before the non linear model can be implemented the capacitors need to be converted to charge sources and g_m and R_{ds} need to be converted to a high frequency current source.

Fig. B.18 shows how a current source is implemented in ADS.

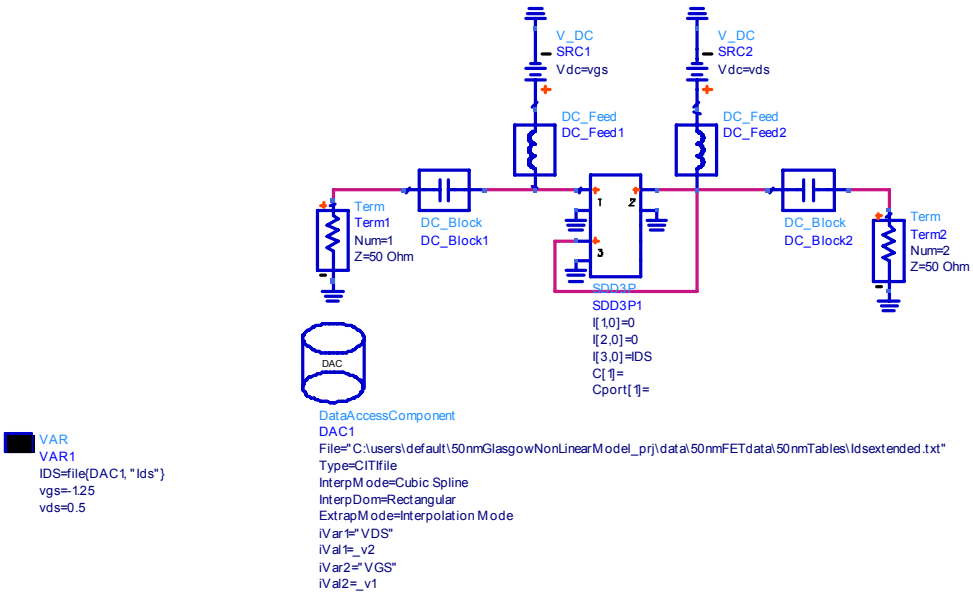


Figure B.18 – ADS implementation of a current source

Here, the current flow from Port 3 to ground is controlled by the two port voltages _v1 and _v2. The instantaneous value of the current is calculated by interpolating the data stored in the table. Before a CITI file can be assembled for g_m and R_{ds} (or the inverse G_{ds}) they can be integrated [3] to form a current table according to:

$$IdsRF = \int_{Vgs0,Vds0}^{Vgs,Vds} gm \cdot dVgs + \int_{Vgs0,Vds0}^{Vgs,Vds} Gds \cdot dVds \qquad \text{(B.17)}$$

Alternatively, they can be modelled by the d.c. curves if the device is not strongly dispersive. Ideally the values of IdsRF should be path independent. It was found,

however, that IdsRF was path dependent. This arises from the fact that the function representing Ids(Vgs,Vds) is not infinitely differentiable. A non linear model in this case can still be derived although the small signal parameters will not match measurements at all bias points. In particular the magnitude of S_{22} and S_{21} will differ as these are the parameters which depend most strongly on g_m and R_{ds}. The d.c. curves were used to model g_m and R_{ds} because of the difficulties just discussed and were found to yield reasonable accuracy.

Fig. B.19 gives an example of a CITIFILE. The values are read out as follows: First value VGS for all values of VDS, second value of VGS for all values of Vds etc. Thus, for instance, the current is 2.5588 mA when Vgs = -1.05 and Vds = 0.05.

```
CITIFILE A.01.00
NAME DATA
VAR VGS MAG 10
VAR VDS MAG 19
DATA IDS MAG
VAR_LIST_BEGIN
-1.05
-1.1
VAR_LIST_END
VAR_LIST_BEGIN
0
0.05
0.1
VAR_LIST_END
BEGIN
0
0.0025588
0.00465707

0
0.00155646
0.00276932
END
```

Figure B.19 – Example of CITIFILE current table

In contrast to other table based models [3,4], none of the capacitors are lumped together. Instead, each capacitor is represented by a charge source. This has the benefit of preserving the topology of the small signal model and it is also more convenient to perform the numerical integration this way. Q_{gs} is given by:

$$Q_{gs} = \int_{Vgs0,Vds0}^{Vgs,Vds} C_{gs} \cdot dVgs \qquad \text{(B.18)}$$

Q_{ds} is given by:

$$Q_{ds} = \int_{Vgs\,0,Vds\,0}^{Vgs,Vds} C_{ds} \cdot dVds \tag{B.19}$$

whilst C_{gd} is split into two parts. The first of which is given by:

$$Q_{gd} = \int_{Vgs\,0,Vds\,0}^{Vgs,Vds} C_{gd} \cdot dVgs \tag{B.20}$$

The second part of Q_{gd} is given by:

$$Q_{gd} = \int_{Vgs\,0,Vds\,0}^{Vgs,Vds} C_{gd} \cdot dVds \tag{B.21}$$

The total charge is then found by subtracting eq. B.20 from eq. B.21. In order to find the charge sources the capacitance data is numerically integrated with respect to the local voltage. For example to find Q_{gs} we fix Vds and integrate with respect to Vgs from 0 V to the particular bias point of interest. Fig. B.20 shows a plot of the charge function Q_{gs}.

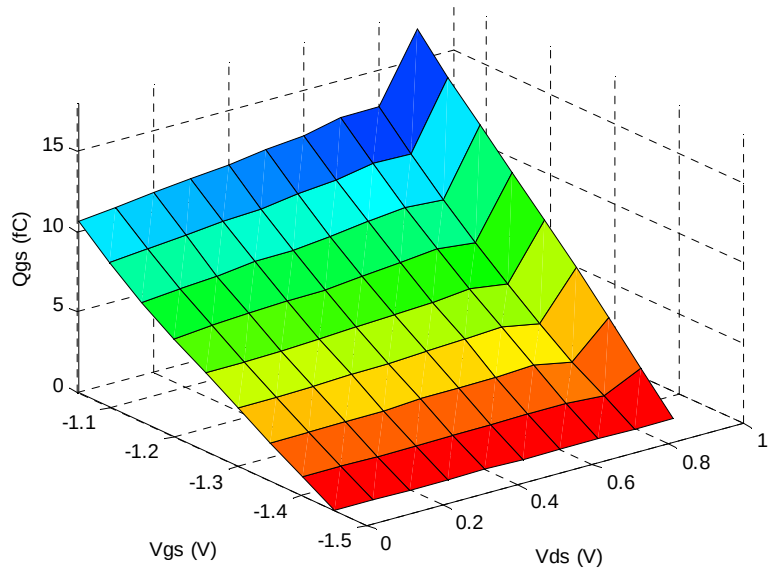


Figure B.20 – Plot of Q_{gs} charge function

Fig. B.21 shows the ADS schematic for the model.

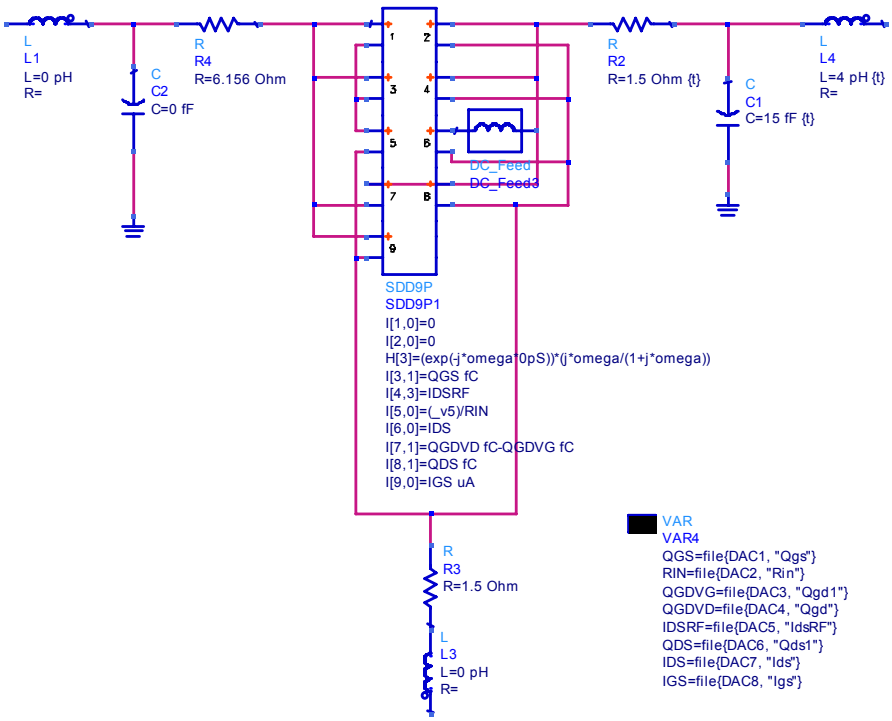


Figure B.21 – ADS schematic of the non linear model

Ports 1 and 2 are the controlling voltages for the whole circuit. It is these voltages which determine the values of the components as a function of both the d.c. and a.c. voltage. Both have the current set to zero so as not to disrupt the RF signals. The control voltage ‘ _v1’ is connected across Cgs and the control voltage ‘_v2’ is connected across R_{ds}, C_{ds} and g_m. Port 3 corresponds to Q_{gs}. Q_{gs} is represented by a charge table which is a function of the two voltages and has a weighting function of 1 i.e. jω or d/dt in the time domain since the voltage equals the time derivative of the charge.

C_{gd} (port 7) and C_{ds} (port 8) are also modelled by charge sources. The correct polarity must be observed in all cases. The gate current is stored in a table and is assigned to port 9. The inclusion of the gate current means that the phase of S_{12} matches measurements at low frequencies. If the gate current is not included the phase of S_{12} starts at 90 degrees instead of 0 degrees. All port equations are linked to DACs (Data Access Components). The independent variables are set to ‘ _v1’ and ‘_v2’ whilst the interpolation is set to cubic spline. The optional RF current has a weighting function with a high pass response with the option to include a time delay. The d.c. current has a d.c. feed (idealised inductor) connected in series. This arrangement ensures that the d.c. current has no effect on the RF signals and that the RF current has no effect on the d.c. curves.

B.5 Model Validation

Figs. B.22 and B.23 show the IV curves for the drain and gate respectively. The Ids curves are out by as much as 0.06 V at high currents due to the difference between internal (_v1 and _v2) and external (measured) node voltages. In other words the difference is due to the voltage drop across R_s and R_d. For more accurate modelling the voltages in the look up table need to be re-referenced. At the gate side, the voltage drop across R_g and R_s is negligible as the gate current is very small.

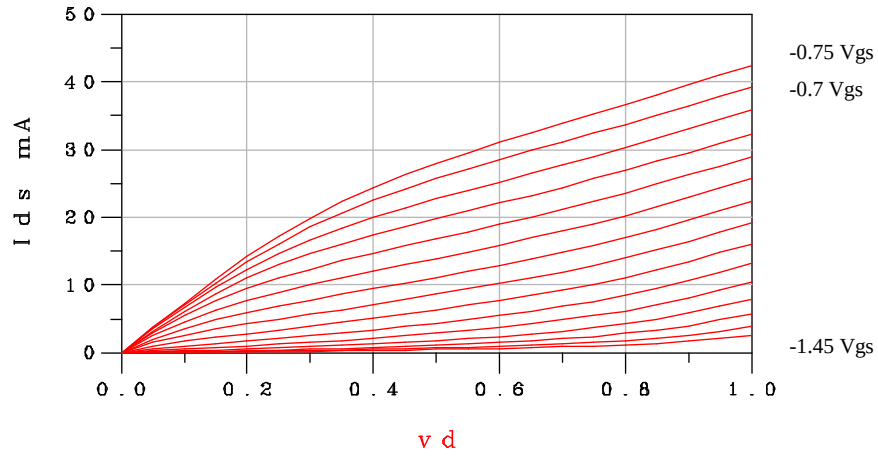


Figure B.22 - Simulated IV curves for 50 nm PHEMT

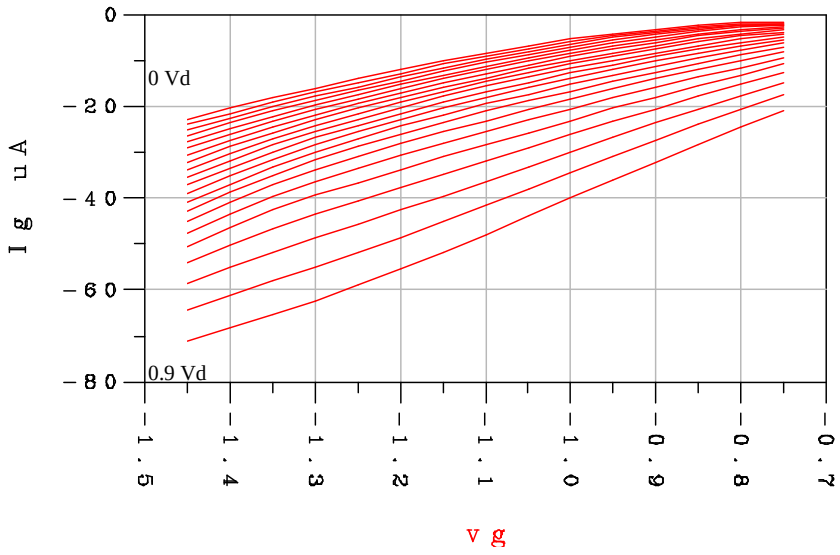


Figure B.23 – Simulated gate current for 50nm PHEMT

Figs. B.24 to B.26 show the measured and modelled S-Parameters at a particular bias point: Vgs = -1.3 V and Vds = 0.5 V.

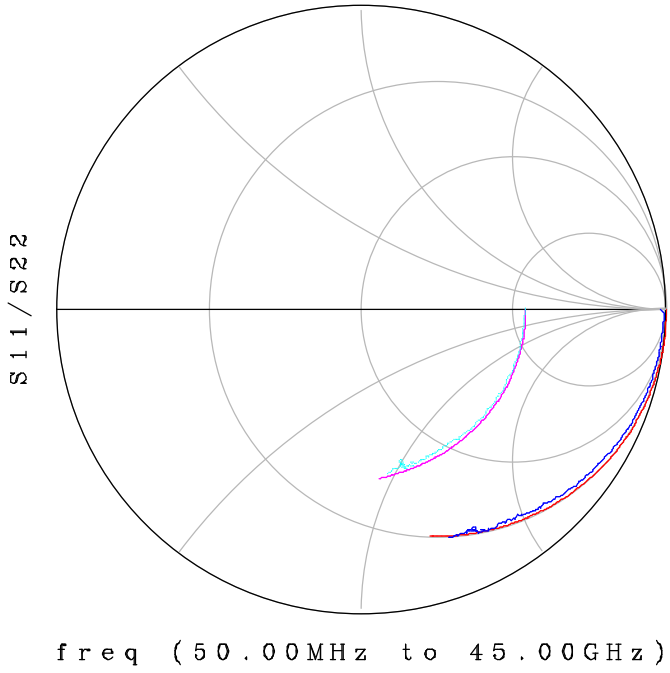


Figure B.24 - Measured and modelled S_{11} and S_{22}

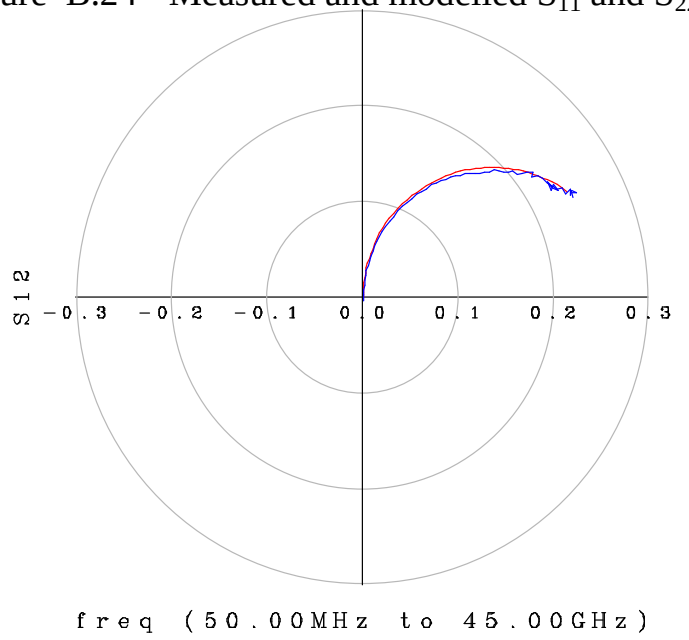


Figure B.25 - Measured and modelled S_{12}

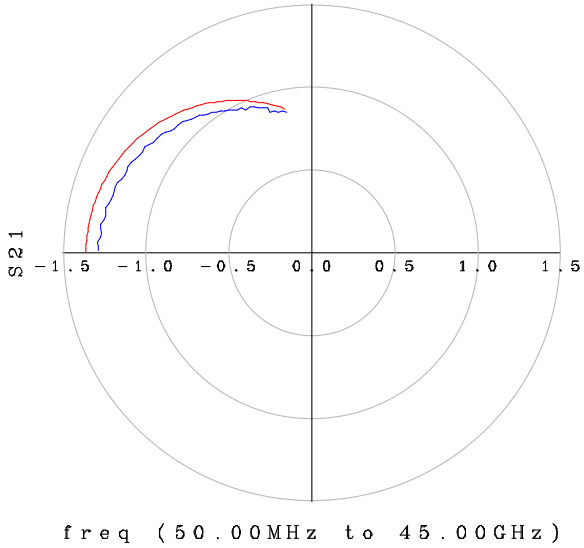


Figure B.26 - Measured and modelled S_{21}

The gain compression characteristic is shown in Fig. B.27. The simulated results are in good agreement with measured values. The max error is 1 dB. The agreement can be made exact by modelling the transistor over a very wide range of gate voltages.

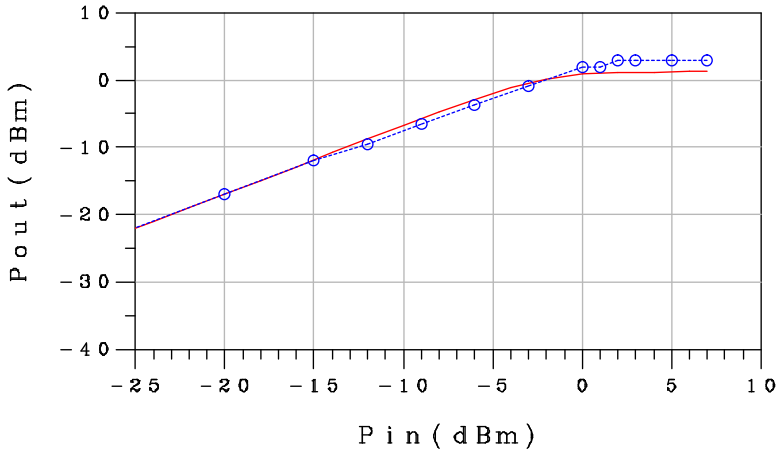


Figure B.27 - Measured and modelled gain compression characteristic

Table B.2 shows the measured and modelled output spectra for two slightly different bias points. The largest error is in the third harmonic.

	Vds	Vgs	Fund. Out (dBm)	2nd Harmonic (dBm)	3rd Harmonic (dBm)
measured	0.5	-1.25	-10	-33	-46
modelled	0.5	-1.25	-9.5	-31	-51
measured	0.5	-1.3	-12.5	-31	-52
modelled	0.5	-1.3	-10.5	-30	-52.5

Table B. 2 - Measured and modelled one tone test (frequency=2 GHz, Pin=-15 dBm)

The model can be used in a time domain oscillator simulation. Fig. B.28 shows the start up transient. Note that the oscillator output reaches a steady state. The frequency of oscillation is 6.96 GHz.

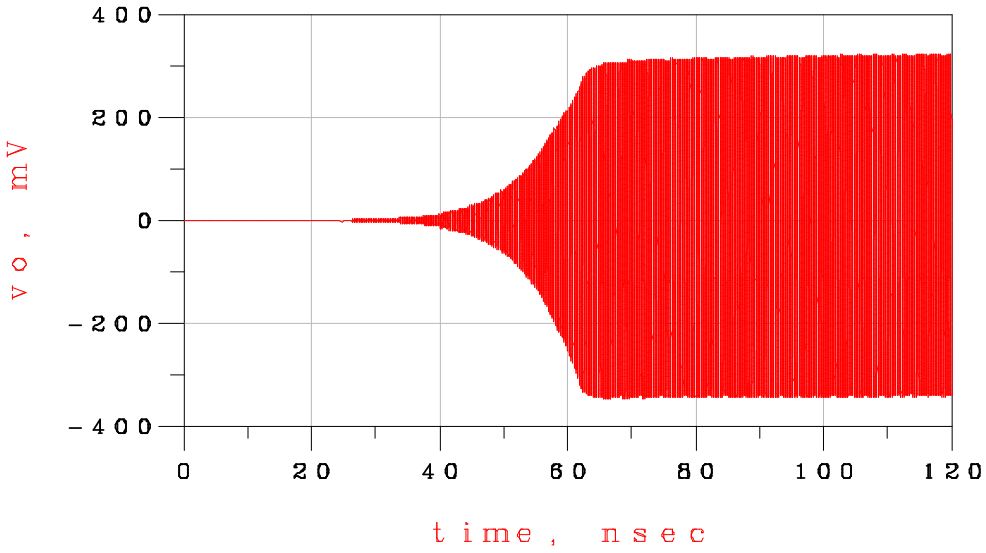


Figure B.28- Time domain oscillator start up transient

This appendix has presented a step by step guide to the implementation and verification of a table based non linear model. No curve fitting is necessary. This fact considerably simplifies the process of non linear modelling.

APPENDIX C: Step Recovery Diode Look-Up Model

C.1: Introduction

In this appendix, the first reported look-up non linear model of a Step Recovery Diode is described. The model uses a more elaborate parasitic network and contains more non linear elements than models previously described. Good agreement is obtained between the measured and modelled results in both the small signal and time domain. Finally, a new bi-phase wavelet generator is described whose output consists of two cycles of 2.4 GHz carrier whose polarity is controlled by the positive and negative transitions of a bipolar data source.

UltraWideBand (UWB) Technology offers many potential benefits such as high data rates, increased resolution in radar applications and increased security. Following from the discussion in sections 4.3 – 4.4, UWB can be considered to be a form of ultra low duty cycle OOK and therefore has the potential to deliver extremely small power consumptions. Ultra short pulses are required for UWB hence the attention pulse generators have received in the literature. Step Recovery Diode (SRD) pulse generators have proved popular for UWB applications in both their fixed [1,2] and variable [3,4] pulse width varieties. In order to investigate performance characteristics such as pulse width, amplitude and ringing, accurate models are required. To date a few workers have constructed models of SRDs. Particular attention has been paid to the problem of modelling the sudden change in junction capacitance that occurs when the diode is sufficiently forward biased. Some have modelled the capacitance as two piecewise linear charge sources [5,6] whilst others have modelled it as two linear capacitors controlled by a switch [7]. The approach in this work is to have a non linear charge source to represent the ‘reverse’ capacitance with a switched high valued linear capacitor in parallel to represent the ‘forward’ capacitance. This approach was found to accurately model the S-Parameters of the diode and the time domain response of SRD

pulse generators. Moreover the convergence properties in time domain simulations are good.

Other researchers have modelled the IV curve by a voltage controlled resistor [5-7] whilst this appendix uses the measured IV curve - re-referenced for higher currents to take account of the voltage drop across the series resistance. The parasitic network is extended to include an extra parasitic inductor and capacitor in order to more accurately model the small signal parameters.

An impulse contains significant low frequency components. It can therefore be hard to radiate and receive without significant distortion unless large antennas with a low cut off frequency are used. One way around this problem is to use more than one impulse to simulate short bursts of an RF carrier. This has the effect of centring the spectrum of the pulse around a carrier frequency (see fig. C.12). One way to achieve such an output is presented in this appendix. The circuit outputs two back to back impulses of a positive polarity when it is input a positive to negative transition and outputs two back to back impulses of opposite polarity when it is input a negative to positive transition.

The proposed model is shown in fig. C.1.

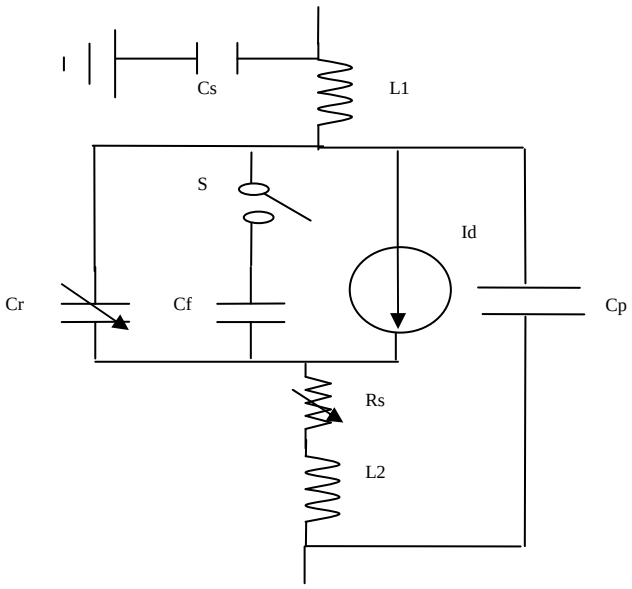


Figure C.1 – Circuit model of the SRD

L1, L2, Cs and Cp represent the package parasitics whilst the current source, Cr and Rs are all non linear. Cf is linear and is switched into the circuit above a certain value of

forward bias. Cr is modelled as a charge source and is connected in parallel with Cf so that its effect when Cf is switched on is negligible.

The methodology used to model the SRD is measurement based. First the IV curve is measured. Then the S-Parameters of the device connected between a transmission line and ground are measured at a number of bias points: from -2 V to 1.2 V in this particular case. The measured S-Parameters are used to derive a small signal model at each bias point. The bias dependence of the non linear elements is now known. These can be directly assembled in a table in the case of the current source and series resistance or can be numerically integrated in the case of Cr to form a charge table according to:

$$Qr = \int_{0}^{Vb} Cr.dVb \tag{C.1}$$

where Vb is the (internal) voltage across the 'reverse' capacitance. Look up tables are used because they can model complex behaviour without the need to fit equations to measured data.

C.2 Model Implementation

The SRD modelled in this chapter is SMMD840 –SOD323 from Aeroflex-Metelics. Fig. C.2 shows the modelled IV curve. The measured and modelled IV curve is exactly the same since the measured, re-referenced, IV curve is copied to a table and linked to the circuit.

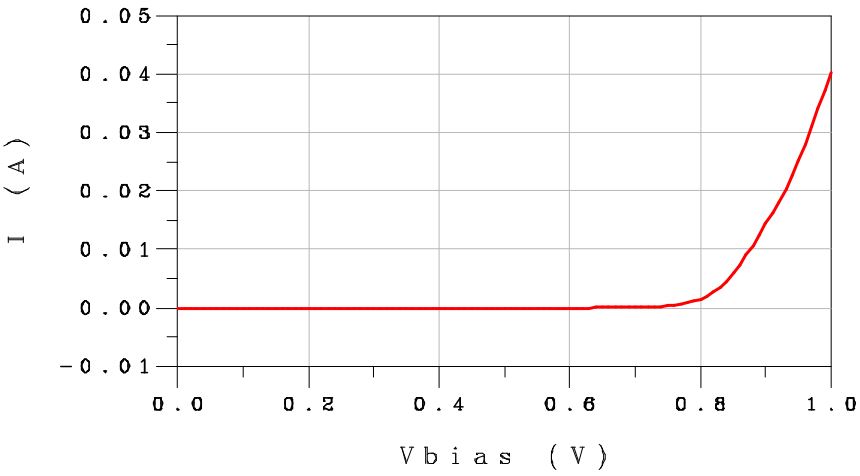


Figure C.2 – IV curve of the SRD

Fig. C.3 shows the modelled charge characteristic of the ‘reverse’ capacitance.

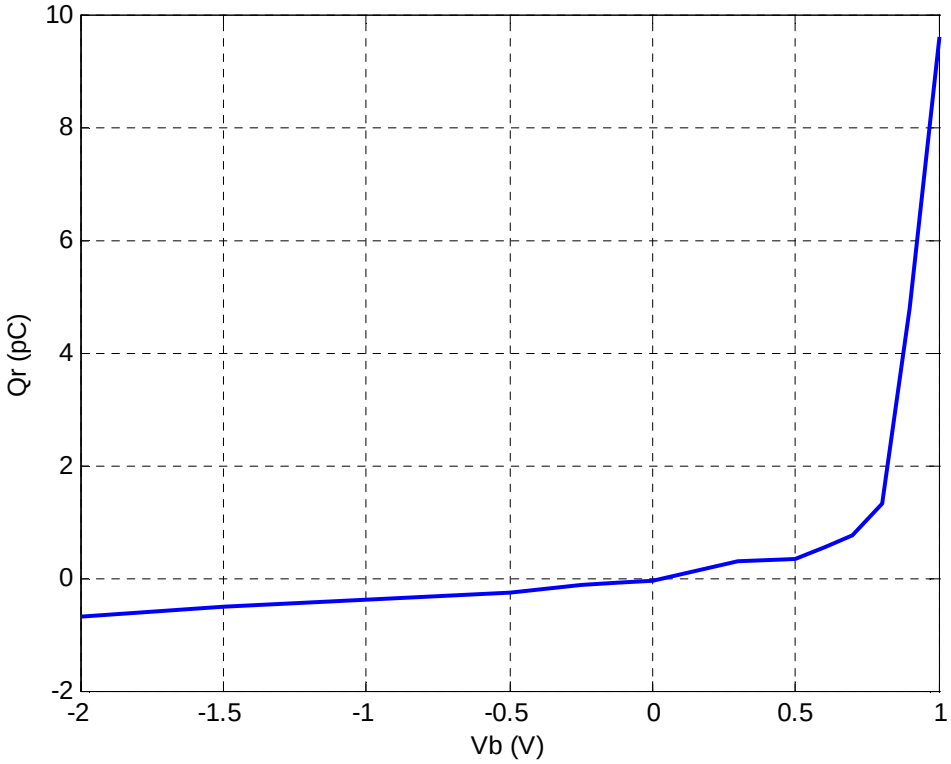


Figure C.3 – Modelled reverse charge curve of the SRD

Note that the charge function is extrapolated above the point (0.72V) where the forward capacitance is turned on – this is to ensure good convergence in time domain simulations.

It was found that in order to make the S-Parameters of the model match to the measured results it was necessary to make Rs non linear. Fig. C.4 shows a graph of the series resistance versus bias voltage.

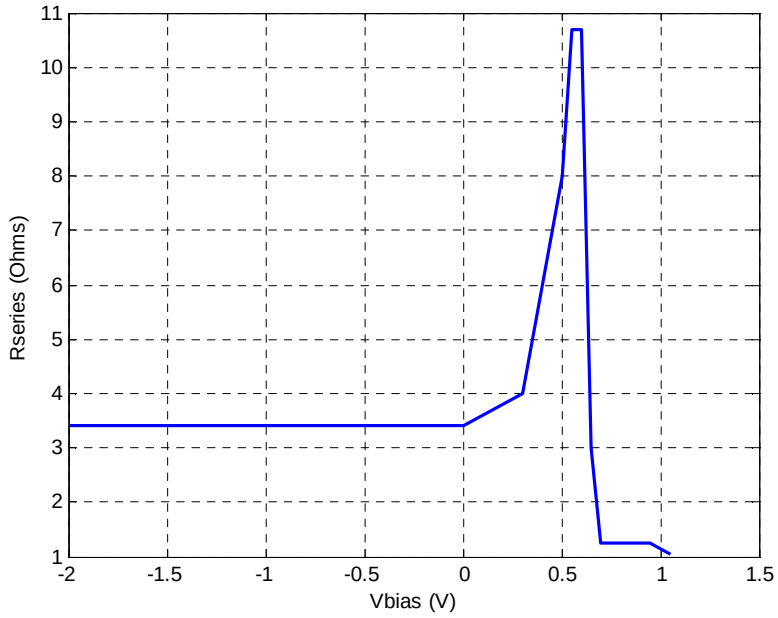


Figure C.4 – Plot of series resistance versus bias voltage

It can be seen that the resistance is highly non linear, being almost constant until 0V where it rises sharply and then falls again after 0.5 V.

The model is implemented as an SDD (Symbolically Defined Device) running in Agilent's ADS. The values of the non linear elements are linked to CITIFILEs via a DAC (Data Access Component). Fig.5 shows the circuit diagram of the model.

Port 1 contains the current source representing the measured characteristic. Port 2 is the reverse charge source and has a weighting function of 1. A weighting function of 1 is equivalent to a time derivative or multiplication by jω in the frequency domain.

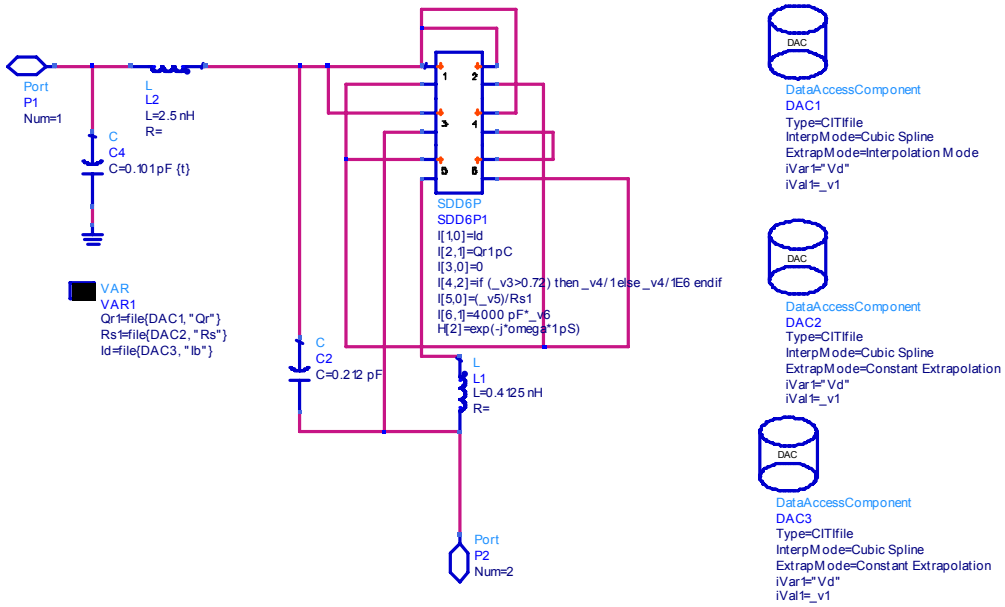


Figure C.5 – ADS schematic of the SRD model

Port 4 implements a switch which closes above 0.72 V and is open circuit otherwise. The controlling voltage for the switch is the voltage across port 3. The switch is connected in series with the forward (linear) capacitance Cf. In this particular case Cf is 4000 pF. To make the model more physical, a time delay of 1 pS is associated with the switch. The time delay is implemented with the weighting function H[2]:

$$H[2] = e^{-j\omega 1.10^{-12}} \qquad \text{(C.2)}$$

C.3 Model Validation

Figs. C.6 and C.7 show the measured and modelled S-Parameters at two different bias points - reverse biased and forward biased beyond the point when Cf is switched into the circuit.

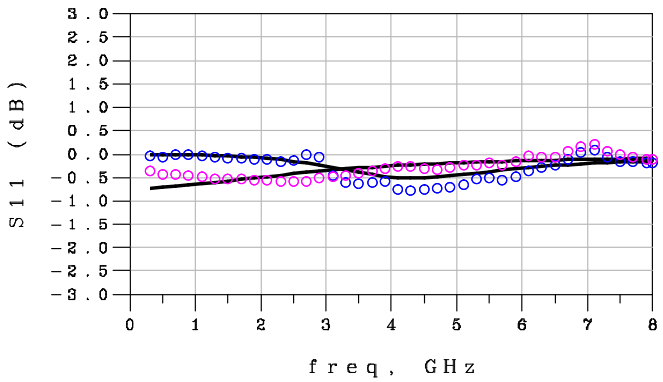


Figure C.6 – Measured (circles) and modelled S_{11} (dB) at -0.5 V and 0.85 V bias

It can be seen that the agreement at both bias points is good thus validating the model in the small signal domain.

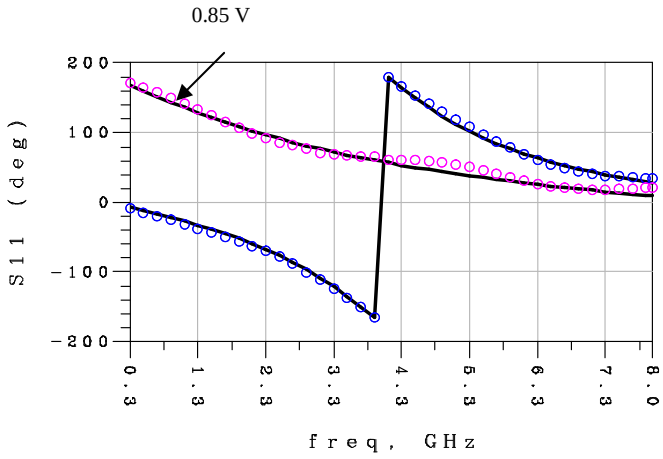


Figure C.7 – Measured (circles) and modelled S_{11} (deg) at -0.5 V and 0.85 V bias

C.4 Bi-Phase Wavelet Generator

A more rigorous test of the model than S-Parameter comparisons is in time domain simulations. For this purpose a pulse generator was designed. It consists of a series connected SRD with a small length of shorted transmission line at the output (cathode) side to form an impulse [2]. Fig. C.8 shows the ADS schematic for the impulse generator.

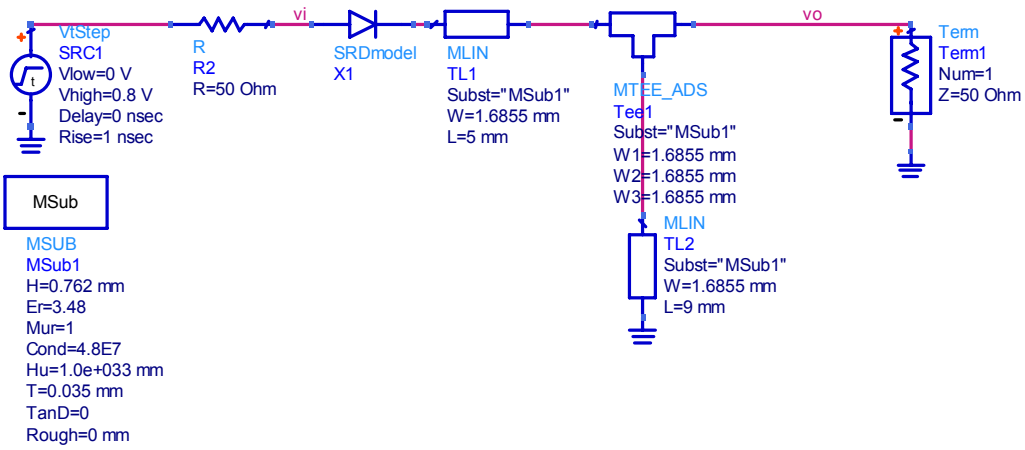


Figure C.8 – ADS schematic of the impulse generator

Fig. C.9 shows the measured and modelled output waveform. It can be seen that the agreement is good. The circuit triggers on a positive to 0 V transition and the pulse width is approximately 400 pS.

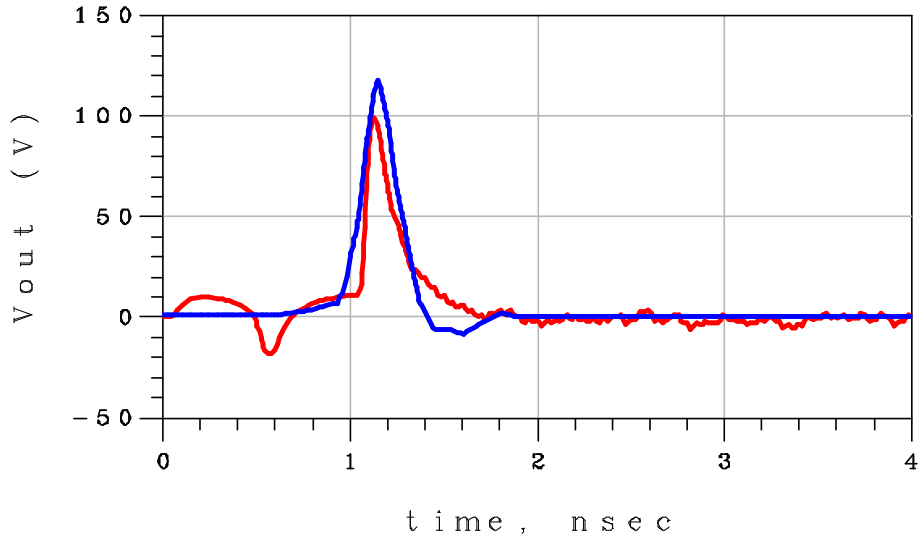


Figure C.9 – Measured (blue) and modelled (red) output waveform of the impulse generator

A dual cycle pulse generator can be made by connecting two pulse generators in parallel and then combining the outputs with a Wilkinson Coupler (W.C.). One output is delayed by a time equal to the pulse width before being combined with the other pulse. A bi-phase UWB modulator can be constructed by adding the output of two pulse

generators with the polarity of the diodes reversed to the output of the other composite pulse generator via another Wilkinson Coupler. This arrangement is shown in Fig. C.10.

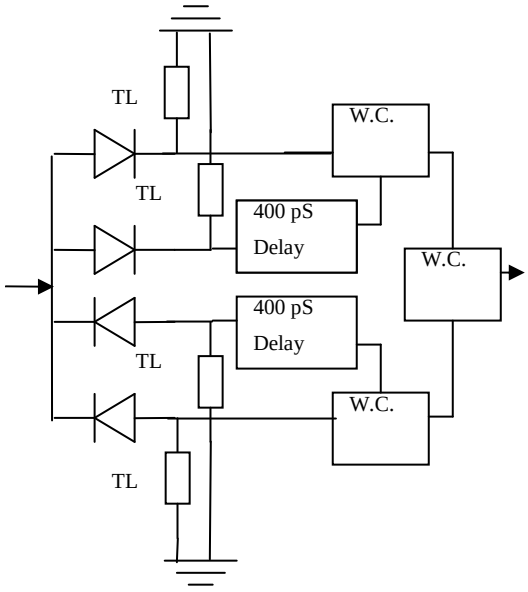


Figure C.10 – Schematic for Bi-phase wavelet generator

The circuit outputs two back to back impulses of positive polarity when there is input a +V to -V transition and outputs two back to back impulses of opposite polarity when it is input a –V to +V transition. Fig. C.11 shows the simulated (red) and measured (blue) output waveforms for negative polarity. It can be seen that the agreement is fairly good. The agreement for positive polarity pulses is similarly good.

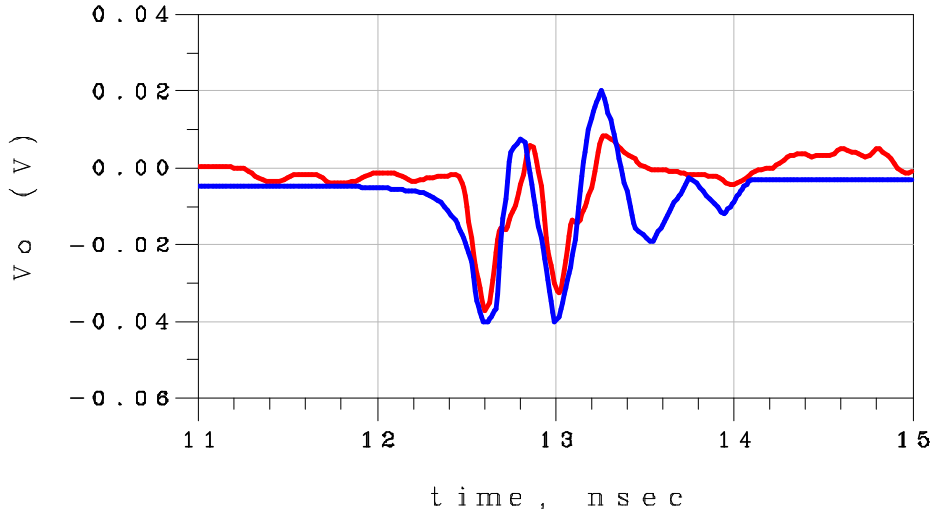


Figure C.11 – Measured (blue) and modelled (red) output waveform of the Bi-phase wavelet generator

Fig. C.12 shows the simulated and measured spectrum of the waveforms in fig. C.11. It can be seen that good agreement is obtained and that the wavelet generator output is centred around 2.2 GHz with a bandwidth of approximately 1 GHz.

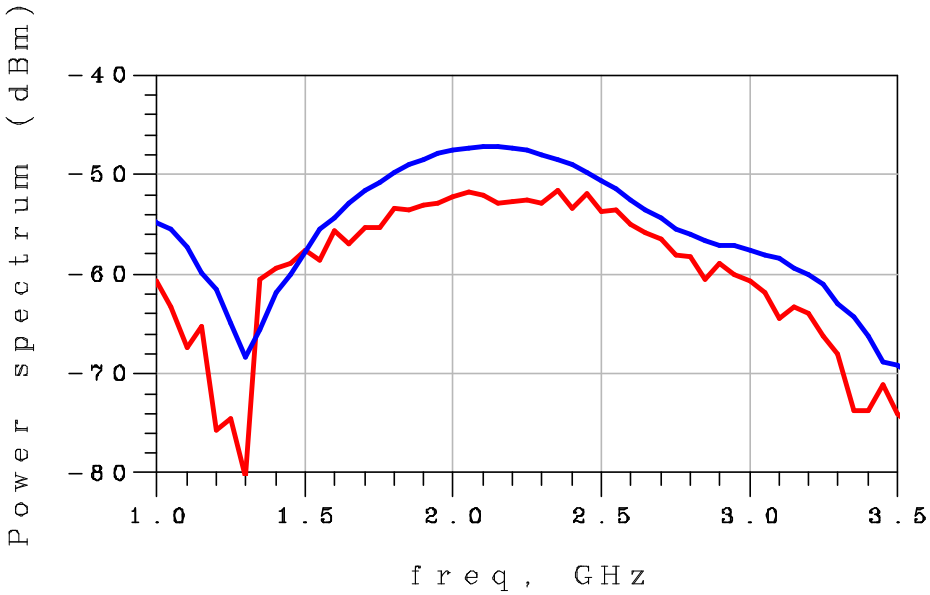


Figure C.12 – Measured (blue) and modelled (red) power spectrum of the Bi-phase wavelet generator

This appendix has described a new measurement based look-up model of an SRD. The agreement obtained in both S-Parameter and time domain simulations are good. Also, a new Bi-Phase Wavelet generator has been described. The circuit outputs either a positive or negative polarity waveform consisting of two back to back impulses. Again good agreement is obtained between measured and modelled results.

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