Thermoelectric Properties on $Ge/Si_{1-x}Ge_x$ Superlattices

Lourdes Ferre Llin

A thesis submitted to

School of Engineering, University of Glasgow

Doctor of Philosophy

November 2013

Abstract

Thermoelectric generation has been found to be a potential field which can be exploited in a wide range of applications. Presently the highest performances at room temperature have been using telluride-based devices, but these technologies are not compatible with MEMs and CMOS processing. In this work Silicon and Germanium 2D superlattices have been studied using micro fabricated devices, which have been designed specifically to complete the thermal and electrical characterization of the different structures.

Suspended 6-contact Hall bars with integrated heaters, thermometers and ohmic contacts, have been micro-fabricated to test the in-plane thermoelectric properties of p-type superlattices. The impact of quantum well thickness on the two thermoelectric figures of merit, for two heterostructures with different Ge content has been studied.

On the other hand, etch mesa structures have been presented to study the cross-plane thermoelectric properties of p and n-type superlattices. In these experiments are presented: the impact of doping level on the two figures of merit, the impact of quantum well width on the two figures of merit, and the more efficient reduction of the thermal conductivity by blocking phonons with different wavelengths. The n-type results showed the highest figures of merit values reported in the literature for Te-free materials, presenting power factors of $12\,\mathrm{mW/K^2 \cdot m}$, which exceeded by a factor of 3 the highest values reported in the literature.

The results showed, that Si and Ge superlattices could compete with the current materials used to commercialise thermoelectric modules. In addition, these materials have the advantage of being compatible with MEMs and CMOS processing, so that they could be integrated as energy harvesters to create complete autonomous sensors.

Publications

Publications arising from this work

D.J. Paul, A. Samarelli, **L. Ferre Llin**, Y. Zhang, J.M.R. Weaver, P.S. Dobson, S. Cecchi, J. Frigerio, F. Isa, D. Chrastina, G. Isella, T. Etzelstorfer, J. Stangl and E. Mller Gubler, *"Si/SiGe Nanoscale Engineered Thermoelectric Materials for Energy Harvesting"*, Proceedings of the IEEE International Conference on Nanotechnology 2012, ThP1T3, 7913 (2012).

D.J. Paul, A. Samarelli, **L. Ferre Llin**, Y. Zhang, J.M.R. Weaver, P.S. Dobson, S. Cecchi, J. Frigerio, F. Isa, D. Chrastina, G. Isella, T. Etzelstorfer, J. Stangl and E. Mller Gubler, *"Si/SiGe Thermoelectric Generators (Invited)"*, Electro- chemical Society Transactions 50(9), pp.959-963 (2012).

A. Samarelli, **L. Ferre Llin**, S. Cecchi, J. Frigerio, T. Etzelstorfer, E. Mller, Y. Zhang, J. R. Watling, D. Chrastina, G. Isella, J. Stangl, J. P. Hague, J. M. R. Weaver, P. Dobson, and D. J. Paul, *"The thermoelectric properties of Ge/SiGe modulation doped superlattices"*, Journal of Applied Physics 113, 233704 (2013).

D. Chrastina, S. Cecchi, J. P. Hague, J. Frigerio, A. Samarelli, **L. Ferre-Llin**, D.J. Paul, E. Mller, T. Etzelstorfer, J. Stangl and G. Isella, *"Ge/SiGe superlattices for nanostructured thermoelectric modules"*, Thin Solid Films (In-press) - DOI: 10.1016/j.tsf.2013.01.002.

L. Ferre Llin, A. Samarelli, Y. Zhang, J. M. R. Weaver, P. Dobson, S. Cecchi, D. Chrastina, G. Isella, T. Etzelstorfer, J. Stangl, E. Mller and D.J. Paul, *"Thermal Conductivity Measurement Methods for SiGe Thermoelectric Materials"*, Journal of Electronic

Materials 42(7), pp 2376-2380 (2013) - DOI: 10.1007/s11664-013-2505-3-z.

A. Samarelli, **L. Ferre Llin**, Y. Zhang, J. M. R. Weaver, P. Dobson, S. Cecchi, D. Chrastina, G. Isella, T. Etzelstorfer, J. Stangl, E. Mller and D.J. Paul, *"Power Factor Characterization of Ge/SiGe Thermoelectric Superlattices at 300*K*"*, Journal of Electronic Materials 42(7), pp 1449 - 1453 (2013) - DOI: 10.1007/s11664-012-2287-z.

S. Cecchi, T. Etzelstorfer, E. Mller, A. Samarelli, **L. Ferre Llin**, D. Chrastina, G. Isella, J. Stangl, J. M. R. Weaver, P. Dobson and D. J. Paul, *"Ge/SiGe Superlattices for Thermoelectric Devices Grown by Low-Energy Plasma-Enhanced Chemical Vapor Deposition"*, Journal of Electronic Materials 42(7) pp. 2829 - 2835 (2013) - DOI: 10.1007/s11664- 013-2511-5.

S.C. Cecchi, T. Etzelstorfer, E. Mller, D. Chrastina, G. Isella, J. Stangl, A. Samarelli, **L. Ferre Llin** and D.J. Paul, *"Ge/ SiGe superlattices for thermoelectric energy conversion devices"*, Journal of Materials Science 48(7), pp. 2829-2835 (2013) - doi 10.1007/s10853-012-6825-0.

L. Ferre Llin, A. Samarelli, S. Cecchi, T. Etzelstorfer, E. Mller Gubler, D. Chrastina, G. Isella, J. Stangl, J.M.R. Weaver, P.S. Dobson and D.J. Paul, *"The cross-plane thermoelectric properties of p-Ge/Si0.5Ge0.5 superlattices"*, Applied Physics Letters 103, 143507 (2013).

D.J. Paul, A. Samarelli, **L. Ferre Llin**, Y. Zhang, J.M.R. Weaver, P.S. Dobson, S. Cecchi, J. Frigerio, F. Isa, D. Chrastina, G. Isella, T. Etzelstorfer, J. Stangl and E. Mller Gubler, *"Prospects for SiGe thermoelectric generators"*, 14^{th} International Conference on Ultimate Integration on Silicon (ULIS) 2013 pp. 5 - 8 (2013) - DOI: 10.1109/ULIS.2013.6523478.

D.J. Paul, A. Samarelli, **L. Ferre Llin**, Y. Zhang, J.M.R. Weaver, P.S. Dobson, S. Cecchi, J. Frigerio, F. Isa, D. Chrastina, G. Isella, T. Etzelstorfer, J. Stangl and E. Mller Gubler, *"Prospects for SiGe thermoelectric generators"* Solid State Electronics (Submitted for publication).

Acknowledgements

First of all, I would like to thank my supervisor, Prof. Douglas Paul. Thanks for giving me the opportunity to collaborate on the Green Silicon project and make this Ph.D possible. Thanks for all your guidance and suggestions, the experience gained working in his group for these three years has helped me to become a better scientist and engineer.

I would also like to thank my second supervisor Dr. Phil Dobson, together with Prof. John Weaver and Dr. Yuan Zhang, for all their helpful suggestions and guidance regarding thermal measurements and thermal analysis. In particular, I would like to thank Dr. Yuan Zhang for the several times I visited her office due to the fruitful discussions and advices that she was always able to give me.

Thanks for the excellent collaboration between all the partners involved in the Green Silicon project. I would like to thank: Dr. Stefano Cecchi, Dr. Giovanni Isella and Dr. Danny Chrastina for growing the heterostructures studied in this thesis; Tanja Etzelstorfer and Prof. Julian Stangl for the X-ray characterisation provided; and Dr. Elisabeth M*ü*ller for performing the TEM characterisation of the multilayer structures. Thanks to you all for creating such a nice, positive and experienced work environment.

A special acknowledgement goes for Dr. Antonio Samarelli. What to say "boss"? Thanks for all the knowledge, discussions, advices and laughs brought during these three years. At first, you were supposed to be as a third supervisor for me, but quickly you became a good colleague to work with and a good friend. Thanks for your spontaneity and for your big support. Grazie Anto.

Thanks to my friends, for your unconditional friendship and for bringing laughs to my life during hard times.

Thanks to the Glasgowegian Kirsty, for her support and the long and funny chats in the office; the sweet Ivon, for being my spanish/mexican connection inside the department and keeping me so sportive in this last period of writing up; the cheerful Leila, who even now that she left Glasgow, is still a close friend that keeps giving me such good advices; the crazy Vasilis, for the many coffee breaks, psychological talks and his many Greek jokes that always made me laugh; the calm Angelos, who always transmitted his serenity; and the friendly Laura, for bringing new fresh air into my life.

To conclude, I would like to thank my brother, and my mum and dad, for their unconditional way of supporting me in any decision I have taken. Thanks for everything you do, for your advices, your patience and love.

Contents

List of Figures

List of Tables

Nomenclature

Acronyms

EH energy harvesting

ICT information and communication technology

TEG thermoelectric generators

CMOS complementary metal oxide semiconductor

MEMS micro-electro-mechanical-systems

Si silicon

Ge germanium

XRD x-ray diffraction

TEM transmission electron microscopy

TBR thermal boundary resistance

QW quantum well

SL superlattice

MBE molecular beam epitaxy

CVD chemical vapour deposition

LEPECVD low energy plasma enhanced chemical vapour deposition

VS virtual substrate

SOI silicon on insulator

TDD threading dislocation density

PF power factor

JWNC James Watt Nanofabrication Center

RIE reactive ion etching

RF radio frequency

CCP capacitive coupled plasma

ICP inductively coupled plasma

SEM scanning electron microscope

PECVD plasma-enhanced chemical vapour deposition

ICP-CVD inductively coupled plasma chemical vapour deposition

TCR temperature coefficient of resistance

dc direct current

AFM atomic-force-microscopy

ThAFM thermal atomir-force-microscopy

TLM transmission line method

CTLM circular transmission line method

MQW multi quantum-well

HRXRD high-resolution x-ray diffraction

Greek Symbols

α Seebeck coefficient

σ electrical conductivity

κ thermal conductivity

μ mobility

ρ resistivity

ρ_c contact resistivity

Other Symbols

ZT figure-of-merit

κ_e electronic thermal conductivity

κ_L phonon thermal conductivity

n carrier concentration

2DEG 2 dimensional electron gas

$\mathbf{Si_3Ni_4}$ silicon nitride

$\mathbf{SiO_2}$ silicon dioxide

$\mathbf{R}_c$ contact resistance

$\mathbf{R}_{sh}$ sheet resistance

Chapter 1

Introduction

The increasing demand for energy has generated a climate change on the planet that has made it necessary to identify new strategies to improve energy use [25]. Energy harvesting (EH) has become an interesting field to take advantage of energy that is released to the environment in order to make a more effective use of it. The environmental discussion of energy harvesting does not consist solely in replacing high power energy sources and their addition to pollution but it considers the use of power electronic devices for other kinds of environmental savings. As an example, EnOcean described how after installing 4,200 energy harvesters to power light switches, occupancy sensors and daylight sensors in a new building, they had saved 40% of lighting energy costs, 20 miles in cables and 42,000 batteries (over 25 years) and as a consequence had reduced the amount of toxins released by batteries to the environment [25]. Information and communication technology (ICT) is not only deployed in building controls but also in the automotive sector and processing plants where using complete autonomous systems is essential in environments with difficult access or with hazardous risks.

Thermoelectric devices are able to deliver electricity to a load using heat as a power source or to produce heating or cooling in presence of an electrical current. The Seebeck effect converts thermal energy into electrical energy, making these devices suitable for EH in systems where the energy is released to the environment as wasted heat. In addition to sustainable energy generation, thermoelectric generators (TEGs) can be easily scaled to satisfy the increasing miniaturization demanded of sensors and modules nowadays.

Currently, commercial TEGs that work mainly around room temperature are made of telluride based materials presenting an 18% Carnot efficiency and a maximum power output of 2.8 mW [26]; enough energy to power a commercial sensor. However, tellurium is one of the rarest elements on the earth and hence the increased interest in using new materials with similar or improved efficiencies as an alternative. Furthermore, telluride technology is not compatible with complementary metal oxide semiconductor (CMOS) and micro-electro-mechanical-systems (MEMS) processing.

Silicon (Si) and germanium (Ge) materials have shown an increasing attraction for energy harvesting, due to their sustainability and complete integrability with CMOS and MEMS technology. However, the thermoelectric efficiencies for these materials are very poor when working at room temperature and hence the necessity to engineer them in order to compete and be cost effective for a consumer market.

This thesis presents new engineered silicon and germanium materials whose thermoelectric properties will be explored to improve their efficiencies. The vision is to produce optimised thermoelectric generators that can compete with the present ones, with the beneficial addition of integrability with CMOS technology. Testing and characterisation techniques shall be developed in the course of this work to provide a complete feedback on the materials presented.

Next, the scope and the structure of this thesis is explained, highlighting the main objectives and giving a brief description of the content of each chapter.

1.1 Aims of the Thesis

This work was part of the *GreenSi* project aimed at turning heat into electricity using micro-fabricated devices. GreenSi was supported by the European Commission through the ICT FET-Proactive Initiative Towards Zero Power.

The material of choice was Si-Ge due to the already mentioned advantages. The main application that GreenSi was looking for, was to use the optimised generator as an energy harvester that would work at room temperature to power a commercial sensor with a standard power input of 3 mW.

The partners involved in the project included: the Politecnico di Milano, the Johannes Kepler University of Linz, ETH Zurich and University of Glasgow.

Prof. Douglas Paul head of the project, performed all the different modelling to provide band-structure analysis. The material was grown at Politecnico di Milano at L-Ness of Como and x-ray diffraction (XRD) and transmission electron microscopy (TEM) analysis were performed by the Johannes Kepler University of Linz and ETH Zurich, respectively. On the other hand, Dr. Yuan Zhang provided the finite element analysis (FEM) of some of the devices presented in this thesis. Therefore, it has to be pointed out that all the design modelling and physical characterisation presented in this thesis were provided by the institutions mentioned above. Even though, these tasks were not part of my direct work, it was considered appropriate to present part of it for a better understanding of the analysis done in the course of this thesis.

My activity in the project consisted in performing the device design and fabrication, and the thermoelectric characterisation and analysis of the different materials supplied to University of Glasgow. Therefore, the aim of my Thesis consisted in studying the different parameters that could contribute to improve the efficiency of single n- and p-type materials so that future Si-Ge generators could be performed.

The materials supplied, superlattices which were between 4 and 10 μm thick, had a strong anisotropic behaviour and so I had to develop consistent and reproducible testing devices and characterisation techniques to estimate cross-plane and in-plane properties. Even though the main application of the project was to create energy harvesters for room temperature operation, the thermoelectric properties were also investigated at higher temperatures for other possible applications. The specific aims of this work are detailed next:

- To develop the fabrication of test devices for in-plane and cross-plane evaluation of material efficiency.
- To develop characterisation techniques that will allow extraction of thermal information from the test devices.
- To develop characterisation techniques to extract the cross-plane electrical properties of materials at room temperature.

- To apply the characterisation techniques to analyse the thermoelectric properties of materials as a function of layer thicknesses, Ge content and doping density.
- To study a new method to scatter phonons in the cross-plane direction, aiming for lower thermal conductivities.

Next is summarised the content presented in each chapter.

Chapter 2 gives an introduction to thermoelectricity, explaining how low-dimensional structures can enhance the efficiency and the power output in comparison to 3-dimensional systems.

Chapter 3 begins with an overview of heterostructures and follows with a description of the two main carrier transport phenomena dominating the heterostructures studied. The chapter then focuses on the strain concerns when growing Ge/SiGe heterostructures, highlighting the main available epitaxial growth techniques and extending to the specific one used within the GreenSi project.

Chapter 4 provides a description of device fabrication and the characterisation techniques used to analyse the different thermoelectric properties. The Chapter divides into two main sections: the first one describes the optimized processes used to fabricate the final devices and the second one focuses mainly on the thermal but also on the electrical techniques involved in the characterisation.

Chapter 5 describes the work done to characterise the in-plane properties of the heterostructures. The chapter first gives a description of the designs that have been studied and some of the physical characterisation performed on those designs. Then, it follows with the processes used to fabricate lateral devices and then presents the thermoelectric characterisation, pointing out the main findings and limitations for lateral designs.

Chapter 6 summarises the work done to characterise the cross-plane properties of the heterostructures. The chapter starts with the presentation of the different designs, explaining the key-points. A physical characterisation of some of the designs is shown, which is then followed by the fabrication involved to perform cross-plane device testing. The remainder of the chapter presents the thermoelectric characterisation results and conclusions.

Chapter 7 describes experiments done to analyse a set of n-type vertical device designs. The chapter presents the designs and the two experiments performed. Physical

characterisation plus modifications adopted to the fabrication of the tested devices are also introduced. The remainder of the chapter splits the results and conclusions obtained for these two experiments.

Chapter 8 highlights the achievements obtained in this work, specifically an overview of the main findings regarding the lateral and the vertical designs studied. To conclude, a section suggesting further work is presented.

Chapter 2

Introduction to Thermoelectric Effects

Thermoelectricity involves the direct conversion between thermal and electrical energy [27]. The Seebeck effect, Peltier effect and Thomson effect are the common ways to exploit thermoelectricity; the Seebeck effect being responsible for power generation.

- Seebeck effect: In 1821, T. J. Seebeck demonstrated that when two electrical conductors were brought together, and the junction between them was heated up, a small voltage reading could be sensed. This effect (α) was defined as the ratio between the voltage sensed (ΔV) and the existent gradient of temperature (ΔT), as defined in Equation 2.1.

$$\alpha = \frac{\Delta V}{\Delta T} \tag{2.1}$$

- Peltier effect: Thirteen years later, in 1834, J. Peltier discovered that when an electrical current was driven through a thermocouple a small heating or cooling was produced depending of the direction of this current. It was defined as the ratio between the heating or cooling rate at each junction (q) and the current passing through it (I), as defined in Equation 2.2:

$$\pi = \frac{q}{I} \tag{2.2}$$

- Thomson effect: In 1855, W. Thomson recognised the relation between the two effects explained above. This effect showed the reversible heating or cooling when there was an electrical current flowing in addition to a gradient of temperature. The relation between the Seebeck and the Peltier effect was given by

$$\pi = \alpha T. \tag{2.3}$$

  The Thomson effect (τ) was defined as the rate of heating or cooling per unit length through a junction, where here existed a unit current and a unit gradient of temperature. This effect was also related to the Seebeck effect by

$$\tau = T\frac{d\alpha}{dT}. \tag{2.4}$$

All these effects were demonstrated by the use of thermocouples at the time. In the 1950s the study of semiconductor materials became very interesting for the construction of thermoelectric generators, as well as practical Peltier coolers.

As it is the Seebeck effect that is responsible for power generation, a more detailed explanation of it is given in the following sections, as well as other parameters which define the efficiency of a thermoelectric system. Following this definition, a review of the different materials and approaches used during the past and present years to achieve improvements in the Seebeck coefficient are reported.

2.1 Thermoelectric Power Generation

Let us consider a pair of legs (p-type and n-type) connected electrically in series and thermally in parallel. If one side of the pair of legs is heated up and the other side is kept at a reference temperature, the ΔT between the two legs produces excess carriers which may diffuse from the hot to the cold side. This diffusion of carriers sets the Seebeck voltage which will deliver a current (I) when the circuit is closed with a load, as shown in Figure 2.1.

The efficiency of the system (η) is given by the ratio of the output power to the rate of the heat that is drawn from the source, $\eta = \frac{w}{q}$. The current flowing through the circuit is given by

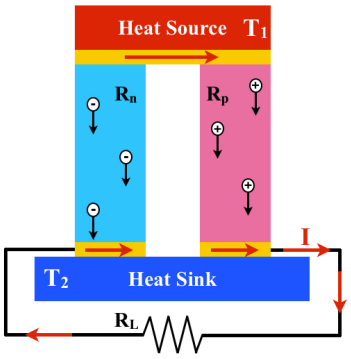

Figure 2.1: Schematic diagram of a module formed by a pair of legs connected electrically in series and thermally in parallel. The circuit has been closed, connecting a resistor across the module.

$$I = \frac{(\alpha_p - \alpha_n)(T_1 - T_2)}{R_L + R_p + R_n}, \tag{2.5}$$

where R_p and R_n are the resistances of each semiconductor material (p-type and n-type), R_L is the resistance of the load and, α_p and α_n are the Seebeck coefficients of each leg [28]. The power delivered to the load resistor is given by Equation 2.6 [28].

$$w = \left(\frac{(\alpha_p - \alpha_n)(T_1 - T_2)}{R_L + R_p + R_n} \right)^2 R_L \tag{2.6}$$

On the other hand, the heat that is drawn from the source is defined by

$$q = (\alpha_p - \alpha_n) I T_1 + (\kappa_p + \kappa_n)(T_1 - T_2), \tag{2.7}$$

where κ_p and κ_n are the thermal conductances of the two legs [28].

The efficiency reaches its maximum when [28]:

$$\frac{R_L}{R_n + R_p} = \sqrt{1 + ZT} \quad where \quad ZT = \frac{\alpha^2 \sigma}{\kappa} T, \tag{2.8}$$

where $\sigma = \sigma_n + \sigma_p$ (S/m) is the electrical conductivity, $\alpha = \alpha_p - \alpha_n$ $(\mu V/K)$ is the Seebeck coefficient and $\kappa = \kappa_p + \kappa_n$ $(W/m \cdot K)$ is the thermal conductivity of the material.

Using Equation 2.8 in Equations 2.6 and 2.7, the efficiency can be defined by the following expression [28]:

$$\eta = \frac{T_1 - T_2}{T_1} \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+\frac{T_2}{T_1}}. \tag{2.9}$$

From the efficiency it is shown that if ZT is much larger than unity, the model approaches the Carnot efficiency given by $(T_1\text{-}T_2)/T_1$. Figure 2.2 shows the efficiency given for different values of ZT, where the system approaches the Carnot efficiency each time the value of ZT becomes larger. Therefore, ZT is known as the figure of merit that defines the efficiency of a thermoelectric material.

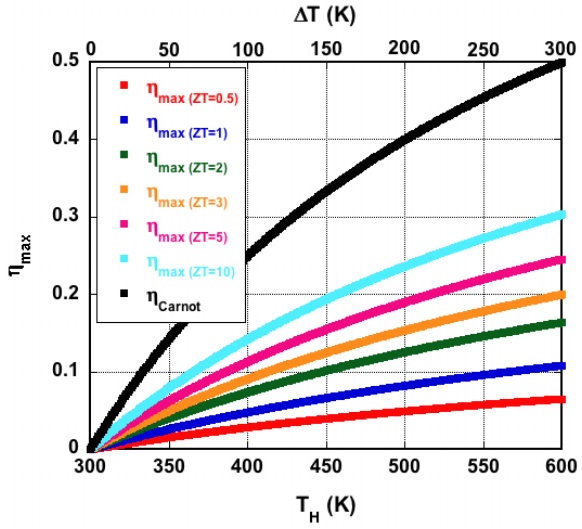

Figure 2.2: Plot showing the maximum thermoelectric efficiency for different ZT values. These values have been compared to the Carnot efficiency, also plotted in the figure.

Until now we have only considered two legs connected to a load but a real thermoelectric generator (TEG) features several of these thermoelectric couples electrically connected in series. Figure 2.3 *c*) shows a diagram of a full module where several thermoelectric couples are connected electrically in series and thermally in parallel. Figure 2.3 *a*) and *b*) shows two scanning electron microscope (SEM) images of 4 μm thick p-type and n-type legs prior to bonding.

Getting the maximum efficiency out of a module does not mean generating the maximum power output, in fact the power output reaches its maximum when R_L=R_n+R_p. Taking this into account, and using the relation given by Equation 2.6, one gets that P_{max} is defined by

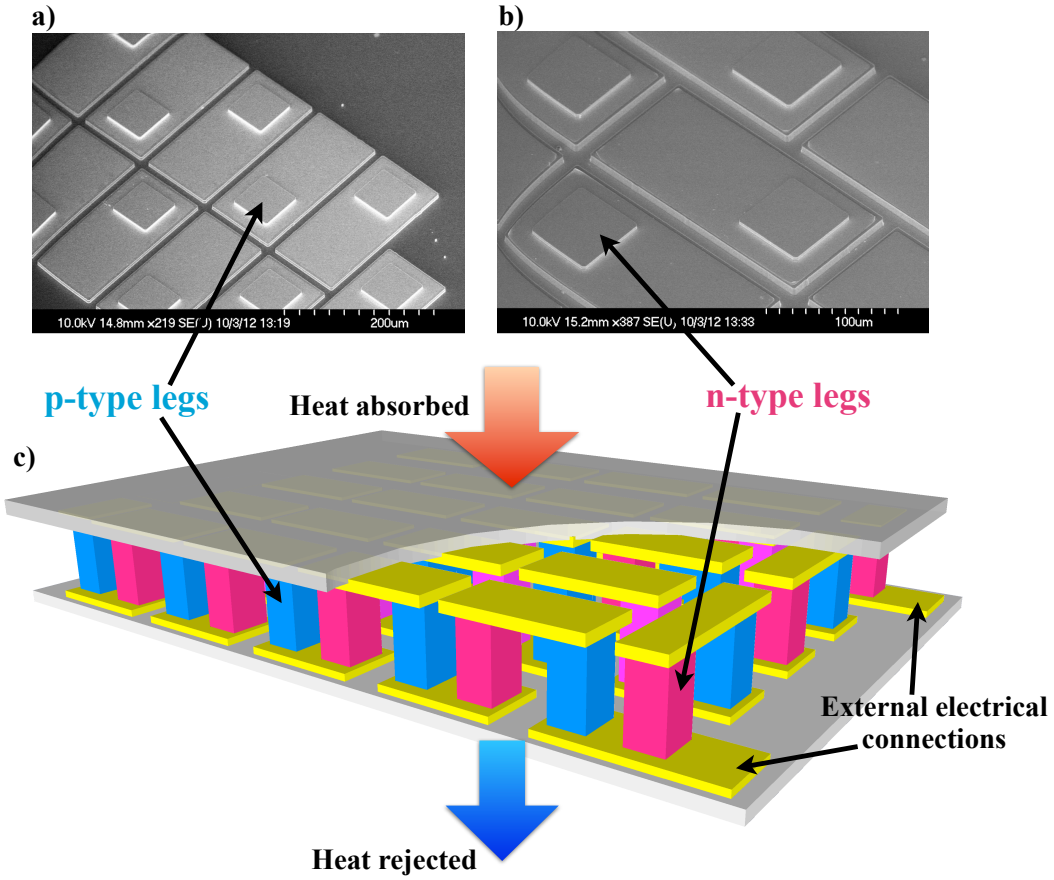

Figure 2.3: Figures *a*) and *b*) show two SEM images of 4 μm thick p-type and n-type legs, respectively. In these images the top and bottom contacts to the legs had already been patterned, but not the bonding pads. *c*) Schematic diagram of a thermoelectric module where the p-type and n-type legs have been bonded together, connecting them electrically in series and thermally in parallel.

$$P_{max} = \frac{1}{2} N F \frac{A}{L} \Delta T^2 \alpha^2 \sigma, \tag{2.10}$$

where N is the number of legs, F is the fabrication factor and A and L are the area and the length of the legs respectively [27]. The fabrication factor denotes the perfect system, where there are not losses of any kind, to account for contact resistances and wasted heat.

When characterising a material, apart from its efficiency, it is also important to consider separately the relation $\alpha^2\sigma$. This is the second figure of merit of a thermoelectric material and represents the output power of the system, also known as the *Power Factor*.

2.1.1 Applications for Power Generation

Thermoelectric generators are robust, do not have moving parts, do not require maintenance and can generate continuous power as long as there is a heat source. Therefore, this technology is an attractive way to recover wasted heat rejected into the enviorement.

Thermoelectric generators can be used over a wide range of temperatures, which makes them useful in many different systems. In the following list, there are mentioned some of the applications where thermoelectric generators are currently used or are under investigation.

- Low-temperatures (Room Temperature Applications):
  - Implantable medical devices have the disadvantage of depending on batteries, with life times ranging from 5 to 10 years. These devices could be powered by using temperature differences that exist between the inner surface of the skin and the core body. A thermoelectric module generating around 70 μW in the presence of these temperature gradients could be useful in these applications [29].
  - Wireless sensors are autonomous devices combining sensing, power, computation and communication into one system; smartdust has become a term to refer to these kind of sensors. In order to create a complete autonomous system the batteries to power those sensors could be replaced by energy harvesters. In fact, when working with compatible materials for CMOS micropower circuits and MEMS processing, these energy harvesters could be integrated within the semiconductor fabrication of such devices, allowing smaller dimensions.
- High-temperatures (Industrial Applications):
  - In cars, 40% of the efficiency is lost to the environment as wasted heat through the exhaust. Part of this wasted heat could be converted into electricity decreasing the fuel consumption [27].
  - Power-plants are investigating the possibility of converting part of the heat wasted through the condenser into electricity in order to heat up some fluids, which need to go from 30 to 300°C, en-route to the next step of the system.

– Due to the absence of vibration, noise or torque during operation, thermoelectric generators are suitable systems for powering space missions [27].

2.2 Materials for Thermoelectric Generators

Most of the thermoelectric modules commercially available are dominated on the material side by n-type and p-type alloys $(Bi, Sb)_2(Te, Se)_3$. As an example, Micropelt is building modules of 8000 p-n couples per cm^2 using 10 μm long legs from n-$Bi_2(Se, Te)_3$ and p-$(Bi, Sb)_2Te_3$ alloys [30], giving a maximum power output of 2.8 mW with a $\Delta T = 10$ K suitable for energy harvesters for powering sensors [26].

Tellurium (Te) is the 9^{th} rarest element on the earth, which makes it less sustainable for large scale production. Moreover, these alloys present their highest performance when working at room temperature. For high temperature applications (above 900°C) telluride compounds are not used due to their low ZT value; silicon-germanium (SiGe) alloys have a better performance for high temperature power generation. Figure 2.4 shows the value of ZT, as a function of temperature for different thermoelectric materials. From Figure 2.4, it can be seen that the ZT values reported for SiGe (n-type and p-type materials) at room temperature are below 0.1.

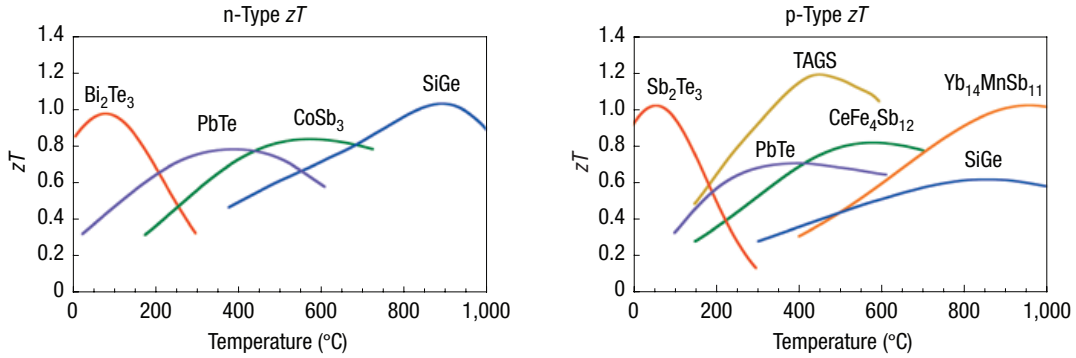

Figure 2.4: Figure of merit for commercial materials, n-type and p-type, as a function of temperature [1].

Table 2.1 shows a comparison between n-type and p-type telluride alloys (as used in commercial micro-generators) with Si and Ge bulk materials for similar doping concen-

trations and at 300 K. The electrical properties for Si and Ge are not so different to the commercial micro-generator ones, allowing large power factor values. On the contrary, these materials have larger thermal conductivities that produce poor values for ZT. If κ was reduced, then Si-Ge materials could compete with tellurides when working at room temperatures.

Material (300 K)	**N** ($\mathbf{cm^{-3}}$)	ρ ($\Omega\cdot\mathbf{m}$)	α ($\mu\mathbf{V/K}$)	κ ($\mathbf{W/m\cdot K}$)	**ZT** (300 K)
n-Bi_2Te_3 [31]	-	1.6x10^{-5}	-160	2.0	0.240
n-Si [32]	1.0x10^{19}	6x10^{-5}	-95	148	0.00031
n-Ge [33]	1.1x10^{19}	1.5x10^{-5}	-308	59.9	0.032
p-$(BiSb)_2Te_3$ [31]	-	1.2x10^{-5}	175	2.0	0.375
p-Si [32]	1.5x10^{19}	9.0x10^{-5}	148	148	0.00049
p-Ge [34]	1.0x10^{19}	2.8x10^{-5}	280	59.9	0.014

Table 2.1: A comparison between n-type and p-type telluride alloys (commercial micro-generators) with Si and Ge bulk values at 300 K.

SiGe alloys already present reduced thermal conductivities when compared with their bulk counterparts. These values could be tuned by changing the Ge concentration of the alloy and the doping concentration as in [14]. Unfortunately, as shall be explained later in Section 2.3, improving one thermoelectric parameter for bulk materials normally results in degrading another one, making it very difficult to optimize the figure of merit.

The total thermal conductivity is a contribution of the electronic and the phonon thermal conductivities, $\kappa = \kappa_e + \kappa_L$. For bulk materials the Wiedemann-Franz law provides a limit to the maximum ZT that can be achieved, as electronic and thermal conductivities are linked by this law [27, 35].

Low-dimensional structures can be engineered to improve the thermoelectric performance of materials by de-coupling the connection between κ, σ and α [36, 37], refer to Section 2.4 for more details.

Two, one and zero dimensional structures have been studied in order to achieve higher efficiency materials. For telluride based materials, Venkatasubramaniam [24] reported an improved ZT at 300 K of 2.4 for p-type Bi_2Te_3/Sb_2Te_3 and a ZT of 1.4 for n-type

$Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ superlattices. The ZT value for the p-type superlattice was increased by a factor of 2 over its alloy counterpart [24]. This improved ZT was mainly due to the reduction of the thermal conductivity value by a factor of 2.2 compared to the $Bi_{0.5}Sb_{1.5}Te_3$ alloy [38]. In 2005 [29] a thermoelectric generator constructed from these superlattices, which presented 30 number of couples in an area of $0.16\,\mathrm{cm}^2$, was built and tested, featuring an output power of $980\,\mu\mathrm{W}$ with a $\Delta T = 2.7\,^{\circ}\mathrm{C}$.

The same approach has been followed to reduce the thermal conductivity for silicon and germanium materials. SiGe superlattices have been proved to produce lower thermal conductivities than their alloy counterparts. Work done in [39, 40, 41, 42, 43] agreed with a cross-plane thermal conductivity value of $\sim$ $2.5\,\mathrm{W/m\cdot K}$ at $300\,\mathrm{K}$ for symmetrically strained SiGe superlattices, which showed a factor of 5 times reduction compared to their alloy counterparts. Yang [39] reported an in-plane value at $300\,\mathrm{K}$, 5 times higher than the cross-plane one, suggesting that the thermal conductivity along the plane is very similar to the alloy value. Yang also studied the anisotropy of the superlattice for σ and α, finding a ratio of 5 for the electrical conductivity ($\sigma_{in-plane}/\sigma_{cross-plane} = 5$) and an almost isotropic behaviour for the Seebeck coefficient at room temperature. Ge quantum dots have also proved to reduce the thermal conductivity down to $10\,\mathrm{W/m\cdot K}$ at $300\,\mathrm{K}$ for cross-plane measurements, although the in-plane value quoted was still 3 times higher [40].

1D SiGe alloy and Si nanowires have shown a ZT of ~ 0.2 at $300\,\mathrm{K}$ [44, 45]. In [45] an increased value for ZT of ~ 1 at $200\,\mathrm{K}$, for $20\,\mathrm{nm}$ diameter Si nanowire with p-type doping of $7x10^{19}\,\mathrm{cm}^{-3}$, was shown. This high ZT was due to the low κ value measured, that was comparable to the thermal conductivity of bulk silica $1.4\,\mathrm{W/m\cdot K}$ [46], and the high value measured for α reaching almost $400\,\mu\mathrm{V/K}$ due to phonon drag effects [47].

As noted above, most of the research done to improve the efficiency of thermoelectric materials has been focused in reducing the thermal conductivity. Another way to increase the value of ZT is by increasing the numerator of the figure of merit. This also has a beneficial effect on the other figure of merit which is the power factor. Since most of the work presented in the literature is focused on the reduction of κ, most of the results available for low-dimensional systems show increase ZT values compared with their alloy counterparts, but similar or even lower PF values [15, 48, 49].

Working in low dimensions brings the possibility to modify α, σ and κ almost independently due to the new variable of length scale which allows quantum-confinement effects. This fact has been already demonstrated in [50, 51, 52, 53] and it is discussed in Section 2.4 but, the current research requires a better understanding of carrier transport as well as the still necessary compromises between the three parameters to get a maximum ZT and a maximum PF [15].

In the following two sections, a review of the three thermoelectric parameters is provided for 3D and 2D systems, supporting the description with theoretical equations for a better understanding of the limitations and improvements given by the two systems.

2.3 Thermoelectric Parameters in 3D Semiconductors

An ideal thermoelectric material should behave as an electrical conductor, a thermal insulator and should also have a large Seebeck coefficient. For metals and degenerate semiconductors, the Seebeck coefficient can be defined as a function of carrier concentration (n) and the effective mass of the carrier (m^*):

$$\alpha = \frac{8\pi^2 k_B^2}{3eh^2} T m^* \left(\frac{\pi}{3n}\right)^{2/3}, \tag{2.11}$$

where k_B is the Boltzmann constant, h is the Planck constant and e is the elementary charge [1]. The electrical conductivity can also be defined as a relation of the carrier concentration and the mobility (μ) [1]:

$$\sigma = ne\mu. \tag{2.12}$$

From Equation 2.11, one can see that a low carrier concentration gives a large Seebeck coefficient, but at the same time this can decrease the electrical conductivity as it is also related to n [54]. A high effective mass for the carrier provides higher α, but this could create another conflict with σ, as heavier carriers move with slower velocity and therefore with smaller mobilities.

On the other hand, κ is defined by the addition of two parameters, the lattice (κ_L) and the electronic (κ_e) contributions to the thermal conductivity. The electronic term is related to the electrical conductivity through the *Wiedemann Franz law*, defined by:

$$\kappa_e = L\sigma T, \tag{2.13}$$

where, L is the Lorenz factor [55]. In metals this factor is equal to the Lorenz number which is also used as a first approximation for thermoelectric semiconductors ($L = \pi^2 k_B^2/3q^2$). Therefore, getting a maximum value for ZT is directly linked to this law for 3D materials, where the only way to reduce the thermal conductivity is by reducing the lattice contribution.

Improving one thermoelectric parameter could mean the decline of other one, resulting in a poor value of ZT and of PF. As an example, Figure 2.5 shows the behaviour of the thermoelectric parameters for Bi_2Te_3 as a function of the carrier concentration, showing the relation between α, σ and κ.

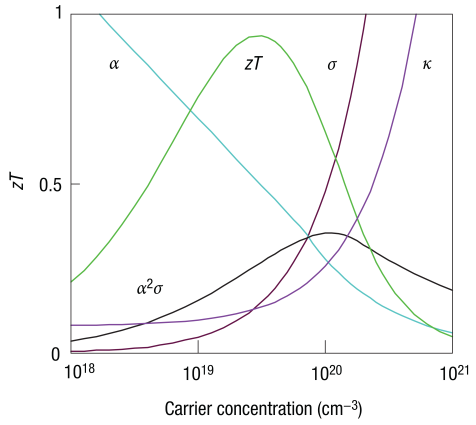

Figure 2.5: Thermoelectric parameters plotted as a function of the carrier concentration for Bi_2Te_3 [1].

Due to the limitations of bulk materials, researchers have put a lot of interest for the last 20 years to improve the value of ZT using low dimensional structures. First, theoretical predictions made by Hicks and Dresselhaus [35], showed that 2D multilayered structures could increase the value of ZT due to quantum confinement effects. Three years

later they demonstrated experimentally these predictions in [50], where an improvement by a factor of 4.1 for a multi-quantum well structure was obtained in comparison with its bulk counterpart. Moreover, having a multilayer structure could help to scatter phonons at the interfaces decreasing the lattice thermal contribution κ_L [56], and therefore decreasing the total value of the thermal conductivity only when this is not dominated by κ_e due to the Wiedemann-Franz law (Equation 2.13).

The work developed within this thesis focuses in 2-dimensional systems, studying the anisotropic thermoelectric properties of multi-quantum well structures. How to enhance the thermoelectric properties for low-dimension structures, more in detail for 2D structures, is discussed in the following section.

2.4 Thermoelectric Parameters in Low-Dimensional Structures

In low-dimensional materials the addition of a new degree of freedom, such as the length scale of a material, can contribute to an increase in the efficiency and power output of the system by de-coupling σ from α and κ. To explain this, we can refer to the Seebeck coefficient derivation made by M. Cutler and N. F. Mott in 1969 [57]. This relation (Equation 2.14) simplified for metals and degenerate semiconductors, shows that the Seebeck coefficient could be enhanced by increasing the energy dependence of the electrical conductivity.

$$\alpha = \frac{\pi^2}{3}\frac{k_B^2}{q}T\Big\{\frac{d[ln(\sigma(E))]}{dE}\Big\}_{E=E_F} \tag{2.14}$$

This could be achieved by enhancing the density of carriers $(dn(E)/dE)$, which is a function of the density of states $(dg(E)/dE)$, or by enhancing the differential mobility $(d\mu(E)/dE)$ or relaxation time $(d\tau(E)/dE)$, see Equation 2.15 [58].

$$\sigma(E) = n(E)e\mu(E) = n(E)e^2\frac{\tau(E)}{m^*} \tag{2.15}$$

The first effect to enhance the density of states could be potentially achieved by working with low-dimensional structures. Figure 2.6 shows the energy dependence of the density of states from bulk materials (3D systems) to 2D, 1D and 0D systems (from left

to right). Referring to Equation 2.14, one can see in Figure 2.6 that the larger asymmetry in low-dimensional systems, compared to the 3D systems (bulk material), could enhance substantially the α value, provided it is around the Fermi energy level.

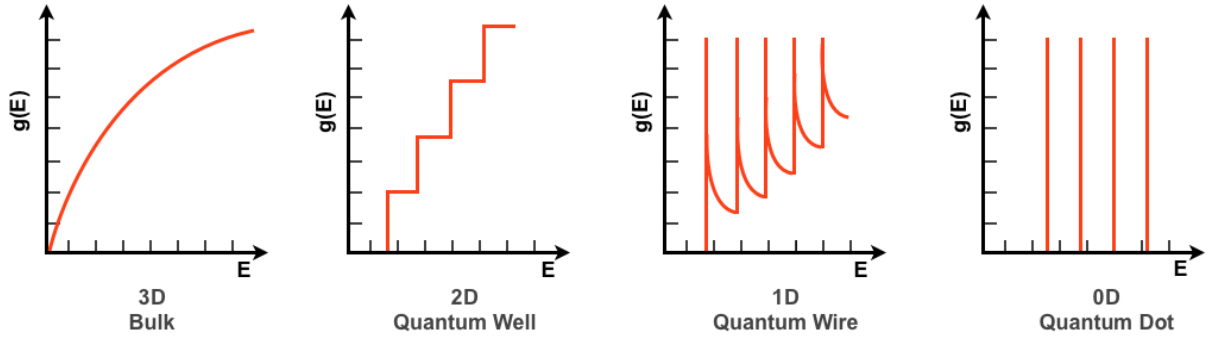

Figure 2.6: Schematic diagram for the energy dependence of the density of states for 3D, 2D, 1D and 0D systems (from left to right).

For a multi-quantum well structure (2D system), this phenomena was first introduced by Hicks and Dresselhaus [35, 50]. They demonstrated in 1996 [50] an improvement in the Seebeck coefficient over the bulk system by studying its enhancement as a function of carrier concentration and quantum well width.

On the other hand, the second effect to increase the carrier mobilities at a given carrier concentration, could be promoted by electron energy filtering [59, 60] or by using δ-doping [61]. In a 2D system electron energy filtering consists of using potential energy barriers, that can filter electrons according to their energy band, promoting thermionic current emission. In [52] it is demonstrated that at room temperature an increased in ZT by a factor of 10 in $In_{0.53}Ga_{0.47}As/In_{0.53}Ga_{0.28}Al_{0.19}$ superlattices compared to their bulk counterpart can be achieved, where 65% of the increment was due to electron filtering and the remaining 35% was due to a reduced thermal conductivity. Furthermore, the authors in [52] reported that electron filtering allowed higher doping densities for increased Seebeck coefficients and therefore achieving higher power factors.

Multi-quantum well structures give the possibility of using δ-doping to promote higher electrical conductivities due to higher mobilities [5, 62]. More details of this doping technique are reported in Section 3.1.4.

2.4.1 Thermal Conductivity

While the power factor is related to the electrical properties of the material, the efficiency is highly influenced by the thermal conductivity value. The thermal conductivity (κ) is the ability of a material to conduct heat. The lattice contribution to the thermal conductivity (κ_L) is related to the elastic vibrations of the lattice, also known as phonons. In the presence of a temperature gradient, the propagation of heat flux can be considered as the propagation of vibrational waves or phonons. There are two different kind of phonons, these are optical and acoustic phonons. Optical phonons represent atoms in a unit cell moving in opposite phase, presenting small group velocities, while acoustic phonons move in the same phase, presenting larger group velocities and therefore being the main contributors to the heat transport [63].

Inside bulk materials phonons can be scattered by impurities and by crystal defects. The lattice contribution to the thermal conductivity can be defined as

$$\kappa_L = \frac{1}{3} c_v v l_t, \tag{2.16}$$

where c_v is the specific heat per unit volume due to the lattice vibrations, v is the speed of sound and l_t is the mean free path of the phonons [28]. As the temperature rises, the thermal vibrations become more and more anharmonic, and as a consequence the mean free path of the phonons varies as 1/T. This phenomena was introduced by Peierls [64] and it was explained under the name of umklapp (or U-) processes. Peierls showed that the phonon scattering events, where the momentum is not conserved, resulted in an increase of the thermal resistivity and therefore a decrease of the thermal conductivity. On the contrary, the normal (or N-) processes where the momentum is conserved after the phonon-phonon scattering process, did not contribute to an increase in the thermal resistance.

As is reported in Section 2.2, many studies have demonstrated that the thermal conductivity of a superlattice can be much lower than the value measured from its bulk material constituent and from its equivalent composition alloy [56]. Phonons waves are normally scattered by impurities and crystal defects, but they can also be strongly scattered at surfaces and interfaces, as in the case of superlattices. By engineering the interfaces and the mismatch of the phonons at the different layers, a reduction in the phonon

group velocity can be produced [56, 65, 66, 67, 68, 69], resulting into the reduction of the thermal conductivity value.

Superlattices present an anisotropic behaviour, with a different thermal conductivity from the in-plane to the cross-plane direction. For in-plane values, phonons are reflected by smooth interfaces creating efficient channels to transfer the heat along the layers and so the in-plane thermal conductivity in superlattices do not differ much from their bulk counterparts [63]. On the contrary, cross-plane values tend to be 4 times smaller than thermal conductivity values along the layers [41, 49]. Both the experiments and theories for these two directions are very different, that is why they need to be considerate separately.

In the following section the reduction of the thermal conductivity values perpendicular to the layer is discussed in more detail, as a key parameter to increasing the efficiency of a material.

2.4.1.1 Perpendicular to the Superlattice: Cross-plane Direction

When heat travels between two materials, a temperature step is developed at the interface which is proportional to the heat flow [63, 68]. This temperature drop is known as thermal boundary resistance (TBR). Inside a superlattice the heat travels perpendicular to a periodic array of interfaces and therefore the TBR addition at each interface contributes to the total thermal resistance of the structure [56, 65, 68, 70]. This effect has been demonstrated in [70] where the thermal resistance of Si/SiGe superlattices is increased for samples with a larger number of periods.

As a second option, the use of phonon bandgap structures for specific phonon energies, may be used to block acoustic phonon transport in superlattice structures. This idea was first introduced by [71], they demonstrated that only phonons at certain wavelengths could pass through the superlattice. As explained by Hyldgaard [66], when there is a finite acoustic mismatch difference in material sound velocities total reflection of phonons arises, eliminating the phonon flux across the interface. This is expected to reduce the

perpendicular group velocity rising to a modal confinement. This approach has been experimentally proved for SiGe and BiTe superlattices [24, 72].

Figure 2.7 [2], shows the cumulative contribution to the heat transport of the acoustic phonon wavelengths for Si and Ge at 300 K. The figure suggests that to achieve an efficient reduction in the phonon transport it is necessary to design superlattice structures featuring barriers thicknesses between 1.2 and 3 nm. This range of wavelengths could block the 95% of the heat transferred by acoustic phonons, potentially reducing the thermal conductivity value.

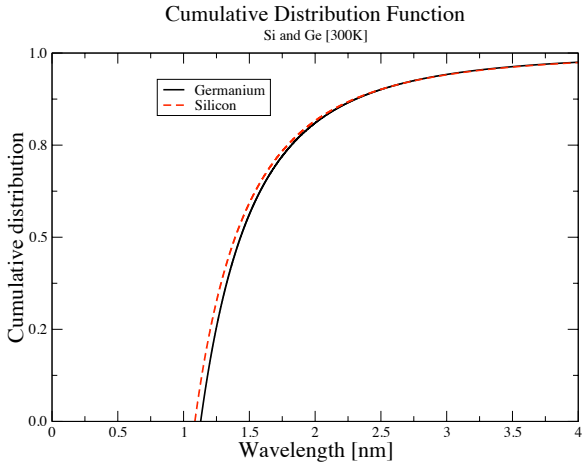

Figure 2.7: Cumulative contribution to the heat transport of acoustic phonon wavelengths for Si and Ge at 300 K [2].

Phonon bandgap structures, following the suggestions described above, are studied within this work. The different designs, thermal conductivity results and conclusions are described in Chapter 7.

2.5 Chapter Summary

Thermoelectric materials have the ability to transform thermal energy into electrical energy. The responsible for thermoelectric power generation is the Seebeck effect which has become a very attractive technology to harvest wasted energy that is released to the environment in many systems.

Currently, the thermoelectric power generation market is dominated by telluride-based materials due to its high working efficiency at room temperature. Nevertheless, Te is a rare and unsustainable material and hence the high interest in finding new alternatives to replace those materials. The thermoelectric properties of Si, Ge and $Si_{1-x}Ge_x$ alloys have demonstrated low efficiencies as power generators at room temperatures and hence the necessity of engineering those materials into low-dimensional structures to enhance their efficiency. Improving a thermoelectric parameter may substantially deteriorate other ones, hence the importance of studying the overall impact of any change.

In particular, 2D structures such as superlattices could be engineered to enhance the Seebeck coefficient due to the larger asymmetry in the density of states, to enhance the electrical conductivity by reducing ionized impurity scattering and reducing significantly the thermal conductivity by increasing the phonon scattering rates at the heterointerfaces and blocking phonons with different wavelengths.

Thin films usually present an anisotropic behaviour and so the in-plane (presented in Chapter 5) and the cross-plane (presented in Chapter 6 and 7) properties of the superlattices should be studied separately to accurately calculate the efficiency and power output of a thermoelectric structure.

Chapter 3

Material: Silicon-Germanium Superlattices

One possible advantage of using Silicon-Germanium materials to build thermoelectric generators is the possibility of integrating this technology with the Si platform which has dominated the semiconductor industry due to the low cost and the mature technology.

This chapter presents a brief introduction to heterostructures and details the two main carrier transport phenomena important to the heterostructures studied. Strain, dislocations and virtual substrates will be introduced, together with the different epitaxial growth techniques available. LEPECVD growth techniques will be described in detail as this was the method of choice for producing the different wafers micro-fabricated and characterised in the course of this work.

3.1 Quantum Transport

In 1924, Louis de Broglie introduced the idea of a particle behaving in the same way as a wave, relating the wavelength (λ) with the momentum of a particle p by

$$\lambda = \frac{h}{p}, \tag{3.1}$$

where h is the Planck constant [4]. In this way, the position of a particle (r) can be described as the motion of a wave with time (t), an angular frequency (ω), and with a wavevector (k). The motion of a harmonic wave is defined by the wavelength of a particle:

$$\psi(r) = e^{i(kr-\omega t)}, \tag{3.2}$$

where the wavevector is defined as $k = \frac{2\pi}{\lambda}$ [4].

The description of a single-particle (time independent) wave behaviour is given by the *Shrödinger* equation:

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(r)}{dr^2} + V(r)\psi(r) = E\psi(r), \tag{3.3}$$

where $V(r)$ is the potential energy in the system, m is the effective mass of the particle, $\hbar$ is equal to $\frac{h}{2\pi}$ and E is the total energy in the system [4].

3.1.1 Quantum Wells and Superlattices

Quantum wells (QW) and superlattices (SL) are engineered materials used to form different semiconductor devices. A QW is the result of using two different semiconductor materials with different band gaps. A SL is just the repetition in one dimension (z-axis) of a certain periodicity formed by a QW and a barrier.

Figure 3.1 shows a schematic diagram of a superlattice built by a periodic repetition of two semiconductors with different band gaps (E_g). The difference in band gaps creates offsets between the conduction bands (ΔE_c) and the valence bands (ΔE_v).

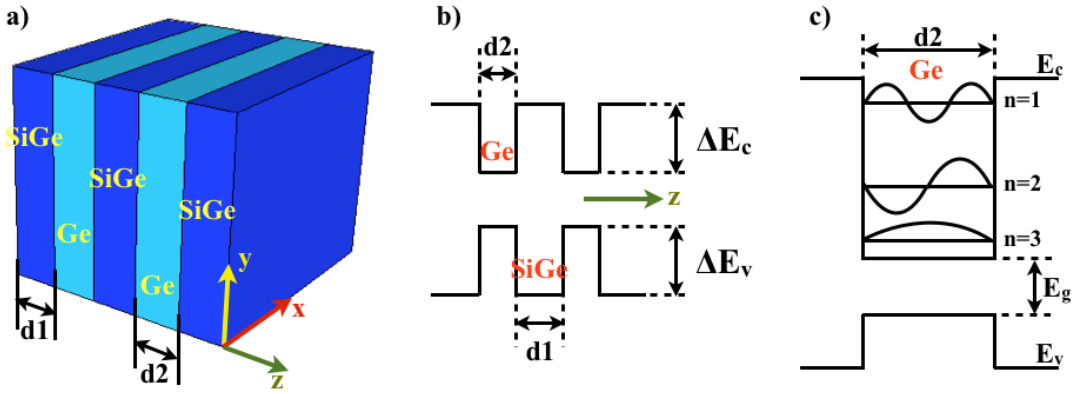

Figure 3.1: *a*) Schematic diagram of a superlattice formed by Ge QW and SiGe barrier. *b*) Band diagram of a superlattice indicating the offset between the conduction and the valence band. *c*) Schematic diagram showing the eigenfunctions of an infinitely deep potential well, as a first approximation to the actual finite barriers of a real Ge/SiGe superlattice.

Let us consider an infinite square potential well where the wavefunctions completely vanish at the walls of the well, as shown in Figure 3.1 *c*). Using Equation 3.3, and knowing that inside the well $V(r) = 0$, we get the following expression:

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} = E\psi(x), \tag{3.4}$$

where the eigenfunctions are given by Equation 3.5 [4].

$$\psi(x) = Asin(\frac{n\pi x}{w}) \quad where \quad n = 1, 2, 3... \tag{3.5}$$

Combining both Equations 3.4 and 3.5, the eigenvalues can be defined by Equation 3.6 [4].

$$E_n = \frac{\hbar^2}{2m}(\frac{n\pi}{w})^2 \tag{3.6}$$

When the potential energy of the well is finite the wavefunction given by Equation 3.5, will decay exponentialy at either sides of the QW walls, $\psi(\mathrm{r}) = \mathrm{De}^{-\beta r}$, giving the carrier a certain probability to tunnel through the barrier in the case of a multi-quantum well structure.

In the following Section 3.1.2 a finite potential well will be considered in order to explain the tunneling process through a potential barrier.

3.1.2 Tunneling Process

In classical mechanics, when a travelling particle with a certain energy arrives at a potential barrier with an energy higher than that of the particle, it is reflected. The particle is only transmitted when its energy is higher than that of the potential barrier.
In quantum mechanics when two semiconductors are brought together, separated by a distance d and with a height potential barrier V_0, if the distance is small enough the particle may be transported through the barrier. This phenomena is known as a quantum tunneling.

Figure 3.2 shows the band diagram of a single potential barrier with distance d, as well as the schematic representation of the $\psi(r)$ in three different regions, $r \leq 0$, $r \geq \mathrm{d}$ and $0 \leq \mathrm{r} \leq \mathrm{d}$).

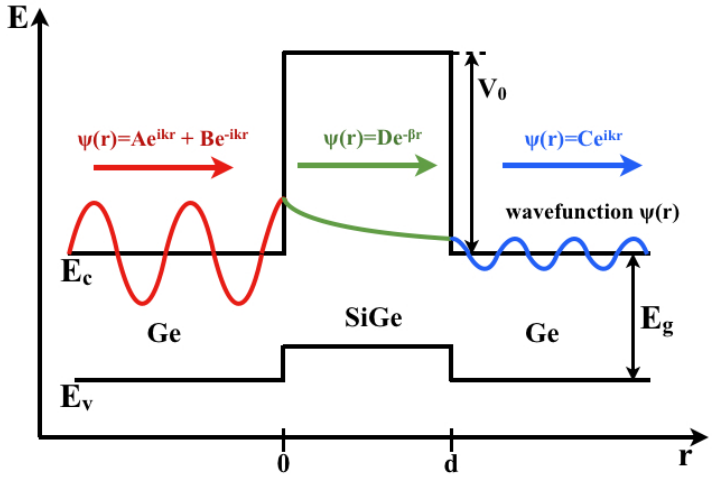

Figure 3.2: Band diagram of a single potential barrier, and the wavefunction of a particle in the three regions, with its corresponding solutions.

Based on Equation 3.3, and taking into account the two regions where $V_r = 0$, we get the same expression as Equation 3.4. The wavefunctions defined for these two regions are [3]:

$$\psi(r) = Ae^{ikr} + Be^{-ikr} \quad r \leq 0 \quad , \tag{3.7}$$

$$\psi(r) = Ce^{ikr} \quad r \geq d \quad . \tag{3.8}$$

For $r \leq 0$ there is an incident particle wavefunction with amplitude A and a reflected wavefunction with amplitude B, while for $r \geq$ d there is a transmitted wave function with amplitude C.

Inside the potential barrier $V(r) = \mathrm{V}_0$. In this region the wavefunction is defined by Equation 3.9 [3].

$$\psi(r) = De^{-\beta r} \quad 0 \leq r \geq d \tag{3.9}$$

Using Equations 3.3 and 3.9 we get that $\beta = \sqrt{2\mathrm{m}(\mathrm{V}_0 - \mathrm{E})/\hbar^2}$.

The probability of an incident particle tunneling through the barrier is given by the transmission coefficient (T):

$$T = e^{-2\beta d}, \tag{3.10}$$

which decays exponentially as the width of the barrier increases [4].

For the vertical designs studied in this work, the carrier transport is based on the tunneling of the electrons (holes) through the barriers [73], as the transport is done perpendicular to the superlattice. The structure of these designs will be reviewed in more detail in Chapters 6 and 7.

3.1.3 Doping in Semiconductors

The carrier concentration of a semiconductor can be increased by introducing impurities in the material. As mentioned in Section 2.3, the carrier concentration is proportional to the electrical conductivity, and so σ can be varied as a function of impurity concentration [4]. Figure 3.3 shows the resistivity (ρ=$1/\sigma$) of a n and p-doped Si sample as a function of impurity concentration [3], where the resistivity is decreased 8 orders of magnitude by increasing the doping concentration from 10^{12} to $10^{21}\,\mathrm{cm}^{-3}$.

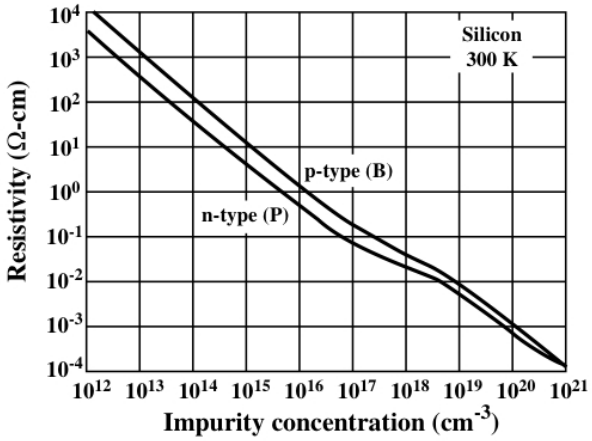

Figure 3.3: Resistivity of a n and p-doped Si sample as a function of impurity concentration [3].

Si and Ge, which belong to group IV of the periodic table, present four valence electrons in the outer shell. Introducing a group V impurity such as boron (B), used as an n-type dopant, increases the number of conducting electrons in the system. Four electrons are

required for the bonding, leaving an additional free electron that moves in the crystal as shown in Figure 3.4 *a*). Similarly, by introducing an impurity such as phosphorus (P), which belongs to group III of the periodic table, three electrons are used to form the covalent bonds leaving a free electron missing from a bond and hence introducing an extra hole into the system (as shown in Figure 3.4 *b*)). P is used as a p-type dopant.

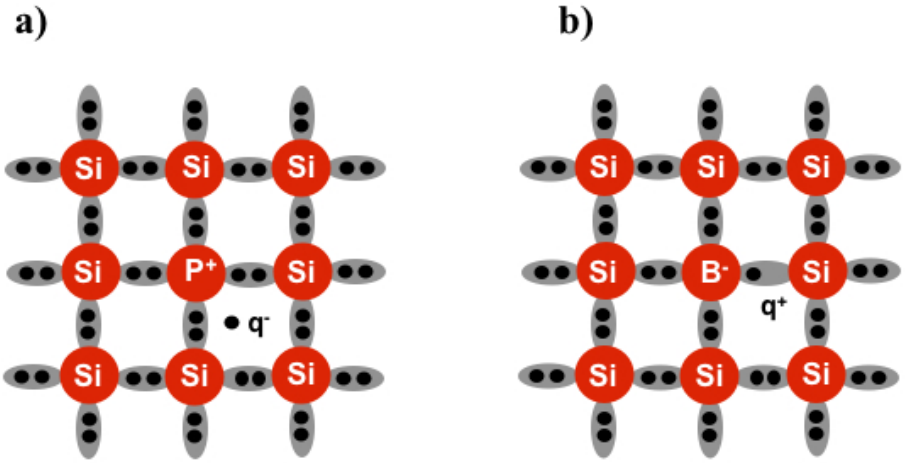

Figure 3.4: Schematic diagrams of *a*) a n-doped and *b*) a p-doped Si [4].

For an intrinsic semiconductor (with no dopants), there are few electrons in the conduction band compared to the number of available states, and therefore the probability of one electron occupaying one of the these states is very small. This probability is provided by the Fermi-Dirac distribution which defines the Fermi level as the energy state that has a 50% probability of being populated by an electron. The Fermi level is normally placed at the middle of the band gap for undoped materials.

On the contrary, doping a semiconductor introduces additional energy states inside the band gap, which are placed close to the minimum of the conduction band, in the case of n-type doping. Normally the energy at room temperature is sufficient to transfer the donors to the conduction band and create free carriers. For highly doped semiconductors, the interactions between the doped atoms are increased and as a consequence the discrete energy state added by the donors turns into a continuous band. This continuous band overlaps with the minimum of the conduction band, effectively decreasing the band gap of the material and shifting the Fermi level closer to the conduction band.

3.1.4 Modulation Doped Semiconductors

Modulation doped is a technique based in δ-doping [74] applied to epitaxially deposited semiconductors. In this technique, the growth of the semiconductor is interrupted to add the dopant impurities on the exposed surface and then the growth is re-started confining the impurities inside the plane where they have been deposited.

In a superlattice the impurities are confined inside the barriers (supply layers) and the channels for the carriers are formed at the side of the undoped material (QW), where the impurity scattering is significantly lower. The two main mechanisms that degrade the mobility of carriers are imperfections in the lattice and the impurity scattering processes. One way to improve the mobility of carriers could be decreasing the doping concentration to reduce the scattering by impurities, but this solution could result in to a lower electrical conductivity degrading the device performance. Modulation doping has demonstrated higher mobilities than uniformly doped superlattices and than similarly doped bulk materials, while keeping high electrical conductivities [75] .

Figure 3.5, shows a schematic diagram of a multi quantum well structure with n-type $Si_{1-x}Ge_x$ supply layers and with i-Ge channels. The electron accumulation lying in the i-Ge channel is known as 2 dimensional electron gas (2DEG). The spacer layers in these structures not only contributes to the confinement of electrons inside the channel but it also separates the supply layer of ionized impurities from the 2DEG, featuring to lower impurity scattering.

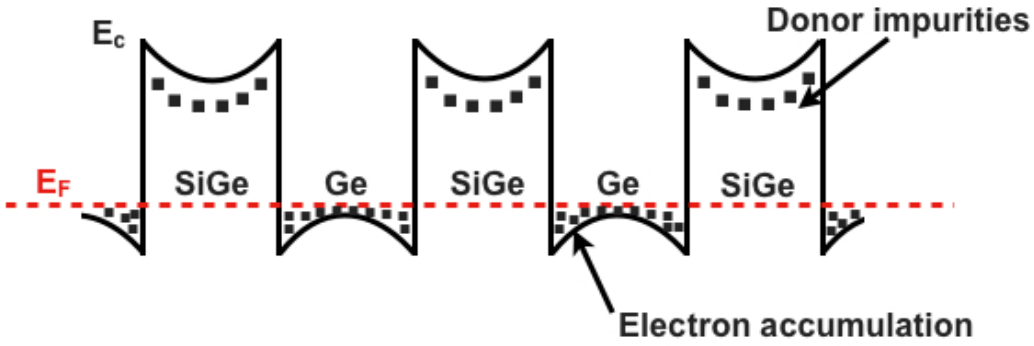

Figure 3.5: Band diagram of a modulation doped n-type $Si_{1-x}Ge_x$ supply layer with an i-Si channel grown on top of an i-$Si_{1-x}Ge_x$ buffer layer [5].

For the lateral designs, as it is explained in Chapter 5, modulation doped superlattices have been studied with the aim of producing high carrier mobilities.

3.1.5 Metal-Semiconductor Contacts

External metal contacts are required in order to test devices. The work function of a solid is defined as the energy difference between the vacuum level and the Fermi level, and so the work function of a metal and a semiconductor is defined by Φ_M and Φ_S respectively (see Figure 3.6). The barrier height that appears at the side of the semiconductor, also known as the Schottky barrier, can be defined as

$$\Phi_B = \Phi_M - \chi, \tag{3.11}$$

where χ is the electron affinity (Figure 3.6), defined by the energy difference between the vacuum level and the bottom of the conduction band. According to Equation 3.11, the barrier height could be engineered by selecting a metal with a Φ_M similar to the χ of the semiconductor, aiming for a contact similar to the one shown in Figure 3.6 *a*).

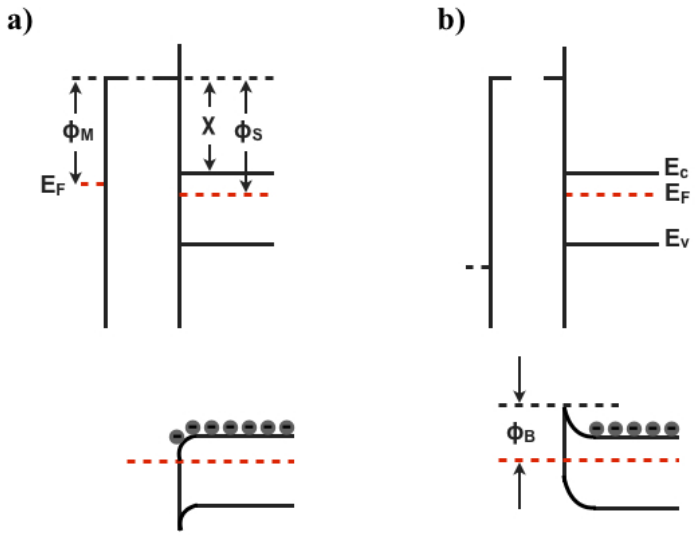

Figure 3.6: Schematic diagrams of *a*) an ohmic and *b*) a Schottky contact. The upper part of the figure shows the metal and semiconductor before bringing them in contact, while the lower part of the figure shows after they are brought in contact [6].

Metal-semiconductor contacts can be defined as one of two categories: ohmic contacts and Schottky contacts.

- An ohmic contact has to be able to drive a current inside the device, producing a small voltage drop across the contact in comparison to the voltage drop produced by the semiconductor. These kind of contacts present linear I-V characteristics. The electrons find small barriers at the interface, therefore flowing into and out of the semiconductor. Figure 3.6 *a*) shows a metal-semiconductor ohmic contact before (upper figure) and after (lower figure) bringing both materials together.

- A Schottky contact presents a non-linear characteristic when a current is driven into and out of the semiconductor. When the two materials are brought together a potential barrier appears at the side of the semiconductor, impeding the electron transfer between the metal-semiconductor and vice versa. Figure 3.6 *b*) shows a Schottky contact before (upper figure) and after (lower figure) the metal and semiconductor are brought in contact.

In practice selecting the appropriate metal is still not enough to create an ohmic contact, and a contact of the type shown in Figure 3.6 *b*) appears as a result. In this case, even if the height of the barrier can not be engineered, the width of it can be narrowed by increasing the doping density. The barrier width is proportional to $N_D{}^{-1/2}$ [6], if the barrier width is thin enough electrons can tunnel from the metal to the semiconductor.

Figure 3.7 shows three conduction mechanisms for lightly-doped, intermediate-doped and highly doped semiconductors (from left to right respectively). Figure 3.7 *a*) shows a metal n-type semiconductor conduction produced by thermionic emission, where the electrons are thermally excited over the barrier. Figure 3.7 *b*) shows a thermionic-field-emission, where some of the conduction is made by thermal excitation and by tunneling, and Figure 3.7 *c*) indicates a field-emission transport, where the conduction is made by tunneling.

3.1.5.1 Contact Resistance

Assuming that an ohmic contact has been created at the interface between the metal and the semiconductor, there is still a voltage drop when the current is driven into the device.

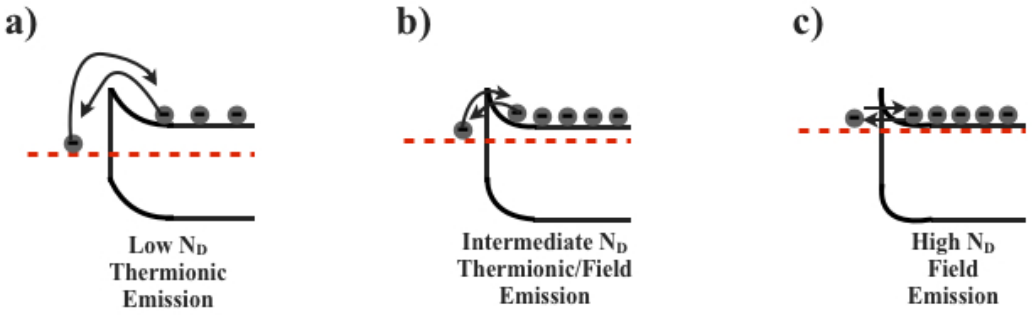

Figure 3.7: Schematic diagram of the three conduction types produced by *a*) thermionic emission, *b*) thermionic/field emission and *c*) field emission [6].

This voltage drop depends on the contact resistance, which should be as small as possible to create high quality ohmic contacts.

For highly doped semiconductors, the width of the barrier is very narrow and in this case the conduction of electrons occurs by tunneling. Furthermore, the barrier height can be engineered by selecting a metal work function similar to the electron affinity of the semiconductor.

There are different test structures available to characterise the contact resistances created at the interface, such as TLM structures (transfer line method) and Van de Pauw structures. TLM structures have been used in the course of this work to characterise electrically the material, aiming for low contact resistances. This method is explained in more detail in Section 4.2.5.

3.2 Ge/SiGe Heterostructures

Epitaxy is the oriented growth of a single crystal layer on top of a single crystal substrate. Chemical instabilities and lattice mismatch are considerable factors that will stop the growth from obtaining high quality semiconductor interfaces.

Silicon and Germanium, both group IV column of the periodic table, have a substitutional alloy ($Si_{1-x}Ge_x$). Si has a lattice parameter which differs 4% from Ge ($a_{Si} = 5.431$ Å and $a_{Ge} = 5.658$ Å), and the $Si_{1-x}Ge_x$ alloy has a lattice constant (Equation 3.12) which follows a linear behaviour (Vegard's law) for different Ge concentrations, as reported by Dismukes [76].

$$a_{SiGe} = 5.431 + 0.1992x + 0.02733x^2 \tag{3.12}$$

When growing a SiGe alloy epitaxial layer on top of a Si substrate, the lattice mismatch between the two materials is given by $f = \frac{a_{SiGe} - a_{Si}}{a_{Si}}$ [5]. The accommodation of mismatched single crystal materials can be answered through the following phenomena:

- Elastic accommodation. The film accommodates by strain.
- Plastic accommodation. The film accommodates via nucleation of misfit dislocations.
- Surface undulation.
- Cracks.
- Curvature of the wafer.

When depositing a film with a larger lattice constant than that of the substrate lattice parameter, the cell fits onto the substrate by producing a compression tension in the in-plane direction, while the opposite tension will occur in the cross-plane direction, passing in this case from a cubic cell to a tetragonal cell (Figure 3.8).

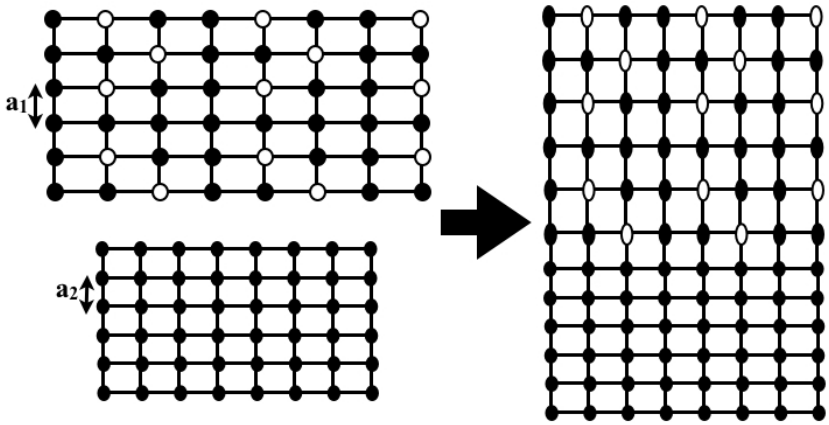

Figure 3.8: Elastic accommodation of a cell with larger lattice constant than the substrate.

Increasing the thickness of the material will increase the elastic energy in the material until (at a certain critical thickness h_c) this one can not be accommodated anymore,

evolving into a plastic relaxation by misfit dislocations at the interface. Misfit dislocations are defined as the discontinuity of atomic planes at the interface. Figure 3.9 shows a schematic diagram of lattice mismatched films with an elastic accommodation on the left and a plastic relaxation on the right.

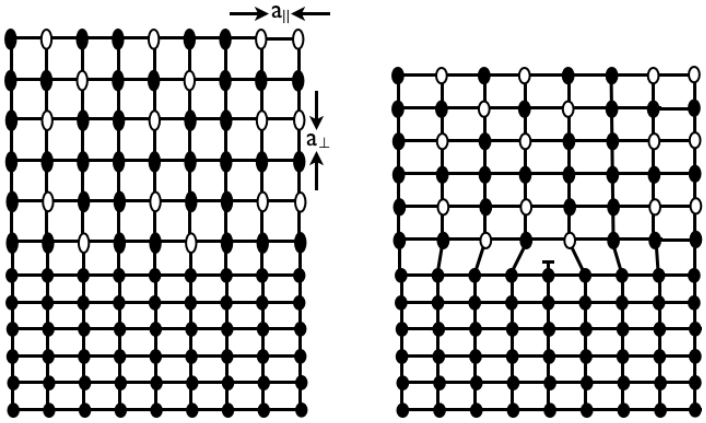

Figure 3.9: Schematic diagrams showing mismatched lattices. On the left can be seen the mismatch corresponding to an elastic accommodation, while the diagram on the right shows a plastic relaxation at the interface.

The existence of defects and dislocations will interact and penetrate through the epilayer through the so called threading arms, in most cases degrading the electrical, optical and thermal properties of the devices.

3.2.1 Strain in Multilayers

To grow thick multilayer structures it is important to compensate for the compressive and tensile forces, reaching a zero-strain situation over the whole structure. This can normally be achieved by having the same average composition inside the heterolayer and the buffer layer [5].

On the other hand the thickness of each individual layer has to be below its critical thickness to avoid the formation of new misfit dislocations at every interface, which will degrade the quality of the material [5]. In this case the lattice mismatch should be calculated with respect to the virtual substrate.

Another issue to take into account is the thermal strain, induced by the different thermal expansion coefficients for Si and Ge. This difference adds a tensile strain in the layer that has been grown during the cool down to room temperature, bending the wafer and even in some cases creating cracks.

3.2.2 Epitaxial Growth Mechanisms

The growth requires the adsorption of atoms, also called adatoms, which constitute a precursor state before the atoms can be incorporated into the lattice. The binding energy is larger than the adsorption energy and that is why diffusion energy is required in order to incorporate the adatom in the crystal. If the diffusion does not happen fast enough, the adatom can escape by desorption due to thermal vibrations. The energy of the diffusion is defined by the temperature of the surface.

The common techniques for epitaxial growth are chemical-vapour deposition (CVD) and molecular-beam epitaxy (MBE):

- *Molecular beam epitaxy:*
  The raw material is heated up until it reached its melting point by effusion cells. The beam of atoms and molecules released from the material reacts with the crystalline surface under ultrahigh-vacuum conditions to produce an epitaxial layer. MBE has a high control of the chemical composition and doping concentrations. However, the high melting points for both Si and Ge makes the use of effusion cells not suitable for this kind of growth, instead it is necessary to use electron beam evaporators.

- *Chemical vapour deposition:*
  The epitaxial layer growth occurs through the chemical reaction of different gaseous compounds. The species (gases and dopants) are brought inside the chamber to the substrate region, some of them are absorbed by the surface substrate where a chemical reaction occurs, producing the growth of the epitaxial layer. The gases products are then desorbed into the main gas flow. Since standard CVD reactors work at high temperatures, going from 900°C up to 1100°C, a number of chemical vapour deposition reactors have been developed for low temperature growth such as ultra-high vacuum CVD (UHV-CVD) [77, 78], low pressure CVD (LPCVD) [79] and low energy plasma enhanced CVD (LEPECVD) [80, 81]. The interest in growing

material at lower temperatures is related to the issue of getting strained $Si_{1-x}Ge_x$ layers, without rough surfaces or the diffusion of germanium.

3.2.2.1 LEPECVD Growth Technique

LEPECVD was used to grow all the wafers that have been characterised within this work. This technique [80, 81] has been developed to reach high growth rates of epitaxial Ge and Ge-rich SiGe alloys, which is suitable for growing layers up to 10 μm thickness within an acceptable time, compared to other techniques.

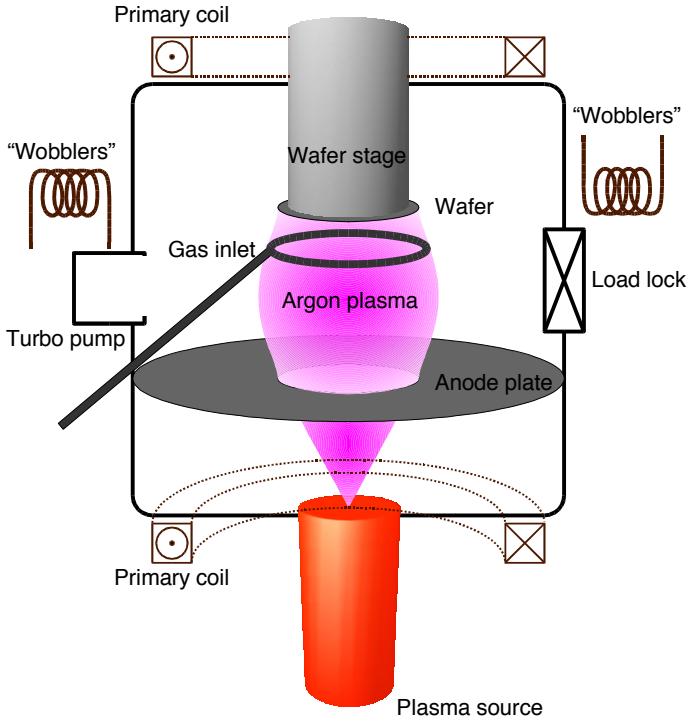

Figure 3.10: Schematic diagram of an LEPECVD reactor, image taken from [7].

The gases are transported into a vacuum chamber where an argon plasma is created to bring the energy necessary to break the gaseous molecules (Figure 3.10). The gases used for Ge and SiGe alloy growth are SiH_4 and GeH_4 for n-type dopants, and PH_3 and B_2H_6 for p-type dopants. In this system the growth rate can be controlled independently from the substrate temperature. The density of the plasma will regulate the growth rate, while the growth temperature can be lowered to optimise the doping profile and the strain of

the material deposited. Depending on the flow of the gases, and the plasma density the growth rate can be regulate from 0.1 Å/s to 100 Å/s.

The focused plasma is characterised as having a bell-shaped inhomogeneity, which will result in a variation in the layer thickness across a 100 mm wafer. The variation of the layer thickness can go from 130 % of the nominal thickness in the centre, to 80 % at the edges.

The detailed structure of each wafer characterised is presented in chapters 5, 6 and 7, followed by their characterisation and their conclusions beside the characterization.

3.2.3 Virtual Substrates

When growing an active heterolayer on top of a Si substrate an intermedium layer, also called *Virtual Substrate* (VS) or *Buffer layer*, is necessary in order to accommodate the lattice mismatch, relaxing the structure and controlling the threading dislocation density.

The ideal case would be to have long threading arms that glide to the edge of the wafer, to stop the dislocations by interacting between them and therefore stopping them from going inside the epitaxial layer grown above the virtual substrate. A way to reduce the TDD to values around $10^6\,\mathrm{cm}^{-2}$ is to grow the buffer layer grading the Ge content from 0 % to the required Ge composition. Work done in [4] showed how reducing the Ge grade rate from 52 % per μm to 5 % per μm resulted in an improvement of the surface, a reduction of the threading segments, a reduced interaction between dislocations and also a high mobility.

For standard LEPECVD growth the buffer layer is grown grading linearly the Ge content at a rate of 7 %/μm. This grading is also followed by a reduction of the temperature from 750°C to the temperature desired for the active layer. These strain relaxed buffer layers can reach low TDD values of $10^6\,\mathrm{cm}^{-2}$ and the thicknesses can vary from 10 to 12 μm depending on the Ge content desired for the active layer.

For the growth of vertical designs having thick buffer layers did not affect the performance of the fabricated devices. For the vertical thermal characterisation it was necessary to confine the heat on a mesa structure (refer to Chapter 6 for more details) where the thick buffer layer and the Si substrate were used as a heat sink. On the other hand, the scenario to thermally characterise the lateral designs changed substantially from the vertical ones. The heat needed to be confined inside a lateral device where the buffer

layer behaved as a parallel parasitic channel. Thin buffer layers were required to reduce this parallel channel contribution and low TDD were mandatory to avoid deterioration of the thermoelectric properties of the material as it is explained later in Chapter 5.

3.3 Chapter Summary

Quantum transport inside 2D structures has been introduced as the focus of this thesis is to study the thermoelectric properties of Ge/SiGe superlattices. Since the behaviour of the thermoelectric properties in superlattices is quite anisotropic the two main mechanisms dominating carrier transport have been introduced: the tunneling process to transport carriers across the superlattice (Chapter 6 and 7) and δ-doping to transport carriers along the quantum wells delivering higher carrier mobilities (Chapter 5). In order to test the micro-fabricated devices (introduced in Chapter 5 and 6) optimised ohmic contacts had to be performed. The physics to understand how to create ohmic contacts became an important issue in the course of this thesis to lower as much as possible the contact resistances to extract the cross-plane electrical conductivities of the different superlattices (work presented in Chapter 6 and 7).

All the superlattices studied were grown by a LEPECVD tool. A virtual substrate or buffer layer was required in order to accommodate the lattice mistmach between the Si substrate and the heterolayer, relaxing the structure and keeping TDD lower than $10^8\,\mathrm{cm}^{-2}$. Keeping the heterostructures with such TDD was considered an important issue to obtain high efficiencies in the material studied. Theoretical analysis to study the impact of ZT as a function of TDD is presented in more detail in Chapter 5, where experimental results are compared to the theoretical analysis.

Chapter 4

Fabrication and Characterisation Techniques

The aim of this chapter is to give a brief description of some of the tools and processes that have been used to fabricate the thermoelectric structures. Each section explains the basic concept behind a fabrication process and/or a particular tool that has been used within the fabrication of the final devices. Developments and optimizations are illustrated with optical and SEM images which were taken during the fabrication. In chapters 5 and 6 detailed descriptions of the steps followed to fabricate the final devices are reported.

4.1 Fabrication Techniques

4.1.1 Optical Lithography

Optical lithography is an important part of semiconductor manufacturing technology for fabricating micromechanical systems (MEMS) where, different masking levels are required to complete a device. This technique transfers a pattern to an optically sensitive resist, which is then used as a mask to perform a subsequent step, such as a lift-off process or an etching process. In this way, the thin-film material of the wafer is selectively removed or built up.

The standard steps to follow when fabricating with optical lithography are listed in Figure 4.1.

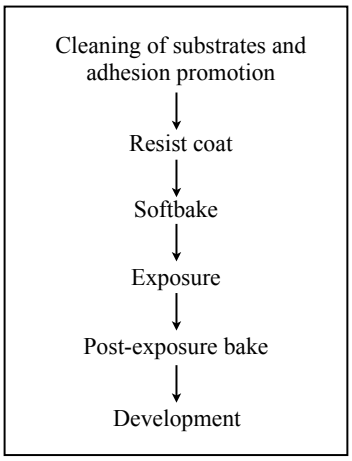

Figure 4.1: Steps involved in a lithography process.

- **Cleaning of substrates and adhesion promotion:** Substrates contaminated with particles or organic impurities are cleaned by using acetone and a subsequent rinse in isopropyl alcohol. A soft bake at 120-140°C for several minutes is used for the desorption of H_2O. The resist coating should be applied immediately after cooling the substrate in order to avoid re-adsorption of water.

- **Resist coat:** To coat the substrates with resist, a small amount of resist in solvent is dropped on top of the substrate which, is then spin at a high speed. The spin coating represents a balance between the centrifugal force and the solvent evaporation, increasing both of them with the spin speed. During the first few seconds of spinning a high concentration of solvents is evaporated, then this concentration saturates. The solvent concentration can be further reduced later on during the softbake of the film resist.

- **Softbake:** After the spin coating, the thin film resist is cured for a few minutes in order to drive off residual solvents. This step also improves the adhesion to the substrate and reduces mask stiction or contamination.

- **Exposure:** The emission spectrum of a mask aligner with a mercury lamp as a light source, contains three lines defined at three different wavelengths, which are g- (436 nm), h- (405 nm) and i-line (365 nm). Photoresists are materials designed to have photochemical reactions when they are exposed to particular emission lines,

therefore it is important to know which is the spectral sensitivity of the photoresist used. The spectral sensitivity for a photoresist does not end at a certain wavelength but it gradually drops to zero over several nm of wavelength.

It is also important to distinguish between positive and negative resists. Positive resists become soluble in developer after being expose to light, while negative resists behave in the opposite manner. Unexposed negative resists have very high solubility in developer and lose their solubility by exposure to light.

- **Post-exposure bake:** This is an optional bake done just after the exposure and before the development. In case of working with negative resists, it is normally used to drive additional chemical reactions, such as the crosslinking mechanism initiated during the exposure.

- **Development:** It is the process where a resist is selectively removed, depending on the areas that have been or have not been exposed.

Two of the limitations for using an optical lithography tool are related to: the feature sizes that can be patterned and the alignment that can be achieved when a second mask layer is required.
The optical lithography mask aligner tool available in the James Watt Nanofabrication Centre (JWNC) is a Süss MA6 [82] which includes a 350 W mercury lamp as a light source. This light source produces $25\,\mathrm{mW/cm^2}$ as an exposure dose for a 365-nm line. Depending on the resist used, lines of $1 \pm 0.5\,\mu$m can be patterned and an alignment of around $1\,\mu$m can be achieved.

The thermoelectric structures fabricated within this work were inside the tens or hundreds of the micrometer scale, and $1\,\mu$m alignment was sufficient in the design of the structure to guarantee working devices. All the different steps for etching and lift off were undertaken by optical lithography.

Thick resists were used during the fabrication process in order to pattern structures on top of $10\,\mu$m high mesas. When working with thick resists, where the film thickness is greater than the penetration depth of light, the illumination density in the resist film is not homogenous. At the beginning of the exposure only the first few μm near the resist surface are absorbed. This few μm let the light to illuminate deeper and deeper until

reaching the substrate. That is why the exposed film thickness increases almost linearly with time.

4.1.2 Etching Techniques

Wet etching processes have been replaced by plasma-based etching technology in many semiconductor manufacturing steps. The main reason for using dry-etching processes, within micro/nano-fabrication when working with semiconductors, is due to the ability to etch directionality and transfer a photoresist pattern into underlaying layers. Other advantages that dry-etch offers are cleanliness and compatibility with automation and vacuum processing technologies.

Reactive ion etching (RIE) is a plasma-based etching process which combines the effects of the physical sputtering with the chemical activity of reactive species. This enables one to create anisotropic etches with uniformity and etch time control. A radio frequency (RF) voltage is applied between two parallel plates (an anode and a cathode) to control a Capacitive Coupled Plasma (CCP) which will create both the ion density and the ion acceleration.

The following steps explain the processes that take place inside a basic reactive ion etching system:

1. Production of active species. A gas is pumped into a vacuum system separated by an anode and cathode. The plasma starts by the collision of ions with gas molecules. The collisions are produced as ionized electrons are accelerated between the plates, and collide with the gas, generating an increasing population of ions and electrons.

2. The material to be etched is placed on top of a Capacitively Couple Electrode. As the mobility of the electrons is higher than the ion mobility the electrode acquires a negative charge which will be exposed to a high positive ion bombardment.

3. Transport of the active species by diffusion from the plasma to the surface of the material to be etched.

4. Adsorption step: Absorption of the radicals on to the surface for concurrent ion bombardment.

5. Reaction step: A reaction between the adsorb radicals and the material to be etched takes place producing some volatile species or a physical sputtering of the substrate.

6. Desorption of volatile reaction product.

7. Pump-out of volatile reaction product.

For the fabrication of the devices different dry etch recipes were developed using a BP80-RIE machine from Oxford Plasma Instruments [83] and STS-ICP from Surface Technology Systems [84].

The BP80-RIE tool was used to anisotropically etch thin layers of Si_3N_4 and SiO_2. The two following tables, 4.1 and 4.2, show the parameters used to etch each dielectric layer, respectively.

Parameter	**Value**
Gas	CHF_3/O_2
Flow (SCCM)	50/5
Platen Power (W)	150
Pressure (mT)	55
Etch rate (nm/min)	50

Table 4.1: Si_3N_4 Etching parameters in BP80 RIE.

Parameter	**Value**
Gas	CHF_3/Ar
Flow (SCCM)	25/18
Platen Power (W)	2000
Pressure (mT)	30
Etch rate (nm/min)	30

Table 4.2: SiO_2 Etching parameters in BP80 RIE.

A STS-ICP was used in order to perform anisotropic and isotropic etches on Si, Ge and SiGe alloys. An arrangement of the Inductively Coupled Plasma (ICP) with the RIE creates a very powerful combination where one is able to change the ion density using the ICP without perturbing the energy of the ions controlled by a CCP.

In an ICP process there are two different RF power generators. One of them is used to produce the excitation of ions, delivered inductively via a coil wrapped around the RIE plasma remote from the sample to be etched. In addition, a coupled plasma RF supply is used to vary the ion acceleration towards the material, allowing reduced ion bombardment damage of the substrate.

Two different anisotropic etches were developed in order to create the mesa structures.

For both devices two recipes were optimised using a gas mixture of between SF_6 and C_4F_8 gases. The majority of the etch relies on the SF_6 etch gas, which behaves as an isotropic etch gas. The C_4F_8 deposits a polymer which acts as an etch mask to SF_6 etching which makes possible to selectively control the direction of the etch to create either straight walls or positive and negative slopes.

A positive slope of the mesa structure was required in order to allow the continuity of metal lines going from the top to the bottom of the mesa. The parameters used in this recipe are displayed in table 4.3, this recipe had an etch rate of 1.1 μm/min to etch the Ge/SiGe superlattices. This positive slope of about 10 degrees was enough to keep the continuity of the metal on the side walls after metal deposition, see section 4.1.4.

Parameter	**Value**
Gas	C_4F_8/SF_6
Flow (SCCM)	90/130
Platen Power (W)	12
ICP Power (W)	600
Pressure (mT)	15
Etch rate (nm/min)	1030

Table 4.3: Silicon/Germanium Etching Parameters to create a 10 μm high mesa structure with a positive slope.

Parameter	**Value**
Gas	C_4F_8/SF_6
Flow (SCCM)	90/40
Platen Power (W)	10
ICP Power (W)	700
Pressure (mT)	10
Etch rate (nm/min)	390

Table 4.4: Silicon/Germanium Etching Parameters to create a mesa structure of 4 μm high with a negative slope.

On the other hand, a negative slope to obtain an undercut between the top and bottom of a mesa structure was also required. This undercut of the structure was used as a self-alignment to create bottom and top contacts with one single lift-off step. Table 4.4 shows the parameters used to create such an undercut. The etch rate was reduced to 400 nm/min to get a better control of the etch and be able to stop within the 500 nm thick bottom contact layer.

Figure 4.2 *a*) shows the side view of one of the mesa structures with a positive slope created after etching. Figure 4.2 *b*) shows the side wall of a 4 μm high mesa with an undercut of about 10 degrees.

One isotropic etch was performed in order to create the suspended membranes. After building-up the full device, a top etch was necessary in order to release the device from

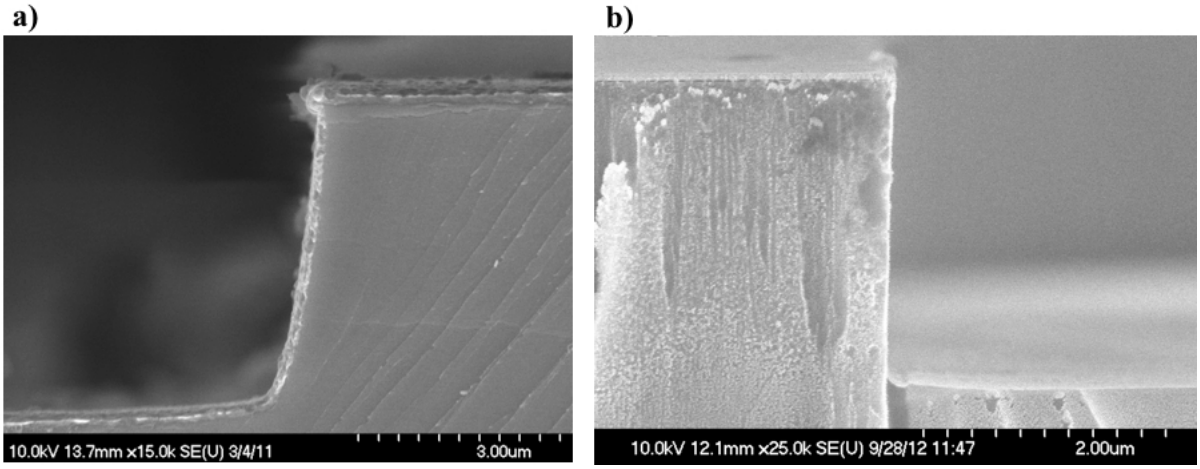

Figure 4.2: *a*) Shows a SEM picture of an optimised recipe to anisotropically etch the epitaxial material and create mesa structures with positive side walls. *b*) Shows the opposite profile, where a side wall with a certain amount of undercut between the top and bottom of the mesa was required.

Parameter	**Value**
Gas	SF_6/N_2
Flow (SCCM)	40/2
Platen Power (W)	0
ICP Power (W)	650
Pressure (mT)	14

Table 4.5: Silicon Etch Parameters to perform an isotropic etch.

the silicon substrate. In this case it was necessary not only to etch vertically but also laterally. A mixed-recipe of SF_6 and N_2 for 75 minutes, table 4.5, was used to create such an etch. Figure 4.3 *a*), shows a SEM image where it can be seen the isotropic etch performed underneath a SiO_2 layer, the sample was under-etched that is why there is still a junction between the substrate and the SiO_2 layer. Figure 4.3 *b*) shows a complete suspended membrane on a SOI (Silicon on insulator) sample, where the Si substrate under the SiO_2 was etched isotropically. The devices that needed to be fabricated on suspended membranes were always fabricated on top of SOI, serving the SiO_2 layer as an etch stop.

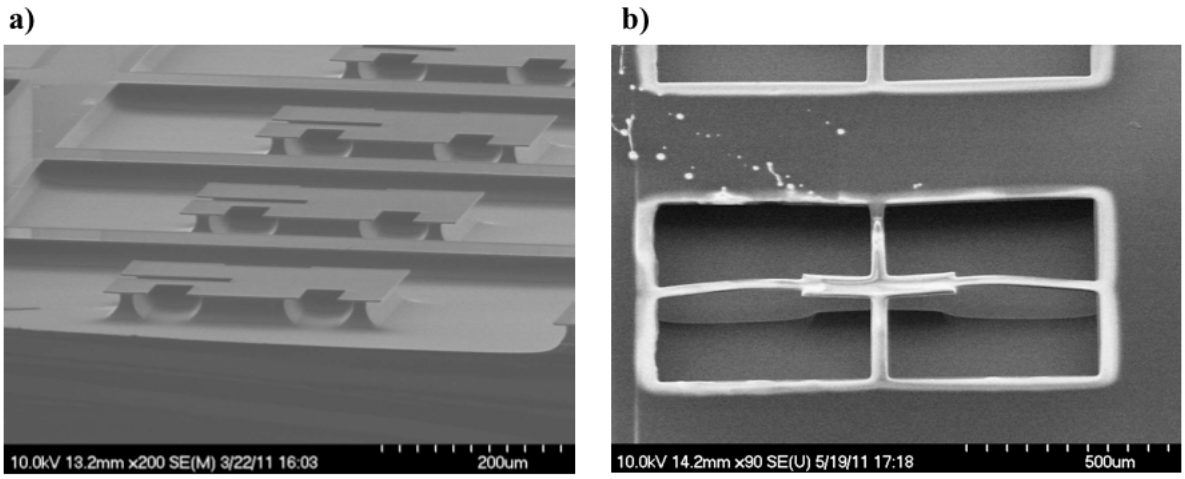

Figure 4.3: *a*) SEM image of the isotropic etch detailed in table 4.5. The substrate is still joined to the SiO_2 layer. *b*) SEM image showing a side view of a suspended membrane. It can be seen that the Si substrate has been isotropically etched.

4.1.3 Passivation: Silicon Nitride Deposition

During fabrication, the deposition of thin layers of silicon nitride (Si_3N_4) was required to isolate the structure from bond-pads, heaters and thermometers.

The two tools available to deposit Si_3N_4 in the JWNC are an Oxford Instruments System 100 ICP 180 PECVD and an Oxford Instruments PECVD 80+ [85]:

- A PECVD (Plasma-enhanced Chemical Vapour Deposition) system consists of a vacuum chamber containing two electrodes placed in parallel. The plasma is generated between the two electrodes where the top one is connected to the RF generator and the bottom one is electrically grounded. The samples are loaded on top of the bottom electrode, the gases are fed inside the chamber entering on the plasma region creating the ionized gas species from which the SiN film is synthesised. The temperature deposition occurs between 200°C and 300°C.
- An ICP-CVD (Inductively Coupled Plasma Chemical Vapour Deposition) system consists of a vacuum chamber containing an ICP power source and a rf powered wafer chuck. This hybrid configuration adds the possibility of controlling ion flux and ion energy independently. In this case the deposition is made at room temperature.

For the lateral devices it was necessary to release the final device from the substrate to create a suspended membrane and cancel the high thermal influence of the substrate. Hall bars of 2 mm long were fabricated at the beginning in order to assist the temperature difference between the two thermometers. A 100 nm thick film of ICP-CVD nitride (see parameters on table 4.6) were deposited to isolate the heaters, thermometers and bond-pads from the semiconductor.

Parameter	**Value**
Gas	SiH_4/N_2
Flow (*SCCM*)	7.2/6
Platen Power (*W*)	100
Pressure (*mT*)	4.4

Table 4.6: Parameters to deposit a thin layer of silicon nitride by an ICP-CVD tool.

Parameter	**Value**
Gas	$SiH_4/He/N_2/NH_3$
Flow (*SCCM*)	8.5/275/16
Platen Power (*W*)	21
Pressure (*mT*)	1000

Table 4.7: Parameters to deposit a thin layer of silicon nitride by a PECVD tool.

For these first devices, it was found that after etching the substrate away the suspended membrane was not able to support the strain, causing the fracture of the structure, Figure 4.4 *a*). To solve this problem, the dimensions of the devices were scaled down by a bit more than half of its original size and a recipe with zero stress for nitride deposition was selected to avoid any additional strain to the structure, Figure 4.4 *b*). This recipe was deposited by PECVD and the parameters of such a recipe are listed in table 4.7.

On the other hand, when the devices did not required to be de-attached from the substrate, problems related to the strain of the structure were not found. In this case an ICP-CVD tool was used to deposit thin layers of nitride. The parameters used are listed in table 4.6.

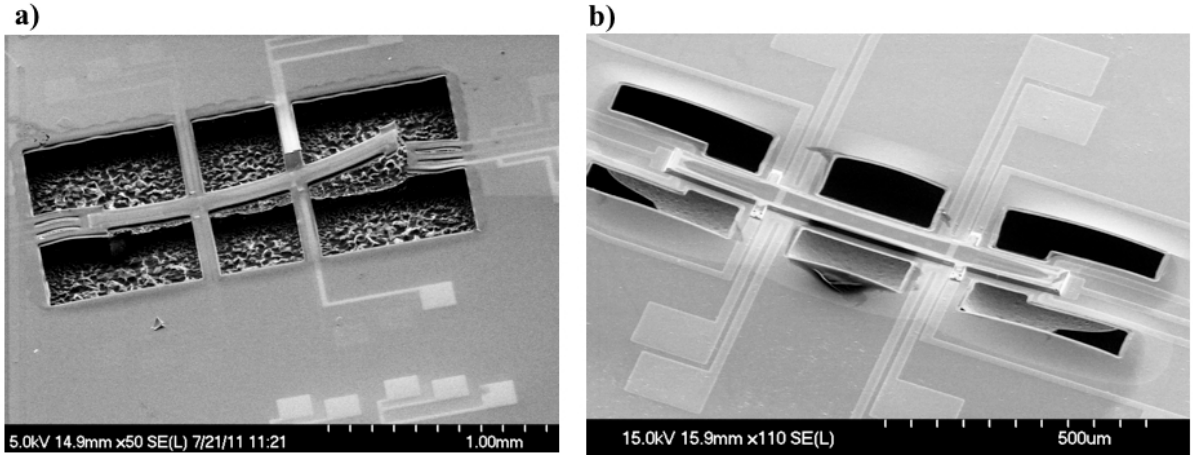

Figure 4.4: *a*) SEM image showing a 2 mm long suspended membrane which broke after releasing the substrate from the final device. *b*) SEM image showing a 800 μm long suspended membrane fully standing after substrate removal.

4.1.4 Metal Deposition, Lift-off and Metal Etching

Metal deposition was used to define heaters, thermometers, ohmic contacts and bond-pads onto the devices. There are two basic techniques that can be used to define a metal pattern onto a substrate; lift-off and metal etching:

- In a lift-off process, a photoresist with a certain undercut defines the pattern on a substrate. The metal is then deposited on top of the sample covering all the areas with and without resist. After metal deposition, the sample is immersed in acetone for a couple minutes. The acetone dissolves the mask lifting off the metal that was deposited on top of the resist and leaving the metal that was in contact with the substrate. The thickness of the resists should be at least 3 times larger than the thickness of the metal to assure a successful lift-off. An undercut profile of the resist is also required to aid the lift-off process.

- In a metal etching process, the metal is first deposited on top of the substrate and then a resist is used to define a pattern. The pattern acts as an etching mask to selectively remove the metal. Etching metals normally requires strong acids which can easily damage the substrate and which normally perform isotropical etches modifying the original pattern. This is why this process is not common when fabricating MEMs. Dry etching is also used to remove metals.

Figure 4.5 (a) shows bilayer of NiCr and Au defined by a lift-off process, while b) shows the same bilayer of metal where just the Au layer had been selectively etched.

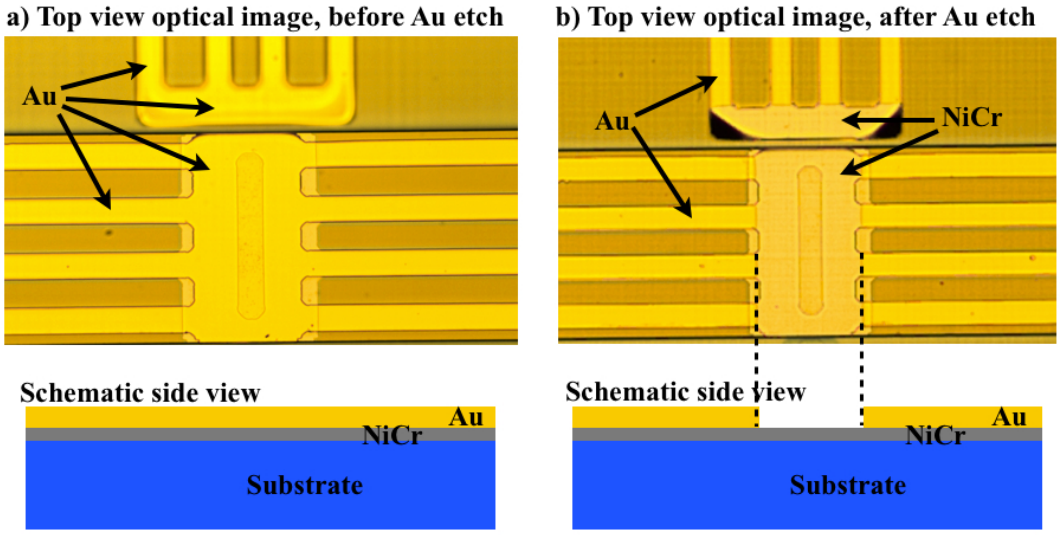

Figure 4.5: a) Shows an optical top view of a metal line formed by a bilayer of NiCr and Au. b) Shows an optical picture where a square of Au has been selectively etched and the NiCr has been released.

The metal deposition was carried out using a Plassys (MEB 400s) electron-beam evaporator [86] or using a Plassys MP900S Sputter coater [87].

- An electron-beam evaporator uses an electron-beam source to heat up the source material until it starts to evaporate. The evaporation takes place under vacuum enabling the molecules to move without scattering in the chamber until they reach the substrate, where they can be absorbed or condensed.

- In a sputter coater system, a plasma is created between two parallel electrodes under vacuum. The sample is normally loaded onto the anode and the source material constitutes the cathode. An electric field removes electrons from neutral gas atoms producing positively charged ions, generally Ar^+. These positively charged ions are driven into the cathode hitting the surface and ejecting or sputtering source material, which is deposited onto the substrate. Sputtering is not directed and has

an isotropically behaviour which helps to coat the resist surface as well as the resist sidewalls.

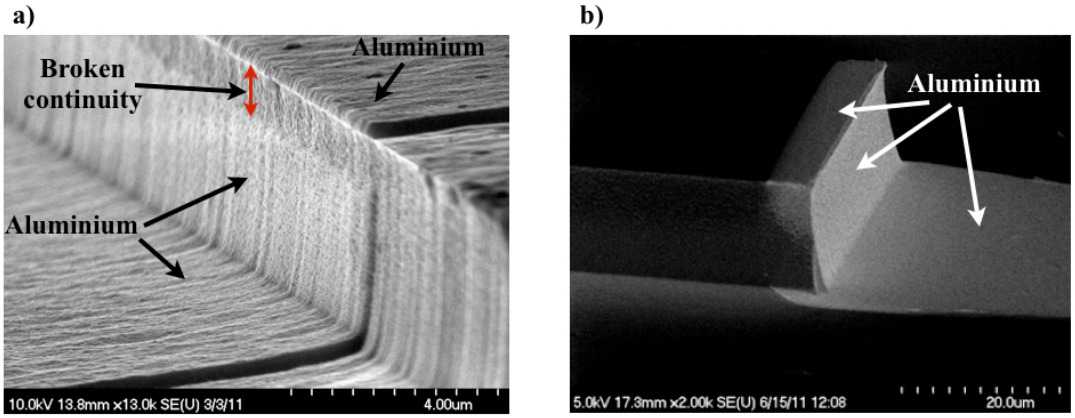

Figure 4.6: The SEM picture on the left *a*), shows the metal deposition of 300 nm of Al by an electron-beam evaporator. It can be seen that the side wall is not completely covered by the Al, breaking the continuity of the metal line between the top and bottom mesa. The SEM image on the right *b*), shows the same metal deposition done by a sputtering tool. In this case the continuity was successfully kept.

The electron-beam evaporator tool was not able to completely coat metal onto the side walls of the 10 μm high mesa structures, required for the fabrication of the final devices. For this reason it was found necessary to sputter the metal to guarantee the continuity from the top to the bottom of the mesa. Figure 4.6 shows the side wall of a mesa structure after depositing 300 nm of Al by *a*) an electron-beam evaporator tool and *b*) a sputter coater tool. *a*) Shows a discontinuity at the side wall, while *b*) shows a uniform thickness that goes from the bottom to the top of the mesa.

4.1.5 Resist Optimisation

When dry etching for a certain time, the side wall profile of the resist can be critical in order to transfer the exact etch desired into the semiconductor. In this case straight side walls for the resist were needed to perform certain anisotropic etches to create the mesa structures of the devices.

As explained in Section 4.1.2, an etch to create a mesa structure with an undercut or negative slope was required. An unoptimised recipe for the resist with a slope on its side

wall was not able to support the dry etch recipe for more than 4 minutes. About 8 minutes were normally needed to etch 4 μm of material. After these first minutes, the gases were able to completely remove part of the mask at the edge of the patterns. The side walls of the mesa structure, which at the beginning of the etch had the correct undercut, were transformed into straight walls once the mask had been attacked by the dry etch recipe. Figure 4.7 *a*) shows a cross section view of a mesa structure with the mask on top after etching for 8 minutes. The side wall of the resist had a pronounced slope producing a weak resistance of the mask at the edges of the pattern and affecting the etching profile.

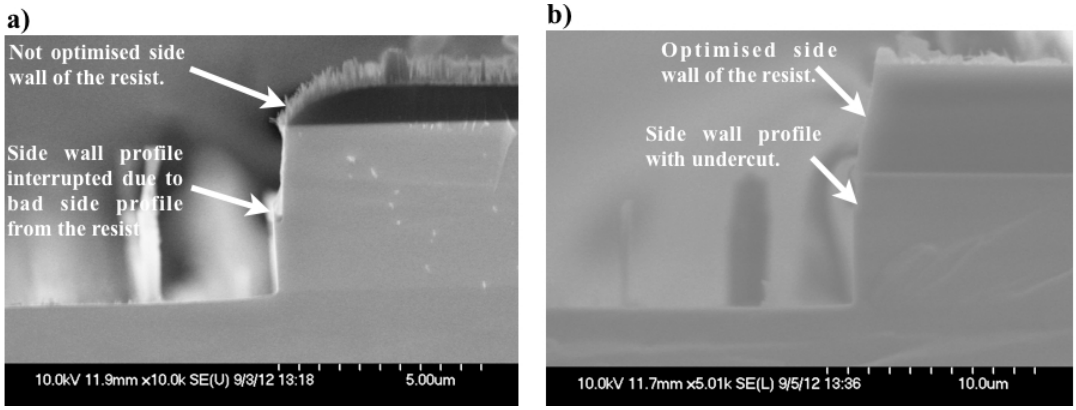

Figure 4.7: Two SEM cross section views of mesa structures with the mask on top. Figure a) shows an unoptimised mask producing the incorrect etch into the semiconductor. Figure b) shows an optimised mask with straight side walls to pattern a mesa structure with an undercut into the semiconductor.

It was found that this pronounced slope at the side of the resist was due to the high mask erosion obtained because of an under-expose and over-developed resist. The exposure time was therefore increased, with a corresponding decrease in development time, and mask erosion was reduced significantly, as indicated by straight side walls. Figure 4.7 *b*) shows the cross section view of a mask with straight side walls on top of a mesa structure after etching for 8 minutes. This optimised recipe allowed the correct transfer of the pattern, producing an undercut on the sides of the mesa structure.

AZ4562 [88], positive resist of $\simeq$ 6.2 μm thickness, was the resist used for dry etch processes and the parameters of the final recipe optimised are listed below:

1. Resist Spinning and baking for AZ4562:

- Spinning at 4000 rpm for 60 sec to obtain 6.2 μm resist layer thickness.
- Baking at 100°C for 6 minutes and 20 seconds.

2. Photolithography exposure for 25 seconds.
3. Development using 1:4 dilution of AZ-400 developer and deionized water (DI water) for 2 minutes and 30 seconds and then subsequent rinse in DI water for at least 30 seconds.
4. O_2 ashing at 100 W for 2 minutes.
5. Dry etch process for the patterning of semiconductor.

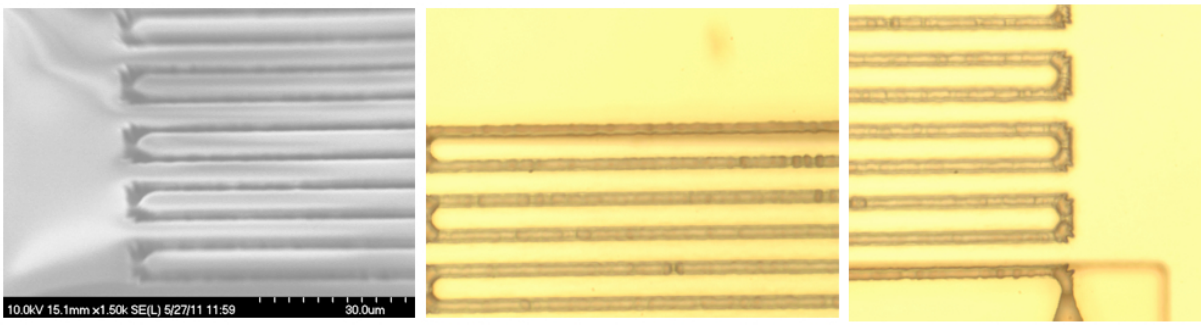

Figure 4.8: The SEM and optical pictures show some of the first attempts to define a serpentine heater on top of a 10 μm high mesa. The big undercut produced for the negative resist was shrinking the patterns resulting in a very poor lift-off process.

A second process developed using AZ2070 [88], negative resist of $\simeq$ 7 μm thickness, was used to make sure that the top of the mesas were coated uniformly to create flat surfaces and to allow good lift off definition. Figure 4.8 shows some of the initial tests where the recipe was not completely optimised due to the big undercut created by over-exposing the resist.

Once the resist had been optimised, reducing its undercut, the recipe was used for patterning heaters, thermometers, ohmic contacts and bond-pads. Figure 4.9 *a*) shows the optimised resist process for defining a NiCr heater on top of a mesa, with a second alignment layer *b*) to define the Al interconnect metal line which goes from the top of a 10 μm high mesa to the bottom.

The steps to follow in order to create the metallic structures are listed below:

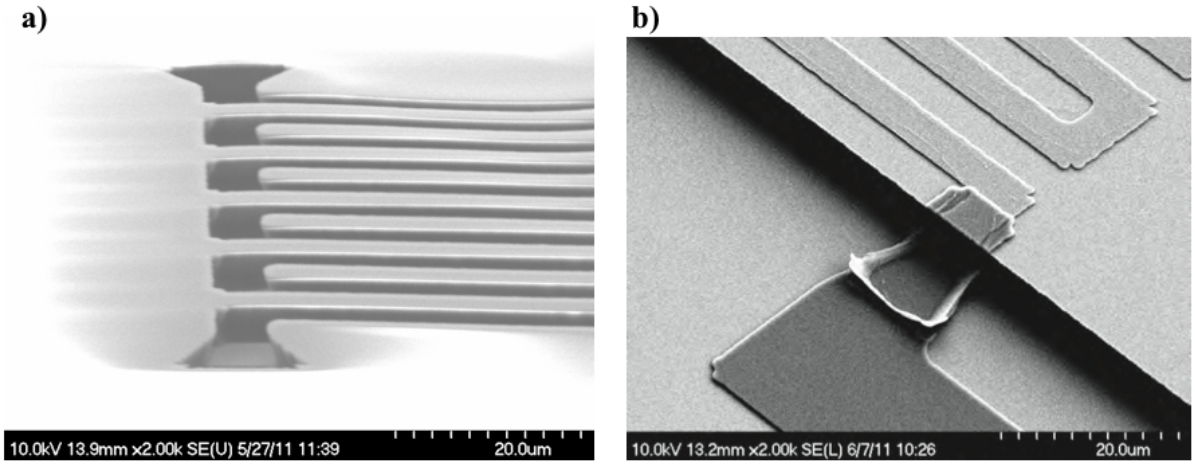

Figure 4.9: Figure *a*) shows the pattern of a heater defined on top of a 10 μm high mesa before metal deposition. *b*) shows the NiCr heater defined after lift-off aligned with a second layer of Al deposited in a separate run, used to create the interconnects to the heater on top of the device mesa.

1. Resist Spinning and baking for AZ2070:
   - Spinning at 4000 rpm for 60 sec to obtain 7 μm resist layer thickness.
   - Baking at 110°C for 1 minute and 30 seconds.
2. Photolithography exposure for 20 seconds.
3. Post-baking at 110°C for 1 minute.
4. Development using MF-319 developer for 1 minute and 15 seconds and then subsequent rinse in DI water for at least 30 seconds.
5. O_2 ashing at 100 W for 2 minutes.
6. Metal deposition by electron-beam evaporator or reactive sputter deposition.
7. Lift-off technique. The sample is immerse in hot acetone after metal deposition. The acetone dissolves the resist layer lifting off only the metal placed on top of the resist.

4.2 Characterisation Techniques

4.2.1 Resistive Thermometry

Thermal characterisation tools were required to measure material thermal conductivity and Seebeck coefficient. In order to do this, two different devices with integrated heaters and thermometers were developed to generate a temperature gradient and measure the temperature value.

The micro-fabricated integrated thermometers, fabricated by lift-off, consisted of 10 nm of titanium (Ti) plus 70 nm of platinum (Pt) or palladium (Pd), while the heater consisted of a thin layer of 50 nm of NiCr. The thermometers were a 4 terminal design to remove the error from access resistances.

Before the temperature gradient across the structure can be determined, it is necessary to calibrate the thermometers [89]. Two lock-in amplifiers were used to measure the voltage across the thermometer and across a 1 kΩ precision resistor. The precision resistor was connected in series to the thermometer just to provide an accurate measurement of the current going through the circuit. Knowing the current and also the voltage dropped across the thermometer allowed an accurate measurement of its resistance. The device was completely immersed inside a beaker containing Flutec PP3 [90]; Flutec PP3 is a high thermally conducting but electrically insulating solution, which allowed an isothermal environment across the device. The beaker was then placed on top of a hot plate, heating up the solution from 25°C to 47°C while the voltages from both the thermometer and the calibrated resistor were monitored. The temperature inside the Flutec was measured by a commercial calibrated thermometer with a resolution of 1°C. As the resistance is proportional to temperature for a metal, this allows the temperature to be determined once calibrated. Figure 4.10, shows a schematic illustration of the thermometer calibration.

From these measurements, the temperature coefficient of resistance (TCR) of the resistive thermometers, β is determined through Equation 4.1:

$$R_2 = R_1(1 + \beta(T_2 - T_1)) \quad where, \quad \beta = \frac{\Delta R}{\Delta T}\frac{1}{R_0} \tag{4.1}$$

The typical value obtained for the Ti/Pt or Ti/Pd thermometers was $0.00205 \pm 0.00006\,1/\mathrm{K}$. The error reported is the standard deviation of ten different calibrations performed at dif-

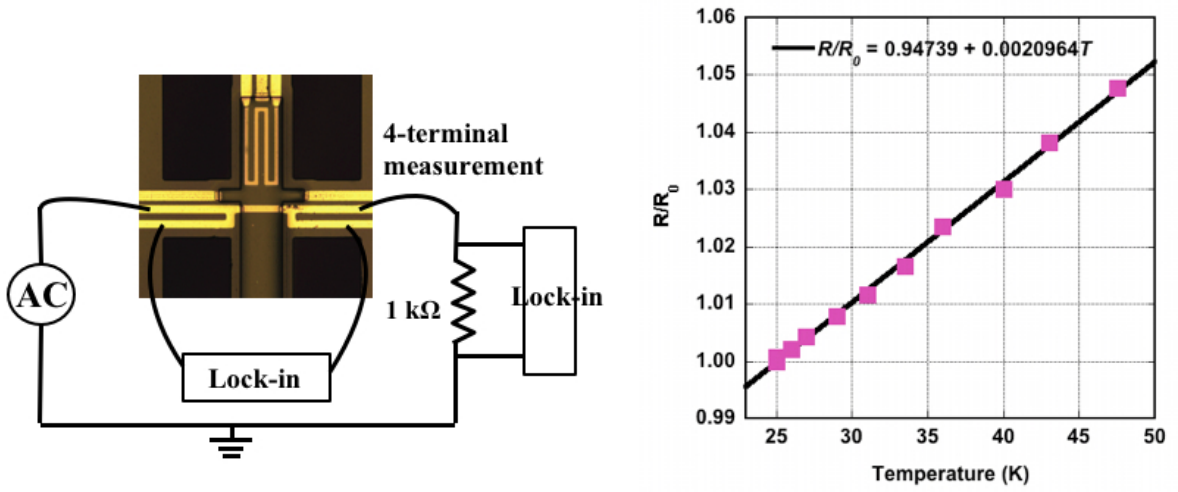

Figure 4.10: A schematic illustration of a calibration done for one of the thermometers patterned on top of a Hall bar device. The resistance measured has been plotted as a function of the temperature, giving in this case a TCR of 0.00209 1/K.

ferent temperatures. This value shows and error lower than 3% indicating a good precision technique and repeatability.

Once the calibration was done, a temperature gradient was generated to the structure by Joule heating through applying a direct current (dc) to one of the NiCr heater. In this case the sample was not immerse in Flutec and the measurement was undertaken at room temperature and at atmospheric pressure. The way of monitoring the thermometer resistance was the same as the one explained above, but in this case the resistance was plotted as a function of the heater power, see Figure 4.11 *a*). The data presented in Figure 4.11, was taken from measuring the device showed in Figure 4.12, when only one of the heaters was being powered by a dc current. We will refer to the 'hot thermometer' for the closest one to the heater being powered and the 'cold thermometer' for the farthest one.

Figure 4.11 *b*) shows the temperature as a function of the heater power after performing the calibration in both, hot and cold thermometers. For this data presented, the distance between the thermometers was 340 μm and part of the heat was confined inside a 10 μm thick membrane, see Figure 4.12. With this kind of geometry a heater power of just 15 mW, was enough to produce a temperature difference of 30 K within the structure. Detailed characterisation to determine the thermal conductivity and Seebeck coefficient on the two different devices is explained in Chapter 5 and 6.

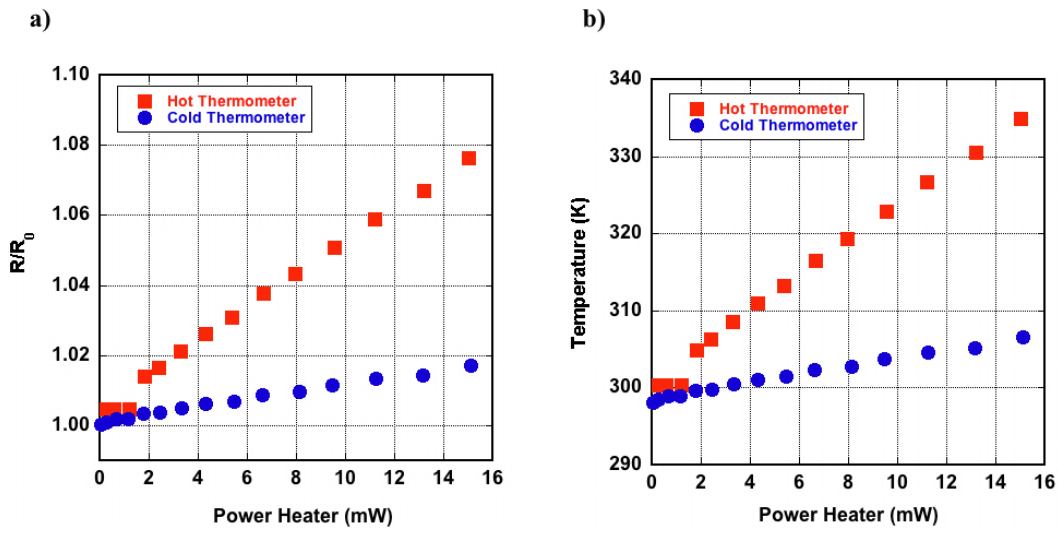

Figure 4.11: *a*) Shows the resistance of the hot and cold thermometer of a Hall bar device as a function of the heater power. *b*) shows the corresponding temperature for both thermometers after the calibration.

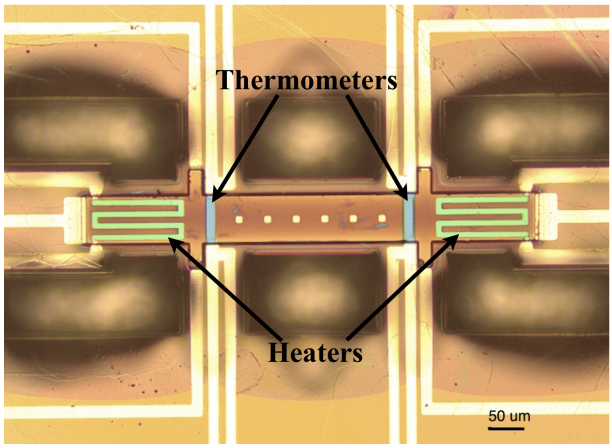

Figure 4.12: An optical microscopy image showing a suspended Hall bar structure with integrated heaters (green), thermometers (metal rectangles placed between the heaters and the markers coloured in blue) and electrical connections (rest of metal lines also coloured in yellow).

4.2.2 Scanning Thermal Atomic Force Microscopy

An Atomic-Force-Microscopy probe (AFM) is used to scan substrate surfaces to produce images with a horizontal and vertical resolution down to the nanometer scale.

The AFM consists of a cantilever with a sharp tip placed at its end. A laser diode points towards the end of the tip producing a light reflection from the cantilever to a sensitive photodiode. The instrument works by measuring the deflection produced on the tip while it is scanning the surface of a substrate, this deflection is sensed by the change of the light reflected. Figure 4.13 shows a schematic diagram of an atomic force microscopy.

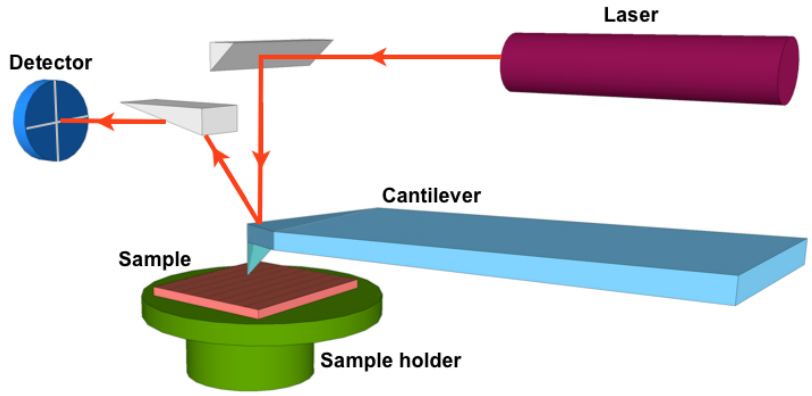

Figure 4.13: Schematic illustration of an AFM instrument.

Thermal atomic force microscopy (ThAFM) combines an AFM probe with a thermal sensing element, so that the temperature can be detected inside the nano and micrometer scale. This technique was used to cross-check the accuracy of the values measured by the resistance thermometry technology. The ThAFM used consisted, of a platinum resistor element placed at the end of an AFM cantilever [92]. The two-contacts Pt sensing resistor were connected to a Wheatstone bridge that worked as a probe amplifier. The micro-fabricated thermal probe was calibrated by a device which measured the Johnson noise in a small NiCr resistor placed a few μm from a target Au dot. As the Johnson noise amplitude is dependant on the temperature, this provides an absolute calibration of the temperature [93]. The thermal probe was placed in contact with the target dot while its calibration, [93]. The probe was scanned in a Digital Instrument VEECO Dimension 3000 AFM system [94], which followed the mechanism showed in Figure 4.13.

The ThAFM was used to check the local temperature of thermometers, the temperature difference and the temperature distribution along the Hall bar devices, [89]. Figures 4.14 *a*) and *b*) show topographic and thermal images for one of the scans along the Hall bar structure when a power of 11.8 mW was applied to one of the heaters. Figure 4.14 *c*)

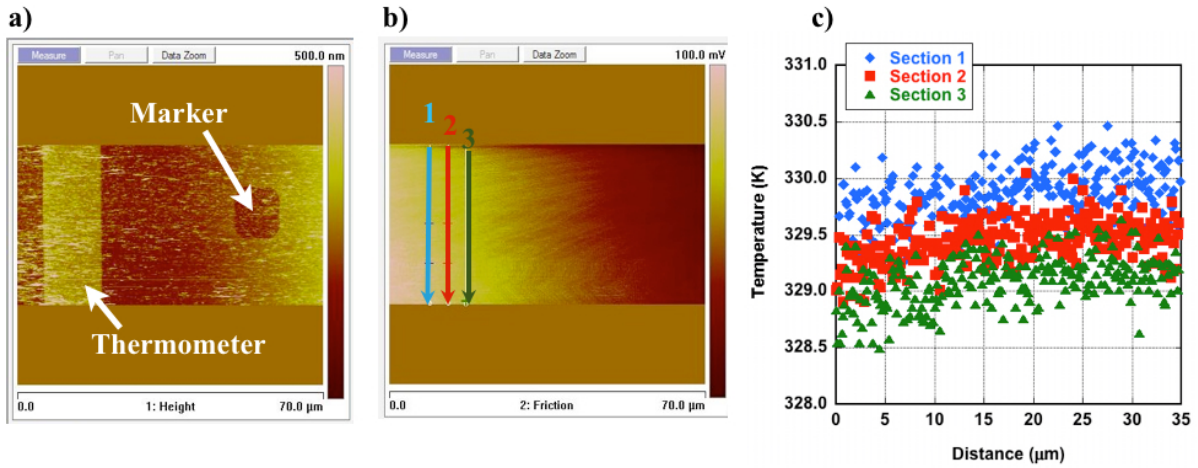

Figure 4.14: *a*) A topographic image of one of the scans undertaken by the ThAFM probe, showing the first thermometer plus the first marker next to it. *b*) Thermal image of the same scan when a power of 11.8 mW was applied to the heater placed at the left of the thermometer. *c*) The temperature versus distance for three different sections (sections 1 to 3) taken along the thermometer to compare the temperature measured by the ThAFM probe and the average temperature given by the thermometer. The three sections and directions are indicated in *b*) by three arrows.

shows the temperature on the thermometer for three different sections indicated in Figure 4.14 *b*) by three arrows. The average temperature measured for these three sections gives a value of 329.5 ± 0.4 K.

The maximum scanning field size by the ThAFM system was of $70\,\mu\text{m} \times 70\,\mu\text{m}$, Figures 4.14 *a*) and *b*) show a scan size of $70\,\mu\text{m} \times 35\,\mu\text{m}$. To scan the entire structure between the two thermometers ($340\,\mu$m), the tip was relocated using periodic markers patterned in the center of the Hall bar structure, as shown in Figure 4.12. The temperature scanned along the bar between the two thermometers is plotted in Figure 4.15, where a uniform temperature drop can be seen for the constant heater power of 11.8 mW. The average temperature from the data points of each scan along the bar always showed a standard deviation no larger than 0.25 K.

Figure 4.16 presents a comparison of the temperature difference between the hot and cold thermometers detected by the ThAFM and the resistive thermometry technique. The difference between the two measurement techniques was less than 4% in the experiment reported. Both techniques were in good agreement, suggesting that the thermometry

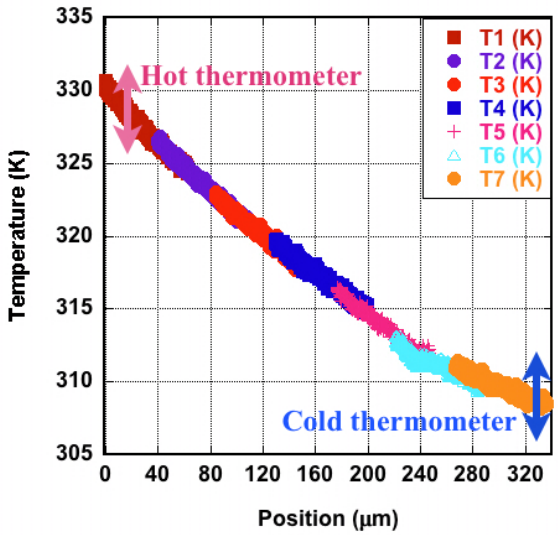

Figure 4.15: Temperature measured along the Hall bar between the two thermometers by a ThAFM probe. Seven different scans were made to complete the distance from the first to the second thermometer.

method was a valid technique to perform temperature measurements.

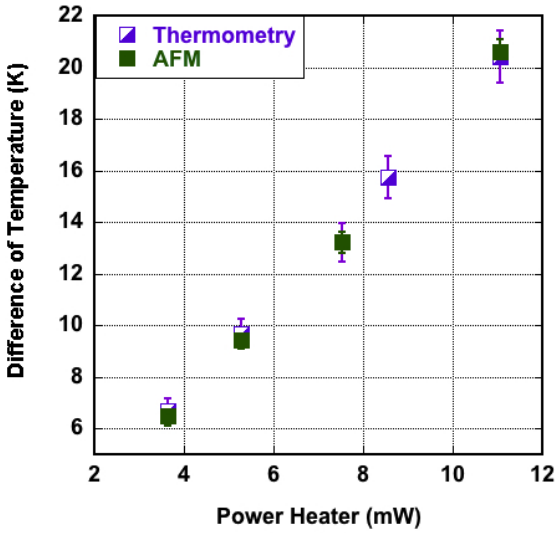

Figure 4.16: The temperature difference between the hot and cold thermometer as a function of the power applied to the heater. The plot shows the data measured by both the resistive thermometry and the ThAFM probe. The difference in the slopes is $\sim 4\%$.

4.2.3 3ω Method

The three-omega method [27, 95, 96] is the most popular technique used in the literature to determine thermal conductivity. This method is based on a metal line with four contacts which work as both, a heater and a thermometer, Figure 4.17 *a*). Driving a sinusoidal current at frequency ω through the metal line heats up the sample creating a thermal wave at frequency 2ω. Due to the temperature dependent resistance of the heater, the resistance also oscillates at twice the frequency. The oscillation of the resistance at 2ω combined with the current at ω, leads to a voltage signal at 3ω [97]. Equation 4.2 [98] shows the temperature oscillation of the metal line, where R is the average resistance, V_1 is the voltage across the line at ω, V_3 is the voltage at 3 times ω and $\Delta T/\Delta R$ is the variation of temperature as a function of resistance. By this technique, increasing the frequency ω can be adapted to measure the thermal conductivity of thin-films on substrates.

$$\Delta T = \frac{2RV_3}{V_1}\frac{\Delta T}{\Delta R} \tag{4.2}$$

Thin-films in general exhibit anisotropic behaviour, thus measuring values of the cross-plane conductivity does not necessarily include the in-plane conductivity. Therefore some

thought needs to be put into the designs of the heaters, [40]. If the heater is very narrow then it acts almost as an isotropic heat source, Figure 4.17 *b*), while if it is very wide compared to the thin film that is trying to be measured then the heat source provides a near 1-dimension uniform heat flow, Figure 4.17 *c*). The first option is used in case of extracting in-plane thermal conductivities while the second one is used for cross-plane measurements.

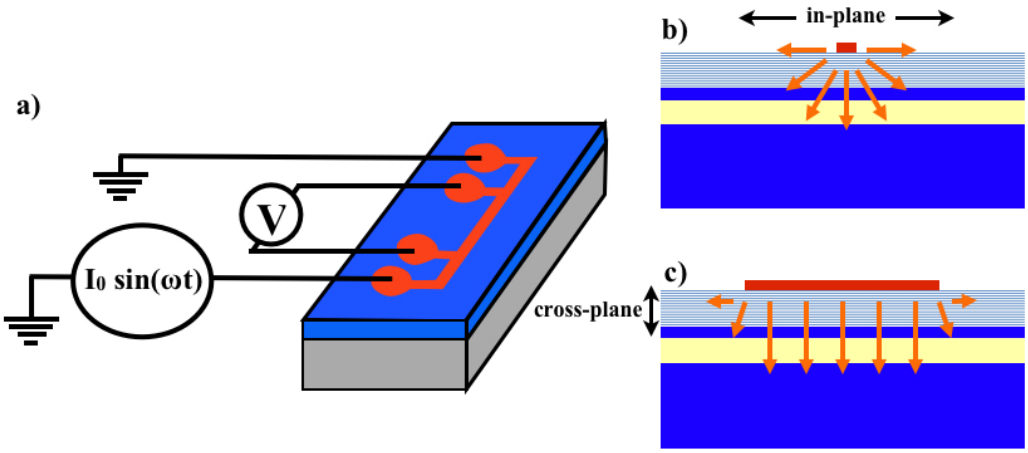

Figure 4.17: *a*) A schematic diagram of the standard 3ω technique. *b*) A cross sectional view schematic of a heater which has a thin width compared to the depth of the thin film to be measured, which provides an isotropic heat source. *c*) Cross view schematic of a heater which width is much wider than the thin film under investigation providing a 1D model for the heat transfer.

If the penetration depth $q^{-1}=\sqrt{D_s/2\omega}$, where D_s is the thermal diffusivity, is considered much larger than half of the heater width (b), $q^{-1} \gg b$, the solution for the temperature rise from the heating strip used within the 3ω technique can be approximated by Equation 4.3, [99].

$$\Delta T(\omega) = \frac{P}{\pi\kappa}\left(\frac{1}{2}ln\left(\frac{D_s}{b^2}\right) + 0.923 - \frac{ln(\omega)}{2} - \frac{i\pi}{4}\right) \tag{4.3}$$

Where P is the power per unit length and κ is the thermal conductivity. Equation 4.3 shows how the thermal conductivity can be extracted from the slope of the real part of the ac temperature amplitude as a function of $ln(\omega)$.

Heaters consisting of 10 nm of NiCr plus 50 nm of Au were patterned by the lift-off technique. The layer of NiCr was used to enhance the adhesion of the Au metal line to the sample. Different widths for the metal lines were used from 5 μm up to 50 μm. Figure 4.18 *a*) shows a four terminal metal line fabricated of 5 μm width and 400 μm length.

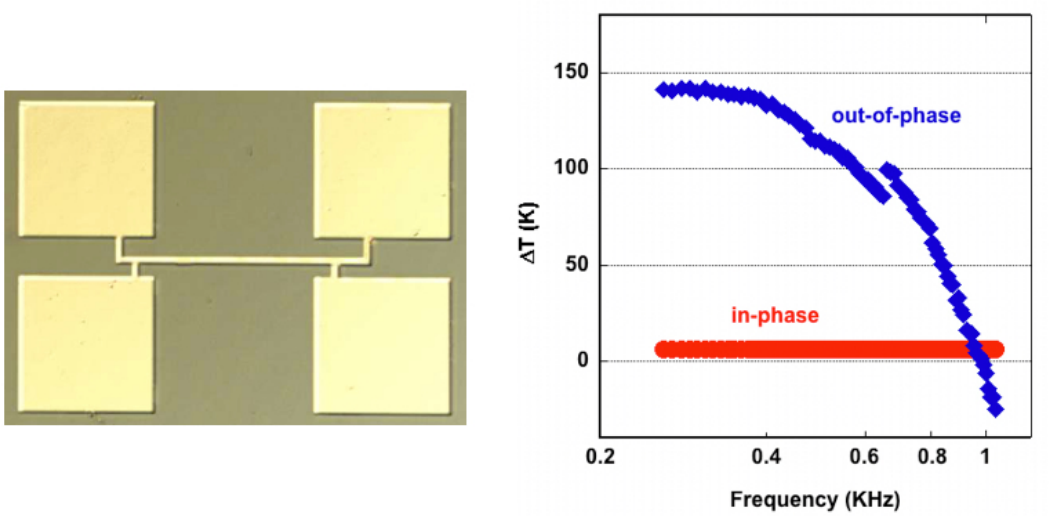

Figure 4.18: *a*) The top view of a heater/thermometer metal line. The line width is 5 μm and line length is 400 μm. *b*) The temperature oscillations of the metal line as a function of the frequency at 1ω.

A dual phase lock-in amplifier was used to drive the device and to scan the voltage across a range of frequencies. This lock-in amplifier was able to read the in-phase and out-of-phase of the voltage signal at the reference frequency selected. Because the voltage at 3ω is a thousand times smaller than the voltage at 1ω, a potentiometer connected in series with the strip line and differential amplifiers were used to cancel the signal created at the frequency 1ω.

Figure 4.18 *b*), shows the in-phase and the out-of-phase collected temperatures vias for bulk p^- Si. For low frequencies (from 250 to 350 Hz) the value for the out-of-phase ΔT was not dependent on the frequency and so stayed constant. This value produced the thermal conductivity result and also the slope of the in-phase ΔT in that range of frequencies. The value measured was $143 \pm 15\,\mathrm{W/m \cdot K}$ which is comparable with literature values of $155\,\mathrm{W/m \cdot K}$ for bulk Si [100].

For the 3ω measurement, the frequency is low and so the thermal penetration depth is much larger than the superlattice thickness under investigation, being the measurement affected by other layers buried underneath the thin film. Figure 4.19 shows the calculated penetration depth of the 3ω technique from one of the superlattice structures as a function of the frequency ω. The penetration depth was calculated weighting the thermal diffusivity average of every layer included in the design. The plot showed that it was necessary to go up to 60 kHz in order to get a penetration depth lower than 10 μm, the usual thickness of the superlattices. The capability of our lock-in amplifiers could only go up to $3\omega = 100$ kHz.

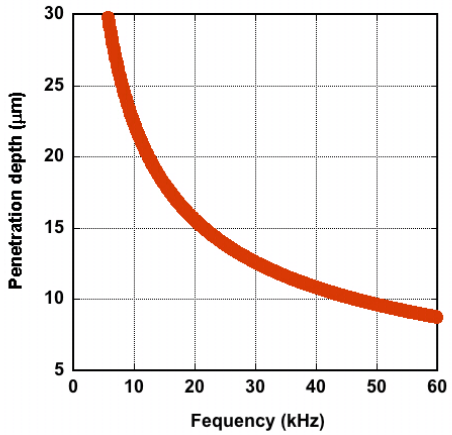

Figure 4.19: The weighted average of the penetration depth for the 3ω technique in one of the superlattice structures as a function of the frequency, ω.

A differential technique [27, 101, 102], where the film under investigation is between the top heater and the consecutive layers under it, can be used in this case, see Figure 4.20. In this technique a second heater is placed on top of the layer under the thin film, which will be used as a reference temperature. The temperature oscillation given by the heater on top of the thin-film and substrate is given now by Equation 4.4, [99]:

$$\Delta T(\omega) = \frac{P}{\pi \kappa_s}\left(\frac{1}{2} ln\left(\frac{D_s}{b^2}\right) + 0.923 - \frac{ln(\omega)}{2} - \frac{i\pi}{4}\right) + \frac{P d_f}{2b\kappa_f} \tag{4.4}$$

where κ_s is the thermal conductivity of the substrate, κ_f is the thermal conductivity of the thin film and d_f is the thickness of the thin film. The first term of the Equation 4.4

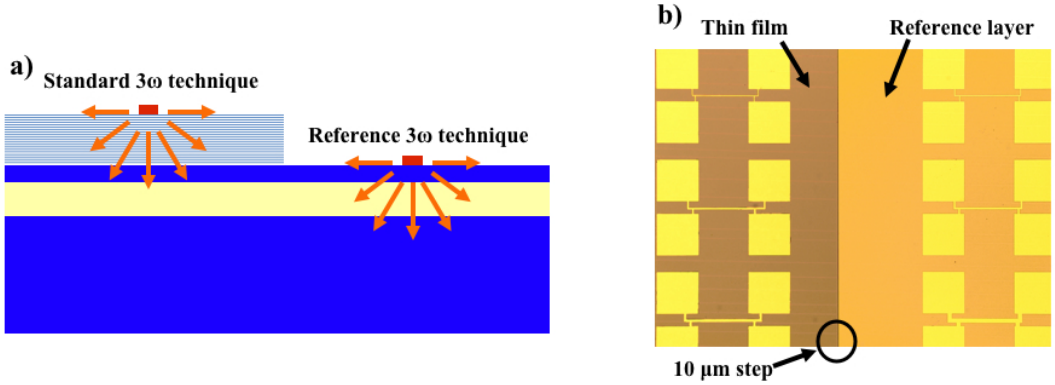

Figure 4.20: *a*) A cross view schematic diagram of a differential technique, where there are two metal strips, one on top of the thin film and then another on top of a reference layer. *b*) Shows a top optical image of a sample, where half of it has been etched for 10 μm until reaching the reference layer.

is extracted from the reference temperature using the heater just on top of the substrate and hence the thermal conductivity of the thin film can be extracted as Equation 4.5:

$$\kappa_f = \frac{Pd_f}{2b(\Delta T_{s+f}(\omega) - \Delta T_s(\omega))} \tag{4.5}$$

This technique was used in a number of samples to calculate the in-plane thermal conductivity of one of the superlattice designs. Four different samples (1x1 cm^2) from the same region of the wafer to assure similar layers thicknesses were selected. The superlattice structure of two of those samples was etched away until reaching the buffer layer so that they could be used as reference samples. Identical heaters were fabricated on top of the 2 SL samples and on top of the 2 reference samples, and measurements using the same settings and conditions were performed in all of them. The thermal conductivity from each 2 group of samples measured, was different in every case producing an error higher than 50%.

One of the requirements is that the buffer thickness and composition should be the same so that a differential technique can be used. As it has been explained in Chapter 3, all the designs characterised within this work were grown by a LEPECVD tool. The plasma in this tool is defined for having a bell-shaped inhomogeneity, which varies the growth rate over a 100 mm wafer. This means that there were locally inhomogeneities when processing close samples from the same wafer. It was believed that this variability

of the buffer layer and composition was affecting the measurement suggesting that this technique was not suitable for the material under investigation.

4.2.4 Hall-Effect

The Hall effect measurement technique is used to calculate the resistivity, the carrier density and the mobility of semiconductor materials, [6]. The model of the Hall effect consists of an electrically conducting material through which a uniform current is driven in the presence of a perpendicular magnetic field externally applied. Because of the presence of the magnetic field, charge carriers will deflect to one side of the sample through the Lorentz force, producing a voltage perpendicular to both the driven current density and the applied magnetic field, see Figure 4.21.

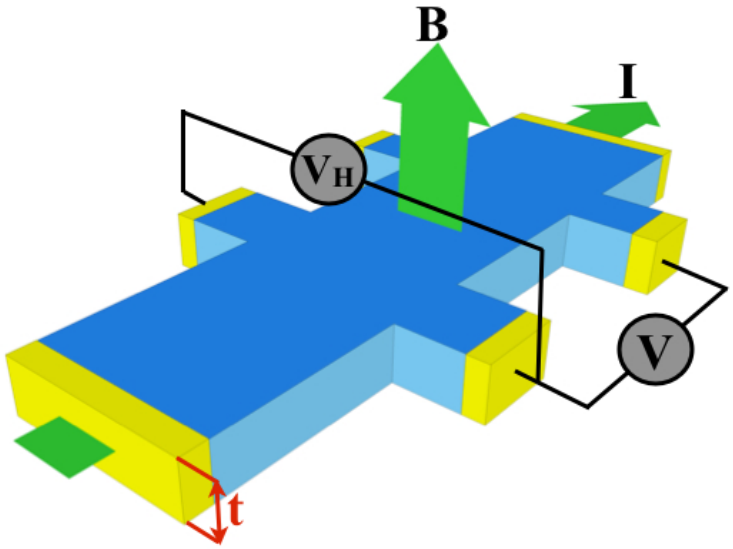

Figure 4.21: Shows a schematic diagram of a Hall bar device, where a current is driven perpendicularly to an external magnetic field applied to the structure. A Hall voltage perpendicular to both is produced in return.

The Hall coefficient and the resistivity are then defined by R_H and ρ respectively, see Equation 4.6:

$$R_H = \frac{t}{B}\frac{V_H}{I} \quad and \quad \rho = \frac{V}{I} \tag{4.6}$$

where t is the thickness of the Hall-bar and B is the magnetic field applied, see Figure 4.21. The ratio between the Hall coefficient and the resistivity measured, gives the mobility of the material under test.

The usual structures to determine the mobility of the material are Hall-bar and van-der-Pauw geometries, [103]. A 6-contact Hall bar, as the one shown in Figure 4.21, was used to determine the mobility of the lateral designs. One of the geometrical considerations for a Hall bar is the tendency of the end contacts to short out the Hall voltage. If the ratio between the length and the width of the sample l/w is bigger than 3, then this error is less than 1%, as the measured voltage is almost the Hall voltage and therefore no correction is needed, [104]. The Hall bars fabricated were 800 μm long and 85 μm wide, given this geometry a ratio bigger than 9 and therefore this geometry resulted in an uncertainty lower than 1%.

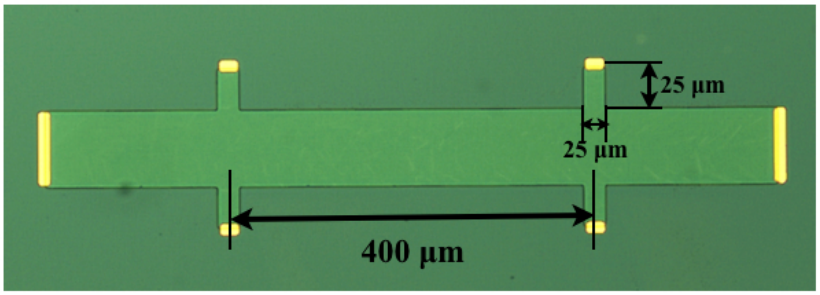

Figure 4.22: A top view of a 6-contact Hall bar. The whole device has been passivated by silicon nitride and just small windows at the end of each arm has been etched in order to create the contacts once the metal is deposited.

The whole device was passivated by a thin layer of Si_3Ni_4 and only $10\,\mathrm{x}\,10\,\mu m^2$ windows were opened at the end of the arms to make the contacts. Figure 4.22, shows a picture of a Hall bar where the Si_3Ni_4 windows had already been etched to create the contacts.

4.2.5 Transfer Line Method

A transmission line method (TLM) is a two terminal test structure which allows extraction of the contact resistance, R_c and the contact specific resistance, ρ_c through the linear relation between the resistance measured and the spacing between the contacts [6].

This structure consists of identical contacts of length L and width W, which are spaced by different distances d_i. A mesa structure of width Z is etched on the thin film under characterisation and the TLM structure is patterned on top of the mesa. The mesa structure is created to assure a homogenous distribution of the current density under the contacts, see Figure 4.23 a).

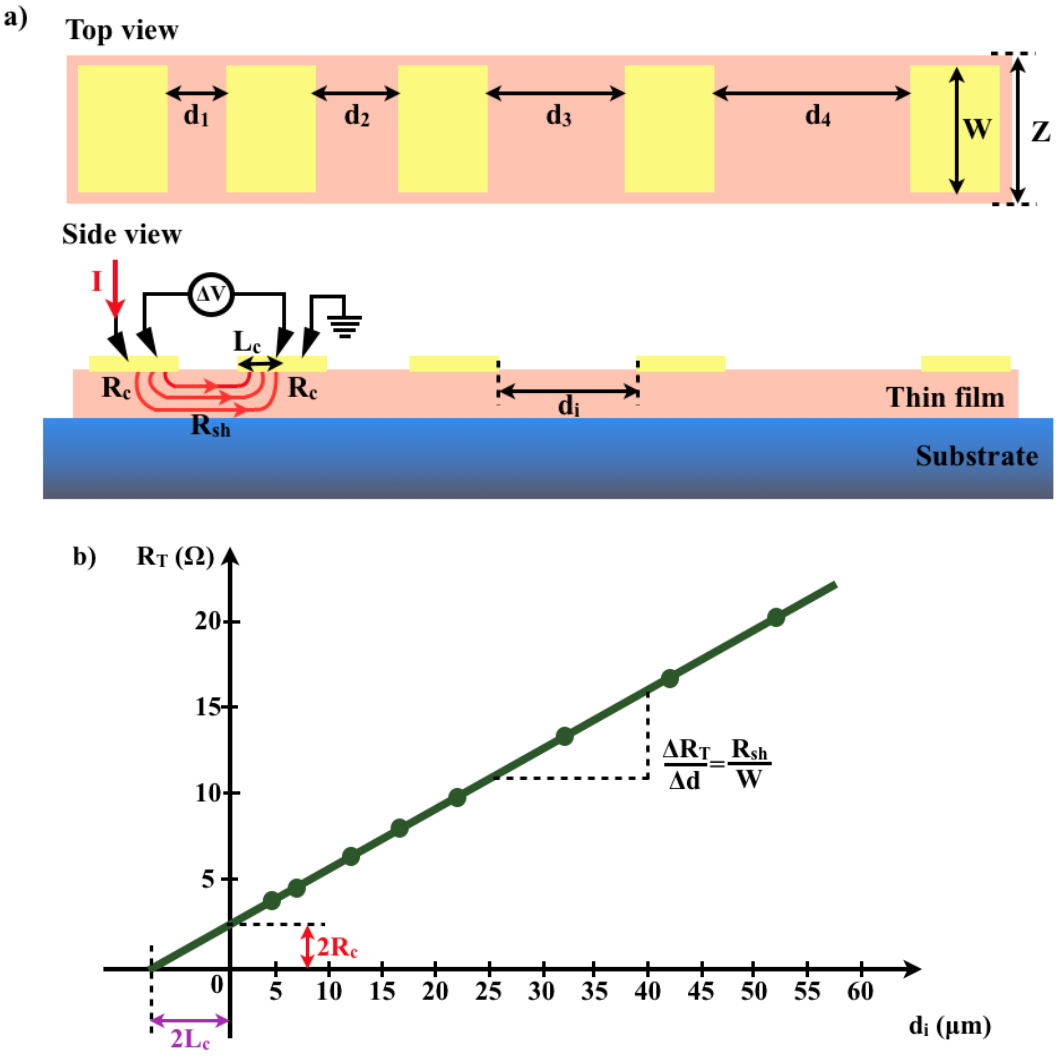

Figure 4.23: a) A schematic diagram of a TLM structure patterned on top of a mesa structure of width Z. b) Representative data from a typical TLM structure, where the resistance measured by a pair of two consecutive contacts is plotted as a function of the gap spacing between them.

A current is driven between two consecutive contacts by a pair of probes and the voltage dropped is measured by another pair of probes. Assuming that R_c is the same for all the contacts, the measured total resistance is given by Equation 4.7 [6]:

$$R_T = \frac{R_{sh}}{W} d_i + 2R_c \tag{4.7}$$

where R_{sh} is the sheet resistance of the semiconductor.

Figure 4.23 *b*) shows a plot of the linear relation given by Equation 4.7. R_{sh} is calculated by the slope of the curve times the contact length, W and 2 times the length of current transfer at the contact, $L_c = \sqrt{\frac{\rho_c}{R_{sh}}}$, can be extracted when $R_T = 0$. The electrical conductivity (σ) of the thin film can be calculated as $\sigma = \frac{1}{tR_{sh}}$, where t is the thickness of the thin film.

The common disadvantage of a linear TLM is that when $Z \neq W$ the distribution of the current density is not homogenous at the edge of the contacts, which results in an underestimation of the contact resistance. To eliminate this problem a circular TLM (CTLM) test structure can be used.

In this case, the structure consists of metal circular pads of radius r, which are differently spaced d_i from metal regions surrounding the inner pads, see Figure 4.24. This circular geometry eliminates the need to isolate the metallisation structures by etching, which makes the fabrication quicker as only a one step mask/lithography is required.

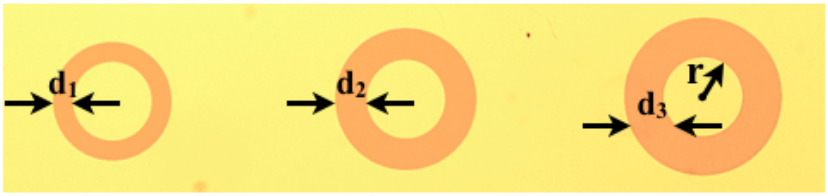

Figure 4.24: The top optical view of an array of CTLMs. The inner metal pad has a radius of 50 μm and the spacings change from 10 μm, 20 μm to 50 μm.

A current is forced between the inner and outer metal pads by two probes and the voltage dropped is again measured by another pair of probes. The different gap spacings give different readings for the total resistance, which values can be plotted again as a function of the distance between the pads. The measurements taken by a ring geometry can be reduced to a standard linear TLM model including a correction factor to compensate

the difference between the two layout geometries [105]. The total resistance measured in this case is described by 4.8 [6]:

$$R_T = \frac{R_{sh}}{2\pi r}(d_i + 2L_t)C \tag{4.8}$$

where the correction factor C is defined as:

$$C = \frac{r}{d_i} ln\left(1 + \frac{d_i}{r}\right) \tag{4.9}$$

Figure 4.25 shows the original data taken when testing all the different structures plus the corrected data after applying the correction factor. The way of extracting all the parameters is the same as the one explained for the linear TLM, which has also been indicated in Figure 4.25.

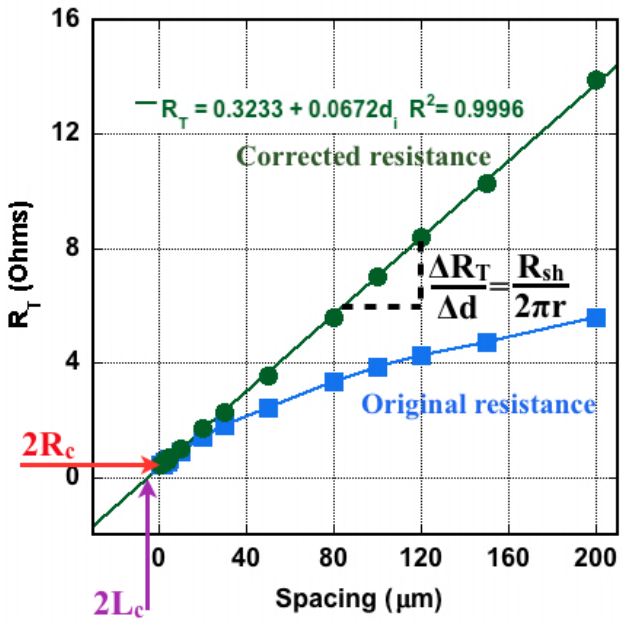

Figure 4.25: The total resistance measured and corrected as a function of the gap spacing. $R_c = 161.6\,\mathrm{m\Omega}$, $L_c = 2.4\,\mu\mathrm{m}$ and $R_{sh} = 21.1\,\Omega$.

A modified technique for the CTLMs was used in order to characterise some of the designs studied within this work. This technique is explained in detailed and discussed in Chapter 6.

4.3 Chapter Summary

The fabrication techniques used to develop individual processes in order to fabricate the final devices have been explained in detail. The different micro-fabricated devices consisted of etched mesas with thicknesses varying from 4 to 10 μm. Therefore, photolithography was used to fabricate the different devices and thick resists were required to create uniform coatings on top of the mesa structures. Different etching recipes had to be developed to create anisotropic etches on the superlattices using an STS-ICP tool. Depending on the device fabricated, either positive or negative slopes were required at the side walls of the mesas and so these processes have been stated and explained in the course of this chapter. The steps followed to fabricated the final devices are listed in Chapter 5 and 6, making reference to the processes explained in this chapter.

In order to thermally and electrically characterise the devices, various techniques used for characterisation have been introduced. Later, in chapters 5, 6 and 7, the results for superlattices characterised using these techniques are presented and considered.

Chapter 5

Thermoelectric Characterisation in the in-plane direction for $Ge/Si_{1-x}Ge_x$ Superlattices

In this chapter, the study of the in-plane thermoelectric properties of two different $Ge/Si_{1-x}Ge_x$ superlattices is reported. The chapter starts explaining the aim of the investigation with a description of the design of the superlattices. The growth description and the physical characterisation of the material is followed by the fabrication process used to obtain the devices for electrical and thermal characterisation. After a detailed description of the structures, the techniques used to measured σ, α and κ are introduced. The results obtained after data analysis are reported together with considerations about the designs.

5.1 Material Design and Growth

Two p-type $Ge/Si_{1-x}Ge_x$ modulation doped superlattices, where the hole transport occurs parallel to the Ge QWs and the heat transport occurs along the superlattice, have been investigated as a function of QW-width for samples with different Ge concentration in the barriers [9, 106].

As explained in Section 2.4, the modified density of states in a 2D system should increase the Seebeck coefficient over 3D systems [35]. This enhancement of the Seebeck coefficient, combined with δ-doping to improve carrier mobilities [5, 62], should significantly increase the power factor of the material.

$Si_{1-x}Ge_x$ barriers were chosen to reduce the lattice thermal conductivity of the material. As reported in [14] the thermal conductivity of $Si_{1-x}Ge_x$ alloys is $\sim 5\,W/m \cdot K$ (provided $0.2 \leqslant x \leqslant 0.8$), which value is significantly lower than bulk Ge ($\kappa = 60\,W/m \cdot K$) [14]. The thickness of the barriers in both designs were twice the thickness of the Ge QWs. The averaged weighted thermal conductivity of the superlattice for these designs (see Figure 5.1) showed a total value of $\sim 20\,W/m \cdot K$, suggesting that the total κ was dominated for the SiGe matrix [11].

Ge was selected to form the QWs of the superlattices, for obtaining p-type electrical conductivities and Seebeck coefficients with a factor of 3.2 and 1.9 higher than p-type Si (as shown in Table 1.1 in Chapter 2, for comparing thermoelectric properties).

A self-consistent Poisson-Schrödinger solution showed that $\geq$90% of the carriers, assuming that no segregation or diffusion occurs during the growth, were confined inside the Ge QWs for these two designs at 300 K [9].

Previous work performed by J. Watling and D. Paul in [11], studied the three thermoelectric properties which define the efficiency of a material as a function of threading dislocation density (TDD). The study showed that for TDD $\geq 10^8\,cm^{-2}$ the scattering mechanism for charge carriers was dominated by the dislocation scattering, decreasing the electrical conductivity while the Seebeck coefficient was close to its saturated value. The results suggested that ZTs of ~ 1 could be achieved at room temperature provided a TDD of $10^6\,cm^{-2}$ could be obtained.

As Ge has a larger lattice constant than Si, the multi quantum-well (MQW) structure had to be strain symmetrized requiring a strain relaxation buffer layer. The samples were grown using a LEPECVD tool, described in Section 3.2.2.1. As mentioned in Section 3.2.3, LEPECVD growth can create buffer layers with low TDD values of $10^6\,cm^{-2}$ depending on the Ge content desired for the active layer. Unfortunately, for these values of TDD the required buffer layer thicknesses could vary from 10 to 12 μm, making them unsuitable for in-plane thermal characterisation. Having such a thick buffer layer would constitute a potential parallel path for the heat to flow when performing thermal measurements, therefore a thin buffer layer 10 times thinner than the active layer had to be optimised for these designs [7].

The samples were grown on 100 mm diameter silicon-on-insulator (SOI) substrates, featuring a 1 μm thick SiO_2 layer buried underneath 340 nm thick Si layer.

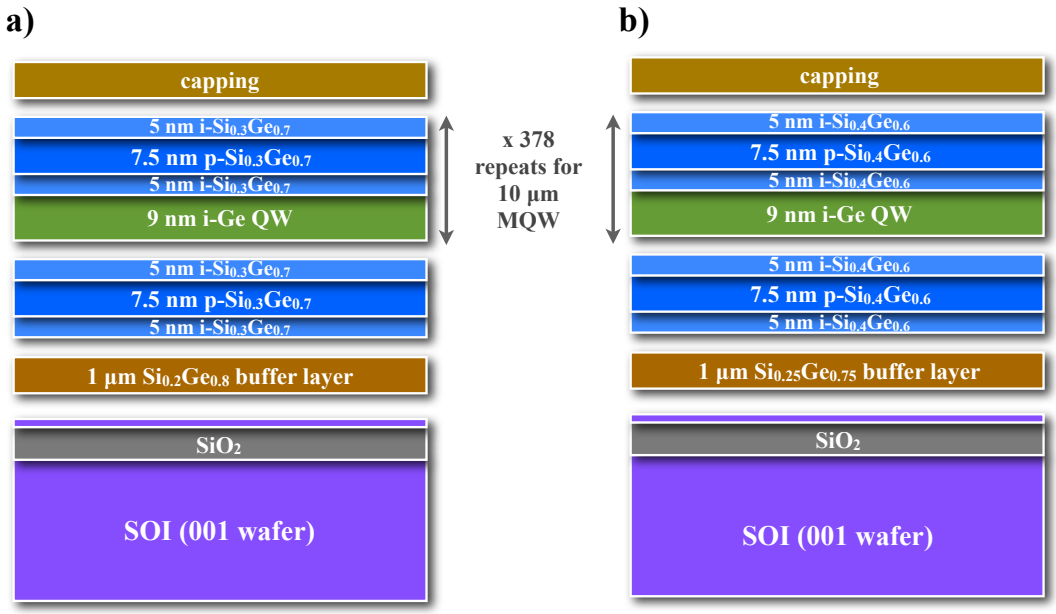

Figure 5.1: *a*) and *b*) schematics of the sample structure for design 1 and design 2, respectively. Both schematics show a strain-symmetrized superlattice grown on top of a relaxed buffer layer on a SOI substrate [7].

For Design 1, a 1 μm thick relaxed $Si_{0.2}Ge_{0.8}$ buffer was grown at 5.5 nm/s at 525°C. The MQW structure was deposited on top of the buffer layer at a growth rate of 1.4 nm/s and a substrate temperature of 475°C. The structure consisted of 378 repetitions of 9 nm compressively strained i-Ge QW and 17.5 nm tensile strained $Si_{0.3}Ge_{0.7}$ barriers [8]. Figure 5.1 *a*) shows a schematic of Design 1, showing the MQW structure grown on top of 1 μm thick buffer layer on top of a SOI substrate.

Design 2, featured for a 1 μm thick relaxed $Si_{0.25}Ge_{0.75}$ buffer layer. In this case the active layer consisted of 378 repetitions of 9 nm i-Ge QW and 17.5 nm of $Si_{0.4}Ge_{0.6}$ barriers. Figure 5.1 *b*) shows a schematic of Design 2, showing the MQW structure plus its correspondent buffer layer grown on top of a SOI substrate.

In both designs the barriers had a doping level of $1x10^{19}$ cm^{-3} and since the nominal thickness of a single period (QW + barrier) was 26.5 nm for both designs, 378 repetitions were required to grow 10 μm thick active layers, so that the electrical and thermal

contributions of the buffer layer and top Si substrate of the SOI could be minimal.

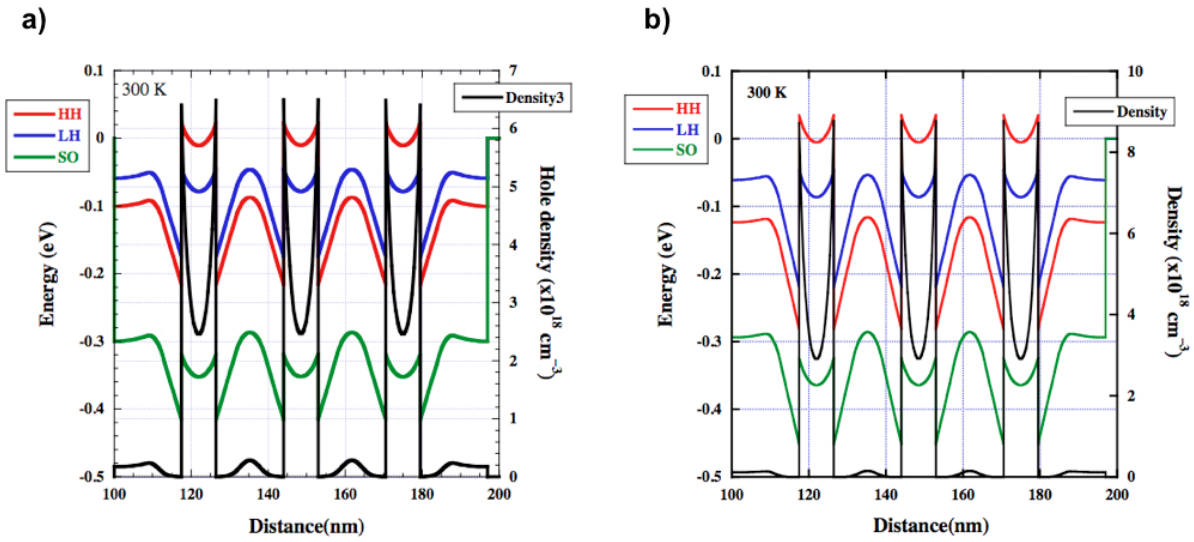

Figure 5.2: A self-consistent Poisson-Schrödinger solution showing the valence band profiles for Design 1 *a*), and Design 2 *b*). The effective mass calculation of the expected hole density is also shown in both graphs (black solid line) showing that more than 90% of the carriers are confined in the Ge QWs.

Figure 5.2 shows the valence band profiles for Designs 1 *a*), and Design 2 *b*). The carrier density for both designs along the QWs and barriers has also been plotted for both designs indicating that 90% of the carriers are confined inside the QWs at 300 K. It has to be pointed out that in this calculation no segregation or diffusion effects in the growth have been considered. Segregation and diffusion during the growth would produce wider QWs than the designed ones, producing subband states lower in energy and closer together to the QWs. Design 2 (Figure 5.2 *b*)) presents larger valence band offsets but also higher interface roughness than Design 1 (Figure 5.2 *a*)).

5.1.1 Physical Characterisation

As introduced previously, low TDD were required to increase the value of ZT. Scanning transmission electron microscopy (TEM) was used to extract the TDD of the samples as well as to inspect the heterostructure periodicity, interfaces and roughness. For both p-type designs studied within this work a range of TEM images from both materials were

used to count the number of threads and determine TDD values between 1 and 5x10^9 cm^{-2} [9].

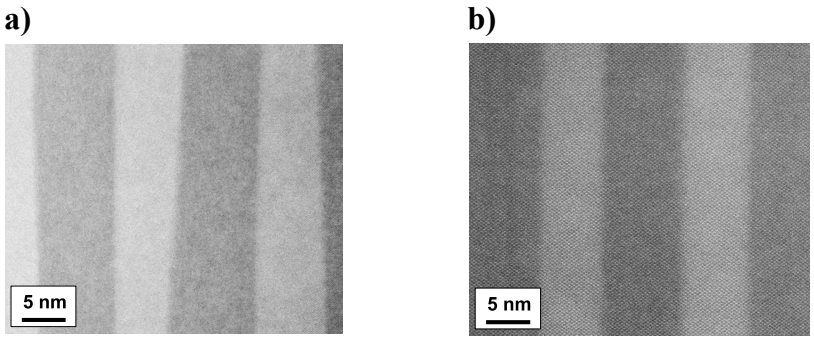

Figure 5.3: *a*) TEM image showing the bottom layers of the superlattice where the thickness variation is visible. *b*) TEM image showing the top layers of the superlattice with the thickness variation almost negligible, showing flat interfaces. Images taken from [8]

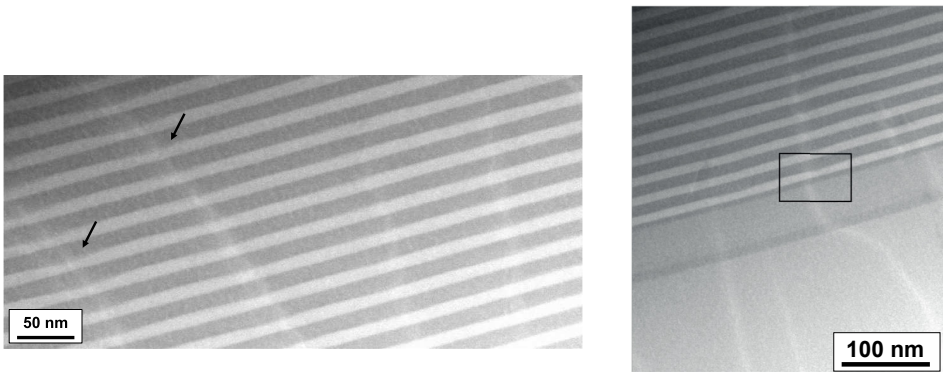

Figure 5.4: Two TEM images showing a range of MQW and some threading dislocations. Threading dislocations seem to reduce the thickness of local QW regions close to them, this reduction of QW thickness was compensated by wider barriers that tended to flatten the surface again [8, 9].

Under TEM inspection, undulation along the growth direction of the superlattices was found. This undulation featured a thickness variation between 2 and 4 nm for the bottom layers of the superlattice, reducing to a variation between 1 and 2 nm after 1 μm of grown material. The top layers of the superlattice were found to have almost flat interfaces.

Figure 5.3 *a*) and *b*) show the bottom and top layers of a superlattice, with the thickness variation clearly visible in *a*) presenting almost flat interfaces in *b*) (growth direction from left to right). The images also suggested that local regions close to threading dislocations tended to reduce the QWs thicknesses, compensated by wider barriers that helped to flatten the MQW structure. Thickness reduction in local QW regions close to threading dislocations, is quite visible in the TEM images shown in Figure 5.4.

On the other hand, the LEPECVD tool presents a non-uniform growth rate over a 100 mm wafer and consequently, the period of a MQW structure can vary from the designed thickness by 1.3 at the center of the wafer or by a factor of 0.8 at the edge of it. Knowledge of the exact thickness of the superlattice, depending on the 1x1 cm^2 piece selected from a 4 inch wafer, was required to fabricate the devices for thermoelectric characterisation.

In this case, high-resolution x-ray diffraction (HRXRD) was used as a routine process to investigate the period thicknesses and material quality [2]. 100 mm wafers were mapped by taking (004) ω-2θ scans on a 1x1 cm^2 grid. Figure 5.5 shows the period map for the p-type Design 1 wafer defined in Figure 5.1 *a*). The nominal thickness for this wafer was 26.5 nm and as shown in Figure 5.5, the period thickness ranged from 24.5 nm at the center of the wafer to a minimum of 10 nm at the edge of it meaning a reduction of 5.42 μm for the full MQW structure.

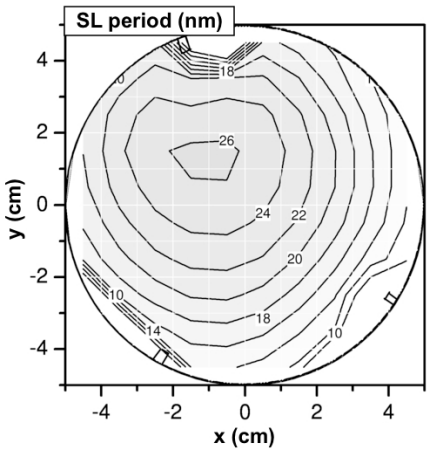

Figure 5.5: Period map for a 4-inch wafer. This wafer corresponds to the p-type Design 1 defined in Figure 5.1 *a*).

To extract individual layer thicknesses, such as QWs and barriers, and to extract Ge

compositions, ω-2θ scans around the symmetric (004) reciprocal lattice point were taken. The intensity peaks along Q_z were then fitted by scattering theory simulations and so accurate data for the barriers and QWs could be extracted [8, 9, 107]. Figure 5.6 shows the data taken from a scan made at the center of the wafer plus the fitted curve from the simulations. In this particular case an average Ge content of 82%, a QW thickness of 9.21 nm and a barrier thickness of 16.19 nm were extracted.

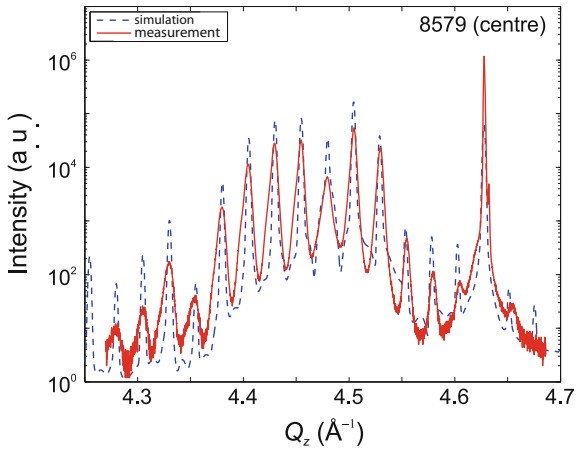

Figure 5.6: ω-2θ scans around the symmetric (004) reciprocal lattice point with fitted data simulation at the center of wafer 8579 (p-type Design 1) [8].

This analysis was repeated for different positions across the wafer to extract information of the individual layers and build a full map by the evaluation of 10 1x1 cm^2 pieces. Figure 5.7 shows the QW, barrier and period thicknesses as well as the Ge content for barriers and buffer layer, as a function of position across the wafer.

The thickness values measured by both, HRXRD and TEM were in good agreement. Table 5.1 demonstrates a comparison between the period measured by both techniques in three different samples across wafer Design 1, the difference of the results was less than 5% [2].

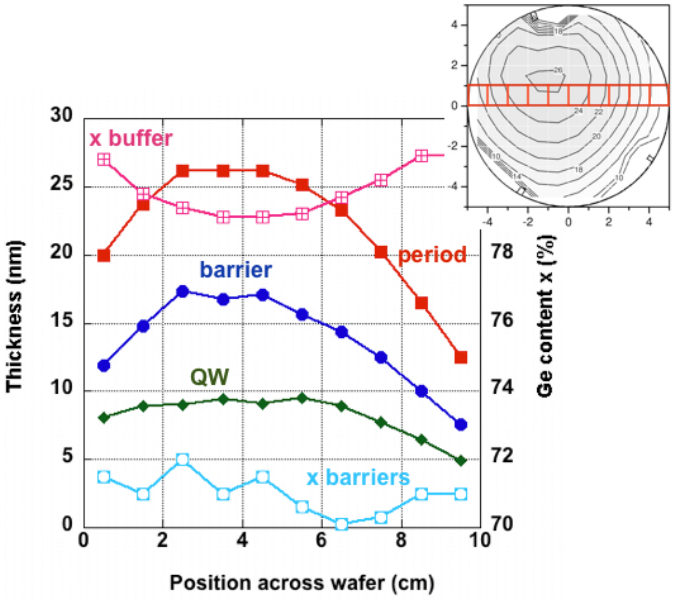

Figure 5.7: QW, barrier and period thicknesses as a function of the position across the wafer. The plot also shows the Ge content for the buffer and for the barriers as a function of position.

Sample ID	TEM Period (nm)	HRXRD Period (nm)
Sample 1	25.0±0.5	25.7±0.1
Sample 2	16.9±0.5	17.7±0.1
Sample 3	21.2±0.5	20.9±0.1

Table 5.1: Period thicknesses measured for three different samples across wafer Design 1. Sample 1 corresponds to a sample from the center of the wafer, Sample 3 to a sample from the edge of it and Sample 2 was picked between the center and the edge of the wafer. This results are matched to the period map showed in Figure 5.5. The periods were measured by HRXRD and TEM, with a difference less than 5% [2].

5.2 Device Characterisation

To measure the thermoelectric properties of 10 μm thick superlattices, where the holes propagated along the quantum wells, it was necessary to fabricate devices inside the micro-meter scale to extract σ, κ and α.

Due to the non-uniformity of the wafer, it was necessary to fabricate devices where the three properties could be extracted from a single device to extract reliable measurements of the efficiency and power factor. These devices needed to confine and propagate a uniform heat flux along the superlattice. This required the removal of the Si substrate which would act as a potential parasitic path for the heat to flow through. Figure 5.8 shows two schematics of a lateral device where heaters and temperature sensors are placed on top of the heterolayer structure to perform thermal measurements, and where parallel heat channels underneath the superlattice had been removed. These diagrams also show the metal contacts made to the structure, which were deposited so that Seebeck voltages and electrical conductivities could be measured.

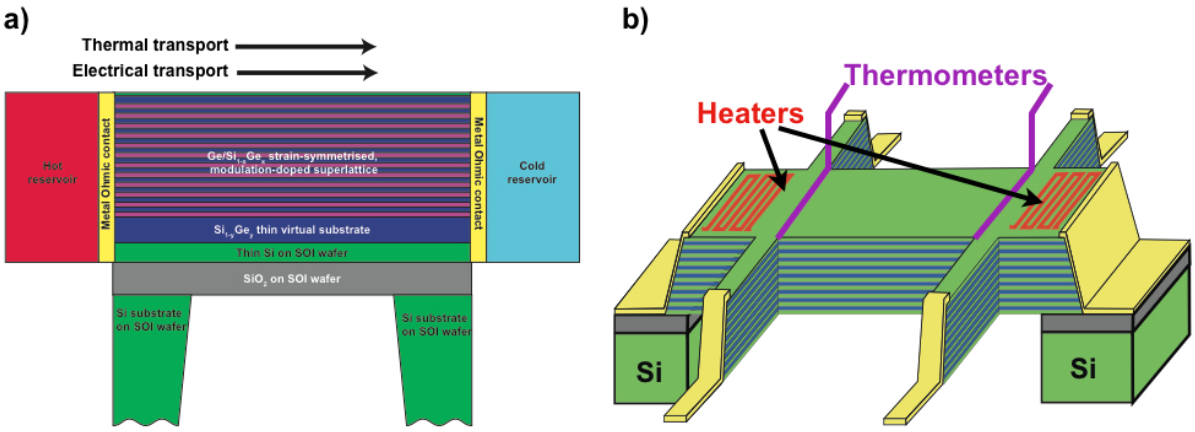

Figure 5.8: Schematics of a lateral structure where σ, κ and α can be measured from a unique device.

A number of possible devices and techniques could have been used to characterize the in-plane properties. The 3ω method [72, 98, 99] is the most popular technique used in the literature to determine the thermal conductivity of thin films and ThAFM [92] is another powerful technique (available in our laboratories) to extract accurate values of κ. Unfortunately, these techniques do not have the capability to measure the value of the electrical conductivity and the Seebeck coefficient, which would require the fabrication of devices on different samples to perform those measurements, and therefore increase the overall uncertainty of ZT. In addition, the 3ω method was found not to be a suitable technique because it is unable to provide credible results of our material due to growth inhomogeneity, refer to Section 4.2.3 for more details.

C. N. Liao [108] presented a test structure to measure Seebeck coefficients but again this would have meant performing measurements on different pieces of material. Authors in [45, 109] presented devices to measure all the required parameters on a single device. In particular, J. de Boor and V. Schmidt [109] suggested van der Pauw structures as an accurate method to extract all the coefficients, however electrical conductivities could have an uncertainty up to 100% if the geometry and, in particular, the ohmic contacts to the structure were too large.

Following the schematic presented in 5.8, a 6-contact Hall bar with integrated heaters and thermometers was chosen to extract all the parameters. Figure 5.9 *a*) shows a top optical view of one of the Hall bar devices fabricated, with 6-contacts to measure σ and with heaters and thermometers to measure α and κ. Two heaters were integrated on each end of the Hall bar, so that the heat transport could be measured in both directions along the bar to check consistency. The Si substrate was removed to avoid heat leakage in the substrate, Figure 5.9 *b*) shows a SEM image of a 10 μm thick superlattice where the substrate had been removed.

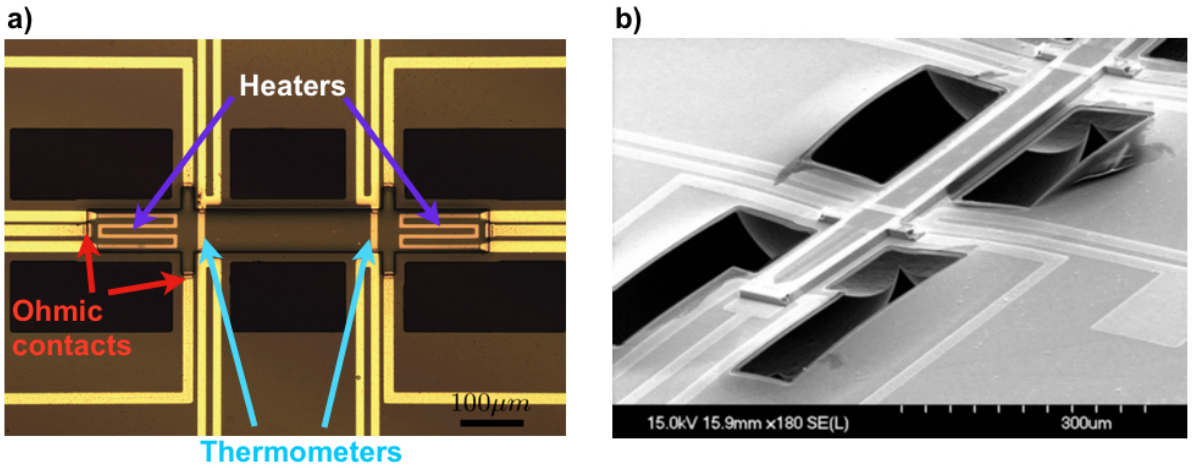

Figure 5.9: *a*) Top view of a 6-contact Hall bar with integrated heaters and thermometers so that σ, α and κ can be measured. *b*) SEM image where it is visible that the device is completely suspended so that the potential thermal influence of the substrate is removed.

The device structure was also able to provide information of the Hall mobility. One of the geometrical considerations for a Hall bar is the tendency of the end contacts to short

out the Hall voltage. If the ratio between the length and the width of the sample l/w is bigger than 3 then this error is less than 1% as the measured voltage is almost the Hall voltage and no correction is needed [104]. The Hall bars fabricated were 800 μm long and 85 μm wide, giving this geometry a ratio larger than 9, refer to Section 4.2.4.

The fabrication steps followed to realise these devices are reported here, while individual processes development are explained in detail in Chapter 4.

1. The first step was to anisotropically etch the superlattice to create a mesa Hall bar structure. A mixed ICP etch in a STS ICP etch tool was used to get a positive slope at the sidewalls of the mesa. This kind of etch was required to guarantee electrical contacts to every quantum well after metal deposition.

2. An RIE tool was used to selectively etch 75 nm of PECVD nitride that had been deposited to isolate the conducting Ge/SiGe superlattice. This nitride was only etched at the end of the six Hall bar arms so that ohmic contacts could be formed by lift-off.

3. Following this etch, 300 nm of Al for ohmic contacts and bond-pads, 33 nm of NiCr for heaters and 10/100 nm of Ti/Pt for thermometers were defined on the structure by lift-off. Sputtering Al was found necessary to assure ohmic contacts over the whole MQW structure and to avoid cuts between bond-pads, heaters and thermometers. A 60 sec anneal at 400°C was used to form the ohmic contacts.

4. The last stage was to remove the substrate from underneath the Hall bar. An isotropic etch was performed from the top of the device using an ICP tool. A photoresist mask was used to protect the full device while large areas around the structure were etched until creating a suspended Hall bar. The superlattices were grown on top of SOI substrates and therefore the SiO_2 box layer was used as a stop layer for the etch.

5.3 Electrical Characterisation: Power Factor

5.3.1 Electrical Conductivity and Mobility

The electrical conductivity was measured using a four-point probe dc measurement on the Hall bar samples from each wafer, in order to remove access resistances. Figure 5.10 demonstrates the results obtained as a function of QW width, all with an error smaller than 0.6%. The errors quoted are the standard deviation from four measurements on the same device, where the symmetry of the Hall bar was used to reverse the current and measure the voltage to check consistency.

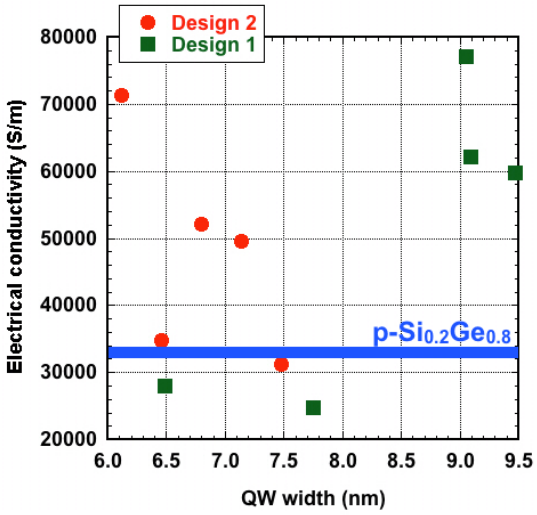

Figure 5.10: The electrical conductivity measured as a function of QW width for the two SL designs and for the reference sample (p-$Si_{0.2}Ge_{0.8}$). All measurements were performed at room temperature.

The electrical conductivity of a reference p-$Si_{0.2}Ge_{0.8}$ sample with the same doping density was also tested for comparison. The value measured corresponded to a σ of $34,900\,\mathrm{S/m}$ (value also plotted in Figure 5.10). The reference sample was grown on the same buffer layer as the one grown for Design 1 and so the TDD was expected to be of the same order of magnitude. Most of the values demonstrated higher electrical conductivities than those measured for the reference sample and for literature p-Ge with a comparable doping level [34].

Design 2, as expected, showed an increase of the electrical conductivities for thinner QWs, while Design 1 showed the complete opposite behaviour. It has to be highlighted than the two values with σ lower than $30,000\,\mathrm{S/m}$ for Design 1 were measured on pieces from the edge of the wafer which could have presented lower material quality.

The high variability of σ could also be explained by high TDD. The electrical conductivity is predicted to sharply decrease for TDD higher than $10^6\,\mathrm{cm}^{-2}$, while the material tested had TDD higher than $10^9\,\mathrm{cm}^{-2}$. Local variations of TDD across the wafer could explain the high variability from one piece of the wafer to another as well as the waviness of the bottom layers showed by TEM could also be a reason to affect the electrical conductivity and mobility of the material.

Hall measurements were performed on the same devices. A current limit of 1 mA through the device and a magnetic field of 0.5 T perpendicular to both current and voltage, were applied in order to measure the Hall voltage. Knowing the Hall voltage, current, magnetic field, geometry and previous electrical conductivities, the mobilities and carrier densities were calculated for each device. Figure 5.11 shows the mobilities and carrier densities measured at 300 K as a function of QW width.

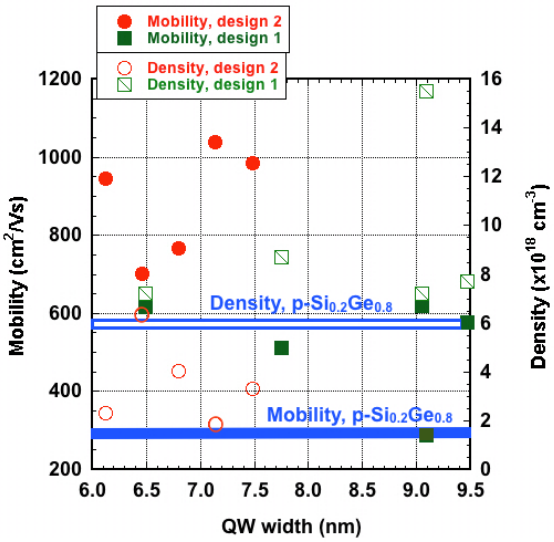

Figure 5.11: Hall mobilities and carrier densities measured at 300 K and plotted as a function of QW width.

Design 2 presents higher mobilities than Design 1, but when compared to PF and ZT (presented later in the chapter) higher values for the two figure of merit are reached by samples with higher carrier concentrations.

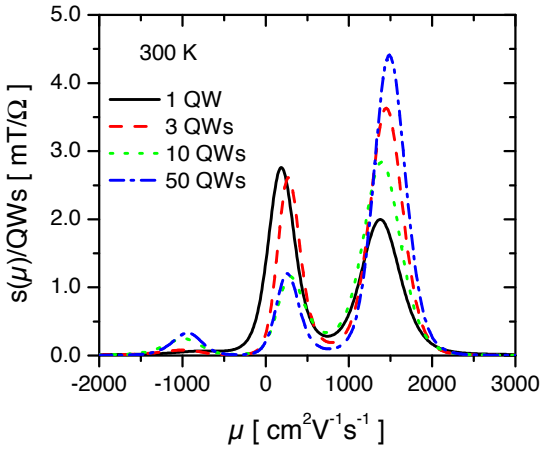

Figure 5.12: Mobility spectra at 300 K for four different samples featuring 1, 3, 10 and 50 QW [10]. The four samples studied featured the same design and the one presented for superlattice Design 2.

Work done and presented in [10] studied the mobility inside the conduction channels (quantum-wells) for Design 2 by a set of four different samples featuring 1, 3, 10 and 50 QW. The mobility spectra at 300 K for these four samples, shown in Figure 5.12, demonstrated two peaks at different mobilities, indicating the presence of two channels that contribute to the conduction of carriers. The peak at 1400 cm^2/Vs corresponds to the conduction inside the QW while the second peak corresponds to the conduction inside the doped barriers. The presence of a parallel conduction is expected to limit the mobility and therefore the electrical conductivity on the present designs. This indicates that the current doping density is too high and that a reduction of this, should reduce the conduction along the low-mobility doped SiGe layers, which could also reduce the thermal conductivity value.

The electrical conductivity of these samples was also measured at 300 K, giving σ values of 9436, 9693, 10047 and 11089 S/m respectively. These numbers also suggested that an increased number of QW meant an increase of the electrical conductivity.

5.3.2 Seebeck Coefficient

The Seebeck coefficient is defined as the voltage dropped (in open circuit) between two points which are at a different temperature, $\alpha = \Delta V/\Delta T$.

In order to have a temperature difference between the voltage probes, a constant dc voltage was applied to one of the heaters to create a uniform and stable heat flux along the bar. The change of the Ti/Pt resistance of each thermometer was monitored by two lock-in amplifiers. In order to accurately calculate the change in resistance, each thermometer was connected in series with a low temperature dependant resistor. The voltage dropped at this resistor was also monitored by a lock-in amplifier and its value was used to calculate the current passing through the thermometers. Knowing the current and the voltage, the resistance of the thermometers was extracted for different powers applied to the heaters. A temperature calibration was used to translate the change of resistance into a change of temperature. More details about the calibration technique are reported in Section 4.2.1.

Figure 5.13 shows two plots of the resistance and temperature measured by the two thermometers as a function of heater power. In the first case *a*), the substrate had not been removed and so no temperature difference was detected. In the second case *b*), the same measurement was performed on a suspended device and a power of only 20 mW applied to the heater was enough to create a ΔT of 20 K. This set of measurements demonstrated the importance of the substrate removal to confine the heat.

Once the substrate had been removed to confine the heat inside the SL structure, only a few mW applied to the heater were required to detect a Seebeck voltage along the Hall bar. Figure 5.14 *a*) shows a schematic of the measurement while *b*) shows the Seebeck voltage measured as a function of ΔT. The plot shows two different measurements of the Seebeck voltage on the same device but, applying power first to the left heater and then to the right heater while keeping the voltage probes static. The heat flux inside the structure was reverse purely to check consistency.

A least square fit was used in both sets of data to determine the gradient of the fit and therefore to calculate the Seebeck voltage as a function of ΔT. The values obtained in both cases were 276.4 μV/K and 282.4 μV/K agreeing to with 3% of each other.

As can be seen in Figure 5.14 *a*), both thermometers were spaced no more than 15 μm (in the X direction) from its respective voltage contact. A ThAFM probe was used to

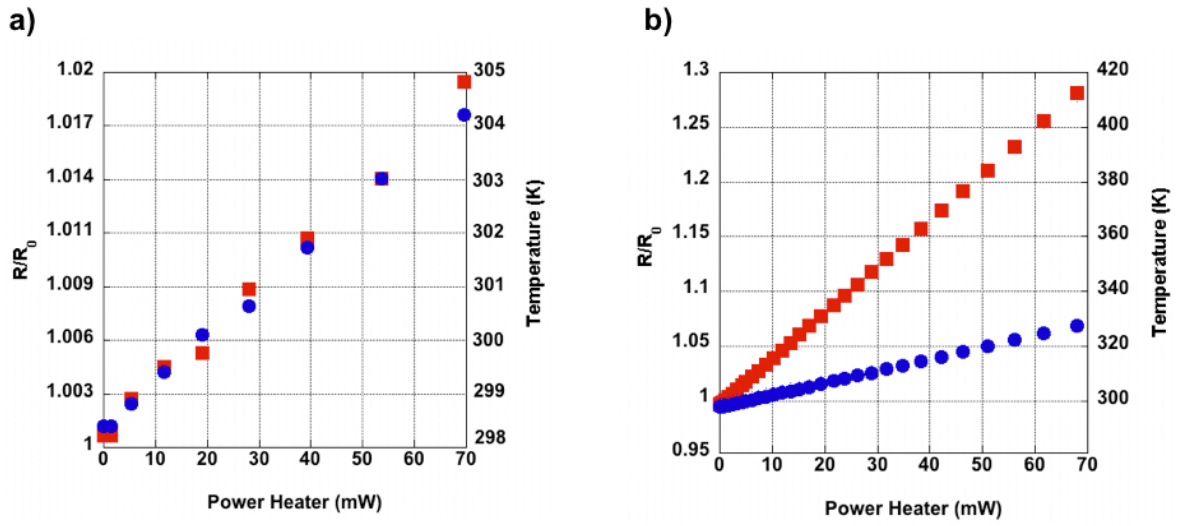

Figure 5.13: Figure *a*) shows the temperature difference between the two thermometers as a function of heater power. In this case the substrate remained in place and so no difference in temperature was measured. Figure *b*) shows the same measurement, but in this case the substrate had been etched away creating a suspended device. Having a suspended membrane confines the heat inside the SL structure creating a high ΔT with a few mW applied to the heater.

measure local temperatures along the bar (see Section 4.2.2) and check in this case, if contacts and thermometers were close enough to guarantee the same temperature. It was found that the average temperature collected by the ThAFM probe in an area of 15 μm along the bar and 85 μm across the bar had always an error smaller than 0.5 K. The error quoted for the thermometers was bigger than the one produced by the ThAFM probe, but still smaller than 1 K. These errors were taken into account by linear least squares fits to calculate the Seebeck coefficient, with the deviation of the fit always smaller than 5%.

The two techniques used to measure ΔT were measuring the temperature on top of the Hall bar and therefore on top of the superlattice. This ΔT was used to calculate the Seebeck coefficient and so it has to be pointed out that a uniform heat across the superlattice was considered.

A finite element analysis of one of the devices fabricated, was studied to investigate the

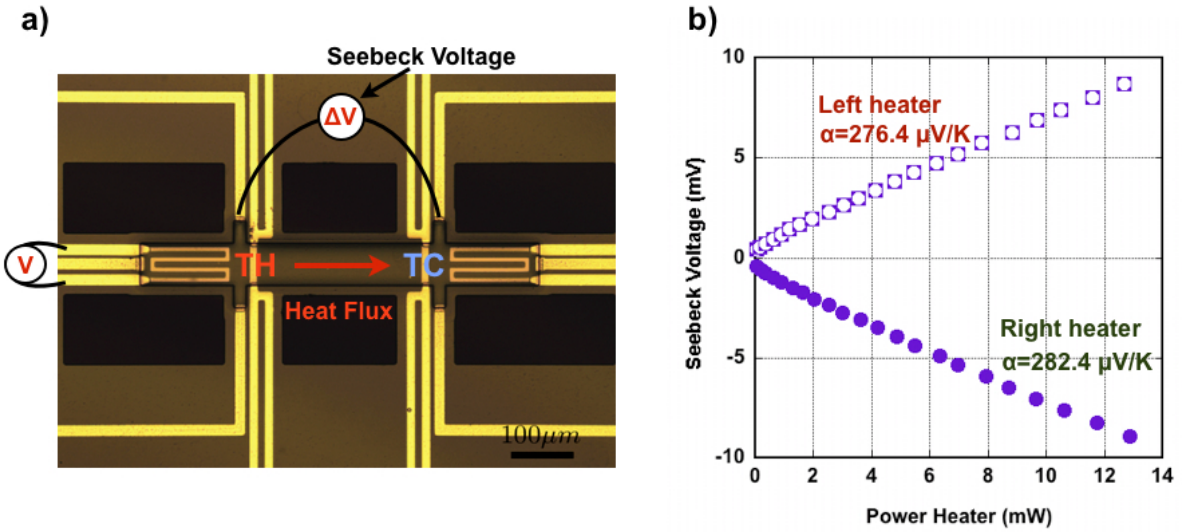

Figure 5.14: Figure *a*), schematic for the measurement used to extract the Seebeck coefficient. Figure *b*), two different measurements taken on the same device while one of the two heaters was powered at a time.

temperature along the bar at three different heights across the suspended membrane. The heights considered were: at the top of the SL, at the bottom of the SL and at the bottom of the membrane (including the buffer layer and the SOI). The temperature simulated was solved by Fourier's equation, where the inputs for the solution were: the exact 3D geometry of the device, the power applied to the heater and the thermal conductivity of the complete stack constituting the membrane.

At this stage, the thermal conductivity of the SL was unknown and so an initial value of $40\,\mathrm{W/m \cdot K}$ was selected to solve the simulation. A second value (4 times smaller) of $10\,\mathrm{W/m \cdot K}$ was also selected to compare the solution between a high and low value of κ. Figure 5.15 shows the solution for both simulations, where the temperature along the bar between the two heaters has been plotted for three different heights.

Both solutions suggested that the temperature across the membrane was the same for two different values of κ, which confirmed that a uniform heat flux could be considered and validated the previous Seebeck measurement.

On the other hand, both plots showed visible sections where the gradient of the temperature profile was different from each other. The points where the slope changes gradient

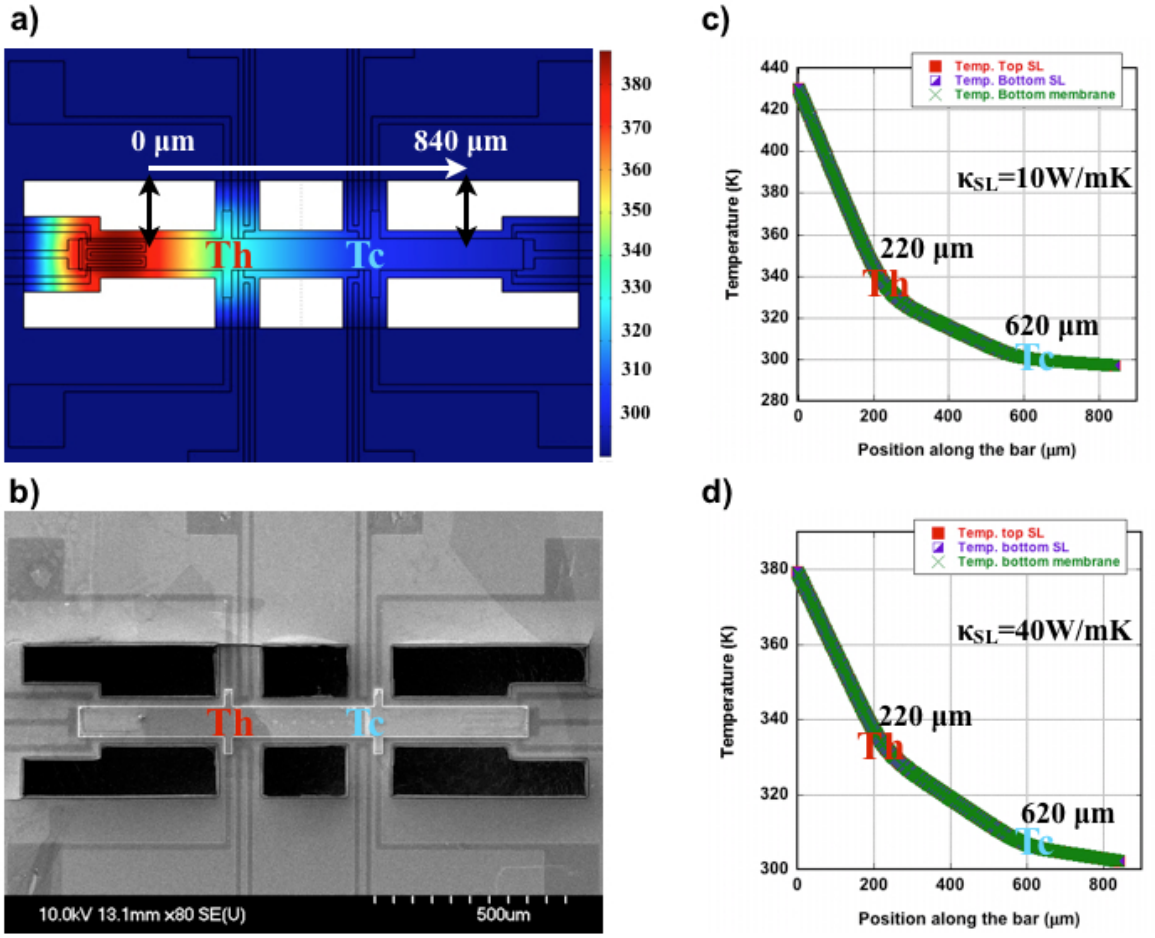

Figure 5.15: Figure *a*), shows an image of the device simulated, considering all the layers conforming the device (courtesy of Yuan Zhang). Figure *b*), shows an SEM image of the device simulated. Plots *c*) and *d*) shows the temperature profile as a function of position for three different heights inside the membrane and considering two different κ values for the SL (courtesy of Yuan Zhang).

corresponded with the two beams of the device used for voltage contacts and thermometers. This change of the slope suggested that there were important parasitic channels for the heat to flow out of the device.

Figure 5.16 shows the measured Seebeck coefficient as a function of QW widths for samples from Designs 1 and 2 and for the reference sample. The behaviour of α for the superlattices is very similar to the one produced for bulk p-$Si_{0.2}Ge_{0.8}$ (reference sample)

and for bulk p-Ge ($\alpha = 280\,\mu$V/K for a comparable doping level [34]). These results indicate that the QWs could be too thick to strongly influence α and that, as the mobility spectrum measurements showed in [10], the present superlattices do not achieve a 2D conduction yet, due to the high influence of carriers inside the bulk SiGe barriers.

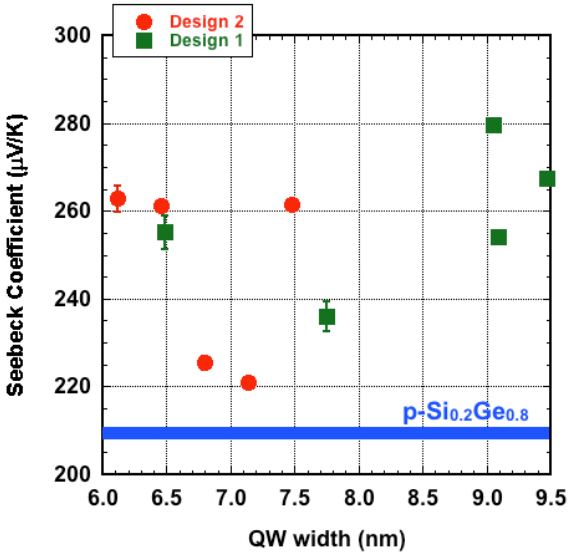

Figure 5.16: The Seebeck coefficient measured for Designs 1 and 2 and for the reference sample as a function of QW width.

Due to the non-enhancement of the Seebeck coefficient, the improvement of the ZT or the power factor could only be achieved by the results of the thermal and the electrical conductivity. Figure 5.17 demonstrates the power factor as a function of QW width for Designs 1 and 2, also compared with the reference sample. The power factor follows the same trend as the electrical conductivity, and so there is not a substantial change with the variation of QW thickness. The highest power factors presented, are obtained for the samples which had the highest electrical conductivities, giving a maximum of $6.02\,\mathrm{mW/m \cdot K^2}$ for Design 1. This result is two times higher than reported values for bulk p-Si [110] and p-Ge [100], 6 times higher than $\alpha^2\sigma$ values reported in [100, 111] for p-$Si_{0.3}Ge_{0.7}$ material at comparable carrier densities and much higher than n-Si/Ge superlattices [39].

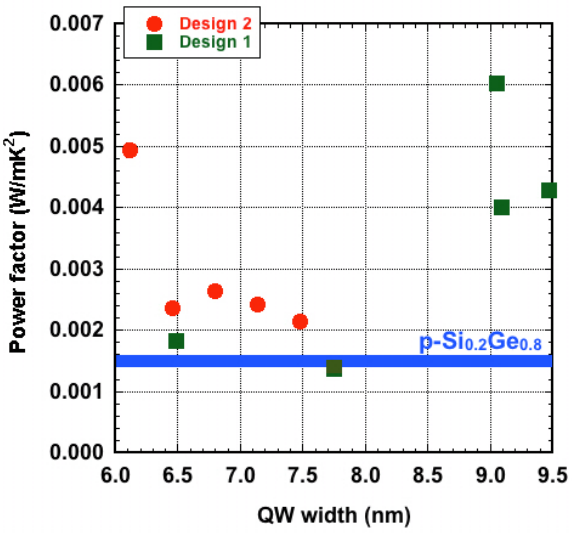

Figure 5.17: The power factor as a function of QW width for Design 1 and 2, values compared with the reference sample.

5.4 Thermal Characterisation: ZT Calculation

5.4.1 Thermal Conductivity

The solution from both simulations, where a κ value of $10\,\mathrm{W/m \cdot K}$ and $40\,\mathrm{W/m \cdot K}$ was considered (see Figure 5.15) showed a 1-dimensional heat transfer along the bar. Having a uniform heat flux inside the structure made it possible to analyse the data by using the 1-dimensional Fourier's law:

$$Q = \kappa \frac{\Delta T A}{L}, \tag{5.1}$$

where Q is the heat flowing inside the structure, A is the cross sectional surface area and L is the distance between the two temperature measurement points.

Even if the influence of the Si substrate had been removed by creating a suspended membrane, there were still some parasitic channels in the device for the heat to flow through. The presence of these parasitic channels, such as beams to support the device and metal lines to connect heaters and thermometers to bond-pads, made not possible to consider that the heat going inside the structure was the same as to the total power applied to the heater.

To accurately extract the value of the thermal conductivity, a precise estimation of the heat flux was required. This estimation was done by a differential method where ΔT was measured before and after the central part of the membrane was removed. Figure 5.18 shows two SEM images of the membranes used for the measurement, *a*) shows a complete device while *b*) shows the same device where the central part had been etched away to calculate how much heat was lost through parasitic channels.

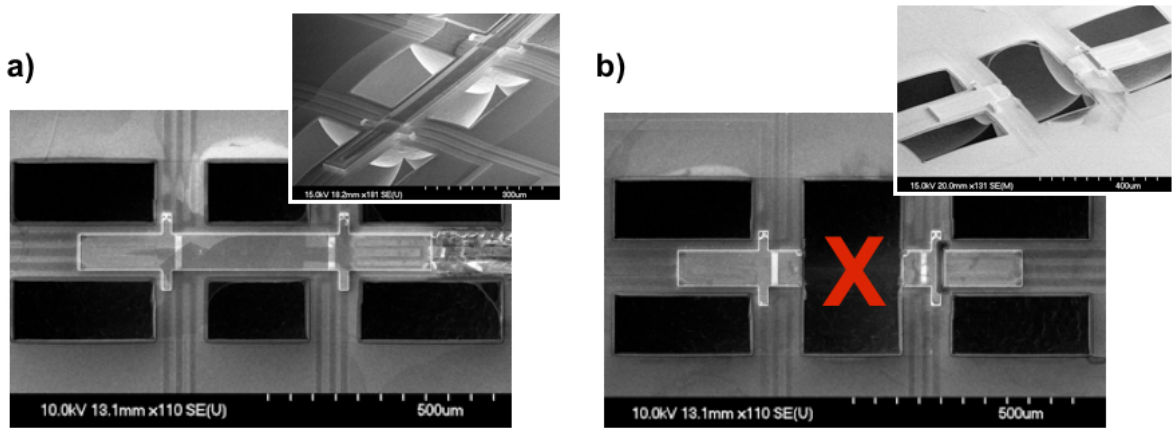

Figure 5.18: SEM pictures of a full *a*), and a broken membrane *b*). The temperature gradient is measured before and after the central part of the hall bar is removed, this is used to subtract the heat flux that flows inside the structure.

In absence of the membrane the local temperature of the hot thermometer increased when compared to the structure with the full membrane, while the cold thermometer in the broken membrane remained almost at room temperature. For a defined temperature, the power difference between the hot thermometer with a full membrane structure and a broken membrane gave information about the amount of heat that was transported through the membrane. ΔT was calculated by the full membrane thermometers for the defined power used to extract the heat flux. The temperature of the cold thermometer of the broken membrane did not vary with heater power, confirming its thermal insulation from the heat source.

The heat flux flowing through the Hall bar (Q_{HB}) was extracted by:

$$Q_{HB} = Q_H - Q_{PC}, \tag{5.2}$$

where Q_{PC} was the heat lost through the different parasitic channels in the structure and Q_H was the power applied to the heater. Figure 5.19 demonstrates the temperature profile for both thermometers for a full and a broken membrane. In this case, an effective power of 1.9 mW with a ΔT of 13.8 K was extracted for one of the samples from Design 2, giving a value of $47.7 \pm 8.9\,\mathrm{W/m \cdot K}$.

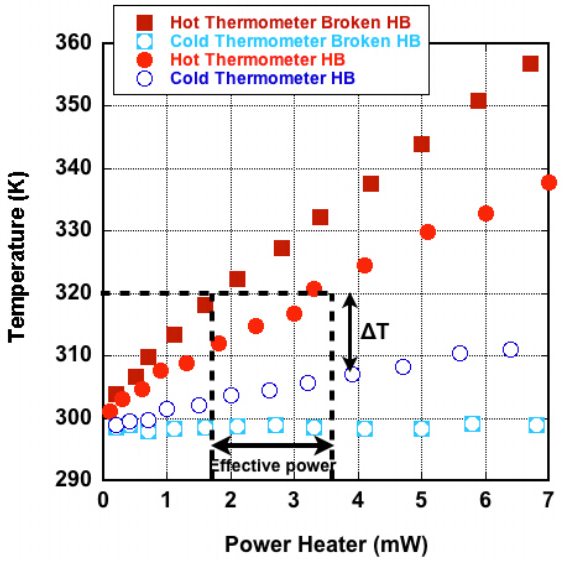

Figure 5.19: The temperature dependance versus heater power for a full and broken membrane. The difference of power required for a defined temperature between hot thermometers gives an indication on the power lost through parasitic channels.

The value of the thermal conductivity obtained was a sum of the thermal conductivity of the individual layers: the SiGe buffer layer (1 μm thick), the SiO_2 layer (1 μm thick), the Si thin layer (340 nm thick) and the SiN layer (75 nm thick) used to passivate the structure from heaters and thermometers. To extract the thermal conductivity of only the SL structure it was necessary to subtract the thermal conductance contribution from these channels. Using Fouriers Law and considering the conductance and geometrical dimensions of every single layer it was possible to obtain:

$$\kappa_{SL} = \frac{\frac{Q_{HB}L}{\Delta T w} - \kappa_{SiGe}t_{SiGe} - \kappa_{Si_3N_4}t_{Si_3N_4} - \kappa_{Si}t_{Si} - \kappa_{SiO_2}t_{SiO_2}}{t_{SL}} \tag{5.3}$$

where κ_i and t_i represent the thermal conductivity and the thickness respectively, of each layer under consideration, L and w are the length and the width of the Hall bar structure respectively, and ΔT is the temperature difference measured with the resistive thermometers.

The thermal conductivities considered for the subtraction were taken from the literature, considering a $\kappa_{SiGe} = 40 \pm 7.9\,\mathrm{W/m \cdot K}$ from [9], a $\kappa_{Si} = 150 \pm 4.5\,\mathrm{W/m \cdot K}$ from [32], a $\kappa_{SiO_2} = 1.6 \pm 0.2\,\mathrm{W/m \cdot K}$ from [46] and a $\kappa_{SiN} = 30 \pm 2.5\,\mathrm{W/m \cdot K}$ from [46]. The thickness for the SiGe buffer layer was considered 1 μm thick with a tolerance of 30% due to the growth uniformity, and the thickness of the SiN layer was 75 nm with a tolerance of 5%. The thicknesses for the Si and the SiO_2 layers were 340 nm and 1 μm respectively, both with tolerances lower than 3% [91].

A final value of $44.1 \pm 9.2\,\mathrm{W/m \cdot K}$ was obtained for a modulation doped quantum well structure with a QW width of 6.1 nm and a doping concentration of $10^{19}\,\mathrm{cm^{-3}}$.

In order to cross check this last value, a ThAFM probe was used to measured the temperature along the bar between the two thermometers. Seven scans were done in order to cover the 340 μm distance between the thermometers, see Section 4.2.2. A finite element analysis, on the same device that had been measured, was used to fit the solution of the simulation to the experimental data. A value of $42.0\,\mathrm{W/m \cdot K}$ for the SL gave the best fit to the data, which was in good agreement with the value extracted by the differential method. Figure 5.20 demonstrates the temperature measured by a ThAFM probe versus the distance between the two thermometers, the plot also shows the temperature profile simulated for the exact same device (exact geometry), with the same power applied to the heater and with an input of $\kappa_{SL} = 42\,\mathrm{W/m \cdot K}$.

Figure 5.21, demonstrates the thermal conductivity as a function of QW widths for the superlattice designs and the reference sample.

All the values are lower than bulk p-Ge ($60\,\mathrm{W/m \cdot K}$ [34]) and most of them are lower than the values measured for the reference sample, which is due to modulation doping and to the presence of interfaces. On the other hand, the value measured for the reference sample (p-$Si_{0.2}Ge_{0.8}$) is about a factor of 4.5 higher than the literature values presented by Dismukes of $7.4\,\mathrm{W/m \cdot K}$ [14].

The values measured for Design 1 show an increase in the thermal conductivity for thicker QWs, however, Design 2 presents the complete opposite behaviour. When plotting the thermal conductivity as a function of electrical conductivity, Figure 5.22, it is quite

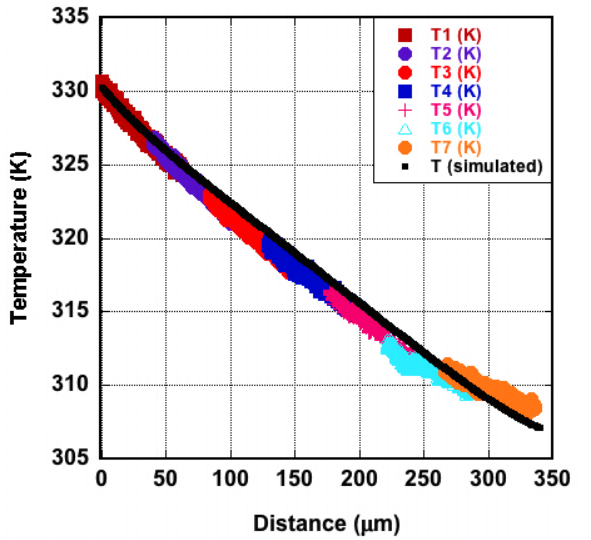

Figure 5.20: The temperature profile measured by a ThAFM probe between the two thermometers as a function of position. A finite element analysis of the exact same device, was solved using a $\kappa_{SL} = 42\,\mathrm{W/m \cdot K}$ giving the best fit to the experimental data.

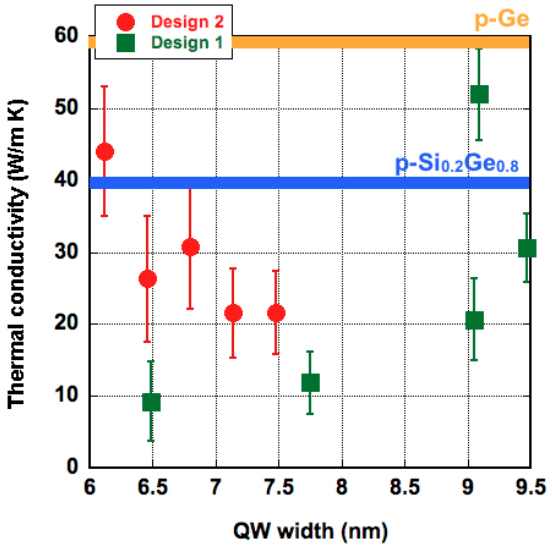

Figure 5.21: The thermal conductivity as a function of QW width. The values must be compared with bulk p-SiGe and bulk p-Ge with similar doping densities (also shown in the plot).

visible that σ has a strong influence on κ, suggesting that the heat conduction is dominated by the carrier transport and not by lattice thermal contribution. The present superlattices have still a strong coupling between σ and κ, suggesting that the present SLs have a bulk behaviour as it is stated by the Wiedemann-Franz law. This bulk behaviour of the superlattice was already predicted after discovering a parallel conduction of carriers inside the barriers, as well as the constant results obtained for the Seebeck coefficient, comparable with bulk p-SiGe (reference sample).

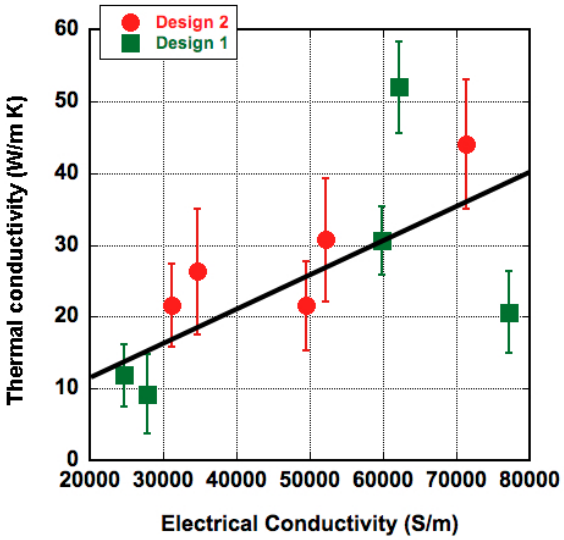

Figure 5.22: The thermal conductivity plotted as a function of the electrical conductivity for each sample, just including Design 1 and Design 2.

A linear fit to the data (also shown in Figure 5.22) of the form;

$$\kappa_{SL} = \kappa_L + CT\sigma, \tag{5.4}$$

where κ_L is the lattice contribution to the thermal conductivity, and C is a constant which in the Wiedemann-Franz law corresponds to the Lorentz number, gives a C value 65 times greater than the Lorentz number. This result suggests that the current superlattices present additional contributions that increases the total thermal conductivity from the theoretical value expected.

An optimisation of the present SLs is required in order to eliminate the carrier transport along the barriers, which at the moment is limiting the quantum effects of the 2D

structure. If the carriers were just travelling inside the conduction channels (QWs), the total carrier thermal conduction would be greatly reduced and the lattice contribution of the thermal conduction could be dominated by the SiGe matrix.

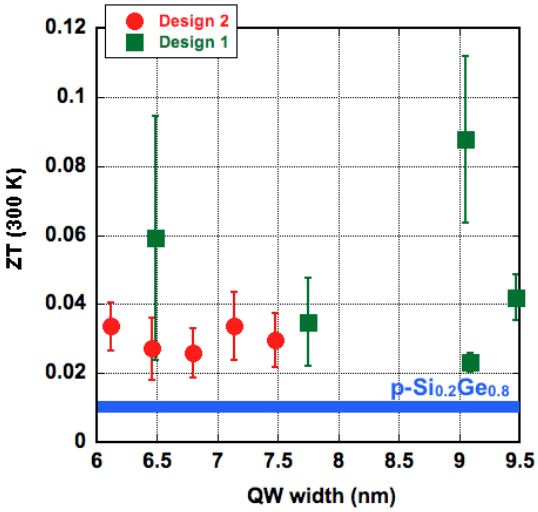

Figure 5.23: The figure of merit (ZT) plotted as a function of QW width for both designs compared to the reference sample.

These high values of κ result in low values of ZT, as shown in Figure 5.23. From these results it is clear that for the range of QW thicknesses studied, there is not a clear trend for the ZT value. The ZT values tended to remain constant, reaching its maximum for the sample that had the highest σ and the lowest κ.

5.5 The Effect of Temperature

Silicon and germanium materials present better thermoelectric generation when working at high temperatures as the parameter Z improves when T increases, as shown in Figure 1.4.

A sample from Design 1 was tested at temperatures above room temperature to study its thermoelectric properties. Devices with broken and full membranes, so that the thermal conductivity could also be evaluated, were wire bonded onto chip carriers and placed inside an environmental chamber. σ, α and κ, as well as the two figure of merit, were

measured as a function of temperature going from 298 K to 370 K, which is the maximum chamber temperature.

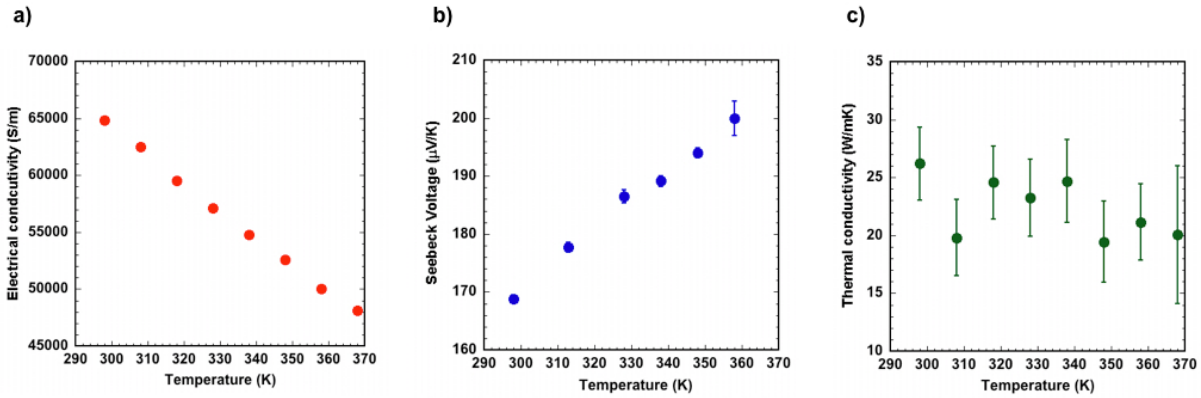

Figure 5.24: The electrical conductivity *a*), Seebeck coefficient *b*) and thermal conductivity *c*) as a function of temperature.

Figure 5.24 *a*) shows the electrical conductivity as a function of temperature. As the plot shows σ is reduced by a factor of 0.7 in a range of 70 degrees. Thin films of p-type SiGe alloys showed σ values that decrease by a factor of 0.85 for the same range of temperature [14]. This suggests that apart from increased phonon scattering, carriers could be thermally excited out of the higher mobility Ge QW into the lower mobility SiGe barriers reducing the value of the electrical conductivity in the present superlattices. This is a clear disadvantage of these lateral designs with δ-doping, where the idea is to confine carriers into high mobility channels to increase the mobility and therefore to increase σ.

Figure 5.24 shows the Seebeck coefficient, *b*) and the electrical conductivity, *c*) as a function of temperature. Both parameters showed the expected improvements, as the Seebeck coefficient is proportional to the absolute temperature, while the lattice contribution of κ is inversely proportional to it.

Figure 5.25 shows the two figures of merit plotted as a function of temperature. The power factor follows the same trend as the Seebeck coefficient, remaining almost constant for the whole range of temperatures, as the increase of α is compensated by the abrupt decrease of σ. On the other hand, ZT shows an increase by a factor of 1.5 over the range of temperatures. It has to be pointed out that even if Z remained constant the value of ZT would improve, however in this case an improvement by a factor of 1.3 in Z is achieved over such a range of temperatures. Thin film p-SiGe alloys with the same doping

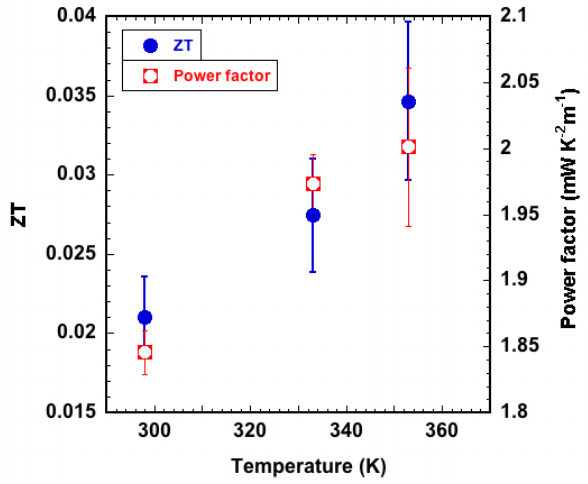

Figure 5.25: The two figures of merit plotted as a function of temperature.

densities, showed figures of merit that increased by a factor of 1.2 over the same range of temperatures [14]. The absolute values for ZT and PF were higher than the values reported in this work mainly due to the low thermal conductivities, which were 3.5 times lower than the κ values measured in the superlattices. As mention in the previous section the two designs studied showed a total κ dominated by the electronic contribution of the thermal conductivity due to the Wiedemann-Franz law which relates κ_e with σ limiting the improvement of the overall κ.

Due to the limitation of the set up, a maximum temperature of 370 K was reached, meaning just an increase of 70 K above room temperature. The maximum temperature of the structures used within this work is limited to a temperature of 673 K, this being the temperature used to optimise the ohmic contacts to the material. Further studies should be done up to 673 K to obtain the maximum ZT that could be achieved for these structures.

5.6 Conclusions

Two p-type modulation doped Ge/$Si_{1-x}Ge_x$ superlattices with different Ge contents have been studied as a function of QW width. The two superlattices were designed to enhance

the in-plane thermoelectric properties of the material.

A suspended Hall bar structure with integrated heaters and thermometers was used to extract the values of σ, α and κ in one single device yielding accurate values of ZT and PF. All the values reported have been compared with an alloy reference sample and have demonstrated improved electrical and thermal conductivities and Seebeck coefficients.

However, the improvements have been very modest indicating that the current superlattices need further optimizations. The highest ZT and PF reported were of 0.08 and $6\,\mathrm{mW/K^2m}$ respectively, corresponding to a superlattice with a QW width of 9 nm and a Ge content inside the barrier of 70% (Design 1). The electrical conductivity increased by a factor of 2.4 above its alloy reference value, the Seebeck coefficient increased by a factor of 1.3 and the thermal conductivity just decreased by a factor of 0.6.

High σ values have been encountered due to δ-doping, but these values are still limited, possibly due to the conduction of carriers inside the barriers. This study indicates that future designs with lower doping densities could help to confine the carriers inside the QW creating just one conduction channel and therefore improving the mobility of the present superlattices. The combination of unoptimised doping, along with QWs which are too thick, has placed a limitation on α; the values of which are still quite similar to 3D systems.

In addition, theoretical analysis suggested that reducing the TDD by two orders of magnitude should significantly increase the present values of ZT, as was studied in [11]. Indeed, Figure 5.26 shows the agreement between the experimental results obtained for Design 1 and the ZT theoretically calculated by [11] for a TDD of $10^9\,\mathrm{cm^{-2}}$.

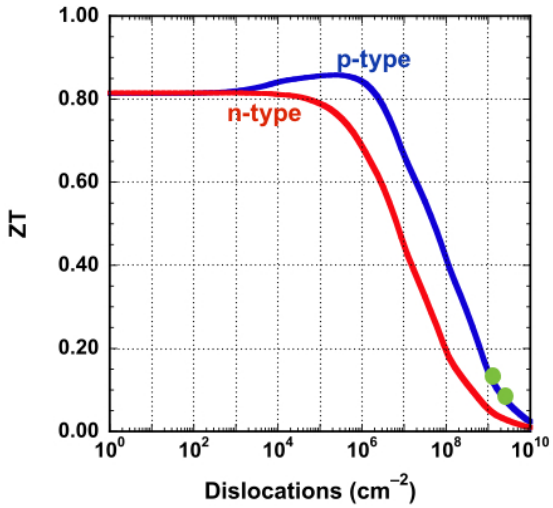

Figure 5.26: The predicted figure of merit (ZT) as a function of TDD for Design 1 [11]. The two green dots are the experimental data obtained from Design 1 samples.

Chapter 6

Thermoelectric Characterisation in the cross-plane direction for p-Ge/$Si_{0.5}Ge_{0.5}$ Superlattices

This chapter is focused on the cross-plane thermoelectric properties of Ge/$Si_{0.5}Ge_{0.5}$ superlattices, where the heat and carrier transport occurs perpendicular to the SL.

A range of p-type Ge/$Si_{0.5}Ge_{0.5}$ superlattices with the same design but different doping levels are investigated in detail to determine the role of the doping density in dictating the thermoelectric properties. This set of samples is also compared with two other structures, where one of them consists of the same design but with δ-doping and the second one with constant doping but with reduced QW and barrier thicknesses [112].

The chapter begins by explaining the different designs studied and is followed by the physical characterisation of the superlattices. It then continues with the fabrication process used to build the devices in order to thermally and electrically characterize the material. The techniques used to measure σ, α and κ are also introduced, presenting the results obtained for each design and comparing them with the literature values.

6.1 Material Design and Growth

For vertical thermoelectric structures the heat and carrier conduction occurs perpendicular to the heterostructure. It is possible to engineer the material in order to scatter or filter the phonons without significantly influencing the carrier transport. Cross-plane

designs should have higher α from the higher asymmetry in the density of states in the thinner QWs [35, 113] and also lower κ due to an increased heterolayer phonon scattering, compared to the in-plane designs [70, 72]. A range of p-type $Ge/Si_{0.5}Ge_{0.5}$ superlattices were designed and grown to investigate the cross-plane thermoelectric properties as a function of doping density.

Following the same idea as for the lateral structures, Ge QWs were selected for obtaining p-type σ and α values higher than p-type Si (see table 1.1) and $Si_{0.5}Ge_{0.5}$ barriers were chosen to reduce the lattice thermal conductivity of the material as presented in [14]. Furthermore, the high mismatch between QWs and barriers would increase the acoustic mismatch, increasing the phonon scattering and reducing the thermal conductivity.

The heat had to flow perpendicular to the superlattice, and so mesa structures that could confine this heat vertically (going from the top to the bottom of the SL) were used as devices. This kind of structure did not need to be suspended for thermal characterisation and the buffer layer and substrate were used as heat sinks. This gave a clear advantage over the lateral devices as the substrate and buffer layer thicknesses were not an issue for the fabrication and thermal characterisation. Thick graded buffer layers were used during the growth of the superlattices to ensure low TDD.

The total thickness of the multi-quantum well structure was also important, as thick active structures are able to provide high temperature differences. The chosen thickness for the active layer was $4\,\mu$m, which was a compromise between the time required to grow the structure and the thickness required to produce working devices.

The samples were grown on 100 mm diameter p-Si (001) substrates of $5 - 10\,\Omega$cm using low-energy plasma enhanced chemical vapor deposition (LEPECVD). A $\sim 13\,\mu$m graded buffer layer from Si to $Si_{0.175}Ge_{0.825}$ was grown at a rate of between 5 and 10 nm/s [27, 107, 114]. On top of this, a 500 nm contact of p-$Si_{0.175}Ge_{0.825}$ (N_A=2.0x$10^{18}\,cm^{-3}$) layer was grown.

The superlattices were grown at rates of 1.0 to 1.5 nm/s for designs SL1 and SL2 and 0.25 nm/s for SL3, SL4 and SL5. These growth rates were chosen to allow control of the layer content, the thicknesses and the doping levels, while ensuring that the whole thermoelectric stack could be fabricated in a reasonable time. Designs SL1 to SL4 consisted of 922 repeats of QWs of 2.85 ± 1.5 nm p-Ge and 1.1 ± 0.6 nm of p-$Si_{0.5}Ge_{0.5}$ with the doping density increasing from $1.9\,x\,10^{17}\,cm^{-3}$ to $2.0\,x\,10^{18}\,cm^{-3}$.

Design SL5 consisted of 2338 repeats of QWs of 1.1 nm p-Ge and 0.6 nm of p-$Si_{0.5}Ge_{0.5}$. Both QWs and barriers thicknesses were reduced by a factor of 0.4 in order to increase the phonon scattering and to assist the tunneling of carriers through the barriers.

For design SL4, only the barriers were doped at 6.0×10^{18} cm^{-3} to produce an average doping of 1.2×10^{18} cm^{-3}. Doping only the barriers should reduce the impurity scattering in the Ge QWs aiming for higher σ.

Finally a cap of 60 nm of p-Ge (N_A=2.0x10^{18} cm^{-3}) was grown for a top ohmic contact. Figure 6.1 *a*) shows the design followed for SL1, SL2, SL3 and SL4 while *b*) shows the design followed for SL5.

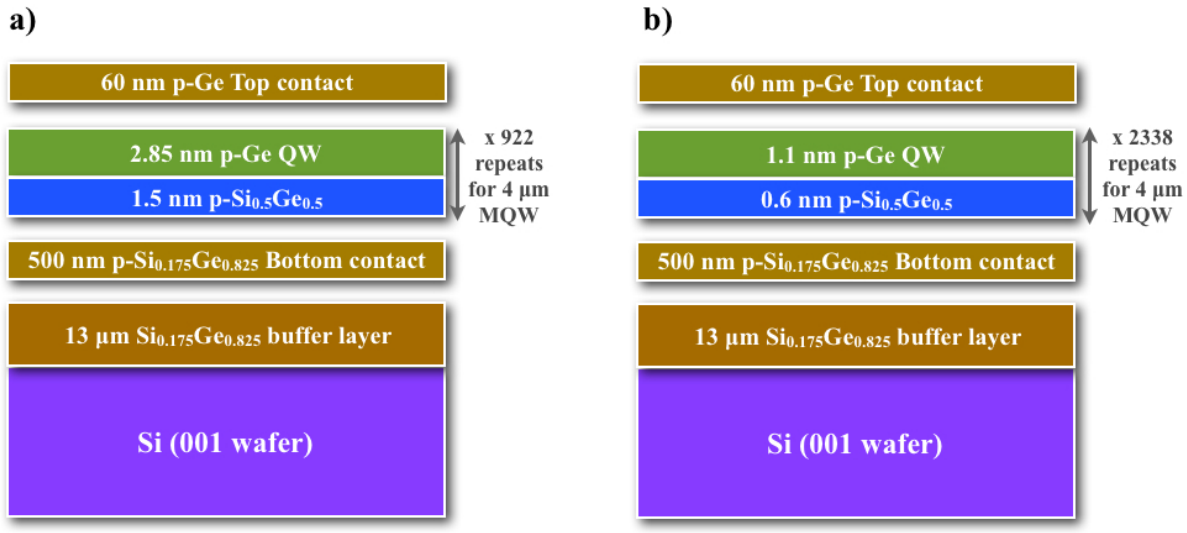

Figure 6.1: *a*) The schematic diagram of the design followed for SL1, SL2, SL3 and SL4. *b*) The design followed for SL5 where the QWs and barriers thicknesses were reduced by a factor of 0.4.

6.1.1 Physical Characterisation

As introduced in Section 3.2.2.1, the LEPECVD tool presents a non-uniform growth rate over a 100 mm wafer. For this reason, while the wafers investigated (SL1, SL2, SL3 and SL4) presented the same nominal period thickness, depending on the 1x1 cm^2 piece selected from the 4-inch wafer, this thickness could change by $\pm$ 20%. HRXRD was used to

investigate the period thickness and material quality, and ω-2θ scans around the symmetric (004) reciprocal lattice point were taken and fitted by scattering theory simulations to extract individual layer thicknesses as well as Ge compositions [115, 116]. The procedure for the physical analysis has already been described for the lateral designs, refer to Section 5.1.1 [2].

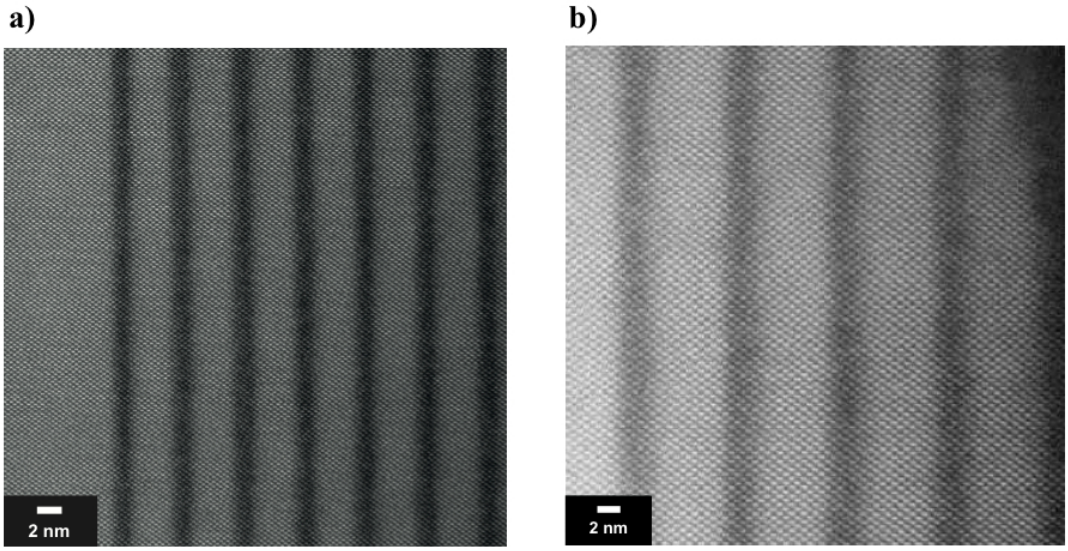

Figure 6.2: *a*) A TEM image of SL3 with QWs of 3.31 ± 0.12 nm (XRD 3.43 nm) p-Ge and 1.51 ± 0.14 nm (XRD 1.17 nm) of p-$Si_{0.5}Ge_{0.5}$. *b*) A TEM image of SL4 width an average Ge QW width of 2.48 nm and barriers of 1.12 nm.

HRXRD indicated that all the superlattices were strain symmetrized to the $Si_{0.175}Ge_{0.825}$ virtual substrates [116]. By this analysis it was also found a splitting of the SL peaks with a different Ge composition, changing from 86% to 85.6% as measured for SL3 [116]. It was suggested that during the growth a composition change could have occurred giving this splitting in the SL as a result. A variation of 0.3% in the Ge content for the barriers over the complete 4 μm stack should not affect the thermoelectric properties under study.

Individual thicknesses of the heterolayer were also determined by transmission electron microscopy (TEM) [9, 107]. Figure 6.2 shows a TEM image of *a*) SL3 with a Ge QW width of 3.31 nm and barriers of 1.17 nm, and *b*) SL4 with an average Ge QW width of 2.48 nm and barriers of 1.12 nm.

6.2 Device Fabrication

For the thermal and electrical characterisation of the vertical designs, devices inside the micro-meter scale were fabricated in order to extract σ, κ and α. In this case, the carrier and heat transport occurred perpendicular to the SL and so mesa structures had to be used to confine a uniform heat travelling across the multi-QW structure.

The first idea consisted of fabricating mesa structures with integrated heaters, thermometers and ohmic contacts at both the top and bottom of the mesa so that electrical and thermal measurements could be obtained. For these devices there was no need to remove the substrate, which acted as a heat sink.

Figure 6.4 shows the initial idea for creating a working device which would allow extraction of the thermoelectric properties. It has to be pointed out that the thickness of the SLs under study were around 4 μm so it was important to be able to create a device capable of maintaining a large enough ΔT between the top and the bottom of the SL.

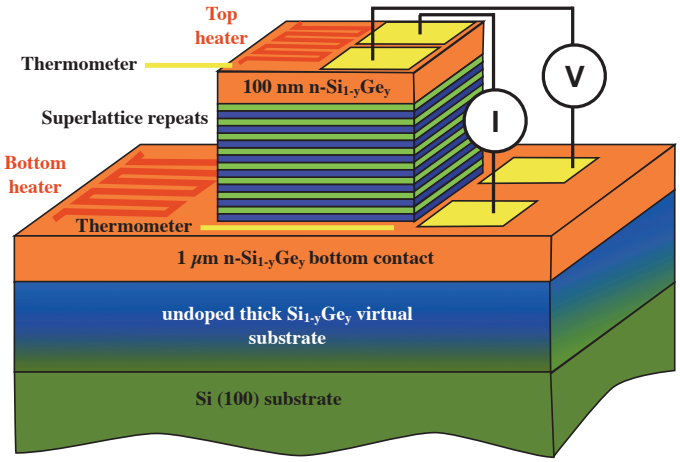

Figure 6.3: Initial schematic of a device to characterise the thermoelectric properties of a single device. The diagram shows a pillar mesa with integrated heaters and thermometers at the top and bottom of the structure plus ohmic contacts so that α and σ can be measured.

Whilst at first the fabrication might appear easier than the lateral structure, measuring and calculating the required electrical and thermal parameters was significantly more complicated than anticipated.

Ideally, due to the interactions between all the important parameters for ZT, both thermal and electrical conductivities plus Seebeck coefficients should be measured on a single test device.

B. Yang [43, 49] presented a method to measure α and κ in the cross-plane direction by using a modified 3ω technique. Their devices consisted of mesa structures with metal strips patterned at the top and bottom of the mesa used as heaters and thermometers, and metal contacts used as voltage probes. This technique was based on the well known 3ω method as discussed in Section 4.2.3. The temperature at 2ω was used to calculate ΔT between the top and bottom of the SL (the metal strip patterned at the bottom was used as the reference temperature) while the voltage probes were used to measure the Seebeck voltage. In this way the Seebeck voltage could be calculated as a function of temperature, and the thermal conductivity could be extracted by the differential 3ω method explained in Section 4.2.3. Unfortunately, the experience acquired using the 3ω method to calculate the in-plane κ for the lateral designs suggested that this modified technique was unsuitable for our SLs due to the wafer inhomogeneity.

In this work a heater was used to create a heat flux flowing down the structure and resistive thermometers were used to measure the ΔT. Using the heater as thermometer resulted in an inaccurate measurement of the temperature difference, as for small heater powers the thermometer was not sensitive to the temperature changes, underestimating the ΔT.

A full process for the fabrication of these devices had to be developed. A series of resist recipes and dry etching profiles were optimised and are explained in detail in Chapter 4, leaving for this section the enumeration of the steps followed to fabricate the complete devices:

1. Firstly a mesa structure was patterned by photolithography and etched by a mixed ICP etch recipe, as shown in Figure 6.4 *a*) (step 1). This recipe was optimised to create a small negative slope at the side walls of the mesa, so that the top and bottom contacts and the thermometers could be patterned using a self-alignement technique.

2. The structure was then passivated with 20 nm of Si_3N_4. Two windows at the top and bottom of the structure were opened inside the nitride to create the ohmic contacts which consisted of 50 nm of nickel, as shown in Figure 6.4 *a*) (step 2).

3. The structure was passivated with 50 nm of Si_3N_4 to isolate the ohmic contacts from the successive deposition of the Ti/Pd (10/70 nm) thermometers created by lift-off, as shown in Figure 6.4 *a*) (step 3).

4. A NiCr/Au (33/100 nm) heater was patterned at the top of the mesa. A window of 30x70 μm^2, aligned with the top thermometer, was patterned on top of the heater and was used as a mask to wet etch the 100 nm layer of Au, as shown in Figure 6.4 *a*) (step 4). The wet etch used to etch the Au (a mixture of deionized water, potassium iodide and iodine crystals) did not attack the NiCr layer, creating a NiCr heater with a resistance of 150 Ω.

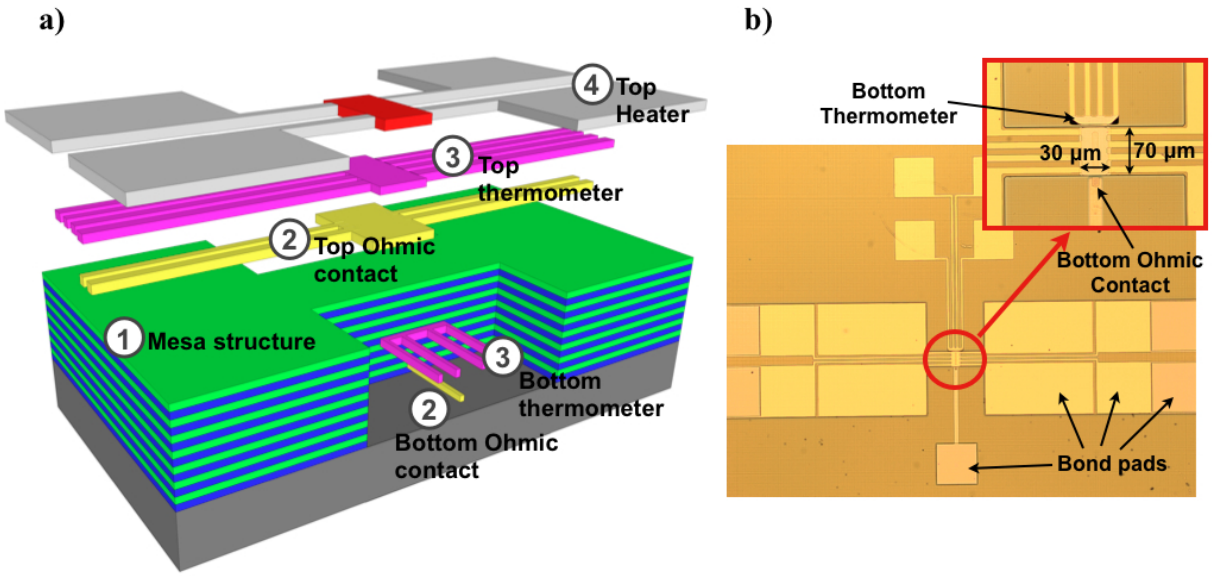

Figure 6.4: *a*) Schematic diagram of the steps followed in fabrication. The numbers indicate the order for the steps. *b*) Optical top view of a full device. The insert shows a zoom of the central part where the device itself is placed. The larger areas at the top and at the bottom of the mesa are bond-pads to probe top heater, thermometers and ohmic contacts.

An optical image of a complete device is shown in Figure 6.4 *b*), where the device itself is placed in the middle of a symmetric mesa structure and the bond-pads are placed at the edges of the mesa. Both top and bottom thermometers consisted of four-terminal devices to allow effects of access resistances to be removed from the results.

High precision measurements for α and κ have been performed for these devices and are discussed later in this chapter. However, these devices suffered from a high uncertainty in the extraction of σ, and so a second device had to be designed to better estimate the electrical conductivity.

The majority of well known test structures to measure the electrical conductivity, such as TLMs, Hall bars and van der Pauw structures, are designed to measure σ along the material but not across bulk materials or thin films.

The SLs analysed within this work were $\sim 4\,\mu$m thick. Devices with a certain geometry to confine and transport the carriers across the SL as well as optimised ohmic contacts, were required so that contact resistances would not overwhelm the measurement of the sheet resistance.

R. Venkatasubramanian [24, 39] introduced a modified TLM structure to measure the electrical conductivity in the cross plane direction for thin films. This technique consisted of fabricating a range of TLMs with different gap spacings between two terminal ohmic contacts. The devices were then modified by etching anisotropically the film between the contacts for different etch depths. The resistances were measured as a function of gap spacing (standard TLM technique) and as a function of etch depth (modified TLM technique).

This modified technique was chosen to extract the cross-plane electrical conductivity for the vertical designs presented in this work. The analysis of the technique is explained in more detail in Section 6.3.1, while this section is limited to explaining the fabrication process for such structures.

CTLMs (see Section 4.2.5) with inner diameters of $100\,\mu$m and gap spacings ranging from $1\,\mu$m to $200\,\mu$m were patterned by electron-beam lithography. Electron-beam lithography was selected to decrease the gap spacing tolerances from $0.7\,\mu$m (resolution offered by a photolithography tool) to 150 nm (e-beam resolution). This resolution was found necessary to improve the accuracy of the data.

5 nm of Ni, 50 nm of Pt and 100 nm of Ni were deposited by an electron-beam evaporator and annealed at 340°C [117]. During the anneal, the first 5 nm of Ni were used to create NiGe ohmic contacts, while the layer of Pt was used as a barrier to stop the top Ni from diffusing into the material. The top Ni was used as a metal mask to etch the SL by a mixed gas recipe inside an ICP tool. The etch rate of the mask was very slow compared to the etch rate of the SL, therefore the metal mask was used several times to perform different etch depths into the MQW.

Figure 6.5 *a*) shows a schematic diagram of a modified CTLM where the SL is anisotropically etched between the metal contacts for different depths and *b*) demonstrates a top view of range of CTLMs fabricated. The insert in *b*) shows a SEM image of a particular gap spacing after dry etching the material.

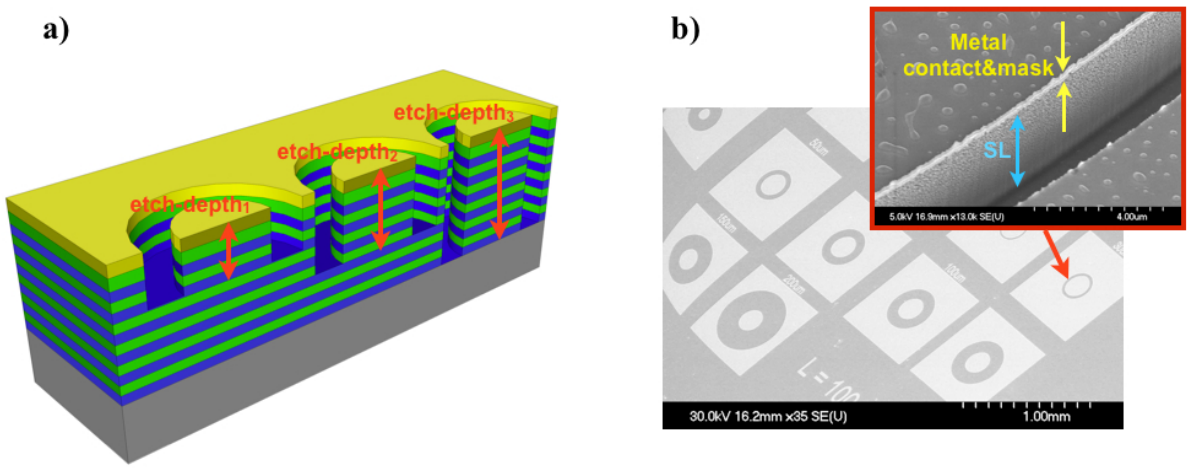

Figure 6.5: *a*) Schematic diagram of a modified CTLM where the metal is not only used as a contact but also as a mask to anisotropically etch between the metal contacts. *b*) SEM image of an array of CTLM with different gap spacings. The insert shows a zoom of a gap spacing where the SL had been etched 3.5 μm using the metal as a mask.

6.3 Electrical and Thermal Characterisation

6.3.1 Electrical Conductivity

In the literature there are several devices able to measure lateral electrical transport, however there are very few investigations on the accurate measurement of the vertical

transport. A modified TLM [24] structure was used to estimate the cross-plane electrical conductivity.

TLM and CTLM configurations are reported in Section 4.2.5, with the CTLM structure the one used in this work.

CTLMs were measured first as a function of gap spacing to extract the contact resistances due to the metal-semiconductor junction, see Figure 6.6 *a*). These devices were then modified by using the metal pads (nickel in this case) not only as the metallic connections but also as a mask to etch anisotropically the superlattice and create various device thicknesses underneath the contacts, see Figure 6.5 *a*). These devices were measured again as a function of gap spacing for eight different etch depths from 0 μm to the maximum thickness of the thin film, 3.5 μm. Figure 6.6 *b*) shows the corrected data for each etch depth collected for SL1. Each time an etch was performed, increasing the device thickness, the resistances measured were slightly larger than the previous ones with thinner devices, as expected. It has to be pointed out that this technique can only be applied when the contact resistances do not exceeds the sheet resistance of the superlattice, as no change of resistance could have been noticed between a standard and a modified CTLM structure.

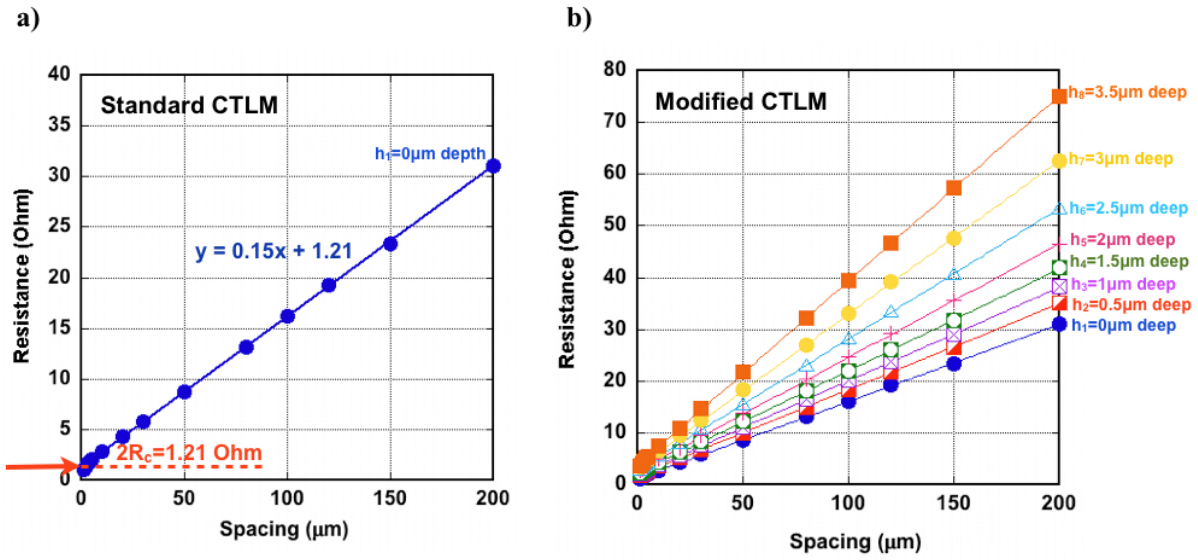

Figure 6.6: *a*) Corrected data for a standard CTLM before performing any etching, data collected for SL1. *b*) Corrected data for different etch depths of the superlattice as a function of gap spacing. Data collected from SL1.

For each etch the intercept resistance, when the gap spacing was 0 μm, was extracted and plotted as a function of etch depth. Figure 6.7 shows the intercept resistance extracted as a function of gap spacing and then plotted as a function of etch depth for SL1. Each value included the addition of $2R_c$ and 2 times the vertical contribution of R_{SL}. The gradient of these data points allowed σ perpendicular to the superlattice to be calculated.

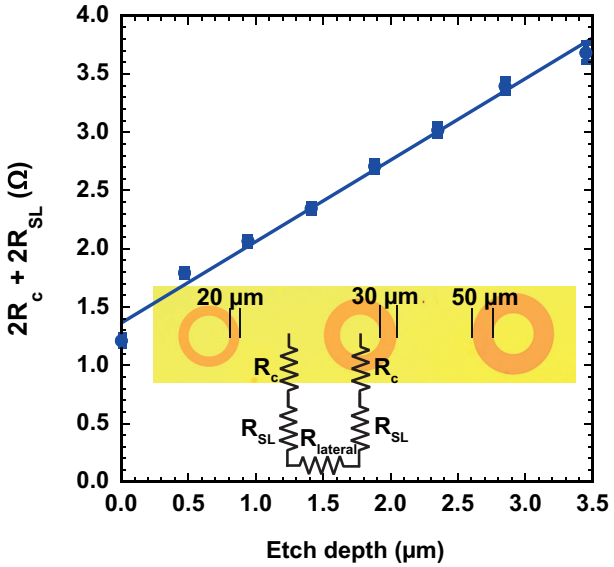

Figure 6.7: The two terminal electrical conductivity from CTLM structures as a function of the etch depth for SL1. The insert shows an optical microscope picture of the CTLM device and a schematic diagram of the measurement where R_c is the contact resistance and R_{SL} is the superlattice resistance for a given etch depth.

Figure 6.8 shows the electrical conductivities extracted for SL1, SL2 and SL3 as a function of doping level. The value of σ increased for higher doping densities and the value extracted for SL3 (highest doping density) was 5.5 times smaller than the one presented for the lateral designs p-Ge/$Si_{0.25}Ge_{0.75}$ with same doping density. This abrupt reduction of σ between the in-plane (values reported in Chapter 5) and cross-plane direction (values reported in this Section) was already reported in [39] with an anisotropy factor of 4.96.

SL4 and SL5 presented σ values of $17,600 \pm 3,330$ S/m and $15,500 \pm 1,490$ S/m, respectively. Both SL with a doping level comparable to SL3, almost doubled their electrical conductivity values. This enhancement of σ for SL4 could be expected due to the presence of δ-doping and so its reduction of impurity scattering in the Ge QW. This phenomena was already demonstrated for the lateral designs, refer to Chapter 5.

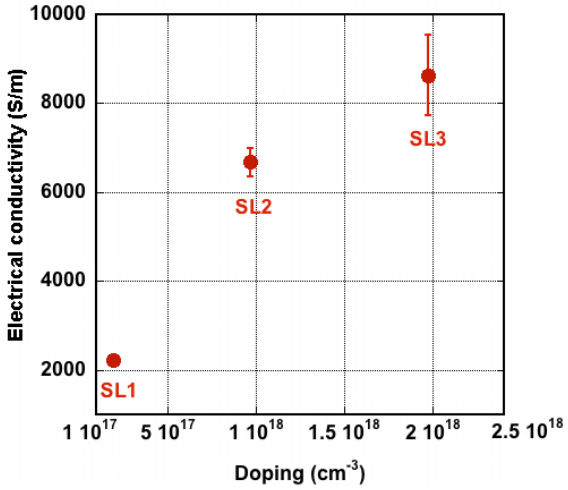

Figure 6.8: Electrical conductivity values for samples SL1, SL2 and SL3, the three of them belonged to the same design. The values have been plotted as a function of doping level, demonstrating higher σ for higher doping densities.

Sample ID	N (cm^{-3})	QW/barrier width (nm)	σ (S/m)
p-Ge [100]	7.1x10^{18}	bulk	30,300
p-$Si_{0.3}Ge_{0.7}$ [14, 111]	1.5x10^{20}	bulk	25,000
p-$Si_{0.188}Ge_{0.812}$ [9]	8.5x10^{18}	bulk	23,000
p-Ge/$Si_{0.25}Ge_{0.75}$ [9]	7.7x10^{18}	9.05/17.13	77,169
SL1	1.9x10^{17}	3.03/0.97	$2,220 \pm 62$
SL2	9.7x10^{17}	2.57/0.82	$6,680 \pm 8630$
SL3	2.0x10^{18}	3.43/1.17	$8,630 \pm 910$
SL4	δ: 1.2x10^{18}	2.48/1.12	$17,600 \pm 3,3330$
SL5	2.0x10^{18}	1.18/0.51	$15,500 \pm 1,490$

Table 6.1: A comparison of bulk Si, bulk Ge, Si/Ge superlattice and SiGe alloy electrical conductivities from the literature and from the present work. The QW widths were extracted from HRXRD measurements of each sample.

The measured values of σ are presented in table 6.1 and are compared with bulk p-Ge and p-SiGe results reported in the literature. All the σ values are smaller than bulk p-Ge and p-SiGe due to the additional interface roughness scattering at the Ge/$Si_{0.5}Ge_{0.5}$ interfaces.

6.3.2 Seebeck coefficient

In order to measure the Seebeck voltage across the SL, a uniform heat had to flow perpendicular to the multi-quantum well structure assuring a sufficient ΔT between the top and the bottom of the SL.

Finite element analysis of different structures was studied prior to the design and fabrication of the structure presented in Figure 6.4, refer to (Appendix A). Figure 6.9 shows the solution obtained for a similar device to the one used to characterise the material.

The device consisted of a 4 μm thick mesa structure with a top 50 nm layer of Ni to create the top ohmic contact and a 33 nm layer of NiCr to create the heater, as shown in Figure 6.9 *c*). The heater was placed on top of the Ni layer separated by 50 nm of Si_3N_4 to isolate one from the other. The area of the heater was 70x170 μm^2 and a 100 nm thick layer of Au was used as beams to power the heater. The inputs for the solution are:

- The geometry of the device.
- The power applied to the heater.
- Thermal conductivity of every single layer involved in the analysis, including κ values for the Ni, NiCr, Au and Si_3N_4 layer plus the SL itself.

As the κ value for the SL was ignored at that moment a value of $10\,W/m \cdot K$ was selected as a first choice. Figures 6.9 *a*) and *b*) demonstrate the temperature profile at the top of the heater and at the bottom of the mesa structure respectively. The temperature profile has been also plotted in *d*) for these two different heights as a function of position, moving along the Y-axes. This direction is indicated in both images by an orange arrow.

The solution suggested that a square shaped heater could produce a uniform heat flow down the SL and spreading in every direction once the heat had reached the bottom of the mesa due to the presence of the substrate. Because of the experience gained with the lateral devices (Chapter 5), it was expected to see some heat flowing in the in-plane direction due to the presence of parasitic channels. However, the scenario was completely different from the lateral devices where the substrate had been etched away forming a suspended membrane. For vertical devices, the simulation seemed to indicate that the heat could just flow in 1-dimension (perpendicular to the SL) and so the cross sectional area of the heat flux could be considered to be the same as the heater area. It has to be

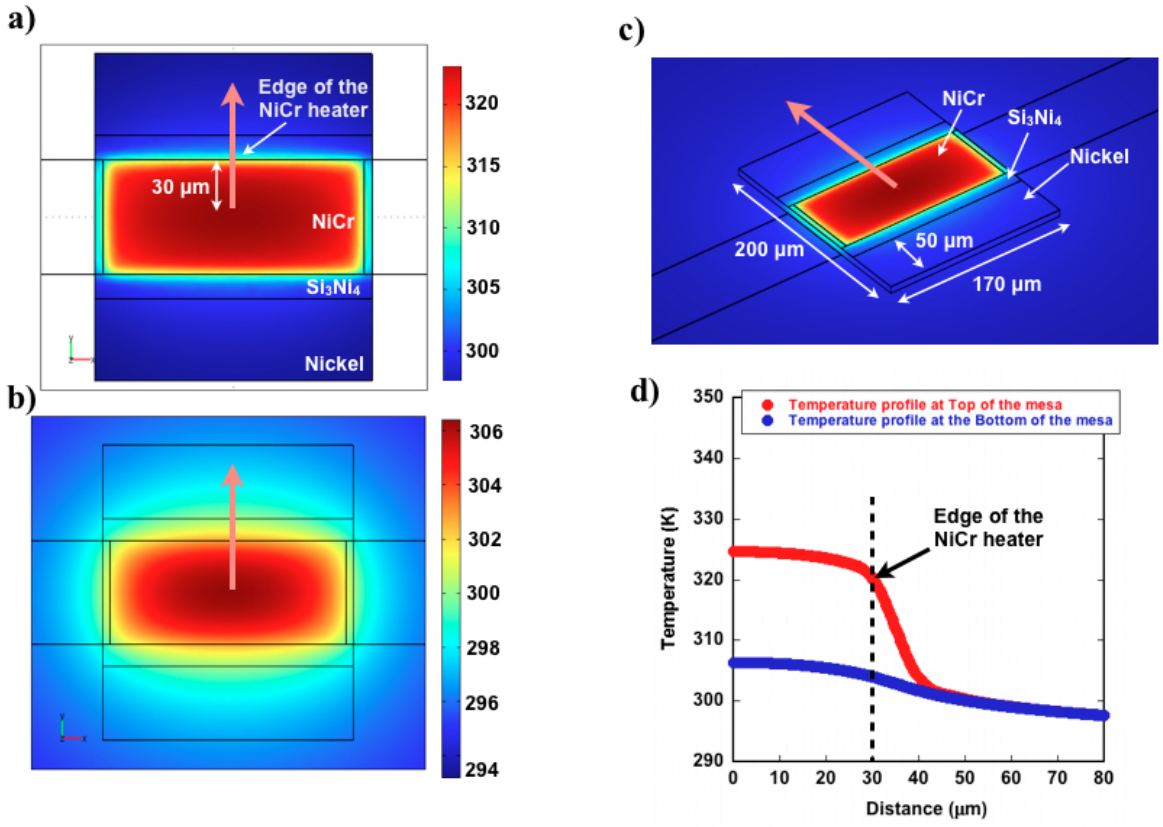

Figure 6.9: Finite element analysis of a vertical device, with a top Nickel contact aligned and separated from a NiCr heater by 50 nm of Si_3N_4 (courtesy of Yuan Zhang). *a*) Shows the temperature analysis made at the top of the device, *b*) demonstrates the simulation of the temperature at the bottom of it and *c*) shows the 3D geometry of the device. *d*) Temperature profile of the top and bottom of the device as a function of position, the orange arrow in *a*), *b*) and *c*) indicates the direction of the position.

noted that the heater size was 70x170 μm^2 while the thickness of the SL and therefore the mesa structure thickness was only 4 μm. This simulated 1-D model where the area of the heat transfer was the same as the area of the heater had still to be experimentally proved, this is explained later in Section 6.3.3.

Under the assumption of a uniform heat flux flowing perpendicular to the SL, α was calculated after measuring the Seebeck voltage as a function of ΔT. A dc current was applied to the NiCr heater and a set up with lock-in amplifier was used to monitor

the voltage changes of both top and bottom thermometers. Both thermometers were connected individually in series with a high precision resistor of 1 kΩ and another set up of lock-in amplifiers measured the voltage dropped in the resistors. The resistor was only used to obtain the current (I_2) passing through the thermometers and therefore to calculate the resistance of the thermometer at different heater powers (I_1). The Seebeck voltage was measured by a voltmeter.

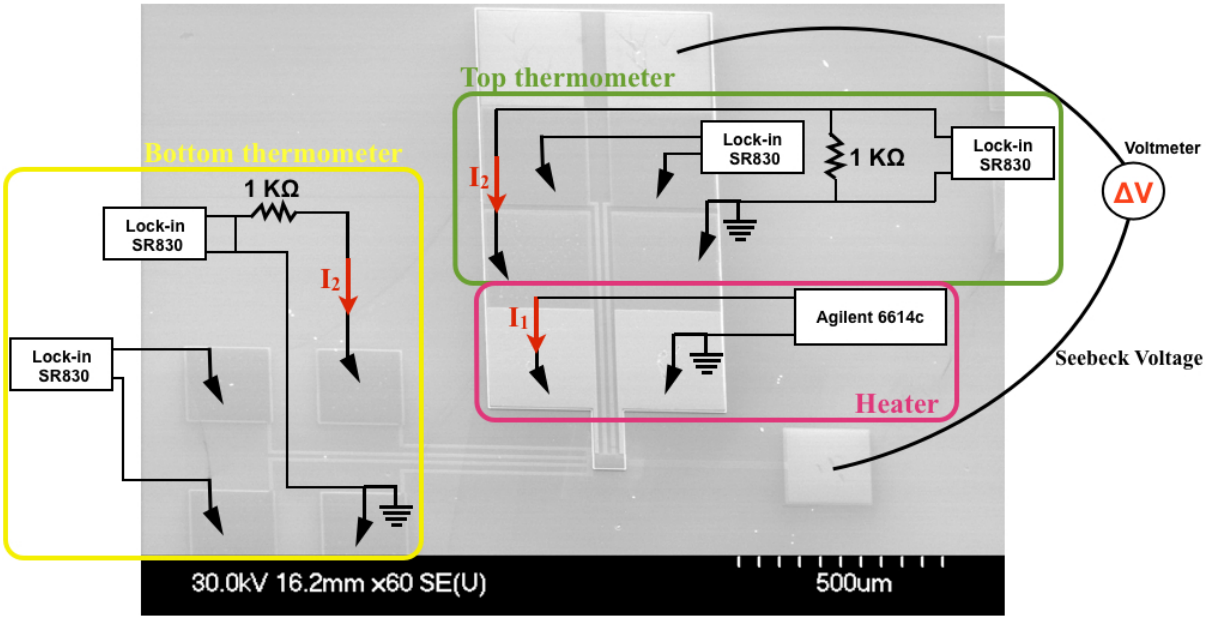

Figure 6.10: A SEM image showing the device with the electrical connections and instruments used to perform the Seebeck coefficient measurement.

Figure 6.10 shows a SEM image of a device with the electrical connections and instruments used to perform the Seebeck coefficient measurement. It has to be pointed out that the device shown in Figure 6.10 is slightly different to the one presented in Figure 6.4 *a*), as the SL at one side of the heater had been etched away. This is explained later in Section 6.3.3 but the configuration of the measurement was exactly the same for both devices.

The TCR of the thermometers was $0.00205 \pm 0.00006\,1/\mathrm{K}$, which allows translation of the change in resistance into a change of temperature and giving an accurate measurement of the ΔT.

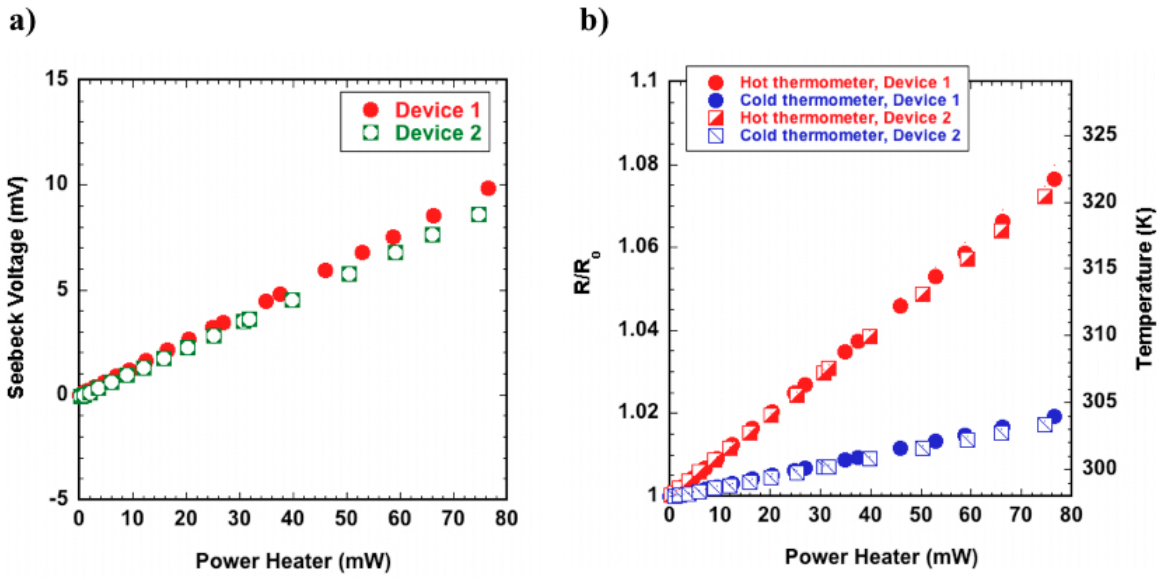

Figure 6.11: *a*) Seebeck voltage measured on two different devices as a function of heater power. *b*) Temperature profile for both thermometers on the same two devices as a function of heater power. The data shown was collected for SL1.

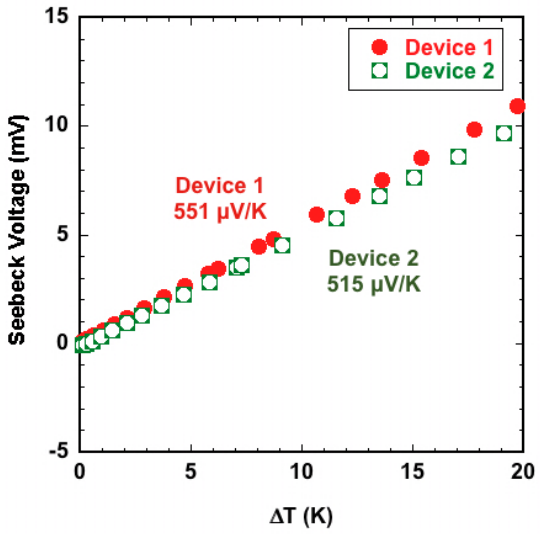

Figure 6.12: Seebeck voltage plotted as a function of ΔT for the data demonstrated in Figure 6.11.

Figure 6.11 shows a set of data analysed for two identical devices (Figure 6.4 *a*)) where, *a*) shows the Seebeck voltage as a function of heater power, *b*) shows the temperature profile for both thermometers as a function of heater power and Figure 6.12 shows the Seebeck voltages plotted as a function of ΔT. The gradient of the straight line fit of the data presented in Figure 6.12 gives the value of α, obtaining in this case an average value of $533 \pm 25\,\mu$V/K for SL1. The error quoted for α is the standard deviation of the two separate data sets presented in Figure 6.12.

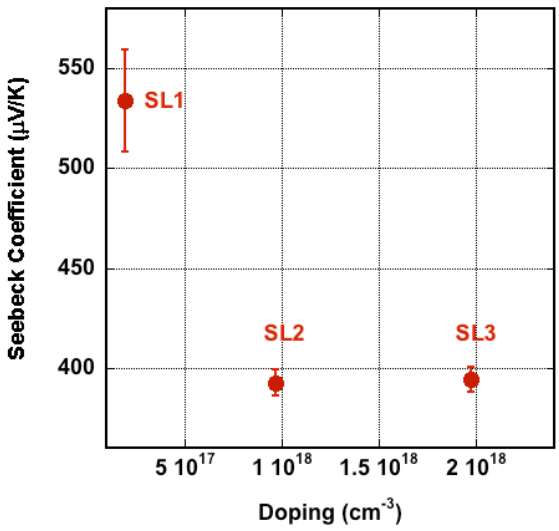

Figure 6.13: Seebeck coefficient as a function of doping level for SL1, SL2 and SL3.

Figure 6.13 shows the Seebeck coefficient measured for SL1, SL2 and SL3 as a function of doping density. The highest value is presented by SL1 with a doping density of $1.9\text{x}10^{17}\,\text{cm}^{-3}$.

SL4 and SL5 presented α values of $113 \pm 7\,\mu$V/K and $91.8 \pm 2.8\,\mu$/K respectively, values that were comparable to bulk SiGe [14] and SiGe quantum dot [23]. These results suggested that holes saw the material as a random bulk alloy rather than a superlattice. This bulk behaviour could be expected for SL5 which presented QW and barrier thicknesses of 1.18 nm and 0.5 nm but it is still not clear why the value obtained for SL4 was so low, as the device follows the same design as SL3 but with δ-doping.

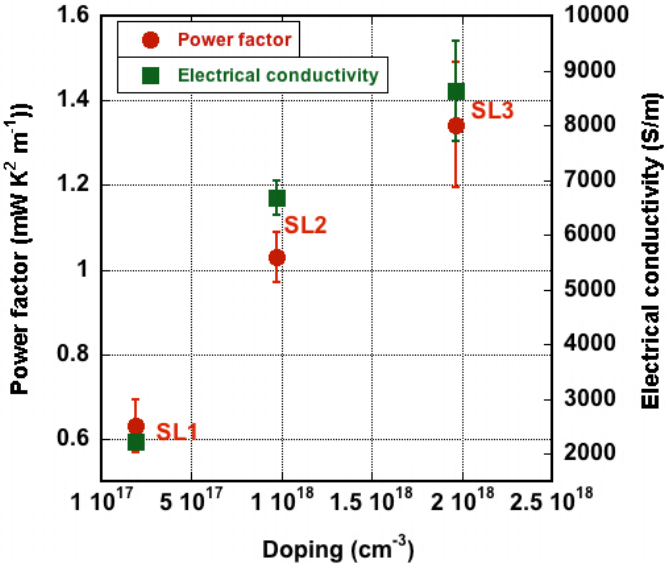

Figure 6.14: Power factor plotted as a function of doping level, additionally showing the values obtained for σ. It is quite clear that the power factor follows the same trend as the electrical conductivity values.

Sample ID	N (cm^{-3})	QW/barrier width (nm)	α ($\mu V/K$)	PF (mW/K^2m)
p-Ge [100]	7.1x10^{18}	bulk	300	2.73
p-$Si_{0.3}Ge_{0.7}$ [14, 111]	1.5x10^{20}	bulk	90	1.26
p-$Si_{0.188}Ge_{0.812}$ [9]	8.5x10^{18}	bulk	298	2.62
p-Ge/$Si_{0.25}Ge_{0.75}$ [9]	7.7x10^{18}	9.05/17.13	279.5	6.02
SL1	1.9x10^{17}	3.03/0.97	533 ± 25	0.63 ± 0.06
SL2	9.7x10^{17}	2.57/0.82	393 ± 7	1.03 ± 0.06
SL3	2.0x10^{18}	3.43/1.17	394 ± 6	1.34 ± 0.15
SL4	δ: 1.2x10^{18}	2.48/1.12	113 ± 7	0.22 ± 0.05
SL5	2.0x10^{18}	1.18/0.51	91.8 ± 2.8	0.13 ± 0.015

Table 6.2: A comparison of bulk Si, bulk Ge, bulk Si/Ge and bulk SiGe Seebeck coefficients and power factors from the literature and from the present work.

Figure 6.14 shows the power factor achieved for SL1, SL2 and SL3. The highest value of $\alpha^2\sigma$ was obtained for samples with a doping density of 2.0x10^{18} cm^{-3} (SL3), which result was comparable to the best power factor obtained for p-SiGe alloys, see table 6.2

to compare results. The values obtained for SL4 and SL5 were 0.22 and 0.13 mW/Km respectively.

6.3.3 Thermal Conductivity

Thermal measurements were problematic because any physical connection to the thermometers or heaters produced parasitic heat paths which perturbed the measurements. For lateral test structures, methods to measure the parasitic heat paths to allow accurate measurements of the heat flowing down the structure were developed in [9] (also presented in Chapter 5). After the experience gained analysing the lateral devices, a similar approach was undertaken to estimate the thermal conductivity of the vertical structures.

A differential method was used to calculate the heat lost through parasitic channels. The test structure shown in 6.15 *a*) (full device) consisted of a heater placed in the middle of a large mesa structure where it could not be assumed that all of the power applied to the heater was travelling perpendicular to the superlattice. A second device identical to the first one, was designed, but in this case the SL at one side of the heater had been etched away, see diagram in Figure 6.15 *b*) (half device).

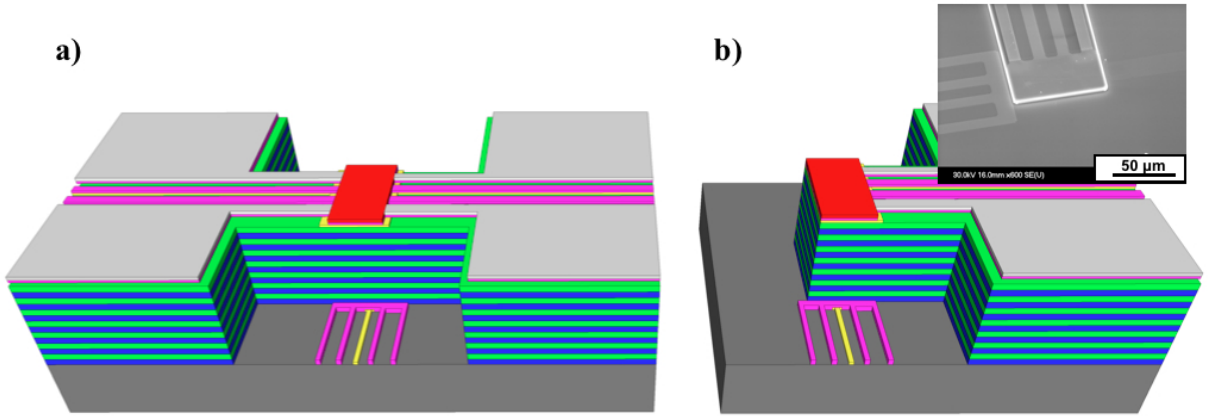

Figure 6.15: *a*) Schematic diagram of a full device, the device itself is placed on the center of a symmetric mesa structure. *b*) Schematic diagram of a half device, where the device itself is this time placed at the edge of a mesa structure. These two devices were used as a differential technique to measure the thermal conductivity.

Figure 6.16 *a*) shows a top view of a full device that had both the in-plane (lateral) and

cross-plane (vertical) heat transport. To be able to measure the parasitic thermal paths of the in-plane direction from both the superlattice and the electrical interconnects, a second device was fabricated to estimate the heat flux flowing in the cross-plane direction, see Figure 6.16 *b*). Twice this parasitic thermal contribution had to be subtracted to obtain an accurate estimate of the heat flux travelling down the structure.

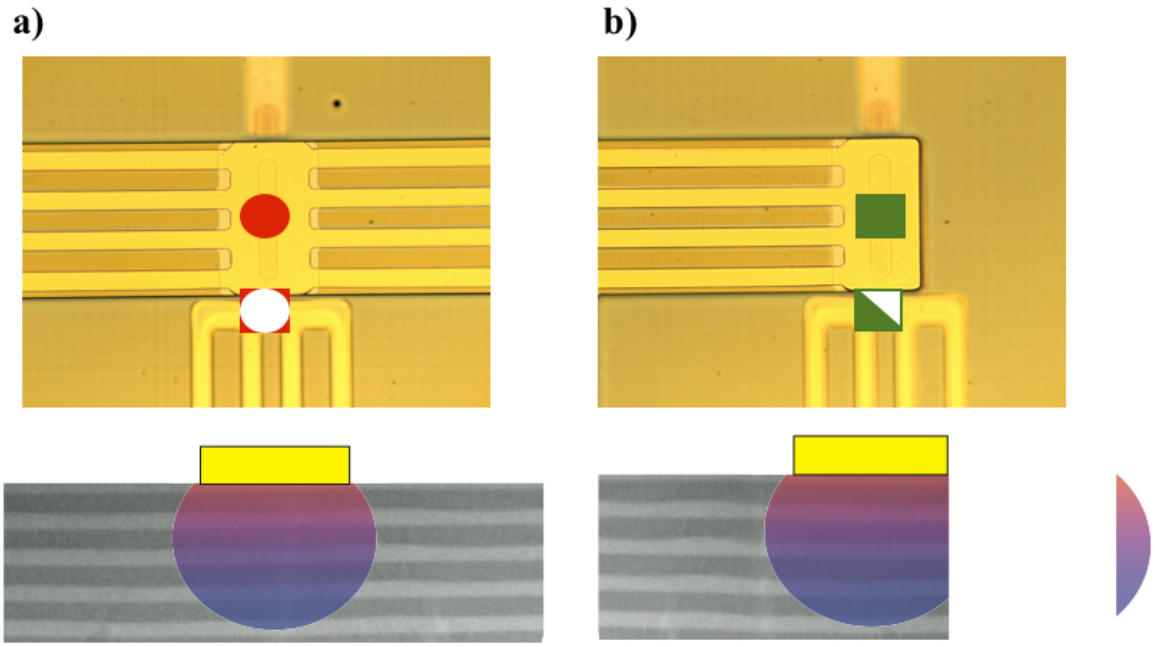

Figure 6.16: *a*) Optical top image of a full device, the device is placed in the middle of a symmetric mesa structure. *b*) Optical top image of a half device, this was identical to the full device showed in *a*), but with the difference that the SL at one side of the heater had been etched away.

Figure 6.17 shows the experimental data for the temperature measurements as a function of heater power for the top and bottom thermometers on both devices.

The results indicated only small changes between the full and half devices suggesting only a small perturbation from the lateral heat transport. This kind of behaviour was already expected due to the information obtained from previous finite element analysis on similar devices, see Section 6.3.2. The solution of the simulation indicated that due to the geometry of the heater and the thickness of the thin film a 1-D model heat transfer was likely to happen. This consideration made the analysis of the data much easier and Fourier's law:

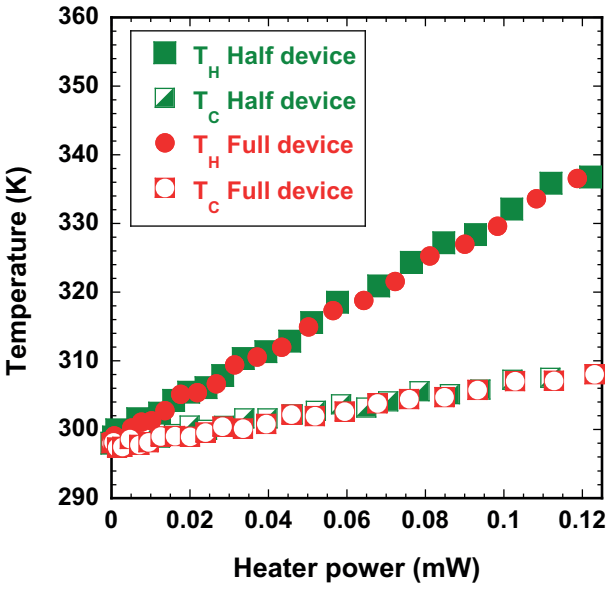

Figure 6.17: Temperature profile measured as a function of heater power for the two devices illustrated in Figure 6.16. The temperature is almost the same for both devices indicating that for this device geometry and material most of the power applied for the heater is travelling perpendicular to the SL.

$$\kappa = Q\frac{\Delta T A}{L}, \tag{6.1}$$

was used to calculate the value of κ in the cross-plane direction. Q was the heat power applied to the heater, ΔT was the temperature difference between top and bottom thermometers, L was the thickness of the mesa structure and A was the area of the NiCr heater. The area of the heat flux was considered the same as the area of the heater due to the weak influence of the lateral transport, as demonstrated in Figure 6.17.

This technique was cross checked by measuring SiO_2 reference samples which produced κ of $1.7 \pm 0.6\,\mathrm{W/m \cdot K}$, values that compare well with the literature numbers of $1.6\,\mathrm{W/m \cdot K}$ [46].

It should be noted that even if the lateral contribution could be neglected due to the geometry of the device, the value of κ was still augmented due to the additional thermal conductivities of the Ti/Pd, Si_3N_4 and Ni layers underneath the heater, thus overestimating the value of the thermal conductivity. The thermometer at the bottom of the SL measured the temperature at the edge of the bottom mesa structure which also

overestimated the value of ΔT and therefore the value of κ.

The thermal conductivities were between 5.1 and 5.6 $W/m \cdot K$, see table 6.3, which are lower than comparable doped bulk $Si_{0.3}Ge_{0.7}$ [14] but higher than undoped Si/Ge superlattices [70, 72]. An undoped superlattice (SL6) with the same design as SL1, SL2 and SL3 was also tested for comparison. The value measured for SL6 was of $5.28 \pm 0.4\,W/m \cdot K$, suggesting that the lattice contribution dominated the value of κ for cross-plane properties. This results has already been observed in [118] for InGaAs/InGaAlAs superlattices.

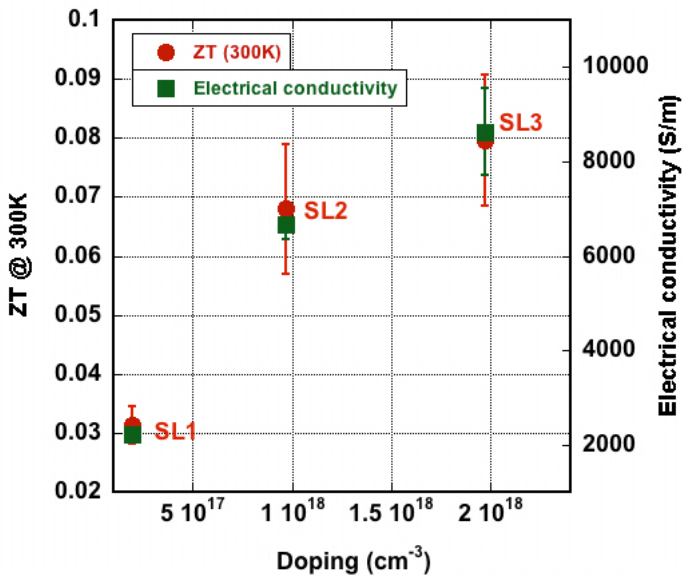

Figure 6.18: The figure of merit ZT, plotted as a function of doping density. The trend of ZT follows the same behaviour as the electrical conductivity values, also shown in the figure.

Figure 6.18 demonstrates the value of ZT as a function of doping level for SL1, SL2 and SL3. The figure of merit was higher for samples with higher doping densities following the same trend as the electrical conductivities (also shown in the plot). The highest ZT obtained was 0.08 for SL3, 4 times higher than bulk SiGe alloys with comparable Ge content and doping density [22].

SL4 and SL5 presented ZTs of 0.012 ± 0.003 and 0.0077 ± 0.0001 respectively, which were lower than bulk p-SiGe alloys in [22]. This reduced values of ZT were mainly due to the lower values of α observed, shown in table 6.3.

Sample ID	N cm^{-3}	QW/barrier width (nm)	σ S/m	α $\mu V/K$	κ $W/m \cdot K$	ZT 300 K
p-Ge [100]	7.1x10^{18}	bulk	30,300	300	59.5	0.014
p-$Si_{0.3}Ge_{0.7}$ [14, 111]	1.5x10^{20}	bulk	25,000	90	6.3	0.013
p-$Si_{0.188}Ge_{0.812}$ [9]	8.5x10^{18}	bulk	23,000	298	40.3	0.019
p-Ge/$Si_{0.25}Ge_{0.75}$ [9]	7.7x10^{18}	9.05/17.13	77,169	279.5	23.14	0.078
SL1	1.9x10^{17}	3.03/0.97	$2,220 \pm 62$	533 ± 25	6.0 ± 0.4	0.031 ± 0.003
SL2	9.7x10^{17}	2.57/0.82	$6,680 \pm 8630$	393 ± 7	4.5 ± 0.4	0.068 ± 0.010
SL3	2.0x10^{18}	3.43/1.17	$8,630 \pm 910$	394 ± 6	5.1 ± 0.4	0.08 ± 0.011
SL4	δ: 1.2x10^{18}	2.48/1.12	$17,600 \pm 3,3330$	113 ± 7	5.6 ± 0.3	0.012 ± 0.0027
SL5	2.0x10^{18}	1.18/0.51	$15,500 \pm 1,490$	91.8 ± 2.8	5.1 ± 0.1	0.0077 ± 0.0001
SL6	undoped	2.6/0.9	-	-	5.28 ± 0.4	-

Table 6.3: A comparison of Si, Ge, Si/Ge and SiGe thermoelectric parameters from the literature and the present work. The QW widths were extracted from HRXRD measurements of each sample.

6.4 Conclusions

Three p-type Ge/$Si_{0.5}Ge_{0.5}$ superlattices (SL1, SL2 and SL3) have been studied as a function of doping density. In order to extract the thermoelectric properties two different devices have been developed and fabricated to test the different designs.

The electrical conductivity increased by 25% from the lowest to the highest doping density and the Seebeck coefficient was reduced by the same percentage. Since the PF is defined by $\alpha^2\sigma$, this increased by a factor of 2.1 reaching a maximum value of 1.34 mW/K^{2}m for a doping density of 2.0x10^{18}. This result is very modest compared to the in-plane values, as had been already reported in Chapter 5 for p-$Si_{0.188}Ge_{0.812}$ alloys and p-Ge/$Si_{0.25}Ge_{0.75}$ superlattices and even smaller than PF for p-Ge material reported in the literature [100]. The main difference was due to the small σ values obtained in the cross-plane direction which were expected to be 4 or 5 times smaller than the in-plane ones, as it had been already reported in the literature [39].

These values were also compared with an identical sample (SL4) that had been selectively doped and with another sample (SL5) which had been uniformly doped but for which the QW and barrier thicknesses had been reduced by a factor of 0.4. Both presented larger σ values but much reduced α values.

As demonstrated in Chapter 5, modulation doped superlattices present larger electrical conductivities due to improved carrier mobilities, which explain the enhanced value of σ for SL4. On the other hand, SL5 presented an α value of 91 μVK, comparable to p-$Si_{0.3}Ge_{0.7}$ alloys [14, 111], suggesting that the holes saw the material as a random bulk alloy rather than a superlattice.

The thermal conductivities measured for the five samples were between 4.5 and 6 $W/m \cdot K$ without following a clear trend versus the doping density. The value of κ in the cross-plane direction seems to be independent of the doping density and therefore dominated by the lattice thermal contribution rather than the electronic. Further reducing the lattice contribution without disturbing the electronic conductivity of the material is one of the advantages offered by superlattices and a key requirement to gaining high efficiencies together with high power outputs.

The highest ZT measured for this set of samples was 0.08, for SL3. This ZT value is the same as the highest one reported for lateral p-Ge/$Si_{0.25}Ge_{0.75}$ superlattices, see Chapter 5. Even if both samples presented the same efficiency, the PF for lateral p-Ge/$Si_{0.25}Ge_{0.75}$ superlattices was 4.5 times higher than the one presented for SL3, indicating that the potential parameters for the set of samples studied within this chapter was the substantial reduction of the thermal conductivity and the increase of the Seebeck coefficient.

To conclude, it should be noted that interface roughness could be a limiting factor for the current values of σ, featuring low power factors. Interface roughness in SiGe materials is known to increase as a function of strain (and therefore Ge content difference) [119], suggesting that a reduction in the strain difference (Ge content difference) between the QWs and barriers could increase σ resulting in higher power factors and ZTs. A reduction of the Ge content difference is studied on a second set of n-type superlattices presented and studied in Chapter 7.

Chapter 7

Thermoelectric Characterisation in the cross-plane direction for n-Ge/$Si_{0.3}Ge_{0.7}$ Superlattices

This chapter investigates the thermoelectric properties of n-Ge/$Si_{0.3}Ge_{0.7}$ superlattices, where the heat and carrier transport occurs perpendicular to the superlattice.

Two sets of experiments are carried out with a set of four different n-type designs. One experiment studies the impact that QW thickness might have on the figure of merit ZT. A second experiment focusses on the effect that the addition of different barrier thicknesses to a period could produce a more effective scattering of acoustic phonons, reducing the thermal conductivity.

Measurement techniques and results for σ, α and κ are presented as well as the values obtained for ZT and $\alpha^2\sigma$. One of the designs was tested as a function of temperature; the results and conclusions are given at the end of the first experiment.

7.1 Material Design and Growth

Four different n-type vertical designs featuring 4 μm thick SLs with top and bottom contact layers were studied and analysed in this Chapter.

As for the designs studied in Chapter 6, the heat and carrier conduction also arised perpendicular to the superlattice, but in this case the Ge content difference between QWs

and barriers was lower and all of the designs were uniformly doped, aiming for the same doping density.

Lower Ge content difference was chosen to reduce the interface roughness, which depends on the strain of the material and therefore on the Ge content difference as shown in [119]. Reducing the interface roughness should help to increase the cross-plane electrical conductivity, which in Chapter 6 was demonstrated to be the weakest point in achieving high ZT and PF.

The dopant used was PH_3 with an estimated dopant density of $1x10^{19}\,cm^{-3}$ in the superlattice and $3x10^{19}\,cm^{-3}$ for the bottom and top contacts. The average Ge content in the active structures varied between 90% and 95% depending on the design [116].

All of the samples were grown using low-energy plasma enhanced chemical vapor deposition (LEPECVD). A $\sim 13\,\mu m$ graded buffer layer from Si to $Si_{0.1}Ge_{0.9}$ was grown at rates of 5 and 10 nm/s. A 500 nm thick layer of n-$Si_{0.1}Ge_{0.9}$ with a doping density of $3x10^{19}\,cm^{-3}$ was grown on top of the virtual substrate. The active areas were grown at rates of 1.0 to 1.5 nm/s and to finish a 60 nm thick cap layer of n-Ge, with a doping density again of $3x10^{19}\,cm^{-3}$, was grown for a top ohmic contact [7].

As described in Section 2.4.1.1, the presence of heterointerfaces in SL structures contributes to the reduction of the phonon thermal conductivity by scattering the phonons. A previous study [2] demonstrated that the acoustic phonon wavelengths that carried the majority of the heat were between 1.2 and 3.5 nm, refer to Figure 1.6. This range of wavelengths could block the 95% of the heat transferred by acoustic phonons, potentially reducing the thermal conductivity by featuring multilayer structures with barrier thicknesses comparable to these wavelenghts.

The first experiment focused in studying how thin or thick QWs impacted on the efficiency of the material. Thinner QWs should present larger values for α [35] but poorer values for σ, as carriers could be significantly scattered by the presence of multiple layers. Two n-type Ge/$Si_{0.3}Ge_{0.7}$ superlattices were studied for this purpose.

SL10 featured a period formed by a 3 nm thick n-Ge QW layer and a 1.5 nm thick n-$Si_{0.3}Ge_{0.7}$ barrier layer. This stack was repeated 889 times to grow a $4\,\mu m$ thick superlattice. SL11 featured a superlattice unit cell with a 9 nm thick n-Ge QW and a 1.5 nm

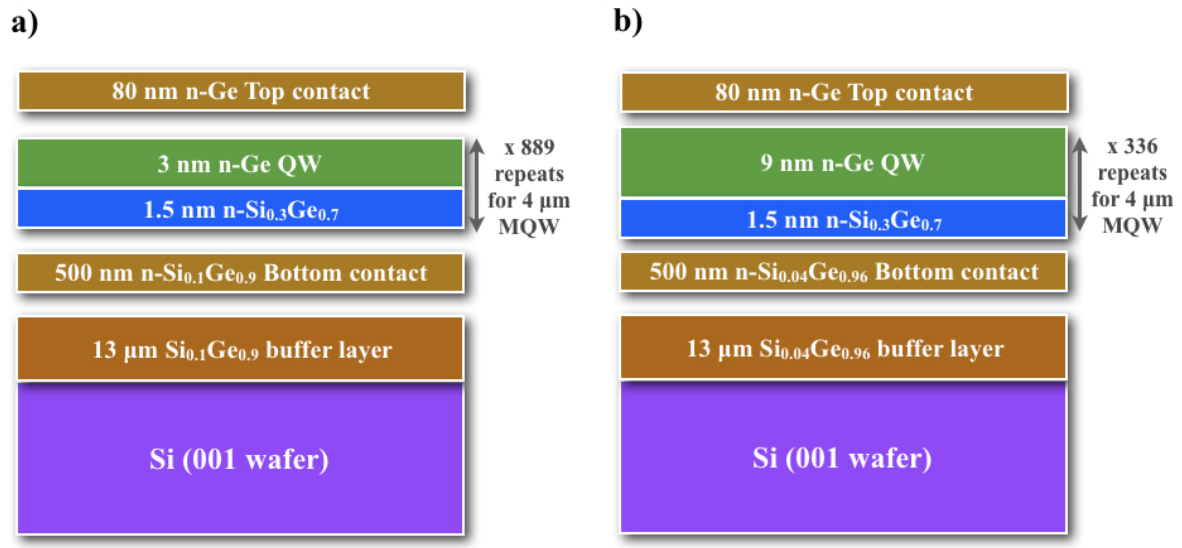

Figure 7.1: Schematic diagram of the n-type vertical designs unit cells. Figure *a*) corresponds to SL10 with thin QWs and *b*) to SL11 with wider QWs.

thick n-$Si_{0.3}Ge_{0.7}$ barrier. This period was then repeated 336 times to get the same total thickness. Figure 7.1 shows the schematic diagrams for both designs.

The second experiment studied a set of three samples where the number of barriers was increased with the aim of scattering acoustic phonons more efficiently. The barrier thickness was kept in the range 1.2-3.5 nm. SL12 and SL13 were grown as a complement to SL11. For SL12, the unit cell was formed by a 9 nm thick n-Ge QW and two n-$Si_{0.3}Ge_{0.7}$ barrier layers with thicknesses of 1.5 and 3 nm. SL13 had a unit cell formed by a 9 nm thick n-Ge QW and three n-$Si_{0.3}Ge_{0.7}$ barrier layers width thicknesses of 1.5, 3 and 4.5 nm. Both periods were then repeated 178 and 111 times, respectively to get 4 μm thick SLs. These three designs are shown in Figure 7.2 for comparison.

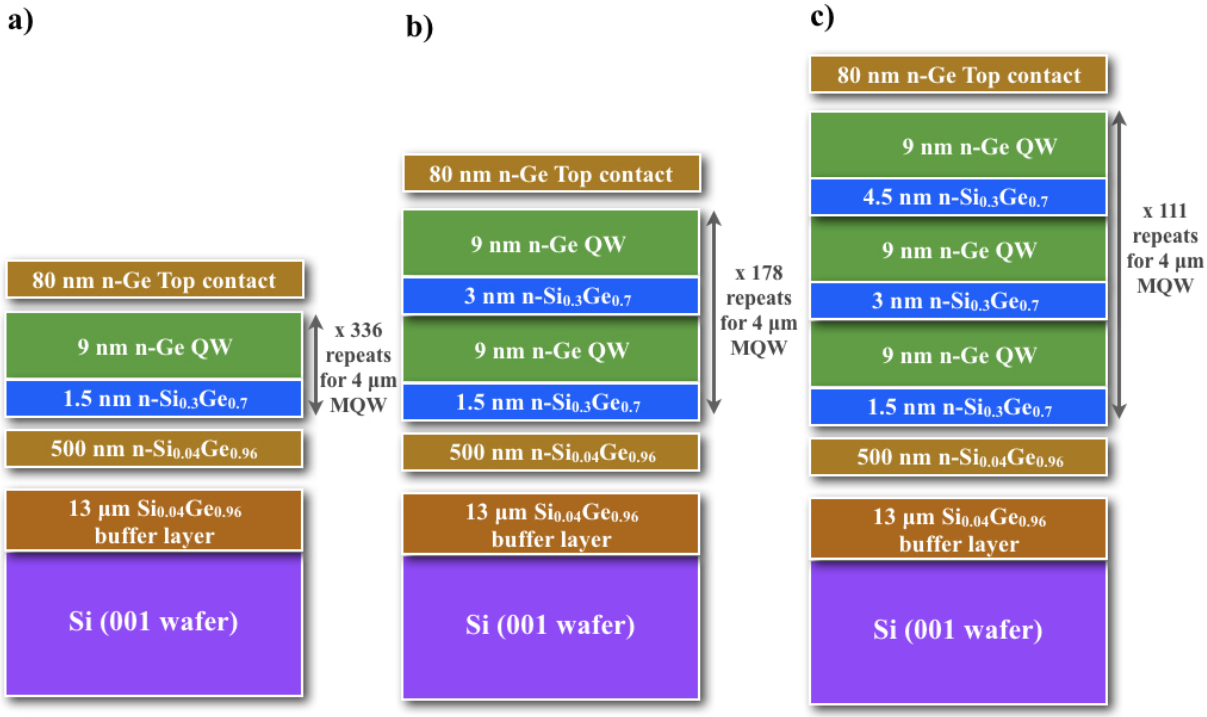

Figure 7.2: Schematic diagram of the n-type vertical designs unit cells. Figure *a*) Corresponds to SL11 width one barrier, *b*) to SL12 with two barriers and *c*) to SL13 with three barriers per period.

7.1.1 Physical Characterisation

Transmission electron microscopy (TEM) was used to measure individual layer thicknesses of the material as well as to investigate the TDD.

Figure 7.3 shows two cross section TEM images from the top and bottom of the SL for SL10. The SL period measured was of 6.2 nm for both, the top and bottom layers [116].

No significant threading dislocation density could be seen using TEM, suggesting that the values were bellow $10^8\,\mathrm{cm}^{-2}$.

Figure 7.4 shows two cross section TEM images from the top and bottom of the SL for SL13. The layers at the top of the SL seemed to be better defined and also narrower than the ones at the bottom, even though the period thicknesses measured were of 43.40 nm and 43.45 nm, respectively. High resolution TEM images also showed the presence of local lateral variations in the barrier thicknesses, which were quite visible for top layers but

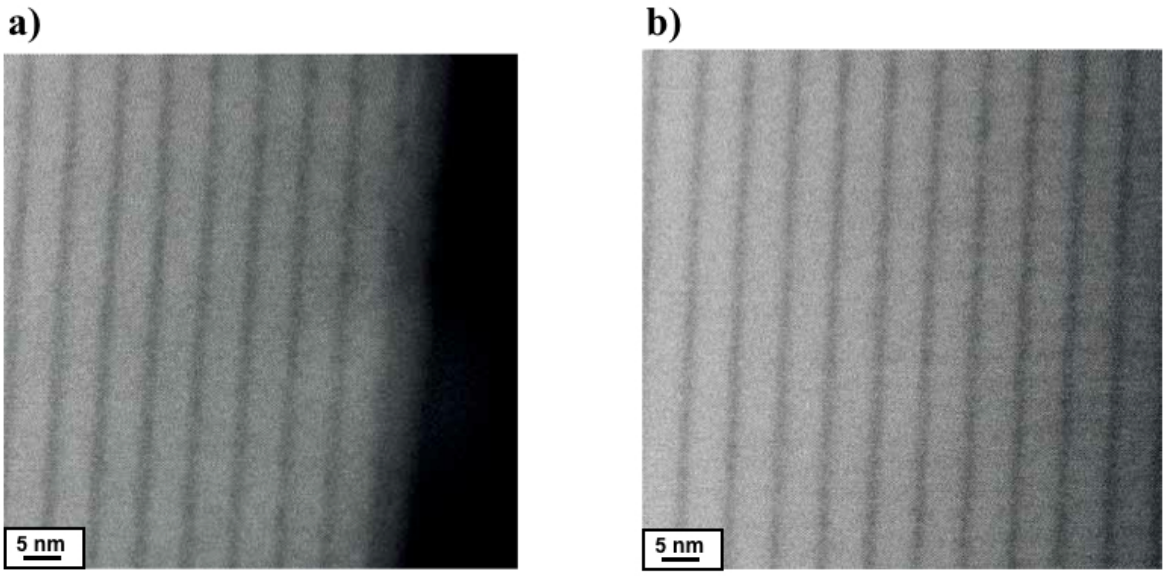

Figure 7.3: Two TEM images of the top and bottom of the superlattice for SL10. *a*) shows the top of the superlattice while *b*) shows the bottom of it.

much more blurred for the bottom ones making measurements more difficult. Figure 7.5 shows two HRTEM images of the top and bottom of the SL for SL13, where the barrier thicknesses were clearly decreasing from the first to the third layers.

HRXRD was also used to physically characterize the material, measuring individual layer thicknesses and Ge compositions for the different devices. The average Ge content was found to change between 90% and 95% depending on the design [116]. HRXRD also indicated that all the superlattices were strain symmetrized to the $Si_{0.1}Ge_{0.9}$ virtual substrates [116].

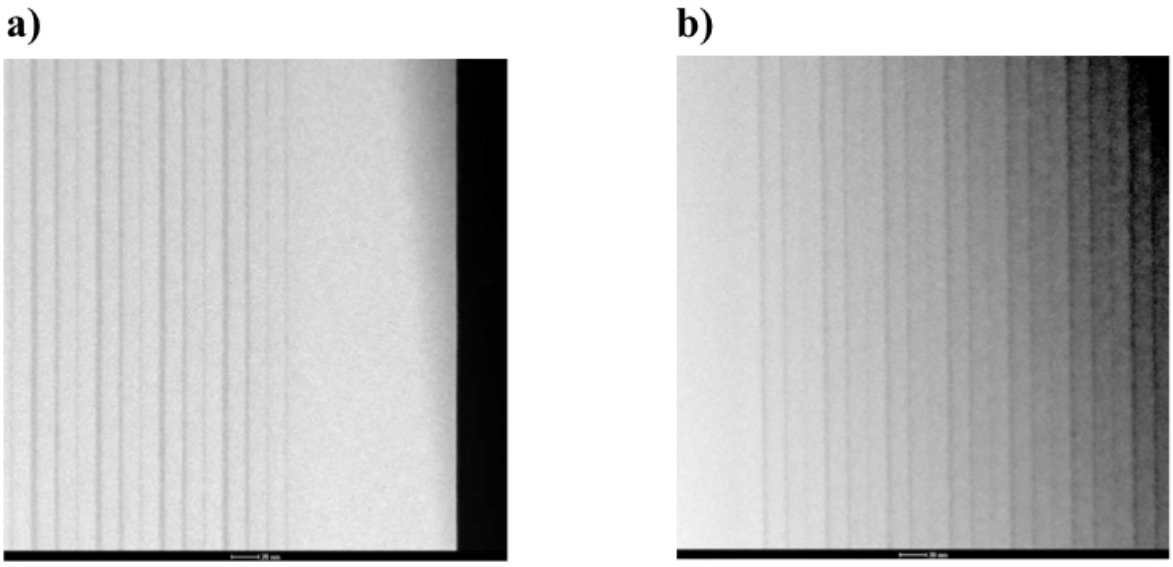

Figure 7.4: *a*) A TEM image of the top of the SL with individual layer thicknesses of 14.9/2.5/14.3/1.78/13.9/1.3 nm (from left to rigth). *b*) A TEM image of the bottom of the SL with individual layer thicknesses of 15.3/3.4/14.3/2.8/13.9/1.2 nm (from left to right).

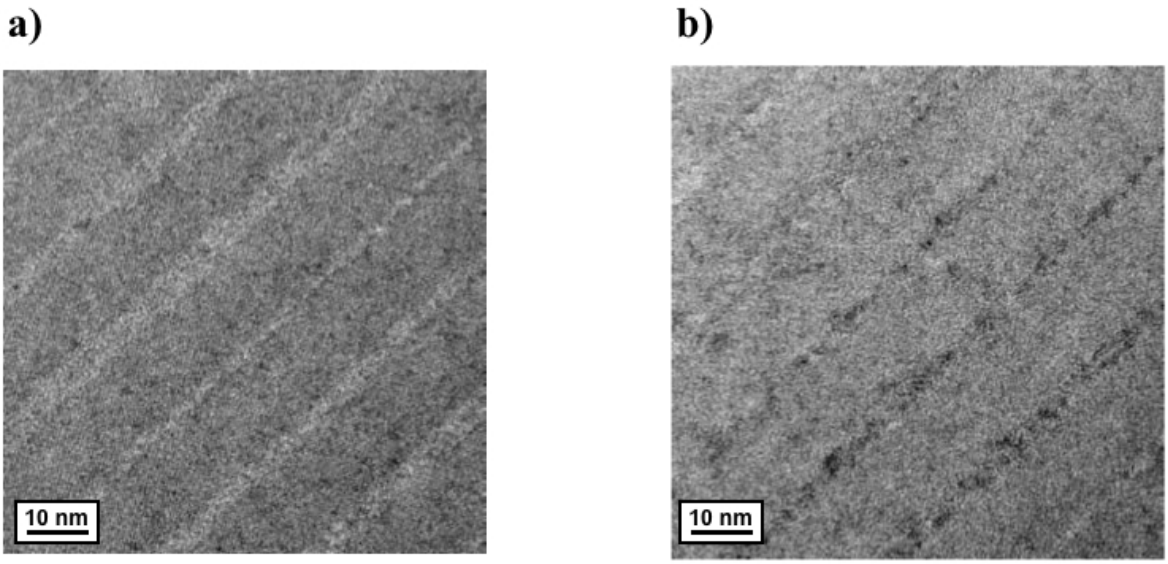

Figure 7.5: *a*) A HRTEM image of the top of SL13, and *b*) a HRTEM image of the bottom of SL13.

7.2 Device Fabrication

The same testing devices presented in section 6.2 and used to characterise p-type vertical SL were used to characterise the n-type vertical SL. The fabrication only differed in the metal used to create ohmic contacts to n-type Ge.

Initially nickel was used to create good ohmic contacts as it was used for p-type superlattices and also demonstrated in [117]. Unfortunately, even if the top and bottom contact layers were highly doped with doping densities up to $3\text{x}10^{19}\,\text{cm}^{-3}$, $I-V$ curves showed a clear Schottky contact. Although the doping density was high enough to create NiGe contacts the activation of the dopant was quite poor, creating a potential energy barrier for electrons to flow from the metal pads to the semiconductor.

A second approach using the deposition of a small percentage of antimony (an n-dopant) with silver was used to achieve good ohmic contacts. A small coil of wire made of Silver/Antimony (99 % and 1 %) was placed on top of a tungsten boat in a thermal evaporator. A current was applied to the boat, heating it to the point required to melt the metal and allow evaporation to take place.

For the devices used to measure α and κ, see Figure 5.14, 100 nm of Ag/Sb was deposited annealing for 5 minutes at $673K$, process used in [120].

For CTLM devices, used to extract the value of σ (Figure 2.6), 100 nm of Ag/Sb was again deposited using a thermal evaporator followed by the deposition of 50 nm of Pt plus 100 nm of Ni using an electron-beam evaporator.

Ni was required as a metal mask to etch the SL between the contacts and therefore an intermediate layer of Pt was required, to act as a diffusion barrier when annealing the contacts at 613 K for 5 minutes.

7.3 Impact of QW thickness on ZT

Figure 7.6 demonstrates the total resistance measured as a function of etch depth for SL10. Seven dry etches of ~ 500 nm were performed on CTLM structures until reaching the bottom contact layer, buried underneath the active area.

For n-type samples the data points were more scattered and the error bars for each point were bigger than the ones presented for p-type samples, as shown in Figure 5.8. It is worth remembering that, even if Ag/Sb was able to create ohmic contacts on n-type

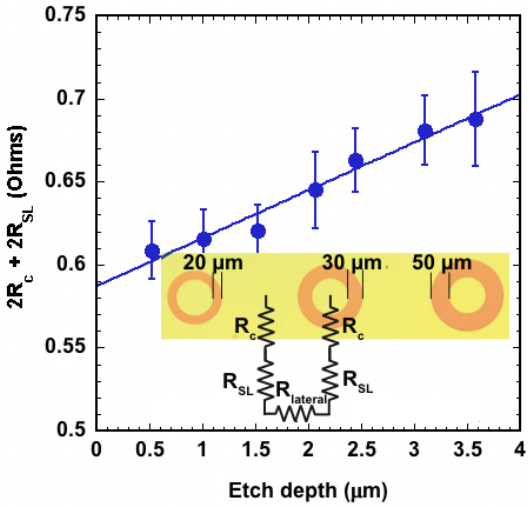

Figure 7.6: The 2 terminal electrical conductivity of sample 8719 SL10 as a function of etch depth.

Ge, the antimony acted solely as a dopant, and did not mix with the Ge layer. On the opposite side, when using Ni as a metal for contacts, the nickel was able to diffuse inside the material creating what is known as a nickel germanide contact. This scattering data was due to the quality of the contacts, causing larger error bars when fitting the data through least-square fits.

In addition, the n-type material was much more conductive than the p-type samples. This was first noticed from the measurement of total resistances which increase by a factor of 1.05 after each etch depth, while for the p-type samples the resistances increased by a factor of 1.2. This meant as expected, that the modified CTLM technique could only be used when the contact resistances were not overwhelming the sheet resistance, highlighting once more that optimised ohmic contacts were necessary for this technique.

The σ values measured for SL10 and SL11 were $50,200 \pm 4,200\,\mathrm{S/m}$ and $55,900 \pm 7,700\,\mathrm{S/m}$ respectively. These values are comparable, though SL11 presented a slightly higher electrical conductivity. This suggested that the QW width (3 times wider for SL11) dominated the value of σ aiming for higher electrical conductivities.

Figure 7.7 *a*) shows the Seebeck voltage measured as a function of temperature differ-

ence on two different devices for SL10. The α values for these two sets of measurements were $-449.21\,\mu V/K$ and $-461.61\,\mu V/K$, giving an average value of $-455 \pm 9\,\mu V/K$. This value should be compared with n-$Si_{0.2}Ge_{0.8}$ [14] and with bulk n-Ge [27] with similar doping densities, and with α values of $-300\,\mu V/K$ and $-308\,\mu V/K$ respectively. It is clear the enhancement of the Seebeck coefficient obtained for SL10 compared to its counterparts.

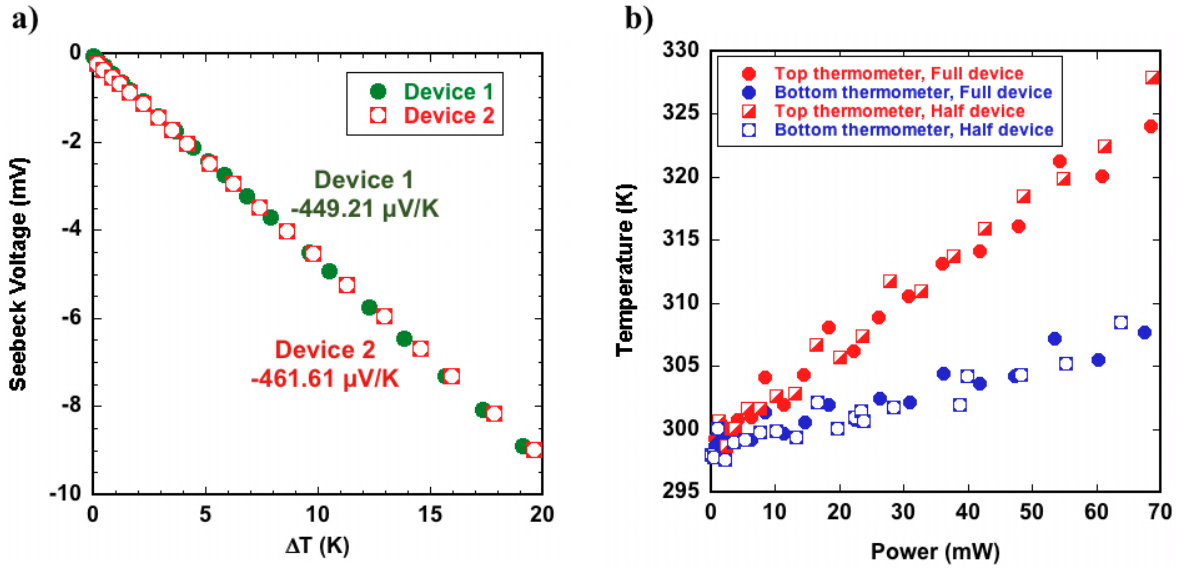

Figure 7.7: Seebeck voltage as a function of temperature difference between the top and bottom of the superlattice for SL10. Both measurements show a standard deviation of $9\,\mu V/K$.

On the contrary, SL11 presented an average α value of $-295 \pm 33\,\mu V/K$. This result is comparable to its bulk counterparts [14, 27] as well as to the lateral (in-plane direction) Seebeck coefficients presented in Chapter 5 [9]. Results presented in Chapter 5 correspond to p-type SL with similar doping densities and the same nominal QW thicknesses.

The anisotropy of the Seebeck coefficient seems to be smaller for wide QWs, whose values are also comparable to their bulk counterparts. This suggests that carriers still see the material as a 3D system, strongly limiting the enhancement of α.

Figure 7.7 *b*) shows the temperature profiles for both the full and half device (Figure 5.14) as a function of heater power. There was more variability in this measurement than the one presented for the p-type vertical devices (Figure 5.16) but linear fits to the results

indicated only a small variation between the full and half devices. The calculated thermal conductivities for SL10 and SL11 were $6.4 \pm 0.7\,\mathrm{W/m \cdot K}$ and $8.6 \pm 0.5\,\mathrm{W/m \cdot K}$, respectively.

These values are much smaller than bulk n-Ge with $\kappa = 59.9\,\mathrm{W/m \cdot K}$ [27] but still comparable to n-$Si_{0.2}Ge_{0.8}$ with $\kappa = 8.9\,\mathrm{W/m \cdot K}$ [14]. SiGe low dimension structures with comparable doping densities tend to show thermal conductivity values at least two times smaller than the ones presented in this work [23, 39, 40]. It is still not clear why the values measured are higher than the ones reported in the literature and this needs to be further investigated, as lower values of κ would produce higher ZT, meaning that the current ZT values reported in this work could be under estimated.

The results suggest once more, that wide QW tend to deteriorate the value of ZT due to higher values of κ. The higher thermal conductivities compared to the p-type vertical SLs could be related to the higher electrical conductivity values, even though the electrical contribution ($\kappa_{el} = \pi^2 K_B^2 T\sigma/3q^2$) to the thermal conductivity model contributes only between 4.7 and a 4.8% of the total thermal conductivity for SL10 and SL11 respectively.

The two figures of merit for both designs are given in table 7.1, containing the thermoelectric results obtained in each case, and literature values. Both ZT and power factor show values two times higher for SL10 than for SL11, mainly due to the high Seebeck coefficient observed in SL10.

Furthermore, both designs present higher ZT than all Ge and SiGe results reported in the literature. More important are the two power factors obtained in both designs, which exceed the values reported at 300 K for tellurides materials, also shown in table 7.1.

SL with thin QW present high Seebeck coefficients while keeping high electrical conductivities, as well as forcing extra phonon scattering events to impede thermal transport and therefore reduce the value of κ.

Sample ID	N_A cm^{-3}	QW/barrier width (nm)	σ S/m	α $\mu V/K$	κ $W/m \cdot K$	ZT 300 K	PF mW/K^2m
n-Bi_2Te_3 [121]	-	bulk	120,000	-160	1.2	0.768	3.72
n-BiTe/BiTeSe [24]	-	5.0/1.0	81,300	-238	0.945	1.46	4.61
n-Ge [27]	1.1x10^{19}	bulk	123,000	-308	59.9	0.032	11.7
n-$Si_{0.2}Ge_{0.8}$ [14]	2x10^{19}	bulk	28,800	-300	8.9	0.087	2.59
Design 1	1x10^{19}	4.64/1.55	$50,200 \pm 4,200$	-455 ± 9	6.4 ± 0.7	0.49 ± 0.04	10.4 ± 1.0
Design 4	1x10^{19}	12.2/2.3	$55,900 \pm 7,700$	-320 ± 4	8.6 ± 0.5	0.20 ± 0.03	5.7 ± 0.8

Table 7.1: A summary of the thermoelectric properties measured for SL10 and SL11, with the aim to investigate how thin or thick QW widths can produce an impact in the two figures of merit. The values have been compared to bulk n-Ge and bulk n-$Si_{0.2}Ge_{0.8}$ alloys reported in literature with similar doping densities. The table also shows the highest values reported for n-type telluride materials.

7.3.1 The Effect of Temperature

SL10 had a ZT value of 0.49 ± 0.04 and a $\alpha^2\sigma$ value of $10.4 \pm 1.0\,\mathrm{mW/K^2m}$ at 300 K. It thermoelectric properties were further studied at higher temperatures to analyse the temperature dependence of its two figures of merit.

The devices could have been wire-bonded onto chip carriers and introduced inside an environmental chamber to perform the different measurements, as described in Section 5.5 for the lateral devices. However, this solution was not suitable for vertical devices as the ultrasonic force applied by the wire-bonder was enough to damage the multiple bond pads placed on top of the mesa structures, creating short-cuts between top heater, top thermometer and top ohmic contact. Furthermore, CTLMs devices wire-bonded onto chip carriers could have not been used to dry etch the SL and perform measurements at different etch depths.

For this reason, the devices were placed on top of a hot plate and a probe station was used in order to probe the integrated heater, the thermometers and the ohmic contacts. The maximum temperature achievable to perform accurate measurements was 390 K, as above this temperature the probes did not stay static.

Figure 7.8 *a*) shows the value of electrical conductivity measured at three different temperatures. The value of σ decreases by a factor of 0.7 in a range of temperatures of 90 K. Figure 7.8 *b*) shows the linear increase of the Seebeck coefficient as the temperature

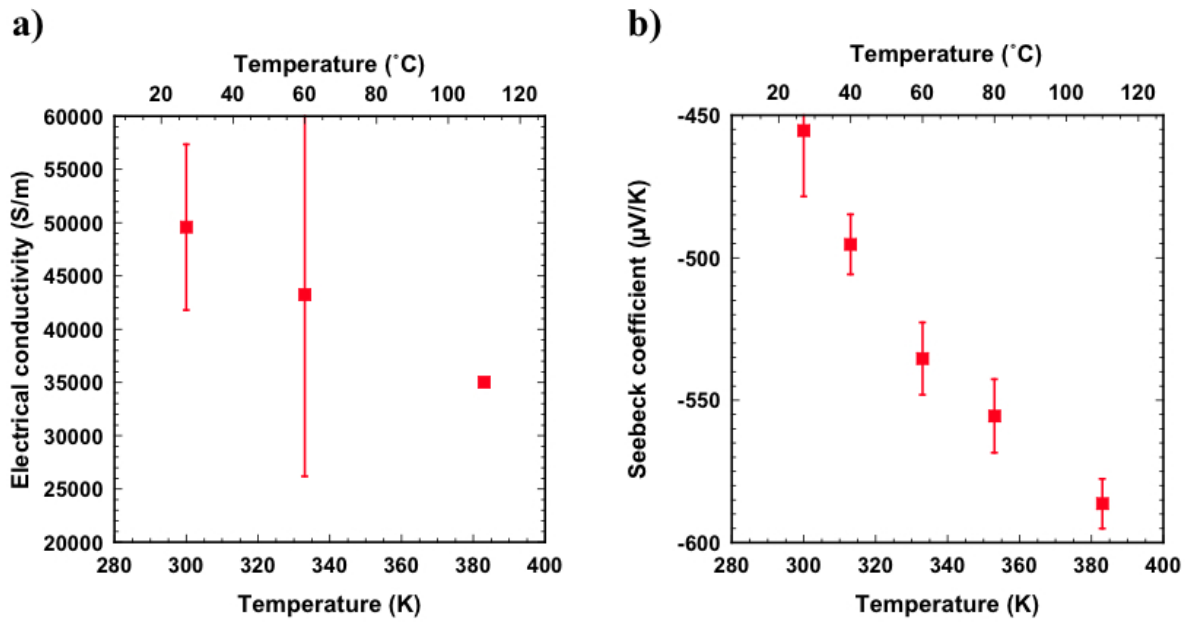

Figure 7.8: The electrical conductivity *a*) and the Seebeck coefficient *b*) for SL10 as a function of temperature.

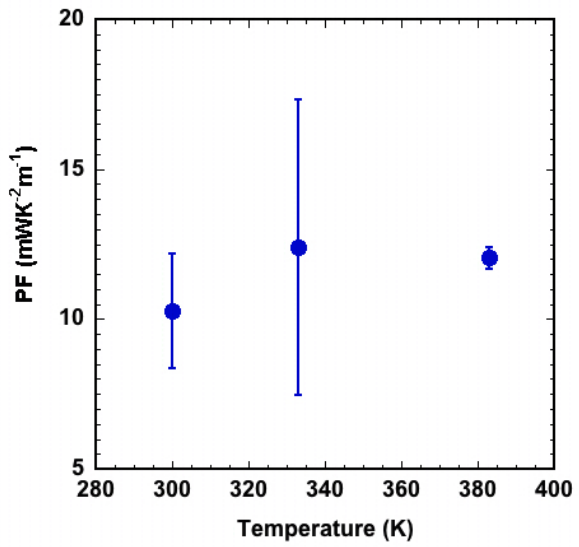

Figure 7.9: The power factor as a function of temperature for SL10.

is increased. This is expected as in all the derivations α is proportional to the temperature, see Equation 1.11 and Equation 1.14.

Figure 7.9, shows the value of $\alpha^2\sigma$ (PF) as a function of three different temperatures. The maximum value achieved for the power factor was $12.4 \pm 0.5\,\mathrm{mW/K^2m}$ at 333 K. There was just a slight increase from room temperature to higher ones because, even if the Seebeck coefficient increased at higher temperatures this improvement was compensated by the decrease in electrical conductivity, resulting in an almost constant value of the power factor.

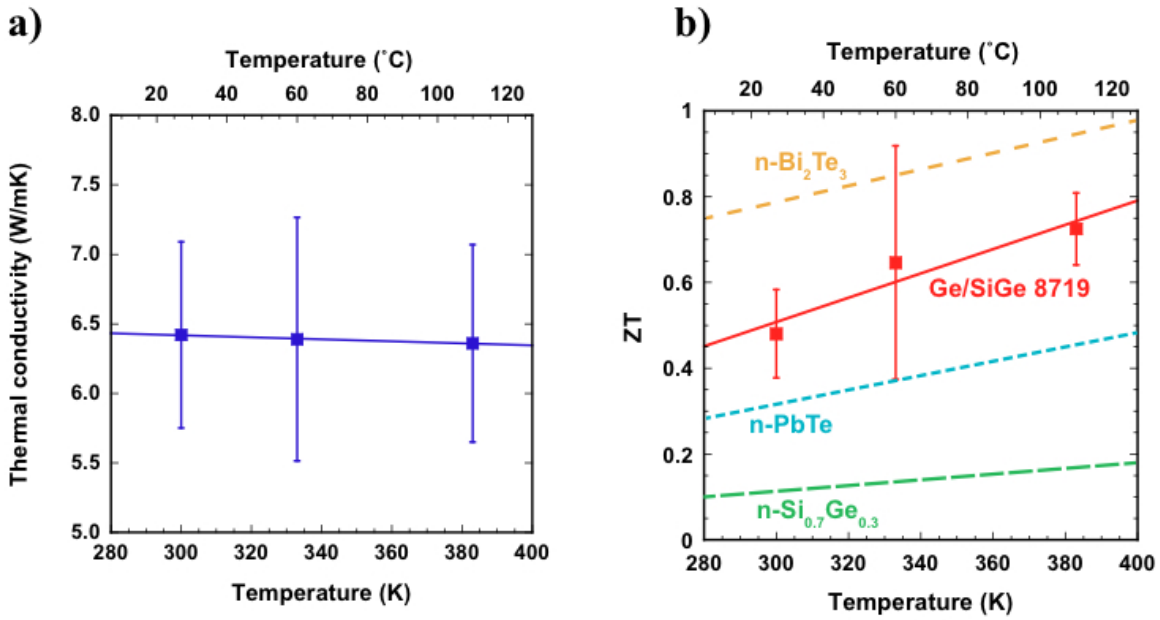

Figure 7.10: *a*) Shows the thermal conductivity as a function of temperature for SL10 and *b*) shows the value of ZT as a function of temperature compared to n-Bi_2Te_3 [12], n-PbTe [13] and n-$Si_{0.7}Ge_{0.3}$ [14].

Figure 7.10 *a*) shows the thermal conductivities extracted for three different temperatures demonstrating a reduction of κ from $6.42\,\mathrm{W/m \cdot K}$ at 300 K to $6.36\,\mathrm{W/m \cdot K}$ at 383 K. *b*) Presents the temperature dependence of SL10 compared to the main thermoelectric materials of Bi_2Te_3, PbTe and bulk SiGe. The value of ZT increases by a factor of 1.5 in a range of temperatures of 90 K.

7.4 Impact of Acoustic Phonon Blocking on κ

Two extra designs (SL12 and SL13) were studied as a complement to SL11 with the aim to investigate whether the thermal conductivity could be further reduced with the addition of barriers with different thicknesses.

Table 7.2 summarizes the thermoelectric values measured for each design, and it can be seen that the thermal conductivity decreased by $2\,\mathrm{W/m \cdot K}$ from SL11 to SL13, also shown in Figure 7.11 *a*). SL13 presented the addition of two extra barriers with different thicknesses to the SL period, suggesting a more efficient material to scatter acoustic phonons. The electronic contribution (also shown in Figure 7.11 *b*)) to the total thermal conductivity was 4.7%, 5.9% and 8.1% for SL11, SL12 and SL13 respectively.

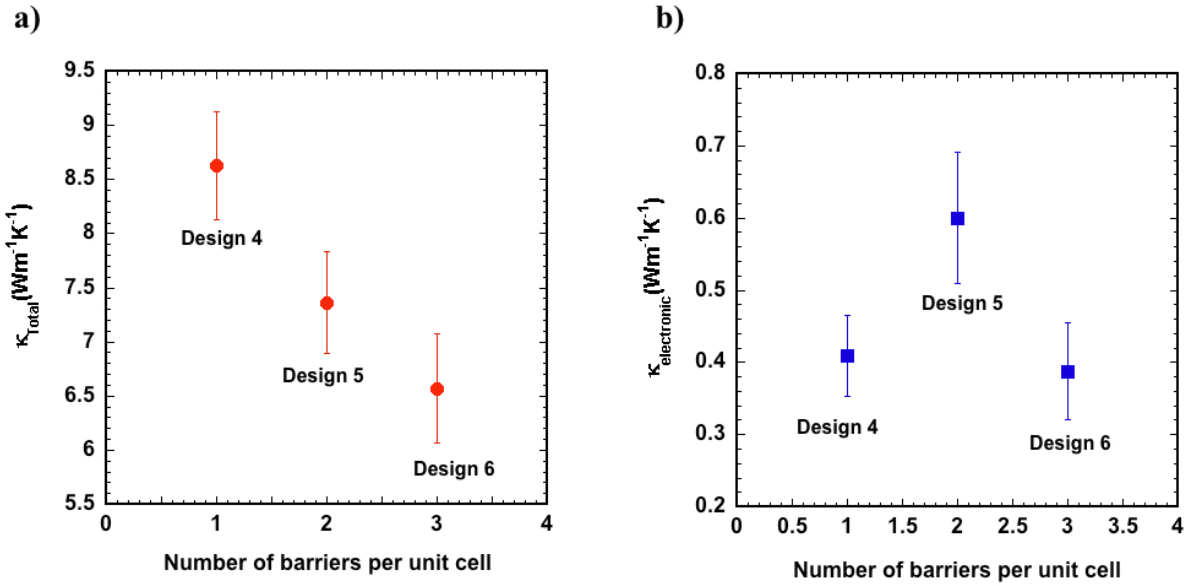

Figure 7.11: *a*) Shows the total value of κ for designs 4, 5 and 6. The thermal conductivity decreases with the addition of barrier per SL period, resulting into a more efficient material to scatter acoustic phonons.*b*) Shows the contribution of the electronic thermal conductivity to the total one, showing a percentage always lower than 8.5%.

The electrical conductivity and the Seebeck coefficient were also measured to check whether the addition of extra layers could deteriorate or improve these two properties. SL12 showed an α value of $-295 \pm 33\,\mu\mathrm{V/K}$, which is comparable to the value reported for SL11 and also for the values reported for n-Ge and n-$Si_{0.2}Ge_{0.8}$, also shown in ta-

ble 7.2. This suggests once more that wide QWs (nominal thickness of 9 nm) limit the enhancement of the Seebeck coefficient as the material seems to have bulk behaviour. The improved α value reported for SL13 of $-403 \pm 3\,\mu$V/K encourages further research. New samples featuring 4 and 5 number of barriers per unit cell should be investigated and compared with the results obtained in this Ph.D to evaluate the correct trend of the Seebeck coefficient.

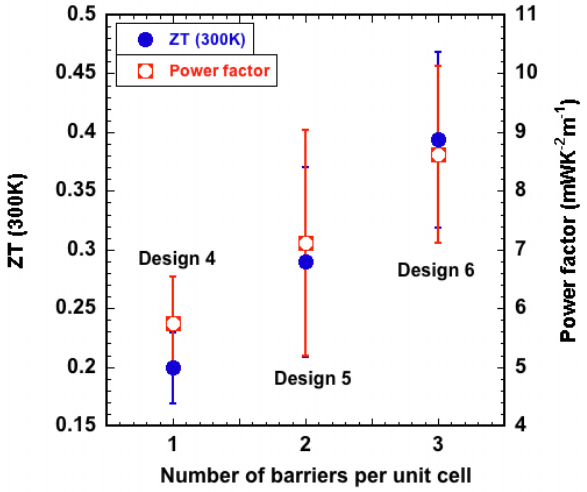

Figure 7.12: The value of ZT and Power Factor for designs 4, 5 and 6 as a function of number of barriers per unit cell. Both figure of merit show an increase with the addition of barriers per SL period.

The values for both figures of merit (ZT and power factor) increase from SL11 to SL13 suggesting that the addition of barriers with different thicknesses inside the period is improving the two figures of merit, as shown in Figure 7.12. This encourages to increase the number of barriers with different thicknesses per period for future designs, to study the impact of this new method on ZT. The results of the current materials studied in this work are approaching to the highest ZT values reported for Te-free materials at room temperature.

Sample ID	N_A cm^{-3}	QW/barrier width (nm)	σ S/m	α $\mu V/K$	κ $W/m \cdot K$	ZT 300 K	PF mW/K^2m
n-Bi_2Te_3 [121]	-	bulk	120,000	-160	1.2	0.768	3.72
n-BiTe/BiTeSe [?]	-	5.0/1.0	81,300	-238	0.945	1.46	4.61
n-Ge [24]	1.1x10^{19}	bulk	123,000	-308	59.9	0.032	11.7
n-$Si_{0.2}Ge_{0.8}$ [14]	2x10^{19}	bulk	28,800	-300	8.9	0.087	2.59
Design 1	1x10^{19}	4.64/1.55	$50,200 \pm 4,200$	-455 ± 9	6.4 ± 0.7	0.49 ± 0.04	10.4 ± 1.0
Design 4	1x10^{19}	12.2/2.3	$55,900 \pm 7,700$	-320 ± 4	8.6 ± 0.5	0.20 ± 0.03	5.7 ± 0.8
Design 5	1x10^{19}	9.3/1.8 9.3/2.6	$82,000 \pm 12,400$	-295 ± 33	7.4 ± 0.5	0.29 ± 0.08	7.1 ± 1.9
Design 6	1x10^{19}	16.7/2.8 16.0/2.0 15.5/1.5	$53,000 \pm 9,200$	-403 ± 3	6.6 ± 0.5	0.39 ± 0.08	8.6 ± 1.5

Table 7.2: A summary of the thermoelectric properties measured for SL11, SL12 and SL13, with the aim to investigate a further reduction of the thermal conductivity by the addition of barriers with different thicknesses to the SL period. The values have been compared to bulk n-Ge and bulk n-$Si_{0.2}Ge_{0.8}$ alloys reported in literature with similar doping densities. The table also presents the highest values reported for n-type telluride materials.

7.5 Conclusions

The cross-plane thermoelectric properties of four n-Ge/$Si_{0.3}Ge_{0.7}$ superlattices with the same doping densities have been studied to perform two different experiments:

- For the first experiment the impact of QW thickness on the ZT and PF was investigated. SL10 featuring a QW nominal width of 3 nm was compared to an identical sample SL11 presenting a QW width of 9 nm.
- For the second experiment the further reduction of the thermal conductivity by adding different barrier thicknesses to the superlattice period was studied. Three samples SL11, SL12 and SL13 featuring 1, 2 and 3 different barrier thicknesses per period were compared as a new approach to scatter phonons more efficiently.

Thin QWs have been shown to present higher Seebeck coefficients and so higher values of ZT and PF. The addition of extra layers in SL10 to reach the same SL thickness as SL11 decreased the value of σ by a 10%, but this slight reduction was compensated by the large increase of α, duplicating the ZT and the PF value for SL10 at 300 K.

SL10 was also tested at higher temperatures and ZT increased by a 35% in a range of 90 K, with a maximum value of 0.75 at 385 K. The PF increased by 17% within the same range, reaching a peak value of 12.4 W/K^2m.

On the other hand, the addition of different barrier thicknesses per period did reduce the thermal conductivity and increase the Seebeck coefficient while keeping an almost constant electrical conductivity. This produced an increase of 50% on ZT and of 40% on the PF from SL11 to SL13.

These results are the highest reported ZTs for a Te-free material.

Comparing the samples studied in this chapter with the p-type samples studied in Chapter 6 (all cross-plane designs), the most interesting result obtained was the abrupt increase of the electrical conductivity by decreasing the Ge content difference between QWs and barriers. Decreasing interface roughness appeared to increase the carrier transport across the superlattice without altering much the lattice contribution to the thermal conductivity. This should be further investigated by testing a set of p-type samples, same designs as SL1, SL2 and SL3 (refer to Chapter 6), but reducing the Ge content difference between barriers and QWs to understand the impact that this fact could produce in the electrical conductivity.

Chapter 8

Conclusions and Future Work

In this work the cross-plane and in-plane properties of Ge/Si_xGe_{1-x} superlattices have been studied in order to maximize the efficiency of single p- and n- legs aiming for improved efficiencies of future thermoelectric modules.

All the different designs were modelled by Prof. Douglas Paul with the aim of enhancing the electrical and thermal conductivities, and the Seebeck coefficients either along or across the superlattices. The superlattices were grown by using a LEPECVD tool at Politecnico di Milano and XRD and TEM physical characterisation were provided by Universitaet Linz and ETH in Zurich, respectively. The work achieved within this thesis is reported next:

- The development of micro-fabricated structures which allowed the characterisation of most of the thermoelectric properties in one single device so that accurate values of ZT and PF could be reported.
- The development of characterisation techniques to evaluate experimentally the heat flux flowing inside the structures, so that thermal properties of the superlattices could be estimated.
- The development of characterisation techniques to evaluate the cross-plane electrical properties of 4 μm thick superlattices.
- The complete thermoelectric characterisation and analysis of Ge-rich superlattices including modulation doped and uniformly doped multi-quantum wells at room

temperature. This involved the separate study of the two thermoelectric figures of merit as a function of QW width, Ge content and doping density.

- A first study of superlattices, including different barrier thicknesses per period, with the aim of scattering phonons with different wavelengths and so decreasing further the thermal conductivity. The analysis of the electrical properties was also studied in these superlattices to evaluate the impact that this new method could produce in the electrical conductivity and Seebeck coefficient.

All the fabrication processes involved in this work were compatible with MEMs and CMOS technology, with the aim of using most of these processes to produce and integrate future modules in industrial foundries. Most of MEMs foundries already have all the tools used to fabricate the devices developed during this work and therefore to produce thermoelectric modules featuring some of the optimized processes used to characterize the material, such as dry etching recipes and optimised ohmic contacts.

Next the main results and limitations presented within the course of this thesis are summarised, and suggestions for future work are indicated at the end of this chapter.

8.1 Lateral Designs

Electrical and thermal properties in the in-plane direction for modulation doped superlattices were studied as a function of QW width for two different designs with different Ge content.

6-contact Hall-bars with integrated heaters and thermometers where fabricated to obtain electrical and thermal characterisation in one single device, allowing an accurate estimation of ZT and PF.

A differential technique, where the absolute temperature of the thermometers was measured before and after etching the central part of the Hall-bar, was developed to estimate the exact heat flux flowing inside the structure. Knowing the effective heat flux, an accurate estimation of the thermal conductivity was found, which was cross checked with finite element analysis and with scanning thermal AFM probes.

Although the values achieved for ZT were very modest, obtaining a maximum value of 0.08, they were all higher than ZT values reported for a reference SiGe alloy (also characterized within this Ph.D) and than literature values for p-Ge. The enhancement of ZT was limited mainly by the high thermal conductivity, which increased for samples with higher electrical conductivities and for the Seebeck coefficient, which was comparable to the SiGe reference alloy. Nevertheless, PF values as high as $6\,\mathrm{mW/K^2m}$ were measured, which is double the values reported in the literature for p-Si and p-Ge and a factor of 4 times the values reported for the reference SiGe alloy with comparable doping densities. The enhancement of the PF was mainly produced by the high electrical conductivity values measured due to the presence of δ-doping.

Mobility spectra analysis performed by Danny Chrastina [10] demonstrated a parallel conduction of carriers inside the barriers for a set of identical samples. These results suggested that the electrical and the thermal conductivities of the present superlattices could be limited by the conduction contribution of a second low-mobility channel.

After analysing all the results, three key-points were identified to further optimise ZT and PF. These key-points are described next:

- A reduction of doping density for future modulation doped superlattices, with the aim of confining most of the carriers inside the high-mobility channels (QW). Pre-

venting the conduction of carriers inside the barriers would increase the mobility and this may enhance both ZT and PF.

- A reduction of QW thicknesses to promote quantum effects and increase the Seebeck coefficient measured. The present QW widths seemed to be too wide and so carriers were behaving as in 3D systems, limiting the enhancement of α.

- A reduction of the TDD by a factor of 100. Theoretical analysis suggested that lower TDD would significantly increase the value of ZT [11]. In fact, Figure 5.25 demonstrated the good agreement between the experimental results obtained within this work and the ZT theoretically calculated by [11] for a TDD of $10^9\,\mathrm{cm}^{-2}$.

8.2 Vertical Designs

Electrical and thermal properties in the cross-plane direction of uniformly doped p and n-Ge/$Si_{1-x}Ge_x$ superlattices were studied from three different aspects: the understanding of the impact of doping density on the two figures of merit, the understanding of the impact of QW width on the two figures of merit and the demonstration of further phonon scattering with different phonon wavelengths.

Two different devices were designed and micro-fabricated to characterise the material. A modified CTLM was used to estimate the electrical conductivity, which involved the optimisation of ohmic contacts in both p and n superlattices in order to perform the measurements. For the estimation of the Seebeck coefficient and the thermal conductivity, devices with an etched mesa of the superlattice and with integrated heaters, thermometers and electrical top and bottom contacts were used. A differential technique was performed to calculate the heat lost through the multiple parasitic channels affecting the thermal measurements. Knowing the exact heat flux flowing through the superlattice allowed the calculation of the thermal conductivity. This new method was used to evaluate the cross-plane thermal conductivity of a SiO_2 thin layer, obtaining a κ that was in 82% agreement with values reported in the literature.

Uniformly doped p-Ge/$Si_{0.5}Ge_{0.5}$ superlattices were studied as a function of doping density, showing a maximum ZT of 0.08 and a PF of $1.34\,\mathrm{mW/K^2m}$ for a measured doping density of $2.0\text{x}10^{18}\,\mathrm{cm}^{-3}$. The enhancement of the Seebeck coefficient showed values well above the ones reported in the literature for p-Ge and p-SiGe alloys with comparable

doping densities. The thermal conductivity showed values between 4.5 and 6.0 $\mathrm{W/m \cdot K}$, showing cross-plane values that were 5 times smaller than the in-plane values measured in previous samples. However, even if the thermal conductivity experienced a sharp decrease, the values measured were still double the reported κ for Si/Ge superlattices in the literature. It is still not clear why larger values of κ were obtained, and this should be further investigated as the thermal conductivities could be over-estimated producing an under-estimation of the ZT values reported in this thesis. Although cross-plane properties experienced an improvement for α and κ, the weak-point for these designs was clearly the electrical conductivity, limiting the value of ZT and PF. This was explained due to the presence of high interface roughness caused by the high Ge content difference between QWs and barriers. In SiGe superlattices it was demonstrated that interface roughness increases with strain which in turn increases with Ge content difference [119]. This issue could be dominating the carrier scattering resulting into low electrical conductivities.

This effect was then studied by a set of uniformly doped n-Ge/$Si_{0.3}Ge_{0.7}$ superlattices in which the electrical conductivity increased by at least a factor of 5. This abrupt enhancement of σ still needs to be further investigated to assure that interface roughness is in fact the key-parameter to improve carrier conduction across superlattices. A second set of p-type superlattices, identical to the ones already studied but with lower Ge content difference between layers, should be grown and electrically tested to be able to compare the electrical conductivities and corroborate the importance of interface roughness between QWs and barriers. Seebeck coefficients had an enhancement above values reported in the literature for n-Ge and n-SiGe alloys, resulting into higher Seebeck coefficients for samples with thinner QWs. The thermal conductivities were between 6.4 and 8.6 $\mathrm{W/m \cdot K}$, values slightly larger than the ones reported for p-type superlattices, which could be explained by the sharp increase of the electrical conductivity. Superlattices with thinner QWs presented the highest values of ZT and PF of 0.49 and 10.4 $\mathrm{mW/K^2m}$, respectively.

On the other hand, the understanding of phonon propagation was studied by the addition of barriers with different thicknesses per period with the aim of scattering phonons with different wavelengths. The thermal conductivity was reduced by this addition, producing a more effective way of scattering phonons. The electrical conductivity did not seem to be affected by the addition and the Seebeck coefficient was increased by increasing the number of barriers. This new method to reduce the thermal conductivity became very interesting as not only did the electrical properties not deteriorate but they were

improved, producing higher values of ZT and PF.

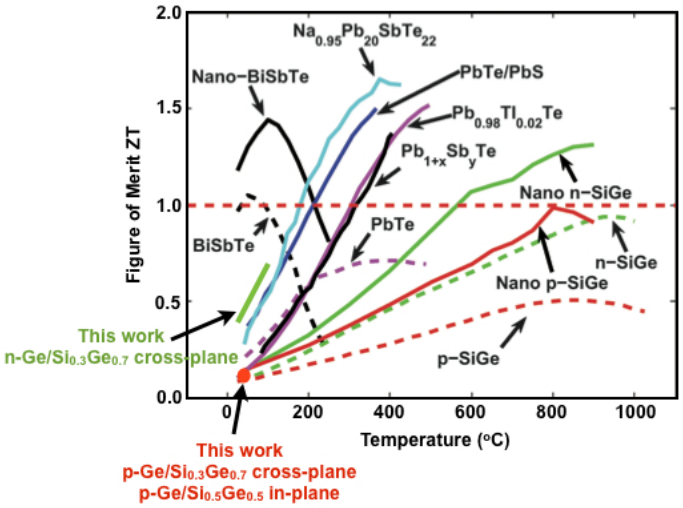

Figure 8.1: ZT values reported in the literature plotted as a function of temperature [15], where the results obtained in the course of this Ph.D have been plotted for comparison. The dashed lines correspond to the ZT values for bulk materials while the solid lines show the recent ZT values reported reported in the literature.

The ZT values reported for the n-type superlattices showed the highest values obtained for SiGe and for free-Te materials between 300 K and 390 K. In fact, the results are potentially competitive with current n-type telluride materials. Figure 8.1 shows the ZT value as a function of temperature for different thermoelectric materials reported in the literature, the values obtained in this work are also shown in the plot for comparison.

Figure 8.2 *a*) shows the PF values reported in the literature for the thermoelectric materials that presented some of the highest ZT. Figure 8.2 *b*) demonstrates the same literature values presented in *a*), compared to the highest PF obtained in the course of this work.

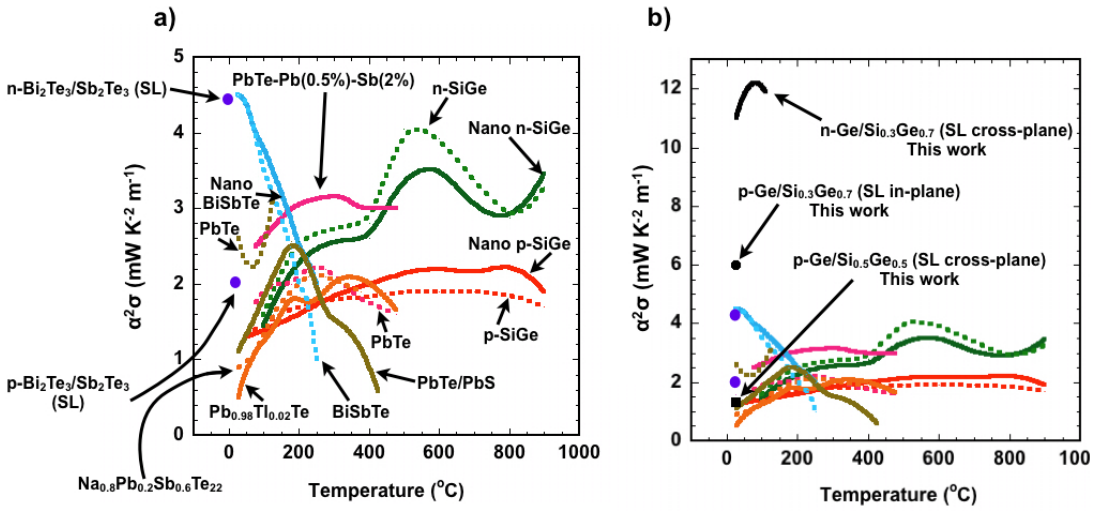

Figure 8.2: *a*) Shows the PF values reported in the literature plotted as a function of temperature and *b*) compares the data collected in *a*) with the highest PF values obtained in this work. The dashed lines correspond to the PF values for bulk materials while the solid lines show the recent PF values reported in the literature for the current thermoelectric materials presenting the highest ZT, many of them obtained in nanostructured materials. (BiSbTe [16]; $Na_{0.95}Pb_{20}SbTe_{22}$ [17]; PbTe/PbS [18, 19]; $Pb_{0.98}Tl_{0.02}Te$ [20]; $Pb_{1+x}Sb_yTe$ [21]; n-SiGe [22]; p-SiGe [23]; n- and p- Bi_2Te_3/Sb_2Te_3 [24]

8.3 Future Work

The ZT values reported for n-type vertical designs, which are comparable to the current highest ZT reported at room temperature, suggested two main points for the natural progression of the current work:

- Firstly, interface roughness was identified as a key-point limiting carrier conduction across the superlattice and therefore resulting into low electrical conductivities. Even though n-type vertical designs showed promising ZT values, new p-type designs with less Ge content difference between the barriers and QWs should be addressed to confirm that interface roughness is the main phenomena dominating carrier scattering.

- Secondly, the improvement of ZT and PF for superlattices with multiple number of barriers per period with different thicknesses, encourage for further extension of the

number of barriers. The addition of even more barriers together with thinner QW could cause a big impact in the two thermoelectric figure of merit and should be investigated.

As shown in Figure 1.4, Si and Ge materials showed improved performances at higher temperatures. In this work some structures were tested up to 390 K, this being the maximum temperature achievable for the present set up and showing n-type ZT as high as 0.7. Further measurements should be taken up to 613 K, this being the maximum temperature that would assure good ohmic contacts and therefore working devices, to investigate the impact of ZT and PF for the present superlattices.

This work focused on 2D superlattices but as demonstrated in the literature 1D nanowires could substantially enhance the two thermoelectric figures of merit. Ge/SiGe superlattices have demonstrated to present low thermal conductivities and higher Seebeck coefficients and electrical conductivities, compared to their alloy counterparts. Moving from 2D to 1D by creating etched nanowires in the current superlattices could reduce much further the thermal conductivity and therefore create a big impact on ZT. Ultimately, the technology used in this work could be used to create testing devices with lateral or vertical nanowires on the deposited superlattices in order to evaluate the efficiency of these structures.

The development of this work, focused on the optimization of p and n-type superlattices, with the aim of creating optimised generators that could work as an energy harvester with an output power of 3 mW. In order to see if this is achievable, p and n-type legs should be integrated into a module and tested. The design should be optimised with the balanced cross section area for each leg and with the lowest impedance mismatch between the legs and the bumps created for flip-chip-boning.

In the long term, these modules should be scalable in order to integrate them inside the fabrication process of CMOS sensors to create a complete autonomous system, where no battery or wiring would be necessary to power a wireless sensor.

Appendix A

Device development for Thermal Vertical Characteriztion

The previous work undertaken to design the device shown in Chapter 6 is presented in this appendix.

The appendix starts with the description of one of the first devices fabricated and characterised to extract the cross-plane values of α and κ on 4 μm thick superlattices.

The thermal characterisation is followed by finite element analysis undertaken in an identical device. The conclusions extracted from this analysis and modelling encouraged to design further devices, which are presented at the end of this appendix.

A.1 Thermal Analysis on Vertical Devices

In order to extract the Seebeck coefficient and the thermal conductivity values perpendicular to the superlattice a mesa structure with integrated heaters, thermometers and ohmic contacts was required. Figures A.1 and A.2 show different images of two different devices fabricated following two different approaches which are explained next:

- Figure A.1 consisted in an etched mesa with two Ni voltage pads placed at the top of the structure and surrounded by a Ti/Pd heater. The four terminal top heater was used as well as a top thermometer, with the aim of simplifying the fabrication process and the thermal analysis by reducing the number of layers. At the bottom of the mesa, a second Ti/Pd thermometer and a Ni voltage pad were

patterned so that the Seebeck voltage and the ΔT between the top and the bottom of the superlattices could be measured. The bond pads and interconnects to the top heater/thermometer were patterned by lift-off using 300 nm of Al so that most of the heat could be concentrated at the Ti/Pd resistor presenting a higher resistance. Placing the Ni voltage pads in between the top heater was done to spread the heat along the top of the mesa structure and therefore creating a uniform in-plane temperature flowing perpendicular to the SL.

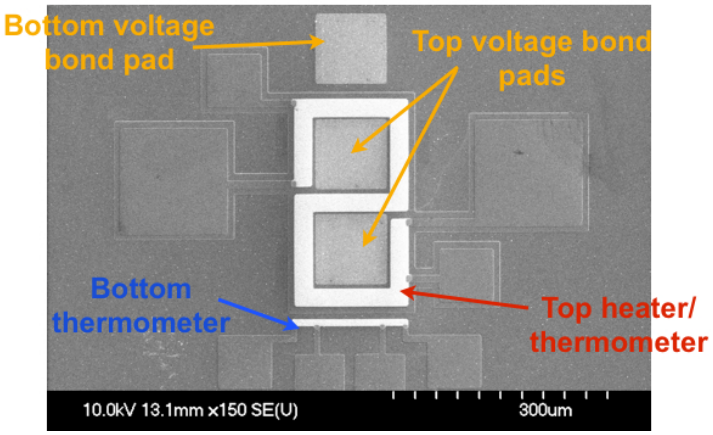

Figure A.1: SEM image of a mesa structure device with a four terminal top heater surrounding two Ni top voltage pads. The image also shows an integrated thermometer and a Ni voltage pad at the bottom of the mesa.

- Figure A.2 *a*) shows a second device which followed another approach. A mesa with a surface area two times smaller than the surface area from the previous device was patterned by a mixed ICP etch recipe. The top of the mesa structure was covered by a Ti/Pd 'serpentine' heater, which was also used as a top thermometer, consisting of 10 μm wide metal lines spaced by other 10 μm gaps. In between the metal lines, small windows were opened to etch the silicon nitride layer that was isolating the heater from the semiconductor with the subsequent metal deposition of Ni to create the ohmic contacts, see Figure A.2 *b*). The four terminal pads of the top heater/thermometer were patterned on top of the 'serpentine' resistor. At the bottom of the mesa, a Ti/Pd thermometer and Ni ohmic contacts were created to measure the Seebeck voltage and the ΔT.

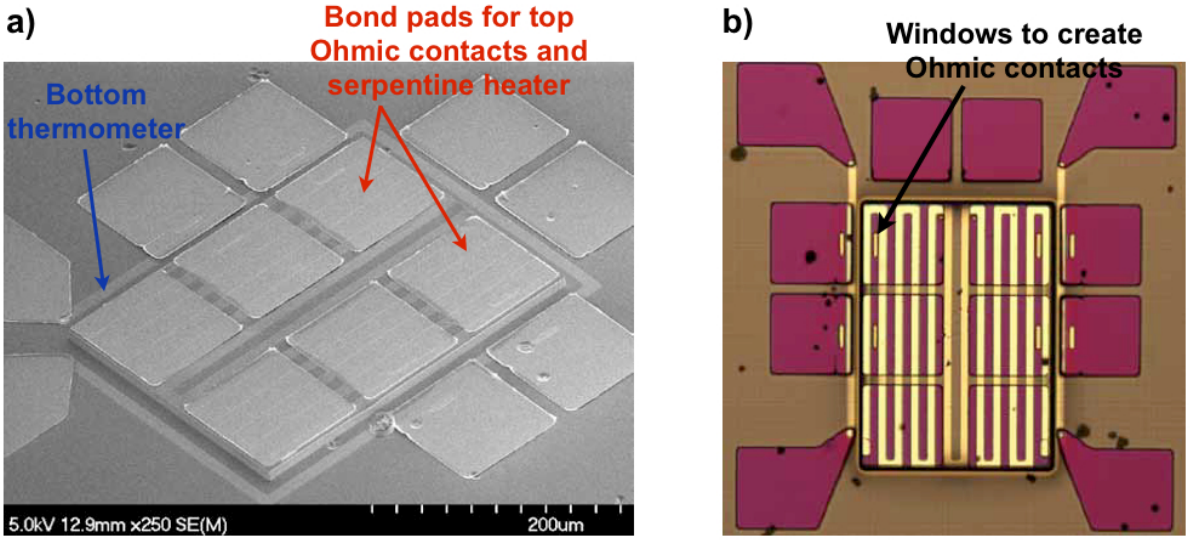

Figure A.2: *a*) Shows an SEM image of a second device with a 'serpentine' heater which covers the full top surface of the mesa structure. The bond pads in order to probe the top heater/thermometer and ohmic contacts were patterned on top of the metal 'serpentine'. The bottom of this device also integrated thermometers and ohmic contacts. *b*) Optical top image of the device presented in Figure A.1 *b*) where the bond pads for the thermometers and the ohmic contacts were patterned previous to metal deposition.

Following it is described most of the thermal characterisation and analysis undertaken on the first device presented in Figure A.1.

A.2 Physical Characterisation

Before undertaking any measurement both thermometers (top and bottom) were calibrated following the technique introduced in Section 4.2.1. The TCR obtained for the Ti/Pd thermometers was of $0.0020536\,\mathrm{K}^{-1}$ with a standard deviation lower than 3%. After performing the calibration, a power ramping from 0 W to 1.2 W was applied to the top heater while the change of resistance of the top and bottom thermometers was monitorized by a set of lock-in amplifiers.

Figure A.3 *a*) shows the temperature profile for both thermometers as a function of power heater. As the plot demonstrates, using the top heater as a thermometer resulted into a spurious region at low powers where the bottom thermometer was heated up quicker

than the top one creating a negative ΔT. This approach introduced a larger error on ΔT and it under-estimated the temperature difference between the top and the bottom of the SL as it was demonstrated later by ThAFM scans (technique explained in Section 4.2.2).

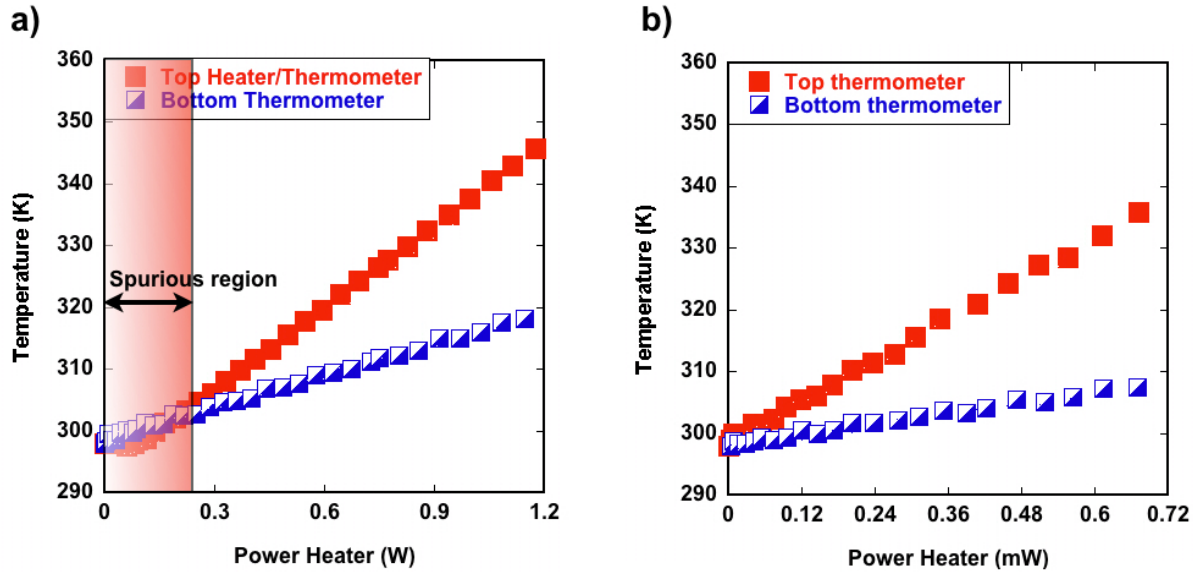

Figure A.3: *a*) Shows the temperature profile of both thermometers, top and bottom, where the top thermometer was also used as a heater. *b*) Shows the temperature profile of both thermometers, where the top thermometer was separated from the heater.

This spurious region was created by the incompatibility between the measurement and the calibration technique. For the calibration, a low constant current was driven through the thermometer while the temperature on this one was increased. The change of resistance was induced due to the change of voltage at the thermometer which was always driven by a constant current. On the contrary, in order to increase the temperature during the measurement, the heater was driven at different voltages and therefore at different currents, creating Joule heating and as a consequence creating a change of the thermometer resistance. As a conclusion, one could say that the measurement and the calibration were not done under the same conditions and hence the error produced by the ΔT measured.

Figure A.3 *b*) shows an identical measurement as the one undertaken in *a*), but in this case the top heater and top thermometer had been patterned separately not revealing any spurious region.

Thermal AFM scans were performed on the different devices to cross-check the ΔT measured by the resistive thermometers. A constant power of 240 mW was applied to the heater while the ThAFM probe scanned the temperature at the top and bottom of the device. The ΔT measured by both techniques agreed within a 96%, value that was sharply reduced when the top heater was also used as the top thermometer. Figure A.4 *a*) shows the part of the device that was scanned to measure the temperature difference between the top and the bottom thermometer. *b*) Shows a topographic image of the scan performed and *c*) shows the temperature profile sensed by the ThAFM probe.

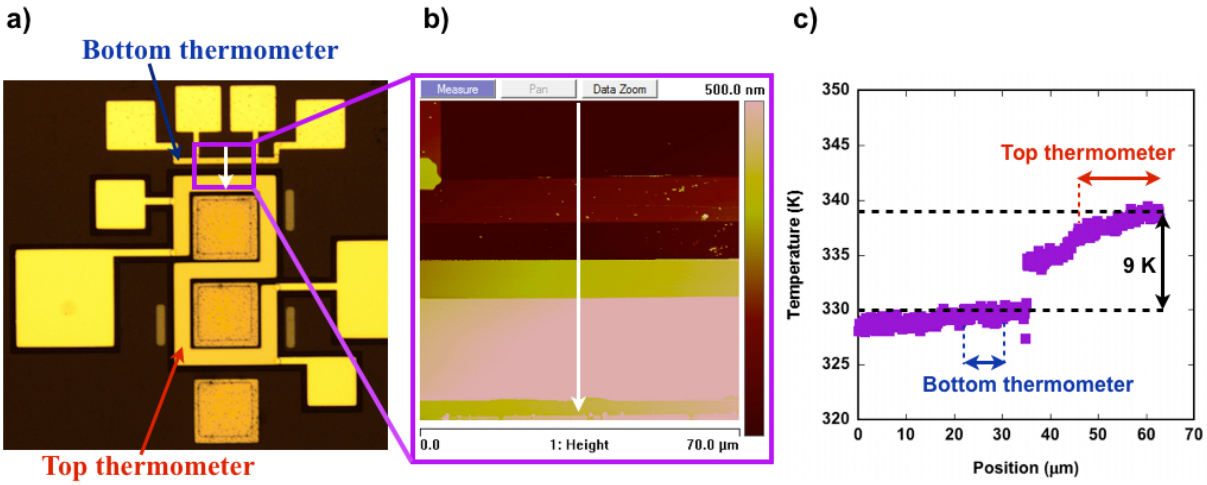

Figure A.4: *a*) An optical picture of the device measured, where the heater was separated from the top thermometer. *b*) Topographical image of the area scanned by the ThAFM probe. *c*) The temperature profile as a function of the position, the direction has been indicated in *a*) and *b*) by a white arrow.

Despite of the good agreement between ThAFM scans and the resistive thermometry technique, the Seebeck voltage measured as a function of ΔT resulted into values 4.2 times smaller than bulk Ge, suggesting that the temperature measured by the thermometers was not the same as the temperature of the voltage pads.

Finite element analysis was undertaken to model the temperature profile along the top and bottom of the device. Figure A.5 *a*) shows the image of the solution and *b*) shows the temperature profile at the top and bottom of the device as a function of position, indicated in *a*) by a white arrow. As it is shown in *b*) the difference of temperature was

only created just underneath the heater, leaving the voltage pads placed at the top of the SL at the same temperature as the bottom of the SL.

This temperature profile could explain the low Seebeck coefficient values produced, as the ΔT used for the analysis was completely different to the temperature difference at the Seebeck voltage pads.

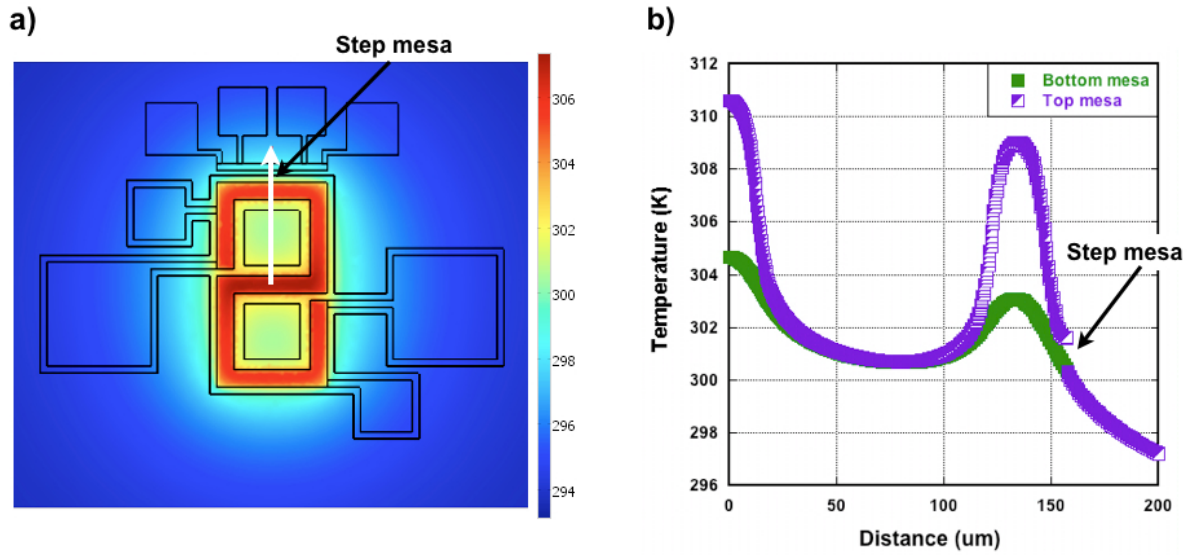

Figure A.5: *a*) Shows the solution of the simulation. *b*) The temperature profile at the top and the bottom of the SL. The ΔT is only created just underneath the heater resistor, while the voltage pads were at the same temperature as the bottom of the SL.

Finite element analysis was done to simulate the temperature at the top and bottom of the superlattice by using a 'serpentine' heater, as the one showed in Figure A.2. Figure A.6 *b*) shows the solution of the simulation.

The heater consisted in 10 μm wide metal lines separated by 10 μm gap spacings but, these gaps were still too wide to spread the heat along the plane, creating a non-uniform ΔT across the SL.

A final analysis using a square heater was done to simulate the temperature profile at the top and bottom of the SL. This last analysis, presented in Chapter 7, showed a uniform heat distributed along the plane and therefore a uniform ΔT across the SL.

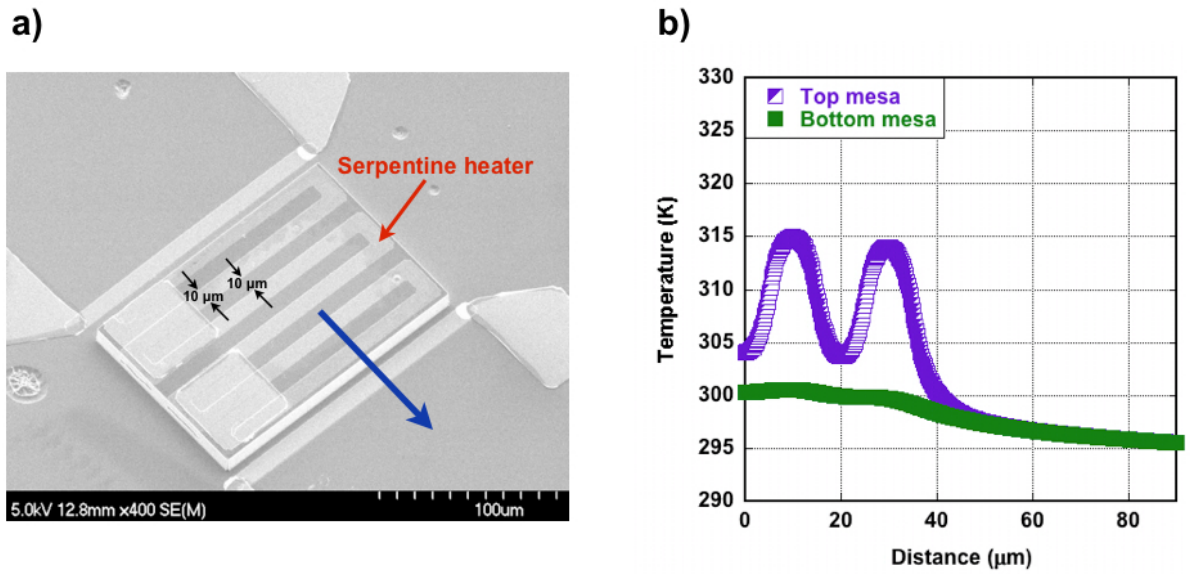

Figure A.6: *a*) Shows an SEM image of a device with a 'serpentine' heater, which consisted of 10 μm metal lines separated by 10 μm gaps. The gaps are too wide to create a uniform heat distribution along the plane which generates a non uniform ΔT across the SL, as can be seen in *b*). *b*) Shows the temperature profile of the top and bottom of the SL as a function of position solved by finite element analysis of the identical device. The position is indicated in *a*) by a blue arrow.

A.2.1 Conclusions

A device had to be developed to thermally characterise the cross-plane properties of 4 μm thick superlattices. This meant that integrated heaters, thermometers and ohmic contacts had to be integrated within the device to create heat and measure the temperature and the Seebeck voltage. A first approach consisted in integrating all these structures one next to each other, designing a heater that could be able to spread the heat along the surface area of the device. The different configurations studied in this work showed poor values of α due to the non-uniformity of ΔT across the SL. The simulations agreed with the results analysed and suggested that a square heater was the best geometry to produce a uniform heat along the plane. This analysis highlighted the necessity of patterning heaters, thermometers and ohmic contacts, on top and aligned to each other. ThAFM scans and resistive thermometry measurements also demonstrated that using heaters as thermometers would simplify the fabrication but would produce big errors on ΔT.

Bibliography

[1] G. J. Snyder and E. S. Toberer. Complex thermoelectric materials. *Nature Materials 7*, 2008.

[2] D. Paul. Project periodic report green silicon: First year. *Green Silicon: Project No. 257750*, 2011.

[3] S. M. Sze. *Semicondcutor devices: physics and technology.* Hoboken, N.J.: Wiley, 1936.

[4] E. Kasper and D. J. Paul. *Silicon Quantum Integrated Circuits.* Springer, 2005.

[5] D. J. Paul. Si/SiGe heterostructures: from material and physics to devices and circuits. *Semiconductor Science and Technology 19, R75-R108*, 2004.

[6] Dieter K. Schroder. *Semicondcutor Material and Device Characterization.* A. John Wiley and Sons, 2006.

[7] Stefano Carlo Cecchi. *Deposition and Characterization of Silicon-Germanium Heterostructures for Thermoelectric Devices.* PhD thesis, Politecnico di Milano, 2013.

[8] S. Cecchi *et al.* Ge/SiGe superlattices for thermoelectric devices grown by low-energy plasma-enhanced chemical vapor deposition. *Journal of Electronic Materials 42, 7*, 2013.

[9] A. Samarelli *et al.* The thermoelectric properties of Ge/SiGe modulation doped superlattices. *Journal of Applied Physics 113, 233704*, 2013.

[10] D. Chrastina *et al.* Ge/SiGe superlattices for nanostructured thermoelectric modules. *Thin Solid Films 543, 153-156*, 2013.

[11] J. R. Watling and D. J. Paul. A study of the impact of dislocations on the thermoelectric properties of quantum wells in the si/sige materials system. *Journal of Applied Physics 110, 114508*, 2011.

[12] *Thermoelectrics and its Energy Harvesting: Materials, Preparation, and Characterization*. CRC Press, Taylor and Francis, 2012.

[13] R. W. Fritts. *Thermoelectric Materials and Devices*. ed. by Cadoff and E. Miller (Reinhold, New York, pp. 143-162), 1960.

[14] J. P. Dismukes et al. Thermal and electrical properties of heavily doped Ge-Si alloys up to 1300 k. *Journal of Applied Physics 35, 10*, 1964.

[15] A. J. Minnich *et al.* Bulk nanostructured thermoelectric materials: current research and future prospects. *Energy Environmental Science 2, 466-479*, 2009.

[16] B. Poudel *et al.* High-thermoelectric performance of nanostructured bismuth antimony telluride bulk alloys. *Science 320, 634*, 2008.

[17] P. F. P. Poudeu *et al.* High thermoelectric figure of merit and nanostructuring in bulk p-type $Na_{1-x}Pb_mSb_yTe_{m+2}$. *Angewandte Chemie International Edition 45, 3835-3839*, 2006.

[18] J. Androulakis *et al.* Spinodal decomposition and nucleation and growth as a means to bulk nanostructured thermoelectrics: Enhanced performance in $pb_{1-x}sn_x$te-pbs. *Journal of the American Chemical Society 129, 9780-9788*, 2007.

[19] J. Heremans *et al.* Thermopower enhnacement in lead telluride nanostructures. *The American Physical Society*, 2004.

[20] J. P. Heremans *et al.* Enhancement of thermoelectric efficiency in PbTe by distortion of the electronic density of states. *Science 321, 554*, 2008.

[21] J. Sootsman *et al.* Large enhancement in the thermoelectric power factor of bulk PbTe at high temperature by synergistic nanostructuring. *Angewandte Chemie International Edition 47, 8618-8622*, 2008.

[22] X. W. Wang *et al.* Enhanced thermoelectric figure of merit in nanostructured n-type silicon germanium bulk alloy. *Applied Physics Letters 93, 193121*, 2008.

[23] Giri Joshi *et al.* Enhanced thermoelectric figure-of-merit in nanostructue p-type silicon germanium bulk alloys. *Nano Letters 8, 12*, 2008.

[24] R. Venkatasubramaniam *et al.* Thin-film thermoelectric devices with high room-temperature figures of merit. *Nature 413*, 2001.

[25] P. Harrop. The hot applications for energy harvesting. *Energy Harvesting Journal, http://www.energyharvestingjournal.com/articles/the-hot-applications-for-energy-harvesting-00001247.asp*, 2009.

[26] H. Bottner *et al.* New high density micro structure thermogenerators for stand alone sensor systmes. *Int. Conference Proc. Thermoelectrics*, 2007.

[27] D. M. Rowe. *Thermoelectrics Handbook: Macro to Nano.* CRC Taylor and Francis, 2006.

[28] H. J. Goldsmid. *Introduction to Thermoelectricity.* Springer−Verlag Berlin Heidelberg, 2010.

[29] C. Watkins *et al.* Low-grade-heat energy harvesting using superlattice thermoelectrics for applications in implantable medical devices and sensors. *Proc. Int. Conference on Thermoelectrics*, 2005.

[30] H. Bottner. Miniaturised thermoelectric devices: Small size, high cooling power densities, short response time. *Int. Conference Proc. Thermoelectrics*, 2005.

[31] H. Bottner *et al.* New thermoelectric components using microsystem technologies. *Journal of Microelectromechanical Systems 13, 3*, 2004.

[32] S. M. Sze. *Physics of Semiconductor Devices.* John Wiley and Sons, New York, 1981.

[33] A. Amith. Seebeck coefficiente in n-type germanium-silicon alloys: "competition" region. *Physical Review 139, 5A*, 1965.

[34] W. L. C. Hui and J. P. Corra. Seebeck coefficient of thin-film germanium. *Journal of Applied Physics 38, 9*, 1967.

[35] L. D. Hicks and M. S. Dresselhaus. Effect of quantum-well structures on the thermoelectric figure of merit. *Physical Review B 47, 19*, 1993.

[36] M. S. Dresselhaus *et al.* Low-dimensional thermoelectric materials. *Physics of the Solid State 41, 5*, 1999.

[37] M. P. Singh and C. M. Bhandari. Thermoelectric properties of bismuth telluride quantum wires. *Solid State Communications 127, 649-654*, 2003.

[38] R. Venkatasubramaniam. Lattice thermal conductivity reduction and phonon localizationlike behavior in superlattice structures. *Physical Review B 61, 4*, 2000.

[39] B. Yang *et al.* Measurements of anisotropic thermoelectric properties in superlattices. *Applied Physics Letters 81, 19*, 2002.

[40] W. L. Liu *et al.* Anisotropic thermal conductivity of Ge quantum-dot and symmetrically strained si/ge superlattices. *Journal of Nanoscience and Nanotechnology 1, 1*, 2001.

[41] T. Borca-Tasciuc *et al.* Thermal conductivity of symmetrically strained Si/Ge superlattices. *Superlattices and Microstructures 28, 3*, 2000.

[42] S. M. Lee *et al.* Themal conductivity of Si-Ge superlattices. *Applied Physics Letters 70, 22*, 1997.

[43] B. Yang *et al.* Simultaneous measurements of seebeck coefficient and thermal conductivity across superlattice. *Applied Physics Letters 80, 10*, 2002.

[44] J. A. Martinez *et al.* Enhanced thermoelectric figure of merit in SiGe alloy nanowires by boundary and hole-phonon scattering. *Journal of Applied Physics 110, 074317*, 2011.

[45] A. I. Boukai *et al.* Silicon nanowires as efficient thermoelectric materials. *Nature 451*, 2008.

[46] G. W. C. Kayne and T. H. Laby. *Table of Physical and Chemical Constants*. 16th ed. Longman, 1995.

[47] A. I. Boukai *et al.* Silicon nanowires as highly efficient thermoelectric materials-supplementary information (experiment). *Nature 06458/doi:10.1038*, 2008.

[48] H. Beyer *et al.* PbTe based superlattice structure with high thermoelectric efficiency. *Applied Physics Letters 80, 7*, 2002.

[49] B. Yang *et al.* Characterisation of cross-plane thermoelectric properties of Si/Ge superlattices. *Proc. Int. Conference on Thermoelectrics*, 2001.

[50] L. D. Hicks *et al.* Experimental study of the effect of quantum-well structures on the thermoelectric figure of merit. *Physical Review B 53,16*, 1996.

[51] M. S. Dres *et al.* New directions for low-dimensional thermoelectric materials. *Advanced Materials 19, 1043-1053*, 2009.

[52] J. M. O. Zide *et al.* Demonstration of electron filtering to increase the seebeck coefficient in $In_{0.53}Ga_{0.47}As/In_{0.53}Ga_{0.28}Al_{0.19}As$ superlattices. *Physical Review B 74, 205335*, 2006.

[53] X. Sun *et al.* Experimental study of the effect of the quantum well structures on the thermoelectric figure of merit in $si/si_{1-x}ge_x$ system. *18th Internation Conference on Thermoelectrics*, 2000.

[54] A. Matoba *et al.* Investigation of thermoelectric properties of Si/Ge multilayer with ultra-heavily b doping. *Materials Transactions 49, 1723-1727*, 2008.

[55] G. V. Chester and A. Therllung. The law of wiedemann and franz. *Proc. R. Soc. London 77, 1005*, 1961.

[56] A. Balandin and K. L. Wang. Effect of phonon confinement on the thermoelectric figure of merit of quantum wells. *Journal of Applied Physics 84, 6149*, 1998.

[57] M. Cutler and N. F. Mott. Observation of anderson localization in an electron gas. *Physical Review 181, 3*, 1969.

[58] J. P. Heremans. Low-dimensional thermoelectricity. *Acta Physica Polonica A 108, 4*, 2005.

[59] Vashaee D and Shakouri A. Improved thermoelectric power factor in metal-based superlattices. *Physical Review Letters 92, 10*, 2004.

[60] D. Vashaee and A. Shakouri. Electronic and thermoelectric transport in semiconductor and metallic superlattices. *Journal of Applied Physics 95, 3*, 2004.

[61] Bo Tyu *et al.* Enhancement of thermoelectric properties by modulation-doping in silicon germanium alloy nanocomposites. *Nanoletters 12, 2077-2082*, 2012.

[62] H.-J. Herzog *et al.* SiGe-based Fets: Buffer issues and device results. *Thin Solid Fikms 380, 36-41*, 2000.

[63] T. M. Tritt. *Thermal Conductivity: Theory, Properties and Applications.* Kluwer Academic/Plenum Publishers, 2004.

[64] R. H. Dalitz and Sir Rudolf Peierls. *Selective Scientific Papers of Sir Rudolf Peierls with Commentary.* Imperial College Press, 1997.

[65] M. V. Simkin and G. D. Mahan. Minimum thermal conductivity of superlattices. *Physical Review Letters 84, 5*, 2000.

[66] P. Hyldgaard and G. D. Mahan. Phonon superlattice transport. *Physical Review B 56, 17*, 1997.

[67] Shin ichiro Tamura and Yukihiro Tanaka. Phonon group velocity and thermal conduction in superlattices. *Physical Review B 60, 4*, 1999.

[68] Gang Chen. Phonon heat conduction in nanostructures. *Int. J. Therm. Sci. 39, 471-480*, 2000.

[69] A. Balandin. Thermoelectric applications of low-dimensional structures with acoustically mismatched boundaries. *Phys. Low-Dim. Struct. 5/6, 73-91*, 2000.

[70] S. T. Huxtable *et al.* Thermal conductivity of Si/SiGe and SiGe/SiGe superlattices. *Applied Physics Letters 80, 10*, 2002.

[71] V. Narayanamurti *et al.* Selective transmission of high-frequency phonons by a superlattice: The "dialectric" phonon filter. *Physical Review Letters 43, 57*, 1979.

[72] S. M. Lee *et al.* Thermal conductivity of Si-Ge superlattices. *Applied Physics Letters 70, 22*, 1997.

[73] J. O. Sofo and G. D. Mahan. Thermoelectric figure of merit of superlattices. *Applied Physics Letters 65, 21*, 1994.

[74] J. J. Harris. Review delta-doping of semiconductors. *Journal of Material Science 4, 93-105*, 1993.

[75] R. Dingle *et al.* Electron mobilities in modulation-doped semiconductor heterojunction superlattices. *Applied Physics Letters 33, 665*, 1978.

[76] J. P. Dismukes *et al.* Lattice parameter and density in germanium-silicon alloys. *The Journal of Physical Chemistry 68, 10*, 1964.

[77] B. S. Meyerson *et al.* Cooperative growth phenomena in silicon/germanium low-temperature epitaxy. *Applied Physics Letters 53, 25*, 1988.

[78] D. W. Greve and Marco Racanelli. Construction and operation of an ultrahigh vacuum chemical vapor deporition epitaxial reactor for growth of ge_xsi_{1-x}. *Journal of Vacuum Science Technology B 8, 3*, 1990.

[79] D. J. Robbins *et al.* A model for heterogeneous growth of $Si_{1-x}Ge_x$ films from hybrides. *Journal of Applied Physics 69, 3729*, 1991.

[80] G. Isella *et al.* Low-energy plasma-enhanced chemical vapor deposition for strained Si and Ge heterostructures and devices. *Solid-State Electronics 48, 1317-1323*, 2004.

[81] C. Rosenblad *et al.* Silicon epitaxy by low-energy plasma enhanced chemical vapor deposition. *Journal of Vacuum Science Technology A 16, 5*, 1998.

[82] Mask Aligner SUSS MicroTec. `Url:http://www.suss.com/en/products-solutions/products/mask-aligner/maba6/details.html.`

[83] Oxford Plasma Instruments. `Url:http://www.oxford-instruments.com.`

[84] Surface Technology Systems STS. Url:http://www.stsystems.com.

[85] Oxford Instruments System 100 ICP 180 PECVD. Url:http://www.oxford-instruments.com/businesses/plasma-technology.

[86] Plassys MEB 400s e-beam evaporator. Url:http://www.jwnc.gla.ac.uk/facility-metallisation.htm.

[87] Plassys MP 900S Sputter Coating Tool. Url:http://www.kelvinnanotechnology.com/equipment/metallisation/plassys_mp900s.html.

[88] MicroChemicals AZ2070 resist. Url:http://www.microchemicals.eu/technical_information.

[89] L. Ferre *et al.* Measurement methods of thermal conductivity for SiGe thermoelectric materials. *Journal of Electronic Materials 10.1007/s11664-01302505-3*, 2013.

[90] Flutec PP3 datasheet. Url:http://www.fluoros.co.uk.

[91] SOI wafers from SOITEC. Url:http://www.soitec.com.

[92] Y. Zhang *et al.* High temperature imaging using a thermally compensated cantilever resistive probe for scanning thermal microscopy. *Journal of Vacuum Science Technology B 30, 1*, 2012.

[93] P. S. Dobson *et al.* Microfabricated temperature standard based on johnson noise measurement for the calibration of micro- and nano-thermometers. *Review Science Instruments 76, 054901*, 2005.

[94] VEECO 3100 AFM. Url:http://membrane.ces.utexas.edu/files/2012/07/afm.pdf.

[95] G. Chen *et al.* Heat conduction in alloy-based superlattices. *17th International Conference on Thermoelectrics*, 1998.

[96] S. Chakraborty *et al.* Thermal conductivity in strain symmetrized Si/Ge superlattices on si(111). *Applied Physics Letters 83, 20*, 2003.

[97] C. Dames and G. Chen. 1ω, 2ω and 3ω methods for measurements of thermal properties. *Review of Scientific Instruments 76, 124902*, 2005.

[98] D. G. Cahill. Thermal conductivity measurement from 30 k to 750 k: the 3ω method. *Review Science Instruments 61, 2*, 1990.

[99] T. Yamane *et al.* Measurement of thermal conductivity of silicon dioxide thin films using a 3ω method. *Journal of Applied Physics 91, 12*, 2002.

[100] T. h. Geballe and G. W. Hull. Seebeck effect in germanium. *Physics Review 94, 1134*, 1954.

[101] D. J. Kim *et al.* Measurement of thermal conductivity of TiO_2 thin films using 3ω method. *International Journal of Thermophysics 25, 1*, 2004.

[102] T. Borca-Tasciuc *et al.* Data reduction in 3ω method for thin-filmm thermal conductivity determination. *Review of Scientific Instruments 72, 4*, 2001.

[103] Lake Shore 7500/9500 Series Hall System User's Manual. Appendix a. Hall effect measurements.

[104] I. Isenberg *et al.* Improved method for measuring Hall coefficients. *Review of Scientific Instruments 19, 10*, 1948.

[105] J. H. Klootwijk and C. E. Timmering. Merits and limitations of circular TLM structures for contact resistance determination dor novel III-V HBTs. *Int. Conference Proc. on Microelectronic Test Structures 17*, 2004.

[106] A. Samarerlli *et al.* Power factor characterization of Ge/SiGe thermoelectric superlattices at 300 k. *Journal of Electronic Materials 42, 7*, 2013.

[107] S. Cecchi *et al.* Ge/SiGe superlattices for thermoelectric energy conversion devices. *Journal of Material Science 48, 2829-2835*, 2013.

[108] C. N. Liao *et al.* Thermoelectric characterization of Si thin films in silicon-on-insulator wafers. *Journal of Applied Physics 86, 6*, 1999.

[109] J. de Boor and V. Schmidt. Complete characterization of thermoelectric materials by a combined van der pauw approach. *Advanced Materials 22, 4303-4307*, 2010.

[110] T. H. Geballe and G. W. Hull. Seebeck effect in silicon. *Physical Review 98, 4*, 1955.

[111] B. Abekes *et al.* Thermal conductivity of Ge-Si alloys at high temperatures. *Physical Review 125, 1*, 1962.

[112] L. Ferre Llin *et al.* The cross-plane Thermoelectric properties of p-Ge/Si_0.5Ge_0.5 superlattices. *Applied Physics Letters 103, 143507*, 2013.

[113] L. D. Hicks *et al.* Use of quantum-well superlattices to obtain a high figure of merit from nonconventional thermoelectric materials. *Applied Physics Letters 63, 23*, 1993.

[114] M. Kummer *et al.* Low energy plasma enhanced chemical vapor deposition. *Materials Science and Engineering B89, 288-295*, 2002.

[115] D. Paul. Project periodic report green silicon: Second year. *Green Silicon: Project No. 257750*, 2012.

[116] D. Paul. Project periodic report green silicon: Third year. *Green Silicon: Project No. 257750*, 2013.

[117] K. Gallagher *et al.* Ohmic contacts to n-type germanium with low specific contact resistivity. *Applied Physics Letters 100, 022113*, 2012.

[118] W. Kim *et al.* Cross-plane lattice and electronic thermal conductivities of ErAs: InGaAs/InGaAlAs superlattices. *Applied Physics Letters 88, 242107*, 2006.

[119] Y. H. Xie *et al.* Semiconductor surface roughness: Dependence on sign and magnitude of bulk strain. *Physical Review Letters 73, 22*, 1994.

[120] S. F. Nelson and T. N. Jackson. Ohmic contacts to n-type silicongermanium. *Applied Physics Letters 69, 3563*, 1996.

[121] *Materials, Preparation, and Characterization in Thermoelectrics.* CRC Press, Francis and Taylor, 2012.