UNIVERSITY OF GLASGOW

MOSFET transistor fabrication on AFM tip

by

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A thesis submitted in partial fulfillment for the
degree of Doctor of Philosophy

in the
School of Engineering
Electronics and Nanoscale Engineering Research Division

July 2014

"Our greatest weakness lies in giving up. The most certain way to succeed is always to try just one more time."

Thomas A. Edison

UNIVERSITY OF GLASGOW

Abstract

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The project is concerned with the development of methods for the fabrication of magnetic sensor devices on Atomic Force Microscopy (AFM) probes and their characterization. The devices use the principle of the Hall effect (based on the Lorentz force) to sense the magnetic properties of a magnetized specimen.

In the past Hall bar sensors have been fabricated using semimetals such as Bismuth, or using 2-d electron gas material based on heterojunctions in III-V material. The former probes are limited by low sensitivity. The latter are limited by the difficulty encountered when trying to integrate the device with a force-sensing cantilever. The highest spatial resolution reported for a Hall bar operating at room temperature is 50 nm. Due to quantum effects (long mean free path), scaling down devices based on high mobility material results in a drop in sensitivity. For magnetic material studies of current interest higher resolutions are required. To achieve this goal in a material system which is compatible with micromachining the proposed approach utilises silicon as the sensing material. Silicon Hall bars have already been reported to work for large scale devices.

This thesis presents the development of p-type enhancement mode MOSFET transistor fabrication process on a tip of Atomic Force Microscope (AFM) probe. The active device fabrication process was developed in order to allow fabrication of a magnetic sensor for Scanning Hall Probe Microscope (SHPM). The Hall bar was constructed on the apex of the AFM tip of attractive mode probes.

The fabrication is performed in batches by using common semiconductor techniques leading to micromachining of the Si substrate, formation of the active device and cantilever release step. The transistor characteristics are presented, compared with expected performance of the modelled device and the reasons for differences are discussed.

In this work, a method for application of spin-on-dopant on highly topographic structures is developed. Other encountered process incompatibilities are dealt with to finally present a full process for p-type enhancement mode MOSFET transistor on AFM tip fabrication.

The technological limitations of this process were investigated and set the spatial resolution at approximately 15 nm, which is over 3 times higher than the reported technology at present.

The technology developed under this project has application beyond that of imaging magnetic field: the fabrication of a MOSFET transistor at the tip of an AFM will permit the measurement of rapidly changing pH or other electrochemical signals, high frequency potentials in devices or biological cells or capacitance changes as a function of voltage in semiconducting materials.

Acknowledgements

Taking the decision to study towards Ph.D. was relatively easy. Sticking with it was challenging due to hardships of trying to achieve something that nobody has ever done before. Now at the end of the project, if somebody asks me what it takes to complete the Ph.D. project, my answer will be:

- a brilliant, wise and supportive supervisor such as **Prof. Jonathan Weaver**

- a supportive and helpful group such as AFM and Hyperlithography Group part of which are/were **Dr Phil Dobson, Dr Yuan Zhang, Dr David Burt, Dr Kevin Docherty, Lesley Donaldson**

- having access to knowledgeable and resourceful people such as **Dr Stephen Thoms, Dr Haiping Zhou, Dr Xu Li**

- a kind and patient lab staff such as Dry Etch Laboratory staff part of which are **Mark Dragsnes, Douglas Lang, Ronnie Roger**

- a friendly and operative staff such as James Watt Nanofabrication Centre staff part of which are **Mary Robertson, Helen McLelland, Susan Ferguson, Elizabeth Wyllie, Linda Pollock, Eve Aitkenhead, Vanda Brash, Margaret McCann, William Monaghan, Robert Harkins, Donald Nicolson** and last but not least **David Gourlay**, with whom I share my passion for good jokes and justice

- a skillful, knowledgeable and very approachable group of professionals such as **Sara McFarlane, Dr Corrie Farmer, Dr David McCloy**

- open and valuable research fellow friends such as **Dr James Grant** and **Dr Phillipe Velha**

- fellow Ph.D. students, who not only help with research but also make the free time count, such as **Dr Zhixiong Hu a.k.a. Jason, Andrew Greer, Ed Pratt, Alex Vasiev, Salah Sharabi, Sankar Peralagu, Chris Martin, Carla Camasta**.

Special thanks go to **Dr Tim Drysdale** for offering me to stay at Glasgow for this project.

Apart from all these people, there are many names of those who allowed it to happen: my family, management, administration and Engineering and Physical Sciences Research Council (EPSRC).

During this project I have made many new acquaintances, however, those who I am proud to call true Scottish friends, who made my time in Glasgow much more enjoyable, are **Fraser Anderson** and **David Docherty**.

Contents

Abstract **v**

Acknowledgements **vii**

List of Figures **xv**

List of Tables **xxiii**

Abbreviations **xxv**

Naming convention **xxvii**

1 Introduction **1**
1.1 Scanning Probe Microscopy . . . 2
1.1.1 Atomic Force Microscopy . . . 3
1.2 Magnetic field metrology . . . 8
1.3 Hall bars and material systems . . . 9
1.3.1 Which material to choose? . . . 13
GaAs . . . 15
InSb . . . 15
Bi . . . 15
Si . . . 15
1.4 Prior Art at Glasgow . . . 16
1.4.1 Functionalization of AFM . . . 16
1.4.2 Tip design . . . 19
1.4.3 Diffusion . . . 22
1.4.4 Work of B. K. Chong . . . 24
1.5 Motivation and research goals . . . 26
1.6 Fundamental design choices . . . 27

2 Background **31**
2.1 Diffusion . . . 31
2.2 Float coating . . . 34
2.3 Dry etching . . . 39
2.3.1 Interferometry . . . 42

2.4 Hall effect . . . 44
2.4.1 Calculations for Si MOSFET Hall bar . . . 48
2.4.2 Noise . . . 52
2.5 Diode . . . 55
2.6 MOSFET transistor . . . 56
2.6.1 Application . . . 57

3 Fabrication **59**
3.1 Triple mask design . . . 59
3.2 NiCr and grass effect . . . 64
3.3 Overhang on edge of pyramid apex . . . 71
3.4 Diffusion challenges on AFM pyramid . . . 75
3.5 Ordering of diffusion processes . . . 77
3.6 Phosphorus contamination . . . 78
3.7 Slow Si dry etch . . . 80
3.7.1 Error analysis of etch depth . . . 84

4 Measurements **87**
4.1 Diffusion depth measurement . . . 87
4.1.1 Angle-lap and staining . . . 87
4.1.2 Selective etch . . . 88
4.1.3 Isolation etch . . . 89
4.1.4 Measurement results . . . 90
4.2 Transistor measurements . . . 93
4.3 Variation in time . . . 96
4.4 DC characteristics, yield and discussion of results . . . 102
4.4.1 Misalignment . . . 111
4.5 AFM . . . 113
4.6 Technological limit . . . 119

5 Summary and future work **123**
5.1 Summary . . . 123
5.2 Future work . . . 124

A Diffusion depth test process **131**

B Batch fabrication process **133**

C Transistor fabrication process **137**

D Release etch process **143**

E BP80+RIE processes **145**

F BP80 processes **147**

G STS processes **149**

H Furnace - level 7 **151**

I RTA **153**

J Notes **155**
J.1 Wafer specification 155
J.2 KOH etch rates and uniformity results 155
J.3 Solvent cleaning process 155

K Vistec VB6 - understanding resolution **157**

L Threshold voltage calculations **159**

M Current calculations in saturation region **161**

Bibliography **163**

List of Figures

1.1 *Interatomic force vs. distance curve with different AFM modes of operation indicated.* 4

1.2 *Diagram presenting principle of modern AFM setup.* 5

1.3 *Diagram presenting Si probe fabrication process proposed by Wolter:* ***a)*** *SiO_2 is thermally grown on Si wafer;* ***b)*** *by means of photolithography and an etching process, the window in the SiO_2 mask is formed;* ***c)*** *anisotropic (KOH) etch is performed to make the wafer thinner (double required thickness of the cantilever);* ***d)*** *back-side of the wafer is patterned using photolithography and the pattern is transferred into the SiO_2 layer;* ***e)*** *KOH wet etch is performed to etch through the membrane and release the cantilever;* ***f)*** *the SiO_2 is stripped from both wafer sides;* 6

1.4 *Diagram presenting fabrication process of Si_3N_4 probe with tips proposed by Albrecht:* ***a)*** *on a Si wafer a SiO_2 layer is thermally grown;* ***b)*** *by using photolithography and etching process a 3 μm window is opened in the SiO_2 mask;* ***c)*** *a pyramidal pit is formed by using anisotropic etch;* ***d)*** *the SiO_2 mask is stripped;* ***e)*** *a Si_3N_4 layer is deposited;* ***f)*** *the deposited layer is shaped into the cantilever by using photolithography and etching processes;* ***g)*** *a glass plate with a saw cut and a Cr bond-inhibiting region is anodically bonded to the Si_3N_4 cantilever;* ***h)*** *by saw cutting the plate, the cantilever is exposed and the probe body is formed;* ***i)*** *the Si substrate is etched away releasing the cantilever;* 7

1.5 *Sensitivity comparison of different Hall bars operating at room temperature - graph presenting sensitivity vs. spatial resolution from data gathered in table 1.2. Full symbol corresponds to a Hall bar device fabricated on top of the AFM tip. Semi-full symbols present achievable devices according to calculations presented in subsection 2.4.1. The lines are sensitivity extrapolation of Yamaguchi and Yang device scaling down.* 12

1.6 *Magnetic field resolution comparison of different Hall bars operating at room temperature - graph presenting magnetic field resolution vs. spatial resolution from data gathered in table 1.2. Full symbol corresponds to a Hall bar device fabricated on top of the AFM tip. Semi-full symbols present achievable devices according to calculations presented in subsection 2.4.1. The lines are magnetic field resolution extrapolation of Yamaguchi and Yang device scaling down.* 13

1.7 *Diagram presenting Hall bar areas sensitive to magnetic field depending on the length of inelastic mean free path.* 14

1.8 *Diagram presenting an AFM tip (with a sensor fabricated on the cantilever) scanning over a sample. Specific distances are indicated.* 17

1.9 *Diagram presenting Si AFM tip fabrication process:* ***a)*** *lightly* $n-doped$ (100) *oriented Si wafer coated with* SiO_2 *and* Si_3N_4*;* ***b)*** *membrane mask - windows opened in hard mask using photolithography and* C_2F_6 *reactive-ion dry etch process;* ***c)*** *membrane definition using* KOH *with* IPA *solution;* ***d)*** *tip mask - windows opened in hard mask using photolithography and* C_2F_6 *reactive-ion dry etch process;* ***e)*** *tip definition using* KOH *with* IPA *solution;* ***f)*** *mask stripping and active device fabrication;* ***g)*** *cantilever release etch using dry etch Bosch process.* 18

1.10 *Diagram presenting the influence of mask size and etching time on the tip height and the apex size of the Si AFM tip during* KOH *etching. On the left hand side the tip height does not change since the etching time is constant, but the mask size change influences the apex size. On the right hand side, the mask size is constant, but the etching time varies. The longer the etch, the higher the tip and the smaller the apex becomes.* . . . 19

1.11 *SEM diagram of a Si AFM tip with indicated crystallographic planes.* . . 21

1.12 *Diagram presenting a feature with steep sidewalls when float-coated with PMMA resist.* 22

1.13 *Diagram presenting a triangle tip with forming it crystallographic planes (on the left top view, on the right diagonal view) [90].* 22

1.14 *Diagram presenting two processes for patterning of SOD at Glasgow.* ***Procedure I****:* ***a)*** *for a Si wafer* ***b)*** *SOD is applied by spin coating;* ***c)*** *by using a photolithography process the resist is patterned;* ***d)*** *the resist is used as a mask in a* $buffered\ HF$ *wet etch process in order to transfer the pattern into the SOD layer;* ***e)*** *after removal of photoresist the SOD pattern remains only in area selected for doping;* ***Procedure II****:* ***a)*** *on a Si wafer* ***b)*** *the* SiO_2 *is thermally grown;* ***c)*** *by combining photolithography process and dry/wet etch process, the pattern is transferred in the* SiO_2 *hard mask;* ***d)*** *the SOD is applied by spin coating;* 23

1.15 *Diagram presenting probe body and SEM diagrams of its specific elements (active device located on the AFM tip in the top left hand corner,* 150 *nm thick Al leads in the top right hand corner, probe body and* 150 *nm thick Al pads). Explanation of the lithography stages is given. On the left hand side lithography stages are presented in order if the lithography techniques were chosen based on the minimum feature size. On the right hand side the stages are presented in order how they are performed.* 29

2.1 *Different doping profiles of B in Si substrate for two different diffusion times and models (Constant Total Dopant and Constant Surface Concentration). Profile calculations based on [101].* 33

2.2 *Diagram presenting the tendency of spin-coated resist to become unacceptably thin when passing over an apex edge.* 34

2.3 *SEM diagram illustrating a problem with the resist thickness during lift-off technique. The metallic film forms a continuous layer leaving no gap for the solvent to penetrate and dissolve the resist. Also, even if the resist does dissolve, the metal film is solid and stays in place.* 34

2.4 *SEM diagram presenting a good resist structure (rule of thumb:* $resist\ thickness = 2 \cdot metal\ thickness$*) and resist profile (an undercut) allowing fabrication of discontinuous metallic films for lift-off.* 35

2.5 *Float coating technique:* ***a)*** *a drop of a PMMA resist is dropped onto the water surface and spreads rapidly over the surface;* ***b)*** *o-xylene solvent evaporates and the resist solidifies;* ***c)*** *water is removed and the solid resist film drapes over the sample.* 35
2.6 *Plot of thicknesses of* 1.5% 2041 *and* 2.5% 2010 *float coated PMMA resists.* 35
2.7 *Diagram presenting locally tripled resist thickness due to wrinkles in the float-coated PMMA resist.* 36
2.8 *The two diagram on the left explain what is presented in each column. Each circle represents one float coating layer of resist. The triangle is to indicate equal separation between central points of the 3 resist layers. Diagram B is the same as diagram A, but cropped to fit the area of* 3" *wafer. Finally column A presents modelled results of 3-layered resist thickness variation depending on the separation a between central points of each layer. Column B presents the the same results but cropped to fit the* 3" *wafer. The brighter the whole modelled* 3" *wafer area, the more uniform the resist thickness is.* 37
2.9 *Modelled PMMA resist (three float coated layers) profiles for different distances between centres of films.* 37
2.10 *Diagram showing sputtering tool and its principle of operation. Ar is ionized by RF power and the ions are accelerated towards the target material. After impact target atoms are released and travel to the substrate where they form layers of atoms of the thin film.* 40
2.11 *Diagram presenting steps of the DRIE etching process.* 42
2.12 *SEM diagram presenting Si AFM cantilever released in the Bosch process. Each indentation in the sidewall of the cantilever represent one Bosch process cycle.* 43
2.13 *Diagram presenting the principle of operation of an interferometer used for dry etch process depth control.* 43
2.14 *Schematic demonstration of the Hall effect.* 45
2.15 *Diagrams presenting COMSOL [114] simulation results of the MOSFET capacitor in a strong inversion. The induced charge thickness depends on the applied voltage and the dielectric layer thickness. For both devices the top electrode width is equal to* $W = 15\ nm$ *and the applied voltage is* $-7.5\ V$. 46
2.16 *The influence of Hall bar wire length and Hall angle on Hall geometrical factor.* 47
2.17 *Diagram presenting COMSOL [114] simulation results of electrical field distribution in* SiO_2. 51
2.18 *Resistive device noise figure across the range of frequencies.* 52
2.19 *Block diagram of the STM system with the noise reduction method proposed by Abraham et al.* 54
2.20 *Block diagram presenting the noise reduction method proposed by Abraham et al. to the SHPM.* 54
2.21 *Diagram of a Si diode with a highly doped layer used as a conductive path.* 55
2.22 *Diagram of a plan view with a Si diode Hall bar. The* SiO_2 *layer is* 70% *transparent to allow the visibility of doped area.* 55
2.23 *Diagram presenting the gate length and width.* 56
2.24 *Diagram of an induced p-type channel Si MOSFET transistor.* 57

2.25 *On the left there is the SEM diagram of a lithographically defined* 280 *nm Hall bar device located on the apex of the AFM tip. The indicated area is zoomed in on the right hand side. The* 150 *nm thick Al metallization sits on top of* 15 *nm* SiO_2 *gate/field oxide.* 58

3.1 *Diagram presenting thermally grown* SiO_2 *on two Si crystallographic planes (*$< 100 >$ *and* $< 313 >$*). Selective removal of* SiO_2 *by using dry etch process may be problematic due to different* SiO_2 *thickness dependent on the plane.* 61
3.2 *SEM of a FIB milled trench in a Si AFM pyramid with thermally grown* SiO_2 *and sputtered Al (image courtesy of Dr Yuan Zhang).* 62
3.3 *SEM of a cross section of a Si AFM pyramid with thermally grown* SiO_2 *and sputtered Al with indicated step in* SiO_2 *layer (image courtesy of Dr Yuan Zhang).* 62
3.4 *SEM images of dry etched* SiO_2 *windows with "grass" problem.* 65
3.5 *SEM of a sample processed to the stage just before dry etching of* 300 *nm of* SiO_2 *with patterned,* 75 *nm of* $NiCr$ *as a mask.* 65
3.6 *SEM images of corners of* 1 *mm square patterns processed following the proposed process with step 7a).* 66
3.7 *SEM images of corners of* 1 *mm square patterns processed following the proposed process with step 7b).* 66
3.8 *SEM images of corners of* 1 *mm square patterns processed following the proposed process with step 7c).* 67
3.9 *Sample processed following the proposed process with step 7d) and dry etched in* CHF_3 *plasma.* 67
3.10 *EDX result of the sample with intensive "grass" issue* 68
3.11 *SEM of patterns processed as indicated in modified process (etched using* $CHF_3 + Ar$*).* 70
3.12 *SEM of a crack in* $NiCr$ *mask along the edge of the AFM pyramid apex.* 71
3.13 *SEM of a tip of AFM pyramid after defining it with wet etch process and removing wet etch hard mask.* 71
3.14 *Diagram presenting evaporated metal layer on different apex shapes of the functionalized Si AFM tips.* 71
3.15 *SEM of an AFM pyramid with hard mask after* KOH *etch. The white, square-shaped, electron charging like line indicates the pyramid apex.* . . 72
3.16 *SEM of a crack in* $NiCr$ *mask along the edge of the AFM pyramid apex. Sample processed with* 300 *nm of wet thermally grown* SiO_2*.* 73
3.17 *SEM of a crack in* $NiCr$ *mask along the edge of the AFM pyramid apex. Sample processed with* 600 *nm of wet thermally grown* SiO_2*.* 73
3.18 *SEM of an AFM pyramid - the edge processed in* KOH *solution for* 1 *min.* 74
3.19 *SEM of an AFM pyramid - the edge processed in* KOH *solution for* 20 *s and then coated with* 300 *nm of PECVD* SiO_2 *and* 75 *nm of evaporated* $NiCr$*.* 74
3.20 *Photo of a substrate with a spin-on dopant poured onto the substrate which has been left to dry up. After the thermal process (see table I.1) cracks and adhesion issues in the doped oxide layer can be observed.* 76
3.21 *Photo of a substrate with AFM pyramids after applying the dopant using a brush and conducting full diffusion process. No cracks and adhesion issues in the doped oxide layer can be observed.* 76

3.22 *SEM of the unidentified contamination.* . . . 78
3.23 *SEM of the unidentified contamination.* . . . 79
3.24 *EDX result of the sample area presented in figure 3.23(a).* . . . 79
3.25 *OES with a step size of* 1 *nm done on a barrel asher used for* O_2 *ash (courtesy of Dr Haiping Zhou).* . . . 82
3.26 *The plot of the depth etch versus time. The process is conducted in 80+RIE machine and the process parameters are: power* 10 W, SF_6 *flow rate* 5 *sccm /* N_2 *flow rate* 45 *sccm, pressure* 10 mT*).* . . . 83

4.1 *Schematic view of the angle lapping and staining method with indicated dimensions.* . . . 88
4.2 *Diagram of the setup for the selective etch.* . . . 89
4.3 *Diagrams of the samples at different level of dry etching for the isolation etch technique:* ***a)*** *no etch;* ***b)*** *etched half way through and* ***c)*** *etched through the p-type layer.* . . . 89
4.4 *Plan view of the TLM pattern used for measurements of p+ doped Si layer thickness.* . . . 90
4.5 *Diagram of the measurement setup for the isolation etch test.* . . . 90
4.6 *Plot of the currents measured on sample I, pad separation* 15 μm*, column 4, rows 1-10.* . . . 91
4.7 *Average current measurement results of TLM pattern. Half of the sample I (columns 1 and 2) is etched to the depth of 40 nm.* . . . 92
4.8 *Average current measurement results of TLM pattern. Half of the sample II (columns 1 and 2) is etched to the depth of 60 nm.* . . . 92
4.9 *Average current measurement results of TLM pattern. Half of the sample III (columns 1 and 2) is etched to the depth of 80 nm.* . . . 93
4.10 *Connectivity setup (and naming convention) for obtaining* $I_d - V_{ds}$ *characteristics of a Si MOSFET transistor.* . . . 94
4.11 *SEM diagram of a p-type MOSFET transistor fabricated on the apex of the AFM tip.* . . . 94
4.12 *Plot of the* $I_d - V_{ds}$ *characteristics of the transistor presented in figure 4.11.* . . . 94
4.13 *Plot of the* I_g *currents measured during obtaining* $I_d - V_{ds}$ *characteristics of the transistor presented in figure 4.11. As expected the* I_g *current shows no dependence on the* V_{ds} *or* V_{gs}*.* . . . 95
4.14 *Plot of the* $I_d - V_{gs}$ *(for* $V_{ds} = -300\ mV$*) characteristics of the transistor presented in figure 4.11. The threshold voltage is equal to approximately* $V_{th} = -3\ V$*.* . . . 95
4.15 *Connectivity setup (and naming convention) for obtaining* $I_g - V_{gb}$ *characteristics of a* SiO_2 *dielectric layer - gate oxide.* . . . 96
4.16 *Plot of* SiO_2 *breakdown voltage measurement (*$V_{br} = -39\ V$*) a p-type MOSFET transistor fabricated on the apex of the AFM tip.* . . . 96
4.17 *Plot presenting the* 15 *nm* SiO_2 *breakdown voltages of* 10 *devices. Devices above* $V_{br} = -42\ V$ *show no breakdown due to the probe station voltage safety limit set at this* $\pm 42\ V$*.* . . . 96
4.18 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken immediately after device fabrication.* . . . 97

4.19 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after imaging with SEM microscope.* 97
4.20 *SEM presenting zoomed in device from the figure 4.11. The* SiO_2 *area indicated in yellow is believed to contain trapped electrons from SEM imaging.* 98
4.21 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after* 24 *hour long UV light treatment.* 99
4.22 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after the device being hidden from light access for* 5 *months.* 99
4.23 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after RTA annealing of the device at* 400 ^oC *in ambient of* N_2 *for* 5 *minutes.* 100
4.24 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after additional RTA annealing of the device at* 500 ^oC *in ambient of* N_2 *for* 5 *minutes.* 101
4.25 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after additional RTA annealing of the device at* 550 ^oC *in ambient of* N_2 *for* 5 *minutes. (This characteristic is identical to the one previously presented in figure 4.12.)* 102
4.26 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor category I fabricated on the apex of the AFM tip. The device has a broken oxide, which is clearly visible on the* $I_g - V_{ds}$ *characteristics presented in figure 4.27.* 103
4.27 $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category I fabricated on the apex of the AFM tip. The characteristics presents the current* I_g *being dependent on the* V_{gs}. 103
4.28 *SEM diagrams of device failures. Red arrows indicate the areas of interest.* 104
4.29 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor category II fabricated on the apex of the AFM tip. The devices show no transconductance.* . . . 104
4.30 $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category II fabricated on the apex of the AFM tip.* 104
4.31 *Diagram showing a profile of a Si sample with* 150 *nm deep B diffusion. Different doping levels are indicated. The longer the overetch is, the lower the doping level of the doped area is effectively and the more difficult it becomes to form a good ohmic contact.* 105
4.32 *Interferometer trace taken while* CHF_3 *dry etching (for specific process parameters see table E.3) of contact windows in* 15 *nm thick* SiO_2. . . . 106
4.33 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor category III fabricated on the apex of the AFM tip. The device delivers limited current* $I_d < 1\ \mu A$. 107
4.34 $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category III fabricated on the apex of the AFM tip.* 107
4.35 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip.* 108

4.36 $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip.* 109
4.37 *Diagram presenting top and corresponding side view of the parametric source/drain design of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11).* 110
4.38 $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip. The characteristics obtained with regular connectivity setup.* 111
4.39 $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip. The characteristics obtained after swapping source and drain voltages.* 112
4.40 *Diagram of a induced p-type channel Si MOSFET transistor with a misalignment gap between source and the induced channel.* 112
4.41 *SEM diagram of the Veeco OTESPAW probe.* 114
4.42 *SEM diagram of the fabricated AFM probe with a lithographically defined Hall bar device.* 114
4.43 *SEM diagram of the fabricated AFM probe with a lithographically defined Hall bar device. Magnification of figure 4.42.* 114
4.44 *AFM diagram of the sample surface containing a metallic path. The image obtained using Veeco OTESPAW probe. The bright horizontal line indicates a location of the profile presented in figure 4.46.* 115
4.45 *AFM diagram of the sample surface containing a metallic path. The image obtained using the Hall bar probe. The bright horizontal line indicates a location of the profile presented in figure 4.47.* 115
4.46 *Diagram presenting a metallic path profile obtained using Veeco OTESPAW probe. The location of the obtained profile is indicated in the figure 4.44.* 116
4.47 *Diagram presenting a metallic path profile obtained using Hall bar probe. The location of the obtained profile is indicated in the figure 4.45.* 116
4.48 *Diagrams presenting two types of probes scanning over the same sample. Red line indicates a path of the tip scan.* 116
4.49 *AFM diagram of a rough side of single side polished Si substrate. The image obtained using the Veeco probe. The bright diagonal line indicates a location of the profile presented in figure 4.51.* 117
4.50 *AFM diagram of a rough side of single side polished Si substrate. The image obtained using the Hall bar probe. The bright diagonal line indicates a location of the profile presented in figure 4.52.* 117
4.51 *Diagram presenting a rough side of a single side polished Si substrate profile obtained using Veeco probe. The location of the obtained profile is indicated in the figure 4.49.* 118
4.52 *Diagram presenting a rough side of a single side polished Si substrate profile obtained using Hall bar probe. The location of the obtained profile is indicated in the figure 4.50* 118
4.53 *SEM diagram of a set of nano wires fabricated on the apex of the AFM tip. The closer view of the wires presented in figure 4.54.* 120
4.54 *SEM diagram of a set of nano wires fabricated on the apex of the AFM tip. The image obtained using a backscatter electron sensor.* 120

4.55 *Diagram presenting exemplary grey scale profile of the nano line widths obtained from the SEM image presented in figure 4.54). Distance is measured in pixels of the SEM image and* 276 *pixels corresponds to* 200 *nm. The grey intensity is defined by a* 16 *bit long value, where* 0 *corresponds to black and* 65535 *to white.* 121

5.1 *Diagram presenting proposed fabrication process with inverted order of deep KOH etching and active device fabrication processes with a view to maintain wafer rigidity through complex active device fabrication process flow:* ***a)*** *a Si wafer is coated with thermally grown* SiO_2 *and LPCVD* Si_3N_4 *layers (hard mask);* ***b)*** *by the means of photolithography and dry etch, the pattern is transferred into the hard masks;* ***c)*** *wet etch using* 7 *molar KOH with IPA solution forms functionalized AFM tips;* ***d)*** *unbuffered HF is used to strip the hard mask;* ***e)*** *active device is fabricated;* ***f)*** *application by spin coating of the ProTEK B3 on the back side and ProTEK PSB on the front side of the wafer;* ***g)*** *by exposing and developing the ProTEK PSB layer the pattern is transferred;* ***h)*** *wet etch using* 7 *molar KOH with IPA solution forms probe body;* ***i)*** *the ProTEK products are stripped;* ***j)*** *by using photolithography and DRIE dry etch process release etch is performed;* 126

5.2 *Diagram presenting fabrication process of two different* SiO_2 *thicknesses depending on the area:* ***a)*** *the fabrication process starts at the point when the the probe body is defined and highly doped regions are formed;* ***b)*** *thermal growth of field* SiO_2*;* ***c)*** *by lithography process the areas, where field oxide is required, remain coated;* ***d)*** *by using buffered HF the field oxide is etched away;* ***e)*** *resist is stripped away;* ***f)*** *the gate oxide is thermally grown* 127

5.3 *SEM images of cross shape MOSFET gates made of* 150 *nm thick Al using single metallization.* 128

5.4 *SEM image of the nano wires fabricated on the apex of the AFM tip using two electron beam lithographies. Firstly the horizontal lines were fabricated using* 2 *nm of Ti and* 10 *nm of Pt. The measured wire width of* 15 *nm. Then the vertical lines were fabricated using* 2 *nm of Ti and* 15 *nm of Pt. The measured wire width of* 25 *nm.* 128

5.5 *Diagram presenting required changes in order to fabricate the technologically limited active device on AFM tip.* 129

List of Tables

0.1 *Table presenting naming convention of materials used at Glasgow.* xxvii

1.1 *Characteristics of different magnetic field measurement techniques.* 9
1.2 *Characteristics of some Hall bar devices operating at room temperature.* . 11

2.1 *Table presenting surface concentrations and junction depths for the two models (Constant Surface Concentration and Constant Total Dopant), different impurities, different diffusion temperatures and times. Calculation based on [101].* 33
2.2 *Statistical data of 3-layered resist thickness and uniformity resulting from different separation distance (a) of the layers. The first (q1) and third (q3) quartiles are presented to give better statistical understanding of the 3-layered resist thickness variations.* 38
2.3 *Table comparing different dry etch processes characteristics.* 41

3.1 *Comparison of some characteristics of ion implantation and diffusion.* . . 60
3.2 *Metals commonly used as a dry etch mask for etching SiO_2 in CHF_3 plasma and considerations for selection as an intermediate layer.* 63
3.3 *Etching results for different process parameters.* 82
3.4 *Table presenting results obtained from etch depth measurements of 4 samples, each etched with the same process parameters for time j [min]. Each measurement point i was taken in different location on the sample. The measured depths $x_{j,i}$ are in [nm].* 84

4.2 *Table presenting numbers (and percentages) of device categories and types for devices fabricated on the apex of the AFM tip.* 110
4.1 *Table presenting values of 3 sets of parameters used for design of the Si MOSFET transistors fabricated on the apex of the AFM tip (device type I presented in figure 4.11). The parameter names are defined in figure 4.37.* 110
4.3 *Table presenting minimum, average and maximum values of the 16 nano line width measurements. Nano line number 1 is on the left hand side of the set presented in figure 4.55.* 121

E.1 *Process for etching* 300 *nm SiO_2 in BP80+RIE - name: phosdiffwindows.* 145
E.2 *Process for etching* 300 *nm SiO_2 in BP80+RIE - name: borondiffwindows.* 145
E.3 *Process for etching* 15 *nm SiO_2 in BP80+RIE - name: contactwindows.* . 145
E.4 *Process for etching* 300 *nm SiO_2 in BP80+RIE - name: chf3argonetch.* . 146
E.5 *Process for O_2 ash in BP80+RIE - name: O2-ash-80.* 146
E.6 *Process for O_2 ash in BP80+RIE - name: O2-ash-20.* 146
E.7 *Process for slow Si etching in BP80+RIE - name: slowsietch.* 146

F.1 *Process for stripping* 40 *nm* SiO_2 / 60 *nm* Si_3N_4 *layers in BP80 - name: bothdielectrics.* 147
F.2 *Process for* O_2 *ash in BP80 - name: O2-ash-80-bp80.* 147

G.1 *Process for release etch of Si cantelevers in STS - name: release.* 149
G.2 *Process implementing Bosch process for DRIE etching of Si - etch rate* 2 $\mu m/min$ *- name: udo1.* 149
G.3 *Process for* O_2 *ash in STS - name: Xu_ash2.* 149

H.1 *Furnace processes.* 151

I.1 *RTA processes.* 153

J.1 *KOH etch uniformity and etch rates for* 5 *h* 17 *min etch.* 155

Abbreviations

AFM	**A**tomic **F**orce **M**icroscope
APC	**A**tomatic **P**ressure **C**ontroller
CAN	**C**eric **A**mmonium **N**itrate
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
DRIE	**D**eep **R**eactive **I**on **E**tching
EDX	**E**nergy **D**ispersive **X**-ray
FIB	**F**ocused **I**on **B**eam
IMFP	**I**nelastic **M**ean **F**ree **P**ath
ISFET	**I**on **S**ensitive **F**ield **E**ffect **T**ransistor
IPA	**I**so**P**ropyl **A**lcohol
LOCOS	**LOC**al **O**xidation of **S**ilicon
LPCVD	**L**ow **P**ressure **C**hemical **V**apour **D**eposition
MEMS	**M**icro **E**lectro **M**echanic **S**ystem
MFM	**M**agnetic **F**orce **M**icroscope
MIBK	**M**ethyl **I**so**B**utyl **K**etone
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
OES	**O**ptical **E**mission **S**pectroscopy
PECVD	**P**lasma **E**nchanced **C**hemical **V**apour **D**eposition
PMMA	**P**oly**M**ethyl **M**eth**A**crylate
PVAC	**P**oly**V**inyl **AC**etate
R.O.	**R**everse **O**smosis
RIE	**R**eactive **I**on **E**tching
RHBD	**R**adiation **H**ardened **B**y **D**esign
RTA	**R**apid **T**hermal **A**nnealer
SEM	**S**canning **E**lectron **M**icroscope

SHPM	**S**canning **H**all **P**robe **M**icroscope
SNOM	**S**canning **N**ear-field **O**ptical **M**icroscopy
SOD	**S**pin-**O**n **D**opant
SOG	**S**pin-**O**n **G**lass
SPM	**S**canning **P**robe **M**icroscope
STM	**S**canning **T**unneling **M**icroscope
TEM	**T**ransmission **E**lectron **M**icroscope
UV	**U**ltra **V**iolet

Naming convention

At Glasgow there is a chemical naming convention, which is maintained throughout this thesis. In order to refer to a specific product from the names used, use the table 0.1.

name used	manufacturer	address	product name
primer	Dow Corning	Belgium, Seneffe	Z-6079 Silazane
primer 80/20	MicroChem	USA (MA), Newton	MCC Primer 80/20
Surpass 3000	DisChem	USA (PA), Ridgway	the same
Surpass 4000	DisChem	USA (PA), Ridgway	the same
s1805	Shipley	UK, Coventry	Microposit s1805
s1818	Shipley	UK, Coventry	Microposit s1818
AZ4562	Microchemicals	Germany, Ulm	the same
2010 PMMA	Lucite Int.	USA (TN), Cordova	Elvacite 2010
2041 PMMA	Lucite Int.	USA (TN), Cordova	Elvacite 2041
Microposit Dev. Conc.	Shipley	UK, Coventry	the same
AZ 400k developer	MicroChemicals	Germany, Ulm	the same
borosilica film	Emulsitone	USA (NJ), Whippany	Borosilica film $5 \cdot 10^{20}$
phosphorosilica film	Emulsitone	USA (NJ), Whippany	Phosphorosilica film $5 \cdot 10^{20}$
nanostrip	Chestech	UK, Warwickshire	MS 20D
chrome etchant	MicroChemicals	Germany, Ulm	MS 8 Chrome etchant

TABLE 0.1: *Table presenting naming convention of materials used at Glasgow.*

To Justyna,

my greatest inspiration,

who influenced me to do this.

Chapter 1

Introduction

In 1965 G. E. Moore made the observation that the number of transistors in an integrated circuit of minimum cost increased roughly by a factor of two per year [1]. Based on this he predicted that this trend would continue for some time and could last even for a decade. 10 years later Moore presented another publication [2] confirming that the prediction was correct and was to continue. In a longer term analysis his new prediction was that the progress would slow down to doubling the number of transistors every 2 years. Until today, nearly 40 years later, the famous Moore's Law is still valid [3]. This trend has been maintained thanks to factors such as growing the die size, increasing the reliability of the integrated circuits and shrinking of the transistor dimensions.

Similar law was also formed by Mark Kryder for magnetic data storage using hard disk drives [4]. The data density storage has been increasing since 1956 when IBM RAMAC (2 kb/in^2), first hard disk drive was presented, reaching data density of 625 Gb/in^2 for modern hard disk drives (e.g. Seagate Barracuda 3TB ST3000DM001) [5]. Such progress was possible thanks to magnetoresistance and giant magnetoresistance heads and swithching to perpendicular recording of data [6].

Today, the computer processors on the market consist of a few billions of transistors fabricated with 22 nm ground rules [7]. A single bit of modern hard disk drives occupies a space of 14 nm by 75 nm. Development to make such state-of-the-art processors and hard disk drives a reality would not be possible without microscopy allowing us to have an insight into the micro- and nano-scale world. It is microscopy that has enabled progress not only of computers, but more widely in the fields of electronics, physics, material sciences, biology and medicine. Furthermore, microscopy allows us to observe and measure different physical characteristics such as size, topography, surface roughness, transparency, refractive index, local stress, color, elemental composition,

magnetic field and temperature, at the scales required by the miniaturization-obsessed world.

1.1 Scanning Probe Microscopy

Scanning Probe Microscopy (SPM) represents a distinct sub-class of microscopy techniques. Images are obtained by mechanically scanning over the sample surface in close proximity with a physical probe. This probe is usually moved in a raster-like manner, allowing the formation of a microscopic map of the required characteristics of the sample. The information is obtained electronically and then, after conversion, may be displayed in a form of a visual image.

The history of scanning microscopy started with invention of Scanning Electron Microscope (SEM) by Knoll in 1931 [8]. Since then a lot of progress has been made in the field. One of the key moments on this long journey requiring recognition is the invention of mechanically scanned probe microscopy in a form of the microtopographer by Williamson in 1967 [9]. A vertical resolution of 12.7 μm was achieved. The scans were performed in 25 parallel lines separated by 330 μm and the height was probed every 165 μm. The invention was a successor to the profilometer invented in 1933 by Abbott et al. [10].

In 1982 the Scanning Tunnelling Microscope (STM) [11] was invented by G. Binnig and H. Rohrer, who received the Nobel Prize in Physics for their invention 4 years later (joint with Ernst Ruska for his work in electron optics and designing the first electron microscope) [12]. STM uses a metal tip scanning over a conductive surface of interest. A map of topography was obtained by measuring the sample height whilst maintaining a constant tunnelling current. Since tunnel current strongly depends on the distance between the tip and the specimen such that a single atomic step changes the tunnelling current by up to 3 orders of magnitude, the vertical resolution of the STM was 0.2 Å and lateral under 10 Å. This enabled the acquisition of a 3 dimensional topographic image of surfaces on an atomic scale, which was orders of magnitude better than Scanning Electron Microscope was capable of.

Despite its amazing resolution STM has one major drawback. In order to conduct tunnelling current, the sample of interest has to be conductive. The measurement of insulators on atomic scale is not possible using an STM. As a solution to this challenge, a new type of microscope was proposed by Binnig and Quate in 1986 - the Atomic Force Microscope (AFM) [13].

1.1.1 Atomic Force Microscopy

The first AFM consisted of a diamond tip glued to a Au foil cantilever scanning over a sample surface. During scans, when an obstacle was encountered, the AFM cantilever would bend. As a system to measure the force by which the cantilever was deflected, an STM was mounted on top of the AFM cantilever. In this way tunnelling current could serve as a very sensitive cantilever deflection system capable of detecting forces as small as 10^{-15} N at room temperature.

Approximately 15 months later Binnig et al. presented atomic resolution capability of AFM [14]. At that time a conductive sample was still used - highly oriented pyrolytic graphite. Such an approach enabled direct comparison between results obtained with STM and AFM. The surface roughness obtained with STM was around 1 Å whereas the AFM provided result of just 0.2 Å. The reason for such a variation was assigned to different sensing mechanisms. Whereas AFM is sensitive to total electron density (screening), STM is sensitive to electron density of states at the Fermi level.

In this AFM setup there was no tip as such. The rectangular SiO_2 cantilever was set at an angle allowing one of its corners to act as the "sensing" element. Despite the limited reproducibility, which was dependent on the cantilever corner being sharp enough, atomic resolution was proven.

A few months later Albrecht et al. presented the first results on an AFM with the capability of scanning insulators under air ambient conditions [15]. An improvement to the tip was introduced in a form of a SiO_2 V-shape tip located at the end of the cantilever, both being in the same plane. The V-shape enabled reproduction of the previous graphite surface roughness results, as well as taking surface images of MoS_2, which were not always taken successfully using STM due to large variations of MoS_2 resistivity (up to 3 orders of magnitude).

All previously presented AFM setups used the contact mode of operation (see figure 1.1), which means that the tip is constantly in contact with the sample surface and it is the force between tip and specimen that is kept at a constant level during scans. In 1987 Martin et al. presented a new scanning mode - a non-contact mode [16]. In this mode the tip is kept between 30 to 150 Å away from the sample surface and the cantilever vibrates. The amplitude of vibrations is kept below the aforementioned range to avoid physical contact between tip and sample and to stay in the Van der Walls attractive force region. When the vibrating tip is affected by the gradient of the attractive forces between tip and sample, the resonance frequency of the cantilever changes. The attractive force gradient affects the vibrating cantilever phase and damping, which affect its amplitude of forced oscillation. This amplitude change is detected by the interferometry system

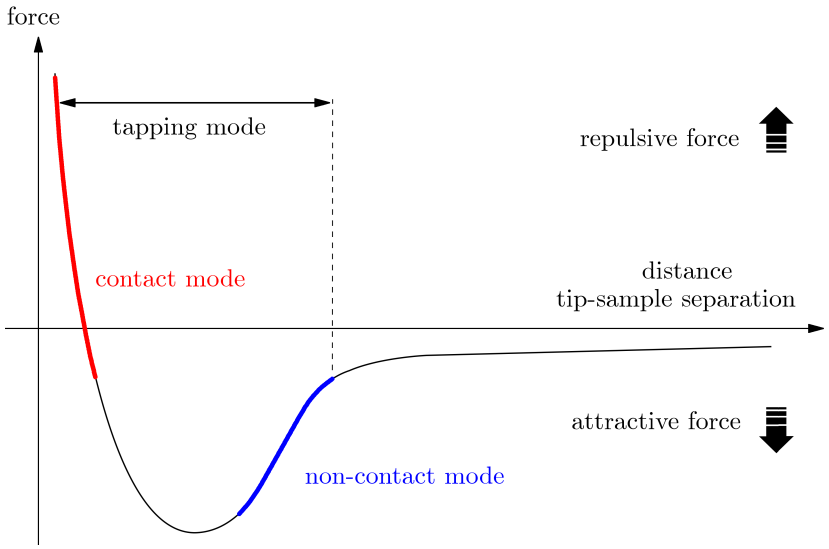


FIGURE 1.1: *Interatomic force vs. distance curve with different AFM modes of operation indicated.*

(see subsection 2.3.1) and is translated into a measurement of the sample topography. Any force gradient greater than 10^{-10} N can be recognised and the achieved spatial resolution is 50 Å. This was also the first use of an optical detection method for AFM. The method used a heterodyne interferometer which is excellent, but complicated.

In 1987 Martin et al. presented a new AFM capable of measuring magnetic properties of the specimen, the Magnetic Force Microscope (MFM) [17]. A 1000 Å thick wire (the cantilever) is bent at its end to form an L-shape (the tip). For modulation of the magnetization a 70-turns coil was wound onto the wire and then the cantilever was mounted onto a piezoelectric stage. For measuring static magnetic fields two approaches were presented, in both non-contact mode was used. The first approach is to modulate the tip magnetization with certain frequency and use the interferometry system to detect the cantilever vibrations at that frequency. The amplitude of vibrations is proportional to the strength of local magnetic field. In the second approach the magnetized tip is vibrated at a resonance frequency using a piezo transducer. When in close proximity with the sample surface, the force gradient is detected due to both the Van der Walls forces and the magnetic field. This means the scans will result in not only desired magnetic field map, but also the topography at the same time. However, using a tip with small spring constant (less than 0.1 N/m) could reduce the topography influence to less than 10% of an overall signal. The magnetic forces have longer range (than Van der Waals forces), but are weaker at closer distances. Operation at large separation emphasises magnetic contrast. The proved spatial resolution was 100 nm - the same as the wire thickness.

Another important modification to AFM setup was introduced in 1988 by Meyer et al. [18]. Instead of complicated STM or interferometry systems to detect the cantilever deflection, a simple optical laser approach was proposed (see figure 1.2). With respect to the tip, to the other side of the cantilever a square 300 μm mirror was attached. A $HeNe$ laser beam was directed at the mirror and the reflected beam was pointed at a position sensitive photodetector. Such a setup proved to be cheaper than the aforementioned systems, less sensitive to nano-particle contamination than the STM and sensitive to the cantilever displacement over a wide range of the tip-specimen spacing and frequencies. As a consequence it is almost universally used in Atomic Force Microscopes available now on the market [19].

There are commercially available AFM systems [20] which do not use optical feedback system but crystal tuning forks [21] instead. To one end of the fork there is a probe attached. This end is excited with a near resonant frequency. The other end acts as a sensing element and by monitoring its current a change in the frequency of the probing end can be detected. The crystal is a stiff material, however, the sensitivity to forces is not limited by the stiffness, but by the smallest change in resonant frequency, which in a device with high Q factor is considerable.

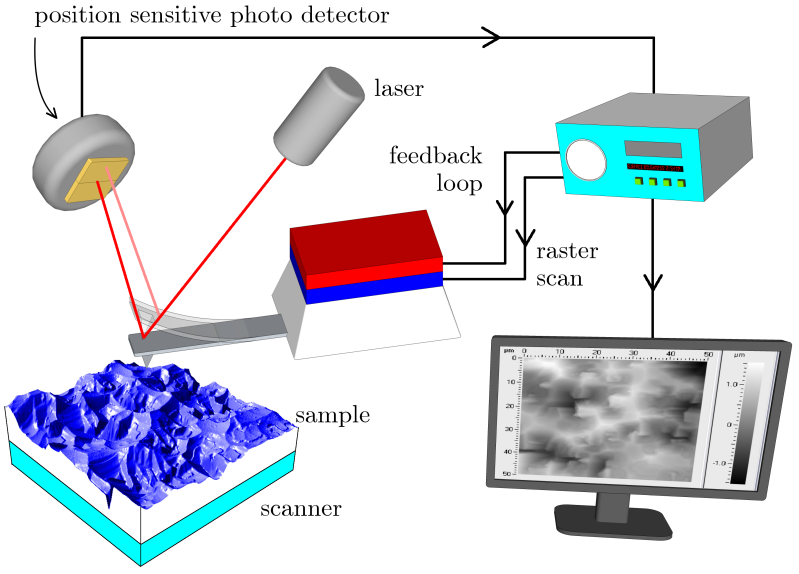


FIGURE 1.2: *Diagram presenting principle of modern AFM setup.*

In 1989 the first microfabricated Si probe made by bulk micromachining was reported by Wolter et al. [22], [23]. As presented in figure 1.3 the wafer was thinned in a KOH solution through a window (fabricated using photolithography) in a back side masking layer until a double thickness of the required cantilever was achieved. Then the front side with the cantilever was patterned and etched again in a KOH solution from both sides, until both etch fronts met and the cantilever was released. The fabrication process

of tip formation was also presented and used a similar approach. While wet etching of the Si material, a circular mask was undercut up to the moment when the underlying Si tip was unable to support it. Once it was fully underetched, the process was complete.

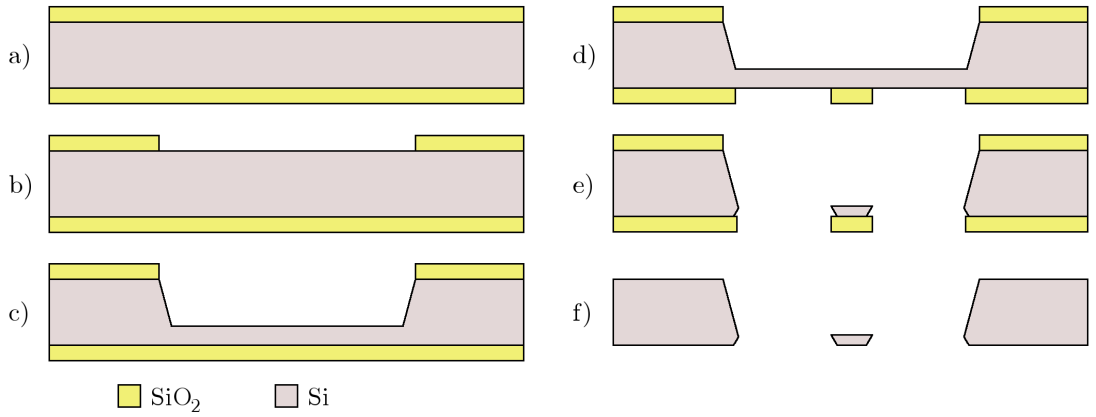


FIGURE 1.3: *Diagram presenting Si probe fabrication process proposed by Wolter:* ***a)*** *SiO_2 is thermally grown on Si wafer;* ***b)*** *by means of photolithography and an etching process, the window in the SiO_2 mask is formed;* ***c)*** *anisotropic (KOH) etch is performed to make the wafer thinner (double required thickness of the cantilever);* ***d)*** *back-side of the wafer is patterned using photolithography and the pattern is transferred into the SiO_2 layer;* ***e)*** *KOH wet etch is performed to etch through the membrane and release the cantilever;* ***f)*** *the SiO_2 is stripped from both wafer sides;*

In 1990 a fabrication process of AFM tips realised in SiO_2 and Si_3N_4 material systems was reported by Albrecht et al. [24]. The presented SiO_2 AFM probe fabrication required preparation of the sharp Si tips first. Then SiO_2 layer was thermally grown consuming the Si tip. Once the tip was fabricated, the probe body was formed by etching away the Si material in a KOH solution. The fabrication process for Si_3N_4 cantilever with pyramidal tip was more complex as presented in figure 1.4. The tip was fabricated by deposition of LPCVD Si_3N_4 on to Si substrate with a prepared pit. The cantilever design was then transferred in to the deposited layer by the means of lithography and dry etch processes. The body of the probe was made of a prepared glass plate, which was then anodically bonded. After removal of the excess of the glass plate and etching away the Si substrate, the Si_3N_4 probe was coated with metal for the deflection detector.

Until 1991 only amplitude detection systems were used as the systems for force gradient measurement in noncontact imaging. Albrecht et al. [25] presented a new, more sensitive way of doing this. The system detected not the amplitude change in the vibrations of the cantilever, but the frequency shift. The sensitivity was improved by one order of magnitude (when using cantilever with very high quality factors), without sacrificing the bandwidth and the dynamic range. It proved to be a valuable alternative to conventional systems, especially for magnetic force microscopy in vacuum.

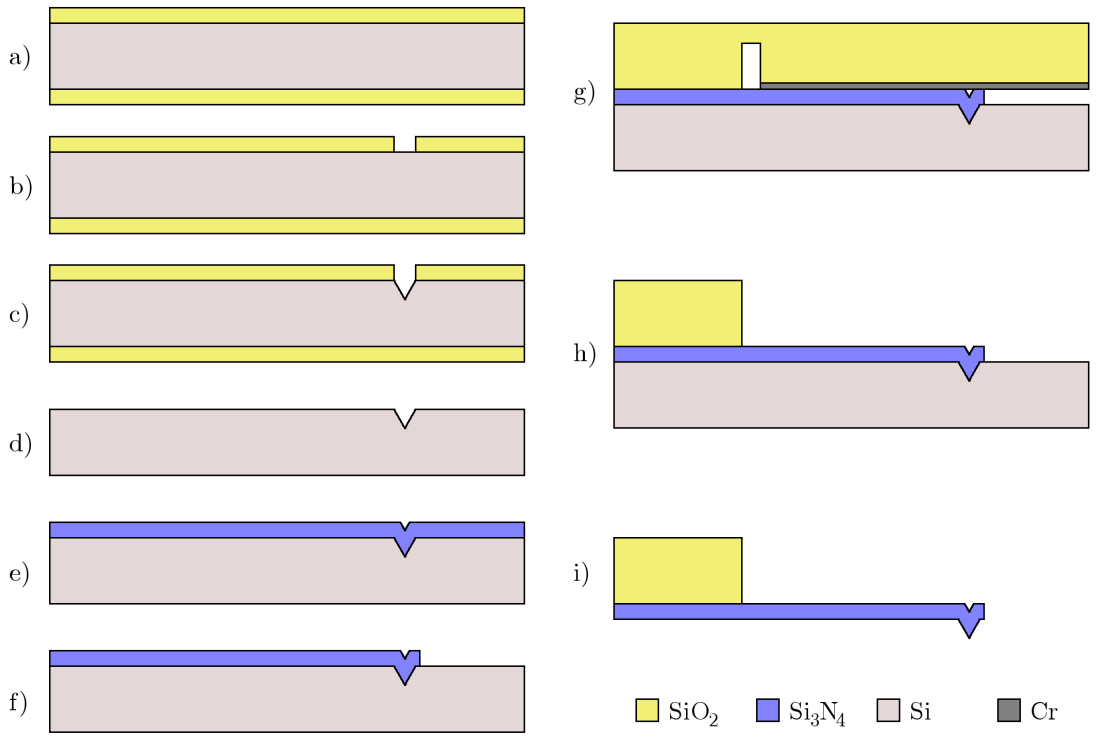


FIGURE 1.4: *Diagram presenting fabrication process of Si_3N_4 probe with tips proposed by Albrecht:* ***a)*** *on a Si wafer a SiO_2 layer is thermally grown;* ***b)*** *by using photolithography and etching process a 3 μm window is opened in the SiO_2 mask;* ***c)*** *a pyramidal pit is formed by using anisotropic etch;* ***d)*** *the SiO_2 mask is stripped;* ***e)*** *a Si_3N_4 layer is deposited;* ***f)*** *the deposited layer is shaped into the cantilever by using photolithography and etching processes;* ***g)*** *a glass plate with a saw cut and a Cr bond-inhibiting region is anodically bonded to the Si_3N_4 cantilever;* ***h)*** *by saw cutting the plate, the cantilever is exposed and the probe body is formed;* ***i)*** *the Si substrate is etched away releasing the cantilever;*

In 1992 the first Scanning Hall Probe Microscope and its performance were presented by Chang et al. [26]. The probe was fabricated in the $GaAs$ material system. The Hall bar with a spatial resolution of $0.35\ \mu m$ offered sensitivity of $0.4\ V/AT$ and a field resolution of $36\ \mu T/\sqrt{Hz}$ at $4.2\ K$. The Hall bar was fabricated on a flat chip close to one of the corners of the square sample. This corner was coated with a thin layer of gold and acted as an STM tip to control tip-sample separation. To allow easy corner access to the sample, the probe was mounted at an angle of 1^o. The smallest distance between active Hall bar area to the sample was approximately 180 nm.

In 1993 Zhong et al. presented the last, third mode of AFM operation in general use - tapping mode [27]. During scanning in contact mode of a silica optical fibre containing fragments of viscoelastic, low modulus polymer, the tip induced damage to the polymer. It was also observed that the scan resolution could be lowered by the wear put on a tip due to tip-sample interactions.

During scans of the same substrate in the non-contact mode there was found to be only a narrow range of amplitudes for which the tip was affected by the short range Van der Walls forces. Out of this range the tip was captured by the large meniscus forces, caused by capillary condensation. It was suggested that the experiment could be conducted in fluid, however, such an approach would require careful consideration of a liquid, as it could reduce polymer-sample adhesion or cause the polymer to swell.

The tapping overcame these drawbacks. The tip vibrates with frequency near the resonance frequency with large amplitudes (typically between 20 to 100 nm) when compared with the non-contact mode. The vibrating tip strikes the sample surface on every oscillation. The amplitude is set so that the tip has enough energy to overcome the stickiness of the sample surface. It was found that in comparison with contact mode, in the tapping mode the contact force is smaller and the tip wear is reduced due to time limited tip-sample contact and lack of lateral forces between tip and sample.

In 1997 Rosa-Zeiser et al. [28] presented a pulsed-force mode AFM in which during one scan not only topography was collected, but also elastic, electrostatic and adhesive sample properties. This mode was made possible by employing additional electrical circuits to sample and hold values of the measured forces whilst modulating the z position of the stage/sample. The frequency used allowed switching between contact and non-contact (with damped oscillation) mode withing a single cycle.

In summary, these are the milestones that made the AFM, what it is today. As presented in figure 1.2 the AFM tip scans the sample surface in a raster-like manner. The tip senses variations in tip-sample interactions and causes the cantilever to bend. A laser beam is reflected off the cantilever and hits a position sensitive photo detector. A change of the angle of the cantilever is sensed by the detector as a change in the position of the beam on the detector. Based on this signal the height of the probe is adjusted, which closes the feedback loop, and topographical and other data are collected and displayed.

The AFM and its successors are used in numerous areas of science such as biology [29], material sciences [30] and data storage [31]; with over 7800 articles published in 2012 [32] alone.

1.2 Magnetic field metrology

A number of ways to detect or measure magnetic field have been developed:

- SQUID - Superconducting Quantum Interference Device [33]
- MOKE - Magneto-Optic Kerr Effect [34]
- TEM - Transmission Electron Microscopy [35]

- GMR - Giant MagnetoResistance [36], [37]
- SHPM - Scanning Hall Probe Microscopy [26]
- MFM - Magnetic Force Microscopy [17]

technique	detectable mag. field $[nT]$	linearity	speed of acquisition	spatial resolution $[nm]$
SQUID	10^{-6} [38]	linear [39]	low	$3 \cdot 10^3$ [40]
MOKE	-	linear [41]	high	$1 \cdot 10^3$ [42]
TEM	10^3 [43]	-	high	$5 \cdot 10^{-3}$ [44]
GMR	200 [38]	non-linear [45]	low	13 [5]
SHPM	10^3 [46]	linear [45]	low	50 [47]
MFM	10^4 [48]	linear	low	10 [49]

TABLE 1.1: *Characteristics of different magnetic field measurement techniques.*

As indicated in table 1.1, all of the methods offer different compromises between sensitivity, magnetic resolution, linearity, spatial magnetic resolution, speed of data acquisition and sample preparation. Scanning SQUID microscopy offers excellent sensitivity, whereas the spatial magnetic resolution is limited. For MOKE, the speed of full image acquisition is high, however, its spatial spatial magnet resolution is limited by the diffraction. Out of all of the presented techniques, the TEM characterizes highest spatial magnetic resolution of 50 pm [44], but the sample prerequisite for measurement is to be thin, which normally indicates destructive sample thinning. GMR does not require special sample preparation and extends the Hall effect spatial resolution range. However, unlike SHPM, GMR suffers from non-linearity.

With the hard disk drive bit size reaching below 15 nm [5] there is a need for techniques allowing measurements of such small features. From the sensitivity and spatial resolution standpoint, the most suited technique for such application is MFM. Due to interactions between magnetic field of the sample and the tip, the sample can undergo remagnetisation, which is undesirable. Such disadvantage can be circumvented by using SHPM, which offers non-destructive measurement due to very limited magnetic field of the sensing element. The only challenge needed to overcome is to extend its spatial magnetic resolution (currently 50 nm [47]).

1.3 Hall bars and material systems

Table 1.2 presents a set of parameters for Hall bar devices realised in different material systems operating at room temperature. Within the same material system group there does not seem to be much of correlation between the current-related sensitivity S_I of

the devices as the dimensions are shrunk. Instead the results seem to be dominated by fabrication-specific effects.

Sugiyama and Sandhu both reported $GaAs$ Hall bar devices. No immediate correlation between performance of their devices can be found. This is due to the fact that the measured carrier mobility was 0.7 m^2/Vs and 0.4 m^2/Vs for Sugiyama and Sandhu, respectively, except for a device with sensitivity of $S_I = 500\ V/AT$, where carrier mobility was 0.6 m^2/Vs. Based on equations 2.20 and 2.12, there is a dependence of device sensitivity on carrier mobility and as a result these devices cannot be compared directly.

A similar case can be made for $InSb$ devices fabricated by Sandhu and Kazakova. The measured carrier mobility was 5.5 m^2/Vs and 1.3 m^2/Vs for Sandhu and Kazakova respectively. Again, the variations due to device size is of secondary importance.

In the case of the Bi devices, due to relatively long mean free path in bulk material at room temperature ($\sim$ 250 nm [50]), the mean free path in deposited thin film device is limited by grain boundary scattering, which depends on the grain size of Bi [51]. Since the grain size of deposited Bi film depends on the substrate material [52], the deposition conditions such as substrate temperature [53], aperture [54] and subsequent thermal treatments [51], the characteristics (e.g. resistance, mean free path) of the devices may vary significantly due to different device fabrication processes.

In the case of the Si diode devices, the doping of the conductive layer influences the mobility of the carriers to an extent that one order of magnitude of doping level difference can change the mobility by nearly one order of magnitude [55]. The doping level also affects the Hall scattering factor r_H, which is given by

$$r_H = \frac{R_0}{R_\infty} \tag{1.1}$$

where R_0 (R_∞) is a Hall coefficient measured at weak (strong) magnetic field [56]. In the referenced articles the doping levels are not specified and as a result no direct comparison can be made.

For Si MOSFET devices, specifying the electrical conditions, which are usually reported, does not provide a common ground for direct comparison, since the electrical behaviour of the device can be easily influenced by e.g. trapped charges (see section 4.3) and minor misalignments (see subsection 4.4.1).

What is more the device parameters will vary based on e.g. the geometric designs, used, precise fabrication techniques or machines used. That is why in order to spot any trends, one should compare devices fabricated by the same person, preferably reported within

no.	reference	material	area $[(\mu m)^2]$	S_I $[V/AT]$	I $[mA]$	B_{min} $[nT/\sqrt{Hz}]$	d $[\mu m]$
1	[57]	$GaAs$	$(5)^2$	3200	0.024	$6.3 \cdot 10^3$	1.4
2	[57]	$GaAs$	$(4)^2$	3100	–	–	1.4
3	[57]	$GaAs$	$(4)^2$	500	0.215	$6.3 \cdot 10^2$	1
4	[58]	$GaAs$	$(1.2)^2$	2600	0.002	$4.1 \cdot 10^4$	–
5	[59]	$InSb$	$(5)^2$	850	–	–	0.3
6	[60], [61], [46]	$InSb$	$(1.5)^2$	340	0.05	$8.0 \cdot 10^2$	1
7	[62]	$InSb$	$(1.5)^2$	1000	0.05	$5.0 \cdot 10^2$	0.3
8	[59]	$InSb$	$(0.6)^2$	660	0.05	$8.7 \cdot 10^2$	0.3
9	[58]	Bi	$(2.8)^2$	3.3	0.4	$3.8 \cdot 10^4$	0.07
10	[63]	Bi	$(0.75)^2$	1.2	5.2	$2.7 \cdot 10^5$	0.078
11	[64], [65]	Bi	$(0.4)^2$	0.34	0.01	$8.4 \cdot 10^5$	0.07
12	[58]	Bi	$(0.25)^2$	–	0.04	$7.2 \cdot 10^5$	–
13	[66]	Bi	$(0.12)^2$	3.3	0.04	$7.2 \cdot 10^5$	0.07
14	[47]	Bi	$(0.05)^2$	4	0.043	$8.5 \cdot 10^4$	0.06
15	[67], [68]	(p-n) Si	$(2.4)^2$	87	2	$6.0 \cdot 10^0$	1.5
16	[69]	(p-n) Si	$(2.4)^2$	180	< 8	$3.0 \cdot 10^2$	4
17	[70]	(n-MOS) Si	$(60)^2$	3700	0.01	$4.0 \cdot 10^4$	0.01[a]
18	[70]	(n-MOS) Si	$(5)^2$	300	0.01	$4.0 \cdot 10^5$	0.01[a]
19	[71]	(n-MOS) Si	50×60	400	–	$1.5 \cdot 10^2$	0.01[a]
20	[71]	(n-MOS) Si	5×6	250	–	$1.5 \cdot 10^3$	0.01[a]

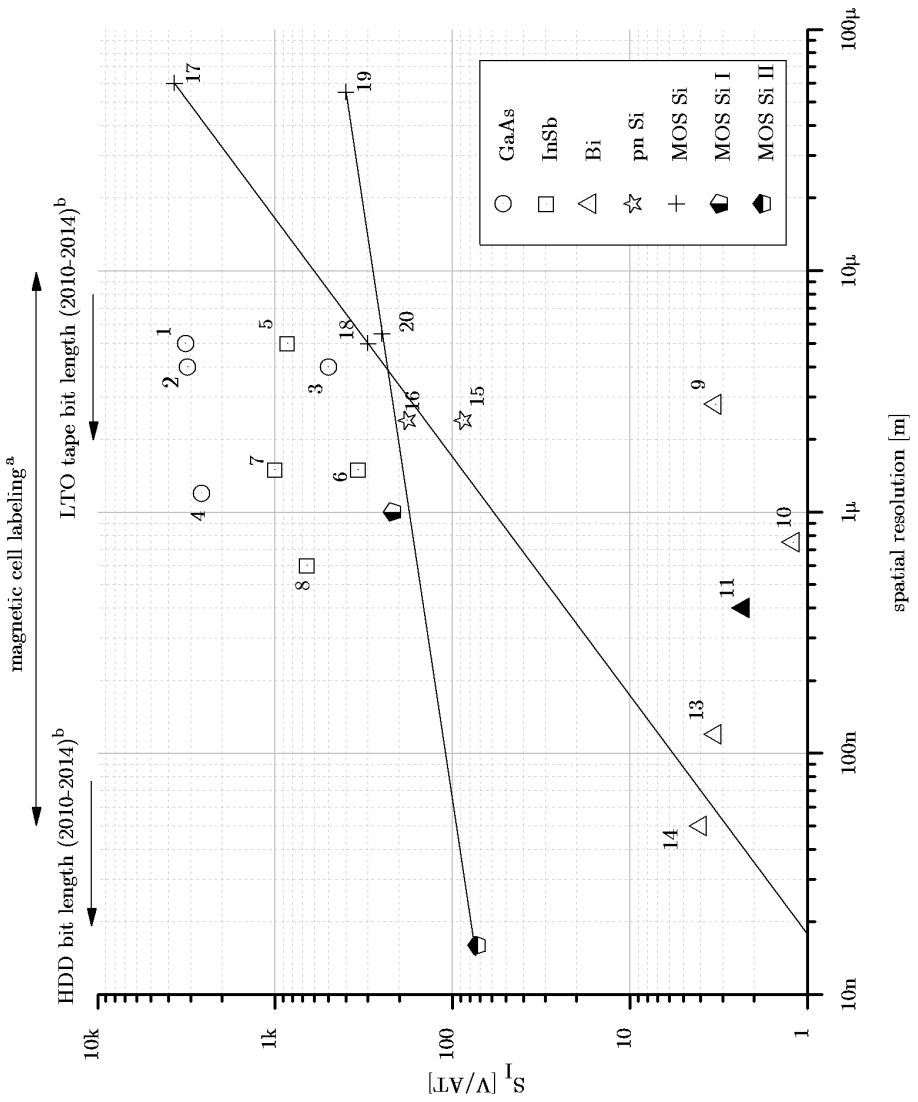
[a] [71]

TABLE 1.2: *Characteristics of some Hall bar devices operating at room temperature.*

the same article. This increases the chance that the fabrication procedure, fabrication conditions and measurement setup were not changed.

Except for [58] where the sensitivity value was not given for one of the devices, all of the references presenting more than one device ([57], apart from the device number 3 due to the different carrier mobilities, [59], [70], [71]) confirm that as the device is scaled down, its sensitivity drops. This confirms that the sensitivity is a function of the active area size within the discussed size range. As presented in [58], [70], [71] with shrinking of the device the magnetic field resolution also drops (B_{min} increases). This trend is not confirmed by the case of [57] devices number 1 and 3, where the thicknesses and the drive currents are different for the devices, which change their working conditions.

In order to achieve the highest magnetic field resolution measurements are performed at a frequency of 1 kHz, which usually puts the measurement out of the $1/f$ noise region. In this way only the thermal noise limits the magnetic field resolution. In [71] the field resolution was measured at 100 Hz and 1 kHz and the results were 400 and 150 $nT/\sqrt{(Hz)}$ respectively.

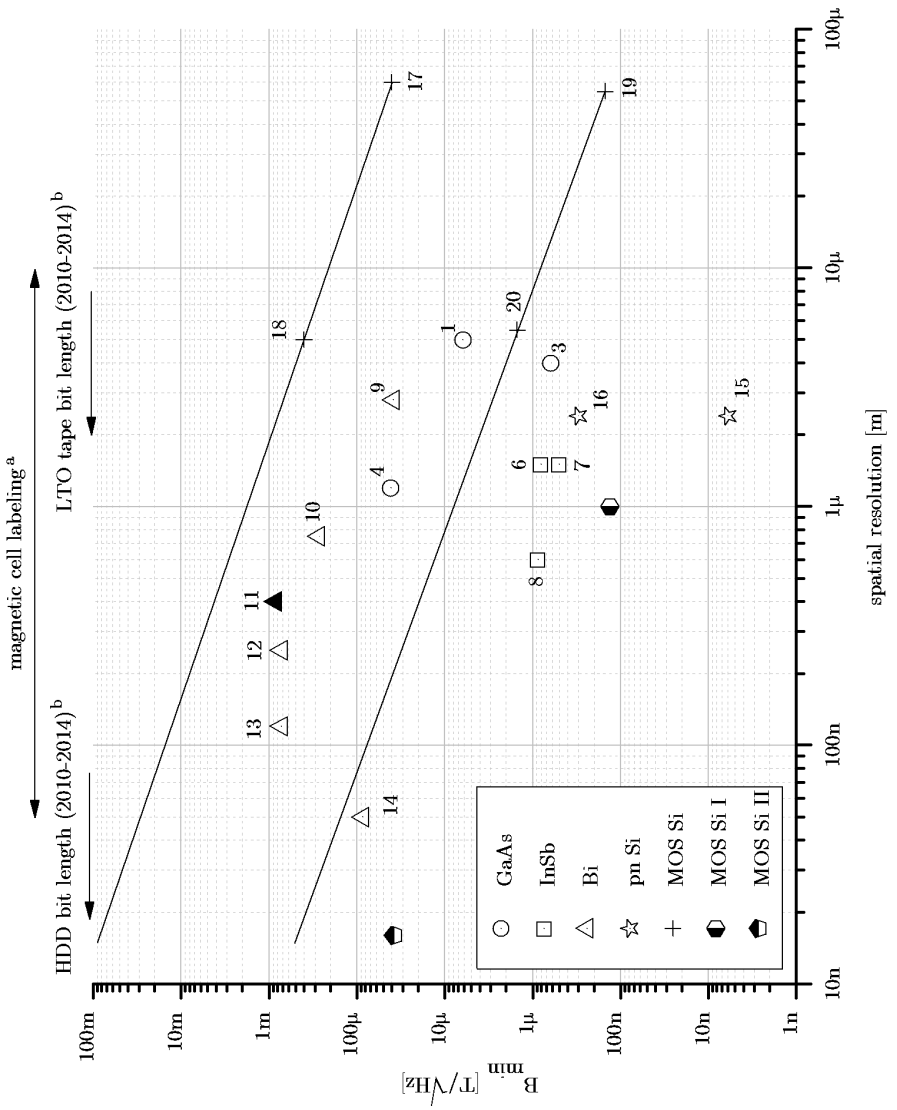


[a]data obtained from [72]
[b]data obtained from [73]

FIGURE 1.5: *Sensitivity comparison of different Hall bars operating at room temperature - graph presenting sensitivity vs. spatial resolution from data gathered in table 1.2. Full symbol corresponds to a Hall bar device fabricated on top of the AFM tip. Semi-full symbols present achievable devices according to calculations presented in subsection 2.4.1. The lines are sensitivity extrapolation of Yamaguchi and Yang device scaling down.*

In [47] Sandhu et al. presented an improvement to the spatial resolution of a Hall bar realised in the *Bi* material system. By shrinking the Hall bar square active area from 120 *nm* [66] to 50 *nm* [47], surprisingly the noise figure was improved by one order of magnitude. However, no details were presented on how this was achieved. This may have been due to the sensitive region being one grain across i.e. single crystal Hall bar.

In [63] Petit concluded that increasing the thickness of the sensing area decreases the noise level. This is in agreement with the calculations presented in subsection 2.4.1.



[a]data obtained from [72]
[b]data obtained from [73]

FIGURE 1.6: *Magnetic field resolution comparison of different Hall bars operating at room temperature - graph presenting magnetic field resolution vs. spatial resolution from data gathered in table 1.2. Full symbol corresponds to a Hall bar device fabricated on top of the AFM tip. Semi-full symbols present achievable devices according to calculations presented in subsection 2.4.1. The lines are magnetic field resolution extrapolation of Yamaguchi and Yang device scaling down.*

1.3.1 Which material to choose?

The magnetic sensitivity depends on the regime in which the device operates - which is directly linked to the size of the Hall bar. For large Hall bars - the linear drift range - the sensitivity is constant and independent of the Hall bar width and the diffusive transport of electrons takes place.

When we significantly scale it down, the device operates in the saturated velocity regime. In order to in increase the Hall bar sensitivity, while scaling the device down, increasing in the charge mobility is required. As a result high mobility materials are used like $GaAs$. In this regime the magnetic sensitivity is proportional to the device width and in terms of the transport it is quasi-ballistic.

If the device is scaled down further, the ballistic regime is entered. An electron travelling through the active area of the Hall bar can do so without scattering. In other words the device feature size is smaller than IMFP. In the case of this regime the Hall effect merges into Aharonov-Bohm effect proved in the experiment described by Umbach et al. in [74]. Two Hall bars are fabricated in Au on Si_3N_4. Each Hall bar is in 'H' configuration. To one end of the other device sensing area a loop is added. From the classical physics point of view, the devices behave in the same way, as the loop does not take part in electron transport. However, Umbach, by lowering the temperature to 40 mK, placed the inelastic mean free path in the range of the device's size. By doing so, the non-locality of electron transport became visible in the measurements, as the presence of the added loop modified the conductance of the device. This proved that for small enough (size range of order of the inelastic mean free path or smaller) devices become affected by non-local electrical properties (see figure 1.7) and the magnetic field measurements performed by Hall bar devices become unreliable because the magnetic field measurements are no longer spatially localized to the Hal bar, but depend on the magnetic field some distance away from the sensor. Thus the magnetic spatial resolution in ballistic regime will be determined by the mean free path, not the lithographic size of the Hall bar.

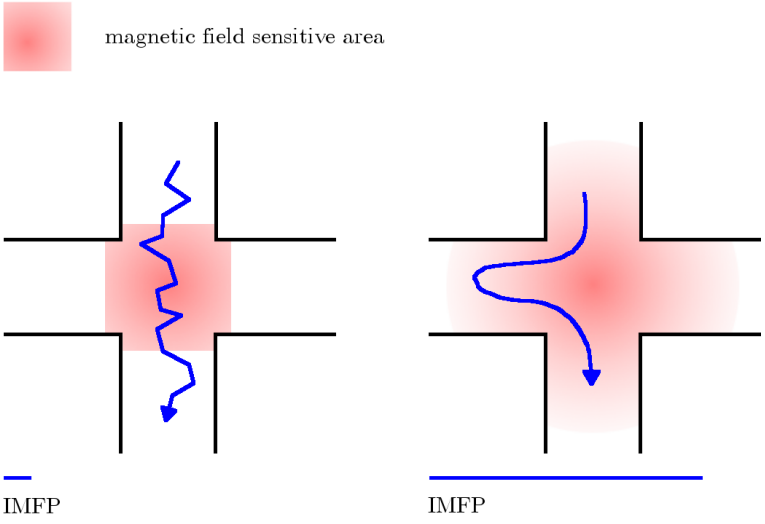


FIGURE 1.7: *Diagram presenting Hall bar areas sensitive to magnetic field depending on the length of inelastic mean free path.*

As a result in order to stay in the quasi-ballistic regime, the IMFP is the main parameter for material selection. For fabricating a Hall bar device with small feature size, a material with even shorter IMFP is required and consequently, because of the lower mobility (which translates into shorter mean free path) the p-type materials are investigated rather than n-type.

As presented in table 1.2 and figures 1.5 and 1.6 there are a few material systems that are commonly used for fabrication of the Hall bars.

GaAs Hall bars offer very high sensitivity with medium magnetic field resolution. However, it suffers from surface charge depletion effects. With scaling down the device, its resistance increases significantly and causes the working current to be very limited. This sets a limit on how small a device (spatial resolution) can be made and is still operational. This limit is in the region of 1 μm.

InSb Hall bar sensitivity is not much less than that of $GaAs$, however, it offers a better magnetic noise level.

As presented in the equations 1.2 and 1.3, high mobility translates into a long mean free path. In case of $InSb$, the IMFP at room temperature is 585 nm and 44 nm for electrons and holes respectively [75].

Bi Hall bars do not offer high sensitivity nor low magnetic noise figure. The advantage of the Bi over $III-V$ materials is that it offers the IMFP that can be modified by changing the grain size. It is possible to achieve a grain size small enough to stay above the ballistic region and still to keep the device sensitive [61].

In order to improve the spatial resolution and keeping the sensitivity reasonably high and noise low, another material system is needed.

Si Hall bars have proved to have higher magnetic sensitivity than Bi ones, as seen in table 1.2. As established, spatial resolution is is limited by the mean free path. The collision time is

$$\tau_c = \frac{\mu_h m_h^*}{q} = \frac{0.045 \cdot 0.39 \cdot 9.11 \cdot 10^{-31}}{1.6 \cdot 10^{-19}} = 0.0998\ ps \tag{1.2}$$

where $m_h^* = 0.39 m_0$ [76], and the mean free path l is equal to

$$l = v_{avg}\tau_c = 1.65 \cdot 10^5 \cdot 0.0998 \cdot 10^{-12} = 16.5\ nm \tag{1.3}$$

These calculations were done for hole mobility $\mu_h = 450cm^2/Vs$, which is true for the bulk Si material.

In order to utilize it, the device should be fabricated as a reversely polarized diode (as explained in section 2.5). However, as explained in section 2.4, in case of the inversion layer, the charge mobility is lower by 2-3 times when compared with bulk material. Lower mobility translates into a shorter IMFP which equals to between 5.5 nm and 8.3 nm. In order to achieve this, a Hall bar should be fabricated as a MOSFET transistor.

In case of the diode approach, the Hall bar device parameters (i.e. sensitivity, charge conductive layer thickness, IMFP) is set by the fabrication process, whereas in the case of the MOSFET Hall bar approach the sensitivity can be tuned by the voltage applied to the gate terminal of the transistor. The gate voltage adjusts the strong inversion layer thickness - conduction layer.

These numbers indicate that fabrication of an operational device with a feature size smaller than 50 nm (exact limitations discussed in section 4.6) should be possible. According to the calculation presented in subsection 2.4.1, the magnetic noise figure should also be better than that for the Bi Hall bars. As a result the most suitable material for achieving high spatial resolution, reasonably high sensitivity and low noise, whilst keeping the device operational, is Si. This is particularly useful as Si is easy to micromachine, when compared with $III - V$ materials, which are very brittle.

1.4 Prior Art at Glasgow

1.4.1 Functionalization of AFM

Since the invention of the AFM, the technique has been subject to significant development enabling localized measurement of different physical characteristics such as temperature [77], magnetic field [78], electrical charge [79], capacitance [80], electrochemical potential [81], near field measurement of optical field [82] and so on.

Ideally the additional sensors to quantify those characteristics are fabricated in a close proximity to the sharp AFM tips. In this way, exotic contrast is obtained at the same time as the topographical data allowing accurate measurement of the location of the image using advanced sensing on the sample, and to some extent the influence of the topography on the measured characteristics. Such a measurement may be of limited accuracy due to the lateral offset between the tip and the sensor (see figure 1.8). In other words the characteristic measurement is not obtained at the very same spot as the topography due to the lateral tip-sensor separation distance. Even if the relative tip

and sensor positions are known, the consequent variation in the sensor-sample separation may affect the measurement precision since the separation between sensor and sample depends on the height of the sample at some other point.

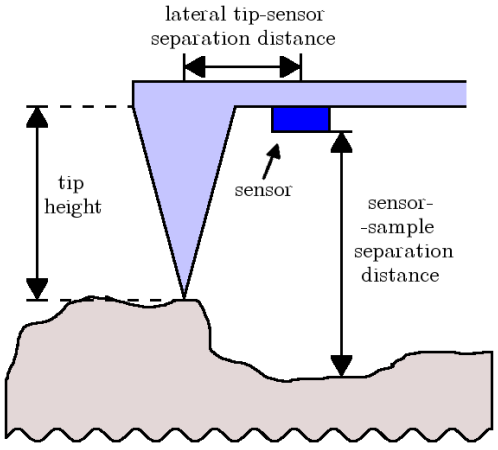


FIGURE 1.8: *Diagram presenting an AFM tip (with a sensor fabricated on the cantilever) scanning over a sample. Specific distances are indicated.*

In addition to this there is also the influence of the separation between the sensor and the sample on spatial resolution. The further away the sensor is located from the specimen, the more the measured property may spread out, effectively lowering the characteristic measurement precision. In such case having a high spatial resolution sensor does not offer any advantage since the resolution cannot be realised.

This leads to a conclusion that in order to make use of an improved spatial resolution sensor, it is necessary to bring it closer to the sample surface. Fabrication of a sensor at the apex of the flattened AFM tip has been presented several times [83], [84], [64]. The flat apex means that the resolution of the topographic AFM scan is limited (see section 4.5), however, high resolution topography information may not be of the greatest importance in the case when other physical characteristics are being measured.

The fabrication of suitable flat apex AFM tips starts with a 3" n type $< 100 >$ oriented 380 μm thick double side polished Si substrate with 40 nm of dry thermally grown SiO_2 and 60 nm of LPCVD Si_3N_4 (see figure 1.9). Using photolithography a resist mask is used for a RIE dry etch process to form a hard mask (detailed process is available in appendix B). The hard mask is used in a timed 7 molar KOH $(4:1)$ IPA wet etch process [85] at a temperature of 80 ^oC to allow the formation of the probe bodies. A similar process is then repeated on the other side of the wafer. A tip mask plate (see subsection 1.4.2) is used in the photolithography process. The unexposed areas of the resist act as a mask for a RIE dry etch process, in order to transfer the pattern into the SiO_2/Si_3N_4 hard mask. The following wet etch process is conducted to expose certain

crystallographic planes of crystalline Si as described in subsection 1.4.2. The process is performed at a lower temperature (55 ^oC) for better etch rate control.

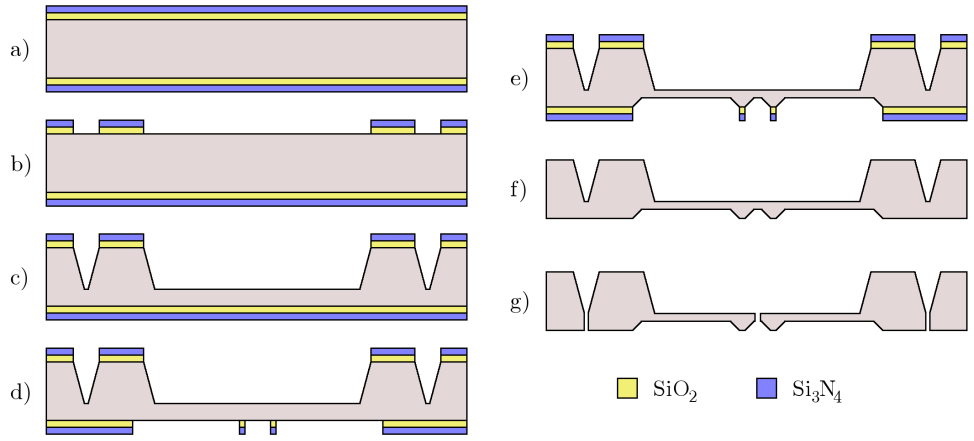


FIGURE 1.9: *Diagram presenting Si AFM tip fabrication process:* ***a)*** *lightly n − doped* (100) *oriented Si wafer coated with* SiO_2 *and* Si_3N_4*;* ***b)*** *membrane mask - windows opened in hard mask using photolithography and* C_2F_6 *reactive-ion dry etch process;* ***c)*** *membrane definition using KOH with IPA solution;* ***d)*** *tip mask - windows opened in hard mask using photolithography and* C_2F_6 *reactive-ion dry etch process;* ***e)*** *tip definition using KOH with IPA solution;* ***f)*** *mask stripping and active device fabrication;* ***g)*** *cantilever release etch using dry etch Bosch process.*

The wet etch process requires extreme temperature stability, since for 7 *molar KOH* solution at 80 ^oC the etch rate control of 1% requires temperature stability to ± 0.2 ^oC [86]. In order to obtain the most reproducible results of etching, the calibration of the wet etch kit needs to be performed. The use of approximately 7 *molar KOH* has a minimum etch rate as a function of concentration eliminating changes in the etch depth with the concentration of KOH (e.g. resulting from CO_2 absorption). Lower KOH concentrations are not recommended as sometimes the etch results in rough finish of the etched {100} planes [87].

For given etching conditions each plane has a well characterised etch rate. The timing of the etching process provides adequate control of the height of the tip. The photolithography process allows the experimenter to modify the flat apex tip size, either by modifying the mask plate design or, within a certain limit, by changing exposure time (see figure 1.10). However, the apex size can be also be influenced by changing the duration of the etching process, as this is directly linked with the undercut of the hard mask.

After the wet etch process is complete, the hard mask is stripped in 48% $unbuffered\ HF$ acid and the Si flat apex AFM tip is revealed. The Si cantilever is still trapped in the Si membrane and at this stage the fabrication process of an active sensor begins. In

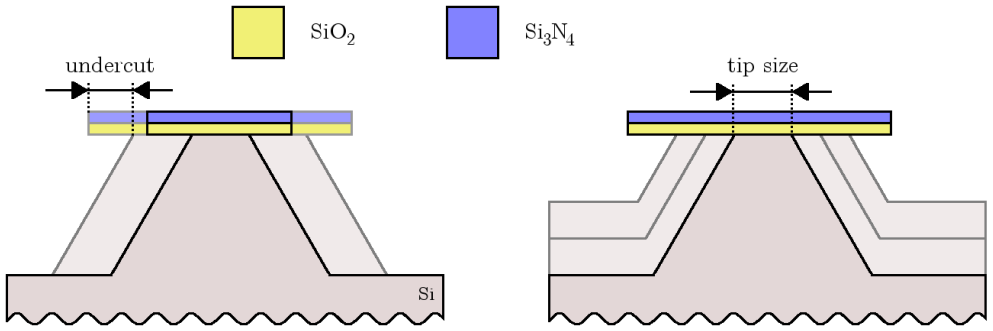


FIGURE 1.10: *Diagram presenting the influence of mask size and etching time on the tip height and the apex size of the Si AFM tip during KOH etching. On the left hand side the tip height does not change since the etching time is constant, but the mask size change influences the apex size. On the right hand side, the mask size is constant, but the etching time varies. The longer the etch, the higher the tip and the smaller the apex becomes.*

order to release the still trapped cantilever without exposing the sensitive active device to a caustic etchant, a $DRIE$ dry etch process is employed.

If necessary the process described above allows a switch in the order of the active device and cantilever release etch stages (see subsection 1.4.4). The consequence of the switch is that there is no membrane to support the cantilevers making them vulnerable to excessive bending and breaking e.g. during resist coating [65], however, such an approach may be required if e.g. the used metals are not compatible with the release etch of the cantilever.

The release etch stage can be done with a wet etch process, especially, when the active device consists of high diffusivity metals (e.g. Au). As a consequence of using such metals, the $DRIE$ dry etch process is ruled out due to a significant amount of heat being produced during etching.

The Si flat apex AFM tip fabrication process allows also the fabrication of the tips in Si_3N_4 [83] or SiO_2 [88] material systems by deposition of Si_3N_4 or thermal growth of SiO_2 on the Si tip. The cantilever shape can be then defined by the means of photolithography and RIE dry etch process, followed by etching away the remaining Si structure - cantilever release etch [88].

1.4.2 Tip design

The first sharp Si AFM tip process was reported by Wolter [23]. To fabricate the cantilevers out of the $< 100 >$ oriented Si wafer, three approaches were tested, using:

- KOH anisotropic etch with mask structures aligned parallel to the $< 110 >$ direction (indicated by the large flat of the wafer), yields a beam with {111} sidewalls;
- KOH anisotropic etch with mask structures aligned parallel to the $< 100 >$ direction, yields a beam with vertical {100} sidewalls;
- RIE dry etch with the resulting sidewalls being vertical irrespective of crystal orientation;

The fabrication of the tip was realised by KOH etching process and masking the Si material with a circular mask. Except for $< 111 >$, when compared with other etching directions, $< 100 >$ has the lowest etch rate and this encourages other directions to undercut the mask. The etching process was complete when the masking material was released. The radius of the tips proved to be lower then 100 Å.

At Glasgow, the AFM tips are realised by using {313} planes as the sidewalls. Such a selection of the planes was the result of many experiments conducted and described in [86] by Midha. It was found that {313} planes are the fastest undercutting planes, so using them as sidewalls for fabrication of AFM pyramids results in the most reproducible process for fabrication of pyramidal tips. The local maximum mask undercutting rate is located along $< 013 >$ axes, so any effects of any minor misorientation of the mask with respect to the crystallographic orientation of the substrate is minimized. As explained in subsection 1.4.1 the flat (100) apex of the AFM tip is a square area which is required for fabrication of a sensor.

In order to obtain {313} planes (see figure 1.11), the square mask pattern has to be aligned with the substrate, so that it is rotated by 26.6^o (or 63.4^o) with respect to $< 110 >$ direction, indicated by the large flat of the wafer. The appearance of the {310} planes is explained in section 3.3. A $17 - 25$ $minute$ etching process in 7 $molar$ KOH mixed by volume with $(4 : 1)$ IPA at 55 ^oC with a square mask having a side dimension of 6 μm results in a square tip apex with the side of $2 - 4$ μm. The apex size depends on the etching time, which also specifies the tip height of $4.1 - 6$ μm (for the stated conditions the etch rate in $< 100 >$ direction is approximately 240 $nm/minute$).

The angle between {313} planes and a (100) surface plane is 46.5^o, which gives reasonable aspect ratio for the AFM tip. The higher the aspect ratio, the greater the degree of specimen access, so highly topographical structures can be analysed. However, if the sidewalls are too close to the vertical, a sensor fabrication becomes impossible because of metal and resist coating of such steep sidewalls, which is relevant e.g. for fabrication of electrical connections to the sensor. A lift-off process requires evaporation of metal in order to achieve a reproducible and clean process. This is due to the fact that the metal evaporation is a directional process and as a consequence coating of nearly

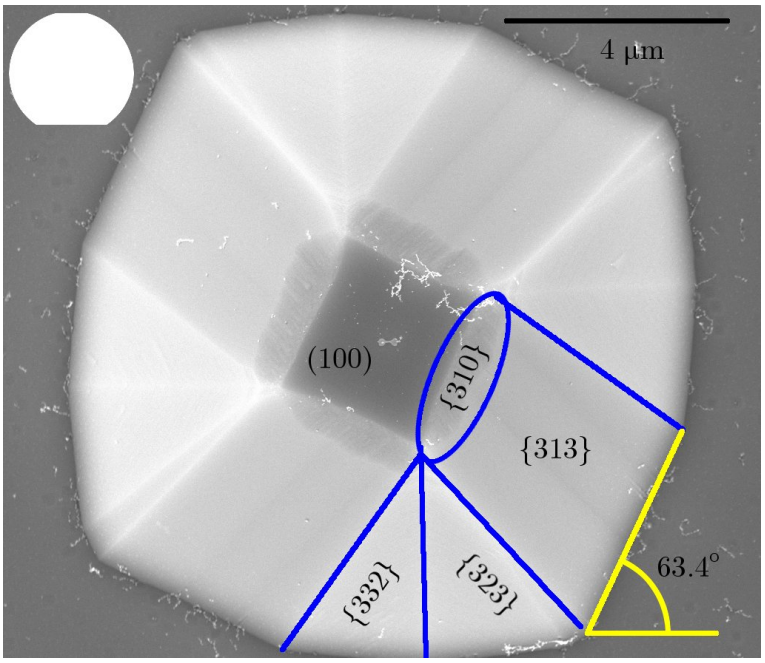


FIGURE 1.11: *SEM diagram of a Si AFM tip with indicated crystallographic planes.*

vertical sidewalls is poor. A switch from evaporation to sputtering would be needed for features with steep sidewalls. Sputtered metal can be used with the lift-off process [89], however, its success depends on the deposition rate and the sputtered metallic layer profile depends on the size of an undercut in the dual layer resist. What is more, the metallic layer thickness can be linked to the aperture (especially for small features) due to the metal clogging up the window in the resist and producing an undesired, continuous film. Such a lift-off process with a sputtered metal coating is design dependent and is not a recommended practice. In summary, the lift-off process would need to be changed to etching of the sputtered metallic layer.

Unfortunately resist coating of nearly vertical features introduces another challenge (see figure 1.12). The resist does not stick to the sidewalls completely, leaving air pockets. Such a resist behaviour does not allow design reproduction to the required level of precision, as the etchant would fill in the pockets and etch not only the areas which are expected to be etched areas but also their surroundings. This is based on assumption that the resist does not break completely due to stress caused by the surface tension of the fluids used i.e. water during coating and etchant during etching. If the resist sticks to sidewalls completely, then no lithography can be performed.

In [90] Burt et al. presented high yield batch fabrication process of sharp *Si* tips. Thanks to conditions encouraging self-sharpening of the tips during the fabrication process, the tip apex had a typical radius of curvature below 5 *nm* (without a subsequent oxide sharpening process [91]). This was achieved by using a triangular mask which allowed

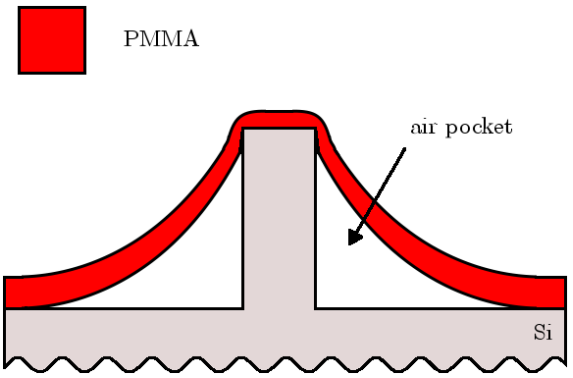


FIGURE 1.12: *Diagram presenting a feature with steep sidewalls when float-coated with PMMA resist.*

formation of a single point tip (see figure 1.13). The mask was specifically oriented in order to cause an undercut of the mask from $< 310 >$ directions. The tip is realised with the {313} planes, but the apex is formed by the steeper planes - {113}.

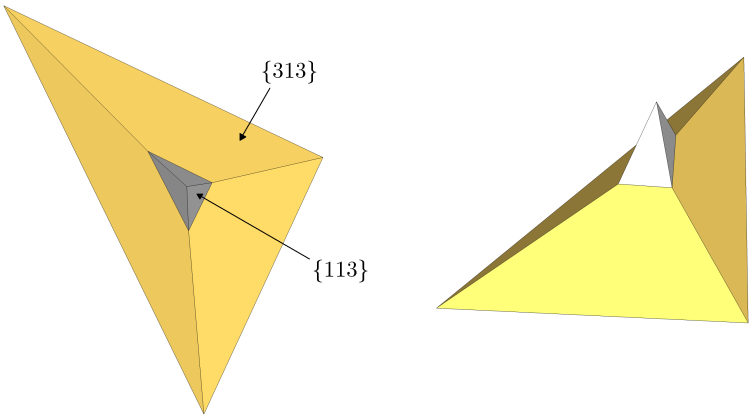


FIGURE 1.13: *Diagram presenting a triangle tip with forming it crystallographic planes (on the left top view, on the right diagonal view) [90].*

1.4.3 Diffusion

At Glasgow, there are two diffusion procedures (see figure 1.14) which can be accomplished completely on-site. Both of them use a spin-on dopant (SOD) as a source of impurities [92]. In the first approach, following application of the SOD on the sample, a resist, which is patterned in a photolithography process, is used as a mask to etch the SOD layer. In this way only the areas where the SOD was not etched are exposed to the dopant, which diffuses during the diffusion anneal. The other approach requires a hard mask - usually a layer of thermally grown SiO_2. By using photolithography and wet or dry etching processes the hard mask is patterned. After the resist mask removal by solvent cleaning, the SOD is applied and the diffusion process is performed. Finally,

after the diffusion is complete in both cases the SOD is removed with 48% HF acid followed by R.O. water rinse and blow dry.

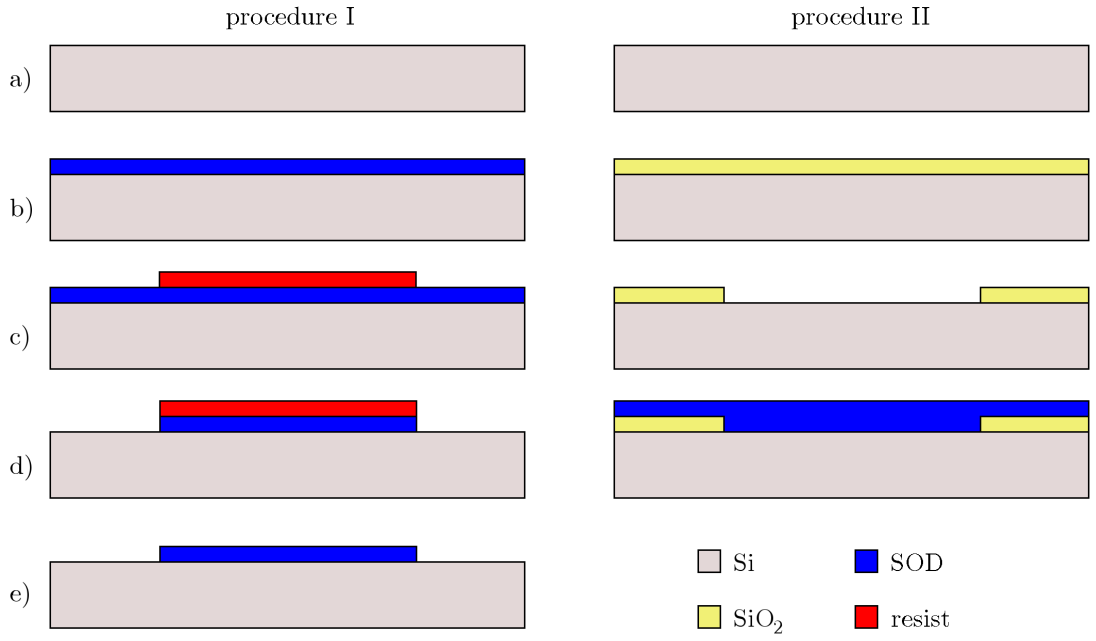


FIGURE 1.14: *Diagram presenting two processes for patterning of SOD at Glasgow.* ***Procedure I****:* ***a)*** *for a Si wafer* ***b)*** *SOD is applied by spin coating;* ***c)*** *by using a photolithography process the resist is patterned;* ***d)*** *the resist is used as a mask in a buffered HF wet etch process in order to transfer the pattern into the SOD layer;* ***e)*** *after removal of photoresist the SOD pattern remains only in area selected for doping;* ***Procedure II****:* ***a)*** *on a Si wafer* ***b)*** *the SiO_2 is thermally grown;* ***c)*** *by combining photolithography process and dry/wet etch process, the pattern is transferred in the SiO_2 hard mask;* ***d)*** *the SOD is applied by spin coating;*

The main advantage of using the second procedure is that it can offer higher spatial resolution [93]. By selecting dry over wet etching, the pattern transfer into the hard mask is closer in shape to the resist mask, due to the directionality of the dry etch process. The minimum feature size is limited mainly by the resist, whereas in case when the wet etch is used, there is a greater undercut, which can become significant for small features. For 500 nm thick thermally grown SiO_2 layer with a mask made off AZ1512 resist, the 6 : 1 buffered HF etching for 8 $minutes$ has been reported to produce an undercut of approximately 1 μm [94]. The above result implies overetching of the SiO_2 film. Assuming the etch rate of thermally grown SiO_2 in 6 : 1 BHF is approximately 80 $nm/minute$ [95], the ratio of the lateral to vertical etch rates is around 1.6. Such increase in the lateral etch rate of isotropic etch could be explained by the resist delamination [96].

It is possible to dry etch the SOD, which would improve the resolution of the features produced using the first procedure, however, this is not a recommended approach due to the possibility of contamination of the etch tool.

The SOD used is Borosilicafilm [92]. After application and before diffusion it requires additional bake at above 550^oC in an ambient containing 5% of O_2. The reason for this is that the SOD contains *polyvinyl acetate* (PVAC), which upon exposure to water (e.g. air humidity or during HF etching) binds up (cross-linking) [93], leaving a very difficult to remove contamination on the sample surface. This thermal cycle burns off the PVAC improving the process yield and sample cleanliness.

As a consequence of the need for the prebake, the first approach requires two separate thermal cycles - the prebake before the etching process and the diffusion driving the dopant. In case of the hard mask procedure, the prebake can be joined with the diffusion process to form a longer, single thermal cycle. This is convenient as it saves approximately 1 day on fabrication, as well as providing better spatial resolution.

After the diffusion anneal the sample should not be subjected to further thermal processing. An example might be thermal growth of thick oxide after a diffusion process. Such an additional thermal cycle can cause an undesired redistribution of the dopant that is already present in the sample. In order to minimize the number of high temperature cycles, thermal growth of oxide can be replaced by a PECVD SiO_2 deposition. Bhatt [97] investigated some properties (such as stress, surface roughness, etch rate) of PECVD SiO_2 films. One of the experiments involved checking if PECVD SiO_2 can be used as a diffusion mask for B. Three samples had their sheet resistances measured and then were coated with 0.5 μm, 1 μm and 1.5 μm of SiO_2. Each sample was then half immersed in HF acid to etch the deposited films. In this way only half of each sample was masked with SiO_2. After diffusion (the process was performed on all of the samples simultaneously from the solid source for 1 *hour* at 1050^oC), the oxides were stripped and the sheet resistances were remeasured. Comparison of measurement results revealed that even the thinnest PECVD SiO_2 proved to be successful in masking the dopant from reaching the sample.

Therefore, based on the Bhatt experience it was decided to use PECVD SiO_2 film as a hard mask for a diffusion process in this project.

1.4.4 Work of B. K. Chong

From 1997 to 2001 Chong worked on building Scanning Hall Probe Microscope probes for operation at room temperature [65].

The AFM probes were realised in Si material system using KOH bulk micromachining, dry etching and photolithography processes. The AFM tips were formed by a 20 μm high pyramid with flat apex (square area $1 - 2.5$ μm). Since the Hall sensor was to

be fabricated in Bi, a reactive, low melting point material, macromachining had to be complete before sensor definition. Therefore, once the whole AFM probe was ready and the cantilever was released, the probe was coated with an insulator - 500 nm of PECVD Si_3N_4 - and the Hall bars were fabricated on top of the flat AFM tips. The application of resist on such a high structure as the AFM tip required using $PMMA$ float coating method (see subsection 2.2). It was found that resist application by float coating needed for definition of the sensor put stress on the cantilever and made it break. Additional supporting structures were incorporated into the probe design to overcome this challenge. Nevertheless, deposition of resist on free space was a continuing problem for this technique.

The sensing elements were made of evaporate Bi with spatial resolution ranging from 400 nm to 50 nm with lithographic definition accomplished by the use of lift-off. The leads and pads to provide electrical connections to/from the sensor were made of 5 nm of $NiCr$ and 50 nm of Au, which were overlaid by the Bi sensor film. The performance of the 400 nm Hall bar was measured. The characteristic parameters are presented and compared with other devices in section 1.3.

Multiple Hall bar devices were also fabricated on a common AFM tip. Having two Hall bar devices located at close proximity to each other confers certain advantages. Two measurements can be obtained during just one scan and comparison of the results can verify the accuracy of readings. What is more, differential field strength measurements at fixed Hall bar separation distances can be acquired. If one of the leads used for sensing the Hall voltage gets damaged, the probe remains at least partially operational. Having a more complex design does not affect the number of fabrication steps, which is convenient as the probes are fragile and the yield of functional devices was low.

Chong also fabricated a single turn $NiCr - Au$ coil located at the AFM tip allowing to use in a Scanning Electromagnetic Force Microscope [65]. The coils were fabricated using the same fabrication techniques. There was a change in the order of fabrication steps. By moving the KOH release etch to the end of the fabrication process, the sample was made stronger and no cantilever failure was observed. This was possible as the Au coil was compatible with KOH release etch, unlike the Bi Hall element.

Au was used as the conductive material for the coil due to its high conductance and corrosion free property. The coils were fabricated with diameters as small as 270 nm, however, only the 0.7 μm coil was tested and proved to work as the imaging tool. Due to low inductance such a coil could potentially deliver very fast (0.1 ns) and high field (1 T, high current) external magnetic field pulses, which could have been used to modify the specimen magnetization. This functionality was not tested, however, due to the severe capacitive loading of the pulses by the pad capacitance (approximately 35 pF).

There were attempts to fabricate a coil next to a Hall bar device. In this way the coil would be able to magnetise the specimen by passing a current through and the Hall bar image the magnetic field. Such a combination of the two devices would practically form a "magnetic laboratory" on a tip. No fully functional probe of this kind was fabricated.

1.5 Motivation and research goals

This project is focused on developing a technology capable of delivering a Hall bar sensor on an Atomic Force Microscope tip in order to investigate magnetic properties of specimen with high spatial resolution. The Hall bar magnetometer studies presented in section 1.3 showed that there is a compromise between spatial and magnetic field resolution. The sensitivity calculation presented in subsection 2.4.1 indicate that the magnetic sensitivity of Si should be higher than that of Bi, although, still much less than one of $III-V$ materials. The $III-V$ materials suffer from difficult micromachining processing and fragility as well as limited current when scaling down due to surface charge depletion. At low temperatures the long mean free path of $III-V$ high mobility probes results in significantly degraded spatial resolution (see section 4.6).

The Scanning Hall Probe Microscope has certain advantages over other Scanning Magnetic Microscope techniques. Unlike the MFM, the Hall bar magnetometer during operation generates negligible field at the inspected magnetic structure, so the SHPM is highly non-invasive. Even though the SHPM does not offer the speed and scanning area size of the Kerr microscope, the achievable spatial resolution is much higher. Unlike the TEM, the specimen requires no preparation allowing operation on solid, thick samples. It provides quantitative information about the magnetic field with the detectable range from 1 μT to 100 T [98] and is suitable for study of soft as well as hard magnetic materials.

Published SHPM instruments usually control the probe-specimen separation using STM [26], [58] or AFM in the contact regime [69], [70]. The reason for this is that the sensor is placed away from the tip. The sensor-specimen separation distance is constant and dependent on the design. In case of Chong's work, the sensing area of the Hall bar was placed at the apex of the AFM tip. In order to protect the sensor from wear the microscope was operated in the non-contact AFM mode. By varying the scanning height the sensor-specimen separation distance was precisely controlled. By using Bi Hall bar device the system could perform measurements at very close proximity. In case of the Si MOSFET Hall bar, the minimum sensor-sample distance would be slightly greater than in case of Chong due to gate SiO_2, metallization and optional passivation layer thicknesses. However, this still leaves the sensor in the close proximity range, bearing in

mind the relatively large tip-sample separation distance in non-contact mode for blunt AFM tips ($5 - 100\ nm$).

The goals of this project were:

- to develop a reliable and reproducible MOSFET transistor fabrication process on AFM tip for magnetic applications
- to develop a scanning Hall probe for a SHPM

The main challenge is to fabricate the MOSFET on the AFM tip, which requires:

- lithography process on highly topographic structures
- doping of specific areas on highly topographic structures
- making sure all materials and processes are compatible

1.6 Fundamental design choices

Before starting the fabrication process for this project, some design choice had to be made and some fabrication limitations had to be recognised. AFM probes are fragile and have to be handled with care [65]. Consequently, the number of fabrication steps in this project is kept to minimum. In order to increase the robustness of the probes in the wafer, the cantilever release etch is moved to the very end of the process. In this way during sensor fabrication each cantilever is still a part of a membrane surrounding and supporting the probe body. The membrane thickness is under 10 μm (the thickness of the cantilever) and from the wafer handling point of view probably it made no difference. However, application of the resist did not require any redesign to include extra supporting structures and allowed the use of spun layers of resist for areas of the sample remote from the tips, unlike the method of Chong.

Fragility of the wafer introduces another important limitation. Doping required for sensor fabrication has to be performed on-site, due to the difficulty of transporting wafers to an implanter, and difficulty of developing the safe handling techniques at an external service provider. At Glasgow, no ion implantation is performed. Doping has to be done by a thermal process from a spin-on dopant, which proved to be problematic to control (see subsection 4.1.4).

By keeping the entire fabrication process on-site, the number of metals available is limited as well. This is a relaxed constraint due to a selection of metals (Au, Ti, Al, Ni, $NiCr$, Ag, Pt) being available, however, the fabrication of a transistor on AFM tip is

meant to be for a magnetic field sensor that produces negligible external magnetic field so as not to affect the sample magnetization. This means that the probe and ultimately the microscope cannot be fabricated using magnetic materials. This translates into the material list: Au, Ti, Al, Ag, Pt. In order to keep the fabrication process compatible with CMOS technology for potential future applications, Al is chosen as the probe metallization.

One more constraint is introduced by the AFM tips and device fabrication on the apex. Lithography on features with such large height variations becomes challenging due to resist coverage issues (see subsection 2.2). At Glasgow, there are two ways to provide good coverage of resist on highly topographic structures. One method is to use a thick layer of resist to completely cover the features in question. The thickness of the resist affects the achievable resolution in the lithography process. In order to achieve feature size in the range of $10's\ nm$, this method is not useful. In this project this approach was, however, successfully used in a photolithography process to form a mask for the cantilever release dry etch at the end of the fabrication process. The other approach is to use a "float coating" technique [99], which uses $PMMA$ as a high resolution electron beam resist. Unlike the previous method this provides locally uniform coating. Wrinkles in the resist layer occur, however, when comparing the area of the wrinkles and the writing area, the risk of a wrinkle being located on the tip is very low since the resist film is under significant tensile stress as it is draped over the tip. Eventually this technique proved to work for the transistor fabrication on an AFM tip.

To summarize the lithography subject, contact photolithography is used in this project for large features (from 2 μm and up), which translates into all work related to MEMS fabrication of AFM probes. For any smaller features electron beam lithography is used. The pads (and even the leads) are large enough to fit in the photolithography process, however, this would introduce a number of additional fabrication steps (see figure 1.15), which does not comply with the aforementioned constraint of limiting them. The whole active device is fabricated solely using e-beam lithography.

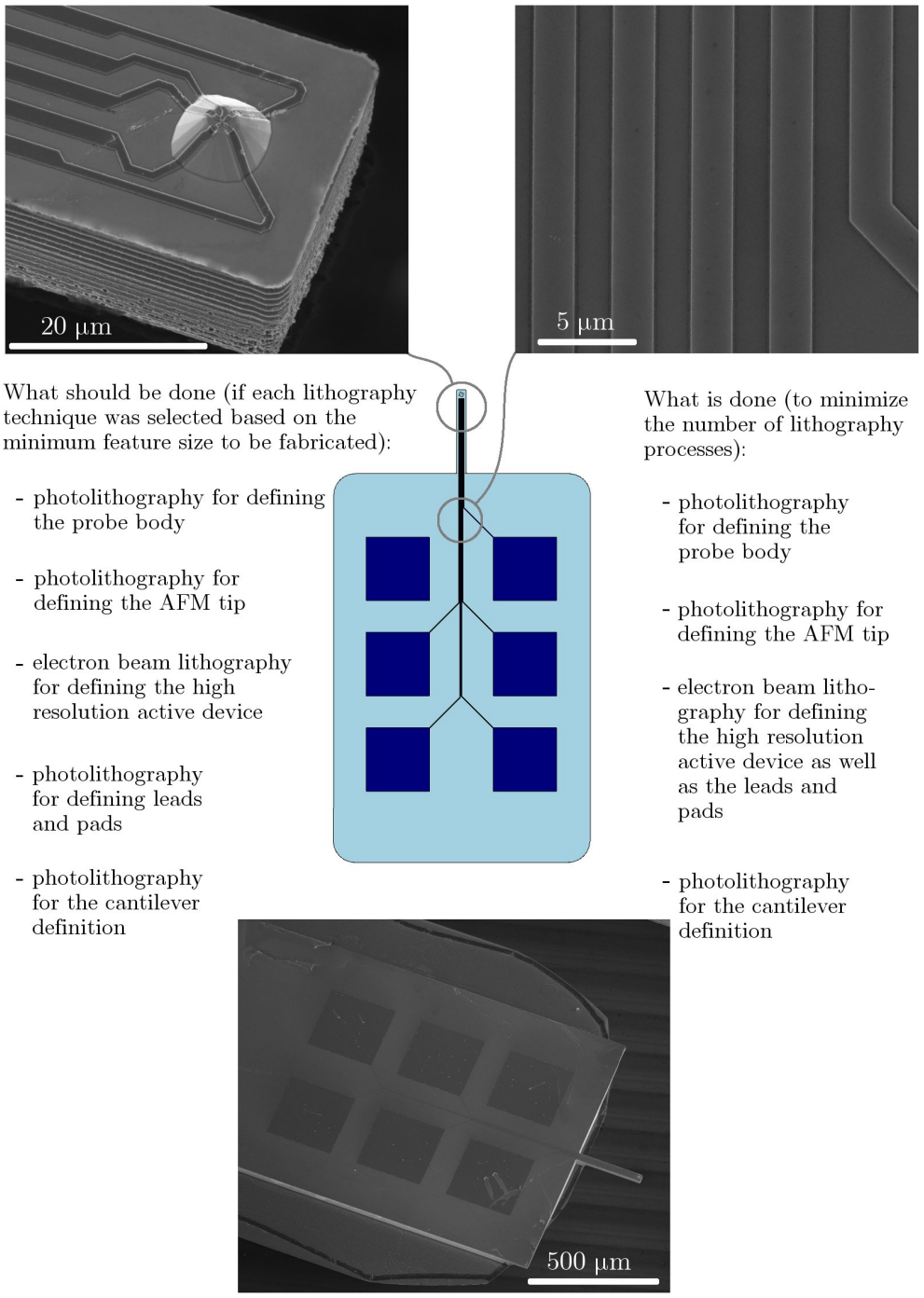


FIGURE 1.15: *Diagram presenting probe body and SEM diagrams of its specific elements (active device located on the AFM tip in the top left hand corner,* 150 *nm thick Al leads in the top right hand corner, probe body and* 150 *nm thick Al pads). Explanation of the lithography stages is given. On the left hand side lithography stages are presented in order if the lithography techniques were chosen based on the minimum feature size. On the right hand side the stages are presented in order how they are performed.*

Chapter 2

Background

2.1 Diffusion

In electronics diffusion is a standard fabrication thermal process to change the properties of surface layer of substrate material by the incorporation of other materials. High temperature allows for thermally actuated motion of impurities, located at/on the surface, deeper into the material. Diffusion is used in CMOS technology for the formation of the $p-$ and $n-wells$ needed for combining $p-$ and $n-type$ MOSFET transistors on a single substrate as well as for the fabrication of highly doped regions for formation of ohmic contacts. In this project the formation of ohmic contacts is required for the production of a standard MOSFET transistor.

There are a number of ways to introduce impurities into a substrate, all of which are well-established processes. The most common ones, except for ion-implantation, are [100]:

- diffusion source in a vapour form at high temperatures
- diffusion from a doped oxide layer

The differences between diffusion from a constant surface concentration and ion implantation followed with annealing are presented in table 2.1. In order to predict a doping profile of diffusion performed from a vapour or solid source, there are two models [100] used: constant surface concentration (CSC) and constant total dopant (CTD). In the first model impurity atoms are transported from a vapour source onto the semiconductor surface and diffused into the semiconductor wafer. The vapour source maintains a constant surface concentration of dopant during the entire diffusion time. This model is

described by the equation:

$$C(x,t) = C_s \; erfc(\frac{x}{2\sqrt{Dt}}) \tag{2.1}$$

where

- $C(x,t)$ $[atoms/cm^3]$ is the concentration level at a depth x $[cm]$ and time t $[s]$ measured from the start of the diffusion process
- C_s $[atoms/cm^3]$ is the surface concentration
- D $[cm^2/s]$ is diffusivity calculated by the equation

$$D = D_0 \; exp(-\frac{E_A}{kT}) \tag{2.2}$$

where

- D_0 $[cm^2/s]$ is the theoretical diffusivity of impurity in the substrate at infinite temperature
- E_A $[eV]$ is the activation energy
- k $[eV/K]$ is the Boltzmann constant
- T $[K]$ is temperature

In case of constant total dopant, a fixed amount of dopant is deposited onto the semiconductor surface and is subsequently diffused into the wafer. The profile resulting from this process is given by the equation:

$$C(x,t) = \frac{Q_T}{\sqrt{\pi Dt}} \; exp(-\frac{x^2}{4Dt}) \tag{2.3}$$

where Q_T $[atoms/cm^2]$ is the total surface impurity concentration.

By using the above equations (equations 2.1, 2.2, 2.3), the profiles of B impurities in a Si substrate for two different diffusion times and models are presented in figure 2.1.

The resulting profiles for the same parameters ($C_s = 5 \times 10^{20}$ and $Q_T = 6.3 \times 10^{13}$) used for the two models are similar in shape. The main difference is with the surface concentration, which differs by more than 1 order of magnitude (see table 2.1).

The ohmic contacts in a CMOS process are formed to Si with doping of 10^{19} $atoms/cm^3$ [100]. Having even higher doping (by a factor of 10) at the surface does not affect the ohmic contact formation. The diffusion depth has to be carefully designed. If the diffusion is for example 1 μm deep than the corresponding lateral diffusion is approximately $750-850$ nm [102]. For a transistor with a gate length of 1.35 μm, such lateral diffusion

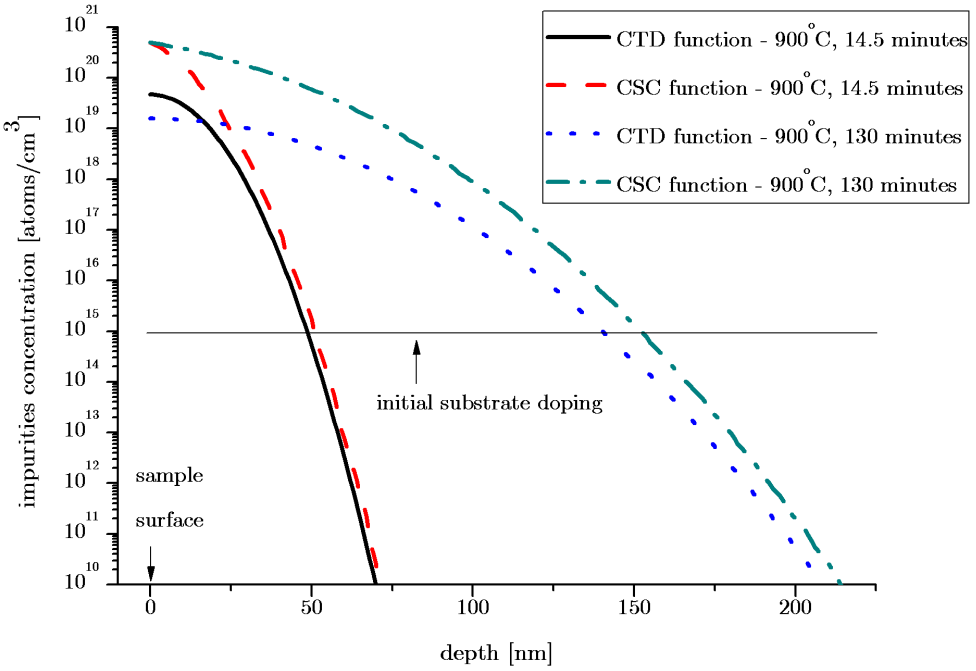


FIGURE 2.1: *Different doping profiles of B in Si substrate for two different diffusion times and models (Constant Total Dopant and Constant Surface Concentration). Profile calculations based on [101].*

imp.	temp.	time	CSC surface conc.	CSC junction depth	CTD surface conc.	CTD junction depth	junction depth error
	$[^oC]$	$[min]$	$[atoms/cm^3]$	$[nm]$	$[atoms/cm^3]$	$[nm]$	%
B	900	14.5	5×10^{20}	50	4.7×10^{19}	48	4
B	900	130	5×10^{20}	150	1.6×10^{19}	140	6.7
P	900	6.3	5×10^{20}	50	4.7×10^{19}	48	4
P	900	100	5×10^{20}	200	1.2×10^{19}	180	10
B	1050	100	5×10^{20}	1000	2.3×10^{18}	800	20
B	1050	4	5×10^{20}	200	1.1×10^{19}	180	10

TABLE 2.1: *Table presenting surface concentrations and junction depths for the two models (Constant Surface Concentration and Constant Total Dopant), different impurities, different diffusion temperatures and times. Calculation based on [101].*

is unacceptable because the source and drain highly doped regions would merge. Such a transistor does not fully switch off and there is no voltage control of the channel thickness. In contrast, a relatively shallow diffusion (for example 50 nm) leaves very little margin for overetching the SiO_2 layer when opening windows for ohmic contacts.

Considering this, the diffusion depth was designed to be 200 nm. Such a diffusion depth results in approximately 160 nm lateral diffusion, which does not affect the transistor performance, and leaves approximately 75 nm as an overetch margin. Even at a maximum overetch, the surface concentration is high enough to form good ohmic contact

with Al.

For shallow diffusions (below 200 nm) both models can be used as an approximation of the dopant equilibrium depth as they differ by no more than 10%. Both models provide high enough doping concentration at the surface for ohmic contact formation.

2.2 Float coating

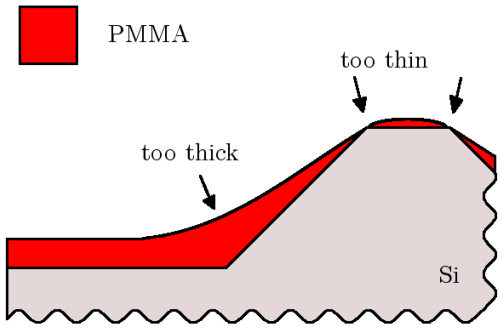


FIGURE 2.2: *Diagram presenting the tendency of spin-coated resist to become unacceptably thin when passing over an apex edge.*

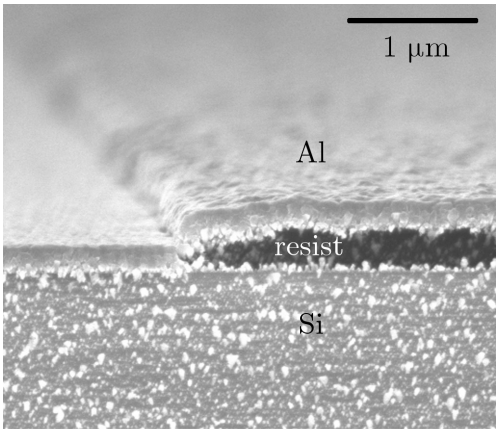


FIGURE 2.3: *SEM diagram illustrating a problem with the resist thickness during lift-off technique. The metallic film forms a continuous layer leaving no gap for the solvent to penetrate and dissolve the resist. Also, even if the resist does dissolve, the metal film is solid and stays in place.*

There is a limited number of ways to apply a resist used for a lithography process. Spin coating is the most common and it is the main method of resist application used at University of Glasgow. Spin coating provides good uniformity and control of resist thickness across a flat substrate. Unfortunately, when dealing with substrates which have strong topographic variations, the thickness of the applied film will be subject to strong local variations in thickness (see figure 2.2). In the case of PMMA resist spun on convex features, at the edges of such features the resist becomes unacceptably thin regardless of the spin speed or resist concentration. This becomes a major concern when the lack of a continuous resist film can render the device inoperable, for example when lifting off metal films (see figure 2.3) or using a dry etch process with low selectivity against resist erosion (eg. C_2F_6, flow rate 20 $sccm$, pressure 30 $mTorr$, power 100 W, selectivity of Si_3N_4 over photoresist 1 : 1 [103]). Another method of a PMMA resist application, called "float-coating", was invented and developed at Glasgow by Zhou et

al. [99] and this technique solves the coverage issue and enables formation of a proper resist thickness and profile needed for the lift-off (see figure 2.4).

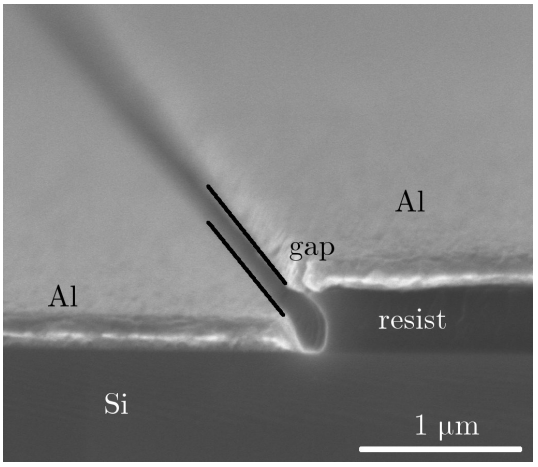


FIGURE 2.4: *SEM diagram presenting a good resist structure (rule of thumb: resist thickness = 2 · metal thickness) and resist profile (an undercut) allowing fabrication of discontinuous metallic films for lift-off.*

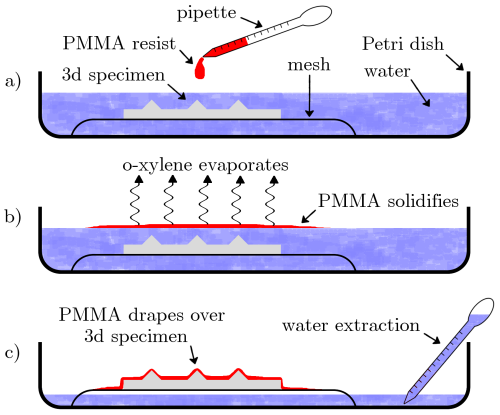


FIGURE 2.5: *Float coating technique:* ***a)*** *a drop of a PMMA resist is dropped onto the water surface and spreads rapidly over the surface;* ***b)*** *o-xylene solvent evaporates and the resist solidifies;* ***c)*** *water is removed and the solid resist film drapes over the sample.*

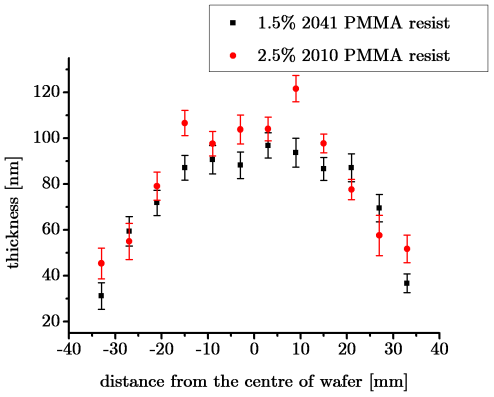


FIGURE 2.6: *Plot of thicknesses of* 1.5% 2041 *and* 2.5% 2010 *float coated PMMA resists.*

The technique is illustrated in figure 2.5. The substrate to be coated is placed on a metallic mesh stand in a Petri dish. After filling the dish with R.O. water, with the substrate fully submerged, a single drop of PMMA resist is released using a pipette onto the water directly above the substrate (see figure 2.5a). The PMMA drop spreads out on the water like oil. In a few minutes the PMMA film solidifies as the o-xylene solvent evaporates, leaving a thin continuous plastic film floating on the water surface (see figure 2.5b). By using a pipette or a syringe the water is then gently removed from

the dish. As the water is pumped out, the solid film is lowered down to the substrate until they meet (see figure 2.5c). The water remaining between the substrate and the resist film lubricates the resist-substrate contact and allows the resist to drape over the tip. The trapped water is then evaporated in an oven at 180 ^oC for 25 *minutes*, which aids adhesion of the resist to the substrate.

Multiple layers of PMMA resist can be float coated on top of each other with a subsequent oven bake after each layer. Such a procedure allows resist to be built up to the thickness needed, for example for metallization using a lift-off technique. Different molecular weights and different concentrations of PMMA resists can be used to obtain a resist bilayer, which is required for obtaining the resist undercut needed for a clean lift-off process.

The float coating technique is not free from imperfections. During the solvent evaporation in the resist film wrinkles appear. Such wrinkles collapse and in this way the resist thickness is tripled locally (see figure 2.7). As a consequence this technique is not suitable for high density patterns consisting of small features, which are particularly susceptible to variations in the lithography process due to the aforementioned resist thickness variation.

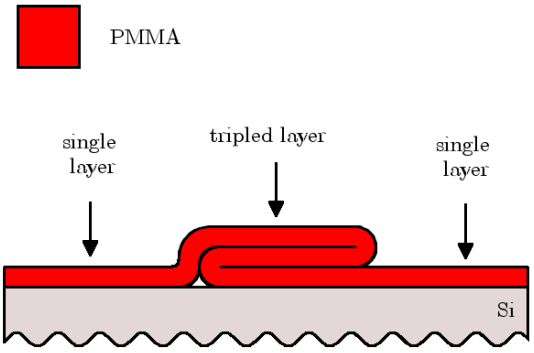


FIGURE 2.7: *Diagram presenting locally tripled resist thickness due to wrinkles in the float-coated PMMA resist.*

Moreover, the solidified resist film is very fragile. Overstressing of the film during the wafer transport leads to cracks and as a consequence the sample will not be completely coated. Excessive stress can be avoided or at least minimized by delicate handling of the sample between the coating and trapped water evaporation steps.

Another problem is that the float coating technique provides a globally non-uniform coating across the 3" wafer (see figure 2.6). The results were obtained by float coating two 3" wafers with 1.5% 2041 and 2.5% 2010 PMMA resist respectively. After 30 minute bake in a 180^oC oven, each sample was patterned with a series of 2 *mm* square windows spaced 6 *mm* apart across the substrate using electron beam with an exposure

beam current of 128 nA, resolution of 1 nm, variable resolution unit of 35 and dose of 1000 $\mu C \cdot cm^{-2}$. Development of the exposed features was performed in IPA:MiBK (2.5 : 1) at 23^oC for 30 s, followed by a rinse in IPA and N_2 blow dry. After development the resist residues [104] were removed by 40 W O_2 ash for 30 s. Each sample was then measured to determine the float coated resist thickness using a Veeco Dektak 6M Profiler with a 12.5 μm tip radius.

It was found that a single layer of float coating of 2.5% 2010 PMMA resist results in a resist thickness of 120 nm in the centre where the drop was placed. Towards the edge of the 3" wafer the resist thickness drops to 45 nm. For 1.5% 2041 PMMA resist these numbers are 100 nm and 30 nm respectively. Having a uniform resist thickness is preferable as it allows the dose, the achievable resolution and the lift-off profile to be kept constant across the whole substrate.

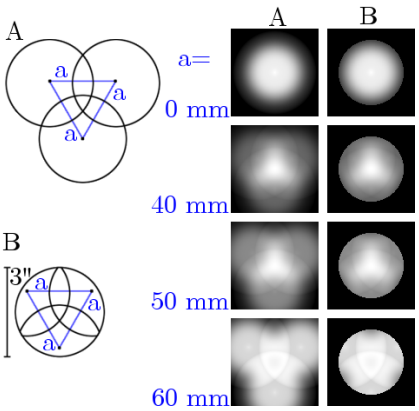


FIGURE 2.8: *The two diagram on the left explain what is presented in each column. Each circle represents one float coating layer of resist. The triangle is to indicate equal separation between central points of the 3 resist layers. Diagram B is the same as diagram A, but cropped to fit the area of* 3" *wafer. Finally column A presents modelled results of 3-layered resist thickness variation depending on the separation a between central points of each layer. Column B presents the the same results but cropped to fit the* 3" *wafer. The brighter the whole modelled* 3" *wafer area, the more uniform the resist thickness is.*

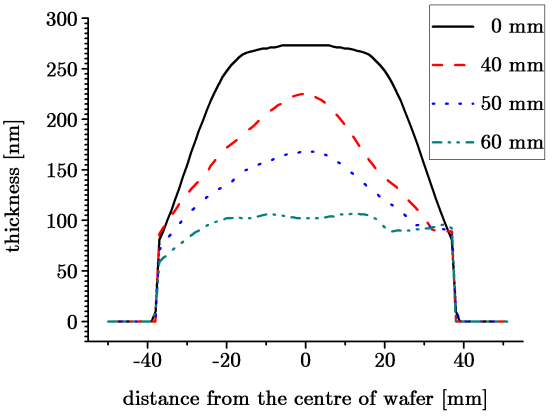


FIGURE 2.9: *Modelled PMMA resist (three float coated layers) profiles for different distances between centres of films.*

The observed resist thickness variation was compensated by using several stages of resist application, placing the resist drops in different places of the sample for each coating

a	r	min	q1	median	q3	max	biased error		max -min	q3-q1
[mm]	[mm]	[nm]	[nm]	[nm]	[nm]	[nm]	[nm]	[%]	[nm]	[nm]
0	0	76	125	194	254	290	64	33.0	214	129
10	5.8	79	125	186	245	277	60	32.3	198	120
20	11.5	77	123	169	223	270	50	29.6	193	100
30	17.3	83	113	147	192	259	38	25.9	176	79
40	23.1	81	104	126	162	225	26	20.6	144	58
50	28.9	73	95	109	132	168	17	15.6	95	37
60	34.6	59	90	94	101	107	6	6.4	48	11
70	40.4	43	65	75	86	93	10	13.3	50	21

TABLE 2.2: *Statistical data of 3-layered resist thickness and uniformity resulting from different separation distance (a) of the layers. The first (q1) and third (q3) quartiles are presented to give better statistical understanding of the 3-layered resist thickness variations.*

event (see figure 2.8). Calculations were made to determine the optimum distance between the drops in order to achieve best uniformity (see table 2.2). Depending on the number of float coating layers, the drops were placed at each vertex of an equilateral triangle (for 3 times 3 layers) and regular pentagon (for 5 layers). Depending on the number of layers, the optimum distance between a centre of each layer was found to be around $a = 60\ mm$ (see figure 2.9) and $a = 40\ mm$ for triangle and pentagon respectively, which translates into a displacement from the centre of the wafer of $r = 34\ mm$ for both approaches. Unfortunately, such a displacement is not achievable. The diameter of the PMMA film is between $115 - 125\ mm$, which for a 3" wafer gives a margin of $20 - 25\ mm$. If the film is placed in a manner such that not the whole wafer is covered, then there is a risk of the film sliding down, due to the trapped water lubrication. This maximum displacement gives $a = 35 - 45\ mm$ for a triangle and $a = 23 - 30\ mm$ for a pentagon. This is true for the diameter of the specific pipette outlet that is used, as a larger drop would result in larger area of dried-up resist film. Even though it is possible to increase the outlet size, consequently increasing the drop size, there was no reason found for doing so.

The PMMA resist layer resulting from the float coating technique is influenced by [99]:

- The concentration of the resist and molecular weight of the polymer. These affect the thickness of the float coating layer. A PMMA resist with higher concentration and heavier molecular weight forms a thicker layer, which becomes more prone to cracks.
- The temperature of water affects the evaporation rate of o-xylene solvent. This is particularly important immediately during the resist spreading. The lower the

water temperature, the more time there is for a PMMA resist to spread before it solidifies, which results in greater diameter of the resist film.

Although effective, float coating suffers from a number of practical problems. Any draft or table vibration during evaporation of the solvent causes wrinkles in the resist. It was also found that in order to minimize the cracks in the resist it is a good idea to run the process on a levelled table. When removing water from the dish, the water trapped between the resist and the substrate on a non-levelled sample/table causes the water to move towards lowest point on the wafer. This causes extra stress on the resist film. It was observed on some occasions that the resist failed to hold the trapped water and cracked. Additionally, if a mesh is approximately the size of the substrate then it is worthwhile to remove only as much water from the dish as it is necessary to level the water surface with the bottom side of the substrate. The wafer together with the mesh can then be removed using 2 index fingers and thumbs, which gives extra support for the overhanging resist. This eliminates the problem whereby the excess of the resist hangs from the edge of the substrate and its weight causes undesired cracks to the resist film due to the film stress. Alternatively, a larger metallic mesh could be used to provide support for the overhanging resist.

2.3 Dry etching

Dry etching processes offer some advantageous over wet etch process. Despite having lower selectivity and etch rates, and requiring expensive machinery, in general dry etching is capable of delivering much smaller features and anisotropic (especially vertical) etch profiles. Within the dry etch processes based on the process parameters certain compromises can be achieved for obtaining specific etch outcomes:

- gases used - different gases have different etch rates for the specific conditions. Mixing of gases can modify the etch rate, etch profile or selectivity.
- gas flow - the higher the flow rate, the higher the etch rate
- RF power - the higher the power, the lower selectivity and the higher the etch rate
- pressure - the lower the pressure, the greater the anisotropy
- temperature - lowering the temperate of the substrate can increase (e.g. for Si) or decrease (e.g. for SiO_2) the etch rate, as well as increases anisotropy and dry etch resistance of organic masks [105]

The dry etch processes can be divided into four types:

- sputter etching
- plasma etching
- Reactive Ion Etching (RIE)
- Deep Reactive Ion Etching (DRIE)

Sputter etching uses a similar principle of operation to sputtering deposition systems (see figure 2.10). Sputtering deposition systems use ion bombardment on the material target to be sputtered. When the energy of an ion is greater than the surface binding energy of the material target (e.g. for $Si - Si$ 2.3 eV [106]), an atom is ejected. In principle, it is a momentum exchange process. If instead of the material target a sample of interest is placed, the bombarding ions remove material from the sample surface - an etching process. This process is referred to as physical etching and results in highly anisotropic etch profiles.

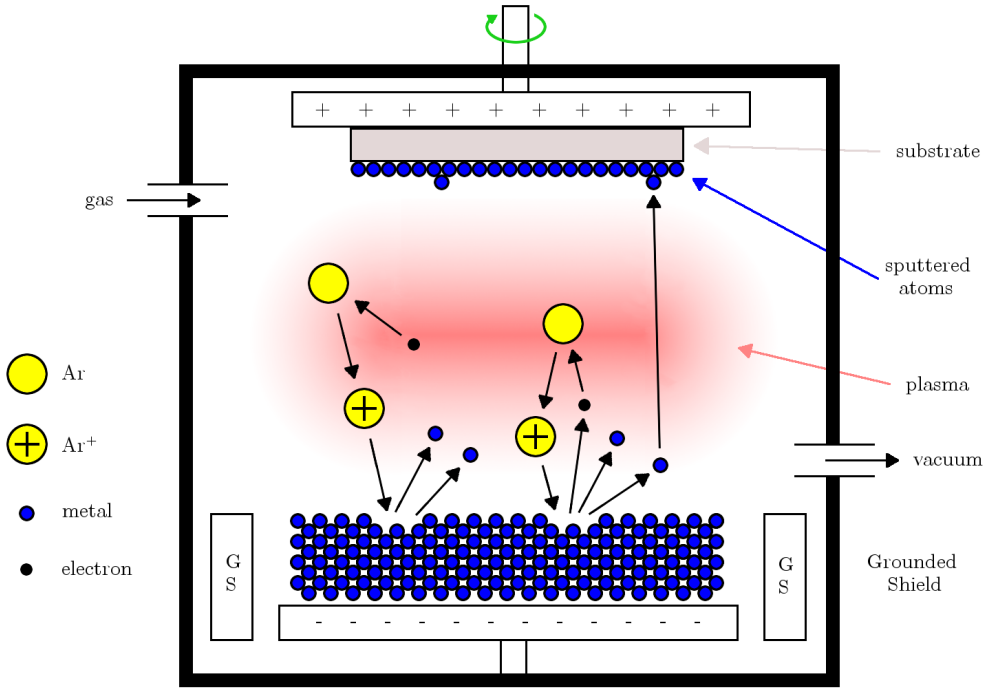


FIGURE 2.10: *Diagram showing sputtering tool and its principle of operation. Ar is ionized by RF power and the ions are accelerated towards the target material. After impact target atoms are released and travel to the substrate where they form layers of atoms of the thin film.*

In plasma etching, an ionized gas (plasma) is formed by the application of the RF power. This ionized gas interacts with a sample surface and in the course of a chemical reaction the material is etched. This process is referred to as chemical etching. Due to the chemical nature of this process, the anisotropy is compromised but the selectivity is much better when compared to the sputter etching. During design of such process care must be taken to make sure that the by-products of the chemical reaction do not

condense on the surface and interfere with the etching process. In [107] Wilkinson et al. show that in the SiO_2 etching process using CHF_3, the decomposition of the gas can give rise to polymeric film formation. Such a film can lower the etch rate of the process.

Reactive ion etching is a combination of plasma and sputter etching. The plasma breaks gas molecules into ions, which are accelerated towards the specimen surface and react with it. There is also ion bombardment taking place, which constitutes the physical part of the RIE etch. Due to combination of the two processes, a flexible compromise between anisotropy and selectivity can be reached [100].

In the table 2.3 a comparison of dry etching characteristics are presented.

etch type	plasma	RIE	DRIE	sputter
pressure	high[a]	medium[b]	low[c]	low
beam energy	low	medium	low	high
etching	chemical	chemical + physical		physical
anisotropy	low	medium	v. high	high
selectivity	high	medium	medium	low

[a] $> 100\ mTorr$
[b] $10 - 100\ mTorr$
[c] $< 10\ mTorr$

TABLE 2.3: *Table comparing different dry etch processes characteristics.*

The remaining dry etching process is Deep Reactive Ion Etching (DRIE). In this process very high etch rates as well and nearly vertical sidewalls of can be achieved. The process is based on "Bosch process" [108]. Unlike the case of plasma etching, the polymeric film formation is required in this process in order to protect the sidewalls of the etched features so the anisotropy can be increased. The passivation of Si material is achieved by application of C_4F_8 gas with specific conditions presented in the process table G.2. During the process of etching two alternating gases or gas mixtures are used. One gas composition etches the substrate whereas the other causes polymer formation on the exposed surface of the sample (see figure 2.11). The previously formed polymer is quickly sputtered by the physical part of the etch and the substrate etching process can progress. Thanks to the anisotropic nature of the physical etching, the sidewalls are protected from the etching, very little undercut can be observed and the sidewalls are vertical.

In figure 2.12, a released cantilever can be observed. The release etch uses the Bosch process. The etched sidewall scalloping is very characteristic, due to each etching cycle leaving a small isotropic bite in the sidewall. The number of these bites gives the number of the cycles of etch gas composition being switched on, which equals to the number of

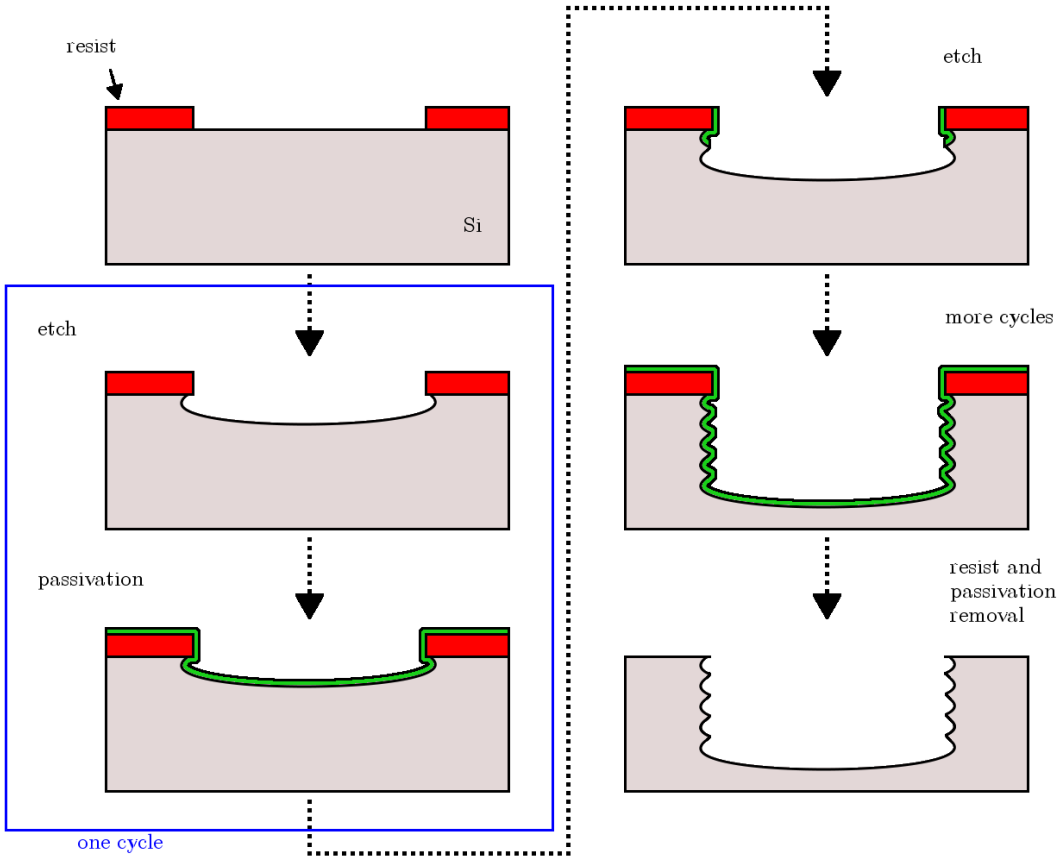


FIGURE 2.11: *Diagram presenting steps of the DRIE etching process.*

cycles in the Bosch process (in figure 2.12 23 cycles were used to etch through the membrane leaving the exposed cantilever).

2.3.1 Interferometry

In order to determine end point of an etching process, calculations can be done to estimate a required etching time based on an average etch rate of the process and the material thickness to be etched. However, such a calculation is only an approximation. If the layer being etched incorporates an etch stop, additional overetching time may need to be added to compensate for non-uniformity of the material being etched or etch rate variation. Minimization of the overetch time is often required to avoid excessive erosion of the underlying etch stop layer and can be achieved by using an interferometer.

The principle of interferometer operation is presented in figure 2.13. The laser light source provides a beam (at Glasgow $\lambda = 670\ nm$) that travels towards the areas of the sample not protected by resist. Once it reaches the sample surface part of it (sampling beam) is reflected from the $SiO_2/ambient$ interface, and the remainder (reference beam) is reflected by the Si/SiO_2 interface. This way two beams are formed, superimposed

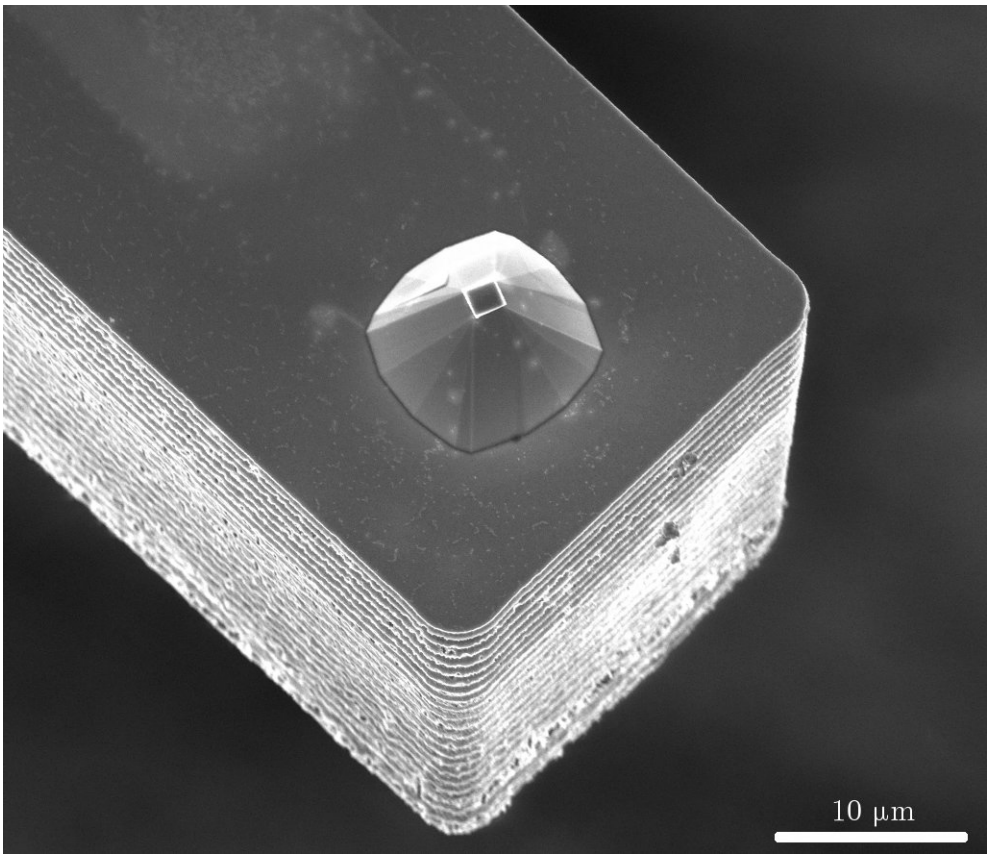


FIGURE 2.12: *SEM diagram presenting Si AFM cantilever released in the Bosch process. Each indentation in the sidewall of the cantilever represent one Bosch process cycle.*

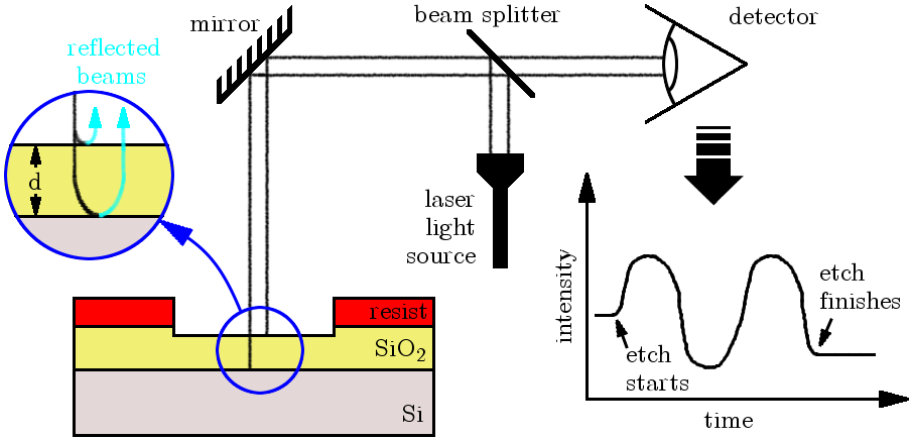


FIGURE 2.13: *Diagram presenting the principle of operation of an interferometer used for dry etch process depth control.*

and read by a detector. If the dry etching process is in progress, the SiO_2 thickness gets smaller and the difference in path lengths for the reference and sampling beams decreases. Due to the beams being superimposed, the light intensity read by the detector changes periodically. The adjacent minima (maxima) spacing of the measured light intensity

corresponds to the change in etched material thickness Δd and is given by [109]

$$\Delta d = \frac{\lambda}{2 \cdot n} \tag{2.4}$$

where λ is the light wavelength used, n is the refractive index of the transparent material being etched ($n = 1.457$ for SiO_2). From the obtained plot, the etch rate can be calculated by

$$etch\ rate = \frac{\Delta d}{t} = \frac{\lambda}{2 \cdot n \cdot t} \tag{2.5}$$

where t is the time needed for the light intensity for form one sine cycle.

When all of the SiO_2 material is etched, both beams travel the same length, effectively the light intensity does not change and this allows accurate termination of the etching process. However, the measurement is obtained at a specific area on the sample and consequently large processing area may be still affected due to non-uniformity of the etch over the sample, but to a smaller degree.

2.4 Hall effect

The Hall effect is a phenomenon that is very often used to perform a direct measurement of a magnetic field. The Hall voltage is proportional to the magnetic field and in order to design such a sensor it is necessary to analyse how this voltage is formed.

As presented in figure 2.14, if there is a current flow through a conductor which is placed in a magnetic field perpendicular to the current flow, then, due to the Lorentz force, the moving charges are deflected to the side of the conductor. This magnetic influence is balanced by charge build-up, which leads to a measurable voltage between the two sides of the conductor, called Hall voltage.

The Lorentz force in absence of an additional electric field is

$$\vec{F} = q\ \vec{v} \times \vec{B} \tag{2.6}$$

so if the magnetic field and electrostatic forces are equal and opposite, i.e. equilibrium

$$F_y = q\ v_x\ B_z = q\ E_y \tag{2.7}$$

Current density is

$$J_x = n\ |q|\ v_x \tag{2.8}$$

and current

$$I_x = J_x\ w\ d = n\ |q|\ v_x\ w\ d \tag{2.9}$$

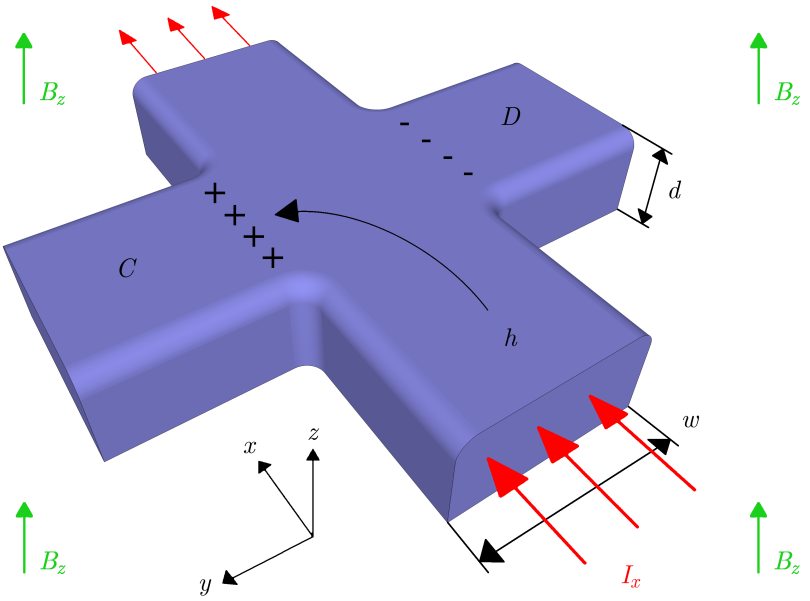


FIGURE 2.14: *Schematic demonstration of the Hall effect.*

V_C, V_D - *electrical potentials of points* C *and* D*, respectively*
$V_H = V_C - V_D$ - *Hall voltage*
I_x - *applied current*
B_z - *magnetic flux intensity*
E_y - *electrical field*
w - *width of wire*
d - *thickness of wire*
n (p) - *number of free electrons (holes) per unit volume*
q - *charge of particles*
e - *charge of electron*
h - *charge of hole*
v_x - *velocity of particles*
μ_e - *electron mobility*
μ_h - *hole mobility*

Hall voltage is

$$V_H = E_y\ w = v_x\ B_z\ w = J_x \left(\frac{1}{n|q|}\right)\ B_z\ w \tag{2.10}$$

Hall coefficient is defined as

$$R_H\ = -\frac{1}{n|q|} \tag{2.11}$$

where the positive sign applies to holes and negative to electrons. This equation is true for metals, however, in case of semiconductors it becomes more complex due to the presence of both electron and holes in the material and may be shown [110] to be

$$R_H\ = \frac{r_h p - r_e b^2 n}{e(p + bn)^2} \tag{2.12}$$

where $b = \mu_e/\mu_h$, r_e (r_h) is the Hall scattering factor for electrons (holes) which takes into account the energy spread of the carriers. The Hall scattering factor is a dimensionless parameter and its value depends on the dominant scattering mechanism:

- lattice scattering
- carrier-carrier - also known as Coulomb - scattering

- defect scattering which can be further divided into:
  - neutral or ionized impurity scattering
  - crystal defect scattering
  - surface roughness scattering
  - interface charge scattering

For low doping levels of bulk silicon at room temperature r_e is equal to 1 [111] and $r_h = 0.9$ [112].

The dominant scattering mechanism will change depending on the form in which the semiconductor is used. When bulk material is used then phonon and impurity scattering are the dominant scattering mechanisms. For the carriers in the induced channel of the MOSFET transistor, there are additionally significant Coulomb scattering and surface roughness scattering processes. This is due to the fact that the carriers are confined to a very thin inversion layer (approximately 10 *nm* thick - see figure 2.15). Consequently, the mobility decreases between 2-3 times [113] when compared to bulk mobility. This change in mobility is described by the effective mobility (μ_{eff}), which accounts for the difference between bulk and surface mobility. The effective mobility increases with decreasing temperature, decreasing doping level, decreasing vertically applied electrical field and also depends on several other scattering mechanisms. Due to the fact that the effective mobility is a technological value, as it depends on the surface processing, no simple equation was found for calculating the effective mobility; it must be determined by experiment.

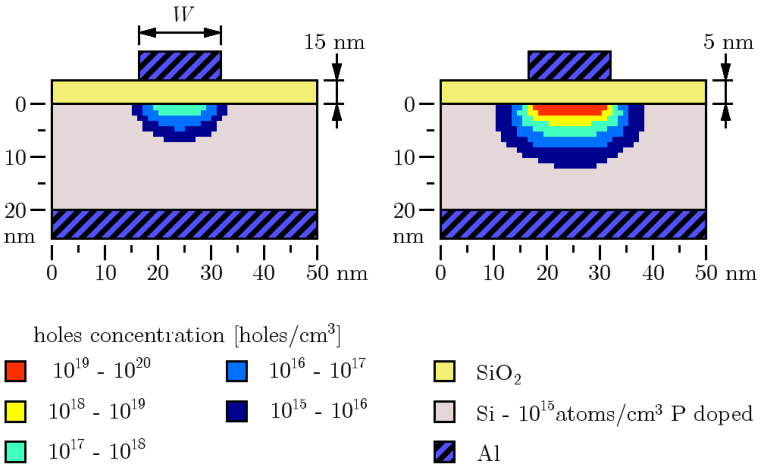


FIGURE 2.15: *Diagrams presenting COMSOL [114] simulation results of the MOSFET capacitor in a strong inversion. The induced charge thickness depends on the applied voltage and the dielectric layer thickness. For both devices the top electrode width is equal to* $W = 15$ *nm and the applied voltage is* -7.5 *V.*

More than one shape of device is commonly used for measuring the Hall effect. For each shape a geometrical factor can be calculated based on the device dimensions. The

geometrical factor describes the diminution of the Hall voltage in a finite-size device compared to the Hall voltage corresponding to infinitely long device, so it is equal to

$$G_H = V_H / V_{H\infty} \tag{2.13}$$

The geometrical factor is a dimensionless parameter and its value depends on the shape of the device, ratio of its dimensions and the Hall angle (Θ_H), which depends on the applied electrical field and the material out of which the device is made. Figure 2.16 presents a plot of the geometrical factor for the cross shape device, which was obtained by plotting the equation 2.14.

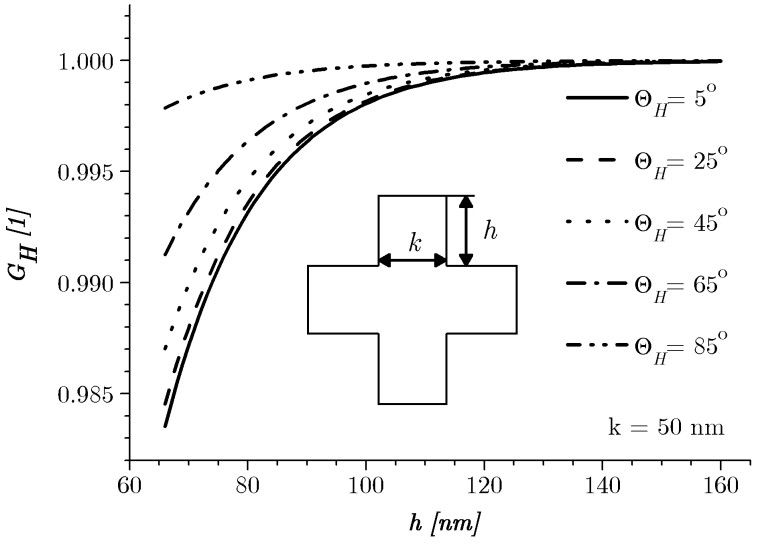


FIGURE 2.16: *The influence of Hall bar wire length and Hall angle on Hall geometrical factor.*

$$G_H(k, h, \Theta_H) = 1 - (1.045 exp(-\pi h/k))(\frac{\Theta_H}{tan\Theta_H}) \tag{2.14}$$

which is accurate to 0.5% if $0.38 \geq k/2h$ [115].

Using the geometrical Hall factor, the Hall voltage is given by

$$V_H = G_H \; J_x \; R_H \; B_z \; w = G_H \; \left(\frac{I_x}{\cancel{w}\; d}\right) \; R_H \; B_z \cancel{w} = G_H \; \frac{I_x}{d} \; R_H \; B_z \tag{2.15}$$

The Hall coefficient becomes

$$R_H = \frac{V_H}{G_H \; I_x \; B_z} \; d \tag{2.16}$$

And the magnetic field strength is

$$B_z = \frac{V_H}{G_H \; I_x \; R_H} \; d \tag{2.17}$$

One of the most important characteristics of a sensor is its sensitivity. For a Hall bar sensor the absolute sensitivity is defined as:

$$S_A = \left|\frac{V_H}{B_z}\right|_c \tag{2.18}$$

where c denotes specific conditions like bias current, frequency and temperature. However, most often the current-related sensitivity is used:

$$S_I = \frac{S_A}{I_x} = \frac{1}{I_x}\left|\frac{V_H}{B_z}\right| \qquad V_H = S_I\ I_x\ B_z \tag{2.19}$$

so the current-related sensitivity for the Hall device is

$$S_I = G_H \frac{|R_H|}{d} \tag{2.20}$$

The geometrical factor in equation 2.20 indicates that the shape of the device is important from the sensitivity point of view. Choosing a rectangular Hall plate, which requires fewer fabrication steps than the cross-shape device, would require an elongated form of the sensor to achieve high geometrical factor (for $length \geq 3 \cdot width$, $G_H \approx 1$) which translates into the high current-related sensitivity. However, having the square sensing element is more important in case of a sensor which finds application in the magnetic AFM. No imaging system provides exact measurement of an object of interest. The geometrical error that the imaging system introduces is described by the point spread function. If the sensor shape is a rectangle then the obtained image of a point object appears to be rectangular. In order to minimize such measurement errors, the sensor needs to be square.

Ultimately the cross-shape sensor was selected, as the cross shape sensing element is still relatively easy to achieve/fabricate and, what is more, its geometrical factor depends on the length of the leads, which do not influence the behaviour of the sensor or its resolution.

2.4.1 Calculations for Si MOSFET Hall bar

In order to check if the proposed technology can potentially deliver the working device, Hall bar sensitivity, Hall coefficient and magnetic field resolution calculations were done. The following calculations were performed using parameters used for fabrication of the MOSFET transistor on the AFM tip (square active area with $w = 1\ \mu m$ and oxide thickness $t = 15\ nm$). Afterwards the same calculations were conducted for the technological

limit established in section 4.6 (square active area with $w = 15\ nm$ and oxide thickness $t = 5\ nm$).

The working conditions of the transistor are set to $V_{ds} = 5\ V$, $V_{gs} = 2\ V$ and $B_z = 0.5\ T$. The working conditions are the same as Yang et al. [71] used in their experiment in order to allow direct comparison with the calculated device performance.

The electrical field applied to the device (to make the current I_x flow) is

$$E_x \ = \ V_{ds} \ / \ w \ = \ 5[V] \ / \ (1\mu[m]) \ = \ 5 \cdot 10^6 \ [V/m] \tag{2.21}$$

Drift velocity of the carriers is

$$v_x \ = \ \mu_h \ E_x = 0.04[m^2/Vs] \ \cdot \ 5 \cdot 10^6[V/m] \ = \ 2 \cdot 10^5 \ [m/s] \tag{2.22}$$

However, such drift velocity is greater than saturation velocity and consequently for the following calculation saturation velocity is taken ($v_x = 10^5\ [m/s]$).

From equation 2.10 Hall voltage is

$$V_H \ = \ v_x \ \ B_z \ w \ = \ 10^5[m/s] \ \cdot \ 0.5[T] \ \cdot \ 1\mu[m] \ = \ 50m \ [V] \tag{2.23}$$

For a parallel plate capacitor, the capacitance C is:

$$C \ = \ \frac{\epsilon_r \epsilon_0}{t} \ = \ \frac{3.9 \ \cdot \ 8.85 \cdot 10^{-12}[F/m]}{15n[m]} \ = \ 2.3m \ [F/m^2] \tag{2.24}$$

where ϵ_r is relative permittivity (for SiO_2 $\epsilon_r = 3.9$), ϵ_0 electric permittivity ($\epsilon_0 = 8.85 \cdot 10^{-12}\ F/m$) and d is the thickness of the dielectric layer.

Charge gathered in the capacitor equals to

$$Q \ = \ C \ V_{gs} \ = \ 2.3m[F/m^2] \ \cdot \ 2[V] \ = \ 4.6m \ [C/m^2] \tag{2.25}$$

The current is

$$I_x \ = \ v_x \ Q \ w \ = \ 10^5[m/s] \ \cdot \ 4.6m[C/m^2] \ \cdot \ 1\mu[m] \ = \ 460\mu \ [A] \tag{2.26}$$

Using equation 2.19 the sensitivity is

$$S_I \ = \ \frac{V_H}{I_x \ B_z} \ = \ \frac{50m[V]}{460\mu[A] \ \cdot \ 0.5[T]} \ = \ 217.3 \ [V/AT] \tag{2.27}$$

By assuming charge thickness $d = 10\ nm$ [71], the Hall coefficient is

$$R_H \ = \ S_I \ \cdot \ d \ = \ 217.3[V/AT] \ \cdot \ 10n[m] \ = \ 2.17\mu \ [Vm/AT] \tag{2.28}$$

Series resistance is

$$R_s \ = \ \frac{V_{ds}}{I_x} \ = \ \frac{5[V]}{460\mu[A]} \ = \ 10,900 \ [\Omega] \tag{2.29}$$

For such series resistance, the thermal noise from equation 2.33 [116] is

$$v_n \ = \ \sqrt{4 \ k_B \ T \ R_s \ \Delta f} = \\ \sqrt{4 \ \cdot \ 1.38 \cdot 10^{-23}[J/K] \ \cdot \ 293.15[K] \ \cdot \ 10,900[\Omega] \ 1[Hz]} = \ 13.3n \ [V/\sqrt{Hz}] \tag{2.30}$$

The corresponding magnetic field resolution is

$$B_{min} \ = \ \frac{v_n}{I_x \ S_I} \ = \ \frac{13.3n[V/\sqrt{Hz}]}{460\mu A \ \cdot \ 217.3[V/AT]} \ = \ 133n \ [T/\sqrt{Hz}] \tag{2.31}$$

These numbers were calculated for a Hall bar device that could be fabricated using available technology. The numbers were also calculated for a technologically limited device. The lithography limit (presented in section 4.6) is set at $w = 15\ nm$.

If the gate is scaled down without scaling down the oxide thickness t_{ox} (channel width $w = t_{ox}$), the carriers in the channel perceive the gate as a point charge. The shape of an induced channel profile becomes not rectangular, but semicircular, due to the fringing effect. Consequently, a Hall bar fabricated using such approach would result in a non-linear sensitivity of the active area, being most sensitive in the central line of the current flow.

Such behaviour can be diminished by scaling down the oxide thickness. Ideally t_{ox} should be small when compared with the capacitor plate dimensions in order to achieve uniform charge distribution by uniform electrical field.

The electrical field distribution in SiO_2 was simulated and the result is presented in figure 2.17. The Al gate is 15 nm wide. Together with scaling down the gate width, the oxide thickness also needs to be scaled down with the same factor α. Assuming scaling down of the applied voltage by α, the electrical field distribution does not change.

For a fixed gate width, the thicker the oxide is, the worse the channel width control becomes. In order to obtain a reasonable (error of 5%) channel width control, the ratio of the gate width to the oxide thickness should not be less than 3 [117].

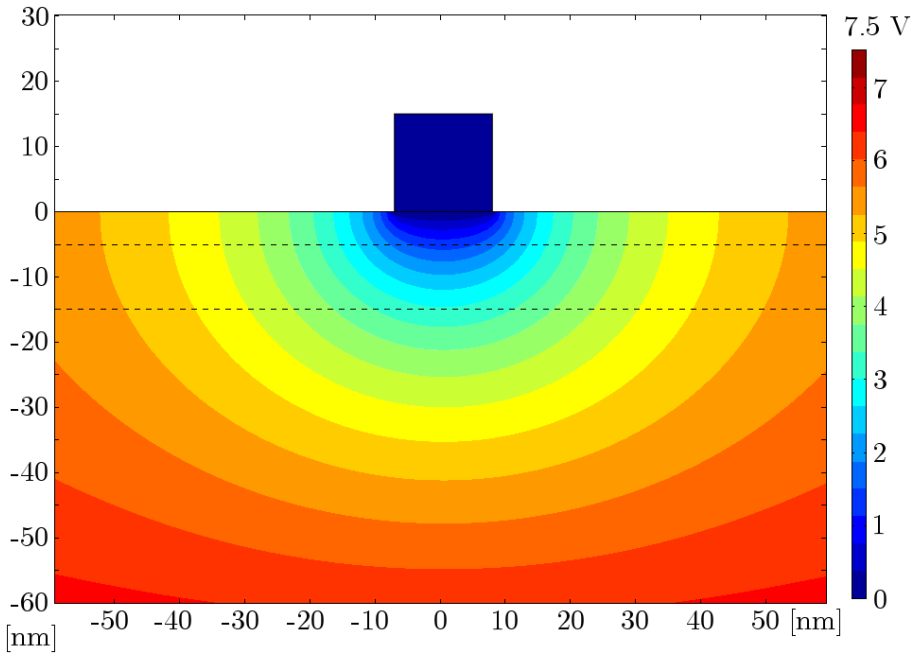


FIGURE 2.17: *Diagram presenting COMSOL [114] simulation results of electrical field distribution in SiO_2.*

In order to achieve a control of the gate, the oxide thickness has to be scaled down to approximately $t = 5\ nm$. By maintaining the same working conditions, the numbers are as follows

$$I_x = 20.7\mu\ [A]$$

$$V_H = 0.75m\ [V]$$

$$S_I = 72.4\ [V/AT]$$

$$B_{min} = 41.7\mu\ [T/\sqrt{Hz}]$$

The results of the calculations of the current-related sensitivity S_I for both ($w = 1\ \mu m$ and $w = 15\ nm$) devices are in good agreement with extrapolation based on the devices presented by Yang. If successfully fabricated, the technologically limited device could increase not only the Hall bar spatial resolution by more than a factor of 3, but also increase its sensitivity by a factor of 18, when compared with the smallest reported device fabricated in Bi material system by Sandhu. What is more, the developed technology results in fabrication of the active device on AFM tip, which allows taking full advantage of the offered magnetic spatial resolution.

As far as the magnetic field resolution is concerned, the calculations indicate an improvement by a factor of 2. This number could be improved a little bit even further by further lowering of the oxide thickness.

Considering a possible improvement in the spatial resolution, the above calculation results suggest that the fabrication of the Hall bar in MOSFET technology should provide a device with very promising characteristics (see section 1.3).

2.4.2 Noise

As size of the Hall bar device is scaled down, its sensitivity becomes smaller (see section 1.3), which means that for certain conditions (I_x, B_z, temperature, bandwidth, frequency) as the spatial resolution increases, the Hall voltage V_H decreases. Assuming, for a moment that a noise figure of a resistive device does not change (even though the $1/f$ noise increases) with scaling down the device, the signal-to-noise ratio decreases, which means that the minimum detectable magnetic field unfortunately increases in value (lower magnetic resolution). This translates into a compromise between spatial and magnetic field resolution when designing a sensor for SHPM.

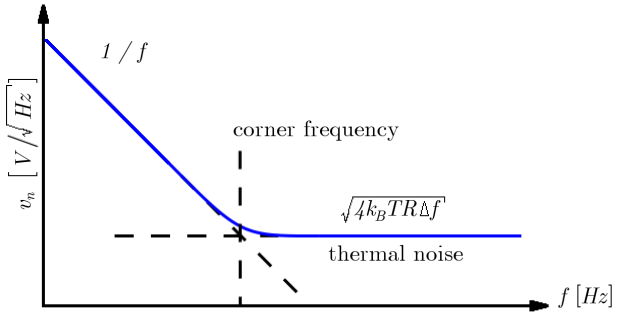


FIGURE 2.18: *Resistive device noise figure across the range of frequencies.*

The dominant types of noise in a resistive device, which a Hall bar is, are thermal (also known as Johnson or white) and $1/f$ (also known as Flicker or pink) noise, as presented in figure 2.18. In devices conducting small current there is also a possibility of observation of shot noise due to a discrete nature of electrons. The shot noise is a random current fluctuation (uncorrelated electron transport) and its value is given by [116]

$$v_n = R\ \sqrt{2\ q\ I\ \Delta f} \tag{2.32}$$

where q is the elementary charge of electron $1.6 \cdot 10^{-19}\ C$, I is the current $[A]$ flowing through the resistance R $[\Omega]$ and Δf is the bandwidth $[Hz]$.

Since the magnitude of thermal noise is determined by the second law of thermodynamics, there is nothing that can be done in case of the thermal noise (see equation 2.33) for a Hall bar device working at room temperature apart from trying to minimize the channel, contact and lead resistances as well as keeping the bandwidth of the measurements narrow. This noise sets the lower limit of how small a signal can be recovered.

The thermal noise can be calculated by [116]

$$v_n = \sqrt{4\ k_B\ T\ R\ \Delta f} \tag{2.33}$$

where k_B is the Boltzmann constant $1.38 \cdot 10^{-23} JK^{-1}$, T is the absolute temperature $[K]$, R is the resistance $[\Omega]$ and Δf is the bandwidth $[Hz]$.

As discussed in section 1.3 the $1/f$ noise can be significant when compared with Johnson noise. With scaling down the Hall bar, the Flicker noise increases and the corner frequency shifts towards higher frequencies.

This dependence can be proven by applying constant voltage scaling law [118]. For device dimensions (L, W) the scaling parameter is $1/S$, however, this becomes of secondary importance in case of the device comparison per area. Such approach introduces useful simplification especially if an assumption of equal aerial trapped charge densities is made. This then indicates that for the same area the trapped charge is the same.

The scaling parameter for the gate oxide thickness t_{ox} is $1/\sqrt{S}$ and consequently, the capacitance per area follows the same trend. By lowering the capacitance and keeping the (trapped) charge the same, the voltage - $1/f$ noise - increases ($U = Q/C$) assuming that the remaining parameters stay unchanged.

Such an increase in the flicker noise, decreases the magnetic field resolution even more. This noise is related to the specific materials and fabrication techniques. Due to the complexity of the p-type induced channel MOSFET Hall bar device using the AFM tip fabrication process and no or limited number of equivalents for each fabrication technique used, the detailed analysis of this problem is hard. Fortunately $1/f$ noise may be circumvented in the context of scanned probe microscopy.

In [119] Abraham et al. presented a method of $1/f$ noise reduction for STM. Apart from normal operation (see figure 2.19), the tip additionally vibrates parallel to the sample surface. This dithering is achieved by feeding additional sinusoidal excitation at frequency f_0 to the piezo driving the tip along the scan line. The amplitude of the vibrations is stated to be as low as 0.01 Å. Because the f_0 frequency is greater than the feedback response frequency, the regular operation of the positioning system is not affected. Thanks to this dithering, when the tip meets an obstacle, probing is done not only with the feedback system, but also with the high frequency f_0. In order to retrieve the topographical information carried by the high frequency signal, the lock-in amplifier is used with reference frequency of f_0. This way the measurement is moved to the higher frequency band allowing to avoid $1/f$ noise.

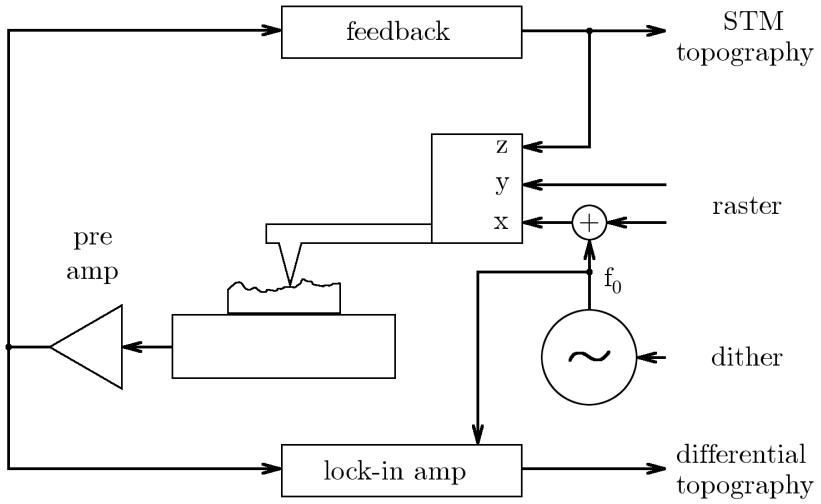


FIGURE 2.19: *Block diagram of the STM system with the noise reduction method proposed by Abraham et al.*

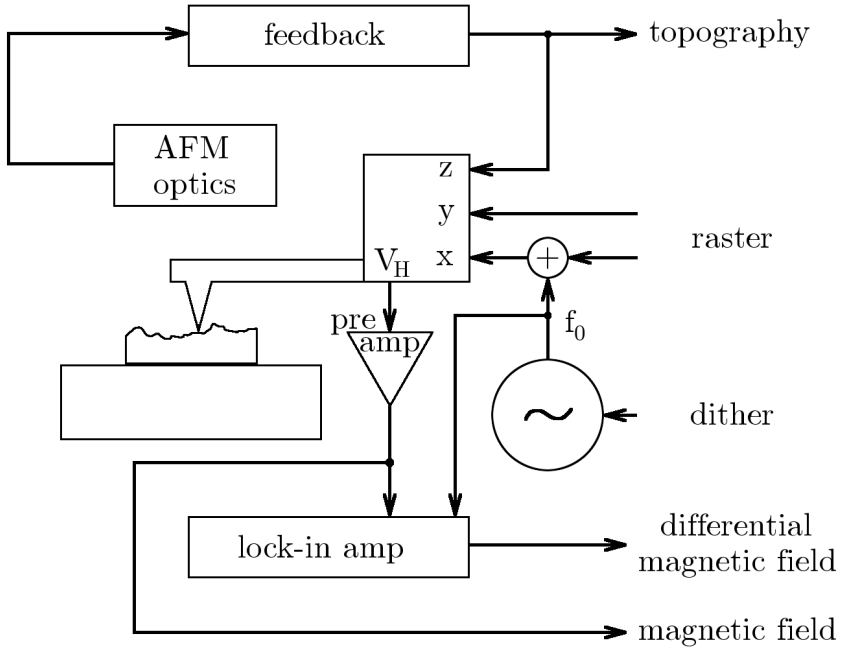


FIGURE 2.20: *Block diagram presenting the noise reduction method proposed by Abraham et al. to the SHPM.*

This technique can be applied to minimize the significance of the $1/f$ noise in the SHPM. The block diagram presenting this technique application is shown in figure 2.20. Like in the original system, the dithering signal is still connected to the piezo driving the tip along the scan line. The differential Hall voltage has to be converted to the single-ended signal, amplified and connected to the lock-in amplifier operating at the reference (dither) frequency f_0. The amplitude of the dithering signal needs to be a significant fraction of the spatial resolution, however, not too large, otherwise the magnetic image

will get blurred.

2.5 Diode

In [69] Kejik et al. presented a Hall bar device fabricated using a standard 0.8 μm CMOS process. The n-type Si 2.4 $\mu m \times 2.4$ μm active area device was fabricated in a form of a diode (see figure 2.21). The highly doped diffused layer is used as a conductive path. By combining two perpendicularly positioned wires a cross is formed - a Hall bar. In such an approach the thickness of the active area d is controlled by the diffusion depth. By keeping the reverse polarization of the diode with respect to the substrate, the leakage current is kept low, so it does not affect the working current which is passed through a device. The access of the Hall bar to the sample surface is limited to $s = 3$ μm due to the top passivation layer of the active device which is located in a corner of a chip.

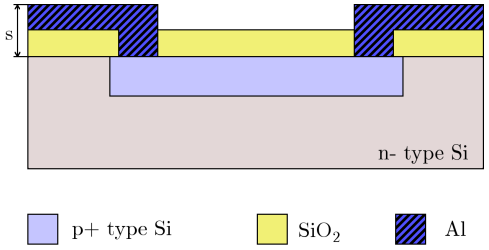


FIGURE 2.21: *Diagram of a Si diode with a highly doped layer used as a conductive path.*

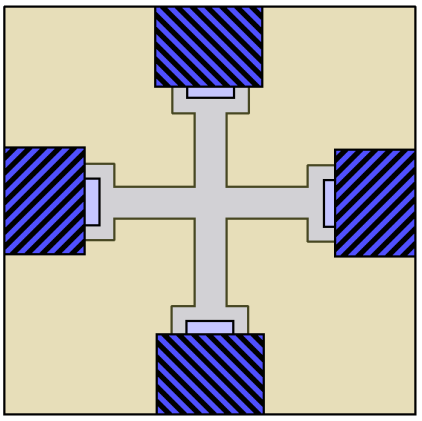


FIGURE 2.22: *Diagram of a plan view with a Si diode Hall bar. The SiO_2 layer is 70% transparent to allow the visibility of doped area.*

An attempt was made to fabricate a similar device in this project with a view to locating the active device on the apex of the AFM tip. In this way the separation distance between the device and the magnetic sample could be made much smaller (below 200 nm). Fabrication of a device with thickness in a range of 10's of nm using a spin-on dopant presents a resolution challenge. As a consequence a larger area on the AFM tip apex was planned to be doped. By the means of electron beam lithography and lift-off, a metal mask would have been prepared. The mask would have been then used in a RIE dry etch process to form the mesa. Based on the results presented by others (see table 1.2) the Si MOSFET Hall bar device is a better choice from the current-related sensitivity point of view. However, since from the standpoint of fabrication the active device realised as a diode is easier to fabricate, both devices were planned to be fabricated and compared.

2.6 MOSFET transistor

Enhancement mode p-type MOSFET transistor is a 4 terminal electronic device with its simplistic structure presented in figure 2.24. It is fabricated on n-type Si substrate with two, separated from each other, p-type islands - source (S) and drain (D), between which resistance is high. On the surface of the substrate there is a thin isolating layer, which is coated with metal (specifically between and a little bit over source and drain) - gate (G).

The gate and the substrate - bulk (B) - act as a MOS capacitor. By applying voltage to this capacitor, charge begins to gather beneath the dielectric layer of the gate. With increase of the voltage, the electrical characteristics of the thin layer begin to change, and above certain voltage (threshold voltage) the n-type silicon starts acting as a p-type forming this way a bridge between source and drain - induced channel. This induced channel reduces significantly the resistance between the source and the drain, so electrical current can pass between them. An exemplary characteristic of such a transistor can be seen in figure 4.12.

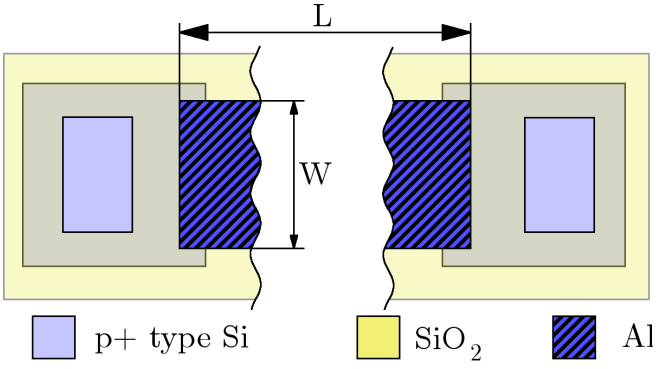


FIGURE 2.23: *Diagram presenting the gate length and width.*

The size of the gate, see figure 2.23, is defined by the gate length (L) and gate width (W), which determines the current for specific electrical conditions. The wider and the shorter the gate is, the lower the channel resistance and consequently the higher current becomes. However, with shortening the channel (well below 1 μm [116]), short-channel effects make the transistor enter the saturation region earlier and as a result the current is limited. The reason for which this happens is that the drift velocity of the carriers enters saturation.

Drift velocity is the average speed with which a charge moves due to electric field. Above a certain electrical field, the charge drift velocity does not depend on the electrical field any more because of charge scattering and the drift velocity becomes saturation velocity.

One of the most important parameters to judge the transistor direct current (DC) performance is transconductance (g_m). It is a measure of how much influence the gate has on the induced channel and it is measured as [116]:

$$g_m = \frac{\Delta I_{out}}{\Delta V in} \tag{2.34}$$

2.6.1 Application

Induced channel Si MOSFET (see figure 2.24) Hall bar devices have already been fabricated and presented in [67] and [70]. Janossy does not provide any details about how scans were performed. In the case of Yamaguchi the 50 μm square active device was fabricated approximately 530 μm from the corner of the die. If the approach angle to the sample is as small as 1^o, the device-sample separation distance is 9.3 μm. By making a device much smaller, to realise the higher resolution active device it needs to be brought much closer to the specimen. In order to bring the active device closer to the sample, one solution could be to bring it much closer to the die corner. However, in this project the separation gap between the device and the specimen will be kept to the minimum by fabrication of the device on the functionalized AFM tip (see figure 2.25).

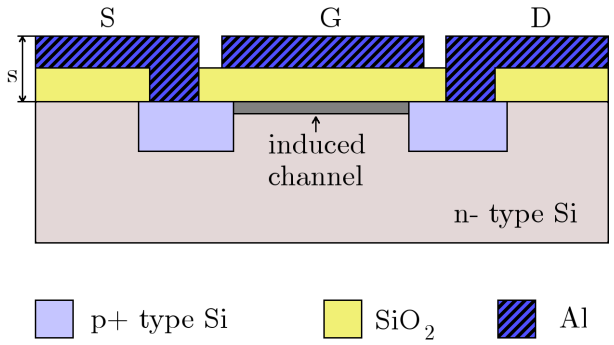


FIGURE 2.24: *Diagram of an induced p-type channel Si MOSFET transistor.*

When compared with the diode approach, the MOSFET transistor Hall bar device comprises one more terminal - the gate - to induce and control the channel between all 4 contact areas. Due to limited space on the apex, the regular cross design will be modified in order to form space for the additional terminal. The separation distance between the device active area and the magnetic specimen is the same as it is in case of a diode (field/gate oxide, metallization, optional top passivation layer).

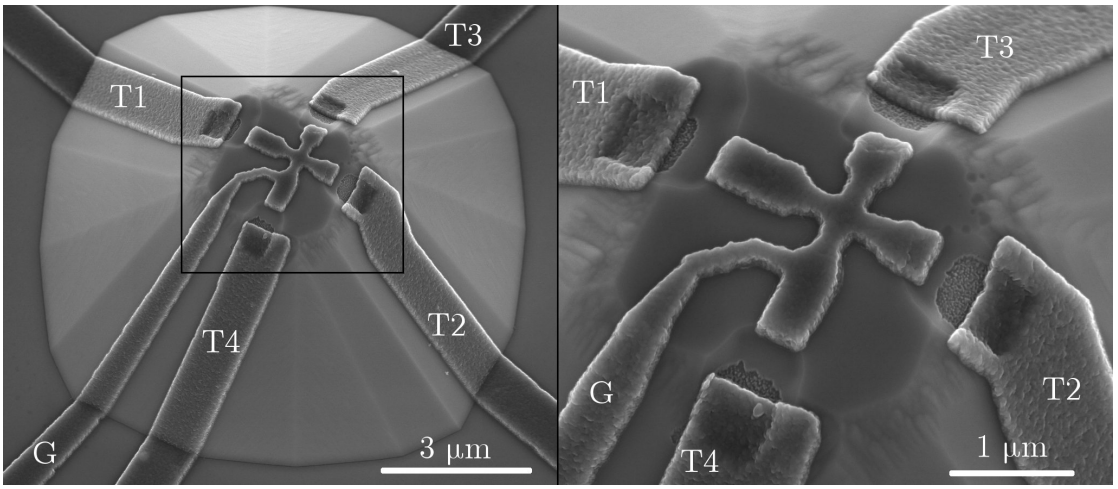


FIGURE 2.25: *On the left there is the SEM diagram of a lithographically defined* 280 *nm Hall bar device located on the apex of the AFM tip. The indicated area is zoomed in on the right hand side. The* 150 *nm thick Al metallization sits on top of* 15 *nm* SiO_2 *gate/field oxide.*

Chapter 3

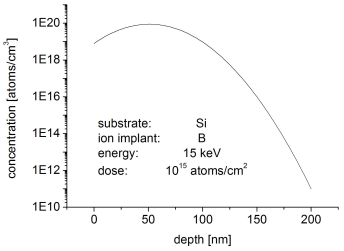
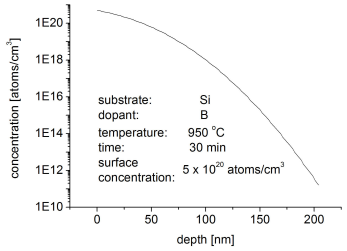
Fabrication

3.1 Triple mask design

In order to fabricate any MOSFET transistor, the introduction of impurities into the substrate is necessary to form source and drain regions. This can be achieved either by the process of ion implantation or diffusion (see table 3.1 for brief comparison of some characteristics of the processes). Ion implantation has many advantages over diffusion, such as smaller lateral spread and better concentration controllability [100]. Due to this, it is a preferred method of introducing impurities into substrates during fabrication of integrated circuits [100]. However, AFM probe fabrication involves etching in Si substrate thin membranes ($5 - 20\ \mu m$). Even though each AFM probe is surrounded by a supporting it Si frame, the wafers are very fragile. Due to this, the advantages of ion implantation were not as important as minimizing the risk of breaking the wafer when sending it to a facility capable of running an ion implantation process. Choosing diffusion from spin-on glass (SOG) process as means of doping the substrate resulted in reduction of the time in the device fabrication cycle. However, if needed, the fabrication process could be switched to ion implantation without significant change due to the universal masking material.

The diffusion process at University of Glasgow (see subsection 1.4.3) is performed from a doped glass film applied by spinning. Selective doping is achieved by using a thermally grown SiO_2, patterned mask to inhibit the diffusion of dopant. This thermal growth of SiO_2:

1. introduces stress in Si, a consequence of a difference in thermal expansion of the two materials [123] (problem described in section 3.3). This can lead to a

characteristic	ion implantation	diffusion
junction depth	10 nm – 10 μm [100]	< 70 nm [120] - > 20μm [92]
available masking materials	SiO_2, Si_3N_4, Ti, W, photoresist [100]	SiO_2, Si_3N_4 [121]
availability of tools for the process on site	✗	✓
simulated profile [101]		
maximum concentration	$1 \cdot 10^{21}$ [122]	$5 \cdot 10^{20}$ [100]
anisotropy	lateral deviation $50 - 60\%^a$ [100]	lateral diffusion $75 - 85\%$ [102]
additional cost to run the process	higher	lower
time needed to run the process	minimum 1 week	under 24 hours

[a] for 70 keV boron implantation into Si, dose $1 \cdot 10^{15} cm^{-2}$

TABLE 3.1: *Comparison of some characteristics of ion implantation and diffusion.*

degradation of substrate properties and the final device performance [100] e.g. by lowering breakdown voltage of p-n junction [124].

2. consumes the substrate - 44% of the grown SiO_2 thickness is the thickness of the Si layer that was consumed in the process [100]. Once the AFM tip is engineered, its shape should not be significantly altered.

3. causes an effect similar to that encountered in LOCOS process - at the bottom of the AFM pyramid there is a step in the thermally grown SiO_2 layer. The figure 3.2 presents a Si AFM pyramid with 1 μm of thermally grown SiO_2 and 150 nm of sputter coated Al, which was then partially Focused Ion Beam (FIB) milled. A closer look at the defect can be taken in a cross section in figure 3.3. This is a problem because such a step may affect formation of the continuous evaporated metallic film used in mask transfer process, cause doping of an area over which the signal leads are later formed and consequently increase crosstalk interference.

4. can cause redistribution of the already diffused dopant in Si (e.g. that used for the back contact), which introduces a change in the doping profile. This thermal process can move the junction deeper into the substrate, cause greater lateral diffusion and lower the doping concentration at the surface of the semiconductor. The extent to which the profile will be affected depends directly on the temperature and

time, and indirectly on the ambient of the oxidation process. The redistribution of dopant is not believed to be of great importance, due to possibility of running the oxidation process at low enough temperature to minimize these effects, and because of other factors described in section 3.5.

5. forms a non-conformal coating due to the dependence of the oxidation rate on the crystallographic plane [125]. Assuming a minimum of 300 nm of SiO_2 is required to fulfil the requirements of the masking material for diffusion process, a wet oxidation process run at 800^oC for 14 *hours* and 25 *minutes* will form 300 nm and 360 nm of SiO_2 respectively for $< 100 >$ and $< 313 >$ planes. The $< 100 >$ plane corresponds to the tip of the AFM pyramid, whereas $< 313 >$ is the plane which forms the sidewalls of the pyramid. This introduces a problem from the dry etch point of view when etching windows in SiO_2 on both planes simultaneously (see figure 3.1). Whereas on the plane $< 100 >$ the SiO_2 thickness is 300 nm, for the plane $< 313 >$ 360 nm of SiO_2 effectively becomes 470 nm of material to be etched due to angles between the planes and the directionality of the dry etch process. In order to fully open windows that are located on both planes when dry etching, it is the 470 nm of SiO_2 that needs to be etched. However, etching that much material on $< 100 >$ plane, where only 300 nm of SiO_2 is available, means that overetching of Si substrate occurs. This phenomenon is caused by the relatively low selectivity of Si over SiO_2 in CHF_3 plasma being from 1 : 6 for higher power (0.37 W/cm^2) to 1 : 9 for lower power (0.15 W/cm^2) [126] when compared with selectivity of e.g. $NiCr$ over SiO_2 being greater than 1 : 25.

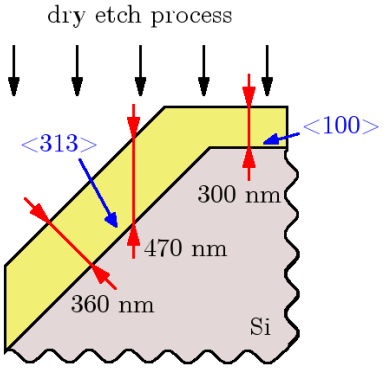


FIGURE 3.1: *Diagram presenting thermally grown SiO_2 on two Si crystallographic planes ($< 100 >$ and $< 313 >$). Selective removal of SiO_2 by using dry etch process may be problematic due to different SiO_2 thickness dependent on the plane.*

Even though using thermally grown SiO_2 as a mask for a diffusion is a common practice [100], a PECVD SiO_2 film has already been investigated, used and proved to work as well by others [97], [127]. Since it can act as a mask for a diffusion and solves the

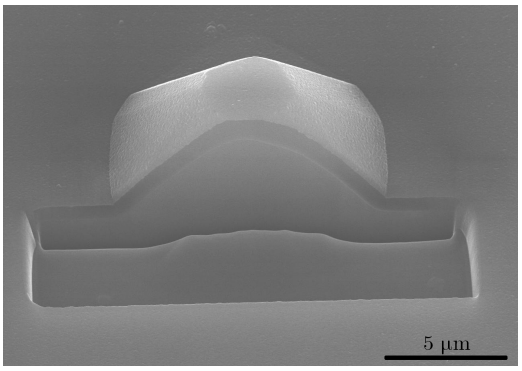


FIGURE 3.2: *SEM of a FIB milled trench in a Si AFM pyramid with thermally grown SiO_2 and sputtered Al (image courtesy of Dr Yuan Zhang).*

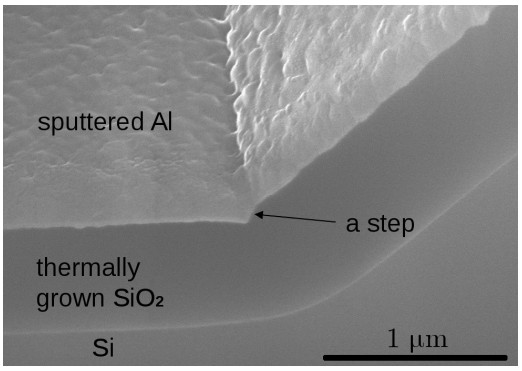


FIGURE 3.3: *SEM of a cross section of a Si AFM pyramid with thermally grown SiO_2 and sputtered Al with indicated step in SiO_2 layer (image courtesy of Dr Yuan Zhang).*

aforementioned oxidation issues associated with 3 dimensional structures, it was decided to use such a PECVD SiO_2 film.

As explained in section 2.2, PMMA was the only choice of resist for high resolution pattern transfer on an AFM pyramid. This resist has low selectivity over SiO_2 in CHF_3 plasma (about 1 : 1.3 [128]). An extensive study on using PMMA as a dry etch mask for etching of SiO_2 was presented by *Chinn* et al. [126]. It was found that the selectivity of PMMA over SiO_2 when dry etching in CHF_3 plasma depends on power and as a consequence the selectivity will non-linearly vary from 1 : 1.4 for higher power (120 W) to 1 : 2.7 for lower power (50 W).

Assuming the lowest stated PMMA selectivity (1 : 1.3) over SiO_2 in CHF_3 plasma means that in order to mask successfully 300 nm thick SiO_2, at least 230 nm of PMMA is required. By taking average thickness of 1.5% 2041 PMMA resist at 65 nm (see section 2.2) this mask would consist of 4 float coating layers. Such a thickness still does not compensate for any cracks in the resist, to which PMMA is prone during float coating. Due to this $8 - 9$ layers of the resist would be required. However, this significantly increases the time of resist preparation and the minimum size of achievable features.

In order to avoid complex, dry etch process optimization, to allow processing with thinner resist and to make the process independent of the thickness of the material to be etched, the decision was made to use an intermediate, metallic layer as a hard mask for etching SiO_2. In this way, theoretically, a single, float coating layer of the crack-free resist compatible with the metal etchant could withstand the wet etch process as a mask. However, cracks in the resist occur and as described in section 2.2 the float coating resist layer thickness varies, which affects the required dose. To maintain the same dose across the 3" wafer during lithography with PMMA and to compensate for the cracks in the

metal	native oxide thickness[a] [monolayers]	etchant	etchant compatible with PMMA
aluminium [129]	$\gg$ several [130]	$H_3PO_4 : H_2O : HNO_3$ [131]	yes
chromium [126]	several [130]	MS8 chrome etchant[b] [130]	yes
nichrome [132]	several [133]	MS8 chrome etchant[c]	yes
nickel [134]	several [130]	diluted HNO_3 [131]	yes [135]

[a] at room temperature
[b] consists of acetic acid and ceric ammonium nitrate
[c] etches 60/40 $NiCr$

TABLE 3.2: *Metals commonly used as a dry etch mask for etching SiO_2 in CHF_3 plasma and considerations for selection as an intermediate layer.*

resist, the number of layers was kept at 5, with PMMA drops distributed in the form of an equilateral pentagon (as explained in section 2.2).

Transferring pattern into the metallic film can be accomplished using:

- lift-off process
- wet etch process

Instead of etching the metallic layer, lift-off process could provide e.g. sharper edges of the features, better control of feature size between design and patterned resist and smaller features possible to fabricate. Sharper edges do not suffer from random indentations as wet etched edges do. So they do not require a large error margin during alignment between layers. Better control of feature size can result in greater flexibility during the design stage. However, because of the fact that PMMA is a positive resist, for the lift-off process the whole wafer apart from the small designed features has to be written with electron beam. Such a solution consumes too much time and resources, as doing this with the largest available beam spot size would take more than 24 *hours* to expose. Also the extreme effects of proximity from the large exposed area would result in an unacceptably small exposure latitude.

Many materials oxidise forming what is known as native oxide - a few monolayers of oxide, which become a stopping barrier for further oxidation process at room temperature. Due to this out of metals commonly used as dry etch masks (presented in table 3.2) aluminium was rejected. Al_2O_3 has lower etch rate than pure Al in the etchant, so from run to run a variation in thickness of oxidized layer of Al introduces change in the induction time when wet etching, which may affect the process reproducibility. Chromium was not available in the laboratory. As a consequence the choice was reduced to $NiCr$ and Ni. Either could have been chosen, but the availability of the ready to use etchant influenced the decision to select $NiCr$.

Due to high melting point (about 1400 $^{\circ}C$ [136]), high selectivity in dry etch processes [137] and resistance to oxidation [130], this alloy is often used as a masking material for dry etch processes using $SiCl_4$, SF_6 or CHF_3 to etch Si, $SiGe$, SiO_2, SiN_x and $III-V$.

3.2 NiCr and grass effect

The following process for fabricating a patterned SiO_2 layer using $NiCr$ (mask for dry etch) and PMMA (mask for wet etch of $NiCr$) was proposed:

1. deposit 300 nm of PECVD SiO_2
2. evaporate 75 nm of $NiCr$
3. apply PMMA resist
4. electron beam lithography and development
5. O_2 ash in barrel asher at 40 W for 30 s to remove resist residues
6. etch $NiCr$ with MS 8 Chrome etchant[1] for 55 s
7. rinse in R.O. water for 2 min while gently stirring
8. N_2 blow dry
9. solvent cleaning (acetone, methanol, IPA)
10. dry etch processing - (see table E.1 and E.4)

PROCESS 3.1: Initial fabrication process used for fabrication of SiO_2 mask (needed for diffusion process), which results in "grass" effect.

This process results in what is commonly referred to as "grass" [138] (see figure 3.4). Tiny pillars made of SiO_2 are formed during dry etch processing. This effect is a consequence of micro masking - some residual material masks SiO_2 and prevents it from being etched.

Due to the fact that under SEM there was no visible, obvious contamination (see figure 3.5), there were three possible sources of this micro masking:

- residue left after wet etching of $NiCr$ (a similar issue happens with development of e.g. PMMA resist [104])
- redeposition of a masking $NiCr$ during dry etch process [107]
- formation of polymeric film during dry etch process due to decomposition products of etching gas [107]

[1] etch rate - 100 nm / min

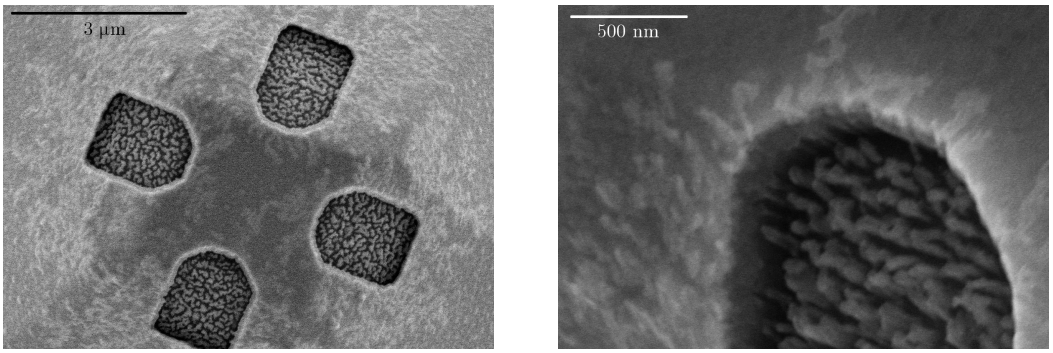


FIGURE 3.4: *SEM images of dry etched SiO_2 windows with "grass" problem.*

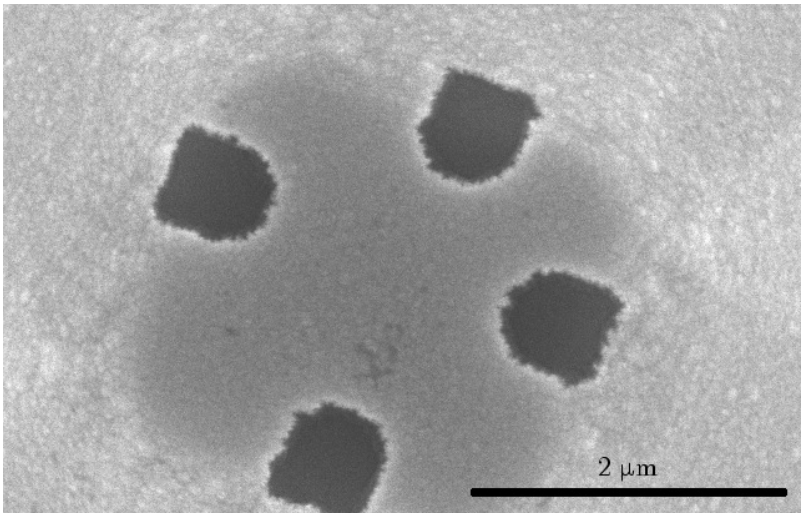
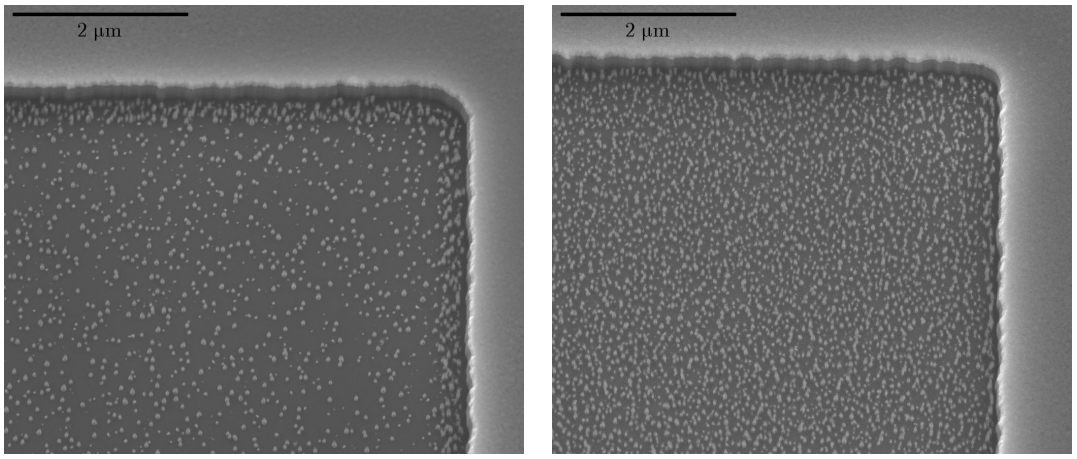


FIGURE 3.5: *SEM of a sample processed to the stage just before dry etching of* 300 *nm of SiO_2 with patterned,* 75 *nm of $NiCr$ as a mask.*

To determine the source of the "grass" a series of experiments was conducted. Two parameters were varied: gases used for dry etch and wet etch post-processing. As described in section 2.3 varying the type of dry etching gases changes the nature of the dry etch process from more chemical etching to more physical etching, so $CHF_3 + Ar$ and CHF_3 gases were used. This could indicate if the issue was directly related to dry etch process. Regarding wet etch post-processing the following changes in the rinsing procedure were attempted:

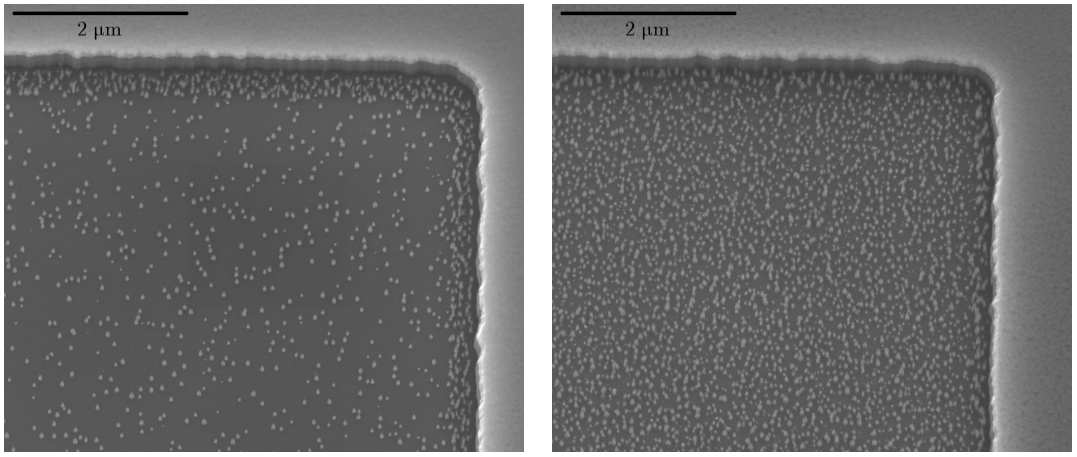
7a) rinse in R.O. water for 10 *s* (see figure 3.6)
7b) rinse in R.O. water for 10 *min* (see figure 3.7)
7c) rinse in R.O. water for 10 *min*, rinse in IPA for 5 *min* (see figure 3.8)

PROCESS 3.2: Proposed modifications of step number 7 of process 3.1 in order to determine the source of "grass" effect.



(a) *Dry etched using* CHF_3 (b) *Dry etched using* $CHF_3 + Ar$

FIGURE 3.6: *SEM images of corners of* 1 *mm square patterns processed following the proposed process with step 7a).*



(a) *Dry etched using* CHF_3 (b) *Dry etched using* $CHF_3 + Ar$

FIGURE 3.7: *SEM images of corners of* 1 *mm square patterns processed following the proposed process with step 7b).*

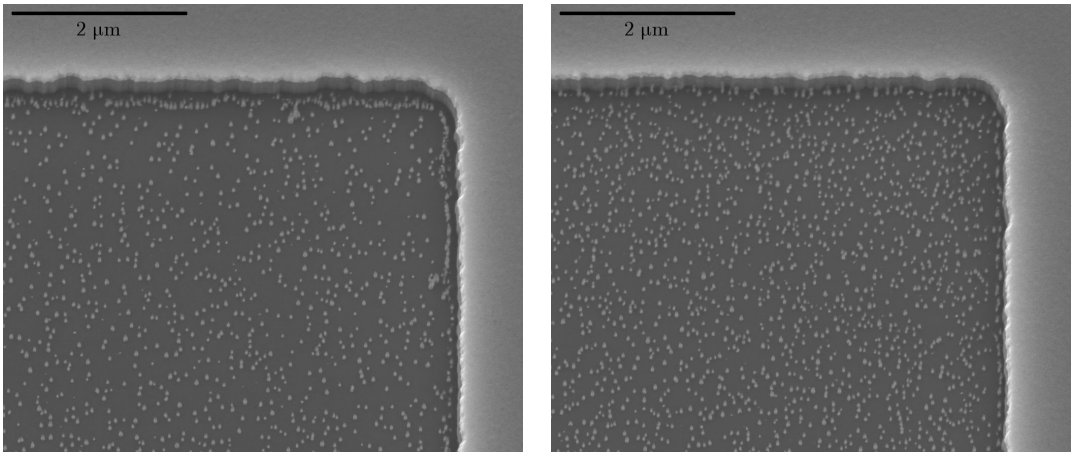
From the SEM photos presented in figures 3.6, 3.7, 3.8 it can be observed that:

- the density of "grass" is visibly higher for samples processed with the dry etch employing $CHF_3 + Ar$ gases, probably due to greater anisotropy (compared to CHF_3 processing) resulting in a smaller undercut [139]
- there is no visible difference between the results of the samples processed with 10 s and 10 min R.O. water rinse
- in the figure 3.8(b) there is a lower density of "grass" compared to figure 3.7(b)
- there is a lower density of "grass" close to the edge of the windows (see figures 3.7(a) and 3.8(a))

Based on these findings, one more test was conducted using:

7d) rinse in IPA for 5 *min* .

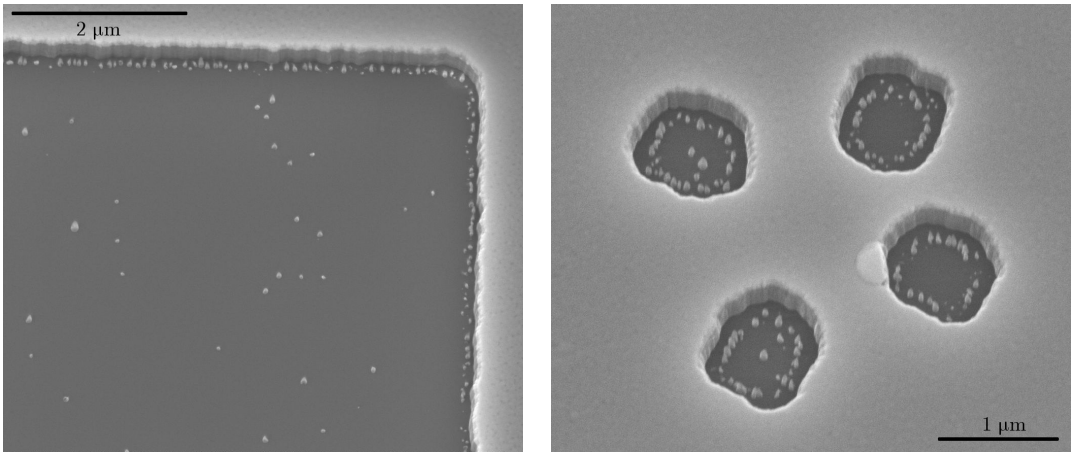
PROCESS 3.3: Another proposed modification of step number 7 of process 3.1 in order to determine/eliminate the source of "grass" effect.



(a) *Dry etched using* CHF_3 (b) *Dry etched using* $CHF_3 + Ar$

FIGURE 3.8: *SEM images of corners of* 1 *mm square patterns processed following the proposed process with step 7c).*

The inspection of the sample (see figure 3.9) revealed the lowest amount of grass compared to all of the previous tests. Only a few, random pillars and some more along the edge of the pattern could be observed. The edge pillars were of concern since this process was being developed for small (approximately $400 - 600\ nm$) features (see figure 3.9(b)).



(a) *SEM of a corner a of a* 1 *mm square pattern.* (b) *SEM of small features.*

FIGURE 3.9: *Sample processed following the proposed process with step 7d) and dry etched in* CHF_3 *plasma.*

To investigate the composition of the micro masking material energy-dispersive X-ray (EDX) spectroscopy was performed on a sample containing many pillars (presented in figure 3.6(b)). Since under SEM there was no visible contamination (see figure 3.5), the measurement required a low energy (5 keV), electron beam in order to investigate the surface, residual layer.

The electron penetration depth can be calculated by using Kanaya-Okayama formula [140]. For the Si substrate at the incident energy of 10 keV the maximum penetration depth is $R = 1500\ nm$, whereas for 5 keV this depth becomes $R = 470\ nm$. Both of these numbers are large when compared to thin residual layer ($1's - 10's\ nm$). However, by lowering the electron beam energy, the residual layer thickness becomes large enough portion of the maximum range depth and the residual layer measurement can be obtained. Due to the integration time of a weak signal, it took 1 *hour* to obtain the result (figure 3.10).

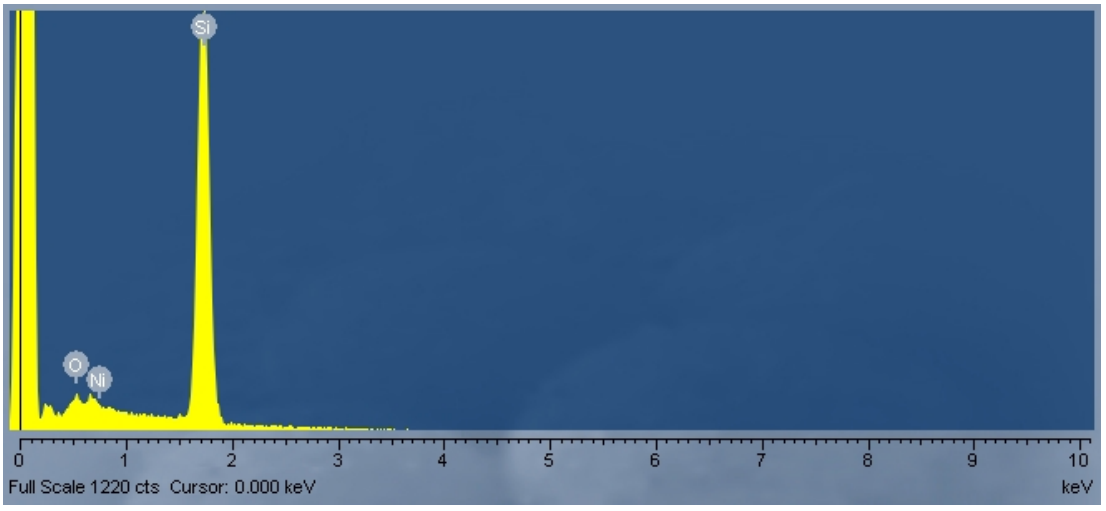


FIGURE 3.10: *EDX result of the sample with intensive "grass" issue*

The outcome of the measurements indicated three elements:

1. Si - expected to be seen because the substrate is made of it and the target of this dry etch process is to reach it
2. O - expected to be seen due to the "grass"; the dry etched material (the material of the pillars) was $Si\mathbf{O}_2$
3. Ni - detection of this element was unexpected, however, it could act as the masking material (see table 3.2) and it was involved in the processing of the samples by using $NiCr$ as a hard mask for dry etching

The appearance of Ni on the EDX plot suggested that it was not etched during the wet etch step. MS8 chrome etchant that is used to etch $NiCr$ consists of ceric ammonium nitrate (CAN), acetic acid and water. As explained in [137] CAN is a strong oxidizing agent and it reacts with Cr in an acidic (H^+) solution following a chemical reaction described by equation 3.1.

$$3\ Ce(IV)(NH_4)_2(NO_3)_{6(aq)} + Cr_{(s)} \underset{H^+}{\rightarrow} Cr(III)(NO_3)_{3(aq)} + 3\ Ce(III)(NH_4)_2(NO_3)_{5(aq)} \quad (3.1)$$

The products of this reaction are chromium nitrate and ceric ammonium nitrate with reduced oxidation state. Both are soluble in water. The acidic solutions can be achieved with acids such as perchloric, nitric or acetic acid [141]. The chromium etchant based on acetic acid has a short shelf life (3 months) when compared to the chromium etchants based on other acids (12 months), however, it provides more consistent etch rate [137] and less undercut of photoresist [137].

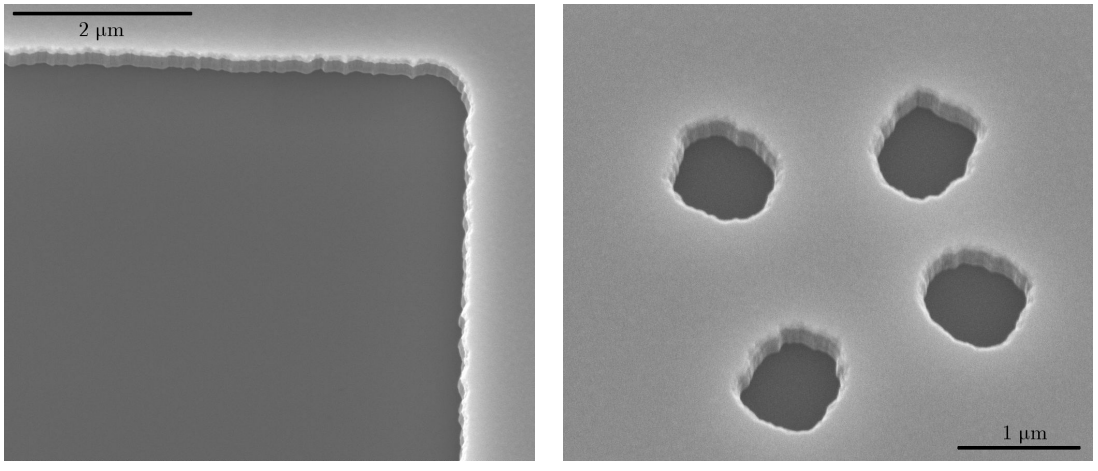
MS8 chrome etchant, as described above, does etch chromium, but it does not etch nickel. The 60/40 $NiCr$ alloy used is etched by this solution due to sufficient proportion of Cr. When Cr is etched, Ni particles float away and can re-deposit on the sample surface. The Ni particles that are directly in contact with SiO_2 are not etched and cause micro-masking. Based on the previous results the adhesion between SiO_2 and those Ni particles seems to be relatively weak. The experiment indicated that IPA lifted off more Ni particles than R.O. water, which can be attributed to over 3 times lower [142] surface tension [143] of IPA in room temperature than R.O. water.

Due to the fact that MS8 chrome etchant does not etch nickel and that IPA cannot lift off all of the Ni particles, an extra step was introduced in order to eliminate the Ni residues. As a result the process is as follows:

1. deposit 300 nm of PECVD SiO_2
2. evaporate 75 nm of $NiCr$
3. apply PMMA resist
4. electron beam lithography and development
5. O_2 ash in barrel asher for 30 s
6. etch $NiCr$ with MS 8 Chrome etchant for 55 s
7. rinse in IPA for 5 min
8. blow dry
9. solvent cleaning (acetone, methanol, IPA, R.O. water) to strip resist
10. N_2 blow dry
11. etch Ni residues in nitric acid (3:7) R.O. water for 1 min
12. rinse in R.O. water for 3 min
13. rinse in IPA for 2 min
14. blow dry
15. dry etch processing - (see table E.1)

PROCESS 3.4: Final fabrication process used for fabrication of SiO_2 mask (needed for diffusion process), with eliminated "grass" effect caused by micromasking.

Following this modified process resulted in features free from "grass" (see figure 3.11). In this way it was proved that the "grass" effect was a consequence of the preparation of the sample for dry etching rather than the dry etch process itself.



(a) *SEM of a corner a of a* 1 *mm square pattern.* (b) *SEM of small (under* 1 *µm) features.*

FIGURE 3.11: *SEM of patterns processed as indicated in modified process (etched using* $CHF_3 + Ar$*).*

3.3 Overhang on edge of pyramid apex

During development of the triple mask (see section 3.1), a feature was observed (see figure 3.12) which appeared to be a crack located on the edge of the pyramid apex in the $NiCr$ mask. This was observed before applying PMMA resist for further processing. Stripping $NiCr$ and underneath PECVD SiO_2 masks revealed the AFM pyramid tip edges were sharp and extended (see figure 3.13).

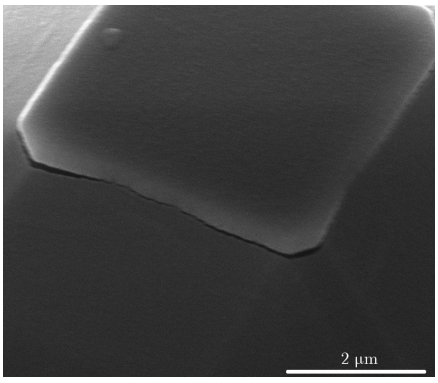


FIGURE 3.12: *SEM of a crack in NiCr mask along the edge of the AFM pyramid apex.*

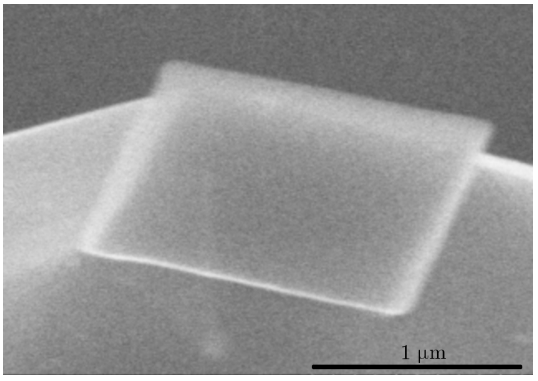
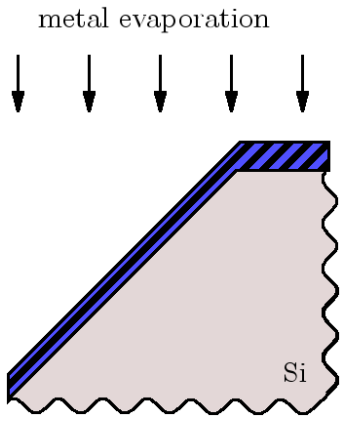
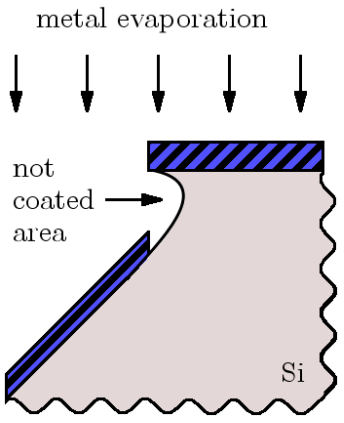


FIGURE 3.13: *SEM of a tip of AFM pyramid after defining it with wet etch process and removing wet etch hard mask.*

Evaporation of metal on a properly shaped, functionalized AFM tip (see figure 3.14(a)) forms a continuous film. The same process performed on an "hourglass" shaped tip results in the aforementioned cracks (see figure 3.12). This happens due to directionality of the metal evaporation process, which does not reach places under overhangs (see figure 3.14(b)).



(a) *All areas of a regular shape apex are coated despite the directionality of the metal evaporation process.*



(b) *Due to the directionality of the metal evaporation process, areas under the overhang remain uncoated.*

FIGURE 3.14: *Diagram presenting evaporated metal layer on different apex shapes of the functionalized Si AFM tips.*

In this case the lack of continuous $NiCr$ film results in cavities in the dry etch mask. Dry etching of SiO_2 using such a deteriorated mask can lead to opening windows in SiO_2 mask in places where it is prohibited. Because there is no material to mask the diffusion process, the designed diffused regions merge and as a consequence the transistor fails to work.

This extended, sharp edge is believed to come from the wet etching of Si in KOH etchant. The LPCVD Si_3N_4 layer, which is used as a masking material for this process, is known to introduce stress in silicon technology [144]. The overhang problem is attributed to film-edge stress, as the overhang follows the line of the patterned Si_3N_4 layer (see figure 3.15). The influence of the stress on the anisotropic etching process has been described [145].

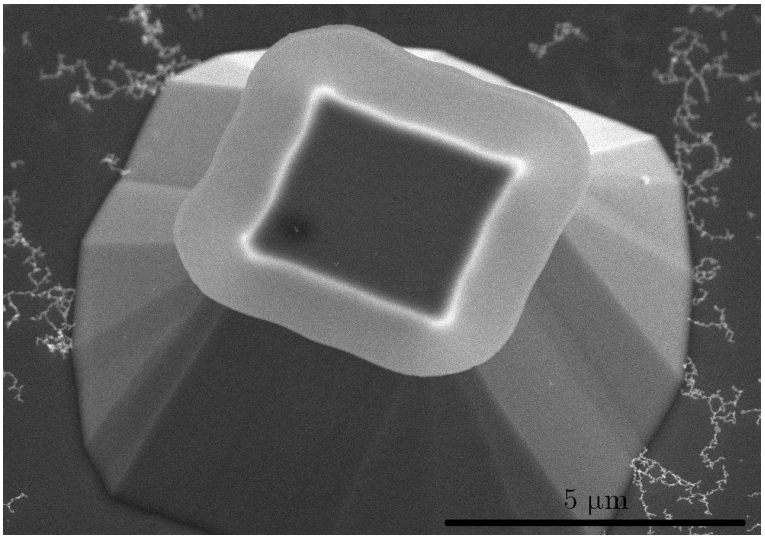


FIGURE 3.15: *SEM of an AFM pyramid with hard mask after KOH etch. The white, square-shaped, electron charging like line indicates the pyramid apex.*

This issue is irrelevant e.g. in case of SNOM probes [88] or thermal probes [84]. Even though Si is the base material for fabricating those AFM probes, the final cantilever is made of wet thermally grown SiO_2 or LPCVD Si_3N_4 respectively. After fabricating the actual devices on the dielectric layers, the Si base supporting the cantilevers is etched away in the final release etch.

In case of Si cantilevers using LPCVD Si_3N_4 as a mask for KOH etch, the same issue was already observed [146]. However, switching to 1 μm of wet thermally grown SiO_2 solved the issue in this case [90].

Having 50 Si wafers already coated with 40 nm of thermally grown SiO_2 and 60 nm of LPCVD Si_3N_4, it was decided to investigate the possible workaround rather than reprocessing the substrates.

The first taken approach was to consume the Si surface together with the defects by wet thermal oxidation. The proposed solution was realized with the following process:

1. grow SiO_2 in water vapour (see table H.1)
2. strip SiO_2 in buffered 10% HF for 3 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry
5. hot plate bake at 180 ^oC for 5 min
6. deposit 300 nm PECVD SiO_2
7. evaporate 75 nm of $NiCr$
8. inspect under SEM

PROCESS 3.5: Fabrication process used for an attempt I of elimination of overhang at the apex of AFM tips with thermal SiO_2 growth.

Two samples were processed. One had 300 nm and the other 600 nm of wet thermally grown SiO_2. The results of SEM inspections are presented in figures 3.16 and 3.17 respectively.

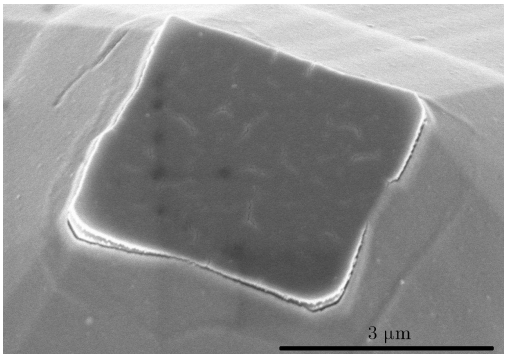


FIGURE 3.16: *SEM of a crack in NiCr mask along the edge of the AFM pyramid apex. Sample processed with* 300 *nm of wet thermally grown* SiO_2.

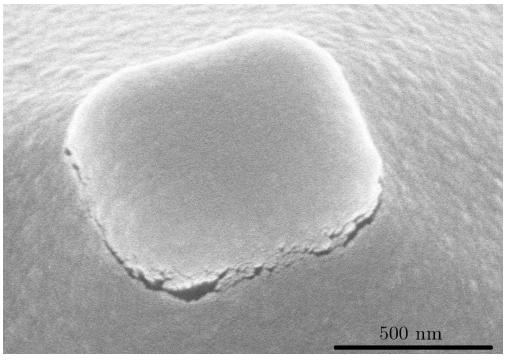


FIGURE 3.17: *SEM of a crack in NiCr mask along the edge of the AFM pyramid apex. Sample processed with* 600 *nm of wet thermally grown* SiO_2.

Both approaches with different thicknesses of thermally grown SiO_2 failed to improve the tip edge profile. As a consequence another attempt was made using KOH etchant.

The KOH solution is an anisotropic etchant for Si. The $< 100 >$ crystallographic plane is etched by KOH with a certain etch rate, which is dependent on the KOH concentration, the temperature and the concentration of IPA [87]. When etching $< 100 >$ plane of a Si substrate with a specifically designed (see subsection 1.4.2) dielectric mask in KOH etchant, $< 313 >$ plane forms a slope.

Once the pyramid is fabricated and the dielectric layers are stripped, putting the sample into KOH solution for more etching results in the following. All areas formed by $< 100 >$ and $< 313 >$ planes are etched. However, the edge where both planes meet, previously protected by the mask, is now the starting point for a formation of a fast etching $< 310 >$ plane. Given enough time in the KOH solution, the newly formed etch planes planarize the substrate and eventually consume the whole pyramid.

An attempt to remove the overhang using this phenomenon was made. After fabricating the AFM pyramids in KOH etchant with SiO_2 and Si_3N_4 as etch mask, a test sample was processed using the following process:

1. strip both dielectric layers in 48% HF for 5 *minutes*
2. rinse in R.O. water for 5 *min*
3. use the same KOH solution and etch without any mask for 60 *seconds*
4. rinse in H_2SO_4 $(1:9)$ with R.O. water for 1 *minute*
5. rinse in R.O. water for 5 *min*
6. N_2 blow dry
7. inspected under SEM (see figure 3.18)

PROCESS 3.6: Fabrication process used for an attempt II of elimination of overhang at the apex of AFM tips using additional KOH etching step.

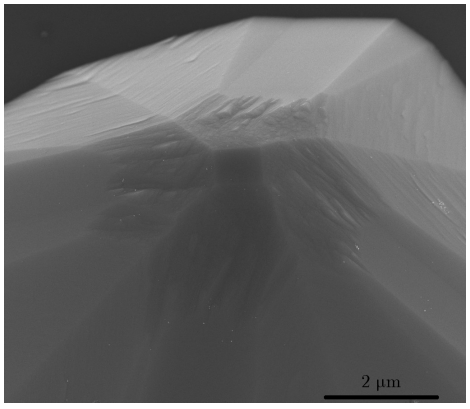


FIGURE 3.18: *SEM of an AFM pyramid - the edge processed in KOH solution for* 1 *min.*

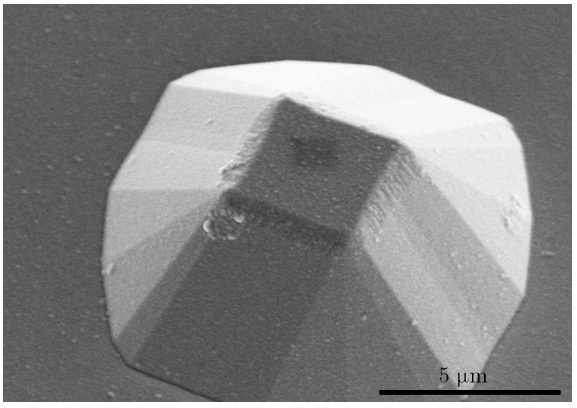


FIGURE 3.19: *SEM of an AFM pyramid - the edge processed in KOH solution for* 20 *s and then coated with* 300 *nm of PECVD* SiO_2 *and* 75 *nm of evaporated NiCr.*

The sharp edge of the pyramid tip was consumed by the KOH solution. The 1 *minute* etch proved to be too long since the areas of $< 310 >$ plane are large and the tip was consumed significantly. As a consequence the edge etch time was reduced to 20 *s* and the final process is as follow:

1. strip both dielectric layers in 48% HF for 5 *minutes*
2. rinse in R.O. water for 5 *min*
3. use the same KOH solution and etch without any mask for 20 *seconds*
4. rinse in H_2SO_4 $(1:9)$ with R.O. water for 1 *minute*
5. rinse in R.O. water for 5 *min*
6. N_2 blow dry
7. baked on a hot plate at 180^oC for 5 *min*
8. deposit 300 *nm* of PECVD SiO_2
9. evaporate 75 *nm* of $NiCr$
10. inspected under SEM

PROCESS 3.7: Final fabrication process used for elimination of overhang at the apex of AFM tips using additional KOH etching step.

Sample inspection revealed no cracks on the edge of the pyramid tip (see figure 3.19).

3.4 Diffusion challenges on AFM pyramid

There are three mayor ways of thermal introduction of impurities into a silicon substrate. They differ based on the source of impurities:

- a source in a gaseous or vapour form at high temperature - due to its ubiquitous nature this method is the preferred one to introduce the impurities into 3 dimensional structures like AFM pyramids. The impurities can reach the bare substrate irrespective of an angle of the slope.
- a doped oxide - e.g. applied by spinning, which suffers from the same issue as a resist spun on such a structure (see subsection 2.2).
- ion implanted layer - ion implantation is a directional process that for this application fails due to the conformal coating of a masking material in various places, since the effective thickness of the masking material depends on the angle of the slopes.

Due to the lack of a furnace permitting use of the first method, a decision was made to use a doped oxide as the source for impurities. The method of application had to be modified if not changed in order to eliminate the problem of covering the pyramid with the oxide source. A solution was proposed to use multiple layers of spin-on dopant applied by spinning. This raised two more issues:

1. an application of spin-on dopant requires a 45 *minute* bake on a hot plate at 105^oC in order to evaporate a solvent, followed by 30 *minute* bake at 550^oC in presence of O_2 in order to burn polyvinyl acetate. Only then is the film solid and does not redissolve when more spin-on dopant solution is added.
2. spinning of the spin-on dopant at 2000 *rpm* results in film thickness of approximately 200 ± 10 *nm* (measured with Dektak 6M). In order to build up enough of spin-on dopant to completely cover the 6 μm high pyramid 30 layers are required. Combined with 75 *minutes* of a thermal cycle after each layer is spun, the process is unfeasibly time consuming.

As a result other solutions were investigated. The elegant solution of float coating known from a PMMA application does not work for spin-on dopant due to its hydrophilic properties. Since the required diffusion is relatively shallow ($100 - 150$ *nm*) the constraints for doped oxide thickness are minimal. What is more, the uniformity of the coating is not important, since it is not the whole layer, but the interface with the substrate that takes part in the diffusion process. As a consequence, an attempt was made to apply the spin-on dopant and leave it to dry up without spinning. After preparation of the dopant layer, the sample was baked in the RTA (see table I.1). The surface of the doped oxide layer was cracked and suffered from poor adhesion to the substrate (see figure 3.20).

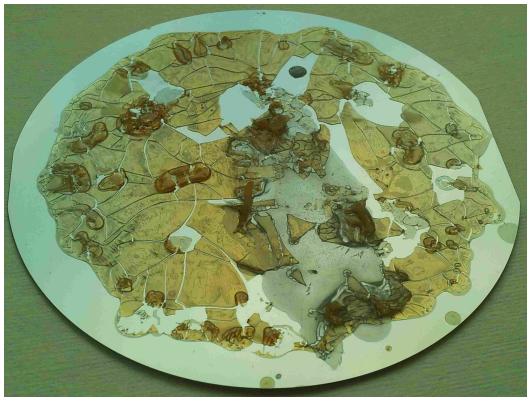


FIGURE 3.20: *Photo of a substrate with a spin-on dopant poured onto the substrate which has been left to dry up. After the thermal process (see table I.1) cracks and adhesion issues in the doped oxide layer can be observed.*

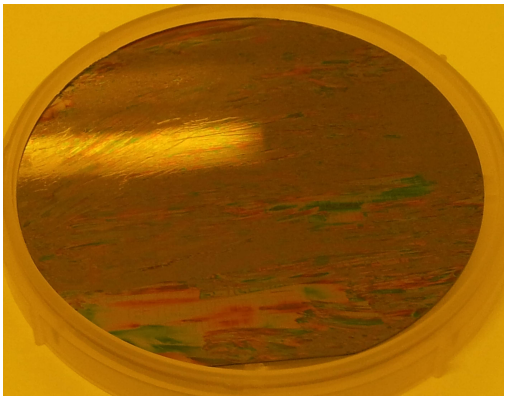


FIGURE 3.21: *Photo of a substrate with AFM pyramids after applying the dopant using a brush and conducting full diffusion process. No cracks and adhesion issues in the doped oxide layer can be observed.*

Due to the fact that a thin spun oxide layer does not crack, this behaviour is believed to be caused by the internal stress of the doped oxide. As a result a method of application had to be modified in order to limit the thickness of the oxide layer. This was achieved by simple mechanical application of the spin-on dopant using a brush. After running a

full diffusion process (see point IX in appendix C), the doped oxide layer is free from cracks and no adhesion issue is observed (see figure 3.21).

The speed of application of the spin-on dopant onto the substrate influences the finish of the layer. If the application of the dopant takes approximately 3 *seconds* to cover the whole 3" wafer, the resulting layer is shiny. In case of the application taking longer, the layer results in a frosted finish. This is attributed to the thickness of the layer and the air bubbles in the spin-on dopant solution. When the application is slow, more time is given for the solution to move from the brush to the substrate which results in a thicker layer.

When the film is thin, the air bubbles have a short distance to travel to the film surface to be freed before the film solidifies. In case of a thicker layer, the air bubbles have a longer distance to travel through the film and it solidifies before the bubbles are freed. In use the finish of the doped oxide layer was not found to have any influence on the diffusion process.

3.5 Ordering of diffusion processes

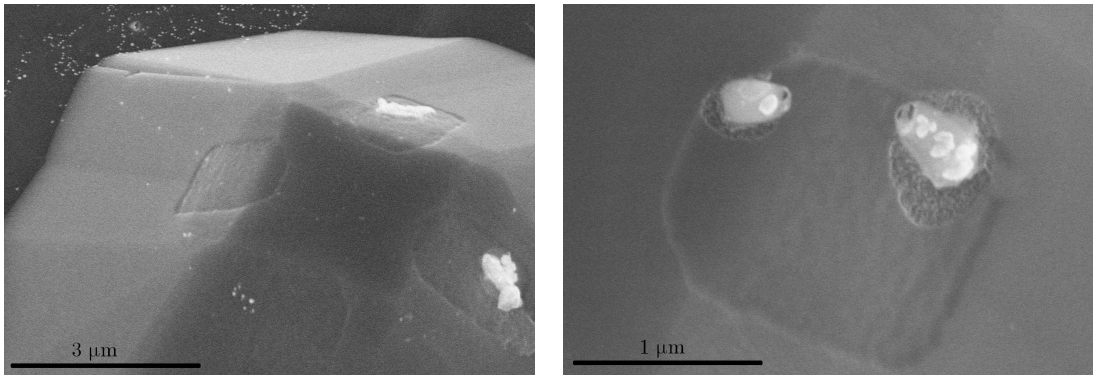
A standard approach to run two diffusion processes with boron and phosphorus is to run the boron process first and then phosphorus. This is dictated by the higher diffusivity of phosphorus. When the phosphorus diffusion process is run, boron dopant, located already in the substrate, diffuses less than phosphorus would in the situation when the two processes are swapped.

For this project the order has been reversed in order to minimize the lateral redistribution of the four p-type regions that are very close to each other on the AFM pyramid. Phosphorus diffusion is run to form a back contact to the substrate and it is located away from the other diffused regions. The back surface concentration of the phosphorus doped region is high ($5 \cdot 10^{20}$ $\frac{atoms}{cm^3}$) and even after additional boron diffusion process, it is still high enough ($2 \cdot 10^{20}$ $\frac{atoms}{cm^3}$) [147] to form a good ohmic contact, so this process is not critical.

In order to minimize the dopant redistribution during the growth of the gate thermal oxide, the temperature can be lowered. Growing dry SiO_2 at a temperature of 775^oC gives approximately 10 nm of lateral boron dopant redistribution [102], [147]. If the two processes are run as standard, the lateral redistribution of the boron dopant is around 70 nm for each region [102], [147], resulting in a risk of shorting the source-drain diffused regions.

3.6 Phosphorus contamination

During the fabrication of the devices a characteristic form of contamination appeared at random on the substrates. This contamination occurred 3 times within one year. It can be observed in the figure 3.22, which is a typical example.

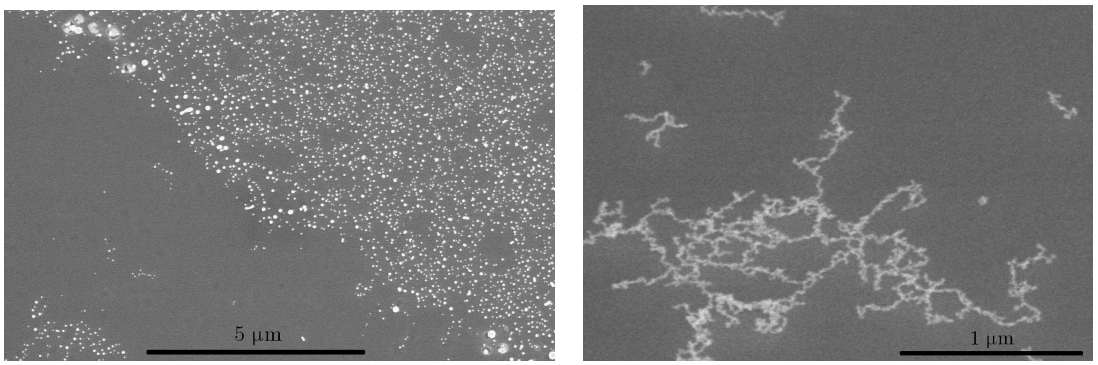


(a) *Contamination located on and around an AFM pyramid.* (b) *Contamination located directly over a boron diffused area.*

FIGURE 3.22: *SEM of the unidentified contamination.*

In the figure 3.22(b) the contamination consumed some of the Si around it. Most probably this was caused during the high temperature (900^oC) process of diffusion, however, the issue was discovered at a late stage of the device fabrication. One of the samples previously inspected under SEM revealed very similar contamination (see figure 3.15). In this case the contamination was also distributed at random across the substrate, but instead of spots (see figure 3.23(a)), fibre-like shapes could be observed (see figure 3.23(b)). This difference could be explained by the fact that this sample was at an early stage of the device fabrication. This means it had not been treated thermally yet. The implication of this observation was that the source of contamination was not associated with the diffusion process. What is more, its presence in figure 3.15 indicated that the AFM pyramids had just been fabricated in Si using KOH solution, but that the hard mask was not removed yet. This information limited the search for the contamination source to:

1. the wet etch kit - due to very limited number of users, the random appearance of the contamination and thorough cleaning before and after use, the possibility of the wet etch kit being the source of the contamination was minimum.
2. KOH pellets and sulphuric acid - if the KOH pellets or sulphuric acid were contaminated the problem would not appear at random. Due to this, the chance of the reactants being contaminated was also felt to be small.
3. beakers used in processing - out of all, the beakers were the most suspect since they are used by many users for different processes.



(a) *Sample treated thermally.*

(b) *Sample not treated thermally. Other laboratory users also observed such contamination occasionally.*

FIGURE 3.23: *SEM of the unidentified contamination.*

In order to investigate the composition of contamination, EDX spectroscopy was conducted. The result (see figure 3.24) of inspection indicated presence of phosphorus.

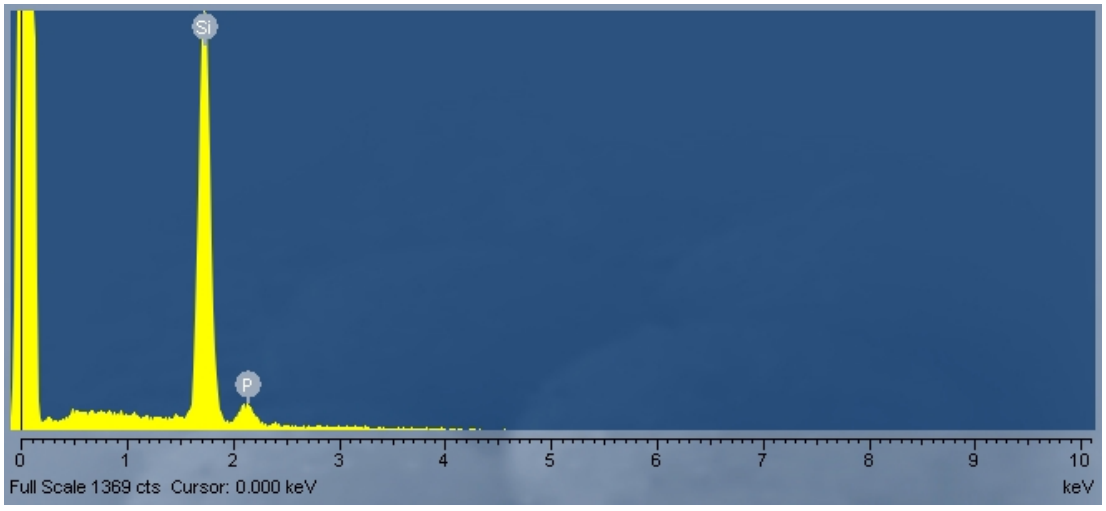


FIGURE 3.24: *EDX result of the sample area presented in figure 3.23(a).*

Phosphorus dissolves in hot water [131], so an experiment was performed to ultimately confirm the element. The sample was put into R.O. water at 95^oC for 5 min prior to thermal treatment and as a result the contamination was removed.

In the laboratory in each room, one set of beakers in common is used for all processes. In the room for KOH processing, HF acid is used as well - e.g. for stripping native oxide before KOH etching. In the same room, HF acid is also used for stripping phosphoro- and borosilica films after diffusion processes, both of which are used in this project. As the described problem indicates, phosphorus dopant is not etched in HF acid, so the contamination could come from substrate processing done previously. This raised the question as to whether boron can contaminate the substrate in the same manner, however, boron is etched by HF acid [131].

Because the contamination came from the beakers and the phosphorus diffusion process, all of the beakers were replaced and a separate set of beakers only for phosphorosilica etch was assigned. After the etch process, each substrate is put into R.O. water at 95^oC for 5 min, in order to eliminate the phosphorus located on the sample. From then on (a period of approximately 4 months) the contamination was not observed again.

3.7 Slow Si dry etch

For the purpose of testing the reverse polarized diode concept for the Hall bar a slow silicon dry etch process had to be established for reasons explained in section 4.1 and subsection 4.1.3. For this purpose the BP80+RIE machine was used using SF_6/N_2 chemistry at 10 W [148]. For each test two samples were processed with etching time of 15 and 30 minutes.

Two is the minimum number of points to calculate real material etch rate and induction time. Two measurement points do not provide any information about variations in etch rate, however, they can be used to determine the etch rate range. The 30-minute etching time was selected to be equal to the longest standard run on this tool in the dry etch laboratory at Glasgow. After each 30 minutes of the dry etch machine processing time, the machine is cleaned using O_2 ash process (power 100 W, O_2 flow rate 50 $sccm$, pressure 50 mT, duration 30 $minutes$). The shorter etching time should be significantly shorter than the first one and it should be close to the induction time in order to give the largest possible difference in etch depth after induction, minimizing the influence of the etch rate variation. Due to the use of a low power etch, which translates into low etch rate, the shorter etching time was set to 15 minutes in order to be sure the etch is longer than the induction time.

The remaining parameters (pressure and flow rate) were varied in order to achieve low etch rate in the region of a couple of nanometres per minute.

All of the test samples were prepared using the following procedure:

1. rinse in MS 20D Stripper $(1:1)$ R.O. water for 15 min
2. rinse in running R.O. water for 5 min
3. N_2 blow dry
4. spin primer 80/20 at $4,000$ rpm for 5 s
5. spin s1818 resist at $4,000$ rpm for 30 s
6. bake at 90 ^oC for 30 min
7. exposure - hard contact, exposure time 5 s
8. rinse in Microposit Developer Concentrate $(1:1)$ R.O. water for 75 s
9. rinse in R.O. water for 3 min
10. N_2 blow dry
11. barrel asher - 40 W for 60 s
12. dry etch
13. solvent cleaning (acetone, methanol, IPA, R.O. water) to strip resist
14. barrel asher - 80 W for 5 min
15. Veeco Dektak 6M profiler measurement of etch depth

PROCESS 3.8: Initial fabrication process used for establishing etch rate of slow Si dry etch.

The first two samples were etched with a flow rate of 10 $sccm$ and 40 $sccm$ for SF_6 and N_2 respectively, with a pressure of 30 $mTorr$ [148]. The resulting etch depths were 850 nm for 15-minute etch and 740 nm for 30-minute etch. As a result of this inconsistency the experiment was repeated and the resulting etch depths were 160 nm and 790 nm for 15 and 30-minute etch, respectively. The fabrication procedure was analysed in order to find the reason for the observed variation of the results. The barrel asher was suspected as the source of contamination. The barrel asher step in the procedure is there to remove residues of the resist after development.

Optical Emission Spectroscopy (OES) was performed on the barrel asher (see figure 3.25). Even though peaks of oxygen are visible, there are more elements visible with the intensity of the same order of magnitude. Apart from the O_2 ash the sample gets sputter coated with different elements including Ti, Cr or Al.

The barrel ashing step number 11, was changed for the dry etch machine to remove resist residues. The parameters of this process are: power of 10 W, O_2 flow rate of 50 $sccm$ and pressure of 50 $mTorr$ for 1 $minute$. This change resulted in the depth measurements becoming consistent to $\pm 10\%$ (see table 3.3) due to the fact that, unlike barrel asher, the dry etch tool is cleaned after every 30 minutes of processing.

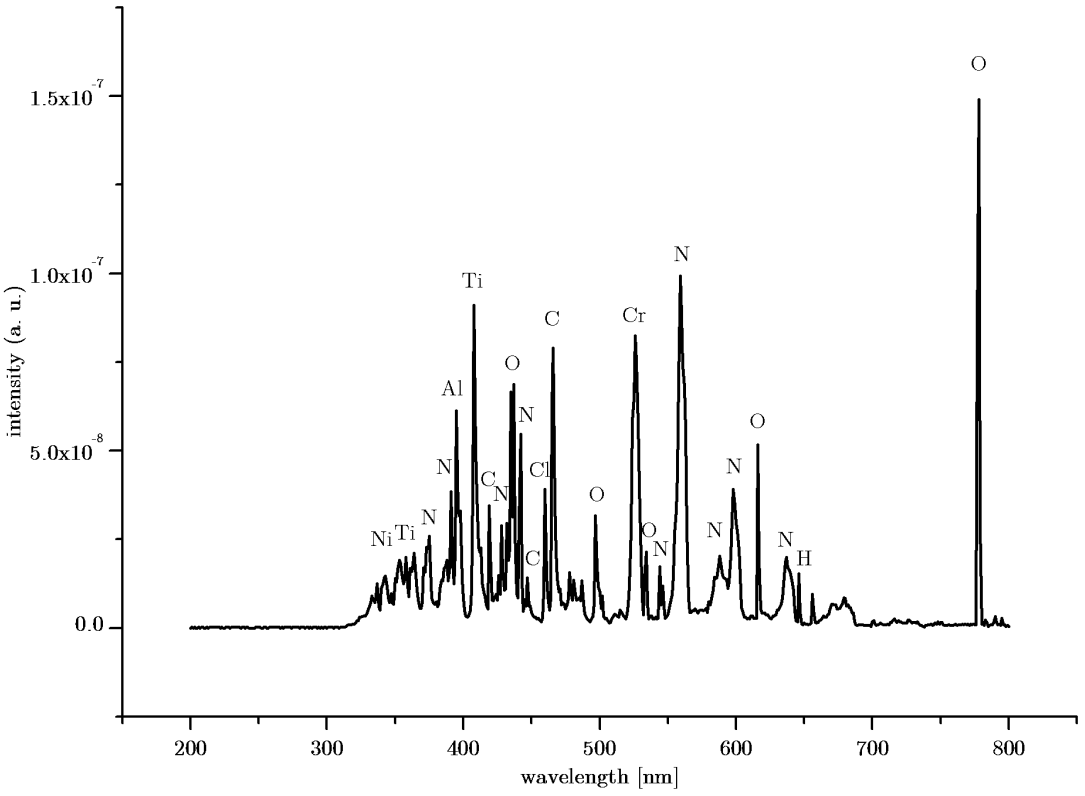


FIGURE 3.25: *OES with a step size of* 1 *nm done on a barrel asher used for* O_2 *ash (courtesy of Dr Haiping Zhou).*

sample id	time $[min]$	SF_6/N_2 flow $[sccm]$	pressure $[mTorr]$	step height[a] $[nm]$	etch rate $[\frac{nm}{min}]$
barrel asher for resist residue removal					
040	15	10 / 40	30	850	56.7
041	30	10 / 40	30	740	24.7
045	15	10 / 40	30	160	10.7
046	30	10 / 40	30	790	26.3
dry etch machine for resist residue removal					
047	15	10 / 40	10	165	11.0
048	30	10 / 40	10	370	12.3
049	15	5 / 45	10	62	4.1
050	30	5 / 45	10	165	5.5

[a]error $\pm$ 5 nm

TABLE 3.3: *Etching results for different process parameters.*

The final process was established to use a power of 10 W and flow rate of 5 *sccm* and 45 *sccm* for SF_6 and N_2 respectively. Such a process gives an etch rate of approximately 4.5 nm/min and an induction time of 2.5 min (see figure 3.26).

In order to obtain the data presented in the figure 3.26 each of the 4 samples were processed with the established process:

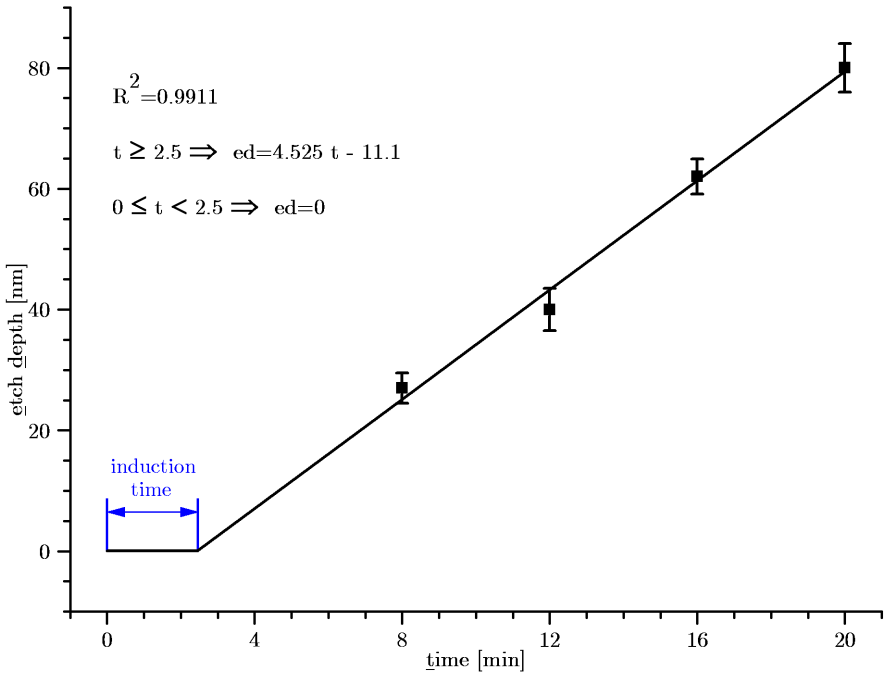


FIGURE 3.26: *The plot of the depth etch versus time. The process is conducted in 80+RIE machine and the process parameters are: power* 10 W, SF_6 *flow rate* 5 *sccm* / N_2 *flow rate* 45 *sccm, pressure* 10 mT*).*

1. `rinse in MS 20D Stripper (1 : 1) R.O. water for` 15 min
2. `rinse in running R.O. water for` 5 min
3. N_2 `blow dry`
4. `spin primer 80/20 at` $4,000$ rpm `for` 5 s
5. `spin s1818 resist at` $4,000$ rpm `for` 30 s
6. `bake at` 90 ^oC `for` 30 min
7. `exposure - hard contact, exposure time` 5 s
8. `rinse in Microposit Developer Concentrate (1 : 1) R.O. water for` 75 s
9. `rinse in R.O. water for` 3 min
10. N_2 `blow dry`
11. `dry etch - for parameters see table E.7`
12. `solvent cleaning (acetone, methanol, IPA, R.O. water) to strip resist`
13. `dry etch -` O_2 `ash - for parameters see table E.5`
14. `Veeco Dektak 6M profiler measurement of etch depth`

PROCESS 3.9: Fabrication process used for establishing etch rate of slow Si dry etch.

i	1	2	3	4	5	6	7	8	9	10
$x_{8,i}$	26	32	29	23	24	29	25	24	23	31
$x_{12,i}$	35	34	39	46	43	46	34	45	41	38
$x_{16,i}$	59	63	67	65	69	59	62	57	59	61
$x_{20,i}$	77	86	80	85	74	72	88	86	78	77

TABLE 3.4: *Table presenting results obtained from etch depth measurements of 4 samples, each etched with the same process parameters for time j [min]. Each measurement point i was taken in different location on the sample. The measured depths $x_{j,i}$ are in [nm].*

Samples were etched in dry etch step number 11 for 8, 12, 16 and 20 *minutes* respectively. By using Veeco Dektak 6M profiler the etched step heights were measured 10 times across each sample (see table 3.4).

3.7.1 Error analysis of etch depth

Based on [149] for each set of data j (here the number represents the etching time of the sample), consisting of $n = 10$ measurements, a mean value was calculated using equation:

$$\overline{x}_j = \frac{1}{n}\sum_{i=1}^{n} x_{j,i} \quad \Rightarrow \quad \overline{x}_8 = \frac{26 + 32 + ... + 31}{10} = 26.6\ nm \tag{3.2}$$

The standard deviation of the mean is expressed by the equation

$$S_{\overline{x}_j} = \sqrt{\frac{1}{n(n-1)}\sum_{i=1}^{n}(\overline{x}_j - x_{j,i})^2} \quad \Rightarrow \tag{3.3}$$

$$S_{\overline{x}_8} = \sqrt{\frac{(26.6-26)^2 + (26.6-32)^2 + ... + (26.6-31)^2}{10(10-1)}} = 1.07\ nm$$

Random error is then equal to

$$\Delta x_{jR} = S_{\overline{x}_j} \cdot t_{\alpha,n-1} \quad \Rightarrow \quad \Delta x_8 = 1.07 \cdot 2.2622 = 2.41\ nm \tag{3.4}$$

where $t_{\alpha,n-1}$ is obtained from the t-distribution table for probability of 95 %.

Finally, the measurement error is equal to

$$\Delta x_j = \sqrt{(\Delta x_{jR})^2 + \frac{1}{3}(\Delta x_T)^2} \quad \Rightarrow \quad \Delta x_8 = \sqrt{(2.41)^2 + \frac{1}{3}(1)^2} = 2.5\ nm \tag{3.5}$$

where $\Delta x_T = 1\ nm$ is the measurement tool resolution.

The same statistical analysis was performed the remaining data giving the following results:

$$x_8 = 26.6 \pm 2.5\ nm$$
$$x_{12} = 40.1 \pm 3.5\ nm$$
$$x_{16} = 62.1 \pm 2.9\ nm$$
$$x_{20} = 80.3 \pm 4.0\ nm$$

Chapter 4

Measurements

4.1 Diffusion depth measurement

The initial approach to fabricate the Hall bar was to utilize a reverse polarized diode. As presented in equation 2.20, the sensitivity of the Hall bar could be increased by selecting a material with higher Hall coefficient R_h or decreasing the thickness d of the sensing layer to increase current density. In order to decrease the thickness in this case there has to be a good control of the diffusion depth. This involves the development of an accurate method for the junction depth measurement. Apart from methods requiring expensive equipment (SIMS - Secondary Ion Mass Spectrometry, SNMS - Secondary Neutral Mass Spectrometry, RBS - Rutherford Back-Scattering) the most common approaches towards this challenge are: angle lapping and staining technique, selective etch and isolation etch.

4.1.1 Angle-lap and staining

At first the n-type doped sample with a p-type layer, of which thickness is in question, is angle lapped between 1^o to 5^o (see figure 4.1). This step acts as a magnification of the doped, surface layer. Afterwards, the sample is stained. Staining techniques use dopant selective growth of a film on a silicon substrate. The film can be formed by e.g. placing the substrate in a solution of 48% HF acid with an addition of nitric acid. The growth rate of the staining film depends on acid concentration, current film thickness, substrate resistivity and substrate type [150]. If the sample is stained under strong illumination, the p-type regions will be darker when compared with n-type. Then using the interference-fringe technique of Tolansky, the measured p-type length x is used to calculate the corresponding layer thickness d using equation 4.1 [100].

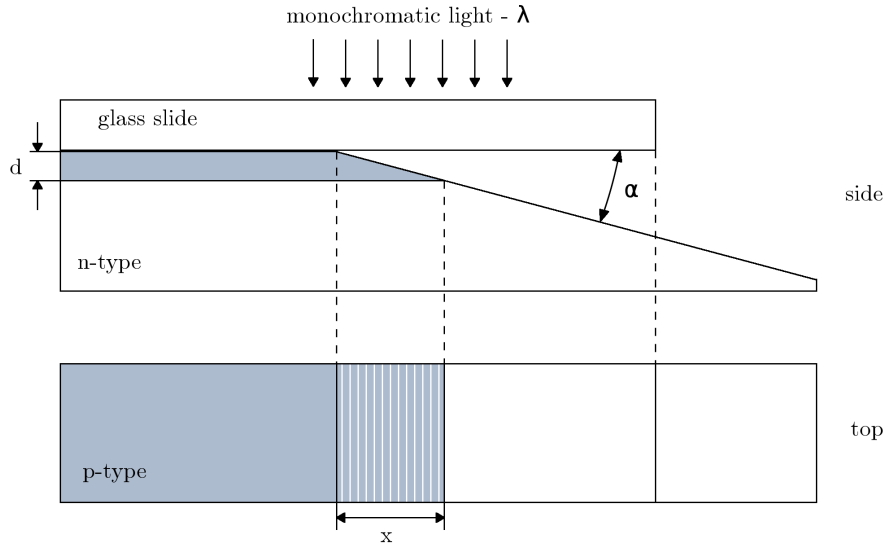


FIGURE 4.1: *Schematic view of the angle lapping and staining method with indicated dimensions.*

$$d = x\ tan(\alpha) = N\ \lambda\ /\ 2\ tan(\alpha) \tag{4.1}$$

This technique provides very wide range of accurate junction depth measurement from 0.5 μm to over 100 μm [100]. However, due to the fact that the required junction depth is below 50 nm, which is an order of magnitude less than measurable with this technique, it is not suitable.

4.1.2 Selective etch

Eijkel et al. in [151] present a method for selective, anodic etching of silicon. This proposed procedure etches all p-type Si and n-type material above the doping level of 10^{16} $atoms/cm^{-3}$. Having partially doped the n-type sample with p-type dopant to form the thin layer, the reverse side of the sample is coated with Al and then partially coated with photoresist. One electrode is attached to an exposed Al side and the other stays in contact with the etchant (see figure 4.2). After immersing the sample in 5% aqueous HF and passing current density of 0.1 $A \cdot cm^{-2}$ the etch rate is approximately 1.5 $\mu m/min$. This process is isotropic and the etch has polishing qualities. The depth of the etched p-type layer could then be measured using AFM.

This method was not used due to the danger involved when dealing with HF together with electricity and lack of an appropriate safety procedure for anodic HF etching.

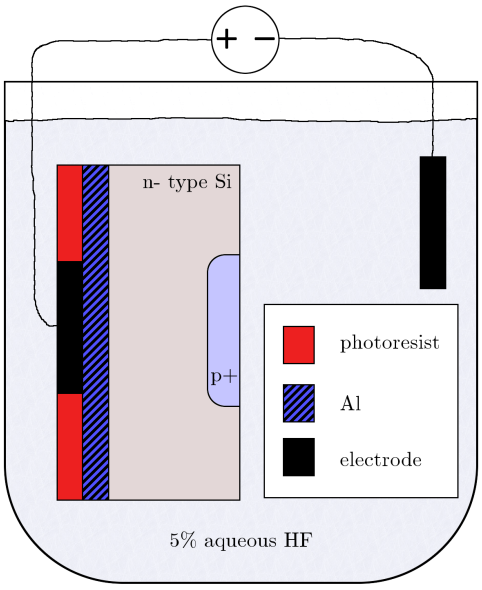


FIGURE 4.2: *Diagram of the setup for the selective etch.*

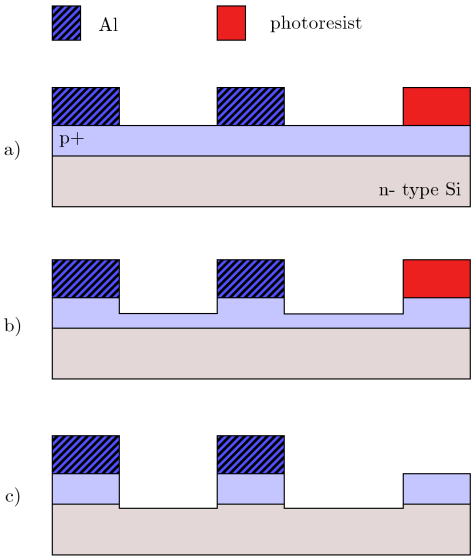


FIGURE 4.3: *Diagrams of the samples at different level of dry etching for the isolation etch technique:* ***a)*** *no etch;* ***b)*** *etched half way through and* ***c)*** *etched through the p-type layer.*

4.1.3 Isolation etch

For this method metallic contacts are formed on top of the thin, p-doped layer (see figure 4.3). The sample is also partially covered with photoresist for the etch depth measurements. Metallic contacts and the photoresist act as the mask for the silicon dry etch process. The isolation etch method uses electrical measurements to measure the resistance between the contacts. So the deeper the etch, the smaller the current becomes. When the p-type layer is etched through, the current reaches the level of leakage current, which is constant with etch depth.

The dry etch process has to be slow in order to achieve a satisfactory resolution. What is more, the current measurement cannot be done simultaneously with the dry etch process, so the required etch depth has to be translated into a dry etch processing time by using the model presented with processing details in section 3.7. Directly after the dry etch process, the measurements can be done. In order to confirm the dry etch process stability and have an exact etch depth, the photoresist is removed with acetone, resist residues removed by oxygen ash, and then using AFM the actual etch depth is obtained. This method is not quick, but, it provides high resolution, unlike the angle-lap and staining technique (subsection 4.1.1), it serves the required measurement range and is much safer to conduct than the selective etch technique (subsection 4.1.2). Also,

since the reverse polarized diode Hall bar is defined using a similar process, the method provides a direct measure of the isolation to be achieved in a real device.

4.1.4 Measurement results

For the diffusion depth measurements, the blank, n-type substrate was processed following the procedure presented in appendix A. The process is designed to produce a sample with 40 *nm* thick p-type diffusion layer. The metallization is used to form a TLM pattern set (see figure 4.4) organized in 4 columns (C) and 10 rows (R). Columns C1 and C2 were exposed to the dry etch, whereas columns C3 and C4 were covered with photoresist in order to provide reference measurements of currents and etch depths. To save time only the pads that were distanced between each other by $n \cdot 2\ \mu m$ and $n \cdot 15\ \mu m$ were tested. Three samples processed in the same manner, each with the TLM pattern were etched to different depths, which were measured to be $40 \pm 3\ nm$ for sample I, $61 \pm 3\ nm$ for sample II and $79 \pm 3\ nm$ for sample III.

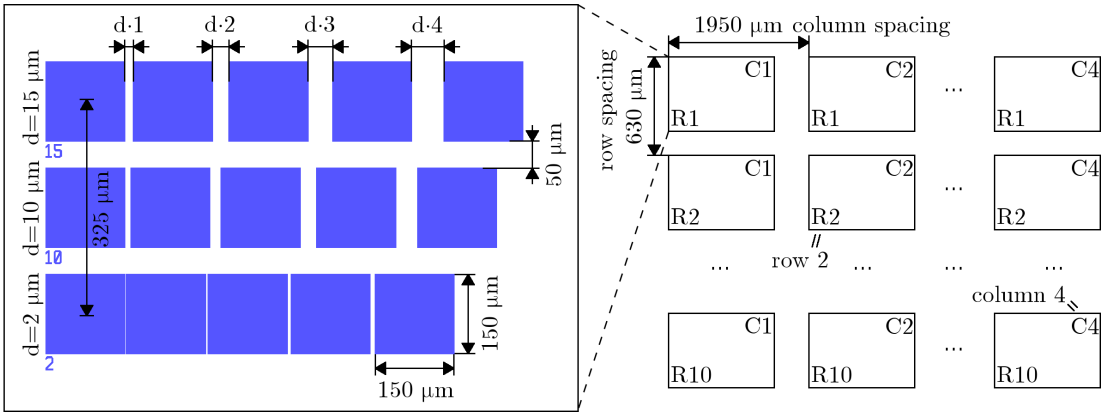


FIGURE 4.4: *Plan view of the TLM pattern used for measurements of p+ doped Si layer thickness.*

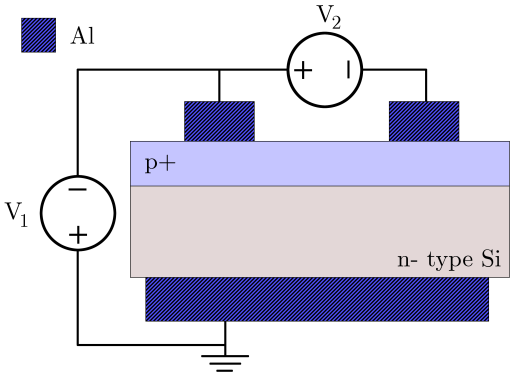


FIGURE 4.5: *Diagram of the measurement setup for the isolation etch test.*

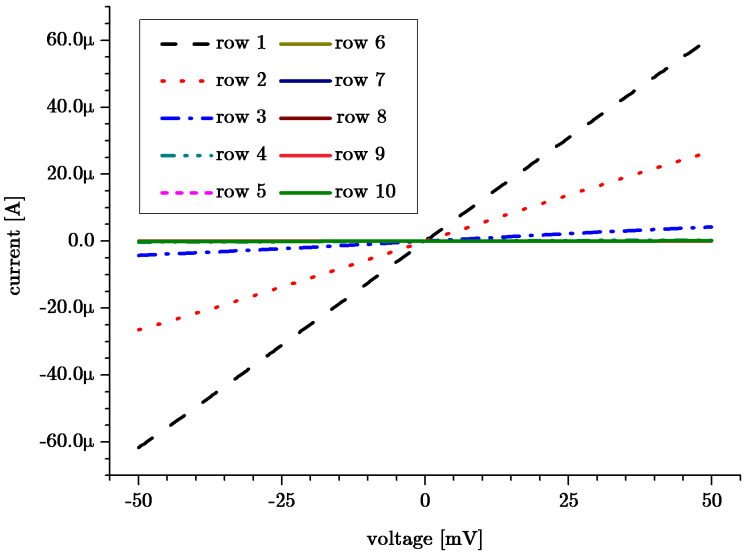


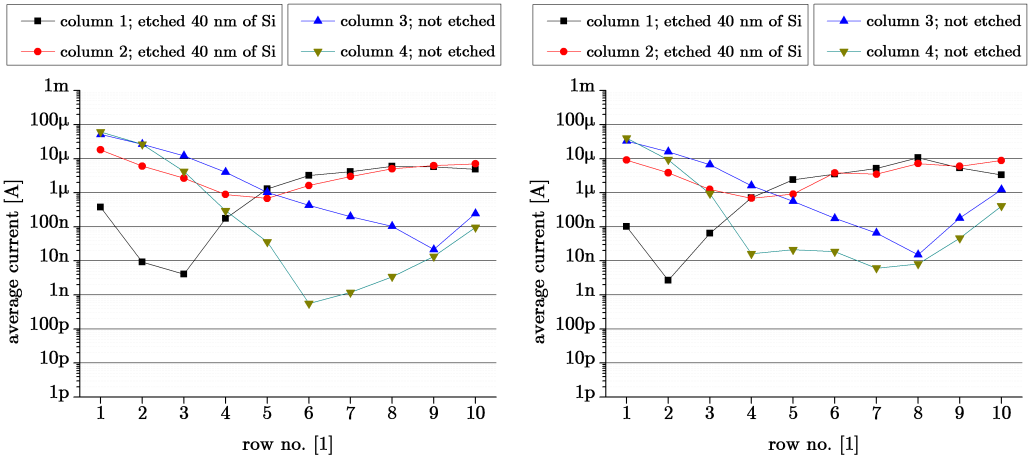
FIGURE 4.6: *Plot of the currents measured on sample I, pad separation* 15 μm*, column 4, rows 1-10.*

The currents flowing through the two contact pads sized 150 μm square and $p+$ layer of the samples were then measured using the connections shown in figure 4.5. Voltage source V_1 provided reverse polarization of the $p-n$ junction at the level of $-0.5\ V$ and voltage source V_2 was varied in the range $\pm 50\ mV$ with a step of $0.5\ mV$. 10 exemplary current characteristics of the sample A (taken at column 4, rows 1-10) are presented in figure 4.6. The plots are linear, however, due to large scatter of the measured currents for theoretically identical patterns, a better way of direct comparison of the plots had to be devised. Each plot was assigned a value y calculated with equation 4.2).

$$y = \frac{max - min}{2} \tag{4.2}$$

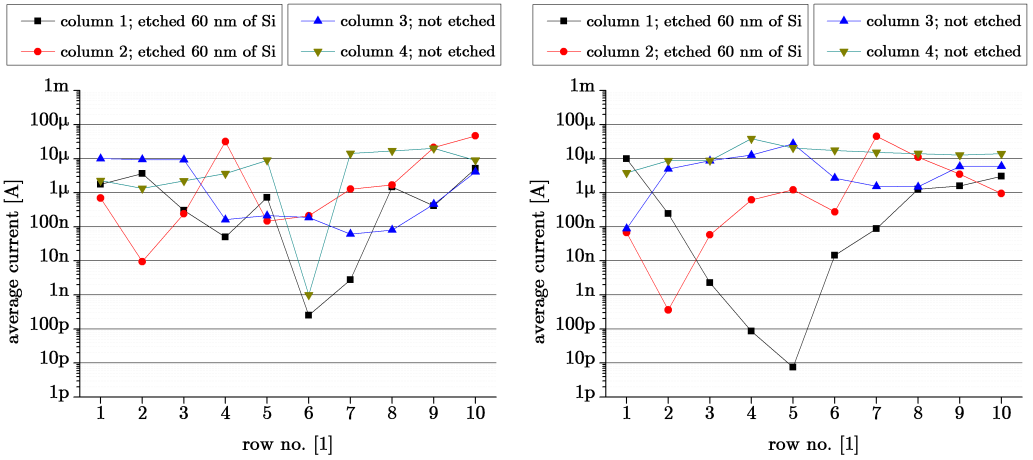
Those values are presented on a logarithmic scale plots in figures 4.7 for sample I, 4.8 for sample II and 4.9 for sample III.

After the analysis of the presented plots, the following conclusions can be drawn. There is some visible correlation between the plots for the devices with pads spaced 2 μm and 15 μm. It is believed that the application of the dopant using spin coating results in the patches of different dopant concentrations. After diffusion these differences across the sample then translate into the variation of the local resistivity, which consequently affects the measured current. It is believed that shallow diffusions magnify the variations of concentration, as longer diffusion time and higher diffusion temperature would allow greater averaging of differences in concentration resulting in greater uniformity across the sample. The spin-on-dopant specification [92] does not state any application limits, however, the thinnest doped layer presented in exemplary processes is approximately



(a) *The pads are separated by 15 μm.* (b) *The pads are separated by 2 μm.*

FIGURE 4.7: *Average current measurement results of TLM pattern. Half of the sample I (columns 1 and 2) is etched to the depth of 40 nm.*



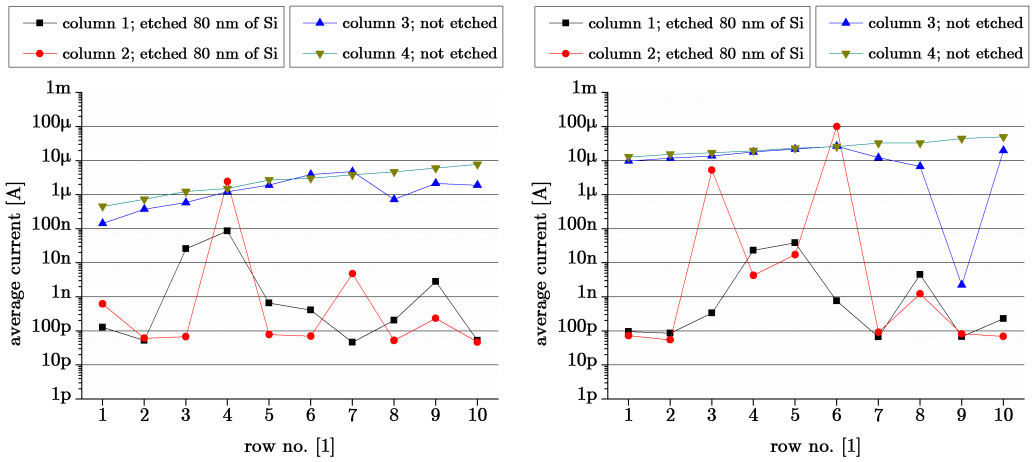
(a) *The pads are separated by 15 μm.* (b) *The pads are separated by 2 μm.*

FIGURE 4.8: *Average current measurement results of TLM pattern. Half of the sample II (columns 1 and 2) is etched to the depth of 60 nm.*

1.1 μm. The required diffusion depth (below 50 nm and ultimately 15 nm) ruled out the use of high temperatures and long diffusion times.

The distance for the closest devices with pads spaced 2 μm and 15 μm is 325 μm and seems to be small enough to see the same current variation behaviour. For the same etched devices in columns 1 and 2, and the same, but not etched ones in columns 3 and 4 this comparison is not that well visible. The distance between the devices is approximately 1950 μm and seems to be large enough to lose the local dopant variation correlation.

The current variation across the same sample for the same type of etched devices is considerable - between 1 and 5 orders of magnitude. For the not-etched devices the



(a) *The pads are separated by 15 μm.* (b) *The pads are separated by 2 μm.*

FIGURE 4.9: *Average current measurement results of TLM pattern. Half of the sample III (columns 1 and 2) is etched to the depth of 80 nm.*

current variation is between 1 and 6 orders of magnitude. When considering the 3 samples, the not etched devices were fabricated using the same processing procedure, which theoretically should give much more uniform performance for sample-to-sample and device-to-device. Even though the sample is approximately 1 *cm* square, the dopant variation is considerable and as a consequence it is difficult to judge which device conducts and which does not. As a result the diffusion depth cannot be measured with this method. If the diffusion depth is not known, according to the equation 2.16, the Hall coefficient cannot be calculated. The local dopant concentration variation affects r_h [112] and resistivity, which influences the current. These variations make this an uncontrollable process which cannot provide a consistent series of devices. Accordingly effects shifted to induced channel devices, in which the source and drain contact diffusions are deeper and more reproducible.

4.2 Transistor measurements

In order to test the fabricated transistors, all measurements were taken with Cascade Microtech Summit 12K Probe Station combined with an Agilent B1500A semiconductor analyser. Using the setup presented in figure 4.10, each transistor of the type shown in figure 4.11 has $I_d - V_{ds}$ curves obtained for a set of V_{gs} voltages (see figure 4.12). V_{ds} is swept from 0 V to -7.5 V with a step of 50 mV, which gives 151 measurement points for each value of V_{gs}, and V_{gs} is swept from 0 V to -7.5 V with a step of -1.5 V.

Simultaneously with the $I_d - V_{ds}$ characteristics, gate current I_g is measured (see figure 4.13) in order to test the SiO_2 layer for pinholes.

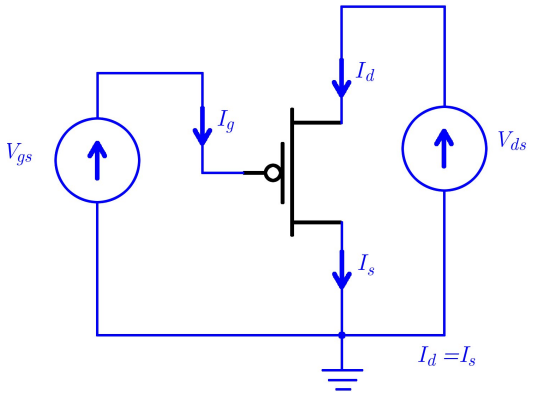


FIGURE 4.10: *Connectivity setup (and naming convention) for obtaining $I_d - V_{ds}$ characteristics of a Si MOSFET transistor.*

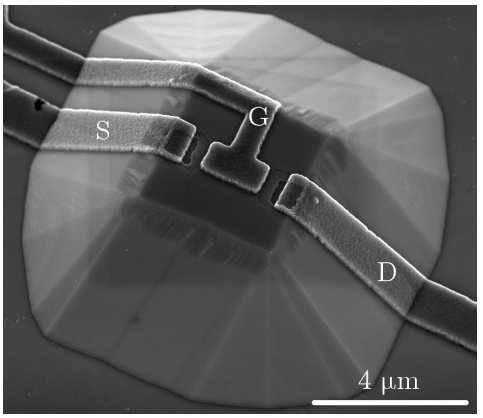


FIGURE 4.11: *SEM diagram of a p-type MOSFET transistor fabricated on the apex of the AFM tip.*

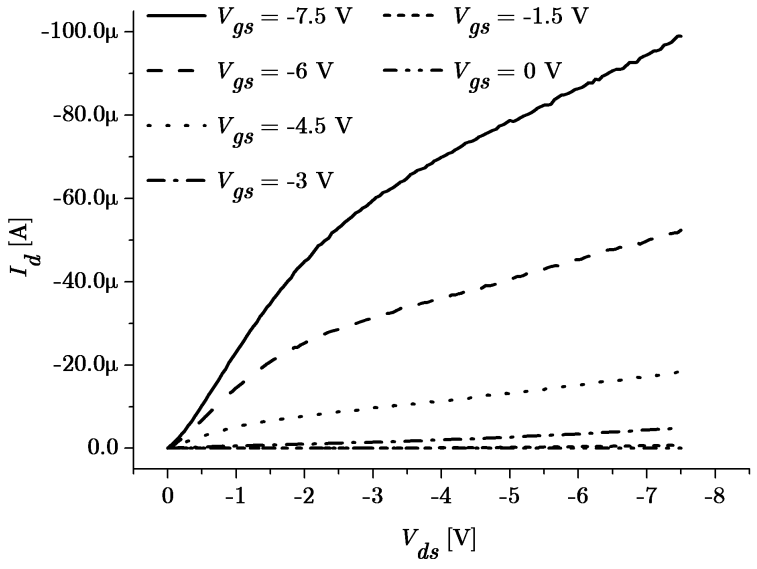


FIGURE 4.12: *Plot of the $I_d - V_{ds}$ characteristics of the transistor presented in figure 4.11.*

Once fully functional devices were recognised, additional measurement of $I_d - V_{gs}$ for $V_{ds} = -300\ mV$ were taken in order to obtain the threshold voltage V_{th} of a transistor (see figure 4.14). For some devices with small I_g current (no more than $100's$ of pA), using a setup presented in figure 4.15, the SiO_2 was tested for dielectric breakdown voltage V_{gb} was swept from 0 V to -42 V with a step of -280 mV. A value of gate current $|I_g| = 3\ \mu A$ corresponds to current density of 300 A/cm^2, which is a large value when compared to what is used by others [152]. However, this value was chosen as 0.25% of the maximum working current for the conditions specified above and is considered acceptable for the target application. At such a current value ($|I_g| = 3\ \mu A$), the applied voltage V_{gb} is equal to V_{br}. An example is shown in figure 4.16.

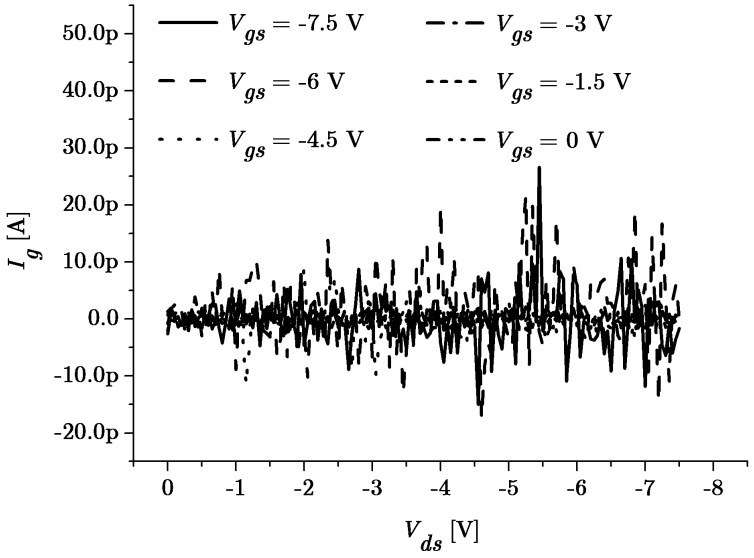


FIGURE 4.13: *Plot of the I_g currents measured during obtaining $I_d - V_{ds}$ characteristics of the transistor presented in figure 4.11. As expected the I_g current shows no dependence on the V_{ds} or V_{gs}.*

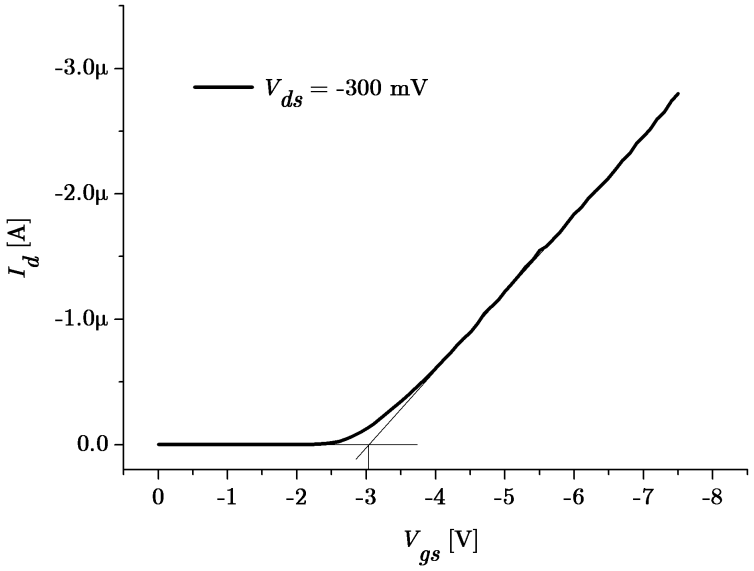


FIGURE 4.14: *Plot of the $I_d - V_{gs}$ (for $V_{ds} = -300\ mV$) characteristics of the transistor presented in figure 4.11. The threshold voltage is equal to approximately $V_{th} = -3\ V$.*

In figure 4.17 results of SiO_2 breakdown strength measurements of 10 devices are presented. The modal breakdown voltage of $V_{br} = -39\ V$ corresponds to oxide breakdown field of 26 MV/cm, which is a reasonable value for a dry thermally grown SiO_2 layer.

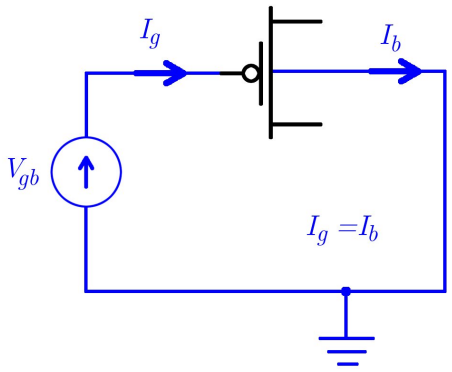


FIGURE 4.15: *Connectivity setup (and naming convention) for obtaining $I_g - V_{gb}$ characteristics of a SiO_2 dielectric layer - gate oxide.*

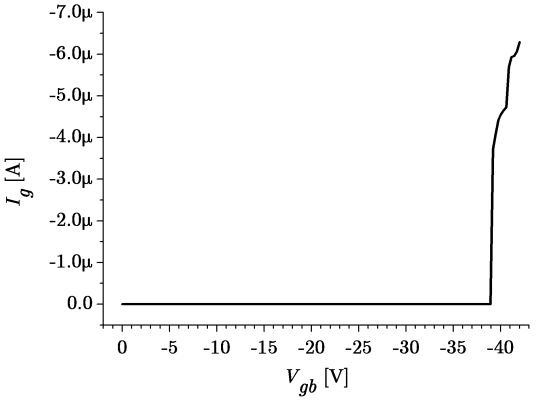


FIGURE 4.16: *Plot of SiO_2 breakdown voltage measurement ($V_{br} = -39\ V$) a p-type MOSFET transistor fabricated on the apex of the AFM tip.*

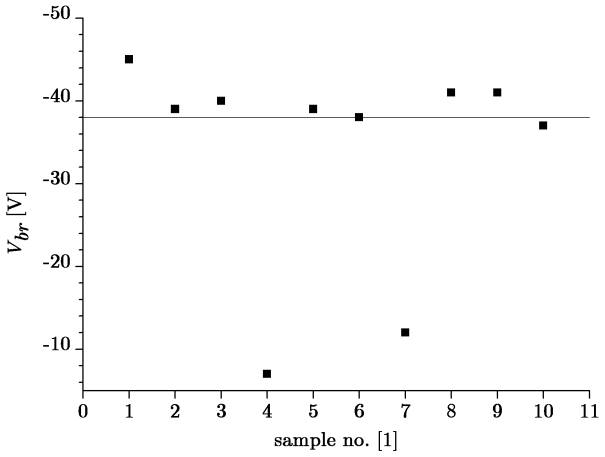


FIGURE 4.17: *Plot presenting the 15 nm SiO_2 breakdown voltages of 10 devices. Devices above $V_{br} = -42\ V$ show no breakdown due to the probe station voltage safety limit set at this $\pm 42\ V$.*

4.3 Variation in time

The measured characteristics of the fabricated transistors were found to show significant variation with time. This made their use as a sensor problematic since it is a requirement of the sensor that its sensitivity is stable.

In this section the $I_d - V_{ds}$ characteristics of the same transistor fabricated on the apex of the AFM tip (see figure 4.11) is presented at different moments of testing.

After successful fabrication of the fully functional transistor, the device was tested by obtaining $I_d - V_{ds}$ characteristics (see figure 4.18). The characteristics show that the gate allows control of the channel, with a transconductance of around 20 μS. The threshold

voltage is $V_{th} = -2.6\ V$. For the maximum applied gate voltage of $V_g = -7.5\ V$ and the maximum drain-source voltage $V_{ds} = -7.5\ V$ (which for a modelled device is enough to enter a saturation region [153]), the transistor is just about to enter saturation region with the drain current around $I_{dMAX} = 60\ \mu A$.

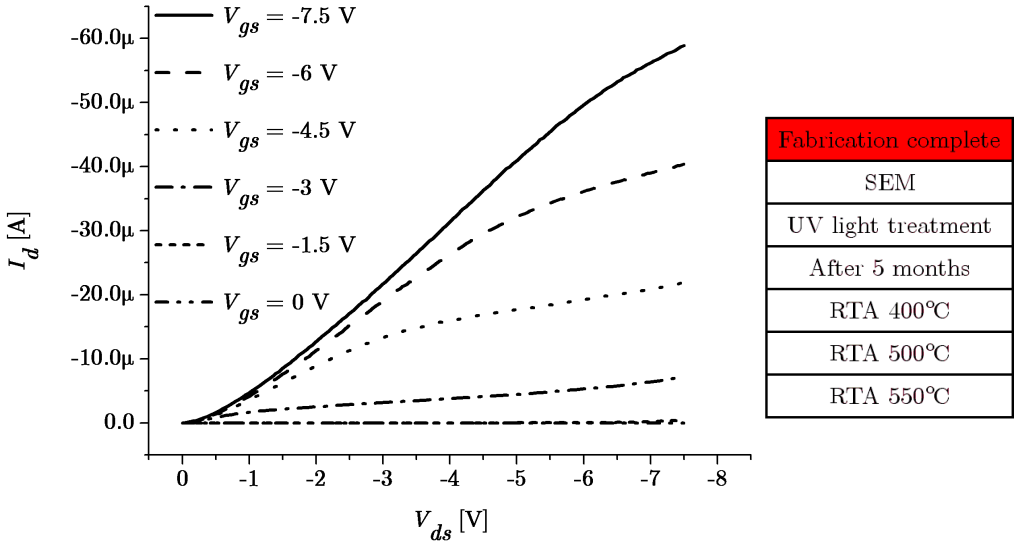


FIGURE 4.18: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken immediately after device fabrication.*

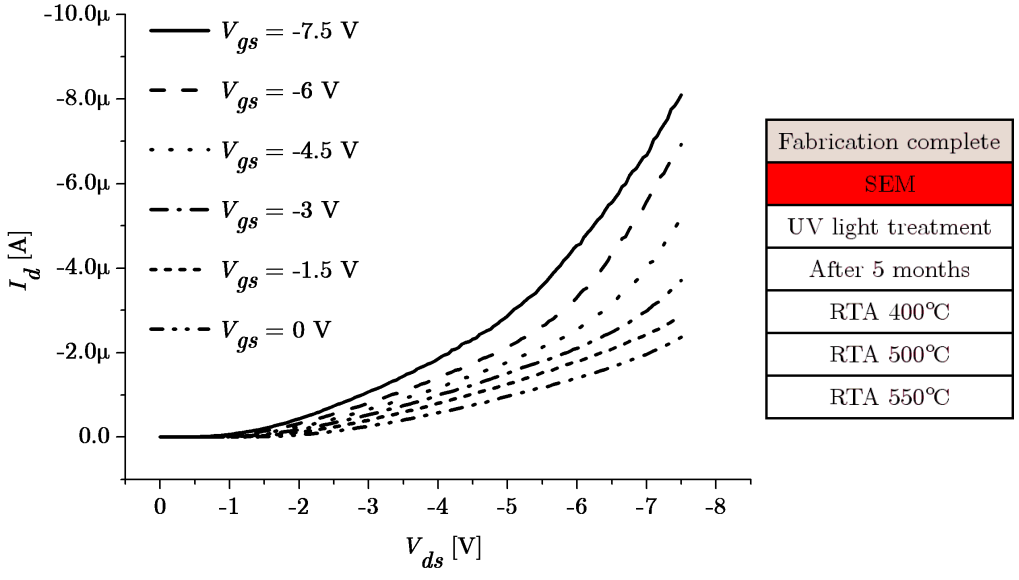


FIGURE 4.19: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after imaging with SEM microscope.*

Following the initial electrical measurements the device was scanned in FEI Nova NanoSEM 630 microscope with acceleration voltages up to 10 kV in order to obtain SEM images

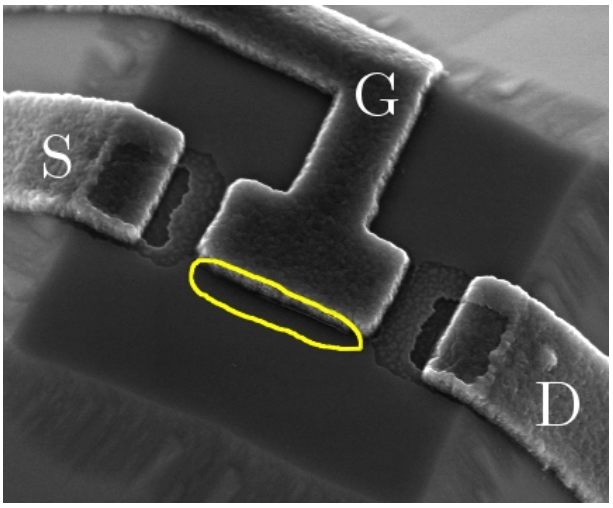


FIGURE 4.20: *SEM presenting zoomed in device from the figure 4.11. The SiO_2 area indicated in yellow is believed to contain trapped electrons from SEM imaging.*

(e.g. figure 4.11) of the specific device and then it was re-tested electrically. The characteristics are presented in figure 4.19 and it is seen that there are considerable changes. The transistor's transconductance dropped by one order of magnitude to around 2 μS. The maximum drain current is equal to $I_{dMAX} = 8\ \mu A$. What is more, the transistor does not switch off. This change in behaviour is believed to be due to the fact that the electrons from the microscope scanning beam are injected into the device, in particular the SiO_2 layer along the edges of the gate (see figure 4.20). When the accumulation of radiation induced electrons reaches a certain level, the device channel inversion occurs along the channel edges, so that leakage paths are formed, making the transistor unable to fully switch off. Effectively the threshold voltage (not measured at this stage) is in a positive voltage range. Such a behaviour is already known from MOSFET devices operating in harsh radiation conditions such as outer space. The problem can be dealt with e.g. by applying the Radiation Hardened By Design (RHBD) techniques [154].

Hammond et al. in [155] used ultra violet (UV) light to modify the threshold voltage of ion sensitive field effect transistors (ISFET) by removing the fixed charge from the passivation layer and by removing the trapped charge from the floating electrode. The change in the threshold voltage was said to be permanent. Since the trapped charges in the SiO_2 layer were felt to be the cause of the transistor's misbehaviour after a treatment in the SEM, it was decided to try to discharge the trapped charges in the manner suggested by Hammond et al.

After application of the UV (wavelength of 365 nm, intensity 120 W/m^2) light lamp for 24 hours, the $I_d - V_{ds}$ characteristics were obtained (see figure 4.21). The I_d current compliance is set at 100 μA to avoid device breakdown. The device still does not switch

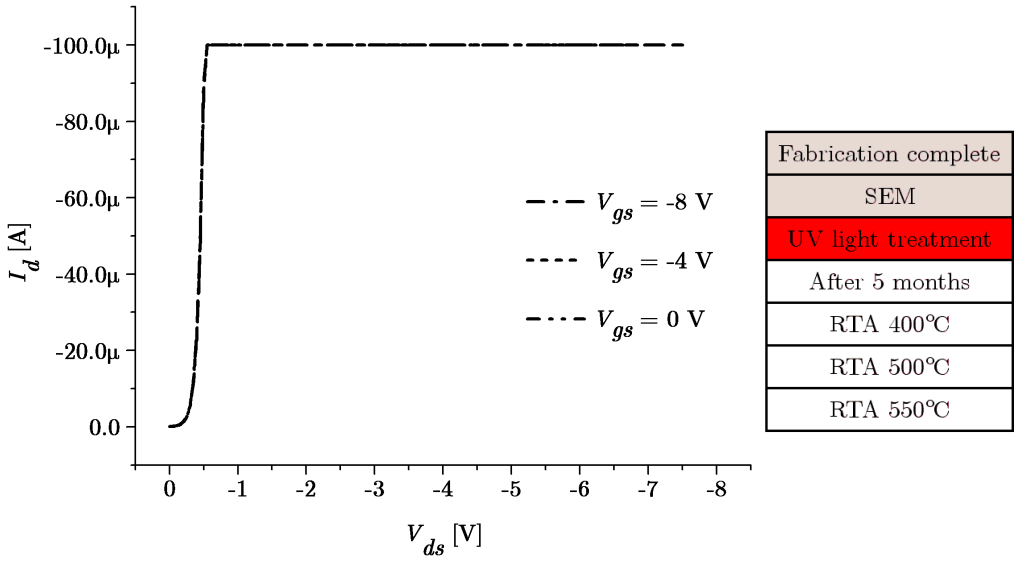


FIGURE 4.21: $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after* 24 *hour long UV light treatment.*

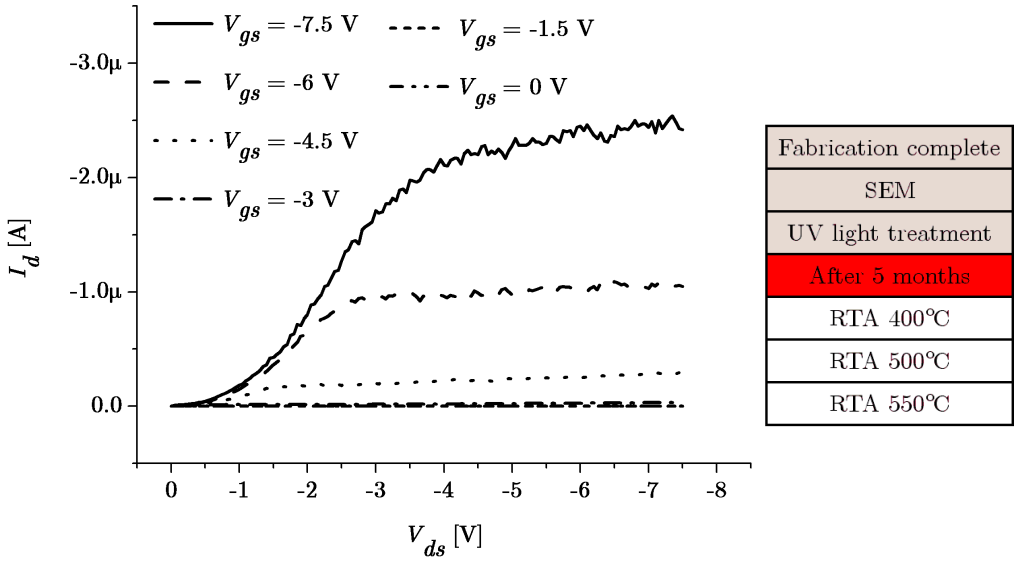


FIGURE 4.22: $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after the device being hidden from light access for* 5 *months.*

off, however, now there is no control of the channel with the gate. This can indicate that the UV light actually injected more electrons into the SiO_2 layer, which caused the induction of a constant channel in the transistor.

For the next 5 months the device was kept in a drawer out of reach of light. After this period the device was again tested electrically (see figure 4.22). The proper transistor behaviour was regained. The device switches off; the threshold voltage ($V_{th} \sim -4.5\ V$) is

higher than before the SEM and UV light treatments. It is believed that the previously injected charges discharged over time. The transconductance is lower than the originally observed and so is the maximum drain current ($I_{dMAX} = 2.5\ \mu A$). It was suspected that the current may have been limited by the contact resistance. In order to test this hypothesis the device was re-annealed in RTA at 400 ^oC in ambient of N_2 for 5 *minutes* (see figure 4.23). The device characteristics changed only slightly. The threshold voltage is even higher ($V_{th} \sim -6\ V$) and the maximum drain current is $I_{dMAX} = 2\ \mu A$.

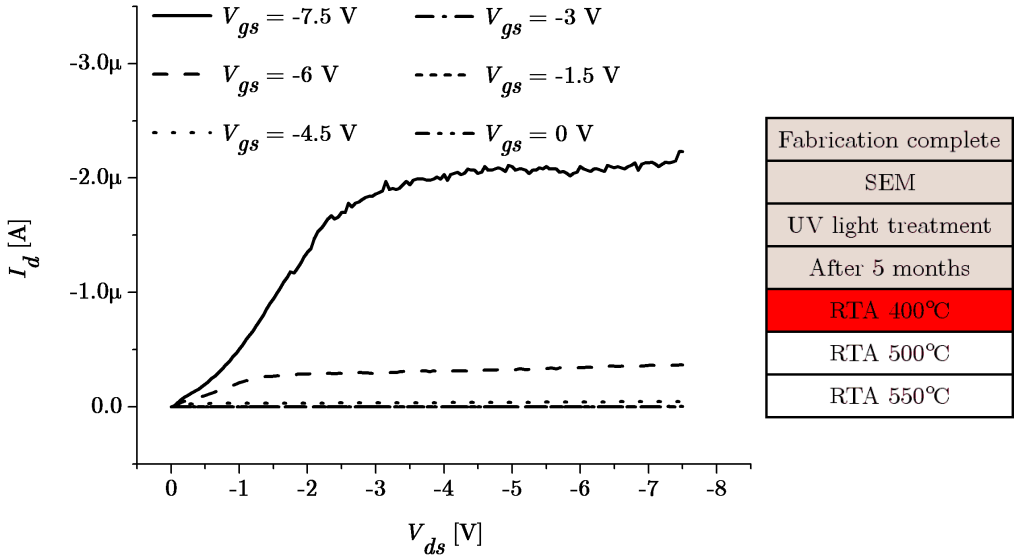


FIGURE 4.23: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after RTA annealing of the device at 400 ^oC in ambient of N_2 for 5 minutes.*

The high contact resistance was confirmed by subsequent RTA anneal at 500 ^oC (ambient of N_2) for 5 *minutes*. Figure 4.24 presents the $I_d - V_{ds}$ characteristics. The threshold voltage dropped to approximately $V_{th} = -4.4\ V$ and the maximum drain current increased to the value of $I_{dMAX} = 70\ \mu A$. The third and last RTA treatment at 550 ^oC (ambient of N_2) for 5 *minutes* resulted in lowering the threshold voltage to $V_{th} = -3\ V$ and increasing the maximum drain current to value of $I_{dMAX} = 100\ \mu A$ as shown in figure 4.25.

The transistor characteristics in the saturation region indicate that the drain current I_d depends on the drain-source voltage V_{ds}, which should not be the case. There are two possible reasons for this behaviour. One is that the doping level of the source and drain regions is not high enough to form a good ohmic contact with *Al*. The higher the doping level, the narrower the depletion region at the interface giving a better ohmic contact. In the opposite case a Schottky diode is formed. Changes in reverse leakage current of the Schottky would then lead to the observed behaviour. The other possible

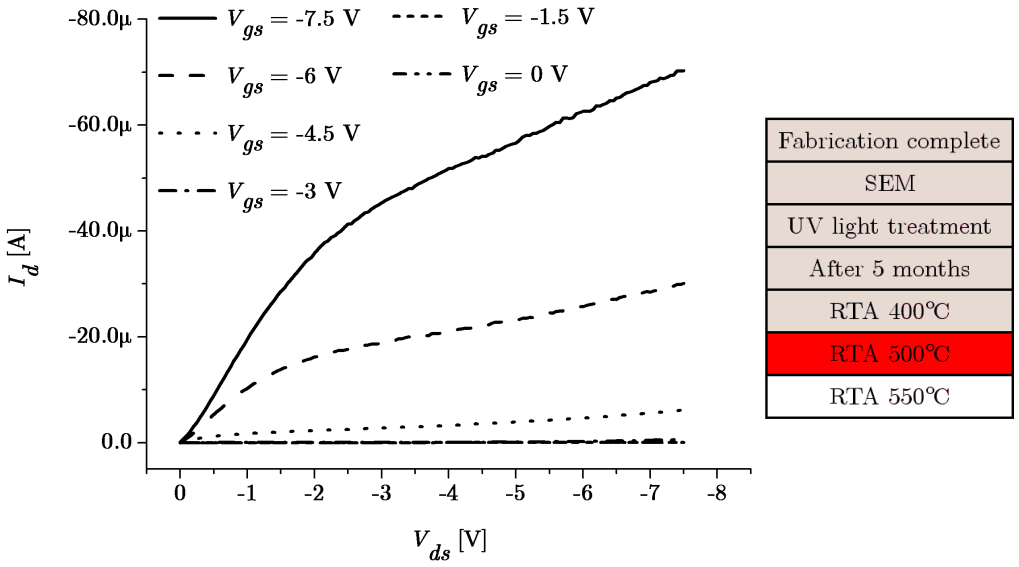


FIGURE 4.24: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after additional RTA annealing of the device at* 500 ^oC *in ambient of* N_2 *for* 5 *minutes.*

reason is that there is a gate-source or gate-drain misalignment resulting in a gap in the conduction path between the highly doped area and the induced channel.

The former problem seems to be the issue of the transistor, since subsequent annealing procedures kept increasing the maximum drain current I_{dMAX} (from figures 4.24 and 4.25 the I_{dMAX} current 2 $\mu A \rightarrow$ 100 μA). The higher the temperature, the deeper the *Al* alloying goes forming a better contact. Such an approach can be continued for a bit more, since the melting point of the *Al* is 660 ^oC, even for thin films [156]. At such a temperature the dopant still does not significantly diffuse, so no profile redistribution occurs. However, as it is explained in the subsection 4.4.1, there also appears to be a misalignment between the highly doped area and the gate.

In conclusion the order in which the same device measurements were obtained (measured after each step) is as follows:

- the fabrication process was accomplished - figure 4.18
- imaging the device in SEM - figure 4.19
- UV light treatment to rectify the SEM treated device - figure 4.21
- 5 months of device being protected from direct light - figure 4.22
- 400 ^oC RTA treatment - figure 4.23
- 500 ^oC RTA treatment - figure 4.24
- 550 ^oC RTA treatment - figure 4.25

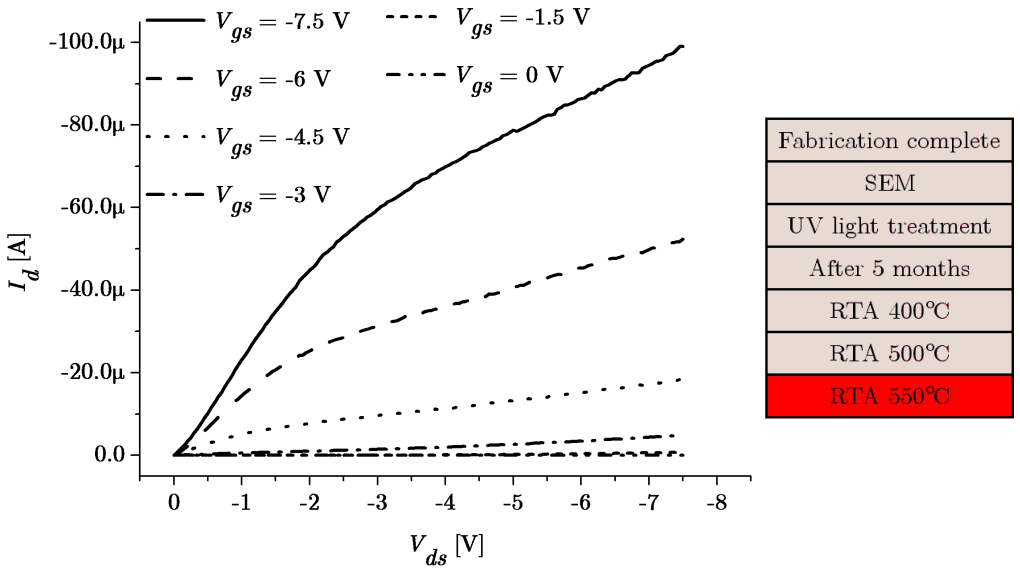


FIGURE 4.25: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11). The measurement was taken after additional RTA annealing of the device at 550 ^oC in ambient of N_2 for 5 minutes. (This characteristic is identical to the one previously presented in figure 4.12.)*

4.4 DC characteristics, yield and discussion of results

The results obtained from the autoprobe measurements were assigned to one of the following 4 categories:

- category I: irrespective of the $I_d - V_{ds}$ characteristics, the gate dielectric layer (SiO_2) is broken and consequently the gate current $I_g \geq I_d$
- category II: the device shows no dependence of V_{gs} on $I_d - V_{ds}$ characteristics
- category III: the device shows dependence of V_{gs} on $I_d - V_{ds}$ characteristics, however, the current I_d is limited ($I_d < 1\ \mu A$) for maximum applied voltages
- category IV: the device shows proper $I_d - V_{ds}$ characteristics and presents workable currents ($I_d > 10\ \mu A$)

The first three categories group different device fabrication failure behaviours, whereas the last category gathers working devices. Typical $I_d - V_{ds}$ and $I_g - V_{ds}$ characteristics of devices from category I are presented in figures 4.26 and 4.27, respectively. This group of devices fail due to broken oxide layer under the gate. Category I device may also suffer from issues such as improper doping level, broken metallic lead (see figure 4.28(a)) or gate misalignment (see figure 4.28(b)). Since damage to the oxide layer can be immediately identified due to large gate current I_g, it forms a separate category of devices.

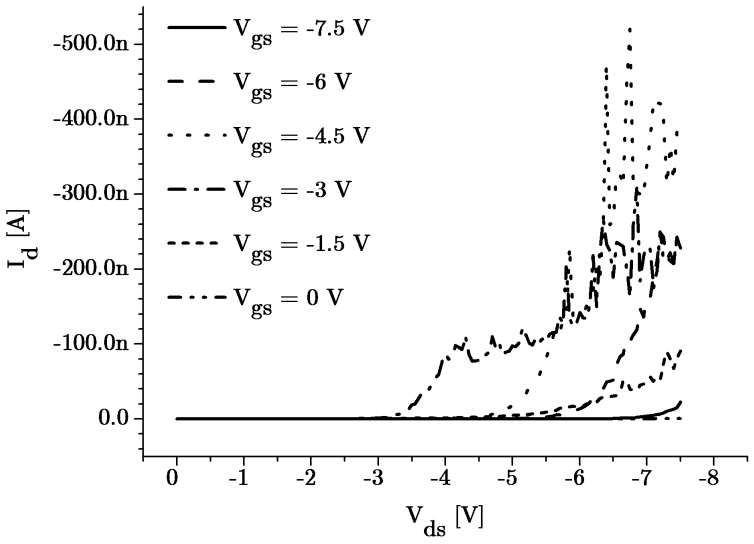


FIGURE 4.26: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor category I fabricated on the apex of the AFM tip. The device has a broken oxide, which is clearly visible on the $I_g - V_{ds}$ characteristics presented in figure 4.27.*

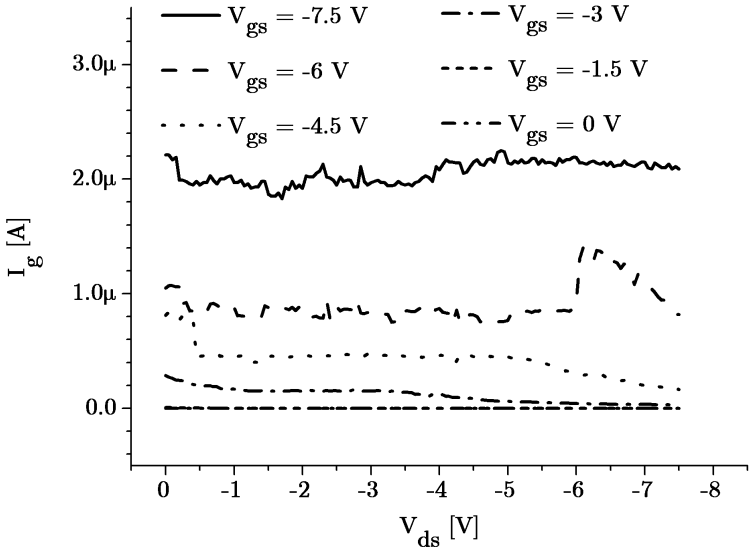
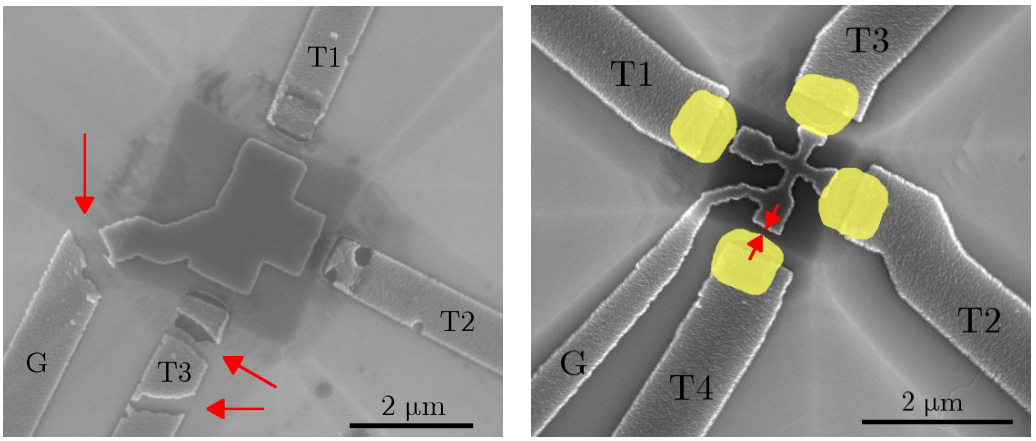


FIGURE 4.27: *$I_g - V_{ds}$ characteristics of the Si MOSFET transistor category I fabricated on the apex of the AFM tip. The characteristics presents the current I_g being dependent on the V_{gs}.*

Category II devices have typical characteristics that are presented in figures 4.29 and 4.30. Unlike category I devices, these transistors do not suffer from broken oxide layer ($I_g \lesssim 10's\ pA$). They do not show any transconductance and the current I_d is in pA range. Such characteristics can be caused by device failure due to:

- broken lead (source, drain, gate or any combination)
- no dopant or low doping level in the drain/source regions



(a) *Broken lead failure.*

(b) *Highly doped area (yellow marks) and gate misalignment.*

FIGURE 4.28: *SEM diagrams of device failures. Red arrows indicate the areas of interest.*

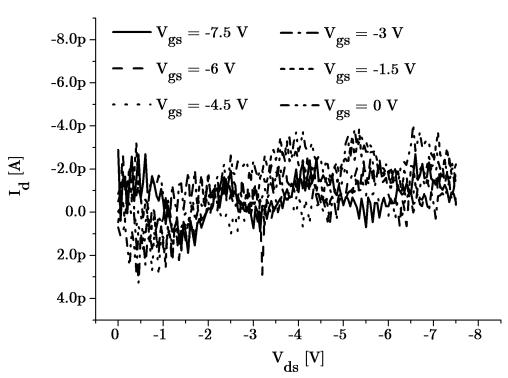


FIGURE 4.29: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor category II fabricated on the apex of the AFM tip. The devices show no transconductance.*

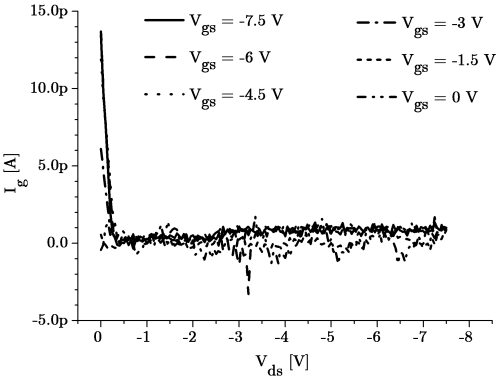


FIGURE 4.30: *$I_g - V_{ds}$ characteristics of the Si MOSFET transistor category II fabricated on the apex of the AFM tip.*

- overetched source/drain regions in contact window etching process (see figure 4.31); the resulting problem is equivalent to the one listed in the previous point
- not etched through oxide layer under contact metal
- source-gate, drain-gate (or both) misalignment resulting in a gap between the induced channel and the highly doped region(s)
- broken field oxide layer and gate lead is shorted to the substrate. No diode characteristic has to be revealed if the short is located fairly far away from the active device. In this way the substrate resistance can diminish the apparent significance of the diode in the electrical characteristic.

Each device was inspected using an optical microscope and as a result failures due to discontinuous leads were eliminated from the list. Despite cracks and wrinkles in the

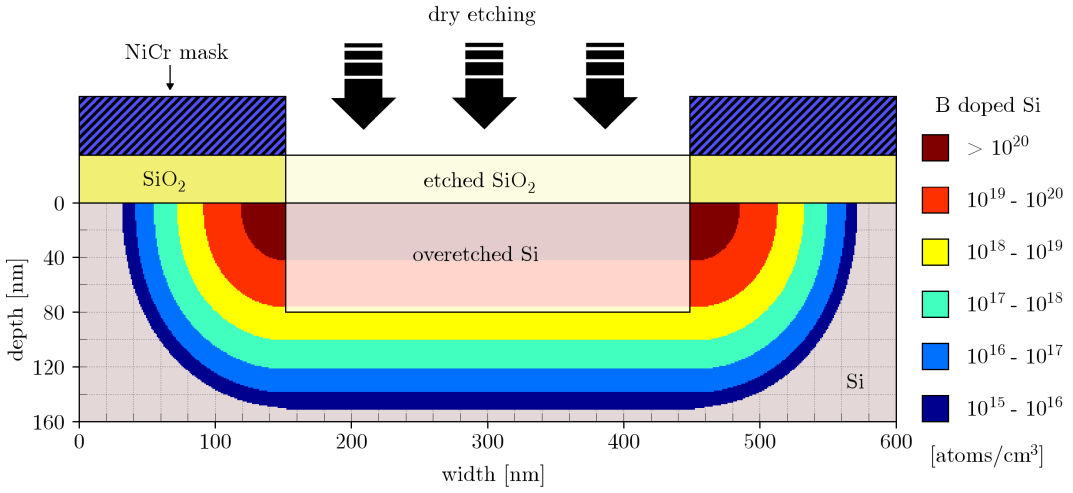


FIGURE 4.31: *Diagram showing a profile of a Si sample with* 150 *nm deep B diffusion. Different doping levels are indicated. The longer the overetch is, the lower the doping level of the doped area is effectively and the more difficult it becomes to form a good ohmic contact.*

resist layers, the float coating technique proved to be 100 % successful in delivering properly lithographically defined metallizations. The etching process of the SiO_2 layer was well controlled using interferometer. The initial test revealed that the 1 *minute* etching process (specific process parameter presented in table E.3) consists of $5-10$ s induction time, approximately 40 s proper etching time and the remaining $10-15$ s is spent on overetching of Si under the etched SiO_2 layer. An exemplary interferometer trace is presented in figure 4.32. The excellent etch depth control provided by the interferometer ensured that the SiO_2 layer window was completely etched and no excessive overetching was done. In the case of the CHF_3 etching process, the selectivity of SiO_2 over Si is greater than 5 : 1 [157]. Hence 1 *minute* overetching would result in approximately 7 nm of Si etched, which is less than 4% of the designed depth of the highly doped region.

In the case of category II devices which show no transconductance, there might be limited amount of dopant or no dopant at all, resulting in contacts forming Schottky diodes oriented in opposite directions to each other. Limited current, I_d (single pA) could then be explained by the relatively large distance (around 1.2 μm) between the source and drain regions, making the series resistance (without induced channel) significant. Such a device would behave like a bipolar junction transistor with no base current applied. The doped regions do seem to suffer from lower than necessary doping levels, which was presented and explained in section 4.3.

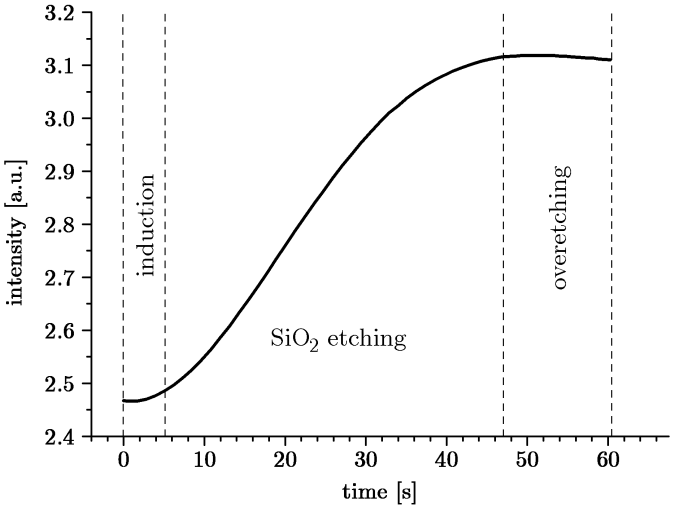


FIGURE 4.32: *Interferometer trace taken while CHF_3 dry etching (for specific process parameters see table E.3) of contact windows in* 15 *nm thick* SiO_2.

There is also a remaining possibility that there is a source-gate and/or drain-gate misalignment. During the device design measures were taken in order to avoid such potential issues by overlapping the highly doped regions with the gate by 120 nm. The tested (Vistec VB6 electron beam lithography tool) alignment error using global, etched Si markers on a flat 3" Si wafer proved to be not worse than 40 nm. By taking 3 times this value as a precaution, the alignment problem should be avoided. However, as shown in subsection 4.4.1, the presented results support the explanation that there is an alignment error greater than 120 nm for some transistors, which were fabricated on the micromachined substrates. Recently it was discovered that such substrates suffer from maximum alignment errors upto 1 μm [158] due to wrong marker locations (caused by not uniform etch rate across the sample during wet etch) and height measurement errors.

The possible explanation of zero measured transconductance is that the gate lead has been connected to the substrate through a pinhole in the field SiO_2 layer. In this way practically no voltage is applied to the gate, since it is cancelled by the same substrate voltage. No charge is gathered under the gate, no channel is induced. During the process design such possibility was taken into account. Due to the complexity of the fabrication process, a simplification was introduced by using a single oxidation process to form only one oxide layer throughout the whole wafer, so that the gate and field oxides are the same oxide (see section 5.2). In order to diminish the probability of pinholes, the SiO_2 layer is dry thermally grown (for parameters see table H.1) to a thickness of 15 nm giving low probability of pinholes with moderately degraded transconductance.

To sum up the category II devices suffer from zero transconductance, which is ascribed to not high enough doping level of the source/drain regions (see section 4.3) and/or source-gate and/or drain-gate misalignment (see subsection 4.4.1). The pinhole in oxide layer explanation is dismissed since the 15 nm thick SiO_2 proved to be of good quality.

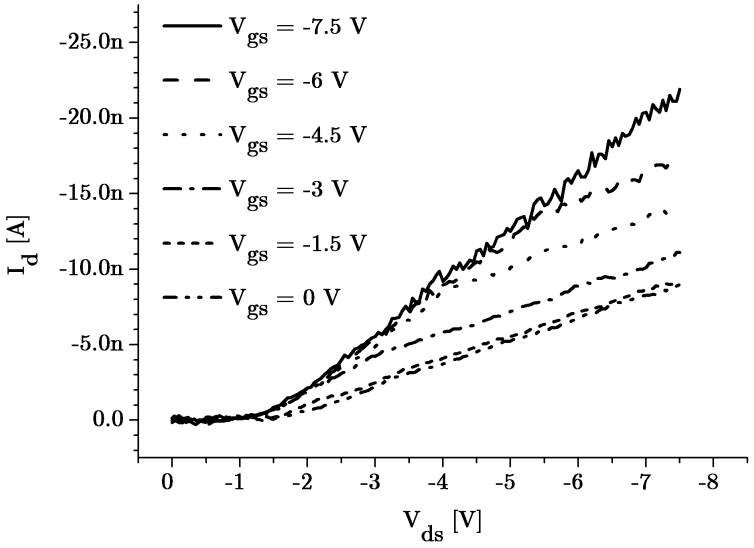


FIGURE 4.33: $I_d - V_{ds}$ *characteristics of the Si MOSFET transistor category III fabricated on the apex of the AFM tip. The device delivers limited current* $I_d < 1\ \mu A$.

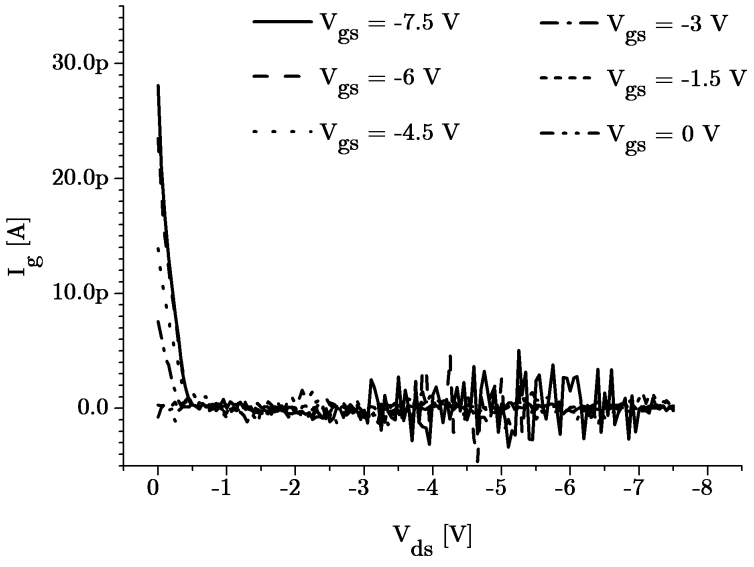


FIGURE 4.34: $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category III fabricated on the apex of the AFM tip.*

Category III devices show a small transconductance and the current I_d is $3-4$ orders of magnitude higher than in category II devices. Exemplary characteristics of such devices are presented in figures 4.33 and 4.34. In terms of possible fabrication failures, these

devices can be treated as a subgroup of category II devices, so the possible reasons for failures are:

- source-gate, drain-gate (or both) misalignment resulting in a gap between the induced channel and the highly doped region(s). The $I_d - V_{ds}$ characteristic (see figure 4.33) indicates no immediate induced channel conductance for low values of V_{ds}.
- no dopant or low doping level in the drain/source regions

Other reasons of device failure such as:

- broken lead (source, drain, gate or any combination)
- not etched through oxide layer
- overetched source/drain regions in contact window etching process
- broken field oxide layer and gate lead is shorted to the substrate

were excluded. The first two points would make device show no transconductance since the there would be an open circuit. Overetching of the highly doped regions could lead to large leakage current (assuming ohmic contacts to the substrate). A broken SiO_2 layer would lead to diode characteristics of the device if the pinhole appeared relatively close to the source/drain or, in the other case, no transconductance would be obtained. To sum up the reasons for the device failure were narrowed down to the limitation of the I_d current due to misalignment and doping concentration issues.

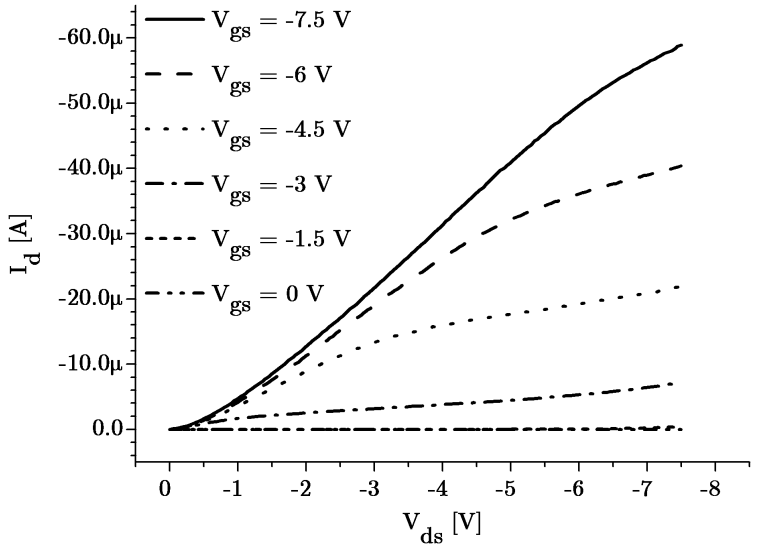


FIGURE 4.35: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip.*

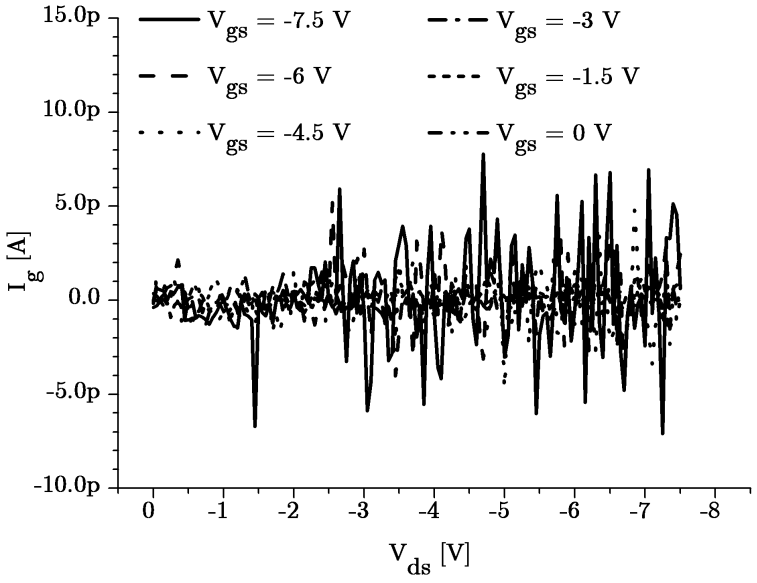


FIGURE 4.36: $I_g - V_{ds}$ *characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip.*

The remaining category, IV, consists of devices with MOSFET transistor characteristics that present current $I_d > 1\ \mu A$. Typical characteristics of the devices are presented in figures 4.35 and 4.36.

On one 3" *Si* wafer there were 3 types of devices fabricated and each type was fabricated as 53 devices. The difference between the 3 types of devices is the size of the source/drain region and the alignment error margin for the contacts. The parametric design of the highly doped area with the overlapping gate is presented in figure 4.37. The gate design with length of 1.35 μm and width of 0.75 μm was the same for all types of devices. The parameters that were varied were intended to check the minimum feasible contact area size. At the same time the highly doped regions were made varied and so was the misalignment margin. The specific values for each device type from the parametric design can be seen in table 4.1. The number of devices of each type and each category are presented in table 4.2.

device	type I		type II		type III		total
	[1]	[%]	[1]	[%]	[1]	[%]	[%]
category I	5	9	1	2	3	6	6
category II	3	6	5	9	12	22	13
category III	42	79	46	87	38	72	79
category IV	3	6	1	2	0	0	2
total	53	100	53	100	53	100	100

TABLE 4.2: *Table presenting numbers (and percentages) of device categories and types for devices fabricated on the apex of the AFM tip.*

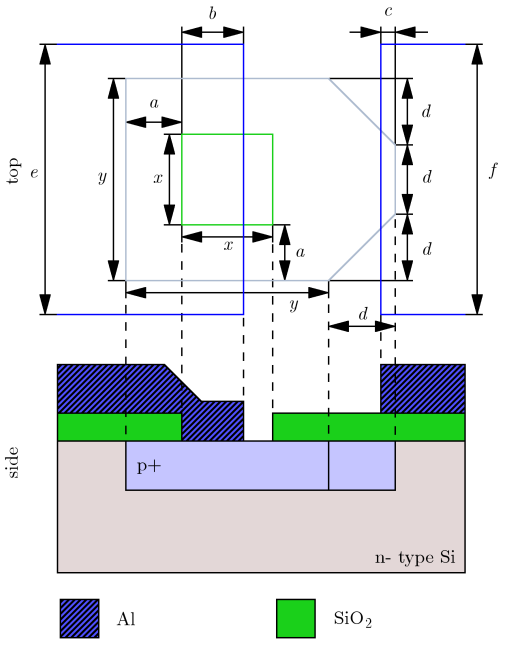


FIGURE 4.37: *Diagram presenting top and corresponding side view of the parametric source/drain design of the Si MOSFET transistor fabricated on the apex of the AFM tip (presented in figure 4.11).*

par.	unit	device type		
		I	II	III
x	$[nm]$	600	450	350
y	$[nm]$	1000	750	500
a	$[nm]$	200	150	75
b	$[nm]$	400	300	233
c	$[nm]$	120	120	120
d	$[nm]$	333	250	167
e	$[nm]$	1000	750	500
f	$[nm]$	750	750	750

TABLE 4.1: *Table presenting values of 3 sets of parameters used for design of the Si MOSFET transistors fabricated on the apex of the AFM tip (device type I presented in figure 4.11). The parameter names are defined in figure 4.37.*

The induced channel, $p-type$ MOSFET Si transistor in saturation region was modelled for comparison with the fabricated devices. The transistor parameters used in the model were the gate length $L = 1.35\ \mu m$, gate width of $W = 0.75\ \mu m$ and oxide thickness $t_{ox} = 150$ Å. For maximum applied voltages ($V_{ds} = -7.5\ V$, $V_{gs} = -7.5\ V$) the transistor with $V_{th} = -0.86\ V$ (see appendix L) delivers current I_d of over $1.29\ mA$ (see appendix M). None of the category IV devices delivered this much current and the best one approaches $I_d = 100\ \mu A$. There are three reasons for this:

- source-gate and drain gate bottleneck - as can be observed in the figure 4.37, the gate does not overlap the highly doped region with its full gate width of 750 nm,

but 573 nm. This will limit the current to 76.4 % of the modelled value value, to approximately 950 μA. Such design was intended for optimization of the contact distances for a Si MOSFET Hall bar, where 5 leads (4 terminals and a gate) are supposed to meet at the apex of the AFM tip, which only provides a limited amount of space of $(2 - 4\ \mu m)^2$.

- issues related to the doping level - as discussed in section 4.3, the doping level is not high enough to form good ohmic contact, which will increase the series resistance and limit the current I_d. As a consequence, once the surface doping level is uniform across the wafer, annealing process will require optimization to form a good ohmic and low resistance contacts.
- minor source-gate misalignment as explained in 4.4.1.

4.4.1 Misalignment

During the measurements of one of the transistors it was discovered that the $I_d - V_{ds}$ characteristics obtained do not match the $I_d - V_{ds}$ characteristics measured after swapping drain and source voltages. The two characteristics are presented in figures 4.38 and 4.39.

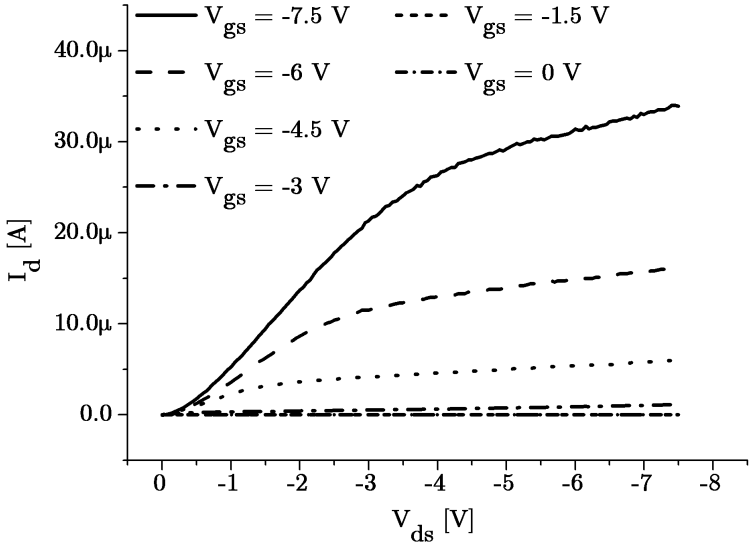


FIGURE 4.38: *$I_d - V_{ds}$ characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip. The characteristics obtained with regular connectivity setup.*

Such behaviour indicates that there is an asymmetry in the fabricated device, even though the transistor design is symmetric. This asymmetry is caused by the gate misalignment with the source (causing a small misalignment gap between channel and contact dopant pocket presented in figure 4.40). For a device without the gap, the applied

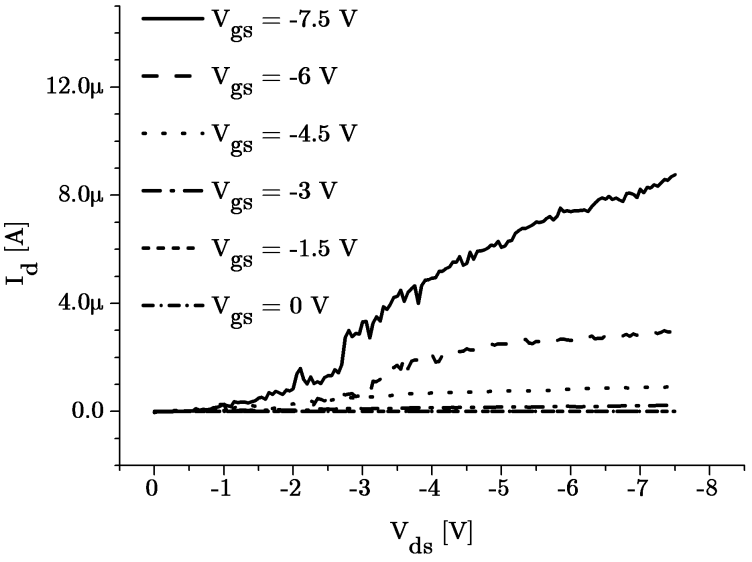


FIGURE 4.39: *$I_g - V_{ds}$ characteristics of the Si MOSFET transistor category IV fabricated on the apex of the AFM tip. The characteristics obtained after swapping source and drain voltages.*

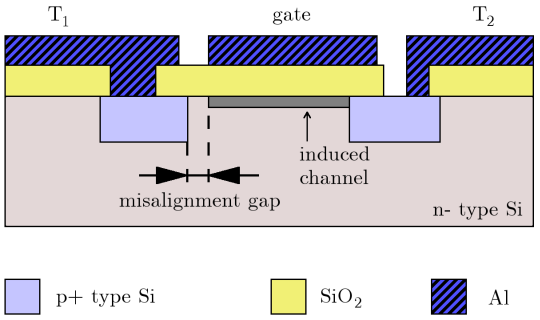


FIGURE 4.40: *Diagram of a induced p-type channel Si MOSFET transistor with a misalignment gap between source and the induced channel.*

voltage to the gate attracts charges, which gather under the gate oxide and form the channel connecting the source and the drain. The interactions between the source/drain and gate are usually discussed in terms of capacitances and the switching speed of the transistor since the gate-contact capacitance is a key parasitic element. However, here the DC characteristics are of interest and consequently the aforementioned interactions usually are minimal and of little interest. These interactions become important if a misalignment gap appears.

If the misalignment gap is small enough and the electric field E_{Tg} between the terminal T_1 and the gate is large enough, the gap can be filled with the charges attracted from the T_1 terminal and form a complete channel between the source and the drain. The higher the electric field E_{Tg}, the more charges fill the gap. As a result in order to get the highest current I_d from such a device it is necessary to name the terminal T_1 as source

and connect the ground to it. Then the electric field E_{Tg} does not depend on the drain potential and stays constant for a specific gate potential.

The misalignment gap not only limits the drain current I_d, but also effectively increases the threshold voltage V_{th}. If the gate voltage is just high enough to induce the channel ($\geq V_{th}$), the misalignment gap still prevents the conduction of the current I_d. Only when electrical field gets high enough to induce the gap, the threshold voltage can be measured.

If the terminal T_2 is the source, then the voltage across the gap becomes dependent on the drain voltage applied. As the drain voltage increases, the induced channel in the gap closes, because the drain-gate voltage decreases. This explains why the saturation current decreases when the source-drain connections are swapped (as presented in figure 4.39).

4.5 AFM

The fabrication of the Hall sensor on the apex of the AFM tip brings the sensing area closer to the magnetic field source, which increases the magnetic spatial resolution, however, to allow such fabrication the spatial resolution of the AFM tip has to be compromised.

At Glasgow, for conventional AFM imaging the Veeco probes model OTESPAW [159] are used. The tip of such a probe is presented in figure 4.41. The probes offer a maximum tip radius of 10 nm [159]. This is less space than is required for the smallest MOSFET Si Hall bar device (the technological limit is discussed in section 4.6). In figure 4.42 a probe fabricated in the course of this project is presented. The apex of the tip is a flat area of $(2 - 4\ \mu m)^2$ on which the Hall bar is lithographically defined.

Both probes are realised in the Si material system. The resonance frequency, the quality factor and the spring constant (nominal) for the Veeco probe used in the test are $f_{res} = 371\ kHz$, $Q = 639$ and $k = 42\ N/m$ [159] respectively. The same parameters for the Hall bar probe are $f_{res} = 459\ kHz$, $Q = 1382$ and $k = 54\ N/m$. To compare the performance of the two probes as topographic imaging AFM tips, two tests were performed using each of the probes. The first measurement is to obtain the step height and the surface roughness of a metallic path. The metallic layer was fabricated in the following manner:

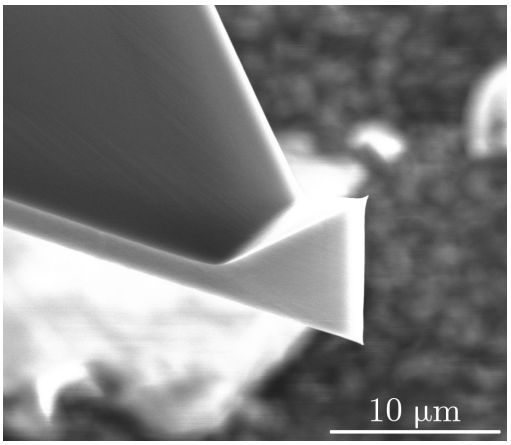


FIGURE 4.41: *SEM diagram of the Veeco OTESPAW probe.*

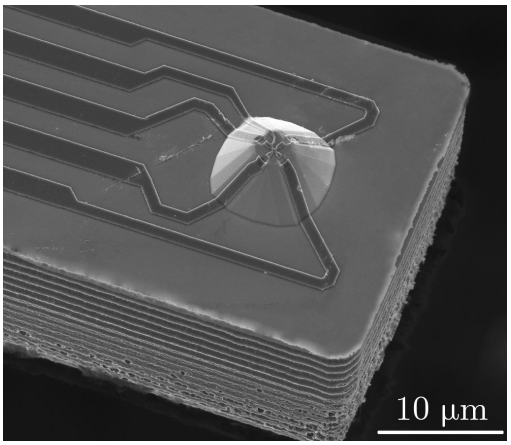


FIGURE 4.42: *SEM diagram of the fabricated AFM probe with a lithographically defined Hall bar device.*

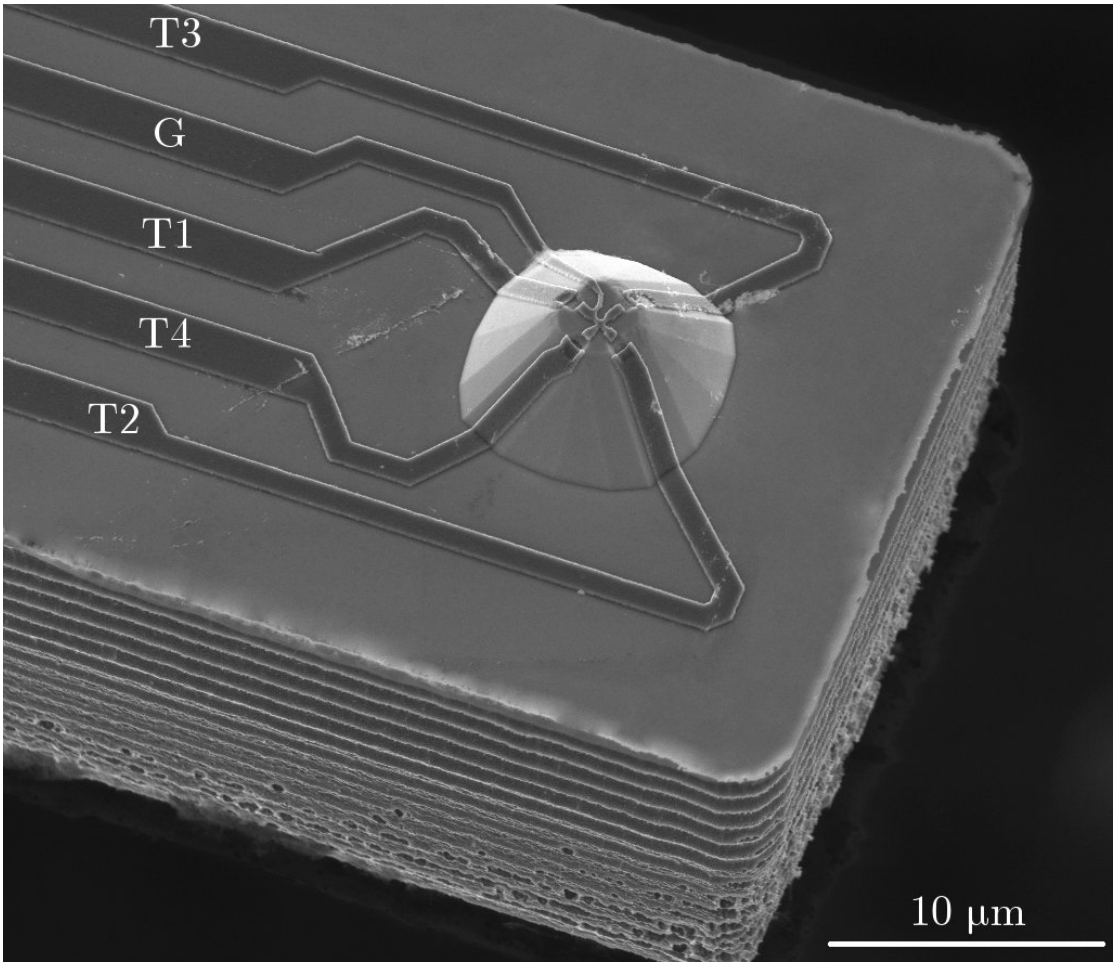


FIGURE 4.43: *SEM diagram of the fabricated AFM probe with a lithographically defined Hall bar device. Magnification of figure 4.42.*

1. spin 8 % 2010 PMMA resist at $5,000$ rpm for 60 s
2. bake in oven at 180 ^oC for 30 min
3. spin 2.5 % 2041 PMMA resist at $5,000$ rpm for 60 s
4. bake in oven at 180 ^oC for 30 min
5. electron beam lithography
6. develop using $IPA : MiBK$ $(2.5 : 1)$ at 23 ^oC for 30 s
7. O_2 ash in a barrel asher at 40 W for 60 s
8. evaporate 30 nm of $NiCr$
9. lift-off

PROCESS 4.1: Fabrication process used for preparation of a test substrate with a metallic 30 nm step for standard topographic AFM scans.

The prepared sample is then scanned in AFM contact mode using the Veeco probe and the Hall bar probe and obtained images are presented in figures 4.44 and 4.45 respectively. The scans do not show any gross differences. In the figures the bright lines show the locations of the obtained profiles, which are presented in figures 4.46 and 4.45 respectively.

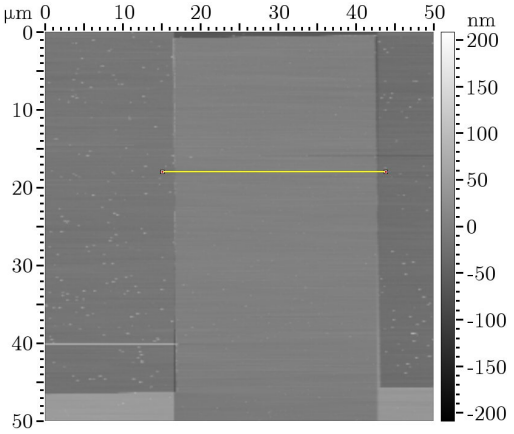


FIGURE 4.44: *AFM diagram of the sample surface containing a metallic path. The image obtained using Veeco OTESPAW probe. The bright horizontal line indicates a location of the profile presented in figure 4.46.*

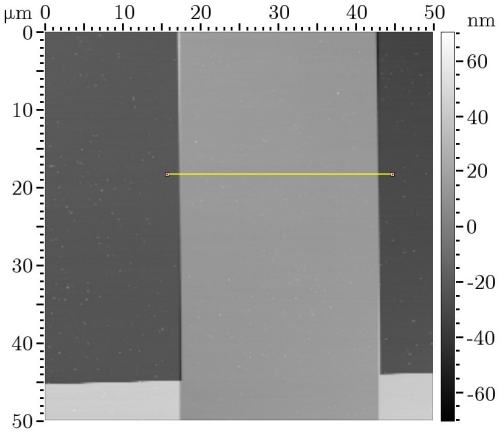


FIGURE 4.45: *AFM diagram of the sample surface containing a metallic path. The image obtained using the Hall bar probe. The bright horizontal line indicates a location of the profile presented in figure 4.47.*

The profiles are obtained approximately in the same area of the sample. On the metallic part of the profile, the Veeco probe provides much more accurate reading due to the high resolution tip, which due to its small dimensions can access the small valleys. The Hall bar probe with its relatively large flat tip does not allow to access those places and as a

result the surface roughness of the metallic layer seems lower (38.9 Å) when compared with the Veeco probe scan (174.5 Å).

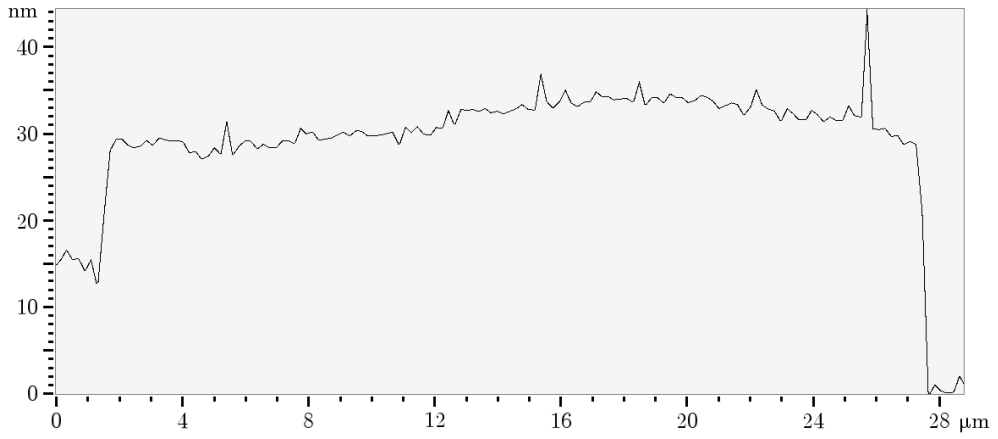


FIGURE 4.46: *Diagram presenting a metallic path profile obtained using Veeco OTES-PAW probe. The location of the obtained profile is indicated in the figure 4.44.*

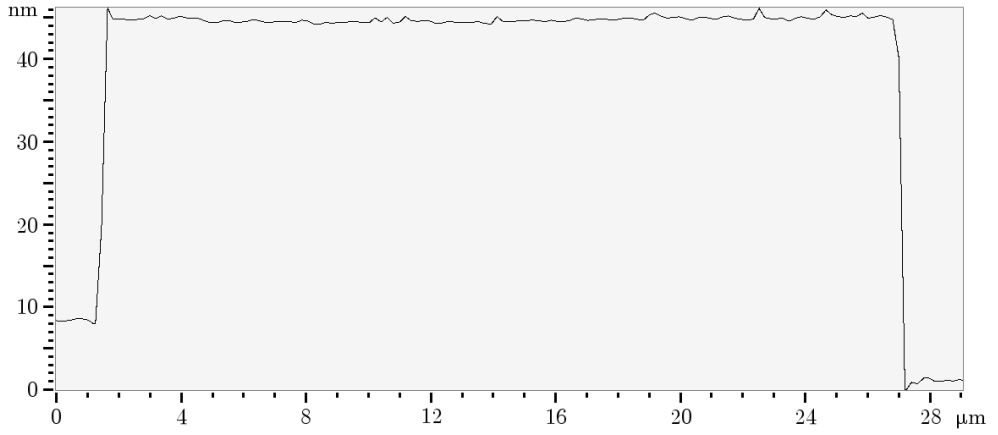
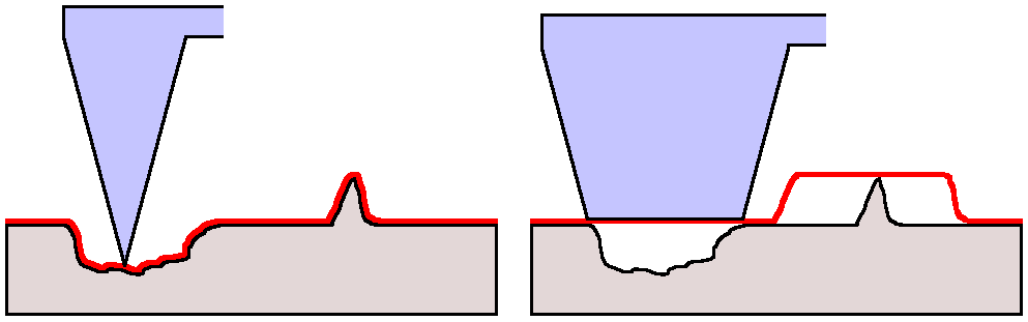


FIGURE 4.47: *Diagram presenting a metallic path profile obtained using Hall bar probe. The location of the obtained profile is indicated in the figure 4.45.*



(a) *Conventional AFM tip has the ease of access to valleys as well as the hill reproduction is accurate.*

(b) *Tip with a flat apex cannot access valleys smaller than the apex size. The hill scan is distorted.*

FIGURE 4.48: *Diagrams presenting two types of probes scanning over the same sample. Red line indicates a path of the tip scan.*

From the two profile graphs presented, the step height appears to be different as well. The step height is greater for scan obtained by the Hall bar probe for the same reason that the measurement of surface roughness differed. The large flat apex of the Hall bar probe slides on top of the local peaks of the metallic layer, without accessing its valleys (see figure 4.48(b)). There is just one peak of similar height presented on the Veeco probe profile plot, however, the apex of the Hall bar probe tip is approximately as wide as it is long, so the locally neighbouring peaks can keep the height of the scan inflated. As a consequence the step appears to be higher than it really is. This indicates that for small topographic features the Hall bar probe does not provide credible measurements. This is an example of a lateral resolution being dependent on the sharpness of the tip [160].

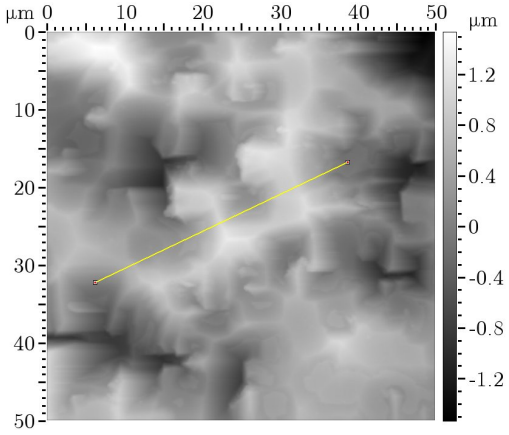


FIGURE 4.49: *AFM diagram of a rough side of single side polished Si substrate. The image obtained using the Veeco probe. The bright diagonal line indicates a location of the profile presented in figure 4.51.*

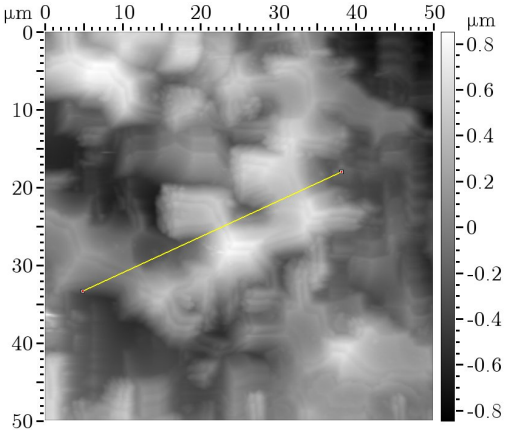


FIGURE 4.50: *AFM diagram of a rough side of single side polished Si substrate. The image obtained using the Hall bar probe. The bright diagonal line indicates a location of the profile presented in figure 4.52.*

The other test performed involved scanning the same area of the rough side of the single side polished *Si* substrate. The obtained images are presented in figure 4.49 for the Veeco probe scan and figure 4.50 for the Hall bar probe scan. The main difference in the immediate comparison is that the Hall bar probe image appears to be blurred. This is another example of the large flat tip affecting the measurement results. The sharp edge features of the sample become relatively wider, as the moving tip senses the edge for longer. This makes tall features seem to be wider than they are. This is confirmed by the profile scans obtained by each probe and presented in figures 4.51 and 4.52.

When scanning the sample with the Hall bar probe, due to the wide tip, the valleys are more difficult to access and as a result measurements of the valleys appear to be narrower than in reality. The measured feature heights are also affected. The mean surface roughness measured for scan obtained by Veeco probe is 3902.1 Å, where by

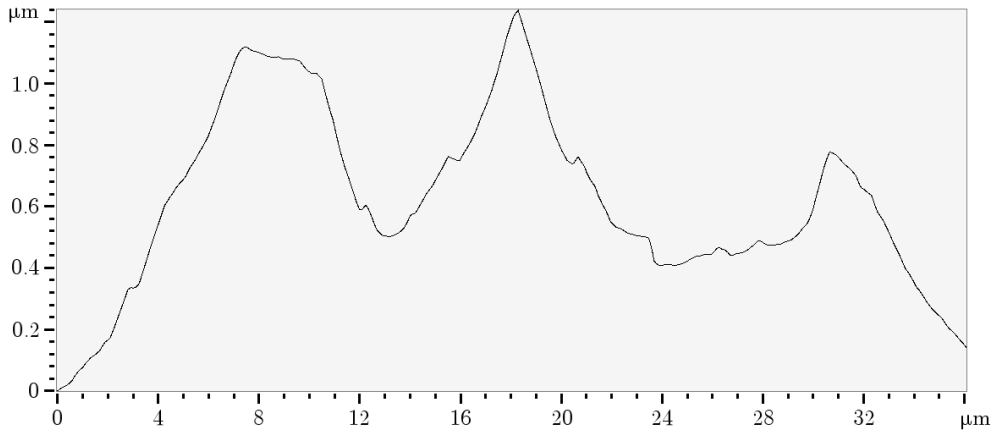


FIGURE 4.51: *Diagram presenting a rough side of a single side polished Si substrate profile obtained using Veeco probe. The location of the obtained profile is indicated in the figure 4.49.*

Hall bar probe is equal to 2592.4 Å, which confirms conclusions drawn from the first test.

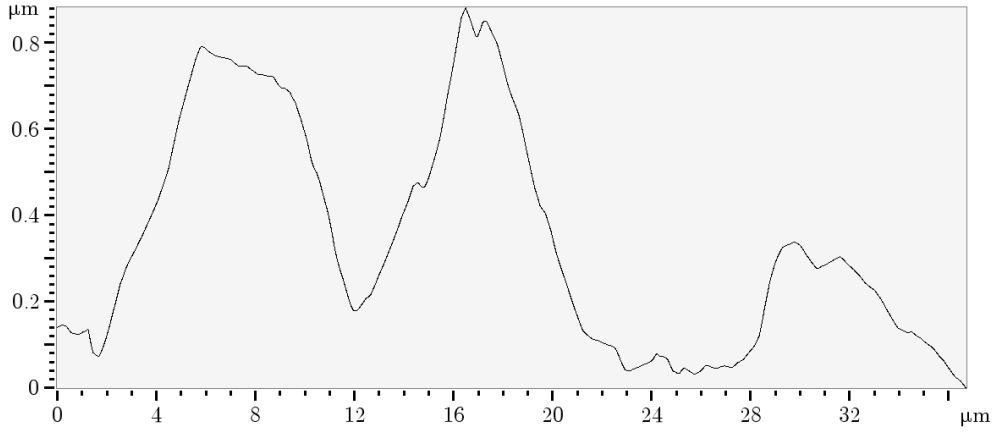


FIGURE 4.52: *Diagram presenting a rough side of a single side polished Si substrate profile obtained using Hall bar probe. The location of the obtained profile is indicated in the figure 4.50*

The Hall bar probe tip size is approximately 2 μm. It may appear that the obtained lateral resolution is higher than the tip size itself. The scans contain probe artefacts, which are a result of a complex function of tip size, shape and its rotation. What is more the Hall bar probe tip contains the 150 nm of Al metallization for leads to active device, which introduces even greater tip-sample interaction complexity.

Both tests suggest that when compared with the commercial probe, the fabricated Hall bar probe performance is poor. This would be true if the application of the fabricated probe was limited to the topographical scans only. The compromise of the spatial resolution allows the functionalization of the probe and measurements of other phenomena,

such as magnetic field. In commercially available hard disk drives, the platters, on which the data is stored, are flat and so are the magnetic heads. Consequently, very high topographic spatial resolution is not required. In case of the Hall bar probe, the topographic data obtained during a scan are used for helping associate magnetic features with a known place on the surface, rather than allowing the simultaneous acquisition of a high quality topographic map. If required such a map may be obtained by using a conventional probe.

4.6 Technological limit

The technological limits of the Si MOSFET Hall bar technology on an AFM tip which has been developed in this thesis are discussed in this section. One of the limits is imposed by the lithography. In order the to achieve high resolution features electron beam lithography is employed. As explained in subsection 2.2, the only choice of resist is PMMA in order to allow float-coating and to provide good resist coverage of topographically varying structures. For a clean lift-off procedure a resist undercut is required, which for PMMA resist is achieved by using two different molecular weight types of PMMA, lighter (molecular weight of 84 k [161]) at the bottom and heavier (molecular weight of 410 M [162]) at the top. Due to the fragility of such float-coated films, it is necessary to apply at least two layers of each resist type. Consequently in order to test the minimum producible feature size, the following procedure was performed on the macromachined substrate:

1. spin 8% 2010 PMMA resist at $2,500$ rpm for 30 s (bake)
2. apply 2 layers of 2.5% 2010 PMMA resist by float coating technique (bake after each layer)
3. apply 2 layers of 1.5% 2041 PMMA resist by float coating technique (bake after each layer)
4. perform electron beam lithography
5. develop resist in IPA:MIBK $(2.5:1)$ at 23 ^oC for 30 s
6. O_2 ash at 40 W in barrel asher for 30 s to remove resist residues
7. evaporate 2 nm of Ti and 10 nm of Pt
8. lift-off in warm acetone (use 55 ^oC bath)
9. inspect under SEM

PROCESS 4.2: Fabrication process used for checking the lithographic limit of a feature fabricated on the apex of the functionalized AFM tip.

The resulting features are presented in figures 4.53 and 4.54.

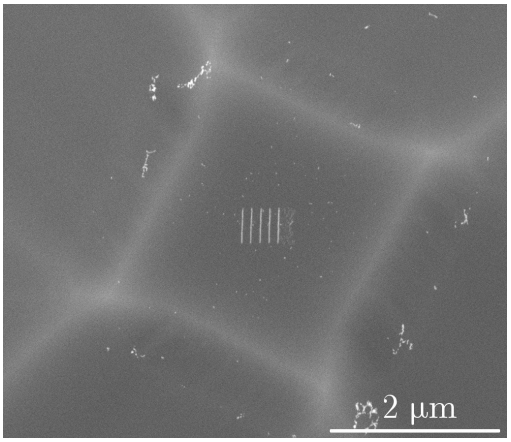


FIGURE 4.53: *SEM diagram of a set of nano wires fabricated on the apex of the AFM tip. The closer view of the wires presented in figure 4.54.*

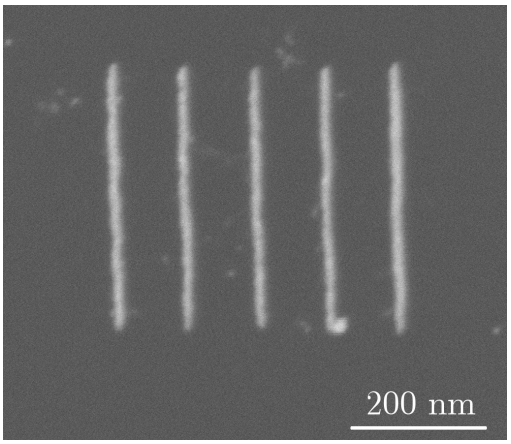


FIGURE 4.54: *SEM diagram of a set of nano wires fabricated on the apex of the AFM tip. The image obtained using a backscatter electron sensor.*

When SEM imaging feature size is approaching 10 nm, the measurement error becomes a significant part of the measurement. Selection of proper imaging SEM contrast mode becomes important in order to minimize the measurement errors. Thoms et al. [163] present evidence that imaging performed using secondary electron sensor of nano wires can provide line width measurement error of over 90%, whereas the usage of a backscatter electron sensor can minimize this this error to approximately 1 nm for 9.4 nm line width. As a consequence, to obtain SEM images of the fabricated nano wires, the backscatter electron sensor is used.

After data acquisition the SEM image (see figure 4.54) was analysed using the ImageJ software [164] to provide a profile of the grey-scale intensity. Such a profile is presented in figure 4.55. In order to obtain the width of the nano wire, the local maximum of the grey-scale intensity has to be found. After the local minimum (localized in the area surrounding the nano wire not further away then 90 nm) is found the mid value is calculated. From the plot the mid value for each line is translated into a corresponding 2 numbers of pixels, one for each slope. By subtracting the two pixel numbers, the nano line width in *pixels* is obtained, which can be then further converted into nm.

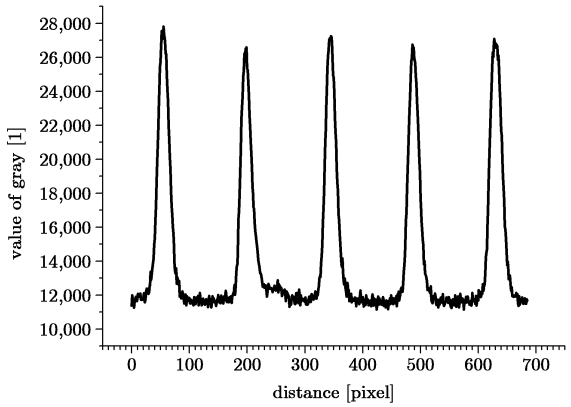


FIGURE 4.55: *Diagram presenting exemplary grey scale profile of the nano line widths obtained from the SEM image presented in figure 4.54). Distance is measured in pixels of the SEM image and* 276 *pixels corresponds to* 200 *nm. The grey intensity is defined by a* 16 *bit long value, where* 0 *corresponds to black and* 65535 *to white.*

line no.	min. [nm]	avg. [nm]	max. [nm]
1	13.8	15.0	16.0
2	12.4	13.6	15.3
3	13.1	13.9	14.9
4	12.4	13.4	14.5
5	14.9	16.4	17.5

TABLE 4.3: *Table presenting minimum, average and maximum values of the 16 nano line width measurements. Nano line number 1 is on the left hand side of the set presented in figure 4.55.*

The results of the calculations are presented in table 4.3. An average nano line width of under 15 nm taken from 16 measurement profiles is demonstrated, so the lithographic limit for the definition of the sensor size has been proven to be 15 nm or better.

As discussed in subsection 1.3.1, by selecting a p-type Si MOSFET induced channel as the means of transport of the majority carriers, the calculated mean free path of the holes is $5.5 - 8.3$ nm. This means that for the sensing area 15 nm wide (and long) there are $2 - 3$ scattering points, leaving this device in quasi ballistic transport range. Consequently, the influence of incoherent electron transport is minimum, so a device with spatial resolution of 15 nm is achievable using the techniques described.

Chapter 5

Summary and future work

5.1 Summary

The work presented in this thesis has been focused on development of the technology allowing fabrication of Hall bar sensors with spatial resolution as high as 15 nm, on an AFM tip. The Si material system was selected for realization of the active device in the form of a p-type induced channel MOSFET transistor. The transistor was fabricated on the AFM tip using electron beam lithography and conventional semiconductor processing techniques.

The fabrication process is organized in batches allowing the processing of up to 200 AFM probes on a 3" wafer. In order to allow fabrication of active devices, several issues were addressed. The lithography limitations due to high topographical variations were mitigated by incorporating float-coating technique. The same challenge for doping was overcome (explained in section 3.4). Due to the fact that borosilica dopant source does not have the same properties as PMMA allowing it to be applied by the float-coating technique, its application had to be achieved by simple mechanical application using a brush.

Incorporating the lithography and doping techniques in the device fabrication process, as described in section 3.1, required an additional, intermediate, metallic layer, which caused problems with the grass effect during SiO_2 etching process (described in section 3.2). This micro-masking was addressed by finding the cause of the issue and dealt with by introducing additional process steps for etching Ni particles.

The micro-machining process requires high quality dielectric layer that introduces stress in the apex of the Si AFM tip. The cause for the hour-glass shape could not be resolved, so the overhang was etched in an additional, quick KOH etching step.

Functional active devices are presented in section 4.2 and basic electrical characteristics are obtained. The active devices fabricated on the AFM tips showed different characteristics, which were divided into 4 categories and each category was analysed from the failure standpoint of device to allow better understanding of their weaknesses and as a guide process for improvement of the yield.

The fabricated AFM probes were tested as standard topographic AFM probes in contact mode and performance parameters were compared with standard Veeco OTESPAW probes. Due to the flat apex of the fabricated probe, the topographic resolution is compromised when compared with the commercial probe. The compromise was necessary in order to facilitate the fabrication of the active device. By fabrication of the sensor on the apex, the sensor can be brought closer to the sample surface and by doing so obtain a higher spatial resolution of the signal of interest.

The whole fabrication process, which is presented in appendices B, C and D, is complex. For the highest achievable resolution device the overall process becomes even more complicated. To achieve a minimally complex fabrication approach, two methods were implemented. Single metallization allowed fabrication of gate, contacts, leads and pads in just one metal deposition step. This limits also the number of lithography processes needed, as for each metallisation, a separate lithography process is required. The other simplification step was to run only once the thermal growth of field SiO_2, which at the same time is the gate SiO_2. The overall effect of these simplifications is to reduce the spatial resolution of the Hall bar but to improve the yield and turnaround time. For obtaining the ultimate, high resolution device the simplistic approach would need to be eliminated.

As the yield data presented in section 4.4 indicates, optimization of the fabrication process is required. The allotted time did not allow the fabrication process to be fully optimized for yield. Consequently, the developed technology is not sufficiently mature to allow fabrication of the Scanning Hall Probe Microscopy with a spatial resolution of 15 nm yet and further development is required.

5.2 Future work

There are several potential improvements that can be implemented in order to progress this technology. Initially development of the reliability of the process is needed. The main recognized areas for improvement are doping and alignment.

To solve the doping issues recognized in section 4.3, the other approaches should be reviewed. The cheapest option is to investigate the doping quality with spin-on dopants

provided by other manufacturers. Apart from the spin-on dopant, other sources (e.g. doping from the vapour phase source) can be also considered.

Ion implantation is also a suitable technique, which in this project was dismissed due to the wafer fragility and the need for large distance substrate transport in order to perform it. Such an approach would require strengthening of the part-processed wafer by using e.g. a carrier wafer. There is a risk of the main wafer being attached to the additional wafer at an angle, which is important from the ion implantation point of view. Assuming the combined wafers thickness varies by 10 μm for the 3" wafer, the variation introduced angle is less than 0.008^o. If the thickness variation is 100 μm, then the angle rises to under 0.08^o. The ion implantation is a very sensitive process to the angle of impurities introduction due to the ion channelling effect. However, this effect needs to be minimized by selecting a optimum tilt angle for the process and the angle variation of under 0.08^o should not introduce a significant error in the doping profile and junction depth, since the standard tolerance is $\pm 1^o$ (some companies offer the tolerance of $\pm 0.1^o$ [165]).

Another possible solution to the issue of weak, part-processed wafer is to reorder the processing stages. The micromachining stage, which makes the wafer fragile, could be moved towards the end of processing after the active device fabrication. Micromachine KOH etching could be then performed with the active device protected from etchant by using Protek B3 [166] and ProTEK PSB [167]. The proposed process flow is presented in figure 5.1. If the ProTEK PSB offers high enough resolution for the photolithography process, it could be even used as a mask for tip definition lithography. Such an approach could lower the cost of fabrication of the final device, as no hard mask would be required in a form of SiO_2 and Si_3N_4, and as a consequence the dry etch processes would not be required in pattern transfer process.

With the aforementioned process, another approach to the device fabrication can be investigated. If a commercial active device without contacts was fabricated on the n-type substrate, the ProTEK products could be then used to process the wafer in order to fabricate the tip and the probe body. Very careful alignment would be required to place the tip mask right on top of the active device. Metallization process would provide the contacts and the leads to the active device. Such approach mitigates the alignment and doping issues. In the end the DRIE process would result in the released AFM cantilever.

The other issue to be investigated is to improve the alignment between all of the electron beam lithography exposures. Initial tests suggest that the alignment between the lithography layers when using etched Si markers is approximately 45 nm in x direction and 20 nm in y direction. To increase the placement accuracy Penrose markers [168] could be implemented into the project. By using them for the local (within one writing

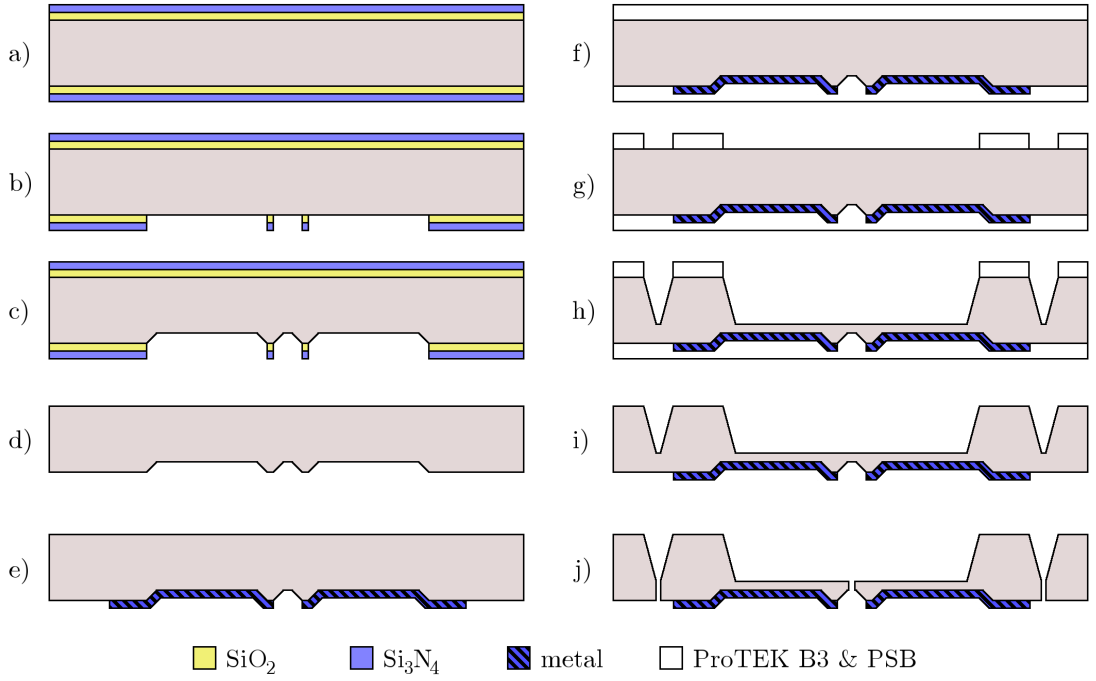


FIGURE 5.1: *Diagram presenting proposed fabrication process with inverted order of deep KOH etching and active device fabrication processes with a view to maintain wafer rigidity through complex active device fabrication process flow:* ***a)*** *a Si wafer is coated with thermally grown SiO_2 and LPCVD Si_3N_4 layers (hard mask);* ***b)*** *by the means of photolithography and dry etch, the pattern is transferred into the hard masks;* ***c)*** *wet etch using 7 molar KOH with IPA solution forms functionalized AFM tips;* ***d)*** *unbuffered HF is used to strip the hard mask;* ***e)*** *active device is fabricated;* ***f)*** *application by spin coating of the ProTEK B3 on the back side and ProTEK PSB on the front side of the wafer;* ***g)*** *by exposing and developing the ProTEK PSB layer the pattern is transferred;* ***h)*** *wet etch using 7 molar KOH with IPA solution forms probe body;* ***i)*** *the ProTEK products are stripped;* ***j)*** *by using photolithography and DRIE dry etch process release etch is performed;*

field), correlation based alignment, the displacement can drop to the value lower than 5 nm [169]. However, to obtain the highest achievable resolution during the electron beam lithography it is important to ensure that the focal planes for reading the markers and the beam writing are the same. Alternatively, the other possible approach would be to focus on the plane with the Penrose markers for alignment and then use the defocus function to make the new focal plane the same as the writing plane. The first approach was tested and failed. The obtained fine alignment data is used to improve global alignment. Due to the failure to recognise the Penrose patterns correctly, the global alignment was undesirably changed. This is most probably due to the fact that the height measurement (used by the focus function) is not taken by the Vistec VB6 lithography tool in the very same spot as the marker location, but $100's$ of μm away. To solve this issue the tip mask plate design will need to compensate for this. The other approach was not tested during this work.

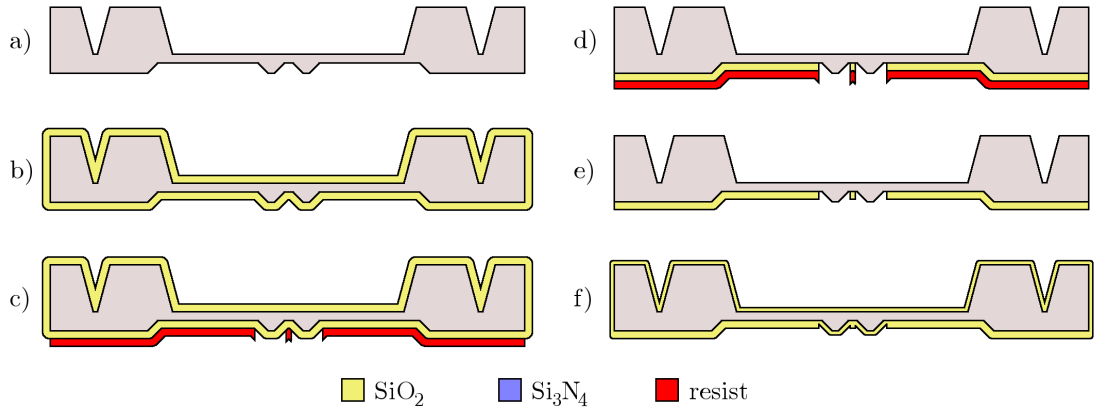


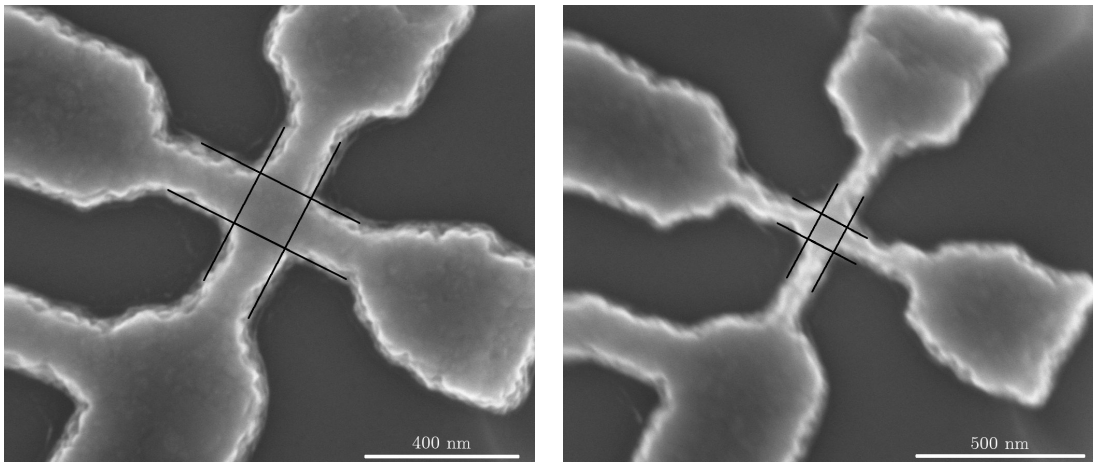
FIGURE 5.2: *Diagram presenting fabrication process of two different SiO_2 thicknesses depending on the area:* ***a)*** *the fabrication process starts at the point when the the probe body is defined and highly doped regions are formed;* ***b)*** *thermal growth of field SiO_2;* ***c)*** *by lithography process the areas, where field oxide is required, remain coated;* ***d)*** *by using $buffered\ HF$ the field oxide is etched away;* ***e)*** *resist is stripped away;* ***f)*** *the gate oxide is thermally grown*

The fabrication of fully operational scanning Hall probe has not been achieved yet, which indicates that this complex technology requires further development in order to increase the yield and reproducibility of the Hall bar devices. The main areas for improvement i.e. doping and alignment were recognised in sections 4.3 and 4.4.

Once these challenges are solved, the Hall bar probes with different spatial resolution of the Hall bars could be fabricated and tested. The key next step will be to fabricate the highest achievable resolution device, which will involve improving the gate SiO_2 thickness, which is needed to keep good channel control of the transistor. This challenge can be solved by growing the SiO_2 in two stages (see figure 5.2). Initial field SiO_2 with thickness of 15 nm can be grown. Additional electron beam lithography could be used to clear the resist on the apex of the AFM tips. A quick $buffered\ HF$ etching step will remove the grown SiO_2 only in the gate region. A second thermal growth of 5 nm high quality SiO_2 will form the gate oxide. As an alternative to the last thermal growth, the use of other high-k (high permittivity) materials could be investigated using an atomic layer deposition tool.

The accuracy of a gate shape definition can influence the spatial resolution of the Hall bars. When the cross shape gate is fabricated using a single metallization, the corners are not well defined due to proximity effect. This becomes an increasingly significant part of the wire width, as the wire dimension gets smaller (see figure 5.3).

For feature sizes under 100 nm the corner error becomes a significant part of the feature size. For features with dimensions approaching 15 nm the error introduced by corner rounding could become over 100% of the wire width. In order to overcome this challenge



(a) *Wires width is approximately* 145 *nm. The corner error is not clearly visible.*

(b) *Wires width is approximately* 85 *nm. The corner error becomes visible.*

FIGURE 5.3: *SEM images of cross shape MOSFET gates made of* 150 *nm thick Al using single metallization.*

an additional level of lithography needs to be introduced. By fabricating half of the gate with one exposure and the other with another exposure, the issue can be solved (see figure 5.4).

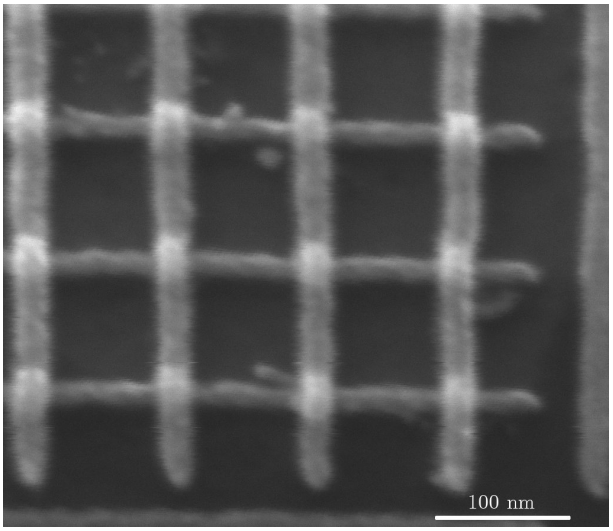


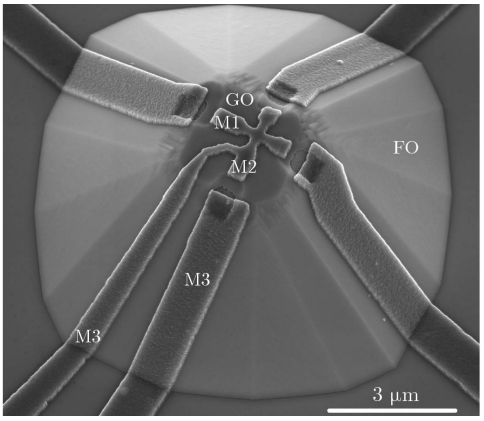
FIGURE 5.4: *SEM image of the nano wires fabricated on the apex of the AFM tip using two electron beam lithographies. Firstly the horizontal lines were fabricated using* 2 *nm of Ti and* 10 *nm of Pt. The measured wire width of* 15 *nm. Then the vertical lines were fabricated using* 2 *nm of Ti and* 15 *nm of Pt. The measured wire width of* 25 *nm.*

Such a treatment does not allow the use of a single metallization due to the aspect ratio of the gate. The two gate lithographies allow accurate fabrication of the gate, however, none of the metallizations is thick enough for the leads and pads. Consequently a third metallization will be needed for the contacts, leads and pads together. Overall

the suggested solution will cost 3 additional electron beam lithographies but will permit Hall bar definition down to 15 *nm*. The comparison of the device fabrication parameters for current state of the technology and the technologically limited devices are presented in figure 5.5.

Current state of technology:

- **oxides**
  field (FO) = 15 nm
  gate (GO) = 15 nm
- **metalizations**
  M1 = 150 nm Al
  M2 = 150 nm Al
  M3 = 150 nm Al



15 nm Hall bar device technology:

- **oxides**
  field (FO) = 15 nm
  gate (GO) = 5 nm
- **metalizations**
  M1 = 2 nm Ti / 10 nm Pt
  M2 = 2 nm Ti / 12 nm Pt
  M3 = 2 nm Ti / 150 nm Pt

FIGURE 5.5: *Diagram presenting required changes in order to fabricate the technologically limited active device on AFM tip.*

After characterisation and comparison of magnetic and spatial resolution of the fabricated scanning Hall probes (including the smallest feature size devices with a modified fabrication process), use of local coils and heaters can allow characterization of magnetic media (e.g. pinning, Curie temperature). As explained in subsection 2.4.2 the use of spatial dithering to eliminate 1/f noise can be implemented.

The ability to fabricate a functioning transistor at the tip of an AFM probe is expected also to have utility in a range of sensing and measurement applications, such as high speed electrochemical micro-measurement and microscopy of electrical properties of samples such as potential or capacitance. High speed electrical measurements with good noise figure require *RF* setup. Typically the nanodevice have the resistance in the range of $10's - 100's\ k\Omega$, which causes large signal reflections in a 50 Ω transmission line. By incorporating the active circuitry (a transistor) close to a sensor this problem can be minimized.

Appendix A

Diffusion depth test process

Blank $< 100 >$ $\pm$ 0.5^o substrate

resistivity: $1 - 10\ \Omega \cdot cm$

dopant: Phosphorous

doping level: $4.5 \cdot 10^{14} - 4.9 \cdot 10^{15}\ \frac{atoms}{cm^3}$

thickness: $380 \pm 2\ \mu m$

I cleaning

1. rinse in MS 20D Stripper $(1:1)$ R.O. water for 15 min
2. rinse in running R.O. water for 5 min
3. N_2 blow dry

II boron diffusion

1. dehydration bake - hot plate at 105 ^oC for 15 min
2. N_2 blow to make sure the sample is not warm - immediately before applying borosilica
3. spin borosilica film ($5 \cdot 10^{20}\ atoms \cdot cm^{-3}$) at $2,000$ rpm for 20 s
4. bake in furnace at 175 ^oC for 45 min
5. bake in furnace at 660 ^oC, N_2/O_2 95%/5% for 120 min
6. diffusion - RTA - ambient N_2 - at 925 ^oC for 120 s

III borosilica removal

1. etch borosilica in 48% HF for 5 min
2. rinse in R.O. water for 5 min
3. rinse in MS 20D Stripper $(1:1)$ R.O. water for 15 min at 105 ^oC (to get the required temperature, slowly add more MS 20D Stripper)
4. rinse in R.O. water for 5 min
5. N_2 blow dry

IV photolithography - TLM patterns

1. dehydration bake - hot plate at 180 ^oC for 6 min
2. resist
   a) apply primer 80/20 to the whole sample

   b) wait for 30 s
   c) spin at 4,000 rpm for 5 s
   d) wait for 30 s
   e) spin s1805 at 4,000 rpm for 30 s
   f) clean bottom side of resist with acetone and a cotton bud
   g) bake on a hotplate at 65 ^oC for 120 s
   h) rinse in Microposit Developer Concentrate (1 : 1) R.O. water for 120 s
   i) rinse in R.O. water for 20 s
   j) N_2 blow dry
   k) bake on a hotplate at 90 ^oC for 120 s
3. exposure - hard contact, expose for 2.8 s
4. post exposure bake - bake on a hotplate at 125 ^oC for 120 s
5. resist development
   a) develop in Microposit Developer Concentrate (1 : 1) R.O. water for 90 s
   b) rinse in R.O. water for 3 min
   c) N_2 blow dry
6. residue removal - O_2 ash, 40 W for 1 min

V metal deposition - evaporate 200 nm of Al

VI lift-off in warm acetone (use 55 ^oC bath)

VII photolithography - etching windows

1. resist
   a) spin primer at 4,000 rpm for 5 s
   b) spin s1818 at 4,000 rpm for 30 s
2. bake at 90 $^\circ C$ for 30 min
3. exposure - hard contact, gap 80 μm, exposure time 5 s
4. development
   a) rinse in Microposit Developer Concentrate (1 : 1) R.O. water for 75 s
   b) rinse in R.O. water for 3 min
   c) N_2 blow dry

VIII dry etch[1] - BP80+RIE - slowsietch (see table E.7)

IX probe station measurements

X cleaning

1. acetone in ultrasonic bath for 5 min
2. methanol in ultrasonic bath for 5 min
3. IPA in ultrasonic bath for 5 min
4. rinse in R.O. water for 5 min
5. N_2 blow dry

XI AFM measurements

[1] Silcon etching process with an etch rate of 4.5 nm/min

Appendix B

Batch fabrication process

For wafer specification see section J.1.

I cleaning

1. rinse in MS 20D Stripper (1 : 1) R.O. water for 15 min
2. rinse in running R.O. water for 5 min
3. N_2 blow dry

II photolithography I - membrane

1. resist (protecting the tip side from scratches) - use a small chuck with rubber seal
   a) spin primer[1] at $4,000$ rpm for 5 s
   b) spin s1818 resist at $4,000$ rpm for 30 s
2. bake at 90 $^{\circ}C$ for 30 min
3. resist
   a) spin primer at $4,000$ rpm for 5 s
   b) spin s1818 at $4,000$ rpm for 30 s
4. bake at 90 $^{\circ}C$ for 30 min
5. exposure - hard contact, gap 80 μm, exposure time 5 s
6. development
   a) rinse in Microposit Developer Concentrate (1 : 1) R.O. water for 75 s
   b) rinse in R.O. water for 3 min
   c) N_2 blow dry
7. cover areas exposed (by rough alignment windows) with s1818 resist
8. hard bake in oven[2] at 120 $^{\circ}C$ for 25 min

III dry etch I - membrane

1. dry etch - BP80 - bothdielectrics (see table F.1)

IV wet etch I - membrane

[1] any of the primers listed in table 0.1 is fine as the features to be exposed are large
[2] hot plate bake at 120 $^{\circ}C$ for 3 min

1. resist stripping
   a) solvent cleaning in ultrasonic bath
   b) dry etch - BP80+RIE - O2-ash-80 (see table E.5)
2. deoxidation for wet etch I
   a) rinse in 900 ml R.O. water and 50 ml 48% HF for 4.5 min (well stirred!)
   b) rinse in running R.O. water for 2 min
3. wet etch I - 630 g KOH + 1,500 ml R.O. water + 500 ml IPA at 80 $^{\circ}C$ for 5 h 17 min - fast stirring[3]
4. wet etch I stopper
   a) rinse in R.O. water (9 : 1) H_2SO_4 for 60 s
   b) rinse in R.O. water for 5 min
   c) N_2 blow dry
5. inspect and measure etch depth under optical microscope
6. if needed, continue etch from step 3
7. if needed, deposit 500 nm of PECVD Si_3N_4

V photolithography II - tip

1. check that the computer for backside alignment on MA6 works - live feed of the cameras is required
2. dehydration bake - hot plate at 180 ^{o}C for 6 min
3. resist
   a) apply primer 80/20[4] to the whole wafer
   b) wait for 30 s
   c) spin at 4,000 rpm for 7 s
   d) wait for 30 s
   e) spin s1818 at 4,000 rpm for 30 s
4. bake on hot plate 115 $^{\circ}C$ for 2 min
5. exposure - backside alignment, hard contact, gap 100 μm, exposure time 4.5 s (use blue foil to cover the chuck, remove two rectangular areas for the backside alignment camera feeds)
6. development
   a) rinse in Microposit Developer Concentrate (1 : 1) R.O. water for 65 s
   b) rinse in R.O. water for 3 min
   c) N_2 blow dry
7. inspect under optical microscope for adhesion of small features and their sizes
8. hard bake in oven at 120 $^{\circ}C$ for 25 min

VI dry etch II - tip

1. dry etch - BP80 - bothdielectrics (see table F.1)

VII wet etch II - tip

1. resist stripping
   a) solvent cleaning (not in ultrasonic bath!)
   b) dry etch - BP80+RIE - O2-ash-80 (see table E.5)

[3] the etching speed of this solution at 80 $^{\circ}C$ varies between $1.10 - 1.15$ $\frac{\mu m}{min}$ for $< 100 >$ plane

[4] 1 min bath in Surpass 3000 or Surpass 4000 can be used instead, followed by N_2 blow dry.

2. deoxidation for wet etch II
   a) rinse in 900 ml R.O. water and 50 ml 48% HF for 4.5 min (well stirred!)
   b) rinse in R.O. water for 5 min
3. wet etch II - 7 molar KOH (1.5 l of R.O. water with 618.9 g KOH pellets, measure 1.6 l) with 400 ml IPA (4 : 1) at 55 $°C$ - fast stirring[5] for 17min, do not dispose of the solution
4. wet etch II stopper
   a) R.O. water (9 : 1) H_2SO_4 for 60 s, do not dispose
   b) rinse in R.O. water for 5 min
   c) N_2 blow dry

VIII inspect under optical microscope for feature sizes; if needed, etch some more.

IX hard mask stripping from both sides of wafer

1. etch dielectric layers with 48% HF for 5 min
2. rinse in R.O. water for 5 min

X removing sharp edges of pyramids

1. etch in the prepared KOH solution for 20 s
2. rinse in R.O. water (9 : 1) H_2SO_4 (already prepared) for 60 s
3. rinse in R.O. water for 5 min
4. N_2 blow dry

XI inspect under SEM

XII cleaning

1. rinse in MS 20D Stripper (1 : 1) R.O. water for 15 min
2. rinse in running R.O. water for 5 min
3. N_2 blow dry

[5] such solution gives the etch rate 0.24 $\frac{\mu m}{min}$ for $< 100 >$ plane

Appendix C

Transistor fabrication process

I hard mask deposition

1. deposit 300 nm of PECVD SiO_2

---

2. evaporate 75 nm of $NiCr$

II ebeam lithography I - phosphorous diffusion

1. resist
   a) spin 8% 2010 PMMA at $2,500$ rpm for 30 s
   b) bake at 180 ^oC for 20 min
   c) float coating - one drop of 1.5% 2041 PMMA resist in cold[1] R.O. water (1 : 1) R.O. water
   d) bake at 180 ^oC for 30 min
   e) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   f) bake at 180 ^oC for 30 min
   g) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   h) bake at 180 ^oC for 30 min
   i) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   j) bake at 180 ^oC for 30 min
   k) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   l) bake at 180 ^oC for 30 min
   m) remove residue from the back side of wafer with acetone and cotton bud
2. expose windows with a dose of 1900, using the 50 nm spot and a VRU of 35, resolution of 1 nm.
3. resist development
   a) develop in IPA:MIBK (2.5 : 1) at 23^oC for 30 s
   b) rinse in IPA for 3 min
   c) N_2 blow dry
4. removing resist residue
   a) barrel asher - 40 W for 60 s

III wet etch - pattern transfer

[1] approximately 4 ^oC

1. etch $NiCr$ with MS 8 chrome etchant[2] for 55 s
2. rinse in IPA for 5 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry

IV stripping resist

1. solvent cleaning (not in ultrasonic bath!) - see section J.3 - with a rinse in acetone for 15 min

V removing Ni residue

1. rinse in 69% nitric acid (3 : 7) R.O. water for 1 min
2. rinse in R.O. water for 3 min
3. N_2 blow dry

VI dry etching of SiO_2

1. dry etch - BP80+RIE - phosdiffwindows (see table E.1)

VII stripping hard mask

1. etch $NiCr$ with MS 8 chrome etchant for 5 min
2. rinse in ipa for 5 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry

VIII removing Ni residue

1. rinse in 69% nitric acid (3 : 7) R.O. water for 1 min
2. rinse in R.O. water for 3 min
3. N_2 blow dry

IX phosphorous diffusion

1. dehydration bake - hot plate at 105 ^oC for 15 min
2. N_2 blow to make sure the sample is not warm - immediately before applying phosphorosilica
3. apply phosphorosilica film ($5 \cdot 10^{20}$ $\frac{atoms}{cm^3}$) with a brush
4. bake on hot plate at 105 ^oC for 45 min
5. diffuse phosphorous (P) in furnace (see table H.1)

X phosphorosilica removal

1. rinse in 48% HF for about 5 min in specifically provided beakers
2. rinse in R.O. water for 5 min
3. N_2 blow dry
4. rinse in hot water (95 ^oC) for 5 min to dissolve P surface contamination
5. N_2 blow dry
6. inspect under SEM
7. rinse in MS 20D Stripper (1 : 1) R.O. water for 15 min at 105 ^oC (to get the required temperature add more MS 20D Stripper)
8. rinse in R.O. water for 5 min
9. N_2 blow dry

[2] the etch rate is 100 $\frac{nm}{min}$

XI hard mask deposition

1. deposit 300 nm of PECVD SiO_2

2. evaporate 50 nm of $NiCr$

XII ebeam lithography II - boron diffusion

1. resist
   a) spin 8% 2010 PMMA resist at $2,500$ rpm for 30 s
   b) bake at 180 ^oC for 20 min
   c) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   d) bake at 180 ^oC for 30 min
   e) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   f) bake at 180 ^oC for 30 min
   g) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   h) bake at 180 ^oC for 30 min
   i) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   j) bake at 180 ^oC for 30 min
   k) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   l) bake at 180 ^oC for 30 min
   m) remove residue from the back side of wafer with acetone and cotton bud
2. expose windows with a dose of 1900, using the 4 nm spot and a VRU of 2, resolution of 1 nm.
3. resist development
   a) develop in IPA:MIBK (2.5 : 1) at 23^oC for 30 s
   b) rinse in IPA for 3 min
   c) N_2 blow dry
4. removing resist residue
   a) barrel asher - 40 W for 60 s

XIII wet etch - pattern transfer

1. etch $NiCr$ with MS 8 chrome etchant for 35 s
2. rinse in IPA for 5 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry

XIV stripping resist

1. solvent cleaning (not in ultrasonic bath!) - see section J.3 - with a rinse in acetone for 15 min

XV removing Ni residue

1. rinse in 69% nitric acid (3 : 7) R.O. water for 1 min
2. rinse in R.O. water for 3 min
3. N_2 blow dry

XVI dry etch

1. dry etch - BP80+RIE - borondiffwindows (see table E.2)

XVII stripping hard mask

1. etch $NiCr$ with MS 8 chrome etchant for 5 min
2. rinse in IPA for 5 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry

XVIII removing Ni residue

1. rinse in 69% nitric acid (3 : 7) R.O. water for 1 min
2. rinse in R.O. water for 3 min
3. N_2 blow dry

XIX boron diffusion

1. dehydration bake - hot plate at 105 ^oC for 15 min
2. N_2 blow dry to make sure the sample is not warm - immediately before applying borosilica
3. put borosilica film ($5 \cdot 10^{20}$ $\frac{atoms}{cm^3}$) with a brush
4. bake on hot plate at 105 ^oC for 45 min
5. diffuse boron (B) in furnace (see table H.1)

XX borosilica removal

1. rinse in 48% HF for about 5 min
2. rinse in R.O. water for 5 min
3. rinse in MS 20D Stripper (1 : 1) R.O. water for 15 min at 105 ^oC (to get the required temperature add more MS 20D Stripper)
4. rinse in R.O. water for 5 min
5. N_2 blow dry

XXI dry thermal SiO_2 - gate oxide

1. grow 15 nm of SiO_2

XXII hard mask deposition

1. evaporate 50 nm of $NiCr$

XXIII ebeam lithography III - contact windows

1. resist
   a) spin 8% 2010 PMMA resist at 2,500 rpm for 30 s
   b) bake at 180 ^oC for 20 min
   c) float coating - one drop of 1.5% 2041 PMMA in cold R.O. water (1 : 1) R.O. water
   d) bake at 180 ^oC for 30 min
   e) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   f) bake at 180 ^oC for 30 min
   g) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   h) bake at 180 ^oC for 30 min
   i) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   j) bake at 180 ^oC for 30 min
   k) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
   l) bake at 180 ^oC for 30 min
   m) remove residue from the back side of wafer with acetone and cotton bud

2. expose windows with a dose of 1900, using the 4 nm spot and a VRU of 2, resolution of 1 nm.
3. resist development
   a) develop in IPA:MIBK (2.5 : 1) at 23^oC for 30 s
   b) rinse in IPA for 3 min
   c) N_2 blow dry
4. removing resist residue
   a) barrel asher at 40 W for 1 min

XXIV wet etch - pattern transfer

1. etch $NiCr$ with MS 8 chrome etchant for 35 s
2. rinse in IPA for 5 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry

XXV stripping resist

1. solvent cleaning (not in ultrasonic bath!) - see section J.3 - with a rinse in acetone for 15 min

XXVI removing Ni residue

1. rinse in 69% nitric acid (3 : 7) R.O. water for 1 min
2. rinse in R.O. water for 3 min
3. N_2 blow dry

XXVII dry etch

1. dry etch - BP80+RIE - contactwindows (see table E.3)

XXVIII stripping hard mask

1. etch $NiCr$ with MS 8 chrome etchant for 5 min
2. rinse in IPA for 5 min
3. rinse in R.O. water for 5 min
4. N_2 blow dry

XXIX removing Ni residue

1. rinse in 69% nitric acid (3 : 7) R.O. water for 1 min
2. rinse in R.O. water for 3 min
3. N_2 blow dry

XXX ebeam lithography IV - metalization

1. resist
   a) spin 8% 2010 PMMA resist at 2,500 rpm for 30 s
   b) bake at 180 ^oC for 20 min
   c) float coating - one drop of 2.5% 2010 PMMA resist in cold R.O. water (1 : 1) R.O. water
   d) bake at 180 ^oC for 30 min
   e) float coating - one drop of 2.5% 2010 PMMA resist in cold R.O. water (1 : 1) R.O. water
   f) bake at 180 ^oC for 30 min
   g) float coating - one drop of 2.5% 2010 PMMA resist in cold R.O. water (1 : 1) R.O. water
   h) bake at 180 ^oC for 30 min

i) float coating - one drop of 2.5% 2010 PMMA resist in cold R.O. water (1 : 1) R.O. water
j) bake at 180 ^oC for 30 min
k) float coating - one drop of 2.5% 2010 PMMA resist in cold R.O. water (1 : 1) R.O. water
l) bake at 180 ^oC for 30 min
m) float coating - one drop of 2.5% 2010 PMMA resist in cold R.O. water (1 : 1) R.O. water
n) bake at 180 ^oC for 30 min
o) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
p) bake at 180 ^oC for 30 min
q) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
r) bake at 180 ^oC for 30 min
s) float coating - one drop of 1.5% 2041 PMMA resist in cold R.O. water (1 : 1) R.O. water
t) bake at 180 ^oC for 30 min
u) remove residue from the back side of wafer with acetone and cotton bud

2. expose windows with a dose of 2250, using the 50 nm spot and a VRU of 35, resolution of 1 nm.
3. resist development
   a) develop in IPA:MIBK (2.5 : 1) at 23^oC for 30 s
   b) rinse in IPA for 3 min
   c) N_2 blow dry
4. removing resist residue
   a) barrel asher - 40 W for 30 s

XXXI metalization

1. evaporate 150 nm of Al (deposition rate: 18 nm/min)
2. lift-off for 2 $hours$ in warm acetone
3. rinse in methanol for 5 min
4. rinse in IPA for 5 min
5. rinse in R.O. water for 5 min
6. N_2 blow dry
7. inspect under SEM
8. anneal contacts in RTA (see table I.1)
9. test devices electronically

Appendix D

Release etch process

I photolithography - cantilever release

1. dehydration bake - hot plate at 180 ^oC for 6 min
2. resist
   a) apply primer 80/20[1] to the whole wafer
   b) wait for 30 s
   c) spin at $4,000$ rpm for 7 s
   d) wait for 30 s
   e) spin AZ4562 resist at $1,000$ rpm (acceleration 200 rpm/s^2) for 30 s
   f) wait for 15 min
   g) clean bottom side of resist with acetone and cotton bud
   h) bake on hot plate[2]
      · bake at 50 ^oC for 2 min
      · bake at 100 ^oC for 14 min
      · bake at 50 ^oC for 2 min
   i) leave overnight in MA6 room to allow time for rehydration of resist
3. exposure - soft contact, gap 120 μm, 10 cycles (5 s esposure and 10 s wait) (use blue foil)
4. resist development
   a) develop in AZ 400k developer (1 : 4) R.O. water for 3.5 min
   b) rinse in R.O. water for 3 min
   c) N_2 blow dry

II dry etch - cantilever release etch

1. attach the wafer to carrier plate with thin layer of s1818 resist applied by a finger
2. bake in oven at 90 ^oC for 30 min
3. dry etch - STS - release (see table G.1)
4. lift-off in plenty of acetone (deep petri dish) for 4 h
5. rinse wafer in methanol for 5 min
6. N_2 blow dry very gently (at a distance)
7. dry etch - BP80+RIE - O2-ash-20 (see table E.6)

[1] 1 min bath in Surpass 3000 or Surpass 4000 can be used instead.
[2] possbile to use oven instead - oven bake at 90 ^oC for 40 min

Appendix E

BP80+RIE processes

parameter	run#1	run#2
process gas required	O_2	CHF_3
gass flow ($sccm$)	40	30
process pressure ($milliTorr$)	50	30
rf power (W)	40	200
processing time ($m:s$)	5 : 00	$\sim 7:00^a$
etch (nm/min)	–	40

[a] use interferometer, overetch for 45 s

TABLE E.1: *Process for etching* 300 nm SiO_2 *in BP80+RIE - name: phosdiffwindows.*

parameter	run#1	run#2
process gas required	O_2	CHF_3
gass flow ($sccm$)	40	30
process pressure ($milliTorr$)	50	30
rf power (W)	40	200
processing time ($m:s$)	5 : 00	$\sim 9:30$
etch (nm/min)	–	40

TABLE E.2: *Process for etching* 300 nm SiO_2 *in BP80+RIE - name: borondiffwindows.*

parameter	run#1	run#2
process gas required	O_2	CHF_3
gas flow ($sccm$)	40	30
process pressure ($milliTorr$)	50	30
rf power (W)	40	200
processing time ($m:s$)	5 : 00	$\sim 1:00^a$
etch rate (nm/min)	–	40

[a] use interferometer, overetch for $10-15$ s

TABLE E.3: *Process for etching* 15 nm SiO_2 *in BP80+RIE - name: contactwindows.*

parameter	run#1	run#2
process gas required	O_2	$CHF_3 + Ar$
gass flow ($sccm$)	40	25/18
process pressure ($milliTorr$)	50	30
rf power (W)	40	200
processing time ($m:s$)	5 : 00	$\sim 7:00^a$
etch (nm/min)	–	40

[a] use interferometer, overetch for 45 s

TABLE E.4: *Process for etching* 300 nm SiO_2 *in BP80+RIE - name: chf3argonetch.*

parameter	run#1
process gas required	O_2
gas flow ($sccm$)	50
process pressure ($milliTorr$)	50
rf power (W)	80
processing time ($m:s$)	10 : 00

TABLE E.5: *Process for* O_2 *ash in BP80+RIE - name: O2-ash-80.*

parameter	run#1
process gas required	O_2
gas flow ($sccm$)	50
process pressure ($milliTorr$)	50
rf power (W)	20
processing time ($m:s$)	5 : 00

TABLE E.6: *Process for* O_2 *ash in BP80+RIE - name: O2-ash-20.*

parameter	run#1	run#2
process gas required	O_2	SF_6/N_2
gass flow ($sccm$)	40	5/45
process pressure ($milliTorr$)	50	10
rf power (W)	40	10
processing time ($m:s$)	5 : 00	timed etch
etch rate (nm/min)	–	4.5

TABLE E.7: *Process for slow Si etching in BP80+RIE - name: slowsietch.*

Appendix F

BP80 processes

parameter	run#1	run#2	run#3
process gas required	O_2	C_2F_6	O_2
gas flow ($sccm$)	10	20	20
process pressure ($milliTorr$)	50	23	50
rf power (W)	10	100	40
processing time ($m:s$)	1 : 00	5 : 00	5 : 00

TABLE F.1: *Process for stripping* 40 *nm* SiO_2 / 60 *nm* Si_3N_4 *layers in BP80 - name: bothdielectrics.*

parameter	run#1
process gas required	O_2
gas flow ($sccm$)	50
process pressure ($milliTorr$)	50
rf power (W)	80
processing time ($m:s$)	10 : 00

TABLE F.2: *Process for* O_2 *ash in BP80 - name: O2-ash-80-bp80.*

Appendix G

STS processes

parameter	run#1	run#2
process name	Xu_ash2	$udo1$
processing time $(m:s)$	1 : 00	depends[a]

[a]depends on membrane thickness, use interferometer camera, overetch for 5 *min*

TABLE G.1: *Process for release etch of Si cantelevers in STS - name: release.*

parameter	etch	passivation
process gas required	O_2/SF_6	C_4F_8
gas flow $(sccm)$	10/130	85
process pressure $(milliTorr)$	APC angle 74%	
power coil (W)	600	600
platen	12	0
processing time $(m:s)$	00 : 13	00 : 07

TABLE G.2: *Process implementing Bosch process for DRIE etching of Si - etch rate 2 $\mu m/min$ - name: udo1.*

parameter	run#1
process gas required	O_2
gas flow $(sccm)$	100
process pressure $(milliTorr)$	90
power coil (W)	400
platen	0
processing time $(m:s)$	01 : 00

TABLE G.3: *Process for O_2 ash in STS - name: Xu_ash2.*

Appendix H

Furnace - level 7

process	gas [sccm]	ramp	hold
15 nm of SiO_2	25 O_2	30 $min \rightarrow 700^oC$	-
		20 $min \rightarrow 900^oC$	1 h 40 $min \rightarrow 900^oC$
15 nm of SiO_2	25 O_2	30 $min \rightarrow 650^oC$	-
		20 $min \rightarrow 850^oC$	3 h 55 $min \rightarrow 850^oC$
15 nm of SiO_2	25 O_2	30 $min \rightarrow 600^oC$	-
		20 $min \rightarrow 775^oC$	17 h 15 $min \rightarrow 775^oC$
300 nm of SiO_2	25 O_2[a]	30 $min \rightarrow 750^oC$	-
		20 $min \rightarrow 950^oC$	1 h 16 $min \rightarrow 950^oC$
600 nm of SiO_2	25 O_2[1]	30 $min \rightarrow 750^oC$	-
		20 $min \rightarrow 950^oC$	3 h 17 $min \rightarrow 950^oC$
P diffusion[b]	475 Ar, 25 O_2	30 $min \rightarrow 550^oC$	120 $min \rightarrow 550^oC$
		30 $min \rightarrow 900^oC$	100 $min \rightarrow 900^oC$
B diffusion[c]	475 Ar, 25 O_2	30 $min \rightarrow 550^oC$	120 $min \rightarrow 550^oC$
		30 $min \rightarrow 900^oC$	130 $min \rightarrow 900^oC$

[a] pass through bubbler with H_2O
[b] phosphorous diffusion depth - 200 nm
[c] boron diffusion depth - 150 nm

TABLE H.1: *Furnace processes.*

Appendix I

RTA

process	gas	ramp	hold
Al contacts	N_2	10 $s \rightarrow 200^oC$	10 $s \rightarrow 200^oC$
		10 $s \rightarrow 350^oC$	10 $s \rightarrow 350^oC$
		10 $s \rightarrow 400^oC$	600 $s \rightarrow 400^oC$
		10 $s \rightarrow 20^oC$	-
dopant test	O_2	10 $s \rightarrow 200^oC$	10 $s \rightarrow 200^oC$
		10 $s \rightarrow 300^oC$	1800 $s \rightarrow 300^oC$
		10 $s \rightarrow 20^oC$	-

TABLE I.1: *RTA processes.*

Appendix J

Notes

J.1 Wafer specification

3" silicon, $< 100 >\ \pm 0.5^o$

resistivity: $1\ -\ 10\ \Omega\ \cdot\ cm$

dopant: Phosphorous

doping level: $4.5\ \cdot\ 10^{14}\ -\ 4.9\ \cdot\ 10^{15}\ \frac{atoms}{cm^3}$

thickness: $380 \pm 2\ \mu m$

double side polished (dsp) with 40 nm of dry thermally grown SiO_2 and 60 nm of LPCVD Si_3N_4 on both sides

J.2 KOH etch rates and uniformity results

sample id	avg. depth $[\mu m]$	error $[\mu m]$	error [%]	etch rate $[\frac{\mu m}{min}]$
id 205	363	2.6	0.72	1.15
id 204	366	2.0	0.55	1.15
id 203	364	2.3	0.63	1.15
id 202	354	2.0	0.56	1.12
id 201	333	2.6	0.78	1.05
samples processed after beaker replacement				
id 511	353	2.3	0.65	1.11
id 514	350	1.9	0.54	1.10

TABLE J.1: *KOH etch uniformity and etch rates for* 5 *h* 17 *min etch.*

J.3 Solvent cleaning process

1. acetone in ultrasonic bath (if indicated, otherwise stir gently) for 5 *min*

2. methanol in ultrasonic bath (if indicated, otherwise stir gently) for 5 min
3. IPA in ultrasonic bath (if indicated, otherwise stir gently) for 5 min
4. rinse in R.O. water for 3 min
5. N_2 blow dry

Appendix K

Vistec VB6 - understanding resolution

resolution - the smallest distance between two spots, which the beam can expose. The resolution takes one of the 3 values: 0.5 nm, 1 nm or 1.25 nm.

field size - the maximum area which can be exposed to the electron beam by beam deflection without stage motion. This limit is imposed by the $20 - bit$ DAC converter e.g. for 1.25 nm resolution the maximum square field size is equal to $(1.310720\ mm)^2$. For larger patterns than the field size a stage motion is required.

beam spot size - the size of the beam spot can take one of the values: 4 nm, 6 nm, 9 nm, 12 nm, 19 nm, 24 nm, 33 nm, 45 nm or 50 nm. Usually this value is selected as $feature\ size \geq 5 \cdot beam\ spot\ size$.

beam step size (BSS) - for a specific pattern it is the distance between two consecutively exposed spots. Its value is equal to

$$BSS = resolution \cdot VRU \tag{K.1}$$

variable resolution unit (VRU) - it is a multiplier.

feature size - the smallest dimension of the pattern to be written.

dose - amount of charge that is used for exposure given as in $\mu C/cm^2$. Its value is pattern and lithography (type of resist, resist thickness) dependent. Usually before writing the actual pattern, a dose test is run to discover the dose value which does not cause under/overexposure.

Appendix L

Threshold voltage calculations

Based on [116]:

$\phi_m = 4.1\ V$ - work function for Al

$\phi_s = 4.05\ V$ - work function for Si

$E_g = 1.12\ eV$ - energy gap for Si

$k = 1.38 \cdot 10^{-23}\ J/K$ - Boltzmann constant

$T = 300\ K$ - temperature

$q = 1.6 \cdot 10^{-19}$ - electrical charge

$V_t = \frac{kT}{q} = 0.25875\ V$

$n_i = 1.45 \cdot 10^{10}\ 1/cm^3$

$N_d = 1 \cdot 10^{15}\ 1/cm^3$

$\epsilon = 8.85 \cdot 10^{-12}\ F/m = 8.85 \cdot 10^{-14}\ F/cm$

$\epsilon_{Si} = 11.7$ - dielectric constant for Si

$\epsilon_{ox} = 3.9$ - dielectric constant for SiO_2

$t_{ox} = 15\ nm = 15 \cdot 10^{-7}\ cm$ - SiO_2 thickness

$$V_{th} = V_{fb} - 2\phi_F - \frac{\sqrt{2\ q\ N_d\ \epsilon\ \epsilon_{Si}\ 2\ \phi_F}}{C_{ox}} \tag{L.1}$$

$$V_{fb} = \phi_m - \phi_s - \frac{E_g}{2e} + \phi_F \tag{L.2}$$

$$V_{th} = \phi_m - \phi_s - \frac{E_g}{2e} - \phi_F - \frac{\sqrt{2\ q\ N_d\ \epsilon\ \epsilon_{Si}\ 2\ \phi_F}}{C_{ox}} \tag{L.3}$$

$$\phi_F = V_t \; ln(\frac{N_d}{n_i}) = 0.25875 \; ln(\frac{10^{15}}{1.45 \cdot 10^{10}}) = 0.288283 \; V \tag{L.4}$$

$$C_{ox} = \frac{\epsilon \; \epsilon_{ox}}{t_{ox}} = \frac{8.85 \cdot 10^{14} \cdot 3.9}{15 \cdot 10^{-7}} = 2.301 \cdot 10^{-7} \; C/cm^2 \tag{L.5}$$

$$V_{th} = \phi_m - \phi_s - \frac{E_g}{2e} - \phi_F - \frac{\sqrt{2 \; q \; N_d \; \epsilon \; \epsilon_{Si} \; 2 \; \phi_F}}{C_{ox}} = 4.1 - 4.05 - \frac{1.12}{2} - 0.288283 + \\ - \frac{\sqrt{2 \cdot 1.6 \cdot 10^{-19} \cdot 10^{15} \cdot 8.85 \cdot 10^{-14} \cdot 11.7 \cdot 2 \cdot 0.288283}}{2.301 \cdot 10^{-7}} = \textbf{-0.86 V} \tag{L.6}$$

Appendix M

Current calculations in saturation region

When the device operates within saturation region ($V_{ds} \geqslant V_{gs} - V_{th}$ and $V_{gs} \geqslant V_{th}$) the drain current I_d is given by [116]

$$I_d = \frac{KP_h}{2} \cdot \frac{W}{L}(V_{gs} - V_{th})^2 \tag{M.1}$$

where the transconductance parameter KP_p is

$$KP_h = \mu_h \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{M.2}$$

ε_{ox} is the dielectric constant of the gate oxide ($3.97 \cdot 8.85 \cdot 10^{-12}\ F/m$) and t_{ox} is the gate oxide thickness.

For gate length $L = 1.35\ \mu m$, gate width of $W = 0.75\ \mu m$, oxide thickness $t_{ox} = 150$ Å, voltages $V_{gs} = -7.5\ V$ and $V_{th} = -0.86\ V$ (from appendix L)

$$KP_h = \mu_h \cdot \frac{\varepsilon_{ox}}{t_{ox}} = 0.045 \cdot \frac{3.97 \cdot 8.85 \cdot 10^{-12}}{15 \cdot 10^{-9}} = 1054035 \cdot 10^{-4}\ [S] \tag{M.3}$$

$$I_d = \frac{KP_h}{2} \cdot \frac{W}{L}(V_{gs} - V_{th})^2 = \frac{0.1054035}{2} \cdot \frac{0.75}{1.35}(-7.5 + 0.86)^2 = 1.29\ [mA] \tag{M.4}$$

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