UNIVERSITY OF GLASGOW

# A NOVEL AlGaN/GaN BASED ENHANCEMENT MODE HIGH ELECTRON MOBILITY TRANSISTOR WITH SUB-CRITICAL BARRIER THICKNESS

by

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# Abstract

Power-switching devices require low on-state conduction losses, high-switching speed, high thermal stability, and high input impedance. Using gallium nitride (GaN) based field-effect transistors, these properties for switching devices can be satisfied. GaN-based High Electron Mobility Transistors (HEMTs) are emerging as promising candidates for high-temperature, high-power (power electronics) and radio-frequency (RF) electronics due to their unique capabilities of achieving higher current density, higher breakdown voltage, higher operating temperatures and higher cut-off frequencies compared to silicon (Si). Conventional GaN HEMTs with an aluminium gallium nitride (AlGaN) barrier are of depletion-mode (d-mode) or normally-on which require a negative polarity power supply to turn off. On the other hand, enhancement-mode (e-mode) or normally-off AlGaN/GaN HEMTs are attracting increasing interest in recent years because no negative gate voltage is necessary to turn off the devices. This leads to the advantage of simple circuit design and low stand-by power dissipation. For power electronics applications, power switches which incorporate e-mode devices provide the highly desirable essential fail-safe operation.

In this research, a new high performance normally-off GaN-based metal-oxide-semiconductor (MOS) high electron mobility transistor (HEMT) that employs an ultra-thin sub-critical 3 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and relies on an induced two dimensional electron gas (2DEG) for operation was designed, fabricated and characterized. The device consists of source and drain Ohmic contacts nominally overlapped by the gate contact and employs a gate dielectric. With no or low gate-to-source voltage ($V_{GS}$), there is no two dimensional electron gas (2DEG) channel at the AlGaN/GaN interface to allow conduction of current between the drain and source contacts as the AlGaN barrier thickness is below the critical thickness required for the formation of such channel. However, if a large enough positive bias voltage $V_{GS}$ is applied, it causes the formation of a quantum well at the AlGaN/GaN interface into which electrons from the source and drain Ohmic regions are attracted (by the positive gate voltage), effectively creating a 2DEG channel, and so the structure is a normally-off field effect transistor.

Normally-off GaN MOS-HEMT devices were fabricated using plasma enhanced chemical vapour-deposited (PECVD) silicon dioxide ($SiO_2$) as the gate dielectric. They demonstrated positive threshold voltages ($V_{th}$) in the range of +1 V to +3 V, and very high maximum drain currents ($I_{DSmax}$) in the range of 450 mA/mm to 650 mA/mm, at high gate voltage ($V_{GS}$) of around 6 V. The devices also exhibited breakdown voltages in the range of 9 V and 17 V depending on the gate dielectric thickness, making them suitable for realising high current low voltage power devices required, for instance, for buck converters for mobile phones, tablets, laptop chargers, etc.

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# Publications

1. R. Brown, D. Macfarlane, A. Al-Khalidi, X. Li, G. Ternent, H. Zhou, I. Thayne and E. Wasige, "A Sub-Critical Barrier Thickness Normally-Off AlGaN/GaN MOS-HEMT," *IEEE Electron Device Letters*,vol. 35, no. 9, pp. 906-908, September 2014.

2. R. Brown, A. Al-Khalidi, D. Macfarlane, S. Taking, G. Ternent, I. Thayne and E. Wasige, "Novel High Performance AlGaN/GaN based Enhancement-Mode Metal-Oxide Semiconductor High Electron Mobility Transistor," *Physica Status Solidi (C)*, vol. 11, no. 3-4, pp. 844-847, January 2014.

3. R. Brown, A. Al-Khalidi, D. Macfarlane, S. Taking and E. Wasige, "A Novel High Performance AlGaN/GaN based Enhancement-Mode Metal-Oxide-Semiconductor High Electron Mobility Transistor," *The* $10^{th}$ *International Conference on Nitride Semiconductors.* Washington, August 2013.

4. R. Brown, A. Al-Khalidi, G. Ternent, I. Thayne and E. Wasige, "A Normally-off AlGaN/GaN MOSHEMT Technology," *The* $22^{nd}$ *European Workshop on Heterostructure Technology.* Glasgow, September 2013.

5. R. Brown, A. Al-Khalidi, D. Macfarlane, S. Taking, G. Ternent, I. Thayne and E. Wasige, "A Normally-off AlGaN/GaN HEMT Technology," *UK Nitrides Consortium.* Sheffield, July 2013.

6. J. Sinclair, R. Brown, A. Al-Khalidi and E. Wasige, "Fabrication and Characterisation of normally-off GaN-based MOS-HEMTs," *The* $7^{th}$ *Institution of Engineering and Technology International Conference on Power Electronics, Machines and Drives.* Manchester, April 2014.

7. J. Wang, K. Alharbi, A. Ofiare, R. Brown, A. Khalid, D. Cumming and E. Wasige, "MMIC Resonant Tunnelling Diode Oscillators for THz applications," *The* $11^{th}$ *Conference on PhD Research in Microelectronics and Electronics (IEEE PRIME 2015).* Glasgow, June 2015.

8. J. Wang, K. Alharbi, A. Ofiare, R. Brown, A. Khalid, D. Cumming and E. Wasige, "D-band Resonant Tunnelling Diode Oscillator with High Output Power," *UK Semiconductors 2015.* Sheffield, July 2015.

9. A. Ofiare, R. Brown, J. Wang, K. Alharbi, A. Khalid, D. Cumming and E. Wasige, "Accurate Pulsed I-V Measurement of the NDR Region of Tunnel Diode and Resonant Tunnelling Diodes," *UK Semiconductors 2015.* Sheffield, July 2015.

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# Abbreviations

| | |
|---|---|
| **2DEG** | **T**wo **D**imensional **E**lectron **Gas** |
| **ALD** | **A**tomic **L**ayer **D**eposition |
| **AlGaN** | **A**luminium **G**allium **N**itride |
| **AlN** | **A**luminium **N**itride |
| **BFOM** | **B**aliga's **F**igure **O**f **M**erit |
| **BHFFOM** | **B**aliga's **H**igh **F**requency **F**igure **O**f **M**erit |
| **CFOM** | **C**ombined **F**igure **O**f **M**erit |
| **CVD** | **C**hemical **V**apour **D**eposition |
| **ECR-RIE** | **E**lectron-**C**yclotron-**R**esonance **R**eactive **I**on **E**tching |
| **FET** | **F**ield **E**ffect **T**ransistor |
| **FOM** | **F**igure **O**f **M**erit |
| **GaN** | **G**allium **N**itride |
| **HEMT** | **H**igh **E**lectron **M**obility **T**ransistor |
| **HVPE** | **H**ydride **V**apour **P**hase **E**pitaxy |
| **ICP-CVD** | **I**nductively-**C**oupled-**P**lasma **C**hemical **V**apour **D**eposition |
| **ICP-RIE** | **I**nductively-**C**oupled-**P**lasma **R**eactive **I**on **E**tching |
| **InGaN** | **I**ndium **G**allium **N**itride |
| **JFET** | **J**unction **F**ield **E**effect **T**ransistor |
| **JFOM** | **J**ohnson's **F**igure **O**f **M**erit |
| **KFOM** | **K**eyes **F**igure **O**f **M**erit |
| **MBE** | **M**olecular **B**eam **E**pitaxy |
| **MISFET** | **M**etal-**I**nsulator **F**ield **E**ffect **T**ransistor |
| **MOCVD** | **M**etal **O**rganic **C**hemical **V**apour **D**eposition |
| **MOSFET** | **M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor |
| **MOSHEMT** | **M**etal-**O**xide-**S**emiconductor **H**igh **E**lectron **M**obility **T**ransistor |

| | |
|---|---|
| **PECVD** | **P**lasma-**E**nhanced **C**hemical **V**apour **D**eposition |
| **RIE** | **R**eactive **I**on **E**tching |
| **Si** | **S**ilicon |
| **SiC** | **S**ilicon **C**arbide |

# Physical Constants

| **Constant Name** | **Symbol** | = | **Constant Value (with units)** |
|---|---|---|---|
| Speed of light | $c$ | = | $2.997\ 924\ 58 \times 10^{8}$ $(m/s)$ (exact) |
| Charge of electron | $e$ | = | $1.602 \times 10^{-19}$ $(Coulombs)$ |
| Plank's constant | $h$ | = | $6.626 \times 10^{-34}$ $(Joules\, sec)$ |
| Mass of electron | $m_e$ | = | $9.109 \times 10^{-31}$ $(Kilograms)$ |
| Reduced Planck's constant | $\hbar$ | = | $1.055 \times 10^{-34}$ $(Joules\, sec)$ |

# Symbols

| | | |
|---|---|---|
| $A$ | Area | $m^2$ |
| $P$ | Power | W ($Js^{-1}$) |
| $E_C$ | Conduction band energy | eV |
| $E_c$ | Critical electric field | $V/m^{-1}$ |
| $E_f$ | Fermi level energy | eV |
| $E_g$ | Bandgap | eV |
| $E_v$ | Valence band energy | eV |
| $\Delta E_v$, $\Delta E_C$ | Discontinuity of the valence/conduction band | |
| | at a heterointerface | eV |
| $\Delta E_g$ | Total difference of the bandgaps | |
| | at a heterointerface | eV |
| $f_{MAX}$ | Maximum frequency of operation | Hz |
| $\Delta f$ | Frequency interval | Hz |
| $f_T$ | Unity current gain cut-off frequency | Hz |
| $Ga_2O_3$ | Gallium oxide | |
| $G_M$ | Transconductance | mS/mm |
| $H_2$ | Hydrogen | |
| $H_2O$ | Water | |
| $I_D$ | Drain current | A |
| $I_{DS}$ | Drain-source current | A |
| $I_S$ | Source current | A |
| $L_{GD}$ | Gate-drain length | m |
| $L_{GS}$ | Gate-source length | m |
| $L_{SD}$ | Source-drain length | m |
| $L_T$ | Transfer length of an Ohmic contact | m |

| | | |
|---|---|---|
| $N_2$ | Nitrogen | |
| $NH_3$ | Ammonia | |
| $P_{PE}$ | Piezoelectric polarization | $C/m^2$ |
| $P_{SP}$ | Spontaneous polarization | $C/m^2$ |
| $R_C$ | Ohmic contact resistance | $\Omega$.mm |
| $R_{CH}$ | Resistance of the channel region | |
| | under the gate-foot | $\Omega$ |
| $R_{DS}$ | Drain-source resistance | $\Omega$ |
| $R_{on}$ | On-resistance of a device | $\Omega$.mm or $\Omega.mm^2$ |
| $R_{SH}$ | Sheet resistance | $\Omega/\square$ |
| $V_{BR}$ | Breakdown voltage | V |
| $V_{DS}$ | Drain-source Voltage | V |
| $V_{FB}$ | Flat band voltage | V |
| $V_{GS}$ | Gate-source voltage | V |
| $V_P$ | Pinch-off voltage | V |
| $V_{TH}$ | Threshold voltage | V |
| $V_x$ | Effective channel voltage | V |
| $SF_6$ | Sulphur hexafluoride | |
| $Si_3N_4, SiN$ | Silicon nitride | |
| $t_{OX}$ | Thickness of oxide | m |
| $T_{OX}$ | Oxidation time | s |
| $W_g$ | Gate width | m |
| $x_0$ | Initial thickness of oxide film | m |
| $v_{sat}$ | Saturation electron velocity | $m/s^{-1}$ |
| | | |
| $\omega$ | angular frequency | $rads^{-1}$ |
| $\varepsilon$ | Permittivity | F/m |
| $\varepsilon_o$ | Vacuum permittivity | F/m |
| $\varepsilon_r$ | Dielectric constant | |
| $\chi, \chi_L$ | Thermal conductivity | W/cm.K |
| $\mu$ | Electron mobility | $cm^2/V.s$ |

*This thesis is dedicated to my late grandmother, Mary Aba Tetteh and my son, Raphael Ilan Brown*

# CHAPTER 1

# INTRODUCTION

Since the production of the first silicon transistor by Gordon Teal in 1954 [1], silicon (Si) has assumed a central role in the development of semiconductor devices. Silicon has been the dominant semiconductor of choice for high-voltage switching applications to date. Recently, however, silicon technology is fast approaching its theoretical limits imposed by the intrinsic material properties such as low saturation velocity, low breakdown voltage, low inversion layer mobility and high device resistance [2]. Due to these limitations, there is growing interest in research activities in modern electronics towards new materials which are able to satisfy the specific needs of higher operating frequencies, higher output power and higher operating voltages. Wide-bandgap semiconductors such as gallium nitride (GaN) and silicon carbide (SiC) have demonstrated the potential for meeting the requirements for high-temperature and high-power switching applications. Figure 1.1 shows the roadmap of the life-cycle of the main semiconductors used in power device technologies, Si, GaN and SiC [3]. It can be seen that wide-bandgap semiconductors such as GaN and SiC are expected to dominate the modern era of power device technology for the foreseeable future. Figure 1.2 shows the relevant material properties for Si, SiC and GaN which include the energy gap, (breakdown) electric field, thermal conductivity, electron velocity, and melting point. This figure gives a good indication of the advantages of GaN over its main competitors in the semiconductor market. The large bandgap energy results in a high electric breakdown field, which is an order of magnitude higher than that of Si. The high electric breakdown field enables the possibility to sustain the application of high bias voltages, thus making GaN suitable for the fabrication of high-voltage devices.

Table 1.1 shows the values of the fundamental material properties of GaN and competing semiconductor materials in power electronics [4–6]. Due to its superior intrinsic

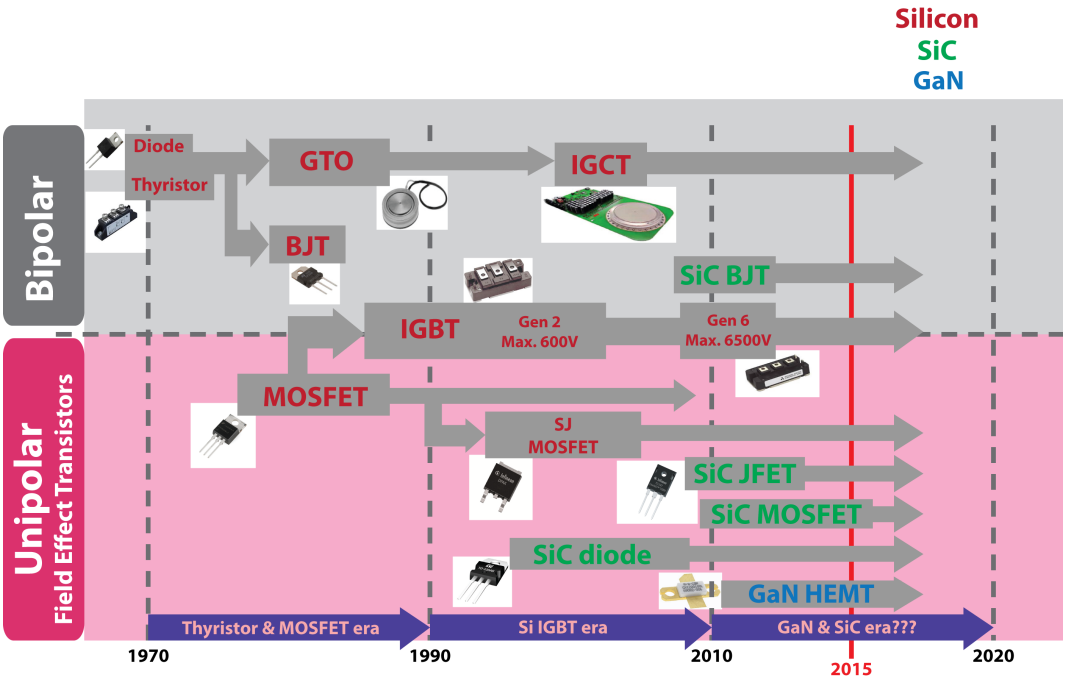



FIGURE 1.1: Roadmap of the life-cycle of competing semiconductor materials, Si, GaN and SiC, indicating a new generation every 20 years.

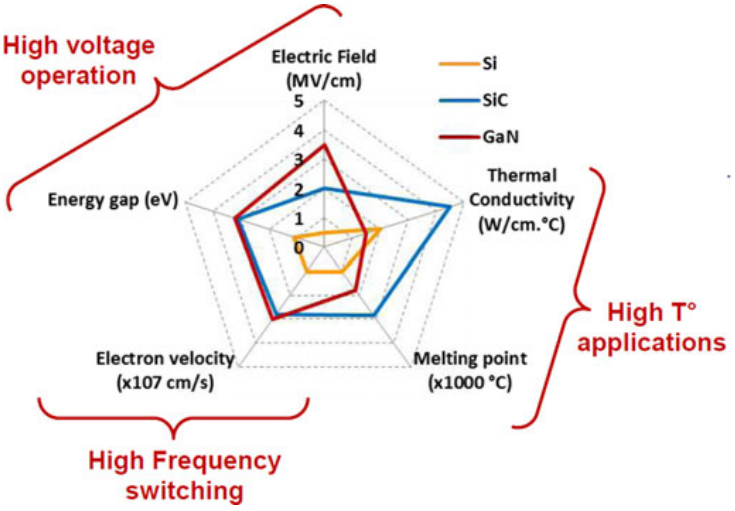



FIGURE 1.2: Summary of Si, SiC and GaN relevant material properties.

physical properties including wide bandgap ($E_g$) of around 3.4 eV, high breakdown electric field ($E_c$) of 3.3 MV/cm, high electron saturation velocity ($v_{sat}$) of $2.5 \times 10^7$ cm/s and high density carriers in the form of two-dimensional electron gas (2DEG) with high mobility ($\mu$) of around 2000 $cm^2$/Vs [5], GaN is considered an outstanding material for high-frequency and high-power devices as well as in the area of opto-electronics. Wide-bandgap semiconductor power devices offer great performance improvements and can work in harsh environments where silicon power devices cannot function. One of the main advantages of III-nitride materials such as gallium nitride (GaN) is the ability to form a heterojunction with a ternary alloy made from another III-nitride semiconductor material such as aluminium gallium nitride (AlGaN). Due to the strong polar material properties, the modification of the material composition results in dramatic modifications of the polar crystal properties and thus of available carrier concentrations obtained at the heterojunction interfaces in the devices. The huge success of III-N materials is not mainly due to the intrinsic bulk material properties, but due to the heterojunction interface properties. In III-N heterostructures, the interfaces allow for the formation of n-channels and intrinsically provide extremely high carrier concentrations $\geqslant 10^{13}\, cm^{-2}$ through polarization engineering without impurity doping [7]. The resulting two-dimensional electron gas (2DEG) at the heterojunction serves as the conductive channel.

The high electric breakdown field of GaN is a result of the wide bandgap of 3.44 eV at room temperature of the material and enables the application of high supply voltages on GaN-based devices, which is one of the two requirements for high-power device performance. The wide bandgap of the material also allows it to withstand high operating temperatures of 300 °C to 700 °C. Large drain currents of greater than 1 A/mm, which are the secondary requirement for a power device, can be achieved due to the high electron mobilities of around 2000 $cm^2$/Vs and high electron sheet densities of around $1 \times 10^{13}$ $cm^{-2}$. These material properties clearly indicate why GaN is a serious candidate for next-generation microwave high-power/high-temperature applications.

Other important parameters that describe the quality of a semiconductor material are the relative permittivity or dielectric constant ($\varepsilon_r$) and the thermal conductivity ($\chi$). The thermal conductivity describes the ease of which heat is conducted in the material, and hence, the possibility to efficiently extract the dissipated power from the device. Materials with lower thermal conductivity typically lead to device degradation at elevated temperatures. Although III-V semiconductors have relatively moderate value of thermal conductivity ($\chi$), GaN has a thermal conductivity of ($1.3\, W cm^{-1} K^{-1}$) which is comparable to that of Si ($1.5\, W cm^{-1} K^{-1}$), which is the dominating semiconductor material of choice in the present electronics industry.

TABLE 1.1: Properties of GaN and competing semiconductor materials in power electronics.

| **Property** | **GaN** | **Si** | **GaAs** | **SiC** | **InP** |
|---|---|---|---|---|---|
| Electron mobility, $\mu$ $(cm^2/V.s)$ | 2000 | 1300 | 5000 | 260 | 5400 |
| Dielectric constant, $\varepsilon_r$ | 9.5 | 11.4 | 13.1 | 9.7 | 12.5 |
| Bandgap, $E_g$ $(eV)$ | 3.4 | 1.1 | 1.4 | 2.9 | 1.35 |
| Electric breakdown field, $E_c$ $(kV/cm)$ | 3300 | 300 | 400 | 2500 | 500 |
| Saturated electron drift velocity, $v_{sat}$ $(\times 10^7\, cm/s)$ | 2.2 | 1.0 | 1.0 | 2 | 1.0 |
| Thermal Conductivity, $\chi$ $(W/cmK)$ | 1.3 | 1.5 | 0.46 | 4.9 | 0.7 |

Beyond the individual material properties, several figures of merit (FOM) have been proposed to benchmark the merit of different semiconductor materials for a given application, with the higher the figure of merit number the better the performance is likely to be. These figures of merit combine the most relevant material properties with respect to high-power and high-frequency applications into one number that represents a rough measure of the relative strengths of the other competing materials. One of the most commonly used is Johnson's Figure of Merit (JFOM), which gives an idea of material suitability for high-power applications at high frequencies and can be calculated using Equation (1.1) [8].

$$JFOM = \left(\frac{E_c v_{sat}}{2\pi}\right)^2 \tag{1.1}$$

where $E_c$ is critical electric field and $v_{sat}$ is saturation electron velocity.

Baliga's Figure of Merit (BFOM), on the other hand, was developed to compare the ultimate performance of field-effect transistors for low-frequency power-switching applications where conduction losses dominate [9]:

$$BFOM = \varepsilon_r \mu E_g^3 \tag{1.2}$$

where $\mu$ is the electron mobility and $\varepsilon_r$ is dielectric constant of the semiconductor.

Baliga's High-Frequency FOM (BHFOM) benchmarks these devices at high-frequency, where switching losses dominate [9]:

$$BHFFOM = \mu E_c^2 V_G^{1/2} / 2V_{BR}^{3/2} \tag{1.3}$$

where $V_G$ is the gate drive voltage and $V_{BR}$ is the breakdown voltage. The latter can be related to an experimental figure of merit involving the on-state specific resistance $R_{on}$ of the device and its critical electric field, $E_c$:

$$FOM = V_{BR}^2 / R_{on} \equiv \varepsilon_r \mu E_c^3 / 4 \tag{1.4}$$

Other FOMs have been proposed for more specific cases. Amongst these, Keyes FOM considers thermal limitations due to transistor switching [9]:

$$KFOM = \chi \left( \frac{c v_{sat}}{4\pi \varepsilon_r} \right)^{0.5} \tag{1.5}$$

where $\chi$ is thermal conductivity and c is the speed of light.

Finally, a Combined FOM (CFOM) was developed to simultaneously account for high-frequency, high-power and high-temperature performance [10]:

$$CFOM = \chi \varepsilon_r \mu v_{sat} E_c^2 \tag{1.6}$$

Table 1.2 compares several figures of merit for the possible high-power and high-frequency performance of GaN relative to other competing semiconductor materials. This table shows that GaN is an excellent candidate for high-frequency power applications. For GaN, the JFOM is about 270 to 480 times that of silicon (Si), about 135 to 240 times that of gallium arsenide (GaAs) and about 1.5 times that of silicon carbide (SiC) [9]. From these figures, it is clear that GaN offers much better high-power/high-frequency performance possibilities than Si, GaAs and SiC. The BFOM of GaN is about 17 to 34 times that of Si, about 1.5 to 2.5 times that of GaAs and about 3 times that of SiC [9]. No matter what FOM is used, wide-bandgap semiconductors offer better performance characteristics for high-frequency, high-power applications. The use

of wide-bandgap materials can be considered amongst one of the best solutions that can meet the requirements of modern day power electronics. Amongst wide-bandgap semiconductors, GaN-based materials are arguably the most matured ones in terms of wafer-size availability, technology and market prospects.

TABLE 1.2: Figures of merit of GaN and competing semiconductor materials in power electronics.

| **Property** | **GaN** | **Si** | **GaAs** | **SiC** |
|---|---|---|---|---|
| Johnson's Figure of Merit, $(JFOM)$ | 270-480 | 1.0 | 2 | 324-400 |
| Keyes Figure of Merit, $(KFOM)$ | 1.4 | 1.0 | 0.4 | 4.5-4.8 |
| Baliga's Figure of Merit, $(BFOM)$ | 17-34 | 1.0 | 13 | 6-12 |
| Baliga's High Frequency Figure of Merit, $(BHFFOM)$, | 86-172 | 1.0 | 10 | 57-76 |
| Combined Figure of Merit, $(CFOM)$ | 108-290 | 1.0 | 4 | 275-310 |
| $T_{max}$, $(^{\circ}C)$ | 700 | 300 | 300 | 600 |

Other advantages of wide-bandgap semiconductor-based power devices compared with silicon-based power devices are as follows:

- Wide-bandgap semiconductor-based power devices can operate at high temperatures of up to 600 °C whilst silicon devices can only operate at a maximum junction temperature of 150 °C although a silicon on insulator (SOI) gate drive integrated circuit (IC) has been demonstrate to operate up to a temperature of around 200 °C [11].
- Due to their higher electric breakdown field, wide-bandgap semiconductor-based power devices have higher breakdown voltages; thus the first commercial SiC schottky diodes are already rated at 600 V compared to silicon schottky diodes which are commercially available typically at 300 V.

- Wide-bandgap semiconductor-based unipolar devices have lower on-resistances, as the on-resistance of a power device is inversely proportional to the cube of the electric breakdown as given by Equation (1.7) [9, 12]. Lower $R_{on}$ means higher overall converter efficiency is attainable.

$$R_{on} = \frac{4(V_{BR})^2}{\varepsilon_r \mu (E_c)^3} \tag{1.7}$$

- Wide-bandgap devices such as SiC have a higher thermal conductivity (4.9 W/cm-K for SiC, as opposed to 1.5 W/cm-K for silicon). Therefore, wide-bandgap semiconductor-based power devices have a lower junction-to-case thermal resistance $R_{th-jc}$. This means that heat is more easily transferred out of the device, and thus the device temperature increase is slower.

## 1.1 Brief History of GaN Technology

The history of GaN began during the early decades of the last century, when in 1930, Johnson et al. prepared gallium nitride by passing ammonia gas on metallic gallium at high temperatures of 900 °C – 1000 °C [13]. In 1938, Juza and Hahn synthesized GaN by passing ammonia ($NH_3$) over liquid gallium at elevated temperatures. This method resulted in a powder consisting of small needles and platelets. Their purpose was to investigate the crystal structure and lattice constant of GaN [14]. However, it was only in 1968 that the first large area GaN epitaxially grown on sapphire substrates by Hydride Vapour Phase Epitaxy (HVPE) was demonstrated [15, 16].

After that discovery, a rapid progress was made in GaN technology leading to 1991 when Khan et al. reported the first evidence of two-dimensional electron gas (2DEG) formation at an $Al_xGa_{1-x}N$/GaN heterojunction grown by metal organic chemical vapour deposition (MOCVD) on sapphire [17]. The first GaN metal semiconductor field-effect transistor (MESFET) and heterostructure field-effect transistor (HFET) grown by metal organic chemical vapour deposition (MOCVD) on sapphire substrates were reported in 1993 and 1994, respectively by Khan et al. [18, 19].

Since the discovery by Khan et al. in 1994, excellent progress has been made in the development of GaN technology. In 2000, AlGaN/GaN HEMT technology was successfully transferred to silicon substrates by Kaiser et al. by growing the heterostructure using Metal Organic Chemical Vapour Deposition (MOCVD) [20].

Another important step in GaN technology was achieved by Tripathy et al. in 2012, by reporting the epitaxial growth, characterization, and device characteristics of crack-free AlGaN/GaN heterostructures on a 200 mm (8 inch) diameter Si(111) substrate [21].

Some of the most important highlights of the scientific research on GaN technology are listed below:

1. In 1930, Johnson et al. demonstrated the first synthesis of GaN [13].
2. In 1938, Juza and Hahn powdered GaN consisting of small needles and platelets in order to study the crystal structure and lattice parameters of GaN [14].
3. In 1959, Grimmeiss at al. conducted the first photo-luminescence measurement on small GaN crystals [22].
4. In 1969, Maruska et al. grew the first single crystal film of GaN, epitaxially grown on a centimetre-sized sapphire substrate using hydride vapour phase epitaxy (HVPE) [15].
5. In 1971, Pankove et al. fabricated the first GaN light emitting diode (LED) [23, 24].
6. In 1972, Maruska et al. fabricated the first hydride vapour phase epitaxy (HVPE) GaN LED using magnesium (Mg) as a p-type dopant, which emits at a wavelength of 430 nm (violet) [25].
7. In 1986, Amano et al. fabricated improved GaN films, grown by metal organic chemical vapour deposition (MOCVD) on sapphire substrates [26].
8. In 1989, Amano et al. was also the first to grow p-type conducting GaN films [27].
9. In 1991, Nakamura grew the first GaN on AlN buffer layer, and observed an improvement in surface morphology which was attributed to the prior deposition of the AlN buffer layer [28].
10. In 1991, Nakamura et al. also grew highly p-typed Mg-doped GaN films with GaN buffer layers which demonstrated the highest hole concentration and lowest resistivity reported to that date [29]. In the same year, Khan et al. made one of the most important discoveries in AlGaN/GaN heterojunctions to date when they reported the first evidence enhanced electron mobility in the form of two-dimensional electron gas (2DEG) formation at an $Al_xGa_{1-x}N$/GaN heterojunction grown by MOCVD on sapphire [17].
11. In 1993, Khan et al. reported the first fabrication and characterization of a metal semiconductor field effect transistor (MESFET) based on single crystal GaN. The GaN layer was deposited over sapphire substrate using low pressure metal organic chemical vapour deposition [18]. Bykhovski et al. also showed during that same year that, strongly pronounced piezoelectric properties play a key role in GaN-AlN-GaN semiconductor-insulator-semiconductor (SIS) and related structures [30].

12. In 1994, Khan et al. also reported the first microwave performance of an AlGaN/GaN heterostructure field-effect transistor(HFET) grown by MOCVD on a sapphire substrate [19].

13. In 1995, Ozgur et al. fabricated the first high transconductance normallv-off GaN based modulation-doped field-effect transistors [31].

14. In 1997, Asbeck et al. quantified the influence of piezoelectric effect on the design and behaviour of III-V nitride heterostructure field-effect transistors (HFETs) grown by both MOCVD and molecular beam epitaxy (MBE) on sapphire and SiC substrates [32].

15. In 1998, Ren et al. fabricated and characterized a GaN metal-oxide semiconductor field-effect transistor (MOSFET) which demonstrates significantly reduced gate leakage and improved I-V characteristics at elevated temperatures [33].

16. In 1999, Yoshida et al. grew the first bipolar junction transistor using only GaN [34].

17. In 2000, Zhang et al. reported on the DC characteristics of the first *pnp* AlGaN/-GaN heterojunction bipolar transistor (HBT) [35].

18. In 2001, Semond et al. reported on the growth of high-electron-mobility AlGaN/-GaN heterostructures on silicon (111) substrates by MBE using ammonia as the nitrogen source [36].

19. In 2006, Cai et al. fabricated a normally-off AlGaN/GaN HEMT which uses a fluoride-based plasma treatment to control the threshold voltages ($V_{th}$) of the device [37].

20. In 2009, Uemoto et al. developed a normally-off GaN-based transistor using conductivity modulation, called a gate injection transistor (GIT). This device principle utilizes hole-injection from the p-AlGaN to the AlGaN/GaN heterojunction, which simultaneously increases the electron density in the channel, resulting in a dramatic increase of the drain current owing to the conductivity modulation [38].

21. In 2012, Tripathy et al. reported crack-free AlGaN/GaN heterostructures grown on 200 mm diameter (111)-oriented silicon substrates and presented an in-depth characterization study of epilayers grown by MOCVD [21].

22. In 2013, Zhang et al. demonstrated E-mode fluorinated MOS-HEMTs with a $V_{th}$ higher than 3 V, no current collapse and long-term stability at 250°C using a dual-gate structure and an $Al_2O_3$ gate oxide deposited by atomic layer deposition [39].

## 1.2 Application Areas of GaN

The direct bandgap of GaN and its alloys enables the material to be used for both optical and electronics applications. At a temperature of 300 K, the bandgap of GaN is 3.44 eV which corresponds to a wavelength of around 360 nm in the near ultraviolet (UV) region of the optical spectrum [40, 41]. The relationship between the bandgap energy ($E_g$) and wavelength is given by Equation (1.8):

$$Bandgap\ Energy\ (E_g) = \frac{hc}{\lambda} \tag{1.8}$$

where $h$ is the Planck's constant, c is the speed of light, $\lambda$ is the wavelength and $1\ eV = 1.6 \times 10^{-19}\ Joules$

Optical applications of GaN include high-brightness blue light emitting diodes (LEDs), backlighting for mobile phones and personal digital assistants (PDAs), and blue-violet laser diodes (LDs).

Figure1.3 shows an overview of GaN-based micro-electronics applications. High frequency applications for GaN-based devices include microwave and millimetre wave amplifiers, RF amplifiers, space and radar electronics including local multipoint distribution systems, military applications inverter systems, digital radio and base station transmitters. Due to the high breakdown voltage of a HEMT, it can work at medium operating voltages like 42 V, hence reducing the cost of circuitry by eliminating the voltage step-down circuit [5]. Power electronics applications for GaN-based HEMTs include electric and hybrid vehicles, electrical inverters, switched mode power supplies and motor drive circuits which operate in the voltage range of 600 V to around 1200 V [4, 42, 43].

## 1.3 Gallium Nitride Power Semiconductors Market

Due to its vast addressable market, the GaN power semiconductors market is quickly expanding. Several transistors, diodes and rectifiers have been in the market since 2008, with extraordinary growth in the volume of power discretes (HEMTs, diodes, rectifiers and FETs) boosting the total revenue of the GaN power semiconductors market. The complete GaN power semiconductors industry shifted to a mass-production scenario in 2011 with the success and revenue potential drawing the focus of several power semiconductor market giants [44].

In 2012, the overall GaN market revenue (including both power and opto segments) accounted for less than 1% ($ 340 million) of the total semiconductors market ($ 34 billion). The GaN power semiconductors market reached $ 12.60 million by the end of 2012. The

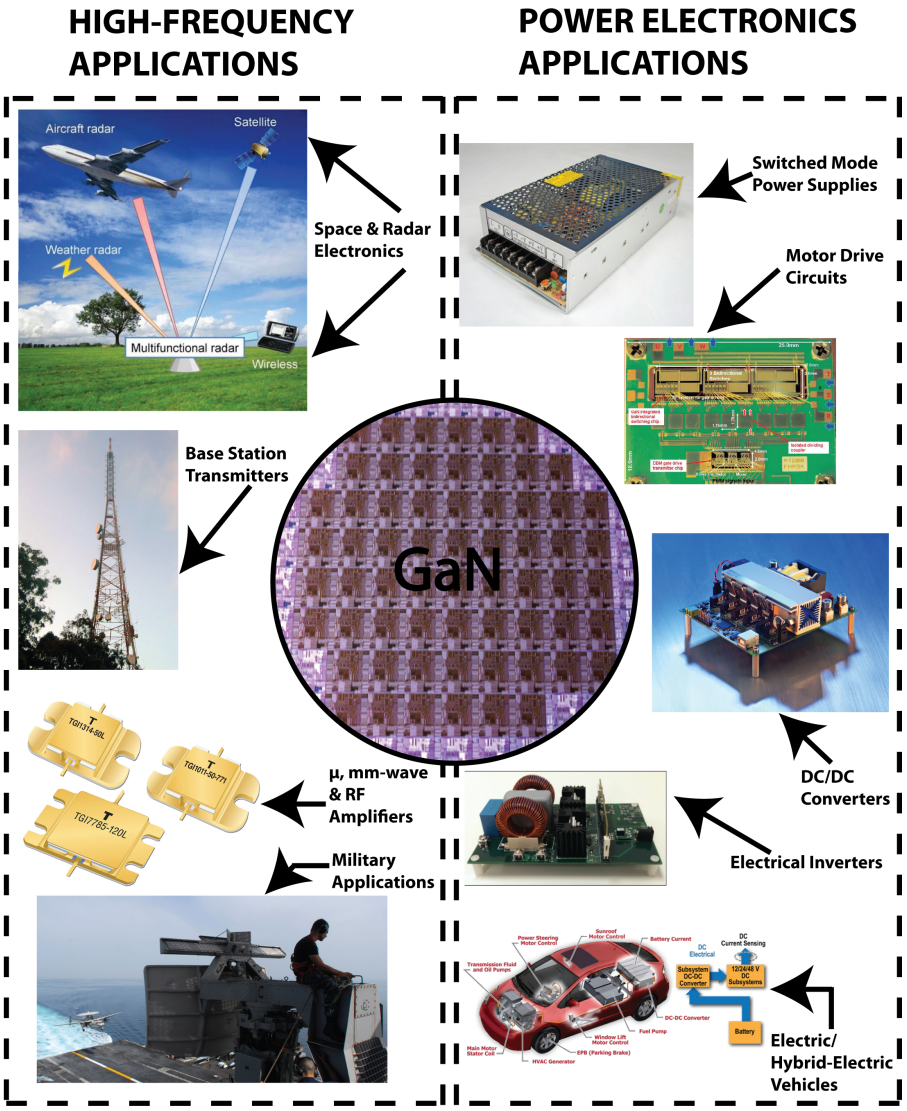
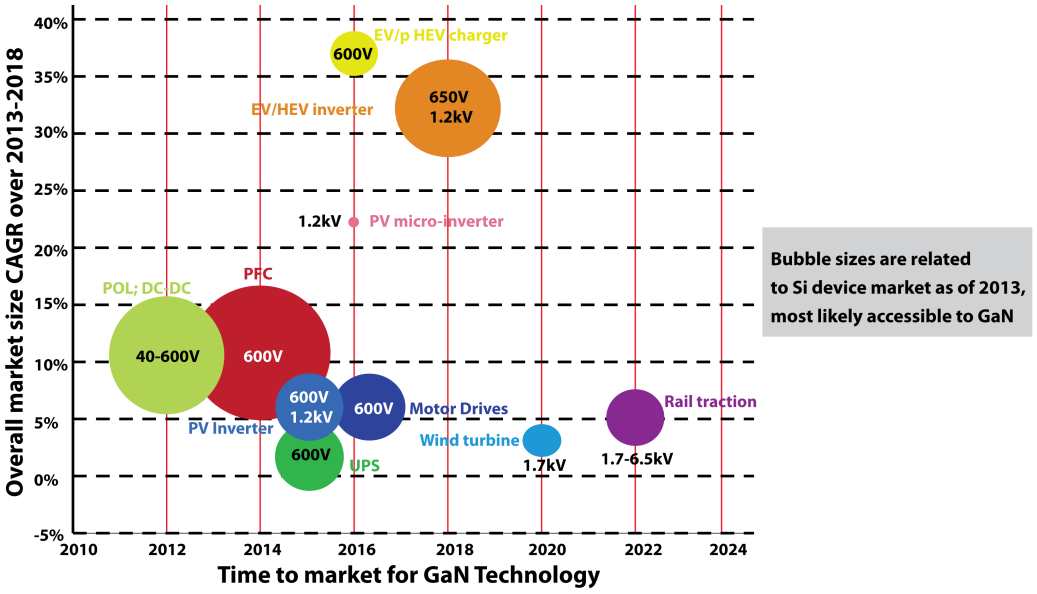



FIGURE 1.3: Electronic applications of GaN-based devices.

phenomenal growth rate of approximately 60 to 80 % year-on-year is expected for the following years. The forecasted revenue for GaN power semiconductors is $ 1.75 billion by end of 2022 at a compound annual growth rate (CAGR) of 63.78 %. According to the Lyon, France-based market research and strategy consulting firm Yole développement, automakers will begin to adopt GaN power devices in inverters, dc-dc converters, and on-board chargers, generating a revenue of around $ 150 million by 2020 as shown in Figure 1.4 [45]. Written in the bubbles is the main device voltage target for GaN, whilst the bubble size is related to Si device market as of 2013, most likely accessible to GaN. Apart from power semiconductors, GaN is predominantly used in optoelectronics for LEDs and laser diodes. The total GaN semiconductors (including both, power and optoelectronics) market revenue is expected to reach $ 2.6 billion at a CAGR of 21.92 % by 2022 [44].




| | POL; DC-DC | PFC | EV/HEV inverter | EV/p HEV charger | PV Inverter | PV micro-inverter | Motor Drives | UPS | Rail traction | Wind turbine |
|---|---|---|---|---|---|---|---|---|---|---|
| **Expected time-to-market for GaN mass volume introduction** | **2012** | **2014** | **2018** | **2016** | **2015** | **2016** | **2016** | **2015** | **2022** | **2020** |
| **CAGR 2013-2018 in %** | **10.5%** | **11.0%** | **32.0%** | **37.0%** | **5.8%** | **22.0%** | **6.8%** | **2.0%** | **5.3%** | **3.3%** |

FIGURE 1.4: Yole's report showing that automakers will begin to adopt GaN power devices in inverters, dc-dc converters, and on-board chargers, generating revenue of $ 150 million by 2020.

## 1.4 Research Aims and Objectives

Conventional GaN-based HEMTs are of depletion mode (D-mode) type but enhancement mode (E-mode) or normally-off devices would be preferable for power electronics since they simplify circuit design by enabling the exclusion of negative-polarity power supply and they also provide the highly desirable essential feature of fail-safe operation [46, 47].

Although a great deal of effort has been made to achieve normally-off AlGaN/GaN HEMTs, the current E-mode HEMT devices do not exhibit high enough threshold voltages for power switching applications ($V_{th}$ in the range of 3-5 V is preferred in order to prevent the mis-operation caused by noise) [48, 49]. Also, current techniques used to realise normally-off operation of these devices have their drawbacks, for example, gate recessed E-mode devices are not easily reproducible and repeatable due to the difficulties in controlling the etch rate to achieve uniform threshold voltage on all devices on a wafer. It has also been proved that physical etching damages the sample surfaces and therefore affects the device performance [50]. For E-mode devices realised using fluorine ion implantation, the plasma treatment normally induces damages and creates defects in the semiconductor material, and consequently degrades the carrier mobility.

This technique is also known to be unreliable as the implanted fluorine ions have the tendency to move around the GaN crystal lattice making the device very unstable [51].

The main aim of this work is therefore to develop an enhancement-mode AlGaN/GaN transistor technology with the following attributes: a positive threshold voltage (3 to 5 V), a low specific on-resistance ($R_{ON}$, approximately between 0.5 $\Omega mm^2$ to 1 $\Omega mm^2$), high drain current ($I_{DS}$, greater than 1 A/mm) and high breakdown voltage ($V_{BR}$, approximately between 100 V to 1500 V).

The specific objectives of this research are to:

- Assess the suitability of a new AlGaN/GaN HEMT with a thin (3 nm) AlGaN barrier layer for normally off operation,
- Develop process modules for fabricating the normally-off AlGaN/GaN HEMT,
- Fabricate the normally-off AlGaN/GaN HEMTs using the developed process flow,
- Characterize the performance of the fabricated devices,
- Optimize the performance of the fabricated transistors.

## 1.5 Organization of Thesis

This thesis is divided into 7 chapters. This chapter, Chapter 1 gives a brief introduction of why wide-bandgap materials and gallium nitride (GaN) in particular have attracted so much attention in the power electronics industry. The chapter also gives a brief history of GaN technology and states some of its application areas. It then goes on to give a brief overview of the impact of GaN in the power semiconductor market. The main aims and objectives of this research project are then presented and discussed briefly.

Chapter 2 describes GaN material properties and polarization effects in the AlGaN/GaN heterostructure. In this chapter, a simulation of the sheet carrier concentration present in the conduction channel at an AlGaN/GaN interface depending on the thickness of AlGaN barrier layer or the aluminium content ($x$) in the AlGaN barrier is then carried out. The layer structure of basic AlGaN/GaN HEMTs and their fundamental operation is introduced. The growth techniques for gallium-based binary and ternary compounds and the choices of substrates for growing GaN are also described. The two main metal contacts, rectifying and Ohmic contacts are then introduced.

Chapter 3 gives an overview of the processing techniques used for fabricating GaN-based devices including etching techniques, lithography and surface passivation.

Chapter 4 reviews some of the current techniques which have been proposed for fabricating enhancement-mode AlGaN/GaN HEMTs and introduces some of their advantages and disadvantages.

Chapter 5 focuses on the development of the fabrication processes used to realise the normally-off GaN transistors in this project. It describes the fabrication processes used for single finger normally-off transistors with focus on the mask design and layout of the transistors. A schematic overview of the process flows used to fabricate the normally-off devices is provided.

Chapter 6 focuses on the fabrication and characterization of the enhancement-mode AlGaN/GaN devices which employ an ultrathin sub-critical 3 nm barrier layer and rely on an induced two-dimensional electron gas for operation. Devices on AlGaN/GaN materials grown on sapphire and silicon substrates are presented here. The results of the performance of these devices are analysed and discussed in this chapter.

Chapter 7 provides a summary of the research project as well as the discussion of potential future work that can be carried out to further improve and enhance the devices studied in this work.

The thesis concludes with appendices A, B and C which provide process details for the devices fabricated in this work, some semiconductor basics and GaN devices with silicon nitride gate dielectric, respectively.

## 1.6 Original Contribution to Research Field

During this research, the author of this thesis was able to:

- Assess the suitability of a new AlGaN/GaN HEMT with a thin (3 nm) AlGaN barrier layer for normally off operation by developing an analytical model of the dependence of polarization induced sheet carrier concentration on the thickness of AlGaN barrier layer or the aluminium content ($x$) in the AlGaN barrier,
- Develop process modules for fabricating a normally-off AlGaN/GaN HEMT,
- Fabricate the normally-off AlGaN/GaN HEMTs using the developed process flow,
- Characterize the performance of the fabricated devices by utilizing test and measurement tools including a probe station and a device parameter analyzer,
- Analyse and discuss the performance of the transistors,
- Make suggestions for future research work that could be carried out to improve the device performance.

# CHAPTER 2

# GaN HIGH ELECTRON MOBILITY TRANSISTORS

As mentioned in Chapter 1, one of the main advantages of GaN-based devices such as AlGaN/GaN high electron mobility transistors (HEMTs) is the formation of a two-dimensional electron gas (2DEG) channel at the interface of the heterostructure. This 2DEG at the heterojunction serves as the conductive channel for large drain currents due to high electron mobility and high electron sheet charge density. In this chapter, the material properties and crystal structure of GaN is discussed, with focus on the polarization effects in the AlGaN/GaN heterostructure. The theory behind the formation of the 2DEG channel in the AlGaN/GaN interface is also discussed and an analytical model of the dependence of polarization induced sheet carrier concentration on the thickness of AlGaN barrier layer or the aluminium content ($x$) in the AlGaN barrier is presented. The typical structure of a GaN-based HEMT is also introduced including the fundamental operation of an AlGaN/GaN HEMT. Some of the techniques used to grow gallium-based compounds, and some substrate choices for growing GaN-based devices are introduced, followed by a brief discussion of the two main metal-semiconductors used in AlGaN/GaN HEMTs. The last section of the chapter gives a brief introduction to the transfer length method (TLM), also known as transmission line model, a technique used to characterize the quality of Ohmic contacts.

## 2.1 GaN Material System

In this section, the material properties and crystal structure of III-Nitride semiconductors, in particular for GaN, are discussed. The effects of polarization on the 2DEG channel formed in the AlGaN/GaN heterostructure will also be briefly described.

### 2.1.1 Material Properties and Crystal Structure of III-Nitride Semiconductors

Group III-Nitride semiconductors can be found in three common crystal structures; wurtzite, zincblende, and rock salt. The zincblende structure can also be found for GaN for thin films [52]. The rock salt phase is of no importance to electronic devices so far. At room temperature and atmospheric pressure, the wurtzite structure is the thermodynamically stable phase for GaN and consists of two inter-penetrating hexagonal close-packed lattices (HCP), which are shifted with respect to each other by $(3/8)c_0$ where $c_0$ is the height of the hexagonal lattice cell. The unit cell of the wurtzite lattice is hexagonal with a basis of four atoms, two nitrogen and two gallium atoms, see Figure 2.1. It contains six atoms and it is characterized by two lattice constants, $a_0$ (3.18 Å) and $c_0$ (5.18 Å) [53]. In this structure, growth is typically performed along the c-axis.

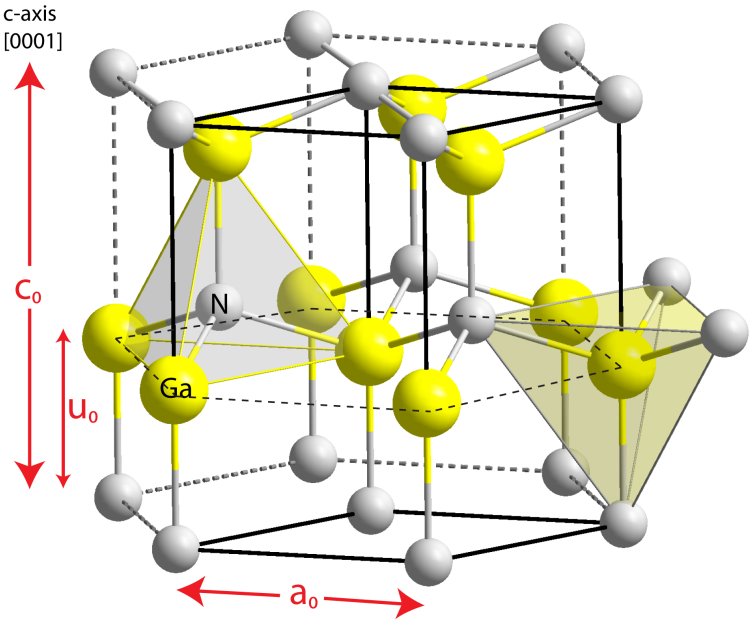



FIGURE 2.1: Wurtzite unit cell of GaN showing the lattice constants $a_0$ and $c_0$.

The chemical bonds of III-nitride compounds such as GaN are predominantly covalent, which means that, each atom is tetrahedrally bonded to four atoms of the other type. There is also an ionic contribution of the bond which determines the stability of the structural phase due to the large difference in electronegativity of Ga and N atoms. There is no inversion symmetry in this lattice along the [0001] direction or $c$-axis, which by convention is the direction shown by the vector pointing from a Ga atom to the nearest neighbouring N atom. Lack of inversion symmetry means that, when defining an atom position on a close-packed plane with coordinates $(x, y, z)$, it is not invariant

to the position $(-x, -y, -z)$ since inversion results in replacement of group III atoms by nitrogen atoms and vice versa. As a result of the lack of symmetry, all atoms on the same plane at each side of a bond are the same. Hence, wurtzite GaN crystals have two distinct faces, commonly known as Ga-face and N-face, which correspond to the (0001) and $(000\bar{1})$ crystalline faces as shown in Figure 2.2.

Figure 2.1 also shows the three parameters that define the wurtzite lattice. These are the edge length of the basal hexagon ($a_0$), the height of the hexagonal lattice cell ($c_0$), and the cation-anion bond length ratio ($u_0$) along the [0001] direction in units of $c_0$. The subscript "0" indicates that these values are those of the equilibrium lattice. In an ideal wurtzite crystal, the $c_0/a_0$ ratio equals $\sqrt{\frac{8}{3}} = 1.633$ and the value for $u_0$ is 0.375. Because of the different metal cations, the bond lengths and the resultant $c_0/a_0$ ratios of AlN, GaN, and InN are different. Table 2.1 shows an overview of these lattice parameters of wurtzite III-nitrides at 300 K [54]. From Table 2.1, it is clear that GaN is closest to the ideal wurtzite structure, followed by InN and AlN. This fact is very important because the degree of non-ideality is a significant factor in determining the strength of polarization in III-nitrides, which will be discussed further in Section 2.1.2.

TABLE 2.1: Lattice parameters of wurtzite III-nitrides at 300 K.

| **Parameter** | **Ideal** | **AlN** | **GaN** | **InN** |
|---|---|---|---|---|
| $a_0$, (Å) | – | 3.112 | 3.189 | 3.54 |
| $a_0$, (Å) | – | 4.982 | 5.185 | 5.705 |
| $c_0/a_0$ [expected] | – | 1.6010 | 1.6259 | 1.6116 |
| $c_0/a_0$ [calculated] | 1.633 | 1.6190 | 1.6336 | 1.6270 |
| $u_0$ | 0.375 | 0.380 | 0.376 | 0.377 |

### 2.1.2 Polarization Effects in the AlGaN/GaN Heterostructure

In the absence of external electric fields, the total polarization ($P$) of a GaN or AlGaN layer is the sum of spontaneous polarization $P_{SP}$ and piezoelectric polarization $P_{PE}$. Spontaneous polarization arises from the lack of symmetry of the wurtzite crystal, whereas piezoelectric polarization, is a result of the stress and strain created due to the lattice mismatch of the GaN and AlN layers. Structural parameters play a significant role in determining spontaneous polarization, which explains the differences in

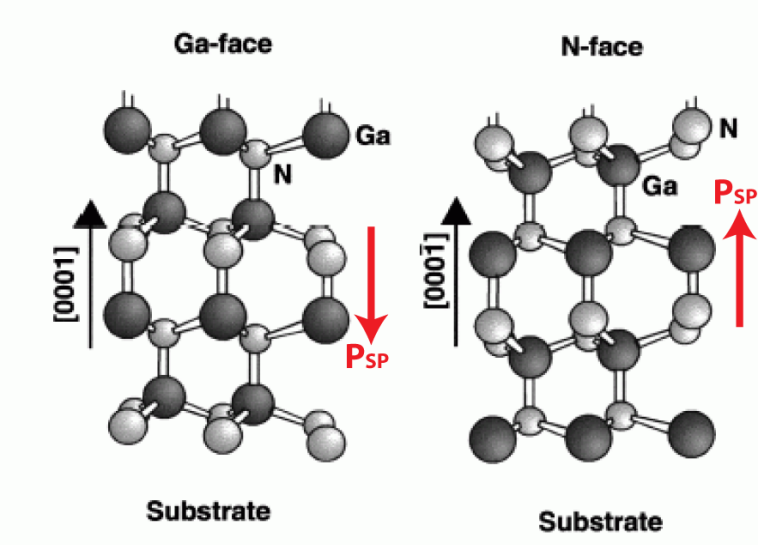



FIGURE 2.2: Atomic arrangement in Ga-face and N-face GaN crystals. Spontaneous polarization vector is also shown.

polarization of GaN and AlN [55]. The increasing non-ideality of the crystal structure from GaN to AlN increases the spontaneous polarization.

A standard AlGaN/GaN epitaxial film is grown along the [0001] axis as described in Section 2.1.1 and hence polarizations along that axis are the only ones considered. The spontaneous polarization along the c-axis is given by $\mathbf{P}_{SP} = P_{sp}.\hat{z}$, whereas the piezoelectric polarization is given by the piezoelectric coefficients $e_{33}$ and $e_{31}$ as:

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) \tag{2.1}$$

and $\varepsilon_z = (c - c_0)/c_0$, which is the strain along the c-axis. The in-plane strain is assumed to be isotropic and is given by $\varepsilon_x = \varepsilon_y = (a - a_0)/a_0$, where $a_0$ and $c_0$ are the equilibrium values of the lattice parameters. The relationship of the lattice constants of the wurtzite GaN is given by Equation (2.2).

$$\frac{c - c_0}{c_0} = 2\frac{C_{13}}{C_{33}}\frac{a - a_0}{a_0} \tag{2.2}$$

where $C_{13}$ and $C_{33}$ are the elastic constants.
Combining Equations (2.1) and (2.2), the net polarization along the c-axis can be calculated as:

$$P_{PE} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33})\frac{C_{13}}{C_{33}} \tag{2.3}$$

Since $[e_{31} - e_{33}(C_{13}/C_{33})] < 0$ for AlGaN over the whole range of compositions, the piezoelectric polarization is negative for tensile and positive for compressive strain barriers

respectively [54].

The spontaneous polarization for Ga-face GaN and AlGaN are negative because the direction vector points towards the substrate as shown in Figure 2.3 [55]. Similarly for N-face materials, spontaneous polarization direction vector points away from the substrate. For both Ga-face and N-face materials, the piezoelectric and spontaneous polarizations are parallel in case of tensile strain and anti-parallel for compressively strained barrier layers which is also shown in Figure 2.3.

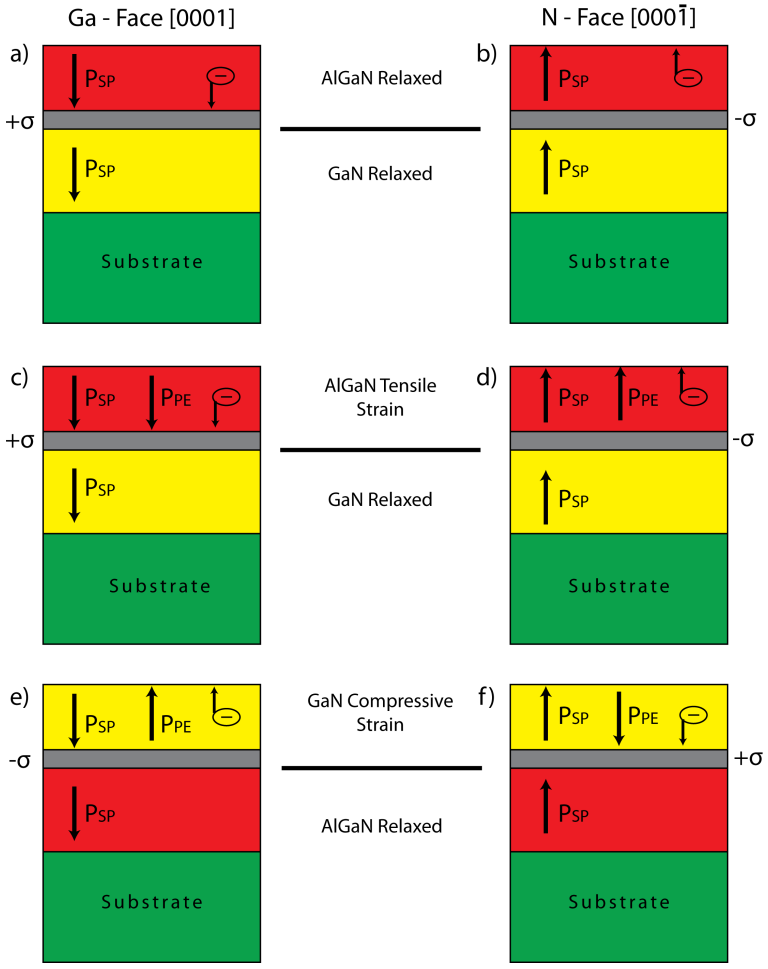



FIGURE 2.3: Directions of spontaneous and piezoelectric polarization in Ga and N-face AlGaN/GaN heterostructures.

The polarization induced charge density in space is given by:

$$\rho_p = \nabla.\mathbf{P} \tag{2.4}$$

The polarization sheet charge density($\sigma$) at an abrupt interface of an AlGaN/GaN or GaN/AlGaN heterostructure is given by [55, 56]:

$$\sigma = P(bottom) - P(top) \tag{2.5}$$

$$\begin{aligned} \sigma &= \{P_{SP}(bottom) + P_{PE}(bottom)\} - \{P_{SP}(top) + P_{PE}(top)\} \\ &= \{P_{PE}(bottom) - P_{PE}(top)\} + \{P_{SP}(bottom) - P_{SP}(top)\} \\ &= \sigma(P_{PE}) + \sigma(P_{SP}) \end{aligned} \tag{2.6}$$

However, if the polarization induced sheet charge density is positive ($+\sigma$), free electrons will try to compensate for the charges induced by polarization and vice versa. These charges will accumulate at the heterojunction of the barrier and the buffer layer to create a Two Dimensional Electron Gas (2DEG). In the case of Ga-face structures with AlGaN on top of GaN, the polarization induced sheet charge density is positive as shown in Figure 2.3a.

If the heterostructure is grown pseudomorphically, the piezoelectric polarization of the tensile strained AlGaN barrier layer will increase the difference between the AlGaN polarization and the GaN polarization and in turn increase the sheet charge density ($+\sigma$) and the electron confinement in the 2DEG. Alternatively for N-face AlGaN/GaN heterostructures, the spontaneous and piezoelectric polarizations have opposite directions (points away from the substrate) to Ga-face AlGaN/GaN structures (points towards the substrate) resulting in a negative polarization induced sheet charge density ($-\sigma$) as shown in Figure 2.3d and 2.3e. The negative sheet charge density assists to confine holes at the heterojunction, creating a "Two Dimensional Hole Gas" (2DHG).

In order to calculate the amount of the polarization induced sheet charge density ($\sigma$) at the AlGaN/GaN and GaN/AlGaN interfaces in dependence of the Al-content $x$ of the $Al_xGa_{1-x}N$ barrier, the following set of linear interpolations between the physical properties of GaN and AlN are used [55, 56]:

Lattice constant:

$$a(x) = (-0.077x + 3.189)10^{-10} \qquad \text{m}, \tag{2.7}$$

Elastic constants:

$$C_{13}(x) = (5x + 103) \quad \text{GPa}, \tag{2.8}$$

$$C_{33}(x) = (-32x + 405) \quad \text{GPa}, \tag{2.9}$$

Piezoelectric constants:

$$e_{31}(x) = (-0.11x - 0.49) \quad \text{C/m}^2, \tag{2.10}$$

$$e_{33}(x) = (0.73x + 0.73) \quad \text{C/m}^2, \tag{2.11}$$

Spontaneous polarization:

$$P_{SP}(x) = (-0.052x - 0.029) \quad \text{C/m}^2. \tag{2.12}$$

The total amount of polarization induced sheet charge density for an undoped $Al_xGa_{1-x}N/GaN$ heterostructure can then be calculated by using Equations 2.3, 2.6 and 2.12, which is given by Ambacher et al. [55, 56]:

$$|\sigma(x)| = |P_{PE}(Al_xGa_{1-x}N) + P_{SP}(Al_xGa_{1-x}N) - P_{SP}(GaN)| \tag{2.13}$$

$$|\sigma(x)| = \left|2\frac{a(0) - a(x)}{a(x)}\left\{e_{31}(x) - e_{33}(x)\frac{C_{13}(x)}{C_{33}(x)} + P_{SP}(x) - P_{SP}(0)\right\}\right| \tag{2.14}$$

The magnitude of the polarization induced sheet charge density ($\sigma$) for both Ga-face or N-face heterostructures is always the same but the sign changes. All of the devices used in this research employ Ga-face GaN.

#### 2.1.2.1 Simulation of 2DEG Sheet Density in GaN-Based HEMTs

Figure 2.4 shows the conduction energy band diagram of an AlGaN/GaN structure. The bandgap offset at the AlGaN/GaN interface, $\Delta E_c$, forms a quantum well in the GaN under the AlGaN barrier layer as shown in Figure 2.4. It is also shown in the diagram that the electrons in the 2DEG channel are provided by the unintentionally doped barrier layer. The electrons confined in a 2-dimensional conduction channel have high mobility and high electron density, which make HEMTs promising for high frequency and high power applications.

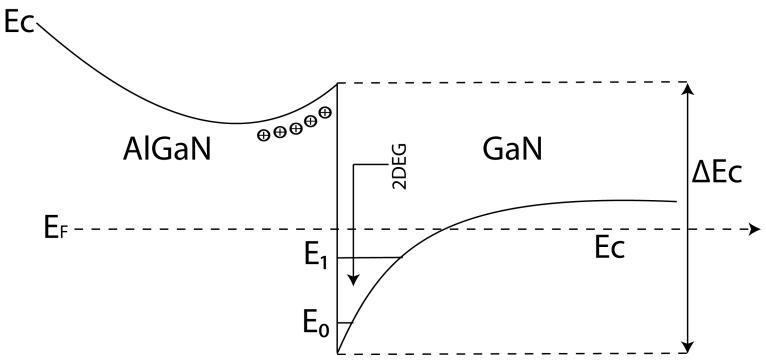



FIGURE 2.4: Conduction energy band of an AlGaN/GaN structure.

Since the total charge must be neutral, the free electrons accumulate in the quantum well to compensate the high positive polarization induced sheet charge at the AlGaN/GaN interface for Ga-face material. The electrons in the quantum well form a two dimensional electron gas (2DEG) channel. The density of the 2DEG is usually around $1 \times 10^{13}\,\mathrm{cm}^{-2}$ with mobility of around $2000\,\mathrm{cm}^2/\mathrm{V.s}$ at room temperature [30, 57]. The 2DEG sheet carrier concentration is given by [55, 56]:

$$n_s(x) = \frac{+\sigma(x)}{e} - \left(\frac{\epsilon_0 \epsilon(x)}{de^2}\right)[e\phi_b(x) + E_F(x) - \Delta E_c(x)] \tag{2.15}$$

where, d is the width of the $Al_xGa_{1-x}N$ barrier, $e\phi_b$ is the schottky-barrier of the gate contact, $E_F$ is the Fermi level with respect to the GaN conduction-band-edge energy, and $\Delta E_c$ is the conduction band offset at the AlGaN/GaN interface.

To determine the sheet carrier concentration from the polarization induced sheet charge from Equation 2.15, the following approximations were used [56]:

Dielectric constant:

$$\epsilon(x) = -0.3x + 10.4 \tag{2.16}$$

Schottky barrier:

$$e\phi_b = (1.3x + 0.84) \qquad \text{eV} \tag{2.17}$$

Fermi energy:

$$E_F = E_0(x) + \frac{\pi\hbar^2}{m^*(x)} n_s(x) \tag{2.18}$$

where the ground sub-band level of 2DEG is given by [56]:

$$E_0(x) = \left\{ \frac{9\pi\hbar e^2}{8\epsilon_0\sqrt{8m^{*(x)}}} \frac{n_s(x)}{\epsilon(x)} \right\}^{\frac{2}{3}} \tag{2.19}$$

with the effective electron mass, $m^*(x) \approx 0.22m_e$

Band offset:

$$\Delta E_C = 0.7[E_g(x) - E_g(0)] \tag{2.20}$$

where the band gap of $Al_xGa_{1-x}N$ is given by:

$$E_g(x) = xE_g(\text{AlN}) + (1-x)E_g(\text{GaN}) - x(1-x)1.0 \quad \text{eV}, \tag{2.21}$$

$$= x6.13 \ \text{eV} + (1-x)3.42 \ \text{eV} - x(1-x)1.0 \quad \text{eV} \tag{2.22}$$

From Equation (2.15), it can be seen that the sheet concentration is dependent on the percentage of aluminium (Al) composition in the $Al_xGa_{1-x}N$ barrier layer and/or the thickness of the barrier layer. To further understand how the 2DEG sheet carrier concentration can be controlled by the percentage of aluminium in the AlGaN alloy and the thickness of the AlGaN barrier, we used the Wolfram Mathematica 9 software to compute Equation (2.15), and generated an analytical model of the expected sheet charge concentration against the thickness of AlGaN barrier layer and the aluminium content in the $Al_xGa_{1-x}N$ alloy.

Figure 2.5 shows a graphical representation of the calculated sheet carrier concentration of the 2DEG sheet carrier density against different alloy compositions for various AlGaN barrier thickness. It can be seen from the graph that, if for example, a constant barrier thickness of 30 nm is considered, the sheet carrier concentration, $n_s$ will be approximately $0.85, 1.5, 2\times10^{13}\,cm^{-2}$ for alloy compositions of $x = 20\,\%, 30\,\%$ and $40\,\%$, respectively. If the thickness of an AlGaN barrier of alloy composition of $x = 25\,\%$ is increased from 10 nm over 20 nm to 30 nm, the sheet carrier concentration is increased from approximately 0.75 over 1.1 to $1.2 \times 10^{13}\,cm^{-2}$.

Figure 2.6 shows the variations of total polarization induced sheet charge carrier concentration of the 2DEG sheet carrier density when the AlGaN barrier thickness is varied for several alloy contents. From the graph, it can be seen that, for example, to achieve a sheet carrier concentration of $1 \times 10^{13}\,cm^{-2}$, only approximately $0.5\,\text{nm}, 2.2\,\text{nm}, 4\,\text{nm}, 7\,\text{nm}$, and 20 nm of AlGaN barrier thickness with alloy contents of $x = 100\,\%, 60\,\%, 45\,\%, 35\,\%$, and $25\,\%$, respectively, is required.

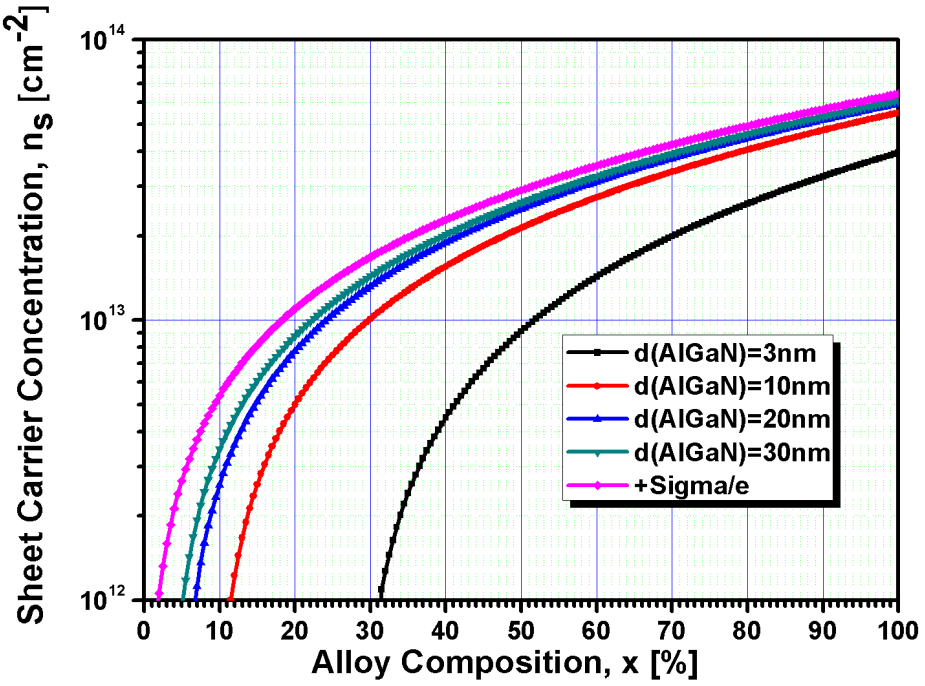



FIGURE 2.5: Total sheet carrier concentration of the 2DEG formed at the AlGaN/-GaN interface versus different alloy compositions for various AlGaN barrier layer thickness.

Conventional AlGaN/GaN devices employ approximately $20 - 25\,\%$ Al content in the AlGaN barrier of thickness of approximately 20 nm [5, 58, 59]. Due to the presence of 2DEG at the AlGaN/GaN interface to allow for conduction even when no gate voltage is applied, these AlGaN/GaN HEMTs are therefore depletion-mode devices. The graph in Figure 2.6 also shows that there is no 2DEG formation in the GaN channel below a certain AlGaN barrier layer thickness. For example, at a barrier thickness of less than approximately 6 nm for $x = 15\,\%$, 4 nm for $x = 25\,\%$, and 3 nm for $x = 35\,\%$, there is no presence of 2DEG in the GaN channel to allow for conduction. This barrier thickness at which there is very little or no electrons present to form a 2DEG channel is known as the "critical barrier thickness" of the barrier layer. Therefore, in order to realize enhancement-mode devices, it is crucial for the AlGaN barrier layer to be below the critical barrier thickness required for the formation of a 2DEG channel in the GaN channel. It will be demonstrated in subsequent chapters that this is indeed one of the main methods of achieving enhancement-mode operation.

The aluminium content in AlGaN barrier layers to date usually range between 15% to 40% for high quality HFETs. The reasons for this limitation are because, for barrier layers with $x < 15\,\%$, the conduction band offset becomes too small ($\Delta E_c < 0.28\,\text{eV}$),

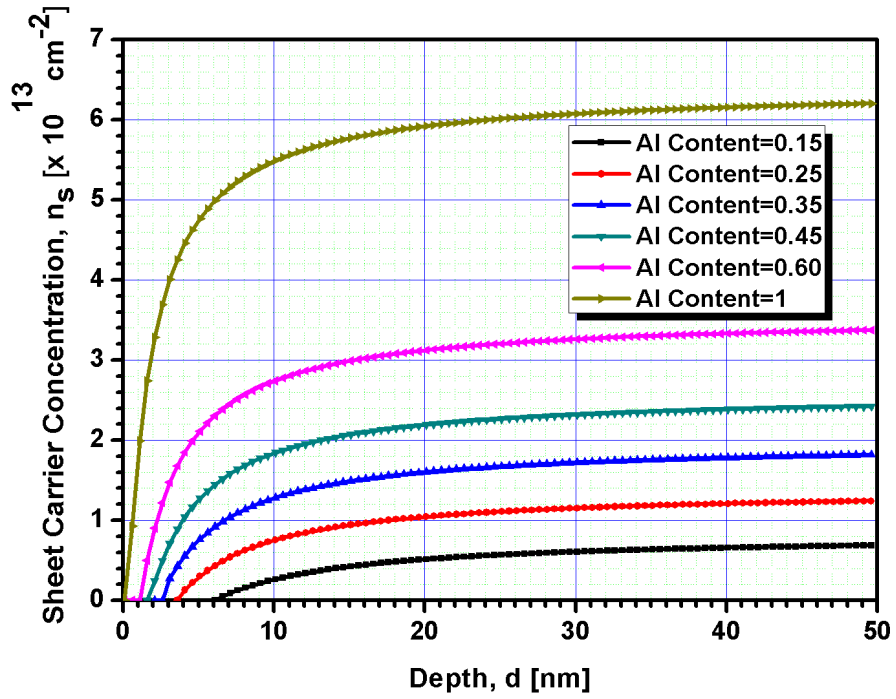



FIGURE 2.6: Variations of total polarization induced sheet carrier concentration of the 2DEG formed at the AlGaN/GaN interface versus various AlGaN barrier thickness for different alloy compositions.

resulting in bad confinement of the polarization induced electron sheet charge. For barrier layers with $x > 40\,\%$, the high lattice and thermal mismatch between the GaN buffer and the barrier layer cause a high density of structural defects in the AlGaN, and rough interfaces which limit the mobility of the 2DEG [55, 56, 60, 61]. All materials used in this project have an AlGaN barrier layer with an aluminium content of $x = 25\,\%$.

## 2.2 The AlGaN/GaN HEMT

### 2.2.1 Fundamentals of HEMTs

As already defined earlier, HEMT stands for High Electron Mobility Transistor. There are similar forms of this structure including HFET
(Heterostructure Field Effect Transistor), MODFET (Modulation-Doped Field Effect Transistor), MISHEMT (Metal Insulator High Electron Mobility Transistor) amongst others. The first generation of HEMT structure was constructed in a lattice-matched GaAs-based AlGaAs/GaAs system [62] which has been widely studied and used in RF, microwave and millimetre wave applications.

The fundamental characteristic of the HEMT structure is the conduction band offset between the materials which construct the barrier and channel layers. The barrier layer has a higher conduction band than the channel layer. Due to the large conduction band discontinuity, the electrons diffusing from the large bandgap AlGaN into the smaller bandgap GaN form a Two-Dimensional Electron Gas (2DEG) in the triangular quantum well at the interface which is the hallmark of a HEMT. In a HEMT, by placing a Schottky barrier gate on the barrier layer, the 2DEG sheet charge concentration can be controlled by applying an appropriate bias.

In 1993, Khan et al. demonstrated the first AlGaN/GaN MODFET (with n-doped barriers), with a transconductance of 23 mS/mm and 2DEG mobility of 563 $cm^2$/Vs at 300 K [63]. They also reported the first microwave results with current gain cut-off frequency ($f_T$) of 11 GHz and maximum frequency of oscillation ($f_{MAX}$) of 14 GHz [19]. In the early stages, the MODFETs exhibited very low transconductances and relatively poor frequency response. With improvements in the materials quality, however, the transconductance, current capacity and drain breakdown voltage were all increased to the point that GaN based MODFETs were used in the arena of high-power RF devices. One of the highest power density achieved for 0.45 × 125 $\mu$m GaN MODFET was 6.8 W/mm at 10 GHz and associated gain of 10.65 dB [64]. The operation temperature was pushed to 750 °C by using a thermally stable Pt/Au gate contact [65].

### 2.2.2 Operation of an AlGaN/GaN HEMT

An AlGaN/GaN HEMT is used to either process data or power (switch/amplifier) as a discrete device or part of an integrated circuit. Figure 2.7 illustrates the output characteristics of a depletion mode HEMT. It should be noted that this figure is for illustrative purposes only and will only be used to describe the operation of the device. The most common way to bias a HEMT is in the common source configuration as illustrated in the inset of Figure 2.7. The gate electrode is the input whilst the drain electrode is the output and the source is the common terminal. The gate's input signal acts as the control signal of the device and has the ability to switch the device on and off. Switching off a depletion mode device requires the application of a negative voltage to deplete the channel of electrons which will result in a highly resistive channel where no current will flow, this is known as "pinch-off". The expression which relates the number of carriers in the channel to the applied bias voltage is given by (modelling the 2DEG - metal gate as a capacitor) [66]:

$$n_s = \frac{\varepsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)}(V_{GS} - V_{TH}) \tag{2.23}$$

where, $n_s$ is the charge density per unit area of the 2DEG, $d_{AlGaN}$ is the thickness of the AlGaN barrier layer, $\Delta d$ is the effective distance of the 2DEG from the heterointerface, $V_{GS}$ is the gate bias voltage, and $V_{TH}$ is the threshold voltage

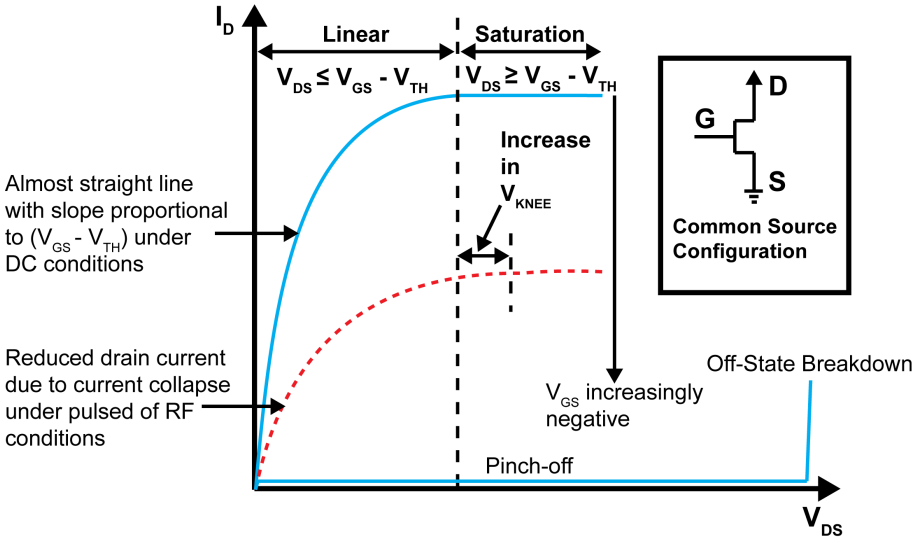



FIGURE 2.7: Typical IV characteristics of a HEMT. The inset shows a common source configuration for a transistor.

When $V_{GS} = V_{TH}$, the term $(V_{GS} - V_{TH})$ in Equation (2.23) will be equal to zero, resulting in $n_s$ being zero and the device shall be off. When $V_{GS} = 0\,V$, the channel will naturally be very densely populated with electrons and the application of a drain to source voltage will cause current flow between the source and drain of the HEMT.

For low drain voltages, i.e. $V_{DS} < V_{GS} - V_{TH}$, the device is said to be operating in the linear regime where the electron velocity in the channel is proportional to the applied electric field and so the current will increase with this field. The current flowing between the source and drain at this point is given by:

$$I_{DS} = qn_s v_{eff} W_G \tag{2.24}$$

where, $v_{eff}$ is the effective velocity of the electrons in the channel, and $W_G$ is the gate width

The velocity of electrons in the channel depends on their mobility and the electric field applied and is given by the relationship [67]:

$$v = \mu_n E \tag{2.25}$$

where, $\mu_n$ is the electron mobility, and $E$ is the applied electric field

The mobility of electrons in the 2DEG of an AlGaN/GaN HEMT is affected by carrier scattering through imperfections and dislocations in the semiconductor crystal and alloy disorder scattering [68]. According to Equation (2.25), the electron velocity increases with the applied electric field and so using this value in Equation (2.24), the current is shown to increase linearly for low fields when $V_{DS} < V_{GS} - V_{TH}$. Increasing the applied electric field so that the drain bias is $V_{DS} > V_{GS} - V_{TH}$, the velocity begins to saturate and becomes independent of the applied electric field. As the drain bias is increased such that $V_{DS} > V_{GS} - V_{TH}$, the lateral bias beneath the gate (due to drain bias) begins to pinch the channel off at the drain end of the gate. This continues until a point where the flow of electrons in the channel is constricted and limits the amount of electrons which can flow to the drain contact. At this point the device moves into what is known as the saturation regime and any further increase in the drain bias does not result in an increase of current. This region of device operation is analogous to a junction field-effect transistor (JFET) where the depletion region intrudes into the channel near the drain when the drain bias is increased. The drain current here can be expressed by:

$$I_{DS} = \frac{\varepsilon_{AlGaN} v_{sat} W_G}{(d_{AlGaN} + \Delta d)} (V_{GS} - V_{TH}) \tag{2.26}$$

where, $v_{sat}$ is the saturated electron velocity

An increase/decrease of the gate width $W_G$ would directly result in an increase/decrease of current since more/less electrons pass through a specific region at any given time.

### 2.2.3 GaN-Based HEMT Layer Structures

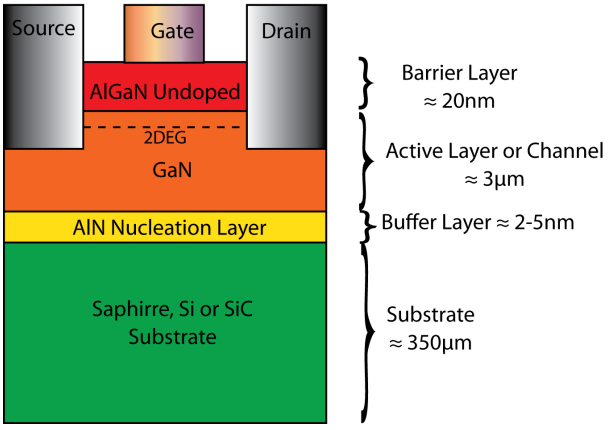



FIGURE 2.8: A basic AlGaN/GaN HEMT.

A basic AlGaN/GaN HEMT shown in Figure 2.8 consists of an AlGaN barrier layer usually around 20 nm thick grown on a GaN channel layer usually around 3 $\mu m$ thick. These device structures are usually grown on sapphire, semi-insulating silicon Carbide (SiC), or Si substrates.

The substrates generally have different lattice constants from the GaN layer (more details is given in Section 2.4), which means that there is a lattice mismatch between the GaN epilayers and the substrate [59, 69, 70]. This mismatch induces strain which results in dislocation or defect areas. Due to this, a thin neucleation layer of GaN or AlN is grown on top of the substrate, on top of which the channel and barrier layers are subsequently grown [5].

A device structure of the typical dimensions given here are of depletion-mode or normally-on mode, meaning this device requires a negative bias voltage in order to be turned off. The band diagram for this normally-on AlGaN/GaN device structure is shown in Figure 2.9.

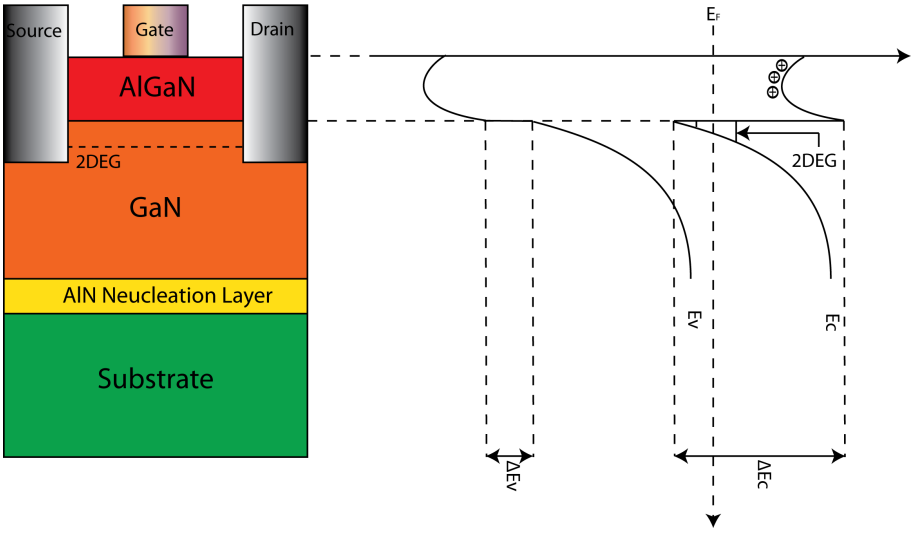



FIGURE 2.9: A basic AlGaN/GaN HEMT with corresponding energy band diagram.

## 2.3 Growth Techniques for Gallium-Based Binary and Ternary Compounds

The growth of good quality GaN based binary and ternary heterostructures is important for the production of high performance HEMT devices. Historically, hydride vapour phase epitaxy (HVPE) and its closely related technique, halide vapour phase epitaxy, have played an important role in the development of semiconductor material systems. The most popular and common procedures used to grow high quality GaN epitaxy are

Metal Organic Chemical Vapor Deposition (MOCVD) and Molecular Beam Epitaxy (MBE).

### 2.3.1 Hydride Vapour Phase Epitaxy

The first technique used to grow epitaxial GaN layers was the hydride vapour phase epitaxy (HVPE). This technique remained the most commonly used method until the early 1980s. During this technique, the gallium monochloride (GaCl) precursor is synthesized inside a reactor by the reaction of hydrochloric acid (HCl) with liquid gallium (Ga) at temperatures between 750 °C and 900 °C. Then the GaCl, which is transported to usually foreign substrates, e.g. sapphire, silicon, gallium arsenide, or silicon carbide, reacts with ammonia ($NH_3$) at 900 °C – 1100 °C to form a GaN film. Finally, the foreign substrate can be removed by techniques such as laser ablation. HVPE has a really high growth rate (typically 100 $\mu$m/hr), which has the potential to facilitate large area, thick and low defect density GaN quasi-substrates for subsequent growth by other epitaxial techniques such as MOCVD or MBE.

### 2.3.2 Metal Organic Chemical Vapour Deposition

Metal organic chemical vapour deposition (MOCVD) is a technique that involves a dynamic flow in which gaseous reactants pass over a heated substrate and react chemically to form a semiconductor layer. The metal organic compounds are transported by a carrier gas, $H_2$, to a heated substrate which reacts with Hydrides to form semiconductor films. The procedure involves the introduction of TriMethyl-Gallium (TMGa) and Ammonia gas simultaneously into the reaction chamber as shown in Equation (2.27) with a substrate heated to temperatures usually in the range of 800 °C ∼ 1000 °C [71].

$$(CH_3)Ga(g) + NH_3(g) = GaN(s) + 3CH_3H(g) \tag{2.27}$$

However, for the growth of ternary compounds like AlGaN, InGaN, etc., Trimethyl-Aluminium or Trimethyl-Indium simultaneously are generally reacted with Trimethyl-Gallium and Ammonia at elevated temperatures as shown in Equation (2.28).

$$x(CH_3)Al + (1-x)(CH_3)_3Ga + NH_3 \rightarrow Al_xGa_{1-x}N + ..... \tag{2.28}$$

MOCVD is currently used to grow high quality GaN epitaxial wafers for commercial purposes such as HEMTs, injection laser diodes and high brightness blue LEDs.

### 2.3.3 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) is one of the modern techniques used to grow single crystals. The main advantages of this technique is that it makes it possible to grow high quality layers, and it is easy to control the doping, concentration and thickness of the layer grown due to its slow deposition rate. In conventional solid-source MBE, ultra-pure elements like Aluminium, Gallium, Indium, etc. are heated in effusion cells to sublimate and allowed to condense on a substrate where the elements react with each other to form thin film layers. MBE growth chamber temperatures vary in the range between 600 °C and 900 °C. A computer controls the effusion cell shutters allowing precise control of the thickness of each layer [72, 73].

## 2.4 Substrate Choice for AlGaN/GaN HEMTs

The most important physical properties of the substrate materials under consideration for III-N devices include lattice-mismatch, thermal conductivity, coefficient of thermal expansion (CTE) and isolation. Table 2.2 presents an overview of the most important physical properties of the substrate materials under consideration for III-N devices.

### 2.4.1 Silicon Carbide Substrates (SiC)

Semi-insulating SiC is one of the most attractive substrate materials for electronic applications, due to favourable combination of lattice-mismatch, isolation, and thermal conductivity [69, 70, 74, 75]. It is available with increasing quality and diameters of up to 4 inch, although recently, both IQE and RFMD have both produced 6 inch GaN on SiC wafers [76–78]. Both polytypes 4H- and 6H-semi-insulating SiC are used. Most of the outstanding electronic device results have been reported on semi-insulating SiC materials, e.g. [79]. Currently, the greatest amount semi-insulating SiC material is produced by Cree [74]. There is a number of other vendors such as II-VI and Toyota. Despite the great advantages, SiC is a relatively expensive substrate on the market and as a result of this, cheaper alternatives are preferred.

### 2.4.2 Sapphire Substrates

Sapphire is a promising material due to the availability of cost-effective 2-4 inch diameter substrates. Recently, however, 6 and 8 inch substrates have been successfully produced by Rubicon Technology [80, 81]. NTT Advanced Technology Corporation have also recently grown 6 inch sapphire substrates [82]. It is widely used for electronic devices and despite the lattice-mismatch, it has displayed very impressive power densities of $\geqslant 12\,Wmm^{-1}$ and high pulsed output powers have been achieved [83, 84]. These substrates

TABLE 2.2: Basic properties of substrates and III-N semiconductor materials

| **Property** | **GaN** | **6H SiC** | **6H s.i. SiC** | **Sapphire** | **Silicon** | **AlN** |
|---|---|---|---|---|---|---|
| Lattice Constant ($\mathring{A}$) | 3.189 | 3.08 | 3.08 | $4.758/\sqrt{3}$ | 5.4301 | 3.112 |
| Mismatch to GaN (%) | 0 | 3.4 | 3.4 | 13 | 17 | 1 |
| Thermal Conductivity, $\kappa_L$ ($Wcm^{-1}K^{-1}$) | 1.3 | 4.9 | 3.7 | 0.5 | 1.5 | 2.0 |
| Isolation ($\Omega cm$) | $\geq 10^9$ | $\geq 10^{11}$ | $\geq 10^{11}$ | - | $1 - 3 \times 10^4$ | $\geq 10^{12}$ |
| Coefficient of Thermal Expansion, CTE ($10^6 K^{-1}$) | 5.9 | 4.2 | 4.2 | 7.5 | 3.59 | 4.2 |

have poor thermal conductivity but have been commonly used in device prototyping and also for GaN-based LEDs.

### 2.4.3 Silicon Substrates

Due its economic importance and widespread use, silicon is the most important semiconductor and substrate material; thereby making the use of silicon as a substrate desirable, mostly for cost efficiency reasons. Silicon wafers are available for large wafer diameters (from 8 inch up to 12 inch), whilst there is also a large pre-existing silicon-based infrastructure (foundries) for manufacturing silicon wafers [85]. The use of silicon however, introduces some critical issues and engineering challenges for III-N devices. Some difficulties of using silicon substrates include the difference in the thermal expansion coefficients between the substrate and the GaN semiconductor material, especially for high-power operation and the impact of the lattice mismatch relative to GaN with respect to material quality, defects and device reliability [86].

### 2.4.4 GaN and AlN Substrates

Native GaN and AlN substrates have been recently developed and used for electronic applications, although they are most important for optoelectronic applications. These substrates face increasing attention due to the expected improvement in electronic device reliability [87]. AlN is highly resistive and has a better thermal conductivity than GaN. Also, AlN compared to all other non-native substrates has the lowest lattice mismatch.

## 2.5 Metal-Semiconductor Contacts

Metal-semiconductor contacts are a vital part of a HEMT as they provide a mechanism of carrier transport to and from the semiconductor and metal contact of the device. There are generally two types of metal-semiconductors which are used in a HEMT. These are Schottky contact; which is mainly used as the gate electrode, and Ohmic contact; which is generally used as the source and drain electrodes. Both Ohmic and Schottky contacts are of critical importance with respect to device functionality, performance and long term reliability. This section gives a brief description of the two types of metal-semiconductor contacts used in an AlGaN/GaN HEMT.

### 2.5.1 Schottky Contact

The main transport mechanism in rectifying contacts is thermionic emission which allows electrons to move over the schottky barrier. For wide bandgap materials such as GaN, the barrier height is strongly influenced by the work function of the contact metal. For GaN based semiconductors, metals with high workfunctions are generally used to fabricate Schottky contacts [88, 89].

Table 2.3 shows various metals and their corresponding workfunctions. It can be seen from this table that Nickel, Platinum and Gold are the best metals for Schottky contacts because they have very high workfunctions compared to other metals on the list. However, Platinum suffers from adhesion problems when in contact with GaN and the presence of Gold at the semiconductor interface is responsible for creating high leakage current at the gate [90]. Additionally, it is known from experiments that the adhesion of Gold (Au) on GaN and on SiN isolation layers can be critical [91]. Based on that, Nickel (Ni) is one of the most widely used Schottky contact metals for GaN based semiconductors. The metal scheme generally used for gate electrode is Ni/Au 50/150 nm. The Au layer prevents the oxidation of the Ni layer.

In a HEMT, the gate contact is a Schottky contact. A voltage applied to the gate modulates the 2DEG carrier density at the AlGaN/GaN interface, and so modulates

TABLE 2.3: Various metals and their workfunctions

| Metal | Workfunction ($eV$) |
|---|---|
| Gallium (Ga) | 4.20 |
| Silver (Ag) | 4.26 |
| Aluminium (Al) | 4.28 |
| Titanium (Ti) | 4.33 |
| Silicon (Si) | 4.52 |
| Molybdenum (Mo) | 4.60 |
| Gold (Au) | 5.10 |
| Nickel (Ni) | 5.15 |
| Platinum (Pt) | 5.65 |

the drain to source current. For conventional HEMTs, the gate has a negative bias (is not forward biased).

### 2.5.2 Ohmic Contact

An Ohmic contact is defined as one in which there is unimpeded transfer of majority carriers from one material to another, i.e., the contacts do not limit the current. The contact resistance between the metal and semiconductor is dependent on the doping concentration of the semiconductor, engineering of the interface structures and unintentionally formed interface states. It is very important to form very low contact resistance, $R_c$, for Field-Effect Transistors (FETs) in order to achieve excellent DC and RF performances. It is generally very difficult to realize Ohmic contacts with very low $R_c$ in wide bandgap materials due to the low workfunction and hence small electron affinity of such materials; meaning that the barrier height ($\Phi_B$) of the metal/semiconductor is generally higher [92]. This is usually the case in $Al_xGa_{1-x}N$ (3.4 eV at $x = 0$ to 6.2eV at $x = 1$) especially as the value of $x$ is increased.

In general, there are two ways of overcoming the Ohmic contact issues on $Al_xGa_{1-x}N/GaN$:

1. Forming a low barrier height at the metal/semiconductor interface in order to allow the thermionic emission effect, and/or
2. Forming a very thin barrier at or near the bottom of the conduction band to allow thermally excited electrons to be tunnelled directly.

In order to realize high performance $Al_xGa_{1-x}N/GaN$ HEMTs, the Ohmic contacts must have very low resistance, excellent edge definition, smooth surface morphology,

as well as high mechanical and thermal stability. Most $Al_xGa_{1-x}N/GaN$ heterostructures use Ti/Al metallization based Ohmic contacts [93]. The most frequently reported schemes are the Ti/Al/Ni/Au, Ti/Al/Pt/Au and Ti/Al/Ti/Au metal schemes. Quite a number of researchers also tend to use Molybdenum (Mo) instead of Nickel (Ni), Platinum (Pt) or Titanium (Ti) as a diffusion layer because it can give low contact resistance of around 0.2 Ωmm with excellent edge acuity and improved surface morphology [94–97]. Each metal in the Ohmic contact stack has its own purpose [95]:

1. Titanium serves as an adhesion layer to provide good stability. It dissolves the native oxide on the AlGaN surface and creates nitrogen vacancies by reacting with nitrogen atoms to form TiN in the AlGaN layer, which in turn acts as n-type donor sites, increasing the doping concentration, and thus, enabling electrons to tunnel through the thinner metal/semiconductor barrier with very little/no resistance.

2. Aluminium reacts with Ti to form an $Al_3Ti$ layer which prevents the underlying Ti layer from oxidizing. It also serves as a diffusion barrier for the metals on top as they form schottky barriers.

3. Nickel, Platinum, Titanium, or Molybdenum then prevents the Al from mixing with the Au as the reaction of such a mix forms a highly resistive layer also known as 'purple plague'.

4. Gold is used as contact with the outside world due to its high conductivity.

The preferred transport mechanism in Ohmic contacts is known as field emission [98, 99]. During field emission, the carriers tunnel through the potential barrier. Field emission takes place when the depletion layer is sufficiently narrow as a result of high doping concentration in the semiconductor. It occurs when carriers do not have enough energy to cross the barrier thermionically, but are able to tunnel through the barrier allowing current flow from either the semiconductor to metal or vice versa and hence it is independent of the system temperature. More basics on metal semiconductor junctions are described in Appendix B for completeness.

### 2.5.3 Transfer Length Method Structures

Transfer Length Method (TLM), also known as Transmission Line Model [100–102], is used for assessing the quality and performance of Ohmic contacts. This technique was introduced by Reeves and Harrison and a detailed analysis is available in Ref. [100]. The two main methods of performing these measurements use either linear TLM structures or circular TLM structures.

### 2.5.3.1 Linear TLMs

Figure 2.10 shows a schematic diagram of a TLM pattern on a doped semiconductor material with Ohmic pads prepared for TLM analysis. In this case, metal pads, of finite width, w, and length, s, are deposited at linearly increasing pad spacing, L, such that $L_1 < L_2 < L_3$. The sample is then mesa-etched usually to the semi-insulating substrate. This is done in order to isolate columns of the conductive epitaxial layer, thereby restricting current flow within the mesa height, d.

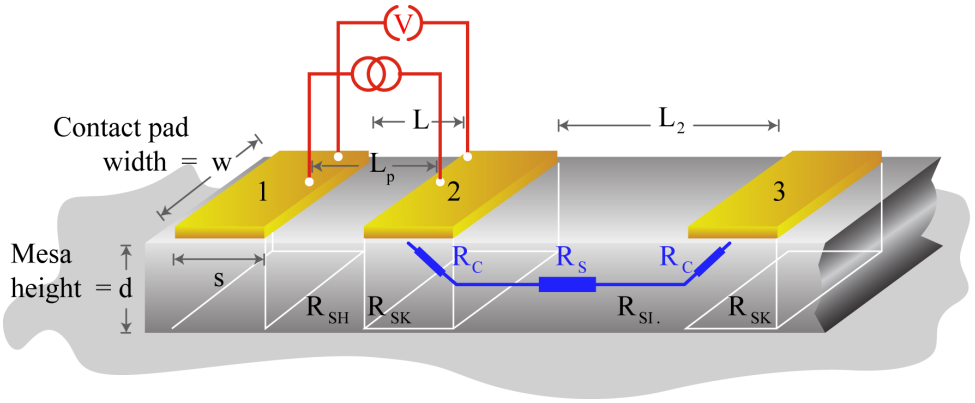



FIGURE 2.10: A semiconductor material with Ohmic contact pads for TLM characterization.

The most common method for characterizing TLMs is the four-point probe method as shown in Figure 2.10. This method is also suitable for measuring the resistivity of grown layers that are electrically isolated from the substrate. The four probes are equally separated by a distance, $L_p$. A constant current is passed between two adjacent probes; a second set of probes is then used to measure the voltage drop using a voltmeter, enabling the total resistance between the pads to be obtained. A separate current source and voltmeter are preferred to single ohm meter because of the latter's relatively low impedance which may give rise to inaccuracies. The current flows from the measuring probes through the metal contact, across the metal-semiconductor region, through the semiconductor transmission line ($L_1, L_2$, etc.) and into the second probe through the second metal-semiconductor region and metal. The net resistance obtained is the sum of the two metal contacts and the sheet resistance of the semiconductor. Several such measurements are repeated and the total resistance is plotted against the pad spacing as illustrated in Figure 2.11. The resistance, $R_{TOTAL}$, between two adjacent pads, is given by:

$$R_{TOTAL} = 2R_c + R_s \tag{2.29}$$

where, $R_c$ is the resistance due to the contact, and $R_s$ is the resistance due to the semiconductor material

$R_s$ is given by:

$$R_s = \rho L/dW \tag{2.30}$$

where, $\rho$ is the resistivity of the semiconductor material, W is the width of the metal pads, L is the pad spacing ($L_1, L_2$, etc.), and d is the mesa height.

But, since the sheet resistance, $R_{sh}$, of the semiconductor is given by $\rho/d$, Equation (2.29) can be re-written as:

$$R_{TOTAL} = 2R_c + R_{sh}(L/W) \tag{2.31}$$

Equation (2.31) has a gradient of $R_{sh}/W$, and x and y axis intercepts at $L_x$ and $2R_c$ respectively. This is illustrated in Figure 2.11. Therefore, by using this procedure, both the metal-semiconductor contact resistance, $R_c$ and the sheet resistance of the semiconductor, $R_{sh}$ can be calculated [100].

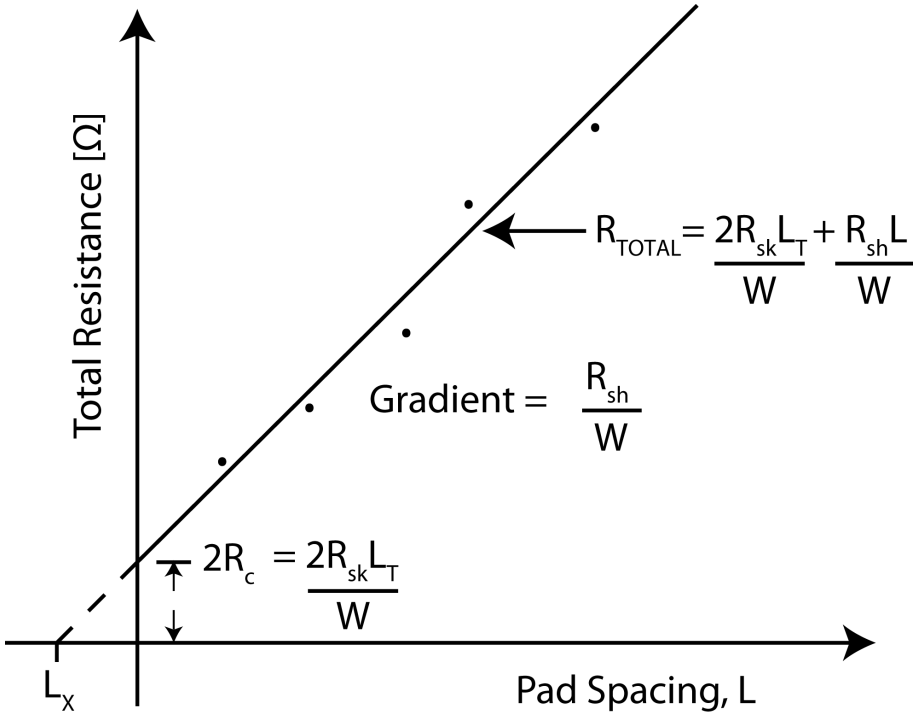



FIGURE 2.11: A graph showing an example of plot of total resistance as a function of pad spacing.

#### 2.5.3.2 Circular TLMs (CTLMs)

Circular TLM structures have been proposed to eliminate the drawbacks of linear TLM technique which tends to suffer from unwanted current flow patterns from contact edges unless mesa structures are fabricated [100, 103–106]. A typical CTLM layout is shown in Figure 2.12. Marlow and Das proposed this structure which consists of a circular contact, which is separated by a ring-shaped gap [106]. This structure is easier to fabricate and requires only one level of photolithography and does not require mesa-isolation.

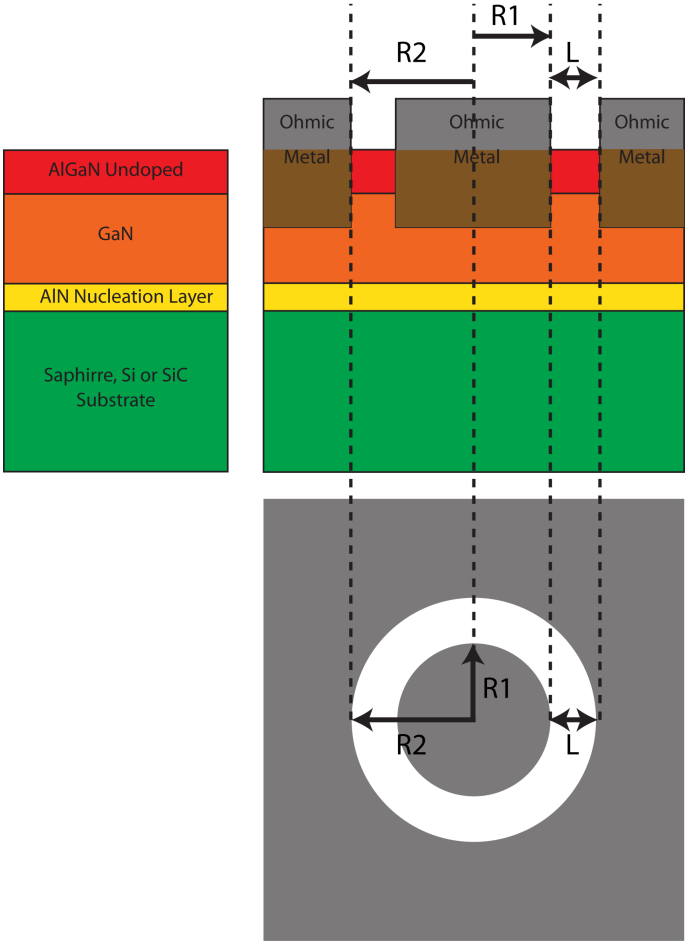



FIGURE 2.12: A cross-section and top view of AlGaN/GaN semiconductor material with Ohmic contact pads for CTLM characterization.

The CTLM structures are characterized in the same way as linear TLMs. The measured resistance changes with varying gap spacing. The total resistance, ($R_{TOTAL}$) between the contacts for the circular configuration [107], assuming $R_1 >> L$ and $R_2 = R_1 + L$, follows the equation:

$$R_{TOTAL} = \frac{R_{sh}}{2\pi}\left[ln\frac{R_2}{R_2 - L} + L_T\left(\frac{1}{R_2 - L} + \frac{1}{R_2}\right)\right] \tag{2.32}$$

where, $R_{sh}$ is the sheet resistance of the semiconductor material, ln is the natural logarithm ($\log_e$), $R_1$ is the radius of the inner contact, $R_2$ is the inner radius of the outer contact, L is the gap spacing, and $L_T$ is the transfer length, which is the length of the contact pad required for the current to flow into or out of the contact

The "ln" or "$\log_e$" term in Equation (2.32) can be evaluated using a Taylor expansion and so Equation (2.32) can be rewritten as shown in Equation (2.33). This relation can be modified into linear approximation by using correction factor c, that accounts for the circular geometry as shown in Equation (2.34) [108].

$$R_{TOTAL} = \frac{R_{sh}}{2\pi(R_1)} [L + 2L_T] \, c \tag{2.33}$$

$$c = \frac{R_1}{L} ln \left[ \frac{R_1 + L}{R_1} \right] \tag{2.34}$$

where, c is the correction factor

Factors that cause errors in the measurement of contact resistance include the effect of the size of the contact areas and the distance between them, and the effect of a finite spreading resistance in the material on the contact metal [108]. The normalized contact resistance, ($R_{c-norm}$) is obtained by multiplying $R_c$ with the length of the contact through which the current enters or leaves the inner contact, which is:

$$R_{c-norm} = R_c W_c \quad [\Omega mm] \tag{2.35}$$

where, $W_c$ is the circumference of inner contact for CTLMs, and $W_c$ = W which is the pad width for linear TLMs.

## 2.6 Summary

This chapter provided a description of the GaN material system, with an overview of the material properties and its crystal structure. The formation of the 2DEG channel at the AlGaN/GaN interface was discussed and an analytical model of the dependence of its density on the thickness of AlGaN barrier layer or the aluminium content ($x$) in the AlGaN barrier was presented. The principle of operation of GaN-based HEMTs was described as well as the metal semiconductor contacts used on these devices.

# CHAPTER 3

# GaN DEVICE PROCESSING TECHNOLOGY

In this chapter, various etching techniques used during GaN-based device fabrication including both dry etch techniques and the two main lithography techniques, optical and electron beam lithography will be introduced. The three popular deposition techniques for dielectric films used to form the device gate dielectric or for device passivation will also be described. The techniques include plasma enhanced chemical vapour deposition (PECVD), inductively-coupled plasma chemical vapour deposition (ICP-CVD) and atomic layer deposition (ALD) .

## 3.1 Etching Techniques for GaN-Based Devices

Improvements in the performance of AlGaN/GaN heterostructure devices depend on the quality of epitaxial materials and the development of device processing technologies. In particular, effective etching techniques are very essential for defining mesas, recess etching (Ohmic and gate recessing) and dielectric etching. Group III-nitrides have high bond energies (8.9 eV/atom for GaN and 11.5 eV/atom for AlN) compared to conventional III-V semiconductors [109]. The wide bandgaps and high bond strengths of these materials make them essentially chemically inert and highly resistant to bases and acids at room temperature. Therefore, dry etching is the main technique for the processing of GaN-based devices and it will be described further in the following sections.

### 3.1.1 Dry Etching

Due to the chemical stability of group III-nitride semiconductors, the difficulty in etching such materials using wet etch makes dry etching the dominant technique for etching

AlGaN/GaN heterostructures, especially for mesa and recess etching. Amongst several techniques used for dry etching, reactive ion etching (RIE) and inductively-coupled-plasma reactive ion etching (ICP-RIE) have been widely studied and used to etch III-nitride materials and will be our main focus of attention in this section.

#### 3.1.1.1 Reactive Ion Etching

Reactive ion etching (RIE) utilizes both the chemical and physical components of an etch mechanism to achieve anisotropic profiles, fast etch rates and dimensional control. Figure 3.1 shows a schematic of a RIE system [110]. RIE plasmas are typically generated by applying RF power of around 13.56 MHz between two parallel electrodes in a reactive gas. The substrate is placed on the powered electrode, where a potential is applied and ion energies (typically a few hundred electron-volts) are defined as they cross the plasma sheath. RIE is operated at low pressures, ranging from a few millitorr up to 200 mTorr, which promotes anisotropic etching due to increased mean free paths and reduced collisional scattering of ions during acceleration in the sheath [111]. The Oxford Instruments RIE 80 Plus tool and $CHF_3$/Ar gases are used for RIE in the James Watt Nanofabrication Centre (JWNC) of the University of Glasgow. Further details on how dry etching was performed in the processing of devices on this project will be presented in Section 5.1.2.6.

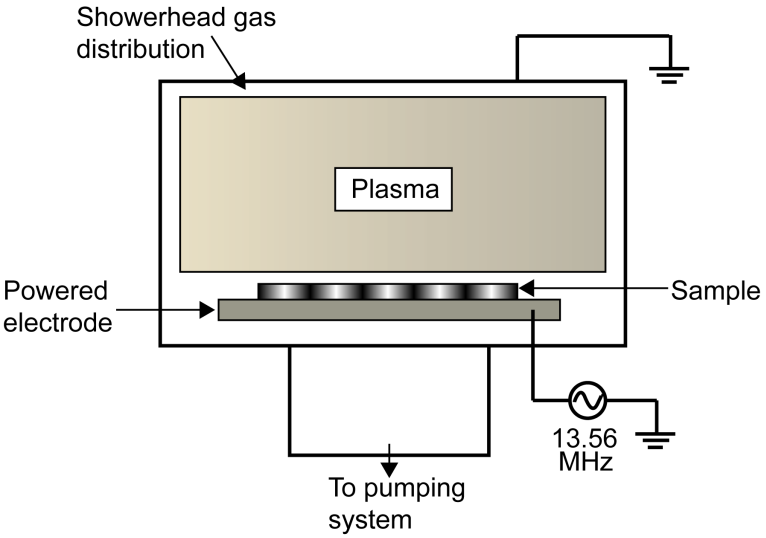



FIGURE 3.1: A schematic of a reactive ion etching (RIE) tool.

The chemistries for dry etching III-nitride semiconductors are mostly halogen-based with the most prevalent being chlorine-based. The etch rates reported for GaN using RIE with various etch chemistries range from 17 to 100 nm/min [112–115]. These etch rates were found to depend strongly on the plasma self-bias voltage, and essentially

independent of the chamber pressure for pressures less than 80 mTorr [114]. Higher etch rates were obtained at high plasma dc biases from -300 to -400 V. Conventional RIE uses both physical (dominant mechanism) and chemical components during etching and both these mechanisms cannot be independently controlled. This impacts the shape of etch profiles significantly especially in the case of III-nitrides where high ion energy is required to break the bonds between their forming atoms.

#### 3.1.1.2 Inductively-Coupled Plasma Reactive Ion Etching

The use of high-density plasma etch systems such as inductively-coupled plasma reactive ion etching (ICP-RIE), offers a high-density plasma etch platform to pattern Group III nitrides and has resulted in improved etch characteristics for GaN-based devices [111]. Figure 3.2 shows a schematic of an ICP-RIE system [110]. ICP plasmas are formed in a dielectric vessel encircled by an inductive coil into which RF power is applied. The alternating electric field between the coils induces a strong alternating magnetic field trapping electrons in the centre of the chamber and generating a high density plasma. Since ion energy and plasma density can be effectively decoupled, uniform density and energy distributions are transferred to the sample while keeping ion and electron energy low. Thus, ICP etching can produce low damage while maintaining fast etch rates. Anisotropy is achieved by superimposing an RF bias on the sample. In the JWNC, the Oxford Instruments PlasmaPro System 100 ICP180 RIE tool is available for performing ICP-RIE on devices.

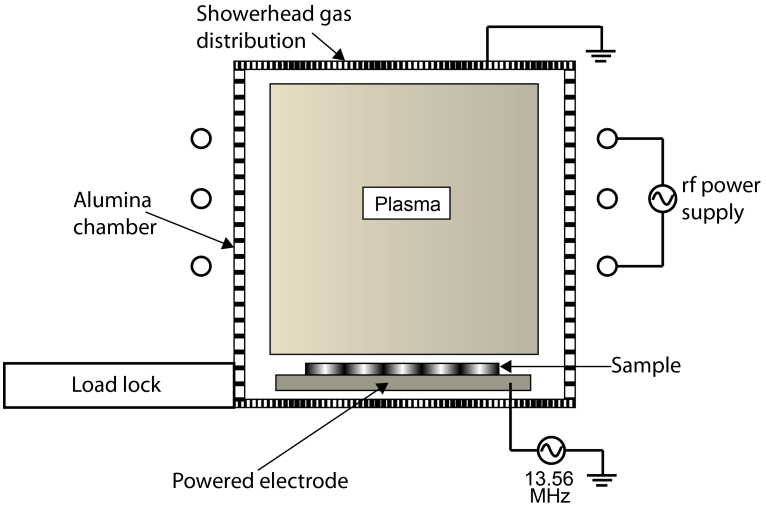



FIGURE 3.2: A schematic of an inductively-couple plasma reactive ion etching (ICP-RIE) tool.

ICP etching is generally believed to have several advantages including improved plasma uniformity over a wider area and higher etch rates. Higher plasma densities and larger ion

fluxes available in ICP-RIE tools lead to higher etch rates in these systems. Inductively-coupled-plasma etching (ICP-RIE) offers low damage etch compared to RIE. The higher efficiency of plasma generation during ICP-RIE method also means that plasma can be generated and sustained in a higher vacuum environment than possible for conventional RIE tools. Etch rates as high as 688 nm/min at DC bias of -280 V and 980 nm/min at -450 V have been reported for GaN using $Cl_2/H_2/Ar$ and $Cl_2/Ar$ plasmas, respectively [110, 111, 116]. An etch rate of 850 nm/min was also demonstrated using $BCl_3/Cl_2$ plasma at DC bias of -120 V and 30 mTorr pressure [117].

### 3.1.2 Wet Etching

The excellent chemical stability makes group III-nitride materials highly resistant to chemical etching. Only AlN has a known wet etch recipe [118–121]. As such, the processing of GaN devices is done with dry etching.

## 3.2 Lithography

The production of micro and nano-electronics has made incredible strides over the past 50 years. The main driver of lithography improvements is reduced device cost. This has come about through improvements in resolution, resulting in more chips per wafer, higher performance devices, and improvements in productivity, all of which continue to reduce the cost per function in integrated circuits. Lithography is an important and fundamental process used during semiconductor device fabrication to define very small features onto the material being used. This process involves the transfer of patterns from a mask plate unto a wafer surface which is covered with a thin layer of photoresist. Lithography can be performed by using either optical or electron beam (e-beam.) In this section, we will introduce a brief description of these two lithography methods.

### 3.2.1 Optical Lithography

Optical lithography, also known as photolithography creates a resist image of a mask on a wafer. The thin film of resist on the wafer is selectively removed or built up and the subsequent etching, lift-off, ion implantation or metallization is masked by the resist at the areas dictated by the lithography mask. Optical lithography is usually performed using a mask aligner. Figure 3.3 shows an illustration of the optical system of a mask aligner which is used to replicate a mask pattern during optical lithography.

Replicating the mask pattern with a mask aligner produces a resist image and the condenser collects ultra-violet (UV) light from the source and illuminates the mask pattern. The illuminated light then passes through the imaging lens to form an aerial image to

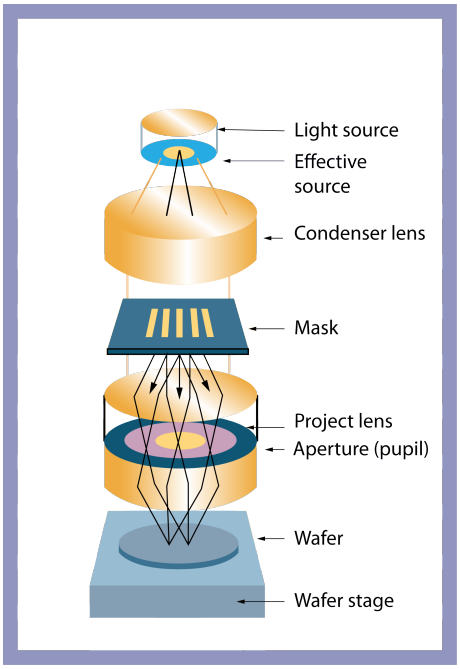



FIGURE 3.3: The optical system of a mask aligner used to replicate a mask pattern during optical lithography.

selectively expose the resist. The substrate can then be isotropically or anisotropically etched, lifted-off, plated, metallized, or implanted using the patterned resist as the mask. Photoresist is a radiation-sensitive compound. There are two types of photoresists used for optical lithography, these are positive and negative photoresist. Figure 3.4 illustrates the outcome of a positive and negative resist once a mask pattern is exposed onto a resist coated wafer and the pattern is etched after resist development of the mask pattern. The photoresists are classified according to their reaction to UV light or radiation. For positive photoresist, the exposed regions become more soluble in developer solutions and can be easily removed through resist development process, which then results in the mask pattern being replicated on the resist coated wafer. On the other hand, the exposed areas in a negative photoresist become less soluble in developer solutions and remain unexposed during resist development, which results in patterns opposite to those on the mask being defined on the wafer.

Optical lithography is, however, limited in resolution to around 1 $\mu$m due to the wavelength of the lamp source used. An ultra-violet (UV) lamp with a wavelength of 365 nm is used in the JWNC.

### 3.2.2 Electron Beam Lithography

Electron beam lithography (EBL) is primarily used for mask plate production. However, due to sub-micron or deep sub-micron patterning requirements, the technique can be

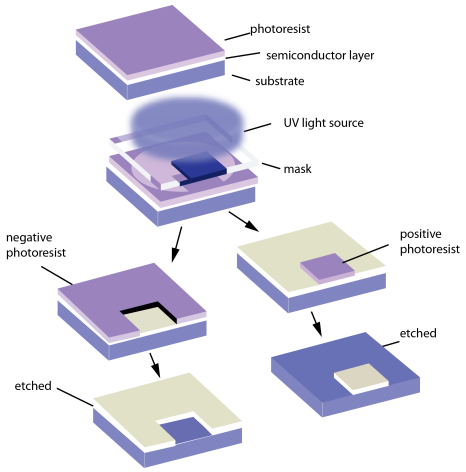



FIGURE 3.4: An image of a negative photoresist (left) and positive photoresist (right) after exposure, development and etch.

used to write patterns directly onto a resist coated wafer surface by a focused electron beam without a mask plate. The resists used for electron beam (e-beam) lithography are polymers. The behaviour of an e-beam resist is similar to photoresist, that is, a chemical or physical change is induced in the e-beam resist by radiation, which allows the resist to be patterned. For positive electron resist, the polymer interacts with electrons, causing chemical bonds to be broken to form shorter molecular fragments which are more easily dissolved by the developer solution during the development process. On the other hand, for a negative electron resist, irradiation causes radiation-induced polymer linking which creates a complex three-dimensional structure and makes the irradiated resist more difficult to be dissolved during the development process.

Some advantages of using EBL include:

- patterning of sub-micron and deep sub-micron features
- highly automated and precisely controlled operation
- positioning/alignment accuracy
- direct patterning on a semiconductor wafer without using a mask plate
- can be easily accesible for corrections since the layout design for EBL are stored and used electronically in the machine tool system

Despite the several advantages of EBL, there are a few drawbacks of using this lithography technique including low throughput, high cost of operation, and complicated and time consuming processing.

## 3.3 Dielectric Deposition Techniques

In semiconductor materials, and in particular GaN-based device processing, insulating thin (dielectric) films can serve three essential purposes. They can be:

1. used as a protecting layer (also known as passivation layer) at the end of device fabrication so as to protect the device from harsh ambience and to ensure reliable device operation over time,
2. a part of the active device (for example, gate dielectric of an AlGaN/GaN HEMT), and
3. used as hard masks to protect against diffusion during ion implantation, etching or annealing.

For these applications, high quality dielectric films deposited at low temperatures that are stable and of low hydrogen content are required. The most commonly used dielectric materials in III-V and in particular GaN-based device technology are silicon dioxide ($SiO_2$) and silicon nitride ($Si_3N_4$), although other dielectrics such as alumina ($Al_2O_3$), hafnia ($HfO_2$) and zirconia ($ZrO_2$) are gaining ground in popularity due to their higher dielectric constants of approximately 10, 25, and 22, respectively [122, 123]. The most common techniques for depositing dielectric films on GaN-based devices are plasma enhanced chemical vapour deposition (PECVD), inductively-coupled plasma chemical vapour deposition (ICP-CVD) and atomic layer deposition (ALD). In this section, we will give a brief overview of how the dielectrics are deposited using these techniques.

### 3.3.1 Plasma Enhanced Chemical Vapour Deposition

Plasma enhanced chemical vapour deposition (PECVD) is the conventional technique for depositing $SiO_2$ and $SiN_x$ dielectric films. Figure 3.5 shows a schematic of a typical PECVD tool from Oxford Instruments [124]. This figure illustrates the wafer, parallel electrodes, RF generator, plasma gas, reactive gas and the chamber of the PECVD system. The presence of a gas plasma allows reactions (which would otherwise only occur at high temperatures) to take place at a comparatively low temperature. Plasma is a partially ionized gas with free electron content (about 50 %). Plasmas are divided into two groups; thermal and cold (also known as non-thermal). In thermal plasmas, both electrons and gas particles are at the same temperature; however, in cold plasmas, the electrons have a much higher temperature than the neutral particles and ions. This feature allows PECVD systems to operate at low temperatures of between 100 °C and 400 °C. PECVD tools must contain two electrodes (in parallel), plasma gas, and reactive

gas in a chamber. In order to excite and sustain the excitement state of the plasma, a voltage must be applied to the plasma by using an RF signal between two electrodes.

The PECVD process begins with placing a wafer on the bottom electrode and the reactive gas with the deposition elements is introduced into the chamber. Deposition is then achieved by introducing reactant gases between the parallel electrodes (grounded electrode and RF-energized electrode). The capacitive coupling between the electrodes excites the reactant gases into a plasma, which induces a chemical reaction and results in the reaction product being deposited on the substrate. The substrate, which is placed on the grounded electrode, is typically heated to between 250 ° C and 350 ° C, depending on the specific film requirements.

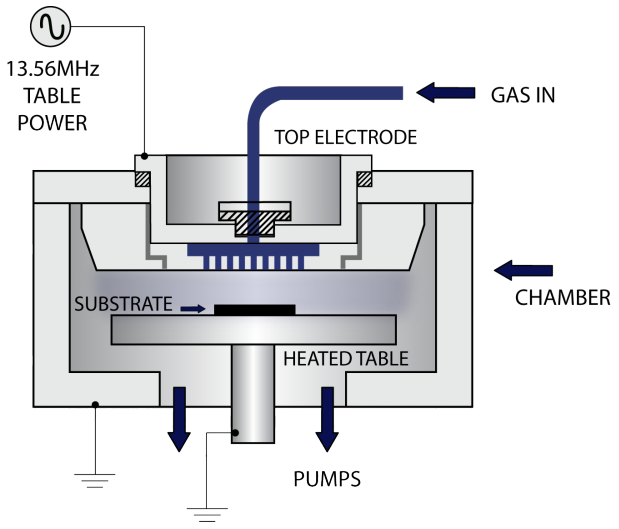



FIGURE 3.5: A schematic of a plasma enhanced chemical vapour deposition (PECVD) tool.

Using PECVD to deposit dielectric films has many advantages including low operation temperature, lower chances of cracking of the deposited layer, good dielectric properties of deposited layer including good stoichiometry (consistence) and good adhesion, good step coverage (the step coverage is the ratio of film thickness along the walls of a step to the thickness of film at the bottom of the step), good control of deposition thickness of dielectric (deposition rates of 30 nm/min to 70 nm/min), good uniformity, and less temperature dependent. However, low temperature films prepared by this technique can contain significant amounts of hydrogen. Generally, hydrogen content in a dielectric film is undesirable for microelectronics applications as it reduces the insulating behaviour of a gate insulator due to the formation of defects by the presence of hydrogen. Another important reason for this undesirable property is that at high temperatures hydrogen induces large stress and imperfections within the dielectric film [125, 126]. Hydrogen incorporation is inevitable in dielectrics deposited by PECVD as the films are typically

prepared from hydride source gases such as silane ($SiH_4$) and ammonia ($NH_3$). Also plasma damage during PECVD can result in physical and electronic degradation of the III-V devices.

### 3.3.2 Inductively-Coupled Plasma Chemical Vapour Deposition

During this technique, dielectric films are deposited by plasma enhanced chemical vapour deposition using an inductively coupled plasma (ICP) as the source. Conventional PECVD systems use high substrate temperatures of greater than 200 °C to achieve a dense film, however, using the high plasma density of the ICP source makes it possible to achieve film densities similar to PECVD at temperatures as low as 20 °C. Figure 3.6 shows a schematic of an ICP-CVD system from Oxford Instruments [127]. The dopant gases are fed through the gas distribution ring located just above the wafer. This minimises the deposition in the source area and reduces the need for cleaning the system. Inert gases are then fed into the chamber via the top of the ICP source. For $SiO_2$ dielectric, the inert (source) gas is usually $O_2$ and the dopant gas is usually $SiH_4$, whilst for $Si_3N_4$ dielectric, the inert (source) gases is usually $N_2$ and Ar, and the dopant gas is usually $SiH_4$. A high conductance chamber and vacuum system enables the ability to flow these process gases at relatively high rate while maintaining the low process pressures of between 1 to 10 mTorr necessary to sustain the high-density plasma.

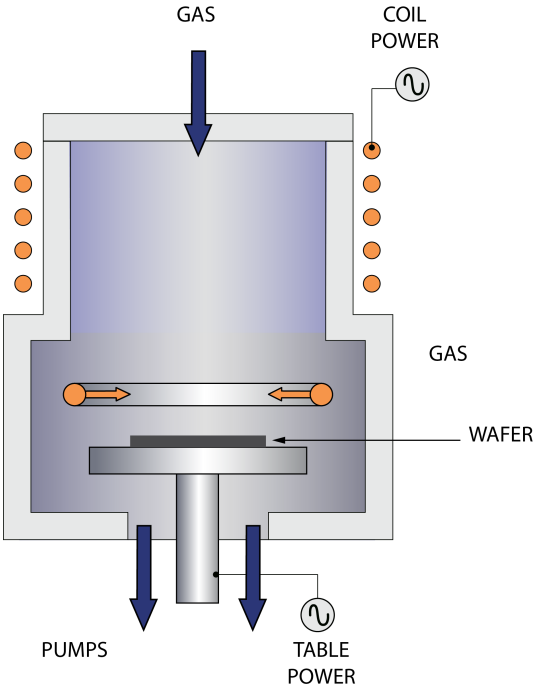



FIGURE 3.6: A schematic of an inductively-coupled plasma chemical vapour deposition (ICP-CVD tool).

Advantages of ICP-CVD include better control of deposited dielectric thickness than PECVD deposited dielectrics (deposition rate of 15 nm/min) and good step coverage. This deposition method also allows better control of the deposited film stress by modifying various parameters such as process pressure, temperature, RF power, and process gases ratio. Furthermore, ICP-CVD allows deposition on temperature sensitive devices and provides better uniformity of deposited film thickness than PECVD. At low pressures, a high dielectric film quality can be maintained in the ICP-CVD process, giving a very high film quality. However, ICP-CVD equipments are more expensive than PECVD ones.

### 3.3.3 Atomic Layer Deposition

Atomic layer deposition (ALD) is a vapour phase technique capable of producing thin films of a variety of materials including hafnia and zirconia. Based on sequential, self-limiting reactions, ALD offers exceptional conformality on high-aspect ratio structures, thickness control at the nanometre level, and tunable film composition [128]. With these advantages, ALD has emerged as a powerful tool for many industrial and research applications. Figure 3.7 shows a schematic of an ALD tool [129]. During ALD, separate precursor gases for a target material are sequentially dosed into a vacuum chamber under computer control. The first precursor is chemisorbed into the substrate surface and the chamber is then purged. The second precursor is then introduced and reacts with the first, yielding a monolayer of film. The cycle then continues by reintroducing the first precursor, and so on [130].

Dielectric films deposited by ALD offer many benefits in semiconductor engineering. Some advantages are that, as the ALD process deposits precisely one atomic layer in each cycle, complete control over the deposition process is obtained at the nanometre scale. Another advantage of ALD is that conformal coating can be achieved even in high aspect ratio and complex structures, whilst pin-hole and particle free deposition can also be achieved. However, ALD is a very time consuming technique which makes depositing thicker layers of film difficult (average deposition rates of around 100 nm to 300 nm/hr). The complicated processes involved during ALD also presents another drawback of this deposition method.

## 3.4 Summary

This chapter reviewed the various etching techniques used during GaN-based device fabrication. The two main lithography techniques used, optical and electron beam lithography were also described. The last section of this chapter then briefly discussed the

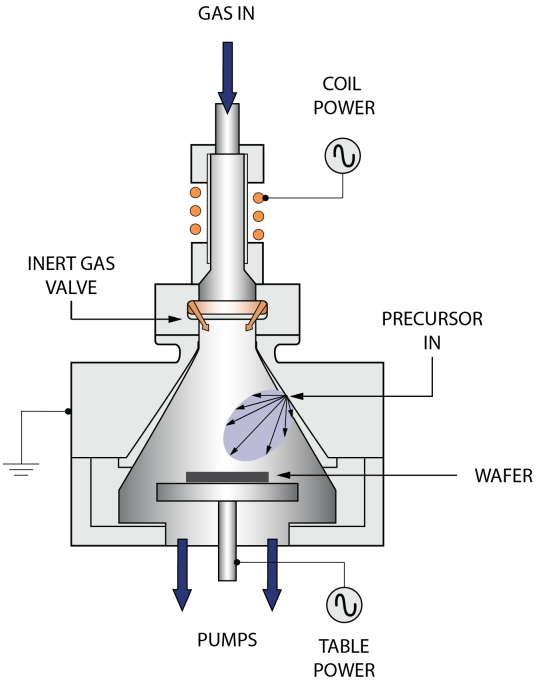



FIGURE 3.7: A schematic of an atomic layer deposition (ALD) tool.

three deposition techniques for dielectric films. In the next chapter, a review of some of the current techniques used to realise GaN-based normally-off high electron mobility transistors (HEMTs) will be given.

# CHAPTER 4

# REVIEW OF GaN-BASED E-MODE HEMTs

Owing to their high breakdown voltages and low on-resistances, GaN based enhancement -mode (E-mode) HEMTs are a major attraction for various electronic applications and in particular power switching applications due to the added safety of a normally off device. There have been several techniques used to fabricate E-mode devices to date, all incorporating different technologies to achieve the thin barrier layer or empty the 2DEG channel underneath the device gate (at zero gate bias) necessary for a normally-off operation. Some of the key challenges of using AlGaN/GaN heterostructure for making normally-off electronic devices are listed below:

- The strong polarization effect in the conventional AlGaN/GaN heterostructure leads to more negative threshold voltages [59], demanding a large positive shift in the threshold voltage ($V_{th}$) for the device to be converted to an enhancement-mode (E-mode) one during the device processing stage.
- Due to the strong chemical inertness of GaN, wet etching techniques which are generally used in gate recessed InP and GaAs-based E-mode HEMTs have proved very difficult in AlGaN/GaN devices.

This chapter reviews some of the commonly used techniques to overcome the above challenges and realise GaN-based E-mode HEMTs.

## 4.1 Double Barrier HEMT with an Etch-Stop Layer

As the name suggests, the double-barrier technique employs two active barrier layers as shown in Figure 4.1. The device consists of a very thin AlGaN layer capped with an AlN

layer. The incorporated thin AlGaN layer is only used to control the threshold voltage of the device and hence the thickness is kept around the critical thickness of the layer for the specific Al-content. Therefore, the threshold voltage is set by epitaxy.

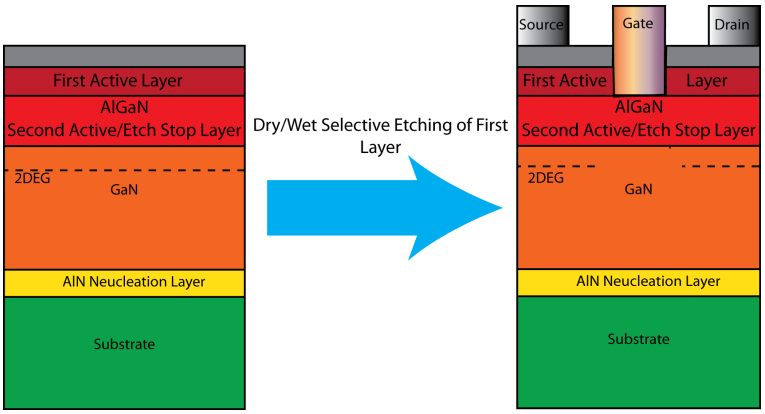



FIGURE 4.1: Double barrier AlGaN/GaN HEMT structure with etch-stop layer.

The polarization charge induced by the thin AlGaN layer is not sufficient to generate a high carrier concentration in the channel. Adding an AlN cap on top of the AlGaN layer induces a large polarization field because of the inherent spontaneous polarization as a result of the lattice mismatch and larger conduction band offset, thereby enhancing the carrier concentration in the channel. The top active layer can, however, be selectively dry/wet etched until the second active layer which acts as an etch-stop layer is reached [120, 131–133]. The addition of the etch-stop layer makes this technique reproducible, however, there is lack of variable options of the top active layer structure as only AlN is known to be selectively chemically etched using AZ400K developer solution at ($> 60\,^oC$) over other materials in the GaN family of semiconductors, limiting the device structure to only have AlN as the top active layer [119, 134]. Another disadvantage of using this technique is that, for dry recess etching, the etch-stop layer is limited to only Indium (In) related chemistries such as InN, InAlN or InGaN as they require very high table-temperature in order to etch [120, 132, 133].

## 4.2 Fluorine Ion Implantation

Another common technique for realising GaN-based e-mode HEMTs is the use of fluorine ion implantation. The fluorine ions can be implanted into the conventional $\approx 20\,\text{nm}$ thick AlGaN barrier layer as illustrated in Figure 4.2. The implantation of these negatively charged fluorine ions causes the channel of electrons underneath the gate-foot region to be depleted [37, 51, 135–138]. Although fluorine ion implantation eliminates the problems incurred during dry etching techniques, it is known to be very unreliable as the implanted fluorine ions have the tendency to move around in the GaN crystal lattice;

making the device very unstable, and thus, degrading the drain breakdown voltage of the device. Also, the threshold voltage $V_{th}$ is not uniform across a wafer of several devices fabricated using this method.

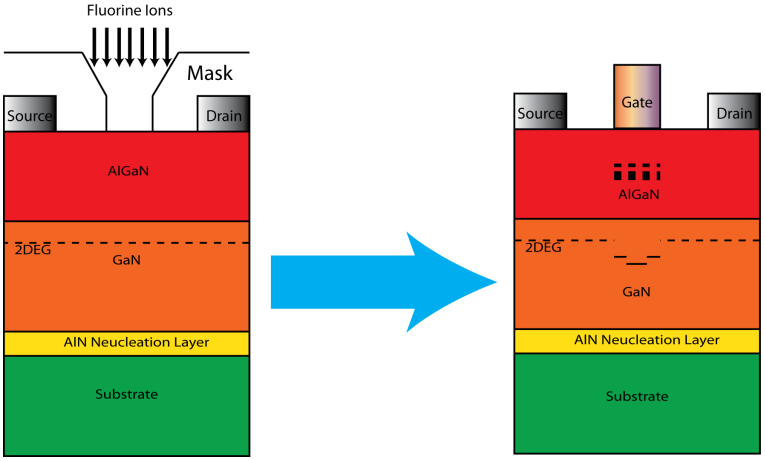



FIGURE 4.2: Achieving an e-mode GaN HEMT device using fluorine ion implantation.

## 4.3 P-N Junction Gate GaN HEMTs

In a technique pioneered by Panasonic, a standard AlGaN/GaN HEMT structure is capped with a p-type AlGaN or GaN layer to realise normally-off operation [139, 140]. This device structure is illustrated in Figure 4.3 and has a p-GaN cap layer of around 100 nm-120 nm thick [139, 140]. At zero gate bias, the electrons in the device channel underneath the gate are depleted due to the high built-in potential of the p-n junction. However, the application of forward bias gate voltage allows the injection of holes in the barrier layer, which in turn attracts free electrons to complete the 2DEG channel and so allows the flow of current if a drain-to-source voltage is applied.

This technique enables the fabrication of both depletion and enhancement mode HFETs on the same wafer, thus opening up the possibility of designing high-speed, low-consumption GaN-based logic integrated circuits. Despite this advantage of using the p-n junction gate device fabrication technique, growing high-quality and uniform p-type material in group III-Nitrides is still difficult. Also, p-GaN/AlGaN interface trap-related dispersion presents this technique with another drawback. Also, the threshold voltage achievable with this device is around +0.55 V and the forward bias voltage is limited to around +3 V.

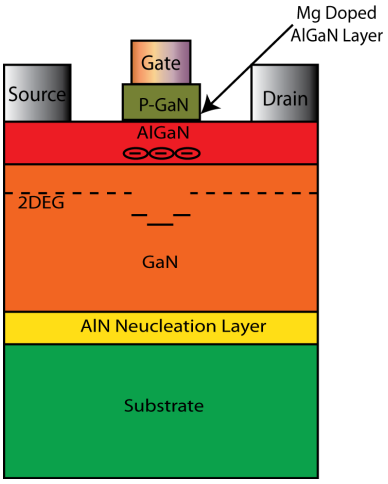



FIGURE 4.3: P-N junction gate e-mode GaN HEMT.

## 4.4 InGaN Cap Layer GaN HEMTs

The use of an InGaN cap layer was first proposed in 2007 by Mizutani et al. [141]. The key idea of this method is to employ the polarization-induced field in the InGaN cap layer as illustrated in Figure 4.4a, by which the conduction band is raised leading to a normally-off operation [141–143]. A thin layer of InGaN was grown on a conventional n-AlGaN/i-GaN HEMT structure. Even though the direction of spontaneous polarization is the same for all the layers in the device, the directions of piezoelectric polarization are opposite between the InGaN cap layer and the AlGaN barrier layer. The polarization-induced field in the InGaN cap layer causes the conduction band to raise leading to normally-off operation of the device as illustrated in Figure 4.5 [141, 143]. However, an application of a forward bias voltage causes the conduction band to lower below the Fermi level and hence there is a presence of 2DEG which allows conduction. In the case of HEMTs without the InGaN cap layer, 2DEG is formed in the AlGaN/GaN interface which leads to the normally-on operation as illustrated in the energy band diagram in Figure 4.5b. InGaN cap E-mode devices do however suffer from small threshold voltage, high sheet resistance, low transconductance and high contact resistance.

## 4.5 Tunnel-Junction GaN HEMTs

One of the most recent techniques proposed for realising e-mode GaN-based HEMTs is the use of a tunnel-junction in the devices. In this method of achieving enhancement mode GaN devices, the control of the source-to-drain current flow is realized through a gate controlled tunnel-junction instead of a gate controlled 2DEG channel. The device structure of a tunnel-junction e-mode GaN HEMT is shown in Figure 4.6. The operating

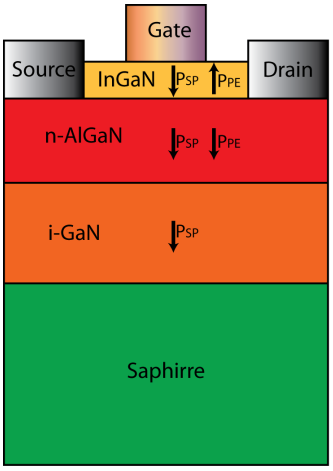



FIGURE 4.4: Schematic cross section diagram of an AlGaN/GaN HEMT with InGaN cap layer.

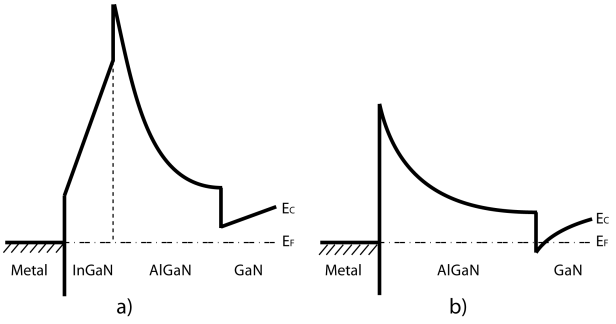



FIGURE 4.5: Energy band diagrams: a) with and b) without InGaN cap layer.

principle of the AlGaN/GaN tunnel-junction FET is that, at zero gate bias, the 2DEG channel is fully turned on. However, the effective Schottky barrier width at the source metal 2DEG junction (with a Schottky barrier height of 0.8 eV) is $\sim 10\,nm$. Such a potential barrier thickness yields a negligible tunnelling current and effectively blocks the current flow, keeping the device in the "OFF" state. As the gate bias becomes more positive, the conduction band of the GaN is pulled down, effectively reducing the schottky barrier width. At $V_{GS}$=3 V, the schottky barrier width is less than 1 nm, and the tunnelling current is significantly higher, turning the device "ON" [144, 145]. Realization of E-mode tunnel-junction devices however involves very complicated fabrication processes which reduces its reproducibility and repeatability. To our knowledge, the fabrication of these devices is neither reproducible nor repeatable [146].

## 4.6 N-Polar GaN HEMTs

In N-face AlGaN/GaN heterostructures, the spontaneous and piezoelectric polarizations have opposite directions in comparison to the Ga-face structure as shown in Figure 4.7a

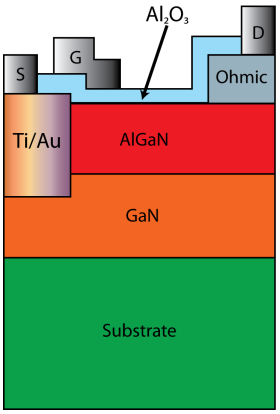



FIGURE 4.6: Cross section of a tunnel-junction AlGaN/GaN FET.

[147]. The polarization induced charge at the interface of this heterostructure is negative, and holes can be accumulated at this interface. However, electrons will be confined at the GaN/AlGaN interface if GaN is grown on top of the AlGaN due to the positive sheet charge which will be formed in this case. A thick enough AlGaN layer is then grown on top of the GaN layer in order to deplete any of the 2DEG induced at the bottom AlGaN/GaN interface [148–150]. In the drain, source and access regions, this top AlGaN is etched away, leading to a high electron density in these regions as shown in Figure 4.7 [147]. The 2DEG under the gate is then induced when the gate is forward biased, while the charge in the access region is always present. Although N-polar devices provide E-mode without gate recess etch and the $V_{th}$ of these devices are not affected by processing steps, these devices suffer from high leakage current and the growth of good quality N-polar GaN is very complex [151, 152].

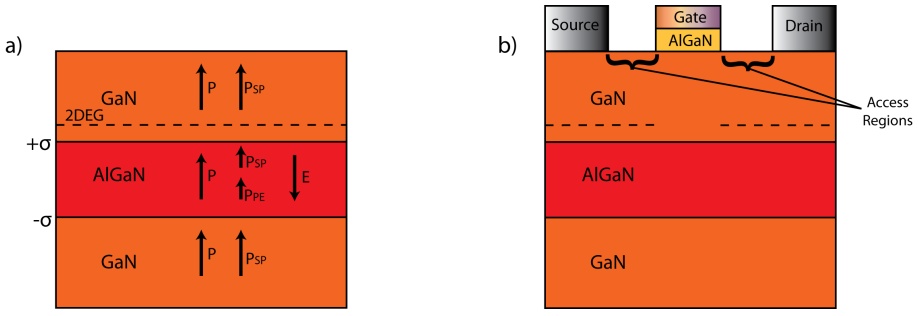



FIGURE 4.7: Cross section of N-Polar AlGaN/GaN HEMT: a) showing directions of polarization charges and b) with AlGaN Layer.

## 4.7 Gate Recessed GaN HEMTs

Gate recess technique is one of the most common methods of achieving an enhancement mode device and it is done by physically thinning the barrier by etching away the barrier

under the local gate-foot region as shown in Figure 4.8. Saito et al., 2006 realized a normally off AlGaN/GaN HEMT using recessed gate fabrication technique which exhibited a maximum drain current of 100 mA/mm, a threshold voltage of -0.14 V and a breakdown voltage of around 435 V [153]. As earlier explained, dry etching is the only effective and easiest method for GaN. However, as Reactive Ion Etching (RIE) using inductively coupled plasma etcher with $BCl_3$ or $SiCl_4/Cl_2$ involves physical etching, it damages the sample surfaces and it is also very difficult to control the etch rate, and thus over-etching becomes an issue [50, 84, 118, 153–158]. Over-etching due to dry etching makes achieving uniform threshold voltage and repeatability between devices fabricated on the same wafer (let alone between wafers) extremely difficult, therefore, gate recess etching is unattractive without an etch stop layer (and to date, no suitable such layer that can be incorporated in the conventional AlGaN/GaN HEMT structure has been identified).

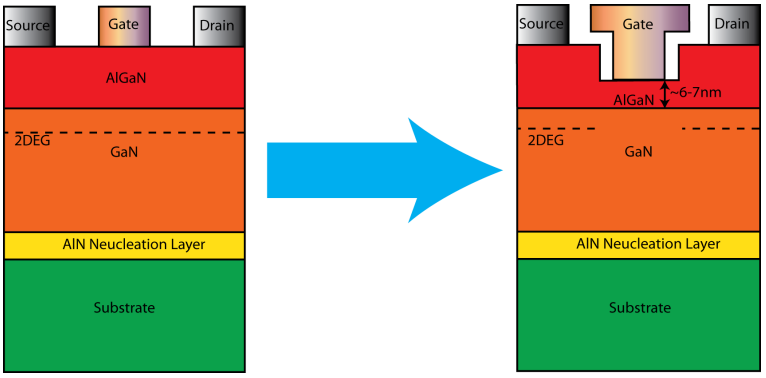



FIGURE 4.8: Gate recessed AlGaN/GaN HEMT structure.

## 4.8 Thin Barrier Devices

The use of a thin barrier to realise e-mode GaN-based devices has been proposed by several groups. Uniform device performance can be obtained through the use of the thin barrier, i.e. an AlGaN thickness of under $\sim 10$ nm because it requires no recessing [119, 159–162]. In this case, the channel can be easily depleted under the gate for normally-off operation due to the reduced 2DEG density, but the devices suffer from reduced drain currents and high On-resistances since the low density 2DEG is across the entire source-drain region. To reduce the access resistance between the gate-source and gate-drain regions, $SiO_2$ passivation layers have been used in these regions [160, 161]. In Reference [119] the use of an epitaxial AlN cap layer that was selectively etched from the gate region was also demonstrated. $V_{th}$ of these devices is around 0 V.

Recently, a thin 12 nm barrier normally-off AlGaN/GaN MOS-HEMT with an overlap gate structure, i.e. also no gate-source and no gate-drain separation, and using a thick

$HfO_2$ with a large dielectric constant as a gate insulator was proposed [163]. The device demonstrated a $V_{th}$ of +3 V and $I_{DSmax}$ of 730 mA/mm at $V_{GS}$ of 10 V. Normally-off operation was attributed to negative charge in the gate dielectric which depleted the 2DEG channel for $V_{GS} < V_{th}$. The main drawback for this approach was the reduced device breakdown voltage.

## 4.9 Summary

In this chapter, the current techniques being used to fabricate enhancement-mode GaN-based HEMTs were reviewed. Due to the drawbacks of current approaches, there is on-going research into realising normally-off GaN devices using a design that is easily repeatable and reproducible and one which does not require too many complicated fabrication steps. The next chapter will provide details of the actual fabrication processes used in realising GaN HEMTs (on this project).

# CHAPTER 5

# DEVICE FABRICATION PROCESSES

In this chapter, the fabrication processes used to realise normally-off GaN transistors will be described. Details of fabrication processes for single finger normally-off or enhancement-mode transistors will be given with focus on the mask design and layout of the transistors.

## 5.1 Device Layout and Process Flows

Prior to fabrication, devices must be designed using a computer aided design (CAD) software; in this case, the Tanner EDA's L-Edit, Version Win 32 14.13 layout editor was used [164]. Once the patterns are designed, the design file is sent to an electron beam lithography tool which writes the required design on a mask plate as described in Section 3.2.2. The quartz mask plate is chrome plated on one side on which patterns are created. The final mask plate is then used for every photolithography step as required throughout the fabrication process of the devices. Figure 5.1 shows an example of a complete transistor layout design in L-Edit. This design layout is 10 mm × 10 mm in size and includes a set of horizontal and vertical alignment markers, 2 circular TLM structures, 16 linear TLM structures, 24 metal-oxide-semiconductor (MOS) capacitors, and 182 transistors.

### 5.1.1 Device Structure

The epitaxial layer structure used for making the devices consists of (from top to bottom) an ultrathin sub-critical 3 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, a 3 $\mu$m GaN channel, a 2 to 5 nm AlN nucleation and transition layers grown on either a sapphire or silicon substrate.

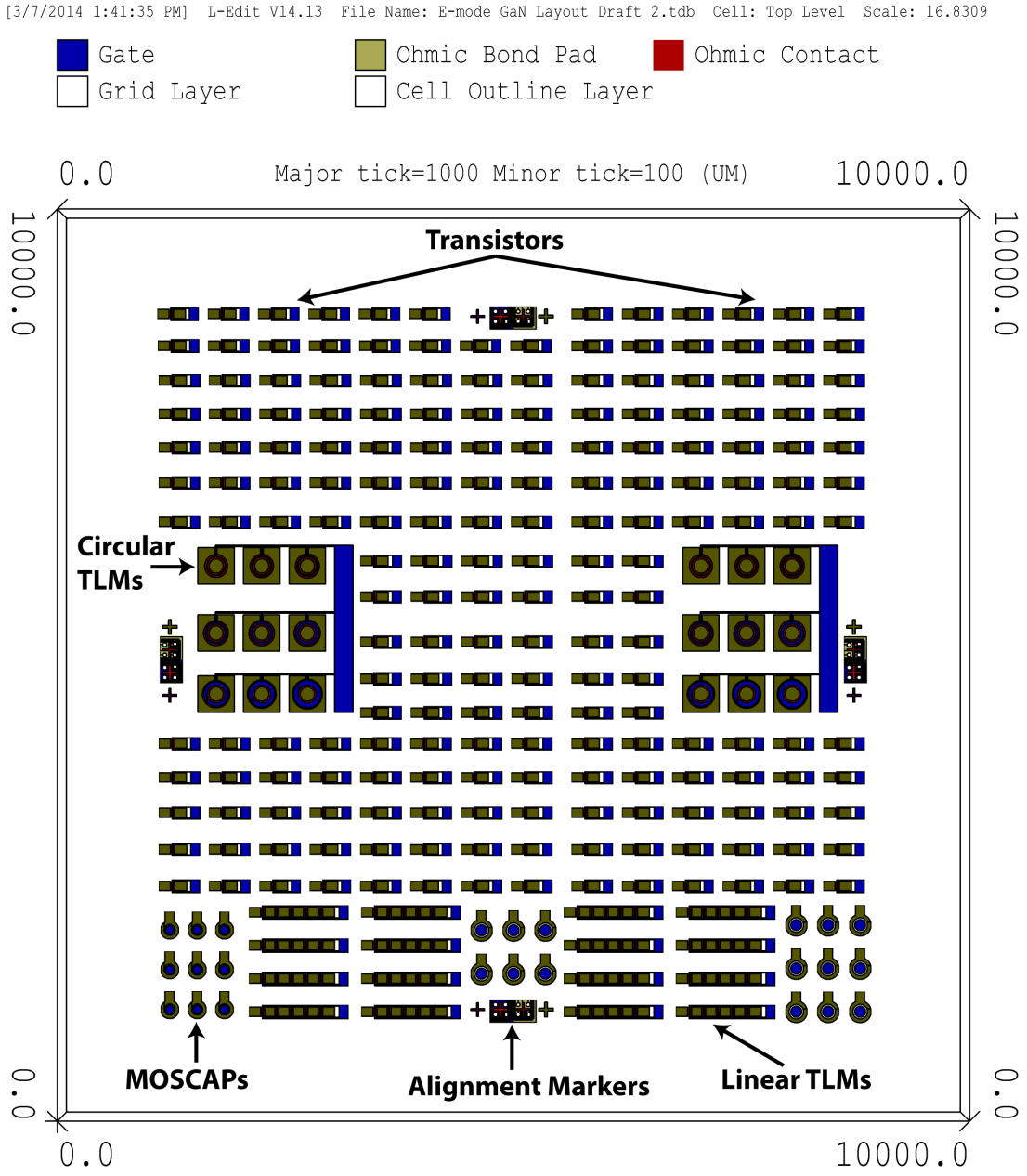



FIGURE 5.1: A screen shot of a complete device layout design in L-Edit including alignment markers, test structures and DC transistors.

Note the very thin AlGaN barrier layer of 3nm, which is crucial to the realisation of normally-off operation. Unlike conventional device structures which use approximately 20 nm thick AlGaN barrier layers, there is no inherent 2DEG channel at the AlGaN/GaN interface in this structure as the AlGaN barrier thickness is below that required for 2DEG formation (4 nm). This was discussed earlier in detail in Section 2.1.2.1 of Chapter 2.

The device layout consisted of a gate contact that nominally overlaps the source and drain contacts, with a dielectric in between the gate and the semiconductor (and the source/drain contacts). This layout is similar to that in Reference [163]. To demonstrate the device concept, only DC characterizations was required, and so a gate wrap-around (drain) transistor layout design was considered in this project. In this type of transistor, the gate contact encircles the drain contact of the device. The advantage of using such a design is that the device mesa isolation is not required which in-turn enables a fast turnaround in device production as only two main lithography steps (excluding bondpad lithography) are needed in order to fabricate devices.

### 5.1.2 Process Flows

The main steps involved in the process flow of fabricating the normally-off AlGaN/GaN HEMTs are sample cleaning and preparation, photolithography (Ohmics and gate), metallization (Ohmic and gate metals), Ohmic contacts annealing, dielectric deposition, and dry etching of dielectric. Figure 5.2 shows the process flow for device fabrication. Some process details, for example use of different photoresist, are applicable using these same fabrication steps. Where there is a modification of the process flow used to fabricate a particular device, this will be indicated in the relevant section.

The device structure is a (drain) wrap-around gate requiring a minimum number of processing steps. The source/drain Ohmic contacts were formed by photolithography, metal deposition and lift-off as illustrated in Figure 5.2(a) and (b). The Ohmic metal scheme used was Ti/Al/Ni/Au with thicknesses of 30 nm, 180 nm, 40 nm, and 100 nm, respectively. The sample was then annealed at 775 °C for 30 seconds in nitrogen ($N_2$) ambient and then a layer of $SiO_2$ with a refractive index of around 1.5 was deposited by plasma enhanced chemical vapour deposition (PECVD) as illustrated in Figure 5.2(c). It should be noted that the sample was not cleaned after annealing and before the deposition of the $SiO_2$ film. This dielectric pre-deposition cleaning process is vital to getting rid of surface traps as is demonstrated in the CV graphs shown in Appendix C.2 of this thesis. Further work is planned to investigate the full extent of the effect of surface cleaning before dielectric deposition. The surface of the sample underneath the gate region was fully exposed to nitrogen ($N_2$) during the annealing step. The exposure of the very thin (3 nm) AlGaN barrier layer to such high annealing temperature could

cause some damge in the material which could affect the device performance. The gate contacts were then formed by lithography, metal deposition and lift-off as indicated in Figure 5.2(d) and (e). The metal scheme used for the gate was Ni/Au with thicknesses of 50 nm and 150 nm, respectively. Ohmic bond pad patterns were then defined by photolithography and the $SiO_2$ dielectric was etched away from the top of the Ohmic contacts by RIE as indicated in Figure 5.2(f). The bondpad metal was then deposited on top of the regions of the Ohmic contacts which were exposed during the dielectric etch. The metal scheme used for the bondpads was Ti/Au with thicknesses of 20 nm and 200 nm, respectively. The final cross-section of the fabricated e-mode HEMT is indicated in Figure 5.2(g). Further details of these processes are presented in the following sections.

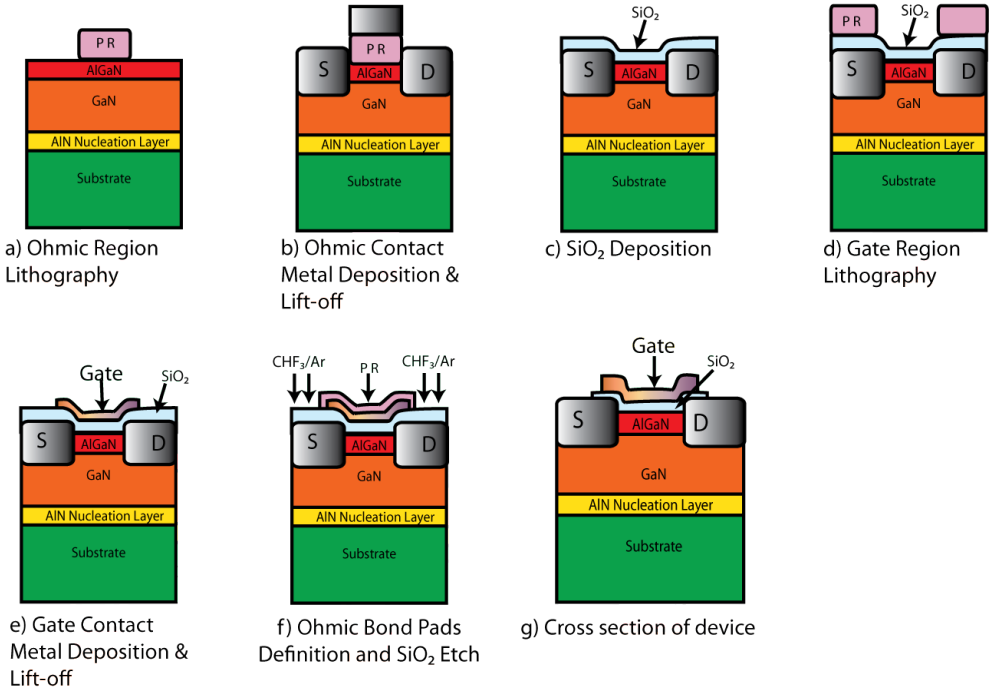



FIGURE 5.2: Typical process flow used to fabricate e-mode HEMTs in this research. PR stands for photoresist.

#### 5.1.2.1 Sample Cleaning and Preparation

Sample cleaning is essential before starting any fabrication process for two main reasons. The first reason is to remove the native oxide that forms when the semiconductor surface is exposed to air or other ambient, while the second reason is to remove any dust particles and the remains or residues that arise, e.g. while the wafer is being cleaved.

#### 5.1.2.2 Photolithography

Two photolithography recipes were used for Ohmic and gate patterning in this project. The photoresists used for the first recipe (photolithography recipe 1) are the Shipley

S1818 for Ohmic lithography and the Shipley S1805 for gate lithography. They are both positive photoresists and were chosen because of their well developed processes available in the James Watt Nanofabrication Centre (JWNC). The optical lithography processing starts with the sample cleaning prior to the photoresist coating. The mask plate is also cleaned prior to the mask exposure. To form a good patterning, the original mask (the chrome plated mask plate) instead of a copy was used. After cleaning, the photoresist (S1818 for Ohmics and S1805 for gate) is applied to the wafer surface with constant spinning speed of 4000 revolutions per minute (rpm) for 2 minutes. After spinning, the sample is baked on a hot plate at 65 °C for 2 minutes. Spinning of the sample provides uniform photoresist coating while the baking is done to remove the solvent from the photoresist film and also to increase the adhesion of the photoresist to the sample. The S1818 photoresist results in a resist layer thickness of 1.8 $\mu$m while the S1805 photoresist results in a thickness of 0.5 $\mu$m. The sample is then pre-developed in a developer solution containing Shipley Microposit Developer Concentrate and water at a ratio of 1:1 for 60 seconds and then it is rinsed with reverse osmosis (RO) water for 60 seconds. The pre-development of the photoresist causes a hardening of the upper layer of the unexposed photoresist. After that, the sample is then aligned with respect to the mask using the Karl Suss MA6 mask aligner machine. When the sample is correctly aligned to the pattern on the mask (this is done by checking through the optical microscope on the mask aligner), it is brought into contact with the mask and the photoresist is exposed under ultraviolet (UV) light (wavelength of 365 nm). The exposure time for Ohmic and gate lithography is 5 and 3 seconds, respectively. The exposed photoresist is dissolved in the developer solution containing Shipley Microposit Developer Concentrate and water at a ratio of 1:1 for 75 seconds with slight agitation. Once developed, the photoresist profile exhibits an undercut created by an increased development time. The sample is then rinsed with RO water for 60 seconds and blow dried with a nitrogen gun. After the photoresist development, the sample is ashed in the Oxygen Barrel Asher at 40 watts for 3 minutes in order to remove the resist residues left in the developed regions of the sample surface after development. Figure 5.3 illustrates the process flow for performing photolithgraphy and metallization using the first recipe. This process flow will be referred to as photolithography recipe 1 in the remainder of this thesis.

A second recipe for photolithography (photolithography recipe 2) was developed in order to improve the undercut profile and hence provide better lift-off. Lift-off after metallization of samples using this new recipe was found to be better and cleaner (hardly any unwanted metal deposits were left on sample surface). The second recipe involved the use of two photoresists; the LOR 10A and the S1818 for both Ohmic and gate lithography. The lithography process for this is started after sample cleaning. The sample surface is firstly covered by the first layer of photoresist LOR 10A, and span at 6000 rpm

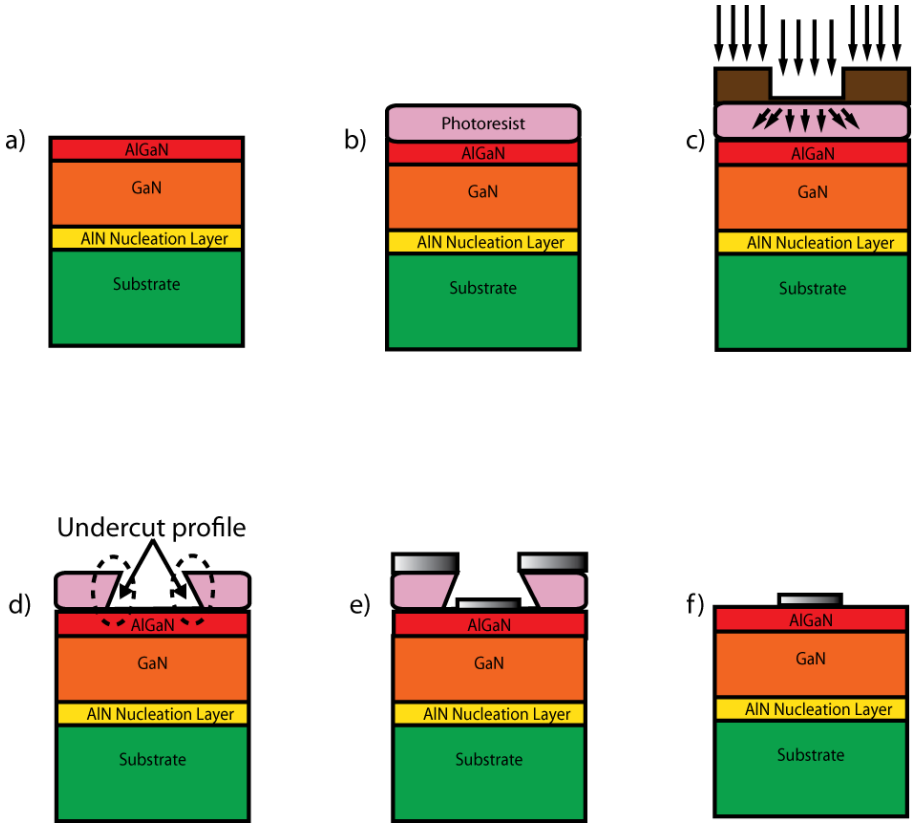



FIGURE 5.3: Photolithography process using recipe 1. a) sample is cleaned b) photoresist is spun onto sample c) sample is soaked in developer solution and exposed under UV light with mask plate in contact with sample d) photoresist is developed giving an undercut profile e) sample is metallized f) lift-off process is performed to remove photoresist and unwanted metal while leaving behind only the metal which is directly evaporated onto the sample surface.

for 30 seconds, then it is baked on a hot plate at 150 °C for 2 minutes. After that, the second layer of photoresist is applied to the sample and span at 4000 rpm for 30 seconds, then it is baked at 115 °C for 3 minutes. Once the coating of the sample is completed, the next step is exposing it in the mask aligner. Once the sample is accurately aligned with the pattern on the mask, the exposure can be performed. The photoresist is exposed to UV light when the sample is brought in contact with the mask and the exposure time is 6 seconds. The exposed sample is then soaked in MF319 developer solution for 2 minutes and 30 seconds and then rinsed with RO water for 60 seconds. Finally the sample is blow dried with a nitrogen gun. After the photoresist development, the sample is ashed in the Oxygen Barrel Asher at 60 watts for 5 minutes in order to remove the resist residues left in the developed regions of the sample surface after development. Figure 5.4 illustrates the process flow for performing photolithography and metallization using the second recipe. Wherever photolithography recipe 2 is stated in this thesis, this description here should be used as reference of the process flow.

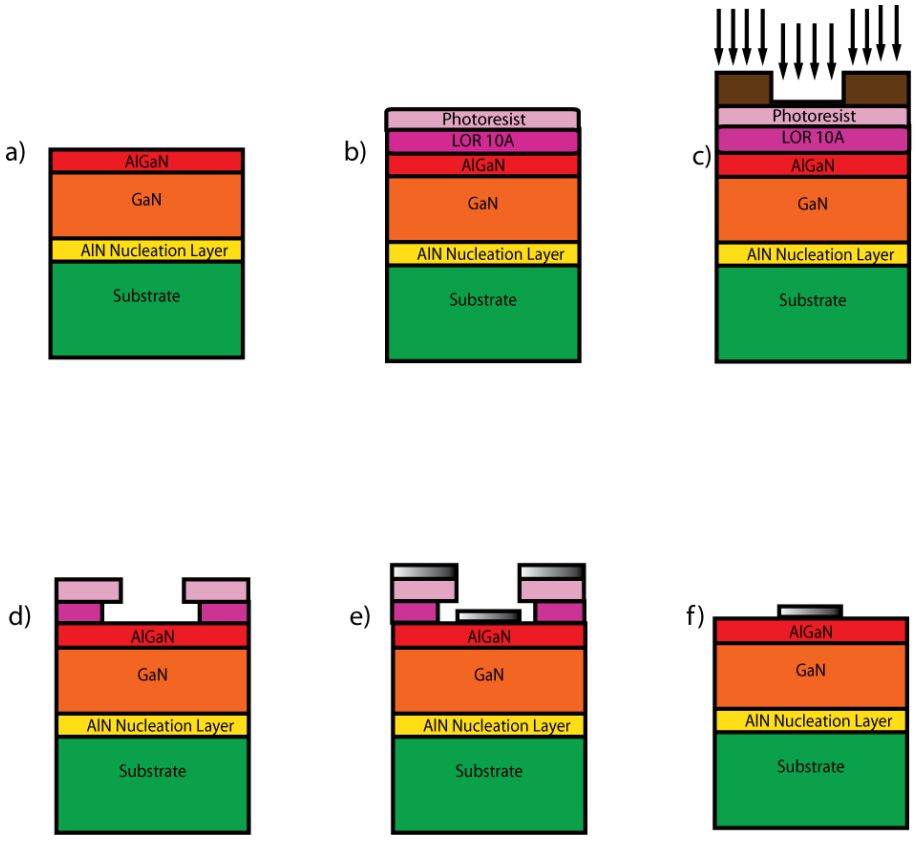



FIGURE 5.4: Photolithography process using recipe 2. a) clean sample b) spin and bake LOR 10A and photoresist c) expose sample under UV light d) develop resist and LOR 10A e) deposit metal f) lift-off the bi-layer stack and unwanted metal from sample surface.

#### 5.1.2.3 Metallization

Deposition of metals onto semiconductor wafers or samples can be performed through several different methods including thermal or electron beam evaporation and sputtering. In this project, electron beam evaporation was employed for the metallization process by using either a Plassys MEB 400S electron beam evaporator (Plassys II) or a Plassys MEB 550S (Plassys IV). Before Ohmic metal deposition, the sample is de-oxidised by soaking it in hydrochloric acid:water ($HCl : H_2O$) solution of 1:4 ratio for 1 minute at room temperature, in order to remove the native oxide which forms when the AlGaN barrier layer surface is exposed to ambient air. The sample is loaded into the chamber of the Plassys and then the required metal stack and layer thickness is specified on the computer connected to the equipment. The Ohmic metal scheme is Ti/Al/Ni/Au (30 nm/180 nm/40 nm/100 nm), respectively. The gate metal scheme is Ni/Au (50 nm/150 nm), respectively. This process is automatic and the equipment deposits the chosen metals on the sample in sequence through a recipe that appears on the computer display. Since the patterns have already been defined on the photoresist during

the photolithograpy stage, when the evaporated metal covers the sample surface, part of the deposited metal covers the exposed areas directly on the semiconductor surface, while the others are deposited on top of the photoresist on the unexposed areas. Lift-off technique is employed for simple and easy patterning of the metals that are deposited. During lift-off, the metals which are deposited on top of photoresist are removed, while the metals directly deposited on the exposed areas on top of the semiconductor material remain to form the contacts. For photolithography recipe 1, the lift-off process is performed by soaking the sample in a 50 °C warm acetone for 15 minutes for complete lift-off of photoresist and unwanted metal. For photolithography recipe 2, lift-off is performed by firstly soaking the sample in a 50 °C warm acetone for 15 minutes to remove the photoresist and then in a 50 °C warm 1165 stripper for 10 minutes to remove the LOR and unwanted metal. After the lift-off of the metals, the sample is rinsed with RO water for 1 minute, soaked in IPA for 1 minute and then blow dried with a nitrogen gun.

#### 5.1.2.4 Ohmic Annealing

Having deposited the metal stack of the Ohmic contacts, annealing is the fundamental process used to achieve many aims including creating an alloy of low resistance, creating nitrogen vacancies (in the AlGaN barrier layer) which act as n-type doping, enhancing the adhesion of metal to the semiconductor and increasing mechanical stability [165]. In Section 2.5.2, the function of each metal in the Ohmic metal scheme was explained. Ohmic contact rapid thermal annealing is often carried out in nitrogen ($N_2$) or hydrogen ($H_2$) ambient for around 30 to 60 seconds. The Joint Industrial Processors for Electronics (JIP ELEC) JetFirst rapid thermal annealer (RTA) system was used for annealing the Ohmic metal contacts at a temperature of 775 °C for 30 seconds under nitrogen ($N_2$) ambient. Figure 5.5 shows microscope images of transistors during fabrication. The image on the left shows the source and drain Ohmics after they are metallized and the image on the right shows the Ohmics after they are annealed at high temperature. The roughness of the Ohmic metals shows the effect of the high temperature during annealing process which enables the mixture of the first metal in the Ohmic metal stack (Ti) with the semiconductor and hence the formation of an alloy.

#### 5.1.2.5 Dielectric Deposition

After annealing of the Ohmic contacts, silicon dioxide ($SiO_2$) was deposited on the samples by plasma enhanced chemical vapour deposition (PECVD) in the dry etch lab of the JWNC using the Oxford Instruments PECVD 80 Plus tool. The following deposition conditions were used: temperature of 300°C, RF power of 15 watts, and pressure of 1 torr. The gases used for dielectric deposition were $SiH_4$, $N_2O$ and $N_2$ at

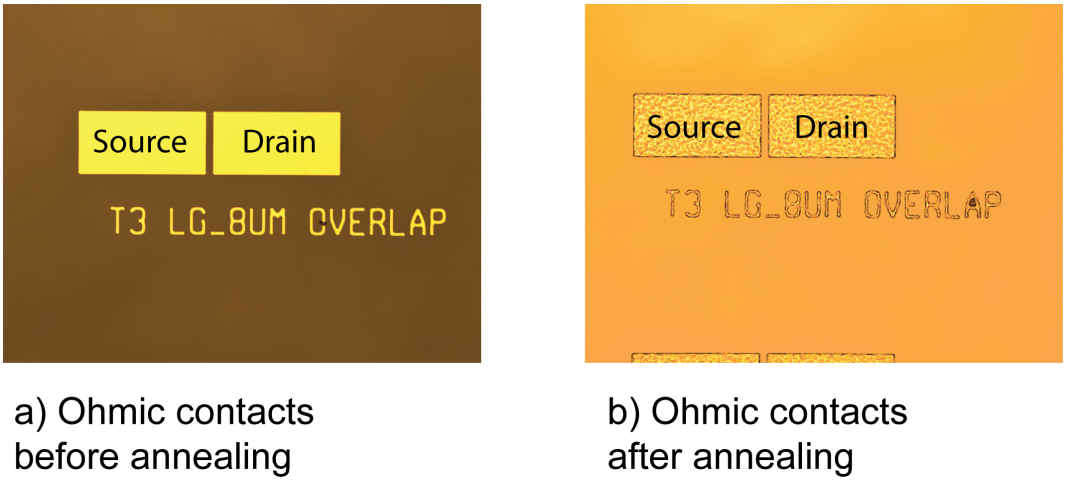



FIGURE 5.5: Optical microscope image of Ohmic contacts for a gate wrap-around device after metallization before and after rapid thermal annealing.

flow rates of 7 sccm, 200 sccm and 85 sccm, respectively. Deposition times depend on the thickness of dielectric film required. The dielectric isolates the gate metal from the Ohmic contacts and the semiconductor. When a positive gate voltage is applied (with respect to the source), the metal gate, dielectric and semiconductor heterojunction act similar to a parallel plate capacitor and electrons are attracted to the heterojunction interface.

#### 5.1.2.6 Dry Etching

Dry etching was used to remove the dielectric from certain parts of the sample surface to expose the metal contacts for device characterization. In the JWNC, the PECVD $SiO_2$ was etched using the Oxford Instruments RIE 80 Plus tool. The gases used were $CHF_3$ and Ar at flow rates of 25 sccm and 18 sccm, respectively. During this process, an RF power of 200 watts and a pressure of 20 millitorr are used at room temperature. All equipment in the lab which require room temperature for operation are run at 22 °C. The etch rate for $SiO_2$ using this etch chemistry is around 37 nm/min, this enables the etching time for various thicknesses of $SiO_2$ to be calculated accordingly. For example, to etch a 20 nm thick $SiO_2$ film, the etch time ia calculated to be around 32.5 seconds. Figure 5.6 shows microscope images of gate wrap-around transistors before the dielectric is etched away from the surface of the Ohmic contact metals and after the bondpads are exposed and metallized on top of the source and drain contacts.

### 5.1.3 Mask Design and Layout

As mentioned earlier, the mask plate is required to pattern the photoresist during the photolithography process. After the L-Edit CAD software is used to create a pattern

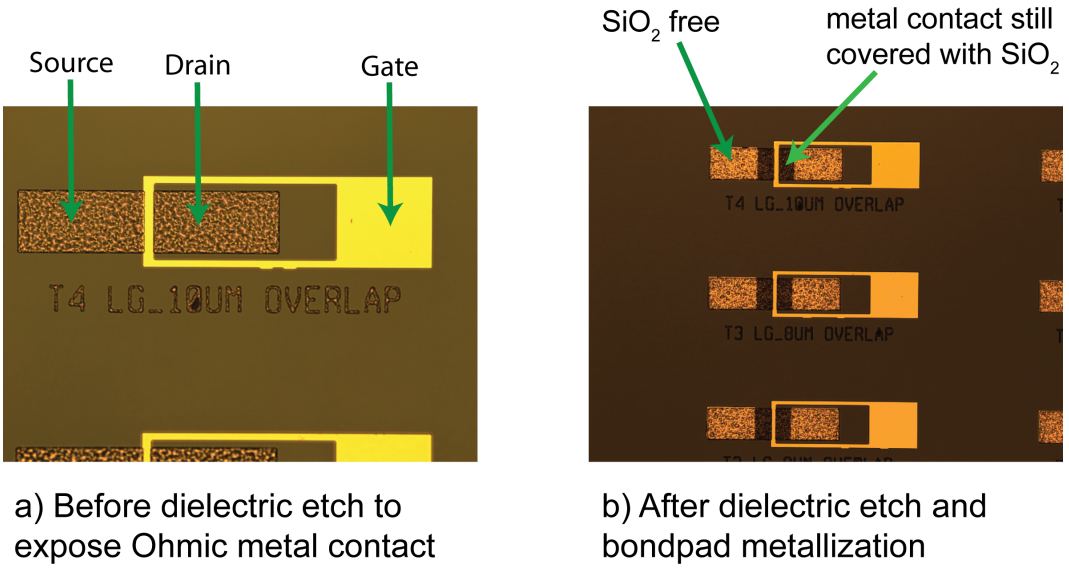



FIGURE 5.6: Optical microscope image of gate wrap-around device before and after dielectric etch and Ohmic bondpad formation.

file, this file is exported into a GDS II file format and sent to the JWNC in University of Glasgow for fabrication on a quartz mask. The devices considered and fabricated in this project are DC devices. Figure 5.7 shows a picture of an L-Edit layout for a gate wrap-around transistor indicating all the layers which will be patterned on the mask plate. Each pattern corresponds to a photolithography step performed during the fabrication of the transistor. Figure 5.8 shows L-Edit images of gate wrap-around (drain) transistors with the gate contacts of each transistor overlapping the source and drain Ohmic contacts nominally. The transistors in "a", "b", "c" and "d" of this figure have gate lengths of 4 $\mu$m, 6 $\mu$m, 8 $\mu$m and 10 $\mu$m, respectively. The e-mode HEMTs fabricated in this project all use the same design layout as shown in this figure. Figures 5.9, 5.10 and 5.11 shows images of the Ohmic, gate and bondpad lithography layers, respectively, while Figure 5.12 shows an image of the combination of all three lithography layers on the mask plate. They also show images of the metal-oxide-semiconductor capacitors (MOSCAPs) which are presented in Appendix C.

## 5.2 Summary

This chapter presented a schematic overview and description of the process flows used to fabricate single finger normally-off GaN devices. A summary of the individual process details is provided in Appendix A for easy reference. A brief discussion on the mask design and layout of these devices was then presented. A detailed presentation and analysis of the DC characteristics of the e-mode GaN devices fabricated in this work will be provided in the next chapter.

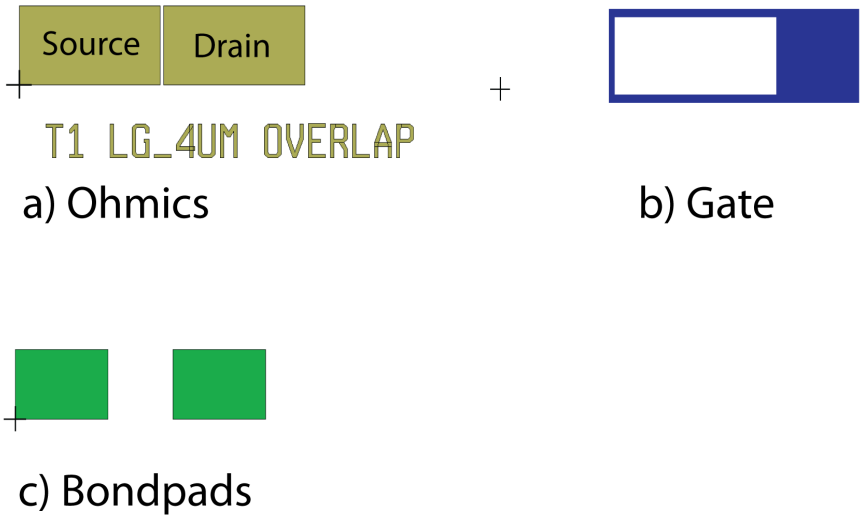



FIGURE 5.7: L-Edit layout of individual cells of a gate wrap-around transistor layers to be formed by photolithography.

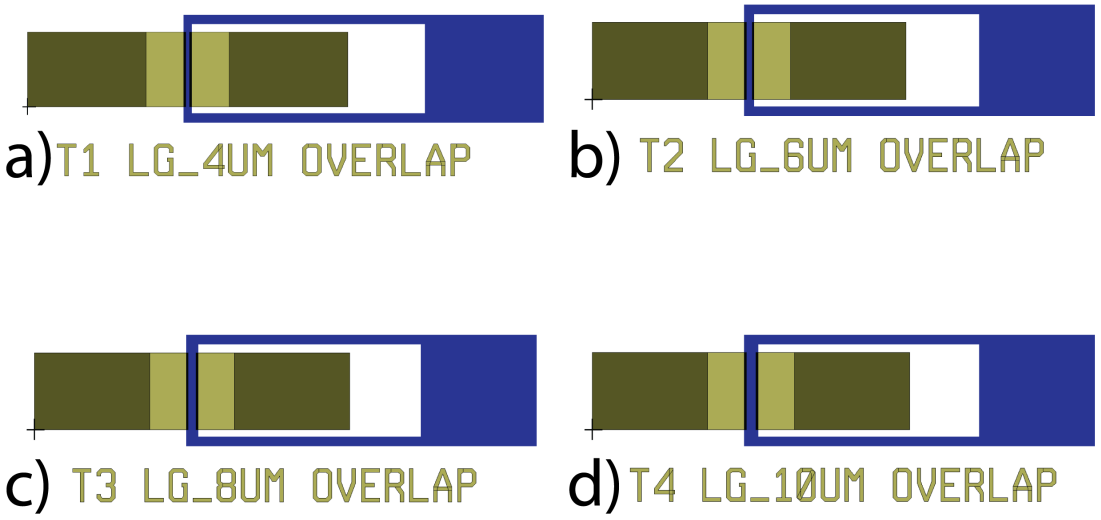



FIGURE 5.8: L-Edit layout of a gate wrap-around HEMT (source and drain Ohmic contacts are nominally overlapped by the gate contact).

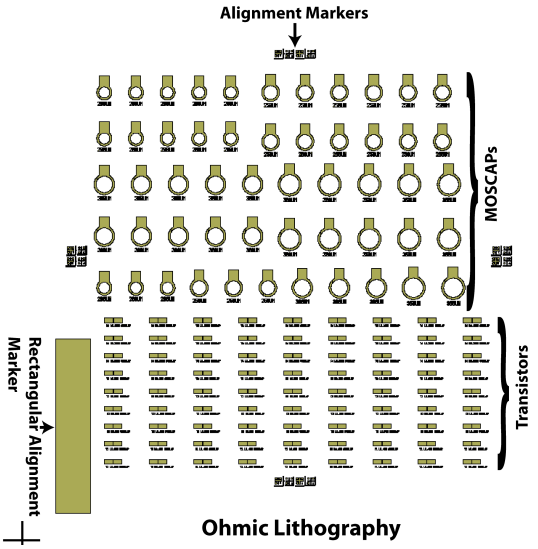



FIGURE 5.9: L-Edit layout of Ohmic contacts on mask plate which was used for Ohmic lithography during fabrication of e-mode HEMTs.

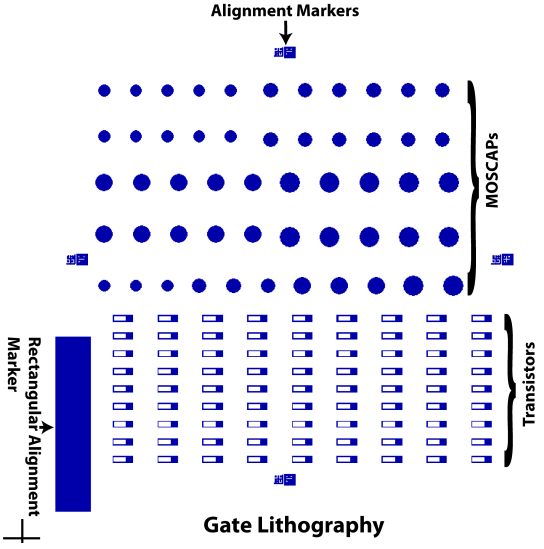



FIGURE 5.10: L-Edit layout of gate contacts on mask plate which was used for gate lithography during fabrication of e-mode HEMTs.

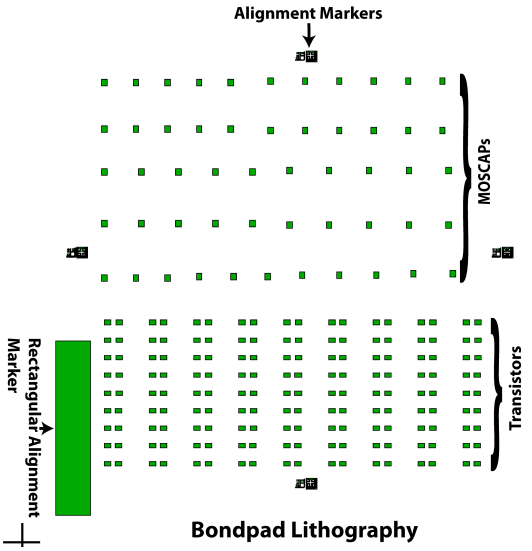



FIGURE 5.11: L-Edit layout of bondpads on mask plate which was used for bondpad lithography during fabrication of e-mode HEMTs.

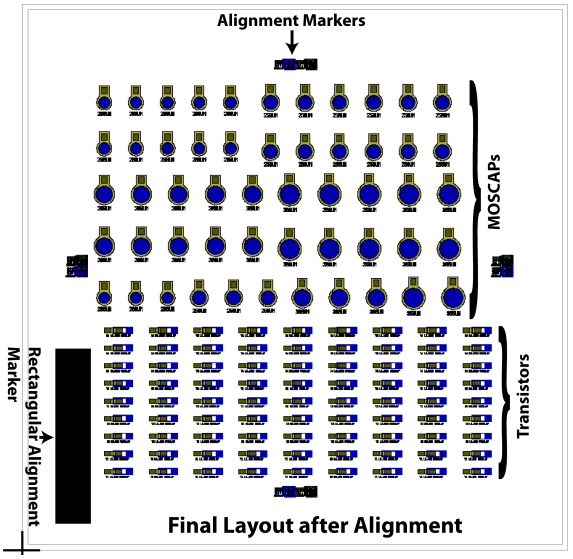



FIGURE 5.12: L-Edit layout of the three lithography layers used during photolithograpy to fabricate e-mode HEMTs after successful alignment.

# CHAPTER 6

# NOVEL NORMALLY-OFF AlGaN/GaN MOS-HEMT

In this chapter, results of the proposed normally-off AlGaN/GaN transistors are presented. Devices grown on different substrates, sapphire and silicon, and employing different gate lengths will be presented. The device characteristics including output characteristics, transfer characteristics, and transconductance of the devices will be given and analysed. We will also present the breakdown voltages of these devices and a preliminary study of their reliability.

## 6.1 Normally-off AlGaN/GaN MOS-HEMT on Sapphire Substrate

### 6.1.1 Device Structure and Fabrication

Figure 6.1 shows a cross-section of the proposed normally-off AlGaN/GaN HEMT. It consists of a sapphire substrate of approximately 350 $\mu$m thickness, a 2-5 nm thick aluminium nitride (AlN) nucleation layer, a 3 $\mu$m GaN channel, and a 3 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The structure was grown using molecular beam epitaxy (MBE) by SVT Assiciates, USA. The device consists of source and drain Ohmic contacts nominally overlapped by the gate contact and employs a gate dielectric. With no or low gate-to-source voltage($V_{GS}$), there is no two dimensional electron gas (2DEG) channel at the AlGaN/GaN interface to allow conduction of current between the drain and source contacts as the AlGaN barrier thickness is below the critical thickness required for the formation of such channel [55]. However, if a large enough positive bias voltage $V_{GS}$ is applied, it causes the formation of a quantum well at the AlGaN/GaN interface into

which electrons from the source and drain Ohmic regions are attracted (by the positive gate voltage), effectively creating a 2DEG channel, and so the structure is a normally-off field effect transistor. As the critical device feature required for normally off operation, the AlGaN layer, is grown epitaxially, and this eliminates the drawbacks experienced with previous techniques such as recess-etching in which the uniformity of the etch and hence that of the threshold voltages ($V_{th}$) is difficult to achieve. $V_{th}$ is set further by the thickness and properties of the gate dielectric.

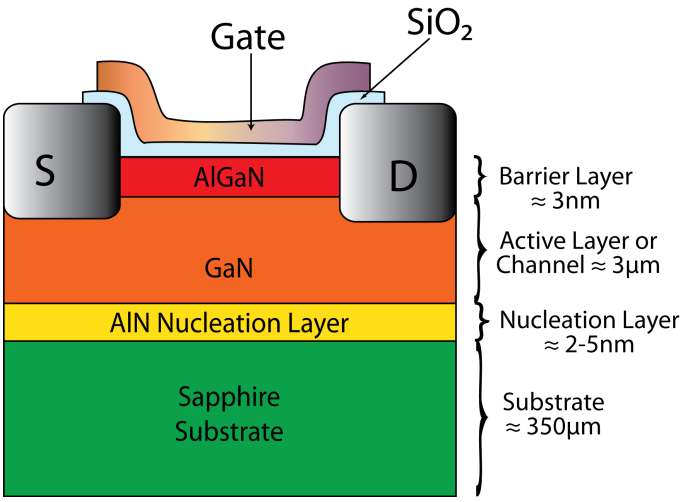



FIGURE 6.1: Cross-section of the proposed e-mode AlGaN/GaN device.

Single finger 100 $\mu$m wide devices were fabricated to test the device concept using process modules described in the earlier chapters. The source and drain Ohmic contacts were formed by photolithography, metal deposition using Ti/Al/Ni/Au metallization scheme, and lift-off. The sample was then annealed at 775 °C for 30 seconds in $N_2$ ambient and then a layer of $SiO_2$ was deposited by PECVD at 300 °C using the following conditions: RF power of 15 watts, pressure of 1 torr, flow rate ($SiH_4/N_2O/N_2$) of 7/200/85 sccm, and a deposition rate of about 70 nm/min. The gate contacts were then formed by photolithography, metal deposition (Ni/Au, 50 nm/150 nm) and lift-off. Ohmic bond pad patterns were then defined by photolithography and the $SiO_2$ dielectric etched to expose the Ohmic contacts to complete the processing.

### 6.1.2 Device Output and Transfer Characteristics

Results from typical devices from 2 samples are presented here. One sample employs a nominal 10 nm, while the other 20 nm thick $SiO_2$ dielectric. Both devices employ 6 $\mu$m long and 100 $\mu$m wide gates. Output and transfer characteristics as well as the transconductance were measured using Agilent's B1500A Device Analyzer. Figure 6.2 shows the output characteristics of the device with 10 nm thick $SiO_2$ gate dielectric

which demonstrated maximum drain current $I_{DSmax}$, of over 450 mA/mm at gate voltage $V_{GS} = 6$ V and drain voltage $V_{DS} = 10$ V.

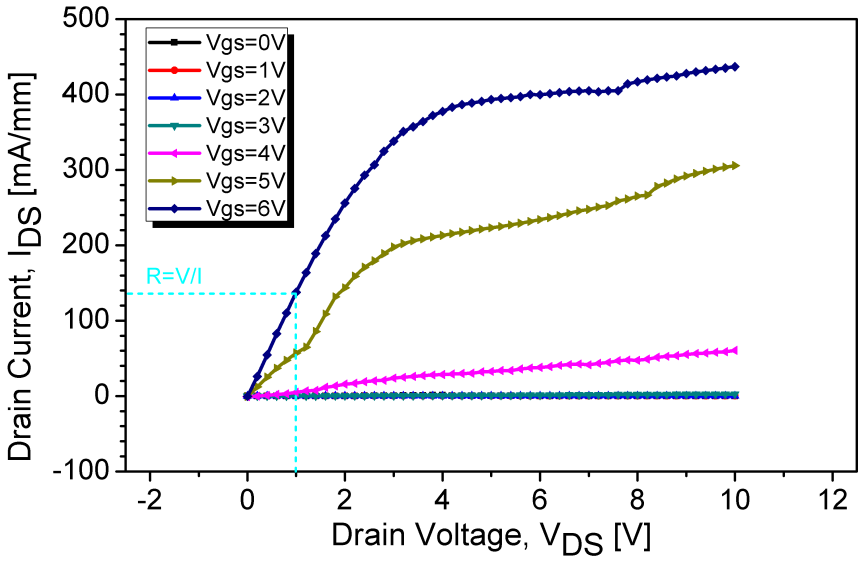



FIGURE 6.2: Output characteristics of an e-mode 6 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 10 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V, 1 V, 2 V, and 3 V.

Figure 6.3 shows the output characteristics of the device with 20 nm thick dielectric. This device demonstrated $I_{DSmax}$ of over 650 mA/mm at $V_{GS} = 6$ V and $V_{DS} = 8$ V. The measured currents are comparable to those of conventional depletion-mode devices demonstrating the equally good properties of an induced 2DEG channel. A procedure to extract contact resistances for this non-conducting structure (when no 2DEG is present) that uses gated TLM structures is being developed, but the low knee voltages indicate good contacts.

The specific on-resistance $R_{ON_{spec}}$ of the device was obtained by multiplying the area, ($L_{SD} \times W_g$) with the resistance (R=V/I, indicated by blue short-dash lines in graph) of the device in the linear region. Note that the specific on-resistance of the device would be higher if the transfer length of the device is included in the calculation as this would result in the area being calculated as $[(L_{SD} + 2L_T) \times W_g]$. For the device output characteristics shown in Figures 6.2 and 6.3, the specific on-resistances are calculated/extracted as 43.5 m$\Omega$mm$^2$ and 42.3 m$\Omega$mm$^2$, respectively.

Transfer characteristics and transconductance at low drain bias voltages for the devices whose output characteristics are shown in Figures 6.2 and 6.3 are plotted in Figure 6.4. The threshold voltages are +3 V and +2 V (estimated at 1 mA/mm) for the 10 nm and

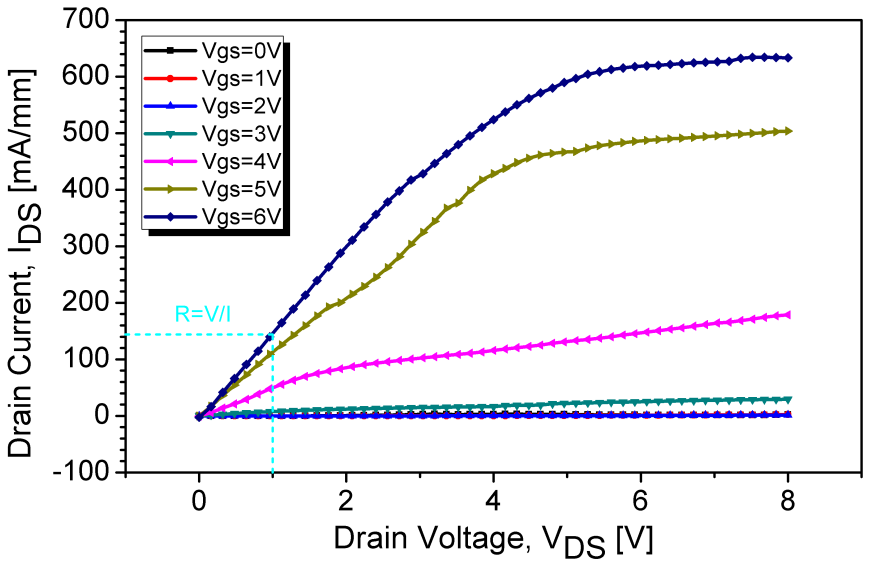



FIGURE 6.3: Output characteristics of an e-mode 6 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric. Drain current traces for $V_{GS}$ of 0 V, 1 V, and 2 V are overlapping.

20 nm thick gate dielectric devices. The enhancement-mode nature of the devices can be seen from these characteristics. The drop in threshold voltage with higher thickness of the $SiO_2$ is attributed to the increase in the $SiO_2$ positive charge with increasing thickness, increased film stress of thicker deposited dielectric, etc. The devices are known to suffer from extra capacitance due to the added capacitance of the gate-source and gate-drain overlap of the device. The added capacitance will affect the switching speed of the gate-overlap devices as the switching time depends on the device capacitance as given in the equation ($\tau = RC$), where $\tau$ is the switching time, R is the resistance of the device, and C is the capacitance in the device. Therefore, increasing the gate-overlap length will result in an increase in capacitance.

### 6.1.3 Offstate Breakdown Characteristics

Off-state ($V_{GS} = 0$ V) breakdown characteristics are shown in Figure 6.5. The breakdown voltages were 9 V and 17 V for the devices with 10 nm and 20 nm thick $SiO_2$ gate dielectrics, respectively. The current rises sharply from about 1 mA/mm to over 1000 mA/mm (set by equipment compliance) on breakdown. The measured breakdown field of approximately 9 MV/cm suggests that device breakdown is limited by the dielectric thickness, as seen in devices of similar geometry [162].

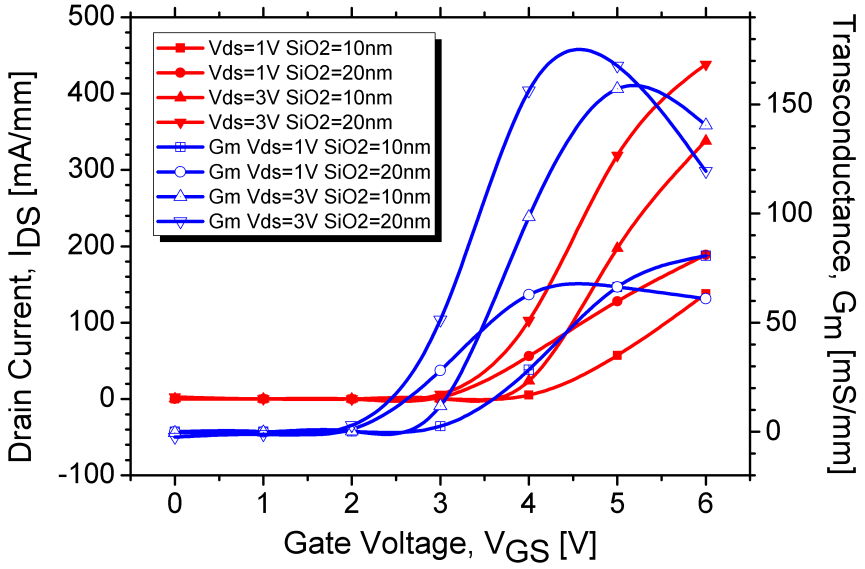



FIGURE 6.4: Transfer characteristics and transconductance of e-mode AlGaN/GaN MOS-HEMTs at low drain bias voltages of 1 V and 3 V.

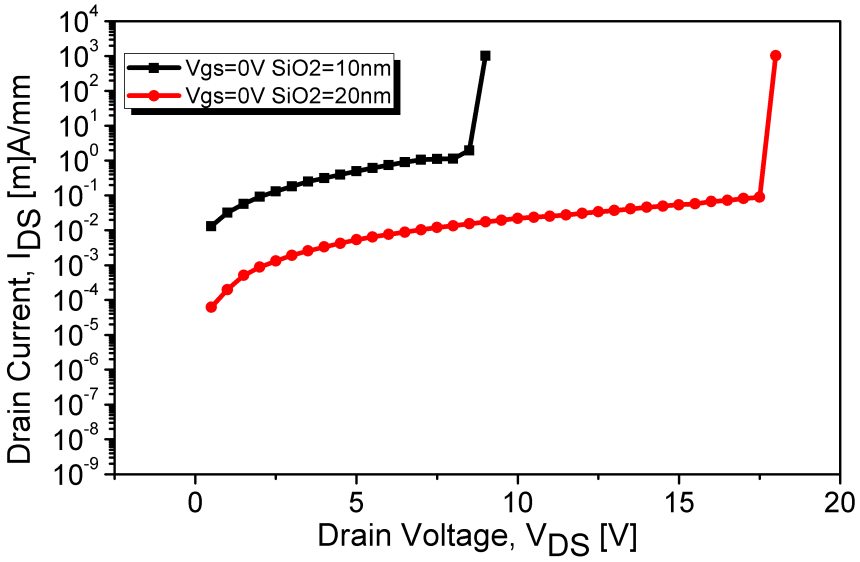



FIGURE 6.5: Breakdown characteristics of e-mode 6 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMTs with 10 nm and 20 nm thick $SiO_2$ gate dielectrics.

### 6.1.4 Device Reliability

Devices with 20 nm $SiO_2$ gate dielectric were assessed for stability. A stress test with $I_{DS} = 300\,mA/mm$ and $V_{DS} = 10\,V$ was performed at 10 minute intervals. Figure 6.6 shows the variation of the threshold voltage, $V_{th}$ with stress time. $V_{th}$ increased by 0.25 V within the first hour and continued to rise with stress time, and increased by approximately 1.25 V after 10 hours. The time-dependent shift of the threshold voltage in the device is attributed to the bulk traps in the gate dielectric and also interface traps located at the dielectric/semiconductor interface [166]. Unlike interface traps which are filled quickly, the bulk traps inside the gate dielectric can only be filled by the electrons tunnelling through the $SiO_2$ layer from the interface. The farther the trap is located from the interface, the lower the probability of the tunnelling process is. It is demonstrated in Figure 6.6 that the time constant to fill the bulk traps inside $SiO_2$ greatly influence the shift of threshold voltage as the traps are gradually filled under forward gate bias. In on-going work in the research group, device stability is being investigated via capacitance-voltage (CV) techniques for atomic layer deposited (ALD) high-$k$ dielectrics namely alumina, hafnia and zirconia that are deemed the best suited for this device structure [167]. Note that similar instability is a present problem in other insulated gate GaN devices [166].

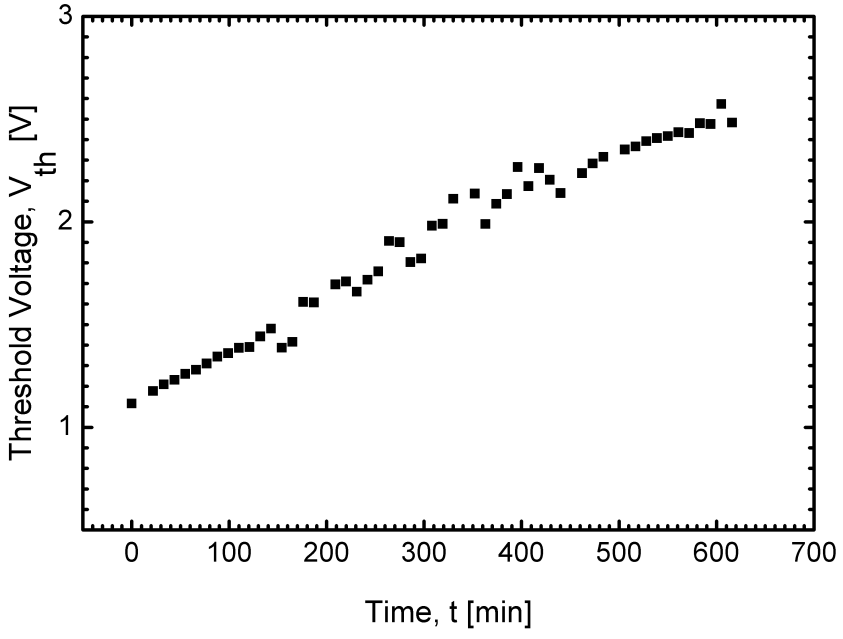



FIGURE 6.6: Variation of the threshold voltage of the proposed e-mode MOS-HEMT employing 20 nm thick $SiO_2$ gate dielectric with stress time.

## 6.2 Normally-off AlGaN/GaN MOS-HEMT on Silicon Substrate

### 6.2.1 Device Structure and Fabrication

The proposed normally-off AlGaN/GaN HEMT was also realised from GaN epitaxial material grown on a silicon substrate due to its low cost and availability of bigger size (diameter) wafers. Devices with varying $SiO_2$ dielectric thickness were fabricated in order to test for the reproducibility and repeatability of our device fabrication techniques. This also allowed us to test the consistency of the device DC characteristics. Figure 6.7 shows a cross-section of the device structure. It consists of a 600 $\mu$m silicon substrate, nucleation and transition/buffer layers, a 3 $\mu$m GaN channel, a 3 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 1 nm GaN cap layer. In AlGaN/GaN HEMTs with a high 2DEG sheet density, the 2D-electron lie very close to the AlGaN/GaN interface, which makes them very susceptible to any physical processes occurring at the interface such as interface roughness scattering, which is the dominant scattering mechanism at low temperatures. In order to reduce such affects, the separation between the 2D-carriers and the interface needs to be increased, which can be achieved if the AlGaN/GaN structures are capped with a GaN layer of appropriate thickness [168]. The GaN cap layer is also known to reduce gate leakage current in devices. The material was grown by metal organic chemical vapour deposition (MOCVD) by IQE Limited. Single finger devices of gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m and gate width of 100 $\mu$m were fabricated using the same process modules as in Section 6.1.1. A micrograph of a fabricated 4 $\mu$m × 100$\mu$m device is shown in Figure 6.8.

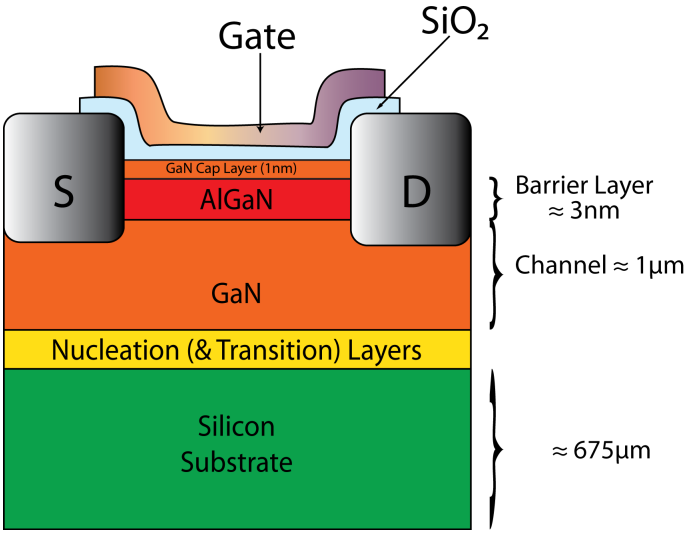



FIGURE 6.7: Cross-section of the proposed e-mode AlGaN/GaN device on silicon substrate.

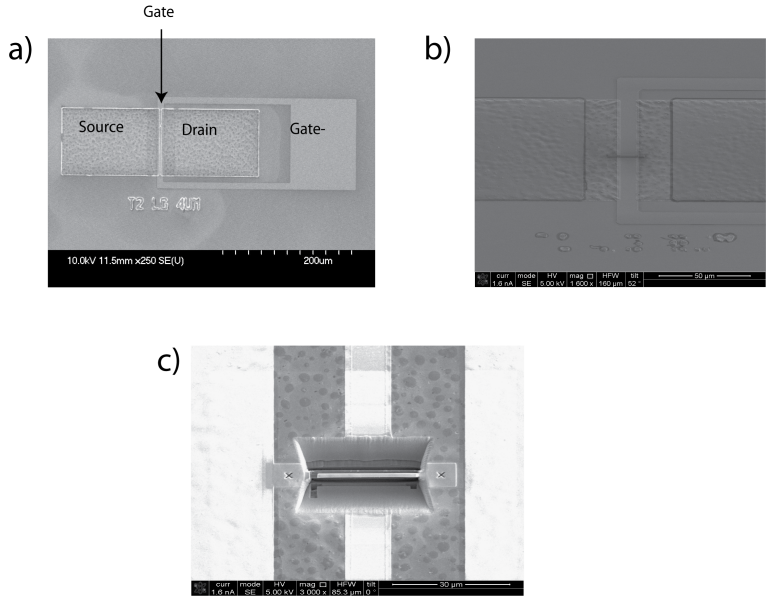



FIGURE 6.8: Scanning electron microscopy (SEM) image of normally-off AlGaN/-GaN device structure fabricated for DC measurements. Figure a) shows the top view of the gate, source and drain, Figure b) shows the image of the section which was cut in order to take transmission electron microscopy (TEM) images of the cross-section of the device, and Figure c) shows a zoomed in image of the section which was cut for TEM analysis

The cross-section of the device was further analysed using transmission electron microscopy (TEM) in order to check the step coverage of the gate and gate dielectric over the source and drain Ohmic metals of the device. The TEM image of the device cross-section is shown in Figure 6.9. It can be seen that the gate metal overlaps both the source and the drain metals of the device and the step coverage of both the gate and the dielectric over the source and drain Ohmic metals can clearly be seen on the zoomed images at the top of the image.

### 6.2.2 Device Output and Transfer Characteristics

Results from typical devices from 2 samples are presented here. One sample employs a nominal 20 nm, while the other 30 nm thick $SiO_2$ dielectric. Device characteristics were measured using Agilent's B1500A Device Analyzer. Figures 6.10, 6.11, and 6.12 show the output characteristics of devices with gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m, respectively. These devices have a 20 nm nominal thick $SiO_2$ dielectric. The devices exhibited maximum drain currents of 240 mA/mm, 180 mA/mm, and 170 mA/mm, respectively, at gate voltage $V_{GS} = 6$ V and drain voltage $V_{DS} = 10$ V. For the device output characteristics shown in Figures 6.10, 6.11, and 6.12, the specific on-resistances are calculated/extracted as 71.4 m$\Omega$mm$^2$, 13.3 m$\Omega$mm$^2$, and 181.8 m$\Omega$mm$^2$, respectively.

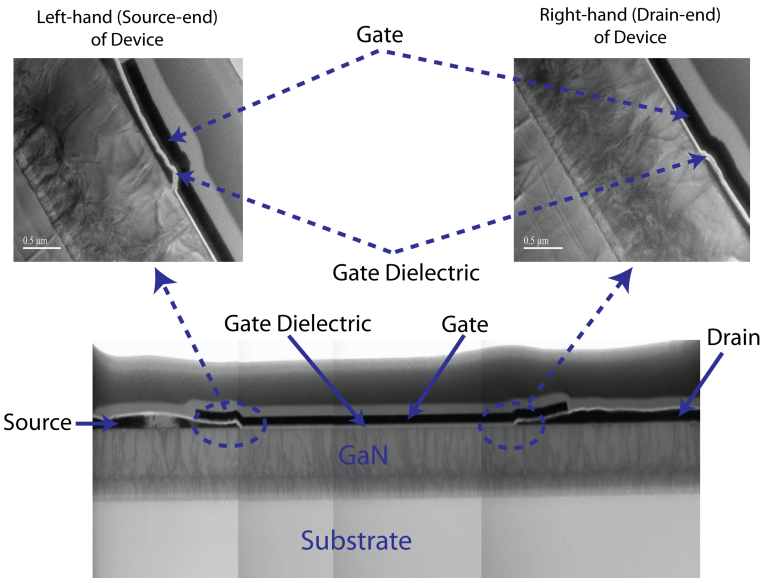



FIGURE 6.9: TEM image of cross-section of gate overlap device showing the dielectric step coverage

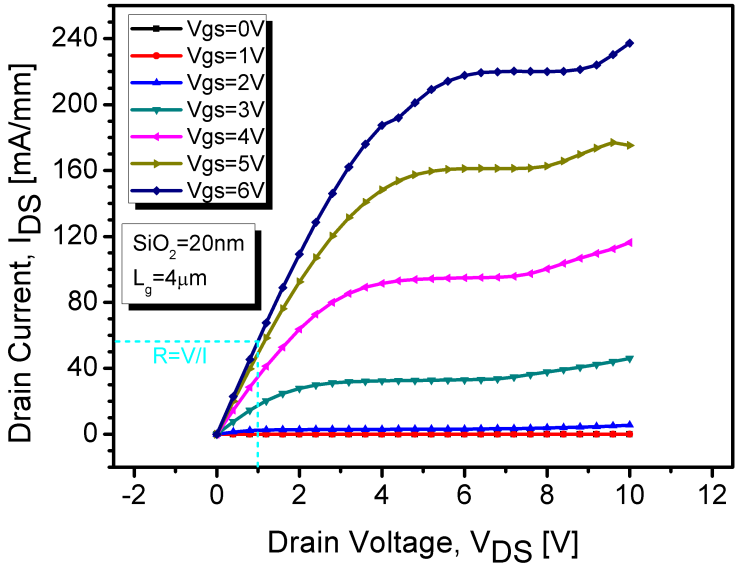



FIGURE 6.10: Output characteristics of an e-mode $4\,\mu\text{m} \times 100\,\mu\text{m}$ AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V and 1 V.

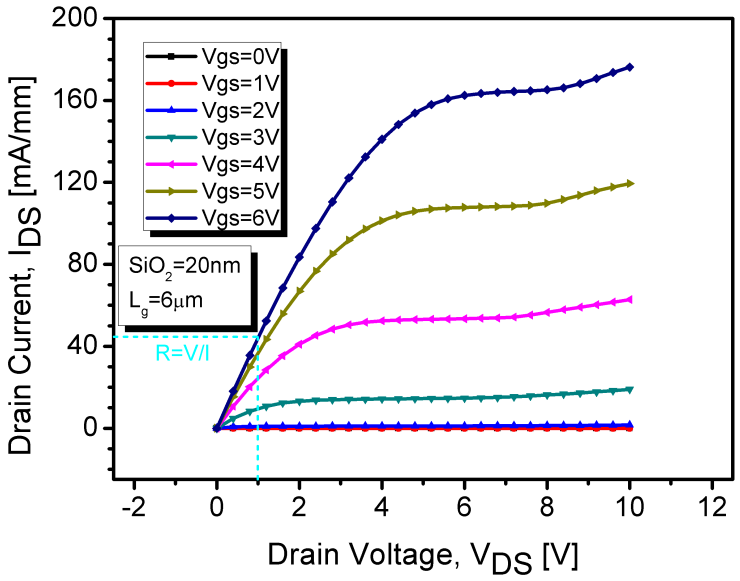



FIGURE 6.11: Output characteristics of an e-mode 6 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V, 1 V and 2 V.

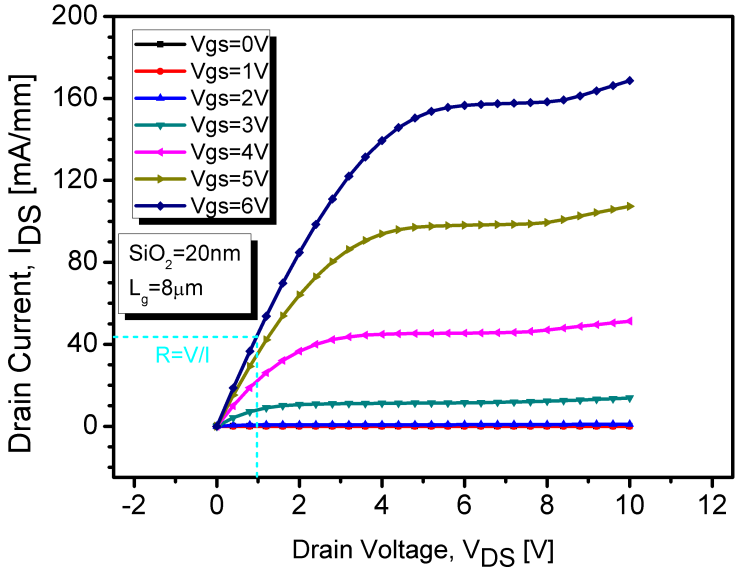



FIGURE 6.12: Output characteristics of an e-mode 8 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V, 1 V and 2 V.

Transfer characteristics and transconductance at linear ($V_{DS} = 1\,V$) and saturation ($V_{DS} = 10\,V$) regions for these devices are plotted in Figures 6.13, 6.14, and 6.15. The threshold voltages are +1 V, +1.5 V, and +1.5 V (estimated at 1 mA/mm), respectively, for these devices. The enhancement-mode nature of these devices can again be seen from these characteristics. The devices exhibited maximum transconductance ($G_{m-max}$) of 60 mS/mm at $V_{GS} = 5\,V$ and $V_{DS} = 10\,V$, 50 mS/mm at $V_{GS} = 5\,V$ and $V_{DS} = 10\,V$, and 50 mS/mm at $V_{GS} = 6\,V$ and $V_{DS} = 10\,V$ for the devices with gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m, respectively.

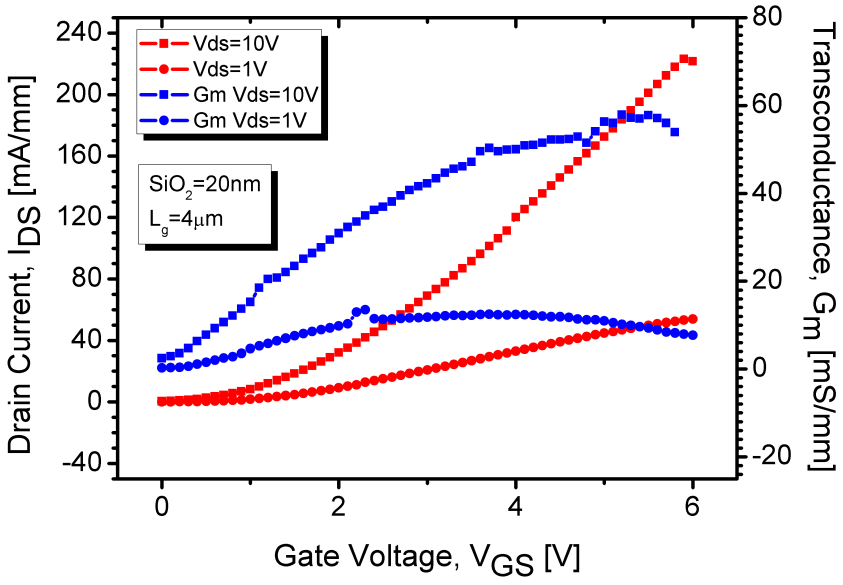



FIGURE 6.13: Transfer characteristics (left y-axis) and transconductance (right y-axis) of an e-mode 4 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric at drain bias voltages of 1 V and 10 V.

Figures 6.16, 6.17, and 6.18 show the output characteristics of devices with gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m, respectively. These devices have a 30 nm nominal thick $SiO_2$ dielectric. The devices exhibited maximum drain currents of 400 mA/mm, 130 mA/mm, and 105 mA/mm, respectively, at gate voltage $V_{GS} = 6\,V$ and drain voltage $V_{DS} = 10\,V$. For the device output characteristics shown in Figures 6.16, 6.17, and 6.18, the specific on-resistances are calculated as 28.2 m$\Omega$mm$^2$, 125 m$\Omega$mm$^2$, and 166.7 m$\Omega$mm$^2$, respectively.

Transfer characteristics and transconductance at linear ($V_{DS} = 0.5\,V$) and saturation ($V_{DS} = 10\,V$) regions for these devices are plotted in Figures 6.19, 6.20, and 6.21. The threshold voltages are +1 V, +1.5 V, and +1.5 V (estimated at 1 mA/mm), respectively, for these devices. The devices exhibited maximum transconductance of around

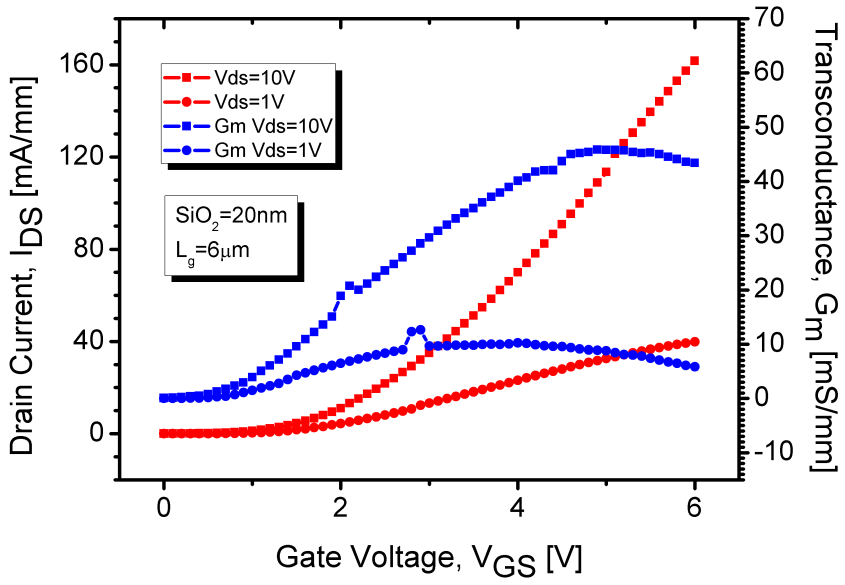



FIGURE 6.14: Transfer characteristics (left y-axis) and transconductance (right y-axis) of an e-mode 6 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric at drain bias voltages of 1 V and 10 V.

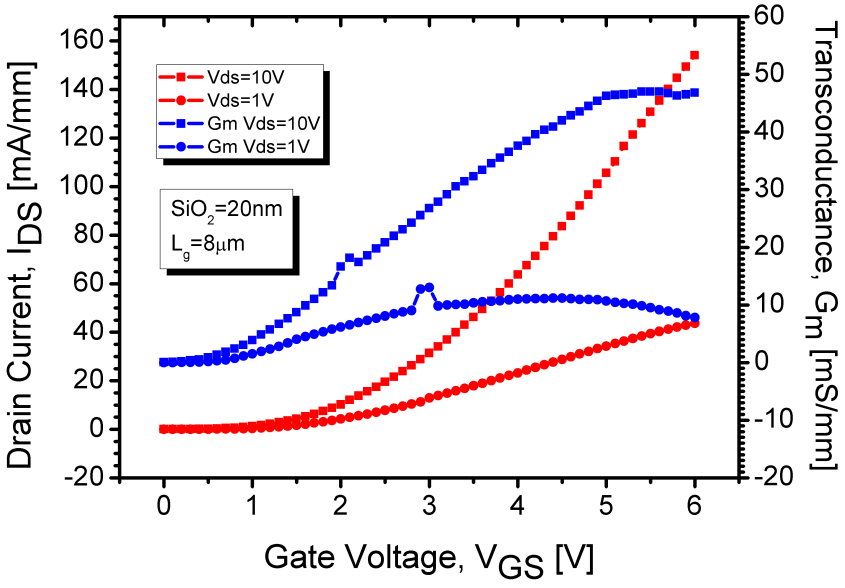



FIGURE 6.15: Transfer characteristics (left y-axis) and transconductance (right y-axis) of an e-mode 8 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick $SiO_2$ dielectric at drain bias voltages of 1 V and 10 V.

60 mS/mm, 50 mS/mm, and 50 mS/mm at a gate voltage of around 5 V and drain voltage of 10 V. The enhancement-mode nature of these devices can again be seen from these characteristics.

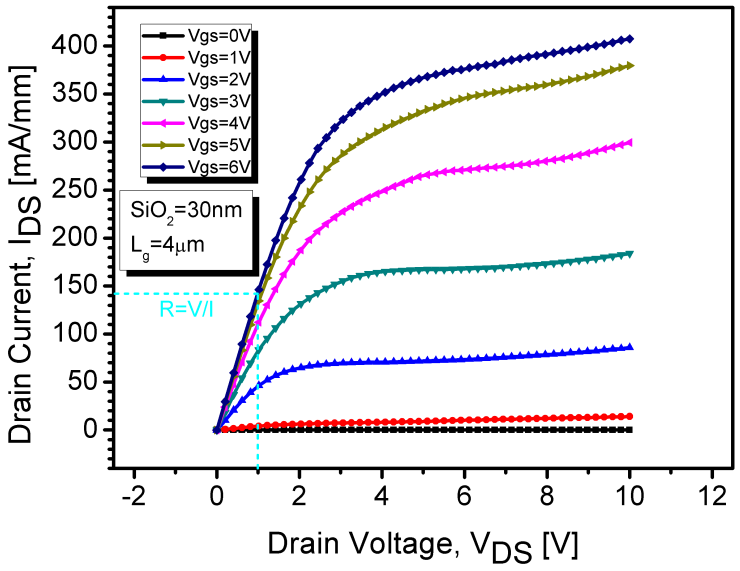



FIGURE 6.16: Output characteristics of an e-mode 4 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 30 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V and 1 V.

Figure 6.22 shows the gate leakage current of the normally-off devices with gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m, respectively for devices with a 20 nm nominal thick $SiO_2$ dielectric. It can be seen on the graph that the devices with gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m demonstrate gate leakage currents of less than 1 $\mu$A/mm at $V_{GS}$ of less than 6 V, 5 V, and 4.5 V, respectively. The devices therefore meet the required leakage current for power electronics application which is set to 1 $\mu$A/mm [169–171].

## 6.3 Summary

A new high performance normally-off GaN-based MOS-HEMT that employs an ultra-thin sub-critical 3 nm thick $Al_{0.25}Ga_{0.75}N$ barrier layer and relies on an induced 2DEG for operation was presented in this chapter. Single finger devices were fabricated using 10 nm and 20 nm PECVD $SiO_2$ as the gate dielectric. These devices, grown on a sapphire substrate, demonstrated threshold voltages ($V_{th}$) of +3 V and +2 V, and very high maximum drain currents ($I_{DSmax}$) of over 450 mA/mm and 650 mA/mm, at a gate voltage ($V_{GS}$) of 6 V, respectively.

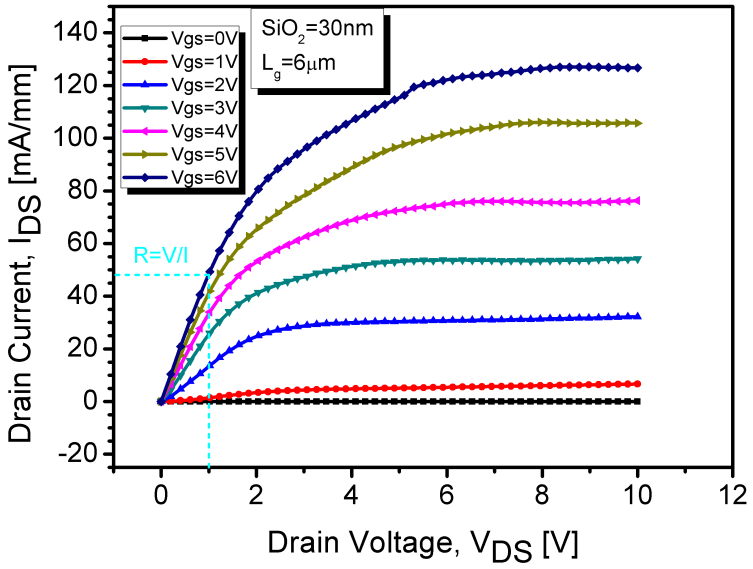



FIGURE 6.17: Output characteristics of an e-mode 6 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 30 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V, 1 V and 2 V.

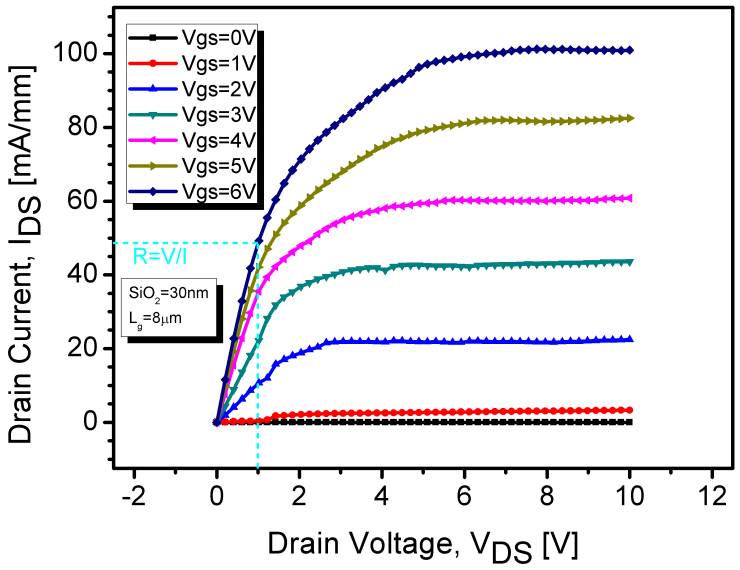



FIGURE 6.18: Output characteristics of an e-mode 8 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 30 nm thick $SiO_2$ dielectric. Note the (near) zero drain currents for $V_{GS}$ of 0 V, 1 V and 2 V.

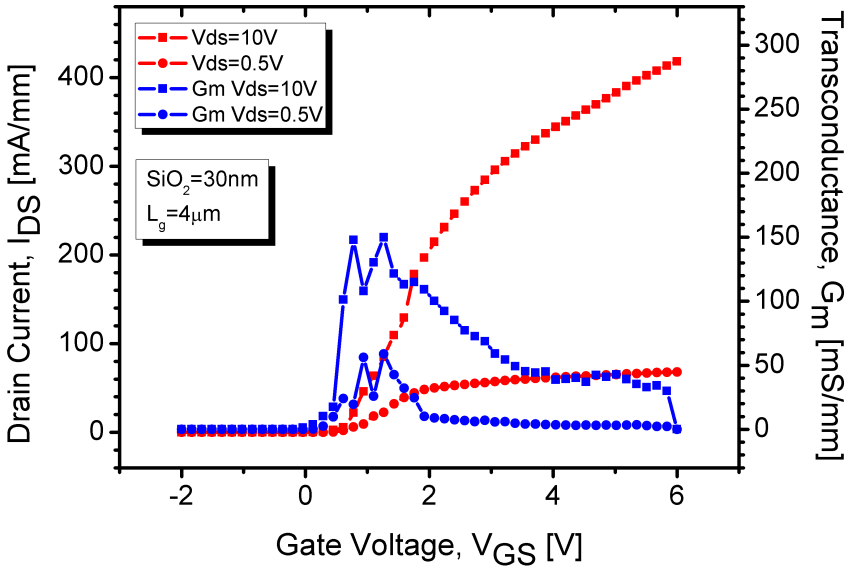



FIGURE 6.19: Transfer characteristics (left y-axis) and transconductance (right y-axis) of an e-mode 4 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 30 nm thick $SiO_2$ dielectric at drain bias voltages of 0.5 V and 10 V.

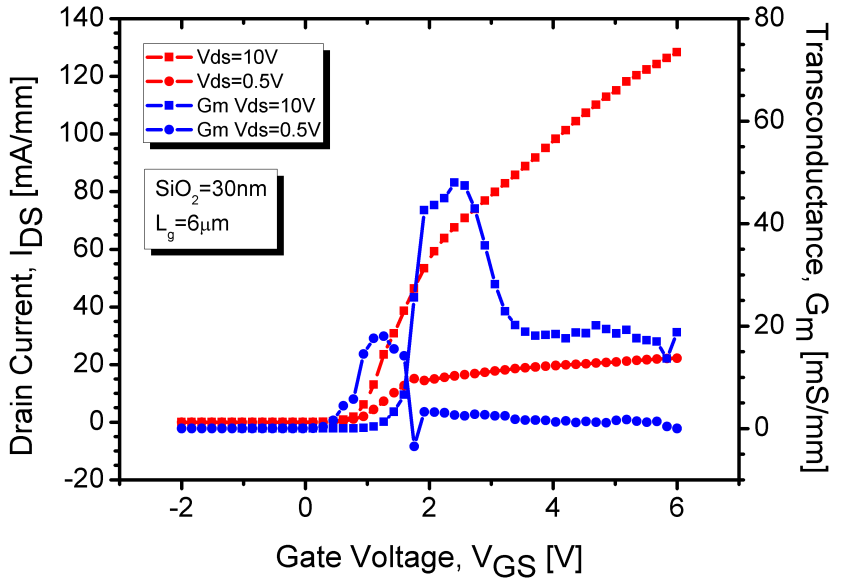



FIGURE 6.20: Transfer characteristics (left y-axis) and transconductance (right y-axis) of an e-mode 6 $\mu$m $\times$ 100 $\mu$m AlGaN/GaN MOS-HEMT with 30 nm thick $SiO_2$ dielectric at drain bias voltages of 0.5 V and 10 V.

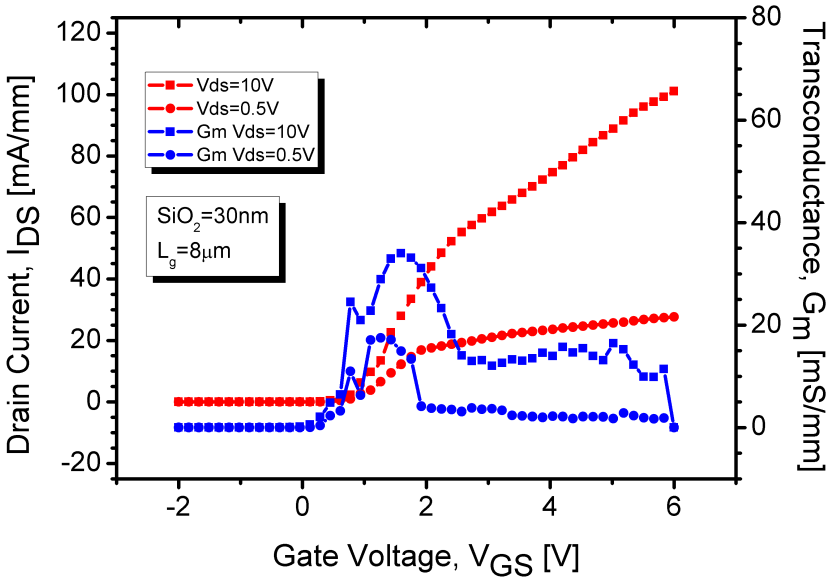



FIGURE 6.21: Transfer characteristics (left y-axis) and transconductance (right y-axis) of an e-mode 8 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 30 nm thick $SiO_2$ dielectric at drain bias voltages of 0.5 V and 10 V.

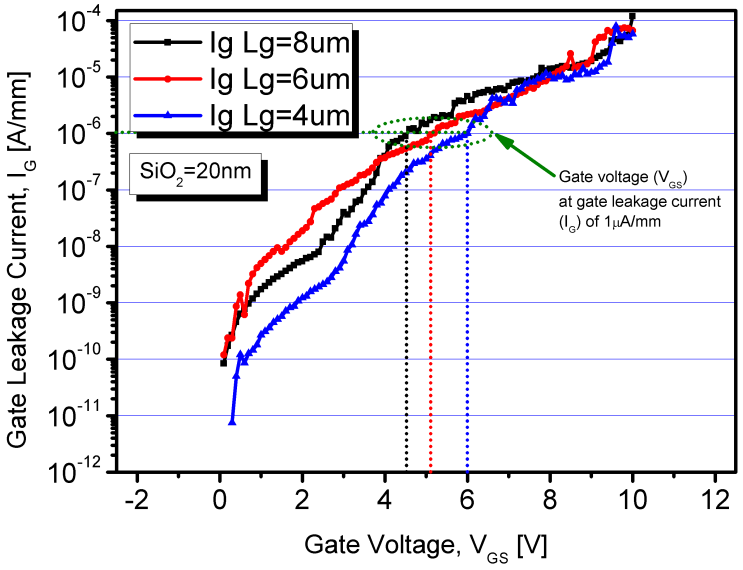



FIGURE 6.22: Gate leakage current as functions of gate bias of e-mode AlGaN/GaN MOS-HEMTs with 20 nm thick $SiO_2$ dielectric.

Single finger devices were also fabricated on GaN epitaxial material grown on a silicon substrate using 20 nm and 30 nm PECVD $SiO_2$ as the gate dielectric. The devices fabricated using a 20 nm $SiO_2$ gate dielectric had gate lengths ($L_g$) of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m and gate width of 100 $\mu$m. They demonstrated threshold voltages of +1 V and +1.5 V, and +1.5 V, respectively, and maximum drain currents of over 240 mA/mm and 180 mA/mm, and 170 mA/mm at a gate voltage ($V_{GS}$) of 6 V, respectively. The devices fabricated using a 30 nm $SiO_2$ gate dielectric had gate lengths of 4 $\mu$m, 6 $\mu$m, and 8 $\mu$m and gate width of 100 $\mu$m and they demonstrated threshold voltages of +0.8 V and maximum drain currents of over 400 mA/mm and 130 mA/mm, and 105 mA/mm at a gate voltage of 6 V, respectively.

The devices on sapphire substrate demonstrated higher drain currents than those on silicon substrate. MBE techniques used to grow the GaN on sapphire make it possible to grow high quality layers due to the slow deposition rate of the technique. On the other hand, silicon has a higher lattice mismatch to GaN (compared to sapphire), and this mismatch causes defects in the material thereby affecting the quality of the material. Also, GaN on silicon material generally tend to suffer from stress related defects due to the difference in coefficient of thermal expansion between GaN and silicon. As these materials are grown by MOCVD under high temperatures of between 800°C and 1000°C, stresses will build up from the difference in the thermal expansion coefficient between silicon and GaN. Therefore, higher dislocation defects in the material used for the devices grown on silicon substrates could have contributed to the lower drain currents exhibited in these devices compared to those grown by MBE on sapphire substrates.

The measured breakdown field of the devices suggest that device breakdown is limited by the dielectric thickness. Despite the low breakdown field of the devices, these devices could be used to replace the low-voltage enhancement-mode silicon transistor used to drive the high-voltage depletion-mode transistor in the hybrid high-voltage cascoded GaN switch configuration.

As the e-mode GaN device described here is very similar in operation to the silicon MOSFET, a short description of the latter is provided in Appendix B for completeness. Also, devices similar to those described in this chapter but employing a $SiN_x$ gate dielectric were fabricated and characterized. The results are presented in Appendix C.

# CHAPTER 7

# CONCLUSION AND FUTURE WORK

## 7.1 Conclusion

Due to its excellent material properties, GaN-based technology is set to become the dominant semiconductor in high-power and high-speed electronics. The research and development aimed at finding engineering solutions to gain the maximum potential from this material is gathering pace, and the work reported in this thesis is one of the many contributions to this goal. This thesis explored a novel high performance enhancement-mode GaN based MOS-HEMT that employs an ultrathin 3 nm $Al_{0.25}Ga_{0.75}N$ barrier layer and relies on an induced 2DEG for operation. As the critical device feature required for normally-off operation, the AlGaN barrier layer, is grown epitaxially, this eliminates the drawbacks experienced with previous techniques such as recess-etching in which the uniformity of the etch and hence that of the threshold voltages is difficult to achieve.

Device fabrication of the new AlGaN/GaN MOS-HEMT is simple, requiring only easily repeatable and reproducible steps. The present device design could be used to realise high current low voltage power devices, operating at say 5 A, required, for instance, for buck converters for mobile phones, tablets, laptop chargers, etc. Although these devices demonstrated high drain currents and high threshold voltages, the breakdown voltages were found to be very low for high power electronics devices. Nonetheless, the proposed design could also be used to replace the low-voltage depletion-mode transistor in the hybrid high-voltage cascoded GaN switch configuration [172]. The $SiO_2$ gate dielectric layers deposited by PECVD have a well known problem of non-uniformity, therefore, it is possible that this might have had an effect on the expected breakdown voltages of the devices. Therefore, an alternative gate dielectric for these devices might

be to incorporate an atomic layer deposited dielectric such as $HfO_2$ or $Al_2O_3$ which is currently being investigated by the group. Not only have these dielectrics shown to improve device performance in the past [173, 174], but they are deposited in such a way that they are uniform across an entire wafer. Further work should be focused on a better understanding of the device operation, characterizing and mitigating the effects of oxide/interface charge and on realizing and characterizing larger gate periphery and high breakdown voltage devices.

## 7.2 Future Work and Research Recommendations

We have demonstrated a novel normally-off AlGaN/GaN HEMT which demonstrates high drain currents. However, further work on process optimization, device characterization, reliability and circuit integration is required in order for these devices to be considered for actual applications.

### 7.2.1 Ohmic Contacts

Using gated TLM structures, contact resistance of around 7 Ωmm and sheet resistances of approximately 557 Ω/□ have been extracted for conventionally processed devices as those reported in this thesis [175]. It is expected that realising quality Ohmic contacts with very low contact resistance will improve the drain currents in the devices, therefore, further work is required to develop metal schemes for both Ohmic and gate contacts, which will enable devices to exhibit $R_{sh}$ of below 500 Ω/□ and $R_c$ of better than 1 Ωmm in order for these devices to match the values currently demonstrated by their conventional normally-on counterparts. Future work should therefore be focused on better understanding and characterizing the gated linear and circular TLM structures.

### 7.2.2 All GaN Cascode Device Configuration

Future work should consider the integration of the normally-off AlGaN/GaN devices in a cascode configuration with a normally-on GaN HEMT in order to provide a high-voltage normally-off mode of operation. Currently, to use a normally-on GaN HEMT in circuit design, it is connected in cascode with a low-voltage silicon MOSFET [176–178]. Figure 7.1 illustrates a GaN HEMT in a cascode structure.

The operating principle of the cascode GaN HEMT is briefly illustrated as follows:

- Because the d-mode GaN HEMT's gate is connected to the source of the e-mode GaN HEMT, the $V_{DS}$ of the e-mode device becomes the negative $V_{GS}$ of the d-mode GaN HEMT, providing the necessary negative voltage bias for turn-off when $V_{GS}$ reaches the threshold voltage required to turn the d-mode device off.

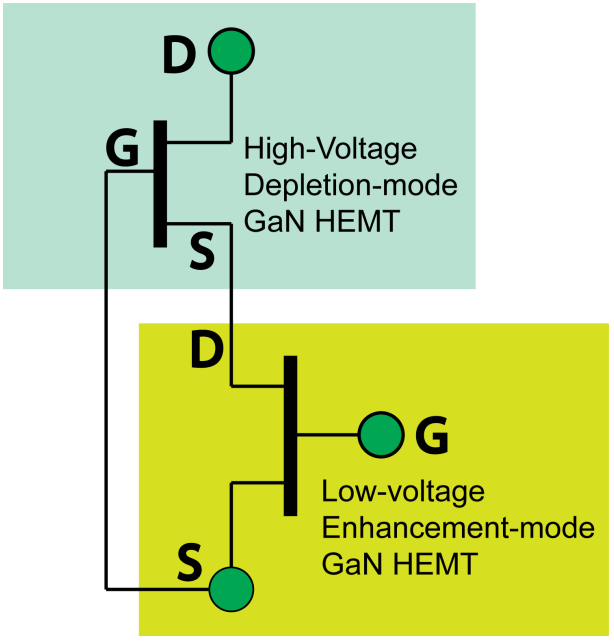



FIGURE 7.1: A cascode configuration featuring a high-voltage normally-on GaN HEMT with a low-voltage normally-off GaN HEMT.

- To turn the cascode structure on, the gate voltage of the e-mode device is increased until it reaches the threshold voltage which in turn lowers the d-mode device's source voltage until it reaches/goes beyond its threshold voltage thereby allowing the d-mode GaN HEMT to conduct current.

In general, controlling the on/off state of the low-voltage enhancement-mode device to control the on/off state of the high-voltage depletion-mode GaN HEMT makes the cascode GaN HEMT behave as a high-voltage enhancement-mode device.

The enhancement-mode device developed in this work seems suitable for cascode configuration with a high-voltage d-mode GaN device as it only requires an operating voltage of under 6 V [179]. Having an all GaN HEMT structure in the cascode configuration can increase the switching speed of the circuit and also enable the circuit to operate in harsh (high temperature) environments where the Si MOSFET might not operate efficiently. Also, the enhancement-mode GaN HEMT will also exhibit a lower on-resistance $R_{on}$ than the normally-off Si MOSFET.

# Appendix A

# FABRICATION PROCESSES

## A.1 Sample Scribing

The wafer is usually coated with a thick resist film (s1818) in order to protect the sample surface from particles generated during scribing. The wafers are cleaved to small rectangular samples measuring approximately $10\,mm \times 10\,mm$.

## A.2 Sample Cleaning

1. Ultrasonic bath in acetone for 10 mins
2. IPA for 5 mins
3. Rinse with reverse osmosis (RO) water for 60 secs

## A.3 Ohmic Lithography Recipe 1

1. Spin S1818 at 4000 rpm for 120 secs
2. Bake on hotplate for 2 mins at 65 °C
3. Develop in (1:1) Microposit : RO water for 60 secs
4. Rinse in RO water for 60 secs
5. Blow-dry with $N_2$ gun
6. Expose with Mask Aligner (MA6) for 5 secs using vacuum contact
7. Develop in (1:1) Microposit : RO water for 75 secs with slight agitation

8. Rinse in RO water for 60 secs
9. Blow-dry with $N_2$ gun
10. Ash in Gala Asher for 3 mins at 40 W

## A.4 Ohmic Metallization Recipe 1

1. De-oxidise in $H_2O$ : HCl using a ratio of 4:1 for 1 min
2. Deposit n-type ohmic contact of 30 nm Ti/ 180 nm Al/ 40 nm Ni/ 100 nm Au using Plassys II or IV
3. Soak in warm acetone (50 °C) for 30 mins for lift-off
4. Agitate solution with a dropper to facilitate lift off and transfer to isopropyl alcohol (IPA)
5. Blow-dry with $N_2$ gun
6. Anneal the sample at 775 °C for 30 secs in nitrogen ambient using a rapid thermal annealer (RTA)

## A.5 Gate Lithography Recipe 1

1. Spin S1805 at 4000 rpm for 120 secs
2. Bake on hotplate for 2 mins at 65 °C
3. Develop in (1:1) Microposit : RO water for 60 secs
4. Rinse in RO water for 60 secs
5. Blow-dry with $N_2$ gun
6. Expose with Mask Aligner (MA6) for 3 secs using vacuum contact
7. Develop in (1:1) Microposit : RO water for 75 secs with slight agitation
8. Rinse in RO water for 60 secs
9. Blow-dry with $N_2$ gun
10. Ash in Gala Asher for 3 mins at 40 W

## A.6 Gate Metallization Recipe 1

1. Deposit 50 nm Ni/ 150 nm Au
2. Soak in warm acetone (50 °C) for 30 mins for lift-off
3. Agitate solution with a dropper to facilitate lift-off and transfer to IPA
4. Blow-dry with $N_2$ gun

## A.7 Ohmic Lithography Recipe 2

1. Spin LOR 10A at 6000 rpm for 30 secs
2. Bake on hotplate at 150 °C for 2 mins
3. Spin S1818 at 4000 rpm for 30 secs
4. Bake on hotplate at 115 °C for 3 mins
5. Expose with Mask Aligner (MA6) for 5 secs using vacuum contact
6. Develop in Microposit MF319 developer for 2 mins 30 secs
7. Rinse in RO water for 60 secs
8. Blow-dry with $N_2$ gun
9. Ash in Gala Asher for 5 mins at 60 W

## A.8 Ohmic Metallization Recipe 2

1. De-oxidise in $H_2O$ : HCl 4:1 for 1 min
2. Rinse in RO water for 60 secs
3. Blow-dry with $N_2$ gun
4. Deposit Ohmic metal contact of 30 nm Ti/ 180 nm Al/ 40 nm Ni/ 100 nm Au using Plassys II or IV
5. Soak in warm acetone (50 °C) for 15 mins for lift-off
6. Agitate solution with a dropper to facilitate lift off and transfer to IPA for 1 min
7. Blow-dry with $N_2$ gun

8. Use the 1165 stripper to remove the LOR 10A in the 50 °C hot water bath for 10 mins
9. Rinse in RO water for 60 secs
10. Blow-dry with $N_2$ gun
11. Anneal sample at 775 °C for 30 secs in nitrogen ambient using a rapid thermal annealer (RTA)

## A.9 Gate Lithography Recipe 2

1. Spin LOR 10A at 6000 rpm for 30 secs
2. Bake on hotplate at 150 °C for 2 mins
3. Spin S1818 at 4000 rpm for 30 secs
4. Bake on hotplate at 115 °C for 3 mins
5. Expose with Mask Aligner (MA6) for 5 secs using vacuum contact
6. Develop in Microposit MF319 developer for 2 mins 30 secs
7. Rinse in RO water for 60 secs
8. Blow-dry with $N_2$ gun
9. Ash in Gala Asher for 5 mins at 60 W

## A.10 Gate Metallization Recipe 2

1. Deposit gate metal contact of 50 nm Ni/ 150 nm Au using Plassys II or IV
2. Soak in warm acetone (50 °C) for 15 mins for lift-off
3. Agitate solution with a dropper to facilitate lift off and transfer to IPA for 1 min
4. Blow-dry with $N_2$ gun
5. Use the 1165 stripper to remove the LOR 10A in the 50 °C hot water bath for 10 mins
6. Rinse in RO Water for 60 secs
7. Blow-dry with $N_2$ gun

## A.11 Bondpad Formation Recipe 2

1. Spin LOR 10A at 6000 rpm for 30 secs
2. Bake on hotplate at 150 °C for 2 mins
3. Spin S1818 at 4000 rpm for 30 secs
4. Bake on hotplate at 115 °C for 3 mins
5. Expose using Mask Aligner (MA6) for 5 secs using vacuum contact
6. Develop in Microposit MF319 developer for 2 mins 30 secs
7. Rinse in RO water for 60 secs
8. Blow-dry with $N_2$ gun
9. Ash in Gala Asher for 5 mins at 60 W

## A.12 Bondpad Metallization Recipe 2

1. Deposit bond pad metal contact of 10 nm Ti/ 150 nm Au
2. Soak in warm acetone (50 °C) for 15 mins for lift-off
3. Agitate solution with a dropper to facilitate lift off and transfer to IPA for 1 min
4. Blow-dry with $N_2$ gun
5. Use the 1165 stripper to remove the LOR 10A in the 50 °C hot water bath for 10 mins
6. Rinse in RO Water for 60 secs
7. Blow-dry with $N_2$

## A.13 E-mode AlGaN/GaN MISHEMT with Silicon Dioxide Gate Insulator Device Fabrication

1. Clean sample
2. Ohmic lithography
3. Ohmic metallization of 30 nm Ti/ 180 nm Al/ 40 nm Ni/ 100 nm Au using Plassys II or IV

4. Ohmic metal annealing at 775 °C for 30 secs in nitrogen ambient using a rapid thermal annealer (RTA)
5. Blanket PECVD dielectric deposition with $SiH_4$, $N_2O$ and $N_2$ gases at flow rates of 7 sccm, 200 sccm and 85 sccm, respectively, at temperature of 300°C, RF power of 15 watts, and pressure of 1 torr using Oxford Instruments PECVD 80 Plus tool
6. Gate lithography
7. Gate metallization of 50 nm Ni/ 150 nm Au using Plassys II or IV
8. Bondpad lithography
9. Silicon dioxide dielectric etch with Oxford Instruments RIE 80 Plus tool using $CHF_3$ and Ar gases at flow rates of 25 sccm and 18 sccm, RF power of 200 watts and a pressure of 20 millitorr at room temperature
10. Bond pad metallization of 10 nm Ti/ 150 nm Au using Plassys II or IV

## A.14 AlGaN/GaN MISHEMT with Silicon Nitride Gate Insulator Device Fabrication

Results from these devices are in Appendix C in Section C.1.

1. Clean sample thoroughly with acetone and IPA
2. Define and expose ohmic contacts
3. Metallise ohmic contacts using Ohmic recipe-1
4. Lift-off
5. Anneal at 775 °C for 30 secs in $N_2$ ambient
6. Blanket PECVD deposition of $SiN_x$ with $SiH_4$, $NH_3$ and $N_2$ gases at flow rates of 10 sccm, 12 sccm and 170 sccm, respectively, at temperature of 300°C, RF power of 20 watts, and pressure of 1 torr using Oxford Instruments PECVD 80 Plus tool
7. Define and expose gate contact
8. Metallise gate contact using gate recipe-1
9. Lift-off
10. Define and expose SiN etch layer

11. Dry etch SiN with the RIE 80+ tool using $CHF_3$ and $O_2$ gases at a flow rate of 50 sccm and 5 sccm, respectively, RF power of 200 watts and a pressure of 30 millitorr at room temperature

12. Clean photoresist from sample by putting in acetone in the 50 °C hotbath for 10 mins

# Appendix B

# SOME SEMICONDUCTOR DEVICE BASICS

A crucial part of making GaN-based devices is the formation of metal/semiconductor contacts, the Ohmic and gate metal contacts. In order to form good quality metal contacts, it is important to understand the physics behind how carriers are transported to and from the metal/semiconductor junctions. Therefore, some semiconductor device basics will be introduced in this section, including metal/semiconductor contacts and the carrier transport mechanisms across metal/semiconductor junctions.

## B.1 Metal/Semiconductor Contacts

Both Ohmic and Schottky (rectifying) contacts are of critical importance with respect to device functionality, performance and long term reliability. A great variety of metal-systems have been proposed for the formation of contacts on GaN-based devices with low-resistances and high thermal and electrical stability, which are discussed in sections 2.5.1 and 2.5.2.

The electrochemical potential (Fermi level) of any two solids in contact must be equal in thermal equilibrium. The difference between the Fermi energy and the vacuum level is known as the work function. The work function of a metal is denoted $\phi_M$ and the work function of a semiconductor is denoted $\phi_S$ as shown in Figure B.1a. Note that a higher work function corresponds lower energy level and vice versa. Therefore, when the metal and semiconductor are placed in contact with each other, electrons will flow from the material with the lower workfunction and higher energy level (semiconductor) to the material with the higher work function and lower energy level(metal) until the Fermi levels become equal, as shown in Figure B.1b. As a result of this, the lower work

function material (semiconductor) becomes slightly more positively charged while the higher workfunction material (metal) becomes more negative. The resulting electrostatic potential is known as the built-in potential ($V_{bi}$). This contact potential will occur between any two solids and is the main cause of the occurrence of rectification in diodes. The built-in field is the cause of band-bending in the semiconductor near the junction [92].

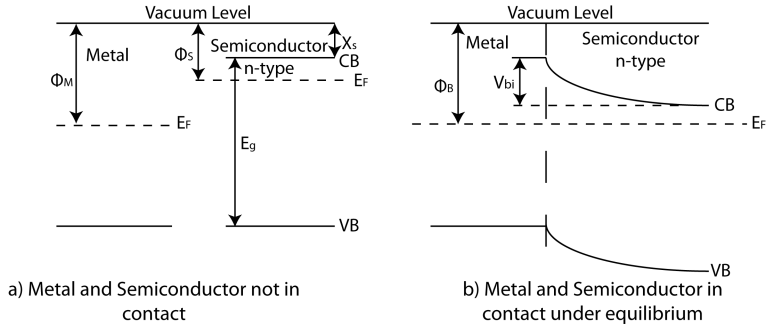



FIGURE B.1: A metal/semiconductor junction

In order to cross the barrier, a carrier in the semiconductor must gain enough energy to move from the Fermi level to the top of the bent conduction band. The needed barrier surmounting energy $\phi_B$ is the sum of the built-in potential and the offset between the Fermi level and the conduction band.

For n-type semiconductors,

$$\phi_B = \phi_M - \chi_S \tag{B.1}$$

where $\chi_S$ is the semiconductor's electron affinity, defined to be the difference between the vacuum level and the conduction band level.

For p-type materials,

$$\phi_B = E_g - (\phi_M - \chi_S) \tag{B.2}$$

The depletion width of a contact is the length scale that the built-in field penetrates into the semiconductor.

$$W = \sqrt{\frac{2\epsilon V_{bi}}{\rho}} \tag{B.3}$$

and

$$X_d = \sqrt{\frac{2k\varepsilon_o\phi_i}{qN_d}} \tag{B.4}$$

W = depletion width
$\epsilon$ = dielectric constant
$V_{bi}$ = built-in potential

$\rho$ = charge density of semiconductor
$N_d$ = doping concentration

From Equation B.4, it can be deduced that increasing the doping concentration will decrease the depletion layer width and vice versa. The barrier height (dependent on electron affinity and built-in field) and barrier thickness (dependent on built-in field, dielectric constant and doping density) can be modified by changing the metal used or changing the doping density of the semiconductor.

## B.2 Carrier Transport Mechanisms across Metal/Semiconductor Junctions

The main conduction mechanisms across metal/semiconductor interfaces/junctions are thermionic emission, field emission and thermionic field emission. The dominant transport mechanism is determined by the barrier height and barrier thickness of the metal/semiconductor junction.

### B.2.1 Thermionic Emission

The current density under thermionic emission ($J_{TE}$) conditions is given by [92, 180]:

$$J_{TE} \propto exp(-\frac{E_{barrier}}{k_B T}) \tag{B.5}$$

$k_B$ = Boltzmann's constant
$J_{TE}$ = Current density under thermionic emission
$E_{barrier}$ = Barrier Energy
$T$ = Absolute temperature

Under zero bias conditions:

$$E_{barrier} = q\phi_b \tag{B.6}$$

$\phi_b$ = Barrier height
$q$ = Charge
and hence under constant temperature the current density is inversely exponentially dependent on the barrier height.

### B.2.2 Field Emission

The tunnelling probability is dependent on the barrier energy and width leading to tunnelling current density ($J_{FE}$)[92].

$$J_{FE} \propto exp(\frac{E_{barrier}}{E_{00}}) \tag{B.7}$$

where $E_{00}$ is the tunnelling parameter:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_D}{\epsilon_s m_e}} \tag{B.8}$$

$m_e$ = Mass of electron
$\hbar$ = Reduced Planck's constant
$N_D$ = Doping density

From Equation B.8, it can be seen that tunnelling current depends directly on doping density. Since barrier width varies with dopant density, the tunnelling probability increases as the barrier thins. Annealing of the ohmic contacts in GaN devices creates a lot of nitrogen vacancies under the contact region and due to the presence of excessive carriers, the tunnelling probability/current increases, resulting in low resistance. In this, current will flow in equal magnitude from metal to semiconductor and vice versa under both forward and reverse bias.

### B.2.3 Thermionic Field Emission

Thermionic field emission (TFE) occurs where carriers have insufficient energy to cross the barrier thermally, and the barrier is too wide for direct tunnelling. In this case, the electrons to combine both thermionic and field emission (tunnelling) to crossover the barrier. Electrons with a degree of thermal excitation, however, may be able to tunnel through the barrier, since its width decreases with increasing energy, which results in the flow of thermionic field current density ($J_{TFE}$) and is given by:

$$J_{TFE} \propto exp(\frac{E_{barrier}}{E_{00}coth(\frac{E_{00}}{k_B T})}) \tag{B.9}$$

Thermionic field emission is therefore expected to increase with increasing temperature and is also strongly dependent on barrier thickness and dopant density.

## B.3 Metal Insulator Semiconductor Field Effect Transistor (MISFET)

Field Effect Transistors (FETs) employing a gate dielectric are generally called Metal Insulator-Semiconductor (MIS) FETs or MISFETs. The most common MISFET is the silicon Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) so the name MOSFET is used much more frequently than MISFET. The basic principle of the MOSFET is that the source-to-drain current ($I_{SD}$) is controlled by the gate voltage, or better, by the gate to source electric field. The electric field induces charge (field effect) at the semiconductor-oxide interface.

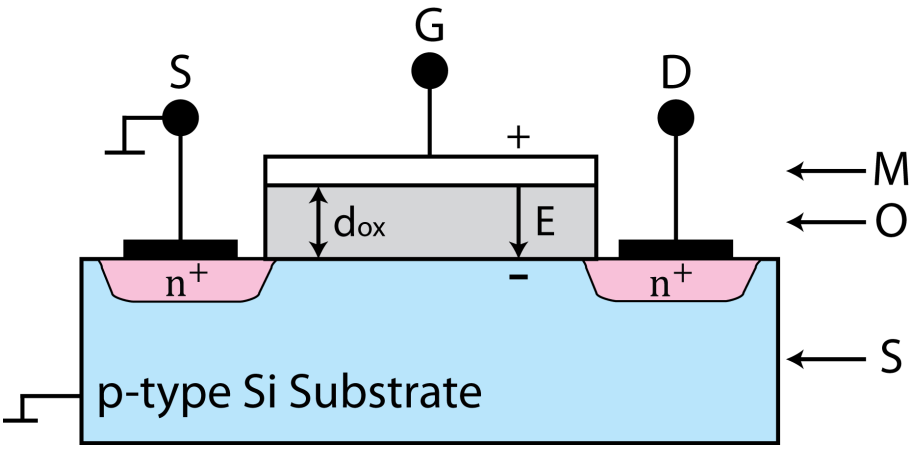



FIGURE B.2: Structure of an n-channel silicon MOSFET.

The understanding of how an enhancement-mode MOSFET operates is helpful to the understanding of the operation of the normally-off gate overlapping HEMTs fabricated in this project. The similarities of a MOSFET and the gate overlap HEMT lie in the nominal overlap of the source and drain by the gate metal and also the gate dielectric used in the devices.

The cross-section physical structure of an enhancement-mode n-type metal-oxide semiconductor (NMOS)-Transistor is shown in Figure B.2. The transistor is fabricated on a p-type silicon substrate. The transistor has two heavily doped n-type regions. A thin ($20 - 100\,\text{nm}$) layer of silicon dioxide ($SiO_2$), which is an excellent electrical insulator, is grown on the surface of the substrate, covering the area between the source and drain regions. Metal is deposited on top of the oxide layer to form the gate electrode. Metal contacts are then made to the source and the drain.

### B.3.1 Operation of a MOSFET with No Gate Voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between the drain and source (pn junctions). These back-to-back diodes prevent current conduction from the drain to source when a voltage $V_{DS}$ is applied. The path between the drain and source has very high resistance (in the order of $10^{12}\,\Omega$)

### B.3.2 Creating a Channel for Current Flow

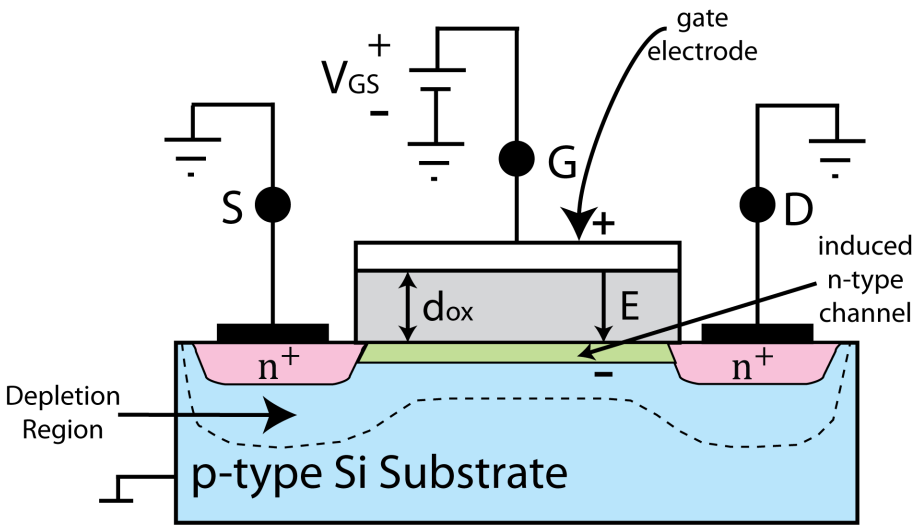



FIGURE B.3: A MOSFET with a channel for current flow.

Consider the source and drain grounded and positive voltage is applied to the gate as shown in Figure B.3. Since the source is grounded, $V_{GS}$ appears in effect between the gate and source. The positive voltage on the gate causes, in the first instance, the free holes (positively charged) to be repelled from the region under the gate (channel region). These holes are pushed downward into the substrate, leaving behind a carrier-free region, the depletion region which is populated by the bound negative charge associated with the acceptor atoms. The positive gate voltage also attracts electrons from the $n^+$ source and drain regions into the channel region. When a sufficient number of electrons accumulate near the surface under the gate, an n-type region is created, connecting the source and drain regions. Now if a voltage is applied between the drain and source, current flows through this induced n region, carried by the mobile electrons. The value of $V_{GS}$ at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage ($V_{th}$) and is usually between 1-3 V for silicon MOSFETs.

The gate metal and body (p-type silicon substrate) of the MOSFET can be considered to form a parallel-plate capacitor dielectric. The positive gate voltage causes positive charge

to accumulate on the top plate of the capacitor (gate electrode). The corresponding negative charge on the bottom plate is formed by the electrons in the induced channel. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus, it determines the channel conductivity and,in turn, the current that will flow through the channel when a voltage $V_{DS}$ is applied.

### B.3.3 Operation at Small Drain-Source Voltage

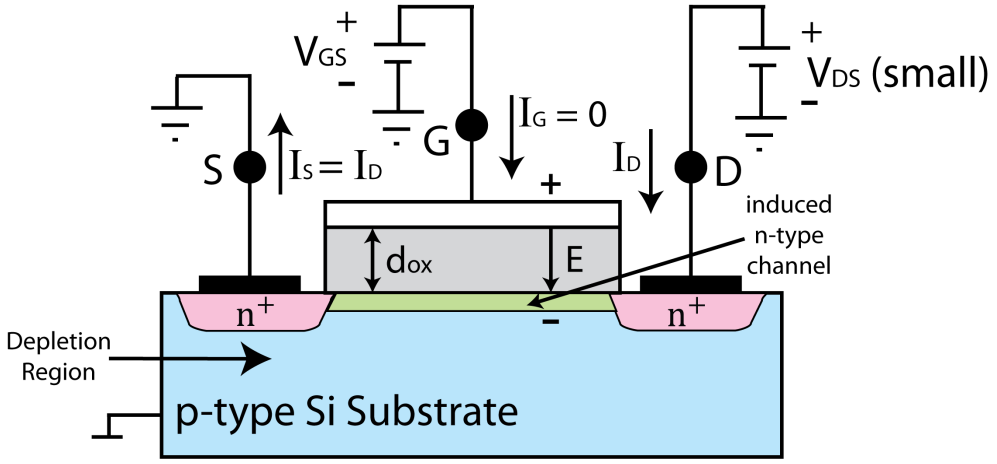



FIGURE B.4: A MOSFET with small drain-source voltage applied.

Having induced a channel, we now apply a positive voltage $V_{DS}$ between the drain and source as shown in Figure B.4. First, consider the case where $V_{DS}$ is small (0.1 or 0.2 V). The voltage $V_{DS}$ causes a current $I_D$ to flow through the induced channel. Current is carried by free electrons travelling from source to drain. The magnitude of $I_D$ depends on the magnitude of $V_{GS}$. For $V_{GS} = V_{th}$, the channel is just induced and the current conducted is still negligibly small. As $V_{GS}$ exceeds $V_{th}$, more electrons are attracted into the channel. The result is a channel of increased conductance or reduced resistance. The conductance of the channel is proportional to the excess gate voltage $(V_{GS} - V_{th})$, also known as the effective voltage. It follows that the current $I_D$ will be proportional to $V_{GS} - V_{th}$ and to the voltage $V_{DS}$ that causes $I_D$ to flow. The current that leaves the source terminal $(I_S)$ is equal to the current that enters the drain terminal $(I_D)$, and the current $(I_G = 0)$.

### B.3.4 Operation at Higher Drain-Source Voltage

Let $V_{GS}$ be held constant at a value greater than $V_{th}$. $V_{DS}$ appears as a voltage drop across the length of the channel. That is, as we travel along the channel from source to drain, the voltage(measured relative to the source) increases from 0 to $V_{DS}$. Thus the voltage between D and points along the channel decreases from $V_{GS}$ at the source end

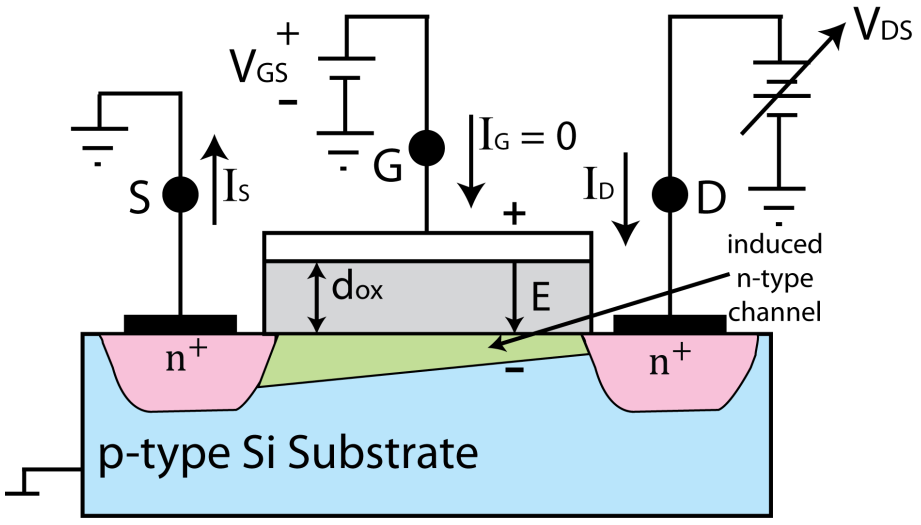



FIGURE B.5: A MOSFET with high drain-source voltage applied.

to $V_{GS} - V_{DS}$ at the drain end. Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth; rather, the channel will take a tapered form as shown in Figure B.5, being deepest at the source end and shallowest at the drain end. As $V_{DS}$ is increased, the channel becomes more tapered and its resistance increases correspondingly. Thus the $I_D - V_{DS}$ curve does not continue as a straight line but bends as shown in Figure B.6. Eventually, when $V_{DS}$ is increased to the value that reduces the voltage between the gate and channel at the drain end to $V_{th}$, i.e., $V_{GS} - V_{DS} = 0$ or $V_{DS} = V_{GS} - V_{th}$, the channel depth at the drain end decreases to almost zero, and the channel is said to be pinched off. Increasing $V_{DS}$ beyond this value has little effect (theoretically no effect) on the channel shape, and the current through the channel remains constant at the value reached for $V_{DS} = V_{GS} - V_{th}$. The drain current thus saturates at this value, and the MOSFET is said to have entered the saturation region of operation. The voltage $V_{DS}$ at which saturation occurs is $V_{DSsat}$.

$$V_{DSsat} = V_{GS} - V_{th} \tag{B.10}$$

For every value of $V_{GS} \geq V_{th}$, there is a corresponding value of $V_{DSsat}$. The region of the $I_D$-$V_{DS}$ characteristic obtained for $V_{DS} < V_{DSsat}$ is called the triode region.

## B.4 Summary

The theory of metal/semiconductor contacts and the carrier transport mechanisms across these metal/semiconductor junctions have been described in this Appendix. In addition, the principle of operation of the common silicon metal-oxide-semiconductor

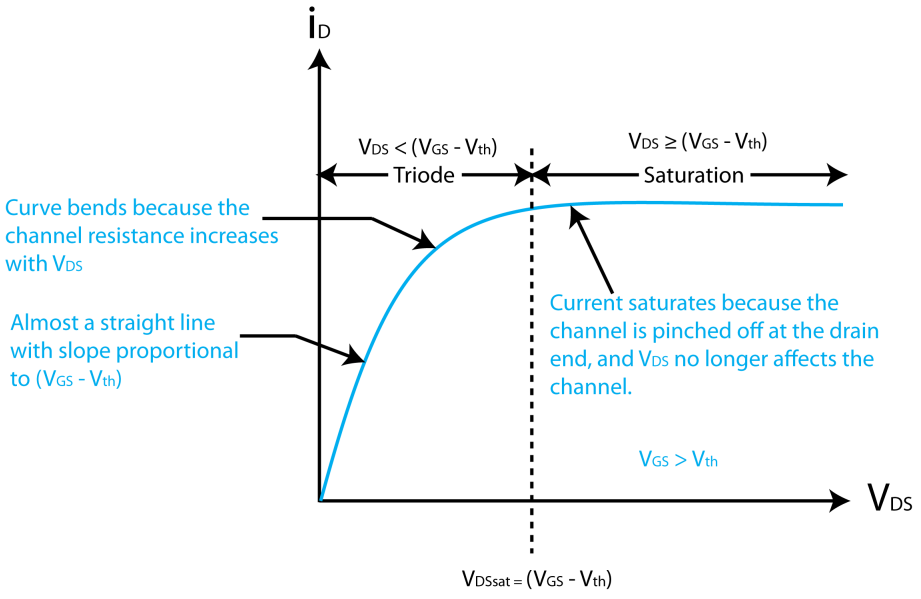



FIGURE B.6: IV Characteristic of an enhancement-type NMOS transistor.

field-effect transistors was presented since it is very similar to the proposed normally-off AlGaN/GaN MOSHEMTs.

# Appendix C

# SILICON NITRIDE GATE DIELECTRIC MISHEMTs AND INTERFACE TRAPS

Results of the gate overlap devices fabricated which employed silicon nitride ($SiN_x$) gate dilectric (refracrtive index of around 1.97) are presented here. This appendix also presents initial results for work being carried out on metal-oxide-semiconductor capacitor (MOSCAP) structures in order to understand the effect of interface trapped charges in the normally-off GaN devices presented in this thesis.

## C.1 AlGaN/GaN MISHEMT with SiN Gate Insulator

The same epitaxial material used for e-mode GaN devices was used for devices with a $SiN_x$ gate dielectric. Figure C.1shows the cross-section of the device structure of the MISHEMT with a silicon nitride gate insulator/dielectric.

The device structure consists of a sapphire substrate of approximately 350 $\mu$m thickness, a 2-5 nm thick aluminium nitride (AlN) nucleation layer, a 3 $\mu$m GaN channel, and a 3 nm $Al_{0.25}Ga_{0.75}N$ barrier layer. The epi-structure was grown using molecular beam epitaxy (MBE) by SVT Assiciates, USA. The device consists of source and drain Ohmic contacts nominally overlapped by the gate contact and employs a gate dielectric. The $SiN_x$ dielectric underneath the gate is 20 nm thick. Figure C.2 shows that the devices with gate length of 4 $\mu m$ and gate width of 100 $\mu$m have a maximum drain current ($I_{DSMAX}$) of approximately 175 mA/mm. The devices were measured at gate voltages ($V_{GS}$) of between -3 and 4 V and drain voltages ($V_{DS}$) of between 0 and 10 V. Figure C.3 shows the transfer characteristics of the devices. It is illustrated that the threshold voltage

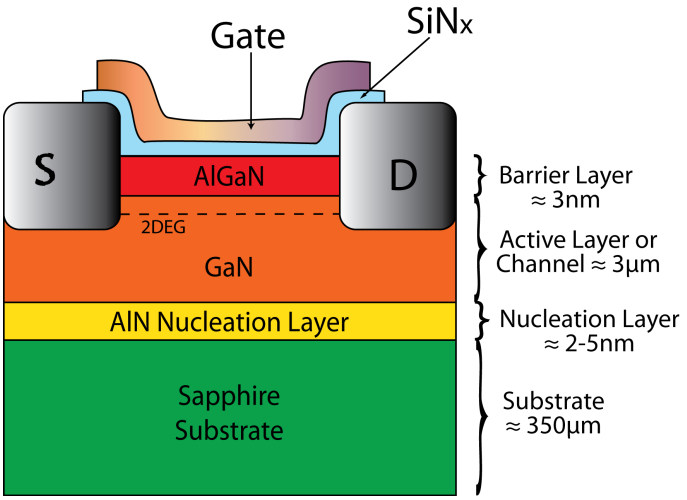



FIGURE C.1: MISHEMT with $SiN_x$ gate insulator.

($V_{th}$) of the devices is approximately -3 V which makes them normally-on transistors instead of the desired normally-off transistors.

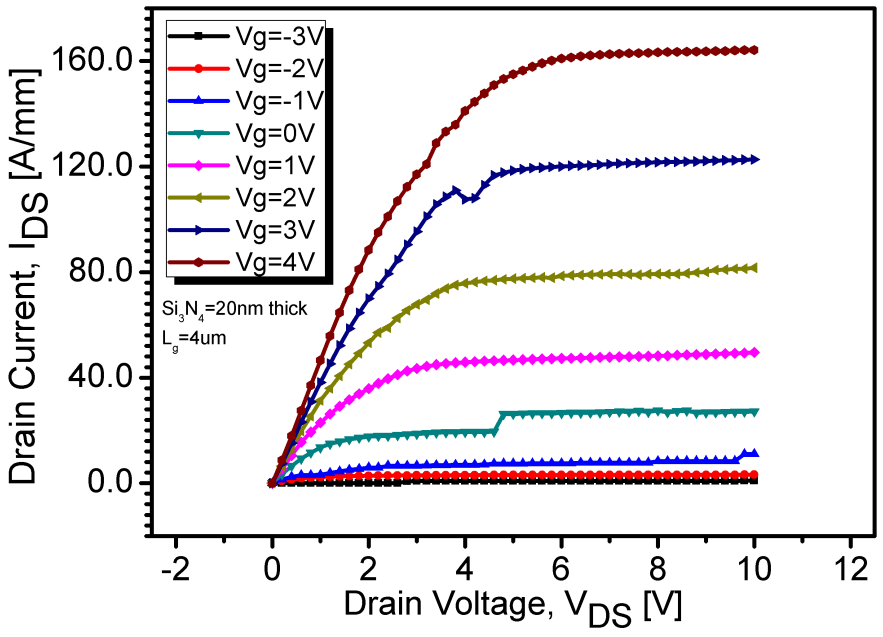



FIGURE C.2: Output characteristics of a 3 nm thick barrier 4 $\mu$m × 100 $\mu$m AlGaN/-GaN MOS-HEMT with 20 nm thick SiN dielectric.

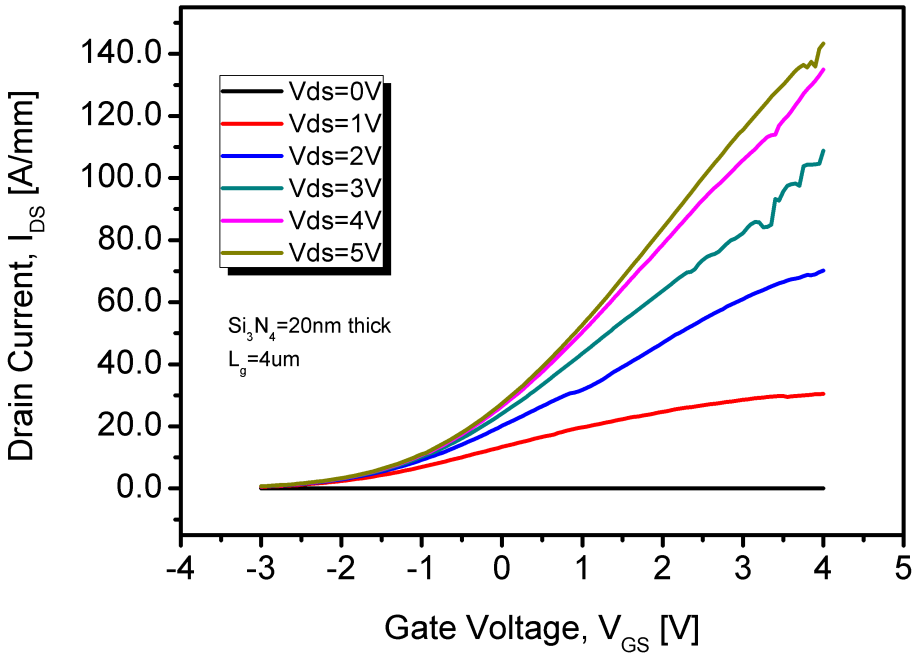



FIGURE C.3: Transfer characteristics and $G_m$ of a 3 nm thick barrier 4 $\mu$m × 100 $\mu$m AlGaN/GaN MOS-HEMT with 20 nm thick SiN dielectric.

## C.2 Metal-Oxide-Semiconductor Capacitors

Forming a stable interface with a semiconductor is a very important requirement for a gate dielectric material. The dielectric must be able to meet this requirement even after being put through the high temperatures that the wafer is exposed to during fabrication process and its density of interface states (traps) must be low. The former condition is met by many dielectrics, but the challenge is meeting the latter condition, which is a low density of interface states (traps). Interface states exist in a semiconductor material for many reasons, for instance, the energy band diagram of the ideal structure of a crystal consists of a conduction band and valence band separated by a band gap. The existence of defects or foreign atoms introduces discrete energy levels in the band gap [181]. For example, in the crystalline structure of any semiconductor, each atom requires a number of electrons from neighbouring atoms to be saturated at the surface of the semiconductor. When some of these bonds are missing due to the broken bonds, traps can be formed. Metal-oxide-semiconductor capacitor (MOSCAP) structures, also known as MOS diodes form the heart of any metal-oxide-semiconductor field-effect transistor (MOSFET), and can be used to determine the trap density at the interface of the dielectric and the semiconductor by performing capacitance-voltage (CV) characterization. Interface trapped charges are positive or negative charges, due to structural defects, oxidation-induced

defects, metal impurities, or other defects caused by radiation or similar bond breaking processes (e.g., hot electrons). A typical MOSCAP is similar to a MOSFET structure but instead of a source and drain it contains one Ohmic contact. It mainly consists of a dielectric layer (oxide) placed between a metal gate and a semiconductor layer. Realising a III-V MOSFET with an effect channel is affected by the type of dielectric used. For instance the relative permittivity of the dielectric must be high enough to minimise the gate leakage current and allow for device scaling.

In work co-supervised by the author of this thesis to further understand the effect of interface trapped charges the GaN MOS-HEMTs, MOSCAP structures were fabricated with 20 nm thick $SiO_2$ gate dielectric and characterized with three variations of process flows [182]. The first sample (sample 1) was realized using the standard process modules derived from the normally-off devices discussed in this thesis. The second sample (sample 2) also went through the standard e-mode fabrication processes but the dielectric surface was cleaned before and after it was deposited using 50 °C warm acetone for 5 minutes and isopropanol for 1 minute. The third sample (sample 3) employed a dual layer $SiO_2$ gate dielectric. The first 10 nm thick dielectric layer was annealed at 900 °C for 30 minutes in nitrogen ambient, then the deposited dielectric surface was cleaned using 50 °C warm acetone for 5 minutes then isopropanol for 1 minute. This was followed by the source and drain Ohmic metallization, deposition of the second 10 nm thick $SiO_2$ gate dielectric layer, gate metal formation, then dielectric etch and bondpad formation.

The graphs obtained from CV measurements are illustrated in Figure C.4, C.5 , and C.6 for capacitors with a diameter size of 250 $\mu$m. The devices show hysteresis due to trap states charging and discharging during the CV sweep. Sample 2 demonstrated a narrower shift between the forward and reverse sweep than sample 1, possibly due to surface cleaning with acetone and isopropanol. The surface donor-like traps are considered to be the main origin of the 2DEG channel, therefore surface cleaning is likely to have a reasonable effect on the devices behaviour as it is believed to get rid of unwanted surface traps. However, the CV for sample 3 demonstrated identical graphs with no shift between forward and reverse sweeping, which means there are no interface traps or trap states occupied in energy levels that can respond to CV sweeping. This is possibly due to the 900 °C dielectric annealing.

In Sample 1 and Sample 2, the forward C-V graph and the reverse C-V graph are not identical, but instead are shifted from each other. This phenomenon is called hysteresis, meaning that the C-V curve in the reverse sweep does not exactly follow the C-V curve in the forward sweep for the same value of bias voltage. This is because of the existence of interface traps at the semiconductor/dielectric interface. However, in Sample 3, the forward and reverse C-V graphs are identical, which is an indication of a high quality

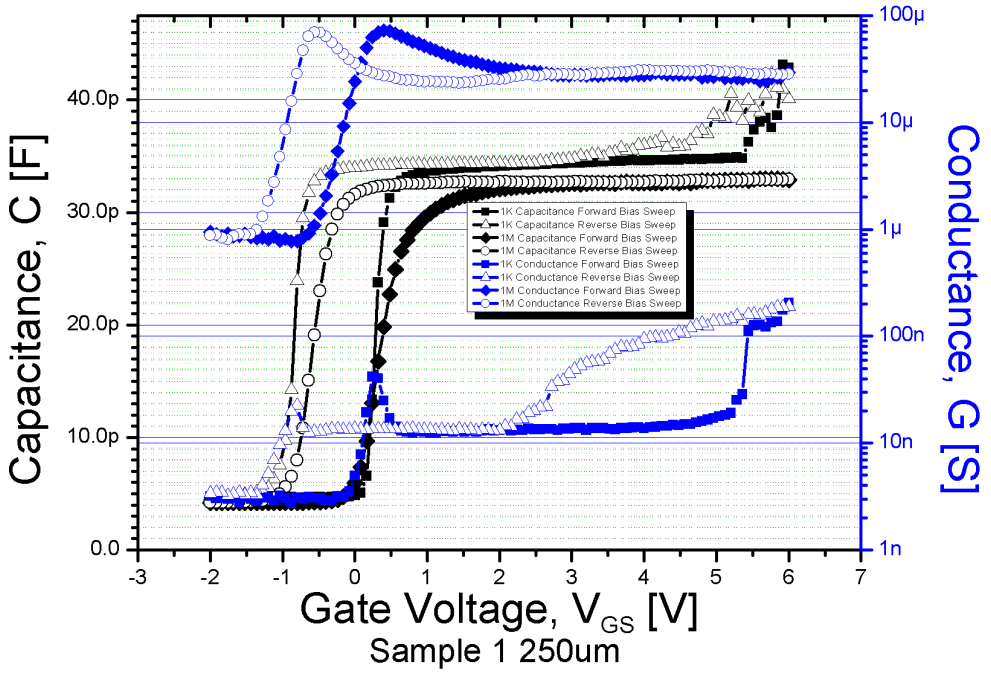



FIGURE C.4: C-V graph of 250 $\mu$m MOSCAP structure with 20 nm $SiO_2$ gate dielectric without surface treatment prior to dielectric deposition (Sample 1).

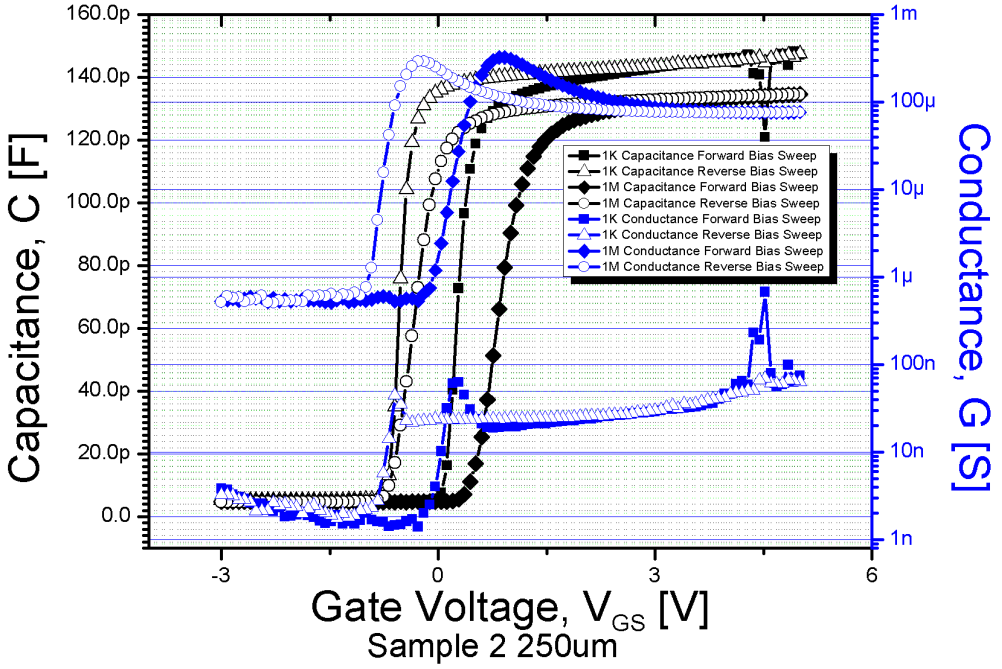



FIGURE C.5: C-V graph of 250 $\mu$m MOSCAP structure with 20 nm $SiO_2$ gate dielectric with surface treatment prior to dielectric deposition (Sample 2).

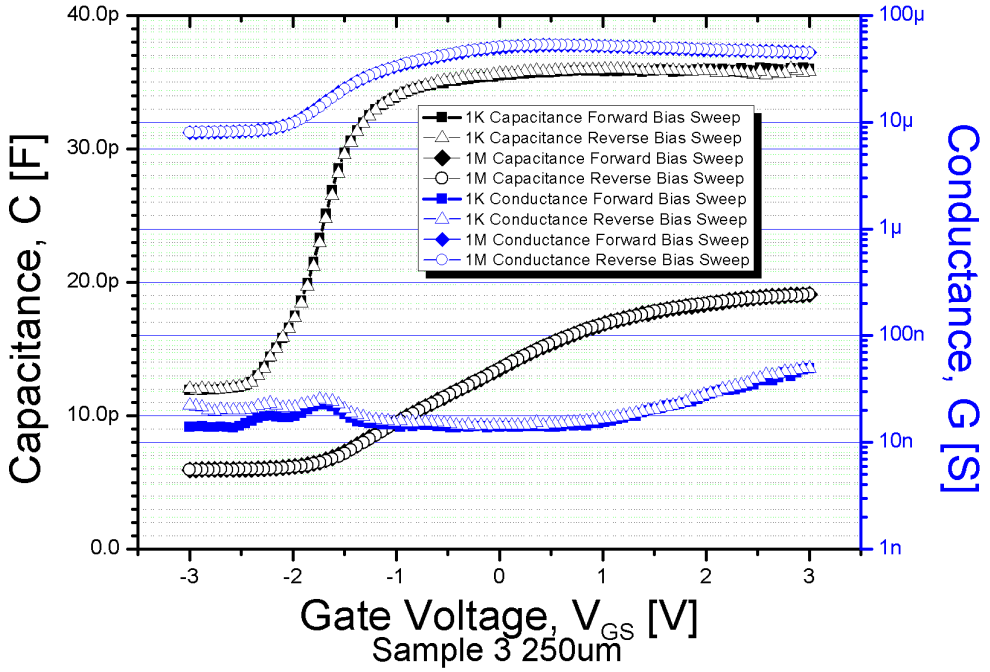



FIGURE C.6: C-V graph of 250 $\mu$m MOSCAP structure with 20 nm $SiO_2$ gate dielectric with surface treatment prior to dielectric deposition and with dielectric treatment (annealing at 900 °C for 30 minutes in nitrogen ambient)(Sample 3).

dielectric-semiconductor interface. In the 1 KHz C-V graphs, in both the forward and reverse sweep, the transition from inversion to accumulation was sharp, another indicator of a good quality interface. Additionally, the hysteresis window between the forward and reverse sweeps was wider in Sample 1 than in Sample 2. Section 4.4 of this chapter goes into greater detail concerning the behaviour of C-V graphs.

From CV graphs for Sample 1 and Sample 2, it can be seen that there is a shift between the forward and reverse sweep, a phenomenon known as hysteresis, which is mainly due to charge and discharge of the existing traps. The response of the traps to the C-V sweep depends on the time for electron emission rate. Based on the Shockley-Read-Hall statistics (SRH) the energy level of the deepest trap state that can respond during CV sweeping can be estimated by Equation [181, 183]:

$$E_{Tm} = kT \ln(\sigma N_C v t_{meas}) \tag{C.1}$$

where, where $k$ is the Boltzmann constant,$T$ is the absolute temperature, $\sigma$ is the capture cross section, $v$ is the thermal velocity, $N_c$ is the effective density of states in the

conduction band, and $t_{meas}$ is CV sweeping time. Therefore, only traps with an energy level above $E_{Tm}$ can respond. All other traps are located in the frozen zone.

From the CV graphs, the hysteresis in Sample 2 is generally narrower than in Sample 1, which may be because the density of surface traps in the former is lower than in the latter. This reflects the importance of the surface treatment on the performance of the device. In Sample 3 not all the devices exhibit good performance, but encouragingly the forward and the reverse CV sweeps are identical and there was no hysteresis. Sample 3 was treated differently to the other samples with the dielectric layer deposited in two layers. The first dielectric layer was 10 nm thick and was deposited before Ohmic contact formation. After the first layer of dielectric deposition, the sample was annealed at 900 °C in N2 ambient for 30 minutes, which possibly assisted the removal of interface traps. The second 10 nm thick dielectric layer was deposited after the Ohmic contact metallisation, therefore the dielectric thickness over the sample surface was not uniform. The thickness of the dielectric layer gate and Ohmic overlap region is only 10 nm, while the thickness in other part become 20nm, the CV measurements for Sample 3 were performed in voltage sweeping range $V_{GS}$ from -3 V to +3 V. The fabrication process in Sample 3 might lead to good e-mode AlGaN/GaN HEMTs, free of traps, however dividing the blanket dielectric into two equal layers of 10 nm probably reduces the break down voltage of the transistor. The first layer should be thinner than the second layer, in order to increase the thickness of the dielectric between the overlapped region between the Ohmic ring in MOS-capacitors (source, drain in transistors) and the gate, which should increase the capability of devices to stand higher voltages before break down. Further work is required to investigate the effect of interface trap charges on the reliability of the normally-off devices.

## C.3 Summary

Details of an AlGaN/GaN metal-insulator-semiconductor high-electron mobility transistor (MISHEMT) employing a silicon nitride $SiN_x$ gate dielectric have been presented. These results demonstrate that normally-on mode of operation is achieved on the same material structure as the normally-off devices by changing the gate dielectric material used to fabricate the devices. It is believed that a different gate dielectric, for example, $SiO_2$ depletes the 2DEG channel at the AlGaN/GaN interface of electrons required to conduct current when the device has no or low gate voltage applied to the gate due to the lower positive charge present in such a dielectric. A summary of MOSCAP structures being fabricated by the group to investigate the effect of interface trap charges on the reliability of the normally-off devices was also presented.

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