Development of Si/SiGe Technology for Microwave Integrated Circuits

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Summary

A complete fabrication process has been developed for the realisation of Si/SiGe microwave integrated circuits (SIMICs). Using the process, a number of active and passive elements for microwave circuits have been demonstrated including

1. Metal gate p-SiGe MOSFETs [1].
2. Low loss transmission lines on CMOS grade silicon [2].
3. High quality spiral inductors on CMOS grade silicon [2].
4. High performance metal gate strained silicon n-MOSFETs [3].

Single stage amplifiers have been designed based on the technology developed in this work [3].

The MOSFETs have good DC performance. Strained SiGe p-channel MOSFETs with 1 μm gate length have an extrinsic transconductance of 36 mS/mm. Strained silicon n-channel MOSFETs with 0.3 μm gate length have extrinsic transconductance of 230 mS/mm. The RF performance of a metal gate 0.3 μm gate length strained silicon MOSFET is measured, with cut off frequency and maximum frequency of oscillation of 20 GHz and 21 GHz respectively. Coplanar waveguide transmission lines of 50 Ohm characteristic impedance, fabricated using spin on dielectrics on a CMOS grade silicon substrate, have losses less than 0.5 dB/mm up to 60 GHz. Spiral inductors fabricated on the low loss dielectric have $Q > 15$. Using the passive and active element library developed, single stage amplifiers were designed with gain of 12 dB at 3 GHz or 7.5 dB at 6 GHz.

The device layer structures were designed using a simple 1D Poisson solver. The p-channel device used a concentration graded SiGe channel to obtain high mobility and carrier concentration. The n-channel RF device with a strained silicon channel incorporates a metal gate technology that is directly responsible for the high values of f_{max} achieved.

The spiral inductors and coplanar waveguides are fabricated using a spin on dielectric process to separate them from the lossy silicon substrate. The same technology is used to reduce the parasitic capacitance of device contact pads.

The engineering conclusion of this work is that SIMICs, for applications in the frequency range 1 to 10 GHz, can be made with the current passive and active element library at the University of Glasgow. Further improvement in both passive and active element performance to increase the frequency is set out in future work.

From a practical viewpoint a process is now in place that will underpin the University of Glasgow's Si / SiGe SIMIC projects in the future.

[1] G.Ternent, A.Asenov, I.G.Thayne, D.S.MacIntyre, S.Thoms, C.D.W.Wilkinson, E.H.C.Parker, A.M.Gundlach "SiGe p-Channel MOSFETs with Tungsten Gate" IEE Electronics Letters, Vol. 35, No. 5, pp.430-431, 1999.

[2] G.Ternent, S.Ferguson, Z.Borsosfoldi, K.Elgaid, T.Lodhi , D.Edgar, C.D.W.Wilkinson, I.G.Thayne, "Coplanar waveguide Transmission Lines and High Q Inductors on CMOS Grade Silicon using Photoresist and Polyimide" IEE Electronics Letters, Vol. 35, No. 22, pp.1957-1958, 1999.

[3] G.Ternent, D.L.Edgar. H.McLelland, F.Williamson, S.Ferguson, S.Kaya, K.Fobelets, J.Hampson, C.D.W.Wilkinson, I.G.Thayne "Single Stage Amplifiers on a CMOS Grade Silicon Substrate using a Polymer Interlayer Dielectric with Strained Silicon MOSFETs" Accepted for presentation at the 2000 Asia-Pacific Microwave Conference.

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Isobel my partner has only known me during the thesis writing period which has been somewhat extended, I hope that she likes the new relaxed Gary when its all done

Of course it would not be my work if I did not mention my four legged friends who provide so much fun and relaxation at weekends, Amber (Horse) Wolfie (Horse). And to Family my father and mother, George and Margaret, sisters Lorraine Diane and Susan and Clyde and Lucy the dogs of course.

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Chapter 1

Introduction

1.1 Semiconductor Technology

Field effect transistors are used in high-speed digital and analogue circuit applications. The silicon metal oxide semiconductor field effect transistor (MOSFET) has been at the heart of the digital revolution of the past 20 years. The MOSFET is the key device in microprocessors and is used in memory chips. Complementary MOS (CMOS) logic has low power consumption which is a major advantage in large digital systems.

GaAs based high electron mobility transistors (HEMTs) or modulation doped transistors (MODFETs), as they will be called here, are widely used in microwave frequency applications such as mobile phones, and for military use. The carrier transport properties compared to silicon and the possibility of a semi insulating substrate make GaAs based devices and circuits more suitable for microwave frequency applications. However GaAs based device and circuit fabrication is very immature compared to those on silicon substrates.

The mobile phone has brought microwave technology to the masses but there is so much more potential if silicon based microwave devices and circuits could become possible. Currently an RF circuit on a GaAs chip is connected to a digital signal processing (DSP) circuit on a silicon chip via a bonding process. Integration of the RF front end with the DSP on a single silicon chip will provide lower cost, power, size and easier manufacturability.

Silicon devices can now be fabricated with cut off frequencies in excess of 100 GHz. The use of the silicon-germanium alloy is expected to further improve the high speed performance of silicon based devices. With the advantages of a mature fabrication technology, silicon is a serious option for microwave designers.

1.2 Aims of the Work

The aim of this work is to draw upon the experience and expertise of one of the world's most successful III–V device fabrication centres in order to develop fabrication processes to investigate the possibility of making microwave circuits on silicon substrates.

Since SiGe layer structures on silicon substrates can lead to improved device performance, the devices designed and fabricated in this work are SiGe devices. Both p and n-channel devices are fabricated incorporating strained Si and SiGe layers for improved carrier transport properties. In the case of a standard silicon MOSFET process flow, useful RF performance can be achieved by

(a) Incorporating metal gates for optimal RF gain and noise performance.
(b) Producing low-loss, high Q passive elements for transmission lines and lumped element matching.

In this work, metal gate Si / SiGe MOSFET technologies, low loss transmission lines and high Q passive elements have been developed on 1-10 Ω-cm CMOS grade silicon substrates to enable the design of single stage monolithic amplifiers.

1.3 Synopsis of the Thesis

In chapter 2, field effect transistors are considered. The operation of the MOSFET is described and the important DC figure of merit transconductance is derived. Carrier transport phenomena and parasitic resistances which effect transconductance are considered. The use of epitaxially grown semiconductor layers of III-V material to produce a device with high transconductance is considered. A comparison is made between the DC and RF performance of Si and III-V based FETs. The chapter concludes with a description of the typical fabrication processes used to make Si and GaAs FETs.

In chapter 3 the alloy silicon / germanium is introduced along with some basic epitaxial growth considerations. The carrier transport properties associated with strained layers are discussed. Simple SiGe / Si heterostructures are described showing how they can improve the performance of silicon based MOSFETs. State of the art results for SiGe FETs are discussed.

In chapter 4 a 1D Poisson solver is discussed and is used to simulate the layer structures used in this work. Ion implantation conditions for the source and drain contacts are simulated using a simple approximation. The choice of gate metals is discussed.

In chapter 5 the fabrication processes developed in this work for p and n-channel metal gate Si / SiGe MOSFETs are described. The processes are described in turn and following each process description, the measured DC results are presented.

In chapter 6 the system used to measure the RF properties of devices is shown. The measured RF performance of the n-channel strained Si MOSFETs fabricated in this work is presented.

Chapter 7 begins with some theory on microwave transmission lines and passive elements. The process developed in this work to produce low loss transmission lines and high Q inductors on CMOS grade silicon substrates is described. The system used to measure the RF properties of the transmission lines and inductors is shown. Results obtained from the measurements are presented and compared with other works.

The thesis is concluded by chapter 8, which considers ongoing and future work including the design and fabrication of a single stage amplifier.

Appendix 1 lists the publications resulting from this work.

Chapter 2

Microwave Field Effect Transistors

2.1 Introduction and List of Symbols

Since this work is concerned with the application of silicon based field effect transistors (FETs) at microwave frequencies, the field effect transistor and its electrical performance is described. The important figures of merit that apply to both DC and RF applications are introduced and discussed. The important transport properties of semiconductor materials are discussed and compared. Recently reported figures of merit on the RF performance of the metal oxide semiconductor field effect transistor (MOSFET) and the modulation doped field effect transistor (MODFET) are compared. Finally a typical MOSFET fabrication process is compared with that of a typical GaAs MODFET process.

List of Symbols

C_{gd} gate-drain capacitance

C_{gs} gate-source capacitance

C_o gate oxide capacitance

C_{gp} gate pad parasitic capacitance

C_{dp} drain pad parasitic capacitance

C_{sd} source drain capacitance

d Dielectric thickness

E Electric field

ε_r Relative Dielectric Constant

ε_o Permittivity of free space

f frequency

f_T unity gain cut off frequency

f_{max} max.freq. of oscillation

g_d output conductance

g_m intrinsic transconductance

g_m' extrinsic transconductance

$(g_m)_{sat}$ saturation transconductance

h_{21} short circuit current gain

I_d drain current

$(I_d)_{sat}$ saturated drain current

L gate length

L_s source inductance

L_d drain Inductance

L_g gate inductance

MAG maximum available gain

m_o electron rest mass

m effective mass

q magnitude of electron charge

Q(x) charge density profile

R_s total source resistance

R_{sh} sheet resistance

R_c contact resistance

R_d total drain resistance

R_g gate resistance

R_{sp} spreading resistance

R_{ds} drain – source resistance

τ mean free time between collisions

T transit time

μ mobility

μ_{eff} effective mobility

ν velocity

ν_{ave} average velocity

V_g gate voltage

V_t threshold voltage

V(x) voltage in channel

V_d drain voltage

ν_{sat} saturation velocity

x_j junction depth

Z channel width

2.2 The MOSFET

2.2 (a) Qualitative Description

A FET is a three terminal device whose schematic diagram is shown in figure 2.1. The current flow between the two terminals called the source and drain is modulated by applying a voltage to the third terminal called the gate.

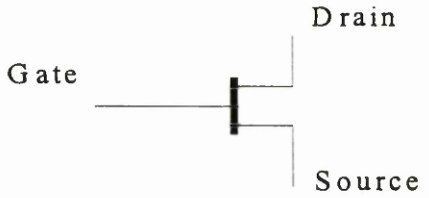
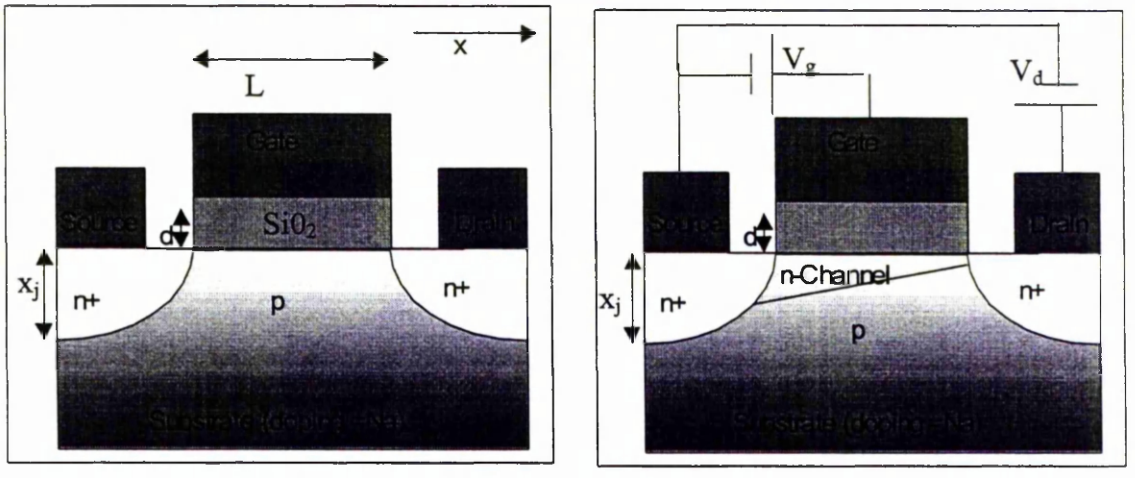


Figure 2.1 Schematic diagram of a FET.

The ability to control current flow between two terminals by applying a voltage to a third terminal allows the device to be used as a switch in digital applications or as an amplifier in analogue applications. The MOSFET has been the workhorse for semiconductor electronics to date. Figure 2.2 (a) shows the cross section of a MOSFET.



(a) (b)

Figure 2.2 The metal oxide semiconductor field effect transistor (MOSFET) (a) with no applied voltage, (b) with the gate and drain positively biased with respect to the source.

The source and drain are shown as n^+-doped regions on either side of the gate. Fabrication techniques are considered at the end of this chapter. The junction depth of the source and drain regions (x_j), the dielectric thickness (d) and the gate length (L) are important dimension.

If a potential difference is applied between the source and drain (the source is usually set to zero volts), there will be negligible current flow because of the n-p-n junction. It is possible however to create a channel for current flow between the source and drain by applying a gate voltage, figure 2.2 (b). In the case of an n-channel device, a positive voltage on the gate will attract electrons from the source towards the gate. The electrons will then be trapped at the Si / SiO_2 interface by the insurmountable energy barrier between the conduction bands of silicon and SiO_2, forming a channel of electrons between the source and drain, figure 2.3.

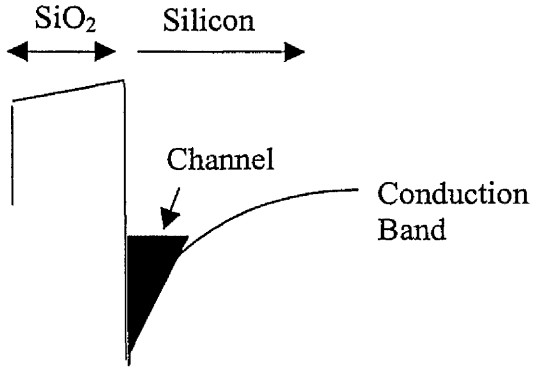


Figure 2.3 A channel confined at the Si / SiO_2 interface by the energy band discontinuity.

The channel is sometimes called the inversion layer because its carrier type is the inverse to that of the substrate. The voltage applied to the gate when a channel begins to form is called the threshold voltage (V_t). The threshold voltage is a critical parameter for digital applications. Reducing the gate length of the MOSFET has been a major factor in increasing the speed and packing density of digital circuit's [2.1]. This requires a reduction in the oxide thickness and source and drain junction depths in order to minimise undesirable short channel effects [2.2].

2.2 (b) Quantitative Analysis

For the following analysis it is assumed that the substrate is p-type and that there are no electrons in the channel at zero gate voltage and that the source and drain are both n-type. Since the gate, oxide and semiconductor form a capacitor, the charge profile along the channel is given by

$$Q(x) = C_o (V_g - V_t - V(x)). \tag{2.1}$$

The source drain current is given by

$$I_d = \mu Z Q(x) E \text{ or } = Z Q(x) \nu \text{ where } \nu = \mu E \tag{2.2}$$

Then

$$I_d = \mu C_o Z (V_g - V_t - V(x)) \frac{dV(x)}{dx} \tag{2.3}$$

Integrate (2.3) from 0 – L to get

$$I_d = \frac{\mu C_o Z}{L}\left[(V_g - V_t)V_d - \frac{V_d^2}{2}\right] \tag{2.4}$$

Equation 2.4 describes I_d in the region when $V_d < V_g - V_t$, this is known as the linear region. When $V_d = V_g - V_t$ no charge is attracted to that part of the channel, this is called pinch off. The variation in channel depth across the channel because of the channel voltage is shown by the triangular profile in figure 2.2 (b). Beyond pinch off I_d is constant, this is known as the saturation region. Putting $V_d = V_g - V_t$ into (2.4) then

$$(I_d)_{sat} = \frac{\mu C_o Z (V_g - V_t)^2}{2L} \tag{2.5}$$

The typical IV characteristics of a MOSFET are shown in figure 2.4.

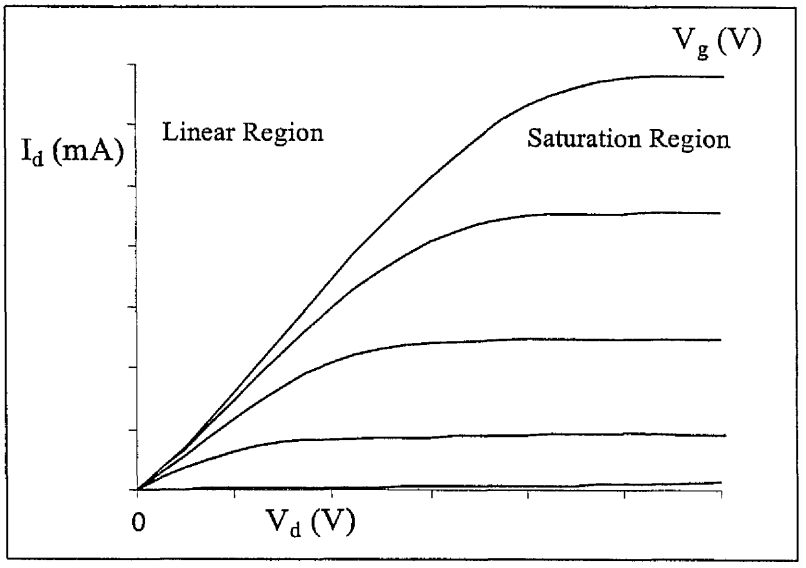


Figure 2.4 Typical IV characteristics of a MOSFET.

An enhancement mode n-channel device has just been described. Other modes of operation could similarly be described such as, a p-channel enhancement mode device, p and n-channel depletion mode device [2.3].

The transconductance g_m is an important figure of merit and is defined as

$$g_m = \frac{d(I_d)}{d(V_g)} \tag{2.6}$$

It will be shown that the high frequency performance of a FET can be estimated from the transconductance and gate capacitance. Since transconductance is easily measured at DC, it is often used to describe potential high frequency operation. The transconductance in the saturation region $(g_m)_{sat}$, can be found by differentiating equation (2.5) to give

$$(g_m)_{sat} = \frac{\mu C_o Z}{L}(V_g - V_t) \tag{2.7}$$

Figure 2.5 shows the typical transfer characteristics of a MOSFET, the transconductance and drain current are shown as a function of gate voltage.

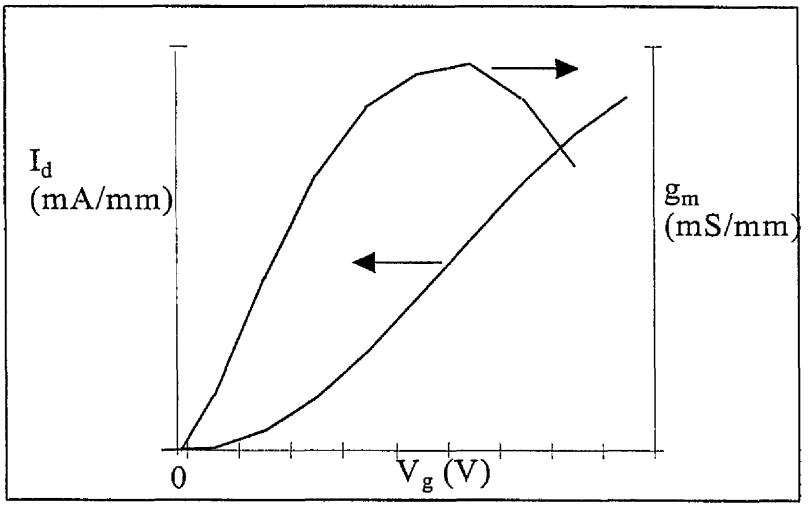


Figure 2.5 Typical transfer characteristics of a MOSFET operating in the saturation region.

The above analysis is true for long channel devices where the equation $v = \mu E$ is valid but at high drain-source field the carrier velocity saturates in which case

$$(I_d)_{sat} = Z Q v_{sat} = Z C_o (V_g - V_t) v_{sat} \quad (2.8)$$

and

$$(g_m)_{sat} = Z C_o v_{sat} \quad (2.9)$$

The above analysis shows that the transconductance is proportional to the saturation velocity and mobility in the channel. It will be shown that the transconductance must be maximised to achieve good high frequency performance. So material transport properties of the semiconductor channel are important in determining the high frequency capability of the device.

2.3 Material Transport Properties

2.3 (a) Mobility

The transport of carriers in a bulk semiconductor is governed by scattering events as the carrier drifts through the semiconductor. Scattering sites include defects in the crystal, donor atoms (ionised impurities) and phonons (lattice vibrations) [2.4]. The periodic nature of the crystal potential leads to an energy band structure, and an effective mass accounts for effect of the crystal potential [2.5]. There are 6 degenerate conduction bands in silicon. Electrons in silicon have an effective mass of $0.28m_o$. In GaAs electrons with low energy have effective mass $0.11m_o$ but because of the polar nature of the crystal there is a satellite band with effective mass $0.19m_o$ that high-energy electrons scatter into. Scattering events are accounted for by a mean free path time, which is the mean time between collisions τ. The mobility is given by

$$\mu = \frac{q\tau}{m} \tag{2.10}$$

For bulk undoped silicon and GaAs the electron mobilities are 1450 cm^2/V-s and 8500 cm^2/V-s respectively [2.6].

The electrons which form the channel of a MOSFET are trapped at the Si / SiO_2 interface by the energy band discontinuity between the Si and SiO_2 layers, figure 2.3. Charge impurities in the oxide and interface roughness will scatter carriers [2.7], so the mobility in the channel of a MOSFET is somewhat lower than the bulk material mobility. The mobility of carriers in a device are generally different than that of bulk material and are described as having an effective mobility (μ_{eff}). The effective mobility in a MOSFET is approximately half of the bulk mobility [2.8]. An effective mobility of 750 cm^2 / V-s in an n-type inversion layer is typical, for a p-type inversion layer 100 cm^2 / V-s is typical.

2.3 (b) 2DEGs and MODFETs

III-V semiconductors do not have a suitable native oxide such as SiO_2 and so use a schottky gate to control the charge density in the channel [2.9]. The channel is trapped by the band discontinuity between two different semiconductor layers, figure 2.6. The band discontinuity between two semiconductors is much smaller than that at a Si / SiO_2 interface. At large gate bias carriers may overcome this barrier and leak into layers with lower mobility, this is known as parallel conduction. The semiconductor layers are epitaxially grown and are crystalline, unlike the amorphous SiO_2 layer, so they do not have unwanted charges or surface roughness as in the Si / SiO_2 interface.

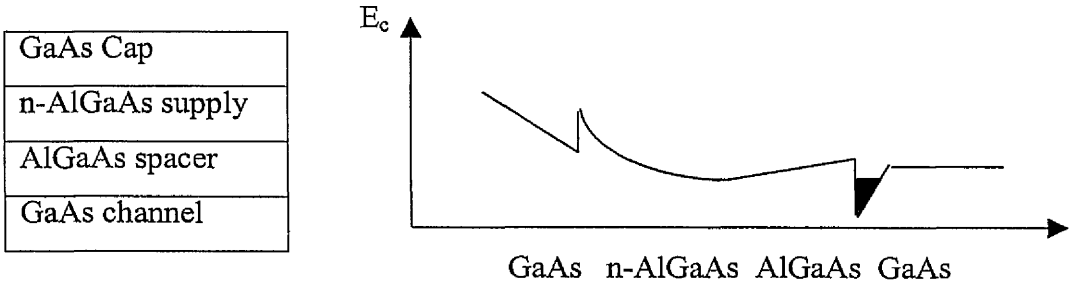


Figure 2.6 Epitaxial layer structure and band diagram of a GaAs / AlGaAs MODFET.

Figure 2.6 shows a typical layer structure of a GaAs / AlGaAs MODFET. The carriers in the channel are supplied by a doped layer called the supply layer. The channel in a MODFET is often referred to as a two dimensional electron gas (2DEG) or a two dimensional hole gas (2DHG). Unlike at a Si / SiO_2 interface, the mobility in a 2DEG can be higher than in the bulk. This is because the carriers in the channel are remote from the donor atoms located in the supply layer, thereby reducing scattering due to ionised impurities. In an GaAs 2DEG where there is already increased bulk mobility and reduced ionised impurity scattering and an epitaxialy grown interface, room temperature electron mobility as high as 12300 cm^2 / V-s has been reported [2.10]. For III-V devices, depletion mode operation is often preferred, the layer structure is designed so that a channel exists at zero gate voltage.

2.3 (c) High Field Effects

Figure 2.7 shows the velocity field characteristics of electrons and holes in silicon and GaAs [2.11]. At low field, $v = \mu E$. At high fields the velocity saturates. The saturation velocities for electrons in silicon and GaAs are similar indeed for silicon it is slightly higher. In GaAs and other III-V compounds, intervalley transfer causes a peak in the velocity field curve.

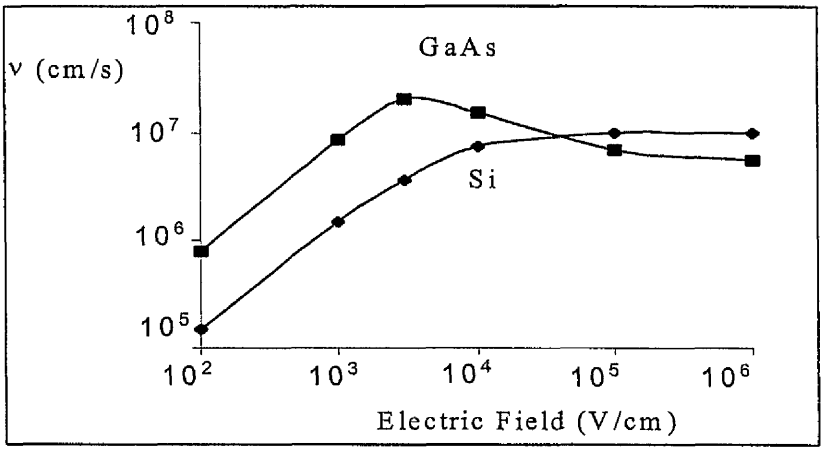


Figure 2.7 Velocity field characteristics of electrons in GaAs and Si.

When an electric field is first applied to a channel, carriers can reach a velocity that is greater than the saturation velocity. This is called velocity overshoot, the effect only lasts for a time period of the order of a few tenths of pico-seconds before steady state is resumed [2.12]. For very short gate length devices a few tenths pico-seconds of overshoot can have significant effect on the high frequency performance [2.13]. In a FET the electric field and carrier concentration are both dependent on position in the channel, so the velocity and mobility will also vary along the channel length. The transient effect of velocity overshoot also leads to a non-uniform carrier velocity along the channel. The average carrier velocity in the channel is the gate length divided by the time that it takes a carrier to travel from the source end to the drain end of the gate (the transit time T) [2.13].

$$v_{ave} = \frac{L}{T} \tag{2.11}$$

A high average velocity (or low transit time) is required for high-speed devices.

2.4 Parasitic Resistance

The transconductance calculated in equations (2.7) and (2.9) is known as the intrinsic transconductance, and neglects the contribution of the series resistance of the source and drain. Figure 2.8 shows the location of the contact resistance (R_c), sheet resistance (R_{sh}) and channel spreading resistance (R_{sp}) [2.12].

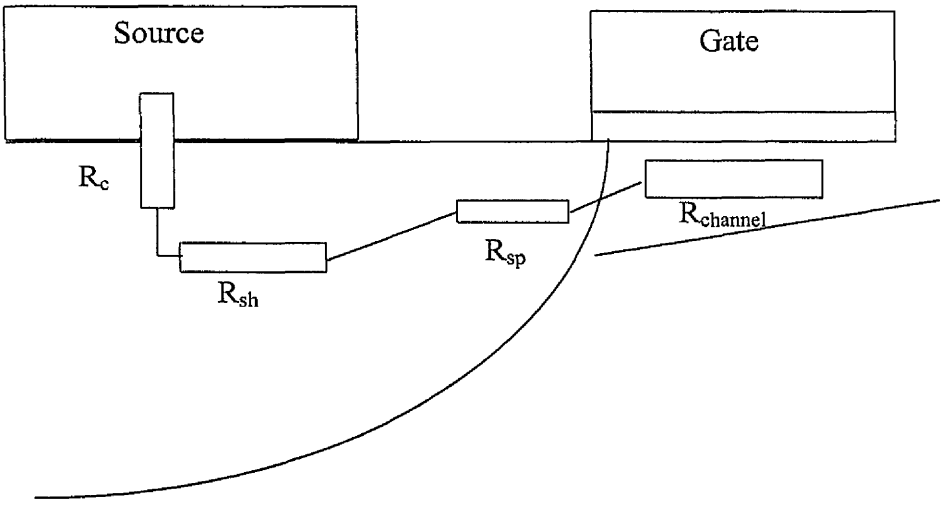


Figure 2.8 Physical location of access resistance in a FET.

The source resistance R_s is sum of three resistances R_c, R_{sh}, R_{sp}.

- R_c is the contact resistance between metal and semiconductor.
- R_{sh} is the sheet resistance of the semiconductor between the metal contacts and the channel.
- R_{sp} is the spreading resistance resulting from the transition from the narrow channel to the deep source / drain regions.

As a result of the total series resistance the effective gate voltage V_g is reduced by the volt drop across the source resistance such that

$$V_g' = V_g + (R_s + R_d) I_d \tag{2.12}$$

Therefore the measured (extrinsic) transconductance is

$$g_m' = \frac{g_m}{(1 + (R_s + R_d) g_m)} \tag{2.13}$$

Contact Resistance (R_c)

R_c x Z has units of Ω-mm and is of the order of 0.1 Ω-mm for alloyed contacts that are used for GaAs MODFETs [2.14]. The use of silicides provides a contact resistance of 0.1 Ω-mm in MOSFETs [2.15]. A 100 μm wide MODFET or MOSFET will have a contact resistance of approximately 1 Ω.

Sheet resistance (R_{sh})

The sheet resistance of a silicide in silicon technology is about 2 Ω / sq [2.16] which effectively eliminates R_{sh} as a limiting resistance. In a GaAs MODFET, the sheet resistance is about 200 Ω / sq [2.17]. Present III-V technology allows for a 0.5 μm gap between the source and gate giving R_{sh} = 1 Ω for a 100 μm wide device.

Spreading resistance (R_{sp})

The region of transition between the deep source and drain junctions to the very thin channel leads to the spreading resistance. It has been shown that the spreading resistance reduces as the gate length is increased because of the increased electric field. [2.18]. For short channel devices the contact resistance is the largest of the three elements of resistance.

2.5 Transconductance

By considering equation (2.6) and that the mobility in GaAs based MODFETs is at least a factor of 10 greater than in MOSFETs we would expect a similar mismatch in transconductance. However for short channel devices it has been shown that velocity saturation and parasitic resistance can play a major role. Figure 2.9 shows transconductance versus gate length for recently reported MOSFETs and GaAs based MODFETs [2.19][2.20] [2.21][2.22].

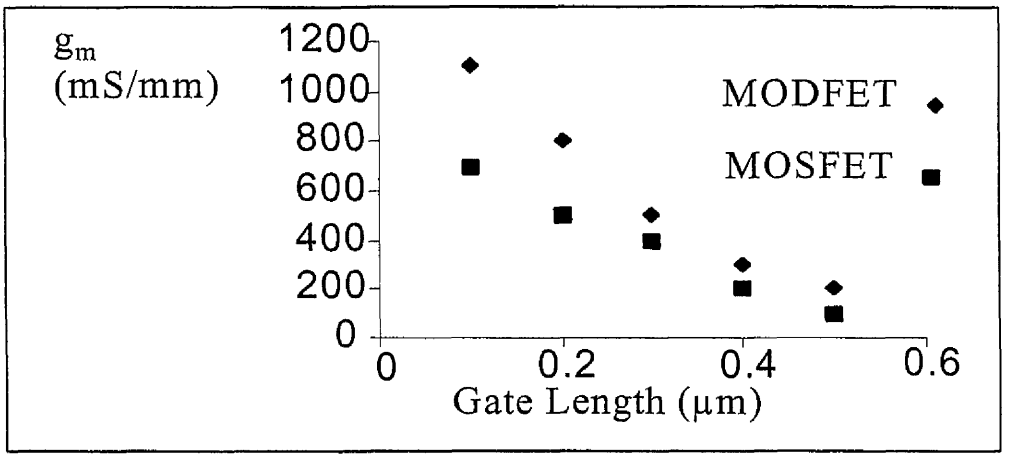


Figure 2.9 Reported maximum transconductance for Si MOSFETs and III-V MODFETs.

2.6 High Frequency Performance

When analysing the high frequency capabilities of a FET, it is customary to consider small signal equivalent circuits. The small signal equivalent circuit of the intrinsic device is shown in figure 2.10, note that the transconductance is the extrinsic value.

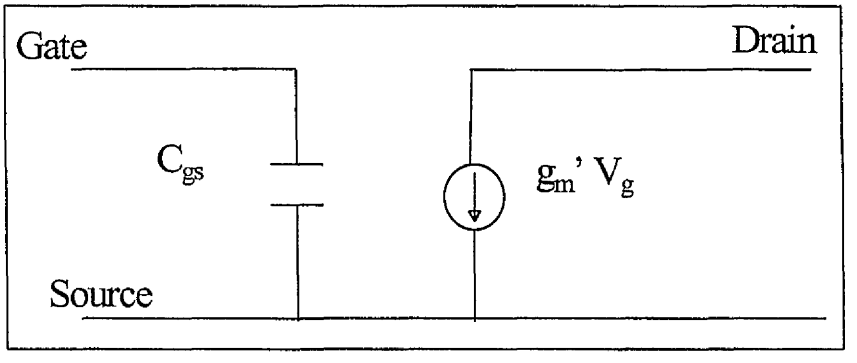


Figure 2.10 Small signal intrinsic equivalent circuit of a FET.

The cut off frequency f_T is defined as the frequency at which the magnitude of the short circuit current gain (h_{21}) is unity. From figure 2.10 it can be shown that

$$f_T = \frac{g_m'}{(2\pi\ C_{gs})} \qquad (2.14)$$

Where C_{gs} is the gate-source capacitance and is given by

$$C_{gs} = \frac{\varepsilon_r \varepsilon_o A}{d} \qquad (2.15)$$

Consider a hypothetical example of a 0.1 μm x 100 μm device using 6 nm of SiO_2 as an insulator, C_{gs} = 50 fF. f_T is obtained by plotting the magnitude of h_{21} in dB versus frequency on a log scale (figure 2.11). The slope of the curve is 20 dB / decade and f_T occurs when $|h_{21}| = 0$ dB.

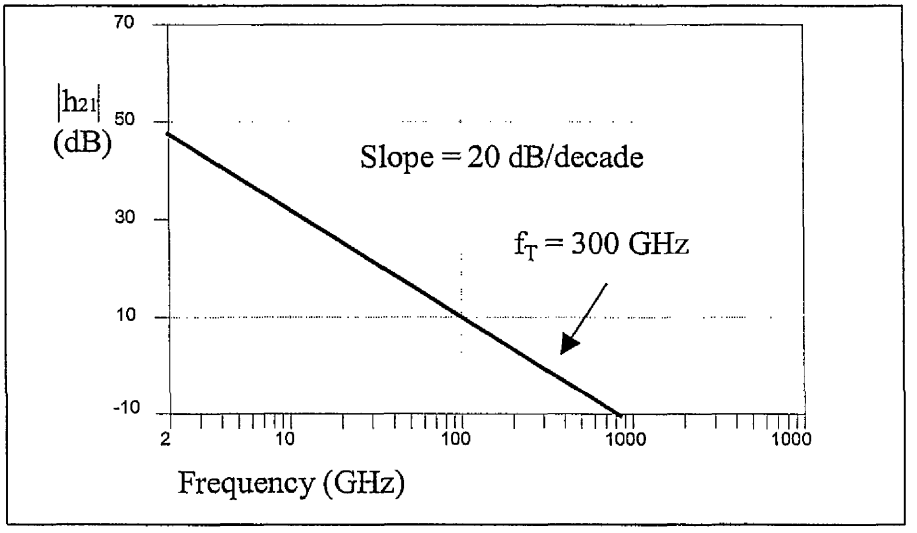


Figure 2.11 $|h_{21}|$ versus frequency, showing f_T.

Figure 2.11 shows that an f_T of 300 GHz is theoretically possible for a device with g_m of 600 mS/mm and C_{gs} of 50 fF. Such transconductance and gate-source capacitance is possible for both Si and GaAs devices of 0.1 μm gate length (figure 2.6). The average carrier velocity and transit time can be obtained from

$$T = \frac{1}{2\pi f_T} \qquad (2.16)$$

In this hypothetical example the transit time would be approximately 0.5 ps. Giving an average carrier velocity of 2 x 10^7 cm/s, which would suggest velocity overshoot in the channel.

The addition of parasitic elements has a significant effect on the RF performance of a device. The equivalent circuit and the physical origin of parasitic lumped elements are shown in figure 2.12 and 2.13 [2.23].

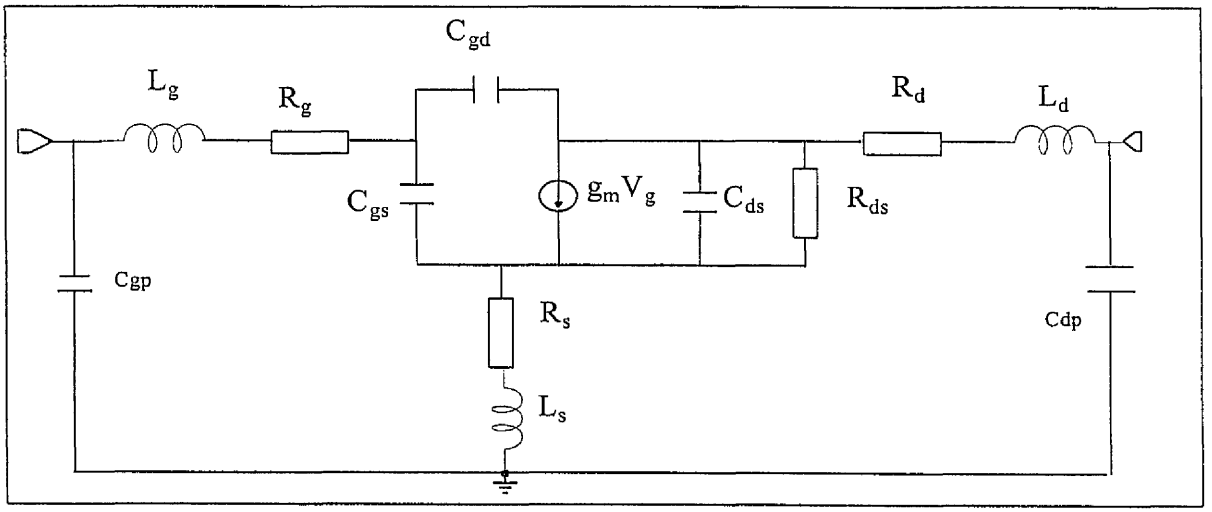


Figure 2.12 Small signal extrinsic equivalent circuit of a FET.

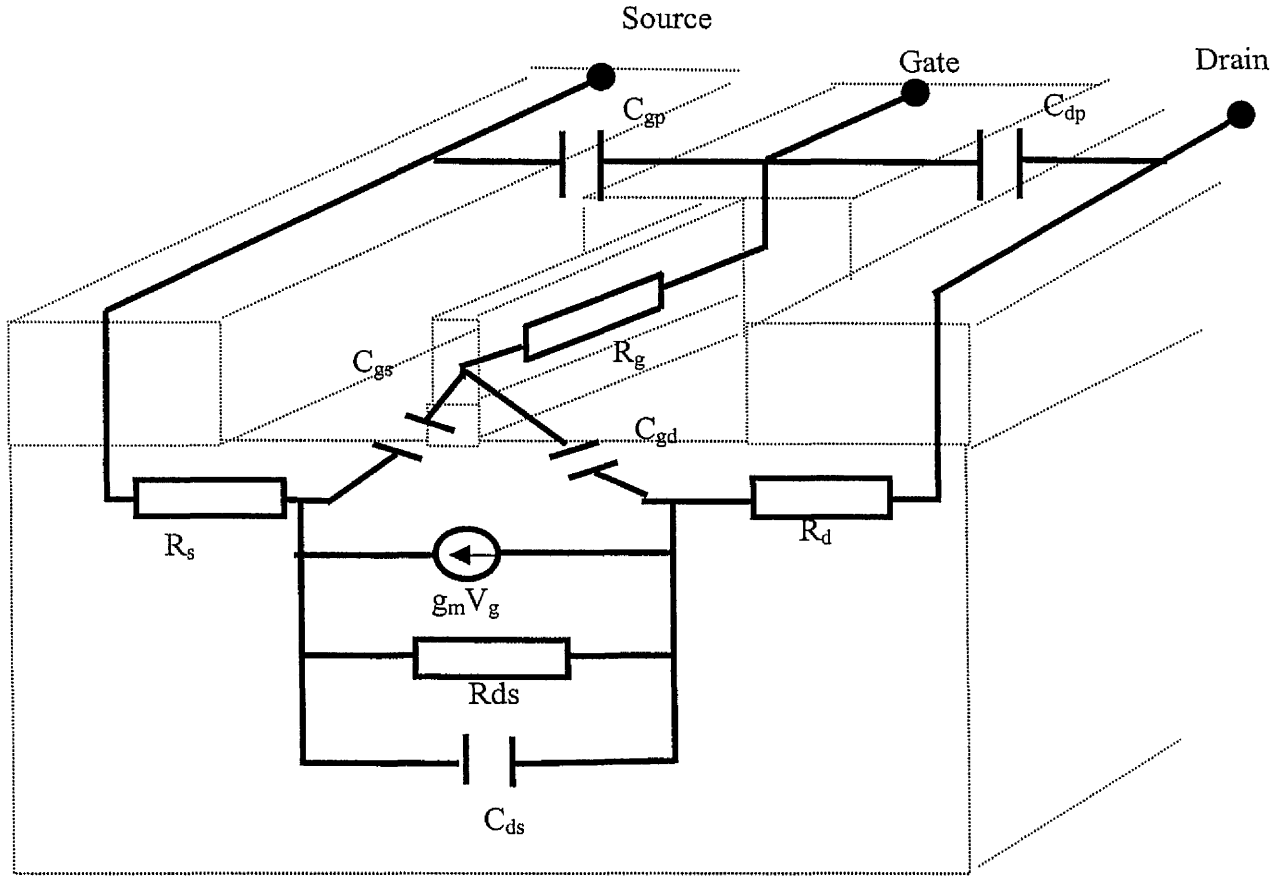


Figure 2.13 Physical origin of parasitic resistance and capacitance.

Typical values of the parasitic elements introduced above are shown in table 2.1 assuming a 100 nm gate length.

	R_g (Ω)	R_s,R_d (Ω)	C_{gs} (fF)	C_{gd} (fF)	C_{gp},C_{dp} (fF)	g_m (mS/mm)	R_{ds} (Ω)	L_g,L_d,L_s (pH)	C_{ds} (fF)
Si	50-100	2-5	10-50	4-6	100-1000	500	400	1-5	5-7
GaAs	10-30	2-5	10-50	4-6	10-100	700	400	1-5	5-7

Table 2.1 Typical equivalent circuit elements for 100 nm gate length FETs.

From the equivalent circuit of figure 2.12, f_T can be shown to be [2.24]

$$f_T = \frac{g_m}{2\pi (C_{gs}+ C_{gd})(1 + (R_s+ R_d)/R_{ds})} \tag{2.17}$$

In a well-designed device, $R_{ds} >>> R_s + R_d$ and $C_{gs} > C_{gd}$ so equation 2.14 is a very good approximation. Transconductance and gate source capacitance are then the limiting parameters for high f_T.

Another important RF figure of merit is the available power gain of the device or maximum available gain (MAG). The maximum frequency of oscillation f_{max} is defined when MAG is unity and can be shown to be [2.24]

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_g+R_s}{R_{ds}} + 2\pi f_T R_g C_{gd}}} \tag{2.18}$$

It can be simplified to be approximately [2.25]

$$f_{max} = \frac{f_T}{2}\sqrt{\frac{R_{ds}}{R_g}} \tag{2.19}$$

So to obtain a high f_{max} from a device with high f_T, R_{ds} / R_g must be maximised.

Discussion of Equivalent Circuit Elements

C_{gs} The gate capacitance C_{gs} of a 0.1 μm x 100 μm gate is about 50 fF. However in order to measure the device or to make contact to the rest of a circuit, contact pads are required. Since GaAs is a semi insulating substrate, contact pad capacitance (**C_{gp}** and **C_{dp}**) can be as low as 10 fF. In present silicon technology probe pad capacitance is typically much greater than 100 fF and is currently a limiting factor for high f_T and f_{max} for devices fabricated on a silicon substrate.

C_{gd} is the gate-drain capacitance and is normally of the order of 5 fF.

R_{ds} is the inverse of channel conductance g_{ds} which is defined as $d(I_d) / d(V_d)$. The device gain is given by g_m / g_d and must be maximised for high f_{max}. A high R_{ds} in the saturation region is desirable, equation 2.19.

R_g includes the probing pad resistance, the gate resistance and any gate discontinuity between pads and gate. Assuming that there is no discontinuity, R_g is dominated by the gate itself. For GaAs MODFETs gold is preferred as the gate metal because of its low sheet resistance which is typically 0.2 Ω / sq. A T shaped gate is used to further reduce the DC gate resistance to about 0.02 Ω / sq [2.26]. Standard silicon technology currently uses a polycide gate material. The sheet resistance of polycide is 3 Ω / sq for line widths greater than 0.15 μm. A sharp increase in sheet resistivity of polycide gates is expected for linewidths below 0.15 μm [2.27]. Using current MOSFET fabrication technology, R_g is a major limiting factor for the f_{max} of Si devices. In addition to the serious effect gate resistance has on f_{max}, it has also been shown that the gate resistance is a dominant factor in the noise figure of a FET and should be minimised [2.28].

R_s and **R_d** have been considered previously, there is a small additional resistance of the probing pads. **C_{ds}** is the drain – source capacitance and has limited effect on microwave figures of merit. **L_s**,**L_d** and **L_g** are the parasitic pad inductance's and may arise from unusually long probing contacts, but in the modelling of devices in this work they are not critical.

Cut off Frequency

Figure 2.14 shows recently published results of f_T versus gate length for Si n-MOSFETs [2.29] [2.30] [2.31] and GaAs based MODFETs [2.32] [2.33] [2.34]. The highest f_T for a GaAs based 0.1 μm gate length device is 200 GHz. Not shown on the graph are the highest f_T ever produced of 300 GHz and 350 GHz for MODFETs fabricated on InP substrates [2.35][2.36]. The maximum cut off frequency reported for a Si MOSFET is 150 GHz.

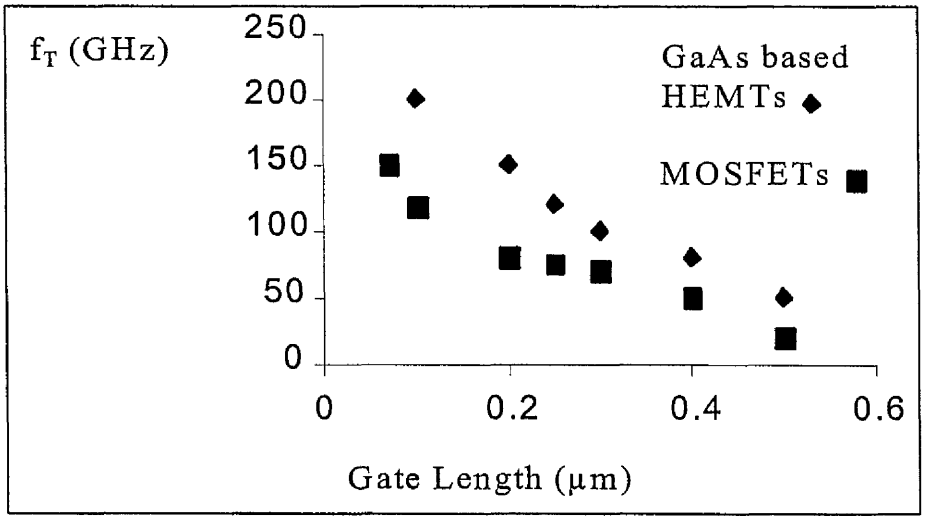


Figure 2.14 Reported cut off frequency versus gate length for Si MOSFETs and GaAs based MODFETs.

Figure 2.14 shows that the performance of Si MOSFETs in terms of cut-off frequency can be compared with that of GaAs based MODFETs. However whilst the maximum frequency of oscillation (f_{max}) of most reported III-V based devices is larger than f_T, it is rare for f_{max} to even be mentioned in a report on a MOSFET. This is because it is so low, a typical f_{max} reported for a MOSFET with 0.18 μm gate length is 30 GHz [2.37].

Summary

In summary there are a number of areas requiring optimisation to produce an RF FET,

1. Intrinsic material transport properties leading to high g_m and f_T.
2. Low parasitic source and drain resistance leading to high g_m and f_T.
3. Low gate resistance leading to high f_{max} and better noise performance.
4. Low parasitic gate capacitance for high f_T and f_{max}.
5. Low output conductance for higher gain and f_{max}.

Criteria 1 and 2 have been met in the MOSFET, criteria 3 and 4 are currently the major limiting factors in MOSFET performance at high frequency.

2.7 Fabrication of MOSFETs and HEMTs

The fabrication processes used are common to both types of device however they can be used in very different ways. Silicon very large scale integration (VLSI) fabrication is dominated by chip layout and circuit requirements. In memory chips, threshold voltage control is more critical than maximising g_m or f_T. In GaAs monolithic microwave integrated circuit (MMIC) technology where there is a much lower level of integration, devices are more important and are designed for maximum RF performance. The following sections are intended as a comparison between MOS and MODFET fabrication technologies so the unit processes are only very briefly described. Details of processes used in this work are contained in chapter 5. The comparison between process flows is made by diagrams of typical fabrication processes for a MOSFET then a MODFET.

2.7 (a) Lithography

Lithography is the technique used to define the physical geometry of devices. A polymer called resist that is sensitive to either light or electrons is spin coated onto the sample. Parts of the sample are then exposed to light through a mask or an electron beam is scanned across the sample. Subsequent developing will remove the resist where exposed if positive resist is used. It is also possible to use negative resist, which removes where not exposed. Optical photolithography is preferred in industry because of its capability for large throughput. Advances in optical techniques and resists have maintained its domination in industry. DUV (Deep Ultra Violet) lithography is capable of 100 nm resolution [2.38][2.39]. Although advances are still being made in optical techniques, electron beam lithography is used in research facilities, where high throughput is not necessary, to define patterns smaller than 100 nm [2.40]. The remaining patterned resist can then be used to lift off deposited material or as an etch mask. To give an undercut profile of the resist that is necessary for reliable lift-off, two layers of resist of different sensitivity are used [2.41] (see Figure 2.15)

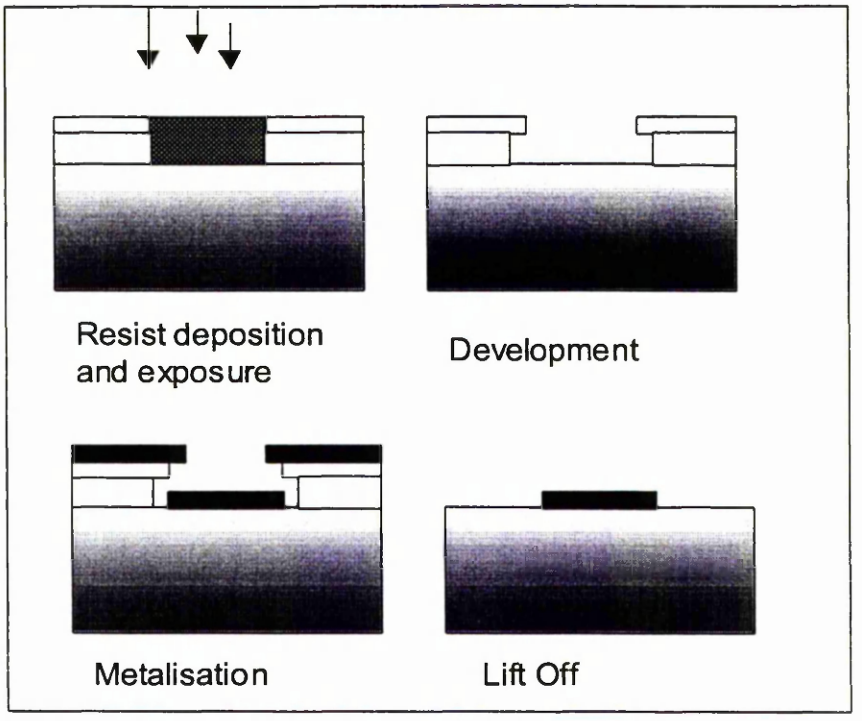


Figure 2.15 The lift off process.

2.7 (b) Dielectric Growth/Deposition

The growth of the insulating gate oxide in a MOSFET is one of the most important processes for VLSI. The charge trapped in the oxide and at the interface must be minimised to avoid variations in threshold voltage [2.42]. Rapid thermal oxidation using a dry oxygen source is regarded by industry as the optimum process for growing the thin gate oxide of MOSFETs. The typical oxide thickness of a 250 nm gate length device is 6 nm. VLSI requires thick (200 – 1000nm) spacer and inter layer dielectrics (ILD) between layers of metalisation. ILD's can be deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) [2.43][2.44]. Spin on glass is also used as an ILD [2.45].

2.7 (c) Ion implantation

Ion implantation is used extensively in silicon device fabrication and is used to place the doped regions accurately in the substrate. Ions of a given species are accelerated inside the implanter and then penetrate into the device. The most common use for this is in the formation of the source and drain contact regions. Source drain junction depth of sub 500 nm gate length devices must be less than 200 nm. This requires implant ions with energy of less than 20 keV [2.46] (chapter 4). BF_2 is used for p-type implants and P or As for n-type implants. Excellent control of dose and profile can be achieved using ion implantation rather than diffusion.

2.7 (d) Metalisation

There are several methods of metalisation employed in device manufacturing, including thermal evaporation, sputtering, CVD and electroplating [2.47]. Sputtering is the method most commonly used in silicon device mass production and is described in chapter 4. The metals used in silicon VLSI are Al, W and Ti. Au, Cu and Silver are also being investigated since gate resistance and interconnect delays are becoming limiting factors in device and circuit performance [2.48][2.49][2.50]. Au is the preferred metal in GaAs devices and circuits, however, the VLSI silicon industry is very reluctant to use gold as it diffuses readily into silicon and acts as a deep trap [2.51] [2.52].

2.7 (e) Rapid Thermal Annealing (RTA)

Contacts and implants need to be annealed at high temperature to allow the donors to be activated and so lowering resistance and reducing implant damage. Implants can be annealed at temperatures up to 1300 °C for a few seconds with fast ramp up and down profiles [2.53].

2.7 (f) Etching

The lift off process previously described is used extensively in the fabrication of GaAs devices. In silicon manufacturing high levels of integration and yield are required and etching is the preferred pattern transfer technique. Wet chemical etching or dry plasma etching are used depending on the requirements. It is often important to be able to etch one material while not etching another. This is referred to as the selectivity of the etch process. Wet etching is normally a quicker and cheaper method of producing an isotropic etch. In dry etching a more vertical etch profile is produced [2.54].

2.8 Typical MOSFET Fabrication Process

This section describes a typical fabrication flow using the above techniques to make a MOSFET. The process shown in figure 2.16 is a simple method compared with a typical industrial process that will have over 20 lithography levels.

fig 2.16 a : An active area is formed by shallow dry etching, only the active area is shown here. The p type silicon substrate is ion implanted with an n type dopant to form a deep n-well, not shown. Thermal gate oxidation is then performed at 1100 °C this will also activate the n-well implant. Immediately, the polysilicon / tungsten gate stack is deposited by sputtering.

fig 2.16 b: The gate is then patterned using photolithography and dry etched. The first source and drain implant called the lightly doped drain (LDD) implant is performed, at low energy and dose to create a very shallow junction.

fig 2.16 c : The next steps form the sidewall spacer, a blanket CVD coverage of oxide is deposited then etched off leaving the vertical spacer on the sides of the gate as shown. A second source drain implant is now performed at higher energy and dose to decrease contact and access resistance of the source and drain. A rapid thermal anneal will be performed at this stage to activate the source and drain implants.

fig 2.16 d : A blanket coverage of Ti is applied. A two stage anneal and etch process is used to form TiSi where the Ti comes into contact with Si or polysilicon. Ti in other areas is removed by a wet etch.

fig 2.16 e : A thick interlayer dielectric (ILD) is then deposited and planarised using chemical mechanical polishing (CMP). Contact windows are then opened up in the ILD, into which tungsten plugs are deposited by sputtering. The first layer of metal is evaporated Aluminium or sputtered W. Up to 6 layers of metal are possible.

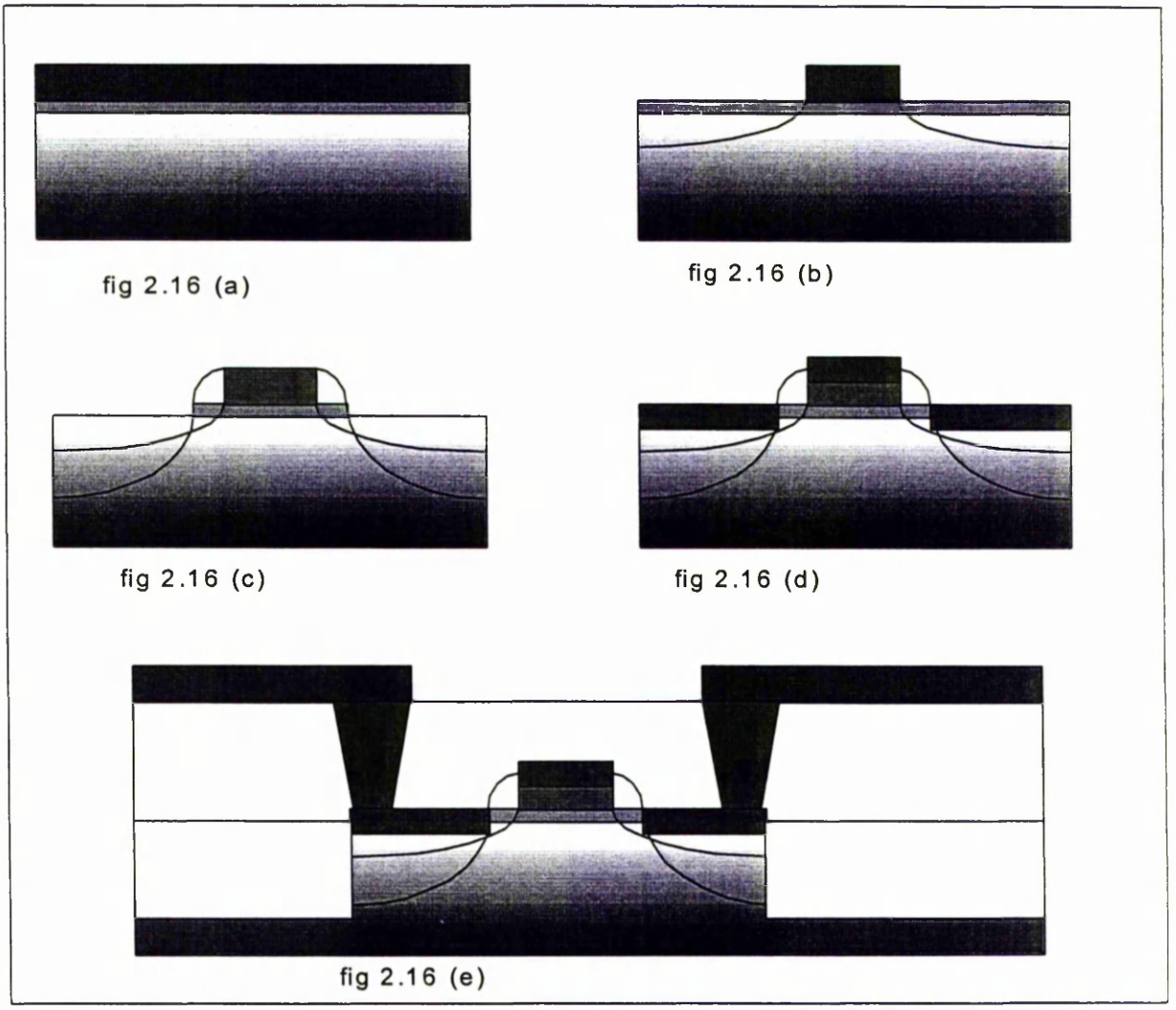


Figure 2.16 Typical MOSFET process flow.

2.9Typical GaAs HEMT Fabrication Process

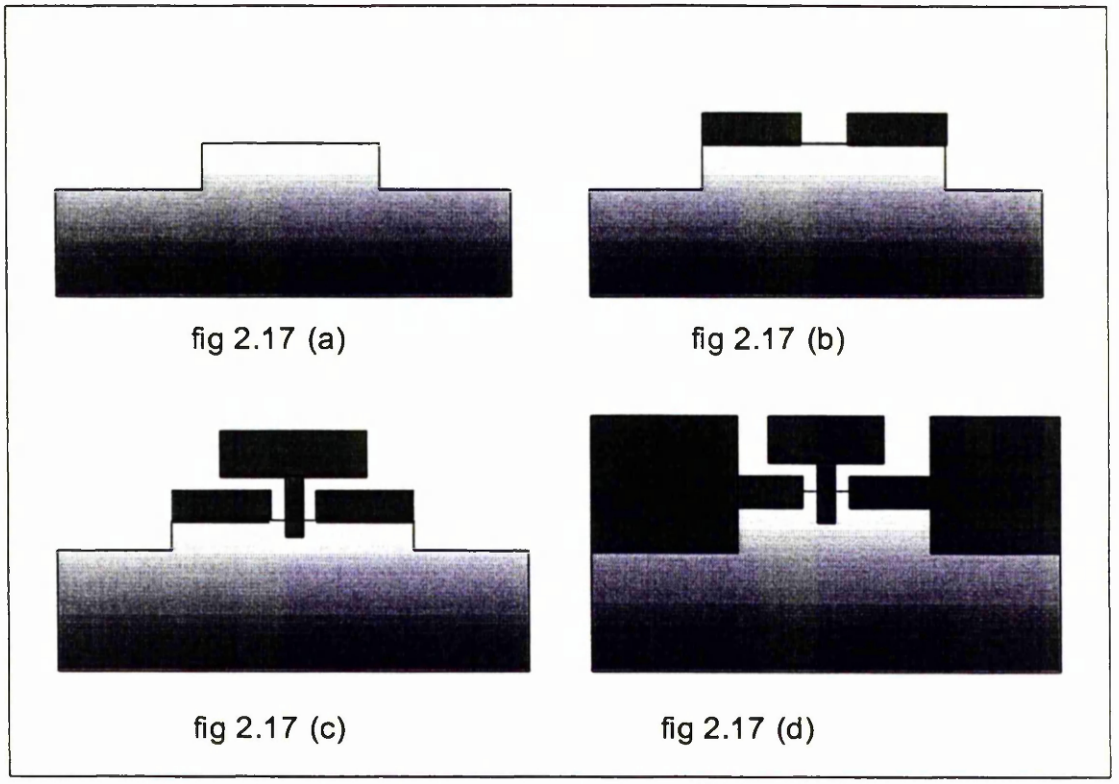


Figure 2.17 Typical MODFET fabrication process flow.

Fig 2.17 (a) An active area is created by dry etching the substrate creating a MESA. The etch is just deep enough to be below the channel which is about 50 nm.

Fig 2.17 (b) Ohmic contacts are formed by evaporating alloys of Ge / Ti / Au which are known to produce low contact resistance. The contacts are annealed at approx. 300 °C.

Fig 2.17 (c) The top 20 nm or so of highly doped layers are etched where the gate will be formed. The gold T shaped gate is the deposited by thermal evaporation using 3 levels of e-beam resist [2.52].

Fig 2.17 (d) Probing pads normally thick layers of gold can then be deposited directly on the semi insulating substrate. The existence of the semi insulating substrate creates lower pad capacitance.

2.10 Conclusion

GaAs MODFETs as a result of high electron mobility, velocity peak and a semi insulating substrate, have dominated electronic applications in the range 1-200 GHz over the past decade or so. Silicon MOSFETs as a result of cost, safety, easy fabrication, integration, high yield and low power consumption have dominated electronic applications at any frequency that they can operate.

A FET operating at microwave frequencies requires material with high mobility and high average carrier velocity. As the gate length is shrunk, parasitic elements such as source drain and gate resistance and capacitance begin to dominate device performance. Silicon technology has optimised parasitic series resistances to the channel allowing the fabrication of sub 100 nm devices with f_T of 150 GHz. However as yet the f_{max} of these devices is yet to break 50 GHz. f_{max} and noise figure are two of the most important figures of merit for microwave transistors. FETs must have low gate resistance for high f_{max} and low noise figure. As yet silicon process designers have essentially ignored the high gate resistance of polysilicon gates in favour of high yield and low series resistance. Another limiting factor for RF performance of MOSFETs is the parasitic gate capacitance associated with the contact pads on a low resistance silicon substrate.

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Chapter 3

Silicon/Silicon-Germanium

3.1 Introduction

Silicon-Germanium (SiGe) epitaxial layer structures offer a possibility to improve on the transport characteristics of silicon based devices. Since Si / SiGe layer structures were to be used in this work to fabricate MOSFETs, this chapter discusses the properties and use of SiGe layer structures. A brief historical perspective from the introduction of SiGe epitaxial layer growth in the 1980's is followed by a discussion of some basic growth properties of the alloy. The basic data required for heterostructure formation is presented followed by a simple example. Low field transport properties of electrons in strained silicon and holes in strained SiGe are reviewed. The results of Monte Carlo simulation of high field electron transport in short channel devices is reviewed. The reported performance of SiGe FETs are compared to silicon FETs and discussed.

3.2 Historical Perspective

There was little interest in the SiGe alloy for use in electronic circuit devices until the advent of epitaxial growth techniques, which were developed in the 1970's for III-V semiconductor's [3.1] [3.2] [3.3]. Serious work on epitaxial Si / SiGe layer structures began in the early 1980's. Two-dimensional hole confinement in Si / SiGe alloy layers [3.4] was observed. Increased electron mobility in strained silicon was reported [3.5]. In 1985 the first p-type SiGe channel FET was made by Pearsal and Bean [3.6]. This was closely followed by the announcement of an n-channel FET from Deambkes in 1986 [3.7]. Details of subsequent demonstration devices both n and p-channel, using silicon germanium epitaxial layers on a silicon substrate have been published [3.8-3.13], with all devices showing better performance than silicon devices. The silicon germanium bipolar transistor first introduced in 1988 [3.14] has made the most use of silicon germanium technology to date and is already in commercial production [3.15]. There has been intense interest in SiGe in recent years and there are a number of good review papers on the subject, covering growth, transport theory, optical, bipolar, FET and RF applications [3.16][3.17][3.18][3.19]. The following sections summarise the areas relevant to this work.

3.3 The Alloy and epitaxial Growth Considerations

It is customary to represent the alloy of Si and Ge as $Si_{1-x}Ge_x$ where x is the fraction of Ge atoms in the alloy. The lattice constant a_0 for silicon is 0.543 nm and for germanium is 0.566 nm. The lattice constant of the SiGe alloy lies between that of Si and Ge, it depends linearly on the Ge content. Figure 3.1 shows the lattice constant of SiGe as a function of Ge content as determined by Dismukes [3.20] showing only slight variations from the fitted linear equation.

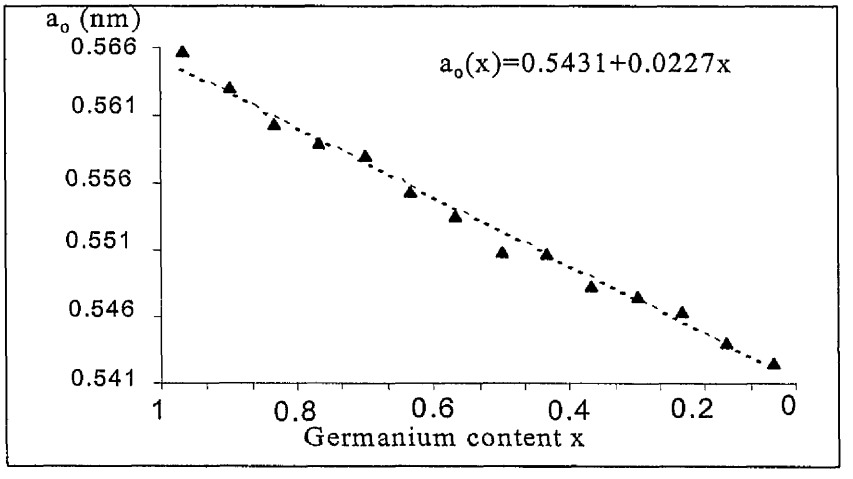

Figure 3.1 Lattice constant of SiGe as function of Ge content as measured by Dismukes fitted to a straight line.

Epitaxial layers of SiGe can be grown on a Si substrate using either Molecular Beam Epitaxy (MBE) [3.21] or Ultra High Vacuum Chemical Vapour Deposition (UHVCVD) [3.22]. Using these methods, very thin layers of a given species can be deposited and grown to a given thickness and doping concentration. Epitaxial processes involve many complex physical and chemical steps. The following is a summary of some useful information for the consideration of SiGe epitaxial layer structures. A 2D representation of separate Si and SiGe lattices are shown in figure 3.2 (not to scale). The diagram emphasizes the relatively large lattice constant mismatch between the two.

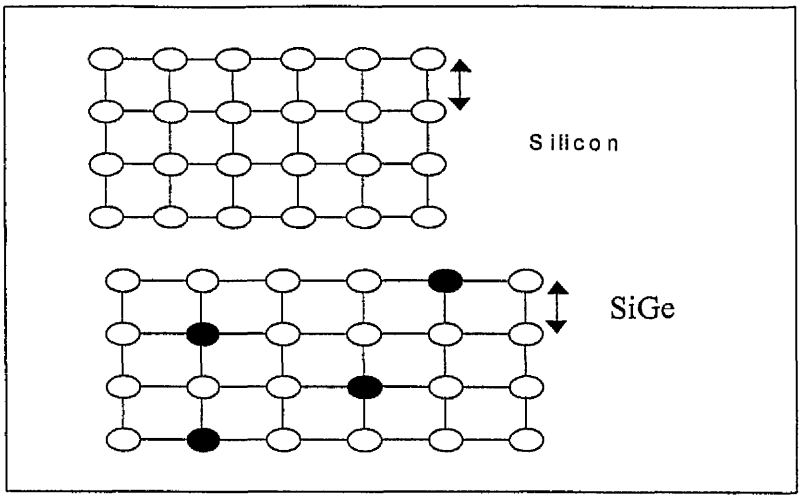

Figure 3.2 Two-dimensional representation of Silicon and SiGe lattice structures.

The difference in lattice constant between the SiGe and the Si substrate implies that there must be some means to accommodate the difference. There are several known mechanisms that can accommodate the strain as shown in figure 3.3.

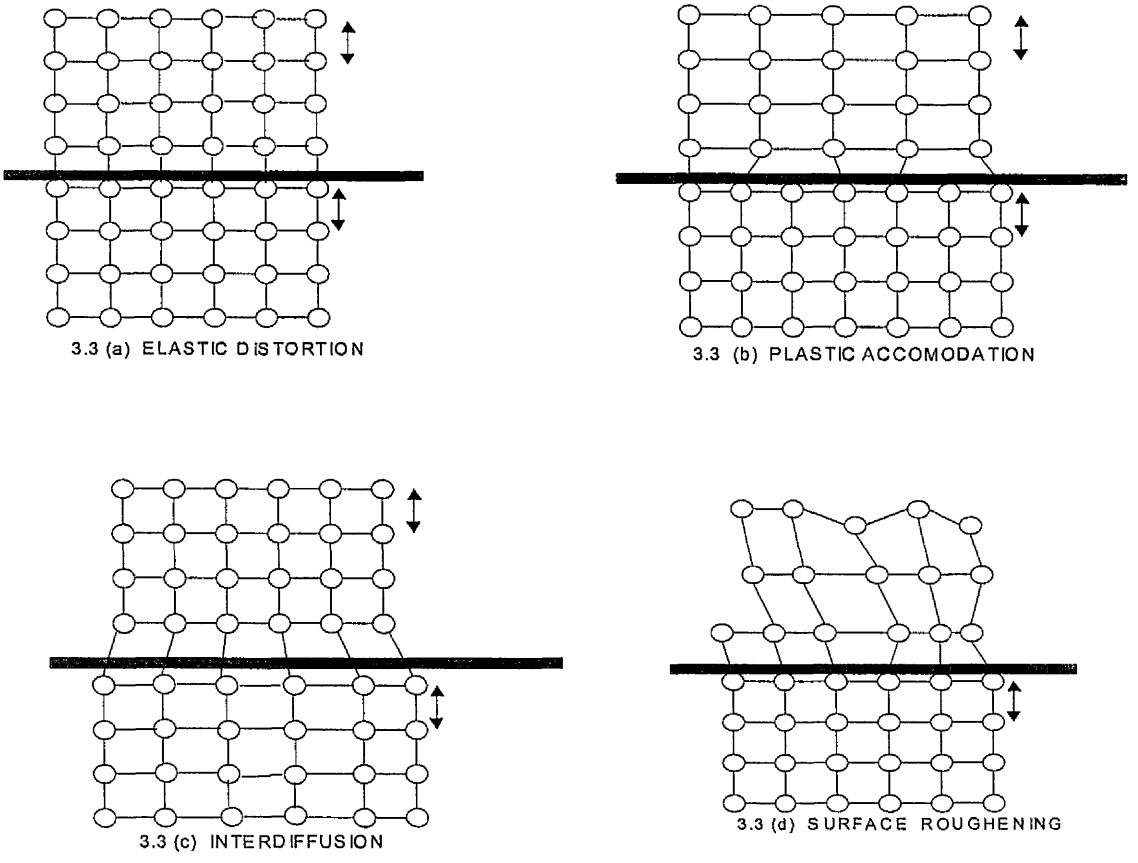

Figure 3.3 Possible consequences of growing mismatched epitaxial layers.

Elastic Distortion (figure 3.3 a)

Here the lattice spacing of the epitaxial layer distorts to fit the lattice of the substrate layer, in which case the epitaxial layer is strained. Si grown on a SiGe substrate has tensile strain. SiGe grown on Si is compressively strained. Strain can be advantageous for carrier transport (section 3.5). The thickness of the strained epitaxial layer must be less than a critical thickness known as the Mathew Blacklees limit [3.23]. If the layer is thicker than the critical thickness the strain begins to relax and plastic accommodation occurs. The critical thickness for Si on SiGe and SiGe on Si is of the order of 20 nm for a Ge concentration of 0.3. Increasing the Ge concentration reduces the critical thickness. Buried layers of strained Si and strained SiGe thinner than the critical thickness can be used as the channel for high mobility FET's.

Plastic Accommodation (figure 3.3 b)

The generation of misfit dislocation arrays for layers thicker than the critical thickness allows the epitaxial layer to relax. Thick relaxed SiGe layers typically > 1 μm thick are grown on silicon substrates to provide a 'virtual' SiGe substrate. A silicon layer can then be grown on top of the SiGe, the epitaxial silicon layer will then be strained. Plastic accommodation of strain produces misfit dislocations. Misfit dislocation lines allow relaxation of atomic bonds and create a wavy surface causing **surface roughness (figure 3.3 d)** [3.24] [3.25].

Interdiffusion (figure 3.3 c)

At high processing temperatures and in layers with high Ge content, Ge will diffuse through a silicon lattice. The diffusion coefficient will depend on temperature. For the present work, such interdiffusion is not desired. Fortunately early studies [3.26] have established that after annealing at 800 °C for 2 hours no detectable difference is detected in the Ge spectrum.

3.4 Simple Initial Analysis of SiGe material in this work

An optical plan view of a Si / SiGe structure containing a virtual SiGe substrate is interesting. Figure 3.4 shows an optical micrograph of two Si / SiGe samples grown by CVD. The top sample was grown at 750 °C while the lower one at 600 °C. The characteristic lines on the sample are caused by the strain relaxation and are sometimes called strain lines. The spacing between the lines is proportional to the number of misfit dislocations. In the sample grown at low temperature, the pitting effect is often observed and is attributed to threading dislocations that grow up to the surface. Both samples have a very thick >1 μm 'virtual substrate' of SiGe grown on a silicon substrate. In addition a simple low-resolution surface profile of a silicon sample and a Si / SiGe sample shown in figure 3.5 can show the surface roughness of a relaxed SiGe layer.

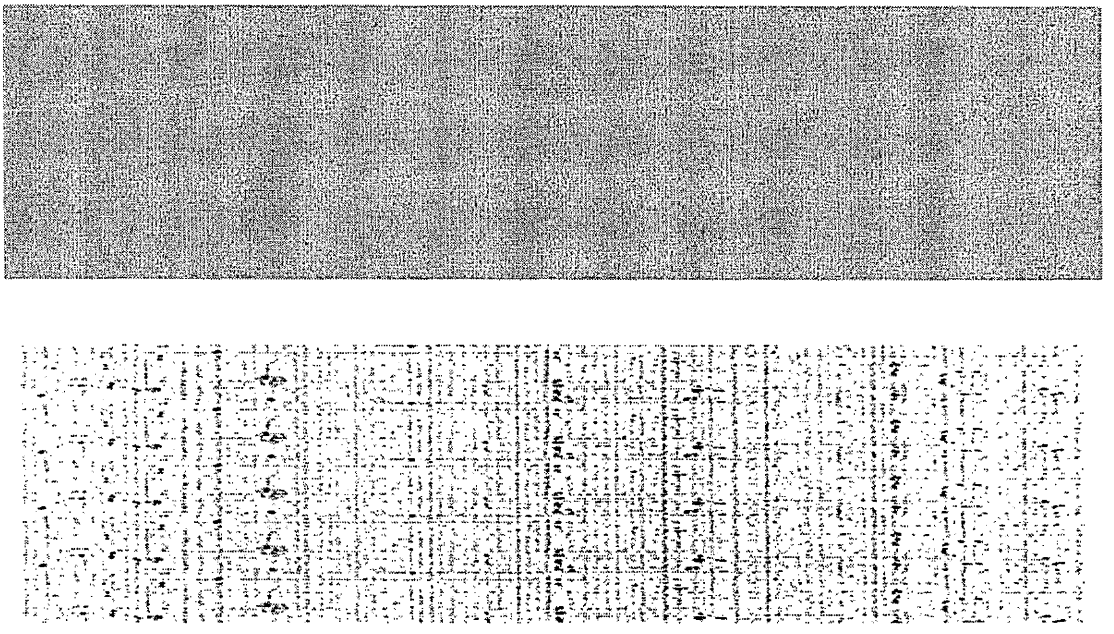

Figure 3.4 Optical micrograph of the top surface of two Si / SiGe samples.

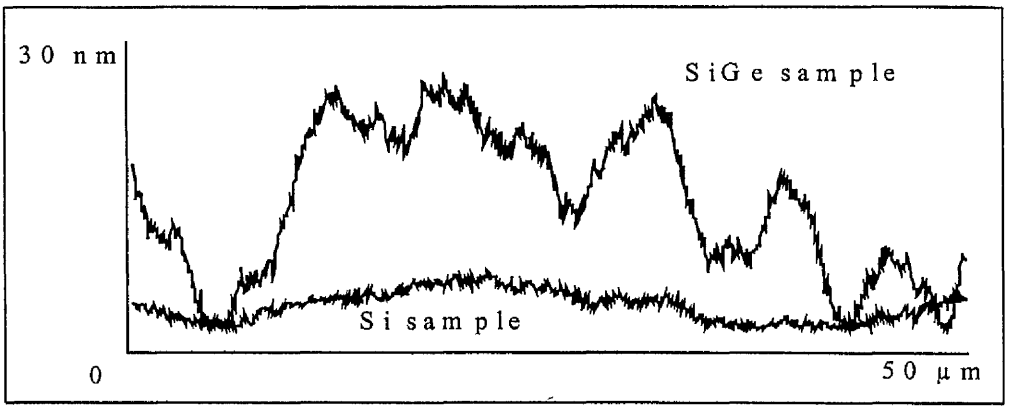

Figure 3.5 Typical surface profile trace of Si and SiGe.

3.5 Heterostructures of Si / SiGe

The minimum data required for a simple example of heterostructure formation are the band gap of the semiconductors and their conduction band (CB) or valence band (VB) discontinuity. The band gaps of Si and Ge at room temperature are 1.11 eV and 0.65 eV respectively. The band gap of unstrained SiGe, strained SiGe and strained Si [3.27] as a function of x is shown in figure 3.6. Valence band offset of Si_xGe_{1-x} on a Si_yGe_{1-y} substrate is shown in figure 3.7 [3.28].

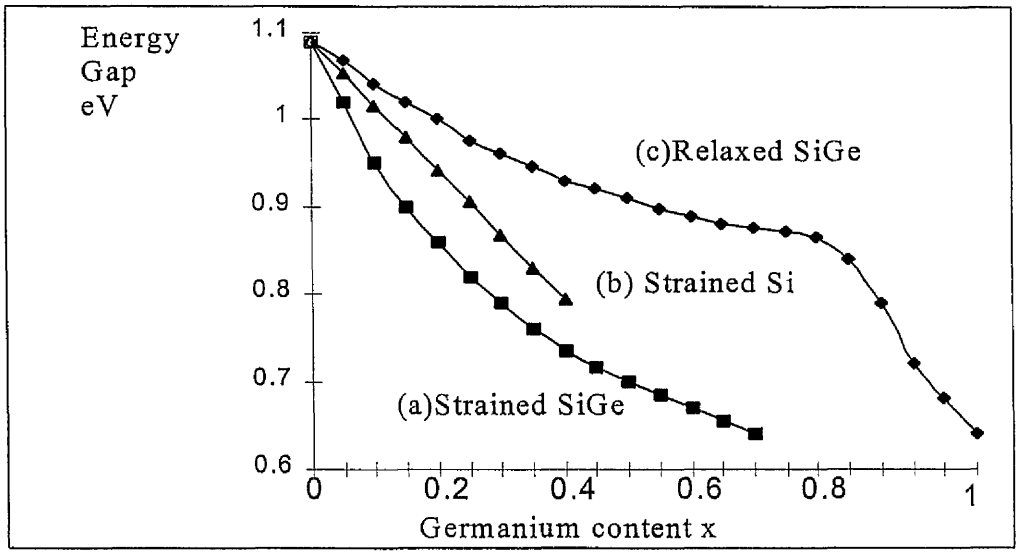

Figure 3.6 Band gap of (a) A SiGe layer on silicon (b) A Si layer on SiGe (c) A relaxed SiGe layer, R.People [3.27].

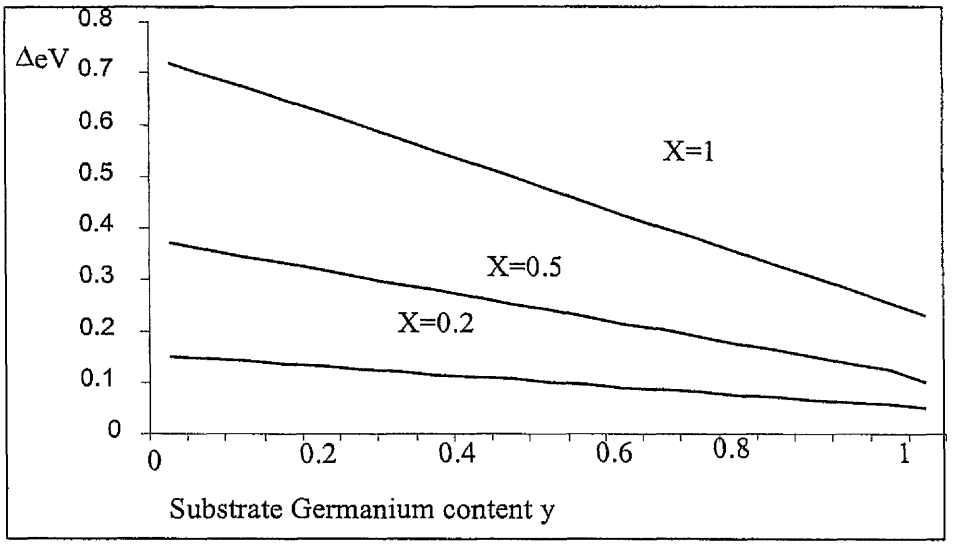

Figure 3.7 Valence band offset of strained SiGe.

A Simple Example

Consider the layer structure shown in figure 3.8, an undoped $Si_{0.8}Ge_{0.2}$ layer 20 nm thick is grown on a lightly doped n-Si substrate and is capped by a 10 nm thick undoped Si layer.

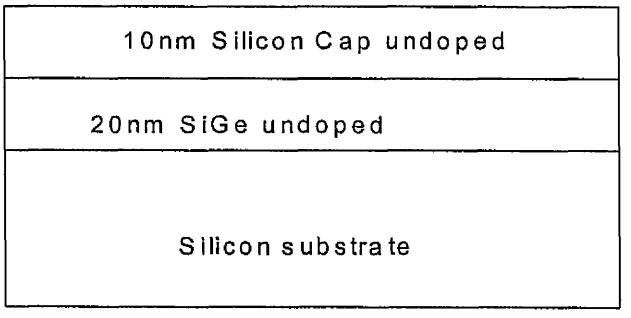

Figure 3.8 Simple Si/SiGe layer structure.

From figure 3.7 the valence band offset of $Si_{0.8}Ge_{0.2}$ on Si is 0.15 eV and figure 3.6 shows that the band gap of strained $Si_{0.8}Ge_{0.2}$ is 1.0 eV. The band diagram is drawn from right to left on figure 3.9a. First the silicon substrate band gap is drawn as straight lines separated by 1.1 eV representing the conduction and valence bands separated by the band gap. To add the $Si_{0.8}Ge_{0.2}$ layer, we know the valence band offset to be 0.15 eV so the $Si_{0.8}Ge_{0.2}$ valence band is drawn to the left of the Si valence band but 0.15 eV higher, the $Si_{0.8}Ge_{0.2}$ conduction band is then

drawn 1.0 eV above the valence band. The cap layer is the same as the substrate since the SiGe layer is less than the critical thickness and is not relaxed. The resulting band structure is shown in figure 3.9a, showing the narrow band gap SiGe layer that will confine the carriers and form the channel when a gate voltage is applied. Figure 3.9b shows the band diagram when the gate voltage forms a channel.

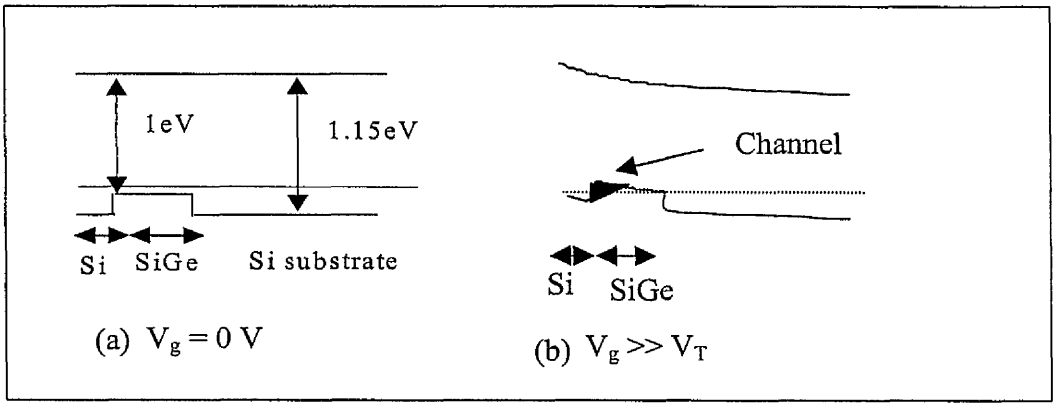

Figure 3.9 Resulting band diagram of simple example.

The above simple structure forms the basis of a buried channel enhancement mode p-SiGe channel MOSFET. The holes attracted by the gate potential are confined to the SiGe layer by the band discontinuity. Complete solutions for layer structures used in this work are given in chapter 4.

3.6 Transport Properties of Strained Layers of Si and SiGe

Strain can lift band degeneracy reducing the effective mass and intervalley scattering thereby increasing carrier mobility and effecting velocity field characteristics [3.28]. In the following two sections, only electron transport in strained silicon and hole transport in strained SiGe is considered as they are currently the most important for device considerations

3.6 (a) Strained Silicon

Silicon grown on a relaxed SiGe virtual substrate has tensile biaxial strain along the interface, resulting in the original six fold degenerate CB (E6) being split into two, the split bands are called (E2) and (E4) [3.29]. The (E2) band goes down in energy and the (E4) band goes up. E2 has an in plane light electron mass

of 0.19mo, and has lowest energy thus forming the quantum well. The electron mobility is enhanced because of the lower effective mass and the reduced intervalley scattering. Fischetti [3.30] recently predicted that electron mobility as high as 2300 cm^2/V-s is possible in strained silicon. The predicted values for electron mobility in strained silicon range from 900 cm^2/V-s [3.31] to 4000 cm^2/V-s [3.32] in the literature. The highest reported measured mobility's to date are 2830 cm^2/V-s [3.33], and 1840 cm^2/V-s [3.34]. Monte Carlo [3.35] simulation of the electron drift velocity show that no increase in electron saturation velocity is expected. However reasonable reduction in the onset field of velocity saturation is predicted [3.36]. Figure 3.10 shows calculated velocity field characteristics of electrons in strained silicon.

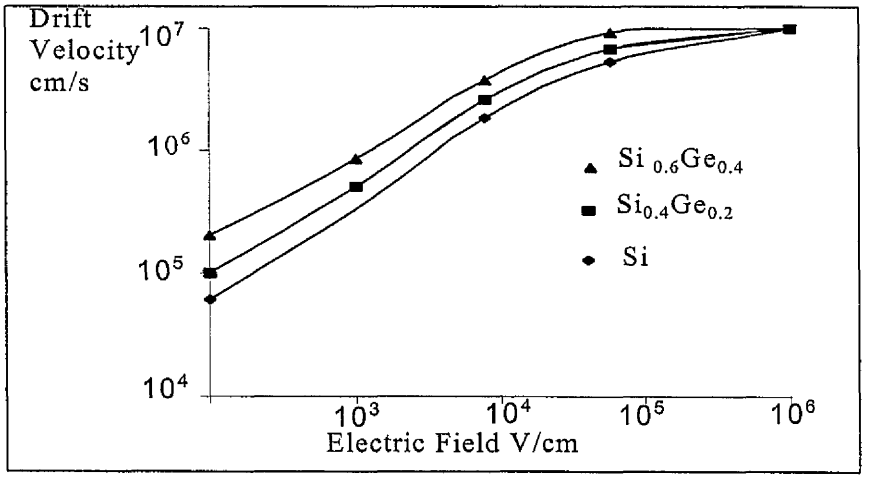

Figure 3.10 Velocity field characteristics of strained Si on relaxed SiGe.

3.6 (b) Strained Silicon-Germanium

The hole mobility is increased in strained SiGe by lifting the degeneracy of the valence bands, whereby the heavy hole band moves up and the light hole band moves down [3.37]. The mobility depends on the Ge content, in general more Ge means higher mobility. Hole mobility as high as 1100 cm^2/V-s [3.38] has been predicted. This is compared to the values of 500 cm^2/V-s and 100 cm^2/V-s for bulk silicon and a silicon inversion layer respectively. In 1994 an effective mobility of 220 cm^2/V-s was measured in a $Si_{0.75}Ge_{0.25}$ MOSFET [3.39], a factor of two greater than that in a similarly doped Si inversion layer. Very recently an

effective mobility in a $Si_{0.17}Ge_{0.83}$ channel MOSFET of 760 cm^2/V-s was reported [3.40]. For a MODFET, mobility as high as 1665 cm^2/V-s [3.41] for a pure Ge channel and 700 cm^2/V-s [3.42] for a $Si_{0.3}Ge_{0.7}$ channel, have been reported, which are close to the maximum theoretical values. Figure 3.11 shows the velocity field characteristic of holes in strained SiGe for different Ge content calculated by Hinckley and Sing [3.43]. It can be seen that for a given electric field, the drift velocity is greater for increased Ge content.

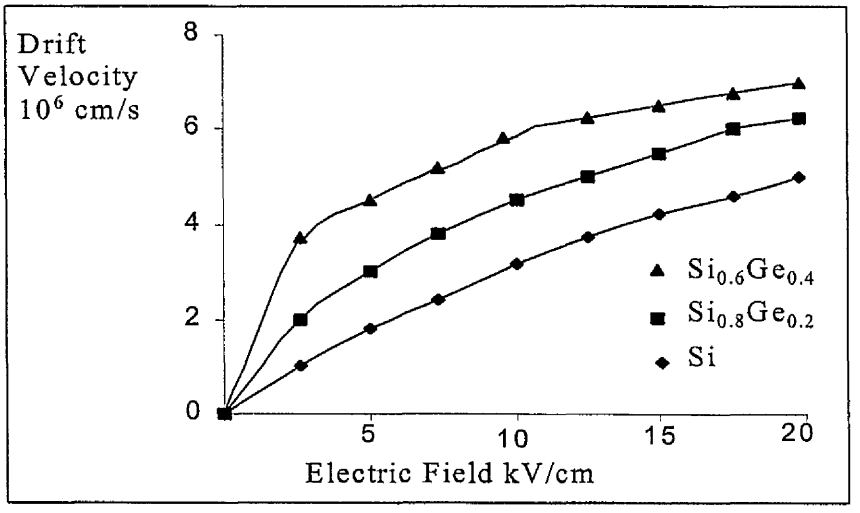

Figure 3.11 Hole velocity field characteristics in strained SiGe for various Ge content.

On the down side, there have been numerous publications citing the perils of surface roughness and alloy scattering [3.30][3.44]. In some cases totally cancelling mobility enhancement in both p and n channel devices. However the fact remains that increased mobility has been measured in real structures.

3.6 (c) Velocity Overshoot in Strained Silicon

As a result of the lower effective mass and reduced intervalley scattering previously discussed, velocity overshoot of electrons is expected to be stronger in strained silicon than in unstrained silicon [3.29]. Enhanced velocity overshoot has lead to predictions of better high-frequency performance [3.45] [3.46]. The simulation of high field effects in short gate length devices is carried out using Monte Carlo simulation techniques [3.35]. Early simulations by Miyata investigating velocity overshoot in strained silicon layers predict an overshoot peak of 4.1 x 10^7 cm/s [3.32].

3.7 Si / SiGe Devices

3.7 (a) Simulation

In 1994 device simulations using the same transport model of Miyata [3.32] show that for a 0.18 μm gate length device, the peak velocity in the channel is 2.6 x 10^7 cm/s [3.45]. Using a different transport model that results in a mobility of 3250 cm^2/V-s, Dollfuss simulates a peak electron velocity of 2.74 x 10^7 cm/s compared with 1.75 x 10^7 cm/s for unstrained silicon [3.46]. Resulting in a 0.08 μm gate length device with g_m of 405 mS/mm and f_T of 135 GHz. Other results such as that of Formicone [3.31], O'Neill [3.47] [3.48] and Roldan [3.49] show similar improvement for strained silicon over unstrained silicon.

A recent monte carlo study of an RF FET has been made by Roy [3.50] using the parameters of Yamada. This study attempts to describe the performance of a strained silicon MODFET optimised for RF properties and includes the effect of parasitic resistances. The resulting 120 nm gate RF FET has peak channel velocity approaching 2 x 10^7 cm/s with f_T of 77 GHz and f_{max} of 161 GHz. However by introducing an optimistic gate and source resistance of only 5 Ω the f_{max} is reduced to 68 GHz.

The high field performance of a strained silicon germanium p-channel device is somewhat inferior to that of electrons in strained silicon. Monte carlo studies of the high field hole transport in strained SiGe indicate that the velocity overshoot is evident, but considerably lower than that of electrons in strained silicon [3.51][3.52].

It is clear that there are still issues to be resolved in terms of the model used to predict transport parameters of strained Si and SiGe. In addition they may also be effected by local growth conditions in terms of surface roughnesss and alloy scattering. Results for device simulation must also include the effect of parasitic resistance and capacitance. Nevertheless the use of Si / SiGe layer structures to improve on the performance of sub 100nm silicon based FETs is the focus of much work. The next section reviews on the current state of the art results in actual device measurement

3.7 (b) State of the Art Devices

The following is a summary of figures of merit of the recent outstanding Si / SiGe field effect devices, beginning with n-channel devices.

3.7 (b) n-channel

The first strained Si n-channel FET reported by Deambkes in 1986 was a MODFET with a $TiSi_2$ schottky gate [3.7]. Since then the focus of n-channel devices has concentrated on fabricating FETs capable of operating at microwave frequencies. A schottky gate device is currently preferred because it can be fabricated directly onto a SiGe layer. It has been shown that the oxide formed directly on a SiGe layer is not suitable so a silicon cap layer is required [3.53]. The Si cap layer required for oxide growth reduces device performance (chapter 4). Depletion mode schottky gate MODFETs are mostly employed. Recently n-channel Si / SiGe MODFETs with very good microwave performance were reported. Table 3.1 summarises published results of recent n-channel Si / SiGe MODFETs and data from IBM on MOSFETs is shown for comparison.

	L (μm)	g_m (mS/mm)	f_T (GHz)	f_{max} (GHz)
Silicon IBM *[3.54]	0.1	650	150	30
Silicon IBM *[3.55]	0.18	350	50	30
O'Neill SiGe *[3.56]	0.15	220		
Konig SiGe[3.57]	0.18	476	46	92
Ismail SiGe[3.58]	0.4		40	56
Koester SiGe[3.59]	0.2	190	47	55

Table 3.1 n-channel MODFET performance * indicates MOSFET.

In comparing the above results it can be noted that in terms of transconductance and cut off frequency, the strained silicon devices are no better than the standard silicon devices. This is because of the use of the self-aligned silicide process to reduce parasitic source resistances in the standard devices of IBM. The demonstration strained silicon devices cited above are all fabricated

without a silicide, so it is difficult to make a direct comparison. Equally the SiGe devices with high f_{max} all have metal gates where the silicon standard device has polysilicon gate which is a reason for the difference in f_{max}. In all cases where a strained silicon demonstration device was fabricated with a silicon control device, significant improvement was shown to be the case.

3.7 (c) Strained SiGe p-channel Devices

The first SiGe p-channel MOSFET produced by Pearsal and Bean 1985 [3.5] was also a schottky gate device. In silicon CMOS circuits, the p-channel devices are made with twice the width of an n-channel device to compensate for the lower hole mobility. A key application for SiGe p-channel devices is to provide high transconductance MOSFET enhancement mode devices for symmetric operation of CMOS circuits thereby reducing packing density. As a result most of the effort on p-channel devices are MOSFETs. A number of centres have done work on implementing SiGe devices in a standard CMOS process [3.60][3.61].

Recently a cut off frequency of f_T of 70 GHz has been obtained by a p-channel SiGe MODFET with a schottky gate [3.62]. For a SiGe MOSFET, the best high frequency performance to date provided a cut off frequency of 23 GHz from a 0.2 μm gate length device [3.63]. Table 3.2 summarises recent SiGe p-channel device performance.

	L (μm)	g_m (mS/mm)	f_T (GHz)	F_{max} (GHz)
Silicon IBM * [3.54]	0.1	320	40	25
Silicon IBM [3.55]	0.18	200	20	20
Arafa [3.62]	0.25	258	70	55
Bhaumik * [3.63]	0.2	83	23	35
Ismail [3.64]	0.25	230	24	37

Table 3.2 p-channel device performance * indicates MOSFET.

3.8 Conclusion

By using epitaxial growth techniques, 2 DEGs and 2 DHGs can be grown, improving the carrier transport properties of silicon based devices. In addition the strain on silicon and silicon germanium layers leads to higher mobility and improves high field effects. High carrier mobility and lower onset for velocity saturation of holes in strained silicon germanium and electrons in strained silicon can be achieved. In addition velocity overshoot may be enhanced in sub 0.1 μm Si / SiGe devices. Excellent high-speed n-channel devices have been made employing a schottky gate on modulation doped structures operating in depletion mode. Some improvements over silicon devices have been shown for enhancement mode SiGe p-channel MOSFETs. Models predict that further improvement is possible. Symmetric CMOS circuits incorporating SiGe p-MOSFETs will become a possibility as silicon moves through the 0.1 μm barrier. If the advantage of velocity overshoot in strained silicon is to be exploited, parasitic resistances and capacitances must be nullified. High performance RF MODFETs incorporating strained silicon channels appear to be the next achievable goal.

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Chapter 4

Layer Structure Modeling and Design

4.1 Introduction and List of Symbols

The Si / SiGe layer structures used in this work are designed or analysed using a 1D Poisson solver. The theory of the self-consistent solution of charge density and potential in a semiconductor required for a full solution to the band diagram is discussed. Data on the band structure of unstrained SiGe, unstrained Si, strained Si and strained SiGe are shown. The 1D Poisson solver is then used to design an optimum layer structure for a SiGe p-channel MOSFET. The material made available to fabricate n-channel strained Si MODFET is analysed and improved. Some background to ion implantation is discussed before the implant conditions are designed. The gate metals chosen to fabricate the p and n-channel devices are discussed.

List of Symbols

∇^2 Laplacian Operator

ΔE_c Conduction band offset relative to silicon

ΔE_v Valence band offset relative to silicon

ε Dielectric constant

ε E_c Conduction Band energy

E_f Fermi Level energy

E_g Band Gap Energy

E_v Valence band energy

h Planck's constant

k Boltzmann's constant

M_{lh}-Dos Light hole effective mass

M_e-dos Electron effective mass

m mass

M_{hh}-Dos Heavy Hole effective mass

N_c Density of states conduction band

n electron density

N_d donor atom density

Na acceptor atom density

N_v Density of states in valence band

ρ Charge density

p hole density

q magnitude of electron charge

T Temperature

V Applied voltage

4.2 1D Poisson Solver

A graphical technique was used in chapter 3 to work out the band diagram of a given layer structure, ignoring the effects of charge. For a complete solution the Poisson equation [4.1] which describes the relationship between charge density and potential must be solved. The Poisson equation is

$$\nabla^2(V) = -q\,\rho \tag{4.1}$$

In a semiconductor the charge density is given by

$$\rho = (p - n + N_d - N_a) \tag{4.2}$$

Using Boltzmann statistics [4.2]

$$n = N_c \exp \frac{(E_f - E_c)}{kT} \tag{4.3}$$

and

$$p = N_v \exp \frac{(E_v - E_f)}{kT} \tag{4.4}$$

In typical semiconductor structures, the solution to the above equations require numerical modeling. In this work, a 1D Poisson solver available on shareware from Greg Snider of the University of Notre Dam is used. This solver uses the method of finite difference [4.4] to find the 1D band diagram by self consistently solving the Poisson equation with Boltzmann statistics or with the Schrodinger equation. For the simulations used in this work there was no notable difference between using the Boltzmann or Schrodinger equation.

4.3 Data used for Si and SiGe

An important point especially in the case of SiGe simulation is that any model is only as good as the data that is put into it. Table 4.1 shows the formula and values input to the model in this work. The table was supplied by the device modelling group at the University of Glasgow.

	Si [4.5	SiGe [4.6]	Si on SiGe [4.7]	SiGe on Si [4.8]
Eg	1.12 a	$1.15-0.43x+0.02x^2$	$1.11-0.74x$	$1.17-0.90x+0.40x^2$
Δec	0		-0.67x	
Δev	0			0.74x
ε	11.9	$11.9+3.03x+1.05x^2$	11.9	$11.9+3.03x+1.05x$
Mhh-	0.951	$0.94-1.44x+1.15x^2$	$0.94-2.67x+2.84x^2$	$0.93-2.23x+1.83x^2$
Mlh-Dos	0.256	$0.25-0.51x+0.40x^2$	$0.26+0.54x-0.28x^2$	$0.25-0.33x+0.21x^2$
Me-dos	0.321	0.321	0.328	0.342

Table 4. 1 Data used in 1D poisson solver.

4.4 1D Band Diagram Simulation

4.4 (a) p-channel layer structure

Many early SiGe enhancement-mode MOSFETs used a simple layer structure that will be analysed next, and is shown in figure 4.1. The simulated band diagrams for 3 gate voltages are shown in figure 4.2. A graph of the peak hole density in the channel and in the cap layer versus gate voltage is shown in figure 4.3.

5 nm Si Cap Layer Undoped
20 nm $Si_{0.8}Ge_{0.2}$ Undoped Channel
Si Substrate n-type 10 Ω-cm

Figure 4.1 Simple structure for SiGe p-channel MOSFET.

As figure 4.2 shows, at low or zero gate voltage the bands are relatively flat and there are no holes in the channel. At increased gate voltage the bands are bent upwards and the channel is populated. Further increase in the gate voltage leads to significant hole population in the cap layer. The current due to the holes in the cap layer is called parallel conduction. Parallel conduction should be minimised because the cap layer has much lower mobility. A figure of merit for parallel conduction is the cross over voltage, which is defined as the gate voltage above threshold at which the carrier density in the cap layer exceeds that of the intended channel layer. For the above structure, figure 4.3 shows that the cross over voltage is –0.5 V. The low cross over voltage of –0.5V means that this structure is unsuitable for a realistic MOSFET because the advantage of the SiGe channel is lost at gate voltages exceeding the cross over voltage. To obtain a more suitable structure, a larger crossover voltage is required to minimise parallel conduction.

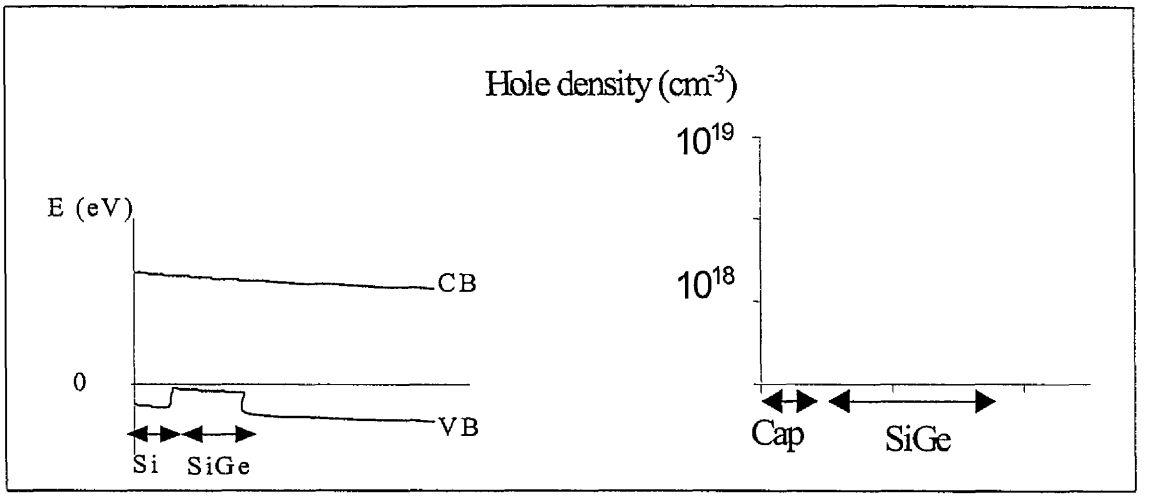


Figure 4.2 (a) $V_g - V_t = 0$ V

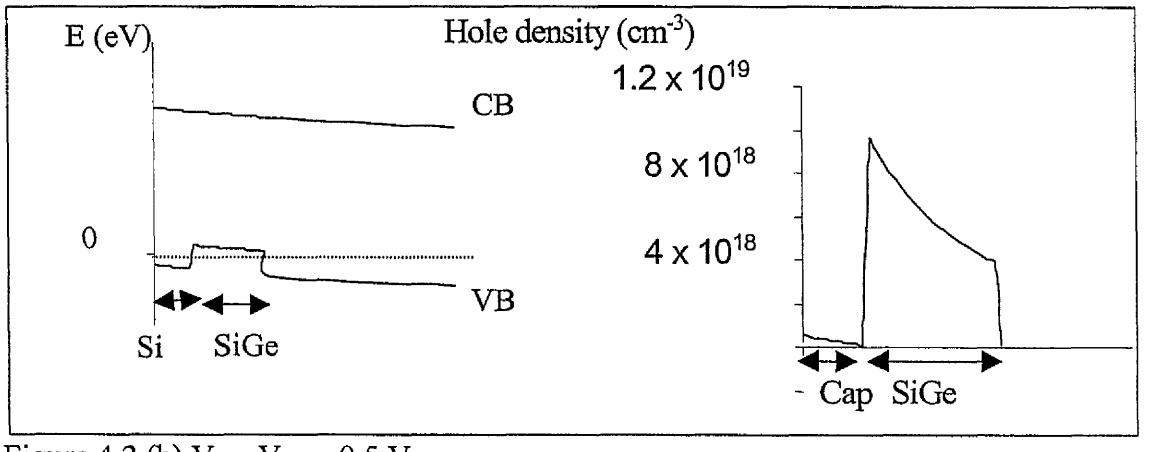


Figure 4.2 (b) $V_g - V_t = -0.5$ V

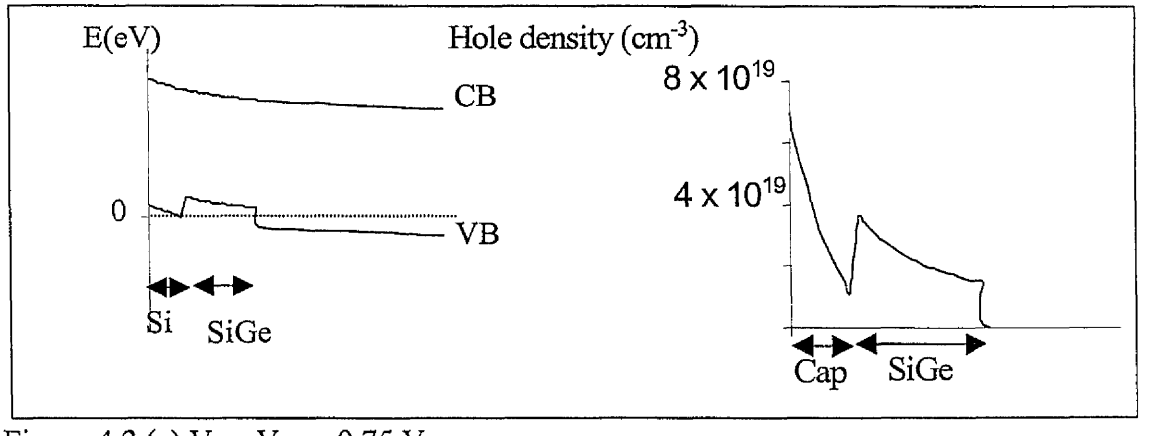


Figure 4.2 (c) $V_g - V_t = -0.75$ V

Figure 4.2 Band diagrams and carrier concentration for simple p-SiGe MOSFET structure.

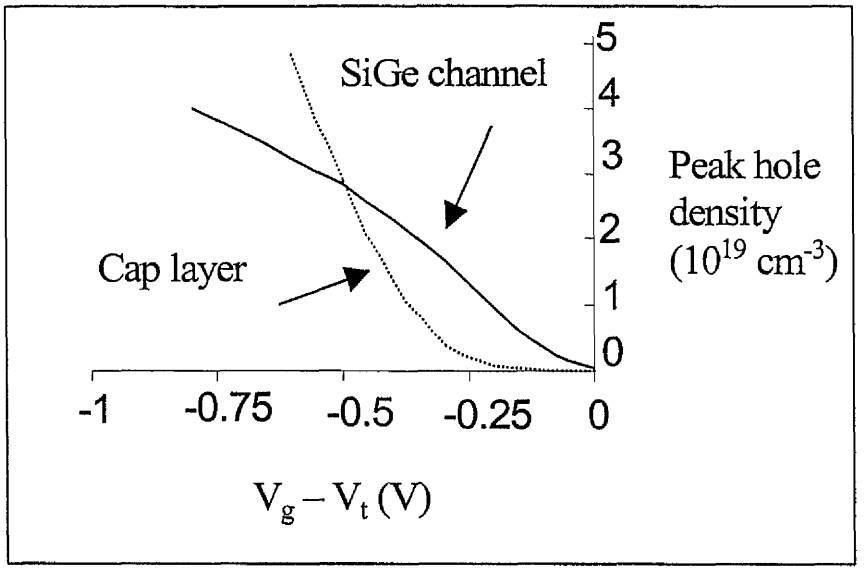


Figure 4.3 Layer hole density versus gate voltage for the simple p-channel structure.

Design of an improved layer structure

An improved layer structure should have a large cross over voltage so that the holes are confined to the SiGe layer and there is no parallel conduction in the silicon cap layer. A high Ge content in the channel is desirable to obtain highest mobility and largest valence band discontinuity. However the maximum Ge content is limited by epitaxial growth considerations such as the critical thickness. Grading the Ge content of the channel and using triangular Ge profiles has been shown to increase carrier confinement and hole mobility [4.9] [4.10] [4.11]. After simulations to optimise the cross over voltage, an improved vertical structure was designed and is shown in figure 4.4. The simulations were carried out with a maximum Ge content of 0.4.

10 nm Si Cap Layer Undoped
5 nm Graded from $Si_{0.6}Ge_{0.4}$ to Si
10 nm Graded from $Si_{0.9}Ge_{0.1}$ to $Si_{0.6}Ge_{0.4}$ Undoped
2 nm Graded from Si to $Si_{0.9}Ge_{0.1}$ Undoped
200 nm Si n-type 1.5×10^{17}
Si Substrate

Figure 4. 4 Improved enhancement mode strained SiGe p-channel structure.

Figure 4.5 shows the band diagram and the carrier concentration as a function of depth for a gate voltage of –1 V. At –1 V all of the carriers are still confined to the SiGe channel. The cross over voltage achieved with this structure is –1.5 V as shown in figure 4.6.

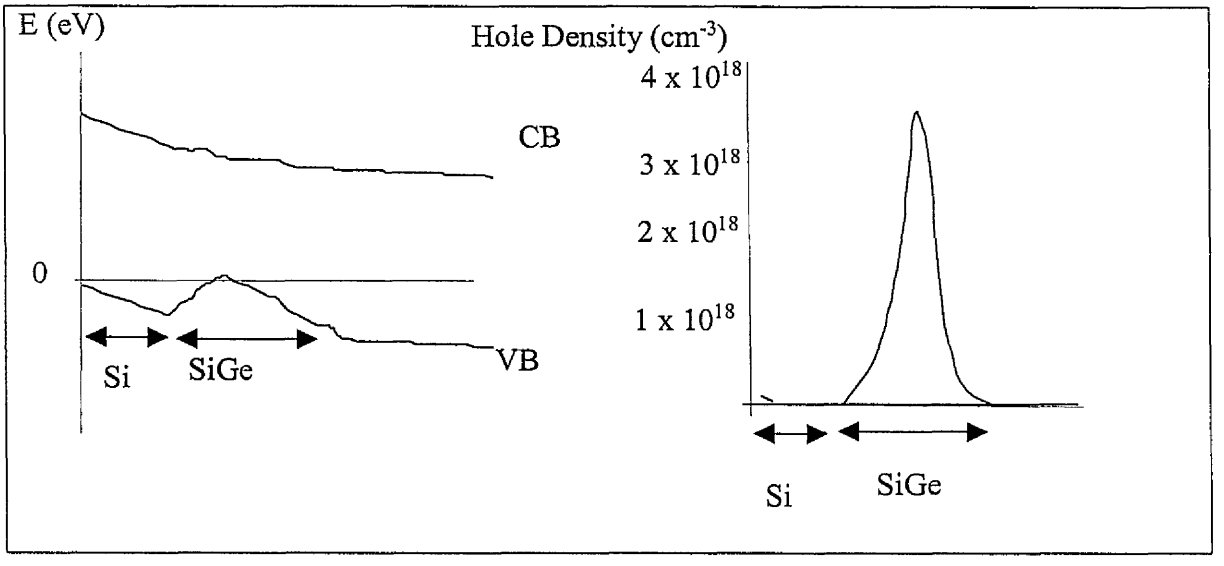


Figure 4.5 Band diagram and carrier concentration versus depth at –1 V for the improved p-SiGe structure.

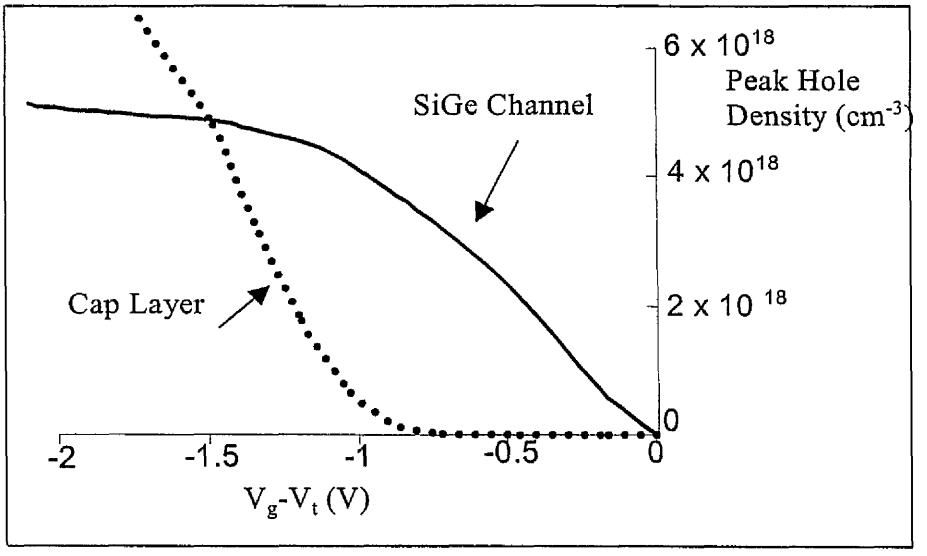


Figure 4 .6 Layer hole concentration for improved p-channel structure.

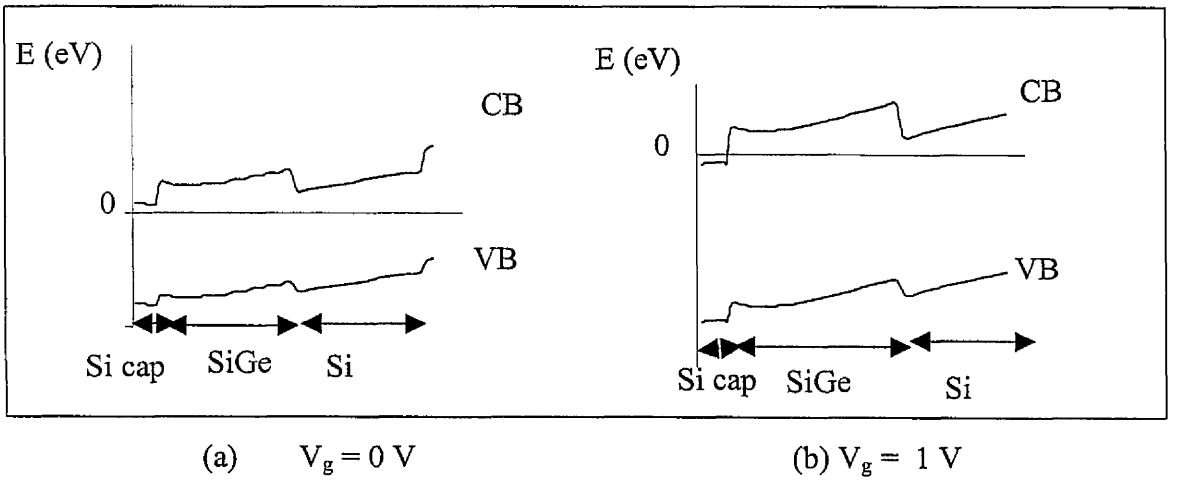
4.4 (b) n – channel

For the fabrication of the n-channel devices in this work, it was not possible to design a layer structure and have it grown. However the material structure of figure 4.7 was made available by the defense evaluation research agency (DERA) for device fabrication. The simulation was carried out assuming a 6 nm oxide layer thermally grown on the structure.

10 nm Si Cap Layer Undoped
5 nm $Si_{0.75}Ge_{0.25}$ n-type 5 x 10^{19}
5 nm $Si_{0.75}Ge_{0.25}$ Spacer Undoped
10 nm Si Channel Undoped
200 nm $Si_{0.75}Ge_{0.25}$ p-type 5 x 10^{17}
1 μm graded $Si_{0.75}Ge_{0.25}$ Virtual Substrate p-type 5 x 10^{17}
Si substrate 1 – 2 Ω–cm p-type

Figure 4. 7 Supplied Layer structure for n-channel devices.

Figure 4.8 shows the band diagram for this structure at 0 V and 1 V. Devices fabricated on this structure will be enhancement mode with all of the carriers in the cap layer. The layer carrier density versus gate voltage is shown in figure 4.9.



(a) $V_g = 0$ V (b) $V_g = 1$ V

Figure 4. 8 Band Diagram of supplied n-channel structure DERA#1 for (a) $V_g = 0$ V and (b) $V_g = 1$ V.

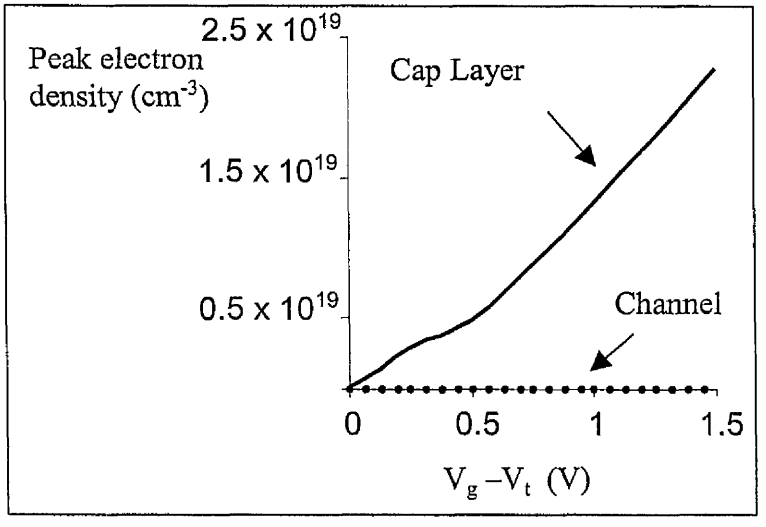


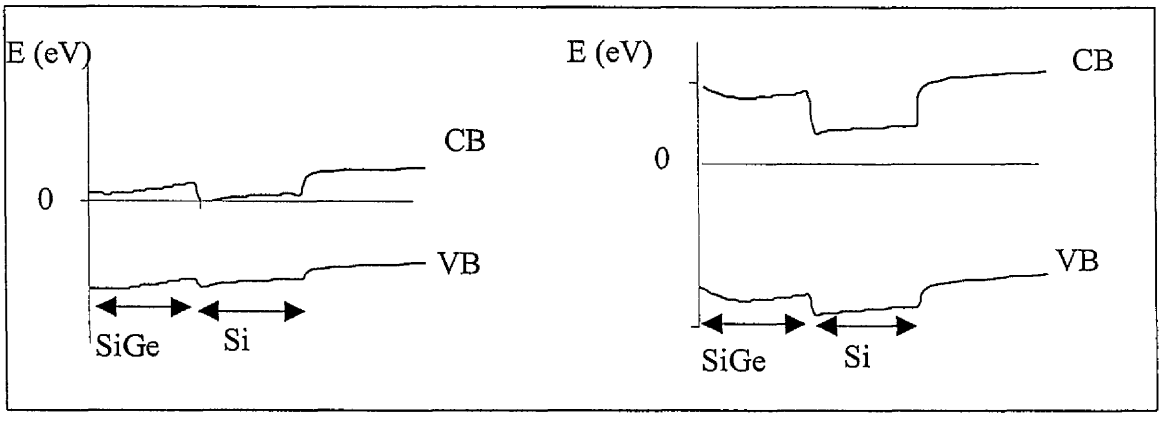
Figure 4.9 Layer electron density versus gate voltage for DERA#1 n-channel structure.

The enhancement mode operation of this device is confirmed by measurement (chapter 5). A depletion mode structure of similar profile would have been preferred. Simulations using the 1D Poisson solver confirmed suspicions that the p-doped buffer layer was responsible for the enhancement mode of operation. A new but similar layer structure incorporating an undoped buffer layer is shown in figure 4.10.

5 nm $Si_{0.75}Ge_{0.25}$ n-type 1 x 10^{19}
5 nm $Si_{0.75}Ge_{0.25}$ undoped spacer
10 nm Si undoped channel
100 nm $Si_{0.75}Ge_{0.25}$ undoped setback
1 μm virtual substrate graded to $Si_{0.75}Ge_{0.25}$ p-type 5 x 10^{17}
Si substrate 1 – 2 Ω–cm p-type

Figure 4. 10 Optimised depletion mode n-channel structure.

This structure was simulated without a silicon cap layer. Figure 4.11 shows the band diagram at 0 V and –0.75 V for the above structure indicating that the device will work in depletion mode. Figure 4.12 shows the carrier concentration in the Si channel and SiGe supply layer as a function of applied gate voltage.



(a) $V_g = 0$ V (b) $V_g = -0.8$ V.

Figure 4.11 Band diagram showing depletion mode operation in optimised n-channel structure with no silicon cap layer for (a) $V_g = 0$ V and (b) $V_g = -0.8$ V.

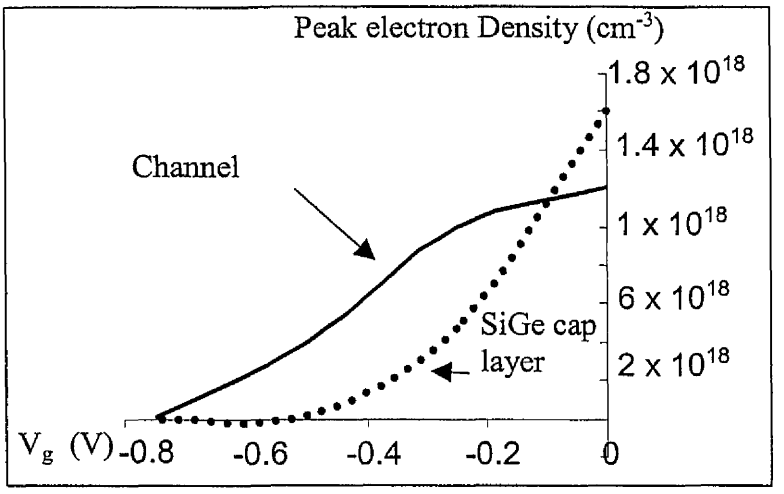


Figure 4.12 Layer carrier densities versus gate voltage for optimised n-channel structure with no silicon cap layer.

From a practical point of view a silicon cap layer is required to allow the growth of the gate oxide on, unless a schottky contact is used. If a 3 nm cap layer is added the structure is still suitable for a depletion mode device but most of the carriers are in the cap layer as shown by figure 4.13. The use of a schottky gate instead of a MOS gate will allow the fabrication of devices with no Si cap layer. This simulation illustrates why the n-strained Si channel devices reported to date have all used a schottky gate.

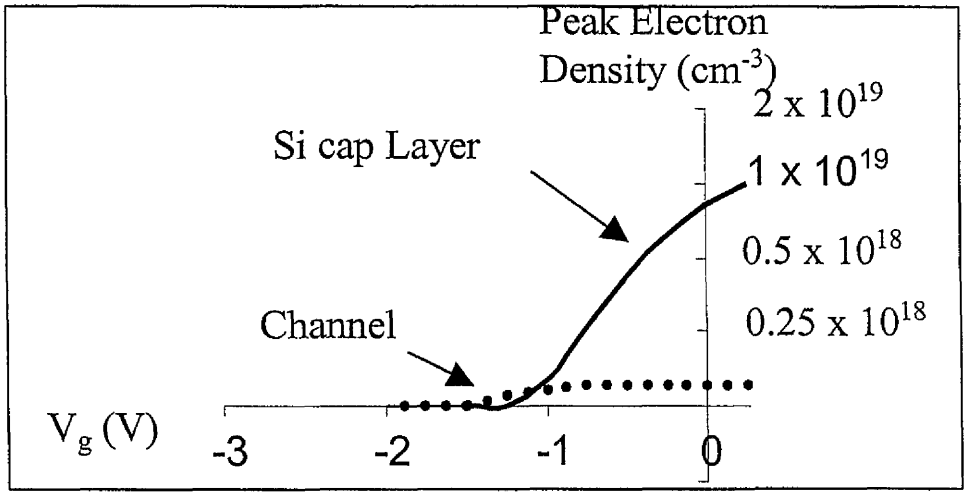


Figure 4.13 Layer carrier density for optimised n-channel structure with a 3 nm cap layer.

4.5 Ion Implantation.

The following simple method was used to obtain the doping profile and ion implant conditions for the source and drain implants.

As the ions penetrate into the substrate they lose energy in collisions with electrons and atomic nuclei and eventually come to rest. The distribution of implanted ions in depth into the substrate can be approximated by [4.12].

$$n(x) = \frac{S}{\Delta R_p \sqrt{2\pi}} \exp \frac{-(x - R_p)^2}{2\ \Delta R_p^{\ 2}} \qquad (4.5)$$

Where

S is the ion dose per unit area (cm^{-2})

ΔR_p is the projected straggle of implanted ions (μm)

R_p is the projected range of implanted ions (μm)

A dose of 5×10^{15} cm^{-2} was used for all implants in this work.

The projected straggle and projected range for the three implant conditions used in this work are shown in table 4.2.

Ion	R_p (μm)	ΔR_p (μm)	Energy (keV)
B	0.03	0.015	10
P	0.028	0.015	20
P	0.05	0.022	40

Table 4.2 Ion implant conditions [4.13].

4.5 (a) p channel ion implant simulation

Since minimum gate length transistors were to be fabricated, short channel effects must be avoided by using very shallow source drain junctions. The minimum energy available to the project is 10 keV. Figure 4.14 shows the simulated boron concentration as a function of depth into the sample.

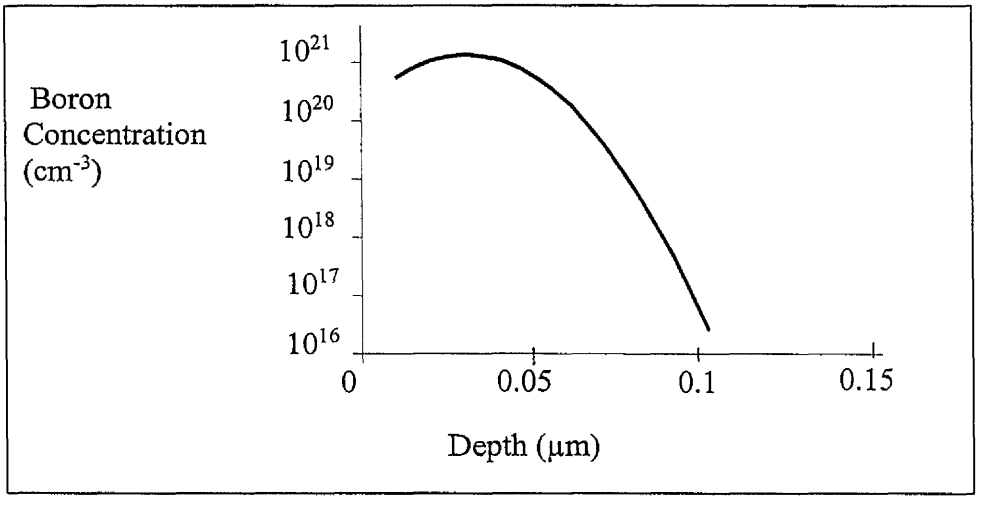


Figure 4.14 Concentration of Boron atoms versus depth into silicon for 10 keV, 5 x 10^{15} cm^{-2} implant.

4.5 (b) (i) n-channel ion implant simulation

For the n-channel source and drain phosphorous is the chosen ion species. A low temperature (600 °C) anneal can be sufficient to activate the implant if P is used [4.14]. Figure 4.15 shows the P concentration as a function of depth into the sample for 2 implant energies used in this work.

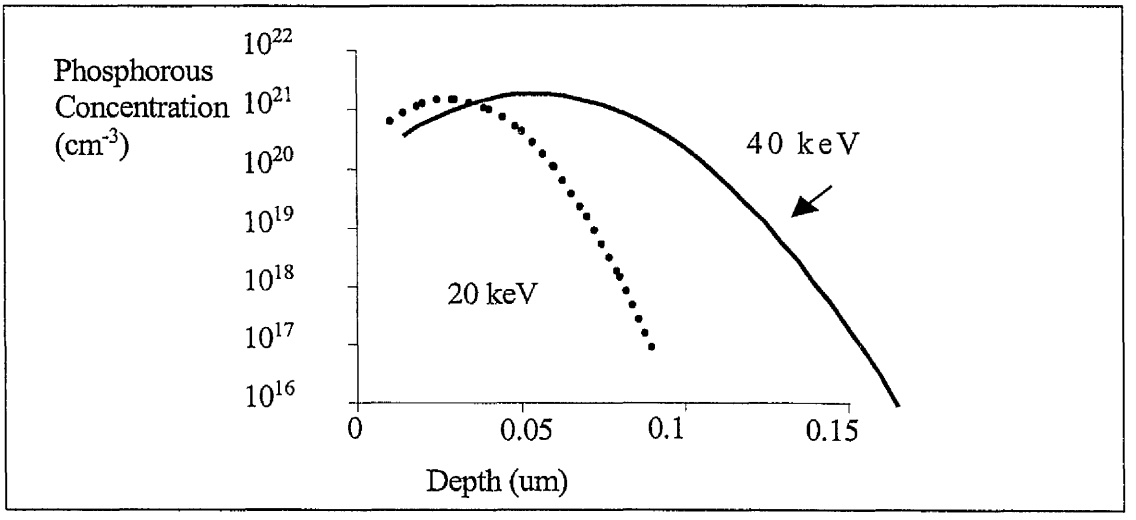


Figure 4.15 P doping concentration for 20 keV and 40 keV implants.

4.6 Gate Metals

For the p-channel device by using a BF_2 implant, an anneal at 900 °C for 10 s is required to obtain a reasonable contact resistance [4.14]. The only metal available to the author for this purpose is tungsten. Using tungsten as a gate metal is not new and there has been recent interest in employing tungsten as a gate metal for short channel CMOS processes [4.15] [4.16] [4.17]. The main problem with using tungsten is the need to find a way to etch the tungsten without etching into the thin gate oxide. This is overcome by in-situ monitoring of the etching process (chapter 5).

For an n-channel device where P doping is used, it is possible to anneal at only 600 °C for 20 s to obtain reasonable contact resistance. This allows more flexibility in the choice of gate metal. In order to take advantage of the technology available at Glasgow, Ti / Pd / Au is the chosen gate metal for the n-channel devices. At Glasgow there exists a mature fabrication process for Ti / Pd / Au gate devices down to sub 100 nm gate length and using T shaped gates. Using this technology would save time in developing new metalisations and allow for a direct

comparison with state of the art GaAs MODFETs. Gold is of course an unpopular metal in silicon fabrication for two reasons [4.18].

1. It diffuses rapidly in silicon.
2. It acts as a deep trap reducing mobility and reliability.

However gold interconnects have been considered recently [4.19]. All of the n-channel SiGe devices reported in chapter 3 had gold gates. Gold drain and source alloyed contacts are becoming common place in demonstration devices [4.20]
It was perhaps a bold choice but the benefits outweigh the disadvantages considerably. It will be possible to transfer the technology to a tungsten or even aluminium gate process.

4.7 Conclusion

An optimum Si / SiGe p-channel layer structure was designed using a 1D Poisson solver. The n-channel structures available for this work were analysed using a 1D Poisson solver. Using feedback from the results of fabricated devices on the initial layer structure, an optimised strained Si n-channel structure is designed. Ion implantation conditions are modelled for the p and n-channel devices using a simple Gausian approximation.

Tungsten is chosen as the gate metal for p-channel devices because of its ability to withstand high temperatures.

Ti / Pd / Au is to be used as the gate metalisation for n-channel devices in order to make full use of the mature microwave device fabrication facilities available.

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CHAPTER 5

Fabrication and DC Analysis of Metal Gate Si / SiGe MOSFETs

5.1 Introduction

The fabrication processes and results of DC characterisation of metal gate MOSFETs are presented in this chapter. The first fabrication process developed was for the tungsten gate p-channel SiGe MOSFETs. The simple fabrication process is first shown by diagram then individual processing steps are described in detail. Basic DC characterisation of the resulting devices follows. A modified process designed for the fabrication of Ti / Pd / Au gate n-channel SiGe MOSFETs is then described and is also followed by DC characterisation of the resulting devices.

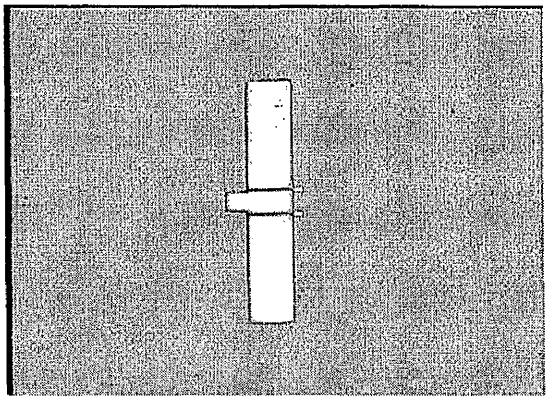

Image of a 2 finger gate with ohmic contacts

5.2 Tungsten Gate SiGe p-channel MOSFETs

5.2 (a) Fabrication process

The first devices to be fabricated in this work were tungsten gate SiGe p-channel enhancement mode MOSFETs as designed in chapter 4. A simple fabrication process was designed that would provide quick results. Figure 5.1 is a diagram of the fabrication process. There are four lithographic levels to define the alignment marks, gate, ohmic contacts and to give isolation as shown in figure 5.2.

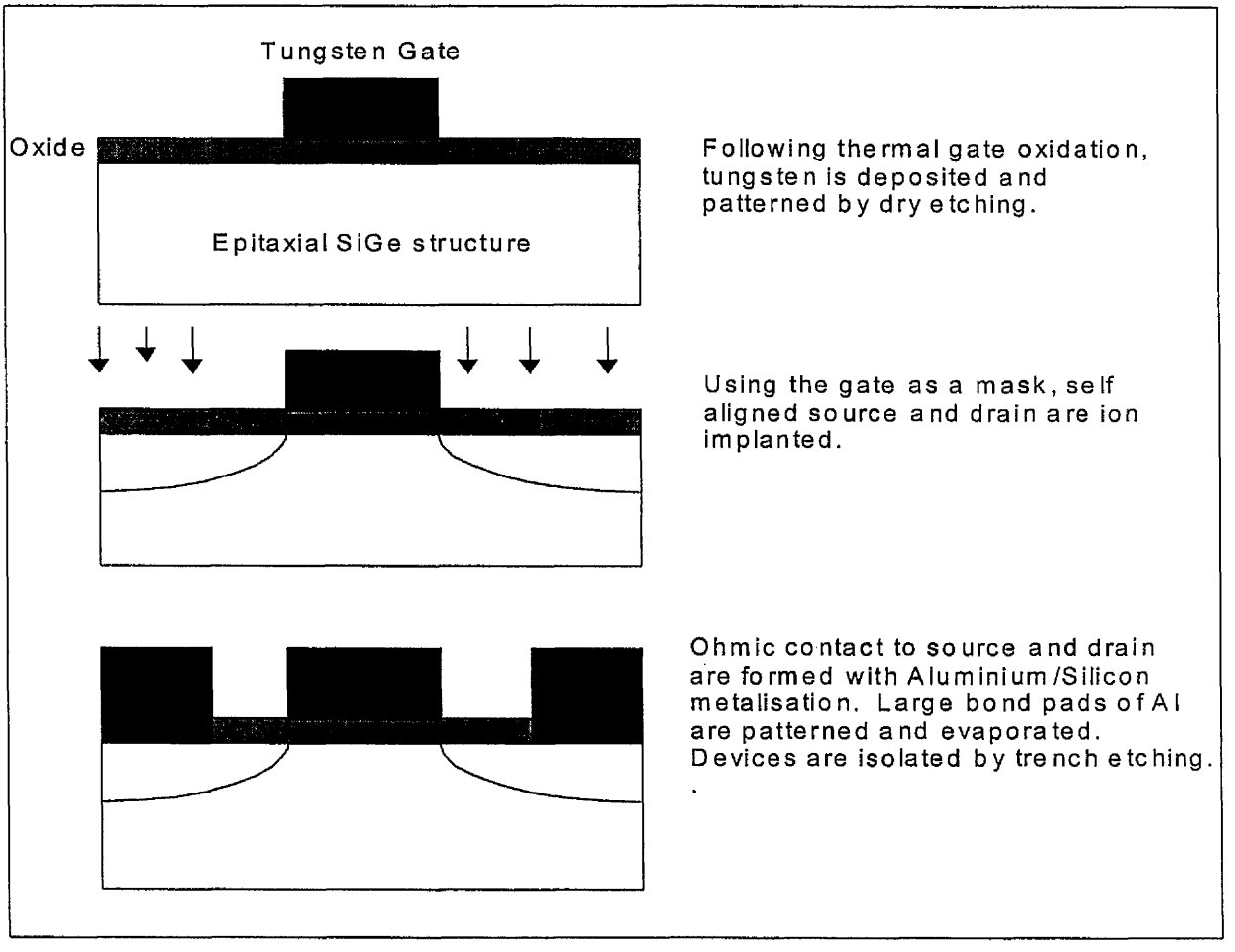

Figure 5.1 Simple Fabrication process for tungsten gate devices.

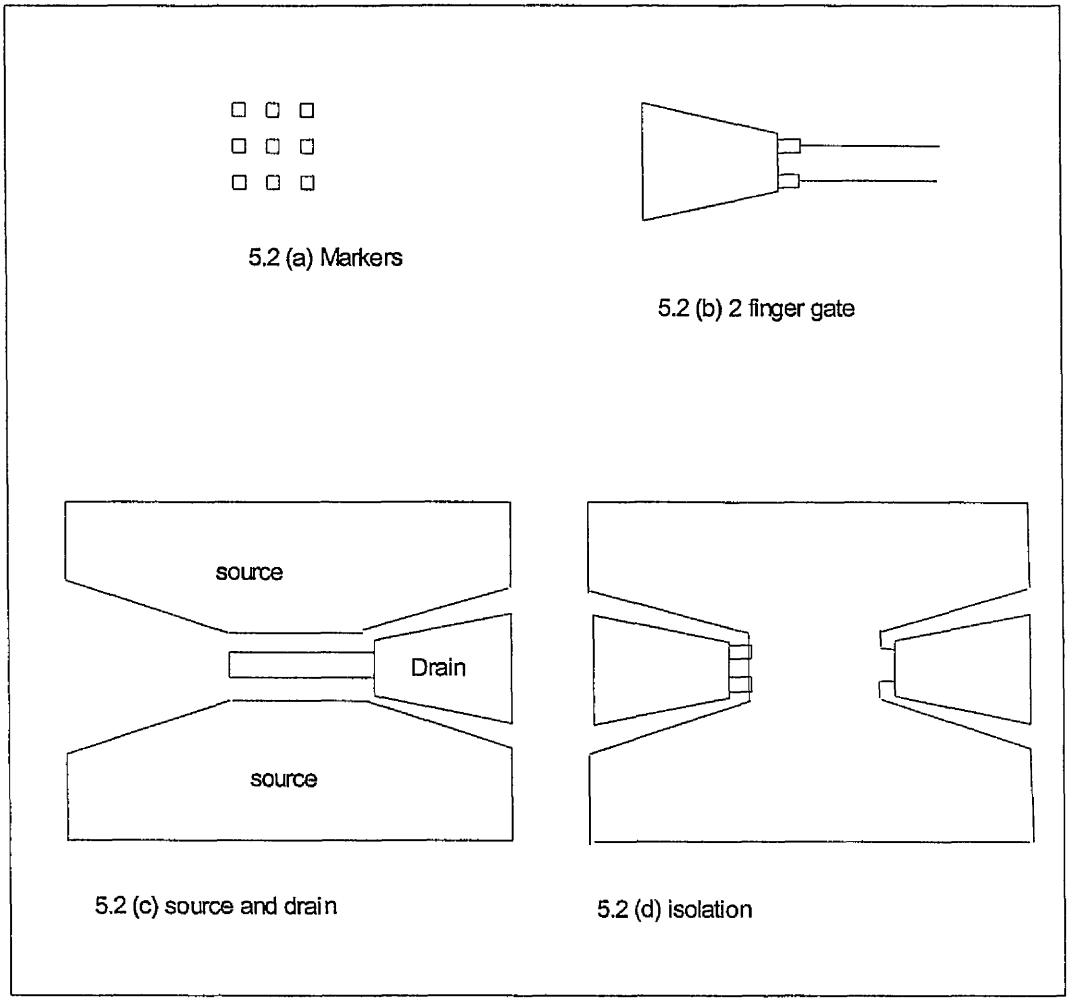

Figure 5.2 Mask layout Used in the Fabrication of Tungsten gate MOSFETs.

5.2 (b) Processing Steps

5.2 (b) (i) Gate Oxidation

Thermal gate oxidation was carried out by placing the samples in a cylindrical furnace maintained at 800 °C with flowing dry oxygen at a flow rate of 2 sccm for 120 mins. The resulting oxide thickness was measured using ellipsometry [5.1] and was found to be 6 nm. Following oxidation the wafers were annealed for a further 30 min at 800 °C in an argon atmosphere. This is known to reduce the high density of fixed oxide charges that are present as a result of growing the oxide at low temperature [5.2]. Large area (1 mm^2) MOS capacitors with Al and W gate metals were fabricated to characterise the oxide. CV curves of the capacitors were measured using an HP4275-A multi frequency LCR meter with a small signal frequency of 1 MHz. Figure 5.3 shows a typical CV curve obtained from such a measurement. Estimates of fixed oxide charge density is easy to obtain and provides a figure of merit for oxide quality. Gate leakage will be considered during device characterisation. The fixed oxide charge density is given by [5.3]

$$Q_f = C_o (V_{ms}-V_{fb}) \qquad (5.1)$$

Where V_{fb} is the flatband voltage shift of the CV curve, figure 5.3 and table 5.1.

V_{ms} is the metal-semiconductor work function difference, table 5.1.

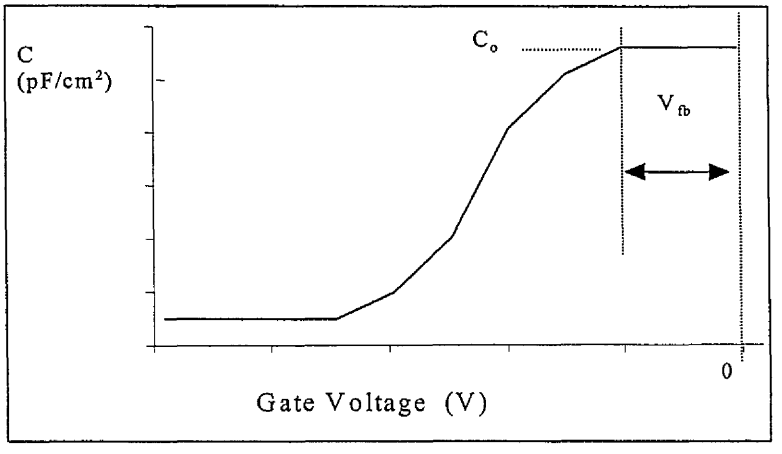

Figure 5.3 Typical CV curve measured at 1 MHz of an Oxide on n- Si

Table 5.1 shows the fixed oxide charge densities of thermal oxides grown at 800 °C and 1100 °C on a n-doped silicon substrate. Industry standard thermal oxidation processes produce oxides with fixed charge densities of $< 10^{10}$ cm^{-3} [5.4]. The fixed oxide charge density as fabricated here is not ideal but is suitable for initial demonstration device fabrication.

Oxidation Temp (°C)	Thickness (nm)	Metal	V_{ms} (V)	V_{fb} (V)	Anneal	Q_f x10^{-10} (cm^{-2})
1100	20	Al	-0.25	-0.5	None	4.3
800	6	Al	-0.25	-0.6	None	22
800	6	Al	-0.25	-0.35	800 °C for 30 min	6
800	6	W	+0.65	+0.55	800 °C for 30 min	6

Table 5.1 Fixed oxide charge densities of Al, Au and W gate MOS capacitors with oxide grown at low and high temperature.

5.2 (b) (ii) Tungsten Gate Deposition

The tungsten gate metal was deposited by sputtering using a single target conventional Nordiko RF sputtering system. Figure 5.4 is a schematic diagram of the sputtering method. A low-pressure argon gas RF discharge is set up between the tungsten target and the substrate. The argon atoms in the plasma are accelerated towards the target and sputter the tungsten. The sputtered tungsten atoms accelerate towards the substrate through the argon plasma and are deposited onto it. Some argon is trapped in the tungsten during the sputtering process and its presence increases the resistivity of the deposited layer [5.5]. In order to avoid this, a very low argon gas pressure of 2 mTorr was used. The chamber background pressure was 2 x 10^{-6} mbar and the DC target bias was –1100 V resulting in a deposition rate of 3 nm/min and applied RF power of 100W.

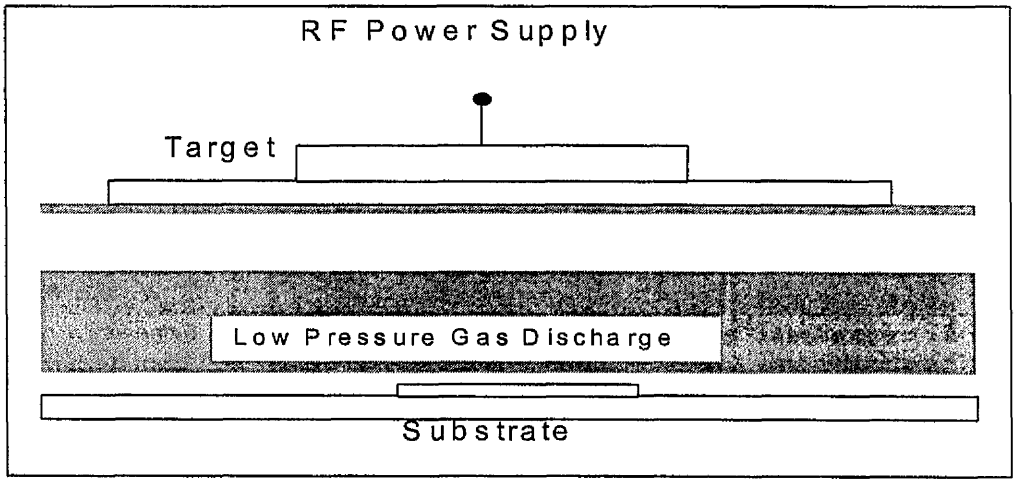

Figure 5.4 Schematic diagram of sputtering system.

The resistivity of the deposited tungsten layer was measured using a Leighton Buzzard 4-probe resistance measurement system. Four probes of 25 μm tip radius that are spaced 1 mm apart make contact with the wafer, the sheet resistance is given by [5.6].

$$Rsh = 4.532 \times V / I \quad \Omega / sq \qquad (5.2)$$

The measured sheet resistance of the deposited tungsten was 1.2 Ω / sq.

5.2 (b) (iii) Tungsten Gate Lithography

The sample was baked on a hotplate at 200 °C for 30 min, then hexamethyldisilazane (HMDS) was spin coated onto the sample at 3000 rpm for 30 s, and then the sample was oven baked at 80 °C for 20 mins. Hoeschst AZ PN114 resist was diluted 1:1 with Hoechst EBX thinner then spin coated onto the sample at 3000 rpm for 30 s [5.7]. Immediately afterwards the sample is softbaked at 120 °C for 120 s on a vacuum hot plate. A range of gates with minimum gate length of

100 nm, were written using a Leica EBPG5 electron-beamwriter onto the Hoechst AZ PN114 negative tone resist. The pattern was exposed with an electron beam of energy 100 keV with a spot size of 40 nm and a dose of 24 $\mu C/cm^2$. Following exposure the sample was baked at 105 °C for 5 min then developed at 20 °C for 60 s in Hoechst AZ400K developer diluted 1:4 with RO water.

5.2 (b) (iv) Tungsten Gate etch

One of the major roadblocks in using tungsten as a gate metal for short channel MOSFETs is that an etching process that is selective between the tungsten and the underlying gate oxide is not available [5.8]. However, using in-situ reflectometry [5.9] the etch depth can be monitored during the etching process allowing the process to be stopped at a predetermined point. In reflectometry, laser light is shone onto and reflected from the surface being etched. The intensity of the reflected light is measured. As the top layer gets thinner and interfaces are etched through, the intensity of the reflected light changes. The reflection coefficient and hence the amplitude of reflected light can be modelled using transmission line theory. The following is an example for a two-layer structure, the theory is easily extended to multilayer structures.

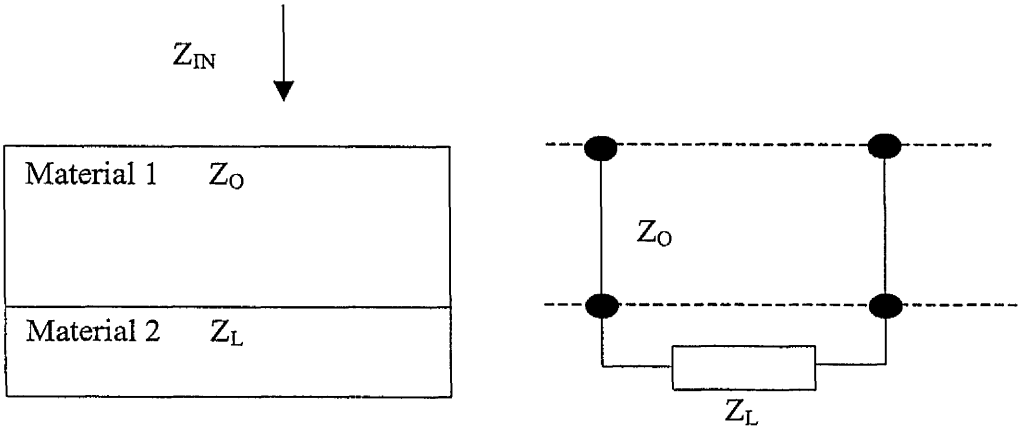

Figure 5.5 Model of a 2 layer structure for calculation of the reflection coefficient.

$$Z_{in} = Z_o \frac{(Z_L + Z_o \tanh(\gamma L))}{(Z_o + Z_L \tanh(\gamma L))} \tag{5.3}$$

$$\rho = \frac{(Z_L - Z_o)}{(Z_L + Z_o)} \tag{5.4}$$

Where L is the thickness of the epitaxial layer.

γ =n-jk is the complex refractive index of the material.

Z is the characteristic impedance of the layer given by: Z_{vac} / γ

ρ is the reflection coefficient

Using the following data

Si	n-jk = 3.79 – j 0.013	
W	n-jk = 3.76 – j 2.95	
SiO_2	n-jk = 1.48	
Z_{vac}	=	377 Ω

The modelled reflection coefficient as a function of depth into a sample is shown in figure 5.6. The sample layer structure consisted of 100 nm of Tungsten on 6 nm of oxide on a silicon substrate. The model used to simulate the reflection coefficient is the same model used in [5.9].

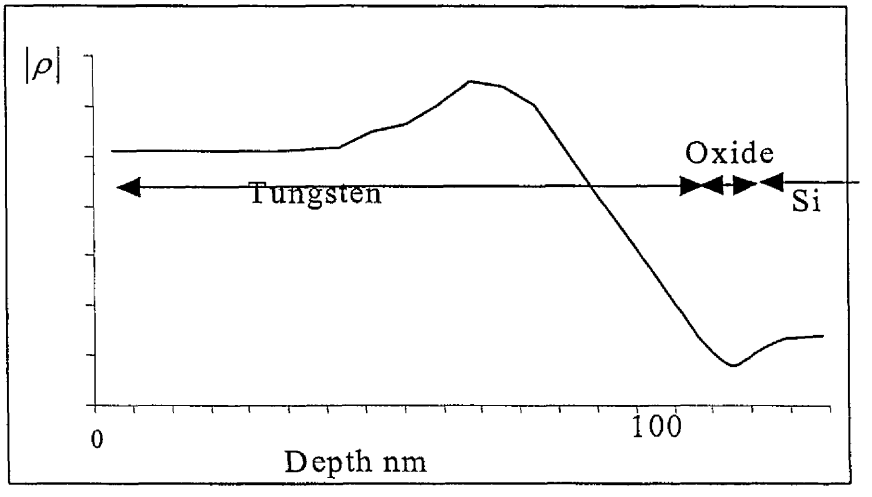

Figure 5.6 Modelled reflection Coefficient of 100 nm W / 6 nm SiO_2 / 500 μm Si as function of depth onto sample.

A BP80 reactive ion etch machine with applied power of 100 W and chamber pressure of 9 mtorr was used with in-situ reflectometry to etch the gates. The gas used was SF_6 at gas flow rate 15 sccm. The average etch time before the stop point was reached was approximately 60 s. The remaining resist was removed by immersing the sample in acetone for 5 mins. Figure 5.7 is an SEM of a 100 nm tungsten gate fabricated using this process. The wafer level uniformity is not very good, over a 300 mm diameter wafer the centre will be overetched by 10 s if at the edge exactly 100 nm of tungsten is etched. However only 20 mm^2 samples were used in this work so wafer variation is not a major concern.

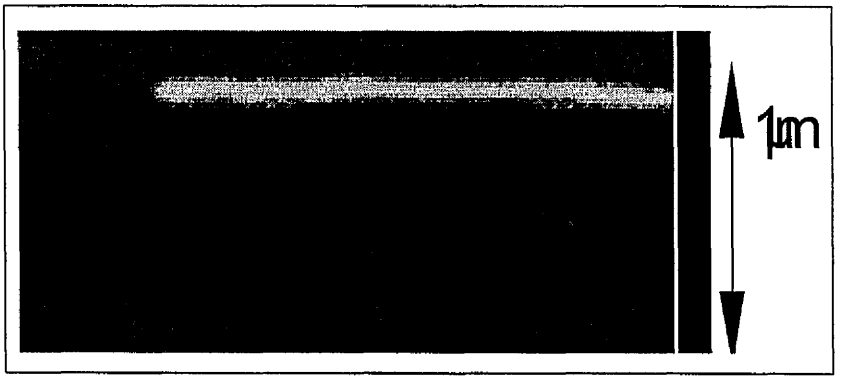

Figure 5.7 SEM of a 100 nm Tungsten Gate.

5.2 (b) (v) Source and Drain Formation

Ion implantation of the source and drain of the p-channel devices was carried out at the University of Edinburgh. A single implant was performed using the tungsten gate as a mask to obtain self aligned source and drain. The dose and energy used was 5 x 10^{15} BF_2 atoms cm^{-3} at 10 keV as designed in chapter 4. Following implantation the wafer was annealed at 900 °C for 20 s in a JIPELEC rapid thermal anneal (RTA) system to activate the implant.

5.2 (b) (vi) Ohmic Contacts

The source and drain patterns were defined using electron beam lithography with positive electron-beam resist. A bilayer of resist called poly(methyl methacrylate) (PMMA) was used. The first layer called ALD has lower molecular weight than the second layer called ELV. The difference in molecular weight enables the use of the two-layer process as shown in chapter 2. The resist was spin coated, exposed and developed as follows:

1. 8% ALD spin coated at 5000 rpm for 60 s then baked for 1 hour at 180 °C.
2. 4% ELV spin coated at 5000 rpm for 60 s then baked for 2 hours at 180 °C.
3. Expose pattern with a 50 keV energy electron beam with 160 nm spot size and dose 260 $\mu C/cm^2$.
4. Develop using 2:1 IPA: MIBK (isopropyl alcohol : methyl iso-butyl ketone) at 20 °C for 60 s then rinsed in IPA then blown dry with nitrogen.
5. The sample was then dipped in hydrophlouric acid (HF) for exactly 10 s to remove the gate oxide from the source and drain areas, then rinsed in reverse osmosis (RO) water. A 100 nm thick layer of aluminium / silicon was then thermally evaporated onto the sample. By immersing the sample in acetone for 1 hour the resist is removed, leaving only the aluminium / silicon in areas patterned by the electron beam. The sample is then rinsed in reverse osmosis RO water then annealed at 400 °C for 4 min to form the ohmic contacts.

In order to measure the contact resistance and resistance of the implant, TLM [5.10] (transmission line modeling) structures were patterned on the wafer. The sheet resistance of the implant was measured using the four-probe technique.

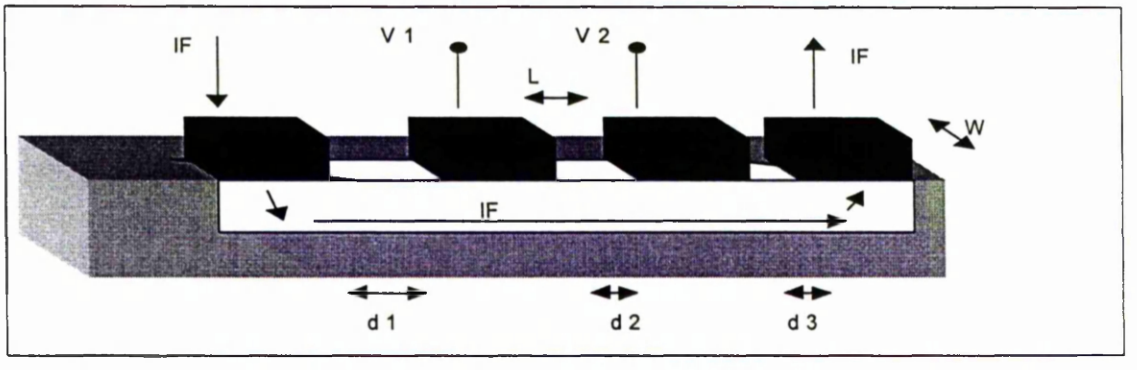

Figure 5.8 Transmission Line Modeling structure for measuring sheet and contact resistance.

From figure 5.8 the standard 4 probe measurement technique gives

$$R_{implant} = \frac{(V_2 - V_1)}{I_f} \tag{5.4}$$

R_c can be determined by measuring the resistance R of the same element using 4 probes on the two pads then

$$2R_c = R - R_{implant} \tag{5.5}$$

$2R_c = R - R_{implant}$

In addition by measuring and plotting the 4 probe resistances as a function of d and by plotting R versus d and using

$$R = \frac{\rho d}{A} + 2R_c \tag{5.6}$$

$2R_c$ is the intersection with the y-axis and R_{sh} / Z is the gradient.

Using the above methods, R_{sh} = 10000 Ω/sq and R_c = 0.3 Ω-mm.

So for a device of width 100 μm with source to gate spacing of 1 μm the total access resistance is estimated to be 103 Ω.

5.2 (b) (vii) Isolation etch

Photoresist was used as the mask for the isolation etch process because of its resistance to the dry etch process. The following process was used:

1. Spin coat the sample with S1818 positive photoresist at 4000 rpm for 30 s.
2. Bake at 90 °C for 15 mins.
3. Expose the sample to UV light through the mask on a manual mask aligner.
4. The isolation etch was performed in a BP80 reactive ion etch machine at 23 °C with 100 W of power using SF_6 gas for 5 mins.

The resulting etch depth as measured on a Dektak surface profiler was approx 1 μm. The remaining resist was removed by immersing in acetone and the sample was then rinsed in RO water.

5.2 (c) DC characterisation of p-channel tungsten gate SiGe MOSFETs

The devices were characterised using a HP4145 parametric analyser and cascade probing station. For the IV characteristics, the source contacts were held at zero volts and the drain voltage was ramped from 0 to –Vd for various fixed gate voltage. The measured IV characteristics, of 3, 1, 0.5 and 0.25 μm gate length devices are shown in figures 5.9 (a–d).

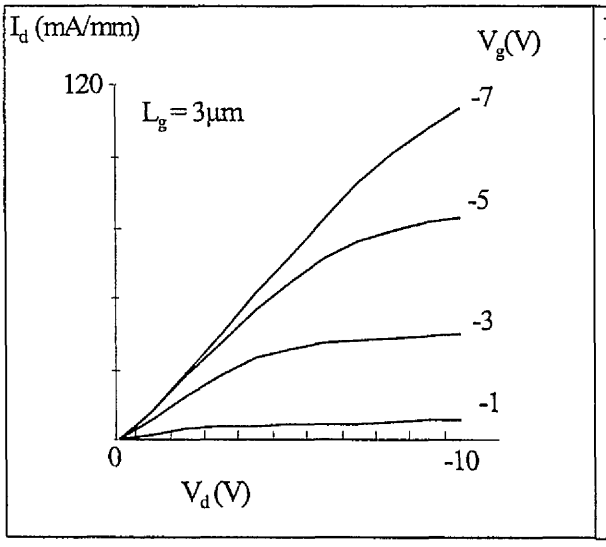

Figure 5.9 (a)

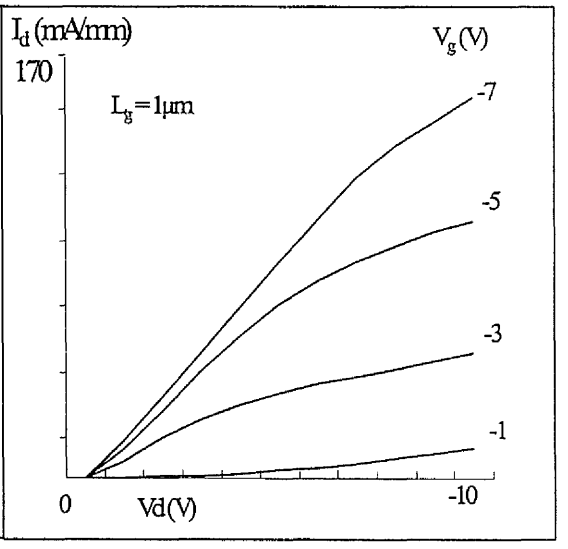

Figure 5.9 (b)

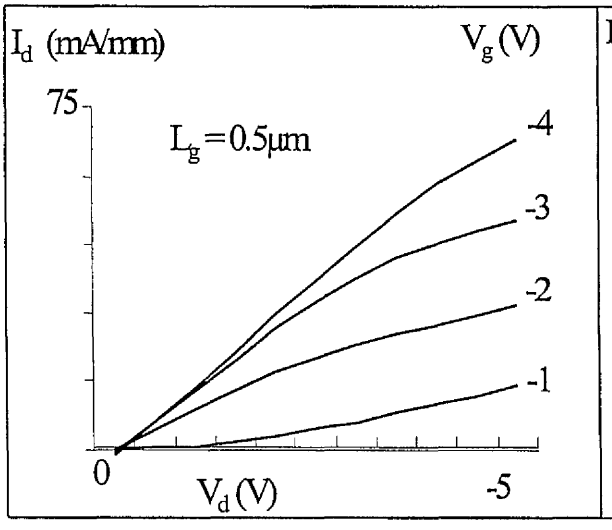

Figure 5.9 (c)

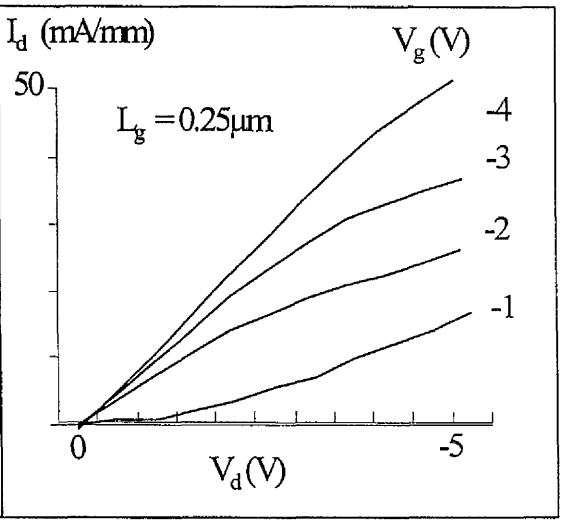

Figure 5.9 (d)

Figure 5.9 (a-d) IV characteristics of p channel tungsten gate MOSFETs.

The transfer characteristics of a 3 μm and a 1μm gate length MOSFET are shown in figure 5.10.

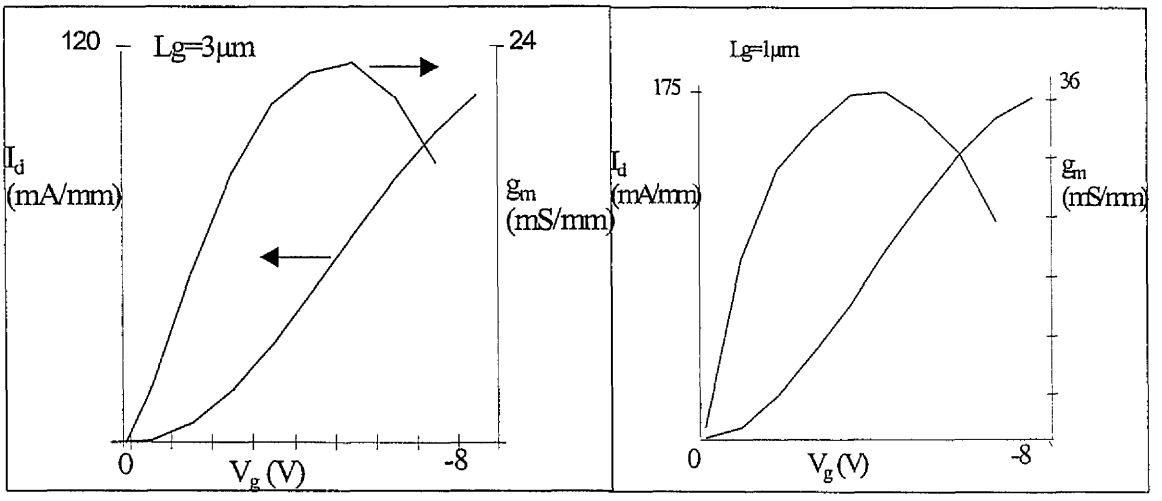

Figure 5.10 Measured transfer characteristics of p-channel SiGe tungsten gate MOSFETs.

The peak transconductance is 36 mS/mm for a 1μm x 200 μm transistor = 1.8 mS
The intrinsic transconductance is estimated using equation

$g_m' = 0.0018 / (1 - 206 \times 0.0018) = 2.9$ mS
Dividing the width gives $g_m' = 58$ mS/mm

The gate leakage is measured to be 150 μA/mm, this is very large and is attributed to

1. Home grown oxide quality.
2. Probing pads placed directly onto gate oxide with no other isolation or ILD.

5.3 Strained silicon n-channel gold gate MODFETs

5.3 (a) Fabrication process

The fabrication process developed for strained silicon gold gate MOSFETs is shown in figure 5.11. There were four major differences from the tungsten gate process.

1] An active area mesa is formed by dry etching the substrate. The sample is then planarised by lifting off sputtered SiO_2. This step has been introduced to reduce gate leakage and capacitance of the probing pads.

2] The thermally grown gate oxide was carried out at the University of Southampton using their 6 nm oxidation process.

3] Ti / Pd / Au gates were employed, a mature electron beam evaporated gold lift off process capable of sub 50 nm gate lithography was used.

4] Ti / Au ohmic contacts were used in preference to aluminium which is known to spike making contact to the substrate. Also as Au probing pads were to be used, Al-Au contact must be avoided.

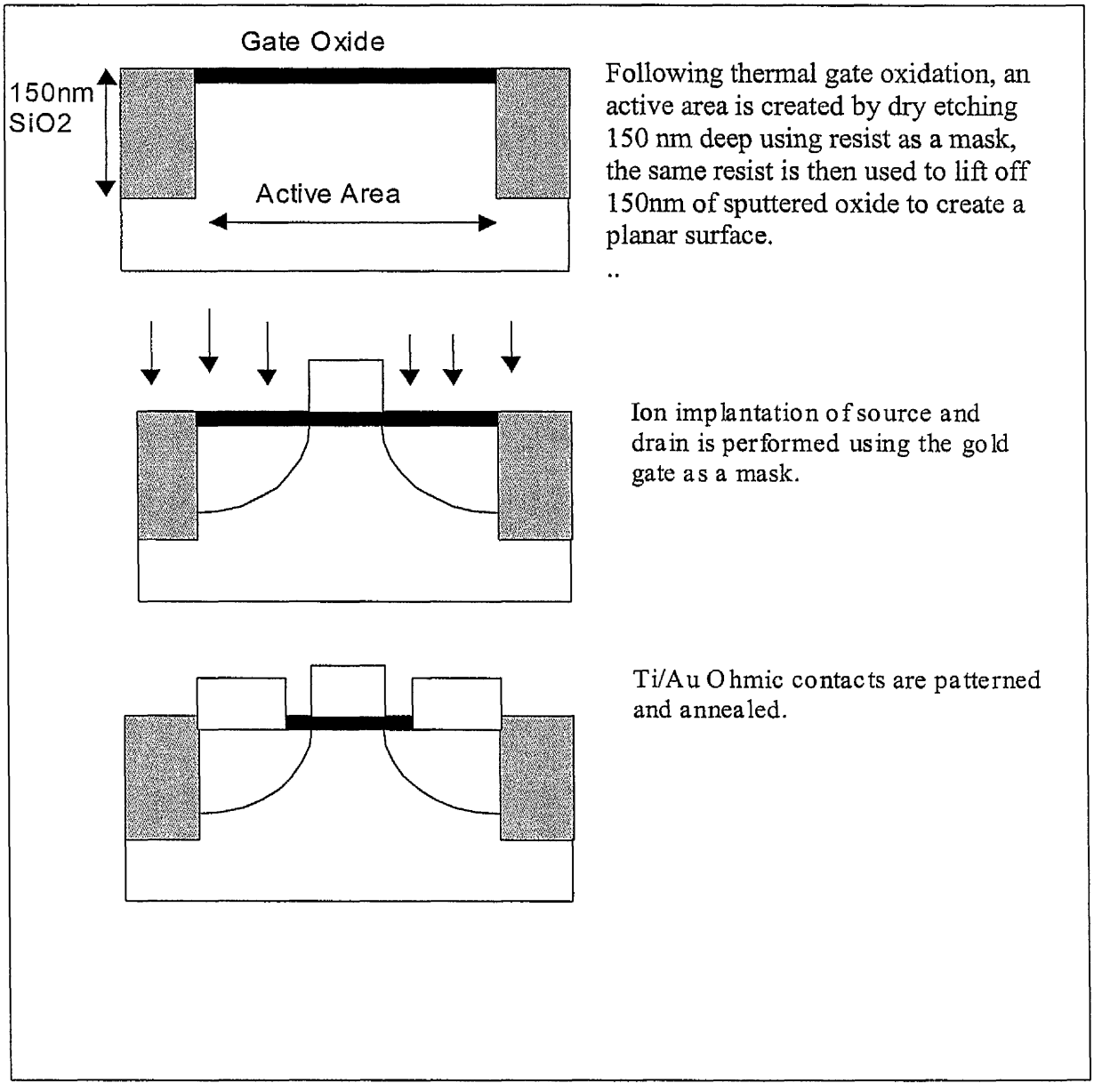

Figure 5.11 Fabrication process for Ti / Pd / Au gate n-channel MOSFETs.

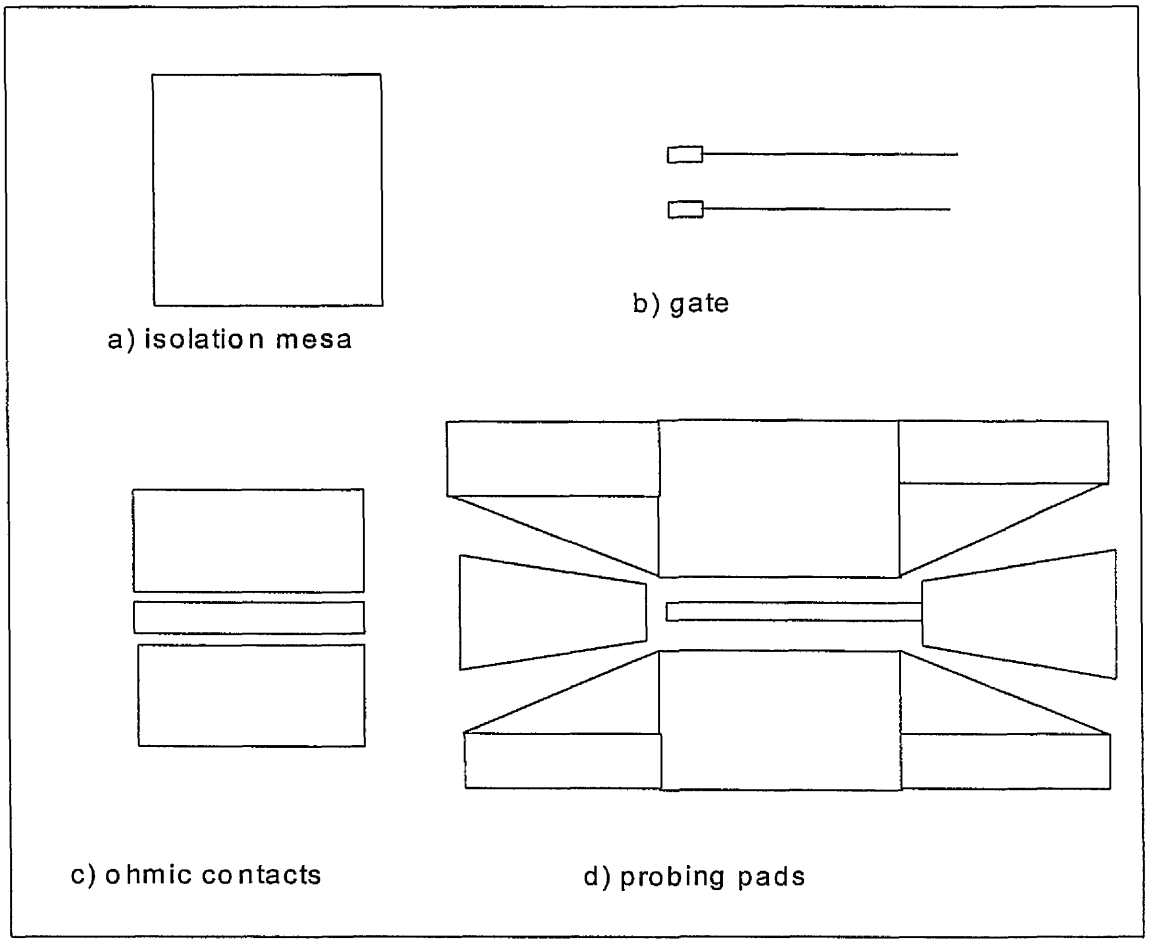

Figure 5.12 Mask layouts for n-channel MOSFETs.

5.3 (b) Process steps

5.3 (b) (i) Gate Oxidation

Gate oxidation of the complete 300 mm diameter wafer was carried out at the University of Southampton. Prior to oxidation, the wafer was subjected to an RCA clean [5.11]. The clean removes some 2-3 nm of the silicon cap layer. The oxide thickness is 6 nm. The sample was then returned to Glasgow and the wafer was scribed into 20 mm^2 bits for further processing.

5.3 (b) (ii) Mesa Pattern and Etch

The mesa was patterned using electron beam lithography and dry etched as follows

1. 15% ALD spin coated at 5000 rpm for 60 s then baked at 180 °C for 1 hour.
2. 4% ELV spin coated at 5000 rpm for 60 s the baked at 180 °C for 2 hours.
3. Electron beam exposure at energy 50 keV, spot size 400 nm, dose 300 $\mu C/cm^2$.
4. Develop in 1:1 MIBK:IPA at 23 °C for 30 s
5. Etched in a BP80 reactive ion etcher using a timed etch to a depth of approximately 150 nm. The etch parameters were, reflected power 100 W, pressure 9 mTorr for 2 mins. A test sample was etched at the same time and the etch depth was measured on a dektak surface profile system.

5.3 (b) (iii) Planarisation

Silicon dioxide was sputtered using the Nordico sputter system at an etch rate of 1.5 nm/min. Lift off was carried out with the sample immersed in acetone and agitated using an ultrasonic bath for 30 mins. The measured step height between the mesa edge and sputtered oxide was always within limits of system and swamped by the surface roughness already present in the SiGe.

5.3 (b) (iv) Gate stack

The gate stack was patterned, evaporated and lifted off as follows:

1. 8% ALD spin coated at 5000 rpm for 60 s then baked at 180 °C for 1 hour.
2. 4% ELV spin coated at 5000 rpm for 60 s the baked at 180 °C for 2 hours.
3. Electron beam exposure at energy 50 keV, spot size 40 nm, dose 600 $\mu C/cm^2$.

4. Develop in 2 : 1 MIBK : IPA for 30 s
5. Evaporation of Ti (15 nm) Pd (15 nm) Au (160 nm) in a plassys electron beam evaporator
6. Lift off in boiling acetone for 1 hour.

5.3 (b) (v) Source Drain Implant

Implantation was carried out at Imperial College London. Initial samples were implanted using Phosphorous at 20 keV with a dose of 5×10^{15} atoms cm^{-2} . The implants were annealed at Glasgow on a JIPELEC RTA at 650 °C for 20 s.

5.3 (b) (vi) Ohmic Contact Metalisation

The ohmic contacts were patterned, evaporated and lifted off as follows:

1. 12% ALD spin coated at 5000 rpm for 60 s then baked at 180 °C for 1 hour.
2. 4% ELV spin coated at 5000 rpm for 60 s the baked at 180 °C for 2 hours.
3. Electron beam exposure at energy 50 keV, spot size 160 nm, dose 260 $\mu C/cm^2$.
4. Develop in 1 : 1 MIBK : IPA for 30 s.
5. Dipped for 10 s in HF then rinsed in RO water.
6. Immediately placed in the evaporator 100 nm Ti 100 nm Au.
7. Annealed at 300 °C for 3 min.

5.3 (b) (vii) Probing Pads

Probing pads were patterned as follows.

1. 12% ALD spin coated at 5000 rpm for 60 s then baked at 180 °C for 1 hour.
2. 4% ELV spin coated at 5000 rpm for 60 s the baked at 180 °C for 2 hours.
3. Electron beam exposure at energy of 50 keV, spot size 160 nm, dose 300 $\mu C/cm^2$.
4. The sample was dry etched in an oxygen plasma for 1min.
5. Develop in 1 : 1 MIBK : IPA for 30 s.
6. Thermal evaporation of 200 nm Au.
7. Lift off in acteone 1 hour.

5.3 (c) n-channel device characteristics

The IV characteristics, of initial 3,1,0.5 and 0.25 μm gate length devices are shown in figure 5.13.

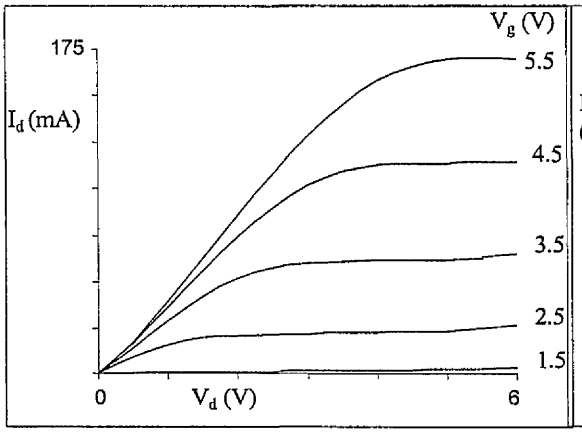

Figure 5.13 (a) L = 3 μm

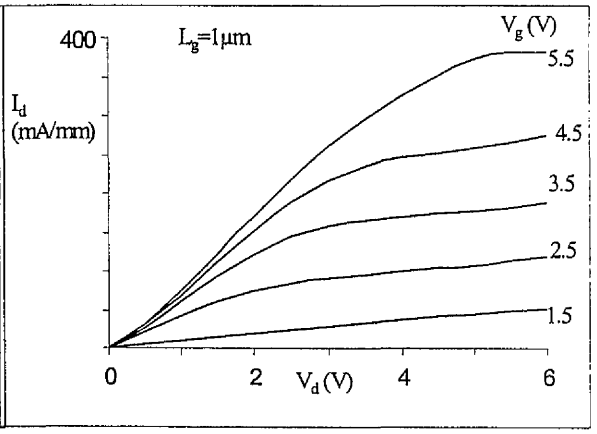

Figure 5.13 (b) L = 1 μm

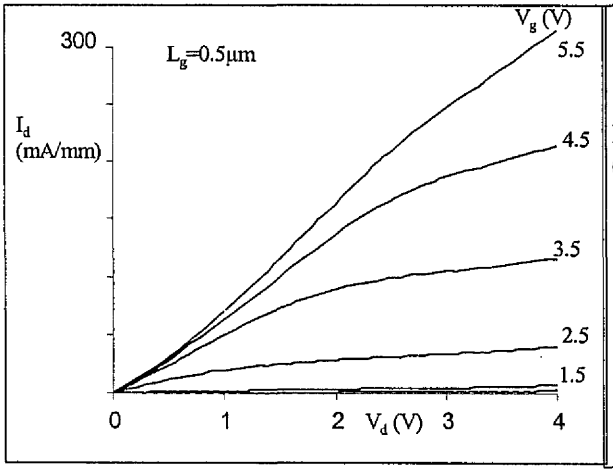

Figure 5.13 (c) L = 0.5 μm

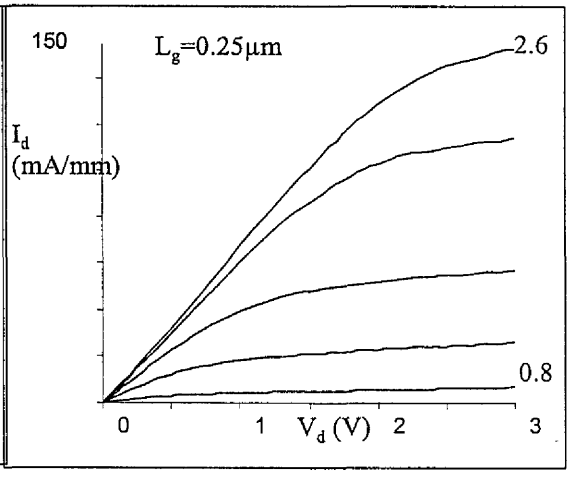

Figure 5.13 (d) L = 0.25 μm

Figure 5.13 IV Characteristics of Strained Si n-channel MOSFETs.

The source and drain contact resistance for the n-channel devices was measured to be 2.2 Ω-mm and the sheet resistance is 430 Ω/sq.

The device R_s is then approx 26.3 Ω (1 μm source-gate gap, 100 μm wide).

The gate leakage measured for the n-channel devices with oxidation carried out at the University of Southampton is always < 2 μA/mm.

Figure 5.14 show the transconductance of a 1 μm gate length MOSFET.

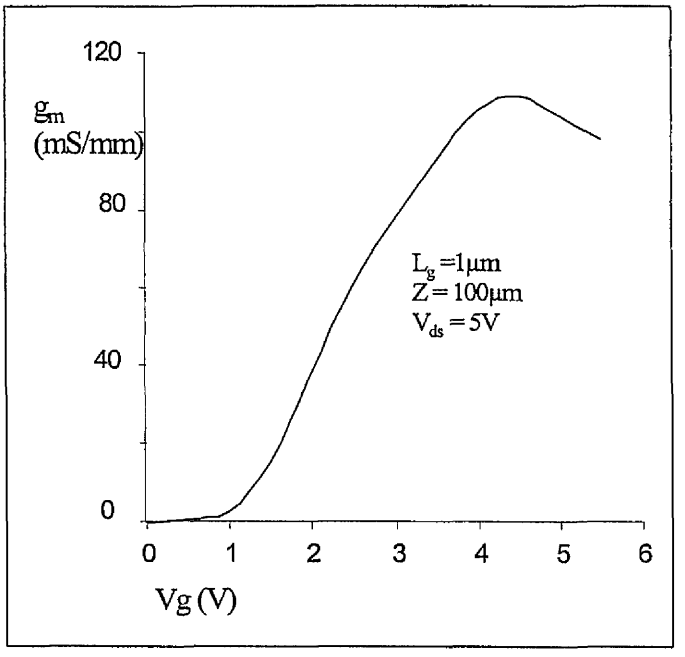

Figure 5.14 Transconductance of a 1 μm x 100 μm n-channel SiGe MOSFET.

An estimate of the intrinsic transconductance is obtained from

$g_m' = 0.0055 / (1-0.0055 \times 52) = 0.77$ mS

Dividing the width gives $g_m' = 154$ mS/mm

A Second Batch

Following the success of these devices and noting that the high source drain resistance limits the performance of sub 1 μm devices, another batch with a deeper source drain implant was fabricated. The dose and species was unchanged while the energy was increased to 40 keV. The resulting IV curve and transconductance of a 0.3 μm x 50 μm device are shown in figure 5.15.

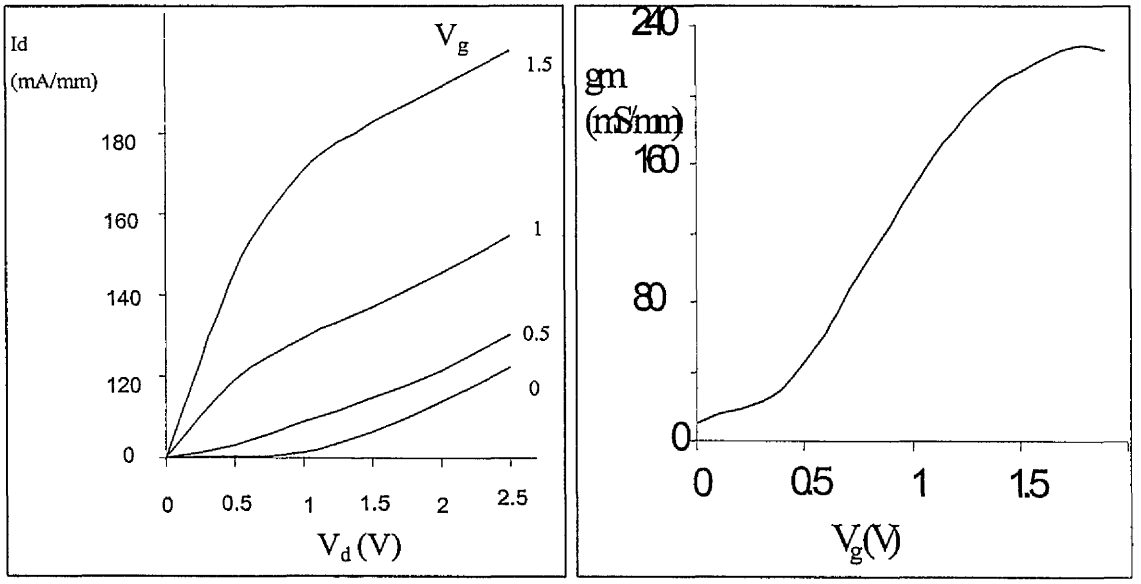

Figure 5.12 measured characteristics of a 0.3 μm x 50 μm device with 40 keV implant.

The increased junction depth lead to a measured R_{sh} and R_c of 200 Ω / square and 1 Ω mm respectively. The measured transconductance was 240 mS/mm. An estimate of the intrinsic transconductance is

$g_m' = 0.012 / (1 - 0.012 * 12) = 0.014$ S

Dividing the width gives $g_m' = 280$ mS/mm.

The extrinsic g_m also scales properly with gate length. Table 5.2 lists measured g_m versus gate length for these devices.

L (μm)	1	0.75	0.5	0.3
g_m' (mS/mm)	110	150	180	240

Table 5.2 Transconductance versus gate length.

5.4 Summary and Conclusion

Two independent metal gate fabrication processes have been developed for Si / SiGe MOSFETs. A tungsten gate deposition and dry etch process was developed capable of producing 100 nm lines. Using this process, p-channel SiGe MOSFETs were fabricated. 1 μm gate length devices had extrinsic and intrinsic g_m of 36 ms/mm and 55 mS/mm respectively.

A Ti / Pd / Au gate process was developed and employed in the fabrication of strained silicon n-channel MOSFETs. The performance of initial devices fabricated with a 20 keV source drain implant was limited by the source resistance. A second set of devices fabricated with a 40 keV implant produced improved results. Transconductance scaled properly with gate length. A 0.3 μm x 50 μm 2 finger MOSFET had extrinsic and intrinsic g_m of 230 mS/mm and 280 mS/mm respectively. The results obtained to date in this work demonstrate that both the metal gate processes can be used to successfully fabricate MOSFETs. Taking into account the demonstrative nature of the process, the DC results are very impressive. In particular the 0.3 μm gate length strained silicon n-MOSFET has good DC properties. The use of a metal gate means that the RF properties of these devices will be of interest.

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Chapter 6

High Frequency Measurement and Analysis of Metal Gate Si/SiGe MOSFETs

6.1 Introduction

In this chapter the measurement system and techniques used to measure the Si/SiGe MOSFETs in the frequency range 0 – 60 GHz are described. A strained silicon MOSFET of 1 μm gate length with probe pads close to the silicon substrate has been characterised. A method of lowering parasitic capacitance using a single layer of polymer to separate the pads from the substrate is described. A 0.3 μm gate length device has been measured. Using the active and passive element library developed in this work, a single stage amplifier is designed.

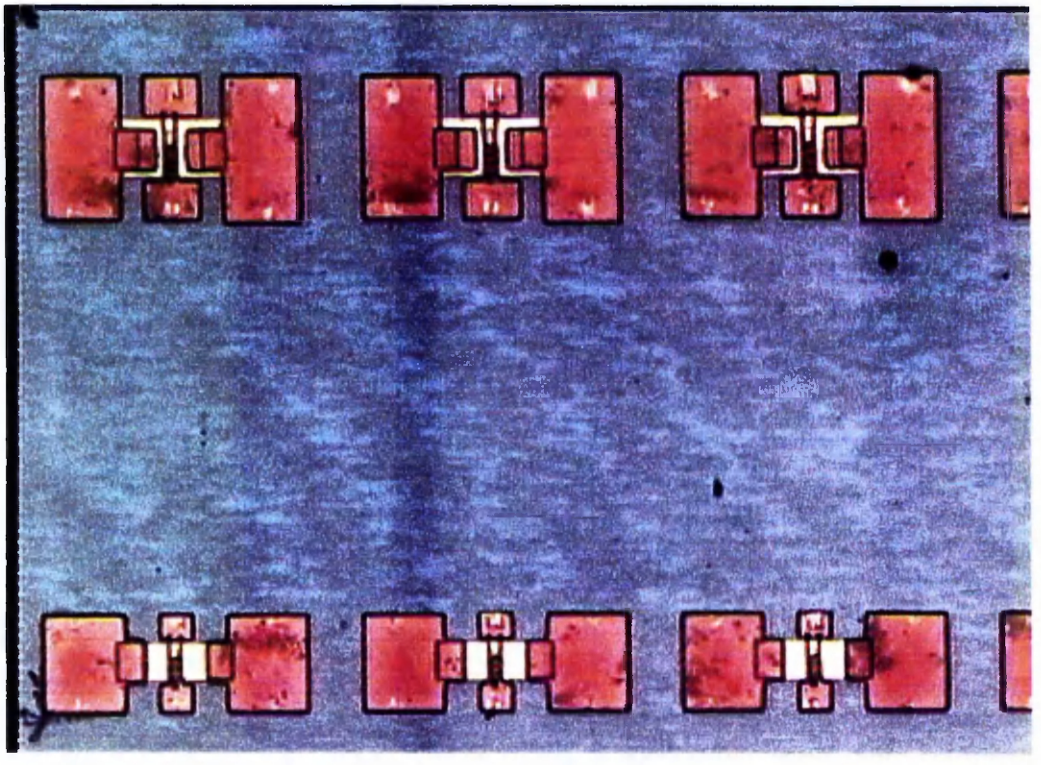

Image of MOSFETs with RF probe pads.

6.2 Measurement Set up and Techniques

The measurement set up is shown in figure 6.1. The HP4145 parametric analyser is used to supply the DC bias voltages while simultaneously monitoring the gate leakage current and the drain current. The frequency generator source provides the RF signal. The test set directs the flow of the RF signal to the test ports and imposes the DC bias from the HP4145 on the RF signal. The system is calibrated to the probe tips using the SOLT (Short Open Load Thru) technique on an ISS (Impedance Standard Substrate) [6.1]. The system described is only capable of RF measurements at a single DC bias point.

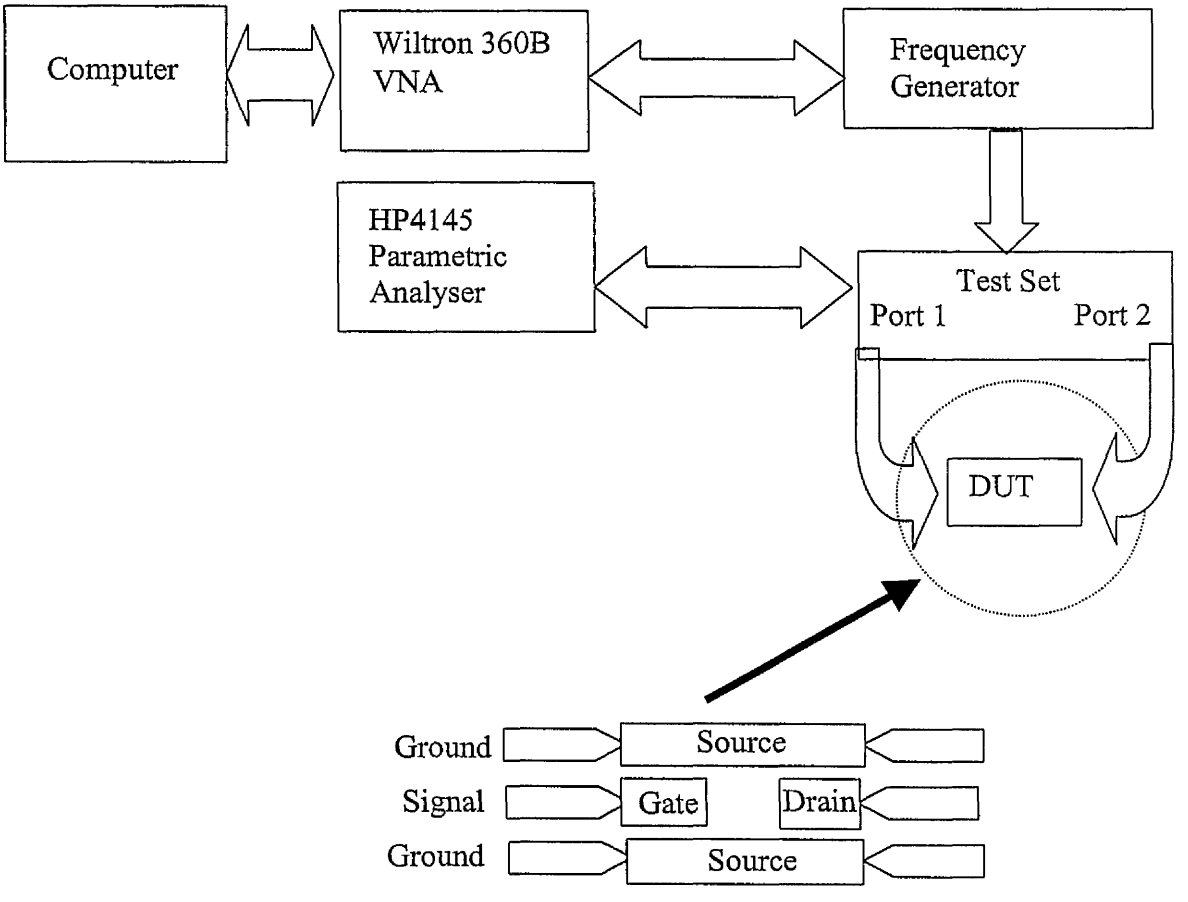

Figure 6.1 Measurement Set-up.

6.3 Initial Device Measurements and Modelling

The device bias point was chosen from the DC measurements for maximum transconductance. The first device tested was a 1 μm x 200 μm n-SiGe MOSFET with a g_m of 110 mS/mm at $V_g = 2$ V and $V_d = 2$ V. Figure 6.1 shows the measured S-parameters in a Smith chart representation [6.2]. Figure 6.1 shows the measured f_T and f_{max} of the device.

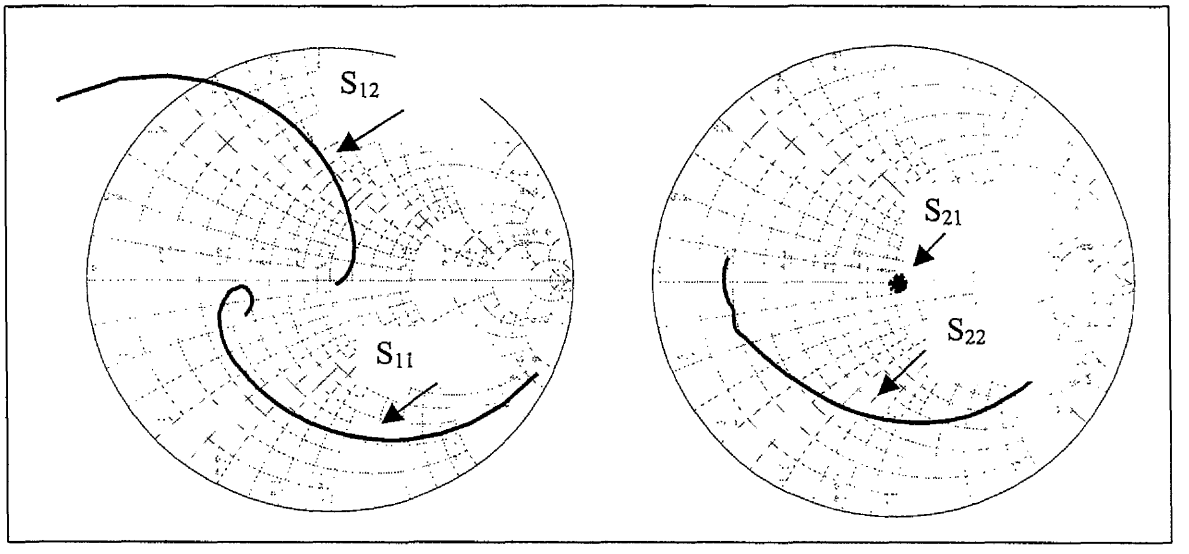

Figure 6.2 S parameters of Ti / Pd / Au gate strained Si MOSFET with 1 μm gate length.

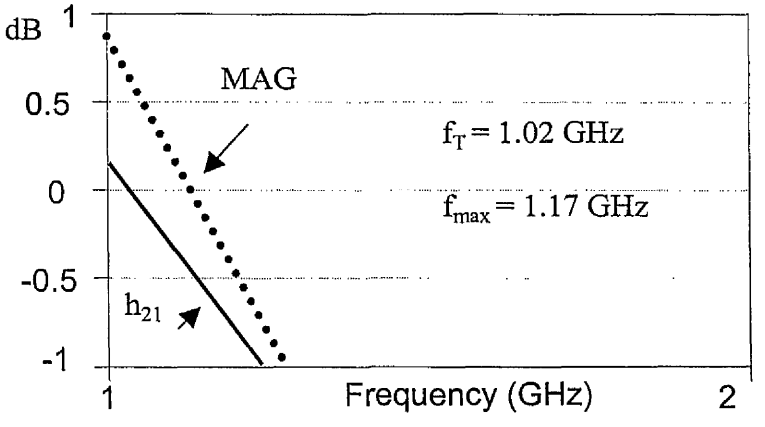

Figure 6.3 $|h_{21}|$ and MAG for a strained Si n-type 1 μm x 100 μm MOSFET.

Device Model

A simplified equivalent circuit from figure 2.12 was used to model the devices and is shown in figure 6.4 [6.3].

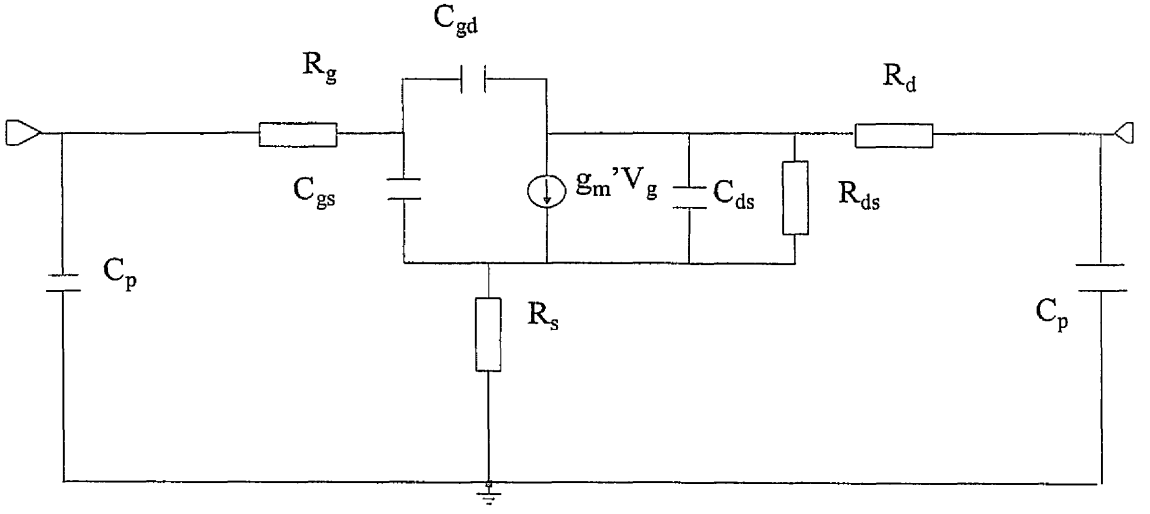

Figure 6.4 The equivalent circuit as used to model the measured results.

The equivalent circuit elements were chosen such that the measured S-parameters matched that of the equivalent circuit. The circuit elements are shown in figure 6.4 and are listed in the table below.

R_g (Ω)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	g_m' (S)	R_s (Ω)	R_{sd} (Ω)	$C_{dp,gp}$ (fF)	C_{ds} (fF)
20	1	90	100	0.019	1	250	4000	1

Table 6.1 Equivalent circuit elements for strained Si n-channel MOSFET with probing pads directly on 150 nm of oxide on silicon.

These devices suffered from large gate and drain pad capacitance because the 100 μm^2 probing pads were placed directly on 150 nm of sputtered oxide on the silicon substrate. The pad capacitance is given by

$$C_{gs}= \frac{\mathcal{E}_r \mathcal{E}_o A}{d} \qquad (6.1)$$

Where

ε_r is the dielectric constant of SiO_2 taken to be 4

A is the area of the pad (μm^2)

d is the thickness of the oxide in this case 150 nm.

The table below compares the capacitance expected of a probing pad of various area fabricated on 150 nm of oxide on a low resistance silicon substrate.

A (μm^2)	C (fF)
100	4000
50	1000
10	200

Table 6.2 Probing pad capacitance for different pad area with d = 150 nm of oxide.

This table illustrates the enormous effect that probing pads have on the parasitic capacitance of a device grown on a low resistance substrate.

De-Embedding by Modeling

It is common practice to extract the intrinsic device performance by de-embedding the probing pad capacitance [6.4]. The intrinsic performance of the device can be estimated by simply changing C_{gs} in the model. This effect on f_T and f_{max} by reducing just C_{gs} is shown in table 6.3.

C_{gs} (fF)	f_T (GHz)	f_{max} (GHz)
4000 (As Measured)	1.02	1.17
1000	3.2	4.8
500	5.1	8.7
100 (Intrinsic)	16	19

Table 6.3 The modelled effect on f_T and f_{max} on reducing C_{gs}.

6.4 Optimisation of the Probe Pad Capacitance

It has been shown above that by reducing the probing pad capacitance, the measured RF figures of merit will be improved. In addition, to implement the MOSFETs in an integrated circuit, contact pads will be required to connect to the rest of the circuit and should also be of low capacitance. A spin on dielectric was chosen as the quickest and best way to get results. A 1 μm thick layer of PMMA was chosen as the dielectric. This meant that alignment could be made automatically with the electron beam-writer straight onto the existing 10 μm^2 gate pad. Figure 6.4 shows the fabrication steps proposed.

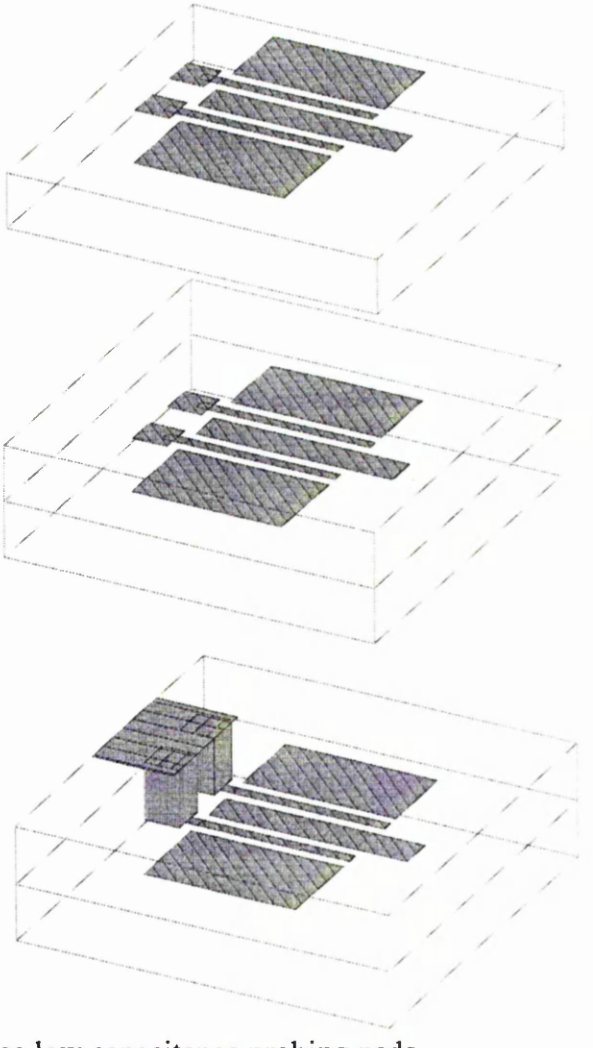

Figure 6.5 Fabrication process to produce low capacitance probing pads.

6.5 Measurement of 0.3 μm gate length MOSFET

Using the method described above to reduce the parasitic pad capacitance, a 2 finger 0.3 μm x 50 μm MOSFET with g_m of 230 mS/mm was measured from 0 – 60 GHz. Figure 6.5 shows the measured and modelled S-parameters. Figure 6.6 shows f_T and f_{max}.

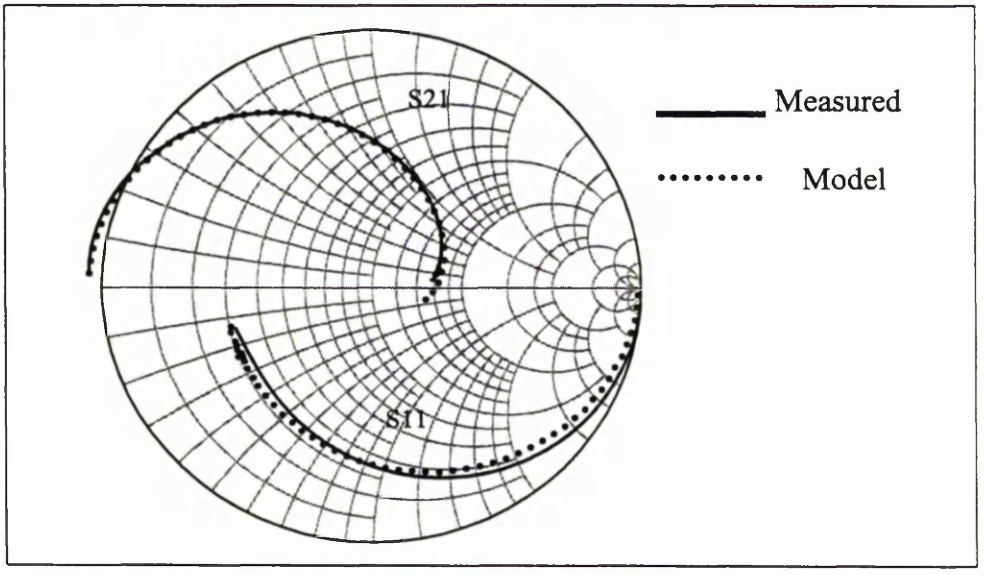

Figure 6.6 Measured and modeled S parameters for a 0.3 μm x 100 μm MOSFET.

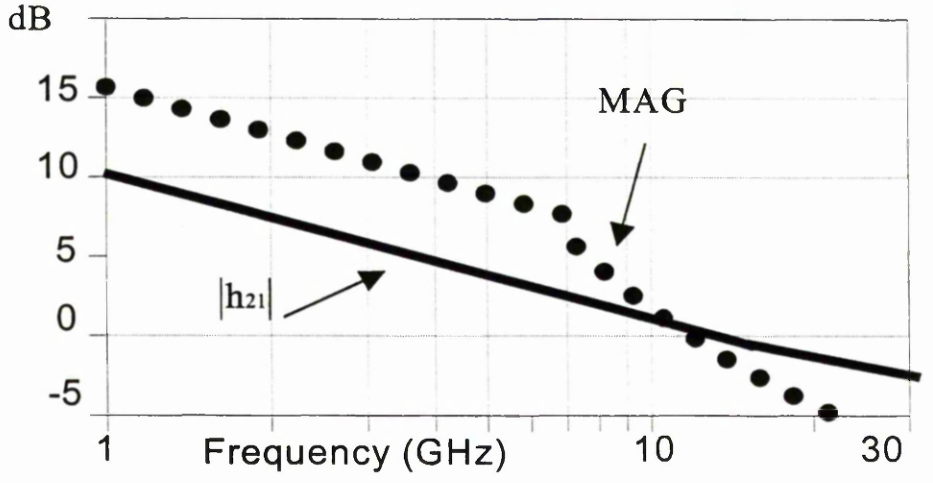

Figure 6.7 f_T and f_{max} of a 0.3 μm gate length strained silicon MOSFET.

The resulting f_T = 12.4 GHz and f_{max} = 11.8 GHz

The equivalent circuit parameters extracted from the model of the 0.3 μm x 50 μm device with probing pads on a 1 μm thick layer of polymer are shown below.

R_g (Ω)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	g_m' (S)	R_s (Ω)	R_{sd} (Ω)	$C_{gp,dp}$ (fF)	C_{ds} (fF)
15	1	50	70	0.013	1	200	100	54

Table 6.4 Equivalent circuit elements for strained Si n-channel 0.3 μm gate length MOSFET with probing pads on polymer.

De-embedding to obtain the intrinsic performance

Despite the new method there is still a 100 pF parasitic gate capacitance, that arises from the 10 μm^2 extension of the gate on 150 nm of sputtered oxide. A more sophisticated method of de-embedding the probe pad capacitance was carried out this time. The pad parasitic removal program available with Wincal software [6.5], will automatically de-embed the effect of the probing pads. To do this, an open-circuited probing pad is measured and the software calculates and returns the de-embedded device S-parameters. The results for the de-embedded device are shown below.

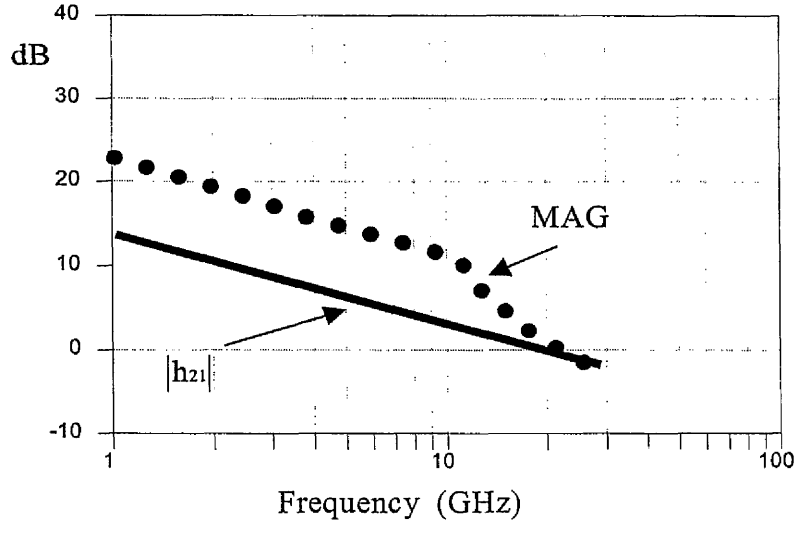

Figure 6.8 De-embedded f_T and f_{max} of a 0.3 μm x 50 μm MOSFET.

f_T = 19.9 GHz f_{max} =21.1 GHz

The above results are very good for a 0.3 um gate length MOSFET. It is one of the very few results in the literature (see Chapter 2) with $f_{max} > f_T$. Despite the developmental nature of the process and the lack of a self-aligned silicide to reduce the source and drain resistance, the results compare well with current state of the art MOSFETs. The extracted equivalent circuit parameters are shown below.

R_g (Ω)	R_d (Ω)	C_{gd} (fF)	C_{gs} (fF)	g_m (S)	R_s (Ω)	R_{sd} (Ω)	C_{ds} (fF)
15	1	50	70	0.013	1	200	20

Table 6.5 Equivalent circuit elements for de-embedded strained Si n-channel MOSFET with 0.3 μm gate length.

6.7 Conclusions

Strained silicon n-channel Ti / Pd / Au gate MOSFETs fabricated on a standard silicon substrate have been characterised at microwave frequencies. The performance of devices with probing pads on a 150 nm oxide layer on the silicon substrate was poor. The poor results are attributed to the probing pad capacitance. A process for fabricating the device with probing pads on a 1 μm thick dielectric layer was developed. Devices characterised with the new probing pad arrangement showed excellent performance at microwave frequencies. For a 0.3 μm gate length device a directly measured f_T 12.4 GHz and f_{max} of 11.8 GHz was measured. By de-embedding the pad parasitics this is increased to an f_T of 19.9 GHz and f_{max} 21.1 GHz. Despite the developmental nature of the device process which has high access resistance these are state of the art microwave characteristics for MOSFETs.

The devices are modelled and equivalent circuit values are extracted. From these it is clear that there is still some improvement possible in reducing the limiting pad capacitance.

Despite the developmental nature of the process, MOSFETs have been fabricated with the capability of operating in the frequency range up to 10 GHz. This frequency range is the focus of much attention at present because of mobile communications applications around 2 GHz.

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Chapter 7

Coplanar Waveguide Transmission Lines and Spiral Inductors on CMOS Grade Silicon.

7.1 Introduction and list of symbols

This chapter is concerned with the problem of producing high frequency transmission lines on a low resistivity silicon substrate. The first section considers the background of transmission lines on semiconductor substrates such as GaAs and silicon. Then transmission line theory on semiconducting substrates is reviewed. The fabrication of a CPW on silicon substrates using spin on glass as an interlayer dielectric is described. CPW transmission lines fabricated using spin on dielectrics are characterised from 0 - 60 GHz. Spiral inductors are also fabricated and characterised using the same technology.

List of symbols

α attenuation coefficient

α_c attenuation coefficient for a conductor

α_d attenuation coefficient of a dielectric

β phase change coefficient

δ skin depth

ε_r relative dielectric constant

ε_o permittivity of free space

ε effective permittivity

f frequency

f_e relaxation frequency

h dielectric thickness

λ_g guide wavelength

λ wavelength

ρ resistivity

σ conductivity

S signal conductor width of CPW

t thickness of conductor metal

μ permeability

v_p phase velocity

ω angular frequency

W signal ground spacing of CPW

γ propagation constant

Z_o characteristic impedance

7.2 Background

The difficulty of combining low loss transmission lines and inductors operating at microwave frequencies made using the same process on silicon substrates is a major roadblock to Si RF circuits [7.1]. Monolithic microwave integrated circuits (MMICs), require low loss transmission lines to interconnect between elements in the circuit. At microwave frequencies, the signal on a standard wire would radiate and cause cross-talk. High Q factor spiral inductors and capacitors are required for matching the input and output impedance of transistors for maximum power transfer [7.2]. Coplanar waveguides (CPW) [7.3] are often used as transmission lines in MMICs. This chapter very briefly reviews the coplanar waveguide and its characterisation. Typical transmission losses for a gold coplanar waveguide on a semi-insulating gallium arsenide (GaAs) substrate is 0.3 dB/mm at 60 GHz [7.4]. Recent attempts to produce low loss transmission lines on a standard silicon process using SiO_2 as a dielectric have been encouraging [7.5][7.6][7.7]. Low loss transmission lines have been produced on standard silicon with thick dielectric layers such as polyimide on top [7.8]. High Q multi level inductors have been produced on standard silicon with multilevel interlayer oxides [7.9][7.10]. However most silicon based RF circuit demonstrators to date have been produced on high resistivity silicon [7.11][7.12]. One major advantage expected of MMICs on silicon could be as a result of using as much as possible of standard CMOS devices and processes. CMOS is not compatible with high resistivity silicon substrates. A complete process on a CMOS grade silicon substrate is required which provides

a) low loss waveguides.
b) spiral inductors.
c) simple interconnect to device contacts.

A spin on dielectric process developed for silicon substrates using photoresist and polyimide is presented. Coplanar waveguide transmission lines were designed and characterised on CMOS grade silicon using this process. A method for interconnecting through the 15 μm thick dielectric layer has been developed. The resulting spiral inductors on the dielectric had a high Q factor.

7.3 Coplanar Waveguides

A coplanar waveguide has a central signal conductor and outside ground conductors as shown in figure 7.1. S is the width of the signal line, W the signal to ground spacing and t the conductor thickness.

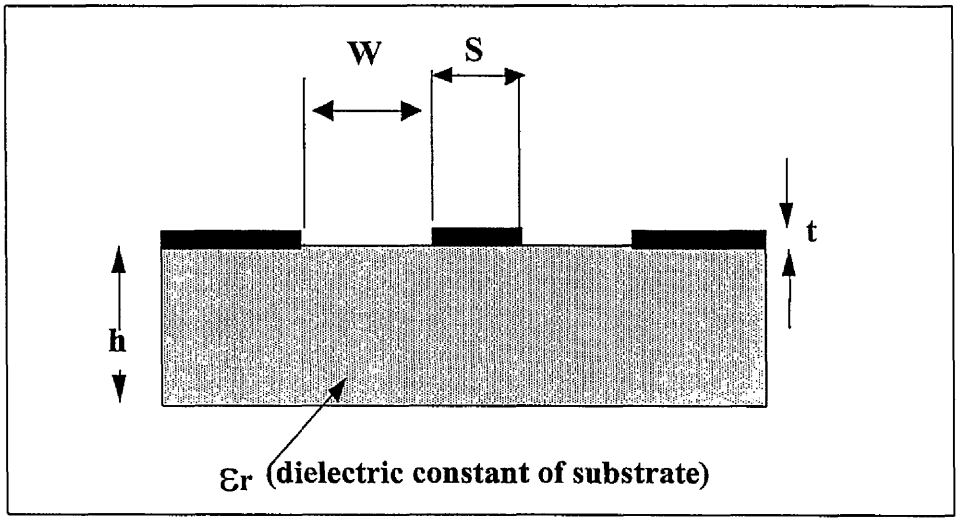

Figure 7.1 Coplanar waveguide.

Important things for a designer to know are the guide wavelength, characteristic impedance and attenuation.

Guide Wavelength (λ_g)

The wave is slowed down by the dielectric medium such that

$$v_p = f\ \lambda_g \tag{7.1}$$

and

$$\lambda_g = \frac{\lambda}{\sqrt{\varepsilon}} \tag{7.2}$$

where ε is the effective permittivity including the effect of the air surrounding and multiple dielectric layers if present.

Characteristic Impedance Z_0

The characteristic impedance of a CPW on an insulating substrate is given by [7.3]

$$Z_o = \frac{3\pi}{\sqrt{\varepsilon}} \frac{K(k')}{K(k)} \tag{7.3}$$

Where

$$k = \frac{S}{S+2W} \tag{7.4}$$

$$k' = \sqrt{(1-k)} \tag{7.5}$$

K is the complete elliptic integral of the first kind and its complement. It has been verified that K(k')/K(k) can be estimated from [7. 13]

$$\frac{K(k')}{K(k)} = \frac{1}{\pi} \log\left(\frac{2\left(1+\sqrt{k'}\right)}{\left(1-\sqrt{k'}\right)} \right) \tag{7.6}$$

Propagation Losses

The propagation of a wave along a transmission line is characterised by the complex propagation coefficient

$$\gamma = \alpha + j\,\beta \tag{7.7}$$

Where α is the attenuation coefficient and β is the phase change coefficient. Attenuation in a waveguide is due to (1) loss in the metal and (2) loss in the dielectric [7.14]. In general the losses in the metal can be evaluated as

$$\alpha_c = \sqrt{\pi f \sigma \mu} \tag{7.8}$$

The depth of penetration of the field into a conductor is called the skin depth given by

$$\delta = \frac{1}{\alpha_c} \tag{7.9}$$

In General Loss in the dielectric is proportional to f

$$\alpha_d = \frac{\omega\varepsilon''}{2}\sqrt{\frac{\mu}{\varepsilon}} \tag{7.10}$$

where ε'' is the imaginary part of the complex effective permittivity.

Transmission lines on a semiconducting substrate

Low resistivity silicon substrates are used in many silicon applications. A dielectric layer has to be put between the silicon substrate and the transmission line. The existence of a low resistivity substrate a finite distance below the transmission line will effect the mode of propagation, phase velocity and losses on the line. There are three distinct propagation modes possible on a semiconducting substrate [7.15].

1) Skin Effect Mode

At very high frequency and substrate conductivity, the skin depth of the conducting substrate is small and it acts as an imperfect ground plane. The skin effect mode requires a very high frequency and low resistivity substrate. The high frequency and high substrate conductivity required for this mode means that it is not normally the case.

2) Slow Wave Mode

The slow wave mode propagates at low frequency and moderate resistivity. The electric field propagates in the dielectric and the magnetic field propagates in the substrate and in the dielectric which could provide a slow wave mode. The

phase velocity is low and the effective relative permitivity is high. The losses are high and are dominated by the substrate resistivity.

3) Quasi-TEM dielectric mode

At high operating frequency when $f > f_e$ silicon is effectively a dielectric and a low loss quasi-TEM mode propagates. The phase velocity reaches theoretical maximum for CPW on a dielectric. The silicon relaxation frequency is given by

$$f_e = \frac{\sigma}{2\pi\varepsilon} \qquad (7.11)$$

The mode of propagation depends on frequency, line dimensions and substrate conductivity. The equivalent circuit for a transmission line on a semiconducting substrate is shown in figure 7.2 [7.16].

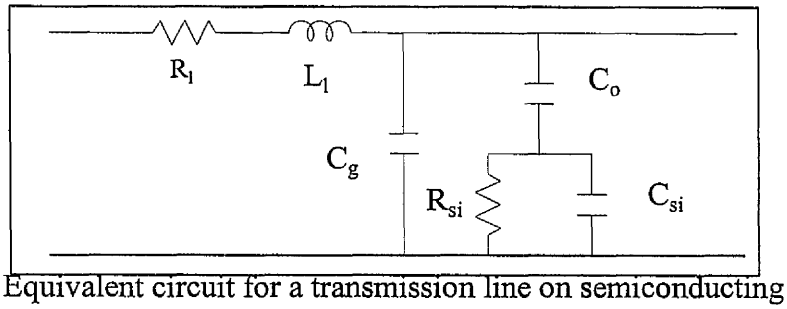

Figure 7. 2 Equivalent circuit for a transmission line on semiconducting substrate.

$\mathbf{R_1}$ is the resistance per unit length of the metal.

$\mathbf{L_1}$ is the inductance per unit length of the metal.

$\mathbf{C_g}$ is the capacitance per unit length between the signal and ground plane when the field is confined to the air and dielectric.

$\mathbf{C_o}$ is the capacitance per unit length of the dielectric.

$\mathbf{R_{si}}$ is the resistance of the substrate caused by induced currents in the substrate by the electric field and depends strongly on signal line width and dielectric thickness. An approximation for R_{si} is $R_{si} = \rho S / t$ where t is the thickness of the dielectric.

$\mathbf{C_{si}}$ is the capacitance of the silicon substrate that accounts for the transition from the lossy slow wave mode to the quasi TEM dielectric mode above f_e.

7.4 Fabrication of Low Loss Transmission Lines on High Resistivity Silicon

CPW transmission lines were fabricated using a spin-on glassy dielectric in order to separate the transmission line from the lossy silicon substrate. The transmission lines themselves are made of electroplated gold 2.2 μm thick. Figure 7.3 shows the fabrication steps involved that use photolithography and electroplating techniques to create a contact from the surface of the dielectric to the silicon surface.

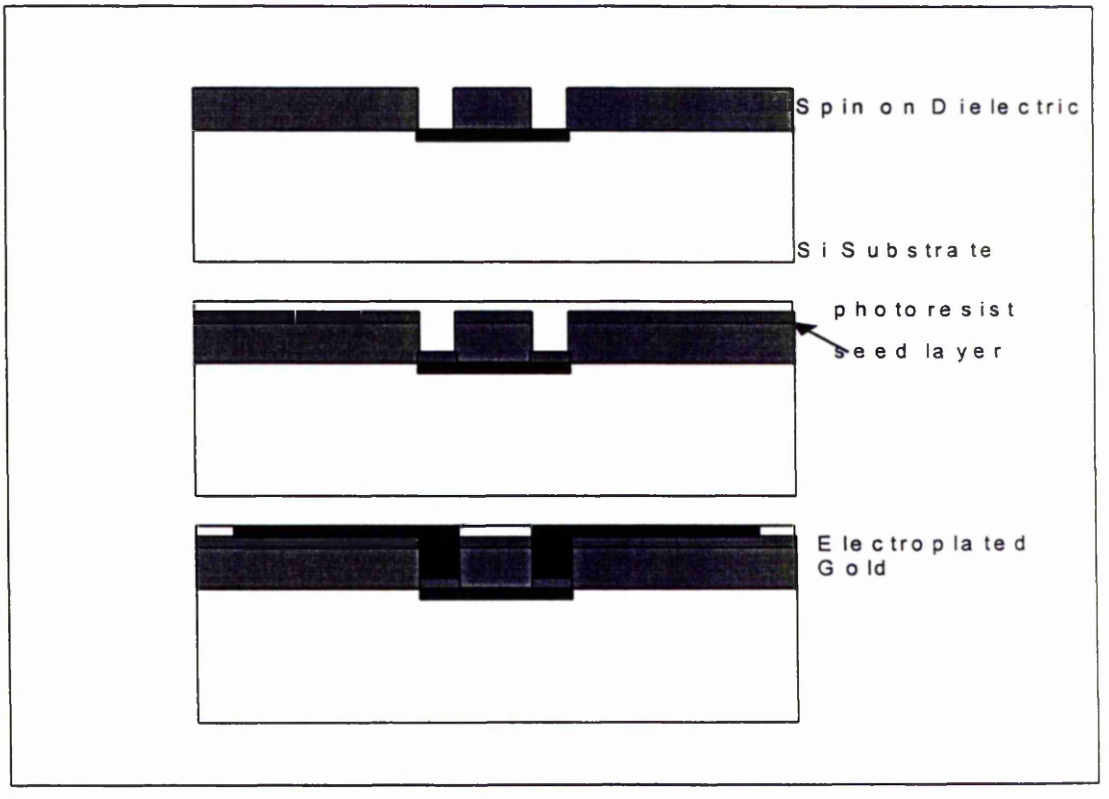

Figure 7.3 Fabrication steps for spin on dielectric process on silicon.

First the polyimide or photoresist to be used as the low loss dielectric is spun onto the silicon substrate. Table 7.1 details the spinning speeds, post baking and the resulting dielectric thickness for the dielectrics used in this work.

Dielectric	Spin Speed (rpm)	Spin Time (s)	PostBakeTemp (°C)	Post Bake Time (mins)	Thickness (μm)
S1818	4000	30	90	20	1.8
S1828	4000	30	90	20	2.8
AZ4562	4000	30	90	20	7
P7020	2000	15	90	10	30

Table 7.1 Spinning details for photoresist and polyimide.

The photoresist and photosensitive polyimide used in this work are all positive. The contact windows down to the device can simply be patterned using photolithography. Following pattern transfer, the dielectric is then heated beyond its glass transition temperature. This renders the resist / polyimide solid and is no longer soluble in hydrofluoric acid or acetone. Table 7.2 shows the exposure, development and anneal conditions.

Dielectric	Exposure Time (s)	Developer/Time (s)	Anneal Temp/Time (°C) / (min)	Thickness (μm)
S1818	12	/ 75	180 / 120	1.8
S1828	12	/ 75	180 / 120	2.8
AZ4562	15	/120	180 / 120	7
P7020	10	/240	300 / 30	15

Table 7.2 Developing and baking details for photoresist and polyimide.

The sample is then blanket coated with the seed layer, which is 20 nm of evaporated Ti, 5 nm of evaporated Au, 40 nm of Sputtered Au. A layer of S1818 photoresist is then spun on and the contact windows are redefined, the resist is exposed for 40 s to clear out the deep contact window of photoresist. On the same resist, the transmission line is then defined, the resist is exposed for 12 s. Gold is then electroplated onto the exposed areas, the top layer of S1818 is removed in acetone and the seed layer is etched with gold etch (1:1 Blah B;ld) for 6 s and HF for 4 s leaving only the electroplated transmission lines on the dielectric connected down to the device.

7.5 S-Parameters and Measurement Techniques

At high frequencies it is difficult to measure voltage and current at device ports. In addition an active device may be damaged with the connection of short or open circuits. So S-parameters were developed for the measurement of devices at high frequencies. Figure 7.4 represents a two port network

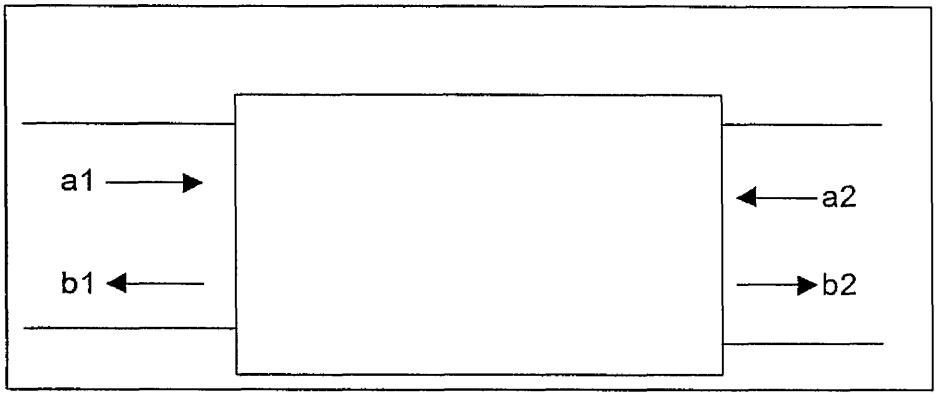

Figure 7.4 Schematic of a 2 port network.

S parameters are defined by:

$$S_{11}=\left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{21}=\left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{12}=\left.\frac{b_1}{a_2}\right|_{a_1=0} \qquad S_{22}=\left.\frac{b_2}{a_2}\right|_{a_1=0} \qquad (7.12)$$

Where a and b are the incident and reflection parameters at the port and b / a is the reflection coefficient at the termination. The parameters measured are the

magnitude and phase of voltage signals when the output is terminated in a matched load. S-parameters are complex numbers often displayed as phase and magnitude form. The transmission losses are $|S_{21}|$ or $|S_{12}|$ normally expressed in dB. The reflection losses are $|S_{11}|$ and $|S_{22}|$ normally expressed in dB. A smith chart representation [7.17] is used to display the complex S-parameters.

Measurement

A network analyzer [7.18] is used to measure microwave frequency 2 port scattering parameters (S parameters) [7.16].

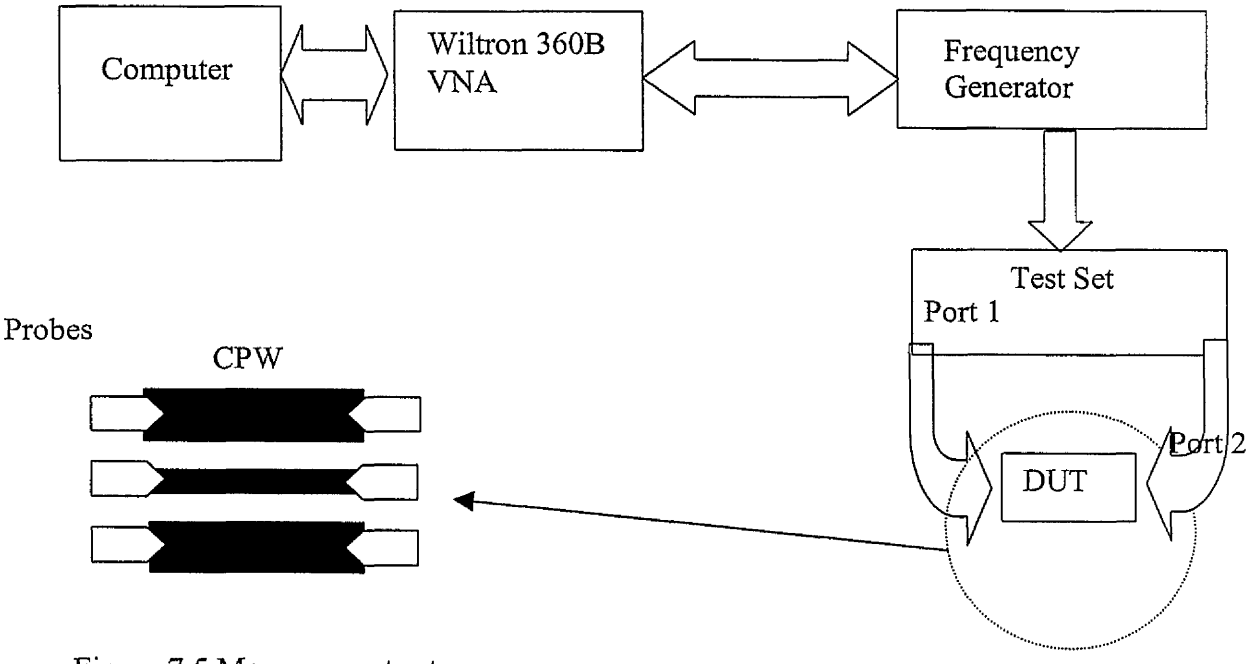

Figure 7.5 Measurement set-up

The frequency generator source provides the RF signal. The test set directs the flow of the RF signal to the test ports. The 380B vector network analyser controls the frequency generator and test set and returns the measured S parameters. Commercially available Wincal software is used to control the network analyser. The results of the measurement are complex S-parameters versus frequency in a standard S2P format. This format allows the S-parameters to be

used in commercial simulation packages such as "Touchstone" or "Microwave Office".

Calibration of the system is very important for accurate measurement. The system is calibrated to the probe tips using known standards. An ISS (Impedance Standard Substrate) is used with the SOLT (Short Open Load Thru) calibration technique [7.19].

7.6 Characterisation and Optimisation of Transmission Lines

Figure 7.6 shows the transmission losses $|S_{12}|$ in dB measured on 2.5 mm long lines from 0.04 – 60 GHz for various thickness of dielectric on a standard silicon substrate. The dimension of the coplanar waveguides were S = 15 μm W = 20 μm.

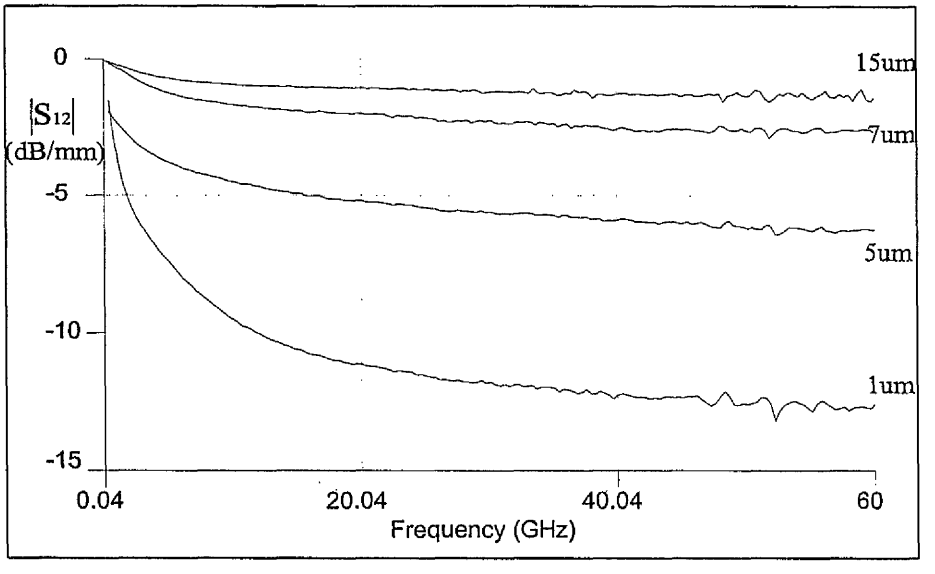

Figure 7.6 Transmission losses for various thickness of dielectric on silicon.

Figure 7.5 shows that a 15 μm thick layer of dielectric on the silicon substrate has acceptable losses of less than 0.6 dB/mm. Figure 7.7 shows the smith chart of S_{11} showing that for these CPW dimensions on the dielectric used, the line is not well matched to the 50 Ω load.

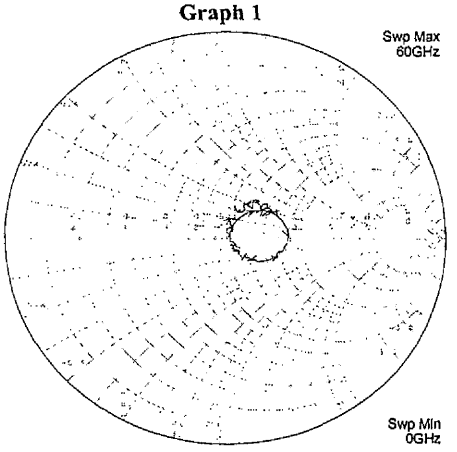

Figure 7.7 Smith Impedance Chart.

Proper characterisation of CPW mode and attenuation is best carried out when the characteristic impedance of the line matches the 50 Ω measurement system. In order to design CPW dimensions to obtain a 50 Ω characteristic impedance, the effective dielectric constant of the substrate must be known. An estimate of the effective dielectric constant, guide wavelength and phase velocity was made using (7.1) and (7.2) as follows

For a 2 mm transmission line the measured electrical length [ang(S_{21})] is 84 degrees at 20 GHz. The wavelength on the line is then

$$\lambda_g = \frac{360\,L}{\text{ang}(S_{12})} = \frac{360x2}{84} = 5.8 \text{ mm}$$

Then

$$v_p = f\,\lambda_g = 20 \text{ x } 0.0058 = 0.171 \text{ x } 10^9 \text{ m/s}$$

Then using

$$v_p = \frac{c}{\sqrt{\varepsilon}}$$

to get

$$\sqrt{\varepsilon} = \frac{c}{v_p} = \frac{3}{1.71} = 1.75$$

$$\varepsilon = 3.06$$

The low value of effective permitivity indicates that most of the wave propagation is concentrated in the air and the dielectric.

Design of optimum CPW dimensions for a 50 Ω line using was calculated using equation (7.2) with ε = 3 as approximately S = 70 μm, W = 20 μm. Transmission lines were fabricated with range of similar slot and conductor widths. Figure 7.8 shows the measured characteristic impedance as a function of conductor width for 25, 20, 15 and 10 μm gap at 10 GHz.

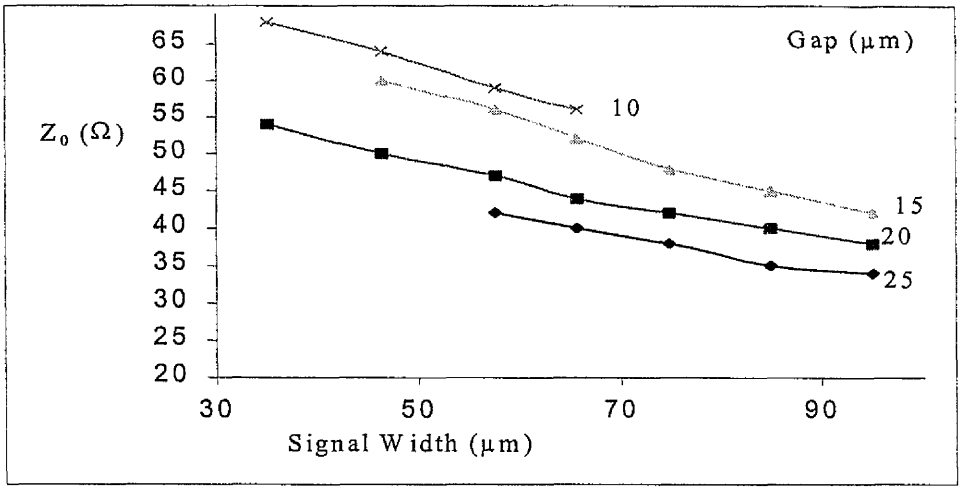

Figure 7.8 Measured Zo of various CPW dimension.

Figure 7.9 compares $|S_{12}|$ of a 50 Ω line on silicon with polyimide and photoresist as a surface dielectric with a 50 Ω line on a GaAs semi insulating substrate. The dimension of the 50 Ω line on silicon is 70 μm signal conductor and 20 μm gap. The dimension of the 50 Ω line on GaAs is 25 μm signal conductor and 15 μm gap.

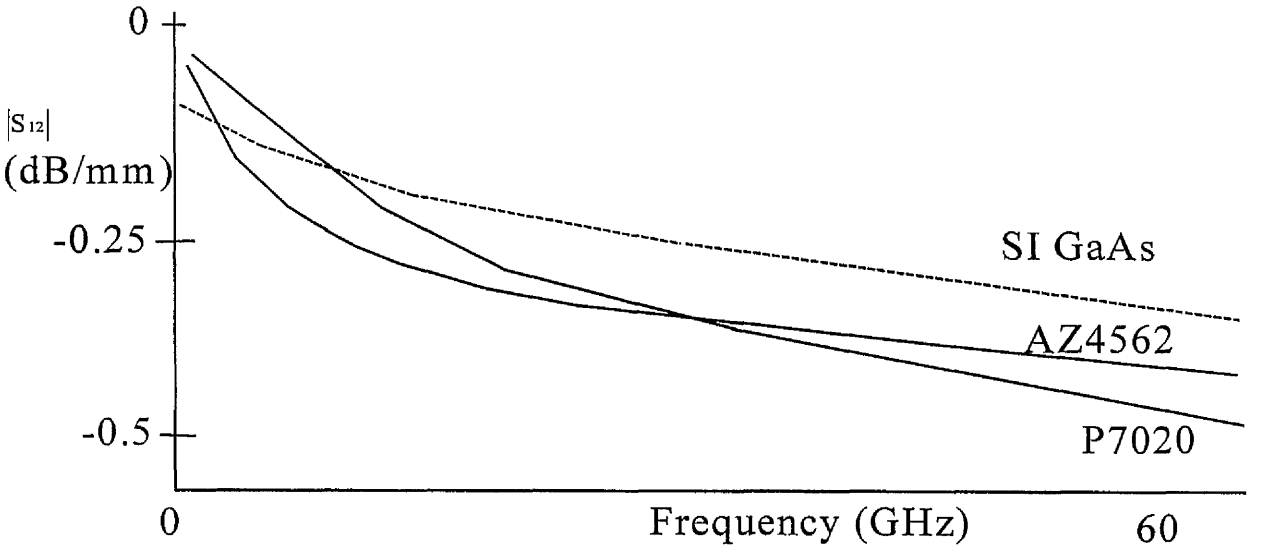

Figure 7.9 Attenuation versus frequency of 50 Ω CPW on silicon and GaAs.

The equivalent circuit (figure 7.3) parameters for the 50 Ω polyimide CPW are shown in table 7. 3.

R_{series}	R_{si}	L_{series}	C_{gap}	C_{si}	C_{poly}
1.5	160	0.05	0.02	0.04	0.9

Table 7.3 Equivalent circuit parameters for a 50 Ω polyimide CPW.

The low losses are attributed to the fact that the waveguide is separated from substrate by the 15 μm thick dielectric. A quasi-TEM mode propagates increasing R_{si} and reducing the dielectric loss. Figure 7.10 shows the phase velocity and relative effective permitivity as a function of frequency. A slow wave

mode propagates to about 15 GHz then a quasi TEM mode propagates for increased frequency.

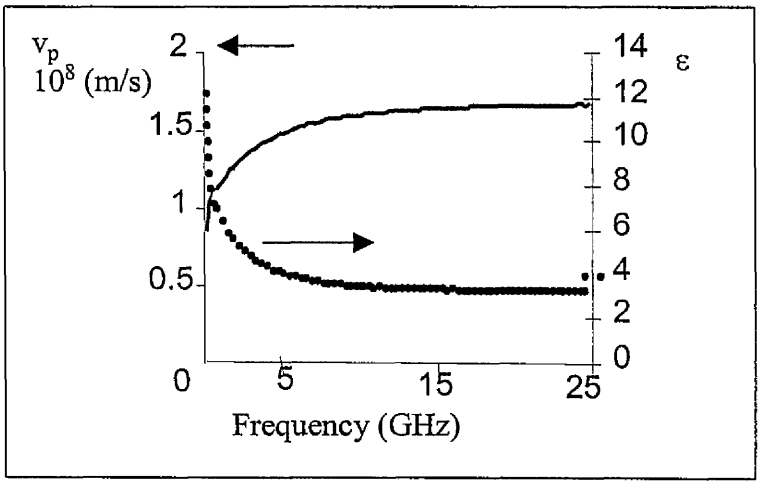

Figure 7.10 measured phase velocity and relative effective permitivity of a 50 Ω line on silicon with 15 μm of polyimide on top.

For the quasi TEM region the dielectric and conductor losses are extracted by a polynomial fit in figure 7.11.

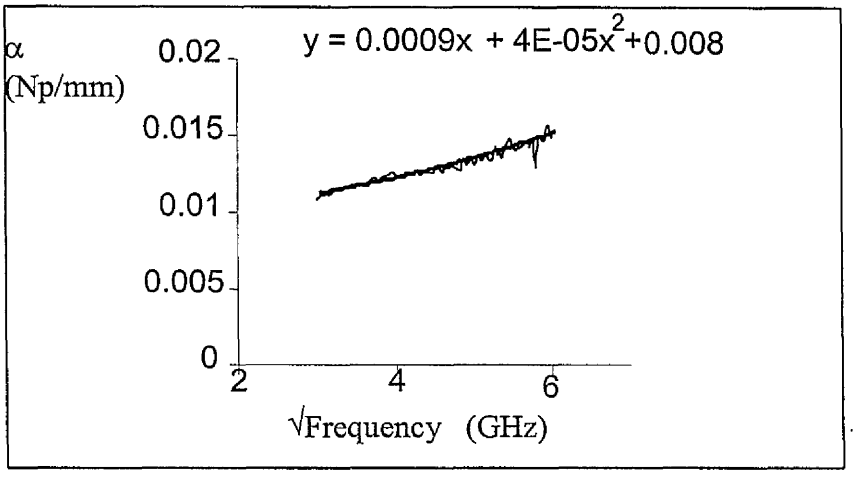

Figure 7.11 Polynomial fitted to data points between 10 GHz and 36 GHz.

Above 10 GHz a quasi TEM low loss mode propagates and from equation 7.8 and 7.10 by fitting a polynomial to the loss curve the conductor and dielectric losses are extracted to be approx.

$\alpha_c =$ 0.0009 Np / mm / $\sqrt{(GHz)}$

$\alpha_d =$ 0.00004 Np / mm / GHz

Clearly and as expected the conductor losses are dominant and in the quasi TEM mode the dielectric loss is minimal. This is further evidence that the 15 μm thick polyimide or resist layer provides a base for a transmission line on high resistivity silicon with losses that are limited by conductor loss.

7.3 Spiral Inductors

The inductor is an important passive circuit component for microwave circuit applications such as impedance matching networks and filters. In the frequency range up to about 10 GHz, a spiral inductor is used. For higher frequencies, an inductance is created by a short circuit length of transmission line known as a stub. A planar spiral inductor is often built on a GaAs semi insulating substrate. A single spiral of metal, normally Au is patterned on the substrate. The use of an airbridge or second layer of metal is required to make contact to the centre of the spiral. Figure 7.12 is an SEM of a spiral inductor with airbridge fabricated in this work.

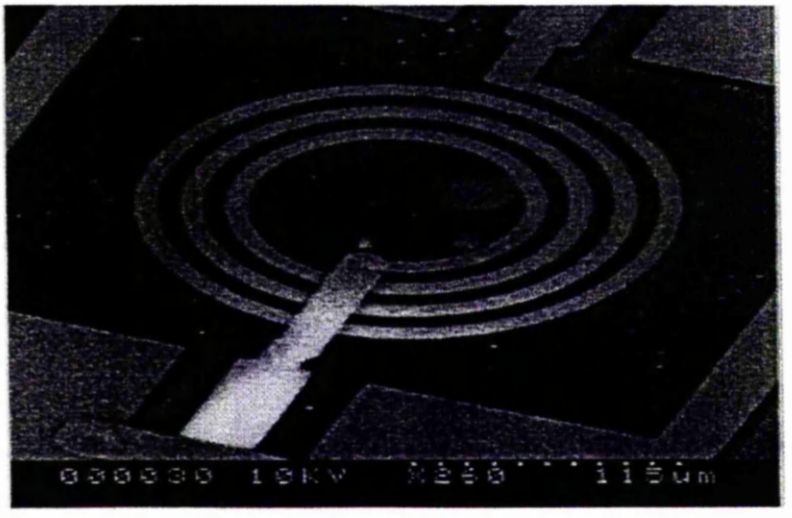

Figure 7.12 SEM of a 3.5 turn electroplated spiral inductor.

Values of inductance range from 0.5 nH –100 nH depending on the application. Q is a figure of merit indicating inductor quality, generally increasing L will decreases Q. The small signal equivalent circuit of a spiral inductor on a silicon substrate is shown in figure 7.13.

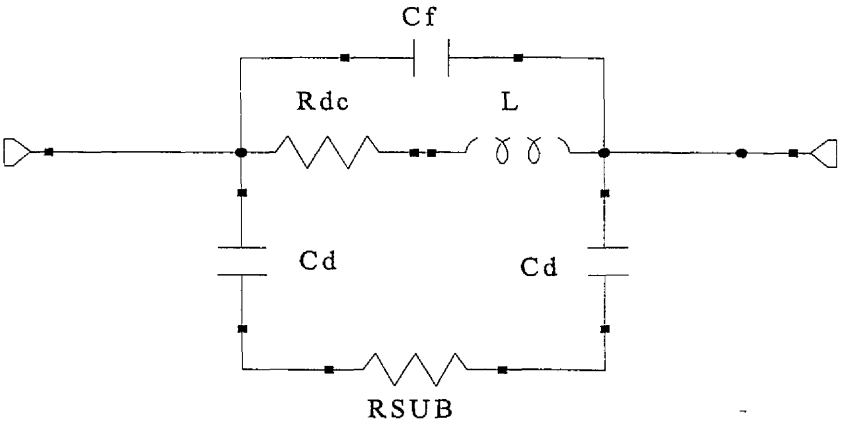

Figure 7.13 Small signal lumped element model for a spiral inductor on conducting silicon [7.20].

Where

C_f is the forward capacitance between the turns of the spiral.

L is the inductance.

R is the resistance of the spiral.

C_d is the capacitance between the spiral and the substrate.

R_{sub} is the resistance of the silicon substrate.

At low frequency, the circuit acts as an inductor, but as the frequency increases the effect of the capacitance C_d begins to dominate. The self-resonance frequency is defined as the frequency at which $2\pi fL = 1 / 2\pi fC_d$ at which point Q = 0. Below the self-resonance frequency, it can be shown for a matched 2 port measurement that

$$Q = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{\mathrm{Re}\left(1/Y_{11}\right)} \tag{7.13}$$

$$L = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{\omega} \tag{7.14}$$

Initial attempts to fabricate spiral inductors on a standard silicon process used a single layer spiral using 1.8 μm thick Al metalisation on a 1.7 um thick layer of oxide on CMOS grade Si. This pioneering work produced good inductors [7.21], table 7.6 summarises the performance of state of the art inductors. Using today's standard technology, multiple metal layers have been used to improve on inductor performance. By using up to 5 levels of metal each separated by a thick layer of oxide, the inductor is separated further from the substrate, decreasing substrate loss. In addition, the shunt-connected levels of metal reduce resistive loss in the spiral [7.22],[7.23]. Further reduction in metal losses is found by using AlCu or Cu metalisation [7.24]. It has also been shown that by etching the silicon in spaces between turns increases inductor performance [7.25], but this deviates somewhat from standard silicon processing. Other novel techniques using standard silicon processing have been used to further improve inductor quality. By using 2 layers of metal, with the first layer spiralling as normal to the centre and connecting the second layer such that it spirals out above the spaces of the lower spiral has been shown to increase L [7.26]. This has been called the MLS (Multi Level Spiral) structure. Patterned ground shields (PSG) placed directly on the substrate under the spiral have been shown to shield the electric field from the substrate reducing energy loss and increasing Q of a given spiral inductor by 10-33% [7.27]. Figure 7.14 shows a cross section of an inductor with patterned polysilicon ground plane using a standard 3-layer silicon process. New dielectrics

such as spin on polyimide with Au metalisation have been introduced recently [7.28].

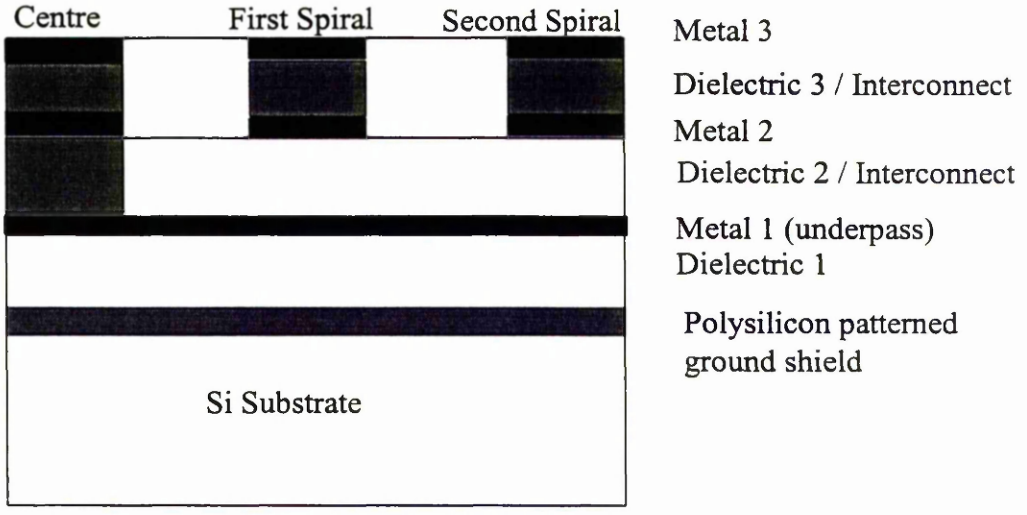

Figure 7.14, 2 level shunt connected spiral inductor with patterned polysilicon ground plane using a standard 3-layer silicon process.

Using the process described in this work, spiral inductors were fabricated on 2 Ω-cm silicon substrate with a 7 μm thick dielectric layer of photoresist. Figure 7.12 is an SEM of a spiral inductor fabricated using the described process.

Figure 7.14 shows the quality factor and inductance versus frequency obtained for a 2.5 turn inductor with conductor width and spacing of 15 μm on 7 μm of AZ4562 photoresist on 2 Ω-cm n-type silicon. The self-resonant frequency of this element is 25 GHz.

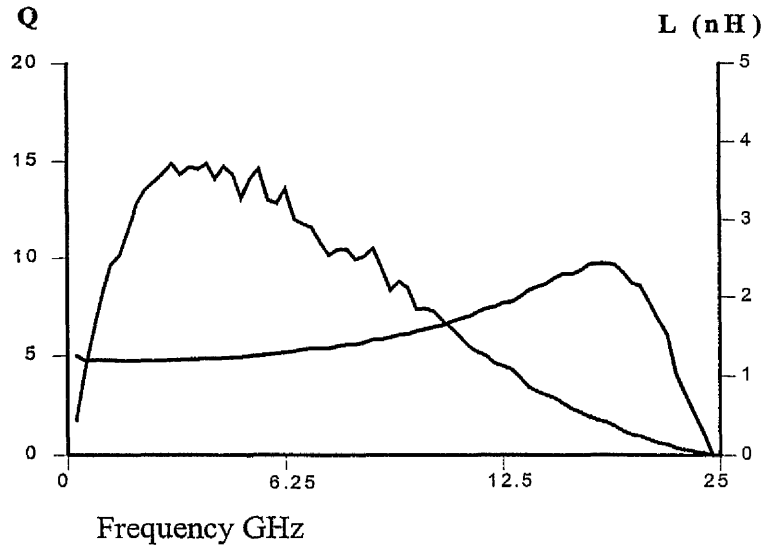

Figure 7.14 Quality factor and Inductance versus frequency for spiral inductor.

Using commercial simulation packages such as touchstone and microwave office, the above model can be simulated and output figures of merit such as S-parameters Q(f) and L(f) can be matched between the measurement and the model, producing lumped element values such that the model fits the measurement. In addition four probe measurements were made of the DC resistance of the spirals to verify the modeled value.

No of turns	Modeled res (Ω)	Meas DC res (Ω)
1.5	0.9 – 1.2	1.1
2.5	1.3 – 1.7	1.5

Table 7.4 Measured versus modeled resistance of spiral inductors.

Table 7.5 shows the results of the complete analysis on spiral inductors with various numbers of turns and varying signal and gap widths on only 7 μm of AZ4562 photoresist.

W, S (μm)	Turns	R Ω	L (nH)	C_1 (pF)	C_d (pF)	C_f (pF)	f_{sr} (GHz)	$Q_{max}(f)$/ (GHz)
15/15	1.5	1.2	0.63	0.02	0.1	0.001	50	16 / 10
15/15	2.5	1.7	1.2	0.03	0.1	0.001	25	15 / 5
15/15	3.5	3.2	2.7	0.03	0.1	0.001	15	10 / 3
15/15	4.5	3.6	2.9	0.04	0.1	0.001	13	8.5 / 2.5

Table 7.5 Q factor and Lumped element values for spiral inductors.

Table 7.6 compares the results from the literature using various techniques

L (nH)	**Q**	**f_Q (GHz)**	**f_{SR} (GHz)**	**Technique**
16	4.3	0.8	2.9	Standard Si process 4 levels Al as MLS structure [7. 26]
10	3	0.9	2.47	Pioneer work using single layer SiO_2 standard process [7.21]
10	17	2	11	100um Layer Polyimide 1 level of Au metalisation [7.28]
9	9.5	1.8	9	Standard silicon process single Al metal on layer 3 [7.26]
7.5	5	2	6.8	Al on 5.2 um Oxide with no ground shield [7.27]
7.4	6.8	2	3.6	Al on 5.2 um Oxide with polysilicon ground shield [7.27]
1.9	8	4.1	9.7	Pioneer work using single layer SiO_2 standard process [7.21]
1.95	9.3	4	20	Standard Si process with 3 layers AlCu [7.23]
1.45	24	2.3	24	Standard Si process with 5 levels of Al [7.23]
1.35	18	3.7		Standard Si process with 1 level of Cu [7.24]
1.2	15	6	25	This Work [7.29]

Table 7.6 Performance of spiral inductors on silicon substrates.

7.8 Conclusions

A process for the realisation of low loss coplanar waveguide transmission lines on a CMOS grade silicon substrate where photoresist and polyimide are used as a spin on dielectric has been presented. 50 Ω characteristic impedance CPW lines with a ground to ground spacing of 110 μm and a signal track width 70 μm realised on a 15 μm thick dielectric layer have losses less than 0.5 dB/mm at 60 GHz. As spin-on photosensitive dielectrics are used, pattern transfer is simple and is easily extended to a multi-layer process. Using an electroplated gold process, interconnect can be made between the waveguide and the device on the substrate. Initial spiral inductors fabricated on a 7 μm of dielectric with losses of 2.5 dB/mm have Q factors of 15. Using the 15 μm process described, higher quality factors are expected, in addition the electroplated interconnect process described will allow the fabrication of multi-level inductors and circuits. The work presented in this chapter provides a novel platform with which to fabricate monolithic microwave integrated circuits on a CMOS substrate. The use of thick gold on a spin on dielectric is simple and cheap in comparison to the multilayer methods described in the text and represents a major breakthrough. The next chapter goes on to the design of a single stage amplifier using this technology.

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Chapter 8

Single Stage Amplifier Design

Introduction

This is a short chapter that was made possible because of the success of the MOSFET fabrication process and the passive RF elements now possible. It has already been shown that as a result of this work that high quality passive and active elements using MOSFET technology can be fabricated at Glasgow.

In this chapter, using the results so far obtained, a single stage amplifier is proposed. The amplifier is designed in a very simple way based on the measured results obtained to date. The amplifier is currently in fabrication.

8.1 Single Stage Amplifier Design

Designing an amplifier is no simple task and a number of design methods exist. In this work a general method using S-parameters is described and used to design a simple single stage amplifier. The amplifier is designed with a simple topology based on the active and passive elements described in this work.

The four 2 port S-parameters applicable to a two port device and some typical values for a single stage amplifier are given in table 8.1 and figure 8.1.

S-Parameter	Definition	Typical (dB)
S_{11}	Input reflection coefficient	-3
S_{22}	Output reflection coefficient	-6
S_{21}	Forward transmission coefficient	6
S_{12}	Reverse transmission coefficient	-20

Table 8.1 S-Parameter definitions and typical values.

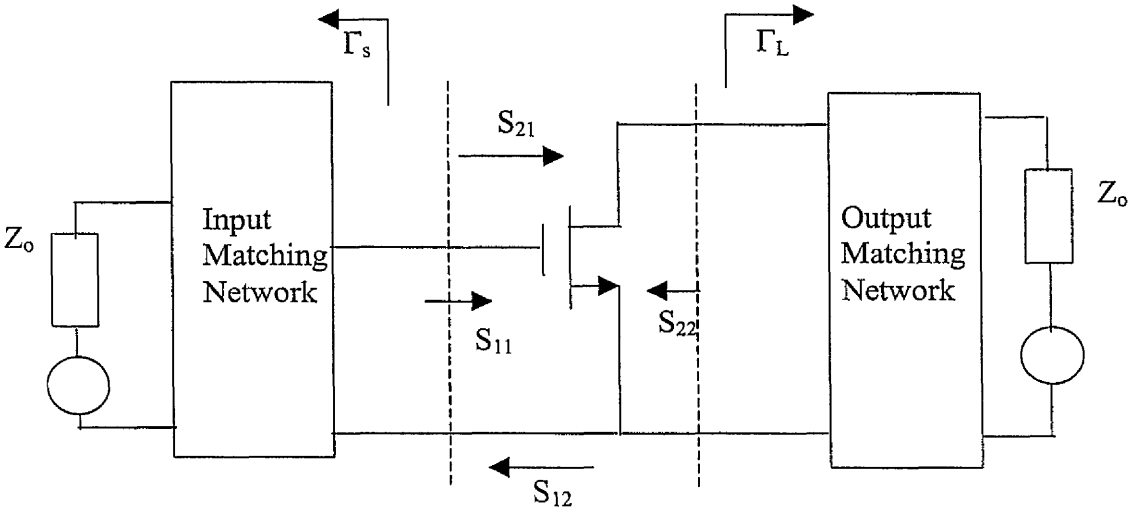

Figure 8.1 Single stage amplifier with input and output matching networks.

By making the assumption that the device is unilateral i.e. $|S_{12}| = 0$ a simple design method can be used. The transducer power gain of the complete amplifier is defined as the power delivered to the load divided by the power available at the source and for a unilateral device is given by [8.1] [8.2]

$$G_T = \frac{1-|\Gamma_s|^2}{|1-S_{11}\Gamma_s|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} \qquad 8.1$$

There are three terms in the formula and each can be thought of a independent gain terms

1. The gain or loss produced by the input matching network.
2. The gain of the active device, $|S_{21}|^2$.
3. The gain or loss produced by the output matching network.

The input and output matching networks are designed such that, the impedance of the input matching network is the complex conjugate of the S_{11} of the device and the impedance of the output matching network is the complex conjugate of S_{22} of the device. In such a case the maximum gain is given by

$$G_{max} = \frac{1}{1-|S_{11}|^2}|S_{21}|^2\frac{1}{1-|S_{22}|^2} \qquad 8.2$$

There are certain values of the source and load impedance that may cause the FET to oscillate. A unilateral device is said to be unconditionally stable if $|S_{11}|$ and $|S_{22}| < 1$, that is any source or load impedance can be applied and the circuit will not oscillate. If $|S_{11}|$ or $|S_{22}| > 1$ very careful design is required to make a stable device, fortunately the devices fabricated in this work can be considered unilateral and unconditionally stable.

There are many methods incorporating lumped and distributed elements to implement the impedance of the matching network. In this work the source regeneration method [8.3] [8.4] is used. The schematic diagram of a single stage amplifier using source regeneration is shown in figure 8.2. Using the actual device measurements and the spiral inductor model presented in chapters 6 and 7, the commercially available software 'Microwave Office' is used to simulate the circuit. The values of inductors can be adjusted so that the circuit is matched and hence provides a narrow band gain around a particular frequency. Figure 8.3 shows the simulated $|S_{21}|$, $|S_{11}|$, $|S_{22}|$ of amplifiers tuned to 4 GHz and 6.5 GHz. Table 8.2 lists the matched frequency, inductance and gain obtainable using different values of inductor.

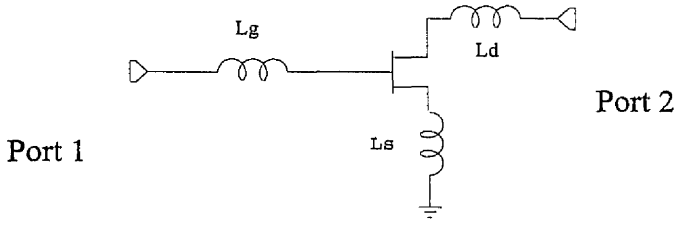

Figure 8.2 Schematic of single stage amplifier using source regeneration.

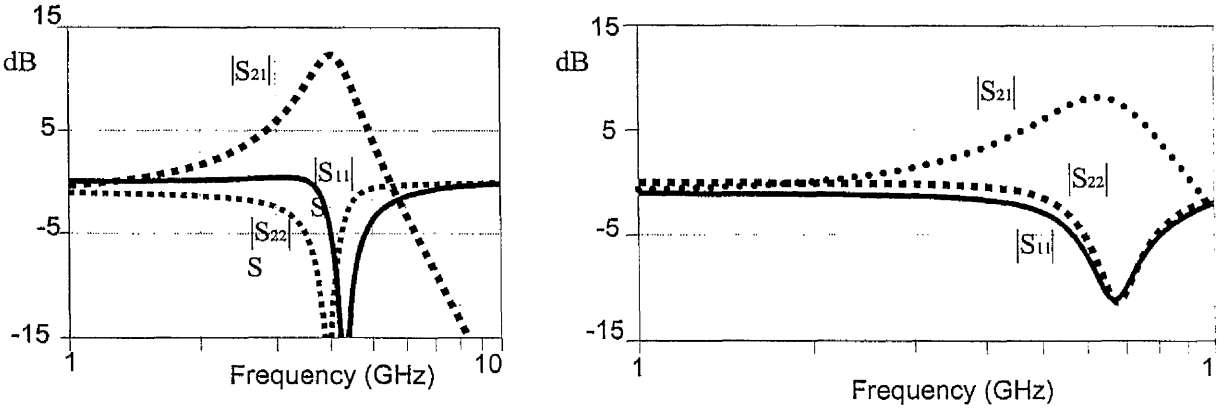

Figure 8.3 Modelled performance of a single stage amplifier matched 4 GHz and at 6.5 GHz.

f (GHz)	L_s (nH)	L_d (nH)	L_g (nH)	Gain (dB)
2	2	8.6	20	10.7
3	1.1	4.4	9	8.2
4 *	2.5	9.5	10	13
4	1	2.2	5.5	6.2
5	0.5	3	3	4.5
6.5 *	1	2.3	5.8	8

Table 8.2 Matched frequency and gain for various values of the inductance.

8.3 Conclusions

Using measured data from spiral inductors and devices, single stage conjugate matched amplifiers are designed. Single stage matched amplifiers are readily fabricated using processes described.

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Chapter 9

Conclusions and future work

Summary

A complete fabrication process has been developed for the realisation of Si/SiGe microwave integrated circuits (SIMICs). Using the process, a number of active and passive elements for microwave circuits have been demonstrated including

1. Metal gate p-SiGe MOSFETs [1].
2. Low loss transmission lines on CMOS grade silicon [2]
3. High quality spiral inductors on CMOS grade silicon [2].
4. High performance metal gate strained silicon n-MOSFETs [3].

Single stage amplifiers have been designed based on the technology developed in this work [3].

The MOSFETs have good DC performance. Strained SiGe p-channel MOSFETs with 1 μm gate length have an extrinsic transconductance of 36 mS/mm. Strained silicon n-channel MOSFETs with 0.3 μm gate length have extrinsic transconductance of 230 mS/mm. The RF performance of a metal gate 0.3 μm gate length strained silicon MOSFET is measured, with cut off frequency and maximum frequency of oscillation of 20 GHz and 21 GHz respectively. Coplanar waveguide transmission lines of 50 Ohm characteristic impedance, fabricated using spin on dielectrics on a CMOS grade silicon substrate, have losses less than 0.5 dB/mm up to 60 GHz. Spiral inductors fabricated on the low loss dielectric have $Q > 15$. Using the passive and active element library developed, single stage amplifiers were designed with gain of 12 dB at 3 GHz or 7.5 dB at 6GHz, and are now under construction.

The device layer structures were designed using a simple 1D Poisson solver. The p-channel device used a concentration graded SiGe channel to obtain high mobility and carrier concentration. The n-channel RF device with a strained

silicon channel incorporates a metal gate technology that is directly responsible for the high values of f_{max} achieved.

The spiral inductors and coplanar waveguides are fabricated using a spin on dielectric process to separate them from the lossy silicon substrate. The same technology is used to reduce the parasitic capacitance of device contact pads.

The engineering conclusion of this work is that SIMICs, for applications in the frequency range 1 to 10 GHz, can be made with the current passive and active element library at the University of Glasgow. Further improvement in both passive and active element performance to increase the frequency is set out in future work.

From a practical viewpoint a process is now in place that will underpin the University of Glasgow's Si / SiGe SIMIC projects in the future.

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9.2 Conclusions

MOSFETs

SiGe layer structures were used in this work for the fabrication of p and n-channel MOSFETs. The device performance was measured at both DC and RF.

The SiGe p-channel MOSFETs with tungsten gates are the first such device to be fabricated. Metal gate technology for CMOS applications is become the focus of some attention. The use of a SiGe channel to improve on the p-channel devices in CMOS circuits is also becoming popular. To the author's knowledge, this is the first work to combine the two emerging technologies. In only one iteration of the process, MOSFETs of 1 um gate length were fabricated with DC transconductance comparable with the state of the art. These devices resulted in the first publication from this work in Electronics Letters.

The main aim of this project was to develop a fabrication process at the University of Glasgow that could be used to investigate the possibility of monolithic silicon microwave integrated circuits. This was done by the creation of a Ti/Pd/Au gate process suitable for fabricating n-channel MOSFETs with gate length as short as 120nm with T shaped gates. The initial devices fabricated with the developed process were strained silicon n-channel devices. Despite the problems in obtaining a suitable Si/SiGe layer structure, the initial, devices were successfully fabricated with cut off frequency and maximum frequency of oscillation of 20 GHz and 21 GHz respectively. This is a major achievement for the first iteration of the process.

Coplanar Waveguide Transmission Lines and Spiral Inductors

Low loss coplanar transmission lines have been fabricated on low resistivity silicon substrates. High Q inductors have been fabricated using exactly the same technology as the CPW lines. The ability to fabricated low loss CPW and high Q inductors on CMOS grade silicon is a major breakthrough. The simple fabrication method will allow the fabrication and design of circuits using devices fabricated in house. In addition, the process can be used to provide 'back end' processing of standard silicon devices from state of the art facilities.

Circuits

A demonstration circuit is designed incorporating the active and passive elements developed in this work and is currently in fabrication.

9.3 Current Work

The amplifier designed in chapter 9 is now under construction. In addition, MOSFETs are currently being fabricated using the optimised n-Si/SiGe depletion mode structure designed in chapter 4. Further, the devices now in fabrication have T shaped gates to reduce the gate resistance. In addition to that, a self aligned ohmic contact process using the T gates has been developed and will be used to reduce the source and drain resistance.

Using a T gate to enable a self aligned ohmic contact is not new to III-V technology, but has not been used in silicon because self aligned silicides are available as standard. Figure 9.1 is an SEM of a Ti/Pd/Au T gate of 120 nm footprint followed by the evaporation of 50 nm Ti and annealed at 600 C for 30 secs. The SEM shows that the T gate, in addition to reducing further the gate resistance, allows the evaporation of the non-silicide ohmic contact to within 100nm of the channel.

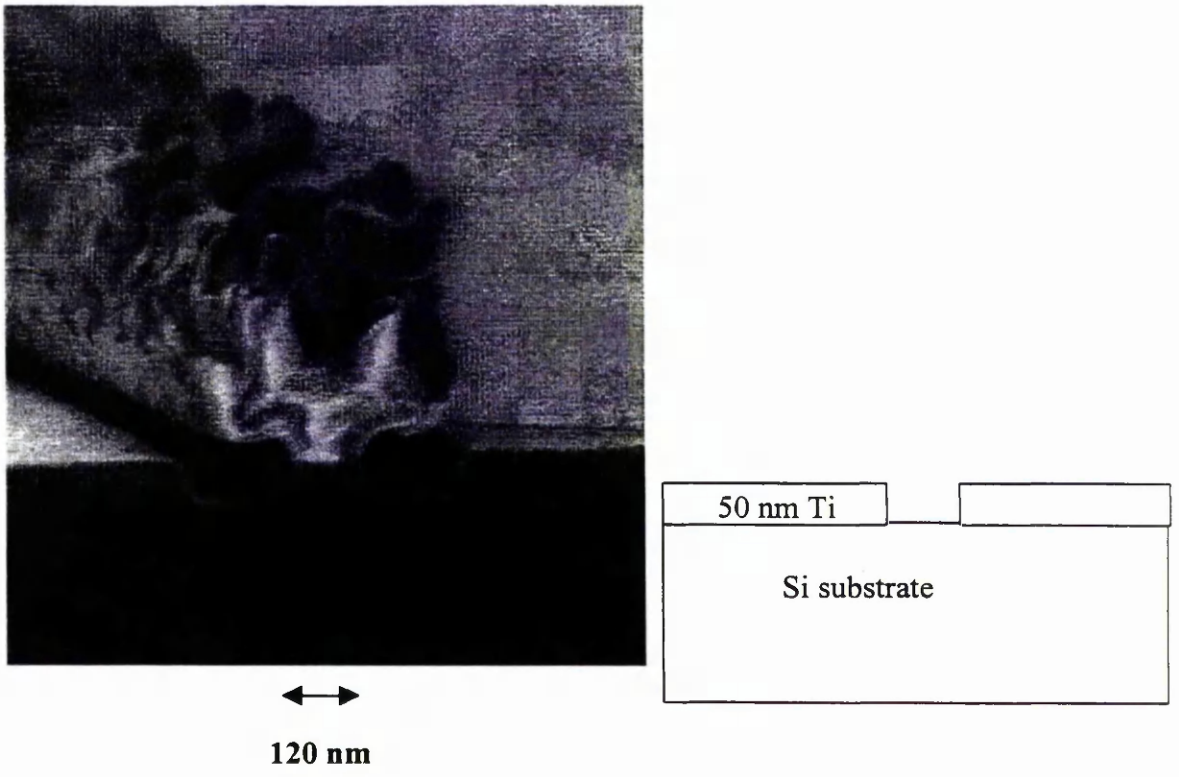

Figure 9.1 SEM of a self-aligned T gate of 120 nm gate length on silicon.

9.4 Future Work

This work has produced a platform from which the fabrication of silicon based microwave integrated circuits can be designed and fabricated. The demonstration processes developed here require optimisation in four fronts.

1) The processes as they are should be carried out regularly with yield issues identified and eliminated.

2) Optimisation of devices will require a reduction in the parasitic series resistance. It is entirely possible to use low temperature silicide technology on the metal gate devices to provide higher f_t. A novel self aligned ohmic contact method using T gates has been presented and is currently being applied. The parasitic probing pad capacitance still has room for improvement and this can be done with smaller gatefeed pads.

3) Further reduction in losses for transmission lines may be possible by using thicker dielectric, reducing the signal line width or by using evaporated gold. A complete passive element library is required.

4) Other steps include, reducing the gate length including proper scaling of a depletion mode layer structure.

5) Finally, the design and fabrication of Si/SiGe microwave integrated circuits can now be carried out at Glasgow in the frequency range 1-10 GHz. If the current research is successful, it may enable the fabrication of microwave circuits in the frequency range 10 – 100 GHz.

APPENDIX 1

To date three publications have been accepted for publication as a result of this work, the title, authors and journals are listed below. Each paper follows

SiGe p-channel MOSFET's with a Tungsten Gate

G.Ternent A.Asenov I.G.Thayne D.S.MacIntyre S.Thoms C.D.W.Wilkinson E.H.C.Parker and A.M.Gundlach

Electronics Letters 4th March 1999 Vol. 35, No. 5, pp 430 – 431.

Coplanar waveguide transmission lines and high Q inductors on CMOS grade silicon using photoresist and polyimide

G.Ternent S.Ferguson, Z.Borsosfoldi, K.Elgaid, T.Lohdi, D.Edgar, C.D.W.Wilkinson I.G.Thayne.

Electronics Letters 28th October 1999 Vol. 35, No. 22, pp 1957 – 1958.

Single stage amplifiers on a CMOS grade silicon substrate using a polymer interlayer dielectric with strained silicon MOSFETs

G.Ternent, D.L.Edgar. H.McLelland, F.Williamson, S.Ferguson, S.Kaya, C.D.W.Wilkinson, I.G.Thayne, K.Fobelets, J.Hampson

Asia Pacific Microwave Conference , Sydney 2000

SiGe p-channel MOSFET's with a Tungsten Gate

G.Ternent A.Asenov I.G.Thayne D.S.MacIntyre S.Thoms C.D.W.Wilkinson E.H.C.Parker and A.M.Gundlach

A self-aligned SiGe p-channel MOSFET tungsten gate process with 0.1 μm resolution is demonstrated. Interface charge densities of MOS capacitors realised with the low pressure sputtered tungsten process are comparable with thermally evaporated aluminium gate technologies ($5x10^{10}$ cm^{-2} and $2x10^{11}$ cm^{-2} for W and Al respectively). Initial results from 1 μm gate length SiGe p-channel MOSFETs using the tungsten-based process show devices with transconductance of 33 mS/mm and effective channel mobility of 190 cm^2/Vs.

Introduction: Recently there has been significant improvement in the performance of SiGe p-channel MOSFETs, strained Si n-channel MODFETs and scaled bulk Si devices [1,2,3]. The motivation for these enhancements is driven by CMOS shrinkage requirements, but also by the goal of realising microwave and millimetre wave Si-based transceiver circuitry compatible with a standard CMOS process flow.

One of the outstanding technological issues limiting the performance of 0.1 μm gate length Si-based MOSFETs for both CMOS and RF applications is the high resistance of conventional poysilicon gate processes[4]. This has led to the development of complex silicide and salicide gate stack processes[5] as well as the demonstration of metal gate CMOS devices[6].

In this paper a self-aligned SiGe p-channel MOSFET tungsten gate technology with 0.1 μm resolution is described, together with the first results on 1 μm gate length SiGe p-channel MOSFETs realised with the process.

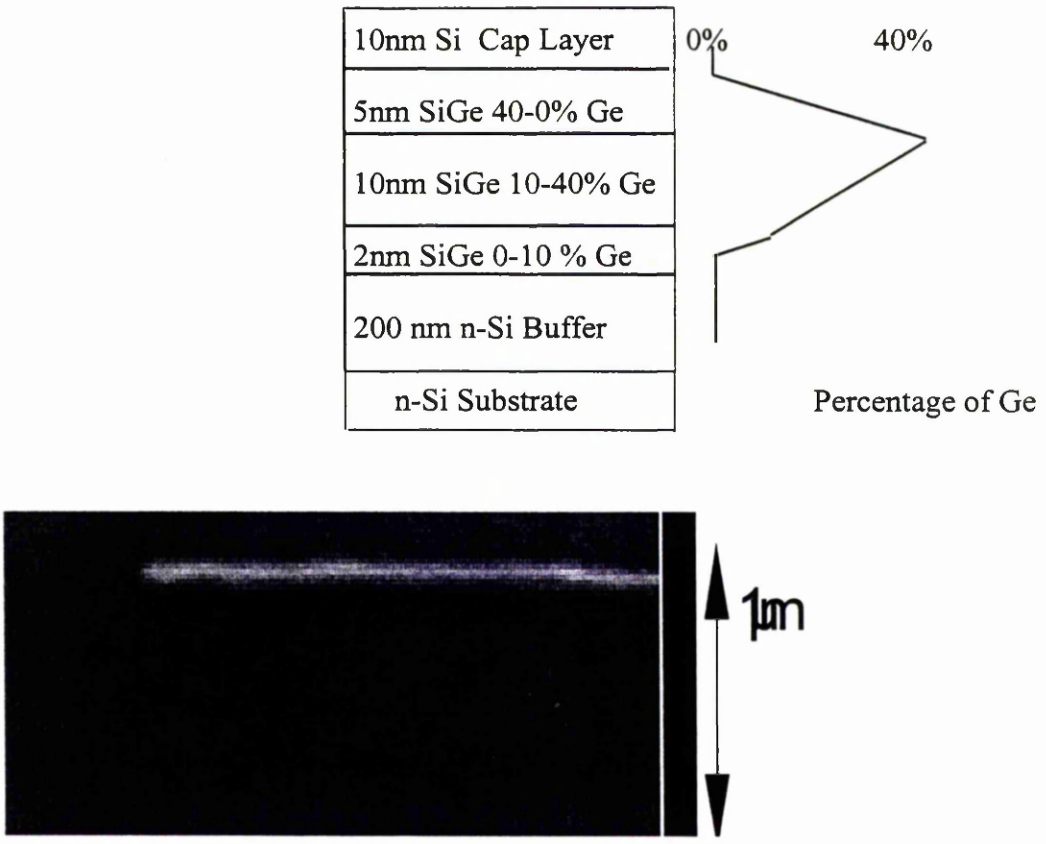

Figure 1. Layer structure showing percentage of Ge concentration, and SEM of 100nm W gate.

(a) Layer structure.

(b) SEM of a 100 nm W Gate.

Fabrication : The layer structure on which devices are fabricated was grown by MBE and is shown in figure 1(a). Using both step and linear grading, a maximum Ge concentration of 40% in the channel was achieved. The 200 nm buffer layer, doped at $5x10^{17}$ cm^{-3} n-type with Sb, is grown on an n-type Si substrate doped at $5x10^{16}$ cm^{-3}. The channel comprises 3 layers : a 2 nm SiGe layer graded from 0–10% Ge followed by a 10 nm SiGe layer graded from 10-40% Ge then a 5 nm SiGe layer graded from 40-0% Ge. Approx 5 nm of the 10 nm Si cap layer is consumed during the cleaning and oxidation processes. All layers above the buffer are nominally undoped at a background level of 10^{15} cm^{-3} n-type.

The device process flow begins with the growth of a 6 nm gate oxide using a 200 minute dry thermal oxidation performed at 750 °C to prevent any out-diffusion of Ge during the oxide growth. A further 30 minute 750 °C anneal in an argon

The device process flow begins with the growth of a 6 nm gate oxide using a 200 minute dry thermal oxidation performed at 750 °C to prevent any out-diffusion of Ge during the oxide growth. A further 30 minute 750 °C anneal in an argon atmosphere results in a device quality oxide layer. Next, the 100 nm thick tungsten gate is deposited by RF sputtering at a pressure of 2 mTorr and power of 100 W. To enable an assessment of the damage induced by the sputtered tungsten process, 100 nm thick thermally evaporated aluminium gate MOS capacitors were also defined for comparison.

Tungsten gates with minimum feature sizes of 100 nm as shown in Figure 1(b), were fabricated using a Leica Microsystems Lithography LTD EBPG5 beamwriter and AZPN114 negative tone resist to define the geometry, followed by tungsten patterning with a 2 minute, 100 W SF_6 reactive ion etch performed at 9 mTorr. In-situ reflectometry was used during the SF_6 etch to stop the gate metal etch on the thin 6 nm SiO_2 layer[7].

The self-aligned source and drain contacts were produced using a shallow (<100 nm) BF_2 implant at an energy of 10 keV and a dose of 10^{15} atoms/cm^2 activated by a 10 second 900 °C anneal. Source and drain metallisation of 100 nm AlSi was followed by a 5 minute 400 °C anneal. Finally, the devices were shallow trench isolated with a 5 minute, 100 W SF_6 reactive ion etch performed at 9 mTorr

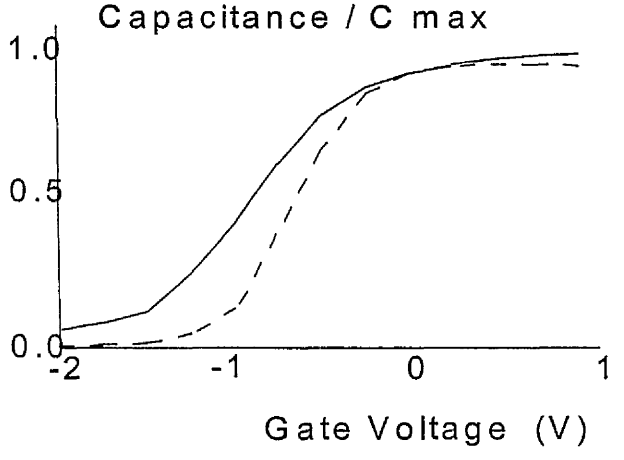

Figure 2. CV Characteristics of W and Al MOS capacitors (20 nm thick oxide).

——————— Al, $Q_{int} = 2 \times 10^{11} cm^{-2}$

---------- W, $Q_{int} = 5 \times 10^{10} cm^{-2}$

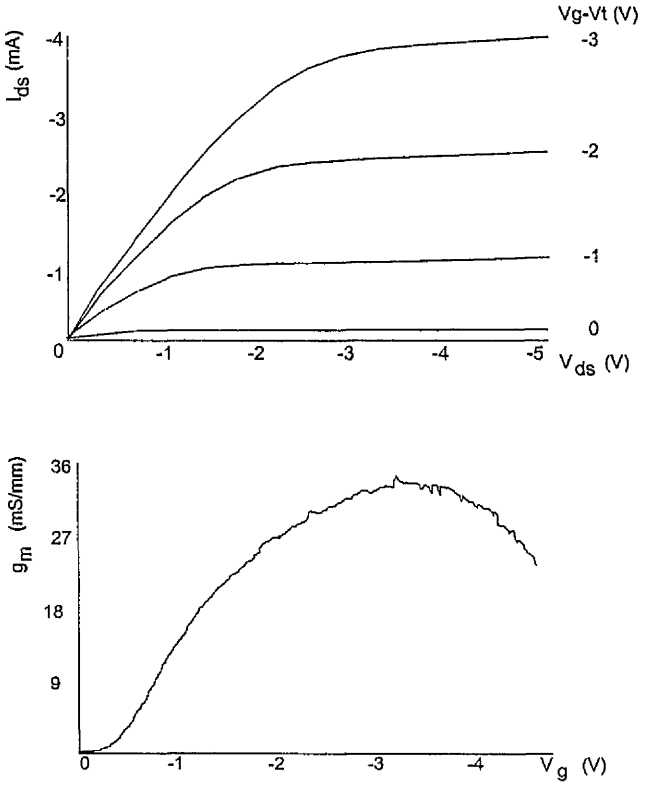

Figure 3. IV and g_m Characteristics of a 1 μm x 100 μm p-SiGe W gate MOSFET.

Results : Figure 2 shows the CV curve of SiGe-SiO_2 capacitors realised using both the sputtered tungsten and evaporated aluminium gate metallisations. The interface charge densities calculated from the flatband voltage shifts are $5x10^{10}$ cm^{-2} and $2x10^{11}$ cm^{-2} for W and Al respectively showing the sputtered tungsten gate process is low damage. In addition the larger work function of tungsten results in a lower flatband voltage and thus a reduced threshold voltage when compared with the aluminium gate capacitors.

Using both the van der Pauw and four probe TLM methods, the resistivity of the 100 nm thick sputtered tungsten gate metal film was determined to be 1.2 Ohms/square, a factor of 3 lower than similar geometry polysilicon and silicide gate structures[8]. The measured resistivity was independent of gate length down to 100 nm.

Figure 3 shows the $I_{ds}(V_{ds}, V_{gs})$ and $g_m(V_{gs})$ characteristics of a 1 x 100 μm gate length SiGe MOSFET realised using the process described above. The maximum extrinsic transconductance is 33 mS/mm. Estimating the channel hole concentration from the C(V) characteristic of the device and accounting for the channel access resistance of 500 Ohms measured with TLM structures, an effective channel mobility of 190 cm^2/Vs was extracted from the channel conductance at low drain bias (V_{ds} = -0.1 V).

Conclusion : We have demonstrated a self-aligned SiGe p-channel MOSFET tungsten gate process with 0.1 μm resolution. Interface charge densities of MOS capacitors realised with the low pressure sputtered tungsten process are comparable with thermally evaporated aluminium gate technologies ($5x10^{10}$ cm^{-2} and $2x10^{11}$ cm^{-2} for W and Al respectively) indicating the process is low damage. The use of a tungsten gate produces devices with gate resistances of 1.2 Ohms/square independent of gate length down to 100 nm, making this process an attractive candidate for the realisation of low gate resistance devices for RF applications.

Initial results from 1 μm gate length SiGe p-channel MOSFETs using the tungsten-based self-aligned gate process yielded transconductance of 33 mS/mm and effective channel mobility of 190 cm^2/Vs.

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Coplanar Waveguide Transmission Lines and High Q Inductors on CMOS Grade Silicon using Photoresist and Polyimide.

G.Ternent, S.Ferguson, Z.Borsosfoldi, K.Elgaid, T.Lohdi, D.Edgar, C.D.W.Wilkinson, I.G. Thayne

Abstract: Gold coplanar waveguide (CPW) transmission lines with losses of less than 0.5 dB/mm at 60 GHz have been produced on CMOS grade silicon substrates using a 15μm thick layer of either photoresist or polyimide. This process, together with an electroplated interconnect technique has been used to produce spiral inductors on a 2-Ohm cm n-Si substrate with Q of 15 and L of 1.2nH at 6GHz.

Introduction: Recent interest in the realisation of CMOS RF circuits has resulted in great activity in silicon microwave research [1]. Leading the way, SiGe RF mixers and low noise amplifiers are now commercially available [2]. Techniques for producing high Q inductors on CMOS grade Si substrates have been presented [3], and circuits operating up to 2GHz with standard submicron CMOS devices have been produced [4]. Furthermore Si and SiGe FETs with impressive millimetre-wave performance have been demonstrated [5,6]. However the requirement of low loss transmission lines means that the majority of RF circuit demonstrators reported to date, have been fabricated on high resistivity silicon substrates. Polyimide has been used as a spin on dielectric for low loss transmission lines [7] however this is relatively difficult to pattern/etch and spiral inductors with high Q on CMOS grade silicon substrates have so far required polyimide thickness of 100μm [8]. This letter presents a simple, readily available fabrication technology for low loss transmission lines on a standard silicon substrate together with a complete solution for interconnect between device and transmission line.

Coplanar waveguide transmission lines were fabricated and characterised using both polyimide and photoresist as a spin on dielectric layer on silicon substrates. The effective dielectric constant of the substrate has been extracted and transmission line dimensions for 50 Ohm matching were calculated and measured up to 60GHz. The 2um thick electroplated gold transmission lines have measured

losses of less than 0.5dB/mm at 60 GHz, comparable with III-V technology. An essential addition to the technology is the demonstration of an electroplated vertical interconnect plug down to devices on the CMOS grade substrate. Using this process, spiral inductors with Q factor of 15 have been realised on a CMOS grade Si substrate.

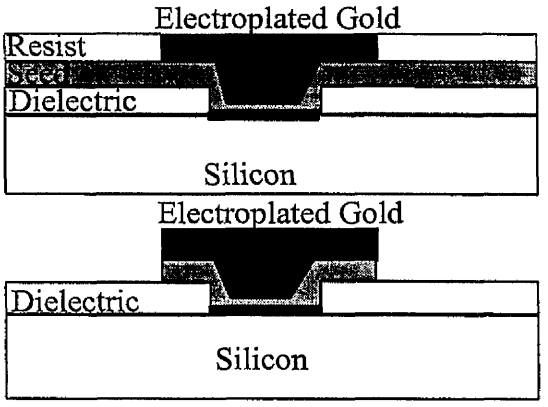

Figure 1. Fabrication steps of electroplated transmission lines and interconnects.

Fabrication: All of the structures were fabricated on a 2-Ohm cm n-Si substrate. Figure 1 shows the fabrication steps including the interconnect process. First the devices (or in the case of this development sample, metal lines for contact chains) are fabricated on the silicon substrate. Then the dielectric is deposited. Two spin on technologies are compared, a single layer of P7020 polyimide and 2 layers of AZ4562 photoresist. The polyimide is spun at 2000rpm for 15 seconds then post baked at 90C for 10 minutes, the resulting layer thickness is 30μm. The photoresist is spun at 4000rpm for 30 seconds and post baked at 90C for 20 minutes before a second layer is spun and baked with the same procedure, resulting in a 15μm thick layer. The contact windows in the dielectric are patterned using standard photolithography. Following pattern transfer, the photoresist is baked at 180C for 2 hours and the polyimide at 350C for 30 minutes to ensure that the dielectrics are no longer soluble in either acetone or hydroflouric acid. Post baking the polyimide reduces its thickness to 15μm. The wafer is then blanket coated in TiAu by evaporation. A single layer of S1818 photoresist is then spun and the contact windows defined. Then the top layer waveguides are patterned in this

photoresist layer. Finally 2μm of gold is electroplated, resist is removed and gold etched leaving transmission lines and interconnect. Figure 2 is an SEM of an airbridged spiral inductor produced using this process on top of the dielectric film.

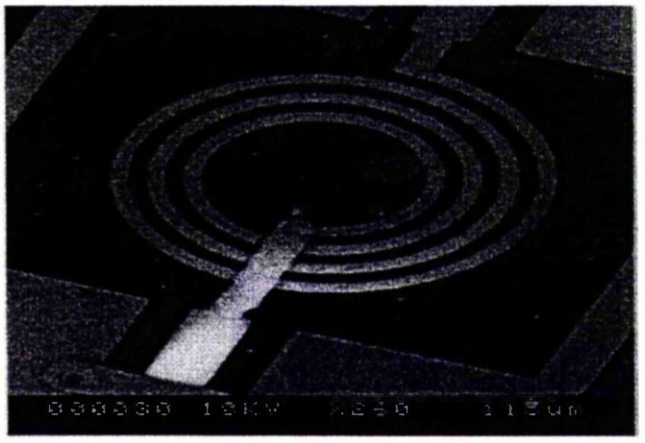

Figure 2. SEM of a 3.5 turn spiral inductor.

Results: From initial measurements on various waveguide dimensions, the effective dielectric constant of a 15μm thick layer of AZ4562 photoresist or single layer of P7020 polyimide on a CMOS grade Si substrate was found to be 6.0. Using this information, 50 Ω characteristic impedance CPW transmission lines with a ground to ground spacing of 110μm and signal track width of 70μm were designed and fabricated. Figure 3 shows the measured transmission loss measured of 2.5 mm long lines fabricated on both dielectrics. For comparison, the measured loss of a 1.2μm thick evaporated gold transmission line fabricated on semi insulating GaAs is also shown in Figure 3.

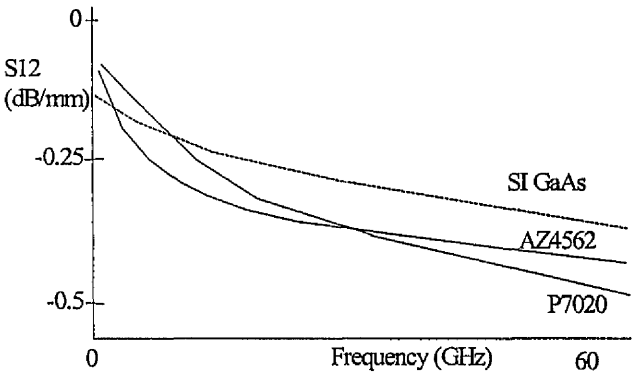

Figure 3. Measured insertion loss of electroplated waveguides on AZ4562 and P1208 compared with GaAs.

DC contact chains to verify the feasibility of the electroplated plug process showed that reliable, low resistance contacts can be made through photoresist using 25μm x 25μm plugs, whilst plugs through polyimide need to be at least 75μm x 75μm. To test the RF properties of the plugs, CPW transmission lines on the dielectric were connected down onto transmission lines on the substrate then back up to the dielectric in the form of a contact chain. Measurements up to 60GHz show that other than a slight increase in losses due to a short section of the transmission line being on silicon, characteristic impedance and insertion loss is not seriously effected.

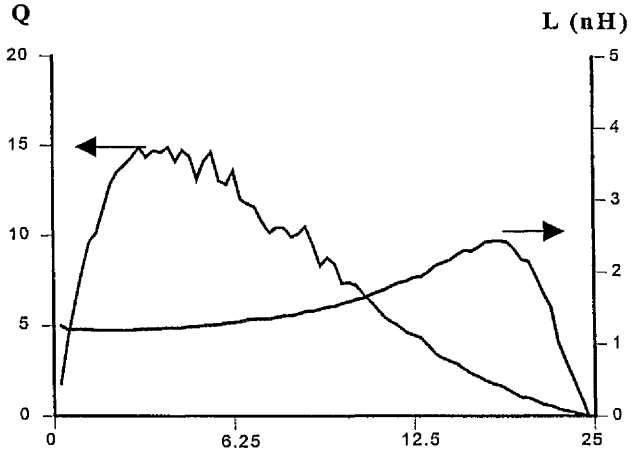

Figure 4. Quality factor and inductance versus frequency for a 2.5turn 1.2nH Spiral Inductor.

Spiral inductors of various dimensions were fabricated on the dielectric using 2μm electroplated gold, and completed by airbridging. Figure 4 shows the inductance and quality factor versus frequency for a 2.5 turn 1.2nH spiral inductor realised with a developmental 7μm photoresist layer process. The Q factor and inductance were calculated from Q= Im(1/Y11)/Re(1/Y11) and L=Im(1/Y11)/2πf, where Y11 was calculated from S-parameters measured in the frequency range 0.24 to 60 GHz. Although 7μm of dielectric produces transmission line losses of 2.5dB/mm at 60 GHz a quality factor of 15 is achieved

Conclusion: A process for the realisation of low loss coplanar waveguide transmission lines on a CMOS grade silicon substrate where photoresist and polyimide are used as a spin on dielectric has been presented. 50 Ω characteristic impedance CPW lines with a ground to ground spacing of 110μm and a signal track width 70μm realised on a 15μm thick dielectric layer have losses less than 0.5dB/mm at 60 GHz. As spin-on photosensitive dielectrics are used, pattern transfer is simple and is easily extended to a multi-layer process. Using an electroplated gold process, interconnect can be made between the waveguide and substrate. Initial spiral inductors fabricated on a 7μm of dielectric with losses of 2.5dB/mm have Q factors of 15. Using the 15μm process described, higher quality factors are expected, in addition the electroplated interconnect process described will allow the fabrication of multi-level inductors and circuits.

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SINGLE STAGE AMPLIFIERS ON A CMOS GRADE SILICON SUBSTRATE USING A POLYMER INTERLAYER DIELECTRIC WITH STRAINED SILICON MOSFETs

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The design of single stage amplifiers based on a metal gate Si/SiGe MOSFET process on a 1 Ohm cm silicon substrate is presented. The amplifier design is based on 0.3 μm gate length MOSFETs with f_T of 19.9 GHz and f_{max} 21 GHz integrated with low loss coplanar waveguide transmission lines and high quality factor spiral inductors realised on a 15 μm thick polymer dielectric. The performance of the amplifier, currently in fabrication, will be presented.

1 Introduction

Recent interest in the realisation of CMOS-based circuits has resulted in great activity in silicon microwave research [1]. Leading the way, SiGe HBT BiCMOS RF mixers and low noise amplifiers are now commercially available [2]. To complement this technology, the implementation of devices having good microwave performance fabricated solely on a high yield silicon process is a very attractive prospect as it leads automatically to a lower mask count process with the

possibility of integrating RF functionality with complex baseband DSP capability. In the case of a standard silicon MOSFET process flow, useful RF performance can be achieved by (a) incorporating metal gates for optimal RF gain and noise performance. (b) producing low loss, high Q passive elements for transmission lines and lumped element matching. In this work, metal gate Si/SiGe MOSFET technologies, low loss transmission lines and high Q passive elements have been developed on 1-2 Ohm cm CMOS grade silicon substrates to enable the design of a single stage monolithic amplifiers.

2 Fabrication

2.1 Active Elements

The active element is a strained silicon channel n-Si/SiGe MOSFET with a metal T shaped gate. The Si/SiGe layer structure is grown on a 1 Ohm cm silicon substrate as shown in figure 1. The gate oxide is thermally grown at 750 °C to an oxide thickness of 4.5nm. Isolation is achieved by dry etching a mesa using SF6. Sputtered SiO_2 then lift off is used to planarise the sample. Ti/Pd/Au gates are patterned by e-beam lithography and lifted off. The source and drain self aligned implantation is carried out at 25keV with a P dose of 1 $x10^{15}cm^{-2}$ and is activated at 600°C for 20 seconds. The evaporated ohmic contacts are 100nm Ti / 50 nm Au annealed at 300°C for 3 mins. The devices are completed with evaporated bondpads of 400nm thick Au. A 2 μm thick layer of resist is put down under the bond pads to reduce capacitance.

6nm Si cap (unintentionally) doped
10nm $Si_{0.7}Ge_{0.3}$ supply, doped: $n=5x10^{18}cm^{-3}$
5nm Si spacer (unintentionally doped)
8nm Si channel (unintentionally doped)
100nm $Si_{0.7}Ge_{0.3}$ set back (unintentionally doped)
100nm $Si_{0.7}Ge_{0.3}$ set back, doped : $p=1x10^{17}cm^{-3}$
1um $Si_{0.7}Ge_{0.3}$ constant composition layer, doped :$p=1x10^{17}cm^{-3}$
Virtual substrate Ge grading : 0 –30%, doped :$p=5x10^{17}cm^{-3}$
p-type Si substrate 1 Ohm cm

Figure 1 - Layer structure of material used to fabricate strained silicon n-MOSFETs.

2.2 Passive Elements and Amplifier

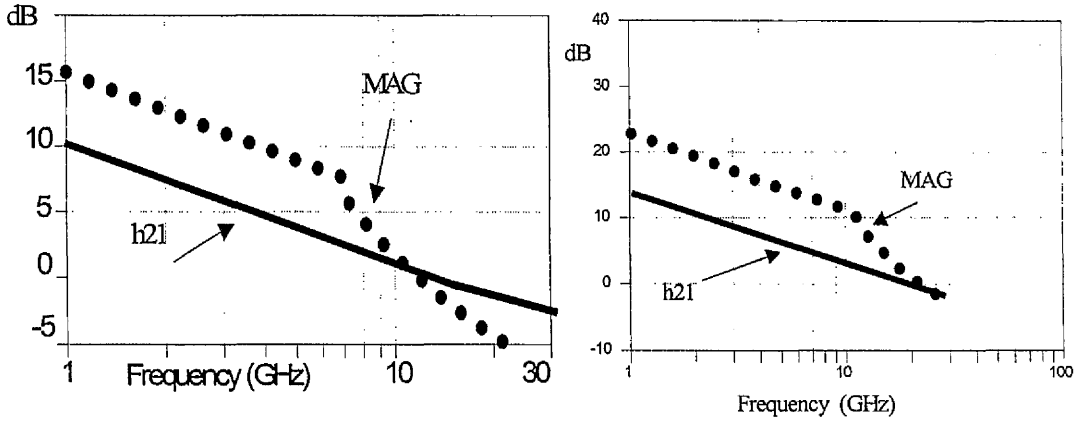
In order to separate the passive elements from the lossy silicon substrate a 15 μm thick spin on dielectric is used. The dielectric is spun onto the silicon substrate and is then cured so that it is resistant to further processing such as immersion in HF or acetone. The fabrication process is summarised below. Details of the fabrication of electroplated gold spiral inductors and transmission lines can be found in [3]. Interconnect down to a device on the substrate is easily achieved using standard photolithography and development. Devices are fabricated as above, then a 15 μm thick layer of photoresist is spun on and patterned with contact windows to the source, drain and gate pads. The photoresist (AZ4562) is spun at 4000 rpm for 30 seconds and post baked at 90°C for 20 minutes before a second layer is spun and baked with the same procedure, resulting in a 15 μm thick layer. The contact windows in the dielectric are patterned using standard photolithography. Following pattern transfer, the photoresist is cured at 180°C for 2 hours. The wafer is then blanket coated in 20 nm Ti / 5 nm Au by evaporation,

then a further 40 nm of sputtered Au. A single layer of S1818 photoresist is then spun and the contact windows defined. The top layer waveguides are patterned in this photoresist layer. Finally 2 μm of gold is electroplated, the resist is removed and the exposed evaporated Ti/Au gold is etched leaving electroplated gold transmission lines and passive elements with CPW interconnects to the devices on the substrate.

3 Results

3.1 Active Elements

Enhancement mode of operation . The contact resistance was measured to be 0.67 Ohm-mm with sheet resistance 190 Ohms/square using the TLM method. Devices were fabricated with gate lengths in the range 0.3 - 1 μm. The 0.3 μm gate length devices 100 um width biased at $V_g = V_{ds} = 1.5$ V have extrinsic transconductance of 230 mS/mm, and after de-embedding of the bondpad capacitance, an f_T of 19.9GHz and an f_{max} of 21.1GHz, as shown in figure 2(b). These devices are suitable for the realisation of test amplifier circuits up to around 6 GHz.

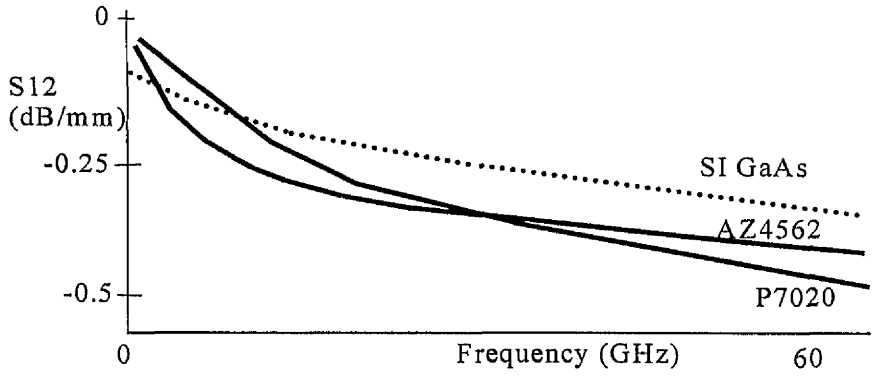


(a) (b)

Figure 2 - Cut off frequency f_T and f_{max} of a 0.3 μm gate length strained silicon MOSFET (a) As measured. (b) After de-embedding the probing pad capacitance.

3.2 Passive Elements

Coplanar waveguide transmission lines fabricated using the spin on dielectric on a 2 Ohm cm silicon substrate have transmission losses less than 0.6 dB/mm up to 60 GHz, as shown in figure 3. The waveguides are matched to 50 Ohms when 110



μm ground to ground spacing and 70 μm signal conductor width are used for both the polyimide and photoresist dielectrics. Table 1 shows the results for spiral inductors fabricated using the above process.

Figure 3 Insertion loss of 50 Ohm matched coplanar waveguide transmission lines on semi insulating GaAs and for a spin on dielectric (AZ4562 photoresist and P7020 Polyimide) on a 2 Ohm cm silicon substrate.

No of turns	L (nH)	Qmax	Freq(Qmax) (GHz)
1.5	0.63	16	10
2.5	1.2	12	5
3.5	2.3	10	3
4.5	3.6	8.5	2.5

Table 1. Measured performance of initial spiral inductors.

3.3 Single Stage Amplifier

Using the commercially available software package microwave office, single stage amplifiers were designed using the measured device results. Figure 4 (a) shows the schematic of the single stage amplifier - a simple topology was chosen based on the available passive library. For the 6.5 GHz design, Lg = 5.8 nH, Ls=1 nH, Ld=2.3 nH. For the 4 GHz design, Lg=10 nH, Ls=2.5 nH, Ld=9.5 nH. Figure 4(b) shows the magnitude of S21,S11 and S22 of the simulated amplifiers.

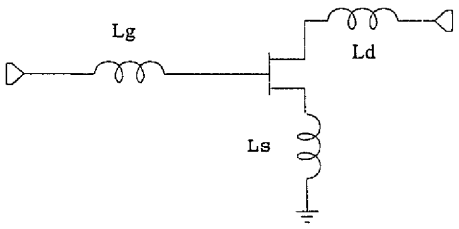


Figure 4 (a) Schematic of amplifier

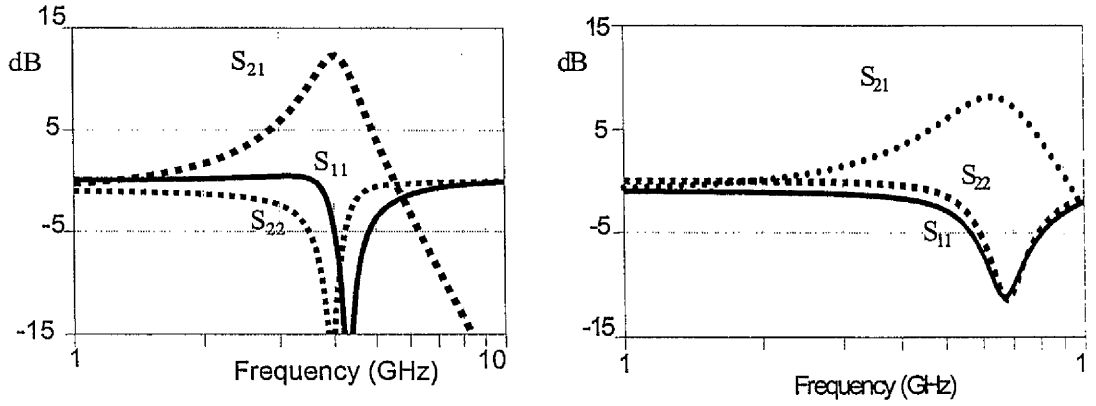


Figure 4(b) Modelled performance of a single stage amplifier matched 4GHz and at 6.5GHz

4 Conclusion

Strained silicon n-MOSFETs with metal gates have been fabricated. The devices show good RF performance having an f_T of 19.9 GHz and an f_{max} of 21.1 GHz for a 0.3μm x 100μm transistor. A spin on dielectric process was used to build a library of low loss transmission lines and passive elements with high Q on a standard silicon substrate. Single stage amplifiers were designed and are now in fabrication.

Acknowledgements

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