Electrons in Multiple Quantum Wires

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Submitted for the Degree of Doctor of Philosophy to
the Department of Physics and Astronomy at the
University of Glasgow

July 1992

ACKNOWLEDGEMENTS

I would like to thank my supervisor Dr. A.R.Long for his help and support throughout this project, particularly in the 'writing-up ' stage. I would also like to thank Dr. J.H.Davies for much useful advice on wire models, and Profs. S.P.Beaumont and C.D.Wilkinson for the use of the facilities in the Nanoelectronics Research Centre, in the Department of Electronic and Electrical Engineering, University of Glasgow.

Most of the time and effort put into this project was dedicated to sample fabrication (unfortunately!) and so there are many people whose help and advice in this area should be acknowledged. Thanks must be extended to Dr. D. McIntyre, D. Gourlay, H. Wallace and S. Capie for the excellent technical support readily available in the fabrication laboratories. The advice of fellow fabricators (or should that be sufferers?) was also greatly appreciated, with particular thanks to I.G. Thayne, Dr. M. Rahman, N. Cameron and A. Craig for their help and respective abilities for relieving the tedium of fabrication.

In the latter stages of the project, whilst using the dilution refrigerator, the technical support of R. Burns and the help and advice of E. Skuras (along with their good humour and tolerance) were also much appreciated.

Finally, last but not least, thanks to Mum, Dad, David, John, Martin, Andrew and Jane, without whose constant love and support none of this would have been possible.

SUMMARY

The research presented in this thesis is the result of an investigation into electrons, and their transport properties, in multiple quantum wires fabricated on GaAs/AlGaAs heterostructures. The aim of the project was to observe and quantify quantum electron confinement in the wires.

The introduction covers some relevant experimental ideas, and a review of the theory used for the analysis of the data presented in later chapters, including a discussion on Landau levels and edges states, and various models for the confinement of electrons in heterostructure wires. Chapters 2 and 3 are concerned with the experimental techniques employed, with Chapter 2 describing the fabrication techniques used to produce the multiple wire samples, covering electron beam lithography and etching, and Chapter 3 outlining the apparatus used for the measurement of sample characteristics at temperatures between room temperature and 50mK and at magnetic fields up to 12T.

Chapter 4 contains a detailed presentation and discussion of the capacitances between gate and channel, and the channel conductances of multiple wire and large area control samples (made without wires), both measured as a function of gate voltage. A model of a standard heterostructure incorporating DX centre trapping is presented, which accounts for the observed control sample characteristics and particularly the change of threshold voltage observed at around 150K. A model for heterostructure wires due to Davies was applied to data taken on the wire samples and these are shown consistently to conform to its predictions. The capacitance characteristics were used for a detailed investigation of charge distribution in the wire samples which indicated a spatial non-uniformity of the charge under the gate.

In Chapter 5 magnetocapacitance and magnetoresistance characteristics in the presence of a perpendicular magnetic field are presented and discussed. The main features of the data are the presence of focusing peaks in low field magnetoresistance and the fact that the carrier concentration was demonstrated to be independent of the gate voltage for the majority of samples, with only low mobility samples showing any signs of electron confinement in the magnetoresistance. A model proposed by Berggren et al for 1D confinement in heterostructure wires assuming a parabolic confinement potential in a perpendicular magnetic field was applied to the data from these samples and was shown to be only qualitatively valid, suggesting that the system could not be correctly described by such a potential. Strong magnetocapacitance signals were found for fractional quantum Hall states at high field.

In Chapter 6 the data presented in Chapters 4 and 5 is compared. The comparison of the carrier concentrations found using the methods outlined in Chapters 4 and 5 highlights the fact that the capacitance measurement was sensitive to more charge than magnetoresistance measurements. This excess charge was attributed to charge in shallow donors in the AlGaAs layer. In comparing the data presented in this thesis with other relevant published material, no obvious reason for the absence of confinement effects in the high mobility samples was found. Therefore, it is suggested that the charge found in the shallow donor distorted the confinement potential significantly reducing the chances of observing quantum effects.

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CHAPTER ONE

INTRODUCTION, THEORY AND REVIEW

1.1 INTRODUCTION

In recent years, much research has been conducted to investigate electron transport in semiconductor nanostructures. The aim of such investigations is to reduce the dimensions of devices to the extent that the length scales are commensurate with the electron Fermi wavelength and mean free path. In these limits the electron transport crosses the boundary between classical and quantum mechanical transport. The eventual goal is to fully understand and thereafter utilise these quantum effects, transforming the nature of modern electronics. Such a transformation is still a very long term goal, despite major technological advances.

The title of this project is "Electrons in multiple quantum wires". The general aim of the project was to investigate how electrons move under the influence of external electromagnetic fields in quantum wires, or quasi one dimensional electron channels. The research was intended to provide an insight into the physics of the material used and the electronic structure, if any, created as a result of 1D confinement in the wires. Such research has become possible as a result of the advent of the GaAs/AlGaAs heterostructure.

In this chapter an overview of current models and some experimental results will be given. The discussion will begin with a description of modulation doped GaAs/AlGaAs heterostructures and the nature of nanostructures fabricated on material of this type, followed by a detailed outline of the project aims. Thereafter, the nature of the measurements performed will be discussed with reference to both 2DEGs and nanostructures; this will cover conductance, magnetoconductance, capacitance, and magnetocapacitance. In the final sections a model proposed by Davies for wires will be reviewed and some relevant experimental work already published will be presented.

1.2 MODULATION DOPED GaAs/AlGaAs HETEROSTRUCTURES

GaAs/AlGaAs heterostructures are designed to produce a thin layer of highly mobile electrons by confining the electrons in a potential well at the GaAs/AlGaAs interface, in which motion perpendicular to the interface is quantised. This plane of electrons is commonly referred to as a two dimensional electron gas (2DEG). Using a 2DEG, only one further dimension of confinement is required to produce a quasi-one-dimensional system.

The 2DEG system has several desirable properties, two of the most important of these being a low electron density and a large electron mean free path. The low electron density, implying a large Fermi wavelength which is typically of the order of 40nm, and the large mean free path, which may exceed 10μm, mean that electron transport can be studied in small structures in the virtual absence of scattering events. Both of these features make the 2DEG an ideal system in which to study quantum electron transport.

The layer structure of a typical modulation doped GaAs/AlGaAs heterostructure is illustrated below in Figure 1.1.

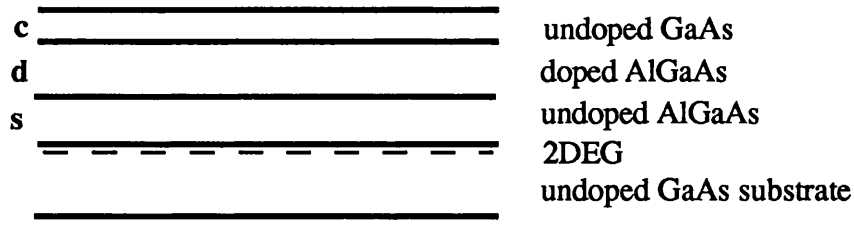


Figure 1.1 Layer structure for GaAs/AlGaAs heterostructures

The structure consists of four different layers of semiconductor. The first of these is the GaAs substrate. On top of this a layer of undoped AlGaAs is grown, then a Si doped AlGaAs layer and finally a thin layer of GaAs. The Al introduced into the GaAs crystal structure occupies random Ga sites, with the composition of the AlGaAs typically $Al_{0.3}Ga_{0.7}As$. AlGaAs and GaAs have nearly the same lattice spacing, which is advantageous as it avoids creating regions of stress and strain within the the crystalline structure of the material. The undoped AlGaAs layer is present to separate the doped layer from the 2DEG, as this has been shown to reduce scattering and enhance electron mobility. The corresponding band diagram is shown in Figure 1.2, where E_f is the Fermi level and E_c is the conduction band edge.

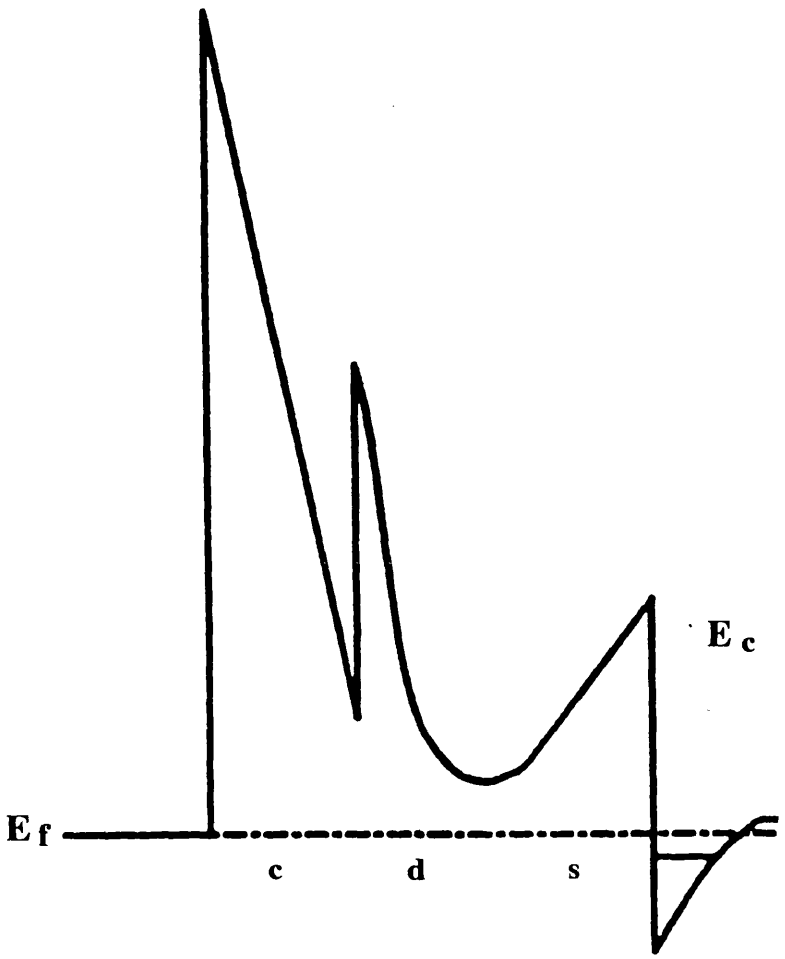


Figure 1.2 Band diagram of a GaAs/AlGaAs heterostructure.

Electrons are confined to the GaAs/AlGaAs interface by a potential well formed by the combined effect of the conduction band offset, which is about 0.23V, between the GaAs and the AlGaAs and the attractive electrostatic potential due to the positively charged ionised donors in the n-doped AlGaAs layer. Two dimensional sub-bands are formed as a result of confinement perpendicular to the interface and free motion along the interface. The density of states for electrons in a 2DEG is illustrated in Figure 1.3.

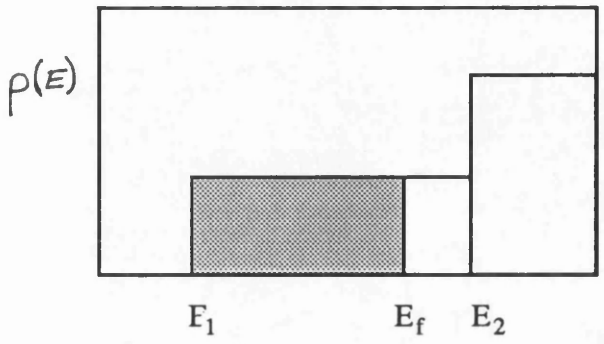


Figure 1.3 Density of states for a 2DEG with only 1 sub-band occupied

States below the Fermi level are occupied - usually only one sub-band is occupied.

The energy of conduction electrons in a single sub-band of an unbounded 2DEG, E(k), is given by,

$$E(k) = \frac{h^2 k^2}{8\pi^2 m^*} \qquad (1.1)$$

where E is measured relative to the bottom of the sub-band, h is Planck's constant, k is the electron wavevector, and m* is the electron effective mass ($m^*=0.067m_e$).

There have been many papers published on the GaAs/AlGaAs heterostructure, and a few of the more instructive are listed here for reference (N.B. the full references for this, and susequent chapters, are given at the end of each chapter): Stormer et al, 1981, discuss the effects of varying the Al concentration; Lee et al, 1983, derive a simple analytical expression for the low field electron mobility in the 2-DEG; Kunzel et al, 1983, discuss persistent photoconductivity in Si doped GaAs/AlGaAs heterostructures; Schubert et al, 1984, discuss the effects of parallel conductance; Schubert and Ploog 1985, present an analytical method for calculating the electron sub-band structure; Smith et al, 1988, discuss the effects of two sub-band transport and Mooney, 1991, discusses the effects of DX centre trapping in the Si doped AlGaAs layer.

1.3 NANOSTRUCTURES ON GaAs/AlGaAs HETEROSTRUCURES

In this section the techniques employed in the fabrication of nanostructures and the nature of the electron confinement in such systems will be discussed.

1.3.1 TECHNIQUES EMPLOYED FOR THE FABRICATION OF NANOSTRUCTURES ON GaAs/AlGaAs HETEROSTRUCTURES.

Several methods are employed to fabricate nanostructures in GaAs/AlGaAs heterostructures. The first of these methods uses etching techniques to confine the electrons physically, producing what will be referred to as etched wires. The second method confines electrons electrostatically by means of split gate contacts at the surface of the material - this was the technique employed for the fabrication of multiple wires in this project. Several groups investigating multiple parallel wire samples used etching techniques, so both methods of confinement will be discussed.

(a) Narrow etched wires

Semiconductor etching techniques are widely used to define patterns. For the fabrication of small features it is usually necessary to use dry etching techniques, which will be discussed briefly in Chapter 2, Section 2.4.2.

The standard method for the fabrication of etched nanostructures is to mask the required areas with an etch resistant material and remove, under suitable and controlled conditions, the exposed material. The remaining features have the profile illustrated in Figure 1.4.

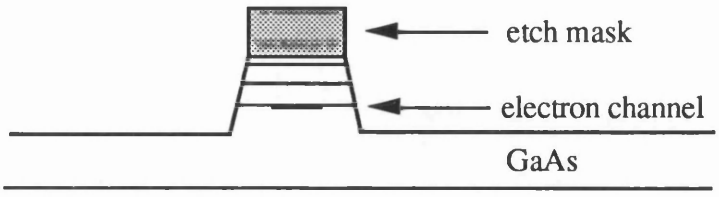


Figure 1.4 Profile of a deep etched wire fabricated on a GaAs/AlGaAs heterostructure.

This shows a structure in which an electron channel is defined physically. This type of feature is often referred to as a deep etched channel, as the exposed material is removed to a level below that of the 2DEG. In some materials, such as n^+ GaAs, it is essential that the etch is taken below the level of the conducting electrons. However, in GaAs/AlGaAs structures this is not always necessary because the etch process induces

damage at the surface of the exposed material thereby upsetting the conditions creating the 2DEG. If the surface damage is severe enough then the etch induced damage itself is sufficient to deplete electrons from the unmasked regions before the etch reaches the 2DEG level. This type of wire will be referred to as a shallow etched wire and is illustrated in Figure 1.5.

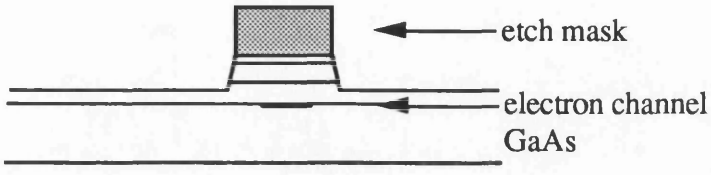


Figure 1.5 Profile of a shallow etched wire fabricated on a GaAa/AlGaAs heterostructure.

The absolute thickness of the layer removed by the etch is a function of both the material and the fabrication techniques employed.

(b) Split gate wires

Split gate depletion was the technique employed for the fabrication of the nanostructures in this project. This technique was developed by Thornton et al, 1986, and Zheng et al, 1986. The structure used is shown in Figure 1.6.

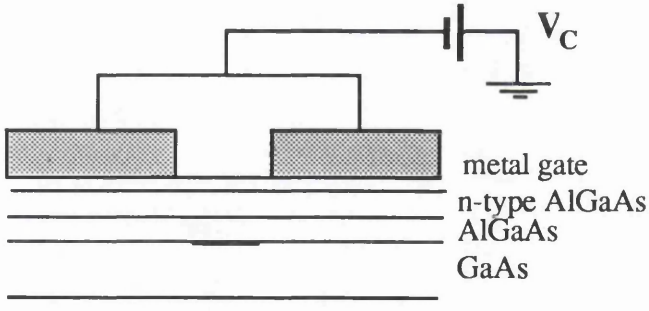


Figure 1.6 A split gate wire formed on a GaAs/AlGaAs heterostructure.

By applying a negative bias V_c (the 2DEG cut-off voltage) to the gate, electrons can be depleted from the regions below the gates leaving only electrons in the channel between the gates. By making the gate bias increasingly more negative the channel itself can be depleted, or pinched-off.

The split gate technique has several advantages over the etching methods. The first, and most important, is that the number of electrons and the channel width can be controlled by varying the gate bias. The second is that, by avoiding the damage inducing process produced by the etching techniques, the wires formed by split gate depletion are fabricated in a 'cleaner' system (by 'cleaner' what is meant is that the

material is not significantly damaged or distorted by the fabrication process). Therefore, split gate wires should be less prone to undesirable carrier trapping effects. In this type of system, boundary roughness is also much less than in etched systems, reducing the probability of diffuse boundary scattering. The magnitude of the voltages required to form wires, and thereafter deplete the channels, will be discussed in Section 1.6.

1.3.2 ENERGY LEVEL SEPARATION AND DENSITY OF STATES IN QUASI-ONE DIMENSIONAL SYSTEMS.

The additional lateral confinement imposed on a 2DEG in the fabrication of narrow wires results in the formation of discrete 1D energy levels. To estimate the energy level separation and density of states in quasi-1D wires it is necessary to solve self-consistently the Schrodinger and Poisson equations. However, this is complex, so as a first order approximation electrons in wires are often modelled as being single particles in a 'box', so it is necessary only to solve the Schrodinger equation. There are two descriptions commonly used for the confinement potential for the electron-in-a-box problem, these being the square well and the parabolic potentials which are illustrated below in Figure 1.7 (a) and (b) respectively.

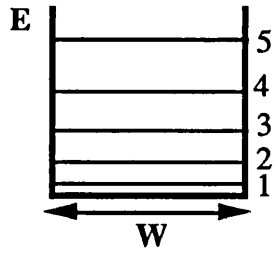


Figure 1.7(a) Square confinement potential

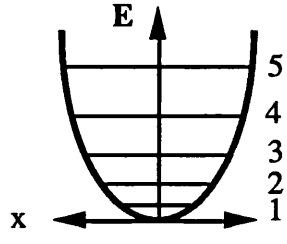


Figure 1.7(b) Parabolic confinement potential

The separation of the energy levels for the square well potential are given by,

$$E_n = \frac{(nh)^2}{2m^* W^2} \qquad (1.2)$$

where W is the width of the wire.

The parabolic potential can be described by,

$$V(x) = \tfrac{1}{2} m^* \omega_0^{\,2} x^2 \qquad (1.3)$$

where ω_o is the characteristic frequency.

The separation of the energy levels for the parabolic potential are given by,

$$E_n = (n - \tfrac{1}{2})\frac{h\omega_0}{2\pi} \qquad (1.4)$$

This is the standard solution for the simple harmonic oscillator problem.

The density of states for a quasi-1D wire with four 1D sub-bands occupied is shown below,

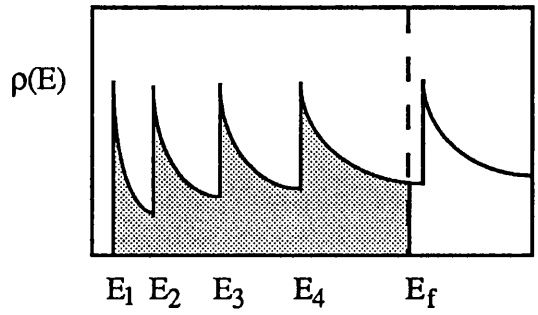


Figure 1.8 Density of states for a quasi 1-D wire, with four 1-D sub-bands occupied.

States below the Fermi level are occupied, i.e., the shaded region in Figure 1.8.

1.4 NANOSTRUCTURES USED, AND AIMS OF PROJECT

As indicated by the title of the project, the research conducted was concerned with electrons, and the transport of these electrons, in multiple wire samples fabricated on GaAs/AlGaAs heterostructures. In this section the sample structure used and the specific aims of the project will be discussed.

1.4.1 MULTIPLE PARALLEL WIRES - SAMPLE STRUCTURE

As noted earlier, the wires were formed using the split gate technique. To produce many of these wires in parallel, multiple split gates were fabricated by depositing a continuous gate over many, typically several hundred, strips of insulating resist. This method was initially developed by Ford et al, 1988. A cross section through a gate of this type gives the profile illustrated in Figure 1.9.

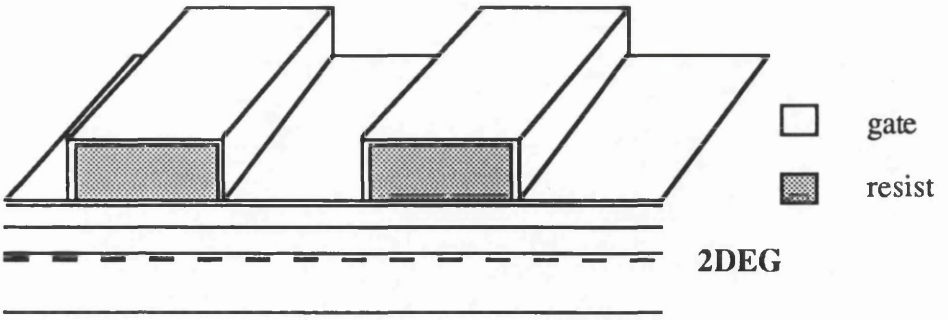
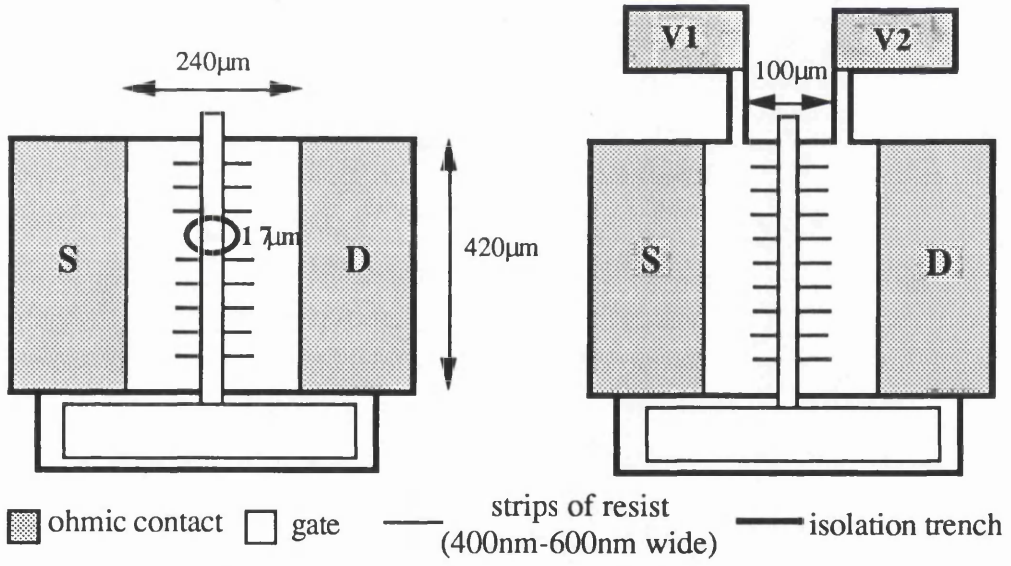


Figure 1.9 Method employed to produce multiple parallel 'split gate' wires

By applying a suitably negative bias to the gate, electrons in the regions below the gate which are in direct contact with the material are repelled until the regions are fully depleted, thus creating channels of electrons in the regions below the resist. The regions directly underneath the resist strips are not depleted by the gate bias as the resist significantly reduces the depleting potential. This results in the formation of multiple parallel wires. By making the gate bias increasingly negative the channels can also be depleted of electrons. The voltage at which this happens will be referred to as the threshold, or cut-off, voltage.

The basic sample design is shown below in Figure 1.10(a). This was later modified to include voltage probes, illustrated in Figure 1.10(b).



(a) sample design used for initial measurements of capacitance and two terminal conductance

(b) sample design used for four terminal conductance measurements

Figure 1.10 Sample design

Specific sample dimensions, wire widths and gate lengths, will be given with the data in Chapter 4.

1.4.2 AIMS OF THE PROJECT

The general aims of this project were to investigate and understand electron transport in multiple parallel wires. It was hoped that it would be possible to use capacitance and conductance techniques to probe 1D sub-bands created by the quantum confinement of electrons in the wires. The sample design allowed both the capacitance and conductance to be measured, with the gate dimensions chosen specifically to satisfy the requirements of the capacitance measurements.

Multiple wire samples were favoured over single wires because the latter are susceptible to quantum interference effects which tend to smear out sub-band effects. However, for multiple wire samples quantum noise effects are averaged out making it, in principle, easier to see quantum effects in the conductance and capacitance. This is of course assuming that the wires are sufficiently uniform, as any variation in the wire widths would also smear out quantum effects. Magnetoconductance and magnetocapacitance measurements were also planned to give further information on quantum structure, if any, and another measure of the number of electrons involved in the transport.

Many experiments on both multiple and single wire samples have been successfully performed to investigate the effects of electron confinement. However few groups have measured both the capacitance and the conductance of wires. Previous capacitance measurements by Smith el al 1987 exhibited 1D confinement in multiple wire samples, but due to the structure which was effectively a parallel plate capacitor, no information on the in-plane sample conductance could be gained. Conductance measurements were carried out by Ismail et al 1989 on a sample similar to those used in the course of this project in which the effects of 1D confinement were seen, but no capacitance measurements were taken. Berggren et al 1986 made the first measurements of the magnetoconductance of a split gate wire. Kotthaus et al 1989 measured the capacitance, magnetoconductance and infrared spectra of similar samples. Each of these experiments was very successful in measuring, and in some cases quantifying sub-band effects. However, the sample structures used limited the number and type of measurements possible.

It was hoped that the samples used in the course of this project would allow a fully comprehensive, and unifying, set of experiments to be performed, with the possibility of measuring sub-band effects on the same sample using four different techniques. The four key measurements are those of conductance,

magnetoconductance, capacitance and magnetocapacitance. These measurements, on multiple parallel wires, form the basis for this thesis.

1.5 REVIEW OF MEASUREMENTS

In this section the four types of measurement conducted will be discussed, these being conductance, magnetoconductance, capacitance and magnetocapacitance. Each of these measurements will be discussed with respect to an unrestricted 2DEG and a quasi-1D system.

1.5.1 CONDUCTANCE OF A 2DEG

The conductance, G, of a 2DEG can be expressed in the usual form,

$$G = \frac{W\sigma}{L} \tag{1.5}$$

where W is the width of the 2DEG, L is the length of the conducting channel in the direction of the current and σ is the 2D sample conductivity. The conductivity of a sample can be estimated from a simple classical approach. The standard Drude expression for the conductivity of a 2DEG sample can be expressed as,

$$\sigma = g_s g_v \frac{e^2}{h} \frac{k_f l}{2} \tag{1.6}$$

where g_v is the valley degeneracy (=1), g_s is the spin degeneracy (=2), e is the electronic charge, k_f is the wave vector for electrons at the Fermi surface, h is Planck's constant and l is the electron mean free path. For a more detailed discussion of this see Beenaker and Van Houten, 1990.

From the conductance, it is possible to estimate the mobility of the electrons in a given sample using,

$$G = \frac{W}{L} e n_{2d} \mu_e \tag{1.7}$$

where μ_e is the electron mobility.

1.5.2 CONDUCTANCE OF NANOSTRUCTURES

The two terminal conductance of nanostructures is best described by the Landauer formula, so called because of the pioneering work conducted by Landauer in 1957, (see Landauer, 1957) which is given below,

$$G = \frac{e^2}{h} \sum_{i,j}^{N_c} T_{ij} \equiv \frac{e^2}{h} T \tag{1.8}$$

where N_c is the number of propagating channels in the sample, T_{ij} is the transmission probability from the jth momentum channel to the ith momentum channel, and T is the total transmission probability, normalised to N_c. This describes the conductance in terms of the electron transmission probability through a constriction and the fundamental unit of conductance e^2/h. This formula was developed from a model of a two terminal diffusion current flowing from one electron reservoir at $E_f+\delta\mu$ through a constriction to another reservoir at a slighty different chemical potential E_f, see Figure 1.11.

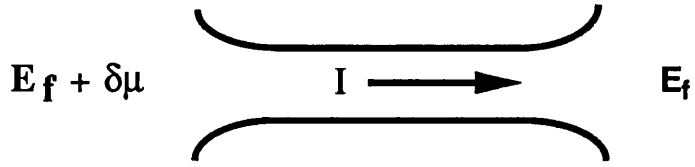


Figure 1.11 Two electron reservoirs connected by a narrow constriction

The E/k plot is given in Figure 1.12,

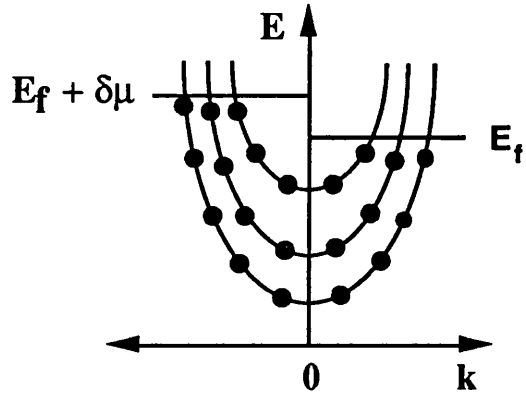


Figure 1.12 E/k plot for system illustrated in figure 1.11

The main assumptions of the model are that $\delta\mu$ is small and only electrons near the Fermi energy contribute to the overall conductance.

The Landauer formula has been shown to provide a good description of the conductance measured in nanostructures, and can be applied equally to macroscopic samples in the presence of a magnetic field. This two terminal description can be extended to the situation where multi-reservoir measurements are used, giving the current as,

$$I_m = \sum_n^{N_L} g_{mn} V_n = \frac{e^2}{h} \sum_n^{N_L} (T_{mn} - N_c \delta_{mn}) V_n \qquad (1.9)$$

where I_m is the total current into lead m and V_n is the voltage applied to lead n, g are conductance coefficients, N_L is the number of reservoirs, and T_{mn} is the total

transmission probability (or reflection coefficient for the case m=n) at the Fermi energy for electrons injected at lead n to be collected at lead m (summed over all channel indices, which have been supressed for clarity). It can be seen that for N_L=2, this reduces to equation 1.8. This expression is known as the Landauer-Buttiker formula, as Buttiker, 1986, generalised the initial two terminal expression proposed by Landauer. Again for a more thorough description of the edge state model see Beenaker and Van Houten, 1990.

The nature of the transport of electrons through the constriction determines the transmission probability. There are three types of transport to be considered - diffusive, ballistic and quasi-ballistic. Each of these is dominant in different limits.

To discuss the nature of the motion of electrons it is necessary to introduce two important length scales. The first of these lengths is the mean free path of the electron, l, which is the mean free path length between scattering events at impurity sites. The second is the phase coherence length l_ϕ, which is the length over which the phase of the electron wave is preserved. It is these lengths which, relative to the sample dimensions, determine the nature of electron transport.

(a) Diffusive transport

This occurs in the limit in which the electron mean free path length and the phase coherence length are both less than the width, W, and length, L, of the sample. The motion of the electron is then dominated by a series of impurity scattering events as shown in Figure 1.13.

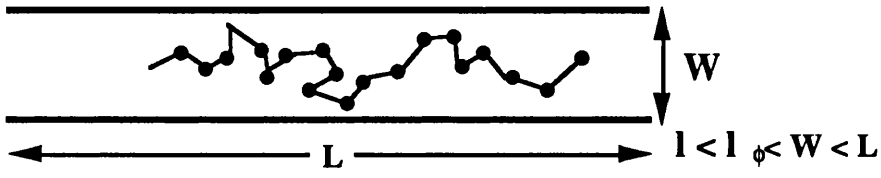


Figure 1.13 Motion of an electron travelling in the diffusive limit

In this instance the conductance of the sample can be described using a classical free electron approach as outlined in the previous section.

Diffusive transport is dominant at high temperatures and in samples with low mean free electron path lengths. Heavily doped n-type GaAs wires formed using dry etching techniques exhibit transport in the purely diffusive regime.

(b) Ballistic transport

Ballistic transport is dominant when the sample dimensions are less than both the electron mean free path and the phase coherence length. In this limit the motion of electrons through the sample is determined by boundary scattering. There are two types of boundary scattering possible - diffusive scattering, in which the scattering boundary is 'rough' and the wave scattering angle is not preserved, and specular scattering, in which the wave amplitude, scattering angle and phase of the scattered electron wave are preserved. In ballistic transport, specular boundary scattering is the dominant process, see Figure 1.14.

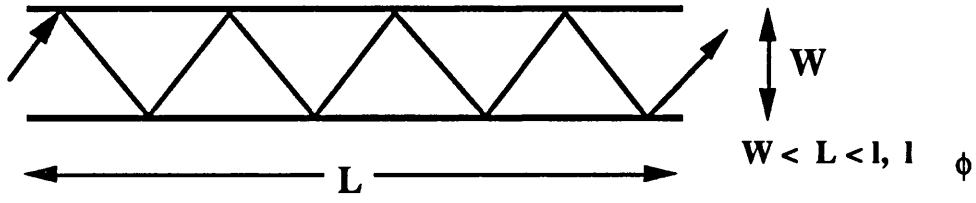


Figure 1.14 Ballistic transport - in this limit transport is dominated by specular boundary scattering.

This process is dominant when the confining potential is uniform along the length of the wire.

The boundary scattering mechanism prevalent in wires formed using the split gate technique is usually specular in nature.

In the purely ballistic regime the transmission probability of the Landauer formula is equal to 1, and the measured conductance is quantised in units of $2e^2/h$, which includes explicitly the effects of two fold spin degeneracy. This has been seen in the conductance of so called quantum point contacts, first measured by Van Wees et al, 1988, and Wharam et al, 1988.

(c) Quasi-ballistic transport

Diffusive and ballistic transports are extreme situations. The intermediate state is quasi-ballistic. This is essentially a combination of the other two, and occurs where the sample dimensions are of the same order as the mean free path length. In this limit the transport is effected equally by impurity scattering events and boundary scattering, see Figure 1.15.

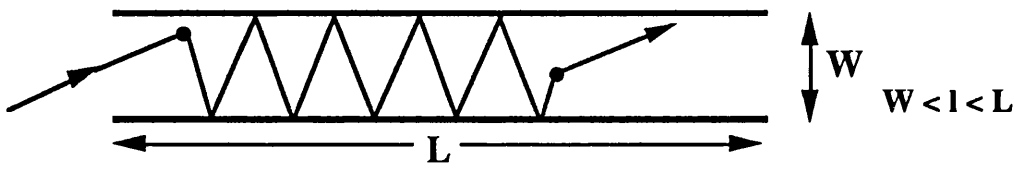


Figure 1.15 Quasi-ballistic transport - affected by both impurity scattering and boundary scattering

1.5.3 MAGNETOCONDUCTANCE OF 2DEGS

This section will begin with an outline of the effects of a perpendicular magnetic field on the density of states in a 2DEG, that is, the formation of Landau levels, and will progress to a discussion of how these Landau levels are manifest in real measurements of magnetoresistance/conductance.

(a) Formation of Landau levels in a perpendicular magnetic field

If a magnetic field is applied perpendicular to the plane of a 2DEG, the electrons experience an additional force added to the driving potential along the plane of the 2DEG. The force is the Lorentz force given by,

$$\underline{F} = e\underline{V} \times \underline{B} \tag{1.10}$$

where $\underline{V}$ is the velocity of the electrons and $\underline{B}$ is the magnetic field. For $\underline{B}=(0,0,B_z)$. and $\underline{V}=(v_x,0,0)$ then

$$F = ev_x B_z \tag{1.11}$$

This additional force causes the electrons to orbit a centre point of motion. Thus the electrons drift with a velocity $|v_x|$ but circle the drift centre.

From Equation 1.1 the energy of electrons in an unbounded 2DEG is given by,

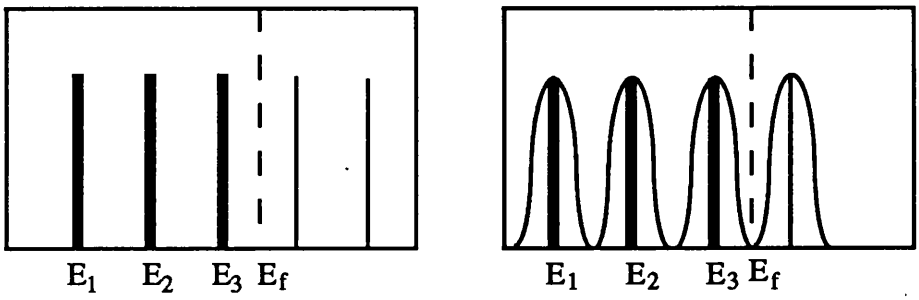
$$E(k) = \frac{h^2 k^2}{8\pi^2 m^*} \tag{1.12}$$

In the presence of a magnetic field applied perpendicular to the plane of the 2DEG, the energy spectrum becomes fully discrete since the electrons are subject not only to the translational force due the applied electric field, but also to the restrictive Lorentz force due to the magnetic field. This leads to the quantisation of the circular cyclotron motion. Assuming that only one of the 2DEG sub-bands is occupied then the total energy of an electron in the nth 1D Landau level can be given by E_n, where

$$E_n = \tfrac{1}{2\pi}(n - \tfrac{1}{2})h\omega_c \tag{1.13}$$

where $\omega_c=eB/m^*$ and is known as the cyclotron frequency. The quantum number, n= 1, 2, 3...., is known as the Landau index. This is the solution for the simple harmonic oscillator, in which the confining potential is parabolic.

The density of states of an unbounded 2DEG in the presence of a magnetic field is shown in Figure 1.16 (a).



(a) Idealised density of states in a 2DEG in the presence of a perpendicular magnetic field

(b) Realistic density of states in a 2DEG in the presence of a perpendicular magnetic field

Figure 1.16 Density of states in a 2DEG in the presence of a perpendicular magnetic field - states up to the Fermi energy are occupied

States below the Fermi level, E_f, are occupied, with the number of states in each Landau level the same. This shows the idealised situation. In reality the density of states is unlikely to ever be fully zero in the energy gap between levels, as localised impurity states broaden and smear the Landau levels, giving the more realistic density of states shown in Figure 1.16(b). It should be noted at this stage that these equations do not take into account the effects of spin degeneracy, for which the number of Landau levels is doubled.

(b) Measurement of magnetoresistance/conductance

Three resistances are commonly measured - the 2 terminal resistance R_{2t}, the longitudinal resistance R_l and the transverse, or Hall, resistance R_H. These resistances are defined as,

$$R_{2t} = \frac{V_{2t}}{I}, \quad R_L = \frac{V_L}{I}, \quad R_H = \frac{V_H}{I} \qquad (1.14)$$

where I is the applied current and V_{2t}, V_L and V_H are defined in Figure 1.17.

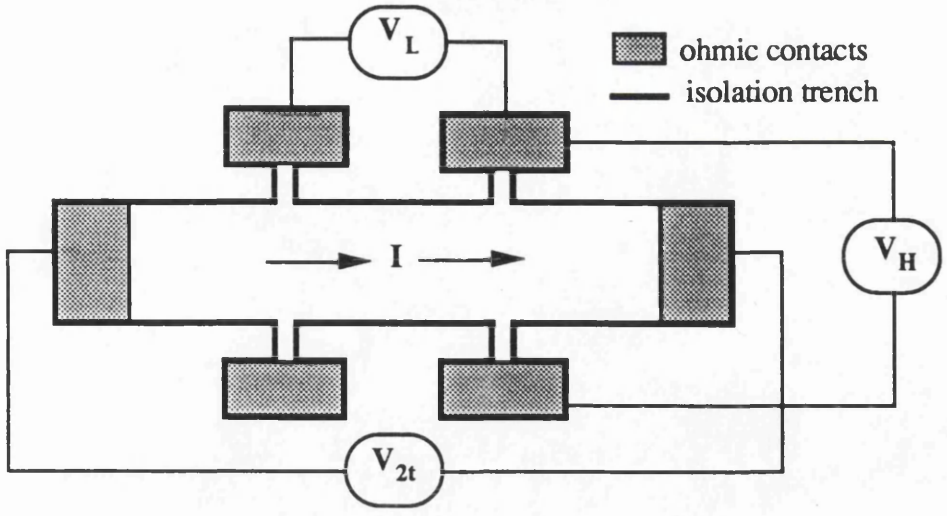


Figure 1.17 Hall bar

Each of these resistances, when measured in the presence of a perpendicular magnetic field, display fundamental effects. The measurement of the two terminal resistance of a 2DEG sample at low T displays quantised steps in the conductance at e^2/h, the measurement of the longitudinal resistance of an unrestricted 2DEG in the presence of a perpendicular magnetic field gives rise to well defined oscillations in R_L, which are known as Shubnikov-de Haas oscillations, and the measurement of the transverse resistance, under the same conditions, displays the quantum Hall effect, which like the two terminal resitance is quantised in units of e^2/h. These three effects can be explained in terms of edge states.

Edge states originate from Landau levels, which, within the bulk of the material, lie below the Fermi energy but rise in energy approaching the sample boundary. The point of intersection of the n-th Landau level with the Fermi level forms the site for the edge states belonging to the n-th edge channel shown in Figure 1.18.

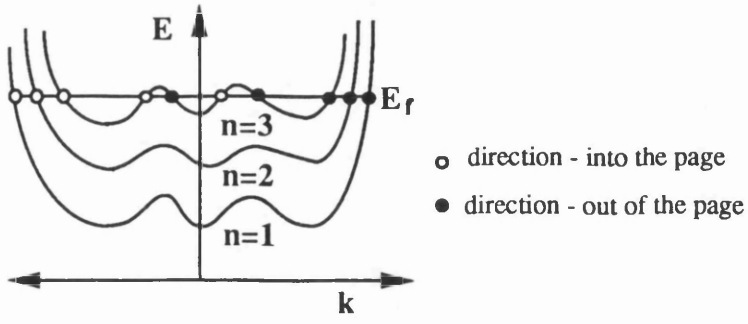


Figure 1.18 E/k plot illustrating the formation of edge states.

The number of edge channels at E_f is equal to the number of Landau levels below E_f. Within each of these channels electrons travel parallel to the edges of the sample. In Figure 1.18 the effect of localised states in the bulk of the material is also illustrated. These states carry current but do not contribute to the conductance of the sample. The 'physical' picture of a sample in which current is carried in both localised and edge states is illustrated in Figure 1.19.

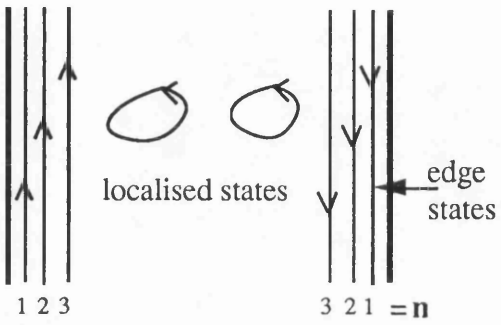


Figure 1.19 Electrons in edge states travel parallel to sample edges.

A description of the quantum Hall effect based on extended edge states and localised bulk states was first proposed by Halperin, 1982. The edge state model was based on the assumption that a local equilibrium was established at the edges of the sample. In the presence of a perpendicular magnetic field, edge states are formed and the net sample current is carried in channels at the edges of the sample. Consider Figure 1.20.

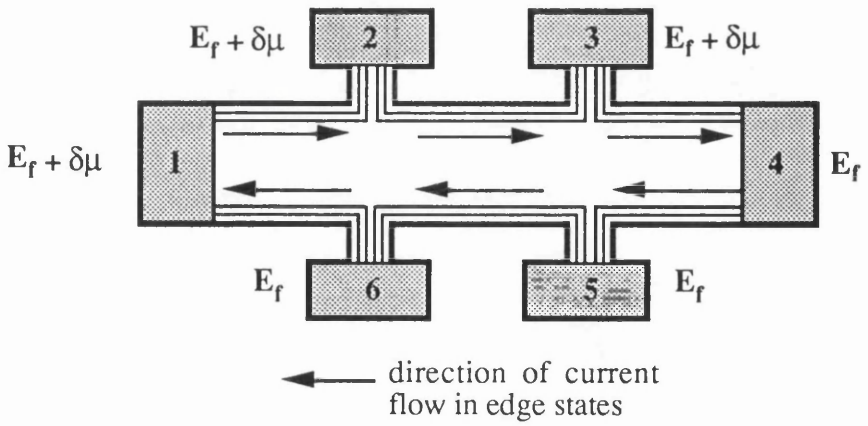


Figure 1.20 Hall bar carrying current in edge states

From the Landauer-Buttiker formula, in the presence of a chemical potential difference of $\delta\mu$ between contacts 1 and 4, the edges of the sample are at different potentials, again with the difference being $\delta\mu$, with each channel carrying a current $(e/h)\delta\mu$ and so

contributing e^2/h to the conductance. For both the 2 terminal resistance and the Hall resistance, the potential difference between the measuring contacts is $\delta\mu$, and so the conductance is given by, $G_{2t}=G_H=e^2/h$ for each channel. Examples of both of these effects are given in Graph 1.1, for a 2-terminal magnetoresistance measurement and Graph 1.2 for a standard Hall resistance measurement, where both of these display the effects of spin splitting of the Landau levels. For the longitudinal resistance this model implies that the adjacent contacts used for this measurement are at the same potential and so the measured resistance, when all the edge states are full, is 0, as shown in Graph 1.3, which again shows the effects of spin splitting.

The edge state model has been shown to be the most physically unifying proposed. However, it should be noted that the Hall plateaus, and zeros in the longitudinal resistance, are not solely due to the formation of edge channels, but are equally dependent on the existence of localised states in the bulk of the 2DEG, since the Fermi level is typically pinned at the mid-point of the Landau levels and resides in the region where only edge channels exist , very briefly, at the centre of the Hall plateau. For a detailed discussion of this point see Stone et al, 1990.

The standard expression for the Hall resistance is,

$$R_H = \frac{h}{e^2 N} \qquad (1.15)$$

where N=1,2,3..... is the number of the spin split Landau levels.

The separation, in 1/B, of the minima or, in the ideal case, the zeros of the Shubnikov-de Haas oscillations can be shown to be,

$$\Delta\left(\frac{1}{B}\right) = \frac{h}{e}\frac{g_s g_v}{n_{2d}} \qquad (1.16)$$

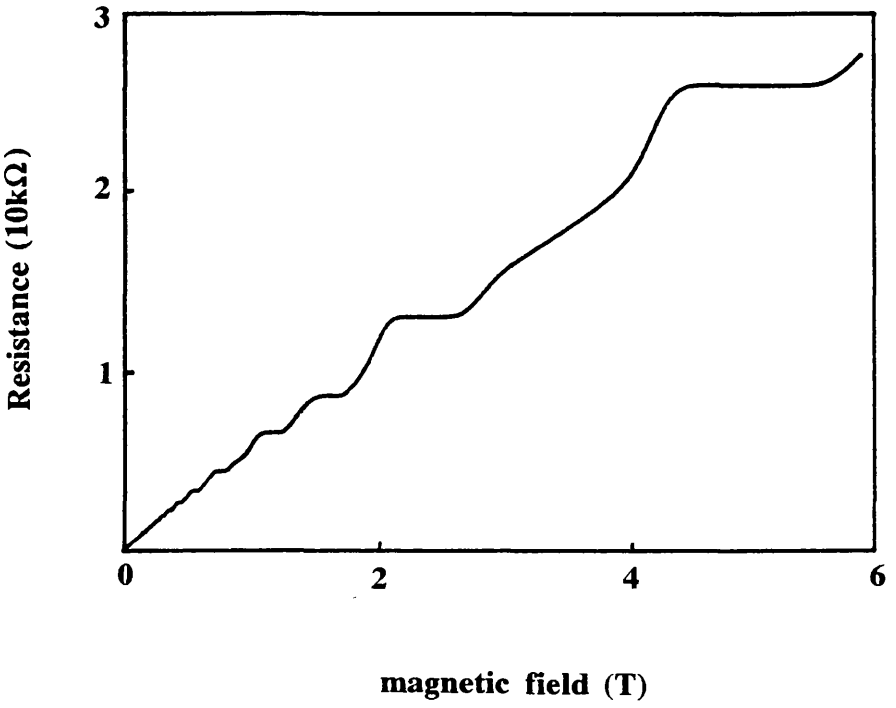
where g_S (=2) is the spin degeneracy factor and g_V (=1) is the valley degeneracy factor. In this instance the factor g_S accounts for the spin degeneracy.

1.5.4 MAGNETOTRANSPORT OF NANOSTRUCTURES

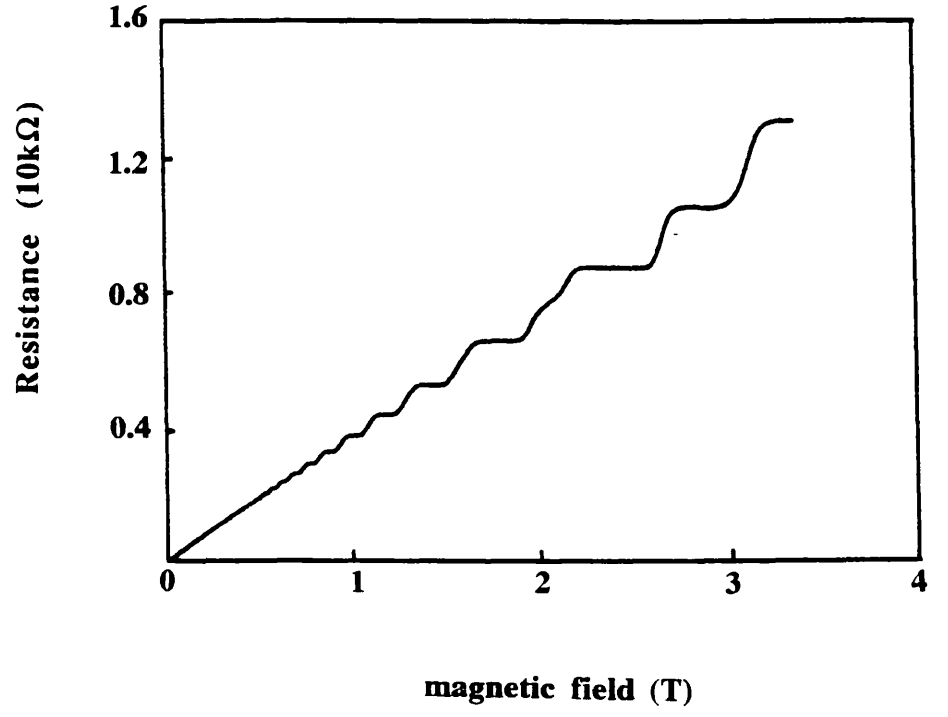
For clarity this discussion will be divided into two sub-sections, $W>d_c$, and, $W<d_c$, where d_c is the cyclotron diameter and W is the width of the constriction. Again the discussions will be on a qualitative level.

(a) $W>d_c$ - 'High B' transport

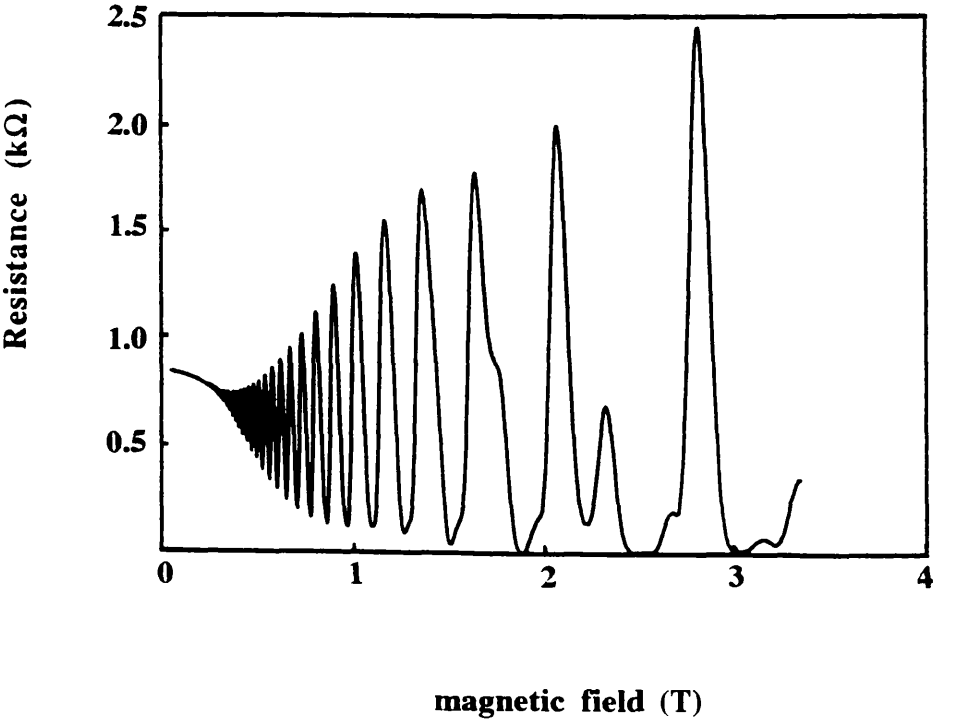
In this limit electrons can either travel in edge states, interacting with only one of the sample boundaries, or in cyclotron orbits, in the bulk of the wire away from the boundaries. Therefore, standard Shubnikov-de Haas oscillations are observed, with the positions of the minima displaying the 1/B vs n (Landau index) linearity, see Equation 1.16.



Graph 1.1: 2-terminal resistance of an unpatterned 2DEG.



Graph 1.2: Hall resitance of an unpatterned 2DEG.



Graph 1.3: Shubnikov-de Haas oscillations of an unpatterned 2DEG.

(b) $W<d_c$ - 'Low B' transport

In this limit two effects may be observed. The first of these is the suppression of backscattering (observed experimentally as a negative magnetoresistance), which can arise from three different effects - diffuse boundary scattering, specular boundary scattering and weak localisation. The second is the deviation from the 1/B vs n linearity for the positions of the Shubnikov-de Haas minima which can be attributed to the formation of 1D magneto-electric sub-bands.

(1) negative magnetoresistance - suppression of backscattering

Diffuse boundary scattering arises when the confining potential forming the wire, or nanostructure, varies along the length of the wire. This uneven potential increases the probability of diffuse scattering events at the wire walls, possibly resulting in backscattering, see Figure 1.21(a).

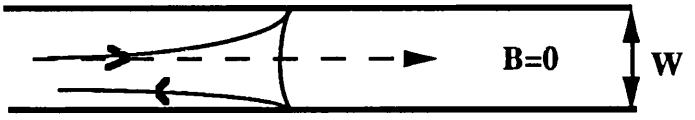


Figure 1.21(a) Diagram showing how electrons in weak magnetic fields can reverse direction as a result of diffuse boundary scattering, thus increasing the resistance

If a magnetic field is applied perpendicular to this system then, at fields at which the cyclotron radius is less than the wire width, backscattering may be suppressed, as illustrated in Figure 1.21(b).

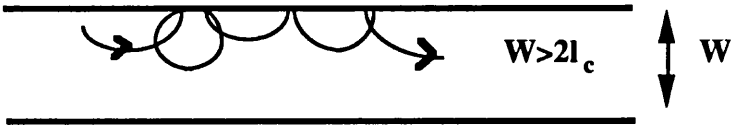


Figure 1.21(b) Illustration of how strong magnetic fields can suppress backscattering and hence reduce resistance

This results in a decrease in the resistance as more electrons pass through the wire to contribute to the conductance. Hence the application of a magnetic field to a nanostructure in which diffuse boundary scattering plays a significant role results in the suppression of backscattering and negative magnetoresistance.

Specular boundary scattering : In systems in which the boundary scattering process is purely specular negative magnetoresistance can still be seen. This may be due to impurity scattering near the wire walls - see Figure 1.22(a).

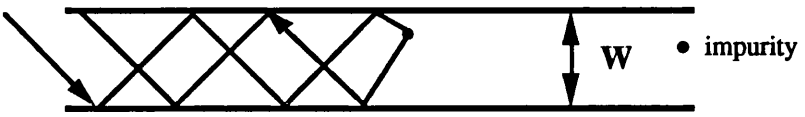


Figure 1.22(a) Illustration of how an isolated impurity may cause backscattering in the case of specular boundary scattering

If a magnetic field is applied perpendicular to the plane of the electrons then backscattering may be suppressed when the cyclotron radius becomes smaller than the separation of impurity ion sites. The mechanism for this suppression is identical to that for diffuse boundary scattering and is shown in Figure 1.22(b).

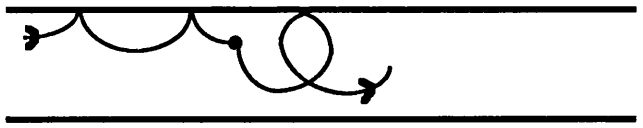


Figure 1.22(b) Suppression of backscattering in case of specular boundary scattering

Weak localisation : Both specular and boundary scattering are classical size effects. However, weak localisation is a considerably more complex result which is attributed to the enhanced probability of coherent backscattering events arising from quantum interference effects. In the presence of a magnetic field this enhanced probability is reduced resulting in a negative magnetoresistance. For a full review of this see Andersen et al, 1979, Gorkov et al, 1979, Bergmann, 1983, and Beenaker and Van Houten, 1990.

(2) 1-d effects in nanostructures

When the cyclotron diameter is greater than the width of the constriction, the electron waves in the constriction can interact with both of the boundaries, which results in the formation of magneto-electric sub-bands. After Van Houten et al, 1987, the critical field, B_c, for the formation of these sub-bands is that at which the wire width is equal to the cyclotron diameter, and is given by,

$$B_c = \frac{hk_f}{e\pi W} \qquad (1.17)$$

where W is the width of the wire, and all other terms are as previously defined. This can be shown to give,

$$B_c = \left(\frac{2}{\pi}\right)^{\frac{1}{2}} \frac{h}{e} \frac{(n_{2d})^{\frac{1}{2}}}{W} \qquad (1.18)$$

Above this field standard 2DEG behaviour is the dominant effect, but below B_c the effect of the boundaries is dominant. This was shown to be qualitatively valid by the experiments of Berggren et al, 1986, and Van Houten 1987. However, a more accurate estimate of wire widths from magnetoresistance oscillations requires a description of the system taking into account the nature of the confining potential, which is often modelled as being parabolic. For a full discussion of this see Berggren et al, 1988.

1.5.5 CAPACITANCE OF A 2DEG

The measurements discussed in the previous sections give valuable information on the methods of transport of electrons in a given system. Unfortunately, it can be difficult from these measurements alone to detect where the charge contributing to the conductance is positioned, and the exact amount of such charge. However, capacitance measurements give a direct measure of the magnitude of the charge in a system, and information on the distribution within the material.

Capacitance is a measure of the ability, or capacity, of a system to store charge. Capacitance is defined to be,

$$C = \frac{\partial Q}{\partial V} \tag{1.19}$$

where Q is the total charge and V is the voltage. The total charge in a system can, in principle, be found by measuring the capacitance of a system as a function of V and then integrating the C-V curve. This is of course dependent on the ability of the measurement to transfer charge at a rate at which all of the charge can be sensed. It can be readily shown that the expression for the capacitance of a parallel plate capacitor is,

$$C = \frac{\varepsilon A}{d} \tag{1.20}$$

where ε is the permittivity of the material between the electrodes, A is the area of the electrodes, and d is the separation of the electrodes. This can be used as an order of magnitude estimate to verify measurements of the capacitance of FETs fabricated on heterostructure material, as in certain limits the system can be treated essentially as a parallel plate capacitor, and allows the possibility of determining the position of free charge in a given system. However, it does not include the effects of the 2DEG. To include the 2DEG in the calculation it is necessary to consider the effect of two capacitances in series, these being the capacitive contribution from the AlGaAs and the capacitance due to electrons in the 2DEG.

The capacitance of an FET is the best way to investigate the depth profile of charge in a heterostructure. This has been modelled by several groups. For a particularly instructive paper with good physical insight see Norris et al, 1985. This

model sums the effective capacitances from sub-band electrons, occupied donors in the AlGaAs, free electrons in the AlGaAs and acceptors in the GaAs substrate. The measurement of the capacitance is dominated by two of these capacitive contributions. The first of these is due to the sub-band effects and the second is due to occupied donors in the AlGaAs. The Norris model agrees well with the experiments, made on FETs with thin spacer material, reported by the authors. The different capacitances are dominant in two distinct voltage regions. The occupied donors in the AlGaAs are closer to the surface of the material than the sub-band electrons, which means that these electrons result in a higher capacitance and will be cut-off first. This results in the formation of two distinct plateaus in the capacitance. The formation of a step was evident in many of the capacitance measurements taken in the course of this project.

1.5.6 CAPACITANCE OF NANOSTRUCTURES

The capacitance of a sample is sensitive to the charge in a system. Thus, in the quasi-1D limit the capacitance should be able to detect the population and depopulation of 1D sub-bands. This was the stimulus for the investigations of the capacitance of the multiple parallel wire samples performed by Smith et al, 1987. These experiments displayed the population and de-population of electron sub-bands using capacitance techniques. The advantage of this technique over conductance measurements is that the capacitance is not sensitive to the scattering processes dominant in the conductance measurements. The experiments of Smith et al will be outlined in detail in Section 1.7.

1.5.7 MAGNETOCAPACITANCE OF A 2DEG

Smith et al, 1985, made the first measurements of the density of states in an unrestricted 2DEG in the presence of a perpendicular magnetic field. They showed that the sample capacitance can be directly related to the density of states of a sample. The capacitance of their sample was measured as a function of perpendicular magnetic field, and the density of states was extracted from the measured capacitance by applying a model developed by Stern, 1983, to the system.

Stern modelled the total capacitance C_t, where C_t consists of the series capacitance of the AlGaAs barrier layer, C_b, and the channel capacitance, C_c. In this model the effects of series resistance and changes in the carrier concentration in the AlGaAs layer are ignored. Thus C_t is given by,

$$\frac{1}{C_t} = \frac{1}{C_b} + \left|\frac{dQ}{d\phi}\right|^{-1} \qquad (1.21)$$

where Q is the total charge and ϕ is the band bending defined in Figure 1.23, overleaf.

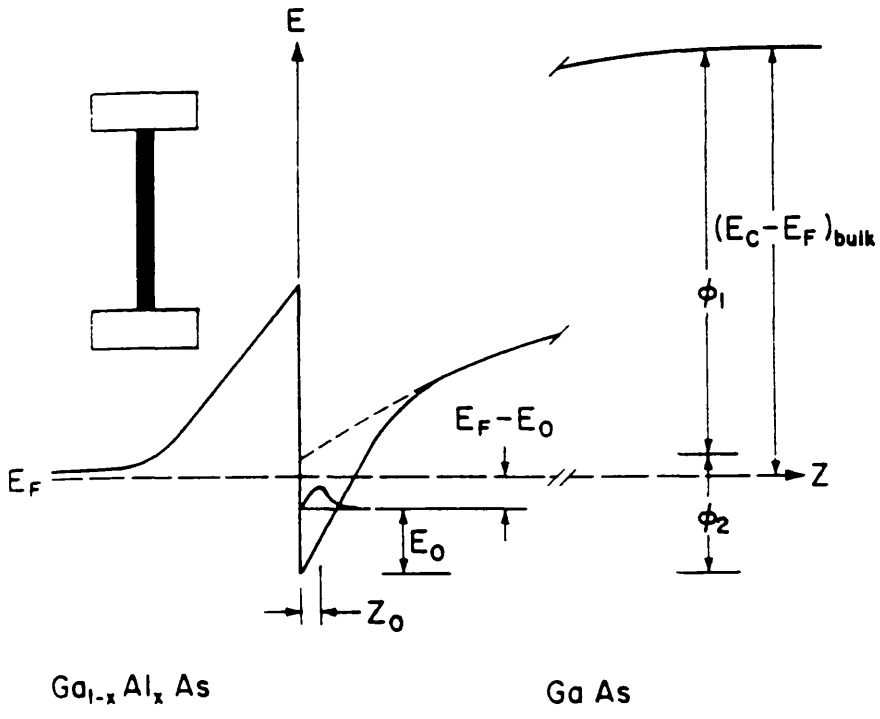


Figure 1.23 Schematic diagram of the conduction band edge for a modulation doped GaAs/AlGaAs heterojunction showing the quantities used in the derivation of the relationship between the measured capacitance and the density of states. An outline of the sample geometry is also shown.

Using a simple variational approximation which ignores image effects, many body effects, penetration of the wave function into the barrier and non-parabolicity of the band structure, Stern estimates that the channel capacitance is given by,

$$\frac{A}{C_c} = \frac{\gamma z_0}{\varepsilon_0 \kappa_c} + \frac{1}{e^2}\left(\frac{dn}{d\mu}\right)^{-1} \qquad (1.22)$$

where A is the area of the capacitor, z_0 is the average position of the electrons in the channel, γ is a numerical constant between 0.5 and 0.7, κ_c is the relative dielectric constant of the channel material, and $(dn/d\mu)$ is the thermodynamic density of states at the Fermi energy. Using this expression Smith et al extracted the density of states of a 2DEG directly from the measurement of magnetocapacitance as z_0, γ, ε_0, and κ_c are essentially constant. Thus

$$\frac{1}{e^2}\left(\frac{dn}{d\mu}\right)^{-1} = \frac{A}{C_{meas}} - \frac{A}{C_b} - \frac{\gamma z_o}{\varepsilon_o \kappa_c} \qquad (1.23)$$

where C_{meas} is the measured capacitance. It was found that the model of Stern agreed well with the experimental data.

1.5.8 MAGNETOCAPACITANCE OF NANOSTRUCTURES

The magnetocapacitance of nanostructures can be used to estimate the density of states in a similar way to that employed for the 2DEG. At low magnetic fields magnetocapacitance oscillations are similar to those of magnetoconductance. As with the magnetoconductance, the positions of the minima of the oscillations are periodic in 1/B for an unpatterned 2DEG. For a restricted 2DEG the oscillations should deviate from this periodicity when the cyclotron orbit exceeds the width of the wire. This is identical to the effect previously described for the magnetoconductance of wires. Again the pioneering measurements of the magnetocapacitance of wire samples were performed by Smith et al, 1988.

1.6 REVIEW OF DAVIES WIRE MODEL

In this section a review of a theory developed by Davies, 1988, for single squeezed wires (i.e. wires formed by the slit gate technique) will be given in some detail. This model was developed to estimate the electronic properties of wires near the threshold voltage, where there are so few electrons that the wire is nearly fully depleted. Working in this limit greatly simplifies the analysis, as in the cut-off region the electron wavefunctions are at their narrowest so that the spacing of the energy levels is maximised. The electrons can be regarded as moving in a purely external potential which can be found from electrostatics. Under these conditions it is no longer

necessary to solve self-consistently Schrodinger's equation and Poisson's equation, thereby allowing a simple analytical solution to the problem. The results of the model developed show a reasonable agreement with experimental data.

This model was used extensively in the analysis of data for the multiple wire samples and so will be reproduced here in full.

Squeezed wires are formed by confining electrons electrostatically with a negative potential applied to two gates with a narrow slit between them. A bias $-V_g$ is applied to the gates with respect to the channel. The source drain field along the length of the wire is assumed to be negligible. The bias sets the difference between the chemical potentials of the channel of the wire and the metal gate. If it is assumed that the chemical potential is constant throughout the semiconductor then the chemical potential for the surface states on the free surface between the gates is the same as that of the channel, and can be taken as being zero. The applied potential on the surface is therefore $-V_g$ on the metal gates and zero in the region between. The potential cannot change abruptly, so there must be a transition region at the edges of the gate that depends on the details of the surface states. The calculations could be modified to include this.

A summary of the method applied is as follows. Poisson's equation is solved for the electrostatic potential, with the boundary conditions that the free surface was an equipotential and that the electric field tended to zero as z tended to infinity. The dimensions are defined in Figure 1.24.

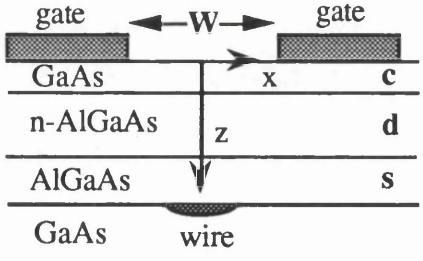


Figure 1.24 Diagram defining relevant dimensions and variables.

Electrons appear in the GaAs channel only if the difference in energy between the lowest bound state and the surface exceeds the potential barrier on the surface of the GaAs cap.

The total electrostatic potential can be split into two parts. The first is caused by the donors and depends only on the z, because the layers are uniform. The second contribution to the potential comes from the bias applied between the gate and channel. It has a more complicated spatial form, and is responsible for squeezing the electrons into a narrow channel. To find this potential, assume that the gates are sufficiently

wide that their outside edges can be ignored and treated as being at $x=\infty$. The electrostatic problem to be solved is to find the potential ϕ in the half space $z>0$. One boundary condition is that the electric field vanishes at infinity. The second is provided by the potential in the plane $z=0$, where $\phi=-V_g$ on the gates and $\phi=0$ in the gap between them. The potential in the $z=0$ plane can be split into two step-functions. Each of these gives a field over all space with equipotentials radiating out from the step. The potential at any point is proportional to the angle between the point and the x-axis measured from the step. This is an example of a (logarithmic) conformal transformation, or it can be obtained using Fourier transforms. Superposing the potentials from the two steps shows that the potential generated by a bias $-V_g$ on the gate is

$$\phi(x, z) = -V_g\left(1 - \frac{\theta(x, z)}{\pi}\right) \tag{1.24}$$

where θ is the angle subtended by the gap at the point (x,z). It follows immediately from elementary geometry that the equipotentials must be circles passing through the edges of the gates. The equipotentials form a radial pattern near the edges, characteristic of step-functions. From symmetry, electrons are expected to appear in the plane $x=0$, where the potential is given by

$$\phi(x, z) = -V_g\left(1 - \frac{2}{\pi}\tan^{-1}\left(\frac{w}{2z}\right)\right) \tag{1.25}$$

with ϕ_s the effective surface pinning potential. Using this it is possible to estimate the voltage at which the wires are fully depleted. Consider firstly the case of a uniform gate. If there is a uniform gate covering the whole $z=0$ plane, the voltage required to cut off the 2DEG can be found from

$$\phi_s + V_c = \frac{eN_D}{2\varepsilon_o\varepsilon_s}d^2 \tag{1.26}$$

It should be noted that this assumes that the AlGaAs is fully depleted at the cut-off point. For split gates, at $-V_c$ (the 2DEG cut-off) electrons beneath the gates are removed leaving an electron channel in the gap. It is at $-V_c$ that wires are just formed. Making the bias increasingly more negative reduces the width of the channel. This continues until the potential generated by the gate in the middle of the channel becomes $-V_c$. At this point the potential energy in the channel is $-e\phi_s$ with respect to the free surface, and the channel itself is cut-off. If the depth of the heterojunction is l, the bias $-V_c'$ needed on the gates to fully deplete the channel can be found by setting $z=l$ and $\phi=-V_c$ in Equation 1.22.

$$V_c' = -V_g\left[1 - \frac{2}{\pi}\tan^{-1}\left(\frac{W}{2l}\right)\right]^{-1} \tag{1.27}$$

This gives a theoretical estimate of the wire cut-off voltage.

This model has been shown to give results in good agreement with experimental data. However it is worth pointing out at this stage a problem with the analysis. The boundary conditions applied in the analysis require that the surface of the

semiconductor is an equipotential surface. In order to satisfy this requirement it is necessary for there to be a transfer of charge from the 2DEG to the surface in response to changes in the gate voltage. At low temperatures this seems an unlikely event and so presents a serious physical difficulty. Another model tested by Davies holds the surface at a fixed charge density, but this was shown to give poorer agreement with experimental data (Davies - a private communication).

1.7 REVIEW

In this section a brief review of some of the experiments inspiring the research conducted in this project will be given. These experiments are the first capacitance and magnetocapacitance spectroscopy measurements by Smith et al, 1987, the conductance measurements by Ismail et al, 1989, and finally the magnetoconductance measurements taken by Berggren et al, 1986.

1.7.1 CAPACITANCE OF MULTIPLE PARALLEL WIRES - SMITH ET AL, 1987

In 1987 Smith et al published data showing confinement effects in the capacitance of multiple wire samples fabricated on GaAs/AlGaAs heterostructure.

Capacitance is a direct measurement of the number of electrons in a given system. The capacitance of a quasi-1D system is therefore sensitive to the population, and de-population, of the 1D levels. This was the motivation for performing the capacitance measurements.

The sample design used by Smith et al is shown in Figure 1.25.

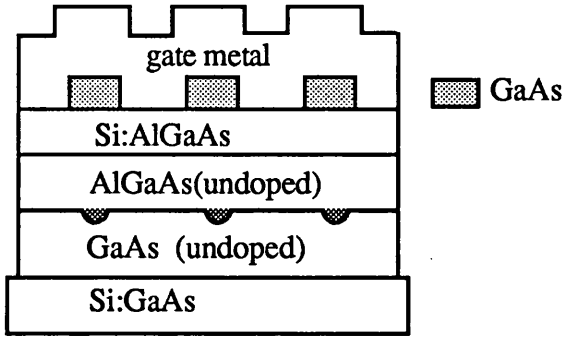


Figure 1.25 Sample design

The wires were formed in this experiment by etching through the GaAs cap thereby depleting the regions below the etched surface. A gate was deposited on top of this to

provide a means of controlling the width of the wires. The samples each had between 250-500 wires in parallel. The capacitance was measured between the gate and the Si doped GaAs back contact.

Smith measured the first derivative of the capacitance with respect to V_g. By filling or emptying the 1D sub-bands produced in the wires, a well resolved set of oscillations was measured. This was done for three different wire widths, see Graph 1.4. The separation in V_g of the oscillations agreed well with calculations performed in the IBM group by Stern and Laux. These experiments provided remarkable evidence of 1D quantum confinement effects in the wires. However because of the sample design no information on the conductance was gained. The magnetocapacitance of these samples was also measured and showed a deviation in the 1/B vs Landau index plot. This provided further evidence of the 1D confinement in the wires.

1.7.2 CONDUCTANCE SPECTROSCOPY - ISMAIL ET AL, 1987

The device used for these measurements is shown in Figure 1.26.

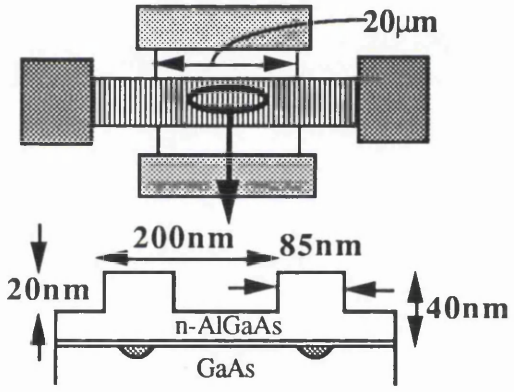
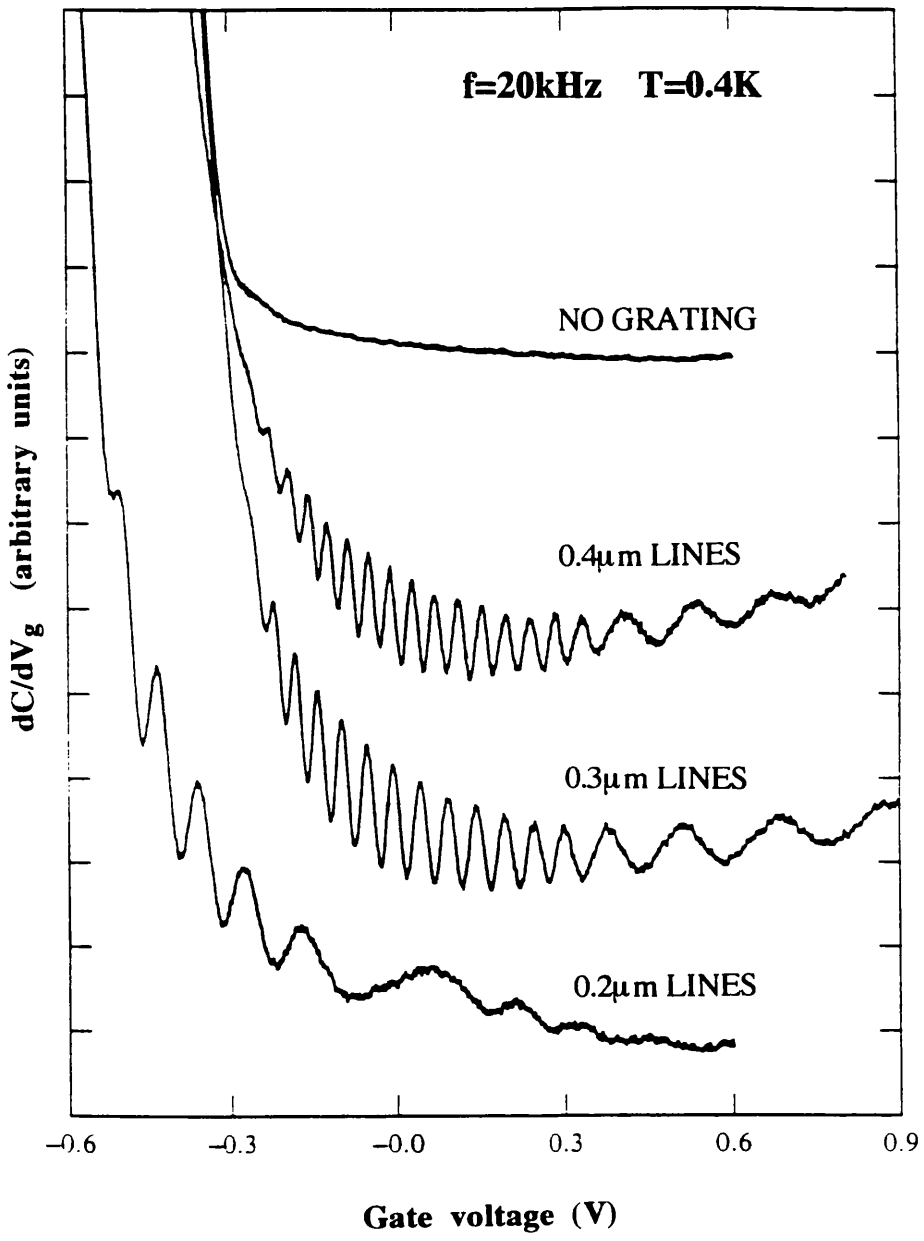


Figure 1.26 Sample design used by Ismail et al

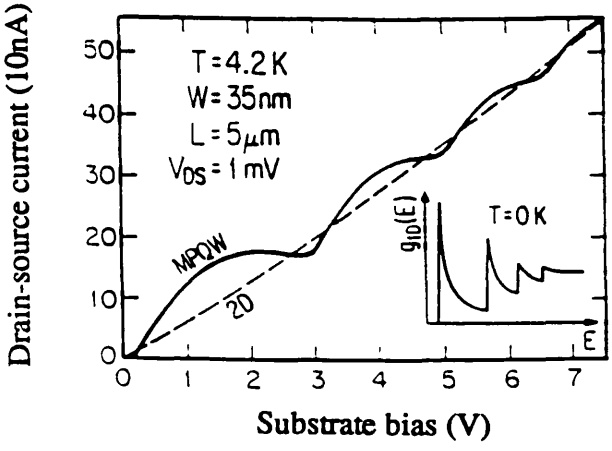
Again the sample was a multiple wire sample fabricated on GaAs/AlGaAs heterostructures. The wires were created by ion beam milling a shallow grating into the doped AlGaAs layer. The width of the wires was controlled by a back gate bias.

The experiments conducted by Ismail et al show evidence of quasi-1D density of states and a corresponding modulation of the electron mobility above and below values in the two dimensional system. These effects were seen strongly at 4.2K and more weakly at 77K. The results are shown in Graph 1.5.

Confinement efects have also been observed in the conductance of wires fabricated in Si inversion layers by Warren et al, 1986, and Gao et al, 1990.



Graph 1.4: Capacitance oscillations, measured by Smith et al, due to 1-D confinement in multiple parallel wires.



Graph 1.5: Drain source current as a function of substrate bias for the multiple wire sample (solid line) and scaled down 2D channel (dashed line). The inset shows the theoretical density of states in a Q1D wire at 0K. Data from Ismail et al, 1987.

1.7.3 MAGNETOCONDUCTANCE OF WIRES - BERGGREN ET AL, 1986

The classical effects of a magnetic field perpendicular to the plane of a 2DEG on the resistance were discussed in in section 1.5.3. Confinement effects in nanostructures, discussed in section 1.5.4, may also be apparent in the magnetoresistance . The first measurement of the magnetoresistance of GaAs/AlGaAs wires was performed by Berggren et al, 1986, and displayed confinement effects.
The structure used by Berggren is illustrated in Figure 1.27.

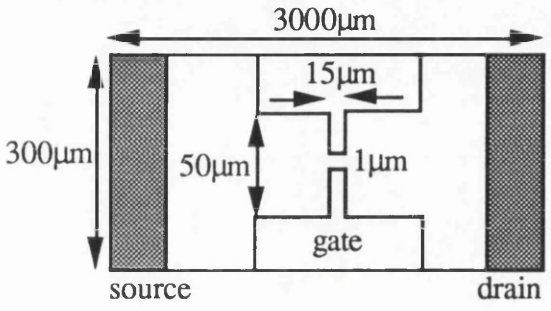


Figure 1.27 Sample used by Berggren

The magnetoconductance was measured at various gate biases. When the estimated wire width was less than 250nm, deviations were seen in the 1/B periodicity in the Shubnikov de Haas data. This was attributed to the successive depopulation of hybrid electric-magnetic sub-bands.

The results are shown in Graph 1.6. From this it can be seen that the deviation occurs at about $1/B=1.67T^{-1}$.

This effect has been measured by many groups since 1986, with some of the more instructive papers as follows: Van Houten et al, 1987, Gao et al, 1990 and Hirler at al, 1990.

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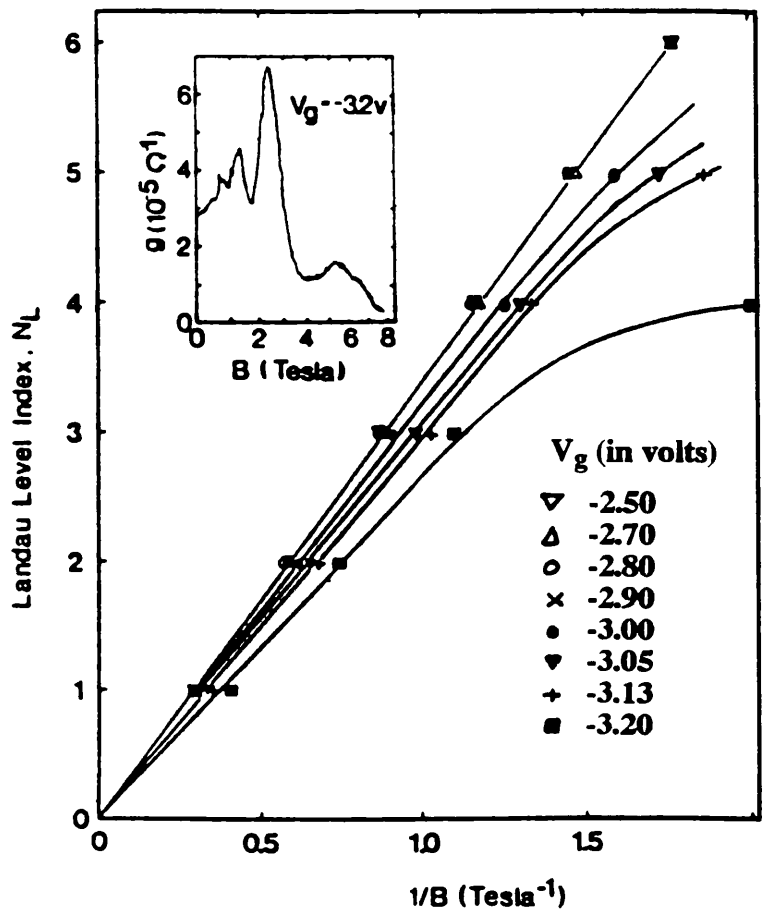

Graph 1.6: A fan diagram showing the conductance as a function of reciprocal magnetic field. For channel widths 500nm>t>250nm (-2.5V>V_g>-3.2V) the points are coincedent but for widths 250nm>t>150nm (-3.0V>V_g>-3.2V) there is a pronounced departure from 1/B behaviour. Inset: Magnetoconductance oscillations for a channel of width 150nm at a temperature of 0.35K. Data taken from Berggren et al 1986.

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CHAPTER TWO

SAMPLE DESIGN AND FABRICATION

2.1 INTRODUCTION

To produce devices with the dimensions required to see quantum effects it is necessary to use high resolution lithography. Several such types of lithography are currently available; for example, X-ray, focussed ion beam, and electron beam lithographies. The type of lithography used for the fabrication of devices for this project was electron beam lithography (EBL). In this chapter, as a general introduction to the processing of devices, EBL, metal-semiconductor contacts and semiconductor etching techniques will be discussed. A brief outline of the semiconductor growth technique, molecular beam epitaxy (MBE), used to produce the material, will also be given. Thereafter, more specific information on the material used, the sample design, and the fabrication techniques employed in the preparation of the multiple wire samples will be discussed.

2.2 ELECTRON BEAM LITHOGRAPHY(EBL)

Electron beam lithography is a technique widely used for the fine patterning of materials. The substrate is coated with an electron sensitive material called resist. Exposure to high energy electrons causes chemical and/or, physical reactions to occur in the resist, thereby enabling patterns to be 'written' on the substrate. Subsequent development of the resist after exposure, using the appropriate solvents, results in patterns being formed in the resist, making the resist essentially a stencil for the required pattern. Further processing using metal deposition or etching techniques makes these patterns permanent features.

2.2.1 GLASGOW UNIVERSITY ELECTRON BEAM FACILITIES

At the time this project was conducted, the electron-beam system used in Glasgow was a Philips 500 scanning electron microscope, modified for the purposes of lithography, Mackie, 1984 and Adams, 1990. The Philips system is illustrated below in Figure 2.1. Various new systems are now available but will not be discussed.

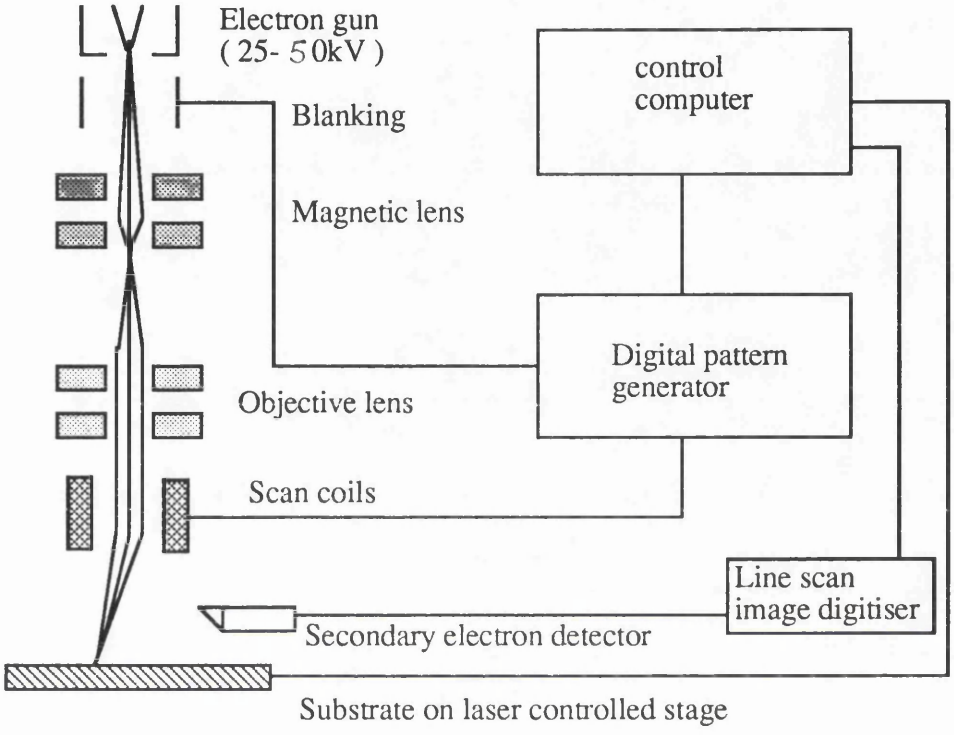

Figure 2.1 Glasgow electron beam system - modified PSEM 500

The electron source used is a tungsten hairpin. This is heated to temperatures in the range 2300-2700 degrees centigrade by a low voltage. The electrons are accelerated down the microscope column by a high tension of 50kV past a blanking stage which, when enabled, can deflect the beam sufficiently to prevent electrons reaching the sample stage (thereby 'blanking' the beam), and then pass through a magnetic focussing lens. It is at this stage that the diameter, or spot size, of the beam is determined. The magnitude of the spot size available in this system is in the range 8nm-1μm. Electrons then pass into an electromagnetic objective lens and are guided into the scan coils where, finally, they are deflected onto the sample.

The scan coils, as the name suggests, guide the incident electron beam onto the regions allocated for exposure. These coils are driven by a computer controlled digital pattern generator. The digital pattern generator determines the areas of the substrate to be scanned, that is exposed to the beam, controls the scanning procedure and blanks

the beam where necessary. The maximum scan field available in this type of system is typically $1cm^2$. The stage is also computer controlled - this allows automatic stepping of the stage from one site to another on the substrate. The stage can be rotated and moved in the x and y directions.

The resolution, or minimum feature size, of devices fabricated using systems of this type is determined by several factors: probe diameter, that is the diameter of the e-beam incident on the substrate, electron scattering, secondary electron generation, and long range chemistry and molecule size effects in the resist. The resolution is of the order of 10nm.

Extensive software has been developed to improve the performance of the Philips system and make it more user friendly. This software has many useful features, some of the more important being outlined below:

DESIGN: This is a software package developed in the Electronic and Electrical Engineering Department by Dr. S. Thoms to facilitate the design of patterns required for lithography. The patterns are drawn using mouse controlled graphics on a 4096x4096 pixel frame. The resulting coordinates are stored in files. Most device fabrication involves several different process stages, or levels. With the design facilities available it was possible to have up to twenty different levels. The coordinate files contain the dimensions of the patterns to be scanned but contain no information on the beam dwell time required at each pixel. Therefore, it is necessary to add exposure data to these files, which is entered in the form of an intensity, that is energy per unit area per second. To calculate the required dwell time it is necessary to have a measure of the beam energy and the beam diameter. The beam energy is found from the beam current which is measured by a picoammeter, and the spot size, or beam diameter, is fixed for a given scan. The computer calculates the required scan dwell time from this information. The exposure is one of the most important variables in the fabrication of devices by EBL - it is usually necessary to vary exposure when designing new patterns to fully optimise the lithography.

EBSS: This is the main software package, again developed in the Electronic and Electrical Engineering Department. This was run on an IBM compatible Olivetti computer for the control of the scan generator, and sample stage. There is also an IEEE interface to a picoammeter which monitors the e-beam current. To begin a typical scan several pieces of information must be supplied to EBSS: pattern files, magnification, beam current, position file, and sample orientation. The pattern files are generated using DESIGN. The beam current is measured by the picoammeter. Position files (files which contain information on the positions on the sample at which the defined patterns are to be scanned) are generated using a short routine, CALCP4, which calculates the positions on the chip from information on chip size, number of

sites required, the necessary site separation, and also the level to be scanned at a given site. The sample orientation is determined by entering the coordinates of the left side corners. Once this information is loaded it is possible to run the main stepping routine called "Step and Repeat". "Step and Repeat" is a routine which reads the coordinates from the position file, moves the stage to the appropriate position, scans the defined pattern, and then moves on to the next site. This stepping procedure continues until all the sites in the position file have been scanned. The estimated resolution with which the stepping motors on the sample stage operate is 1μm. This limits the use of the Philips for pattern 'stitching', that is joining together adjacent patterns.

There are several other facilities available within EBSS which, although not crucial, are very useful. Briefly, these are as follows: automatic focusing at every site (this is important in obtaining consistent results for fine features), automatic alignment of levels (this is useful for chips with large numbers of sites as the manual alignment of levels is time consuming), and finally a very user friendly editing facility which can be called on at virtually any stage whilst in EBSS.

2.2.2 ELECTRON BEAM RESISTS

Electron resists are polymers. There are two types of resist available: positive and negative resist. Positive resist is one in which polymer/electron interactions serve to break the long chain polymers into smaller units. The smaller molecules can be selectively dissolved in solvents which attack only low molecular weight material - this process is known as development. Negative resist acts in the opposite way, in that the areas of the resist exposed to e-beam remain after chemical development. This is due to radiation induced crosslinking of the polymer molecules resulting in regions of high molecular weight material. The resist profiles before, and after development are shown below in Figure 2.2.

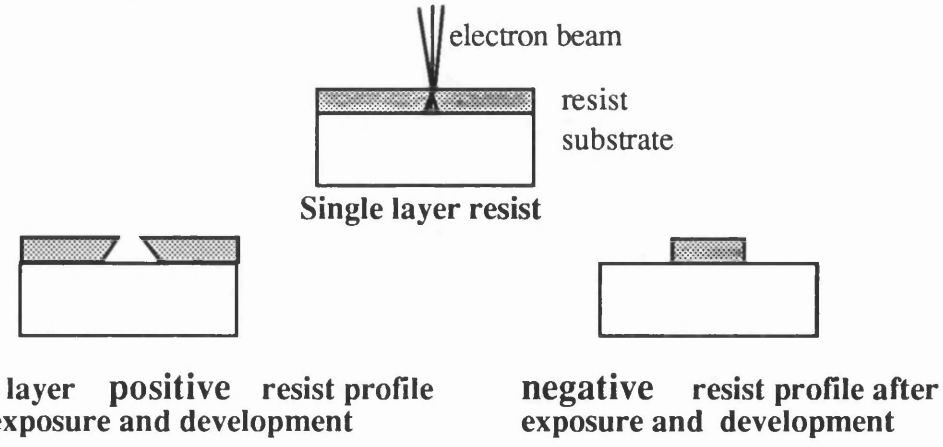

Figure 2.2 Single layer resist profiles before, and after, exposure and development

The positive resists used in Glasgow are PMMA $((CH_2CCH_3)COOCH_3)_n$ which is manufactured by BDH, and will be referred to as PMMA, and elvacite, made by Dupont Chemicals. The molecular weights of PMMA and elvacite are 85,000 and 350,000 respectively. The negative resist used is HRN (high resolution negative resist). All the resists are available in different concentrations. It is usually necessary, initially, to try various solutions to obtain the optimum for a given application.

(a) Positive resist processing

Resist is deposited on substrates by dissolving resist powder in solvent, dropping it onto the surface of the sample and spinning it at frequencies in the range 1-8kHz. If PMMA is used, the sample is then baked at 180C to remove traces of the solvent. The thickness of the resultant layer depends on the amount of solvent in which the resist was dissolved and the spinning frequency. The thickness of the resist layer plays a major part in limiting the final resolution. Line widths of 25nm have been achieved using single layer positive resists and lift-off techniques.

(b) Lift-off

One of the major uses of positive resist is for the patterning of metal contacts. The technique for forming these contacts after EBL and development is commonly referred to as lift-off. Firstly metal is evaporated onto the patterned sample then the sample is immersed in acetone. Positive resist dissolves in acetone so metal not in contact with the substrate is lifted off leaving permanent metal features on the substrate surface. The metal lift-off can be improved by using warm acetone, usually at about 40C. The lift-off process is illustrated in Figure 2.3.

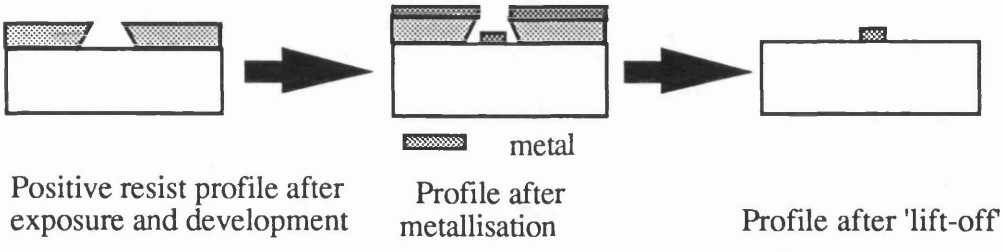

Figure 2.3 'Lift-off' process

The main criterion for resist is that the resist thickness must be greater than the required metal thickness. However, the profile of the resist is also important. It is best to have a slight 'overhang' effect as this prevents coating of the resist walls, and so improves lift-off yield. To produce this effect routinely bi-layer resists are used.

(c) Bi-layer resist

The resolution of single layer positive resists is about 25nm, but can be reduced further by using bi-layer resist systems. The bi-layer resist is formed by firstly spinning PMMA on the substrate and then baking for an hour at 180C to harden. PMMA has a lower molecular weight than elvacite, and is therefore the more sensitive of the two positive resists. Elvacite is then spun on top of this and the chip is baked for a minimum of two hours, again at 180C. When resist systems of this nature are exposed and developed a small window in the upper layer (less sensitive of the two) is opened, and a larger window in the lower layer. This creates a resist profile in which the upper layer hangs over the lower level. This is often a desirable situation, particularly when evaporating metals as it prevents the resist 'walls' from being fully coated with metal, see Figure 2.4.

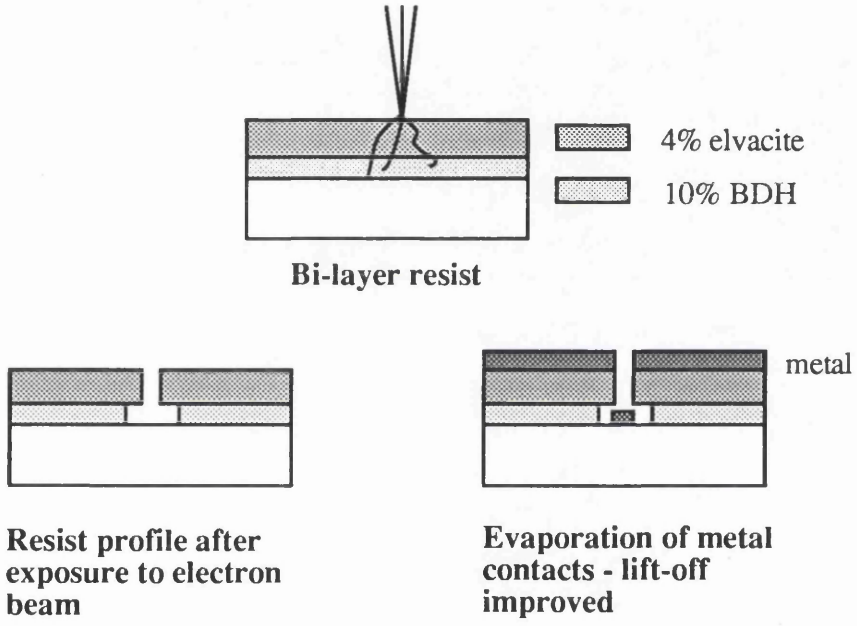

Figure 2.4 Bi-layer resist profile

The main advantages of using bi-layer resist are improved resolution, due to the shielding effect of the lower layer protecting the elvacite from backscattered electrons, and higher lift-off yield, as a result of the overhang profile. A further benefit is that, by using two layers, the likelihood of there being pinholes (sometimes a problem with single layer resists) is greatly reduced.

(d) Negative resist

The method of deposition of negative resist is identical to that used for positive resist except that a different solvent is used, and is removed by baking at 120C. The

resolution of HRN is similar to that of the single layer positive resists - about 25nm. Exposed HRN is resilient to all of the common chemicals used for processing, and so, for the purposes of this project, is very useful. It is often quicker to work with HRN when processing.

2.3 METAL-SEMICONDUCTOR CONTACTS

There are two types of metal - semiconductor contacts: rectifying or Schottky contacts, and non-rectifying or ohmic contacts. The fabrication requirements for each of these will be discussed.

2.3.1 OHMIC CONTACTS TO GaAs/AlGaAs HETEROSTRUCTURES

To make ohmic contact to GaAs and GaAs/AlGaAs heterostructures it is necessary to dope artificially the semiconductor in the region at the interface between metal/semiconductor, by diffusing suitable dopants into the semiconductor. This serves to decrease the width of the depletion region at the metal semiconductor interface, thereby allowing electron tunnelling across the interface to occur.

The metals used to form ohmic contacts are typically Au, Ge, and Ni (Pd is also used occasionally). The type and thickness of the layers deposited depends on the material being used. However, as a general guide to the functions of the metals, Ge is used to dope the semiconductor, Ni is used to improve surface adhesion, and Au is included to provide a good medium to contact the outside world. A typical recipe used to form ohmic contact to GaAs/AlGaAs heterostructures is as follows:

1. Ni 8nm
2. Ge 120nm
3. Au 136nm
4. Ni 80nm
5. Au 50nm

To form the contact it is necessary to diffuse the Ge into the active region of the heterostructure, that is the 2DEG. This is achieved by heating the sample, or annealing. The temperature and time required to do this are dependent on the material used. For a more complete description of ohmic contacts see Sze, 1981.

2.3.2 SCHOTTKY CONTACTS TO GaAs/AlGaAs HETEROSTRUCTURES

To form Schottky contacts it is necessary to use metals which increase the depletion region at the metal/semiconductor interface, thereby reducing electron tunnelling. For the gates fabricated in this project Ti and Au were used. A typical recipe being, 100nm of Ti then 200nm of Au.
There is no annealing stage for the Schottky contact.

2.4 SEMICONDUTOR ETCHING TECHNIQUES

There are two techniques employed for the etching of semiconductors: wet etching and dry etching. For the purposes of this project wet etches were used, but dry etching is included as it was felt necessary to provide an insight into the fabrication techniques employed by other groups working with similar devices.

2.4.1 WET ETCHING

Wet chemical etching is used extensively in semicondutor processing. The mechanisms for wet etching involve three essential steps: (1) the reactants are transported (e.g. by diffusion) to the reacting surface, (2) chemical reactions occur at the surface, and (3) the products from the surface are transported away, for example, by diffusion. Both agitation and the temperature influence the etch rate.

Two wet etches were tried, both of which used H_2O_2 as the etching agent . Table 2.1 shows the details of the etches used.

Etch constituents	ratios of volumes	etch rate (per min)
$H_2O : H_2O_2 : H_2SO_4$	200 : 1 : 5	20nm
$H_2O : H_2O_2 : NH_3$	250 : 2 : 5	300nm

Table 2.1 Details of wet etches used

The sulphuric acid etch was used initially, but it was found that this regularly did not isolate the conducting regions and left an unacceptable amount of debris on the

surface of the semiconductor, which was often very difficult to remove and resulted in low yield after an etch. This method of isolation was abandoned.

The ammonia based etch was found to be fast, and very clean. This etch was adopted.

Wet etching is a fast and, generally, reliable method of etching semiconductors. The main disadvantage of this method is that it is an isotropic process, the semiconductor being etched equally in all directions. This limits the use of wet etches for the fabrication of small features. Dry etching is not isotropic and so is employed for the fabrication of nanostructures.

2.4.2 DRY ETCHING

Dry etching is used to fabricate devices with small features. The basic steps involved in this process are shown in Figure 2.5.

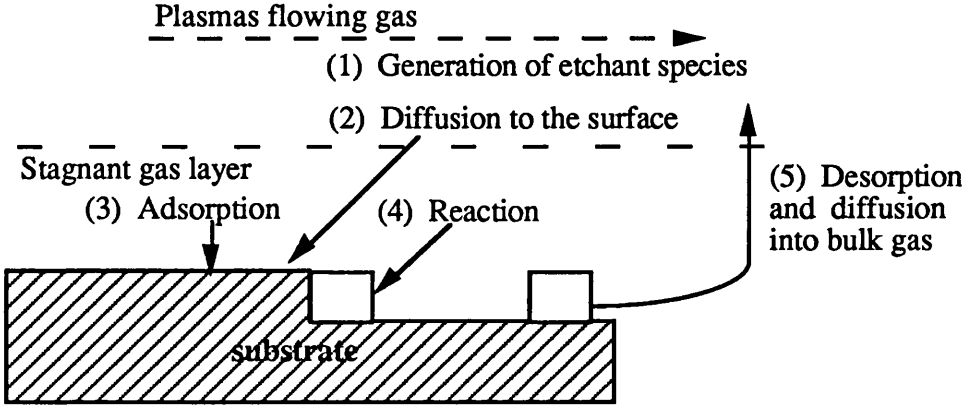

Figure 2.5 Steps involved in dry etching process

The process begins with the generation of the etchant species in a plasma. The reactant is then transported through a stagnant gas layer to the exposed surface, where it is adsorbed. This is followed by chemical reaction , with physical effects such as ion bombardment, to form volatile compounds. These compounds are desorbed from the surface, diffused into the bulk gas and pumped out by the vacuum system.

2.5 MOLECULAR BEAM EPITAXY(MBE)

MBE was the growth process used to produce all the material used in this project. This process has been described by C.T. Foxon, 1990, as a refined form of vacuum evaporation. The molecular beams are produced by evaporation or sublimation from heated liquids or solids contained in crucibles. The flux produced is determined

by the vapour pressure of the element or compound in the MBE source. At the pressures used in MBE equipment, collision free beams from the various sources interact chemically on the subtrate to form an epitaxially related film. Ultra high vacuum techniques are used to reduce the pressure of gases from the ambient background and thus improve the purity of the layers.

2.6 FABRICATION OF MULTIPLE WIRE SAMPLES

In this section a detailed description of the design and fabrication of the multiple wire samples will be given.

2.6.1 MATERIAL

The multiple wire samples were fabricated on molecular-beam-epitaxy (MBE) grown GaAs/AlGaAs heterostructures. As discussed in chapter 1, in this type of material the mobile carriers are separated from the dopant ions, thus reducing ionised impurity scattering, increasing mobility, and making it an ideal system in which to investigate quantum effects.

To avoid having to repeatedly present material details in the experimental chapters the materials used in the course of this project have been tabulated in Table 2.2. Two materials were investigated, with identification numbers A216 and A425. The samples were numbered according to material, chip number and then site number, so for example, A21614 was A216 material, chip number 1 and site number 4.

material details	A216	A425
c (nm)	170	170
d (nm)	500	500
s (nm)	400	400
N_D $(10^{18} m^{-3})$	0.8	0.8
n_{2d} (1.2K) $(10^{15} m^{-3})$	2.7	1.6
μ (1.2K) $(cm^2 V^{-1} s^{-1})$	300,000	800,000

Table 2.2 Materials used for fabrication of multiple parallel wires, where c is the thickness of the GaAs cap, d is the thickness of the doped AlGaAs layer, s is the thickness of the spacer layer, N_D is the dopant concentration in the doped AlGaAs layer, n_{2d} is the carrier concentration in the 2DEG, and μ is the electron mobility.

2.6.2 SAMPLE DESIGN

A cross-section through the gate and the sample design are shown in chapter 1, figures 1.9 and 1.10, respectively. From this it can be seen that the structure is essentially a long gate field effect transistor (FET) with wires under the gate. The dimensions of the device were chosen to maximise the gate area, making the source-gate capacitance a measurable quantity, and yet still have the resolution available to fabricate wires with dimensions in the few hundred nm range.

2.6.3 FABRICATION TECHNIQUES

The multiple wire samples require seven process stages: sample preparation, formation of ohmic contacts, isolation of active region, surface cleaning, formation of wires, production of gates, and finally, formation of bonding pads.

(a) Sample preparation

Before lithography it is necessary to prepare the substrate. This involves scribing the required chip size, a cleaning stage, and the deposition of resist on the substrate surface.

(a) Sample scribing: This was done using a diamond tipped scribe bit. Chip sizes of as little as $1mm^2$ can be obtained using this type of scriber. However at this stage it was standard to use chip sizes of $(5 \times 6)mm^2$.

(b) Cleaning procedure: The substrate was cleaned by immersing the samples in various chemicals and then placing them, in turn, in an ultrasonic bath to aid the cleaning process. The chemicals used are given below in the order of use. The sample was cleaned in each chemical for five minutes.

1. trichloroethylene
2. methanol
3. acetone
4. rinse in isopropyl alchohol (IPA), blow dry with nitrogen

(c) Resist deposition: The resist used for the ohmic level of the multiple wire samples was a 10% PMMA/4% elvacite bi-layer. The 10% PMMA was deposited on the sample in liquid form and then spun at 5kHz for 60 seconds. This was the optimum value for this particular application, but if thinner resist layers are required then a higher spinning frequency, or a thinner resist can be used. The sample was then baked at 180C for a minimum of 1 hour, to allow the resist to harden. The process was repeated for the elvacite, and the sample baked for a further 4 hours. The resist thickness resulting was 700nm.

(b) Formation of ohmic contacts

Six stages were required to form ohmic contacts: EBL, development of resist, de-oxidisation, metal deposition, lift-off, and finally, annealing.

(a) EBL: The ohmic contact pattern is illustrated on page8.This level was exposed at a magnification of 160, the spot size used was 0.25mm, and the exposure value used was 390. Each site took about three minutes to scan.

(b) Resist development: 10% BDH/4% elvacite was developed in 1:1 MIBK : IPA, at 23C for 30s.

(c) De-oxidation: This stage was required to remove any oxide on the exposed areas of substrate. This was achieved by immersing the sample in solution of 4:1 water : HCL, for 60s. The sample was then dried with nitrogen and quickly put into the evaporator to avoid further oxidation.

(d) Metal deposition: The metals were evaporated onto the surface of the chip. Two types of evaporator were used for this purpose; an interlocked evaporator, in which the metals are heated by applying a high field across crucibles containing the metal, and an e-beam evaporator, in which the heating is caused by an incident beam of high energy electrons. The metals used to form the contacts were as follows:

1. Ni 8nm
2. Ge 120nm
3. Au 136nm
4. Ni 80nm
5. Au 50nm

(e) Lift-off: The lift-off technique is illustrated in Figure 2.3. The excess metal was removed by dissolving the resist in acetone. This was made easier if the acetone was heated to about 40C.

(f) Annealing: This was required to diffuse the germanium from the surface of the substrate into the doped region, where it actually contacted the carriers. For the HEMT ohmics an annealing temperature of 360C was maintained for 30s.

(c) Isolation of active region

This level was required to isolate the ohmic contacts from the gate pad. The method used was to effectively dig a trench around the ohmic contacts and the conducting channel. The trench was exposed as a series of rectangles round the ohmics and the active region. The magnification used was 160 with the spot size 125μm, and the exposure value 390. After exposure and development the trench was 'dug'. This was done using the ammonia based wet etch previously described.

(d) Surface cleaning

This stage was essential to ensure that the active channel was clean before exposing the wires level. The entire cleaning process outlined previously was repeated.

(e) Formation of wires

The resists used were 8% and 6% HRN, spun at 7kHz, for 60s. Both of these were baked at 120C for twenty minutes. The wires were exposed approximately midway between the source and the drain contacts. The magnification used was 160, the spot sizes used were 16nm and 32nm, and the exposure values ranged between 140 and 200. Typically 250-500 wires were exposed in the channel, depending on the thickness and spacing, or pitch. The HRN was developed in MIBK for 15s, then IPA for 15s, and then a complete repeat of this. This method was found to give the best edge profile.

(f) Production of gates

The 10% BDH/4% elvacite bi-layer resist outlined previously was used for this layer. The magnifaction used was 160, the spot size was 125nm and the exposure value was 390. The resist was developed in 1:1 MIBK:IPA. The gate length varied between 15-17μm, and the width was constant at about 400μm. The metals used to form the Schottky barrier were Ti and Au. The thickness of these layers was not crucial, the main criteria being that there was enough metal to facilitate external contact, and that the metal thickness was less than that of the resist. Usually 100nm of Ti and 400nm of Au were deposited.

(g) Formation of bonding pads

This was the final stage. It was required to make bonding to the ohmic contacts less difficult as it was difficult to bond to annealed Au. The magnification used was, again, 160, the spot size was125nm, and exposure value was 390. The metals forming the contact were 50nm Ni, then 400nm of Au.

2.7 SUMMARY

The fabrication techniques employed to fabricate multiple wire samples have been outlined in detail. It should be noted that the exposure values quoted were varied from time to time, which was usually necessary, for example, when a new batch of resist was produced, or some feature of the Philips system was altered. The figures are given as a guide, but should not be taken as being definitive. Experience has shown that fabrication is very sensitive to changes in the fabrication configuration.

2.8 REFERENCES

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CHAPTER THREE

EXPERIMENTAL APPARATUS AND TECHNIQUES

3.1 INTRODUCTION

In this chapter the experimental apparatus and techniques employed in the investigation of the transport properties of multiple wires will be discussed. The discussion will cover cryogenics, temperature measurement and control, sample mounting procedures, magnetic field provisions and finally measurement facilities.

3.2 CRYOGENIC FACILITIES

Three cryogenic systems were available, all of which access different temperature ranges. The first of these was a closed circuit cryocooler, which can reliably produce temperatures in the range 300K to 12K; the second was a He_4 pumped cryostat, which accesses the range 4.2K-1.2K and the last was a dilution refrigerator which can produce temperatures in the range 4.2K-30mK. Each of these will be discussed in detail.

3.2.1 CLOSED CIRCUIT SYSTEM

For cooling from room temperature to 12K a CTI Cryogenics Model 21 cryocooler was used. This system uses a Gifford McMahon cycle to cool to low temperatures, see White, 1968. This cycle has four stages. In the first stage compressed helium gas flows into the warm end of the cylinder when the piston is displaced towards the cold end. The piston then moves upwards and the size of the cold volume is increased - gas is displaced through the regenerator, towards the cold end, and more gas enters through the intake valve, which remains open to equalise the pressure. The third phase, the expansion phase, occurs when the intake valve is closed and the exhaust valve is slowly opened. The expansion causes the cold volume to be cooled and the final stage takes place as the piston moves downwards to displace

the remaining cold gas. By repeating this cycle, cooling to around 12K can be achieved in the CTI cryocooler.

3.2.2 He_4 CRYOSTAT AND INSERT

Another method of cooling uses the passive cooling of samples by liquid helium. The cryostat used was an He_4 cryostat. The system available was connected to a large pump to allow the temperature to be reduced below 4.2K, as when He_4 is pumped to a pressure of 1mbar the ambient temperature drops to about 1.2K. A heater was available in this system to provide access to stabilised temperatures between 4.2K and 1.2K, but was generally not used.

The He_4 cryostat and pumping lines are shown overleaf in Figure 3.1. The outer dewar was made of stainless steel and provided a bath for precooling the system with nitrogen. The inner dewar was of glass. The main external pumping line was taken into the He_4 bath and the pressure was monitored with a manometer.

The He_4 insert used is also illustrated in Figure 3.1. Starting from the top of the insert it can be seen that there were four main lines forming the insert. The three smallest of these contained electrical leads, the other was the main pumping line. One of the smaller lines contained leads to the temperature sensors, and the others contained leads which were taken into the vacuum can and onto the sample mount. A vacuum can was required in this system, firstly, to establish a vacuum to prevent water vapour freezing on the sample, and secondly, if it was necessary to measure at a temperature different from that of helium, to prevent He_4 leaking in from the He_4 bath. The seal was made with indium, and the vacuum can was pumped through the insert pumping line.

The minimum temperature achievable with this system was approximately 1.2K, to reach this it was necessary to take several precautions to avoid the transfer of heat from the top of the insert down the electrical leads. The first of these precautionary stages occurred at the base of the vacuum can. At this level the electrical leads were fed through thin metallic tubes and sealed with stycast, which is a material with a high thermal conductivity and a low electrical conductivity. Stycast can form good high vacuum seals as it has a similar thermal expansion coefficient to that of the Cu/Ni insert, which prevents cracking of the seal, or gaps forming at low temperatures. The final stage was at the sample wiring level where the contact pins were also sealed in stycast.

The mounting procedures used will be discussed in a later section.

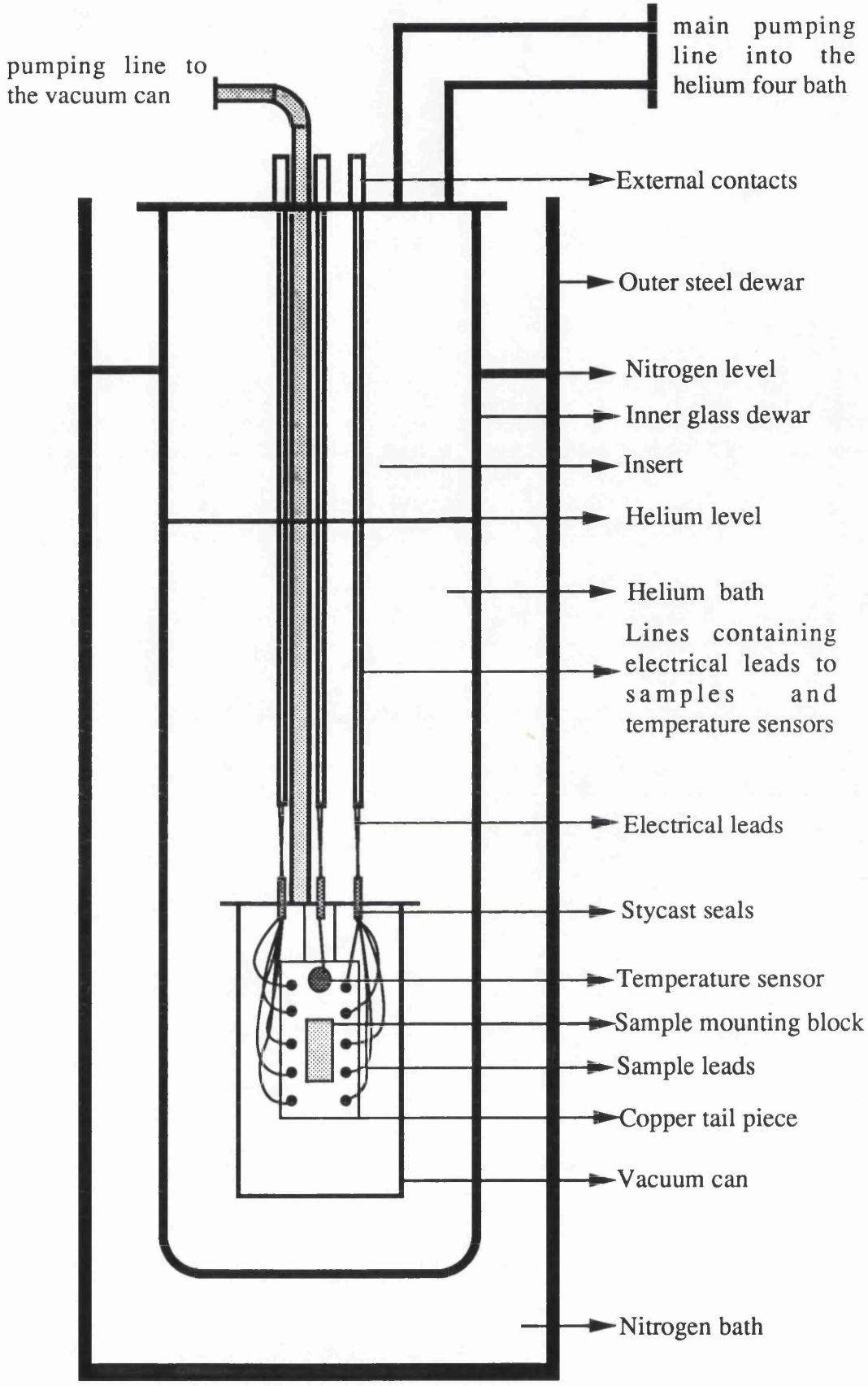


Figure 3.1 Helium four cryostat, pumping lines, and insert

3.2.3 DILUTION REFRIGERATOR

The dilution refrigerator used was an Oxford Instruments Kelvinox, which accesses temperatures in the range 30mK to 4.2K.

The cooling action of a dilution refrigerator is produced by using a controlled mixture of He_3 and He_4, the two isotopes of He. To understand exactly how a dilution refrigerator works consider the phase diagram of He_3-He_4 mixtures shown overleaf in Figure 3.2.

If the temperature of any mixture of more than 6%He_3 is lowered sufficiently the mixture separates into two phases. One of these phases is mostly pure He_3. The other is mostly He_4, but even at T=0 will have a 6% He_3 impurity content. This last point is the key to the operation of the refrigerator. After Nunes and Earle, 1991, a simple U-tube model of a dilution refrigerator is given in Figure 3.3.

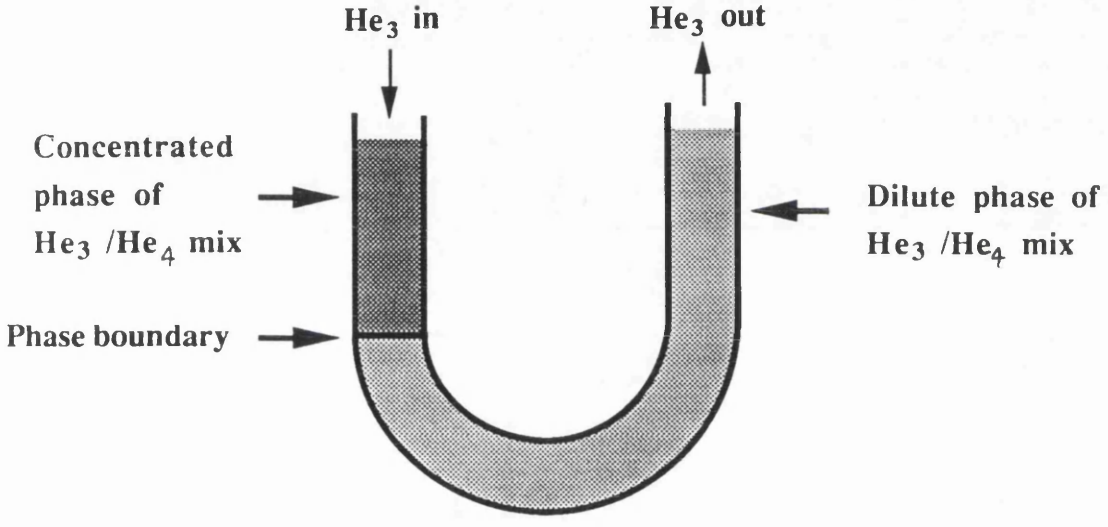


Figure 3.3 Simple U-tube model of a dilution refrigerator

If the liquid-vapour interface on the He_3-poor side is kept at about 0.7K, most of the vapour will be He_3. Pumping this vapour will remove He_3 from the liquid on the right hand side of the tube, and destroy the equilibrium between the two phases. In order to restore the equilibrium He_3 atoms "evaporate" across the phase boundary from left to right. For this migration to occur the associated latent heat must be supplied by the sample. Hence, the sample is cooled.

The insert used in the refrigerator was considerably more complex than that for the He_4 cryostat and is shown in Photograph 3.1, shown overleaf. The inner vacuum chamber section of the insert is isolated from the main He_4 bath by a stainless steel can which has an indium seal on the rim and is screwed to the top flange. Starting from the

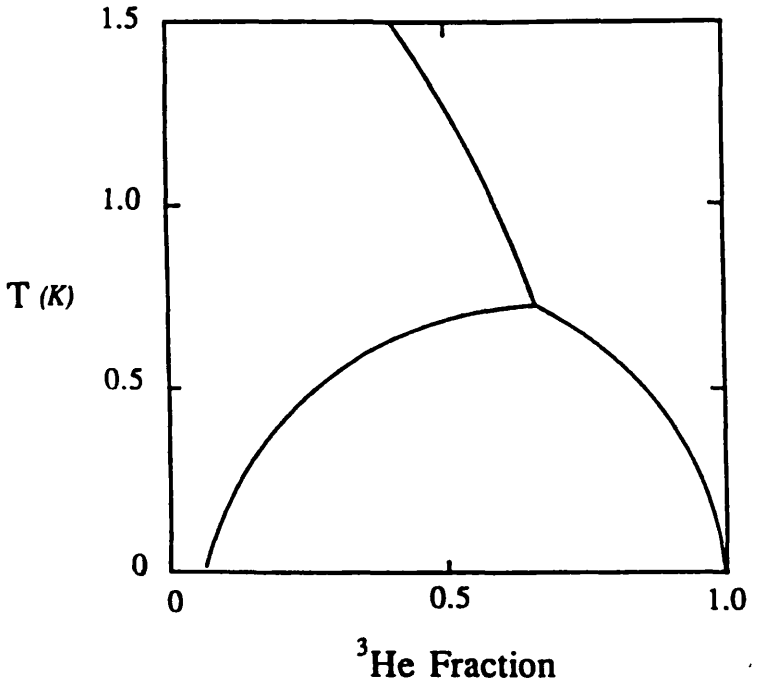
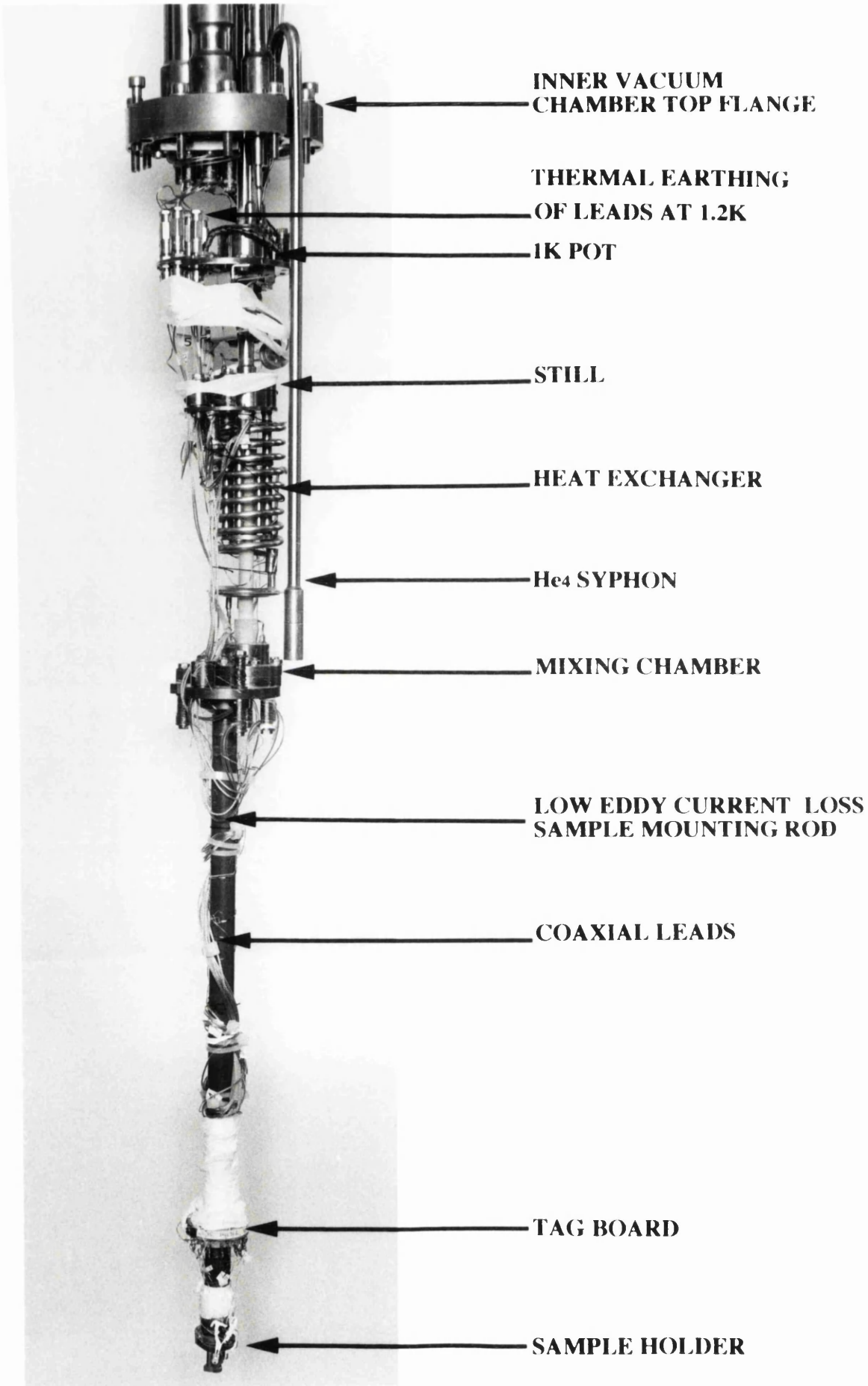


Figure 3.2 A representation of the He_3 - He_4 phase diagram

Photograph 3.1 Dilution Refrigerator Insert.


INNER VACUUM
CHAMBER TOP FLANGE
THERMAL EARTHING
OF LEADS AT 1.2K
1K POT
STILL
HEAT EXCHANGER
He4 SYPHON
MIXING CHAMBER
LOW EDDY CURRENT LOSS
SAMPLE MOUNTING ROD
COAXIAL LEADS
TAG BOARD
SAMPLE HOLDER

bottom the most important features are the sample mount, a tag board (at which electrical contact between the sample and external leads is made), a low loss mounting rod, coaxial leads, and then the mixing chamber - it is in this chamber that the phase boundary discussed in the previous section is established. Thereafter the stages are all present for the purpose of precooling the system, with the temperature increasing towards the top of the insert. There are 12 copper leads and 8 coaxial leads available on the refrigerator insert, the latter being necessary to perform high frequency capacitance measurements.

3.3 SAMPLE MOUNTING PROCEDURES

For the closed circuit and the He_4 insert, samples were mounted on twelve pin transistor bases, illustrated opposite, in Figure 3.4. The chips were glued to the transistor bases with Bostik. External contact was then made to the sample by bonding to the sample using an ultrasonic bonder. The bond is formed by pressing thin wire onto the surface of the contact and passing an ultrasonic pulse through the wire. This effectively vibrates the metal of the wire into the contact, thereby forming an electrical connection to the sample. After the first bond is formed the wire is then guided to a pin on the transistor base where the second bond is formed. To protect the bonds, which are very delicate, caps are fitted to the bases.

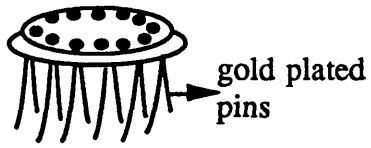


Figure 3.4 sample mount

Once the samples were mounted on the transistor bases, several methods were employed to mount them in the low temperature cryogenic systems available. For the closed circuit system and the He_4 cryostat a copper mount was designed to provide both good thermal contact and mechanical stability. This is illustrated, in Figure 3.5. The transistor bases fitted into the support which was then screwed securely to the second cold head, in the case of the cryocooler, or the copper tail piece of the He_4 insert.

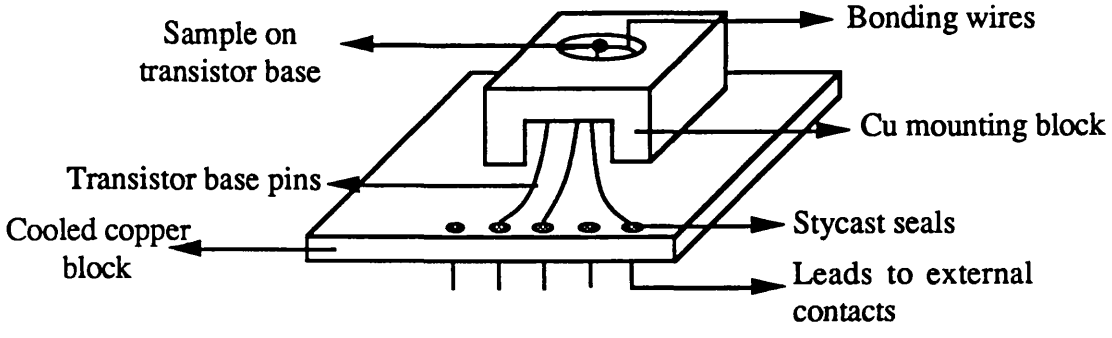


Figure 3.5 Mounting procedure used for closed circuit and He_4 insert

The procedure used for the dilution refrigerator was slightly different, here the sample was mounted on a copper support, then turned upside down and clamped to a copper block mounted on the end of the insert, as illustrated in Figure 3.6. This minimised the distance between the mixing chamber and the sample, and the number of boundaries, and therefore maximised the cooling effect.

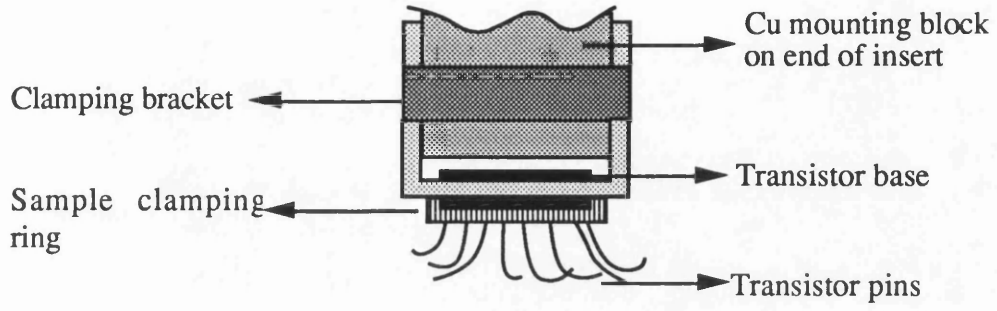


Figure 3.6 Mounting procedure used for the dilution refrigerator

Electrical contact was made to the samples by soldering the transistor pins to the insert leads. It was necessary to take care at this stage to avoid heating leads or charging the samples, particularly when contacting to Schottky gates.

3.4 TEMPERATURE MEASUREMENT AND CONTROL

Several temperature measurement and control systems were used. Each cryogenic arrangement had a separate system for the control and measurement of temperature. For the He_4 cryostat and the cryocooler, the systems were identical. For the dilution refrigerator the system was slightly different, and consequently will be discussed in a separate section.

3.4.1 He_4 CRYOSTAT AND CRYOCOOLER

Temperatures were measured using sensors whose resistance varied with temperature. A constant current was applied to all the sensors used and the voltage measured. This was controlled by a temperature control unit (TCU).

(a) Temperature sensors

The sensor used in the CTI Cryocooler was a silicon diode, this type of sensor being effective over the range 300K-4K. At a constant sense current of 10μA the voltage drop across the diode increases from 0.4V to 2.0V over the temperature range 300K to 12K. This sensor was precalibrated by the manufacturer, Lakeshore.

For the He_4 insert two sensors were used, a carbon and a germanium resistor. The germanium resistor was calibrated by the manufacturer from 40K to 1.2K, with the most accurate calibration information lying in the 5K-1.2K range. As with the sensor used in the Cryocooler, to ensure accurate readings of sample temperature, it was essential that the sensors were securely in contact with the insert. For temperatures below 4.2K, the He_4 vapour pressure was also monitored as a cross check of the resistors.

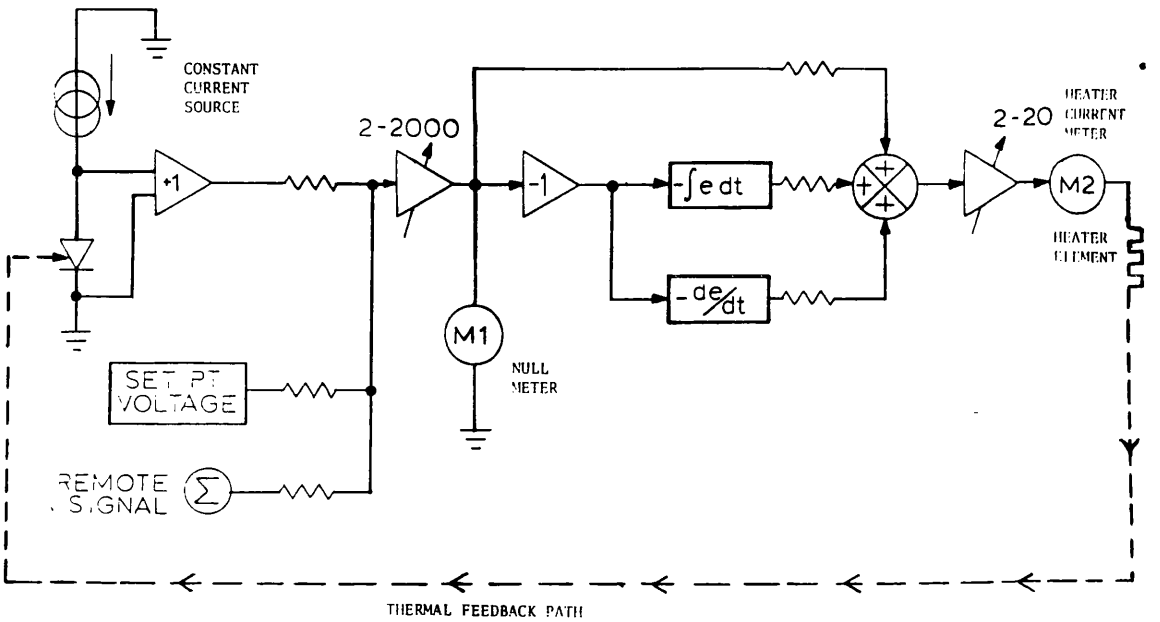
(b) Temperature control units

Temperature control units operate by applying a constant current to a sensor and measuring the voltage, thus determining the temperature. To select a temperature above the boiling point of a liquid gas the voltage signal must be monitored, amplified and compared with a reference signal which corresponds to a preset temperature. This process enables a controlled output current through a constantan wire heater to be produced, thereby heating the sample and surroundings to the required temperature. Automatic operation ensures that the temperature is monitored constantly, allowing the heater output to be controlled precisely. A typical T.C.U. is shown overleaf in Block Diagram 3.1.

Two TCUs were used in the course of this work - a Lakeshore Cryotronics Inc. Cryogenic TCU model DTC-500SP for the cryocooler, and an updated version of this, a Lakeshore TCU model DRC 91C, for the He_4 cryostat. Both of these units operate on the same principle, and contain the following stages:

1. A constant current source to supply the thermometers.
2. An amplifier to amplify the voltage across the thermometers - this creates a positive current through a 3MΩ resistor and is fed into a current summing amplifier.
3. The digital set point (preset temperature) is converted to an analogue voltage by a DAC. The resulting negative voltage is applied to a string of resistors and the current generated is fed into a summing amplifier to balance the thermometer current. When a balance is reached the digital set point is the actual temperature measured by the sensor.
4. The error signal is measured on a null meter and can be integrated. The integrated output signal is then added to the existing controller output. This enables the overall output to change until no error remains. The temperature is now at the required point with no offset in the set point.
5. A heater is supplied by a current controlled by the size of the error signal measured on the null meter and by the set point.

The CTI Cryocooler , with the TCU (in this case mod. DTC-500SP), can maintain a very stable temperature. The temperature drift at temperatures less than 50K was measured to be less than 0.01K, see M.Anderson thesis.



Block Diagram 3.1: Block diagram of DTC-500SP Temperature Controller.

3.4.2 DILUTION REFRIGERATOR

The temperature was monitored at various stages on the insert: at the still, at the He pot and at the sample. It was essential to continuously monitor T as at low temperatures the sample measurements could introduce heat to the system. In practise it was found that at about 50mK the conductance measurement did not affect T, but the capacitance measurement resulted in a variation in T of +/-5mK at the mixing chamber level. However, because of the rapid change in measured resistance, this was ascribed to R.F. pick-up on the resistor and was thereafter ignored.

Following the structure of the previous section the refrigerator temperature sensors will be discussed, and then the temperature control unit.

(a) Temperature sensors

The temperature sensors used for the fridge were Matsushita carbon resistors, calibrated below 50mK by nuclear orientation thermometry. A pre-calibrated germanium resistor was also used to calibrate the carbon resistor above 0.1K.

(b) Temperature control system

The system used to control and monitor the temperature of the refrigerator is essentially the same as for the previous cryogenic systems described. However some features were slightly different, the main difference being that the temperature control unit consisted of four separate constituents rather than being incorporated in one single unit.

The system has four main constituents: the sensors, as previously described, an a.c. resitance bridge, a heater, a power supply to the heater, and finally the main temperature control unit. The function of each of these is fairly self explanatory. The first two constituents, the sensors and the a.c. resistance bridge, were used to monitor the temperature. An a.c. resistance bridge was used to increase the sensitivity of the measurement of the temperature sensors and, as the voltages required are very low to limit the dissipation of heat into the refrigerator (the Oxford instrument bridge used dissipated only 1 picowatt of power in operation). The heater was used to heat the sample, and was driven by the power supply (it was possible to heat the system at various stages along the insert). The temperature control unit controlled the temperature. To achieve a temperature above the base temperature the procedure used was as follows: firstly, the a.c. resistance bridge was set to the resistance corresponding to the required temperature, then the power supply was set to a reasonable level and current was driven through the heater, thus increasing the temperature. To stabilise the temperature the temperature control unit was used in

conjunction with the a.c. resitance bridge and the sensors. The method for achieving this was identical to that outlined for the Lakeshore Cryogenic temperature control unit.

3.5 MAGNET

The magnet available for use with the fridge was an Oxford Instuments Cryomag. This magnet consisted of a number of concentric solenoid sections together with compensating coils. Each section was wound from multifilamentary superconducting wire formed from niobium titanium (NbTi) filaments surrounded by a stabilising matrix of copper. To produce fields above 11T an inner coil wound from niobium-tin was installed. A superconducting magnet, such as this, can be considered as a pure inductance.

A protection circuit was provided to counter the effect of possible problems in the event of a magnet quench, that is the rapid conversion from the superconducting to the normal resistive state. This was once shown to be in good working order!

The power supply used for the magnet was an Oxford PS120-10(120A, 10V), which was specifically designed for energising and de-energising superconducting magnets. The polarity of the current supplied could be varied allowing the magnetic field to be swept in two directions. This supply has an RS232 interface enabling remote computer control.

3.6 MEASUREMENT FACILITIES

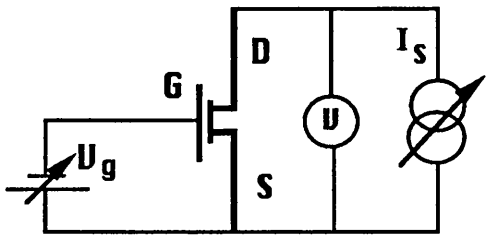
A wide range of measurements were taken in the course of this project. These can be classified in four main groups: conductance, magnetoconductance, capacitance, and magnetocapacitance. The samples under investigation were basically FET like structures so all electron transport was measured as a function of gate voltage. Each type of measurement will be discussed in some detail.

3.6.1 CONDUCTANCE MEASUREMENT FACILITIES

The conductance of the multiple wire samples was measured using various techniques, initially using a d.c. source as a supply, then, in the later stages of the project, using a low frequency a.c. supply from a lock-in amplifier. The conductance of these devices was measured between the large source drain contacts as a function of the bias applied to the gate.

(a) D.C conductance

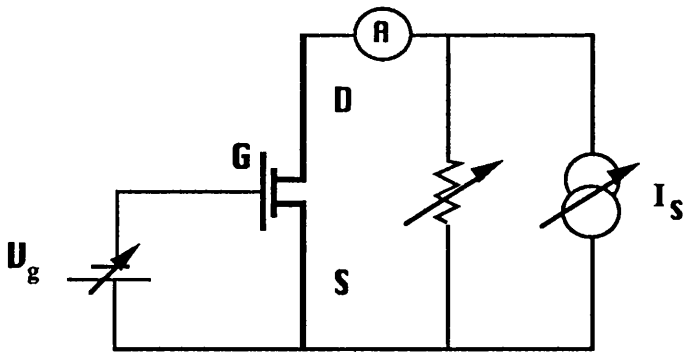
The system used for initial measurements is illustrated, below, in Circuit 3.1.



Circuit 3.1 for the measurement of 2-terminal conductance as a function of gate bias, with a constant current source

This system was used to measure the characteristics of three terminal, FET like, devices. The arrangement consists of a Keithley 230 programmable voltage source, a Keithley digital voltmeter and a Keithley 240 programmable current source. These were all on an IEEE bus controlled by a Sinclair QL computer.

Initially the system was set up to supply a constant current and measure the resulting voltage dropped across the channel. However, in certain limits, the type of measurements taken required the measurement of regions of very low conductance, typically 10^{-7}S and it was found that large voltages were developed in the high resistance range. This was found to be an undesirable situation as it increased the probability of carrier trapping and hot electron effects. Therefore, to avoid excessive voltages being applied across the sample, it was necessary to convert the current source to a voltage source and thereafter supply a constant voltage and measure the current. This was achieved by putting resistors across the terminals of the current source, and measuring the current with a Keithley ammeter, see Circuit 3.2



Circuit 3.2 for the measurement of 2-terminal conductance as a function of gate bias, with a constant voltage supply.

The software used to control this measurement system was written to allow all the measurement parameters to be entered from the keyboard. The required information included the source-drain voltage/current, the voltage step on the gate, and the number of such steps. Having entered this information the p.c. controlled the automatic sweep of the preset conditions and the measurement of the source/drain current/voltage.

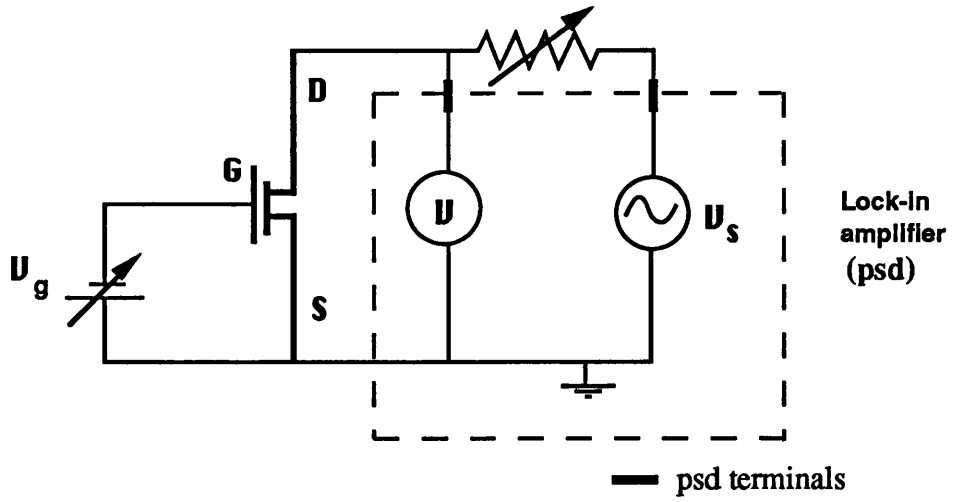
(b) A.C. conductance

Both three and five terminal measurements were used for the measurement of a.c. characteristics. The three terminal measurements involved the two terminal measurement of channel conductance as a function of gate bias, and the five terminal measurements, used in the later stages of the project, were taken using a four terminal technique for measuring the channel conductance, again, as a function of gate bias.

For most of the experiments conducted lock-in amplifiers were used for the measurement of sample conductance. A lock-in amplifier works by measuring the required signal at a specified reference frequency. The input signal is amplified and applied to a phase sensitive detector operated at the reference frequency. The frequency translation effects of the phase sensitive detector result in an output that includes a value from the amplitude of the signal of interest as well as fluctuating components that may be due to noise and interference effects. The a.c. resulting from noise is then reduced, to any arbitrary degree, by low pass filters under the control of the user. The lock-in amplifier used in the course of this project was a Princeton lock-in amplifier, model 5210. In this there are two phase sensitive detectors working in quadrature.

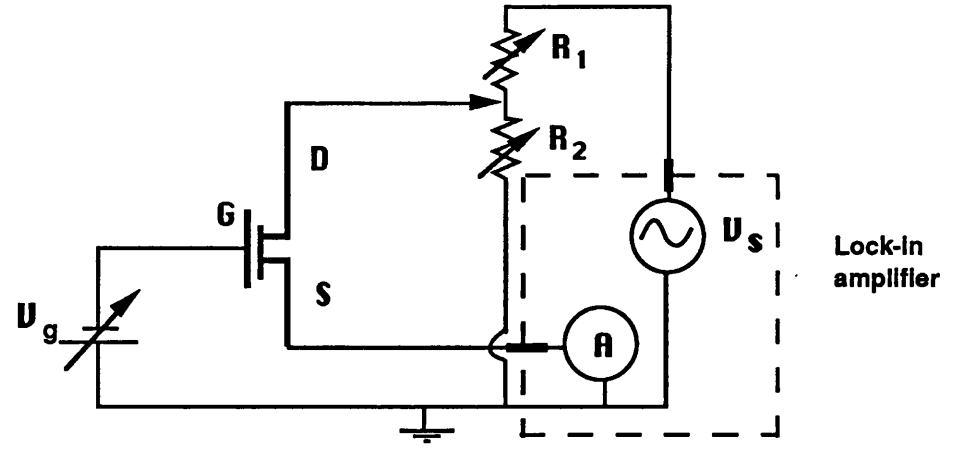
There are several advantages of using a.c. lock-in techniques to measure the conductance of the multiple wire samples. The first of these is the reduction of the 1/f noise in the signal, which can be achieved using a 'trial and error' selection of reference frequency. The second advantage is that in the d.c. measurement of conductance the measurement was in some instances adversely affected by d.c. leakage from the gate. Direct measurement of d.c. signals are often affected in this way by drift in the signal. By modulating the signal at a frequency that is also fed into the lock-in amplifier as a reference frequency, d.c drift is eliminated and a very high rejection of interfering frequencies is achieved.

For three terminal measurements the ac channel conductance was measured using the Princeton lock-in amplifier described, with the dc gate voltage supplied by a Keithley 236 Source Measuring Unit. This was controlled by a Elonex PCXT. As with the d.c. conductance measurements, two options were available for measuring the conductance, either with a constant voltage supply, or with a constant current supply. Circuit 3.3 shows the circuit used for measuring with a constant current.



Circuit 3.3 for the measurement of 2-terminal a.c. conductance, as a function of gate bias, using a constant current supply.

The lock-in amplifier has an internal a.c. voltage supply which was converted to a contant current supply by putting a large resistance in series with the voltage supply. The resistance used was typically 10MΩ. Circuit 3.4 shows the circuit used for measuring with a constant voltage.

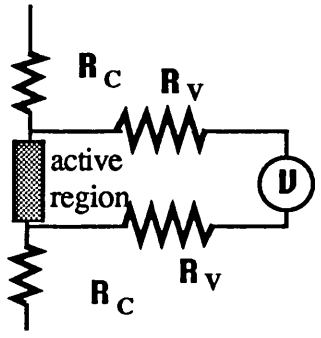


Circuit 3.4 for the measurement of 2-terminal a.c. conductance, as a function of gate bias, with a constant voltage source.

In this circuit the voltage supplied was determined by the ratio of the resistances in the potential divider. This circuit was used to provide a suitably low, and stable, voltage supply to the sample, with the current measured by the feedback ammeter integral to the amplifier. This is not a suitable way of measuring sample conductance in the high conductance limit where lead resistances are significant and currents are too high; for this the current drive circuit should be used.

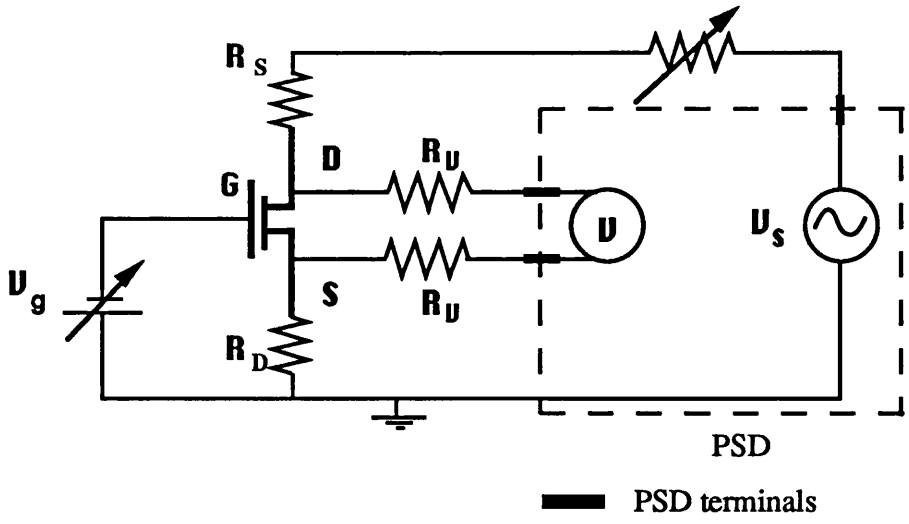
The software driving these systems shared similar features; setting of measurement parameters from the keyboard, such as driving current/voltage, frequency, sweep rate, and delay times, automatic sweep of preset gate biases and voltage/current measurement at each gate bias. The data was saved as conductance values, calculated from the measured voltage/current data and the driving current/voltage.

For five terminal measurements the arrangement used was essentially the same as for the three terminal system when set up for the current drive arrangement, except that the side terminals were used to measure the voltage drop across the channel, and the source drain contacts were used to drive the current. The advantage of using this type of system was that effects due to contact resistance were eliminated. Justification for this can be obtained by examining Circuit 3.5. If the volt meter has a very high resistance, relative to the contact resistances, then little current flows through the voltage probes or the volt meter, so the voltage drop across the active region is measured and the effects of contact resistance are avoided.



Circuit 3.5 for the measurement of 4-terminal resistance.

The circuit diagram for the four terminal conductance measurement is shown in Circuit 3.6. In this the contact resistances are explicity defined, with R_S and R_D representing the contact resistance for the source and drain respectively, and R_V representing the resistance of the side voltage probes, to illustrate further the advantages of using a four terminal configuration.



Circuit 3.6 for the measurement of 4-terminal conductance using a constant current supply

3.6.2 MAGNETOCONDUCTANCE

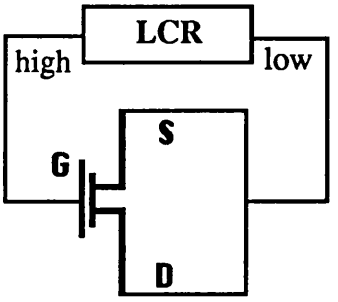
The sample magnetoconductance was measured using four terminal current drive techniques, as illustrated above in Circuit 3.6. There were two reasons for using a four terminal measurement. The first of these is that two terminal magnetoconductance measurements of 2DEGs is dominated by electrons moving in extended edge states. This is a fundamental effect, and was seen several times in the course of this project, but gives no information on the electronic structure of the wires. This was discussed briefly in chapter 1, section 1.5.3 (b). The second reason is that the effects of contact resistance and the series resistance of the ungated channel region are minimsed.

For the measurement of four terminal sample magnetoconductance the magnetic field was swept at a preset rate and measured at regular intervals, and the conductance was measured by supplying a constant current and measuring the resultant voltage dropped across the channel. As with the four terminal current drive measurement described previously, the constant current was produced by connecting a high resistance, typically 10MΩ, in series with the constant voltage supplied by the lock-in amplifier. The system was controlled by a Viglen GENIE 11 PCAT, but did not incorporate a gate bias facility so gate voltages were applied manually using the Keithley 368 Source Measurement Unit.

The software for the four terminal conductance as a function of magnetic field measurements was developed by E.Skuras. The program controlled the measurement of the sample voltage and magnetic field and displayed the data on screen as it was accumulated.

3.6.3 CAPACITANCE MEASUREMENTS

The sample capacitance was measured using a Hewlet Packard LCR meter, which contains an internal dc bias allowing the gate-source capacitance to be measured as a function of gate voltage. The circuit used is shown in Circuit 3.7. The measurement was two terminal in nature with a high frequency oscillator signal, superimposed on a d.c. bias, applied to the gate and used to measure the capacitance between the gate and the source contacts. It should be noted that in general the source and drain contacts were connected together and taken to the low terminal. The parallel conductance was also measured.



Circuit 3.7 for measurement of capacitance characteristics

The meter was on an IEEE bus driven by a Sinclair QL computer. Measurement parameters such as oscillator frequency, oscillator voltage level, time between successive measurements, number of averages at each measurement point, gate bias increment, and number of increments were all entered from the keyboard. The program was arranged to measure the sample capacitance and parallel conductance, as a function of gate bias at the preset values.

3.6.4 MAGNETOCAPACITANCE

The magnetocapacitance of the samples was measured using a combination of the techniques already described. The LCR meter was used for the measurement of the capacitance and the parallel conductance. The circuit diagram is essentially the same as in the previous section, except that the system was controlled from the Viglen-genie.

The program controlling the measurements set the oscillator frequency, the oscillator level, the gate bias (in this case the bias was held constant), the measurement rate, the number of averages per point, and the number of measurements required. As

before the magnetic field sweep rate was set manually. The data was again plotted as it was being collected.

3.6.5 EARTHING

For the cryocooler and the He_4 insert there was no problem due to earthing. However the refrigerator was found to be floating at an unknown potential, which caused problems, particularly with the capacitance measurements. This was overcome by connecting the refrigerator and insert to the screened wall surrounding the system. It should be noted that this may not be sufficient for other applications.

3.7 REFERENCES

M. Anderson, PhD. thesis, Glasgow 1989.

G.K. White, "Experimental Techniques in Low Temperature Physics.", Oxford Press, **1968.**

Nunes and Earle, Chapter 2, "Characterisation of Semiconductors", edited by R.A. Stradling, and P.C. Klipstein, Adam Hilger, Bristol, **1990.**

CHAPTER FOUR

CAPACITANCE AND CONDUCTANCE DATA

4.1 INTRODUCTION

In this chapter sample characteristics in the absence of a magnetic field will be discussed. The discussion will begin with a section illustrating and discussing the general shape and temperature dependence of C-V and G-V characteristics. Thereafter the sections will be somewhat more specific, relating to particular samples and materials.

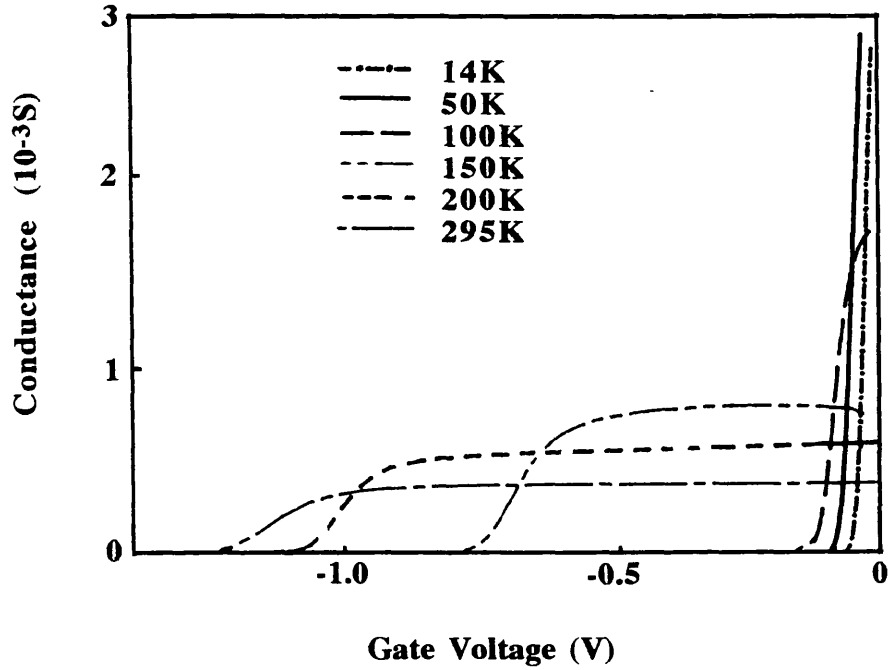
4.2 TEMPERATURE DEPENDENCE OF C-V AND G-V CHARACTERISTICS

The initial measurements taken on the multiple wire samples were those of capacitance, C, and channel conductance, G, both as a function of gate bias, V_g, and as a function of temperature. These measurements were taken in the closed circuit cryocooler in order that data could be taken in the range 300K to 12K. The capacitance data was measured using the LCR - meter, which measured both the capacitance and the equivalent parallel conductance.

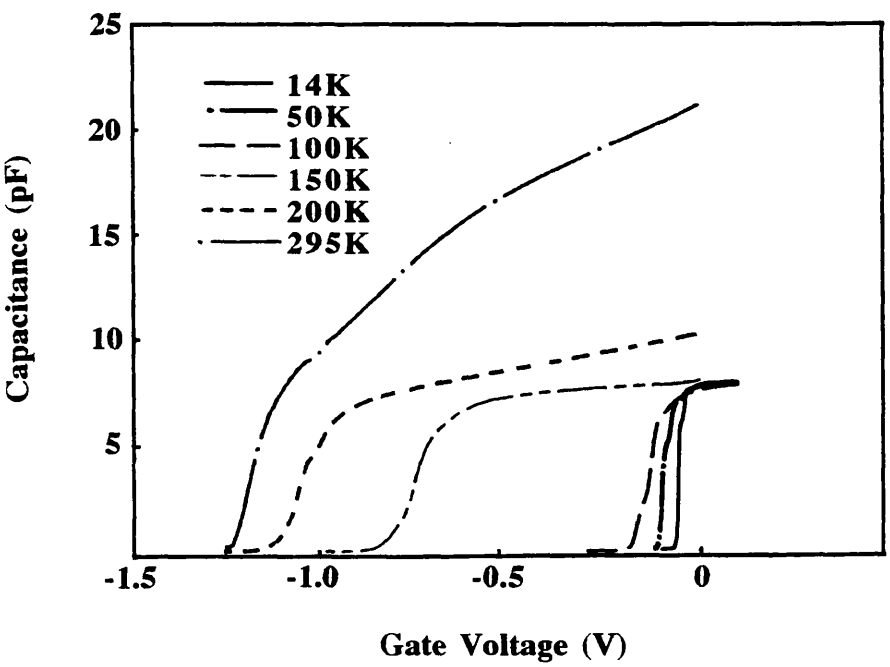
Typical curves for an FET are shown in Graphs 4.1 (a) and (b), with (a) showing the G-V_g characteristic as a function of temperature, and (b) showing the corresponding C-V_g characteristic. Typical curves for the multiple wire samples are shown in Graphs 4.2 (a) and (b).

The most striking feature of both sets of curves is the shift in the cut-off voltage, V_c, for the FET samples and V_c', for the wire samples. If it can be assumed that the measurement is sensing all the charge in the system, then the change in area under the C-V_g characteristics represents the amount of charge lost, so the shift in the threshold voltage represents a dramatic loss of charge.

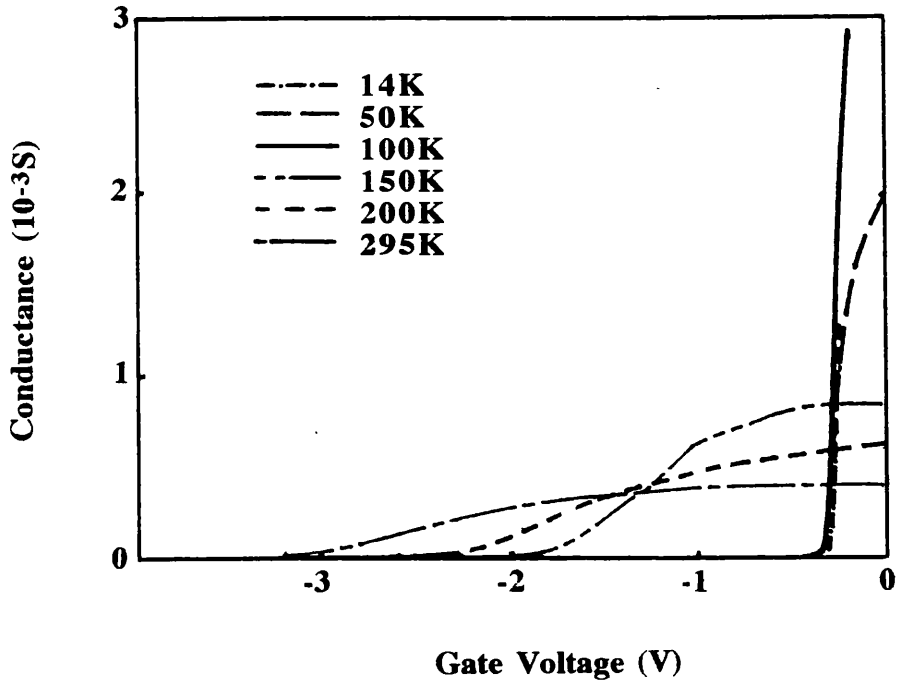
The threshold shift at low temperatures was evident to varying degrees in all of the samples measured and was attributed to carrier trapping in DX centres in the doped



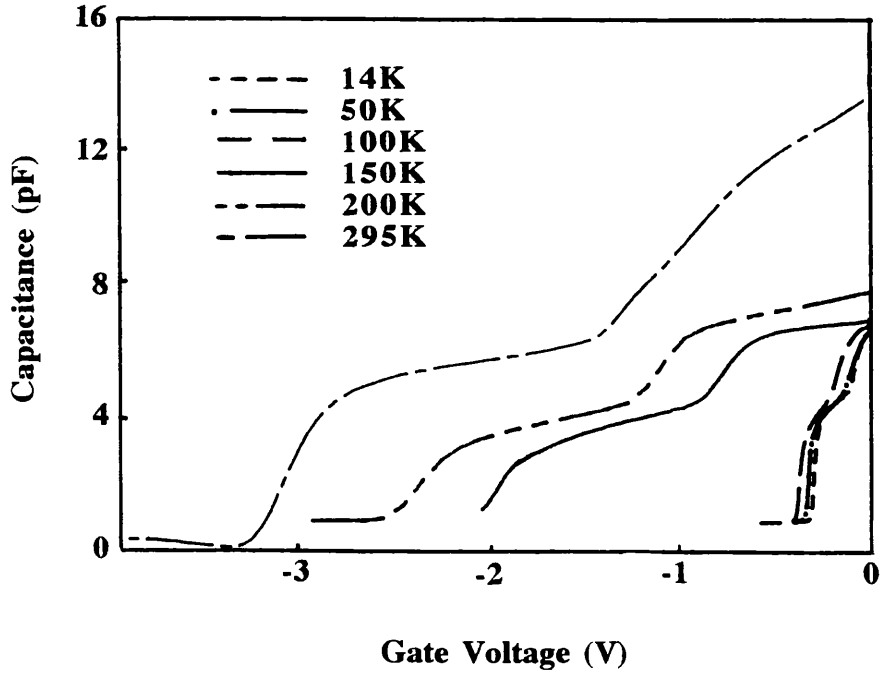
Graph 4.1(a): Conductance characteristics as a function of temperature for A21618(FET).



Graph 4.1(b): Capacitance characteristics as a function of temperature for A21618(FET).



Graph 4.2(a): Conductance characteristics as a function of temperature for A21611(WIRE).

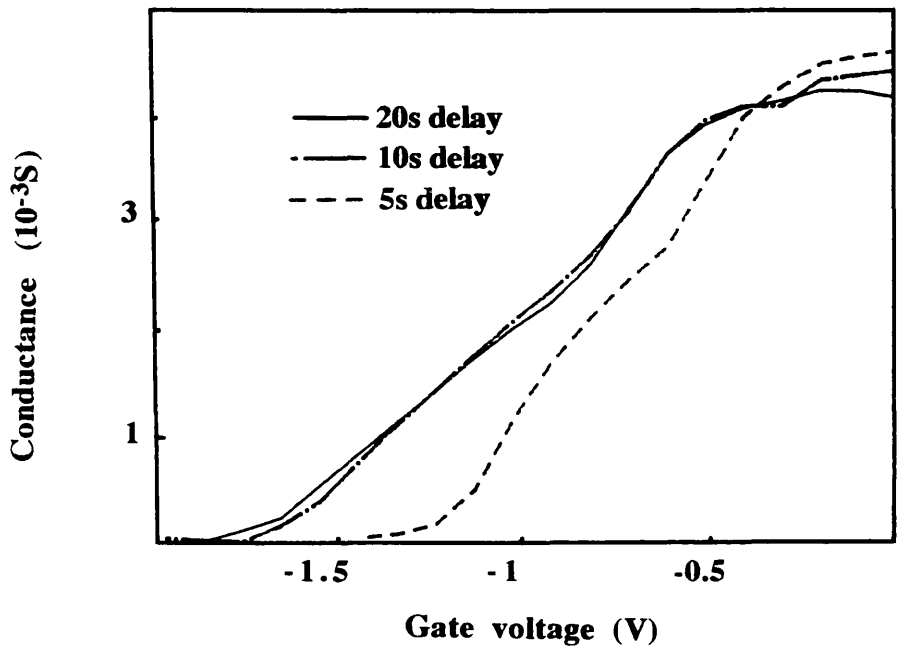


Graph 4.2(b): Capacitance characteristics as a function of temperature for A21611(WIRE).

AlGaAs region. DX centres are widely accepted to be ground states of isolated substitutional donors in distorted configurations, which are stabilized by trapping two electrons. The DX centre has an energy barrier to both electron capture and electron emission. As the temperature decreases the energy barrier for emission from the trap increases, so the probability for the release of electrons from traps decreases, and the loss of the charge occurs. This process of carrier trapping is limited by the simultaneously increasing magnitude of the electron capture barrier energy which prevents the capture of all the free charge in the system. The trapping and de-trapping of charge in DX centres is a time and temperature dependent process, in which electrons may be permanently or temporarily trapped, depending on the level of thermal excitation and the measurement frequency. For a full description of DX centres refer to Mooney 1989 and 1991.

The experimental data can be divided into three categories: high, low and intermediate temperatures. At high temperatures, above or around 200K, the threshold voltage was found to vary slowly, implying that the thermal energy in this limit was higher than the emission energy barrier, and, hence, the capture lifetime was low, allowing the continual capture and release of charge from the DX centres. At low temperatures, less than 50K, the threshold voltage was also observed to change slowly with temperature, suggesting that in this limit the thermal energy was significantly lower than the barrier energy for both the capture and release of electrons from DX centres, resulting in a high lifetime for electrons in traps and at the same time a low probability of free electrons being captured. It was at intermediate temperatures that the threshold voltage was observed to shift most dramatically implying that, in this range, the thermal energy was of a similar magnitude to the trap emission and capture energies. In theory, it is in this limit that the rate at which the measurements are taken should be most significant.

The model outlined above was tested by varying the time between measurements at high, low, and intermediate temperatures. At high and low temperatures it was found that varying the time delay between successive voltage increments on the gate had no effect on the threshold voltage. However, at an intermediate temperature the threshold voltage was found to be affected by the time delay between measurements. The temperature selected was 80K, and the data taken is shown in Graph 4.3, from which it can be seen that as the delay between measurements is increased from 5s to 10s between measurements the cut-off voltage moves to more negative voltages. At delays longer than 10s it was found that there was no further shift in the threshold voltage. This indicates the validity of the hypothesis that, in this intermediate temperature range, the emission of electrons is time dependent.



Graph 4.3: Conductance characteristics for A21668 taken with time delay between measurements 5s, 10s, and 20s, at 80K.

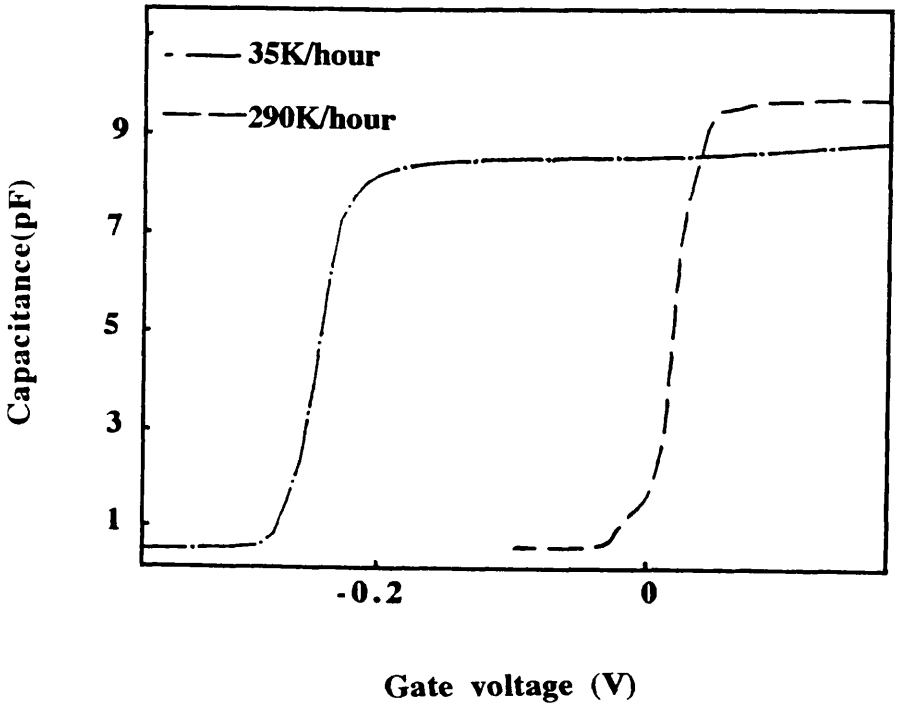
The significance of this model of DX centre electron trapping for the later measurements is that at low temperatures DX centres are effectively passive, the energy barrier for electron capture being so high that the probability of trapping is very low, and the barrier to electron emission from the traps again being high so that it is not possible to communicate with charge trapped in DX centres. Therefore, a state of equilibrium is reached, in which electrons can be neither emitted nor captured by traps. Thus, any changes in the capacitance can be unambiguously related to changes in the amount of charge in the conduction band, whether in the doped AlGaAs layer, or in the 2DEG.

It is difficult to quantify the causes and effects of carrier trapping in the AlGaAs. However, it is useful to note some experimental observations on the factors contributing to the magnitude of the shift. The shift in the threshold voltage seen in the C-V_g and G-V_g characteristics seems, over a wide range of experiments, to occur at about 150K, which suggests that the activation energy for the trapping/detrapping process occurs at the equivalent energy. The magnitude of the shift was observed to be strongly dependent on the rate at which the sample was cooled, particularly at or around the trap activation temperature 150K-100K. It was found that the higher the cooling rate, the more charge was trapped. This is illustrated in Graph 4.4. For simplicity, an FET was chosen to illustrate this effect as the threshold voltage of the wires is dependent on the width of the wires as well as the cooling conditions. From this it can be seen that the sample with the threshold voltage at about zero volts was cooled from 295K to 4.2K in 1 hour, whereas the sample showing a cut-off at -0.3V was cooled slowly from 295K to 15K over a period of eight hours.

In the closed circuit cryocooler it was easy to control the rate of cooling. However, in both the dilution refrigerator and He_4 insert there was no specific mechanism for limiting the cooling rate from room temperature, although efforts were taken to minimise the rate, particularly at the nitrogen precooling stage.

4.3 GENERAL SHAPE OF FET AND WIRE SAMPLE CAPACITANCE CHARACTERISTICS

As is well known to researchers working with nanostructures fabricated on GaAs/AlGaAs heterostructures, device characteristics at low temperatures are highly dependent on the history of the sample, mainly as a result of the trapping phenomena discussed above. This makes the direct comparison of samples measured at different times and in different systems very difficult. However, some features of the capacitance curves were common to all of the samples measured.



Graph 4.4: Capacitance characteristics for two FET samples, illustrating the effect of the sample cooling rate.

Typical curves for an FET and a wire sample are shown in Graph 4.5. This sample was fabricated on A216 material (material details are given in Table 2.2), the sample numbers for the wire and FET samples are A21611, and A21618, respectively. For A21611 the wire width was 580nm and the wire separation was 620nm. The wires are formed when the regions between the resist strips are fully depleted. Graph 4.5 illustrates clearly the voltage range in which the wires are formed. The cut-off voltage for the FET sample is at -0.4V, so the transition from the full 2DEG to the isolated wires occurs in this particular sample at approximately -0.40V.

4.4 LOW TEMPERATURE CAPACITANCE CHARACTERISTICS

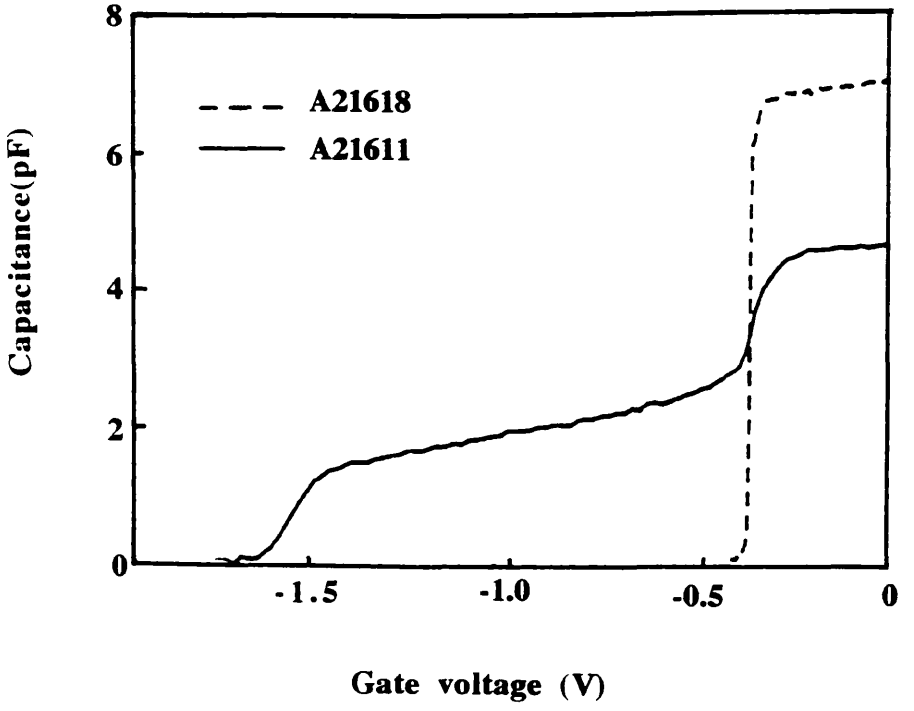
The characteristics shown in Graph 4.5 are typical curves, which show features evident in the majority of samples . However, some features were peculiar to specific samples and materials. In the following sections some of the capacitance data taken will be presented; firstly for A216 samples, and then for A425 samples. This is complemented by an attempt to explain any features of the characteristics.

Firstly, it is necessary to discuss the measurement conditions and the relative effects of noise with respect to the capacitance measurements.

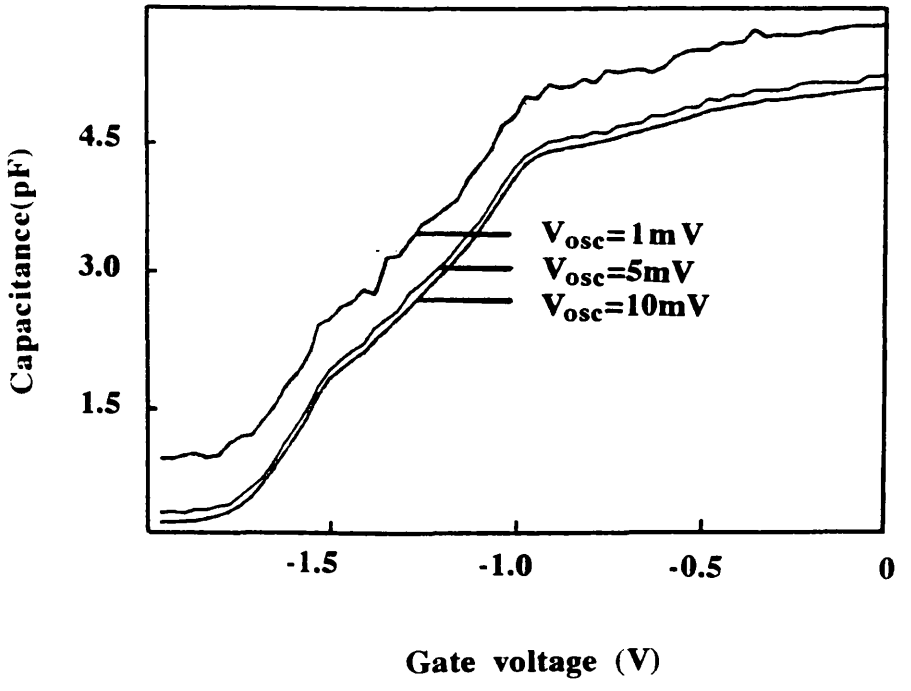
4.4.1 MEASUREMENT CONDITIONS AND EFFECTS OF NOISE AT LOW TEMPERATURES

The main variables in the measurement of the capacitance were the a.c. oscillator voltage level and its frequency; also varied were the time delay between the measurements at each point, the voltage increment on the gate, and the number of measurements over which the data was averaged at each gate bias. At the time some of these measurements were taken, the noise level in the capacitance measurements presented a problem for samples measured in the dilution refrigerator. Earthing the refrigerator to the screened room removed the noise problem.

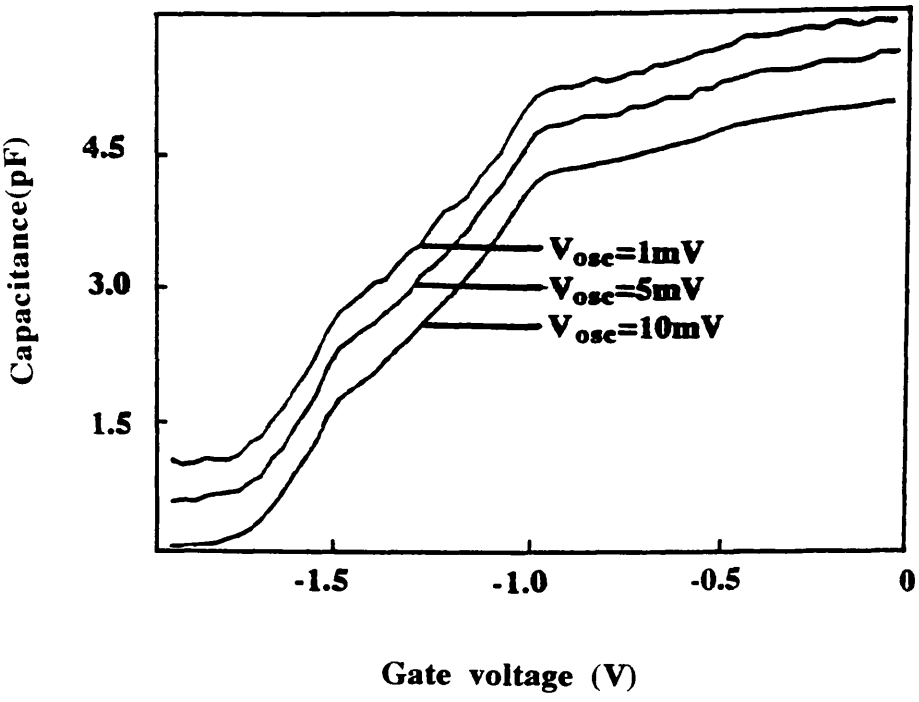
Several experiments were conducted to optimise the capacitance measurement conditions. The capacitance was measured as a function of frequency and a.c. voltage level, with each measurement averaged over a sample size of 10 separate measurements, which was effectively an average over 40 on the 'high resolution' mode as the meter internally averaged over four measurements. Typical results are shown in Graphs 4.6 (a)-(c) for the sample A42529 (a wire sample which will be discussed more fully later). Graph 4.6(a) shows the capacitance measured at a frequency of 10kHz at oscillator levels of 1mV, 5mV and 10mV; (b) shows the



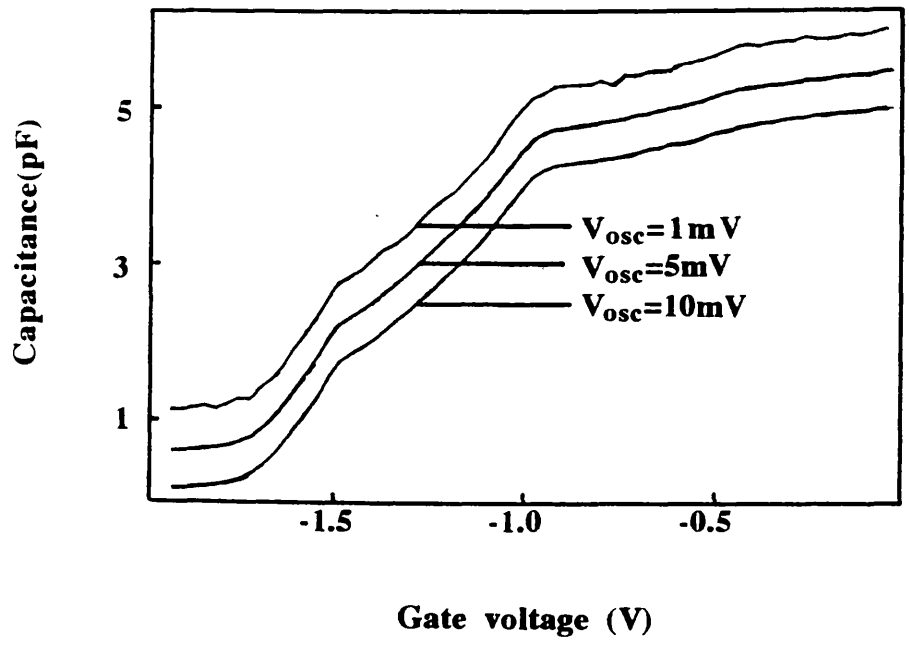
Graph 4.5: A21611 and A21618 capacitance characteristics at 80mK.



Graph 4.6(a): A42529, capacitance characteristics at 10kHz as a function of oscillator voltage level.



Graph 4.6(b): A42529, capacitance characteristics at 20kHz as a function of oscillator voltage level.



Graph 4.6(c): A42529, capacitance characteristics at 40kHz as a function of oscillator level.

characteristics measured at 20kHz, and (c) shows those measured at 40kHz. The characteristics measured at 20kHz and 40kHz have been offset in the y-axis for clarity. The characteristics measured at 10kHz were not artificially offset.

From the graphs it can be seen that at all frequencies the characteristics measured at an oscillator level of 1mV were very noisy. At 10kHz and 20kHz the characteristics measured at 5mV were equally noisy, but at 10mV the noise level was estimated to be tolerable. At 40kHz the data taken at both 5mV and 10mV was found to be relatively noise free. At 10kHz and 20kHz the capacitance offset was found to be dependent on the oscillator voltage level, although the shape of the characteristics was the same; this can easily be attributed to the input capacitance of the measurement system. However, at 40kHz the magnitude of the capacitance showed no such dependence on the magnitude of the a.c. signal.

The conclusion from this data was that, if the frequency dependence of the capacitance curves was to be investigated, it was necessary to measure at 10mV in order to keep the noise level within tolerable limits. This caused some concern initially as 10mV was thought to be too high, as the sub-band separations for the samples measured were estimated to be in the range 30mV-5mV, which is of the same order as the oscillator level. However, the excellent data taken by Smith et al, 1987, displaying evidence of confinement effects was also measured at 10mV (private communication).

4.4.2 LOW TEMPERATURE CAPACITANCE DATA FOR A216 SAMPLES

A216 was the more extensively investigated of the two materials used in the course of this project. Capacitance characteristics of several samples will be presented to highlight particular features. The effects of frequency dependence, illumination with HeNe radiation and illumination with light from a GaAs LED will also be discussed.

In the following sections, unless otherwise stated the capacitance data presented is measured at 100kHz and an oscillator level of 10mV.

(a) Presentation of capacitance data taken on A216 samples A2169/10

A2169 and A21610 were among the first samples measured, the former being a wire sample and the latter an FET sample. Unfortunately the dimensions for the wire sample are not known. However the characteristics measured for both samples display effects which, it was felt, would be instructive to present. These samples were measured in the closed circuit system, in the dark state and under illumination with

HeNe radiation. The dark state characteristics at 15K are given in Graph 4.7. Both of the characteristics were measured from +0.4V to the cut-off voltage, which resulted in the observation of an increase in both the FET and the wire sample capacitance at about +0.15V. It is thought that at this voltage the conduction band in the AlGaAs layer is pulled below the Fermi level, allowing electrons to populate regions of the AlGaAs. It should be noted that the magnitude of this step is lower than expected for charge in the AlGaAs - this can be readily attributed to the finite time required to transfer electrons from the AlGaAs to the 2DEG. The other feature of interest is the step in the wire characteristic at about -0.3V, not evident in the characteristic presented as being 'standard'.

A21611/18

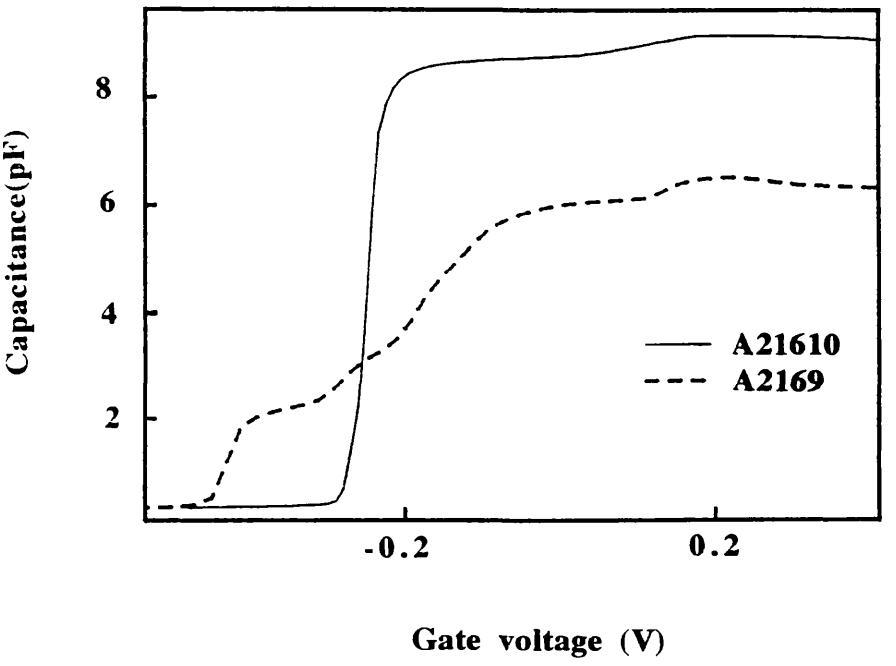
A21611 was a wire sample, with wire widths of 580nm and wire separations of 620nm, and A21618 was an FET control sample - both of these samples were five terminal in nature. The samples were measured in both the closed circuit system and the dilution refrigerator. The capacitance characteristics, taken at 15K, of the wire and the FET samples are plotted in Graph 4.8(a). Although the wire sample has a cut-off voltage similar to that of A2169, the capacitance characteristic does not display the 'step' seen in the wire region of A2169. The FET displays a peak in the capacitance before the full planar cut-off, which was seen in several samples.

The characteristics measured in the dilution refrigerator at 40mK are shown in Graph 4.8(b). The noise level on the capacitance characteristic was very high at this stage as the earthing problems with the refrigerator had not been overcome.

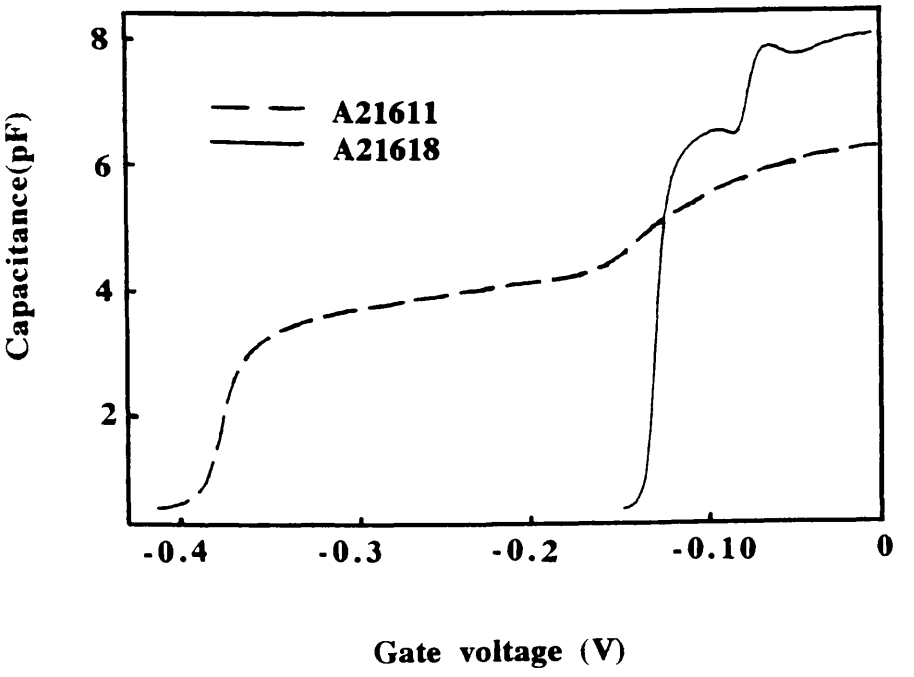
It is interesting to note the differences between 4.8 (a) and (b) as these illustrate how dependent characteristics are on the specific thermal history of the sample, although the relative voltage widths of the FET and wire regions remain constant.

A21614/15

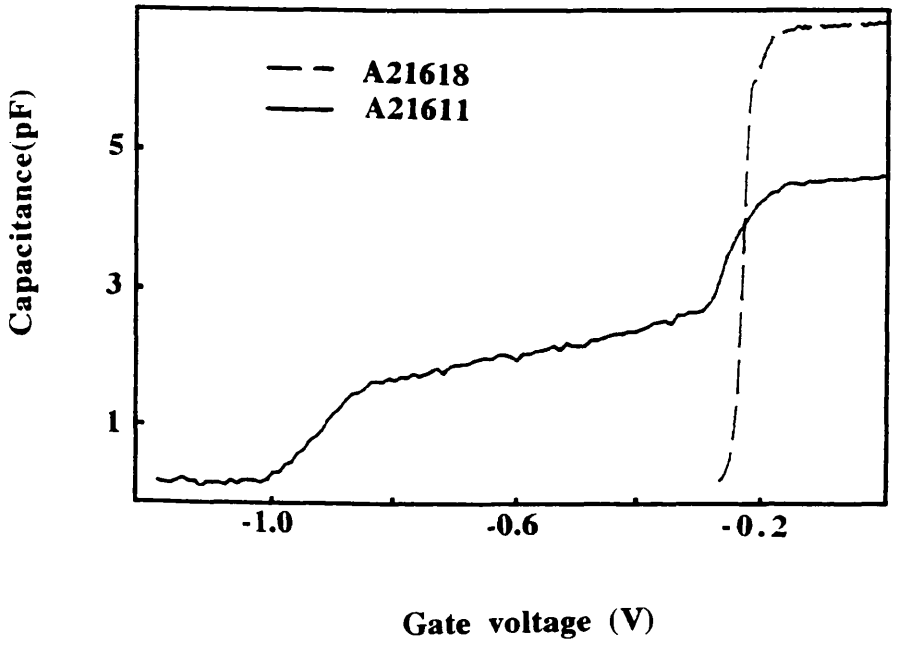
A21614 was a wire sample with a wire width of 470nm and separation of 470nm, and A21615 was an FET control. Both samples were five terminal devices, and were measured in the refrigerator. The capacitance characteristics are shown in Graph 4.9. There are two obvious features displayed in these curves. Firstly the FET cut-off point is very close to 0V at -0.08V, and, secondly, the wire characteristic exhibits an additional step in the capacitance in the voltage range -0.5V to -0.7V. This is similar to the shape of the characteristics for A2169, although somewhat more pronounced, with both samples displaying FET cut-off points close to 0V.



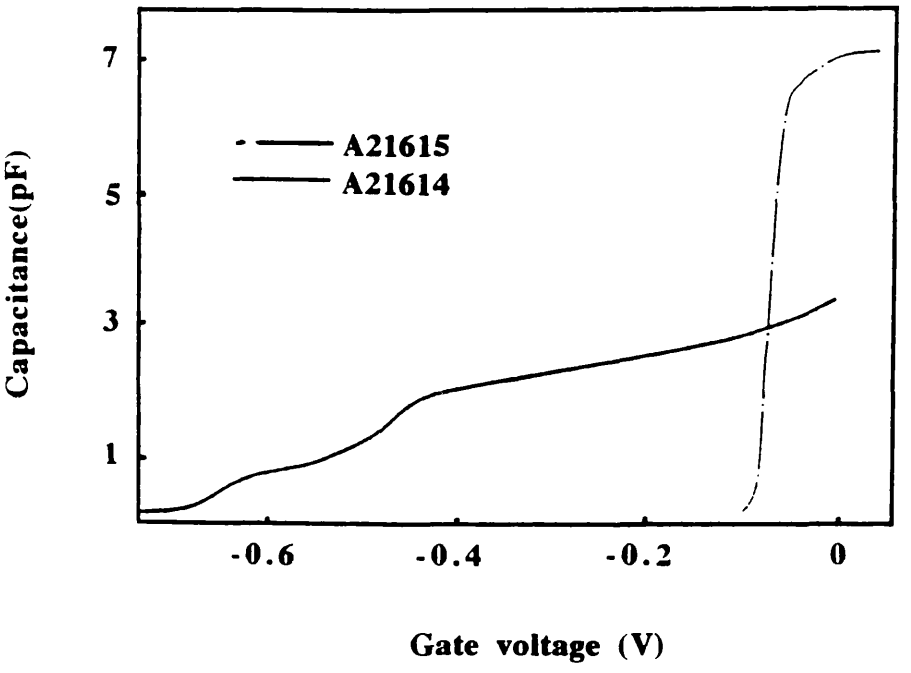
Graph 4.7: Capacitance characteristics for A2169 (wire) and A21610 (FET), at 15K.



Graph 4.8(a): Capacitance characteristics for A21611, a wire sample, and A21618, an FET sample, at 15K.



Graph 4.8(b): Capacitance characteristics for A21611, a wire sample, and A21618, an FET sample, at 80mK.



Graph 4.9: Capacitance characteristics for A21614, a wire sample, and A21615, an FET sample, at 50mK.

(b) Effects of illumination with HeNe radiation and light from the GaAs LED

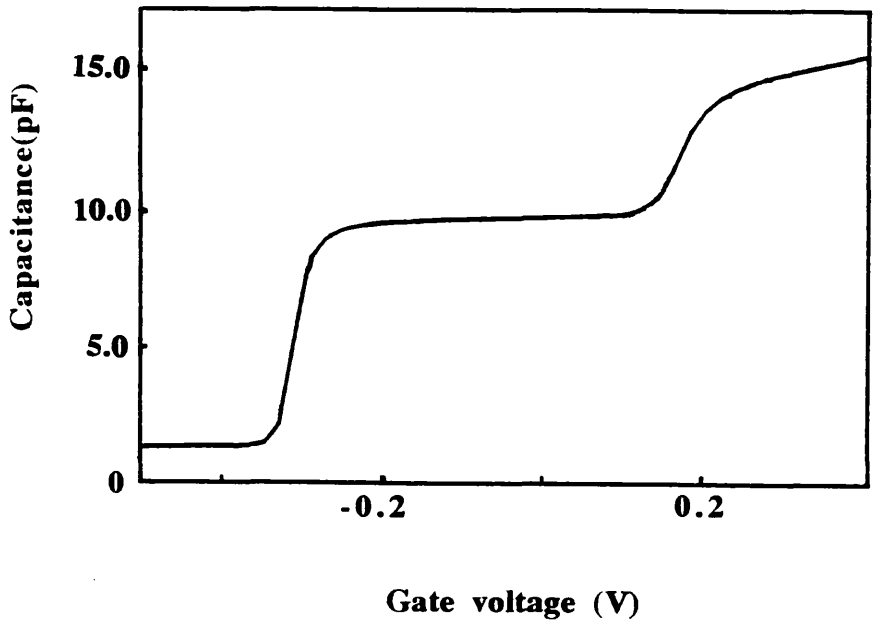
Several of the samples measured in the closed circuit system were illuminated with HeNe radiation. A21611 and A21610 were both measured in the dark and illuminated states. The capacitance characteristics for the samples when under illumination are shown in Graphs 4.10(a), for A21610, and 4.10(b), for A21611.

Consider firstly the FET sample, A21610, which was illuminated with 1μW of HeNe radiation. From the dark characteristics, Graph 4.7, it can be seen that at +0.15V there is a small increase in the capacitance which was thought to be due to carriers in the conduction band in the AlGaAs layer. The effect of illumination was to increase the magnitude of the capacitance at voltages above +0.15V, suggesting that many electrons were excited into the conduction band in the AlGaAs, and therefore, confirming that the feature at +0.15V in the 'dark' characteristic was indeed the voltage at which electrons start to populate the conduction band in the AlGaAs. The illumination did not significantly affect the FET cut-off voltage, although, a few of the other FETs illuminated did show a small shift in the position of the cut-off.

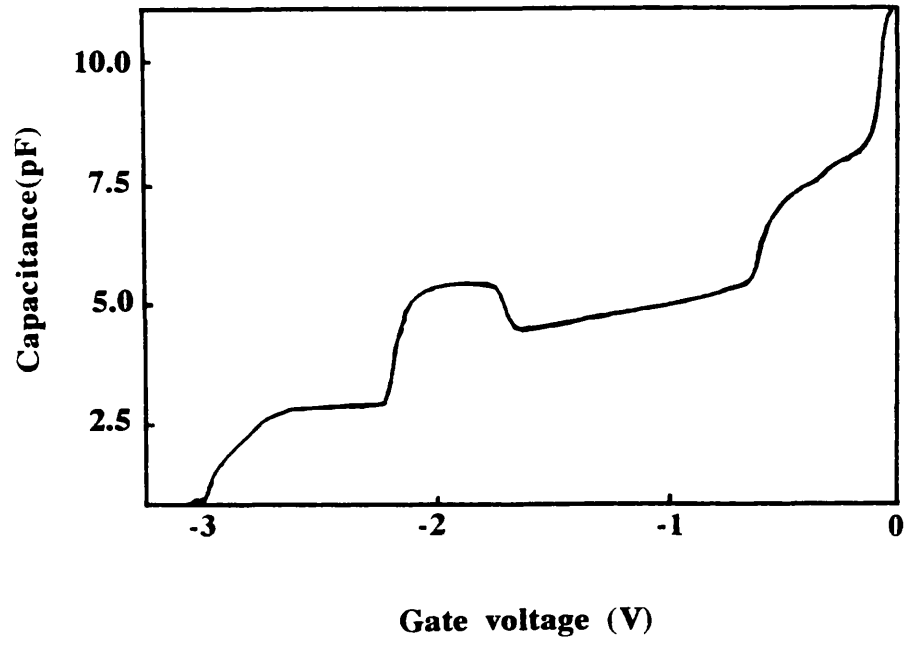
Now consider the wire sample, which was also illuminated with 1μW of HeNe radiation. Comparing Graph 4.8(a) with Graph 4.10(b) it can be seen that the effect of illumination, at this frequency, is dramatic, with the threshold voltage moving from -0.4V to -3V. There are also various new 'bumps' in the characteristic, the most unusual of which occurs at about -1.7V when the capacitance of the sample actually increases as the gate bias is made more negative. The reason for this is not understood.

It is difficult to come to any particular conclusions on these light effects, other than that they were, in general, not particularly beneficial to the system when trying to investigate quantum effects. The wire samples were consistently found to be more sensitive to illumination with HeNe radiation than the FETs.

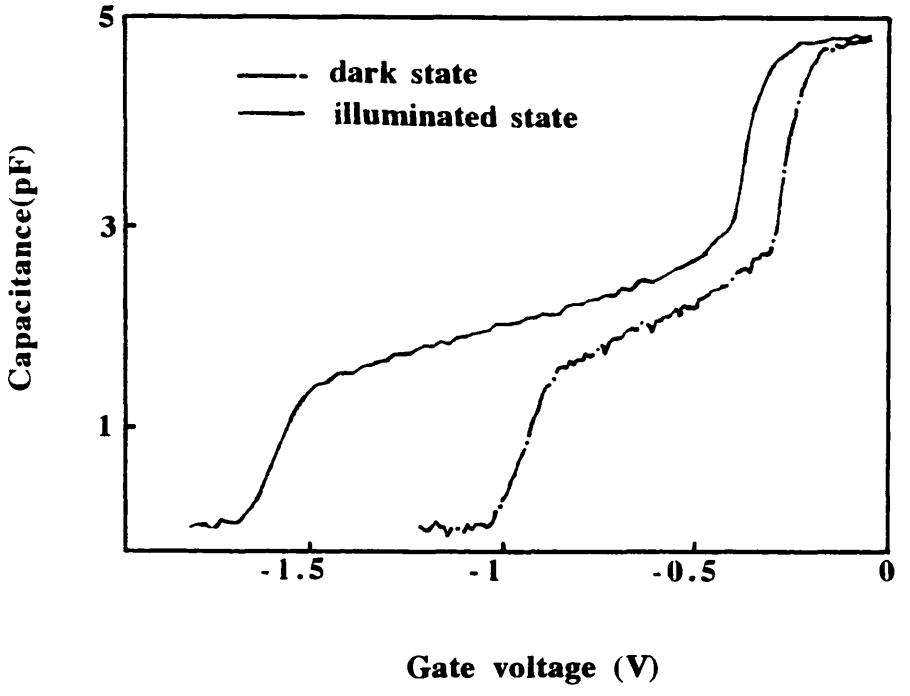
Several of the samples measured in the refrigerator were illuminated with light from a GaAs LED. The effect of this was quite different from that of illumination with HeNe radiation. The characteristics measured in the dark and illuminated state for A21611 are given in Graph 4.11. From this it can be seen that the effect of the GaAs radiation was to effectively extend the wire and FET regions to more negative voltages. The characteristics were otherwise unaffected by the illumination. Unfortunately there was no way of estimating the intensity of the light from the LED, so it is difficult to say if the differences in the effects seen for illumination with HeNe radiation and illumination with radiation from the GaAs LED are merely due to differences in intensity.



Graph 4.10(a): Capacitance characteristic for A21610 (FET) after illumination with 1μW of HeNe radiation at 15K.



Graph 4.10(b): Capacitance characteristic for A21611 (wire) after illumination with 1μW of HeNe radiation at 15K.

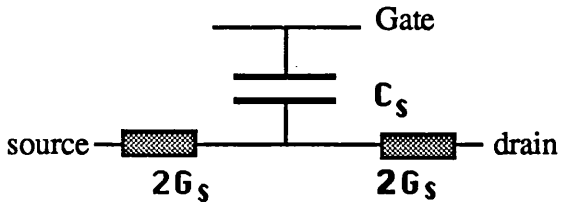


Graph 4.11: Capacitance characteristics for A21611 (wire) before and after illumination with radiation from a GaAs LED at 80mK.

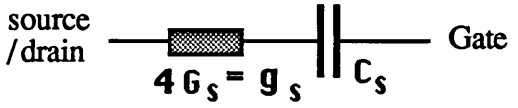
(c) Frequency dependence of A216 samples

The frequency dependence of the characteristics of four samples will be discussed. The first two of these are A21611, a wire sample, and A21618, an FET, which were measured at 15K, and the second two are A21614, a wire sample, and A21615, an FET, which were measured extensively at 50mK.

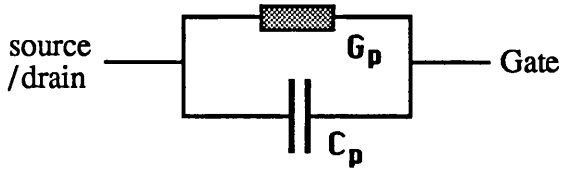
The characteristics for the samples measured at 15K are given in Graphs 4.12 (a) and (b), from which it can be seen that there are two effects evident. The first effect is a constant offset in the capacitance which increases as the frequency decreases, and can be attributed to the input capacitance of the measurement system and, the second is a slight frequency dependence in the cut-off region, which can be explained by considering the equivalent circuit for the measurement. For simplicity consider the FET sample, which can be represented by



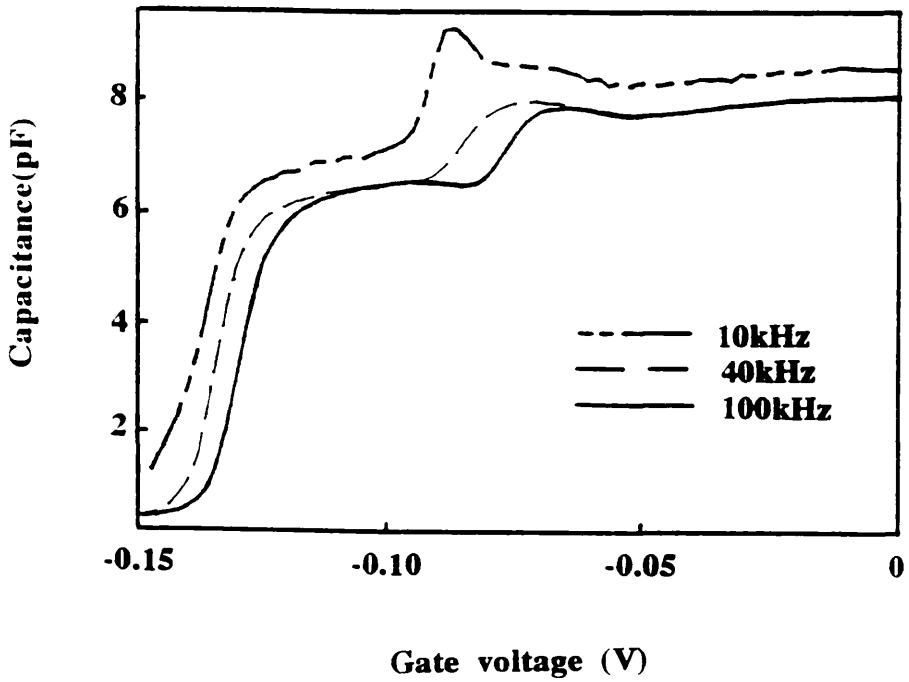
where G_S is the total conductance and C_S is the capacitance between the gate and the channel. This is a crude approximation of the system, but suffices for this simple model. For the capacitance measurement the source and drain contacts are connected to the 'low' terminal, so for the purposes of the capacitance measurement the sample can be represented by,



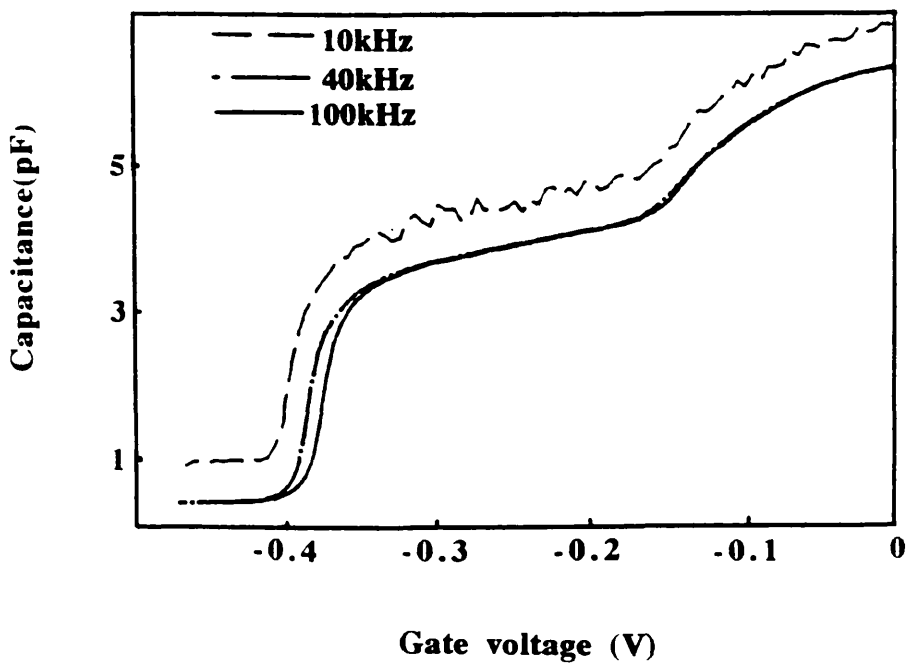
However, in order to use the optimal scales on the LCR meter, the capacitance was measured with the LCR in the "parallel" mode, so the measurements taken are, in fact, C_p and G_p, represented by,



Using simple circuit theory it can be shown that,



Graph 4.12(a): Capacitance characteristics for A21618 (FET) as a function of frequency, at 15K.



Graph 4.12(b): Capacitance characteristics for A21611 (wire) as a function of frequency, at 15K.

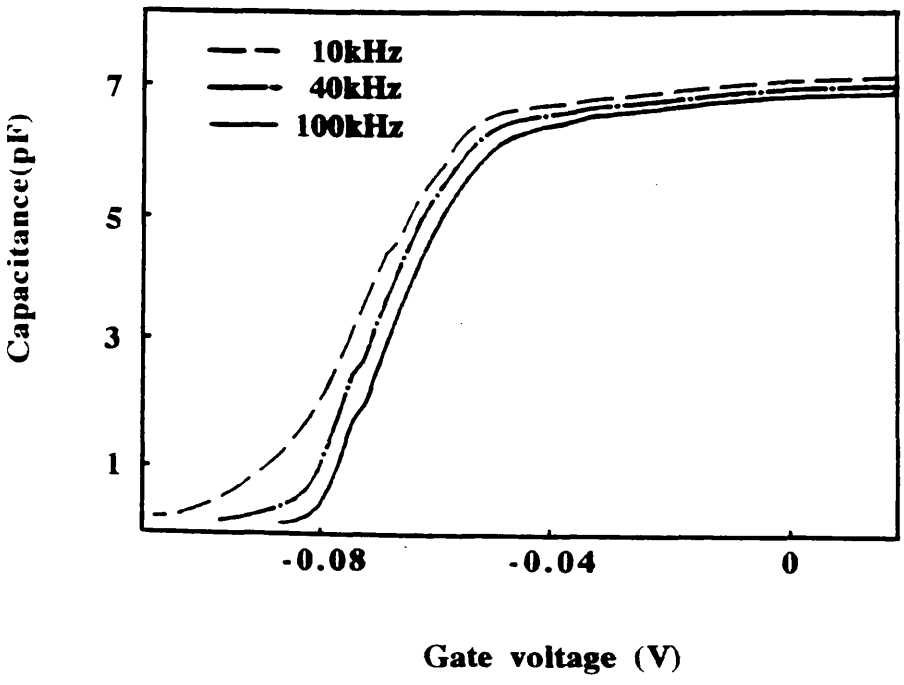
$$C_p = \frac{C_s g_s^2}{\omega^2 C_s^2 + g_s^2} \qquad (4.1)$$

which expresses the measured capacitance in terms of the measurement frequency, and the equivalent series capacitance and conductance. Analytically, this expression can be treated in three different limits, the first being the high conductance limit in which $g_S >> \omega C_S$, and the magnitude of the capacitance is not dependent on the measurement frequency, the second being $g_S \sim \omega C_S$, in which case the capacitance magnitude is dependent on the frequency and, finally, the limit $g_S << \omega C_S$ where the magnitude of the capacitance is dominated by the frequency.

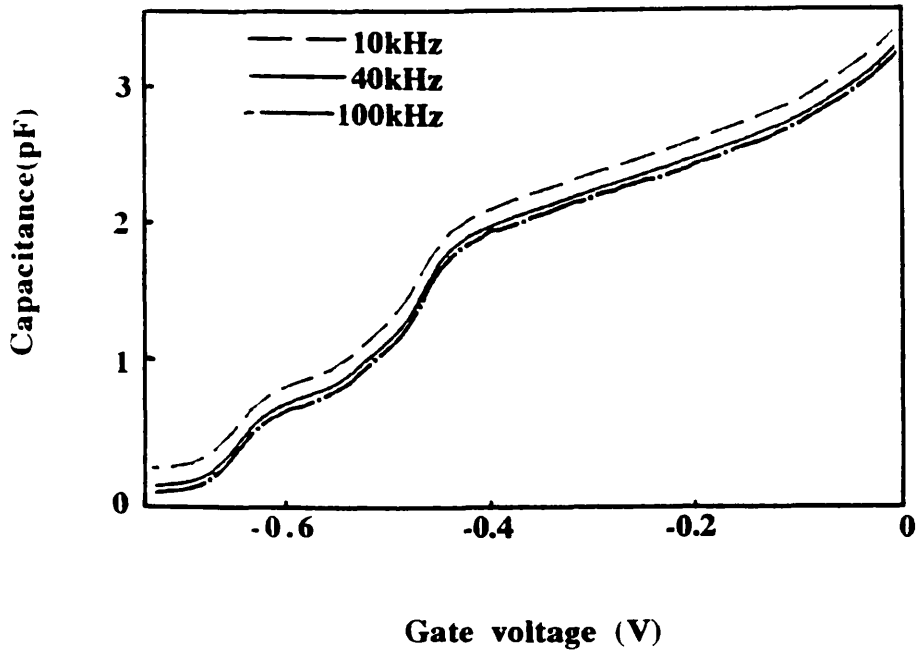
At 15K the first limit was applicable in the high conductance voltage range, away from the cut-off voltage, where the 2DEG was not significantly depleted by the gate bias. The second limit was achieved in the cut-off region, where frequency dependent effects are observed experimentally in both A21611 and A21618. The third of these limits was not physically realised as the series conductance was never found to be significantly less than ωC_S.

The characteristics for the samples measured at 40mK are given in Graph 4.13 (a) and (b). From these curves it can be seen that the main effect of a change in frequency is the addition of a constant capacitance to each of the characteristics, which again is attributed to input and lead effects. In the FET sample there is some evidence of a shift in the threshold voltage as the frequency is changed, similar to that seen in the high T measurements, but no such effects are evident in the wire sample at 40mK, which suggests that the conductance and the capacitance always remain in the limit $g_S >> \omega C_S$.

It should be noted that the frequency dependence of samples gives an indication of the sample and material quality. In 'good' samples, with high electron mobilities, both the conductance and the capacitance should merely reflect changes in the amount of charge in a system, so the ratio $g_S/\omega C_S$ should remain constant and $g_S >> \omega C_S$, and the capacitance characteristic should display no frequency dependence. However, if the transport is dominated by scattering events and the effects of non-uniformities in the system then the mobility, and hence the conductance (which is sensitive to such effects) is reduced faster than the capacitance enabling the condition $g_S \sim \omega C_S$ to be satisfied. The effects of non-uniformities and scattering events become more significant as the gate bias approaches the cut-off voltage as the number of electrons is reduced and so any screening of non-uniformities is removed. The fact that the characteristics of A216 wire samples measured at 15K always display frequency dependent effects, whereas wire characteristics measured at 50mK never show such effects, reflects the increase in the electron mobilities as the temperature is decreased, which is sustained even at gate voltages near the cut-off voltage.



Graph 4.13(a): Capacitance characteristics for A21615 (FET) as a function of frequency, at 50mK.



Graph 4.13(b): Capacitance characteristics for A21614 (wire) as a function of frequency, at 50mK.

It is interesting to note that the FET samples did show frequency dependence in the cut-off region at 50mK. This is due to the planar nature of the depleting potential for FETs which reduces the number of electrons in the 2DEG by lowering the carrier concentration, thereby removing the screening of non-uniformities. In contrast, in the wire samples the depleting potential is lateral and reduces the number of electrons by narrowing the channel not by reducing the carrier concentration (this is confirmed by the magnetotransport data presented in Chapter 5 which shows conclusively that the carrier concentration in the wires remains constant even at voltages near the cut-off voltage).

(d) a.c. parallel conductance

The parallel conductance was measured with the capacitance. A full expression for this, in terms of the sample parameters is complex; for a discussion of this see Norris et al, 1990. However, following the simple model presented in the previous section the parallel conductance, G_p, can be expressed as,

$$G_p = \frac{\omega^2 C_s^{\,2} g_s}{\omega^2 C_s^{\,2} + g_s^{\,2}} \qquad (4.2)$$

The parallel conductance data for A21611 (wire), and A21618 (FET), at 15K is plotted in Graphs 4.14(a) and (b), respectively. The parallel conductance for A21614 (wire) and A21615 (FET), at 50mK, is plotted in Graphs 4.15 (a) and (b). These are the same samples used in the previous section, for reference see Graphs 4.12 (a) and (b), and 4.13 (a) and (b).

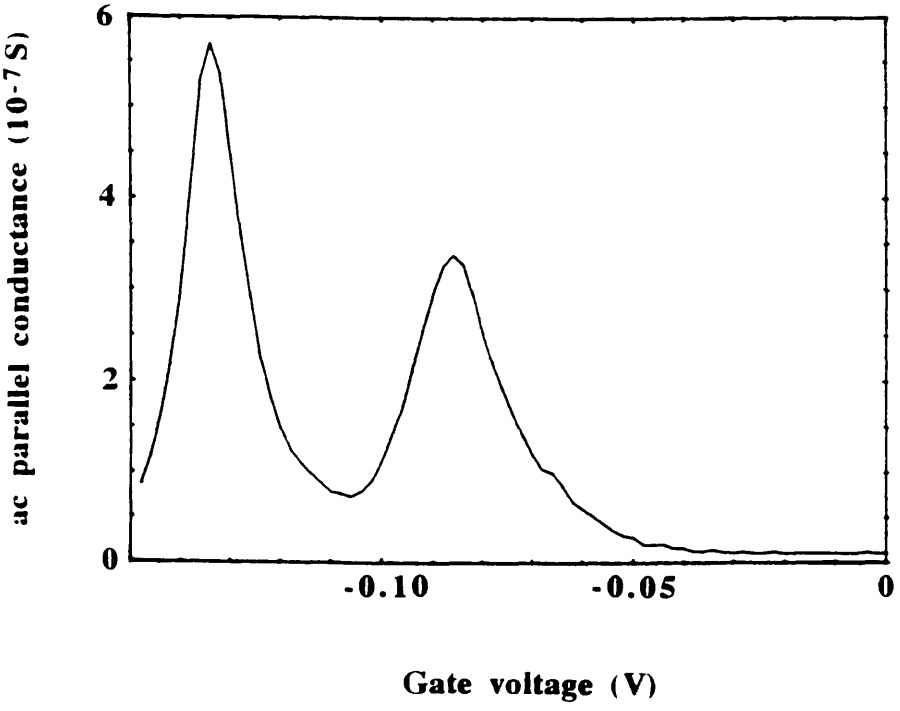
From Graphs 4.14 and 4.15 it can be seen that there are peaks in the parallel conductance when the capacitance is changing rapidly, mainly in the cut-off regions of the devices.

From the expression above it can be shown that the parallel conductance is at a maximum when,

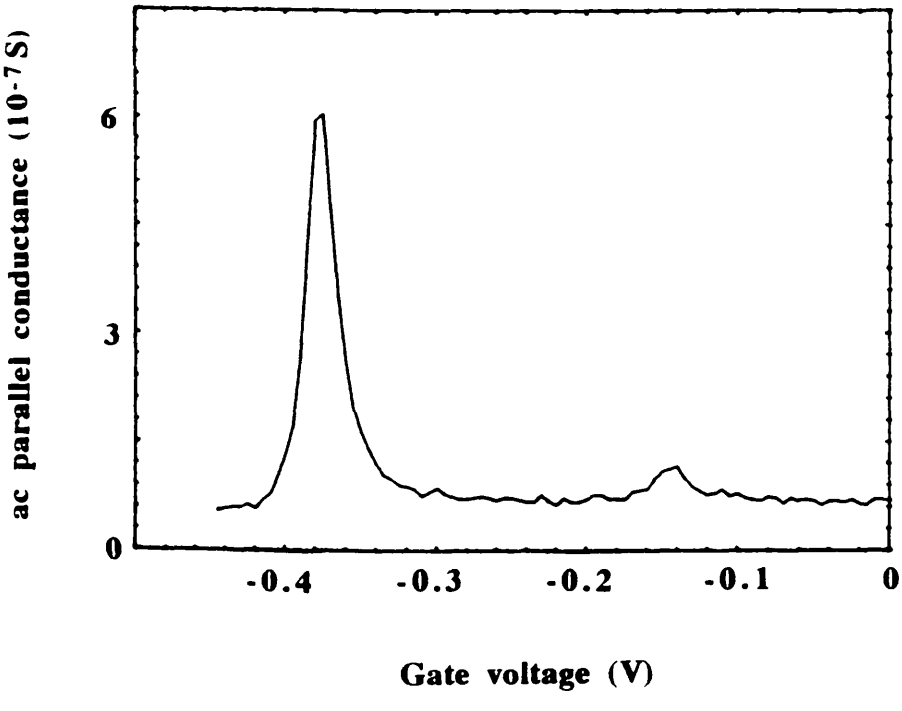
$$\frac{g_s}{\omega C_s} = 1 \qquad (4.3)$$

This is the same condition required to observe frequency dependence in the capacitance characteristics. As with the frequency dependence this condition is realised in the cut-off region due to the effects of non-uniformities and enhanced scattering events in the 2DEG, which can reduce the conductance significantly without affecting the capacitance.

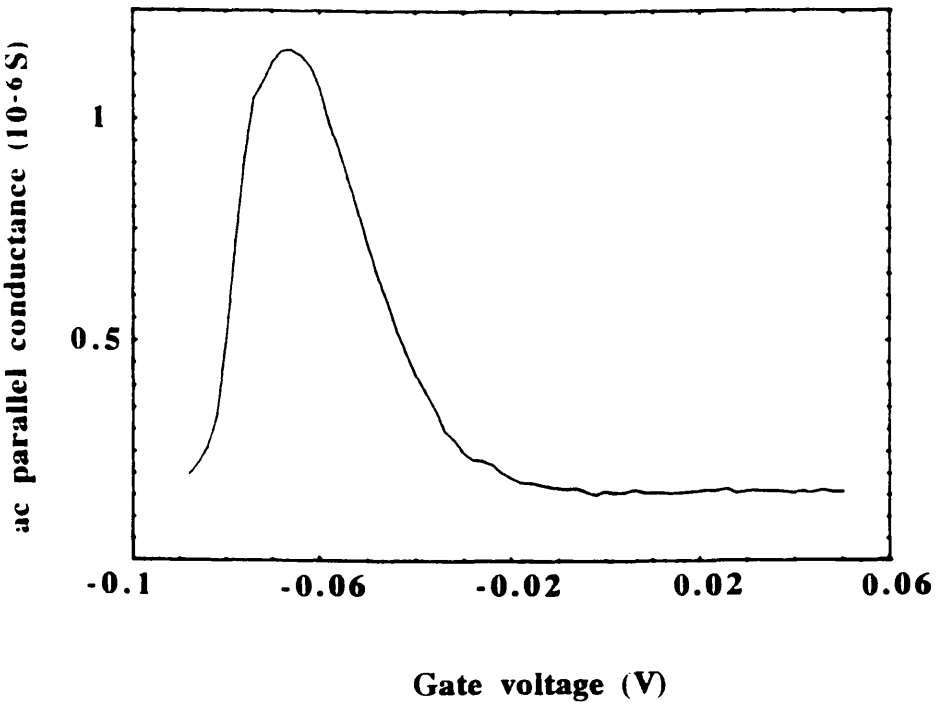
From Graph 4.15(b) it can be seen that at low temperatures the parallel conductance of A21614, the wire sample, displays the peaks in the parallel conductance seen at 15K, but the magnitude of the peaks is much lower, implying that



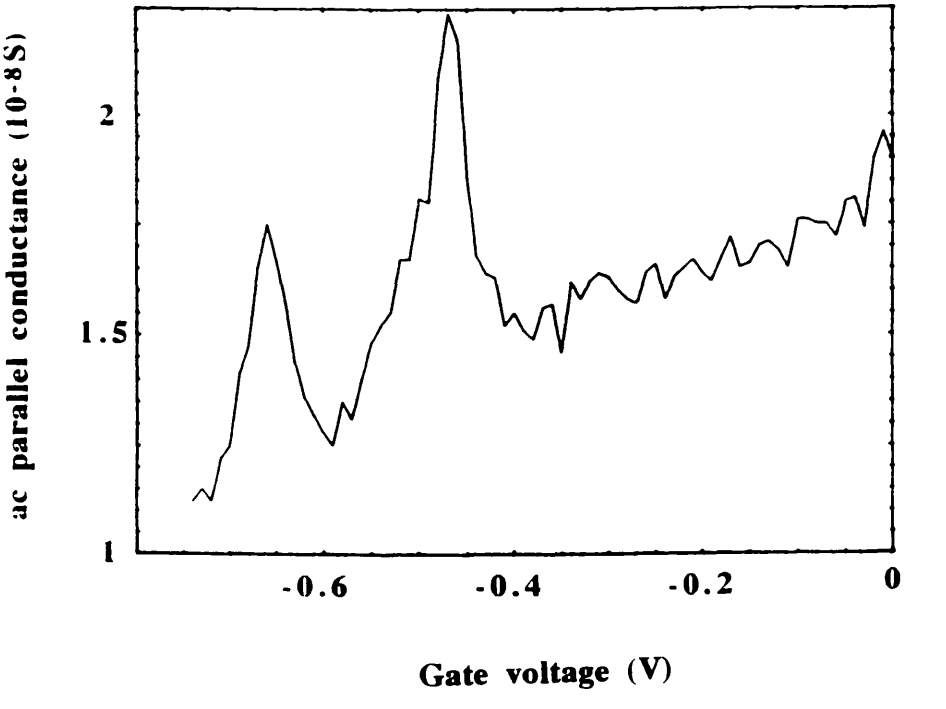
Graph 4.14(a): ac parallel conductance characteristic for A21618 (FET), at 15K.



Graph 4.14(b): ac parallel conductance characteristic for A21611 (wire), at 15K.



Graph 4.15(a): ac parallel conductance characteristic for A21615 (FET), at 50mK.



Graph 4.15(b): ac parallel conductance characteristic for A21614 (wire), at 50mK.

at 50mK the mobility of the electrons, and hence the conductance, remains high well into the cut-off region, with the capacitance and conductance both reflecting only changes in the number of electrons. However, the parallel conductance of the FET is similar to that at high temperature, so again it is proposed that this is due to the lowering of the carrier concentration in the 2DEG.

(e) Evidence of 1D sub-band structure

One of the main aims of this project was to observe structure in the capacitance characteristics indicating quantum confinement. This was expected to be seen at temperatures below 1K. Each of the capacitance characteristics measured was differentiated with respect to V_g in a search for structure. The capacitance characteristic for A21614 at 50mK, and the corresponding derivative with respect to V_g, are given on Graph 4.16.

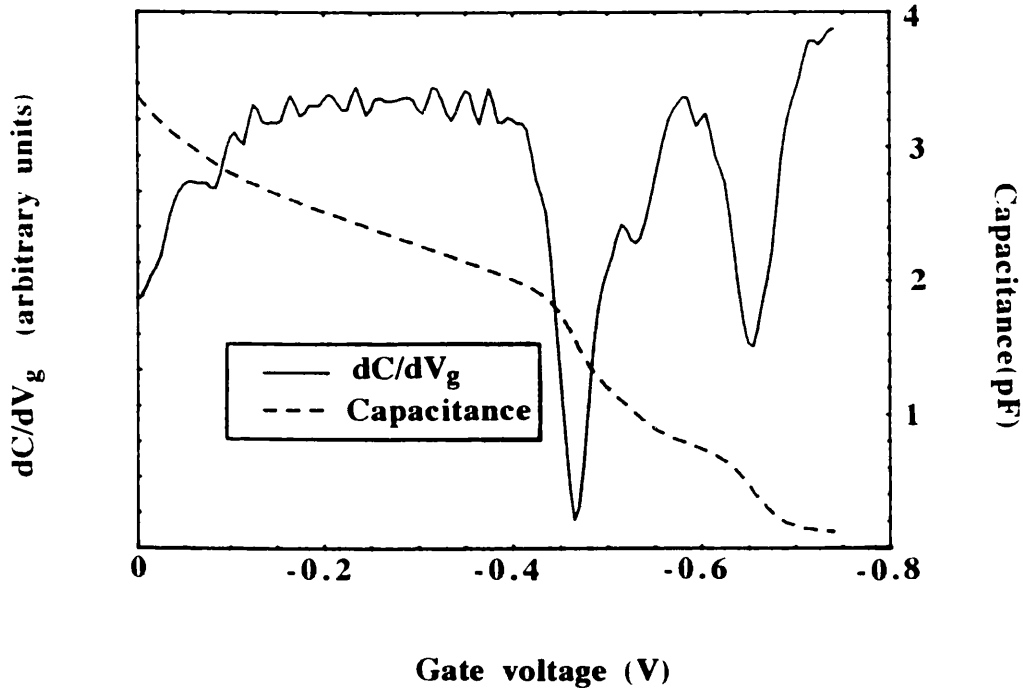
It can be seen that there is no convincing evidence of any sub-band structure.

(f) Summary of effects seen in the capacitance characteristics of A216 samples

The A216 samples, although all different, do display similar features. Consider firstly the FET samples. Several of the FET characteristics measured at 15K displayed a slight increase in the capacitance at about +0.15V, also seen in the wire sample A2169, suggesting that, at this voltage, electrons were in the conduction band in the AlGaAs layer and able to communicate with the channel. The increase in the magnitude of the capacitance at biases above +0.15V, when the FET sample A21610 was illuminated, implies that this is valid. Several of the capacitance characteristics also displayed a peak in the capacitance at, or around, the planar cut-off point. This feature was found to be particularly sensitive to light and frequency.

Several of the wire samples displayed a step in the capacitance near the cut-off voltage, illustrated by A21614 in Section 4.4.2(a). The reason for this step is not clear. Initially it was thought that it may have been due to electrons in the conduction band in the AlGaAs. However, on a qualitative level, due to the lateral nature of the squeezing potential depleting the wires, it would be expected that the 2DEG would be depleted before the AlGaAs, so the capacitance of the wire should remain at the high AlGaAs value.

Finally the A216 samples measured at 15K show evidence of frequency dependence in the cut-off regions of the capacitance characteristics, and are sensitive to illumination with HeNe radiation. However, at low temperatures, the capacitance characteristics of A216 wire samples display no frequency dependence and, unfortunately, no evidence of structure indicating quantum confinement.



Graph 4.16: Capacitance characteristic for A21614 (wire), and derivative with respect to gate voltage, at 50mK.

4.4.3 CAPACITANCE DATA FOR A425 SAMPLES

Three A425 samples were measured in the refrigerator, the sample indentification numbers being as follows, A42529, A42532, and A42531. An FET sample, fabricated by the author, was measured in the closed circuit system by S.Vallis, a project student and the results obtained will be used for reference.

(a) Presentation of capacitance data for A425

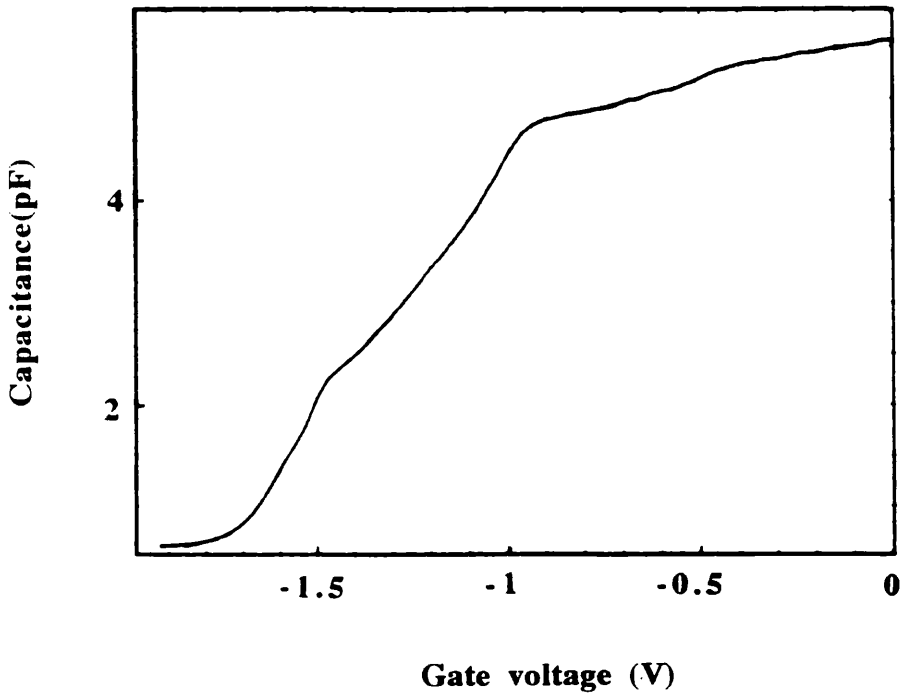
A42529

This was a wire sample with wire widths of 430nm and separations of 690nm and, again, five terminals. The sample was measured in two refrigerator runs. The capacitance characteristic is shown in Graph 4.17. It can be seen that there are three main features in this characteristic. The first of these is at -0.5V where there is a slight step in the capacitance. The second feature is the rapid fall in the capacitance at -1.0V. The third, and final, feature is at -1.5 V, where the wires are cutting-off. As a result of the fact that there was no control FET sample measured it is difficult to estimate the position of the FET cut-off. However the most likely FET cut-off voltage is at -1.0V. The feature at -0.5V is reminiscent of that seen in the A216 FET samples at +0.15V, so it is proposed that at this voltage electrons are populating the conduction band in the AlGaAs. The implications of this will be discussed later.

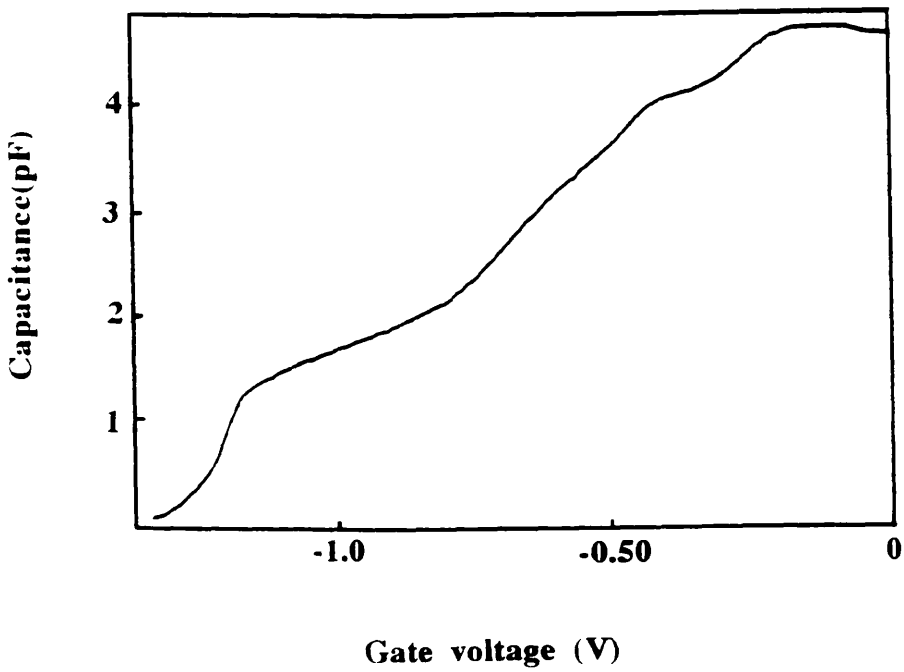
A42532

This is a wire sample with five terminals, wire widths of 570nm, and separations of 600nm. In the virgin state, only the gate contact and one of the large side ohmic contacts were functioning, allowing the capacitance to be measured but not the channel conductance. The characteristics taken in the dark state are shown in Graph 4.18(a). From this it can be seen that the characteristic exhibits a plateau in the range 0V to -0.3V, then a sharp decrease in capacitance and a further levelling of the capacitance until -0.45V. Thereafter, the capacitance appears to have two distinct gradients, the first of these in the range -0.45V to -0.7V and the second in the range -0.7V to -1.0V. As with A42529 it is difficult to determine the FET cut-off. However an estimate for this was taken to be at -0.45V. Again, the plateau in the characteristic in the voltage range 0V to -0.3V suggests that there were electrons in the conduction band in the AlGaAs.

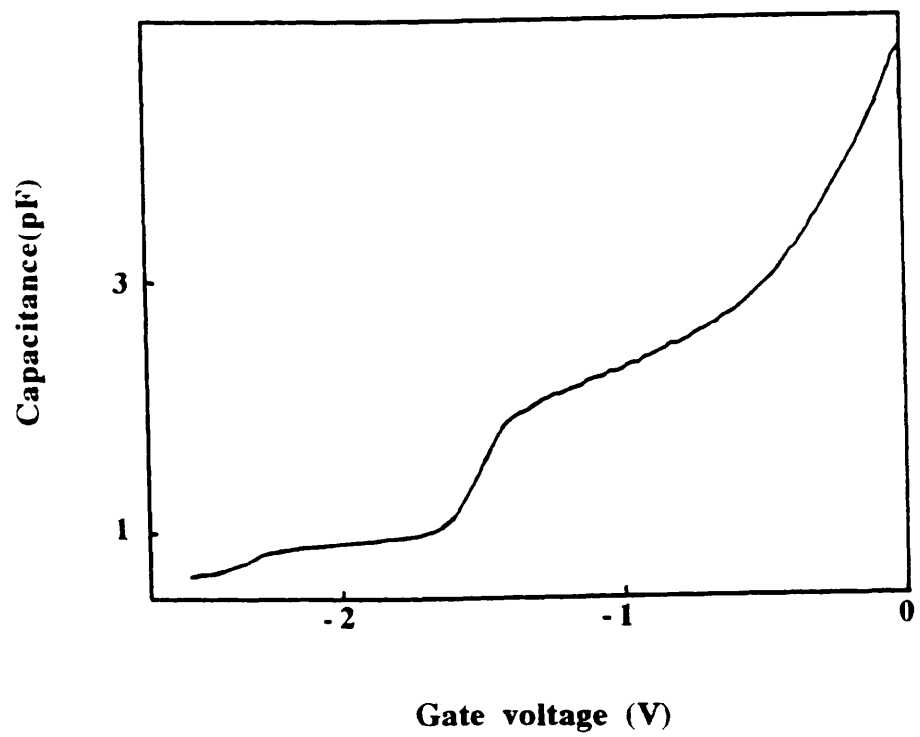
To stimulate the high resistance contacts, the sample was illuminated with light from a GaAs LED. This excited so many electrons into the conduction band in the AlGaAs that the gate could not sustain a negative bias sufficient to deplete the channel fully. To redress this, the sample was annealed by lifting the insert out of the He_4 bath



Graph 4.17: Capacitance characteristic for A42529 (wire) at 4.2K.



Graph 4.18(a): Capacitance characteristic for A42532 (wire), in dark state, at 4.2K.



Graph 4.18(b): Capacitance characteristic for A42532 (wire), in illuminated state, at 4.2K.

and allowing it to heat up to about 200K for half an hour. After this the sample was in a suitable state to be used, with all the contacts in good working order. The characteristics in this condition are given in Graph 4.18(b). From this it can be seen that the effect of the light was to make the cut-off voltage significantly more negative, implying that the number of electrons in the conduction band was greatly increased. The characteristic displays a step and then a long 'tail' in the capacitance, extending from -1.6V to -2.7V. This isn't unlike the steps seen in some of the A216 samples, particularly A21614, although the cut-off voltages involved are markedly more negative.

A425 31

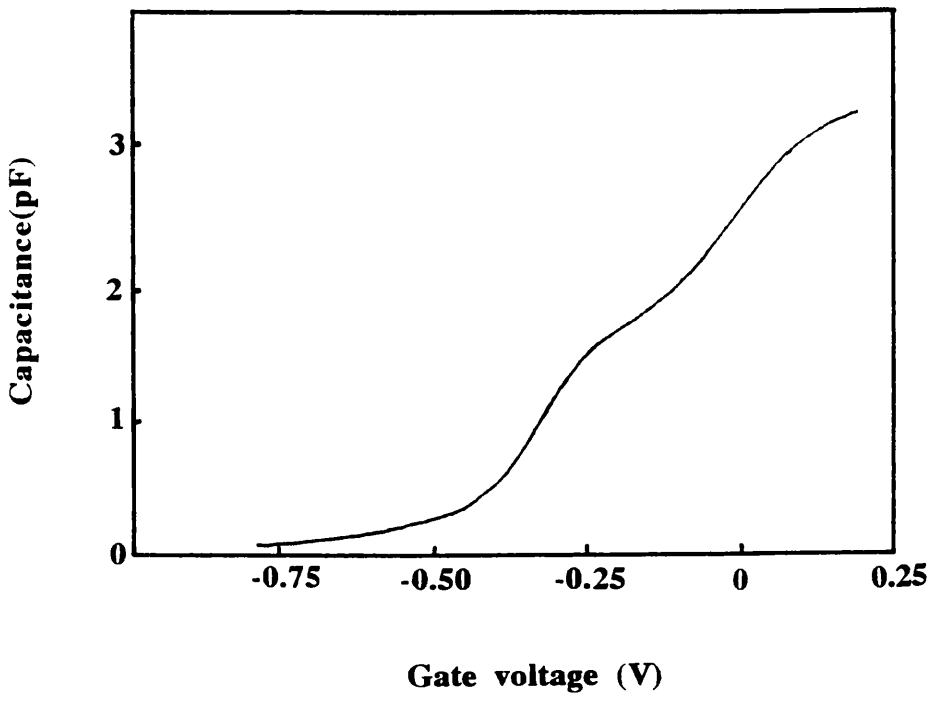
This sample had five terminals, wire widths of 430nm and separations of 560nm. The sample was measured in the same refrigerator run as A42532. Therefore, it experienced the somewhat traumatic cycle described in the previous section (traumatic for both sample and experimenter!). Like A42532, in its initial state none of the side voltage contacts on the sample were working, and only one of the source/drain contacts. Again it was possible to measure the sample capacitance in the dark, but not the channel conductance. The capacitance characteristic taken in the dark state is shown in Graph 4.19 (a). From this it can be seen that the wire cut-off voltage is at -0.3V and that the wires become fully formed in positive bias at +0.2V. This characteristic is quite dramatically different from that of A42532. This is somewhat suprising as the wires on A42531 were only 60nm narrower than those of A42532, with all the other sample dimensions identical. The devices were also on adjacent sites of the same chip, and so experienced identical fabrication steps. After the light and annealing stages described previously all the sample contacts recovered. The capacitance characteristic in the illuminated state is shown in Graph 4.19 (b) and is quite different from that taken in the dark state. The cut-off voltage is significantly more negative and the wire region is extended. The wires are formed at about -0.6V. There is also a sharp rise in the capacitance at -0.2V.

A42522

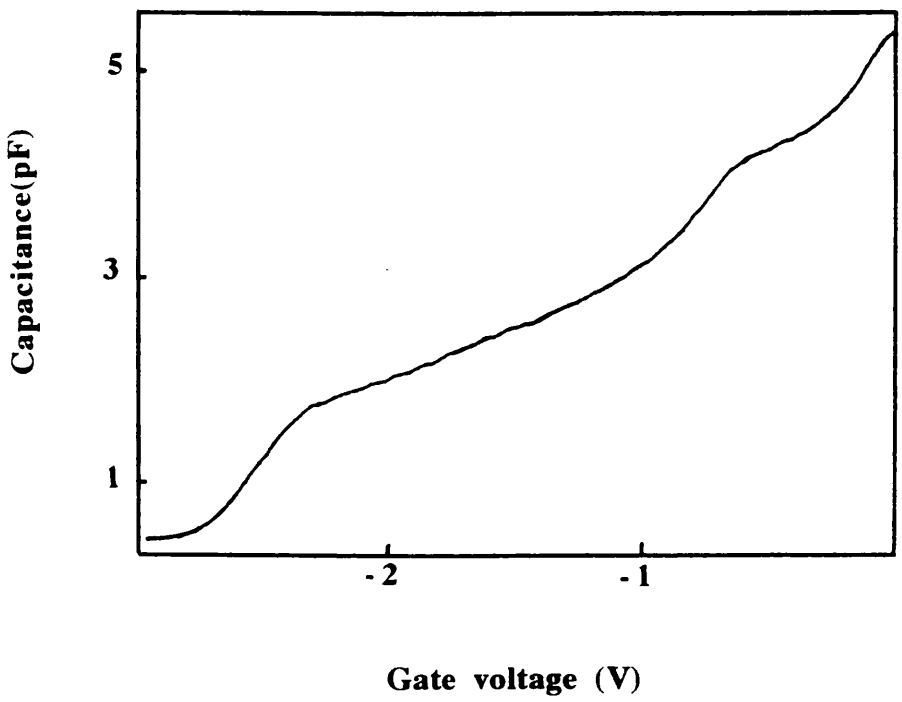
This sample was measured by Stuart Vallis, a project student. A42522 was an FET sample, and was measured in the closed circuit system. The capacitance characteristic measured at 15K is given in Graph 4.20.

(b) Effects of illumination with light from a GaAs LED

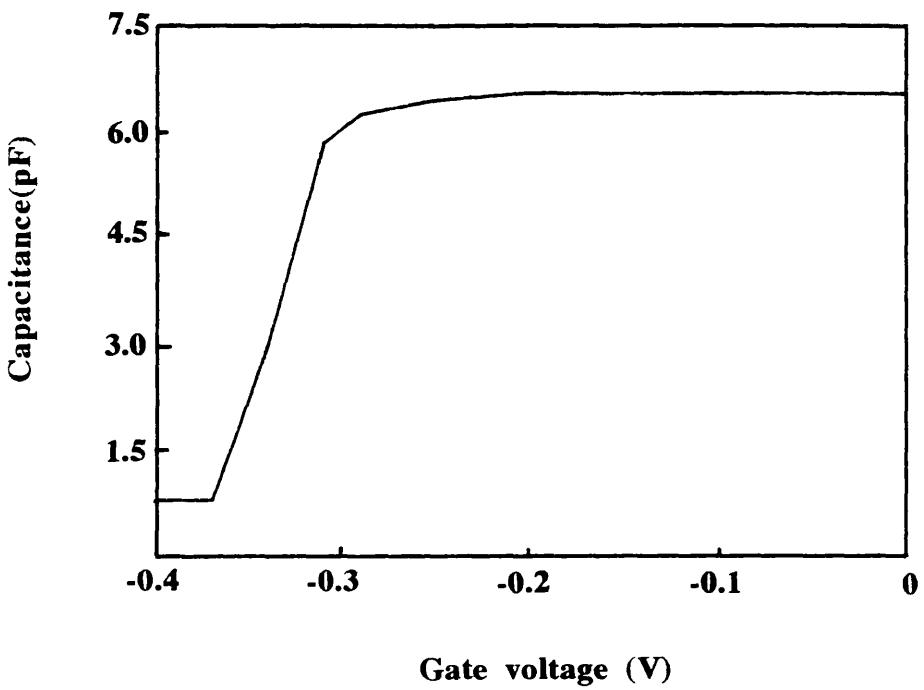
As with A216 samples the effect of sample illumination with a GaAs LED was to stimulate carriers into the conduction band, in both the 2DEG and AlGaAs layers.



Graph 4.19(a): Capacitance characteristic for A42531 (wire), in dark, at 4.2K.



Graph 4.19(b): Capacitance characteristic for A42531 (wire), in illuminated state, at 4.2K.



Graph 4.20: Capacitance characteristic for A42522 (FET) at 15K.

The light state characteristics were presented fully in the previous sections.

(c) Frequency dependence of A425 samples

The frequency dependence of all the A425 samples was measured. The data taken on A42532, in its original (pre-illumination) state, is shown to illustrate the general behaviour, in Graphs 4.21(a) and (b). Graph 4.21(a) shows the characteristics taken at 4.2K when the sample was in the original dark state, and Graph 4.21(b) shows the characteristic taken at 50mK, again in the dark state. From these graphs it can be seen that the main difference in the curves is a constant capacitive offset. As with the A216 samples this is attributed to the parallel capacitance in the leads and the input circuitry of the LCR meter. The only region in which the sample capacitance displays any frequency dependence is in the voltage range 0V to -0.3V. This is an effect seen in all the A425 samples which exhibit this extra step in the capacitance characteristic in the voltage range before the wires are formed, suggesting that in this region there is a time dependent transfer of charge in and out of the conduction band in the AlGaAs layer at 4.2K, which is reduced as the temperature decreases.

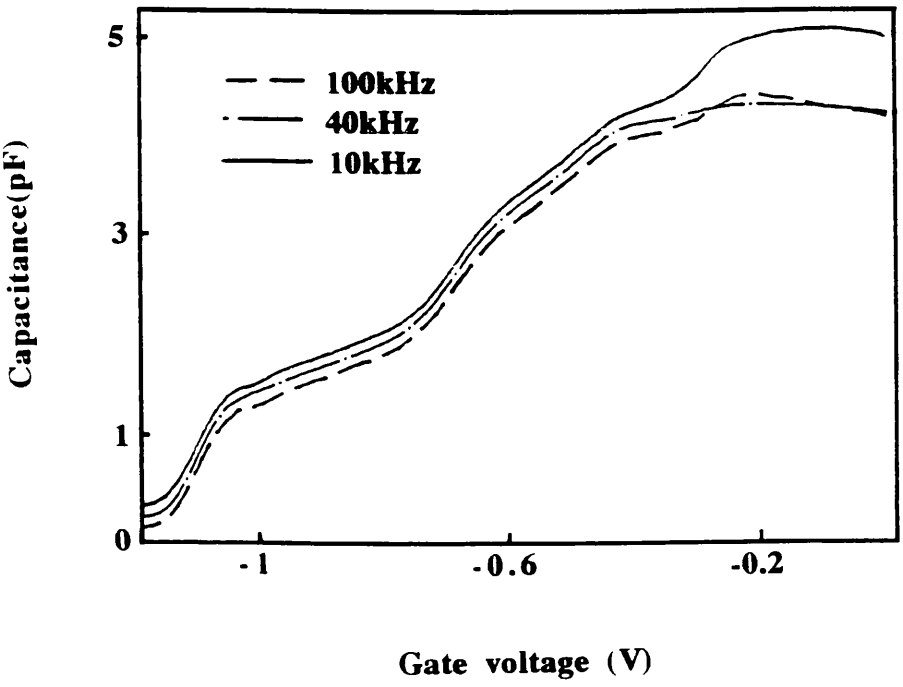
The complete absence of any frequency dependence in the wire cut off region indicates that, following the argument given in Section 4.4.2 (c) for the A216 samples, the conductance of the wires fabricated on A425 remains consistently higher than the capacitance term (ωC_S), suggesting that the conductance cuts off very sharply, never approaching the limit in which the two terms are of the same order, and therefore the electron mobility remains high even at gate voltages approaching the cut-off voltage. The conductance data to be presented later, in Section 4.6(a), agrees very well with this suggestion.

(d) ac parallel conductance data

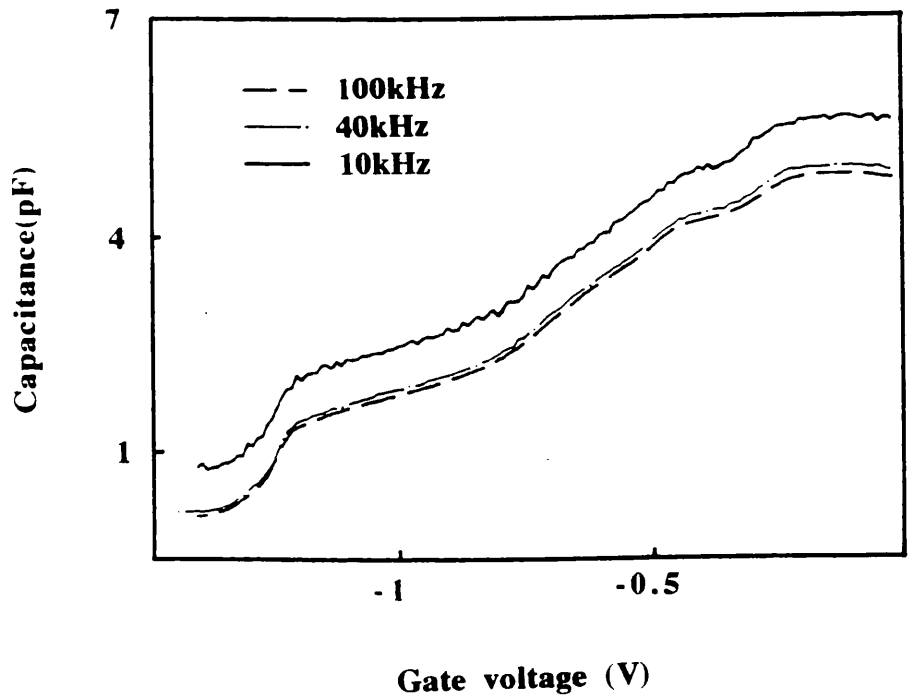
The parallel conductance for A42531, at 40mK, is plotted in Graph 4.22 and shows that the parallel conductance is similar to that seen in the low temperature characteristics of A216, with no sign of a peak in the conductance. Again this suggests that the channel conductance and channel capacitance in A42531 are decreasing at the same rate, and that the channel conductance always remains significantly higher than ωC_S.

(e) Hysteresis effects in A425 samples

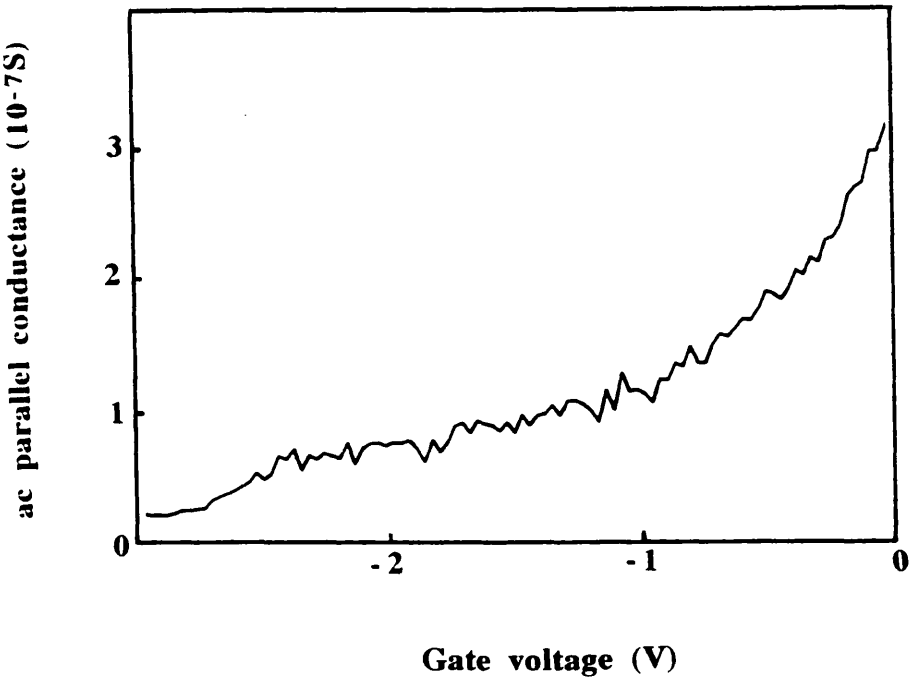
The effects of any possible hysteresis in the capacitance characteristics were investigated. This was most thoroughly executed on A42531, for which the sample capacitance was measured in the voltage range -0.6V to -3.0V, the wire region. The capacitance characteristics were measured from -0.6V to -3.0V and then from -3.0V to



Graph 4.21(a): Capacitance characteristics for A42532 (wire) as a function of frequency at 4.2K.



Graph 4.21(b): Capacitance characteristics for A42532 (wire) as a function of frequency at 50mK.



Graph 4.22: ac parallel conductance characteristic for A42531 (wire) at 40mK.

-0.6V. This experiment was conducted at 100kHz, 40kHz and 20kHz to investigate the frequency dependence. The results for the 100kHz characteristics are shown in Graph 4.23.

From Graph 4.23 it can be seen that changing the direction of the voltage sweep has no effect on the capacitance characteristics at 100kHz. The voltage 'up' and 'down' sweeps result in characteristics which are, in fact, indistinguishable. This was found to be the case for the characteristics measured at all other frequencies and is identical to the result for the A216 samples.

The significance of the lack of hysteresis in the gate voltage is that it indicates that it is not possible to communicate with charge in DX centres in the AlGaAs.

(f) Evidence of 1D confinement

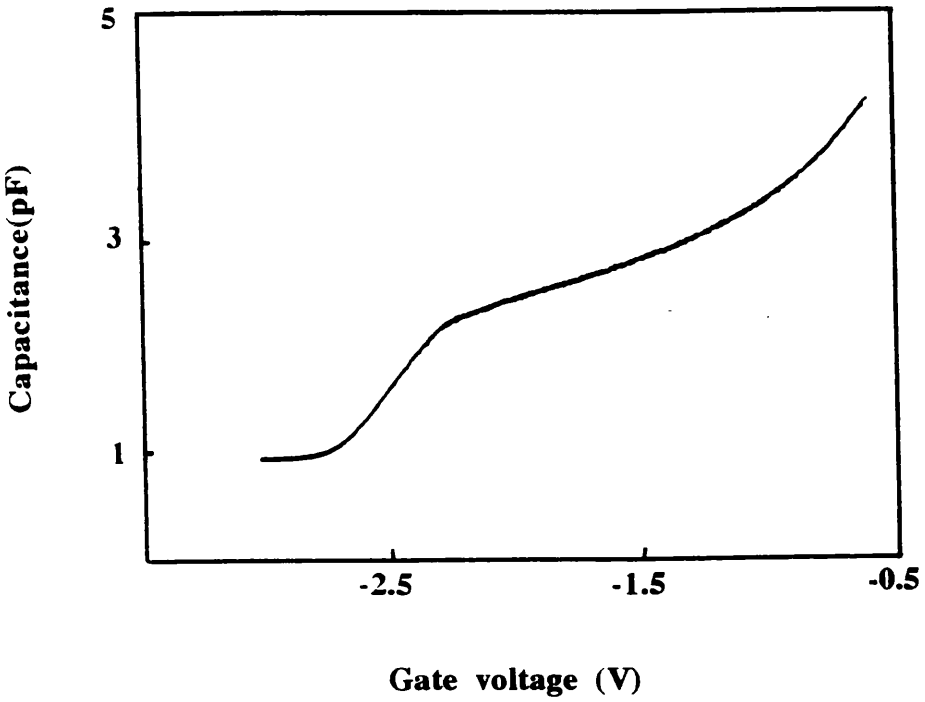
The derivative with respect to V_g for the capacitance characteristic of A42531 at 70mK is given on Graph 4.24, which again displays no evidence of any structure suggesting confinement in the wires.

(g) Summary of effects seen in capacitance characteristics of A425

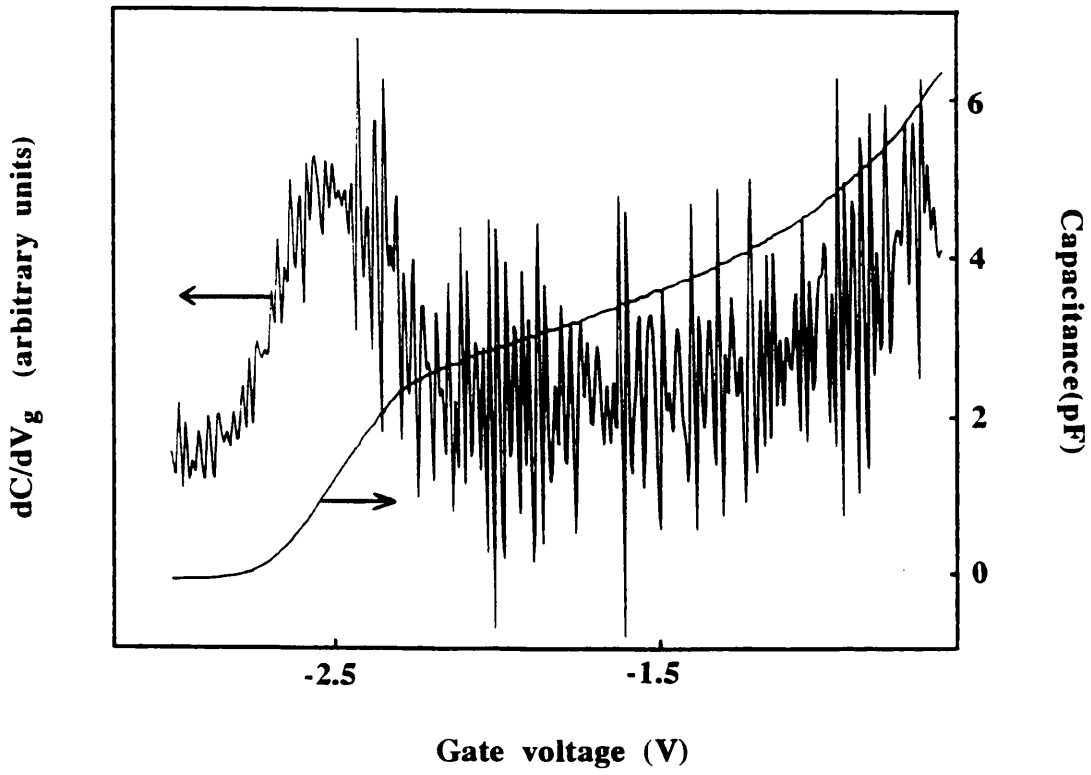
As with A216, all the A425 samples display similar features. In the dark state both A42529 and A42532 show signs of well defined 'steps' in the capacitance, at -0.5V for A42529 and at -0.3V for A42532, suggesting that in these samples electrons were populating the conduction band in the AlGaAs. In the illuminated state for A42531 and A42532, these bumps are no longer evident. Also seen in the illuminated state of A42532 is the long 'tail' in the capacitance, similar to that seen in A21614, but more pronounced.

The differences in the dark state characteristics of A42532 and A42531 illustrate why it is unlikely that devices fabricated on GaAs/AlGaAs heterostructures, in their present form, will ever be suitable for use in engineering applications. The characteristics of these devices depend critically on the specific history of every individual sample. It would be virtually impossible to predict quantitative low temperature sample behaviour of samples of this type.

Finally the data shows conclusively that the capacitance measurements taken on A425 wire samples show no frequency dependence and hysteresis, and, unfortunately, as with A216, none of the capacitance data taken at any temperature, and under any experimental conditions, display structure produced by confinement effects. This can only be described as enormously disappointing.



Graph 4.23: Capacitance characteristics for A42531 (wire) with gate voltage swept from -0.6V to -3.0V, and -3.0V to -0.6V, at 80mK.



Graph 4.24: Capacitance characteristic for A42531 and derivative with respect to gate voltage at 70mK.

4.5 LOW T CHANNEL CONDUCTANCE CHARACTERISTICS

In this section the channel conductance, measured as a function of gate bias, will be presented. To avoid having to repeat sample dimensions the details of the geometries are summarised in Table 4.1.

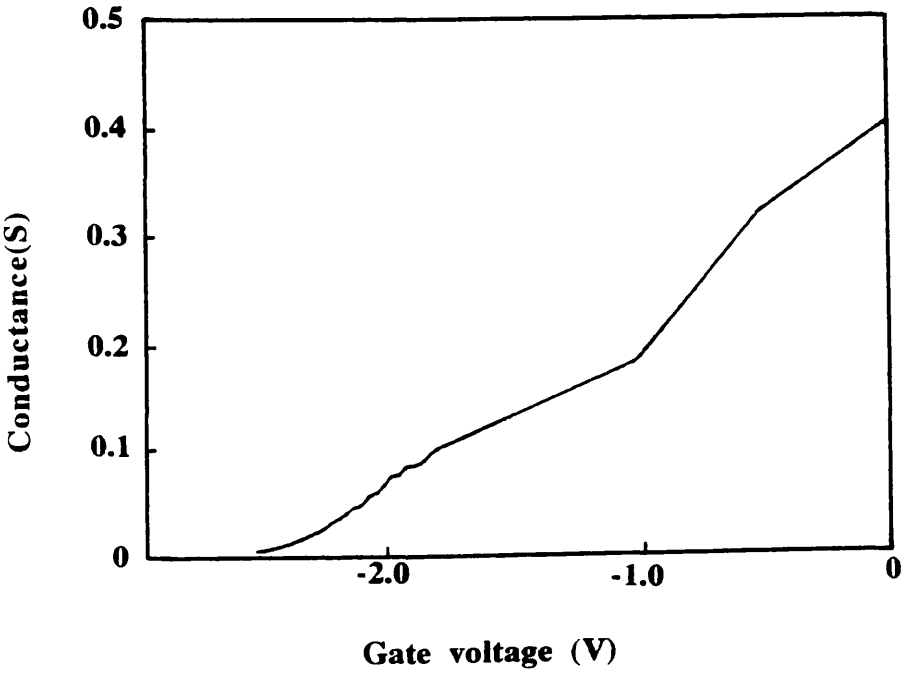
Sample identification	gate length(μm)	gate width(μm)	resist width(nm)	separation of resist ribs (nm)
A21612	17	380	340	525
A21668	17	380	750	400
A21611	17	420	580	620
A21614	17	420	470	470
A42529	17	420	430	690
A42532	17	420	570	600
A42531	17	420	430	560

Table 4.1 Table of sample geometries

A typical conductance characteristic is shown in Graph 4.25 for A42531. From this it can be seen that the conductance follows the general trend seen in the capacitance data with the conductance falling at the FET cut-off point and then gradually decreasing in the region where the wires are being depleted. This is typical of the wire samples.

4.6 LOW T CONDUCTANCE IN CUT-OFF REGION

The temperature dependence of G-V in the range 40-300mK, in the cut-off region was measured extensively. The intention was to look for sub-band effects, temperature dependent hopping currents, or fluctuation effects, in the limit where very



Graph 4.25: Conductance characteristic for A42531 at 70mK.

few electrons were present in the wires. The samples measured in this temperature range were A21614, A21611, A21618, A42529, A42532, and A42531.

The source drain voltage used was 1mV and the measurement frequency was 35Hz, other more specific measurement conditions are given on the graphs.

(a) Presentation of data

A21614

The conductance characteristics measured at 4.2K and 70mK are given on Graph 4.26. The conductance in the cut-off region of this sample is typical of the wire samples and effectively shows no temperature dependence, but evidence of three distinct gradients.

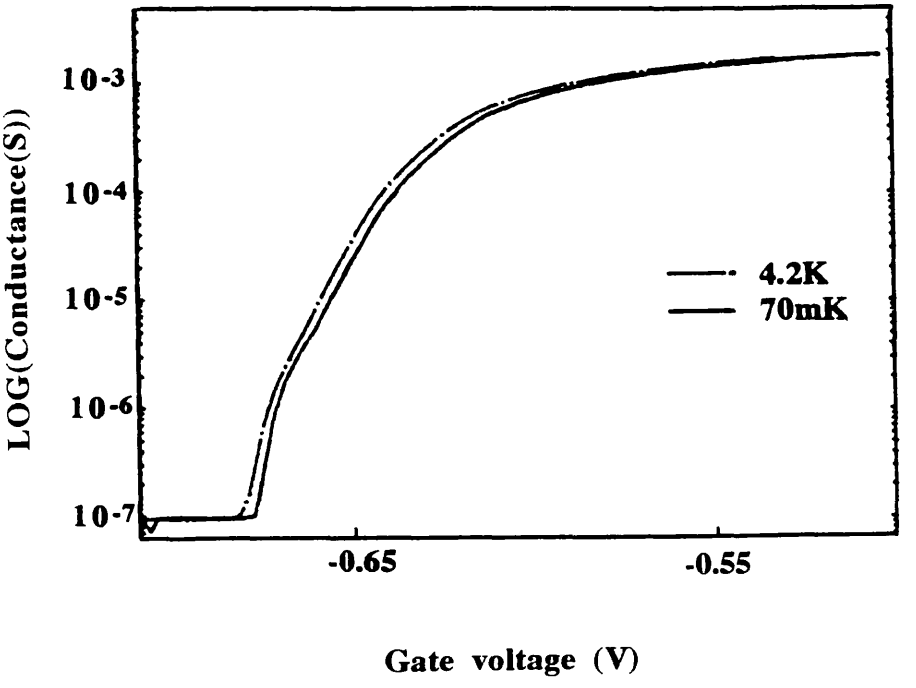
A21611/8

The conductance data for A21618, an FET, and for A21611, a wire sample, are shown on Graphs 4.27 and 4.28 respectively. From Graph 4.28(a) it can be seen that there is very little temperature dependence in the wire sample A21611. However, in the FET, A21618, there is some evidence of a low temperature shift in the threshold voltage to a more positive value. This may indicate that in this particular sample the system has not reached a state of equilibrium. However, the effect is very small, the shift being only about 5mV.

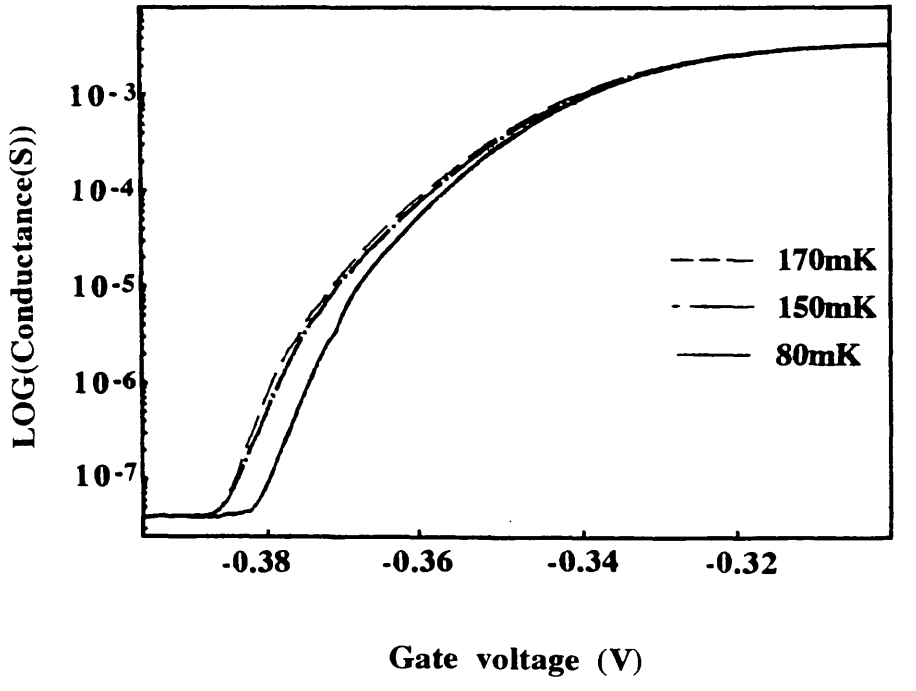
Like A21614, the conductance for A21611 shows three distinct gradients. The first of these gradients is in the high conductance region, in the voltage range -1.4V to -1.56V, when most of the wires are contributing to the conductance and confinement effects, if any, are most likely to be seen. The other two gradients are where the effects of any potential fluctuations should become significant. In the second section, between -1.56V and -1.6V, the conductance starts to fall rapidly, and it is in this region that the majority of the wires are being depleted, and in the final section, where the gradient is steepest, it is estimated that only a few of the wires are still conducting.

Comparing Graphs 4.27 and 4.28(a) it can be seen that the drop in the conductance in the FET is much more gradual than that seen in the wire sample.

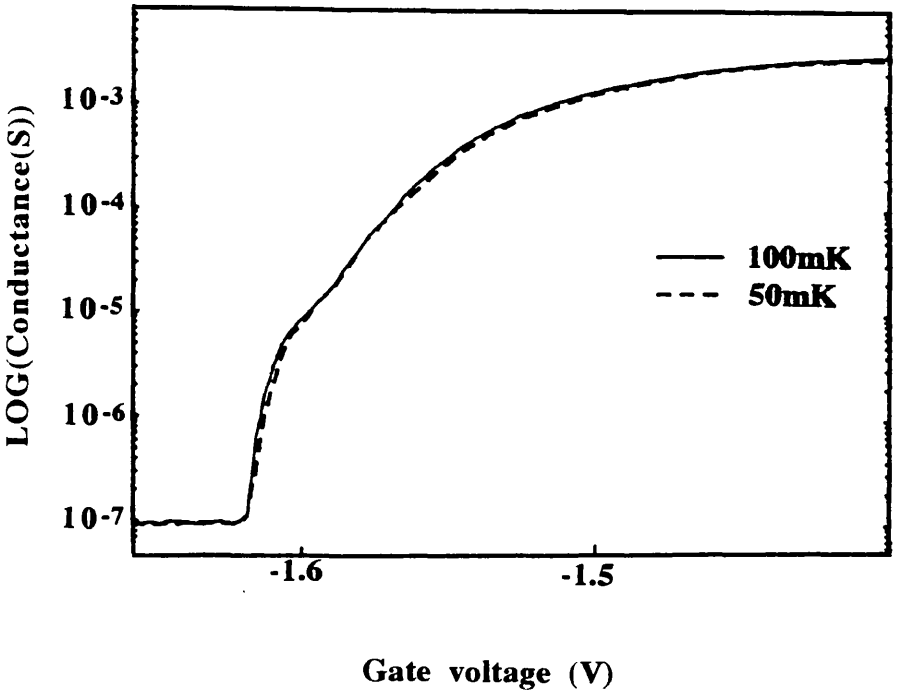
The derivative of the wire conductance with respect to the gate voltage is given in Graph 4.28(b). From this it can be seen that in the range -1.4V to -1.54V there are a well resolved set of oscillations with a period of 10mV. For wires of width 580nm the estimated separation of the electron sub-bands in gate voltage is about 10mV. Therefore these oscillations may actually be the result of confinement effects in the wires, although it is difficult to say that this is definitely the case but it is the most convincing evidence available from the conductance data. Unfortunately, due to the



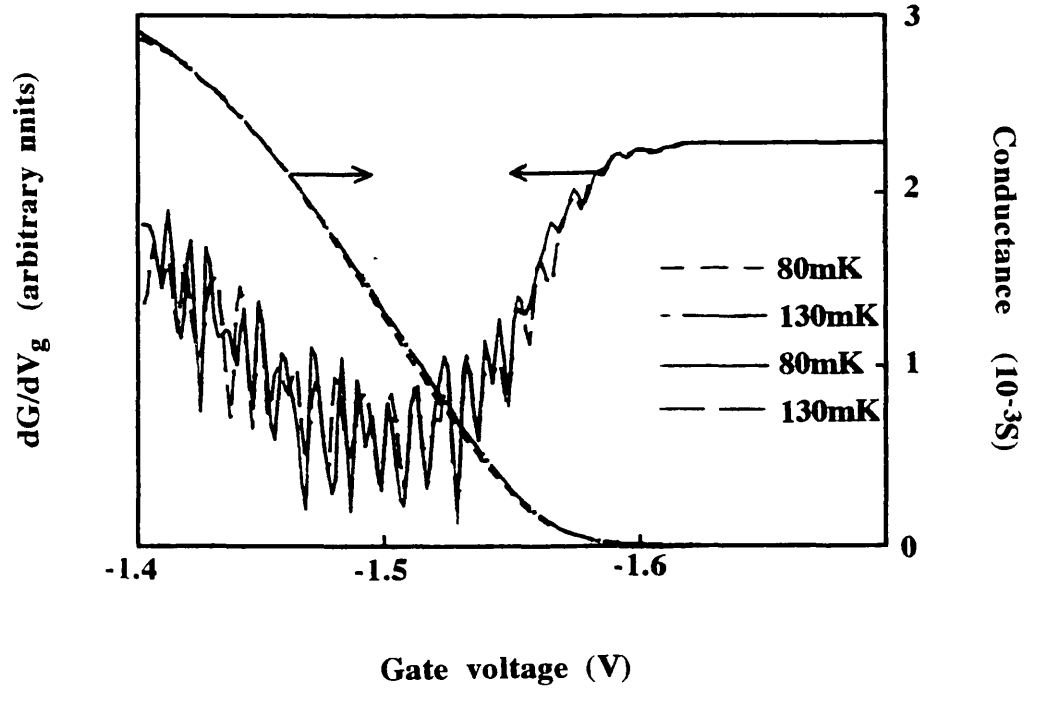
Graph 4.26: Conductance characteristics in cut-off region, for A21614 (wire) at 4.2K and 70mK.



Graph 4.27: Conductance characteristics in cut-off region, for A21618 (FET) as a function of temperature.



Graph 4.28(a): Conductance characteristics in cut-off region, for A21611 (wire) as a function of temperature.



Graph 4.28(b): Conductance characteristics in cut-off region, for A21611 (wire) and derivative with respect to gate voltage.

noise level on the capacitance measurement it is not possible to make a direct comparison with the conductance data.

A42529

The conductance characteristic taken in the first refrigerator run at 80mK is given on Graph 4.29(a), and is very similar to that of A21611 and A21614. The conductance data for A42529 taken as a function of temperature is shown in Graph 4.29(b) - these characteristics were taken in the second of the refrigerator cycles, for which there is no corresponding capacitance characteristic.

From Graph 4.29(b) it can be seen that again there are three regions to this curve estimated to be, from -1.6V to -1.95V, from -1.95V to -2.05V and from -2.05V to-2.12V. It can be seen that there is little dependence on the temperature in the characteristic until -1.95V when the curves deviate slightly at the higher temperatures. At -2.05V the conductance exhibits a resonant tunnelling-like feature. At this point the conductance is of the order of 10μS so this may represent resonant tunnelling through a single impurity site.

The derivative of the conductance with respect to the gate bias is shown in Graph 4.29(c). This graph shows that, although there is a degree of similarity in all the curves, there is not a distinct period, as seen in the A21611 sample.

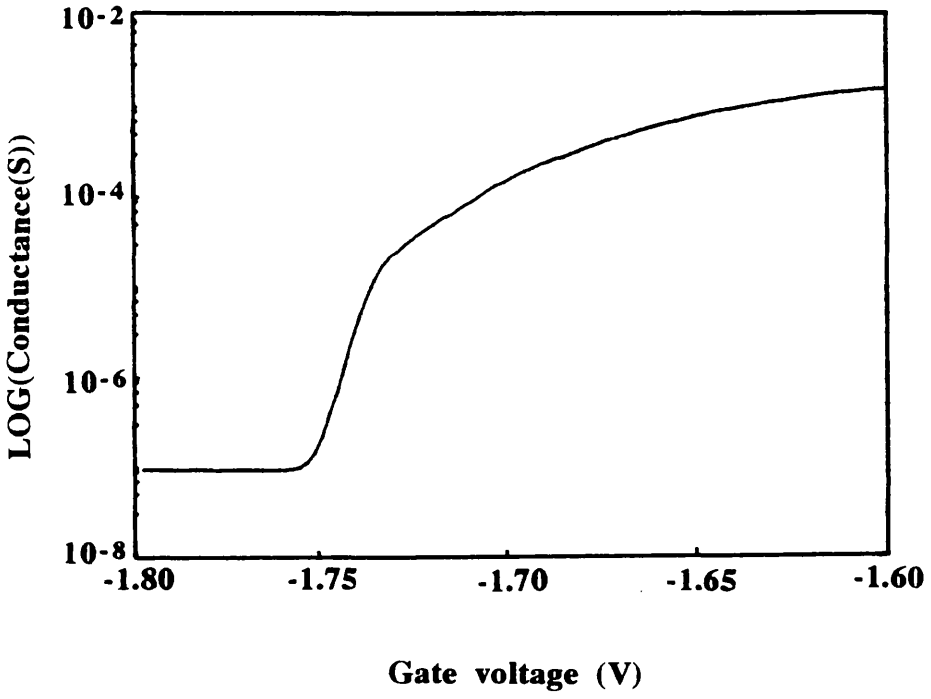
A42532

The conductance data for this sample is given in Graph 4.30(a). Because of the initial state of this sample, in which only one of the side contacts was working, this sample was only measured in its illuminated state. The curves here are quite different in nature from those of the previous samples in that in the third of the 'sections', discussed above, there is a plateau, rather than a steep drop to cut-off, followed by an almost instantaneous cut-off.

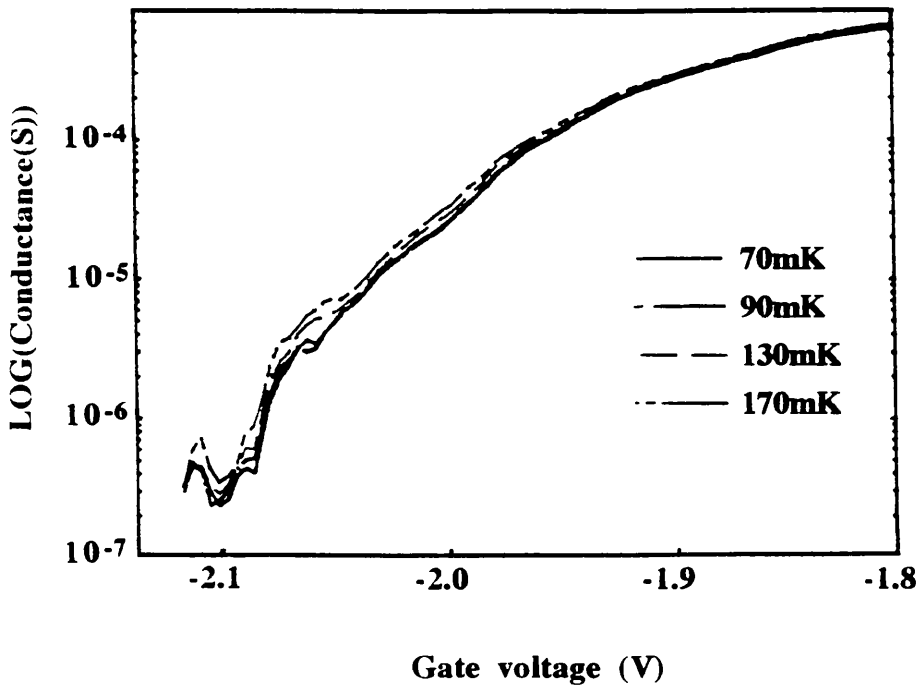
The derivative of the conductance with respect to the gate bias is given on Graph 4.30(b). From this it can be seen that there is very little similarity in derivatives at the various temperatures.

A42531

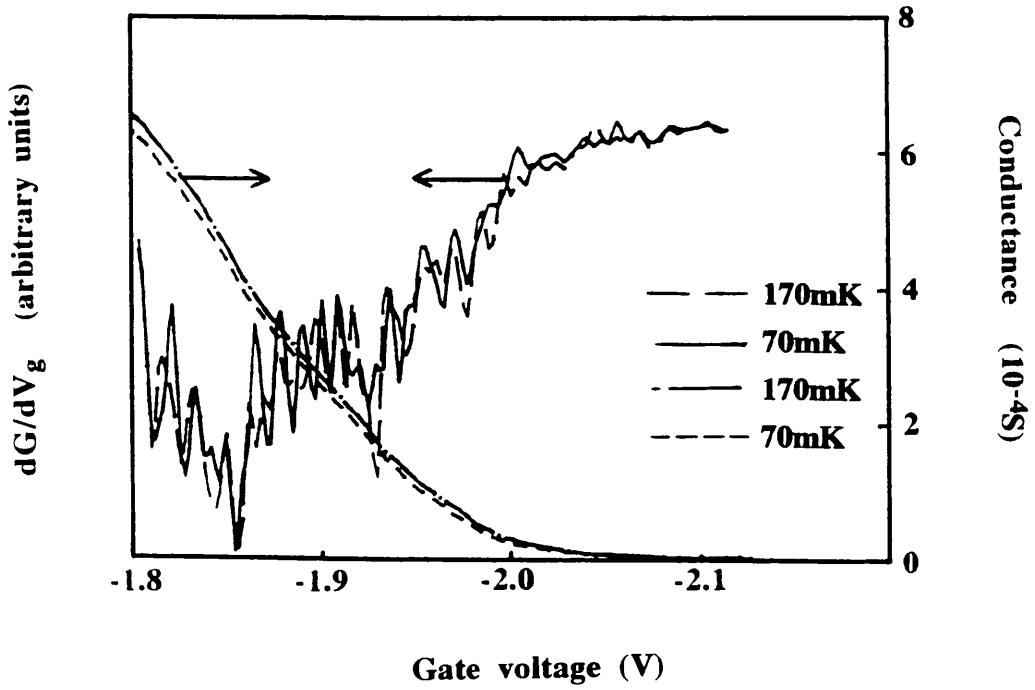
The conductance characteristics for this sample are shown in Graph 4.31(a). These display very similar features to those of A42532 which was also measured in the illuminated state only. The similarity of the characteristics suggests that the exposure to light produced the effects that are dominant in the sample.



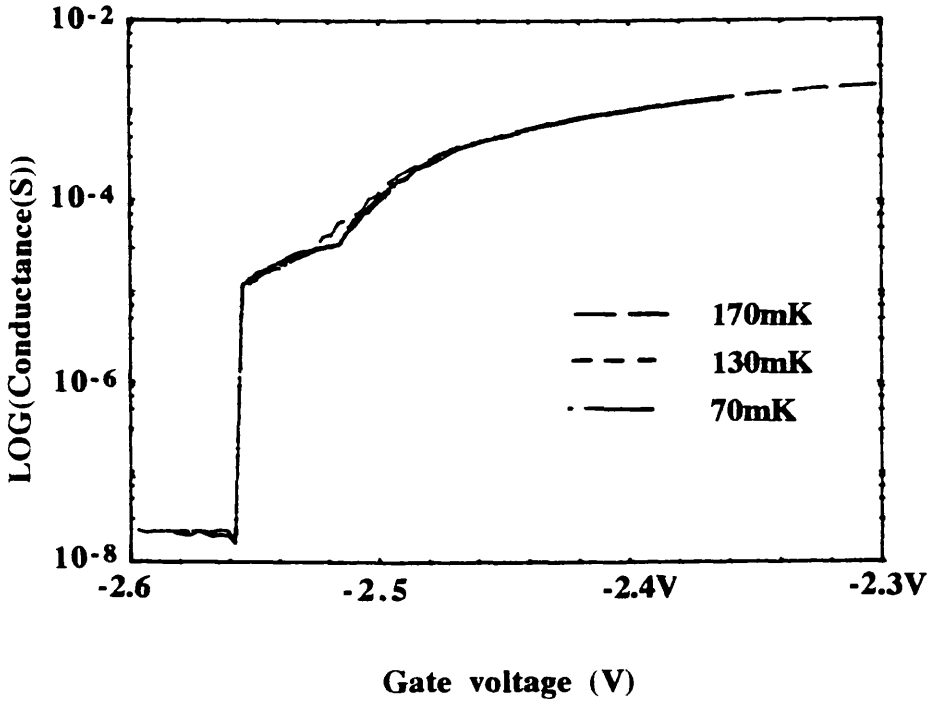
Graph 4.29(a): Conductance characteristics in cut-off region, for A42529 (wire) at 80mK.



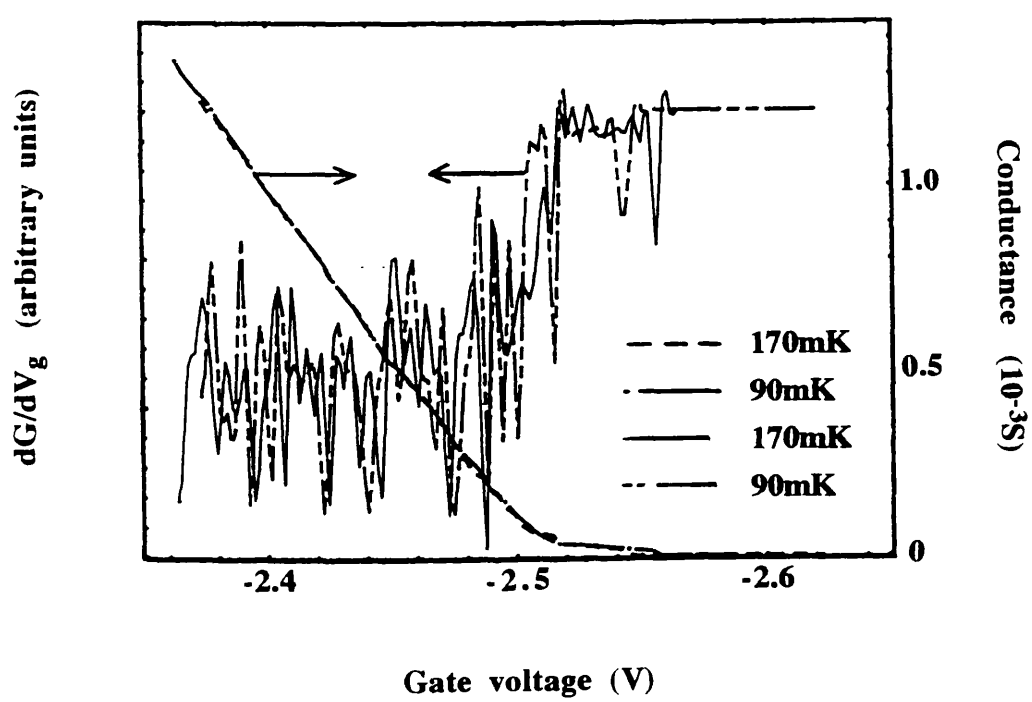
Graph 4.29(b): Conductance characteristics in cut-off region, for A42529 (wire) as a function of temperature.



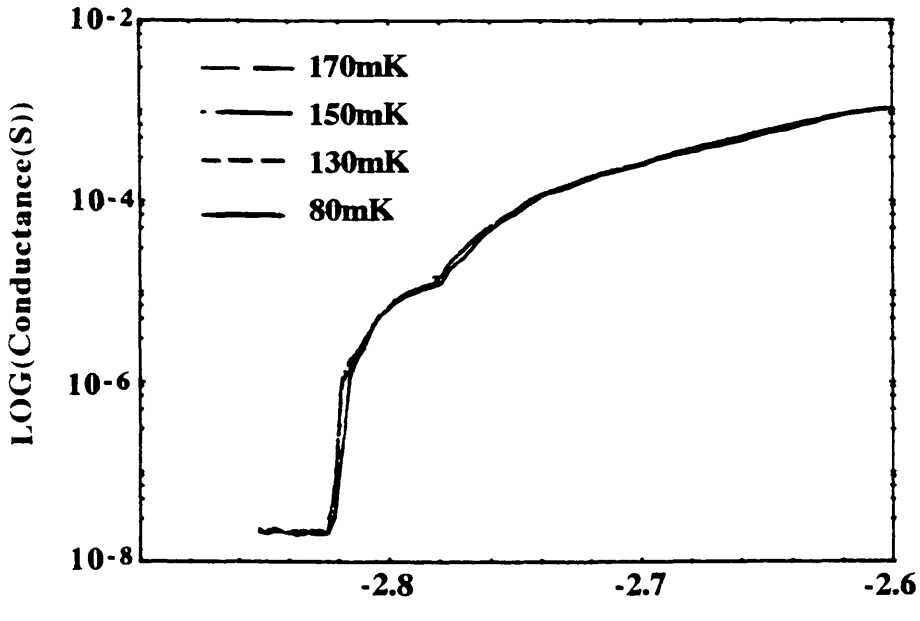
Graph 4.29(c): Conductance characteristics in cut-off region, for A42529 (wire) as a function of temperature, and derivative with respect to gate voltage.



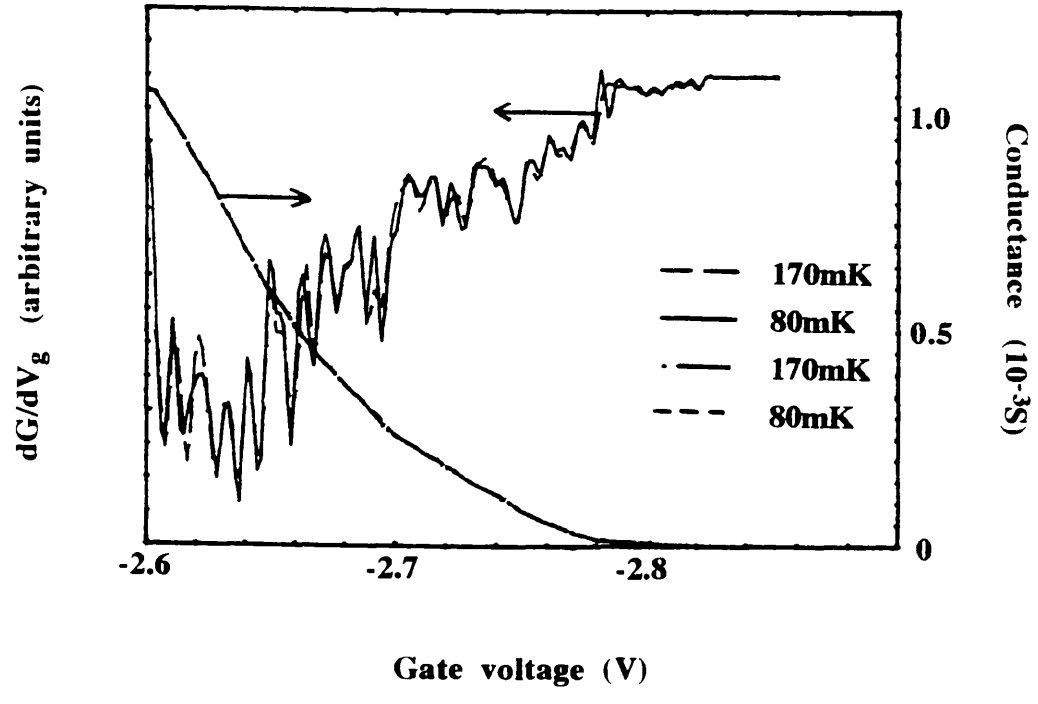
Graph 4.30(a): Conductance characteristics in cut-off region for A42532 (wire) as a function of T.



Graph 4.30(b): Conductance characteristics in cut-off region for A42532 (wire) as a function of T, and derivative with respect to gate voltage.



Graph 4.31(a): Conductance characteristics in cut-off region for A42531 (wire) as a function of T.



Graph 4.31(b): Conductance characteristics in cut-off region for A42531 (wire) as a function of T, and derivative with respect to gate voltage.

The derivative with respect to the gate bias is given in Graph 4.31(b). From this it can be seen that, as with A42529, there is some degree of correlation between the various derivatives, but again no clear period.

(b) Summary of low T conductance data

The most significant feature of the investigation of the low T conductance in the cut-off regions of the devices is that there is no temperature dependence of the conductance in the cut-off region, which proves conclusively that there are no temperature assisted hopping effects, no temperature dependent potential fluctuation effects, and with the exception (possibly) of A21611 no sub-band effects in this limit.

The other main feature of the data is that the wire characteristics of samples fabricated on both A216 and A425 were shown consistently to display three definite periods when measured in the dark, whereas the FET characteristic was somewhat more gradual. It is proposed that this is a reflection of the difference in the methods of depletion, which for the wire samples was lateral in nature and for the FETs was planar. The A425 sample wire characteristics measured in the light were also seen to be consistent, but cut-off more rapidly than the dark state characteristics. It should be noted that the conductance characteristics for A42531 and A42532 are very similar, which, given the obvious difference of the capacitance characteristics, is surprising.

4.7 COMPARISON OF CONDUCTANCE AND CAPACITANCE CHARACTERISTICS

In this section the conductance and capacitance characteristics of devices fabricated on both A216 and A425 will be compared and discussed. This discussion will be presented in two sub-sections, the first of which will be concerned with the comparative behaviour of the capacitance and conductance characteristics in the cut-off region as a function of temperature, and the second with conductance and capacitance data at low temperatures over the full gate voltage range.

4.7.1 COMPARISON OF CONDUCTANCE AND CAPACITANCE CHARACTERISTICS NEAR CUT-OFF, AT TEMPERATURES IN THE RANGE 295K-14K

In this section the capacitance and conductance characteristics for A21611, a wire sample, and A21618, an FET, will be presented and discussed.

(a) Presentation of high T FET and wire capacitance and conductance characteristics

The conductance and capacitance data for A21618 at 295K and 15K are given in Graphs 4.32(a) and (b) respectively, from which it can be seen that the conductance of the sample remains finite when the capacitance is effectively 'off'. This effect is most obvious at 295K where the capacitance is effectively 'off' at -1.2V, but the conductance remains finite until -1.45V. The difference is reduced as the temperature is decreased.

The data for A21611 is shown in Graphs 4.33(a) and (b), which shows the conductance (on a LOG scale) and capacitance characteristics at 295K and 15K. It can be seen that, as with the FET sample, the conductance of the wire sample is measurable over five orders of magnitude, and remains measurable when the capacitance of the sample is effectively zero. Again this effect is reduced as the temperature is decreased.

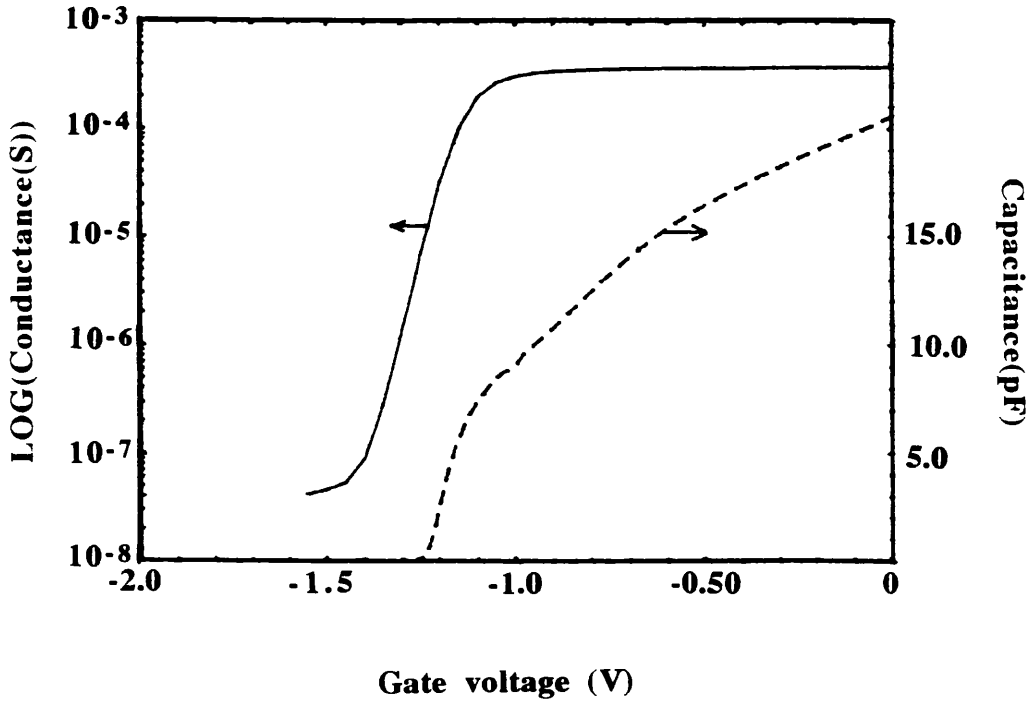
(b) Discussion of high T conductance and capacitance characteristics.

In all of the samples measured at high temperatures the discrepancy between the capacitance and conductance data seen in Graphs 4.32 and 4.33 was observed. This effect is due to both the nature of the capacitance measurement and the low electron mobility at high temperatures. From the discussion in Section 4.4.2(c) it was shown that the parallel capacitance, C_P, can be expressed as,

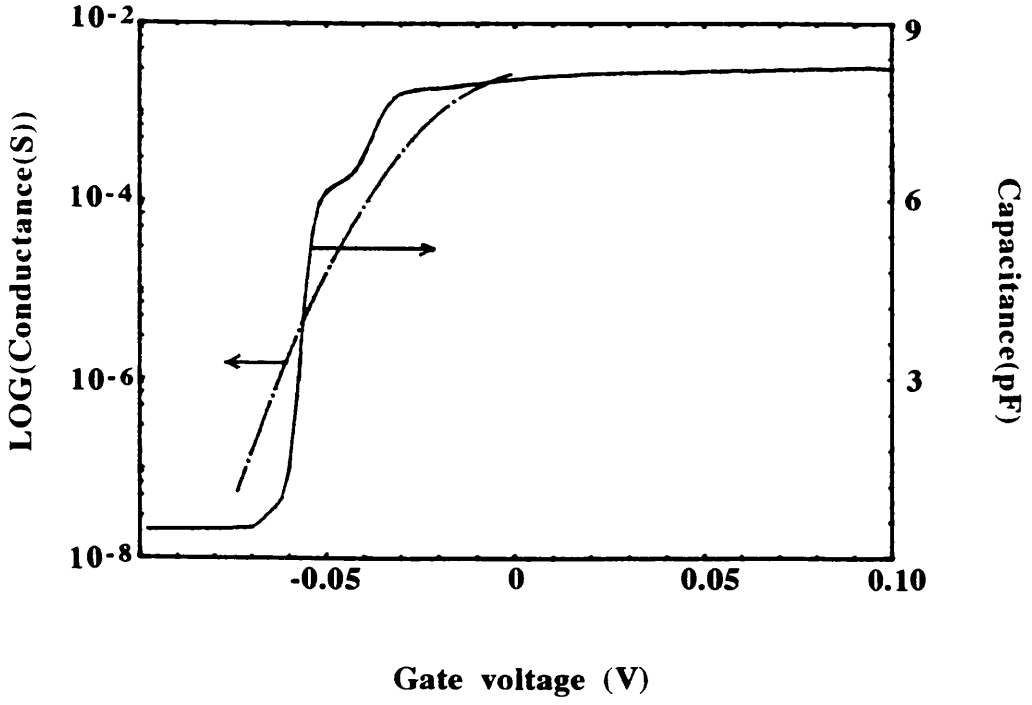
$$C_P = \frac{C_S g_S^2}{\omega^2 C_S^2 + g_S^2} \qquad (4.4)$$

At high temperatures electron mobility, and hence conductance, is low. If the mobility is sufficiently low in the cut-off region then the limits $g_S \sim \omega C_S$ and $g_S << \omega C_S$ may be realised. In these limits the parallel capacitance is dependent on the measurement frequency, the higher the frequency used the lower the magnitude of the parallel capacitance. Therefore at 'high' frequencies, and 'low' conductances, the capacitance may cut-off due to frequency effects, arising as a result of the measurement technique employed, rather than due to the total depletion of the samples.

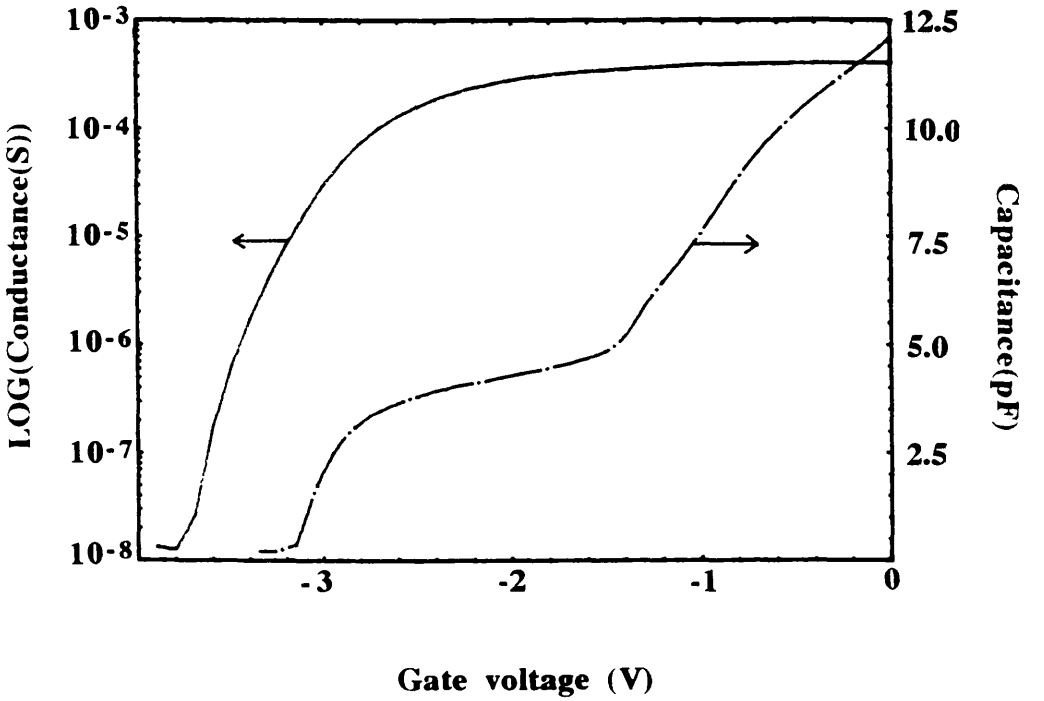
For A21611 the characteristics presented were measured at 100kHz, which is in the 'high' frequency limit for this sample at 15K. The conductance and capacitance characteristics, measured at 10kHz, 40kHz and 100kHz, are plotted in Graph 4.34, which shows that as the frequency is reduced the capacitance cut-off voltage moves closer to that of the conductance, until at 10kHz there is no apparent difference. This illustrates that it is the measurement frequency, as well as the low sample conductivity, which gives rise to the discrepancy between the capacitance and conductance



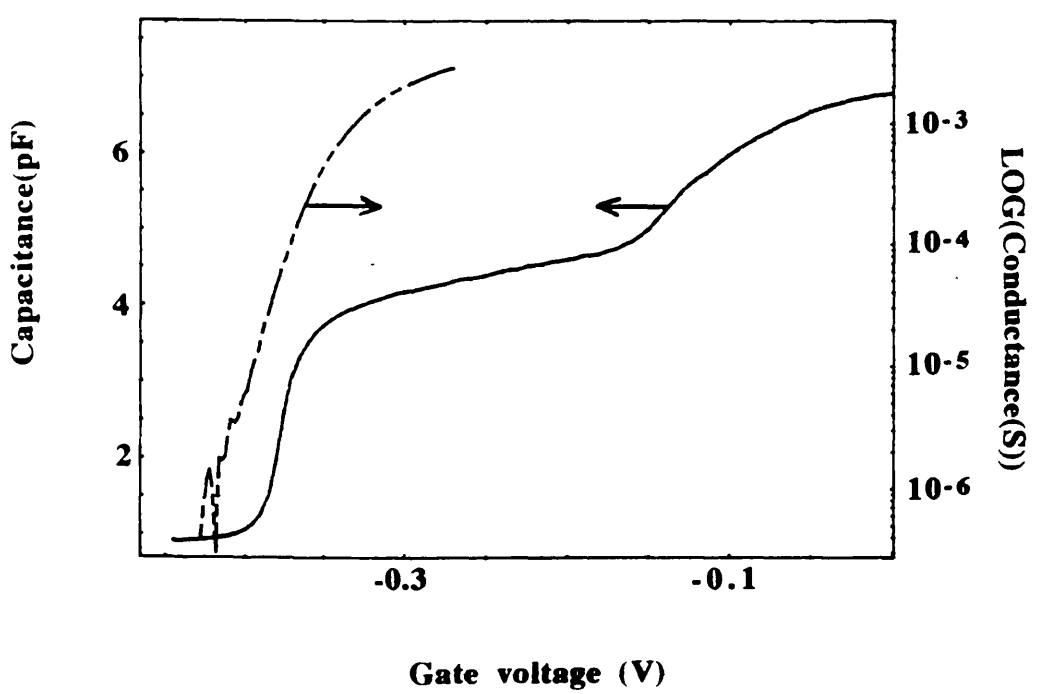
Graph 4.32(a): Capacitance and conductance characteristics for A21618 at 295K.



Graph 4.32(b): Capacitance and conductance characteristics for A21618 at 15K.



Graph 4.33(a): Capacitance and conductance characteristics for A21611 at 295K.



Graph 4.33(b): Capacitance and conductance characteristics for A21611 at 15K.

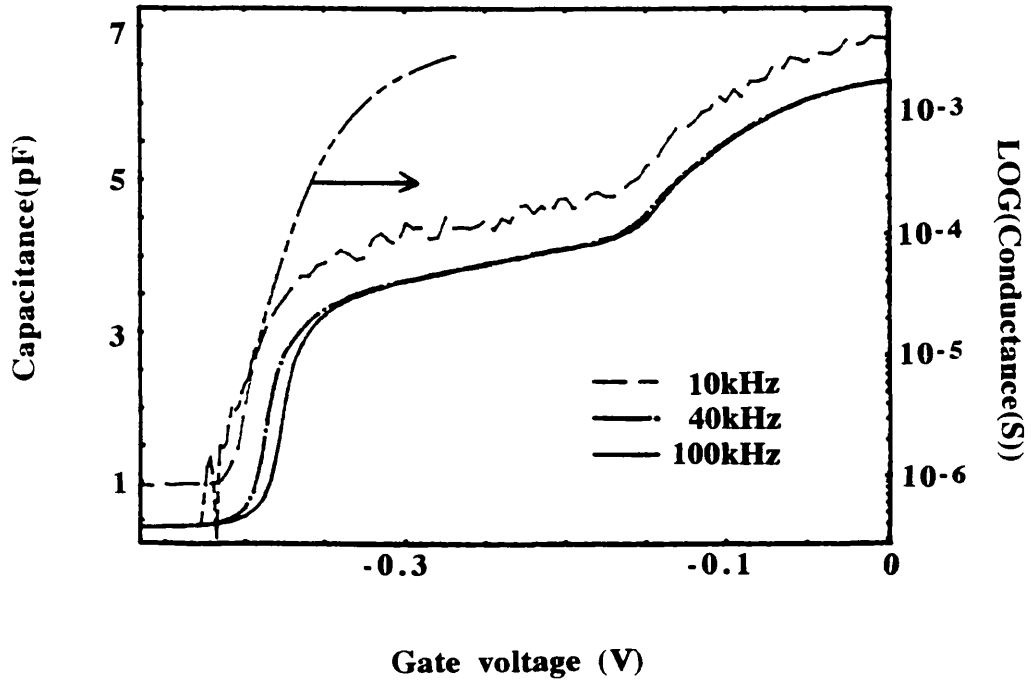


Figure 4.34: Conductance and capacitance characteristics for A21611 (wire) at 15K, with the capacitance measured at 10kHz, 40kHz and 100kHz.

measurements. The argument is further strengthened by the fact that samples with capacitance characteristics independent of frequency never display this difference.

It should be noted that none of the wire samples measured at temperatures below 4.2K displayed any frequency dependent effects in the capacitance data.

4.7.2 COMPARISON OF CAPACITANCE AND CONDUCTANCE CHARACTERISTICS AT LOW TEMPERATURES

The characteristics for two samples will be presented in this section, namely A42531 and A42532, for which the characteristics are shown in Graphs 4.35(a) and (b) respectively.

It can be seen that for both samples the conductance characteristics reflect the same features as the capacitance characteristics. It is significant to note that for A42532 where there is an obvious step in the capacitance there is a corresponding change in the conductance, which suggests that either the conductance measurement is sensitive to electrons in the conduction band in the AlGaAs or the step in the capacitance is is due to effects in the 2DEG. This step in the capacitance and conductance characteristics of A42532 will be discussed in Chapter 6.

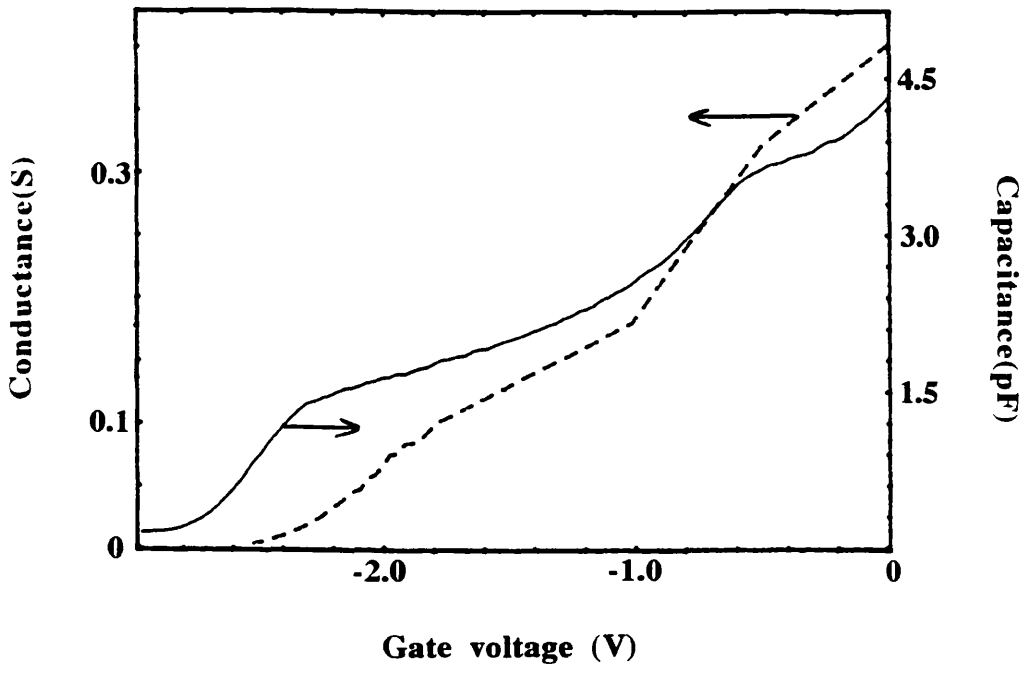
At this stage it is not possible to discuss the conductance data fully as it is dependent not only on the sample geometry and the carrier concentration but also the electron mobility. Therefore this data will be discussed more fully in Chapter 5 after the presentation of the magnetoresistance data, which allows the carrier concentration to be estimated and reduces the number of unknown variables in the problem.

4.8 QUANTITATIVE DISCUSSION OF CAPACITANCE CHARACTERISTICS OF FET SAMPLES

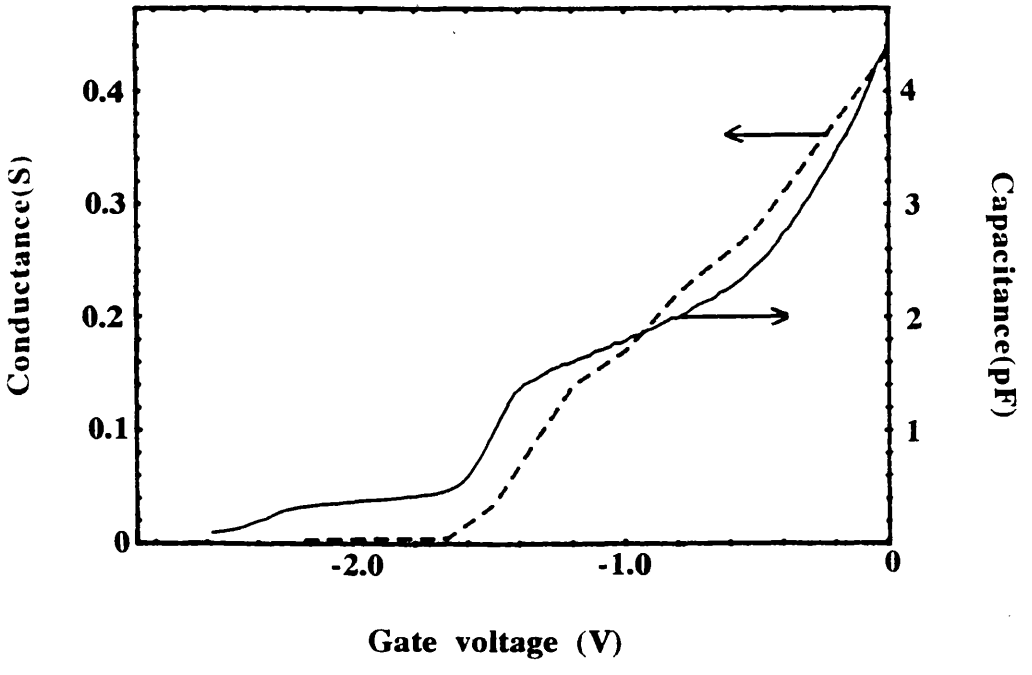
In this section the FET capacitance characteristics will be discussed. The arguments presented will attempt to explain the main features of the capacitance characteristics. Firstly, a model of heterostructures will be presented.

4.8.1 MODEL OF HETEROSTRUCTURES

It is difficult to predict the quantitative behaviour of heterostructures. However, in the following section a model to quantify the high and low temperature threshold voltages will be presented. From the data presented in Section 4.2 it can be seen that DX centres play a vital role in determining the the number of electrons in a 2DEG, so it



Graph 4.35(a): Capacitance and conductance characteristics for A42531 at 70mK.



Graph 4.35(b): Capacitance and conductance characteristics for A42532 at 70mK.

is essential that a model of a heterostructure at low temperatures should consider the effects of these deep traps.

Consider firstly a standard heterostructure at high temperatures, shown overleaf in Band diagram 4.1.

In the subsequent diagrams and analysis, energy is denoted by E, electric fields by ξ, and ΔE_c is the conduction band offset between GaAs and AlGaAs. The effective width of the 2DEG is a_0 (approx. 10nm) and the relative permittivity of GaAs and AlGaAs are assumed to be the same and equal to 13.

At high temperatures donors in the doped AlGaAs layer can be ionised if they are above the Fermi energy. To calculate the threshold voltage for an FET it is necessary to consider fully the fields and energy in the system.

Consider the conservation of energy in the heterostructure. The potential energy at the surface of the system should equal the sum of all the other potential energies. This implies that, relative to E_f,

$$\underbrace{E_c(0)}_{\text{conduction band energy at z=0}} = \underbrace{e\xi_0 c}_{\text{drop in energy across GaAs cap}} + \underbrace{\Delta E_c}_{\text{energy band discontinuity at GaAs/AlGaAs interface}} - \underbrace{eV_{c-c+d}}_{\text{change in potential energy across dopedAlGaAs layer}} + \underbrace{e\xi_1 s}_{\text{energy dropped across AlGaAs undoped spacer layer}} - \underbrace{\Delta E_c}_{\text{energy band discontinuity at AlGaAs/GaAs interface}} + \underbrace{e\xi_1 a_0}_{\text{energy dropped across channel}} \tag{4.5}$$

The conduction band discontinuity at the GaAs/AlGaAs interfaces cancel leaving only three terms in this equation. From Gauss's law V_{c-c+d} is given by,

$$V_{c-c+d} = \int_c^{c+d} \xi_z dz \tag{4.6}$$

where,

$$\xi_z = \xi_1 - \frac{N_D e(c+d-z)}{\varepsilon} \tag{4.7}$$

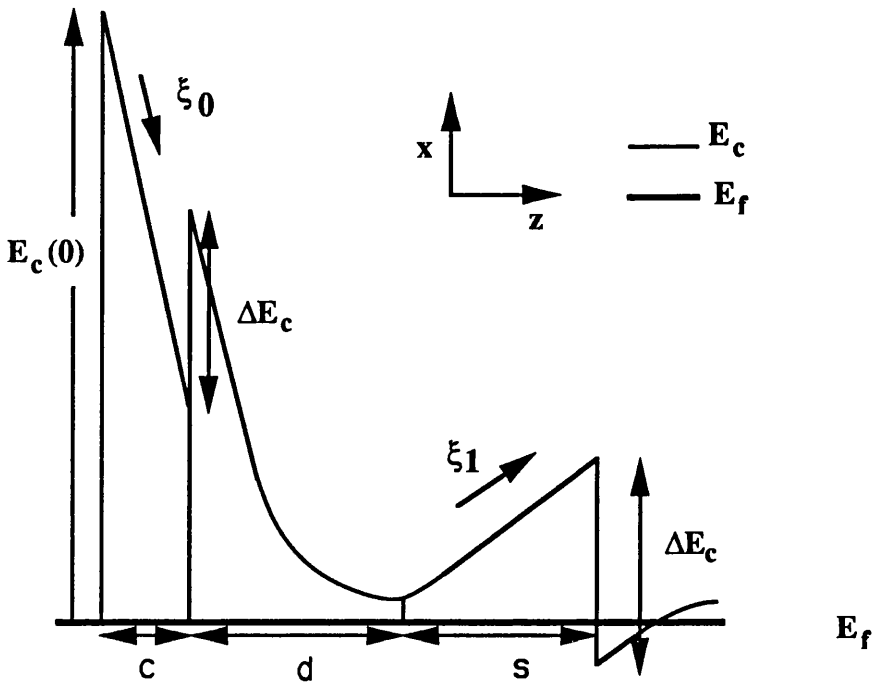
and,

$$\xi_1 - \xi_0 = \frac{e\int N_D dz}{\varepsilon} = \frac{eN_D d}{e} \tag{4.8}$$

where N_D is the dopant concentration in the doped AlGaAs layer. This assumes that the number of donors is sufficiently low so that no charge is stored in the AlGaAs. ξ_1 can also be described in terms of the 2DEG carrier concentration n_{2d},

$$\xi_1 = \frac{en_{2d}}{\varepsilon} \tag{4.9}$$

Combining these equations gives



Band diagram 4.1: Band diagram for an undepleted GaAs/AlGaAs heterostructure at high temperatures where DX centres are active.

$$E_c(0) = -e\xi_1(c + d + s + a_0) + \frac{eN_D d}{\varepsilon}\left(\frac{d}{2} + c\right) \quad (4.10)$$

where $E_C(0)$ includes the potential due to the gate voltage and the surface pinning, that is,

$$E_c(0) = -eV_g + eV_s \quad (4.11)$$

where V_S is the surface pinning potential, assumed to be 0.7V.

If a negative voltage is applied to the gate sufficient to remove electrons from the channel then, from Equation 4.9, ξ_1=0, so the potential energy at the surface at cut-off, E'(0), is given by,

$$E'_c(0) = \frac{eN_D d}{\varepsilon}\left(\frac{d}{2} + c\right) \quad (4.12)$$

which, using Equation 4.11, enables an estimate of the threshold voltage to be made.

This model gives reasonable values for the threshold voltage at high temperatures. Applying Equation 4.12 to the A216 samples, and assuming that the surface potential is 0.7V, predicts a room temperature voltage cut-off at -1.6V. From Graph 4.32(a) it can be seen that for A21618 the cut-off voltage of the conductance characteristic is at -1.45V.

A further expression for the threshold voltage is given below,

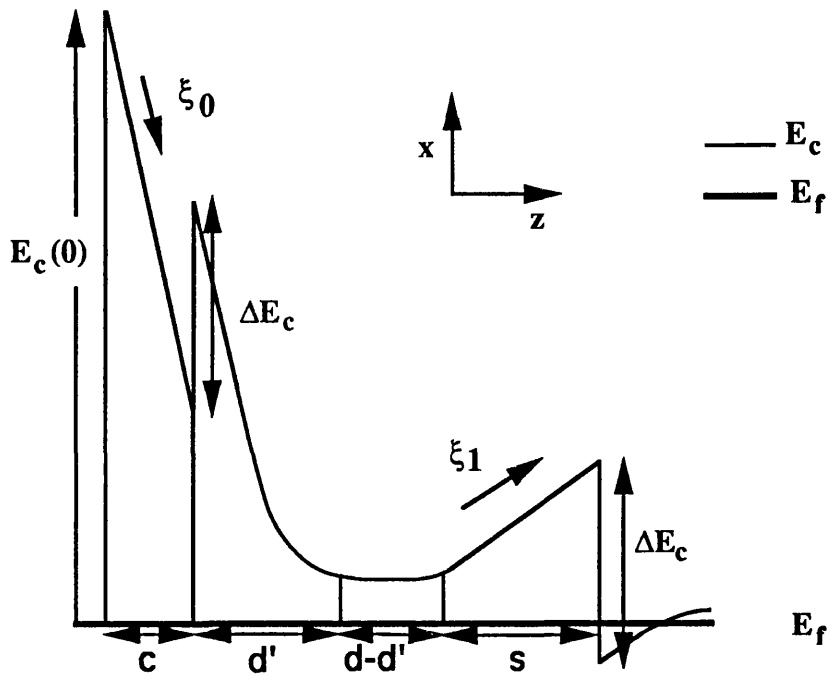
$$E'_c(0) - E_c(0) = e\xi_1(c + d + s + a_0) \quad (4.13)$$

Although this model may not correctly describe the charge stored in the AlGaAs it will always be correct near the cut-off voltage as at that point the donor centres are fully depleted. However, at low temperatures a model of this type is unsuitable for predicting the threshold voltage as it does not take into account the effects of charge trapping in the DX centres. The energy band diagram for a heterostructure at low temperatures in which DX trapping of charge is significant is given overleaf in Band diagram 4.2.

The effective width of the doped region, d in the previous section, is now reduced to d' as the result of electron trapping in DX centres in the doped AlGaAs, with the remainder of the doped layer (d-d') containing no net charge, and therefore, at 0V on the gate, no internal field. It should be noted that, by conservation of charge, this implicitly requires the presence of a region of space charge at the interface between the doped AlGaAs layer and the undoped spacer layer, equal and opposite in magnitude to the free charge in the channel.

For the purposes of this model it is assumed that, at the DX freezing temperature and below, the separation of the Fermi energy and the conduction band edge is pinned close to the net energy of the DX trap, E_{DD}. Therefore,

$$E_{DD} \approx -e\xi_1(s + a_0) + \Delta E_c \quad (4.14)$$



Band diagram 4.2: Band diagram for undepleted GaAs/AlGaAs heterostructure at low temperatures with DX centres occupied.

Following the approach used in the previous section, the potential energy equation is now,

$$E_c(0) = -e\xi_0 c - eV_{c-c+d'} + e\xi_1(s + a_0) \qquad (4.15)$$

where,

$$V_{c-c+d'} = \frac{eN_D d'^2}{2\varepsilon} \qquad (4.16)$$

and,

$$\xi_0 = \frac{eN_D d'}{\varepsilon} \qquad (4.17)$$

with neither (4.18) nor (4.19) containing ξ_1 terms, as the field in the range d' to d is now zero. This gives the energy equation as,

$$E_c(0) = -e\xi_1(s + a_0) + \frac{eN_D d'}{\varepsilon}\left(c + \frac{d'}{2}\right) \qquad (4.18)$$

Now consider the band diagram for the system at cut-off when there are no electrons in the channel which is given overleaf in Band diagram 4.3.

The electric field in the region (d-d') is now necessarily $-\xi_1$ as a result of the space charge at the interface between the spacer layer and the doped layer. The field in the spacer layer is zero when there are no electrons in the channel.

Again, summing over the various potentials in the system, it can be shown that the potential energy at the surface $E'_c(0)$, at cut-off, can be given by,

$$E'_c(0) = \xi_1(c + d) + \frac{eN_D d'}{\varepsilon}\left(c + \frac{d'}{2}\right) \qquad (4.19)$$

Therefore the net potential energy required on the gate to deplete the channel is given by,

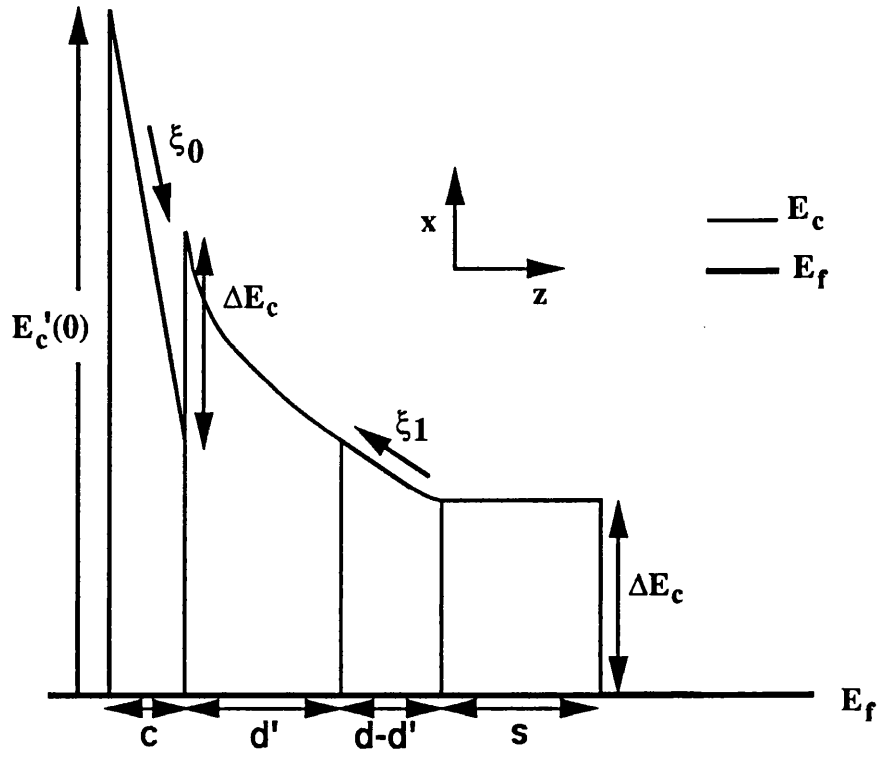
$$E'_c(0) - E_c(0) = e\xi_1(c + d + s + a_0) \qquad (4.20)$$

From equation (4.16) relating ξ_1 to physical sample constants it can be seen that,

$$E'_c(0) - E_c(0) = -e(c + d + s + a_0)\frac{(\Delta E_c - E_{DD})}{(s + a_0)} \qquad (4.21)$$

Thus the cut-off potential at low temperatures, assuming that DX centres are passive, can be expressed solely in terms of the physical constants of the heterostructure, thereby enabling an estimate of the threshold voltage of an FET at low temperatures to be made with no prior knowledge of the carrier concentration.

For the samples used in this project, using ΔE_C=0.23eV, and E_{DD}=0.07eV, this predicts -0.4V as the cut-off voltage at low temperatures. This is in very good agreement with several of the samples measured, for example A21618, which cuts-off at -0.4V; and in qualitative agreement with the others, for example, A42531 which displays an FET cut-off at -0.6V.



Band diagram 4.3: Band diagram for fully depleted GaAs/AlGaAs heterostructure at low temperatures with DX centres occupied.

4.8.2 MAGNITUDE OF FET CAPACITANCE

The magnitude of the capacitance, C, of an FET, with no parallel conductance, can be found by using Equation 4.13 (and, equally, 4.20). These equations express the total potential energy required to deplete the channel fully. The expression for C is given by,

$$C = \frac{dq}{dV} = \frac{d(en_{2d})}{dV_g} \qquad (4.22)$$

From equation 4.15 it can be shown that,

$$C = \frac{\varepsilon A}{(c + d + s + a_o)} \qquad (4.23)$$

where A is the area of the gate and the other terms are as defined in the previous section. This is the standard expression for the capacitance of a parallel plate capacitor.

The magnitudes of the capacitance from various sample characteristics, C_{exp}, are given in Table 4.2 with the theoretical value, C_{theor}, predicted from the geometry, with the width of the 2DEG, a_o, assumed to be 10nm, and ε_r=13.

Sample number	T(K)	gate length(μm)	gate width(μm)	C_{exp}(pF)	C_{theor}(pF)
A21610	15	380	17	8.0	6.4
A21663	15	360	17	7.2	6.0
A21613	15	380	17	8.8	6.4
A21627	15	380	17	8.0	6.4
A21668	4.2	420	17	6.7	7.0
A21618	15	420	17	8.0	7.0
A21618	0.08	420	17	6.9	7.0
A21615	0.04	420	17	6.9	7.0
A42522	15	420	17	5.8	7.0

Table 4.2 Capacitance magnitudes for FET samples

From Table 4.2 it can be seen that for A216 the magnitude of the capacitance for characteristics measured at 15K is consistently higher than the predicted value, whereas the low temperature data is consistently lower than the predicted value,

although within experimental error. The reason for the high values of the capacitance at 15K is not fully understood, as from a simple circuit analysis of the system the magnitude of the capacitance is the series combination of the capacitance of the AlGaAs and the capacitance of the channel, and therefore should never be higher than the value predicted from the sample geometry.

The data for A42522 at 15K is lower than the predicted value, which does not fit into the pattern seen in the A216 samples. This suggests that the separation between the gate contact and the 2DEG in A425 is somewhat larger than expected from the nominal material geometry. This can be explained by considering the effect of an interfacial layer between the surface of the GaAs cap and the Schottky gate, introduced in the fabrication process, after Schubert, Ploog et al, 1984. This layer will have a different permittivity from that of the GaAs/AlGaAs layers. The total separation of the gate and the 2DEG, l_R, is then given by,

$$l_R = W + c + d + s + a_o \qquad (4.24)$$

where W is the thickness of the interfacial layer. However, capacitance measures not only the depth but the relative permittivities of the dielectric layers, so the depth implied by the magnitude of the capacitance, l_c, is in fact,

$$l_c = \frac{\varepsilon}{\varepsilon_1} W + c + d + s + a_o \qquad (4.25)$$

where ε_1 and ε are the permittivities of the interfacial layer and the AlGaAs layers respectively. It is difficult to quantify l_R as neither ε_1 nor W are known. However, from the measured capacitance on A42522, l_c is approximately 145nm for this material. This apparent interfacial layer in A425 samples causes problems for the later analysis of the capacitance characteristics of the wire samples fabricated on A425.

4.9 QUANTITATIVE DISCUSSION OF CAPACITANCE CHARACTERISTICS OF WIRE SAMPLES

In this section the magnitude of typical wire capacitance characteristics, the charge distribution in the wire samples and the threshold voltages will be discussed. These will be discussed with reference to the low temperature data only.

4.9.1 MAGNITUDE OF CAPACITANCE OF WIRE SAMPLES

The magnitude of the capacitance is determined by the geometry of the sample and the electron density of states in the 2DEG, or the wire. To calculate the capacitance of the wire samples as a function of gate voltage requires the solution of a two dimensional Poisson-Schrodinger equation. This is a major computational task for which there was insufficient time in the course of this project. However, it is possible

to make an order of magnitude estimate of the capacitance of wire samples by assuming that the capacitance is dominated by the geometrical effects. In this case it is necessary to solve only Laplace's equation for the wires by treating the surface potential as being one electrode in the system and electrons in the 2DEG as another, and assuming that the charge state in the intervening layers remains unaltered by the perturbation.

T. Luffingham, a project student, developed a program to allow the magnitude of the capacitance to be estimated. This calculation basically solved Laplace's equation for the wire systems. The program allowed the width of the wire to be varied and regions of different permittivity to be treated. The calculation was performed for a single wire, represented by half the wire and half the gap, which, due to the symmetry, could be scaled up to the complete device. The geometry used is shown in Figure 4.2.

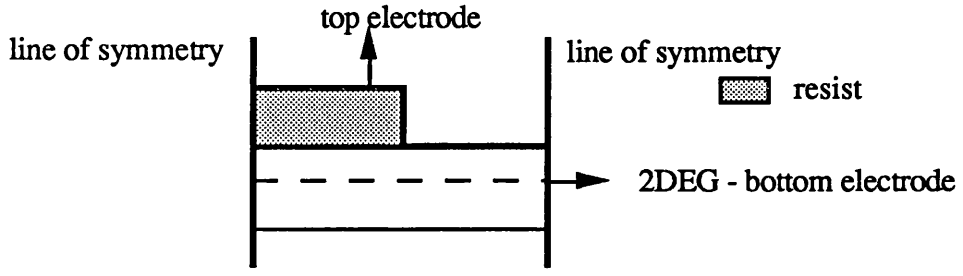


Figure 4.2 Geometry used for Laplace solver

The width of the top electrode was not varied, but the width of the lower electrode, representing the electrons in the wire as an equipotential plane, was, and the capacitance calculated around a fixed potential. This allowed a measure of the capacitance as a function of the wire width. The maximum grid size for the geometrical representation of the wire was 50 by 80 boxes, which limited the resolution. The magnitude of the capacitance was calculated for all the samples measured, but only the results for A21611 and A42531 will be discussed. The wire capacitance, normalised to the FET capacitance, calculated from the theoretical data for given channel widths for both samples is given in Table 4. 3. The absolute thickness of the resist, R, was not known, so the capacitance was calculated at the lower and upper limits of 100nm and 200nm respectively.

A21611			A42531		
width of channel (nm)	C_W/C_F for R = 100nm	C_W/C_F for R = 200nm	width of channel (nm)	C_W/C_F for R = 100nm	C_W/C_F for R = 200nm
1200	0.67	0.69	1000	0.74	0.85
1000	0.61	0.63	800	0.59	0.66
800	0.55	0.50	600	0.52	0.51
580	0.33	0.34	440	0.39	0.38
400	0.22	0.24	300	0.29	0.28
200	0.16	0.17	200	0.23	0.22
100	0.13	0.14	100	0.19	0.18

Table 4.3 Magnitude of capacitance for wire samples A21611 and A42531, estimated from solution of Laplace's equation

To relate this to the experimental data it is easiest to pick out specific features on the capacitance characteristics. For example, the magnitude of the wire capacitance when the system is undepleted, the magnitude of the wire capacitance when the wires are just formed and the magnitude of the wire capacitance just before the cut-off.

The width of the wires for A21611 was 580nm and the wire separation was 620nm and so was repesented by a grid of size 29 by 60 boxes, with each box equal to 10nm. The relative permittivity of the resist and the AlGaAs were taken to be 2.0 and 13 respectively. For A21618 the FET capacitance, C_F, is 6.9pF. For the wire sample A21611 the capacitance at zero volts, C_0, is 4.8pF, the capacitance when the wires are just formed, C_A, is 2.8pF and finally the capacitance at the start of the cut-off, C_C, is 1.4pF. Normalising this to the FET capacitance gives the following ratios, C_0/C_F=0.70, C_A/C_F=0.41, C_C/C_F=0.20. Comparing these values with those estimated from the Poisson equation shows that at 0V where the channel is undepleted the agreement is quite good. The experimental value is 0.70 and the calculated values are 0.67 and 0.69. This agreement indicates that in this limit the original assumption that the main contribution to the capacitance is the sample geometry, and sub-band effects can be ignored is valid. The width at which the wires are formed is approximately the geometrical width of the resist. The calculations indicate that at C_A/C_F=0.44 the width of the bottom electrode is about 700nm -considerably larger than the width of the resist. For C_C/C_F=0.22 the calculations imply a width of 400nm. There is clearly a problem with the analysis, as this data suggests that when the

capacitance characteristics are indicating the wires are nearly depleted the calculations imply that the wires are barely formed.

The width of the wires for A42531 was 430nm with the wire separation 560nm. The capacitance data for A42531 was as follows: C_F=5.8pF, C_0=3.7pF, C_A=2.6pF, and C_C=1.2pF, with the experimental ratios now C_0/C_F=0.64, C_A/C_F=0.45, and C_A/C_F=0.20. The calculated value for the full channel is C_0/C_F=0.74, which is somewhat higher than observed experimentally. For the other ratios the widths implied by the calculations are about 500nm when the wires are formed and 100nm at the wire cut-off. As with A216 this shows that the calculation implies that the wire widths are higher than the geometry suggests should be possible. However, the agreement between the experimental and calculated values for this sample can be improved because of the suspected presence of an interfacial layer between the gate and the GaAs cap which lowers the capacitance in the region below the gate but does not affect the capacitance in the wire region. If the expected value of the FET capacitance, C_F=7.0pF, is used to normalise the capacitance in the wire region then the ratios become, C_A/C_F=0.38 and C_A/C_F=0.17, which correspond to channel widths of 440nm and <100nm. The lithographical width of the wires is 430nm so these values are in good agreement with expected widths

In conclusion, for A21611 there is a major discrepancy between the capacitance measurements and the calculated values. The calculations suggest that either the sample geometries are wildly inaccurate or there is a significant amount of charge being sensed by the capacitance measurement which is not in the 2DEG region. However, for A42531 the agreement is reasonable, for both values of the FET capacitance. The reason for the model being applicable for one sample, but not the other is not fully understood as the sample dimensions are similar.

4.9.2 CALCULATION OF N_{2d} USING CAPACITANCE CHARACTERISTICS

Capacitance measurements allow the total charge in a system to be estimated. The standard expression for capacitance, C, is,

$$C = \frac{\partial Q}{\partial V} \tag{4.26}$$

where Q is the total charge, and V is the potential applied to remove the charge Q. For FETs and wire samples the expression becomes,

$$C = \frac{\partial Q}{\partial V_g} \tag{4.27}$$

Capacitance measurements not only give the magnitude of the charge but also a spatial profile of charge.

From the temperature dependence of the capacitance it was deduced that charge was trapped in the doped AlGaAs layer. From the hysteresis experiments it was shown that this charge cannot communicate with the channel. Therefore the only apparent charge sensed by the capacitance measurement is in the conduction band in either the AlGaAs or the 2DEG. In theory this enables a direct measure of the free electron concentration. If there is no charge in the conduction band in the AlGaAs then the carrier concentration in the 2DEG can be estimated by integrating the C-V_g curve. For the wire samples it is necessary to treat the capacitance characteristic as having two distinct regions, the 'FET' (or gated) region and the wire region, which is the area beneath the resist.

From the capacitance characteristics the charge in the region under the gate, Q_F, and the charge in the region under the resist, Q_W, can be found using,

$$Q_{tot} = A_{tot} = Q_F + Q_W \qquad (4.28)$$

where Q_{tot} is the total charge, and A_{tot} is the total area under the capacitance characteristic. From Graph 4.5 it can be seen that the FET cut-off voltage for A21611 is at -0.4V, so

$$Q_F = A_{0 \rightarrow -0.4} \qquad (4.29)$$

where $A_{0--0.4}$ is the area of the graph in the voltage range 0V to -0.4V. The wire cut-off voltage is at -1.6V, so Q_W for A21611 is

$$Q_W = A_{-0.4 \rightarrow -1.6} \qquad (4.30)$$

The carrier concentration, n_{2d}, can then be found using,

$$n_{2d} = \frac{A_V}{eS}\frac{p}{w} \qquad (4.31)$$

where A_V is the area under the graph in the voltage range 'V', S is the total gate area, p is the sum of the width of the resist and the width of the gate in contact with the surface and, finally, w is the width of which ever of the two regions is of interest.

The areas under the capacitance characteristics were computed using the software package "Easyplot". For A21611, S=7140μm^2 and p=1100nm. For A21611 in the FET region, where w=620nm, the estimated carrier concentration is $2.9 \times 10^{15} m^{-2}$. In the wire region, where w=580nm, n_{2d} is estimated to be $4.0 \times 10^{15} m^{-2}$. Again this suggests that the charge in the wires measured by the capacitance is higher than expected. This is a significant difference which cannot be wholly attributed to errors in the sample dimensions. The results from some of the samples discussed in this chapter are given in Table 4.4.

Sample no.	wire width(nm)	wire sep.(nm)	(V_c) - FET cut-off (V)	(V_c') - wire cut-off (V)	n_{2d} from charge in wire ($10^{15}m^{-2}$)	n_{2d} from charge in gate ($10^{15}m^{-2}$)
A21612	340	525	-0.08	-0.34	1.0	0.4
A21668	750	400	-0.17	-0.9	1.8	1.9
A21611	580	620	-0.4	-1.6	4.0	2.9
A21614	470	470	-0.09	-0.7	2.0	0.7
A42529	430	690	-1.0	-1.5	2.8	6.5
A42532 (dark)	570	600	-0.45	-1.2	3.4	3.1
A42532 (light)	570	600	-0.4	-2.7	2.9	2.0
A42531	430	560	-0.6	-2.3	7.1	3.5

Table 4.4 Table of carrier concentrations below the gate and below the resist(i.e. in the wire)

From Table 4.4 it can be seen that the other A216 samples follow the trend seen in A21611 , that is, the carrier concentrations estimated from the amount of charge in the wire regions tend to be significantly higher than those estimated from the gate regions.

From Table 4.4, it can be seen that not all of the A425 samples follow the trend displayed by the A216 samples. For A42529, the wires have a lower carrier concentration than the regions beneath the gate. However, for A42532, the two carrier concentrations are roughly the same, and for A42531 the carrier concencentration in the wire is higher than in the FET region. Interpreting the capacitance characteristics for the A425 samples is complicated by the fact that no control FET was measured, as it becomes difficult to decide which are the wire regions and which are the FET regions. This is compounded by the slightly irregular shape of the curves. Each of A42529 and A42532, when measured in the dark, exhibit a step in the capacitance characteristics. The A42531 characteristic, Graph 4.19(b), also displays this in its illuminated state, although somewhat less convincingly, at about -0.2V where the capacitance characteristic, having plateaued, then begins to rise.

These differences in the carrier concentration may be explained by considering the effect of the gate on the surface of the semiconductor. A 2DEG can be affected by the presence of a gate in two possible ways; the first being the reduction of the carrier concentration, and the second being the introduction of the electrons in the conduction band in the AlGaAs layer. The fact that the A216 and A425 samples display opposite trends merely reflects the fact that the A216 material was estimated to be partially depleted under the gate at 0V, thus giving lower carrier concentrations in the gated regions compared to those from the wire regions; whereas the A425 material in the region under the gate was thought to have extra charge in the conduction band in the AlGaAs, giving a higher carrier concentration in the gated region than in the wire region.

Consider A21618, where the FET cut-off voltage is -0.4V. From previous FETs fabricated on A216, with similar cut-off voltages, the conduction band in the AlGaAs starts to be populated at a bias of +0.15V. If this is taken as the maximum voltage, beyond which the 2DEG is no longer altered, then the estimate of the maximum carrier concentration found from the region under the gate is increased by an amount 0.15/0.4. This gives the carrier concentration as $(1+0.15/0.4).3.0\times10^{15}=4.1\times10^{15}m^{-2}$, which compares favourably with the estimate of $4.0\times10^{15}m^{-2}$ made from the wire region. It should be noted that it will not always be appropriate to use the voltage at which the conduction band in the AlGaAs begins to be populated as a reference voltage, although it works well in this case.

Now consider A42529. The voltage at which the carrier concentration under the gate is equal to the estimate from the wire region, $2.8\times10^{15}m^{-2}$, is -0.6V. It should be noted that this value may not be exact as there is ambiguity in the position of the FET cut-off which arises because the transition from the full 2DEG to isolated wires appears to be very gradual, unlike A21611, where the voltage at which the wires are formed is very definite. The capacitance characteristic indicates that there is charge in the conduction band in the AlGaAs in the voltage range 0 to -0.5V, so the fact that the magnitude of the charge in the wire region agrees well with that estimated from the capacitance in the range -0.6 to -1V, suggests that there is no such extra charge in the wires. This implies that it is the effect of the gate on the 2DEG which creates the conditions for charge to populate the conduction band in the AlGaAs. It is worth noting that the figures quoted for A42531 displayed the trend seen in the A216 samples because in the illuminated state the capacitance characteristic did not display the step seen in the other A425 characteristics, implying that in this sample there was no charge in the AlGaAs.

Although the carrier concentrations discussed above have been shown to be internally consistent, further problems arise when comparing the values of n_{2d},

calculated using the capacitance data, with estimates taken from later Shubnikov de Haas measurements. This is a serious problem and will be discussed fully in Chapter 6.

4.9.3 THRESHOLD VOLTAGE - EXPERIMENTAL AND THEORETICAL

In this section the observed experimental cut-off voltage and the predicted cut-off voltage will be compared.

The gate bias at which the wires are fully depleted, that is cut-off, can be estimated from the predictions of the Davies model, outlined in Section 1.6. From this

$$V_c' = V_c\left[1 - \tan^{-1}\left(\frac{z}{2l}\right)\right]^{-1} \qquad (4.32)$$

where V_c' is the wire cut-off voltage, V_c is the FET cut-off voltage, z is the width of the wire and l is the depth of the 2DEG below the surface.

The ratio V_c'/V_c was calculated for all the devices measured at low temperatures. The cut-off voltages were taken from the capacitance data as in several instances an FET sample was not available to pin-point the 2DEG cut-off voltage. It was found in practice that it was considerably easier to establish the FET cut-off voltage from the capacitance as opposed to the conductance data.

It should be noted that, for the A216 samples, there was generally no problem in identifying the exact voltage at which the wires were formed, so the respective cut-off voltages were taken as the voltages at which the FET, and then the wires were *totally* depleted. For example, for A21611, this gives the FET voltage as -0.4V and the wire cut-off voltage as -1.6V. For the A425 samples the transition from full 2DEG to isolated wires was much more difficult to estimate. Therefore, it was decided that the voltages at which the FET and wires started to cut-off fast would be used for the purposes of these calculations. For example, for A42531 in the illuminated state this means that the FET cut-off is taken as -0.6V, and the wire cut-off as -2.3V

The experimental and predicted values of (V_c'/V_c) are shown in Table 4. 5.

sample number	$(V_c)_{exp}$	$(V_c')_{exp}$	$\left(\frac{V_c'}{V_c'}\right)_{exp}$	$\left(\frac{V_c'}{V_c'}\right)_{theor}$
A21612	-0.08	-0.34	4.3	2.6
A21668	-0.17	-0.9	5.6	5.2
A21611 (low T)	-0.4	-1.6	4.0	3.9
A21614	-0.09	-0.7	7.7	3.4
A42529	-1.0	-1.5	1.5	3.1
A42532 (dark)	-0.45	-1.2	3.0	4.0
A42532 (light)	-0.4	-2.7	6.8	4.0
A42531	-0.6	-2.3	3.8	3.2

Table 4.5 Table showing calculated and experimental values for V_C'/V_C.

From Table 4.5 it can be seen that some of the experimental and theoretical data is in reasonable agreement. However, there are a few samples for which the agreement is very poor, e.g., A21614 and A42529. The explanation for this lies in an implicit assumption made in the Davies calculation, which is that at 0V on the gate the carrier concentration is uniform across the sample, that is, the same in the regions below the gate and in the wires. From the previous section, this has been shown not to be the case, as the processing of the devices, particularly gates, affects the surface of the material, which may lead to surface 'depletion', or, in fact, extra charge in the AlGaAs layers screening the 2DEG. Therefore, to apply this model correctly the threshold voltages must be measured with reference to the voltage at which the carrier concentration across the whole device is uniform, which may, or may not, be at 0V.

From Table 4.4 it can be seen that for A21614 the carrier concentration in the wire region is $2x10^{15}m^{-2}$, and in the gate region is $0.7x10^{15}m^{-2}$. By assuming the magnitude of the capacitance in the gate region remains constant, and scaling the voltage to equalise the carrier concentrations in the wire and FET regions, it is possible to estimate the voltage at which the sample carrier concentration is uniform. For A21614 this implies that the reference voltage is no longer 0V but +0.17V. Relative to

this voltage the FET threshold voltage, V_c, is now (0.09+0.17)V and the magnitude of the voltage required to fully deplete the wires, V_c', is (0.17+0.7)V. This results in an experimental value for (V_c'/V_c) of 3.3 compared to the previous value of 7.77. The theoretical value for (V_c'/V_c) from the Davies calculations was 3.4.

For the A425 samples the situation is slightly different. In this case there is a step in the characteristic at a negative voltage, which for A42529 is at -0.5V. If the uniform carrier concentration argument is applied in this case then -0.6V should be taken as the reference voltage. This means that the magnitude of the voltage required to activate the wires is (1-0.6)V instead of 1V, and the magnitude of the voltage required to deplete the wires is (1.5-0.6)V rather than 1.5V. The predicted ratio was 3.2; using these revised figures the experimental ratio is 2.3. The revised experimental and theoretical data is given in Table 4.6.

sample number	$(V_c)_{\text{exp new}}$	$(V_c')_{\text{exp new}}$	$\left(\frac{V_c'}{V_c}\right)_{\text{exp new}}$	$\left(\frac{V_c'}{V_c}\right)_{\text{theor}}$
A21612	0.2	0.49	2.5	2.6
A21668	0.19	0.92	4.8	5.2
A21611 (low T)	0.55	1.75	3.2	3.9
A21614	0.26	0.87	3.3	3.4
A42529	0.4	0.9	2.3	3.1
A42532 (dark)	0.45	1.2	2.7	4.0
A42532 (light)	0.65	2.95	4.5	4.0
A42531	1.2	2.9	2.4	3.2

Table 4.6 Table showing calculated and revised experimental values for V_c'/V_c.

The values of V_c and V_c' are quoted in Table 4.6 as the magnitude of the voltage range of interest. For example, for A21614 the magnitude of the revised voltage range for the FET region is (0.17+0.09) and the voltage range for the wire region is (0.7+0.17).

This is, of course, altering the figures to fit the model, which in general is not a good approach, particularly when it has already been pointed out that there are physical difficulties with the model. However, it should be noted that the assumption that the 2DEG is not in a state of equilibrium at 0V is not unrealistic. In fact, from the dark state capacitance characteristics for A42531 it can be seen that the wires become formed at a positive voltage, indicating that a corresponding FET sample would have been cut-off at 0V.

From Table 4.6 it can be seen that, for the A216 samples, the revised figures give, generally, good agreement, but for the A425 samples, with the exception of A42532 in the illuminated state, the experimental values of V_c'/V_c are significantly less than the predicted values. In Section 4.8.2, in the discussion of the magnitude of FET capacitances, it was suggested that the 2DEG in A425 was further from the surface than expected, due to the presence of an interfacial layer between the gate and the GaAs cap. This would have an effect on the predicted value of V_c'/V_c. However, corrections of this type to force the data to agree with the model take the analysis into the realms of 'wishful thinking'.

It should be noted that to calculate the revised figures it was necessary to assume that all the charge was in the 2DEG. As has been pointed out on several occasions, this may not be valid.

4.10 SUMMARY OF EFFECTS SEEN IN CAPACITANCE AND CONDUCTANCE DATA

The effects seen in the capacitance and the conductance data are summarised as follows.

(1) The capacitance and conductance characteristics show a strong temperature dependence in the temperature range 295K-12K.
(2) There is no temperature dependence of the conductance at low temperatures, i.e. <1K.
(3) The wire sample conductances consistently display three distinct gradients in the cut-off limit, whereas the FET samples show a more gradual cut-off.
(4) The magnitude of the FET capacitance at low temperatures is in reasonable agreement with the predicted value.
(5) The threshold voltages of the wire samples are in reasonable agreement with the predictions of Davies.

(6) The magnitude of the capacitance of the wires is higher than expected, from the sample geometry.

The most significant of these is the fact that the amount of charge in the wires is always higher than expected. This is confirmed in the next chapter when comparing the carrier concentration found from the Shubnikov de Haas data with that estimated from the capacitance data. The suprising feature of this discrepancy is that it is seen in all of the samples measured and on both of the materials used, which suggests that it may be either a fundamantal effect, or an effect induced by the sample processing techniques employed.

4.11 REFERENCES

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CHAPTER FIVE

MAGNETOCONDUCTANCE AND MAGNETOCAPACITANCE DATA

5.1 INTRODUCTION

In this chapter the effects of a magnetic field on the conductance and capacitance of FETs and wire samples will be discussed. For all of the measurements taken in this project the magnetic field was applied perpendicular to the plane of the sample.

This chapter will be divided into three sections on magnetoresistance, magnetocapacitance, and finally summary.

5.2 MAGNETORESISTANCE

This section will cover the presentation and discussion of low and high B magnetoresistance data.

The sample design used is shown in Figure 1.10(b). The magnetoresistance was measured by driving a constant current through the source and drain contacts and measuring the voltage dropped across the side voltage probes. The voltage probes are 100μm apart with the standard gate width of 17μm, so the measured voltage is divided across the wire region and two 2DEG regions, as shown below, in Figure 5.1.

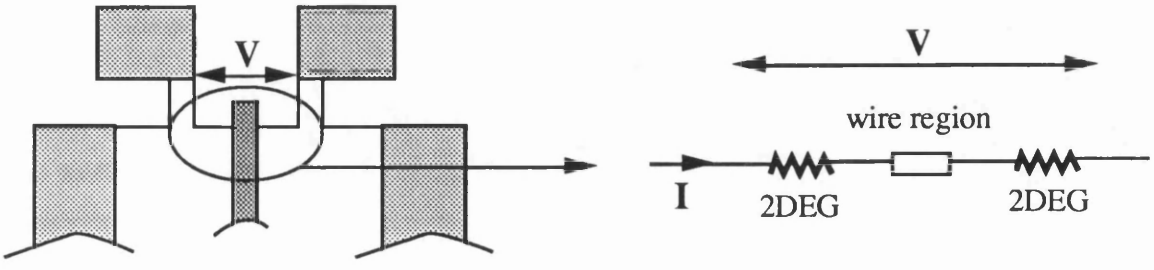


Figure 5.1 Diagram illustrating the voltage measured in the magnetoresistance measurements.

The potential division across the different regions makes interpretation of the data somewhat difficult, as will be discussed in the following sections.

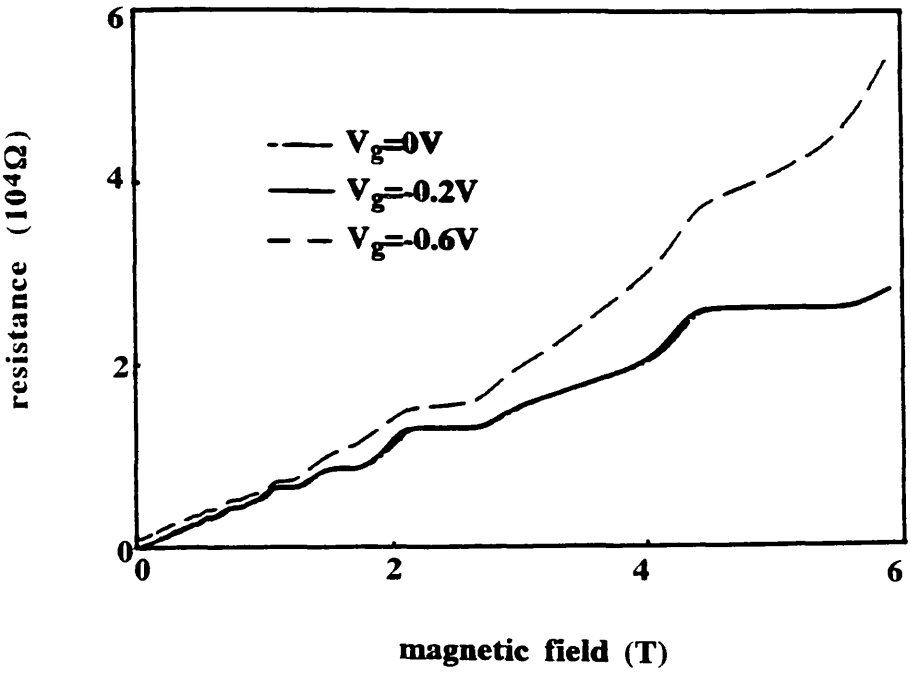
5.2.1 MAGNETORESISTANCE DATA IN THE RANGE 0T-2T

Shubnikov-de Haas measurements were taken on four of the five samples measured in the refrigerator. The standard measurement current used was 10nA, as it was found that at this level the voltages developed across the samples were not high, so avoiding electron heating, with, at the same time, a low noise level on the signal of the order of a few nanovolts. The standard measurement frequency was 17Hz. The low B data taken for A21614, A42529, A42532 and A42531 will be discussed. Unfortunately for A21614 the side contacts were not working so no Shubnikov-de Haas results are available for this sample. However, the two terminal resistance was measured as a function of magnetic field in order to give an estimate for n_{2d}.

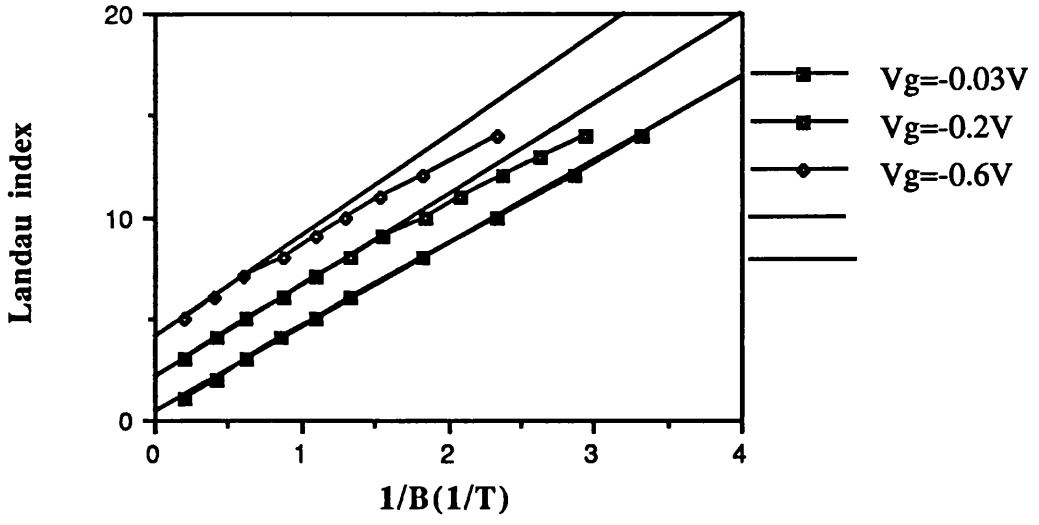
(a) Presentation of data

A21614

As noted above the voltage contacts on this sample were not working so the only low B data available is that of the two terminal resistance. For reference the capacitance characteristic is given in Graph 4.9. The magnetoresistance data is shown overleaf in Graph 5.1, and from this it can be seen that there are plateaux in the resistance at 1/integer multiples of h/e^2. As pointed out in section 1.5.3(b), these plateaux in the two terminal conductance result from the formation of edge states. The observation of well defined plateaus in the two terminal resistance only occurs if the contacts are ideal and electrons propagate through the edge channels with a high transmission coefficient. Thus, the 2 terminal measurements taken on this sample indicate high quality ohmic contacts. The position in 1/B of the plateaux is plotted in Graph 5.2 to give an estimate of the carrier concentration.



Graph 5.1: Low B 2-terminal magnetoresistance data for A21614 at 70mK and gate voltages of 0V, -0.2V and -0.6V.



Graph 5.2: Landau index against position of resistance minima, in 1/B, for A21614

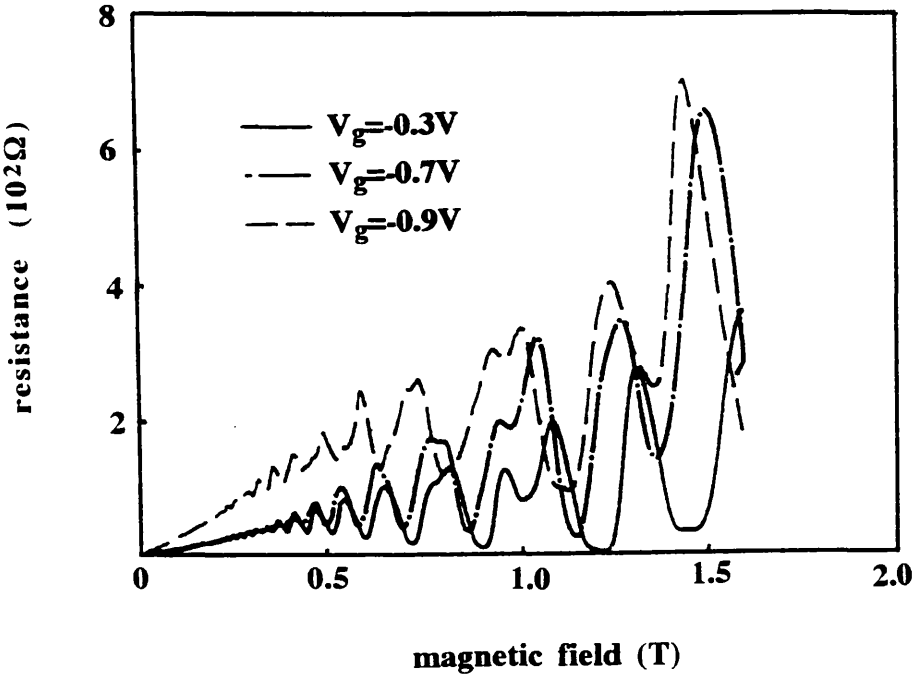
In this and subsequent graphs the Landau index for different gate voltages is offset by integral values for clarity.

From Graph 5.2 it can be seen that at -0.03V there is no deviation from linearity in the Landau plot, which indicates a carrier concentration of $1.0 \times 10^{15} m^{-2}$, but when the wires are formed at gate voltages of -0.2V and -0.6V there is curvature in the Landau plots. It can be seen that as the gate voltage is made more negative the deviation occurs at higher fields, suggesting that this is due to confinement effects in the wires, although it should be noted that in the high field limit the carrier concentration remains at the bulk material value of $1.0 \times 10^{15} m^{-2}$.

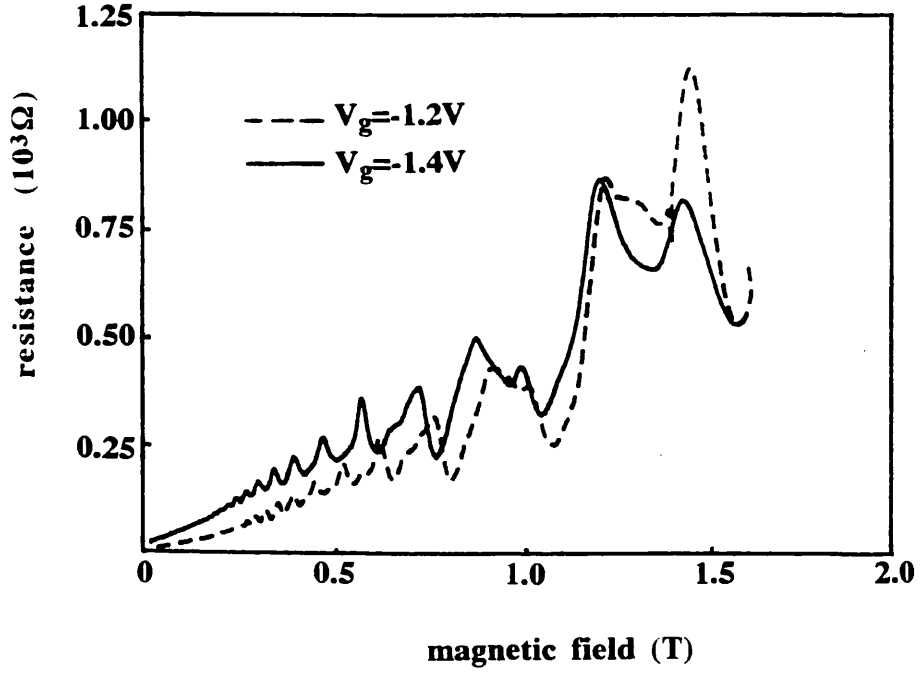
Using equation 1.17 and the positions of the deviations, the width of the wires are estimated to be 200nm and 90nm at -0.2V and -0.6V respectively. A more accurate estimate can be made by assuming a parabolic confining potential, and calculating the density of 1D states. This will be discussed in Section 5.2.3. The wire widths can also be estimated from the capacitance characteristic, assuming that the carrier concentration is not a function of the gate bias. However, this highlights a problem with the data collectively so will be discussed in Section 5.2.1(b).

A42529

This sample was measured extensively. The low B data is shown overleaf in Graph 5.3(a) for gate voltages -0.3V, -0.7V and -0.9V and Graph 5.3 (b) for -1.2V, and -1.4V. The voltages at which the magnetoresistance was measured were selected by considering the relative position along the capacitance characteristic, which is shown in Graph 4.17. For A42529 the capacitance characteristic displayed a step at -



Graph 5.3(a): Low B magnetoresistance data for A42529 at 70mK and gate voltages of -0.3V, -0.7 and -0.9V.

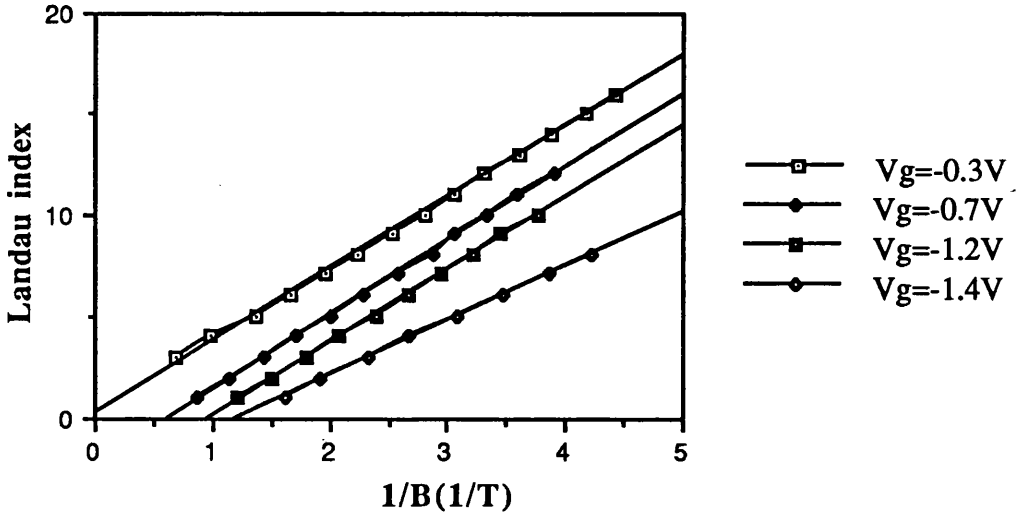


Graph 5.3(b): Low B magnetoresistance data for A42529 at 70mK and gate voltages of -1.2V and -1.4V.

0.5V so the magnetoresistance was measured at -0.3 and -0.7V to see if the region between 0V and -0.5V could be distinguished from the region -0.5V to -1.0V. The magnetoresistance was also measured at -1.2V and -1.4V as both of these voltages were in the voltage range in which the wires were formed. The cut-off voltage of A42529 was at -1.5V. However, it was found that the resistances developed at -1.5V were too high to measure so -1.4V was the most negative voltage used.

From mere inspection of these graphs it is difficult to pick out clear differences in the characteristics, other than the obvious rise in the background resistance as the gate bias becomes more negative. However, there is evidence that the dominance of the spin split states shifts as the gate bias becomes more negative. For example, for the curve at V_g=-0.3V the first resolved spin split states occur at about 1T, with the spin-up state (the second peak) larger than the spin-down (the first peak). However, at -1.4V, and similar fields, the spin-down state becomes dominant.

To estimate the carrier concentration of this sample the positions of the minima were analysed. The positions of the minima in 1/B are plotted against arbitrary integers in Graph 5.4, below, for gate voltages of -0.3V, -0.7V, -1.2V and -1.4V.



Graph 5.4: Position of resistance minima in 1/B against Landau index for A42529

From this it can be seen that there is no evidence, at any gate bias, of any deviation from the linear relationship typical of standard 2DEG samples. The carrier concentration found from the plots at -0.3V, -0.7V and -1.2V is $1.7 \times 10^{15} m^{-2}$, and from the -1.4V plot $1.3 \times 10^{15} m^{-2}$. In general it was found that the carrier concentration estimated from the 1/B plots did not vary significantly with the applied gate bias until very close to the wire cut-off voltage. The variation between the carrier concentrations

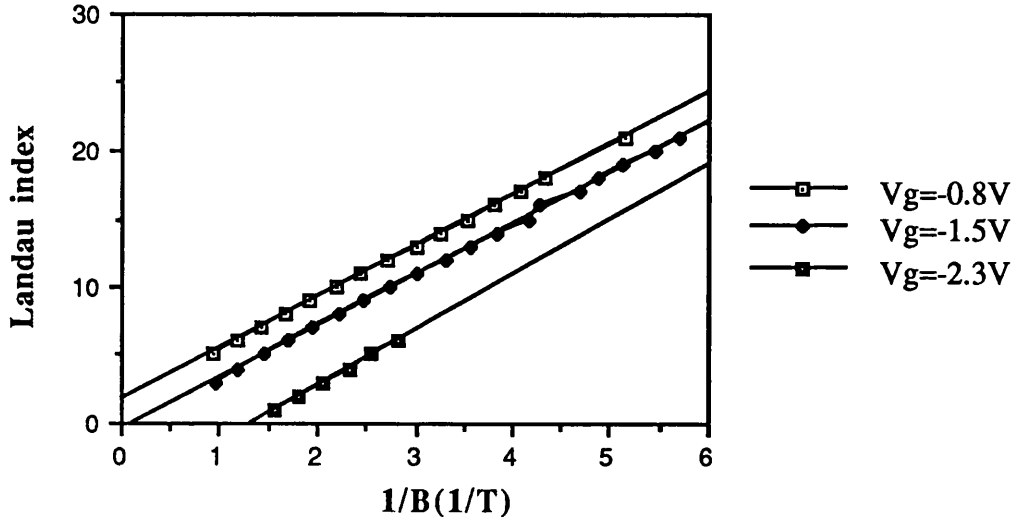
at the more positive gate voltages was 1% which is within the limits of experimental error. It should be noted that the increase in the capacitance in the voltage range 0V to -0.5V is not reflected in this data, suggesting that the extra charge, measured in the capacitance characteristic does not contribute to the conductance.

A42532

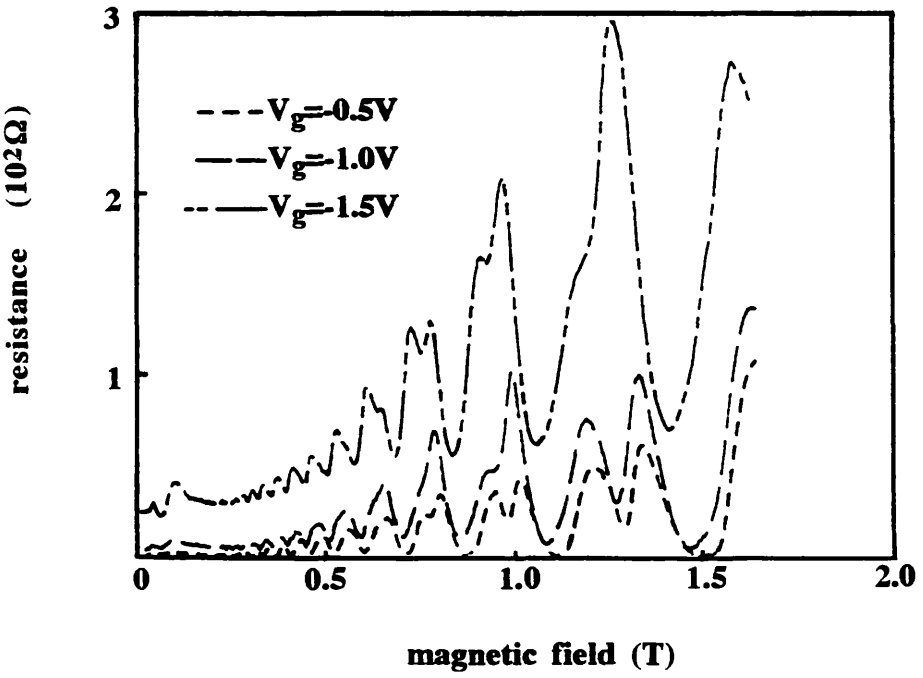
The magnetoresistance of this sample was measured in the illuminated state. The capacitance characteristic for this is shown in Graph 4.18(b), and the magnetoresistance data at gate voltages of 0V, -1.2V, and -1.5V at is given in Graph 5.5(a). The corresponding data at -2.0V, -2.2V and -2.3V is given on Graph 5.5(b) for clarity.

From Graphs 5.5 (a) and (b) it can be seen that there are several interesting features apparent. At voltages more negative than -0.5V, that is when the wires are formed, two peaks are observed in the resistance below 0.2T. These peaks are attributed to electron focusing effects, which will be discussed fully in section 5.2 (b). At -0.5V the minima in the oscillations decrease in resistance and reach zero at 1.45T. This reduction to 0Ω in the minima indicates that there is no evidence for parallel conduction in this sample, which was a possibility as the magnetoresistance was measured in the illuminated state. The Landau levels in this sample become spin-split at 0.7T and as the gate voltage becomes increasingly negative the spin-split up-state becomes dominant. In the curve at -2.3V there is some evidence of negative magnetoresistance. Finally, perhaps the most obvious effect of making the gate bias more negative is the increase in the offset resistance at 0T.

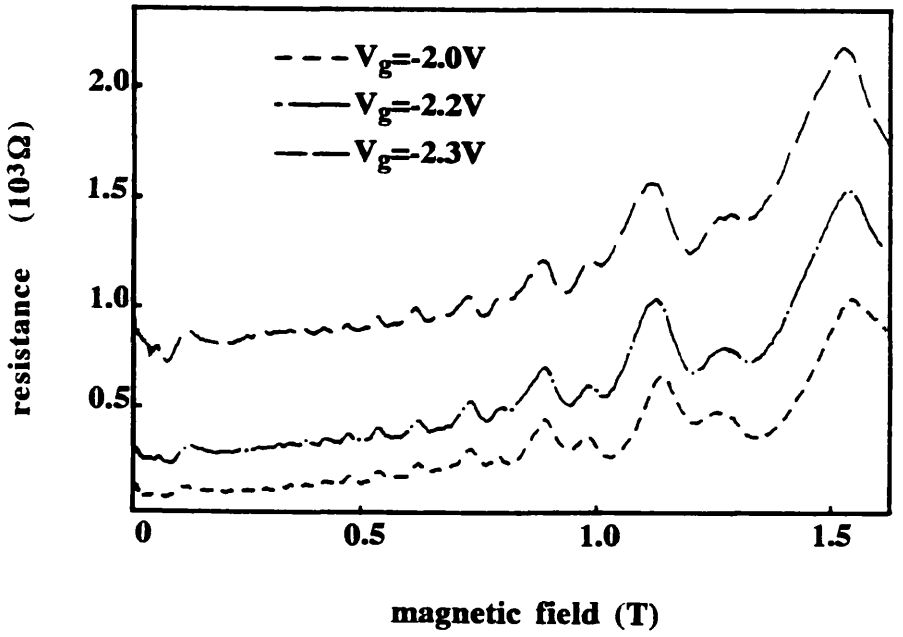
A plot of the minima in 1/B against Landau number is given in Graph 5.6.



Graph 5.6: Position of resistance minima in 1/B against Landau index for A42532



Graph 5.5(a): Low B magnetoresistance data for A42532 at 80mK and gate voltages of 0V, -1.0V and -1.5V.



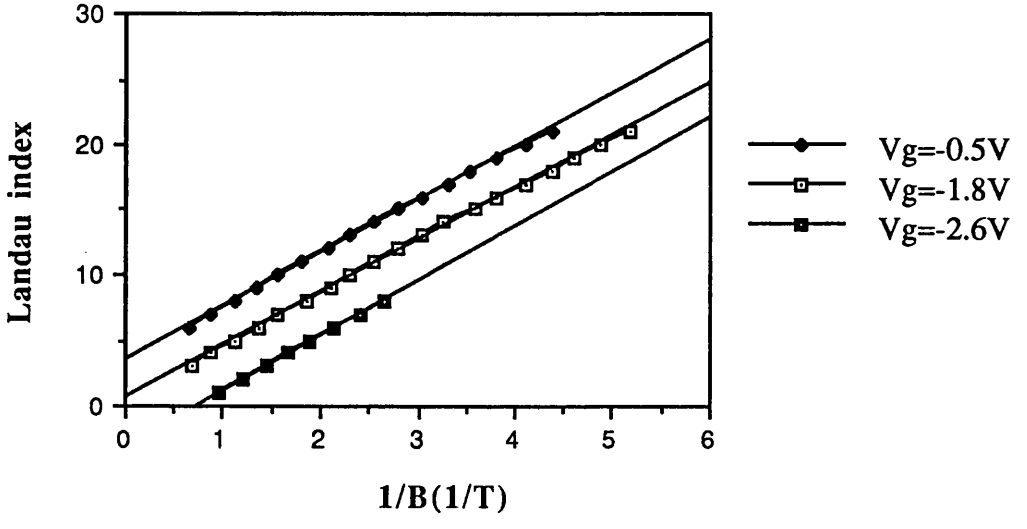
Graph 5.5(b): Low B magnetoresistance data for A42532 at 80mK and gate voltages of -2.0V, -2.2V and -2.3V.

From this it can be seen that again there is no deviation from linearity. The estimated carrier concentration is $1.8 \times 10^{15} m^{-2}$, which is again independent of the gate bias. The Fourier transform of this data was taken and displayed only one period corresponding to a carrier concentration of $1.8 \times 10^{15} m^{-2}$, which indicates that the carrier concentration in the wire and the 2DEG regions must be very similar, if not the same.

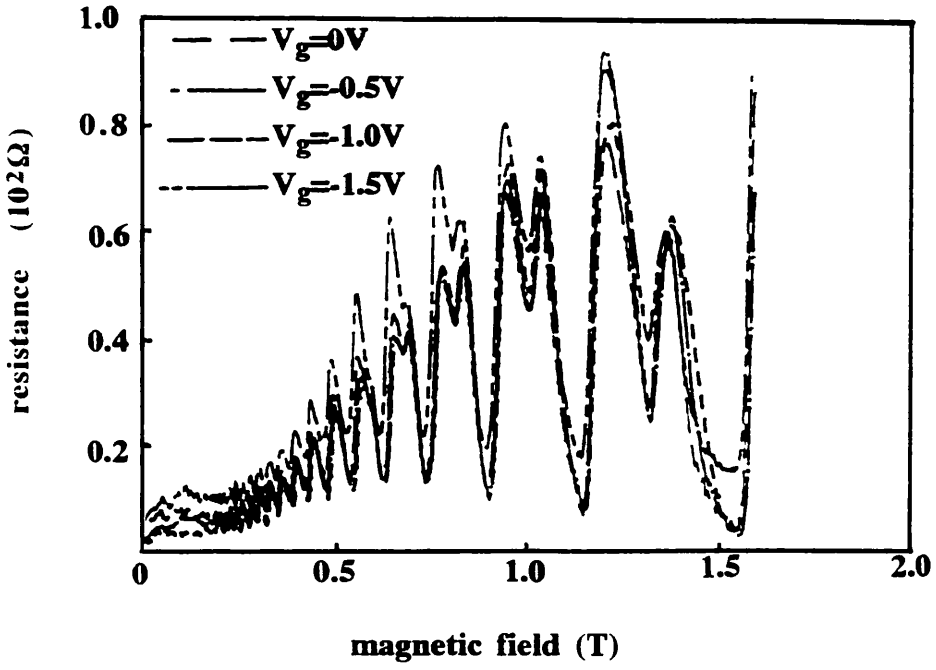
A42531

The magnetoresistance of A42531 was measured in its illuminated state at gate biases of 0V, -0.5V, -1.0V, -1.5V, -1.8V, -2.0V, -2.2V, and -2.4V. These voltages spanned the full range of the capacitance characteristic, which is shown in Graph 4.19(b). The magnetoresistance data for this sample at gate voltages of 0V, -0.5V, -1.0V, and -1.5V is given in Graph 5.7(a), and for -1.8V, -2.0V, -2.2V and -2.4V in Graph 5.7(b), both of these are given overleaf. The low field data at -2.2V and -2.4V is given in graph 5.7(c).

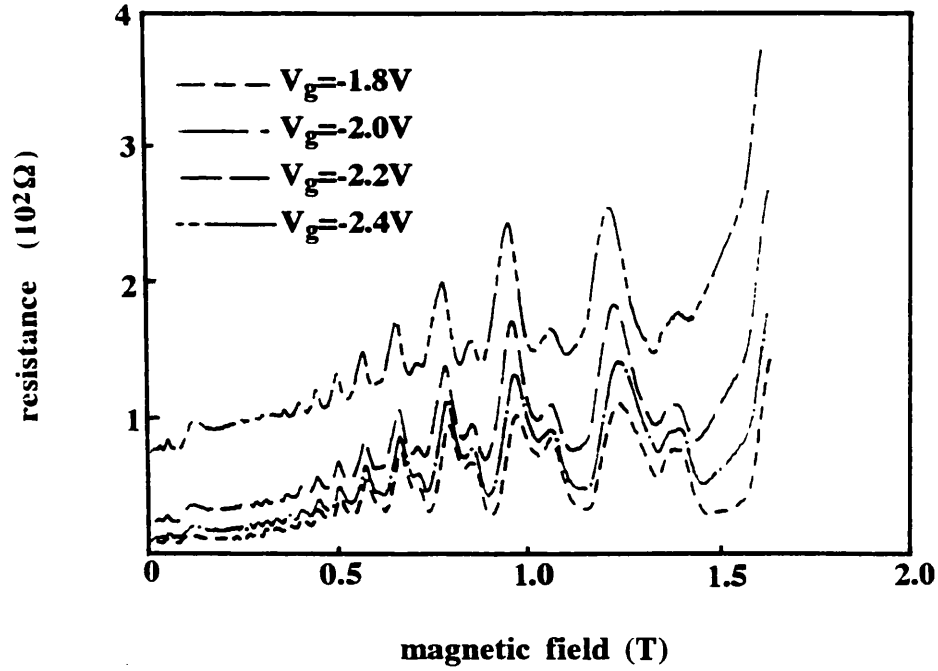
From Graphs 5.7 (a) and (b) it can be seen that oscillations in the resistance begin at 0.2T, indicating a very high carrier mobility. These curves also show the low field focusing peaks seen in the magnetoresistance of A42532, starting at about -1V, which is in good agreement with the voltage at which the wires were estimated to form. The minima in the oscillations, although not reaching 0Ω in this field range, decrease in resistance as the field increases, suggesting the absence of parallel conduction in this sample. The most obvious effect of the increasingly negative bias is the increase in the background resistance of the curves. As with A42529 and A42532 one of the spin split states asserts dominance; in this case it is the spin down state.
A plot of the minima in 1/B against Landau number is given below in Graph 5.8.



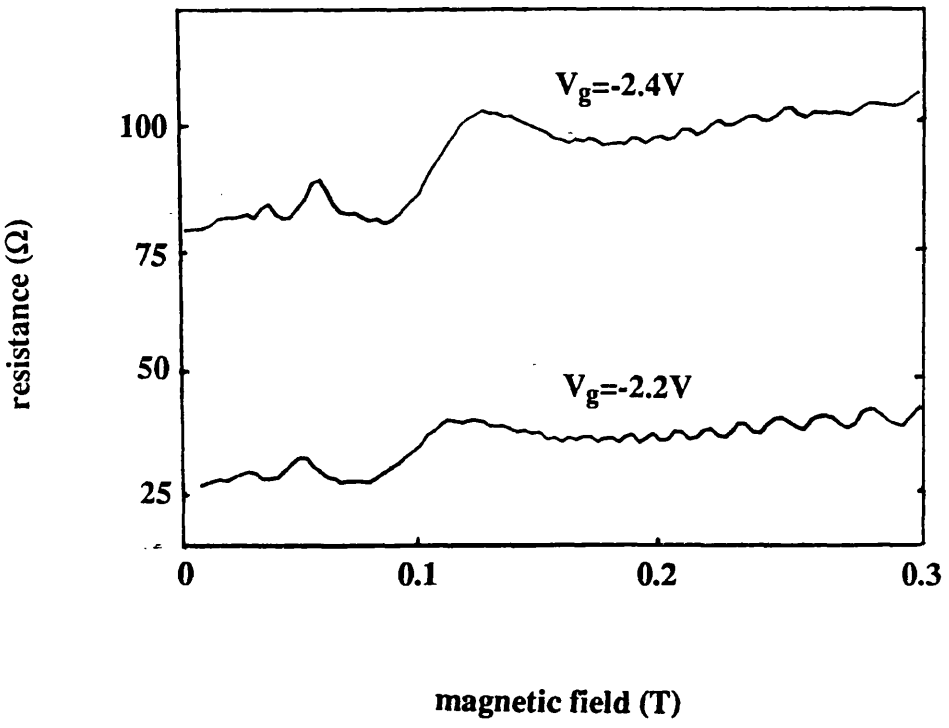
Graph 5.8: Position of resistance minima in 1/B against Landau index for A42531



Graph 5.7(a): Low B magnetoresistance data for A42531 at 80mK and gate voltages of 0V, -0.5V, -1.0V and -1.5V.



Graph 5.7(b): Low B magnetoresistance data for A42531 at 80mK and gate voltages of -1.8V, -2.0V, -2.2V and -2.4V.



Graph 5.7(c): A42531, low B focusing peaks at gate voltages of -2.2V and -2.4V, at 80mK.

From this it can be seen that again there is no deviation from the linear relationship for 2DEG samples at -2.6V, although there is a slight curvature in the plot at -0.5V. However, the wires were not formed at -0.5V so the curvature cannot be attributed to confinement effects. From the Landau plots the carrier concentration at all gate biases, was found to be $1.9 \times 10^{15} m^{-2}$. The Fourier transform of this data also implied a carrier concentration of $1.9 \times 10^{15} m^{-2}$ with no dependence on the gate bias, again implying that the carrier concentration was uniform over all regions of the sample.

(b) Electron focusing

The peaks seen in the low B magnetoresistance of A42532 and A42531 are attributed to electron focusing effects. Electron focusing was first studied by Sharvin et al, 1965. Since then, the techniques have been used to explore the Fermi surface and surface conditions of metals, and more recently of GaAs/AlGaAs heterostructures. The samples used in the recent experiments by Van Houten et al, 1989, were so-called point contacts. These systems were ideal for conducting such experiments, but similar effects have also been seen in multiple wire samples. The first reports of this were published by Nakamura et al, 1989.

Electron focusing can be produced in nanostructures fabricated on GaAs/AlGaAs heterostructures by the application of a magnetic field perpendicular to the 2DEG. Electrons no longer travel in straight lines between scattering events; rather, they orbit a fixed centre travelling between such events, or 'skip' along the sides of the sample. At the ends of the wires the electrons may be bent back into another wire. This is what is termed electron focusing. This is illustrated opposite in Figure 5.2.

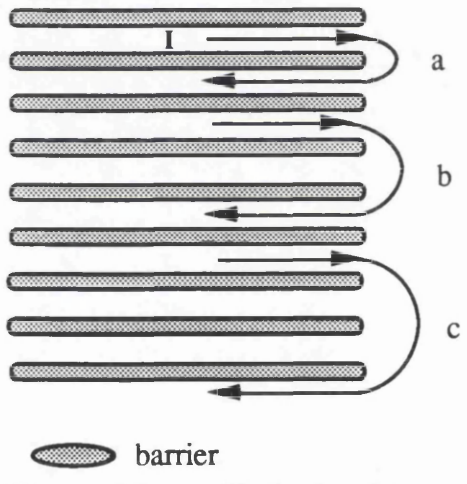


Figure 5.2 Mechanism for electron focusing

The result of this focusing effect is that peaks are seen in the magnetoresistance as electrons are emitted from one wire and focused back into another wire. Electron focusing can occur when the cyclotron diameter is the same length as the separation of adjacent wires. The field values at which focusing occurs can be found from,

$$R_c = \frac{v_f}{\omega_c} \qquad (5.1)$$

Focusing is apparent when $2R_c=S$, where S is the separation between the emitting and the collecting wires. v_f is given by,

$$v_f = \frac{hK_f}{2\pi m^*} \tag{5.2}$$

and ω_c is given by,

$$\omega_c = \frac{eB}{m^*} \tag{5.3}$$

This implies that the focusing field, B_f, values for wires of separation S can be given by,

$$B_f = \left(\frac{2}{\pi} N_{2D}\right)^{\frac{1}{2}} \frac{h}{eS} \tag{5.4}$$

The measurements taken in this project differ somewhat from those of Nakamura et al. The wire samples investigated by Nakamura et al, 1989 were fabricated, in the first instance, using ion beam implantation techniques, and then in later experiments using wet etching (Nihey, Nakamura et al, 1990). Neither of these two techniques allows the possibility of varying the width of the wires, whereas the split gate depletion method employed in the course of this project does allow this. Also the samples used by Nakamura had, at most, eight wires in parallel, whereas the multiple wire samples made for this project comprised at least 400 wires.

The positions of the various peaks observed in the low B data are given in table 5.1 with the corresponding positions calculated using the separation between the centres of adjacent channels. The peaks are named (a), (b) and (c) to correspond with the trajectories illustrated in Figure 5.2. This data is also plotted in Diagram 5.1, overleaf.

Sample number	V_g(V)	exper. position of peak a (T)	calculated position of peak a (T)	exper. position of peak b (T)	calculated position of peak b (T)	exper. position of peak c (T)	calculated position of peak c (T)
A42532	-0.8	0.100	0.120	0.056	0.060	—	0.040
A42532	-1.5	0.107	0.120	0.050	0.060	—	0.040
A42532	-2.3	0.119	0.120	0.045	0.060	—	0.040
A42531	-1.5	0.125	0.145	0.059	0.072	0.038	0.048
A42531	-2.2	0.124	0.145	0.062	0.072	0.041	0.048
A42531	-2.3	0.133	0.145	0.077	0.072	0.056	0.048

ERROR ASSOCIATED WITH EXPERIMENTAL PEAK POSITION=+/-0.001T

Table 5.1 Table of position of focusing peaks at various gate voltages

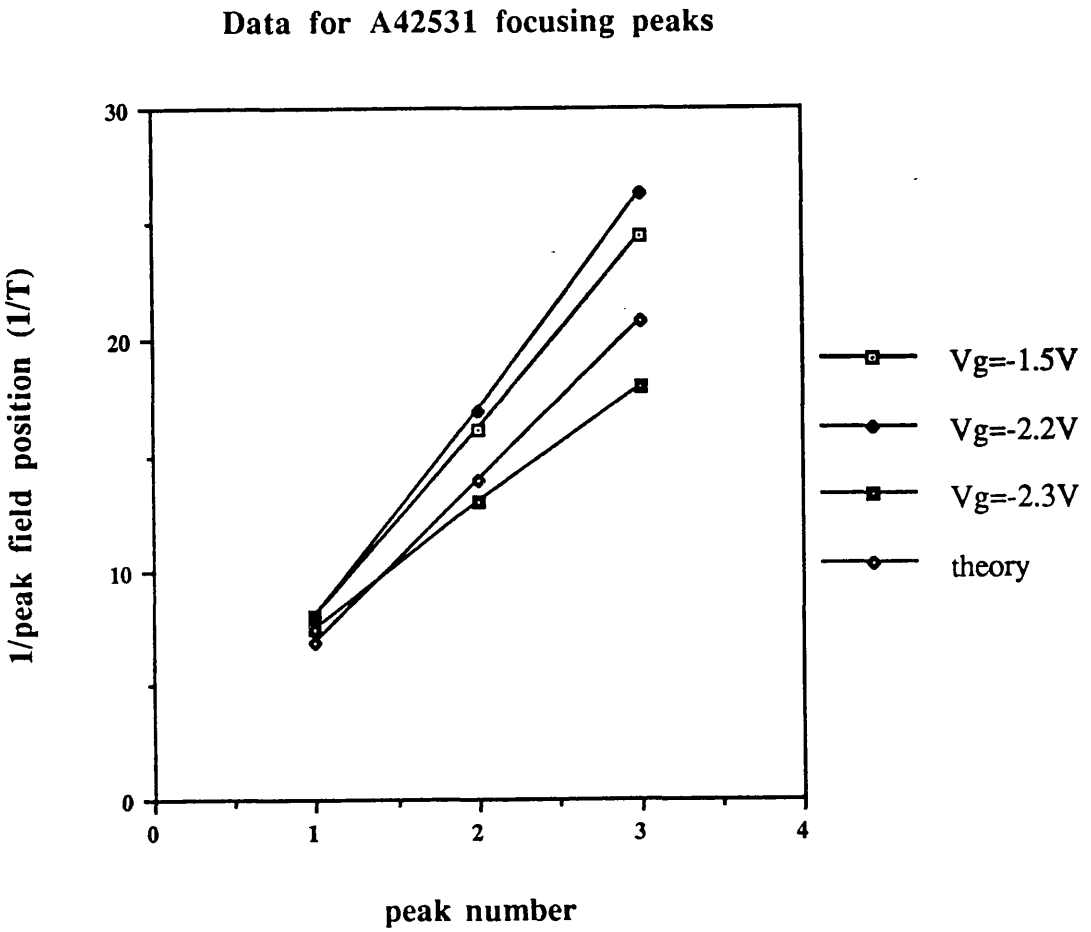


Diagram 5.1: Plot of focusing peak position in 1/B as a function of peak number (where peak a is 1, peak b is 2 etc.) for A42531 at gate voltages of -1.5V, -2.2V and -2.4V, and the theoretical plot found using Equation 1.18.

From table 5.1 it can be seen that the measured values do differ from the predicted values. However, for both samples the measured values for peak (a) move closer to the calculated values as the gate bias becomes increasingly negative, until near the cut-off voltage, the agreement is very good. This is attributed to the strengthening nature of the confining potential as the bias becomes more negative, which makes the potential at the wire edges better defined and the wires narrower. The calculated values for the positions of the peaks were found using the separation of the wires, assuming that electrons were scattered from the centre of the emitting wire to the centre of the collecting wire, and the carrier concentrations found from the Shubnikov de Haas oscillations. At very negative biases, where the confining potential is strong and well defined, and the wires are narrow, electrons are more likely to be scattered from the centre of one wire to the centre of the adjacent wire. The fact that at the very negative biases the agreement is quite good is remarkable since the multiple wire samples have on average 400 wires contributing to the magnetotransport. The measured value of peak (b) for A42531 follows a similar trend, giving equally good agreement at -2.3V, with peak (c) also showing reasonable agreement with predictions. However, for A42532 the position of peak (b) deviates from the predicted value as the gate bias is made more negative, although is in good agreement with predictions at the more positive voltages. Peak (b) actually moves to fields at which peak (c) for this sample would be expected. This is not understood.

The position of the focusing peaks can give information on the strength of the confining potential. The magnitude of the peaks can give information on the mean free path of the electrons in the system. After Spector et al, 1989, the amplitude of the peaks is exponentially related to the separation of the wires. This can be described by,

$$\frac{V_P}{V_{SD}} = C \exp\left(\frac{-S}{\lambda_c}\right) \qquad (5.5)$$

where V_p is the peak voltage, V_{sd} is the applied source drain voltage, C is a constant, S is the distance between the emitting wire and the wire the electrons are focused into and λ_c is the electron mean free path. For A42531, which displays three focusing peaks, λ_c is estimated to be 3(+/-1)μm over a range of gate biases. This is low when compared with the estimate from the mobility measurements taken on an unpatterned sample which suggest that the electron mean free path is 10μm. This is not entirely surprising as electrons being focused from one wire into another are more susceptible to forward, that is, small angle, scattering events.

(c) General comments on low B Shubnikov-de Haas data

All of the low B data taken in the course of this project has been presented. There are several features to note about these data. The first of these features is that most

of the four terminal data does not indicate any negative magnetoresistance in the very low field limit, that is < 0.2T, with the only exception being the magnetoresistance at -2.3V for A42532. Negative magnetoresistance is so often apparent in wire samples that it is regularly presented as evidence that wires actually exist. There are three possible explanations for this absence. The first, and most optimistic of these, is that the wires are of such a high quality that boundary scattering is purely specular in nature and the characteristic separation of impurity sites is so great that no scattering events are possible along the length of the wire, implying that no backscattering events can occur and so the conditions required for negative magnetoresistance are not satisfied. The second, and more sobering, explanation is that the wires were not formed, and the third is that the wire effects were simply swamped by effects due to the electron reservoirs connecting the active region to the ohmic contacts. Fortunately these latter suggestions can be dismissed. The capacitance characteristics were used to select the voltages appropriate for the measurement of the magnetoresistance, and provide the best evidence to suggest that the wires were fully formed. The possibility that the wire region was not being measured is slightly more difficult to dismiss. However, the presence of electron focusing peaks confirms that the wires were fully formed and more importantly, implies that below 0.2T the measurement was in some limits sensing the electrons in the wires and not merely measuring the magnetoresistance of the regions between the wires and the ohmic contacts. Therefore, it can be concluded that the absence of negative magnetoresistance indicates the high quality of both the wires and the material.

The second main feature of the low B magnetoresistance data is that A21614 displayed a deviation from the standard 2DEG 1/B linearity with Landau index indicating confinement, whereas the A425 samples measured did not display this effect, behaving as unpatterned 2DEGs with the magnetoresistance oscillations indicating that the carrier concentration in the wire samples was independent of the bias applied to the gate. The deviation from linearity should occur when the cyclotron diameter, $2R_c$, is larger than the width of the wires. There are three possible explanations; the first is again the possibility that for the A425 samples the wire effects in this field range were simply swamped by the magnetoresistance of the electron resevoirs between the active region and the voltage probes; the second is that the gate bias was not taken to sufficiently negative values, and hence the wires were never narrow enough to be smaller than $2R_c$, and the third, that the field range investigated was outwith that in which deviations should occur.

To investigate the possible effects of the regions of 2DEG connecting the active area to the voltage probes for the A425 samples two techniques were employed. The first of these was to Fourier transform the data. However, the Fourier transforms

consistently displayed only one period suggesting that the carrier concentration was, within the limits of the measurement and the analysis, uniform over the samples. The second method employed was to subtract the 0V magnetoresistance characteristics from those taken at finite gate voltages, under the assumption that the magnetoresistance in the ungated 2DEG regions was unaffected by the gate voltage and merely added as a resistance in series with the wire region. This method of data subtraction had little effect on the data taken in the wire voltage region. Therefore, it can be concluded that the effects of the series resistance due to the 2DEG regions were negligible.

To discuss the second and third of the possibilities listed above it is necessary to consider the fields at which deviations were expected - these can be found using Equation 1.18 and are shown in Table 5.2.

Sample number	Wire width (nm)	critical B(T) for wire width=R_c	critical B(T) for wire width=$2R_c$	critical B(T) for wire width=$4R_c$
A21614	430	0.23	0.46	0.92
A42529	430	0.32	0.64	1.28
A42532	570	0.25	0.5	1.00
A42531	430	0.33	0.66	1.32

Table 5.2 Table showing fields at which deviations were predicted.

The data for A21614 is included for comparison.

To fully utilise this table it is necessary to know the wire width as a function of gate bias. This highlights a major problem with the data collectively, as both the capacitance characteristics and the estimates of the carrier concentration from the magnetoresistance oscillations have to be used to estimate the widths of the wires. In theory, the best way to find the width of the wires is to use the capacitance to find the amount of charge in the wires as a function of the gate bias and then divide this by the wire length, e, and the carrier concentration, as found from the magnetoresistance measurements. Unfortunately doing so results in wire widths that are obviously too large, in fact, significantly larger than the maximum lithographical width of the wires. This is as a direct result of the fact that the carrier concentrations calculated from the magnetic field data are considerably lower than the estimates made from the capacitance

data. For example, for A42531 the carrier concentration in the wires estimated from the capacitance data was $7.1 \times 10^{15} m^{-2}$ whereas from the magnetoresistance measurements the estimated carrier concentration was $1.9 \times 10^{15} m^{-2}$. This is a major problem and will be discussed in a later section. It is, of course, possible to make crude estimates of the wire width from the capacitance data alone. For example, for A42531 with a gate bias of -2.0V the capacitance data suggests that the wires were only 100nm wide, at which deviations would normally be expected in the low B field range.

Using the capacitance data it is also possible to estimate the widths of the wire as a function of gate bias to compare with those estimated from the fields at which the deviations occurred for A21614. For A21614, the wire widths estimated from the magnetoresistance were 200nm at -0.2V and 90nm at -0.6V, and from the capacitance 280nm at -0.2V and 30nm at -0.6V.

In conclusion the low B magnetoresistance data suggest that the wires and the materials used are of high quality. The main observations are that the carrier concentration in the wires is not a function of gate bias until very close to the wire cut-off, and there are deviations from the linear relationship between the positions in 1/B of the resistance minima and the Landau index observed for A21614, but not the A425 samples. The carrier concentrations are also observed to be consistently lower than the concentrations found from the capacitance data.

5.2.2 MAGNETORESISTANCE IN B RANGE 0T-12T

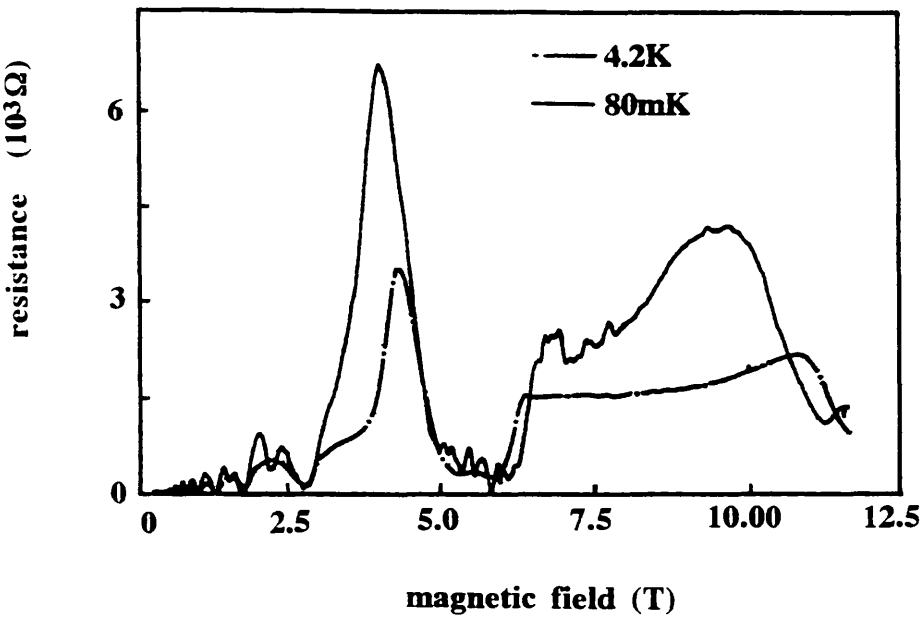
The samples were all measured at high and low B fields. The measurements at high B will be presented in this section, more for the sake of completeness than for their scientific significance. The high B data for A21614 will not be presented as it is all two terminal in nature.

(a) Presentation of data

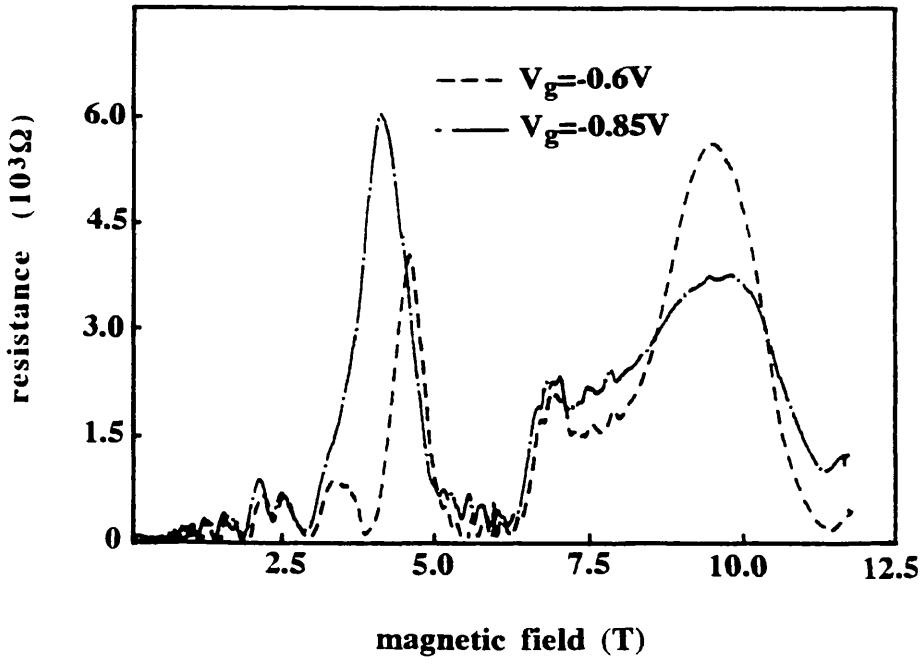
A21611/8

The magnetoresistance at 4.2K and 80mK at a gate bias of -0.6V is plotted overleaf in Graph 5.9(a) for A21611. From these it can be seen that the positions of the minima are, qualitatively, the same at both temperatures indicating that the carrier concentration does not change significantly between 4.2K and 80mK. The main effect of lowering the temperature is to resolve the spin-split peaks.

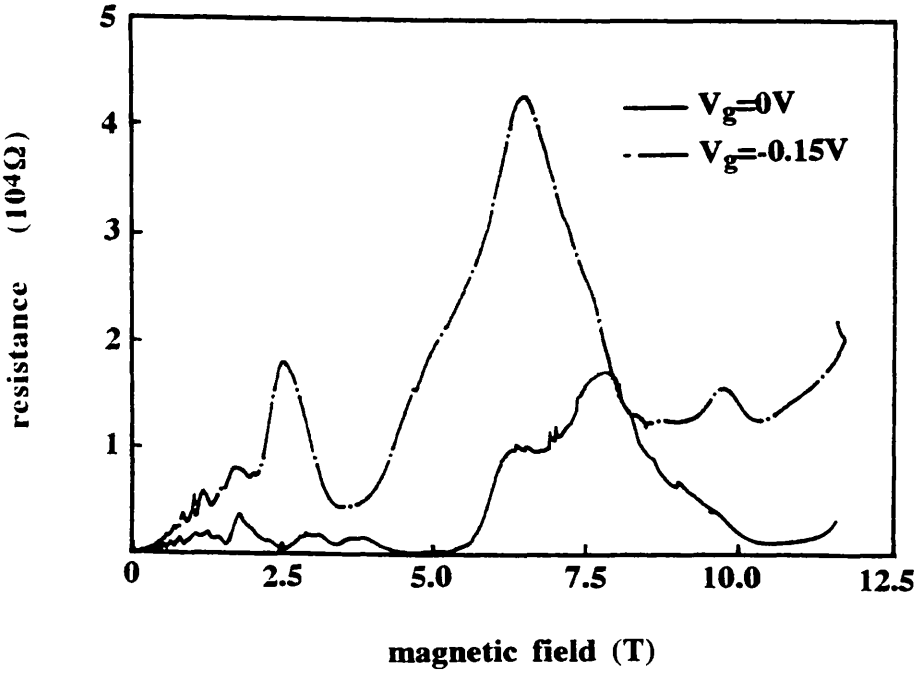
Now consider A21618, the FET sample. The data taken at 80mK is plotted overleaf on Graph 5.10. From this it can be seen that the magnetoresistance displays fewer spin split peaks than for A21611, the wire sample. The carrier concentrations estimated from the FET sample with 0V and -0.15V on the gate were $1.5 \times 10^{15} m^{-2}$ and



Graph 5.9(a): High B magnetoresistance data for A21611 at gate voltage of -0.6V as a function of temperature.



Graph 5.9(b): High B magnetoresistance data for A21611 at gate voltages of -0.6V and -0.85V, at 80mK.

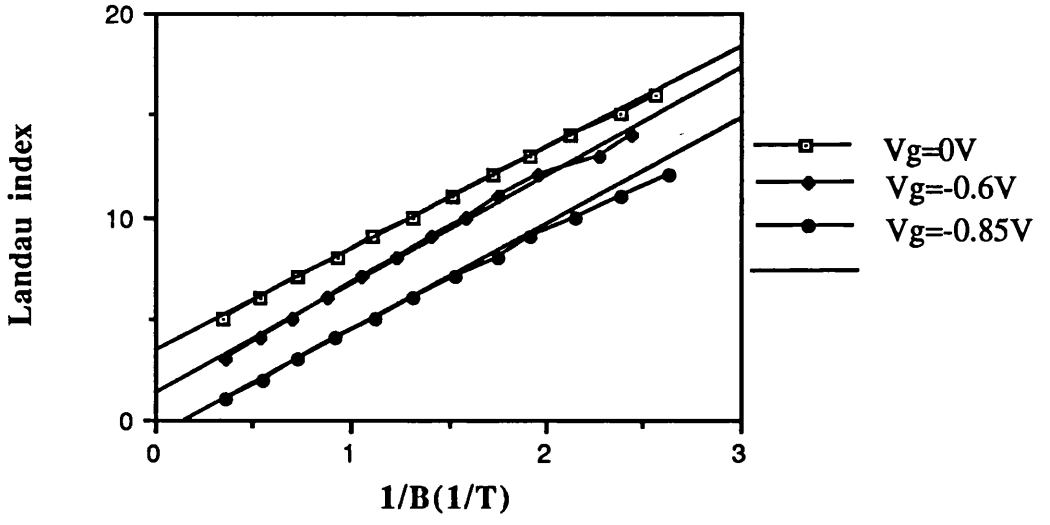


Graph 5.10: High B magnetoresistance data for A21618 at 80mK and gate voltages of 0V and -0.15V.

$1.0x10^{15}m^{-2}$ respectively. This reduction in the carrier concentration as the gate bias is made more negative arises as a result of the planar nature of the depleting potential. It is also interesting to note that the magnitude of the oscillations in this sample relative to those in the wire sample are significantly higher, which may explain the absence in the low B data of any features indicating that the gated regions were being depleted, as a high resistance in parallel with a low resistance is effectively shorted.

The 80mK magnetoresistance data for A21611 is plotted on Graph 5.9(b). From this it can be seen that the magnetoresistance at low B exhibits standard Shubnikov de Haas oscillations. On a qualitative level, the similarity in the positions of the minima of the oscillations suggests that the carrier concentration does not vary as a function of the applied gate bias. Also the minima at the high field reach 0Ω indicating that the charge contributing to the resistance is in the 2DEG only. From Graph 5.9(b) it can be seen that below 5T for the -0.6V magnetoresistance the oscillations remain spin split with each of the states well resolved, but at -0.85V the spin-up peak becomes dominant almost swamping the spin-down state. Finally, in the range 5.5T to 6.5T oscillations at the 'zero' are observed, these were found to be highly reproducible at fixed gate voltages.

The positions of the resistance minima, in 1/B, vs Landau index are given in Graph 5.11.



Graph 5.11: Position of resistance minima in 1/B against Landau index for A21611

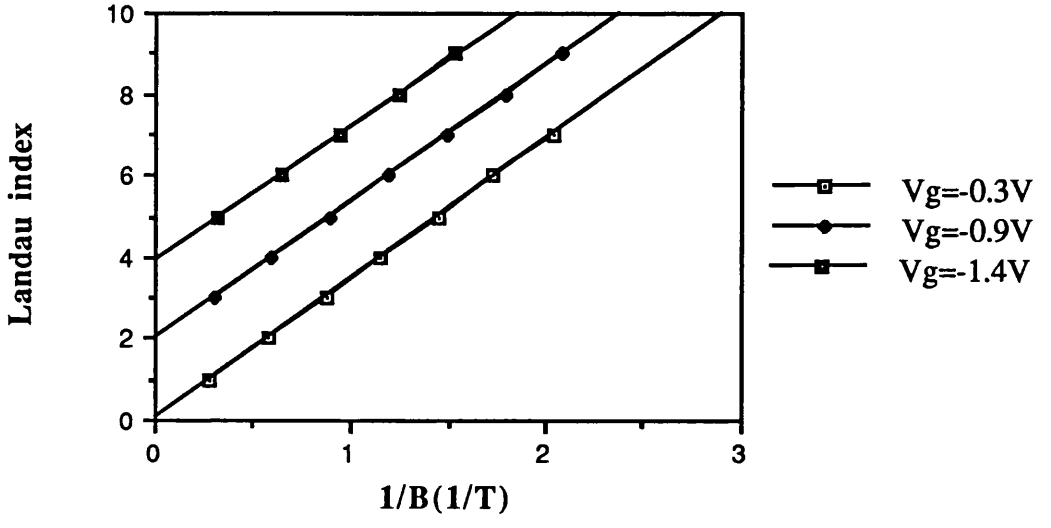
From Graph 5.11 it can be seen that there is no deviation in the linearity of the Landau plot at 0V, but the plots taken at 0.6V and -0.85V do show signs of a 'kink' in the 1/B range $(1.8\text{-}2.0)T^{-1}$, with the -0.85V plot showing definite signs of curvature at $1/B=1.9T^{-1}$.

The carrier concentration from the 0V plot, and the linear region of the -0.85V plot, is $2.1 \times 10^{15} m^{-2}$. For the characteristic at -0.6V the concentration is somewhat higher at $2.6 \times 10^{15} m^{-2}$. The reason for this difference is not obvious. It is interesting to note that the carrier concentration for this sample is higher than that of the FET sample and does not depend as strongly on the gate voltage, reflecting the different depleting potentials which for the wire samples is lateral in nature but for FETs is planar. The fact that the carrier concentration for the FET is lower suggests that it is the gate which causes surface damage, thereby reducing the number of electrons in the channel, as suspected from the analysis of the capacitance characteristics in Section 4.9.2.

Using the carrier concentration estimated above, and the position of the deviation the wire width was calculated to be about 290nm, which is slighty lower than the estimate from the capacitance data of 340nm. This deviation will also be discussed in Section 5.2.3.

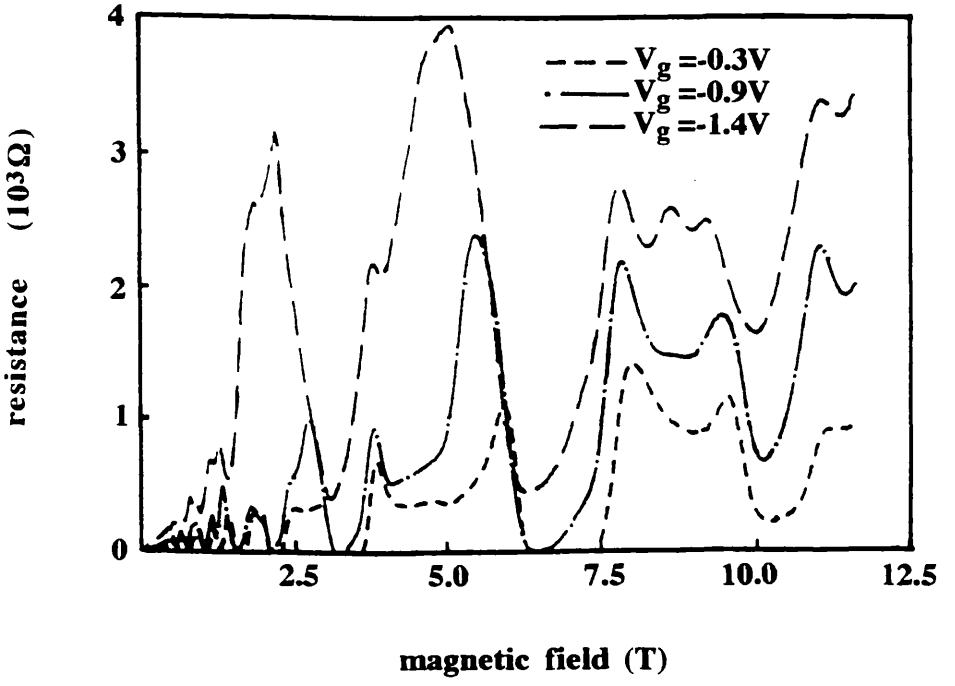
A42529

The magnetoresistance at -0.3V, -0.9V and -1.4V is plotted overleaf in Graph 5.12. From this it can be seen that these curves demonstrate zeroes in the resistance minima, which is final evidence to dispel the possibility that A42529 had a parallel conducting layer in the AlGaAs. The Landau plots are given in Graph 5.13.



Graph 5.13: Position of minima in 1/B as a function of Landau index for A42529 high B data

The carrier concentration estimated from these curves is $1.6 \times 10^{15} m^{-2}$, that is, slightly lower than the estimate from the low B characteristics. Again these plots display the standard unpatterned 2DEG linearity.



Graph 5.12: High B magnetoresistance data for A42529 at 70mK and gate voltages of -0.3V, -0.9V and -1.4V.

At about 10T this sample displays oscillations in the 'fractional' regime. In this limit the effects of electron - electron interactions in edge states become significant, but this will not be discussed in this thesis. The result of these interactions is that minima are seen in the magnetoresistance at fractional values of the Landau index. For this sample the 2/3 minimum is observed at 10.05T, and the 4/5 minima at about 9T. The curve at -1.4V also displays an extra peak in the fractional regime, at 8.8T. This was not evident at any of the more positive biases and so is being attributed to confinement effects. However, it is difficult to quantify any such effect.

Fractional states are generally seen in samples with very low carrier concentrations, and of a very high quality. It is interesting to note that the relative depth of the 2/3 minima increases slightly on this sample as the gate bias becomes more negative. This is contrary to the observations made by Smith et al, 1988, who measured the magnetocapacitance of similar samples and observed the minima strengthening as the gate bias was made more positive. This may have been as a result of the fact that the carrier concentration of the Smith sample was altered as the gate bias was changed, whereas for A42529 the carrier concentration was roughly independent of the gate bias.

For a general review of fractional quantum states see Beenaker and Van Houten, 1990.

A42532

The magnetoresistance at -1.2V, -1.5V and -2.0V is plotted in Graph 5.14. The positions of the minima in 1/B are linear with the Landau index and imply a carrier concentration of $1.8 \times 10^{15} m^{-2}$, this being the same as from the low B data. From Graph 5.14 it can be seen that, as with the previous samples, the main effect of the gate bias on the magnetoresistance is to make it progressively more difficult to resolve the spin split levels, particularly at high B fields, and to increase the magnitude of the resistance peaks.

A42531

The magnetoresistance at 0V, -2.0V and -2.4V is plotted in Graph 5.15. These curves are similar to those of A42532 and A21618 which were also measured in the illuminated state. Again, there is no deviation in the 1/B vs Landau index linearity, and the carrier concentration found from the positions in the minima is the same as that from the low B data at $1.9 \times 10^{15} m^{-2}$. It is interesting to note the similarity in the curves for this sample and A42532, as the capacitance characteristics for each sample were dramatically different.

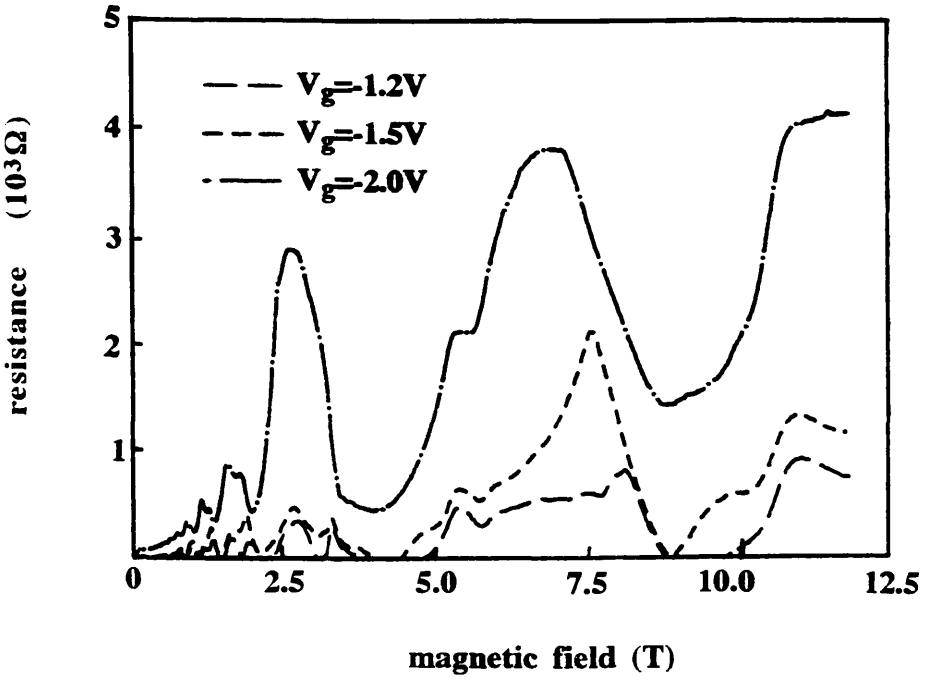


Figure 5.14: High B magnetoresistance data for A42532 at 80mK and gate voltages of -1.2V, -1.5V and -2.0V.

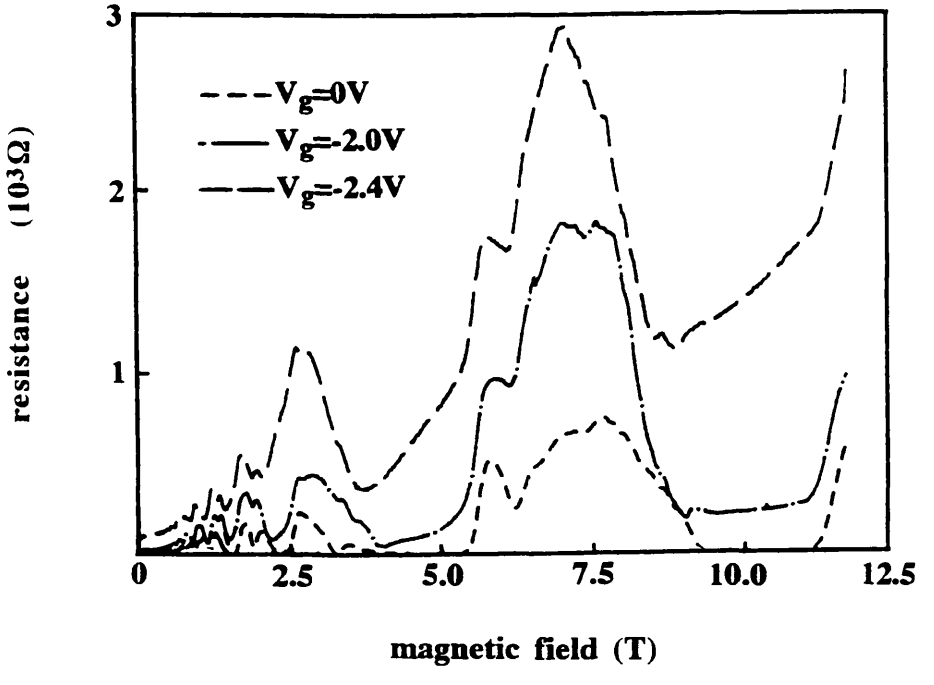


Figure 5.15: High B magnetoresistance data for A42531 at 80mK and gate voltages of 0V, -2.0V and -2.4V.

(b) Estimates of mobility from high B data.

Now that all of the magnetoresistance data has been presented and shown to be consistent it is useful to discuss the electron mobilities in the wire samples.

In this section the electron mobility estimated from the channel conductance will be discussed. The discussion is on a qualitative level and is intended to give an indication of the material and sample quality.

The sample mobilities were calculated using Equation 1.7. In these calculations it is necessary to take into account the effects of the 2DEG regions as well as the active wire region. To illustrate the ambiguity in these estimates upper and lower limits of mobility were calculated with the former calculated assuming that the potential measured between the voltage probes is dropped uniformly across the 2DEG and wire region, and the latter assuming that, even at 0V on the gate, the wire region dominates the conductance.

The estimated mobilities and corresponding electron mean free paths, l_e, (where $l_e=v_f\tau$) are given in Table 5.3. for A21611, A42529, A42532 and A42531. Unfortunately the data for A21614 was all two terminal in nature, so there is no reliable way of estimating the electron mobility.

sample number	conductance at 0V and 0T (S)	max. mobility ($m^2/V/s$)	min. mobility ($m^2/V/s$)	le max. (μm)	le min. (μm)
A21611	0.08	59	7.7	5	1
A42529	0.23	300	39	21	3
A42532	0.45	420	54	30	4
A42531	0.4	490	64	36	5

Table 5.3 Sample mobilities and electron mean free paths.

From this it can be seen for A425 both the upper and lower limits are high, confirming the previous statements that the quality of the material is very high. It can only be assumed that the real mobility in the wires lies somewhere between the limits quoted above, although, given that the carrier concentration was found to be uniform across the wire samples, it is likely to be nearer the upper limit. It should be noted that the estimate of l_e for A42531 is considerably higher than found from the magnitude of the

focusing peaks. As pointed out earlier this is due to the fact that the electrons focused into adjacent wires are more susceptible to small angle scattering effects.

Table 6.1 indicates that A425 is a 'better' material than A216, which makes the observation of confinement effects in the A216 samples as opposed to A425 samples somewhat surprising. However, it may explain the absence of negative magnetoresistance in the low B range for the A425 samples (the low B 4-terminal magnetoresistance of the A216 samples was not measured).

(c) General comments on 'high' B data

The high B data confirms the observations made from the low B data, these being that the A216 samples display a deviation from linearity in the Landau plots indicating the confinement of electrons in the wires, in contrast to the A425 samples which do not display this effect; none of the samples display parallel conductance, and the carrier concentration in the wire samples is, in general, independent of the gate bias. It also shows that one of the spin split peaks (not always the same peak) becomes dominant at high fields and as the gate bias becomes increasingly negative, confirming that electrons in the wires are dominating the magnetoresistance.

5.2.3 MODEL FOR LATERALLY CONFINED ELECTRONS IN A PERPENDICULAR MAGNETIC FIELD.

The standard model for laterally confined electrons in a perpendicular field assumes a parabolic confining potential as this can be solved analytically. Using this model it is possible to calculate the 1D carrier concentration, the separation of 1D energy levels and the wire widths.

The parabolic confining potential is of the form,

$$V(x) = \tfrac{1}{2} m^* \omega_0^{\,2} x^2 \qquad (5.6)$$

The equidistant 1D sub-band levels in a perpendicular magnetic field are then given by,

$$E_n = \frac{h}{2\pi}\omega(n + \tfrac{1}{2}) + \frac{h^2 k_y^{\,2}}{8\pi^2 m^*(B)} \qquad (5.7)$$

where,

$$\omega^2 = \omega_0^{\,2} + \omega_c^{\,2} \qquad (5.8)$$

with w_c the cycloton frequency, and,

$$m^*(B) = \frac{\omega^2}{\omega_0^{\,2}} m^* \qquad (5.9)$$

The positions of the magnetoresistance oscillations due to the depopulation of the 1D sub-bands can be calculated using a two parameter fit, taking into account the

1D density of states. After Berggren et al, 1988, the effective width, W, of the 1D channels is given by,

$$W = \frac{n_{1D}}{n_{2D}} \tag{5.10}$$

where n_{1d} and n_{2d} are the 1D and 2D density of states respectively and n_{1d} is given by,

$$n_{1d} = \frac{2}{\pi}\left(\frac{4\pi m^*}{h}\right)^{\frac{1}{2}} \frac{\omega^{\frac{3}{2}}}{\omega_0} \sum_{v=1}^{n} v^{\frac{1}{2}} \tag{5.11}$$

If the summation is replaced by an integration the following expression is gained,

$$n_{1d} = \frac{2}{\pi}\left(\frac{4\pi m^*}{h}\right)^{\frac{1}{2}} \frac{\omega^{\frac{3}{2}}}{\omega_0} \frac{2}{3} n^{\frac{3}{2}} \tag{5.12}$$

In the limit $w >> w_c$, Equation 5.12 gives,

$$n_{1d}\omega_0 = \frac{4}{3\pi}\left(\frac{4\pi m^*}{h}\right)^{\frac{1}{2}} n^{\frac{3}{2}}\omega_c \tag{5.13}$$

Using Equations 5.10, 5.13 and the standard expression for the 2D density of states, gives,

$$W_{eff} = 2\pi n_{1d}^{1/3}\left[\frac{2h}{6\pi^2 m^* \omega_0}\right]^{2/3} \tag{5.14}$$

The method outlined by Berggren et al was applied to the magnetoresistance data for both A21614 and A21611, and was as follows; in the plots of n vs 1/B, determine ($n_{1d}\omega_0$) from the linear region using Equation 5.13, then substitute this value in Equation 5.12 and using data from the non-linear region find n_{1d} and w_0 separately.

The results obtained from this fit for A21614 and A21611 are given in Table 5.4.

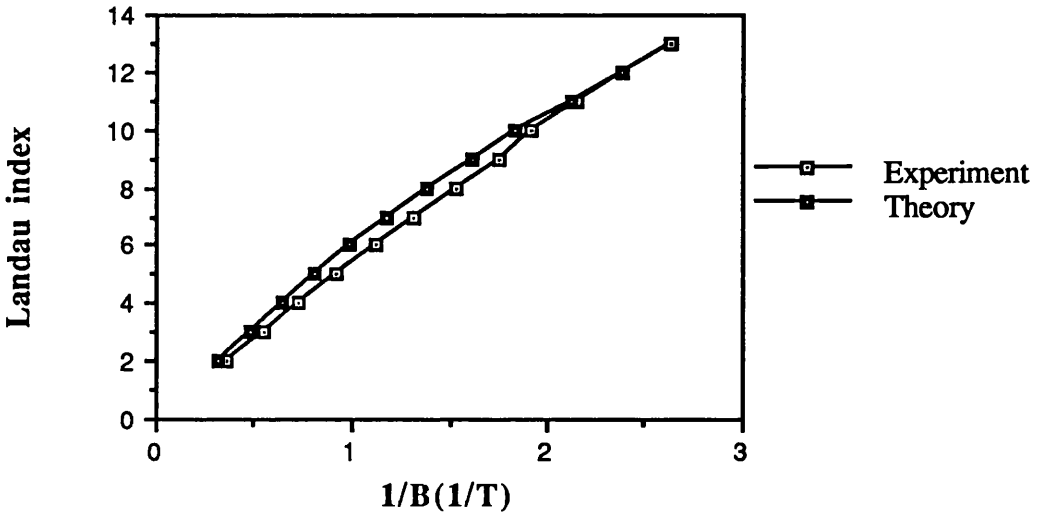
Sample number	Gate Voltage(V)	n_{1d} ($10^8 m^{-1}$)	ω_0 ($10^{11} s^{-1}$)	W_{eff} (nm)	n_{2d} ($10^{15} m^{-2}$)	W_{cap} (nm)	W_{dev} (nm)
A21614	-0.2	3.0	7.1	220	1.4	280	200
A21614	-0.6	2.5	8.6	190	1.3	30	90
A21611	-0.85	8.6	9.0	260	3.3	340	290

Table 5.4 Table showing the parameters calaculated using the Berggren model.

The wire widths estimated from the capacitance and position of the deviation in the magnetoresistance data (found using Equation 1.17), W_{cap} and W_{dev} respectively are also given.

From Table 5.4 it can be seen that the fit did not give wire widths and carrier concentrations in quantitative agreement with other measurements, suggesting that the confinement potential was not parabolic in nature, although qualitatively the data is reasonable with both the wire widths and the 1D density of states decreasing as the gate voltage is made more negative (for A21614) as expected. The parameters found for A21614 at -0.6V in fact give the worst agreement, which is somewhat surprising as the parabolic potential is most likely to be applicable in thin wires. However, this may be due to the fact that only the 2-terminal resistance for A21614 was measured resulting in some ambiguity in the absolute position at which the Landau levels were populated, with this becoming increasingly so as the gate voltage was made more negative.

A fit of the data for A21611 at a gate voltage of -0.85V is given below in Plot 5.1.



Plot 5.1 Experimental and predicted plots of n vs 1/B for A21611 at a gate voltage of -0.85V.

From this it can be seen that the predicted data displays curvature over the entire 1/B range, whereas the experimental data is linear until about 1/B=1.7T^{-1} where a deviation is observed. This absence of curvature in the experimental data gives substance to the suggestion that the confinement potential is not accurately represented by the parabolic model. However, to model the potential in the wire accurately would be very difficult, and almost certainly could not be done analytically.

5.3 MAGNETOCAPACITANCE

The magnetocapacitance measurement system was developed late in the project and so there is a limited range of data available. All of the magnetocapacitance was measured on A42531 and A42532 - the capacitance was measured at constant gate biases as a function of B.

The measurement of magnetocapacitance is somewhat different in nature to the magnetoresistance measurement. The capacitance is measured between the gate and the source/drain contacts so only the charge under the gate is sensed, and hence the regions of unpatterned 2DEG connecting the wire region to the ohmic contacts do not contribute to the magnetocapacitance. This makes the measurement of magnetocapacitance a very attractive method for investigating quantum effects.

In many respects the magnetocapacitance is very similar to the magnetoresistance in that oscillations arise due to the formation of Landau levels and edge states. However, the magnetocapacitance oscillations arise specifically as a result of oscillations in the density of states as the Fermi level moves through edge and localised states, whereas the magnetoconductance oscillations also reflect the reduction of scattering effects in edge states. Therefore, the magnetocapacitance can be used not only to estimate the carrier concentration, but also as a qualitative guide to the number of localised states in a sample.

(a) Presentation of data

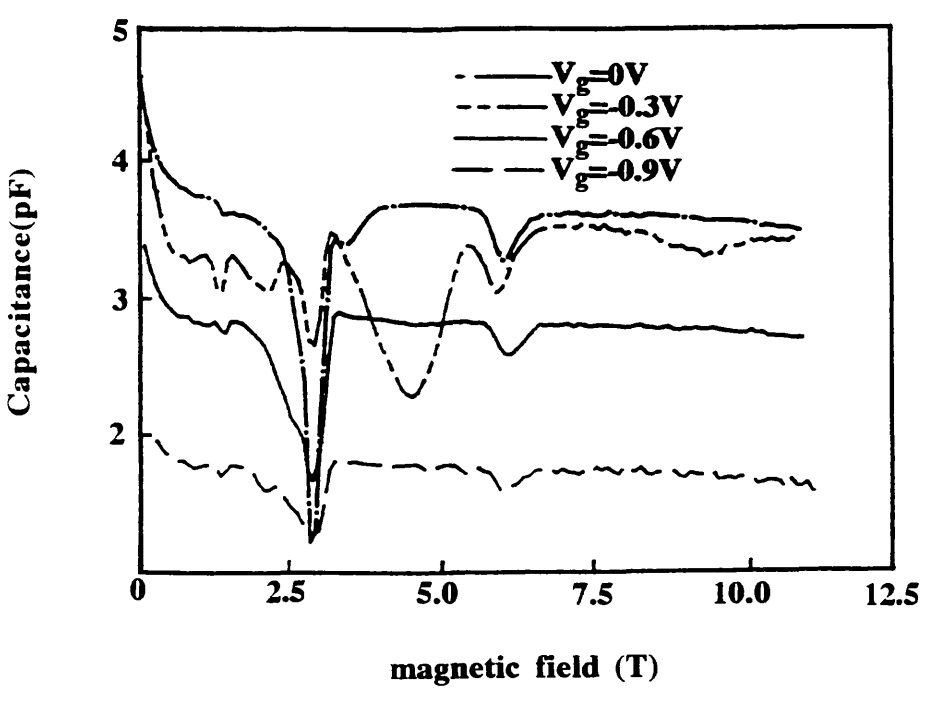
A42532

The magnetocapacitance of this sample was measured in the initial dark state and in the illuminated state at both 4.2K and 80mK.

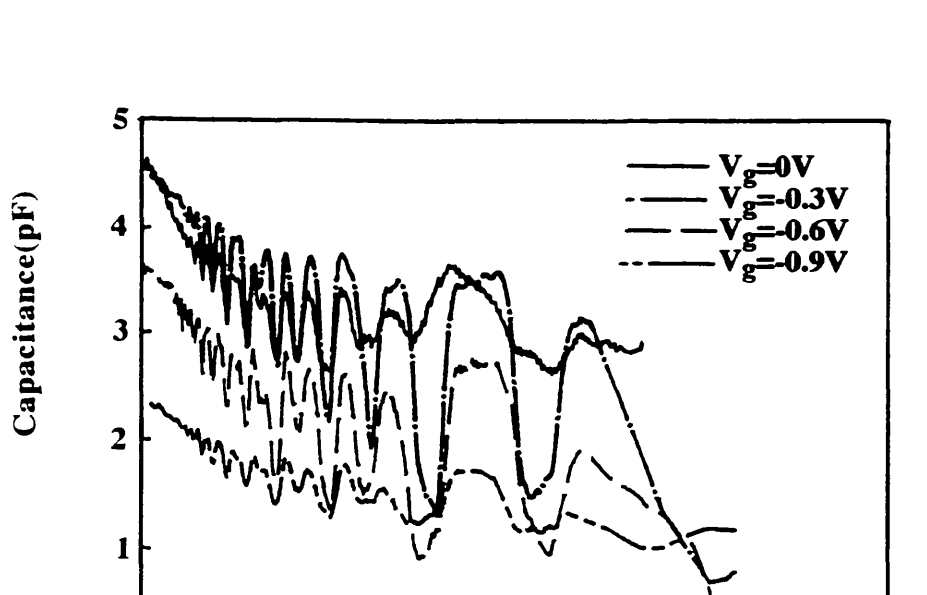
The data taken in the dark state at 4.2K is shown in Graph 5.16(a), with that taken at 80mK for low B in Graph 5.16(b) and high B in Graph 5.16(c).

From Graph 5.16(a) it can be seen that at 4.2K the curves show a sharp drop in the capacitance at low B, and thereafter some signs of oscillations, although not very well defined except at 0V on the gate, until at about 2.6T the second Landau level becomes apparent. At fields above this all of the curves display the first Landau level at about 6T, and then only the curve taken with 0V on the gate shows the 2/3 minimum at 9.5T. It is difficult to estimate from these characteristics a carrier concentration.

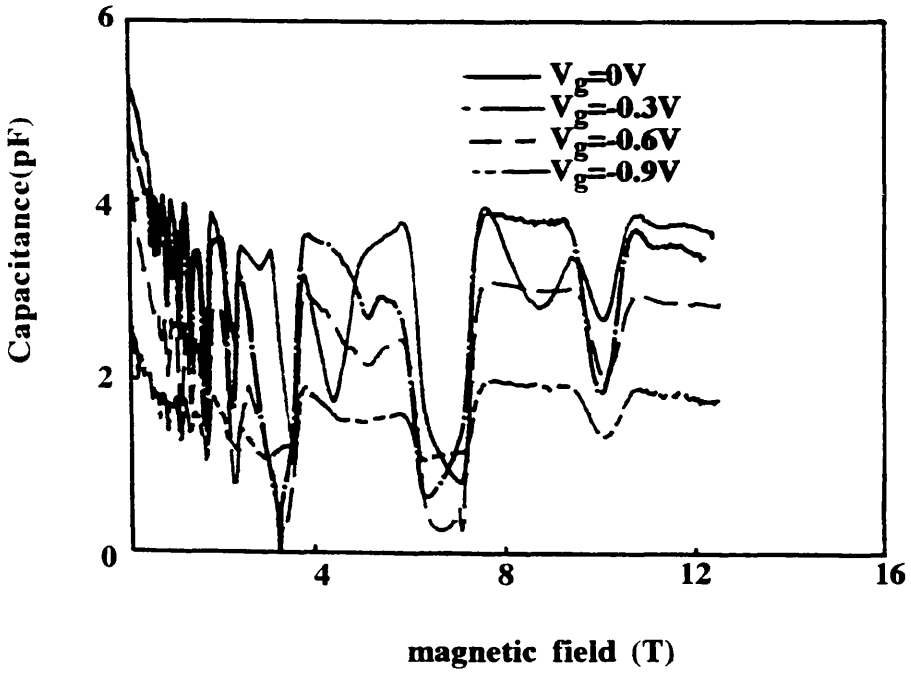
From Graph 5.16(b) it can be seen that the low field, 80mK, magnetocapacitance displays Shubnikov-de Haas-like oscillations. If these are treated as such, the carrier concentration in this state is estimated to be $1.3 \times 10^{15} m^{-2}$. Spin splitting of the Landau levels starts at about 0.25T.



Graph 5.16(a): High B magnetocapacitance data for A42532 at 4.2K and gate voltages of 0V, -0.3V, -0.6V and -0.9V.

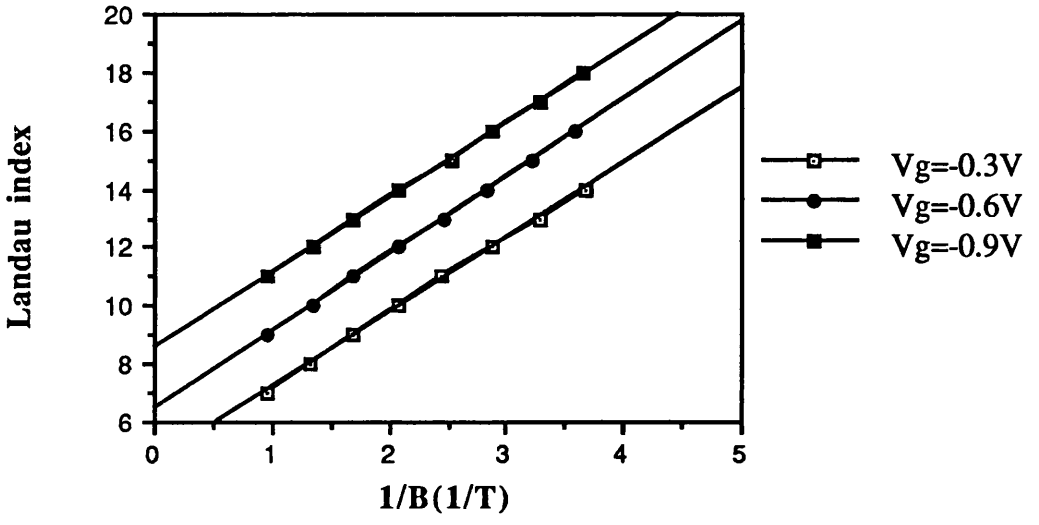


Graph 5.16(b): Low B magnetocapacitance data for A42532 at 80mK and gate voltages of 0V, -0.3V, -0.6V and -0.9V.



Graph 5.16(c): High B magnetocapacitance data for A42532 at 80mK and gate voltages of 0V, -0.3V, -0.6V and -0.9V.

The high B curves, in Graph 5.16(c), show the low B ~~Shubnikov-de Haas~~ oscillations, and then at high fields well defined minima at 1 and 2/3. The 0V curve also displays the 4/5 minima at 8.5T. The carrier concentration from these is estimated to be $1.3 \times 10^{15} m^{-2}$. The Landau plots for the low field data at 80mK are shown in Graph 5.17.

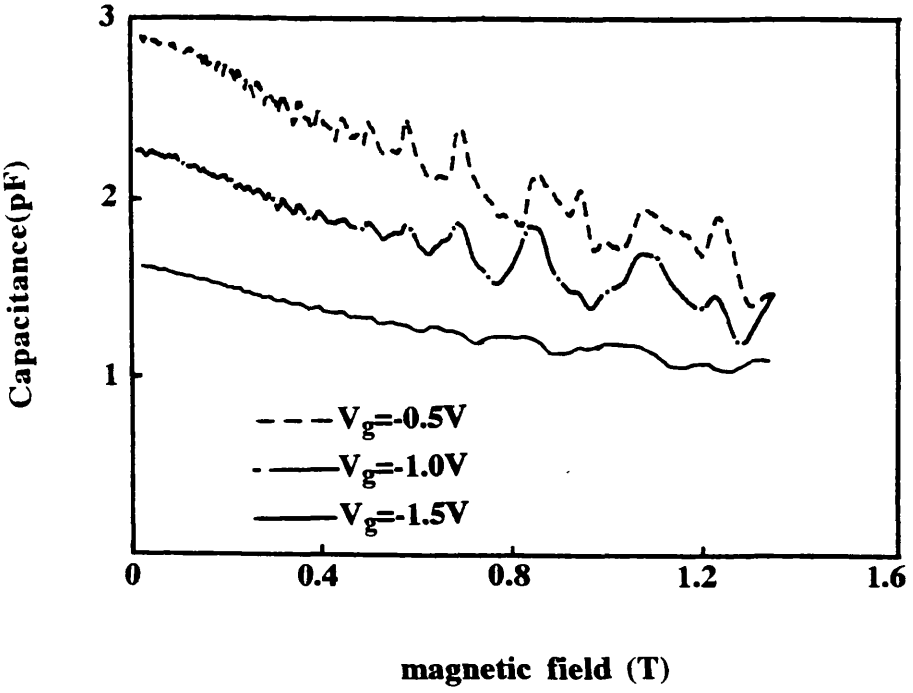


Graph 5.17: Position of resistance minima in 1/B against Landau index for A42532, magnetocapacitance.

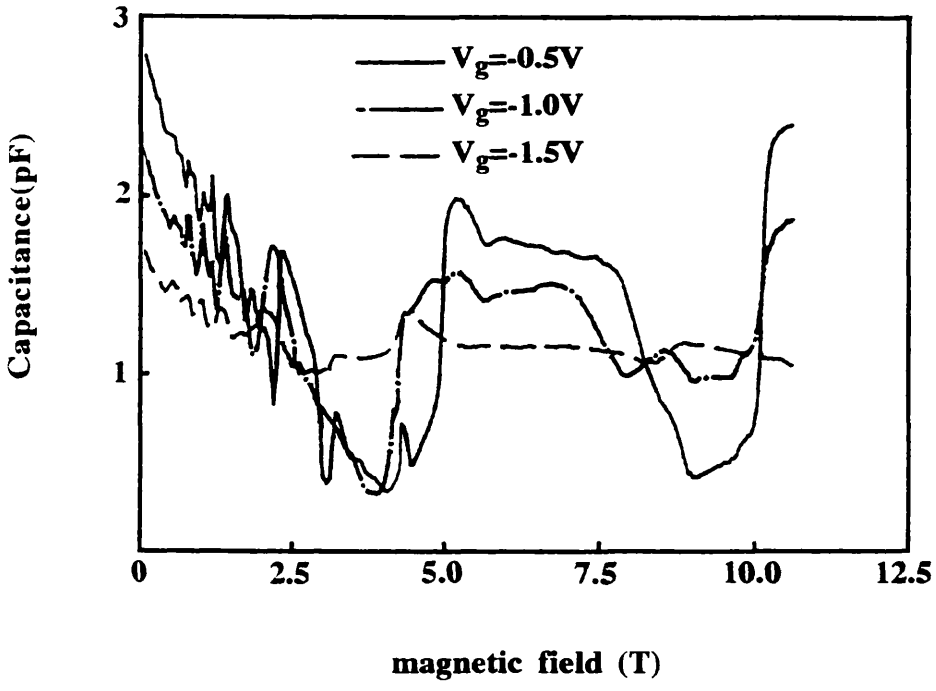
Again these curves display a remarkable degree of linearity, with no sign of any deviation at any gate bias, and no carrier concentration dependence on the gate bias. The dark state estimate of $1.3 \times 10^{15} m^{-2}$ is in reasonable agreement with that found from A42529, $1.7 \times 10^{15} m^{-2}$, which was also measured in the dark.

The illuminated state characteristics are shown in Graph 5.18. From this it can be seen that the capacitance is considerably more noisy than that in the dark state, with the magnitude of the oscillations greatly reduced. The estimated carrier concentration from this sample is $1.8 \times 10^{15} m^{-2}$, which is the same as found from the magnetoresistance measurements.

It is interesting to note the differences in the dark and illuminated state characteristics, the most obvious of which is the reduction of the depth of the minima in the illuminated state, suggesting that electrons were populating the region between edge states, probably in localised states. This is not an unlikely scenario in the illuminated state.



Graph 5.18(a): Low B magnetocapacitance data for A42532 in illuminated state, at 80mK.



Graph 5.18(b): High B magnetocapacitance data for A42532 in illuminated state, at 80mK.

A42531

This sample was measured in the illuminated state only. The magnetocapacitance taken at selected gate biases for this sample is shown on Graph 5.19, from which it can be seen that the capacitance is very similar to that of A42532 in the illuminated state. The estimated carrier concentration is $1.9 \times 10^{15} m^{-2}$ which is in good agreement with that found from the low, and high B magnetoresistance data. Again there is no deviation seen in the Landau plots, although it should be noted that there it was very difficult to estimate the position of the minima due to the shallowness of the minima and the noise level.

(b) General comments on magnetocapacitance data

The magnetocapacitance data confirm the observations made in the previous section on magnetoresistance. These being that none of the samples display signs of parallel conductance, the carrrier concentrations are in general agreement with those estimated from the magnetoresistance, effects due to the reduced dimensionality of the wires are not observed, A425 samples measured in the dark state display states in the fractional regime, indicating the high quality of the material, and illuminating the samples increased the density of states between the edge states.

The most significant feature of the magnetocapacitance data is that it provides absolute evidence that the carrier concentrations associated with the wire region are independent of the gate bias, and, since the magnetoresistance data is in general agreement with the magnetocapacitance, that the magnetoresistance measured was due to electrons in the wires.

5.4 SUMMARY

The main features of the magnetotransport and magnetocapacitance data, are summarised below.

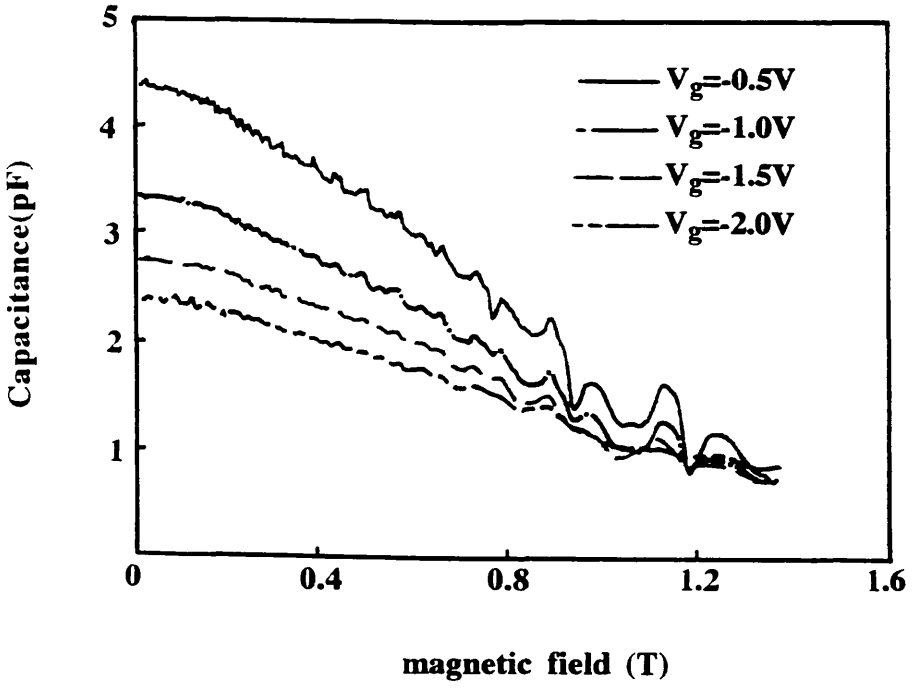
(1) Focusing peaks were observed in the low B magnetoresistance for two samples.

(2) Fractional quantum Hall states were observed in A425 samples measured in the dark state, indicating the high quality of the material.

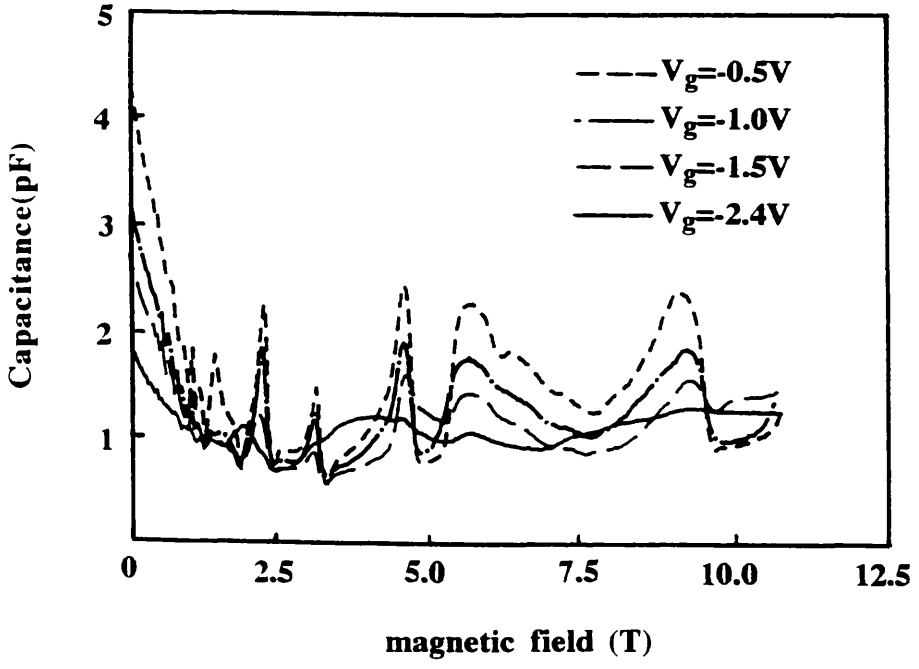
(3) None of the samples displayed any evidence to suggest that there was parallel conductance.

(4) The carrier concentrations were observed to be almost independent of the gate bias, with the notable exception of A42529 at -1.4V.

(5) The plots of 1/B vs Landau index for both A216 samples displayed evidence of deviations indicating electron confinement in the wires.



Graph 5.19(a): Low B magnetocapacitance data for A42531 in illuminated state, at 80mK.



Graph 5.19(b): High B magnetocapacitance data for A42531 in illuminated state, at 80mK.

(6) The plots of 1/B vs Landau index for every A425 sample, at every gate bias used, were linear, displaying no evidence of a deviation in the limit where the wire width was of a similar magnitude to the cyclotron diameter.
(7) The carrier concentration estimated from the magnetoresistance was in good agreement with that estimated from the magnetocapacitance.
(8) The carrier concentrations estimated from the magnetoresistance and magnetocapacitance were found to be significantly lower than those estimated from the capacitance data discussed in section 4.
(9) The conductance data suggests that the electron mobility in the A425 samples was extremely high.

The absence of the deviation in the positions in 1/B vs Landau index for the A425 samples, and the discrepancy in the carrier concentrations will be discussed fully in Chapter 6.

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CHAPTER SIX

DISCUSSION OF EXPERIMENTAL DATA

6.1 INTRODUCTION

In this chapter the experimental data presented in Chapters 4 and 5 will be discussed. This discussion will be presented in four sections, comparison and discussion of carrier concentrations, absence of deviation in the Landau plots, absence of confinement effects in the capacitance data and finally a summary. The data and results will also be compared to those of other groups.

6.2 CARRIER CONCENTRATION

In this section the carrier concentrations found from the Shubnikov-de Haas data and the capacitance data will be compared and discussed.

The carrier concentrations found from the capacitance data and the magnetoresistance are given overleaf in Table 6.1. Following the convention of Chapter 4, Q_W and Q_F are the charge in the wire and gated regions of the wire sample capacitance characteristics, respectively.

From Table 6.1 it can be seen that in general the carrier concentrations estimated from the capacitance characteristics for both the wire and FET samples are significantly higher than those found from the Shubnikov de Haas data. The most obvious source of this excess charge in the system is the population of the conduction band in the doped AlGaAs layer resulting from either a parallel conducting layer in the bulk material or the fabrication process employed to form the resist strips - the Shubnikov-de Haas data proved conclusively that none of the samples measured displayed parallel conductance, leaving the latter suggestion as the more likely. However, some of the data suggest that this may not be the correct interpretation.

It should be noted that although Kotthaus et al, 1989, performed experiments similar to those described in this thesis, the data presented in the publication was insufficient to include in this discussion.

Sample number	n_{2d} using Q_W from capacitance (10^{15} m^{-2})	n_{2d} using Q_F from capacitance (10^{15} m^{-2})	n_{2d} from Shubnikov de Haas (10^{15} m^{-2})
A21614	2.0	0.7	1.0
A21611	4.0	2.9	2.1
A21618 (FET)	—	2.7	1.5
A42529	2.8	6.5	1.7
A42532 (dark state)	3.4	3.1	1.3
A42532 (illuminated state)	2.9	2.0	1.8
A42531 (illuminated state)	7.1	3.5	1.9

Table 6.1: Comparison of carrier concentrations estimated from Shubnikov-de Haas and capacitance data, for wire samples and A21618, an FET sample.

Consider firstly the A216 samples. For A21618, the FET sample, the carrier concentration found from the capacitance is significantly higher than that found from the Shubnikov-de Haas. For the wire samples the carrier concentration in the gated region is in reasonable agreement with that of the Shubnikov de Haas estimate, but both have higher carrier concentrations in the wires. The fact that for A21614 the agreement is poorer than for A21611 is somewhat surprising, as the latter was illuminated, which from previous experiments was shown to pull the conduction band in the AlGaAs below the Fermi level. However, this excess charge is unlikely to be in the conduction band in the AlGaAs as neither of the FET samples (A21615 and A21618) measured with A21611 and A21614 displayed any signs of the step (seen for example in A2169 and A21610), indicative of electrons in the conduction band in the AlGaAs.

Now consider the A425 samples. For A42529 and A42531 the carrier concentrations estimated from the charge in both the gate and wire regions were found to be consistently higher than the estimates made from the Shubnikov-de Haas data, but for A42532 the FET and Shubnikov-de Haas data were in reasonable agreement with only the wire region indicating excess charge. This suggests that for A42529 and A42531 electrons were populating the conduction band in the AlGaAs in both the gated region and the wire region. However, again, there are several experimental observations which appear to contradict this suggestion. Firstly, consider the capacitance characteristic for A42529, which is shown in Graph 4.17. In Section 4.4.4.(b) it was suggested that the increase in the capacitance at -0.5V indicated the population of the conduction band in the AlGaAs. In a later section, on the discussion of the Davies model (Section 4.9.3), it was estimated that if the charge in the wire region was in the 2DEG, then the carrier concentration across the sample was uniform at -0.6V on the gate. The significance of this is that this gate voltage is more negative than the voltage at which the AlGaAs is depleted of charge, implying that the charge in the wire region not in the conduction band in the AlGaAs (although it should be noted that implicit in this is the assumption that the carrier concentration under the resist should be the same as that under the gated regions). For A42531 the capacitance characteristic shows an increase at about -0.2V, suggesting that the conduction band in the AlGaAs is being pulled below the Fermi level, which may explain the high carrier concentration in the gated region but is insufficient to account for the very high carrier concentration calculated in the wire region.

A42532, in its illuminated state, for which the capacitance characteristic is shown in Graph 4.18(b), is particularly interesting because the Shubnikov de Haas carrier concentration remains constant over the full gate voltage range when the capacitance and the channel conductance both indicate that the amount of charge in the

system is drastically reduced, shown in Graph 4.35(b). It is tempting to attribute the step seen in the characteristics to geometrical effects, for example large scale non-uniformity in the wires, but the dark state capacitance characteristic does not display this step suggesting that it must arise from a macroscopic sample effect. The presence of the step in both of the characteristics suggests that only a fraction of the charge in the system is contributing to the magnetoresistance, but again, since the channel conductance shows a step at the same voltage as the capacitance, it seems unlikely that this extra charge is present in the conduction band in the AlGaAs layer.

In conclusion the samples fabricated on both A216 and A425 suggest that the capacitance measurement consistently senses more charge than the Shubnikov-de Haas measurement. It should be noted that the estimates of carrier concentration from the capacitance data are, if anything, a lower limit due to the finite time required to transfer charge. The data shows that this excess charge found in both the FET and wire samples cannot be attributed to the presence of electrons in the conduction band in the AlGaAs, or in DX centres in the AlGaAs. Two reasons are proposed for the apparent excess charge measured in the capacitance characteristics, the first is that the Shubnikov-de Haas measurement is sensitive only to high mobility electrons and the second is that the capacitance measurement is sensitive to charge in shallow traps in the AlGaAs layer.

Consider firstly the measurement of the Shubnikov-de Haas effect, which was discussed in terms of edge states in Section 1.5.3. The edge state model of magnetotransport suggests that mobile charge travels in channels at the edges of the sample, although it was also pointed out that charge also exists in localised states in the bulk of the material. Charge in localised states does not affect the positions of the minima in the magnetoresistance oscillations, and so does not contribute to the estimate of the carrier concentration. However, capacitance is sensitive to charge in both edge and localised states, thereby increasing the estimates of carrier concentration taken from the capacitance data above those found from the Shubnikov-de Haas oscillations. Although it should be noted that charge in localised states alone is unlikely to be the sole source of the excess charge in the capacitance characteristics.

As noted above, there has been much discussion in this thesis on DX (deep donor) centres and the effects of having electrons in the conduction band in the AlGaAs. However, it was concluded that neither could be responsible for the excess charge detected by the capacitance measurement, since none of the capacitance characteristics display hysteresis in the gate voltage and charge in the conduction band in the AlGaAs can contribute to the magnitude of the capacitance and so be detected. Therefore, it is proposed that the excess charge is due to *shallow* traps in the AlGaAs, with the electrons depleted from these traps by the gate voltage, but unable to

contribute to the magnitude of the capacitance due to the finite time required to transfer charge. This makes it necessary to deplete the shallow donor states before 2DEG depletion can occur, thereby extending the active device voltage range without being able to detect the presence of such states in the capacitance magnitude. This is the most likely explanation, but it is difficult to present any further evidence to give it substance.

6.3 ABSENCE OF CONFINEMENT EFFECTS IN MAGNETORESISTANCE FOR A425 SAMPLES

This discussion will be presented in two sections, the first of these presenting in greater detail the wire widths as a function of gate bias, to determine more quantitatively the limits in which the effect should have been observed on the A425 samples, and the second presenting the samples and data from other groups, to make direct comparisons with samples which displayed the confinement and size effects.

6.3.1 WIRE WIDTHS AS A FUNCTION OF GATE BIAS, AND PREDICTED POSITIONS OF MINIMA FOR A425 SAMPLES

The wire widths estimated from the capacitance characteristics and the predicted fields at which size effects should have occurred are given overleaf in Table 6.2. The critical fields were estimated using Equation 1.18. The wire widths, W, were estimated from,

$$W = \frac{Q_w}{en_{2d}lN} \qquad (6.1)$$

where l is the length of the wire, N is the number of wires, and the carrier concentrations used were found from the capacitance data as opposed to the Shubnikov de Haas data. This is not unreasonable, even if the conduction band in the AlGaAs is populated, as it can be assumed that each wire contains the same amount of charge regardless of the position of such charge.

From Table 6.2 it can be seen that for the A425 samples the magnetoresistance for each of the samples was measured at voltages close enough to the cut-off voltage to observe the effects of the reduced dimensionality of the wires on the transport, although for A42531 at -2.2V and -2.4V the deviation is predicted to occur at fields at, or above the first Landau level. However, in this limit the gradient of the plots, in the presence of confinement effects, should have been sufficiently curved to detect the formation of magneto electric sub-bands. The data for A42532 is not presented in this

Sample number	gate voltage (V)	wire width (nm)	B_c (T)
A21614	-0.2	300	0.27
	-0.6	30	2.7
A21611	-0.6	450	0.45
	-0.85	290	0.71
A42529	-1.2	230	0.57
	-1.4	100	1.3
A42531	-1.0	330	0.44
	-1.8	140	1.0
	-2.0	95	1.5
	-2.2	60	2.4
	-2.4	20	7.1

Table 6.2: Wire widths estimated from capacitance data, as a function of gate voltage, and position at which deviations from the Landau plot linearity were expected.

table because of the distorted nature of the capacitance curve, which, it was felt, could not be interpreted usefully using the methods employed for the other characteristics.

The data shown in Table 6.2 dispels the possibility that the magnetoresistance was not measured in suitable gate voltage and magnetic field ranges.

6.3.2 COMPARISON OF DATA FROM VARIOUS GROUPS

To investigate further the reason for the absence of confinement effects in the A425 magnetoresistance taken in this project the data was compared, in detail, with that of other groups. The materials, samples and results obtained are given overleaf in Table 6.3.

From Table 6.3 it can be seen that there is no obvious reason for the complete absence of the size effects in the magnetotransport for the A425 samples, as they appear, if anything, to be fabricated on higher quality material. The results of Kotthaus et al are of particular interest as the sample geometry used was very similar to that used in this project, although the wires were fabricated using holographic techniques, as opposed to electron beam lithography, and were half the width of the wires measured in this project.

For most of the experiments detailed in Table 6.3 the measurements taken were on wires of smaller widths than fabricated by the author, which may explain the absence of size effects, although the A216 samples displayed the deviation, as did the data of Hirler et al, which was measured on wires in the range 150nm-500nm and that of Berggren et al using a single split gate of separation 1μm. The only other feature unique to the A425 samples is the extremely high electron mobility.

6.3.3 CONCLUSION

In conclusion the reason for the absence of any deviation in the positions of the magnetoresistance minima in 1/B vs Landau index is not fully understood. Table 6.2 demonstrates that the magnetoresistance was measured at suitable fields and gate biases, and Table 6.3 gives no obvious indication as to why the A425 samples should not display the magnetic field size effects seen in the A216 samples and by many other groups. There are two possibilties for the absence of these effects. Firstly, the very high mobility of the A425 samples - of all the data published, successfully showing deviations at appropriate fields, none had mobilities of $>10 m^2V^{-1}s^{-1}$. This is the only obvious difference between the previously published data and the data taken on the A425 samples, although why this should influence what is really just a size effect is not understood. The second possibility is that if there was charge in shallow donors

	material details		sample details				
research group	n_{2d} (10^{15} m^{-2})	μ (m^2/Vs)	type of sample	lith. width- S (nm)	conduct. width- W (nm)	wire length (μm)	effects observed
Berggren et al - 1986	1.5	-	single split gate	1000	1000	15	deviation in linearity of positions of minima in magnetoconductance in 1/B vs Landau index when W<250nm
Van Houten et al - 1987	2.5	10	single shallow dry- etch	500-1500	110-390	10	deviation in linearity of positions of minima in magnetoconductance in 1/B vs Landau index
Smith et al - 1987	5.0	50	multiple gated dry-etched	200 - 400	90 - 180	250	1-D capacitance steps and deviation in linearity of positions of minima in magnetocapacitance in 1/B vs Landau index
Kotthaus et al - 1989	6.0	-	multiple split gate	200	200	6000	deviation in linearity of positions of minima in magnetoconductance in 1/B vs Landau index/1-D sub-band separation from infra-red spectroscopy
Ismail et al - 1989	-	25	multiple gated dry-etched	85	35	5 and 10	Steps in conductance as a function of gate bias, resulting from 1-D confinement in wires
Hirler et al - 1990	3.6	8	multiple gated wet-etched	500-150	500-150	300	deviation in linearity of positions of minima in magnetoconductance in 1/B vs Landau index/1-D sub-band separation seen using tunneling spectros.
Kinsler	1.0-2.7	8-59	multiple split gate on A216	400-550	400-550	17	deviation in linearity of positions of minima in magnetoconductance in 1/B vs Landau index.
	1.3-1.9	39-490	multiple split gate on A425	400-550	400-550	17	Electron focusing effects/no deviation/no negative magnetoresistance

Table 6.3: Comparison of relevant data.

the AlGaAs this may interfere with the transport in the channel, by perhaps distorting the confining potential. It is interesting to note that these two explanations may be connected, as mobile charge in the AlGaAs would be expected to screen ionised donor charge and hence reduced scattering and increase mobility. However, a detailed 2D Poisson Schrodinger simulation would be required to confirm such an argument.

6.4 ABSENCE OF CONFINEMENT EFFECTS IN CAPACITANCE

Fortunately the measurement of capacitance oscillations is not as common as the measurement of size effects in the magnetotransport experiments, and so is less suprising in its absence in the samples measured in this project. The only successful measurements of 1-D confinement effects using capacitance techniques were performed by Smith et al. As noted previously, Kotthaus et al used samples similar to those used in this project - they also failed to see any oscillations in the capacitance characteristics. The wires on the sample used by Smith et al were formed using etching techniques, with the gate deposited over GaAs and AlGaAs, so under the gate the surface was uniform, whereas the samples used in this project, and by Kotthaus et al, were formed by depositing a gate over strips of insulating resist, so the surface of the sample was covered alternately by resist and gate metal. This non-uniformity on the surface of the material may affect the device properties as, in recent years, surface states have been recognised as being significant, although no quantitative evidence for the effects of surface states has been produced. The fact that the Davies model (4.9.3) was shown to give reasonable agreement with the data when the model takes into account the effect of surface states, suggests that these states may indeed be affecting, if not dominating, the device characteristics.

6.5 SUMMARY

In summary the data presented in the first section highlights a discrepancy in the carrier concentrations found from the capacitance and the Shubnikov-de Haas data which cannot be wholly attributed to the presence of electrons in the conduction band in the AlGaAs. Two explanations were proposed the first being that only a proportion of the charge in the 2DEG contributes to the Shubnikov-de Haas oscillations the rest residing in localised states, and the second that shallow donor states in the AlGaAs layer extend the device depletion regions.

The section discussing the absence of the deviation from linearity in the Landau plots for the A425 samples does not give clear indication as to why this should be the

case, as the A216 samples and data presented by other groups on similar samples, but with lower mobilities, do display the deviation.

The final section, discussing the absence of oscillations in the capacitance, suggests that it is the non-uniformity at the surface of the samples which prevents the observation of any such oscillations in the capacitance.

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CHAPTER SEVEN

CONCLUSIONS

The main conclusions reached from the data presented in this thesis are summarised in this chapter. The aims of the project outlined in Section 1.4.2 were to investigate confinement effects in conductance, capacitance, magnetoconductance and magnetocapacitance. In fact only the magnetoresistance of the A216 samples displayed any confinement effects, so in terms of the initial aims the project was a dismal failure. However, the range of the experiments performed has highlighted several significant problems in the standard understanding of the GaAs/AlGaAs heterostructure, and it is in this respect that the experiments are most interesting.

The range of samples and capacitance characteristics measured in the course of this project has shown some unexpected features. The, so called, 'typical' curve presented in Graph 4.5 is in fact often not observed, with the most common deviation being a step in the capacitance characteristics, as seen in the characteristics of A21614 and A42532, Graphs 4.9 and 4.18(b) respectively. This step is not explicable in terms of standard models for squeezed wires. These steps in the capacitance characteristics are not unique to the samples fabricated in this project as they were referred to in the Kotthaus paper, although not presented. In fact, the capacitance characteristic presented in the Kotthaus paper (of the 'typical' type) did not correspond to the sample under discussion in the later stages of the paper. Unfortunately the origin of the steps in the capacitance characteristics, and the corresponding steps in the conductance, are not understood.

The Davies model for squeezed wires, discussed in Sections 1.7 and 4.9.3 was found to be applicable, with a significant proportion of the large number of samples measured in this project displaying wire threshold voltages in remarkably good agreement with the model, as do the samples of various other groups. This model of gated wires assumes that the surface of the material is an equipotential which necessarily requires that as the wires are depleted there is a transfer of charge from the 2DEG to the surface states. However, at low temperatures, and by the current

understanding of the heterostructure system, this can only be regarded as physically unlikely.

There is always a discrepancy in the carrier concentration estimates from the Shubnikov-de Haas and capacitance measurements in both the wire and the FET samples, with the capacitance consistently sensing more charge. The possibility that the conduction band in the AlGaAs was populated was discussed and dismissed. Two suggestions were made as to why this difference should arise, the first being that the Shubnikov-de Haas measurements were sensitive only to high mobility electrons in the 2DEG whereas the capacitance measurements were sensitive to all electrons present, and the second that the capacitance measurement was sensitive to charge in shallow donors in the AlGaAs. However, there is no quantitative evidence to give any of these suggestions any substance.

The capacitance data did not display the oscillations observed by Smith et al, due to electron confinement in the wires. Experiments similar to those conducted in this project were performed by Kotthaus et al, and these also showed no oscillations in the capacitance. It is proposed that this may be due to the non-uniformity at the surface of the material produced by the fabrication techniques employed.

Finally, it can be seen that there are many questions raised by the work conducted in this project, which are as yet unanswered.