Lateral and longitudinal surface superlattices on Shallow GaAs Heterostructures

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Abstract

Longitudinal and lateral surface superlattices were fabricated on GaAs heterostructures. Most devices were made on shallow materials to exploit the proximity of the two dimensional electron gas to the surface, although some devices were fabricated on deeper material to compare their behaviour with the results obtained from devices fabricated on shallow material. The superlattices were fabricated on Hall-bars enabling four probe measurements to be made. Measurements were made at temperatures of 20 K, 4.2 K or 1.5 K depending on the requirement of the experiment and the measurement system used.

Longitudinal superlattices were fabricated using negative resist techniques. In this process a periodic array of resist strips was deposited along the channel of a Hall-bar parallel to the direction of current flow. An overlying Schottky gate was deposited on the array. Bias was applied to confine the electrons electrostatically under the resist. As negative bias is further increased the channels of electrons become squeezed and should show evidence of one dimensional quantum confinement, although no evidence of one dimensional confinement was seen in the samples fabricated in this work. The values of negative voltage which define the points at which electrons are depleted from the ungated areas (the cut-off voltage) and gated areas (the threshold voltage) are compared to theory. It was found that, due to complicated factors inherent in the fabrication process, the data did not agree well with models which predict the cut-off voltage.

Lateral surface superlattice samples were fabricated using positive resist. This technique leaves strips of metal which cross the Hall-bar channel perpendicular to the direction of current flow. Superlattices were fabricated with periods down to 60 nm, the smallest period yet reported. Using lateral superlattices allows an estimation of the potential in the 2DEG induced by the surface gate, from the analysis of a series of oscillations in the longitudinal magneto-resistance measurement which are known as commensurability oscillations. The variation of this induced potential with gate bias was also studied. This was found to vary depending on the type of barrier material used. Shallow AlAs barrier material has a layer of screening electrons around the donors. This screening layer reduces the induced potential in the 2DEG. This layer of screening electrons is not present in shallow AlGaAs barrier material so larger induced potentials are observed using these samples. A secondary aim, measuring the smallest period superlattices, was to enter a purely quantum regime where new physical effects are predicted. The devices with the smallest periods did not show any evidence of quantum effects and the possible reasons for this absence are discussed.

After the failure of the longitudinal negative resist samples to give consistent values of cut-off voltage, a third type of gate structure was fabricated, called a finger superlattice. This finger structure is similar to a lateral superlattice but was designed so that the strips of metal did not completely cross the channel, which allows access to the bulk regions between the metal fingers. These samples were fabricated using positive resist techniques and were used to compare the cut-off voltages with two theoretical models. The theoretical models differ in the boundary conditions assumed at the ungated areas, which lead to quite different results. The longitudinal superlattices did not give conclusive evidence of which model was correct because of the unquantifiable effect of gate bias through the resist ribs. The finger superlattices were fabricated to overcome this problem, and offer strong evidence that one model, the 'frozen surface' model, correctly describes the behaviour of ungated GaAs at low temperatures.

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Chapter one.

Introduction and outline.

1.1 Introduction

This thesis will present experimental work carried out in Glasgow University from October 1992 until October 1995 using shallow heterostructures with patterned gates to modulate the two dimensional electron gas. Most of the work carried out was a continuation of experiments begun by previous students in Glasgow, M. Kinsler with longitudinal superlattices and R. Cusco with lateral superlattices.

In conventional heterostructures the conducting layer is about 100 nm from the surface. Material recently grown in Glasgow has the conducting layer only 28 nm from the surface. It was hoped to exploit this development in two ways, firstly by increasing the magnitudes of the potentials in the conducting layers and secondly bringing the 2DEG closer to the surface allows devices with feature sizes of less than 100 nm to be investigated.

Transport by electrons in multiple narrow conducting channels was investigated. Exploiting the increased potential from the surface gate on shallow materials, it was hoped to observe evidence of quantum transport in the wires. Devices were fabricated by use of high resolution negative resist (HRN) ribs with an overlying Schottky gate. A negative voltage applied to this gate should define narrow channels of electrons underneath the strips of resist. The existence of quantum transport is probed by orthodox conductance and capacitance techniques, and by equivalent measurements in a magnetic field. Because of problems inherent in the fabrication process for HRN rib longitudinal wires, a fundamental question remained unresolved after the completion of the longitudinal wire work. This problem concerned the surface condition of ungated areas at low temperatures. There are two models describing the surface

condition, known as the 'pinned' and 'frozen' models, and these predict rather different experimental behaviour. However, it was not possible to differentiate between them unambiguously because the gate on top of the resist strips has some unquantifiable effects. A side elevation of a wire formed by HRN ribs is shown in fig 1.1a).

Devices were also fabricated with positive resist using a large period lateral surface superlattice where the metal strips do not completely cover the channel (there is a ten micron gap left down one side of the channel leaving the areas between the fingers open to the bulk area of the 2DEG). This type of gate is called a side gated finger superlattice. A side elevation of a wire formed by two fingers of a side gated superlattice is shown in fig 1.1b).

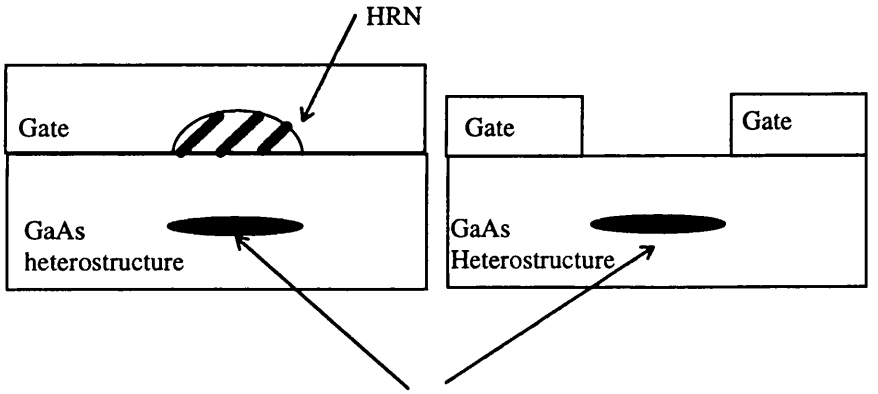

Fig 1.1 a) An electron wire formed by HRN ribs with an overlying gate. A negative voltage applied to the gate depletes electrons from under the areas where the gate is in contact with the surface

Fig 1.1 b) An electron wire formed by two strips of gate metal. A negative voltage applied to the gate depletes electrons from under the gates first, forming the wire

Experiments on electron transport under small period lateral surface superlattices lying completely across the channel were also performed. Magneto-resistance measurements on these devices allow a determination of the magnitude and variation of the potential induced by the gates with gate bias. The potential could be determined using three different features in the magneto-resistance data. These were (i)

commensurability oscillations, (ii) a low field peak which defines the start of the commensurability oscillations and (iii) a quadratically increasing background magneto-resistance. A comparison of the potentials obtained from deep and shallow materials and the attenuation mechanisms present in different barrier materials will be made. An additional motivation of these experiments was to reduce the period of the superlattice to a small enough value to observe new quantum effects. When the magnitude of the Fermi wavelength is equal to half the period of the superlattice, quantum considerations become important and it has been widely predicted that new quantum mechanical structure will be observed. The period of the lateral surface superlattice required for these new effects is of the order of 50 nm which is at the limit of current technology. Using an electron beamwriter it was possible after many attempts to fabricate surface superlattices on devices with a periodic structure of 60 nm. Data from these devices will be presented in this work.

1.2 Thesis outline.

In Chapter 2 fabrication techniques will be explained. The wafers were grown in the Dept. of Electronics and Electrical Engineering in the University of Glasgow. Chapter 2 then explains the different device structures used in the experiments and the fabrication steps used to make the different gate geometries, some of which are at the limits of current technology, will then be discussed.

Chapter 3 will outline the different experimental techniques and apparatus used to make measurements. These involved cooling devices and making magneto-conductance, magneto-capacitance, and orthodox conductance and capacitance measurements in two cooling systems, an Oxford Instruments He^4 cryostat with a variable temperature insert and a CTI Cryogenics closed circuit cryocooler, in the Department of Physics and Astronomy in Glasgow University.

Chapter 4 gives the theory behind the behaviour of the layers used in the experiments. The layers used and the theoretical ideas are common to all the measurements made with the different periodic gate configurations. Chapters 5 and 6 deal with the experiments carried out in this work, Chapter 5 with experiments on longitudinal surface superlattices formed using HRN ribs with an overlying Schottky gate. An alternative design for the formation of longitudinal wires is then presented using side gated fingers. Chapter 6 presents experimental work using small period lateral surface superlattices. The layout of the two experimental chapters is similar. In an introduction, there is some theory specific to the chapter and predictions of what was expected to be observed in the measurements. The following section deals with the types and dimensions of material, gate structure and Hall-bar. The next section contains details of the measurements made and presents the experimental data and results. The last section contains a summary of the results, a discussion and conclusions. Chapter 7 collects the main conclusions of the thesis.

1.3 Review

1.3.1 Introduction

Work in this thesis is a continuation of previous work by R. Cusco [3] on lateral superlattices and by M. Kinsler [1] on longitudinal wires formed by use of negative resist. In her work, Kinsler found evidence of 1D quantisation in one device fabricated on deep material. Cusco showed that the magnitude of the potential which modulates a two dimensional electron gas from a lateral surface superlattice could not be explained by electrostatic perturbation alone, using either the pinned or frozen models. He found that the model that gave a more accurate representation of the magnitude of the potential observed was based on a combination of potential induced by mechanical strain and electrostatics.

1.3.2 Electrons in narrow quantum wires. Experiments of M. Kinsler.

Kinsler set out to measure quantisation in narrow multiple quantum wires on deep heterostructures. The 2DEG (two dimensional electron gas) in these heterostructures was approximately 100 nm from the surface. This material was of very high quality with electron mobilities of greater than 100 $m^2V^{-1}s^{-1}$.

The devices were fabricated in a form similar to field effect transistors but with a periodic array of resist ribs under the gates. A diagram of the form of a device is shown below in fig 1.2.

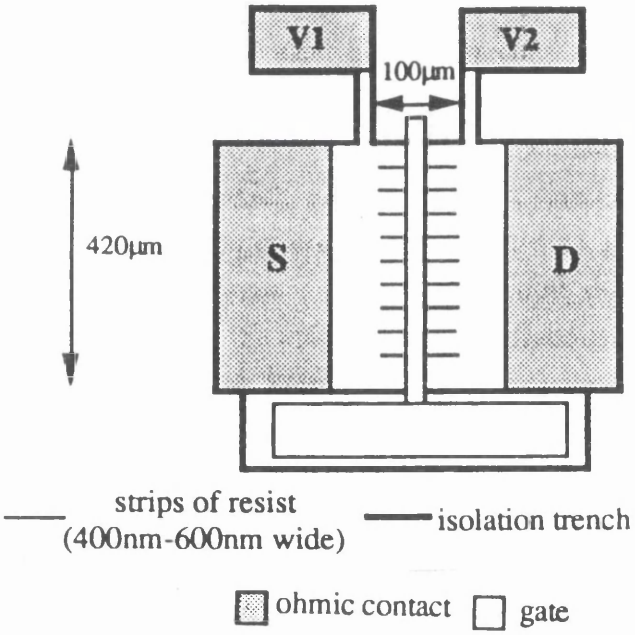

Fig. 1.2. Diagram of the device structure used by M. Kinsler in her experiments on multiple quantum wires.

Resistance, capacitance, magneto-resistance and magneto-capacitance measurements were made on a large number of devices. Only one device showed evidence of one

dimensional quantum confinement in a measurement of magneto-resistance. This is shown below in fig 1.3

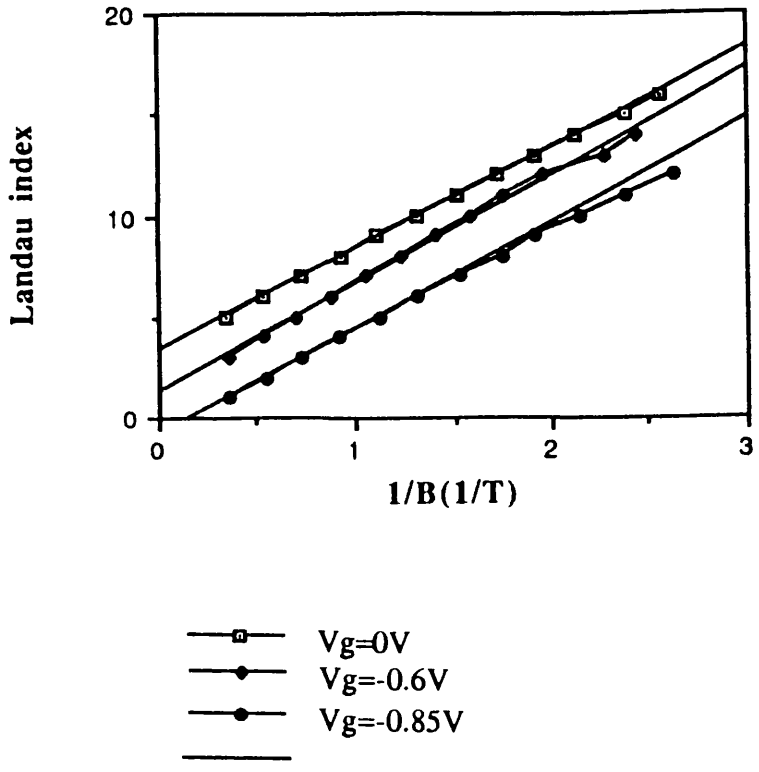

Fig 1.3. M. Kinsler's experiments with longitudinal wire devices showed deviation in the Shubnikov de Haas minima vs. Landau index traces. The sample was A216, bulk doped with an AlGaAs barrier and with the 2DEG 100 nm below the surface.

M. Kinsler also found that that the voltage where the electrons were removed from the areas under the resist (the cut-off voltage) could be best described by a model [2] known as the 'pinned' model. M. Kinsler found that the more physically realistic model known as the 'frozen' model gave poorer agreement. These models are discussed with reference to the present work in section 5.1.3.1.

1.3.2 Potential modulation under lateral surface superlattices. Experiments of R. Cusco. And co-workers [3,4].

R. Cusco et al [3,4] made a systematic analysis of the origin and form of the potential under lateral surface superlattices. He found that the potential is due to a combination of the effects of electrostatics and mechanical strain. R. Cusco then made a study of the dependence of the potential on gate bias, the period and the mark to space ratio of the gate array. The devices used by Cusco et al. were of a shallow type where the electrons were roughly 35 nm from the surface, and a deeper type where the electron gas was roughly 100 nm from the surface. The shallow AlAs barrier devices had a higher mobility than is expected for an electron layer so close to a donor layer. This is due to a layer of electrons round the donors which screen the conducting layer from the full random potential of the donors. The superlattice arrays were prepared using electron beam lithography and measured at low temperatures (of the order of 4.2 K) using standard a.c. lock in techniques. A range of superlattice periods were measured. It was found that the strain model could account for the presence of second harmonics observed in the magneto-resistance measurements, although the agreement with the magnitudes of the perturbation was less good. The variation of potential with gate bias was also studied shown in fig. 1.4 below. Fig 1.4 shows the variation of the perturbing potential with gate bias for four devices.

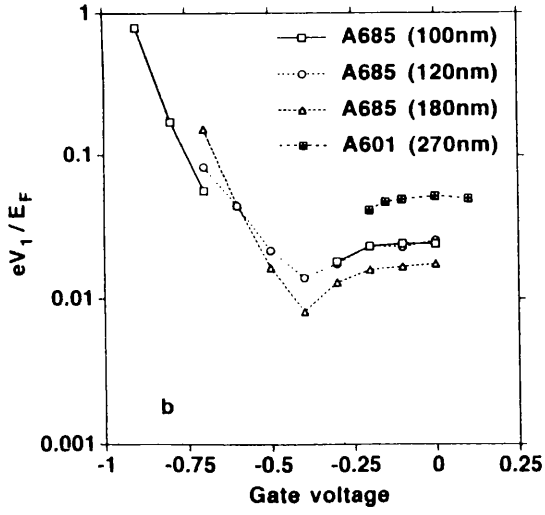

Fig 1.4. Variation of potential with gate bias for four devices measured in Glasgow. The samples used for these experiments were shallow AlAs barrier materials. From [4].

The results show the magnitude of the potential initially decreasing with negative bias then increasing sharply at a bias of around -0.45 V. The sharp increase is attributed to the point where electrons are depleted from a screening layer around the ionised donors, the full electrostatic potential from the gate then acts on the conducting layer. The initial reduction in potential with bias could not be explained by the strain model alone. It was thought an additional attenuation mechanism was responsible for this behaviour.

References

[1] M Kinsler. PhD. Thesis pg. 20, University of Glasgow. 1992.

[2] J.H. Davies. Semicond. Sci. Technol 3, 995, 1988.

[3] R. Cusco, PhD. Thesis, University of Glasgow

[4] R. Cusco, E Skuras, S Vallis, M.C. Holland, A.R. Long, S.P. Beaumont, A.A. Larkin and J.H. Davies. Superlattices and Microstructures 16, 283 1994.

Chapter 2

Fabrication.

2.1 Introduction

In this chapter the facilities required and procedures adopted to fabricate our small gate superlattice structures. The wafers used were grown by molecular beam epitaxy (MBE) and consisted of a series of AlAs, AlGaAs and GaAs layers grown in such a way as to confine a layer of electrons below the surface. This layer of electrons is known as a two dimensional electron gas or 2DEG. Non-rectifying contacts to this layer, known as ohmic contacts, were made and conducting paths between ohmic contacts are defined by etching away unwanted areas of semiconductor.

The devices were fabricated as 'Hall-bars'. Fig 2.1 shows a schematic view of a Hall-bar. The contacts are arranged so that current i is passed through two outer contacts remote from the area of interest and voltage V is measured from a separate pair of contacts situated on either side of the active area. The Hall-bars used were designed with various dimensions. The only critical feature was that the end current contact was at least 3 times the channel width from the nearest voltage contact. Gates were fabricated in the centre of the Hall-bar and connections made from the contacts between the voltage pads.

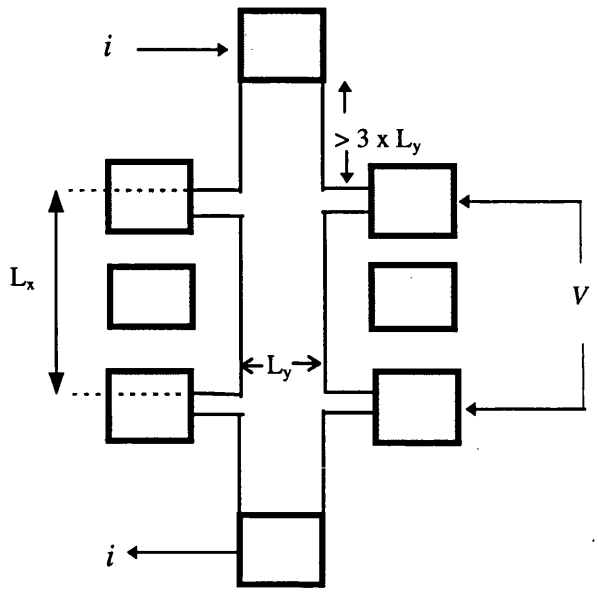

Fig 2.1 Schematic diagram of a Hall-bar

Devices were fabricated using epitaxial techniques. An array of devices was fabricated (typically 6 by 6) to maximise throughput. Patterns were written using an electron beam writer (described in section 2.2.2) which was capable of writing with different spot sizes and resolutions so that both large areas and very small features could be exposed. Positive and negative resists were used to define patterns. The positive resists used were both of PMMA (poly-methyl methacrylate). BDH Chemicals supplied one of 180000 average molecular weight and another called Elv was supplied by DuPont Co. with an average molecular weight of 360000. The chemical composition of one repeat unit of PMMA is shown below in fig 2.2. [1].

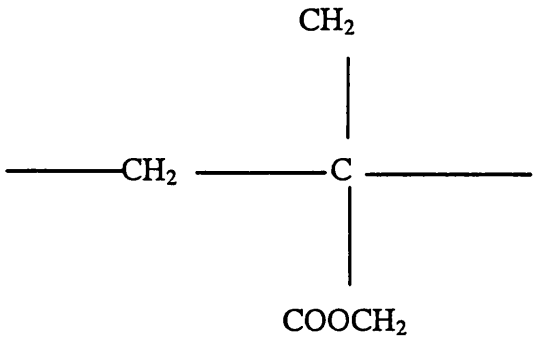

Fig 2.2 The chemical composition of one unit of PMMA.

A positive resist is one in which the area exposed to the electrons is made sensitive to removal. The electrons do this by breaking the long chain polymers into smaller units. The smaller molecules are more susceptible to being dissolved by solvents known as developers. Negative resist acts in the opposite way. Areas exposed to the electron beam remain after development. Positive resists are used in this work to leave areas without resist in defined patterns. If metals are then evaporated onto the sample, they are then in contact with the semiconductor in these defined areas and separated by the resist layers outside. The sample is then exposed to a chemical which attacks and

removes the remaining resist. The result is then that some areas of semiconductor are metallised and other areas are left unmetallised. To do this reliably it is helpful to use bi-layer resist. This method involves spinning and baking on two resist layers, the first a high concentration BDH layer and the second a lower concentration Elv layer. This system has the advantage that after development an overhanging resist profile is obtained because the developer acts faster on the lower molecular weight BDH resist. The overhang profile is desirable as an aid to removal of the unwanted adjacent resist areas in the process known as 'lift-off'. Lift-off is achieved using acetone which attacks the resist via the exposed sidewalls. Bi-layer resist profiles ensure the sidewalls are not covered in metal and hence open to the acetone. The lift-off process is shown schematically below in fig 2.3

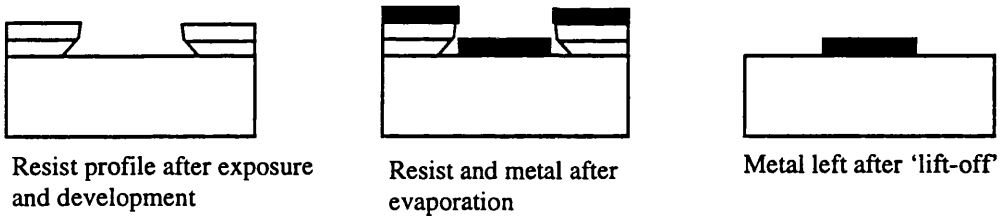

Fig 2.3 Stages of evaporation and 'lift-off'

2.2 Fabrication facilities.

2.2.1 Molecular beam epitaxy.

The substrates used were grown in the University of Glasgow MBE suite in the Department of Electrical and Electronic Engineering. The facility consists of two MBE machines, labelled A and B. Machine A is used exclusively for GaAs/AlGaAs

structures and had produced, prior to 1992, some very high quality material. Machine B is also used so grow other III-V semiconductors such as InGaAs and AlInAs and consequently GaAs/AlGaAs from machine B is generally of less good quality (because some of the indium contaminates the GaAs/AlGaAs samples and causes a high number of impurities). Most of the samples used in this work originated in machine A.

2.2.2 Clean room facilities.

All fabrication facilities were located in the Department of Electrical and Electronic Engineering, University of Glasgow. Fabrication was carried out in a clean room. The clean room contained two clean room cabinets (equipped with a variable speed substrate spinner, an ultrasonic bath and a variable temperature water bath), two ovens and a Plassys automated deposition evaporator. A separate clean room contained a rapid thermal annealer (RTA).

Pattern writing was carried out by a Leica Cambridge Beamwriter EBPG-5 system which could be operated at 50 kV or 100 kV cathode voltage. This cathode voltage accelerates electrons which originate from a tungsten filament heated to 2300-2700°C. The 100 kV facility allowed very fine features to be written because the number of backscattered electrons is minimised giving better resist profiles after development.

Electromagnetic lenses focus the beam to a spot in the sample plane. Too great a variation in height across the sample surface will lead to an unfocussed spot so a laser detection system is used to eliminate this possibility. To use this system it was necessary to include accurate information of the thickness of the sample. This was measured with a digital micrometer on receipt of the wafer.

Other items of equipment used included an ultrasonic bonder, S800 and S900 Hitachi scanning electron microscopes and a D.C. probe station for checking the quality of ohmic contacts.

2.3 Fabrication techniques.

2.3.1 The design of the devices.

Hall-bars and gate structures were designed using a CAD package called Wavemaker. These patterns were translated into a format usable by the electron Beamwriter and combined together with a 'job file'. The pattern file contained details of areas to be written by the beamwriter and the job file contained details of pattern orientation and electron dose.

The devices were designed with orientation marks. These 'alignment marks' are used by the beamwriter to place the pattern with sub micro-metre accuracy in the correct position on each Hall-bar. Initially the alignment marks were written in the same level as the ohmic layer i.e. the ohmic contacts were written at the same time as the alignment marks and so they were processed with each other. A detailed description of device design using the hierarchical cell structure of Wavemaker can be found in the handbook [2]. However, fabricating ohmic contacts and alignment marks at the same time proved to be disadvantageous, as it limited the maximum annealing temperature (because the ohmic layer became lumpy after annealing, leading to poor alignment). In the later devices, the alignment marks were evaporated separately using metals not sensitive to the annealing process. It is this later, more successful process which is described below.

2.3.2 Device preparation.

2.3.2.1 Substrate cleaning.

On receipt from the MBE grower, the substrate was cleaved using a diamond scribe into pieces approximately 10 mm x 10 mm for ease of handling. The samples were

cleaned in preparation for deposition of an ohmic layer. The following chemicals and procedures were used:

2 minutes ultrasonic agitation in trichloroethylene or optoclear
2 minutes ultrasonic agitation in methanol
2 minutes ultrasonic agitation in acetone
30 s rinse in isopropylalcohol, then blow dry with nitrogen.

Initially trichloroethylene was used, but latterly a switch was made to 'optoclear' (a commercial degreaser/cleaner) when trichloroethylene was banned as an ozone depletant.

2.3.2.2 Ohmic layer.

After cleaning, the sample was immediately coated with 15 percent solution of BDH (in chlorobenzene), spun at 5000 revs/min for 1 minute, baked for one hour at 180°C, coated with 4 percent Elv solution (in xylene), spun at 5000 revs/min for 1 minute and baked overnight at 180°C.

The sample was then submitted to a beamwriter technician with an instruction sheet for writing. This enabled the beamwriter operator to clamp and mount the sample in the beamwriter with the correct orientation. The samples were written by electrons accelerated by 50 kV with an exposure dose of 300 $\mu C/cm^2$ and a spot size of 400 nm. After writing, the samples were processed as soon as possible. Firstly they were developed with 1:1 IPA:MiBK [isopropyl alcohol:methyl isobutyl ketone] for 60 s at 23°C. This removed the resist on the areas of the sample which were to be coated with the metals that comprise the ohmic contacts. The sample was then deoxidised using roughly a 1:4 mixture of hydrochloric acid and de-ionised water immediately prior to being placed in the evaporator. The following metal films were then evaporated onto

the sample: 8 nm Ni
120 nm Ge
130 nm Au
80 nm Ni
250 nm Au

The thin Ni layer allowed the Ge to adhere to the surface of the GaAs. The purpose of the Ge layer was to form a contact with the 2DEG. This was done by annealing at temperatures up to 400°C which diffused the Ge into the wafer, forming an alloy with the GaAs and a contact between the 2DEG and the thick Au surface pad [3]. The purpose of the intermediate Ni layer was to form a eutectic alloy which improves the properties of the Au pad. The sample now comprised areas of ohmic contacts where the metal was in contact with the surface of the sample, and other areas where the metal was separated by a layer of resist. Lift-off was carried out in warm acetone at 45°C by placing the sample in a beaker of acetone, which was itself placed in a water bath. This method was found to give the quickest lift-off leaving the required areas coated with the metals.

Fig 2.4 shows areas defined for the four patterns used in this thesis. Pattern A was a pattern designed by Chris Barton, a previous PhD student, and pattern D was designed by Dr. Elef Skuras (a post doctoral research assistant) in the Physics Department. Patterns B and C were designed by the author. The patterns are not all drawn to the same scale.

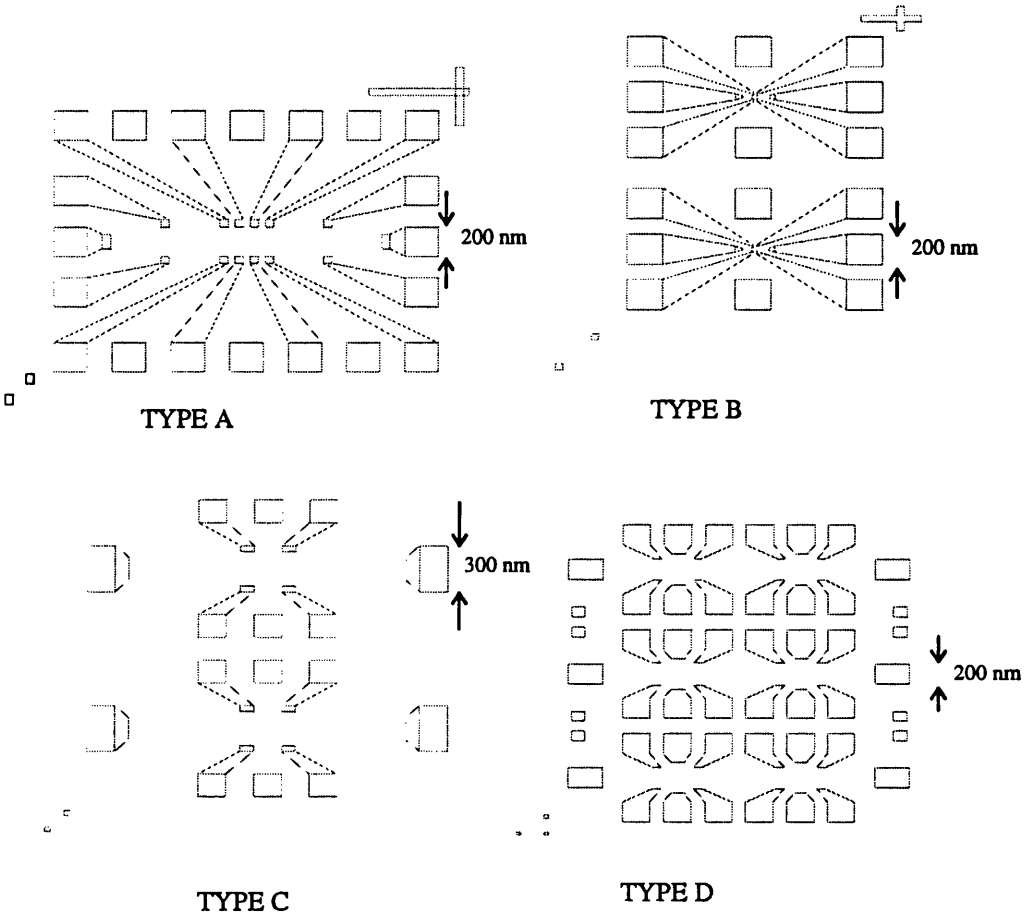

Fig 2.4 Ohmic level patterns

2.3.2.3 Alignment marks.

In the bottom left hand corner of the patterns in fig 2.4 there can be seen some small square markers (the dimensions are either 40 μm square or 30 μm square). These were used to align the next level which was the alignment layer. The resist layers used in this process were the same combinations as for the ohmic layer. This layer was written using an 80 nm spot with an exposure dose of 300 $\mu C/cm^2$. Evaporation and lift-off were carried out in a similar way to the ohmic layer, with the metals being 30 nm

NiCr and 150 nm Au. Annealing could then be carried out. This was done on the RTA. After many attempts, it was found that the optimum recipe for this process was the temperature and annealing time that gave the ohmic contacts a lumpy and cracked look under a microscope. This was normally a temperature of 390°C for 60 s. The ohmic alignment marks were then unusable for the next layer but the separately deposited alignment marks were still smooth and gave good alignment.

After completion of the alignment level, the samples were checked on the D.C. probestation using a two probe measurement. A good sample had a DC measurement of the order of typically 300 Ω - 1 kΩ resistance dependent on the distance between the gold pads probed.

2.3.2.4 Isolation.

This process defines the channel and isolates gate connections from ohmic contacts. The resist combinations were the same as that used for the ohmic layer. The patterns were written with a 400 nm spot with 300 $\mu C/cm^2$ exposure dose. After development an ammonia based etch was used to dig trenches in the material which provide the isolation. The composition of the etch was 200 parts water/4 parts ammonia (67% ammonia solution in water)/1.5 parts hydrogen peroxide (35% hydrogen peroxide solution in water). This gives an etch rate of 100 nm per minute and so for the deeper material the etch time was 1 minute and for the shallower material 30 s was used. Fig 2.5 shows the isolation patterns used for Hall-bars A-D (as defined in fig 2.4). L_x and L_y are as defined in fig 2.1. The patterns are not drawn to the same scale (as each other or as those in fig 2.4). Pattern A is shown with a 100 μm channel width, although some Hall-bars were made with the channel width L_y reduced in the gate region to 20 μm for particular longitudinal wire and superlattice experiments. At the end of this stage the samples were again measured on the DC probestation to check the ohmic contacts. For a good device, the resistance would have increased to about

20 Ω - 30 kΩ at this stage and a straight line would be observed on the I-V curve, indicating an ohmic response to the measurement.

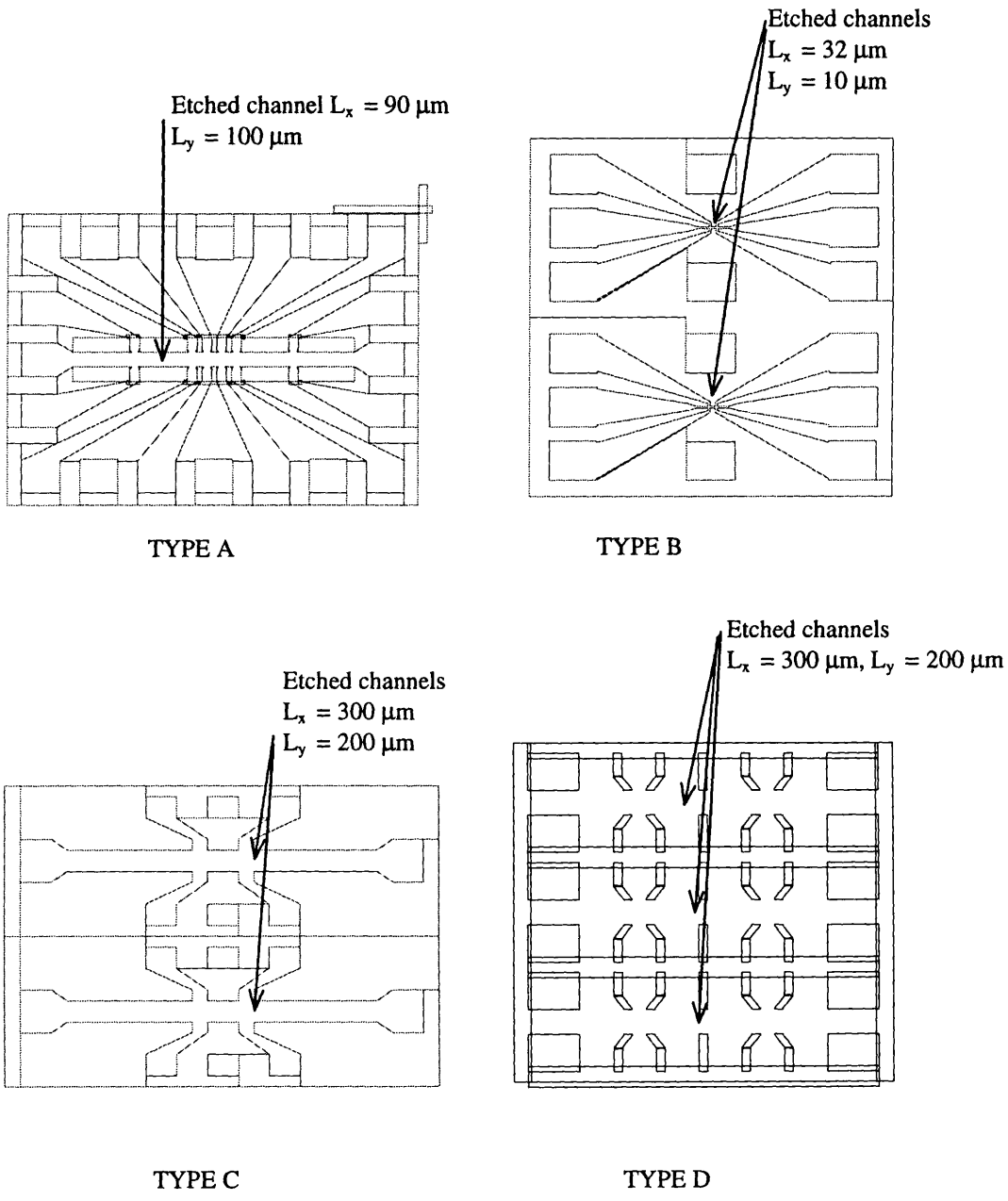

Fig 2.5 Isolation Layers

2.3.2.5 Gated areas and connections.

2.3.2.5a) Longitudinal wires

These were written using negative resist. The negative resist was a type known as HRN (high resolution negative resist) diluted in chlorobenzene to 4 percent. The sample was spun at 5000 rpm for one minute and baked overnight at 120°C. The resist was then exposed to electrons accelerated through 100 kV, to minimise backscattering and with an exposure dose of 500 $\mu C/cm^2$ and a 12 nm spot size. Development was with a 1:1 mixture of IPA and MiBK for 20 s at 23°C followed by a 20 s rinse in IPA, repeated twice and followed by blowing dry with nitrogen. This procedure gives optimum wire profiles [4] (optimum meaning that maximum resist is cleared from unexposed areas). After exposure to an electron beam, HRN is not affected by acetone, so the overlying gates and connections could be fabricated using an acetone lift-off without destroying the wires. The gates and connections were fabricated using the same procedure as the ohmic contacts but with a gate metal of 12 nm Ti and 15 nm Au.

2.3.2.5b) Small period Superlattices.

These were written using positive resist. This resist was a lot thinner than that previously used, comprising 2.5 percent BDH and 2.5 percent ELV each spun on at 5000 rpm, with a one hour bake at 180°C between layers followed by an overnight bake. Resist thickness here is important. Figs 2.6 (a)-(c) show schematically the results after lift-off for different thicknesses of resist.

If the resist is thinner than the evaporated metal, then there will not be enough clearance after development to allow the acetone to lift-off adjacent strips of metal. This is shown schematically in fig 2.6 (a). If the resist is too thick then when the development process takes place the sidewalls of adjacent strips will also be developed, collapsing the resist strips. After evaporation and attempted lift-off, this situation is characterised by areas comprising a few superlattice periods of solid metal

and other areas with no metal as shown in fig 2.6 (b). The desired effect is shown in fig 2.6 (c) with only uniform strips of metal remaining after lift-off.

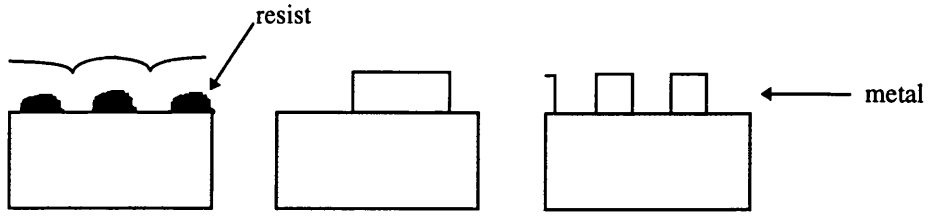

Fig 2.6 (a) Fig. 2.6 (b) Fig 2.6 (c)

Fig. 2.6 Results of attempted lift-off with various resist thickness
a) resist too thin, b) resist too thick, c) ideal lift-off.

To obtain the optimum metal profile, many exposure tests were made on bulk material. The optimum exposure dose and development time were determined by fabricating a series of superlattices, each with the exposure dose increased by a known amount. The small period strips were written using 100 kV to ensure maximum resolution. Extremely high exposure doses, of the order of 4500 $\mu C/cm^2$ with a spot size of 12 nm were used to write the wires. Development was with 4:1 IPA:MiBK for 25 s. The gate metal was 20 nm NiCr. Connections to the superlattice were made using the method for the ohmic contacts (above), but with gate metal of 12 nm Ti and 15 nm Au. These connections were normally made outside the channel but for the deeper material it was necessary to bring the connections onto the channel (as is shown in Chapter 6, Fig 6.2) because of breakages when the narrow strips of metal climb onto the channel up an etched height of 100 nm.

2.3.2.4c) Large period superlattices and finger superlattices.

These were written using positive resist. The resist comprised 4 percent BDH and 4 percent ELV each spun at 5000 rpm, with a one hour bake at 180°C between layers followed by an overnight bake at 180°C for both layers. The samples were written with an exposure dose of 600 $\mu C/cm^2$ with an 80 nm spot using electrons accelerated

through 50 kV. Development was with a 4:1 mixture of IPA:MiBK for 20 s. The evaporated gate metal was 50 nm of NiCr. Side connections were made to the lattices with the same recipe as for the small period superlattices.

2.4 Preparation of samples for measurement.

During the steps in this section an earthing bracelet was worn to prevent electrostatic damage to the devices.

2.4.1. Scribing and mounting of samples on 18 pin packages.

The samples in the array typically had a 0.5 mm gap between them to allow the devices to be separated. This was done using a diamond scribe. The individual samples could then be mounted using a contact adhesive on an 18 pin package. The package and sample are shown schematically below in fig 2.7. Also shown are the gold wires used to connect the package to the sample. These were 40 μm diameter and were bonded using the ultrasonic bonder.

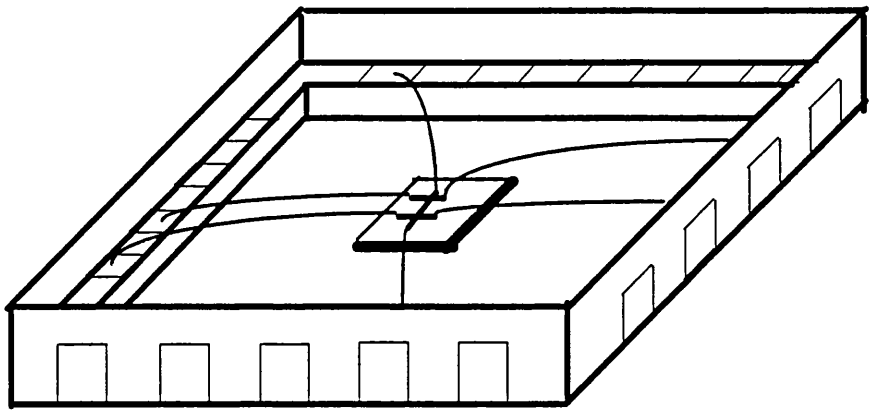

Fig 2.7. Package and sample showing wire bond connections

2.4.2 Connection to measurement equipment.

The package could now be mounted on the measurement rod. The three measurement systems used all a had permanent sample holder onto which the package could be mounted without soldering. This consisted of a recess the same shape as a package with a number of gold plated sprung copper pins. A thumb-screw and polythene plate pushes the package onto the pins, making the connections.

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Chapter 3

Experimental techniques

3.1 Introduction.

This chapter will discuss the experimental apparatus employed to measure the devices whose fabrication was described in chapter 2. The reasons for cooling samples are briefly discussed and the two cooling systems which were used, situated in the Department of Physics and Astronomy, will be described. Transport and capacitance measurement techniques will be outlined.

3.1.1 Transport measurements.

Heterostructures are designed specifically to reduce scattering from ionised dopant impurities by separating the conducting channel from the donors with a spacer. The dominant scattering mechanism then limiting the mobility at high temperatures is from inelastic collisions with phonons or lattice vibrations [1]. At low temperatures the energy available to generate phonons, k_BT, is reduced. This is too small for optical phonon emission [2] and also reduces acoustic phonon scattering. The dominant scattering mechanism is then from ionised donors in the remote doping plane or from interface roughness if the lattice matching is poor, or in a poor material from residual impurities in the channel. The cryogenic equipment used was equipped with a superconducting magnet which enabled magneto-resistance measurements to be carried out.

3.1.2 Capacitance measurements.

Shallow and deep AlGaAs barrier materials are designed with the doping layer remote from the conducting channel. At low temperatures charge in the donor layer is trapped in the ground states of isolated substitutional donors, in distorted configurations known as DX centres. A measurement of capacitance between the channel and a surface gate as a function of gate voltage should be a measurement of the amount of

charge in the conducting layer. Capacitance measurements were carried out on deep and shallow AlGaAs barrier materials at low temperatures, for longitudinal and finger superlattice samples. Measurements of the capacitance were also carried out where the sample was subject to a perpendicular magnetic field linearly varying with time (magneto-capacitance measurements).

3.2 Cryogenic equipment.

3.2.1 Oxford Instruments cryostat with Variable Temperature Insert.

Transport measurements were made at 1.5 K or 4.2 K and capacitance measurements were carried out at 1.5 K using an Oxford Instruments cryostat situated inside an electrostatically screened room. The cryostat could be used with a dilution refrigerator insert or with a variable temperature gas flow insert (VTI). The VTI was the one used for measurements in this thesis. Fig 3.1 [3] is a schematic diagram of the insert showing the position of the VTI rod.

A continuous flow of He^4 is supplied to the sample space via a needle valve. To obtain a temperature of 4.2 K the needle valve is opened fully, the sample space pumping line is closed and the sample space is vented to the helium return line which allows the sample space to fill with liquid helium. This temperature could be further reduced to 1.5 K by opening the pumping port and reducing the pressure above the helium. The sample space temperature was monitored using a calibrated Rh-Fe resistor in thermal contact with the sample. There was also a heating unit on the capillary inlet to allow access to a stabilised temperature in the region of 1.2 K to 100 K, but this facility was not required for these measurements.

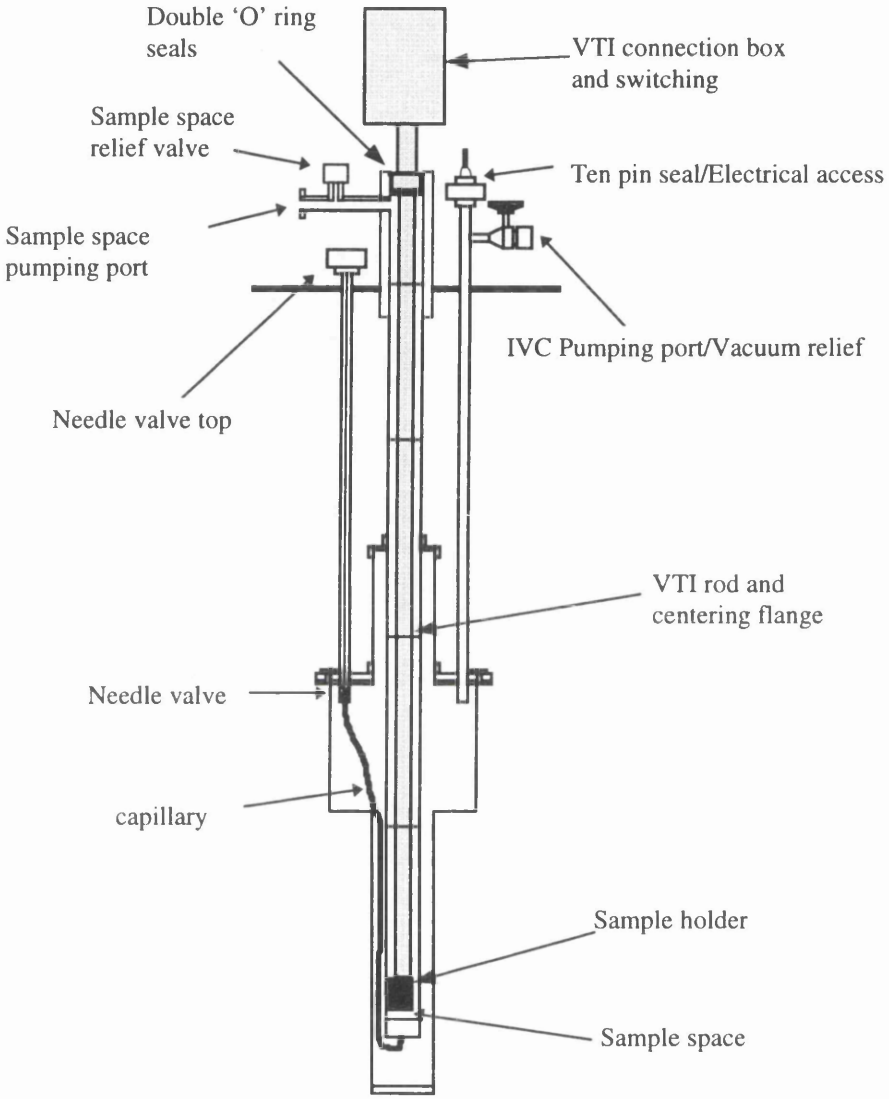

Fig 3.1 Schematic diagram of a VTI rod and insert

The cryostat had a superconducting magnet sitting in a bath of He^4 in its base. This was controlled, via a RS232 connection, by a remote Oxford Instruments 120A, 10V power supply unit PS120-10 situated outside the screened room. The magnet was used to generate fields up to 12.7 T in the sample space. The magnetic field was swept linearly at a rate of around 0.01 T/minute for low field measurements and up to 0.3 T/minute for fields to 12.7 T.

For resistance and magneto-resistance measurements, the samples were mounted on the VTI rod with 14 connections to a spring loaded connector. On the box at the top of the rod, 14 switches connected the sample wires either to an earth position or direct to a connecting socket. This allowed the gates to be connected to earth to protect them from high transient voltages during switching of equipment. A short length of cable connected the socket to the pre-amplifiers used for resistance measurements. These were situated next to the cryostat inside the screened room.

For capacitance measurements, a different VTI rod was used. This had 5 coaxial leads running from the top connector box to the spring loaded sample connectors. The top connector box has five small coax type connectors (known as SMB connectors) which were connected to a Hewlett-Packard HP4274 multi frequency LCR meter. The HP4274 was situated near the cryostat inside the screened room.

Illumination can be used to free electrons trapped in the donor layer. This technique results in an increase in the carrier concentration in the conduction layer. Both VTI rods were fitted with an LED to illuminate the sample. Initially the LED was situated on the end of the VTI next to the sample. Later this arrangement was changed because of difficulty in operating the LED at low temperatures. The LED was mounted close to the top of the sample rod and light was transmitted to the sample via an optical fibre. Illumination with either system never proved to be advantageous for the samples measured. The data presented in this thesis were taken after cooling in the dark, and without any pre-illumination.

3.2.2 Closed circuit system.

A CTI Cryogenics Model 21 cryocooler was used to cool samples to temperatures between room temperature and 20K. Cooling was achieved by expansion of helium gas through two cold stations situated in a cold head. A two stage rotary pump was used to pump out the sample space. A pressure of less than 0.05 torr was obtained in the sample space before cooling was started.

A diagram of the cooler arrangement is shown below in fig 3.2. [4].

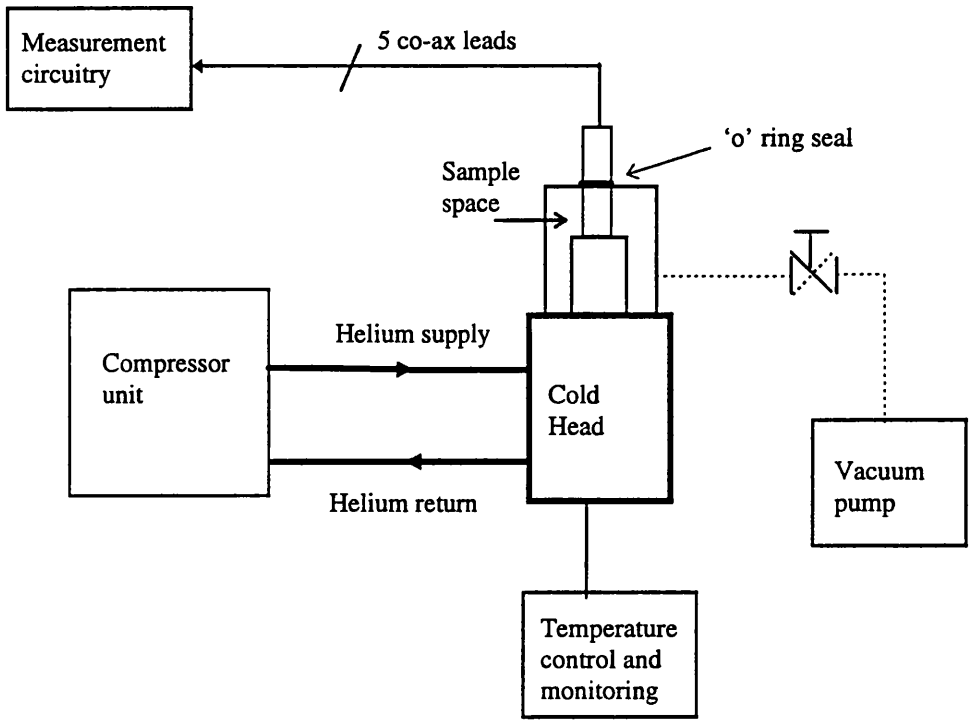

Fig 3.2 Schematic diagram of the closed circuit system

It was possible to measure the temperature of the sample using a Si diode in thermal contact with the sample. The temperature could be stabilised at any value between 20K and room temperature using a differential amplifier which monitored voltages from the diode and a pre-set supply, and fed back power to a heater until the difference in the voltage values was zero. In practice however the equipment was usually operated at the lowest possible temperature, which was at or slightly below 20K.

3.3 Measurement equipment

3.3.1 Resistance and magneto-resistance measurement equipment.

Measurements were carried out using very low currents and voltages to avoid the generation of hot electrons due to high electric fields. The use of Phase Sensitive Detection (PSD) enables low excitation signals to be used with a very good signal to noise ratio. The PSD equipment used was two EG&G PARC 5210 PSDs connected to the sample via a connection circuit and two EG&G PARC model 113 pre-amplifiers. The cryostat, pre-amplifiers and measurement circuit were enclosed in a screened room. Connections to and from the screened room passed through filters in the screened room wall to minimise coupling of unwanted r.f. radiation to and from the sample via the measurement leads. The resulting system is shown below in fig 3.3. This is an overall view of the measurement system, a detailed view is shown in Fig 3.4. The letters a, b, c, d, e, f, and g correspond to points on fig 3.4.

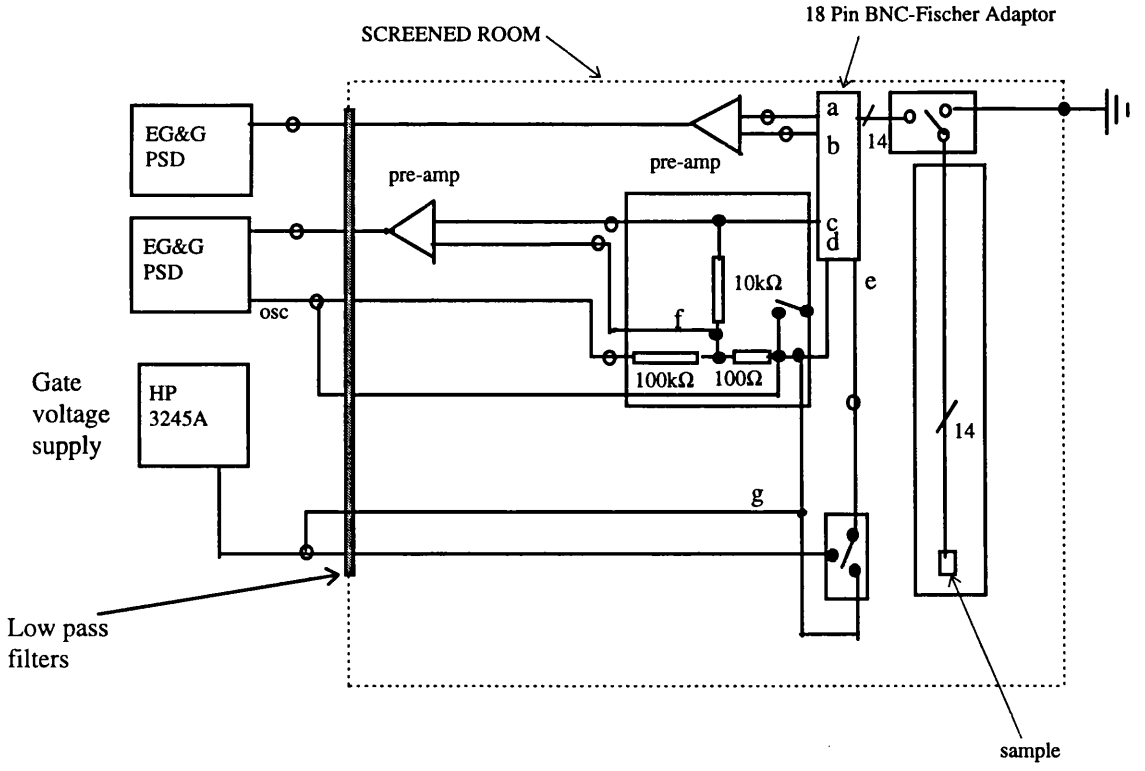

Fig 3.3 Screened room and measurement circuitry

Also shown in fig 3.3 is the gate bias circuit which consisted of a Hewlett-Packard 3245A universal voltage source. The magnet, PSDs, and voltage source were controlled via an IEEE488 bus from a computer. The measurement programmes for the computer were written as Turbo-Pascal routines by Dr. Elef Skuras and others. For transport measurements, a sinusoidal excitation signal at a frequency of approximately 18Hz was used, drawn from the internal oscillator of one of the PSDs. The excitation signal was reduced from 200 - 600 mV by a factor of about 1000 in the measurement circuit and then fed to the sample via a 10 kΩ high stability resistor. The measurement circuits on the PSDs monitor voltages from the circuits a) across the 10 kΩ resistor, which is effectively the current through the sample, and b) across two voltage terminals, which is the voltage in the required measurement area. This four terminal technique eliminates the effect of contact resistances to the sample.
This is shown schematically below in fig 3.4.

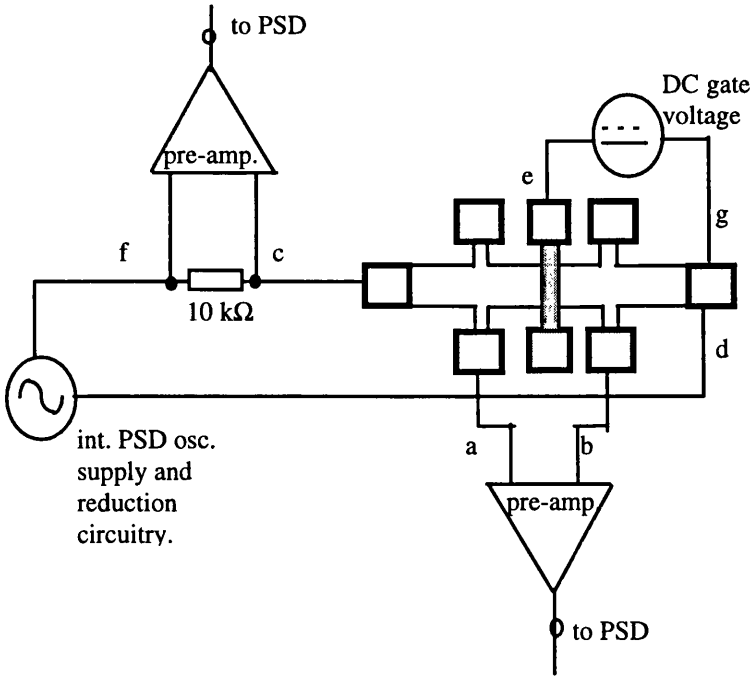

Fig 3.4 Four terminal measurement circuit.

The PSDs measure the oscillator signal in a narrow band around a pre-set reference frequency. The signal is amplified and applied to a phase sensitive detector operated at the reference frequency. The phase sensitive detector gives a time dependent response to frequencies different from the reference frequency and a d.c. output at the reference frequency. The unwanted a.c. components are attenuated by an internal low pass filter [5]. The computer monitors the values from the PSDs as a function of gate bias or magnetic field and stores the values as resistance and voltage or magnetic field in turbo Pascal (binary) format. These files were converted from Turbo-Pascal to ASCII format using a programme written by Mr B. Burns and were then plotted using an 'off the shelf' plotting programme called Easy-plot.

3.3.2 Capacitance measurements

Capacitance measurements were carried out using a Hewlett Packard 4274A Multi-frequency LCR meter. The measurement was a two terminal one with the 'high current' and 'high voltage' connected together and then via coax and BNC connectors to the gate of the sample. The 'low current' and 'low voltage' leads were connected together and then to as many of the ohmic contacts as was possible. In practice, because of the limited number of coax leads available (five on both the VTI and closed circuit systems) and because more than one device or gate was mounted on the 18 pin holders, there were normally two gate connections and three ohmic contacts available. Ohmic contacts were normally selected to be on either side of the gate (to minimise series resistance in the channel) and extra gates of devices not being measured were connected to the measurement low of the circuit. This is to eliminate errors in the capacitance measurements because the additional leads would otherwise draw current which is not measured at the input of the capacitance meter.

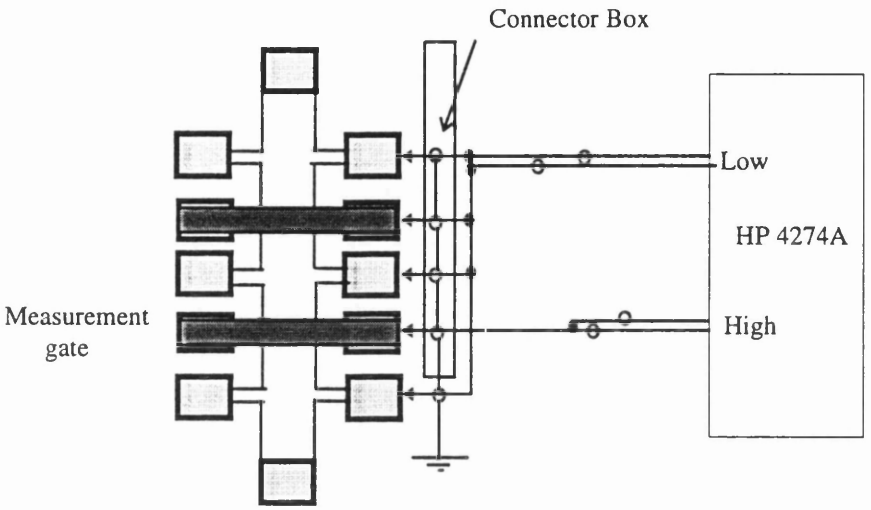

Fig 3.5 Diagram of measurement arrangement for capacitance and magneto-capacitance measurements

The coax outers were connected together and to earth in the connection box. The HP 4274A was computer controlled via an IEEE488 bus using Turbo-Pascal programmes. One measurement program allowed capacitance to be recorded as a function of d.c. voltage applied to the device, and a second recorded capacitance as a function of magnetic field. The measurement programmes also allowed measurement parameters to be entered such as oscillator frequency (usually set at 100kHz), oscillator voltage level, time between measurements, number of averages and gate bias levels. The capacitance meter measures the AC response to an applied sinusoidal measurement voltage. Two parameters are generated depending on the circuit mode selected. Any sample can be approximated by either a resistor in series with a capacitor or a conductor in parallel with a capacitor. The series mode should be used for low impedance samples and the parallel circuit for high impedance samples. The circuit mode used in all our measurements was the parallel one and hence the parameters measured were parallel conductance and capacitance. If the inappropriate measurement system was chosen, e.g. in a device where the main components of loss were in the series connections or 2DEG, the data could be converted to series form using conversion equations given in the operating manual [6]. The conversion

equations used are shown below for conversion of parallel conductance (G_P) to series resistance (R_S), and for parallel capacitance (C_P) to series capacitance (C_S) . This is shown below in fig 3.6.

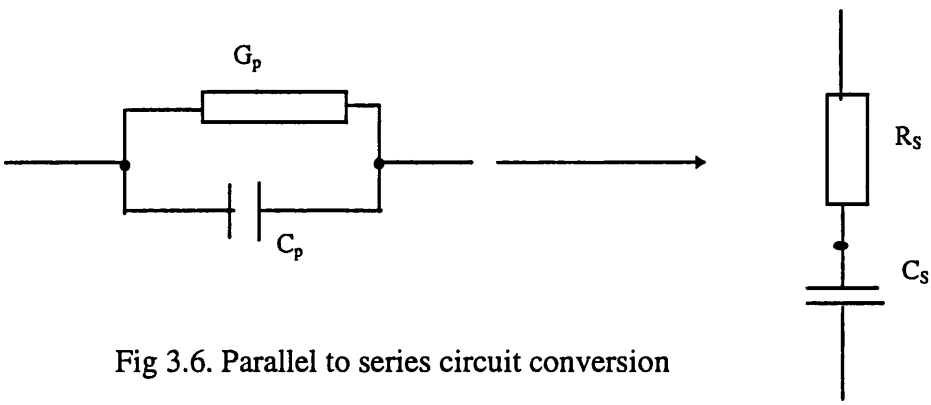

Fig 3.6. Parallel to series circuit conversion

$$C_S = (G_p^2 + \omega^2 C_p^2)/\omega^2 C_p \qquad (3.1)$$

$$R_S = G_p/(G_p^2 + \omega^2 C_p^2) \qquad (3.2)$$

Here ω is $2\pi f$ where f is the measurement frequency. To measure capacitance as a function of gate bias, the AC measurement signal is superimposed on a DC bias voltage, which was also generated by the capacitance meter

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Chapter 4

General theory of III-V semiconductor materials and heterostructures.

4.1 Crystal structure and doping.

In conventional semiconductor devices the transport of electrons through the device is impeded by ionised impurities which are introduced to give an artificially higher concentration (as compared to an intrinsic or undoped semiconductor where electron concentration is independent of the number of impurities) of electrons (for n type devices). These impurities act as scattering centres, decreasing the mobility. To reduce this effect, structures are used where the doping layer is separated from the conducting channel. This process is called modulation doping and is the basis of the modulation doped field effect transistor (MODFET). These devices can be made with gallium arsenide (GaAs) and aluminium gallium arsenide ($Al_xGa_{1-x}As$ where x denotes the aluminium fraction) layers to take advantage of the low effective mass ($m^* = 0.067m_e$) of an electron in GaAs.

GaAs and AlGaAs can be lattice matched, which eliminates the effect of scattering due to trapped charge and interface strain, such as that found at the interface between the semiconductor and the SiO_2 insulating layer in a metal oxide semiconductor field effect transistor. The crystal structure of GaAs is shown below in Fig. 4.1 [1] and consists of two interpenetrating face centred cubic sublattices, alternately Ga and As, displaced by a quarter of the distance along the diagonal of the cube.

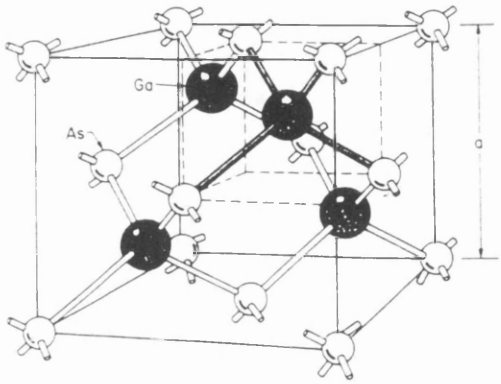

Fig 4.1 The structure of a GaAs crystal

An $Al_xGa_{1-x}As$ crystal structure is similar to the GaAs structure but with some of the gallium atoms replaced at random by aluminium. In MODFETS, doping is introduced by depositing silicon into an $Al_xGa_{1-x}As$ layer. Silicon is an amphoteric dopant which acts as a donor in low concentrations. The silicon atoms sit substitutionally on gallium sites in the lattice. The extra electron has an ionisation energy of 7meV if a simple hydrogenic model is used for the binding energy. However, it is widely accepted that the Si dopants do not behave in this way and instead have an ionisation energy of around 150meV in $Al_{0.3}Ga_{0.7}As$. These donor centres are known as 'DX' centres. DX centres are widely believed [2,3] to be ground states of isolated substitutional donors in a distorted lattice configuration, which can be stabilised by trapping two electrons. The lattice distortion comes about if a Si bond is broken and the Si moves to an interstitial site near three As atoms. Four different DX levels have been resolved in Si doped $Al_x Ga_{1-x} As$, whereas there is only a single DX level in GaAs. This suggests that in $Al_x Ga_{1-x} As$, the energies of the DX centres are dependent on the number of Al atoms near the Si donor. The trapping of electrons is also strongly temperature dependent. At low temperatures, the most important feature of the DX centre is that there is a barrier to charge moving in or out of the centre. The result is that charge is trapped in the centres below about 150K and there is a barrier to charge entering the DX centre below 50K. It is however always possible to excite electrons out of DX centres by illuminating the sample.

4.2 Band structure of GaAs and the formation of the 2DEG.

The crystal is a three dimensional periodic array of atoms. Each atom has a potential, and this periodic potential gives rise to energy bands in the energy spectrum, of which the most important for us are the conduction band and the valence band. These bands are separated by a region of the energy spectrum which designates energies that the electrons in the solid cannot possess. This region is known as the band gap and has a (minimum) energy difference of E_g.

Fig. 4.2(a) shows a simplified schematic diagram of n-doped $Al_xGa_{1-x}As$ and undoped GaAs bandstructures. In reality there are 4 valence and 4 conduction bands which have a complex shape. The shape varies with position inside the Brilloun zone, labelled by the crystal momentum *k*. A GaAs crystal has a conduction band minimum and valence band maximum at k=0.

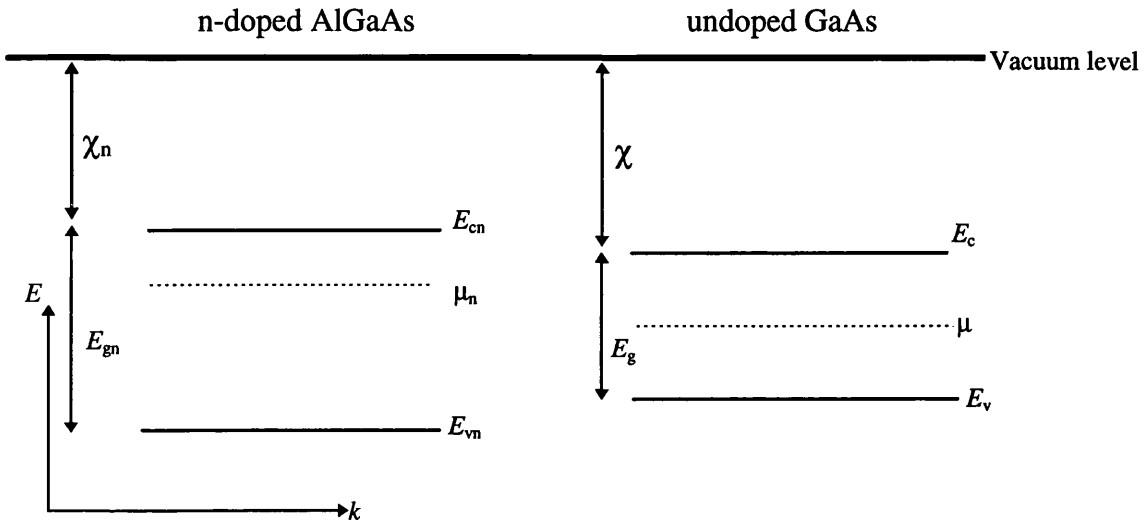

Fig 4.2(a) The energy bands of n-doped AlGaAs and undoped GaAs showing the position of the chemical potentials μ_n and μ.

In fig 4.2(a) E_{cn} and E_{vn} are the conduction and valence band edges in the $Al_xGa_{1-x}As$ layers. E_c and E_v are the conduction and valence band edges in the GaAs layers. μ_n and μ are the chemical potentials in the $Al_xGa_{1-x}As$ and GaAs layers. The chemical potentials are set by the doping level, χ_n and χ are the electron affinities in the $Al_xGa_{1-x}As$ and GaAs layers.

When the two semiconductors are joined together, an empirical model known as the Anderson model [4] can be used to analyse the electron energy bands at the junction between the two materials. The basis of this model is that the conduction band discontinuity is ΔE_c.

$$\Delta E_c = \chi_n - \chi \qquad (4.1)$$

The valence band discontinuity is ΔE_v.

$$\Delta E_v = E_{gn} - E_g - \Delta E_c \qquad (4.2)$$

With no bias applied the chemical potential is constant through the device. A schematic diagram of the resultant band structure is shown in Fig. 4.2(b)

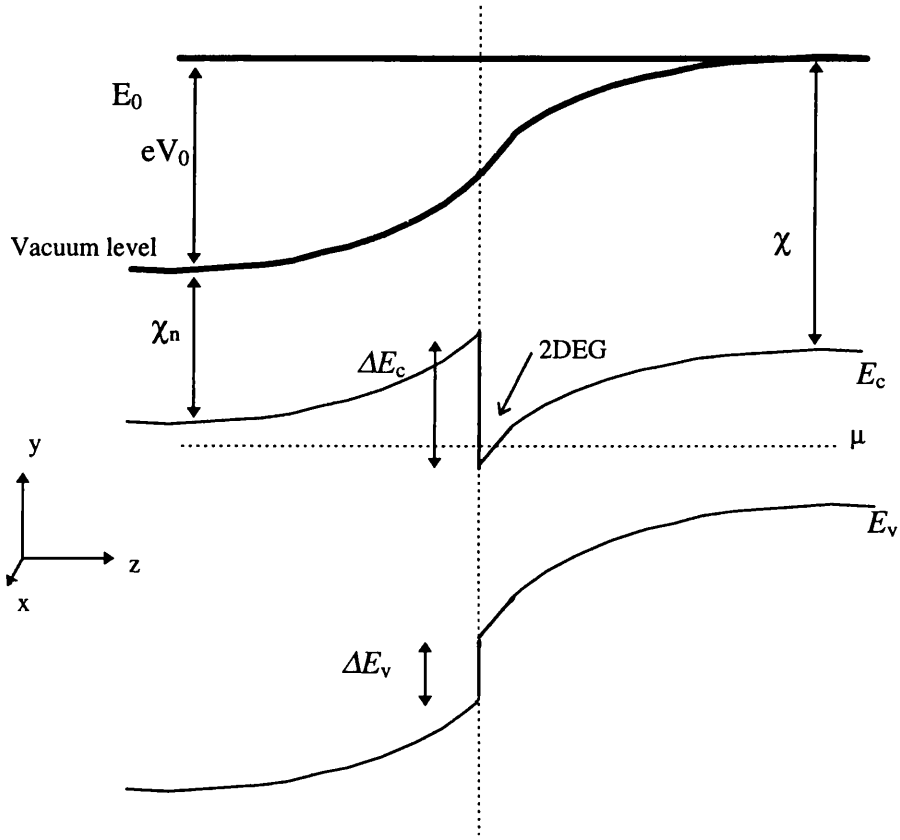

Fig. 4.2(b) Conduction band diagram of joined undoped GaAs and n-doped AlGaAs crystals

The Anderson model shows that joining the materials together results in the formation of a built-in potential eV_0 across the junction and that the band offset in the conduction band between the n-doped $Al_xGa_{1-x}As$ and the undoped GaAs forms a potential step. Electrons separated from the donors form a two dimensional electron gas at the interface in a roughly triangular potential well of a width of a few nanometres. Energy levels in this well are quantised. They are restricted by the potential in the z direction

(perpendicular to the interface) but are free to move parallel to the interface in the x and y directions. To find the energy levels in this well, the time independent Schrödinger wave equation (SWE) must be solved.

$$[-\hbar^2/2m^*(\nabla^2)+ V(z)]\Psi(x,y,z) = E\Psi(x,y,z) \quad (4.3)$$

The wavefunction $\Psi(r)$ is made up of plane wave components in x and y and some function dependent on z .

$$\Psi(r) = \exp(ik_x x)\exp(ik_y y)u(z) \quad (4.4)$$

substituting 4.4 into 4.3 cancelling exponential terms and defining

$$\varepsilon = E - [(\hbar^2 k_x^2/2m^*) + (\hbar^2 k_y^2/2m^*)] \quad (4.5)$$

reduces 4.3 to

$$[-\hbar^2/2m^*(\partial^2/\partial z^2) + V(z)]u(z) = \varepsilon u(z) \quad (4.6)$$

This is a SWE in one dimension. To solve this the potential that the electrons move in, $V(z)$ must be found. There are two contributions, the electrostatic potential $\phi(z)$, and the band offsets. $\phi(z)$ is found from Poisson's equation,

$$\partial^2\phi(z)/\partial z^2 = -\rho(z)/\varepsilon_r\varepsilon_o \quad (4.7)$$

where ε_r and ε_o are the permittivity of the material and free space respectively and $\rho(z)$ is the charge density which is itself made up of two components, the charge density from any external potential from impurities plus any gate bias applied and the charge density of other electrons. With no gate bias, and assuming the GaAs to be impurity free, this leaves the charge, from all other electrons, on a given electron j

$$\rho(z) = -e\Sigma_k |u(z)|^2 \quad (k\neq j) \quad (4.8)$$

which must be summed over all other electrons. This $\rho(z)$ is dependent on $u(z)$. The wavefunction $u(z)$ is required to find $V(z)$ and to solve Schrödinger's equation $V(z)$ must be found. So Poisson's and Schrödinger's equations must be solved self consistently. This can be done analytically by approximating the potential as a triangular potential well as in Fig. 4.3, or numerically for the most accurate results [16].

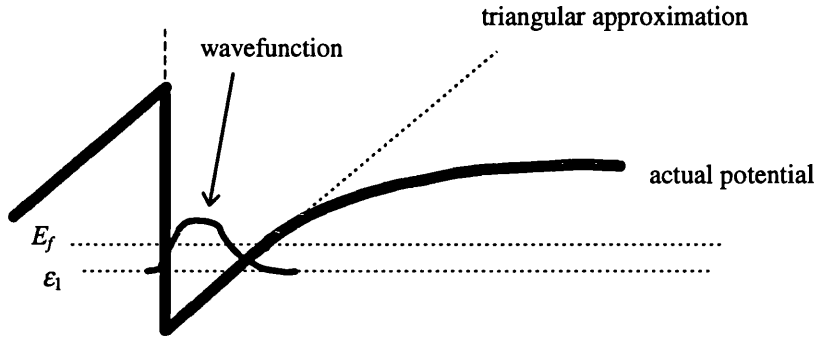

Fig. 4.3 Approximation of the potential well as a triangular potential.

In fig 4.3 the potential in the region of the interface is approximated by a triangular potential well shown with one energy level occupied. (High mobility structures are designed to have only one z energy level occupied because scattering of electrons from one level to another leads to a drop in mobility.)

Using the triangular well approximation, which is reasonably accurate for the lowest energy level which has a wavefunction close to the interface, $V(z) = eFz$ where F is the electric field. Wavefunctions and energy levels can be found by substituting this $V(z)$ into Schrödinger's equation.

Assuming that the wavefunctions and energy levels have been found numerically or analytically as outlined above, the total energy is given by

$$E = [(\hbar^2 k_x^2/2m^*) + (\hbar^2 k_y^2/2m^*)] + \varepsilon_n. \qquad (4.9)$$

Three numbers k_x, k_y and n (n=1 for the case in fig 4.3) label the states and for each value of n, there is a 2DEG called an electric sub-band. The density of states or $D(E)$ is

defined as the number of allowed energy states per unit energy and per unit area. For a two dimensional system

$$D(E) = g_S g_V m^*/2\hbar^2\pi \qquad (4.10)$$

The energy levels and density of states is shown in Fig. 4.4 for the first two levels in a two dimensional system, with the spin degeneracy $g_S = 2$ and the valley degeneracy $g_V = 1$ for GaAs.

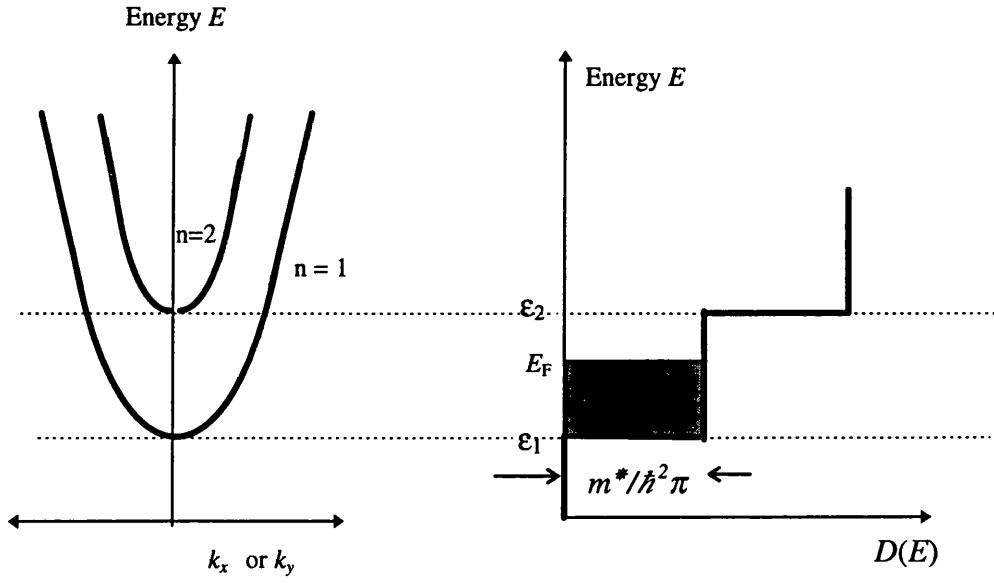

Fig. 4.4 Energy levels and density of states for a 2DEG.

At zero temperature electron states up to energy E_F are occupied; this is known as the Fermi energy. The electron sheet density $n_{2d} = E_F D(E)$ and the Fermi wave vector $k_F = (2\pi n_{2d})^{1/2}$.

In practice an undoped spacer layer is grown between the doping layer and the 2DEG in order to reduce the effect of scattering from the random potential from the ionised donor centres and an undoped GaAs cap is added to prevent oxidisation of the AlGaAs donor layer. This structure then forms the basis of the heterostructures used in experiments described in this thesis.

4.3 Transport in the 2DEG.

Electrons in the 2DEG are free to move in two dimensions. With no electric field applied, they move randomly in the x-y plane. These electrons are scattered from impurities in the conducting layer or from the potential from ionised donors. The average distance between collisions is called the mean free path ℓ and the average time between collisions the mean free time τ_c. If an electric field E is applied each electron experiences a force so that

$$F = -eE \tag{4.11}$$

then an additional velocity is superimposed on the random thermal motion of the electrons. This velocity is the drift velocity v_n. To find this drift velocity, the momentum applied to the electron (4.11 multiplied by τ_c) is equated with the momentum gained by the electron in the same period ($m^* v_n$). The resultant expression for v_n is

$$v_n = -(e\tau_c/m^*)E \tag{4.12}$$

The drift velocity is proportional to the applied field and the proportionality factor is defined as the mobility $\mu = (e\tau_c/m^*)$. The electron sheet density n_{2d} and the mobility μ define the Drude conductivity $\sigma = e\, n_{2d}\, \mu$.

A large mobility gives a high drift velocity which is generally desirable. To achieve a large μ, a low effective mass and a large time between collisions are required. The first condition is satisfied by the low effective mass of electrons in GaAs and the second is satisfied in 'pure' GaAs with low impurity scattering and the doping layer separated from the conducting channel by an undoped spacer layer. The most important mechanism then limiting the mobility at normal temperatures is scattering from lattice vibrations or phonon scattering. Scattering from lattice vibrations is reduced by cooling the devices. Devices in this work were cooled to liquid helium temperatures.

The transport of an electron through the 2DEG is determined by the mean free path ℓ. Using this length scale three regions of transport can be defined: Fig. 4.5(a) shows the

case of ballistic transport. In this regime there is no scattering by impurities of the electron over the area (which has a length L and width W). The electron scatters elastically from the constriction boundaries and the scattering angle is not changed. Part of this thesis will detail experiments made in which electrons are forced through channels with the boundaries made electrostatically. Scattering from these electrostatic constrictions at low temperatures should be elastic.

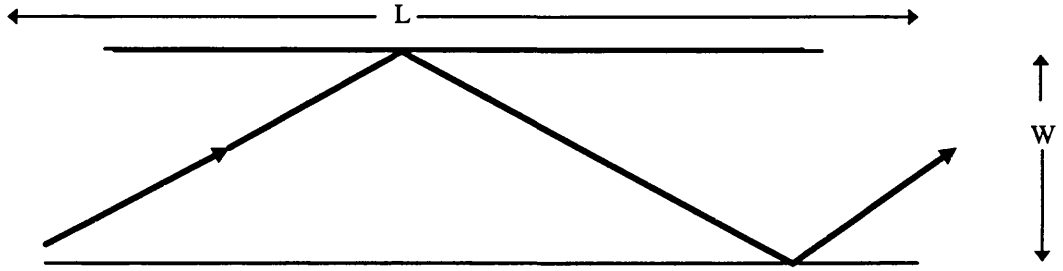

Fig. 4.5(a) Electron transport through a constriction in the ballistic regime $\ell >$ W,L

In a regime where the length scale of the device is much larger than ℓ the diffusive regime is dominated by a series of scattering events. Fig. 4.5(b) shows the trajectory of an electron in this regime. At high temperatures transport is generally diffusive.

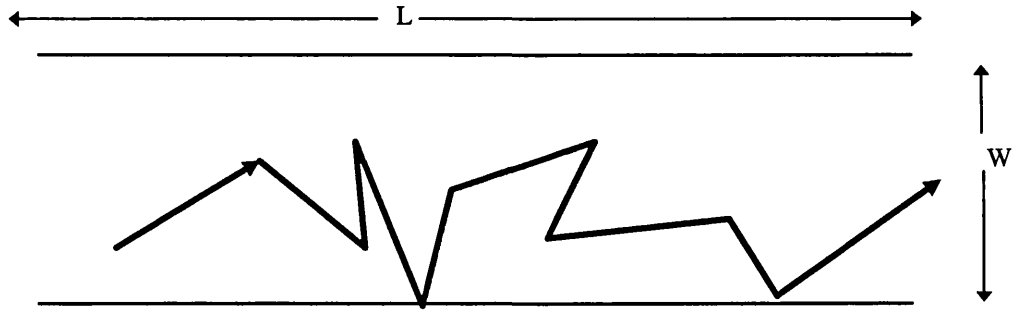

Fig. 4.5(b) Electron transport through a constriction in the diffusive regime where $\ell <$ W,L

A third regime can be distinguished, which is known as the quasi ballistic regime. In this regime, the transport is mainly ballistic, with a few random scattering events, and

$W < \ell < L$. The regime is sometimes known as the mesoscopic regime, because the exact configuration of scattering centres is important.

4.4 Layer Structure of samples used.

In all experiments the samples used were grown by Molecular Beam Epitaxy (MBE). The materials used were grown in order to trap a gas of electrons in the material at the interface between layers of semiconductors. The semiconductors used were lattice matched gallium arsenide (GaAs), aluminium arsenide (AlAs), and aluminium gallium arsenide ($Al_xGa_{1-x}As$). [The aluminium fraction, x in all material used was 30%; the term AlGaAs will be used from now on to mean $Al_{0.3}Ga_{0.7}As$].

A conventional deep GaAs-AlGaAs heterostructure is shown in Fig. 4.6

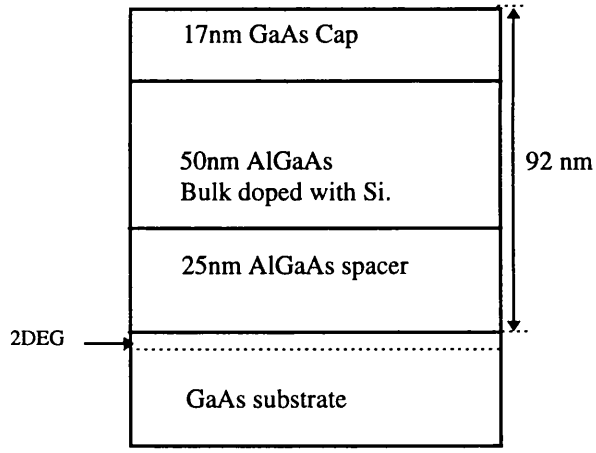

Fig. 4.6 Layer structure of a deep sample.

Recently layers have been grown at Glasgow where the 2DEG interface is only 28 nm from the surface. These layers offer advantages over the conventional layer described above due to the proximity of the conducting layer to the surface. A surface gate should give a larger and better defined potential in the conducting layer, and allow smaller gate feature sizes. The structure of these layers is shown in Fig. 4.7, for designs with AlGaAs and AlAs barriers.

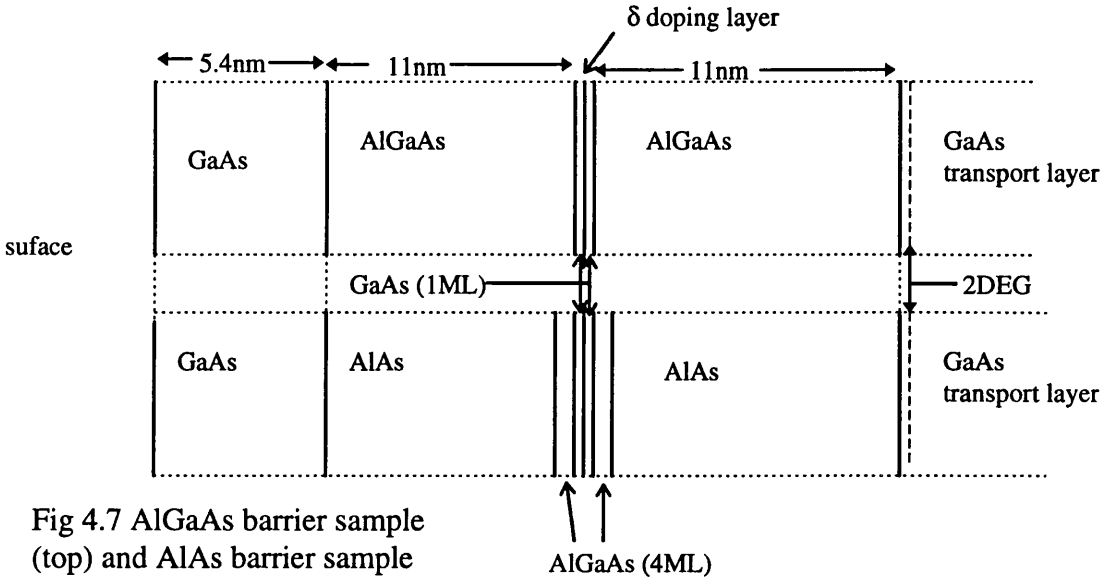

Fig 4.7 AlGaAs barrier sample (top) and AlAs barrier sample (bottom)

With the deeper structures electron mobilities of greater than 100 $m^2V^{-1}s^{-1}$ have been achieved. In the shallow structures studied in this work mobilities of up to 40 $m^2V^{-1}s^{-1}$ were measured for the AlAs barrier structure and up to 18 $m^2V^{-1}s^{-1}$ were measured for the AlGaAs barrier structure. Much materials research [5] has been carried out in Glasgow into the shallow structures and many layers have been grown. The highest mobility layers grown at Glasgow have had mobilities of 80 $m^2V^{-1}s^{-1}$ for the AlAs barrier materials and 30 $m^2V^{-1}s^{-1}$ for the AlGaAs barrier material. The proximity of the conducting layer to the donors leads to increased scattering due to the ionised impurity potential, which is the main factor in reducing the mobility of the shallow structures. The mobilities observed for AlAs barrier samples are greater. This is thought to be due to a layer of parasitic electrons around the doping layer which, although making a negligible contribution to transport, screen the conducting layer from the full potential due to the donors. The AlGaAs barrier samples however also have higher than expected mobilities. An estimate using the Born approximation with a remote plane 11 nm from the conducting layer [6] gives the mobility as 6 $m^2V^{-1}s^{-1}$. The increased mobility seen experimentally is attributed to correlations in electron occupation of the donors [5].

4.5 Band Structure of an AlGaAs/GaAs heterostructure.

Fig. 4.8 shows the conduction band energy of a deep (a) and shallow (b) heterostructure as a function of depth into the sample.

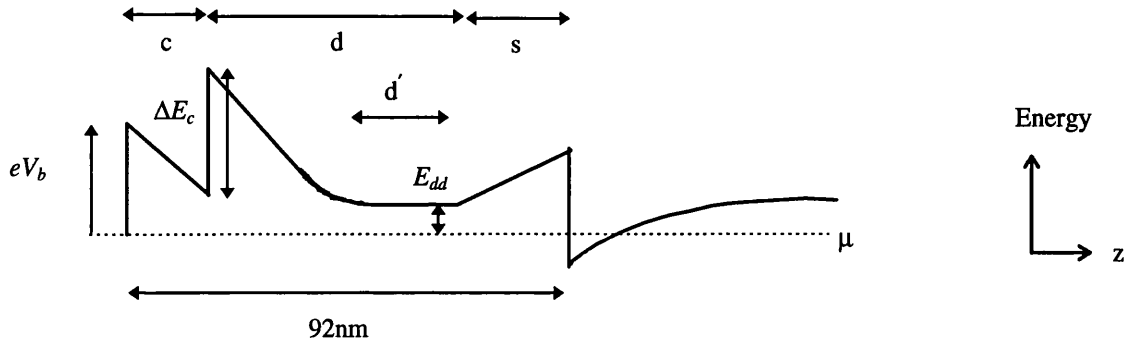

Fig. 4.8(a) Conduction band structure of a deep sample.

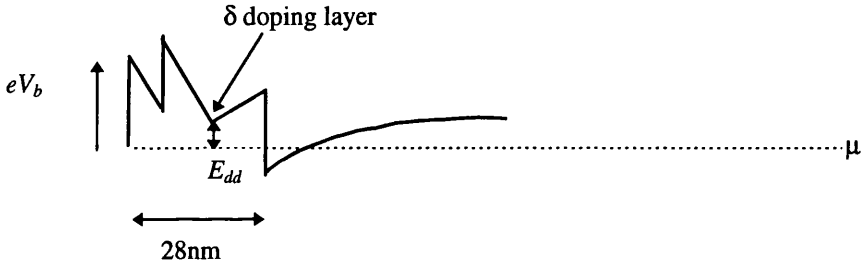

Fig. 4.8(b) Conduction band structure of a shallow sample.

Here c is the thickness of the cap layer, d is the thickness of the donor layer and s is the thickness of the spacer layer.

The band structure through the device can be used to derive values of important parameters in the layers. A parameter of interest is the threshold voltage V_t defined as that negative voltage applied to a surface gate which removes all the electrons from the channel. At this voltage n_{2d} is zero and the bands are flat in the channel. This is shown in fig 4.9 below.

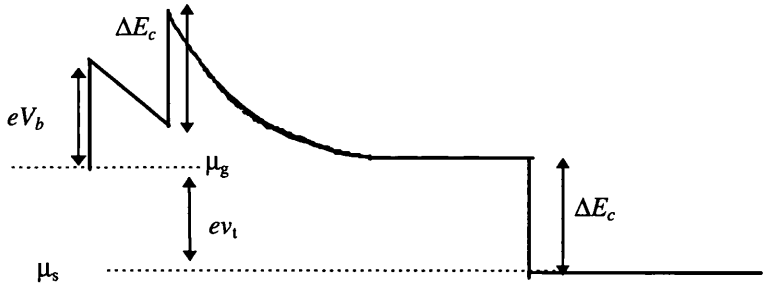

Fig 4.9 Conduction band profile at threshold

μ_g and μ_s are the chemical potentials in the surface gate and the semiconductor respectively. The model developed by Long et al [7] to describe the electrostatics of deep material makes the following assumptions: 1. On the surface of the sample there is a Schottky barrier formed by a metal semiconductor contact which pins the conduction band energy at a height eV_b above the chemical potential. 2. There is a conduction band discontinuity ΔE_c between the AlGaAs and GaAs layers. 3. Only one subband is occupied. 4. There is a doped region where the conduction band is pinned at an energy E_{dd} above the chemical potential. This region is shown as d' in Fig 4.8. Such behaviour results from the DX model referred to in section 4.1. Using this model Long et al found that the electron density in the channel n_{2d} with no gate bias

$$n_{2d} = [(\Delta E_c - E_{dd})\varepsilon_o]/[(s/\varepsilon_a + a/\varepsilon_g)e^2] \qquad (4.13)$$

where a is the effective width of the 2DEG (of the order of 8nm) and ε_a and ε_g are the dielectric constants of the AlGaAs and GaAs regions. The threshold voltage is given by $v_t^{(F)}$ where (F) indicates that the sample is at low temperatures and charge in the region of d' is frozen into the DX centres. Using simple electrostatics the threshold voltage was found to be:

$$-e\, v_t^{(F)} = e^2 n_{2d} [c/\varepsilon_g + d/\varepsilon_a + s/\varepsilon_a + a/\varepsilon_g] /\varepsilon_o \qquad (4.14)$$

These values agreed well with experimental data for deep materials [7]. Skuras et al [5] applied this model to the shallow materials and found good agreement for the values of $v_t^{(F)}$ and n_{2d} for the AlGaAs barrier material but not for the AlAs barrier material. This is thought to be due to the layer of charge in the AlAs spacer region which does not then act as a neutral region. The most obvious manifestation of this is in the threshold voltage, which is larger for AlAs samples, implying that, when a negative bias voltage is applied, the free charge in the AlAs barriers is removed first. Once this free charge is fully depleted, only then are electrons removed from the channel and the threshold reached.

4.6 The 2DEG in a magnetic field

In order to probe the effects of patterned gates on the 2DEG, it is useful to apply a perpendicular magnetic field. This leads to the quantisation of energy levels in the 2DEG, the Landau levels. In the 2DEG shown in Fig. 4.10(a) a magnetic field ***B*** is directed along the negative z axis.

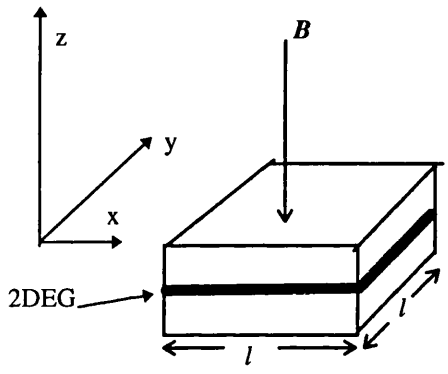

Fig. 4.10(a) Segment of 2DEG sample of dimensions $l \times l$

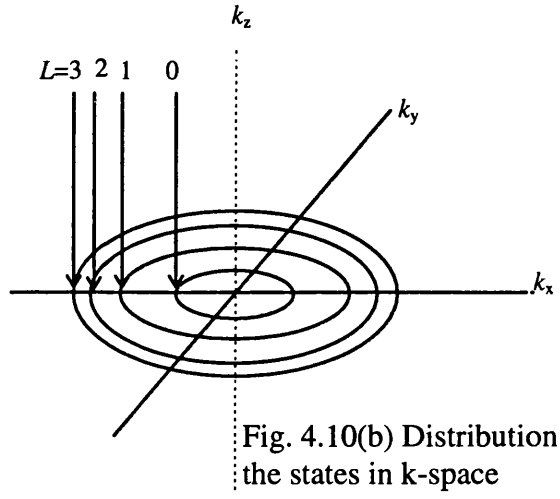

Fig. 4.10(b) Distribution of the states in k-space

Prior to the application of the magnetic field, the electron states were uniformly distributed as an infinite array of points in the x-y plane in k space [8], with spacing between the states of $2\pi/l$ (where l is defined in fig 4.10(a)). With the application of magnetic field, states of higher and lower energies condense into rings of constant energy and move tangentially to these lines, as schematically shown in Fig. 4.10(b). In real space, this results in circular motion. The angular frequency of this motion is the cyclotron frequency

$$\omega_c = eB/m^* \tag{4.15}$$

and the energy is quantised into levels of

$$E_L = (L + 1/2)\hbar\omega_c \text{ , where } L = 0,1,2,3... \tag{4.16}$$

As the magnetic field increases it can be seen from equation 4.15 and 4.16 that the spacing of the energy levels increases. The situation for three occupied Landau levels below the Fermi energy is shown in Fig. 4.11. for $T = 0$ K (in reality the energy states occupied broaden out reflecting thermal, impurity and disorder broadening).

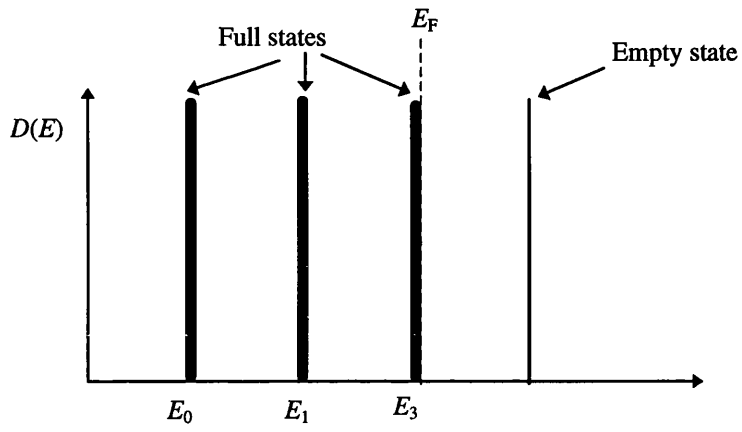

Fig. 4.11 Landau level distribution at T= 0 K

The quantisation of energy into Landau levels manifests itself in different ways depending on the combination of measurement contacts. The 2DEG samples are fabricated as Hall-bars and current passed through the sample. Different measurements of voltage can be made, shown as V_{2t},V_L and V_H in fig 4.12.

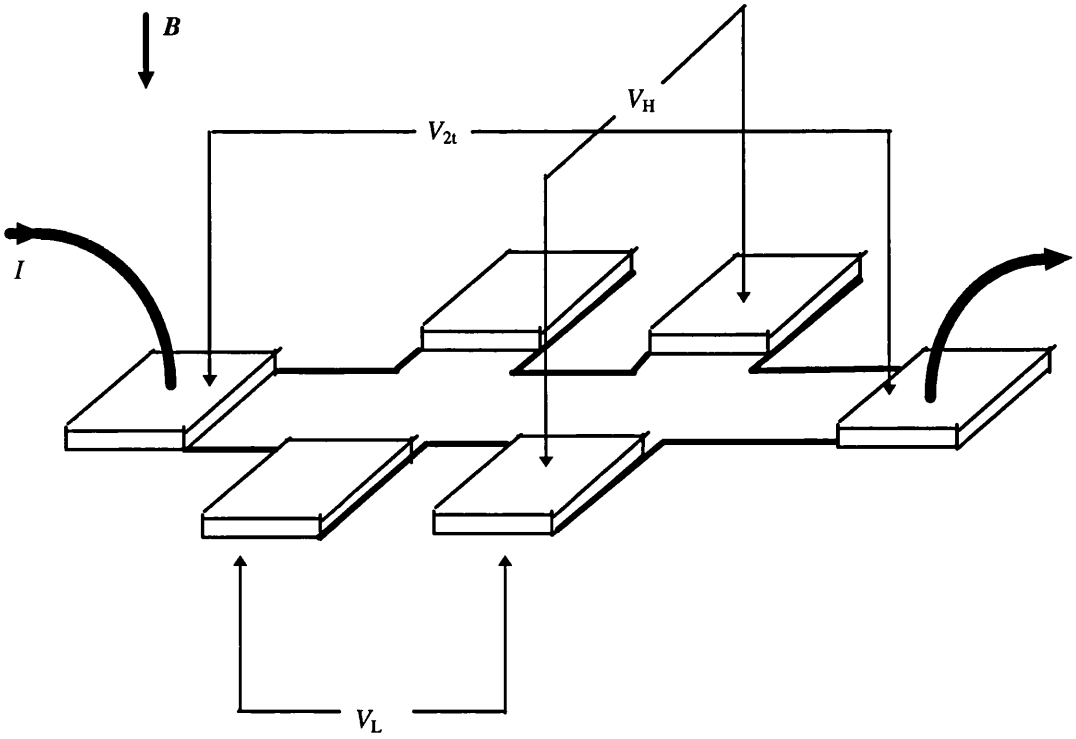

Fig. 4.12 Schematic representation of a Hall-bar showing important measurement configurations.

Measurements are made at temperatures of 4.2 K or less in a magnetic field linearly varying with time. A measurement of I/V_{2t} is a two terminal measurement and shows a series of plateaux in units of e^2/h. Measurement of V_L/I is a longitudinal measurement and reveals a series of oscillations called Shubnikov de Haas (SdH) oscillations. In this work, measurements with this combination of contacts are referred to as SdH type measurements. Measurements of I/V_H again reveal the quantum Hall effect which shows up as quantisation in units of e^2/h.

The most complete explanation of the effects seen in the measurements above comes from the concept of edge channels. When a magnetic field is applied, electrons travel down the Hall-bar in helical paths. In k-space electrons occupy orbits determined by the magnitude of the magnetic field. Near the edges of the channel, and around potential fluctuations in the bulk, the electrons travel in edge states. Edge states correspond to electrons in skipping orbits which interact with one side of the Hall-bar. Edge states move in opposite directions on opposite sides of the Hall-bar. This is shown below in fig 4.13.

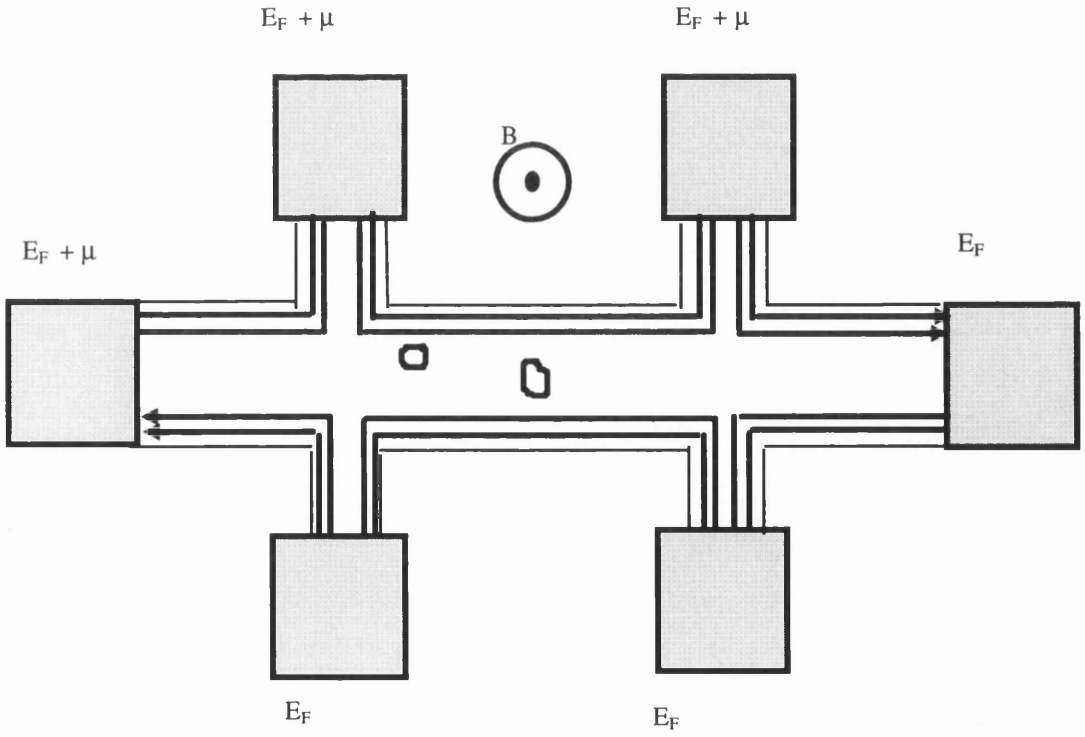

Fig 4.13 Hall-bar carrying current in edge states, also shown are localised states in the centre of the Hall-bar due to potential fluctuations in the bulk.

In the presence of a chemical potential difference $\delta\mu$ each edge channel carries a current of $(e/h)\delta\mu$ which contributes h/e^2 to the Hall resistance [9] and in the case of local equilibrium this is the same as the two terminal resistance [10]. This assumes that each edge channel corresponds to one spin split Landau level. A two terminal or Hall measurement shows an increasing resistance quantised in steps of h/e^2.

A SdH measurement reveals a series of oscillations periodic in $1/B$ with a spacing given by $\Delta(1/B)$.

$$\Delta(1/B) = g_S g_V e/hn_{2d} \qquad (4.17)$$

Here g_S and g_V are the spin and valley degeneracy and have the values 2 and 1 respectively.

This measurement of V_I/I versus B allows an estimation of the carrier concentration n_{2d}. The minima in the oscillations correspond to the situation where all the current is carried in edge channels. For strongly confined and well separated edge channels, there is no electron back-scattering and hence the longitudinal resistance falls to zero.

Fig 4.14 below shows another view [10] of the edge channels. The edge channels are formed where the Landau levels rise at a boundary of a constriction (either defined electrostatically or by etching). The intersection of the Fermi energy with the nth Landau level forms the edge channel.

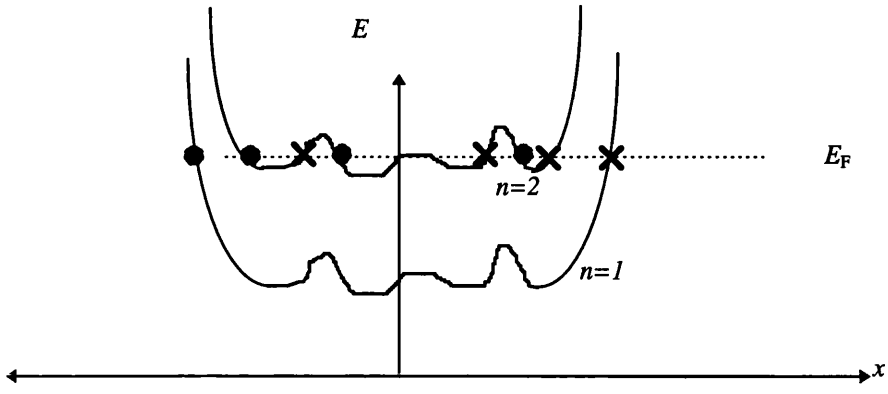

Fig. 4.14 E-x plot of the Landau levels in the channel of a Hall-bar

From Fig. 4.14 it can be seen that, for small potential fluctuations in the bulk of the sample, only states in the highest Landau level contribute to the conductance. The above simple theory is a one electron picture which does not take into account electron-electron interactions or screening effects in the presence of a magnetic field.

The one electron picture shown in Fig 4.14 suggests that the two terminal conductance should increase abruptly. When a bulk Landau level passes through the Fermi energy. However such steep steps are not seen experimentally either for bulk Hall-bars [11] or in short clean channels such as point contacts [12], and so the simple edge state picture needs to be developed further. A qualitative theory was proposed by Beenakker and Chang who divided the 2DEG at the boundary into alternating strips of compressible bands corresponding to the edge channels in fig 4.14, and incompressible bands [13]. A quantitative picture was developed by Chklovskii, Shklovskii and Glazman (CSG) [14] for an electrostatically defined boundary between the edge of the 2DEG and the bulk. CSG found that the position and width of the strips of incompressible fluid could be calculated from the density of the 2DEG in zero magnetic field.

Fig 4.15 is a representation of the self consistent electrostatic picture. Fig 4.15a) Shows a top view of the 2DEG near the gate (the edge of the gate corresponds to $x = 0$ in Fig 4.15) with the arrows indicating the direction of current flow, fig 4.15b) shows the bending of the electrostatic potential and the Landau levels and Fig 4.15c) the electron density as a function of distance to the middle of the depletion region. With the application of magnetic field CSG found that narrow strips are formed along lines where an integer number of Landau levels are occupied. CSG called these strips dipolar strips.

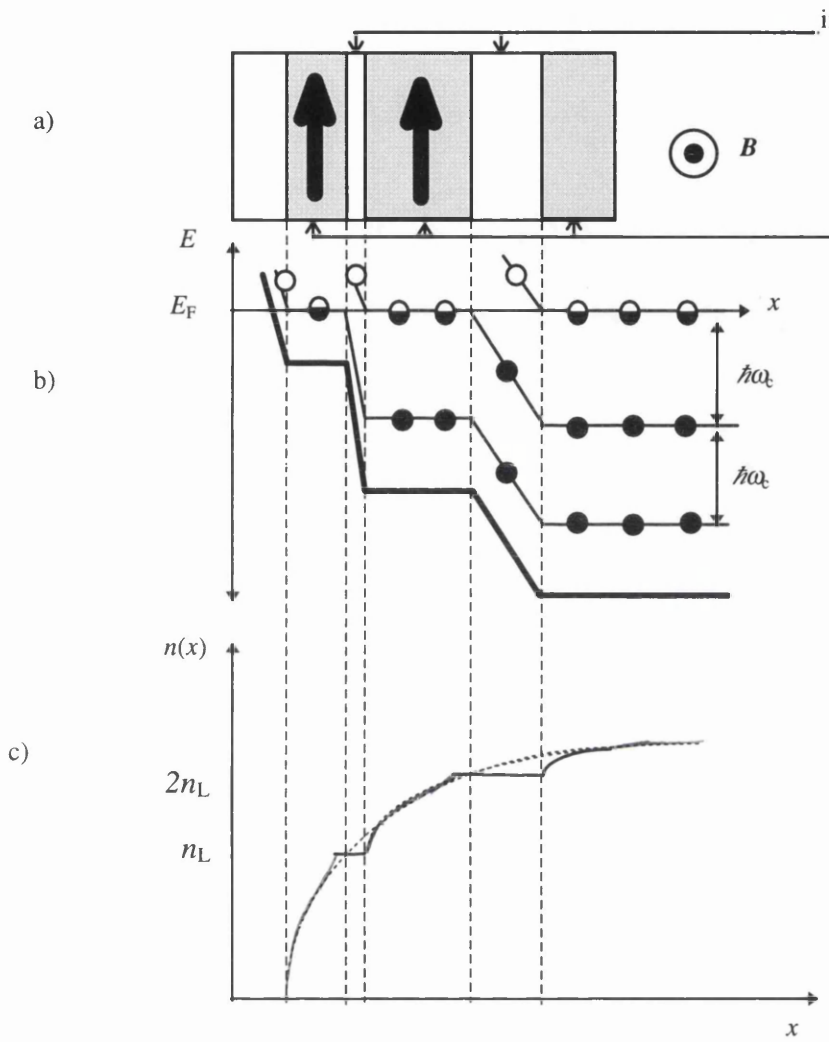

Fig. 4.15 Representation of 2DEG at the edge of the channel. Taken from CSG [14]. Here ● represents a filled state ◒ a partly filled state and ❍ an empty state. a) shows a top view of the 2DEG near the gate. b) shows the bending of the potential and the Landau levels and c) shows the electron density as a function of distance to the middle of the depletion region.

According to CSG the dipolar strips produce a steep drop in the electrostatic potential which brings the next Landau level to the Fermi energy. The relationship between the widths of adjacent compressible and incompressible strips does not depend on strip number, magnetic field or gate voltage, provided that the widths are greater than the magnetic length, ($l_m = (\hbar/eB)^{1/2}$). The electron density distribution changes from being step like to having much smaller steps quantised at n_L and $2n_L$ (n_L is the electron

density for one completely full Landau level) superimposed on a background which is the electron density at zero magnetic field.

Chklovskii, Matveev and Shklovskii (CMS) [15] proposed a quantitative electrostatic theory for an electrostatically defined channel such as a point contact. The description of the situation at the edge of the constriction is not substantially different from the half plane in CSG, but they divided the state of the channel into a *C* (compressible) or an *I* (incompressible) state depending on whether the centre of the channel was occupied by a region of compressible or incompressible liquid. The *I* states lead to plateaux in the Hall conductance at values of $e^2/2\pi\hbar$ multiplied by the filling factor analogous to that defined in the one electron representation. Joining these narrow plateaux are much wider regions where *C* states are dominant. Here the conductance is not quantised. Experimentally a situation is found somewhere between the one electron theory and the CMS theory. CMS attribute this to disorder in the channel.

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Chapter 5

Measurements on electrostatically formed longitudinal wire arrays.

5.1 Motivation and introduction.

5.1.1 Motivation.

In this chapter measurements made on electrostatically formed multiple quantum wires will be described. The first aim of these measurements was to find out if there was any evidence of one dimensional quantisation of energy when the electrons were trapped in channels less than 250 nm in width. All quantisation experiments were carried out on devices made with multiple HRN ribs. Several devices were measured. Quantisation was not observed although there was strong evidence that the wires were formed. Evidence will be presented that the lack of quantisation was due to inherent problems with the fabrication process and also the low mobility of shallow AlGaAs materials.

A second aim of the experiments in this chapter was to clearly differentiate between two models which are used to predict the cut-off voltages of the wire arrays. These models, which are known as the 'pinned' and 'frozen' models, differ in the boundary conditions describing the ungated GaAs surface condition used in the calculation of the cut-off voltage. The experiments using HRN ribs did not give conclusive results in this area and so an additional type of device was fabricated. This new type of device consisted of a periodic array of strips of metal formed using positive resist techniques (no HRN was used in the fabrication of these devices so they are different to those devices which were used for the quantisation experiments). These later devices gave convincing evidence that the frozen model correctly describes the surface condition of the ungated GaAs.

5.1.2 Introduction.

5.1.2.1 HRN longitudinal wires devices.

The fabrication of narrow channels using wet etching, the process used to define channels in Hall-bars, is not reliable below 1μm because of irregularities in the exposed sidewalls of the structure [1]. The technique chosen to investigate 1D effects in narrow longitudinal wires uses a gate split by negative resist ribs. The electrostatically formed wires are fabricated using strips of negative resist with an overlying Schottky gate. In order to probe for one dimensional confinement the negative resist wire patterns were fabricated on Hall-bars. A schematic diagram of this arrangement is shown in Fig. 5.1.

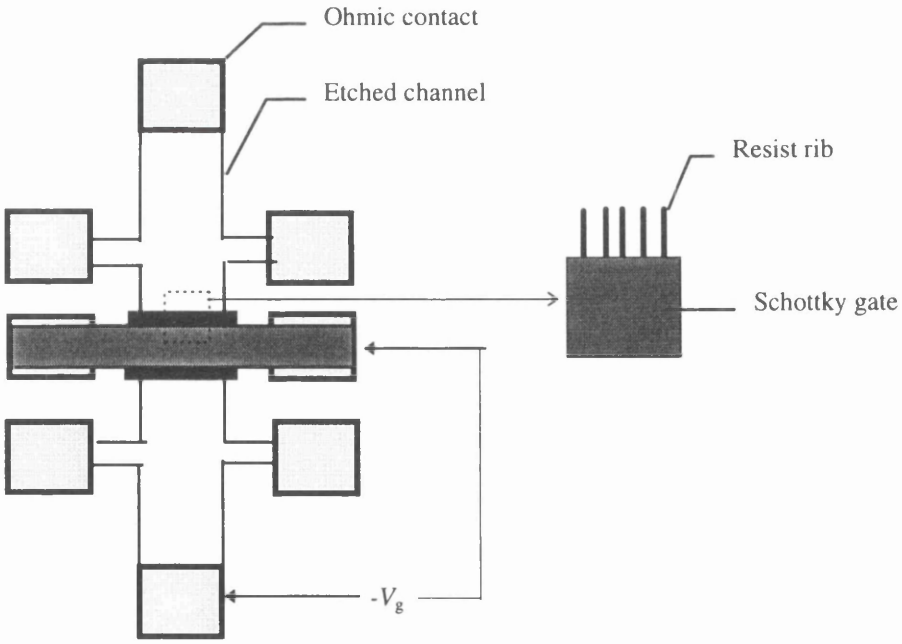


Fig 5.1 Diagram of Hall-bar and gate arrangement for measurement of electrostatically formed wires.

Detail is shown of the negative resist wires running underneath the gate. When a negative voltage $-V_g$ is applied to the gate, electrons in the 2DEG are initially depleted from the areas where the gate is in contact with the cap, leaving electrons in channels defined by the negative resist. This is shown schematically in Fig. 5.2.

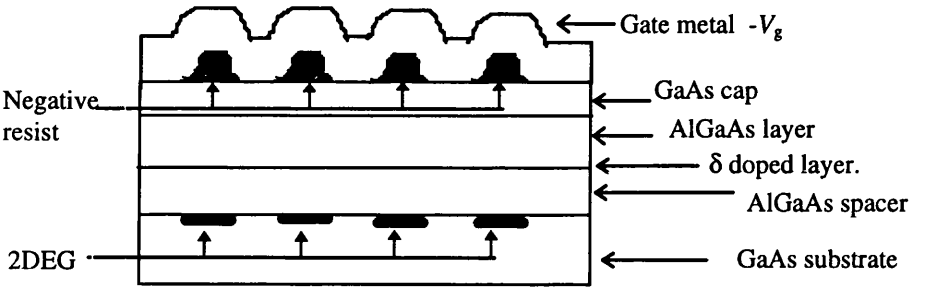


Fig 5.2 Diagram of resist profiles and gate arrangement. The vertical dimension is accentuated with respect to the horizontal dimension for clarity.

For comparison purposes devices were also fabricated without the resist ribs but with the same overall dimensions. These devices are referred to as 'big-gate' devices.

5.1.2.2 Side gated finger superlattice devices.

Side gated finger superlattices are strips of metal fabricated using positive resist techniques and are formed perpendicular to the direction of current flow. The fingers do not traverse the full width of the Hall-bar. This means that the areas between gate fingers are open to the ungated bulk of the channel and charge can flow into and out of these regions in response to changes in gate bias. Although the fingers are laid laterally across the Hall-bar, this ready access to the regions between means that these devices act analogously to 'longitudinal' wire arrays. A plan view of the important details of the Hall-bar and a few periods of the finger superlattice (there are typically 100 or 120 periods) is shown in fig 5.3 below.

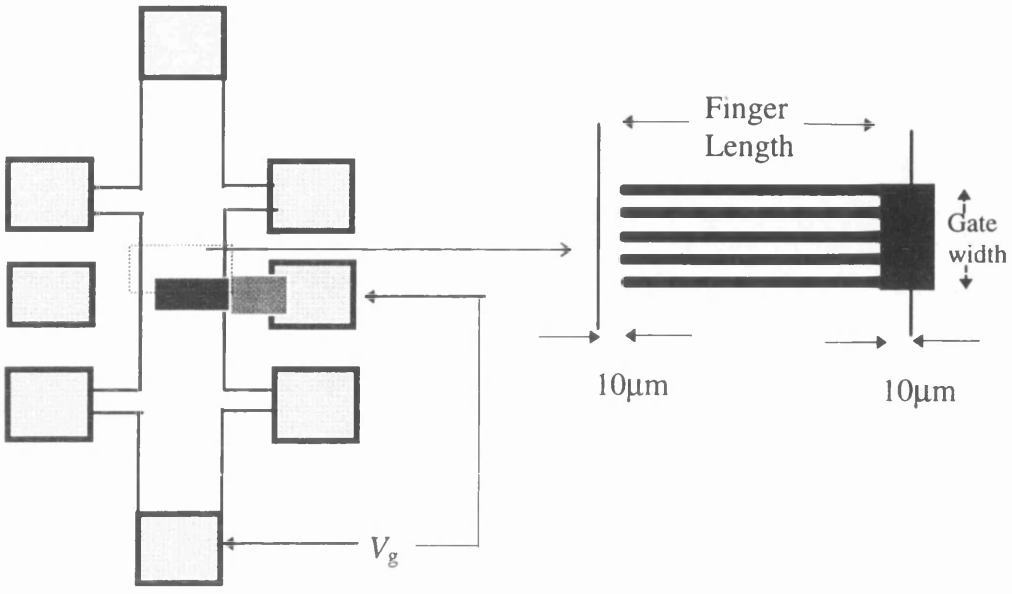


Fig 5.3 Schematic diagram of gate fingers on Hall-bar with detail of gate layout.

Detail is shown in fig 5.4 of the gates on the surface of the GaAs, a side elevation of fig 5.3. With no gate bias, the 2DEG is uniformly distributed below the gate shown in Fig 5.4 (a). A negative bias is applied until electrons are depleted from below the gated areas. This region is termed the 'gate region' and the bias voltage defining this is V_t as shown in Fig 5.4 (b). As the bias voltage is increased, a point V_c is reached, shown in Fig 5.4 (c), where all electrons are depleted from beneath the ungated regions; this defines the 'tail' region. Making V_g more negative than V_c defines the cut-off region.

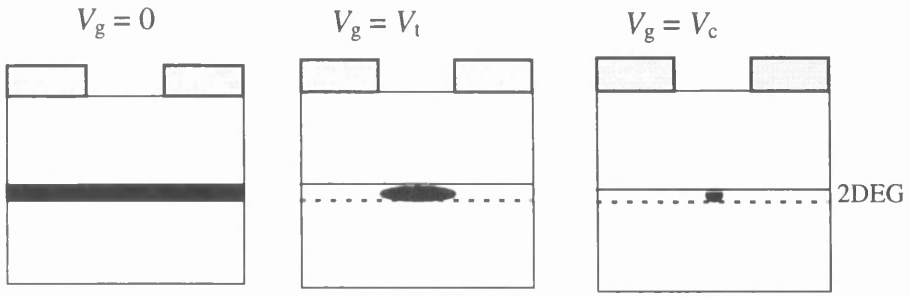


Fig 5.4 (a) Fig 5.4 (b) Fig 5.4 (c)

Fig 5.4 a) - c) Schematic sectional view of the 2DEG for values of V_g

These devices were fabricated to test whether the 'frozen' or 'pinned' model better describes the surface of the GaAs. Two problems were found in making the same test with the HRN devices. The first was the presence of metal on top of the resist. This part of the gate was believed to produce a bias which depleted the electrons under the HRN ribs when bias was applied. Secondly there was the problem of the poor profile of the HRN ribs, because of the areas exposed by backscattered electrons during writing in the electron beamwriter. Positive resist has a much better profile after development and the subsequent lift-off produces strips of metal very close to the ideal picture seen in fig 5.4.

5.1.3 1D Transport.

5.1.3.1 HRN longitudinal wires background theory.

A one dimensional electronic system is one whose energy levels consist of a set of defined 1D quantum subbands. Electrons have only a free dispersion in the *y* direction. The energy levels are given by

$$E^{ij}(k_y) = \hbar^2 k_y^2/2m^* + E^i_x + E^j_z \qquad (5.1)$$
$$(i,j = 0,1,2,3.....)$$

The gate voltage which confines an electron to the wire produces a force varying approximately linearly with lateral position. This leads to a parabolic confining potential. Laux et al [2], using self consistent band structure calculations, found that the confining potential for electrons has a parabolic shape for a small number of electrons. Screening then flattens the potential making it more 'U' shaped. Increasing 1D densities in the wire reduce the subband separation [3]. In the case of only a small voltage applied to the gates, or if there is an additional screening layer present, there is only a variation of carrier concentration under the gate. Regions of high carrier concentration correspond to lines where wires will eventually be formed. These regions of high carrier concentration are separated by strips of lower concentration, which eventually become the regions that are fully depleted of electrons. For the

limiting case where regions of charge under resist strips and gates are the same, this situation is indistinguishable from the case of electrons under a large plane gate.

The density of states in a 1D system is given by

$$\rho(E) = [m^*/\pi\hbar^2].[\hbar^2/(2m^*/E - E_n)]^{1/2} \qquad (5.2)$$

A system with four occupied 1D subbands is shown below in Fig. 5.5; all states below E_F are filled

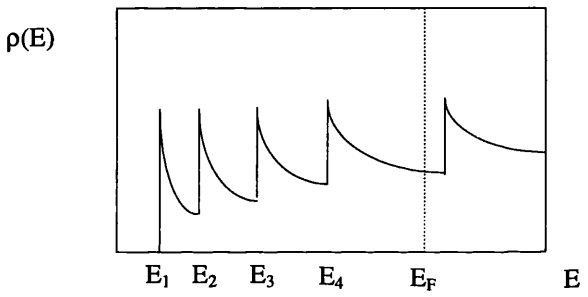


Fig 5.5 Quasi-1D wire density of states with four sub-bands occupied

The application of a perpendicular (to the sample surface) magnetic field leads to mixed magneto-electric sub-bands. This occurs when the circulating electron waves can interact with both of the boundaries. The critical field B_C for the formation of these sub-bands is that which the wire width (W) is equal to the cyclotron diameter [4].

$$B_C = [h(2n_{2d}/\pi)^{1/2}]/eW \qquad (5.3)$$

At fields greater than B_C the behaviour is that of a 2DEG.

Using resistance, magneto-resistance, capacitance, and magneto-capacitance measurements, it was hoped in this work to detect one dimensional confinement in wires formed using the HRN split gate technique on shallow AlGaAs materials.

5.1.3.2 Resistance measurements.

A four terminal longitudinal measurement of resistance as a function of negative gate bias shows an increasing resistance. As the gate is made more negative with respect to the 2DEG, electrons are depleted from the 2DEG and this reduces the carrier concentration. With the split gate technique, the areas underneath the Schottky gate are depleted first. When the electrons are fully depleted from under the gate this defines the threshold voltage V_t. With increasing negative bias, the areas under the resist strips are squeezed by a combination of the potential from the side and through the resist layer above the electrons. Eventually when all electrons are depleted the cut off voltage, V_c, is reached. Davies [5] developed models for the ratio V_c/V_t, depending on the GaAs surface conditions, for a single split gate wire formed electrostatically as shown schematically in Fig. 5.6. The thickness of the HRN ribs is approximately 60 nm, and to use these models it must be assumed that the effect of the gate through the resist is negligible.

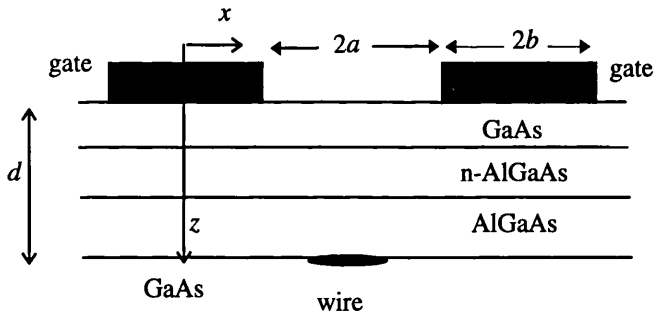


Fig. 5.6 Diagram showing critical dimensions of a single split gate electrostatically formed wire

With no bias applied, all chemical potentials in the system are equal. When negaative bias is applied to the gate, the behaviour of the device depends on what assumptions are made about the response of the semiconductor surface. There are two extreme models which have been applied, the "pinned surface" model and the "frozen surface model". In the former, the chemical potential at the surface in the ungated regions is assumed to remain unaltered at a value defined by the surface states, whilst the

chemical potential in the area under the gate changes in response to the applied potential. This potential difference between gated and ungated areas forms the wire. Using the boundary conditions (that the free surface is an equipotential and the electric field tends to zero as z tends to infinity) and solving Poissons's equation, the ratio of threshold voltages can be estimated. For this model, known as the 'pinned' model,

$$V_c/V_t = \{1 - (2\arctan(a/d))/\pi\}^{-1} \qquad (5.4)$$

Here a and d are defined in Fig 5.6. The problem with this model is that charge must move from the 2DEG to the surface in response to a change in V_g to keep the free surface an equipotential. This is feasible at room temperature, but is unlikely when the device is cooled to typically 1.5 K (because of the Schottky barrier at the surface).

The other model, known as the Frozen model [6] treats the surface like a dielectric with a fixed charge density. On biasing the gate no charge is exchanged with the 2DEG. The surface boundary condition is that the normal derivative of the potential $\delta\phi/\delta n = 0$, giving

$$V_c/V_t = ((a/d)^2 + 1)^{1/2} \qquad (5.5)$$

The above results are for a single wire. Recently the calculation has been extended to a periodic structure for the pinned condition [7]. The result for the pinned surface is

$$V_c/V_t = \pi[\, 2\arctan(\tanh(\pi d/2(a+b)))]^{-1} \qquad (5.6)$$

A value of V_c/V_t for the frozen model is obtained by finding a solution [8] which, matches the boundary condition and is a solution of Laplace's equation

$$V_c/V_t = \{2(a+b)/\pi d\}.\cosh^{-1}\{[\cosh(\pi d/2(a+b))].[\cos(\pi a/2(a+b))]^{-1}\} \qquad (5.7)$$

Measurements of conductance as a function of gate voltage should show two regions corresponding to $0 > V_g > V_t$ and $V_t > V_g > V_c$. By comparing the results from the

experiments on longitudinal channels of electrons formed using HRN ribs and lateral channels formed using side-gated finger superlattices to the above models, it was hoped to determine whether pinned or frozen surface conditions better describe the surface of GaAs at low temperatures.

5.1.3.3 Magneto-resistance measurements

a) Shubnikov de Haas measurements.

Here the magnetic field is swept from zero at a fixed rate (0.15T/minute or 0.3T/minute were used for these measurements). The gate bias is fixed at a value between zero and the cut-off voltage. The longitudinal resistance across the gated region is measured. A measurement of resistance at a given gate voltage as a function of magnetic field will be referred to as a SdH (type) measurement.

A SdH measurement of an ungated Hall-bar shows a series of oscillations, whose period is dependent on the carrier density. When a SdH measurement is made on a gated region with bias there are two regions of differing carrier concentration in series. This is reflected in the SdH measurement as mixture of two oscillations corresponding to the two regions. The values of the carrier concentration under the gate can then only be recovered by using Fourier transform techniques. The SdH measurements were Fourier transformed by first interpolating to give data equally spaced in 1/B then applying a fast Fourier transform routine.

Most evidence of confinement effects in 1D systems [9,10,11,12] has been seen using longitudinal measurements. In a 2D system, the minima of the SdH oscillations are periodic in 1/B. As the magnetic field decreases, an ever increasing number of oscillations are found (in principle). In a 1D system however the number of subbands occupied at zero field is finite. Only a finite number of magneto-electric sub-bands are formed and hence SdH oscillations occur which are no longer linear in 1/B. The critical field B_c for the formation of these hybrid magneto electric sub-bands is given

by (5.3). Well above this critical field the cyclotron radius is smaller than the constriction and the electrons behave as in an unbounded 2DEG.

The first observation of this effect was made by Berggen et al [12]. Berggen et al noted deviations in the minima of SdH oscillations from the positions expected for bulk behaviour, when their wire width was estimated to be between 250 and 150 nm.

For surface gated wires such as those fabricated in this chapter where the gate bias is set in the region $0 > V_g > V_t$, the effect is approximately as for a 2DEG under a planar gate. In this thesis a planar gate is referred to as a 'big-gate'. For a gate bias value of $V_t > V_g > V_c$, the wires form and narrow. For well defined wires, edge channels propagate down the wires if the wire is sufficiently wide. As negative bias is applied to the gate the number of propagating edge channels is reduced as the bias approaches the cut-off voltage. Recently [13] deviations in minima of 1/B vs. Landau index plots of wires formed using multiple HRN ribs have been seen on high mobility deep material by M. Kinsler.

b) Haug measurements [14]

For these measurements, the magnetic field is set to a minimum of the bulk longitudinal magneto-resistance SdH trace. This minimum corresponds to an integer filling factor in the ungated area. When the gate bias is swept towards cut-off, the resistance increases and shows plateaus at quantised values. Such measurements of resistance as a function of gate voltage for a given magnetic field will be referred to as Haug (type) measurements. N_g edge channels pass under the gated region (either under the gate for $V_t < V_g < 0$ or through the wires for $V_c < V_g < V_t$) and N_w in the bulk region. The four terminal longitudinal resistance is given by [14]

$$R_L = [h/2e^2].[1/N_g - 1/N_w] \qquad (5.8)$$

The positions of the plateaux given by (5.8) are used to obtain the carrier concentration as a function of bias. This is a simpler method of finding out how the carrier concentration varies with bias than the SdH technique because it is not necessary to further process the data using Fourier transform methods.

As the gate bias is made more negative, it might be expected that the resistance increase monotonically, (as 5.8 predicts). However, in practice, the resistance dips after a plateau and then rises again. A theory for this behaviour has been put forward by Haug [15], based on competition between backscattering from and tunnelling through localised states in the barrier region, which suggests, as observed in experimental work, that some edge states that are totally reflected may be partially transmitted as the barrier height is further increased.

5.1.3.4a Capacitance measurements of HRN devices.

The capacitance is a measure of the free charge in the system. The dynamic capacitance is defined to be $C = \delta Q/\delta V$ where Q is the total charge and V is the voltage applied to the gate. A measurement of integrated capacitance as a function of voltage gives an estimate of the total movable charge in the system, including any charge in the AlGaAs doping layer. If all charge can be moved at the measurement frequency, then the carrier concentration n_{2d} can be calculated from $Q/A = n_{2d}e = -\int C dV$ calculated for $V_c < V_g < 0$.

For an ideal 2DEG of zero thickness, Stern [16] showed the channel capacitance is directly related to the density of states

$$A/C_c = \gamma Z_0/\varepsilon_r\varepsilon_o + 1/(e^2 dn/d\mu) \qquad (5.9)$$

where A is the area of the capacitor, γ a numerical constant of order unity, Z_0 the average position of the electrons in the channel and ε_r the relative dielectric constant of GaAs. Assuming A, γ, Z_0, and ε_r are constant, Stern showed that magneto-capacitance data could be inverted to extract $dn/d\mu$, the thermodynamic density of states of a 2DEG at the Fermi energy.

Smith et al. [17] used capacitance measurements to show confinement effects in back-gated multiple wire devices. These were fabricated by etching a periodic array of lines in the cap layer and depositing a surface gate. The wires were then formed electrostatically by applying a bias voltage. A differential measurement of capacitance vs. gate bias between the surface-gate and a back-gate revealed oscillations which were explained by Stern's theory, modified to correspond to the 1D case. The structure of this device is different to that used in this work, which may be important in the explanation of the absence of oscillations in devices measured in Glasgow [18].

A simple model was calculated by Long et al [19] for the capacitance for a 2DEG in a bulk doped device fabricated with a plane gate and measured at low temperatures (1.5 K). This model assumes that no free charge exists in the dopant layers.

$$C/A = \varepsilon_o\{a/\varepsilon_g + s/\varepsilon_a + d/\varepsilon_a + c/\varepsilon_g\}^{-1} \qquad (5.10)$$

where ε_o is the permittivity of free space, ε_g and ε_a the relative permittivity of GaAs and AlGaAs respectively, A the area of the electrodes, a the effective thickness of the 2DEG (assumed to be 8 nm), s the thickness of the spacer layer, d the thickness of the doping layer and c the thickness of the cap layer. (5.10) is the series combination of the different layers in the structure. This relation can also be derived from (5.9) by assuming an effective thickness of the 2DEG of value a. Capacitance measurements were made on several devices with different layer thicknesses and the values of capacitance will be compared with the predictions of (5.10).

A measurement of capacitance as a function of gate bias will show a decreasing capacitance as the bias goes negative, reducing the charge density beneath the gate. A measurement of the capacitance of a wire device should show two regions corresponding to gate and wire depletion. If these two regions are not seen, then whether wires have been formed is questionable. The two regions are shown schematically in figure 5.7.

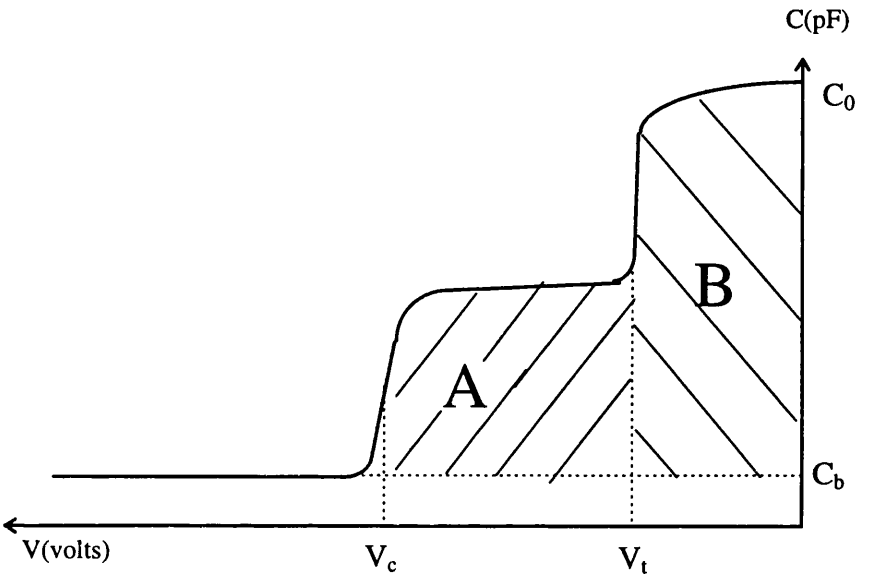


Fig. 5.7 Representation of a possible capacitance measurement of a multiple parallel wire device showing critical values.

Theoretical values of V_c /V_t have been derived from electrostatics and were given as (5.6) for a pinned surface and (5.7) for a frozen surface. Experimental values of V_c and V_t are taken from the measurement graphs at positions shown on fig. 5.7. In fig. 5.7 Region B corresponds to the charge depleted under the gate region and region A the charge under the HRN wires. The areas A and B should be approximately in proportion to the appropriate areas of the device. For example for a device where the ratio of gate area to wire area is 1:1, it is expected that the areas of each region $\int CdV$ (which is a measurement of charge) should be the same. Carrier concentrations that were obtained by estimating $\int CdV$ of the whole region can be compared to carrier concentrations that were obtained from SdH calculations. The charge $\int CdV$ was estimated using the integral function on the graph program easyplot for the total hatched area in fig. 5.7. Also shown in fig 5.7 is C_b, the capacitance of leads and connections, which is subtracted to give the actual capacitance of the device

$C_m = C_0 - C_b$.

5.1.3.4b Capacitance measurements of side gated finger superlattice devices.

Side gated finger superlattices were also investigated mainly using capacitance-voltage techniques as described above). In addition resistance and magneto-resistance measurements were made. These are not as useful as the capacitance measurements but do give confirmation of the cut-off voltages and zero-bias carrier concentration. The experimentally derived values of V_c /V_t and the areas under the C-V curves (as shown schematically in fig 5.8) were determined and will be compared with the theoretical results (as described above in section 5.1.3.4a).

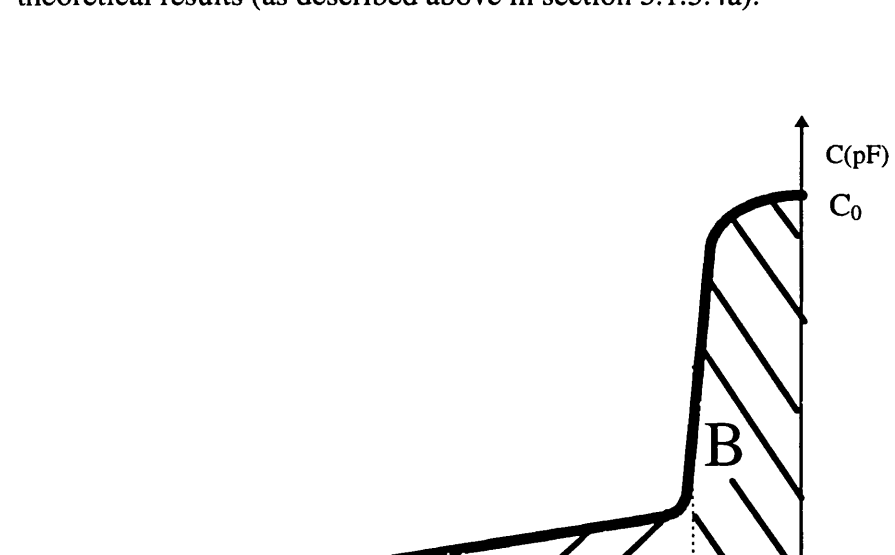


Fig. 5.8. Schematic diagram of typical measurement showing capacitance and voltage values.

5.1.3.5 Magneto-capacitance measurements.

A measurement of capacitance of a large gate as a function of magnetic field shows minima periodic in $1/B$, similar to SdH oscillations in magneto-resistance measurements. These minima can be used in a similar way to the magneto-resistance SdH oscillations to estimate the carrier concentration [21]. The minima occur because, when the magnetic field is set so that when the Fermi energy is between two Landau levels, the capacitance measured is that between the gate and the edge channels, which is much less than that to the bulk of the 2DEG.

For gates on HRN ribs, it was expected that the application of bias would change the edge channel capacitance due to the formation of edge channels along the multiple parallel wires. If the wires were successfully formed the capacitance in the minima should reflect this increased edge channel capacitance.

5.2. Materials and structures.

5.2.1 Materials and gate structures used for the fabrication of HRN longitudinal wire devices

All materials used in this work were 28nm depth shallow AlGaAs barrier materials δ-doped with 2 x 10^{16} m^{-2} silicon atoms for A707 and 4 x 10^{16} m^{-2} silicon atoms for A909 and A866. Measurements were carried out on different gate geometries. A summary of the design dimensions of the wire devices measured is shown below in table 5.1.

Device number	Gate length [μm]	Gate Width [μm]	Gate Area [x10^{-9} m^2]	Resist rib width [nm]	Rib Period [nm]
A707 #1,2,3	20	100	2	100 250 Big-gate	500 500
A866 #2	20	200	4	200 Big-gate	2000
A909 #2,3	50	200	10	200 Big-gate	2000

Table 5.1 Critical dimensions for the devices measured in this chapter.

For comparison purposes devices were measured without the resist strips but with the same overall dimensions. These are referred to as 'Big-gate' devices.

5.2.2 Materials and Structures used for side gated finger superlattice structure devices.

Three materials were used for the finger superlattice work.

A909 is a shallow AlGaAs material already used in the longitudinal wire work detailed previously; the layer structure was shown in fig 4.7 .

B591 is an AlGaAs intermediate depth material. The layer structure is shown below in fig. 5.9. A648 is a deep bulk doped sample. The layer structure is shown in fig 4.6.

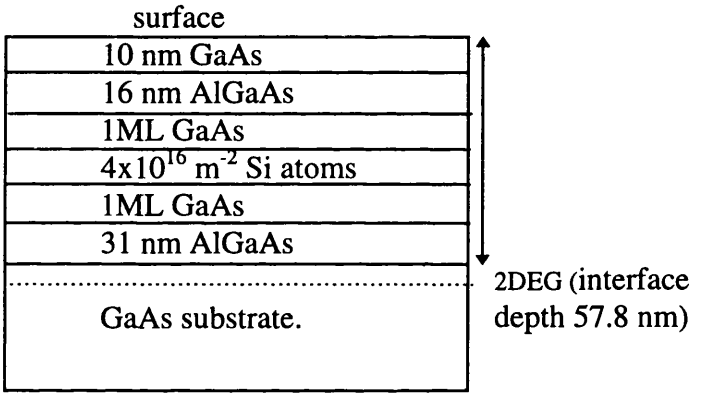


Fig. 5.9. Layer structure of intermediate depth sample B591.

The gate layout measured in most cases was of "gate on" type. "Gate on" refers to how the side connection to the superlattice is made. In this type of device "on" means that the connection came up onto the top of the channel for a distance of 10 microns across the channel (this was shown in fig 5.3). Other gate types referred to as "gate off" devices were also measured. Here the gate connection was made off the channel and only the strips of the gate are present on the channel; this device is shown in Fig 5.10(a). Gate-off devices gave poorer results on A648 and A909 devices, probably due to breaks in the gate strips as they rise up to the channel height from the etched area. For comparison purposes, devices were fabricated on A648 with other designs of gates. One pattern was fabricated in the same position as a finger superlattice but consisted of a continuous gate covering all the channel apart from a 10 μm uncovered

strip down one side. This is referred to as a 'partial' gate and is shown in fig 5.10(b). Another design of gate completely covered the channel and had the same length as in Fig 5.10 (a) and 5.10 (b). This is referred to as a 'big-gate' and is shown in fig. 5.10 (c)

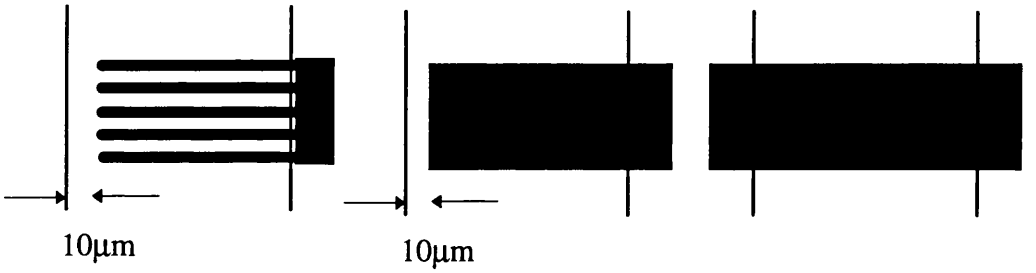


Fig 5.10(a)
'Gate-off' device

Fig 5.10(b)
'Partial' gate device

Fig 5.10(c)
'Big-gate' device

Fig 5.10 Detail of Hall-bar channel with variations in gate configurations referred to in the text

The devices were fabricated using different Hall-bar designs. A909 and A648 were fabricated using Hall-bar D. (See chapter 2, Fig 2.5 for Hall-bar types). Each Hall-bar had two areas where a gate structure could be measured. These designs also had three Hall-bars per alignment mark, allowing a total of 6 options for different types of gates. On these devices the fingers were 50nm thick NiCr and the connecting gate was 27 nm Ti/Au. The B591 devices were fabricated using Hall-bar C. The channel width was 200 μm, but there was only one gate per Hall-bar. Two Hall-bars were fabricated side by side with one being a gate-on device and the other a gate-off. Here the fingers and connecting gate were 50nm thick NiCr evaporated at the same time. The gate connection contact to the thick gold pad was 27nm Ti/Au.

The finger dimensions in all cases were designed to be 1 μm wide with a 2 μm period giving a 1:1 mark:space ratio. A summary of the gate structures measured is shown below in table 5.2.

Device number	Gate type	Gate width (μm)	Gate(finger) length (μm)	Gate Area ($\times 10^{-9}$ m^2)
A909 #1,2	on	220	190	22.0
B591 #1,2,4,5	on off	180 180	190 190	18.0 17.1
A648 #2,3	on	220	190	22.0
#4	partial big	220 220	190 200	41.8 44.0

Table 5.2 Table showing critical dimensions of gate structures measured. 'Gate length' and 'gate width' are defined in fig.5.3

5.3 Measurements.

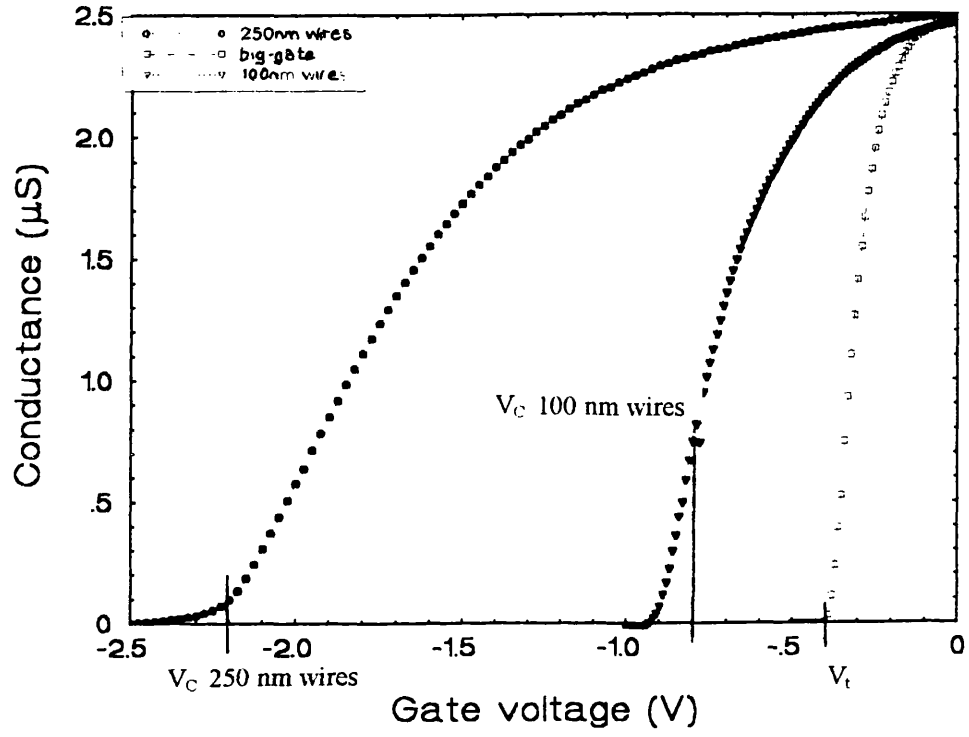
5.3.1 Experiments with HRN longitudinal wire devices.

5.3.1.1 Measurement of A707 devices.

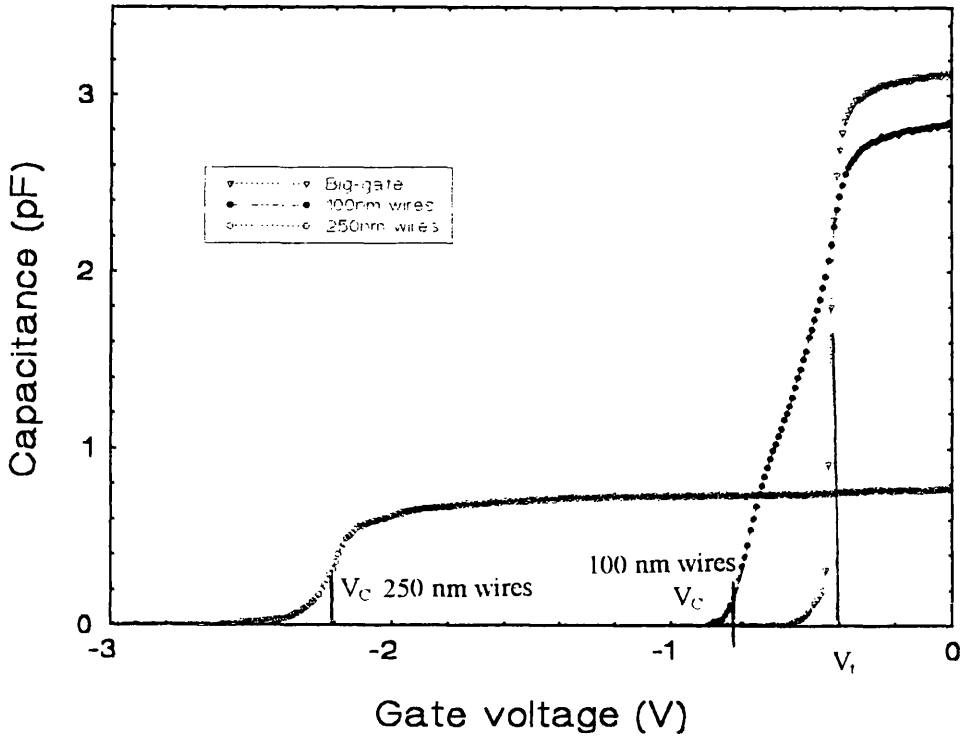
Three devices labelled #1,2,3 were measured from this chip. All three consisted of three gates in a row on the same type A Hall-bar (Hall-bar types are shown in chapter 2. This particular design used 100 μm channel width). The dimensions of the gates and wires are shown in table 5.1. The magneto-resistances of devices #1 and #3 were measured on the VTI rod at 1.5 K, the zero field resistance of #2 was also measured. The capacitances of devices #1 and #2 were measured in the closed circuit system at 20 K. The capacitance of device #3 was studied at 77 K. The distance between voltage probes (that is one pair on either side of the gate) for these devices was 90 μm and resistance between voltage probes of about 70 Ω giving a typical low temperature mobility at 1.5 K of 14 $m^2V^{-1}s^{-1}$.

a) Cut-off voltages.

Threshold voltages were obtained from the capacitance and from conductance measurements as a function of gate voltage. Graph 5.1 shows the conductance measurements, and 5.2 shows the capacitance measurements for device A707#1. Table 5.3 shows the comparisons of cut-off voltages for the three devices (taken from the capacitance measurements) with the pinned and frozen theories for a superlattice. To predict the cut-off voltage, the carrier concentration must be used. In all calculations of V_c for the three devices measured, the carrier concentration used was that obtained from the low temperature SdH measurements. The SdH carrier concentration was found to give the least error, estimated at not more than $\pm 0.1 \times 10^{15}$ m^{-2}.



Graph 5.1 conductance measurements of A707#1



Graph 5.2 capacitance measurements of A707#1

Device A707	Gate	Carrier concentration ($\times 10^{15}$) m^{-2} $\pm 0.1 \times 10^{15}$ m^{-2}	Measured [V]		Theoretical [V]		
			V_t ±0.02	V_c ±0.05	V_t ±0.01	$V_c^{(P)}$ ±0.01	$V_c^{(F)}$ ±0.01
#1	Big-gate	5.6	-0.42		-0.30		
	100nm wires	5.8	-0.42	-0.80	-0.31	-1.03	-0.55
	250nm wires	5.7	-	-2.20	-0.31	-2.22	-1.26
#2	Big-gate	5.7	-0.80		-0.31		
	100nm wires	5.7	-0.80	-1.00	-0.31	-1.03	-0.55
	250nm wires	5.7	-0.40	-2.00	-0.31	-2.22	-1.26
#3	Big-gate	5.6	-0.60		-0.30		
	100nm wires	5.6	-0.70	-1.10	-0.30	-0.99	-0.53
	250nm wires	5.6	-	-1.70	-0.30	-2.15	-1.22

Table 5.3. Comparison of measured and theoretical cut-off voltages. The estimated positions of V_c and V_t are shown in fig 5.7.
Ideally the estimates of voltage were taken at a position half way down the slope associated with that cuf-off voltage. As in fig 5.1 100 nm wires. When this was not clear (as in fig 5.1 250 nm wires data) the estimate was taken at the bottom of the slope associated with that voltage.

b) Capacitance measurements.

Measurements for A707#1 are shown in graph 5.2. The magnitudes of the capacitance compared to theory at zero gate bias using equation 5.9, and the calculations of carrier density obtained by integrating the area under the capacitance curves (measured at ~17 K), compared to those measured using the SdH measurements (measured at ~1.5 K), are shown below in table 5.4.

Device A707	Measured Capacitance pF ±0.1pF	Theoretical Capacitance pF ±0.1pF	Capacitance Carrier Density ($\times 10^{15}$) m^{-2} $\pm 0.2 \times 10^{15}$ m^{-2}	SdH Carrier Density ($\times 10^{15}$) m^{-2} $\pm 0.1 \times 10^{15}$ m^{-2}
#1				
100nm	2.9	6.3	5.0	5.8
250nm	0.8	6.3	5.0	5.7
Big-gate	3.1	6.3	4.2	5.6
#2				
100nm	1.9	6.3	5.4	-
250nm	1.8	6.3	7.9	-
Big-gate	2.4	6.3	9.8	-
#3				
100nm	2.3	6.3	5.0	5.6
250nm	1.1	6.3	5.0	5.6
Big-gate	3.0	6.3	5.2	5.6

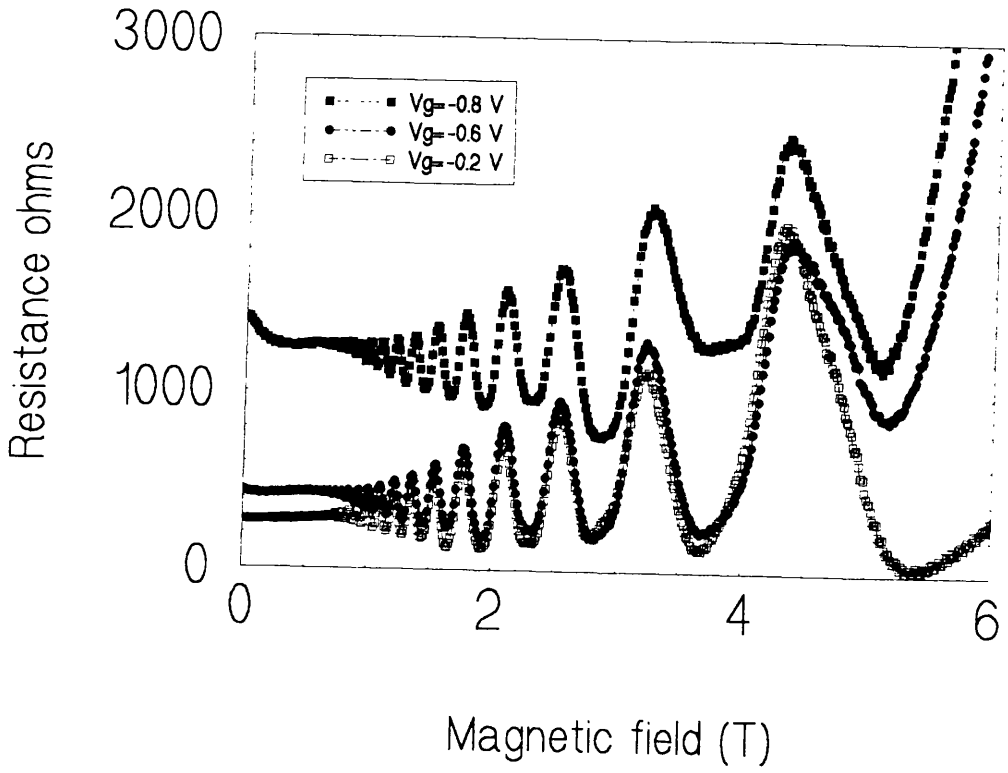
Table 5.4 comparison of measured and theoretical capacitance plus comparisons of carrier density obtained from SdH and capacitance measurements.

The comparison of carrier densities from measurements taken at different temperatures in table 5.4 is valid, because the measurements are all made below the DX freezing temperature (150 K).

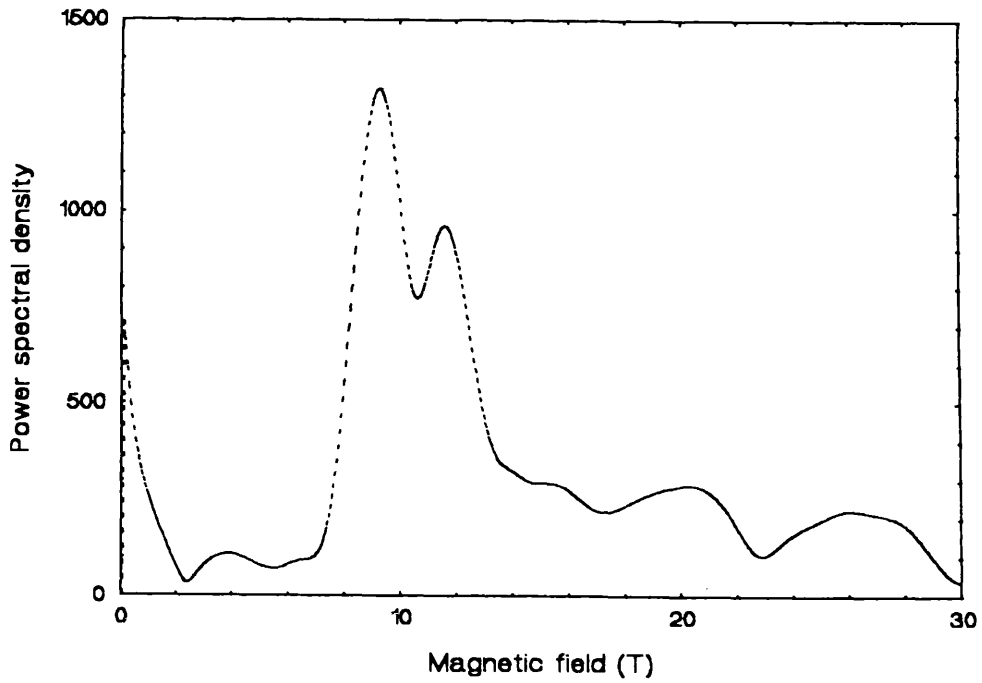
c) Magneto-resistance measurements.

Shubnikov de Haas Measurements

Devices A707#1 and A707#3 were measured on the VTI for different gate biases and varying magnetic field. Graph 5.3 shows a series of SdH measurements for 250 nm wires on device A707#1. Graph 5.4 shows a Fourier transform of a SdH measurement of 250 nm wires on A707#1 with a gate bias of V_g=-0.6 V. The Fourier transform shows two main peaks which correspond to the gated and the ungated areas. The lower of these peaks can be used to give an estimate of carrier concentration under the gated region. These values will be used together with the Haug measurements to see how the carrier concentration is being depleted under the gate.



Graph 5.3 SdH measurements of 250 nm sample A707/1



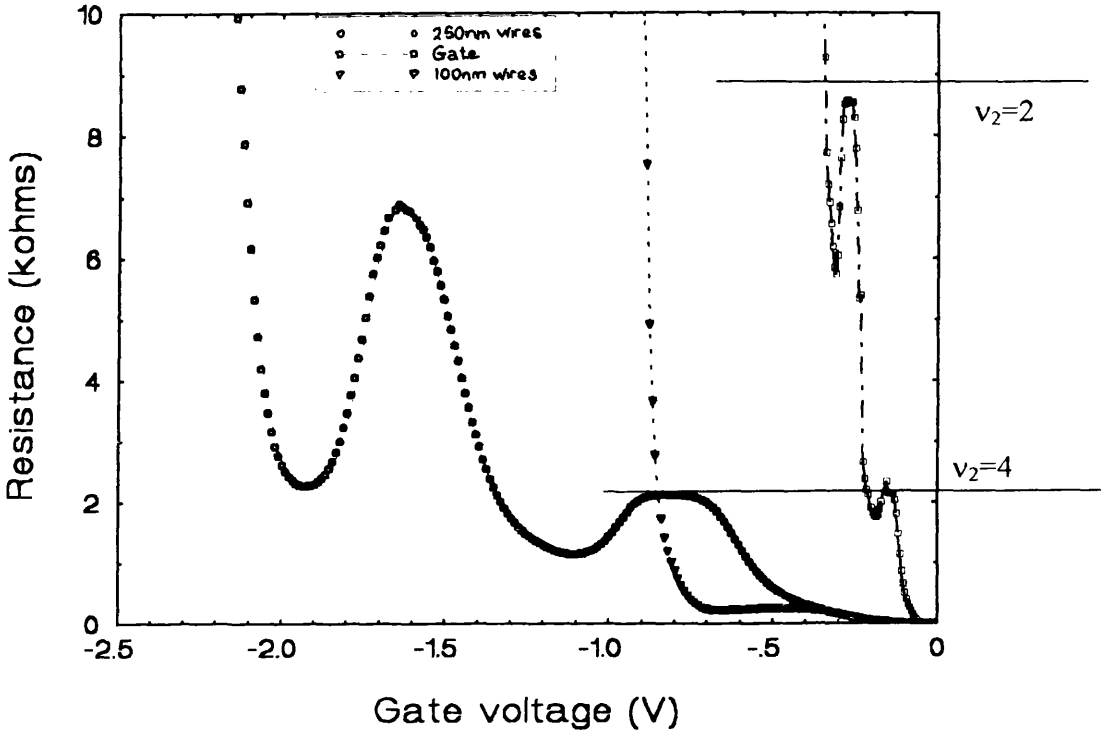
Graph 5.4. FT of 250 nm wires A707#1 with Vg=-0.6 V

d) Haug measurements.

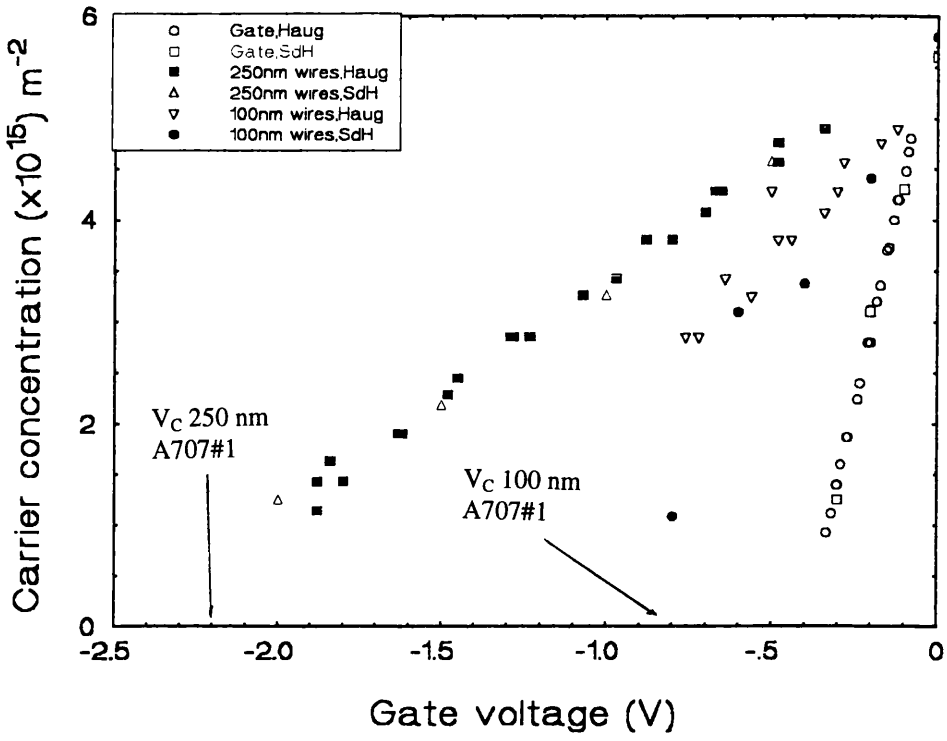
Devices A707#1 and A707#3 were measured using the Haug technique. Haug measurements for the three gates on A707#1 are shown in graph 5.5. Theoretical values of R_L from (5.8) are indicated, which correspond to the Landau levels $N_w = 3$, $N_g = 2$ and $N_w = 3$, $N_g = 1$. The positions of the plateaus are used to estimate the carrier concentration as a function of gate bias. A plot of the carrier concentrations vs. gate bias is shown in Graphs 5.6 for devices A707#1 and A707#3. The majority of the data comes from the Haug measurements, but some points obtained from the Fourier transforms of the SdH plots are also added. Graphs 5.6 shows that there is good agreement between the carrier concentration calculated from the Haug and SdH measurements. Big-gate and 250 nm wires data decrease linearly up to the cut-off voltage. The 100 nm data, particularily for A707#1, behaves differently. The carrier concentration decreases with bias towards a point more negative than the observed cut-off voltage. However before that point is reached there is a sharp decrease to zero carrier concentration at the cut-off voltage.

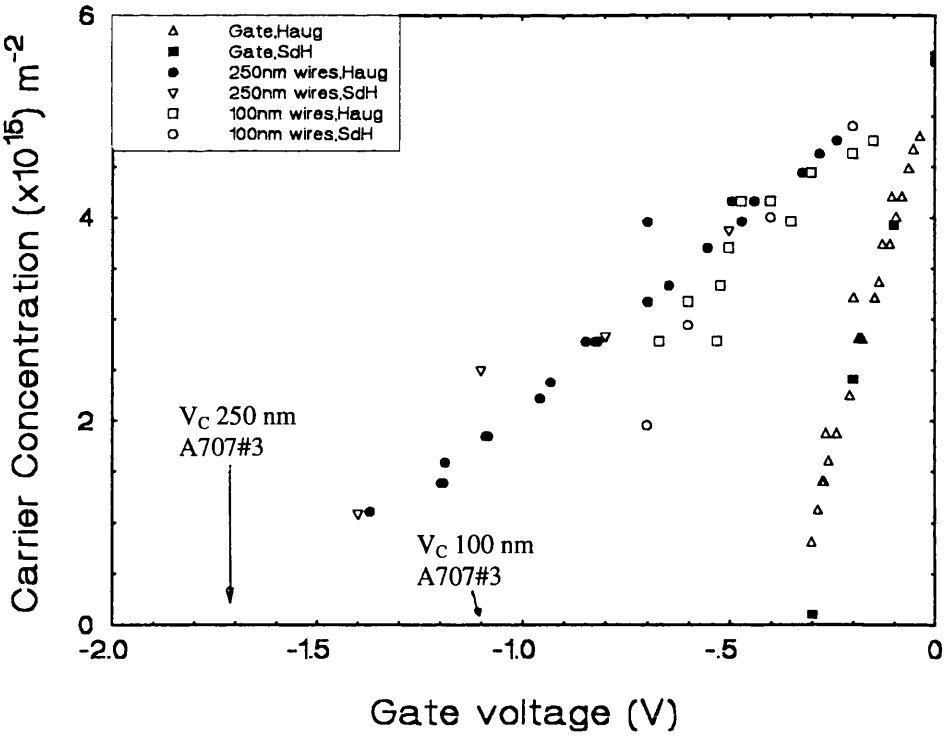
5.3.1.2 Measurements of the A866 device.

One device was measured, device #2. It consisted of two type C Hall-bars side by side on the same chip (one wire device, one gate device). The dimensions of the gate and wires are shown in table 5.1. These Hall-bars were fabricated at the same time and cooled at the same time, under the same conditions. The Hall-bars were 200 μm wide with a distance between voltage probes of 300 μm, giving a resistance of 260 Ω. This leads to a mobility at low temperatures (1.5 K) of about 8.5 $m^2V^{-1}s^{-1}$ for these devices, which is rather low, even compared with the other devices measured, probably because this layer was grown towards the end of a cycle before the MBE system was cleaned.



Graph 5.5 Haug measurements for A707#1 B=3.6 T





Graphs 5.6. Carrier conentrations with bias for A707#1 (top) and A707#3 (bottom)

a) Cut-off voltages.

Cut-off voltages were obtained from conductance-gate voltage measurements, as shown in Graph 5.7. On this device there is clear evidence of a shoulder on the wire data; and the formation voltage of the wire can be seen at the point at which the big-gate cuts off, at about -0.27 V, indicating that electrons are being squeezed into wires. The theoretical and measured cut-off voltages are shown in Table 5.5. The carrier concentration values are those obtained from SdH measurements.

Device A866	Gate	Carrier concentration ($\times 10^{15}$) m^{-2} $\pm 0.1\times 10^{15}$ m^{-2}	Measured [V]		Theoretical [V]		
			V_t ± 0.01	V_c ± 0.05	V_t ± 0.01	$V_c^{(P)}$ ± 0.01	$V_c^{(F)}$ ± 0.01
#2	200nm wires (2μm period)	4.3	-0.27	-0.38	-0.22	-1.29	-0.65
	Big-gate	4.4	-0.27	-	-0.23	-	-

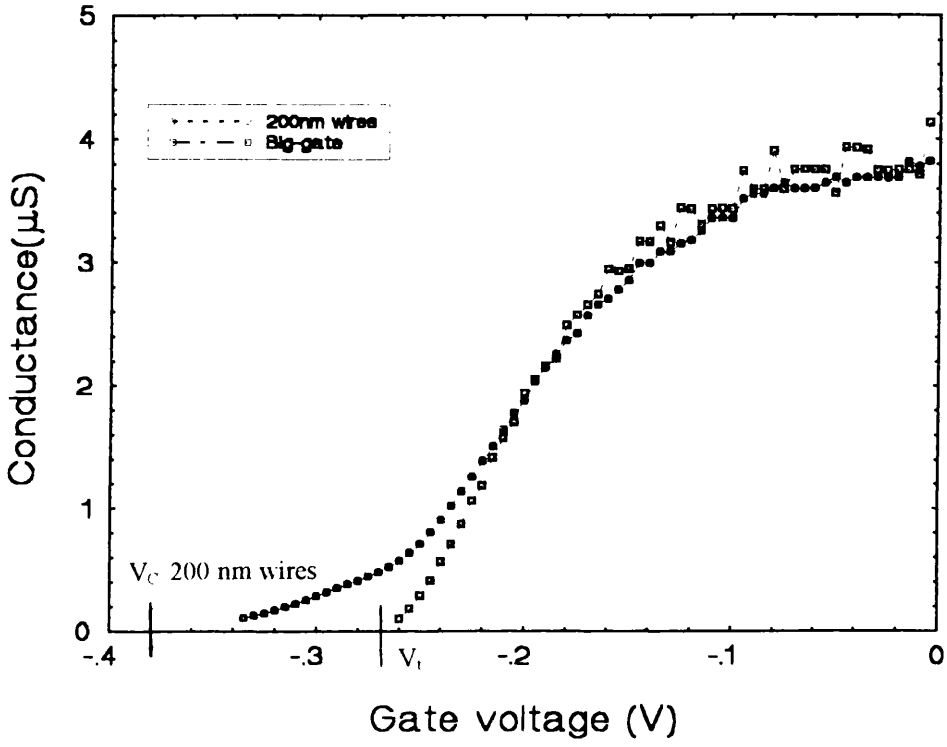
Table 5.5 Comparison of measured and theoretical cut-offs for the A866 device. The positions of estimate of V_c and V_t are shown in fig 5.7.

b) Shubnikov de Haas measurements.

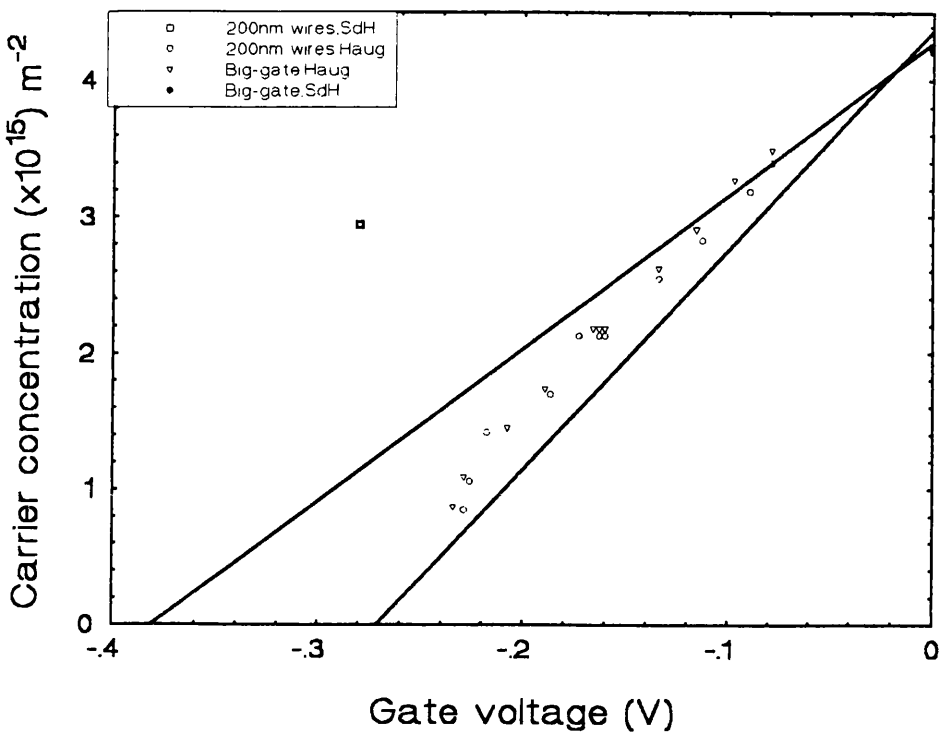
SdH measurements were made for zero bias on both gates of A866#2. In addition a SdH sweep was made in a region of interest past the gate cut-off voltage at -0.28 V to get an estimate of the carrier concentration in this region. The carrier concentrations obtained are shown in graph 5.8.

c) Haug measurements.

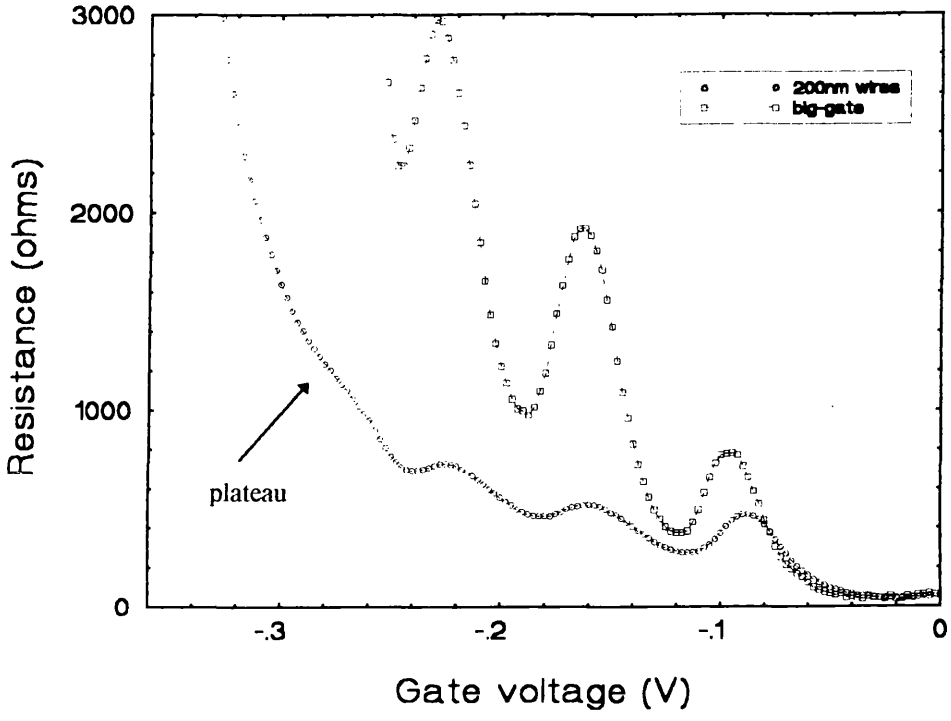
A866#2 carrier concentration data obtained from Haug measurements are plotted in graph 5.8. Here the Haug carrier concentration data is similar for the big-gate and the wire. The carrier concentration under the area of gate on GaAs (between the HRN ribs) and the big-gate depletes in a similar way. Of interest in the Haug data for the A866#2 wire is that there is evidence of structure past the gate cut-off. A curve is shown for B=2.2 T in graph 5.9.



Graph 5.7 conductance data for A866#2



Graph 5.8. Carrier concentration for A866#2 with bias. The solid lines are a guide to the eye. They are drawn between the zero bias carrier concentration for the two devices and the threshold and cut-off voltages.



Graph 5.9 Haug data for A866#2

5.3.1.3 Measurement of A909 devices.

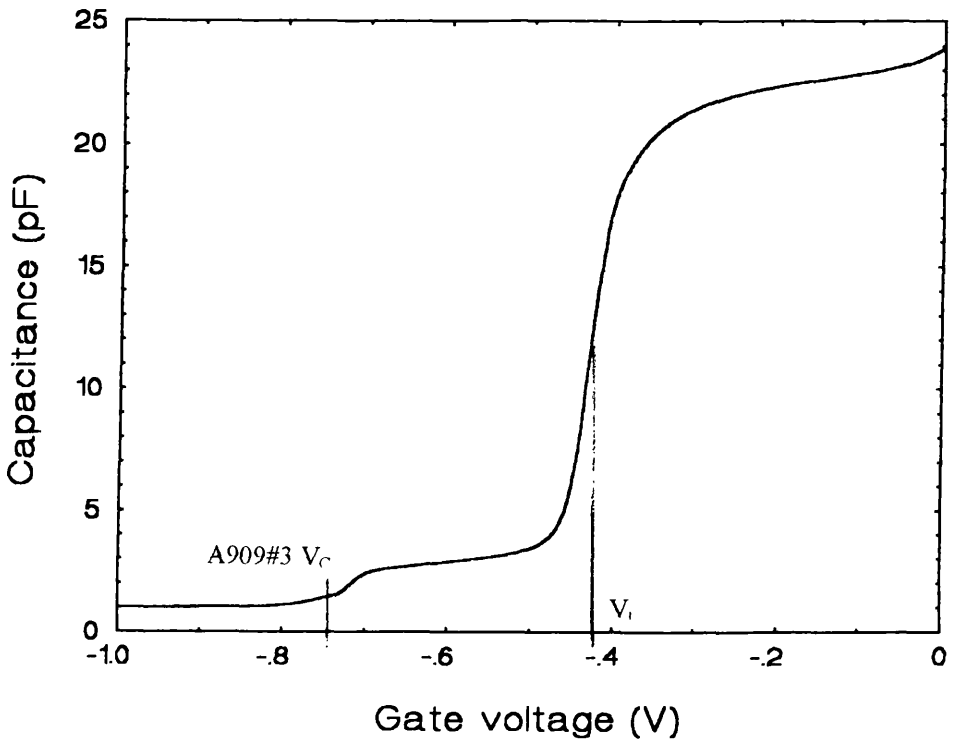
Two devices were measured from this chip labelled #2,3. These devices consisted of two gates on the same type D Hall-bar. Gate and wire dimensions are shown in table 5.1. The magneto-resistance of device #2 was measured on the VTI. Capacitance and magneto-capacitance of this device, and of device #3, were also studied on the VTI capacitance rod. The distance between voltage probes for these devices was 300 μm and resistance between voltage probes of 138 Ω giving a low temperature (1.5 K) mobility of 13.2 $m^2V^{-1}s^{-1}$.

a) Cut-off voltages

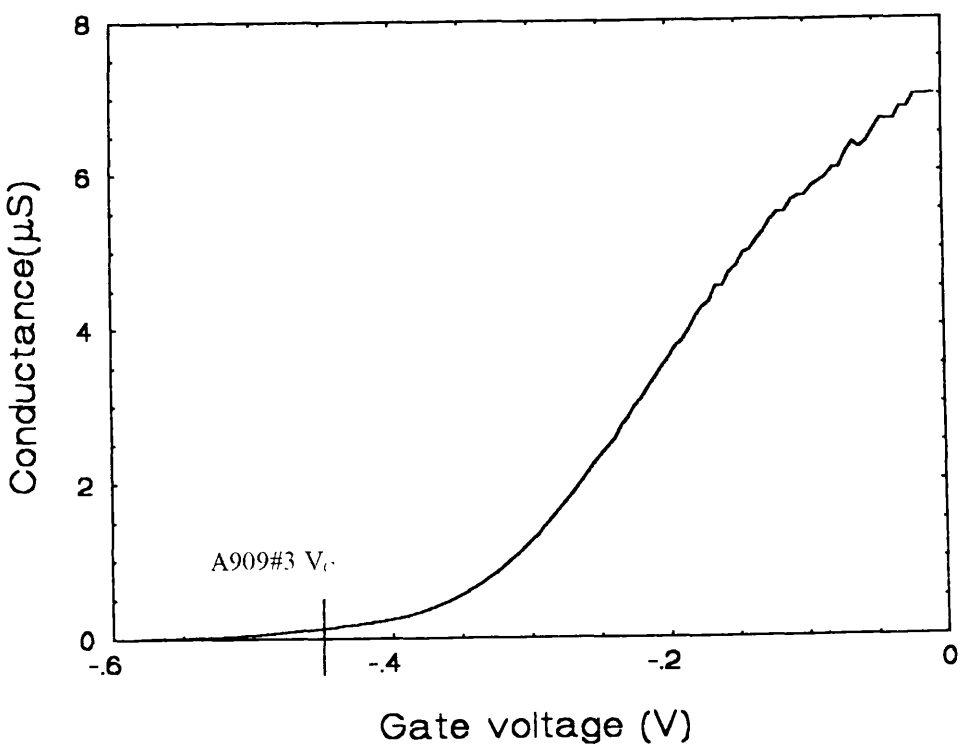
Threshold voltages were obtained from the capacitance measurements. Graph 5.10 shows a capacitance measurement and graph 5.11 shows a conductance measurement for device #3. Table 5.6 shows a summary of the theoretical and measured cut-off voltages for these devices. The carrier concentrations were obtained from the SdH measurements at low temperatures.

Device A909	Gate	Carrier concentration ($\times 10^{15}$) m^{-2} $\pm 0.1\times 10^{15}$ m^{-2}	Measured [V]		Theoretical [V]		
			V_t ±0.02	V_c ±0.02	V_t ±0.01	$V_c^{(P)}$ ±0.01	$V_c^{(F)}$ ±0.01
#2	200nm wires	5.3	-1.35	-1.50	-0.27	-1.58	-0.80
	Big-gate	5.4	-0.40	-	-0.28	-	-
#3	200nm wires	5.2	-0.43	-0.75	-0.27	-1.58	-0.80

Table 5.6. Theoretical and measured cut-off voltages for A909 samples. The positions of V_c and V_t are shown in fig 5.7.



Graph 5.10. Capacitance measurement of A909#3



Graph 5.11. A909#3conductance measurement.

b) Shubnikov de Haas measurements.

Devices #2 and 3 were measured on the VTI and the carrier concentrations were obtained from SdH and Haug measurements. These are shown in Graph 5.12 for both wire and gate devices.

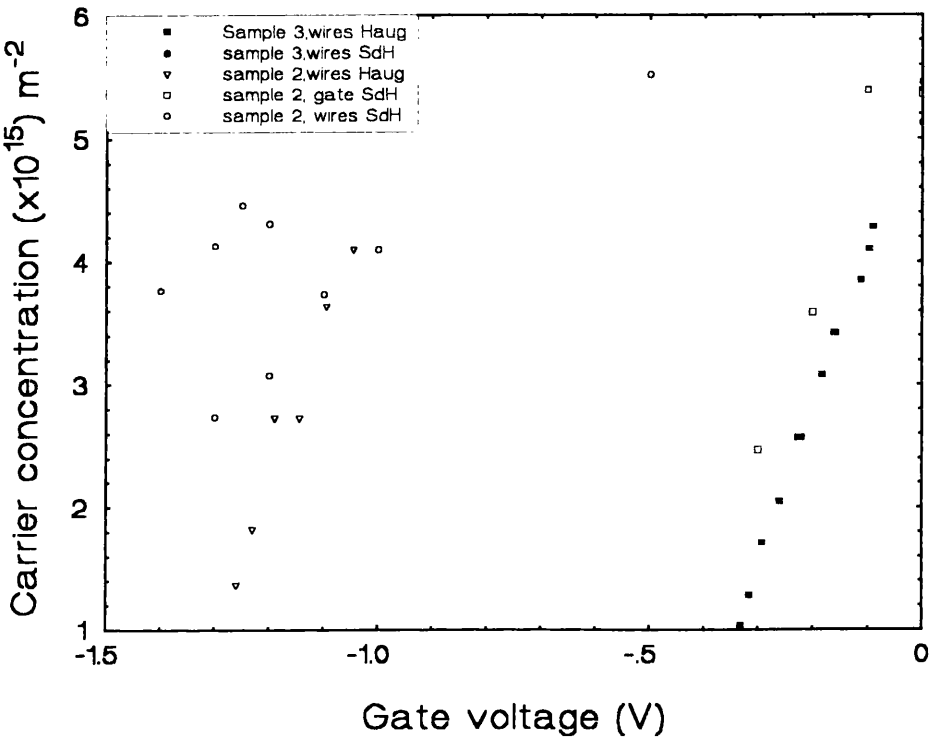
c) Capacitance measurements

Capacitance-voltage studies were made of a longitudinal wires device (device #3) and a big-gate device (device #2). The measurement for the wire device was shown in graph 5.10.

The magnitudes of the capacitance compared to theory at zero gate bias using (5.10) are shown in table 5.7. Also shown are the calculations of carrier density obtained by integrating the area under the capacitance curves (measured at ~17 K), compared to the values obtained using the SdH measurements (measured at ~1.5 K).

Device A909	Measured Capacitance pF ±0.2pF	Theoretical Capacitance pF ±0.6pF	Capacitance Carrier Density ($\times 10^{15}$) m^{-2} $\pm 0.2 \times 10^{15}$ m^{-2}	SdH Carrier Density ($\times 10^{15}$) m^{-2} $\pm 0.1 \times 10^{15}$ m^{-2}
#3 200nm wires	23.9	31.3	6.1	5.2
#2 Big-gate	28.7	31.3	6.5	5.4

Table 5.7 comparison of measured and theoretical capacitance plus comparisons of carrier density obtained from SdH and capacitance measurements.



Graph 5.12. Carrier concentrations for A909#3. When formed, the wire regions in device 3 are too narrow for the edge state transport to be apparent.

d) Magneto-capacitance measurements.

The wire gate on device #3 and the big-gate on device #2 were measured on the capacitance VTI rod. Measurements of capacitance against magnetic field at given gate voltage (analogous to SdH measurements) for device 3 are shown in graph 5.13. Measurements of capacitance against gate voltage at given fields (analogous to Haug measurements) are shown in graph 5.14.

5.3.2 Experiments with side gated superlattice devices.

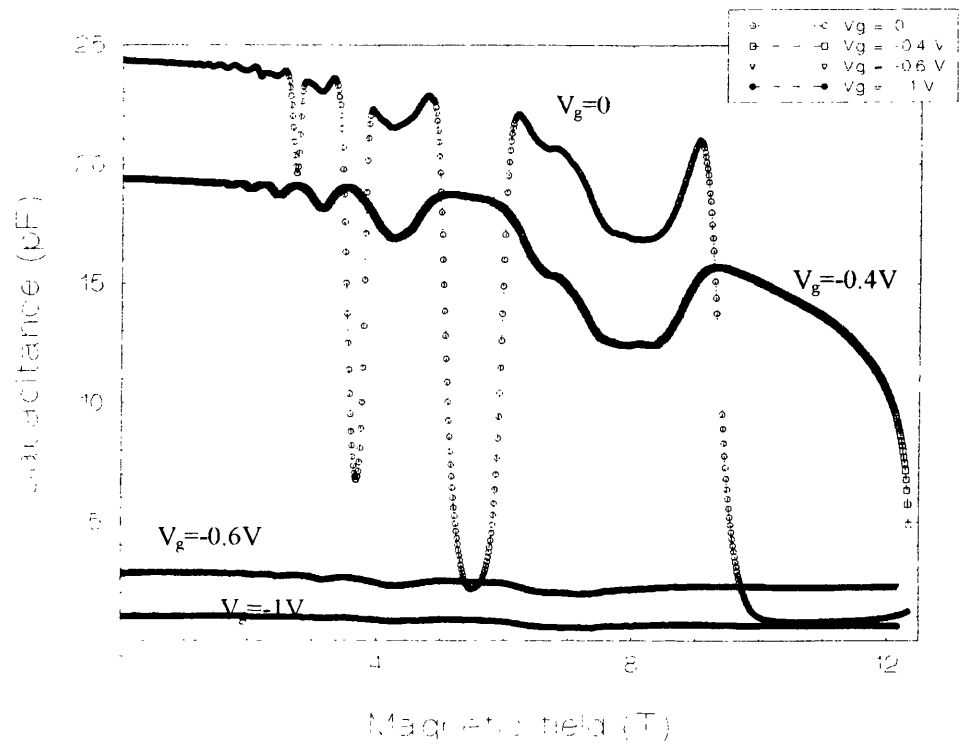
5.3.2.1 Measurements of the A909 devices.

Two devices labelled #1 and #2 were measured from different Hall-bars. The devices were fabricated at the same time on the same piece of material.

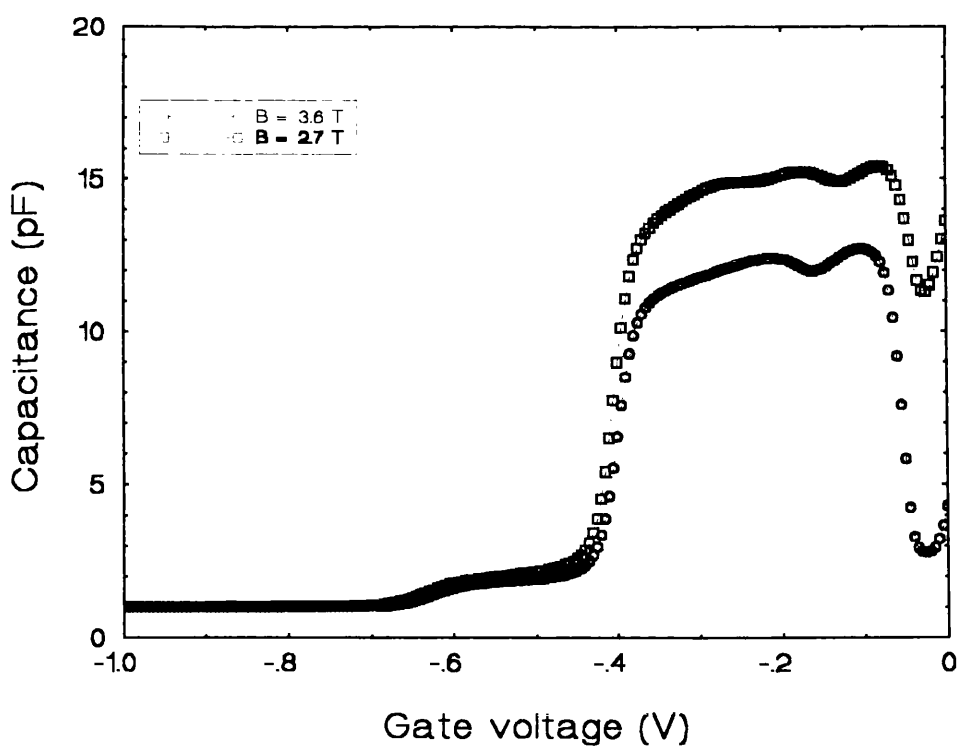
The gates that gave the most consistent results (with each other and between repeated gate measurements) were the gate-on devices and data will be presented from experiments on these devices. Gate-off devices gave poor results which are thought to be due to broken gate connections where the strips step over the edge created by the etch process defining the channel. All experiments were carried out at 1.5K on either the capacitance or the resistance VTI rods. The distance between voltage probes was 300 μm for these devices giving a resistance of 180 Ω and a mobility of 9.5 $m^2V^{-1}s^{-1}$ at a measurement temperature of 1.5 K.

a) Capacitance measurements

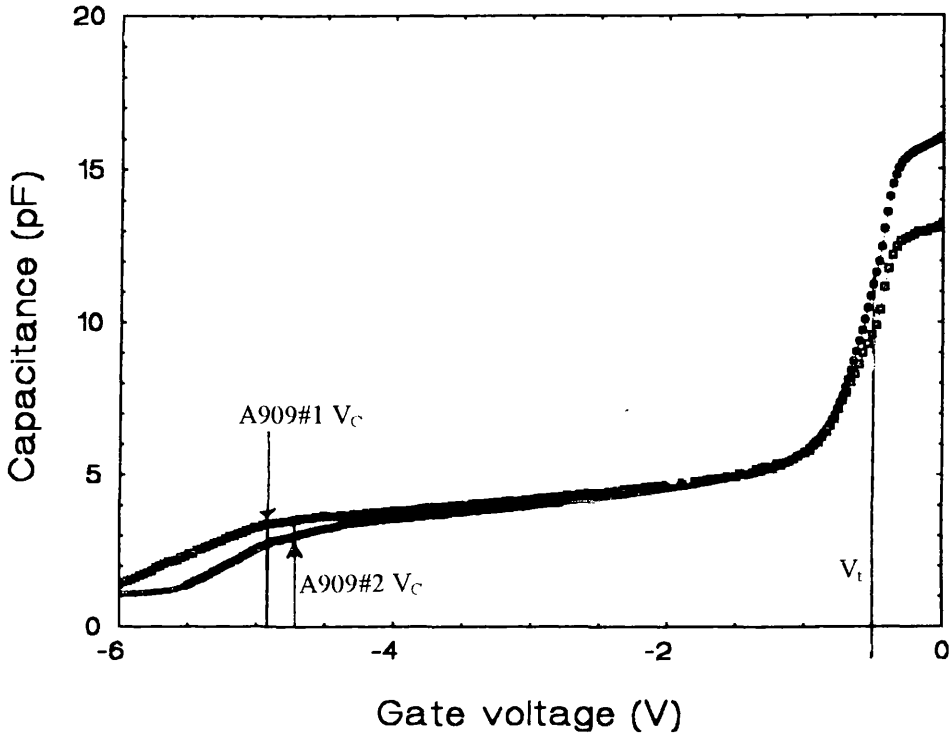
Measurements of capacitance as a function of gate bias for the two devices are shown in graph 5.15. The graphs show the capacitance starting at a high value (which should be comparable to the geometric one obtained from equation 5.9), then dropping rapidly to a point defined by a bias voltage, V_t. The capacitance then decreases at a slower rate until it reaches a point near V_c when it falls more rapidly to a background capacitance defined by the capacitance of connections and leads to the device.



Graph 5.13 Magneto-capacitance data for A909#3



Graph 5.14. Measurement of capacitance with magnetic field held at a fixed value for A909#3



Graph 5.15 A909 Capacitance measurements

Table 5.8 below summarises cut-off voltages obtained from measurements of capacitance for the two devices. The carrier concentration was obtained from the low temperature SdH measurements.

Device A909	Gate	Carrier concentration ($\times 10^{15}$) m^{-2} $\pm 0.1 \times 10^{15}$ m^{-2}	Measured [V]		Theoretical [V]		
			V_t ± 0.05	V_c ± 0.20	V_t ± 0.01	$V_c^{(P)}$ ± 0.01	$V_c^{(F)}$ ± 0.01
#1	gate on	5.5	-0.50	-4.93	-0.28	-7.80	-4.37
#2	gate on	5.3	-0.50	-4.70	-0.27	-7.51	-4.21

Table 5.8 Comparison of threshold and cut-off voltages using the pinned and frozen theories. The estimated positions of V_c and V_t are shown in graph 5.15.

The value of actual measured capacitance at zero bias ($C_m=C_0 - C_b$) can be compared to the capacitance obtained from equation 5.9 and the carrier concentration obtained from the SdH measurements can be compared to the carrier concentration obtained from the area under the curves (areas A+B in fig 5.8). These data are summarised in table 5.9 below.

Device A909	Measured Capacitance pF ± 0.2 pF	Theoretical Capacitance pF ± 2 pF	Capacitance Carrier density ($\times 10^{15}$) m^{-2} $\pm 0.2 \times 10^{15}$ m^{-2}	SdH Carrier density ($\times 10^{15}$) m^{-2} $\pm 0.1 \times 10^{15}$ m^{-2}
#1	13.2	68.8	1.5	5.5
#2	15.2	68.8	1.9	5.3

Table 5.9 Comparison of measured and theoretical capacitance, and carrier concentrations obtained from magneto-resistance and capacitance measurements.

b) Resistance and magneto-resistance measurements.

Both devices were measured on the resistance VTI to confirm threshold voltages (V_t) and for an estimate of carrier concentration from the SdH oscillations.

The resistance measurements show threshold voltages which are the same as the threshold voltages observed in the capacitance measurements (-0.5 V) . Graph 5.16 shows resistance as a function of gate bias for measurements from each side of the channel. The differences between the two measurements reflect the increased path that the electrons are forced to take around the gate when measured from the gate-on side above threshold. The gradual increase in resistance when the gate bias is made more negative than V_t is a result of the 10 μm channel shown in fig. 5.3 being squeezed.

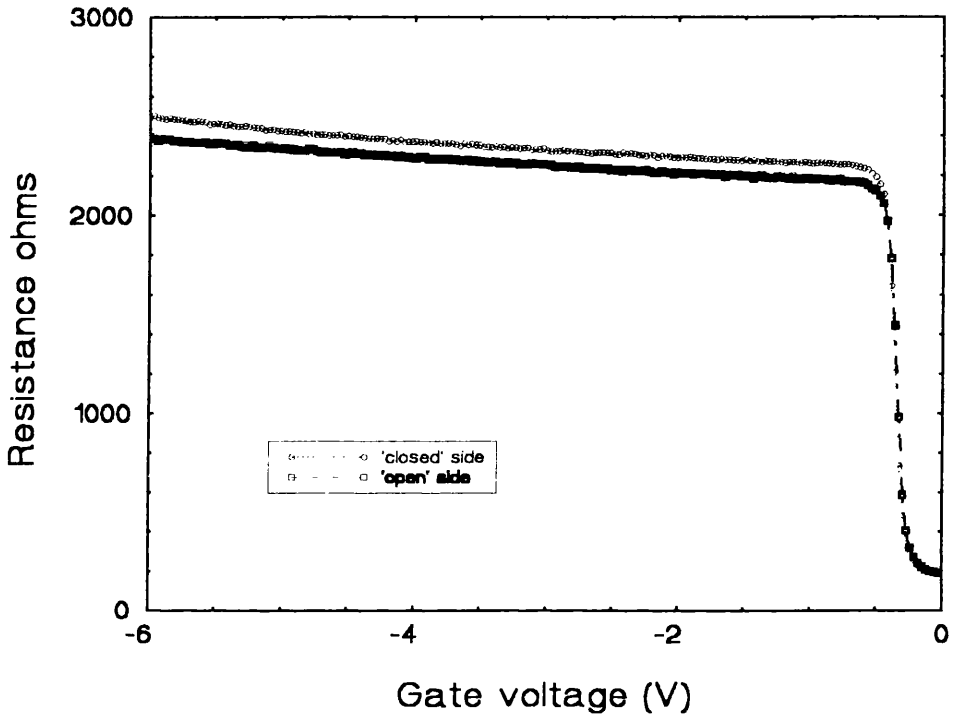
Graph 5.17 shows magneto-resistance measurements. These are used to find the zero bias carrier concentration.

5.3.2.2 Measurements of the B591 devices.

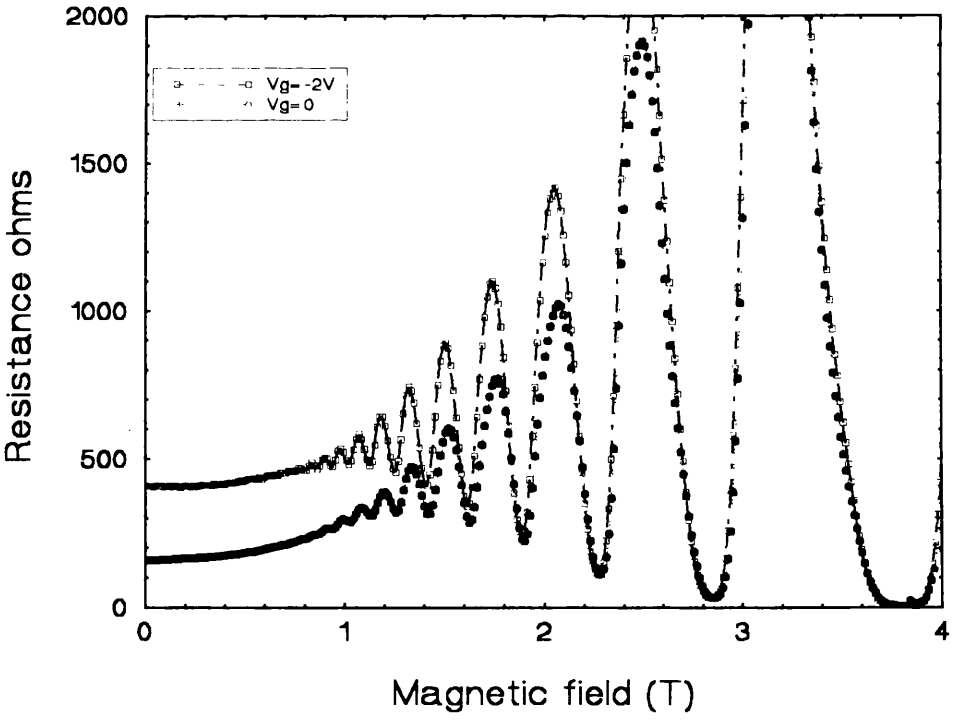
Four B591 devices were measured, labelled #1,2,4 and #5. Both gate-on and gate-off type gates were measured. Devices were measured in the closed circuit system at 20K and on the VTI resistance and capacitance rods at 1.5 K. From the magneto-resistance measurements it was found that the mobility of a typical device was 20 $m^2V^{-1}s^{-1}$ (a resistance of 200 Ω with voltage probes 300 μm apart at a measurement temperature of 1.5 K).

a) Capacitance measurements

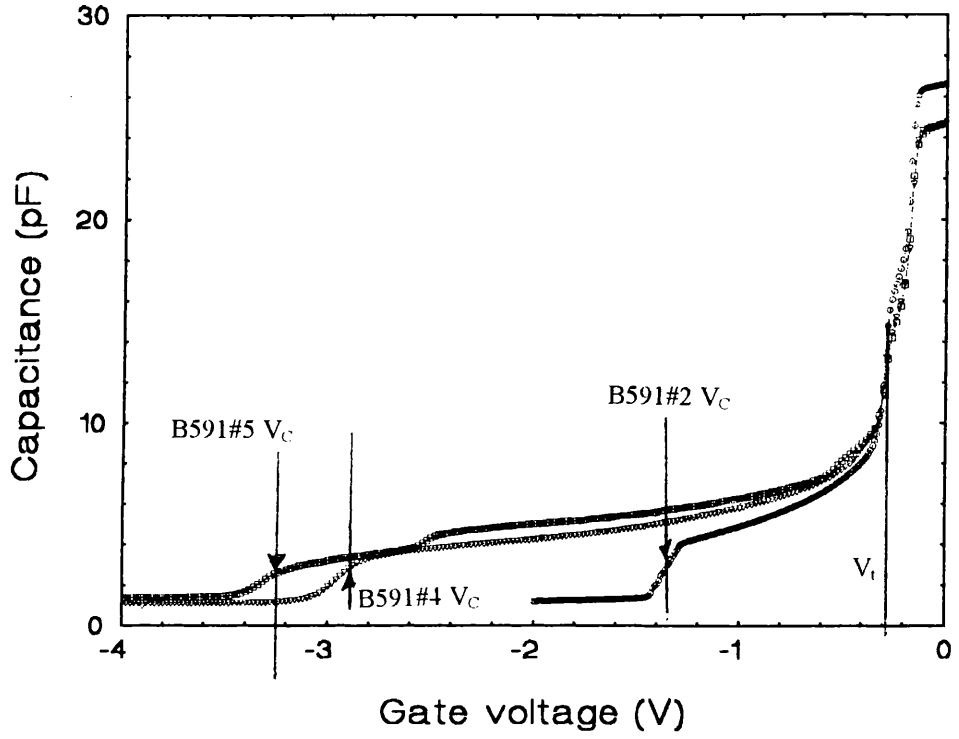
All four devices were measured on the closed circuit system at temperatures of about 20 K. Three devices, #2, 4 and 5, were measured on the capacitance VTI rod at 1.5 K. Typical measurements are shown in graph 5.18. The measurements are similar to those made on A909, with a rapidly decreasing capacitance at V_t and a more gently sloping decrease to V_c. However, whilst V_t is in good agreement for all devices, there is a considerable disparity between measured values of V_c for four devices, including a difference in the value derived from the C-V curve of device #2 measured at 1.5 K and



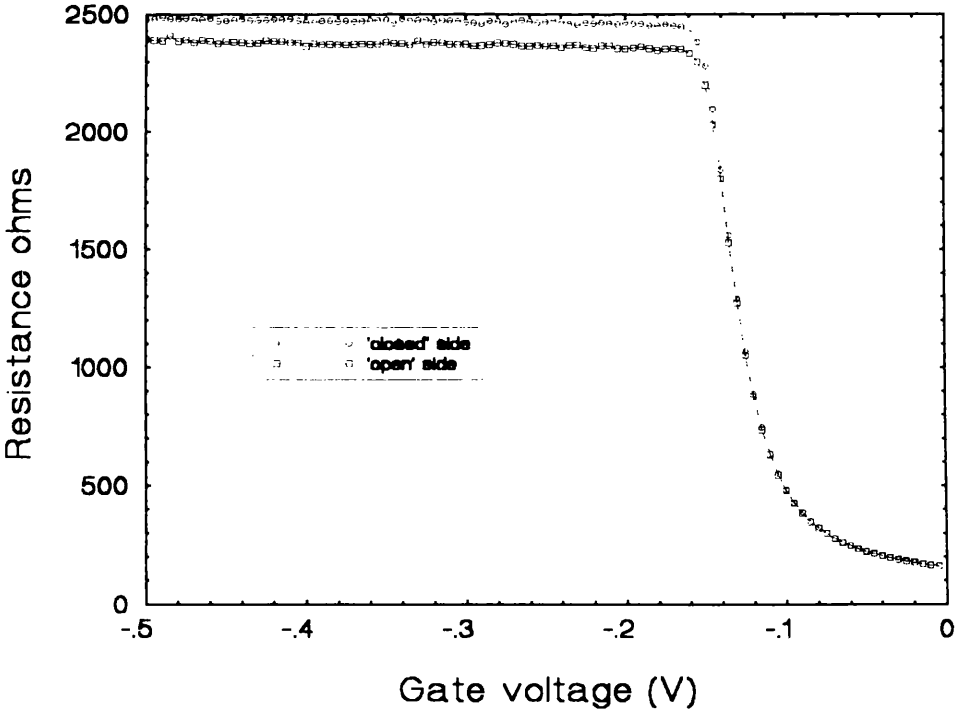
Graph 5.16. Resistance measurements on A909#2.



Graph 5.17. SdH measurements on A909#2



Graph 5.18 Capacitance measurements of B591 samples.



Graph 5.19 Resistance measurements of B591#2.

17 K. Also of note is one feature, common to all B591 devices but which was not observed on the A909 or A648 devices. This is the additional plateaux observed on the curves near V_t.

The cut-off and carrier concentrations from all measurements of the devices are summarised below in table 5.10.

Device B591	Gate	Carrier concentration ($\times 10^{15}$) m^{-2} $\pm 0.1 \times 10^{15} m^{-2}$	Measured [V]		Theoretical [V]		
			V_t ± 0.01	V_c ± 0.20	V_t ± 0.01	$V_c^{(P)}$ ± 0.01	$V_c^{(F)}$ ± 0.01
#1 (17K)	gate on		-0.25	-2.00			
#2 (18K)	gate on		-0.25	-0.84			
(18K)	gate off		-0.25	-1.62			
(1.7K)	gate on	2.7	-0.25	-1.35	-0.26	-3.98	-2.24
#4 (17K)	gate on		-0.25	-3.22			
(17K)	gate off		-0.25	-3.40			
(1.6K)	gate off	2.6	-0.25	-2.90	-0.25	-3.83	-2.15
#5 (17K)	gate on		-0.25	-2.26			
(17K)	gate off		-0.25	-3.25			
(1.5K)	gate off		-0.25	-3.20			

Table 5.10. Measured and theoretical cut-off and threshold voltages for B591 devices. The positions of estimate of V_c and V_t are shown in fig 5.8.

Table 5.11 shows the capacitance at zero bias compared the capacitance calculated from theory (using equation 5.10). Also shown is a comparison of carrier concentrations obtained using the area under the capacitance curves, compared to the SdH values for devices #2 and 4.

Device B591	Measured Capacitance pF	Theoretical Capacitance pF ± 1.2 pF	Capacitance Carrier density ($\times 10^{15}$) m^{-2} $\pm 0.2\times 10^{15}$ m^{-2}	SdH Carrier density ($\times 10^{15}$) m^{-2} $\pm 0.1\times 10^{15}$ m^{-2}
#1 gate on	25.0	30.1	1.8	
#2 gate on	25.2	30.1	2.0	2.7
gate off	23.9	28.6	1.8	
#4 gate on	25.1	30.1	1.8	
gate off	23.2	28.6	1.8	2.6
#5 gate on	24.9	30.1	1.9	
gate off	23.3	28.6	2.0	

Table 5.11. Comparison of theoretical and measured capacitance, and carrier concentration measured from the SdH and capacitance data.

b) Resistance and magneto-resistance measurements.

The resistance of device #2 (gate-on) was measured as a function of magnetic field and gate voltage on the resistance VTI rod. The threshold voltage from this measurement is shown in graph 5.19 and is smaller than that observed in the capacitance measurement (-0.16 V compared to -0.25 V). The magneto-resistance plots show an increase in resistance at zero magnetic field as the gate bias is made negative. The SdH oscillations in the magneto-resistance measurement are unaffected by gate bias and reflect the bulk device outside the gate.

5.3.2.3 Measurements of the A648 devices.

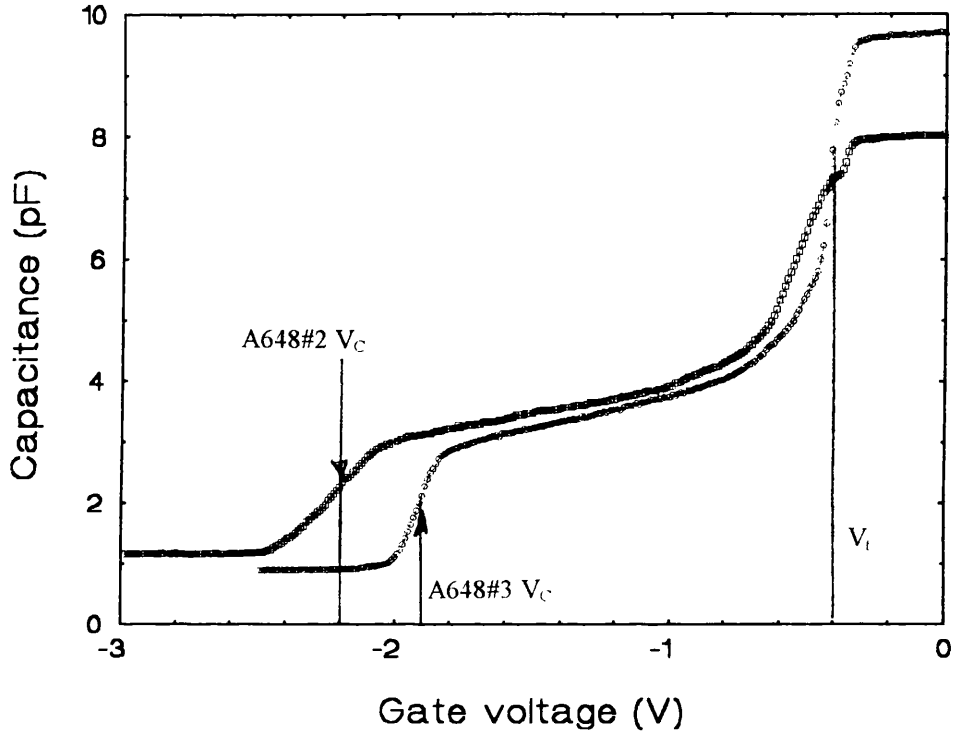
Two A648 gate-on devices labelled #2 and #3 were measured. In addition, a large gate device was measured, #4. This device had both a big-gate and a partial gate. Devices were measured on the VTI capacitance or resistance rods at 1.5 K. Using the carrier concentration from the SdH measurements, it was calculated that these devices had a mobility of 47 $m^2V^{-1}s^{-1}$ at 1.5 K. The voltage probes were 300 μm apart and at zero magnetic field, the resistance measured was 77Ω .

a) Capacitance measurements.

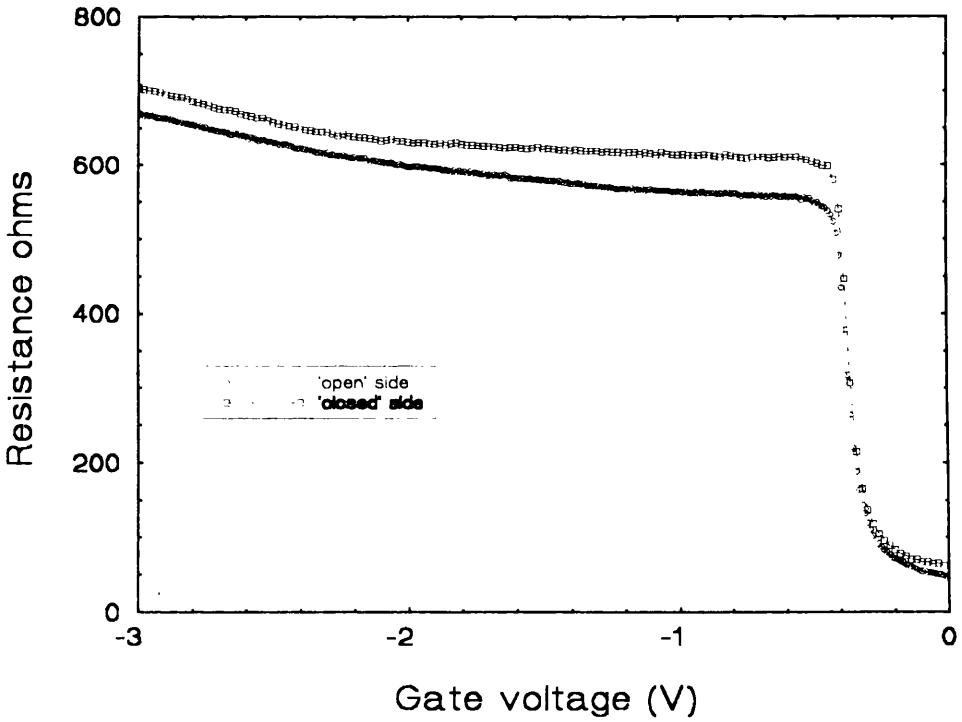
All three devices were measured on the VTI capacitance rod at 1.5 K. Graph 5.20 shows capacitance as a function of gate bias for the two A648 devices. The shape of the capacitance curves of the A648 devices is similar to the A909 devices, with a steep cut-off at V_t followed by a more gradual decrease in the capacitance until V_c is reached, when there is a sharp drop. The big-gate and partial gate showed only a sharp decrease in the capacitance at the cut-off voltage. The partial gate had a slightly larger magnitude of V_t. A summary of the results is shown below in table 5.12.

Device A648	Gate	Carrier concentration ($\times10^{15}$) m^{-2} $\pm0.1\times10^{15}m^{-2}$	Measured [V]		Theoretical [V]		
			V_t $\pm$ 0.05	V_c $\pm$ 0.2	V_t ±0.02	$V_c^{(P)}$ ±0.02	$V_c^{(F)}$ ±0.02
#2	gate on	2.5	-0.40	-2.20	-0.37	-3.60	-2.04
#3	gate on		-0.40	-1.90			
#4	big-gate partial		-0.40 -0.45				

Table 5.12. Comparison of measured and theoretical cut-off and threshold voltages for A648 (deep) devices.



Graph 5.20. Capacitance measurements on A648.



Graph 5.21 Resistance measurements on A648#2.

Table 5.13 shows comparisons of measured and theoretical capacitances together with comparisons of the charge densities obtained from the area under the capacitance curve and from the SdH measurement.

Device A648	Measured Capacitance pF ±0.5pF	Theoretical Capacitance pF ± 1pF	Capacitance Carrier density ($\times 10^{15}$) m^{-2} $\pm 0.2\times 10^{15} m^{-2}$	SdH Carrier density ($\times 10^{15}$) m^{-2} $\pm 0.1\times 10^{15} m^{-2}$
#2 gate on	9.0	24.1	2.1	2.5
#3 gate on	6.8	24.1	2.2	
#4 big-gate partial	41.4 39.1	48.1 45.7	2.3 2.3	

Table 5.13. Comparison of measured and theoretical capacitances, and comparison of carrier concentrations obtained using SdH data and capacitance data.

b) Resistance and magneto-resistance measurements.

The resistance of device #2 was measured as a function of gate voltage and magnetic field on the resistance VTI at 1.5 K. The resistance measurements are shown in graph 5.21. Magneto-resistance measurements were made which enabled a calculation of zero gate bias carrier concentration to be deduced.

5.4 Summary and discussion

5.4.1 Summary and discussion of HRN longitudinal wire data.

5.4.1.1 Introduction

Three devices were measured with different gate geometries. All three layers were of a similar type, shallow AlGaAs material with the interface 28 nm from the surface. The first layer measured was A707, this had less doping than A866 or A909 but the highest mobility. The next devices were on the an A866 layer which had the poorest mobility. Two Hall-bars were measured, one with gate on HRN ribs and another control device with the same overall dimensions but with no HRN ribs. The final devices that were measured were A909 #2 and #3. A909 was a wide channel device with the channel width 200 μm and with a mobility less than that of A707 but greater than that of the A866 devices.

5.4.1.2 Cut-off voltages.

It was expected that, by comparing the cut-off voltages to those predicted by the pinned and frozen models, it would be possible to differentiate clearly between the two. From the data, it was hoped to see a formation voltage similar to the cut-off voltage for the big-gate, and comparable to the theoretical cut-off obtained from either equation (5.6) or (5.7). The measured values of V_t were in reasonable agreement with the theoretical values, taking into consideration that the model was developed for deep bulk materials, and the values are also in good agreement with other big-gate experimental results measured using devices fabricated on shallow materials grown in Glasgow [22].

The measured cut-off voltages, V_c were also compared to the calculated values from the two models. For A707 devices, the measured V_c values lie in a range from mid-way between the two models tending towards the pinned values. A866 and A909

devices showed better agreement with the frozen model. A909 #2 was an exception showing larger values of both V_t and V_c than predicted by the theoretical models.
The results are ambiguous and do not seem to support either the pinned or the frozen models, but there are complicating factors. The first is that there must be some effect of the gate on top of the resist. This will lead to the V_c measured being less than expected due to the depletion of the electrons in the wire areas. This may also be partly to blame for the non-formation of continuous channels of electrons (1D electron wires). Secondly, there is an additional problem due to the fabrication process. When the wires are written, backscattered electrons expose areas of resist between the wires. This effect have been most important for large mark:space ratios and in the worst case may have meant that there was a complete covering of thin resist in the areas of GaAs between the wires. This would explain the poor results for the A707 devices where there are large variations between measured values of V_c and V_t between the big-gate devices and the various wire devices. SEM work could not prove that this was happening because of the poor contrast between resist and GaAs. However, in the optical microscope, there was a slight difference in shading in the spaces between ribs increasing from the edge to the middle of the patterns. This would correspond to resist increasing in thickness closer to the middle of patterns, where the number of backscattered electrons is higher.

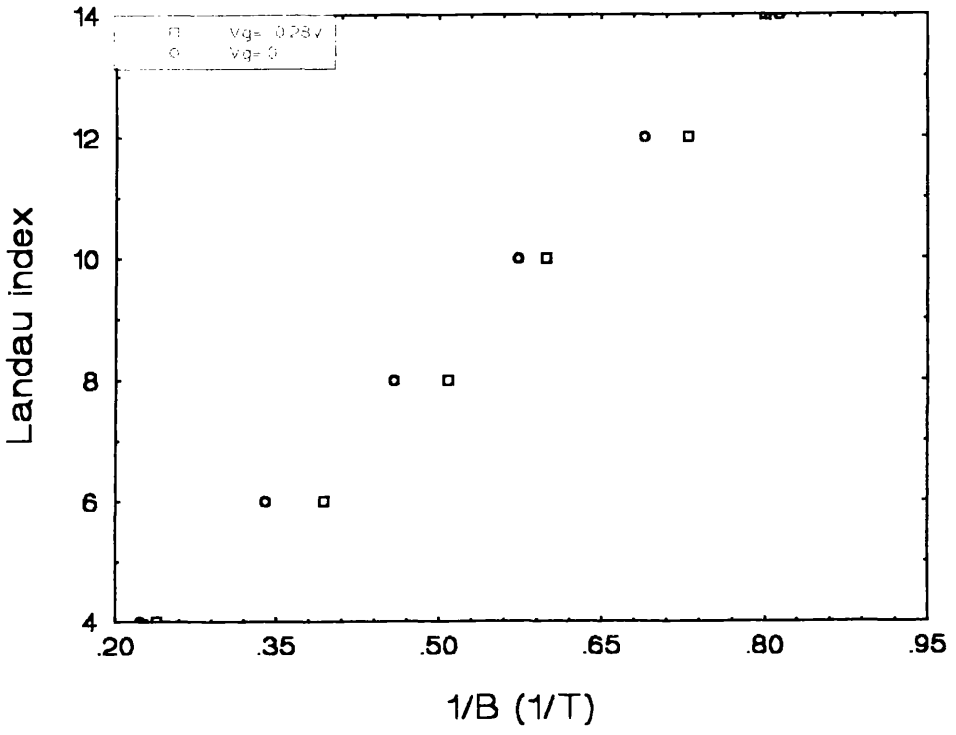
The later devices such as A866 and A909 with smaller mark:space ratios showed better agreement between values of V_t measured on gates and wires, indicating that the resist contamination problem was less severe on these devices. The exception was the A909#2 wire device, which showed much larger V_c and V_t values, indicating there was probably an additional surface contamination problem under this gate.

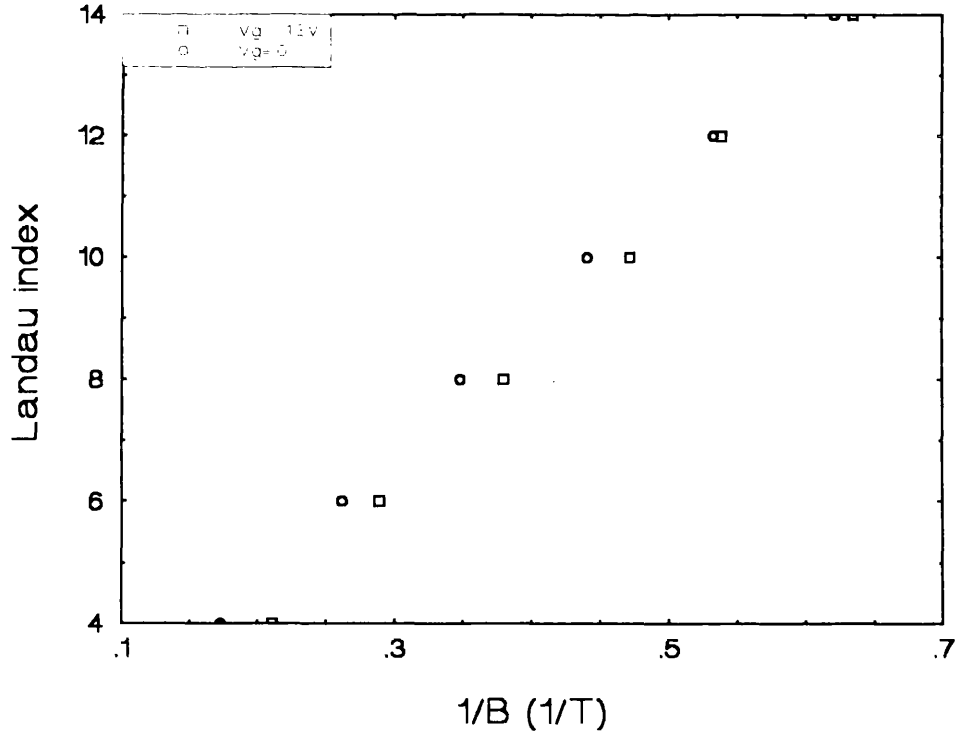
In conclusion the results from this section tend to support the frozen rather than the pinned model, but do not supply a definitive answer. It is difficult to quantify the effects of the resist between wires, or the possible effects of metals on top of the resist, which are inherent in the use of HRN electrostatically formed wires.

5.4.1.3 Magneto-resistance measurements.

Magneto-resistance measurements were used as a probe of how the electrons are behaving underneath the gate. Evidence of 1D behaviour was looked for in the SdH and Haug measurements. Firstly the SdH measurements were examined for any deviation of the positions in the minima. There are no significant deviations in the positions of minima plotted as 1/B vs. Landau index for any of the devices measured (graphs 5.22 shows plots for devices A866#2 and A909 #2). Secondly the SdH and Haug measurements were used to give the carrier concentration for various bias voltages. For the A707 devices (graphs 5.6), there is good agreement between the SdH measurements and the Haug measurements. The 250nm wires data is similar to the big-gate data, the carrier concentration decreases linearly towards the cut-off voltage given in table 5.2. This is consistent with a nearly uniform HRN layer right across the device, with relatively little thinning between the wire regions. The 100nm wires are slightly different. Here the carrier concentration decreases linearly towards a voltage greater than the cut-off and then falls very rapidly towards the actual cut-off voltage. This is evidence of wire formation in these devices with the carrier concentration remaining high under the HRN ribs until squeezed by the side potential. This is confirmed by the capacitance data, where a double cut-off can only be seen clearly for the 100 nm data.

The A866#2 data (graphs 5.7) shows similar values of threshold voltage. The two measured values of V_t, from gate and wire devices, are clearly in the same place, with an extra cut-off (V_c) corresponding to the cut off for the wire. This is a more "hopeful" device for showing 1D behaviour. However, the plot of the SdH minima vs Landau level index did not show any evidence of 1D behaviour (graph 5.22)), when the gate is biased in the region beyond V_c where the wires ought to be formed. The carrier concentration plots (graph 5.8) are more interesting. The variation of the carrier concentration with bias decreases linearly towards V_t but with the SdH trace showing a higher carrier concentration in the region $V_c<V_g<V_t$, corresponding to electrons trapped underneath the resist. In addition, in the Haug plots (graph 5.9 shows a plot for





Graphs 5.22 Landau index plots for A866#2 (top) and A909#2 (bottom).

B= 2.2T), there is evidence of an extra plateau in the wire region (at around V_g = -0.27 V) suggesting a region of high charge concentration under the wire corresponding to this plateau.

Graph 5.12 shows all the carrier concentrations obtained from the A909 devices. Device #2 shows good agreement between SdH and Haug measurements, but the threshold voltages are in poor agreement with the measurements on the big-gate devices. This suggests a surface contamination problem, perhaps again involving non lift-off of HRN in unexposed areas. Device #3 shows a decreasing carrier concentration towards the gate cut-off, but there is no evidence of extra charge under the wires in the Haug data, as is suggested from the cut-off data, where a region corresponding to possible wire formation is seen. This may reflect the dimensions of the device, where the wire area is only 1/10th that of the total area.

5.4.1.4 Capacitance as a function of gate bias.

On A707 #1,2,3, A909 #3 (wire) A909 #2 (gate) capacitance was measured as a function of gate bias. The aims of these experiments were firstly to check for 1D behaviour in the wires and secondly to obtain confirmation that the devices were behaving as expected, i.e. the carrier concentration obtained from the capacitance graphs (from $\int CdV$) gives a value of charge and hence carrier concentration equivalent to that obtained from the SdH measurements. In addition to this, the amount of charge in the two regions should be in proportion to the areas covered by resist or gate. With reference to fig 5.7, for a device with a 1:1 mark space ratio (such as the A707 with 250 nm wires and 500 nm period), area A should be the same as area B. For a gate structure comprising 200 nm wide wires with 2000 nm period, like the A909 device, the area corresponding to the wires should be 1/10th of the area corresponding to the gate.

A909 # 3 was measured at 1.5K and the A707 devices #1,2,3 at 17K in the closed circuit system. No oscillations in the C(V) measurement were seen on the A909 device

data when $\delta C/\delta V$ of the measurement was calculated and plotted. The A707 devices were also checked and no oscillations were found, though 1D behaviour is less likely in these devices since these experiments were carried out at 17K. These results are in agreement with the magneto-resistance measurements, where no 1D effects were seen. There are two reasons for this. Firstly, the existence of resist between wires combined with the effect of the gate on top of the resist ribs will reduce with difference in potential between gated and ungated areas. The difference in potential is now that between two poorly differentiated areas; one with a gate on resist 60 nm thick and another on resist of unknown thickness. This reduces the likelihood of seeing 1D effects because, with the potential 'flattened out', wires are not formed and the situation is closer to that of a 2DEG with only weak modulation. In this case 1D effects are not likely to be seen [23]. In addition to this, if the backscattered electrons exposed areas of resist in a random fashion there would be a variation in the width of the wires leading to pools of charge separated by depleted areas.

The measured values of capacitance at zero gate bias can be compared to the theoretical values obtained from (5.10). These were shown in table 5.4 for A707 and table 5.7 for A909. The values for A707 are low and in poor agreement with the theoretical values (half or less than half the theoretical values), although looking at the two right hand columns of table 5.4, it can be seen that for A707 #1 and #3 which were also measured using the SdH technique, there is good agreement between the two measurements of the carrier concentrations. The values for the A909 devices are in closer agreement with the theoretical figure (compared to the A707 devices). These were shown in table 5.7. The values of zero gate voltage capacitance are 76 percent of the theoretical for the wire device and 92 percent for the big-gate device. The carrier concentrations are also quite close to those obtained from the SdH values.

The relative amounts of charge in the wire and gate regions of the A707 and the A909 device are compared to the expected values for the geometry of the device in table

5.14. For the 100 nm A707 wires, there is clearly a double cut-off for each of the three devices. The amount of charge in the wire region should be 1/5th of the total. For the 250nm device there is only clearly a double cut-off for device number 2, for which the wire charge should be half the total.

Device/gate	wire charge ($x10^{-12}$)C	total charge ($x10^{-12}$)C	percentage (±1.5%)	expected percentage (from geometry)
A707				
#1 100nm	0.39	1.59	24.5	20.0
#2 100nm	0.26	1.72	15.1	20.0
250nm	1.43	2.53	56.5	50.0
#3 100nm	0.29	1.60	18.1	20.0
A909				
#3 200nm	0.75	9.78	7.7	10.0

Table 5.14 Comparison of percentage of charge in wire regions compared to the theoretical value from the geometry of the wire structures. The error of 1.5% is estimated from the areas of charge under the CV plots.

For devices A707 #1 and #3 250 nm wires, there are no indications of separate wire and gate regions and so the data are not presented in table 5.14. There is good agreement between the experimental values and the geometrical percentages in table 5.14. This is in contrast to the very poor agreement between theory and experiment for the zero bias capacitances in tables 5.4 and 5.7. The low values of zero bias capacitance are compensated by the larger cut off voltages which keeps the carrier concentration correct. These results can be best explained by the presence of surface contamination, most likely a thin variable layer of the HRN, exposed during fabrication by backscattered electrons or left after development. It is difficult to ascertain the thickness and spread of the resist because the contrast in a SEM between HRN and GaAs is very poor.

5.4.1.5 Magneto-capacitance data.

The A909 gate (# 2) and wire (#3) samples were measured on the capacitance VTI rod with a varying magnetic field at fixed bias voltage (analogous to SdH measurements) and at fixed magnetic fields with a varying bias voltages (analogous to Haug measurements).

Magneto-capacitance data can be used in a similar way to the magneto-resistance data to find how the carrier concentration varies with gate bias. The magneto-capacitance measurements give a carrier concentration of 5.6×10^{15} m^{-2} ($\pm 0.2 \times 10^{15}$ m^{-2}) at zero bias which compares very favourably with the value of 5.2×10^{15} m^{-2} ($\pm 0.1 \times 10^{15}$ m^{-2}) from the magneto-resistance SdH measurements for the wire device. For the gate device the carrier concentration for the magneto-capacitance measurement was 6.2×10^{15} m^{-2} (± 0.2 x 10^{15} m^{-2}) which also compares quite favourably with the SdH magneto-resistance measurement of 5.4×10^{15} m^{-2} ($\pm 0.1 \times 10^{15}$ m^{-2}).

The extra charge seen in the capacitance graph 5.10 for $V_t < V_g < V_c$ indicates the formation of wires in this device. Haug and SdH type magneto-capacitance measurements show no evidence of 1D effects. SdH type measurements are presented in graph 5.13 for 4 values of gate bias. The curves for Vg=0 and -0.4 V are in the gate region ($V_g > V_t$). The shifts in the minima show the variation of carrier concentration under the gate. The lower two curves are for a gate bias chosen so that the C(V) curve is on the wire region ($V_t < V_g < V_c$), and past the wire region ($V_g < V_c$). The minima observed in these two curves are at the same values of magnetic field. It was hoped that magneto-resistance oscillations in the wire region would give information on the increased number of edge channels running under the gate along the lines of HRN strips. Instead, they seem to indicate that the edge channel capacitance is so small that the sum of the capacitance to the bulk area plus the capacitance to the edge channels running along the boundary between ungated and gated areas is much larger than the capacitance of the edge channels within the device.

5.4.2 Summary and discussion of the side gated superlattice data.

5.4.2.1 Introduction

Qualitatively the data for side gated finger superlattices presented in this chapter were in good agreement with theoretical models. Quantitatively however, there are some fairly serious problems with the data. The most important problems are the reduced capacitance at zero bias in the A909 and A648 devices, and the large range of V_c values observed in the B591 devices.

5.4.2.2 Capacitance, resistance and magneto-resistance data

In all measurements (tables 5.9, 5.11, 5.13), the observed capacitance was less than that predicted theoretically. The poorest data are those obtained for the A909 devices. These values are about a quarter of the calculated values and are in poor agreement with each other. The values from A648 which show better agreement between devices, but are still less than half the theoretical values. The four B591 devices show excellent agreement with each other, but in all cases the measured values are about 5 pF less than the theoretical values.

All the devices were fabricated using the same techniques. The gate metal used was 50nm of NiCr. Since this is a relatively thick layer of material it was thought that it would be enough to prevent breakages where strips of metal make a connection from the etched area onto the channel (in the case of gate off devices). One possible reason for the missing capacitance would be breakages in the wires either on the channel, either physically (due to some separation between two areas of strip which are supposed to be connected) or electrically, (from an area of high resistance due to some impurity problems). In the case of the gate off devices, problems could also have arisen where the fingers rise onto the channel. However S.E.M. photographs of the devices proved that physical breakages were not present. It seems likely that the

problem is an electrical one of lack of connection down the fingers, perhaps due to impurities in the gate metal.

The mark:space ratio was nominally 1:1 for all the devices. Thus, for a gate off device the ratio of charge in the gate area (region 'B' in fig 5.8) to that in the tail plus gate area (region 'A+B' in fig 5.8) should be 50 %. For the gate on devices, there is slightly more gate region due to the gate covering part of the channel, hence the increased expected value of 53 percent.

Ratios for measurements of the integrated charge under the C(V) graphs are shown in table 5.15. The measurement temperature is 1.5 K unless otherwise stated.

Device/gate	wire charge pC	total charge pC	percentage ±1.5	expected percentage (from geometry)
A909				
1 on	5.3	20.9	25	53
2 on	6.6	20.6	32	53
B591				
1 on (17 K)	7.9	12.5	63	53
2 on	5.6	11.1	50	53
off (18K)	4.9	11.7	42	50
4 on (17K)	5.3	17.1	31	53
off	5.0	15.7	32	50
5 on (17K)	5.4	14.7	37	50
off	5.4	13.8	39	53
A648				
2 on	2.7	7.3	37	53
3 on	3.5	7.7	46	53

Table 5.15. Comparison of measured and theoretical ratios of integrated charge under gates to total integrated charge.

The ratios in table 5.15 show that the A909 and A648 data are in poor agreement with the expected values, with less charge in the wire than in the gate regions. Total charge and C_0 values are also low for these devices (Table 5.10). The B591 devices show better agreement between experiment and theory for C_0 and V_t, but poor agreement with V_c. The percentage charge under the gate is in better agreement with theory for the B591 devices, but varies considerably from device to device. It can be seen from tables 5.15 and 5.10 that the poor agreement of the percentage value is not correlated with the variation of V_c.

The metal strips forming the fingers were examined using a SEM. No breakages were found. The low observed values of the A909 and A648 capacitance are most likely due to poor electrical connections to the superlattice as a result of an impurity problem with the evaporated NiCr gate. The B591 devices were fabricated before the A909 and A648 devices. In the Plassys evaporator, the NiCr metal source was changed to one from a new manufacturer in the time period between the fabrication of the B591 devices and the other two, and this may have been associated with the subsequent problems.

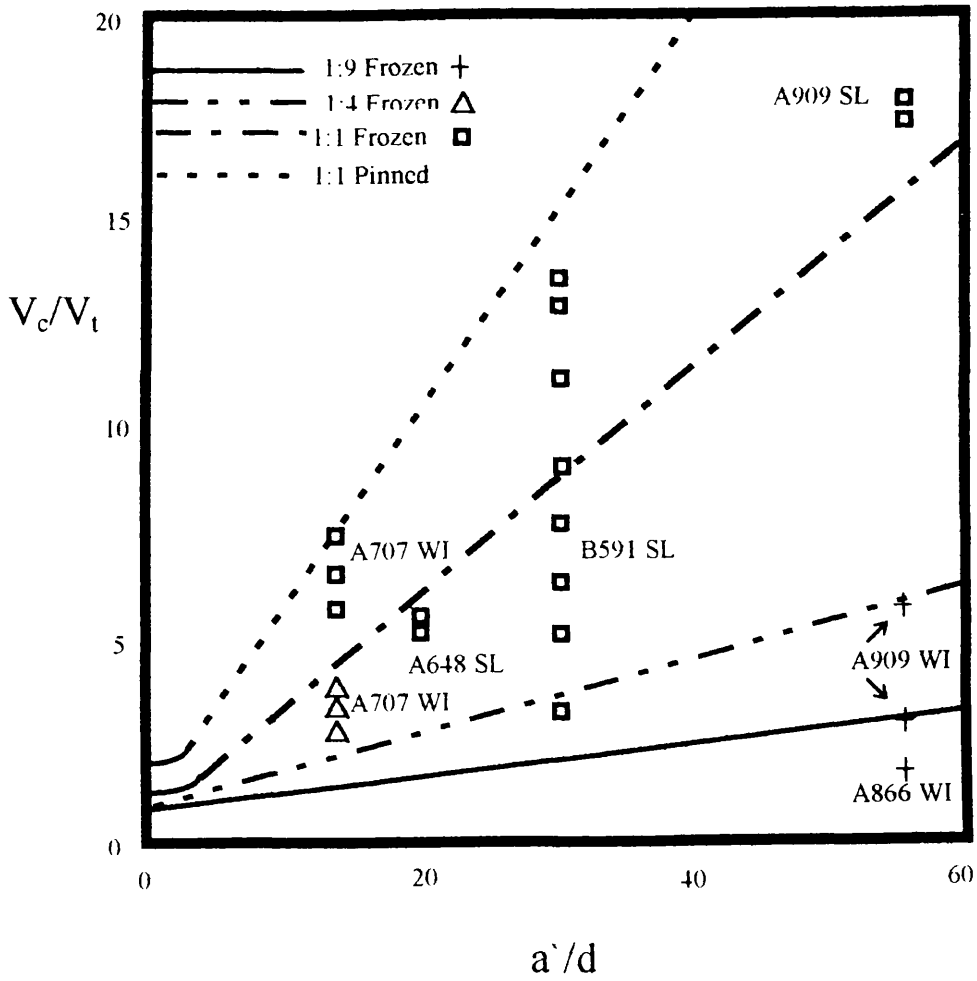
It is possible that the variations in V_c and the relative charges in the gate areas for B591 devices are due to local variations in doping density in the channel. These variations would have to be localised on a scale much smaller than the gate dimensions (180 μm × 190 μm) so as not to be detected by the SdH measurements which were consistent with each other (and with other devices measured). A B591 device with a small period superlattice was measured and is reported in chapter 6. It had a carrier concentration of 2.5×10^{15} m^{-2} in excellent agreement with devices measured in this chapter.

5.4.2.3 Cut-off voltages.

The data obtained from the three devices was presented in tables 5.8, 5.10, and 5.12. The measured values for the A648 devices show the best agreement with each other and with the frozen surface model, this value being within 0.5V of the measured one.

The values for the A909 devices agree with each other but are more ambiguous although still tending towards the frozen theory.

The B591 devices show the biggest range of values of V_c, whilst V_t is in excellent agreement with theory. Again these measurements of V_c are much closer to the frozen than the pinned theory, with the theoretical frozen calculation lying in the middle of the range of measured values. All the results of V_c/V_t from the devices in chapter 5 (longitudinal wires on HRN and side gated superlattice) are shown in graph 5.23. Also plotted are theoretical curves for the different mark:space ratios.



Graph 5.23. Theoretical curves and experimental values of V_c/V_t from chapter 5. Here a` is the period of the superlattice and d the depth of the 2DEG. WI refers to a wire measurement and SL a side gated superlattice measurement. 1:1, 1:4 and 1:9 are mark:space ratios

5.5 Conclusions.

Overall the results of the experiments on the longitudinal wires in this chapter did not fulfil the main objectives. These were firstly to find evidence for 1D effects in longitudinal wire arrays formed electrostatically on shallow materials. A secondary aim was to differentiate between the pinned and frozen models which describe the ungated areas of GaAs. The lack of evidence of 1D effects has been shown to be most likely due to fabrication problems in producing uniform wires, together with poor material which manifested itself in the poor mobilities (and hence low mean free paths) seen in the three devices used. Steps to try and improve the chances of the observation of 1D effects were made initially by reducing the number of periods and increasing the spacing between resist strips. The most recent devices had an increased number of periods and gate length but a very small mark to space ratio. A full set of capacitance and magneto-capacitance studies were carried out. The capacitance measurements showed that there was an accumulation of charge under the resist strips but magneto-capacitance and magneto-resistance measurements did not show these electrons behaving one-dimensionally. Problems with controlling the HRN profile made it difficult to draw unambiguous conclusions from the data, and this technique of wire production is not likely to be of much use in the future.

The pinned/frozen argument was also unresolved because of fabrication difficulties. The experiments on the three side gated finger superlattice devices supported the more physically realistic frozen model for the behaviour of ungated surfaces of GaAs at low temperatures.

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Chapter 6

Experiments on lateral surface superlattices.

6.1 Motivation and Introduction.

6.1.1 Motivation.

In this chapter measurements on lateral surface superlattices will be described. The periodic potential from the superlattice modulates the channel in a direction perpendicular to the current flow in a Hall-bar. At very small periods, new physical effects are predicted. Among other measurements, data will be presented in this chapter from a lateral surface superlattice with a period of 60 nm. This is the smallest period yet reported using this type of gate structure. In addition, the relative magnitudes of electrostatic and strain induced potential can be calculated using the experimental magneto-resistance data and these results will be compared with recent models. It was found that the potential from strain modulating the 2DEG (via the deformation potential) could not account for the magnitude of the potential or its variation with gate bias. An alternative coupling scheme based on the piezo-electric effect was found to be the most likely mechanism for the observed magnitude and variation of the potential with gate bias.

6.1.2 Introduction.

Lateral surface superlattices comprise a periodic array of strips of metal which are fabricated using positive resist and cover the channel of a Hall-bar perpendicular to the current flow direction. A schematic diagram of this arrangement with detail of the superlattice is shown below in figure 6.1.

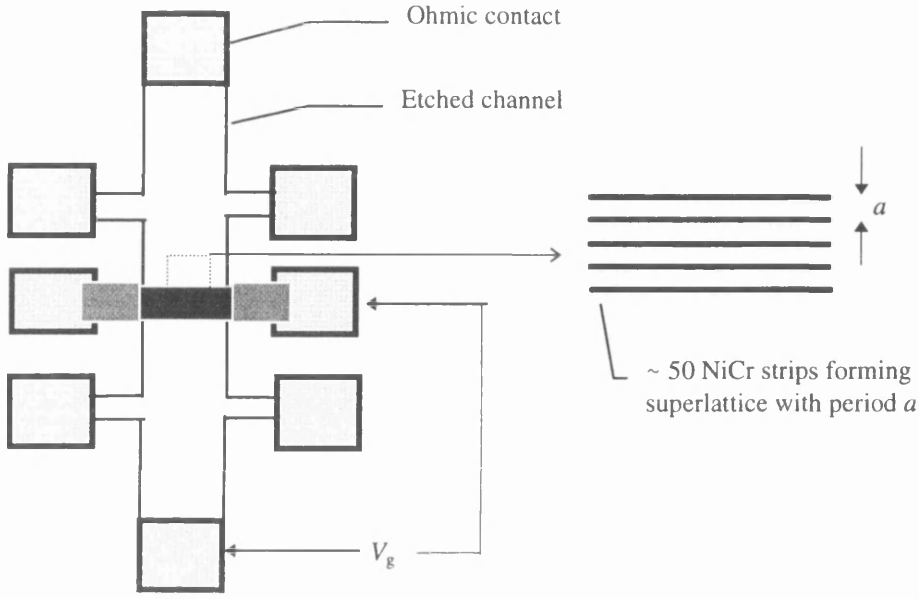


Fig 6.1 Plan view of Hall-bar showing detail of gate arrangement.

Detail of the gate arrangement is shown in the diagram below. There were two types of superlattice design, one where the superlattice connections were made off the channel (shown in fig 6.2 a) and another design where the superlattice connections were made on the channel (shown in fig 6.2 b).

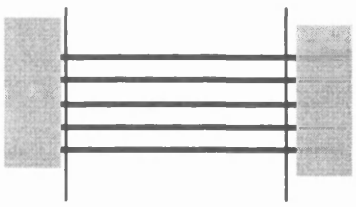


fig 6.2 (a) Representation of gate connections showing 'gate-off' arrangement.

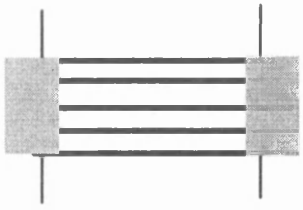


fig 6.2 (b) Representation of gate connections showing 'gate-on' arrangement.

Lateral surface superlattices were made with different periods ranging from 2000 nm to 60 nm on deep and shallow AlGaAs/GaAs and AlAs/GaAs heterostructures. Most effort was concentrated on the smaller period superlattices on shallow materials. Resistance and magneto-resistance measurements were made at 4.2 K using the VTI.

6.1.2.1 Magneto-transport measurements.

Low field magneto-resistance (MR) measurements reveal a series of oscillations first observed by Weiss [1]. These oscillations have their origin in a semiclassical effect which is a result of the crossed electric and magnetic fields. When the cyclotron orbit is commensurate with a period or number of periods of the potential imposed by the superlattice, the oscillations (known as Weiss or commensurability oscillations, CO) are observed. At the extrema of the orbit, the electron experiences an electric field from the superlattice which is additive in the direction parallel to the equipotentials, but cancels for perpendicular motion. The additive electric field results in a drift in the guiding centre motion of the electron at a drift velocity, v_d [2]. This guiding centre motion can be understood in terms of the drift velocity, $(1/B^2)(\mathbf{E}\times\mathbf{B})$ [3], experienced by an electron in the crossed electric and magnetic fields. In the case of a weak periodic potential $eV/E_f << 1$, the electron will experience alternating signs of $\mathbf{E}\times\mathbf{B}$ drifts. The time average of the drift velocity along a cyclotron orbit is obtained by integrating the electric field along the orbit, $v_d(Y) = (2\pi B)^{-1} \int_0^{2\pi} d\phi E(Y+R\sin\phi)$ where Y is the coordinate of the centre of the orbit, R is its radius and ϕ is the angular coordinate round the orbit. v_d is enhanced or reduced depending whether E(Y+R) and E(Y-R) have the same sign or the opposite sign. This is shown in fig 6.3. for an oscillation where E(Y+R) and E(Y-R) have the same sign and so drift is enhanced.

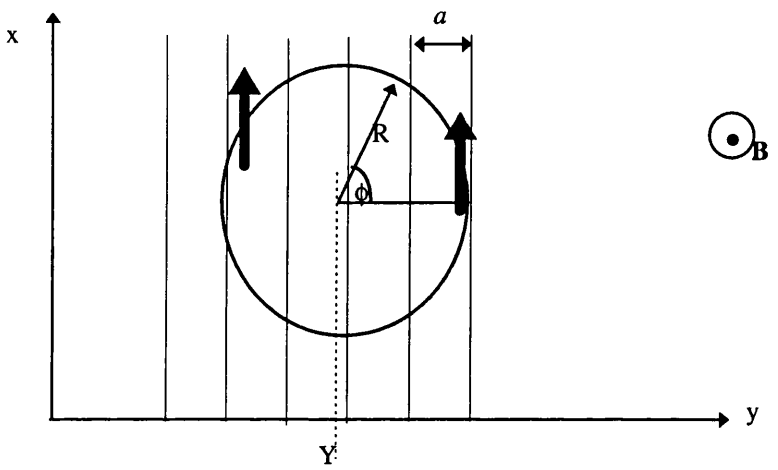


Fig. 6.3 A potential grating, generating a potential V in the 2DEG. The superlattice period is a. A cyclotron orbit is shown superimposed on the superlattice.

The overall effect is to enhance the motion of the orbits parallel to the superlattice for values of B where the cyclotron orbit diameter is (approximately) equal to one or more periods. These oscillations are labelled by k where $k = 1$ corresponds to the electron orbit diameter which is approximately equal to one period of the superlattice, $k = 2$ an electron orbit is approximately equal to two periods of the superlattice etc.

Fig 6.4 is a typical graph of a magneto-resistance measurement. It shows commensurability oscillations with their k values, a low field magneto-resistance peak marked by the label B_C and SdH oscillations.

Beenakker [2] showed that the fractional change in the MR for the nth harmonic of the surface potential V_n is given by:

$$\delta\rho/\rho = (eV_n/E_F)^2(nl^2/aR_c)\cos^2\{(2\pi nR_c)/a - \pi/4\} \qquad (6.1)$$

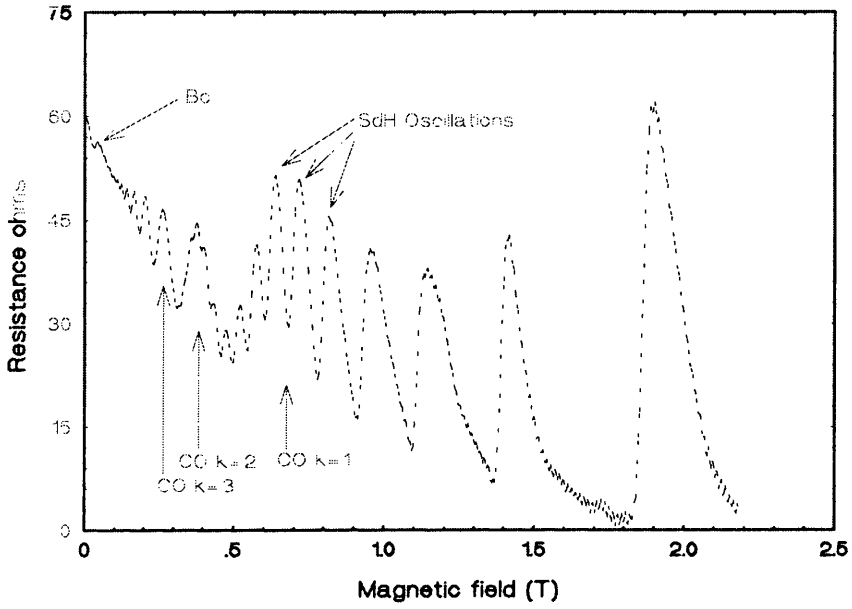


Fig 6.4. Typical magneto-resistance measurement showing significant features for a device with a 200 nm superlattice on A448 (deep material).

Here $\delta\rho/\rho$ is the fractional change in the magneto-resistance, E_F is the Fermi energy, l the electron mean free path, a the fundamental period of the superlattice and R_c is the cyclotron radius. This result is extremely useful because it allows the magnitude of potential V_n 'seen' by the electrons in the 2DEG to be calculated. This potential was calculated by differentiating equation 6.1 with respect to magnetic field. The magneto-resistance data were also differentiated (using the plotting program, Easyplot) to find the peak change in resistance. The value for the change in resistance obtained from Easyplot was divided by the zero field resistance of the area under the gated region. This value was then substituted for the term $\delta\rho/\rho$ in equation 6.1. The other terms in 6.1 are known or can be calculated and the value of V_0 is obtained. This technique using the derivative was adopted to remove any linear magneto-resistance variation from the data and hence enhance the accuracy with which the amplitudes could be deduced.

Three problems with the Beenakker formula have been identified by Bøggild et al. [4]. 1) The low field oscillations die away more quickly than is predicted by (6.1) as magnetic field is reduced. 2) The low field peak marked as B_C in fig 6.3 is not observed in magneto-resistance curves generated from (6.1). 3) At high magnetic field a large quadratic magneto-resistance is observed for large values of V_0. Bøggild et al explained point 1) as being the result of small angle scattering. They used a Monte Carlo technique and, by adjusting the modulation strength and a parameter τ_t/τ_s, a theoretical curve was drawn and compared to experimental data. Here τ_t is the momentum (transport) relaxation time and τ_s is the unweighted scattering time which is dominated by small angle effects. Bøggild et al. showed that the most likely cause of the reduction in low field CO was due to the parameter τ_s. This has little effect on low field resistance but can easily scatter an electron from one resonant orbit to another. Electrons with higher k values travel further (higher k corresponds to lower magnetic field and hence a larger cyclotron radius) and so have more chance of being scattered.

Point 2) The low field resistance peak was attributed by Bøggild et al to open electron trajectories. This peak had been previously studied by Beton et al [3] who found that V_0 could also be calculated from this low field resistance peak. Beton et al found that the peak was due to streaming orbits where the electrons do not obtain sufficient momentum to overcome the electrostatic force of the applied V_0 and the electrons stream parallel to the equipotentials. This peak defines the start of the semi-classical magneto-resistance oscillations since an increase in magnetic field past this point gives the electrons enough effective energy to overcome the electrostatic force. The streaming velocity is very close to the Fermi velocity (v_f) and these trajectories make a large contribution to the magneto-resistance. The critical field B_C at which oscillations first appear was estimated as

$$B_C = 2\pi V_o/av_f \qquad (6.2)$$

This was confirmed by Müller et al [5] to within a factor of the order of unity. Previous work in Glasgow [6] has shown V_0 calculated from B_C to be larger than and in relatively poor agreement with the value of V_0 obtained from the CO.

The third problem, point 3) which was identified by Bøggild et al. for large values of V_0 was tackled by Geim et al [7] who found that this effect could be explained by a more complete form of Beenakker's formula (6.1). The difference in carrier concentration between the gated and ungated regions leads to a distortion of the cyclotron radius and a drift in the guiding centre along the direction of the superlattice equipotentials. Geim et al. found that in the limit $a >> R_c$

$$\delta\rho/\rho = 1 + (eV_0/E_F)^2.(l/R_c)^2 \qquad (6.3)$$

for a one dimensional lateral superlattice. This one dimensional case suggests a B^2 dependence, which was observed in Geim's experiments. Geim et al. also found experimentally that in the same region a two dimensional surface superlattice had a linear variation with B.

6.1.2.2 Possible variation of V_0 with gate bias.

The origin of the potential V_0 was initially assumed to be mainly electrostatic. Experiments with $V_g = 0$ also revealed CO [6] and this was assumed to be due to a built-in voltage V_{bi} as a result of the change in the Schottky barrier height between metalled and unmetalled areas. The expected variation of the potential with bias for this simple model is shown below in fig 6.5. V_{bi} can in principle be positive or negative and it should be possible to cancel V_{bi} by applying an external potential.

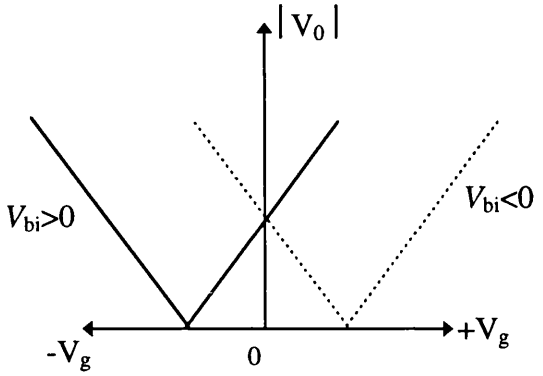


Fig. 6.5 Potential variation with gate bias for an ideal layer with no screening.

The most obvious problem with this simple model is that it does not take into account the screening effects of electrons in the donor layer or in the 2DEG. This is especially important for shallow AlAs materials. In shallow AlAs materials, a layer of electrons is believed to be present around the donors. This shifts the threshold voltage because the screening electrons must be depleted first. This is shown in fig. 6.6 for two AlGaAs barrier and two AlAs barrier materials grown in Glasgow [8].

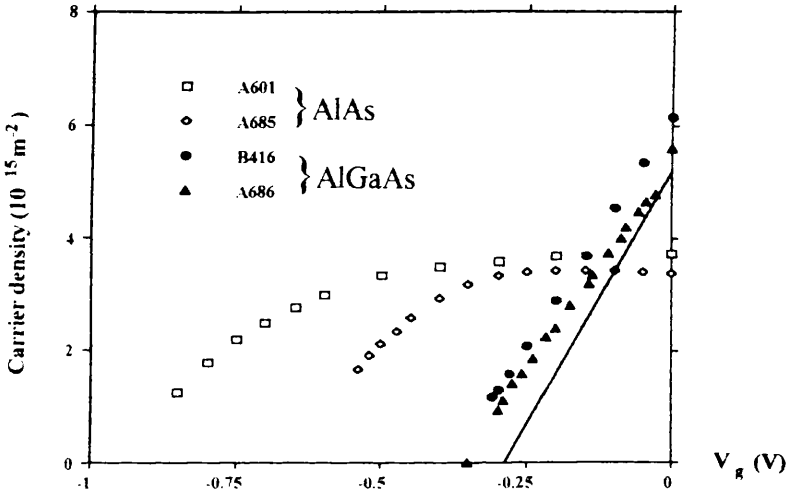


Fig 6.6. Carrier concentrations with bias for AlAs and AlGaAs barrier materials measured in Glasgow by Skuras et al. [8]

This layer of electrons makes a negligible contribution to transport but increases the mobility of the electrons in the conducting layer. This increase is obtained because the layer screens the full random potential from the ionised donors and increases the mobility from an estimate of about 20 $m^2V^{-1}s^{-1}$ to the values of over 60 $m^2V^{-1}s^{-1}$ observed [9]. For these layers, the effect of an electrostatic potential will be reduced as the bias is made more negative until the screening layer of electrons is depleted. This in turn introduces an additional problem because the Beenakker formula predicts that the CO are directly proportional to the mean free path. As negative bias is applied, removing screening electrons will reduce the mean free path and hence the amplitude of oscillations, particularly at high k values. In forward bias the positive voltage will add electrons to the screening layer under the gates further reducing V_0. A possible variation of the potential with bias is shown in fig 6.7 below. This would

be applicable to a CO with a low k value which is unaffected by a low mean free path.

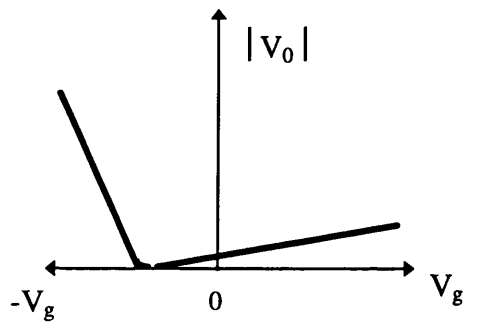


Fig. 6.7 Estimated potential variation with gate bias after screening for $V_{bi}>0$

Davies and Larkin [9] calculated the electrostatic potential with screening for the pinned and frozen models (for descriptions of pinned and frozen boundary conditions see chapter 5, section 1.3.1) and compared the results to experimental data. Their calculations suggested a potential rather larger than observed for devices fabricated on shallow AlAs (assuming $V_{bi} = 100$ mV). The material used, A601, was of the same dimensions and grown in the same MBE machine as the shallow AlAs barrier material in this work, A858 and A881. The only difference was in the doping concentration. A601 was doped with 4×10^{16} m^{-2} Si atoms and A858 and A881 were doped with 7×10^{16} m^{-2} Si atoms. The experimental data [6] also showed evidence of a very strong second harmonic indicating an anharmonic potential which also could not be explained from the pinned or frozen electrostatic models. A model in better agreement with the experiments developed by Davies and Larkin was based on a potential originating from elastic strain from differential contraction between the metal gates and GaAs. This arises because the device is rapidly cooled after evaporation of the Ti/Au gates at high temperatures. The strain then couples to the 2DEG through the deformation potential. This model gave the agreement with the results but the magnitude was still out by a factor of 2. The discrepancy was thought to be due to lack of knowledge of the surface conditions during the deposition of the evaporated metal. In fact, because the screening effects of the electron gas were omitted from these calculations, it is now believed that the results of the strain model are even further astray, by at least a factor of ten.

A possible variation of the potential with gate bias for electrostatic and strain contributions is shown below in fig. 6.8, for an AlAs device. Here the strain and negative electrostatic contributions are in addition (this is predicted for the differential contraction between Ti gates and GaAs [9]) and the resultant potential is shown by the bold line.

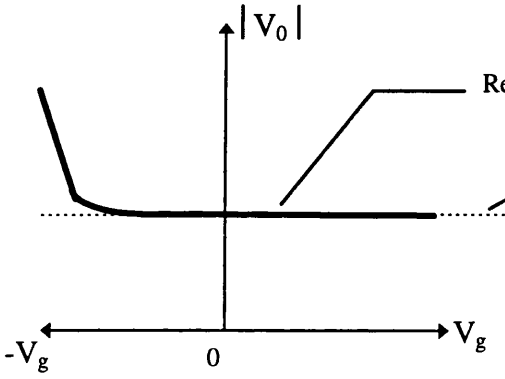


Fig. 6.8. The estimated potential profile with gate bias including strain, electrostatic potentials and the effect of screening.

A factor not considered in the Davies strain analysis is the piezo-electric effect. Piezo-electric effects due to stress from Schottky gates [10] give rise to a volume charge density which can significantly change the characteristics of surface gated devices, such as FETs fabricated on GaAs. The resultant shift in threshold voltage is dependent on the growth direction of the substrate and orientation of the Hall-bar. For example a Hall-bar fabricated on a (100) substrate is fabricated along a natural cleave which could be $[0\bar{1}1]$ or [011] and the sign of the predicted piezo-electric potential is opposite for these two cases.

6.1.2.3. Prediction of new quantum effects.

The motivation for fabricating superlattices with very small periods was due to the prediction of new quantum mechanical effects such as minibands with accompanying Bloch oscillations. Theoretical calculations [11,12] predict the observation of quantum mechanical effects if the period of the lateral surface superlattice is reduced below the Fermi wavelength. Shallow AlAs barrier materials typically have a carrier concentration of $3.5 \times 10^{15}\ m^{-2}$ corresponding to a Fermi wavelength of approximately 40 nm, while shallow AlGaAs barrier materials have a higher carrier

concentration of the order of 6 x 10^{15} m^{-2} which corresponds to a Fermi wavelength of 30 nm. Initially experiments were concentrated on the shallow AlAs barrier materials since the Fermi wavelength is closer in these devices to the minimum experimental superlattices period of 60 nm. The application of negative gate bias will reduce the carrier concentration and bring the Fermi wavelength close to the applied periodic potential of the superlattice. An additional consideration is the amount of potential 'seen' by the electrons in the 2DEG. A potential of 5-10 meV is estimated [13] to be required to see quantum effects.

An interesting extension of the work on lateral superlattices is to fabricate a two dimensional surface superlattice. When a magnetic field is applied to a device with a two dimensional surface superlattice, a remarkable energy spectrum known as the Hofstadter Butterfly is predicted [12]. This fractal structure is a result of the internal resolution of subband structure of the Landau levels. Observations of these effects are predicted for B $\approx$ 1T and a $\approx$ 50nm. In this work, data is presented on a superlattice formed by two lateral surface superlattices fabricated so that the second superlattice lies at right angles on top of the lower one. This results in a periodic array of squares which form a two dimensional surface superlattice. The period of the square superlattice fabricated in this work was 100 nm.

6.2 Materials and structures.

Devices on deep bulk-doped material (as shown in fig 4.6) were made with superlattices which had periods between 1000 nm and 200 nm. Shallow AlAs materials (shown in fig 4.7) were used with superlattices of periods 100 nm and 60 nm. Measurements were also attempted on a range of shallow AlGaAs materials using 60 nm period superlattices. These did not show any evidence of the semi-classical CO. Details of materials, Hall-bar type and gate structures for which measurements were completed are shown in table 6.1.

Device/barrier type	2DEG interface depth (nm)	Carrier conc. ($x10^{15}$) m^{-2}	Hall-bar type (see fig 2.3)	Gate period (nm)	mfp (μm)
A448 Deep AlGaAs	92	2.8 2.7	B B	200 300	10.3 9.2
A659 Deep AlGaAs	92	2.9 3.0 3.0 2.9	A A A B	200 300 400 300	12.0 12.4 11.9 7.2
A648 Deep AlGaAs	92	2.5	D	1000	7.7
A858 Shallow AlAs	28	3.5 3.6	B B	60 100	2.6 2.9
A881 Shallow AlAs	28	3.3	B	100	4.0
B591 Intermed-iate AlGaAs	57	2.5	B	60	1.5
A916 Shallow AlGaAs	38	5.3	B	60	1.3
B466 Shallow AlGaAs	38	5.4	B	60	5.0

Table 6.1 Materials types and gate dimensions of devices measured in chapter 6.

6.3 Measurements.

Resistance and magneto-resistance measurements were taken using the VTI for all the devices in table 6.1. Cut-off voltages were obtained from the resistance measurements. Magneto-resistance measurements revealed series of CO and SdH oscillations. A useful tool in analysis of the magneto-resistance data is to take the Fourier transform (FT) of the curves. (A description of the FT process is given in

Chapter 5, section 1.3.2). In the FT of measurement curves there is a peak typically at 6-7 T which is as a result of the SdH oscillations. This peak can be used to find the carrier concentration. Lower field peaks are a result of the CO. The positions of the CO minima in the magneto-resistance curves can be compared to theoretical values [4] given by

$$2R_c = (n - 1/4)a \qquad (6.4)$$

When the fundamental of the potential, V_0, is large, higher harmonics may appear, though only the second harmonic is strongly present in any of the data. It occurs at a position of $2 \times B_0$ where B_0 is the position of the first harmonic given by,

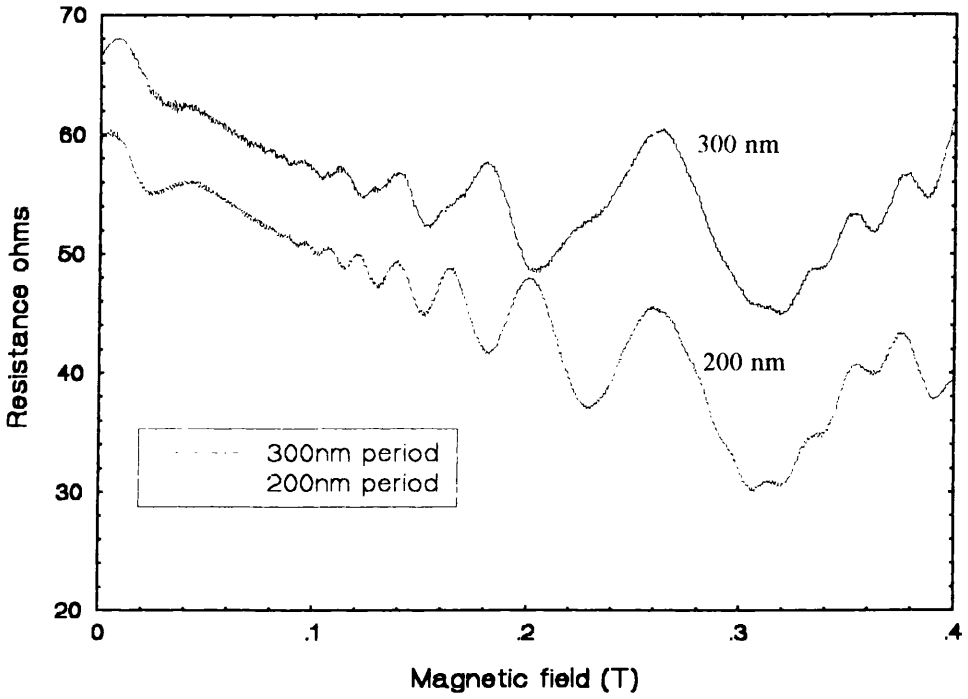
$$B_0 = \hbar(8\pi n)^{1/2}/ea \qquad (6.5)$$

In the analysis to obtain the potentials using (6.1), an Excel spreadsheet was used and the graphs of the potential against gate bias were also produced using Excel.

6.3.1 Measurements on deep bulk doped materials (A448, A659 and A648).

a) A448 devices.

The first measurements were carried out on this very high quality material which had a very large mobility. The device consisted of two type B Hall-bars side by side both fabricated on the same chip at the same time. There were enough connections on the header to measure both devices so they were both studied in the same cooling cycle. Unfortunately the gate connections to these devices appeared to be faulty. Applying an increasing negative gate bias did not cut-off the channel on these devices, but only caused an increase in the resistance by about 4 ohms. However the magneto-resistance measurements revealed many CO. Plots of A448 #1 are shown in graph 6.1. Of note on these graphs is the strong second harmonic for the 300 nm period



Graph 6.1. SdH measurements of A448 200 nm and 300 nm superlattices

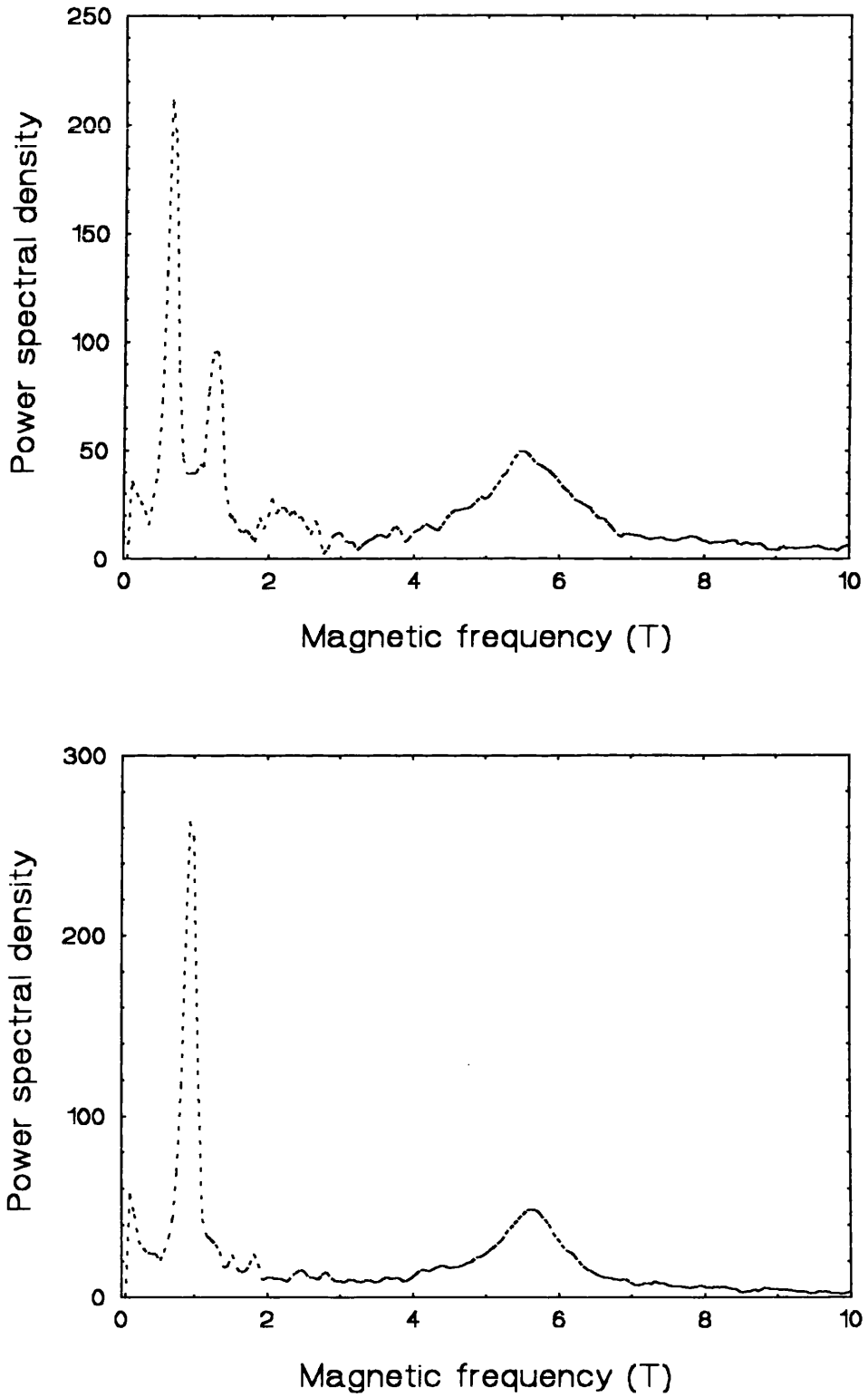
device which is absent in the 200 nm device. This is observed much more clearly in the Fourier transform of these curves shown in graph 6.2. The magnitudes of the peaks for these devices were analysed, and the potentials obtained are shown in table 6.2 (pg 123).

b) A659 device.

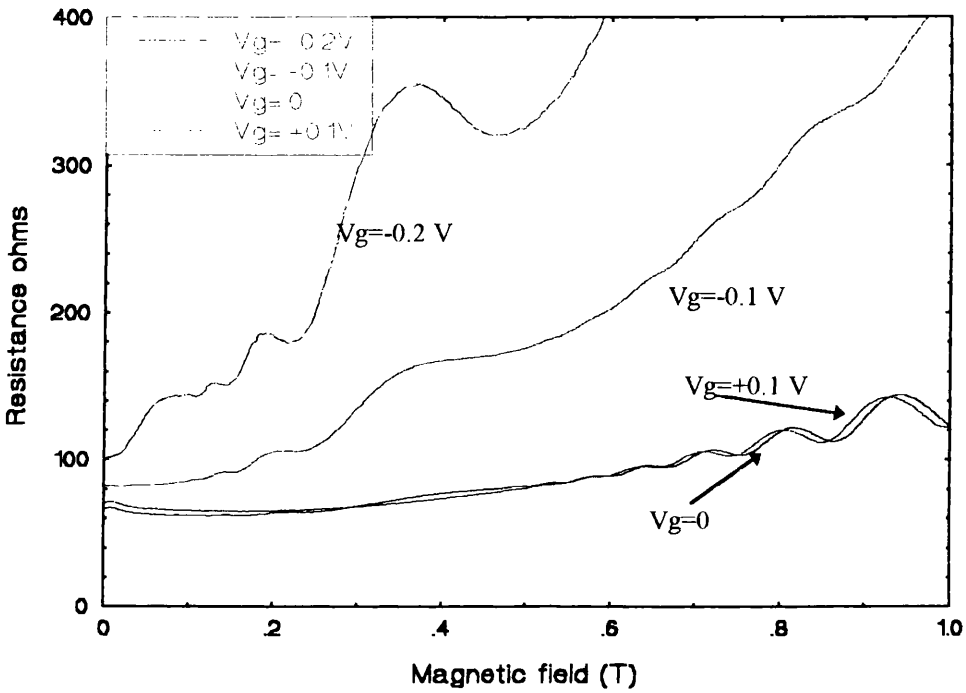
This device consisted of a type A Hall-bar with channel width reduced to 20 μm in the region of the gates. There were three gates in series and here the gate connections came up onto the Hall-bar ensuring a gate connection (as shown in fig 6.2b)). The lattices were designed to have 200 nm, 300 nm, and 400 nm periods with differing mark:space ratios of 1:1, 1:2 and 1:3 respectively. The devices actually fabricated had the "mark" slightly bigger than designed (the width of one of the gate strips was estimated to be 120-130nm). This was due to the backscattered electrons (used to expose the resist during electron beam lithography) over-exposing neighbouring strips. The channels cut off as expected, all gates reaching threshold voltage below -0.7V. Graph 6.3 shows the magneto-resistance plots for the 400 nm superlattice. The oscillations are superimposed on a positive magneto-resistance and increase in magnitude with negative gate bias. The rate of increase of this background positive magneto-resistance also increases with negative gate bias. The 200 nm data showed CO at zero bias and this decreased when negative bias was applied to the gate, whereas the 300 nm data were similar to the 400 nm data. The 400 nm data showed the strongest CO the Fourier transform is shown in graph 6.4. All this data were analysed and the potentials were calculated. Table 6.2 (pg. 123) shows values for zero bias and non zero gate biases for the 400 nm superlattice. Graph 6.11 shows the potentials calculated from the amplitudes of two oscillations for the 400 nm superlattice.

c) A648 devices.

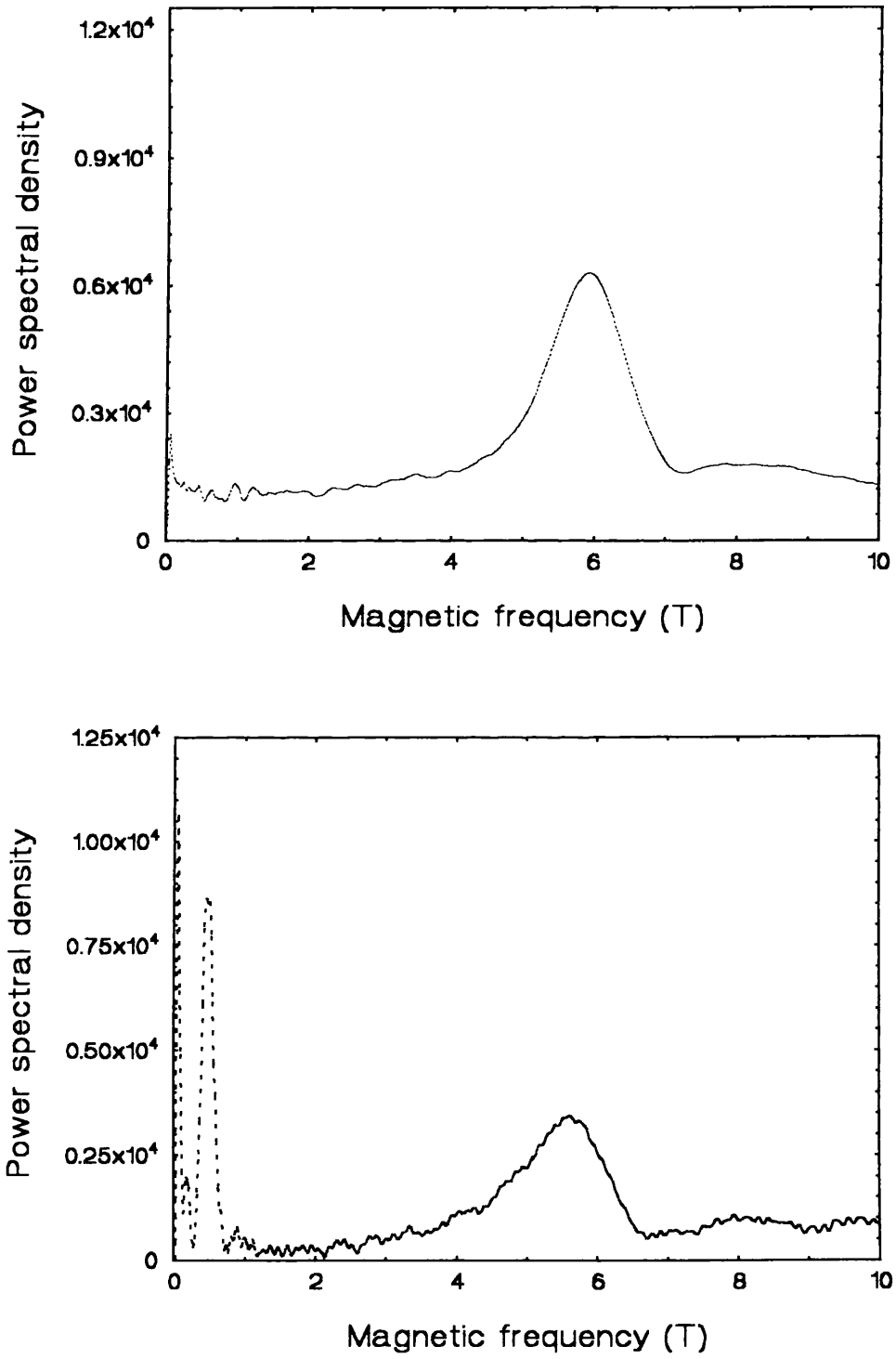
These devices were fabricated at the same time as the finger superlattices (described in the previous chapter) and were intended for comparison with the finger devices.



Graph 6.2. Fourier transform of A448 data 300 nm (top) and 200 nm (bottom). The peaks at 5.8 T are from SdH oscillations.



Graph 6.3 SdH measurements of 400 nm A659 sample.



Graph 6.4. A659 400 nm Fourier transform for Vg=0 (top) and Vg=-0.1 V (bottom). The peak at 5.8 T is from the SdH oscillations

Two devices were made using the Hall-bar D design pattern (which has a 200 μm channel width). One had a 1 μm period superlattice and the other a 2 μm period superlattice with 1:1 mark space ratio. These periods are very high for the observation of CO but it was thought they might show CO because of the large mean free path in this high mobility layer. These devices showed a strongly increasing magneto-resistance but no sign of a series of CO, either in the raw data or in the Fourier transform.

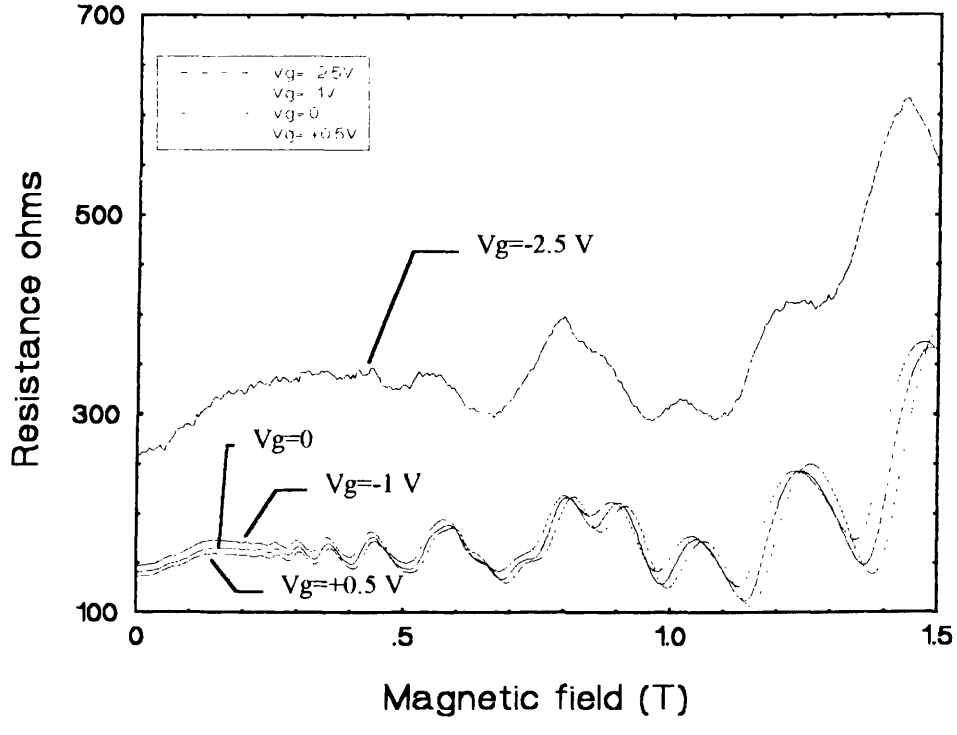
6.3.2 Measurement of shallow AlAs materials (A858, A881)

These experiments were made on Hall-bars of type B, which had a narrow 10 μm channel.

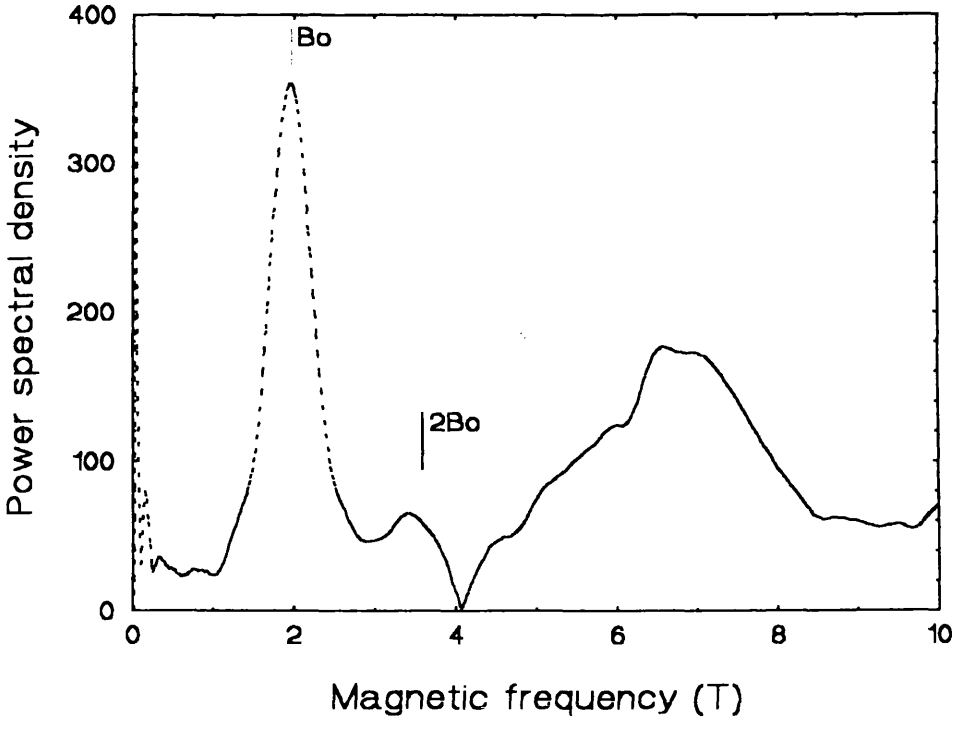
a) Two 100 nm superlattices were measured on A881. One was of the standard type and the other a variation where another longitudinal lattice was placed on top of the lateral one to produce a series of periodic squares. This was an idea of Dr Elef Skuras for generating a short period square superlattice. It had been hoped to fabricate more of these on different materials with 60 nm periods if time had permitted. The device with the square superlattice was fabricated on the same chip as the 100 nm lateral superlattice.

The 100 nm device had a cut-off of -3 V. Graph 6.5 shows a series of curves for various bias voltages from +0.5 V to close to cut-off at -2.5 V. The SdH oscillations are superimposed on the CO from about 0.7 T. The CO decrease in amplitude with negative gate bias, as shown in graph 6.8. The Fourier transform of a curve at V_g=0 is given in graph 6.6, and shows a strong fundamental with a little second harmonic. The theoretical position of 1st harmonic B_0 and 2nd harmonic $2B_0$ are indicated by pointers on the graph.

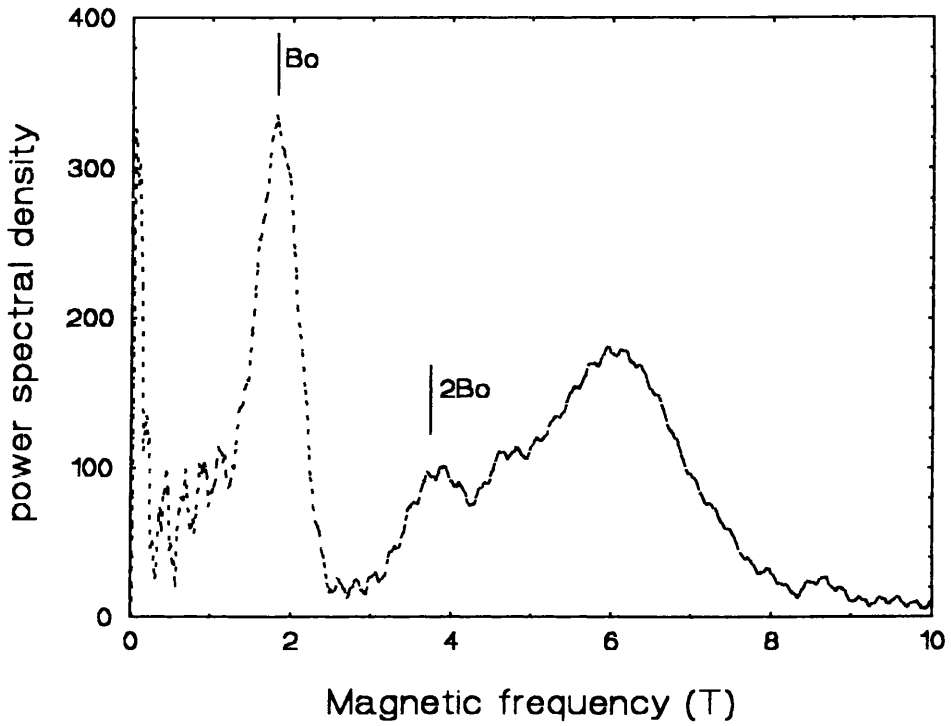
The 100 nm square device had a cut-off of -1 V and a series of magneto-resistance plots were measured for different gate biases. The curve obtained from the Fourier transform of the zero gate bias plot is shown in graph 6.7. The CO were analysed directly for both devices and a typical plot of potential V_0 vs. gate bias is shown for k



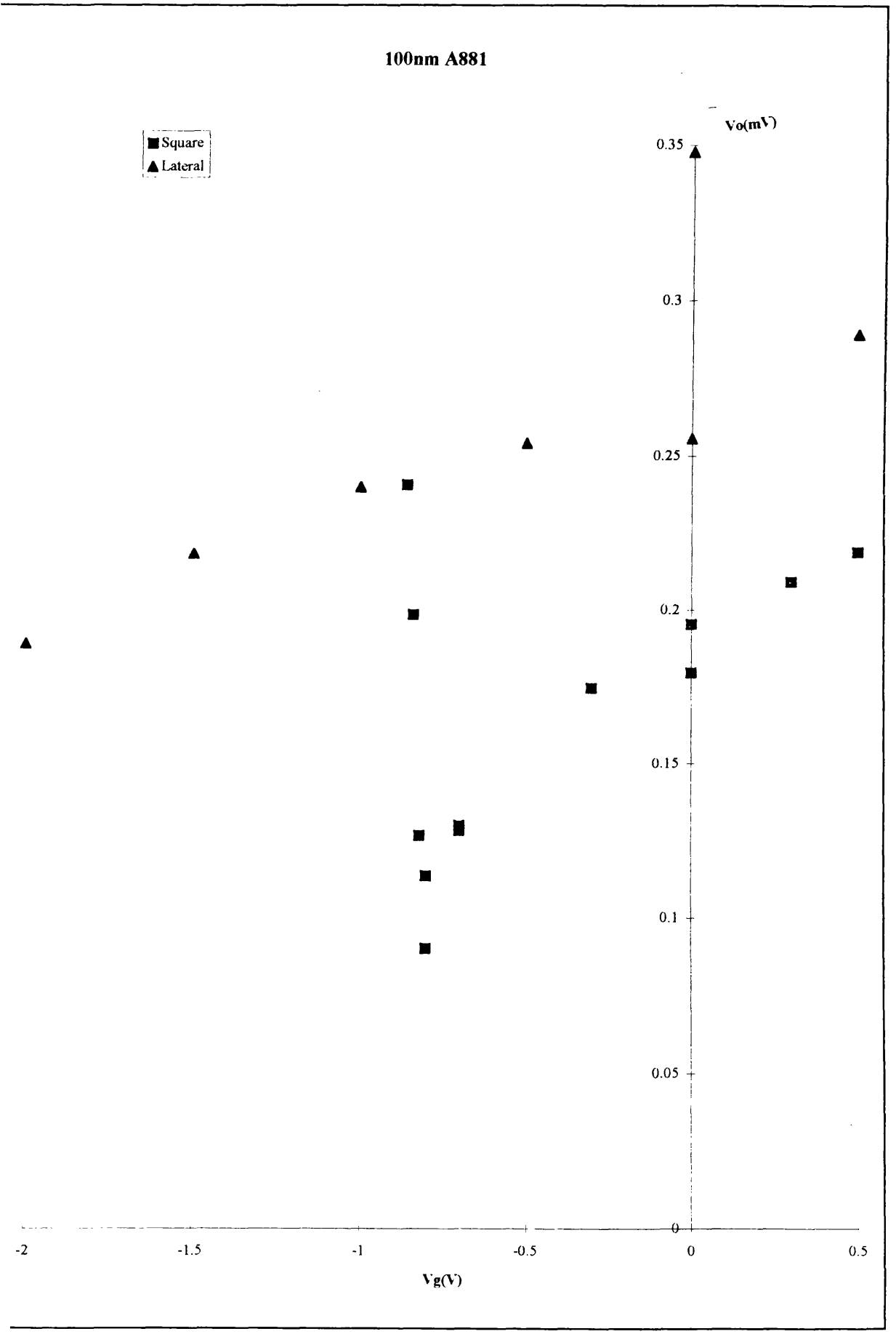
Graph 6.5. A881 100 nm superlattice SdH data



Graph 6.6 A881 100 nm lateral superlattice FFT plot.
The peak at 7 T is from the SdH oscillations



Graph 6.7 A881 100 nm square superlattice
The peak at 6 T is from the SdH oscillations.



Graph 6.8. 100nm lateral and square superlattice potentials with bias

= 6 in graph 6.8 where it can be seen that V_0 decreases and then increases with negative bias. Potentials at zero gate bias are shown in table 6.2. for both the 100 nm square and the 100 nm lateral devices.

b) 60 nm and 100 nm lateral superlattices on layer A858.

The first A858 device had a cut-off voltage of -0.65 V and produced very strong CO. The amplitude of these CO increase with negative gate bias. This device had a period of 60 nm, believed to be the shortest period superlattice ever reported. A measurement for zero gate bias is shown in graph 6.9 and the Fourier transform is shown in graph 6.10 with arrows showing the theoretical positions of the fundamental and 2nd harmonic peaks. The magnitudes of the potentials deduced from zero bias curves are shown in table 6.2. Potentials as a function of gate bias are shown in graph 6.11 for two oscillations, together with plots of potentials from one of the deep devices (A659, 400 nm) for comparison.

Two devices with 100 nm superlattices were measured. They had the same cut-off voltages and similar CO which decreased with the application of negative gate bias. These CO were similar to A881 100 nm lateral data.

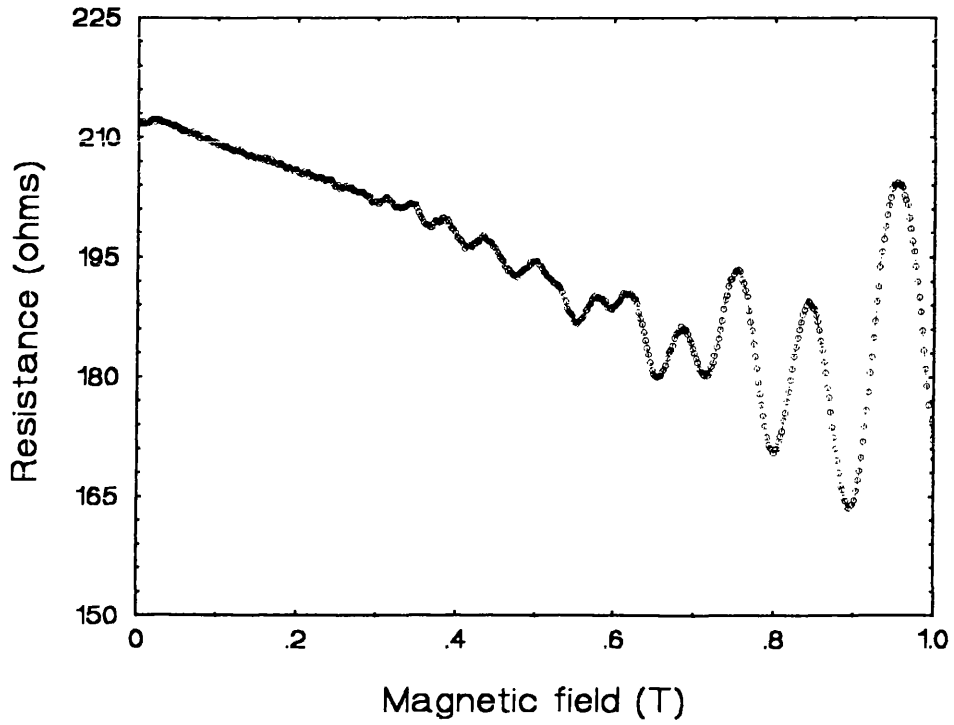
6.3.3 Measurements of shallow AlGaAs devices (B591, A916, B466).

Four devices with a superlattice period of 60 nm were measured in this category. The magneto-resistance measurements on these devices did not show any sign of CO, although it was possible to cut-off the channel by applying negative bias to the gate.

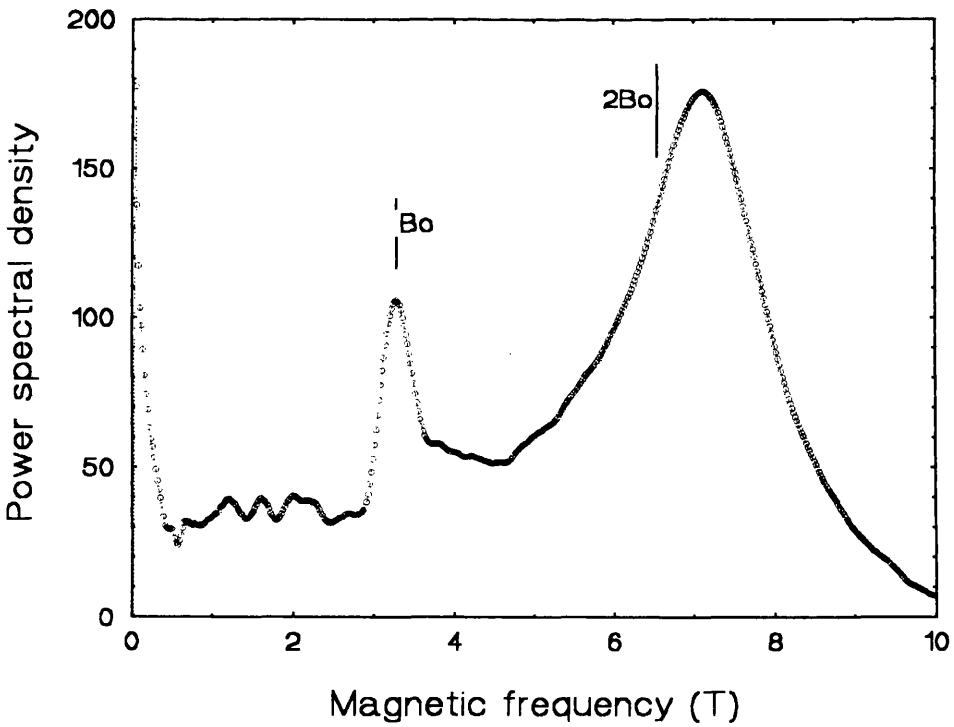
6.4 Summary and discussion.

6.4.1 Introduction

There were two main objectives of this work. The first was to make a study of the strength of the potentials, V_0, seen by the electrons through different layers. This information was obtained by analysing the CO using the Beenakker formula.



Graph 6.9 A858 60 nm superlattice SdH data for Vg=0



Graph 6.10 A858 60 nm Fourier transform
The peak at 6.8 T is from the SdH oscillations

Secondly, it was hoped to probe for the existence of quantum effects predicted when the applied periodic potential was close to the Fermi wavelength. The first objective was partially met. Information was obtained as to the size and origin of V_0 from experiments on deep AlGaAs and shallow AlAs materials. However, disappointingly, experiments on the devices fabricated on shallow AlGaAs materials did not reveal any CO. No evidence of quantum effects was seen on either of the shallow device types so the second objective was not achieved.

6.4.2 Experiments that showed semi-classical behaviour

a) Analysis to obtain V_0 using Beenakkers formula.

Experiments on A448 (graphs 6.1 and 6.2) showed strong CO on both 200 nm and 300 nm devices. The CO did not vary with gate bias. These CO were analysed and gave potentials of 0.14 mV and 0.21 mV respectively. The lack of effect of gate bias on the zero magnetic field resistance and the strong CO are evidence that there are breakages in the strips of metal making up the superlattice. This occurs where they climb onto the channel from the etched area through a height of 100 nm. The material is deep, too deep for harmonics due to the strain potential to be evident. The observed CO most likely reflect some charging effects of the isolated superlattice together with a possible a strain component. Of interest in this device is the strong second harmonic element in the 300 nm data which is a result of the 1:2 mark:space ratio having a much stronger second harmonic element than the 200 nm which has a 1:1 mark:space ratio.

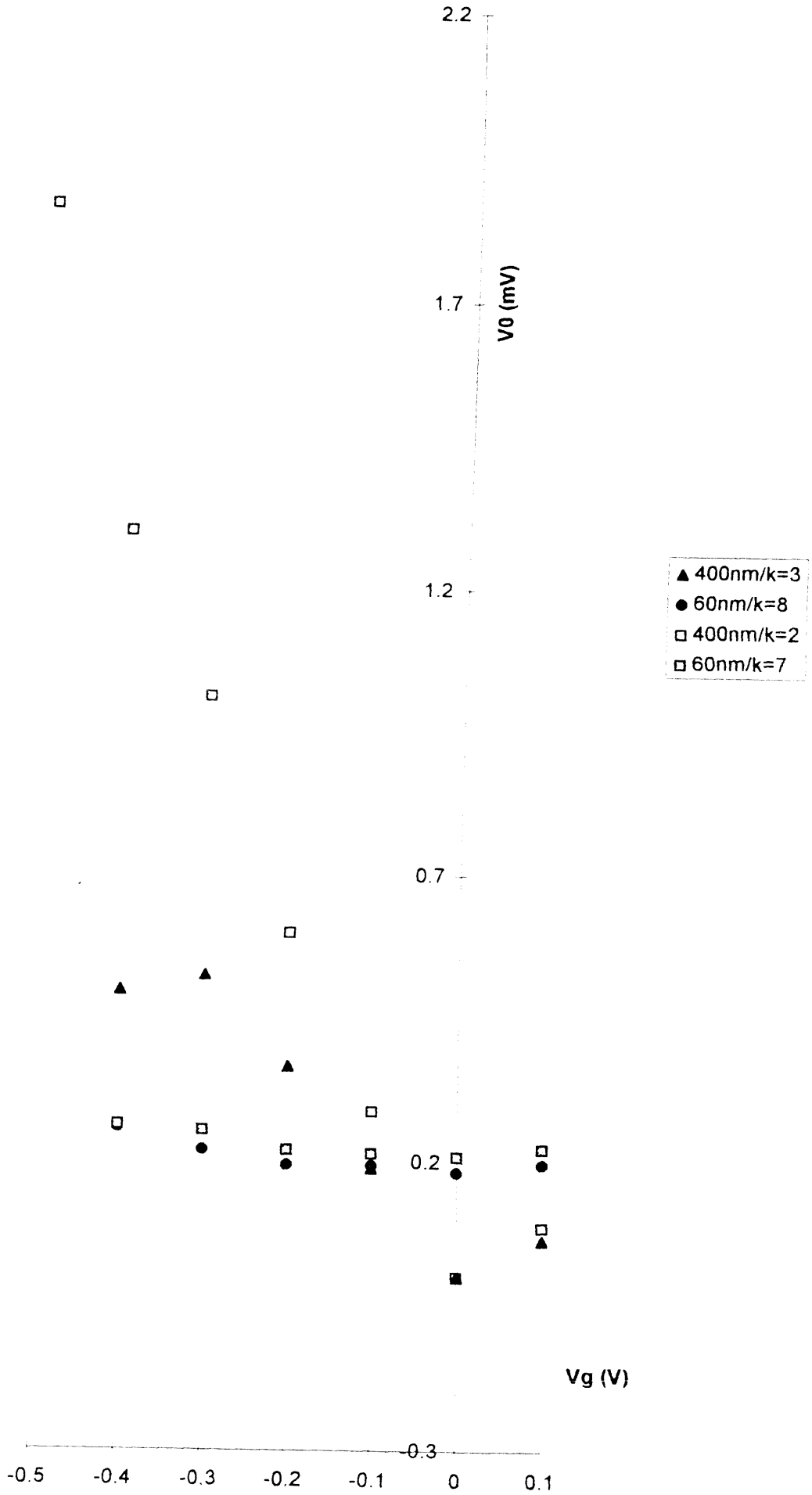
To overcome the problem of the broken connections, devices were fabricated with gate connections on top of the channel (fig 6.2). The A659 device consisted of a series of three gates on an A type Hall-bar with reduced channel width of 20 μm. These superlattices were fabricated for mark:space ratios of 1:1, 1:2, and 1:3 to investigate further the extra harmonic content. The CO observed in these devices were obscured by a rapidly increasing positive quadratic magneto-resistance. The rate of increase of this magneto-resistance becomes larger with negative gate bias. This is

shown on graph 6.3 for the 400 nm device. These results are in agreement with the predictions of Geim et al [7] who found that the increase in magneto-resistance is the result of differing carrier concentrations between gated and ungated areas.

The A659 CO were analysed and potentials obtained from them. In the 200 nm superlattice data, there is evidence of CO at zero gate bias and when analysed these gave a small V_0 of 0.06 meV. This possibly reflects a small component of strain potential due to a larger width of metal on this gate. SEM work showed that the gate strips had been overexposed due to the effect of the proximity of neighbouring strips, and the mark:space ratio was greater than expected. This effect was most acute on the 200 nm device. When bias is applied to the gate of this device the CO die away. The reason for this behaviour is not understood.

The 300 nm and 400 nm superlattices have no CO at zero gate bias and increasing CO amplitudes with negative or positive gate bias. It was hoped to compare the results of devices fabricated on deep materials with those obtained on shallow materials to show how the effect of the proximity of the electron layer to the superlattice leads to an increased value of V_0 in the 2DEG. Graph 6.11 shows a comparison of the potentials deduced from two oscillations of the 400 nm A659 data and two oscillations from the 60 nm A858 experiment (shallow AlAs barrier material). It can be clearly seen from this data that the origin of V_0 is different for shallow devices compared to deep devices. For shallow devices, the potential increases at a much smaller rate with negative or positive gate bias. For the deep devices on the other hand, V_0 is dominated by the potential due to charging the gate, bias since it increases rapidly and linearly with negative gate bias.

The effect of small angle scattering can be seen on the k = 3, 400 nm data where the rate of increase of the potential decreases at large negative gate bias values. This is because the k = 3 oscillation has a larger cyclotron radius than k = 2 and the electrons



aph 6.11. 400 nm and 60 nm potentials with bias. High *k* values are chosen for the 60 nm nple to avoid errors calculated in the potential caused by the SdH oscillations.

are more likely to be scattered. The observed CO become smaller as the effective mean free path is reduced at negative bias, in agreement with Bøggild et al [3].

The other shallow AlAs barrier lateral superlattice devices have a similar value of V_0 to the A858 devices at zero bias. However, the effect of gate bias differs between devices fabricated at different times. With some devices, such as the A858 60 nm period superlattice devices mentioned above, V_0 increases slowly with bias. In others, such as A881 shown in graph 6.8, V_0 decreases with bias. Other shallow AlAs barrier devices measured at Glasgow showed a marked decrease then increase of potential with increasing negative gate bias [6]. One of my devices, the 100 nm square on A881, shows this dip then rise in the potential with negative gate bias. The potentials deduced for the square superlattice device for all analysable experimental traces for k = 6 are also shown in graph 6.8. The amplitude and number of the CO are not otherwise significantly different from the truly lateral (as defined in section 6.1.2) A881 100 nm device (they have the same B_0, harmonic content and similar B_C). This device was fabricated with the lateral superlattice first, then the longitudinal superlattice evaporated as a separate layer afterwards. The first layer seems to be dominating the transport with the second level in poor contact with the surface, although it may provide a better connection to more strips of the lateral superlattice producing the shift in threshold voltage (-3 V for lateral, -1 V for the square).

The decrease then strong increase, with negative gate bias, in the magnitude of the potential observed in other devices measured in Glasgow is seen in graph 6.8 for the square superlattice device. The strong rise in V_0 at large negative biases corresponds to the full unscreened electrostatic potential from the applied negative gate bias acting on the 2DEG once the screening electrons have been depleted.

However the initial reduction in potential with bias is more difficult to explain. Here there is strong evidence for the dominant potential at zero bias being of opposite sign to the applied bias. When negative bias is applied it acts in opposition to the zero bias

potential, reducing the magnitude of the potential seen by the electron layer. Because strain interacting via a deformation potential cannot account for the magnitude or the sign of V_0 it seems unlikely that this is the dominant mechanism. The potential is more likely to be due to strain coupled to the 2DEG via the piezo-electric effect. The piezo-electric effect successfully explains the two types of variation with gate bias seen in Glasgow. The variation of V_0 with negative gate bias is dependent on the device orientation and the electrostatic component either subtracts (shown in fig 6.9) or adds (shown in fig 6.10).

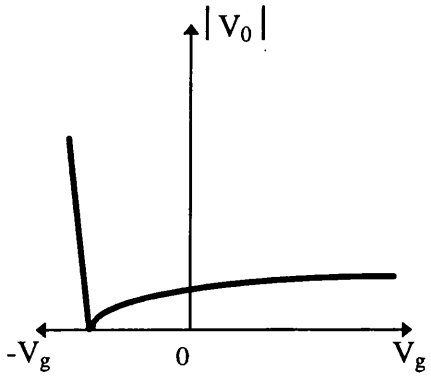


Fig 6.9 Resultant potential for the Piezo- electric potential opposing the electrostatic potential

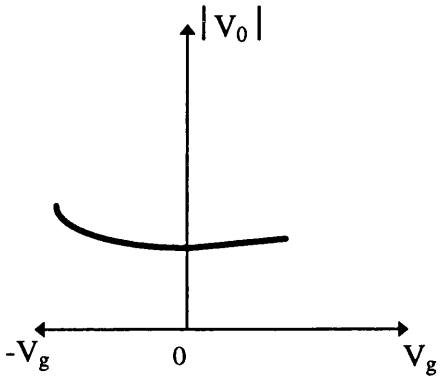


Fig 6.10 Resultant potential for the Piezo-electric potential adding to the electrostatic potential

b) Analysis of V_0 using the low field peak B_C.

Potentials obtained from the low field magneto-resistance peak B_C (equation 6.2) are shown in table 6.2 and compared with values calculated from the amplitude of the oscillations (equation 6.1).

Device	2DEG depth [nm]	Period [nm]	Gate voltage [V]	V_0 (Beenakker) (± 0.02) [mV]	V_0 (Beton) (±0.04) [mV]
A448	92	200	no gating	0.14	0.30
		300	no gating	0.21	0.45
A659	92	400	0	0	0
			-0.2	0.60	0.87
			-0.3	1.01	1.18
			-0.4	1.30	1.50
		300	0	0	0
		200	0	0.06	0
A858	28	60	0	0.21	0.05
		100	0	0.39	0.27
A881	28	100	0	0.62	0.55
		100 (squares)	0	0.54	0.56

Table 6.2 showing V_0 calculated from Beenakker (equation 6.1) and Beton (equation 6.2). B_C was obtained from the low field peak in the magneto-resistance data and used in equation 6.2 to find V_0.

It can be seen from table 6.2 that the potentials obtained from the low field magneto-resistance peak using (6.2) are generally in reasonable agreement with V_0 obtained from the CO. The best results are for A881 which are very close. The agreement between the potential calculated from equations (6.1) and (6.2) for the A659 400 nm device is good, both in magnitude and in trend with gate bias.

c) Calculation of V_0 using the positive quadratic magneto-resistance.

The A659 devices showed rapidly increasing magneto-resistance, which closely followed the B^2 behaviour predicted by Geim et al [7]. The potentials were obtained from this quadratic term for the 400 nm device. (A magneto-resistance trace was shown in graph 6.3). This device best meets the required condition $a >> R_c$. Graph

6.12 shows the potentials calculated from the equations of Beenakker (6.1), Beton et al. (6.2), and Geim et al. (6.3). The magnitudes of the potentials increase approximately linearly with gate bias and show reasonable agreement.

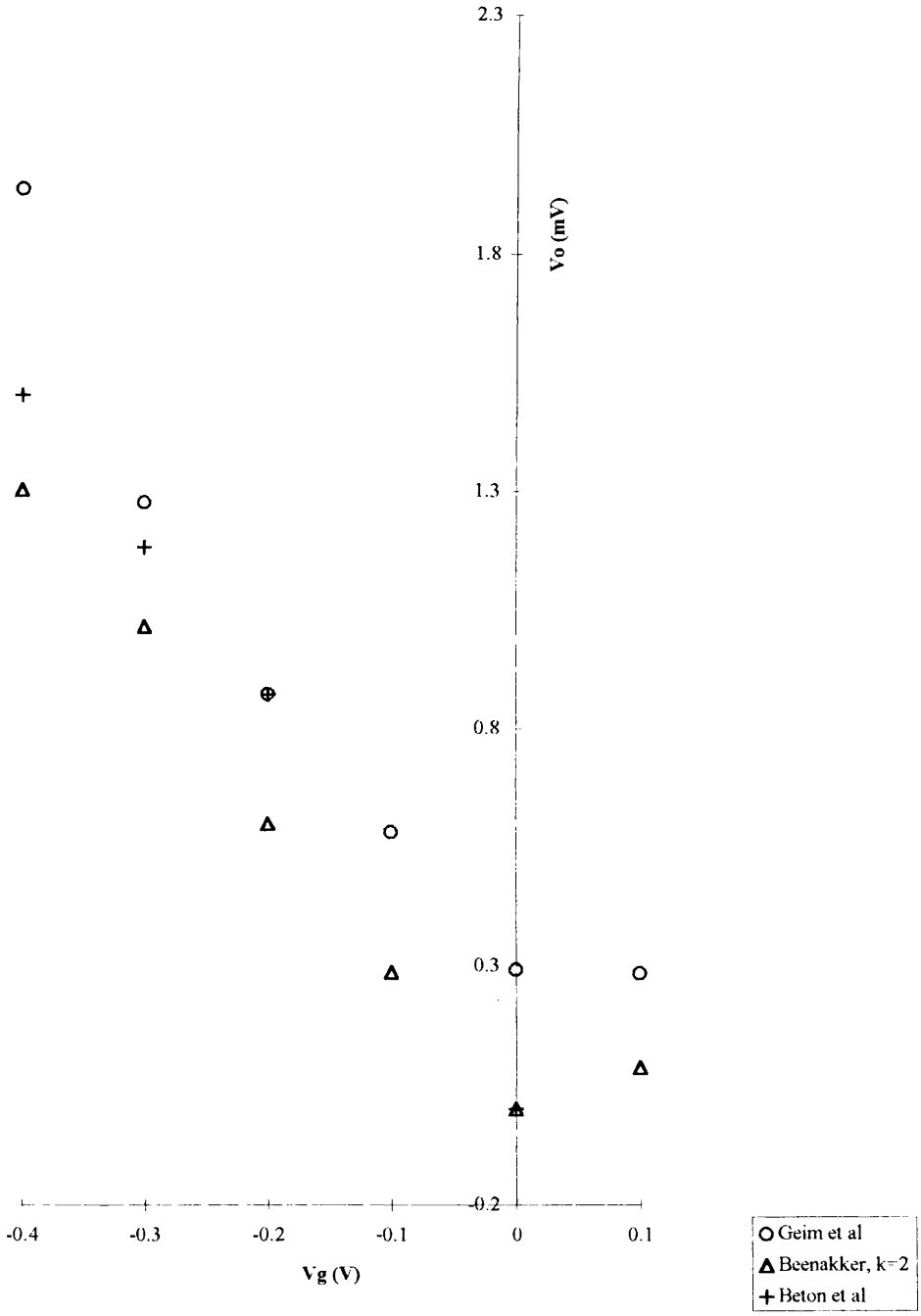
d) Prediction of the position of B_0 using equation 6.4.

Equation 6.4 predicts the position of minima in the CO for a given period of superlattice. By considering two minima n and $n + 1$, writing R_c in terms of B, then substituting $\Delta(1/B_n\text{-}1/B_{n+1})$ and subtracting to eliminate n, equation (6.4) was rearranged to give: $a = \{2\hbar(2\pi n_{2d})^{1/2}\}/eB_0$. Using the measured value of the peaks in the Fourier transform, the periodicity of the CO may be compared to the actual physical value for the device (the actual period written by the beamwriter is very accurate). Periods obtained from devices measured are shown below in table 6.3.

Device	a (actual) (nm)	B_0 (T)	Carrier Conc. ($\times 10^{15}$) m^{-2} $\pm 0.1\times 10^{15}$ m^{-2}	a (calc.) (nm) ± 5 nm
A448	300	0.644	2.7	266
	200	0.935	2.8	186
A659	200	0.995	2.9	180
	300	0.680	3.0	265
	400	0.528	3.0	342
A858	60	3.220	3.5	59
	100	2.020	3.6	100
A881	100	1.886	3.3	100
	100 (squares)	1.790	2.9	99

Table 6.3 Table showing comparison of fabricated and measured period a.

Equation (6.4) accurately predicts a for the smaller periods, with agreement becoming less good as the period increases, e.g. the 400 nm A659 device is in very poor agreement. It is not known why this is the case. Possible reasons such as hysteresis in



Graph 6.12. Comparison of 400nm potential calulated using 3 different theories

the measurement system or varying harmonic content were investigated. Hysteresis was investigated and discounted because there was found to be no difference between measurements at the beginning of a series of measurements and after a series of measurements. Harmonic content was discounted because there was no difference in the error between devices which do have a large harmonic content (such as A448 300 nm superlattice device) and those which do not (such as the A659 300 nm superlattice device).

6.4.3 Experiments which did not show semi-classical behaviour.

a) Deep A648 devices with large 1000 nm period superlattice.

The largest periods of superlattice fabricated were 1000 nm and 2000 nm on both deep and shallow materials. These failed to show CO. The main motivation for these experiments was for comparison with the results of the finger superlattices in the last chapter but it was also hoped to observe CO, especially with the deep devices. The mean free path is larger than the applied potential period in these devices but still no CO were observed, although a peak which may correspond to B_C was seen. The strong positive magneto-resistance seems to suggest a strong potential from the superlattice in the 2DEG even at zero bias. These devices are of the same period as in the experiments by Geim et al [7] who also observed little evidence of CO and a strong magneto-resistance. The strong positive magneto-resistance was also observed in the shorter period A659 devices (see the section above). The strong positive magneto-resistance has its origin in the difference in carrier concentrations between gated and ungated regions distorting the cyclotron radius and leading to drift of guiding centres along the equipotentials. However unlike the experiments by Geim et al. or the A659 measurement, the magneto-resistance observed varies linearly rather than with the square of magnetic field.

b) Shallow AlGaAs barrier materials

After the failure of shallow AlAs small period devices to show miniband effects, several small period shallow AlGaAs barrier devices were prepared with a superlattice period of 60 nm. These devices failed to show any signs of classical CO,

with or without bias. The reason for this is unclear. The cut-off voltages of these devices were not consistent with each other and were much larger than predicted theoretically. This suggests that there are problems with the connections to the superlattice, either where the gate comes onto the channel or in the superlattice itself (on the channel). SEM photos do not show any significant breaks in the fingers on the channel. Breaks at the edge of the channel are more difficult to see. However, if such breaks were present, then it is likely that some CO would be observed (as with the deep A448 devices, where the superlattice charges to some voltage giving strong CO Even with some kind of breakage in the superlattice, it would be expected (as was seen on the shallow AlAs barrier material devices) that some kind of non-electrostatic modulation (such as strain coupling through the piezo-electric effect or the deformation potential) would be present. This is not so, and is a mystery since recent work [14] found that strain effects are also present in deep AlGaAs materials.

Two of these devices did show a quadratic magneto-resistance as observed by Geim et al [7]. These devices were analysed and V_0 obtained. This analysis should not be exactly applicable here, because here at 1T, where the analysis was made $R_c \sim a$ and the analyses of Geim et al. requires $a >> R_c$. However the potentials obtained do vary linearly with gate bias, and as expected are larger for the shallower AlGaAs layer A916 (up to 4.5mV) than for the intermediate depth layer B591 (up to 2.5mV). As noted above, it is likely that the superlattice is not well defined, most likely due to breakages where the strips climb from the etched areas to the channel. Equation 6.3 is independent of a, the superlattice period, so the positive magneto-resistance observed could be a result of random connected strips, which would explain the lack of CO.

6.5 Conclusions.

The aims of the lateral superlattice experiments were to investigate the origin and the strength of the periodic potential V_0 in shallow materials, and to push towards the limit in which the period of the superlattice is close to the Fermi wavelength. The investigations of V_0 have been partially successful, with a number of layers measured and the origin of the potential investigated. In deep devices the electrostatic potential resulting from the applied gate bias was found to dominate. This potential was calculated from measurements of one device using three different methods. Reasonable agreement between the three approaches was found both in magnitude of the potential and variation with gate bias. The results from the deep devices were compared to measurements of devices fabricated on shallow AlAs barrier materials, where the dominant source of the potential is thought to lie in a strain field caused by differential contraction between the gates and the surface of the GaAs during fabrication. It had been originally intended to compare the experimental results with the Davies and Larkin model. However when screening was included the model based on a deformation potential coupling via the strain could not account for the magnitude of the potential observed, or the variation of V_0 with gate bias. The dominant source of potential is now believed to be due to strain coupled via the piezo-electric effect. None of the devices showed quantum effects, although splitting of the Landau levels has recently been seen by the Munich group [15] in an array of antidots formed on the layer B466, a shallow AlGaAs sample used in this work for the 60 nm superlattices.

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Chapter 7

Conclusions

7.1 Introduction

In this work many layers were patterned and characterised. A few were found to be of good enough quality to fabricate gate structures on them. The resulting devices consisted of either a longitudinal type using HRN resist ribs and an overlying Schottky gate, or strips of metal fabricated in a periodic array across the Hall-bar channel.

Initially shallow AlGaAs barrier samples were used for the longitudinal work and shallow AlAs barrier materials were used for the superlattice work. Later a number of lateral superlattice devices were fabricated on shallow AlGaAs barrier material and some were also fabricated on conventional deep bulk doped materials (which also had AlGaAs barriers).

7.2 Devices measured for experiments with a gate structure using HRN (High resolution negative resist).

Three sets of devices with HRN longitudinal wire structures were measured. These were fabricated on Hall-bars. Measurements were made at 1.5 K.

The main purpose of these measurements was to find evidence of 1D confinement. Magneto-resistance data was examined for evidence of quantum confinement in the wires. The threshold voltages of the devices were compared to values from a simple model which was derived from electrostatics. The cut-off voltages were compared to the theoretical values obtained from two models, assuming respectively 'pinned' and 'frozen' surfaces. It was expected that the results of the experiments would give

conclusive evidence as to which model correctly described the behaviour of the devices at low temperatures.

The first devices (fabricated on sample type A707) consisted of 100 or 250 nm wide HRN strips with a 500 nm period across a channel 100 μm wide. The measurements on these wires did not show any evidence of 1D confinement. The threshold voltages were not consistent between devices and did not agree well with the theoretical value obtained from simple electrostatics. The results of the measurements of cut-off voltage also did not agree well with the values predicted by either of the two theoretical models (the pinned and frozen models).

The second set of devices measured (on sample type A866) were fabricated with a channel width of 200 μm. The gate structure on these devices was of 2000 nm period with 200 nm wide HRN strips. These devices also failed to show any evidence of 1D confinement. Resistance measurements on these devices showed a consistent value of V_t for wire and big-gate devices. This value of V_t was also in better agreement with the theoretical V_t than for the A707 results. The cut-off voltages were in poor agreement with the cut-off voltages calculated from either the pinned or the frozen model.

The last set of devices measured with HRN ribs were fabricated on the layer A909. These were of the same structure as the A866 devices, but this time used a Hall-bar with a 200 μm channel width. These devices did not show any evidence of 1D quantum confinement. The cut-off and threshold voltages did not show good agreement with the values obtained from theoretical models.

In conclusion, none of the experiments carried out with HRN longitudinal ribs showed any evidence for 1D quantum confinement. Experimental measurements of threshold and cut-off voltages were inconsistent between nominally identical devices, or agreed poorly with the threshold and cut-off voltages obtained from theoretical models. We believe the poor results obtained from these devices were due to surface

contamination problems. The most likely source of this contamination was HRN exposed by backscattered electrons during the writing of the wire ribs.
The problems encountered with fabrication suggest that longitudinal wires fabricated with HRN are unlikely to be of any use in the future.

7.3 Devices fabricated with a gate structure consisting of a periodic array of fingers

After the unsuitability of the HRN longitudinal devices for testing theoretical models of the cut-off voltage was shown, gate fingers were fabricated which would electrostatically confine electrons in narrow wires without the need for HRN. They could not be used for 1D measurements because of the layout of the gate structure. These devices were fabricated with positive resist and consisted of a periodic array of fingers connected together at one side of a Hall-bar channel. There was a space between the ends of the fingers and the other side of the Hall-bar channel which allowed access to the regions between the fingers for electrons from the ungated areas of the Hall-bar.

The first measurements on devices with a gate structure to this lateral finger design were on two devices fabricated on sample A909. This was a shallow AlGaAs barrier material. These devices had threshold voltages which were consistent for the two devices, but which did not agree well with the values calculated from the simple model derived from electrostatics. The cut-off voltages were also consistent for the two devices, and were in better agreement with the frozen model than the pinned model. The measured and theoretical capacitance of these devices were in very poor agreement, suggesting that there were breakages in some of the fingers.

The second set of finger measurements were carried out on devices fabricated on an intermediate depth material, B591. These devices showed very good agreement between theoretical and measured threshold voltages. The cut-off voltages from these

devices were in closer agreement with the frozen model. There was, however, a large variation in the measured values of cut-off voltage between devices. There was good agreement between the theoretical and the measured values of capacitance.
The last device measured in this series was fabricated on a "standard" deep sample, A648, bulk doped and with AlGaAs barriers. There was good agreement for these devices between the calculated and measured values of threshold voltage. Measured cut-off voltages showed better agreement with the frozen theoretical values. The agreement between measured and calculated capacitances is not good on these devices.
Two big-gate devices were also measured using sample A648. These devices had capacitance values which were in better agreement with theoretical capacitances than the finger devices. It is likely that the reason for the low capacitance values observed for A648 finger devices is due to breakages of the fingers.

These measurements support the hypothesis that the more physically realistic frozen model correctly describes the ungated areas of GaAs at low temperatures. There were problems with the measurements in that the capacitance values measured on devices using samples A648 and A909 gave very poor agreement with theory. The most likely explanation for this is breakages of some fingers of the NiCr gates.

7.4 Measurements on Lateral surface superlattice devices.

The primary objective of the measurements of lateral surface superlattices was to try and find evidence of new physical effects. These effects are predicted when the period of the lateral surface superlattice is of the order of 50nm. An additional objective was to study the variation of the potential with bias for different depths of two dimensional electron gas and types of barrier material.

Lateral surface superlattice gates were fabricated on Hall-bars. Deep AlGaAs bulk doped layers, shallow AlGaAs barrier layers and shallow AlAs barrier layers were all used. Magneto-resistance measurements were made. By analysing the amplitudes of the commensurability magneto-resistance oscillations (CO), the potential induced by the gates could be derived.

On the deep layers, superlattices were fabricated with periods of between 200nm and 2000nm. CO were observed on devices fabricated with superlattice periods of between 200nm and 400nm. The perturbing potentials deduced were found to vary linearly with gate bias. Two other techniques were also used to derive the potentials induced by the gates, a) analysis of the low magnetic field peak in the magneto-resistance due to open streaming orbits and b) analysis of the background quadratic magneto-resistance. The three methods for finding the potential gave consistent results.

On the shallow AlAs barrier layers superlattices were fabricated with periods of 60nm and 100nm. No quantum effects were seen in measuring these devices. This was most likely because of the layer of electrons around the donors screening the two dimensional electron gas from the electrostatic potential. Information about the magnitude and variation of the potential with gate bias was obtained from the magneto-resistance measurements using Beenakker's formula. All the measurements on AlAs barrier devices showed CO at zero bias. The potential obtained from these measurements is calculated to be of the order of 0.5 mV. This modulation was due to the electrostatic potential which results from strain. This strain had its origin in the different rates of cooling of the NiCr gates and the GaAs crystal surface after the evaporation of the gates. This strain was coupled to the 2DEG either via the deformation potential or the piezo-electric effect. When negative bias was applied,

the magnitude of the potential either increases or decreases slowly. The sign of this variation in potential was dependent on the device measured. It could not be explained by the strain being coupled via the deformation potential and this variation provided evidence that the strain is coupled via the piezo-electric effect. This is because device orientation on the crystal determines whether the potential from the applied bias will add or subtract to the potential from the strain. As the bias was made more negative a sharp increase in the potential was seen on one device measured. This sharp increase corresponded to a point where the layer of electrons around the donors was depleted.
The variation of potential with gate bias observed is consistent with previous work on devices fabricated on shallow AlAs barrier materials.

Some 60 nm period superlattices were also fabricated on shallow AlGaAs barrier materials. Shallow AlGaAs barrier materials have a lower mobility but have an advantage over shallow AlAs materials in that the electrostatic potential from gate bias is not significantly screened by the layer of electrons around the donors. Several 60 nm superlattices were fabricated on shallow AlGaAs materials. These did not show any sign of classical commensurability oscillations or quantum effects. This was most likely due to breakages in the superlattice where it climbed onto the surface of the Hall-bar channel.