MODERN VLSI ANALOGUE FILTER DESIGN: METHODOLOGY AND SOFTWARE DEVELOPMENT

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SUMMARY

This thesis describes various approaches for the design of modern analogue filters and provides a practical filter and equaliser design aids system XFILT.

The thesis begins by placing the analogue filter design technique and software into a historical and technology perspective. The evolution of the analogue filter is traced from early work, through the passive-RLC to transconductor-C and switched-current realisations. The software development in VLSI analogue filter automation is reviewed.

For SC filter design, a cascade SC design approach which includes a novel pole-zero pairing method and a comprehensive comparison of SC filter realisation using different biquads are presented. Very useful guidelines for the choice of a suitable biquad structure according to the nature of the filter problem are presented. The canonical realisations of SC filter are studied. The multirate SC system design is described. Several strategies and the algorithms for multirate SC system design are proposed.

In transconductor-C filter design research, the definition of a canonical ladder based transconductor-C filter is introduced, and two canonical ladder based transconductor-C filter design approaches are proposed. The ladder based transconductor-C equaliser design is also discussed. A practical video frequency transconductor-C filter and equaliser design is given to demonstrate the utility of the matrix design method and the design software.

A new approach to realise exact ladder based SI filter with first and second generation memory cell has been proposed. The bilinear transformation is used in the design procedure. Eight different SI ladder based structures can be obtained for

one prototype ladder. Therefore it provides SI filter designers with various circuit choices based on different requirement such as area, maximum ratio of transistor aspect ratio limit, sensitivity or noise performance. Techniques to improve dynamic range and reduce circuit parameter spread are also presented. The proposed approach is well suited for a computer compiler implementation. A suitability study of each decomposition method for different filtering applications is also carried out and a general guideline for the choice of different decomposition methods is obtained.

A comparison study on SI filter sensitivity performance based on first generation and second generation memory cells is carried out. Using four filter examples, it is demonstrated that SI filters based on a second generation SI memory cell have good sensitivity performance. For SI filters based on first generation memory cells, it is shown that a high ratio of clock frequency to cutoff frequency in the lowpass case, or a high ratio of clock frequency to midband frequency in the bandpass case would introduce high sensitivity.

A novel approach for SI ladder filter based on the S^2I integrator is also proposed and a canonical realisation for SI filter based on S^2I integrator is developed. Examination of SI equaliser design reveals that cascade structure is a better candidate than ladder based structure. Multirate SI filter system design is also studied.

Finally, a very brief introduction to the assembly of the design methods in this thesis into a software package XFILT for VLSI analogue filter and equaliser design is given. The user aspects of XFILT have been discussed and various capabilities of XFILT are demonstrated. Several advanced facilities which remove traditional design limitations are illustrated. The philosophy of the system is explained. It is shown that the distinguished features of XFILT are **Ease of Use**, **General Applicability**, and **Ease of Extension**. The system structure is described and the

graphics interface which acts both as user friendly interface and a system manager of all the software is outlined.

Fabricated SC, transconductor-C, and SI filter and equaliser have been designed by using XFILT. The system is under further enhancement toward a commercial product.

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Chapter 1: Introduction

CHAPTER 1: INTRODUCTION

1.1Background

Electronics is, and certainly will continue to be, a dominant force in shaping our world. Electronics, in particular microelectronics, is involved directly or indirectly in every facet of our daily activities. Applications are wide and diverse, ranging over communication, business, defence, education, entertainment, health care, space exploration, transportation, and various other areas. The use of electronics began in the early twentieth century and almost from the beginning, the electrical filter has been an important part of most electronic systems.

An electrical filter processes an electrical signal applied to its input such that the signal at the output has desirable properties according to the specifications in a particular application. In some applications, the filter is an electrical network exhibiting frequency selective properties. Such a network may be used to pass certain frequency components and stop other frequency components in the input signal. In this case, the processed signal appearing at the filter's output contains essentially the frequency components that are allowed to pass through without much degradation. A frequency selective filter may also be used to compensate for the dispersion caused by a transmission medium such as the wideband cable and its inevitable reflection due to mismatching so that the overall system appears close to an ideal transmission channel with a constant delay. There are applications where the filter is designed to exhibit specific time-domain characteristics. In fact, presently, any electrical network designed to develop a specific response, whether in the frequency-domain or in the time-domain, for a given excitation is called a filter.

Generally speaking, filters can be classified into two broad groups: continuous and sampled-data. This classification is primarily based on the type of electrical signal being processed by the filter. In continuous filters the signal is a continuous function of time with its amplitude at each instant of time being permitted in principle to take any value. In a sampled-data filter, on the other hand, the signal is sampled and processed at discrete instants of time that usually occur at equally spaced intervals. This latter type of filter can again be one of two types. In one type, called analogue sampled-data filters, the sampled signal in principle can take any value, whereas, in the other type, called digital filters, the sampled signal is further discretized and can take one of a fixed number of quantized values represented by binary numbers. This last type of signal is commonly called a digital signal in contrast to the none-digitized ones which are referred to as analogue signals.

The circuit techniques for filter implementation are very variable[1]. Presently, technologies used to construct continuous analogue filters include passive lumped RLC, mechanical, crystal, surface acoustic wave (SAW), active-RC, transconductor-C, OTA-C, and integrated active-RLC. Circuit techniques in use for implementing sampled-data filters are charge-transfer device (CTD), switched-capacitor (SC), switched-current (SI) and digital.

1.2 VLSI Filters

The origin of electronic filters dates back to 1915 when K.W.Wagner in Germany and G.R.Campbell in the United States independently introduced passive electric wave filters to meet the needs of the young communications industry. Since then, there have been significant and continuous advances in filter theory and technology along with the broadening of the term filter. Before 1960s, the dominant technology was the passive lumped filter which consequently received the most attention with regard to the development of the both theory and practice. However, as the passive

lumped filter technology reached a plateau with respect to performance, size, and cost reductions, a number of developments precipitated the search for different filter technologies. The rapid growth of the telecommunication industry along with the use of filters in various other systems, increased the market for filters; many applications required filters with more exacting performance characteristics; and furthermore, high volume production at low cost of some types of filters required technologies offering higher precision in tuning and stability over time and required temperature ranges.

The passive lumped LC filter technology was introduced first. It is based on the interconnection of discrete elementary components consisting of inductors, capacitors, and resistors. Here electrical resonances are provided by tuned circuits composed of inductors and capacitors. Since its introduction in 1915, the passive LC filter technology has dominated in most applications until about 1965[2].

The development of silicon integrated circuit technology in the 1960s led to an extensive search for the design of inductorless filters for very low frequency applications where inductors tend to be bulky and expensive. With the availability of monolithic operational amplifiers in the mid-1960s, filters were designed using these amplifiers together with discrete resistors and capacitors. They are more commonly called active-RC filters and became an attractive alternative. The introduction of computer-controlled laser trimming of thin-film and thick-film resistors provided a convenient way of adjusting the performances of active RC filters and thus led to an increased use of these filters in low frequency, high-volume applications[3][4]. However, attempts to directly fabricate active-RC filters in monolithic form were not successful for two reasons: (1) the need for large resistors and capacitors (especially for low frequency filters), and (2) the need for accurate RC time constants.

Due to the difficulty in making fully integrated resistors, active RC filters were not amenable to fabrication in monolithic form on one silicon chip. The search thus continued to develop active circuits without inductors and without resistors. There are two main streams for the implementation of precision analogue filtering functions in monolithic integrated circuit form. Although both approaches use MOS technology, they differ in a fundamental way: while in one (Transconductor-C, and MOS-C) the analogue signal is processed directly in its continuous-time form, the other approach (SC and SI) is based on processing samples of the analogue signal and thus the resulting circuits are discrete time or sampled data systems.

The switched-capacitor filter was proposed in late 1970s[5]. It is generally agreed that the paper by Freid[6] was one of several that gave a major impetus to the development at Berkeley of the first MOS switched-capacitor filters. Certainly this is the first paper to recognise the potential of the MOSFET technology, in the form of switches and capacitors for the realisation of integrated simulated RC filters. Nevertheless, this idea did not grow out of a vacuum. Much work on related concepts had been published previously one to two decades earlier[7,8]. However, only after [9] and [10] had been published, was the full impact of this new filter technology appreciated by the circuit community at large. For many applications, the difficulties faced by active-RC technique have been overcome by the development of SC technique. In an SC filter the scaling in frequency is set by capacitor ratios as a fraction of a reference clock frequency. So a transfer function can be implemented which is scaled correctly in both magnitude and frequency to the accuracy of capacitor matching (of the order of 0.1% in a good process). SC filters have been applied successfully to many applications and are used routinely in analogue CMOS circuits.

There are however a number of application areas, such as video signal processing, in which they are not easily applicable for SC filters due to the high signal frequencies

involved. Another drawback of SC filters in high frequency applications is the fact that they are sampled data in nature. Some applications, such as anti-aliasing filtering for video ADCs, require a continuous time solution. This motivated the continued search for a type of monolithically integrated filter which is accurately tunable, continuous time, and which can operate at high frequencies. Depending on the circuit implementation, continuous-time filters can be classified as MOSFET-C filter[11] and transconductor-capacitor filter[12,13,14]. In these filters, the scaling in frequency is set by the ratios of Gm to C.

The switched-current (SI) technique proposed by Hughes et al[15,16] to perform sampled-data analogue signal-processing are currently receiving considerable attention. In contrast to the switched-capacitor (SC) approach, which requires a non-standard digital CMOS process to realise floating linear capacitors, the SI technique can perform accurate signal processing functions in a standard digital CMOS process without the direct use of any capacitor. This is an attractive feature due to the tendency toward the integration of large analogue/digital systems in a single chip. Moreover, the SI technique does not utilise CMOS op-amps but rather performs all its analogue signal processing with much simpler current mirrors. It is therefore expected that SI circuits will operate over much wider signal bandwidths than present day SC circuits. Also, the current mode nature of SI circuits should make them less adversely affected by the imminent reduction in power supply voltages.

With the development of communication, the high frequency operation filter has received great attention. Research was carried out again to put inductors on an integrated silicon chip[17]. Since the achievable quality factors in those filters are low, due to resistive losses of the inductor, modified active-RLC version filter are proposed[18,19,20]. It is expected that this kind filter will be able to work in GHz

frequency range. In contrast, some researchers are working with GaAs technology[21,22,23]. The GHz range GaAs filter is also under investigation.

The emergence of complex digital integrated circuits has steadily displaced analogue solutions from many applications. Often, the advantages of digital implementations are overwhelming; they offer programmability, flexibility, additional product functionality, short design cycles and they exhibit good immunity to both noise and manufacturing process tolerances. However, for a digital system to interact effectively with an inherently analogue world, analogue signal conditioning and data conversion circuits are still required. The role of analogue integrated circuits is therefore changing, no longer are complex systems entirely analogue, rather they typically consist of a core of digital signal processing and computation circuits, buffered from an analogue external environment by a layer of analogue interface circuits. Complete analogue systems will still continue to be required in some applications, mainly those in which the frequency of the operation is too high for digital implementation, and those with low complexity that does not justify a digital implementation or in very low power applications.

1.3 Analogue VLSI Filter Computer Design Automation

Design automation of digital VLSI circuits is a relatively mature and well developed area, while design automation of analogue VLSI circuits started slowly in the 80s and has more recently received increased attention from the research community and industry. Although analogue circuits may only take up a minor part of most ASIC's, their design time and cost is very important.

Main aims in the development of CAD tools for filters are:

1. Easy design for system designer. Usually the filter design needs a designer with a sound knowledge of filters, but with filter CAD tools a system designer with little filter knowledge can obtain a filter design with only the specification of the filter as input to the software. This is very important in VLSI design. Here a system is often a large digital circuit with a small analogue interface.

2. Reduced design time and cost. Designs which would take weeks to complete by manual methods can be done in minutes.

3. Quick estimates of silicon area, power dissipation, sensitivity, and noise performance.

4. To provide optimal designs. Improvements may be made to filter attributes such as area, power, sensitivity and noise performance. Important trade-offs at system and circuit level can be considered.

5. To make advanced technologies accessible. New technologies for circuit and filter structures are continually being developed. However, they are often slow to gain acceptance because of the complicated design process. Computer software can ensure that all designs are produced with equal ease and that the use of a given filter structure is not prejudiced by the effort demanded to obtain them.

The use of digital computer in filter design started with LC filter synthesis, approximation and simulation. The theory of LC filter synthesis matured many years ago, and the computer was simply used as a glorified desk calculator to relieve the designer of the drudgery of lengthy numerical computations. The earliest design programs were developed in the 1950s and 1960s for passive RLC filters. When the active-RC filter arrived in the 1960s, they were followed up quickly by computer automation[24]. The most notable software are FILTOR2[25] and FILSYN[26]. In

the late 1970s and early 1980s, the SC filter technique inspired an overwhelming research effort on VLSI analogue filter design automation, and motivated the development of software, such as AROMA[27], SICOMP[28], Auto-SC[29], PANDDA[30], filtorX[31] and SWCAP[32]. Into 1990s, the VLSI analogue filter design automation is continuing to be an active area of research and development. New software capable to design biquad based OTA-C filter[33] has been proposed.

Although filter design tools are available, their acceptance by designers is quite low. The reason is essentially due to the limited capabilities of the tools and to their philosophy, to the missing links between the tools, and sometimes, due to the reluctance of designers to consider new design methods which they do not fully understand.

1.4 General Aim and Outline of the Thesis

1.4.1 General aim of the thesis

The aim of this thesis is to study the design methodology of modern VLSI analogue filter and develop advanced CAD tools for modern VLSI analogue filters. Special attention is paid to SC, transconductor-C and SI filter design. Since the SC filter design automation is a relatively mature area, the research focus is on the SC canonical ladder design, multirate SC system design, and multiple biquad SC cascade design, which are some topics not included in previous SC design software. For transconductor-C filter design, the ladder based filter and equaliser design are studied. In SI filter design, the emphasis is given to develop various ladder based design methods. Finally, but most importantly, the challenge is to develop a modern unified VLSI analogue filter design system XFILT.

1.4.2 Outline of the thesis

This thesis consists of four main parts. Chapter 2, Chapter 3, and Chapter 4 each deal with one particular form of integrated filter, these are SC, transconductor-C and SI realisation. The design software XFILT is described in Chapter 5.

SC filter design is considered in Chapter 2. A novel pole-zero pairing scheme is presented and a comprehensive comparison of biquads in the realisation of SC filters is carried out. Based on the comparison some very useful guidelines are obtained in cascade SC filter design using different SC biquads. Following a brief review of matrix design methods for ladder SC filters, the modified canonical design approach for ladder based SC filter design is given. Multirate SC system design strategies and algorithms are presented in section 4 and are implemented in XFILT. Several SC filter design examples are also given in this chapter.

In Chapter 3, transconductor-C filter design methods are covered. The canonical transconductor-C ladder based structure is proposed. The matrix method for transconductor-C filter and equaliser design is discussed. A video frequency filter and equaliser was designed and fabricated. A number of optimisation strategies are presented.

In Chapter 4, the SI filter system design approach is considered. The novel SI ladder based filter design methods are presented and a suitability study of the proposed approach is carried out. A comparison of SI filters using first and second generation SI cell is given. The results show that second-generation SI memory cell based SI filter have good sensitivity performance. New design methods for S^2I based ladder filter are also proposed and a canonical realisation is presented. The multirate SI system idea is applied and several multirate SI filter systems are given.

The filter and equaliser suite XFILT (X-window based FILTer and equaliser design system) is presented in Chapter 5. This is the first system which has the facility to design passive-RLC, active-RC, transconductor-C, SC and SI filters and equalisers. The system concept, characteristics, structure and implementation are reported. A brief description of design, simulation and optimisation procedures for filter and equaliser designs is presented.

The main features of the XFILT are:

1. User friendly graphical interface
2. SC, SI and transconductor-C filter and equaliser design under one system
2. Multiple ladder structures for active-RC, SC, SI and TC filter design
3. Multirate SC and SI system design capability
4. Powerful simulation facility
5. Global optimisation scheme
7. Classical approximation and arbitary approximation with free or fixed higher order touch point

Finally the main results obtained in this thesis will be summarised in Chapter 6. Some suggestions for further research in integrated filter design and software development will also be given.

1.5 Statement of Originality

The following results of the research work presented in this thesis are, to the best of author's knowledge, original and, as indicated below, some of the results have been or will be published. The contributions of others to the work are acknowledged in the text where appropriate.

In Chapter 2, a novel pole-zero pairing scheme is presented and a comprehensive comparison of biquads in the realisation of SC filters is carried out and useful cascade SC filter designs using different SC biquads are presented. The modified canonical ladder based SC filter design is given. Multirate SC strategies and algorithms is given in section 4 and implemented in XFILT.

Lu Yue and J.I.Sewell, "A comparison study of SC biquads in the realisation of SC filters", Proc. 1994 IEEE ISCAS'94, London, UK, pp.5.711-5.714

Lu Yue and J.I.Sewell, "Multirate SC and SI filter design by XFILT" Proc.IEEE ISCAS'85, Seattle, May 1995

Lu Yue, R.K.Henderson, and J.I.Sewell, "XFILT: An X-window based modern filter and equaliser design system", ECCTD'93, Davos, Switzerland, pp.305-310

In Chapter 3, a canonical transconductor-C ladder based structure was proposed. Complete transconductor-C computer aided system was developed and the video frequency filter and equaliser is presented.

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In Chapter 4, novel SI ladder based filter design methods are presented and the suitability research of the proposed approach is carried out. A comparison of first and second generation SI cell realised SI filter system is given. New methods for S^2I integrator based ladder structure filter are presented and a canonical design method is given. Multirate SI system concepts are applied and several multirate SI filter system are presented.

Lu Yue and J.I.Sewell, "A systematic approach for ladder based switched-current filter design", Proc. IEEE ISCAS'95

Lu Yue and J.I.Sewell, "Multirate SC and SI filter design by XFILT" Proc. IEEE ISCAS'95

Lu Yue and J.I.Sewell, "First or second generation SI cell: A sensitivity comparison from SI filter system point of view", IEE Saraga Colloquium, pp.7.1-7.8, London, Nov.1994

In Chapter 5, the concept of filter design system integration and passive-RLC, active-RC, transconductor-C, SC and SI filters realisation under one design environment is given. Graphics editing function in modern filter approximation is presented. Xwindow, design and simulation integration is considered. More than 60,000 lines C-code are developed for the realisation of XFILT.

Lu Yue, R.K.Henderson, and J.I.Sewell, "XFILT: An X-window based modern filter and equaliser design system", ECCTD'93, Davos, Switzerland, pp.305-310

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Chapter 2: Switched Capacitor Filter Design

CHAPTER 2: SWITCHED CAPACITOR FILTER DESIGN

2.1. INTRODUCTION

Active-RC filters utilise opamps together with resistors and capacitors and are implemented either on printed circuit boards using IC opamps and discrete resistors and capacitors, or as thick or thin film hybrid circuits. Attempts to directly fabricate active-RC filters in VLSI form have not been successful because of the problems due to need for large-values of resistance and capacitance and the need for accurate RC time constants. Switched-capacitor filters are based on the principle that a capacitor periodically switched between two circuit nodes at a sufficiently high rate is approximately equivalent to a resistor connecting the two nodes[1,2,3]. It is thus possible to realise filter functions using opamps, capacitors and periodically operated switches[4]. Since MOS technology provides high quality capacitors, offset free switches and opamps, it is eminently suited for the realisation of SC filters. Two problems encountered in active-RC filter realisation can be easily overcome by using SC circuits. The large resistors can be simulated using small sized capacitors and very precise frequency responses can be achieved by using MOS SC filters since capacitor ratios can be realised to a high accuracy (as good as 0.1%).

The design methods of SC filter have received considerably attention in recent years. A large number of papers have been published[5,6]. SC filter design methods can be divided into three major categories, namely cascade approaches[7,8], ladder based approaches[9-15] and special approaches which are used to design particular

filters such as N-path filters[16], SPFT filters[17], multirate filters[18] and so on or to obtain special performances .

Because of the abundance of design methods for SC filters available in the literature, it is sometimes difficult to decide which method should be chosen for a particular application. For the SC cascade design method, a comparison of different SC biquads in the realisation of SC filters was carried out. When existing biquadratic sections are utilised, the performance such as total capacitance, capacitance spread, dynamic range, sensitivity, non-ideal effect and noise are compared. In the SC ladder design method, a canonical realisation approach is implemented which is of importance due to recent demands for lower power circuit. The final part of the chapter is concerned with multirate SC filter design.

2.2 CASCADE SC FILTER DESIGN METHOD

2.2.1 Cascade SC Filter Design Approach

Cascade design is by far the simplest and most popular method for active filter realisation. The filter transfer function is realised as the voltage transfer ratio of a cascade of filter sections, each having a biquadratic voltage transfer function. An additional first-order section is required in the odd order case.

A high order filter transfer function can be expressed as

$$H(z) = \prod_{i=1}^{n} \frac{d_{i0} + d_{i1}z^{-1} + d_{i2}z^{-2}}{1 + c_{i1}z^{-1} + c_{i2}z^{-2}} \qquad (2\text{-}1)$$

when n is even, there will be n/2 biquads needed for the cascade realisation of the filter. When n is odd, the filter will be realised by (n-1)/2 biquads and a first order section, which has the transfer function

$$H(z) = \frac{d_0 + d_1 z^{-1}}{1 + c_1 z^{-1}} \tag{2-2}$$

The cascade method of design involves two major steps:

Step 1: Decomposing the Nth order transfer function H(z) into the product of second-order (and one first-order, for odd N) factors; that is, $H(z) = \prod_j H_j(z)$.

Step 2: Realising each biquadratic function with a biquad circuit.

The problem of decomposing an Nth order transfer function into the product of second-order, and possibly one first-order, functions may be split into three parts. These are:

(1) Pole-Zero Pairing:

To form second-order functions, each of the (N/2) pole-pairs has to be combined with one of the (N/2) pairs of zeros (including those zeros at zero and s at infinity). There are (N/2)! possible different combinations to choose from.

(2) Cascading Sequence:

Having determined the transfer function of each filter section, to within a gain constant, the question remains as to the sequence in which the sections should be cascaded. Note that since the sections have low output impedance, the overall form of

transfer function of the cascade does not depend on the cascading sequence. There are (N/2)! possible different sequences to choose from.

(3) Gain Distribution:

Given a specified value of total filter gain, the question arises as to how this gain should be distributed among the different sections in the cascade. In other words, what gain level should be assigned to each biquad section? There is an infinite number of possible gain assignments.

Among the many filter performance measures which one may attempt to optimise in solving the decomposition problem, the dynamic range is usually the most important. The solution of the decomposition problem affects the filter dynamic range more than any other performance. For this reason, effort is focused on finding a decomposition that maximises the filter dynamic range. Special programs are developed to solve the pairing problem such that the magnitude of the transfer function over the filter passband for each biquad is as flat as possible. For a specified total filter gain, gain constants are assigned to the various biquads such that the peak of the magnitude of each of the intermediate transfer functions is equal to that of the filter transfer function. As for finding an "optimum" cascade sequence, sections with the flattest response are placed at the input followed by sections with less flatness and gradually moving from low Q sections to high Q ones.

SC filter cascade design approach has reached a certain level of maturity, most of it was developed in the early 80s. The method is attractive because the associated mathematics is simple and the biquadratic sections are easy to design practically hence it has been frequently chosen to design IC implementation. Many practical SC systems have been designed using cascade approach[19,20,21,22]. A large

amount of research has also been carried out on detailed development of biquadratic structures suitable for cascaded biquad designs[23-29]. Several groups have developed "SC Silicon Compilers" based on SC cascade design approach, most of which only employ one kind of biquadratic structure[30,31,32].

2.2.2 Modified Pole-Zero Pairing Scheme in Cascade SC Filter Design

Pole-zero pairing has been discussed in active-RC filter structures for optimal dynamic range and inband losses[33]. For the case of SC filter implementations, pole-zero pairing is considered in order to reduce the total capacitance of cascaded biquad SC filters[34]. Each cascade block has an associated gain factor. In order to obtain the largest voltage swing, the associated gain factor is selected so that the output voltages of each stage are of equal magnitude and as large as possible without causing overload of the filter. Furthermore, the internal opamp output nodes and the output node of each block should satisfy the same condition of equal magnitude. The value of each gain factor determines a corresponding total capacitance value. Thus there is a trade-off between each gain factor and total capacitance.

However the gain distributions in [34] are independent of how the individual biquads are ordered in the cascade structure. Therefore a circuit with maximum dynamic range could not be obtained. Moreover, because there is limited freedom of the gain distribution, this also restricts the possibility of getting the best results with minimum total capacitance. A new pole-zero pairing and gain distribution strategy is introduced. The scheme is shown below:

do pole_zero_pairing:

    do gain_distribution:

```
            circuit_realisation
            if(total_C >= Cmax) Cmax = total_C;
            if(total_C < Cmin) {
                  Cmin = total_C;
                  preseve order of pole_zero_pairing and gain_distribution
            }
      end
end
```

Using the new pole zero pairing scheme together with dynamic range scaling, a significant improvement on reduction of total capacitance is achieved. Fig.2-1 is a 6th-order filter response meeting CCITT V.22 specification for 1200 baud modems. The specification is particularly interesting due to its sloping passband. Using the arbitrary amplitude approximation method in XFILT, a 6th-order transfer function is obtained. The circuit response is shown in Fig.2-1. With a clock frequency of 128kHz, the total capacitance in E-type biquad cascade circuit realisation is 262.3 units. This result is better than the filter designed by using multirate techniques[18] and which yields a filter with total capacitance 491 units.

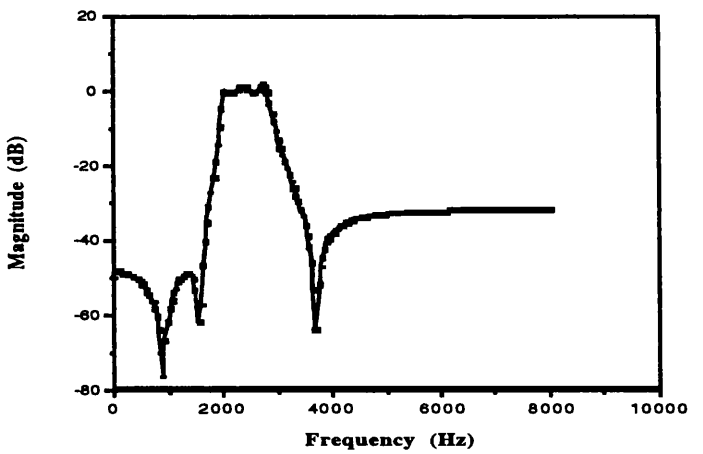


Fig.2-1 6th-order CCITT V.22 Filter Response

2.2.3 A Comparison Study of SC Biquads in the Realisation of SC Filters

In integrated filter design, the realisation of a given transfer function can be accomplished by a variety of different circuit structures. In SC technology, it is essential that the circuit be insensitive to parasitic capacitance. For this reason, the principal choices have been the cascade biquad and passive ladder simulation filters. Each circuit is characterised by different performance with respect to various design criteria. In the past, a comparison of the relative merits of different structures has been difficult due to the diverse nature of the design methods. Designers normally have to choose the circuit structure they are familiar with or for which tools are available usually limiting designs to simple ladder and biquad structures. On the other hand, a variety of design methods can provide quite different circuit structures with different total capacitance, capacitance spread, sensitivity, and non-idealities and still meet specification. Proper choice of circuit structure can often greatly reduce implementation cost and improve circuit performance. Recently matrix methods have considerably unified and regularised the design procedures for a wide range of ladder SC filter types. A comparison study for different ladder based designs is given in [15]. It is well-known that ladder filters have low sensitivity to component deviations compared to biquads, however they also appear to be unsuitable for realisation of certain transfer function categories where biquad structures have great superiority in both sensitivity and capacitance spread. Most of the biquads proposed have been analysed individually and the investigations have been based on the characteristics of the biquad itself. However when a filter designer is faced with the question of implementing a SC filter with particular specification, it is very difficult for him to decide which biquad should be used, just based on the individual biquad performance, because the high order filter transfer

function is usually factorised into several biquadratic functions. Also the various filters proposed are intended for different applications, frequency ranges, sensitivity requirements, dynamic range etc., therefore it is difficult to judge the suitability of the biquads. With the aid of the XFILT filter compiler, a systematic comparison for the realisation of SC filters using the most popular SC biquads is now given. Although the software has the facility to design a SC system with combined biquads, we restrict our comparison here to systems only composed of one kind of SC biquad, in order to simplify the question and make the guidelines of selecting SC biquads more practical for the SC filter designer who does not have an SC filter compiler or has a compiler but with only limited biquad structures. Comparison for SC filter realisation on total capacitance, capacitance spread, sensitivity, non-idealities and dynamic range is given. Some conclusions are obtained as very useful guidelines for the choice of a suitable biquad structure according to the nature of the filter problem.

2.2.3.1 Biquad Configurations

The biquads that we adopt here are:

Type-E: Traditional Fleischer and Laker's E-type biquad in [23].

Type-F: Traditional Fleischer and Laker's F-type biquad in [23].

FGL Type: Modified Fleischer and Laker's biquad given in [24].

G-T type: Gregorian and Temes's biquad presented in [25].

M-S type: Martin and Sedra's biquad in [26].

SSGI type: Sanchez-Sinencio, Silva-Martinez and Geiger's type-I biquad in [27].

SSGII type: Sanchez-Sinencio, Silva-Martinez and Geiger's type-II biquad in [27].

Nagaraj type: Nagaraj's biquad proposed in [28].

All these biquad structures are insensitive to stray capacitances. The number of capacitors and switches used in the above biquads is given in Table 2-1.

	No. Capacitors	No. Switches
Type-E	9	12
Type-F	9	12
FGL	11	12
SSGI	10	14
SSGII	9	14
G-T	8	10
M-S	8	10
Nagaraj	11	15

Table 2-1. Number of capacitors and switches used in biquads

Type-E and Type-F biquads are well known biquads. The Type-E biquad is a capacitive damping structure formed by connecting a non-switched capacitor around the entire loop and the Type-F biquad is a resistive damping structure by connecting a switched capacitor around one of the two integrators. Usually the capacitive damping structure leads to some reduction in the capacitance spread. The FGL type biquad is a modified version of Type-E and Type-F structure, has addition of unswitched capacitors connected to the negative input terminal of opamp, and improvement in sensitivity is made. The G-T type biquad is a set of biquads which change topology according to the Q factor and zero position of the transfer function to achieve positive coefficient values and minimum overall capacitance. An unswitched-capacitor is also used to improve the sensitivity performance. The M-S

type biquad differs from G-T type biquads only in several switch phase arrangements. SSGI and SSGII are resistively damped biquads and a trade-off between total capacitance and sensitivity can be made. Nagaraj's biquad is especially attractive for large time-constant application realisation. In this case, the total capacitance and capacitance spread can be reduced significantly.

2.2.3.2 Filter Realisation Comparison

Five different kinds of SC filters (lowpass, wide bandpass, narrow bandpass, highpass and bandstop) are realised by the above SC biquads. All the comparisons are based on these filters. Many designs have been carried out and similar conclusions are obtained.

a). Lowpass Filter

The lowpass filter, which is used in a dual-channel speech processing chip, is of the following specification:

Clock frequency = 106.7kHz

Upper passband edge = 3.4kHz

Lower stopband edge = 8kHz

Passband ripple < 0.5dB

Stopband attenuation > 60dB

Passband gain = 6dB

A 6th order elliptic filter is employed and the circuit response is shown in Fig.2-2(a). Table 2-2 shows the realisation statistics of different biquad cascades.

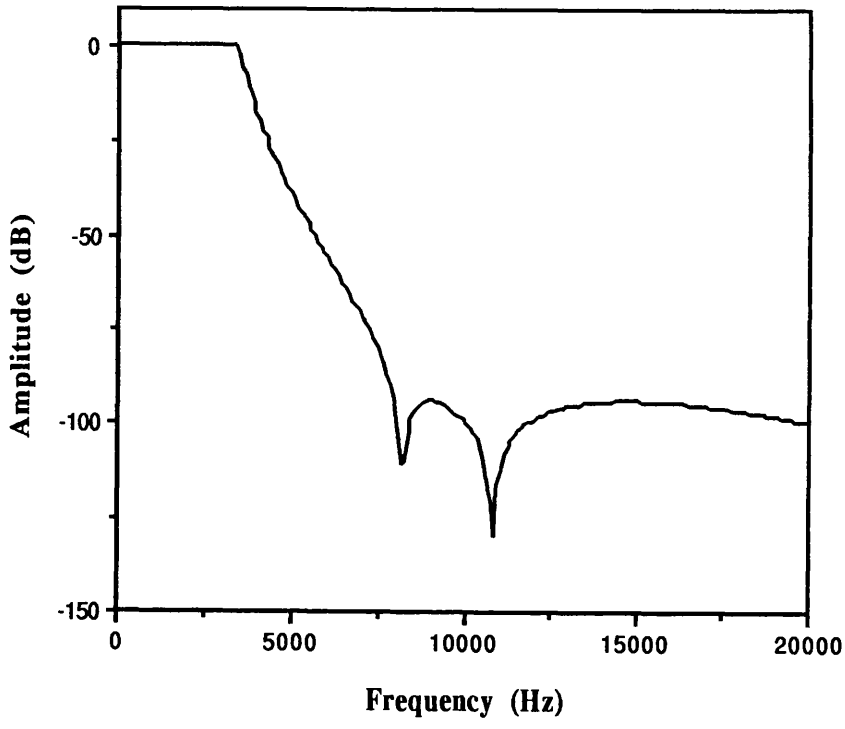


Fig. 2-2(a) Lowpass Filter Response

	No. AMP	No. C	No. SW	Total C	C Spread
Type E	6	22	27	144	46
Type F	6	22	27	130	45
LGF	6	21	36	181	44
SSGI	6	27	42	171	22
SSGII	6	27	42	171	22
G-T	6	21	30	145	44
M-S	6	21	30	151	44
Nagaraj	6	27	45	199	44

Table 2-2. 6th-order lowpass filter realisation

In the lowpass case, the type-F biquad realisation gives minimum total capacitance and SSGI and SSGII biquad realisations give very small capacitance spread.

b).Wide bandpass filter

This wide bandpass filter is a 6th-order filter with CCITTV.22 specification for 1200 baud modems. The specification is of sloping passband that is given in Table 2-3. The SC circuit sampling frequency is 128kHz. The circuit frequency response is given in Fig.2-2(b).

Freq(Hz)	800	1200	1600	2000	2400	2800	3200	3500
Gain Max	-50	-50	-50	0.0	0.75	1.5	-10	-20
Gain min				-1.5	-0.75	0.0		

Table 2-3. Specification for bandpass filter

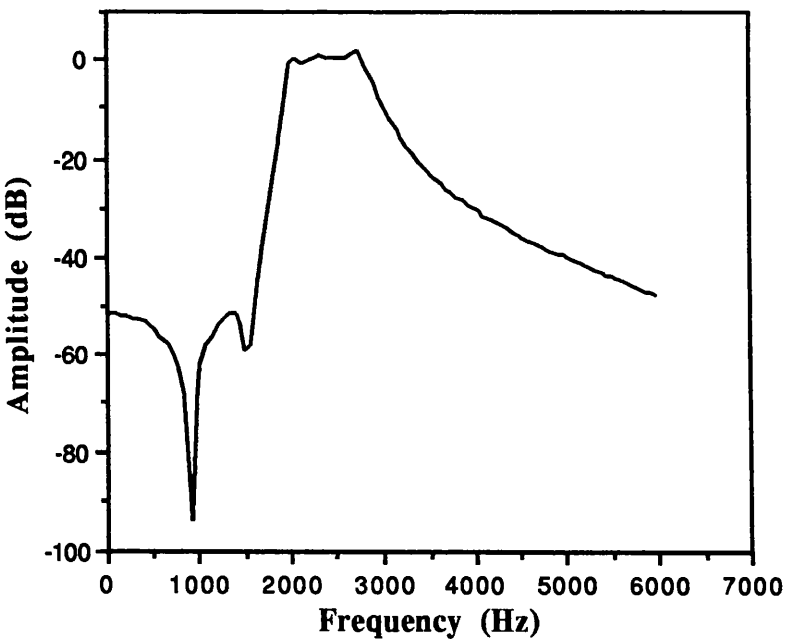


Fig.2-2(b) Wide Bandpass Filter Response

The design results are given in Table 4.

	No. AMP	No. C	No. SW	Total C	C Spread
Type E	6	22	27	316	78
Type F	6	22	27	706	191
LGF Type	6	21	36	329	95
SSGI	6	27	42	351	95
SSGII	6	27	42	351	95
G-T	6	21	30	329	95
M-S	6	21	30	329	95
Nagaraj	6	27	45	213	47

Table 2-4. Bandpass filter design results

It is seen from Table 2-4 that the filter realised by Nagaraj biquad gives very good results both in total capacitance and capacitance spread. The cost is that Nagaraj biquad needs more switches. For the total area, the Nagaraj biquad realisation is still the best one. It is also interesting to notice that just because the choice of different damping capacitor in the type-E and type-F biquads, the total capacitance and capacitance spread can be quite different. This situation is also observed in the highpass and bandstop examples.

c).Narrow bandpass filter

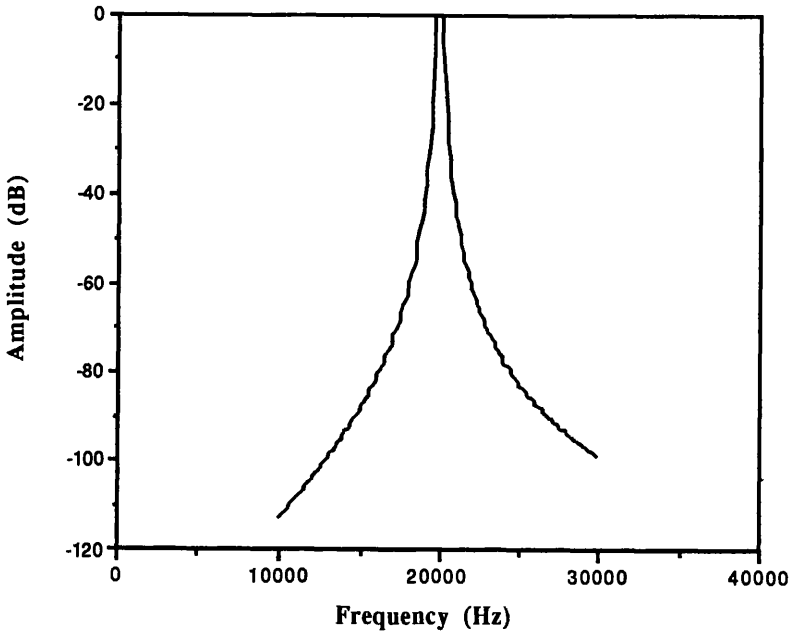


Fig.2-2(c) Narrow Bandpass Filter Response

	No. op	No. C	No. SW	Total C	C Spread
Type E	6	20	24	1150	334
Type F	6	20	24	1113	332
LGF Type	6	20	36	1126	337
SSGI	6	25	42	1235	169
SSGII	6	25	42	1152	169
G-T	6	20	30	1126	337
M-S	6	20	30	1126	337
Nagaraj	6	27	45	5796	1051

Table 2-5. Narrow band bandpass filter design results

A 6th order bandpass chebyshev filter centred on 20kHz with -0.01dB ripple, 480Hz bandwidth, and 30dB stopband attenuation is chosen. The frequency response is given in Fig.2-2(c) and Table 2-5 shows different cascades realisation statistics.

In this filter realisation, SSGII gives better results. Both SSGI and SSGII have small capacitance spread. Although this spread is still too large for most SC implementation, it shows that SSGI and SSGII are good candidates for narrow band filter realisations. In practice, the realisation of very narrow band filters needs special methods, such as multirate techniques. Table 2-5 also shows that Nagaraj biquad structure is definitely not suitable for narrow band filter realisation.

d). Highpass Filter

Here we show a 5th-order inverse-Chebyshev high-pass filter that gives 40dB attenuation at low stopband. The filter is used in a radiotelephone system. The filter frequency response is given in Fig.2-2(d) and Table 2-6 gives the design results.

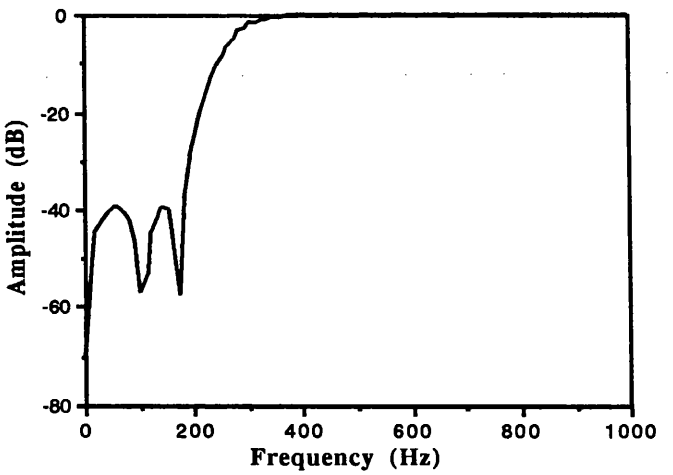


Fig.2-2(d) Highpass Filter Response

	No. AMP	No. C	No. SW	Total C	C Spread
Type E	5	18	23	539	156
Type F	5	18	23	319	63
LGF Type	5	18	30	485	138
SSGI	5	23	36	366	67
SSGII	5	23	36	366	67
G-T	5	17	26	522	124
M-S	5	17	26	458	136
Nagaraj	5	21	36	158	28

Table 2-6. Fourth-order Inverse-Chebyshev highpass filter realisation

In Table 2-6, it is also shown that Nagaraj biquad gives good results both in total capacitance and capacitance spread. The Nagaraj biquad realisation gives a reduction in total capacitance and capacitance spread by more than 50%. Notice also the wide variation in Type-E and Type-F designs. In highpass filter realisation, SSGI, SSGII and Type-F can be selected if Nagaraj biquads are not suitable or non-ideality effects need to be considered.

e).Bandstop Filter

The specification for a bandstop filter is given as:

Clock frequency = 300kHz

Lower passband edge = 3kHz

Upper passband edge = 5kHz

Lower stopband edge = 3.3kHz

Upper stopband edge = 4.5kHz

Passband ripple < 2dB

Stopband attenuation > 40dB

The circuit response is shown in Fig.3-2(e) and the design results are given in Table 2-7.

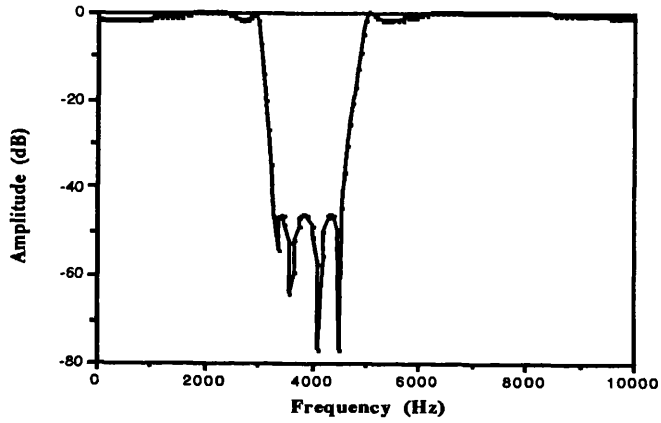


Fig.3-2(e) Bandstop Filter Response

	No. AMP	No. C	No. SW	Total C	C Spread
Type E	8	29	35	221	29
Type F	8	29	35	1310	361
LGF Type	8	28	48	220	33
SSGI	8	36	56	259	25
SSGII	8	36	56	259	25
G-T	8	28	40	555	107
M-S	8	28	40	213	23
Nagaraj	8	36	60	143	23

Table 2-7. 8th-order Elliptic bandstop filter realisation

This example also demonstrates that the Nagaraj biquad has smallest total capacitance and capacitance spread. Second choice for total capacitance and capacitance spread is the M-S biquad realisation. Type-F gives unacceptably larger total capacitance and capacitance spread.

Although it has not yet been studied thoroughly, it appears that cascade biquads are superior in all respects for bandstop type of filtering compared to ladder realisation, having excellent sensitivity (even better than ladders) and very low total capacitance and capacitance spread. The biquad seems to be ideally suited to notch transfer functions.

2.2.3.3 Sensitivity Comparison

The following index is used as a global measure of system sensitivity $S(\omega)$[35]

$$S(\omega) = 8.686\left\{\sum_i \left[\frac{c_i}{|H(\omega)|}\frac{\partial|H(\omega)|}{\partial c_i}\right]^2\right\}^{1/2} / 100.0 \qquad (2\text{-}3)$$

where C_i and $H(\omega)$ are the sets of capacitances and filter transfer function. $S(\omega)$ in Eq.(2-3) is a multiparameter sensitivity which accounts for the effect of every capacitance change. $S(\omega)$ is required to be as small as possible.

Because of the similarity of some biquads, the total sensitivity index curves sometimes are so close to each other it is difficult to distinguish them. Fig.2-3(a)-(e) give the comparison of sensitivities of the five different filter designs. These show that in these examples G-T type realisation always gives best sensitivity

performance. M-S type design has sensitivity performance as good as G-T except in the highpass realisation. The sensitivity performance of Type-E, Type-F and LGF are close to M-S and G-Ts with LGF structure showing slight improvement due to the introduction of two continuous capacitor feedthrough capacitors. SSGI and SSGII structures give fairly high sensitivity compared to other realisations,. however, in a narrow bandpass filter realisation, the circuit sensitivity is not bad. Nagaraj's structure gives somewhat higher sensitivity.

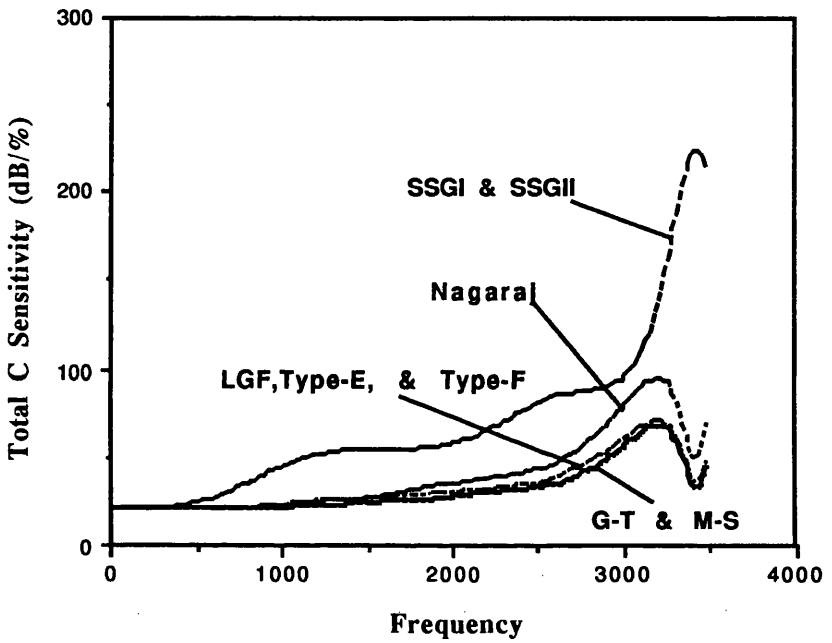


Fig.2-3(a) Comparison of Lowpass Filter Sensitivities

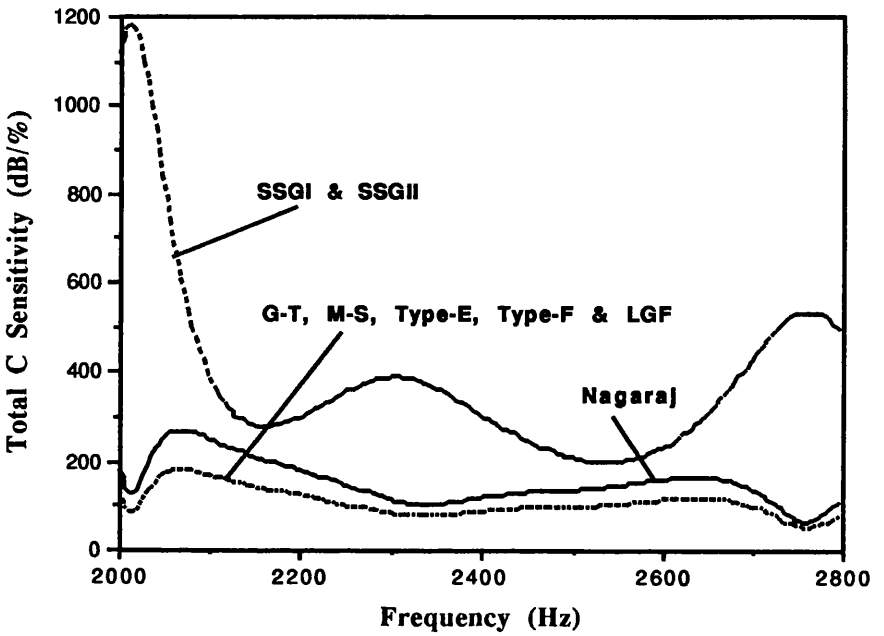


Fig.2-3(b)Comparison of Wide Bandpass Filter Sensitivities

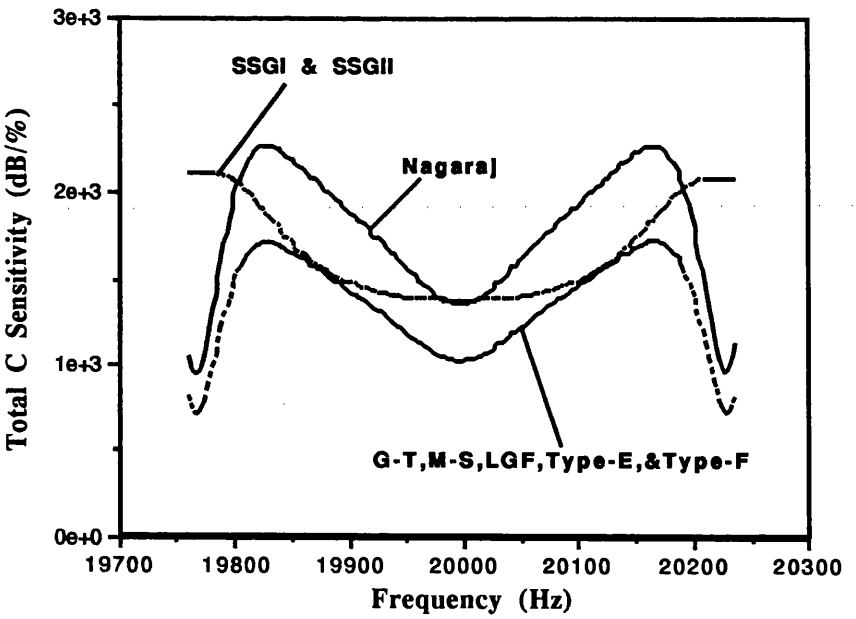


Fig.2-3(c) Comparison of Narrow Bandpass Filter Sensitivities

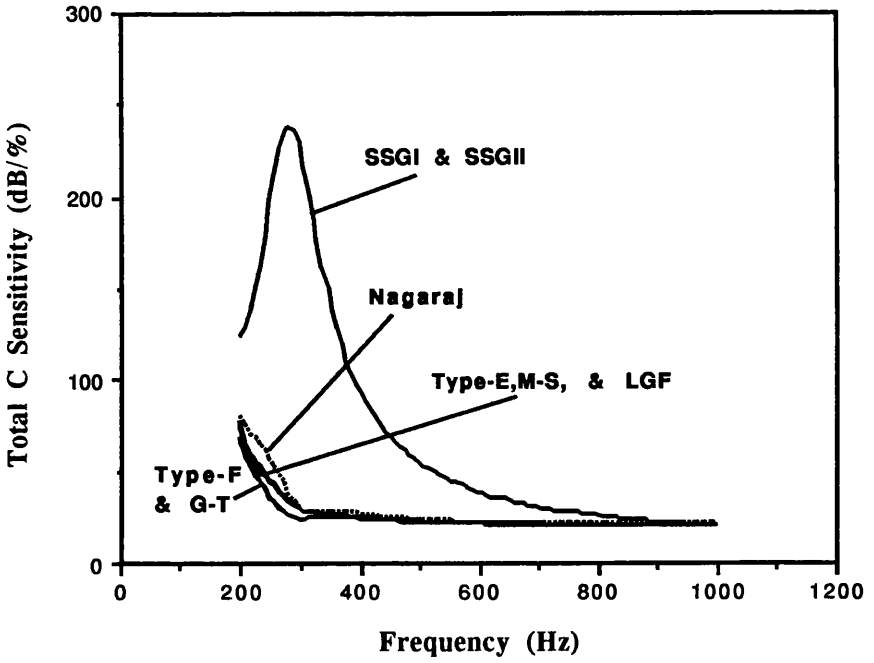


Fig.2-3(d) Comparison of Highpass Filter Sensitivities

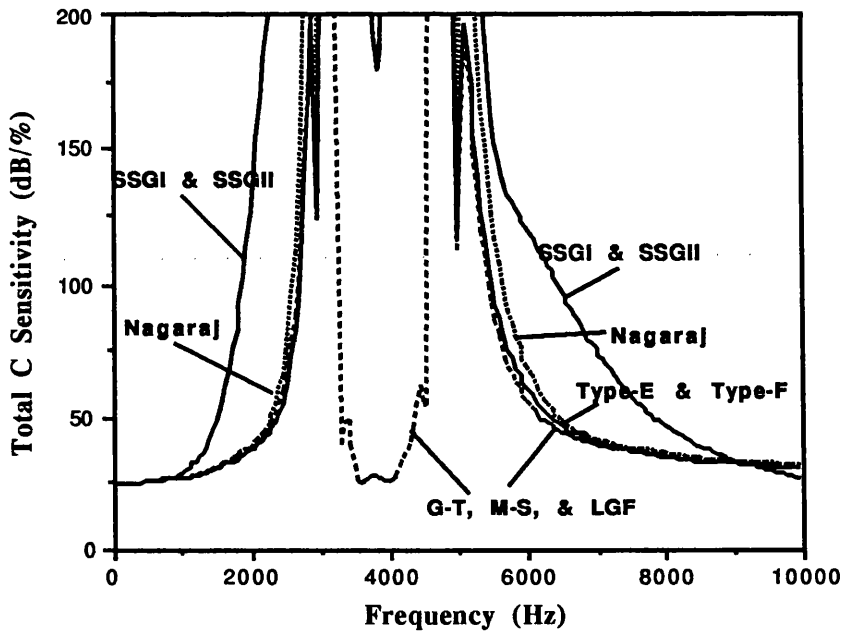


Fig.2-3(e) Comparison of Bandstop Filter Sensitivities

2.2.3.4. Dynamic Range Comparison

The following index is used as a global measure of dynamic range[15]

$$D(\omega) = \frac{1}{M}\sum_{i} 20\log|H_i(\omega)| \qquad (2\text{-}4)$$

where M is the number of opamps and $H_i(\omega)$ is the transfer function from input to i-th opamp's output. $D(\omega)$ is not a direct dynamic range measure of a SC filter, but is a measure of all opamp's output voltage range. It is related to SC filter dynamic range or signal handling capability. It is hoped that the dynamic index curve $D(\omega)$ is as flat as possible and as close to zero or a fixed filter gain as possible in passband in order to obtain a maximum dynamic range and maximum signal handling capability.

Comparisons of the dynamic index curves are given in Fig.2-4(a)-(e). In the filter design process, the equal peak gain scaling is carried out. The comparison shows that SSGI and SSGII have best performance in the example lowpass, wide bandpass, and bandstop filters, and also keep good performance in highpass and narrow-bandpass filter systems. Type-E and Type-F are good in the example narrow bandpass, lowpass, and wide bandpass, but poor in highpass and bandstop cases. LGF biquad realisation shows slight improvement over Type-E and Type-F realisations. Nagaraj's structure exhibits a modest performance on dynamic range. In most cases, G-T and M-S dynamic range performance is slightly poorer than Nagaraj except in highpass case where M-S shows the best performance.

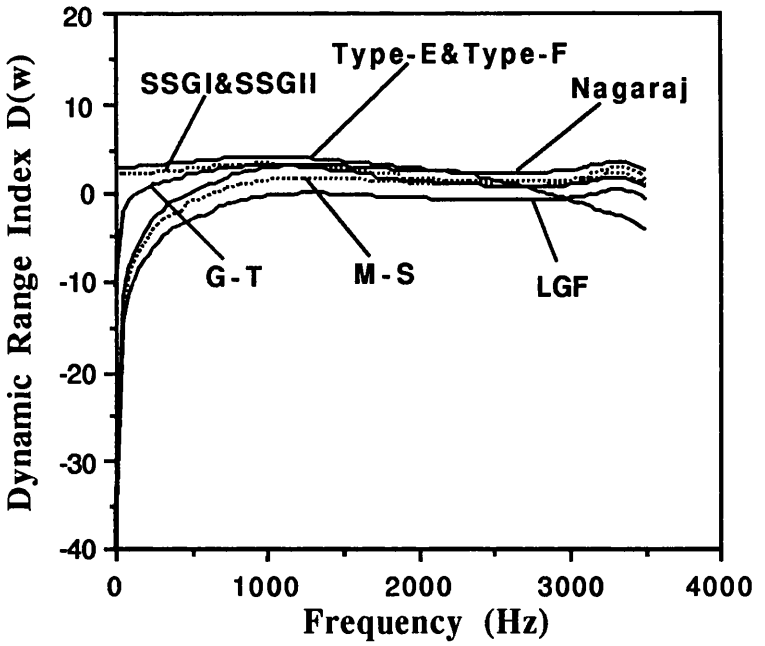


Fig.2-4(a) Dynamic Range Index of Lowpass Filter

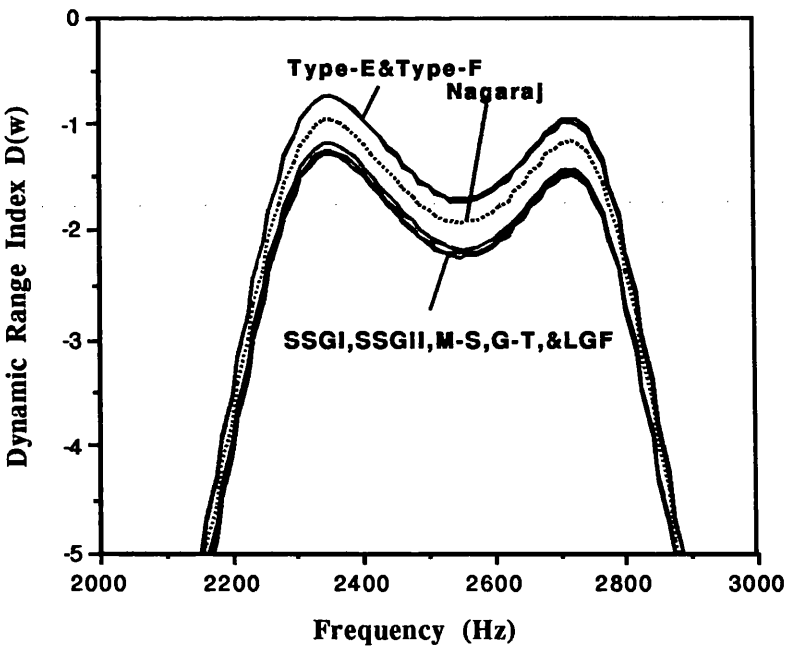


Fig.2-4(b) Dynamic Range Index of Wide Bandpass Filter

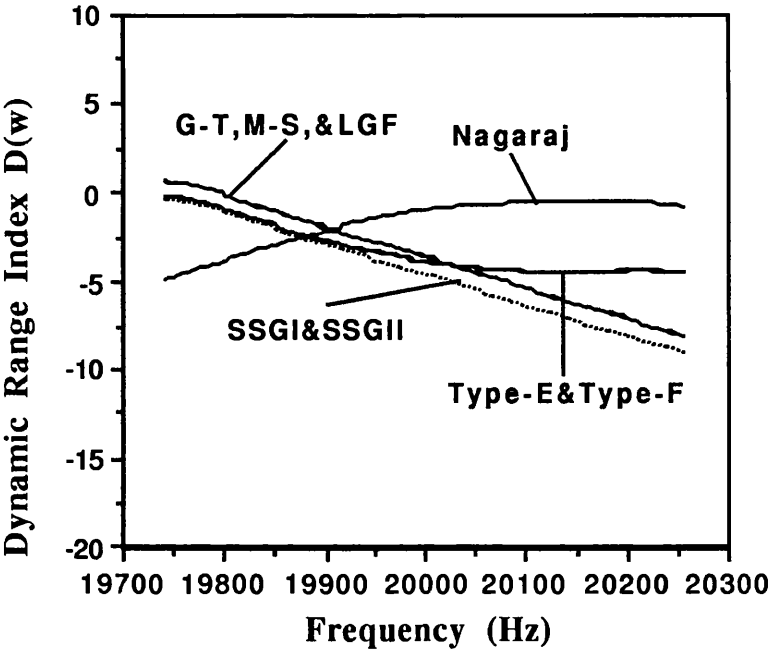


Fig.2-4(c) Dynamic Range Index of Narrow Bandpass Filter

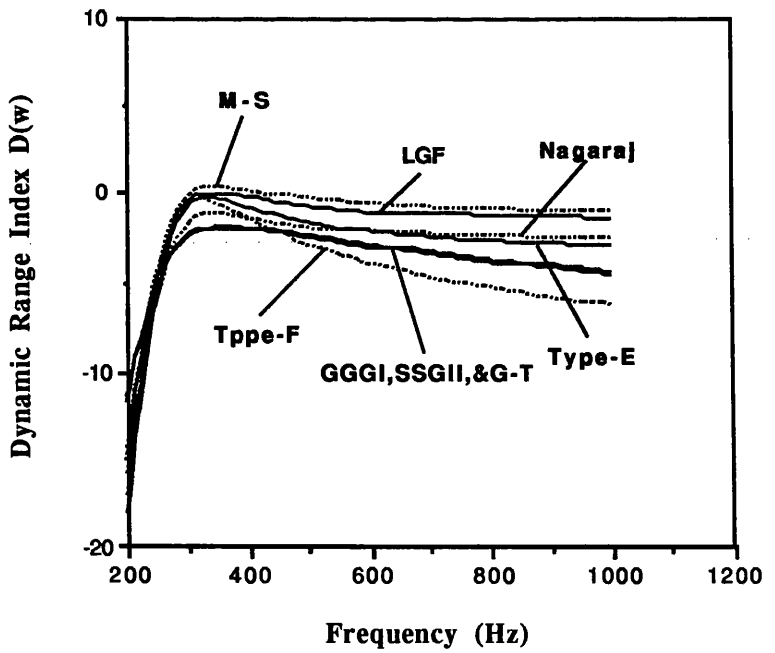


Fig.2-4(d) Dynamic Range Index of Highpass Filter

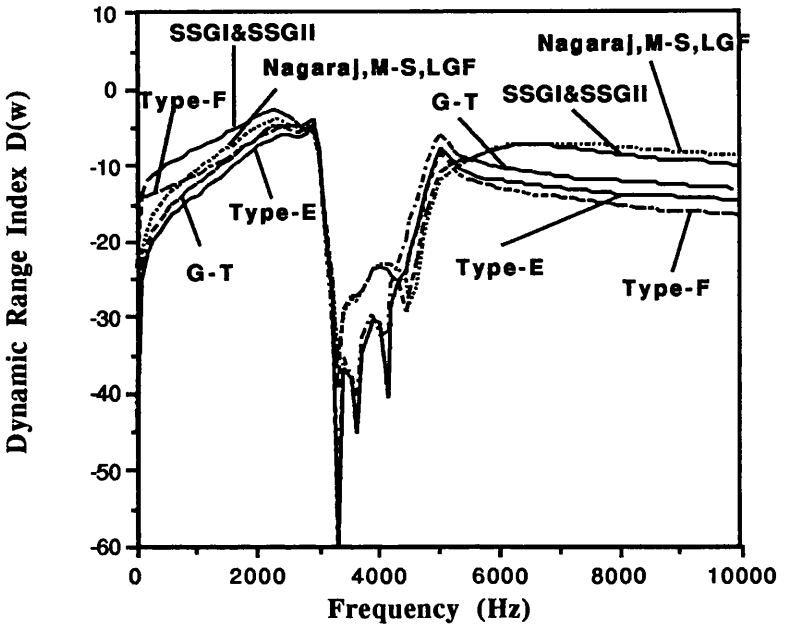


Fig.2-4(e) Dynamic Range Index of Bandstop Filter

2.2.3.5. Finite GB and Switch Resistance Effect Comparison

One of the fundamental aspects determining the selection of preferred circuit topologies for the proposed SC filter, is the performance behaviour under non-ideal characteristics of the components namely, finite DC-gain and bandwidth of the opamps, finite on and off resistance of the switches. The non-ideality effect of opamp can be approximately evaluated from circuit topologies if certain conditions are satisfied[27]. However, because each circuit has a different topology the non-ideality effect of finite on and off resistance of switches cannot be simply calculated. The only way of predicting all these non-idealities of an SC circuit is to simulate it by SC analysis software capable of including non-ideal effects. For comparison proposes, we choose the opamp with 2MHz gain-bandwidth product and the switches with 1kΩ on resistance and 1MΩ. off resistance. A full non-ideal analysis is carried out and Figs.2-5(a)-(e) show the non-ideal circuit response of the

designed circuits. Generally speaking, Nagaraj structure is very sensitive to non-ideal effects. SSGI and SSGII have better performance in lowpass, and highpass cases, but worse in wide bandpass, narrow bandpass, and bandstop cases. M-S has good performance for all filter realisation. G-T is good in lowpass, bandpass, and bandstop cases, but shows a large variation in the highpass filter realisation. Type-E is good in bandpass, and bandstop, but slightly worse in lowpass, and highpass cases. Type-F is poor in narrow bandpass and highpass realisations.

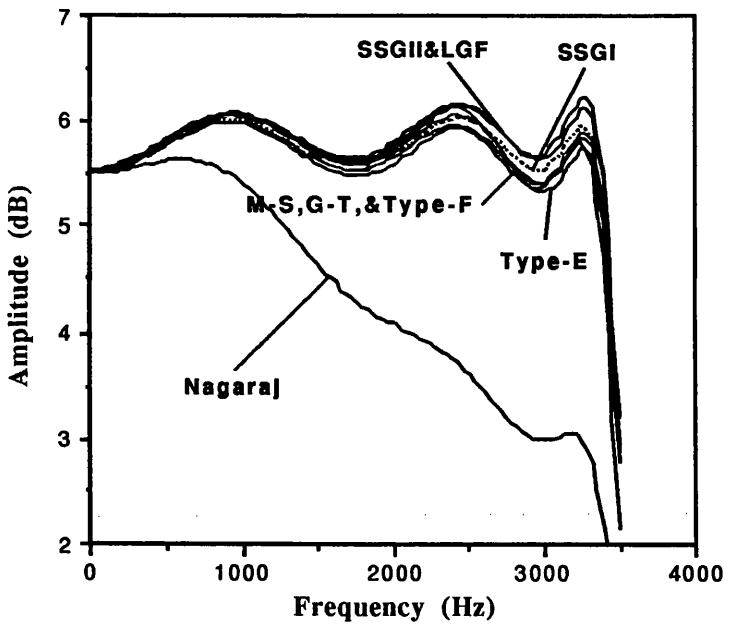


Fig.2-5(a) Non-ideal Response of Lowpass Filter

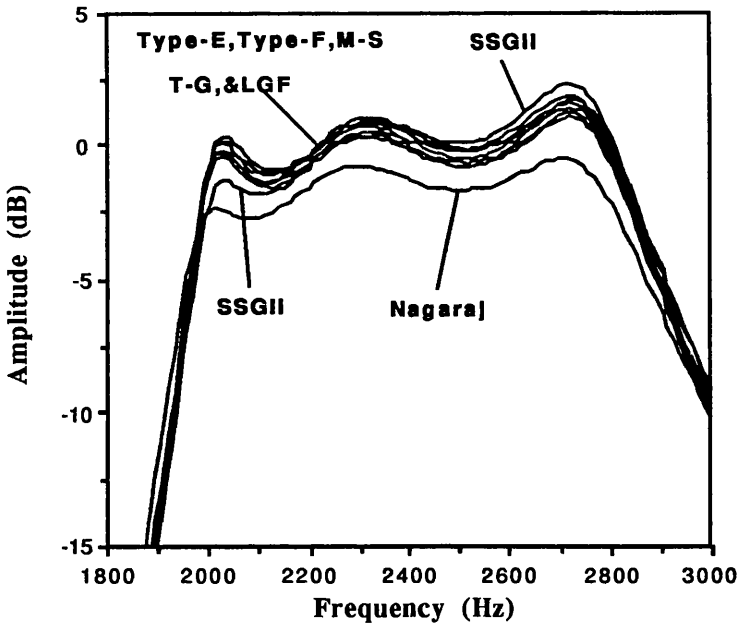


Fig.2-5(b)Non-ideal Response of Wide Bandpass Filter

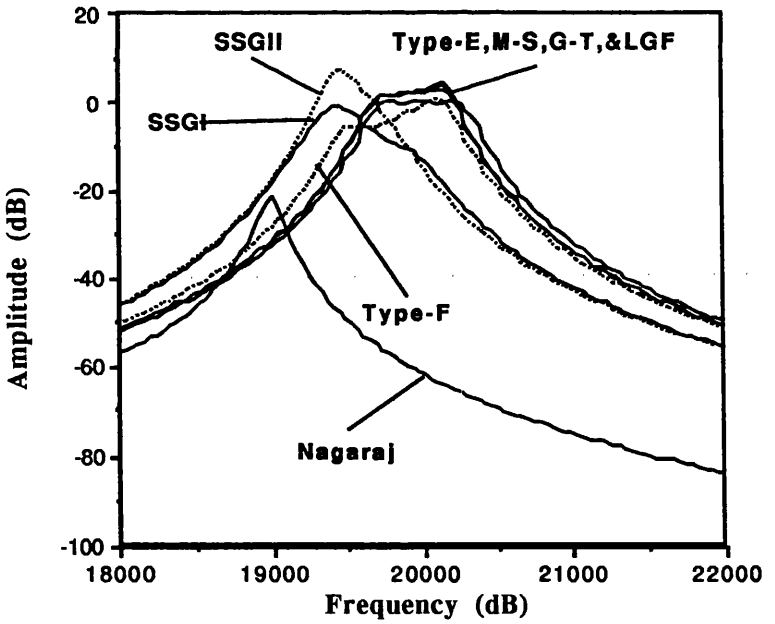


Fig.2-5(c) Non-ideal Response of Narrow Bandpass Filter

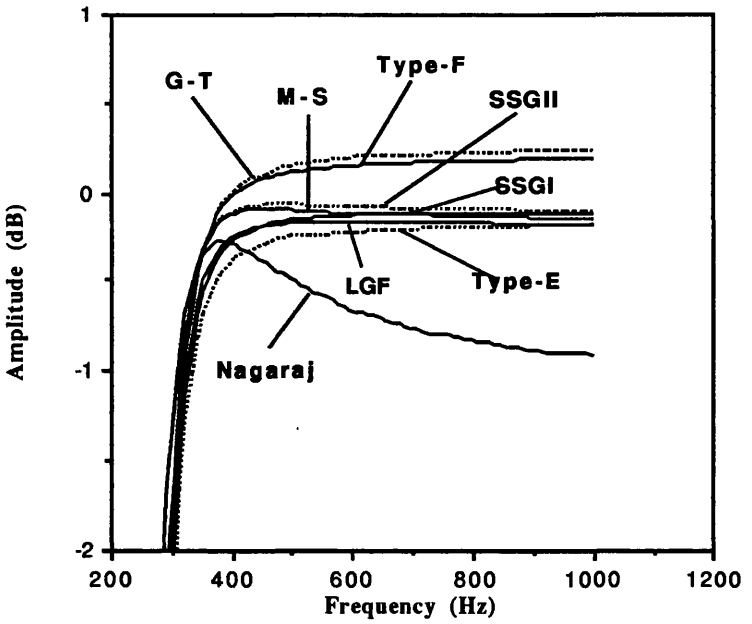


Fig.2-5(d) Non-ideal Response of Highpass Filter

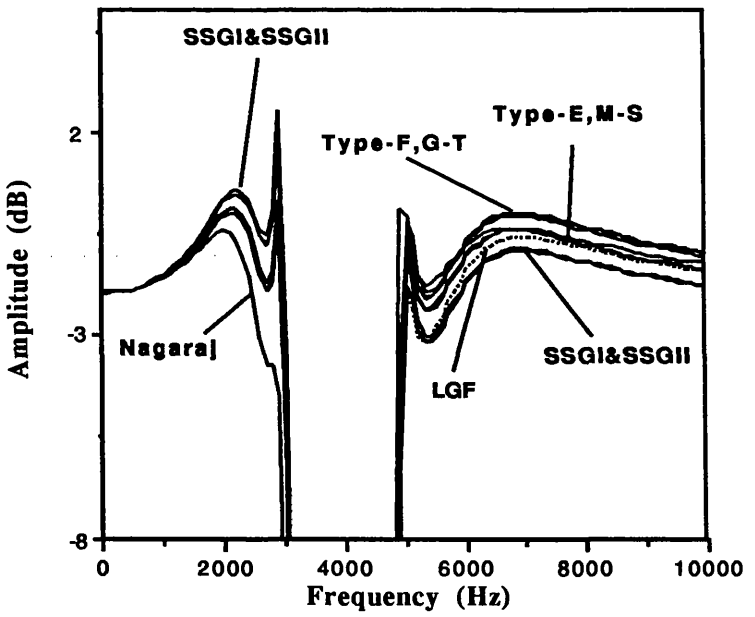


Fig.2-5(e) Non-ideal Response of Bandstop Filter

2.2.3.6 Noise Comparison

Noise simulation results for the example filters are shown in Figs.2-6(a)-(e). It is assumed that the equivalent white noise of opamp is $50nV/\sqrt{Hz}$, and the corner frequency of the 1/f noise (flicker noise) is 1kHz, and 20 higher band contributions are considered. Fig.2-6(a) gives noise comparison of 6th-order Elliptic lowpass filters, it is apparent that a filter designed by G-T type biquads yields best noise performance. The filters designed by Type-F, Type-E, M-S, and LGF biquads also give good noise performance. Nagaraj biquad based realisation gives a higher noise response, and the SSGI and SSGII based realisations are similar. The noise comparison of the 6th-order IIR wide bandpass filters is presented in Fig.2-6(b). In wide bandpass case, filter designed by Type-F biquads has best noise performance. Type-E, M-S, G-T and LGF based filters also give good noise performance. SSGI and SSGII based filters have relatively high noise responses with the Nagaraj biquad based filter following close behind. The noise comparison for narrow bandpass filters is shown in Fig.2-6(c). The Type-E, Type-F, M-S, G-T and LGF biquads based cascade structure have lower noise responses while Nagaraj, SSGI and SSGII biquads based cascade structures have higher noise responses. The highpass filter noise comparison is given in Fig.2-6(d). The noise performance from best to worse follows the sequence Type-F, G-T, M-S, LGF, Type-E, SSGI, SSGII and Nagaraj, with the worst group being the Nagaraj, SSGI and SSGII based cascade structures. Fig.2-6(e) shows noise comparison of 8th-order Elliptic bandstop filters. G-T, M-S, LGF, Type-E, and Type-F based structures give best noise performances, while SSGI, SSGII and Nagaraj based realisations present poorer performance. From all five filter design examples, it can be shown that Nagaraj, SSGI and SSGII based structure have a relatively poorer noise performance compared to the other biquad realisations. It is also seen that when lowpass and bandpass filters are designed, the 1/f noise effect must be considered.

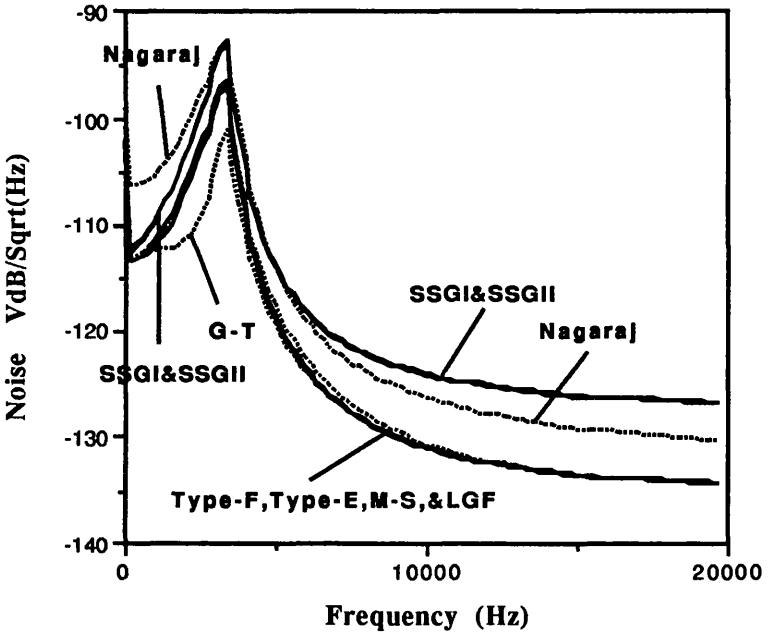


Fig.2-6(a) Noise comparison of 6th-order Elliptic lowpass filter

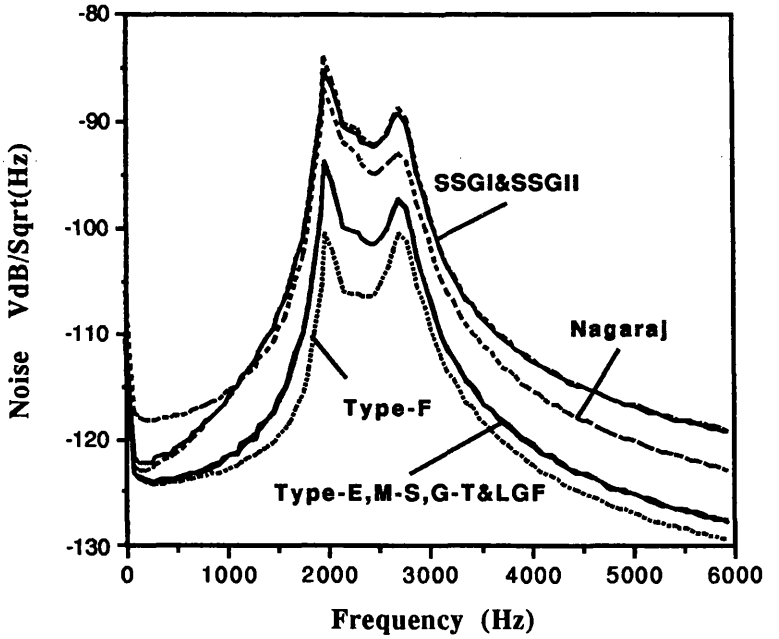


Fig.2-6(b) Noise comparison of 6th-order IIR wide bandpass filters

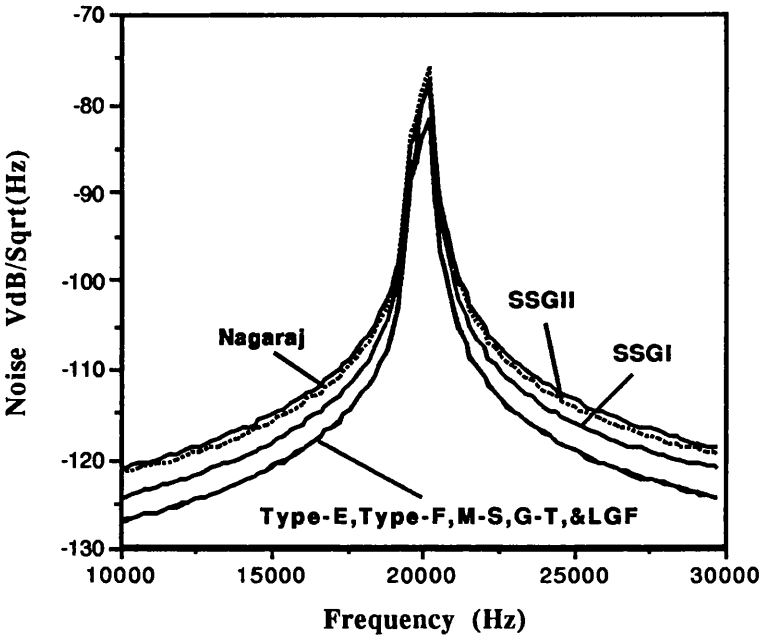


Fig.2-6(c) Noise comparison of 6th-order Chebyshev narrow bandpass filters

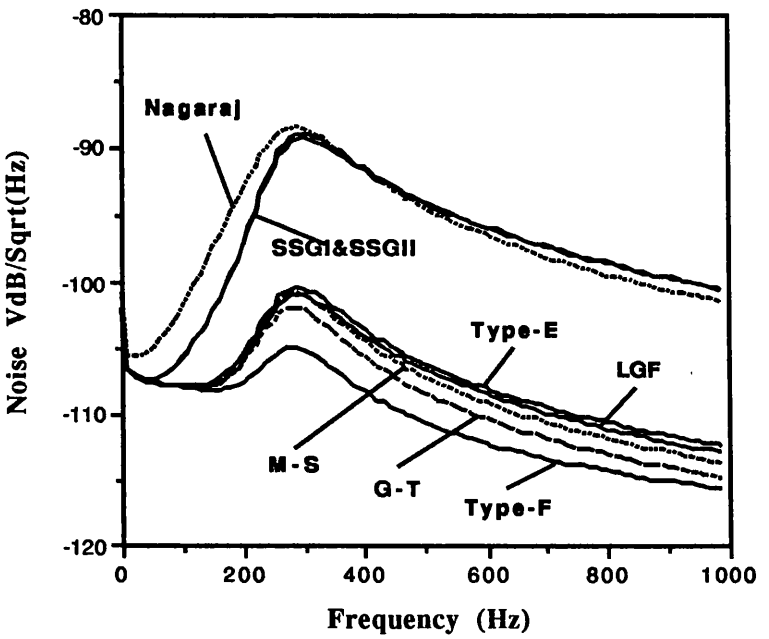


Fig.2-6(d) Noise comparison of 5th-order inverse-Chebyshev highpass filters

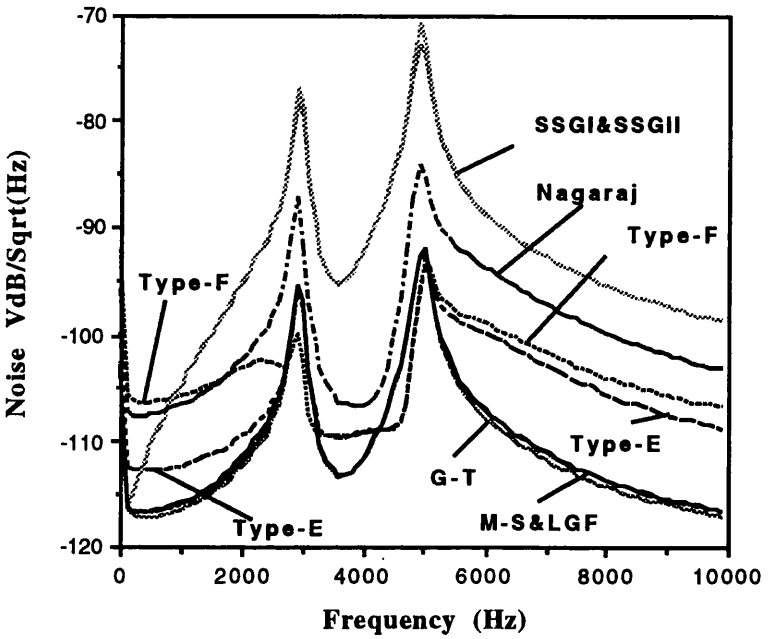


Fig.2-6(e) Noise comparison of 8th-order Elliptic bandstop filters

2.2.3.7 Summary of Comparison

After a comprehensive survey of a variety of filter realisations using a selection of biquad cascades, it can be concluded:

Nagaraj's biquad has significant advantages for wide bandpass, bandstop, and highpass filter designs regarding total capacitance and capacitance spread. It also has very good dynamic range performance, but it is comparatively sensitive to non-ideal effects, shows a slightly higher sensitivity and relatively higher noise response when compared to other biquad realisations. Therefore a compensated structure[29] is critical in cascading Nagaraj biquad realisations, in order to obtain a stable and less sensitive circuit realisation.

SSGI and SSGII biquads have very good dynamic range performance and they are best candidates for narrow band filters regarding total capacitance and capacitance

spread. They also gives best capacitance spread in lowpass filter realisation. However, SSGI and SSGII structures usually show slightly higher sensitivity to component change and poorer noise performance.

The G-T biquad has lowest sensitivity and smallest response to non-ideal effects. Generally, type-E, LGF, M-S, and G-T structures have similar total capacitance and capacitance spread, except in a bandstop filter where the G-T biquad shows a large total capacitance and capacitance spread. They also have lower sensitivity, good dynamic range, small non-ideal effects, and low noise performance.

Type-F biquad has a good total capacitance and capacitance spread for the highpass case, but poor in wide bandpass, and bandstop cases. It has fairly good sensitivity performance and dynamic range, a small non-ideal effect and low noise response.

2.3 LADDER BASED SWITCHED-CAPACITOR FILTER DESIGN

Cascade design approach presented in previous section is a simplest and popular method for active filter realisation. However for high order monolithic filters, the cascading of biquadratic sections leads to an unacceptably high sensitivity of the response to component parameter variations. It is well known that appropriately designed LC ladders have very low sensitivities to component tolerance and hence active filters simulating the internal workings of doubly terminated RLC ladder prototypes are widely used in high precision integrated filters. Passive ladder prototypes for standard lowpass approximations are readily available from filter tables and component values of all other types of frequency response (bandpass, bandstop and highpass) can be obtained by applying standard frequency transformation and scaling methods. Alternatively, computer programs can be used to generate a passive ladder automatically for more general approximations. Various techniques have been introduced which allow the expert user to control or modify the prototype ladder development to assist in the reduction in component spread and sensitivity of the subsequent active realisations. The prototype ladders can often become unrealisable in

passive terms, but active implementations are quite feasible and often demonstrate improved performance results.

A powerful matrix based approach[15] has been developed and applied to the design of SC, active-RC, and digital ladder based filters and equalisers. In the case of SC filters this has led to configurations which are far from intuitively obvious but which offer improved performance with respect to parameters such as settling time and capacitance spread. Moreover, this method is well suited for CAD software development. After a brief review of the matrix based SC filter design approach, a modified and extended canonical realisation is presented, which shows much more accuracy than the previous one in SC case[36]. As an example, a 8th-order Elliptic bandpass filter is designed. The sensitivity comparison with a cascade realisation is given.

2.3.1 Review of Matrix Method for SC Ladder Based Filter Design

A passive ladder can be represented by the standard nodal admittance matrix equation

$$\mathbf{J} = (\mathbf{G}+s\mathbf{C}+s^{-1}\Gamma)\mathbf{V} \qquad (2\text{-}5)$$

where **V** is the vector representing the nodal voltages and **J** is a vector representing the input current sources. **G**,**C**, and Γ are admittance matrices formed by the contributions of resistors, capacitors and inductors respectively. Equation (2-5) represents a set of equations of second order in the Laplacian variable s. It is well known that a set of linear first order algebraic equations can represent a signal flow graph and be realised by active building blocks. The matrix method enables direct decomposition of the second order matrix to give two inter-related first order equations, and these first order systems are then directly implemented using the active building blocks.

The design of a switched-capacitor simulation starts from the prototype system equation (2-5), which after bilinear transformation becomes

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}\mathbf{C} + \frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma + \mathbf{G}\right]\mathbf{V} = \mathbf{J} \tag{2-6}$$

Rearranging gives

$$\left[\frac{1}{\psi}\mathbf{A} + \phi\mathbf{B} + \mathbf{D}\right]\mathbf{V} = \mathbf{J}(1+z) \tag{2-7}$$

or alternatively

$$\left[\frac{1}{\phi}\mathbf{A} + \psi\mathbf{B} + \mathbf{D}\right]\mathbf{V} = \mathbf{J}(1+z^{-1}) \tag{2-8}$$

where

$$\mathbf{A} = 2\mathbf{C}/T + T\Gamma/2 + \mathbf{G} \text{ for (2-7)} \tag{2-9a}$$

$$\mathbf{A} = 2\mathbf{C}/T + T\Gamma/2 - \mathbf{G} \text{ for (2-8)} \tag{2-9b}$$

$$\mathbf{B} = 2T\Gamma \tag{2-9c}$$

$$\mathbf{D} = 2\,\mathbf{G} \tag{2-9d}$$

$$\Phi = 1/(1-z^{-1}) \tag{2-9e}$$

$$\Psi = z^{-1}/(1-z^{-1}) \tag{2-9f}$$

The bilinear transformation has the advantage of both stability and exactness. Unfortunately, bilinear integrators are sensitive to the stray capacitance and are not practically useful. Instead a modified SC ladder based structure utilising LDI integrators can be formed.

Factorise the matrix **A** into $\mathbf{A}_l\mathbf{A}_r$ and the *SC Left Decomposition* is obtained as

$$(\Phi B+\mathbf{D})\mathbf{V} + \mathbf{A}_l\mathbf{W} = 2\mathbf{J} \quad (2\text{-}10a)$$

$$\mathbf{A}_r\mathbf{V} + \Psi\mathbf{W} = \mathbf{A}_r^{-1}\mathbf{J} \quad (2\text{-}10b)$$

Factorise the matrix **B** into $\mathbf{B}_l\mathbf{B}_r$ and the *SC Right Decomposition* is obtained as

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \mathbf{B}_l\mathbf{W} = -\mathbf{J} \quad (2\text{-}11a)$$

$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = -2\mathbf{B}_r^{-1}\mathbf{J} \quad (2\text{-}11b)$$

Standard numerical techniques for matrix decomposition of **A** or **B** yield a range of circuit implementations whose suitability in various applications has been examined.

SC Left Inverse Decomposition

$$(\Phi B + \mathbf{D})\mathbf{V} + \mathbf{W} = (1+z)\mathbf{J} \quad (2\text{-}12a)$$

$$\mathbf{V} + \Psi\mathbf{A}^{-1}\mathbf{W} = \mathbf{0} \quad (2\text{-}12b)$$

SC Right Inverse Decomposition

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{W} = \mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (2\text{-}13a)$$

$$-\Psi\mathbf{V} + \mathbf{B}^{-1}\mathbf{W} = \mathbf{0} \quad (2\text{-}13b)$$

Generally the SC Left Decompositions demonstrate excellent properties regarding component spread and dynamic range for bandpass designs. However, these structures sometimes need more opamps in circuit realisation. They are not suitable for lowpass filter design because of a peak in sensitivity at zero frequency.

The SC Right Decomposition approaches can demand fewer opamps in circuit realisation and they demonstrate good sensitivity performance for lowpass designs. Undesirably large component spread and poor dynamic range are unfortunately observed for certain bandpass designs.

2.3.2 Canonical Realisation of Ladder Based SC Filter

An analog VLSI design is a multiple criteria optimisation procedure. One objective in this procedure is to use a minimum number of active components, since these usually occupy relatively large area, consume power, and are sources of noise. With the continued development of personal communication equipment, these considerations will assume even more importance in VLSI circuit design. In active-RC and SC filter design, it is generally accepted that one-opamp-per-pole realisations are canonical for low sensitivity realisation. Circuit configurations with less than one opamp per pole are usually quite sensitive to component deviations, and in the SC case, they would usually require more switches, capacitors, and clock waveforms.

Previous work has shown that the problem of finding a canonical ladder based active filter relies upon finding a canonical ladder prototype[36]. If the order of transfer function is n, then a canonical ladder prototype is a structure with n/2 nodes (for n even) or (n+1)/2 nodes (for n odd). The constraints for a transfer function to be realisable by a canonical doubly-terminated ladder are that numerator of the transfer function of a canonical even-order doubly-terminated ladder is an odd polynomial, and that the numerator of the transfer function of an odd-order doubly-terminated ladder is an odd polynomial if $|C|$ is non-singular or an even polynomial if $|\Gamma|$ is non-singular. For most filter design problems the numerator of the transfer functions are polynomials with purely even or odd terms. So the numerator parity alone determines where a given transfer function can be realised by a canonical standard ladder. The solution is to augment the transfer function, unrealisable by canonical ladder, to

produce the transfer function which is realisable by canonical ladder. When the ladder is simulated by an active circuit the original transfer function behavior is then restored by a change in input circuitry. If H(s) is a transfer function with all its zeros on the imaginary axis or at infinity, then parity manipulation can be effected by s, 1/s, $s/(s^2+\omega_i^2)$. The parity of the modified transfer function H'(s) facilitates realisation by a canonical prototype ladder. A system realising the original transfer function H(s) can be obtained by multiplying the input vector **J** by the inverse of the modifying function.

$$(\mathbf{sC}+s^{-1}\Gamma + \mathbf{G})\mathbf{V}=s^{-1}\mathbf{J} \qquad (2\text{-}14a)$$

$$(\mathbf{sC}+s^{-1}\Gamma + \mathbf{G})\mathbf{V}=s\mathbf{J} \qquad (2\text{-}14b)$$

$$(\mathbf{sC}+s^{-1}\Gamma + \mathbf{G})\mathbf{V}=(s+\omega_i^2 s^{-1})\mathbf{J} \qquad (2\text{-}14c)$$

SC Left Decomposition canonical realisations for systems (2-14a), (2-14b) and (2-14c) become

$$\mathbf{A}_l\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2T\Phi\mathbf{J} \qquad (2\text{-}15a)$$

$$-\Psi\mathbf{W} + \mathbf{A}_r\mathbf{V} = \mathbf{A}_l^{-1}T\mathbf{J}/2 \qquad (2\text{-}15b)$$

$$\mathbf{A}_l\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = \mathbf{0} \qquad (2\text{-}15c)$$

$$-\Psi\mathbf{W} + \mathbf{A}_r\mathbf{V} = 2\mathbf{A}_l^{-1}\mathbf{J}/T \qquad (2\text{-}15d)$$

$$\mathbf{A}_l\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2T\Phi\omega_i^2\mathbf{J} \qquad (2\text{-}15e)$$

$$-\Psi\mathbf{W} + \mathbf{A}_r\mathbf{V} = \mathbf{A}_l^{-1}(T\omega_i^2/2+2/T)\mathbf{J} \qquad (2\text{-}15f)$$

The circuit realisation of Eq.(2-15a,b) and (2-15e,f) retains the basic topology with only the introduction of 2 more switches and 1 more capacitor. The circuit realisation of Eq.(2-15c,d) is very efficient, since **J** has only one non-zero input and if $\mathbf{A}_l^{-1}$ is an

upper triangular matrix, which occurs when **UL** or **IA** decompositions are selected, only one input branch is required.

SC Right Decomposition canonical realisation for systems (2-14a), (2-14b) and (2-14c) are

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{B}_l\mathbf{W} = T\mathbf{J}/2 \qquad (2\text{-}16a)$$

$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = -2T\Psi\mathbf{B}_l{}^{-1}\mathbf{J} \qquad (2\text{-}16b)$$

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{B}_l\mathbf{W} = 2\mathbf{J}/T \qquad (2\text{-}16c)$$

$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = \mathbf{0} \qquad (2\text{-}16d)$$

$$(\mathbf{A} + \Phi\mathbf{D})\mathbf{V} + \Phi\mathbf{B}_l\mathbf{W} = (T\omega_i{}^2/2+2/T)\mathbf{J} \qquad (2\text{-}16e)$$

$$-\Psi\mathbf{B}_r\mathbf{V} + \mathbf{W} = -2T\Psi\mathbf{B}_l{}^{-1}\omega_i{}^2\mathbf{J} \qquad (2\text{-}16f)$$

Eqns.(2-16a,b) and (2-16e,f) will yield identical topologies, having $2N$ more switches than a realisation based on Eq.(2-11a,b). However, Eqns.(2-16c,d) lead to a very efficient circuit realisation with N fewer capacitor input branches than demanded by Eqns.(2-11a,b; e,f).

The *SC Left Inverse Decomposition* canonical realisation form can be written as

$$\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2T\Phi\mathbf{J} \qquad (2\text{-}17a)$$

$$-\Psi\mathbf{A}^{-1}\mathbf{W} + \mathbf{V} = \mathbf{A}^{-1}T\mathbf{J}/2 \qquad (2\text{-}17b)$$

$$\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = \mathbf{0} \qquad (2\text{-}17c)$$

$$-\Psi\mathbf{A}^{-1}\mathbf{W} + \mathbf{V} = 2\mathbf{A}^{-1}\mathbf{J}/T \qquad (2\text{-}17d)$$

$$\mathbf{W} + (\Phi\mathbf{B} + \mathbf{D})\mathbf{V} = 2T\Phi\omega_i{}^2\mathbf{J} \qquad (2\text{-}17e)$$

$$-\Psi A^{-1}W + V = A^{-1}(T\omega_i^2/2+2/T)J \qquad (2\text{-}17f)$$

The realisation of Eq.(2-17c,d) introduces N more capacitors, and Eq.(2-17a,b) and (2-17e,f) have same topologies which introduce $2(N-1)$ switches and $2N$ capacitors.

The *SC Right Inverse Decomposition* canonical realisation forms are

$$(A + \Phi D)V + \Phi W = TJ/2 \qquad (2\text{-}18a)$$

$$-\Psi V + B^{-1}W = -2T\Psi B^{-1}J \qquad (2\text{-}18b)$$

$$(A + \Phi D)V + \Phi W = 2B^{-1}J/T \qquad (2\text{-}18c)$$

$$-\Psi V + B^{-1}W = 0 \qquad (2\text{-}18d)$$

$$(A + \Phi D)V + \Phi W = (T\omega_i^2/2+2/T)J \qquad (2\text{-}18e)$$

$$-\Psi V + B^{-1}W = -2T\Psi B^{-1}\omega_i^2 J \qquad (2\text{-}18f)$$

Eq.(2-18c,d) can produce an efficient circuit realisation and Eq.(2-18a,b) and (2-18e,f) have same topologies which have $2(N-1)$ more switches and N more capacitors.

In all cases of SC canonical design, the UL and IA decompositions are always recommended, since they minimise the number of the input branches significantly and generally produce efficient circuit configurations.

A typical 8th-order bandpass filter which satisfies the specification of a speech processing channel is designed by canonical techniques using the Left-UL decomposition. The circuit response is shown in Fig.2-7 and closely agrees with the approximation. The design statistics for different circuit designs is given in Table 2-8, and the sensitivity comparison of a ladder based design and a cascade based design is

given in Fig.2-8. The lower curve is the sensitivity characteristics of Left-UL realisation and the upper curve is the sensitivity characteristics of K.Martin and A.S.Sedra's[26] biquad cascade realisation.

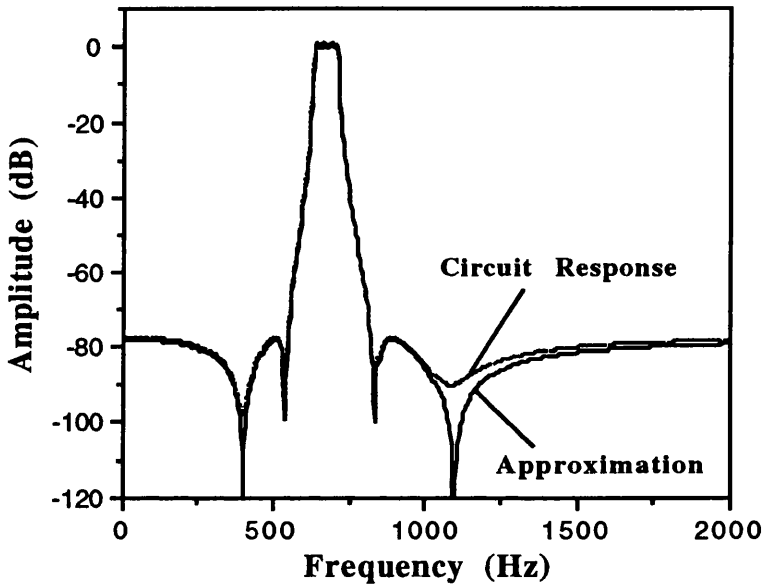


Fig.2-6 8th-order Elliptic canonical SC bandpass filter response

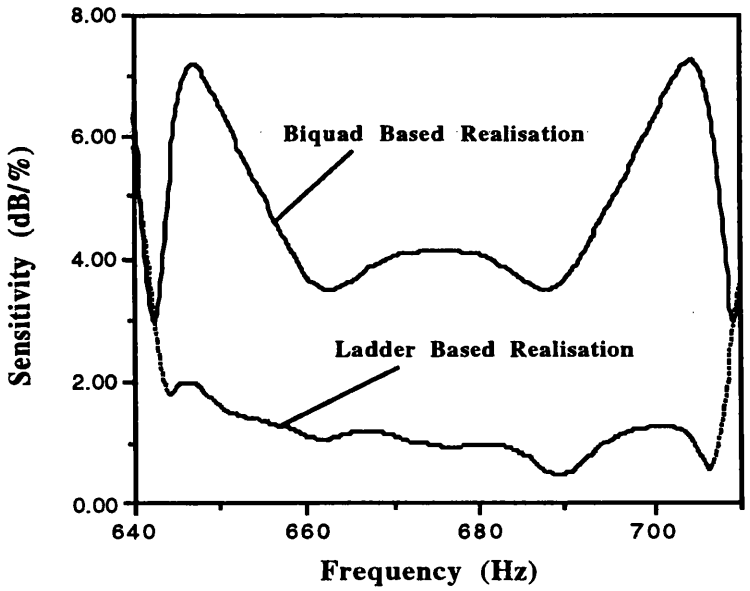


Fig.2-8 Sensitivity comparison of SC ladder based and biquad based filters

	Left-UL	Left-IA	Right-UL	Right-IB	E-F Type[13]	Sedra
No. Opamps	8	8	8	8	8	8
No. C	32	32	32	32	28	28
No. SW	34	34	38	38	34	40
Total C	341	320	356	409	425	393
C Spread	58	54	56	54	77	73

Table 2-8. Statistics of 8th-order SC bandpass filter realisation

2.4 MULTIRATE SC FILTER SYSTEM DESIGN

In previous sections, the single clock frequency SC system design has been studied. In order to address some of the problems encountered in the progress towards single chip realisation of communication front-end systems and the extension to high frequency applications, the multirate SC system is addressed in this section. The main aim of using multirate SC systems is to relax the specifications of the anti-aliasing filters and the speed of some amplifiers, and also reduce the total capacitance and spread in narrow bandpass filters[17,18,37-44].

2.4.1 Multirate SC System Structure

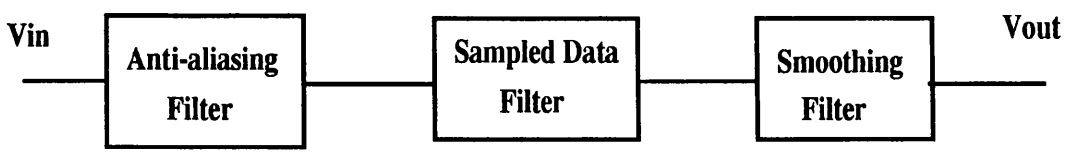


Fig.2-9 An analogue sampled-data filter system

The typical structure of an analogue sampled-data filter system, is illustrated in Fig.2-9. Traditionally only one clock frequency was employed in these systems. To improve

system performance and reduce the cost, the sampled data filter can be a cascade of several sampled data filters using different sampling frequencies, as shown in Fig.2-10. Most commonly, the sampled data filter following the anti-aliasing filter becomes a decimator and the final sampled data filter becomes an interpolator, Fig.2-11.

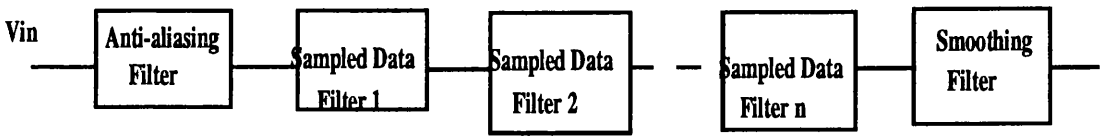


Fig.2-10 Multirate System With Multistage Filters

Fig.2-11 Multirate System With a Decimator and Interpolator

To obtain further reduction of the area, component spread and speed requirements, a multistage, multirate decimator and interpolator structure was developed, Fig.2-12. This structure also yields considerable savings in power consumption.

Fig.2-12 Multirate System With Multistage Decimator and Interpolator

Alternatively, another structure shown in Fig.2-13 can also be used to optimise the system performance.

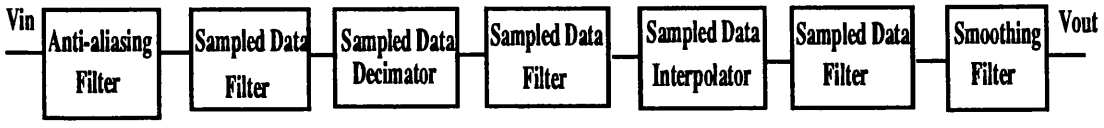


Fig.2-13 Alternate multirate system

The decimators and interpolators have numerous implementations and the sampled data

filter realisations divide into ladder-based and biquad configurations, each with a variety of circuit implementations. From the different multirate structures given above, it is shown that a filter system can be realised by different multirate structures which satisfy all the specifications but with a variety of area, accuracy, power consumption, noise and sensitivity performances. With different cascade and ladder structures for each section, more possibilities for system level trade-off and optimisation are available. The solution of system level optimisation can obtain much better results than that obtained from a fixed structure. However, the cost of system level optimisation is very high and can only be achieved with the aid of a multirate filter CAD system.

2.4.2 Multirate SC System Design Strategies

When a system specification is given, dividing the whole system into a multirate and multistage system is a very efficient way to simplify the design. Various strategies for decomposing the design into multirate and multistage sections are known. For a bandpass filter, a lowpass section and a highpass section with low sampling frequency can be used. A multiband filter system can be designed by several filter sections with different sampling frequencies. A single-path frequency-translated bandpass filter system can also be designed as a multirate structure. However, sometimes combining several sections together can lead to a better design. An alternative scheme can be developed by consdering Fig.2-14 where a decimator implements a sampling rate decrease from MF_S to F_S and an interpolator implements a sampling rate increase from F_S to LF_S.

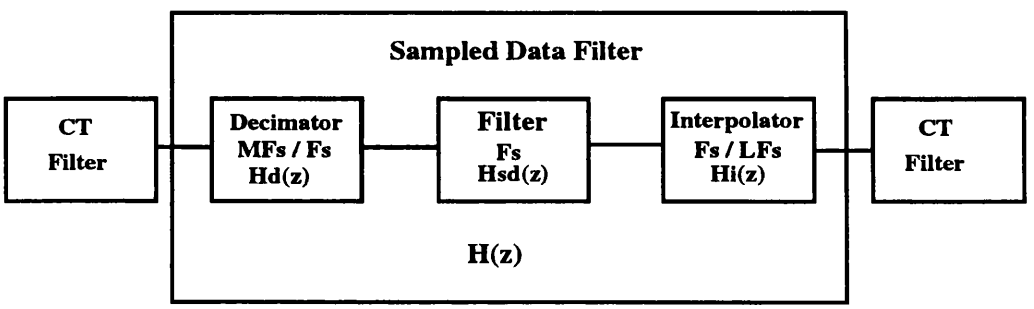


Fig.2-14 Multirate system design example

The transfer function of any decimator or interpolator can be expressed as

$$H_{d/i}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_K z^{-K}}{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots + a_N z^{-N}} \tag{2-19}$$

where the unit delay period corresponds to the high sampling period $1/MF_S$ in decimator case or $1/LF_S$ in the interpolator case. A well known modification of the original z-transfer function (2-19) leads to [45]

$$H_{d/i}(z) = \frac{(b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_K z^{-K}) \sum_{i=0}^{N(M-1)} c_i z^{-i}}{1 + d_1 z^{-1M} + d_2 z^{-2M} + \ldots + d_K z^{-KM}} \tag{2-20}$$

$H_{d/i}(z)$ can be decomposed into two parts. Decompose $H_{d/i}(z)$ as:

$$H_{d/i}(z) = H_1(z) H_2(z) \tag{2-21}$$

where

$$H_1(z) = \left[(b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots + b_K z^{-K}) \sum_{i=0}^{N(M-1)} c_i z^{-i} \right] \tag{2-22}$$

and

$$H_2(z) = \frac{1}{1 + d_1 z^{-1M} + d_2 z^{-2M} + \ldots + d_N z^{-NM}} \tag{2-23}$$

$H_1(z)$ is of FIR transfer function form with sampling frequency MF_C and can be realised by a FIR decimator structure. $H_2(z)$ is of the IIR transfer function form with sampling frequency F_S and can be realised by an IIR decimator.

The transfer function for the whole sampled data system in Fig.2-14 is

$$H(z) = H_D(z) H_{SD}(z) H_I(z) \tag{2-24}$$

where $H_D(z)$ represents the decimator transfer function, $H_{SD}(z)$ for the centre sampled data filter transfer function and $H_I(z)$ for the interpolator transfer function. For the decimator and interpolator, the transfer function can also be expressed as low sampling frequency and high sampling frequency parts.

$$H_I(z) = H_{Ilow}(z)H_{Ihigh}(z) \tag{2-25}$$

and

$$H_D(z) = H_{Dlow}(z)H_{Dhigh}(z) \tag{2-26}$$

Therefore the whole system transfer function can be expressed as

$$H(z) = H_{Dhigh}(z)H_{Dlow}(z)H_{SD}(z)H_{Ilow}(z)H_{Ihigh}(z) \tag{2-27}$$

Instead of following the traditional way by designing the decimator, the sampled data filter and interpolator in straight cascade, a new design methodology is proposed consisting of two FIR filters with the higher sampling frequency and one IIR filter with the lower sampling frequency whose transfer function is

$$H_F(z) = H_{Dlow}(z)H_{SC}(z)H_{Ilow}(z) \tag{2-28}$$

Since each section of the filter system is operated at different sampling frequency, the sin(x)/x effects will cause a shaped passband. Therefore, in multirate system design, the passband correction is necessary in some case. One method to realise these systems is to employ a section to correct any passband error. Optimisation is often used in this stage.

2.4.3.Narrow Baseband Bandpass Filter Design

The design of a narrow band SC bandpass filter is often complicated by large capacitance spread. Large spreads in SC circuit cause the frequency response to be affected by capacitance ratio errors. Beside, large capacitance ratios are not practical for integrated circuit fabrication on account of increased area and sensitivity, reduced yield, and thus increasing the cost of manufacturing. One solution to narrow band bandpass filter design is to employ a multirate technique. Instead of using a lowpass and a highpass filter to construct a bandpass filter, the multirate structure in Fig.2-15 is adopted. The centre bandpass filter with low sampling frequency will reduce capacitance ratio but give rise to unwanted alias and image frequency-translated components at low frequencies, which have to be attenuated using an anti-aliasing filter and an anti-imaging filter, respectively, with increased selectivity.

The design example here is a bandpass filter with maximum ripple 0.28dB, desired midband frequency is 20kHz, and corresponding -3dB bandwidth is 480Hz. It is required that a minimum rejection of 40dB of the alias signals up to 300kHz. Below 300kHz, the frequency bands of the input continuous-time spectrum that relate to the desired system passband have to be attenuated, also by a minimum of 40dB.

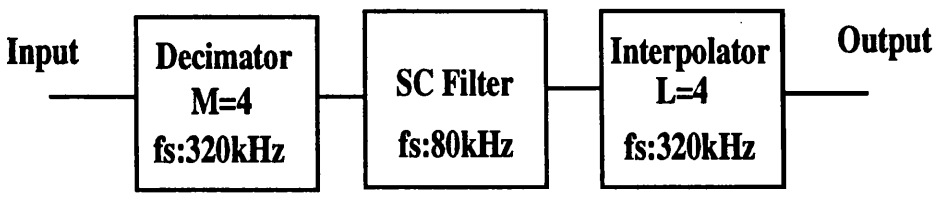


Fig.2-15 Baseband bandpass filter system

Table 2-9 shows the comparison of three different design results. Design 1 is a traditional design using a single rate clock of 320kHz. Design 2[39] obtains an optimum total capacitance and capacitance spread, with a reduction of 8dB of the signal

handling capability of the SC filter and Design 3[39] is a design without loss of signal handling capability. Design 4 is a multirate system implemented by XFILT and the schematic diagram of the circuit is shown in Fig.2-16. In this design, the SC bandpass filter is realised by a Right-BI ladder structure and the decimator and interpolator are implemented by cascading F-damped biquads. From Table 2-9 it can be seen that multirate system have significant advantages over single rate system in capacitance spread. Design 4 also leads to 65% and 39% unit reductions in capacitance spread and total capacitance respectively. Fig.2-17(a) and (b) gives the filter responses around midband and wide frequency band. The cost of multirate structure is the introduction of more opamps, switches and clock waveforms.

	Total C	C Spread	No. opamp	No. C	No. SW	No. ClockWF
Design 1	717	221	6	25	32	2
Design 2	973	88	12	57	75	9
Design 3	1002	151	12	57	75	9
Design 4	436	78	14	57	72	4

Table 2-9. Comparison of Baseband Bandpass Filter Design

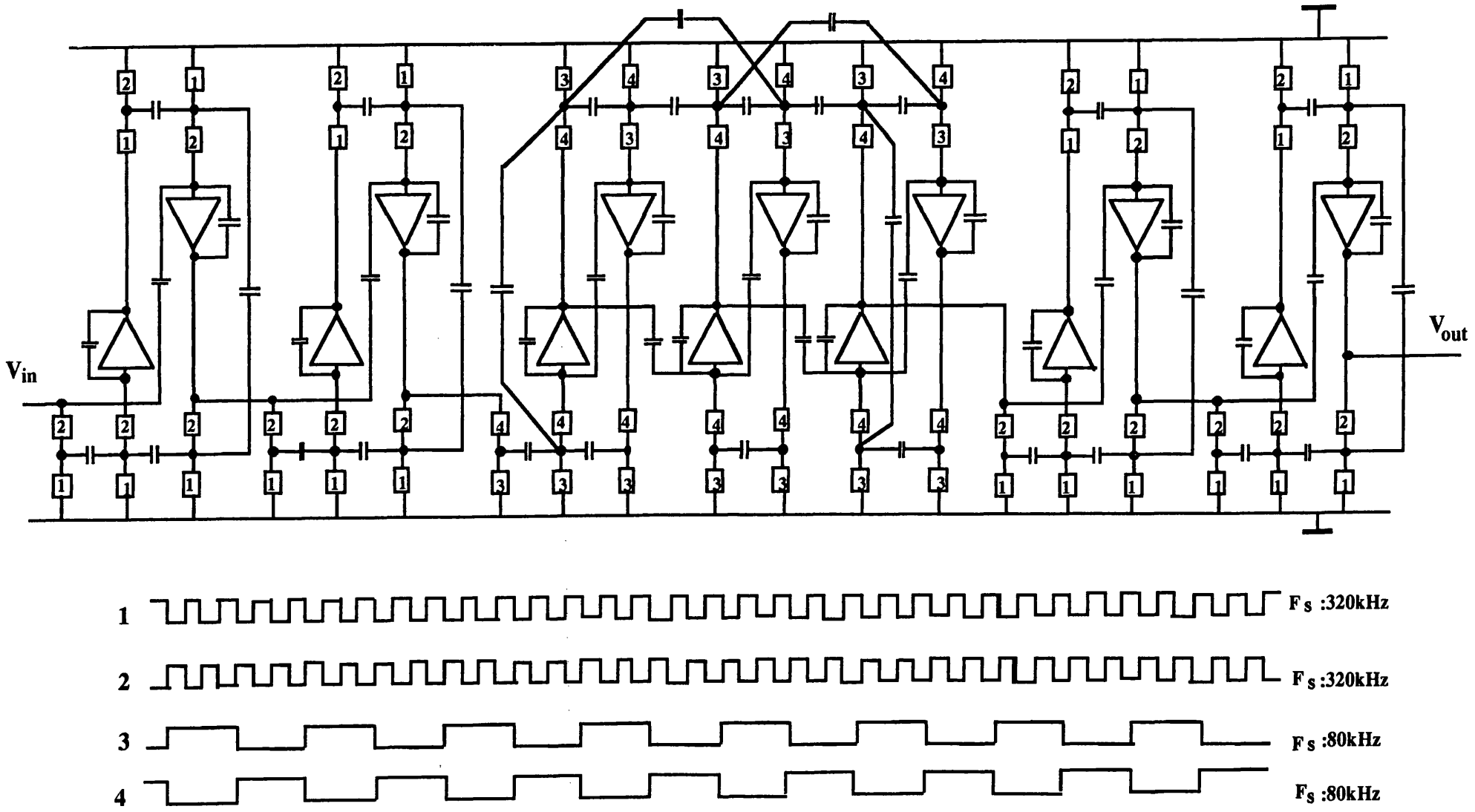
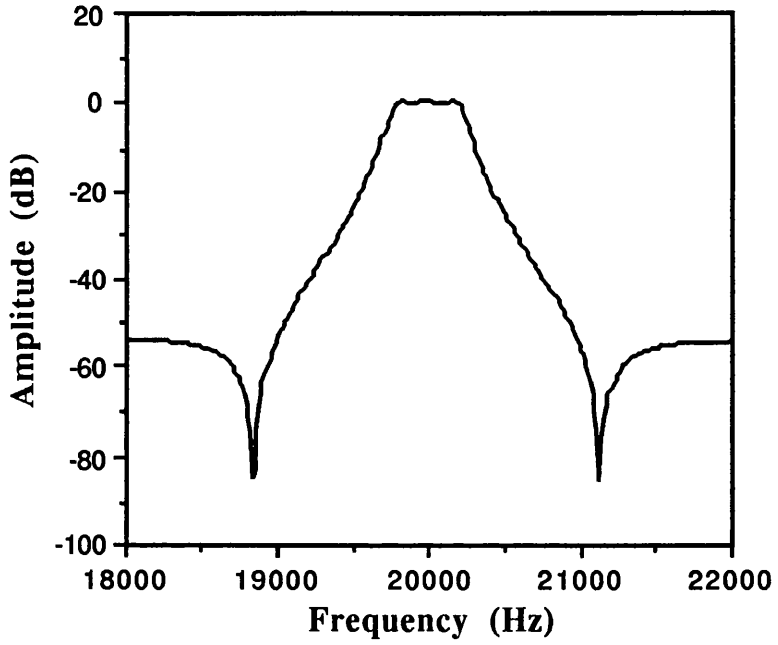
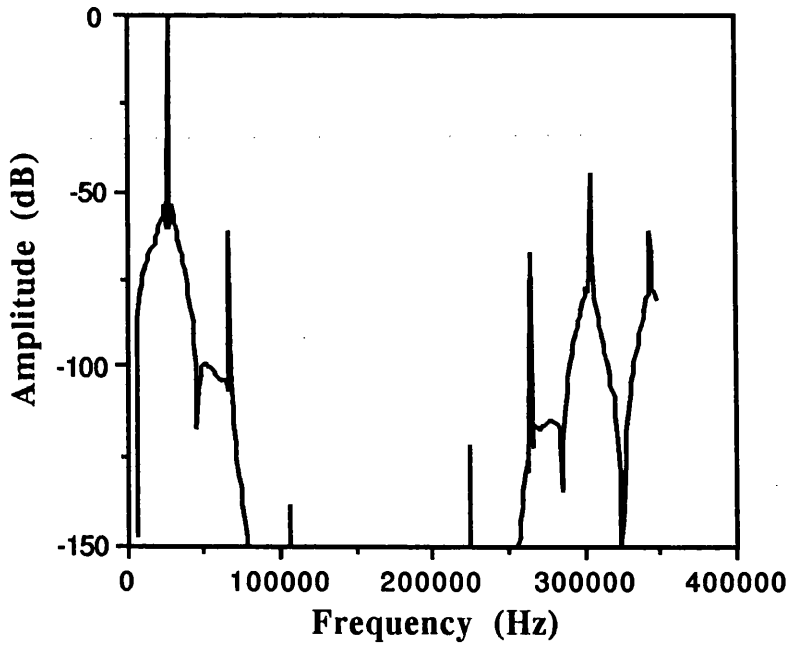


Fig.2-16 Circuit schematic diagram of multirate SC bandpass filter system



(a)



(b)

Fig.2-17 Frequency response of baseband filter

2.4.4 Single-Path Frequency-Translated SC Bandpass Filter Design

Another method for narrow band SC filter design is called single-path frequency-translated (SPFT) approach[17,39,40]. This structure allows a conventional SC bandpass filter with low midband frequency to realise a bandpass response at a much higher frequency and having a correspondingly smaller relative bandwidth. The specifications of the SPFT system designed here are corresponding -3dB bandwidth 80Hz, passband ripple 0.28dB, midband frequency 20kHz, and rejection of unwanted alias and image 35dB up to 170kHz.

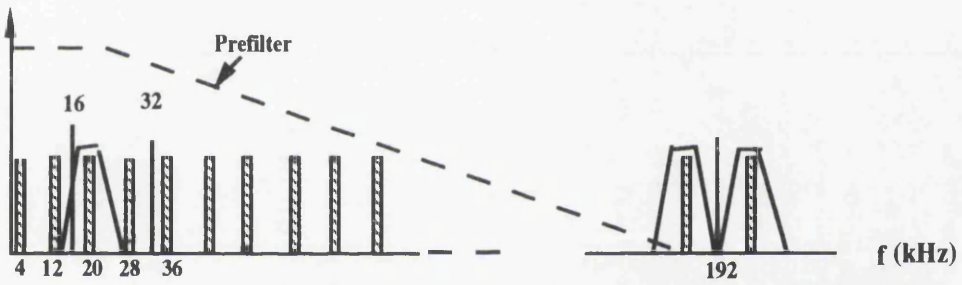


Fig.2-18 Frequency Selection in SPFT System

The frequency selection scheme of SPFT is shown in Fig.2-18. A narrow bandpass filter with a midband frequency of 4kHz is designed. Instead of using a lowpass anti-aliasing and anti-imaging filter to select frequency components below $F_S/2$, the bandpass anti-aliasing and anti-imaging filter are used to recover one of the frequency translated components above $F_S/2$, here f_0 = 20 kHz as shown in Fig.2-18. In the conventional SC bandpass filter system with lowpass anti-aliasing and anti-imaging, the selectivity corresponds to that of the SC bandpass filter. On the contrary, in an SPFT system with bandpass anti-aliasing and anti-imaging filter the selectivity of the SC bandpass system is increased without increasing either the sensitivity or the capacitance spread of the SC bandpass filter. Furthermore, the SPFT system at high midband frequency f_0 employs an SC bandpass filter which operates at much lower midband frequency and therefore, needs simple opamps with low speed and consuming less power. The SPFT system we designed is shown in Fig.2-19, which has three

filters, a decimator and a interpolator. The first and last filter can also be considered as part of decimator and interpolator. The SC bandpass filter in the centre has a midband frequency of 4kHz and sampling frequency 16kHz. The design results and those of Franca are compared in Table 2-10, where Design 1 is a single rate design, Design 2 is a design given by Franca[39] and Design 3 is a design carried out by using XFILT. The circuit schematic diagram is given in Fig.2-20. Since there are more choices available in the filter realisation, a better design in total capacitance and capacitance spread can be obtained. It is shown that for very narrow band filter, multirate structure is a very efficient way for a practical circuit realisation. The frequency response of the SPFT system in f_0 is shown in Fig.2-21(a). Fig.2-21(b) shows the frequency translated component rejection in frequency band.

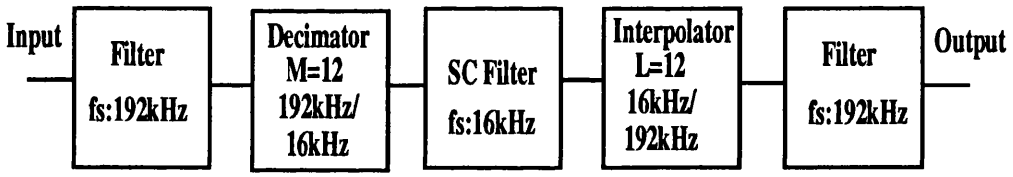


Fig.2-19 SPFT Bandpass Filter System

	Total C	C Spread	No. opamp	No. C	No. SW	No. Clock WF
Design 1	7943	1396	6	25	32	2
Design 2	1148	88	13	64	113	17
Design 3	434	66	14	59	78	4

Table 2-10. Comparison of SPFT System Realisation

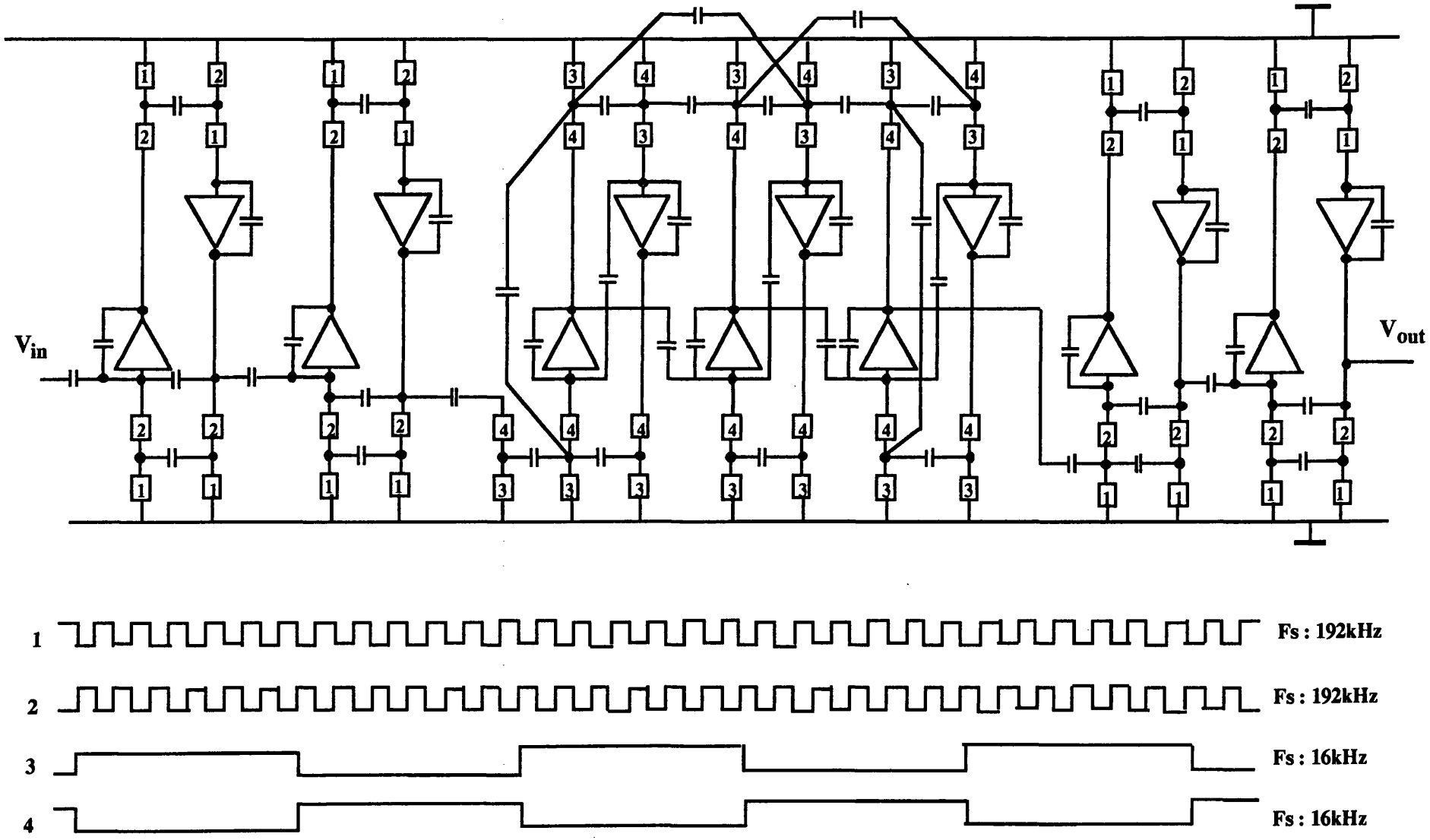
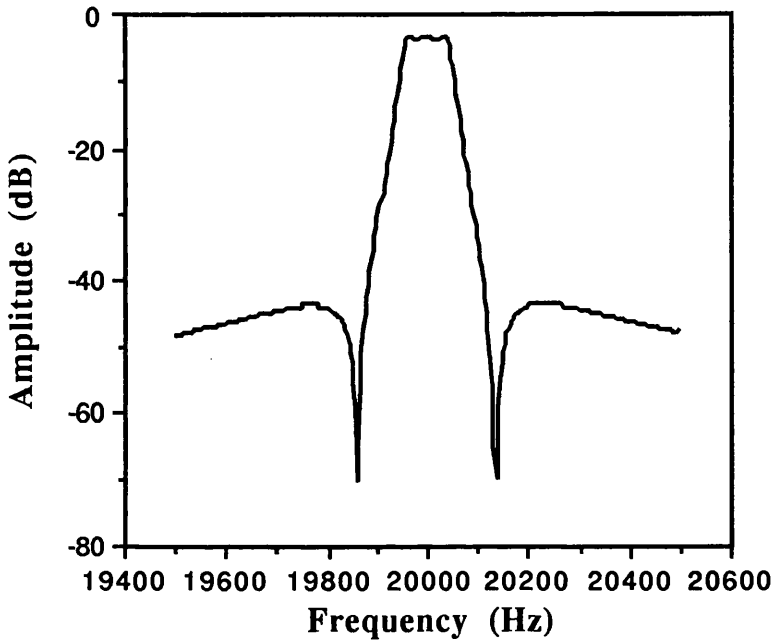
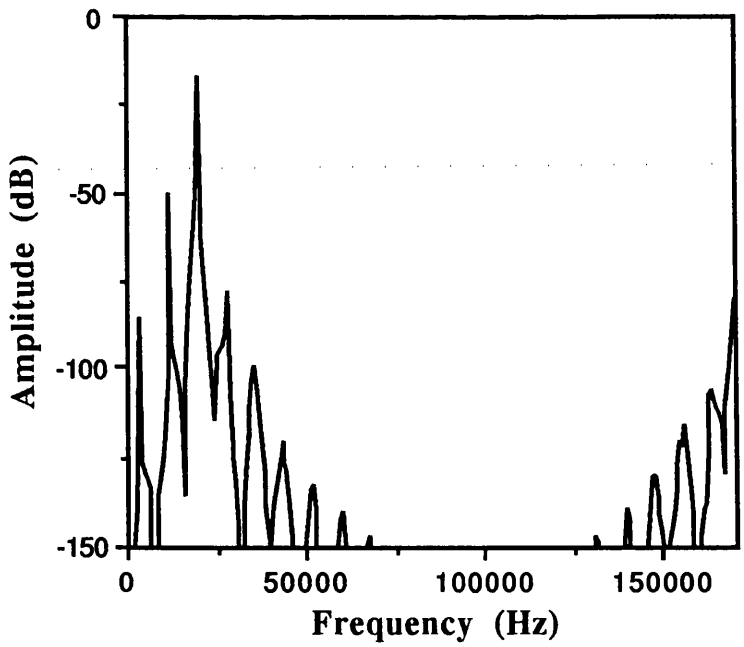


Fig.2-20 Circuit schematic diagram of SPFT filter system



(a)



(b)

Fig.2-21 SPFT system response

2.5. Summary

This chapter consisted of three parts. The first part is covered the cascade SC design approach which included a novel pole-zero pairing method and a comprehensive comparison of SC filters realisation using different SC biquads. By using the XFILT filter compiler, five SC filter systems (lowpass, wide bandpass, narrow bandpass, highpass, and bandstop) were constructed. A comparison for SC filter realisations on total capacitance, capacitance spread, sensitivity, non-idealities, dynamic range and noise performance is given. Some conclusions are obtained as very useful guidelines for the choice of a suitable biquad structure according to the nature of the filter problem.

In the second part, a brief review of matrix design methods for SC filters was given. The canonical realisations of SC filter were studied. An example was given to demonstrate that the proposed canonical design method can be efficient.

The final part discussed multirate SC system design. The strategies and the algorithms for multirate SC system design were presented. A narrow baseband bandpass filter and a single-path frequency-translated SC bandpass filter are given as examples.

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Chapter 3: Transconductor-Capacitor Filter Design

CHAPTER 3: TRANSCONDUCTOR-CAPACITOR FILTER DESIGN

3.1. INTRODUCTION

SC filters have been applied successfully to many applications and are used routinely in analogue CMOS circuits. There are however a number of application areas, such as video signal processing, in which they are not easily applicable due to the high signal frequencies involved. Usually the clock frequency is designed to be several tens of times the passband frequencies, and the fastest rate at which CMOS SC circuit can settle satisfactorily is a few MHz, therefore such filters are not often designed with passband frequencies greater than several tens of kHz. Occasionally SC filters have been reported with passband frequencies greater than 1MHz[1,2], however they are difficult to design, consume a large amount of current and generate a lot of clock noise. The requirement for fast settling amplifiers can be met by using GaAs technologies[3,4], but this solution is expensive both in terms of the cost of the process and the power supply current used. Another drawback of SC filters in high frequency applications is the fact that they are "sampled data" in nature. Some applications, such as anti-aliasing filtering for video ADCs, require a continuous time solution. All of these reasons have motivated an alternative type of monolithically integrated, accurate tunable and continuous time filter : the Transconductor-Capacitor Filter.

The transconductor is an active circuit which generates an output current directly proportional to an input voltage, the constant of transconductance being adjustable by a d.c bias (or control) voltage. Its function can be analogous to that of both the resistors and opamps in an active-RC filter, therefore the only other components that are essential to complete a transconductor filter are capacitors. However, additional

components are usually required to form a control loop which sets the control voltage such that the filter is correctly scaled in frequency with respect to the frequency of a reference clock signal.

Like other active filters, a transconductor-capacitor filter can be designed as a cascade of biquadratic stages [5-8], or as a simulation of a passive RLC ladder[9-13]. The former architecture appears to be preferable for those transconductor-capacitor filters which are of such high frequency and selectivity that multiple control loops are required[5,7], and the latter is generally preferable due to their lower sensitivity to component value tolerances[14].

3.2 Cascade Transconductor-Capacitor Filter Design

In the transconductor-capacitor filter design field most practical design approaches are based on cascade method. This is because of the serious and challenging problem of having to tune the filter by some automatic on-chip method[6-10], to compensate for fabrication tolerances, parasitic effects, and component drifts during operation. When designing cascaded integrated-based transconductor-capacitor filter structures, it may be the case that the input impedance of some stages is not infinite. If that is the case, a unity gain buffer would be required for coupling, since the output impedance of all integrators are nonzero.

The first-order sections used in XFILT are given in Fig.3-1[15] and the circuit transfer functions are given in (3-1a,b,c).

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC + g_m} \tag{3-1a}$$

$$\frac{V_{out}}{V_{in}} = \frac{sC}{sC + g_m} \tag{3-1b}$$

$$\frac{V_{out}}{V_{in}} = \frac{sC + g_{m1}}{sC + g_{m2}} \tag{3-1c}$$

Fig.3-1(a) is a first-order lowpass section. The 3dB cutoff frequency is given by the expression $f_{3db}=g_m/2\pi C$. Linear adjustment of f_{3dB} with g_m is attainable with this circuit while maintaining a unity dc frequency gain. The highpass structure is shown in Fig.3-1(b), which also has a 3dB cutoff frequency given by $f_{3db}=g_m/2\pi C$. It can be observed that the characteristic networks for the lowpass and highpass structures of Fig.3-1(a) and (b) are identical, and thus they have the same pole structures.

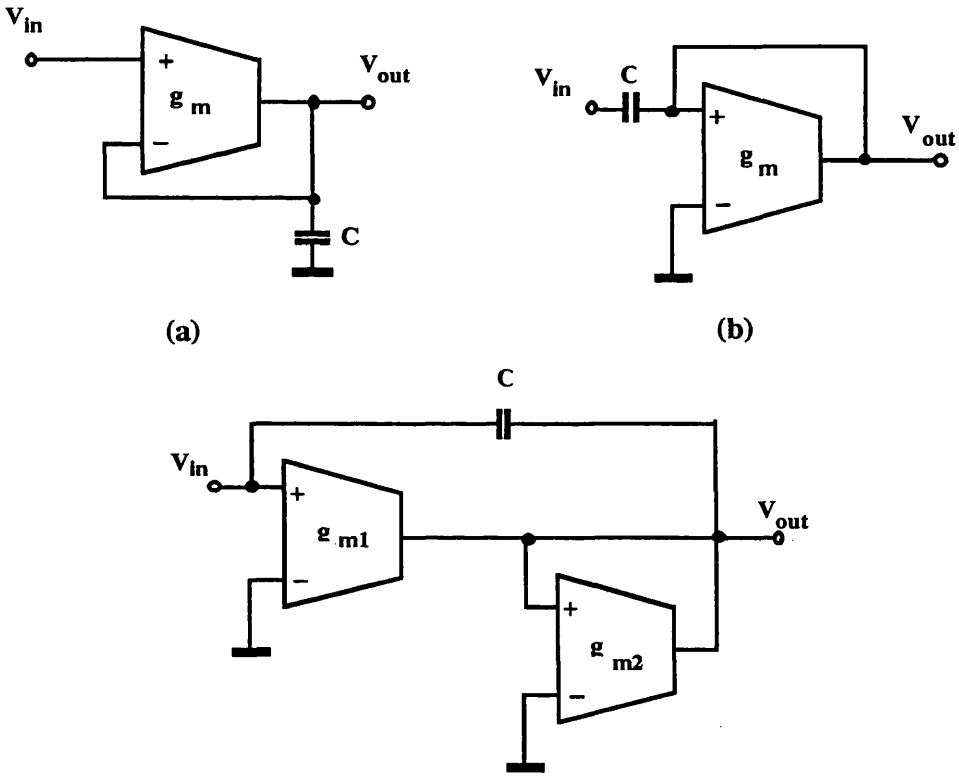

Fig.3-1 First-Order Transconductor-Capacitor Section

(a).Lowpass First-Order Section

(b).Highpass First-Order Section

(c).Allpass First-Order Section

The circuit of Fig.3-1(c) utilises an additional transconductor and offers considerable flexibility. If g_{m1} and g_{m2} are adjusted simultaneously, then a fixed pole-zero ratio and hence, shape preserving response is possible. In this case, the circuit can be lowpass, allpass, or highpass, depending upon the g_{m1}/g_{m2} ratio. If the "+" and "-" terminals of g_{m1} are interchanged and the transconductance gains are adjusted so that $g_{m1}=g_{m2}$, the circuit behaves as a phase equaliser. The general second-order biquad structure is shown in Fig.3-2[15]. The transfer function is given by

$$V_{out} = \frac{s^2C_1C_2V_C + sC_1g_{m4}V_B + g_{m2}g_{m5}V_A}{s^2C_1C_2 + sC_1g_{m3} + g_{m2}g_{m1}} \qquad (3\text{-}2)$$

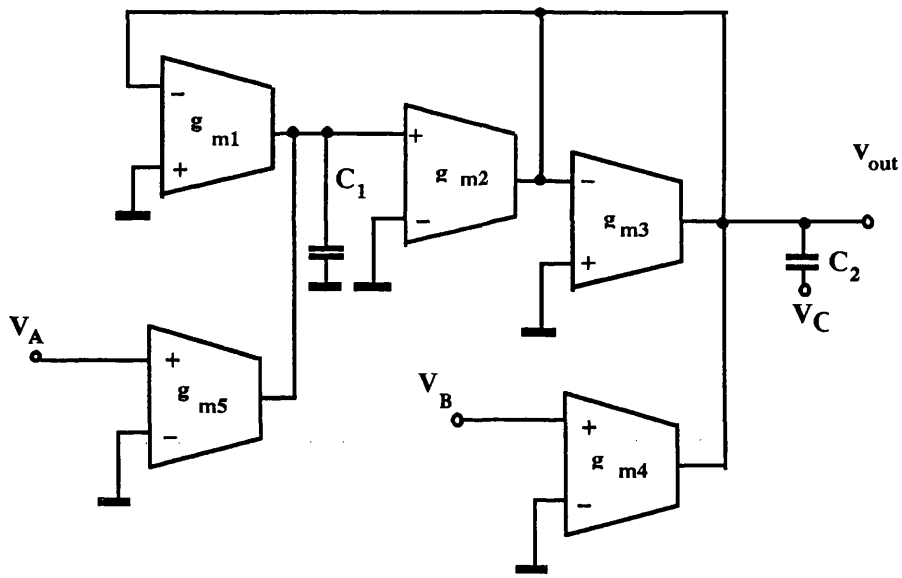

Fig.3-2 General Biquadratic Transconductor-Capacitor Structure

The potential for tuning the w_0 and Q for both the poles and zeros (when $V_i=V_a=V_b=V_c$) to any desired value is apparent. Although somewhat expensive in components, it can be argued that if there is to be capability for completely arbitrary location of a pair of poles and a pair of zeros via adjustment of the transconductance gain of the transconductor, then at least four degrees of freedom and, hence, four transconductors are required. This circuit uses only one more than the minimum. The

capability for various types of pole and/or zero movement through the simultaneous adjustment of two or more of the transconductance gains is also apparent. Many other biquadratic structures, some of which offer more flexibility at the expense of additional complexity, also exist but are not implemented in XFILT at present. Since the software is designed to facilitate the addition of more biquadratic sections, there is no difficulty in adding new biquadratic transconductor-capacitor structures.

By matching the coefficients of a general biquadratic transfer function

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{ms^2 + cs + d}{s^2 + as + b} \tag{3-3}$$

with that of (3-1), a set of design equations with positive gm coefficients is obtained as follows:

$$\begin{aligned} g_{m1} &= g_{m2} = C_1 b^{1/2} \\ g_{m3} &= aC_1 \\ g_{m4} &= cC_1/m \\ g_{m5} &= dC_1/mb^{1/2} \\ g_{m6} &= mC_1 b^{1/2} \\ g_{m7} &= C_1 b^{1/2} \end{aligned} \tag{3-4}$$

where C_1 and C_2 are the free parameters. Note that depending on the numerator coefficients, g_{m4} or g_{m5} may be not necessary. In these cases, only three or four transconductors are required. The values of C_1 and C_2 are chosen to obtain convenient element values.

As an example, a 8th-order bandstop elliptic filter is designed. The filter has 40dB attenuation from 800kHz to 1.2MHz and 1.5dB passband ripple. This filter design

will encounter the canonical realisation problem in any ladder based design approach. Fig.3-3 gives frequency response of cascade circuit realisation.

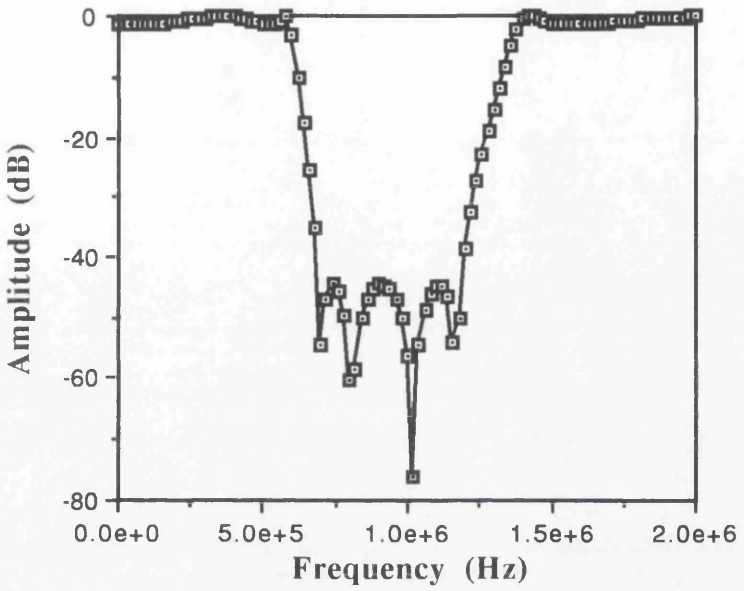

Fig.3-3 8th-order Bandstop Cascade Transconductor-Capacitor Filter Response

3.3.LADDER BASED TRANSCONDUCTOR-CAPACITOR FILTER DESIGN METHOD

Ladder based transconductor-C filters are commonly implemented using signal-flow graph techniques. These techniques have been applied successfully to the design of lowpass filter but they cannot generally be applied to bandpass ladders without the use of ratioed transconductor inputs[13,19]. The problem is compounded for prototypes containing inductor loops or unequal termination resistors since these imply non-integer ratios that cannot be implemented by combinations of a unit transconductance. Moreover existing ladder based transconductor-C filter realisations were invariably for specific circuit topologies and lack generality. The matrix approach for SC filter design has been extended to include transconductor-C realisations[16]. With the matrix method, the realisation of highly selective bandpass filters can be made by using a low impedance input transconductors with equal values of transconductance. The

matrix design method with its compact form is well suited for and compatible with CAD software development[17] and has been successfully used in designing several practical transconductor-C filters and equalisers[16,18].

3.3.1 Matrix Based Ladder Transconductor-Capacitor Filter Design Method

There are two main types of matrix based ladder transconductor-C filter realisations, these are Topological Decomposition and Inverse Decomposition. Inverse Decomposition is again divided into Right and Left Inverse Decomposition. The building blocks for circuit realisation utilising both conventional transconductors and low impedance input transconductors[19] are given in Fig.3-4(a) and Fig.3-4(b). In Fig.3-4(a) the capacitor C_i (i=1,2,3...) can only realise a bidirectional path when driven by internal nodes, since most of the input voltages will be from the high impedance outputs of other transconductors. To facilitate the realisation of some decompositions, the low impedance input transconductors are required, these also have the added attraction of being insensitive to the effects of botttom plate parasitic capacitance.

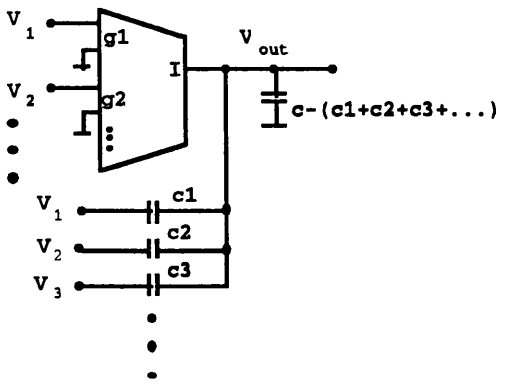

Fig.3-4(a) First Order Section Using Conventional Transconductor

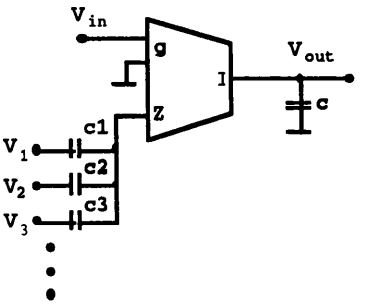

Fig.3-4(b) First Order Section Using Transconductor With Low Impedance Inputs

a)*TC Topological Decomposition*

In the topological decomposition,

$$\Gamma=\mathbf{A}\mathbf{D}\mathbf{A}^{T} \tag{3-5}$$

where **D** is a diagonal matrix of the inverse inductance values of the prototype, **A** is a conventional incidence matrix of inductors, the auxiliary variables are defined by:

$$\mathbf{W}=(sg)^{-1}\mathbf{D}\mathbf{A}^{T}\mathbf{V} \tag{3-6}$$

where g is a scaling factor with the dimension of transconductance, often set as $g=1/\alpha R$ where the R is the ladder filter terminating resistor and α takes an optimum value close to the fractional bandwidth of the filter.

Substituting (3-5) and (3-6) into (2-5) and rearranging gives

$$s^{-1}g\mathbf{A}\mathbf{W}+(\mathbf{C}+s^{-1}\mathbf{G})\mathbf{V}=s^{-1}\mathbf{J} \tag{3-7a}$$

$$g^{2}\mathbf{D}^{-1}\mathbf{W}-s^{-1}g\mathbf{A}^{T}\mathbf{V}=\mathbf{0} \tag{3-7b}$$

If the prototype ladder is equally terminated, the filter can be realised with one value transconductance. In transconductor-capacitor realisation, the entries in non-integrated matrices are realised by capacitors while the components in integrated matrices are implemented by transconductances. Here we define a matrix multiplied by s^{-1} an integrated matrix. All non-integrated matrices in Topological Decomposition are symmetrical, so the realisation can utilise both conventional and low impedance input transconductor structures. The auxiliary voltages **W** are directly proportional to the currents in the inductors of the prototype ladder. The topological decomposition will generally lead to equivalent leapfrog topologies in active-RC and SC and

transconductance-capacitor designs, if conventional transconductors are used. In the bandpass case, this decomposition can not be guaranteed to generate stable active circuits and alternative decompositions are required[20].

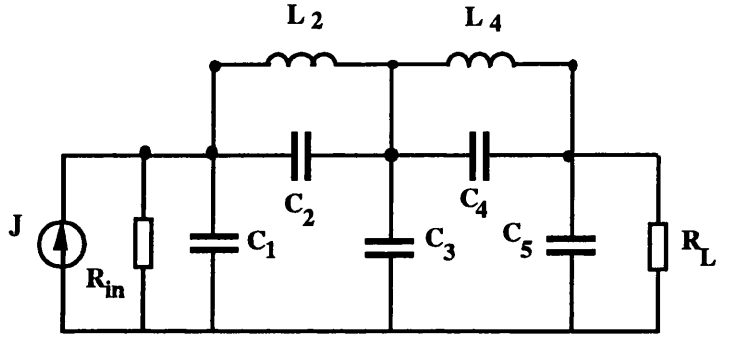

Fig.3-5 Lowpass 5th-order Ladder With Finite Transmission Zeros

As an example, consider the 5th-order elliptic prototype ladder lowpass filter with finite transmission shown in Fig.3-5. For this ladder prototype the vectors and matrices in (3-7a) and (3-7b) take the form

$$J=\begin{pmatrix} Vin/Rin \\ 0 \\ 0 \end{pmatrix} \quad V=\begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix}$$

$$A=\begin{pmatrix} 1 & 0 \\ -1 & 1 \\ 0 & -1 \end{pmatrix} \quad D=\begin{pmatrix} L_2^{-1} & 0 \\ 0 & L_4^{-1} \end{pmatrix} \quad C=\begin{pmatrix} C_1+C_2 & -C_2 & 0 \\ -C_2 & C_2+C_3+C_4 & -C_4 \\ 0 & -C_4 & C_4+C_5 \end{pmatrix}$$

$$\Gamma=\begin{pmatrix} L_2^{-1} & -L_2^{-1} & 0 \\ -L_2^{-1} & L_2^{-1}+L_4^{-1} & -L_4^{-1} \\ 0 & -L_4^{-1} & L_4^{-1} \end{pmatrix} \quad G=\begin{pmatrix} R_{in}^{-1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_L^{-1} \end{pmatrix}$$

(3-8a-g)

Substituting these into (3-7a) and (3-7b), gives the variables explicitly :

$$V_1 = \{(V_{in}-V_1)/R_{in}-gW_1\}/S(C_1+C_2)+C_2V_2/(C_1+C_2)$$

$$V_2 = g(W_1-W_2)/SC(C_2+C_3+C_4)+C_2V_1/(C_2+C_3+C_4)+C_4V_3/(C_2+C_3+C_4)$$

$$V_3 = (-V_3/R_L+gW_2)/S(C_4+C_5)+C_4V_2/(C_4+C_5)$$

$$W_1 = (V_1-V_2)/SgL_2$$

$$W_2 = (V_2-V_3)/SgL_4$$

(3-9)

The equations (3-9) can be simulated by the circuit in Fig.3-6(a) using conventional transconductors and Fig.3-6(b) using low impedance input transconductors. In the conventional transconductor-capacitor realisation the circuit structure has now introduced two floating capacitors. In this circuit five differential transconductors with equal transconductance are used. Two transconductors are used in the implementation of terminations. If $R_L=R_{in}=1/g$, only six transconductors are needed. In circuit realisation using low impedance transconductor, still seven transconductors with same spread as conventional structure are used, however since no floating capacitors are presented in this circuit, the bottom plate parasitics problem can be overcome.

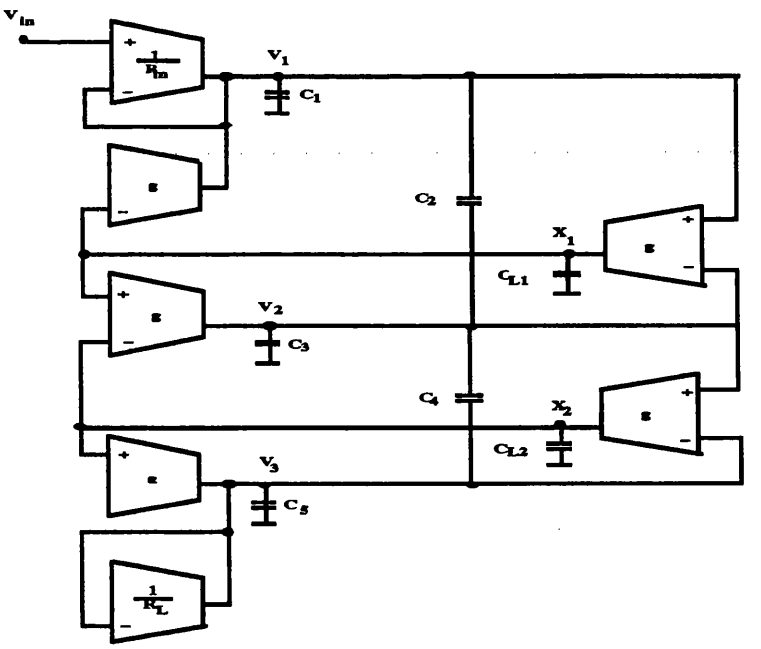

Fig.3-6(a) TC Realisation of the Filter in Fig.3-5 (With Conventional Transconductors)

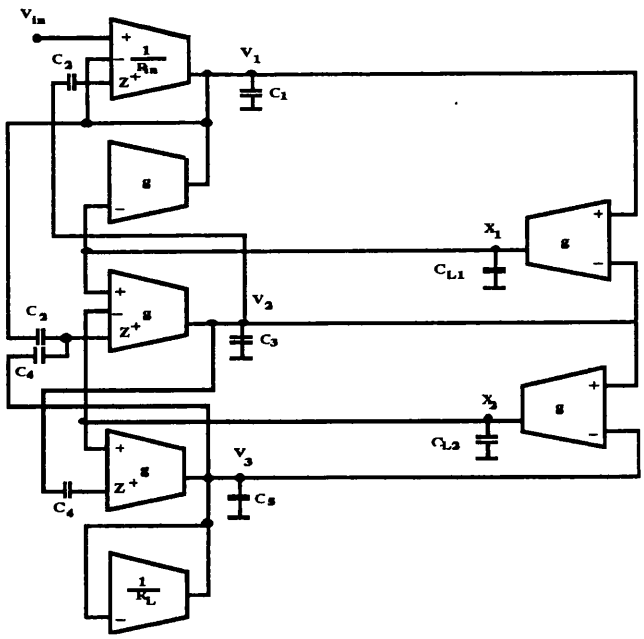

Fig.3-6(b) TC Realisation of the Filter in Fig.3-5 (With Low Impedance Transconductors)

b)*TC Right Inverse Decomposition*

The auxiliary variables are defined by

$$\mathbf{W}=(s^{-1}\Gamma\mathbf{V})/g \tag{3-10}$$

The resulting design matrix equations are:

$$g^2\Gamma^{-1}\mathbf{W}-s^{-1}g\mathbf{V}=\mathbf{0} \tag{3-11a}$$

$$s^{-1}g\mathbf{W}+(\mathbf{C}+s^{-1}\mathbf{G})\mathbf{V}=s^{-1}\mathbf{J} \tag{3-11b}$$

In (3-11), the integrated vector V is premultiplied by a matrix **G**. Only when the prototype ladder has equal resistance at both terminations, would the transconductor-capacitor filter require one transconductance value in the complete realisation. Because all the non-integrated matrices in TC Right Inverse Decomposition are symmetrical, it

can be realised both using conventional transconductor and low impedance input transconductor building blocks. In the final design, parasitic capacitances have to be estimated and the circuit capacitances adjusted accordingly.

c)*TC Left Inverse Decomposition*

The Left Inverse Decomposition results from decomposing the C matrix into two matrices $\mathbf{C}_l$ and $\mathbf{C}_r$. Defining the vector of auxiliary variables by

$$\mathbf{W} = (s\mathbf{C}_r\mathbf{V})/g \tag{3-12}$$

The general *TC Left Inverse Decomposition* design equations are obtained by substituting (3-12) into (2-5) and rearranging (2-5):

$$g^2\Gamma^{-1}\mathbf{C}_l\mathbf{W} + (s^{-1}g + g\Gamma^{-1}\mathbf{G})\mathbf{V} = g\Gamma^{-1}\mathbf{J} \tag{3-13a}$$

$$-s^{-1}g\mathbf{W} + \mathbf{C}_r\mathbf{V} = \mathbf{0} \tag{3-13b}$$

Only low impedance input transconductors can be used in the realisation of Eq.(3-13a,b), because some of the non-integrated matrices are asymmetric. For $\mathbf{C}_l = \mathbf{I}$ and $\mathbf{C}_r = \mathbf{C}$, *TC Left-IC Decomposition* can be obtained from (3-13a,b) as:

$$g^2\Gamma^{-1}\mathbf{W} + (s^{-1}g + g\Gamma^{-1}\mathbf{G})\mathbf{V} = g\Gamma^{-1}\mathbf{J} \tag{3-14a}$$

$$-s^{-1}g\mathbf{W} + \mathbf{C}\mathbf{V} = \mathbf{0} \tag{3-14b}$$

Since Γ^{-1} and C are generally full and tridiagonal respectively, a relatively large number of capacitors is required in the circuit realisation. However since all non-integrated matrices
($\Gamma^{-1}\mathbf{G}$ and C) are symmetric, they can be implemented using conventional transconductors.

When $\mathbf{C}_l = \mathbf{C}$ and $\mathbf{C}_r = \mathbf{I}$, the *TC Left-CI Decomposition* is obtained:

$$g^2\Gamma^{-1}\mathbf{C}\mathbf{W}+(s^{-1}g+g\Gamma^{-1}\mathbf{G})\mathbf{V} = g\Gamma^{-1}\mathbf{J} \qquad (3\text{-}15a)$$

$$-s^{-1}g\mathbf{W}+\mathbf{V} = \mathbf{0} \qquad (3\text{-}15b)$$

This requires fewer capacitors than Left-IC because the only coupling capacitors are those of the product matrix $\Gamma^{-1}\mathbf{C}$. These coupling paths must be implemented using low impedance inputs since $\Gamma^{-1}\mathbf{C}$ is generally asymmetric.

The important feature of equations (3-13) to (3-15) is that all of the integrated vectors are multiplied by a single constant g, this allows the equations to be implemented as a transconductor-capacitor circuit with a single value of transconductance.

3.3.2 Canonical Ladder Transconductor-Capacitor Filter Definitions

In active-RC and SC filter design, it is generally accepted that **one-opamp-per-pole realisations are canonical** for low sensitivity realisation[21]. For transconductor-C filter ladder-based realisation with conventional transconductors, two extra transconductors are needed for realisation of the passive prototype ladder terminations. We define ***a canonical transconductor-C filter with conventional transconductors as a one-transconductor-per-pole realisation plus two termination transconductors, each possessing the same value of transconductance. A transconductor-C filter with conventional transconductors, which has one-transconductor-per-pole and two termination transconductors, with a small number ($\leq$ 3) of different transconductance values, is defined as quasi-canonical realisation.***

If the transconductor-C filter is realised using low-impedance transconductors, two transconductors for the termination realisation can be replaced by capacitance branches. Therefore we define ***a canonical transconductor-C filter with low-impedance transconductors as a one-transconductor-per-pole realisation, each possessing the same value of transconductance. A transconductor-C filter with low-impedance transconductors, which has one-transconductor-per-pole, with a small number ($\leq$ 3) of different transconductance values, is defined as quasi-canonical realisation***[22].

3.3.3. Transfer Function Modification Approach for Transconductor-Capacitor Canonical Realisation

a)*TC Topological Decomposition*

The design equations for a canonical topological decomposition is obtained by substituting (3-7a,b) into (2-14a,b,c) and are shown as

$$\mathbf{CV} = -s^{-1}[\mathbf{AgW}+\mathbf{GV}] \qquad (3\text{-}16a)$$

$$\mathbf{W}=(sg)^{-1}[\mathbf{DA}^{T}\mathbf{V}-\mathbf{JA}^{-1}] \qquad (3\text{-}16b)$$

$$\mathbf{CV} = s^{-1}[\mathbf{sJ}-\mathbf{AgW}-\mathbf{GV}] \qquad (3\text{-}16c)$$

$$\mathbf{W}=(sg)^{-1}\mathbf{DA}^{T}\mathbf{V} \qquad (3\text{-}16d)$$

$$\mathbf{CV} = s^{-1}[\mathbf{sJ}-\mathbf{AgW}-\mathbf{GV}] \qquad (3\text{-}16e)$$

$$\mathbf{W}=(sg)^{-1}[\mathbf{DA}^{T}\mathbf{V}-\mathbf{JA}^{-1}\omega_{i}^{2}] \qquad (3\text{-}16f)$$

The validity of these equations is dependent upon A being square and A having an inverse, which is not usually the case. Even when A is square and invertable, the implementation of

$s^{-1}\mathbf{A}^{-1}\mathbf{J}$ in Eq.(3-16b) and $s^{-1}\mathbf{A}^{-1}\omega_i^2\mathbf{J}$ in Eq.(3-16f) would introduce a extra n (dimension of A matrix) transconductors with different transconductance values, and this destroys the main advantage of a ladder based transconductor-capacitor filter. However, Eq.(3-16c,d) will always yield an efficient circuit structure no matter what form of A matrix is.

b)*Right Inverse Decomposition*

The canonical realisations are written as

$$\mathbf{CV}=-s^{-1}(\mathbf{GV}+g\mathbf{W}) \qquad (3\text{-}17a)$$

$$\Gamma^{-1}\mathbf{W}=(sg)^{-1}(\mathbf{V}-\Gamma^{-1}\mathbf{J}) \qquad (3\text{-}17b)$$

$$\mathbf{CV}=\mathbf{J}-s^{-1}(\mathbf{GV}+g\mathbf{W}) \qquad (3\text{-}17c)$$

$$\Gamma^{-1}\mathbf{W}=(sg)^{-1}\mathbf{V} \qquad (3\text{-}15d)$$

$$\mathbf{CV}=\mathbf{J}-s^{-1}(\mathbf{GV}+g\mathbf{W}) \qquad (3\text{-}17e)$$

$$\Gamma^{-1}\mathbf{W}=(sg)^{-1}(\mathbf{V}-\omega_i^2\Gamma^{-1}\mathbf{J}) \qquad (3\text{-}17f)$$

The terms $(sg)^{-1}\Gamma^{-1}\mathbf{J}$ in Eq.(3-17b) and $(sg)^{-1}\omega_i^2\Gamma^{-1}\mathbf{J}$ in Eq.(3-17f) can only be realised by n extra transconductors with different transconductance values. However for Eq.(3-17c,d), an efficient circuit realisation can be obtained.

c)*TC Left Inverse Decomposition*

Only the canonical realisation for Eq.(3-14) is given here, the other variations on the *TC Left Inverse Decomposition* method give exactly the same results. The canonical realisation can be written as

Only the canonical realisation for Eq.(3-14) is given here, the other variations on the *TC Left Inverse Decomposition* method give exactly the same results. The canonical realisation can be written as

$$\mathbf{CV}=s^{-1}g\mathbf{W} \tag{3-18a}$$

$$g^2\Gamma^{-1}\mathbf{W}=s^{-1}g\Gamma^{-1}\mathbf{J}-g\Gamma^{-1}\mathbf{GV}-s^{-1}g\mathbf{V} \tag{3-18b}$$

$$\mathbf{CV}=s^{-1}g\mathbf{W}+\mathbf{J} \tag{3-18c}$$

$$g^2\Gamma^{-1}\mathbf{W}=-g\Gamma^{-1}\mathbf{GV}-s^{-1}g\mathbf{V} \tag{3-18d}$$

$$\mathbf{CV}=s^{-1}g\mathbf{W}+\mathbf{J} \tag{3-18e}$$

$$g^2\Gamma^{-1}\mathbf{W}=s^{-1}g\Gamma^{-1}\omega_i^2\mathbf{J}-g\Gamma^{-1}\mathbf{GV}-s^{-1}g\mathbf{V} \tag{3-18f}$$

The terms $s^{-1}g\Gamma^{-1}\mathbf{J}$ in Eq.(3-18b) and $s^{-1}g\Gamma^{-1}\omega_i^2\mathbf{J}$ in Eq.(3-18f) can only be realised by n extra transconductors with different transconductance values. Only Eq.(3-18c,d) can be realised by a canonical form.

As an example, we consider the design of an 8th-order Butterworth bandpass transconductor-C filter. The transfer function for this filter is of the form

$$H(s)=\frac{s^4}{(s^2+p_1^2)(s^2+p_2^2)(s^2+p_3^2)(s^2+p_4^2)} \tag{3-19}$$

Because the transfer function has even order denominator with even order numerator, it cannot immediately be realised in canonical form. Actually, the ladder derived from the transfer function is shown in Fig.3-7, which has 5 nodes, so it requires fifth order matrices, which in turn would lead to a tenth order transconductor-capacitor filter as shown in Fig.3-8.

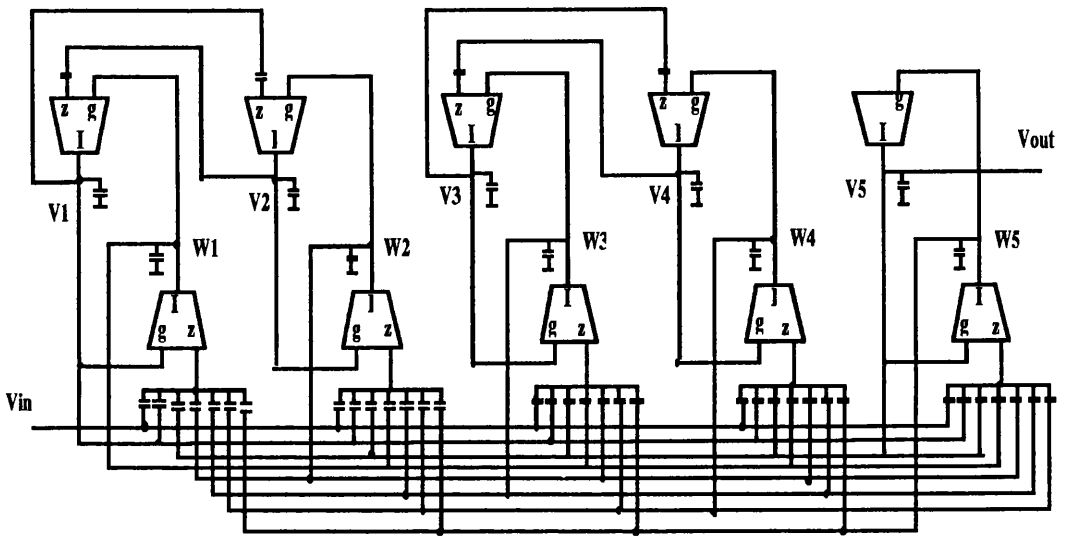

Fig.3-8 Transconductor-C filter based on prototype in Fig.3-7

If the canonical design approach is applied, the transfer function is changed to the form

$$H(s) = \frac{s^3}{(s^2 + p_1^2)(s^2 + p_2^2)(s^2 + p_3^2)(s^2 + p_4^2)} \qquad (3\text{-}20)$$

and a modified ladder is obtained as in Fig.3-9. This is now a four node network, and using any of the design equations (3-17c,d) or (3-18c,d), a canonical realisation can be implemented. Fig.3-10 shows the canonical realisation circuit structure of Eq(3-17c,d). Compared to the non-canonical realisation in Fig.3-8, two transconductors can be removed.

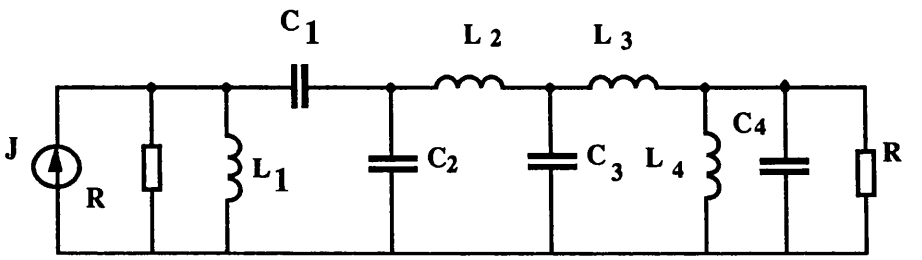

Fig.3-9 Modified 8th-order Butterworth bandpass ladder prototype

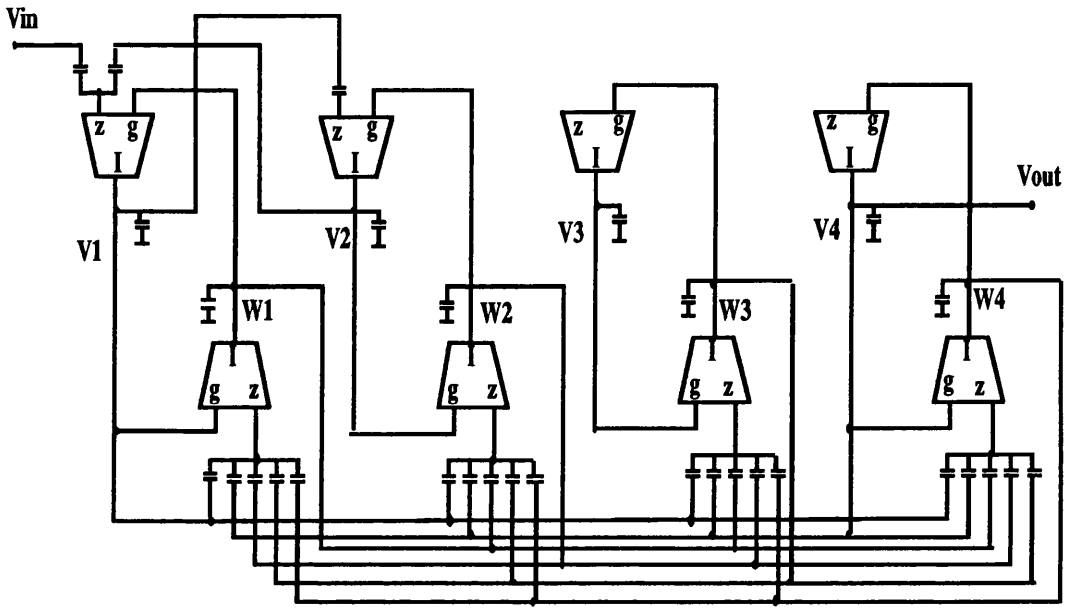

Fig.3-10 Transconductor-C filter based on modified prototype

3.3.4 Mixed Variable Representation Approach for Canonical Ladder Based Transconductor-Capacitor Filter Design

In the Transfer Function Modification Approach, we focus on finding a canonical ladder prototype, and then use a matrix design method to obtain a canonical transconductor-capacitor filter. Because the limitation of equal transconductance in transconductor-capacitor filter design, a large number of designs cannot be realised in canonical form. To overcome the difficulty, a new canonical design approach called Mixed Variable Representation Approach is introduced. Instead of finding a canonical ladder prototype, we try to find a best variable representation in order to get a canonical transconductor-capacitor design from a non-canonical ladder prototype. If nodal voltages alone are selected as primary variables to describe a non-canonic ladder prototype, it is found that the number of these and hence the order of the matrix is larger than the number of poles. This will lead to an excessive number of transconductors in an active simulation. It is also noticed that extra nodes are usually introduced by series LC or LR branches. In the Mixed Variable Representation

Approach both current and voltage variables are selected in the formulation of the vector **V** when a non-canonical prototype ladder is encountered. A compact matrix is thus formed, which is then entered into the standard matrix design method to achieve a cannonical transconductor-C implementation. The topology of the initial ladder prototype dictates the selection of the variables and the efficiency of the approach. Consider the initial prototype in Fig.3-7, a direct realisation from nodal voltage representation requires 10 transconductors. **V** is constructed from two nodal voltages (V_1, V_3) and the currents through the two LC series branches (I_2, I_4). We use voltage (V_{I2} and V_{I4}) proportional to the currents and the terminating resistance, in order to preserve dimensional consistency. It is not necessary to simulate the output voltage (V_5) of the passive ladder explicitly, because all of I_4 passes through the termination resistor and V_{I4} can therefore be treated as the output voltage. For the mixed voltage-and-current representation of the eighth order Butterworth bandpass ladder the matrices are:

$$J=\begin{pmatrix}\frac{V_{in}}{R}\\0\\0\\0\end{pmatrix},V=\begin{pmatrix}V_1\\V_{I2}\\V_3\\V_{I4}\end{pmatrix},G=\frac{1}{R}\begin{pmatrix}1&1&0&0\\1&0&-1&0\\0&1&0&-1\\0&0&-1&1\end{pmatrix}, \qquad (3\text{-}21,a,b,c)$$

$$C=\begin{pmatrix}C_1&0&0&0\\0&\frac{-L_2}{R^2}&0&0\\0&0&C_3&0\\0&0&0&\frac{-L_4}{R^2}\end{pmatrix},\Gamma=\begin{pmatrix}\frac{1}{L_1}&0&0&0\\0&\frac{-1}{R^2C_2}&0&0\\0&0&\frac{1}{L_3}&0\\0&0&0&\frac{-1}{R^2C_4}\end{pmatrix} \qquad (3\text{-}21,d,e)$$

Substituting (3-21a,b,c,d,e) into the left-decomposition equations (3-14a,b) gives the transconductor-capacitor ladder shown in Fig.3-11. Again a circuit realisation with eight transconductors is obtained. A SPICE simulation of the fully differential version is shown in Fig.3-12.

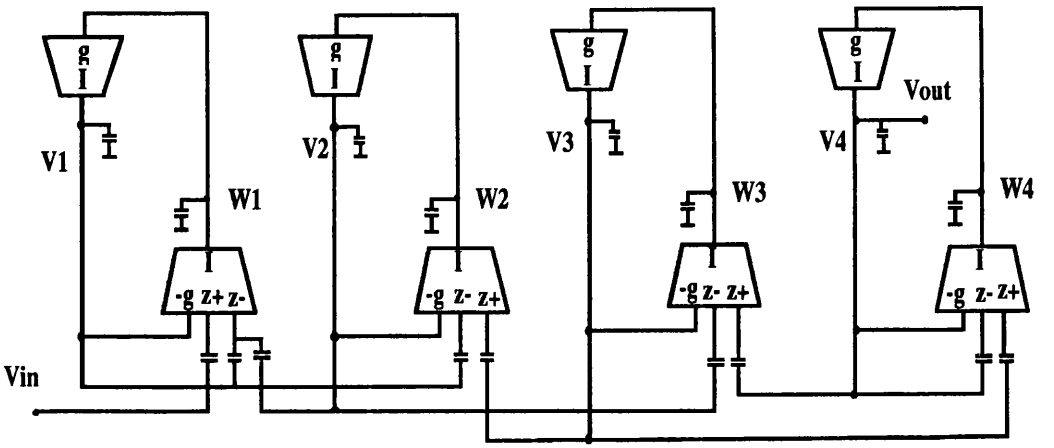

Fig.3-11 Transconductor-C filter designed by mixed variable representation approach

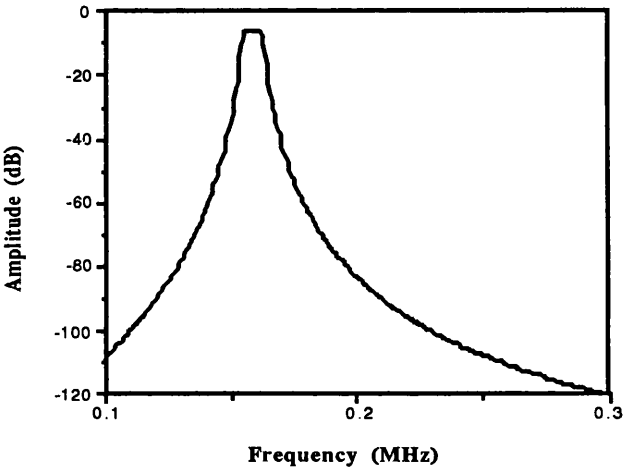

Fig.3-12 SPICE simulation of 8th-order Butterworth transconductor-C ladder filter

3.4 LADDER TRANSCONDUCTOR-CAPACITOR EQUALISER DESIGN

Recently, continuous-time filters for applications in video signal processing have received considerable attention[22,23]. Continuous-time filters and equalisers based on operational transconductance amplifiers and capacitors can replace SC circuits when low noise and/or high frequency operation is necessary. Usually group delay equalisation is provided in analogue filters by one or more allpass biquadratic stages. However where the equaliser required is of order greater than two it would be

preferable to use a ladder derived circuit, for the usual sensitivity considerations. A method for allpass transconductor-C ladder based design, directly analogous to techniques recently proposed for digital[25] and SC[26] filters, can be developed.

Consider allpass transfer functions of the form

$$H(s) = k\frac{P(-s)}{P(s)} \tag{3-22}$$

where P(s) is Hurwitz polynominal of order n and k = 1 if n is odd order and k = -1 if n is even. The polynomial P(s) is separated into odd and even parts:

$$P(s) = E(s) + O(s) \tag{3-23}$$

Define

$$Y(s) = \begin{cases} \dfrac{E(s)}{O(s)} & \text{if n is even} \\ \dfrac{O(s)}{E(s)} & \text{if n is odd} \end{cases} \tag{3-24}$$

Substituting (3-23) and (3-24) into (3-22) gives

$$H(s) = \frac{1 - Y(s)}{1 + Y(s)} = 1 - \frac{2}{1 + Y(s)} \tag{3-25}$$

Since P(s) is Hurwitz, Y(s) can be expanded as a continued fraction, and equation (3-25) can then be realised as the combination of a singly terminated RLC ladder and an active summing stage as shown in Fig.3-13. The singly terminated passive ladder network part can be simulated by a transconductor-C circuit using the above matrix decomposition method and the overall transconductor-C group delay equaliser structure is shown in Fig.3-14.

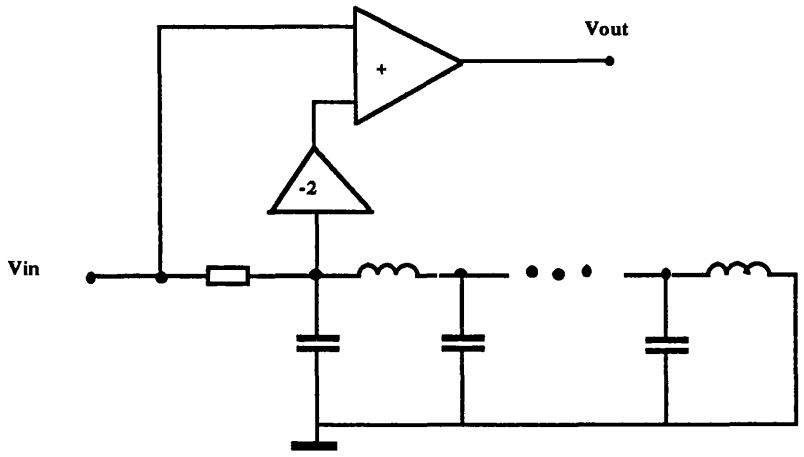

Fig.3-13 Prototype of an Allpass Ladder Filter

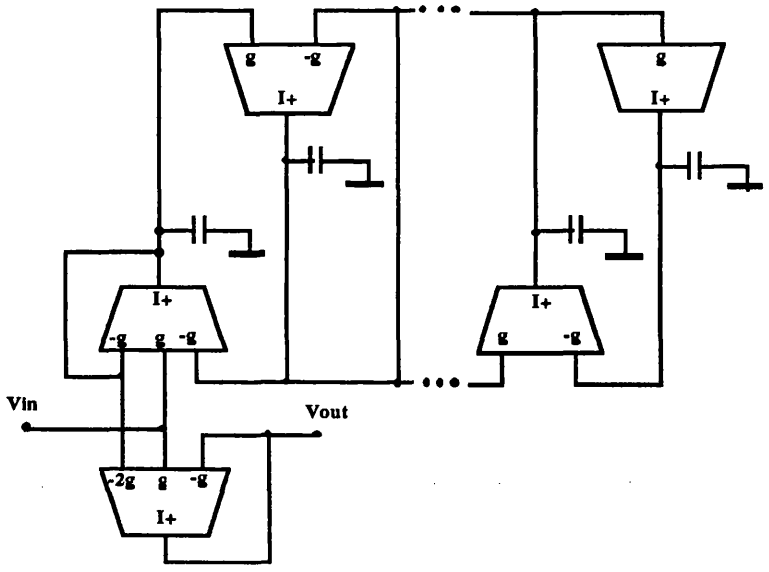

Fig.3-14 Allpass Transconductor-Capacitor Ladder Filter

3.5. A VIDEO FREQUENCY TRANSCONDUCTOR-CAPACITOR FILTER AND EQUALISER DESIGN EXAMPLE

For a lowpass video filter with specifications of passband edge frequency 1MHz, stopband edge frequency 1.887MHz, passband ripple 0.28dB and stopband attenuation 50.5dB, a 5th-order elliptic ladder prototype will satisfy the requirements.

Using the above matrix decomposition method, a fully differential transconductor-C circuit realisation is given in Fig.3-15, where all transconductors have the same value, and the solid line in Fig.3-16 shows the frequency response simulated by SPICE. The transconductance spread is 1 and the capacitance spread is 23.54. If a cascade of biquadratic stages is used, it is not possible to have equal valued transconductances, but the alternative equal valued capacitance realisation demands a transconductance spread of 7.3×10^6! Fig.3-17 shows the sensitivity comparison between a ladder based realisation and a cascade biquad configuration, and the obvious advantage of ladder based structure is clearly apparent.

The filter group delay variation within the passband is 1.1μs, whereas the original specifications require a maximum variation of 0.4μs. An initial 12th-order equaliser design, which reduces the group delay variation to 0.13 μs with an equal ripple behaviour, was considered. However with the help of XFILT compiler, the maximum group delay variation can still be satisfied by utilising a 6th-order equaliser, though the equal ripple behaviour no longer applies. A fully differential realisation of the 6th-order equaliser is given in Fig.3-18. The comparative sensitivity analysis for the ladder based equaliser and a typical cascaded biquad equaliser is shown in Fig.3-19; the ladder based structure is again significantly better. The filter and equaliser were fabricated on a 1 micron CMOS process, having double polysilicon and double metal and using a 5V power supply. Fig.3-16 shows the overall amplitude response of the filter and equaliser, the measured results are typical ones from the range obtained . It will be noted from the circuit response, that there is a loss of attenuation in the stopband including the dissappearance of the second notch, though the level of stopband attenuation remains within specification. This retention of performance is due to deliberately allowing an initial filter approximation with a very generous stopband attenuation to absorb process variations and inaccuracies, and deterioration due to noise, though the noise level in the passband is tyically -128dBm/$\sqrt{\text{Hz}}$. The passband response of the fabricated circuit shows some variation in ripple level and

corner frequency. Detailed investigation of the equaliser amplitude response shows an arbtirary rippling behaviour over the passband of up to 1.1dB, whereas the computed amplitude response of the all-pass equaliser shows a completely flat characteristic over a wide frequency range. These variations in equaliser response can be directly attributed to the accuracy problems in realising the very wide spread in capacitance 2120:1 (transconductance spread is 1). It was also noted that the dynamic range of the equaliser was considerably less than the filter. It is now possible to utilise various signal scaling techniques at different stages of transconductance-C ladder based designs and it would be sensible to invoke these in any re-design. The group delay responses, Fig.3-20, show very effective equalisation within the passband, the measured group delay variation of the filter is 1.02μs and the measured combined group delay variation of all system (filter and equaliser) is 0.38μs, which satisfies the initial specification.

Use of XFILT has enabled further improvements to the equaliser. Simply increasing the number of iterations in the group delay approximation stage improves the equal ripple nature of the response at no extra cost in circuit terms as shown in Fig.3-21. A more significant improvement in silicon area can be achieved by utilising the arbitrary amplitude approximation facility for the filter. The use of a 4th order touch point near the band edge reduces the group delay variation of the filter to 0.72μs and thus lowers the equalisation requirements considerably. Fig.3-22(a) gives the passband response of the modified filter and there is a cost of about 4dB loss of attenuation in the stopband of the filter as shown in Fig.3-22(b). Fig.3-23 presents the comparison of modified filter group delay and original filter group delay. A 4th-order equaliser can now be used. The silicon area can be reduced about one third. The improvement is even significant when a high order equaliser is modified. In this cases, the silicon area saving can reach a half.

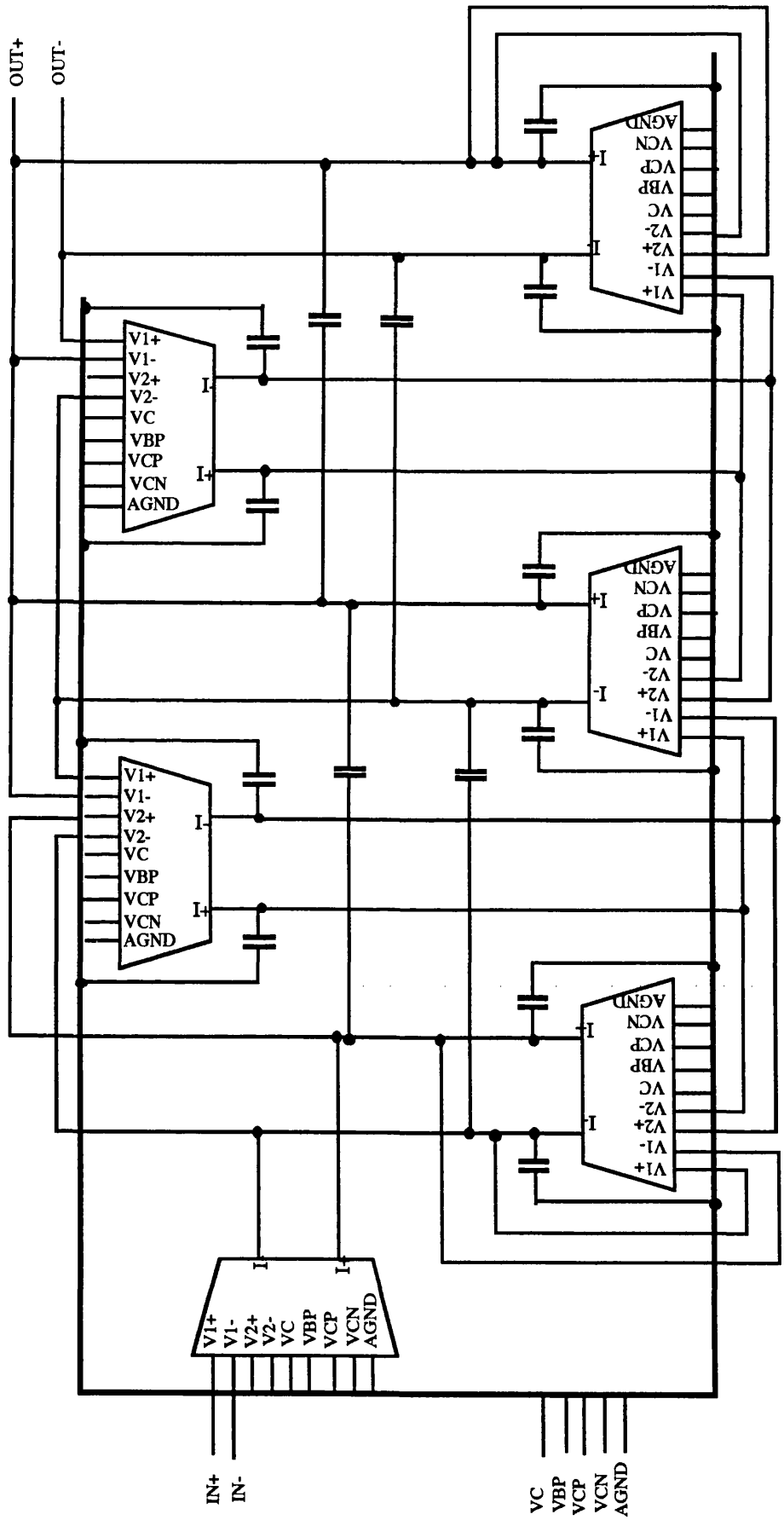

Fig.3-15 Fully differential 5th-order Elliptic Filter

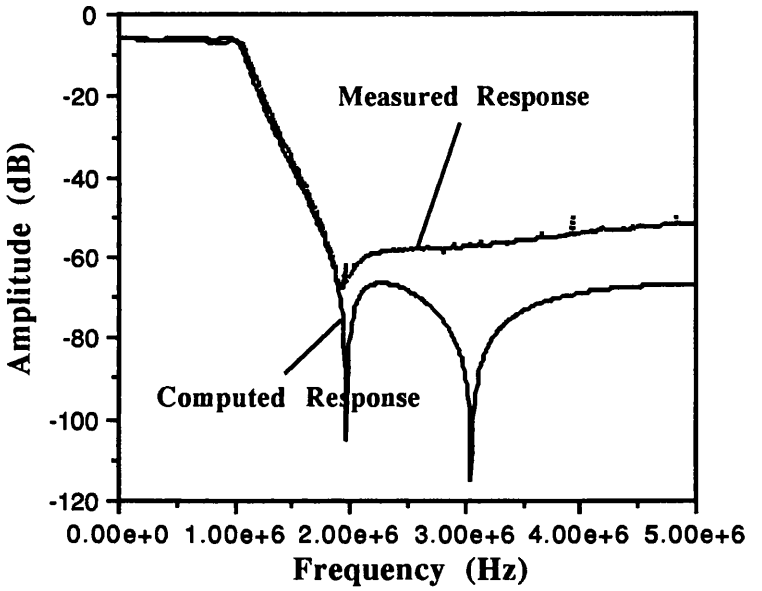

Fig.3-16 Measured and SPICE simulation of transconductor-C video filter response

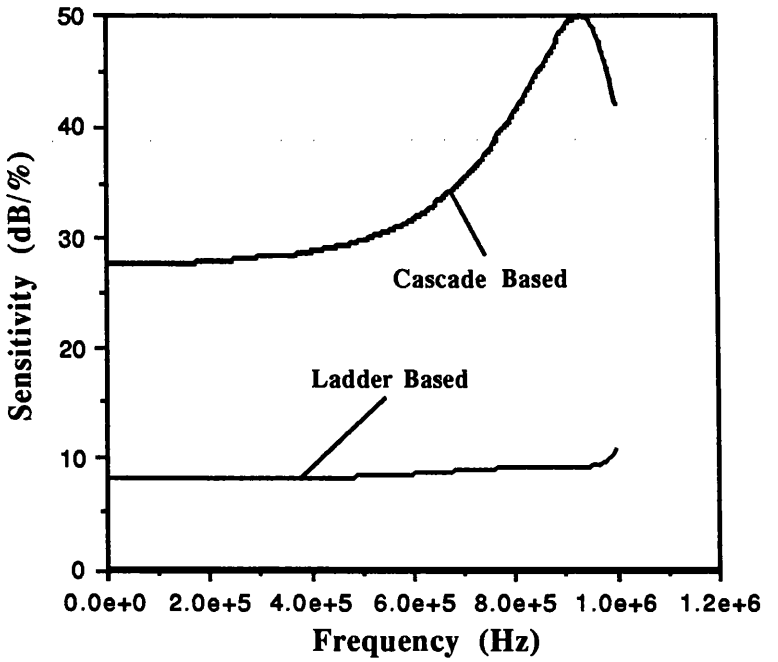

Fig.3-17 Passband sensitivity of video filters

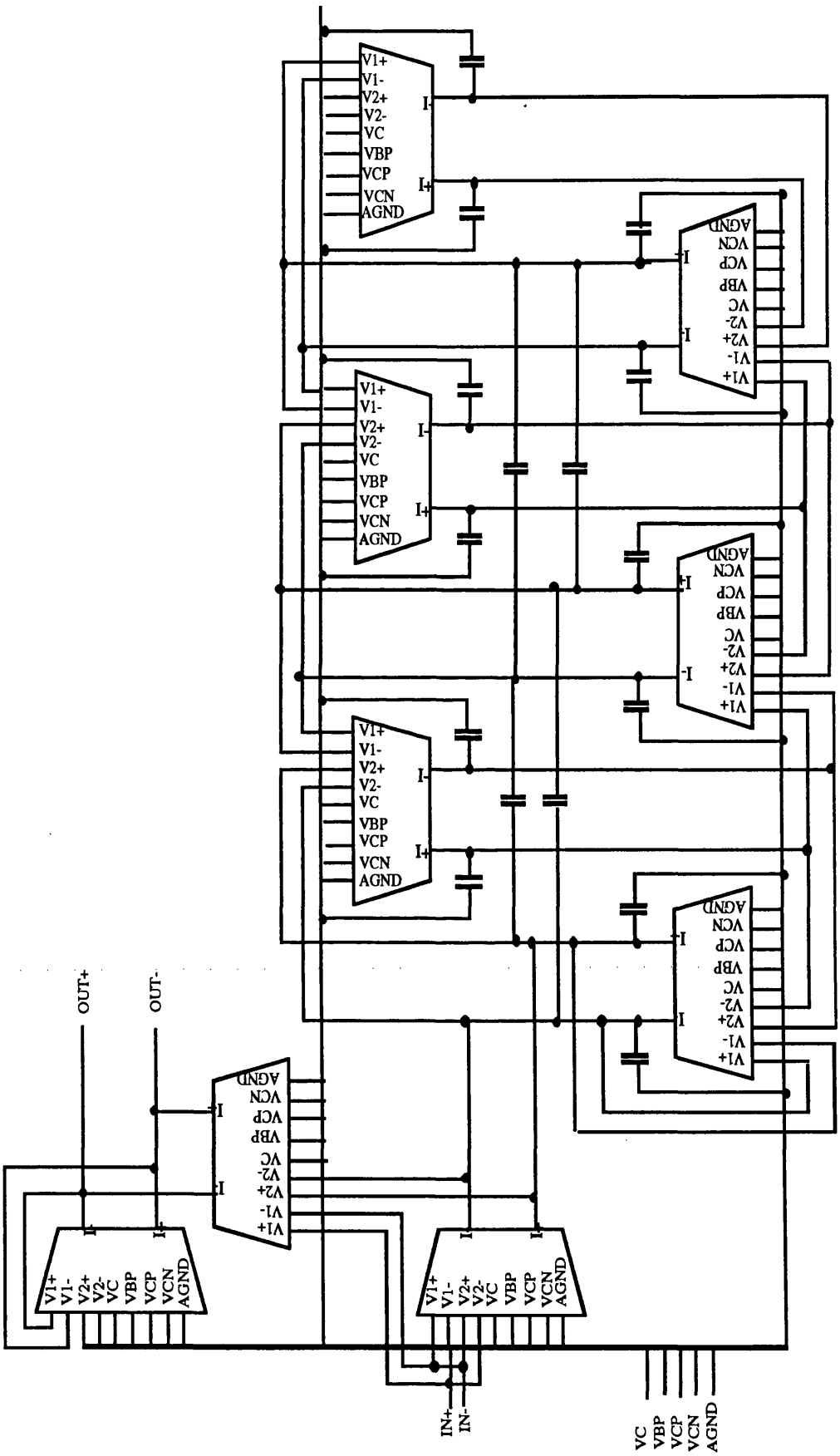

Fig.3-18 Fully differential ladder based transconductor-C equaliser

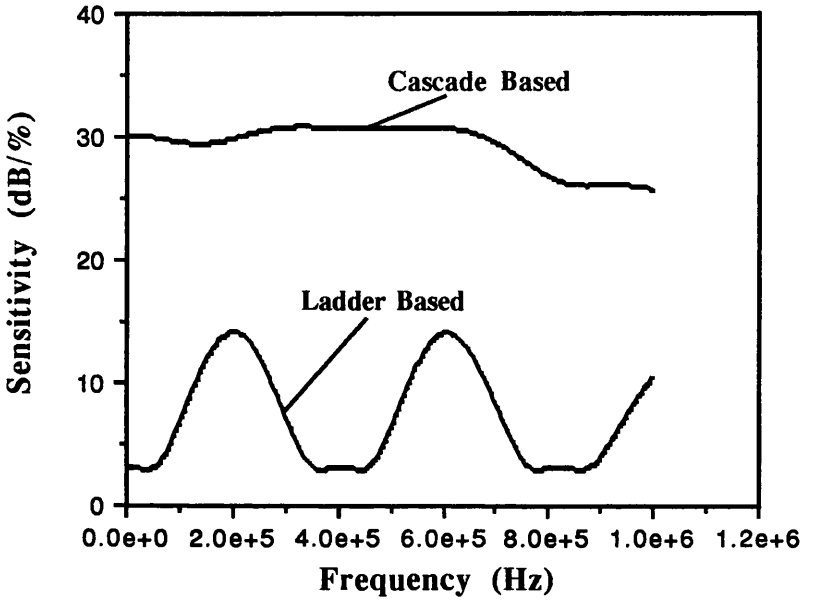

Fig.3-19 Video equaliser sensitivity comparison

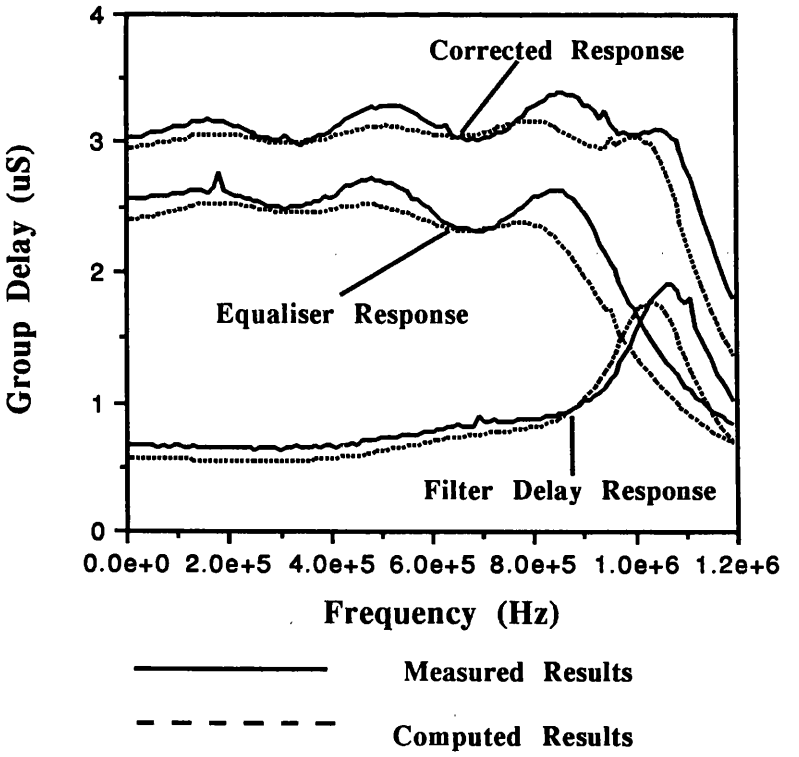

Fig.3-20 6th-order video equaliser group delay response

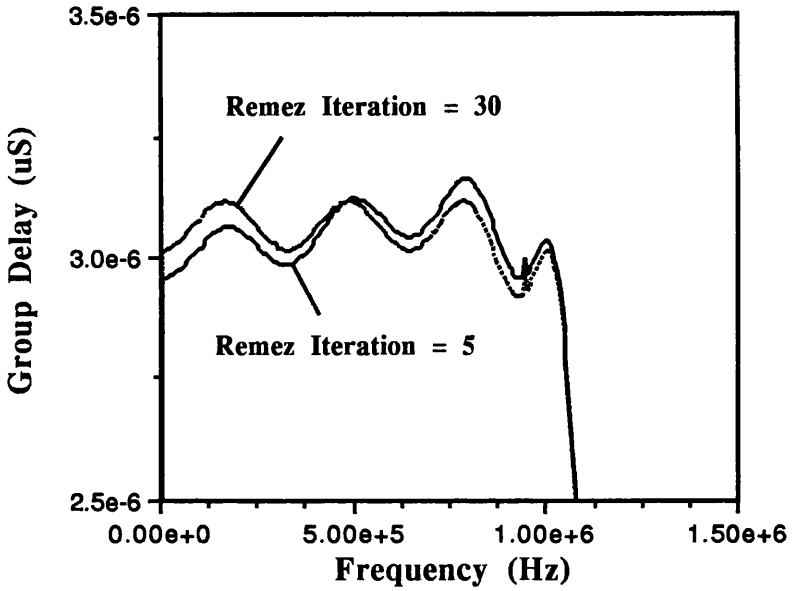

Fig.3-21 Group delay response with different numbers of Remez iterations

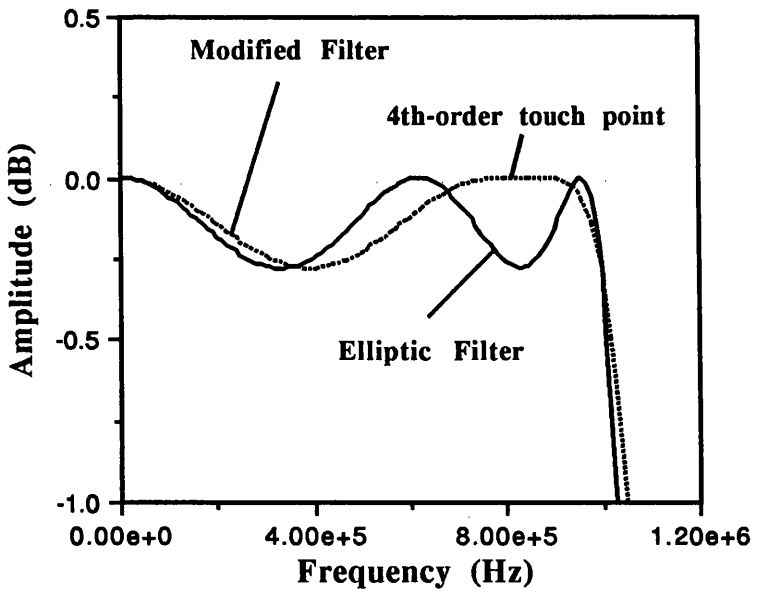

Fig.3-22(a) Comparison of video filter passband response

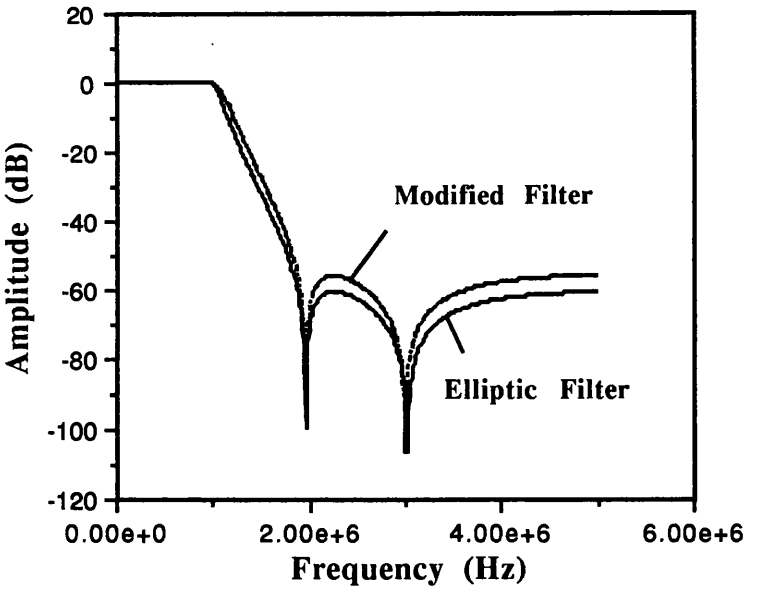

Fig.3-22(b) Comparison of video filter response

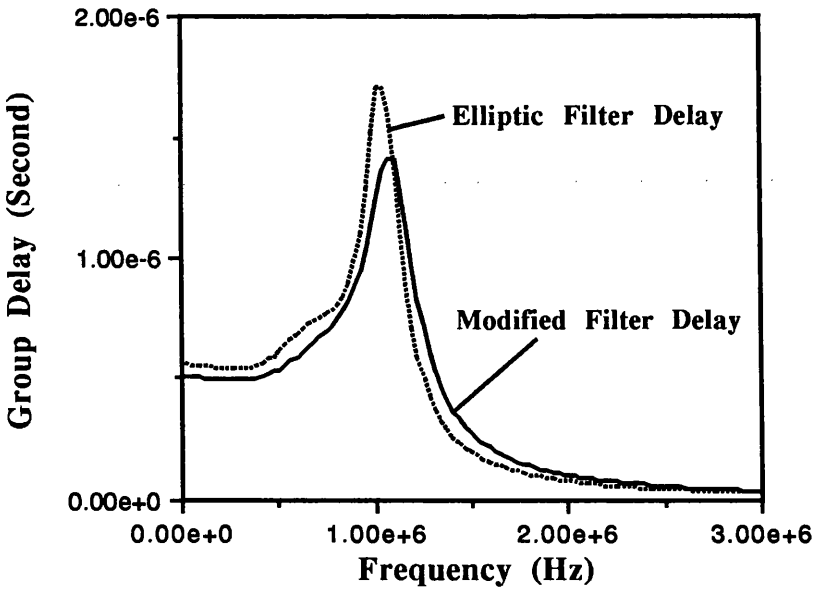

Fig.3-23 4th order equaliser group delay response

3.6.SUMMARY

In this chapter, the approach for cascade transconductor-C filter design has been presented. The matrix based ladder transconductor-C filter design approach was reviewed. The definition of ladder based canonical transconductor-capacitor filter was introduced, and two canonical ladder based transconductor-capacitor filter design approaches were proposed. In the Transfer Function Modification Approach, a transfer function which is unrealisable by canonical ladder is modified to a transfer function which is realisable by canonical ladder, and when the ladder is simulated by a transconductor-C circuit the original transfer function is then restored by a change in input circuitry. This approach can also be used when prototype ladder is not realisable, such as in even-order Elliptic case. The Mixed Variable Representation Approach is applied by properly choosing voltage and current variables to form vector **V** and to ensure a compact matrix form. Low sensitivity property of the circuit can be maintained because no modification has been made to circuit structure. This approach can be used in the case where ladder is already available or Transfer Function Modification Approach cannot be employed. The application of the two approaches is demonstrated in an 8th-order Butterworth bandpass filter design.

The ladder based transconductor-C equaliser design method was also discussed. A practical video frequency transconductor-C filter and equaliser design is given to demonstrate the utility of the matrix design method and the transconductor-C filter and equaliser design software. Both simulated and measured results are presented. Comparison of sensitivity for ladder based and cascade based structure was also carried out. Strategies for system level optimisation were also proposed.

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Chapter 4: Switched Current Filter Design

CHAPTER 4: SWITCHED CURRENT FILTER DESIGN

4.1 .INTRODUCTION

The switched-current (SI) techniques proposed by Hughes et al[1,2] to perform sampled-data analogue signal-processing are currently receiving considerable attention. In contrast to the switched-capacitor (SC) approach, which requires a additional processing steps to a digital CMOS process to realise floating linear capacitors, the SI technique can perform accurate signal processing functions in a standard digital CMOS process without the direct use of any capacitor. This becomes an increasingly attractive feature for integration of large analogue/digital systems in a single chip. Moreover, the SI technique does not utilise CMOS op-amps but rather performs all its analogue signal processing with much simpler current mirrors. It is therefore expected that SI circuits will operate over much wider signal bandwidths than present day SC circuits. Also, the current mode nature of SI circuits should make them less adversely affected by the imminent reduction in power supply voltages. However, based on present technologies it appears that in most important categories of performance, such as SNR (Signal Noise Ratio), speed and low power consumption, the SC circuits still have an edge over the SI ones[3]. If SI techniques are to gain wide acceptance, new techniques and circuits which are less dependent upon the accuracy of the analogue component and manufacturing variations need to be developed. It is also very important to have a suite of CAD tools to automate and simplify the design process[4]. In this chapter, the CAD algorithms and software development required for SI filters and equalisers are addressed.

4.2. CASCADE SWITCHED-CURRENT FILTER DESIGN

In recent years much research has been directed towards the development of switched-current filters. A biquad cascade method was first used in the implementation of SI filters[5], both integrator based and differentiator based biquadratic sections have been proposed[6]. As in active-RC, and SC cascade cases, a high order filter transfer function is first presented as a product of a number of biquadratic functions and a first order function if the transfer function is of odd order. The first order transfer function is of the form

$$H(z) = -\frac{d_0 + d_1 z^{-1}}{1 + c_1 z^{-1}} \tag{4-1}$$

The first order SI topology for the implementation of Eq.(4-1) is shown in Fig.4-1. This structure can implement either a low-pass or a high-pass function needed for odd order filters. The transfer function of the section is

$$H(z) = -\frac{\alpha_2 - \alpha_1 z^{-1}}{(1 + \alpha_3) - z^{-1}} \tag{4-2}$$

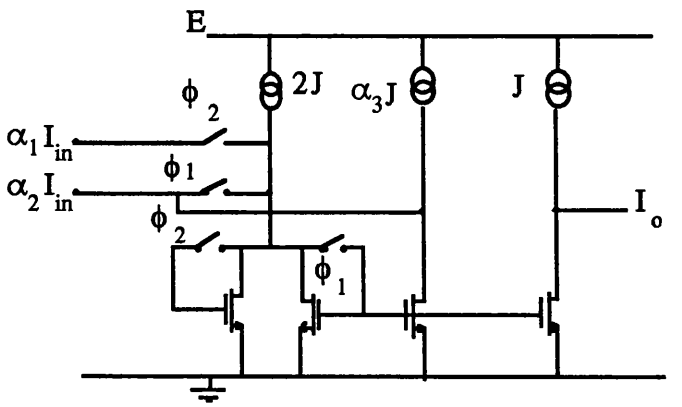


Fig.4-1 First-order SI section

Clearly, the pole is inside the unit circle and has a positive value. Zeros, both inside and outside the unit circle on the positive real axis can be realised. Negative zeros can also be obtained by inverting the input current direction associated with α_1. By comparing the coefficients of Eq.(4-1) and (4-2), the circuit parameters can be calculated by

$$\alpha_3 = -\frac{1}{c_1} - 1 \tag{4-3a}$$

$$\alpha_1 = -(1+\alpha_3)d_1 \tag{4-3b}$$

$$\alpha_2 = (1+\alpha_3)d_0 \tag{4-3c}$$

The transfer function of a biquadratic filter section is of the form

$$H(z) = -\frac{d_0 + d_1 z^{-1} + d_2 z^{-2}}{1 + c_1 z^{-1} + c_2 z^{-2}} \tag{4-4}$$

The integrator based biquadratic section which implements the Eq.(4-4) is shown in Fig.4-2 with transfer function

$$H(z) = -\frac{(\alpha_5 + \alpha_6) + (\alpha_1\alpha_3 - \alpha_5 - 2\alpha_6)z^{-1} + \alpha_6 z^{-2}}{(1+\alpha_4) + (\alpha_2\alpha_3 - 2 - \alpha_4)z^{-1} + z^{-2}} \tag{4-5}$$

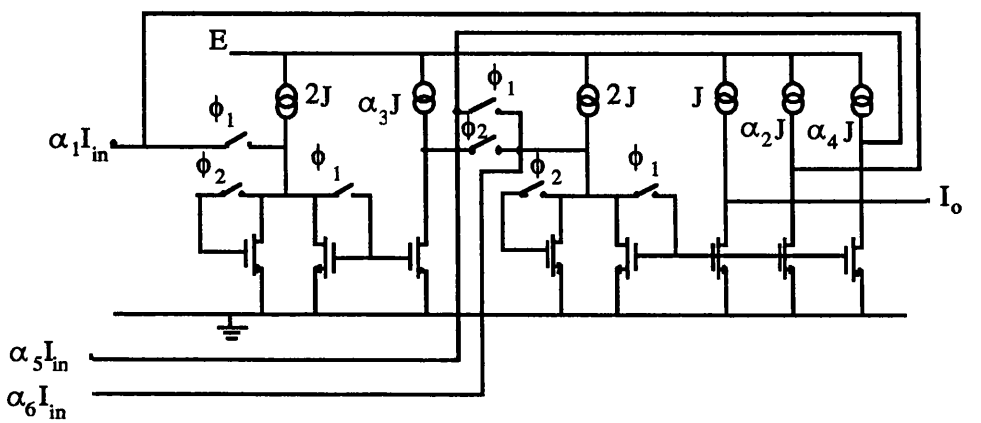


Fig.4-2 Integrator based biquadratic section

Comparing Eq.(4-5) with (4-4), a set of equations can be obtained for the calculation of the circuit parameters

$$\alpha_1\alpha_3 = \frac{d_0 + d_1 + d_2}{c_2} \tag{4-6a}$$

$$\alpha_2\alpha_3 = \frac{1 + c_1 + c_2}{c_2} \tag{4-6b}$$

$$\alpha_4 = \frac{1}{c_2} - 1 \tag{4-6c}$$

$$\alpha_5 = \frac{d_0 - d_2}{c_2} \tag{4-6d}$$

$$\alpha_6 = \frac{d_2}{c_2} \tag{4-6e}$$

The differentiator based biquadratic section is shown in Fig.4-3 with transfer function

$$H(z) = -\frac{\frac{\alpha_1\alpha_3 + \alpha_2\alpha_3}{\alpha_3\alpha_5} + \frac{(\alpha_0 - \alpha_1\alpha_3 - 2\alpha_2\alpha_3)}{\alpha_3\alpha_5}z^{-1} + \frac{\alpha_2}{\alpha_5}z^{-2}}{1 + \frac{(1 + \alpha_4 - 2\alpha_3\alpha_5)}{\alpha_3\alpha_5}z^{-1} + \frac{(\alpha_3\alpha_5 - \alpha_4)}{\alpha_3\alpha_5}z^{-2}} \tag{4-7}$$

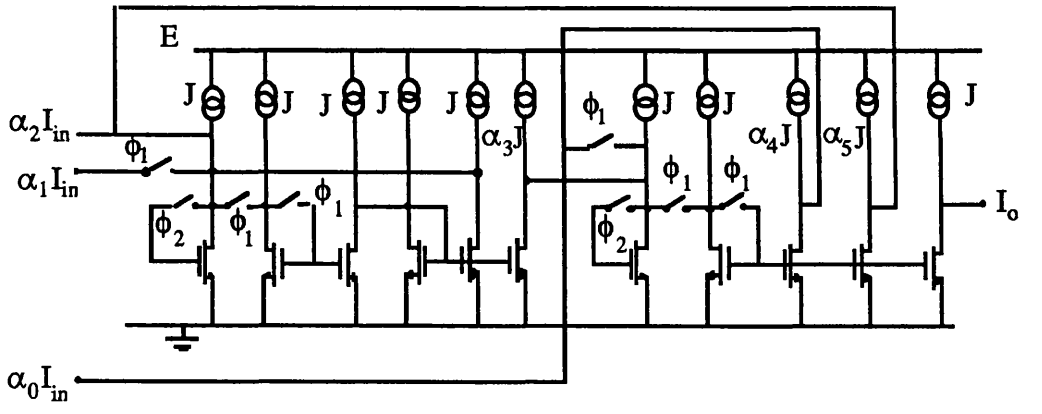


Fig.4-3 Differentiator base biquadratic section

After comparing the coefficients of Eq.(4-4) and (4-7), and properly arranging, the following equations can be obtained for the calculation of parameters in differentiator based biquadratic section.

$$\alpha_0 = \frac{d_0 + d_1 + d_2}{1 + c_1 + c_2} \tag{4-8a}$$

$$\alpha_1 = d_0 - d_2 \tag{4-8b}$$

$$\alpha_2 = d_2 \tag{4-8c}$$

$$\alpha_3 = \frac{1}{1 + c_1 + c_2} \tag{4-8d}$$

$$\alpha_4 = \frac{1 - c_2}{1 + c_1 + c_2} \tag{4-8e}$$

$$\alpha_5 = 1 \tag{4-8f}$$

By cascading single and biquadratic filter sections it is possible to realise a wide range of high order SI filters. However, in practice, the sensitivity of such cascade structures to component variations can become unacceptably high, especially in high order or high Q filters. This has lead to further research on ladder structure SI filters.

4.3 .FIRST AND SECOND GENERATION INTEGRATOR BASED SWITCHED CURRENT LADDER FILTER DESIGN APPROACH

The low sensitivity performance of ladder based filters has resulted in their wide acceptance in SC circuits. Because of a generic similarity, a well known approach is to transpose the signal flowgraph of an existing SC filter to accommodate SI implementation. Here the signal flowgraph of a SC filter containing multiple-input single-output integrators is transposed to give a SI filter containing single-input multiple-output integrators[7]. Other researchers have proposed different SI ladder

prototype, construct a flowgraph, and then replace the integrator branches with switched-current LDI, bilinear, forward or backward Euler integrators to obtain a SI filter[8-12].

The matrix decomposition method has been successfully used in SC and transconductor-C ladder filter design as described earlier. In this section, we present a systematic approach for ladder SI filter design based on the matrix decomposition method. The approach can produce eight different structures for one prototype ladder, all maintaining the low sensitivity property, but producing a range of different maximum ratios of transistor aspect ratios and different sums of ratios of transistor aspect ratios. The designer can choose the smallest maximum ratio of transistor aspect ratios to maintain the accuracy and minimum sums of transistor aspect ratios to save area. The general leapfrog SI design method used by many filter designers is a special case of the general structure. The approach is an exact simulation of prototype ladder and without any approximation being involved compared to those in [7][8]. The bilinear transformation is adopted but no actual bilinear integrators are used, this leads to a much simpler circuit structure than those based on bilinear integrators[9][10]. The approach is completely general and suited for any filter type (lowpass, bandpass, bandstop, highpass and allpass), furthermore no special techniques are needed to deal with different types of filter[11][12]. Moreover, the approach is well suitable for computer aided implementation and has been included in the XFILT filter design system.

Again start with the matrix equation for a passive ladder

$$(\mathbf{sC}+s^{-1}\mathbf{\Gamma}+\mathbf{G})\mathbf{V}=\mathbf{J} \tag{4-9}$$

Consider a lowpass 5th-order ladder with finite transmission zeros as in Fig.4-4.

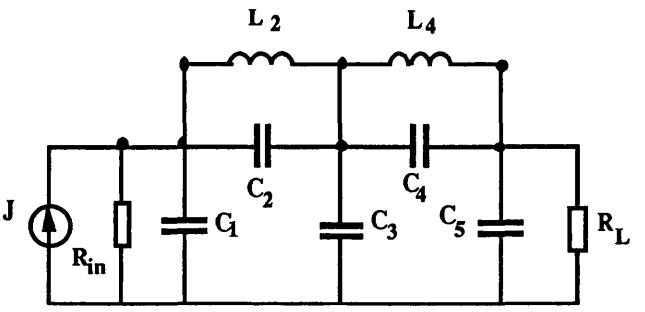


Fig.4-4 Lowpass 5th Order Ladder With Finite Transmission Zeros

The C, Γ, and G are

$$\mathbf{C}=\begin{bmatrix} C_1+C_2 & C_2 & 0 \\ C_2 & C_2+C_3+C_4 & C_4 \\ 0 & C_4 & C_4+C_5 \end{bmatrix}$$

$$\Gamma=\begin{bmatrix} L_2^{-1} & L_2^{-1} & 0 \\ L_2^{-1} & L_2^{-1}+L_4^{-1} & L_4^{-1} \\ 0 & L_4^{-1} & L_4^{-1} \end{bmatrix} \qquad \mathbf{G}=\begin{bmatrix} R_{in}^{-1} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R_L^{-1} \end{bmatrix}$$

Since the operational blocks in SI circuits process currents, all prototype variables must be transformed to current variables using a scaling resistor (chosen to be 1Ω for convenience). The equation (4-9) then can be represented as

$$(\mathbf{sC}+\mathbf{s}^{-1}\Gamma+\mathbf{G})\mathbf{I}=\mathbf{J} \tag{4-10}$$

After bilinear transformation

$$s \rightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{4-11}$$

equation (4-11) becomes

$$\left[\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}C+\frac{T}{2}\frac{1+z^{-1}}{1-z^{-1}}\Gamma+G\right]I=J \tag{4-12}$$

By multiplying the system through by $(1+z^{-1})/(1-z^{-1})$ and after special manipulation, it gives

$$\left[\frac{1}{\phi}A+\psi B+D\right]I=(1+z^{-1})J \tag{4-13}$$

In equation (4-13)

$$\psi=\frac{z^{-1}}{1-z^{-1}} \tag{4-13a}$$

$$\phi=\frac{1}{1-z^{-1}} \tag{4-13b}$$

$$A=\frac{2}{T}C+\frac{T}{2}\Gamma-G \tag{4-13c}$$

$$B=2T\Gamma \tag{4-13d}$$

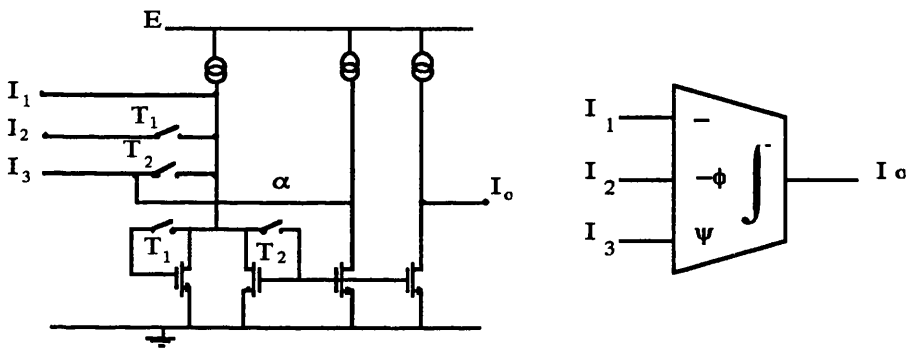
$$D=2G \tag{4-13e}$$

The operations ψ and ϕ can now be realised by SI building blocks. However equation (4-13) is still a second order equation. To implement SI filter, the equation

(4-13) needs to be decomposed into two first order equations by the introduction of a vector of intermediate variables. A typical second-generation SI memory cell based first order SI building block as shown in Fig.4-5 is used in the implementation of each first order equation. It has a transfer function:

$$I_o = -\frac{\beta(1-z^{-1})}{1-\beta z^{-1}} I_1 - \frac{\beta}{1-z^{-1}} I_2 + \frac{\beta z^{-1}}{1-z^{-1}} I_3 \qquad (4\text{-}14)$$

where $\beta = 1/(1+\alpha)$.



(a)Typical circuit (b) Block symbol

Fig.4-5 SI Filter First Order Building Block

In practice, any enhanced type memory cell can be employed to form a first order building block, such as cascode memory cell[13], regulated cascode memory cell[14], folded cascode memory cell[6], active memory cell[15], common gate memory cell[16,17], or class AB memory cell[18].

4.3.1.Left Matrix Decomposition

Either the **A** or the **B** matrix can be factorised, leading to left and right decomposition respectively.

Factorise the matrix **A** into

$$\mathbf{A} = \mathbf{A}_l\mathbf{A}_r \tag{4-15}$$

The equation.(4-13) can be expressed as

$$\mathbf{A}_l\mathbf{X} = -(\psi\mathbf{B}+\mathbf{D})\mathbf{I}+(1+z^{-1})\mathbf{J} \tag{4-16a}$$

$$\mathbf{A}_r\mathbf{I} = \phi\mathbf{X} \tag{4-16b}$$

For the convenience of circuit realisation, let **W**=-**X**, and equation (4-16) becomes

$$\mathbf{A}_l\mathbf{W} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \tag{4-17a}$$

$$\mathbf{A}_r\mathbf{I} = -\phi\mathbf{W} \tag{4-17b}$$

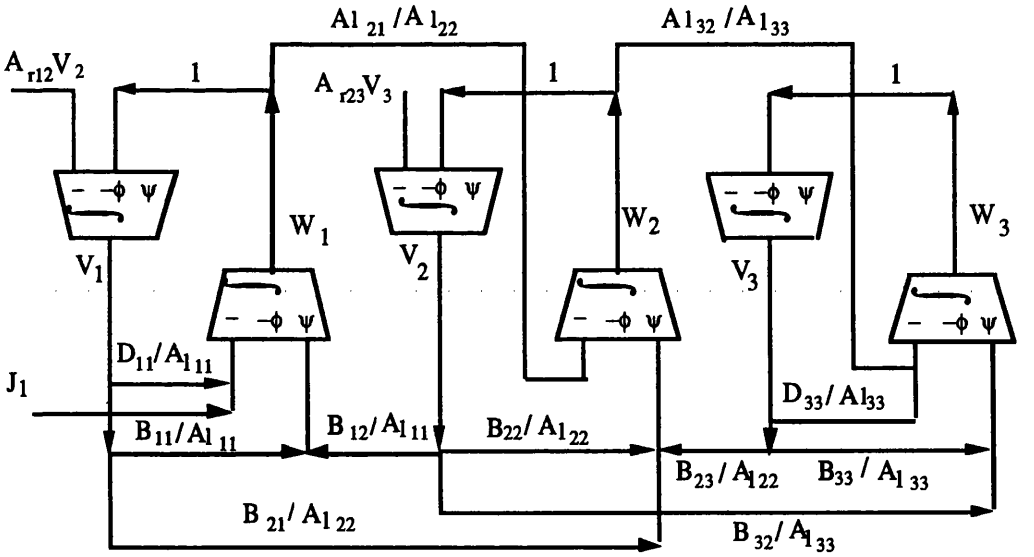


Fig.4-6 6th-order Left Decomposition SI Structure

where W is the vector of intermediate variables. Using the building block in Fig.4-5, equations (4-17) can be realised by SI circuits. The one-to-one correspondence

between the circuit elements and the matrix entries indicates that the efficiency of the SI implementation in terms of numbers of integrator outputs is related to the sparsity of the system matrices. To maintain the sparsity of the matrices, the well known LU, UL, or the direct methods which decompose matrix A into $\mathbf{AI_u}$ or $\mathbf{I_uA}$ (Here $\mathbf{I_u}$ is the identity matrix) can be used. A standard representation of the circuit produced by left decomposition of a 6th-order matrix system is shown in Fig.4-6.

The four left decomposition methods are as follows.

Left-LU Decomposition

Let **A=LU** where L stands for the lower triangular and U for the upper triangular matrix, the Eq.(4-17) becomes

$$\mathbf{LW} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \tag{4-18a}$$

$$\mathbf{UI} = -\phi\mathbf{W} \tag{4-18b}$$

Left-UL Decomposition

If **A** is decomposed as **A=UL**, the system design equations are

$$\mathbf{UW} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \tag{4-19a}$$

$$\mathbf{LI} = -\phi\mathbf{W} \tag{4-19b}$$

Left-IA Decomposition

For the case $\mathbf{A=I_uA}$, the design equations are

$$\mathbf{W} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \quad (4\text{-}20a)$$

$$\mathbf{AI} = -\phi\mathbf{W} \quad (4\text{-}20b)$$

Left-AI Decomposition

If $\mathbf{A}=\mathbf{AI}_u$, the following equations are obtained

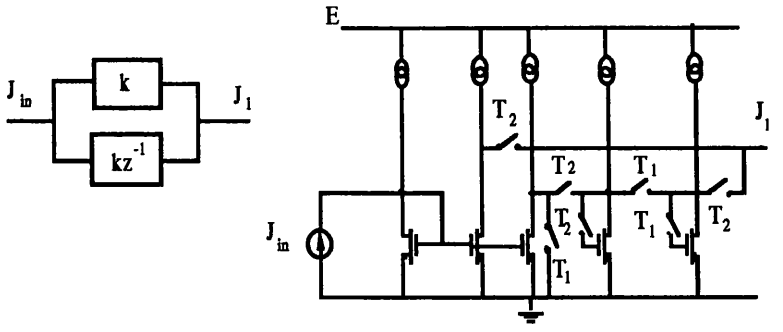
$$\mathbf{AW} = (\psi\mathbf{B}+\mathbf{D})\mathbf{I}-(1+z^{-1})\mathbf{J} \quad (4\text{-}21a)$$

$$\mathbf{I} = -\phi\mathbf{W} \quad (4\text{-}21b)$$

After matrix scaling, the input current J_1 in Fig.4-6 can be represented as

$$J_1=k(1+z^{-1})J_{in} \quad (4\text{-}22)$$

where J_{in} is the prototype ladder input current and k is a constant. The symbol for the realisation of J_1 is shown in Fig.4-7(a) and the proposed circuit realisation shown in Fig.4-7(b).



(a) (b)

Fig.4-7 Left Decomposition Input Terminal SI Realisation

4.3.2.Right Matrix Decomposition

Matrix **B** can also be factorised as

$$\mathbf{B} = \mathbf{B}_l\mathbf{B}_r \tag{4-23}$$

which leads to a group of right hand matrix decomposition methods. The following pair of equations is equivalent to (4-13).

$$\mathbf{AI} = -\phi(\mathbf{B}_l\mathbf{W}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \tag{4-24a}$$

$$\mathbf{W} = \psi\mathbf{B}_r\mathbf{I} \tag{4-24b}$$

From equations (4-24a) and (4-24b), a 6th-order system realisation structure can be obtained as shown in Fig.4-8.

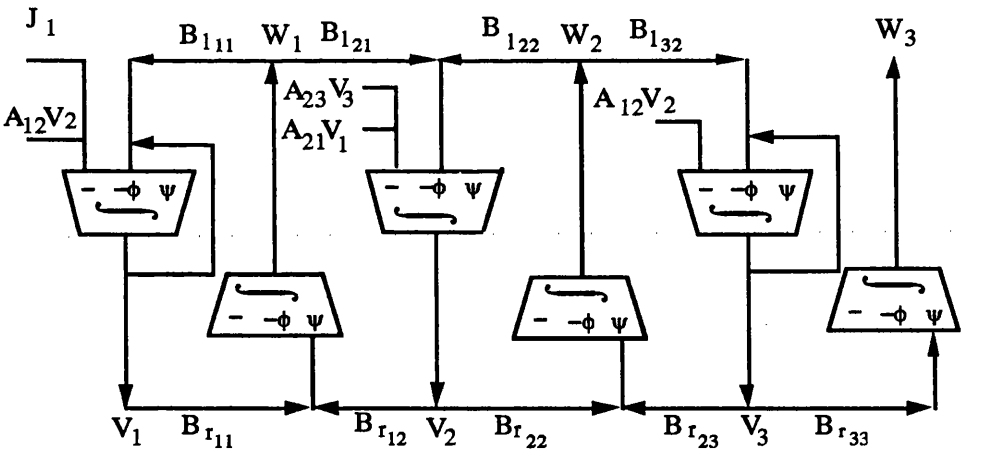


Fig.4-8 6th-order Right Decomposition SI Structure

The four right decomposition methods are as follows.

Right-LU Decomposition

If **B** is decomposed as **B=LU**, the design equations are

$$\mathbf{AI} = -\phi(\mathbf{LW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (4\text{-}25a)$$

$$\mathbf{W} = \psi\mathbf{U} \quad (4\text{-}25b)$$

For the lowpass case, the Right-LU Decomposition results in identical circuit structures to those derived from a leapfrog approach.

Right-UL Decomposition

Let **B=UL**, the system design equations become

$$\mathbf{AI} = -\phi(\mathbf{UW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (4\text{-}26a)$$

$$\mathbf{W} = \psi\mathbf{L} \quad (4\text{-}26b)$$

Right-IB Decomposition

If **B=IB**, the system design equations are

$$\mathbf{AI} = -\phi(\mathbf{BW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (4\text{-}27a)$$

$$\mathbf{W} = \psi\mathbf{I} \quad (4\text{-}27b)$$

Right-BI Decomposition

For **B=BI**, the following design equations are obtained

$$\mathbf{AI} = -\phi(\mathbf{IW}+\mathbf{DI})+\mathbf{J}(1+z^{-1})/(1-z^{-1}) \quad (4\text{-}28a)$$

$$\mathbf{W} = \psi\mathbf{B} \quad (4\text{-}28b)$$

The input current J_1 in Fig.4-8 is

$$J_1 = J_{in}\frac{1+z^{-1}}{1-z^{-1}} \quad (4\text{-}29)$$

This can be realised by any bilinear SI integrator. Fig.4-9 is the realisation structure based on the basic building block in Fig.4-5.

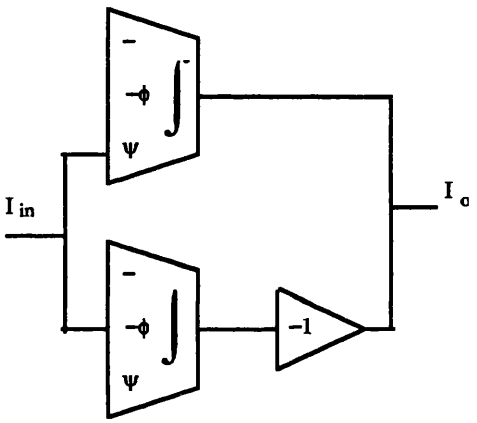


Fig.4-9 Right Decomposition Input Terminal SI Realisation

4.3.3 Circuit Scaling for Ladder Based Switched-Current Filters

Two kinds of scaling are involved in the matrix design approach. These are maximum dynamic range scaling and minimum transistor ratio scaling.

4.3.3.1 Maximum Dynamic Range Scaling

For SI filters the maximum dynamic range is determined by the peak output signal current relative to the DC bias current of that stage. To equalise this ratio for each stage, either the signal current and/or the DC bias current can be scaled. If no scaling is performed, there will be some reduction in dynamic range with direct simulation.

A general matrix system is a very convenient form for scaling the design. For left and right decomposition methods, the equations

$$\begin{bmatrix} \mathbf{A}_l & \psi\mathbf{B}+\mathbf{D} \\ -\mathbf{I}_u\phi & \mathbf{A}_r \end{bmatrix}\begin{bmatrix} \mathbf{W} \\ \mathbf{I} \end{bmatrix}=\begin{bmatrix} \mathbf{J}(1+z^{-1}) \\ \mathbf{0} \end{bmatrix} \tag{4-30}$$

$$\begin{bmatrix} \mathbf{A}+\phi\mathbf{D} & \phi\mathbf{B}_l \\ -\psi\mathbf{B}_r & \mathbf{I}_u \end{bmatrix}\begin{bmatrix} \mathbf{I} \\ \mathbf{W} \end{bmatrix}=\begin{bmatrix} \frac{1+z^{-1}}{1-z^{-1}}\mathbf{J} \\ \mathbf{0} \end{bmatrix} \tag{4-31}$$

can be used to perform scaling. These two equations can be simplified as

$$\mathbf{MX}=\mathbf{J} \tag{4-32}$$

In the dynamic range scaling phase, a frequency sweep analysis of the filter passband is performed to determine the maximum signal levels of the internal currents. Scaling can be done by multiplying column j of M by the maximum value of the variable X_j for all variables in X. This is equivalent to creating a new variable X_j/X_{jmax}, where X_{jmax} is the maximum value attained by X_j.

4.3.3.2 Transistor Ratios Reduction Scaling

The elements in matrix M determine the circuit parameters and the transistors W/L. The ratio of maximum to minimum element value in M determines the transistor

aspect ratios in an SI circuit. For each row of equation in (23), a minimum entry can be found. By dividing each entry in the same row by the smallest coefficient, a scaled equation is obtained. However this scaling does not have any effect on system response, and the transistor aspect ratios can be reduced as long as the maximum and minimum elements are not within the same row of equations.

4.3.4.Design Example

All the decompositions and scaling routines have been incorporated in XFILT. An example of a 10th-order bandpass filter is given here to show the utility of the approach. The filter has 1.5dB passband ripple with passband extending from 800kHz to 1.2MHz, 50dB stopband attenuation and a sampling frequency of 10MHz. The matrix entries translate directly to ratios of transistor width/length ratios (elsewhere called circuit coefficient values or simply g_m ratios). Comparative design results are shown in Table 4-1, where the Left-UL is seen to be the most efficient realisation. By trying the all design methods, we can achieve about 39.04% reduction in g_m spread and 38.73% reduction in g_m sum. The simulated Left-UL circuit response is shown in Fig.4-10 and Fig.4-11 shows the circuit schematic with the biasing circuits omitted. To compare the sensitivity performance, the total multiparameter sensitivity simulation over all g_ms has been carried out. The sensitivity simulation results of a comparative biquad realisation, having a maximum g_m spread of 63.78, are also presented in Fig.4-12. It is clear that the ladder based design demonstrates lower passband sensitivity, especially in the vicinity of the corner frequencies.

	Integs	SWs	g_m Spread	g_mSum
Left-LU	10	34	16.32	813.04
Left-UL	10	34	14.55	727.02
Left-IA	10	34	21.93	1038.44
Left-AI	10	34	18.83	909.01
Right-LU	12	36	16.11	830.77
Right-UL	12	36	18.00	923.38
Right-IB	12	36	23.87	1186.68
Right-BI	12	36	16.11	836.49

Table 4-1. Comparative design results for 10th-order bandpass SI filters

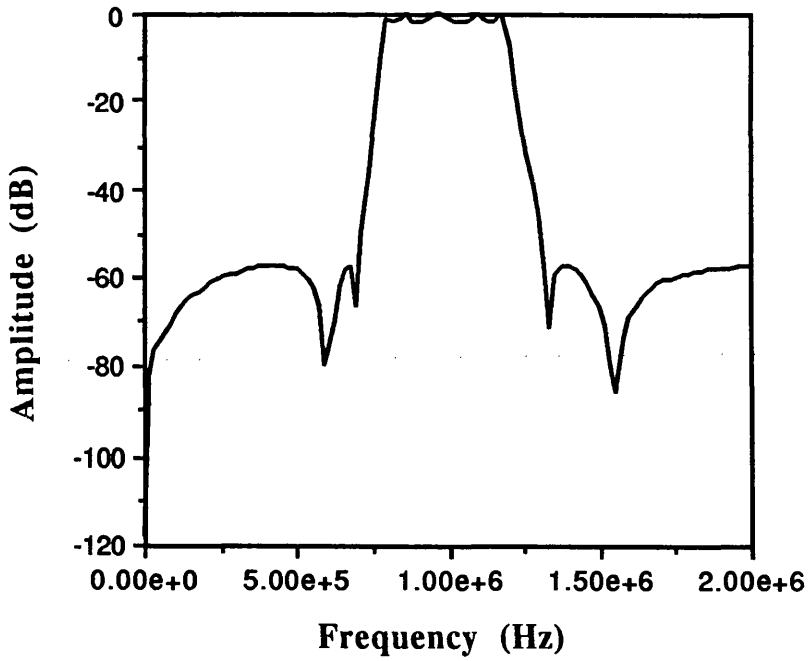


Fig.4-10 10th-order bandpass SI filter response

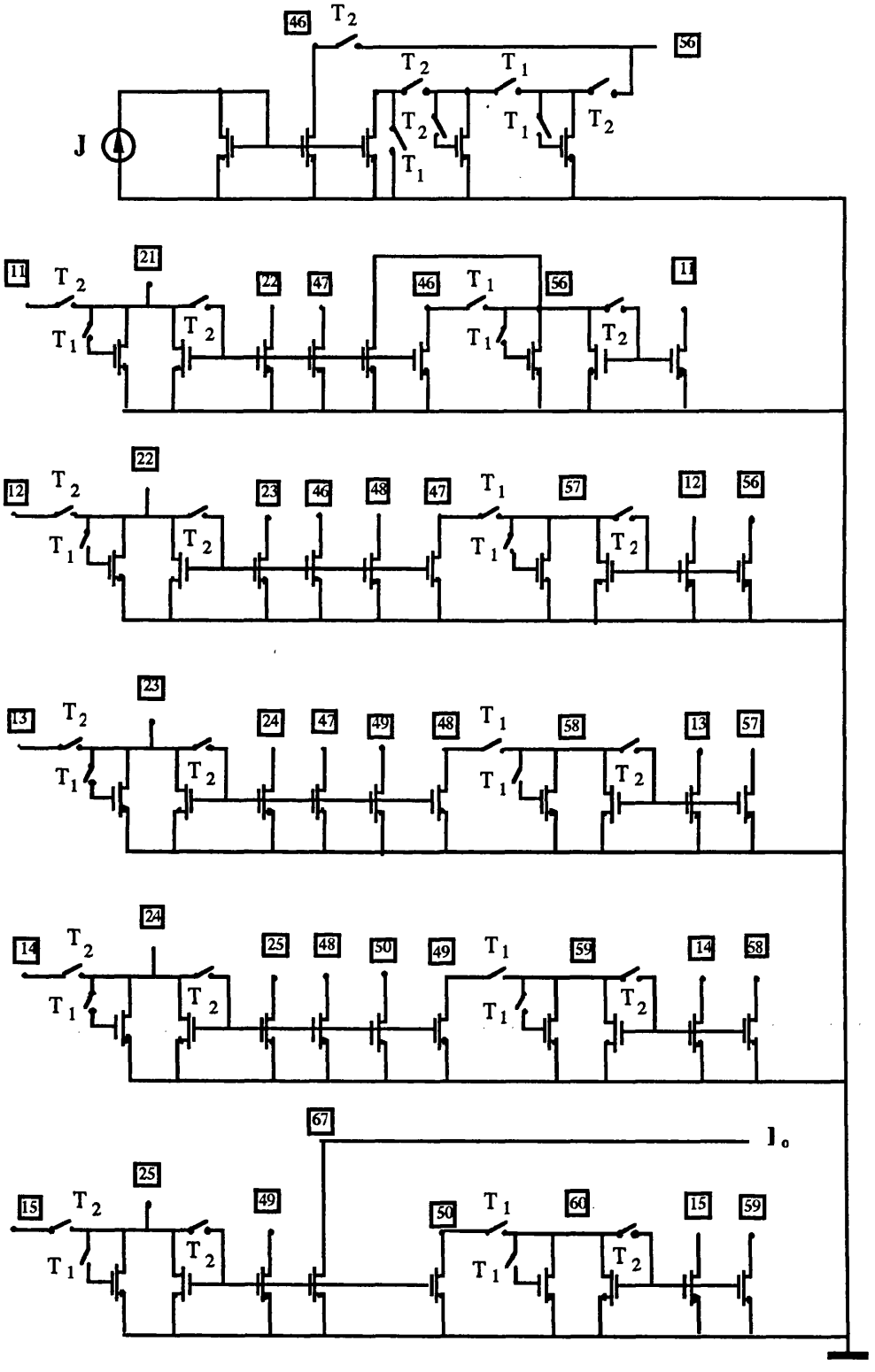


Fig.4-11 Circuit schematic realisation of SI filter

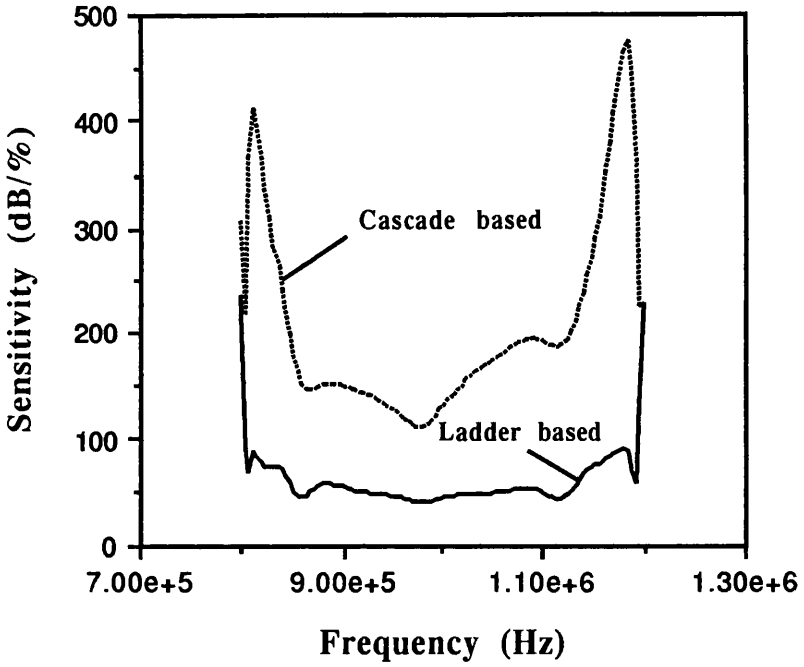


Fig.4-12 Sensitivity simulation of the SI bandpass filter

4.4 SENSITIVITY COMPARISON OF SWITCHED-CURRENT FILTERS REALISED BY FIRST AND SECOND GENERATION SWITCHED-CURRENT MEMORY CELLS

Although the SI technique has been widely used to construct filters and converters and many SI building blocks have been proposed recently, the first generation[1] and second generation[2] memory cells are still the most fundamental elements. The overall performance of an SI system is determined directly from errors in its constituent memory cells.

Mismatch is a problem common to all high precision analogue circuits, and arises from the small variations in transistor characteristics. In contrast to digital circuits, the fabrication tolerance of electrical characteristics of analogue integrated circuits depends highly on the device matching accuracy. The result of transistor mismatch is

to introduce both gain error and an offset in the memory cell. The basic second generation SI memory cell was proposed as a modification of the first generation SI memory cell to reduce sensitivity to transistor mismatch performance. However, recent results from comparison of the two cells produced two quite different conclusions[19,2].

4.4.1 Sensitivity Comparison Based on Memory Cell

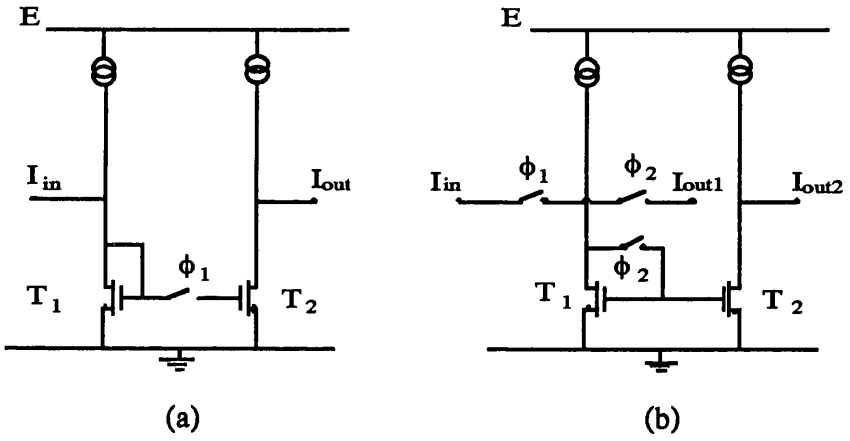


Fig.4-13 (a) first generation SI memory cell (b) second generation SI memory cell

The circuit schematics of first generation and second generation memory cells are shown in Fig.4-13(a) and Fig.4-13(b). It has been shown that[19]

$$\frac{I_{out}(z)}{I_{in}(z)} = \frac{(W/L)_2}{(W/L)_1} z^{-1/2} \tag{4-33}$$

for the first generation memory cell and

$$\frac{I_{out1}(z)}{I_{in}(z)} = z^{-1/2} \tag{4-34a}$$

$$\frac{I_{out2}(z)}{I_{in}(z)} = \frac{(W/L)_2}{(W/L)_1} z^{-1/2} \tag{4-34b}$$

for the second generation memory cell. Eq.(4-34a) demonstrates that when the output is taken from I_{out1}, the basic second generation SI memory cell does not suffer from mismatch errors since the same memory transistor is used in both the sampling and retrieval phase. However, in SI filter circuits the ratios between transistors are used to determine filter coefficients in the same way as capacitor ratios are employed in SC circuits. To construct filters, the second generation memory cell with an output taken from I_{out2} has to be used. Hence similar sensitivity properties for both cells ensue.

4.4.2 Sensitivity Comparison Based on Switched-Current Integrator

However, quite a different conclusion can be obtained from the sensitivity analysis of SI integrators formed from first generation and second generation memory cells. When a first generation memory cell is used to produce an integrator, the transfer function has the form:

$$H(z) = \frac{Az^{-1}}{1 - Bz^{-1}} \tag{4-35}$$

Here A and B are transistor aspect ratios. It can be shown[2] that sensitivity of ω_0/Q to B is $-\infty$ when B=1. The transfer functions of integrators formed by the second generation memory cell are

$$H(z) = \frac{-A_2}{1 - Bz^{-1}} \tag{4-36a}$$

for a backward Euler damped integrator or

$$H(z) = \frac{A_1 z^{-1}}{1 - Bz^{-1}} \tag{4-36b}$$

for a forward Euler damped integrator. Here A_1, and A_2 are transistor aspect ratios and B is a combination of transistor aspect ratios. In each case, the sensitivity of ω_0/Q to transistor aspect ratio is $2/(2+\alpha_4)$, (α_4 is a transistor aspect ratio) which is much less sensitive than the first generation integrator.

For the simple memory cell or integrator, a direct mathematical expression can be obtained and insight into sensitivity can be obtained from the explicit expression. But for the complicated filter transfer function, no direct mathematical expression can be obtained easily. Is the second generation memory cell really better in sensitivity performance in filter realisation ? And if it is better, then to what level ? The question can only be answered when both the first generation and the second generation based memory cell filters are designed and simulated or tested. Based on the matrix design approach and the XFILT system, we show that second generation memory cell based filters do display a better sensitivity performance than first generation memory cell based filters. And we also show that sensitivity of SI filters based on first generation SI memory cells is highly related to the ratio of the sampling frequency to cutoff frequency in lowpass case or midband frequency in bandpass case.

4.4.3 The Multiparameter Sensitivity Definition for Switched-Current Filter

The sensitivity information of a filter can show all the effect of circuit changes. To compare the sensitivity performance, the following multiparameter sensitivity index is used as a global measure of SI filter system sensitivity

$$S(\omega) = 8.686\left\{\sum_i\left[\frac{Gm_i}{|H(\omega)|}\frac{\partial|H(\omega)|}{\partial Gm_i}\right]^2\right\}^{1/2} / 100.0 \qquad (4\text{-}37)$$

where Gm_i is the transconductance of each transistor which can reflect any mismatch caused in the transistor parameters such as threshold voltage V_t, device aspect ratio W/L, transconductance parameter μ and the channel-length modulation parameter λ.

4.4.4 Sensitivity Comparison of Lowpass Switched-Current Filters

Example 1: The first example is a 5th-order elliptic lowpass filter with cutoff frequency 2MHz, passband ripple 0.5dB, and stop band attenuation 50dB. The filter is designed by simulation of the prototype ladder and the right-BI decomposition is applied in circuit realisation. The bilinear transformation is employed in the circuit realisation. The SI filter circuit contains 7 integrators with a maximum transistor aspect ratio 15.28. The simulated circuit response is shown in Fig.4-14. Sensitivity simulation results of ladder filter based on first generation and second generation memory cells are given in Fig.4-15. It is clearly shown from Fig.4-15 that the second generation memory cell based structures have much better sensitivity performance than that of the first generation memory cell based structures. A sensitivity peak at low frequencies is displayed in first generation based realisation. It is also noticed that for the first generation structures the sensitivity increases when $R=f_c/f_{cutoff}$ increases (f_c is sampling frequency and f_{cutoff} is lowpass filter cutoff frequency).

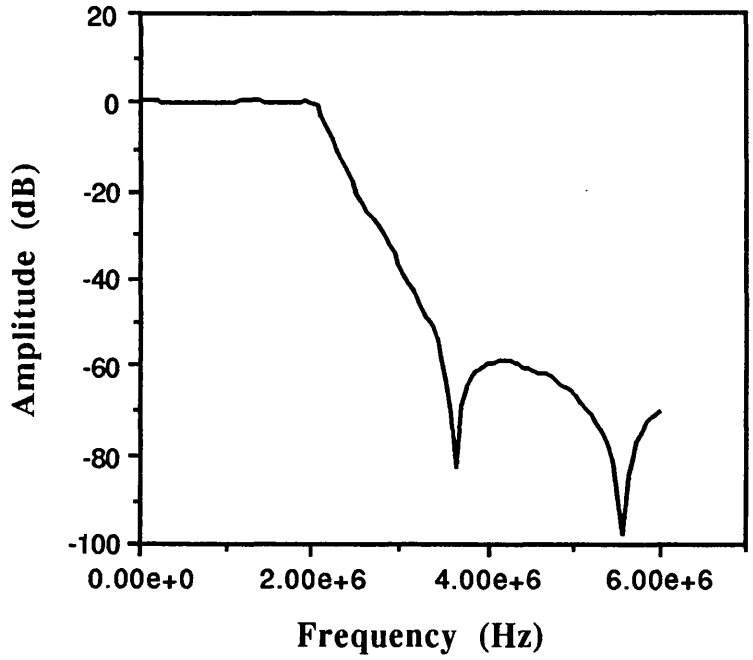


Fig.4-14 5th-order Lowpass Response

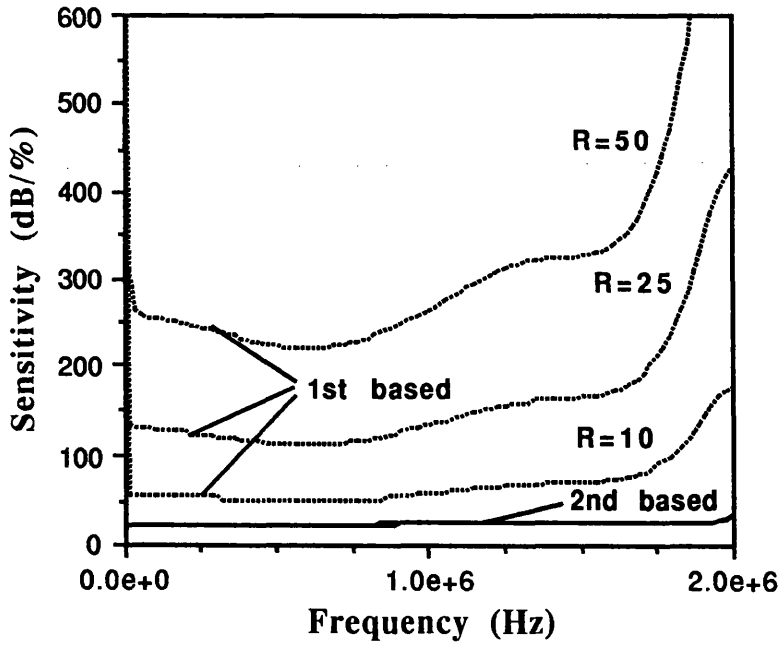


Fig.4-15 Sensitivity simulation results

Example 2: The second lowpass SI filter is a 4th-order Elliptic filter with passband ripple 1dB, stopband attenuation 50dB, cutoff frequency 1MHz and is realised by cascade structure. The simulated circuit response is shown in Fig.4-16. Both the first generation memory cell based biquad and the second generation memory cell biquad are used to construct the filter circuit. The sensitivity simulation results are given in Fig.4-17. Better sensitivity performance can be obtained by using the second generation memory cell based biquads. It is also noticed that the sensitivity increases when the R increases in first generation based realisations.

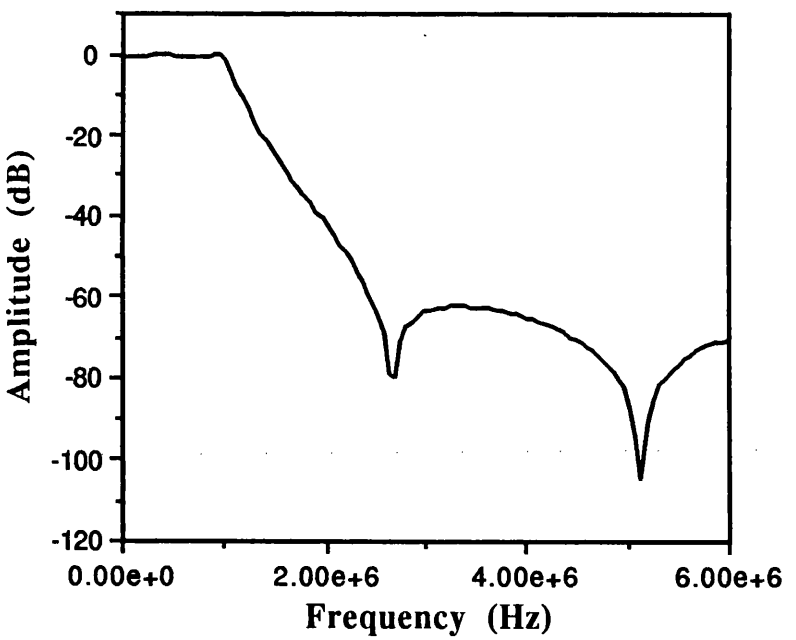


Fig.4-16 4th-order lowpass response

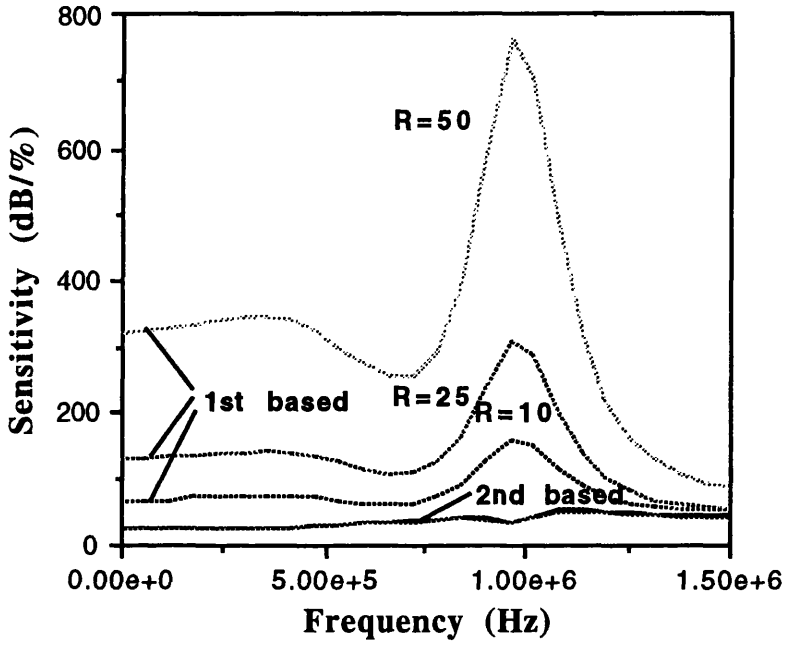


Fig.4-17 Sensitivity simulation results for biquad realisation

Sensitivity simulation of two examples of lowpass filters show that the second generation SI memory cell based filters have better sensitivity performance for both ladder derived or cascade structures. The sensitivity of the first generation based SI filters is related to the R while the sensitivity of the second generation based SI filter are not.

4.4.5 Sensitivity Comparison of Bandpass Switched-Current Filter

Example 3. A 10th-order Elliptic Bandpass Filter has the specifications

Passband	0.8MHz to 1.2MHz
Stopbands	0.1HZ to 0.653MHz and 1.33MHz to 10MHZ
Passband Ripple	1.5dB
Stopband Attenuation	50dB

Sampling Frequency 20MHz

The bandpass filter response is shown in Fig.4-18. A ladder based SI filter using right-BI decomposition is designed. The SI circuit contains 10 integrators and with a maximum transistor aspect ratio 29.64. Sensitivity simulation results of the first generation and second generation based structures are given in Fig.4-19. These show that the second generation memory cell based structures give better sensitivity performance. The sensitivity of the first generation memory cell based structure is found to depend on the ratio of $R = f_c/f_0$, where f_0 is the midband frequency and f_c is the sampling frequency. The larger the R, the higher the sensitivity. The sensitivity of the second generation SI memory cell based structure shows no change with the change in R.

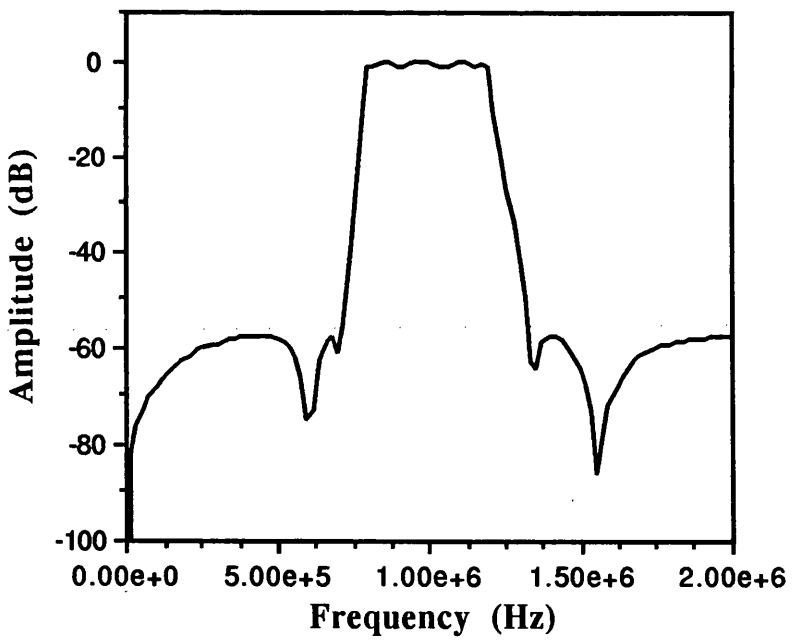


Fig.4-18 10th-order bandpass response

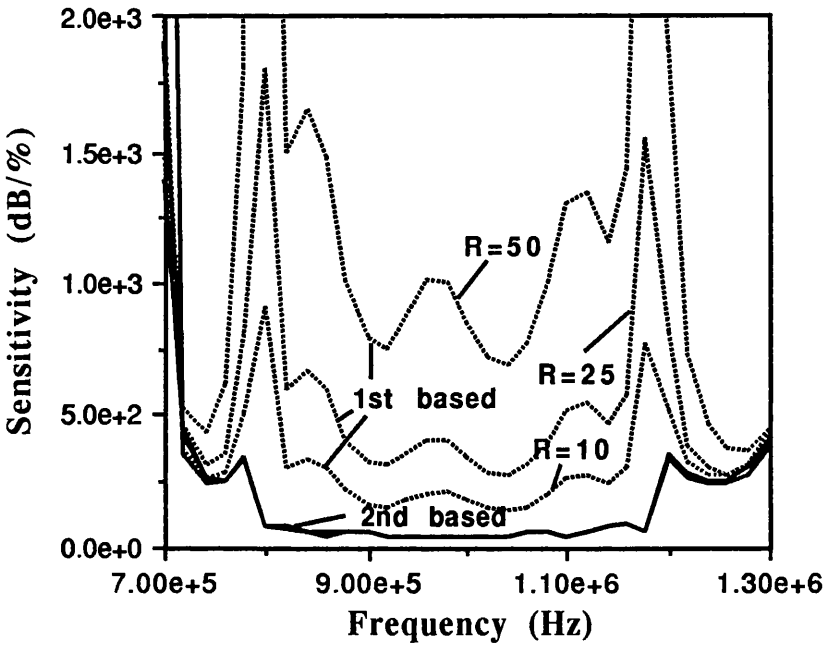


Fig.4-19 Sensitivity simulation results

Example 4: This is a video frequency 8th-order Elliptic bandpass filter with specifications of passband from 4.25MHz to 6.8MHz, stopbands from 0.1Hz to 3.75MHz and from 7.25MHz to 10MHz, passband ripple 0.5dB and stopband attenuation 20dB. The filter is realised by cascading four biquads. The filter response is shown in Fig.4-20 and the sensitivity simulation of the first and the second generation SI memory cell based structures is shown in Fig.4-21. These show that the second generation memory cell based structures give better sensitivity performance. The sensitivity of the first generation memory cell based structure also depends on the R. The larger the R, the higher the sensitivity. The sensitivity of the second generation SI memory cell based structure shows no change with changing R.

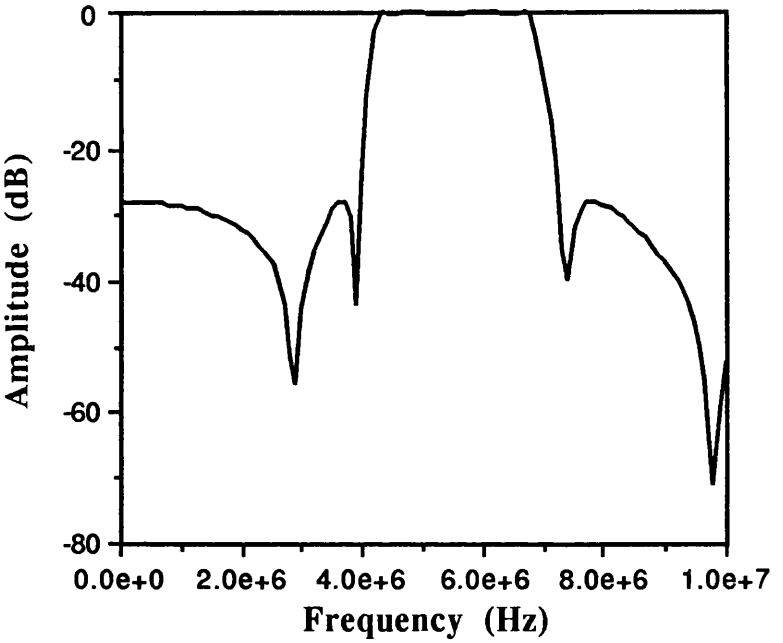


Fig.4-20 8th-order bandpass response

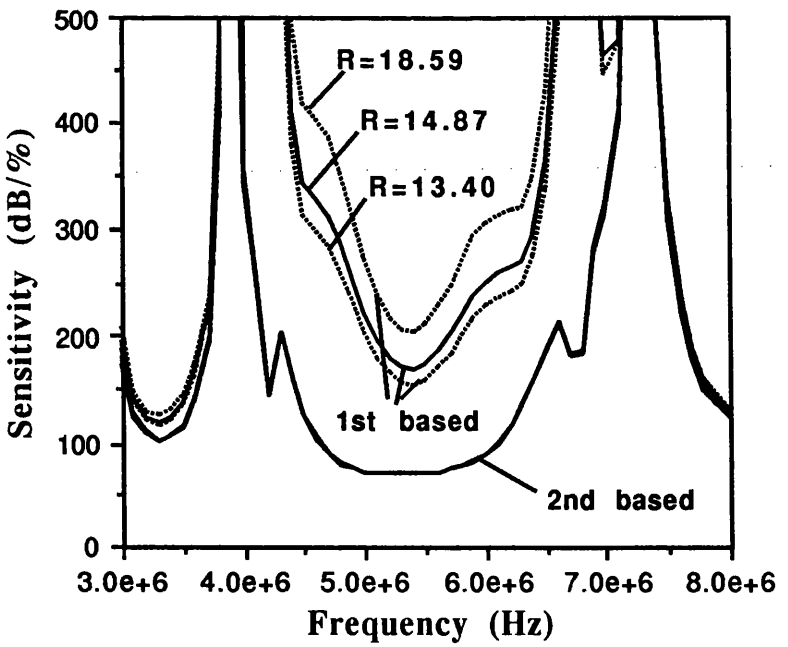


Fig.4-21 Sensitivity simulation results

4.4.6 Summary of Sensitivity Comparisons

From the above comparison it is shown that better sensitivity performance of second generation SI cell based structures is demonstrated by four filters. For SI filters based on first generation memory cells, it is shown that high ratio of clock frequency to cutoff frequency in lowpass case or high ratio of clock frequency to midband frequency in bandpass case would introduce high sensitivity performance, while the sensitivities of SI filters based on the second generation memory cell are not affected by the ratio.

4.5 COMPARISON OF LADDER BASED SWITCHED-CURRENT FILTER REALISATION

In order to determine the suitability of each matrix decomposition method for ladder based switched-current (SI) filters, a comprehensive comparison of filter parameter spread, total Gm, sensitivities and noise performance is carried out in this section. Four different types (lowpass, bandpass, bandstop and highpass) have been designed and compared. Further understanding has been obtained and suitability of the proposed approach has been shown. All the comparisons are based on the second generation memory cell based structures.

4.5.1.Circuit Comparison of Switched-Current Filters Realised by Different Methods

1. 5th-Order Elliptic Lowpass Filter

The first example is a 5th-order Elliptic lowpass filter with cutoff Frequency 10kHz, passband ripple 1.5dB, stopband attenuation 40dB, and sampling frequency 100kHz.

The frequency response of one of circuits is shown in Fig.4-22 and the statistics of the eight different design methods are given in Table 4-2.

	No. Int	No. SW	Gm Spread	Gm Sum
Left-LU	6	22	7.21	262.91
Left-UL	6	22	8.46	252.09
Left-IA	6	22	8.19	285.25
Left-AI	6	22	9.74	297.16
Right-LU	7	21	12.60	338.78
Right-UL	7	21	12.60	338.78
Right-IB	8	24	12.60	372.78
Right-BI	8	24	9025823.23	76410596.22

Table 4-2 Statistics of SI Lowpass Filters

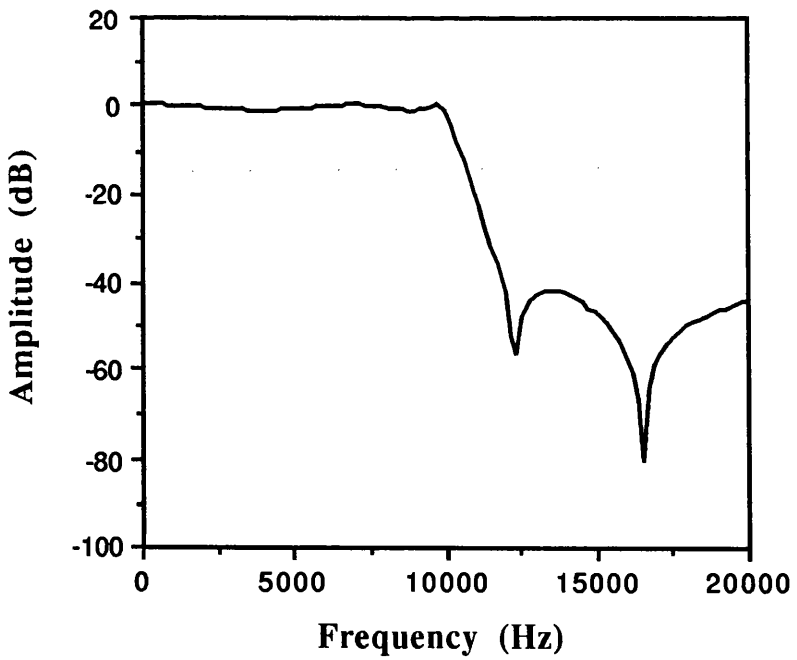


Fig.4-22 Frequency Response of SI Lowpass Filter

From Table 4-2 it is shown that the Left Decomposition Methods yield less gm spread and gm sum. However, the sensitivity simulation later will show that Left Decomposition Methods produce a very high sensitivity in D.C. gain, therefore only Right Decomposition Methods are suitable for lowpass filter design. Right-LU and Right-UL give the most efficient circuit realisation with minimum gm sum and gm spread.

2. 10th-Order Elliptic Bandpass Filter

The second design example is a 10th-order Elliptic bandpass filter with passband from 0.8MHz to 1.2MHz, stopband from 0.1HZ to 0.653MHz and 1.33MHz to 10MHz, passband ripple 1.5dB, stopband attenuation and 50dB sampling frequency 20MHz. The frequency response of the filter is shown in Fig.4-23 and the statistics of the different matrix based designs are given in Table 4-3. It is shown that the Left-UL is a best realisation with the minimum gm sum and gm spread. By trying the all design methods, we can achieve, about 33.26% reduction in gm spread and 35.07% reduction in gm sum.

	No. Int	No. SW	Gm Spread	Gm Sum
Left-LU	10	34	33.88	1418.49
Left-UL	10	34	29.64	1253.62
Left-IA	10	34	44.41	1810.41
Left-AI	10	34	38.25	1561.54
Right-LU	12	36	33.31	1448.09
Right-UL	12	36	34.40	1491.51
Right-IB	12	36	44.40	1930.82
Right-BI	12	36	33.31	1454.20

Table 4-3 Statistics of SI Bandpass Filter Design

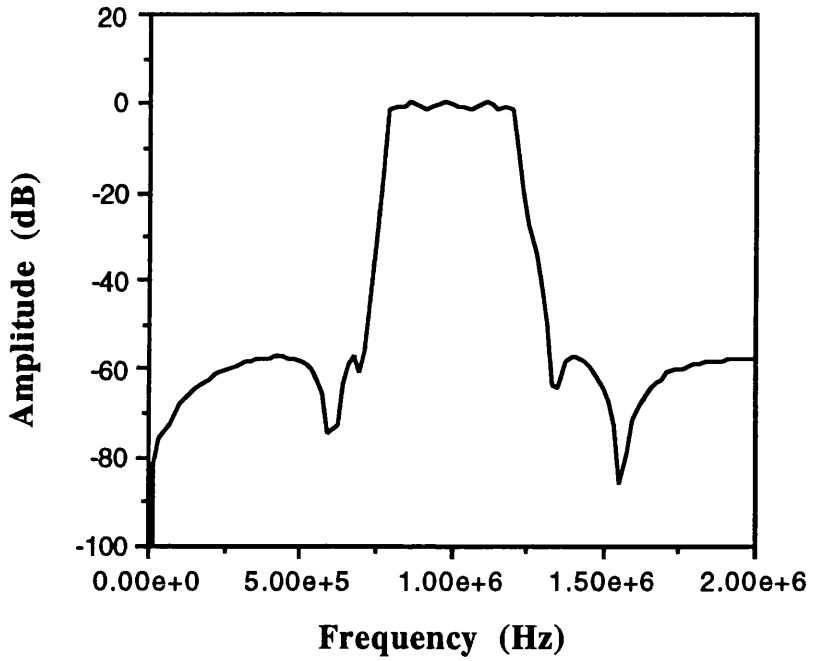


Fig.4-23 Frequency Response of SI Bandpass Filter

3. 6th-Order Butterworth Highpass Filter

This is a 6th-order Butterworth highpass filter with passband from 300Hz to 32kHz, stopband from 0.1Hz to 180Hz, passband ripple 1.6dB, and stopband attenuation 38dB. The circuit frequency response is shown in Fig.4-24 and the statistics of SI designs are given in Table 4-4 (X denotes an ill-condition solution). It can be seen that the Left-LU gives smallest gm spread and the Left-IA has smallest gm sum, either structure can be selected for practical realisation.

	No. Int	No. SW	Gm Spread	Gm Sum
Left-LU	8	28	95.03	2400.55
Left-UL	8	28	311.03	3697.58
Left-IA	8	28	102.47	2188.50
Left-AI	8	28	648.87	21944.36
Right-LU	10	30	5138.58	141995.54
Right-UL	8	28	117.81	3288.00
Right-IB	10	30	117.81	X
Right-BI	10	30	5075.89	143727.35

Table 4-4 Statistics of SI Highpass Filter Design

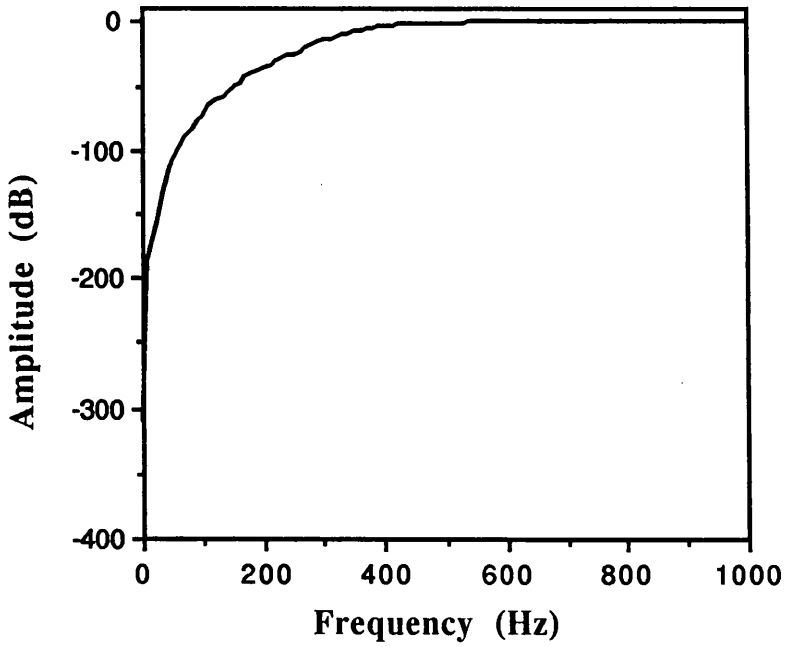


Fig.4-24 Frequency Response of SI Highpass Filter

4.6th-Order Bandstop SI Filter

The final example is a 6th-order bandstop SI filter with passband from 0.1Hz to 4.5kHz and 5.2kHz to 20kHz, passband ripple 1dB, stopband from 4.8kHz to 4.9kHz, and stopband attenuation 20dB. The frequency response of the filter is shown in Fig.4-25 and the Table 4-5 gives the statistics of all the different designs. The results suggest that the Left-IA and Left-AI can be regarded as a suitable structures, of which Left-IA has the lowest gm sum and Left-AI has the smallest gm spread.

	No. Int	No. SW	Gm Spread	Gm Sum
Left-LU	10	34	415544.04	2648724.27
Left-UL	10	34	24368.00	192168.30
Left-IA	10	34	287.71	10213.46
Left-AI	10	34	249.26	11504.22
Right-LU	11	33	552.74	20069.21
Right-UL	11	33	343.65	12319.78
Right-IB	12	36	343.64	12998.59
Right-BI	12	36	928102.35	7846032.70

Table 4-5 Statistics of SI Bandstop Filter Design

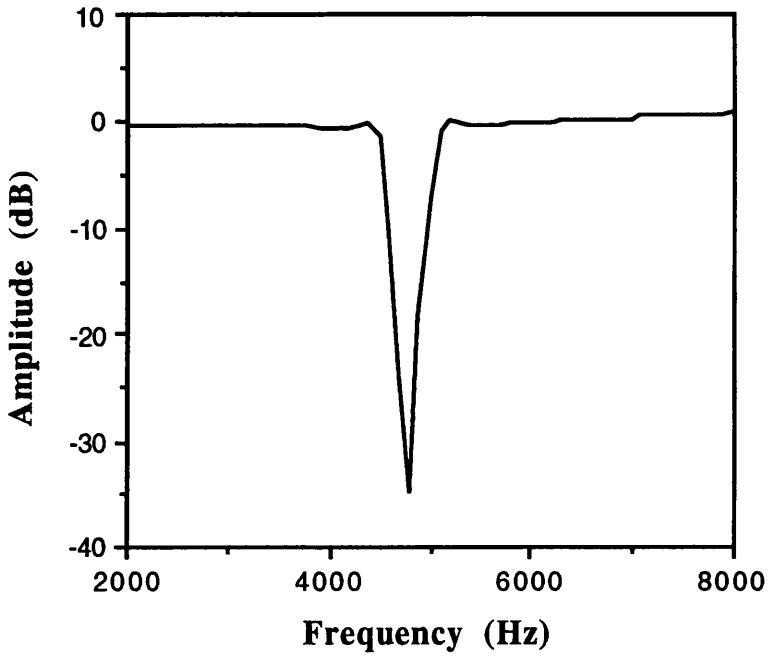


Fig.4-25 Frequency Response of SI Bandstop Filter

4.5.3.Total Sensitivity Comparison of Switched-Current Filters

Fig.4-26 gives a comparison of sensitivities for the various ladder based lowpass filter realisations. It shows that a large peak of sensitivity exists at low frequencies in all the left decomposition approaches as well as right-BI and right-IB. The best sensitivity performance is obtained by right-LU or right-UL approach. The comparison of bandpass filter sensitivities is shown in Fig.4-27, the results demonstrate that all the decomposition methods give good sensitivity performance. Fig.4-28 is the highpass filter sensitivity comparison, it can be seen that the left matrix decomposition approach gives better sensitivity performance, with left-LU and left-UL being the best ones. The bandstop filter sensitivity comparison is given in Fig.4-29. Only right-LU and right-UL decompositions present good performance, with all others having a big peak at low frequencies.

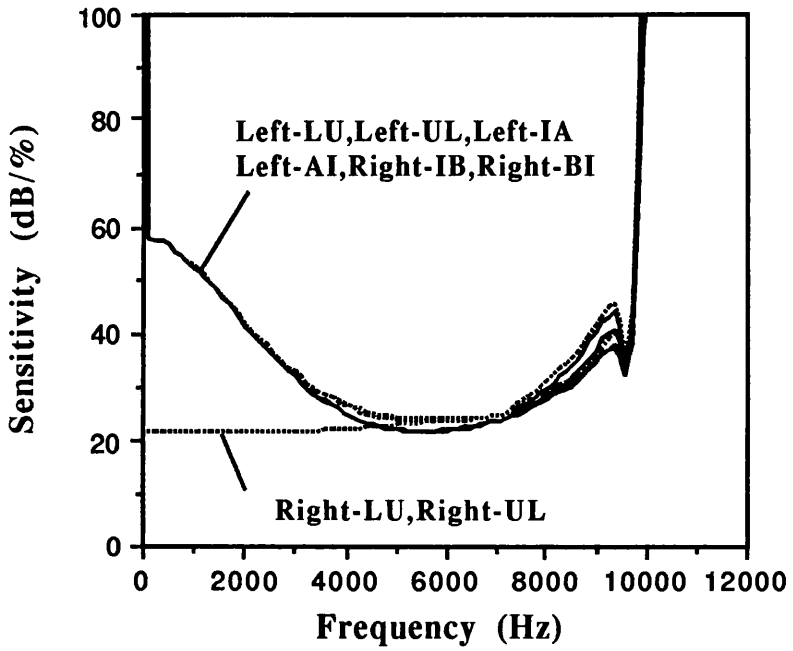


Fig.4-26 Sensitivity Comparison of SI Lowpass Filters

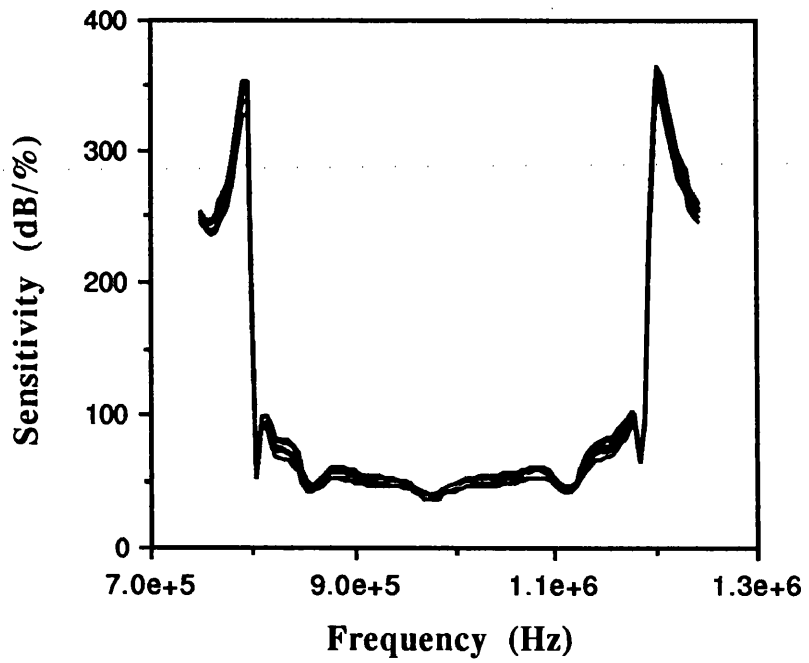


Fig.4-27 Sensitivity Comparison of SI Bandpass Filters

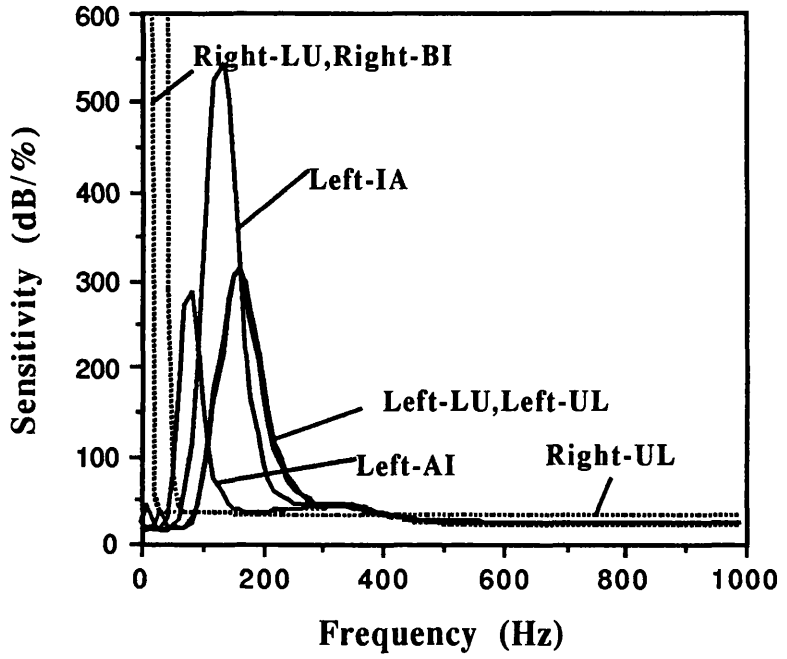


Fig.4-28 Sensitivity Comparison of SI Highpass Filters

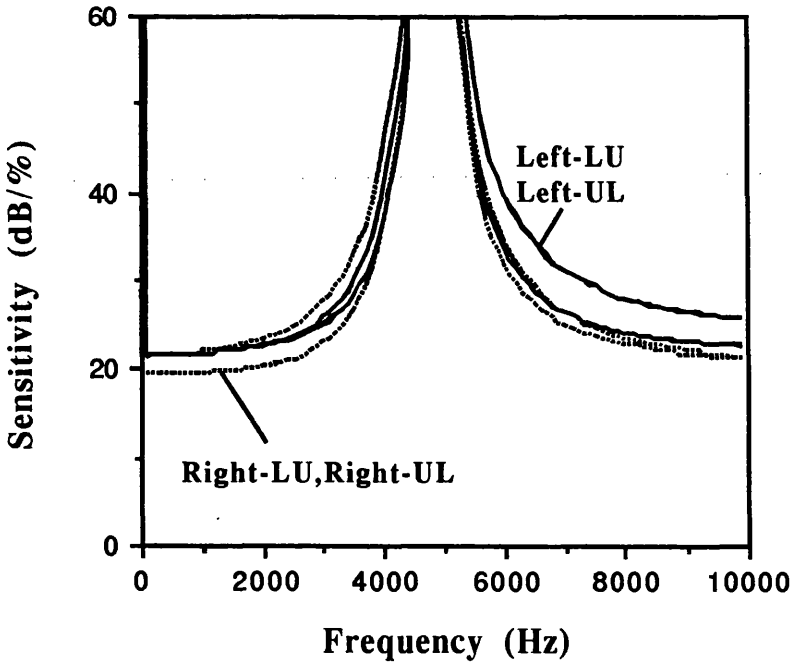


Fig.4-29 Sensitivity Comparison of SI Bandstop Filters

4.3.4. Noise Performance Comparison of Switched-Current Filter

The noise comparisons are presented in Fig.4-30 to Fig.4-33. It is assumed that the equivalent magnitude of the white noise of a MOS transistor is $10nA/\sqrt{Hz}$, and the corner frequency of the 1/f noise is 100Hz, and 10 higher band contributions are considered. The lowpass filter noise comparison is shown in Fig.4-30. It shows that right-LU and right-UL present best noise performance and right-BI gives poorest performance. Fig.4-31 is a bandpass filter noise comparison, it demonstrates that all the decomposition methods give good performance, with right-LU, right-UL and right-BI being slightly better. The highpass filter noise comparison is shown in Fig.4-32. It demonstrates that left-LU, left-UL are the best candidates, right-UL is with good performance, and right-LU, right-BI, left-IA and left-AI are all poor in performance. The bandstop filter noise comparison is shown in Fig.4-33, right-LU and right-UL have good performance and right-BI the poorest performance.

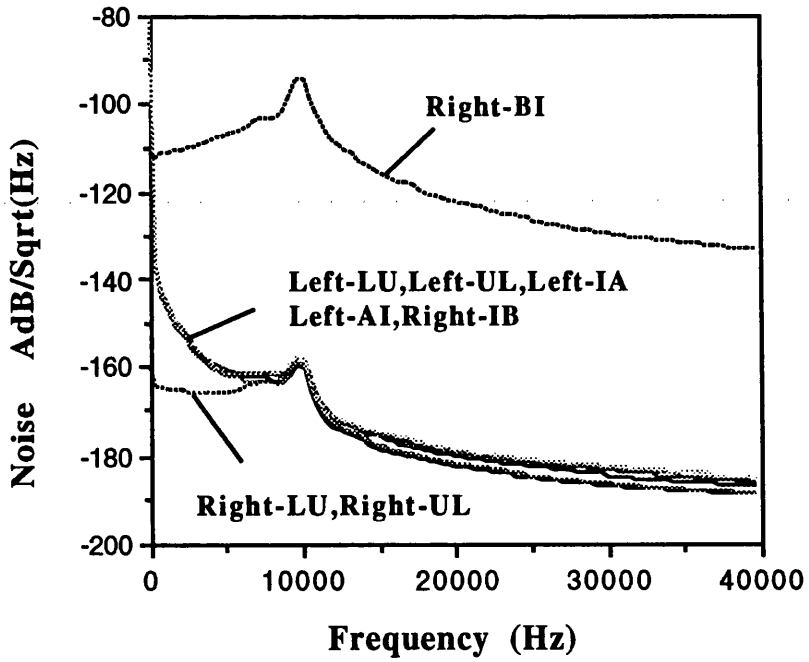


Fig.4-30 Noise Performance Comparison of SI Lowpass Filters

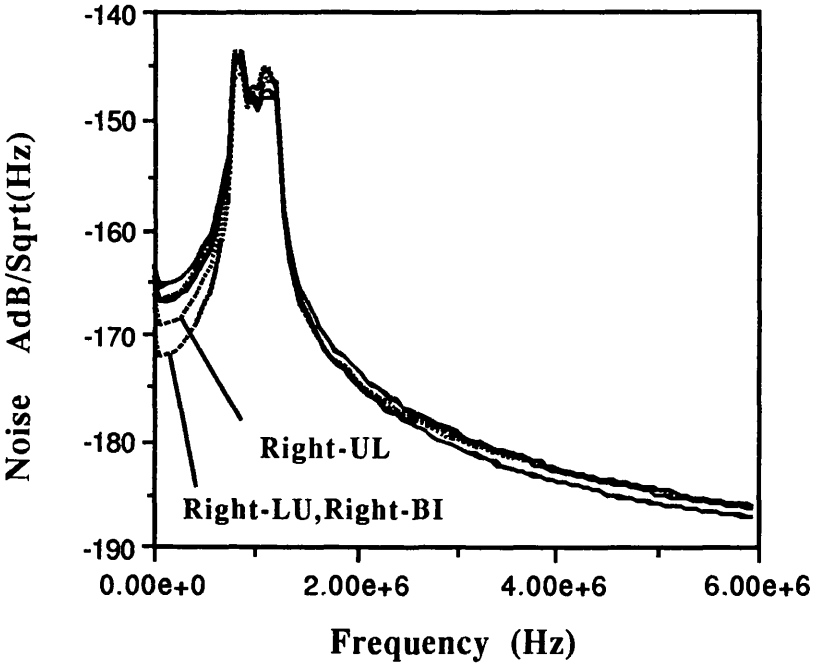


Fig.4-31 Noise Performance Comparison of SI Bandpass Filters

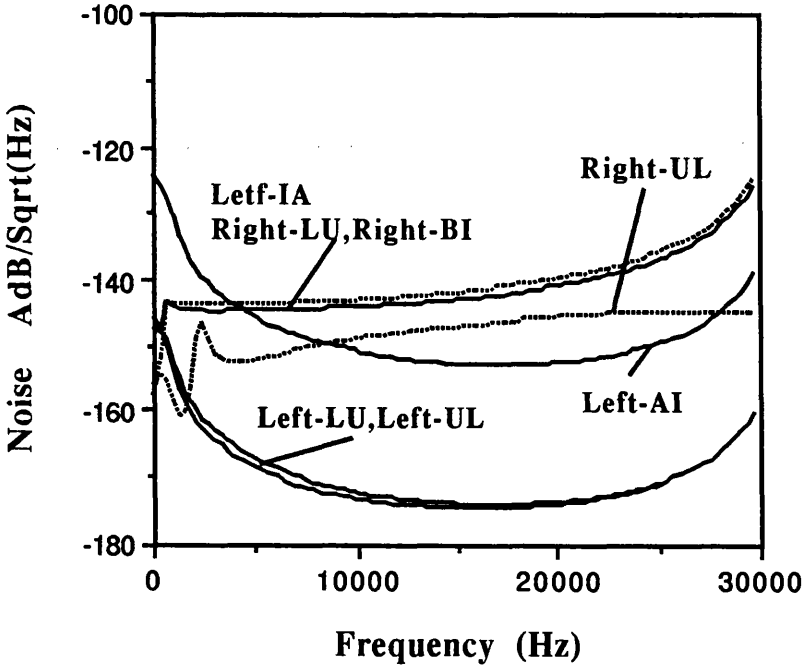


Fig.4-32 Noise Performance Comparison of SI Highpass Filters

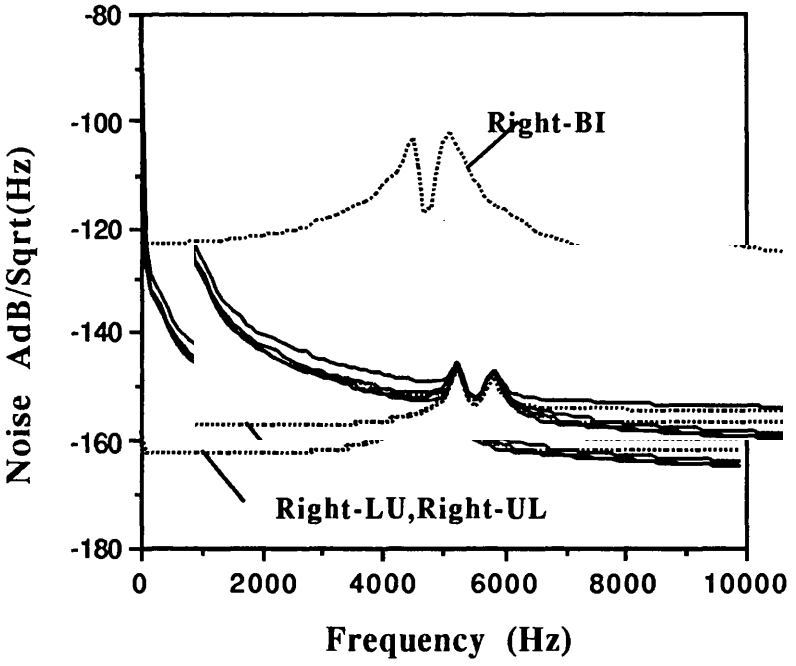


Fig.4-33 Noise Performance Comparison of SI Bandstop Filters

4.5.4 Summary of Comparison of Ladder Based Switched-Current Filter Realisations

Following conclusions can be obtained from above comparison

1. Right-LU and Right-UL are the best candidates for lowpass filter design, having small gm spread, gm sum, lower sensitivity and better noise performance.
2. All the decompositions yield reasonable circuit structures for bandpass filter realisation and they all have similar sensitivity performance. For small gm spread and gm sum, the Left-LU and Left-UL can be chosen. For better noise performance, the Right-LU and Right-UL can be chosen.
3. Left-LU is a best choice of highpass filter realisation with small gm spread, gm sum, lower sensitivity and better noise performance.

4. Left-AI and Left-IA achieve most efficient circuit realisations, though Right-LU and Right-UL offer better sensitivity and noise performance in bandstop filter realisations.

The above are only a general guidelines, which will be helpful for novice users in starting a filter design. Many special cases can lead to a different result and particular care must be taken. Since the XFILT design system is available, it is always better to try many designs before committing to hardware realisation.

4.6 S^2I INTEGRATOR BASED SWITCHED-CURRENT LADDER FILTER DESIGN APPROACH

The SI memory cell is the most primitive element in an SI circuit, therefore naturally great effort has been expended in developing improved versions. Over the years, the non-ideal behaviour, which includes finite conductance errors, charge injection errors, settling errors, mismatch errors, noise errors have posed the major problems in SI circuit design and several modified memory cells to overcome some of these effects have been proposed. The cascode memory cell[13], regulated cascode memory cell[14], folded cascode memory cell[6], active memory cell[15], common gate memory cell[16,17], and class AB technique memory cell[18] are just some of those proposed for enhancing the memory cell performance. However, all these approaches have drawbacks for silicon area, power dissipation, bandwidth and low supply voltage operation. Recently, Hughes and Moulding have proposed an elegant and simple scheme[21], which detects and cancels the combined memory cell error but with virtually no detriment to any other performance. The cell is termed an S^2I memory cell.

4.6.1 S^2I Design Technique and S^2I Integrator

The basic S^2I memory cell arrangement together with clock waveforms is shown in Fig.4-34. It has a "Coarse Step" in which an input sample is memorised, and a "Fine Step" in which the error current is sampled. The principle advantage of this technique is that it uses a single PMOS device to sense and subtract the error, as opposed to two additional NMOS devices employed in other schemes. The basic idea is that the coarse memory samples the input in phase ϕ_{1a} whilst M_2 provides the bias. The difference between the input and the memorised input (i.e. the error) is then sampled by fine memory M_2 during ϕ_{1b}. The input is then disconnected and the output current is formed by the difference in current between the two memories, which to a first order will be identical to the input current since the error has been subtracted. Since M_2 only handles the error currents, the cell produces an effective "virtual earth" at its input that reduces conductance errors and signal dependent charge injection errors. The inherent simplicity of this switched-current memory cell holds the promise of considerably highly performance and bandwidth.

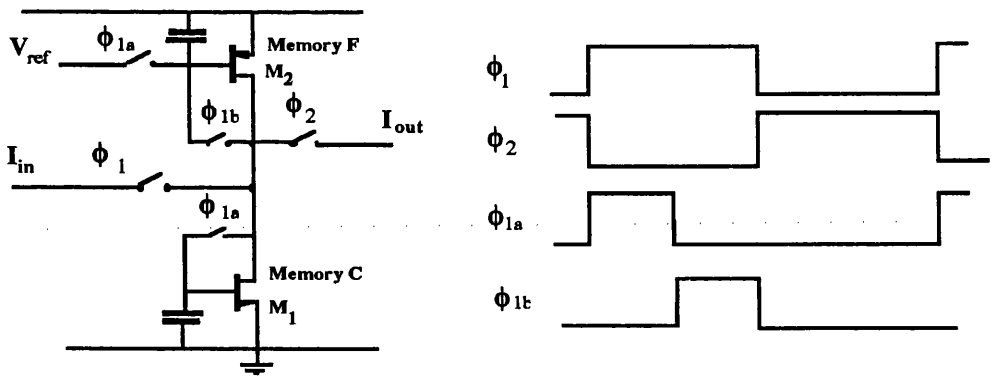


Fig.4-34 The S^2I memory cell

With the introduction of S^2I memory cell, a new bilinear z-transform integrator can be proposed[21]. Several switched-current bilinear z-transform integrators have already been proposed[9,10], and all employ single-ended circuits and require current mirrors to produce signal inversion. These mirrors introduce excess phase errors and, to keep these small, the clock frequency must be made large compared with the filter cut-off frequency, thereby losing one of the major advantages of

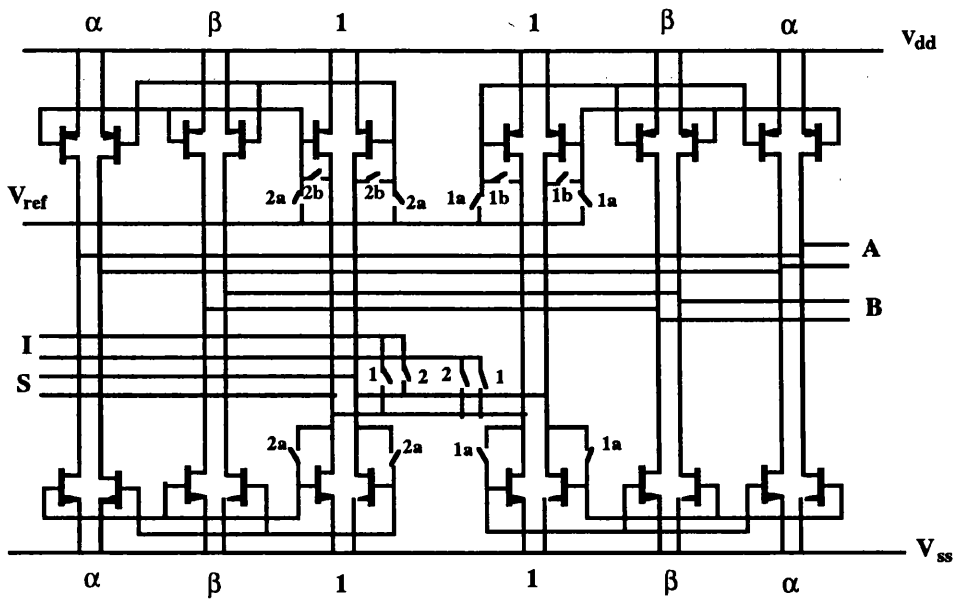
bilinear mapping. In [21], Hughes and Moulding propose an SI integrator/summer building block which performs bilinear z-transformation without excess phase error. It employs balanced circuit structures and features double sampling that effectively doubles the available bandwidth. A fully differential version of integrator/summer is shown in Fig.4-35 together with the clock waveforms. The transfer functions of the circuit are

$$H_A(z) = \alpha \frac{1+z^{-1}}{1-z^{-1}} \tag{4-38}$$

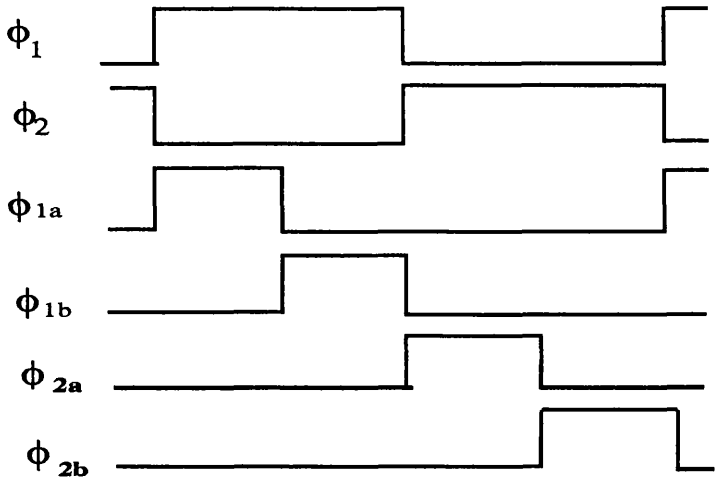
when the output is from terminal A and input from terminal I, and

$$H_B(z) = \beta \tag{4-39}$$

when the output is from terminal B and input from terminal S. The output at node A is giving integration with bilinear z-transformation while the output at node B is giving simple amplification.



(a)



(b)

Fig.4-35 A bilinear z-transform S^2I integrator

A number of existing SFG based SI filter designs can be readily adapted to use the S^2I integrator. However, for the matrix based SI ladder design approach, a new derivation is needed.

4.6.2 Left Matrix Decomposition

As before, we start from the standard nodal admittance matrix equation for prototype ladder filter

$$\mathbf{J} = (\mathbf{G}+s\mathbf{C}+s^{-1}\Gamma)\mathbf{I} \tag{4-40}$$

Equation (4-40) represents a set of equations of second order in the Laplacian variable s. It is well known that a set of linear first order algebraic equations can represent a signal flow graph and be realised by active building blocks. The new SI matrix method enables direct decomposition of the second order matrix to give two inter-related first order equations, and these first order systems are then directly implemented using the S^2I integrator building blocks.

The C and Γ matrices are candidates for decomposition and when matrix C is under attention this leads to the left decompositions and similarly for Γ the right decompositions result.

Factorise the C into

$$\mathbf{C} = \mathbf{C}_l \mathbf{C}_r \tag{4-41}$$

The following pair of equations is equivalent to (4-40)

$$(s^{-1}\Gamma + \mathbf{G})\,\mathbf{I} + \mathbf{C}_l\mathbf{W} = \mathbf{J} \tag{4-42a}$$

$$\mathbf{C}_r\,\mathbf{I} - s^{-1}\mathbf{W} = \mathbf{0} \tag{4-42b}$$

where **W** is the vector of intermediate variables. This decomposition is called *SI Left Decomposition*. The actual methods employed to perform the decomposition indicated in equation (4-41) are those commonly known to preserve the sparsity of the matrices: **LU**, **UL** and the direct methods that decompose any matrix **A** into $\mathbf{AI}_u$ or $\mathbf{I}_u\mathbf{A}$.

By performing bilinear z-transformation, the equations (4-42a,b) can be further represented as

$$[T*H_A(z)/2*\Gamma + \mathbf{G}]\,\mathbf{I} + \mathbf{C}_l\mathbf{W} = \mathbf{J} \tag{4-43a}$$

$$\mathbf{C}_r\,\mathbf{I} - T*H_A(z)/2*\mathbf{W} = \mathbf{0} \tag{4-43b}$$

Each equation in (4-43) can be realised by a first-order SI building block. In these equations the matrix multiplied by s^{-1} or $H_A(z)$ is called integrated matrix and it will be observed that in the SI circuit realisation, the entries in the integrated matrices are

realised by α branch in S^2I integrator and the entries in non-integrated matrices are identified with β branches in S^2I integrator. To explain the proposed approach, a 3rd-order lowpass filter design is considered. The passive ladder structure is shown in Fig.4-36. Following the procedures of the Left-LU design approach, and after the decomposition of matrix, the system SFG derived from the equations can be obtained as in Fig.4-37. The circuit schematic diagram obtained from SFG is shown in Fig.4-38. The circuit realisation has 4 integrators, 9 α type branches, and 2 β type branches. In practical design, no SFG is needed, the SI circuit can be directly achieved from matrix equations.

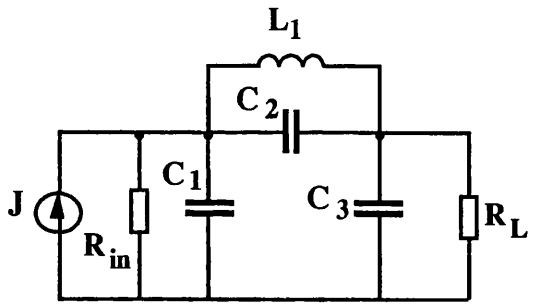


Fig.4-36 Third order SI lowpass filter

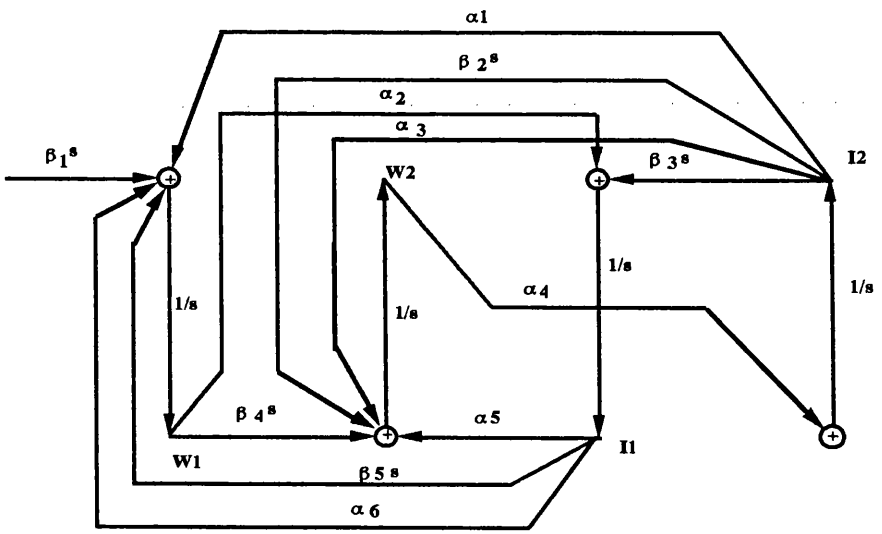


Fig.4-37 Left-LU Signal flow graph of lowpass filter

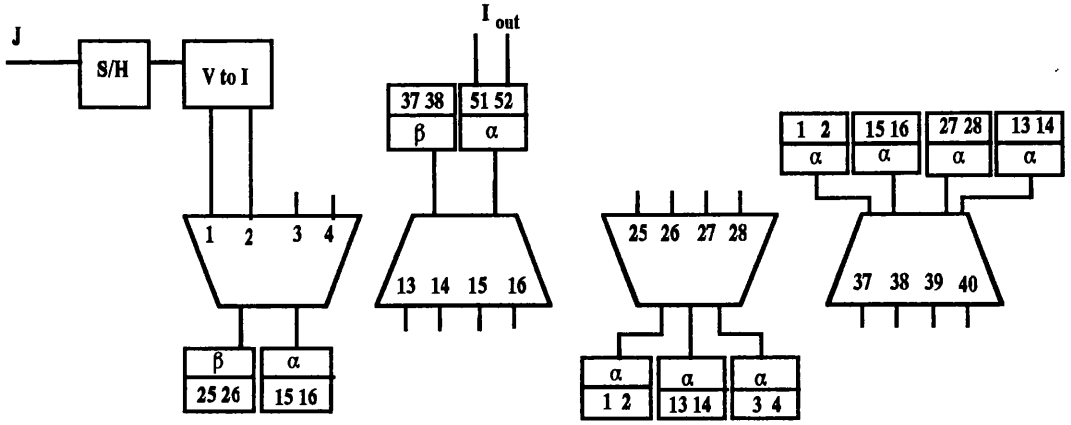


Fig.4-38 Left-LU circuit schematic diagram of SI lowpass filter

4.6.3 Right Matrix Decomposition

If Γ is factorised as

$$\Gamma = \Gamma_l \Gamma_r \tag{4-44}$$

then the *SI Right Decomposition* method is obtained and the following pair of equations is equivalent to (4-40)

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{I} + s^{-1}\Gamma_l \mathbf{W} = s^{-1}\mathbf{J} \tag{4-45a}$$

$$-s^{-1}\Gamma_r \mathbf{I} + \mathbf{W} = \mathbf{0} \tag{4-45b}$$

By performing bilinear z-transformation, the following equations can be obtained.

$$[\mathbf{C} + T*H_A(z)/2*\mathbf{G}]\mathbf{I} + T*H_A(z)/2*\Gamma_l \mathbf{W} = T*H_A(z)/2*\mathbf{J} \tag{4-46a}$$

$$-T*H_A(z)/2*\Gamma_r \mathbf{I} + \mathbf{W} = \mathbf{0} \tag{4-46b}$$

By applying a Right-UL decomposition to same example in Fig.4-36, a SFG can be derived as in Fig.4-39 and the system realisation schematic diagram is shown in

Fig.4-40. It is shown by comparing Fig.4-37 with Fig.4-39 that different matrix decompositions can yield different circuit structure with different costs.

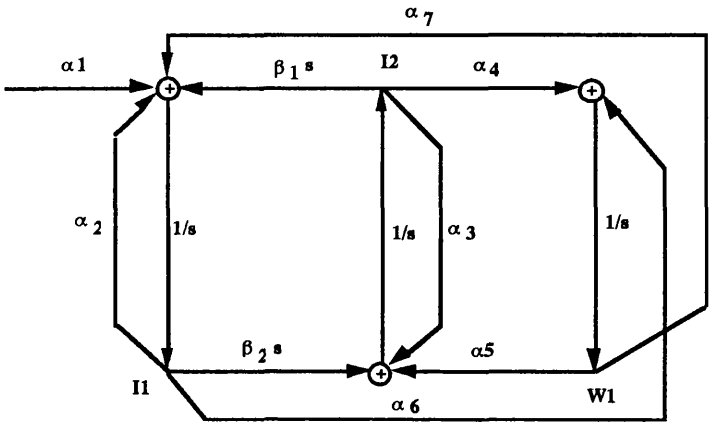


Fig.4-39 Right-UL signal flow graph of SI lowpass filter

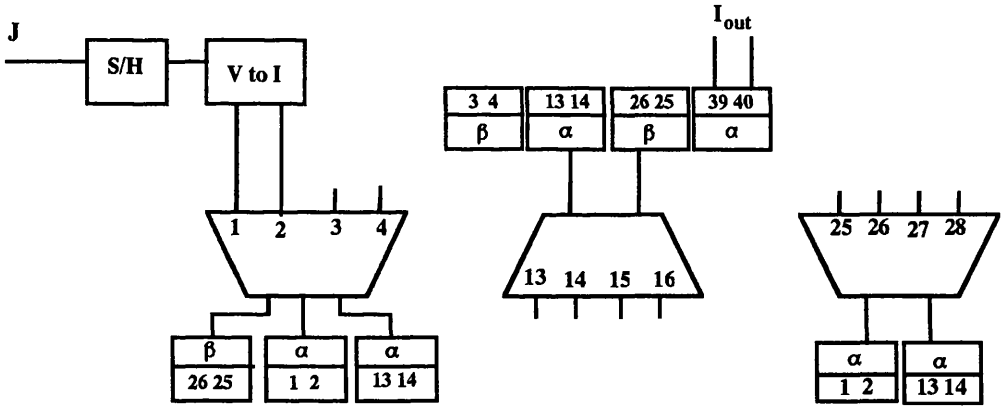


Fig.4-40 Right-UL circuit schematic diagram of SI lowpass filter

Using the proposed approach to design a 10kHz cutoff frequency lowpass filter (passband ripple 1.5dB, stopband attenuation 40dB from 28.5kHz upwards, and a sampling frequency of 100kHz), the design results are given in Table 4-6 and the circuit response is shown in Fig.4-41. From the statistics it can be shown that Right-LU and Right-UL structures achieve best realisations. Fig.4-42(a), (b) and Fig.4-43(a), (b) also give the sensitivity and noise simulation for both S^2I integrator based and second-generation memory cell based approaches. It can be seen that design using S^2I based approach achieves better sensitivity and noise performance.

	No. Int	No. SW	Gm Sum	Gm Spread
Left-LU	4	64	2938.81	31.11
Left-UL	4	64	3145.91	33.07
Left-IA	4	64	2954.10	31.11
Left-AI	4	64	3238.90	34.25
Right-LU	3	48	2340.67	31.11
Right-UL	3	48	2340.67	31.11
Right-IB	4	64	2922.17	31.11
Right-BI	4	64	x	x

Table 4-6. Statistics of S^2I integrator based matrix design methods for SI lowpass filter

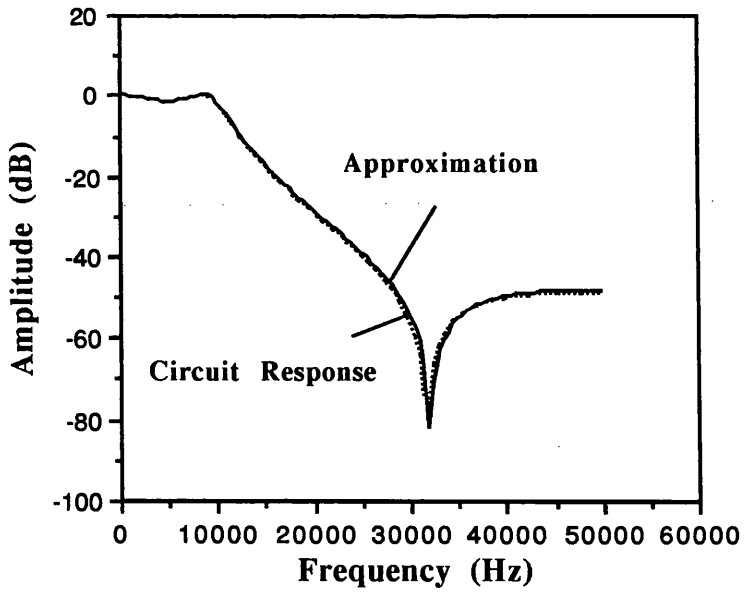


Fig.4-41 A lowpass SI filter

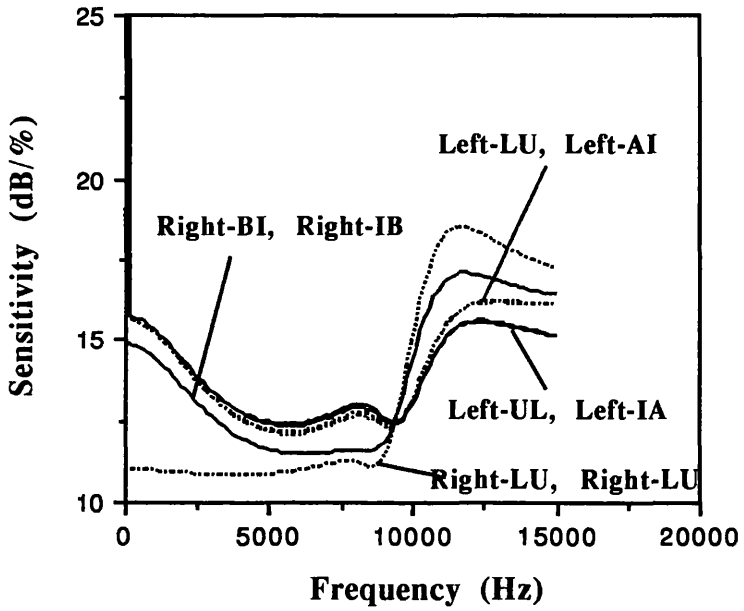


Fig.4-42(a) Sensitivity simulation of S^2I integrator based lowpass filters

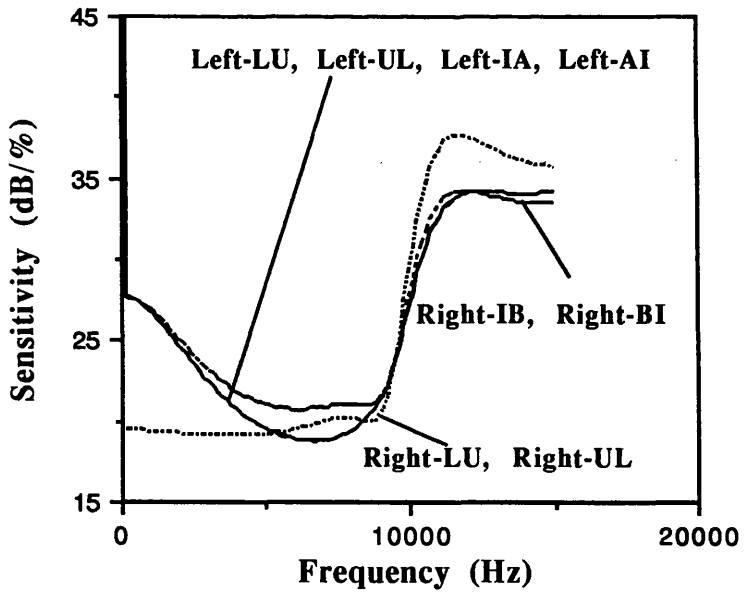


Fig.4-42(b) Sensitivity simulation of second generation memory cell based lowpass filters

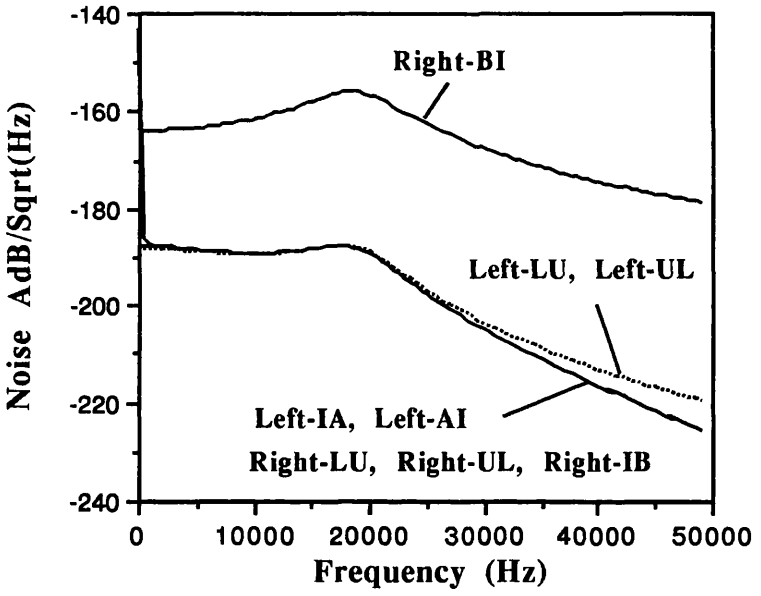


Fig.4-43(a) Noise simulation of S^2I integrator based lowpass filters

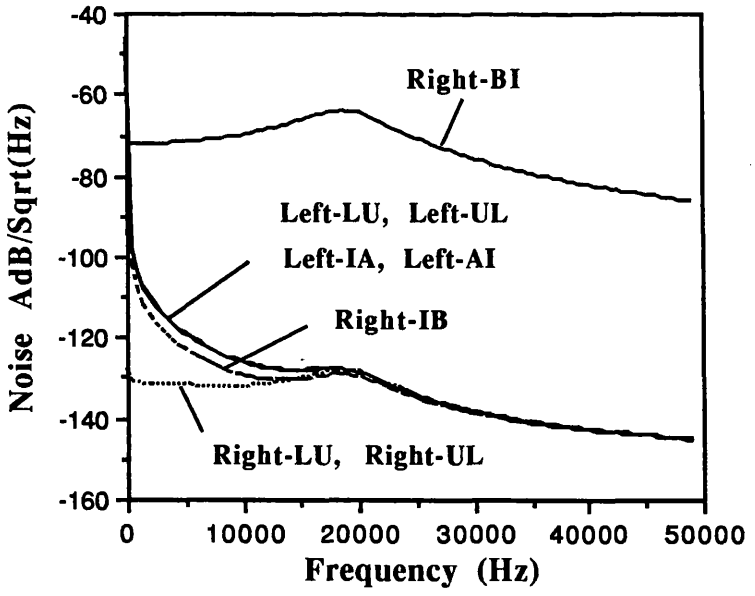


Fig.4-43(b) Noise simulation of second generation memory cell based lowpass filters

4.6.4 Canonical Realisation for Ladder Based Switched-Current Filter

In the design of active-RC and SC ladder filters it is generally assumed that an optimum design contains a minimum number of opamps and similarly a minimum number of transconductors are desirable in transconductor-capacitor filter design. In an SI circuit realisation, it is assumption that one-integrator-per-pole realisations are canonical, which leads to a minimum number of integrators.

In canonical SI realisation, for *Left Decomposition* form, the system (4-42) can be decomposed in the following ways by employing (2-13a,b,c).

$$\mathbf{C}_l\mathbf{W} + (s^{-1}\Gamma + \mathbf{G})\mathbf{I} = s^{-1}\mathbf{J} \tag{4-47a}$$

$$-s^{-1}\mathbf{W} + \mathbf{C}_r\mathbf{I} = \mathbf{0} \tag{4-47b}$$

$$\mathbf{C}_l\mathbf{W} + (s^{-1}\Gamma + \mathbf{G})\mathbf{I} = \mathbf{0} \tag{4-47c}$$

$$-s^{-1}\mathbf{W} + \mathbf{C}_r\mathbf{I} = \mathbf{C}_l^{-1}\mathbf{J} \tag{4-47d}$$

$$\mathbf{C}_l\mathbf{W}+(s^{-1}\Gamma+\mathbf{G})\mathbf{I}=\omega_i^2 s^{-1}\mathbf{J} \tag{4-47e}$$

$$-s^{-1}\mathbf{W}+\mathbf{C}_r\mathbf{I}=\mathbf{C}_l^{-1}\mathbf{J} \tag{4-47f}$$

Now canonical SI networks can be obtained directly from equations (4-47). These circuits use n S^2I integrators, where n is the order of original transfer function H(s). The different parity arrangements and decompositions available lead to different circuit realisation efficiency. Eq.(4-47a,b) produce the same topological structure as the original one, the only difference is that the input at terminals I in Fig.4-35a are changed to terminals S. Analysis of Eq.(4-47c,d) and (4-47e,f) shows that canonical realisation generally leads to the introduction of extra current mirrors. However, if UL or IA decompositions are used, the number of current mirrors can be minimised.

For these two decompositions, only the input terminals are changed in case Eq.(4-47c,d) or one additional current mirror is added in case (4-47e,f). If other decompositions are used, they can introduce up to N (number of nodes in prototype ladder) extra current mirrors.

For *Right Decomposition*, the canonical systems take the form

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{I} + s^{-1}\Gamma_l\mathbf{W} = \mathbf{0} \tag{4-48a}$$

$$-s^{-1}\Gamma_r\mathbf{I} + \mathbf{W} = -s^{-1}\Gamma_l^{-1}\mathbf{J} \tag{4-48b}$$

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{I} + s^{-1}\Gamma_l\mathbf{W} = \mathbf{J} \tag{4-48c}$$

$$-s^{-1}\Gamma_r\mathbf{I} + \mathbf{W} = \mathbf{0} \tag{4-48d}$$

$$(\mathbf{C} + s^{-1}\mathbf{G})\mathbf{I} + s^{-1}\Gamma_l\mathbf{W} = \mathbf{J} \tag{4-48e}$$

$$-s^{-1}\Gamma_r\mathbf{I} + \mathbf{W} = -s^{-1}\Gamma_l^{-1}\omega_i^2\mathbf{J} \tag{4-48f}$$

Eq.(4-48c,d) demonstrates a very efficient canonical form with input terminals changed from I to S. The equations of (4-48a,b) and (4-48e,f) shows that canonical realisation can be realised at the cost of introducing N current mirrors. If UL or IA decompositions are used, very efficient realisations can be achieved, since $\Gamma_l^{-1}\mathbf{J}$ produces a vector with only one non-zero entry, which can be produced by one current mirror only.

4.7 SWITCHED-CURRENT EQUALISER DESIGN

Because of the inherent high speed operation of SI circuits, these is a natural application to video frequency work. In video applications, often group delay equalisation is as demanding as any filtering requirement.

Again two approaches can be used in SI equaliser realisation, a cascade design and a ladder based technique. For a cascade design, the method presented in Section 4.2 can be used. For a ladder based approach, a similar strategy to that used in Section 3.4 can be adopted. The block diagram of an SI ladder based equaliser structure is given Fig.4-44, where Y(s) is realised by a ladder prototype and then be replaced by an SI equivalent realisation using the matrix decomposition methods developed in Section 4.3 or Section 4.6. In this section, two examples of filters and equalisers are given, and some useful conclusions can be drawn.

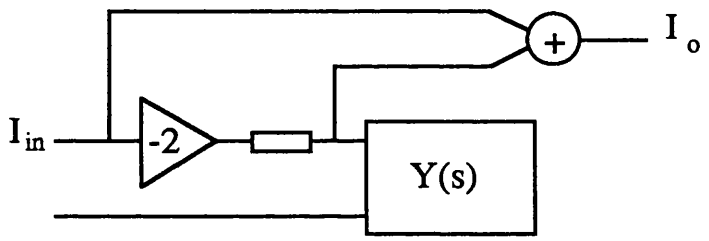


Fig.4-44 Ladder Based SI Equaliser Structure

The first example is a lowpass filter together with equaliser design. The filter is a 5th-order elliptic lowpass with cutoff frequency 2MHz, passband ripple 0.5dB and stopband attenuation 50dB. The sampling frequency of the circuit is 20MHz. By using Right-UL decomposition, a SI filter is obtained. The simulated circuit response is shown in Fig.4-45 and the schematic representation of circuit is shown in Fig.4-46. Sensitivity simulation and noise simulation results of ladder based and cascade realisations are given in Fig.4-47 and Fig.4-48. It obviously shows that ladder based SI filter has a better sensitivity and noise performances than the cascade realisation. The filter has the passband group delay variation 0.7us, whereas the original specifications require a maximum variation of 0.3us for the overall system. A 6th-order equaliser is designed to effect a reduction in group delay variation. Fig.4-49 gives the system group delay responses. The corrected response is the group delay which is formed by combination of filter group delay and equaliser delay together. Table 4-7 gives different equaliser design results, Cascade

I uses an integrator based design method and Cascade II a differentiator based method. The schematic representation of SI ladder based equaliser is shown in Fig.4-50. The Right-IB decomposition method, which in this case is the most efficient realisation of the ladder structures, will need 8 integrators, 24 switches, gm spread 19.40 and gm sum 414.39. If cascade approach is used, a circuit of 6 integrators, 23 switches, gm spread 7.26 and gm sum 96.02 can be obtained. Sensitivity and noise simulation results of Right-IB ladder design and Cascade I realisations are given in Fig.4-51 and Fig.4-52 respectively. It can be seen that the ladder based structure is slightly better than the cascade structure in sensitivity performance, while cascade structure has a significantly better noise performance. For the sensitivity simulations of the SI filter and equaliser, it is interesting to notice that the sensitivity characteristics of SI filter and equaliser designed here bear some similarity with those of a transconductor-capacitor filter and equaliser in Section 3.5.

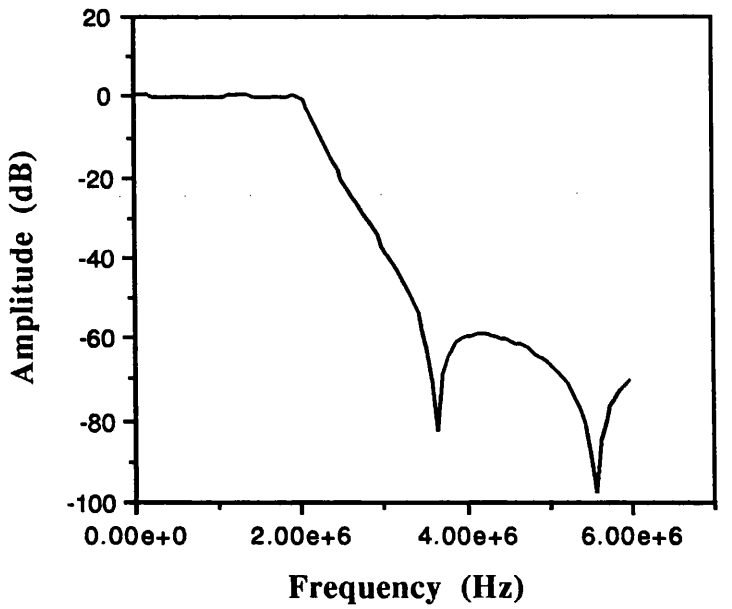


Fig.4-45 5th-order Elliptic Lowpass SI Video Filter

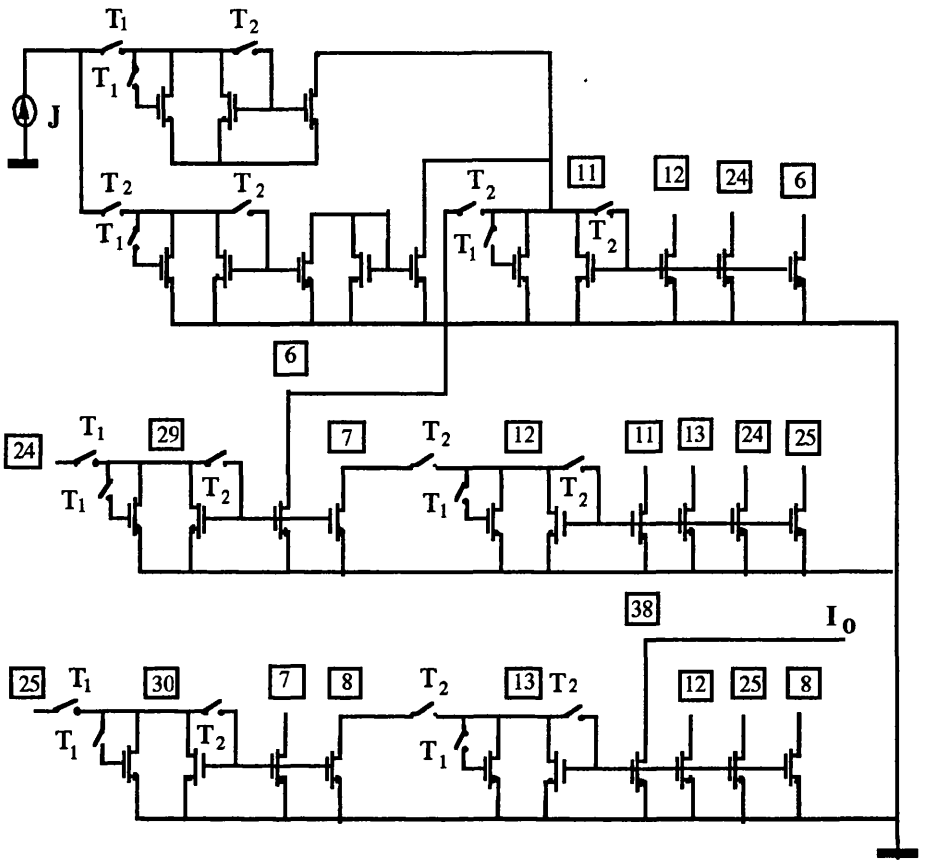


Fig.4-46 Schematic Representation of SI 5th-Order Lowpass Filter

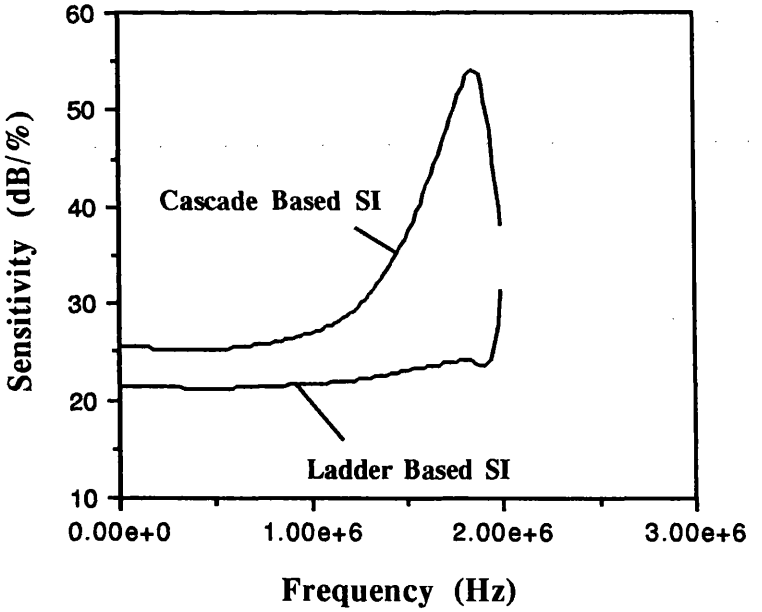


Fig.4-47 Sensitivity Simulation of 5th-order SI Lowpass Filter

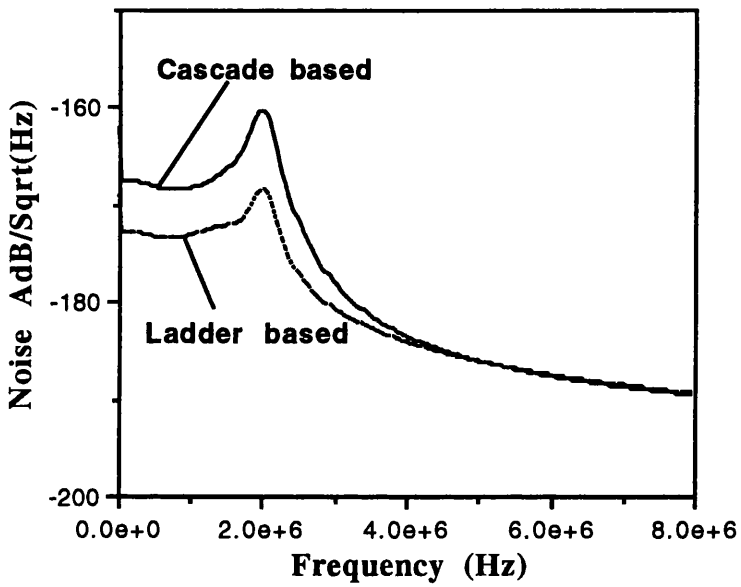


Fig.4-48 Noise Simulation of SI 5th-Order Lowpass Filter

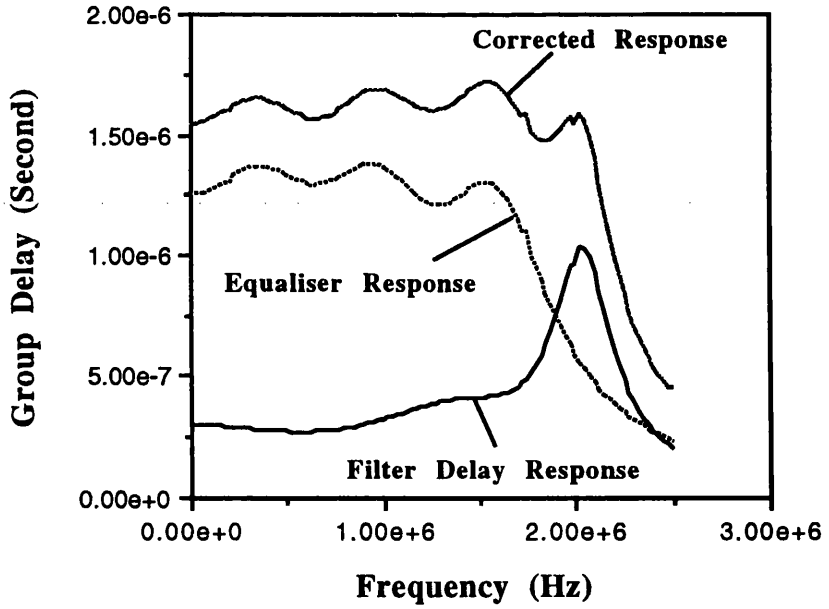


Fig.4-49 Group Delay Response of the SI Equaliser

	Integrator	Switches	g_m Sum	g_m Spread
Left-LU	6	22	661.96	35.75
Left-UL	6	22	450.48	19.40
Left_IA	6	22	450.48	19.40
Left-AI	6	22	661.96	35.75
Right-LU	8	24	1270.33	61.05
Right-UL	8	24	428.75	21.80
Right-IB	8	24	414.39	19.40
Right-BI	8	24	695.21	35.75
Cascade I	6	23	96.02	7.26
Cascade II	6	26	803.81	207.50

Table 4-7 Statistics of SI Equaliser Designs

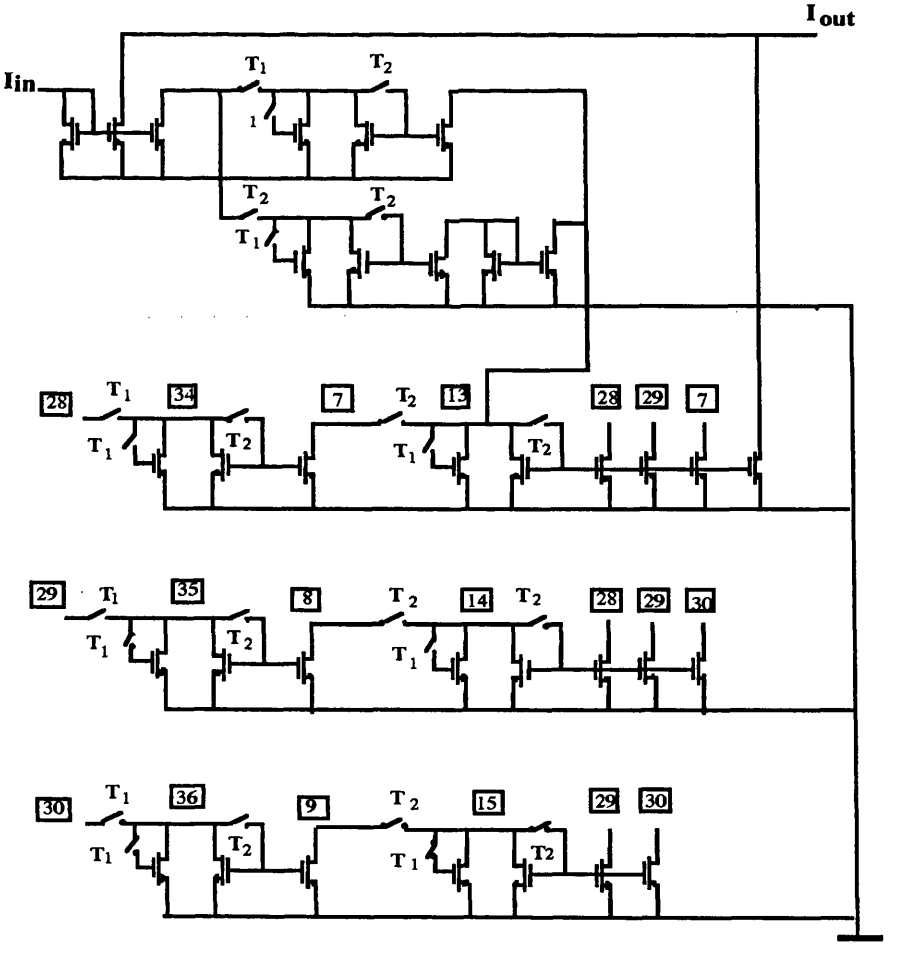


Fig.4-50 Schematic Representation of SI Equaliser Designed by Right-IB Method

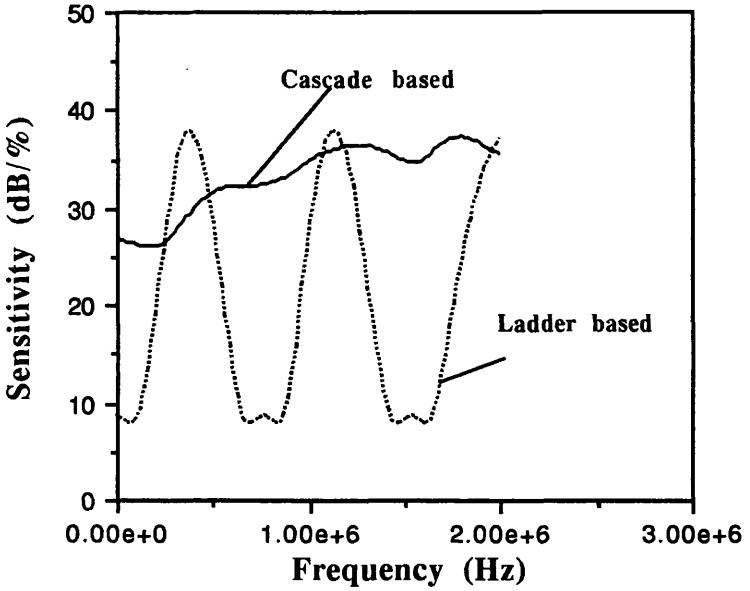


Fig.4-51 Sensitivity Simulation of SI Equaliser for Lowpass Filter

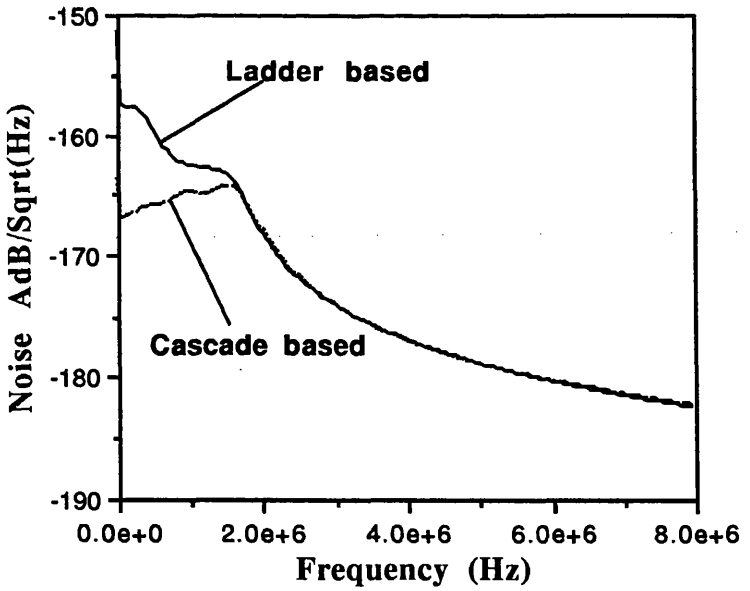


Fig.4-52 Noise Simulation of SI Equaliser for SI Lowpass Filter

The second example is a 6th-order Elliptic bandpass filter. The filter has 0.5dB passband ripple with passband extending from 4.25MHz to 6.8MHz, 20dB stopband

attenuation and sampling frequency of 72MHz. The simulated Left-LU circuit response is shown in Fig.4-53. The sensitivity simulation results compared with Cascade I realisation are presented in Fig.4-54. Again it is apparent that the ladder approach has much lower sensitivity than that of cascade approach, especially at the passband edge frequencies. In Fig.4-55, the noise responses are given and it is shown that ladder based filter structure also has a better noise performance. The filter has a passband group delay variation of 0.6us, and the original specifications require a maximum variation of 0.15us for the overall system. A 14th-order equaliser is designed to perform a reduction in group delay variation. Fig.4-56 gives the system group delay responses. Table 4-8 presents the statistics for a number of different designs, and it can be seen that the cascade SI equaliser structure realises a far more efficient circuit in terms of gm spread and gm sum. Sensitivity simulation results of ladder with left-LU decomposition and cascade I realisations are given in Fig.4-57 and it is shown that circuit structure derived from Cascade I approach has a relatively high sensitivity in passband. But the ladder structure has a very poor noise performance as shown in Fig.4-58.

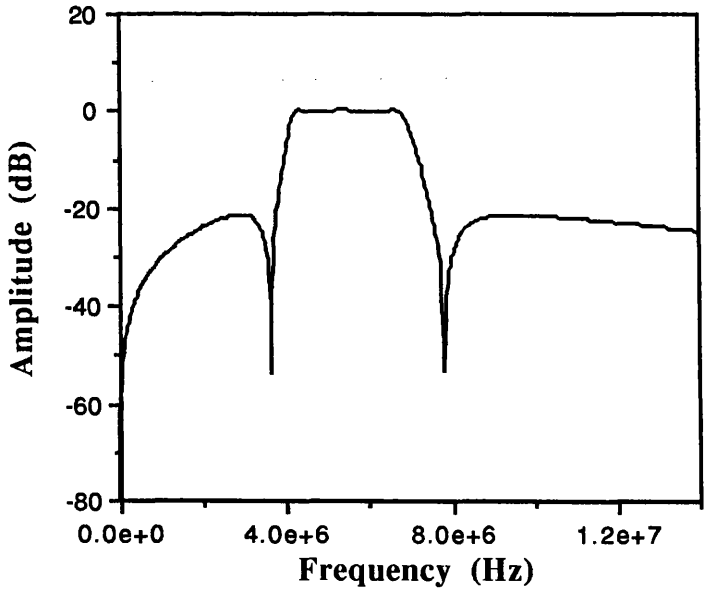


Fig.4-53 6th-order Bandpass SI Filter Response

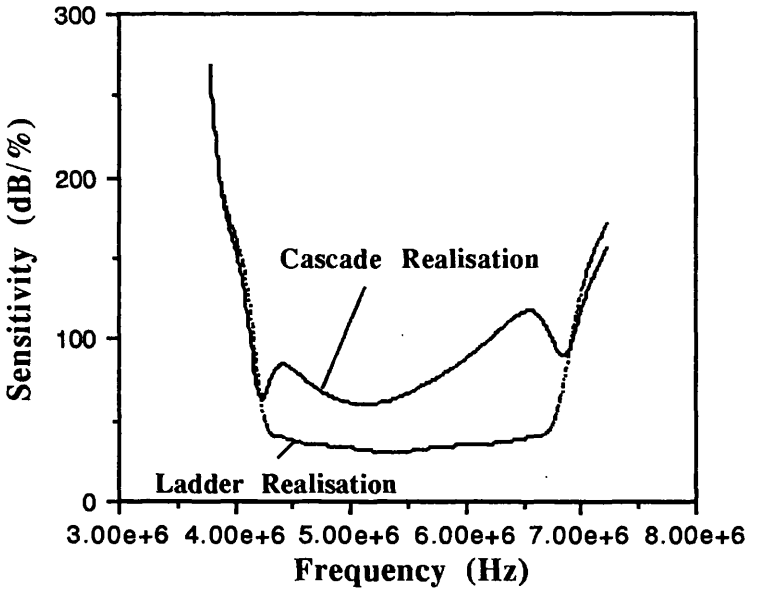


Fig.4-54 Sensitivity Simulation of the SI Bandpass Filter

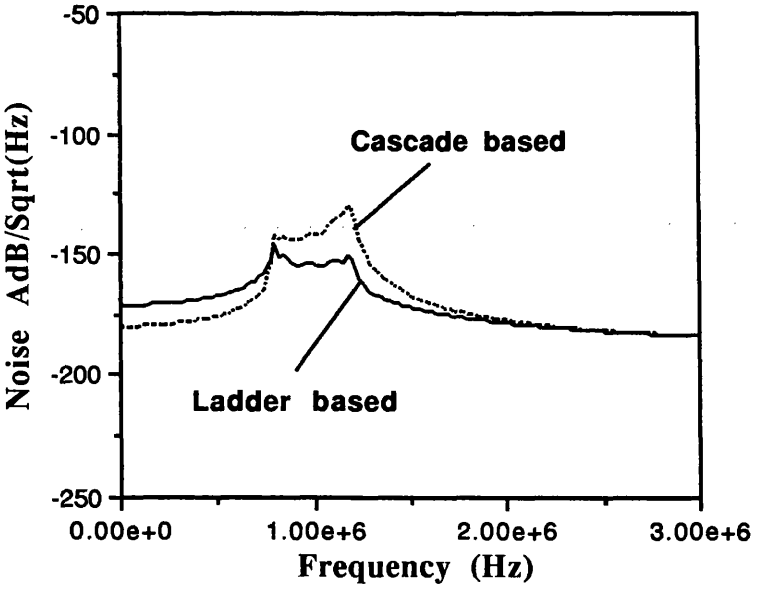


Fig.4-55 Noise Simulation of the SI Bandpass Filter

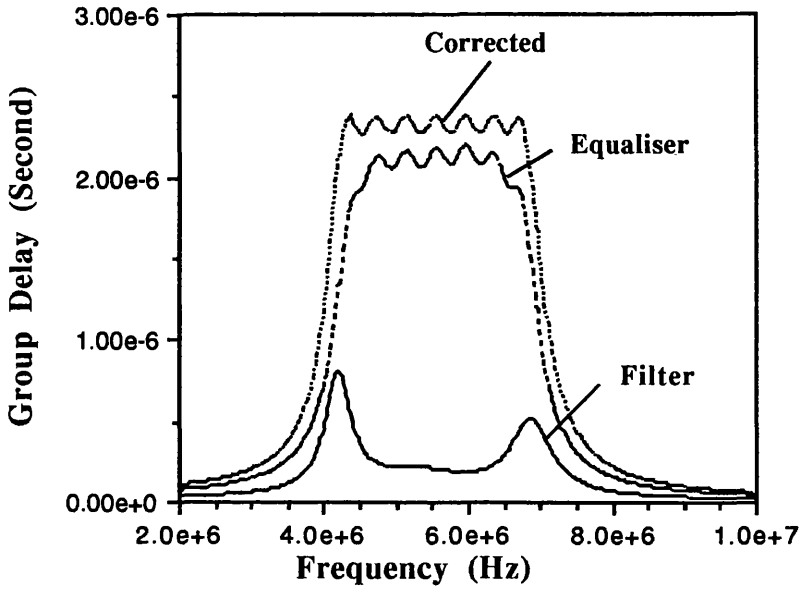


Fig.4-56 14th-order Equaliser Group Delay Response

	Integrator	Switches	g_m Sum	g_m Spread
Left-LU	14	46	13810.02	452.19
Left-UL	14	46	X	X
Left-IA	14	46	X	X
Left-AI	14	46	13810.02	452.19
Right-LU	16	48	16545.03	452.19
Right-UL	16	48	X	X
Right-IB	16	48	X	X
Right-BI	16	48	14524.87	452.19
Cascade I	14	51	777.44	22.38
Cascade II	14	58	2492.36	158.42

Table 4-8. Comparative design results of 14th-order equalisers

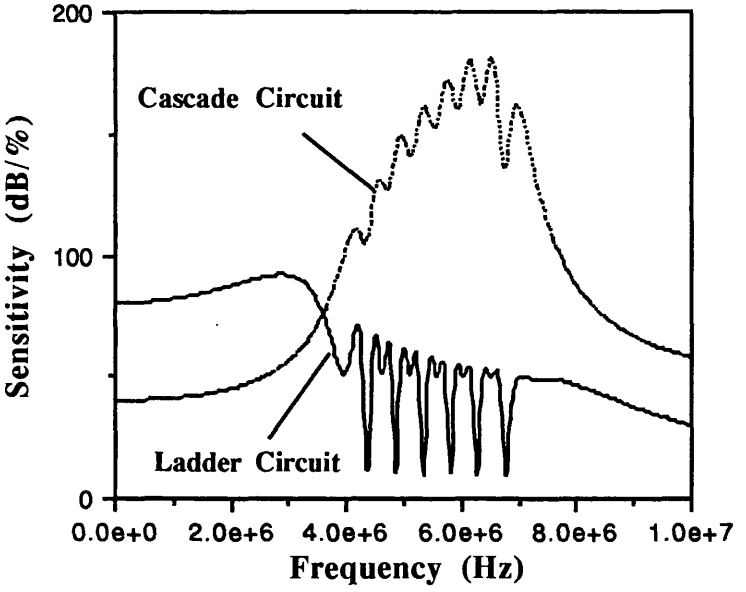


Fig.4-57 Sensitivity Simulation of SI Equalisers

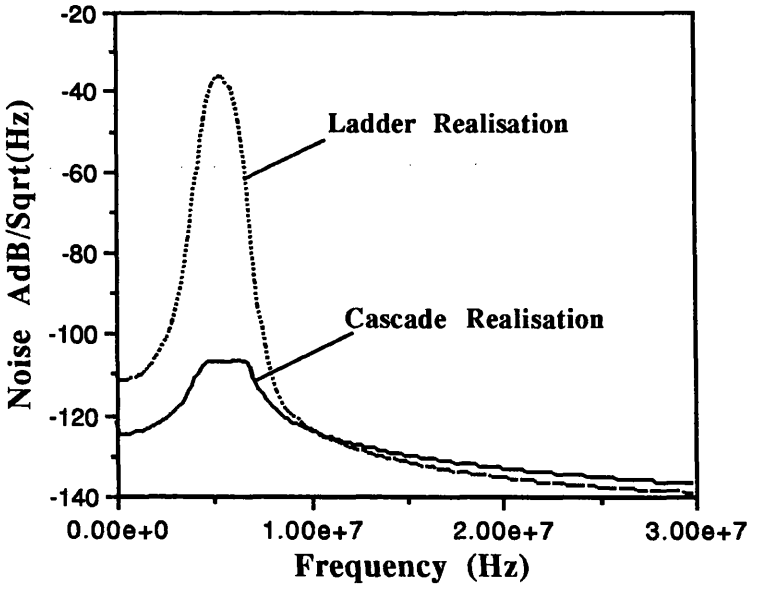


Fig.4-58 Noise Simulation of SI Equaliser for SI Bandpass Filter

It would seem that in general the ladder based designs produce better SI filters, whereas the cascade designs show more cost efficient circuits and better noise performances for SI equalisers, though at some penalty of increased sensitivity.

4.8 MULTIRATE SWITCHED-CURRENT SYSTEM DESIGN

Multirate system design techniques are used extensively in digital and switched-capacitor systems to achieve better performance than those obtained by using a single rate system. Since a switched-current system is also of a sample-data nature, the multirate design technique can also be used. There are very few papers on multirate switched-current system design[24,25]. In this section, we show two SI examples designed by two different multirate approaches. The results demonstrate that improvement in some performance parameters can be obtained.

4.8.1 Switched-Current Narrow Band Filter Design

As in narrow bandpass SC filter design, narrow bandpass SI filter design also encounters the problem of wide gm spread and large gm sum. These would lead to the filter designed being less accurate and having large chip area. Design approaches already developed previously can be used to design cascade based or ladder based narrow bandpass SI filters, however they cannot produce efficient circuit realisations. The first example is a video frequency bandpass filter with specifications of passband from 4.25MHz to 6.8MHz, stopbands from 0.1Hz to 3.75MHz and from 7.25MHz to 60MHz, passband ripple 2dB and stopband attenuation 30dB. Using an Elliptic approximation, an 8th-order filter is realised by cascading four biquads with sampling frequency 72MHz. We take the gm spread and gm sum of the filter as two index in evaluating the accuracy, chip area and power consumption of the circuit. The small spread will maintain an accurate filter response and small sum will lead to a lower power and smaller chip area circuit design. The design results are given in Table 4-9.

In single rate realisation, the total coefficients are 1651.73 and the maximum spread of transistor aspect ratio is 192.78. To reduce the gm spread and gm sum, a multirate multistage structure is adopted as shown in Fig.4-59, where the lowpass filter has a 72MHz sampling frequency and the highpass filter has a sampling frequency of 36MHz. The lowpass filter also has the function of an anti-aliasing filter up to 67MHz. The lowpass filter is realised by a cascaded structure and has gm sum 547.81 units and the maximum gm spread of transistor aspect ratio 26.19. And the highpass filter is implemented by a ladder structure and has the gm sum 437.42 and the maximum spread of transistor aspect ratio 19.79. The overall multirate SI system has the total coefficient 985.23 and the maximum spread of transistor aspect ratio 26.19. By using a multirate design technique the gm sum has reduced by 40.0% and the gm spread has reduced by 86.4%. The multirate system response is shown in Fig.4-60.

	gm Spread	gm Sum
Single Rate	192.78	1651.73
Multirate	26.19	985.23

Table 4-9. SI Filter Design Results

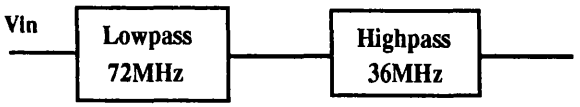


Fig.4-59 Multirate bandpass SI filter system

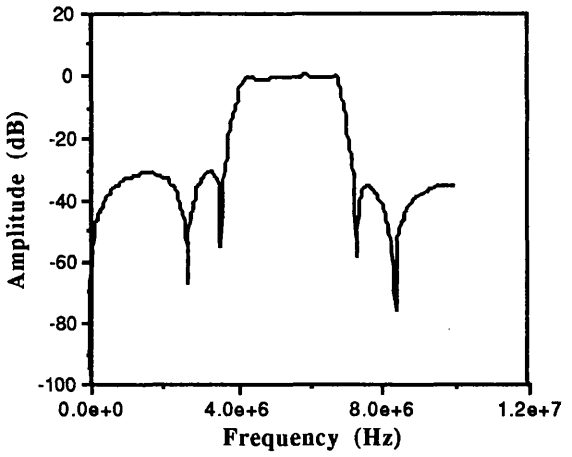


Fig.4-60 SI multirate bandpass filter response

4.8.2 Switched-Current SPFT Filter System Design

It has been already demonstrated that SPFT (Single Path Frequency Translated) is a very efficient technique for very narrow SC filter design[26,27]. The same idea can also be used for very narrow band SI filter design. Consider the design of a very narrow band SI filter with passband from 7.49MHz to 7.51MHz, passband ripple 0.4dB, stopband attenuation 50dB. This specification corresponds to a relative bandwidth B=0.4%. If a single rate filter is designed, the best results that can be achieved give a Gm spread of 608.37 and Gm Sum of 28704.14. Since the Gm spread is too large to ensure an accurate SI circuit realisation, a SPFT system is proposed to accomplish this design. The SPFT system is shown in Fig.4-61 and has five sections. The first and last filter can also be considered as part of decimator and interpolator. The first two and last two sections are realised by a second order cascade structure with 80MHz sampling frequency. The SI bandpass filter in the centre has a passband from 490kHz to 510kHz and sampling frequency 8MHz. The schematic diagram of switched-current SPFT system is shown in Fig.4-62 and the circuit design results in a circuit realisation with Gm spread 45.83 and Gm Sum 2550.38. In comparison with the Gm spread 608.37 in the single rate case, the multirate technique

has achieved significant improvement in circuit realisation. It has changed an unrealisable circuit implementation to a potentially realisable implementation with reasonable Gm spread. The circuit response around midband is shown in Fig.4-63. The global frequency response is given in Fig.4-64, from which it is can be seen that frequency components around 8.5MHz are the closest sideband frequency components to midband 7.5MHz but these are below -50dB. The multirate design also shows much better sensitivity and noise performance, as in Fig.4-65, and Fig.4-66 respectively.

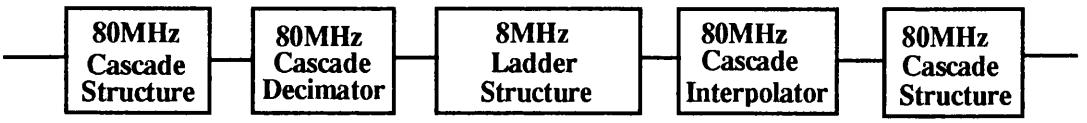


Fig.4-61 SI Multirate SPFT system

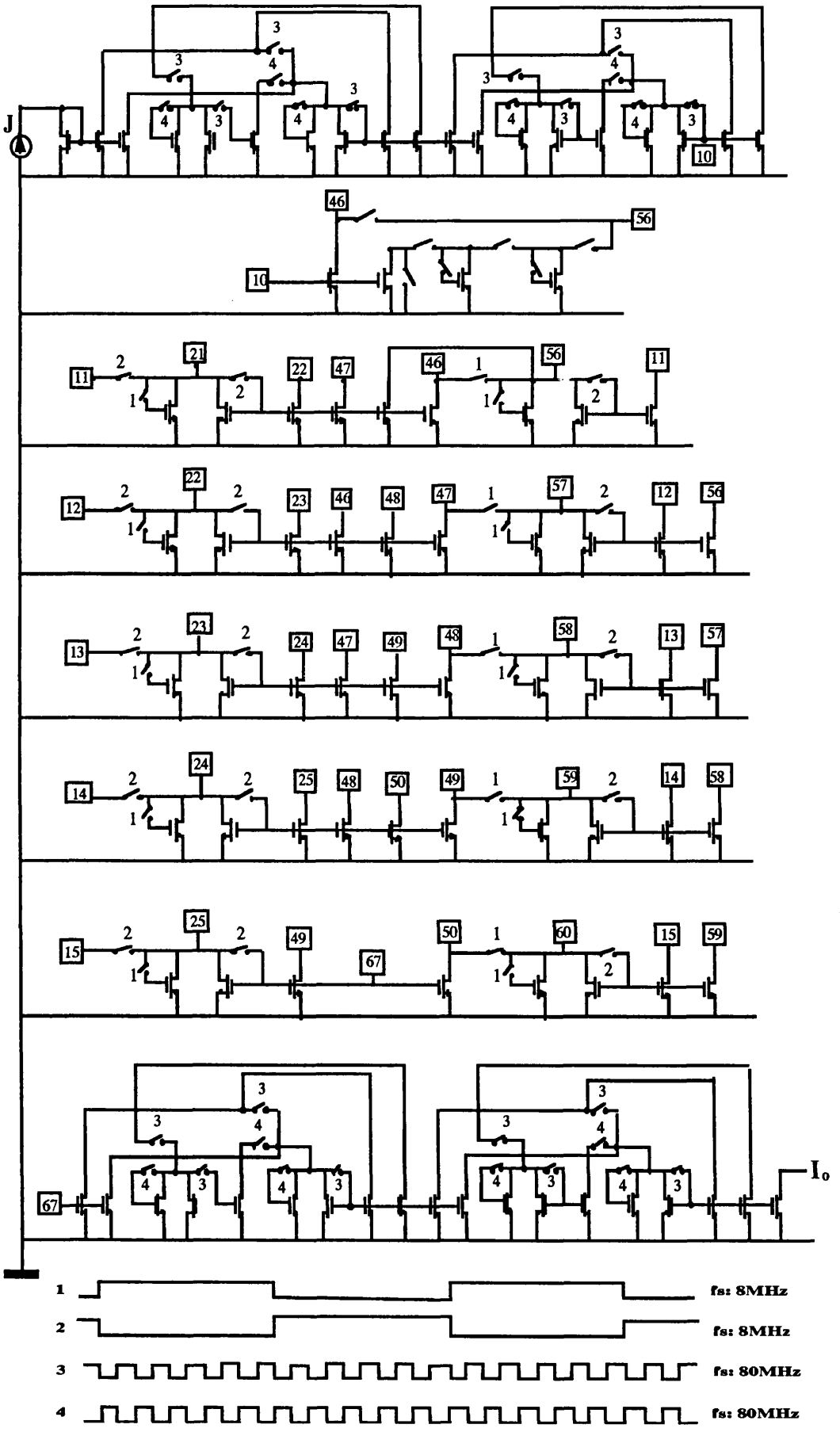


Fig.4-62 Schematic diagram of SI SPFT system

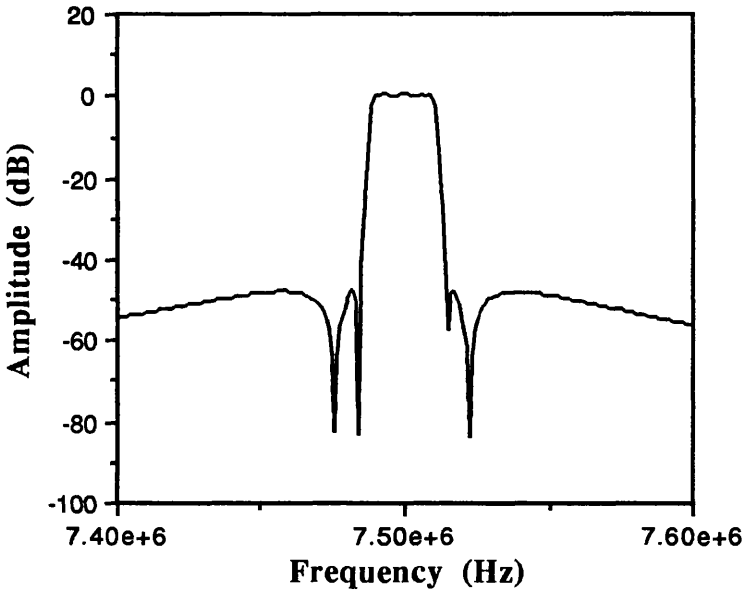


Fig.4-61 Frequency response of SPFT SI narrow-band filter

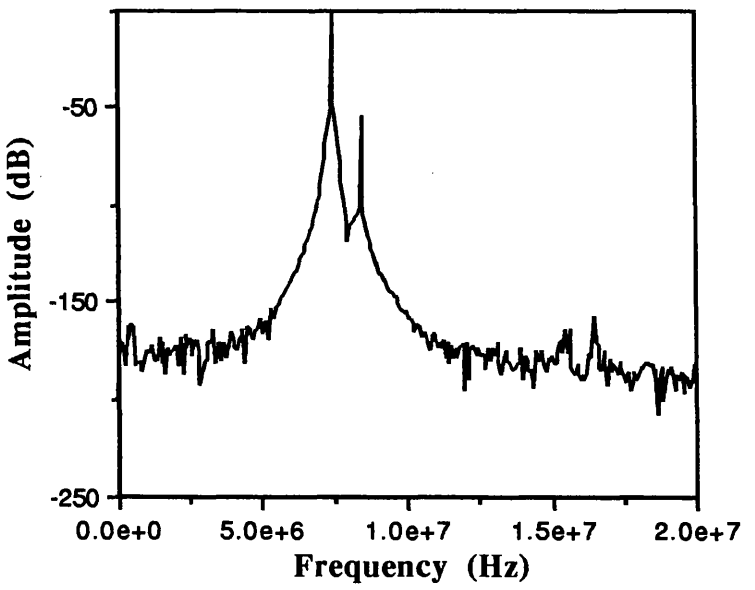


Fig.4-62 Global frequency response of SI narrow bandpass filter

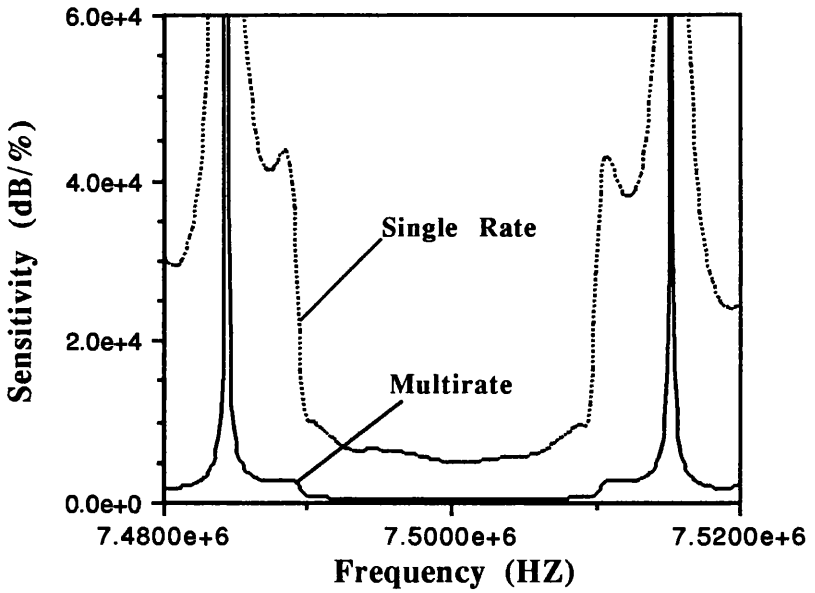


Fig.4-63 Sensitivity simulation of single rate and multirate SI narrow bandpass filter

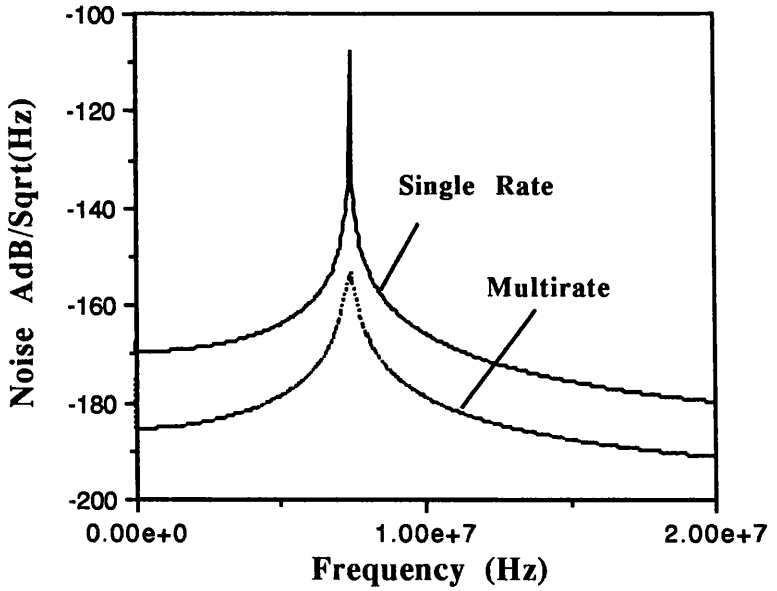


Fig.4-64 Noise simulation of single rate and multirate SI narrow bandpass filter

4.9 SUMMARY

This Chapter has discussed the synthesis and realisation of switched-current filters.

A new approach to realise exact ladder SI filters based on first and second generation memory cell has been presented. The bilinear transformation is used in the design procedures. Eight different types of SI structures can be obtained from one passive prototype ladder . This provides SI filter designers with a choice of different circuits based on different requirement such as area, maximum ratio of transistor aspect ratio, sensitivity or noise performance. Techniques to improve dynamic range and reduce circuit parameter spread are also presented. The proposed approach is well suited for filter compiler implementation and is already realised in XFILT. A suitability study for each decomposition method for different filtering applications has been also carried out and a general guideline for the choice of decomposition method been obtained.

A comparison study on switched-current (SI) filter sensitivity performance based on first generation and second generation cell realisation was carried out. It was demonstrated by four filters examples that SI filters based on a second generation SI cell do have good sensitivity performance. For SI filters based on first generation memory cells, it is shown that a high ratio of clock frequency to cutoff frequency in the lowpass case, or a high ratio of clock frequency to midband frequency in the bandpass case would introduce high sensitivity.

A novel approach for the synthesis of SI ladder filter using S^2I integrators is also proposed and the requirements for canonical realisations are derived.

SI equaliser design has been presented and it appears that a cascade structure is a better candidate for realisation of these circuits.

Finally, multirate SI filter system design was addressed. Two examples were given to show that two different multirate approaches can be used in narrow band filter design and better performance parameters can be obtained.

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Chapter 5: XFILT an X-Window Based Modern Filter and Equaliser Design System

CHAPTER 5: XFILT AN X-WINDOW BASED MODERN FILTER AND EQUALISER DESIGN SYSTEM

5.1.INTRODUCTION

Previous chapters have described the development of a set of computer methods for various filter design techniques: active-RC, SC, SI and transconductor-C. In this chapter, an X-window based modern filter and equaliser design system called XFILT, based on the assembly of proposed methods is presented. The system consists of more than 50,000 lines of C-code and runs on a SUN workstation. XFILT can help the expert designer to be more efficient and to extend his capability, and also it provides automatic synthesis for those without design experience. The system can design passive-RLC, active-RC, SC, transconductor-capacitor, and switched-current filters with classical or arbitrary approximations. Simulation facilities are provided. An optimisation scheme is provided to improve the design. The philosophy of the system is explained and XFILT structure is examined. Major functions and special features of the system are addressed. Circuit design, simulation and system performance optimisation are described. Further details on the usage of the software are given in the XFILT User's Guide[1].

5.2 XFILT Design Philosophy and System Structure

5.2.1 Design Philosophy

The CAD for filters is a relatively well developed area in analogue circuit automation. Several software packages are already available for passive-RLC, active-RC, SC and transconductor-C filter design[2-10]. Unfortunately although more tools are becoming

available, their acceptance by designers is surprisingly low. The reasons are essentially due to the difficulty in using the tools, to their limited capabilities, and to the missing links between the various tools. For these reasons, special attention were given to **Ease of Use, General Applicability** and **Ease of Extension** of the software when XFILT was developed.

The distinguishing features of XFILT are:

1.**Ease of Use**: The system has a user friendly graphical interface. The specification of the filter can be described in terms of numerical parameters or as a graphically displayed template. A graphics editor is provided to enable the user to modify the template freely. The circuit synthesis and simulation are combined into one system. Simulation software SPICE, SCNAP4[11], and SWITCAP[12] can be invoked easily, and no manual tools for linking and transferring data are needed between circuit design and circuit simulation. The requirements of both novice and experienced designers are considered. For the novice designer, automatic synthesis can produce a circuit topology and component values directly from filter specifications, and for the experienced designer, choices are provided during approximation, prototype ladder design and circuit realisation which allow the designers to explore for a more efficient circuit realisation.

2. **General Applicability**: XFILT is a completely general filter and equaliser design system with ability for passive-RLC, active-RC, SC, transconductor-C and SI realisation. It can produce both classical and arbitrary amplitude approximation for filters and arbitrary group delay approximation for equalisers. The optimisation scheme used in XFILT accepts principal non-ideal effects and most types of circuits.

3. **Ease of Extension**: General ladder design methods can be extended to include new filter types. A flexible software structure makes it very easy to add new ladder or

biquad structures. New simulation packages can be readily included. The XFILT can be used in multirate and multistage system design to produce large switched filter networks.

5.2.2 System Structure

The XFILT system structure is shown in Fig.5-1. A graphical interface utilises standard X11[13] and is provided both as a user friendly interface to the designer and as a system manager of all the software in XFILT. The specifications of the filter and equaliser can be read in from menus or existing files. Graphic editing facilities are offered to specify the templates of classical and arbitrary magnitude filters and group-delay equalisers.

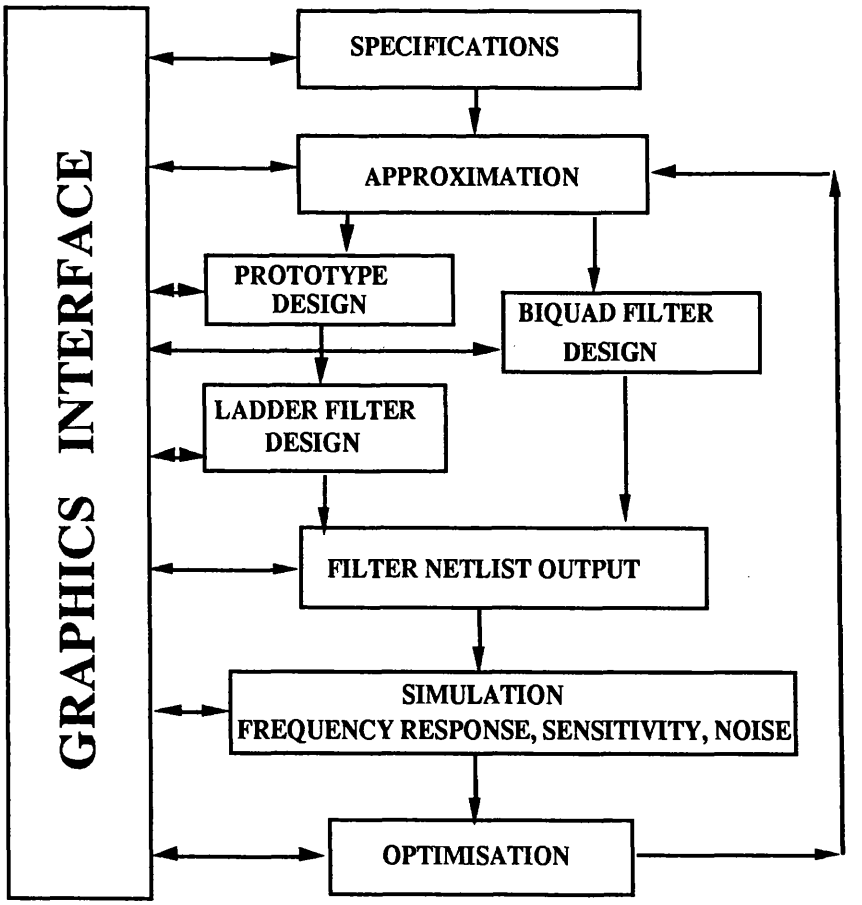


Fig.5-1 XFILT System Structure Block Diagram

Arbitrary passband and stopband response approximations as well as Butterworth, Chebyshev, Inverse-Chebyshev, Elliptic, Bessel and Legendre approximation functions are available. In the arbitrary magnitude design mode, the desired amplitude response of the filter is specified by a pair of piece-wise linear boundaries (a template) of amplitude against frequency. The arbitrary response approximation will attempt to fit a response within the upper and lower boundary[14].

The filter circuit design falls into two structural categories: cascade biquad and passive ladder simulation. The passive ladder simulation requires a passive ladder prototype which can either be synthesised internally or read from an external file. There are four ladder prototype synthesis modes: *expert* for experienced designers whereby complete control is exercised over the classes and sequence of zero removals; *interactive* in which only the sequence of removals is selected, *automatic* when no manual intervention is necessary[15], and *external* in which a predetermined prototype ladder can be read in from a file. The passive prototype can be simulated by a variety of active filter structures depending on the particular implementation required[5]. Filter and equaliser synthesis in active-RC, switched-capacitor, switched-current and transconductor-capacitor form are offered.

Simulation facilities for frequency response, group delay, sensitivity and noise are provided. For passive-RLC, active-RC, and transconductor-C realisations, SPICE is provided as a simulation tool and for SC and SI realisations SCNAP4 or SWITCAP can be used.

A special global optimisation scheme is provided to improve the design. The order of optimisation corresponds to order of the original filter and is not determined by the number of components in the filter circuit.

5.3 XFILT Graphical Interface

The essential feature of the interface is **Ease of Use**. It can provide a menu-driven interface for checking and facilitating the entry of design parameters. The menu-driven interface can avoid incorrect input and remind users of the input required. Graphical display is another characteristic of the interface. The graphs of the approximation function and different circuit responses are given. Besides the graphical display facility, a special feature of the XFILT graphical interface is that it provides a graphical editor. By using the graphical editor the user can specify arbitrary, or classical magnitude and group delay templates with a mouse. The graphical interface is also a software system manager; all the design, simulation and optimisation software is linked by this interface. The graphical interface consists three kernel elements:

1)menu-driven interface
2)text editor
3)graphical editor

The menu-driven interface consists of a set of menus and sub-menus, which are used to select different control commands and to enter the specifications.

The text editor is mainly used as template editor for editing arbitrary approximation magnitude. The editor is easy to use and scroll bars are provided for a large template file. In text editor, the template is entered as a sequence of frequency, lower template and upper template values. In the template editor, four facilities are provided; these are **X-Y definition** function, **show** function, **save** function and **clear** function. **X-Y definition** function is used to define X axis of linear or Log value, and Y axis of linear or dB value. **Show** function is used to display the template. **Save** function is used to save template file and the **clear** function is used to clear the template editor context.

A very flexible graphics editor is provided for the editing of the filter specification graphically. In the classical approximation design mode, the user can employ the mouse to move template lines and change the filter specifications. The software gives the approximation transfer function under the new template immediately and changes menu parameters at the same time. In the arbitrary magnitude and group-delay design mode, the basic graphics editing functions include **Template Point Move, Add Template Points, Add Group Template Points,** and **Clear Template.** A **Zoom** facility is provided to facilitate examination of the transfer function plots in greater detail.

A touch point editor is provided for arbitrary magnitude and/or group-delay approximation. High order touch points[14] in the filter stopband create deep, multiple notches for single frequency rejection, whereas high order touch points in the passband can ease group-delay requirements. In the touch point editor, the touch point sequence, type, order and frequency are specified.

5.4 System Transfer Function Approximation

The system transfer function is obtained by approximation to the specification given. The approximation cycle can produce classical magnitude, arbitrary magnitude and arbitrary group delay transfer functions.

5.4.1 Classical Magnitude Approximation

The available classical magnitude approximation types are Elliptic, Chebyshev, Butterworth, Inverse-Chebyshev, Legendre, and Bessel. In a classical approximation mode, the window would be as shown in Fig.5-2. Assuming that we want to design a lowpass elliptic switched-capacitor filter with specifications:

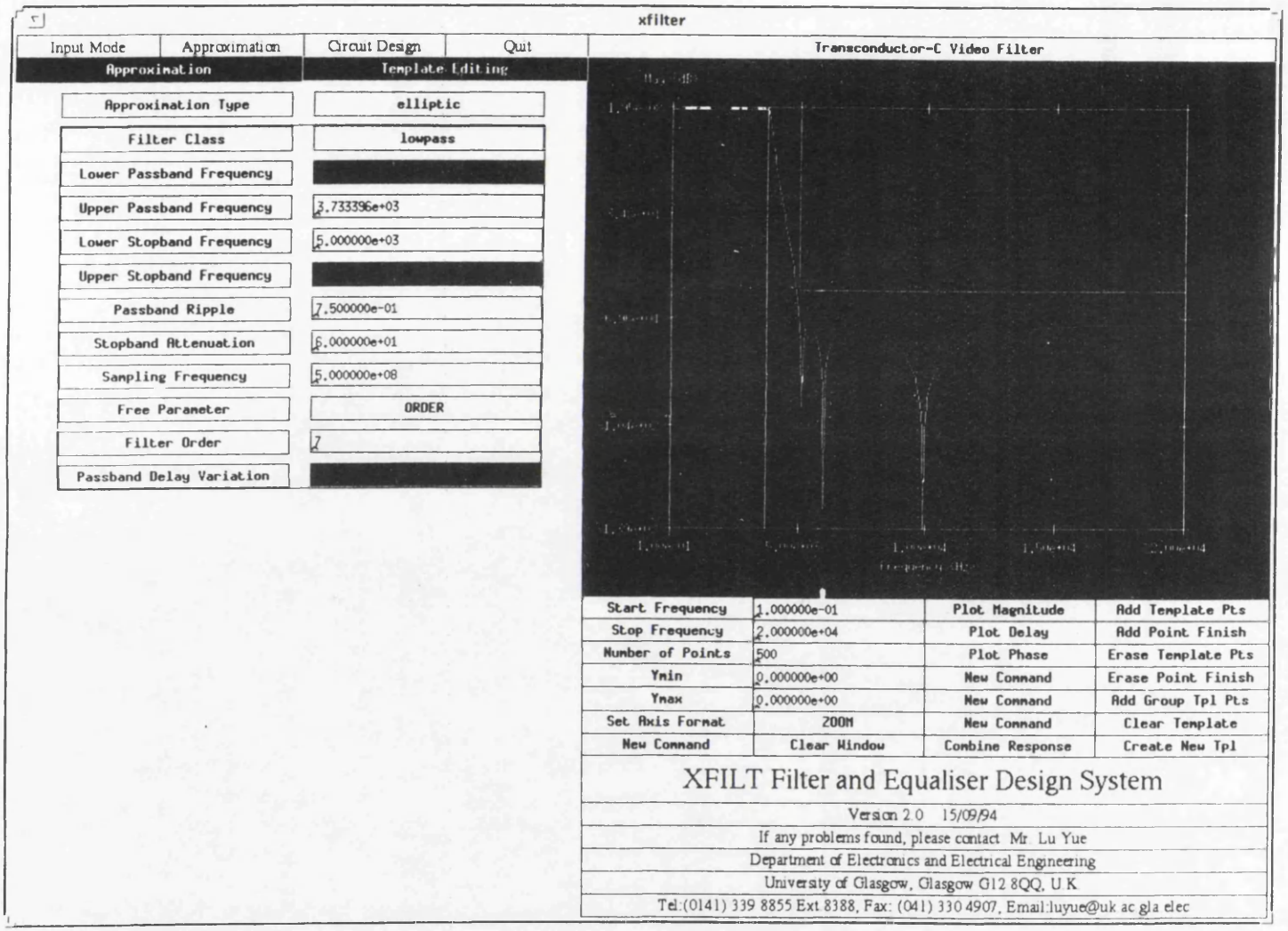


Fig.5-2 Screen shot of XFILT showing an Elliptic lowpass approximation

Passband edge frequency : 3733.396Hz

Stopband edge frequency: 5000.000Hz

Passband ripple: 0.75

Stopband attenuation: 60.00dB

The classical template is shown in Fig.5-3. Fig.5-4 gives all four types (lowpass, bandpass, highpass and bandstop) template definitions.

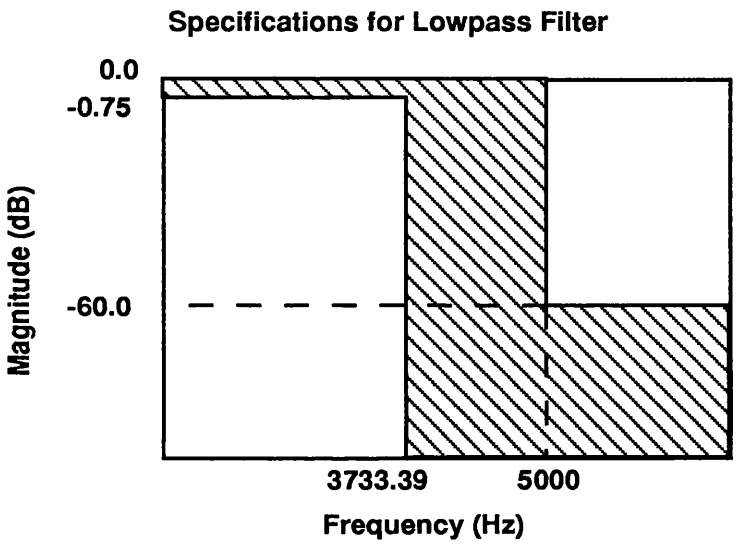


Fig.5-3 Lowpass Filter Specification

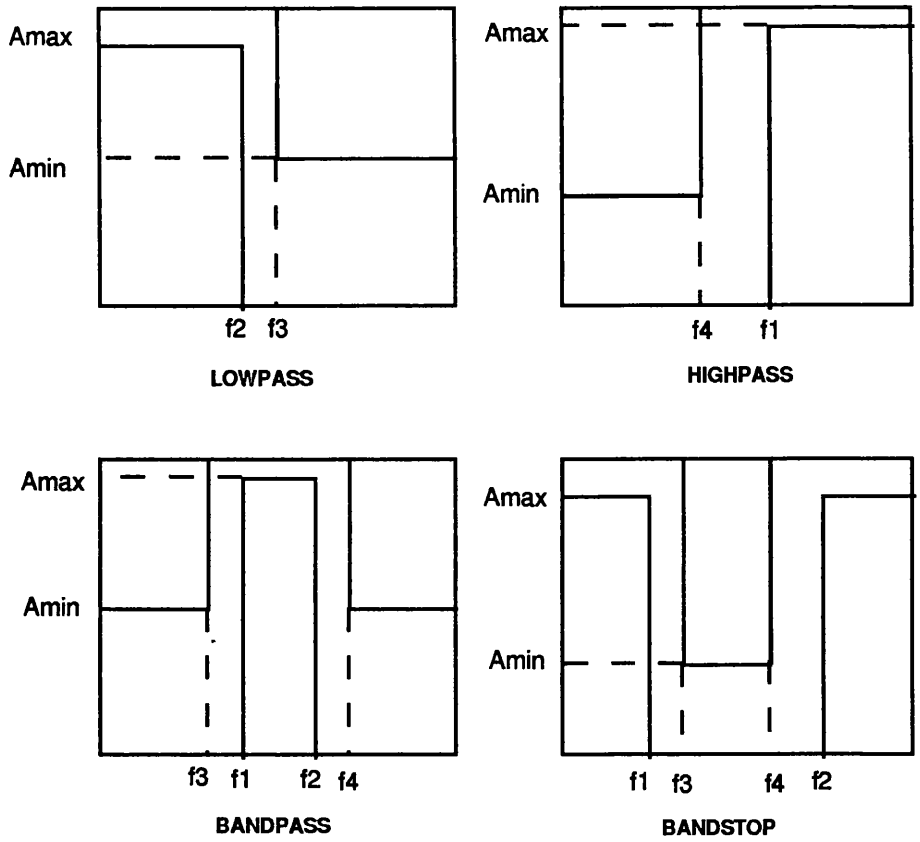


Fig.5-4 Edge Frequencies, passband ripple and stopband attenuation definition

where

f1 = lower passband edge frequency

f2 = upper passband edge frequency

f3 = lower stopband edge frequency

f4 = upper stopband edge frequency

Amax = maximum passband ripple

Amin = minimum stopband attenuation

By using the Template Editing facility, the designer can change the filter edge frequency, passband ripple and stopband attenuation in the graphics window and obtain a new approximation transfer function immediately. In the graphics window, the approximation transfer function is plotted together with the template. In classical

approximation case, the template consists of horizontal and vertical lines only. Vertical lines are for edge frequencies and horizontal lines are for passband ripple and stopband ripple. Simply dragging a line with the curve will change the template. . After the template change, the specification menu on the left will be updated accordingly.

5.4.2 General Magnitude Approximation (IIR)

The general approximation provides the user with the facility to design arbitrary passband and stopband responses. In arbitrary magnitude design mode, the desired amplitude response of the filter is specified by a pair of piece-wise linear boundaries (a template) of amplitude against frequency. The arbitrary response approximation program will attempt to fit a response within the upper and lower boundary. Specialised amplitude responses may be designed by a combination of the Remez-exchange and Newton approximation algorithm. The algorithm permits the order of tangency of certain extreme points (touch points) of the amplitude response to attenuation boundaries to be specified. The designer has the freedom to specify the sequence of passbands and stopbands and the distribution of touch points in each. A sequence of high order touch points placed in the passband of a filter approximation will yield a discrete sequence of functions, between Butterworth and Elliptic. Within the passband, higher order touch points usually smooth the amplitude function and lessen the delay peaking near the band edge at the expense of poorer stopband rejection. Higher order touch points in the filter stopband create sharp, deep notches useful for producing sharp transition band and for the rejection of specified signal frequencies.

A set of amplitude weighting function are available:

1.FLAT -- no weighting,

2.SINCX -- inverse sinc(x) weighting,

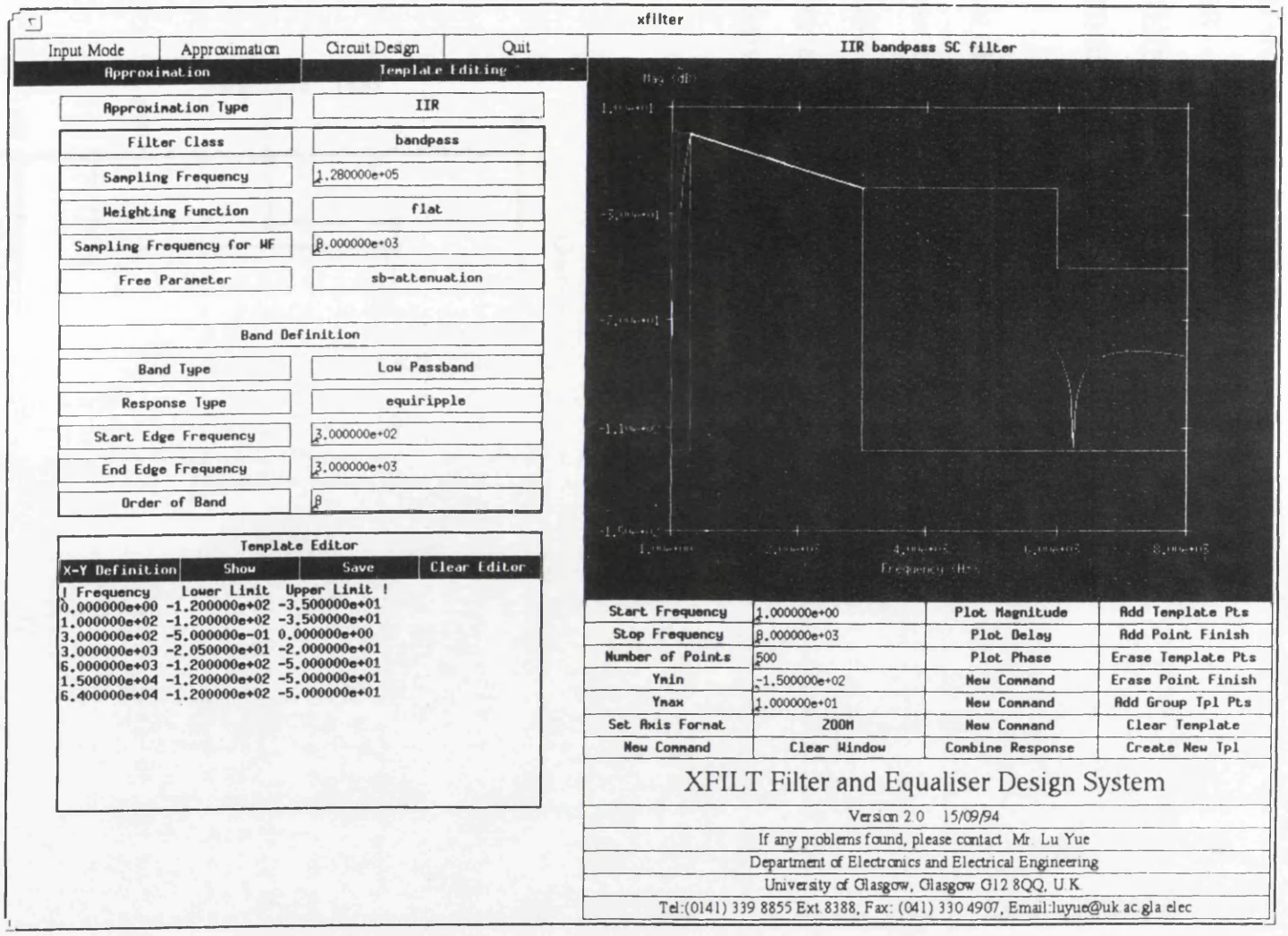


Fig.5-5 Screen shot of XFILT showing a sloping passband filter approximation

3.TANCX -- SINCX & LDI weighting,

4.LDI -- LDI termination error compensation due to single phase selected in circuit realisation (for SC circuit),

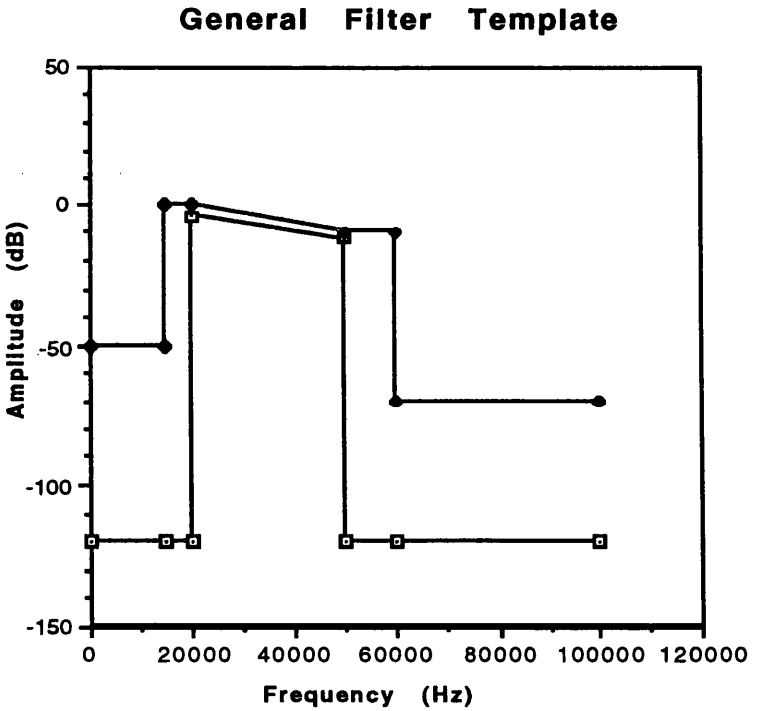
5.BANANA -- sagging passband

6.USER -- user specified function - needs C procedure to evaluate.

7.EXTERNAL-TF reads values of a predistorting function from a file.

8.OPTIMISATION -- create template file used to compensate for deviation.

General filter approximation can generate very special transfer functions. To facilitate the construction and display of these, a structured approximation interface is offered. It consists of a *general menu*, 4 *band definition menus*, a *touch point edit menu* and a *template editor*. Fig.5-5 gives a typical sloping passband filter design window and Fig.5-6 gives one example for the template editor.



(a)

Template Editor			
X-Y Definition	Show	Save	Clear Editor

! Frequency	Lower Limit	Upper Limit !
0.000	-120.000	-50.000
15000.000	-120.000	-50.000
15010.000	-120.000	0.000
19999.900	-120.000	0.000
20000.000	-4.000	0.000
50000.000	-12.000	-10.000
50010.000	-120.000	-10.000
59999.000	-120.000	-70.000
60000.000	-120.000	-70.000
100000.000	-120.000	-70.000

(b)

Fig.5-6 Example for Template Editor

5.4.3 Group Delay Approximation

For applications where group delay response is important, approximations can be obtained for an equaliser associated with a filter or for an independent specification. For equaliser design, the template specifies the overall system (both filter and equaliser) group delay. A screen shot of a equaliser approximation is shown in Fig.5-7. In the graphics window of Fig.5-7, the system group delay response is shown in the top curve which is within the template, the bottom curve is the group delay of the filter designed and the middle curve is the group delay of the equaliser. For an independently specified group delay response design, any arbitrary shaped group delay response can be approximated. Fig.5-8 gives an example of a special group delay response. The Template Editor is also utilised in the definition of the template for group delay approximation.

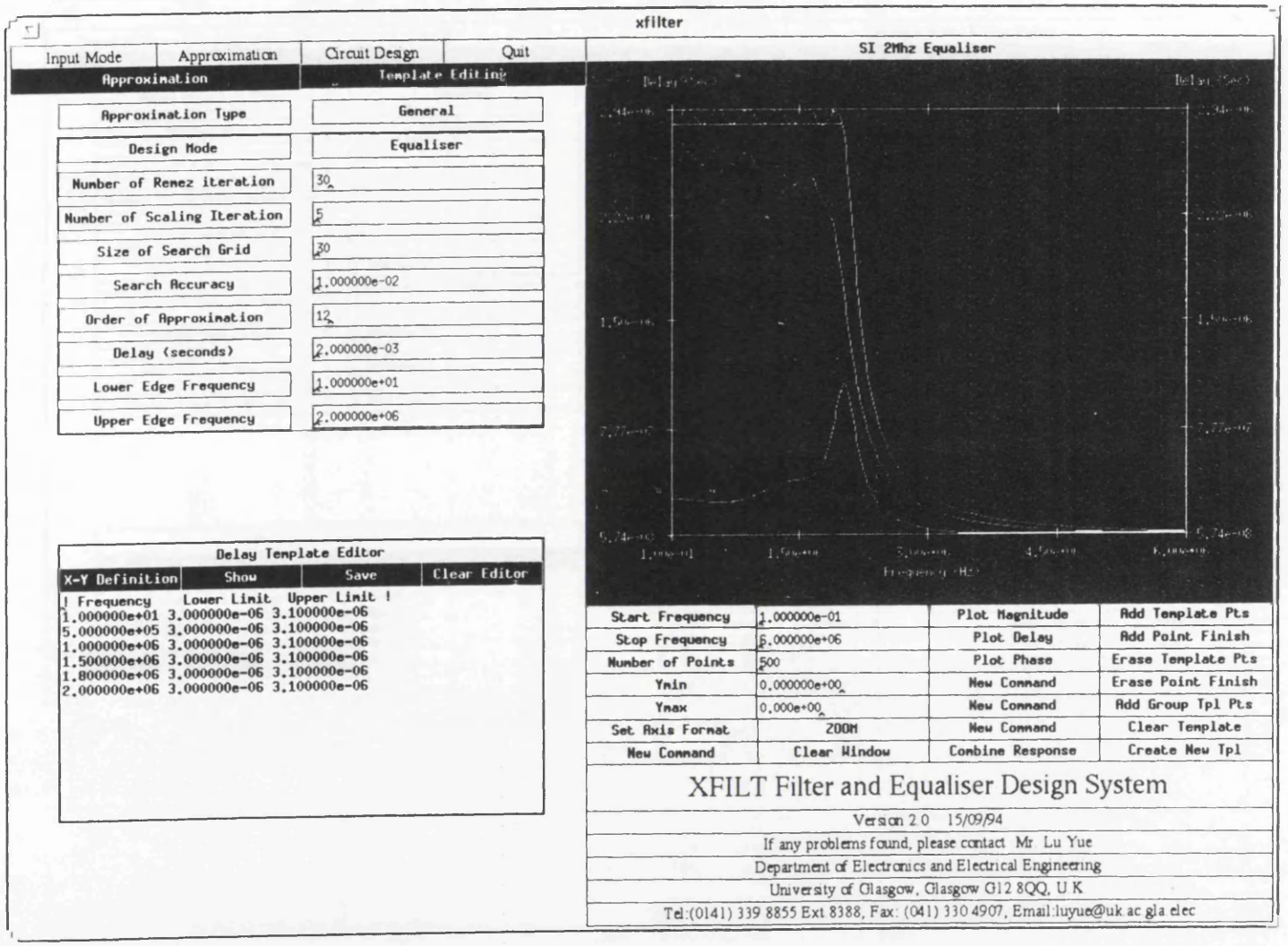


Fig.5-7 Screen shot of XFILT showing an equaliser approximation

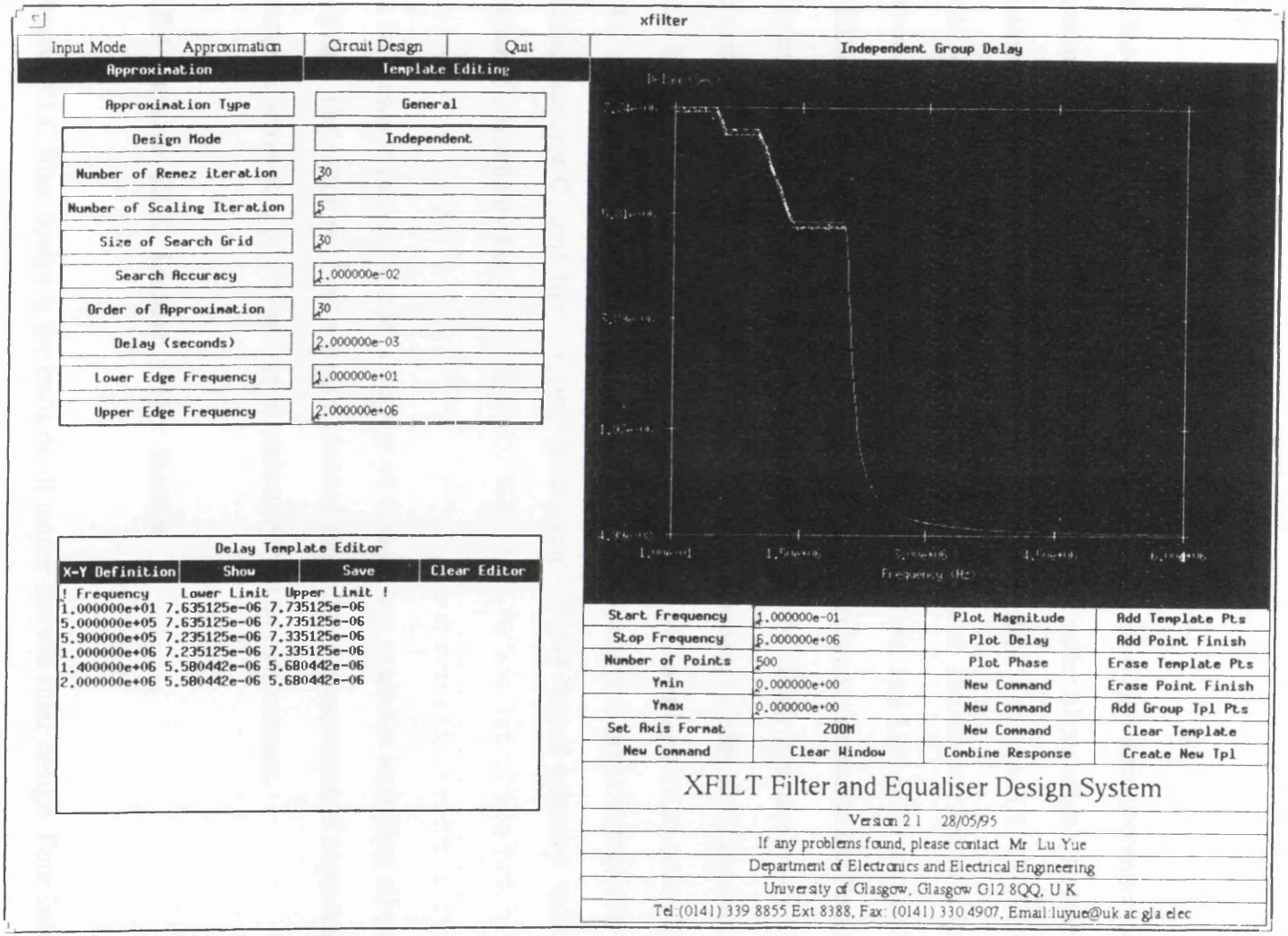


Fig.5-8 Screen shot of XFILT showing an independent group delay approximation

5.5 Circuit Realisation

Both biquad and ladder-based filter realisations are implemented in XFILT for active-RC, SC, SI and transconductor-C configurations. Passive RLC ladder synthesis is also available.

In ladder based filter design, all filter structures are derived by matrix decomposition methods. Besides including the conventional leapfrog ladder filter design, the matrix method also introduces many new methods such as LUD, LU-UL and UL-LU for SC realisation, Topological Decomposition, Right Inverse Decomposition and Left Inverse Decomposition for transconductor-C realisation, and Left-LUD and right-LUD decomposition for SI realisation. A matrix system is a very concise and flexible means of representation of a wide variety of networks. Each non-zero entry in a matrix represents the connection of a building-block between nodes. Building-blocks may belong to a variety of different technologies e.g. Miller integrator in active-RC, LDI integrator in SC, conventional and low-impedance input integrator in transconductor-C, and first, second generation or S^2I based memory cell in switched-current circuits.

In the cascade biquad mode, a variety of designs are available including all-pass biquads. The structure of the software enables the addition of any required biquadratic sections, active-RC, SC, SI and transconductor-C, in an easy manner.

5.5.1 Passive RLC Ladder Filter Design

Passive RLC filter design is the basis of all ladder derived filter design. Four ladder synthesis modes -- automatic, interactive, expert and external -- are provided. The Automatic Design Mode can be used to produce a ladder filter automatically. The Interactive Design Mode provides the designer with the ability to define the order of

the realisation of the resonant frequencies, while Expert Mode offers the facility of both definition of realisation order of resonant frequencies and the choice of removal operation in ladder synthesis. By using the Expert Design Mode, the experienced filter designer can design passive ladder RLC filter to the most demanding specification. The External Design mode is provided for entering predetermined passive RLC prototype from a file. The file may be in an actual SPICE format describing an existing design, or in an abbreviated SPICE like format. This facilitates the active circuit realisation of existing filters without re-approximation.

5.5.2 Active-RC Filter Design

Available decompositions for active-RC ladder filter design are Left-LU, left-UL, left-IA, Left-AI, Right-LU, Right-UL, Right-IB, Right-BI, Left-Inverse, and Right-Inverse.

The circuit for first-order functions in active-RC filter cascade biquad design is shown in Fig.5-9. The circuit in Fig.5-9(a) realises a lowpass first-order section and the circuit in Fig.5-9(b) realises a highpass first-order section. An allpass first-order section can be realised using Fig.5-9(c). The biquadratic active-RC structure is shown in Fig.5-10. Although this is the only biquadratic active-RC structure implemented in XFILT, the program's structure enables the addition of any required biquadratic active-RC section in an easy way.

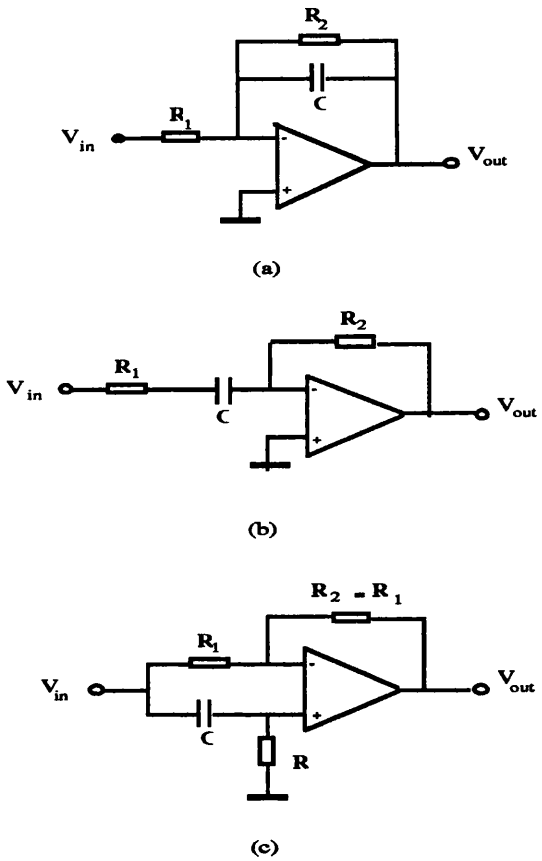


Fig.5-9 First-Order Active-RC Sections

(a).Lowpass First-Order Section

(b).Highpass First-Order Section

(c).Allpass First-Order Section

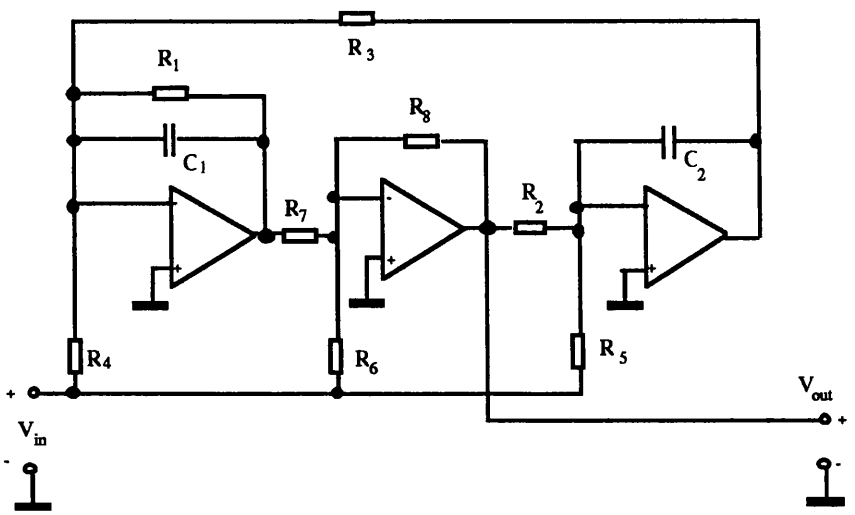


Fig.5-10 General Biquadratic Active-RC Structure

5.5.3 Switched-Capacitor Filter Design

All the switched-capacitor structures realised are strays-insensitive. Available decomposition methods for SC ladder filter design are Left-LU, left-UL, left-IA, Left-AI, Right-LU, Right-UL, Right-IB, Right-BI, Left-Inverse, Right-Inverse, LU-UL and UL-LU.

In cascade biquad SC filter design, the first-order stray-insensitive SC sections used in XFILT is shown in Fig.5-11. The building block can be used to construct a capacitive feedthrough branch, a LDI inverting integrator, a non-inverting integrator, a bilinear integrator or a LUD integrator or a linear combination of them. The second order biquad sections available in XFILT are traditional Fleischer and Laker's E-type and F-type biquads[16], modified Fleischer and Laker's biquads[17], Gregorian and Temes's biquad[18], Martin and Sedra's biquad[19], Sanchez-Sinencio, Silva-Martinez and Geiger's type-I and type-II biquads[20], and Nagaraj's biquad[21]. This is comprehensive, though not exhaustive, and selection between the biquads is possible.

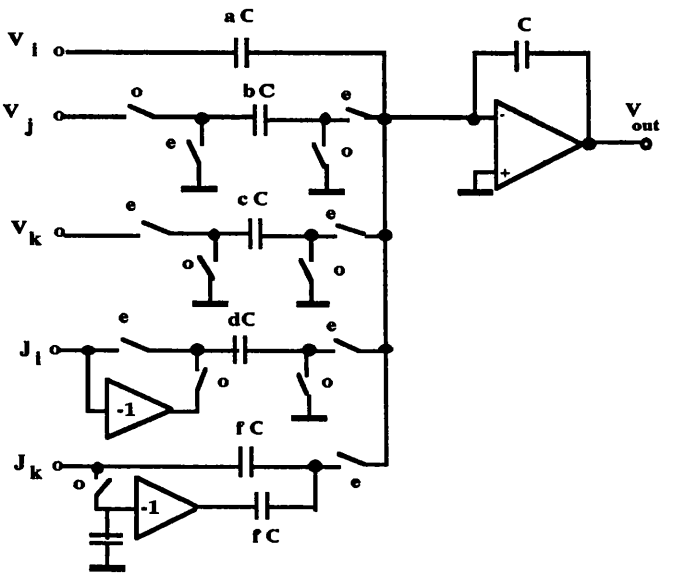


Fig.5-11 First-Order SC Section

The ability to design various ladder and cascade structures make XFILT a most powerful software package for SC filter and equaliser design.

5.5.4 Transconductor-Capacitor Filter Design

The decompositions available for transconductor-C filter design are the Topological Decomposition method for canonical transconductor-C and low impedance transconductor-C realisation, Right-Inverse Decomposition for conventional transconductor-C, and Left-Inverse Decomposition for low impedance transconductor circuit realisations. All realisations are generated as fully-differential circuits.

For biquad realisation, the first-order and second-order sections used in XFILT have already been given in Fig.3-1 and Fig.3-2 respectively.

5.5.5 Switched-Current Filter Design

Two decomposition methods are available for SI ladder filter design. One is based on first or second generation SI memory cell, the other is based on S^2I integrators. There are eight different approaches for each different memory cell. Therefore 24 different topologies can be derived for one ladder prototype.

The SI biquads used in cascade filter design are integrator-based and differentiator based biquads.

XFILT is the first SI filter and equaliser synthesis system to be reported.

5.5.6 Multirate and Multistage System Design

Multirate and multistage design ability is another special feature in XFILT. Using this design technique a system level performance comparison can be carried out. It is one step further to full system optimisation. In SC and SI design, multirate structures can be used to obtain more efficient circuit realisations.

5.6 Circuit Simulation

The simulation software used in XFILT are SCNAP4, SPICE and SWITCAP.

SCNAP4 is a high performance program developed in Glasgow University for analysing ideal and non-ideal switched-capacitor and switched-current circuits in both time and frequency domain. It also provides non-ideal sensitivity analysis and noise analysis. It can also provide simulation facilities for continuous-time circuits.

SPICE is the circuit simulator employed for simulations of passive-RLC, active-RC and transconductance-C circuits.

SWITCAP is a general simulation program developed in Columbia University for analysing switched-capacitor networks.

The source code of these programs has been modified for produce a readable output format for XFILT graphics output. The design phase of XFILT will produce a circuit netlist suitable for simulation software. The simulation software is invoked when the simulation menu is selected and the simulation results are presented graphically and also retained in a file.

5.7 System Performance Optimisation

Because of circuit non-idealities such as finite amplifier gain-bandwidth in active-RC and SC circuit, switch resistance in SC circuits, non-ideal transconductor in transconductor-C, and mismatch and truncation error in SI circuit, the filter response may not correspond precisely with the approximation function. To improve the circuit designed, a template-correction based, global optimisation method has been developed. The method is completely general and is applicable to active-RC, SC, SI, and transconductor-C filters realisation.

The software generates an error function determined by the difference between circuit simulation results and approximation transfer function. The template is then modified using the error function. The software automatically produces a new approximation, carries out a new circuit realisation followed by simulation and display of the optimised circuit response.

The procedures for optimisation are:

Step 1. Approximation (Using general IIR approximation only)

Step 2. Circuit realisation

Step 3. Circuit simulation

Step 4. Error function generation based on circuit simulation results and approximation transfer function

Step 5. Template modification using the error function

Step 6. Re-approximation, Re-circuit realisation and Re-circuit simulation

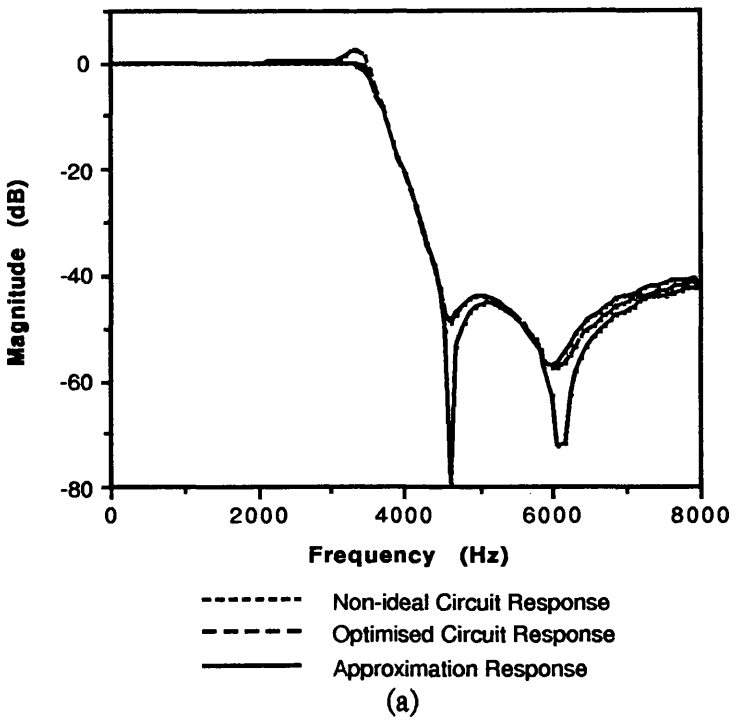
If results are satisfied, finish the design phase. Otherwise, back to Step 4 again.

To demonstrate the use of optimisation in XFILT, three examples are given below.

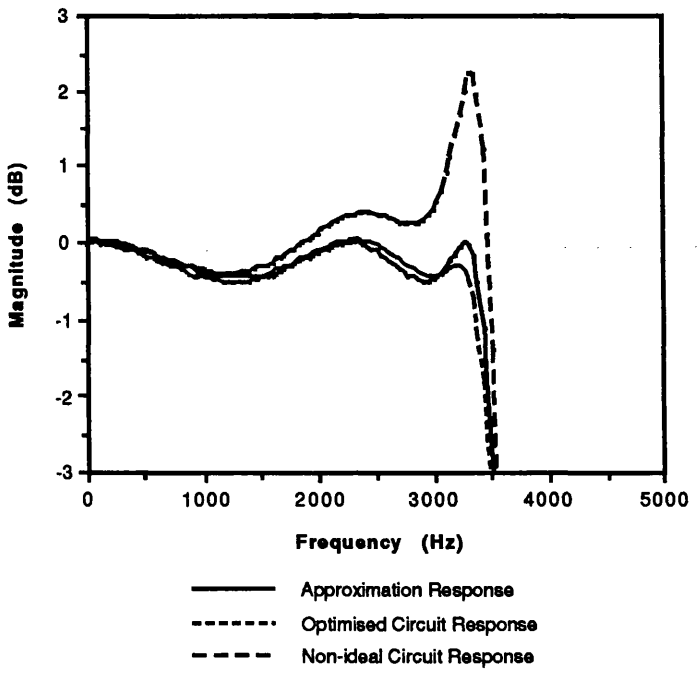
The first example is a 7th-order lowpass active-RC filter. The opamp model used has 80dB gain and 20MHz unit gain bandwidth. The filter response is given in Fig.5-12(a) and the passband details are shown in Fig.5-12(b). It can be seen from Fig.5-12(b) that non-ideal opamp would introduce about 2.3dB variation in the passband. When the optimisation scheme is applied, distortion of the characteristic due to non-ideal operational amplifiers is corrected.

The second optimisation example is an 8MHz cutoff frequency SI filter using S^2I technique. The filter frequency response is shown in Fig.5-13. The non-ideal integrator is simulated by giving the transistors an artificially low output resistance of 100Ω with gm normalised to 1S and the frequency response of ideal and non-ideal integrator is shown in Fig.5-14. Using the non-ideal integrator, results in a cutoff frequency shifting from 8MHz to 7.5MHz, a reduction in the ripple and a loss in D.C gain as shown in Fig.5-15. By adopting the optimiser in XFILT, the circuit response is corrected to a cutoff frequency of 8MHz and the ripple restored as shown in the Fig.5-15.

The third example is to study parameter truncation error effect on circuit response. The filter is an SI voice band lowpass filter and the frequency response is shown in Fig.5-16. The passband response is simulated with all the circuit parameters (Gm) truncated to two decimal places, Fig.5-17. The amplitude variation is increased towards the band edge frequency. Optimisation is applied and a realisation with circuit parameters still truncated to two decimal places gives an improved response. This example shows the possibility of correction of filter parameter truncation error and similar results have been obtained for a higher order bandpass filter. The practical reasons for truncation error are many and varied, these examples merely indicate that if a non-ideal model can be produced, optimisation can be used to good effect.



(a)



(b)

Fig.5-12(a) Optimisation of a 7th order lowpass active-RC filter

Fig.5-12(b) Passband detail of the example

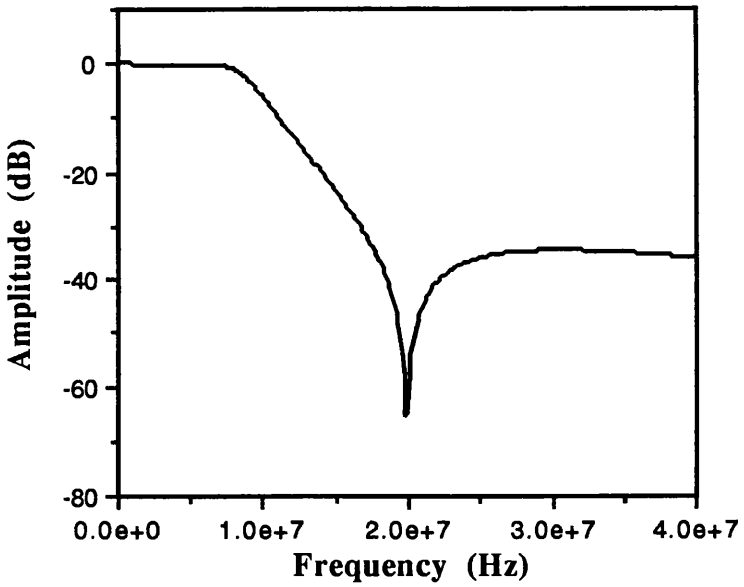


Fig.5-13 An 8MHz cutoff frequency lowpass filter

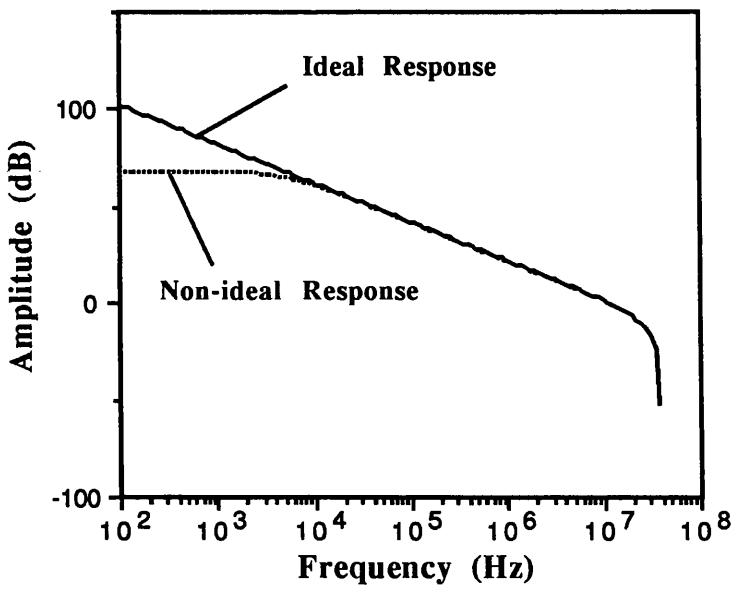


Fig.5-14 Frequency response of S^2I integrator

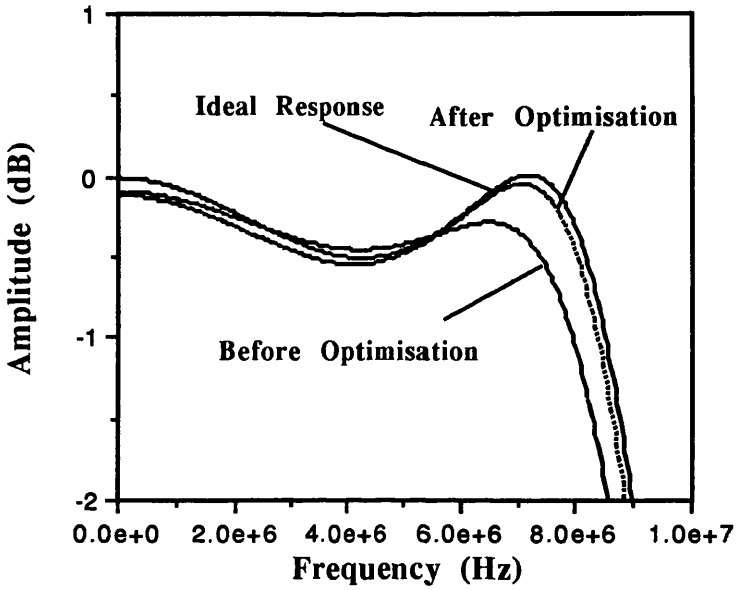


Fig.5-15 Optimisation of 8MHz lowpass filter passband details
(D.C gain scaling has been used)

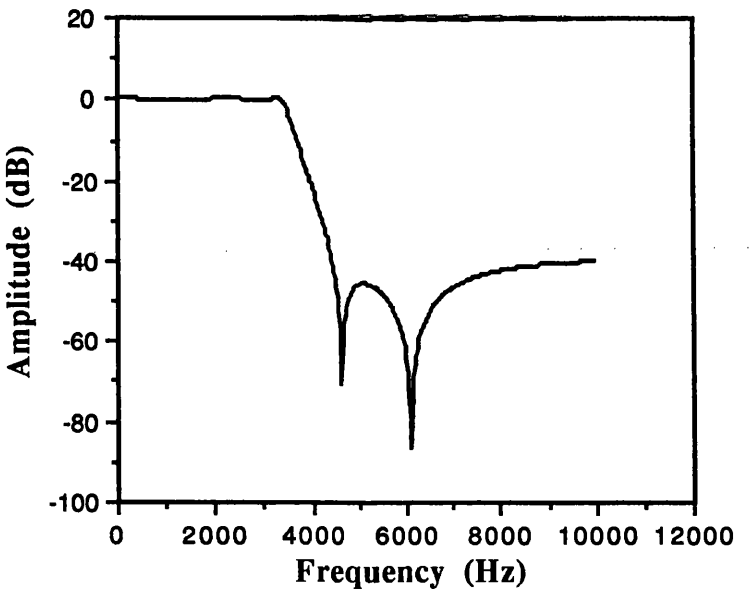


Fig.5-16 Lowpass filter for truncation error minimisation

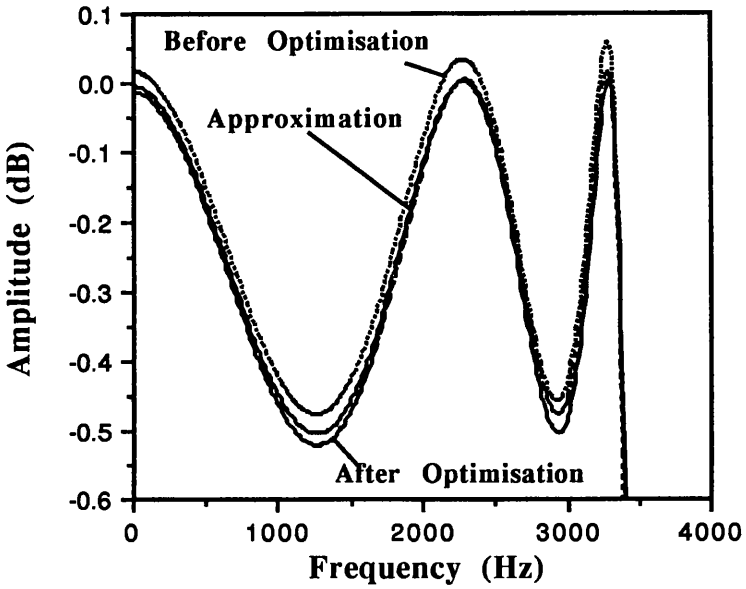


Fig.5-17 Optimisation in truncation error effect minimisation

The main attraction of this optimisation approach is the general applicability and the low order optimisation space, which always corresponds to the order of the original filter rather than the number of nodes in the circuit. The process is quick and usually completed within minutes.

5.8 Summary

A new system for filter design has been introduced. Several advanced facilities which remove traditional design limitations have been illustrated. The graphics based system makes software integration and management easy to handle. Amplitude and group delay responses with arbitrary and classical shaped filter specifications can be approximated. A wide variety of filter realisations can be quickly obtained. Both ladder-based and biquad topologies are available plus several new structures in SC, SI

and transconductor-C realisations. XFILT also offers a set of efficient optimisation facilities to improve the final designs within physical constraints.

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Chapter 6: Conclusions and Future Development

CHAPTER 6: CONCLUSIONS AND FUTURE DEVELOPMENT

Research on VLSI analogue filter design and signal conditioning circuits continues to be a very active area due to an analogue "real" world of signals and its wide range of frequencies.

This thesis has developed various approaches for the design of modern analogue filters and provides a practical analogue filter and equaliser computer aided design system. In this final Chapter, conclusions are drawn from the work presented and promising avenues of future work are discussed.

6.1 Conclusions

The thesis began by placing the analogue filter design technique and software into a historical and technology perspective. The evolution of the analogue filter was traced from early work, through the passive-RLC to transconductor-C and switched-current realisations. The software development in VLSI analogue filter automation is reviewed. It is demonstrated that the development of novel design methods for filters and equalisers is still of great interest and a general user friendly software package is a prime requirement. The new design methods and software form the main topics of this thesis.

The thesis contains four major technique parts. Three parts are related to different filter design techniques, which are SC, transconductor-C and SI realisations. The fourth part describes the development of XFILT software.

In SC filter design, a cascade SC design approach which includes a novel pole-zero pairing method and a comprehensive comparison of SC filter realisation using different biquads are presented. By using the XFILT filter compiler, five SC filter systems (lowpass, wide bandpass, narrow bandpass, highpass, and bandstop) are constructed. Comparison for SC filter realisations on total capacitance, capacitance spread, sensitivity, non-idealities, dynamic range and noise performance is given. Very useful guidelines for the choice of a suitable biquad structures are proposed.

The brief review of matrix design method for SC filters is given. The canonical realisations of SC filter are studied. An example is given to demonstrate that the proposed canonical design method can be efficiently used.

The research on multirate SC system design is pursued. Several strategies and the algorithms for multirate SC system design are presented. A narrow baseband bandpass filter and a single-path frequency-translated SC bandpass filter are given as examples to demonstrate the new technique and the suitability of XFILT.

In transconductor-C filter design, a cascade approach is presented. The matrix based ladder transconductor-C filter design approach is reviewed. The definition of a canonical ladder based transconductor-capacitor filter is introduced and two canonical ladder based transconductor-capacitor filter design approaches are proposed. In the Transfer Function Modification Approach, a transfer function which is unrealisable by a canonical ladder is modified to a transfer function which is realisable by canonical ladder, and when the ladder is simulated by a transconductor-C circuit the original transfer function is then realised by a change in input circuitry. This approach can also be used when prototype ladder is not realisable, such as in even-order Elliptic case. The Mixed Variable Representation Approach is applied by properly choosing voltage and current variables to ensure a compact matrix form. The low sensitivity property of the circuit can be maintained because no

modification has been made to the circuit structure. This approach can be used in the case where ladder is already available or Transfer Function Modification Approach cannot be employed. Application of both approaches is demonstrated in an 8th-order Butterworth bandpass filter design.

The ladder based transconductor-C equaliser design is also discussed. A practical video frequency transconductor-C filter and equaliser design is given to demonstrate the utility of the matrix design method and the transconductor-C filter and equaliser design software. Both simulated and measured results are presented. A comparison of sensitivity for ladder based and cascade structures was also carried out.

For SI circuit realisation, a new approach to realise an exact ladder based SI filter with first and second generation memory cell has been presented. The bilinear transformation is used in the design procedure. Eight different SI ladder structures can be obtained for one prototype ladder. Therefore it provides SI filter designers with various circuit choices based on different requirement such as area, maximum ratio of transistor aspect ratio limit, sensitivity or noise performance. Techniques to improve dynamic range and reduce circuit parameter spread are also presented. The proposed approach is well suited for a computer compiler implementation and has been incorporated into XFILT. A suitability study of each decomposition method for different filtering applications is also carried out and a general guideline for the choice of different decomposition methods is obtained.

A comparison study on switched-current (SI) filter sensitivity performance based on first generation and second generation memory cells is carried out. Using four filters examples, it is demonstrated that SI filters based on a second generation SI cell have good sensitivity performance. For SI filters based on first generation memory cells, it is shown that a high ratio of clock frequency to cutoff frequency in the

lowpass case, or a high ratio of clock frequency to midband frequency in the bandpass case would introduce high sensitivity.

A novel approach for SI ladder filter based on the S^2I integrator is also proposed and a canonical realisation for filters using these is developed. Examination of SI equaliser design reveals that cascade structure is often a better candidate than ladder based structures.

Finally, multirate SI filter system design is addressed and various examples illustrate how multirate approaches can be used in narrow band filter design to good advantage.

Work on developing the XFILT software occupied a large proportion of the research time though the description of the software only consists of a small part of this thesis. The distinguished features of XFILT are its **Ease of Use**, **General Applicability**, and **Ease of Extension**. The philosophy of the system is explained and the system structure is described. A very brief introduction of to the assembly of the design methods of this thesis into a software package (XFILT) for VLSI analogue filter and equaliser design is given. The user aspects of XFILT have been discussed and various capabilities of XFILT have been demonstrated. Several advanced facilities which remove traditional design limitations have been illustrated. The circuit design capability in XFILT is explained and the circuit simulation software used in XFILT are briefly addressed. The system performance optimisation is explained and demonstrated by examples.

XFILT has been used in various circuits taken through to fabrication, including an SC filter, a transconductor-C filter and equaliser, and an SI filter and equaliser. The system is under further enhancement towards a commercial product.

6.2 Future Development

The extended Remez algorithm[1] is a powerful approximation algorithm used in most filter design. However, there is occasionally a need to design filters with multiple bands or requirements on both amplitude and group delay properties. In this case, the extended Remez algorithm cannot be employed and a more general optimisation based approximation algorithm is required.

The use of optimisation for filter design represents a classical problem considered in the analogue and digital filter design literature. Some typical approaches are least-square[2], least-pth error[3,4], linear programming[5,6] and the iterating Remez algorithm[7]. Several approaches have been presented on the simultaneous design of both magnitude and group-delay (phase)[8,9].

One potential problem with these optimisation methods is that conventional optimisation techniques lead only to local, not global solution. The selection of a suitable starting point thus becomes of great importance. Because of the complexity of the function to be optimised in filter design, commonly used algorithms do not give a sufficiently good solution. Moreover, approximation and implementation are usually in two procedures and the requirement on approximation and on circuit realisation are considered separately in the filter synthesis. However if the question is to design a filter with globally optimum performance in magnitude, group-delay, component spread and area, sensitivity, dynamic range, noise .... then none of the above methods can be applied.

A solution to all these problem is to use a global optimisation method, which makes no assumption on the particular cost function. Simulated annealing and genetic algorithms as global optimisation algorithms have been extensively used in digital filter design[10,11,12,13,14,15]. These two algorithms can also be used in analogue

filter design and are very appealing because they produce high quality solutions and are in general easy to implement. It must be noted that simulated annealing and genetic algorithm are general design methodologies rather than completely specified algorithms. Thus, application of these methods to an analogue filter design problem require careful consideration. Many avenues are open for new research.

Adaptive filters are widely used in communication systems. The realisation of adaptive SC, transconductor-C and SI filter will have wide application. The research on matrix design approach combined with adaptive structures will produce various new filter configurations.

With the development of satellite communication, the ultra high frequency (UHF) operation filter has received great attention. Research into including inductors on a integrated silicon chip has been progressing steadily recently[16]. Since the achievable quality factors in those filters are low, due to resistive losses of the inductors, modified active-RLC version filter are proposed[17,18,19]. It is expected that this kind filter will be able to work in GHz frequency range. XFILT can be easily extended to include the design of such filters.

A knowledge based analogue filter and equaliser synthesis system could be built based on XFILT. A heuristic design technique can be used and the knowledge data base needs to be created. The stored knowledge can be either mathematical techniques or intuitive reasoning procedures frequently used by filter design experts. The system performance comparison can be carried out automatically by the software.

The software can also be used as a front-end design aid for analogue field programmable gate array (FPGA). The generality of the XFILT make itself suitable

to several kinds of analogue FPGA CAD systems such as, SC realisation, transconductor-C realisation or switched-current realisation.

The combination of XFILT with an existing digital design system will make a powerful ASIC design system and a PC version of XFILT will attract many users.

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