SIMULATION TOOLS FOR THE ANALYSIS OF SINGLE ELECTRONIC SYSTEMS

by

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June 1994

A Thesis presented to the University of Glasgow
Department of Electronics and Electrical Engineering
in partial fulfilment of the requirements
for the degree of Doctor of Philosophy

hoc adiutoribus dono

Dixeris egregie notum si callida verbum
Reddiderit iunctura novum.

Horace, *Ars Poetica* l.47

ABSTRACT

Developments in theory and experiment have raised the prospect of an electronic technology based on the discrete nature of electron tunnelling through a potential barrier. This thesis deals with novel design and analysis tools developed to study such systems.

Possible devices include those constructed from ultrasmall normal tunnelling junctions. These exhibit charging effects including the Coulomb blockade and correlated electron tunnelling. They allow transistor-like control of the transfer of single carriers, and present the prospect of digital systems operating at the information theoretic limit. As such, they are often referred to as single electronic devices.

Single electronic devices exhibit self quantising logic and good structural tolerance. Their speed, immunity to thermal noise, and operating voltage all scale beneficially with junction capacitance. For ultrasmall junctions the possibility of room temperature operation at sub picosecond timescales seems feasible. However, they are sensitive to external charge; whether from trapping-detrapping events, externally gated potentials, or system cross-talk. Quantum effects such as charge macroscopic quantum tunnelling may degrade performance. Finally, any practical system will be complex and spatially extended (amplifying the above problems), and prone to fabrication imperfection. This summarises why new design and analysis tools are required.

Simulation tools are developed, concentrating on the basic building blocks of single electronic systems; the tunnelling junction array and gated turnstile device. Three main points are considered: the best method of estimating capacitance values from physical system geometry; the mathematical model which should represent electron tunnelling based on this data; application of this model to the investigation of single electronic systems.

At present, most capacitance estimates ignore fringing fields and systematically underestimate capacitance values. Formulae based on bispherical co-ordinates are developed, which provide better estimates without the computational expense of finite element calculations. These prove especially appropriate for the new generation of granular metal-insulator-metal systems. Calculations show that these systems will be required for reliable device operation above 77K.

A number of descriptions of electron tunnelling in ultrasmall junctions are reviewed. A semi-classical approach is chosen, which treats the system as a capacitive equivalent circuit under the action of discrete tunnelling events. This allows simple investigation of complex systems using Monte Carlo techniques, while accounting for

thermal fluctuations - the most important source of noise in present devices. A heuristic Lengevin equation model and more detailed phase correlation model are described. These include further physics of the tunnelling process, but require increased computational effort.

Two core modelling tools are designed to investigate single electronic systems. The General Network Solver is a suite of Monte Carlo modelling routines which can be applied to any system equivalent circuit. A linear programming technique is also developed. This efficiently calculates areas of legal operation in control parameter space for any system.

It is found that: array threshold voltage at zero offset bias is a good figure of merit in tunnelling junction arrays. For steady charge flow, these systems show remarkable resilience to component variation. Stability is optimised when array capacitance to ground is small in relation to junction capacitance. Similarly, coupling strays less than junction and grounding capacitance have little effect on device performance. However, from these detailed stability studies, it is found that transmission of more realistic bitstream patterns results in information loss - for array electrons tend to stable, equidistant configurations.

The frequency response of single and three phase gated turnstiles is investigated. Under realistic operating conditions the three phase turnstile has no advantage. Its extra complexity reduces unacceptably its operating area in control parameter space. The operation of coupled turnstiles is perturbed both by coupling capacitance directly, and by cross-talk from non-static charge. Both effects reduce the operating areas in control parameter space. These effects are intrinsically complex in nature; however some practical insight is gained by using our tools. Bit error rates in coupled turnstiles are also investigated.

ACKNOWLEDGEMENTS

No original research is solely the achievement of one person; but a collaborative effort. I have had the opportunity to work with a number of people while a research student at Glasgow University. Each has helped in their own way; sharing expertise, exchanging views or simply lending moral support. It gives me great pleasure to acknowledge some of their aid.

I would like to thank my supervisor, Professor John Barker, for his enthusiasm, vision and prudent advice, which have proved crucial to this project. I also benefited from discussions with Asen Asenov and Sharief Babiker. As research students in the same area, Sharief and I often had the chance to cross-pollinate ideas, certainly to my benefit.

The capable experimental group in the Nanoelectronics Research Centre at Glasgow have also been of help, ensuring that theoretical work retained its practical edge and offering physical devices to model. John Weaver, Rebecca Cheung and Robert Nicol all deserve my gratitude.

Particular thanks are due to Professor Steve Beaumont, head of the Nanoelectronics Research Centre, and the late Professor John Lamb, head of the Electronics and Electrical Engineering Department during my early research work. Both showed an interest in my progress and made available timely and unexpected finance to supplement my grant.

During this initial period, the postgraduate lecture course arranged by John Davies and information on mainframe arcana provided by Mike Laughton also proved useful.

This work was supported by the Science and Engineering Research Council

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PUBLICATIONS

Aspects of this work have been published as :

J.R. Barker, S. Roy, and S. Babikir, *Trajectory Representations, Fluctuations, and Stability of Granular Electronic Devices.* In 'Science and Technology of Mesoscopic Structures' in Japan, edited by S. Namba, C. Hamaguchi, and T. Ando, Springer-Verlag: London, Tokyo, New York, 213-232, (1992).

J.R. Barker, J.M.R. Weaver, S. Babikir, and S. Roy, *Theory, Modelling and Construction of Single-Electronic Systems.* In 'Second International Symposium on New Phenomena in Mesoscopic Structures' in Hawaii, (1992).

S. Roy, J.R. Barker, and A. Asenov, *System Simulation Tools for Single-Electronic Devices.* In 'Proceedings of the International Workshop on Computational Electronics' in Leeds, England, edited by C.M.Snowden and M.J. Howes, (1993).

J.R. Barker, S. Babikir, and S. Roy, *Single Electron Transport in Nanostructure Systems.* Submitted to Physica B

Publications associated with this research include :

S. Roy, A. Asenov, and J. R. Barker, *Optimum Partitioning of Topologically Rectangular Grids.* Accepted for 'International EUROSIM Conference HPSN Challenges in Telecomp and Telecom: Parallel Simulation of Complex Systems and Large-Scale Applications' in Delft, Netherlands, (1996)

S. Roy, A. Asenov, A.R. Brown and J. R. Barker, *Partitioning of Topologically Rectangular Finite Element Grids.* Accepted for '4th ACME Conference on Computational Mechanics in the UK' in Glasgow, Scotland, (1996)

A. Asenov, A.R. Brown, S. Roy and J. R. Barker, *Topologically rectangular grids in the parallel simulation of semiconductor devices.* In 'International Workshop on Computational Electronics' in Tempe, Arizona, (1995) (Will appear in as regular paper in VLSI Design)

Publications (cont.)

A.R. Brown, A. Asenov, S. Roy and J. R. Barker, *Parallel 3D Finite Element Power Semiconductor Device Simulator based on topological rectangular grid.* In 'Simulation of Semiconductor Devices and Processes' vol 6, edited by H. Ryssel, P.Pichler, Springer-Verlag Wien, New York, p.336-339, (1995)

A.R. Brown, A. Asenov, S. Roy and J. R. Barker, *Development of a parallel 3D finite element power semiconductor device.* IEE Digest, 1995/064, 2, 1-6 (1995)

CHAPTER 1 INTRODUCTION

Since the invention of the transistor in 1947 and its subsequent service in integrated circuits, the history of digital electronics has been a relentless quest for device miniaturisation. Three facts drive this search. Firstly, miniaturisation reduces the volumes across which electric fields act, allowing lower power dissipation. Secondly, lower capacitance and shorter interconnects lead to faster systems. Finally, miniaturisation (in tandem with increased chip size) allows more devices on a chip and thus reduces relative costs [1].

It is obvious that the feature size of modern devices cannot be reduced without limit. Eventually it will rival the electron wavelength. In this regime many classical concepts become invalid. A more detailed quantum mechanical approach is needed to fully understand electron transport, and develop the new concepts necessary to describe device operation.
There is also the opportunity to *exploit* quantum mechanics and develop novel devices. Apart from any intrinsic benefits gained from quantum mechanical operation, such devices will retain the power, speed, and cost benefits which miniaturisation brings.

In recent years, new developments in both theory and experiment [2] have allowed the serious consideration of an electronics technology based on one basic quantum mechanical phenomena - the discrete nature of electron tunnelling through a potential barrier. Such *granular electronic* devices include those constructed from ultrasmall normal tunnelling junctions. They exhibit charging effects including the *Coulomb blockade* and *correlated electron tunnelling*. These devices allow operation at the limit of one transferred carrier per bit, the information theoretic limit. As such, they are often referred to as *single electronic devices.*

1.1 Properties of Single Electronic Systems

Two properties of tunnelling junction systems are vital to the operation of single electronic devices. Firstly, ultrasmall junctions allow ultrasmall junction capacitance. The electrostatic charging energy of a single tunnelling event across such a junction is,

$$E_c = \frac{e^2}{2C} \qquad (1.1)$$

Junctions with capacitance as low as $C = 10^{-18}$ F have been reported [3], which give $E_c \approx 80$ meV. If C can be made small enough, the energy associated with tunnelling may be far greater than the average energy of thermal or quantum fluctuations. For thermal fluctuations the condition on temperature T is,

$$k_B T << E_c \quad \Rightarrow \quad T << \frac{e^2}{2k_B C} = T_c \qquad T_c \text{ is } \textit{critical temperature} \qquad (1.2)$$

For quantum fluctuations in a junction of tunnelling resistance R_t, the condition is,

$$\frac{\hbar}{R_t C} << E_c \quad \Rightarrow \quad R_t >> \frac{2\hbar}{e^2} \approx \frac{\pi\hbar}{2e^2} = R_Q \qquad R_Q \text{ is } \textit{quantum resistance} \qquad (1.3)$$

Under these conditions, charging effects are no longer masked by quantum noise and normal quasi-continuous current flow no longer occurs. Unless the external applied potential V makes tunnelling energetically advantageous, charge is not transferred. There is a *Coulomb blockade* of current at $V < e/2C$. The importance of this phenomenon in device terms is obvious. There is direct control of a microscopic process via an easily measurable and controllable macroscopic parameter, independent of the precise nature of the tunnelling barrier.

The second property of junction systems results from the discrete nature of charge on an electrode itself. For instance, in a double junction system such as that of figure 1.1 the central electrode is detached from a source of continuous charge. It has relative charge $ne+\delta Q$. δQ is an initial fractional charge dependant on junction Fermi levels, and external potentials gated to the electrode by strays. ne is an integral charge due to tunnelling events. In such a system, tunnelling events in the two junctions are no longer independent, but are *correlated* by the need for ne to remain integral. The correlation can be tuned by external gating of the fractional charge δQ.

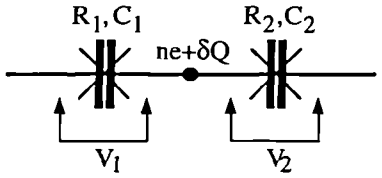


Fig 1.1 Equivalent circuit of a double junction system. Charge on central electrode is $ne+\delta Q$.

Correlated tunnelling has been observed in a number of systems, most strikingly in ultrasmall metal-oxide-semiconductor field-effect transistors (MOSFETs) [4]. In such transistors, conduction occurs through a narrow source-drain channel of two-dimensional electron gas. When the channel is narrow enough (typically 20nm) fluctuations in semiconductor doping potential can form potential barriers, cutting the channel into electron pools separated by tunnelling junctions. As MOSFET gate potential is varied

(changing δQ values) electron correlation is exhibited as periodic fluctuations in source-drain conductance. The MOSFET is acting as a *single-electron transistor.*

Although there are other examples of potentially useful single electron switching processes - for example electron waveguide interferometer switches [5] - such phenomena are limited by coherence problems. They have little integrability, and are critically dependant on accurate fabrication [6]. On the contrary - because of the Coulomb blockade and correlated tunnelling effects - single electronic devices have the benefits of good structural tolerance and self quantising logic.
The speed of single electronic systems is limited by circuit relaxation. This requires switching timescales greater than $\tau_c = R_t C$, the nominal time between tunnelling events through a junction. (Note that τ_c is the characteristic time of junction relaxation, not the duration of the actual tunnelling event itself [7].) The operating voltage of such a system is proportional to junction threshold voltage V.
Thus immunity to thermal noise, speed and nominal operating voltage all scale beneficially with junction capacitance. For ultrasmall junctions the possibility of room temperature operation at sub picosecond timescales seems feasible [8]. Practical devices have been reported, operating at liquid Helium temperatures at gigahertz frequencies [9, 10].

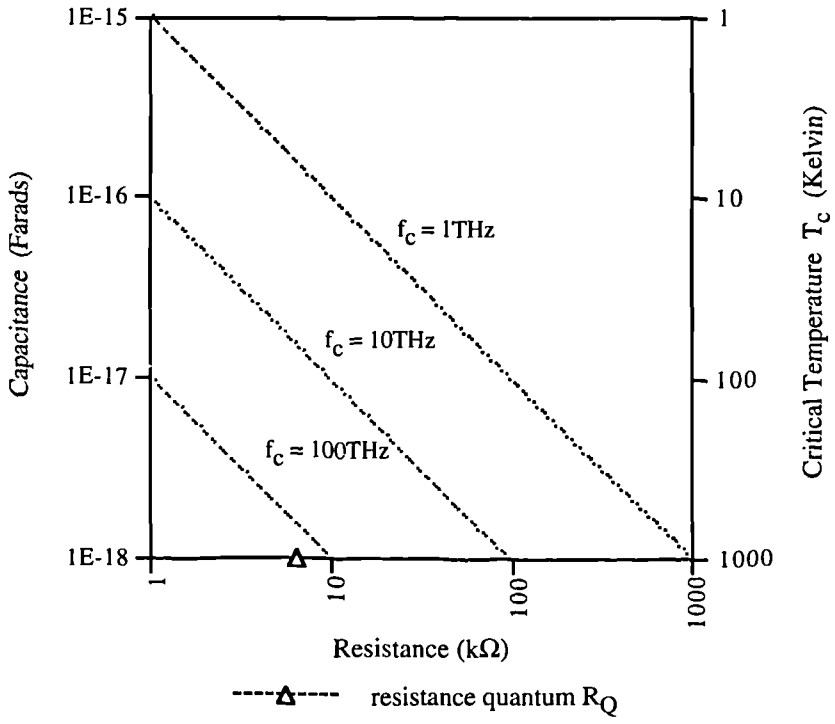


Fig 1.2 Comparison of the critical parameters of ultrasmall tunnelling junctions in relation to their junction capacitance and tunnelling resistance. The critical frequency $f_c = 1/\tau_c$.

1.2 The Need for Novel Analysis Tools

Single electronic devices do, however, pose novel modelling and analysis problems. By their very nature, they can only be fully described quantum mechanically, or by quantum mechanically based semi-classical models. Because of their reliance on correlated electron tunnelling, they are extremely sensitive to external charge [11]. Such charge may be the result of material trapping-detrapping events, external potentials gated via strays, or cross-talk from other parts of a single electronic system. Other possible effects that must be considered include *charge macroscopic quantum tunnelling* and *electron cotunnelling*. These processes are the result of thermal or quantum fluctuations acting upon a system of junctions, allowing simultaneous multiple tunnelling events. They are discussed in detail in Chapter 4. In practical systems the effect of fabrication variation in junction parameters on system performance must also be considered.

To act as an integrable digital technology, single electronics must perform well in spacially extended systems of many junctions. When the Coulomb blockade was first observed, it was found impossible to produce the necessary high impedance measurement conditions for a single junction. Instead, *tunnelling junction arrays* were required to decouple the junction of interest from its environment (see for instance [11]). It can also be shown that sets of junction arrays are required to buffer against some of the cotunnelling effects mentioned above [12, 13]. Thus even simple logic functions will require the operation of extended systems.
Figure 2.6 shows an electron micrograph of one simple system under fabrication at Glasgow. It, and all other extended systems, will by nature be complex to model.

Because of all these reasons, new tools are required for design and analysis of single electronic systems. Chapter 2 reviews the background of single electronics technology and follows in detail the argument for the development of such tools.

1.3 Breakdown of Work to be Accomplished

The aim, therefore, is to develop practical aids for the analysis of single electronic systems. This aim can be separated into three subgoals; requiring answers to three sets of questions. Firstly, what data must be extracted from the physical devices themselves? It will be seen that accurate estimation of tunnelling junction and electrode grounding capacitance is paramount in predicting device operation. How can such estimates be achieved? Secondly, what mathematical model should be chosen to represent the tunnelling process? Finally, and most importantly, how can the model be best applied to the investigation of single electronic systems? In order to develop

general analysis tools, the basic building blocks of any system should first be considered. Characterising these will hone skills and evolve tools which can then be applied to more complex systems. What are the basic building blocks of single electronics? How is their characterisation to be carried out?

Capacitance Estimates :

At present, the only proven fabrication approach appropriate for integrated systems is the metal-insulator-metal technique pioneered by Fulton & Dolan [14]. Almost without exception, geometrical capacitance calculations for these systems are based on the parallel plate approximation. This ignores edge effects which dominate in small junctions. Therefore the parallel plate approximation gives systematically lower values of device T_c than are possible in practice. Finite element analysis will give more accurate results, but at the cost of calculation time and complexity.
We develop analytic capacitance results based on the two spheres approximation. This geometrical idealisation contains more of the intrinsic physics of the problem, while remaining simple to calculate. It should prove especially useful for the granular metal-insulator-metal fabrication approaches under development. Chapter 3 comprises a full discussion of capacitance estimates.

Choice of Mathematical Model :

Any mathematical model of a physical system must strike a balance between simplicity and the inclusion of physics relevant to the system. The model must be simple enough to produce results in a reasonable timescale. It must include the physics necessary to make those results useful. One basic description of a system of tunnelling junctions is its capacitive equivalent circuit. The action of this circuit under the influence of discrete tunnelling events can be considered - with tunnelling rates modelled as a function of system parameters. This description exhibits all the non-trivial nature of real life systems while remaining simple to investigate using Monte Carlo techniques. Its accuracy (and speed) are dependant on the physics included in the tunnelling rate calculations.
Chapter 4 considers a number of mathematical models of junction tunnelling rates, based on the quantum nature of electron tunnelling. The physical effects considered include; thermal and charge fluctuations, the general electromagnetic environment of each junction, and other systems effects such as charge macroscopic quantum tunnelling. The conditions under which each model holds valid are also investigated.

Development of Analysis Tools :

As noted above, the development of analysis tools for single electronic systems is inextricably linked to the choice of basic system building blocks. Two of the most primitive building blocks are the tunnelling junction array and gated turnstile.
A tunnelling junction array is the simplest single electron device to model, and to construct physically. It can be represented as a line of junctions along which charge moves. The line is capacitively linked to a common ground, and this coupling allows soliton states to form in the system [12]. The importance of these soliton states for this work is that they allow some analytic description of the system. Thus modelling tools in development can be compared with simple analytic results.
The gated turnstile is a device proposed by Ésteve, and constructed by Geerligs *et al.* [9]. It clocks electrons across a short junction array by way of an oscillating control voltage on the array's central electrode. It is the first device to show detailed control of single electrons, and the precursor of switching devices and shift registers.

For each device, we wish to develop tools which will give quantitative results for;

- device operating parameters, and component values which optimise operation.
- device stability with respect to component deviation, external charge and quantum fluctuations.
- the effect of interdevice coupling or cross-talk.

The starting point for development of such system tools is a Monte Carlo modelling routine based on the work of Bakhavlov *et al.* [12]. As junction arrays and turnstiles are investigated with this routine it is modified and extended to form a far more useful set of modelling tools.
A detailed description of system building blocks, and the tools developed to study them, is given in chapter 5. Results from the application of these tools are noted in chapter 6.

CHAPTER 2 BACKGROUND

A historical overview of both theoretical and experimental work on granular electronics is given. Specific emphasis is placed on the methods by which Coulomb blockade effects are used to correlate and control electron tunnelling. The physical systems in which tunnelling occurs are discussed, and the possibility of using each as an integrable fabrication technology noted. Methods of constructing practical granular electronic systems are considered. Novel design and analysis tools will be needed to investigate such systems.

2.1 Historical Background

2.1.1 Coulomb Blockade

The origins of work on single electronic systems were experiments into the conduction of thin, granular metallic films; first in 1951 [15] and then again in 1962. Neugebauer and Webb [16] measured a suppression in the dc conductance of films at low temperature, and suggested the electric charging of film grains by discrete electrons as its source.

Grains can be considered as small electrodes linked by tunnelling junctions. If electrode intercapacitance is large, then conduction occurs, with the discreteness of tunnelling manifest as system shot noise [8]. For small electrode intercapacitance, the electrostatic energy of tunnelling,

$$E_c = \frac{e^2}{2C} \tag{2.1}$$

may be much greater than the thermal fluctuations of the system, which are of scale k_BT. This occurs at temperatures,

$$T \ll T_c, \qquad \text{where} \qquad T_c = \frac{e^2}{2k_BC} \tag{2.2}$$

(T_c is referred to as the *critical temperature*.) If in addition the tunnelling resistance of the potential barrier R_t, and any associated shunting resistances, are greater than the resistance quantum $R_Q = h/4e^2 \approx 6.45\ k\Omega$, then quantum fluctuations of the system will also be less than the energy scale E_c and a *Coulomb blockade* of tunnelling will occur. This blockade is only lifted if the electrostatic energy of tunnelling is

supplied by the potential drop across the junction, i.e for junction voltages above a threshold,

$$V_{thresh} = \frac{e}{2C} \tag{2.3}$$

(Table 2.1 gives estimates of the voltage, current and time scales associated with various values of junction capacitance, based on equations 2.1 - 2.3.)

Source	Junction Area S (nm^2)	Junction Capacitance C (aF)	Critical Temp. T_c (K)	Junction Resistance R (kΩ)	Voltage Scale V = e/2C (mV)	Current Scale I = V/R (nA)	Time Scale t = RC (ps)
(a)	100×100	300	3	100	0.25	2.5	30
(b)	30×30	30	30	100	2.5	25	3
(c)	10×10	3	300	100	25	250	0.3
(d)	100×100	20	46	1000	4	4	20
(e)	?	1000	0.9	340	0.08	0.2	340

Table 2.1 Estimates of tunnelling junction main parameters. Estimates (a-c) reproduced from [8] with $C = C_0S$ where $C_0 = 3\times10^{-6}$ F/cm^2, and R = 100kΩ, typical values for metal oxide barriers. (a) represents state-of-the-art junctions [17], (b) represents a record junction [14], and (c) represents the nanolithographic limit [18]. Estimate (d) calculated from L.S.Kuzmin, *et al.* [11] as typical of metal-insulator-metal junctions in 1-dimensional tunnelling junction arrays. Estimate (e) calculated from L.J.Geerligs, *et al.* [10] for metal-insulator-metal junctions in their gated turnstile device.

Despite extensive experimental work on such films [19], a detailed quantitative theory of the suppression based on multiple tunnelling events was not then derived, due to the random structure of the conducting grains. Recently there has been renewed interest in this field [20-22].

Further progress came with simpler systems that allowed more direct measurement of junction threshold voltage V_{thresh}. These structures, first studied by Zeller and Giaever [23] and then by Lambe and Jaklevic [24], consist of 'granular films' sandwiched between metallic electrodes. Each grain in the metallic film forms a two junction system between the macroscopic electrodes, the whole system acting as a two-dimensional parallel array of double junctions. A full theoretical analysis of such systems has been achieved [25].

2.1.2 Coulomb Staircase

Although these results gave direct experimental evidence of Coulomb blockade, it was not until 18 years later, in 1987, that techniques were refined enough to allow measurement of another predicted effect - that of the *Coulomb staircase* [14, 26].

Coulomb Staircase Theory :

This phenomenon is exhibited in double junction systems under voltage bias (for example, by *one* of the grains in the system of Zeller & Giaever mentioned above). The

parameters of such a system are shown schematically in figure 2.1. Its analysis requires consideration both of the discrete nature of electron tunnelling, and of the discrete charge within the central electrode of the device.

Assume initially that $C_1 << C_2$, $R_1 << R_2$ so that the tunnelling rate through the first junction is far greater than that through the second. Set the external bias conditions so that charge flow from left to right is preferred, and increase the bias voltage above the initial Coulomb blockade gap. The governing circuit equations are ;

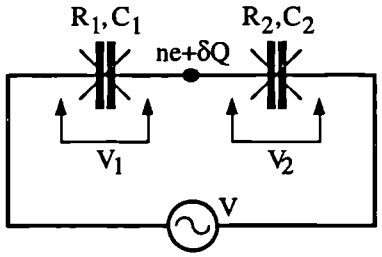


Fig 2.1 Equivalent circuit parameters of a double junction system under voltage bias. Modified capacitor symbols represent tunnelling junctions of capacitance C, resistance R. Charge on central electrode is ne+δQ.

$$V_1 = \frac{C_2}{C_1+C_2}V - \frac{ne+\delta Q}{C_1+C_2}$$

$$V_2 = \frac{C_1}{C_1+C_2}V + \frac{ne+\delta Q}{C_1+C_2} \qquad (2.4)$$

where $ne+\delta Q$ is the charge on the central electrode. This is the result of n electrons on the electrode due to tunnelling events, and an initial charge δQ due to external voltages coupled to the electrode via stray or gating capacitance.

For given external voltage V, electrons will tunnel onto the central electrode until V_1 becomes smaller than $e/(C_1+C_2)$, at which point the junction becomes Coulomb blockaded. Because of the tunnelling rate assumptions above, we may assume that this blockade condition is always reached before we need consider charge tunnelling out through C_2. Since the tunnelling rate through C_2 limits and governs the current through the device, and since V_2 is pinned by the blockade condition on junction 1, current through the device remains constant over a range of external V.

In order to raise the number of electrons contained in the central electrode by one, V_1 must be raised by $\Delta V_1 = e/(C_1+C_2)$, i.e,

$$\Delta V_1 = \frac{e}{C_1+C_2} = \frac{C_2}{C_1+C_2}\Delta V \quad \Rightarrow \quad \Delta V = \frac{e}{C_2} \qquad (2.5)$$

which in turn allows a current increase of,

$$\Delta I = \frac{\Delta V_2}{R_2} = \frac{e}{R_2(C_1+C_2)} \qquad (2.6)$$

Thus the IV curve of such a device shows distinct steps of width ΔV and height ΔI. As the junction parameters are brought nearer to $C_1 \approx C_2$, $R_1 \approx R_2$ and tunnelling rates through each junction become comparable, blockade conditions are less likely to build up, and the IV curve approaches linearity (although of course offset by the

Coulomb blockade voltage of $e/2(C_1+C_2)$). Detailed theory describing the double junction system is given in [27], with application of the theory to typical experimental conditions noted in [28].

Coulomb Staircase Observed :

Two methods were used to obtain measurement of the Coulomb staircase. The later experiment, performed by Barner and Ruggiero [26], studied Ag particles of mean diameter 7.5nm sandwiched between Cu or Ag films and separated from them by Al_2O_3 barriers. This was a refinement of the methods discussed above, and a schematic of the experimental device is shown in figure 2.2.

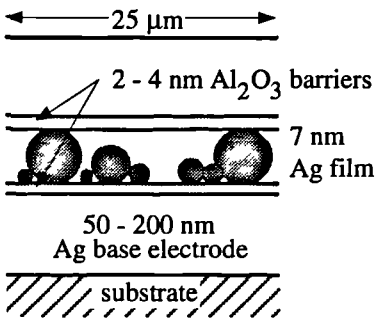


Fig 2.2 Cross section schematic of an array of double junctions formed by sandwiching a thin conducting film between two bulk electrodes [26]. In this case devices $(25\mu m)^2$ were used, with total resistance in the range 1-100MΩ.

The other method, due to Fulton and Dolan [14] used the techniques of electron-beam lithography to pattern sets of Al-Al_2O_3-Al junctions onto a silicon substrate. These structures exhibited single electron charging effects just as expected. Figure 2.4 shows the process by which the junctions were formed and notes the scales involved. These were the first artificially fabricated junction sets that allowed control over the position and capacitance of individual junctions.

2.1.3 Single Electronic Transistor

Theory of Operation :

At the same time as Coulomb staircase effects were being measured in the IV curves of double junction systems, the importance of the fractional charge δQ on device operation was being realised [29, 30]. Consider again the schematic of figure 2.1, with negligible external bias $V\approx 0$. The capacitive energy of the central electrode is,

$$E = \frac{(ne+\delta Q)^2}{2(C_1+C_2)} \qquad (2.7)$$

with n the net number of electronic charges which have tunnelled onto the central electrode above equilibrium, and δQ a fractional charge due to potentials coupled to the central electrode via stray capacitance. (Of course δQ may have any charge value, but $\delta Q \geq e$ will induce tunnelling events bringing the system to a new equilibrium condition, so only δQ of the order of e need be considered in practice.)

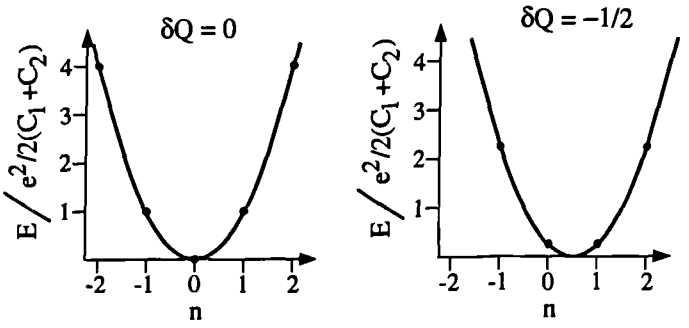


Fig 2.3 Energy diagram illustrating the effect of fractional charge on the central electrode of a double junction. Charge on the junction can only change by an integral amount, into the states marked by solid dots. For $\delta Q = 0,1,\ldots$ an energy barrier of at least $e^2/2(C_1+C_2)$ is encountered. For δQ = 'half integral' tunnelling can occur without experiencing a blockade effect.

Figure 2.3 shows the electrostatic energy of this central electrode as a function of n, for two limiting values of δQ. Note that because of the discrete nature of tunnelling only those energy states marked with solid dots are allowable. When $\delta Q = 0$ there is a tunnelling activation energy of $e^2/2(C_1+C_2)$. This is the normal Coulomb blockade effect. However, when $\delta Q = -\frac{1}{2}e$, the activation energy is reduced to zero, and charge transfer can occur without penalty. If it were possible to closely control the fractional charge on the central electrode of this double junction, then a switch or *single electronic transistor* could be formed. Coupling a gating voltage V_g to the electrode by way of a small non tunnelling capacitance $C < C_1,C_2$ is the simplest way of doing this, $q = CV_g$. It has also been suggested that 'trickling' charge onto the electrode by way of a high impedance resistor (forming a *resistive single electronic transistor*) may be an alternative [30]. Both capacitive and resistive single electronic transistors have now been fabricated and their transfer characteristics measured [31, 32]. The results of these studies are discussed below in §2.3.1.

Importance of Staircase and Transistor Effects :

These phenomena, the Coulomb staircase and single electronic transistor, are basic to the whole field of single electronics. Each relies both on the integral nature of tunnelling charge, and on the integral nature of charge on an isolated electrode. Firstly, the Coulomb staircase shows mutual correlation of junction tunnelling events. Such correlation effects are vital in governing and stabilising electron flow in extended systems. Conversely, the single electronic transistor shows the effect of externally controlled fractional electrode charge on the IV curve of a system. It is the basis of single electronic turnstile devices [9, 10], where a varying gate voltage provides detailed control of electron flow in a system of junctions.

This sensitivity to external charge is also the source of many of the problems encountered in systems of single electronic devices. For example the presence of random static charge trapped next to a single electronic transistor will introduce an indeterminate shift in its transfer characteristic along the V_g axis. This makes practical biasing of groups of such devices extremely difficult. Such problems are returned to in §2.3.1.

Validity of Theoretical Model :

A semiclassical model, describing not only the Coulomb staircase and single electron transistor, but general systems of tunnelling junctions, was derived from the basic quantum mechanics [8, 29, 30, 33, 34]. This theory is reviewed in [35] along with experimental results confirming its validity. It holds under two main assumptions. Firstly that thermal and quantum fluctuations are less than the characteristic energy scales of the junctions (i.e $R_t, R_{shunt} >> R_Q$ and $E_c << k_B T$). Secondly, that the relaxation time of the electromagnetic environment of any junction is much smaller than the time between subsequent tunnelling events. These conditions will be examined, and the theory described in detail, in chapter 4. They are found to apply in many metal-insulator-metal structures. This model is used as the basis for the simulation tools we shall develop.

2.1.4 Further Areas of Research

Since these foundational discoveries, progress in the field has been rapid and has taken a number of directions.

Extensions of the Theoretical Model :

Theoretically, several extensions to the semiclassical model have been made. Firstly, the effect of fluctuations in the external electromagnetic environment of junctions has been included [36-38]. Higher order tunnelling processes - *macroscopic quantum tunnelling* (MQT) or *electron cotunnelling* - have also been considered [13] and experimentally measured [39, 40]. In the literature, MQT often refers to tunnelling events occurring in a number of junctions simultaneously, bringing the system from an initial to final charge state by way of one or more virtual intermediate states which would not normally be energetically possible. This is an important 'killer' process in single electronic systems. Invariably, the virtual states through which macroscopic quantum tunnelling occurs are those states designed to be illegal in order for the system to operate properly. Extensions to the simple theory including quantum fluctuations and cotunnelling will be discussed in detail in chapter 4.

Possible Device Technologies :

Experimentally, following a suggestion by Mullen *et al.* [34], the Coulomb staircase was observed using a scanning tunnelling microscope (STM) imaging an In droplet above an Al-Al_2O_3 plane, with junctions formed across the oxide barrier and by the vacuum between the dot and STM tip [41]. The highest T_c values have consistently been measured by scanning tunnelling microscopy, with reports [42, 43] and later confirmation [3, 44, 45] of single electron tunnelling effects at room temperature. Junctions have been formed with $T_c \approx 1150$ K [3]. STM work is of particular use where it is possible to measure the Coulomb staircase *and* image the structures from which they derive [27, 46], thus comparing geometrical and measured capacitance.

Of greater interest for this work are fabrication approaches where integration is possible - i.e where it is possible to make some choice over both the value of junction parameters and how those junctions interconnect.
Initially, the fabrication of integrable systems relied upon the 'suspended resist' technique used by Fulton and Dolan [47]. As well as single and double junctions, systems comprising four gated junctions (electron pumps or 'turnstiles') [9, 10] and longer linear junction arrays [11, 48-50] have been fabricated. Studies in regular 2D arrays have also been reported [51, 52]. Indeed the field has progressed to the extent that design and construction of a single electronic current standard is already under way [53]. This work will concentrate on the modelling of metal-insulator systems.

However single electron charging phenomena are not confined to metal-insulator systems. Much present research is aimed at exploring charging effects in squeezed geometry, two-dimensional electron gas (2DEG) systems.
The periodic conductance oscillations characteristic of double junction single electronic transistors were first recognised in quasi-one-dimensional quantum wires by Scott-Thomas *et al.* [54]. Later, the same lithographic techniques were used to create devices which allowed the formation of small 'pools' of 2DEG (*quantum dots*) into which electrons could tunnel from larger 2DEG reservoirs [55]. These quantum dots are the analogue of the central electrode in metal-insulator-metal systems. Thus many devices fabricated using metal-insulator-metal technology can also be constructed as semiconductor devices.
Semiconductor systems are particularly convenient for research into single electronics because device parameters can easily be changed by variation of bias conditions. However this versatility is offset by complications due to the nature of electron transport in semiconductors. These complications are discussed in more detail in §2.2.2.
At present both single electronic transistors [56] and gated turnstile devices [57] have been demonstrated in 2DEG systems.

2.2 Fabrication Technologies

2.2.1 Metal-Insulator Technologies

Figures 2.4 to 2.8 describe schematically four fabrication approaches which allow the possibility of integrating systems of tunnelling junctions onto a single substrate. Figure 2.6 is an electron micrograph of an actual system, whose fabrication approach is shown schematically in figure 2.7.

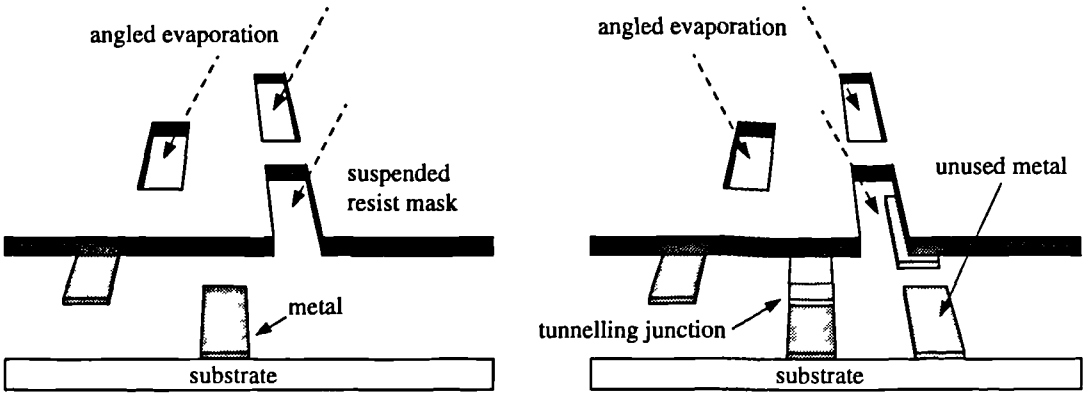


Fig 2.4 Processing steps involved in creating metal-oxide-metal tunnelling junctions. The technique was developed by Dolan [47] using photolithography, and extended for fabrication of Josephson junctions [58] and tunnelling junctions [14, 59] using e-beam lithography. The suspended mask is formed from a germanium layer deposited on top of a polymeric resist and then itself patterned. Some of the underlying polymer is removed with the germanium resist coating, forming the overhang. Oxidation between successive metal depositions forms the insulating tunnelling layer. Typical recorded junctions have side 30nm (i.e area 900nm^2) [14].

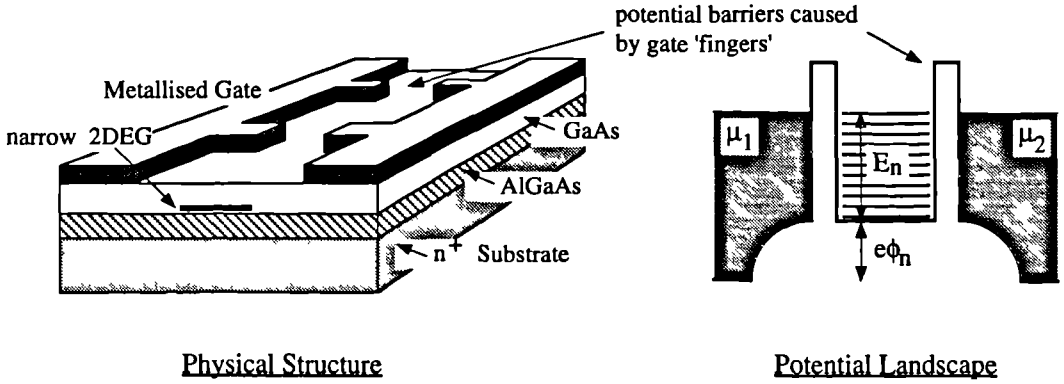


Fig 2.5 Laterally patterned two-dimensional electron gas in a semiconductor heterostructure, and schematic of the potential landscape along the narrow 2DEG (quasi-1DEG) channel in that heterostructure. The gate fingers induce an island or 'dot' of 2DEG separated from the end reservoirs by tunnelling barriers. The energy levels of this dot are discrete, unlike metallic electrodes where levels can be assumed to be continuous. μ_1 and μ_2 are the electrochemical potentials of wide two-dimensional electron gas reservoirs at each end of the structure. ϕ_n is the electrostatic potential of the dot containing n electrons, and E_n is the energy level of the nth electron in that dot. Potential landscape diagram based on [57].

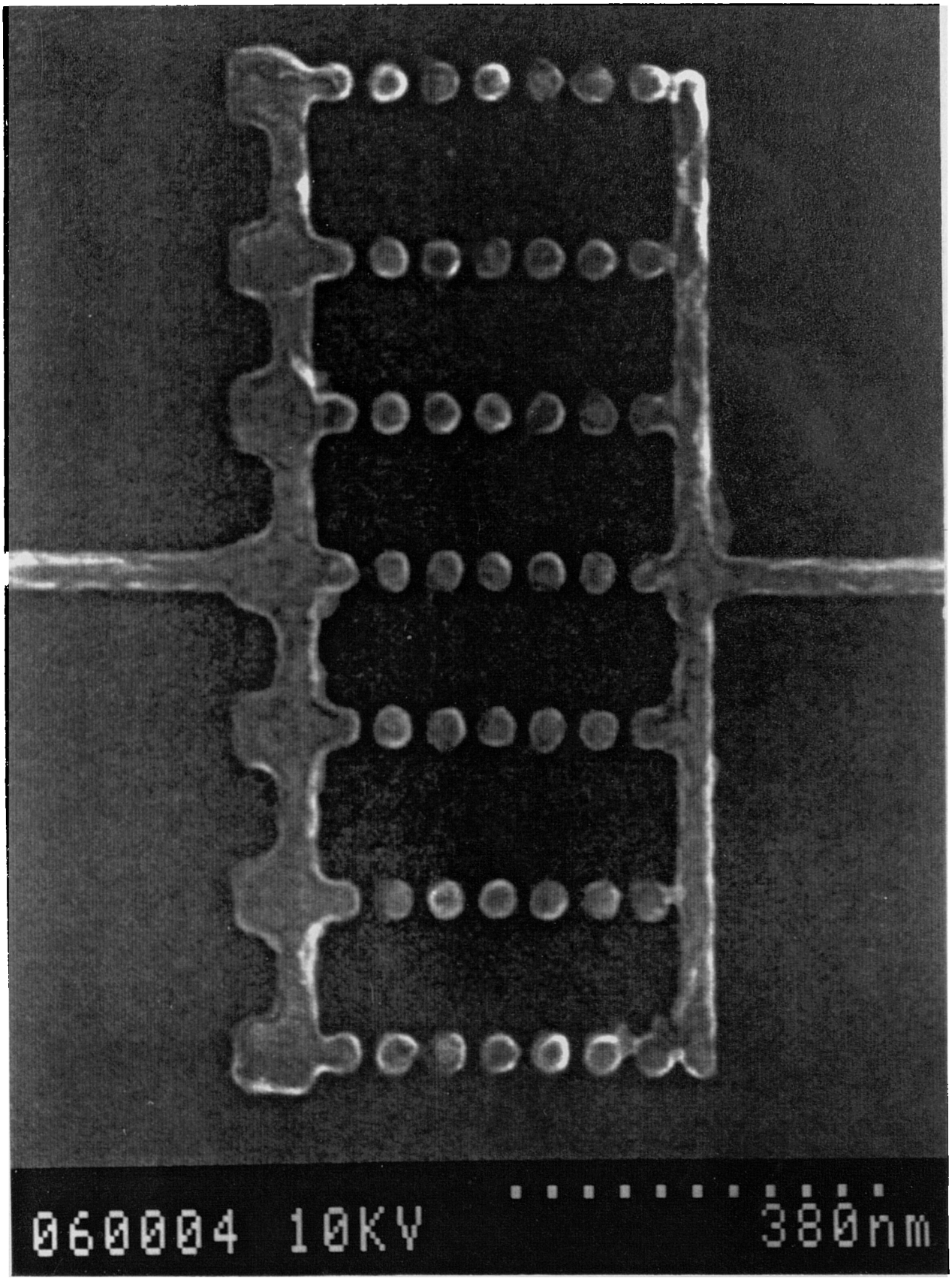


Fig 2.6 Electron micrograph of lateral metal-semiconductor-metal, Schottky dot device developed at Glasgow by Weaver *et al.* [60] (see figure 2.7 and text for description of junction operation). The device consists of six linear junction arrays arranged in parallel. Each linear junction array consists of 7 junctions. Results of the modelling of such a system are given in chapter 6.

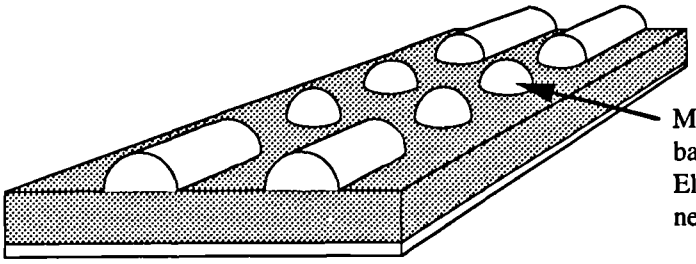


Fig 2.7 Lateral metal-semiconductor-metal, Schottky dot system developed at Glasgow (figure 2.6 shows an actual device viewed by electron microscope) by Weaver *et al.* [60]. Al dots are deposited on a p-type silicon substrate, forming Schottky contacts with it. Overlapping 'Schottky tunnelling tails' should permit electron tunnelling from dot to dot via the semiconductor. The high resolution lithography involves fewer processing steps than traditional 'suspended resist' methods and dots of 20nm radius and 12nm spacing have been demonstrated. Geometrical calculations including fringing fields estimate critical temperatures of up to $T_c = 75$ K [61]. Dots of < 5nm radius should eventually be possible.

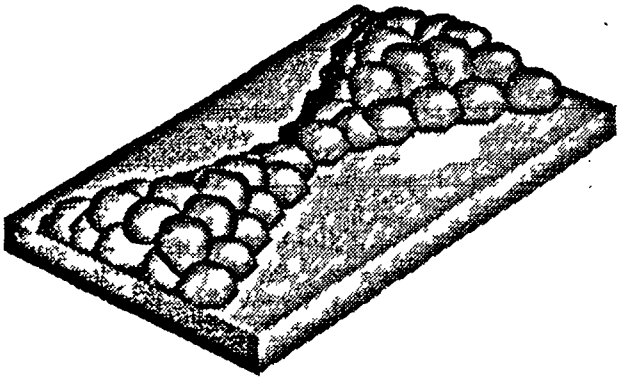


Fig 2.8 Schematic of controlled position, granular structure under development at Glasgow by Nicol [62]. Resolution limit electron-beam lithography is used to control the size and positioning of Al grains deposited on a silicon substrate. Charge transfer will take place by electrons tunnelling through grain oxide layers. The ideal situation is shown, a single grain-grain connection. Grain diameters of 10 - 30nm, each with a 3nm oxide layer, are possible. Geometrical calculations, including fringing fields, estimate critical temperatures for 30nm grains of $T_c = 130$K.

Hanging Resist Systems :

Figure 2.4 describes the 'hanging resist' technique devised by Fulton and Dolan [47]. The technique is well proven, and has been successfully used to fabricate a number of devices [9, 48, 49, 63]. At present it is the only proven method of producing metal-insulator-metal tunnelling junctions that are small enough to exhibit strong blockade effects and are integrable into multi-junction systems.

The disadvantages of the hanging resist process stem from its complexity. A number of exacting patterning, etching and evaporation steps are required. The initial design of the slotted mask (see figure 2.4) through which metallisations take place is intricate, and care must be taken with the placing of both junctions and unused metal. Finally, polymer thicknesses and evaporation angles place limits on the scale of possible structures. At present, typical junctions have capacitance from 2×10^{-16} F to 7×10^{-16} F, with grounding strays $C_0 \approx 2\times10^{-17}$ F and gating capacitances

$C_g \approx 5\times10^{-18}$ F [11]. Tunnelling resistances in the range 100kΩ to 1MΩ are common [49].
Such junction capacitances are equivalent to at best $T_c \approx 4.6$ K, which requires millikelvin temperatures for practical device operation (it will be shown in chapter 6 that practical operating temperatures need to be some 30 times lower than the T_c value). Obviously metal-insulator-metal junctions with capacitances closer to those of STM and granular systems would be more desirable.

Controlled Granular Systems :

Figures 2.7 - 2.8 describe fabrication approaches due to J. Weaver *et al.* [60] and J. Nicol [62]. These structures attempt to create the high T_c values of granular structures in a controlled and integrable fashion. They make use of ultra high resolution lithography techniques developed at Glasgow, and have the added advantage of requiring fewer processing steps than the hanging resist technology.
Figure 2.7 shows a metal-on-semiconductor, Schottky dot system. An essential feature of this system is that the 'tunnelling tails' of the Schottky islands overlap - thus permitting correlated tunnelling from dot to dot via the semiconductor. A full analysis of tunnelling capacitance requires knowledge of dot geometry, semiconductor doping levels, and the nature of both the metal-semiconductor interface and semiconductor surface. However simplified modelling of 20nm radius Al dots spaced 12nm apart on a silicon substrate suggest critical temperatures up to $T_c = 75$ K [61]. Dots of < 5nm radii and spacing should eventually be achievable [60].
Figure 2.8 shows a controlled granular structure under investigation by J. Nicol. Here a combination of resolution limit, electron-beam lithography and carefully controlled metal deposition is used to form a constriction in an Al wire. The ideal situation is shown in figure 2.8, where the apex of the constriction is made up of two Al grains, separated only by oxide layers. Charge transfer will then occur with electrons tunnelling across these oxide layers. Geometrical calculations estimate critical temperatures up to $T_c = 130$ K for grains of 30nm diameter (see chapter 3). It is estimated that grain diameters of 10-30nm are possible using present lithographic equipment [62]. Effective oxide thicknesses of 3nm are assumed.

Examples of both metal-on-semiconductor and controlled granular structures have been fabricated. An electron micrograph of the Schottky dot system (Al wires on a p-silicon substrate) is shown in figure 2.6. The IV curve of this set of 6 parallel junction arrays, each 7 junctions long, is modelled in chapter 6. If such structures are found to be experimentally viable, then it will be possible to construct practical metal-insulator-metal devices operating at liquid nitrogen temperatures.

2.2.2 Semiconductor Technologies

Reasons for Studying Charging Effects in Semiconductors :

As noted above, a great deal of present work concentrates on charging effects in semiconductor systems, particularly those in which a confined 'pool' of conduction electrons is produced. This is for three main reasons. Firstly, there is already a wide body of experience in the fabrication of such systems. Secondly the active region of such a device can usually be modified drastically by differing bias conditions, making it an ideal research platform. Thirdly, and most importantly, differences in electron transport between these and metal-insulator-metal devices give rise to novel device properties which require study.
A great deal of experimental work has been accomplished in the field [56, 64-67] and theories of varying detail developed [68-70]. However a modified semiclassical theory (developed for metal-insulator-metal systems, but including the *discrete energy* states of confined electrons) seems to fit well, even in small semiconductor devices where more detailed quantum mechanics suggests that its results will be invalid [4]. Experimental results such as these mean that semiconductor systems are still under active research.

Properties of Lateral Semiconductor Devices :

Two main classes of semiconductor system are important. Most common are laterally patterned devices, where a GaAs/AlGaAs heterojunction allows the accumulation of a thin, quasi two-dimensional layer of electrons (a 2-D electron gas or 2DEG). Metallised gates on the surface of the structure are then biased to deplete some regions of this 2DEG, leaving confined pools and reservoirs of electrons. Such a structure is shown in figure 2.5. Here electrons are effectively confined to a narrow channel down the centre of the device. The channel is itself pinched off by two sets of 'fingers', forming a pool or *quantum dot* of electrons between two reservoirs. This device is a first approximation to the double junction system of figure 2.1 with the quantum dot taking the place of the central metallic electrode. Variation of gate bias will change the size of the dot, and the width of the potential barriers between it and the 2DEG reservoirs. Different gate geometries should allow more complex integrated systems of junctions and electrodes.

The right hand diagram of figure 2.5 shows the potential landscape through the channel of the double junction device and indicates two main reasons why single electron charging phenomena in semiconductors and metals should differ.
We have so far assumed a semiclassical model of tunnelling, where only the discrete quantum nature of the electron was needed to explain experiment. However in semi-

conductor systems the Bohr radius a_B is large ($a_B \approx 10$nm for GaAs), and as such the energy level spectrum in a confined dot can no longer be considered as continuous. For small dots, this energy spacing ΔE_n may even be comparable to the charging energy scale $e^2/2C$. Figure 2.5 shows dot energy levels with 'half integral' ϕ_n (i.e the potential of the dot is such that Coulomb blockade is suppressed, as shown in figure 2.3 above). Even under these conditions strong conduction can only occur when a charge state E_n is appropriately aligned with the electrochemical potentials of the reservoirs. The change in dot potential needed to move from one conduction maximum to the next therefore becomes a combination of Coulomb and energy state spacings $\Delta V = e^2/C + \Delta E_n$.

A second complication arises because the Fermi energy in semiconductors may itself be comparable to the charging energy scale and the dot may not contain more than a few conduction electrons [70]. For a dot containing a few thousand free electrons ΔE_n can be assumed to be approximately constant over n, and the device will operate in a linear regime. However with few free electrons in the dot the differences between energy levels are more marked. Electron-electron interaction energies will vary strongly with the number of filled states, as will the distribution of confined charge for each state [71]. Indeed under these conditions the semiclassical model of an electron 'pool' with capacitive tunnelling junctions becomes increasingly invalid. It becomes more appropriate to think of a double barrier resonant tunnelling device with wide, low barriers and a central region containing trapped charge and scattering centres. A full quantum mechanical treatment, including the effect of the device fluctuation potential [72], becomes necessary to accurately predict experimental results.

A number of laterally patterned quantum devices have been fabricated with physical dimensions in the 0.5 - 1.0 μm range being common. Because of depletion, the quantum dots produced have diameters approximately 350 nm smaller [71], with dots as small as 100 nm in diameter being reported [67]. These smallest dots may contain fewer then 25 electrons. Dot capacitance is usually estimated by using the formula for the self-capacitance of a circular disc, $C = 4\varepsilon_0\varepsilon_r d$ [73], which gives good results for larger dots. Capacitance values are obtained experimentally by graphing the period of conductance oscillations versus gate voltage, using $\Delta V = e^2/C + \Delta E_n$. In general, single electron charging dominates the separation of energy levels in these systems, and so ΔE_n can be ignored when approximating C. Capacitance values in the region 2×10^{-16} F to 3×10^{-17} F have been observed [65, 71]. Recently sub 100 nm dots have been reported with $C \approx 5\times10^{-18}$ F (which implies a critical temperature $T_c \approx 370$ K) [74]. However this 'dot' was the result of an uncontrolled

artefact in the fabrication process of a device with nominally greater C, and would not be reproducible in integrated systems.

Properties of Vertical Semiconductor Devices :

The second class of semiconductor system in which Coulomb charging effects have been studied are the double barrier resonant tunnelling devices (DBRTDs). A generic DBRTD is shown in figure 2.9. The main difference between these and laterally patterned devices is of course the vertical conduction path, with tunnelling barriers being formed at fabrication by semiconductor heterostructures. A number of important properties then follow:

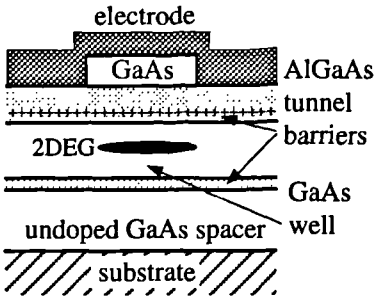


Fig 2.9 Schematic of a double barrier resonant tunnelling device. A thin potential well is formed between two AlGaAs tunnel barriers. Well extent is determined by the GaAs cap layer. Conduction is vertical. '+' represents delta doping in the top blocking barrier.

Firstly, device parameters cannot be varied after fabrication. This leads to less flexibility of operation, but it does allow those parameters to be measured and known far more accurately than with lateral devices. Secondly, device gating is difficult (although this has been done [75]) and this adds to the difficulties of integrating DBRTD systems.

Electrically, DBRTDs have all the complications of small, few electron, laterally patterned devices. It is relatively easy to produce size quantisation between tunnelling barriers so that $\Delta E_n \approx e^2/2C$. This complicates the measured charging effects on device conductance. With no applied voltage, there is no free charge in the 'dot' between tunnelling barriers. For small n each ΔE_n and charging energy will then vary markedly. Finally, DBRTDs by their very nature are designed to avoid scattering between the tunnelling barriers. They retain phase information in the tunnelling electron wavefunction and require conservation of both energy and momentum [71].

All of these factors suggest that charging effects in DBRTDs should vary markedly from the predictions of simple Coulomb blockade theory.

The experimental evidence [71, 75-77] does show blockade effects, with estimated dot capacitances of $C \approx 3\times10^{-17}$ F. However, further work is required before systematic agreement between experiment and present theory is obtained.

Advantages / Disadvantages of Semiconductors for Single-electronic Systems :

To summarise, semiconductor systems seem to have two main advantages over metal-insulator-metal devices. Smaller capacitance values can presently be produced, and lateral devices have a flexibility that makes them ideal for research.

They also have a number of complications, due to quantum effects (size quantisation and finite number of free carriers) which can be ignored in present metallic systems. These perturb device operation to a greater or lesser extent, and further research is needed to fully characterise them. However, experimental results show that even when these effects are present, devices still approximately obey simple Coulomb blockade theories - there is no catastrophic breakdown of charging effects. It is reasonable to assume that practical single electronic systems could be fabricated even allowing for these further quantum complications.

Finally, there are a number of major problems which have to be overcome in order to produce practical single electronic systems in semiconductor materials. These mainly concern unwanted charge and its effects on the system. The effect of external charge states has already been mentioned above. Single electronic systems are *extremely* sensitive to stray external charge (this is precisely the reason that they have been suggested as the basis for high sensitivity electrometers [53]). Any unwanted fixed charge will perturb the biasing of semiconductor systems, and varying charge (from trapping-detrapping events for instance) can produce unwanted gating effects destructive to system operation. Much of the work of single electronic systems is in fact aimed at designing systems resistant to stray charge. As noted in this section, impurities in tunnelling electrodes themselves also cause problems, perturbing conduction. These impurities frequently occur in experimental systems [75, 77]. Single electronics system design must assume that such impurities will occur in any practical systems and design circuits which minimise their effect.

It should be noted that, notwithstanding these problems, several results first obtained in metallic systems have been demonstrated in semiconductor devices - including a functioning gated turnstile device [57], and the observation of electron cotunnelling [78].

2.3 System Properties

2.3.1 Analogue Systems

Capacitive and Resistive Single Electronic Transistors :

The idea of using single electronic devices as components in more complex systems was raised in early theoretical work describing Coulomb blockade effects [29]. Initially it was envisaged that single electronic transistors could be used for the processing and amplification of both analogue and digital signals.

Figure 2.10 shows a single electronic transistor formed from a double junction system and gated through a small non-tunnelling capacitance C_o. The voltage gain, given by,

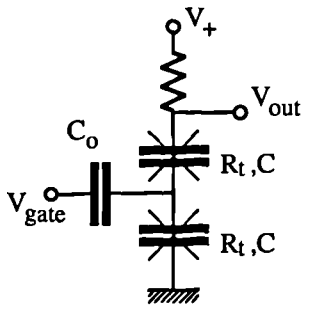


Fig 2.10 Circuit schematic of a capacitive single electronic transistor (C-SET). The resistive single electronic transistor (R-SET) is identical apart from a resistance R_o in place of C_o.

$$K_v = \left| \frac{\partial V_{out}}{\partial V_{gate}} \right|_{I = const} \tag{2.8}$$

can be analysed using standard semiclassical theory, and is found to be close to C_o/C [30]. However, in order to avoid undue sensitivity to noise at the gate electrode, C_o/C cannot be raised much higher than unity. In practice, therefore, voltage gains of $K_v \approx 0.35$ are typical [79]. Another problem with this *capacitive single electronic transistor* (C-SET) is that of the initial charge on the gated electrode. The transfer characteristic of the device is periodic in V_{gate}, with period e/C_o. Any fractional charge on the gated electrode (due to random impurities or external potentials coupled by strays to the electrode) effectively biases the C-SET at a random point within this transfer characteristic. In highly integrated circuits it would be impossible to trim each C-SET individually. Because of the low K_v, using feedback to provide stability is also impracticable.

To overcome the difficulties in using the C-SET we consider the *resistive single electronic transistor* (R-SET). Here a high impedance resistance R_o is used in place of the gating capacitance C_o to trickle charge into the central electrode. The rate of charge flow to the electrode is given by,

$$\delta\dot{Q} = \frac{V_{gate} - V_{electrode}}{R_o} \tag{2.9}$$

where $V_{electrode}$ is itself a function of δQ, determined by standard semiclassical theory. Analysis [30] shows a well defined transfer characteristic, independent of any initial electrode charge and with high K_v. Electrically, the only advantage of the C-SET is its almost infinite input impedance at low frequencies.

There is, however, a major practical problem with the R-SET. To be effective, its gate resistance must be larger than the resistances of the tunnelling junctions, and must occupy a small enough area of substrate to avoid large stray capacitance. Resistances of the order of $M\Omega$ in μm^2 areas are required. Present thin film resistances do not yet achieve this goal [37]. One suggested work-around is to use an array of tunnelling junctions as a high impedance gate resistance [32]. An R-SET can be formed by this technique, but the threshold voltage of the junction array interferes with the operation of the device and at present the highest voltage gain obtained is $K_v = 0.85$. There is as yet no clear solution to the physical problem of creating R-SET gating resistances.

Summary of C/R-SET Properties :

Thus the fabrication difficulties of R-SET devices, and the gain and biasing difficulties of C-SET devices, mean that neither is a likely candidate for large scale integrated systems processing analogue data. The processing of digital data, if attempted using the 'transistor-like' action of R & C-SET devices, will also be possible only for low scale integration.

2.3.2 'Digital' Systems

Another way to use tunnelling junctions in digital systems is to make use of the integral nature of electron tunnelling directly. Here the presence or absence of excess charge on a metallic electrode (due to tunnelling events from or to it) may be used to represent digital bits. We refer to this 'digital' use of Coulomb blockade effects as *single electronic logic*. This is opposed to the term *granular electronics* which covers all devices whose operation relies on the integral nature of charge.

Benefits of Single Electronic Logic :

Such a use of double junction devices turns out to be directly analogous to an effect in Josephson Junctions - that of the movement of magnetic flux quanta in double junction superconducting quantum interferometers [30]. These systems have been widely studied, and considered as the basis for logic elements in digital systems [80]. The mathematics governing both types of system is very similar, indeed a simple set of transforms (given in Table 2.2) relate the equations governing both effects.

Single Electronic Tunnelling Devices		Superconducting Quantum Interferometer Devices
charge Q	↔	flux ϕ
electronic charge e	↔	flux quantum ϕ_o
voltage V	↔	current I
capacitance C	↔	inductance L
resistance R	↔	conductance G
series connections	↔	parallel connections

Table 2.2 Electromagnetic duality transformations relating the operation of single electronic devices with those of Josephson Junction based superconducting quantum interferometer devices [30]. The same form of equations governs both systems, so that results derived for one set of devices will, on transformation, apply to the other.

In particular, circuits developed for the *resistive single flux quantum logic* (RSQL) family using Josephson Junctions [5] transform directly into single electronic logic circuits (Some examples are given in [8]). These include both combinatorial logic and memory elements. Some of the benefits obtained by using this approach to the processing of digital signals are outlined below [81];

- Performance : device speed is ultimately governed by system RC time constants, and immunity to thermal noise by how far the operating temperature is below $T_c = e^2/2k_BC$. Both these qualities improve as device size reduces. Table 2.1 gives some 'handhold' figures for RC & T_c.
- Logic regeneration : because device operation is governed by the tunnelling of discrete charges, there is no degradation of the digital signal and logic 'regeneration' is automatic.
- Fabrication tolerances : unlike waveguide interferometer switches, the separation and height of tunnelling barriers need not be carefully controlled. Thus devices are thus relatively insensitive to poorly controlled aspects of fabrication such as barrier thickness.
- Energy dissipation : the speed-power product of single electronic logic is substantially better than any of the present logic families. The single electronic transistor power-delay product is of the order of k_BT_c. Record metal-insulator-metal junctions may have $T_c \approx 30$ K (see table 2.1), or 2.5 meV. If stable, room temperature single electronic logic requires $T_c \approx 9000$ K, this still gives ≈ 0.75 eV. This compares with complementary metal-oxide silicon (CMOS) technology, $\approx 10^{10}$ eV, and single flux quantum logic, $\approx 10^4$ eV. Single electronic transistors thus easily break the 1 fJ barrier of 6×10^3 eV.

From these benefits, it appears that single electronic logic may allow the fabrication of extended digital systems operating under low power, at room temperature, with fine stability to thermal fluctuations and fabrication imperfections. In order to produce

such systems, the fabrication technology must deliver integrable, ultra small junction capacitances (<< 1 aF for room temperature operation). The technology must also allow the careful control and elimination of unwanted stray charge. As shown in §2.2, both metal-insulator-metal and semiconductor fabrication technologies are at present an order of magnitude outside the 1 aF barrier. Both technologies offer the possibility of good integrability. Semiconductor systems seem to present the greater problems when trying to control unwanted charge.

2.3.3 Unanswered Questions

Independent of whatever fabrication technology is used to construct single electronic devices, there are a number of important questions still to be researched. Most link to the problems of uncontrolled stray charge, but it is also necessary to consider system stability, signal input/output, and the effect of higher order tunnelling processes on system performance. We summarize some of these questions below;

- What effects on system operation are caused by the presence of stray external charge? How does such charge effect the bias of electrodes? Can systems be designed which are resistant to such charge? Answers to these questions will indicate what level of shielding is required between and around single electronic systems and devices.
- What are the particular effects of non-static charge on system operation? This could be caused by; external noise coupled through strays, charge trapping-detrapping in the devices themselves, or the movement of charge in other parts of an extended system (cross-talk). What shielding methods or reduction in device density might be required to counteract these problems? Again, can systems resistant to these effects be constructed.
- What are the effects on system operation of variation in system components? No fabrication process is ideal, and there will always be a spread of component parameters around their nominal values. How critical are these values to correct system operation?
- Under what external biasing does ideal system operation occur? How can systems be designed which operate correctly under a wide range of biasing conditions?
- What levels of thermal and quantum fluctuations cause system breakdown?
- When digital signals are processed by single electronic systems what level of processing errors is likely? How do these error rates relate to the magnitude of thermal and quantum fluctuations, component variation and the presence of static and non-static stray charge?
- How can input/output (I/O) operations be performed on single electronic systems?

- How will higher order tunnelling processes (i.e macroscopic quantum tunnelling or electron cotunnelling) effect single electronic systems? What effect will such processes have on the 'bit error rates' of a system?

2.3.4 The Need for Modelling Tools

The purpose of this work is to develop new tools for the design and analysis of single electronic systems - tools which will allow some of the above questions to be answered for specific systems, and which will aid in the design of systems resistant to the stray charge based problems mentioned above.

It would be convenient if it were possible to answer some of the above questions by simple analytic results, even if such results only approximated device properties. This is sometimes possible (for instance in Chapter 3 various analytic approximations to the capacitance of a tunnelling junction are offered and compared).
However, in the majority of cases no simple analytic results can be obtained. This is due in part to the complexity of single electronic systems, but also because the equations describing their operation must describe both continuous (charging) and discrete (tunnelling) processes.
As an example of this, Appendix A describes an elementary stability analysis of tunnelling junction arrays. The stability of such an array to perturbations in its capacitance values is discussed (an important question given the impossibility of perfect fabrication methods). The theory can adequately describe such arrays when no tunnelling takes place. However, when discrete tunnelling events are included, the governing equations become non-autonomous and the problem highly non-trivial.

Thus, our tools emphasise computer modelling for the investigation of general single electronic systems. Equivalent circuits of each physical system may be constructed, and modelling used to discover how each physical parameter effects its operation. In this way we expect to answer some of the questions noted above.

The remainder of this work concentrates on system equivalent circuits; how their component values are obtained, how charge tunnelling rates within them are calculated, and the computer programs used to model their action. Initially, these tools are applied to the simplest systems of single electronic logic, tunnelling junction arrays. They are then improved and extended to deal with more complex systems including electron turnstiles and coupled devices.

CHAPTER 3 ANALYSIS OF DEVICE GEOMETRY & CAPACITANCE

This chapter considers in detail the calculation of junction and grounding capacitance for tunnelling junctions and electrodes based on their physical geometry. Such results are necessary if accurate equivalent circuits of single electronic systems are to be constructed. The value of analytic capacitance estimates based on simplified geometries is discussed, and some of the formulae in common use considered. The intercapacitance of two metallic spheres surrounded by dielectric shells is derived. Comparisons are made between this result and parallel plate or spherical capacitor estimates.

3.1 The Need for Analytic Capacitance Calculations

3.1.1 Analytic Solution Versus Finite Element Methods

There are two main reasons for performing geometrical calculations of the capacitances involved in a single electronic system.
Firstly, to allow effective comparison between experimental results and theoretical predictions. Obviously, the more accurate the geometrical estimate of junction and stray capacitances in a system, the better chance of making useful comparison with experimental results.
Secondly, to be able to obtain 'working estimates' of capacitance quickly and easily. These give experimentalists a simple indication of probable device operating parameters and help in deciding whether a device would be feasible given limitations in material properties and fabrication techniques. They may also help in choosing which devices to model more precisely if more accurate models are not available, or are computationally expensive.

Advantages of Finite Element Calculation :

In order to make accurate predictions of junction capacitance, the geometry of the system must be well defined, and some form of finite element solution of the electrostatic field equations (i.e Laplace's equation) used. The materials and geometry of any real system make direct analytic derivation of these equations impossible in practice. Such finite element calculations are being performed for the metal-semiconductor-metal Schottky dot system under development at Glasgow. The work has been under-

taken by Asen Asenov using a computer model originally developed for work on MESFETs and HEMTs [82]. A sample of the results obtained is shown in figure 3.1. The model is of particular use in metal-semiconductor-metal systems as it includes the presence of donor and acceptor states in the semiconductor substrate and surface pinning states. Both of these can modify junction and grounding capacitances, increasing them by up to 25% [61].

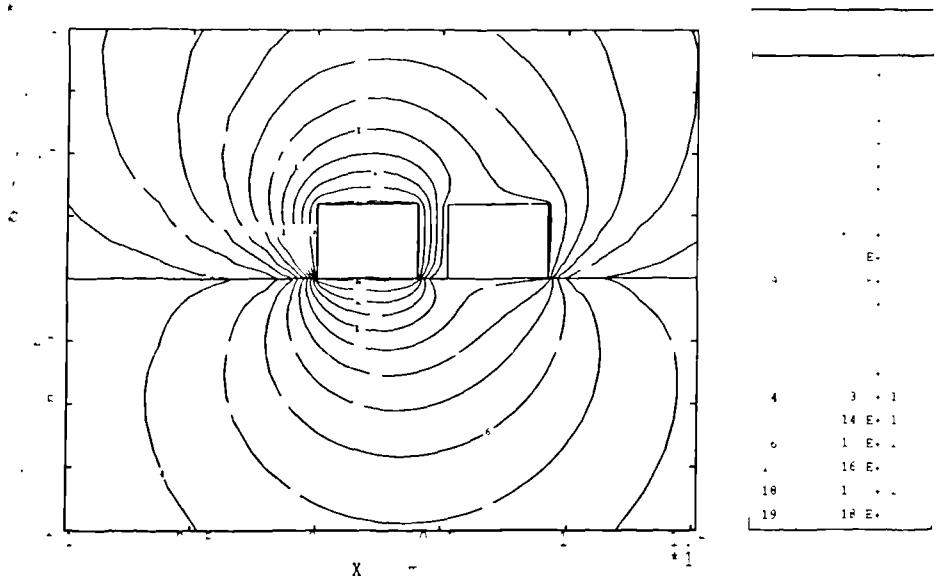


Fig 3.1 The electric potential surrounding two aluminium wires on a silicon substrate - modelling work done by A. Asenov using the model of [82]. The wires are 40nm wide and spaced 12nm apart on a p-silicon substrate 250nm deep. Calculations based on these modelled potentials yield an intercapacitance of 8.0×10^{-13} Fcm^{-1} with a capacitance to ground of 15.0×10^{-13} Fcm^{-1}.

Figure 3.1 shows the solution of a two-dimensional problem. The majority of real-life problems also have small size (and therefore large fringing fields) in the third dimension. Work is presently under way developing full three-dimensional solvers.

Advantages of Analytic Solution :

One method of obtaining a working estimate of the junction or grounding capacitance of a device is to analytically solve for the capacitance of a simpler approximate geometry. Although not requiring the accuracy of a finite element calculation, an analytic approximate solution must have two main qualities in order to be useful. It must firstly be easy to calculate - ideally a relatively simple formula that requires only a hand calculator. Secondly, it must represent all the important physics of the problem. For instance, small tunnelling junctions are often approximated by the common 'parallel plate' capacitance formula $C = \varepsilon_0\varepsilon_r A/d$, where A is the area and d the distance between capacitor plates, ε_0 the permittivity of free space and ε_r the relative permittivity of the dielectric medium between the plates. This formula does

not take account of fringing fields at the edges of capacitor plates. For small junctions these fringing fields will make a major contribution to the final capacitance value. A solution which ignores these fields is ignoring an important part of the problem.

This chapter will be mainly concerned with deriving analytic results which allow easy capacitance calculation for simple geometries - results that can be used as tools in approximating the capacitance of more complex systems.

3.1.2 Geometrical Idealisations

Common Geometrical Idealisations :

As noted in Chapter 2, single electron tunnelling effects have been shown to occur in many fabrication systems, including; thin granular films [20, 26], scanning tunnelling microscopy on small metallic grains [41, 46] and hanging resist fabricated metal-insulator-metal structures [11, 14, 49, 83]. Blockade effects have even been measured in thin crossed wires held touching by magnetic fields [84]. A range of approximation techniques for the calculation of junction capacitance in these devices has been used. The geometry of the system is idealised so that a simple analytical result applies. The major geometrical idealisations are shown in table 3.1.

Capacitance of Common Geometric Idealisations

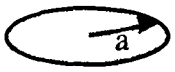
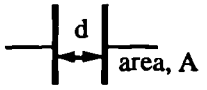
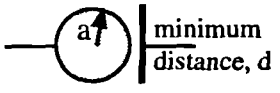
description	formulae	diagram
self capacitance of a conducting sphere	$C = 4\pi\varepsilon_0 a$	
self capacitance of a thin conducting disc	$C = 8\varepsilon_0 a$	
parallel plate capacitor	$C = \frac{\varepsilon_0 A}{d}$	
sphere/plane capacitor	$C = 2\pi\varepsilon_0 a \ln[(a+d)/d]$ $a >> d$	

Table 3.1 Formulae for the common geometric idealisations used to estimate junction and electrode capacitances in the literature. All formulae assume the conductors are in vacuo, with the permittivity of free space represented by ε_0. Note the diagram for the sphere/plane formulae is not to scale, as the formula holds only for $a >> d$.

In granular film or scanning tunnelling microscope approaches it is usual to make idealisations based on spherical geometries [26, 46]. However in the 'lithographic' approaches (e.g hanging resist structures) it is more common to find parallel plate

calculations [11, 49]. Although the junctions are plate-like in nature, the inaccuracy caused by neglecting fringing fields becomes proportionally larger as plate area reduces. This gives values for junction capacitance far smaller than are possible in practice. In turn, estimates of T_c for ultra small junctions (such as those given for the smallest junctions of table 2.1) are exaggerated. Even when the geometry of a small device is a good approximation to parallel plates we consider it more useful to apply a spherically based formula, if by that method fringing fields are accounted for.

Idealisations Used in Lateral Semiconductor Systems :

Note that in the above discussion semiconductor systems have been ignored. This is because of the added complications of such systems mentioned in §2.2.2. In practice, quantum dots in 2DEG containing a large number of free electrons are usually modelled by using the formulae for the self-capacitance of a thin conducting disc. In some cases even parallel plate approximations have been used [85]. However, it is more difficult to define a capacitor 'geometry' for systems with few free electrons. As the number of electron states changes in such a device, both the effective size of the dot and charge distribution will vary. Therefore the results of this chapter will apply mainly to metal-insulator-metal devices.

Idealisations for Controlled Granular Systems :

As has been noted above, two novel fabrication approaches for single electronic devices have been developed at Glasgow. These make use of ultra high resolution nanolithography, in an attempt to create controllable junctions with capacitances as small as those in granular systems. They are shown in figures 2.6 - 2.8. Consideration of these structures leads to the geometric idealisation of figure 3.2.

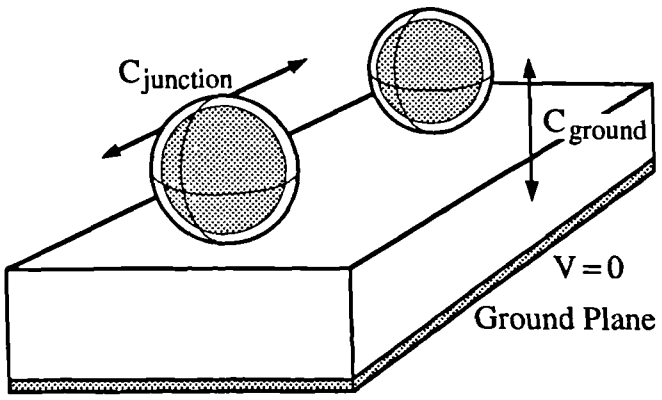


Fig 3.2 Geometrical idealisation of experimental tunnelling devices built at Glasgow, including that of figures 2.7 and 2.8. The diagram shows two aluminium spheres with dielectric (aluminium oxide) shells atop an insulating substrate backed by a ground plane. The two capacitance values of interest are indicated.

If analytical solutions to the capacitance values of this idealisation could be found, they would allow simple characterisation of the Glasgow devices. Solutions would also provide capacitance estimates for other metal-insulator-metal devices where junction size is small enough for fringing effects to dominate.

Unfortunately there is no coordinate system which will allow full solution of the capacitances of figure 3.2, but use of bispherical coordinates does allow partial solutions. $C_{junction}$ can be found if the ground plane is moved far from the spheres (the problem simplifies to that of two lone spheres). C_{ground} can be found if one sphere is moved to ∞, and the insulating substrate is assumed to pervade all space (the problem simplifies to that of two lone spheres, with the radius of one $\rightarrow \infty$).

The rest of this chapter deals with solutions to the geometry of figure 3.2, and comparison between them and the formulae of table 3.1.

3.2 Analytic Solutions

3.2.1 Spherical Conductor with Dielectric Shell [86, p. 109,316]

In a spherical coordinate system the solution to Laplace's equation is of form, $\phi = R(r)\,\Theta(\theta)\,\Psi(\psi)$

where $\Psi = A\,\sin q\psi + B\,\cos q\psi$

$R = A\,r^p + B\,r^{-(p+1)}$

$\Theta = A\,P_p^q(\mu) + B\,Q_p^q(\mu)$

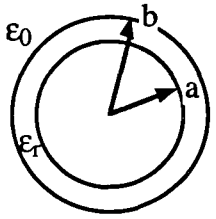


Fig 3.3 Schematic of a metal sphere surrounded by a dielectric shell, and sitting in a medium of dielectric constant ε_o.

Symmetry considerations give ϕ independent of θ, ψ.
Therefore $q = p = 0$
This gives a general solution, $\phi = A + B/r$

For a sphere with no dielectric shell, applying the boundary conditions $\left.\begin{matrix}\phi=V \text{ at } r=a\\ \phi=0 \text{ at } r=\infty\end{matrix}\right\}$

gives solution $\phi = \dfrac{Va}{r}$.

Obtain $\mathbf{E} = -\text{grad}\phi = -\mathbf{e}_r \dfrac{\partial\phi}{\partial r} = \mathbf{e}_r \dfrac{Va}{r^2}$ $(r > a)$ with $\mathbf{D} = \varepsilon_0\mathbf{E}$,

and the charge on the sphere $Q = \int_S \mathbf{D}.d\mathbf{S} = 4\pi\varepsilon_0 aV$

(considering a Gaussian surface just outside the sphere)

Therefore the capacitance of the sphere is $C_{sphere} = \dfrac{Q}{V} = 4\pi\varepsilon_0 a$ (3.1)

The capacitance of the shell is found similarly, using conditions $\left.\begin{matrix}\phi=V \text{ at } r=a\\ \phi=0 \text{ at } r=b\end{matrix}\right\}$,

to obtain $C_{shell} = 4\pi\,\varepsilon_0\varepsilon_r \dfrac{ab}{b-a}$ (3.2)

To get the total capacitance, we note that $\mathbf{E}$ is always perpendicular to the dielectric surface through symmetry, so that $C_{total}^{-1} = C_{sphere}^{-1} + C_{shell}^{-1}$
Therefore,

$$C_{total} = 4\pi\,\varepsilon_0\varepsilon_r \frac{ab}{b-a(1-\varepsilon_r)} = 4\pi\,\varepsilon_0\varepsilon_r\, a \frac{1}{1-\frac{a}{b}(1-\varepsilon_r)} \qquad (3.3)$$

This somewhat trivial example indicates clearly each stage in the capacitance calculation. First Laplace's equation is separated in the coordinate system of choice. Then symmetry considerations are used to find the simplest possible general solution. Finally boundary conditions are invoked to solve for the potential.

Once this potential function is obtained, it can be used to find a form for the **E** field at any point, and then this is used to find the charge on the conductor as a function of conductor voltage. Hence $C = Q/V$.

The method can now be applied to more complex problems.

3.2.2 Two Conducting Spheres Surrounded by Dielectric Shells

Bispherical Coordinates :

In order to deal with the potential field created between two spheres, a bispherical coordinate system is required. Figure 2.4 shows the relation between bispherical coordinates (η,θ,ψ) and Cartesian coordinates (x,y,z).

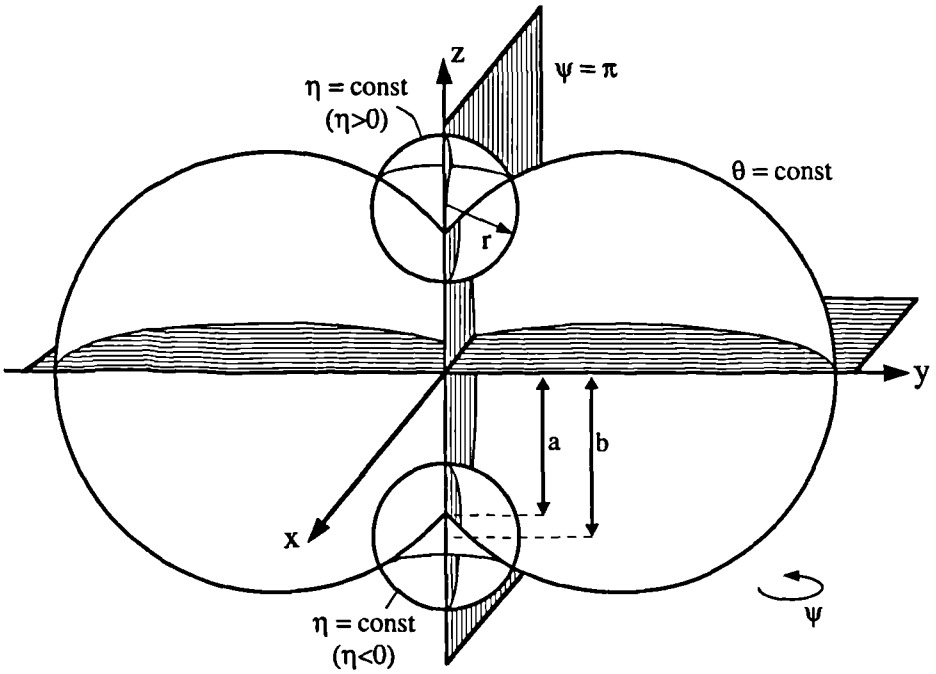


Fig 3.4 Bispherical Coordinates. Orthogonal surfaces are spheres (η=const), 'apple' or 'spindle' shaped (θ=const), and half planes (ψ=const). As $\eta \to \infty$ the spheres approach the plane z=0. $\theta = \pi/2$ is a sphere centred on the origin, and $\psi = 0$ is the half plane y=0, x>0. From [87]

The coordinate system defines as η = const a set of spheres above and below the $z = 0$ plane. Each sphere has radius r and centre at (0,0,b) in (x,y,z) coordinates, where,

$$r = a\,\mathrm{csch}\eta, \qquad b = a\coth\eta \tag{3.4}$$

with 'a' a constant of the coordinate system. Unfortunately it is impossible to fully separate Laplace's equation in bispherical coordinates, but it can be *R-separated* [88]. This procedure is given in Appendix B, and results in a potential,

$$\phi = (\cosh\eta - \cos\theta)^{1/2}\, H(\eta)\, \Theta(\theta)\, \Psi(\psi) \tag{3.5}$$

with general solutions of the form,

$$\Psi = A \sin m\psi + B \cos m\psi \tag{3.6a}$$

$$H = A\, e^{(p+1/2)\eta} + B\, e^{-(p+1/2)\eta} \tag{3.6b}$$

$$\Theta = A\, P_p^m(\cos\theta) + B\, Q_p^m(\cos\theta) \tag{3.6c}$$

Solution of Charge on Two Conducting Spheres with Dielectric Shells :

Figure 3.5 shows how the problem of two conducting spheres - surrounded by dielectrics of arbitrary thickness and dielectric constant - is set up. A solution is obtained by finding the potential functions ϕ_i in the three regions of differing dielectric constant ε_i, each region requiring a superposition of two fields ϕ_i^{I} and ϕ_i^{II} (one to deal with each boundary condition). These functions are then matched by equations governing continuity of **E** and **D** across dielectric boundaries.

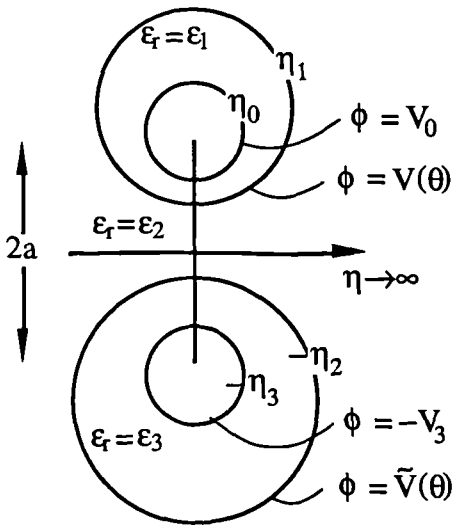


Fig 3.5 Schematic representation of two metal spheres surrounded by dielectric shells and sitting in a dielectric medium.

Note that because of the nature of bispherical coordinates, if the boundaries of the dielectric shells and metal spheres are taken at constant η values, they will only be concentric as $\eta \to 0$. This concern is dealt with in §3.3.2.

The involved algebraic manipulations required to solve this problem are set out in detail in Appendix C. The final solution is complex and unwieldy. In essence we obtain a value for the charge on the top conductor,

$$Q^{top} = \sum_{n=0}^{\infty} Q_n^{top} \qquad \text{where } Q_n^{top} \text{ is an integral function of } V_0, V_3$$

and likewise for the bottom conductor. The equation $Q^{top} = Q^{bot} = Q$ must then be used to solve for the voltages, from which the capacitance $C = Q/(V_0+V_3)$ follows

immediately. In practice this is algebraically difficult. In order to get a more useful outcome it is necessary to simplify the problem, introducing more symmetries into the mathematics in order to allow algebraic cancellation.

3.2.3 Two Equal Conducting Spheres

Firstly, the intercapacitance of two metallic spheres is derived, as a simplification of the formulae of Appendix C. (See figure 3.6.)

The geometry of this problem is defined by $\eta_3=\eta_0$ and $\eta_2=\eta_1$. From the symmetry of this configuration it can be seen that $Q^{bot} = Q^{top} = Q$ and that $V_3 = V_0 = V$. Finally $\varepsilon_3 = \varepsilon_2 = \varepsilon_1$, and without loss of generality all these relative permeabilities can be set to unity, taking into account the dielectric media solely through ε_0.

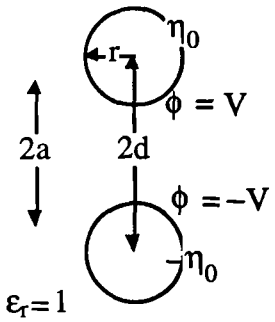


Fig 3.6 Schematic representation of two equivalent metal spheres.

Substituting these simplifications into equations C.32 and C.33, Q can be obtained as a summation of terms (substituting $\zeta = n+1/2$),

$$Q_n = 2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I}\, (\cosh\eta_0-\mu)^{-3/2}\, \frac{1}{2} \sinh\eta_0\, d\mu \; + \tag{3.7}$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I}\, (\cosh\eta_0-\mu)^{-1/2}\, \zeta \coth[\zeta(\eta_0-\eta_1)]\, d\mu \; +$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I}\, (\cosh\eta_0-\mu)^{-1/2}\, \frac{\zeta \operatorname{csch}^2[\zeta(\eta_0-\eta_1)]\, \chi}{-\chi^2 + \operatorname{csch}^2[\zeta 2\eta_1]}\, d\mu \; -$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu) A_n^{1I}\, (\cosh\eta_0-\mu)^{-1/2}\, \frac{\zeta \operatorname{csch}^2[\zeta(\eta_0-\eta_1)] \operatorname{csch}[\zeta 2\eta_1]}{-\chi^2 + \operatorname{csch}^2[\zeta 2\eta_1]}\, d\mu$$

where,

$$\chi = \coth[\zeta 2\eta_1] + \coth[\zeta(\eta_0-\eta_1)] \tag{3.8}$$

and,

$$A_n^{1I} = V(n+1/2) \int_{-1}^{1} P_n(\mu)\, (\cosh\eta_0-\mu)^{-1/2}\, d\mu \tag{3.9}$$

this simplifies to,

$$Q_n = 2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I}\, (\cosh\eta_0-\mu)^{-3/2} \{ \tfrac{1}{2}\sinh\eta_0 + (\cosh\eta_0-\mu)\,\zeta \coth[\zeta\eta_0] \}$$

(3.10)

From Appendix D we have equations D.14a,b (for $\eta_0 > 0$),

$$\int_{-1}^{1} P_n(\mu)\, (\cosh\eta_0-\mu)^{-3/2}\, d\mu = \frac{\sqrt{2}}{\alpha\beta} (\cosh(n+1/2)\eta_0 - \sinh(n+1/2)\eta_0)$$

$$\int_{-1}^{1} P_n(\mu)\, (\cosh\eta_0-\mu)^{-1/2}\, d\mu = \frac{\sqrt{2}}{n+1/2} (\cosh(n+1/2)\eta_0 - \sinh(n+1/2)\eta_0)$$

where $\alpha\beta = \sinh(\eta_0/2)\cosh(\eta_0/2) = \frac{1}{2}\sinh\eta_0$. Substituting these into equation 3.7 it is found that after trivial cancellation;

$$Q_n = 2\pi\varepsilon_0 a\, A_n^{1I}\, \sqrt{2} \;/\; \sinh(n+1/2)\eta_0 \qquad (3.11)$$

Furthermore, from equation 3.9 and D.14b we have,

$$A_n^{1I} = V(n+1/2) \int_{-1}^{1} P_n(\mu)\, (\cosh\eta_0-\mu)^{-1/2}\, d\mu$$

$$= \sqrt{2}V\{\cosh(n+1/2)\eta_0 - \sinh(n+1/2)\eta_0\} \qquad (3.12)$$

The two results immediately above solve the problem of finding the charge Q on either one of two congruent metallic spheres knowing the potential ±V on each of the spheres. Q is merely the summation over of all n contributions Q_n.

To find the intercapacitance of such spheres, note that the potential difference between them is 2V, and employ C = Q/(2V)

$$C = \sum_n \frac{Q_n}{2V} = \sum_n \frac{2\sqrt{2}\pi\varepsilon_0 a}{\sinh(n+1/2)\eta_0} \frac{\sqrt{2}V(\cosh(n+1/2)\eta_0 - \sinh(n+1/2)\eta_0)}{2V}$$

$$C = \sum_n 2\pi\varepsilon_0 a \{ \coth(n+1/2)\eta_0 - 1 \} \qquad (3.13)$$

3.2.4 Conducting Sphere and Plane

We next solve the problem of the intercapacitance of a metal sphere placed above an (infinite) metal plate, as shown in figure 3.7.

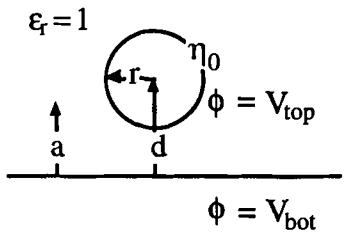


Fig 3.7 Schematic representation of a metal sphere and metal surface.

Geometry is now defined by $\eta_3 \rightarrow \infty$ and as previously, it is assumed that $\varepsilon_3 = \varepsilon_2 = \varepsilon_1 = 1$, an assumption which will again lead to the cancellation of η_1 and η_2 from the equations. However, Q^{bot} and Q^{top} must be calculated separately, as the symmetry assumed earlier has been broken.

By substituting these simplifications into equations C.32, C.33 and C.36, and then using equations C.19, C.21 and D.14b precisely as in the above problem;

$$Q_n^{top} = 4\pi\varepsilon_0 a\,(V_{top} + V_{bot})\,\{\,\coth(n+1/2)\eta_0 - 1\,\} \tag{3.14}$$

$$-Q_n^{bot} = 4\pi\varepsilon_0 a\,V_{top}\,\{\,\coth(n+1/2)\eta_0 - 1\,\} + 4\pi\varepsilon_0 a\,V_{bot}\,\{\,\coth(n+1/2)\eta_0 + 1\,\} \tag{3.15}$$

The condition $Q_n^{top} = -Q_n^{bot}$ is satisfied if $V_{bot} = 0$ which gives,

$$Qn = 4\pi\varepsilon_0 a\,V\,\{\,\coth(n+1/2)\eta_0 - 1\,\} \tag{3.16}$$

where V is the potential difference between the sphere and the plate. The resulting capacitance is found by employing C = Q/V,

$$C = \sum_n 4\pi\varepsilon_0 a\,\{\,\coth(n+1/2)\eta_0 - 1\,\} \tag{3.17}$$

Note that this result can alternately be found by realising that the $\eta \rightarrow \infty$ plane of the above problem is at zero potential and has E field with zero θ component. Charge and potential values are then obtained from the above problem by the method of images [86, p. 101].

3.3 Comparison of Solutions

3.3.1 Spheres without Dielectric Shells

Comparison with Parallel Plate Approximations :

In order to compare the various capacitance estimates that might be made for systems like that of figure 2.7 or 2.8, the graphs of figures 3.9 and 3.10 were calculated. Figure 3.9 shows the intersphere capacitance versus separation for two 10nm radius metallic dots, calculated using four estimation formulae. The solid line uses the 'two spheres' formula derived above. We assume this to be the most accurate estimate, since it most closely fits the geometry of the system (i.e it only assumes perfectly spherical spheres with no oxide layers and ignores the substrate). The straight dashed line is half the self capacitance of a 10nm metallic sphere, to which the 'two spheres' curve approaches as $d \rightarrow \infty$. The other curves are given by the two parallel plate estimates shown in figure 3.8.

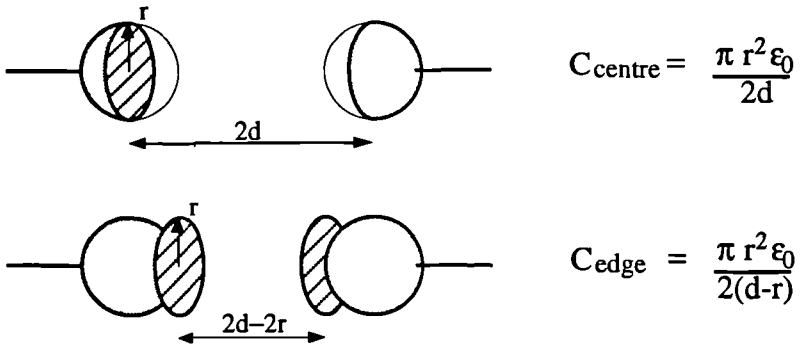


Fig 3.8 Schematic representation of two methods of approximating the capacitance between two spheres. Method one imagines two parallel discs of identical radius to the spheres at the centre of each sphere and uses the 'parallel plate' formula. Method two is similar, but imagines the discs to be as close as possible while still touching the spheres.

Figure 3.10 shows the results of figure 3.9 in different form, graphing the ratio of the parallel plate to 'two spheres' estimate as a function of dot separation.

Note also that the actual separation of electrodes in a tunnelling junction is governed by the need for a finite tunnelling resistance. A balance needs to be made between low junction capacitance and finite tunnelling currents. The form of $C_{twoSpheres}$ helps to show this relation. Scaling the geometries of devices produced at Glasgow would place them approximately in the area $12nm < d < 14nm$ on this graph (although obviously the absolute capacitance values would be different).

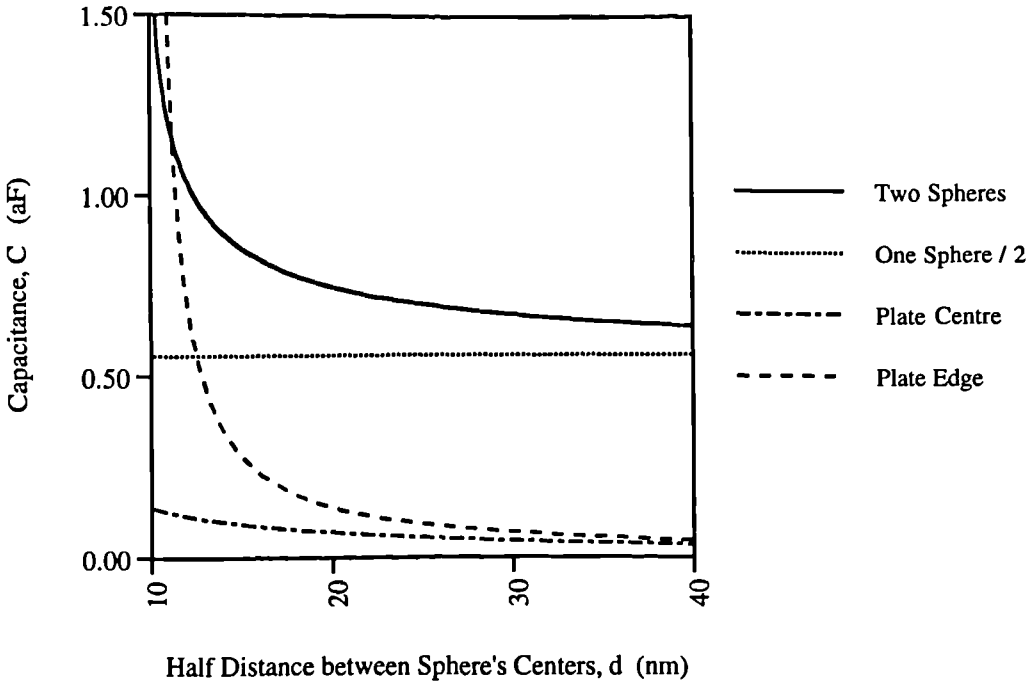


Fig 3.9 Capacitance versus intersphere Distance for two 10nm radius metallic spheres in vacuuo. The 'two spheres' solution solves the problem using a formula derived above. 'one sphere' is the capacitance of a single isolated sphere, while 'plate centre' and 'plate edge' are the parallel plate capacitor approximations, C_{centre} and C_{edge} in figure 2.8

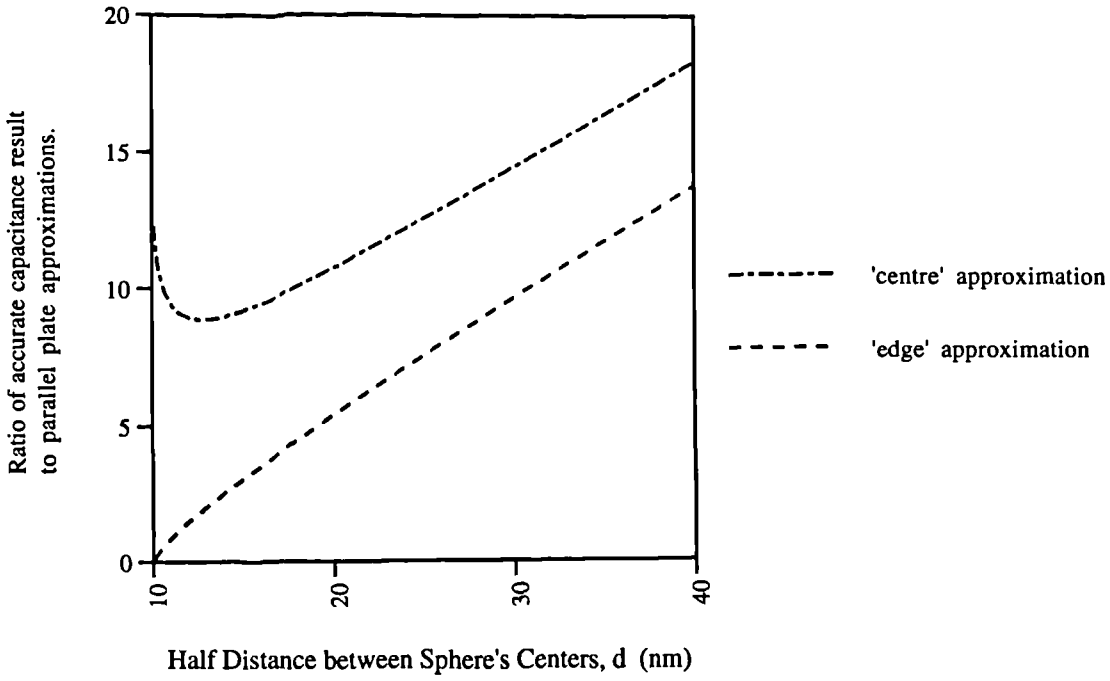


Fig 3.10 Ratio of 'parallel plate' Capacitance to 'two spheres' Capacitance versus intersphere Distance for two 10nm radius metallic spheres in vacuuo. The 'centre' and 'edge' approx's are calculated from the parallel plate capacitor formulae of figure 2.8 and apply to C_{centre} and C_{edge} respectively.

Results of Comparison with Parallel Plate Approximations :

It is obvious that the parallel plate formulae give capacitance values which are, in general, at least an order of magnitude lower than the 'two spheres' result. This is due to omission of fringing fields in such calculations. Even when the value for C_{edge} does approach that of $C_{twoSpheres}$ the ratio of the two is changing so rapidly with separation that it can not be considered a reliable approximation.

We conclude that the parallel plate approximation is not a good method for obtaining realistic estimates of junction capacitance for proposed ultra small tunnelling junctions. Indeed half the capacitance of a lone sphere in space turns out to be the best simple approximation for $d > 2r$, while none of the approximations considered here closely mirror $C_{twoSpheres}$ for $r < d < 2r$.

Considering again the $C_{twoSpheres}$ and C_{edge} curves of figure 3.9 at low values of d, it can be seen that the curves cross at $d \approx 11$nm. This is the point at which (in parallel plate type junctions) the parallel plate component of capacitance outweighs that of fringing fields. This suggests that when the ratio of plate radius to plate separation distance in a parallel plate capacitor exceeds ≈ 5, fringing effects can no longer be ignored. Of course this is a broad rule-of-thumb. To give a detailed analysis of the effect of fringing fields on capacitance values would require more detailed finite element modelling

Comparison with other Spherically Based Approximations :

In the literature there are three spherically based geometrical idealisations explicitly mentioned. Two [26, 46] are based on the sphere/plane formula noted in table 3.1. This requires $d/r > 100$ for accuracy, being derived for calculations on large, closely spaced grains, and is not applicable to any of the lithographically fabricated devices being investigated at present. The other [20] is based on a treatise on granular systems by Abeles *et al.* [19]. This result is actually equivalent to equation 3.13, with the disadvantage of a far slower convergence rate. More than twice the number the expansion terms are needed for a given accuracy, which makes it of less use for simple hand calculations. Table 3.2 indicates the convergence rate of equation 3.13.

Half distance between sphere's centres, d (nm)	Number of terms for accuracy better than 1%
> 50	1
17 - 50	2
13 - 17	3
12 - 13	4

Table 3.2 Rate of convergence of equation 3.13 for two metal spheres of 10nm radius.

Comparison with 2-Dimensional Finite Element Calculations :

Finally we consider how these results compare with the finite element calculations carried out by Asen Asenov (see §3.1). These were based on 20nm radius metal hemispheres fabricated on a silicon substrate, approximated by the geometry of figure 3.1. Table 3.3 lists $C_{junction}$, C_{ground} and $C_{ground}/C_{junction}$ for this model, and other approximation methods. The ratio $C_{ground}/C_{junction}$ is found to be a critical value in the operation of actual devices, see section §5.1.3. The 'coaxial cable' approximation uses the formula for the capacitance per unit length of coaxial cable,

$$C = \frac{2\pi\varepsilon_o}{\ln(b/a)} \quad \text{per unit length} \tag{3.18}$$

(with 'a' and 'b' the radii of the inner and outer conductors respectively) to estimate the capacitance to ground of one of the conductors. Both this and the finite element models are two-dimensional in nature.

Approximation Method	$C_{junction}$ (aF)	C_{ground} (aF)	$C_{ground}/C_{junction}$
Parallel Plate/Coaxial Cable (40nm length)	0.88	9.6	10.8
Finite Element Simulation (40nm length)	3.2	6.0	1.9
Two Metal Spheres (ignoring Substrate)	1.9	2.3	1.2
Spheres with Substrate	12.3	27.6	2.2

Table 3.3 Summary of capacitance approximations for 20nm radius aluminium hemispheres 12nm apart on a 250nm silicon substrate. The 2-D simulation is that of figure 3.1, choosing a wire length of 40nm (and ignoring fringing in the third dimension). The spheres calculation assumes 20nm radius spheres buried half deep in the substrate. Calculations for C_{ground} assume that the substrate pervades all space.

From this table the importance of fringing fields can again be seen. As the number of dimensions considered is raised ('parallel plate' is a 1-D solution, 'finite element' 2-D and 'spheres with substrate' 3-D), further fringing is included. The estimations of $C_{junction}$ and C_{ground} in turn are raised by a factor of $\times 3$ to $\times 4$. Much of this increase is due to the high permittivity of the silicon substrate. Forming metallic electrodes on top of etched pillars of silicon may allow the junction capacitances to be reduced further. A junction capacitance of 12.3 aF is equivalent to $T_c = 75$ K. The wide discrepancy between the estimated $C_{ground}/C_{junction}$ ratios should also be noted. The importance of this ratio, and the need for an accurate indication of its value is one compelling reason for the use of more sophisticated approximation techniques.

3.3.2 Spheres with Dielectric Shells

Calculation of Capacitance for Spheres with Dielectric Shells :

The geometry of the problem of two identical metal spheres surrounded by equal dielectric shells is defined by; $\eta_3 = \eta_0$ and $\eta_2 = \eta_1$ with $\varepsilon_3 = \varepsilon_1$. Unlike the analysis of 'bare metal' spheres, it proves impossible to produce a concise simplification of equations C.32, C.33 and C.36 under these conditions. The equations are, however, amenable to numeric solution - and a commercial symbolic or numeric mathematics computer package such as [89] can easily produce solutions to any required degree of accuracy, each data point taking only a few seconds.

An example of such numerical results is show in figure 3.11. This figure graphs the capacitance between two metallic spheres of radius 10nm, enclosed in dielectric shells 1nm thick at their thinnest point and of relative permittivity $\varepsilon_r = 10$. Two other results are noted for comparison. The first is the capacitance of the spheres without the dielectric shells (using the result of equation 3.13). The other is a hybrid result, calculating the capacitance of two metallic spheres whose radius is such that at large inter-sphere distances their capacitance equals that of 10nm spheres with 1nm dielectric shells. The reason for such a hybrid result is discussed below.

Complications Due to the Nature of Bispherical Coordinates :

As mentioned in §3.2.2, one problem with the nature of bispherical coordinates is that spheres of constant η are only concentric as $\eta \rightarrow 0$. If a dielectric shell is chosen to have thickness of 1nm at it's closest point to the sphere and is described by 'η = const' then its thickness will get steadily greater as we move away from this point. Both the thickest and thinnest points on the shell are found on the z-axis in figure 3.4.

The variation of these thicknesses as a function of sphere separation is shown in figure 3.12. Here the limiting boundary points of both sphere and shell are graphed as we keep the thinnest part of the shell at 1nm. It can be seen that the problem becomes extreme as the distance from sphere to origin becomes comparable to the radius of the sphere itself. Under these conditions the calculations give an overestimate of the real capacitance. Unfortunately this is the region of most interest for practical devices.

Validity of the Results :

Note that for regions where the shell is thickest the electric flux density is also the lowest (i.e the area farthest from the second sphere). These regions will have the smallest contribution to the final capacitance value. This suggests that the 'sphere plus shell' calculations should give a close upper limit to the true capacitance, and as such

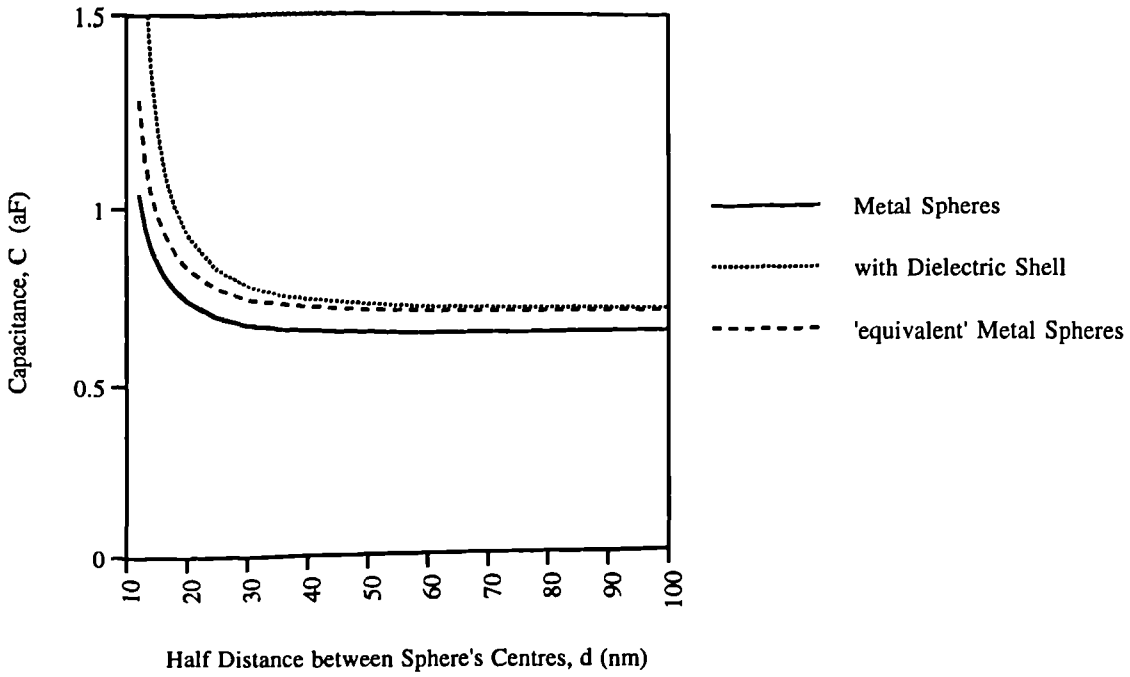


Fig 3.11 Capacitance versus intersphere Distance for metallic spheres in vacuuo. The 'Metal Spheres' case is calculated from the analytic solution for spheres of 10nm radius. The case 'with Dielectric Shell' solves for 10nm radius spheres with a dielecric shell minimum thickness 1nm. The 'equivalent Metal Spheres' case solves for metal spheres whose radius is such that their capacitance is equal to the 'with Dielectric Shell' case for large intersphere distance. A relative permittivity ε_r=10 is assumed for the shells.

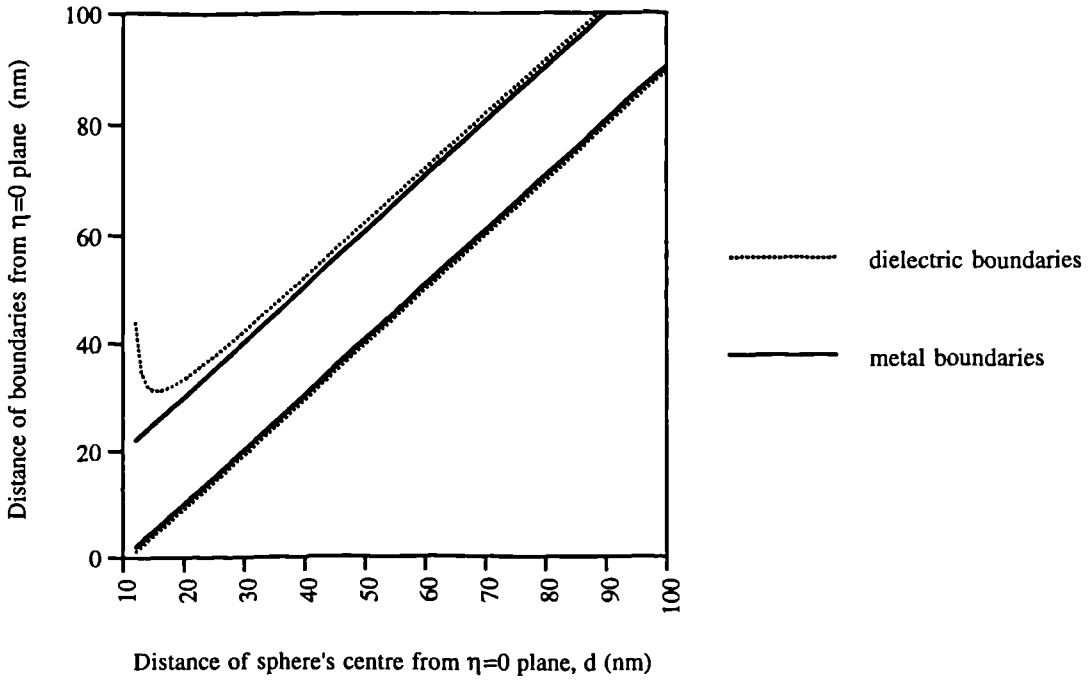


Fig 3.12 Boundaries of a 10nm metallic sphere and dielectric shell versus the distance of the centre of the sphere from the $\eta \to \infty$ (i.e z=0) plane. To perform useful capacitance calculations in a bispherical coordinate system the shell must be defined by 'η = some constant' and we require the shell to be 1nm thick at its closest point to the $\eta \to \infty$ plane. The form of the coordinate system forces the thickness of the shell to vary elsewhere, reaching maximum thickness furthest from the $\eta \to \infty$ plane. These limiting boundaries are shown above as systems of differing distance from the $\eta \to \infty$ plane are considered.

a useful limit to the operating parameters of fabricated tunnelling devices. A lower limit to junction capacitance is given by the simple metal spheres solution.
The hybrid result was chosen as an alternative estimate for very thin shells. It holds when the dielectric shell is thin enough (or of low enough relative permittivity) that the flux lines passing through it remain almost normal to its surface. Both the hybrid result and 'spheres plus shells' calculations agree as $\eta \rightarrow 0$. If greater accuracy at larger η is needed, only finite element numerical results will suffice.

3.4 Summary of Results

Various geometric idealisations of single electronic systems have been considered. These were used to develop simple analytic formulae for the capacitance of ultra small tunnelling junctions. For ultra small devices, spherically based formulae have an advantage over the more usual parallel plate approximations. This is because they include the important contribution of fringing fields. Simple formulae (3.13, 3.17) have been derived as excellent approximations for particular granular devices under study at Glasgow. They are more complex than parallel plate approximations, and require four or five terms of summation to give useful accuracy for spheres close together. However, they have the advantage of being accurate over all intersphere distances. They provide a first order estimate of physical capacitance without the need for computationally intensive numerical work.
Extensions of these analytic formulae, of particular applicability to spheres enclosed in dielectric shells (i.e. oxide layers), have been investigated. Intrinsic problems in the model (due to the nature of bispherical coordinates) have been noted. However, as a first order estimate of capacitance the results are still of value - particularly for spheres with relatively thin shells.

Further work in this area requires the development of three-dimensional finite element models of real systems. This will allow comparison of our analytic approximations with more precise results, and give a better indication of their usefulness.

CHAPTER 4 THEORETICAL MODELS OF TUNNELLING JUNCTION OPERATION

Before considering the tunnelling of single electrons through systems of junctions it is necessary to gain a sound understanding of the models used to describe the tunnelling of electrons through single junctions. One successful approach to modelling the action of discrete tunnelling through capacitive junctions is due to Averin & Likharev [29], elaborated and discussed in [8, 30, 33]. We give a brief summary of this microscopic model and its resultant governing equations. We also consider extensions to these results that look at tunnelling in an attendant electromagnetic environment - models due to Cleland *et al.* [37, 90] and Nazarov [38, 91-93]. In each case we need to know;

- a form for $\Gamma^{\pm}$ the tunnelling rate through a junction,
- the limits of applicability of the model,
- how the single junction model extends to systems of junctions.

This will give a firm theoretical basis to the modelling tools that we shall develop to analyse systems of such junctions.
Finally macroscopic quantum tunnelling is considered, and its implications for system operation are discussed.

4.1 Tunnelling Junctions - Microscopic model [29]

4.1.1 Derivation of Governing Equations

The equivalent circuit of figure 4.1 is studied, consisting of a current source I(t) with associated shunt resistance R_S, in series with a junction of tunnelling resistance R_t, and capacitance C.
(As $R_S \rightarrow \infty$ or 0 the junction can be considered either as perfectly current or voltage biased.)

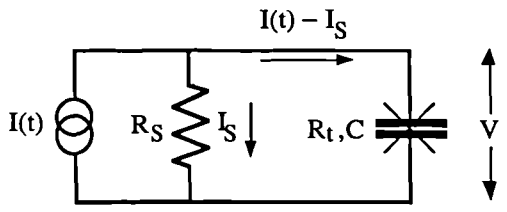


Fig 4.1 Single tunnel junction of capacitance C, and tunnelling resistance R_t with its associated driving circuit.

One way of writing the Hamiltonian of this system is;

$$H = H_1 + H_2 + H_S + H_T + \frac{Q^2}{2C} + \{I_S - I(t)\}\phi \tag{4.1}$$

where H_1, H_2 & H_S describe the energy of internal degrees of freedom in the junction electrodes and shunt resistance of the source. H_T is the tunnelling Hamiltonian and $Q^2/2C$ describes the charging energy of the junction. The final term is the interaction of the junction with charging current, with;

$$\phi \equiv \int V\,dt = \int Q/C\,dt \tag{4.2}$$

The tunnelling Hamiltonian can be expressed in a microscopic approach, by;

$$H_T = H_+H_-, \qquad H_- \equiv H_+^\dagger \tag{4.3}$$

where H_+ is represented by a summation of creation and annihilation operators acting over all states within the two electrodes of the junction.

$$H_+ = \sum_{k1,k2} T_{k1k2}\, c_{k1}^\dagger\, c_{k2} \tag{4.4}$$

Since these creation and annihilation operators describe the electrons in the junction electrodes, it is possible and useful to describe the charge operator Q (used in the final two terms of 4.1) by summations of them;

$$Q = -\frac{e}{2}\left(\sum_{k1} T_{k1k2}\, c_{k1}^\dagger\, c_{k1} - \sum_{k2} T_{k1k2}\, c_{k2}^\dagger\, c_{k2} \right) + \text{const} \tag{4.5}$$

Having specified the operators, commutation relations between them are sought. From [94, p. 113] we obtain,

$$[\phi,Q] = i\hbar \tag{4.6}$$

and from consideration of the microscopic results in equations 4.4 and 4.5 it is found that, for any function f(Q),

$$H_\pm f(Q) = f(Q\pm e)\, H_\pm \tag{4.7}$$

this result automatically implies that H_1, H_2 do not commute with Q. If, however, it is assumed that each electrode has a large number of states, so that expected charges have negligible effect on the internal properties of the electrode, then,

$$[H_{1,2},Q] \approx 0 \tag{4.8}$$

is a reasonable approximation, and with equations 4.6 and 4.7 allows analysis of the density matrix, without recourse to microscopic calculation. The condition of a large number of available states close together is characteristic of metal electrodes, for which this model would be expected to perform well (and indeed does, e.g [14, 27, 49]), and the tools developed below are primarily designed for such systems. However, as mentioned in §2.2.2, the simple semi-classical theory of Coulomb blockade is surprisingly useful in explaining effects in conducting islands with as few as 100 electrons [4].

Further simplification of this microscopic model is possible if the quantum fluctuations in junction and shunt circuit are smaller than the order of the charging energy, i.e,

$$G_S, G_t << R_Q^{-1}, \qquad R_Q \equiv \frac{h}{4e^2} \approx 6.45\ k\Omega \tag{4.9}$$

These conditions are met in the metal-insulator-metal fabrication approach by careful control of metal oxide layer growth in the fabrication process, and careful design of the physical circuit used to drive the junction (for instance by driving through high impedance thin film leads [36, 37]).

This simplification leads to the description of the model as 'semi-classical'. Under these conditions the density matrix diagonalises, and the time evolution of charge in figure 4.1 can be described by a classical probability density $\sigma(Q,t)$, governed by;

$$\frac{\partial \sigma}{\partial t} = -I(t)\frac{\partial \sigma}{\partial Q} + F_T + F_S \tag{4.10a}$$

$$F_T(Q) = \Gamma^+(Q-e)\sigma(Q-e) + \Gamma^-(Q+e)\sigma(Q+e) - [\Gamma^+(Q) + \Gamma^-(Q)]\sigma(Q) \tag{4.10b}$$

$$F_S = \frac{G_S}{C}\frac{\partial}{\partial Q}\left(Ck_BT\frac{\partial \sigma}{\partial Q} + \sigma Q\right) \tag{4.10c}$$

an extension of the Fokker-Plank equation of the system [95] including a tunnelling term.
The tunnelling rate of electrons changing the initial junction charge Q (assuming in this instance a voltage biased junction), is given by,

$$\Gamma^{\pm}(Q) = \frac{\Delta E^{\pm}}{e^2 R_t}\left[1 - \exp\left(-\frac{\Delta E^{\pm}}{k_B T}\right)\right]^{-1} \tag{4.11}$$

where $\Delta E^{\pm}$ is the change of free energy of the circuit due to the tunnelling event. In this case,

$$\Delta E^{\pm} = \frac{e}{C}\left(\frac{e}{2} \pm Q\right) \tag{4.12}$$

Figure 4.2 shows graphically how equations 4.10 and 4.11 apply to a single tunnelling junction. First, assume that no current flows in the external circuit, and there exists a nominal charge, Q_o, on the junction electrodes. The probability distribution in σ is then centred on Q_o, with spread dependant on the thermal fluctuations of the circuit at $T \neq 0$. As current flows, the nominal charge increases and the distribution drifts towards $Q = e/2$. In absence of tunnelling the charge would increase until capacitor breakdown, and the probability distribution would move with constant velocity in the $+Q$ direction. However, when tunnelling becomes energetically advantageous at $e/2$ the distribution collapses, reforming at $-e/2$ as a tunnelling event shifts the charge distribution by e. The process then continues as the probability distribution again drifts towards $Q = e/2$. Likharev [8] has coined the term 'dripping tap' as an analogy of this process. It allows a clear understanding of the production of SET oscillations in current biased devices. It also shows how Coulomb blockade occurs. An applied voltage of less than $e/2C$ cannot shift the charge distribution far enough to allow tunnelling (i.e no part of the distribution is in the regime $Q > e/2$), unless thermal broadening of the distribution occurs.

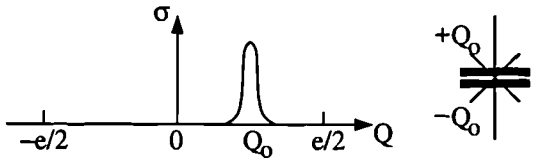


Fig 4.2 Graphical representation of probability density σ in charge space, and its relation to actual charge on the electrodes of a tunnelling junction.

Note the further simplification to equation 4.11 which occurs as $T \rightarrow 0$;

$$\left.\begin{aligned} \Gamma^{\pm}(Q) &= \frac{\Delta E^{\pm}}{e^2 R_t} \qquad \Delta E > 0 \\ \Gamma^{\pm}(Q) &= 0 \qquad\qquad \Delta E \leq 0 \end{aligned}\right\} \tag{4.13}$$

Although of limited use in predicting the action of real physical circuits at finite temperature, the formula does predict the 'best possible operating conditions' of a system. It is the foundation of the *critical charge* concept discussed below in connection with the *linear programming* method. At finite T, equations 4.11 and 4.12 show the effect on electron transport through a junction decreasing exponentially as the temperature falls below a critical value $k_B T_c < e^2/2C$. In practical systems temperatures some thirty times lower than the critical temperature were found to give results obeying equation 4.13 to good approximation (see §6.1.1)

4.1.2 Systems of Tunnelling Junctions

All the above results apply to a single biased junction. Extension to a system of N junctions is accomplished by considering the change in the free energy of a system, rather than that of a single junction. The free energy of a general system of N junctions can be written as $E(n_1,\ldots,n_k,\ldots,n_N)$, where n_k is the net number of electrons which have tunnelled through the kth junction. From the quantum golden rule, the the rate of event $n_k \rightarrow n_k \pm 1$ can be written as,

$$\Gamma_k^{\pm} = \frac{2\pi}{\hbar} \sum_{i,f} |H_{Tk}|^2_{i,f} \; f(E_i)\,[1-f(E_f)] \times \delta\left\{ [E(n_1,\ldots,n_k,\ldots,n_N)+E_i] - [E(n_1,\ldots,n_k \pm 1,\ldots,n_N)+E_f] \right\} \tag{4.14}$$

where $E_{i,f}$ are the energies of the internal degrees of freedom of the initial and final states of the system and $f(E)$ is the Fermi function. A similar form of equation describes the current I in this kth junction biased with voltage V, as given by standard tunnelling theory [96].

$$I(V) = I^{+}(V) - I^{-}(V), \tag{4.15}$$

$$I^{\pm}(V) = e\,\frac{2\pi}{\hbar} \sum_{i,f} |H_{Tk}|^2_{i,f} \; f(E_i)\,[1-f(E_f)]\;\delta\left\{ E_i + [\pm eV - E_f] \right\} \tag{4.16}$$

and combining these gives the required result,

$$\Delta E_k^{\pm} = E(n_1,\ldots,n_k,\ldots,n_N) - E(n_1,\ldots,n_k \pm 1,\ldots,n_N) \tag{4.17}$$

This is an important result for systems of junctions, and agrees with the directly analysed single junction formulae of equation 4.11 under the limits of equation 4.9 [8]. It means that in multi-junction systems obeying equation 4.9 a good approximation to any tunnelling rate can be obtained by calculating the free energy for the system before and after that event occurs. This free energy is easy to calculate as only the junction capacitances need be considered. Equation 4.17 will be used in all the systems modelling discussed below.

4.2 Tunnelling Junctions - Quantum Lengevin Equation [37, 90]

The two first order effects that 'smear' the Coulomb blockade in tunnel junctions are quantum fluctuations due to temperature (thermal fluctuations) and the dissipative effect of an imperfectly biased environment. (In the remainder of this chapter, such dissipative fluctuations will be implied when quantum fluctuations are referred to.) Temperature is taken into account in equation 4.11, but the dissipative environment is specifically ignored through application of the limits of equation 4.9. There has been extensive experimental study of dissipation [48, 59, 92]. Two general approaches to including these effects within tunnelling probability theory will be considered. The first of these is a heuristic approach making use of the quantum Lengevin equation.

4.2.1 Derivation of Governing Equations

Consider the external equivalent circuit of figure 4.3, with inductance L_c, resistance R_c, capacitance C_c and a source of noise V_n to represent the quantum fluctuations. The spectral distribution of this voltage noise is given by the Johnson-Nyquist formula [97, 98].

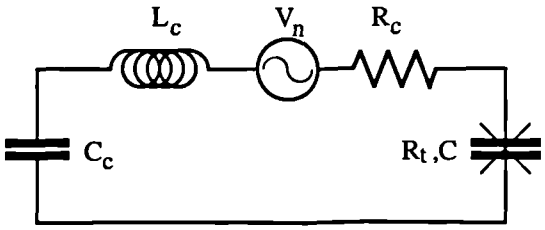


Fig 4.3 Single tunnel junction of capacitance C, and tunnelling resistance R_t with lumped description of electromagnetic environment (L_c,R_c,C_c) and source of quantum fluctuations V_n.

$$S_v(\omega) = \frac{\hbar\omega R_c}{\pi} \coth(\hbar\omega/2k_BT) \tag{4.18}$$

We wish to calculate the spread of the fluctuation $q(t)$ of the junction charge Q caused by V_n so that the equation 4.11 can be modified to take quantum fluctuations into account. For the equivalent circuit of 4.3, the charge fluctuations are linked to the voltage noise fluctuations by the circuit equation,

$$L_c \frac{\partial^2 q}{\partial t^2} + R_c \frac{\partial q}{\partial t} + \frac{1}{C_{total}} q = V_n(t) \tag{4.19}$$

Fourier transforming this equation will give $S_q(\omega)$, the spectral density of the charge fluctuations in terms of $S_v(\omega)$. Then a measure of the spread of q(t), the mean square $\langle q^2(t)\rangle$, is given by

$$\langle q^2(t)\rangle = \int_0^\infty S_q(\omega)\, \partial\omega \tag{4.20}$$

Finally a new effective tunnelling rate $\langle\Gamma^{\pm}(Q)\rangle$ can be approximated by convolving equation 4.11, the tunnelling rate without fluctuations, with the probability P(q) of a given magnitude of fluctuation. P(q) can be simply taken as a Gaussian distribution centred on q with a spread of $\langle q^2\rangle$.

This procedure can be performed analytically to give (at T=0 for simplicity)

$$\langle\Gamma^{\pm}\rangle = -\frac{\Delta E^{\pm}}{2e^2R_t}\,\mathrm{erfc}\left[\frac{\Delta E^{\pm}\,C}{e\sqrt{2\langle q^2\rangle}}\right] + \frac{1}{eR_tC}\sqrt{\langle q^2\rangle/2\pi}\,\exp\left[-\frac{\Delta E^{\pm 2}\,C^2}{2e^2\langle q^2\rangle}\right] \qquad (4.21)$$

with $\Delta E^{\pm} = \frac{e}{C}\left(\frac{e}{2} \pm Q\right)$ for a single junction as before.

4.2.2 Comparison of Thermal and 'Quantum' Fluctuation Effects

Figures 4.4 and 4.5 graph the rate of electron tunnelling through a single junction against the average applied charge (graphs proportional to the IV characteristics of the junctions for voltage bias). They compare smearing produced by thermal fluctuations as calculated from the Averin model, with that of quantum fluctuations as described by the Lengevin equation extension. They indicate that temperatures $T < T_c/10$ and charge fluctuations $\langle q^2\rangle < e^2/100$ are required if such fluctuations are to be considered negligible. As expected, the graphs also show that the effect of quantum fluctuations is to produce an overall result similar to that of temperature fluctuations. This is useful in practice for system analysis, as it implies that both types of fluctuation could be included as a crude 'effective temperature' under the simple Averin model once circuit parameters are known, instead of using the Lengevin equation in its more complex, $T \neq 0$, form.

In order to fully characterise this model the link between $\langle q^2\rangle$ and the circuit parameters L_c, C_c and R_c must be specified. Setting $\alpha = R_c\sqrt{C/L_c}$ and considering the transform of equation 4.19 and the integration of equation 4.20 under the simplifying assumptions that $C_c >> C$ (i.e neglecting stray capacitances) and $\hbar\omega << k_BT$ (i.e the low temperature limit), we obtain for $\alpha < 2$,

$$\langle q^2\rangle = \frac{\hbar\alpha}{\pi R_c}\frac{1}{\sqrt{4-\alpha^2}}\left[\frac{\pi}{2} - \mathrm{Arctan}\left(\frac{\alpha^2-2}{\alpha\sqrt{4-\alpha^2}}\right)\right] \qquad (4.22)$$

and for $\alpha > 2$,

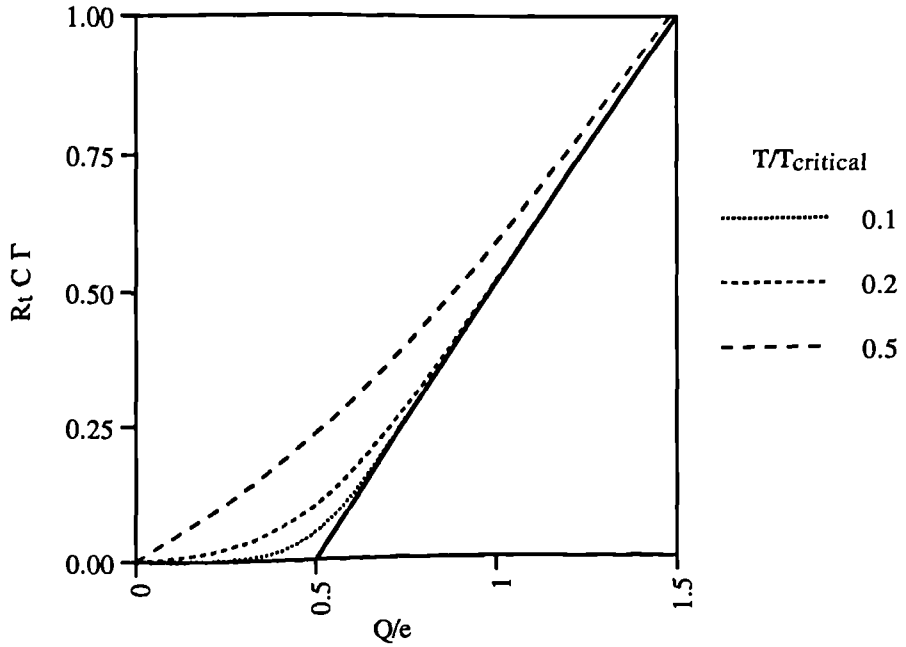


Fig 4.4 Normalised tunnelling rate Γ of electrons through a junction versus charge Q/e, for the 'standard' simple microscopic model. The solid line is the tunnelling rate at zero temperature. The dashed lines are modelled for temperatures $T/T_{critical}$ = 0.1, 0.2, 0.5. $T_{critical} = e^2 / 2k_B C$

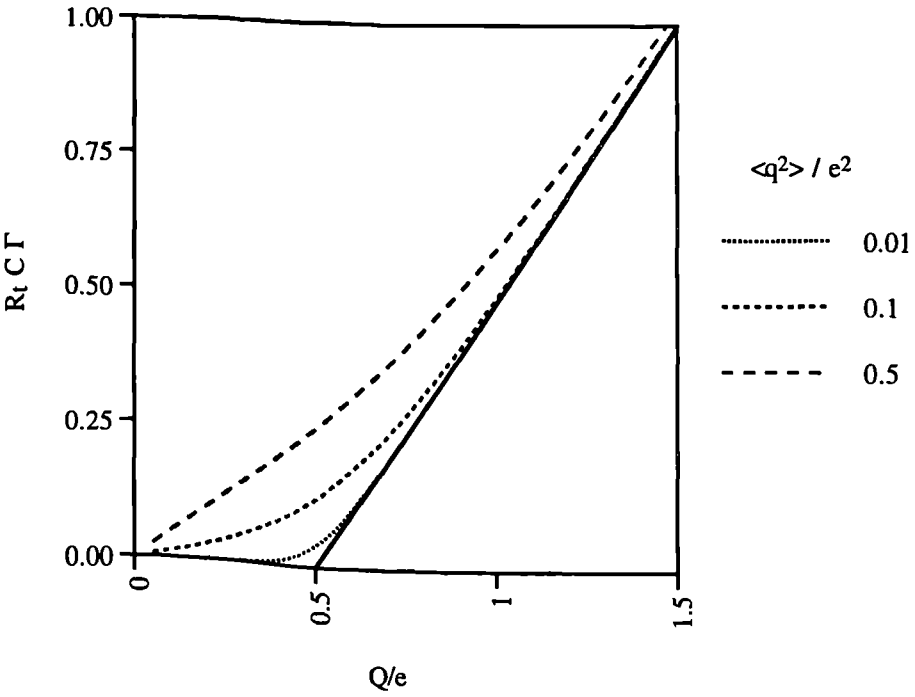


Fig 4.5 Normalised tunnelling rate Γ of electrons through a junction versus charge Q/e, as predicted by the quantum Langevin model for zero temperature. The solid line is the tunnelling rate in absence of fluctuations. The dashed lines are modelled for values of $\langle q^2 \rangle$ = 0.01, 0.1, 0.5. $\langle q^2 \rangle$ is the spread of the distribution describing the probability of a charge fluctuation q on the junction, which in the 'standard' theory is assumed to be a δ function.

$$\langle q^2 \rangle = \frac{\hbar\alpha}{2\pi R_c} \frac{1}{\sqrt{4-\alpha^2}} \ln\left[\frac{\alpha^2 - 2 + \alpha\sqrt{\alpha^2-4}}{\alpha^2 - 2 - \alpha\sqrt{\alpha^2-4}} \right] \tag{4.23}$$

In general $\langle q^2 \rangle$ is kept to a minimum in the limit of large R_c. (Under these conditions $\langle q^2 \rangle$ is logarithmically dependant on L_c which therefore has relatively little effect on the smearing of the Coulomb blockade.) This agrees with the general results of other theoretical calculations [38, 92, 93] and experimental work [48, 59]. Indeed although the difficulty in calculating the circuit parameters L_c, C_c and R_c in nano-electronic experimental circuits makes it difficult to make detailed checks on the accuracy of this heuristic model, it agrees in form to experimental results even in the low temperature limit [90].

4.3 Tunnelling Junctions - Phase-Correlation Theory [91-93, 99]

The second approach to including the effect of fluctuations of the external environment on the action of a tunnelling junction is that of the phase-correlation theory. As opposed to the Lengevin equation approach, which takes the results of the basic microscopic model and adds a source of noise to account for the quantum fluctuations of junction and environment, this method attempts to consider both the junction capacitance and external environment as a quantum system, perturbed by the tunnelling events through the junction.

4.3.1 Derivation of Governing Equations

Initially consider the equivalent circuit of figure 4.6. Instead of the charging terms of the Hamiltonian in equation 4.1 of the simple microscopic model (the $Q^2/2C$ and $\{I_S - I(t)\}\phi$ terms) we now have,

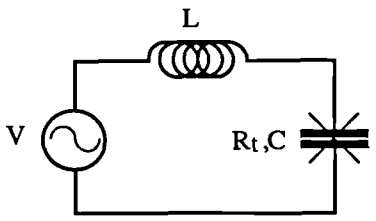


Fig 4.6 Equivalent circuit for a voltage biased tunnel junction in series with an inductor, L.

$$H_c = \frac{Q^2}{2C} + \frac{\hbar^2}{2e^2L}\phi^2 - QV \tag{4.24}$$

taking into account the effect of changes of energy in the whole system. Using the same conditions for R_t as in equation 4.9, Devoret *et al.* [92] obtain a total tunnelling rate for the system by the same approach as above,

$$\Gamma(V) = \frac{1}{e^2 R_t} \int_{-\infty}^{+\infty} dE \int_{-\infty}^{+\infty} dE' \{ f(E)[1-f(E')] P(E+eV-E') - [1-f(E)]f(E') P(E'-E-eV) \} \quad (4.25)$$

where $f(E)$ is the Fermi function as before. The function $P(E)$ is the probability that the tunnelling electron can create an excitation of energy E in the external circuit. This is important as the ability of an electron to induce such an excitation is critical to the formation of the Coulomb blockade effect. For instance, as the impedance of the environment increases, $P(E)$ approaches a $\delta(E)$ function in form, and the probability that the electron can exchange energy with its environment approaches zero. (Or at least only very low frequency modes of the system will be excited and tunnelling will thus be highly inelastic.) The junction becomes isolated from the environment and strong blockade effects occur.

In general,

$$P(E) = \frac{1}{2\pi\hbar} \int_{-\infty}^{+\infty} dt \ \exp[\, J(t) + iEt/\hbar \,] \quad (4.26)$$

with, $$J(t) = < [\phi(t)-\phi(0)] \, \phi(0) > \quad (4.27)$$

where $\phi(t)$ is given by equation 4.2 with definite integral from $[-\infty,t]$. $J(t)$ is the *equilibrium phase correlation function.*
For the circuit of figure 4.4,

$$J(t) = \frac{e^2}{\hbar\omega_L C} \left\{ \coth\left(\frac{\hbar\omega_L}{2k_B T}\right)[\cos(\omega_L t)-1] - i \sin(\omega_L t) \right\} \quad (4.28)$$

where $\omega_L = 1/\sqrt{LC}$ is the frequency of the resonant mode created by the L,C components of the circuit.
This result for $J(t)$ also indicates how the theory for an 'LC' equivalent circuit can be extended to account for any general environment $Z(\omega)$ say. $Z(\omega)$ can be treated as an infinite number of LC oscillators [100], and the Hamiltonian of equation 4.24 replaced by an infinite number of terms each applying to one of these oscillators, to give a general form of $J(t)$,

$$J(t) = \int_0^{+\infty} \frac{d\omega}{\omega} \frac{\Re(Z_{tot}(\omega))}{R_Q} \left\{ \coth\left(\frac{\hbar\omega}{2k_B T}\right)[\cos(\omega t)-1] - i \sin(\omega t) \right\} \quad (4.29)$$

where the total impedance $Z_{tot}(\omega)$ combines the external impedance with the capacitance of the tunnelling junction,

$$Z_{tot}(\omega) = \frac{1}{i\omega C + Z^{-1}(\omega)} \tag{4.30}$$

A final simplification to the problem, now completely characterised via equations 4.25, 4.26, 4.29 and 4.30, can be made by eliminating the Fermi functions and combining the P(E) functions of equation 4.25 to give,

$$\Gamma(V) = \frac{1}{e^2 R_t} \int_{-\infty}^{+\infty} dE\, E \frac{1 - e^{-eV/k_B T}}{1 - e^{-E/k_B T}} P(eV-E) \tag{4.31}$$

Comparison with Experiment and Quantum Lengevin Theory :

This set of equations is found to give good agreement with experimental results [90], particularly at high currents. However as with the Lengevin equation approach it is difficult to physically estimate the experimental impedance accurately enough for detailed comparison. As expected from equations attempting to describe quantum fluctuations due to the electromagnetic environment, a smearing of the blockade is predicted for low external impedances.This is in approximate agreement with the results calculated from the heuristic Lengevin approach shown in figure 4.5.

4.3.2 Systems of Tunnelling Junctions

Modification of the Governing Equations for Multiple Junctions :

Due to the more fundamental nature of this approach, it is possible to confidently extend the theory from single junctions in an electromagnetic environment to systems of junctions and impedances [38, 101]. In such a system the potential map is completely described by the applied voltages and number of excess charges on internal electrodes which will only change (by units of ne, n = integer) through tunnelling. Thus expressions for the tunnelling rates of each of the junctions of the system can be obtained by using the same approach as outlined immediately above. The only change that need be made to equations 4.26, 4.29, 4.30 and 4.31 is that instead of $Z_{tot}(\omega)$ being the summation of the junction capacitance and external impedance $Z(\omega)$, it is now the summation of the junction capacitance and the Thévenin equivalent impedance of the rest of the circuit. I.e the formulae are modified by the capacitance values of the other junctions.

This is similar to the result for systems in the simple microscopic model (equation 4.17) obtained from the quantum Golden Rule. Here the tunnelling rate for any junc-

tion is obtained from a calculation of the free energy of the system before and after tunnelling. The change in free energy is then applied to equation 4.11 to find the tunnelling rate. Such a free energy can be calculated in a capacitive system by calculating a Thévenin equivalent capacitance from the other junctions and capacitances, and indeed this is the method we use in our *general network solver* below.

Limits of the Theory :

Indeed, in the limit where the relaxation time of the electromagnetic environment is much smaller than the time between subsequent tunnelling events, i.e,

$$R_i >> \Re(Z_i(\omega)) \qquad \text{for} \qquad \hbar\omega < eV_i \tag{4.32}$$

there will exist no quantum mechanical correlations between events. The procedure noted immediately above can then be extended to networks with an associated electromagnetic environment. Note that in the above equation, R_i is the tunnelling resistance for junction i, Z_i is the Thévenin impedance of the circuit excluding junction i (treating other tunnelling junctions simply as capacitances), and Vi is the potential difference across junction i before tunnelling. Also note that this treatment still assumes $R_i >> R_Q$ (see equation 4.9).

Practical Application of the Theory :

Although consideration of the phase correlation theory leads to this useful result for systems, the equations that allow calculation of tunnelling rates are impractical for use in Monte Carlo modelling. At least two integrations must needs be performed [38]. For an N junction system, 2N such calculations must be completed to obtain the probabilities required to make a decision on which tunnelling event should be allowed to occur next in the Monte Carlo process. Although the algorithm that is used to calculate the potential map of a system is essentially an N^2 process, the overhead of double integration would be enough to make calculation of tunnelling rates from this potential map the critical time constraint in all but the largest modelled systems.

4.4 Summary of Tunnelling Junction Theories

All the Monte Carlo modelling described in this report is calculated using the simple microscopic model of equation 4.11 of §4.1, i.e,

$$\Gamma^{\pm}(Q) = \frac{\Delta E^{\pm}}{e^2 R_t}\left[1 - \exp(-\frac{\Delta E^{\pm}}{k_B T})\right]^{-1} \tag{4.11}$$

The *linear programming* models are based on the $T \rightarrow 0$ equivalent of this equation, equation 4.13. These governing equations were used on grounds of calculation speed and simplicity, while still accounting for thermal fluctuations at the junction. The model holds true under conditions that assume no quantum fluctuations due to an electromagnetic environment (i.e systems can be assumed to consist only of capacitances and voltage sources), and where the tunnelling resistances are far greater than the quantum resistance (equation 4.9). The theory extends in simple fashion to systems of junctions.

For more accurate and detailed modelling of systems that obey the limits of equation 4.32, the phase correlation theory of §4.3 was developed. Here equation 4.31 is used as the tunnelling rate equation, with values of P(E) obtained by performing the integrations of equations 4.26 and 4.29. Experimentally this theory is found to account well for the effects of a tunnelling junction in an electromagnetic environment. Under the condition that the relaxation time for such an environment (consisting of the Thévenin equivalent circuit of the junction - other junctions being considered only as capacitances) is much smaller than the time between tunnelling events, it allows the simple extension of the theory of one junction to systems of junctions.
Unfortunately, performing the two integrations for each tunnelling probability in a Monte Carlo loop is computationally expensive. This could be eased by pre-calculating tunnelling rates, based on an appropriate spread of impedance and energy, into a look-up table. From this, tunnelling rates could be interpolated during the Monte Carlo loop. Although such a method is feasible, it would require extensive recoding of present computer algorithms based on the elementary microscopic model.

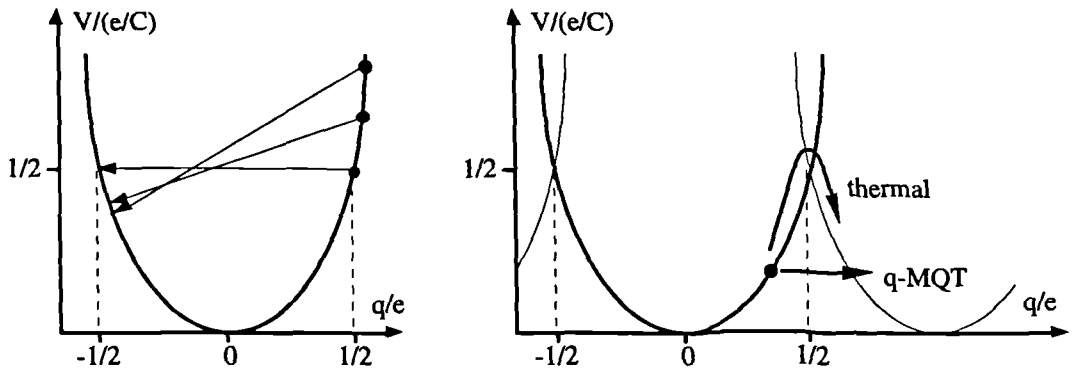
Two approximations to the phase correlation theory are available, involving less computational expense.
The first is to use an approach based on the quantum Lengevin equation theory of §4.2. Here quantum fluctuations are introduced to the system heuristically. Equation 4.21 is used as the tunnelling rate equation, with values for $\langle q^2 \rangle$ obtained from equations 4.22 and 4.23. Under the limits of equation 4.32 this method is extended to systems of junctions in similar fashion to the full phase-correlation theory. The approach agrees well with experiment and could be easily substituted into computer algorithms based on the microscopic model.
Finally, for crude estimation, the quantum fluctuations of the system may be assumed to raise its effective temperature. The simple microscopic model is used, with some phenomenological increase in the thermal effects.

4.5 Higher Order Processes / Macroscopic Quantum Tunnelling [13, 102]

There are a number of processes that may modify the operation of a system of tunnelling junctions from the action governed by the simple theory laid out in §4.1.1. Some may be associated with particular fabrication approaches. These include the trapping/detrapping of charge in semiconductor systems that can upset the electrostatic profile of a device by spuriously gating junction electrodes. Other processes may be general to all fabrication systems, such as the effects of thermal or quantum fluctuations discussed above. *Macroscopic quantum tunnelling* (MQT) is the result of quantum fluctuations in the junction and its environment, and an effect of peculiar relevance to systems of tunnelling junctions.

4.5.1 Macroscopic Quantum Tunnelling in a Single Junction

Figure 4.7 shows schematically the three major forms of tunnelling event which may occur in a single tunnelling junction. Each shows the energy diagram for such a junction, with $E = q^2/2C$. Diagram a) describes the Coulomb blockade. At zero temperature, and without the presence of other quantum fluctuations, tunnelling only becomes energetically advantageous at $E > e^2/2C$. Diagram b) describes tunnelling in the presence of fluctuations. Thermal fluctuations may allow the electron to gain enough energy to overcome the barrier in charge space. However it is also possible for the junction charge variable to 'tunnel' through the barrier, due to quantum fluctuations of the junction. Such tunnelling of the charge variable, simultaneous to the tunnelling of the electron position variable through the junction potential barrier, is referred to as *Charge Macroscopic Quantum Tunnelling* (q-MQT or MQT).



a) tunnelling in absence of fluctuations b) tunnelling processes involving fluctuations

Fig 4.7 Energy diagrams of possible tunnelling processes in a single junction. Potential is graphed against junction charge. (a) shows that without the presence of fluctuations, tunnelling only occurs when $V > e/2C$, each event reducing junction charge by e. (b) shows the two additional tunnelling processes which are the result of fluctuations in the system. The graph is extended to show potential minima for the n-1, n, n+1... events. Energy (thermal) fluctuations can give an electron $V > e/2C$, raising it over the potential barrier in charge space. Quantum fluctuations in the charge variable (q-MQT) can allow an electron to tunnel through both the physical potential barrier *and* the potential barrier in charge space.

The result of such tunnelling events is to allow a small current to flow through a tunnelling junction below the Coulomb blockade, even as $T \rightarrow 0$. Calculation of this current has been made by Babikir [103]. He analyses leakage of the charge variable from the first energy level in the metastable state of fig 4.7b, in the absence of dissipation.

Macroscopic Quantum Tunnelling and Cotunnelling :

Of greater importance for this work are the effects that may arise as MQT processes occur in *systems* of tunnelling junctions.
In one tunnelling junction it is unlikely that most charge fluctuations will lead to an energetically advantageous state, and so its effects are minimal. In a system of junctions, several fluctuation events may occur simultaneously. This can take the system to an otherwise unavailable energetically advantageous state, via a set of intermediate virtual states. The simplest example of this occurs in the double junction. Often the requirement of integer charge on the central electrode of such a system, disbars tunnelling events. Through MQT events, an electron can effectively tunnel through both junctions at once via an intermediate virtual state (the double junction will be discussed in detail in §4.5.1). This leakage can occur even as $T \rightarrow 0$, within the classical Coulomb blockade regime. It is dependant only on the initial and final states of the system, and on the number of possible virtual states available.
Often q-MQT in a single junction, and the effect of multiple tunnelling events described above, are both termed Macroscopic Quantum Tunnelling. We shall follow this convention. However, multiple tunnelling through virtual states is really a separate process based on q-MQT. The term *cotunnelling* has been coined in the literature to differentiate the two.

4.5.2 Macroscopic Quantum Tunnelling in Double Junctions

Figure 4.8 shows schematically the process of macroscopic quantum tunnelling in a two junction device. It can be seen that there are two types of processes that can occur, termed *elastic* and *inelastic* MQT, both of which involve an electron tunnelling through two junctions via an intermediate virtual state in the centre electrode.

Elastic and Inelastic Macroscopic Quantum Tunnelling :

Consider first the inelastic case. Here it is assumed that coherence between the wave functions of the electrons in the two junction barriers can be neglected - i.e electrons are assumed to tunnel independently. The combined result is an electron-hole excitation formed in the electrode (the term inelastic is coined because of this excitation,

and has nothing to do with scattering processes in the barriers). Energy conservation requires that the absolute energies of the initial and final electron states are equal.

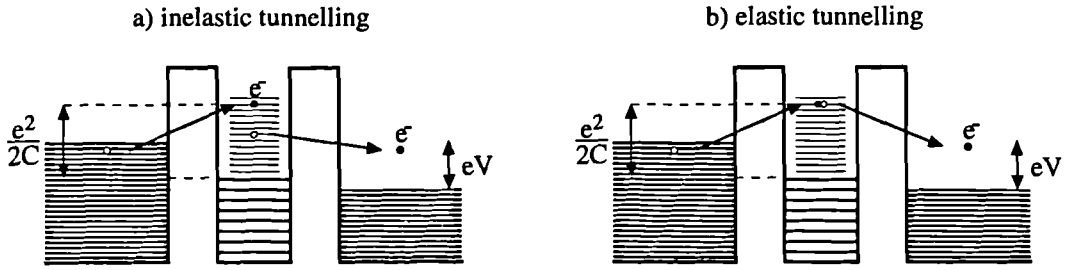


Fig 4.8 Schematic of the potential structure of a double junction array connected by a small electrode, illustrating the simplest cases of both inelastic and elastic macroscopic quantum tunnelling (MQT). In the inelastic case the 'composite electron' is made up of separate tunnelling events leaving an electron-hole excitation at the electrode. In the elastic case the same electron may take part in both events, no excitation being formed. In both cases, the energies of each state, relative to the chemical potential of its electrode, must sum to eV to allow energy conservation. Adapted from [40].

This is equivalent to requiring that the energy levels of initial, final and intermediate states (w.r.t electrode Fermi levels) sum to eV [40]. The magnitude of the tunnelling current due to MQT is obtained by summing over all of the possible conduction paths - i.e the possible initial, final and intermediate energy levels.
In elastic MQT, the assumption is that the electron wavefunctions are coherent. This implies that one electron tunnels through both barriers, passing through a virtual state in the central electrode (represented in figure 4.8b). Transition paths must be chosen by the stricter rule, that the two intermediate states must be at the same energy level.

This argument implies that inelastic processes should dominate over elastic MQT, whose conditions are more strict. Domination will be especially pronounced where there is a high density of states in the central electrode - i.e where the state separation $\Delta << E_C$, with E_C the characteristic charging energy of the system. If however the states in the central electrode are well spaced in energy (for instance in a semiconductor fabrication approach, or with ultra small metallic electrodes) both elastic and inelastic MQT may become comparable, or elastic MQT may dominate.

Calculation of Tunnelling Currents due to Elastic and Inelastic MQT :

Specific analysis of tunnelling currents due to both types of MQT has been performed by Averin *et al.* [13, 102] on the double junction. This extends the simple microscopic formalism of §4.1.1, considering terms until fourth order in the tunnelling Hamiltonian (each MQT event in such a system consists of two correlated tunnelling events, and fourth order in H_T is the second non-vanishing order). For low voltage and temperature - the only conditions under which MQT is liable to be an important contribution to the tunnelling current - they obtain,

$$I_{inelastic} = \frac{\hbar}{12\pi e^2 R_1 R_2}\left(\frac{1}{E_1}+\frac{1}{E_2}\right)^2 [(eV)^2 + (2\pi k_B T)^2]\, V \qquad (4.33)$$

The specific voltage and temperature conditions are; $eV << E_i$, $k_BT << E_i$, with E_i the lowest of the charging energies of the two junctions,

$$E_1 = \frac{e}{C_1+C_2}\left(\frac{e}{2} + Q_o - VC_2\right) \qquad E_2 = \frac{e}{C_1+C_2}\left(\frac{e}{2} - Q_o - VC_1\right) \qquad (4.34)$$

Q_o again representing the fractional gating charge on the central electrode.

In general, elastic MQT is dependant on the precise geometry of the electrode in which tunnelling takes place. However, there are two limits in which geometry can be ignored. Firstly, when the dimensions of the electrode are greater than the bulk mean free path of an electron in the electrode material, and the characteristic tunnelling time $\hbar/E_C$ is greater than the classical diffusion time through the electrode L^2/D, (L is the length scale of the electrode and D the electron diffusion coefficient). Under these conditions,

$$I_{elastic} = \frac{\hbar\Delta}{4\pi e^2 R_1 R_2}\left(\frac{1}{E_1}+\frac{1}{E_2}\right)V \qquad (4.35)$$

(R_i the tunnelling resistance of junction i, and Δ the state separation in the central electrode.)

The second limit is where the dimension of the electrode is less than the bulk mean free path of an electron in the electrode material, but where the surface scattering is considered diffusive and $E_C << \hbar v_F/L$. This condition on the Fermi velocity v_F again asks that the allowed tunnelling time $\hbar/E_C$ is greater than the expected time for the electron to cross the electrode, L/v_F). Under these conditions $I_{elastic}$ is again given by equation 4.35.

Note that equations 4.33 and 4.35 show a linear dependence of $I_{elastic}$ on V, while $I_{inelastic} \propto V^3$. Under most circumstances where MQT is not swamped by thermal fluctuations in the classical blockade region, $I_{inelastic}$ will dominate. However when,

$$\frac{1}{3}\left(\frac{1}{E_1}+\frac{1}{E_2}\right)((eV)^2 + (2\pi k_B T)^2) < \Delta \qquad (4.36)$$

$I_{elastic}$ may be larger. This occurs for small electrodes (giving larger Δ) at very low voltages. Both inelastic and elastic MQT have been observed [39, 40], with good agreement between experimental measurement and theory.

Application to Devices Fabricated at Glasgow :

The conditions implying equation 4.35 are the ones most likely to apply to structures fabricated at Glasgow. As an indication of the orders of magnitude involved, consider 20nm Aluminium spheres spaced 12nm apart on a Silicon substrate. A capacitance of 12.3 aF is obtained, giving $E_C = 13$ meV. A Fermi velocity of the order of 10^{16} ms^{-1} [40] gives $\hbar v_F/L = 0.3$ GeV at 4.2K, a temperature at which the mean free electron path in bulk Aluminium is 17.5 μm [104]. This mean free path is much larger than the device size. Therefore equation 4.35 is appropriate, if diffusive surface scattering in the electrode can be assumed.

4.5.3 Macroscopic Quantum Tunnelling in Extended Systems

MQT in Tunnelling Junction Arrays :

The most important extended system in single electronic logic is the tunnelling junction array. Ungated, such arrays act as single electron transmission lines. Gated electrodes in arrays allow control of the movement of electrons. Tunnelling junction arrays will be considered in detail in §5.1.
Specific analyses of MQT in such systems have been made [13]. However, equations 4.33 and 4.35 make clear the most important point - that the rate of tunnelling for both elastic and inelastic MQT is inversely proportional to the product of the junction impedances. For nominal junction impedance R_t, the MQT rate in an array with i junctions decreases as $(R_t)^i$.

This result clearly has very important consequences for the design of tunnelling junction arrays, and has been verified by experiment [39, 50]. To fulfil the conditions of $R_t >> R_Q$ tunnelling resistances greater than $R_t \approx 1$ MΩ are common in practice. For such resistances in tunnelling junctions of $C \approx 100$ aF the double junction effectively presents a resistance to the circuit of $< 10^{13}$ Ω. A quadruple junction array gives an effective resistance of $> 10^{17}$ Ω. Obviously increasing the number of junctions in an array has a marked effect on the magnitude of the MQT current in any system.

Implications for General Systems :

Macroscopic quantum tunnelling, therefore, although acting as a serious perturbation to the operation of tunnelling junction systems, can be counteracted by the use of multiple junction arrays as buffers to block its effects. This means that in practical systems a trade off between operational speed and system accuracy must be made. The necessity of such buffer arrays again implies systems that will be extended and

complex in nature, relying for operation on cooperative effects between sets of junctions. This adds weight to the need for tools to investigate such extended systems.

As an aside, we note that detailed analysis of macroscopic quantum tunnelling in a dissipative environment shows a strong suppression of MQT due to electromagnetic fluctuations in the external system.
Specifically, Odintsov *et al.* [105] predict inelastic MQT in a double junction system at zero temperature, that obeys,

$$I \propto V^{3+2z}, \qquad z = \frac{Re^2}{h} \tag{4.37}$$

where R is the total resistance of the high impedance leads feeding the double junction. Equation 4.37 holds for voltages inside the Coulomb blockade region, and where $V << \hbar\Omega_z/e$ (Ω_z is the characteristic frequency of the environment). The constant of proportionality is $3/(8\Gamma(2z+4))$ times that of equation 4.33.
It is suggested that driving a single-electron turnstile through high impedance leads will provide greater device reliability at the cost of a larger RC time constant. This would allow the formation of more accurate single-electron electrometers. However, as already noted in §1.3.1, the physical size of such high impedance leads makes this method of reducing MQT unattractive for more highly integrated systems.

CHAPTER 5 DEVELOPMENT OF SIMULATION TOOLS FOR SINGLE ELECTRONIC SYSTEMS

There have been two important initial developments in the technology of single electronic *systems*. First is the demonstration and analysis of tunnelling junction arrays as single electron transmission lines [11, 12, 49, 106-108]. Second is the fabrication of gated turnstiling devices through which electrons may be pumped in a synchronous and controlled fashion [9, 10, 57, 63, 109]. Such small scale systems are of intrinsic interest, but in §2.3.2 it is noted that they may also act as sub-units of complex single electronic systems with attractive operating characteristics [81]. However under all present fabrication approaches, the required ultra-small tunnelling junctions are obtained at the cost of strong capacitive coupling between circuit components. Even excluding other possible killer effects (such as thermal and quantum fluctuations, macroscopic quantum tunnelling and charge trapping/de-trapping), the effects of capacitive coupling on extended systems will require the development of new tools for design and analysis [61].

In this chapter we consider the simplest small systems (the tunnelling junction array and gated turnstiling device mentioned above), and using the experience gained in their analysis, develop and generalise important modelling tools.

We describe a model of a tunnelling junction array system developed by Bakhavlov [12, 106] and based on the microscopic model laid out in §4.1.1. Both an analytic approach and Monte Carlo modelling routine are used to characterise the operation of the array. Concepts of use in characterising general tunnelling junction systems are emphasised. The models are extended to consider arrays whose component values vary along their length.
Gated turnstile devices are modelled with a Monte Carlo routine using a bespoke analysis of the turnstile equivalent circuit. In considering analytical methods of describing turnstile operation, a *linear programming* model is introduced, which is used to calculate device stability in control parameter space.
Finally, these basic tools are further extended to deal with general capacitive networks. The relative advantages & disadvantages of each tool are discussed.

5.1 Development through Analysis of Tunnelling Junction Arrays

The use of tunnelling junction arrays as a first step in building models and tools for complex single electronic systems is discussed. Equivalent circuit equations which govern such arrays are developed, and an analytic approach to their operation described. This approach is due to Bakhvalov *et al.* [12]. It is based on conditions allowing the formation in the arrays of charge *solitons*. Bakhvalov's simple Monte Carlo modelling approach is extended to systems in which component values (junction and grounding capacitances) vary throughout the array. From this analysis, we consider principles which will be of use in developing a *general solver* of single electronic systems.
Specific modelling results from the tools developed here are considered in Chapter 6.

5.1.1 Reasons For Studying Tunnelling Junction Arrays

The motivation for initially studying tunnelling junction arrays is broadly threefold. First, such arrays are the simplest structures to construct for a wide range of fabrication techniques. They are particularly simple for those lithographic techniques that seem to hold the most promise for the controlled fabrication of large systems of such junctions. Arrays have been specifically constructed using for instance the hanging resist vertical MIM method [11, 48, 49] and with ultra-small Schottky dots on semiconductor substrates [60]. Results of theoretical array analysis can therefore be easily compared with experimental data. Such arrays may also act as first order approximations of granular systems [20-22] and the 'squeezed wire' systems of laterally patterned 2-dimensional electron gases in semiconductor heterostructures [55, 68, 110, 111]. Simple methods of array characterisation would then aid in the modelling of such systems.
Secondly, multiple junction arrays are the first step up in complexity from single junctions. They should therefore be the simplest systems to analyse, both in themselves and as a route to gaining the experience and techniques necessary to successfully analyse more complex systems. Simple models would also be invaluable in testing general tools for more complex systems.
Finally, cooperative effects in multiple junction arrays suggest [106] that they act analogously to controlled transmission lines (or shift registers) for single electrons. As such they would be important components in any extended single electronic system.

5.1.2 Equivalent Circuit Model

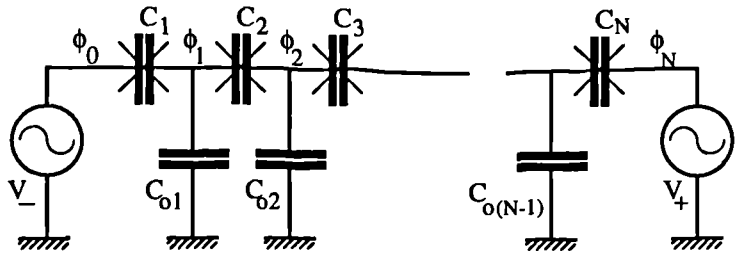


Fig 5.1 Equivalent circuit diagram of an array of tunnelling junctions, including strays to ground and biasing voltage sources.

Consider the equivalent circuit of a tunnelling junction array, figure 5.1. It consists of a series of tunnelling junctions 1,...i,...N each of capacitance C_i. These are connected by electrodes 1,...i,...N-1 at potential ϕ_i, and coupled to the ground plane via capacitances C_{oi}. The array is voltage biased by an offset from ground U, and a differential voltage across the array V, so that $V_- = U - V/2$ and $V_+ = U + V/2$. This means $\phi_0 = V_-$ and $\phi_N = V_+$.

By the theory summarised in equation 4.17, the electron tunnelling rate through any junction of the array is a function (equation 4.11) of the change in the free energy of the system caused by such tunnelling events. The full expression for the free energy of the circuit of figure 5.1 is;

$$E = \sum_{i=1}^{N-1} \frac{C_{oi}}{2} \phi_i^2 + \sum_{i=1}^{N} \frac{C_i}{2} (\phi_i - \phi_{i-1})^2 - V_+Q_+ - V_-Q_- \qquad (5.1)$$

where,

$$Q_+ = C_N(\phi_N - \phi_{N-1}) + em_+, \qquad Q_- = C(\phi_0 - \phi_1) - em_- \qquad (5.2)$$

m_+ and m_- being the number of electrons passing through the left and right hand junctions of the array respectively. This formula is needed in its entirety to model arrays whose capacitance parameters vary. However if all the junction and grounding capacitances are taken as equal, i.e $C_{oi} = C_o$ & $C_i = C$ then equation 5.1 simplifies to;

$$\Delta E_i^+ = \frac{e}{2} (\phi_i + \phi'_i - \phi_{i+1} - \phi'_{i+1}) \qquad (5.3)$$

(and similarly for ΔE_i^-) where ΔE_i^+ is the change in free energy of the system due to a tunnelling event across the ith junction and ϕ_i and ϕ'_i are the potentials of the ith electrode before and after the tunnelling event occurs.

In order to characterise the system so that equations 5.1 and 5.3 can be used, it is necessary to obtain the values for all ϕ_i. For an array of junctions with identical capacitances, as noted above, the formula;

$$-C_i\phi_{i-1} + (C_i+C_{i+1}+C_{oi})\phi_i - C_{i+1}\phi_{i+1} = en_i \qquad (5.4)$$

(n_i being the number of excess electrons at electrode i, giving en_i as the excess charge on this electrode) can be used to form a system of N-1 linear equations in N+1 unknown potentials. To this system of equations is added $\phi_0 = V_-$ and $\phi_N = V_+$, allowing exact solution of the problem for all ϕ_i. (It should be noted that a more accurate form of equation 5.4 would replace en_i with en_i+Q_i, where Q_i is a fractional charge caused by the presence of trapped charge in the dielectric medium of the junction or differences in the electrode materials [25].) In many practical systems it may be assumed that Q_i is negligible [112] and we shall follow this assumption. However this will not always the case; consider for instance the fluctuations due to the random positioning of dopants in 2-dimensional electron gas structures in semiconductor heterostructure systems [72], systems which are currently under active study [64-67, 78, 113, 114]).

Tunnelling Junction Arrays with Non-Uniform Component Parameters :

Experimentally, the most likely reason for considering TJAs where junction capacitance and grounding capacitance are not all identical is to model the effect of imperfections in the fabrication process. The stability of such systems with respect to junction parameter variation can then be studied. Therefore the substitutions $\zeta_i = C_i/C$, $\eta_i = C_{oi}/C$ and $\beta = e/C$ are made, where C is the nominal average value of junction capacitance, to obtain,

$$-\zeta_i\,\phi_{i-1} + (\zeta_i+\zeta_{i+1}+\eta_i)\,\phi_i - \zeta_{i+1}\,\phi_{i+1} = \beta n_i \qquad (5.5)$$

Knowing the values n_i, V_-, V_+ and how the parameters of this array differ from their nominal values through ζ_i and η_i; the potentials of each electrode can again be calculated as before.

Limitations of Equivalent Circuit Model :

As an aside, it should be noted that this model only includes within its scope the intercapacitance of 'nearest neighbour' electrode; stray capacitance from electrode i to i±2 is for example ignored. This approximation may be assumed to hold in fabrication systems where the distance between junctions is, or can easily be made, large. However in the case of Schottky dots on semiconductor substrates, the assumption

will most probably be invalid. Here fringing fields must be accounted for in intercapacitance calculations. As an example, we note that for 20 nm radius metallic spheres 12 nm apart the intercapacitance is approximately 1.90 aF. For equivalent spheres 64 nm apart (the 'next nearest neighbour' distance) intercapacitance is calculated at 1.38 aF. Clearly the effect of fringing fields makes the problem more complex than the simple equivalent circuit of figure 5.1 implies, and adds weight to the desire expressed in §3.1.1 that we obtain the full capacitance matrix for such a physical system. However, within these limitations, the model is still found to be the source of useful results.

5.1.3 Device Operation, Theoretical Analysis [12, 106]

The form of equations governing a tunnelling junction array immediately leads to a simple analytical approach describing its operation. Note that with no excess electrons, $n_i e = 0$, equations 5.4, (those governing an array of similar junctions) are a discretised form of,

$$C\varepsilon^2 \frac{d^2\phi}{dx^2} = C_o \phi(x) \qquad (5.6)$$

where ε is an arbitrarily small distance. This equation has solutions of exponential form, implying a potential, on application of a single excess charge into a previously neutral junction array, of the form shown in figure 5.2 - assuming a long array and considering a junction far from its ends.

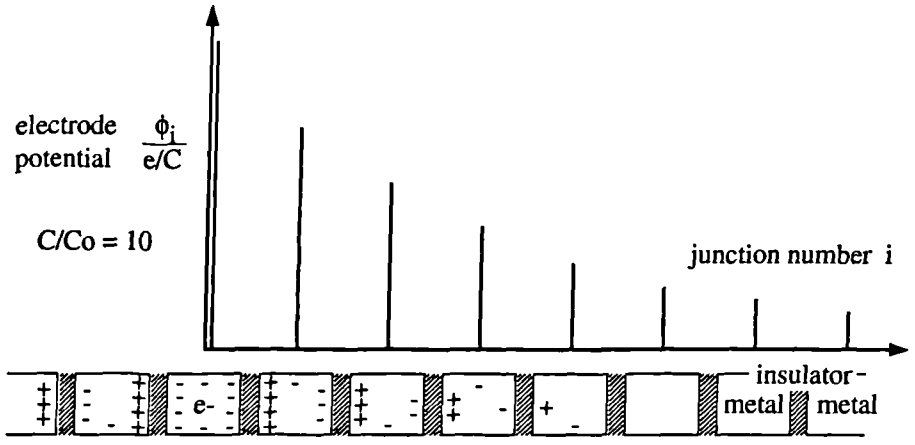


Fig 5.2 Schematic of the polarisation effect caused by placing an excess electrode on an initially neutral array of metal-insulator-metal tunnelling junctions. Shown above the array is the resultant potential of each electrode - based on a junction to ground capacitance ratio of C/Co = 10.

The exponential potential 'decay' occurs symmetrically to both right and left of the electrode that contains the excess electron, forming a charge *soliton* [115] in the array

produced by the polarization field around the junction. Explicit analysis of the constants in the exponential solution to equation 5.6, based on equation 5.4 give,

$$\phi_i = \frac{e}{\sqrt{C_o^2 + 4CC_o}} \exp(-\lambda |i|) , \qquad \lambda = \cosh^{-1}\left(1 + \frac{C_o}{2C}\right) \tag{5.7}$$

where the coefficient λ (actually its inverse) gives an indication of the extent of the polarization, with $C/\sqrt{C_o^2 + 4CC_o}$ its magnitude in units of e/C.
For $C >> C_o$ such polarisation fields can indeed be considered as solitons, for their dimension covers a number of junctions, and their energy,

$$E_{soliton} = \frac{e^2}{2\sqrt{C_o^2 + 4CC_o}} \tag{5.8}$$

is much greater than the characteristic tunnelling energy of a single junction, $e^2/2C$. Calculating the energy of two such solitons (found from equation 5.1 by applying equation 5.7) in the same array shows that those with similar charge sign will repel, while those with dissimilar charge sign will attract and possibly annihilate each other.

Array IV Characteristics - Interaction of Solitons with Array Ends :

Of most interest, however, is the way in which these solitons interact with the ends of a tunnelling junction array, for this gives important information on the IV characteristic of the array itself. It can be found (again by applying equation 5.7 to the energy equation 5.1) that,

$$E_{passive\ end} = -E_{soliton} \exp(-2\lambda j) \tag{5.9}$$

$$E_{active\ end} = \pm eV \exp(-\lambda j) \tag{5.10}$$

Here, $E_{passive\ end}$ is the energy of interaction of the soliton with the end of an array to which no external voltage is applied (it mimics the energy of the soliton and a virtual antisoliton mirrored in the passive end of the array forming an 'image charge'). j is the distance in junctions from the end of the array. It can be seen that attraction takes place, ensuring that an array with no applied voltages will have solitons 'fall out of the ends' thus bringing the system to charge neutrality.

$E_{active\ end}$ is the energy of interaction of the soliton with the end of an array when a potential of magnitude V is applied. The energy will ensure repulsion of the soliton into the array when the voltage sign is the same as that of the charge creating the soliton. We note that for such an array, this effect produced by the action of the external voltage upon a group of junctions of extent λ^{-1} into the array, rather than on a

single end tunnelling junction, means that injection of electrons into the array does not occur until a threshold voltage greater than e/2C is achieved,

$$V_{threshold} = \frac{e}{2C} \left(\exp(\lambda) - 1 \right)^{-1} \qquad (5.11)$$

Thus, in a tunnelling junction array with $C >> C_o$, the region of coulomb blockade is widened from that of a single junction. This is still appreciably less than the ne/2C coulomb gap predicted from a simple assumption of n similar tunnelling junctions with no grounding strays. It should be noted that equation 5.11 does not return this ne/2C value in the limit as $C_o \rightarrow 0$. This is because it only considers the injection of electrons into a long array (length $>> \lambda^{-1}$), and does not take into account the effect of the opposite end.

At the threshold voltage, the effective resistance of the array is also lowered in comparison with the high voltage limit, again because the injection voltage is somewhat higher than e/2C. This gives an IV curve which 'jumps' quickly from the coulomb gap before settling to the ratio governed by the array conductance. Such a jump is characteristic of an array structure. The form of this jump can be clearly seen in the results shown in figure 6.2.

Zero Differential Bias Characteristic of Array - Soliton Density :

The threshold voltage also has importance when considering the process by which solitons enter finite arrays. If, for instance both ends of such an array are brought to a potential V, then the array will fill with an integer number of such solitons until a stable state is obtained where the soliton's mutual repulsion counteracts the effect of the external potential attempting further injections into the array. Again no soliton will be injected until $V > V_{threshold}$, after which a complex 'devil's staircase' pattern is produced, further solitons being allowed into the system at threshold voltages dependant on the precise values of C and C_o. Analysis of particular values of these voltages is summarised in [12], however for our purposes a result of particular importance is that an integer change in soliton density (i.e a change from an average of soliton per site to two solitons per site in an array) is marked by a change in applied bias voltage of,

$$\Delta V = \frac{2E_{soliton}}{e} \coth(\lambda/2) \qquad (5.12)$$

Application to Physical Systems of Interest :

Unfortunately, the initial capacitance calculations of Chapter 3 give C_0/C ratios from 1 to 10. The theory discussed above is applicable to extended solitons, which are formed when $C_0/C<<1$. Observation of effects based on solitons within the array may not be possible with the particular Schottky dot devices under construction at Glasgow. However the results are of use in other systems, and are of particular aid in verifying the results of a computer program specifically designed to model the operation of tunnelling junction arrays by use of an iterative Monte Carlo modelling technique.

5.1.4 Device Operation, Monte Carlo Modelling

Reasons for Concentrating on Monte Carlo Techniques :

In addition to the soliton based approach described above, further analysis of tunnelling junction array operation was attempted. One major area of interest is the stability of such devices with respect to perturbation of their component parameters. In practice such perturbations might be caused by imperfections in physical device fabrication processes. Analytical attempts to deal with this problem are described in Appendix A - Elementary Stability Analysis of Tunnelling Junction Arrays. However, the discrete nature of charge introduced into a junction array elicits governing equations which are non-autonomous - and whose solution is highly non-trivial. Such difficulties are characteristic of many problems associated with systems of tunnelling junctions.

An appropriate non-analytic approach to studying problems such as that of tunnelling array stability is to use Monte Carlo modelling. A large number of single electrons are tracked through the junction system. Following each electron gives insight into the processes taking place within the system. Its macroscopic properties can be calculated by measuring the flow of large ensembles of single electrons.

Monte Carlo Modelling Method - Calculation of Tunnelling Rates :

The approach used in the Monte Carlo modelling of tunnelling junction systems is straightforward. Essentially answers are required to the two questions;

a) when does the next tunnelling event occur ? i.e the probability $P(t)$ of a tunnelling event at time t.
b) which tunnelling event will occur next ?

Each of these questions can be answered once the tunnelling probability $\Gamma_i^{\pm}$ for each possible event is known. (The $\pm$ distinguishes forwards and backwards tunnelling events at junction i.) In the simple microscopic model $\Gamma_i^{\pm}$ is calculated from the change in free energy of the system $\Delta E^{\pm}$ due to tunnelling, via equation 4.11. There are, in turn, two routes to obtaining $\Delta E^{\pm}$. The first is to calculate the potential profile of the system from a matrix equation such as 5.13.

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & \cdots \\ -\zeta_1 & (\zeta_1+\zeta_2+\eta_1) & -\zeta_2 & 0 & 0 & \cdots \\ \vdots & \vdots & \vdots & \vdots & \vdots & \end{bmatrix} \begin{bmatrix} \phi_0 \\ \phi_1 \\ \vdots \end{bmatrix} = \beta \begin{bmatrix} V_+/\beta \\ n_1 \\ \vdots \end{bmatrix} \qquad (5.13)$$

(which describes the tunnelling junction array with governing equation 5.5). Solutions for ϕ are obtained for both initial, and all possible final, states of the system. For each event, the free energy difference $\Delta E^{\pm}$ is calculated using equations 5.1 and 5.2. Then equation 4.11 is used to obtain the appropriate tunnelling probabilities. This algorithm will calculate the potential profile as a $\frac{1}{2}N^2$ process for a system of N junctions. (I.e computation time is proportional to the square of the number of junctions.) The calculation of all tunnelling probabilities based on this potential profile is a $2N^2$ process.

The second method of obtaining $\Gamma_i^{\pm}$ values is detailed below in §5.2.4. In brief, a charge profile of the system is calculated by way of a matrix equation such as 5.18. Then the critical charge equation 5.25 is used to obtain $\Delta E^{\pm}$ values and equation 4.11 again used to find the appropriate tunnelling probabilities. This method is analytically identical to the potential profile route. Computationally, however, it is preferable. The calculation of all tunnelling probabilities based on the system charge profile is only a 2N process.

Obviously some considerable computational effort is required to process large arrays. For the chosen junction/grounding capacitance ratio $C/C_0 = 10$ at which our test results were obtained, a value of $\lambda^{-1} \approx 3$ means that arrays of 20 or so junctions can be considered 'long' for analytic predictions. As will be noted below, a typical Monte Carlo experiment tracking 2×10^5 electrons through a 20 junction array required of the order of 10 cpu seconds of processing time on an IBM 3090 mainframe computer.

Monte Carlo Modelling Method - Tunnelling Events :

Having obtained the system tunnelling rates, weightings can be calculated for the choice of next event and time to next event. For an event that occurs Γ_{tot} times per second, the probability of such an event occurring at time t after the system has been placed in an initial state is,

$$P(t) = 1 - \exp(-\Gamma_{tot}\, t) \tag{5.14}$$

By the principle of indifference [116] in this case we find that,

$$\Gamma_{tot} = \sum_{i=1}^{N} (\Gamma_i^+ + \Gamma_i^-) \tag{5.15}$$

Γ_{tot} is calculated from the sum of tunnelling rates of all possible events that lead from a given state. From a random Monte Carlo variable, equations 5.14 and 5.15 are used to determine the time t till the next event.

To discover which of the tunnelling events occurs, a similar random variable is used. The probability of an event occurring is directly proportional to its tunnelling rate. Event $i^{\pm}$ is therefore chosen by the random variable, weighted by the $\Gamma_i^{\pm}$ values.

Summary :

A Monte Carlo solver has been developed to model the operation of arrays of tunnelling junctions. It will give results which can be compared with the purely analytical work of § 5.2.3. In constructing such an aid we first require an appropriate equivalent circuit model for the junction arrays. Having this, an iterative method is used to model the circuit;

1) Characterise the system by either its potential or charge profile.
2) Calculate the tunnelling rate for each possible system state change.
3) Choose which event will occur, and the time at which it will occur, based on weightings given by these tunnelling rates.
4) Recharacterise the system, based on the new distribution of excess charge and bias conditions.

This iterative loop is the basis of all the Monte Carlo modelling we use to investigate tunnelling systems. Although extended to deal with more complex systems of junctions, its basic principles will remain unchanged.
The Monte Carlo solver will prove to be a useful and versatile tool in the analysis of single electronic systems. Its only major disadvantage is the need for sizable processing power to perform the simulations in a reasonable time.

5.2 Development through Analysis of Turnstiling Devices

The motivation for studying gated junction array systems is discussed. Some of the applications of devices where the flow of electrons may be controlled are considered. Experimental work in the fabrication and measurement of such systems is noted. The equivalent circuit equations of a simple gated junction array system - the four junction gated turnstile device - are developed and solutions found for both electrode potentials and junction charges. The detailed operation of such a device is explained. Techniques are developed to extend the modelling tools of §5.1. The concept of *critical charge* is introduced as a method of speeding calculation in Monte Carlo modelling. A new *linear programming* technique is described. This technique allows calculation of the stability of a gated turnstile in control parameter space.

5.2.1 Reasons For Studying Turnstiling Devices

The next stage in system complexity, above that of the tunnelling junction array, is the gated turnstiling device or electron pump [10, 63, 109] first suggested by Esteve [9]. At their simplest, such devices consist of a junction array with one or more electrodes linked by small gating capacitances to a set of control voltages. Variation of the control voltages effects the fractional charge on the gated electrodes, which in turn controls tunnelling of electrons through the array. Given appropriate biasing conditions it is possible to drastically alter array impedance by small variations of the control voltages. This gives the system transistor like switching properties.
(In some sections of the literature [63, 109] a distinction is made between gated arrays, depending on the number of control voltages used. In this work the term 'gated turnstile' will be used to describe devices with *one* gated control voltage. More complex systems will be specified as '2-phase', '3-phase',... devices.)

The ability to control electron flow has obvious applications. Suggestions include;

- Highly sensitive electrometers [11], where the charge to be measured is capacitively coupled to a controlling electrode of a gated junction array,
- Quantum metrology [8], where a turnstile is used as the basis for a dc current standard,
- digital systems [81], where excess electrons are used as information bit carriers and gated turnstiles act as the basis of switching circuits such as those noted in §2.3.2.

There has also been recent interest in the fabrication of gated turnstile devices using a variety of approaches. Metal-insulator-metal systems have been fabricated using the hanging resist technique of [14] and junctions of area as small as $(30nm)^2$ have been

produced. Both gated turnstiles [10] and 2-phase devices [63] have been constructed and measured using this technique. Turnstiling systems have also been constructed around a quantum dot (lateral dots with capacitance in the order of 240 aF defined by metal gates producing a two-dimensional electron gas in a GaAs/AlGaAs hetero-structure [57]). In Glasgow, work is in progress for the construction of turnstiles using a metal-semiconductor-metal approach at ultra-fine (< 5nm radii) resolution [60].

The experimental progress on gated junction arrays, and their obvious importance in single electronic systems, are the prime reasons for developing tools for the analysis of turnstile operation.

5.2.2 Equivalent Circuit Model

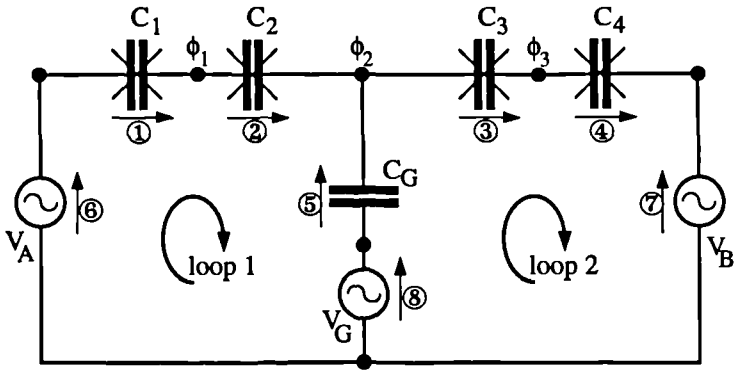


Fig 5.3 Equivalent circuit diagram of a gated turnstiling device, whose purpose is to clock electrons from the electrode at potential V_A to that at V_B as a result of an oscillating voltage applied to V_G. As well as the biasing potentials, junction and gating capacitances being show, characterising information required for the general network solver of §5.3 is noted - the components and circuit loops are numbered, and nominal current flows noted.

Consider the circuit diagram of a simple gated turnstiling device shown in figure 5.3. It consists of four tunnelling junctions $C_1,...C_4$ and a non-tunnelling gate capacitance C_G, with bias produced by voltage sources V_A, V_B, and V_G. Excess electrons may be found on the three electrodes of the device, at potential ϕ_1, ϕ_2 and ϕ_3, respectively. The charge carried by excess electrons at these three points is Q_1, Q_2 and Q_3.

In operation, V_G cycles between two voltage levels. At one level the bias of the system allows electrons to tunnel from V_A onto the central electrode, but no further. Tunnelling from the central electrode, through electrode 3 to V_B, is disallowed under this bias. At the other level of V_G, electrons can tunnel out from the device, but no further electrons can enter. Thus charge is clocked through the system by an oscillating gate voltage. We wish to analyse the area in bias-parameter space under which this turnstiling action occurs.

Circuit Analysis :

The circuit of figure 5.3 can be characterised by the following equations;

$$\begin{aligned} (V_A - \phi_1)\, C_1 &= -q_1 & (\phi_1 - \phi_2)\, C_2 &= -q_2 \\ (\phi_3 - V_B)\, C_4 &= -q_4 & (\phi_2 - \phi_3)\, C_3 &= -q_3 \\ & & (\phi_2 - V_G)\, C_G &= q_G \end{aligned} \tag{5.16}$$

$$\begin{aligned} Q_1 &= q_1 - q_2 & Q_3 &= q_3 - q_4 \\ & & Q_2 &= q_2 - q_3 + q_G \end{aligned} \tag{5.17}$$

where the equations 5.16 are from the definition of capacitance and the equations 5.17 from charge conservation. With eight equations and eight unknowns the system is exactly soluble.

These equations can be manipulated into matrix form, solving for the charge across each capacitance in terms of the known constants; Q's, V's and C's. This elimination of the ϕ_i anticipates the *critical charge* approach described below.

$$\begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 1 \\ 0 & 0 & 1 & -1 & 0 \\ \frac{1}{C_1} & \frac{1}{C_2} & 0 & 0 & -\frac{1}{C_G} \\ 0 & 0 & \frac{1}{C_3} & \frac{1}{C_4} & \frac{1}{C_G} \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \\ q_3 \\ q_4 \\ q_G \end{bmatrix} = \begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ V_G - V_A \\ V_B - V_G \end{bmatrix} \tag{5.18}$$

(Here, the first three rows of the matrix again come from charge conservation and the last two from the application of Kirchoff's Laws.)

Expansion of 5.18 gives;

$$q_G = \frac{C_3(V_B - V_G) - Q_3 + \frac{C_3+C_4}{C_4}\left[Q_2 + Q_3 - \frac{C_2}{C_1+C_2}(C_1(V_G - V_A) - Q_1)\right]}{\left(1 + \frac{C_1 C_2}{C_G(C_1+C_2)}\right)\frac{C_4+C_3}{C_4} + \frac{C_3}{C_G}} \tag{5.19}$$

$$q_4 = q_G\left(1 + \frac{C_1 C_2}{C_G(C_1+C_2)}\right) + Q_2 + Q_3 - \frac{C_2}{C_1+C_2}(C_1(V_G - V_A) - Q_1) \tag{5.20}$$

and,

$$q_1 - q_4 + q_G = Q_1 + Q_2 + Q_3 \tag{5.21}$$

$$q_2 - q_4 + q_G = Q_1 + Q_2 \qquad q_3 - q_4 = Q_3$$

Which in the special case of $C_{1,\ldots,4} = C$ and $C_G = C/2$, cancel to give,

$$q_G = \frac{1}{6}\{C(V_B+V_A-2V_G) + Q_1 + 2Q_2 + Q_3\}$$
$$q_4 = \frac{1}{6}\{C(2V_B-V_A-V_G) - Q_1 - 2Q_2 - 4Q_3\}$$
$$q_3 = \frac{1}{6}\{C(2V_B-V_A-V_G) - Q_1 - 2Q_2 + 2Q_3\}$$
$$q_2 = \frac{1}{6}\{C(V_B-2V_A+V_G) - 2Q_1 + 2Q_2 + Q_3\}$$
$$q_1 = \frac{1}{6}\{C(V_B-2V_A+V_G) + 4Q_1 + 2Q_2 + Q_3\} \qquad (5.22)$$

The four junction turnstile device can be fully characterised by either equations 5.16-17, matrix equation 5.18 or equations 5.19-21. The simplified set of equations 5.22 will be used below to further explain the operation of the turnstile.

5.2.3 Turnstile Operation

Equations 5.16-21, although fully characterising the four junction gated turnstile, do not give an immediately transparent view of its operation. To visualise these processes more clearly, a device with equal junction capacitances C and gate capacitance C/2 (obeying equations 5.22) is considered as an example. It is biased by $V_A = -V_B = 0.35$ V/(e/C) and $V_G = 0.0$ or -2.0 V/(e/C). The results of potential calculations for this device are shown in figure 5.4. This indicates the potential landscape of the device for various combinations of applied gate voltage and excess electron position.

Consider first the numbered schematics of figure 5.4a, where a gate potential of −2.0 V/(e/C) is used to drag an electron into the array. The electron is inclined to tunnel to an electrode with a lower potential, but because of the Coulomb blockade effect it can only do so if the potential drop is greater than 0.5 V/(e/C). This drop is indicated by the 'I' bar in each diagram. As can be seen, the combined effect of both bias and gate potential is sufficient to allow tunnelling of a single electron into the central electrode. However once this point is reached, the drops in potential through the system are not great enough to allow further tunnelling. Further electrons from V_A are also effectively blocked. If the higher order processes of §4.5 can be ignored, then a stable configuration is the result.

Now consider an applied gate voltage of 0.0 V/(e/C), as shown in figure 5.4b. The effect of the applied bias potentials (perturbed by the presence of the excess electron itself) is sufficient to allow the electron's exit from the system, while also disallowing further tunnelling into the array. Thus, assuming the interplay of no higher order processes and sufficient time for each tunnelling event ($t >> R_tC$, where R_t is the nom-

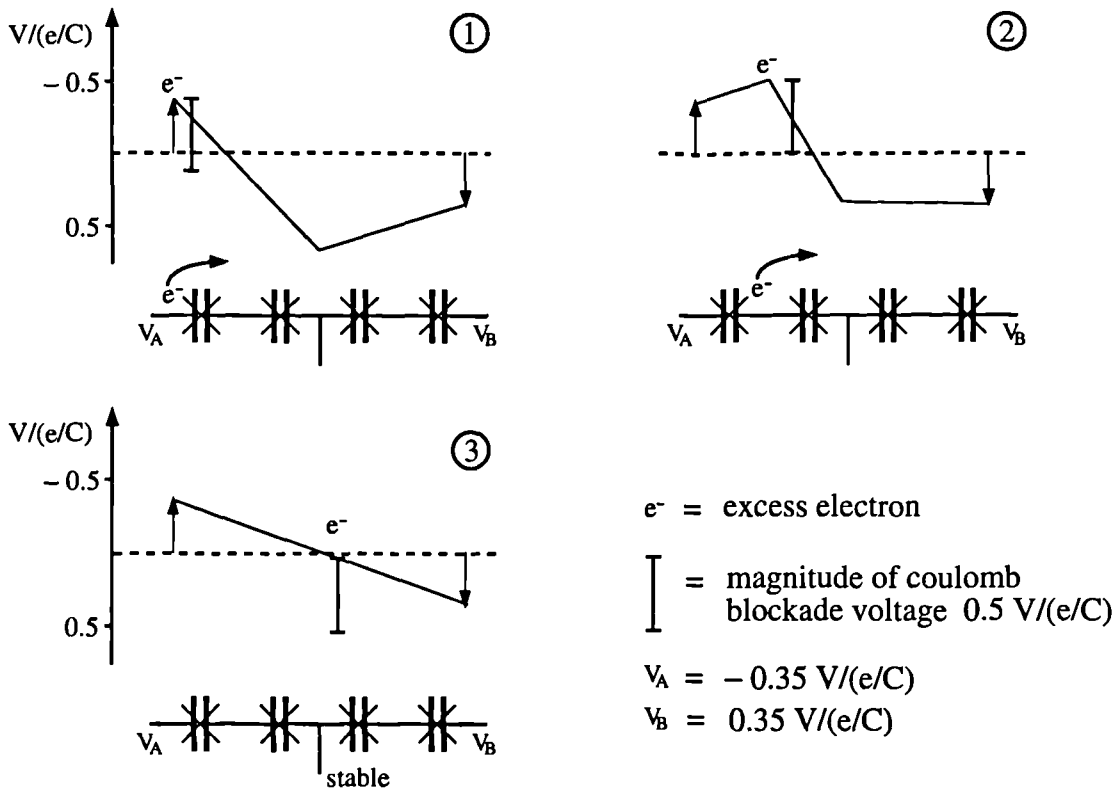


Fig 5.4a Schematic of the potentials found in a gated turnstile during injection of an excess electron. The turnstile has junctions with capacitance C and a gating (non-tunnelling) capacitance of C/2. A voltage of -2 V/(e/C) is applied at the gate for electron injection.

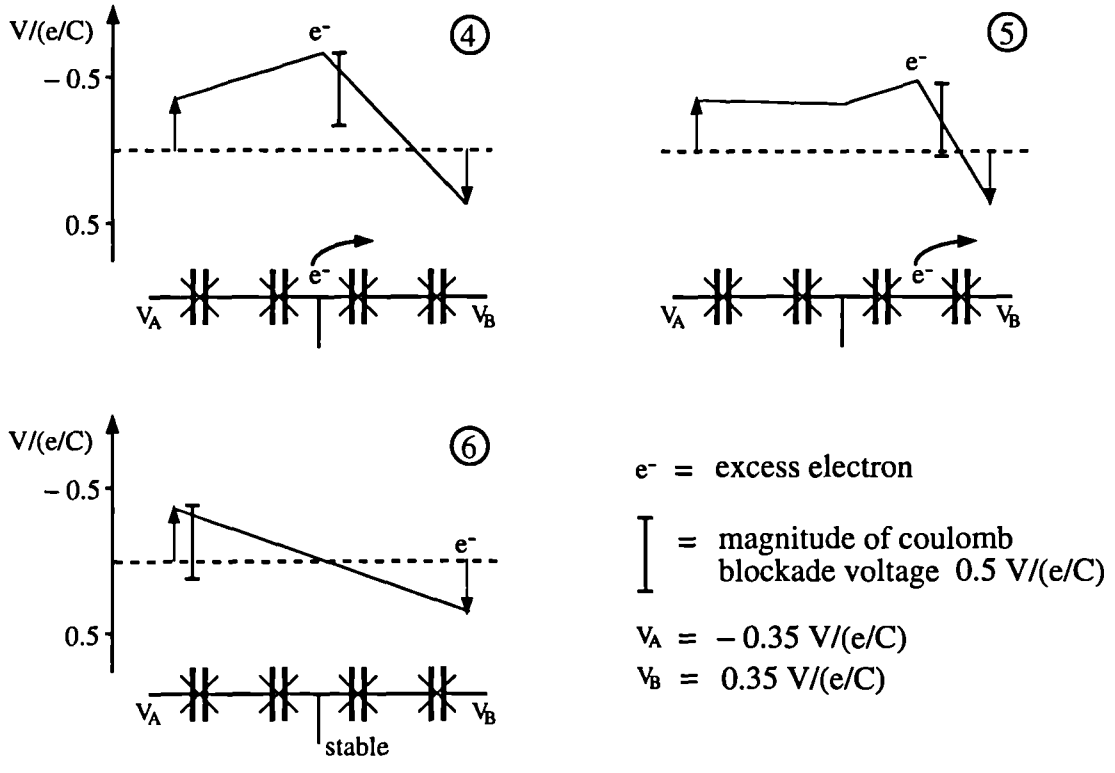


Fig 5.4b Schematic of the potentials found in a gated turnstile during ejection of an excess electron. The turnstile has junctions with capacitance C and a gating (non-tunnelling) capacitance of C/2. A voltage of 0 V/(e/C) is applied at the gate for electron ejection.

inal tunnelling resistance of each junction), the turnstile will clock one electron from V_A to V_B with each cycle of the gate voltage. The current is then governed by the frequency of the oscillating signal at V_G.

Although giving detailed explanation of the operation of the gated turnstile, such an analysis is of little use in providing information on the range of bias conditions under which turnstiling may occur. There is a simple technique that will allow easy access to such information; the method of *linear programming* developed below. However, in order to make use of this technique, the idea of *critical charges*, a concept suggested by Esteve [117] to reduce the complexity of modelling calculations, must be developed.

5.2.4 Concept of 'Critical Charges'

The technique of critical charges is most useful when considering systems consisting only of voltage sources and capacitive elements. By Thévenin's theorem the system is reduced to that of figure 5.5 consisting of the junction of interest (capacitance C, tunnelling resistance R_t) and the lumped effective capacitance of the rest of the equivalent circuit, C_{eff}.

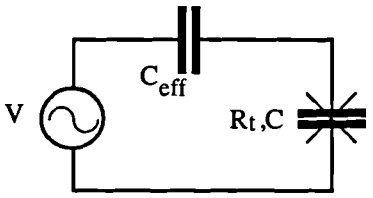


Fig 5.5 Thévenin equivalent circuit of a tunnel junction in series with the lumped remainder of the circuit, capacitance C_{eff}

The free energy of such a system is readily obtained in terms of the charges on these capacitances and a charge through the voltage source, Q_v, as

$$E = \frac{Q_{eff}^2}{2C_{eff}} + \frac{Q^2}{2C} + Q_v V \tag{5.23}$$

so that the energy change due to a tunnelling event in C is given by,

$$\Delta E = -\frac{eQ}{C} + \frac{e^2}{2}\frac{1}{C_{eff}+C} \tag{5.24}$$

which formula can be rewritten as,

$$\Delta E = -\frac{e(Q-Q_{critical})}{C}, \qquad Q_{critical} = \frac{e}{2(1+C_{eff}/C)} \tag{5.25}$$

This implies that the change in free energy of the system caused by a tunnelling event through any particular junction can be calculated in simple fashion from the initial charge across that junction, and it's relation to a critical charge for that junction. The critical charge is a parameter solely dependant on the system components, and not on

its particular bias conditions at any one time. It can be seen to be the charge above which, at $T \rightarrow 0$, conduction starts to take place through the junction, i.e the Coulomb blockade charge for the junction.

The idea of using critical charges originated in a desire to speed the calculation of the Monte Carlo model described in §5.1.4. $Q_{critical}$ values can be precalculated before entering the iterative loop, and junction charge values calculated in the loop instead of electrode potentials. Obtaining charge values requires the solution of a matrix equation such as 5.18, and in practice this process is less computationally expensive than the calculation of full potentials (although it is still an N^2 process).

Practical Application of Critical Charge Approach :

The structure of the code used to model the gated turnstile is described in Appendix E - Code Structures. A bespoke Monte Carlo routine was written, based on equations 5.19 - 5.21. This produced the initial modelling results of Chapter 6. Evolving from this bespoke code, a *General Network Solver* was developed, and is described in §5.3.2. This solver was used to obtain the bulk of the results of Chapter 6. It also relies upon the critical charge approach described above.

5.2.5 Device Operation, Linear Programming Approach

One consequence of using this critical charge approach is the development of the idea of *linear programming* as a simple way to discover the area of operation in control parameter/bias voltage space of the gated turnstile. The approach can also be extended to other more complex single electronic systems.

As an example of the use - and a description - of this linear programming technique, consider again the simple gated turnstile of figure 5.3 described by equations 5.22 (i.e with $C_G = C/2$). Further simplify the problem by requiring that $V_B = -V_A$. Then it can easily be seen that the formulae of 5.22 all have the form,

$$q_i = \alpha_i V_A + \beta_i V_G + \gamma_i \qquad \alpha,\beta,\gamma \text{ constants} \qquad (5.26)$$

where the ith junction, at $T \rightarrow 0$, will commence conduction at $q_i = q_{i\,critical}$. Equations 5.26 degenerate into straight lines in V_A, V_G space. Each of these divides control parameter space into regions in which a particular tunnelling event is or is not allowed. For more complex problems control parameter space is divided into regions by linear surfaces of higher dimension. The position of these demarcation lines for a

particular tunnelling event is solely dependant on fixed parameters (C_i and $q_{i\,critical}$ values) and the position of excess electrons in the system before tunnelling occurs.

This gives rise to a simple process for describing the stable area of operation of a system - a process which may be thought of as the inverse of the Monte Carlo technique. There, knowing bias voltages and excess charge positions, the charge across each junction can be calculated. These are then compared with $Q_{critical}$ values to find the next likely tunnelling event. In the linear programming approach decisions are first made as to which events are allowed and disallowed for the device to operate. The parameters of the system define $Q_{critical}$ values. These in turn uniquely define stable areas of device operation in voltage bias space

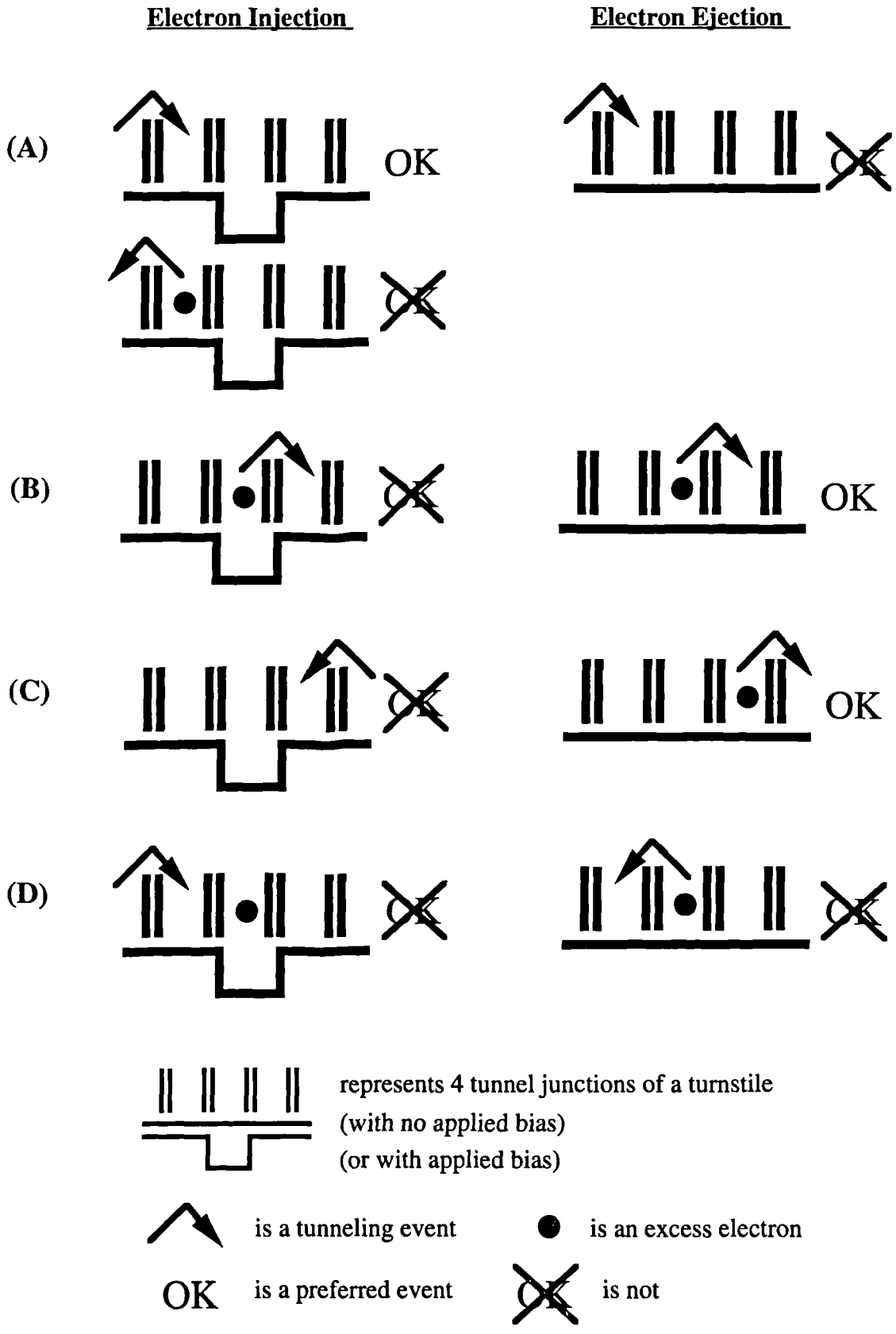
Figures 5.6 and 5.7 show the results of this process for the simplified gated turnstile. Figure 5.6 shows schematically the most important tunnelling events defining operation of the device, both for electron injection and ejection. Figure 5.7 shows the areas of legal operation for electron injection and ejection based on these tunnelling events. Critical lines in figure 5.7 are cross-referenced to their defining events in figure 5.6. It should be noted that in this example, particularly simple results are obtained. The defining equations give lines of equal gradient because of the equal capacitances of each tunnelling junction. There are a number of degeneracies (for instance, two types of tunnelling event give the same electron injection line, A). More realistic problems will give far more complex operating area diagrams. Also, we have assumed $T \rightarrow 0$. At finite temperature perfect turnstiling action will only occur well within the legal turnstiling area defined in figure 5.7.

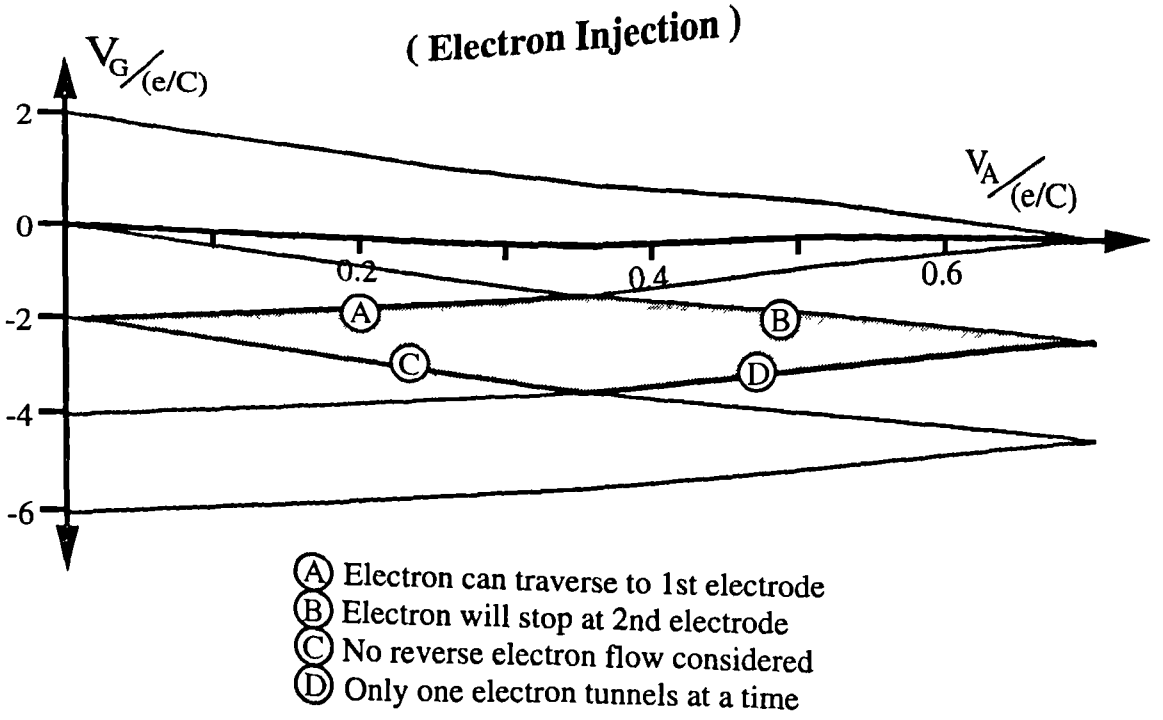
Note that because this approach is based on linear programming, and is simplified by the $T \rightarrow 0$ condition, computation times are linear with respect to the number of junctions in the system under analysis.

Summary :

The Monte Carlo modelling approach introduced in §5.1.4 has been improved by characterising systems on the basis of junction charges instead of electrode potentials. As noted in §5.1.4. this method is more efficient computationally, and allows greater preparatory calculation outside the main iterative loop of the algorithm. The charge profile of a system is obtained by solution of a simple governing matrix equation based on Kirchoff's Laws and charge continuity.
Another useful modelling tool has been developed from this critical charge approach to Monte Carlo modelling - the linear programming technique. This tool was introduced to specify the area of turnstiling action of a gated turnstile device in control

Fig 5.6 The following schematics describe the **important tunnelling events** which govern the operation of a gated turnstile.
The important allowed or disallowed events are split into those that concern injection of an electron into the device, and those which concern the ejection of the electron from the device. The reference letters A...D correlate with similarly lettered lines on the graph of legal turnstiling area in V_A,V_G space of figure 5.7. Each event corresponds to an associated bounding line of the legal turnstiling area.





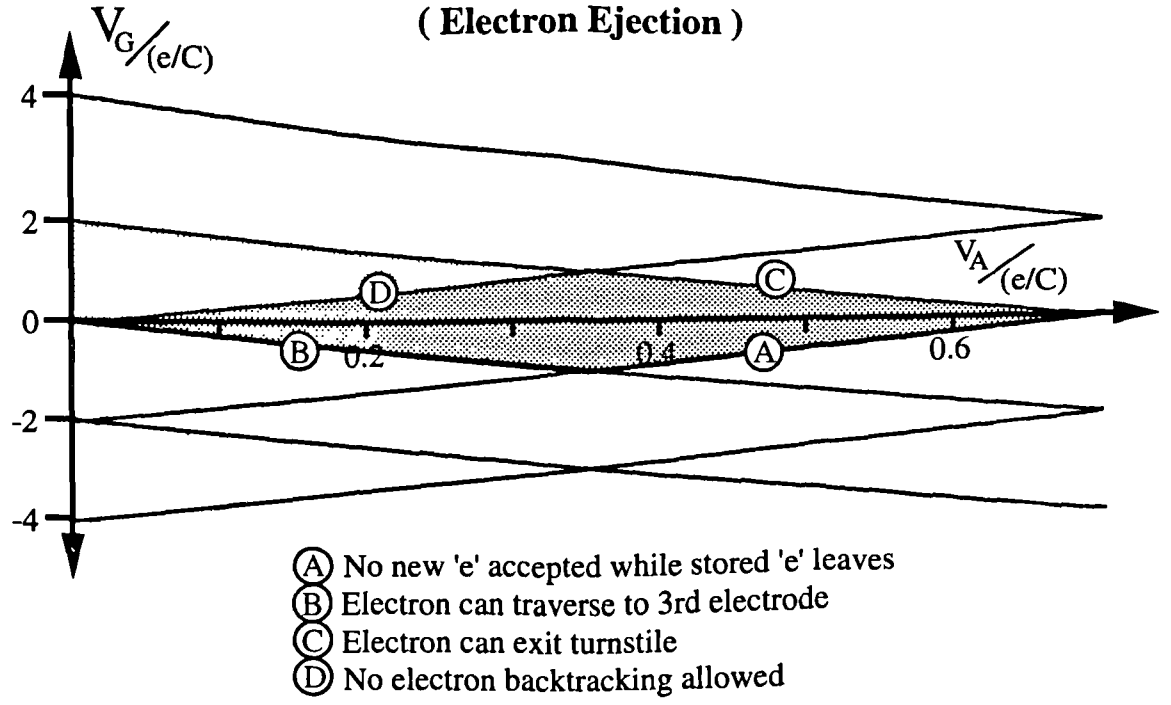


Fig 5.7 Schematic plots of **Legal Turnstiling Area** in V_G, V_A space for a gated turnstile. Heavy shading shows region of safe operation. Light shading shows region where reverse electron drift can occur at low bias voltages.

parameter space. It can be extended to consider operational modes of more general systems and the areas of control parameter space in which those modes legally operate. Compared with Monte Carlo calculation of stability in control parameter space, the linear programming technique is overwhelmingly more efficient in its use of computing time.

5.3 General Network Solver & Linear Programming Technique

The bespoke modelling techniques developed in sections 5.2 and 5.3 are extended to algorithms of general applicability. A general Monte Carlo simulator is described. Some of the devices and systems whose analysis might benefit from the use of such tools are noted.
The advantages and disadvantages of both the general network solver and the linear programming technique are discussed. The benefits of applying both methods in complementary fashion are noted.
Specific modelling results from the tools here developed are considered in Chapter 6.

5.3.1 The Need For General Simulation Tools

Having developed bespoke algorithms to model tunnelling junction arrays and gated turnstiling devices, we now wish to develop these routines to allow the modelling of general networks of components. Initially equivalent circuits consisting only of tunnelling junctions, pure capacitances and voltage sources will be considered. These tools are required for the following reasons;

Firstly, a set of general tools allow calculations to be performed on a wide range of differing systems without the need for extensive recoding and hand analysis of each system in turn. Even considering only the turnstiling devices, there are a wide variety of different designs. These employ many different sets of gated control voltages and buffer junctions. 3-phase devices have already been proposed and constructed [63, 109]. Other devices and systems have also been proposed, including the other basic requirement of a digital system - memory cells [61, 118]. Even systems based on the macroscopic quantum tunnelling effects generally considered undesirable have been suggested for correlated electron transport [119]. Rapid modelling of general systems would of course be useful; in leading experiment by testing the validity of new device proposals, in verifying the experimental results, and in optimising the component values and bias conditions of devices.

Secondly, as mentioned in §5.1.2, the physical geometry of many single electronic devices means that tunnelling junctions can no longer be assumed to obey 'parallel-plate' capacitance approximations. Fringing fields become non-negligible. As a result the system capacitance matrix is non-diagonal and 'next-nearest-neighbour' effects may play a significant rôle. Modelling tools, which can easily include such effects, would allow greater understanding of the constraints intercapacitance coupling might have on device operation.

Finally, it should be noted that any practical single electronic devices will be complex and extended systems subject to charging effects far less subtle than macroscopic quantum tunnelling or quantum fluctuations. The extreme sensitivity to external charge that makes tunnelling junction systems so suitable for use as electrometers ($i_n < 2\times10^{-4}$ eHz$^{-1/2}$ [11]) makes shielding and isolation of such devices critical. Vital questions which may be explored with general modelling tools, even those which only consider capacitive circuits, include;

- How well shielded do typical systems have to be before external charge seriously perturbs their operation ?
- Can systems be constructed which by their nature are tolerant to such external charge ?
- What range of system packing densities can be achieved where sections of a system will not adversely effect others ?
- Can systems be constructed which make use of correlated effects produced by this lack of charge isolation (analogous to the beneficial soliton effects in tunnelling junction arrays) ?

5.3.2 General Network Solver - Charge Profile Calculation

The principles which define the Monte Carlo modelling algorithm are laid out in §5.1.4. In brief, two main areas of calculation must be performed. Firstly, critical charge values must be obtained for each tunnelling junction in the system. Then an iterative loop is entered, which repeatedly calculates the system charge profile. This is compared with the critical charge profile, and equations 5.25 and 4.11 used to choose the next tunnelling event to occur. Associated with this core algorithm are routines that extract desired 'experimental' information; IV curves, number of electrons through turnstile, etc.
In this section, the algorithm to calculate the charge profile of a general circuit network is considered in detail.

Predefined matrices are used to input circuit information to the general solver. As an illustrative example, consider the matrices that describe the turnstile of figure 5.3.

$$
\begin{aligned}
\texttt{Volts} &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & V_A & V_B & V_G \end{bmatrix} \\
\texttt{Elas} &= \begin{bmatrix} \frac{1}{C_1} & \frac{1}{C_2} & \frac{1}{C_3} & \frac{1}{C_4} & \frac{1}{C_G} & 0 & 0 & 0 \end{bmatrix} \\
\texttt{Conn} &= \begin{bmatrix} 1 & 1 & 0 & 0 & -1 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 & 1 & 0 & -1 & 1 \end{bmatrix} \\
\texttt{Qcon} &= \begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 1 \\ 0 & 0 & 1 & -1 & 0 \end{bmatrix} \\
\texttt{Zcon} &= \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \end{bmatrix}
\end{aligned}
\qquad (5.27)
$$

Here the elements of `Volts` and `Elas` are the initial bias voltages and elastances of each component of the gated turnstile, numbered 1-8 in figure 5.3. (As can be seen, a general rule is made to number the circuit components in the sequence; tunnelling junctions, other non-tunnelling capacitances, voltage sources. This ensures easier coding of the algorithm.) Each row of the connection matrix `Conn` describes a loop in the device equivalent circuit, each column the presence of a particular component in that loop. The sign of an element of `Conn` signifies the direction of nominal current flow through each component.

The information contained in these matrices is enough to form equations based on Kirchoff's Laws, but to include charge continuity and form a soluble set of circuit equations two other pieces of information must be available. Firstly, information on the possible sites of excess electrons is contained in `Qcon`. It has as many rows as there are electrodes in the equivalent circuit that can support excess electrons. Its columns note which capacitive components effect the charge on this electrode.

Also cases like that shown in figure 5.8 must be taken into consideration, where the charges on junctions C_1 and C_2 must be equal by symmetry. Such situations are found to be rare in practice, but must be included to ensure that the matrix equation governing circuit operation is always soluble. The matrix `Zcon` is used to store the information which defines such situations.

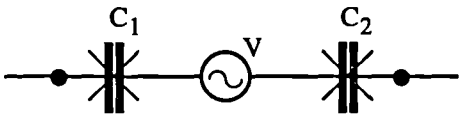


Fig 5.8 Equivalent circuit components requiring the matrix `Zcon`.

Having defined these matrices, solution of the system charge profile becomes simple. Two matrices, `Econ` and `Vcon`, are obtained from the elastance and bias voltage portions of `Conn` by multiplying by the component values in `Elas` and `Volts`. If $\mathbf{q}$ represents the vector of capacitance charge values in the circuit, and $\mathbf{Q}$ the vector of excess charge value on circuit electrodes, then

$$\begin{aligned} \text{Qcon} \,.\, \mathbf{q} &= \mathbf{Q} \\ \text{Econ} \,.\, \mathbf{q} &= -\text{Vcon} \,.\, \mathbf{1} \\ \text{Zcon} \,.\, \mathbf{q} &= \mathbf{0} \end{aligned} \tag{5.28}$$

completely define the charge profile of the system. For the example described by matrices 5.27, these give;

$$\begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 1 \\ 0 & 0 & 1 & -1 & 0 \\ \frac{1}{C_1} & \frac{1}{C_2} & 0 & 0 & -\frac{1}{C_G} \\ 0 & 0 & \frac{1}{C_3} & \frac{1}{C_4} & \frac{1}{C_G} \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \\ q_3 \\ q_4 \\ q_G \end{bmatrix} = \begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \\ V_G - V_A \\ V_B - V_G \end{bmatrix} \tag{5.18}$$

Having obtained such a matrix equation, solution for $\mathbf{q}$ can be performed by standard linear algebra toolbox routines, such as those provided in FORTRAN by the Numerical Algorithms Group [120].
Code structures that perform the operations of forming and solving such matrix equations are presented in detail in Appendix E - Code Structures.

5.3.3 General Network Solver - Critical Charge Calculation

Of more complexity is the problem of calculating a vector of $\mathbf{q}_{crit}$ values from the circuit information matrices. As described in §5.2.4, the procedure is to form a Thévenin equivalent circuit around the junction of interest, with C_{eff} signifying the Thévenin lumped capacitance (see figure 5.5). Then equation 5.25 can be used to calculate one q_{crit}. This in itself is trivial. The complexities arise in automating the calculation of a series of C_{eff} values.

Solution of this problem comes through using the circuit *impedance matrix*. A network of components can always be split into meshes or loops ringed by circuit elements. The square impedance matrix has rank equal to the number of such loops. Its diagonal elements equal the total impedance of a loop and off diagonal elements the total shared impedance of loops (i.e element (1,2) is the sum of impedance common to loops 1 and 2). As such, the matrix is symmetric and positive definite.
Such a matrix can be partitioned into four submatrices. An example of such a partitioning for an arbitrary 3×3 matrix is given below in equation 5.29

$$\mathbf{Z} = \begin{bmatrix} Z_{11} & -Z_{12} & -Z_{13} \\ -Z_{12} & Z_{22} & -Z_{23} \\ -Z_{13} & -Z_{23} & Z_{33} \end{bmatrix} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix} \qquad \text{with,}$$

$$\mathbf{A} = \begin{bmatrix} Z_{11} & -Z_{12} \\ -Z_{12} & Z_{22} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} -Z_{13} \\ -Z_{23} \end{bmatrix} \quad \mathbf{C} = [-Z_{13} \; -Z_{23}] \quad \mathbf{D} = Z_{33} \qquad (5.29)$$

One property of this impedance matrix is that the effect of loops in which we have no interest can be merged into the rest of the loops mathematically - an *effective* impedance matrix resulting. For instance, if **Z** is partitioned into **A, B, C, D** then a matrix,

$$\mathbf{Z_{eff}} = \mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C} \qquad (5.30)$$

is equivalent to **Z** in a reduced network.

In our solver, all loops other than those containing the junctions of interest are merged. For a two dimensional network this gives a reduced $\mathbf{Z_{eff}}$ matrix with one or two loops. Figure 5.9 below shows the two possible results (no further simplification is made for code performance reasons). Calculation of the Thévenin impedance is now simple and immediately leads to the critical charge for the junction of interest.

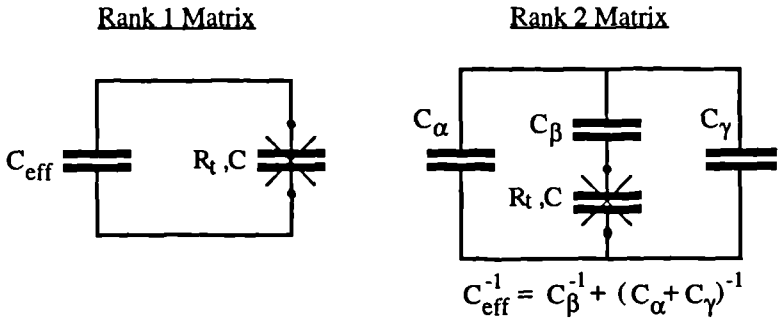


Fig 5.9 Equivalent circuit diagrams for possible reduced $\mathbf{Z_{eff}}$ matrix results.

This automates the processes of finding critical charge values for each junction in a general system, and for calculating the potential profile of that system. It allows construction of a fully automated general Monte Carlo modeller (referred to as the General Network Solver) for capacitive single electronic systems. Detailed coding structures of the modelling algorithm are shown in Appendix E - Code Structures.

Tracking single electrons through a single electronic system by Monte Carlo modelling is a computationally expensive and thus often slow process. For example, calculation of the IV curve of figure 6.2 took a little over 1.5 hours of CPU time on an IBM 3090 mainframe (with associated vector processor) using optimised VMS FORTRAN code. The curve was produced by tracking 7×10^4 electrons through a 8 junction array for 200 data points.

However, the general network solver has the advantage of being extremely flexible in the data which it can collect from the system under test. IV curves, average electron event times through particular components, areas of device operation, and many other

results are all as simple to produce. The process can also give results for both $T \rightarrow 0$ and finite temperatures with only minor modification. It should also be easily extensible to deal with quantum fluctuations in the system based on the quantum Langevin approach discussed in §4.2.1.

5.3.4 Linear Programming

Extension of Linear Programming Techniques to General Systems :

The principles of the linear programming technique are presented in §5.2.5, using the example of a simple gated turnstile device. It would be beneficial if this algorithm could be automated and extended to more general single electronic systems.
From §5.2.5 it can be seen that this is a twofold process. Firstly a method of obtaining q_{crit} values must be found. Secondly, a procedure must be devised for deciding which events are critical to device operation. The problem of obtaining q_{crit} values has already been solved above - and thus the main section of any linear programming code simply uses the same routines developed for the general network solver. However the procedure for choosing critical state transitions is far from trivial and work on its automation is still in progress.

The number of possible state transitions is one source of problems. If equation 5.26 is used as a basis, then the number of linear programming lines in control parameter space is the product of N (the number of tunnelling junctions) and the number of possible states of the system.
Also the state transitions that might be assumed to be critical are often discovered not to be, when plotted by linear programming code. An example of this may be found in the injection of electrons into the four junction turnstile discussed above. It is a requirement for device operation that electrons must be able to tunnel from the first to middle electrode of the system. Such an event is in fact irrelevant to the area of stable device operation - it turns out to be an automatic consequence of biasing conditions allowing an electron to tunnel to the first electrode itself. Another example concerns the reverse tunnelling of electrons at low bias voltages in the same four junction turnstile. Superficial consideration assumed that with forward bias of the system, reverse current could be ignored (events C and D of figure 5.7). More detailed modelling with the general network solver shows this not to be the case - there is significant reverse leakage current.

Combined Use of Linear Programming and Monte Carlo Techniques :

For more complex systems it becomes progressively more difficult to make initial guesses of the tunnelling events that will be found to be important, and so a combination attack with the general network solver and linear programming model is employed. Initial guesses of critical events are fed to the linear programming model. Then based on its results, a coarse grid of tests in control parameter space is made with the general network solver for verification. If errors have been found in the initial choice of allowed and disallowed events, adjustments are made. The general network solver is used to probe those areas of control parameter space in which the operation of the device is unclear. Often it is found that in some areas of control parameter space a different sequence of state transitions than that anticipated is the major route for electron flow. There may be more than one set of state transitions leading to identical final outcomes. Examples of such processes may be found in figures 6.12 and 6.13 of §6.2.2 below.

The main advantage of the linear programming method is its ability to produce results in 'real time' (usually the computation time involved is of the same order as the time required to display the results). Its disadvantages include the need for experience and insight on the operator's part in choosing which allowed and disallowed events to plot. Also the limitation of working most effectively as $T \rightarrow 0$. Thus, when analysing the area of operation of a system in control parameter space by this method, the advantages of linear programming can be fully applied, while its disadvantages are largely counteracted by the limited use of the far slower general network solver.

5.4 Summary

Tunnelling junction arrays and gated turnstiles have been considered in detail. Their possible rôle as sub-units of integrable single electronic systems has been noted. Simple equivalent circuits have been constructed to model their operation, and in the process Monte Carlo based routines and a linear programming technique have been developed. These techniques have greatly aided the analysis of arrays and turnstiles.

The modelling techniques were then extended to deal with general systems of junctions, capacitances and voltage sources. The Monte Carlo routines were optimised by using the concept of critical charges, and a General Network Solver developed. This gives tools that are more effective in analysing extended single electronic systems. The effects of system component variation, interdevice coupling and external noise can now be studied more easily. More complex device equivalent circuits (such as those including 'next-nearest-neighbour' coupling) can also be easily analysed. For the specific calculation of regions of system operation in control parameter space it is found that a combination of both tools, combining the speed of the linear programming process with the flexibility and immunity to operator error of the general network solver, are a great aid in fully characterising systems.

There are three obvious extensions that could be made to our present tools;

- Consideration of system quantum fluctuations, as well as the thermal fluctuations already accounted for in the simple microscopic model. This might be done by the heuristic approach of the quantum Lengevin equation as noted in Chapter 4. It would involve a change in the tunnelling rate calculation of the general network solver. Instead of using equation 4.11, equation 4.21 would be applied. This would involve more complex calculations, but would require little recoding of existing computer programs.
- Inclusion of resistive and inductive elements in the allowed equivalent circuit models. This would involve extensive recoding of existing programs, but no change to the structure of the algorithms themselves. However, theory assumes complete relaxation of the system between tunnelling events. Care must be taken to avoid violating this condition. The modelling tools would therefore be of most use for devices operating only at low frequencies.
- Full automation of the linear programming technique. This requires study of the rules governing which sets of state transitions allow a system to move from its initial state to a desired final state. Knowledge of the allowed sets of intermediate states immediately leads to critical allowed and disallowed events which the linear programming method maps to a stable area in control parameter space.

CHAPTER 6 APPLICATION OF SIMULATION TOOLS TO SINGLE ELECTRONIC SYSTEMS

A set of simulation tools for single electronic devices have been developed. They are now applied in the investigation of;

- idealised single electronic sub-systems (gated and ungated junction arrays),
- more realistic models of such sub-systems (subject to component deviation and static stray charge),
- groups of capacitively coupled devices - i.e small idealised systems.

The basic single electronic sub-systems considered in the literature are the tunnelling junction array and the gated turnstile device. These fulfil the rôles of transmission line and control device for single electronic signals. They were the devices used to aid the development of our simulation tools, and are described in detail in Chapter 4. In this chapter the results of modelling such systems are presented.

Results are also presented for the modelling of a number of systems *based* on the junction array and gated turnstile. Arrays are considered, where junction and grounding capacitances may vary randomly about a norm (representing the natural variation in component values resulting from a fabrication process). We also consider a multi-phase system, where more than one control voltage is applied to the turnstile in an attempt to improve device performance.

Finally, the natural effect of device integration - stray coupling capacitance and the subsequent device cross-talk produced - is investigated. Pairs of tunnelling junction arrays and four phase gated turnstiles are linked by a simple coupling model, and the effect of varying coupling capacitance considered.

Choice of Grounding Capacitance Values :

Much of this work was carried out before the results of Chapter 3, which indicates a C_0/C value of the order 2 to 10 for typical fabrication techniques. An assumption of $C_0/C = 0.1$ is made in the literature analysing tunnelling junction arrays [12, 106], and for gated turnstiling devices a common assumption is $C_G/C = 0.5$ [9]. Thus, many of the results presented below follow these assumptions. The effect of raising C_0/C by an order of magnitude will be discussed separately for each system.

6.1 Tunnelling Junction Arrays

6.1.1 Junction Arrays Under Idealised Conditions

Initial modelling considered homogeneous arrays, with both junction and grounding capacitances constant (as in the work of Bakhvalov *et al.* [12]). The theoretical work of §5.1.3 indicates that such arrays will show correlated electron flow most clearly.

Steady State Soliton Densities :

The first results, those of figure 6.1, show the concentration of solitons in a 22 junction array. Such a result would be extremely difficult to measure in any physical system. However, it does allow a number of comparisons between junction array theory and Monte Carlo modelled results. It also demonstrates most obviously the correlation of system charge.

A negative bias is applied to *both* ends of the array, injecting electrons and forming a set of soliton states. $C_0/C = 0.1$ produces solitons $\lambda^{-1} \approx 3.2$ junctions long. From equation 4.11 the first injection is expected to occur at $V_{thresh} \approx 1.3$ V/(e/C), thereafter a 'devil's staircase' being formed. The period of this staircase (the point when all junction sites are filled and double solitons begin to form) is twice $\Delta V = 5$ V/(e/C) The low temperature graph of figure 6.1 ($\beta = 100$, where $\beta = T_c/T$) clearly shows this space correlation of charge, and the entry of each excess electron into the array can be seen as bias voltage U is raised. Random fluctuations are suppressed by Coulomb blockade and mutual repulsion of solitons. The period of the staircase is indeed twice 5 V/(e/C), and the first full 1-electron jump in <n> does occur at $V_{thresh} \approx 1.3$ V/(e/C).

Figure 6.1 also shows the effect of raising the modelled temperature closer to T_c. These results essentially follow the work of Bakhvalov *et al.* However, in that work the smooth average of soliton density is plotted for an assumed infinite number of tunnelling events. The results of figure 6.1 are based on 500 tunnelling events, and clearly show the transition from strong correlation to a 'shot noise' governed density. This noise is caused by constant thermal production, and subsequent annihilation, of soliton-antisoliton pairs.

Finally, note two small half-electron jumps in the graphs at $U = 0$ and just below $U = V_{thresh}$. These are caused by errors in the coding of the modelling routines which erroneously include an average of electrons passing through the voltage sources. The simple array model was also found to be very susceptible to round off error in the cal-

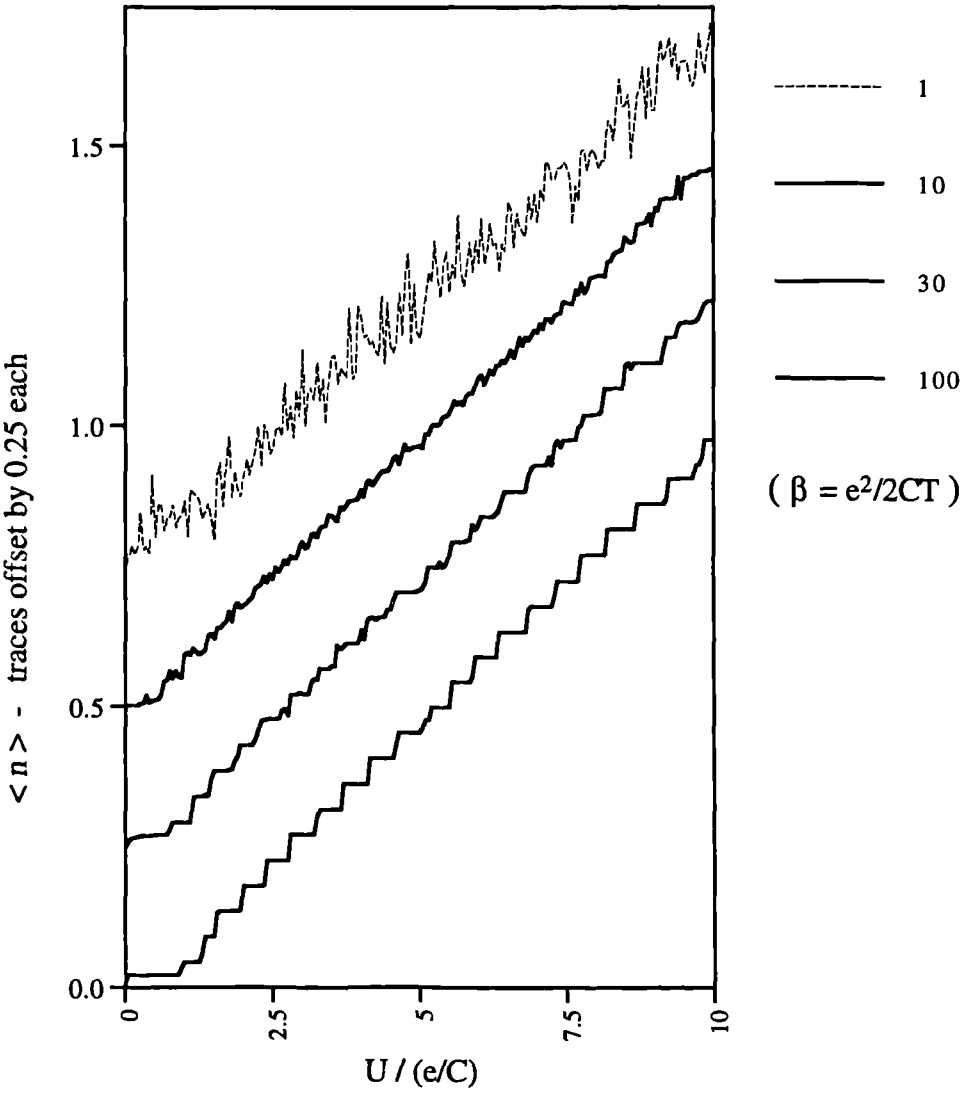


Fig 6.1 Average concentration of solitons in a tunnelling junction array versus bias voltage U. (see figure 5.1)

Calculation by Monte-Carlo technique averaging over a 'snapshot' of 500 tunnelling events. Array has 22 junctions with all tunnelling capacitances similar and all grounding capacitances similar. $C_o/C = 0.1$

Each trace is offset by 0.25 for clarity and has $\beta = T_{critical}/T$, $T_{critical} = e^2/2C$

culation of potentials. The algorithm (equations E.2 of Appendix E) calculates potentials iteratively based on potential differences that may be vanishingly small at the ends of a sparsely populated array. Such errors increase exponentially with array length. In the worst case, 10% errors in potential were noted in a 35 junction array. Such coding errors were resolved in further modelling programs.

Current / Voltage Response :

The second set of results, array IV curves, are more conducive to experimental measurement. Figure 6.2 shows the classic Coulomb blockade curve for an array at low temperature (in this case $\beta = 100$). Again $V_{thresh} \approx 1.3$ V/(e/C) for $C_o/C = 0.1$. As predicted in §5.1.3, the current rises sharply at this threshold voltage before approaching the expected gradient defined by the tunnelling resistances of the system. Such an IV curve is characteristic of extended solitons in systems with $C >> C_o$.
Figure 6.3 shows the equivalent results for systems with smaller $\lambda^{-1} = 1.8$ with data points calculated from only 1000 tunnelling events again at $\beta = 100$. The threshold voltage is now closer to $V = e/2C$, and less of a 'knee' is noted in the curve above threshold (although the variation of data points makes this a little more difficult to see). Comparing traces for 10 and 25 junction arrays with equivalent tunnelling resistances we verify that current is in the ratio 25:10 as expected.

Computation of these basic results is vital in preparing the techniques required to deal with more complex systems.

6.1.2 Non-Homogeneous Array Systems

In any physical system, it is impractical to expect tunnelling junctions and grounding capacitances to have uniform value. For hanging resist fabrication, estimates of variation in components of $\times 2\, R_{junction}$ and $\times 1.25\, C_{junction}$ have been reported [50]. We investigate junction arrays with differing levels of component variation and the operational stability of such systems.

The model used is that of equation 5.5 of §5.1.2. Here ζ_i and η_i represent the fractional variation in junction and grounding capacitances C_i, C_{oi} from some nominal C. In these results, ζ_i and η_i are formed from a Gaussian distribution,

$$P(\zeta_i;\sigma)\, d\zeta_i = \frac{1}{\sqrt{2\pi}\,\sigma} \exp\left[\frac{-(\zeta_i-1)^2}{2\sigma^2}\right] d\zeta_i \qquad (6.1)$$

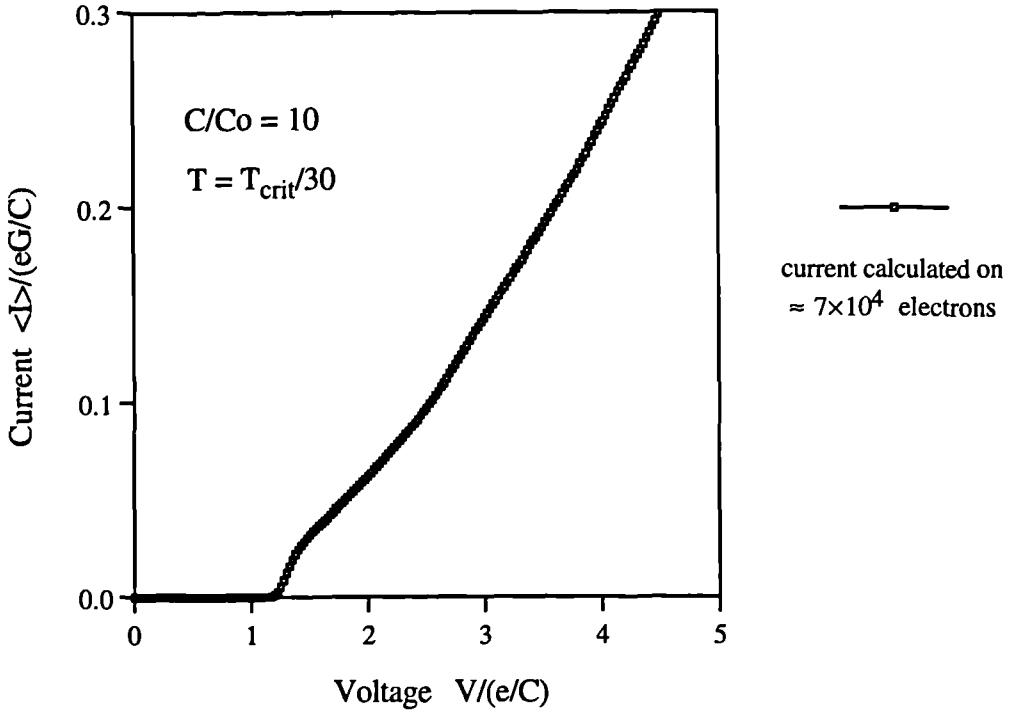


Fig 6.2 IV curve for a 8 junction array obtained through Monte Carlo modelling. Curve is produced from 5×10^5 tunnelling events, and thus follows approximately 7×10^4 electrons

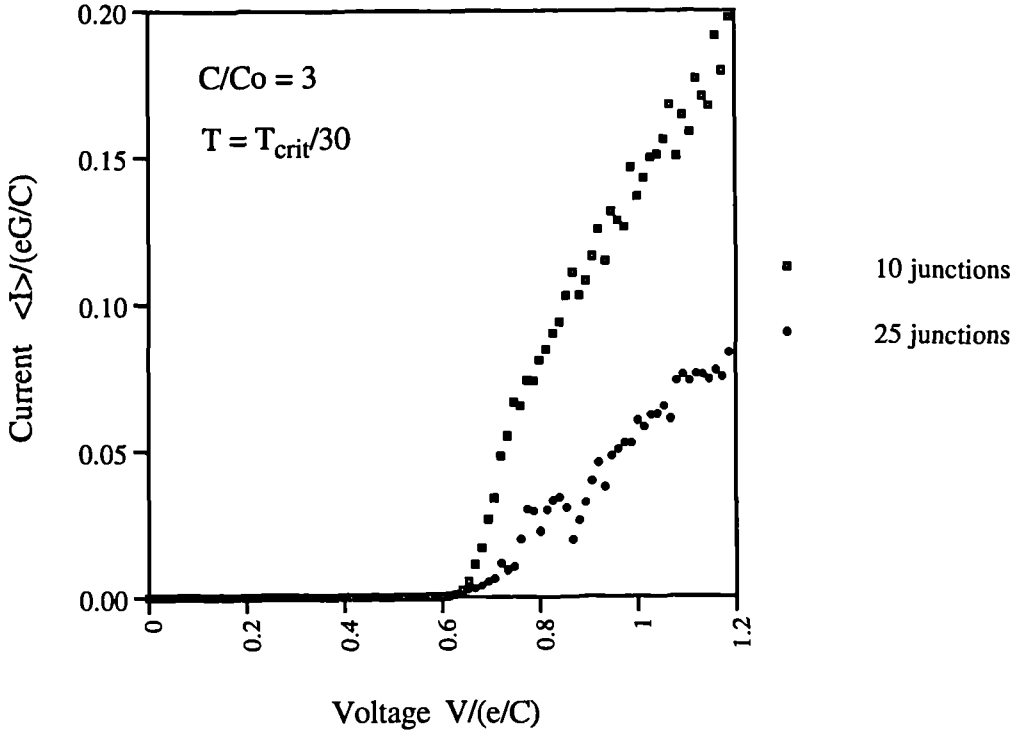


Fig 6.3 IV curves for 10 and 25 junction arrays obtained through the Monte Carlo modelling of 1000 tunnelling events.

This method most effectively models the variation due to *linear* misalignment errors in fabrication processes, giving a preponderance of very small capacitance values. It is preferred over the more obvious method, forming ζ_i,η_i from the logarithm of a Gaussian about zero.

Steady State Soliton Density :

Figure 6.4 is a recalculation of the steady state soliton array density in a 22 junction array. It shows the average soliton concentration in a negatively biased array as a function of bias voltage U. Here each trace has $T \rightarrow 0$ and both C and C_o values are varied. The 'average fractional deviation' is σ of equation 6.1. The ζ_i,η_i are uncorrelated; i.e the variation on junction i is totally independent of the rest of the system. There is also no correlation between traces, a new array is calculated for each modelling run. $\sigma = 0.43$ was chosen as a maximum in this system, as it was the point where breakdown regularly occurred and spatial charge correlation was destroyed.

Note that the system does still exhibit spatial charge correlation under relatively high values of component variation. This implies that tunnelling junction arrays may be resistant to large fabrication variations in their parameters. However, even below breakdown, increasing junction deviation can greatly modify the soliton distribution. Specifically, the regularity of threshold voltages is destroyed. At some threshold points multiple solitons may enter the array.

To see more clearly the basis of this effect, consider an array where only the ith grounding capacitance is varied,

$$-C\phi_{i-1} + (2C+\eta C_o)\phi_i - C\phi_{i+1} = Q_i \qquad (6.2)$$

This can be trivially recast as,

$$\Rightarrow \quad -C\phi_{i-1} + (2C + C_o)\phi_i - C\phi_{i+1} = Q_i - (\eta-1)C_o\phi_i \qquad (6.3)$$

where $(\eta-1)C_o\phi_i$ acts as an additional effective fractional charge. The variation of grounding capacitance can be viewed as the introduction of a new soliton into the array. This 'soliton' is spatially fixed and potential dependant. An $\eta < 1$ variation will induce a positive charge that will repel any other positive solitons in the array. Figures 6.5 and 6.6 show the potential barrier induced by variation of a single junction or grounding capacitance. They graph the energy of an array system as a real soliton is brought steadily closer to the component anomaly. The energy scale is compared with the energy of a lone soliton in an infinite homogeneous array,

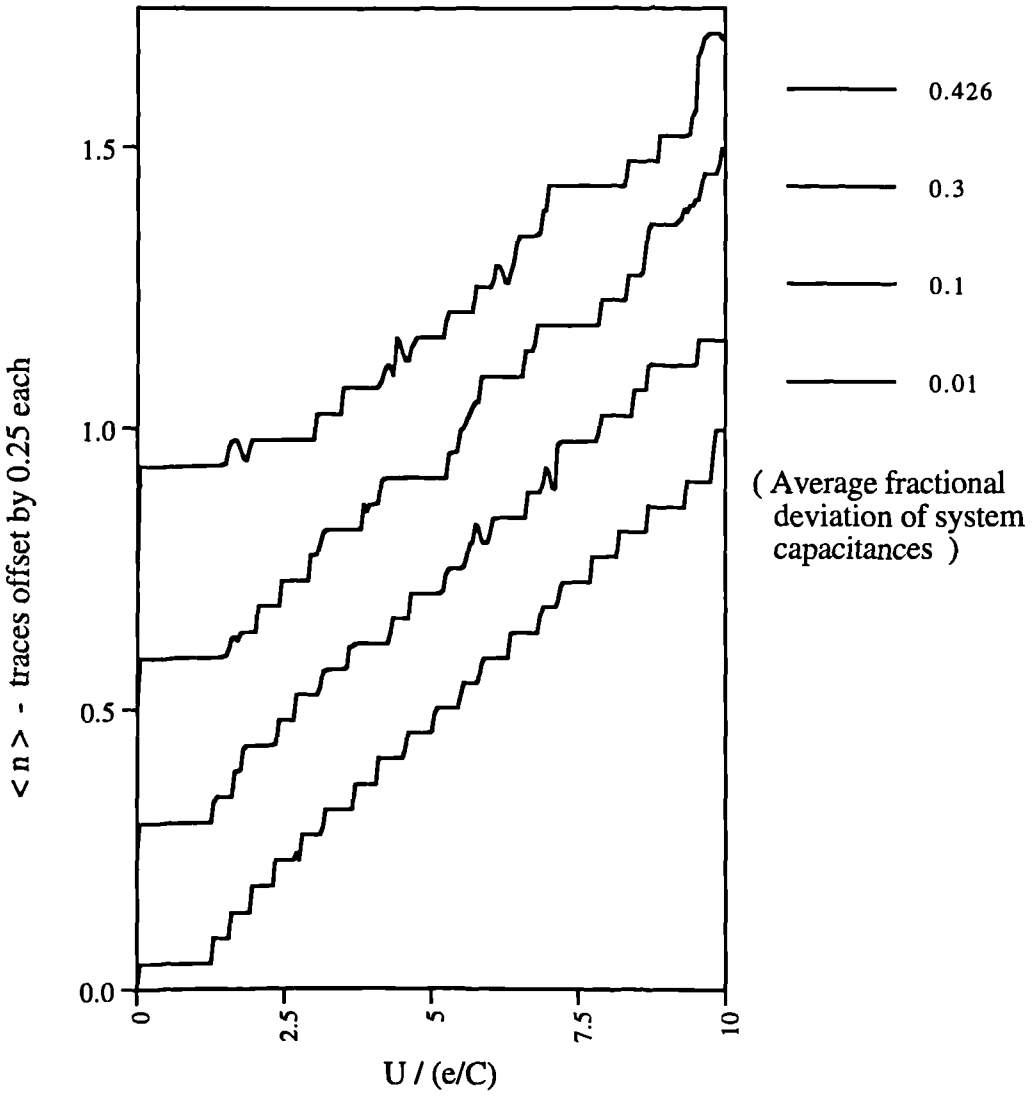


Fig 6.4 Average concentration of solitons in a tunnelling junction array versus bias voltage U. (see figure 5.1)

Calculation by Monte-Carlo technique averaging over a 'snapshot' of 500 tunnelling events. Array has 22 junctions with a nominal Co/C = 0.1

Both Co & C values have a random (gaussian) fractional deviation applied to each individual capacitance. Deviations are calculated anew for each trace, which are offset by 0.25 for clarity.

$$E = \frac{1}{2} e^2 (C_o^2 + 4CC_o)^{1/2} \qquad (6.4)$$

Note that only one half of the potential barrier is shown. It is symmetrical about the component anomaly.

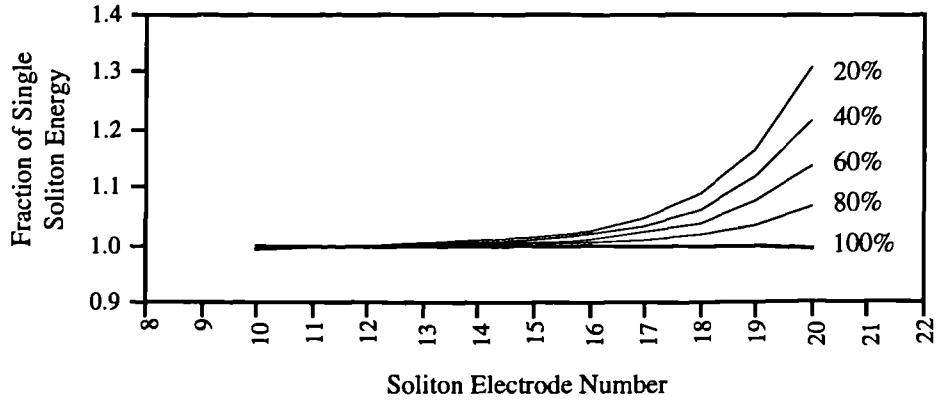


Fig 6.5 Graph of system energy versus soliton position for a junction array with a single perturbed grounding capacitance. The grounding capacitance of electrode 20 in an otherwise homogeneous 30 junction array is reduced to 20-100% of its original C_o value. The array has $C_o/C = 0.1$. System energy is calculated as a soliton is moved from electrode $10 \rightarrow 20$. Energy is scaled to that of a lone soliton in an infinite junction array.

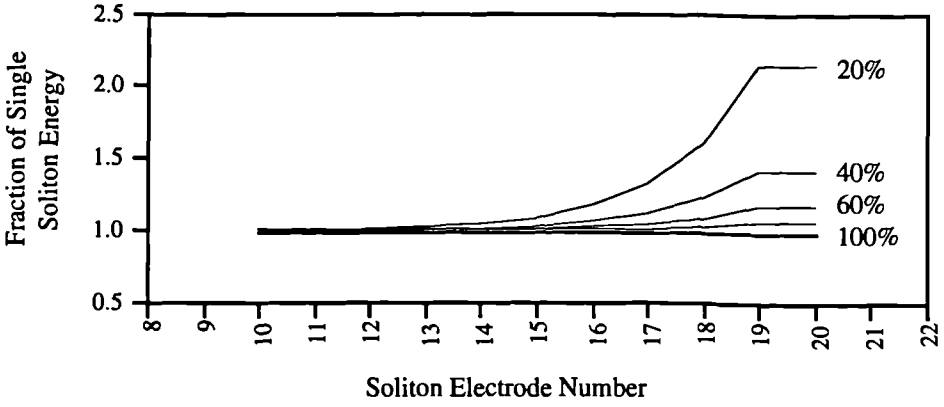


Fig 6.6 Graph of system energy versus soliton position for a junction array with a single perturbed junction capacitance. The junction capacitance of electrode 20 in an otherwise homogeneous 30 junction array is reduced to 20-100% of its original C value. The array has $C_o/C = 0.1$. System energy is calculated as a soliton is moved from electrode $10 \rightarrow 20$. Energy is scaled to that of a lone soliton in an infinite junction array.

Comparing these results to the interaction of two real array solitons is instructive. There, the system energy is also maximum when both solitons are simultaneously at the same electrode. At this point a system energy of 4E is obtained. The decay of the barrier with position is exponential with decay constant λ (the inverse of soliton length). In the above graphs the decay constant is 2λ. This is a result of the potential dependence of the effective charge $(\eta\text{-}1)C_o\phi_i$.

Thus component variation imposes additional potential structure in a tunnelling junction array. This structure modifies the value of threshold voltages. However the potential landscape can induce the movement of solitons until stability occurs. Potential wells 'plugged' by excess electrons mean that a number of solitons can exist even without external bias voltage. This self stabilising further suggests that tunnelling junction arrays may be resistant to large fabrication variations in their parameters. However to test this fully we must consider results that are more applicable to experiment than steady state soliton density.

Threshold Voltage as a Figure of Merit :

As noted in the previous section, the IV curve of a tunnelling junction array is simple to model, as well as being applicable to experiment. However, although IV curves are easily modelled for a specific array, they are unwieldy as a source of information about comparative array quality. A single array can yield many widely differing IV curves depending on bias conditions. A simple figure of merit would be useful in considering such devices.

Experience comparing many sets of IV curves led to the choice of *threshold voltage at zero offset bias* (i.e applied potentials at the ends of the array are equal and opposite) as such a figure of merit. High V_{thresh} is generally favourable for practical device operation. Even though component values in an array may be perturbed quite radically, the threshold voltage will remain approximately constant if breakdown does not occur. However, as larger component deviations induce the onset of breakdown, the value of modelled threshold voltage is found to increase radically. Such an increase would not be found in a physical system. Instead of developing an increased Coulomb blockade voltage, the physical tunnelling junction array would become unstable with respect to component deviation. In the models such instability is characterised by large jumps in threshold voltage (caused mathematically by exceptionally small capacitance values in the array model).

Results of Threshold Voltage Calculations :

Figures 6.7 - 6.9 show the variation of threshold voltage versus component deviation for various C_o/C values of a 21 junction array. Arrays are studied where either junction capacitance, grounding capacitance, or both components are varied.

From these graphs it can be seen that ;

- the highest stable V_{thresh} values occur when grounding capacitances, C_o, are small compared with junction capacitances, C.
- At deviations of less then 30%, in the range $0.1 < C_o/C < 10$, tunnelling junction arrays are found to be stable. When the deviations exceed 30%, either if both C

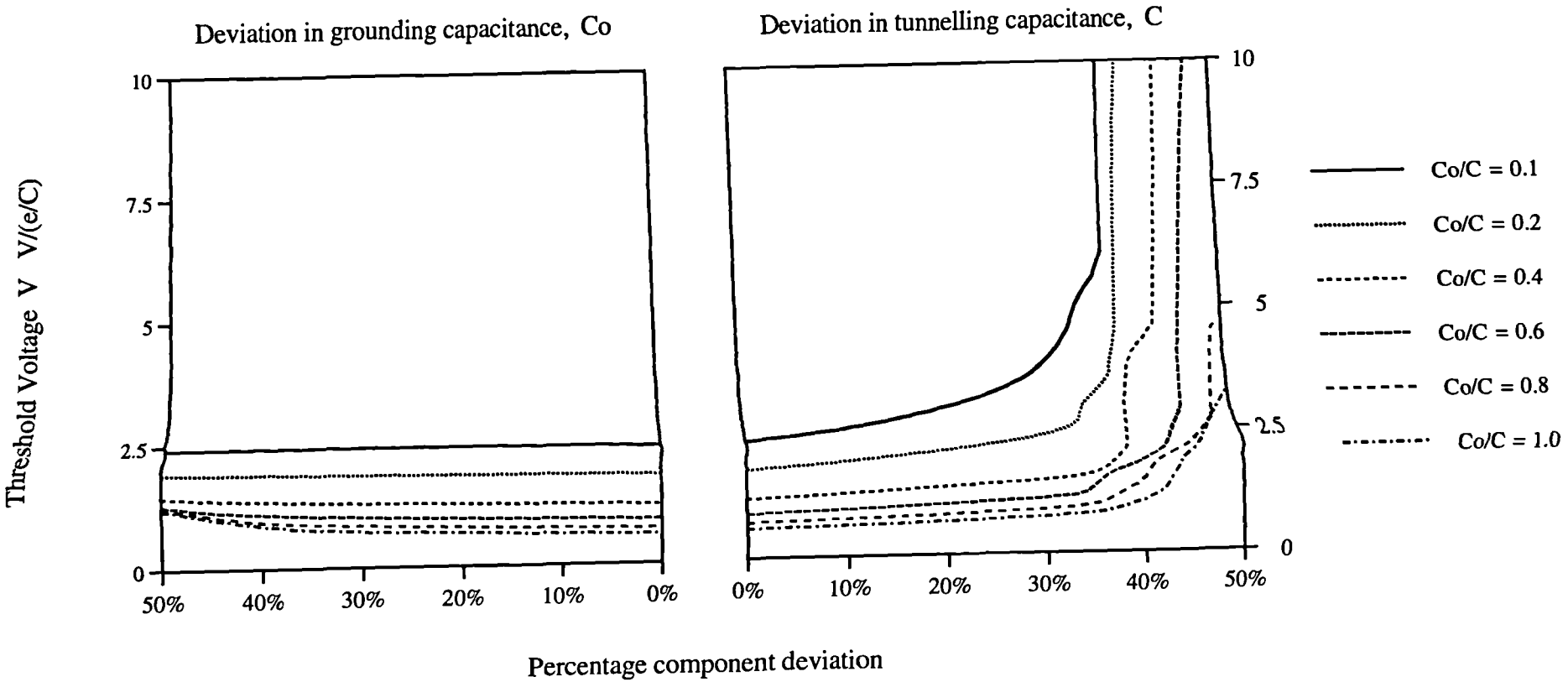


Fig 6.7 Graphs of Array Threshold Voltage versus the average Deviation of its capacitances. LHS shows results for deviations of grounding capacitance, RHS shows results for deviation of junction capacitances. 21 Junction array considered.

All results at temperature 30 times lower than $T_{critical} = e^2/2C$

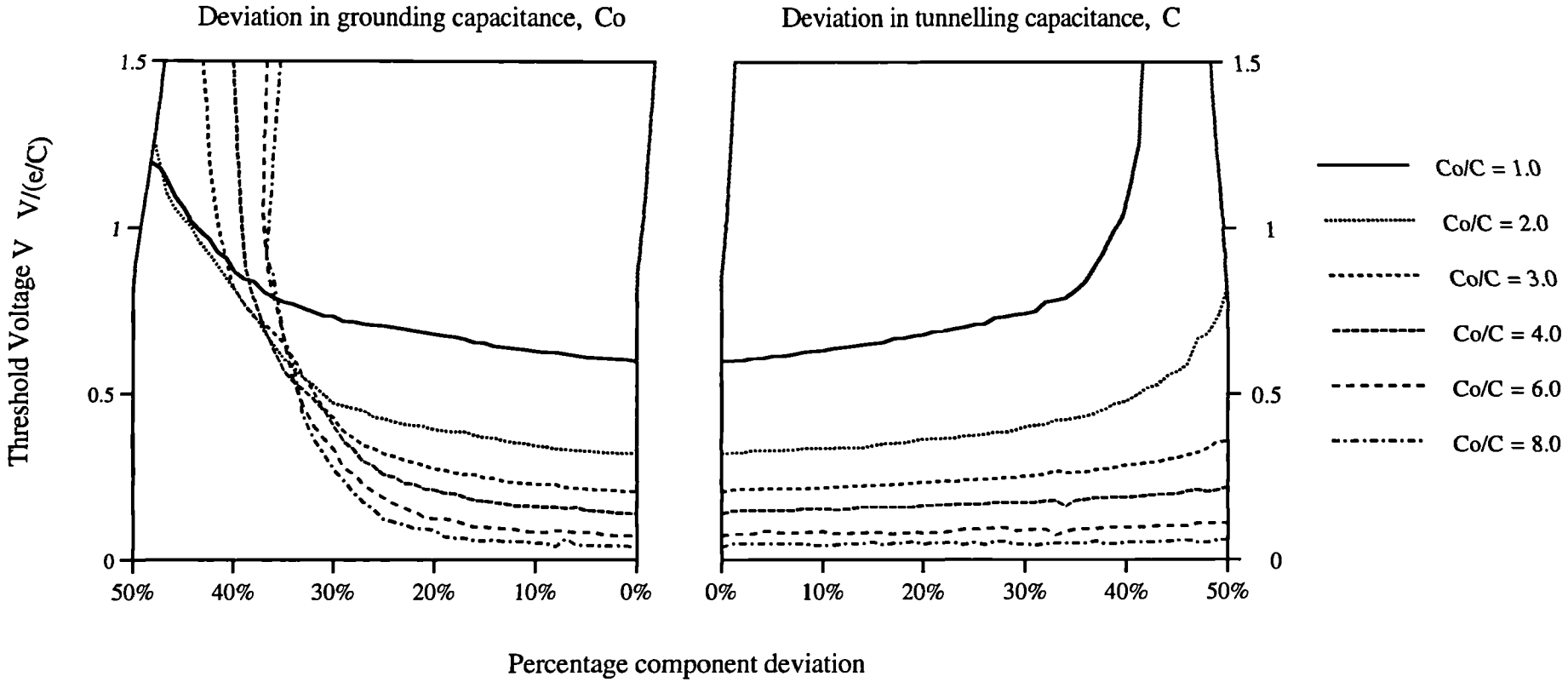


Fig 6.8 Graphs of Array Threshold Voltage versus the average Deviation of its capacitances. LHS shows results for deviations of grounding capacitance, RHS shows results for deviation of junction capacitances. Graphs show situation where Co > C. 21 Junction array considered.

All results at temperature 30 times lower than $T_{critical} = e^2/2C$

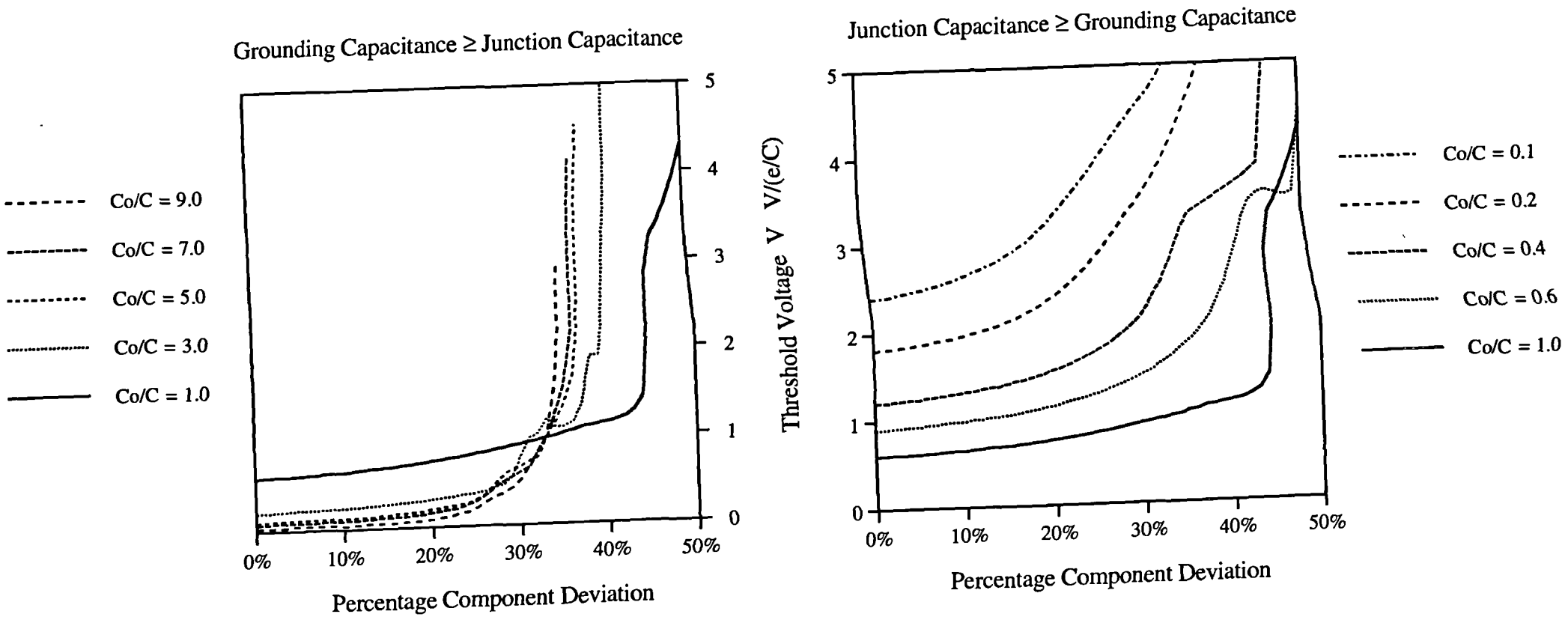


Fig 6.9 Graphs of 21 Junction Array Threshold Voltage versus the average Deviation of its capacitances. Graphs consider variation in both grounding and junction capacitances.

All results at temperature 30 times lower than $T_{critical} = e^2/2C$

and C_0 are varied, or if the variation occurs in the *dominant* capacitor type, the threshold voltage values rise dramatically. This indicates the presence of very small (< an order of magnitude smaller) capacitance values than average in the array, which cause instability and breakdown of the correlated effect both in physical set-ups, and in the modelled IV curves.

- At $C_0 > C$, the threshold curves become noticeably more noisy. At these values, V_{thresh} (proportional to the geometric mean of C,C_0) becomes small, soliton effects in the array become weak, and the knee of the associated IV curves becomes less pronounced. Small changes in the number of electrons moving through the device due to the stochastic nature of the Monte Carlo modelling therefore have a more noticeable effect on the position of V_{thresh}.

Other results not noted in these graphs include ;

- Further lowering of the temperature has little effect on the V_{thresh} curves. Any effects occurring at higher temperatures are swamped by the breakdown of correlation caused by that temperature rise itself.
- Correlation of capacitance values seems to have little effect on the point at which deviation instability occurs. Initially the effect of alternating high and low C values was investigated, as might occur if misalignment occurred during device fabrication. This failed to produce noticeable results - as did many other methods of inducing component value correlation on the system, involving C's, C_0's, or combinations of the two.
- Perturbing otherwise stable arrays by lowering or raising one particular capacitance value in the array had little effect. This was the case whether that capacitance was in the centre or at the edges of the array, or whether it was a grounding or junction capacitance. To have a noticeable effect, the capacitor value had to be raised or lowered by an order of magnitude.
- The same stability conditions were found both in the 21 junction arrays considered in figures 6.7 - 6.9, and in arrays with as few as 7 junctions. The nature of the modelling program precluded smaller arrays from being tested.

Extensions of the Work :

There are a number of obvious extensions that could be made to the work on tunnelling junction arrays.

Firstly, it would be interesting to consider the full capacitance matrix of such a system. The present model includes only tunnelling and grounding capacitance. Certainly the effect of non-tunnelling stray capacitance between next nearest neighbour junctions should be considered. However, this could only be accomplished after

accurate geometrical modelling of proposed experimental devices. Initial work in this area by Asen Asenov is noted in §2.1.1.

Secondly, modelling of additional common experimental techniques might be performed. The measurement of array frequency response under a.c. bias is an experimental technique applied [49][121, Chapter 2], and theoretically considered [122, 123]. Some modelling work computing array spectra is under way. However present algorithms are computationally exorbitant, and prone to round off errors.

Finally, the effect of stray charge in the vicinity of single electronic systems is thought to be critical to their operation [81]. Such charge will be gated by strays to array electrodes to give,

$$-C\phi_{i-1} + (2C+C_o)\phi_i - C\phi_{i+1} = Q_i \qquad (6.5)$$

where Q_i may now take on *fractional* values. The effect of such fractional charge sets should be qualitatively similar to that of component variation. There are two important differences between the two, however. Firstly, the Q_i are independent of electrode potential. The 'virtual solitons' produced will therefore have differing magnitude and an exponential decay constant of λ rather than 2λ. Secondly, a single external charge gated to a number of junction electrodes will produce a set of Q_i far more correlated in nature than considered in the work on component variations. These differences mean that the detailed and quantitative effects of external charge may be far different from that of component deviation. An analysis of system stability under the influence of static external charge would be important. (Note that non-static external charge is considered in §6.3.1, associated with system cross-talk.)

To summarise, we have extended the treatment of Bakhvalov *et al.* to include component variation in tunnelling junction arrays. This better models real life devices. It was found that such arrays are remarkably resistant to component variation, up to a standard deviation of approximately 30%. This is independent of whether component deviation is random or correlated. We repeat that for the hanging resist fabrication technique, estimates of variation in components of $\times 1.25\, C_{junction}$ have been reported [50]. The system is also resistant to extreme variation of a single component, no noticeable effect being produced until that component is perturbed by over an order of magnitude. Finally, it was noted that the best performance of such systems is obtained with grounding capacitances $C_o << C$. However, even for $C_o >> C$, and with the reduced V_{thresh} that results, array stability remains for component values that vary with deviation less then 30%.

6.2 Gated Turnstile Devices

Results obtained from the study of gated turnstiling devices are recorded and discussed. We are especially interested in the frequency response of such devices, and the area of control parameter space within which they operate. Two particular types of turnstile are considered. The four junction gated turnstile was originally suggested by Esteve and fabricated by Geerligs *et al.* [9, 10]. It is a simple system with the direction of electron flow solely governed by differential bias of the junction array.
A three phase device has been suggested by experimentalists at Glasgow [124] and independently considered by Urbina and others [63, 109].

The equivalent circuit schematic of the modelled three phase device is shown in figure 6.12. Its operation is described in detail in §6.2.2. The flow of electrons is controlled by three gate voltages and as such, the device is expected to have advantages over a single phase system. Three gate signals will give greater control of junction bias conditions, allowing flexibility in optimisation. Thus, better stability and frequency response might be available. However such a system has greater complexity and this may effect its area of operation in control parameter space. Calculation of this area is considered in some detail. As with tunnelling junction arrays the effect of component variation on device stability is also considered for the three phase turnstile.

6.2.1 Simple Turnstile Devices

Figures 6.10 - 6.11 summarise the main results obtained from investigation of a simple four junction turnstile with tunnelling junctions of capacitance C, and tunnelling resistance R_t. In figure 6.10 a gating capacitance of $C_G = C/2$ is assumed, and the turnstile is biased close to the centre of its area of operation in V_A,V_G space (values of $V_A = -V_B = -0.35$ V/(e/C), and $V_G = 0,-2.0$ V/(e/C) were used). Ideal conditions were assumed, ignoring thermal fluctuations and macroscopic quantum tunnelling.

Frequency Response :

Figure 6.10 shows that at low frequencies the device does act as an electron turnstile. However as frequency is raised towards the critical value $f_{crit} = 1/CR_t$, typical tunnelling times become comparable with the period of the driving signal $\tau = 1/f$. Imperfect device operation results. From figure 6.10 it can be seen that a 1% error rate corresponds to $f \approx f_{crit}/5$. This places limits on the speed of proposed logic circuits based on single electron effects, and on the use of such a system as an $\langle i \rangle = ef$ current standard.

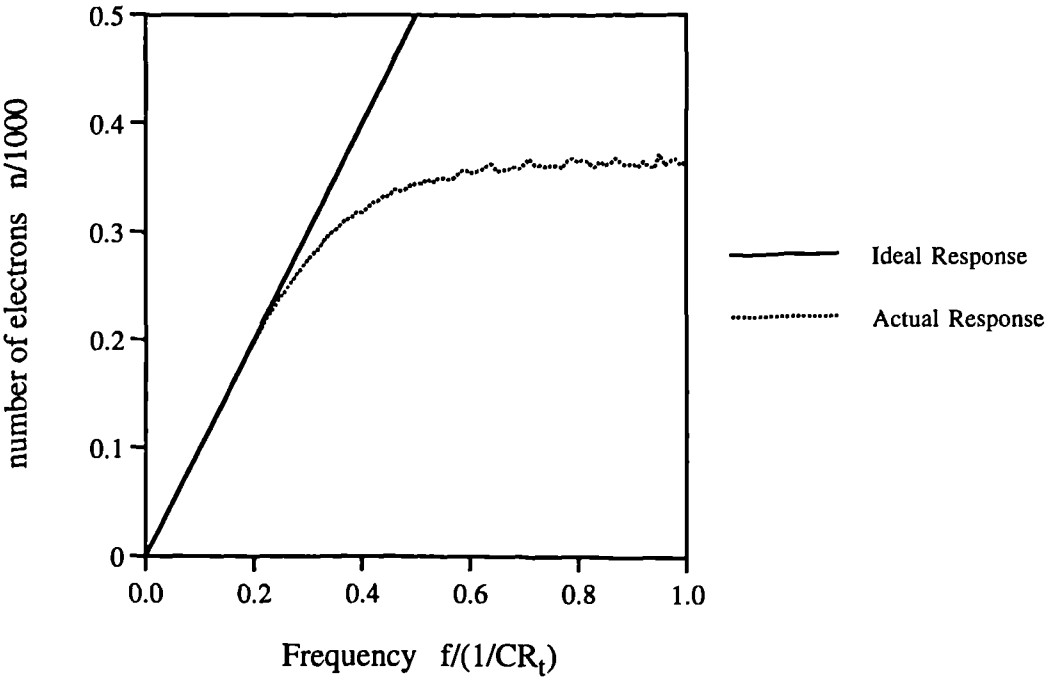


Fig 6.10 Graph of number of clocked electrons versus clocking frequency for a gated turnstile device running over 1000 characteristic time periods CR_t (where the turnstile's junctions have tunnelling resistance R_t and capacitance C)

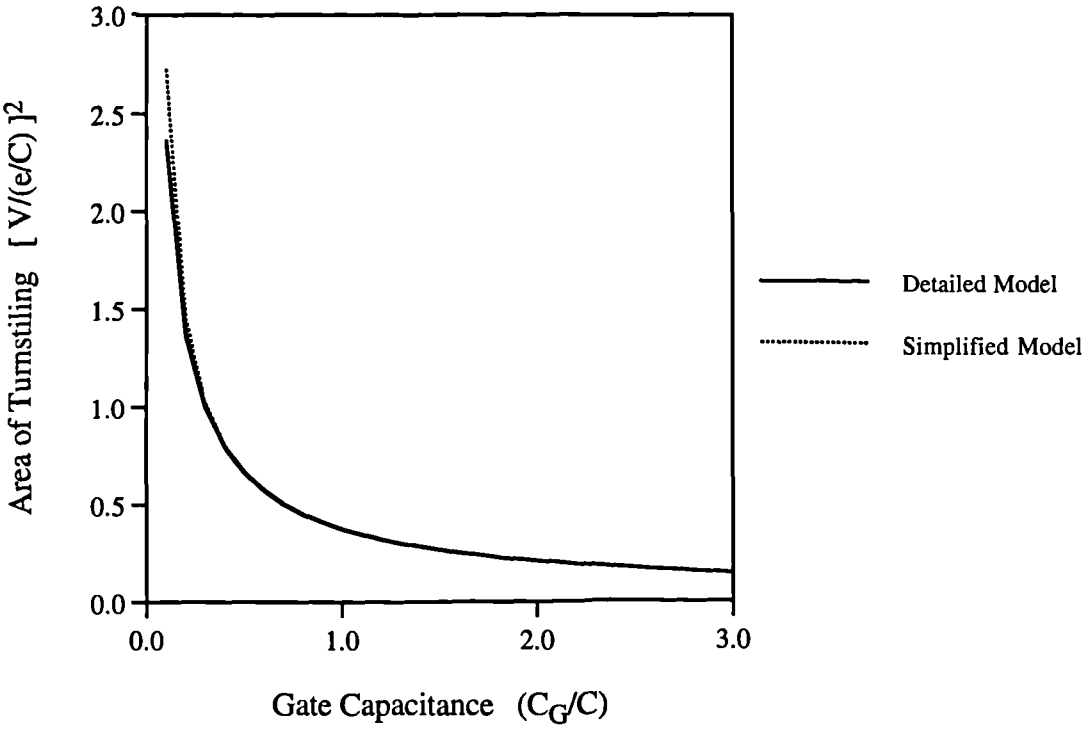


Fig 6.11 Graph of Area of Turnstiling Operation versus Gate Capacitance for a simple gated turnstile.

Area of operation is in control parameter ($V_{gate} \times V_{bias}$) space.
'Detailed Model' calculations are from the Monte Carlo model, while the 'Simplified Model' is based on a linear programming approach.

The modelled data of figure 6.10 is only accurate to 0.1%. However at approximately these levels of accuracy macroscopic quantum tunnelling and other dissipative effects come into play for the double junctions of many real systems [48, 50].

Due to the symmetry of this system, it is also possible to easily derive the $T \rightarrow 0$, non-MQT accuracy of the turnstile analytically. For electron injection there are two possible sets of tunnelling processes. In the first, an electron tunnels from the source, via electrode 1 of figure 5.3, to the central electrode - the obvious route. In the second, tunnelling across C_2 occurs first, producing an 'electron-hole' pair. Then a tunnelling event across C_1 annihilates the hole. Both of these routes are equally likely, and have the same set of tunnelling probabilities Γ_1,Γ_2 for first and second events. For the above bias conditions,

$$\Gamma_1 = 0.35\,\frac{1}{CR_t} \qquad \Gamma_2 = 0.51\,\frac{1}{CR_t} \tag{6.6}$$

(Electron ejection has identical Γ_1,Γ_2.) Using $P(t) = 1 - \exp(-\Gamma t)$ as the probability of the next tunnelling event occurring at time t, the probable total time of electron injection can be calculated. This integrates to give the probability of electron injection occurring before the gate voltage changes,

$$P(t < \frac{\tau}{2}) = \frac{\Gamma_2}{(\Gamma_1-\Gamma_2)}\left[\exp(-\Gamma_1\frac{\tau}{2}) - 1\right] + \frac{\Gamma_1}{(\Gamma_2-\Gamma_1)}\left[\exp(-\Gamma_2\frac{\tau}{2}) - 1\right] \tag{6.7}$$

which gives the error rate for arbitrary driving frequency $f = 1/\tau$. Although not shown graphically, this analytical result agrees with the Monte Carlo simulation result shown in figure 6.10.

Operating Area in Control Parameter Space :

Figure 6.11 shows the legal area of $T \rightarrow 0$ operation of the turnstile in control parameter space (V_A, V_G space). This is shown as a function of the ratio C_G/C. The broken curve is calculated using the linear programming technique, while the solid curve is obtained from a purely Monte Carlo model. Each data point on the Monte Carlo curve required calculation of several hundred points in V_A,V_G space - testing repeatedly for perfect turnstiling action.

As expected, the area of turnstiling is in inverse proportion to the value of gate capacitance. The system is governed by the fractional control charge q_c on the central electrode, produced in the main by the gate voltage V_G acting through C_G. As C_G is reduced, the magnitude of q_c becomes less sensitive to V_G and so

turnstiling will occur over a greater range of V_G values. This is clearly shown in figure 6.11.

Note the difference between the results of the linear programming and Monte Carlo models at low C_G. Although originally thought to be a computational artifact caused by pixellation errors in the Monte Carlo plots, this discrepancy was actually due to oversimplification of the linear programming model. The model assumed that perfect turnstiling was governed only by the events described in figures 5.6-7. However at low C_G it was found that alternate events may become critical, and these make perfect turnstiling is less likely to occur. This is a problem of great importance when dealing with complex systems. Under certain bias conditions a number of different event sets can lead to the same overall system state. This problem will be more clearly appreciated as the three phase turnstiling device is considered.

6.2.2 3-Phase Turnstile Devices

To aid in the analysis of such systems, some simplifying assumptions are made. Only symmetrical devices are dealt with; with the outer junction capacitances C_{outj} identical, outer gate capacitances C_{outs} identical, and so on. The equivalent circuit schematic of such a 3-phase turnstile is shown in figure 6.14. Secondly, we assume unless otherwise noted, that gate voltages swing from $V_L = 0$ to their V_H values. Finally turnstile C_G values are only allowed to vary from $C/10 \rightarrow 10C$. It is assumed that gating capacitances smaller than $C/10$ are physically impracticable, while very large C_G values give negligibly small areas of legal turnstiling.

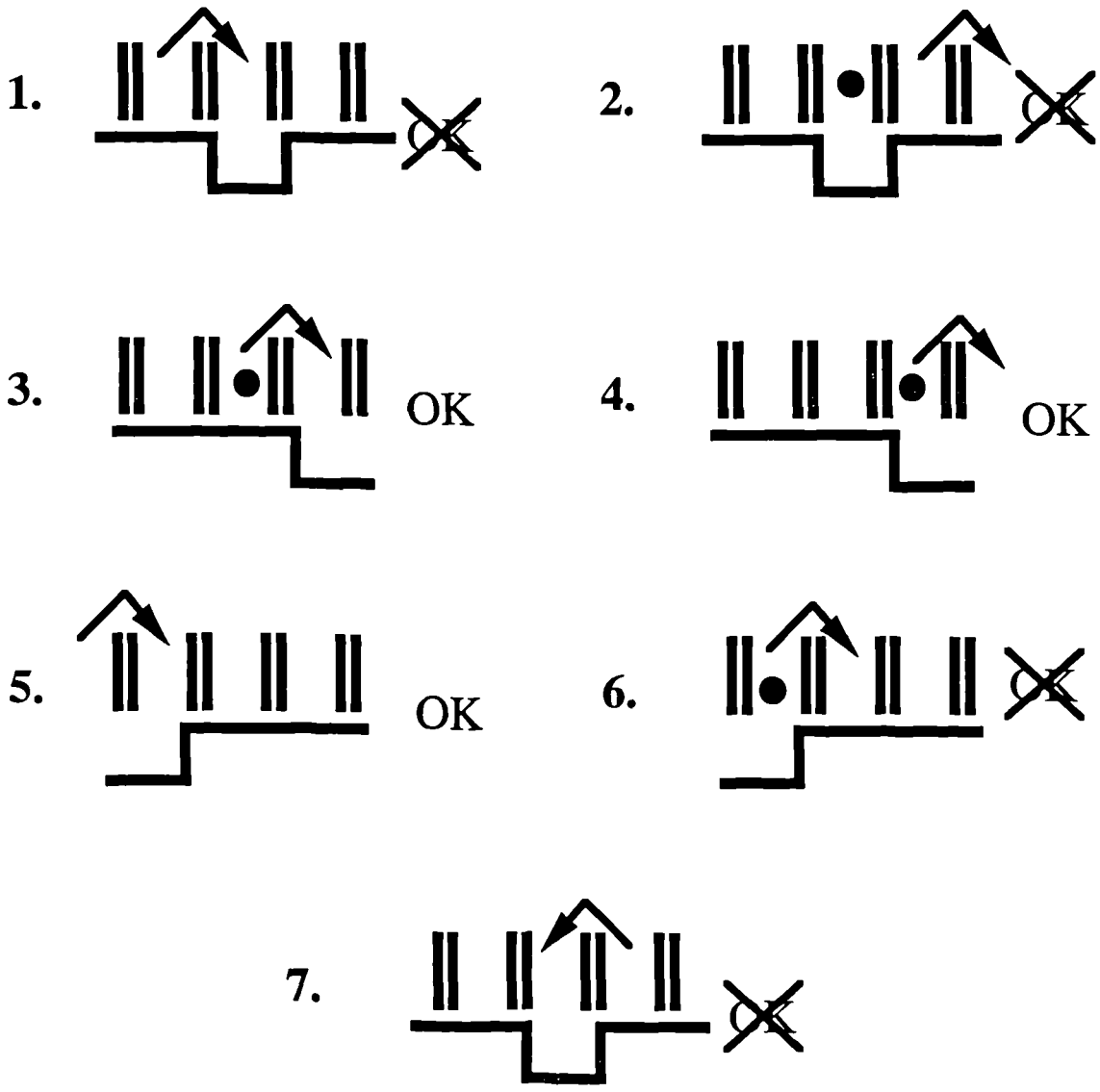
Calculation of Legal Turnstiling Area :

Figures 6.12 show the important tunnelling events that govern the operation of the three phase tunnelling device of figure 6.14. These are the only events that need be considered as long as any component value varies by less than an order of magnitude from nominal capacitance C.

The seven critical allowed and disallowed state transitions were distilled from a large number of possible state transitions by iterative application of the Monte Carlo and linear programming techniques. Initial guesses, based on experience of other systems, were plotted by the linear programming method. Then the Monte Carlo modelling of particular points in parameter space was used to refine these guesses.

Figure 6.13 shows some of the plots produced. A large number of Monte Carlo points are used to show the close correlation between the two methods. In practice, fewer test points are needed to predict which state transitions prove critical to correct device

Fig 6.12 The following schematics describe the **important tunnelling events** which govern the operation of a **three-phase gated turnstile.**
The reference numbers 1...7 correlate with similarly numbered lines on the graph of legal turnstiling area in V_A,V_H space of figure 6.13. Each event corresponds to an associated bounding line of the legal turnstiling area.



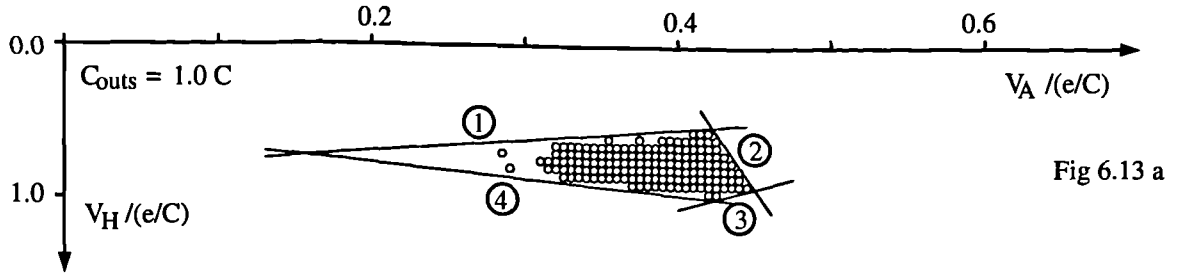


Fig 6.13 a

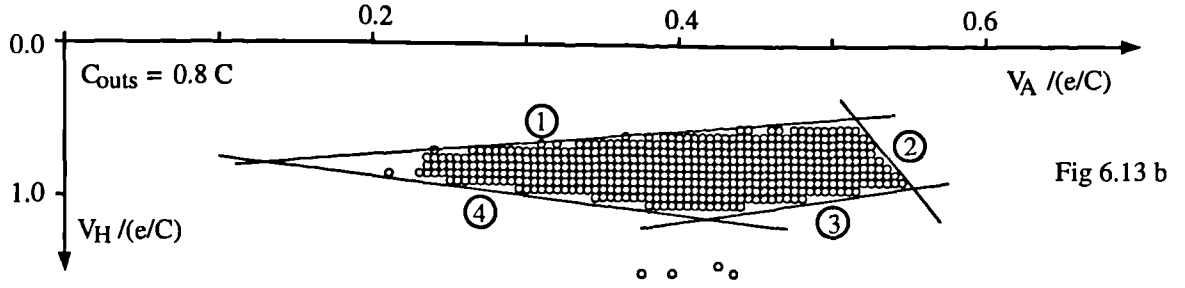


Fig 6.13 b

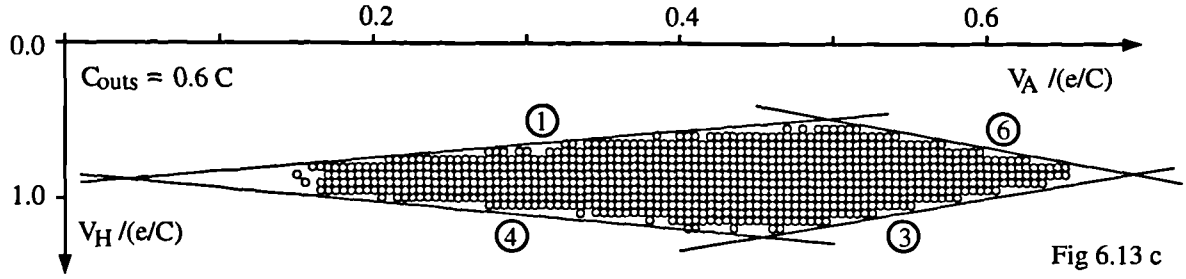


Fig 6.13 c

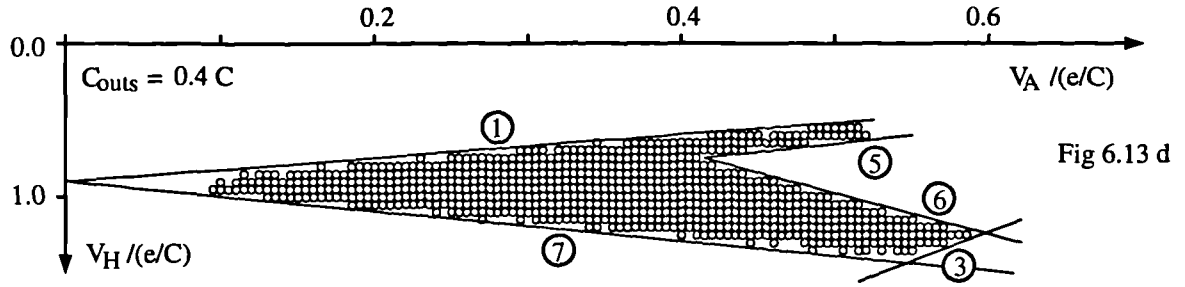


Fig 6.13 d

Fig 6.13 Plots of **legal operating area** in control parameter space for a three-phase **gated turnstile device.** The device modelled is that of figure 6.12.

In all the figures, parameters $C_{outj} = C$, $C_{innj} = C/10$, $C_{inns} = C$ have been used, with C_{outs} varied for each plot.

The 'circles' were produced by successive runs of the Monte Carlo modelling program at differing V_A, V_H, testing in turn whether perfect turnstiling action occurred.
The lines are formed by the linear programming model. Labelling numbers beside each line refer to the critical events of figure 6.12 which define their position.

operation. Linear programming assumes $T \rightarrow 0$, while the Monte Carlo points were calculated at $\beta = T_c/T = 30$. Turnstiling accuracy is determined over 1000 time periods, each some 100 times longer than the characteristic time period CR_t.

The degradation of turnstiling for small (V_A) bias voltages can easily be seen as a discrepancy between the Monte Carlo and linear programming results. At small bias voltages, junctions are operating with applied charge close to their critical charge. This means that thermal fluctuations are more likely to cause errors in operation. Also, tunnelling rates are reduced. Thus correct operation will only occur at low frequencies. In practical circuits a trade off between such errors and the greater self heating of devices operated at higher bias voltages [109] must be made.
At very high (V_A) bias conditions, errors in turnstiling are generally associated with system breakdown. Such bias conditions (aided by thermal fluctuations) raise the Coulomb blockade of junctions allowing electron avalanche and dramatic degradation in system performance.

Degeneracy of State Transition Sets :

This high bias region of Figure 6.13d is of particular interest. Here turnstiling occurs in two distinct regions of V_H. A more detailed look at the way electrons are transported through the turnstile shows that different sets of state transitions can lead to identical final results. The state transition sets are degenerate. For instance if [X X X] represents the number of excess electrons in the three central electrodes of a three phase turnstile, then the following state transitions are all effectively identical. Each represents the transfer of an electronic charge from source V_A to sink V_B.

[0 0 0] → [1 0 0] → [0 1 0] → [0 0 1] → [0 0 0] electron transfer
[0 0 0] → [0 0-1] → [0-1 0] → [-1 0 0] → [0 0 0] hole transfer
[0 0 0] → [0-1 1] → [0-1 0] → [-1 0 0] → [0 0 0] e-h creation
[0 0 0] → [-1 1 0] → [0 1 0] → [0 0 1] → [0 0 0] e-h creation

In the plots of figure 6.13 the major transport process is found to be direct electron transfer. However current is also carried by a minority e-h creation process. In the plot of figure 6.13d, particular component values and high bias produce regions of legal turnstiling where the two types of process are separated. The lower region of the 'V' conducts through electron transfer, the upper through e-h creation.

Note that for device component values $< C/10$ or $> 10C$ other allowed and disallowed state transitions may be found to be critical.

Comparison of Simple and 3-Phase Turnstile :

Figure 6.15 shows the frequency response of a three phase turnstile and compares it to that of a simple four junction device. The curves are taken at $T \rightarrow 0$. Both turnstiles have junction capacitances C and gating capacitances C/2. It is impossible to compare devices with equal junction capacitances and voltage biases, for each acts as a turnstile at differing bias points. Therefore each plot is representative of a class of device; we compare two turnstiles with equivalent component values operating in the *middle of their respective ranges*. Note that the critical time periods are $\tau = 1/2f$, $\Delta T = 1/3f$ for the simple and 3-phase turnstiles respectively. Thus in a given time only 2/3 of the electrons transferred by the two phase device will be transferred by the three phase device - even though both systems have the same number of tunnelling junctions.

Ignoring this handicap of 2/3, the three phase device does have a high frequency advantage because of its ability to bias the tunnelling junctions more effectively. This, however, is only a factor of some 20%. Including the 2/3 handicap puts the three phase turnstile at a disadvantage. The 3-phase turnstile does bias its tunnelling junctions closer to their critical values for its unhandicapped 20% improvement in frequency response, however. Thus it may be of use in applications for which ultra low device self heating is crucial.

Another disadvantage of the 3-phase turnstile is its smaller operating area in control parameter space (compare figure 6.11 with figures 6.16-17). This is a result of its extra complexity. One reason for investigating this system was the possibility of greater control over bias voltages. It was thought that large gate voltages could increase electron tunnelling rates and therefore operating speed. However because of the smaller operating area, the practical effect of large gating voltages is to produce electron avalanche, destroying any turnstiling action.

Area of Operation Under Component Deviation :

Figures 6.16 - 6.17 graph the calculated area of turnstiling action of a 3-phase device for a large range of component capacitance values. Figure 6.16 gives these areas for $V_L = 0.0$ V/(e/C), the low voltage gate bias used in previous turnstiling results. Figure 6.17 gives the same results with $V_L = 0.2$ V/(e/C), at which the largest areas of turnstiling action can be obtained for a given C. Small improvements in turnstiling area can be made by varying this V_L value.

The other main conclusions drawn from these graphs are threefold. Firstly, as with the simple turnstile, large areas of operating area require small gating capacitances.

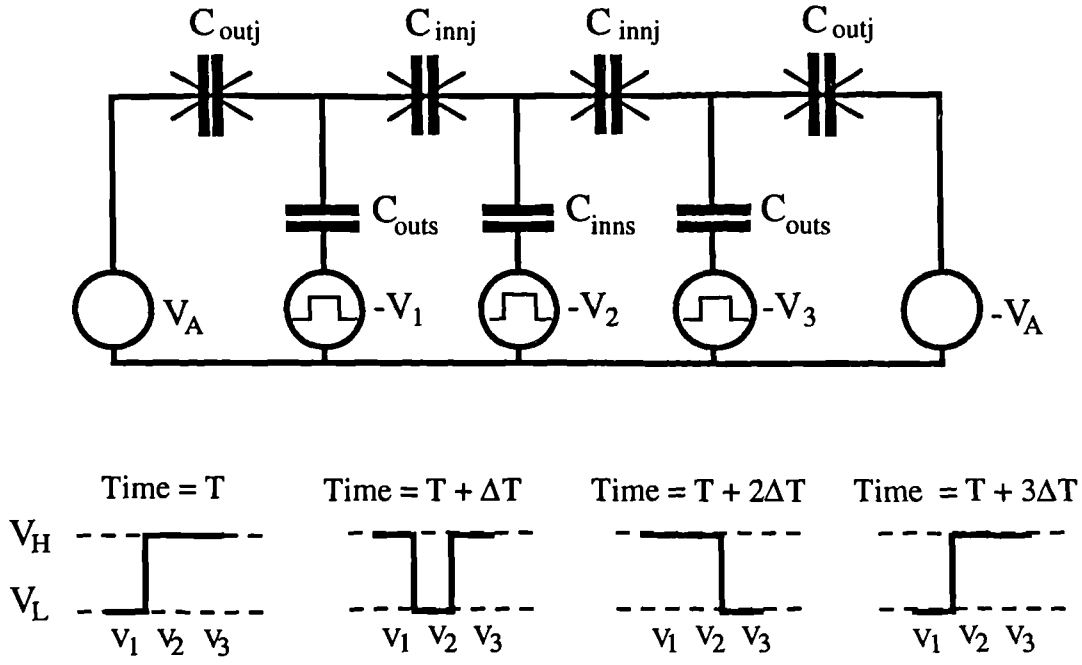


Fig 6.14 Schematic of three phase turnstile device, showing the time dependance and magnitude of gating potentials.

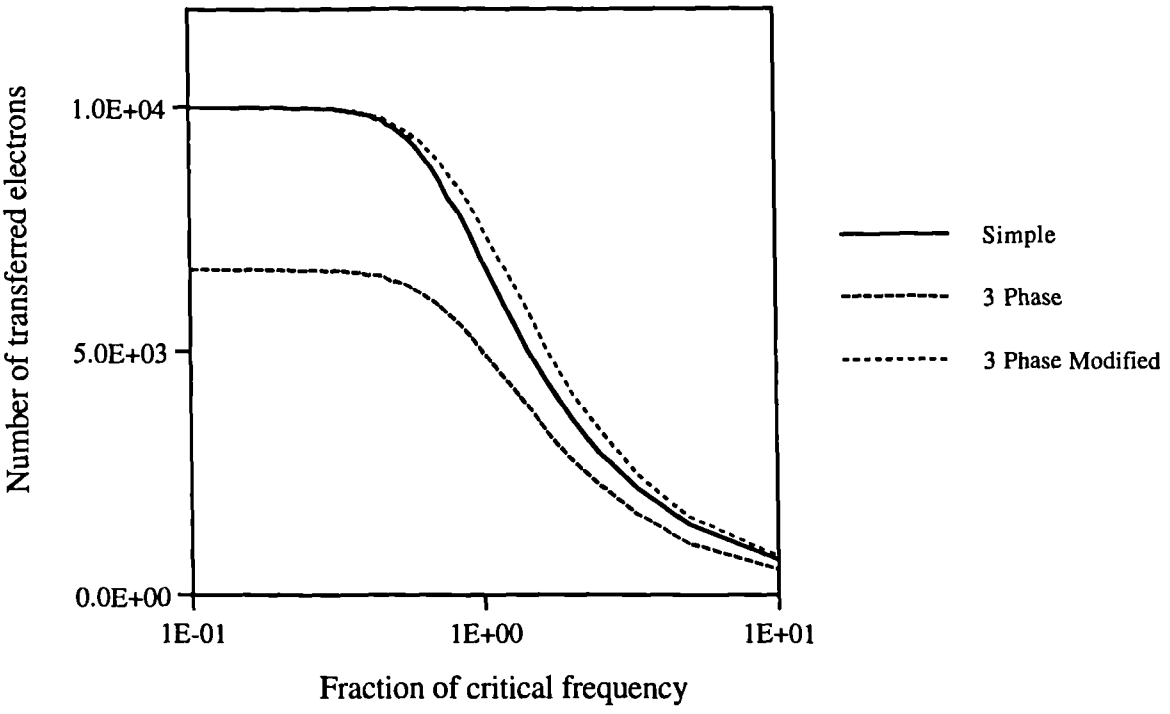


Fig 6.15 Graph of **transferred electrons** through simple and three phase turnstiles versus **fraction of junction critical frequency**.

For these calculations devices have junction capacitances C, gating capacitances C/2.

Bias voltages on the simple device are ±0.2 V/(e/C), with gate cycling between 0.0, -2.0 V/(e/C). Bias voltages on the three phase device are ±0.225 V/(e/C), with gate cycling between 0.0,-1.2 V/(e/C).

'Three Phase Modified' plot is 3/2 times that of the unmodified graph (accounting for differing overall throughput times) to ease comparison.

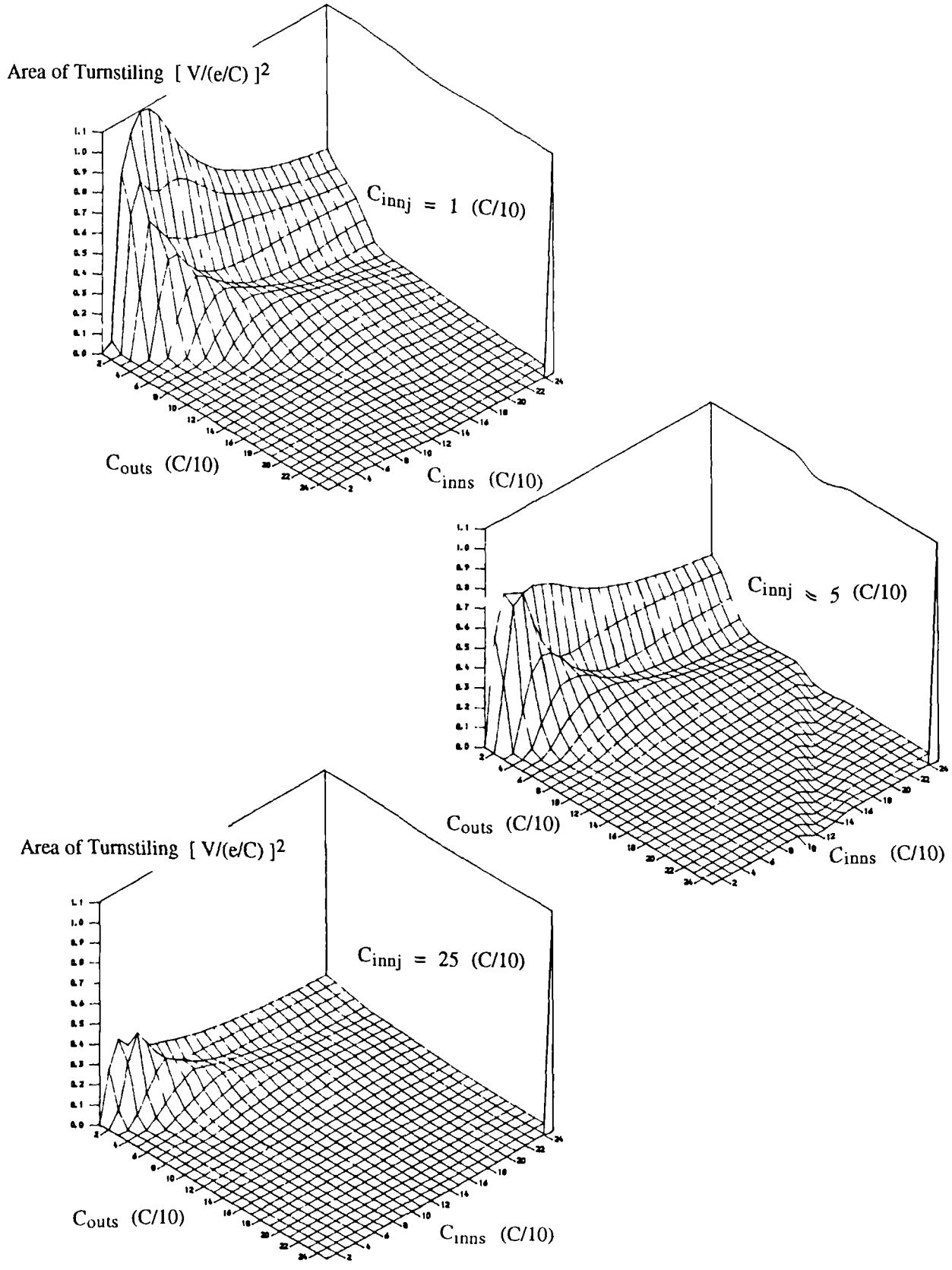


Fig 6.16 Area of **legal turnstiling action** for a **3-phase device** such as that of figure 6.14

In each plot $C_{outj} = C$, C_{outs} & C_{inns} are varied, and $V_L = 0.0$ V/(e/C)

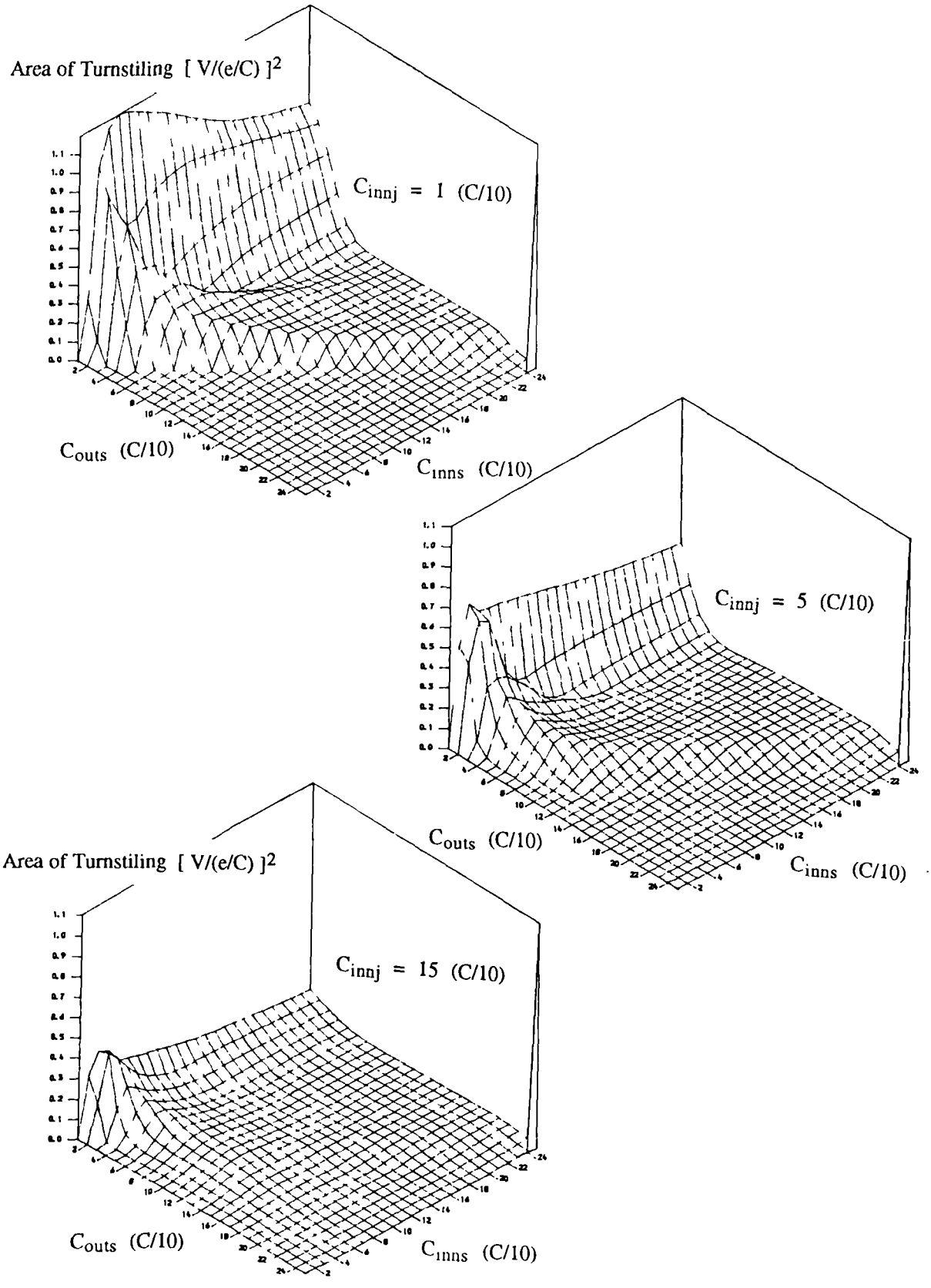


Fig 6.17 Area of **legal turnstiling action** for a **3-phase device** such as that of figure 6.14

In each plot $C_{outj} = C$, C_{outs} & C_{inns} are varied, and $V_L = 0.2$ V/(e/C)

Secondly, unless the condition $C_{outs} > C_{inns}$ is met, no turnstiling will occur. Without this condition, an electron tunnelling from the voltage source into the first electrode will not be able to tunnel further unless the forward bias is so large that system break-down happens. Finally, given $C_{outs} > C_{inns}$, the system is most sensitive to changes in C_{outs}. Variation in outer gating capacitance will effect device performance to a somewhat greater extent than similar changes in inner gating capacitances or junction capacitances themselves. Thus in fabrication, particular attention should be paid to ensuring close control over outer gating capacitances.

Summary :

We have compared the operation of both simple and 3-phase, four junction turnstiles. Although initially it was thought that the 3-phase device would be preferable, our models show this not to be the case. Under typical operating conditions the 3-phase device does not exhibit a frequency response advantage. Also, in real multi-junction systems deviation in component values due to fabrication errors is unavoidable. Such component deviation will perturb the area of turnstiling. Therefore a large nominal area of operation for any device is important in the construction of multi-device systems - to allow a tolerance to component deviation. For given component values, the simple four junction turnstile allows the largest area of stable operation.

Some preliminary work on the effect of component variation on a 3-phase turnstile has been completed, considering a symmetrical system. Investigations are underway into general component deviations in a simple turnstile, as was done for tunnelling junction arrays in §6.1.2. Both systems with two buffer junctions to source (i.e the device above) and multiple junctions buffering to source require study. As noted above, such multiple junction buffers should act as a barrier to macroscopic quantum tunnelling effects.

6.3 Coupled Junction Arrays

6.3.1 Reasons For Studying Coupled Systems

As noted above, a critical concern in the design of more complex single electronic systems is their sensitivity to external charge. This sensitivity is the reason such systems are suggested as accurate electrometers [8, 11]. The effect of static external charge was discussed in §6.1.2. The similarity between such effects and those of component variation in a tunnelling junction array were noted. The work of §6.1.2 suggests that arrays of junctions may have characteristic structural immunity to static charge.

The effect of non-static charge (e.g trapping/detrapping of electrons in semiconductor systems) is liable to be much more serious as a 'killer effect' in single electronic systems. The important turnstiling action discussed in §6.2 relies on a gate voltage varying the fractional charge on one or more electrodes of a tunnelling junction array. This is similar to the modification of electrode charge that would occur as the result of a trapping/detrapping electron coupled to it by system strays. The success of gated turnstile devices as controllers of electron flow underlines the problem of external non-static charge. Such problems can only be eliminated by careful system shielding and fabrication technologies which reduce to a minimum the presence of charge traps. Another final source of non-static charge - impossible to counteract externally - is the effect of charge flow in one part of an extended system coupled to other parts by stray capacitance. Cross-talk is a serious potential obstacle for the development of practical capacitive circuits, and merits considerable study. Results on the sensitivity of systems to cross-talk immediately define maximum device densities for practical fabrication approaches, and give indications of whether further isolation than simple device distance is needed. Such isolation may be difficult to construct for ultra small devices, and its need should be avoided if possible.

As a start to the study of cross-talk in single electronic systems, two types of capacitively linked device are considered. Firstly, coupled tunnelling junction arrays are modelled. Then simple coupling of four junction turnstiles is studied.

6.3.2 Coupled Tunnelling Junction Arrays

Model Under Study :

In studying coupled junction arrays, a specific system is modelled - a set of parallel 6-junction arrays fabricated using a Schottky dot on silicon, lateral metal-semiconductor-metal approach [60]. Although the fabricated device has six parallel arrays, only the results for two arrays linked by capacitive strays are presented. No new results are seen on scaling up the model. As the original purpose behind this area of work was to provide predictions of device operation for the experimental group fabricating this device, we concentrate on its IV characteristics.
A schematic of the modelled system is shown in figure 6.18, and consists of two, 6-junction tunnelling arrays and the addition of 'nearest electrode' coupling strays. This gives a first order approximation to the full capacitance matrix of such a system. Estimations of junction capacitances and grounding strays were made using the best approximation available at the time - the 2D simulation originally designed for use on MESFETs and HEMTs [82]. These results are discussed in Chapter 3 and give $C \approx 3.2$ aF and $C_{ground} \approx 6.0$ aF. This gives a critical temperature of device operation of $T_c \approx 290$ K. The results of applying modelling tools to this system are shown in figures 6.19 - 6.21.

Results of Temperature Variation - Minimal Cross-talk :

An initial result of use to the experimentalists working on this device was the prediction of IV characteristics as a function of temperature. These show whether a critical temperature of 290 K would allow useful experimental measurements at liquid nitrogen temperatures. Figure 6.19 shows the predicted IV curve for the system with small stray capacitance (i.e minimal cross-talk) at approximately liquid nitrogen, liquid helium and ultra low temperatures. From array theory above, a threshold voltage of $V_{thresh} \approx 0.19$ V/(e/C) and soliton length of $\lambda^{-1} = 0.78$ junctions are calculated. With such short soliton length the arrays are not expected to perfectly follow a theory built around the concept of extended solitons.
It can immediately be seen that at temperatures around that of liquid helium and below, the system exhibits clear Coulomb blockade characteristics. However thermal fluctuations at 77K effectively destroy the blockade. The modelled threshold voltage agrees well with the theory presented above. Experimentally therefore, temperatures of approximately 4 K should be adequate to investigate the linked array system.

Effects of Finite Cross-talk :

Figures 6.20 and 6.21 show the asymptotic and blockade region views of the linked arrays at low (i.e below 4 K) temperatures, but with a variation of stray coupling

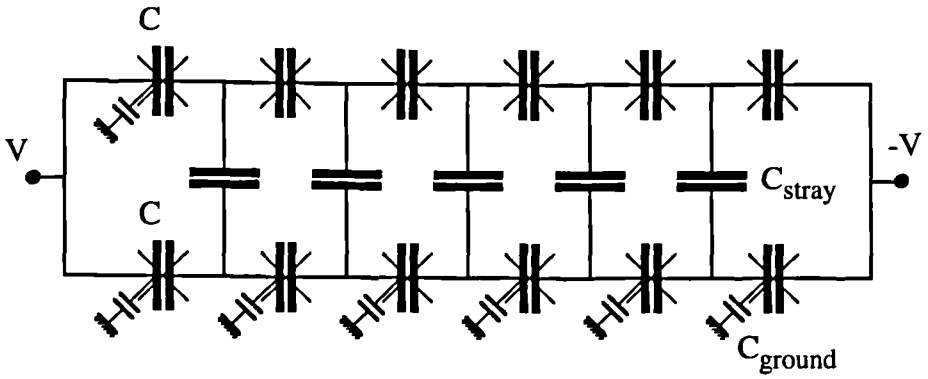


Fig 6.18 Schematic of two tunnelling junction arrays, linked by stray capacitance, and including stray or gating capacitance to ground.

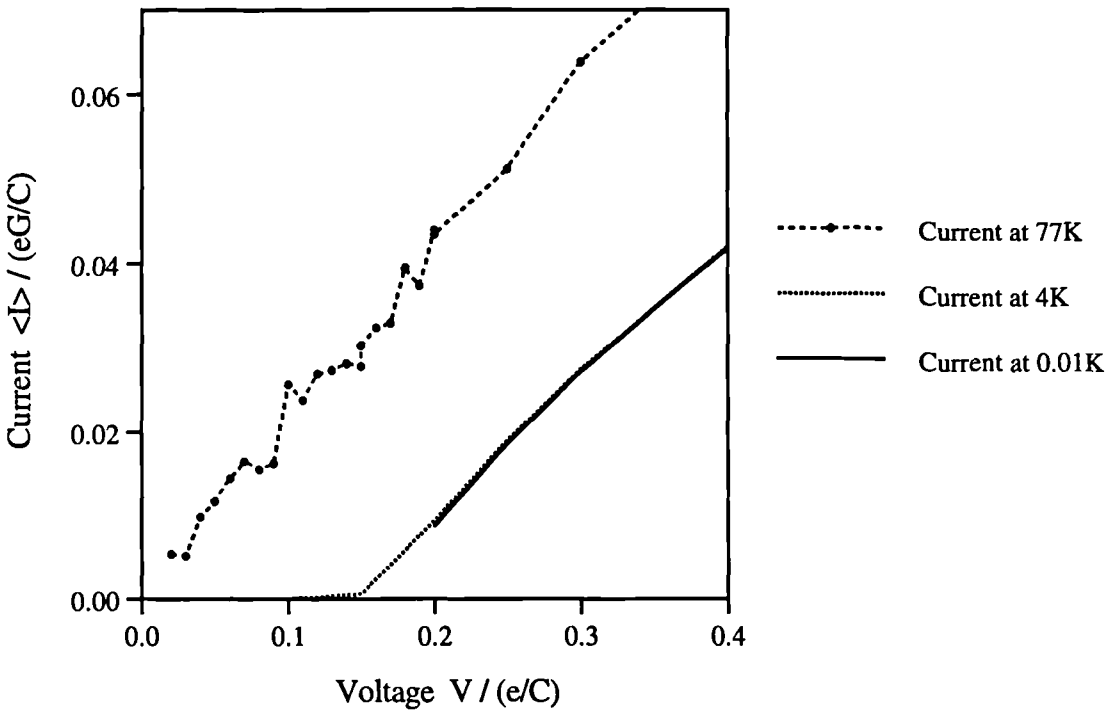


Fig 6.19 IV Curves for two linked arrays of six junctions showing temperature variation. Device has grounding capacitances 2C, and strays linking the arrays of 10^{-4} C. Junction capacitance C is estimated by geometrical modelling (see §3.3.1) and corresponds to a critical temperature of 290K.

Curves are calculated over 3×10^4 events, approximately 2500 electrons transferred.

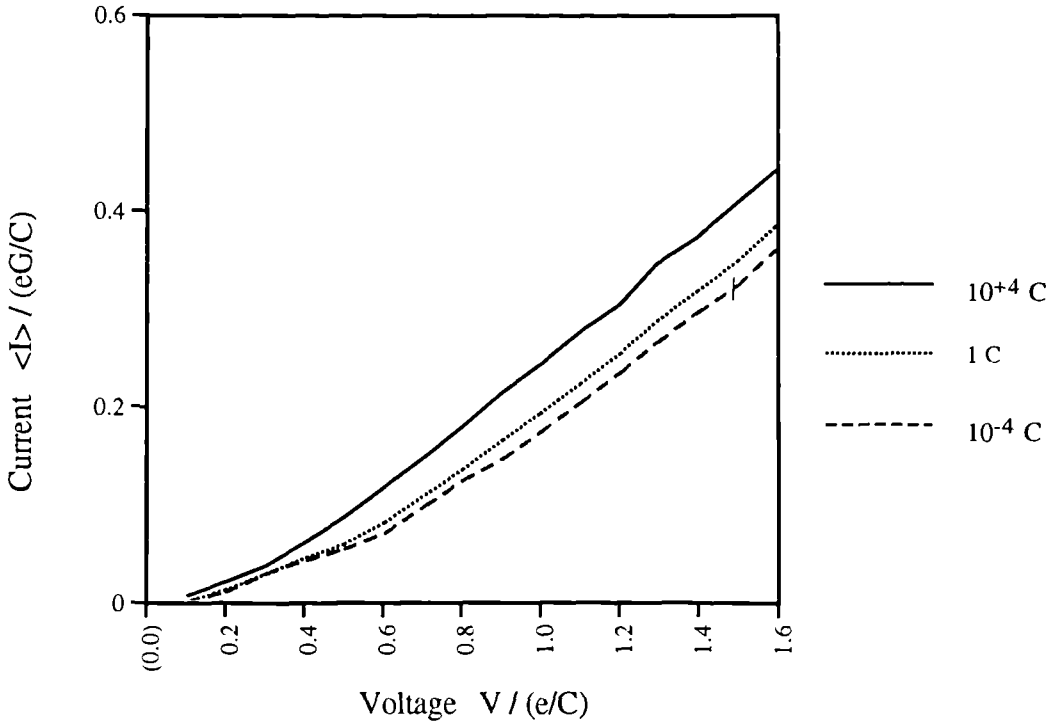


Fig 6.20 IV Curves for two linked arrays of six junctions - showing dependance on linking strays. Asymptotic View.

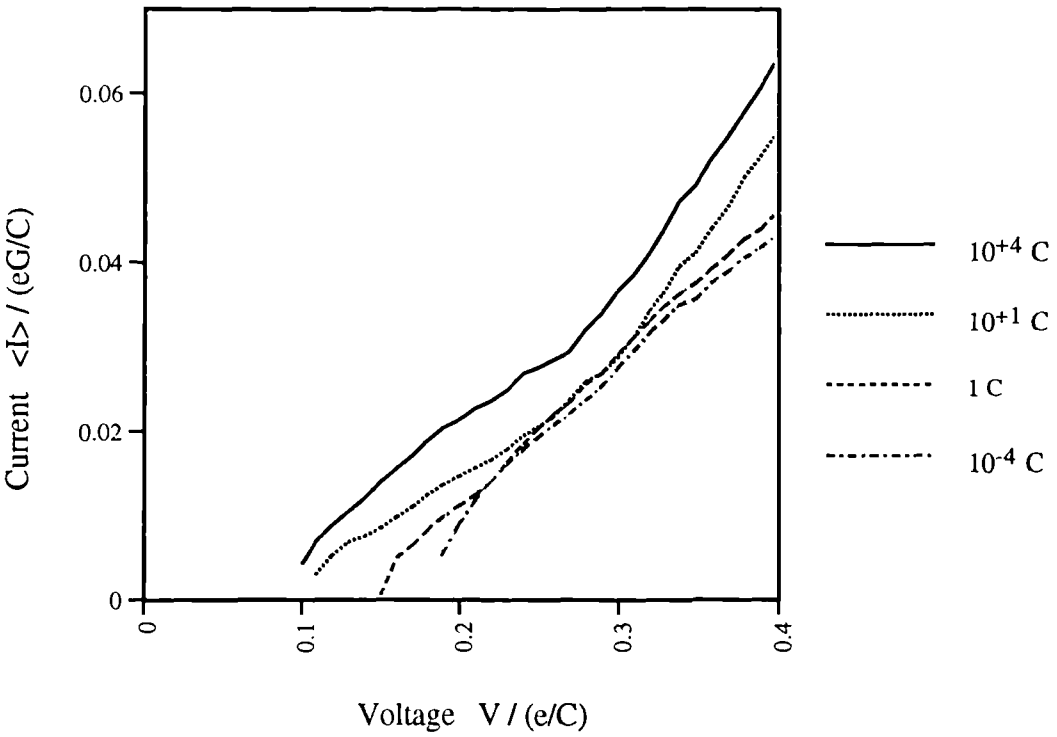


Fig 6.21 IV Curves for two linked arrays of six junctions - showing dependance on linking strays. Detail of Coulomb Blockade region.

Device has grounding capacitances 2C, and junction capacitances C (estimated by geometrical modelling and corresponding to a critical temperature of 290K).

Temperature $T \rightarrow 0$

Curves are calculated from 2×10^4 events, approximately 1700 electrons transferred.

capacitance. Strays from 10^{-4} C (which should give minimal cross-talk and independent array action) to 10^{+4} C were considered.

First, and most obviously, large array coupling capacitance does have a marked effect on IV characteristics - both asymptotically and in the blockade region. Asymptotically the blockade offset voltage is reduced from approximately 0.5 V/(e/C) with minimal strays, to approximately 0.25 V/(e/C) at $C_{stray} = 10^{+4}$ C. At such high coupling capacitances, the two arrays are highly correlated, and to all intents act as one. In the blockade region, V_{thresh} is also reduced by the effect of large coupling strays, from approximately 0.15 V/(e/C) to 0.10 V/(e/C).
The second important result from these graphs is the magnitude of C_{stray} required to produce such effects. Over the range $10^{-4} < C_{stray} < 10^{0}$ there is only a small variation in offset voltage, and very little change in threshold voltage. The larger changes in device operation occur only when $C_{stray} > C_{junction}$. This result is borne out by similarly collected data for other C_{stray}/C values. In practice, this means that if stray capacitances can be kept smaller than junction capacitances, the strays should have little effect on average current flow in a tunnelling junction array. In particular, they should have minimal effect on the threshold voltage of the array.

The detailed, discrete nature of current flow in these coupled arrays makes analysis difficult. This was the main reason for choosing to model their operation. However at high voltage and average current flows it is possible to make simplifying assumptions that allow some direct analysis - particularly of the asymptotic offset voltage, V_{off}. For a single junction array, with $C_o \rightarrow 0$, the offset voltage can be obtained by comparing junction critical charges with the average charge across each junction. For an N junction array,

$$C_{eff} = \frac{C}{N\text{-}1} \Rightarrow Q_c = \frac{e}{2}\left(\frac{N\text{-}1}{N}\right) \quad \text{and} \quad Q_{ave} = \frac{CV}{N} \tag{6.8}$$

Setting $Q_c = Q_{ave}$ gives, $$V_{off} = \frac{e}{2C}(N\text{-}1) \tag{6.9}$$

For a single junction array with finite C_o, a similar process can be followed. The effective capacitances (and therefore critical charges) of junctions will however vary throughout the array. If the effective capacitance of a C/C_o 'ladder' of n rungs is known to be f_n then these can easily be obtained (see Appendix F, Effective Capacitance of Ladder Circuits). The maximum and minimum effective impedances of an N junction array will then be,

$$f_{N-1} \quad \text{and} \quad \begin{cases} \dfrac{f_{(N-1)/2}}{2} & N \text{ odd} \\ f_{N/2} \,||\, f_{(N-2)/2} & N \text{ even} \end{cases} \tag{6.10}$$

An average of these allows a good estimate of V_{off} which applies for all N, λ. This is in contrast to the limited (and incorrect) estimation formula stated in [11]. Results for the asymptotic response of linked arrays can be obtained similarly. Appendix F gives formulae for linked N junction arrays where $C_o \rightarrow 0$. However for more complex systems it was found simplest to use the Thévenin calculation routines of the General Network Solver. Figure 6.22 graphs critical charges for junctions of the above modelled array, where N = 6, $C_o/C = 2$. From this graph the limiting offset voltages of the system are calculated at $V_{min} = 0.26$ V/(e/C) and $V_{max} = 0.52$ V/(e/C), in agreement with the modelled results.

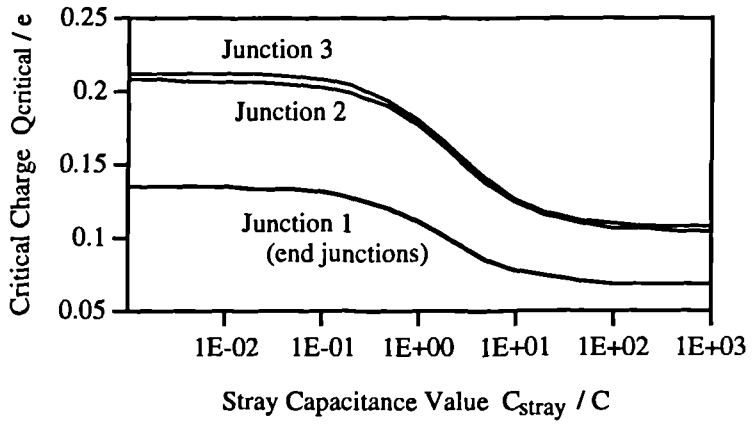


Fig 6.22 Graph of junction critical charge versus stray linking capacitance for a pair of six junction arrays with $C_o/C = 2$. Symmetry means that only three junctions need be considered when calculating such charges.

These results of course only apply to the IV characteristics of tunnelling junction arrays. Such systems operate without the need for accurate control of single electrons, dealing only with average electron flow. However these results do imply that junction arrays *are* remarkably resistant to the effects of capacitive strays, as well as those of component variation.

6.4 Coupled Gated Turnstiles

Attention is now turned to devices which *do* require the accurate control of single electrons, and may therefore be less resistant to coupling strays. We consider turnstiling devices, and in particular the four junction gated turnstile of §6.3. The results of §6.3 imply that such a turnstile will be an important component of practical single electronic systems. The conditions of coupling under which ideal turnstiling is allowed are considered. The accuracy of such coupled systems in transferring more realistic streams of electrons is also considered. The accurate transmission of such bitstreams is vital if real data processing is to be achieved.

6.4.1 Coupled Four-Junction Turnstiles

Modelled System :

A schematic of the system investigated is shown in figure 6.23. It consists of two four-junction turnstiles linked by a simple set of 'nearest electrode' stray capacitances. (Note that in figure 6.23 both top and bottom stray capacitances are superfluous due to the ground line.) To aid comparison, the turnstiles themselves use the same components as those of §6.3. These have constant junction capacitance C, and gate capacitance C/2. The choice of gate capacitance is a trade off between operating area in control parameter space and the difficulties of practical fabrication. Each turnstile of the system is biased by the same V_A and range of V_G. By changing the sign of the bias potentials on the second turnstile it is possible to consider electron flow both parallel and anti-parallel to flow in the first turnstile.

Figure 6.25 shows initial results of modelling the system of figure 6.23. The frequency response of each turnstile is calculated over 10^4 periods of V_G. Both turnstiles are biased at $V_A = 0.2$ V/(e/C), $V_G = 0.0,-2.0$ V/(e/C). This is well within the legal area of turnstiling operation for an uncoupled turnstile. Superimposed on these traces is the response of such an uncoupled turnstile, which indeed shows ideal response at low frequency. Large coupling capacitances of 10^4 C are used for the plotted results. Results were also obtained for smaller values of C_S, and these tend to the uncoupled response as C_S is reduced.

Two general conclusions can be drawn from these results. Firstly, as expected, the inclusion of strays modifies the legal operating area of each turnstile. In this case, the area is modified so much that our experimental bias points now fall outside, and imperfect turnstiling occurs. Secondly, the system symmetry is broken. This cannot be explained only by a change in turnstiling area. Such a change effects both turnstiles equally, for both parallel or antiparallel electron flow. Here there is a 5% difference

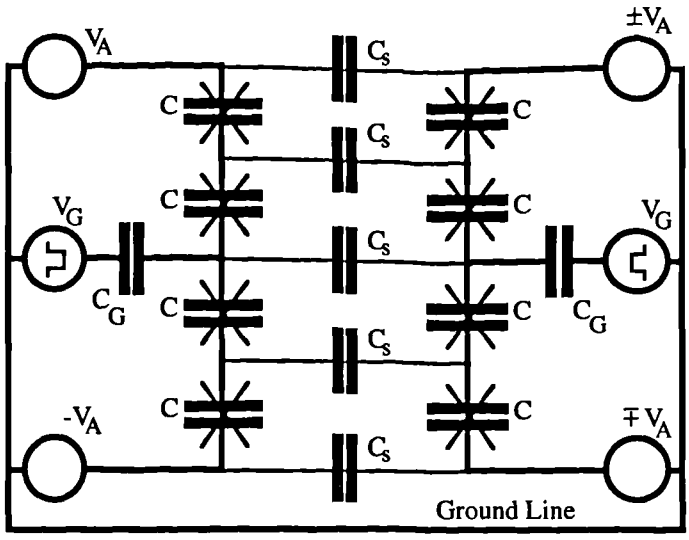


Fig 6.23 Schematic of 2-phase, four junction gated turnstiles linked by stray capacitance and driven by separate bias voltages. Second turnstile can be driven so that electron flow is parallel or anti-parallel to electron flow in the first.

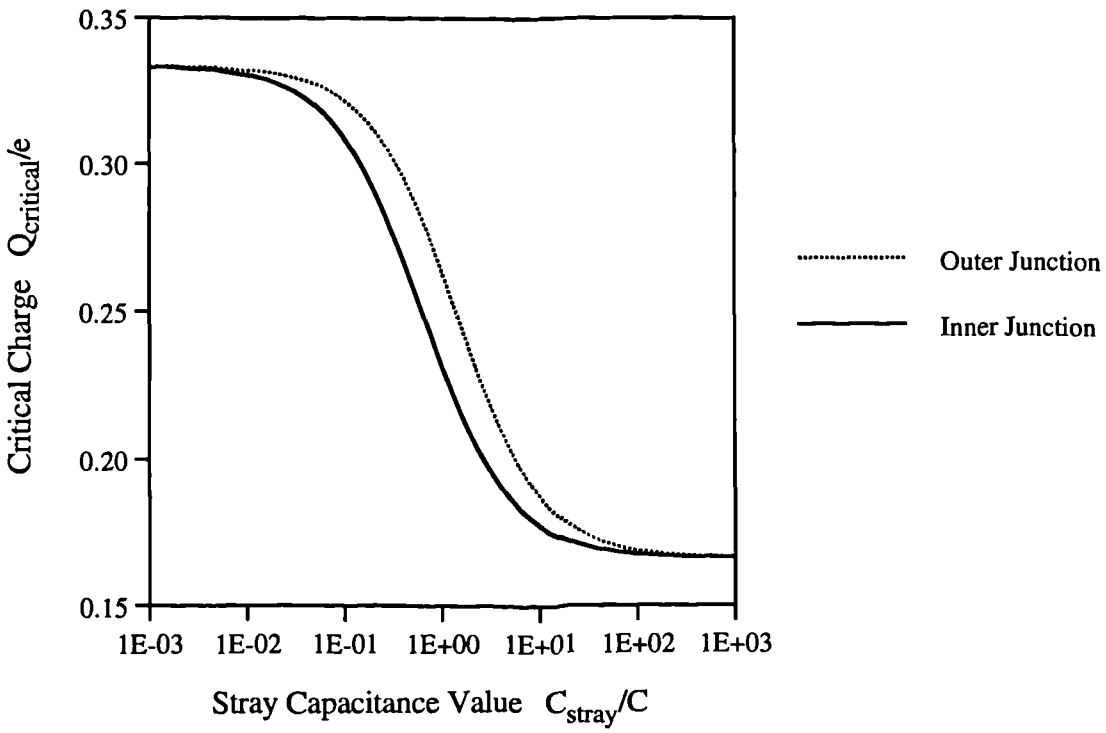


Fig 6.24 Graph of **Critical charge** (the charge magnitude across a junction which allows tunnelling) versus **Stray capacitance**, for two identical four junction gated turnstiles.

Junction capacitances C, gate capacitances C/2.

Operation as $C_{stray} \rightarrow 0$ gives $Q_{critical} = e/3$, identical to a lone turnstile.

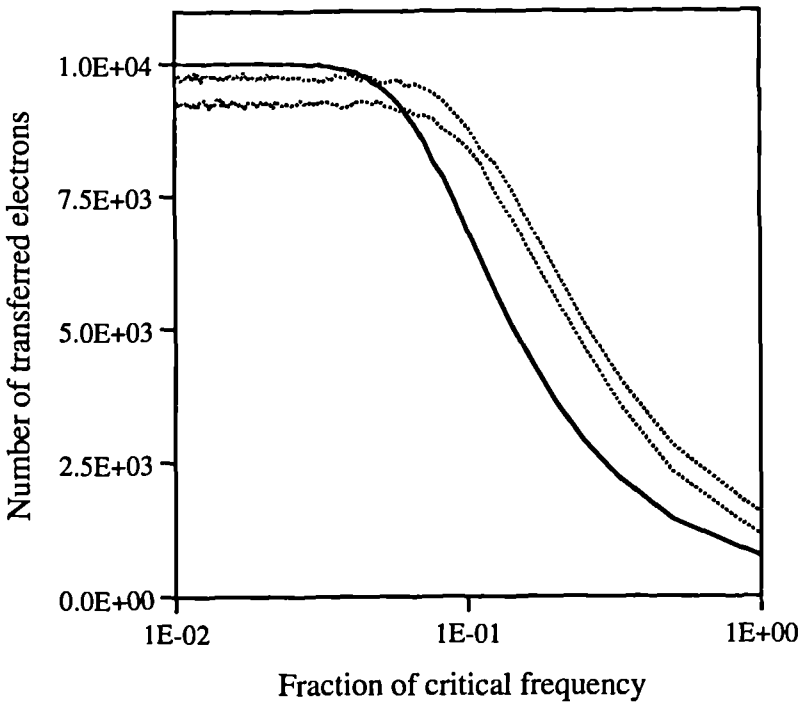


Fig. 6.25 a

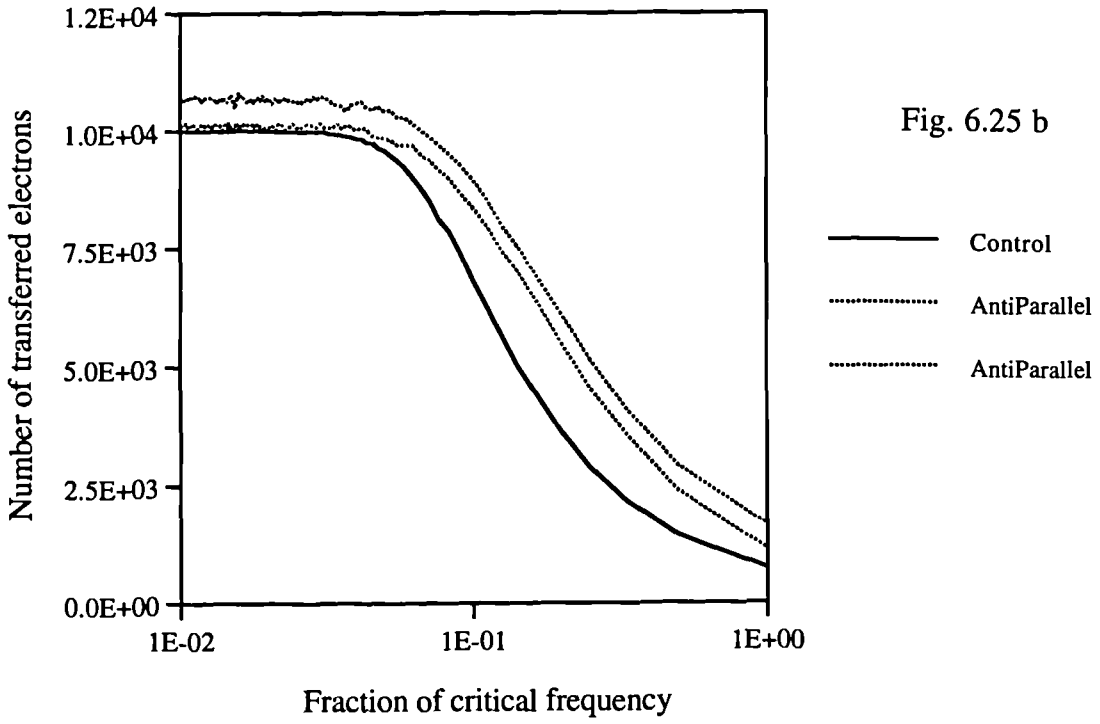


Fig. 6.25 b

Fig 6.25 Graphs of **transferred electrons** through two linked, four junction gated turnstiles **versus fraction of junction critical frequency**. Solid line is result from lone device, dashed lines are the results from devices in proximity. Top graph deals with parallel electron flow, bottom graph with antiparallel flow. Turnstile junction capacitances C, gate capacitances C/2, linking strays 10^4C.

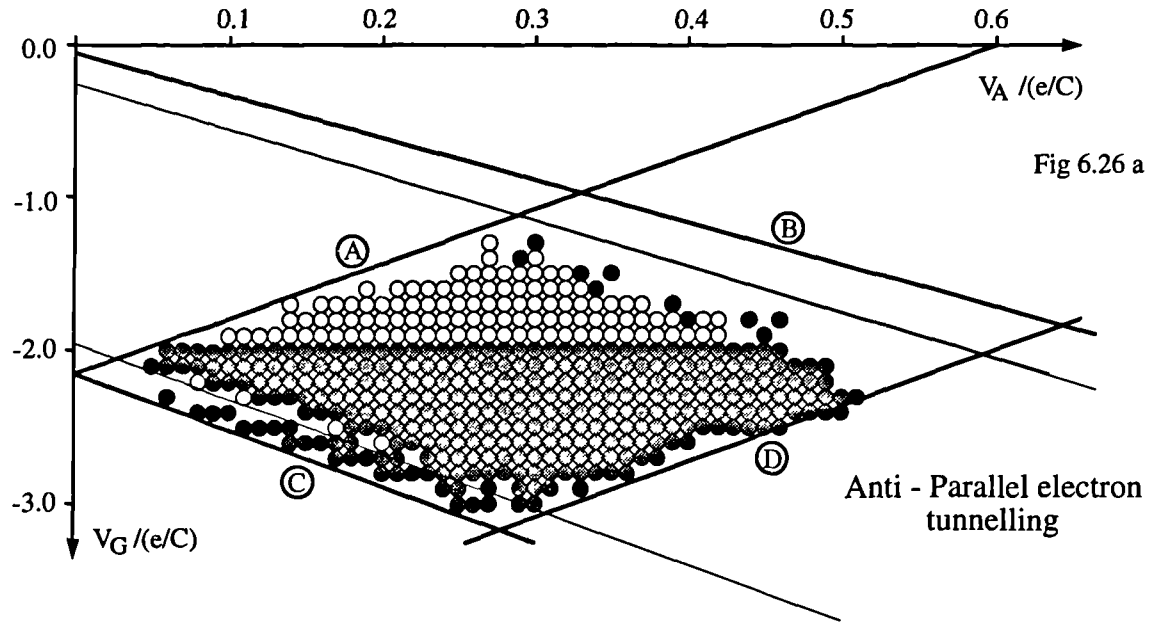


Fig 6.26 a

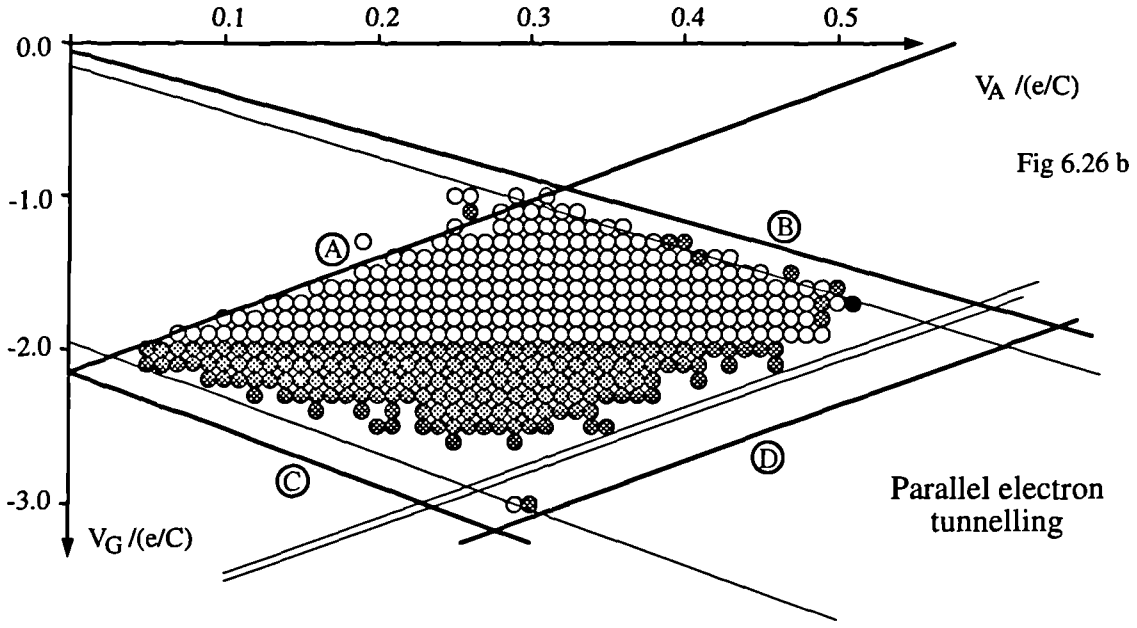


Fig 6.26 b

Fig 6.26 Plots of **legal operating area** in control parameter space for capacitively linked 2-phase **gated turnstile devices.** The devices are those of figure 6.23.

Both figures have junction capacitances C, gating capacitances C/2, and strays linking the two devices of C/10.

The 'circles' were produced by successive runs of the Monte Carlo modelling program at differing V_A, V_G, testing in turn whether perfect turnstiling action occurred. Filled circles represent perfect turnstiling action, open circles represent perfect turnstiling action minus one electron. Only the electrons driven through one of the two devices are recorded.
The heavy lines are formed by the linear programming model. Labelling letters beside each line refer to the defining events of figure 5.6. Hairlines take into account the possibility of single electrons present in the opposing turnstile.

in the flow through two identical devices. Under parallel flow both turnstiles show less than perfect action, while for antiparallel flow the devices are pushed past breakdown.

Analysis of Results :

To further analyse the modification of operating area with respect to system strays, the concept of critical charge is used. As noted above, the charge needed across a junction to cause tunnelling is dependant on both the junction capacitance and the effective impedance of the rest of the circuit. As the external circuit of a junction is varied (by introducing strays) its critical charges will also vary. We expect changes in the action of a system to be proportionate to changes in these critical charges.
For the system of figure 6.23, the change in critical charge can be trivially obtained from circuit parameters; for outer junctions,

$$q_{crit} = \frac{e}{24}\left(\frac{16 + 64s + 75s^2 + 24s^3}{4 + 13s + 12s^2 + 3s^3}\right) \tag{6.11}$$

where s is a parameter defined by $C_S = C/s$. This formula is more enlightening at limiting values of s. For $C_S < 10^{-1}$ C, for instance, it approximates to,

$$q_{crit} \approx \frac{e}{3}\left(1 - \frac{7}{8s}\right) \tag{6.12}$$

Thus at low coupling capacitance the change in critical charge is proportional to the magnitude of the coupling. (For this system the constant of proportionality is a function of gating capacitance.)
However, the simplest way to investigate q_{crit} is use the critical charge calculation module of the general network solver to graph their value against C_S. This is done in figure 6.24. For low C_S all critical charges are $q_{crit} = e/3$, but as C_S is increased $q_{crit} \rightarrow e/6$, reducing the legal area of turnstile operation, by allowing more opportunity for turnstile breakdown for a given set of bias voltages.

Linear programming results based on these critical charge values are shown in figure 6.26 (for strays $C_S = C/10$, the point where major change in critical charges is starting to occur). Overlaid on these graphs are Monte Carlo plots of legal turnstiling area. Comparison of figures 6.26 and 5.7 shows the reduction of legal turnstiling area caused by the modification of system critical charge values.

Greater insight into system symmetry breaking can also be gleaned from figure 6.26. Firstly note that the Monte Carlo data contains points where perfect turnstiling action occurs, and where one electron is lost. Further modelling shows that for these points,

one electron is lost independent of the number of electrons finally transferred. The immediate implication is of an electron being 'lodged' at a particular device electrode. Such an electron may perturb the potential map of the system, 'locking' itself in position, and effecting the remaining electron flow through both turnstiles. This is one clear possible source of symmetry breaking with random chance determining which turnstile first has an electron lodge in its structure.
Secondly, note the discrepancy between the Monte Carlo modelled area of turnstiling action and that indicated by the linear programming technique. The Monte Carlo areas follow the critical boundaries of the linear programming technique, but are offset from them. This suggests normal turnstiling - perturbed by a fractional charge caused by the charge configuration of the other operating turnstile.
Modification of the linear programming boundaries of one turnstile due to an electron trapped on an opposing turnstile can be calculated by the modelling program. This was done and the best fit results are shown as hairlines overlaid on figure 6.26. It is found that no one opposing electron configuration reproduces the Monte Carlo data. For instance, in parallel electron flow, line C of figure 6.26 is modified to fit the Monte Carlo data when a single excess electron occupies electrode 1. Line D fits when the electron occupies electrode 2 (the central electrode). However all the fitting configurations represent situations of normal electron flow in the opposing device. This indicates another possible source of system symmetry breaking. Instead of a single electron lodged at one device electrode, one turnstile may be lodged into a particular set of state transitions for electron transfer. The charge configurations of these state transitions would then directly effect the probability of electron transfers in the opposing turnstile - thus altering the current through that device.

From the results of figures 6.24 and 6.26 then, a more detailed explanation of the responses of figure 6.25 can be given. At $C_S = 10^4$ C the 'iris' of linear programming lines formed by the area of turnstiling action has been reduced until the bias points of the two turnstiles are in areas of imperfect turnstiling. The first random tunnelling events in the system may induce an electron to lodge in one of the turnstiles. More likely, they will give events in one turnstile a self perpetuating priority. Since the system is in breakdown (i.e electron flow is a combination of blockaded and non-blockaded effects) this will change the transmission coefficient of each device. The result will be differing numbers of transmitted electrons through each side of the system in a given time. Finally, the differing charge configurations experienced by each turnstile as the other is biased for parallel or antiparallel electron flow will modify both non-ideal transmission coefficients and the parameters under which ideal turnstiling action is seen.

For practical systems we are less interested in coupling effects than in the conditions under which they can be avoided. A simple approach would modify each of the event lines bounding the area of ideal operation of a system according to all possible coupled charge configurations. The minimum resultant area is sure to give stable operation. However this would unnecessarily restrict the area of ideal operation. Work is in progress to develop a scheme for choosing appropriate boundary events automatically.

6.4.2 Bit Error Rates in Coupled Turnstiles

The above results deal with single electron devices that clock a controlled number of excess electrons from source to drain via applied gate frequency. Such systems are of interest as electrometers. However for use in digital systems, the ability to cope accurately with more realistic bit patterns (presence and absence of excess electrons) is necessary.

Description of Results :

As a first step in investigating such information flow, the circuit of figure 6.23 is again considered. A '1' can be injected into the turnstile by biasing V_A at some level over the period of turnstiling (controlled by the frequency of square wave applied to V_G). A '0' can be injected by biasing $V_A = 0$ over the same period. If an appropriate '1' or '0' is ejected from the turnstile at the end of this period then we may consider the bit to have been transferred successfully. In these experiments a pseudo-random bitstream with an equal proportion of '1's & '0's was used.
Results of investigating bit error rates are shown in figures 6.27 - 6.29. Bias conditions both at the centre of the device turnstiling area, and in the areas of imperfect turnstiling, are considered. Unless noted otherwise, both turnstiles are active when the measurements are taken. However data is only collected from one turnstile.

Figure 6.27 show the number of successfully transferred bits through a coupled turnstile with bias conditions around the boundary line 'C' of figure 6.26. The solid trace [0.21,-2.3] is well within the perfect turnstiling area of a device only transmitting '1's. Successive traces are closer to the boundary, with the final one [0.15,-2.6] outside it. The hairline trace [0.23,-2.1] is biased in the centre of the legal turnstiling area (again for a device only transmitting '1's). It is immediately obvious that it is more difficult to perfectly transmit a random bitstream. This is because additional possible device states must now be considered, some of which lead to imperfect

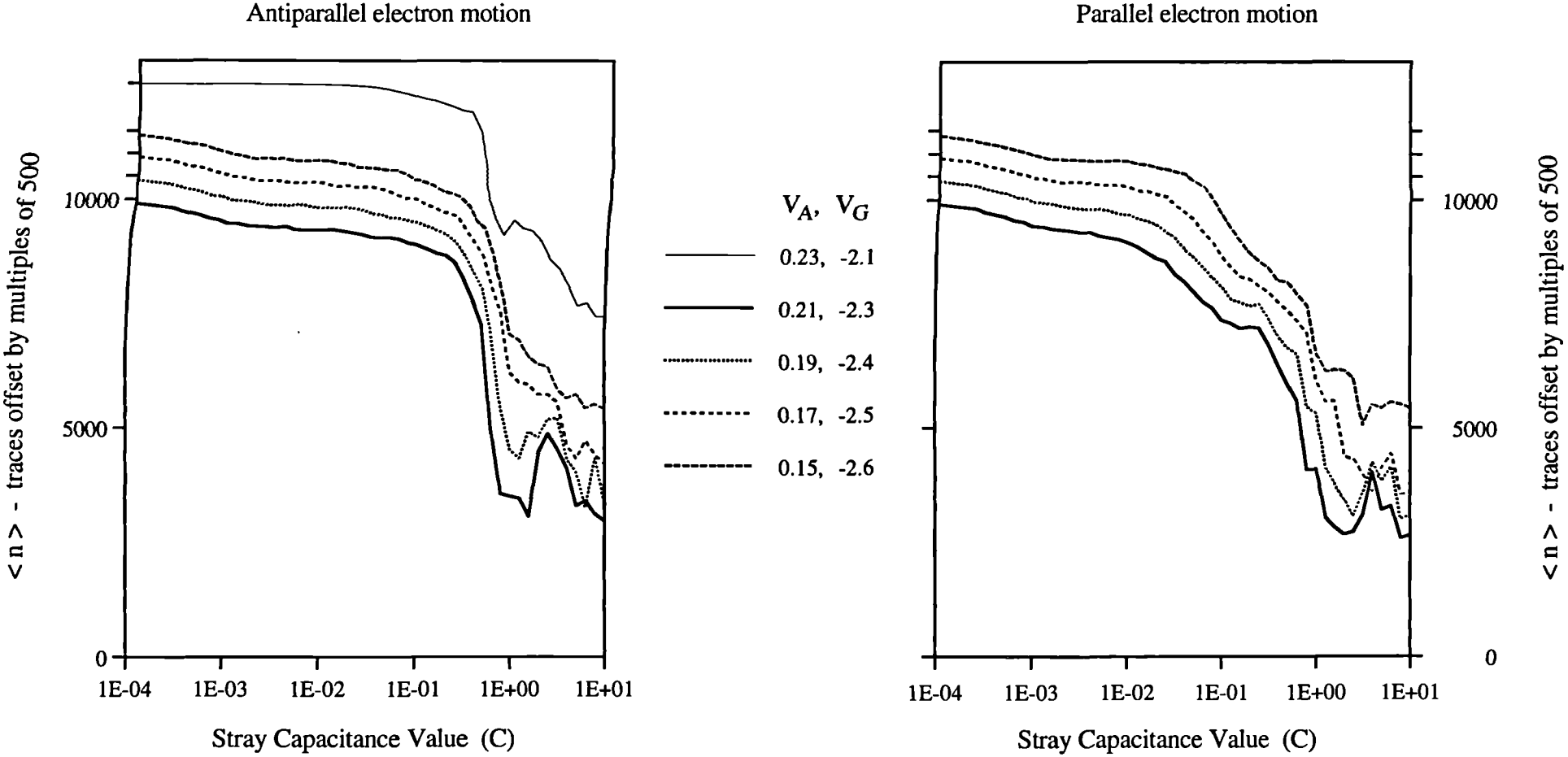


Fig 6.27 Graphs of **bitstream accuracy** of a **four junction gated turnstile** linked to another active turnstile by a simple model of stray capacitance (see figure 6.23). A random (50% '1's and '0's) pattern of 10000 bits is presented to the input of the turnstile, and the number of correctly transferred bits is measured. Majority electron flow both parallel and antiparallel to that in the second device is plotted. The hairline plot describes operation at the centre of the legal turnstiling area, other plots are taken through the edge of this area (see figure 6.26).

Turnstile junction capacitances C, gate capacitances C/2.

transmission. Thus even at coupling capacitance values of $< 10^{-4}$ C perfect turnstiling action has already broken down, unless the device is biased centrally.
Two other structures are also evident in the traces. Firstly, below $C_S \approx C$, the drop in correctly transferred bits is smooth and overlaid with regular peaks. The position of these peaks varies with bias. They are most clearly seen on the traces of parallel electron motion. Secondly, between $C < C_S < 10C$, a large peak is seen, both in the graphs of parallel and antiparallel electron motion.

Analysis :

For an explanation of the large peak between $C < C_S < 10C$, again consider figure 6.26. Here the area marked out by lines 'A' to 'D' represent perfect turnstiling, with one electron clocked through in a single time period. There are geometrically similar areas mapped out for larger values of V_G. In these regions V_G is large enough to avalanche a number of electrons into the central electrode of the device during the electron input phase. On average the current through the device remains the same, controlled by V_A. However detailed control of electrons is lost. Once such control is lost, the boundaries of successive regions (increasing V_G) define a modulation of the transmission coefficient of real bitstreams. In each successive region a greater number of sets of state transitions are possible, and the magnitude of modulation is less pronounced.
In figure 6.27, the increased stray capacitance produces a drop in q_{crit} values from 1/3 to 1/6. To first order, this is equivalent to halving the scale of the V_G axis. This moves the device bias point out of an area of detailed control into the next similar area of higher V_G. As the bias point moves through this area, the modulation peak between C & 10C is produced.

The smaller modulations of the fall-off traces of figure 6.27 are the result of different phenomena. As noted above, various sets of state transitions may produce the same effect - one bit moving through the turnstile. Which of these conduction routes predominates depends on bias and coupling conditions.
As an example, for the system of figure 6.23 with turnstiles biased at [0.23,-2.1] and [0,0] respectively (i.e $[V_A,V_G]$ scaled to 1/(e/C)) there are two main electron conduction paths. Which path is taken depends on the first state transition. The normalised probability of the transition $[0,0,0] \rightarrow [1,0,0]$ can be calculated as,

$$\Gamma_{10} = \frac{12 + 27s + 17s^2 + 6s^3}{4\,(4 + 11s + 9s^2 + 3s^3)} \qquad (6.13)$$

while the contribution of the transition $[0,0,0] \rightarrow [-1,1,0]$ is,

$$\Gamma_{-11} = \frac{(1+s)(4+13s+6s^2)}{4\,(4+11s+9s^2+3s^3)} \qquad (6.14)$$

(s is given by by $C_S = C/s$). These results assume no excess electrons in the opposite turnstile. At very low coupling capacitance there is a 50% probability of either event occurring, and both lead to perfect electron transfer. At the point where s is low enough to negate this simple analysis, the $[0,0,0] \rightarrow [1,0,0]$ transition will occur 57% of the time.

If effects from the second turnstile are ignored, and only transmission of '1's is assumed, then both the above conduction paths are equally valid. In more realistic circumstances, one of the paths will be more likely to lead to perfect transmission. Thus as coupling capacitance is varied, both the probability of a given conduction path occurring *and* its chance of leading to perfect bit transmission varies. The structure associated with the fall-off traces of figure 6.27 is caused by the interplay of a number of such differing conduction paths.

Accuracy for Small C_S :

A problem of practical importance is turnstiling at low coupling capacitance, where real devices must operate. Figures 6.28 and 6.29 show results of experiments on turnstile accuracy under such conditions. Figure 6.28 gives the number of accurately transferred bits for a turnstile biased in the centre of its area of turnstiling operation. Two traces are shown, one where the opposing turnstile is active, and the other with a zero biased or passive turnstile. (Excess electrons induced in this passive turnstile are included in the model.) Note that in each case only the accuracy of the initial turnstile is considered. Figure 6.29 expands the active trace of figure 6.28. The fractional bitstream error is plotted, with up to 10^6 bits modelled to obtain accuracy.

The modelling indicates that for a fractional error in the bitstream y, and stray capacitance value x=1/s, then x obeys a power law for low coupling. Specifically, with the second turnstile active,

$$y = (0.32 \pm 0.04)\, x^{(1.09 \pm 0.05)} \qquad (6.15)$$

And with the second turnstile passive,

$$y = (71.0 \pm 9.0)\, x^{(1.75 \pm 0.05)} \qquad (6.16)$$

The results of §6.4.1 suggest that at low coupling, turnstile accuracy should be proportional to the magnitude of coupling. Work is ongoing to further develop the detailed analytical link between coupling capacitance and bitstream accuracy.

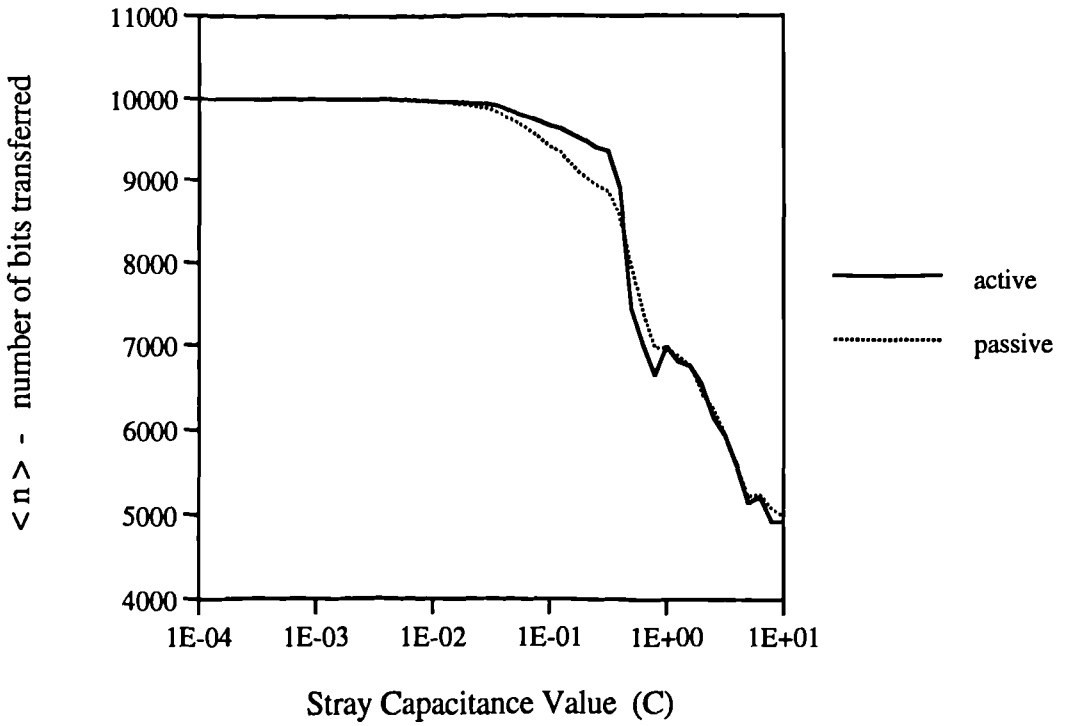


Fig 6.28 Graph of **bitstream accuracy** of a **four junction gated turnstile** linked to another through a simple model of stray capacitance (see figure 6.23).
A random (50% '1's and '0's) pattern of 10000 bits is presented to the input of the turnstile, and the number of correctly transferred bits measured. Calculations making up the 'active' plot have a seperate random bitstream in the second device, whereas for the 'passive' plot the second device has bias potentials held at 0 V/(e/C). Antiparallel bitstream flow is assumed.
Turnstile junction capacitances C, gate capacitances C/2, bias potentials of ±0.23 V/(e/C) and gate potentials of 0,-2.1 V/(e/C).

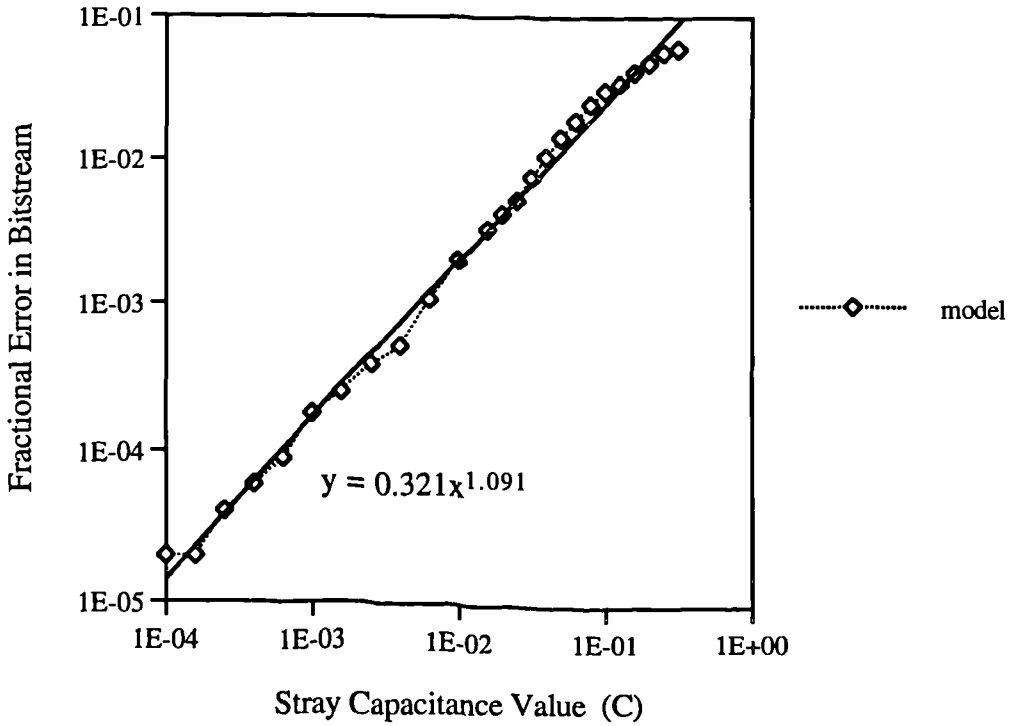


Fig 6.29 Graph of **bitstream accuracy** of a **four junction gated turnstile** linked to another active turnstile by a simple model of stray capacitance.
Plot shows the response for small stray capacitances.

6.5 Summary

Simulation tools have been applied in the investigation of a number of single electronic systems. Efforts were concentrated on tunnelling junction arrays and gated turnstiles as the basic building blocks of such systems. Two practical sources of operating imperfection were considered - component deviation and interdevice coupling.

It was found that tunnelling junction arrays are remarkably resilient to component variation. Whether random or correlated, such variation has little effect on practical arrays unless a deviation of greater than 30% is applied. As a result of this structural resilience, junction arrays are also expected to be far more resistant to the presence of external static charge than single junctions. Performance of an array is at its best when the relationship between junction and grounding strays is $C_G << C_J$.
Cross-talk in tunnelling junction arrays was investigated through modelling of a system presently under fabrication. It was found that when coupling strays were smaller than the other components of the array ($C_S << C_G, C_J$) then there was little change in system characteristics from the uncoupled state.

Gated turnstile devices - which exert control over transmitted bitstreams - are more sensitive to both component variation and interdevice coupling. This sensitivity is exhibited as a reduction in the legal turnstiling area in control parameter space. The turnstiling area is reduced by the effect of coupling capacitance on system critical charges, and by charge tunnelling in other parts of the system. These effects are complex - intrinsically as complex as the number of possible system states. However some insight into their nature was achieved by use of the Monte Carlo and linear programming tools developed in Chapter 4.
Small gating capacitances are crucial to optimising turnstile operation. They allow the greatest are of operation in control parameter space. Resilience to component variation is then achieved by biasing devices in the centre of this area. It has been predicted that three phase tunnelling devices (often referred to as electron pumps) would allow the turnstiling process to be further optimised. In practical systems, however, their extra complexity reduces their effectiveness compared with single-phase devices.
Error rates in bitstreams transmitted through coupled gated turnstiles were investigated. For the four junction gated turnstile, bit transmission errors are approximately proportional to interdevice coupling capacitance at low coupling, $C_S < C_J/10$.

CHAPTER 7 CONCLUSIONS AND FURTHER WORK

This work has considered single electronic devices - devices based on ultrasmall tunnelling junctions, and which rely for their operation on the discrete nature of an electron. They have great potential as the building blocks of integrable, digital switching systems, due to their good fabrication tolerances and self quantising logic. Energy dissipation, nominal voltage and operating speed all scale beneficially as junction capacitance is reduced.
Single electronic devices do, however, have drawbacks. These include extreme sensitivity to external charge and therefore to system wide cross-talk. Thus new tools for modelling and analysis are required if systems of practical use are to be developed.
A set of such tools has been constructed; including a general Monte Carlo modelling program, and a linear programming technique. These tools have been used to study some of the basic building blocks of single electronic systems; the tunnelling junction array and gated turnstile.

The conclusions of this investigation are presented below, and fall naturally into three sections;

- Fabrication and Geometry deals with the information required to construct a useful equivalent circuit for any given single electronic device.
- Mathematical Models considers the equations used to describe tunnelling in sets of junctions.
- Application to Specific Systems describes the results obtained when our tools are used to investigate tunnelling junction arrays or gated turnstiles.

Further work which might be accomplished in each of these three areas is also presented.

7.1 Conclusions

7.1.1 Fabrication and Geometry

At present, most geometrical capacitance estimates ignore the effect of fringing fields and thus systematically underestimate capacitance values. This is especially true when considering metal-insulator-metal junctions formed by hanging resist lithography. Accurate capacitance calculation is vital to estimate T_c and the important ratio $C_{junction}/C_{ground}$. Formulae have been developed which include fringing and therefore better estimate junction capacitance. These formulae will be of most use applied to the metal-semiconductor-metal granular systems presently under development. Capacitance calculations show that practical single-electronic devices operating reliably at liquid Nitrogen temperatures will need to be granular in nature. Present integrable fabrication techniques do not give low enough junction capacitance.

Semiconductor systems report extremely low capacitance values [74]. This is due to their increasingly quantum nature and the reduced confinement of electrons in quantum dots compared with those in metal-insulator-metal electrodes. However low capacitance is offset by stray charge problems associated with semiconductor traps. A detailed assessment of semiconductor systems requires a fuller quantum mechanical treatment outside the scope of this work.

7.1.2 Mathematical Models

Three models of electron transfer in tunnelling junctions were considered ;

- The microscopic model gives speed and simplicity of calculation, while accounting for thermal fluctuations. These are the most important source of noise effecting practical systems at present T_c values. The model assumes purely capacitive circuits.
- The phase correlation model can describe tunnelling in an electromagnetic environment, including quantum fluctuations. It assumes only that the relaxation time of the system is much shorter than the time between tunnelling events. However it is computationally expensive.
- The Lengevin equation model introduces quantum fluctuations heuristically. It leaves out much of the physics of the phase correlation theory, but allows faster computation and is compatible with the coding routines of the simple microscopic model.

Macroscopic quantum tunnelling in systems of junctions is an important 'killer' process for reliable electron transfer. Multiple junction arrays can act as buffers, minimising the effect of MQT. This will however decrease the operational speed of practical systems. The systems will themselves become more complex; requiring the use of tools such as those we have developed. Note that present computer algorithms do not account for MQT or cotunnelling processes.

7.1.3 Application to Specific Systems

Tunnelling Junction Arrays :

The properties of ideal, homogeneous tunnelling junction arrays are well described by the analytical work of Bakhvalov *et al.* [12]. They are optimised when grounding capacitance is as low as possible in relation to junction capacitance. This increases the device operating area in bias space. It increases the size of solitons within the array and thus their spacial correlation.

To investigate more realistic tunnelling junction arrays with a variation of component values, additional tools are required. On modelling a wide range of tunnelling arrays with the General Network Solver, it was found that;

- The array threshold voltage at zero offset bias is a good figure of merit. Variation of threshold voltage with component deviation is a good indication of array stability.
- Junction arrays are found to be very resilient to component variation. For practical capacitance values (junction and grounding capacitance within an order of magnitude of each other) the devices are stable for deviations of standard deviation $< 30\%$.
- Correlation of component deviation has no noticeable effect over that of random deviation. Deviation of single capacitance values by an order of magnitude likewise has no noticeable effect.

This resilience to component variation suggests that tunnelling junction arrays will have a resilience to static external charge.

Gated Turnstile Systems :

The frequency response of an idealised, single phase, 4-junction turnstile was investigated analytically and by Monte Carlo modelling (microscopic model, $T \rightarrow 0$). The error rate of electron transmission increases exponentially with frequency. When gating capacitance $C_G = C/2$, a 1% error rate corresponds to a frequency 5 times lower than the critical frequency $f_{crit} = 1/CR_t$.

Single phase and three phase 4-junction turnstiles were compared. Under typical operating conditions there is no advantage in using a three phase turnstile. Its extra complexity reduces the area in operating parameter space in which perfect turnstiling occurs. Therefore, under normal fabrication deviations, three phase devices are more likely to fail in integrated systems. Using equivalent tunnelling junctions, no advantage in operating speed was seen for the three phase devices.

Coupled Systems :

When coupling strays are lower than grounding capacitance and junction capacitance in coupled tunnelling junction arrays, there is little effect on the IV characteristic of the system. These arrays show a structural resilience to cross talk when charge flow is steady.

In coupled gated turnstiles two types of deviation must be considered. Firstly, the effect of coupling on critical charge values. Secondly, the effect of non-static charge from one part of the system on the remainder. Both reduce the area of legal turnstiling in control parameter space. The effects are intrinsically complex in nature; however some practical insight can be gained using our tools. The General Network Solver provides information on the preferred sets of state transitions allowing current flow (which sets are allowed, and the probability of each occurring under given bias conditions). The linear programming technique can supply a worst case area of legal operation for the system. Bit error rates in coupled turnstiles were also investigated, and work is ongoing in developing general results.

7.2 Further Work

7.2.1 Fabrication and Geometry

The most pressing need is to perform accurate finite element calculations on the geometry of granular systems presently under fabrication. Comparison of the two spheres formula with some specific finite element results will indicate just how accurate its geometrical approximations are in practice. Such data will help tune the model as a good first order estimate of capacitance.

In the longer term, a detailed understanding of charge anomalies in semiconductor systems must be gained - both considering static and non-static stray charge. The simulation tools that have been developed are only as good as the equivalent circuit model describing the system. This must accurately account for such strays. The effec-

tive capacitance of semiconductor systems is very good, but such qualities are of little use if stray charge problems are insurmountable.

7.2.2 Mathematical Models

The theoretical descriptions of electron tunnelling in ultrasmall, ultra-low capacitance junctions are mature. They need only be encoded into the present simulation tool routines. Use of the heuristic quantum Langevin equation to include quantum fluctuations in the model requires little recoding, at the cost of a moderate increase in computational effort.
More accurate, however, is the full phase correlation theory. This would require extensive recoding and be computationally expensive, but would not involve change in the basic algorithms of the general network solver. To speed the simulation, a three stage approach is required. First, preliminary modelling with one of the simpler sets of tunnelling equations. Second, calculation of tunnelling probability look up tables - based on the range of potentials and effective impedances derived in the preliminary modelling. Finally, a more accurate modelling pass, interpolating from the calculated look up tables.

Further work is also required to fully automate the linear programming method. This involves further research into the nature of state transition sets; to discover general rules governing which transition lines are critical to the operation of any general system.

7.2.3 Application to Specific Systems

A number of avenues of investigation immediately present themselves. These include;

- A more detailed analysis of symmetry breaking in coupled systems (i.e the phenomena of self perpetuating sets of state transitions, and of excess electrons lodging on device electrodes). A complete understanding of symmetry breaking will allow us to avoid over restrictive system bias conditions. These are calculated by the linear programming technique, but without guiding rules the calculations can only easily be performed for 'worst case' coupling - avoiding *all* possible sets of interfering state transitions. A deeper understanding would limit calculations to only those interfering state transitions that degrade system performance. It might also allow development of information coding to avoid such interfering state transitions. This would allow increased tolerance to interdevice coupling.

These principles may also allow the design of systems where the trapping of excess electrons is desirable (for example the memory cell design of [118]).

- Consideration of coupled, gated turnstiles away from idealised $T \rightarrow 0$. It would be useful to compare the magnitude of thermally induced transmission errors with those due to coupling - and the effect of thermal fluctuations on coupling induced errors.
- While tunnelling junction arrays are remarkably stable for situations where charge flow is continuous, they are not as appropriate for the transmission of realistic bit-stream patterns. In long arrays, soliton energies tend to push excess electrons into stable, equidistant configurations, with resultant information loss. This can be counteracted by gating the array (forming a shift register) or slowing transmission speed (making the interbit spacing in the array greater). Tunnelling junction arrays are used as buffers to resist Macroscopic Quantum Tunnelling. However unless gated, the speed of the buffered system will automatically be reduced. The trade off between buffer blockade resistance and operation speed in practical systems requires investigation.

Of equal importance are more detailed analyses of basic tunnelling junction arrays and gated turnstiles. It is important that additional terms in the capacitance matrix are considered; including next nearest neighbour coupling, coupling to external potentials and coupling to external strays. However, to do this requires a detailed knowledge of the system capacitance matrix. This requires information on the geometry of real systems (including the position of ground planes and voltage sources). It also requires a more accurate estimation of equivalent circuit values derived from system geometry. Such data can only be obtained by finite element analysis of practical systems.

APPENDIX A ELEMENTARY STABILITY ANALYSIS OF TUNNELLING JUNCTION ARRAYS

Motivation :

The modelling of tunnelling junction arrays is discussed in Chapters 5 & 6, with particular emphasis on the stability of the correlated electron movement through the array with respect to deviation of component values (the grounding and junction capacitances making up the array). This was done to model the effect of the natural deviations that would occur in the fabrication of such systems.
An analytical adjunct to that numerical work is desired.

Theory : [125]

We consider autonomous systems of the form $\ddot{x} = -f(x,\dot{x})$ with equivalent equations;

$$\dot{x} = y,\ \dot{y} = -f(x,y) \qquad (A.1) \qquad \text{so that} \quad \frac{dy}{dx} = -\frac{f(x,y)}{y} \qquad (A.2)$$

Equation A.1 describes the system with respect to time, while equation A.2 describes a *trajectory* in *phase space* (i.e in the x,y or x,$\dot{x}$ plane) which represents the system, and along which the system progresses as it changes state.
Singular points of the system equations occur when $x = 0,\ y = 0$ (always on the x-axis of the phase plane) and correspond to points of stable or unstable system equilibrium
We can re-write equation A.1 as $\dot{x} = ax + by + P(x,y),\ \dot{y} = cx + dy + Q(x,y)$ where P,Q are power series with terms of degree >2 (in our specific case a=0, b=1) and close to a singular point we can assume that they have negligible value. Hence the system can be approximately characterised (through linear analysis) by the equation,

$$S^2 - (a+d)S + (ad-bc) = 0 \qquad (A.3)$$

the roots of which indicate how trajectories approach the singular points - and thus which points show stable or unstable equilibrium.

Application of Theory to Tunnelling Junction Arrays :

The governing equation for a tunnelling junction array with junction capacitances, C, and grounding capacitances C_o, is;

$$-C\phi_{i-1} + (2C+C_o)\phi_i - C\phi_{i-1} = en_i \qquad (A.4)$$

for potential ϕ_i and number of excess charges n_i at the ith electrode.

We note that this is a discretisation of;

$$-C\varepsilon^2 \frac{d^2\phi}{dx^2} = en(x,t) - C_o\phi(x) \qquad (A.5)$$

Where n(x,t) is a discrete variable, only taking on integer values.

Our problem then becomes the investigation of the stability of a set of equations of the form A.4, or the differential equation A.5 as we perturb capacitance values, i.e vary each about C or C_o by a value ΔC or ΔC_o

There are (at least) two forms of approach to the problem. Either through equation A.4 by methods of discrete mathematics, or through equation A.5 which is close to the form discussed in 'Theory' above. The continuous version of the problem seems more promising.

It should be noted that 'n' can only take on integer values, and varies with time as tunnelling events occur. This makes equation A.5 *non-autonomous* and the problem becomes highly non-trivial. (The time varying, discrete excess charges on each electrode of tunneling devices are also the main source of problems in modelling these systems as electrical networks).

Solutions can be found for non-autonomous systems of a periodic nature, and other systems may be broken down into periodic components (somewhat akin to finding Fourier components) to form a solution.
However the step function n(x,t) is, in general, not periodic. It is therefore unlikely that solutions will be found using this method.

APPENDIX B BISPHERICAL COORDINATE SYSTEMS [126]

The defining equations of a bispherical coordinate system are;

$$x = \frac{a \sin\theta \cos\psi}{\cosh\eta - \cos\theta} \qquad y = \frac{a \sin\theta \sin\psi}{\cosh\eta - \cos\theta} \qquad z = \frac{a \sinh\eta}{\cosh\eta - \cos\theta} \tag{B.1}$$

A natural way to use this coordinate system is in problems where a sphere of radius r is considered, its centre being a distance b above the $z=0, \eta=0$ plane (see fig. 3.4). In such problems the following are useful;

$$r = a\,\mathrm{csch}\eta, \quad b = a\coth\eta \quad \text{which give} \quad \eta = \operatorname{arccosh}(b/r) \tag{B.2}$$

The metric coefficients of this system, with rotational symmetry about the z axis, are;

$$g_{11} = g_{22} = \frac{a^2}{(\cosh\eta - \cos\theta)^2} \qquad g_{33} = \frac{a^2 \sin^2\theta}{(\cosh\eta - \cos\theta)^2}$$

$$\sqrt{g} = \frac{a^3 \sin\theta}{(\cosh\eta - \sin\theta)^3} \tag{B.3}$$

It can be shown that the Laplacian $\nabla^2\phi = 0$ cannot be separated into the simple form $\phi = H(\eta)\,\Theta(\theta)\,\Psi(\psi)$ in bispherical coordinates, but *can* be R-separated [88], i.e cast into a form $\phi = U_1(u_1)\,U_2(u_2)\,U_3(u_3) / R(u_1,u_2,u_3)$ where we attempt to keep R as simple a factor as possible.

R-separation is accomplished in a rotationally derived coordinate system by considering a Stäkel determinant,

$$S = \begin{vmatrix} \Phi_{11}(\eta) & -1 & \Phi_{13}(\eta) \\ \Phi_{21}(\theta) & 1 & \Phi_{23}(\theta) \\ 0 & 0 & 1 \end{vmatrix} = \Phi_{11} + \Phi_{21} \tag{B.4}$$

and choosing $Q(u_1,u_2,u_3)$ and $R(u_1,u_2,u_3)$ so that the following hold true;

$$g_{ii} = \frac{S}{M_{i1}} Q\,, \qquad \frac{\sqrt{g}}{QS} = f_1(u_1)\, f_2(u_2)\, f_3(u_3)\, R^2 \tag{B.5}$$

where M_{ij} are the cofactors of S, and f_i are any functions of u_i.

Then separability will occur if;

$$\alpha_1 = -\frac{Q}{R}\sum_{i=1}^{3}\frac{1}{f_i g_{ii}}\frac{\partial}{\partial u_i}\left(f_i\frac{\partial R}{\partial u_i}\right) \qquad \alpha_1 \text{ constant,} \tag{B.6}$$

and the solutions of ϕ will be $U_i(u_i)$ given by;

$$\frac{1}{f_i}\frac{d}{du_i}\left(f_i\frac{dU_i}{du_i}\right)+ U_i\sum_{j=1}^{3}\alpha_j\Phi_{ij} = 0 \tag{B.7}$$

For bispherical coordinates, using B.4 and B.5, we choose;

$$Q=\frac{a^2}{(\cosh\eta - \cos\theta)^2} \qquad \text{to give} \qquad \frac{S}{M_{11}}=1,\ \frac{S}{M_{21}}=1,\ \frac{S}{M_{31}}=\sin^2\theta$$

so,

$$S=\begin{vmatrix} 1 & -1 & 0 \\ 0 & 1 & -\csc^2\theta \\ 0 & 0 & 1 \end{vmatrix} = 1$$

to finally obtain $f_1 = 1,\ f_2 = a\sin\theta,\ f_3 = 1,\ R = (\cosh\eta - \cos\theta)^{-1}$
and after some manipulation, substituting into B.6, $\alpha_1 = -\frac{1}{4}$

$\therefore$ Laplace's equation is R-separable in bispherical coordinates with solutions of form

$$\phi = (\cosh\eta - \cos\theta)^{1/2}\, H(\eta)\, \Theta(\theta)\, \Psi(\psi) \tag{B.8}$$

where, using B.7, on substitution of $\alpha_3 = m^2,\ \alpha_2 = p(p+1),\ \xi = \cos\theta$;

$$\frac{d^2H}{d\eta^2} - \left(p+\frac{1}{2}\right)^2 H = 0 \tag{B.9a}$$

$$(1-\xi^2)\frac{d^2\Theta}{d^2\xi} - 2\xi\frac{d\Theta}{d\xi} + \left[p(p+1) - \frac{m^2}{1-\xi^2}\right]\Theta = 0 \tag{B.9b}$$

$$\frac{d^2\Psi}{d^2\psi} + m^2\,\Psi = 0 \tag{B.9c}$$

The general solutions of these equations are of the form

$$\Psi = A\sin m\psi + B\cos m\psi \tag{B.10a}$$

$$H = A\, e^{(p+1/2)\eta} + B\, e^{-(p+1/2)\eta} \tag{B.10b}$$

$$\Theta = A\, P_p^m(\xi) + B\, Q_p^m(\xi) \tag{B.10c}$$

APPENDIX C RESULTS NECESSARY TO OBTAIN THE CAPACITANCE OF TWO SPHERICAL CONDUCTORS.

(Conductors are of arbitrary diameter and surrounded by dielectric shells. The method approximately follows a solution laid out in [87, p. 380])

The problem is solved in a bispherical coordinate system by finding the potential functions ϕ_i i n the three regions of differing dielectric constant ε_i, each region requiring a superposition of two fields ϕ_i^{I} and ϕ_i^{II}. These solutions are then matched through equations governing continuity of **E** and **D** across dielectric boundaries.

Note that because of the nature of bispherical coordinates, if boundaries of the dielectric shells and metal spheres are taken at constant η values, they will only be concentric as $\eta \to 0$.

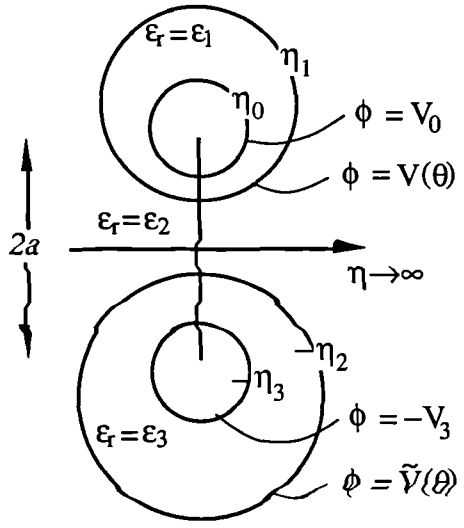


Fig C.1 Schematic representation of two metal spheres surrounded by dielectric shells and sitting in a dielectric medium.

Assuming a rotational symmetry about the ψ axis, and the necessity of finite potential solutions at the dielectric and dielectric/metal boundaries, the general form of the potential function in bispherical coordinates is ;

$$\phi = (\cosh\eta - \cos\theta)^{1/2} P_p(\cos\theta) [A_p e^{(p+1/2)\eta} + B_p e^{-(p+1/2)\eta}] \qquad (C.1)$$

Region 1

$\phi_1 = \phi_1^{I} + \phi_1^{II}$ where ϕ_1^{I} is the potential function with; $\phi=V_0$ at $\eta=\eta_0$, $\phi=0$ at $\eta=\eta_1$
and ϕ_1^{II} is the potential function with; $\phi=0$ at $\eta=\eta_0$, $\phi=V(\theta)$ at $\eta=\eta_1$

assume solution,

$$\phi_1^I = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\,[A_n e^{(n+1/2)\eta} + B_n e^{-(n+1/2)\eta}]$$

at $\eta = \eta_1$, boundary conditions give,

$$0 = (\cosh\eta_1 - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\,[A_n e^{(n+1/2)\eta_1} + B_n e^{-(n+1/2)\eta_1}]$$

$$(\text{i.e} \quad B_n = -A_n e^{2(n+1/2)\eta_1})$$

so $$\phi_1^I = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n[e^{(n+1/2)\eta} - e^{2(n+1/2)\eta_1} e^{-(n+1/2)\eta}]$$

or $$\phi_1^I = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{1I} \frac{e^{(n+1/2)\eta} - e^{2(n+1/2)\eta_1} e^{-(n+1/2)\eta}}{e^{(n+1/2)\eta_0} - e^{2(n+1/2)\eta_1} e^{-(n+1/2)\eta_0}} \qquad (C.2)$$

where each A_n has been redefined by a multiplicative constant.

at $\eta = \eta_0$, the other boundary condition gives (after cancellation),

$$V_0 = (\cosh\eta_0 - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{1I}$$

this shows '$V_0 (\cosh\eta_0 - \cos\theta)^{-1/2}$' expanded as a series of Legendre functions. By the theory of such orthogonal functions [127],

$$A_n^{1I} = V_0 \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu)\, (\cosh\eta_o - \mu)^{-1/2}\, d\mu \qquad \text{where } \mu = \cos\theta \qquad (C.3)$$

similarly, considering the boundary conditions for ϕ_1^{II} we obtain,

$$\phi_1^{II} = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{1II} \frac{e^{(n+1/2)\eta} - e^{2(n+1/2)\eta_0} e^{-(n+1/2)\eta}}{e^{(n+1/2)\eta_1} - e^{2(n+1/2)\eta_0} e^{-(n+1/2)\eta_1}} \qquad (C.4)$$

with $$A_n^{1II} = \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu)\, V(\mu)\, (\cosh\eta_1 - \mu)^{-1/2}\, d\mu \qquad (C.5)$$

Region 2

$\phi_2 = \phi_2^I + \phi_2^{II}$ where ϕ_2^I is the potential function with; $\phi=V(\theta)$ at $\eta=\eta_1$, $\phi=0$ at $\eta=-\eta_2$

and ϕ_2^{II} is the potential function with; $\phi=0$ at $\eta=\eta_1$, $\phi=\tilde{V}(\theta)$ at $\eta=-\eta_2$

by the same techniques outlined above, we obtain,

$$\phi_2^I = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{2I}\, \frac{e^{(n+1/2)\eta} - e^{-2(n+1/2)\eta_2}\, e^{-(n+1/2)\eta}}{e^{(n+1/2)\eta_1} - e^{-2(n+1/2)\eta_2}\, e^{-(n+1/2)\eta_1}} \qquad (C..6)$$

with
$$A_n^{2I} = \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu)\, V(\mu)\, (\cosh\eta_1 - \mu)^{-1/2}\, d\mu \qquad (C.7)$$

and,

$$\phi_2^{II} = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{2II}\, \frac{e^{(n+1/2)\eta} - e^{2(n+1/2)\eta_1}\, e^{-(n+1/2)\eta}}{e^{-(n+1/2)\eta_2} - e^{2(n+1/2)\eta_1}\, e^{(n+1/2)\eta_2}} \qquad (C.8)$$

with
$$A_n^{2II} = \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu)\, \tilde{V}(\mu)\, (\cosh\eta_2 - \mu)^{-1/2}\, d\mu \qquad (C.9)$$

Region 3

$\phi_3 = \phi_3^I + \phi_3^{II}$ where ϕ_3^I is the potential function with; $\phi=0$ at $\eta=-\eta_2$, $\phi=-V_3$ at $\eta=-\eta_3$

and ϕ_3^{II} is the potential function with; $\phi=\tilde{V}(\theta)$ at $\eta=-\eta_2$, $\phi=0$ at $\eta=-\eta_3$

again we obtain,

$$\phi_3^I = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{3I}\, \frac{e^{(n+1/2)\eta} - e^{-2(n+1/2)\eta_2}\, e^{-(n+1/2)\eta}}{e^{-(n+1/2)\eta_3} - e^{-2(n+1/2)\eta_2}\, e^{(n+1/2)\eta_3}} \qquad (C.10)$$

with
$$A_n^{3I} = -V_3 \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu)\, (\cosh\eta_3 - \mu)^{-1/2}\, d\mu \qquad (C.11)$$

and,

$$\phi_3^{II} = (\cosh\eta - \cos\theta)^{1/2} \sum_{n=0}^{\infty} P_n(\cos\theta)\, A_n^{3II}\, \frac{e^{(n+1/2)\eta} - e^{-2(n+1/2)\eta_3}\, e^{-(n+1/2)\eta}}{e^{-(n+1/2)\eta_2} - e^{2(n+1/2)\eta_3}\, e^{(n+1/2)\eta_2}} \qquad (C.12)$$

with
$$A_n^{3II} = \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu)\, \tilde{V}(\mu)\, (\cosh\eta_2 - \mu)^{-1/2}\, d\mu \qquad (C.13)$$

To aid in simplifying these equations we note that,

$$\frac{e^{(n+1/2)\eta} - e^{2(n+1/2)\eta_x} e^{-(n+1/2)\eta}}{e^{(n+1/2)\eta_y} - e^{2(n+1/2)\eta_x} e^{-(n+1/2)\eta_y}} = \frac{\sinh[(n+1/2)(\eta-\eta_x)]}{\sinh[(n+1/2)(\eta_y-\eta_x)]} \qquad \text{(C.14)}$$

and that,

$$A_n^{2I} = A_n^{1II}, \qquad A_n^{2II} = A_n^{3II} \qquad \text{(C.15a,b)}$$

which produce the following simplification,

$$\phi_1 = (\cosh\eta - \mu)^{1/2} \sum_{n=0}^{\infty} P_n(\mu) \left(A_n^{1I}\sinh[(n+1/2)(\eta-\eta_1)] \right. \qquad \text{(C.16)}$$

$$\left. - A_n^{1II}\sinh[(n+1/2)(\eta-\eta_0)] \right) / \sinh[(n+1/2)(\eta_0-\eta_1)]$$

$$\phi_2 = (\cosh\eta - \mu)^{1/2} \sum_{n=0}^{\infty} P_n(\mu) \left(A_n^{1II}\sinh[(n+1/2)(\eta+\eta_2)] \right. \qquad \text{(C.17)}$$

$$\left. - A_n^{3II}\sinh[(n+1/2)(\eta-\eta_1)] \right) / \sinh[(n+1/2)(\eta_1+\eta_2)]$$

$$\phi_3 = (\cosh\eta - \mu)^{1/2} \sum_{n=0}^{\infty} P_n(\mu) \left(A_n^{3I}\sinh[(n+1/2)(\eta+\eta_2)] \right. \qquad \text{(C.18)}$$

$$\left. - A_n^{3II}\sinh[(n+1/2)(\eta+\eta_3)] \right) / \sinh[(n+1/2)(\eta_2-\eta_3)]$$

$$A_n^{1I} = V_0 \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu) (\cosh\eta_0 - \mu)^{-1/2} \, d\mu \qquad \text{(C.19)}$$

$$A_n^{1II} = \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu) \, V(\mu) (\cosh\eta_1 - \mu)^{-1/2} \, d\mu \qquad \text{(C.20)}$$

$$A_n^{3I} = -V_3 \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu) (\cosh\eta_3 - \mu)^{-1/2} \, d\mu \qquad \text{(C.21)}$$

$$A_n^{3II} = \left(\frac{2n+1}{2}\right) \int_{-1}^{1} P_n(\mu) \, \tilde{V}(\mu) (\cosh\eta_2 - \mu)^{-1/2} \, d\mu \qquad \text{(C.22)}$$

We wish to eliminate the $V(\mu)$, $\tilde{V}(\mu)$ terms which are unknown functions of $\mu = \cos\theta$. This is done by finding formulae for $\mathbf{E}$ and (assuming homogeneous media) $\mathbf{D} = \varepsilon_0\varepsilon_r\mathbf{E}$ in each region and matching boundary conditions [86, p. 316].

$$\mathbf{E} = -\text{grad}\phi = \frac{\mathbf{e}_\eta}{\sqrt{g_{11}}}\frac{\partial\phi}{\partial\eta} + \frac{\mathbf{e}_\theta}{\sqrt{g_{22}}}\frac{\partial\phi}{\partial\theta} + 0 = \frac{(\cosh\eta - \cos\theta)}{-a}\left\{ \frac{\partial\phi}{\partial\eta} + \frac{\partial\phi}{\partial\theta} \right\} \qquad \text{(C.23)}$$

Continuity of **E** ; across dielectric boundaries tangential **E** field values are equal, at metal/dielectric boundaries the tangential **E** field values are = 0. (These conditions are fulfilled automatically and performing these calculations simply verifies algebraic manipulation).

Continuity of **D** ; across dielectric boundaries normal **D** field values are equal, i.e D_η is constant across $\eta_1,-\eta_2$. at metal/dielectric boundaries the normal **D** field values integrate to ρ, the charge density.

obtain, using $\zeta = n+1/2$ for clarity,

$$\frac{\partial\phi_1}{\partial\eta} = (\cosh\eta - \mu)^{-1/2} \sum_{n=0}^{\infty} \frac{P_n(\mu)}{\sinh[\zeta(\eta_0-\eta_1)]} \{\tfrac{1}{2}\sinh\eta\,(A_n^{1I}\sinh[\zeta(\eta-\eta_1)] - \quad (C.24)$$

$$A_n^{1II}\sinh[\zeta(\eta-\eta_0)]) + \zeta\,(\cosh\eta - \mu)\,(A_n^{1I}\cosh[\zeta(\eta-\eta_1)] - A_n^{1II}\cosh[\zeta(\eta-\eta_0)])\}$$

$$\frac{\partial\phi_2}{\partial\eta} = (\cosh\eta - \mu)^{-1/2} \sum_{n=0}^{\infty} \frac{P_n(\mu)}{\sinh[\zeta(\eta_1+\eta_2)]} \{\tfrac{1}{2}\sinh\eta\,(A_n^{1II}\sinh[\zeta(\eta+\eta_2)] - \quad (C.25)$$

$$A_n^{3II}\sinh[\zeta(\eta-\eta_1)]) + \zeta\,(\cosh\eta - \mu)\,(A_n^{1II}\cosh[\zeta(\eta+\eta_2)] - A_n^{3II}\cosh[\zeta(\eta-\eta_1)])\}$$

$$\frac{\partial\phi_3}{\partial\eta} = (\cosh\eta - \mu)^{-1/2} \sum_{n=0}^{\infty} \frac{P_n(\mu)}{\sinh[\zeta(\eta_2-\eta_3)]} \{\tfrac{1}{2}\sinh\eta\,(A_n^{3I}\sinh[\zeta(\eta+\eta_2)] - \quad (C.26)$$

$$A_n^{3II}\sinh[\zeta(\eta+\eta_3)]) + \zeta\,(\cosh\eta - \mu)\,(A_n^{3I}\cosh[\zeta(\eta+\eta_2)] - A_n^{3II}\cosh[\zeta(\eta+\eta_3)])\}$$

Matching of boundary conditions occurs when,

$$\varepsilon_1 \left.\frac{\partial\phi_1}{\partial\eta}\right|_{\eta_1} = \varepsilon_2 \left.\frac{\partial\phi_2}{\partial\eta}\right|_{\eta_1} \qquad \text{and} \qquad \varepsilon_2 \left.\frac{\partial\phi_2}{\partial\eta}\right|_{-\eta_2} = \varepsilon_3 \left.\frac{\partial\phi_3}{\partial\eta}\right|_{-\eta_2} \quad (C.27a,b)$$

If we assume that the above equations hold true for the summations if and only if they hold for each n then we obtain,

$$\frac{\varepsilon_1}{2}\sinh\eta_1\, A_n^{1II} + \frac{\varepsilon_1(\cosh\eta_1 - \cos\theta)\,\zeta}{\sinh[\zeta(\eta_0-\eta_1)]}\{A_n^{1I} - A_n^{1II}\cosh[\zeta(\eta_0-\eta_1)]\} \qquad \text{(C.28)}$$

$$= \frac{\varepsilon_2}{2}\sinh\eta_1\, A_n^{1II} + \frac{\varepsilon_2(\cosh\eta_1 - \cos\theta)\,\zeta}{\sinh[\zeta(\eta_1+\eta_2)]}\{A_n^{1II}\cosh[\zeta(\eta_1+\eta_2)] - A_n^{3II}\}$$

and,

$$-\frac{\varepsilon_2}{2}\sinh\eta_2\, A_n^{3II} + \frac{\varepsilon_2(\cosh\eta_2 - \cos\theta)\,\zeta}{\sinh[\zeta(\eta_1+\eta_2)]}\{A_n^{1II} - A_n^{3II}\cosh[\zeta(\eta_1+\eta_2)]\} \qquad \text{(C.29)}$$

$$= -\frac{\varepsilon_3}{2}\sinh\eta_2\, A_n^{3II} + \frac{\varepsilon_3(\cosh\eta_2 - \cos\theta)\,\zeta}{\sinh[\zeta(\eta_2-\eta_3)]}\{A_n^{3I} - A_n^{3II}\cosh[\zeta(\eta_2-\eta_3)]\}$$

These two equations are enough to specify the potential functions in terms of A_n^{1I} and A_n^{3I} only, and so obtain ϕ_i for a given V_0, V_3.

A_n^{3I} itself can be eliminated by using the requirement that the charge on the top and bottom spheres should be equal and opposite, this fixes the voltage on one sphere, V_3, if the voltage on the other is known, V_0. To make this further simplification, formulae are required for the charge on each of the conductors.

The charge on the 'top' conductor (that bounded by $\eta=\eta_0$) is calculated by taking a Gaussian surface close to $\eta=\eta_0$, recalling that classically, only the E_η term is non-zero close to a perfect metal.

$$Q^{top} = 2\pi\varepsilon_0\varepsilon_1 a\int_{-1}^{1}(\cosh\eta_0-\mu)^{-1}\left.\frac{\partial\phi}{\partial\eta}\right|_{\eta_0} d\mu \qquad \text{with of course } \phi=\phi_1 \qquad \text{(C.30)}$$

where,

$$\left.\frac{\partial\phi}{\partial\eta}\right|_{\eta_0} = (\cosh\eta_0-\mu)^{-1/2}\sum_{n=0}^{\infty}P_n(\mu)\{\tfrac{1}{2}\sinh\eta_0\, A_n^{1I} + \qquad \text{(C.31)}$$

$$\zeta(\cosh\eta_0 - \mu)(A_n^{1I}\coth[\zeta(\eta_0-\eta_1)] - A_n^{1II}(\mu)\operatorname{csch}[\zeta(\eta_0-\eta_1)])\}$$

after some manipulation, Q is obtained as a summation of terms,

$$Q_n^{top} \approx 2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I} (\cosh\eta_0 - \mu)^{-3/2}\, \varepsilon_1 \tfrac{1}{2} \sinh\eta_0 \, d\mu + \qquad \text{(C.32)}$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I} (\cosh\eta_0 - \mu)^{-1/2}\, \varepsilon_1 \zeta \coth[\zeta(\eta_0 - \eta_1)] \, d\mu +$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I} (\cosh\eta_0 - \mu)^{-1/2} \frac{\varepsilon_1^2 \zeta \operatorname{csch}^2[\zeta(\eta_0 - \eta_1)]\, \chi}{\chi\psi + \varepsilon_2^2 \operatorname{csch}^2[\zeta(\eta_1 + \eta_2)]} \, d\mu -$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{3I} (\text{`})^{-1/2} \frac{\varepsilon_1\varepsilon_2\varepsilon_3 \zeta \operatorname{csch}[\zeta(\eta_0 - \eta_1)] \operatorname{csch}[\zeta(\eta_2 - \eta_3)] \operatorname{csch}[\zeta(\eta_1 + \eta_2)]}{\chi\psi + \varepsilon_2^2 \operatorname{csch}^2[\zeta(\eta_1 + \eta_2)]}$$

where $\chi = \varepsilon_2 \coth[\zeta(\eta_1+\eta_2)] - \varepsilon_3 \coth[\zeta(\eta_2-\eta_3)] + (\varepsilon_2-\varepsilon_3) \sinh\eta_2 / 2\zeta(\cosh\eta_2 - \mu)$

$\psi = \varepsilon_1 \coth[\zeta(\eta_1-\eta_0)] - \varepsilon_2 \coth[\zeta(\eta_1+\eta_2)] + (\varepsilon_1-\varepsilon_2) \sinh\eta_1 / 2\zeta(\cosh\eta_1 - \mu)$

(C.33a,b)

Likewise for the 'bottom' conductor,

$$-Q^{bot} = 2\pi\varepsilon_0\varepsilon_3 a \int_{-1}^{1} (\cosh\eta_3 - \mu)^{-1} \left.\frac{\partial\phi}{\partial\eta}\right|_{-\eta_3} d\mu \qquad \text{with of course } \phi=\phi_3 \qquad \text{(C.34)}$$

where,

$$\left.\frac{\partial\phi}{\partial\eta}\right|_{-\eta_3} = (\cosh\eta_3 - \mu)^{-1/2} \sum_{n=0}^{\infty} P_n(\mu) \{-\tfrac{1}{2} \sinh\eta_3\, A_n^{3I} - \qquad \text{(C.35)}$$

$$\zeta (\cosh\eta_3 - \mu) (A_n^{3I} \coth[\zeta(\eta_2-\eta_3)] - A_n^{3II}(\mu) \operatorname{csch}[\zeta(\eta_2-\eta_3)])\}$$

again after manipulation,

$$Q_n^{bot} = 2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{3I} (\cosh\eta_3 - \mu)^{-3/2}\, \varepsilon_3 \tfrac{1}{2} \sinh\eta_3 \, d\mu + \qquad (C.36)$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{3I} (\cosh\eta_3 - \mu)^{-1/2}\, \varepsilon_3 \zeta \coth[\zeta(\eta_2 - \eta_3)] \, d\mu +$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{3I} (\cosh\eta_3 - \mu)^{-1/2} \frac{\varepsilon_3^2 \zeta \operatorname{csch}^2[\zeta(\eta_2 - \eta_3)]\, \psi}{\chi\psi + \varepsilon_2^2 \operatorname{csch}^2[\zeta(\eta_1 + \eta_2)]} \, d\mu -$$

$$2\pi\varepsilon_0 a \int_{-1}^{1} P_n(\mu)\, A_n^{1I} (\text{`})^{-1/2} \frac{\varepsilon_1\varepsilon_2\varepsilon_3 \zeta \operatorname{csch}[\zeta(\eta_1 - \eta_0)] \operatorname{csch}[\zeta(\eta_2 - \eta_3)] \operatorname{csch}[\zeta(\eta_1 + \eta_2)]}{\chi\psi + \varepsilon_2^2 \operatorname{csch}^2[\zeta(\eta_1 + \eta_2)]}$$

where χ and ψ are defined as above.

In principle $Q^{top} = Q^{bot}$ can be solved to obtain a relation between A_n^{1I}, A_n^{3I} and therefore (via equations C.19, C.21) between V_0, V_3. These results can then be substituted into the formulae $C = Q/(V_0+V_3)$ to obtain the intercapacitance of the two spheres.

In practice solving the above integrals (equations C.19, C.21, C.32 and C.36) in general results in formulae which do not lend themselves to simple manipulation. However in some problems additional symmetries are present which do allow a simple formula for C to be found.

APPENDIX D INTEGRAL RESULTS NECESSARY FOR THE SOLUTION OF LAPLACE'S EQUATION IN BISPHERICAL COORDINATES.

Wish to solve $\int_{-1}^{1} P_n(\mu)\,(\cosh\eta_o-\mu)^{-1/2}\,d\mu$ and $\int_{-1}^{1} P_n(\mu)\,(\cosh\eta_o-\mu)^{-3/2}\,d\mu$ in general.

Put $\cosh\eta_o = b$, $(b-1)^{1/2} = \sqrt{2}\sinh(\eta_o/2) = \sqrt{2}\alpha$ (defining α)

$(b+1)^{1/2} = \sqrt{2}\cosh(\eta_o/2) = \sqrt{2}\beta$ (defining β)

First need to find an expansion for the number of terms μ^k in $P_n(\mu)$ and the coefficients of these terms. Use the hypergeometric expansion [128] ;

$$P_n(\mu) = F\left(-n, n+1; 1; \frac{1-\mu}{2}\right)$$

$$= \frac{\Gamma(1)}{\Gamma(-n)\Gamma(n+1)} \sum_{p=0}^{\infty} \frac{\Gamma(p-n)\,\Gamma(p+1+n)}{\Gamma(1+p)} \left(\frac{1-\mu}{2}\right)^p \frac{1}{p!}$$

$$= \frac{1}{n!\,\Gamma(-n)} \sum_{p=0}^{\infty} \frac{\Gamma(p-n)\,(p+n)!}{(p!)^2\,2^p} (1-\mu)^p \qquad \text{(D.1)}$$

i.e the coefficient of μ^k in $P_n(\mu)$ is ;

$$= \frac{(-1)^k}{n!\,\Gamma(-n)} \sum_{p=0}^{\infty} \binom{p}{k} \frac{\Gamma(p-n)\,(p+n)!}{(p!)^2\,2^p}$$

$$= (-1)^k \sum_{p=0}^{n} \binom{p}{k} \frac{(p+n)!\,(-1)^p}{(p!)^2\,(n-p)!\,2^p} = g_n^k \qquad \text{(D.2)}$$

Now consider the integral $P_n(\mu)\,(\cosh\eta_o-\mu)^{-1/2}$ and solve, considering only $\eta_0 > 0$ initially;

$$\int_{-1}^{1} \mu^k\,(b-\mu)^{-1/2}\,d\mu = -\left[\mu^k \frac{2}{1}(b-\mu)^{1/2}\right]_{-1}^{1} - \left[\mu^{k-1}\frac{2}{1}\frac{2}{3}(b-\mu)^{3/2}\,k\right]_{-1}^{1} - \left[\mu^{k-2}\frac{2}{1}\frac{2}{3}\frac{2}{5}(b-\mu)^{5/2}\,k(k-1)\right]_{-1}^{1}$$

$$\ldots - \left[\mu^0 \frac{2}{1}\frac{2}{3}\frac{2}{5}\cdots\frac{2}{2k+1}(b-\mu)^{(2k+1)/2}\,k(k-1)\ldots 1\right]_{-1}^{1}$$

by repeated integration by parts.

$$= -\sqrt{2}\alpha \sum_{j=0}^{k} \frac{(b-1)^j\, 2^{2j+1}\, k!\, j!}{(2j+1)!\,(k-j)!} + \sqrt{2}\beta \sum_{j=0}^{k} (-1)^{k-j} \frac{(b+1)^j\, 2^{2j+1}\, k!\, j!}{(2j+1)!\,(k-j)!} \qquad \text{(D.3)}$$

Two routes of simplification follow. The first is to consider the coefficients of powers b^m in the two terms above, defining γ_m^k as the coefficient in the "α" sum and $\tilde{\gamma}_m^k$ as the coefficient in the "β" sum. We then obtain for the full integral,

$$\int_{-1}^{1} P_n(\mu)\,(b-\mu)^{-1/2}\,d\mu = \sum_{k=0}^{n} \left(-\sqrt{2}\alpha \sum_{m=0}^{k} g_n^k \gamma_m^k b^m + \sqrt{2}\beta \sum_{m=0}^{k} g_n^k \tilde{\gamma}_m^k b^m \right) \qquad \text{(D.4)}$$

where we can condense the sum containing g_n^k and γ_m^k into one with a single factor Δ_n^m

$$\Delta_n^m = 2n+1 \sum_{k=m}^{n} (-1)^{k-m} \binom{k}{m} \frac{2^{k+1}\,(k+n)!}{(2k+1)!\,(n-k)!} \qquad \text{(D.5)}$$

and the sum containing g_n^k and $\tilde{\gamma}_m^k$ into $\tilde{\Delta}_n^m = (-1)^{m+n}\,\Delta_n^m$. (D.6)

This is the approach used in [87]. However a second route of simplification follows from noting that $(b-1)^j = 2^j\alpha^{2j}$ and $(b+1)^j = 2^j\beta^{2j}$. Substituting these into equation D.3 and using equation D.2 gives,

$$\int_{-1}^{1} P_n(\mu)\,(b-\mu)^{-1/2}\,d\mu = \sqrt{2} \sum_{k=0}^{n} g_n^k \sum_{j=0}^{k} \frac{2^{3j+1}\, k!\, j!}{(2j+1)!\,(k-j)!} \left[\beta^{2j+1}(-1)^{k-j} - \alpha^{2j+1}\right] \qquad \text{(D.7)}$$

Consider the coefficient, X say, of β^{2j+1} in D.7, and expand out the factor g_n^k, (ignoring the $\sqrt{2}$)

$$X = \sum_{k=j}^{n} \sum_{p=k}^{n} \frac{(p+n)!\,(-1)^p}{p!\,(n-p)!\,(p-k)!} \frac{1}{2^p} \frac{2^{3j+1}\, j!\,(-1)^j}{(2j+1)!\,(k-j)!}$$

Use the fact that $\sum_{k=j}^{n} \sum_{p=k}^{n} c_p \frac{1}{(k-j)!} \frac{1}{(k-j)!} = \sum_{p=j}^{n} c_p \frac{2^{p-j}}{(p-j)!}$ to obtain in binomial form,

$$X = (-1)^j \frac{2^{2j+1}}{(2j+1)!} (j!)^2 \sum_{p=j}^{n} \binom{n}{p}\binom{p}{j}\binom{p+n}{n} (-1)^p$$

$$= (-1)^j \frac{2^{2j+1}}{(2j+1)!} (j!)^2 \binom{n}{j} \sum_{p=j}^{n} \binom{n-j}{p-j}\binom{p+n}{n} (-1)^p \quad \text{(trinomial revision [129, p.174])}$$

$$= (-1)^j \frac{2^{2j+1}}{(2j+1)!} (j!)^2 \binom{n}{j}\binom{n+j}{j} (-1)^n \quad \text{(Tables 169,174 of [129])}$$

$$= (-1)^{j+n} \frac{2^{2j+1}}{(2j+1)!} \frac{(n+j)!}{(n-j)!} \tag{D.8}$$

Equivalent working for the α^{2j+1} term in D.7 gives the simplification,

$$\int_{-1}^{1} P_n(\mu) (\cosh\eta_0 - \mu)^{-1/2} \, d\mu = \sqrt{2} \sum_{j=0}^{n} \frac{2^{2j+1} (n+j)!}{(2j+1)! (n-j)!} \left[\beta^{2j+1}(-1)^{j+n} - \alpha^{2j+1}\right] \tag{D.9}$$

Now consider $\int_{-1}^{1} P_n(\mu) (\cosh\eta_o - \mu)^{-3/2} \, d\mu$, first decomposing $P_n(\mu)$ and then integrating by parts once to give,

$$\int_{-1}^{1} P_n(\mu) (b-\mu)^{-3/2} \, d\mu = \sum_{k=0}^{n} g_n^k \left\{ \frac{\sqrt{2}}{\alpha} - (-1)^k \frac{\sqrt{2}}{\beta} - 2k \int_{-1}^{1} \mu^{k-1} (b-\mu)^{-1/2} \, d\mu \right\} \tag{D.10}$$

Applying the result of equation D.3, expanding out the factor g_n^k, and considering the coefficient, Y say, of β^{2j}/α, (ignoring the $\sqrt{2}$)

$$Y = \sum_{k=j}^{n} \frac{(k+n)!\, 2^{2k-2}\, (k-1)!^2\, (-1)^{k-j}\, 2k}{k!\, (n-k)!\, j!\, (k-j)!\, (2k-1)!} = (-1)^j \binom{n}{j} \sum_{k=j}^{n} \binom{n-j}{k-j} \binom{k+n}{n} \binom{-1/2}{k}^{-1}$$

Simplifying, by the application of upper negation and trinomial revision [129, p.174] to the second and fourth terms of the sum,

$$Y = (-1)^j \binom{-1/2}{n}^{-1} \binom{-n-1}{j} \sum_{k} (-1)^n \binom{n-1/2}{n-k} \binom{-n-j-1}{k-j}$$

$$= \binom{-1/2}{n}^{-1} \binom{-n-1}{j} \binom{n+1/2}{n-j} \qquad \text{(Vandermonde convolution [129, p.174])}$$

$$= (-1)^{j+n} (n+1/2) \frac{2^{2j+1} (n+j)!}{(2j+1)! (n-j)!} \tag{D.11}$$

Equivalent working for the α^{2j}/β term in equation D.10 gives a simplification,

$$\int_{-1}^{1} P_n(\mu) (\cosh\eta_0 - \mu)^{-3/2} \, d\mu = \sqrt{2} (n+1/2) \sum_{j=0}^{n} \frac{2^{2j+1} (n+j)!}{(2j+1)! (n-j)!} \left[\frac{\beta^{2j}(-1)^{j+n}}{\alpha} - \frac{\alpha^{2j}}{\beta} \right] \tag{D.12}$$

Note that using similar algebraic techniques on the 'multiple angle' hyperbolic functions leads to,

$$\cosh(n+1/2)\eta_0 = (n+1/2) \sum_{j=0}^{n} \frac{2^{2j+1}\,(n+j)!}{(2j+1)!\,(n-j)!} \left[\beta^{2j+1}(-1)^{j+n}\right] \qquad \text{(D.13a)}$$

$$\sinh(n+1/2)\eta_0 = (n+1/2) \sum_{j=0}^{n} \frac{2^{2j+1}\,(n+j)!}{(2j+1)!\,(n-j)!} \left[\alpha^{2j+1}\right] \qquad \text{(D.13b)}$$

This result simplifies equations D.9 and D.12 greatly, to obtain for $\eta_0 > 0$,

$$\int_{-1}^{1} P_n(\mu)\,(\cosh\eta_0-\mu)^{-3/2}\,d\mu = \frac{\sqrt{2}}{\alpha\beta}\left(\cosh(n+1/2)\eta_0 - \sinh(n+1/2)\eta_0\right) \qquad \text{(D.14a)}$$

$$\int_{-1}^{1} P_n(\mu)\,(\cosh\eta_0-\mu)^{-1/2}\,d\mu = \frac{\sqrt{2}}{n+1/2}\left(\cosh(n+1/2)\eta_0 - \sinh(n+1/2)\eta_0\right) \qquad \text{(D.14b)}$$

Although unnecessary for present consideration, the equivalent results for $\eta_0 < 0$ are,

$$\int_{-1}^{1} P_n(\mu)\,(\cosh\eta_0-\mu)^{-3/2}\,d\mu = -\frac{\sqrt{2}}{\alpha\beta}\left(\cosh(n+1/2)\eta_0 + \sinh(n+1/2)\eta_0\right) \qquad \text{(D.15a)}$$

$$\int_{-1}^{1} P_n(\mu)\,(\cosh\eta_0-\mu)^{-1/2}\,d\mu = \frac{\sqrt{2}}{n+1/2}\left(\cosh(n+1/2)\eta_0 + \sinh(n+1/2)\eta_0\right) \qquad \text{(D.15b)}$$

reminding ourselves that in equations D.14a and D.15a, $\alpha = \sinh(\eta_0/2)$, $\beta = \cosh(\eta_0/2)$.

APPENDIX E CODE STRUCTURES

The following sections list the essential computational structures used in our computer programs. Full programs are not included due to space considerations; neither are sections of code that provide limit checking and error trapping In each section a brief outline is given of the translation of theory and formulae to code, the essential parameters and variables used, and flow charts of the important code segments themselves.

The programming language used was a superset of FORTRAN 77 allowing the use of further control statements common in many structured languages (for example `DO...ENDDO` loops mimicking the use of `FOR` loops in ANSI PASCAL) [130]. The programs were compiled on an IBM 3090 mainframe computer, with associated vector processor. Compilation was performed with full automatic optimisation.

The random number generator used in the Monte Carlo routines is a standard NAG routine, G05CAF [120]. It is based on a multiplicative congruence method where a term N is iteratively updated by,

$$N := 13^{13} \times N \bmod 2^{59} \tag{E.1}$$

and a pseudo-random number $N/2^{59}$ returned. Analysis of data correlations within this pseudo-random set has been performed by Knuth [131]. The set repeats after 2^{57} iterations.

E.1 Monte Carlo Modelling of Tunnelling Junction Arrays

A tunnelling junction array with N junctions is considered. We are given the circuit parameters of the device, the biasing potentials, and the initial distribution of excess electrons on its electrodes. The core of the modelling process calculates the probability of any particular tunnelling event occurring in the device. Then the Monte Carlo portion of the process chooses one event based on these probabilities, and the time at which that event occurs. A controlling program iterates events, changing bias and collecting data as required to obtain macroscopic results. Each macroscopic 'experiment' requires a tailored controlling program.

Most computational effort is concentrated on obtaining the potential landscape of the system. From this, tunnelling probabilities are calculated from equation 4.11. In the general case, where each system capacitance is independent, the potential landscape is governed by equations 5.5,

$$-\zeta_i \phi_{i-1} + (\zeta_i+\zeta_{i+1}+\eta_{oi})\,\phi_i - \zeta_{i+1}\,\phi_{i+1} = \beta\, s_i \qquad (5.5)$$

where $\zeta_i = C_i/C$, $\eta_i = C_{oi}/C$ and $\beta = e/C$, with C the nominal average value of junction capacitance, C_i and C_{oi} the actual values of junction and grounding capacitance of junction i. s_i is the number of excess electrons at electrode i. It stores the soliton positions in the device.

As in any other system, the set of equations 5.5 must be solved for ϕ_i. We make use of a set of coefficients ν_i, which can be precalculated to save computation time in the main calculation loops. ν_i can be recursively defined by (where $\alpha_i = \zeta_i+\zeta_{i+1}+\eta_i$) ;

```
C      .. SET UP VECTORS OF USEFUL COEFFS FOR CALCULATION OF POTENTIALS  ..

      DO j = 0,(N-2)
        Nu(j)   = 0.0
        Nu(j+1) = 1.0
        DO I = j+2,N
          Nu(i) = Alpha(i-1)*Nu(i-1) - Zeta(i-1)**2*Nu(i-2)
        ENDDO
        Nu(j) = Nu(N)
      ENDDO
      Nu(N) = 0.0
```

Then all ϕ_i values can be obtained from the following;

$$\phi_o = V_L\,, \qquad \phi_N = V_R\,, \qquad \nu_N s_N = \phi_N/\beta$$

$$\phi_1 = \frac{1}{\nu_o}\left[\phi_o \nu_1 \zeta_1 + \beta \sum_{i=1}^{N} \nu_i s_i \zeta_i \zeta_{i-1}\right]$$

$$\phi_{i+1} = \frac{(\zeta_i+\zeta_{i+1}+\eta_i)\phi_i - \zeta_i\phi_{i-1} - \beta s_i}{\zeta_{i+1}} \qquad i > 0 \qquad (E.2)$$

The code for the main iterative loop is shown in flow chart form in figure E.1. It divides into four main sections. Firstly, the potential profile is calculated from the biasing potentials, the excess electron data, and the various coefficient arrays. Next, the work of testing every possible tunnelling event is carried out. s_i is updated as if the event had occurred, a partial potential profile is obtained, and the energy difference between initial and final states used to calculate Γ_j. This is repeated for both forwards and backwards tunnelling processes. Thirdly, the accumulated probability of tunnelling events is used to calculate the time for tunnelling, and finally the choice is made as to which event occurs.

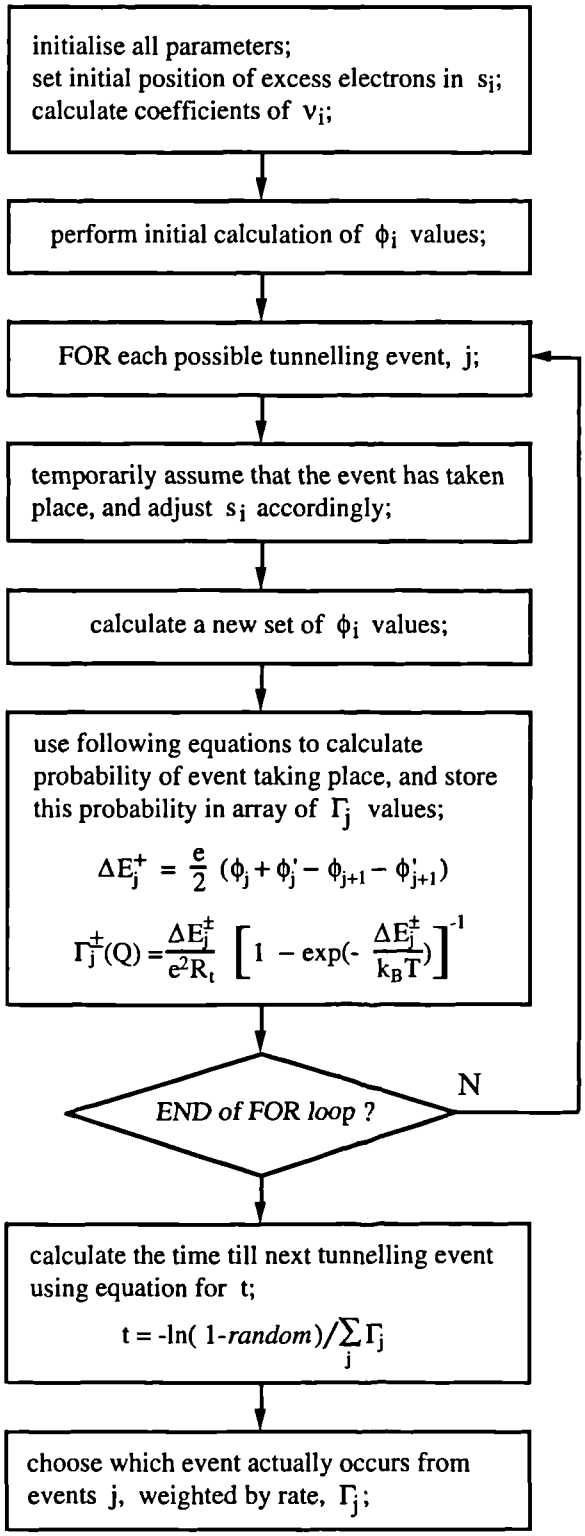


Fig E.1 Flow chart of the algorithm used to calculate one iteration of tunnelling events in a tunnelling junction array. Further sections of a modelling program extract necessary data from the array state and then cycle back to the initial ϕ_i calculation. 'random' is a random number [0,1) with constant distribution.

E.2 Monte Carlo Modelling of Turnstile Device

The ideas that govern the code structure for modelling the turnstile device are the same as for tunnelling junction arrays. The state of the device is characterised, and this data used to choose which tunnelling event will occur next. However, the form of code shows two extensions to these principles; both noted in the flow chart of fig. E.2.

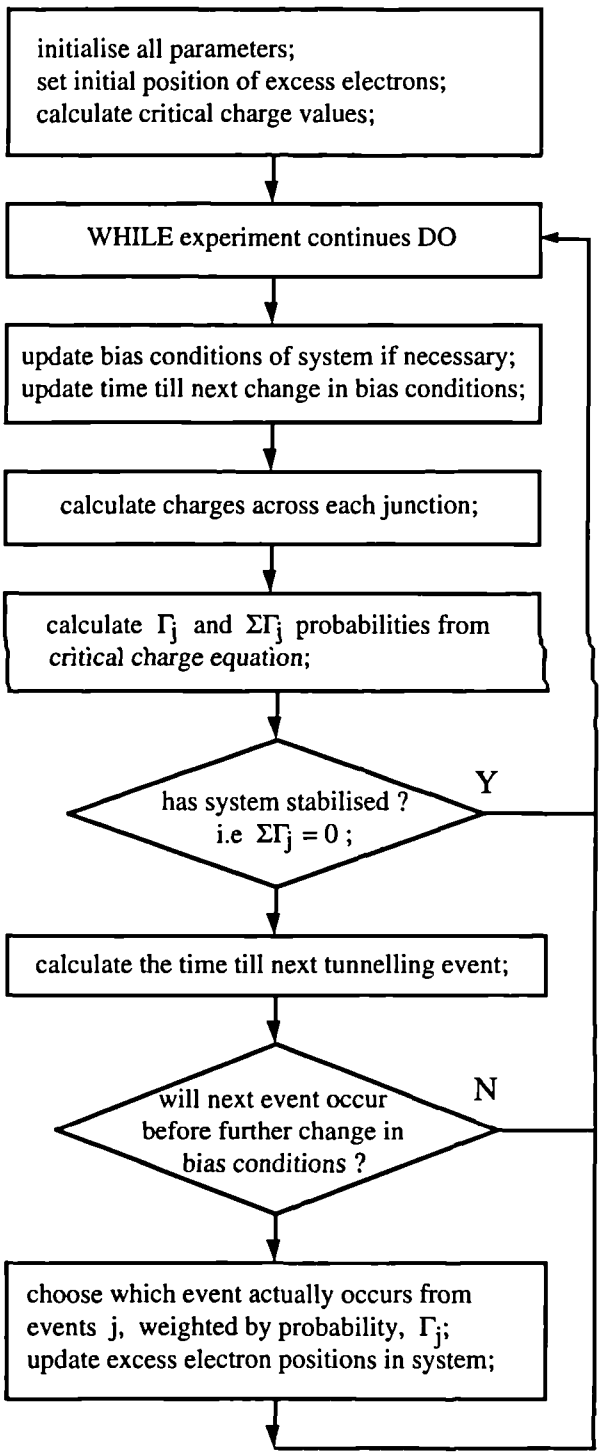


Fig E.2 Flow chart of the algorithm used to calculate multiple iterations of events and bias condition changes in a four-junction turnstile device. This code structure is only applicable for large discrete changes in bias conditions.

The first modification is a rudimentary consideration of non-static bias conditions. The method by which this is handled is easily seen from the flow chart diagram of modelling code structure.
The second modification is the introduction of *critical charges* as a systematic way of reducing computation in the main program loop. In the original algorithm, tunnelling junction array formulae were hand tuned so that as many coefficients as possible could be precalculated. This process is now automated by the critical charge concept of §5.2.4. Instead of calculating a potential landscape, the device is characterised by a charge landscape. These junction charges are compared with critical charges to obtain the tunnelling probabilities for each junction. Equations 5.25 and 4.11 are used. For the five junction turnstile, computation is also eased by manual expansion of the governing circuit equations. The equations used are 5.19 - 5.21.

E.3 General Network Solver

The algorithms which govern the operation of the general network solver are identical to those used to investigate the gated turnstile device. The work on the gated turnstile can be thought of as a specific example of such a solver, with governing formulae obtained by hand. To create a general solver therefore, we automate the two types of hand calculations required.
First is a routine that takes a network of junctions, capacitors and voltage sources, and calculates a Thévenin equivalent circuit for any junction i. The effective capacitance of this circuit is used to compute the critical charge for junction i. The method by which this charge is calculated, and the prerequisite Thévenin circuit obtained, are detailed in §5.2.4.

Secondly, instead of a bespoke analysis of the equations governing the charge profile of a device, a general solution is performed. This is based on solution of the matrix equation 5.28 which condenses the rules of charge continuity and Kirchoff's laws. The matrix equation is then solved by using toolbox routines provided by NAG [120].

We first note the data structures which define an equivalent circuit, then the routines that calculate critical charge values from this data, and finally the main modelling routine itself.

Data Structures :

The form of the equivalent circuit itself is defined by five arrays;

`Volts(elem)`	specifies the magnitude of the voltage sources.
`Elas(elem)`	initially contains the capacitance of both tunnelling and non-tunnelling junctions. Its components are then inverted so that elastances are stored.
`Conn(elem,loops)`	specifies which components are connected to which.
`Qcon(juns,qs)`	information on the electrodes which support excess electrons, and which junctions connect to them.
`Zcon(juns,zeros)`	junctions which directly connect to each other via only a voltage source (required to fully analyse charge conservation).

The size of these matrices are defined by the following (not necessarily independent) parameters of the system;

`elem`	the total number of circuit elements
`nodes`	the total number of circuit nodes
`loops`	the number of loops in the circuit net
`caps`	the number of capacitances (both tunnelling and non-tunnelling)
`pots`	the number of voltage sources
`juns`	the number of tunnelling junctions
`qs`	the number of nodes which may support excess electrons
`zeros`	the number of linear junction / voltage source / junction component strings

Section 5.4.2 shows an example of the definition of these data structures for a four-junction gated turnstile device. They contain all the required information needed to obtain the critical charges or charge profile of the system. Often `Qcon` is divided into its elastance and voltage segments (multiplied through by their respective parameter values) to form matrices `Econ` and `Vcon`. These simplify the formulation of governing equations.

Calculation of Critical Charges :

Figure E.3 shows the structure of code needed to obtain a critical charge value for one of the junctions in a purely capacitive equivalent circuit.

Firstly an impedance matrix, `Z(loops,loops)`, is derived from the connection matrix and component elastance values. Elementary row operations ensure that the rows containing the junction of interest are moved to the top. For small impedance matrices, further simplification may not be needed and an effective impedance may be calculated directly. For larger matrices an automated simplification process based on

the formula $Z_{eff} = A - BD^{-1}C$ is used. The impedance matrix is partitioned into two diagonal submatrices, A & D, and two off-diagonal submatrices B & C. Submatrix A is chosen to contain those rows and columns of z that deal with the junction of interest. Having obtained Z_{eff}, the value of $Q_{critical}$ for this junction is calculated from equation 5.25. The procedure shown in figure E.3 is then repeated for each junction in the circuit.

Again it should be noted that all error and limit checking (including that on the operation of NAG routines) is omitted from this discussion. In practice such checks are vital as errors in coding large circuit matrices are common.

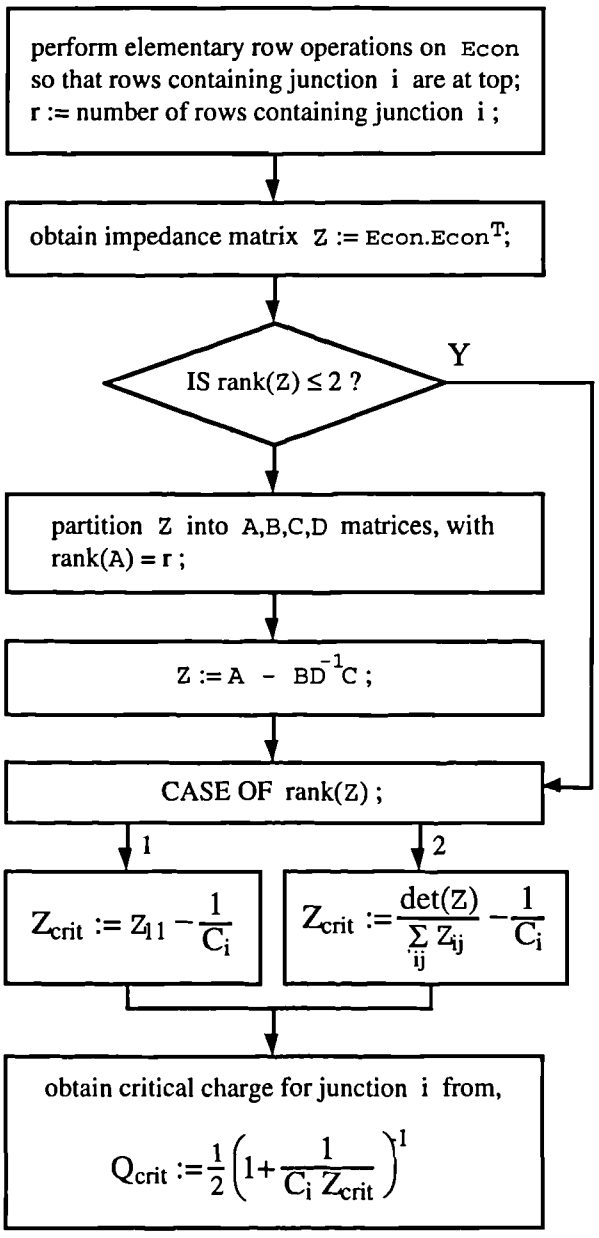


Fig E.3 Flow chart of the algorithm used to calculate critical charge values of a general network. Z,A,B,C,D and Econ are matrices, all other variables represent reals. The 'T' superscript indicates matrix transposition.

General Network Solver Modelling Routine :

The code for the general network solver is precisely that of figure E.2. The only changes from §2 are in the methods by which $\mathbf{q}_{crit}$ (the vector of critical charge values) and $\mathbf{q}$ (the vector of circuit charge values) are obtained. Critical charge values are computed above. In order to obtain the system charge profile equations 5.28 must be solved.

On considering equations 5.28 it can be seen that they can be merged into one matrix equation,

$$\mathbf{M}_{fixed} \times \mathbf{q} = \mathbf{V}_{variable} \qquad \text{(E.3)}$$

where $\mathbf{M}_{fixed}$ is an array of parameters dependent only on the structure of the device, and $\mathbf{V}_{variable}$ a vector of state values (excess electron numbers and bias voltages). Solution for $\mathbf{q}$ can be performed by toolbox routines.

The general procedure of the general network solver is therefore to initialise $\mathbf{M}_{fixed}$ as part of the initial parameters of figure E.2, along with the vector of critical charges. Then whenever the charge profile of the system need be calculated, $\mathbf{V}_{variable}$ is updated and equation E.3 solved to find $\mathbf{q}$. These extensions to the code structures of the gated turnstile modeller completely describe the general network solver.

APPENDIX F EFFECTIVE CAPACITANCE OF LADDER CIRCUITS

F.1 Effective Capacitance of a C/Co 'Ladder'

Wish to calculate the effective Thévenin capacitance C_{eff} of the circuit of figure F.1 for arbitrary n segments, with $\gamma = C_o/C$ and $f_n = C_{eff}/C$. Simple circuit theory gives,

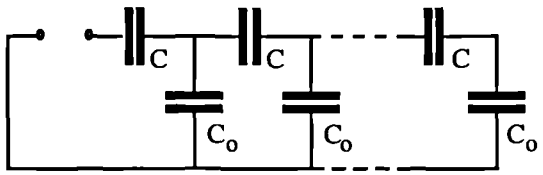


Fig F.1 Circuit schematic of a C/C_o ladder.

$$f_1 = \gamma + 1, \qquad f_n = \gamma + \frac{f_{n-1}}{1 + f_{n-1}}$$

as a recursive solution of f_n. The recursion can be eliminated to give f_n as the ratio of n and n-1 polynomials in γ,

$$f_n = \frac{\sum_{m=0}^{n} \binom{n+m}{2m} \gamma^m}{\sum_{m=0}^{n-1} \binom{n+m}{2m+1} \gamma^m} \qquad \text{(F.2)}$$

F.1 Effective Capacitance of a C/Cs/C 'Ladder'

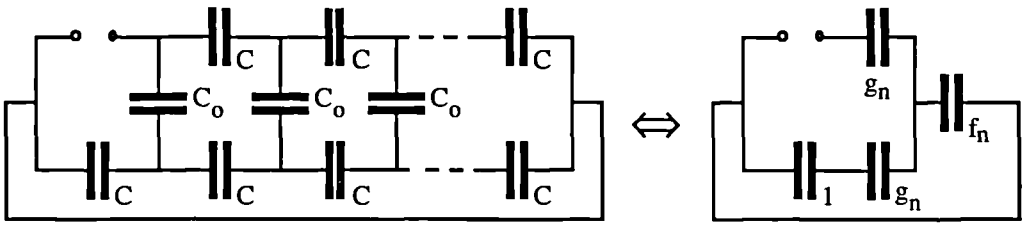


Fig F.2 Circuit schematic of a $C/C_s/C$ ladder. Such a circuit might act as a first order approximation to 2 capacitively linked tunnelling junction arrays.

Wish to calculate the capacitances f_n and g_n of figure F.2b. These can then be used to calculate the effective capacitance c_n of the circuit from,

$$c_n = \left(\frac{g_n}{1 + g_n} + f_n \right) || \, g_n \qquad \text{(F.3)}$$

where $||$ represents capacitors in parallel. As above, all capacitance is normalised to C. I.e $\gamma = C_s/C$. It is simple to obtain,

$$g_1 = 2\gamma + 1, \quad g_n = 2\gamma + \frac{g_{n-1}}{1+ g_{n-1}} \tag{F.4}$$

$$f_1 = \frac{2\gamma + 1}{\gamma}, \quad f_n = \frac{f_{n-1}\, g_{n-1}\, (g_{n-1} + 2\gamma(1+ g_{n-1}))}{(1+ g_{n-1})^2\, \gamma\, f_{n-1} + g_{n-1}^2 + 2\gamma\, g_{n-1}(1+ g_{n-1})} \tag{F.5}$$

and recursion can be eliminated to give,

$$g_n = \frac{\sum_{m=0}^{n} 2^m \binom{n+m}{2m} \gamma^m}{\sum_{m=0}^{n-1} 2^m \binom{n+m}{2m+1} \gamma^m} \tag{F.6}$$

$$f_n = \frac{\sum_{m=0}^{n} 2^m \binom{n+m}{2m} \gamma^m}{\gamma \sum_{m=0}^{n-1} \gamma^m \sum_{p=m}^{n-1} 2^m (p+1) \binom{p+m+1}{2m+1} \gamma^m} \tag{F.7}$$

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