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High Efficiency and High Frequency Resonant Tunneling Diode Sources

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A thesis submitted in fulfillment of the requirements for the degree of

Doctor of Philosophy

December 2019

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Abstract

Terahertz (THz) technology has been generating a lot of interest due to the numerous potential applications for systems working in this previously unexplored frequency range. THz radiation has unique properties suited for high capacity communication systems and non-invasive, non-ionizing properties that when coupled with a fairly good spatial resolution are unparalleled in its sensing capabilities for use in biomedical, industrial and security fields. However, in order to achieve this potential, effective and efficient ways of generating THz radiation are required. Devices which exhibit negative differential resistance (NDR) in their current-voltage (I – V) characteristics can be used for the generation of these radio frequency (RF) signals. Among them, the resonant tunneling diode (RTD) is considered to be one of the most promising solid-state sources for millimeter and submillimeter wave radiation, which can operate at room temperature.

However, the main limitations of RTD oscillators are producing high output power and increasing the DC-to-RF conversion efficiency. Although oscillation frequencies of up to 1.98 THz have been already reported, the output power is in the range of micro-Watts and conversion efficiencies are under 1 %. This thesis describes the systematic work done on the design, fabrication, and characterization of RTD-based oscillators in monolithic microwave/millimeter-wave integrated circuits (MMIC) that can produce high output power and have a high conversion efficiency at the same time.

At the device level, parasitic oscillations caused by the biasing line inductance when the diode is biased in the NDR region prevents accurate characterization and compromises the maximum RF power output. In order to stabilise the NDR devices, a common method is the use of a suitable resistor connected across the device, to make the differential resistance in the NDR region positive. However, this approach severely hinders the diode's performance in terms of DC-to-RF conversion efficiency.

In this work, a new DC bias decoupling circuit topology has been developed to enable accurate, direct measurements of the device's NDR characteristic and when implemented in an oscillator design provides over a 10-fold improvement in DC-to-RF conversion efficiency. The proposed method can be adapted for higher frequency and higher power devices and could have a major impact with regards to the adoption of RTD technology, especially for portable devices where power consumption must be taken into consideration.

RF and DC characterization of the device were used in the realization on an accurate large-signal model of the RTD. S-parameter measurements were used to determine an accurate small-signal model for the device's capacitance and inductance, while the extracted DC characteristics where used to replicate the *I-V* characteristics. The model is able to replicate the non-stable behavior of RTD devices when biased in the NDR region and the RF characteristics seen in oscillator circuits. It is expected that the developed model will serve in future optimization processes of RTD devices in millimeter and submillimeter wave applications.

Finally, a wireless data transmission link operating in the Ka-band (26.5 GHz – – 40 GHz) using two RTDs operating as a transmitter and receiver is presented in this thesis. Wireless error-free data transfer of up to 2 gigabits per second (Gbit/s) was achieved at a transmission distance of 15 cm.

In summary, this work makes important contributions to the accurate characterization, and modeling of RTDs and demonstrates the feasibility of this technology for use in future portable wireless communication systems and imaging setups.

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[2] **Cornescu, A. C.,** Wang, J., Al-Khalidi, A., Morariu, R. and Wasige, E., “I-V characteristics of a stabilized resonant tunneling diode,” *Compound Semiconductor Week (CSW) 2017*, Berlin, Germany, 14 – 18 May 2017.

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List of Symbols, Acronyms and Constants

Acronyms

- AC — Alternating Current
- ADS — Advanced Design System
- CAD — Computer Aid Design
- CMOS — Complementary Metal Oxide Semiconductor
- CPW — Coplanar Waveguide
- DBQW — Double Barrier Quantum Well
- DC — Direct Current
- DI — De-Ionised
- DUT — Device Under Test
- FIR — Far-InfraRed
- FOM — Figure of Merit
- Gbitps — Gigabits per second
- GHz — Gigahertz
- GSG — Ground Signal Ground
- HEMT — High Electron mobility Transistor
- ICP-CVD — Inductively Coupled Plasma Chemical Vapour Deposition
- IF — Intermediate Frequency
- IMPATT — Impact Ionization Transit Time
- IOT — Internet of Things
- IP — Internet Protocol
- ITU — International Telecommunications Union
- JWNC — James Watt Nanofabrication Centre
- LO — Local Oscillator
- LOR — Lift-off Resit
- MBE — Molecular Beam Epitaxy
- MMIC — Monolithic Microwave Integrated Circuit
- MIM — Metal-Insulator-Metal

- NDR Negative Differential Resistance
- PCA Photoconductive Antenna
- PDR Positive Differential Resistance
- PVCR Peak Valley Current Ration
- QCL Quantum Cascade Laser
- RF Radio Frequency
- RIE Reactive Ion Etching
- RTD Resonant Tunneling Diode
- SEM Scanning Electron Microscope
- SOLT Short-Open-Load-Thru
- S-parameters Scattering Parameters
- TCR Temperature Coefficient of Resistance
- THz Terahertz
- TLM Transmission Line Model / Method
- TUNNET Tunnel Injection Transit Time
- VCO Voltage Controlled Oscillator
- VIA Vertical Interconnect Access
- VNA Vector Network Analyser

Physical Constants

- c_0 $= 3 \times 10^8$ m / s Speed of Light in Free Space
- μ_0 $= 4\pi \times 10^{-7}$ H / m Vacuum Permeability
- ε_0 $= 8.85 \times 10^{-12}$ F / m Vacuum Permittivity
- h $= 4.136 \times 10^{-15}$ eVs Planck's Constant
- ħ $= 6.582 \times 10^{-15}$ eVs Reduced Planck's Constant
- e $= 1.6 \times 10^{-19}$ C Elementary Charge
- m_0 $= 9.11 \times 10^{-31}$ kg Electron Rest Mass

Chemical Symbols

- $(CH_3)_2CO$ Acetone
- Al Aluminium

- AlAs Aluminium Arsenide
- AlSb Aluminium Antimonide
- As Arsenic
- Au Gold
- C_3H_8O Propanol
- C_6H_6Cl Chlorobenzene
- C_7H_8 Toluene
- CH_3OH Methanol
- CO_2 Carbon Dioxide
- Ga Gallium
- GaAs Gallium Arsenide
- Ge Germanium
- H_2O_2 Hydrogen Peroxide
- H_3PO_4 Phosphoric Acid
- HCl Hydrogen Chloride
- In Indium
- InAlAs Indium Aluminium Arsenide
- InAs Indium Arsenide
- InGaAs Indium Gallium Arsenide
- InP Indium Phosphide
- Mo Molybdenum
- NH_4OH Ammonium Hydroxide
- NiCr Nickel Chrome
- Pd Palladium
- Si Silicon
- Si_3N_4 Silicon Nitride
- SiGe Silicon Germanium
- SiO_2 Silicon Dioxide
- Ti Titanium

Symbols

- C_n RTD Self-capacitance
- E_g Band Gap
- I_p Peak Current
- I_v Valley Current
- J Current Density
- m^* Electron Effective Mass
- V_p Peak Voltage
- V_v Valley Voltage
- ΔE_c Conduction Band Offset
- ε_r Dielectric Constant
- λ Wavelength

Chapter 1. Millimetre and Terahertz Wave Radiation

1.1 Introduction

Millimetre and terahertz wave technologies are fields that lie in between microwave electronics and photonics. Millimetre waves (mm waves) are located within the 30 GHz – 300 GHz frequency band, with wavelengths, λ, corresponding to 10 mm to 1 mm wavelength. Electromagnetic waves with λ between 1 mm and 100 μm are usually referred to as terahertz (THz) or sub-millimetre wave (sub-mm-wave) radiation. This corresponds to the frequency range between 300 GHz and 3 THz [1]-[3]. The electromagnetic spectrum is shown in Fig. 1.1.

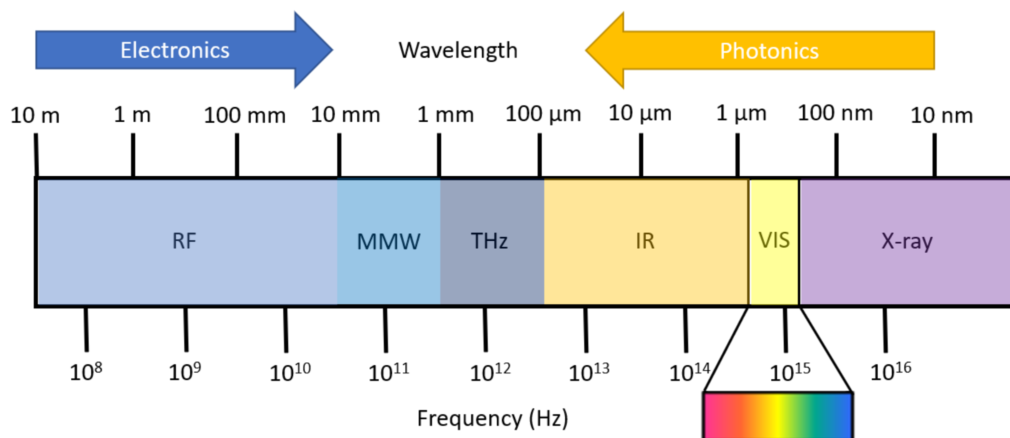

Figure 1.1: *Electromagnetic spectrum showing the millimetre and sub-millimetre radiation location between microwaves and infrared spectrum.*

In nature, mm-wave and sub-mm-wave emissions occur from black body radiations with temperatures between 14 K – 140 K, well below the ambient background temperature on Earth [1]. The results from the NASA Diffuse Infrared Background Experiment (DIRBE), show that approximately one-half of the total luminosity and 98% of the number of photons emitted since the Big Bang fall into the millimetre and sub-millimetre frequency range [4].

The amount of energy carried by a single photon is directly proportional to the photon's electromagnetic frequency, and equivalently, inversely proportional to the wavelength. The photon energy can be calculated using Eq. 1.1

$$E = \frac{hc}{\lambda} \tag{1.1}$$

where h is Planks constant, c represents the speed of light and λ is the wavelength of the radiation. For the frequency span 30 GHz – 3 THz, the corresponding photon energy level ranges from 0.12 meV – 12.4 meV. This energy level is well below the range of ionising radiation level (10 eV), as they do not contain the amount of energy needed to displace an electron from an atom or molecule, in contrast with X-rays which have enough energy to strip electrons from an atom and therefore causing radiation damage.

The mm waves, more relevant to the current work, present different atmosphere attenuation rates at different frequencies. As shown in Fig. 1.2, the electromagnetic waves with frequencies up to and including microwave are generally unaffected by atmospheric effects, making them suitable for long-range radio communications. However, millimetre and terahertz waves suffer from attenuation caused by rain and gas molecules, making them unsuitable for long-distance transmission [5].

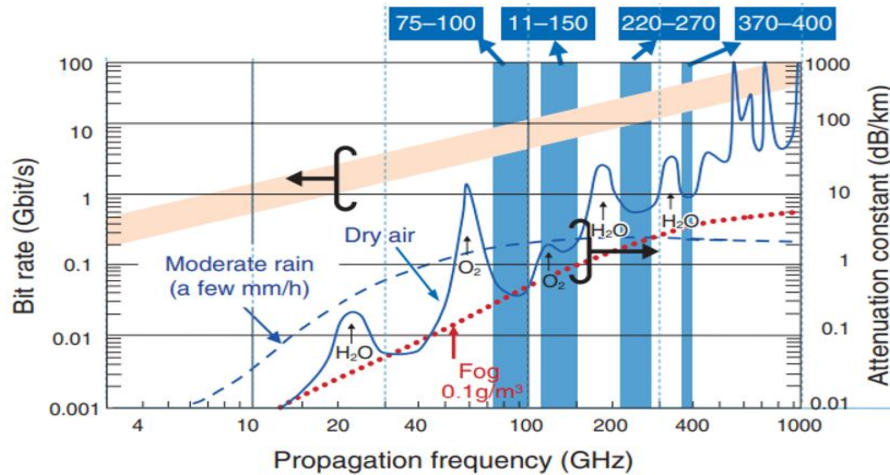

Figure 1.2: *Atmospheric attenuation and expected data transfer rate of different propagation frequencies . Adapted from [5].*

Radiation in these frequency bands is of great interest as it offers many different applications such as ultra-fast wireless communication for short-range, high-capacity, line-of-sight data transfer [6], security imaging, which exploits the properties of terahertz wave to penetrate many non-conducting materials to identify hidden objects [7][8], and non-invasive highly sensitive medical imaging due to the non-ionizing nature of the radiation [9].

The current cellular network technologies operate at frequencies between 800 MHz to 2.6 GHz. The International Telecommunication Union (ITU), the organization that coordinates the shared global use of the radio spectrum, published the WRC-19 document [10], which states that 24-86 GHz frequency bands will be used for the next 5G technologies, with a particular focus on the spectrum range 26.5 to 29.5 GHz, which many countries have already adapted while waiting for the specifications to be completed.

Despite of on-going research in millimetre and terahertz waves, the lack of reliable, compact, high power sources, which can operate at room temperature, has resulted in this being one of the least used regions of the electromagnetic spectrum. This region is also referred in literature as the "THz gap" [11]-[13] because there had been no effective way of generation and detection of THz signals. This is illustrated in the output power versus frequency graph of various electronic and photonic sources shown in Fig. 1.3.

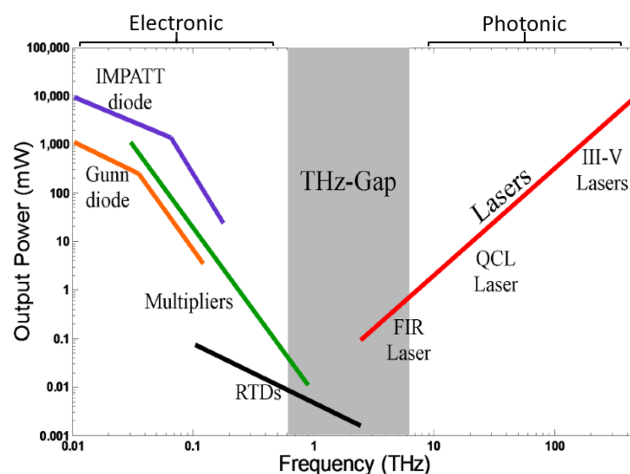

Figure 1.3: *Semiconductor devices showing the RF power output decreasing towards the THz-gap. Adapted from [11].*

1.2 THz Applications

New advances in different technologies have made the previously unused portion of the electromagnetic spectrum accessible to a wide variety of applications. This section therefore tries to provide a brief overview of the possible applications of millimetre and terahertz waves. The first major commercial application area is in millimetre and sub-millimetre wave communications. It is foreseen that the global internet protocol (IP) traffic will increase threefold in 2022 when compared to that of 2017 and reach about 400 exabytes (EB) per month [14]. Most notably the traffic from wireless and mobile devices account for 71% of the total traffic, driven largely by the popularity of content-based applications like YouTube and Netflix, as well as the expansion of Internet of Things (IoT) devices, allowing in principle any object to be networked wirelessly [15]-[17].

The evolution of the radio frequency (RF) spectrum used in mobile networks (from 1G analog cellular networks to high speed, internet protocol based 4G networks) has allowed for larger communication bandwidths and/or tailoring the employed technology to the specific link requirements. As such as higher frequencies are opening up, the capacity of wireless networks will extend beyond the few gigabits per second (Gbit/s) into the range of hundreds of Gbit/s [18][19]. The RF spectrum and mobile network band allocations are presented in Fig. 1.4 [20].

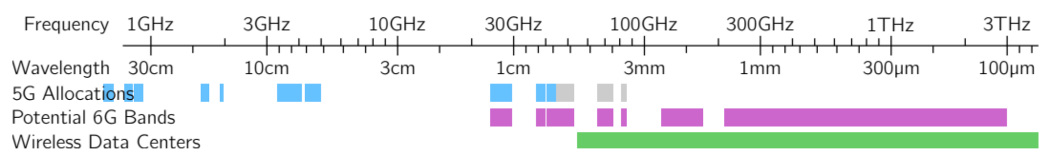

Figure 1.4: *Electromagnetic spectrum from microwave to the end of the THz region, showing the allocations for 5G, 6G and spectrum unification for wireless data centres. Adapted from [20].*

As data volumes grow substantially so too data centres need to evolve and develop new hybrid architectures based on wireless and mobile technology to attain higher bandwidth, lower latency and higher fault tolerance. The total energy consumption of data centres worldwide was estimated at about 270 TWh in 2012, which represented

about 2% of the global power consumption [21], with a significant portion of the power consumed attributed to the air-conditioning of the equipment. In the front section of a data centre cabinet there are several tens of metres of category 6 ethernet cables connecting multiple servers together [22]. This cabling substantially impedes the proper airflow and increases the cooling energy cost. Furthermore, the wired networks entail high wiring cost, suffer from performance bottlenecks and have a low fault tolerance. Mobile data centres can solve these issues by replacing hundreds of meters of cable connections with mm-wave wireless connections both intra- and inter-rack. Fig. 1.5 depicts a hybrid data centre with ad-hoc point to point wireless connectivity to help solve hotspots/bottlenecks and allow reconfigurability.

Figure 1.5: *Hybrid wired / wireless data centre with wireless nodes connection between the server racks. Adapted from [20].*

Moreover, spectrum regulations can be somewhat relaxed when compared to outdoor applications allowing for spectrum unification, with more than three decades of continuous electromagnetic spectrum (60 GHz – 3 THz) for usage [20]. Key elements for opening the new opportunities in communication are technical performance and cost. Therefore, a high performance, reliable and high yield monolithic microwave integrated circuit (MMIC) process needs to be available.

Another possible application stems from the fact that THz radiation is characterized by its low photon energy, which would not cause detrimental photoionization in organic tissue. As such the technology opens a multitude of non-invasive applications in the biomedical field. In [23] the authors make direct measurements of the water content of the cornea, made possible by exploiting the high sensitivity of terahertz frequencies to water content, which can be used to assess the onset and evolution of

diseases which affect the hydration of the eye such as dystrophies, degenerations, injuries and corneal graft rejection and can be helpful in evaluating contact lenses and eye drops in order to preserve the health hydration balance in the cornea.

In oral healthcare X-rays only reveal tooth decay at relatively late stages, when drilling and filling is the only method available to stop the process. Terahertz imaging can distinguish between the different types of tissue in a human tooth; detect carriers at an early stage in the enamel and dentine layers and monitor demineralization spots in the tooth. In [24] the authors used frequencies between 200 GHz and 1.5 THz where the contrast was associated with changes of refractive indexes. If the decay can be detected early enough it is possible to reverse the process without the need for drilling by using either fissure sealing or remineralization [25].

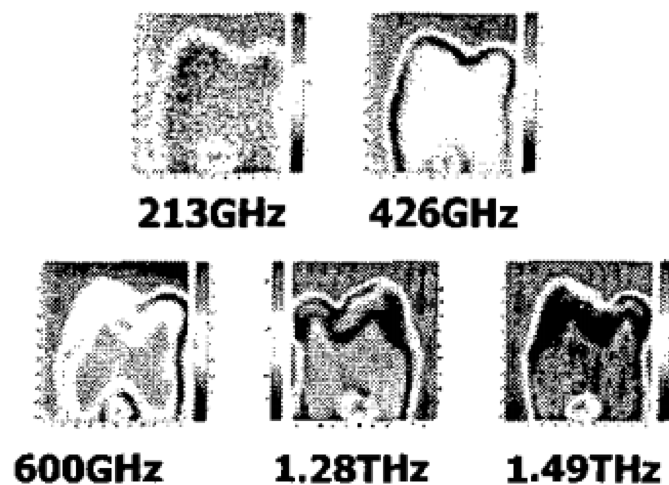

Figure 1.6: *Transmission image of a tooth showing the contrast at several frequencies in the mm-wave and terahertz range. Adapted from [24].*

Intensive research is currently being carried out on intrinsic contrast reflection imaging techniques to differentiate cancerous and healthy tissue using THz radiation [26]-[29]. The main difficulty that limits its application is the penetration depth of THz radiation into water-abundant specimens, however it can be overcome by using several techniques such as freezing [26][27] and the use of penetration enhancing gels [30].

Another important property of THz radiation is that it can penetrate many dielectric materials such as plastic, wood, paper and semiconductors, which makes THz waves a valuable tool in non-destructive detection fields such as security where they can be used in the detection and identification of concealed prohibited items and/or explosives.

International customs and border security agencies have traditionally used screening technologies based on X-rays to inspect baggage, vehicles, mail and cargo for illicit goods. However, pedestrian based smuggling of items such as narcotics and weapons has largely been neglected due to the lack of viable solutions. Among promising candidates is a full body passive millimetre-wave security screening portal such as the one developed by Trex Enterprises working at frequencies between 75.5 GHz to 93.5 GHz [31]. The system requires 48 seconds of scan time due to its limited number of detectors and use of mechanical scanning. An image collected with the system showing concealed objects (black contrast) against the emitted body heat (white) is shown in Fig. 1.7.

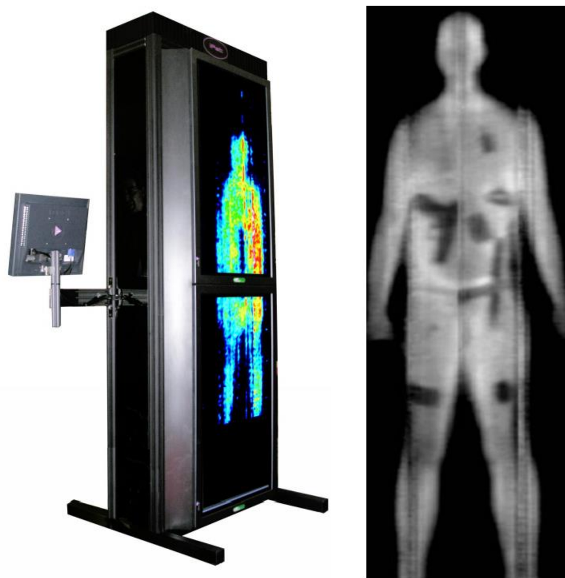

Figure 1.7: *Passive full body millimetre-wave security screening portal developed by Trex Enterprises working between 75.5 GHz to 93.5 GHz. Adapted from [31].*

Since the properties of materials are frequency dependent, the transmission/absorptivity, emissivity, reflectivity and scattering of the object of interest all change with respect to frequency. In [32] the authors showed how multi-spectral THz imaging can be used to combine images taken at different frequencies in order to enhance the contrast and spatial resolution of the final processed image. The Safe VISITOR: Visible, Infrared and Terahertz Object Recognition project uses the 350 GHz frequency range to define and detect objects from 5 m distance and resolve them to 256 shades of grey [33].

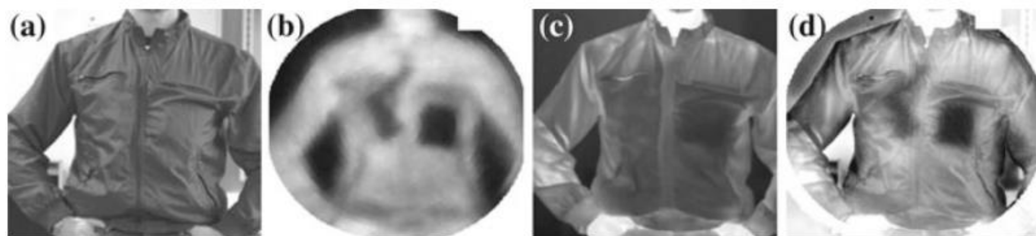

Figure 1.8: *Image fusion from Safe VISITOR project. (a) visible image, (b) THz image at 350 GHz, (c) Infrared image, (d) final fused image. Adapted from* [33].

1.3 THz Sources

The two main sources for terahertz radiation are electronic, which operate at the lower frequency end of the spectrum and photonic, operating at the higher frequency end. There are many candidates for electronic THz sources such as tunnel transit-time (TUNNET) diodes, impact ionization avalanche transit-time (IMPATT) diodes, Gunn diodes, resonant tunneling diodes (RTDs) and CMOS or III-V semiconductor frequency multipliers. Among them, the RTD has the highest reported oscillation frequency of 1.98 THz [34][35]. The most common photonic sources are terahertz photoconductive antennas (THz-PCAs) and terahertz semiconductor lasers, such as far-infrared (FIR) and quantum cascade lasers (QCL).

1.3.1 Electronic Sources

Gunn diodes are two-terminal devices which exhibit negative differential resistance (NDR), and when coupled to a suitable resonator, are able to generate RF power. Typically, the Gunn diode is made of a uniformly doped n-type III-V material, such as gallium arsenide (GaAs) or indium phosphide (InP) sandwiched between heavily doped regions at each end (Fig. 1.9 (a)). In these types of devices, the lowest conduction band profile presents distinct valleys, labelled Γ and L, as shown in Fig. 1.9 (b) [36].

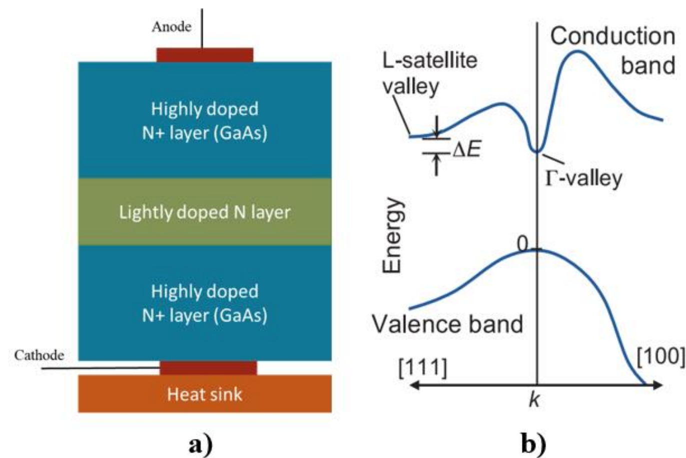

Figure 1.9: *Operating principle of Gunn diodes (a) Gunn diode structure, (b) conduction and valence band profile of Gunn diode. Adapted from [36].*

When the electrons reside in the lower Γ-valley, they exhibit very high mobility and a small effective mass, whereas in the L-valley the effective mass is large, and the mobility is low. The valleys are separated by a small energy gap ΔE. When sufficient bias voltage is applied, electrons gain enough energy to be transferred from the Γ-valley to the L-valley, where due to their increased effective mass the electrons have a lower drift velocity and the current decreases with bias. Gunn diodes are conventionally implemented in vertical device structures and are available in a number of commercial and industrial applications such as radar [37] and imaging [38].

A planar Gunn diode operating at 78.9 GHz was reported in [39] with 24.7 mW output power and 2.5% conversion efficiency. Fundamental oscillation frequencies of 100

GHz - 150 GHz with very high output power (300 mW – 100 mW) were achieved with devices mounted on diamond heat sinks [40] in a dual cavity power combining circuit as shown in Fig. 1.10. The authors later reported second harmonic oscillators with 4.8 mW output power at 282 GHz [41]. The efficiency of such oscillators is quite low at around 0.2%.

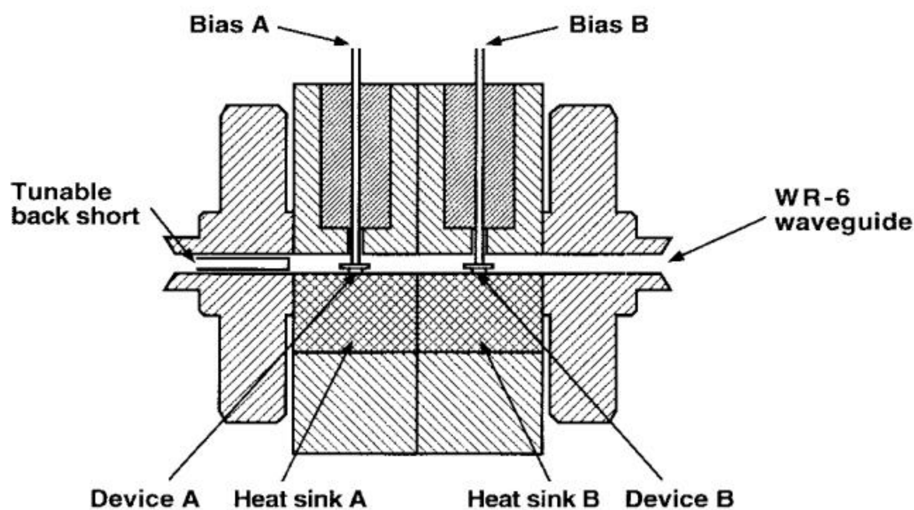

Figure 1.10: *Dual cavity power combining circuit using Gunn diodes mounted on diamond heatsinks. Adapted from [40].*

Impact ionization avalanche transit time diodes or IMPATT diodes in their basic form are based on a reverse-biased p-n junction and an intrinsic (high-resistivity) drift layer. When a sufficiently high reverse bias voltage is applied across the junction, avalanche breakdown occurs, resulting in a large number of carriers in the avalanche region. The negative differential resistance (NDR) characteristic of an IMPATT diode is produced by a combination of impact avalanche breakdown and charge-carrier transit time effects. Inside the diode the current lags the voltage by 90 degrees, known as the injection delay. The length of the diode can then be tailored so that the transit time delay results in a further 90 degrees phase lag and therefore the NDR is formed. An external resonant circuit can then be connected to the diode in order to sustain the oscillations. The basic structure of an IMPATT diode is shown in Fig. 1.11.

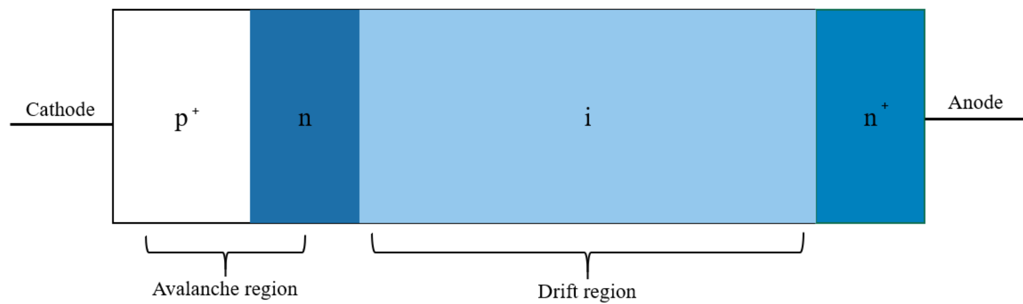

Figure 1.11: *IMPATT diode structure. When a sufficiently high negative voltage is applied, avalanche breakdown occurs in the p^+- n region resulting in a large number of carriers. The phase lag is controlled by the width of the drift region.*

The main advantage of the IMPATT diode is its high RF power capability. IMPATT diode oscillators have been reported with fundamental frequencies up to 217 GHz in continuous wave mode, with an output power of 1 W implemented in rectangular waveguide technology [42]. Monolithically integrated IMPATT diodes operating at 82 GHz with 14.6 mW output power have been reported in [43], with 4.3% conversion efficiency.

The main disadvantage of the IMPATT diode is that the avalanche breakdown process is noisy, making the oscillators susceptible to high phase noise [36]. A variation of the IMPATT diode is the tunnel injection transit time or TUNNETT diode, where the avalanche region of the IMPATT diode is changed to a highly doped, narrow, $p^{++}n^{+}$ junction that changes the breakdown mechanism from avalanche to tunnel injection. Compared with the IMPATT diode, the TUNNETT exhibits very low noise and high operation frequency at the cost of output power. TUNNET diodes have been developed with fundamental frequencies at 655 GHz with 0.8 nW output power and 0.2 nW at 701 GHz [44][45].

Frequency multiplication is the most common approach for generating THz radiation. A non-linear element, which is usually a Schottky diode because of their low self-capacitance and very high switching rate, implemented in CMOS or III-V semiconductor technologies is used to generate harmonics of an input signal.

Multiplier chains with cascaded frequency doublers and triplers are used to upconvert signals from the GHz frequency range up to THz frequencies.

However, the main disadvantage of multipliers chains is that they require high power input signals, have low power generation capability and conversion efficiency. To date the highest reported oscillation frequency is 2.55 THz with an output power of 0.1 μW and 0.002 % conversion efficiency [46].

1.3.2 Photonic Sources

The photoconductive antenna (PCA), consists of a low temperature grown GaAs or InGaAs film covered by two dc-biased electrodes that form an antenna. An ultrashort optical pulse from a femtosecond laser is focused on the gap between the electrodes. The optical pulses generate free electrons, which are accelerated by the electric field formed at the interface between the photoconductor and the antenna electrodes before becoming trapped in the semiconductor. If the process occurs at sub-picosecond timescale the resulting impulse current is at THz frequencies [47]. The operating principle is shown in Fig. 1.12.

However, since the output of such a system is not a continuous wave THz radiation, they are most commonly used in spectroscopy applications for material characterization. The PCA has been extensively studied and many different structures have been presented, such as the THz dipole antenna [48], Yagi–Uda antenna [49], spiral-type antenna [50], and butterfly-shaped antenna [51], with various degrees of radiation efficiency.

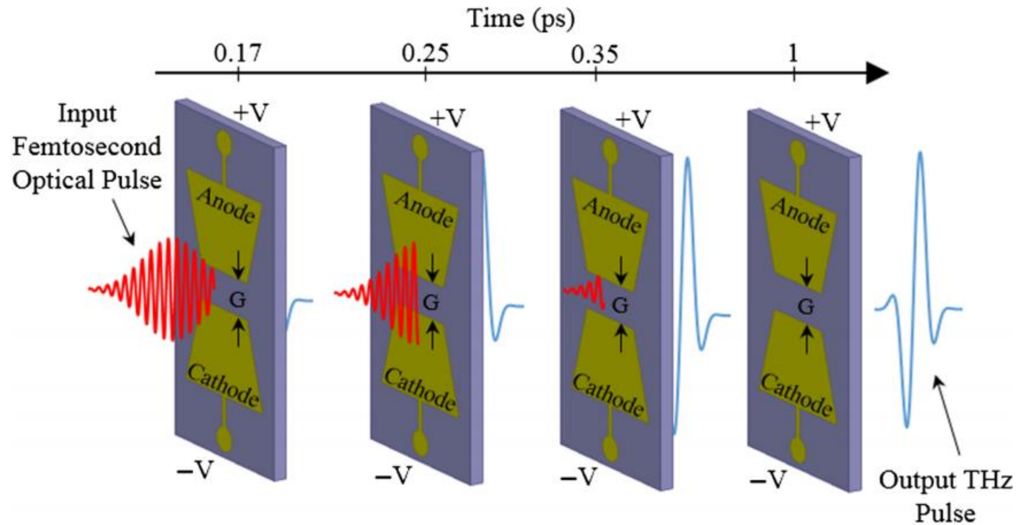

Figure 1.12: *Photoconductive antenna operating principle. A femtosecond laser is focused at the gap between the two electrodes generating free carriers, which are then accelerated by the bias voltage across the gap. Adapted from [47].*

While most lasers are located at the high end of the THz range, several laser devices have been developed to bridge the THz gap, such as far-infrared gas lasers (FIR) and quantum cascade lasers (QCL). In FIR lasers the THz emission originates from transitions between rotational states of gas molecules such as methanol (CH_3OH), which are stimulated by an external carbon dioxide (CO_2) laser [52][53]. High output power of 100 mW has been reported at a frequency of 2.5 THz for such a system [54]. QCL lasers are semiconductor heterostructures capable of emitting continuous wave THz radiation by exploiting transitions between conduction band states [55]. The lowest published frequency for QCL is 2.1 THz with 1.2 mW power in continuous-wave mode [56]. However, both systems are bulky and QCLs require cryogenic cooling to operate, making them unusable outside the laboratory environment.

1.4 The Resonant Tunneling Diode

1.4.1 Historical Perspective

In 1958, a Japanese PhD research student named Leo Esaki reported at the International Conference on Solid State Physics in Brussels a new type of diode based on the quantum-mechanical tunneling effect, which exhibited a region of negative differential resistance [57]. In 1973 Esaki received the Nobel Prize in physics for the pioneering work done in the first experimental demonstration of electron tunneling in semiconductor materials [58]. The tunnel diode was made with a very highly doped (10^{19} cm^{-3}) germanium p-n junction [59]. The operation principle of the tunnel diode is shown in Fig. 1.13.

At zero and low forward bias condition, shown in Fig. 1.13 (a) the states in the conduction band of the n-type doped side are filled with electrons resulting in the Fermi level (E_{Fn}) to move up and into the conduction band. Likewise, the states in the valence band on the p-type material are not filled with electrons, and as a result the Fermi level (E_{Fp}) goes down into the valence band. When a forward bias is applied, a number of electrons will have sufficient energy to tunnel through the barrier between the conduction band of the n-type to the valence band of the p-type material. The current will continue to increase with forward bias until the Fermi level E_{Fn} aligns with the p-type material valence band energy level shown in Fig. 1.13 (b), where a peak current value (I_p) is reached, at which the bias voltage is called peak voltage (V_p). When the bias voltage is increased beyond V_p, i.e. Fig. 1.13 (c), the tunneling current begins to drop rapidly as the bands between both sides become mis-aligned and the tunneling probability decreases until the valley voltage is reached (V_v) with valley current (I_v). A further increase in forward bias beyond the V_v point, as shown in Fig. 1.13 (d), results into conduction of carriers through diffusion as a normal p-n diode.

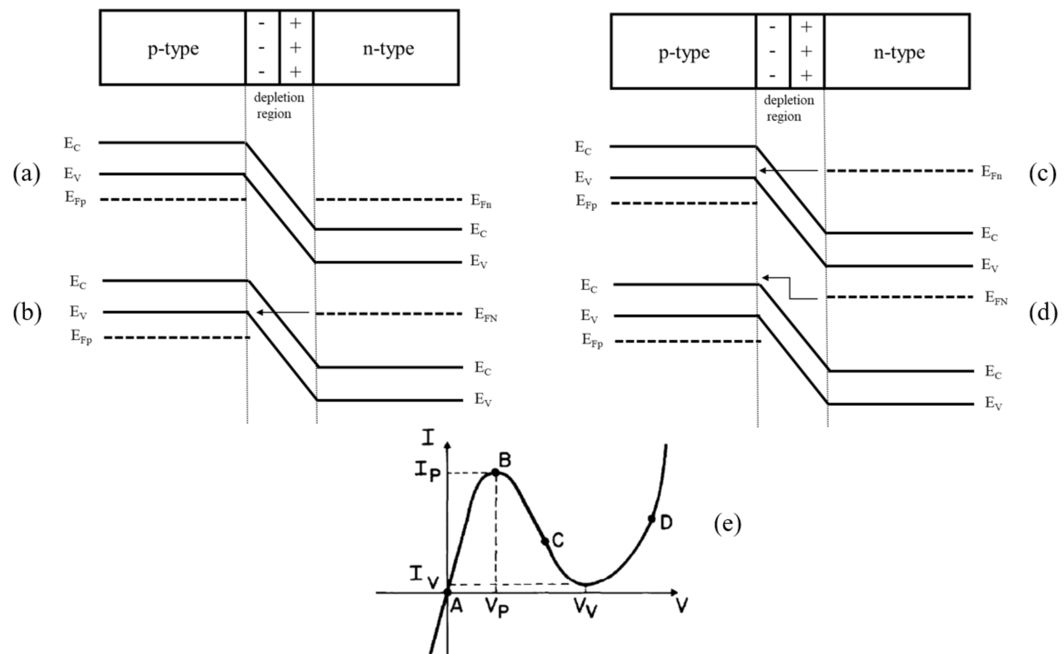

Figure 1.13: *Energy band diagram of a tunnel diode and its I-V characteristic. (a) Tunnel diode at zero bias, (b) band diagram at the peak voltage, (c) band diagram at the valley voltage, (d) band diagram at the second positive differential region, (e) I-V characteristic of tunnel diode at each biasing point.*

The Esaki tunnel diode was employed in high frequency amplifiers, logic circuits and oscillator applications, as early transistors did not operate well at frequencies of several GHz [60]. However, their inherently high specific capacitance restricted their use at higher frequencies, i.e. millimetre wave frequencies and above.

A new tunneling phenomenon was reported by Tsu and Esaki in 1973 [61] while they were exploring the properties of superlattices in terms of electrical transportation. This theoretically predicted behaviour showed electrons tunneling inside a double barrier quantum well (DBQW) in the form of a thin gallium arsenide (GaAs) well sandwiched between two aluminium gallium arsenide (AlGaAs) barriers. A year later, the team demonstrated a practical quantum barrier device, currently known as the resonant tunneling diode or RTD [62].

1.4.2 Operational Principle of RTD

The operating principle of the resonant tunneling diode (RTD) can be illustrated with the help of the conduction band diagram of the double barrier structure at different bias voltages with the corresponding *I-V* characteristics shown in Fig. 1.14. The quantum well in its most basic form consists of a layer of narrow-gap material sandwiched between two large-gap layers. The resulting conduction band profile resembles a square well whose width is dictated by the thickness of the narrow gap material and depth is controlled by the conduction band discontinuity between the barrier and well material. For electrons trapped inside the well, the motion of electrons is quantized in discrete energy states called resonant energy levels. If no voltage is applied, then the fermi level of the emitter E_{FE} and the fermi level of the collector are aligned below the resonant energy levels E_{r1} and E_{r2} as shown in Fig. 1.14 (a). In this case, no current will flow from the emitter to the collector due to thermal equilibrium.

When the bias voltage increases from zero, the conduction band profile of the DBQW structure shifts as shown in Fig. 1.14 (b). The bias voltage induces an electric field from the emitter to the collector and electrons obtain kinetic energy, and thus the probability of electrons to tunnel through the barrier increases in accordance with the bias level. This corresponds with the first positive differential resistance (PDR) region on the device's *I-V* characteristic. By further increasing the bias voltage the emitter conduction band reaches the resonant energy state, shown in Fig. 1.14 (c), where the probability of tunneling through the barrier is unity. This corresponds to the voltage peak point (V_p) and current peak (I_p) in the *I-V* characteristic.

Increasing the potential beyond V_p the resonant energy level and the conduction band energy level become mis-aligned and the probability of electrons to tunnel through drops rapidly as shown in Fig. 1.14 (d). This will correspond to the negative differential region of the diode, where V_v is the valley voltage and I_v is the valley current. Further increasing the applied bias voltage, the electrons acquire enough kinetic and thermal energy to go over the barrier and the current rises again with bias voltage, Fig. 1.14 (e).

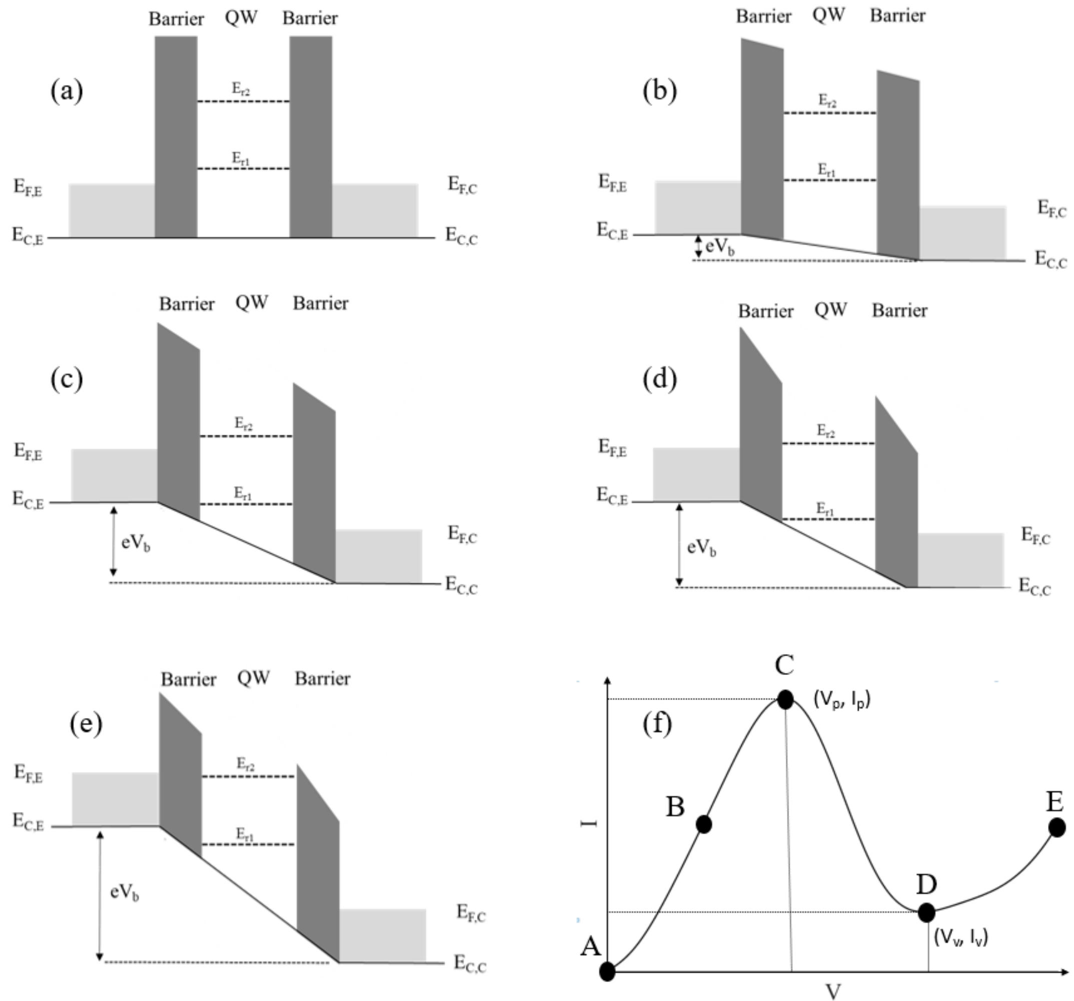

Figure 1.14: *Energy band diagram of a resonant tunneling diode (RTD) and its I-V characteristic. (a) RTD at zero bias, no current flows due to thermal equilibrium, (b) a small bias voltage is applied increasing the probability of electrons to tunnel through the barrier, (c) band diagram when the conduction band aligns with the resonant energy state* E_{r1} *and the transmission probability is at unity, (d) band diagram when the conduction band and the resonant energy state become misaligned and the current drops rapidly, (e) at a high enough bias voltage the current starts increasing again due to thermal emission, having enough energy to go over the barrier, (f) the I-V characteristic of the RTD at each biasing condition.*

From the *I-V* characteristics of an RTD device, different key parameters can be extracted to estimate the device performance. The figures of merit (FOM) of an RTD include the peak-to-valley voltage difference ($\Delta V = V_v - V_p$), the peak-to-valley current difference ($\Delta I = I_p - I_v$), and the peak-to-valley current ratio (PVCR = $\frac{I_p}{I_v}$). The parameters ΔV and ΔI are used to estimate the maximum RF power that an RTD-based oscillator can deliver to the load, which is given by $P_{max} = \frac{3}{16}\Delta I \Delta V$ [63]. A large PVCR maximises the dynamic range of the device. The valley current can often be associated with thermionic emission through higher resonant states or above the barrier, scattering effects and tunneling via X and L states [64].

1.4.3 RTD Material Systems

RTD devices are usually realized using III-V semiconductor materials [65]-[67], that possess a small effective electron mass (m^*) and have a high electron mobility, which leads to a high current density (J_p). Furthermore, the materials have a high conduction band offset which improves the peak voltage-current ratio (PVCR) by suppressing thermal current [68]. The typical III-V materials used to realise RTDs are gallium arsenide / aluminium gallium arsenide (GaAs/AlGaAs), indium arsenide / aluminium antimonide (InAs/AlSb) and indium gallium arsenide / aluminium arsenide (InGaAs/AlAs). In addition, silicon-based RTDs such as silicon / silicon germanium (Si/SiGe) are also being investigated due to the potential integration of RTDs with silicon technologies.

The parameters of the RTD material systems are summarized in Table 1.1, where the effective electron mass is denoted with m^*, m_o represents the electron rest mass ($m_o = 9.11 \times 10^{-31}$ kg), the band gap is denoted with E_g, relative dielectric constant (ε_r) and conduction band offset (ΔE_c) [69].

Table 1.1: *III-V RTD material parameters at room temperature*

Material	**m^***	**E_g (eV)**	**ε_r**	**ΔE_c (eV)**
GaAs AlAs	$0.067m_o$ $0.1m_o$	1.42 2.16	12.9 10.1	0.28
$In_{0.53}Ga_{0.47}As$ AlAs	$0.042m_o$ $0.1m_o$	0.71 2.16	12.9 10.1	0.65
InAs AlSb	$0.027m_o$ $0.12m_o$	0.36 1.61	14.6 12.04	1.35
$In_xGa_{1-x}As$	$(0.067+0.083x)$ m_o	$1.424+1.247x$	$12.9-2.84x$	N/A
$In_{0.48}In_{0.52}As$	$0.084m_o$	$In_{0.53}Ga_{0.47}As$	12.45	N/A

The GaAs quantum well with $Al_xGa_{1-x}As$ barriers was the first demonstrated resonant tunneling material system [70] and, remains an important system for high-speed RTDs due to the simple growing procedure [71]. By changing the composition (mole fraction x) a PVCR = 3.9 at room temperature with $J_p = 7.7$ kA/cm^2 was reported in [65].

The InAs/AlSb material system offers several advantages when compared to GaAs/AlGaAs, such as low effective mass and high conduction band offset. Secondly, using InAs instead of GaAs lowers the series contact resistance, as nearly ideal ohmic contacts can be formed to InAs, where the Fermi level is pinned in the conduction band [72]. However, the system can suffer from impact ionization due to the low bang gap of InAs ($E_g = 0.36$ eV). When a high electric field is applied, an electron with energy slightly larger than the band gap could collide with an electron in the valence band and knock it out into the conduction band. The number of current carriers will therefore multiply, and the current will begin to increase rapidly due to carrier multiplication, a process referred to as avalanche breakdown [73].

The most popular, and the one used in this work is the InGaAs/AlAs material system, as it can offer a very high PVCR and high peak to valley current density ($\Delta J = J_p - J_v$). In [74] a PVCR of 30 was reported where an InAs sub-well and AlAs barriers was used. The InAs sub-well enabled a low resonance energy, provided a large separation between the resonant levels, and greatly reduced alloy scattering when compared to an InGaAs well. A comparison between the different RTD material systems can be seen in Fig. 1.15.

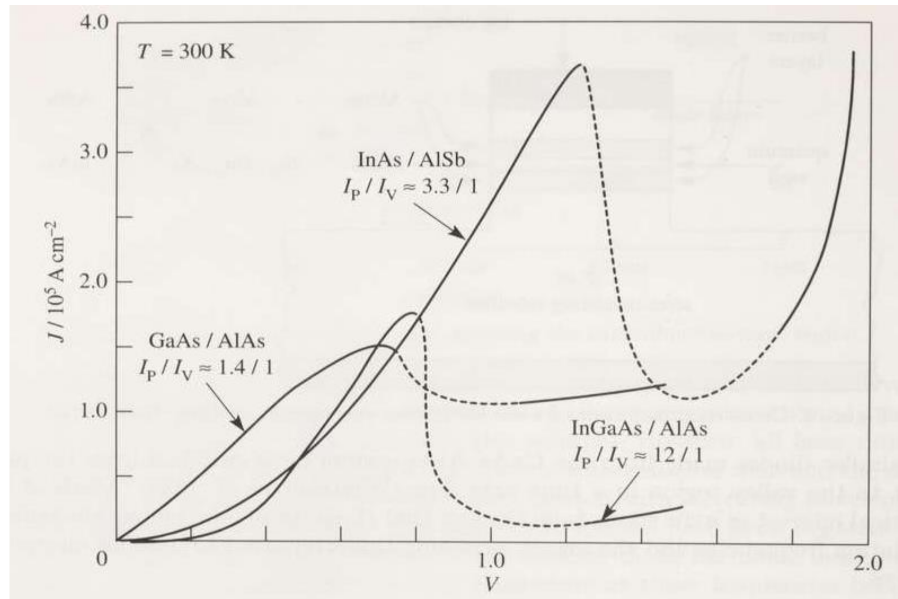

***Figure 1.15:** Current density versus voltage curves for different resonant-tunneling diode materials. The dashed lines represent interpolations through the respective NDR regions. Adapted from [71].*

Several attempts have been made to integrate an RTD into a complementary metal oxide semiconductor (CMOS) process [75] [76]. Memory and logic circuits employing RTD devices would provide a significant advantage to CMOS technology by reducing circuit complexity, power consumption, and enhancing high-speed operation [77]. Furthermore, series connected vertically integrated resonant tunneling diodes (VIRTD) with multiple negative resistance (NDR) regions would allow the realisation of multiple-valued memory (MVM) [78] [79]. Traditionally, the memory cell contains only one bit of information (1 or 0), however MVM offers the possibility of storing and transferring more information with fewer interconnects between devices, thereby providing a more compact solution to data storage.

1.4.4 State of the Art

The first RTD oscillator was demonstrated by Sollner et. al. in 1984, with a maximum observed oscillation frequency of 18 GHz and 50 μW output power [80]. For the first two decades of RTD device development, the oscillators were realized using a quasi-

optical resonator [81]-[83] as shown in Fig. 1.16, where a semi-confocal open-cavity resonator was used to stabilise the RTD waveguide oscillator.

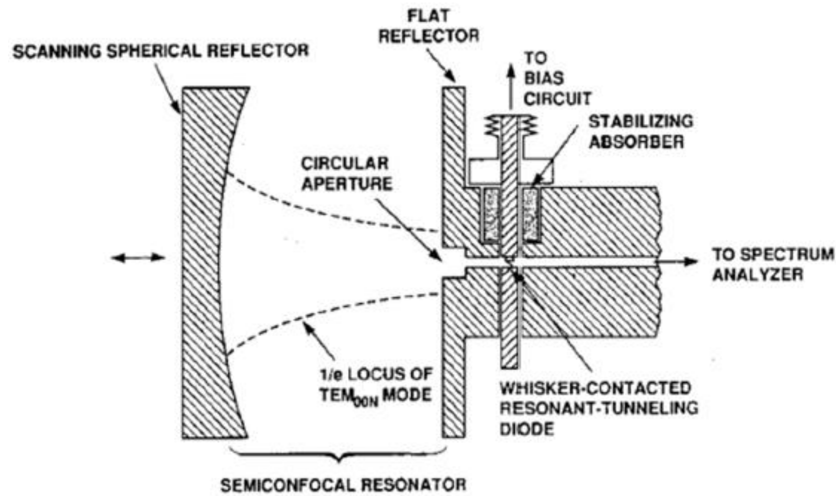

Figure 1.16: *Schematic cross-section of a quasi-optical RTD oscillator. Adapted from [81].*

Due to the large contact inductance, introduced by the whisker contacts and the high series resistance a large portion of the RF power was dissipated due to spurious bias oscillations and by the high series resistance. The highest obtained oscillation power obtained was 50 μW at a fundamental frequency of 210 GHz [83], and the highest frequency of the quasi-optical RTD was 720 GHz with 0.3 μW output power [84].

Planar RTD technology has since become more popular due to advancements in manufacturing technology as well as fewer constraints imposed on the bias stability circuit. In 1994, Smith et. al. proposed a technique with the top collector Ohmic contact replaced by a Schottky contact in order to reduce parasitic resistance and consequently increase the maximum oscillation frequency [85]. A 64-element array was first demonstrated by Reddy et. al. using the Schottky contact technique (SRTD), shown in Fig. 1.17, in which a fundamental frequency of 650 GHz was achieved [86]. Furthermore, a Si lens was used to couple the power from the oscillator array from the substrate into free space.

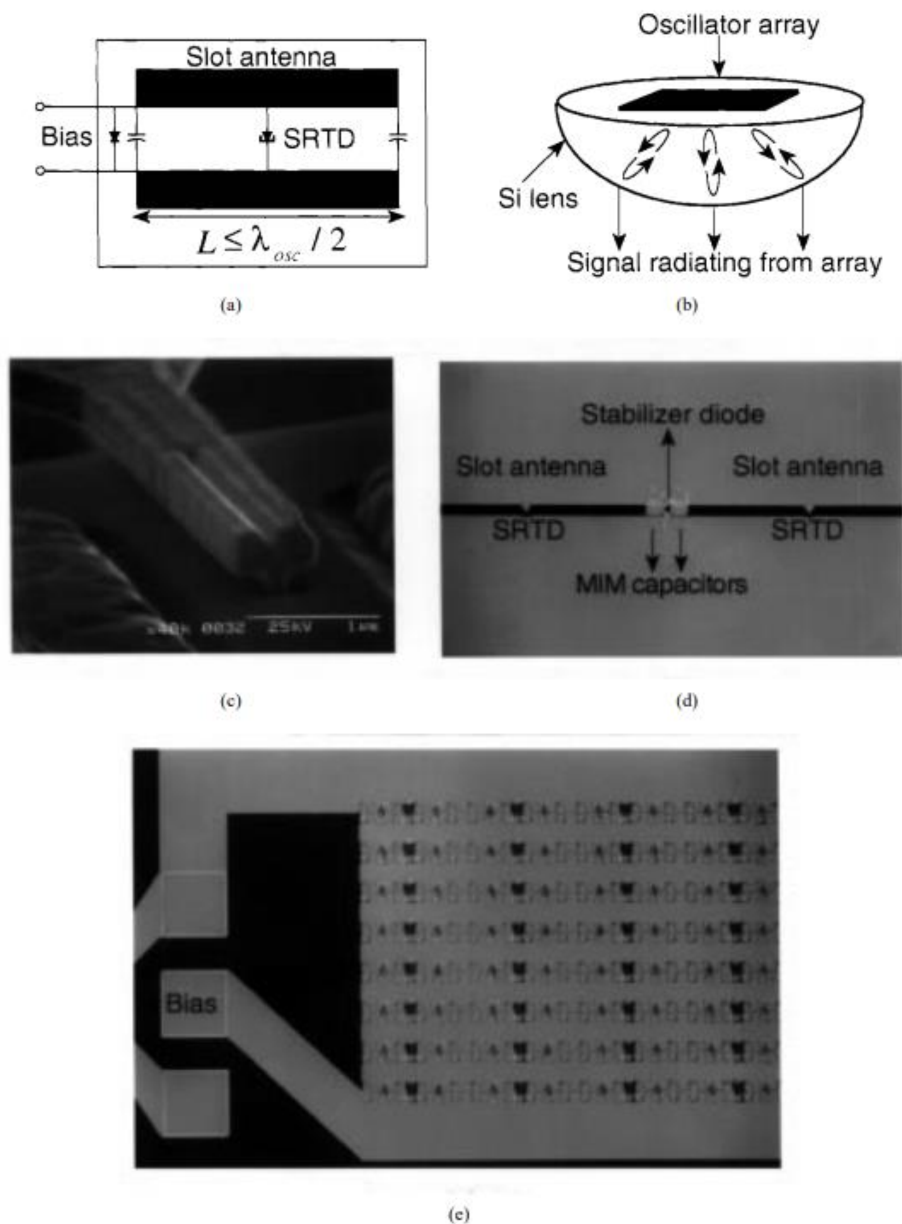

Figure 1.17: *Planar RTD oscillator with 64 elements (a) circuit schematic of a monolithic slot-antenna coupled SRTD oscillator, (b) oscillator array mounted on a silicon lens, (c) SEM image of 0.1 – μm contact stripe, (d) oscillator array section, (e) photograph of a 64-element SRTD oscillator. Adapted from [86].*

In 1995, a planar-slot antenna integrated RTD was first reported [87] with a fundamental and third harmonic frequency of 342 GHz and 1.02 THz, respectively. The devices were fabricated using e-beam lithography and metal-insulator-metal reflectors were integrated for the slot antenna. The output power at these frequencies was 23 μW and 0.6 μW, respectively. A bismuth sheet resistor was deposited in

parallel to the RTD in order to suppress the parasitic oscillations from the biasing circuit.

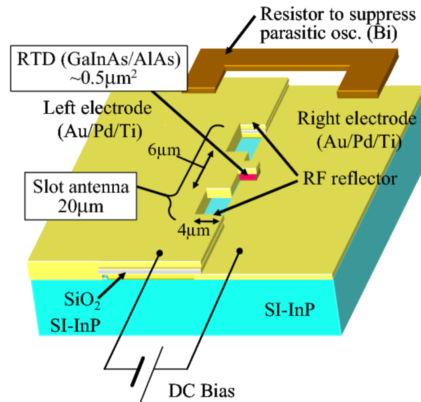

Figure 1.18: *Structure of RTD oscillator with integrated slot antenna. Adapted from [89].*

Fundamental oscillation frequencies of 831 GHz, and 1.04 THz were later reported by the same research group in 2009 [88], 2010 [89], respectively through epi-layer design optimizations.

In 2011, Feigninov et. al. reported on an RTD oscillator operating at a fundamental frequency of 1.1 THz and an estimated 0.5 μW output power [90]. The RTD mesa size was 0.35 μm^2 and had a peak current density of 14 mA/μm^2. The RTD oscillator used a planar Vivaldi antenna placed on top of a dielectric membrane that was used to extract the radiation. The RTD Vivaldi oscillator is shown in Fig. 1.19.

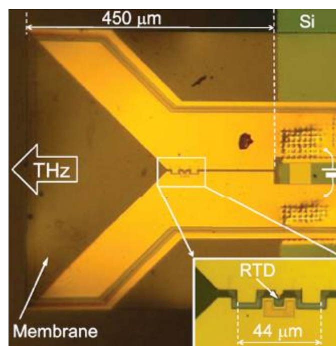

Figure 1.19: *RTD oscillator integrated with Vivaldi antenna operating at 1.1 THz. Adapted from [90].*

A new RTD circuit structure was proposed by Suzuki and Asada in 2007 based on an offset slot antenna, where the position of the RTD is shifted within the slot antenna [91]. Using this technique, the radiation conductance of the antenna and oscillation frequency can be independently determined by the lengths of the short and long parts of the slot, respectively. An RTD oscillator was fabricated with a fundamental oscillation frequency of 1.92 THz with 0.4 μW output power [34].

High performance double RTD oscillators implemented in coplanar waveguide (CPW) technology were presented in [92] [93], operating in the J frequency band (220 GHz – 325 GHz) and with about 1mW output power. A picture of the double RTD oscillator design is shown in Fig. 1.20. It is expected that output powers of 10 mW and 1mW at 500 GHz and 1 THz, respectively, can be obtained from coupled RTD technology, making the RTD a suitable candidate for the next-generation millimetre-wave and submillimetre-wave applications [94].

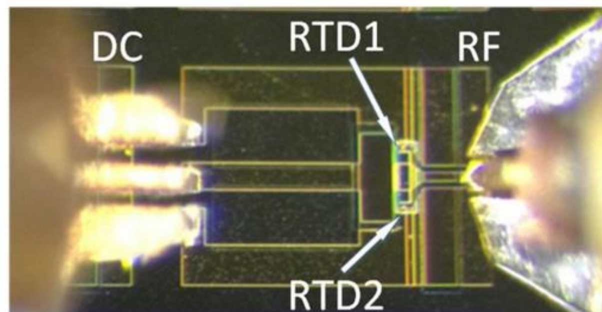

Figure 1.20: *A double RTD oscillator implemented in CPW technology operating in the J-band with around 1 mW RF output power. Adapted from [92].*

1.5 Thesis Aim and Organization

The aim of this PhD thesis was to realize and characterize RTD oscillators in monolithic microwave/millimetre-wave integrated circuit (MMIC) form for high power and frequency applications. The oscillators described in this thesis are designed to operate in the Ka-band (26.5 GHz – 40 GHz) with output power higher than 1 mW. A new circuit for RTD oscillators to suppress parasitic oscillations and increase the DC-to-RF conversion efficiency was developed and will be described.

The thesis is organized as follows: Chapter 1 introduces and reviews millimetre-wave and submillimetre-wave radiation and its characteristics. The main sources being developed are described in this chapter with discussion on possible applications. The operating principle of negative differential resistance devices is also presented alongside the current state of the art in RTD technology.

In Chapter 2 the main fabrication process required to realize RTD-based circuits using MMIC technology is discussed including photolithography, dry/wet etching, metallization, lift-off and vertical interconnect access (VIA) opening through polyimide.

Chapter 3 describes the fabrication process required for passive components that include metal-insulator-metal (MIM) capacitors, coplanar waveguide (CPW) transmission line, shorted CPW lines for inductors and thin-film resistors. The realization of low ohmic contact resistance to InGaAs is also investigated.

Chapter 4 discusses the bias circuit instabilities, their effects on performance and methods to suppress these parasitic effects. A method to accurately measure the DC current-voltage (I–V) characteristics and a model for the RTD is discussed.

Chapter 5 shows the design procedure of MMIC RTD oscillators, as well as defining the important parameters required to characterize voltage-controlled oscillators (VCOs). A new circuit topology for RTD oscillators is proposed, fabricated and compared with the previous generation of RTD oscillators in terms of DC-to-RF conversion efficiency. The RTD oscillators presented in this work operated at

frequencies between 17 GHz - 36 GHz with most of them exceeding the 1 mW output power target.

Chapter 6 presents a wireless link application in the Ka-band (26.5 GHz - 40 GHz) using an RTD modulated by a pseudo-random binary sequence (PRBRS) generator as a transmitter (Tx), and an RTD receiver (Rx) to demodulate the signal. A measured 2 Gb/s wireless data transfer speed was achieved with this setup.

Finally, conclusions and future work are discussed in Chapter 7.

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Chapter 2. RTD MMIC Fabrication Technology

2.1 Introduction

This chapter outlines the main fabrication processes required to realize an RTD-based circuit using monolithic microwave/millimetre-wave integrated circuit (MMIC) technology. The fabrication was done at the James Watt Nanofabrication Centre (JWNC) at the University of Glasgow. Cleanrooms have a classification based on the number of particles permitted per volume of air, as such the JWNC has rooms ranging from class 10,000 down to class 10, that greatly reduce the possibility of failure due to dust particles. The RTD layer structure is specified in Section 2.2 followed by an explanation to the different MMIC fabrication processes used in this project that include:

- Lithography
- Wet / Dry Etching
- Metal Deposition
- Lift-off process

RTD devices with mesa sizes ranging from 3 x 3 μm^2 up to 30 x 30 μm^2 were fabricated during this project by optical lithography due to the achievable resolution that meets the requirements, low cost, ease of access and high throughput. In total there are 9 lithography steps required to fabricate an RTD oscillator, almost all of them requiring accurate positioning relative to each other to ensure the proper alignment. For a 3 x 3 μm^2 RTD device the vertical interconnect access (VIA) size is 1.5 x 1.5 μm^2 which results in an alignment tolerance of 0.75 μm. Misalignment will result in a failing device and a failed fabrication run. Wet etching process is used to pattern the III-V semiconductor material, while dry etching is used to open a contact VIA over a polymer. Finally, the lift-off process ensures that the pattern placed in lithography comes out, leaving a clean metallisation on the sample.

2.2 RTD Device Fabrication Flow

2.2.1 Layer Structure

The project involved multiple epilayer structure designs, one such design is detailed below in Table 2.1. The wafer was grown by molecular beam epitaxy (MBE) by IQE Ltd on a semi-insulating InP substrate. The RTD device consists of (arranged from the top layer to the bottom layer): highly n-type doped contact layers ($In_{0.53}Ga_{0.47}As$) used as an interface layer for titanium/palladium/gold (Ti/Pd/Au) metallisation in the realization of ohmic contacts, 50 nm lightly doped spacer layer ($In_{0.53}Ga_{0.47}As$), 2 nm un-doped spacer layer ($In_{0.53}Ga_{0.47}As$), 1.1 nm wide band gap material barrier layer (AlAs; E_g = 2.15 eV), 1.1 nm un-doped narrow band gap material quantum well layer ($In_{0.53}Ga_{0.47}As$; E_g = 0.71 eV), 1.4 nm un-doped narrow band gap sub-well layer (InAs; E_g = 0.36 eV) used to lower the resonant energy level inside the quantum well [1] [2], that help reduce the peak voltage, 1.1 nm un-doped narrow band gap material quantum well ($In_{0.53}Ga_{0.47}As$), 1.1 nm un-doped wide band gap material barrier (AlAs), 2 nm un-doped spacer layer ($In_{0.53}Ga_{0.47}As$), 50 nm lightly doped spacer layer, a 20 nm highly doped etch stop layer (InP), a highly doped contact layer ($In_{0.53}Ga_{0.47}As$). The lightly doped spacer layers are used to increase the depletion region width, thereby decreasing the diode's capacitance, making the device suitable for high-frequency operation. It also has been reported that the peak-to-valley current ratio (PVCR) increases with increasing spacer layer thickness, while the peak current density decreases [3]. The un doped spacer layers help reduce the diffusion of dopant impurities to the double quantum well structure. Finally, the InP etch stop layer is used to control the etch depth during wet etching as a different chemical composition is needed to etch the InP layer.

The complete epitaxial layer structure was adapted from [4]. It provides a large peak to valley current ratio (PVCR) and low peak voltage, which are essential device characteristics for high performance oscillator design.

Table 2.1: *RTD epi-layer design structure used in this project.*

Layer No.	Layer Structure #1 Wafer China Wafer			
	Thickness (A)	Composition	Doping	Description
1	450	$In_{0.53}Ga_{0.47}As$	3E19: Si	Collector
2	800	$In_{0.53}Ga_{0.47}As$	3E18: Si	Sub-Collector
3	500	$In_{0.53}Ga_{0.47}As$	5E16: Si	Spacer
4	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
5	11	AlAs	Un-doped	Barrier
6	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
7	14	InAs	Un-doped	Sub-Well
8	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
9	11	AlAs	Un-doped	Barrier
10	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
11	500	$In_{0.53}Ga_{0.47}As$	5E16: Si	Spacer
12	800	$In_{0.53}Ga_{0.47}As$	3E18: Si	Sub-Emitter
13	200	InP	1E19: Si	Etch-Stop
14	4000	$In_{0.53}Ga_{0.47}As$	3E19: Si	Emitter
15	2000	InP	Un-doped	Buffer
		SI: InP		Substrate

2.2.2 Sample Preparation

The first step is sample preparation and cleaning, where the 3-inch wafer is cleaved into smaller samples of approximately 12 mm x 12 mm dimensions. Before the cleave process the wafer is covered with a layer of photoresist to protect from scratches and contamination. The cleaning process follows with an ultrasonic bath in acetone ($(CH_3)_2CO$), methanol (CH_3OH) followed by isopropyl alcohol (C_3H_8O). Acetone is a good polar solvent and the primary chemical used to remove organic residue; however, the high evaporation rate of the chemical can cause re-deposition of the remnants. Therefore methanol, another polar solvent is used to remove the contaminants related to acetone residue. Isopropanol is the last cleaning agent used and is most suitable for dissolving non-polar contaminants that remain on the sample.

Another important step before starting the fabrication process is to determine the correct side of the InP sample, since both sides are polished and are visually hard to distinguish. Current-voltage (*I*-*V*) measurements are therefore carried out on both sides, the measured resistance of the semi-insulating substrate is in the order of

giga-ohms, while that of the highly doped contact layer is usually in the tens of ohms range. An *I-V* curve of the InGaAs layer and InP layer is shown in Fig. 2.1.

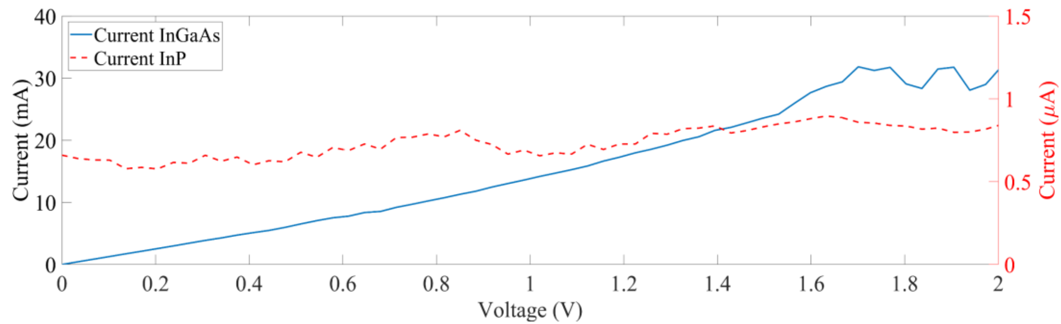

Figure 2.1: *Measured current for the top InGaAs layer (left axis) and substrate InP layer (right axis) for the RTD-EPI layer structure presented in Table 2.1.*

2.2.3 Fabrication Process Flow

The fabrication flow diagram needed to realize an RTD device is shown in Figure 2.2. Fabrication starts with the deposition of the top metal contacts on the emitter / collector layer as shown in Fig. 2.2 (a). A number of reviews of ohmic contacts on III - V compound semiconductors are available from [5]-[7]. The metal scheme used is Ti/Pd/Au (20/30/150 nm), which has a reported specific contact resistance ρ_c of $0.73 \pm 0.44\Omega\ \mu m^2$ [5]. After metal deposition the sample is placed in a 1:1 solution of acetone and photoresist stripper 1605. The next step, as shown in Fig. 2.2 (b), is to etch the epitaxial layers down to the bottom contact / emitter layer using an acid solvent (H_3PO_4:H_2O_2:H_2O 1:1:38) which has an etching rate of about 100 nm/min. The etch stop layer is removed using a different acid solvent (HCl:H_2O_2 = 1:4) for about 30 seconds. After wet etching another contact metal is deposited on the bottom collector / emitter layer as shown in Fig. 2.2 (c). A second wet etch process follows, illustrated in Fig. 2.2 (d), that exposes the InP substrate and isolates the individual RTD devices. Again, a combination of acid solutions as described previously are used to etch the different layer compositions. Thereafter, the next step is to deposit the passivation layer (polyimide PI-2545) and a VIA is opened by dry etching over the polymer once it has cured as shown in Fig. 2.2 (e). The final metal contacts (Ti/Au 20/380 nm) are deposited to provide a landing surface large enough for the probes and completes the RTD device fabrication as shown in Fig.2.2 (f).

Figure 2.2: *RTD device fabrication steps: (a) top contact metal deposition, (b) wet etch to the bottom emitter/collector layer, (c) bottom contact metal deposition, (d) wet etch to substrate, (e) PI-2545 deposition and via opening using dry etch, (f) bond pad metal deposition*

For oscillator circuits additional passive components such as a thin-film resistor and a metal-insulator-metal (MIM) capacitor are required and extra fabrication steps are needed in order to accomplish this. These will be described in Chapter 3.

2.3 Fabrication Processes

2.3.1 Lithography

Lithography is the process used to transfer patterns from a mask onto the sample surface. The most common lithography techniques are photolithography using ultra-violet (UV) light for exposure, electron beam (e-beam) lithography, x-ray lithography and extreme ultraviolet lithography. After being cleaned, the sample is heated on a hot-plate at 120°C for 5 minutes, in order to remove any moisture present on the wafer surface. The sample is then attached to a spinner inside a laminar air flow (LAF) cabinet by means of a vacuum and covered in resist. It is then rotated at high speed in order to spread the resist by means of centrifugal force. The thickness of the resist film is dependent on the rotational speed and fluid viscosity. After spinning, the resist-coated sample is then pre-baked typically at 115°C for 1 min (S1805) and is ready for patterning. The lithography tools used in this project are the Karl Suss MA6 mask aligner (photolithography) and the Vistec VB6-UHR-EWF (e-beam lithography). The pattern is then developed using a solvent to selectively remove the exposed areas of the thin film. The next step is to remove any residual resist using a barrel asher, that uses an oxygen powered plasma. The oxygen ions etch the residual resist at a 10nm/min rate using 120W RF power, removing any residue resist. The sample is ready for deposition or etching. Fig. 2.3 shows an illustration of the photolithography process.

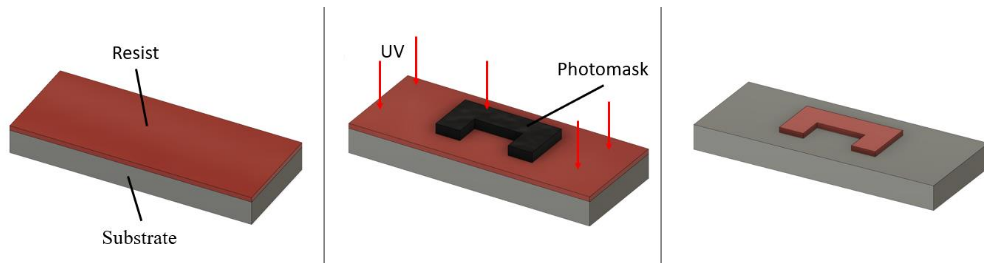

Figure 2.3: *Illustration of the photolithography process. The substrate is first coated with a thin layer of positive photoresist. Using the Karl Suss MA6 mask aligner, the photomask is placed in contact with the sample. After exposure the sample is developed, whereby the resist that was not shielded by the photomask is removed leaving an accurate reproduction of the mask pattern.*

Electron-beam Lithography

In electron-beam lithography a focused beam of electrons is directed at the sample surface covered with suitable resist (PMMA, ZEP), sensitive to the electron beam. Due to the bombardment of electrons, the molecular structure and solubility of the resist film are altered. The Vistec VB6-UHR-EWF tool available at the JWNC has a minimum resolution of 0.5 nm and a minimum spot size of 4nm.

In this project e-beam was used in the manufacturing of the optical masks (by Compugraphics) for the photolithography process, and for the manufacturing of single step jobs such as antennas or correcting photolithography mask errors. The desired patterns are first designed using CAD software tools such as L-Edit. An un-processed photomask, consisting of a glass plate coated on one side with a thin layer of chrome, is coated with e-beam sensitive photoresist and placed inside the e-beam tool for patterning. After patterning the mask is immersed into a developing solution where the areas exposed to the electron beam are dissolved, leaving the desired pattern. A chrome etch follows that removes the zones not protected by the resist.

Compared to photolithography, e-beam lithography has a much higher resolution and registration (how accurately successive patterns on the mask can be aligned), but the lower throughput and high cost make it unsuitable for micron-sized RTDs.

Photolithography

Photolithography makes use of an ultra-violet (UV) light source of wavelength between λ = 200 - 400 nm to expose the photoresist, in a process that is similar to the e-beam lithography process described previously. When compared to e-beam, photolithography is a low cost and high throughput technique, with a resolution capability of 0.5 µm, that meets all the requirements of the manufactured micron-sized RTDs [8]. The sample and hard mask are loaded onto the mask-aligner. After alignment, the mask is placed in contact with the sample, where it blocks light in the areas covered by the chromium pattern. Once developed the patterns define the required features which will be used in the different fabrication steps such as metal/dielectric deposition and etching.

Photoresist

Photoresists are essential compounds used in microfabrication and consists of binders, sensitizers and solvents. The role of the sensitizer is to define the photosensitivity of the resist. When exposed to UV light, the chemical structure of the resist becomes insoluble or soluble, depending on the resist type in the developer. The solvents define the viscosity of the resist, which allows the resist to be spun and to form thin layers on the wafer surface. The binders control the thermal characteristics of the resist. There are two types of photoresists, positive and negative resist. In the positive resist, the exposed area dissolves during the developing process, while the un-exposed region remains unchanged. The same principles work in reverse for the negative resist. Both negative and positive photoresist have advantages and disadvantages. The positive photoresists present excellent resolution and can be developed in aqueous developers, however they suffer from bad adhesion and lower resistance to etching when compared to their counterpart. The negative resists offer better adhesion and resistance against etch processes at the cost of lower resolution and can only be developed in toxic organic developers.

Spin coating is the standard resist application method, where a few drops of resist are applied at the centre of a static or a slowly rotating wafer. After application the wafer is accelerated, in most cases to 4000 rpm, where the resist spreads over the wafer, leaving a uniform layer. The soft bake or pre-bake process (115° C for 1 min) that

follows evaporates the remaining solvent, hardening the resist. Spin-film definition at the edge of the sample is often poor [9], as the resist always flows over the edge, it forms a non-uniform coating. This is known as *edge bead* [10]. As such steps are carried out in order to remove the excess resist present at the edge of the sample. A cotton bud containing acetone is carefully used to clean the edge of the sample and/or the underside of the sample if resist is present there.

In this project, two positive photoresists have been used: S1805 and S1818 from MicroChem. The difference between the two photoresists are their respective spin-thickness and is shown in Figure 2.4 [11]. At 4000 rpm spin speed, the thickness measured were 1.8 µm and 0.5µm for the S1818 and S1805, respectively.

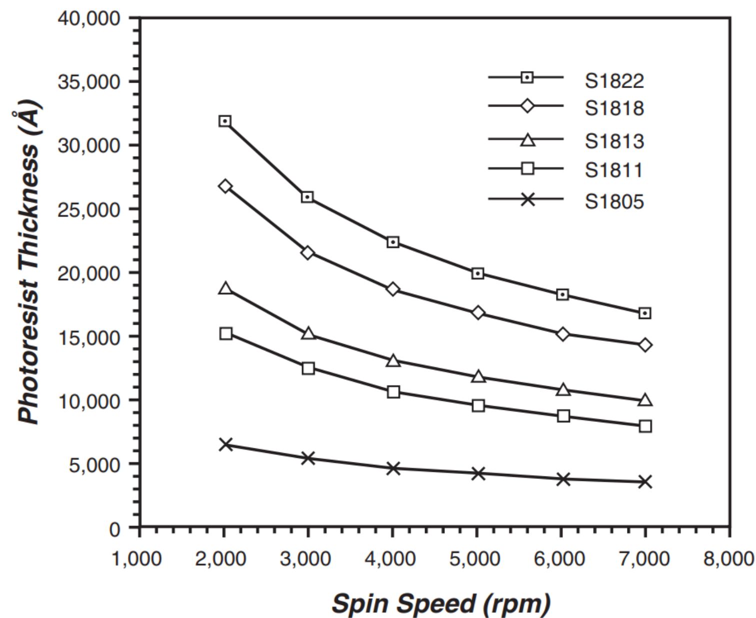

Figure 2.4: *S1800 series photoresist spin speed vs thickness. Adapted from [11].*

The thickness of the resist must be considered during the lift-off process, used in metallisation patterning (to be described in Section 2.3.2). Thin resists layers are preferred for better resolution, however there is a minimum resist-film ratio that needs to be satisfied for a successful lift-off. As such for thin metal films (around ~200 nm) a single layer of S1805 resist was used (2.5:1 resist-film ratio). Positive photoresists usually have a slightly positive slope [9] that needs to be corrected in order to prevent side-wall deposition during metallisation. In this project, the sample was soaked in either chlorobenzene (C_6H_5Cl) or toluene (C_7H_8) for a couple of minutes before

exposure to reduce the dissolving rate of the resist's top surface. As a result, the profile of the soaked resist will have an undercut characteristic, making the lift-off process easier. Chlorobenzene was initially used but was discontinued from the JWNC due to health concerns. An illustration of the single-layer metal lift-off process is given in Fig. 2.5.

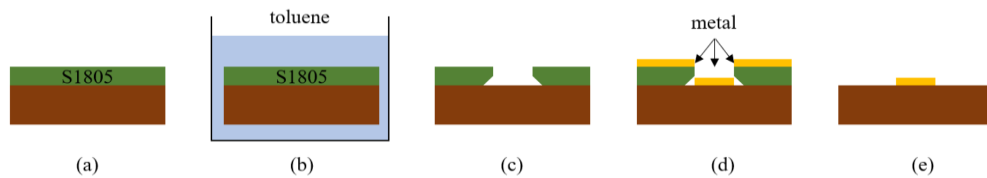

Figure 2.5: *Illustration of the lift-off process using toluene. (a) clean, spin and pre-bake the photoresist (b) dip in toluene for about 1-minute (c) expose and develop the photoresist, (d) metallization, and (e) metal lift-off.*

When thicker metal layers are required (~400 nm) a bi-layer lift-off process was used. A lift-off resist, usually LOR-10A, is first spun onto the sample and pre-baked at 150°C for 3 mins followed by S1800 series resist deposition. After exposure and development, an overhang profile is formed due to the different dissolution rates between the LOR and S1800 resist. The undercut formed is larger than that of the toluene treated single layer lift-off and ensures an easier lift-off due to no possible side-wall deposition. An illustration of the bilayer lift-off is shown in Fig. 2.6.

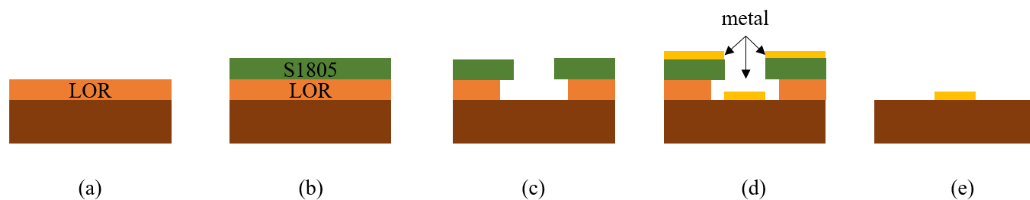

Figure 2.6: *Illustration of the bilayer lift-off process (a) clean, spin and pre-bake the LOR layer (b) spin and deposit S1800 resist (c) expose and develop the photoresist, (d) metallization, and (e) lift-off.*

2.3.2 Metallisation

Depositing metal on the semiconductor wafer can be accomplished in several different ways, such as physical vapour deposition (PVD), sputtering or electroplating. The technique used to deposit thin metal films in this project was electron-beam physical vapor deposition (EBPVD), a variation of PVD. A Plassys MEB 550S (Plassys II and Plassys IV) system was used to deposit the titanium (Ti), palladium (Pd), molybdenum (Mo), gold (Au) and nickel – chromium (NiCr) metals used in the fabrication. Once the sample is loaded into the evaporator, the main chamber is pumped to a base pressure of 2×10^{-6} Torr and the desired metal scheme is selected via control software. Following the desired metal scheme, the metal crucibles inside the chamber are heated over the melting point by a beam of electrons. The heated metals have high vapor pressures and in the high vacuum, the evaporated atoms will be transported to the substrate. A mechanical shutter is used to turn on the deposition, once the required evaporation rate has been achieved (0.5 nm/s for Au).

Another important feature of the Plassys tool is the available argon gun, that is used to clean the surface of the sample by bombardment with ions. This technique de-oxidises the surface of the sample and lowers the ohmic contact resistance. The specific contact resistance was measured by transmission line model (TLM) technique and is detailed in Chapter 3.

In order to improve the quality of the contacts and their adhesion to the substrate a Rapid Thermal Annealing (RTA) process is used. The sample is loaded in a chamber pumped with nitrogen, where it is rapidly heated to 275° C for 60 s. A degradation can be observed on the metal contacts for longer anneal times and is attributed to indium out-diffusion [12] from the InGaAs layers under the metal film.

2.3.3 Dielectric Layer Deposition

In the fabrication process for RTD oscillators, it is necessary to deposit thin films of dielectric materials for the creation of metal-insulator-metal (MIM) capacitors. The two most common passivation materials are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), which was used in this project. Inductively Coupled Plasma Chemical Vapour

Deposition (ICP-CVD) is the process used to deposit the thin dielectric film, using the System 100 ICP-CVD from Oxford Instruments. The high-density plasma allows the deposition at low temperatures of the silicon nitride film with minimal hydrogen present [13]. The low deposition temperature is an essential requirement for the S1800 mask. A bi-layer lift-off process was employed as it offers better lift-off when compared to a single layer lift-off process, mainly due to the side-wall deposition of the Si_3N_4.

2.3.4 Etching

Etching is referred to as the physical and/or chemical process that removes layers from the surface of the substrate in the areas that are not protected by hard (metal) or soft (resist) masks. This process is accomplished by either wet or dry etching, according to the requirements of the application:

- *Uniformity* is defined as the deviation in etch rate across the sample.
- *Selectivity* is the ratio between the etch rates of different materials.
- *Isotropy* is the uniformity of the etch in all directions

Knowing the etch rates of the materials that are exposed to the dry etch / wet etch solution is crucial in the manufacturing process. High selectivity is desired between the film and substrate. In wet etching the resist selectivity is high (> 50:1), however during dry etch the selectivity is low (~ 1.5:1), and care must be taken not to over-etch and remove the protective resist film. Another important requirement is the degree of isotropy, and is defined as:

$$Isotropy = 1 - \frac{R_l}{R_v} \quad (2.1)$$

where R_l represents the lateral etch rate and R_v is the vertical etch rate. An etch process that has a degree of isotropy equal to 0, meaning that there is no lateral etching is called *perfectly isotropic*, while a degree of isotropy equal to 1 is called *perfectly anisotropic*. The wet etching process is shown in Fig. 2.7.

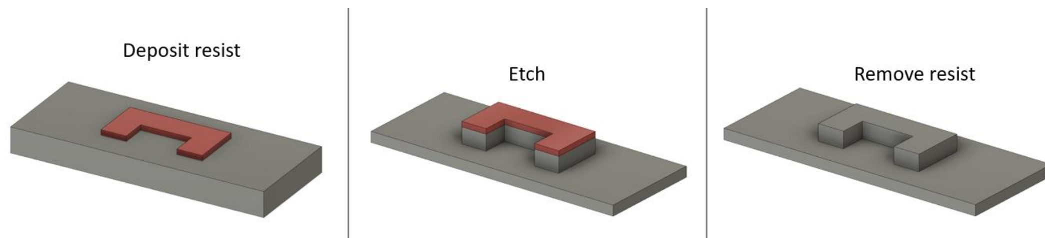

Figure 2.7: *Etching process. The substrate is first coated with a layer of photoresist which is used as an etch mask to protect the desired areas. A wet or dry etching is carried out. The resist is then removed.*

Wet etching

The most common techniques used in the wet etch process is immersion and spray methods. In the immersion method, the wafers are submerged in a container containing the etching solution for the required time. The advantages of using a wet etch process are:

- Low cost and fast process that does not involve any specialized equipment
- Very high selectivity, making possible the use of the etch stop layers and does not damage the resist mask.
- Low surface damage

Disadvantages include:

- Isotropic process resulting in undercut
- Highly toxic and corrosive chemicals are used
- Non-uniformity across the wafer

For the wet etching of the InGaAs, AlAs, InAs layers a solution of orthophosphoric acid (H_3PO_4) and hydrogen peroxide (H_2O_2), diluted in water was used (H_3PO_4:H_2O_2:H_2O 1:1:38). The oxidising agent (H_2O_2) creates an oxide layer at the material surface and then the acid is used to remove the oxide in a reduction reaction [9]. The etching rate is around 100 nm/min and does not etch the InP substrate. For InP a solution of hydrochloric acid (HCl) and hydrogen peroxide is used (HCl:H_2O_2 1:4)

and has an etch rate of 600 nm/min. Because of the isotropic nature of the process, the etch profile is rounded. Undercutting is similar to vertical etched depth and will become severe when the aspect ratio of the feature is high. This undercut is undesirable since it will cause a reduction in the designed device size and lowers the expected performance. Undercutting can be compensated by making the initial mask feature slightly larger than the desired width. Figure 2.8 shows the undercut profile of a 3 μm x 3 μm fabricated device, taken with a scanning electron microscope (SEM).

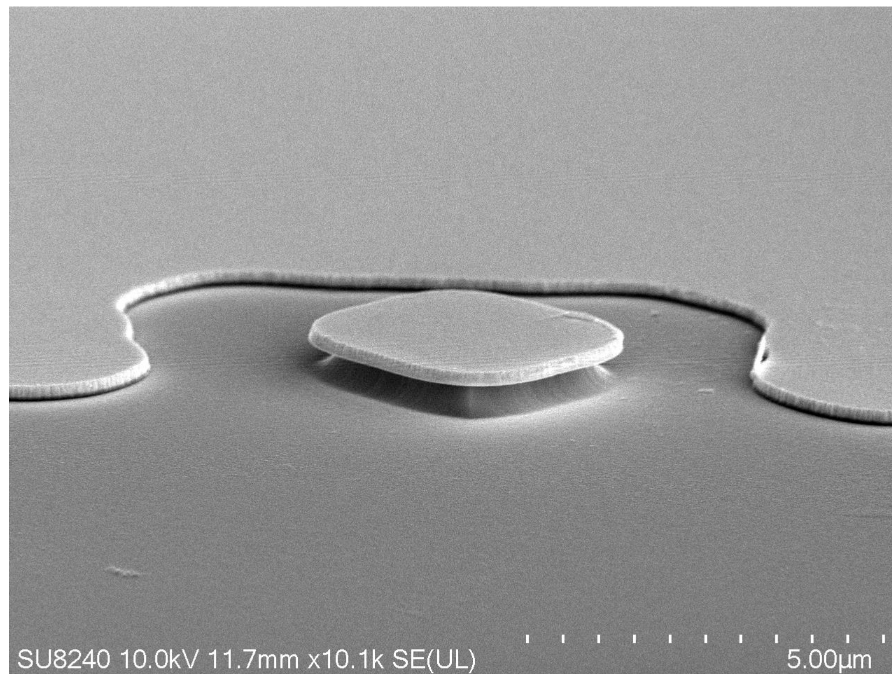

Figure 2.8: *SEM picture of an RTD device showing the undercut profile caused by wet etching. The effective area of the RTD is reduced due to lateral etching.*

Dry etching

The dry etch process is a combination of a physical process and chemical reactivity, whereby the reactive gasses are excited and ionized by RF-fields inside the chamber and bombard the material surface, where the chemical reactivity of the ion removes the material at the surface. The low-pressure in the chamber prevents the particles that are etched away from redepositing on the surface. The process provides high uniformity, etch-rate control and has high levels of anisotropy.

The dry etch process was used to open the VIA in the polyimide (PI-2545) and make a connection between the top contact of the RTD device and the bond pads. In this projected the Oxford Instruments RIE80+ tool was used for dry etching. In order to etch the polyamide layer a mixture of tetrafluoromethane/oxygen (CF_4/O_2) was used, with an RF power of 200 W and a mass flow rate of 5/20 sccm. The measured dry etch rate is about 220 nm/min for PI-2545 and 150 nm/min for S1805 photoresist. A laser interferometer was used as an end-point detection technique [14]. The interferometer creates a coherent beam of light (constant phase and frequency) that is split by a beam splitter into two identical beams, one aimed at the sample. These travel different routes and recombine before arriving at the detector. During the etching process, the path length of the beam aimed at the sample varies causing constructive and destructive interference at the detector. Waves which are not completely in phase or out of phase will have a different intensity pattern. When the PI-2545 is completely etched, the laser will have constant intensity. Figure 2.9 shows the interferogram example obtained during the dry etch process.

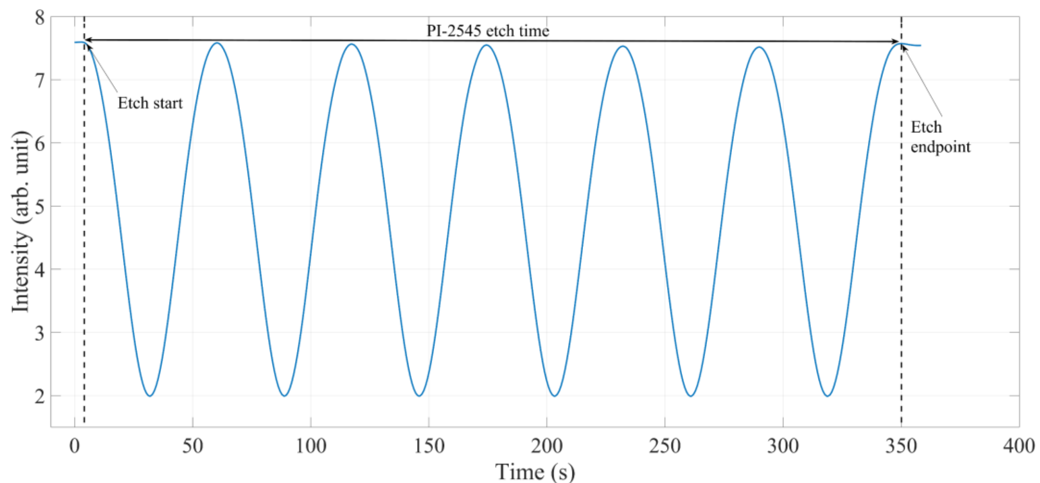

Figure 2.9: *Interferogram obtained during the dry etch process of the polyimide layer. The etch duration is approximately 5 min and 30 seconds, total etch depth is 1.2 μm for the polyimide layer.*

Another purpose of the polyamide layer was to prevent the breaking of the metal when deposited on two areas of different heights. The polyamide cushion allowed for the deposition of thin metal layers, as shown in Fig. 2.10. Without this layer, thicker electrodes would have been needed to prevent the metal from breaking.

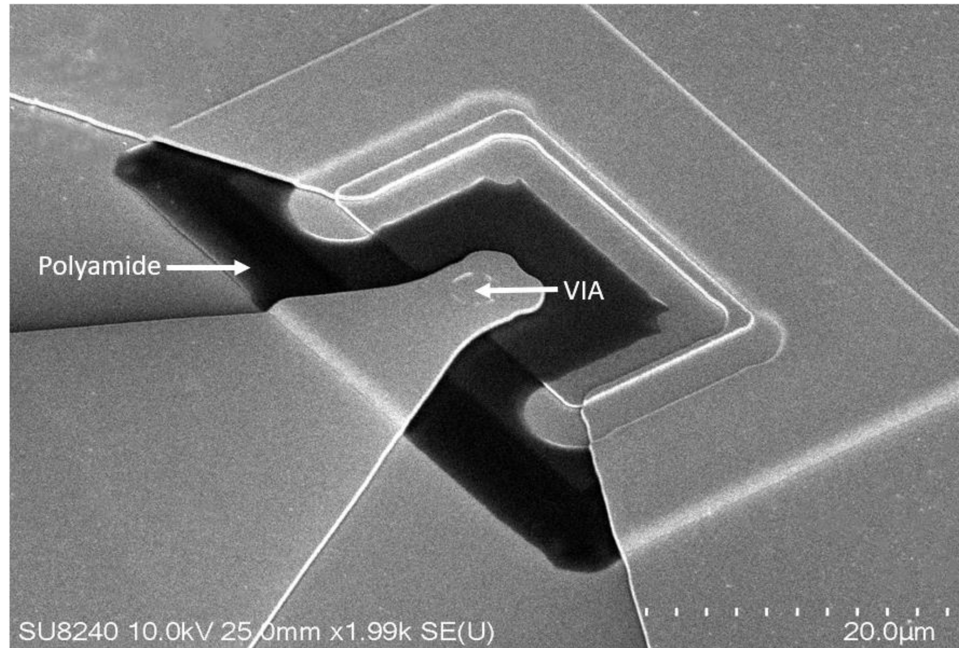

Figure 2.10: *SEM picture of an RTD device showing the polyamide cushion that isolates the top emitter and bottom collector metals and prevents the metal from breaking.*

2.4 Summary

In this chapter the main aspects of the RTD MMIC fabrication process have been discussed. Photolithography was used to transfer the patterns from the mask onto the resist covered substrate. The wet etching process was used to remove the InGaAs layers as defined by the mask, while dry etching was used to create a VIA opening in the polyimide layer. Single and bi-layer lift-off process have been explained and have been successfully applied to the metallization and dielectric layer deposition procedures. The fabrication process described in this chapter is detailed in Appendix A.

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Chapter 3. Design and Characterization of Passive Components

3.1 Introduction

The realization of RTD oscillators requires several additional passive components according to the specific design. These include the metal-insulator-metal (MIM) capacitors, the coplanar waveguide (CPW) transmission line, shorted CPW inductors and resistors. In this chapter, the design procedures for these different components are described. Theoretical values of these components are calculated and validated with experimental results. The realization and characterization of Ohmic contacts is also investigated as it plays an important role in the performance of an RTD oscillator.

3.2 Design of Passive Components

3.2.1Thin-film and Semiconductor Resistors

In this project thin-film or semiconductor resistors were used to suppresses the bias oscillations present in the NDR region of RTDs. Several factors are considered when designing integrated resistors [1]:

- Sheet resistance
- Power density handling capability
- Accuracy and reproducibility
- Temperature coefficient of resistance (TCR)
- Frequency response

Two different materials were used in this project nickel – chromium (NiCr) and semiconductor (InGaAs) resistors. The advantages of using NiCr resistors are that they show a low TCR (77 ppm / °C) [2]-[4], and are fairly easy to fabricate, however several manufacturing runs suffered from low yield, due to poor adhesion of the NiCr to the InP substrate. A more reliable process was developed using the bottom highly doped

InGaAs layer of the RTD epitaxial structure as a semiconductor resistor. The geometry of a fabricated thin-film NiCr resistors test structure is shown in Fig. 3.1.

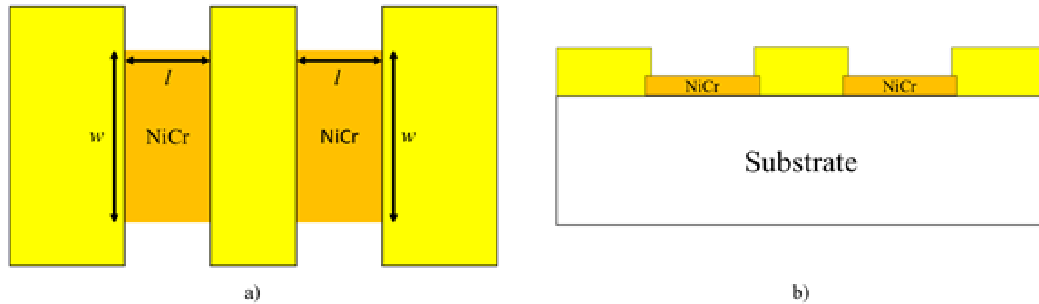

Figure 3.1: *NiCr thin-film resistor design test structure: (a) top view, (b) cross section view.*

The resistance value R can be calculated using Eq. 3.1 [5] , where ρ is the material bulk resistivity (1.65×10^{-6} Ω m), l is the length of the resistor in the direction of current flow, and w and t are the width and thickness of the film materials respectively.

$$R = \rho \frac{l}{wt} \tag{3.1}$$

With thin film resistors, sheet resistance R_{sh} is a common property used when designing thin film resistors of uniform thickness. The unit of measure for sheet resistance is Ω/□. For a 33 nm thick nichrome film, the sheet resistance of NiCr is around 50 Ω/□ [6][7]. For the InGaAs semiconductor resistor with high doping concentration ($n = 3\times10^{19}$ cm^{-3}) and 400 nm thickness the sheet resistance is 5 Ω/□, obtained through experimental measurements. The total resistance can be calculated using Eq. 3.2, where the sheet resistance $R_{sh} = \frac{\rho}{t}$.

$$R = R_{sh} \frac{l}{w} \tag{3.2}$$

3.2.2 Metal-Insulator-Metal Capacitors

Planar metal-insulator-metal capacitors (MIM) are a key component in RF circuits due to their low parasitic capacitance and low resistivity electrodes [8]. The MIM capacitor consists of a thin dielectric layer placed in-between two metal plates. The layout of a MIM capacitor is show in Fig. 4.2.

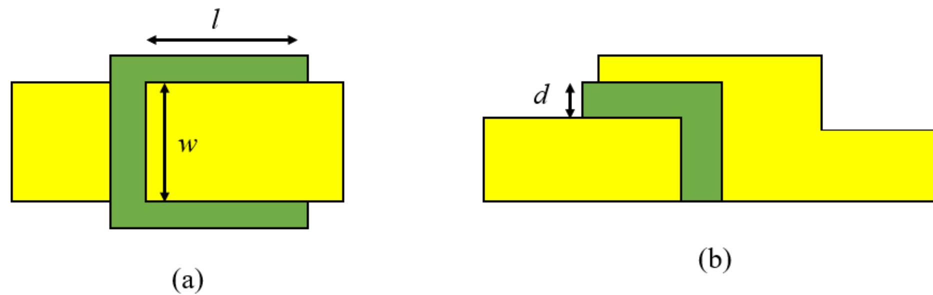

Figure 3.2: *Metal-insulator-metal capacitor design: (a) top view, (b) cross section view.*

For this project silicon nitride (Si_3N_4) was used as the dielectric material. The capacitance value can be calculated using Eq 3.3, where ε_0 is the vacuum permittivity ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), ε_r is the dielectric constant of the Si_3N_4 ($\varepsilon_r = 6.8$), A is the area, and d the thickness of the dielectric material. The thickness used in this project was 75nm, which corresponds to 0.8 fF/μm^2 capacitance.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{3.3}$$

During this project a parallel and a series placed capacitor were designed and used in the oscillator circuits. The parallel capacitor (C_E) is used as an RF short circuit to prevent RF power being dissipated across the stabilising resistor (R_E), and for the shorted transmission line structure used in realizing the resonating inductors (to be described in Section 3.2.3). A series capacitor was used as a DC block, to protect the spectrum analyser from the DC bias current applied during characterization. The impedance value for the parallel and series capacitor was chosen to be less than 0.1 Ω at the oscillation frequency, i.e. $(2\pi fC)^{-1} < 0.1\ \Omega$.

3.2.3 Coplanar Waveguide

The coplanar waveguide (CPW) was first proposed by C.P. Wen in 1969 and consists of a dielectric substrate with conductors placed on the top surface [9]. The conductors form a center strip line separated by a narrow gap, followed by ground planes on either side. The dimensions of the center strip line, the gap width, and the characteristics of the dielectric substrate determine the effective dielectric constant and characteristic impedance (Z_0). The uniplanar construction of the CPW line, in which all conductors are placed on the same side of the substrate simplifies the manufacturing process, allows for shunt / series surface mounting of components and permits fast on-wafer characterization of the devices [10]. This structure demonstrates better dispersion characteristics than microstrip and does not require any vias for grounding. Packaging can be a problem for this type of structure, as the dielectric substrate may come into close proximity to other materials, altering the transmission line characteristics [11]. A CPW structure is shown in Fig. 3.3, where *w*, *s*, *g*, *l*, and *t* are the CPW signal line width, the gap between the center conductor line and the ground plane, the ground plane width, the CPW length and the thickness of the CPW lines, respectively.

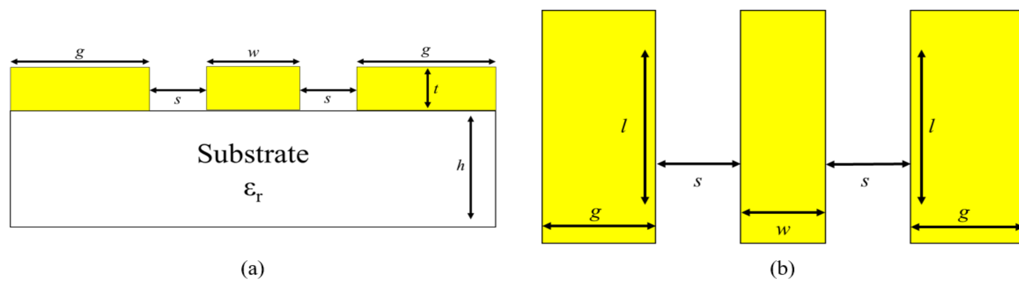

Figure 3.3: *Coplanar waveguide structure on a substrate with dielectric constant ε_r and thickness h. The centre conductor line width is denoted as w, the width of the ground planes is g, the gap between the signal line and ground plane is s, the thickness of the conductor is t and the lengths are denoted with l. (a) top view, (b) cross section view.*

In this project the LineCalc tool available within Agilent's Advanced Design System software was used to calculate the dimensions (*w* and *s*) for a 50 Ω transmission line

on InP substrate with the dielectric constant $\varepsilon_r = 12.5$ [12] and thickness $h = 630$ µm. The required signal line width and gap spacing was 60 µm and 40 µm, respectively.

In order to reduce the attenuation of the signal, the thickness of the conductor was chosen to be three times the skin depth δ [10]. Equation 3.4 is used to calculate the skin depth for a given frequency, where ρ is the conductor resistivity (2.44×10^{-8} Ω m for gold), μ_0 is the vacuum permeability ($4\pi\times10^{-7}$ H/m), μ_r the relative permeability ($\mu_r = 1$) and f the lowest frequency of interest. For the targeted 30 GHz oscillation frequency the thickness required is 1.3 µm.

$$\delta = \sqrt{\frac{\rho}{\mu_0 \mu_r \pi f}} \tag{3.4}$$

For a transmission line of length l, the input impedance Z_{in} is calculated by Eq. 4.5 [10], where Z_0 is the characteristic impedance, Z_L denotes the load impedance and β represents the phase constant. The effective dielectric constant (ε_{eff}) for a CPW line can be calculated using Eq 3.7 [13].

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 tan(\beta l)}{Z_0 + jZ_L tan(\beta l)} \tag{3.5}$$

$$\beta = \frac{2\pi f \sqrt{\varepsilon_{eff}}}{c_0} \tag{3.6}$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} \tag{3.7}$$

The CPW structures were also used to realize the different resonating inductor values required in the oscillator circuits. Fig. 3.4 (a) illustrates a shorted CPW line. In this configuration, the current flows through the metallisation at the end of the slots, storing magnetic energy behind the termination. The result is an inductive reactance when the electrical length of the line is less than 90 degrees [14].

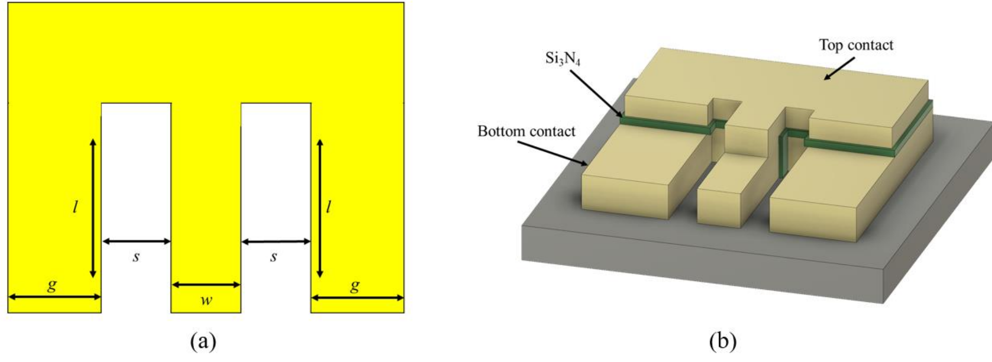

Figure 3.4: *Schematic of a coplanar waveguide stub: (a) simple short circuit stub, (b) MIM-short stub 3D model.*

For a short circuit CPW line structure (i.e. $Z_L = 0$) Eq 3.5 can be rewritten as

$$j\omega L = jZ_0 tan(\beta l) \tag{3.8}$$

where *L* is the line inductance and *ω* represents the angular frequency. Equation 3.8 can be rewritten in terms of the CPW line length *l* as shown in Eq. 3.9.

$$l = \frac{1}{\beta} atan(\frac{\omega L}{Z_0}) \tag{3.9}$$

The simple short configuration shown in Fig. 3.4 (a) has the disadvantage that it does not allow for different bias potentials on the centre and ground conductors. This restriction can be circumvented by placing a large MIM capacitor placed between the centre strip and the ground conductor. The electrical behaviour of this configuration can be described by an inductance connected in series with the MIM capacitance [15]. As stated in the previous section the value for this MIM capacitor needs to be large enough as to not deteriorate the short-circuit characteristics of the stub at the oscillation frequency .

3.3 Characterization of Passive Components

This section covers the characterization of the individual passive components described in the previous section. The CPW and MIM capacitors were characterized

with the help of scattering parameter (S-parameter) measurements using a calibrated vector network analyzer (VNA).

The VNA used in this project is the N5250C VNA from Agilent technologies, which has an operational frequency range from 10 MHz to 110 GHz. The VNA was calibrated using precise reference impedance standards in order to correct the systematic errors found in the system, i.e. frequency response error caused by reflection and transmission tracking with the device under test (DUT), directivity and crosstalk related to signal leakage, source mis-match, and load mis-match [16]. The calibration routine used is Short-Open-Load-Through (SOLT) method, which uses a short circuit, an open circuit, a precisely defined 50 Ω load and a through connection to enhance the accuracy of the measurement.

3.3.1 Coplanar Waveguide

In order to characterize the designed CPW lines, test structures were fabricated and characterized by 2-port S-parameter measurements. The CPW line was designed for a characteristic impedance Z_0 = 50 Ω on a semi-insulating InP substrate with dielectric constant ε_r = 12.5. The width of the centre conductor line is 60 µm and the gap is 40 µm. The ground plane was designed to be at least 3 times the centre strip line width , in order to minimize the radiation losses [17] [18]. A micrograph of the fabricated CPW test structure is shown in Fig. 3.5.

Figure 3.5: *Micrograph of CPW test structure. The centre strip width is 60 µm, the gap width is 40 µm, while the ground plane width is 200 µm. The CPW test structure length is 500 µm.*

The measured return loss (S_{11} and S_{22}) are plotted in Fig. 3.6 while the measured insertion loss (S_{12} and S_{21}) are plotted in Fig. 3.7. The return loss is 25 dB at 30 GHz, which indicates that very little power of the transmitted signal is reflected back to the same port. The insertion loss is 0.1 dB, which indicates that the CPW line transmits the signal from one port to the other without losses. Noise is introduced around 67 GHz by the change from coaxial source (1.85 mm) to the waveguide source (WR-10) in the extenders, which provide the extended broadband range of the equipment from 10 MHz to 110 GHz.

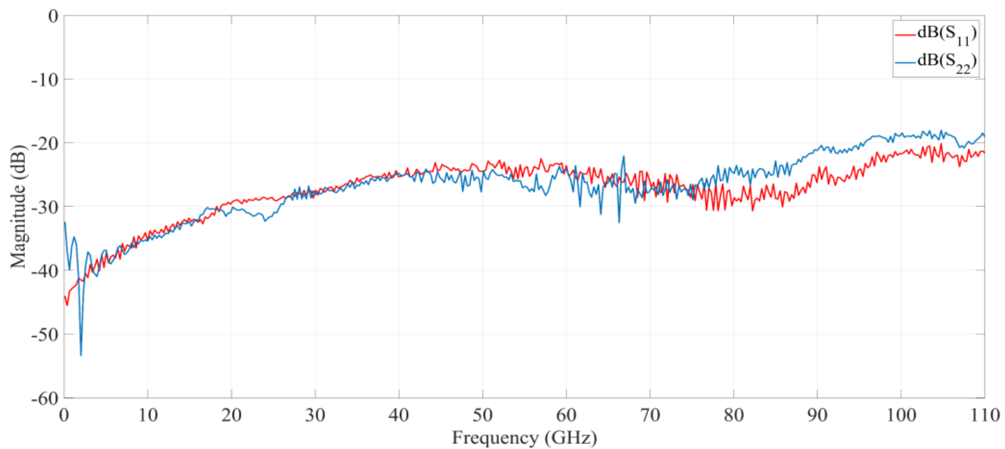

Figure 3.6: *Measured S-parameters (S_{11}, S_{22}) of the CPW line test structure. The return loss indicates that most of the power transmitted is not reflected back to the same port.*

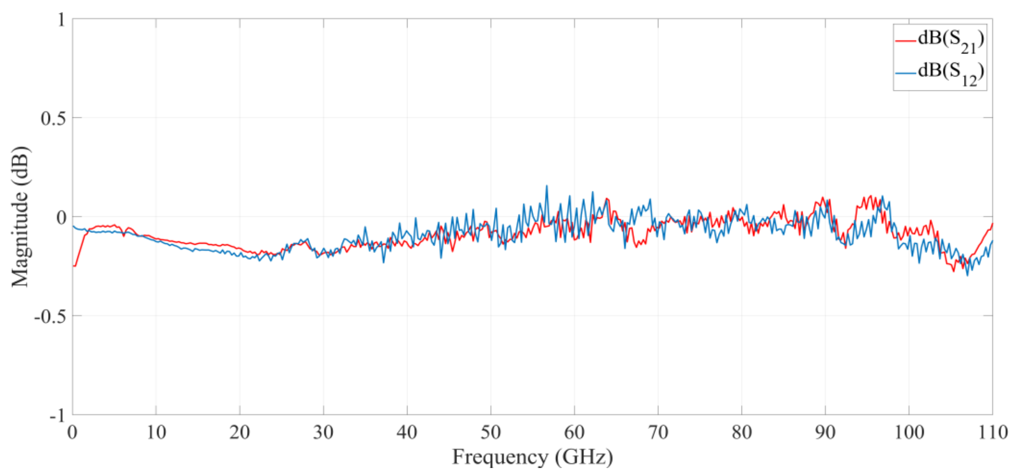

Figure 3.7: *Measured S-parameters (S_{12}, S_{21}) of the CPW line test structure. The insertion loss indicates that most of the power is transmitted to the second port.*

3.3.2 MIM Capacitor

Metal-insulator-metal (MIM) capacitors are widely used in RF circuits due to their low leakage-current, high capacitance value and ease of integration. For this project two types of MIM capacitors, for in-series and in-parallel configurations were used. The series capacitor is used for DC blocking or RF decoupling circuits, while the parallel capacitor has been used for stabilisation and as an RF short in the CPW stub configuration. The performance of the capacitors was investigated using 2 port S-parameter measurements. The capacitors were designed to operate around 30 GHz oscillation frequency. The measured return loss (S_{11}) and insertion loss (S_{12}) for the parallel capacitor and the series capacitor are shown in Fig. 3.8 and Fig. 3.9, respectively. Fig. 3.10 shows the Smith chart for both capacitors. The S-parameters of the parallel capacitor show that it acts as a short circuit where the insertion loss is below -20 dB. The input impedance for the parallel capacitor at 30 GHz is 1 + j0.15 Ω. The series capacitor acts as a short circuit for frequency ranges from 10 GHz to 110 GHz with an insertion loss of about -0.1 dB. The input impedance for the series capacitor at 30 GHz is 50.15 + j0.65 Ω. At higher frequencies the parasitic elements (inductance and resistance) become more dominant and start to degrade the capacitor performance.

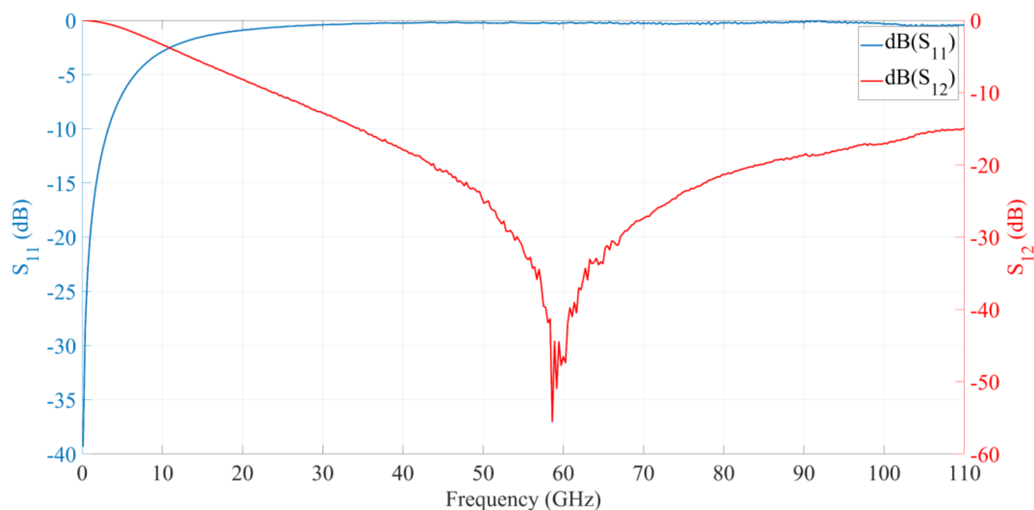

Figure 3.8: *Measured S-parameter (S_{11}, S_{12}) of the parallel capacitor test structure.*

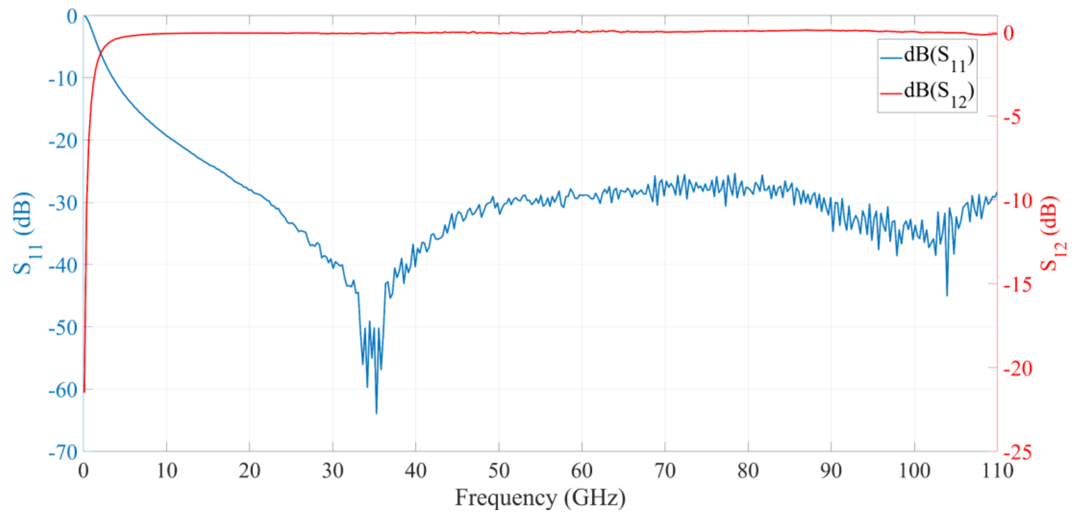

Figure 3.9: *Measured S-parameter (S_{11}, S_{22}) of the series capacitor test structure.*

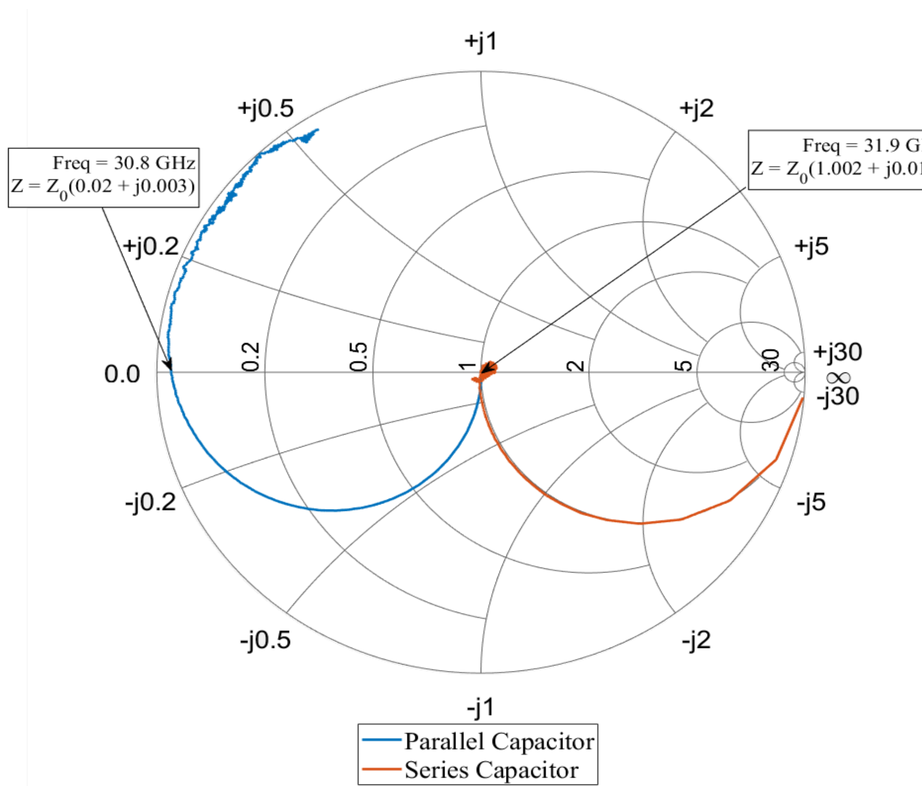

Figure 3.10: *Measured S-parameters (S_{11}) of the series and parallel capacitor test structures plotted on a Smith chart.*

3.3.3 Thin-film and Semiconductor Resistors

As discussed in the previous section, on-chip resistors were used in the RTD devices and oscillators for stabilisation. NiCr thin-film resistors and InGaAs semiconductor resistors were both used in this project. The measured sheet resistance of a thin film 33 nm thick NiCr resistor is 50 Ω/□, while the InGaAs semiconductor resistor has a sheet resistance of 5 Ω/□ when the thickness is 400 nm. A micrograph of a fabricated NiCr resistor can be seen in Fig. 3.11, while the designed and measured values of the resistors can be seen in Table 3.1. Small discrepancy was observed between the theoretical and measured resistance values, this was attributed to the non-uniform deposition thickness and contaminated interface between the material and contact pads.

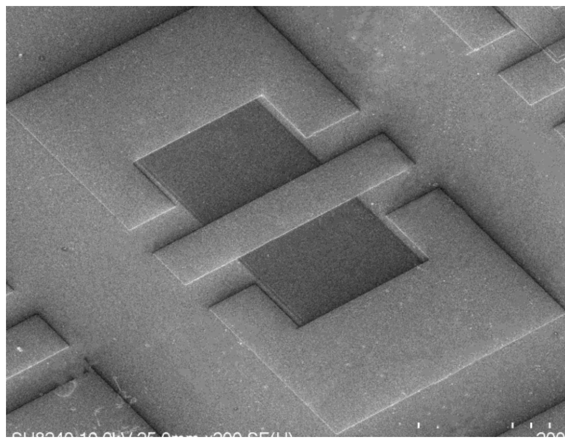

Figure 3.11: *SEM picture of a fabricated NiCr resistor test structure. Two resistors are placed in parallel to achieve the designed value.*

Table 3.1 *Thin-film NiCr and InGaAs resistor test structure measurements*

Type	R_{sh} (Ω/□)	Designed Value (Ω)	Measured Value (Ω)	Divergence (%)
NiCr	50	10	11.3	13
		20	21.3	6.5
InGaAs	5	12	11.4	5
		15	13.9	7.33

3.4 Ohmic Contacts on InGaAs

Very high frequency devices, including the RTD, require a low metal-semiconductor contact resistance in order to reduce the resistive losses, minimize the self-heating effects and the resistive capacitive delay, that imposes a limit on the maximum oscillation frequency of the device [19][20]. Linear transfer length measurements (LTLM) test structures were fabricated in order to accurately measure the contact performance [19][21]. The TLM measurement structures consists of a series of metal-semiconductor contact pads separated by increasing distances as shown in Fig. 3.12. The resistivity is measured by 4-point probe measurement technique [22][23], where a constant current is applied between two probes (named force) and the voltage is measured across the two other probes (sense). The sense probes have a high resistivity, and thus almost no current flows through the sense cable, allowing for an accurate measurement of the voltage drop.

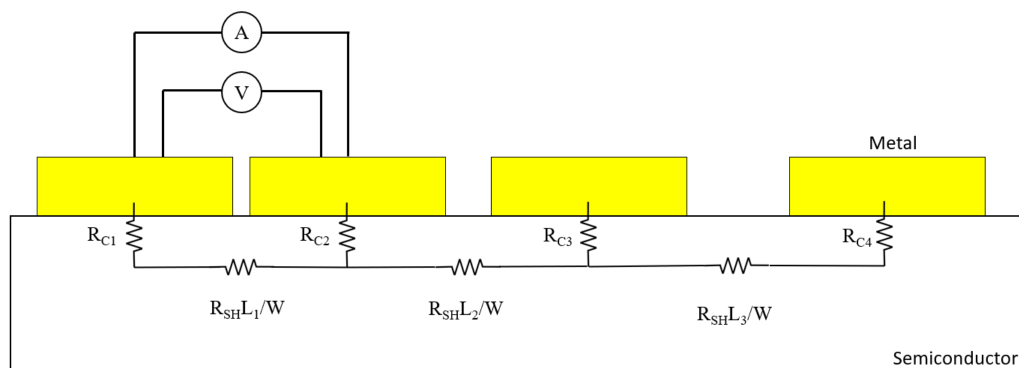

Figure 3.12: *LTLM structure with various separation distances. Four probes are placed on two adjacent contact pads, where a constant current is applied, and the voltage drop measured.*

The LTLM test-structures were fabricated on an InGaAs wafer with a heavily doped 45 nm contact layer ($n = 3\times10^{19}$ cm^{-3}). The test structures were fabricated by patterning the sample using photolithography, followed by Ti/Pd/Au (20/30/150 nm) metal deposition and lift-off process. Each pattern was then electrically isolated by photolithography and wet etching to the semi-insulating InP substrate. The nominal pad dimensions are 30 µm × 40 µm and the nominal gap widths between the contacts are between 1 to 15 µm. The fabrication of low ohmic contact onto heavily n-doped

InGaAs layers has been extensively researched in the literature [24]-[27]. The main focus has been on removing the native-oxide that forms on the surface of the contact layer before deposition. In order to remove the native-oxide, an argon gun treatment for 1 min was applied before the metal deposition. The argon gun tool is available in Plassys IV and is carried out under vacuum. Deposition happens immediately after, as such, the sample is not exposed to the atmosphere which prevents the formation of the oxidation layer. After lift-off annealing was done at a temperature of 275° C for 1 minute.

The total resistance (R_t) between two pads is composed of the two contact resistances (R_C), assuming that the contact resistances are the same (i.e. $R_{C1} = R_{C2}$), and the sheet resistance in-between the contacts (R_{sh}) multiplied by the ratio between the length and width of the gap as shown in Eq. 3.10.

$$R_t = 2R_C + R_{sh}\frac{l}{w} \tag{3.10}$$

The measurement is carried out for each contact pair that is separated by various distances. A linear plot of distance vs resistance is then obtained as shown in Fig. 3.13. From Eq. 3.10 it can be seen that the slope of the line represents the semiconductor sheet resistance over the width of the contact pad (Eq. 3.11). The intersection between the line and the resistance-axis is equal to double the contact resistance (i.e. $2\times R_C$). The intersection of the line with the distance axis (when $R_t = 0$) equals to double the transfer length ($-2\times L_T$). The transfer length is the average distance that an electron/hole travels in the semiconductor beneath the contact pad, before it flows up into the contact [19]. As such the effective area of contact can be regarded as $L_T\times W$.

$$Slope = \frac{R_{sh}}{w} \tag{3.11}$$

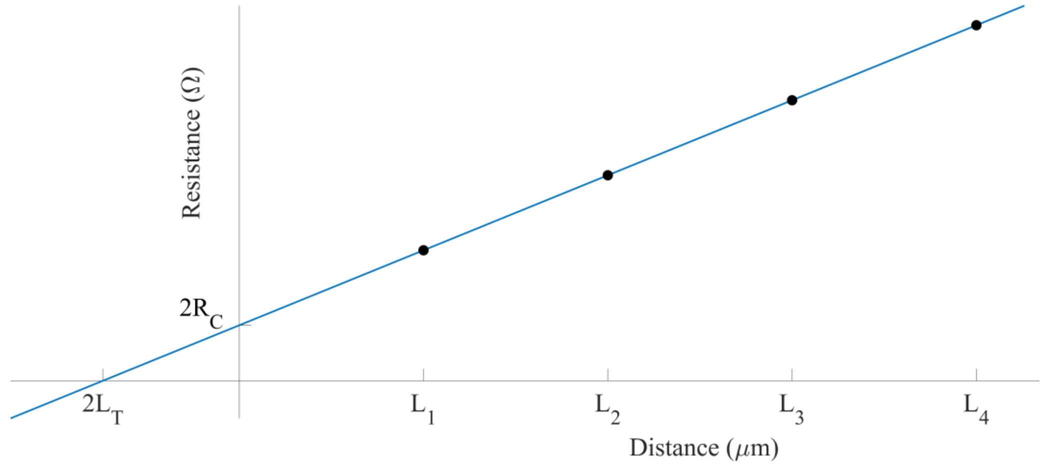

Figure 3.13: *Example of LTLM resistance as a function of gap distance. The intersection between the line and the resistance axis is double the contact resistance, while the intersection with the distance axis represents double the transfer length.*

The specific contact resistivity of the metal contact is calculated using Eq 3.12.

$$\rho_c = L_T^2 R_{sh} \tag{3.12}$$

A fabricated LTLM test structure with a gap between the two metal contacts of 2 µm is shown in Fig. 3.14. The measured resistance values are plotted in Fig. 3.15 and tabulated in Table 3.2. The extracted contact resistance (R_C), the transfer length (L_T), the sheet resistance (R_{sh}) and the specific contact resistance are listed in Table 3.3. The achieved specific contact resistance is 10.15 Ω µm^2. For 4 µm × 4 µm and 5 µm × 5 µm devices the contact resistance is equal to 0.6 Ω and 0.4 Ω, respectively. The result is one order of magnitude higher when compared to the lowest reported contact resistance in [24].

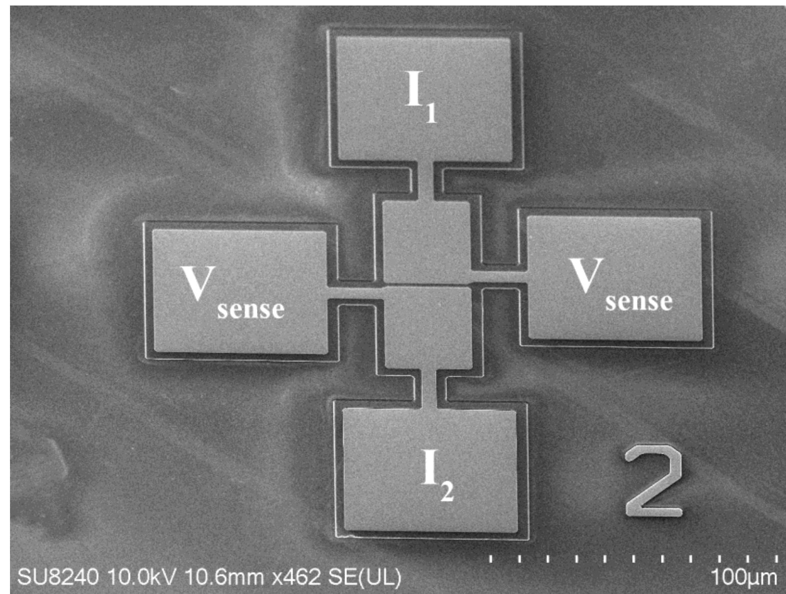

Figure 3.14: *SEM of a fabricated LTML test structure with a gap spacing of 2 μm. The position of the current probes is marked with I_1 and I_2, while the sense probes are marked V_{sense}.*

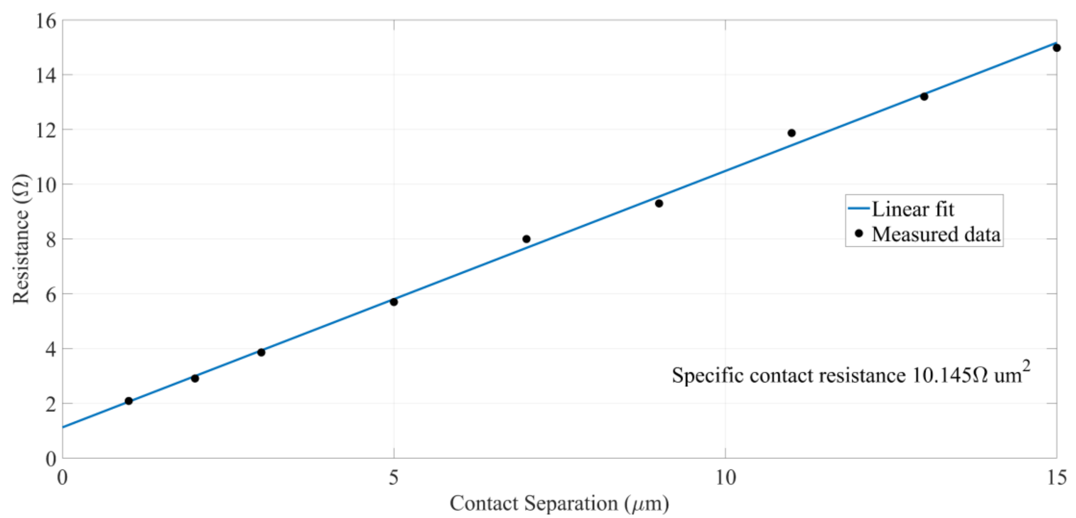

Figure 3.15: *Measured plot of resistance as a function of contact separation distance for TLM structure.*

Table 3.2 *TLM measurement data*

Gap spacing (μm)	Resistance (Ω)	Gap spacing (μm)	Resistance (Ω)
1	2.09	9	9.55
2	2.81	11	11.23
3	3.99	13	12.82
5	6.13	15	14.28
7	7.62		

Table 3.3 *Extracted TLM parameters*

R_C (Ω)	L_T (μm)	R_{SH} (Ω/□)	ρ_C(Ω μm^2)
0.67	0.60	26.52	10.15

3.5 Summary

In this chapter, the fabrication steps required for manufacturing of the passive components (thin-film and semiconductor resistors, MIM capacitors, coplanar waveguide) were detailed. The characteristics of the passive components were analyzed using S-parameter measurements that showed that at the frequency of interest (30 GHz) their behavior is as expected. The metal-semiconductor contact resistance was also investigated by LTLM test structures. The obtained resistance is one order of magnitude higher than the lowest reported in literature and is expected to be reduced by optimizing the surface treatment process before metallization.

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Chapter 4. Resonant Tunneling Diode Bias Circuit Instabilities

4.1 Introduction

Many of the proposed applications of Resonant Tunneling Diodes (RTDs) such as transceivers [1]-[3] and digital logic circuits [4]-[6] make use of the negative differential resistance region (NDR) exhibited by the device. Therefore, accurate DC and high frequency characterisation of this critical region is essential for device modelling in computer simulations [7]. However, instability in the NDR can negatively affect the diode's performance, in terms of output power, when used as an oscillator [1] and reduces the dynamic input range when operated as a receiver [2]. In this chapter, the parasitic oscillations as a result of the biasing network are studied. The basic differential equations for a typical RTD circuit are deduced and the stability criteria is derived. This chapter presents a systematic study on the influence of bias circuit oscillations on the measured DC characteristics of an RTD.

The typical measured current-voltage (*I*-*V*) characteristics of a single RTD device is shown in Fig. 4.1. Due to the presence of parasitic oscillations, the *I*-*V* curve shows a plateau-like feature, which has been extensively observed in literature [8]-[12], where it has been attributed to both intrinsic and extrinsic factors. In [9] the authors have explained how the coupling between the energy levels in the emitter well and in the main quantum well can result in a plateau-like structure that is seen in DC measurements, an intrinsic behaviour of their epi-layer structure design. By applying a magnetic field perpendicular to the tunnel barriers, the in-plane motion of electrons is quantized into discrete energy levels, known as Landau levels. The experimental measurements showed that the width of the plateau region decreased with respect to an increasing magnetic field, and finally disappeared at a magnetic field strength of around 8 Tesla (T) [9]. Extrinsic factors, more relevant to the current work, are attributed to the resonance between the RTD self-capacitance and the parasitic resistance and inductance present due to the biasing cables. Since reducing and/or eliminating the parasitics beyond a certain point is not feasible, various techniques need to be employed in order to maintain DC stability [12].

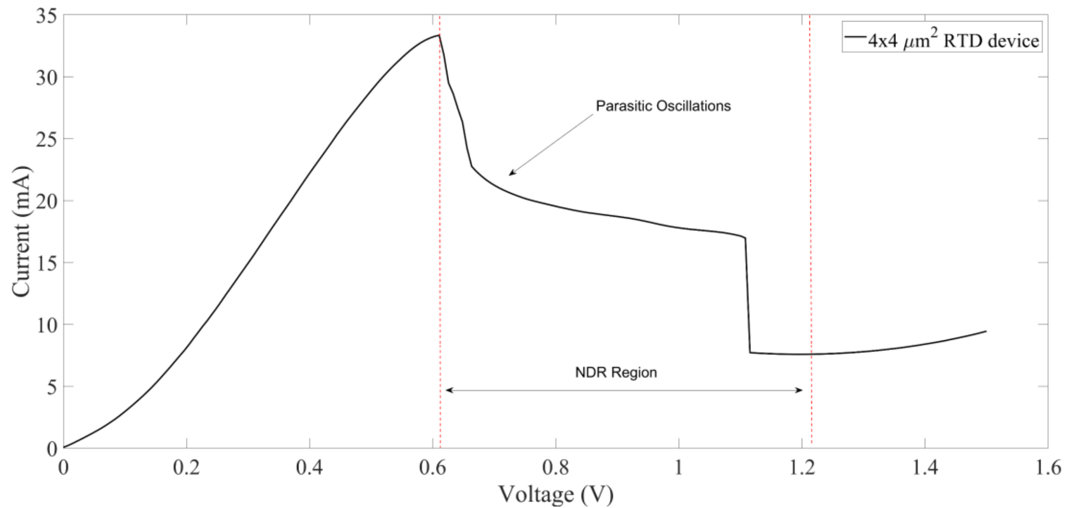


Figure 4.1: *DC measurement of a 4x4 µm² RTD device. The negative differential resistance (NDR) region is located between 0.6 V and 1.2 V. The diode shows a signature plateau-region within the NDR due to parasitic oscillations.*

This chapter is organized as follows. Section 4.2 presents the two RTD epi-layer structure designs used in this project as well as their DC characteristics with no bias stabilisation network. In Section 4.3, the main RTD models referenced in literature are analysed and the small-signal circuit parameter extraction discussed. Section 4.4 focuses on the stability criteria, based on the models discussed in the previous section and a new method to overcome the DC-instability is proposed. Numerical calculations, simulations and experimental data are presented in Section 4.5

4.2 RTD Layer Structure

Semiconductor film growth has benefited from modern epitaxial layer growth techniques such as metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE). Both techniques are able to grow high quality semiconductor materials with precise control over composition and thickness [13]. The wafers in this project were grown using MBE by IQE Ltd on a semi-insulating InP substrate. The two RTD layer structures that were used in this project are presented in Table 4.1.

Table 4.1: *RTD epi-layer design structures used in this project.*

Layer No.	Layer Structure #1 Wafer China Wafer			
	Thickness (A)	**Composition**	**Doping**	**Description**
1	450	$In_{0.53}Ga_{0.47}As$	3E19: Si	Collector
2	800	$In_{0.53}Ga_{0.47}As$	3E18: Si	Sub-Collector
3	500	$In_{0.53}Ga_{0.47}As$	5E16: Si	Spacer
4	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
5	11	AlAs	Un-doped	Barrier
6	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
7	14	InAs	Un-doped	Sub-Well
8	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
9	11	AlAs	Un-doped	Barrier
10	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
11	500	$In_{0.53}Ga_{0.47}As$	5E16: Si	Spacer
12	800	$In_{0.53}Ga_{0.47}As$	3E18: Si	Sub-Emitter
13	200	InP	1E19: Si	Etch-Stop
14	4000	$In_{0.53}Ga_{0.47}As$	3E19: Si	Emitter
15	2000	InP	Un-doped	Buffer
		SI: InP		Substrate

Layer No.	Layer Structure #2 Wafer Baseline2			
	Thickness (A)	**Composition**	**Doping**	**Description**
1	400	$In_{0.53}Ga_{0.47}As$	3E19: Si	Collector
2	800	$In_{0.53}Ga_{0.47}As$	2E18: Si	Sub-Collector
3	1200	$In_{0.53}Ga_{0.47}As$	5E16: Si	Spacer
4	100	$In_{0.53}Ga_{0.47}As$	2E16: Si	Spacer
5	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
6	25	AlAs	Un-doped	Barrier
7	47	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
8	25	AlAs	Un-doped	Barrier
9	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
10	100	$In_{0.53}Ga_{0.47}As$	2E16: Si	Spacer
11	100	$In_{0.53}Ga_{0.47}As$	5E16: Si	Spacer
12	800	$In_{0.53}Ga_{0.47}As$	2E18: Si	Sub-Emitter
13	4000	$In_{0.53}Ga_{0.47}As$	3E19: Si	Emitter
14	2000	InP	Un-doped	Buffer
		SI: InP		Substrate

Starting from the top for layer structure #1, a highly n-type doped contact layer is used as an interface between the metallization and the RTD structure, followed by a collector/emitter layer (depending on the bias polarity); graded spacer layers are added (with 5E16 doping to un-doped) and are used to increase the depletion region width, and thereby decreasing the diode's capacitance and increasing the cut-off frequency of the diode. The undoped spacer layers help reduce the diffusion of dopant impurities to the double quantum well structure. The quantum well is formed by an un-doped narrow band gap material ($In_{0.53}Ga_{0.47}As$; E_g = 0.71 eV) sandwiched between two un-doped wide band gap barriers (AlAs; E_g = 2.14 eV). A 1.4 nm sub-well (layer 7) was introduced in the epilayer structure to lower the resonant energy levels inside the quantum well [14], in order to reduce the peak voltage point (V_p). On the emitter side a 20 nm etch-stop layer was introduced in order to control the etch depth during wet/dry etching. The RTD *I-V* characteristics for the two different layer structures is shown in Fig. 4.2.

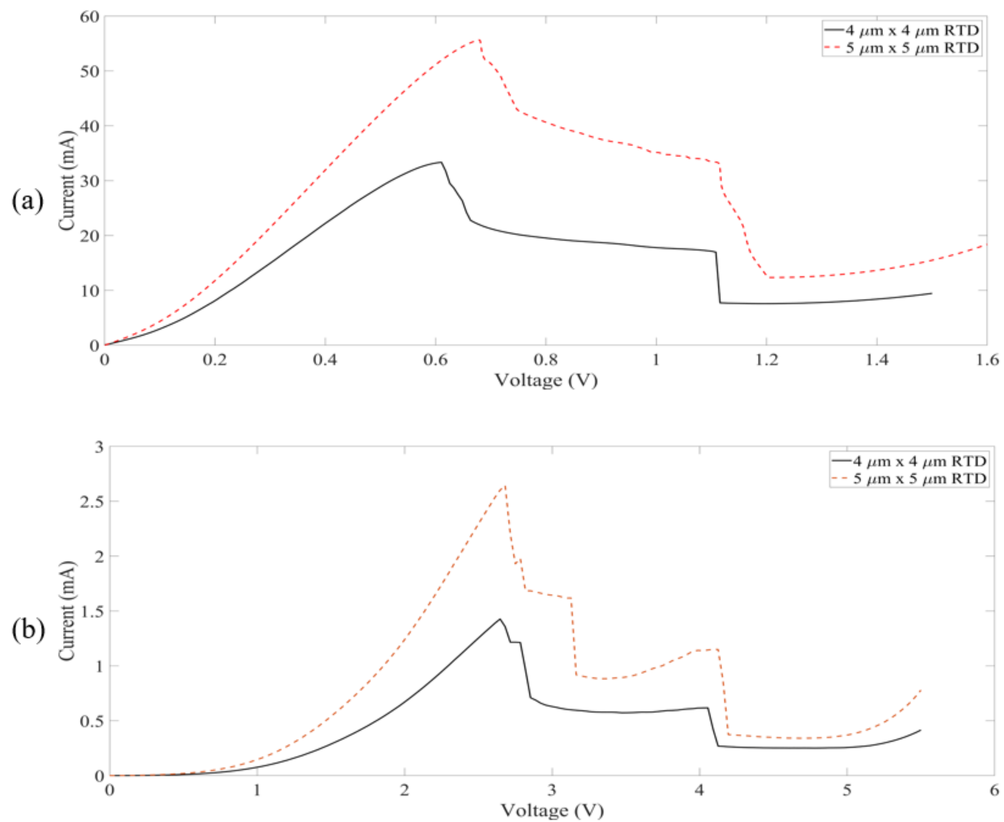


Figure 4.2: *RTD I-V characteristic of the two wafer structures used in this project: (a) layer structure #1, (b) layer structure #2*

4.3 Resonant Tunneling Diode Models

Various physical, analytical and semi-analytical models have been proposed to describe the RTD operation. An overview of the equivalent circuit models found in literature [15]-[21] indicate that most deal with the small-signal operation of the RTD. Several large-signal models of an RTD [22]-[25] derived from their small-signal parameters have been implemented into simulation programs with integrated circuit emphasis (SPICE) environments and are used in simulations. The theoretical identification of an accurate equivalent circuit for the RTD is important for:

i. The suppression of bias circuitry oscillations [12]
ii. Extraction of device characteristics from experimental measurements [7][26]
iii. Maximizing the power, frequency and efficiency of RTD oscillators [1]
iv. Understanding structural changes to the RTD which will lead to improved device characteristics [27]

4.3.1 RC Circuit Model

The simplest model is the small-signal equivalent RC circuit, based on the Esaki tunnel diode equivalent circuit [22], where the RTD is modelled as a resistor, with negative conductance $-G_n$ and capacitance C_n connected in parallel as shown in Fig. 4.3. The conductance G_n of the model is the differential conductance of the device. This conductance, which has a negative sign in the NDR region is obtained by differentiating the stable DC *I-V* curve of the device, as shown in Eq 4.1.

$$G_n = \frac{\Delta I}{\Delta V} \tag{4.1}$$

The capacitance C_n represents the parallel-plate capacitance formed due to the formation of depletion layers on the collector side. This geometrical capacitance can be estimated using Eq. 4.2, where A is the device size, L_W, L_B and L_D is the width of quantum well, barrier and depletion region respectively and ε_W, ε_B, and ε_D are their respective dielectric constants .

$$C_n = \frac{A}{\frac{L_W}{\varepsilon_W}+\frac{2L_B}{\epsilon_B}+\frac{L_D}{\epsilon_D}} \tag{4.2}$$

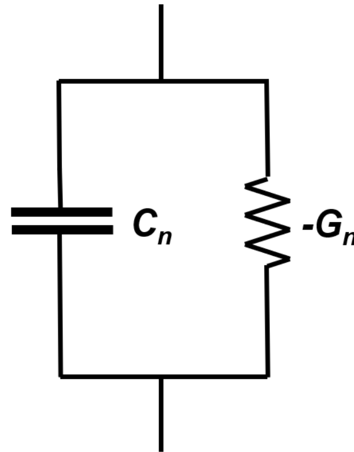


Figure 4.3: *RC small-signal circuit model for the RTD. The capacitance C_n represents the geometrical capacitance of the device. The conductance G_n is obtained by differentiating the stable I-V curve of the device.*

4.3.2 RLC Circuit Model

A more accurate small-signal equivalent circuit model of the RTD is based upon the parallel-inductance theoretical model, which was proposed by Brown et. al. [17]. The physical origin of the inductance is explained as follows:

At the interface between two different semiconductor materials a heterojunction is formed, band bending will then result in the formation of a triangular well. The formation of the triangular well creates a 2d electron gas (2DEG) population [28], in which the electrons occupy quasibound states. It was observed that, when the applied bias voltage is changed, the current inside the RTD takes time to reach its new value, implying that the RTD should have an inductive character.

In his letter, Brown derived that the inductive character is related to the quasibound state lifetime (Γ_d). The small-signal RLC model is shown in Fig. 4.4 with L_{qw} denoting the quantum well inductance.

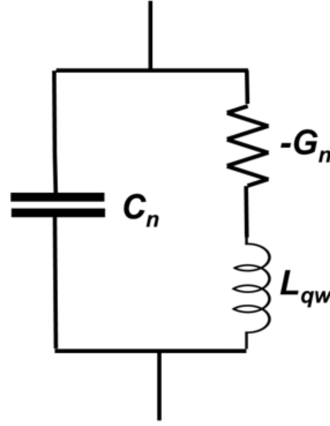


Figure 4.4: *RLC small-signal equivalent circuit model for RTD. The capacitance C_n represents the geometrical capacitance of the device. The conductance G_n is obtained by differentiating the stable I-V curve of the device.*

The RTD's capacitance (C_n) is composed of the device geometrical capacitance (C_0), which arises from the depletion layers, and the quantum well capacitance C_{qw}, originating from the change in charge in the quantum well [21].

$$C_n = C_0 + C_{qw} \tag{4.3}$$

The geometrical capacitance C_0 is the parallel plate capacitance formed by the undoped regions confined in the highly doped collector / emitter layers and is calculated using Eq. 4.2. The quantum well capacitance C_{qw} arises from the electron density change in the quantum well as a function of applied bias.

The charge variation has been derived by [21][29], where ΔQ_c is the charge variation seen in the collector as a result of the quantum well charge ($\Delta Q_c = -\Delta Q_w$) and is given by Eq. 4.4. The quantum well capacitance can also be expressed in terms of the RTDs differential conductance G_n and electron escape rate ν_c (s^{-1}).

$$C_{qw} = A\frac{\Delta Q_c}{\Delta V} = -\frac{G_n}{\nu_c} \tag{4.4}$$

The quantum inductance L_{qw} arises from the charging and discharging effect of the quantum well and is directly proportional to the electron dwell time (τ_{dwell}) in the quantum well during resonant tunneling [17][21]. This quantity changes exponentially with the thickness of the barrier and the electron effective mass in the barrier. The

electron dwell time is calculated using Eq. 4.5, where Γ is the energy full-width through the first resonant level. The frequency independent inductance can be thus estimated using Eq 4.6.

$$\tau_{dwell} = \frac{\hbar}{2\pi\Gamma} \tag{4.5}$$

$$L_{qw} = \frac{\tau_{dwell}}{G_n} \tag{4.6}$$

4.4 Bias Circuit Instabilities

A typical RTD device measurement setup is presented in Fig. 4.5 (a), where V_{bias} is the bias voltage, R_B and L_B are the parasitic resistance and inductance introduced by the biasing cable, L_d is the inductance of the on-chip coplanar waveguide (CPW) pad and R_d represents the device contact resistance.

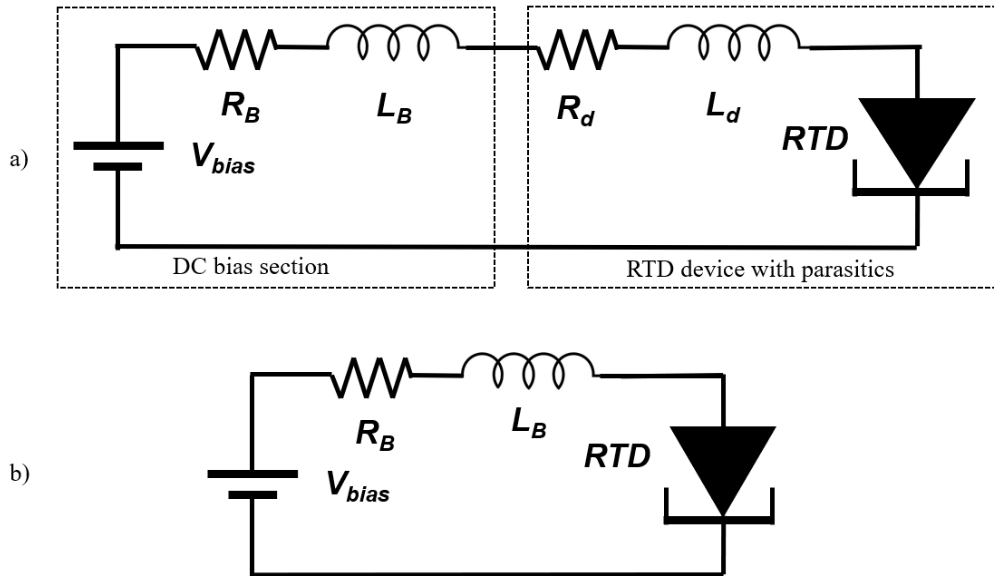


Figure 4.5: *(a) DC measurement setup of an RTD device including the bias circuit and device parasitics, (b) simplified equivalent circuit.*

The circuit present in Fig. 4.5 (a) can be simplified to the one in Fig. 4.5 (b), since all the parasitic elements are connected in series. Biasing the RTD in the NDR region using the measurement setup described in Fig. 4.5 (b) usually leads to unwanted bias oscillation. This is because the net resistance of the circuit is negative, assuming that the negative differential conductance is much greater than the parasitic elements

introduced. Increasing the series resistance R_B to be numerically larger than G_n will result in DC bistability [12][30].

4.4.1 Shunt Resistor Stabilisation

The main approach to stabilise an RTD found in literature is to connect a stabilising resistor R_{shunt} across the device as shown in Fig. 4.6 [31]-[33], which ensures that the combined resistance of the circuit remains positive when biased in the NDR region.

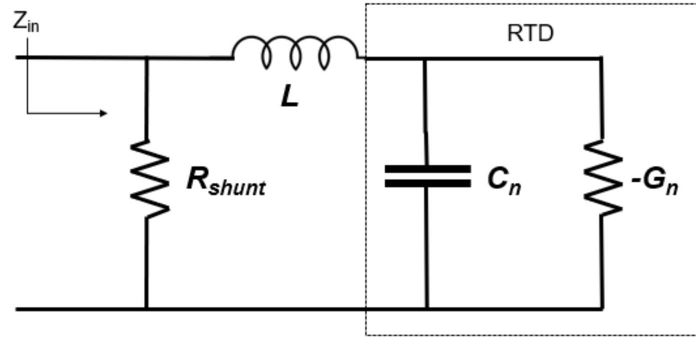


Figure 4.6: Circuit for stabilising the RTD using a parallel resistance (R_{shunt}) across the device. L denotes the parasitic inductance. C_n is the diode capacitance and -G_n is the negative differential conductance. The device contact resistance has been omitted.

Looking into the circuit the real part of admittance is given by Eq. 4.7

$$Re(Y_{in}) = \frac{1}{R_{shunt}} - G_n \frac{1}{(1-\omega^2 LC_n)^2 + (\omega LC_n)^2} \tag{4.7}$$

At low frequencies ($\omega \approx 0$) the equation can be simplified as shown in Eq. 4.8. In order to suppress low frequency oscillations, the real part of the admittance must remain positive [31][32].

$$Re(Y_{in}) = \frac{1}{R_{shunt}} - G_n > 0 \tag{4.8}$$

$$R_{shunt} < \frac{1}{G_n} \tag{4.9}$$

The shunt resistor stabilisation method is the most widely used to date, however, there are significant drawbacks when used in circuits.

i. the dc characteristics of the diode must be indirectly determined by firstly de-embedding the resistor from measurements [31].
ii. the DC-to-RF conversion efficiency is greatly reduced due to a dc path to ground through the usually low value resistance [1].
iii. the sensitivity of the diode is affected when operated as a receiver [34].

4.4.2 Shunt Capacitor and Resistor Stabilisation

The RTD bias stabilisation network approach proposed in this work employs the addition of a shunt capacitor C_B connected in series with the stabilising resistance, to eliminate the dc path to ground [1]. The circuit is shown in Fig. 4.7, where V_{bias} is the bias voltage to set the device in the NDR region, R_S and L_S are the resistance and inductance introduced by the biasing cable, R_B and C_B are the shunt resistor and capacitor, respectively, and L is the series inductance of the contact pads of the device.

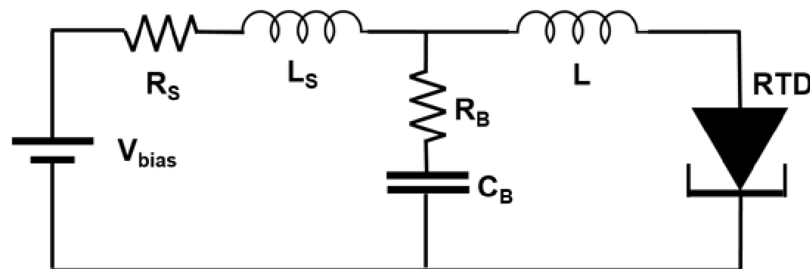


Figure 4.7: *Circuit for stabilising the RTD using a parallel resistance (R_B) and capacitance (C_B) across the device.*

For the analysis, the circuit presented in Fig. 4.7 is split into the low frequency and high frequency equivalents. At low frequencies (MHz range), the circuit in Fig. 4.7 can be simplified to the equivalent circuit in Fig. 4.8 (a), where the RTD is represented by its negative differential conductance ($-G_n$) and self-capacitance (C_n).

In this case, the inductance L is considered a short circuit, the shunt resistance R_B is ignored, as the impedance of capacitor C_B becomes dominant at low frequencies, and

the device capacitance C_n (typically tens of femtofarads) is considered negligible when compared with C_B (typically tens of picofarads).

On the other hand, at high frequencies (GHz range), the circuit in Fig. 4.7 can be simplified to the equivalent circuit in Fig. 4.8 (b), where the inductance L_B is considered an open circuit and the capacitance C_B is a short circuit. Note that the circuits in Fig. 4.8 are identical, only with different element values representing their low and high frequency variants.

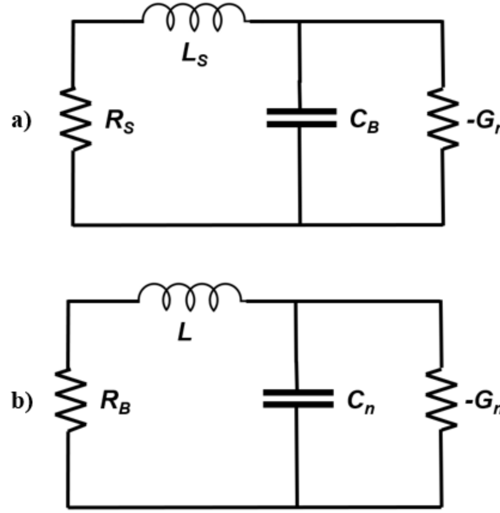


Figure 4.8: *(a) Simplified low frequency equivalent circuit, (b) simplified high frequency equivalent circuit.*

We analyse the circuit in Fig. 4.8 (a) using nodal analysis by applying Kirchhoff's current law to give:

$$\frac{V}{R_S+sL_S} + sC_BV - G_nV = 0 \tag{4.10}$$

where V is the voltage across the parallel circuit and s the complex frequency. From (4.10), we can obtain the following characteristic equation:

$$C_BL_Ss^2 + (C_BR_S - L_sG_n)s + 1 - G_nR_s = 0 \tag{4.11}$$

The solutions to (4.11) are given by:

$$s_{1,2} = \frac{(L_SG_n - C_BR_S) \pm \sqrt{(C_BR_S - L_SG_n)^2 - 4C_BL_S(1 - G_nR_S)}}{2C_BL_S} \tag{4.13}$$

The solutions of Eq. 4.13 can be classified as real or complex. Case 1: the solutions are complex and therefore:

$$(C_B R_S - G_n L_s)^2 - 4C_B L_s(1 - G_n R_s) < 0 \qquad (4.14)$$

For the circuit to be stable, the solutions of (4.14) must fall on the left half of the complex frequency plane. As a result, the circuit is stable if:

$$C_B > \frac{L_S G_n}{R_S} \qquad (4.15)$$

Case 2: the solutions are real and so:

$$(C_B R_S - G_n L_s)^2 - 4C_B L_s(1 - G_n R_s) > 0 \qquad (4.16)$$

For these solutions to fall in the left half of the complex frequency plane the magnitude of the term under the square root sign of (4.13) must be smaller than the magnitude of the first term, so:

$$R_s < \frac{1}{G_n} \qquad (4.17)$$

Combining the conditions derived from case 1 and 2, the condition to achieve low frequency circuit stability is:

$$\frac{L_S G_n}{C_B} < R_s < \frac{1}{G_n} \qquad (4.18)$$

Since the circuits of Fig. 4.8 (a) and Fig. 4.8 (b) are identical, equation (4.18) can be re-written with the corresponding elements to provide the condition for stability at high frequencies as:

$$\frac{L G_n}{C_n} < R_B < \frac{1}{G_n} \qquad (4.19)$$

4.5 Measurement Results and Simulations

To determine the efficacy of the proposed bias stabilisation approach, devices on the two different layer structures were fabricated using optical lithography techniques. The diodes where then characterised using DC and RF measurements in order to extract the parameters, G_n, L_{qw} and C_n, as a function of the bias voltage. An accurate large-signal model of the RTD's equivalent circuit could then be established and the

stabilising networks tested. RTD's with integrated stabilising networks were then designed, fabricated and measured. The fabrication process details are described in chapters 3 and 4.

4.5.1 DC Measurements

A diagram of the DC measurement set up is shown in Fig. 4.9 and it consists of the Keysight technology B1500 to supply the bias voltage, the bias tee, the DUT and the spectrum analyser/oscilloscope to measure any parasitic oscillations.

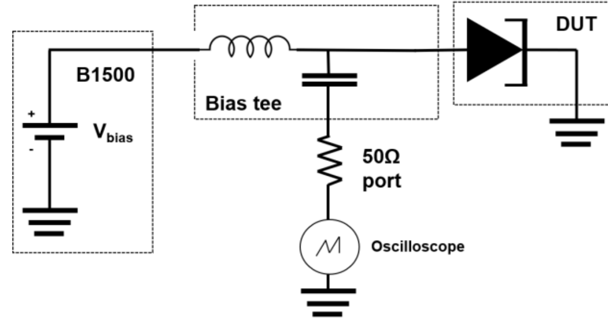


Figure 4.9: *DC measurement set-up for an RTD device. A spectrum analyser/oscilloscope is used to measure the parasitic oscillations.*

The measured *I-V* characteristic of a fabricated device is shown in Fig. 4.10. The *I-V* presents the typical plateau-like feature in the NDR region due to the presence of parasitic oscillations during measurement. Without a working stabilising network to extract the true characteristics of the device, the data points extracted from the DC measurements in the NDR are inaccurate and must be discarded. In order to calculate the differential conductance, a large-signal analytical model [25] is used to reconstruct the I-V characteristic, with the NDR approximated with a smooth trace.

From the described model in [25], the RTD I-V is given by:

$$I(V) = S \times \left(J_{exp}(V) + J_{Gaussian}(V) + J_{mod}(V)\right) \quad (4.20)$$

where

$$J_{exp}(V) = A(\exp(B \times V) - \exp(-B \times V)) \quad (4.21)$$

$$J_{Gaussian}(V) = C1(\exp(-\mathrm{D1} \times (V - E1)^2 - \exp(-D1 \times (V + E1)^2) \quad (4.22)$$

$$J_{mod}(V) = C2(tan^{-1}(D2 \times (V - E2)) + tan^{-1}(D2 \times (V + E2))) \quad (4.23)$$

The parameters of the equation A, B, C, D, and E are used to achieve the different RTD I-V characteristics and S represents the scaling factor. The parameters are extracted using a curve fitting tool in MATLAB. The resulting spline is continuous and using (4.1) the negative differential conductance is computed and plotted on the right-axis of Fig. 4.10.

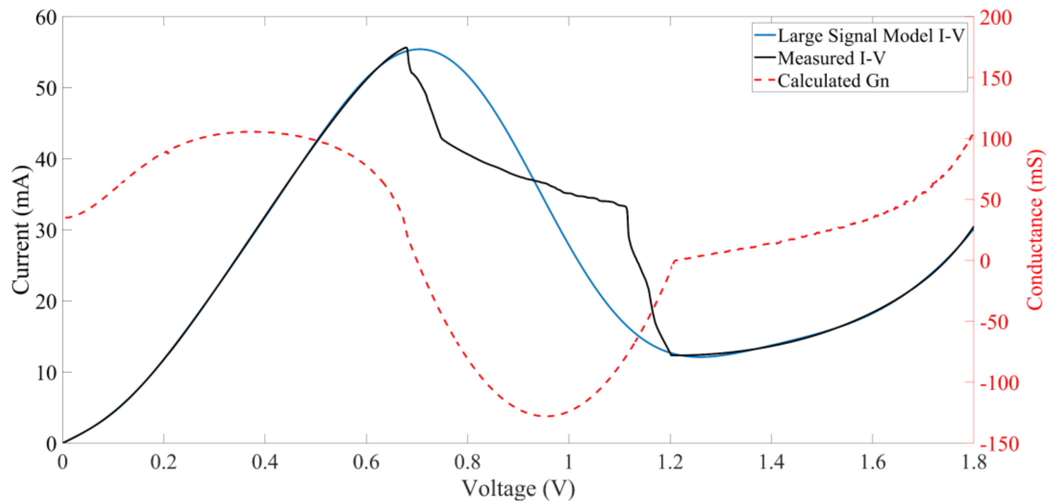


Figure 4.10: *Measured I-V characteristic of an RTD device (black), large-signal model of the I-V characteristic with the NDR approximated with a smooth trace (blue), calculated value of conductance of model I-V (red).*

The extracted model parameters are:

A = 0.9623 A/m^2, B = 0.0945 V^{-1}, C1= 0.1362 A/m^2, C2 = -0.2847 A/m^2, D1 = 6.351 V^{-2}, D2 = 0.3915 V^{-1} , E1 = 0.6744 V, E2 =-0.2612 V

The large-signal model provides a good fit to the measured data, able to reproduce the RTD's PDR regions. The NDR is an approximate and should be sufficiently accurate to calculate G_n. Using the same setup as described in Fig. 4.9, the parasitic oscillations were measured by a spectrum analyser and are presented in Fig. 4.11. The frequency of oscillation is around 3.25 MHz.

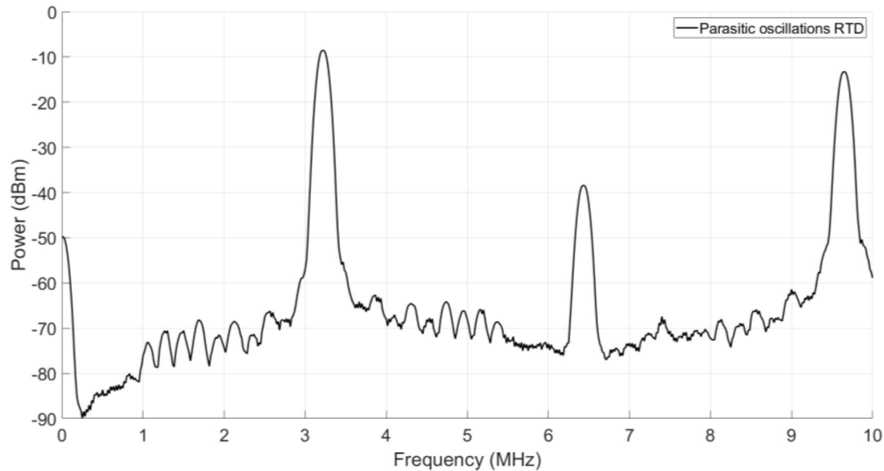


Figure 4.11: *Low frequency oscillations of the RTD measured by a spectrum analyser.*

4.5.2 RF Measurements

For the purpose of accurate parameter extraction, S-parameter measurements were carried out at different bias points in the positive differential regions using a Keysight E8361A vector analyser (VNA) with a port power of -20 dBm together with a Keysight 1500A device parameter analyser. The signal from the VNA and the bias voltage were both fed using a 100 µm co-planar ground-signal-ground (GSG) probe using a bias tee. The measurement setup is similar to the one presented in Fig. 4.8, with the VNA replacing the oscilloscope.

An initial short-open-load (SOLT) calibration was performed to eliminate systematic errors and move the measurement reference point to the tips of the probe. The Cascade Microtech standard substrate was used for the short, thru and 50 Ω precision load standard. The open standard was done by lifting the probe tips in the air [35].

The effects of the parasitic elements originating from the pad structures of the RTD have been de-embedded after measurements by including open and short dummy pad test structures on the wafer substrate. The full details on the de-embedding procedure is detailed in [7] and a micrograph of the dummy pad structure is shown in Fig. 4.12.

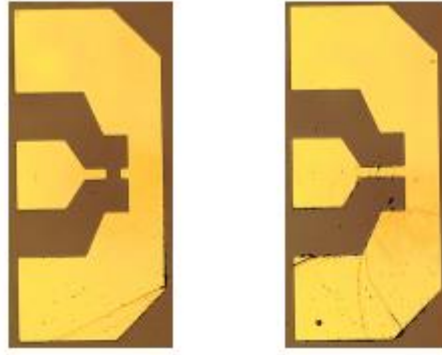


Figure 4.12: *Micrograph of open and short dummy pad structures used for de-embedding of the parasitic elements originating from the CPW pads.*

Fig. 4.13 shows the measured and fitted values for the real and imaginary part of S11. The frequency span for the measured data was 10 MHz to 110 GHz, however around 20 GHz the system had a resonance and no data could be extracted. A schematic model of the small signal parameters R_s, L_{qw}, G_n and C_n was created in Keysight Advanced Design System (ADS) software, where, the circuit elements are extracted by adjusting the simulated model circuit to the measured results. The contact resistance R_s was extracted using transmission line method (TLM) measurements and the process was described in Chapter 3.

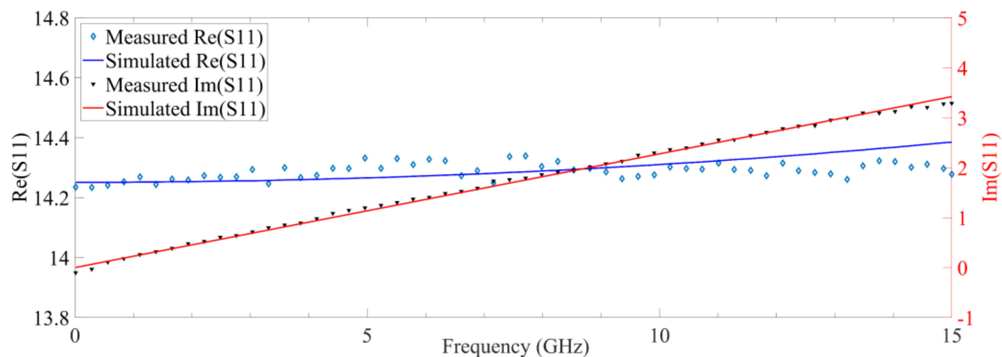


Figure 4.13: *Measured and simulated real and imaginary parts of S11 after de-embedding the parasitics at 0.1 V bias voltage. No data could be extracted above 15 GHz as the RTD and the pads were in resonance.*

The process was carried out in the microwave frequencies range at several bias points in the first and second PDR regions. No data could be extracted in the NDR due to not having a device bias stabilization method. Using the extracted values for the inductance at several bias points the experimental value of the time constant τ is

obtained from the extracted parameters and is estimated at 2.65 ps. This estimation is reasonable, with the experimental value being matched when considering 1.2 nm barrier thickness in the calculation. Using (4.6) the model for the device inductance is presented in Fig. 4.14.

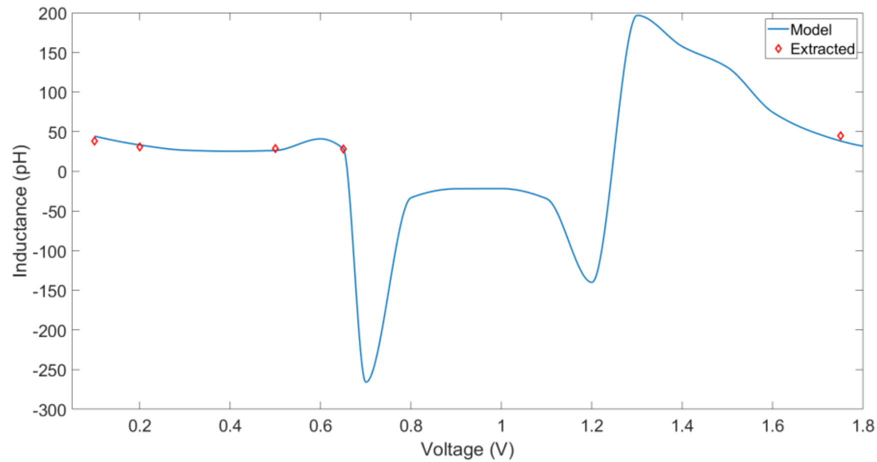


Figure 4.14: *Extracted values for the device inductance (red), model of the device inductance obtained (blue)*

The device capacitance C_n is composed of the geometrical capacitance and the quantum well capacitance. The geometrical capacitance estimated using Eq. 4.2 is about 21 fF with a device area of 5x5 μm^2. The quantum well capacitance can then be calculated by subtracting the geometrical capacitance from the measured data. Using Eq 4.3 the electron escape rate from the quantum well to the collector is calculated at 0.1 ps and the capacitance variation with bias is plotted in Fig. 4.15.

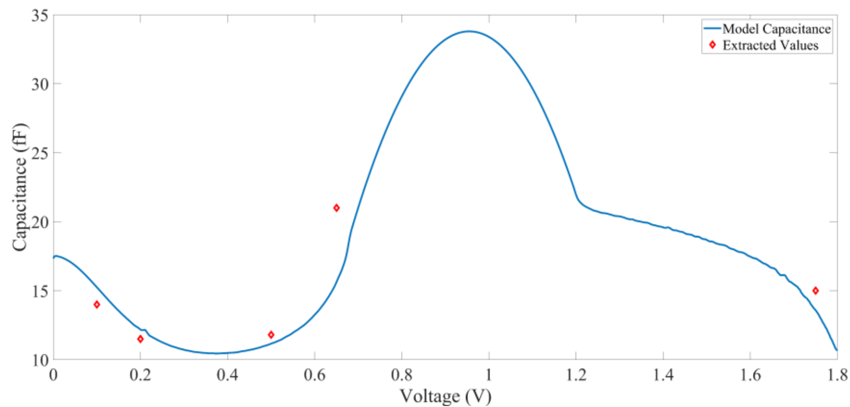


Figure 4.15: *Extracted values for the device capacitance (red), model of the device capacitance obtained (blue)*

4.5.3 Simulation Results

Based on the extracted parameter values, a MATLAB large-signal model of the RTD was realized and can be seen in Fig. 4.16. The lumped elements L_{qw}, C_n and G_n represent the quantum inductance (RLC) model. $R_{contact}$ represents the device contact resistance and was set to be 5 Ω, G_n was modelled as a variable resistance, L_{qw} and C_n as custom blocks with the values based on the model inductance and capacitance described previously. The lumped elements R_s (0.1Ω) and L_s (56 nH) represent the bias cable resistance and inductance respectively.

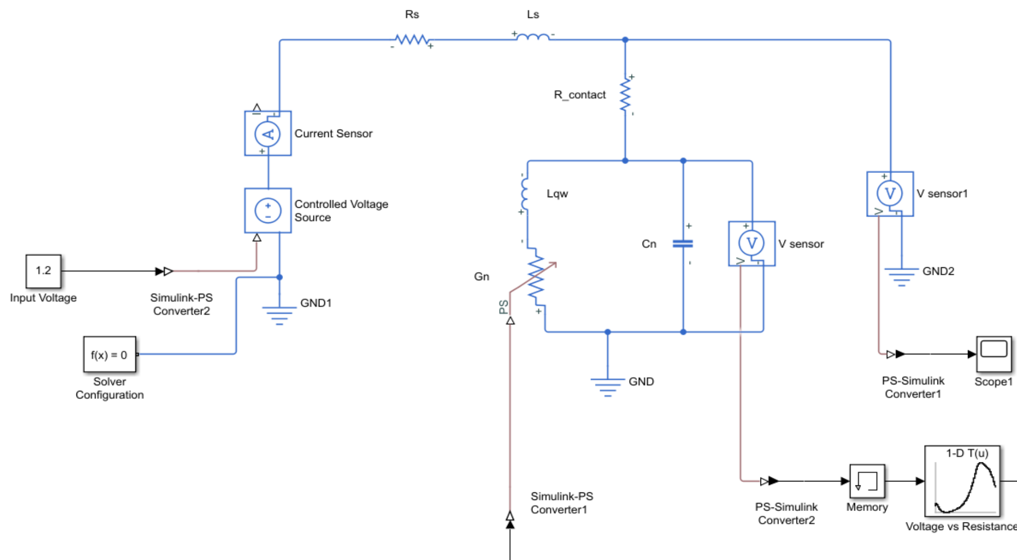


Figure 4.16: *MATLAB Simulink large-signal model of RTD measurement setup. The negative differential resistance has been modelled as a variable resistance with the values extracted from the DC large-signal model of the RTD (Fig. 4.10). The inductance and capacitance have been modelled using custom block with their values extracted from Fig. 4.14 and Fig. 4.15, respectively.*

The input voltage was increased in the time-domain simulation at fixed intervals and current measurements were recorded in-between voltage changes. The RMS current value at a specific voltage level could then be calculated. When biased in the NDR the circuit oscillated, and a plateau-like region was observed when calculating the RMS current value at each biasing condition. The model and the measurement data are presented below with good agreement, however the model's NDR region extends 100mV more than the measured RTD device and is attributed to inaccuracies

introduced by the large signal model. As a result, the parasitic oscillations are sustained until 1.3V.

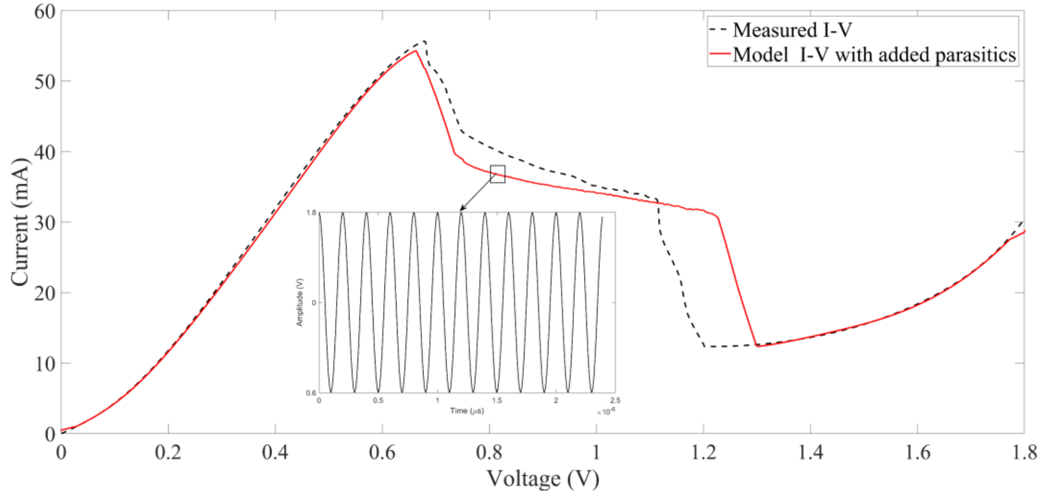


Figure 4.17: *Measured I-V characteristic of an RTD device (black), Simulated MATLAB model of DC measurement setup with added extrinsic parasitic elements (red).*

The MATLAB model was then modified to include the proposed stabilisation network. Based on the model the values for the stabilising network required are R_B = 10 Ω and C_B = 144pF. The requirements on L_S and C_B could be relaxed by using an additional small series resistance R_s, which can then be de-embedded from the measurements. The simulations show that with the addition of the stabilisation network no parasitic oscillations are present in the device, and the *I-V* characteristic matches the large-signal model *I-V*.

4.5.4 Experimental Results

To demonstrate the feasibility of the stabilisation network, RTDs with monolithically integrated bias resistors and capacitors were fabricated on the two different layer structures. A micrograph of a fabricated 4x4 μm^2 RTD with integrated stabilisation network is shown in Fig. 4.18, where the capacitor C_B (144 pF) and resistor R_B (10 Ω) are each realized from two parts placed in parallel with the device. The value for the stabilising network is chosen to satisfy both Eq. (4.18) and (4.19).

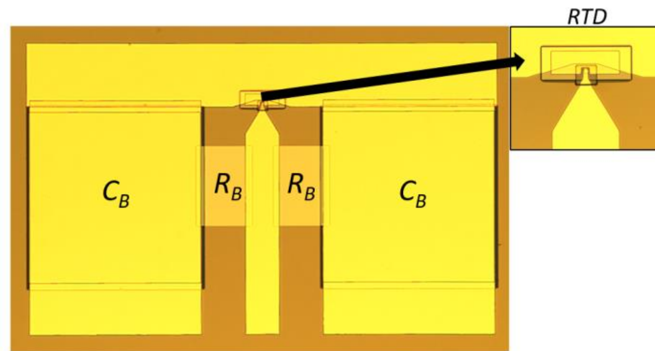


Figure 4.18: *Micrograph of a fabricated 4x4 RTD device with integrated bias stabilisation. The capacitor C_B and resistor R_B are comprised of two parts connected in parallel with the RTD device.*

Using the same measurement setup as described in Fig. 4.9 the frequency spectrum of the RTDs in the NDR region was analysed and shown in Fig. 4.19. For the R and RC stabilisation network the 3 MHz bias oscillation has been removed, and no other high frequency oscillations were observed beyond 10MHz.

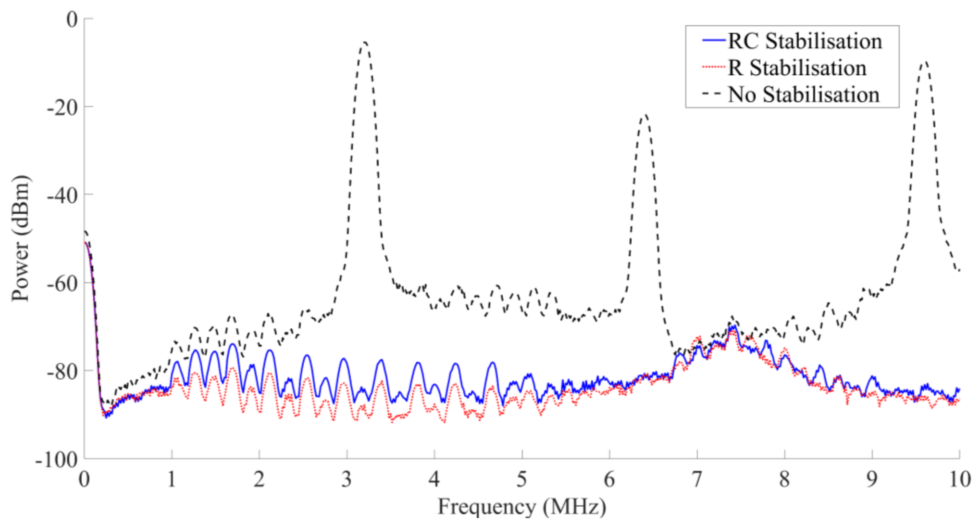
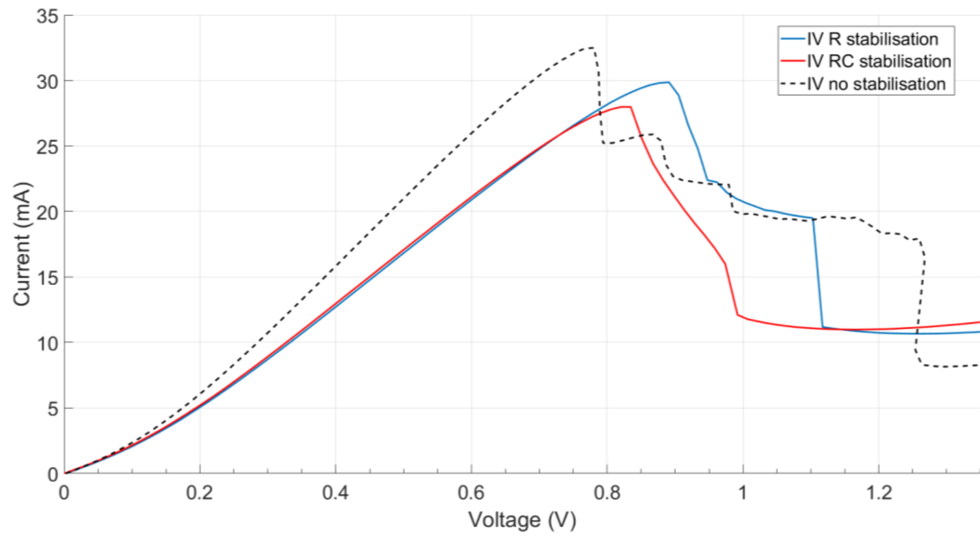


Figure 4.19: *Frequency spectrum of RTDs with different stabilisation networks.*

The RTD *I-V* characteristics for the two different RTD structures is presented in Fig. 4.20. For the RTD in Fig. 4.20 (a) the plateau region can be seen in both the device with no stabilisation and the R stabilisation method. The RC stabilisation I-V still presents a small plateau-region; however, it is believed that it's the result of the coupling between energy levels in the emitter well and in the main quantum well [9]. For the RTD shown in Fig. 4.20 (b) both stabilisation networks have resulted in similar

I-V characteristics with the small distortions of the R stabilisation network attributed to small errors in the de-embedding process of the resistor.



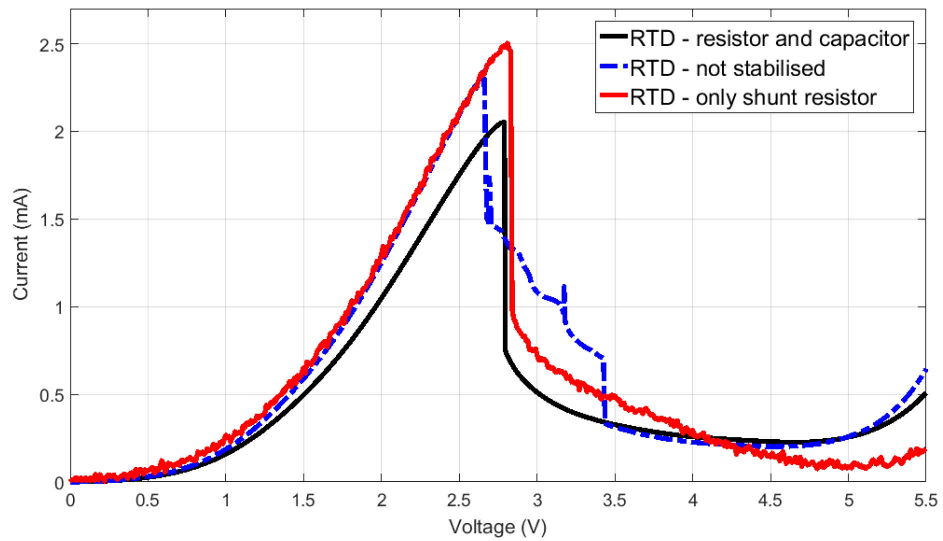


Figure 4.20: *RTD I-V characteristics: (a) 4x4 μm^2 RTD I-V with and without bias stabilisation based on wafer #1,(b) 4x4 μm^2 RTD I-V with and without bias stabilisation based on wafer #2*

The experimental results show that both the bias circuits eliminate parasitic oscillations associated with the biasing network. Compared with the shunt resistor stabilisation network, the RC method would eliminate the need of de-embedding the shunt resistance and improve the DC-to-RF conversion efficiency of the RTD oscillators by removing the dc path to ground through the usually low value resistance, typically ~10 Ω.

4.6 Summary

In this chapter the origin of the resonant tunneling diodes plateau region has been investigated. Design equations for an RTD biasing circuit that prevents parasitic oscillations in the NDR region has been derived, based on the discussed models. The design approach used in this work eliminates both low-frequency bias oscillations and high-frequency oscillations, which would hinder oscillator performance and increase the DC-to-RF conversion efficiency. The measured frequency spectrum of the stabilised RTDs confirms the validity of the design criteria.

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Chapter 5. Resonant Tunneling Diode Based Oscillators

5.1 Introduction

As described previously in Chapter 1, devices which exhibit negative differential resistance (NDR) can be used to realize RF sources. This chapter describes and presents RTD based oscillator topologies and adapts the proposed stabilisation method discussed in Chapter 4 to increase the DC-to-RF conversion efficiency of an oscillator circuit. The derivation of the theoretical maximum output power and cut-off frequency for an RTD oscillator is also presented.

The RTD oscillators in this project were designed for on-wafer characterization. The spectrum analyzer used in this project was the E4448A spectrum analyzer from Agilent Technologies, which can measure frequencies up to 50 GHz. For higher frequency measurements an external mixer is used to down-convert the frequency. The measurement setup for RF oscillators is shown in Fig. 5.1.

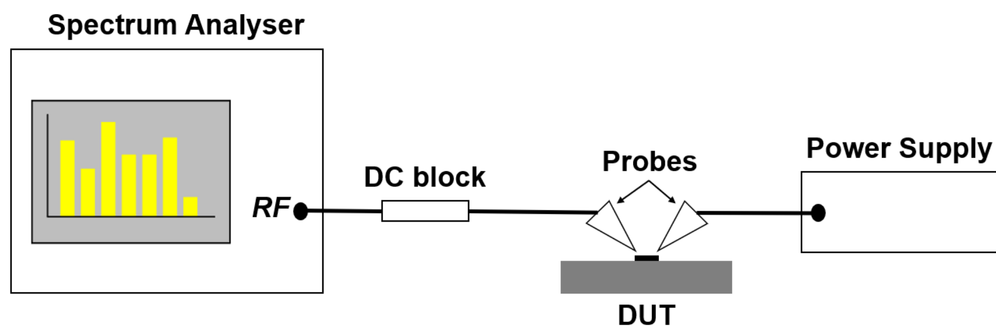

Figure 5.1: *Schematic block diagram used for on-wafer frequency measurements using a spectrum analyser. Biasing of the device is done through a ground-signal-ground (GSG) probe, an external DC block capacitor is used when not incorporated on-chip.*

This chapter is organized as follows: Section 5.2 describes the various performance metrics of RTD-based oscillator circuits, including the expected radio frequency (RF) power generated. Section 5.3 covers the conventional RTD oscillators as well as the high-efficiency design and compares them based on their respective figure-of-merits (FOM). A comparison between RTD-based voltage-controlled oscillators (VCOs) and other published oscillators in the same frequency range is also presented.

5.2 Characteristics of RTD oscillator

5.2.1 Maximum RF Power

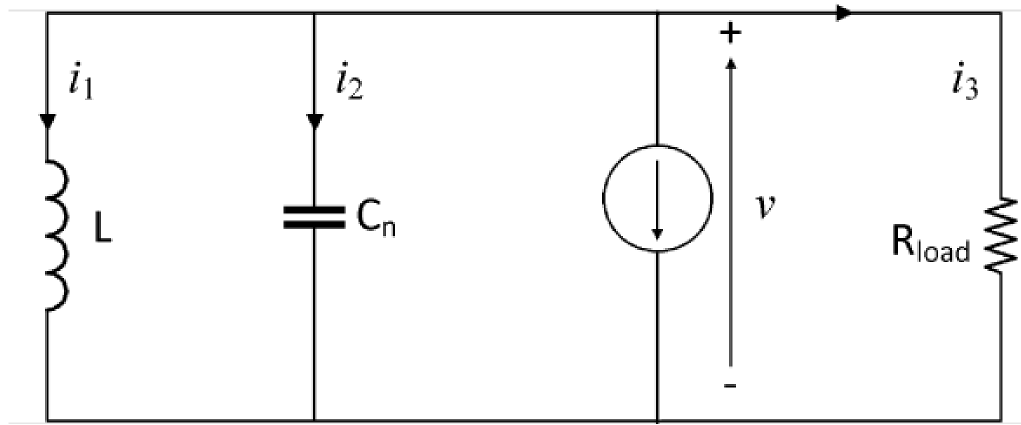

Figure 5.2: *RF large-signal equivalent circuit of an RTD based oscillator with the RTD represented by a voltage controlled current source I = f(V) and self-capacitance C_n. L represents the resonating inductor and R_{load} is the load resistance.*

The RF equivalent circuit of an RTD based oscillator is shown in Fig. 5.2, where the RTD is replaced by its large signal model, consisting of a voltage controlled current source and self-capacitance (C_n) [1]. For analytical purposes the voltage controlled current source $I = f(V)$ when biased in the NDR can be represented by a cubic polynomial [2]-[4] as shown in Eq. 5.1, where a and b are constant positive coefficients associated with the particular device, $a = (3\Delta I/2\Delta V)$ and $b = (2\Delta I/\Delta V^3)$.

$$I(V) = -aV + bV^3 \tag{5.1}$$

By applying Kirchhoff's current, the currents in the circuit can be expressed as $i_1 + i_2 + i_3 + i = 0$, or

$$\frac{1}{L}\int v\,dt + C_n\frac{dv}{dt} + \frac{v}{R_{load}} + (-av + bv^3) = 0 \tag{5.2}$$

by differentiating with respect to time Eq. 5.2 can be re-written as

$$\frac{v}{L} + C_n\frac{d^2v}{dt^2} + \left(\frac{1}{R_{load}} - a + 3bv^2\right)\frac{dv}{dt} = 0 \tag{5.3}$$

And can be re-arranged as shown in Eq. 5.4, where $G_{load} = 1/R_{load}$

$$LC_n\frac{d^2v}{dt^2} + L(G_{load} - a + 3bv^2)\frac{dv}{dt} + v = 0 \tag{5.4}$$

Assuming that the voltage v is a sinusoidal signal, $v = V\cos(\omega t)$ where V is the amplitude of the signal and ω is the angular frequency given by $\frac{1}{\sqrt{LC_n}}$. The instantaneous power dissipated by the load can be described as

$$P_{load} = v^2 G_{load} = (V cos(\omega t))^2 G_{load} \tag{5.5}$$

by integrating Eq. 5.5 over one period the average power dissipated by the load can be written as

$$P_{avg_load} = \int_0^{2\pi} V^2 \cos(\omega t)^2 G_{load}\, dt = G_{load}\frac{V^2}{2} \tag{5.6}$$

Similarly, the instantaneous power over the RTD device is given by

$$P_{RTD} = -iv = av^2 - bv^4 \tag{5.7}$$

which, when integrating over one period will result the average power generated by the RTD device

$$P_{RTD_{avg}} = \int_0^{2\pi} a(\mathrm{V}\cos(\omega t))^2 - b(\mathrm{V}\cos(\omega t))^4 \, dt =$$

$$= \frac{aV^2}{2} - \frac{3bV^4}{8} \tag{5.8}$$

As the power generated by the RTD device is equal to the power dissipated over the load (5.6) and (5.8) can be combined, as shown in (5.9)

$$\frac{aV^2}{2} - \frac{3bV^4}{8} = G_{load}\frac{V^2}{2} \tag{5.9}$$

The solution for *V* in Eq. 5.9 is given by

$$V = 2\sqrt{\frac{G_n - G_{load}}{3b}} \tag{5.10}$$

By substituting (5.10) into (5.6), the average power dissipated over the load is then given by

$$P_{avg_load} = \frac{2(G_n - G_{load})G_{load}}{3b} \tag{5.11}$$

And when $G_{load} = Gn / 2$, the maximum theoretical output power delivered to the load (obtained by differentiating Eq. 5. 11 and equating to zero) is given by

$$P_{max} = \frac{G_n^2}{6b} = \frac{3}{16}\Delta I \Delta V \tag{5.12}$$

The maximum output power is proportional to the difference in peak-to-valley current ΔI and peak-to-valley voltage ΔV. A device with a larger area and hence a larger ΔI is needed in order to obtain a higher output power. For 4 µm × 4 µm and 5 µm × 5 µm devices fabricated on layer structure #1 (detailed in Chapter 4) the maximum RF power is 3.3 mW and 5.6 mW, respectively.

5.2.2 Effect of Parasitics on Maximum RF Power

In the derivation of output power presented in the previous section, the circuit model does not account for the resistive losses due to parasitics. The series contact resistance R_s and parasitic inductance L_s have a large impact on power delivery as the oscillation frequency of the circuit increases. The RF equivalent circuit in which the parasitic elements are also included is shown in Fig. 5.3 (a) [5][6]. This circuit can be re-drawn as shown in Fig. 5.3 (b) where the total equivalent impedance of the load Z_{total} is given by Eq. 5.13.

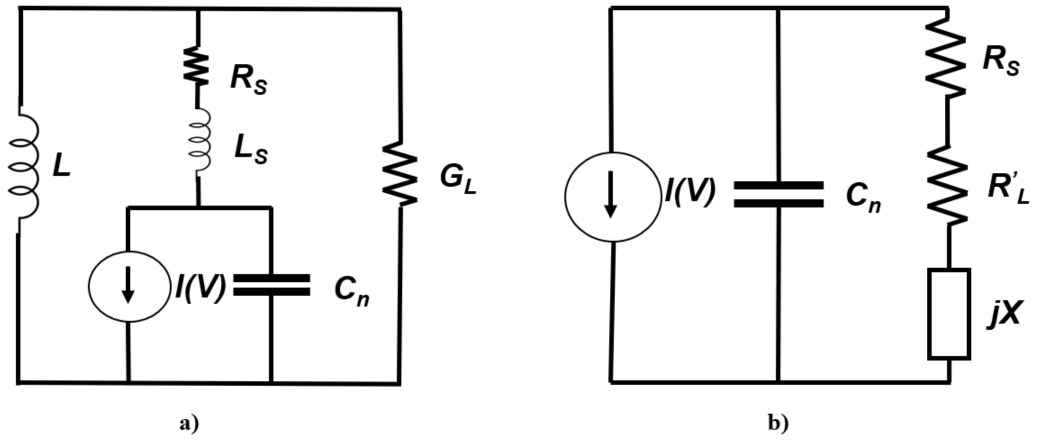

Figure 5.3: *(a) RTD large-signal model oscillator with parasitic resistance R_s and parasitic inductance L_s. (b) RF equivalent circuit of RTD large-signal model oscillator.*

$$Z_{total} = R_s + R_L' + jX \tag{5.13}$$

$$R_L' = \frac{\omega^2 L^2 G_L}{1+\omega^2 L^2 G_L^2} \tag{5.14}$$

$$X = \frac{\omega L}{1+\omega^2 L^2 G_L^2} + \omega L_s \tag{5.15}$$

The circuit shown in Fig. 5.3 (b) can be re-drawn in terms of admittance Y_{total} of the series resistance R_s, inductance L and load G_L as shown in Fig. 5.4.

$$Y_{total} = \frac{1}{Z_{total}} \tag{5.16}$$

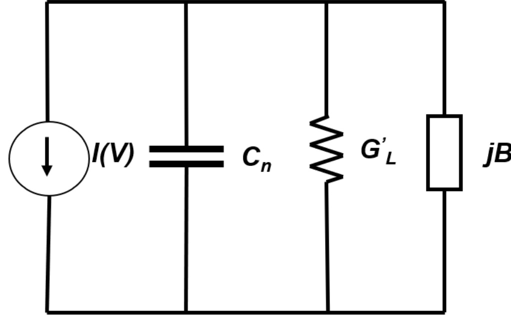

Figure 5.4: *RTD large-signal model oscillator with equivalent parallel load conductance G'_L and equivalent parallel susceptance B.*

By combining (5.13) – (5.16), the equivalent conductance G'_L and equivalent susceptance B can be described as

$$G_L' = \frac{R_S + \frac{\omega^2 L^2 G_L}{1+\omega^2 L^2 G_L^2}}{(R_S + \frac{\omega^2 L^2 G_L}{1+\omega^2 L^2 G_L^2})^2 + (\frac{\omega L}{1+\omega^2 L^2 G_L^2} + \omega L_S)^2} \tag{5.17}$$

$$B = \frac{\frac{\omega L}{1+\omega^2 L^2 G_L^2} + \omega L_S}{(R_S + \frac{\omega^2 L^2 G_L}{1+\omega^2 L^2 G_L^2})^2 + (\frac{\omega L}{1+\omega^2 L^2 G_L^2} + \omega L_S)^2} \tag{5.18}$$

Since the circuit presented in Fig. 5.4 is identical to that described in Fig. 5.2, the power delivered to the equivalent load is given by

$$P_{load} = \frac{2(G_n - G_L')G_L'}{3b} \tag{5.19}$$

Referring back to Fig. 5.3 the resistance R'_L is the apparent load resistance seen by the diode due to the external circuit components. Therefore, the power delivered to the load can be expressed as

$$P_{load} = \frac{2(G_n - G_L')G_L'}{3b} \frac{R_L'}{R_L' + R_S} \tag{5.20}$$

The apparent load G_L varies with frequency and therefore does not present an ideal load for maximum power, i.e. the output power drops when the oscillation frequency increases. For any given frequency, an optimum value for the RTD oscillator load G_L may be found.

For a 5 μm × 5 μm RTD oscillator on layer structure #1 with G_n = 150 mS, R_s = 0.6 Ω, L_s = 10 fH, L = 150 pH and b = 0.28, the simulated output power vs frequency is presented in Fig. 5.5. The simulations show that for a given RTD device an optimum frequency and load conductance exists. The analysis presented here is an upper limit to the maximum output power as it does not include the efects of the quantum well inductance L_{qw}, or the variation in conductance G_n and capacitance C_n with bias and frequency.

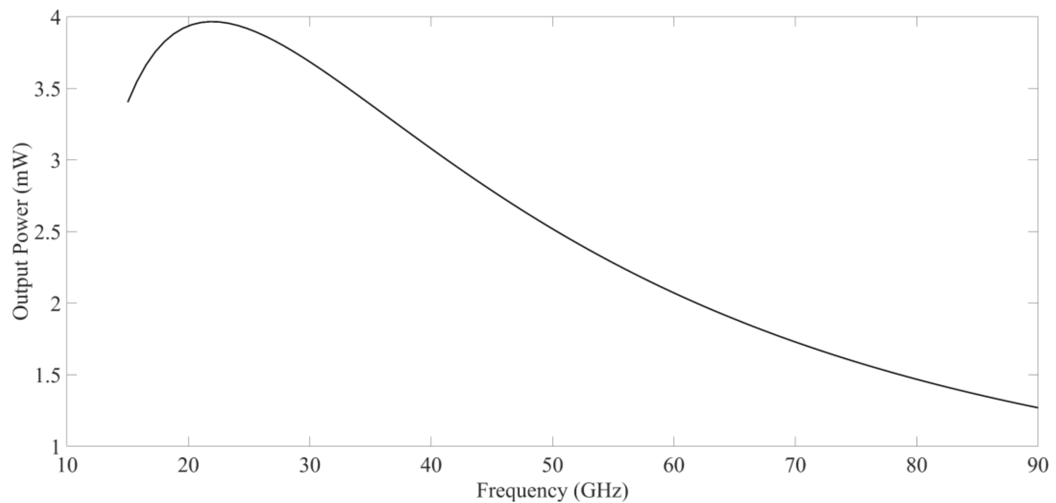

Figure 5.5: *Simulated output power as a function of frequency for a single 5 μm × 5 μm RTD oscillator with Gn = 150 mS, Rs = 0.6 Ω, Ls = 10 fH, L = 150 pH and b = 0.28.*

5.2.3 Oscillation and Cut-off Frequency

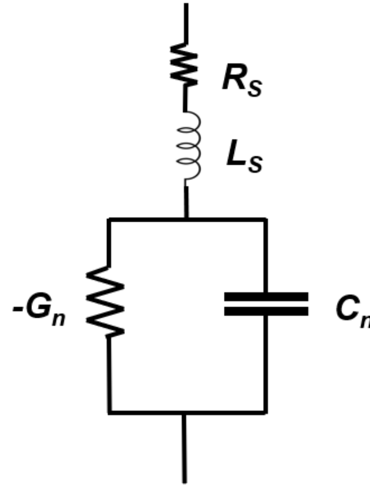

Figure 5.6: *RTD small-signal equivalent circuit with parasitic series resistance R_s and parasitic inductance L_s.*

The equivalent circuit model of an RTD including the parasitic series resistance R_s and inductance L_s is shown in Fig. 5.6, where the impedance of the system can be described by

$$Z = R_s + \frac{-G_n}{G_n^2 + \omega C_n^2} + j\omega\left(L_s - \frac{C_n}{G_n^2 + \omega C_n^2}\right) \tag{5.21}$$

At the angular frequency ω_r given by (5.22) the real part of the impedance becomes zero. This frequency corresponds to f_{max}, the cut-off frequency for the diode. When the frequency is larger than f_{max} the real part of Z becomes positive, and so the RTD will no longer functions as an active device.

$$\omega_r = \frac{G_n}{C_n}\sqrt{\frac{1}{G_n R_s} - 1} \tag{5.22}$$

For an RTD oscillator the oscillation frequency can be derived from the susceptance of the circuit. Fig. 5.7 shows the equivalent circuit model for an RTD oscillator including parasitic elements.

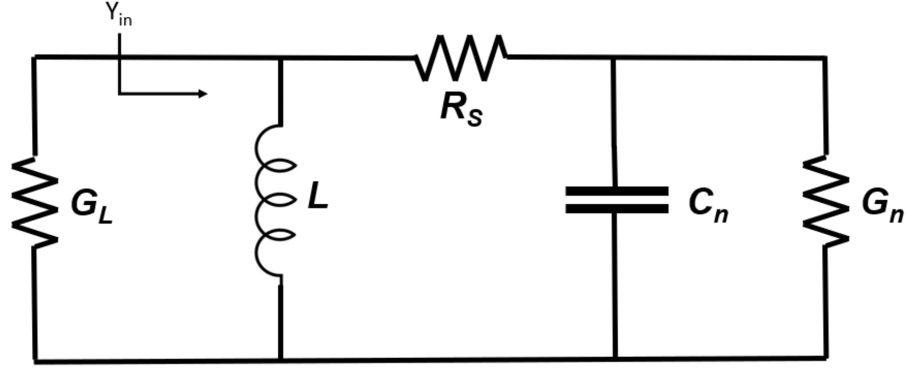

Figure 5.7: *RTD RF small-signal equivalent circuit with parasitic resistance R_s.*

The admittance looking into the RTD circuit is given by

$$Y_{in} = \frac{\omega^2 C_n^2 R_s + G_n^2 R_s + G_n}{G_n^2 R_s^2 + 2G_n R_s + \omega^2 C_n^2 R_s^2 + 1} +$$

$$+ j\left(\frac{\omega C_n}{G_n^2 R_s^2 + 2G_n R_s + \omega^2 C_n^2 R_s^2 + 1} - \frac{1}{\omega L}\right) \quad (5.23)$$

The susceptance B is given by

$$B = \frac{\omega C_n}{G_n^2 R_s^2 + 2G_n R_s + \omega^2 C_n^2 R_s^2 + 1} - \frac{1}{\omega L} \quad (5.24)$$

And by equating (5.24) to 0 the frequency of oscillation is given by

$$f_{osc} = \frac{G_n R_s + 1}{2\pi\sqrt{LC_n - C_n^2 R_s^2}} \quad (5.25)$$

Assuming that the parasitic series resistance is negligible, i.e. $R_s \approx 0$ the above equation can be simplified to

$$f_{osc} = \frac{1}{2\pi\sqrt{LC_n}} \quad (5.26)$$

5.2.4 Phase Noise

Phase noise (PN) is a key parameter for many oscillator applications and is a measure of the power spectral density of the phase angle. It is the result of short-term variations or fluctuations that occur in a signal due to time-domain instabilities. Phase noise in the frequency domain is equivalent to jitter in the time domain. An ideal oscillation can be expressed in the frequency domain as [7][8]

$$V(t) = A \sin(\omega t) \tag{5.27}$$

where A is the signal amplitude and ω represents the angular frequency given by $\omega=2\pi f$. However, circuit and device noise can alter both the phase and amplitude of the oscillator. The disturbance from an ideal oscillation can be expressed as

$$V(t) = [A + \varepsilon(t)] \sin(\omega t + \varphi(t)) \tag{5.28}$$

where $\varepsilon(t)$ represents fluctuations present in the amplitude of the signal and $\varphi(t)$ is the phase fluctuations. Inherently all practical oscillators have an amplitude-limiting mechanism, because the oscillations occur when the loop gain is unity. If the amplitude grows, gain compression caused by the non-linearity of the transfer function occurs and the oscillation amplitude dampens. Likewise, if the amplitude drops, the loop gain goes over unity and its restored due to expansive characteristics. As such the contribution of the amplitude variation on the signal is greatly attenuated and phase noise generally dominates [9].

The spectrum of a pure sinusoid such as the one described in (5.27) is a thin line and can be mathematically described as a Dirac delta function [10]. Noise present in the signal broadens the spectrum of the signal as shown in Fig. 5.8, where the noise spectrum of an RTD oscillator is shown spreading out on either side of the signal.

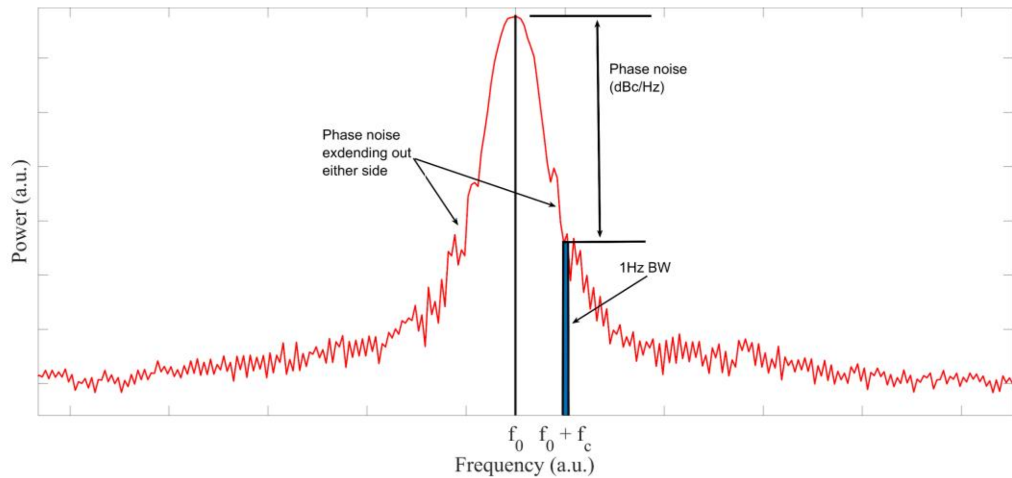

Figure 5.8: *Noise spectrum of an RTD oscillator. The ideal oscillator is represented by a Dirac delta function at f_0. The phase noise is measured as the ratio of offset frequency output power (highlighted in blue) relative to the carrier output power.*

The phase noise is characterized by the ratio of the noise power in 1 Hz bandwidth at a frequency offset (f_0 + fc) away from the carrier (f_0) to the carrier signal power (5.29) and it is measured in decibels relative to the carrier per Hertz of bandwidth, dBc/Hz.

$$L(f) = \frac{P_{offset/Hz}}{P_{carrier}} \tag{5.29}$$

where L(f) is the single sideband power referenced to the carrier, $P_{offset/Hz}$ is the power in a 1Hz bandwidth at a frequency away from the carrier and $P_{carrier}$ is the power of the carrier signal.

5.2.5 Figure of Merit for VCOs

Efficiency in an oscillator is defined as the ration between the useful power output (RF output power) divided by the total power dissipation in the system, i.e. (5.30) where P_{RF} is the power delivered to the RF load and P_{DC} is the dc power dissipated by the oscillator. The DC-to-RF conversion efficiency of conventional RTD oscillators is usually less than 1%, a problem caused mainly by the usually low value shunt resistor used for stabilisation (~ 10 Ω) in oscillator topologies. For a conventional RTD oscillator design (shown in Fig. 5.9) when the voltage bias V_{bias} = 1 V the power dissipated by a 10 Ω shunt resistance is 100mW, while the RTD device only consumes around 10 - 20 mW.

$$Efficiency = \frac{P_{RF}}{P_{DC}} * 100 \tag{5.30}$$

As the characteristics of voltage-controlled oscillators (VCO) include oscillation frequency, output power, efficiency and tuning range a widely adopted measure to identify the characteristics of the VCO is the figure-of-merit (FOM) [11].

$$FOM = L(\Delta f_{offset}) - 20\log\left(\frac{f_0}{\Delta f_{offset}}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \tag{5.31}$$

$$FOM_T = FOM - 20\log\left(\frac{TR}{10}\right) \tag{5.32}$$

$$FOM_{TP} = FOM_T - 10\log\left(\frac{P_{RF}}{1mW}\right) \tag{5.33}$$

where $L(\Delta f_{offset})$ represents the phase noise at the offset frequency, f_0 is the oscillation frequency, P_{DC} is the dc power dissipated by the oscillator, TR represents the tuning range (%) and P_{RF} is the measured output power of the oscillator. The performance of the VCO is regarded to be better with a higher absolute value of FOM.

5.3 RTD Oscillator Topologies

5.3.1 Single RTD Oscillators

The schematic circuit diagram of a single RTD oscillator is shown in Fig. 5.9. V_{bias} represents the bias voltage applied to the diode with R_S and L_S representing the parasitic resistance and inductance introduced by the biasing network. R_B is the stabilising resistor connected in parallel with the RTD in order to suppress the low frequency bias oscillations. The value for R_B is chosen as to satisfy Eq. 5.34.

$$R_B < \frac{1}{G_n} \tag{5.34}$$

The decoupling capacitor C_E is used to short-circuit the RF signal to ground in order to avoid RF power been dissipated across the stabilising resistor R_B [12]. The capacitor has a width and height of 100 μm and 350 μm respectively, the thickness of the Si_3N_4 dielectric is 75 nm ($\varepsilon_r = 6.8$) which corresponds to a capacitance value of $C_E = 30$pF. C_E will act as a short circuit at the desired oscillation frequency if

$$\frac{1}{2\pi f_0 C_E} < 0.1\ \Omega \tag{5.35}$$

The RTD is connected through a CPW line with length l_r to the decoupling capacitor C_E. Since the RF signal sees the decoupling capacitor as a short, the connection of l_r and C_E can be approximated by an inductor L for the RF signal and its inductance value is determined by l_r. The inductor L is designed to resonated with the RTD self-capacitance C_n to obtain the desired frequency of oscillation. The frequency of oscillation is given by (5.26).

An on-chip or external capacitor C_{block} is introduced in the circuit to prevent any DC from reaching the load resistance R_L and is chosen as to satisfy (5.35).

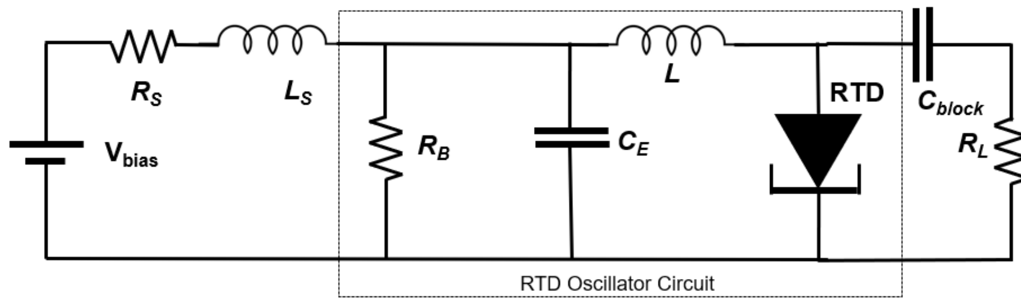

Figure 5.9: *Conventional single RTD device oscillator topology where V_{bias} is the biasing voltage, R_S and L_S represent the bias cable inductance and resistance, respectively. Shunt resistance R_B is used to suppress the low frequency bias oscillations. C_E is the decoupling capacitor and L the resonating inductor.*

Fig. 5.10 shows the small signal RF equivalent circuit of the single RTD device oscillator where the RTD is represented by its self-capacitance C_n and negative differential conductance -G_n. From the de-embedding procedure discussed previously in chapter 2 the RTD self-capacitance is in the 0.8 – 1.5 fF/µm^2 range. The 3D illustration of the design described in Fig. 5.9 is shown in Fig. 5.11.

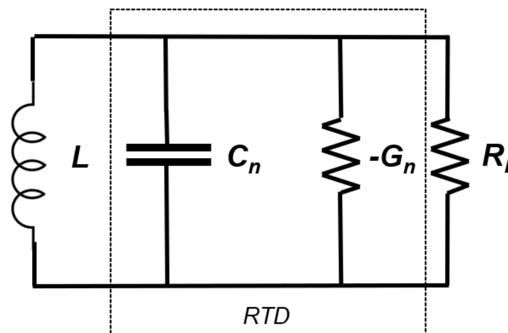

Figure 5.10: *Small-signal equivalent circuit where the RTD is represented by the self-capacitance C_n in parallel with the negative conductance -G_n.*

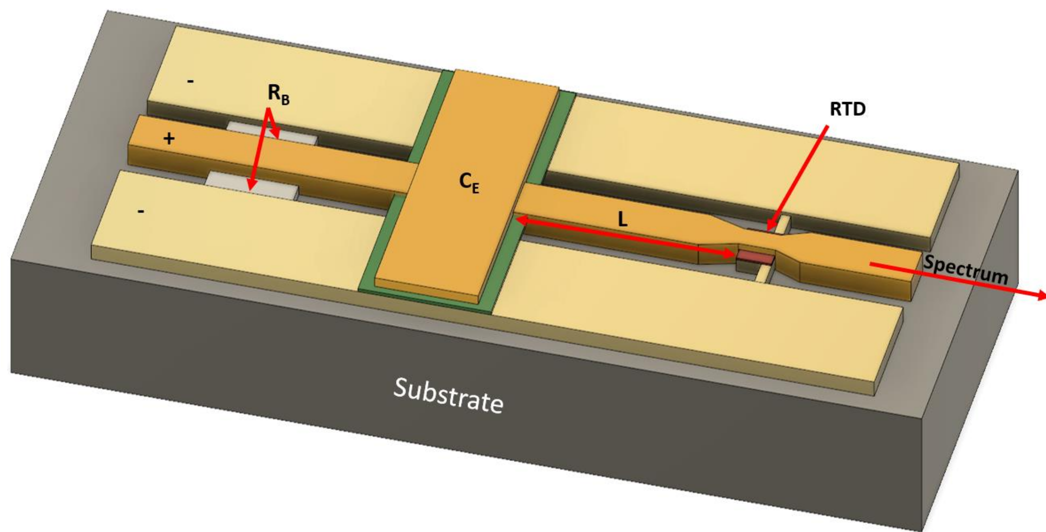

Figure 5.11: *3D illustration of a single RTD device oscillator. The shunt resistance R_B is fabricated from two parts placed on either side of the DC line.*

Single RTD oscillators with two different device sizes 4 µm × 4 µm, and 5 µm × µm were designed and fabricated using the single oscillator topology, but with different CPW lengths. The 50 Ω characteristic impedance CPW line structure consists of a 60 µm wide signal line and 40 µm gap to the ground planes. The device sizing has been done according to [6].

For a single 5 µm × 5 µm device with a CPW length of 80 µm, the measured oscillation frequency was 27.84 GHz with a measured oscillation power of -2.8 dBm (0.52 mW) when the bias voltage was V_{bias} = 0.84 V and I_{bias} = 129 mA. For this measurement setup, the insertion loss of the probe, cables and dc block were measured using a reference 30 GHz signal source with the output power set at 0 dBm. To measure the insertion loss, the signal from the reference source was first measured using the spectrum analyzer, then again through the biasing lines and probes placed on a 50 Ω characteristic impedance CPW line. The insertion loss at 30 GHz was measured to be 5.4 dB and the corrected result for the oscillator output power is 2.6 dBm (1.8 mW). The stabilising resistor R_B (R_B = 8Ω) has a total I_{Rb} = 105 mA current flowing across with 93 mW power dissipated. The current flowing through the diode was I_{bias} - I_{Rb} = 24 mA. The total DC power consumed by the oscillator is 108 mW, and the DC-to-RF conversion efficiency is 1.66 %.

The measured single side-band phase noise of a 30 GHz RTD oscillator from 100 kHz to 100 MHz offset frequency is shown in Fig. 5.12. The phase noise is -92 dBc/Hz at 100 kHz offset, -100 dBc/Hz at 1 MHz offset and -137 dBc/Hz at 10 MHz offset from the carrier. The calculated FOM of the fabricated oscillator is -168.7 dBc/Hz.

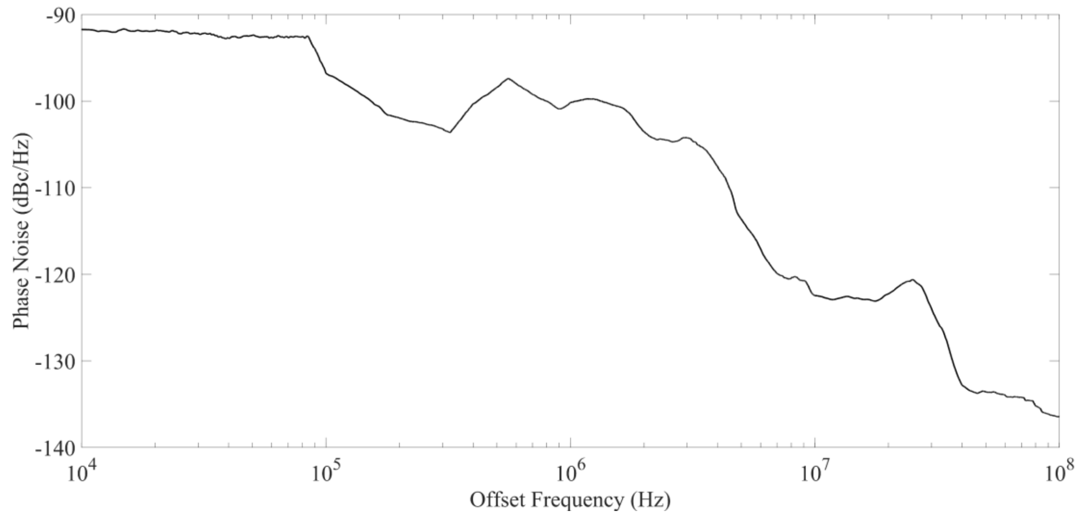

Figure 5.12: *Measured single side-band phase noise of 30 GHz single RTD oscillator at 10 kHz offset from carrier to 100 MHz offset from carrier.*

Using the parameters extracted for a 5 μm × 5 μm RTD device from layer structure #1 discussed previously in chapter 2, a model of the conventional RTD oscillator (Fig. 5.9) was simulated in MATLAB software. The measured and simulated spectrum of the RTD oscillator is presented in Fig. 5.13 at a bias level of 0.84 V.

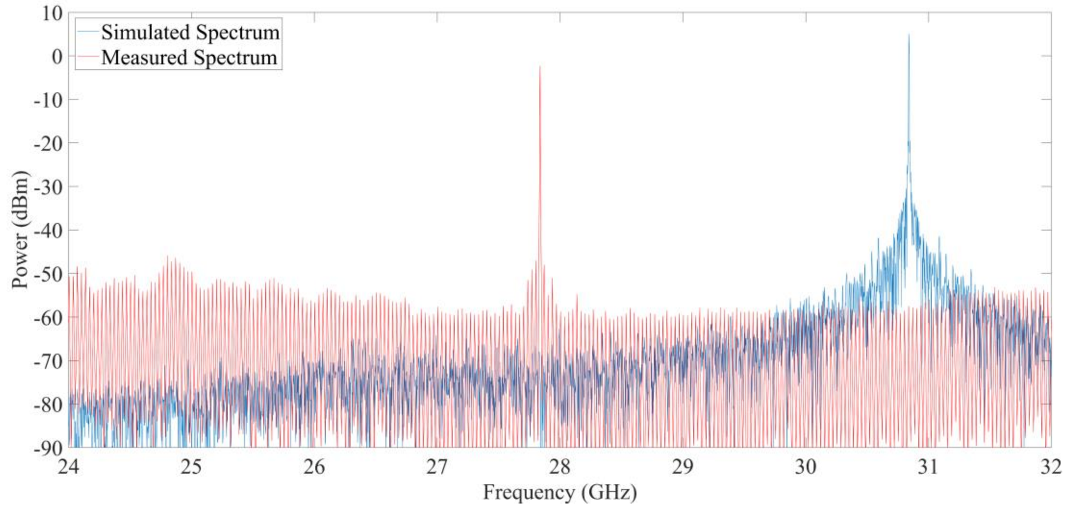

Figure 5.13: *Simulated and measured spectrum of RTD oscillator. The output power of the simulated RTD is about 3 mW with an oscillation frequency of 30.9 GHz.*

The calculated frequency of oscillation using (5.25) was 30.6 GHz, the simulated frequency is 30.9 GHz and the measured frequency 27.8 GHz. The output power of the simulated RTD oscillator (3 mW) is about half of to the theoretical maximum oscillation power (5.6 mW) given by (5.12). The model described in Chapter 4 is able to reproduce both the DC and RF characteristics of the fabricated devices.

The RF characteristics of the fabricated of the 4 µm × 4 µm and 5 µm × µm devices are summarized in Table 5.1. The average frequency tuning range (Δf) of the fabricated RTD oscillators is about 6 GHz, with tuning sensitivity $\Delta f / \Delta V_{bias}$ = 10 GHz / V. The output power fluctuates by about 5 dB to 7 dB over the tuning range.

Table 5.1: *Measurement results of the single RTD oscillators*

RTD size (μm)	Bias Voltage (V)	CPW length (μm)	Measured frequency (GHz)	Corrected output power (mW)	DC-to-RF efficiency (%)
4×4 μm²	*1.0*	*300*	*23.4*	*0.71*	*0.47*
	0.94	*180*	*25*	*0.74*	*0.55*
	0.8	*150*	*27.5*	*0.70*	*0.70*
	1.2	*90*	*34.16*	*1.3*	*0.62*
5×5 μm²	*0.90*	*240*	*17.4*	*1.54*	*1.25*
	1.05	*180*	*21.3*	*1.73*	*1.06*
	0.93	*120*	*24.0*	*2.34*	*1.79*
	0.84	*80*	*27.8*	*1.80*	*1.66*
Simulated	*0.84*	*N/A*	*30.9*	*3.0*	*2.7*

5.3.2 High-Efficiency RTD Oscillators

As the efficiency of the standard single RTD oscillator topology described in the previous section is limited, mostly by the high power dissipated by the shunt resistance R_B, the oscillator circuit topology utilizing the RC stabilisation network was proposed as shown in Fig. 5.14 [13]. The value of the stabilising resistance R_B is calculated the same as in the previous section using (5.32). The value of capacitor C_B = 144 pH is calculated using Eq. 5.36, where the parasitic inductance L_S = 0.9 nH and parasitic resistance R_S = 2 Ω where assumed to be dominated by the bias-tee connector. For a 4 μm × 4 μm RTD the maximum negative differential conductance was measured at G_n = -70 mS.

$$C_B > \frac{L_S G_n}{R_S} \tag{5.36}$$

At low parasitic oscillation frequencies (low MHz range) the resistor R_B can be ignored, and the capacitance C_E adds to the capacitance C_B. At higher parasitic oscillation frequencies C_B will appear as a short for the parasitic oscillations and R_B is used to stabilise the device. No RF power generated by the RTD is dissipated across the stabilising network as the capacitance C_E is designed to be a short at the designed oscillation frequency.

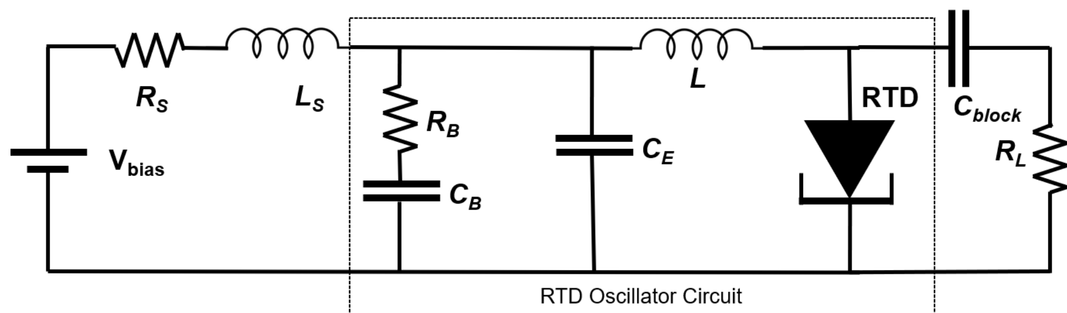

Figure 5.14: *Proposed RTD device oscillator topology with RC stabilisation network.*

Oscillators with the RC stabilisation network topology where fabricated with a device size of 4 µm × 4 µm. The value for the inductance L was 140 pH for ~30 GHz oscillators. The choice of the oscillation frequency and device size was to facilitate easier circuit realisation and device characterisation. A micrograph of the fabricated oscillator circuit is shown in Fig. 5.15. The overall size of the oscillator circuit was around 1000×700 µm^2.

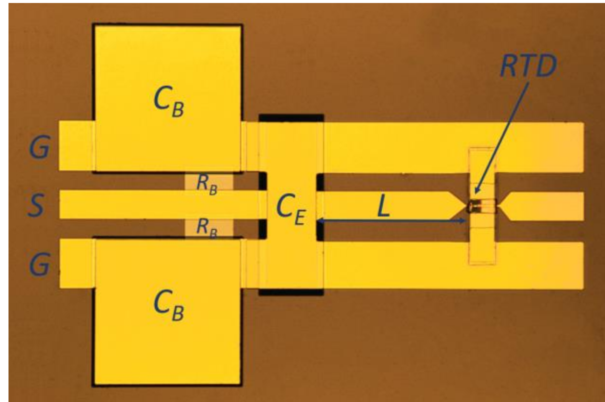

Figure 5.15: *Micrograph of the fabricated RTD oscillator with an integrated stabilising network. For measurement, a GSG probe is used. The capacitor C_B and resistance R_B are split in two and placed in parallel with the RTD. The capacitor C_E acts as a short to ground for the RF signal.*

For the high efficiency RTD oscillator the measured frequency of oscillation was 34.1 GHz at V_{bias} = 0.94 V and I_{bias} = 18 mA. The corrected output power was 3.95 dBm (2.48 mW), which compares well with the theoretical 5.18 dBm (3.3 mW) estimated from the 4 μm × 4 μm dc characteristics of the device. The measured oscillator spectrum is shown in Fig. 5.16 and Fig. 5.17 shows the measured oscillator output power and frequency as a function of bias voltage.

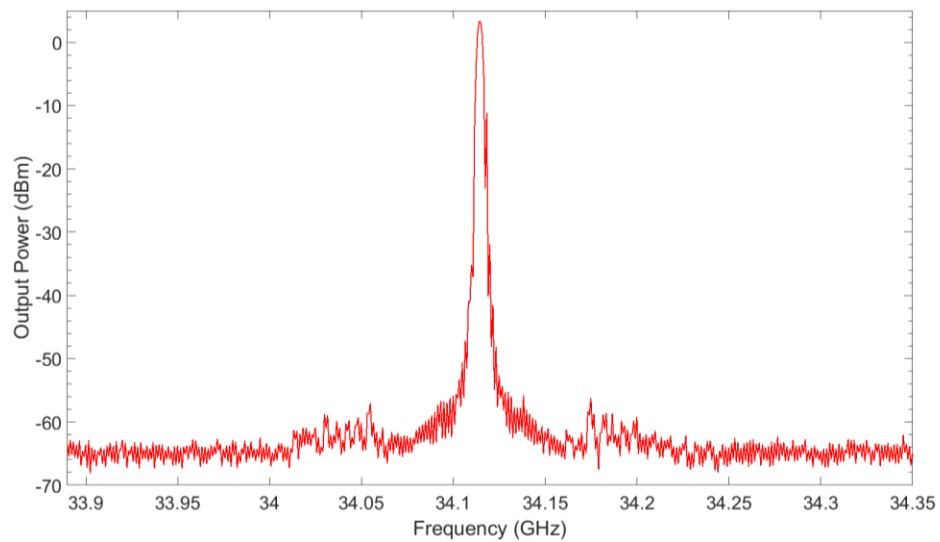

Figure 5.16: *Measured high efficiency RTD spectrum at V_{bias} = 0.94 V and I_{bias} = 18 mA. The frequency of oscillation is 34.1GHz with an output power of 3.95 dBm.*

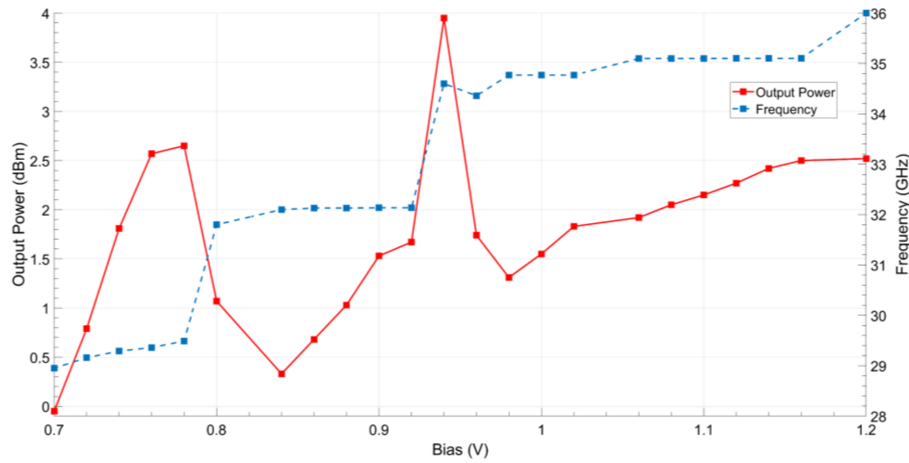

Figure 5.17: *Measured oscillator output power and frequency as a function of* V_{bias}.

The RTD oscillator has a tuning range of about 7 GHz, with a tuning sensitivity of Δf / ΔV_{bias} = 11.7 GHz / V and high output power (1 to 2 dBm) across most of the operating voltage range. The calculated DC-to-RF conversion efficiency at $V_{bias} = 0.94$ V is 14.7%, over a 10-fold improvement when compared to the conventional design and close to the theoretical 19.5% maximum efficiency for this epi-layer structure design and size. The measured phase noise of the high efficiency RTD oscillator is shown in Fig. 5.18. The phase noise is -89 dBc/Hz at 100 kHz offset, -137 dBc/Hz at 1 MHz offset and -133 dBc/Hz at 10 MHz offset from the carrier. The calculated FOM for the high efficiency RTD oscillator is -215 dBc/Hz.

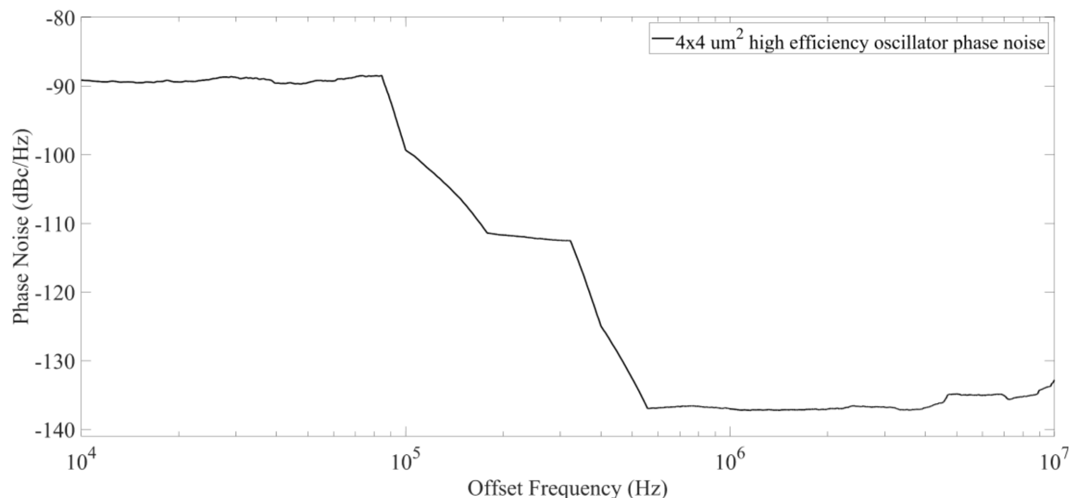

Figure 5.18: *Measured phase noise for the high efficiency RTD oscillator. The phase noise is -89 dBc/Hz at 100 kHz offset, -137 dBc/Hz at 1 MHz offset and -133 dBc/Hz at 10 MHz offset from the carrier.*

5.3.3 Discussion

RTD oscillators with two different circuit topologies that produce a high oscillation power in the Ka-band (26.5 GHz – 40 GHz) have been described in this chapter. The oscillators were fabricated using photolithography process and employed different CPW structures in order to realize the MIM capacitors and inductance values.

Conventional RTD oscillators use the shunt-resistor method for bias oscillation suppression and, as a result, the efficiency of such oscillators is severely degraded. The proposed method does not hinder the oscillator performance and can be adapted to higher PVCR (peak-to-valley current ratio) epitaxial structures, thereby increasing the oscillator output power and conversion efficiency. A comparison between the fabricated oscillators and other published work is summarized in Table 5.2. To the best of author’s knowledge, the fabricated high efficiency RTDs have the highest FOM between the different fabrication technologies.

Table 5.2: *Comparison between different VCOs in the Ka-band*

Reference	**[16]**	**[15]**	**[18]**	**[14]**	**[17]**	**This work**	**This work**
TECH.	0.15 um pHEMT	130 nm SiGe BiCMOS	65-nm CMOS	65-nm CMOS	InGaAs /AlAs RTD	InGaAs /AlAs RTD	InGaAs /AlAs **RTD**
F_{OSC} (GHz)	28.3	30.9	35.1	28.3	28.7	27.8	**34.1**
TR (%)	13.4	16.8	24.4	17.8	3.48	10.9	**10.7**
P_{DC} (mW)	80	40.2	4.8	4.1	289.1	108	**16.92**
P_{RF} (mW)	15	2.5	0.06	0.15	0.26	1.8	**2.48**
DC-to-RF Efficiency (%)	18.7	6.21	1.25	3.65	0.08	1.6	**14.6**
PN (dBc/Hz) @ 1MHz	-102	-101.4	-106.6	-102.8	-114	-100	**-137**
FOM (dBc/Hz)	-172.0	-175.1	-187.2	-185.7	-178.3	-168.7	**-215**
FOM_T (dBc/Hz)	-174.5	-179.6	-194.9	-190.7	-168.9	-169.4	**-215.5**
FOM_{TP} (dBc/Hz)	-186.3	-183.6	-207.1	-198.9	-163.0	-171.9	**-219.4**

5.4 Summary

In this chapter, a new biasing network for RTD oscillators for high DC-to-RF conversion efficiency was presented. Highly efficient mm-wave RTD oscillators with tunable frequency between 29 and 36 GHz were fabricated and measured. The employed bias stabilisation network does not consume dc power resulting in over a 10-fold improvement in the DC-to-RF conversion efficiency when compared with the standard shunt resistance method. Combined with the low phase noise of the oscillator, RTDs provide a simple, low cost solution for high-capacity wireless communication systems and other applications. Higher efficiencies are expected by a reduction in the peak voltage and of the valley current. The design can be scaled for other epitaxial layer structures with higher PVCR, thereby further increasing the output power and the conversion efficiency.

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Chapter 6. Wireless Data Transmission Link

6.1 Introduction

Chip-sized and room-temperature devices that can both emit and detect millimeter/submillimeter wave radiation are key components for future mobile communication applications [1]-[4]. Recently, high power RTD transmitters have been reported operating in the J-band (220 GHz – 325 GHz) frequency range and with approximately 1 mW output power [5][6]. As data transmitters RTDs are easily modulated by a signal superimposed on the bias lines, and also possess a wide modulation bandwidth [6][7]. On the detector side, most commonly used are Schottky-barrier diodes (SBDs), due to their small-form factor and high-speed response at room temperature [8]-[10], however SBDs are strongly temperature dependent due to thermionic emission of charge carriers over the potential barrier [11][12]. RTD based detectors have recently gained research momentum [1][13]-[15] due to their strong non-linear *I*-*V* characteristics and the possibility of integrating the transmitter and receiver on the same circuit, thereby lowering the implementation cost and accelerating adoption into the market. When compared to SBDs, the RTD detectors were able to match and/or surpass the performance of their commercially available counterparts [13][16].

In this chapter, wireless links experiments were done jointly with another PhD student (Razvan Morariu) to assess the feasibility of future RTD transceiver designs. The RTD detectors where designed and developed as part of Razvan Morariu's PhD research project, while the RTD transmitters were designed and developed as part of this project. The full characteristics of the RTD detector design will be covered in his thesis, which will be published in the future. The (joint) result of the wireless transmission experiments is reported here as a joint result with the consent of Razvan Morariu.

6.2 Experimental Setup

The experimental setup for wireless data transmission using two RTDs, one operating as a transmitter (Tx) and one as a receiver (Rx), is shown in Fig. 6.1. A pseudo-random binary sequence (PRBS) generator was connected through a bias-T to the Tx. The RTD was biased in the PDR region, close to the peak voltage, and the signal from the PRBRS was used to modulate the carrier using OOK (on-off keying). The signal was radiated into free space through a 26 GHz to 40 GHz horn antenna (15 dBi gain) connected to the RTD through a CPW-to-waveguide transition. An identical antenna fitted with a waveguide-to-CPW transition is used at the receiver side. The Tx and Rx RTD were separated by a distance of 15 cm for data communications (constrained by the limited space available in the measurement setup). The RTD receiver is biased from a second power supply through a bias-T. The demodulated RF signal is obtained from the DC side of the RTD Rx and is passed through a low noise amplifier (LNA) and into an oscilloscope/spectrum analyzer for measurements.

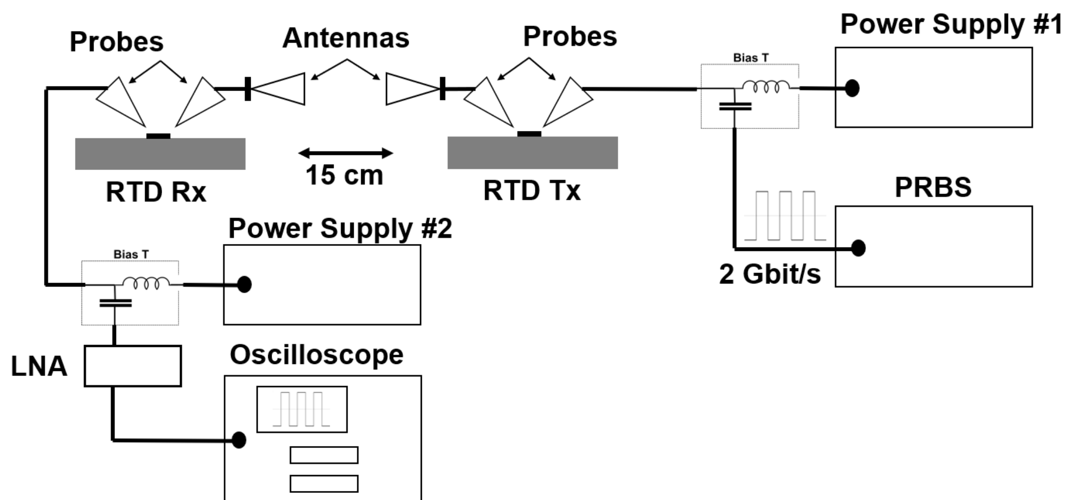

Figure 6.1: *Schematic block diagram of wireless data transmission setup using RTDs as transmitters and receivers.*

6.2.1 RTD Transmitter

Fig. 6.2 shows how the RTD transmitter is modulated. The RTD Tx is biased within the PDR at V_{off}, and the baseband (BB) signal is used to shift the operating bias point at V_{on}. The modulated signal is created by the on-off keying of the BB signal, in which a logic-one biases the RTD in the NDR to create oscillations and a logic-zero returns the RTD at the V_{off} position and the oscillations stop. The BB signal level has been chosen to move the RTD biasing point to where the power of the oscillator is at its highest. A similar modulation scheme has been tested where the RTD is biased within the NDR region and the BB signal is used to turn off the oscillations by moving the bias in the second positive differential region.

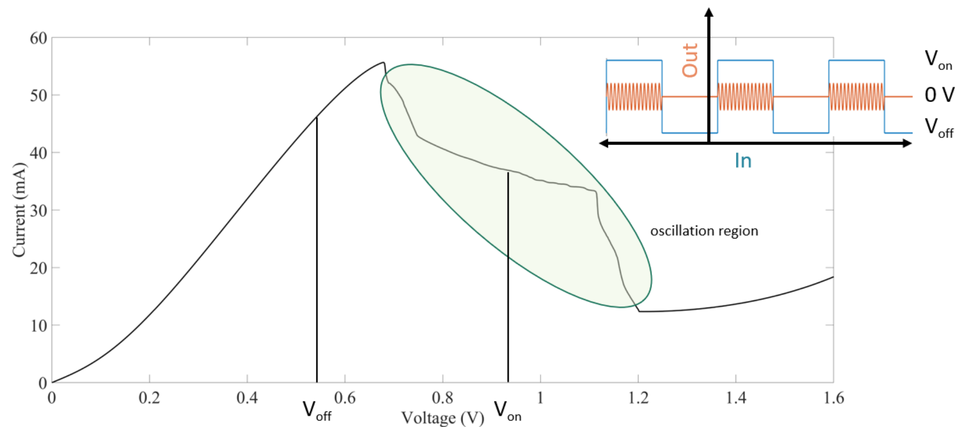

Figure 6.2: *Operation of the RTD as a transmitter using OOK modulation scheme. The BB signal is used to move the operating point of the RTD (on/off).*

The resulting signal changes with respect to the baseband modulating signal, where the amplitude of the high frequency carrier takes on the shape of the lower frequency modulating signal. An ideal carrier and baseband signal can be expressed mathematically as:

$$e_c = E_c \sin(\omega_c t) \tag{6.1}$$

$$e_m = E_m \sin(\omega_m t) \tag{6.2}$$

where E_c and E_m represent the amplitude of the carrier and baseband signal and ω_c and ω_m the angular frequency of the carrier and baseband signal, respectively. For the analysis, the BB signal was treated as a single sine wave, however the actual BB signal has a square-wave form which can be regarded as a sum of sine waves. The resulting signal can be written in the form:

$$e_{am} = (E_c + E_m \sin(\omega_m t))\sin(\omega_c t) \tag{6.3}$$

by normalizing the carrier amplitude to one the equation can be re-written as:

$$e_{am} = (1 + m \sin(\omega_m t))\sin(\omega_c t) \tag{6.4}$$

where m represents the modulation index and is defined as the ratio of the modulation signal amplitude to the carrier amplitude i.e.

$$m = \frac{E_m}{E_c} \; ; 0 \leq m \leq 1 \tag{6.5}$$

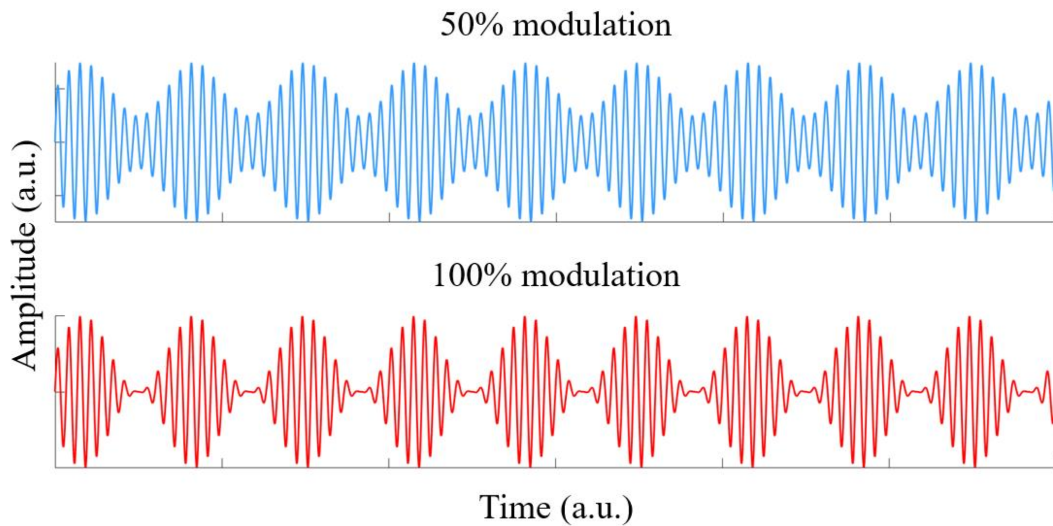

Figure 6.3: *Amplitude modulation of a carrier signal by a much lower frequency modulating signal at 0.5 and 1 modulation index value. For OOK modulation the modulation index is 1 (100 %).*

by expanding Eq. 6.4 we obtain:

$$e_{am} = \sin \omega_c t + \frac{m}{2}\cos(\omega_c - \omega_m)\, t - \frac{m}{2}\cos(\omega_c + \omega_m)\, t \quad (6.6)$$

where $\sin \omega_c t$ represents the carrier frequency, $\frac{m}{2}\cos(\omega_c - \omega_m)\, t$ represents the lower sideband and $\frac{m}{2}\cos(\omega_c + \omega_m)\, t$ is the upper sideband. For an OOK modulation scheme the modulation index *m* is 1, as such the sideband amplitudes is half of the carrier amplitude, i.e. a quarter of the power.

The RF spectrum of an RTD oscillator modulated with a 1-0-1-0 pattern at 2 GHz clock frequency is shown in Fig. 6.4. The RTD transmitter has an oscillation frequency of approximately 30 GHz with -1.6 dBm (0.7 mW) corrected output power. The output of the RTD transmitter was fed to a CPW-to-waveguide transition and into the antenna.

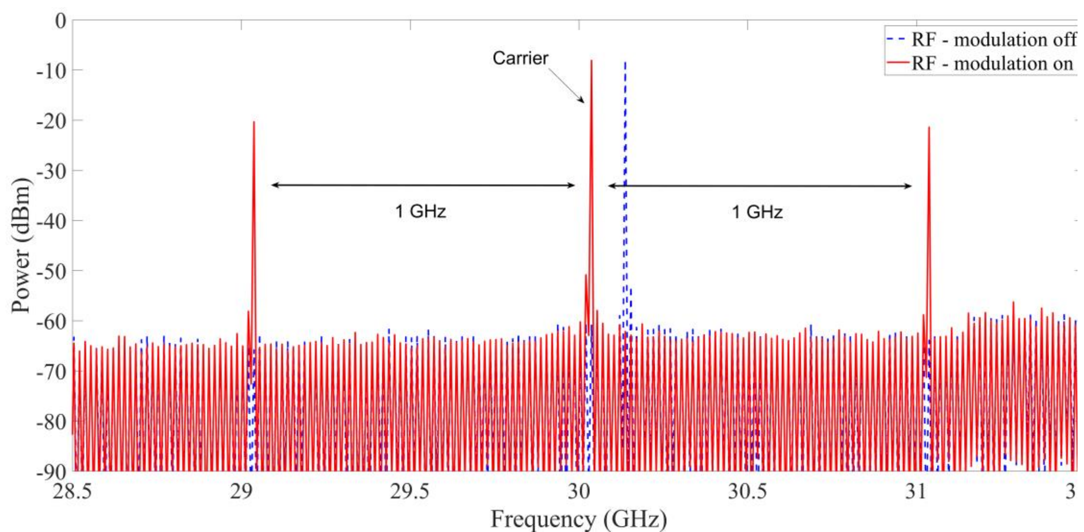

Figure 6.4: *RF spectrum of transmitter RTD when biased in the NDR and the BB signal was used to move the biasing point in the second PDR region. The modulating sidebands can be seen at a 1 GHz distance from the carrier (1-0-1-0 pattern @ 2 GHz clock frequency)*

6.2.2 RTD Receiver

The measured RF power at the receiver antenna with a distance between the antennas set to 15 cm was approximately -30 dBm (1 μW). The modulated signal was then fed through a waveguide-to-CPW transition to the RTD receiver, which operated in the square-law region as shown in Fig. 6.5.

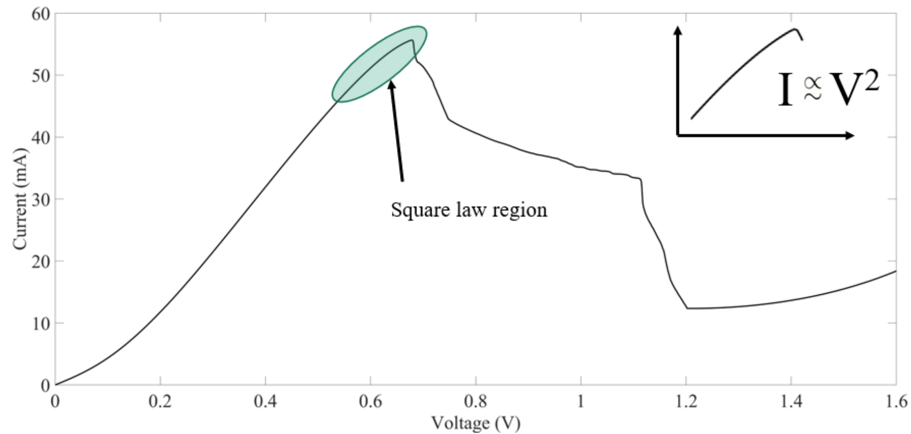

Figure 6.5: *Operating point of an RTD receiver. The non-linear characteristics of the IV are shown in the inset.*

The current-voltage relationship of the diode detector when biased in the non-linear region is of the form:

$$i(t) = av^2(t) + bv(t) \tag{6.7}$$

where the coefficients *a* and *b* are constants associated with the detector. The output of the system varies with respect to the squared input voltage. By applying the modulated signal to the squaring device, we get:

$$i(t) = ae_{am}(t)^2 + be_{am}(t) \tag{6.8}$$

For the analysis the second term of Eq. 6.8 can be ignored, and by expanding the input signal the resulting equation is shown in (6.9)

$$i(t) = a\left(\sin\omega_c t + \frac{m}{2}\cos(\omega_c - \omega_m)\,t - \frac{m}{2}\cos(\omega_c + \omega_m)\,t\right)^2 \quad (6.9)$$

The output of the detector is the square of the amplitude modulated signal and since the input is being multiplied by the sin $\omega_c t$ term, two of the resulting terms will be the original modulation signal i.e.

$$e_{am} \times sin\omega_C t = \underbrace{\frac{m}{2}\sin\omega_m t}_{\text{original BB signal}} \underbrace{- \frac{1}{2}cos2\omega_c t + \frac{m}{4}[\sin(2\omega_c - \omega_m)t - \sin(2\omega_c + \omega_m)t]}_{\text{AM signal centred at } 2\omega_c} \quad (6.10)$$

6.3 Measurement Results

The output of the RTD receiver was connected two a 20-dB gain (0 – 3 GHz) LNA in order to enhance the demodulated signal before connecting it to the oscilloscope. The measured eye diagrams for a 1 Gb/s and a 2 Gb/s data transfer speed is shown in Fig. 6.6. The complete measurement setup is shown in Fig. 6.7. For a 1 Gb/s data transfer the measured signal was 7.2 mV V_{pp} with a signal to noise ratio of approximately 15. For the 2 Gb/s data transfer the signal measured 2.2 mV V_{pp} and a signal to noise ratio of 5. Error-free transmission measured with a bit error rate tester (BERT) was achieved from 1 Gb/s to 2.4 Gb/s.

Beyond 2.4 Gb/s the BER increased (5.8×10^{-6} at 2.6 Gb/s), largely due to the 3-dB bandwidth of the RTD baseband circuit. For higher data rates the RC time constant at the input of the RTD transmitter must be taken into consideration [15][17]. The time constant τ is the product of the circuit resistance and the circuit capacitance, i.e. $\tau = RC$. In the RTD oscillator design, a shunt capacitor (60 pF) is used to create the shorted-CPW inductance. The RC delay time associated with this system is 60 picoseconds (C_E = 60 pF, R_S = 1 Ω approximated), thus the data rate limited by this constraint is 2.6 Gb/s.

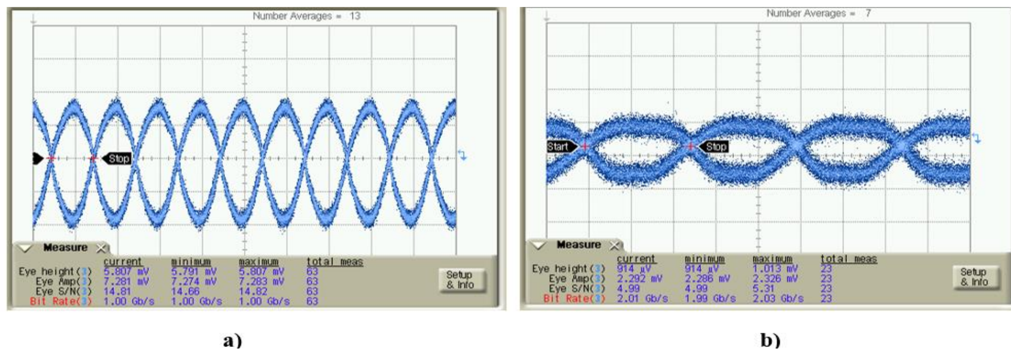

Figure 6.6: *Eye diagrams of RTD wireless link (a) 1 Gbit/s data rate , 7.2mV V_{pp}, S/N = 15 (b) 2 Gbit/s data rate, 2.2 mV V_{pp}, S/N = 5.*

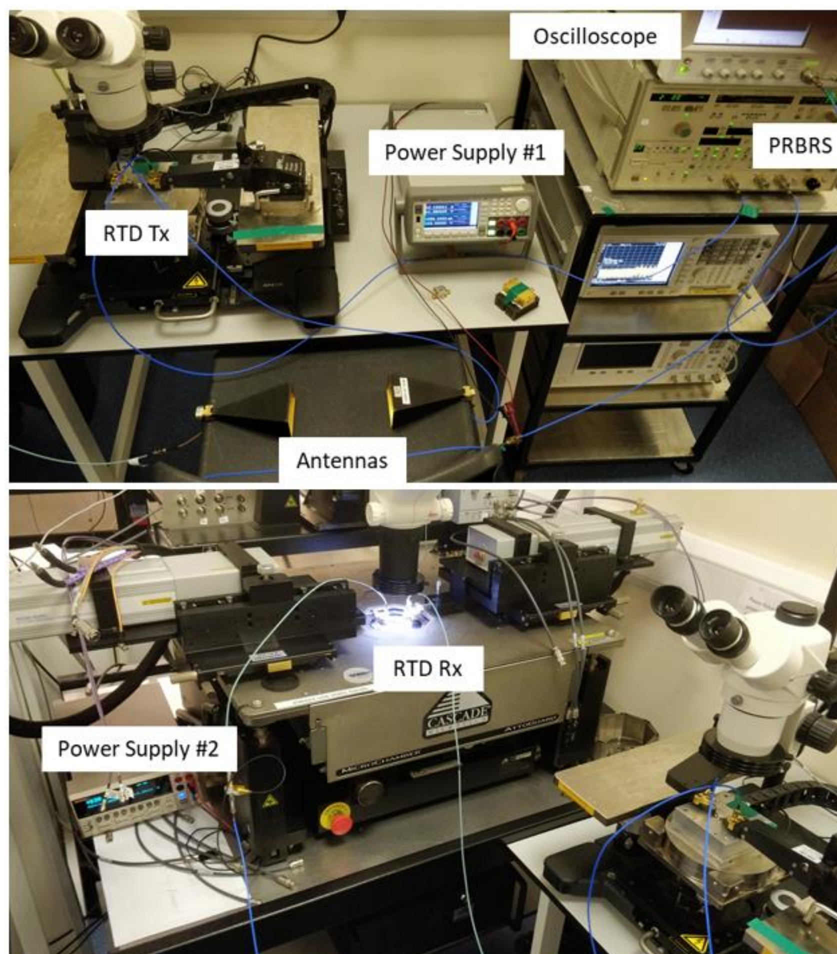

Figure 6.7: *Picture of the measurement setup used in the wireless data transmission link.*

6.4 Summary

In this chapter a joint experiment of an RTD transmitter and an RTD receiver has been presented including an explanation of the operating principle of the modulation / demodulation process. Wireless, error-free data transmission has been achieved at a distance of 15 cm and 2 Gb/s data transfer rate with a respectable signal-to-noise ration. Further improvements can be made in both transmitter and receiver by increasing the 3dB-bandwith point of the RTD transmitter and by selecting an appropriate RTD which has a higher curvature component $(\frac{d^2I}{dV^2} / \frac{dI}{dV})$ in the dc characteristics [18]. This experiment has shown that RTD transceivers are feasible for next generation low-cost wireless transmission.

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Chapter 7. Conclusions and Future Work

7.1 Conclusions

Devices that exhibit negative differential resistance (NDR) such as tunnel diodes, IMPATT diodes, Gunn diodes and resonant tunneling diodes can be used as electronic sources for high frequency signals. Among them, the RTD is the fastest operating solid-state electronic device with a reported frequency of oscillation up till now of 1.98 THz [1], and with a theoretical bandwidth of 2.5 THz [2]. However, the biggest limitations of an RTD oscillator are its low output power and low DC-to-RF conversion efficiency, due to the presence of parasitic oscillations when biased in the NDR. The bias oscillations associated with the device makes it difficult to accurately determine the DC characteristics of the device and therefore, results in a lack of accurate models which could help in the optimization process of various applications. The purpose of this PhD project was to address these limitations and focused on the stability criteria of RTDs and their application in high frequency oscillator circuits.

The results achieved in this project are as follows:

i. Design equations for realizing a stable RTD biasing network were derived. The method enables direct measurement of the RTD's *I-V* characteristics, in contrast with the conventional shunt resistor stabilisation method which the *I-V* characteristics had to be de-embedded after the measurement. The proposed method eliminates both low frequency bias oscillations as well as high frequency oscillations which would otherwise distort the measured characteristics. Furthermore, the method described can be adapted for oscillator designs, thereby improving the DC-to-RF conversion efficiency by reducing the DC current consumption.
ii. Radio frequency (RF) characterization of an RTD device and DC characterization were used in the realization on an accurate large-signal model of the RTD. The S-parameter measurements were used to determine an

accurate small-signal model of the device, which when combined with the large-signal *I-V* characteristics was able to reproduce the DC measurement results in a non-stable RTD device (plateau region) and the RF characteristics when used in an oscillator circuit. The model is expected to serve in the optimization process of RTD devices for millimeter and submillimeter wave applications.

iii. MMIC RTD oscillators using the proposed stabilisation method were designed and fabricated. Highly efficient millimeter wave RTD oscillators with over 7 GHz tuning frequency and over a milliwatt output power were presented. The employed bias stabilisation network did not consume any DC power, resulting in over a 10-fold improvement in DC-to-RF conversion efficiency when compared to the conventional designs and close to the theoretical maximum of the employed epi-layer structure. The presented approach could have a major impact with regards to the adoption of RTD technology for portable devices where battery capacity is at a premium.

iv. A wireless data transmission link using two RTDs operating as transmitter and receiver was demonstrated, proving the feasibility of future RTD transceiver designs, where the same RTD chip can be used in a half-duplex system to both transmit and receive, thereby lowering the implementation cost and accelerating the adoption of this technology into the market.

7.2 Future Work

7.2.1 RTD Modulation Bandwidth

In this thesis a millimeter-wave communication system using two RTDs has been demonstrated and has the potential to play a major role in the next generation of communication devices. However, the RTD oscillators in this thesis were not optimized for high data transfer rates, as such the bandwidth was limited to approximately 2.6 Gb/s. A large decoupling capacitor in the bias network results in a slow response as the capacitor charges/discharges when a data signal is applied to it. The modulation bandwidth is therefore limited by the biasing network and decoupling capacitor $C_{E,}$ which form a low pass filter. An alternative method would be to modulate the signal on the RF side of the oscillator, where a balun / lange coupler paired with

PIN diodes can be used to perform binary phase shift keying modulation (BPSK) [3][4], therefore removing the constraint imposed on the biasing network. A layout design of a CPW balun is shown in Fig. 7.1 and a schematic diagram of a BPSK modulator is shown in Fig. 7.2.

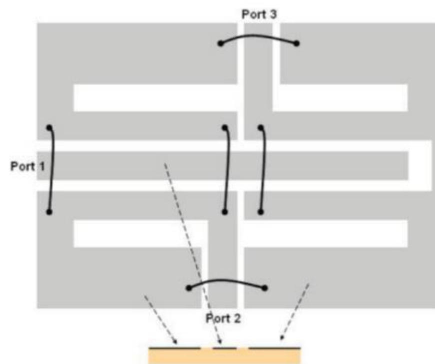

Figure 7.1: *Layout of CPW balun, the phase difference between the output at port 2 and 3 is 180°. Adapted from [3].*

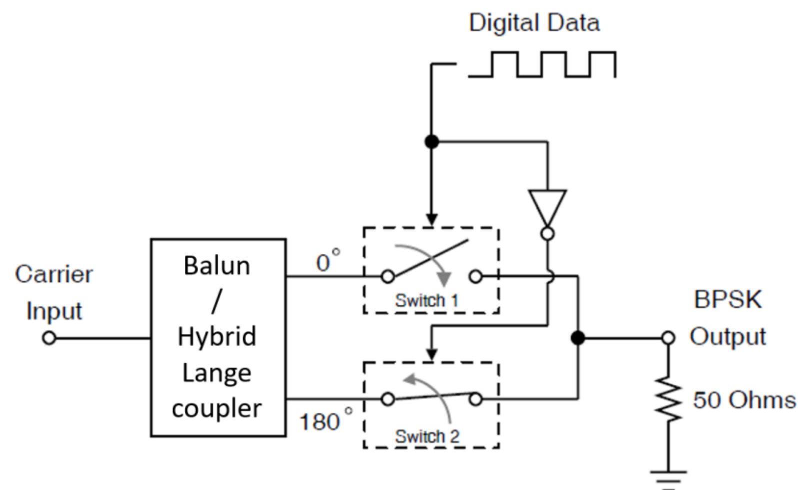

Figure 7.2: *Schematic block diagram of a BPSK modulator. The switches represent the PIN diodes, which are used to turn on/off the carrier input. Adapted from [4].*

In summary, high performance and highly efficient RTD oscillators were demonstrated in this thesis. The oscillators could form compact, room temperature operating building blocks for THz system in different mobile short-range communication and imaging systems.

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Appendix A. Fabrication Process

Sample cleaning

1. Ultrasonic bath in acetone for 3 minutes
2. Ultrasonic bath in methanol for 3 minutes
3. Ultrasonic bath in IPA for 3 minutes
4. Rinse with de-ionized water (RO-water)

Collector contact metal

1. Spin S1805 at 4000 RPM for 30 s
2. Bake sample on hotplate at 115° C for 60 s
3. Submerge in chlorobenzene for 5 minutes
4. Expose using MA6 for 2.4 s / hard contact / 40 µm separation
5. Develop sample in solution 1:1 Microposit developer concentrate (MDC): H_2O for 50 s
6. Rinse in RO-water for 60 s
7. Blow dry with N_2
8. Plasma ash the sample at 120 W RF power for 2 minutes
9. Submerge sample in solution 1:10 ammonium hydroxide (NH_4OH): H_2O for 20 s
10. Rinse in RO-water for 60s
11. Blow dry with N_2
12. Argon gun for 30 s (in Plassys 4)
13. Deposit Ohmic contact Ti/Pd/Au 20/30/150 nm
14. Lift-off after submerging in acetone/1165 resist remover at 50° C for 60 minutes
15. Rinse in Ro-water for 60 s
16. Blow dry with N_2

Etch to the bottom InGaAs contact layer

1. Spin S1805 at 4000 RPM for 30 s
2. Bake sample on hotplate at 115° C for 60 s
3. Expose using MA6 for 2.4 s / hard contact / 40 µm separation
4. Develop sample in solution 1:1 MDC: H2O for 50 s
5. Rinse in RO-water for 60 s
6. Blow dry with N_2
7. Plasma ash the sample at 120 W RF power for 2 minutes
8. Etch using solution orthophosphoric acid (H_3PO_4): hydrogen peroxide (H_2O_2): H_2O 1:1:38, etch rate 100 nm / min
9. Rinse in RO-water for 60 s
10. Measure etch depth
11. Submerge in acetone/1165 resist remover at 50° C for 30 minutes

Emitter contact metal

1. Same as collector contact metal

Etch to InP substrate

1. Spin S1805 at 4000 RPM for 30 s
2. Bake sample on hotplate at 115° C for 60 s
3. Expose using MA6 for 2.4 s / hard contact / 40 µm separation
4. Develop sample in solution 1:1 MDC: H_2O for 50 s
5. Rinse in RO-water for 60 s
6. Blow dry with N_2
7. Plasma ash the sample at 120 W RF power for 2 minutes
8. Etch using solution H_3PO_4: H_2O_2: H_2O 1:1:38, etch rate 100 nm / min
9. Etch into InP substrate using solution hydrochloric acid (HCl): H_3PO_4 1:4 for 30 s
10. Rinse in RO-water for 60 s
11. Measure etch depth
12. Submerge in acetone/1165 resist remover at 50° C for 30 minutes

Passivation and VIA opening

1. Spin polyimide PI-2545 at 8000 RPM for 30 s
2. Bake sample on hotplate at 115° C for 2 minutes
3. Bake sample in oven at 180° C for a minimum of 6 hours
4. Spin S1805 at 1500 RPM for 30 s
5. Bake sample on hotplate at 115° C for 2 minutes
6. Expose using MA6 for 2.8 s / hard contact / 40 μm separation
7. Develop sample in solution 1:1 MDC: H_2O for 50 s
8. Bake sample on hotplate at 115° C for 10 minutes
9. Dry etch using tetrafluoromethane (CF_4): O_2 5: 20 sccm, 200 W RF power until interferometer shows straight line (approximately ~ 6 minutes)
10. Submerge in acetone/1165 resist remover at 50° C for 30 minutes

Thin-film resistor

1. Spin S1805 at 4000 RPM for 30 s
2. Bake sample on hotplate at 115° C for 60 s
3. Submerge in chlorobenzene for 5 minutes
4. Expose using MA6 for 2.4 s / hard contact / 40 μm separation
5. Develop sample in solution 1:1 Microposit developer concentrate (MDC): H_2O for 50 s
6. Rinse in RO-water for 60 s
7. Blow dry with N_2
8. Plasma ash the sample at 120 W RF power for 2 minutes
9. Etch into InP substrate using solution HCl: H_3PO_4 1:4 for 30 s
10. Bake sample on hotplate at 115° C for 60 s
11. Deposit resistor NiCr 33 nm thickness
12. Submerge in acetone/1165 resist remover at 50° C for 30 minutes

1st Bond pad

1. Spin LOR 10A at 6000 RPM for 30 s
2. Bake sample on hotplate at 150° C for 3 minutes
3. Spin S1805 at 4000 RPM for 30 s
4. Bake sample on hotplate at 115° C for 2 minutes
5. Expose using MA6 for 2.4 s / hard contact / 40 µm separation
6. Develop sample in MF319 for 75 s
7. Plasma ash the sample at 120 W RF power for 2 minutes
8. Deposit bond pad Ti/Au 20/380 nm
9. Submerge in acetone/1165 resist remover at 50° C for 60 minutes

Metal-insulator-metal capacitor

1. Spin LOR 3A at 3000 RPM for 30 s
2. Bake sample on hotplate at 150° C for 3 minutes
3. Spin S1805 at 4000 RPM for 30 s
4. Bake sample on hotplate at 115° C for 2 minutes
5. Expose using MA6 for 2.4 s / hard contact / 40 µm separation
6. Develop sample in MF319 for 75 s
7. Plasma ash the sample at 120 W RF power for 2 minutes
8. Deposit silicon nitride (Si_3N_4) dielectric by ICP-CVD 75 nm
9. Submerge in acetone/1165 resist remover at 50° C for 60 minutes

2nd Bond pad

1. Same as 1st bond pad

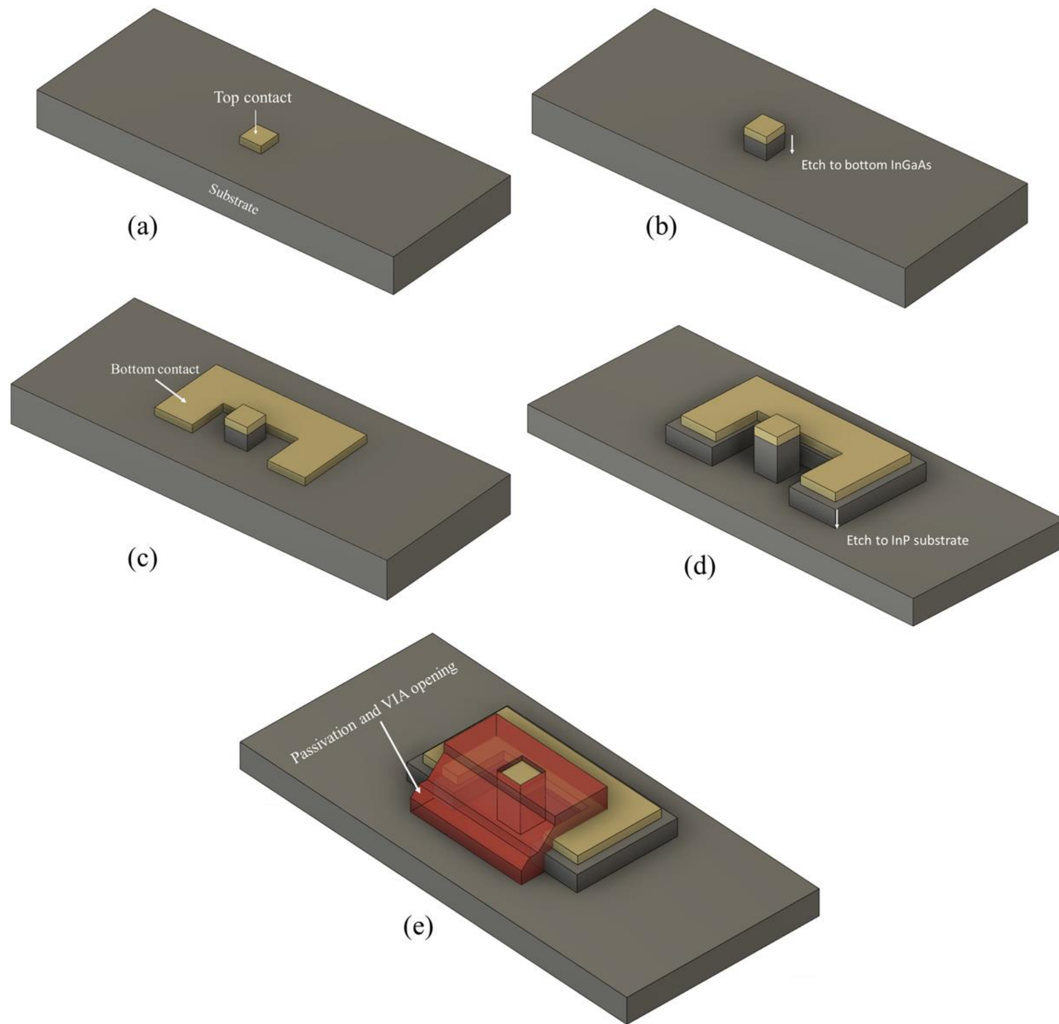

Figure A.1: *Fabrication process: (a) top contact metal deposition, (b) etch to bottom InGaAs layer, (c) bottom contact metal deposition, (d) etch to InP substrate, (e) deposit polyamide and open VIA for bond pad contact*

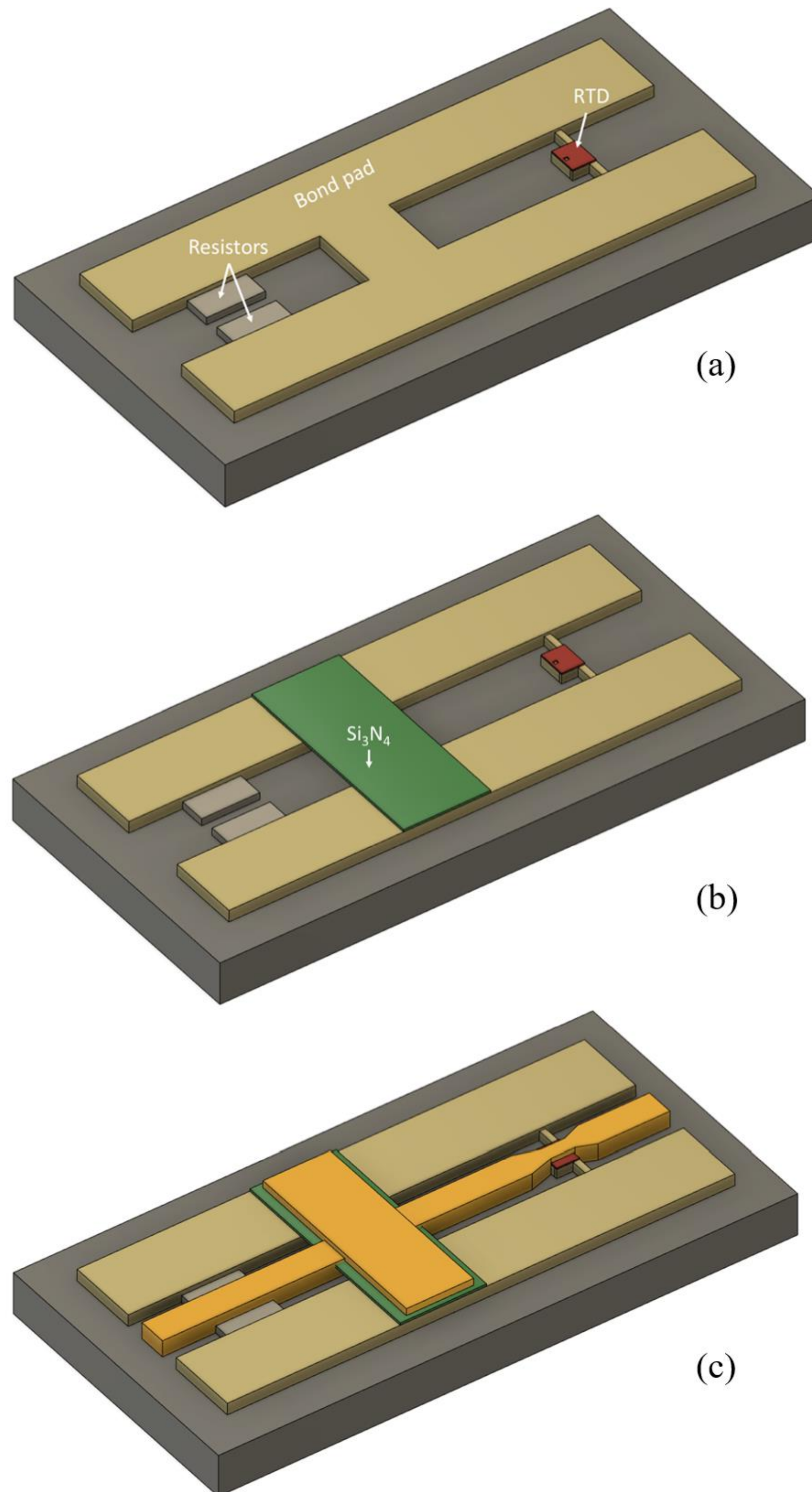

Figure A.2: *Fabrication process: (a) thin-film resistor and 1st bond pad metal deposition, (b) dielectric silicon nitride deposition (Si_3N_4), (c) 2nd bond pad metal deposition*