The Fabrication of GaAs Membrane and GaAs/GaAlAs Heterostructure Field Effect Transistor Devices

A Thesis submitted to

the Faculty of Engineering of the

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by

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This thesis is dedicated to my parents.

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Summary

The principal aim of the work presented in this thesis was to develop the techniques for fabricating FET devices on 50 nm thick active $n^+ - GaAs$ membranes. The use of these membranes for electron beam lithography offers the advantage of very high resolution patterning due to the lack of backscattering, and the use of high contrast STEM (Scanning Transmission Electron Microscope) microscopy for very high resolution alignment and analysis.

The electron beam lithographic techniques for fabricating nanostructures on thin substrates (principally thin carbon and Si_3N_4 membranes) are well established in this Department through the effort of previous workers. These techniques were successfully combined with very high resolution alignment to pattern interdigital metal gratings. With 8 nm probe size, alignment accuracy of better than 3 nm was demonstrated and gratings with 24 nm centre–to–centre spacing were fabricated on 60nm thick Si_3N_4 membranes.

The membrane processing techniques were transferred to GaAs and MESFETs successfully fabricated. MESFETs were also fabricated with a fine pitch grating in place of the gate. Electrical characteristics of these devices indicated that surface effects dominated. Comparison between membrane MESFETs and conventional substrated MESFETs permitted an analysis of the effects of the substrate on device operation.

Electrical measurements on membrane devices suggest carriers are confined to a thin layer. A theoretical investigation performed in collaboration with Dr. John Davies of this Department indicates that carrier energies are quantised. In order to substantiate this, GaAs membranes were characterised optically using transmission spectroscopy

and photoconductivity. The use of membranes permitted a signal corresponding to the higher energy band−gap (L−L band) of GaAs to be resolved.

Finally, GaAs MESFETs with gate−lengths of between 0.08μm and 0.2μm were fabricated on a MBE grown heterostructure (n^+ − GaAs/ undoped $Ga_{0.3}Al_{0.7}As$). These devices showed excellent d.c. characteristics with very high transconductance and low output conductance. However, interface effects which degrade pinchoff characteristics were observed.

CONTENTS

Chapter 1 General Introduction

1.1 Introduction

The resolution limiting effect of backscattering in electron beam lithography can be eliminated by the use of thin (or electron transparent) substrates (1.1). The fabrication of 10 nm metal lines and gratings with 40 nm centre–to–centre spacing on 60 nm thick Si_3N_4 membranes (1.2) represents the highest resolution structures formed by electron beam lithography using polymer resists (1.3). Thin substrates also allow the use of high contrast STEM microscopy for very high resolution alignment. On 60nm thick Si_3N_4 membranes, alignment accuracy of 3nm has been demonstrated using an 8nm spot size (1.2). Moreover, wide latitude in exposure and process control are available for making nanostructures on thin substrates (1.4). Therefore, from a research point of view, thin semiconductor membranes may be suited to the fabrication of experimental structures requiring very high resolution lithography (i.e. beyond the resolution limits for patterning on solid substrates).

1.2 Project Aims

The principal aim of this project was to develop the techniques for fabricating FET devices at the limit of electron beam lithography on thin active GaAs membranes. Of particular interest to this work were Lateral Surface Superlattices (LSSLs) and very small geometry MESFETs. Such devices may exhibit electronic properties dominated by quantum and ballistic transport phenomena. Interesting effects predicted in superlattices include negative differential resistance (1.5)

and Bloch oscillations (1.6) thought to be at above 1000GHz (compared with the maximum achievable of about 100GHz by present devices such as the Gunn diode)(1.7). In MESFETs, ballistic transport may occur if the distance electrons have to travel is shorter than their mean free path (1.8−9). This would enable the device to operate at extremely high speed.

The structure of the LSSL was envisaged to be similar to the membrane MESFET but with a metal grating in place of the gate. In order to observe superlattice effects, the period of the grating has to be comparable to electron scattering length (between few tens to few hundreds of nanometres in GaAs). On thin substrates, such gratings can be fabricated with good reproducibility and reliability using electron beam lithography.

In addition to the lithographic benefits gained, fabricating MESFETs on GaAs membranes also provides a means of directly investigating the effects of the substrates on GaAs MESFETs characteristics. Relevent to this work is the influence of the substrates on the performance of short gate−length MESFETs. Decreasing the gate−length can result in worse d.c. characteristics, typified by increased output conductance and poorer saturation and pinchoff characteristics. This trend is clearly demonstrated experimentally by Jaeckel *et al* (1.10). Theoretical studies (1.11−12) indicate that the effects are partly due to injection of carriers from the active channel into the substrate. Therefore, a short gate−length MESFET fabricated on a membrane may exhibit superior characteristics to that on solid substrate. This was the subject of investigation in the second part of the thesis.

1.3 Thesis Outline

The electron beam lithographic techniques used throughout this work are reviewed in Chapter 2. In addition, a method for fabricating interdigital gratings on 60nm thick Si_3N_4 membranes is described. This allows patterning of gratings with centre–to–centre spacings smaller than the resolution limits imposed by interproximity and resist effects. The finest gratings fabricated consisted of 16nm lines with 24nm pitch which are the closest spaced gratings reported on any substrates.

50nm thick GaAs membranes with 3×10^{18} cm^{-3} doping density were fabricated by selective etching of GaAs/$Ga_{0.3}Al_{0.7}As$ heterostructures grown by molecular beam epitaxy (MBE) and metal organic vapour phase epitaxy (MOVPE) (Chapter 3). On these membranes, high resolution electron beam patterning was demonstrated together with the formation of ohmic and Schottky contacts. Finally, a strategy for fabricating FET devices was developed

The fabrication of membrane MESFETs and LSSL structures is set out in Chapter 4 along with an alternative method for fabricating membrane MESFETs. Electrical characteristics of the membrane devices were measured which indicated that surface effects dominated. A comparison of the performances of membrane MESFETs to conventional MESFETs on solid substrate was made in order to study substrate effects. In the course of this work, it was discovered that carrier injection which degrades short gate–length MESFETs performance as mentioned earlier was suppressed by the use of a $Ga_{0.3}Al_{0.7}As$ buffer layer.

Electrical measurements on membrane devices in Chapter 4 suggest that carriers are confined to a thin layer. A theoretical investigation indicates that the confinement results in quantisation of

the carrier energies (Chapter 5). Photo−absorption and photoconductivity measurements were performed to probe the calculated quantised energy levels.

The fabrication and evaluation of GaAs MESFETs with $Ga_{0.3}Al_{0.7}As$ buffer layer with gate−lengths of between 0.08μm to 0.2μm are described in Chapter 6. These devices exhibit excellent d.c. characteristics with very high transconductance and low output conductance. The performance of the devices was observed to be affected by the GaAs/GaAlAs interface. A discussion of this is given.

Finally, a summary of the major findings of this work and suggestions for future work are given in Chapter 7.

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2.1 Introduction

This chapter gives an overview of the technology used in the fabrication of micro– and nano–structures. As detailed reviews of electron beam lithographic processing can be found in the theses of Mackie (2.1), Rishton (2.2) and Binnie (2.3), only brief description of the main processes will be given here.

2.2 Electron Beam Lithography

2.2.1 Background

In Electron Beam Lithography (EBL), a focused electron beam is deflected in a controlled manner over an electron sensitive material (usually polymer) known as a resist. The irradiation modifies the resist's molecular structure such that either the exposed or the unexposed resist can be dissolved selectively in a developer. The developed resist layer can then be used either as a stencil to transfer a metallic pattern (liftoff process) or as a mask for etching. The process is illustrated in Figure 2.1.

2.2.2 The EBL System

The Glasgow EBL system is shown schematically in Figure 2.2. The key components of the system are:

Philips PSEM S500 Electron Microscope (2.1)

The Philips machine has been modified for electron beam writing. Its essential features are:

a) electron spot sizes ranging from 8 nm to 1 micron

b) variable accelerating voltage from 1.5 to 80 kV

c) a specially fitted transmission detector for Scanning Transmission Microscopy (STEM)

d) a fully eucentric goniometer on which a specimen can be positioned in the X and Y directions in 1 μm steps and rotated with an accuracy of 1/68th of a degree

e) X– and Y– electronic beam shifters for fine positioning in the X and Y directions of up to ± 10 μm

f) X– and Y– Varymag control which allows the magnification and therefore frame size in the X and Y directions to be increased continuously by a factor between 1 and 2.5

g) beam blank which, when switched on, deflects the beam into an aperture thus avoiding unwanted exposure.

GEC 4180 Computer

Pattern files are designed, generated and edited in the GEC 4180 computer using an interactive pattern editor called DESIGN (2.1).

ITHACA Microcomputer

This is linked to the GEC 4180 computer and the electron microscope. Pattern files generated by DESIGN are transferred to the

microcomputer where they are stored in a disc. When a program (EBSS) is run on the microcomputer, the pattern data is fed into the scan generator which controls the beam deflection via D/A converters connected to the scan coils.

2.2.3 Resist

Resists are classified as either positive or negative, depending on how they respond to exposing radiation (2.1−4). Positive resists are rendered more soluble and is dissolved selectively in a developer. The reverse effect occurs for the negative resists. This distinction is illustrated in Figure 2.1.

The positive resists used were Poly(Methyl Methacryalate) (PMMA) with molecular weights of 185,00 and 350,000. Two resist systems were used:

1) 1 μm thick layer 185,000 MW PMMA

2) a bilayer resist system consisting typically of a 20 nm thick layer of 350,000 MW PMMA on a 100 nm thick 185,000 MW PMMA layer.

Resist (1) is obtained by spinning 15% w/w of the PMMA solution (in chlorobenzene) at 5000 rpm for 60s. For resist (2), 4% w/w 185,000MW PMMA solution (in xylene) and then 4% w/w 350,000 MW PMMA (in xylene) are spun for 60s at 6000 rpm and 8000 rpm respectively. The bottom layer is baked at 180°C for at least 1 hour before coating on the top resist layer. Both resist systems are hardened by baking at 180°C for at least an hour before exposure. It is necessary to bake the resists overnight at 180°C if they are to be used as wet etch masks.

Resist (1) is used for patterning coarse features requiring thick metallisation while the bilayer resist is suitable for defining high resolution patterns. The developers are 1:1 MIBK:IPA and 1:3 MIBK:IPA for the thick resist and the bilayer resist respectively. Both resist systems are thought to develop into undercut profiles (Figure 2.3) which facilitate lift–off. In the case of resist (1), the undercut profile results from the divergence of the electron beam by electron scattering as it passes through the resist film (2.2). The undercut in resist (2) arises because the lower resist layer is more sensitive than the top layer. Therefore, when the resist is developed, more material is dissolved from the bottom layer, leaving an undercut profile as shown in Figure 2.3 (2.5).

2.3 Alignment Techniques

Alignment is necessary for positioning a pattern in one process level accurately with respect to another pattern defined in a previous level. Two alignment techniques were used, one for low resolution work on thick substrates and the other for high resolution alignment on thin substrates. The techniques rely on the fact that the position of an image seen on the screen of the electron microscope corresponds to the position of the electron spot on the specimen.

POSITION

POSITION (2.1) is a computer program for calculating exposure positions on a wafer in terms of the goniometer coordinates. The positions are aligned to the wafer axes with the bottom left corner taken as the reference point and are spaced at regular intervals in the

X and Y directions on the wafer. Therefore, these positions can be located at a subsequent lithographic level using POSITION i.e. the program facilitates approximate positioning required for alignment.

2.3.1 Low Resolution Alignment Technique

This technique was used extensively for alignment of coarse features at X80 magnification (1.5 by 1.2 mm frame size) on thick substrates. An example is in the alignment of isolation and ohmic levels in the fabrication of GaAs MESFETs (Chapter 4).

Registration Marks

The standard registration mark pattern is shown in Figure 2.4. It consists of a pair of rectangles aligned in the horizontal and vertical directions to form a T− shape near each corner.

Coarse Alignment

Using POSITION, the sample is moved approximately to the first exposure site. A coarse alignment pattern which consists of a 20 pixel pitch (horizontal) grating and partial outlines corresponding to the top horizontal rectangles of the alignment marks is scanned at a speed of 2 μs per pixel. The scan speed is the fastest that can be driven by the scan generator. The scanned pattern allows the top pair of T− shape rectangles to be viewed thus enabling the operator to determine how the exposure frame is positioned with respect to the registration marks. At this stage, there is usually a significant offset between the scanned partial outlines and the corresponding rectangles

in the X– and Y– directions and in the orientation of the wafer. These offsets are corrected approximately by dead reckoning (i.e. with no image on the SEM screen) and then checked by scanning the alignment pattern for a second time.

Fine Alignment

Two fine alignment patterns are scanned, one at a time, over the alignment marks at 2 μs/pixel. The first contains partial outlines corresponding to the horizontal rectangles, while the second consists of partial outlines corresponding to the vertical rectangles of the registration marks (Figures 2.5a and b). The exposure frame is deemed to be aligned to the registration marks when either scanned pattern coincides with the corresponding registration marks. This is achieved by adjusting the rotation, the beam shifters and the varymag controls. The main reason for using two sets of scanned patterns is to avoid scanning a particular area more than twice so that unnecessary exposure of the resist is prevented. This alignment technique is accurate to within 0.5 μm.

2.3.2 Very High Resolution Alignment

The use of thin substrates for electron beam lithography offers the advantage of high resolution due to the lack of backscattering and the use of high contrast Scanning Transmission Electron Microscopy (STEM) for imaging and analysis (2.1,2.6). A very high resolution alignment technique that exploits the high contrast and high resolution STEM imaging on thin substrates had been developed in this department by Mackie (2.7). The method was modified slightly and

was applied for fabricating interdigital gratings on thin substrates.

2.3.2.1 Alignment Method

When operating in STEM mode, the contrast achievable in the Philips machine is such that when about 20% of the electron spot is obstructed from the transmission detector, the spot changes from bright to dark on the screen. If an electron beam with diameter d is scanned across a metal line of width x, the change in contrast should just occur when the centre of the spot is at a distance $(0.3d + x/2)$ from the centre of the metal line (Figure 2.6). If the spot is scanned in parallel to the metal line, the whole scanned line will be either bright or dark. The alignment test which involves aligning the scanned line with the metal line should then give an overlay accuracy of about $\pm(0.3d + x/2)$.

The above alignment method can be improved by using a three segment line scan as shown in Figure 2.7 (2.7). The condition for all 3 segments to appear dark simultaneously is $0.3d + x/2 \geq p$ (Figure 2.7), where p is the displacement between the centre and the end segments. By increasing the displacement p, there is a point at which the condition is just satisfied i.e. $0.3d + x/2 = p$. When this happens, the centre segment should be aligned to the metal line such that a slight misalignment results in one of the end segment turning bright as illustrated in Figure 2.8. As the displacement can only be varied by an integral number of pixel, alignment accuracy of within one pixel might be expected. Therefore, the accuracy should improve with smaller frame size i.e. smaller pixel size.

The very high resolution alignment technique exploits the above facts. The method developed by Mackie with one minor change was

used. The alignment marks are shown in Figure 2.9. The blocks and the T− bars are used for coarse and fine alignment respectively. During alignment, the pattern shown in Figure 2.10a is scanned repeatedly over the alignment marks. A magnified view of one corner of the pattern is shown in Figure 2.10b. It consists of a vertical and a horizontal rasters designed for viewing of alignment marks on the screen. The extended lines are the reference lines corresponding to the positions of the T− bars. Each of these lines is made up of 3 segments, the centre segment having the same X− (or Y−) coordinates as the vertical (or horizontal) line of the T− bar. The displacement between the end segments and the centre segment is 1 pixel.

Coarse alignment is carried out initially by moving the blocks of the alignment marks to either side of the corresponding T− bar using the beam shifters. Fine alignment is then performed by adjusting the stage rotation, X and Y precision magnification (varymag) control and the beam shifters to change the shape and position of the scanned alignment marks until all 3 segments of each reference line appear dark at the same time i.e. until all 4 T− bars are aligned at once.

The fine alignment procedure is repeated using a series of the scanned patterns (Figure 10a) which are identical except that the displacement between the centre and the end sections of the reference lines are increased progressively by a pixel. This is stopped when the displacement is too large for all three sections of the reference lines to turn dark at the same time. When this happens the condition $0.3d + x/2 = p$ is very nearly satisfied.

This high resolution alignment technique was used for fabricating interdigital gratings which is described below.

2.4 Fabrication of Interdigital Gratings

2.4.1 Introduction

The resolution of a electron beam written grating is limited by interproximity and resist effects (2.1, 2.2, 2.8). These effects can be overcome by using two lithographic stages. The method is outlined below.

a) Perform resolution tests to find the minimum reproducible pitch

b) Level 1– write lines 1,3,5,7,.....(Figure 2.11)

c) Develop pattern, metallise and lift–off

d) Spin on fresh resist. Align second exposure level to Level 1

d) Level 2– write lines 2,4,6,8,.....(Figure 2.11)

e) process as (c).

The interdigitation technique was developed for fabricating Lateral Surface Superlattices on the 50 nm thick GaAs membranes described in Chapters 3 and 4. Si_3N_4 membranes (60 nm thick) were readily available and initial tests were conducted with these before extending these experiments to the GaAs membranes. The Si_3N_4 experiments are described below.

2.4. Fabrication Procedure

A high resolution 2 layer resist system comprising of 40 nm of 350,000 MW PMMA on 40 nm of 185,000 MW PMMA was used throughout. This was baked (180^{o}C) overnight before exposure.

Resolution Tests

The pattern shown in Figure 2.12 was used for the resolution tests. It contains a matrix of gratings in which exposure dose and pitch are varied along rows and columns respectively. The pattern was written with a 8 nm electron spot of 50 keV energy in a 12.5 X 9.5 μm frame. After exposure, the specimen was developed in 1:3 MIBK:IPA at 23^{o}C for 20s followed by a 30s rinse in IPA. 10 nm of Au/Pd was subsequently evaporated onto the specimen and lift−off performed in chlorobenzene using the shooting technique (2.9).

Interdigital Gratings

A pattern consisting of gratings with a range of pitches together with the high resolution alignment marks (Figure 2.13) was exposed in a 12.5 X 9.5 μm frame. 50 kV electron beam with 8 nm spot size was used. After exposure, the specimen was processed as above. Fresh resist was spun on after liftoff. The second exposure level was aligned to the first using the high resolution technique described earlier. Once aligned, the second set of identical gratings was written between the fingers of the gratings previously exposed. This resulted in interdigital gratings with half the pitch of the original sets. Accuracy of the alignment was better than 3 nm. A TEM micrograph, Figure 2.14, which shows one of the finest grating thus fabricated. The grating consisted of 16 nm lines with 24 nm pitch (i.e. spaced 8 nm apart). This is the finest pitch grating reported to date on any substrate (2.10).

2.5 Fabrication of MOP masks

Electrical isolation for all FET devices fabricated in this work was achieved by boron implantation. Metal On Polymer (MOP) masks were used to define active areas. The bombardment of epitaxial GaAs with the energetic ions causes formation of deep traps and renders it semi– insulating.

2.5.1 Fabrication Procedure

The MOP mask consists of a 800nm thick Ge layer on a 0.3 μm layer of polyimide. This is fabricated using a bilayer resist comprising of a 1 μm thick 185,000 PMMA layer on a 0.3 μm thick of polyimide.

Procedure (2.11)

A 0.3 μm thick polyimide layer is first coated on a wafer by spinning 10% w/w Polyimide solution (solvent 35:65 by volume of acetophenone:xylene) at 5000 rpm for 60s. This is baked at 180^{o}C for an hour before coating the wafer with a 1 μm thick PMMA layer (15% w/w solution in chlorobenzene at 5000 rpm for a minute). The bilayer resist is then baked for 2 hours at 180^{o}C before exposure.

Exposed PMMA is developed in 1:1 MIBK:IPA at 23^{o}C for 60s. 10nm of NiCr followed by 800nm of Ge are evaporated, liftoff performed in acetone. The NiCr enhances adhesion of the Ge layer to the polyimide. Finally, unexposed polyimide is developed in 1:1 acetophenone:xylene at room temperature for 2 minutes. The fabrication process is illustrated in Figure 2.15.

After implantation, MOP masks were removed by dissolving the polyimide layer in boiling acetophenone.

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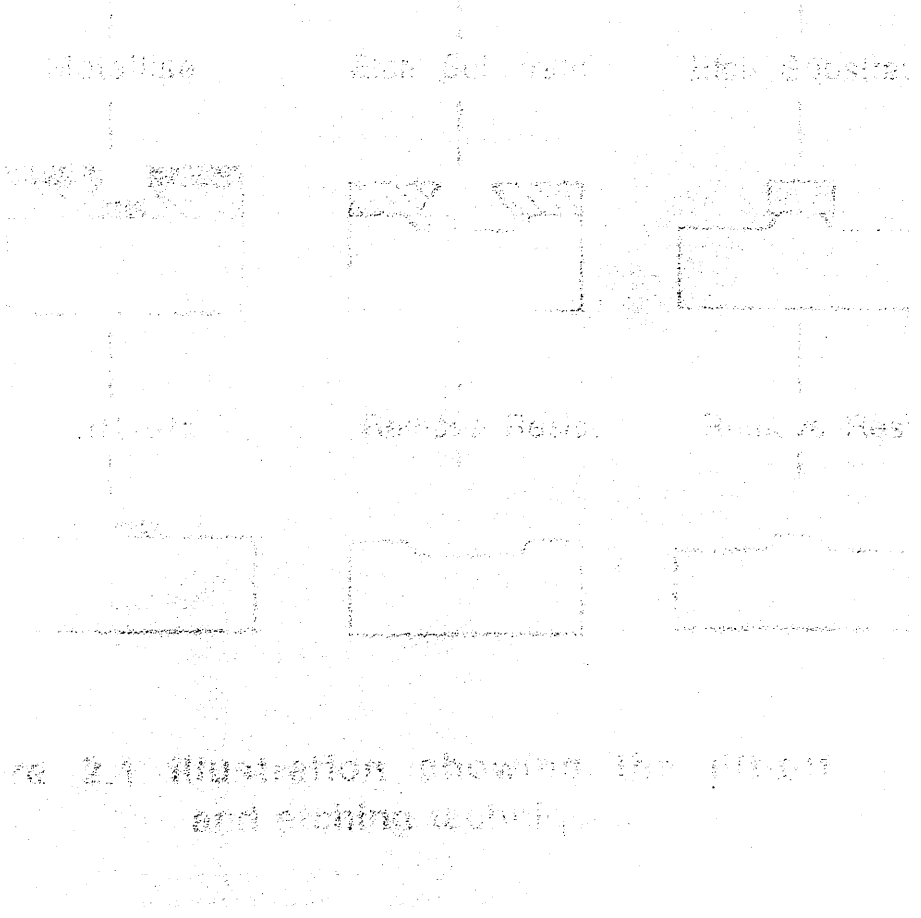


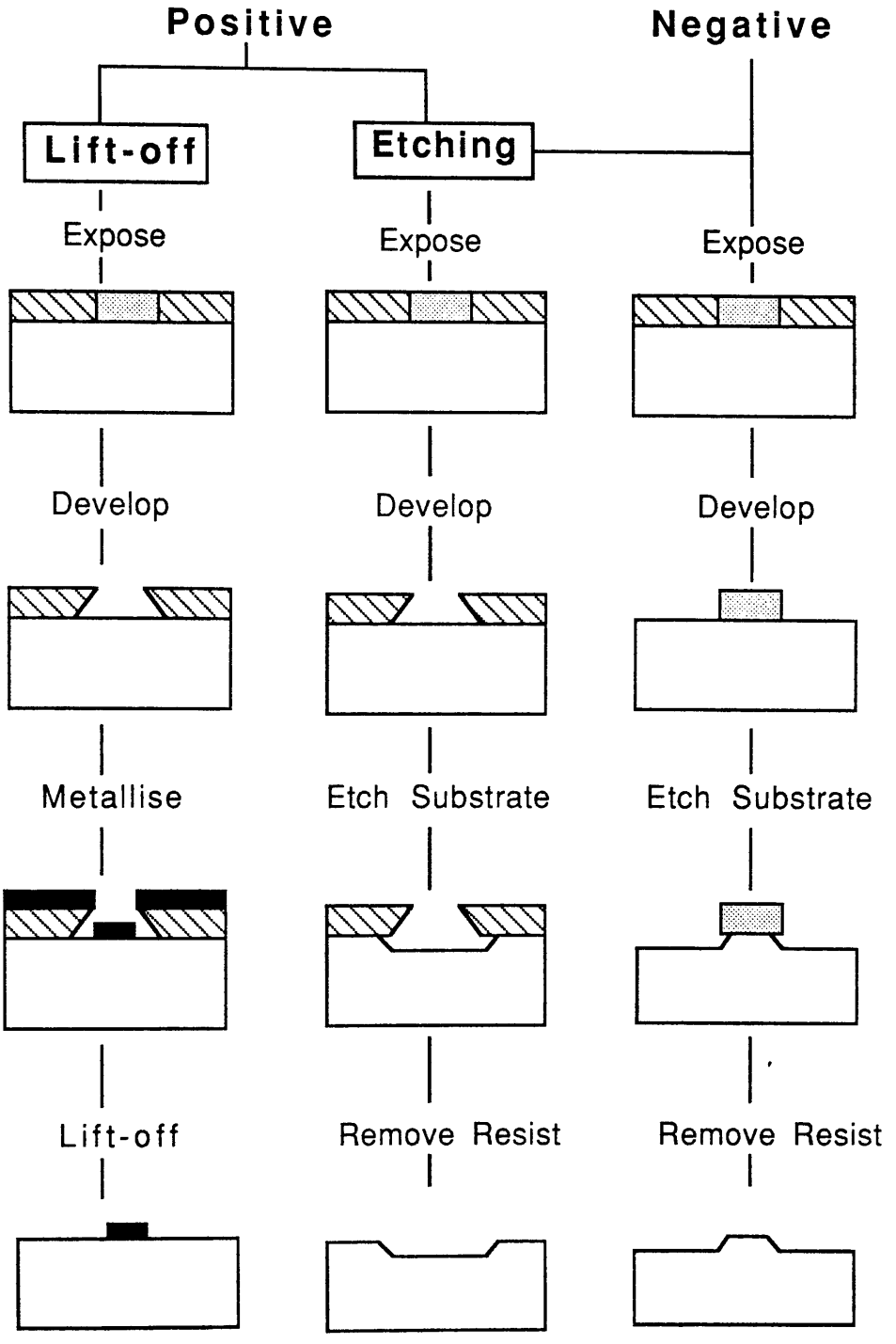


Figure 2.1 Illustration showing the lift-off and etching techniques.

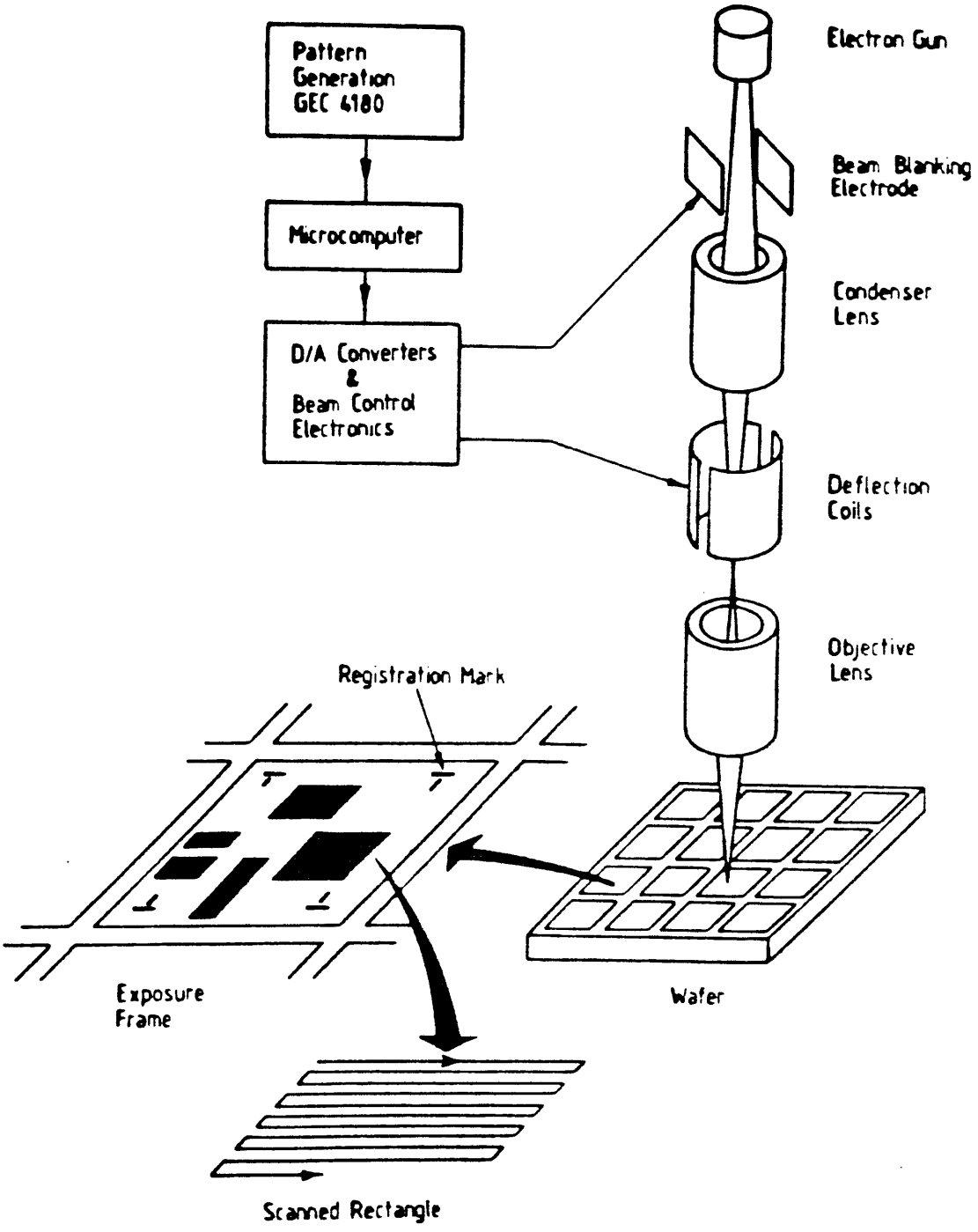
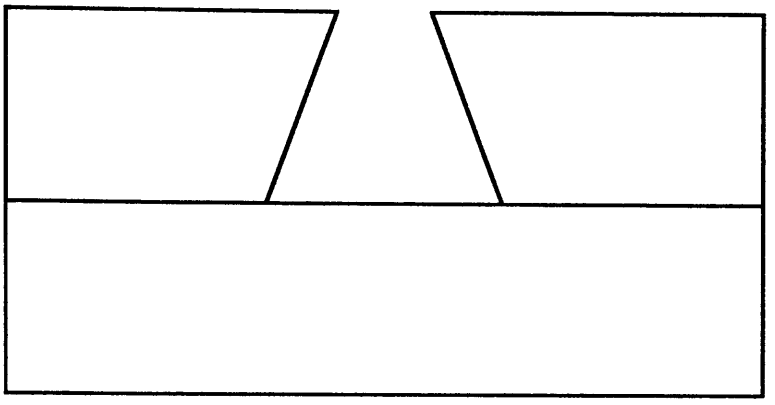
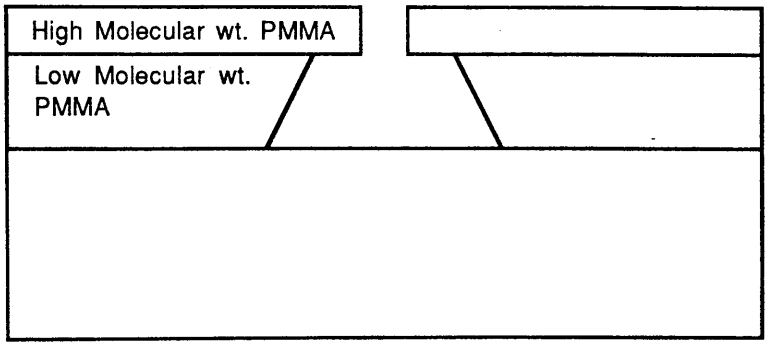


Figure 2.2

The Glasgow Electron-beam Lithoraphic System (After Patrick, ref. (2.12)).



(a)



(b)

Figure 2.3 Developed Profiles of (a) thick (1μm) PMMA and (b) bilayer resist system

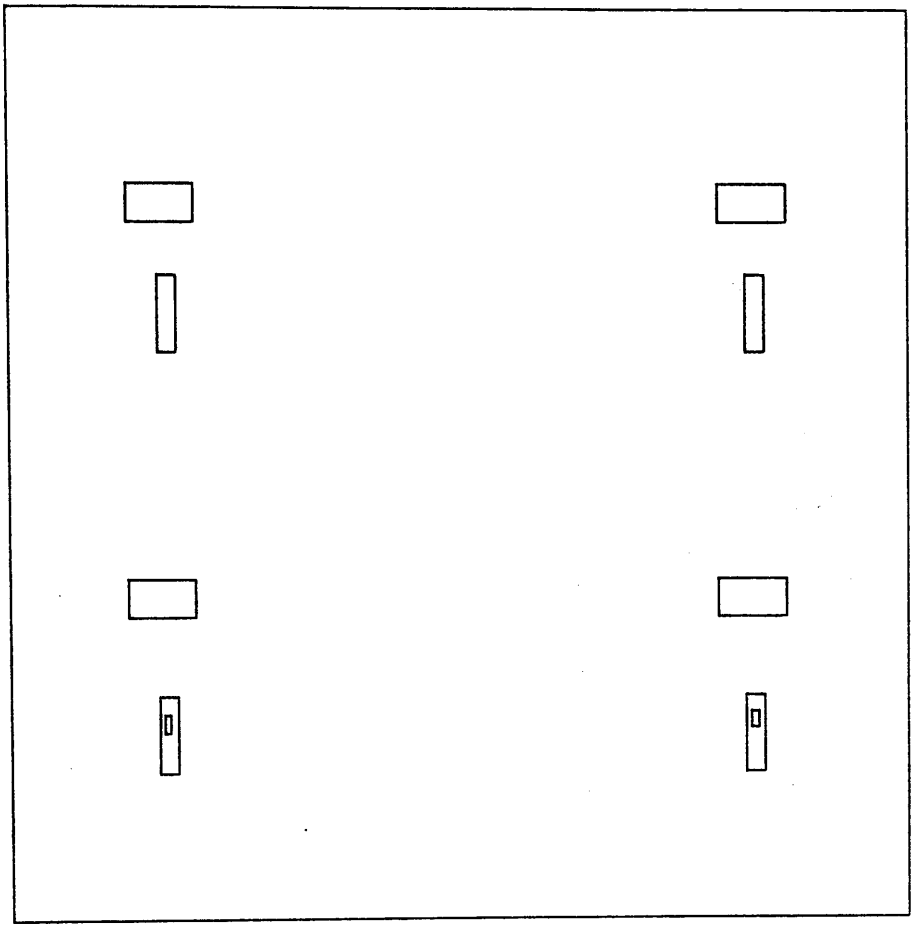


Figure 2.4 Standard Registration Mark Pattern.

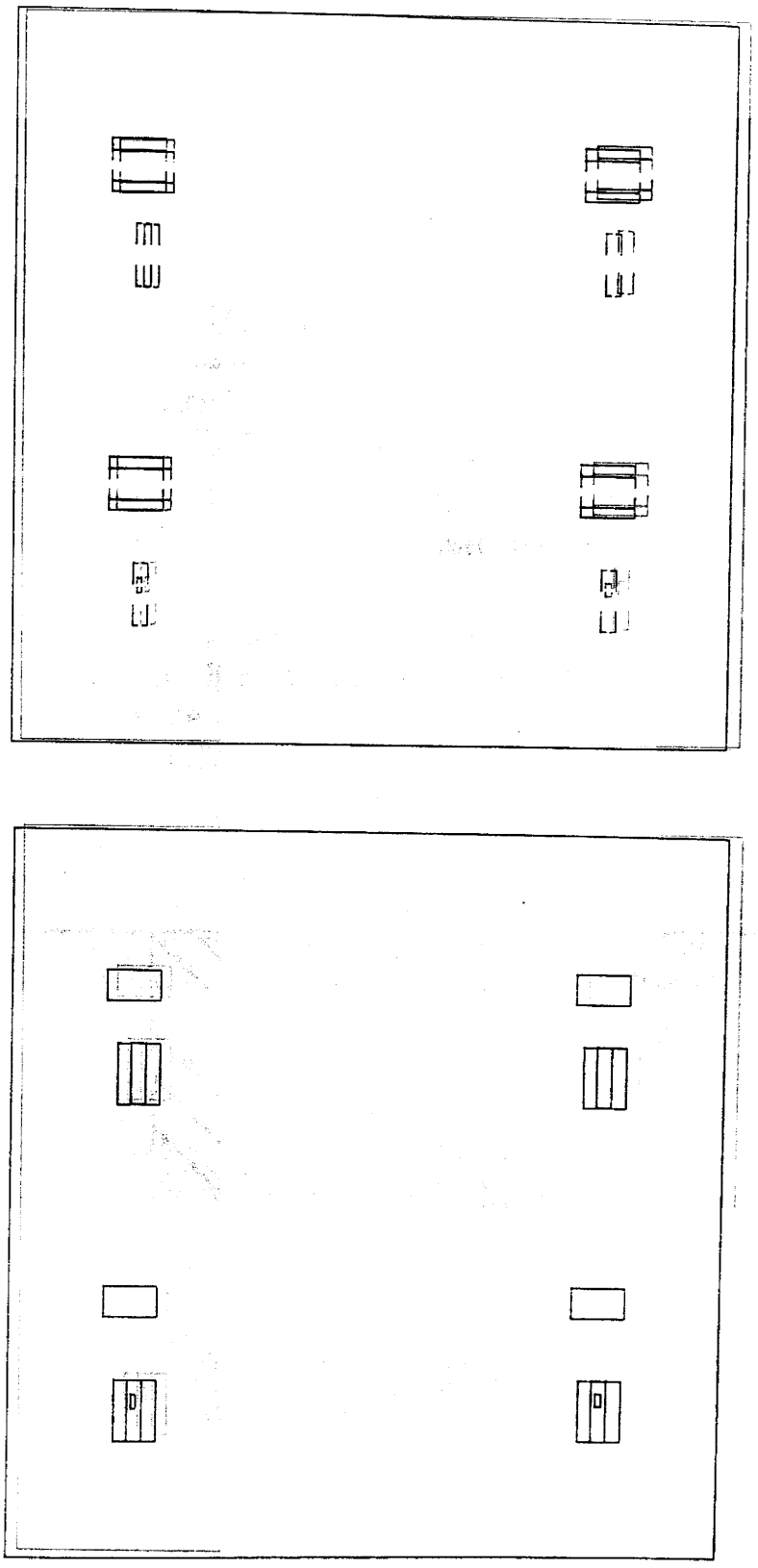
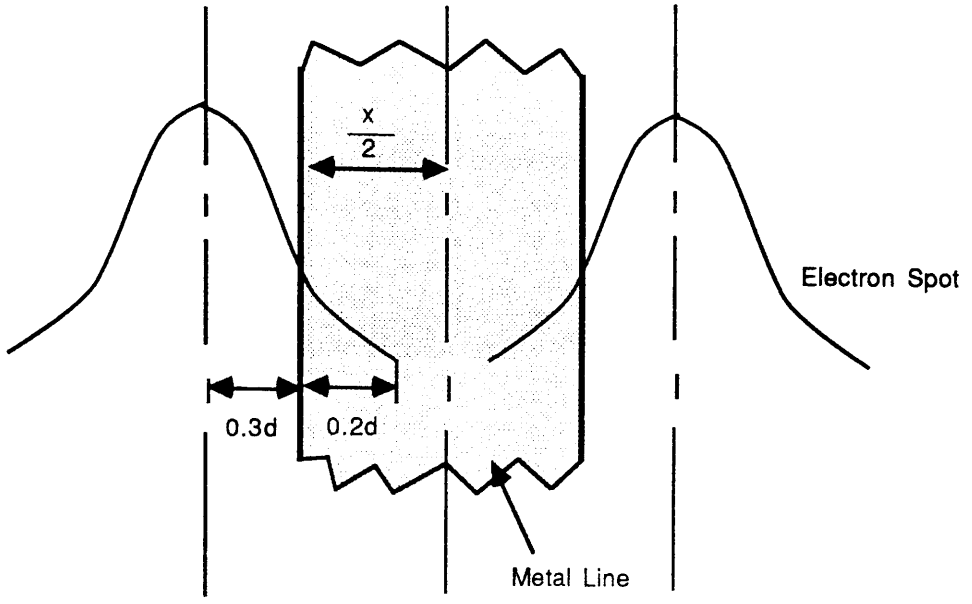
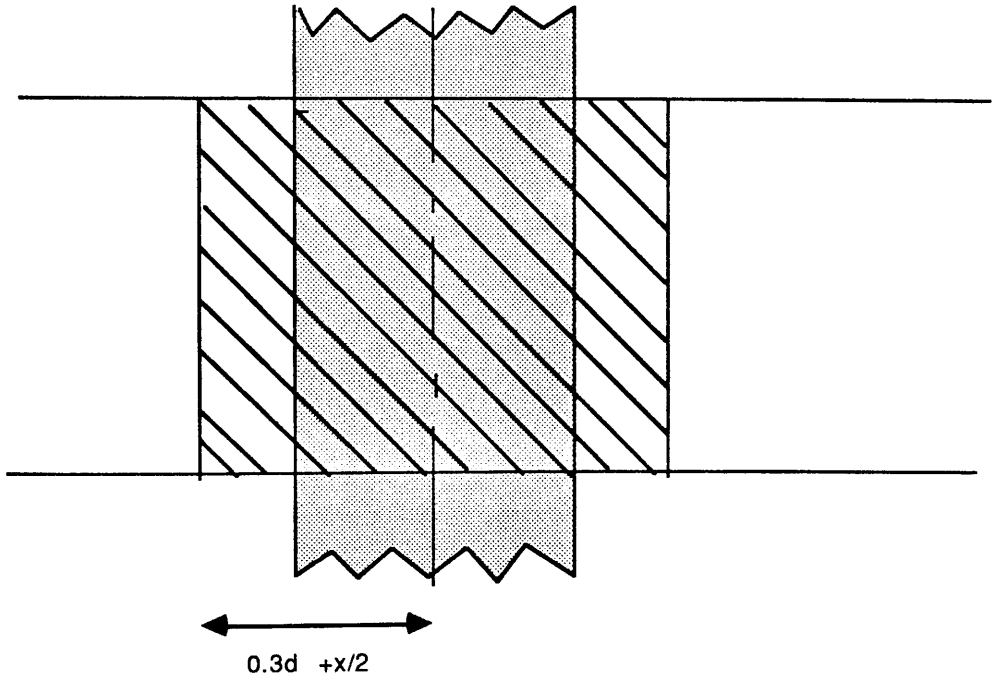


Figure 2.5 Scanned Alignment Patterns

Positions of (a) Horizontal and (b) Vertical scanned patterns relative to standard registration marks are shown schematically.

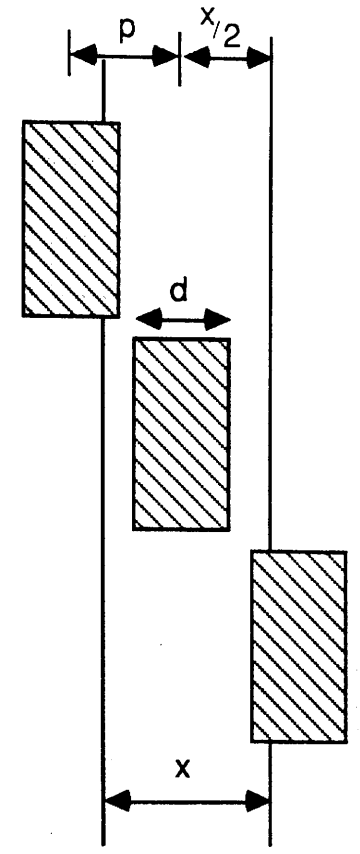


An electron beam with spot size d turns from bright to dark when about 20% of the beam diameter crosses the metal line i.e. when the separation between the centres of the beam and the line is $0.3d + \frac{x}{2}$

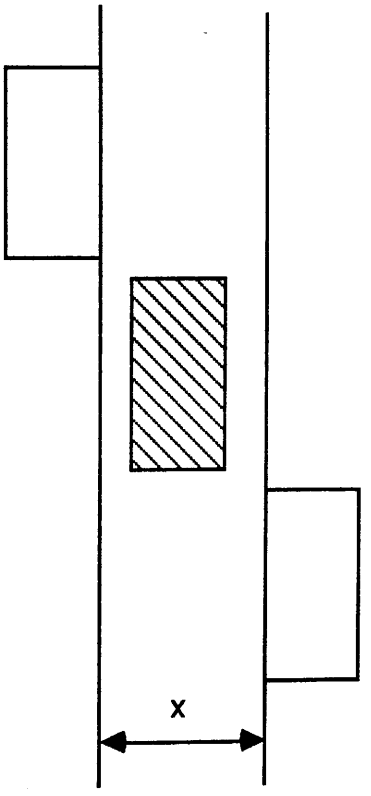


If the beam is scanned in parallel to the metal line, the scanned line turns dark if the centre of the spot is within  region

Figure 2.6



Condition for all 3-segments to turn dark at the same time is $p \leq 0.3d + x/2$



If $p > 0.3d + x/2$ only one segment can turn dark at a time

Figure 2.7

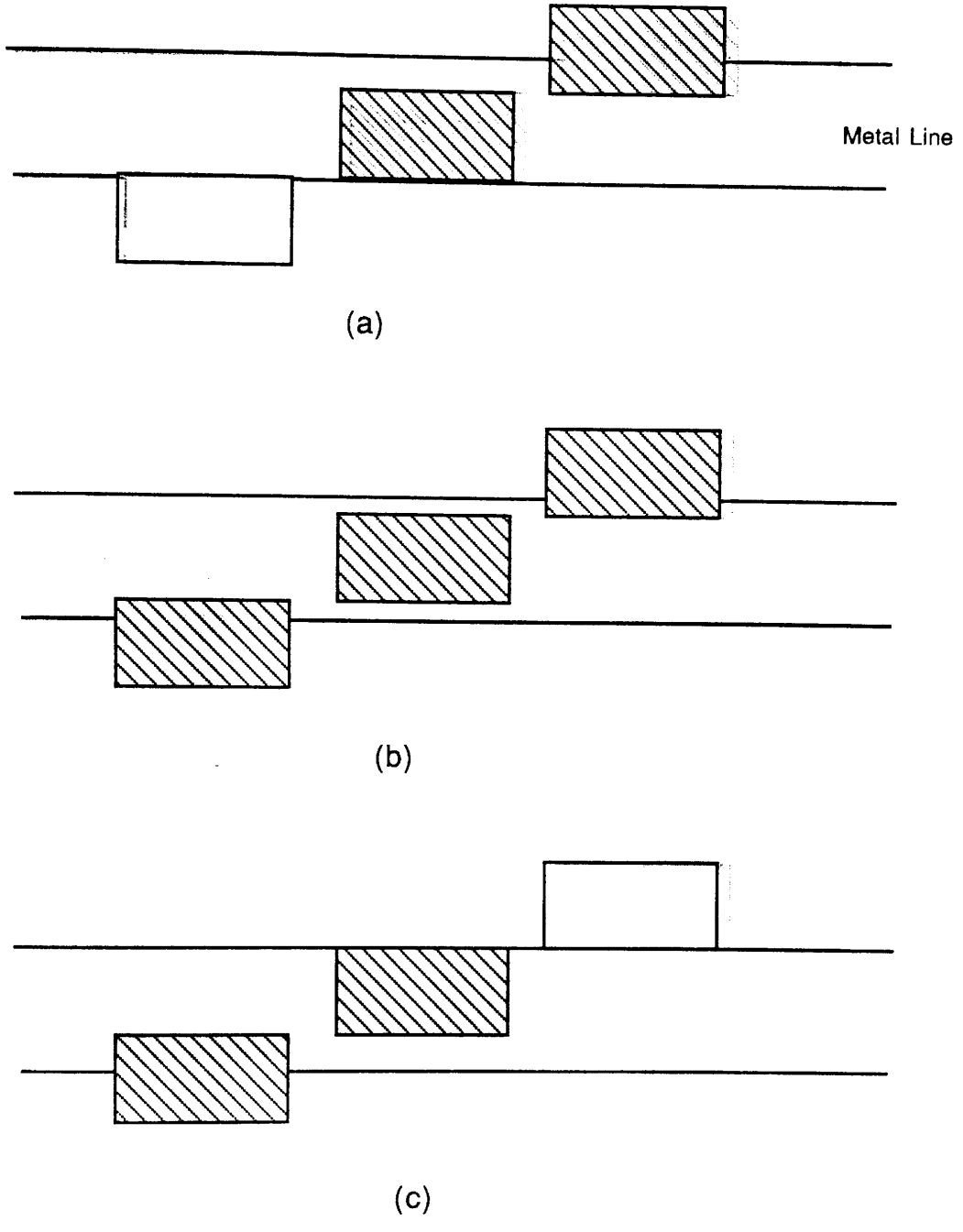


Figure 2.8 Very High Resolution Alignment

Using a 3-segment scan, a slight misalignment (a & c) results in one of the end segment turning bright.

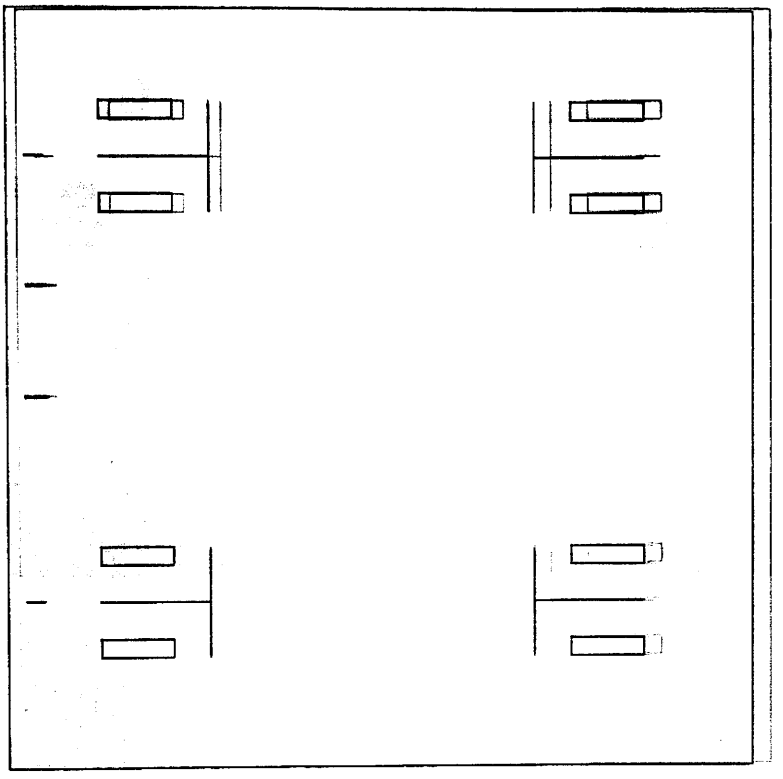
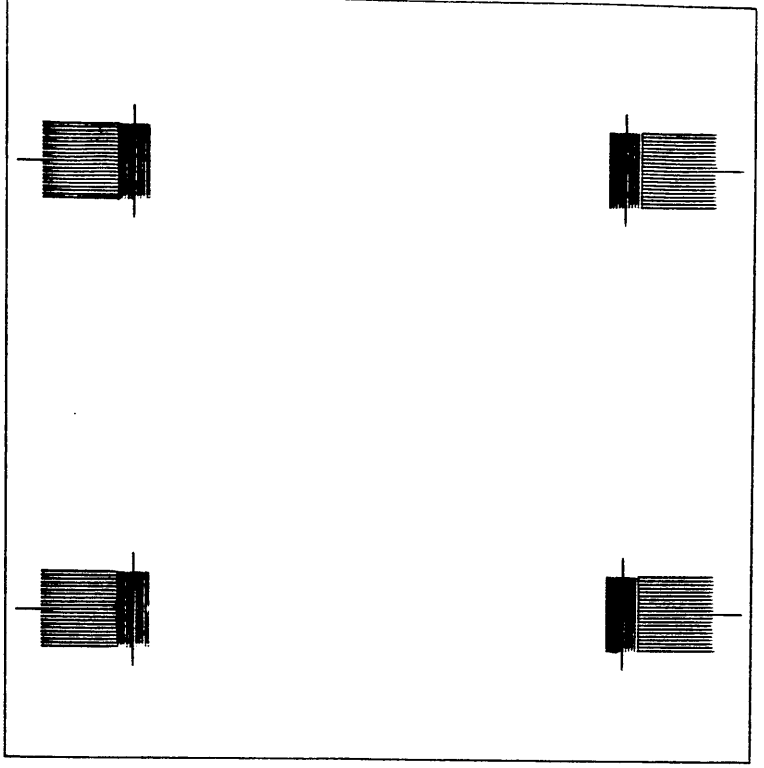
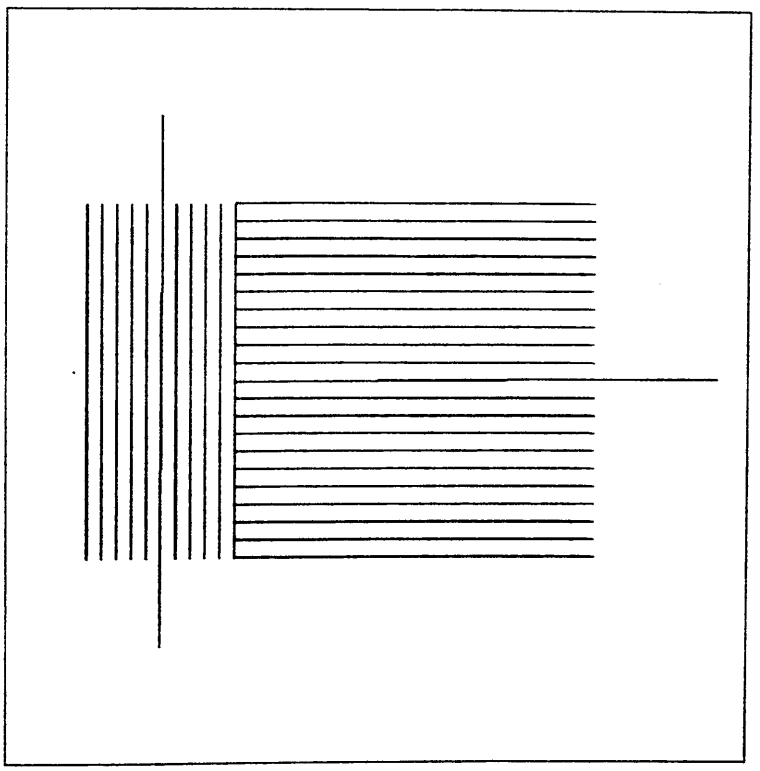


Figure 2.9

Alignment Mark Pattern for Very High Resolution Alignment.



(a)

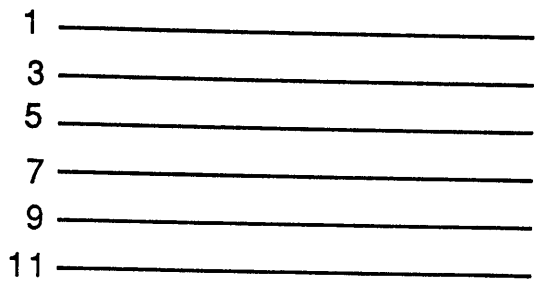


(b)

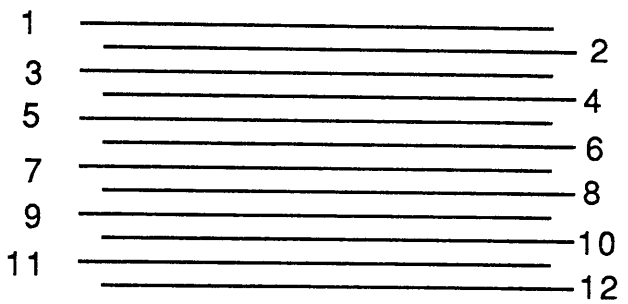
Figure 2.10

a) Scanned Alignment Pattern for Very High Resolution Alignment

b) Magnified view of one corner



1) Pattern lines 1,3,5,7,9 & 11



2) Coat fresh layer of resist and pattern lines 2,4,6,8, 10 & 12 between the fingers of the first set of grating

Figure 2.11 Fabrication of Interdigital Grating

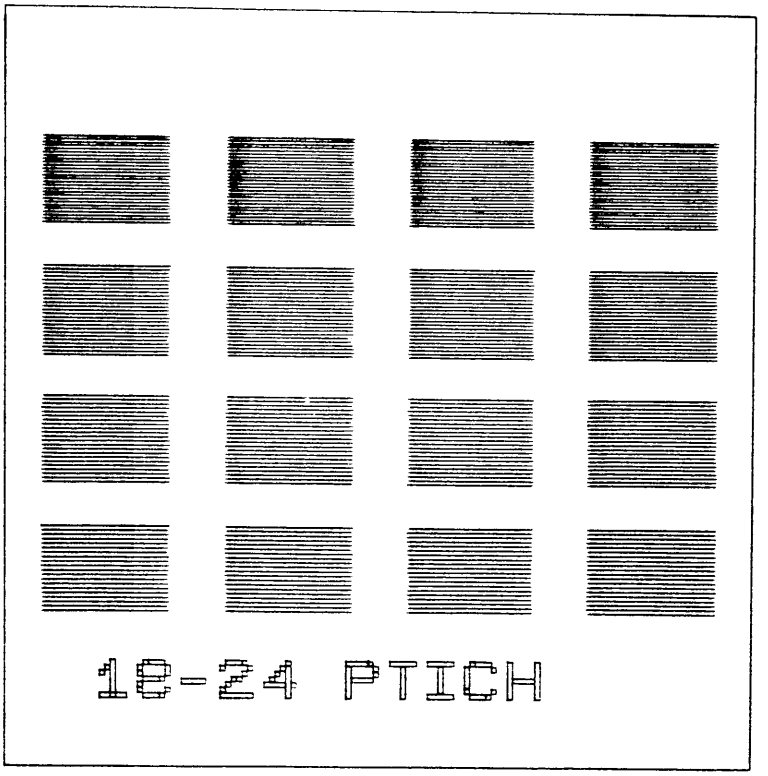


Figure 2.12

Grating Resolution Test Pattern

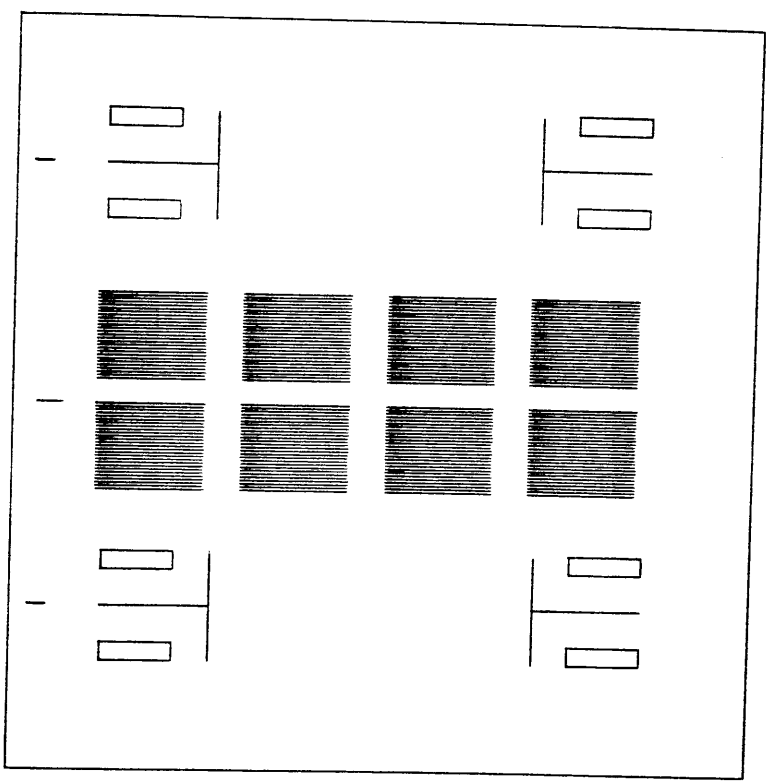


Figure 2.13

Pattern used for exposure in the fabrication of interdigital gratings.

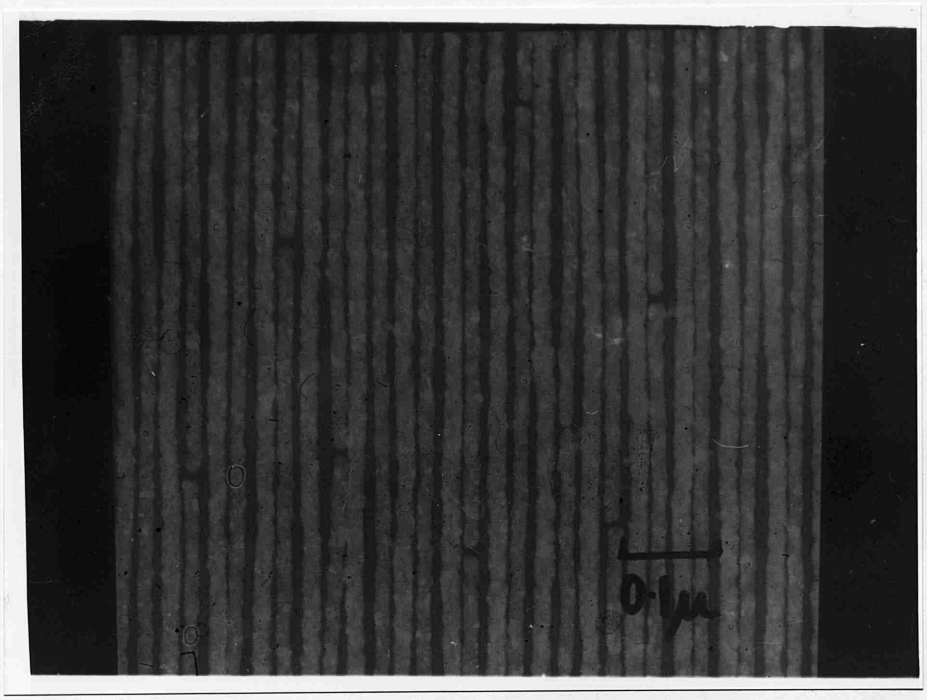


Figure 2.14

TEM micrograph of a interdigital grating with 24nm centre-to-centre spacing and 16nm linewidth (8nm gaps). The grating was fabricated on 50nm thick Si_3N_4 membrane using 2 lithographic stages.

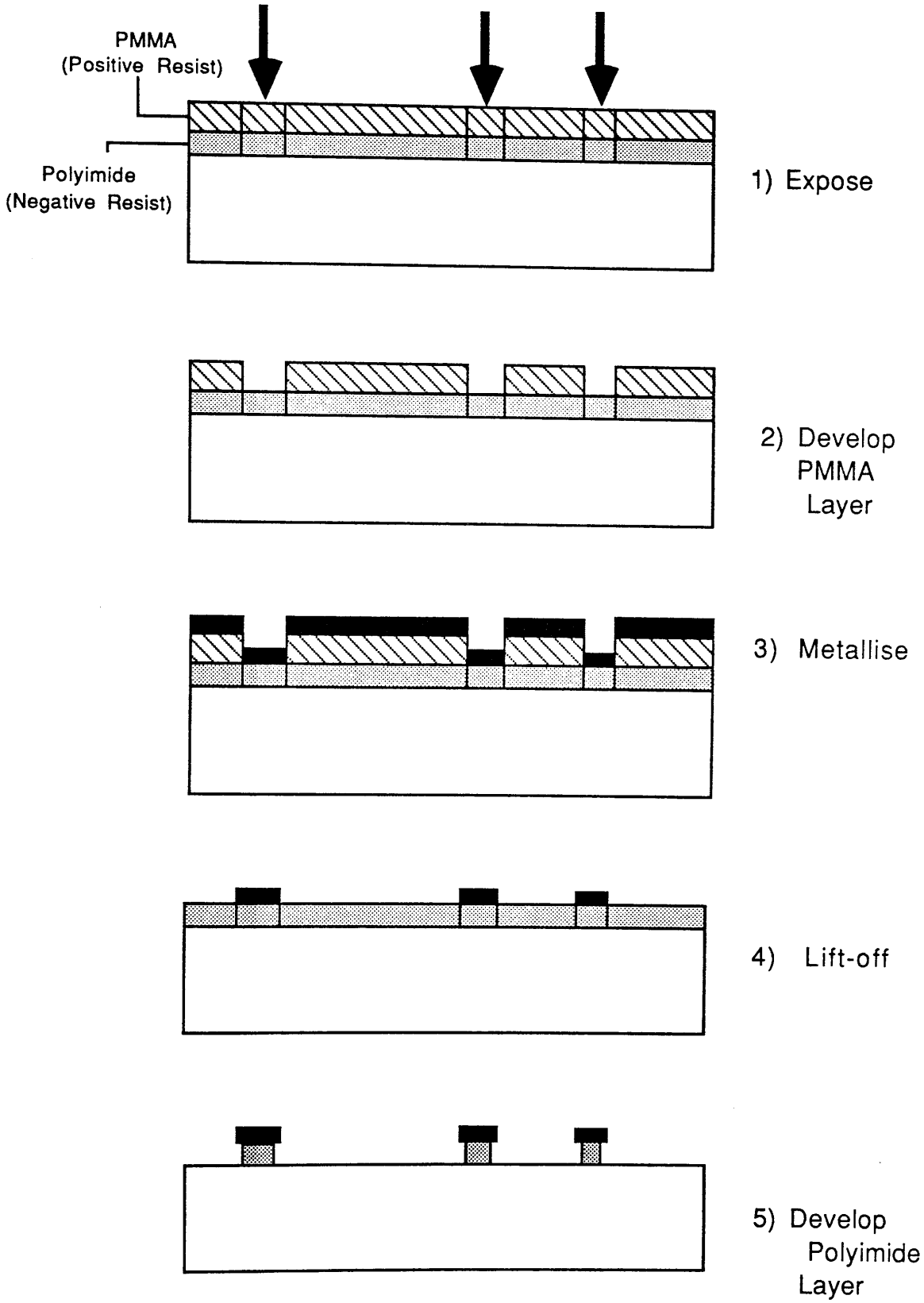


Figure 2.15 Fabrication of Metal On Polymer Mask

Chapter 3 The Fabrication of GaAs Membranes

3.1 Introduction

This chapter is concerned with work carried out to explore the feasibility of fabricating FET devices on 50 nm thick GaAs membranes. The method used for producing the GaAs membranes is first described. Next, the development of the techniques and processes required for making the membrane devices are presented.

3.2 Fabrication of 50 nm Thick $n^+ - GaAs$ Membranes

GaAs membranes were initially made from MOVPE (Metal Organic Vapour Phase Epitaxy) wafers using the method developed by Mackie (3.1). The reliability and the reproducibility of the method were later improved by making some modifications. This included using wafers grown by MBE (Molecular Beam Epitaxy).

3.2.1 Fabrication Outline

The starting material was a GaAs/GaAlAs heterostructure designed specially to facilitate membrane fabrication. As shown in Figure 3.1, the heterostructure consisted of GaAs/GaAlAs etch stop layers and a top active GaAs layer grown on a semi− insulating GaAs substrate. Membranes were formed by removing the underlying etch stop layers from the back surface with selective GaAs/GaAlAs etches. The method is shown schematically in Figure 3.2. The main steps are:

1. Pattern and open etch windows into a NiCr/Au mask on the

back surface of the wafer.

2. Etch GaAs through the windows in a fast non selective etch to within 10 μm from the top surface.

3. Etch remaining GaAs and the etch stop layers in selective etches until the top GaAs layer remains.

3.2.2 Material

The starting wafers were grown by MOVPE at Sheffield University (3.2) and by MBE in this department (3.3). The main features of the heterostructure (Figure 3.1) are:

a) GaAs and $Ga_{0.3}Al_{0.7}As$ etch stop layers: the Al concentration was selected in order to obtain high GaAs/GaAlAs etch selectivity.

b) 50 nm thick GaAs active layer n− doped to a concentration of 3 X 10^{18} cm^{-3}. This layer formed the final membrane; very high doping density was therefore required to prevent total carrier depletion from both surfaces (3.4). At this doping density and assuming a surface barrier height of 0.7 eV (due to surface states), the calculated depletion width from each surface is 17nm (see Chapter 5).

All layers were grown on (100) semi− insulating GaAs wafers.

3.2.3 Etches (3.1)

The following etches were used:

1) 1:8:1 H_2SO_4: H_2O_2: H_2O

This is a fast non selective anisotropic etch which etches GaAs at a rate of about 15 μm/minute when freshly prepared. The etch rate drops to less than 10 μm/minute as it cools.

2) 95:5 H_2O_2: NH_3

This etches GaAs at a rate of about 2 μm/minute and was used as the selective etch for GaAs. Its etch rate for $Ga_{1-x}Al_xAs$ drops exponentially with increase in x, becoming negligible for x greater than 0.3.

3) 20% HF

This does not etch GaAs but etches $Ga_{1-x}Al_xAs$ at a rate which increases exponentially with x. It was used as the selective GaAlAs etch (20% HF etches $Ga_{0.3}Al_{0.7}As$ at about 1 μm/minute).

For each of the above etches, it was necessary first to wet the resist by immersing the samples into IPA followed by a water rinse. This measure ensures uniform etching especially for very small resist openings.

3.2.4 Membrane Fabrication Procedure

Size of Membrane

Mackie had shown previously that, due to the properties of the 1:8:1 etch, the size of the final membrane is determined by the shape and the size of the etch windows and the wafer thickness (3.1). It was decided to make membranes with edges of between 100 and 200 μm i.e. same size as the ones fabricated by Mackie. These can be formed by etching through 20 X 200 μm windows on 100 μm thick wafer with the length of the windows aligned parallel to the [011] crystal direction (3.1).

Polishing

The 2" wafers as received were about 450 μm thick. It was therefore necessary to thin down the wafers in order to produce membranes of the required size. They were diced into quarters and sent for polishing. The back surface was first polished with coarse Aloxite 800 grit until the thickness of the wafer was about 200 μm, then to 100 μm using 0.3 μm Alumina.

Crystal Orientation

The crystal orientation of a wafer was determined by observing the profiles of a cross that had been etched into the substrate with the 1:8:1 etch. The bottom of the etched grooves would appear rounded in one direction and flat in the other, corresponding to the [011] direction and the [01$\bar{1}$] direction respectively (3.1).

To carry out this test, a small piece of the material was broken off the polished wafer and its back surface masked with wax. Using the tip of a pair of tweezers, a cross was scratched into the wax and the exposed GaAs surface etched in the 1:8:1 mixture for 5 minutes. The wax was then dissolved in trichloroethylene to enable clearer examination of the etched cross under an optical microscope.

Diced wafers and Initial Cleaning

The polished material was diced into 6 X 7.5 mm wafers with the long edge of the wafers aligned parallel to the [011] crystal direction. This allowed identification of the crystal orientation at later process stages. Residual wax on the wafers from the polishing step

was removed in trichloroethylene followed by a rinse in acetone and then in IPA.

A polyimide layer was spun on the front (membrane) surface of the wafers and baked at 180° C for at least one hour. The polyimide layer served only as a mechanical mask against dirt particles and scratches and was not intended as protection against wet chemical etches. It was, however, insoluble in acetone, trichloroethylene and IPA which were used extensively in the process for cleaning the wafers.

Evaporation of NiCr/Au Mask

The etch mask evaporated on the back surface of the wafers consisted of a 50 nm layer of Au on a 10 nm layer of NiCr. The metallisation step was preceded by a 30s surface oxide etch in 1:1 $HCl:H_2O$ which improved adhesion of the NiCr/Au mask on the wafers. The mask was adequate against all the etches used in the etching steps (3.1). After the metallisation, a 1 μm thick PMMA layer was spun on the NiCr/Au surface and baked overnight at 180°C.

Etch Windows Patterning

20 X 200 μm windows were written into the resist with a 0.25 μm electron spot at 50 kV. Two such windows were patterned in each exposure frame of 1.5 x 1.2 mm. The length of the windows were aligned to the (011) crystal direction (i.e. parallel to the length of the chip). There were 5 by 4 exposure positions on each 7.5 by 6 mm wafer. Exposed resist was developed in 1:1 MIBK:IPA for 60s.

Windows were opened into the GaAs substrate by etching the

exposed NiCr/Au in I_2/KI solution (consisting of 4g/1g I_2/KI in 40ml of H_2O (3.5)) using the developed resist as the mask. But this etch also attacks GaAs and so it was necessary to protect the front surface of the wafers.

Each wafer was therefore waxed onto a glass cover slip after development. Care was taken to ensure that the entire front surface was covered with wax (Figure 3.3). This not only served to mask the surface during the subsequent etching in the NiCr/Au etch and then in the 1:8:1 etch but was also useful for handling the wafer. The etch time in the NiCr/Au etch was 2 minutes.

Etching Procedure

Fast Non Selective Etch

The GaAs substrate was first etched through the windows in the 1:8:1 mixture. The etching was stopped after 5 minutes by rinsing the wafer in deionised water. The undercutting action of the anisotropic etch formed an area of overhanging NiCr/Au/PMMA in the periphery of the etch windows. It was necessary to remove this to ensure that the etch was not prevented from diffusing into the etch well by trapped air bubbles during subsequent etching. To do this, the wafer was placed in IPA in an ultrasonic bath for 10s. Removal of the overhanging layer also enabled the bottom of the well to be viewed easily.

An optical microscope with calibrated vertical movement was used (as a vertical travelling microscope) to measure the depth of the etch wells. The depth after 5 minutes etching in the 1:8:1 mixture was typically about 50 μm.

A further 3 minutes etch in the 1:8:1 solution was carried out

and the overhanging part of the mask removed afterwards as before. The etch well was usually about 70 μm deep at this stage. From this point onwards the sample was etched at one minute intervals. In between, the etched depth was monitored using the optical microscope. The etching was stopped when the bottom of the well was within 10 μm of the top surface.

Selective Etching of GaAs/GaAlAs Etch Stop Layers

The wafers were removed from the cover slips by melting the wax on a hot plate. Each wafer was then diced into twenty 1.5 X 1.5 mm samples, each containing 2 etched wells. Usually, twelve of the samples were then waxed onto a plastic strip, again making sure that the front surface of each sample was completely masked with wax.

The remaining GaAs to the first hetero– interface was removed in the 95:5 etch. The samples were immersed in the etch for no more than two minutes at a time. This was because prolonged etching in the solution caused the etch wells to be clotted up with brown precipitate which can be removed in HCl. At the end of each etch period, the wells were cleared by rinsing the samples in 1:1 HCl:H_2O for 15s. The first hetero– interface was normally reached after about 4 to 8 minutes etching. Under an optical microscope, the GaAlAs surface appears white and mirror– like.

The 1 μm thick GaAlAs layer was removed by etching in 20% HF for 2 minutes. Next, a 20s etch in the 95:5 solution to remove the last GaAs etch stop layer was carried out. This was followed by a 10s rinse in 1:1 HCl:H_2O to clear the well of the brown precipitate. At this point the bottom of the well normally appears light green in colour. Finally, the last GaAlAs etch stop layer was removed by

etching in 20% HF for 15s. The 50 nm thick membranes should be reddish orange in colour.

Detach Membranes from Plastic Strip

The samples containing the membranes were detached from the plastic strip by dissolving the wax in trichloroethylene. This was done by floating the plastic strip on the solvent so that the samples were caused to slide off the strip eventually. Most of the breakages occurred at this stage due to the stress induced on the membranes by the detachment process. The yield of intact membranes was improved by accelerating the detachment process by heating the solvent. Previously, room temperature trichloroethylene had been used and the detachment process took about 5 minutes giving a yield of about 50% of intact membranes. The detachment was almost instantaneous in boiling trichloroethylene and the resultant yield was better than 90%.

The polyimide layer on the membrane surface of the samples was removed in acetophenone. Finally, the samples were cleaned individually by rinsing in acetone and then IPA.

3.2.5 MBE vs MOVPE

Two out of three wafers grown by MOVPE were found to be unsuitable for making membranes. The etch stop layers of the "bad" wafers were found to be ineffectual due to the lack of GaAs/GaAlAs etch selectivity at the interfaces. This was attributed to fuzzy GaAs/GaAlAs interfaces.

Hyper– abrupt interfaces are more readily obtainable by MBE growth (3.6). Two wafers, nominally identical to the MOVPE wafers,

were grown by MBE in this department. Both gave excellent etch selectivity.

MBE material was used for all experiments on membranes and for fabricating membrane devices in this work.

3.3 Electron Beam Lithography

Electron beam processing was carried out on 50 nm thick GaAs membranes with the following aims. Firstly, to see if the processing was destructive to the membranes; secondly, to determine the resolution limits of electron beam writing on the membranes and finally, to demonstrate high resolution re– alignment.

For ease of handling, the 1.5 X 1.5 mm chip containing two membranes was mounted on a specially designed holder shown in Figure 3.4. The chip was fitted in the recess and glued on with polyimide (10% in 35:65 xylene:acetophenone). The recessed structure prevented the resist from thickening near the corners during spinning so that a uniform resist layer was obtained. The transmission hole facilitated STEM and TEM microscopy.

3.3.1. Resolution Tests

Isolated Lines

A high resolution bilayer resist system comprised of 40 nm of 350,000 molecular weight PMMA on 40 nm of 185,000 molecular weight PMMA was spin coated on the GaAs membranes and baked overnight at 180^{o}C. Isolated single pixel lines were scanned in a 25 X 19 μm frame with a 8 nm electron spot accelerated to 50 kV. The

exposed resist was developed in 1:3 MIBK:IPA for 20s followed by a 30s rinse in IPA. The sample was then coated with 10 nm of AuPd. Liftoff by shooting chlorobenzene on the sample in methanol (3.7) was found to be unsuitable as the process caused the membranes to break. Instead, liftoff was performed as follows. The sample was first soaked in acetone for at least half an hour. The metallisation was then caused to liftoff by gently squirting a jet of acetone on the sample from a squeezy bottle.

For comparisons, a similar experiment was carried out on 60 nm thick Si_3N_4 membranes. The results are plotted in the graph in Figure 3.5. On GaAs membranes, the critical dose was lower and the lines were wider for a given exposure dose. The minimum linewidths achieved were 10 nm on nitride membrane and 17 nm on GaAs membrane.

Closely Spaced Lines

Using the above bilayer resist system (40 nm: 40 nm 185,000 MW: 350,000 MW PMMAs), Mackie had demonstrated that the smallest grating that could be fabricated on a 60 nm thick nitride membrane and on a 50 nm thick GaAs membrane had a centre–to–centre spacing of 40 nm and 70 nm respectively (3.1).

The aim here was to make device quality gratings on GaAs membranes which satisfied the following conditions. First, the fabrication of the gratings must be reliable and reproducible. Second, the lines of the gratings must be unbroken.

The thickness of the metallisation intended for device application was at least 60 nm. A bilayer resist consisting of 20 nm of 350,000 MW PMMA on 100 nm of 185,000 MW PMMA was used for the

resolution tests. This was more than adequate to allow liftoff of a 60 nm thick metal layer.

The pattern shown in Figure 3.6 was exposed in a 25 X 19 μm frame. A 50 kV electron beam with 8 nm spot size was used. After exposure, the samples were developed in 1:3 MIBK:IPA for 30s and then rinsed in IPA for another 30s. The metallisation consisted of 10 nm of AuPd and liftoff was performed in acetone.

The pitch of the smallest grating was 70 nm. But the minimum pitch of the gratings which were reproducible and which satisfied the requirements for device purposes was 100 nm.

Very High Resolution Alignment

Two sets of gratings were interdigitated on 50 nm thick GaAs membrane using the very high resolution alignment technique described in Chapter 2. A bilayer resist consisting of 20 nm:100 nm of 350,000 MW: 185,000 MW PMMAs was used. The alignment was performed in a 25 X 19 μm frame and the resist was developed in 1:3 MIBK:IPA for 30s after exposure. The alignment procedure was as described in Chapter 2 (Section 2.3.2). A STEM micrograph of a 50 nm pitch interdigital grating is shown in Figure 3.7. The pitch of the finest interdigital grating achieved was 35 nm.

Comments on the Resolution Tests

The above experiments show that the resolution of electron beam writing on 50 nm thick GaAs membrane is poorer than on 60 nm thick Si_3N_4 membrane. This may be due to more pronounced backscattering effects in the GaAs membrane as GaAs is a denser

material than silicon nitride.

The smallest gratings that can be fabricated reliably and with good reproducibility on the GaAs membrane is limited to about 100 nm. Gratings with smaller pitch, down to 70 nm, can be fabricated but at the expense of the quality of the gratings (more breaks in the lines) and the reliability and reproducibility of the process. Therefore, the best way to make device quality gratings with pitch smaller than 100 nm on the semiconductor membrane is by interdigitating two sets of gratings with a wider pitch.

3.4 The Fabrication of FET devices on GaAs Membranes

The target membrane FET devices were MESFETs and Lateral Surface Superlattices (LSSLs). The proposed structures of the devices are shown in Figure 3.8. The LSSL is similar to the membrane MESFET in structure but with a Schottky metal grating in place of the gate. The process requirements for both devices are common apart from the patterning of the gate level.

3.4.1 Requirements for Membrane Device Fabrication

3.4.1.1 Lithography

It was observed that the number of lithographic levels that could be performed on GaAs membranes was limited to 2 or 3 before the membranes started to break, usually during liftoff. To take account of this, the process for fabricating devices on GaAs membranes should involve minimal lithographic processing on the membranes.

3.4.1.2 Isolation

Conventional isolation technique by mesa isolation is clearly not suited to making membrane devices. A planar isolation method is required.

The bombardment of epitaxial GaAs with energetic ions causes formation of deep traps and renders it semi–insulating. Active channels can thus be defined using a suitable masking system to protect against the implant. Isolation by ion implantation became practicable when a MOP masks fabrication technique was developed in this Department (3.8). As the surface of the GaAs epilayer remains flat, this isolation technique is suitable for membrane devices.

Electrical isolation of all the GaAs FET devices fabricated was achieved by boron isolation. The standard process consisted of implantation of boron ions with dosages of 2×10^{13} cm^{-3} at 40 and 80 kV. The effect of the implantation on the crystalline structure of GaAs had been studied in this Department by McMeekin (3.9). This was done by comparing TEM electron diffraction patterns of two 50 nm thick GaAs membranes, one was implanted with the standard dose of boron ions while the other was protected against the implantation (the implantation is more than sufficient to passivate 50 nm thick layer of epitaxial GaAs). The results indicated that the crystalline structure of the implanted membrane was strained. Thus, deep traps caused by ion implantation which render active GaAs semi–insulating may be linked to strain of the GaAs crystal structure.

3.4.1.3 Ohmic Contacts

Alloyed $Au_{0.88}Ge_{0.12}$/Ni contacts (3.10–11) were used to make ohmic connections on the GaAs membranes. The contacts are Schottky–type as deposited and have to be annealed at a temperature commonly between 300°C and 400°C.

The approach to contact fabrication on membranes was as follows. First, the process for patterning ohmic contacts was demonstrated. Next, experiments on the alloying of the contacts to GaAs membranes were performed.

Ohmic Contact Patterning on GaAs membranes

Interproximity effects are less severe on thin substrates due to the reduced effect of backscattering. To exploit this, the drain and the source of the membrane MESFET were intended to be patterned on the membrane in order to obtain very narrow separation between the contacts.

The first ohmic level containing the probing pads and connecting tracks were patterned on the solid substrate before forming the membranes. The method is shown schematically in Figure 3.9. A fuller account of this will be given in the next chapter. Next, a 1 μm thick PMMA layer was coated on the 1.5 X 1.5 mm sample and baked at 180°C for 2 hours. The pattern containing a pair of closely spaced drain–source pads was exposed individually between the end of two connecting tracks on the membrane in a 25 X 19 μm frame. A 50 kV electron beam with 16 nm spot size was used. After developing in 1:1 MIBK:IPA for 60s, ohmic metallisation consisting of 100 nm $Au_{0.88}Ge_{0.12}$, 15 nm of Ni and 50 nm of Au capping layer was

evaporated. Liftoff was performed in acetone as in the case for the high resolution processing.

Micrographs of the metallisation on the membrane are shown in Figure 3.10. It can be seen that the edges of the drain and the source contacts are sharp and well defined. This was obtain without having to optimise the exposure conditions (i.e. no proximity correction). The smallest drain source gap achieved was 0.2 μm.

Alloying

The ohmic contacts were alloyed at 350^{o}C for 60s in a reducing atmosphere of 5:95 hydrogen:argon. The process was found to disintegrate all the membranes and was attributed to the stress induced on the membranes by the contacts during the alloying.

To avoid this problem, the ohmic contact was alloyed on the solid substrate before forming the membranes. But the process was found to cause the GaAs/GaAlAs etch selectivity required for forming membranes to be lost. This was attributed to the diffusion of the contact metallisation materials into the underlying GaAlAs layer during the annealing. Membranes must therefore be formed before alloying of the ohmic metallisation was carried out.

It was found that the damage to the membranes during the alloying process could be reduced by lowering the anneal temperature. By varying the thickness of the Ni layer in the composition of the ohmic contacts (3.12), it was possible to optimise contact resistance using a structure consisting of 100nm/20nm/50nm of $Au_{0.88}Ge_{0.12}$/Ni/Au when annealed at a temperature between 250 and 275^{o}C. This can be deduced from Figure 3.11 in which the resistance between two ohmic contacts consisting of this composition is plotted

against the annealing temperature. This experiment was conducted on the solid heterostructure rather than the GaAs membranes because of the difficulty in making ohmic contacts to the membranes. Yield could be further improved by filling the etch wells with polyimide to give additional support to the membranes during annealing. The polyimide layer also acted as a heat sink giving better heat distribution across the membrane. Using low annealing temperatures and strengthening with polyimide, the damage was reduced to a hair line fracture (Figure 3.12) on each membrane, damaging, on average, one in four possible devices on each membrane.

The fracture incurred during the alloying weakened the membrane so much that further processing on the membrane was impossible. This meant that the annealing must be carried out last in the fabrication of an actual device.

3.4.1.4 Schottky Contacts

High temperature treatment of a Schottky contact results in the lowering of the barrier height and reverse breakdown field and increases the ideality factor (3.13−16). The choice of gate metallisation for the membrane device must therefore be one that forms a thermally stable Schottky junction with n− GaAs.

Tests carried out by other workers have shown that Ti/n− GaAs Schottky contact is stable up to 500°C (3.15). Ti is therefore a suitable choice for the gate metallisation as the Schottky junction formed is stable over the temperature at which the alloying of the ohmic metallisation would be performed. Although there are alternatives other than Ti such as the combination of metals used in SAINTs (3.16), Ti is preferred because it is available and relatively

easy to handle.

3.4.2 Membrane FET Fabrication Strategy

Based on the above work, the strategy for fabricating GaAs FET devices on membranes was devised:

a) Thin down wafer with GaAs/GaAlAs etch stop layers – this enables membranes of the required size to be produced

b) Perform all processes requiring low resolution on solid substrate – to minimise handling of the membranes (see Section 3.4.1.2)

c) Fabricate membranes

d) Perform high resolution patterning on membranes – for MESFETs, this would include the ohmic drain–source contacts and then the Ti gate. For LSSLs, Ti grating is patterned at this point, followed by, if desired, interdigitation.

e) Anneal ohmic contacts

f) test devices

3.5 Discussions and Conclusions

It was demonstrated that the requirements for fabricating FET devices on 50 nm thick GaAs membranes can be fulfilled. Hence the fabrication of FET devices on the membranes is practicable.

Both high resolution and coarse electron beam patterning on the membranes have been demonstrated. It was shown that the smallest grating which was suitable for device application was 100 nm. Although such a resolution can be achieved on solid GaAs (with 50 kV electron beam), on membranes gratings with narrower lines can be

fabricated and with better reliability. Further, if a smaller pitch grating is desired, it has been shown that this can be made by interdigitating two sets of gratings using the very high resolution alignment technique. The pitch of the smallest interdigital grating fabricated on GaAs membranes was 35 nm. Re-alignment at this resolution is difficult if not impossible on solid GaAs. On membranes, it was also shown that structures with thick metallisation can be spaced closely apart without the need for proximity correction. The smallest drain-source gap defined on the membrane was 0.2 μm. The resolution capabilities demonstrate the potential of making ultrasmall devices on the GaAs membranes.

Abrupt interfaces are required for the heterostructure used for making membranes to ensure that the etch stop layers are effective. The growth of the heterostructure by MBE is preferred to that by MOVPE as the former growth method allows abrupt interfaces to be obtained more readily. It was also discovered that that interdiffusion between the ohmic metallisation materials and the GaAs/GaAlAs layers alters their chemical properties so that the GaAs/GaAlAs etch selectivity for the system of the selective etches used is destroyed.

Chapter 3 References

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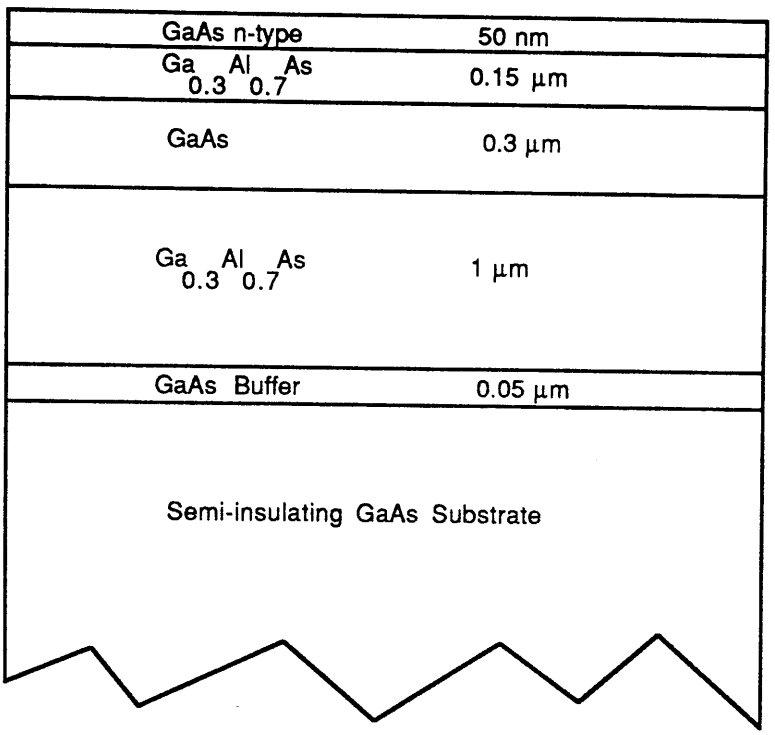


Figure 3.1 Heterostructure used for Fabrication of GaAs membranes.

Layers were grown by MBE on a semi-insulating GaAs substrate.

Top GaAs Layer $N_D = 3E+18\ cm^{-3}$

The other layers were nominally undoped

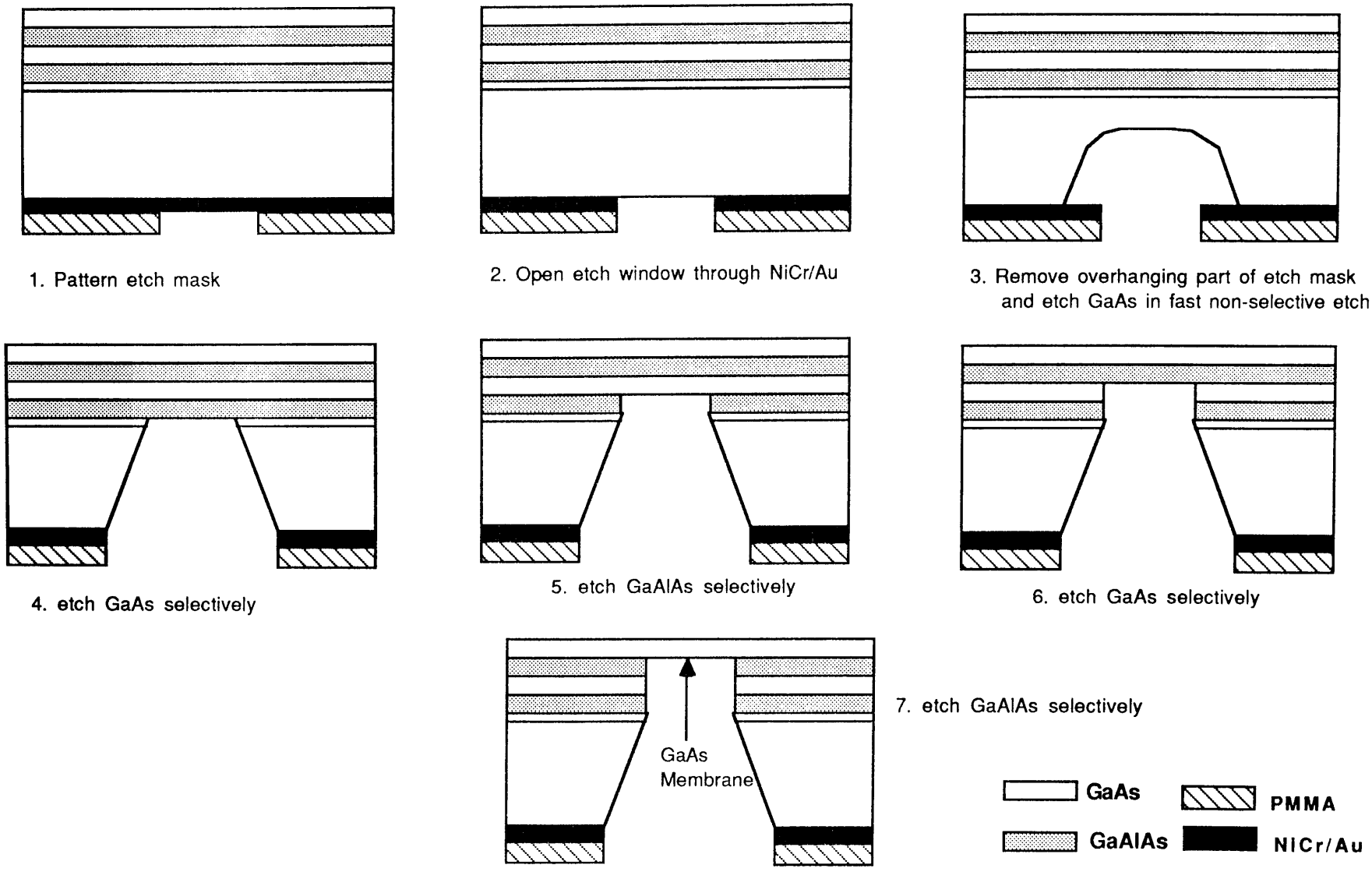


Figure 3.2 Fabrication of GaAs Membrane

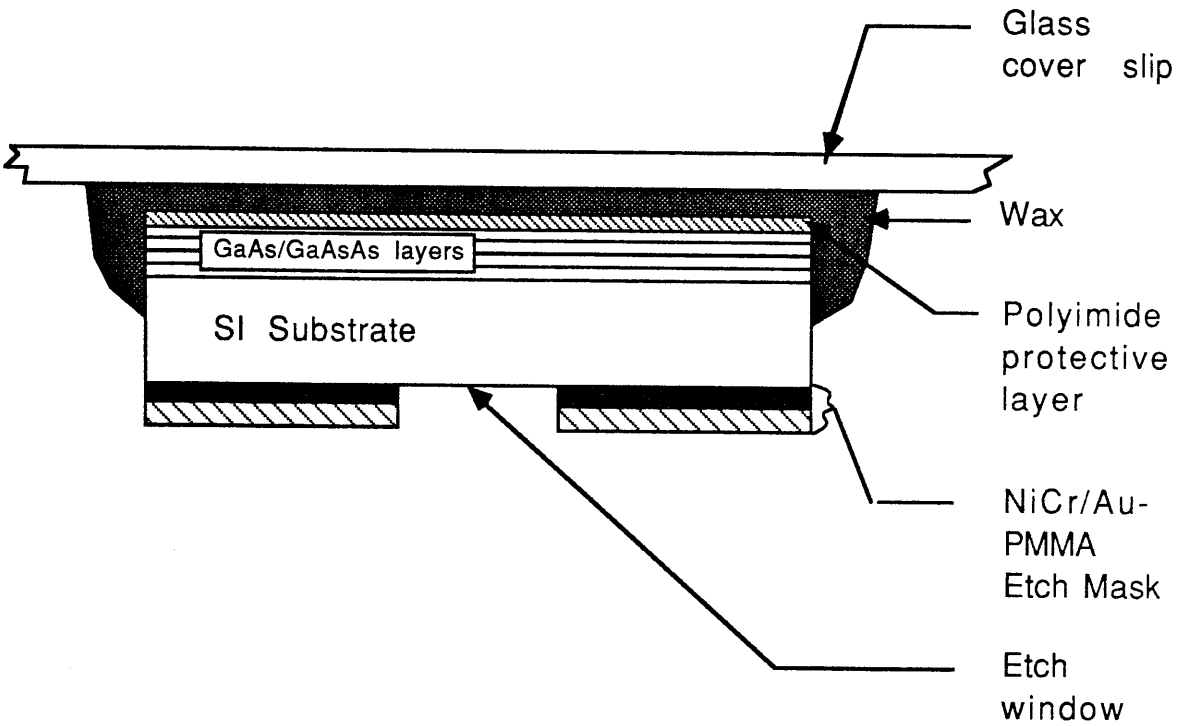


Figure 3.3

The membrane chip is waxed onto a glass cover slip to mask the hetero-layers from the etches used to form membranes.

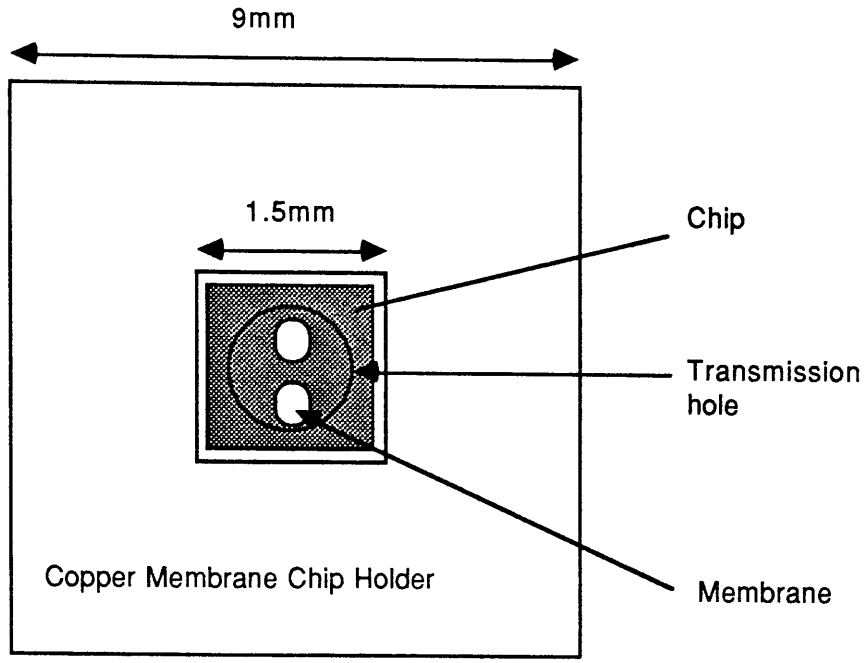


Figure 3.4 Special Copper Holder

The diagrams illustrate the design of the holder and the way a membrane chip is mounted. The holder consists of a 1 µm hole which facilitates transmission microscopy. The recessed structure allows a uniform layer of resist to be spin coated on the chip.

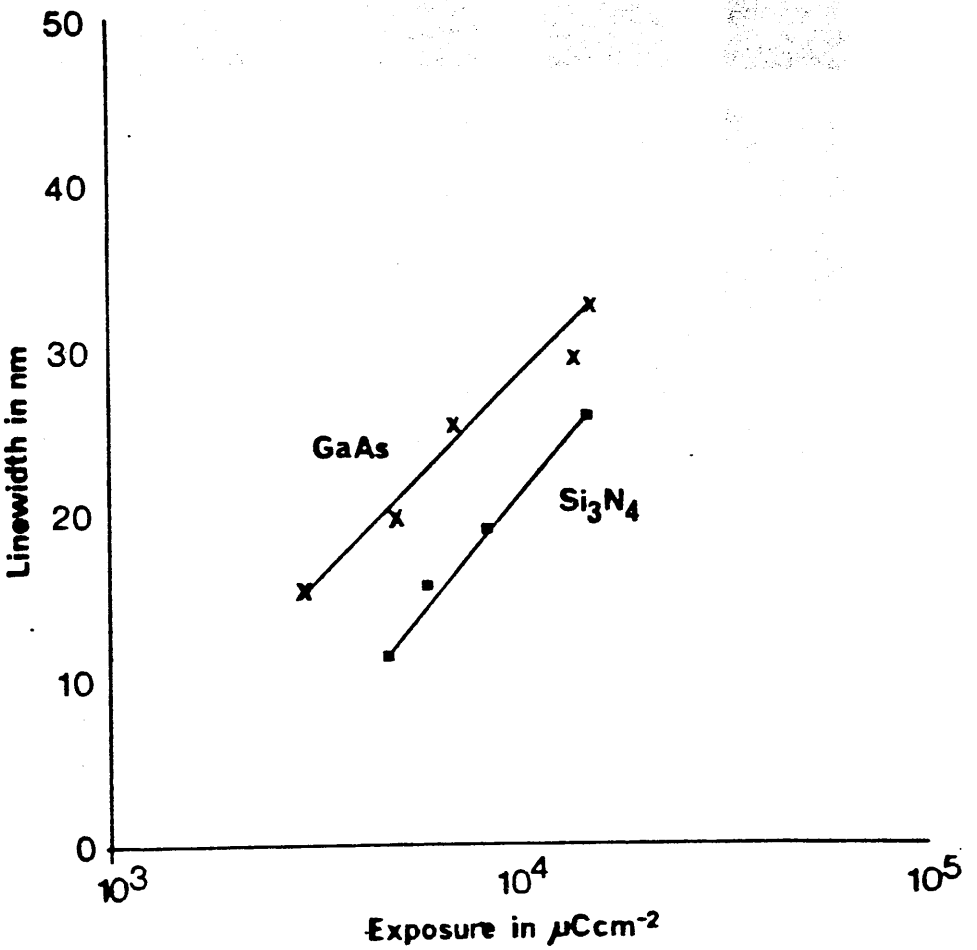


Figure 3.5

Linewidth versus Exposure Dose Plot from Resolution tests on 50 nm thick GaAs and 60 nm thick Si_3Ni_4 membranes. Isolated single lines were written on a 2-layer resist system (40nm:40nm 350,000MW:185,000MW PMMAs) with 8nm diameter electron beam accelerated to 50kV in 25X19μm frame. 10nm thick AuPd was deposited and liftoff process used.

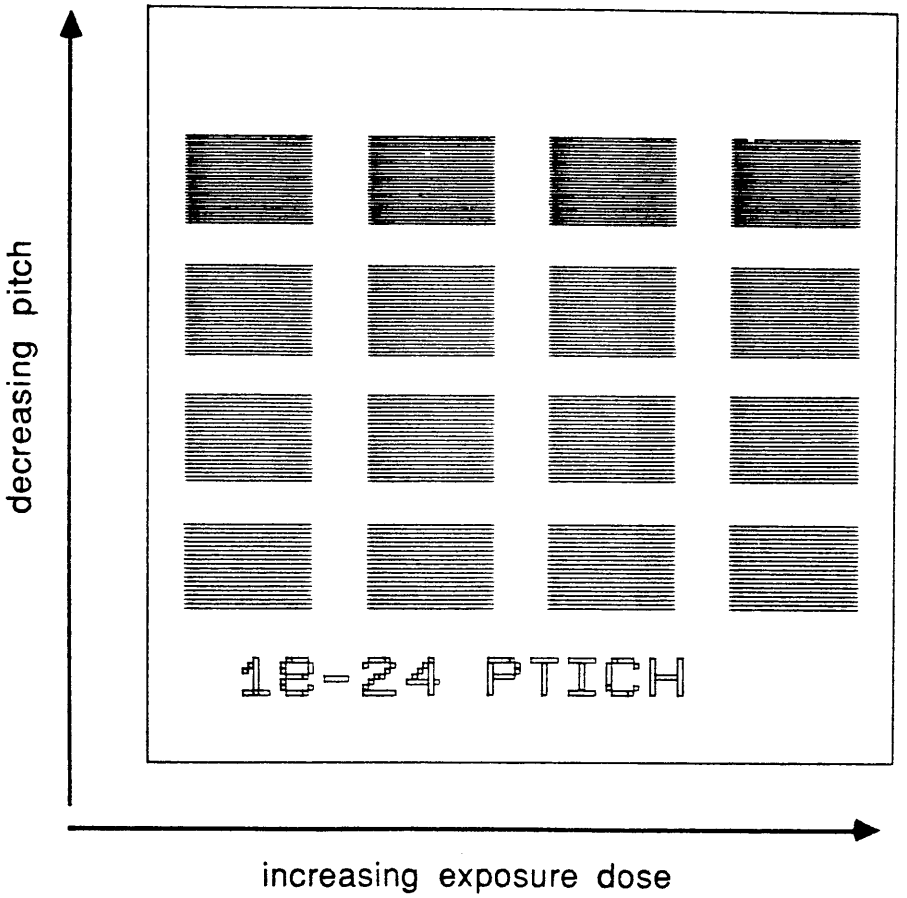


Figure 3.6 Grating Test Pattern

The exposure dose and pitch are varied along rows and columns respectively.

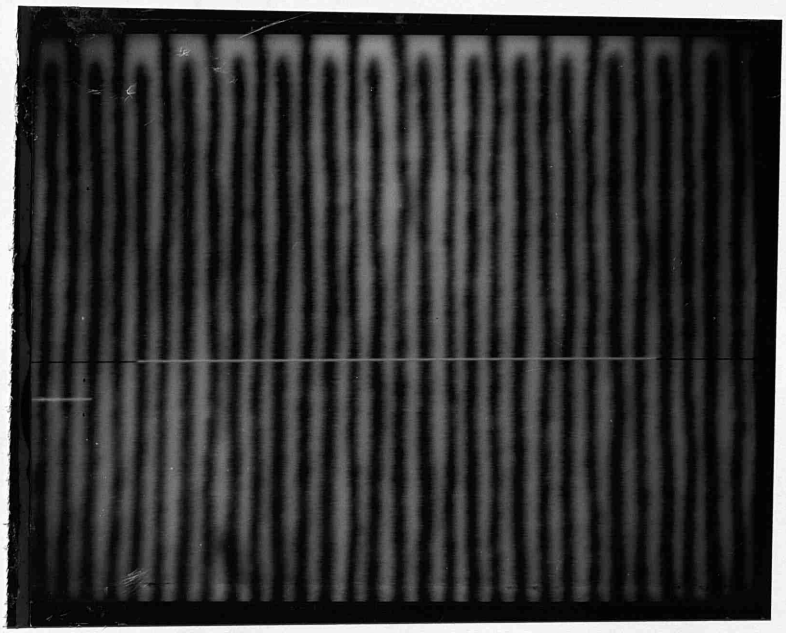


Figure 3.7

STEM micrograph of a interdigital grating with 50nm centre-to-centre spacing patterned on a 50nm thick GaAs membrane using two aligned lithographic steps. The light segment of the marker denotes 1μm.

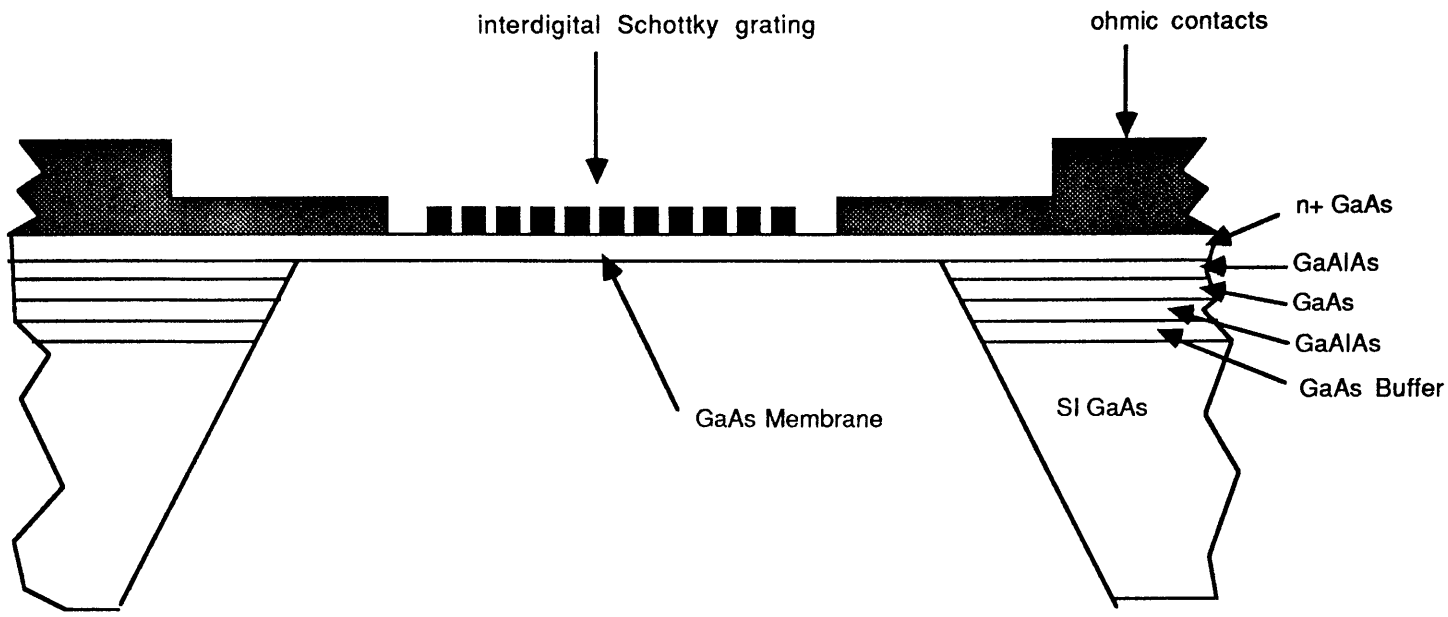
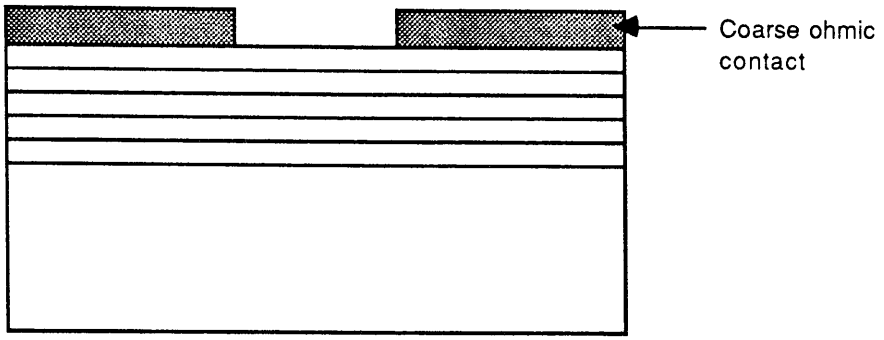
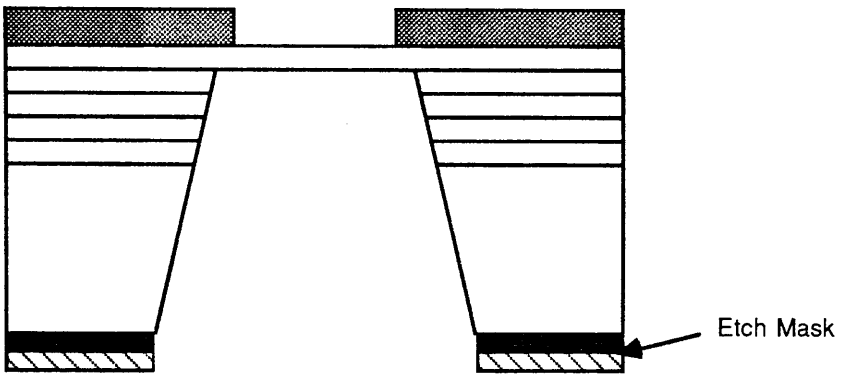


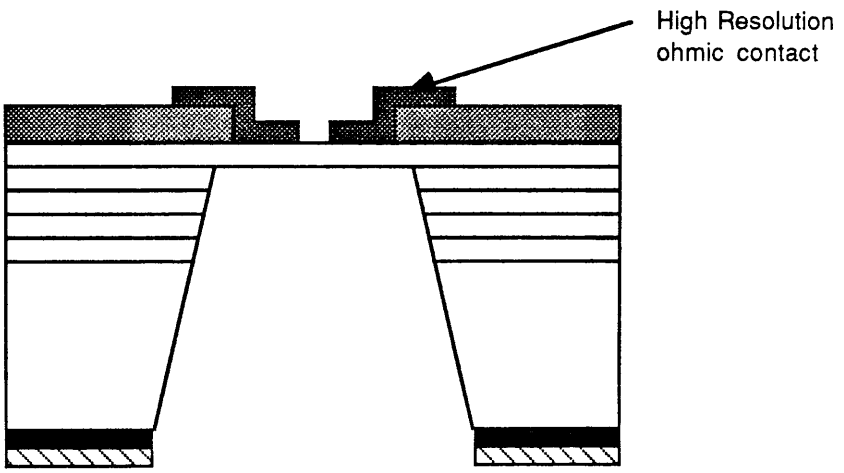
Figure 3.8 Proposed Lateral Superlattice Structure



1. Pattern low resolution ohmic contacts on solid heterostructure



2. Form Membrane



3. Pattern high resolution ohmic contacts on membrane

Figure 3.9

Diagrams showing the fabrication of closely spaced ohmic contacts on 50nm thick GaAs membrane.

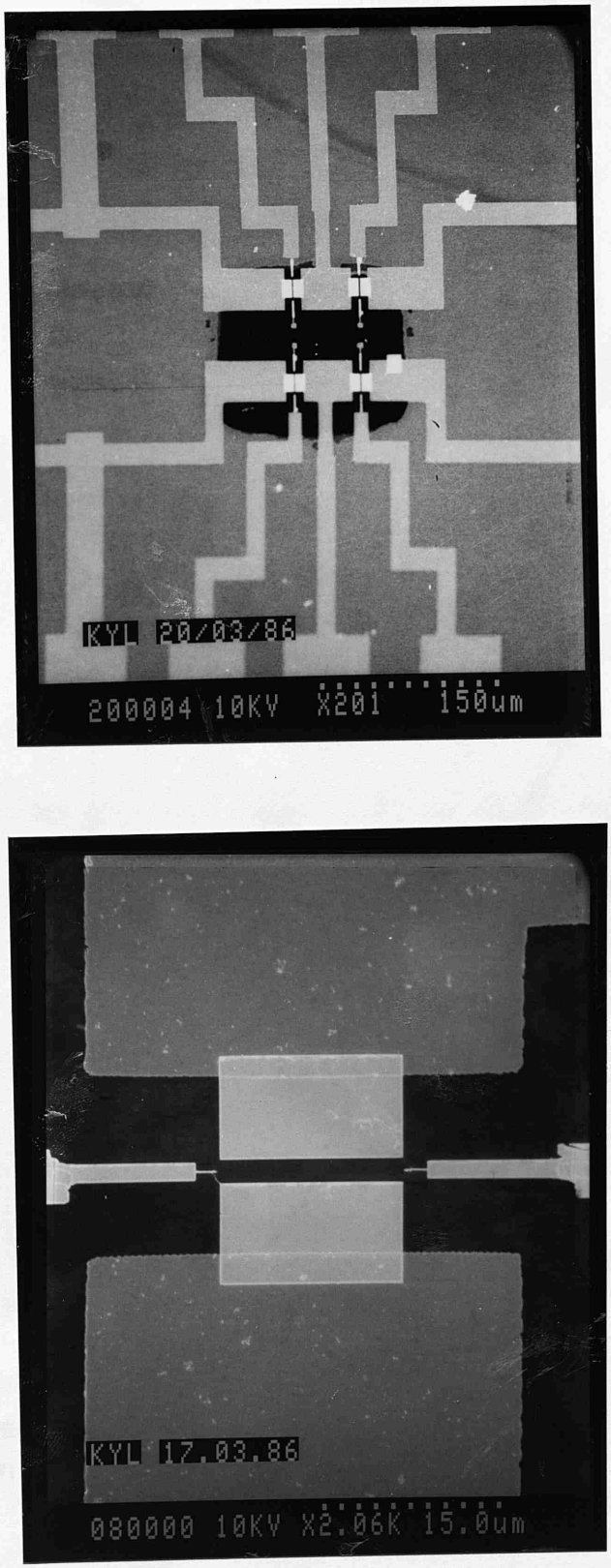


Figure 3.10

SEM micrographs of ungated MESFETs with closely spaced drain-source ohmic contacts patterned on 50nm thick GaAs membranes (dark areas)

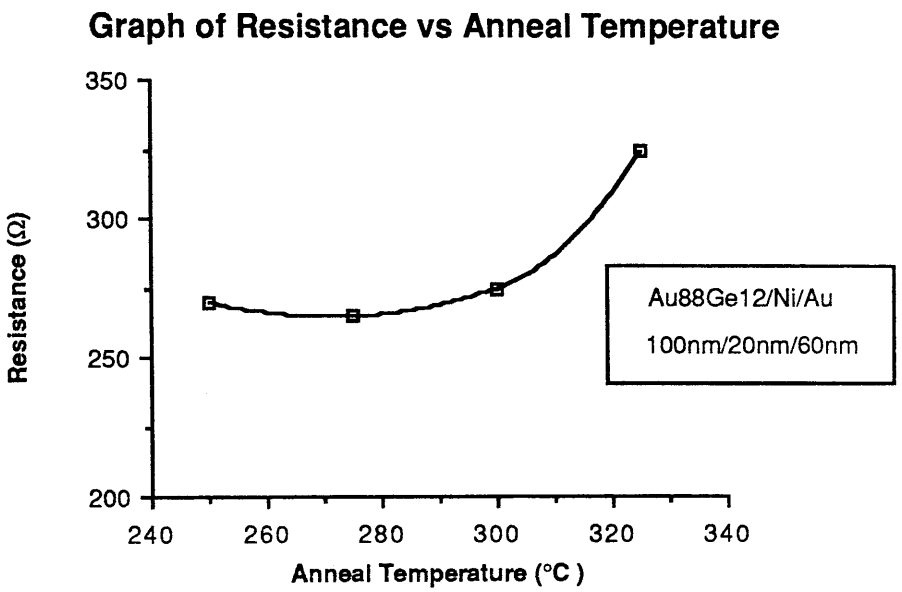


Figure 3.11

Graph showing the resistance between two ohmic contacts with 1μm separation on the heterostucture at different anneal temperatures. The channel width was 5μm.

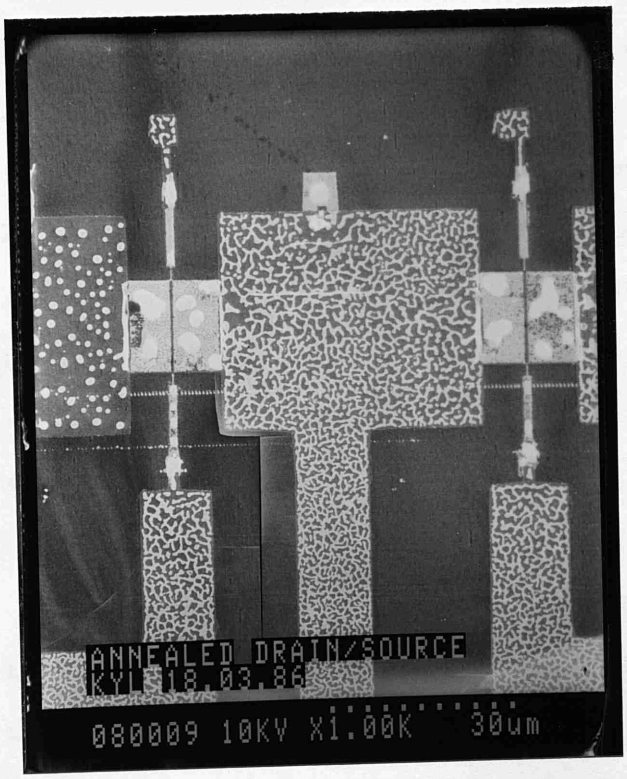


Figure 3.12

SEM micrograph showing hairline fracture on membrane caused by annealing of ohmic contacts.

Chapter 4 The Fabrication of MESFETs and LSSLs on Thin Active GaAs Membranes

4.1 Introduction

In this chapter, the process steps required for fabricating MESFETs (MEtal–Semiconductor Field Effect Transistors) and LSSLs (Lateral Surface SuperLattices) on 50 nm thick active GaAs ($n^+ = 3 \times 10^{18}$ cm^{-3}) membranes are described.

The fabrication process for making membrane MESFETs and LSSLs was based on the strategy developed in Chapter 3. An alternative method for fabricating membrane MESFETs has also been developed.

4.1.1 Membrane MESFETs

Apart from the absence of a substrate, the structure of the membrane MESFET is similar to that on solid GaAs. A description of the device and the basis of its operation can be found in Chapter 6.

There are two reasons for making MESFETs on the thin substrates. Firstly, as was shown in chapter 3, the use of the membranes facilitates very high resolution electron beam lithography. The fabrication of 15 nm linewidths and ohmic drain–source contacts with separation as small as 0.2 μm had been demonstrated on GaAs membranes. Secondly, membrane MESFETs can be compared with conventional devices on solid substrate to study the effect of the substrate on device operation.

4.1.2 LSSL

The basic idea of a superlattice, as first put forward by Esaki and Tsu (4.1), is to superimpose a one dimensional man made periodic potential on the atomic periodicity of the crystal structure. This additional periodicity splits the energy spectrum of the original crystal and produces minibands and minigaps which alter the physical properties of the original crystal (4.2).

The idea of a lateral superlattice was first put forward by Kastal'skii and Khusainov in 1970 (4.3), but the concept of an electrically controllable lateral surface superlattice (LSSL) was first proposed by Bate in 1977 (4.4). In order to form an LSSL, one must a) form a two–dimensional electron gas (2DEG) (the carriers can also be holes) , and b) impose on it a periodic modulation in one or two dimensions (4.4– 4.8).

A 2–DEG refers to an ensemble of electrons which are confined to a thin layer such that the number of degrees of spatial freedom of an electron is reduced from three to two. The criterion for observing superlattice effect is that the period of the external modulation has to be comparable to or less than the scattering length λ of an electron. Earlier analysis had assumed λ to be the shortest scattering length i.e. the elastic scattering length (4.2). But recent work by Warren et. al. (4.5) indicates that λ is associated with the longer inelastic scattering length.

The proposed structure of the LSSL is shown in Figure 3.8. The device is similar to the membrane MESFET but with a grating in place of the gate. This induces a periodic Schottky potential which can be controlled externally. The inelastic scattering length of an electron in n–GaAs doped to 3×10^{18} cm^{-3} had been measured by

Whittington et. al. (4.9) to be 0.3 μm at 5^{o}K. Using membranes, the lithographic requirement is not only more than satisfied, but the membrane structure can also provide confinement of electrons required for observing LSSL effects, as shown in Figure 4.1. An investigation into the nature of the 2– DEG in the GaAs membranes was carried out in parallel with this work and is covered in Chapter 5.

4.2 Fabrication of membrane FET devices

The fabrication method based on the strategy developed in Chapter 3 is described in this section. The starting material was the heterostructure used for making GaAs membranes (Figure 3.1).

4.2.1 Device Design and Fabrication Outline

The design and the structure of the membrane FET devices are shown in Figure 4.2. The basic membrane device consists of two ohmic contacts (the drain and the source) and a Schottky gate in the case of a MESFET, or, for a LSSL, a Schottky grating. The devices are patterned on a 1.5 X 1.5 mm chip which contains two membranes. There are four devices on each membrane which are connected to probing pads patterned on solid substrate of the chip via ohmic connecting tracks. For comparison, two control devices are located on solid GaAs on the same chip.

All process steps requiring low resolution lithography are performed on the solid heterostructure before forming membranes. Only high resolution patterning is carried out on the membranes. As these are produced by etching from the back surface of the heterostructure, a back surface to front surface alignment technique is

necessary so that the membranes are formed at the active areas. The low resolution process levels are:

1) registration marks level

2) isolation level

3) ohmic level

The standard registration marks for low resolution alignment are patterned in level (1). These allow alignment between patterns in levels (1) to (3). The alignment and patterning at all three levels are carried out in a 1.5 X 1.2 mm frame using a 50 kV beam with 0.25 μm spot size. A 1 μm thick PMMA (185,000 MW) layer is used as the positive resist at all three levels. The resist is baked overnight at 180^{o}C if etching is involved and for at least 2 hours otherwise. Exposed PMMA is developed in 1:1 MIBK:IPA for 60s followed by a 30s rinse in IPA.

Following deposition of ohmic contacts at level 3, membranes are formed using the etching process described in Chapter 3.

The high resolution process steps are then performed on membranes and these are:

For fabricating Membrane MESFETs

1) patterning of very closely spaced drain–source contacts and

2) patterning Schottky gate

For fabricating LSSL

1) patterning of Schottky grating and

2) if required, interdigitating the above grating with a second set of grating.

The above patterns are exposed with either a 8 nm or 16 nm electron spot at 50 kV. The fine drain–source contacts in (1) are patterned on a 1 μm thick PMMA (185,000 MW baked overnight at 180^{o}C) layer which is developed in 1:1 MIBK:IPA for 60s. A bilayer

resist system comprised of 20 nm/20 nm of 350,000 MW/185,000 MW PMMAs is used for writing the Schottky patterns. It is necessary to bake the resist overnight at 180°C. Development of the resist is carried out in 1:3 MIBK:IPA for 30s followed by a 30s rinse in IPA.

Prior to a metallisation step, a sample is subjected to a 30 to 60s surface oxide etch in 1:1 $HCl:H_2SO_4$ in order to improve adhesion of the metallisation on the sample. Liftoff at all levels is performed in acetone.

Finally, the sample is annealed at 250−275°C in a reducing atmosphere of 5%:95% of H_2/Ar to alloy the ohmic contacts. Before this, the etch wells are filled with polyimide. This serves to strengthen the membranes and also ensures a more uniform heat distribution across the membranes during annealing.

The process for fabricating MESFETs and LSSLs on GaAs membranes is summarised in a flow diagram Figure 4.3. The process steps needed for making membrane MESFETs and LSSLs are the same until the membranes are formed, so the fabrication of the devices are described separately only from that point onwards.

4.2.2 Low Resolution Fabrication Process Steps

The starting material was first polished down to about 100 μm. Once its crystal orientation had been determined, the material was diced into 6 X 7.5 mm wafers.

Registration Marks Level

On each wafer, the standard registration marks pattern (Figure 4.4) was exposed at twenty (5 X 4) exposure positions calculated using

POSITION. The wafer was metallised with 10 nm of NiCr and then 50 nm of Au.

Isolation Level

The standard bilayer resist comprised of a 1 μm thick PMMA layer on a 0.3 μm thick polyimide layer for fabricating MOP masks was coated on the wafer. The exposure frame at this level was aligned to the registration marks pattern using the standard low resolution alignment procedure (described in Chapter 2). Once aligned, the MOP mask pattern shown in Figure 4.5 was exposed. The procedure was repeated at all the exposure sites on the wafer.

MOP masks were fabricated using the technique described in Chapter 2. The wafer was then implanted with boron ions with doses of $2x10^{18}cm^{-3}$ at 40 and 80 kV. Afterwards, the MOP masks were removed by dissolving the polyimide layer in boiling acetophenone.

Ohmic Level

At each exposure site, the ohmic contacts pattern shown in Figure 4.6 was first aligned to the isolation pattern and then exposed. The alignment method was as above. The metallisation consisted of 100nm:20nm:50nm of $Au_{88}Ge_{12}$:Ni:Au, which is the composition optimised for low temperature ohmic contacts formation.

Next, a 0.3 μm thick layer of polyimide was coated on the front surface of the wafer and then baked at 180^{o}C for two hours. The polyimide layer was used to protect the surface against scratches during subsequent processing.

Deposition of NiCr/Au Etch Mask on the Back Surface

The back surface of the wafer was coated with a layer of NiCr/Au (10 nm/50 nm) and on it, a 1 μm thick PMMA layer. The wafer was then baked overnight at 180^{o}C after which it was diced into ten 1.5 X 3 mm samples. On each sample, there were two sets of isolated ohmic patterns.

Back surface to front surface Alignment

Membranes were required to be formed at the active regions on the front surface of a sample. In order to do this, a simple back surface to front surface alignment technique was used.

First, the positions of the ohmic patterns on the front surface were defined by their horizontal and vertical displacements from the nearest corner of the sample. The distances were measured with an optical microscope. The alignment process in the SEM involved moving the sample by the appropriate distances from the reference corner of the sample to the exposure positions. The alignment was performed at X80 magnification (1.5 by 1.2 mm frame) with a 16 nm beam. The use of the small electron spot size ensured that the resist did not become exposed as the alignment was carried out with the beam unblanked.

A misalignment of within 20 μm was permissible due to the size of the membranes.

Membrane Formation

Two 20 X 200 μm windows were exposed in a 1.5 X 1.2 mm frame. A 50 kV electron beam with 0.25 μm spot size was use. Afterwards, six exposed samples (typically) were waxed onto a glass cover slip and then developed in 1:1 MIBK:IPA. Etch windows were opened into GaAs by etching through the NiCr/Au layer using the developed resist as the mask. The samples were etched through the windows in a fast non-selective etch (1:8:1 H_2SO_4:H_2O_2:H_2O) until the bottom of the wells was within 10 μm from the front surface. Afterwards, the samples were removed from the cover slip and then diced into 1.5 X 1.5 mm chips, each with two etch wells. These were waxed onto a plastic strip. The selective etching procedure required to form membranes was then carried out. A photograph showing the metallisation on a membrane taken from the back surface of a chip is shown in Figure 4.7.

Finally, the chips were removed from the plastic strip, cleaned and then mounted on special copper holders (described in Chapter 3).

The membrane fabrication process has been described in Chapter 3.

Preliminary Electrical Testing

Some of the above samples were annealed to alloy the ohmic contacts. A micrograph of one of the gateless MESFETs fabricated is shown in Figure 4.8. Figure 4.9 shows the I-V characteristics of nominally identical ungated MESFETs, one on a solid substrate and the other on a membrane, on the same chip. The devices had

drain–source separations of 2 μm and a channel width of 10 μm. The absence of a substrate greatly reduced heat sinking causing the membranes to melt at a current density below the saturation field at d.c. It was therefore necessary to pulse the devices to test their characteristics.

The saturation current for the membrane device is approximately 50% less than that for the solid substrate device. The reduction in the drain current of the membrane device was very likely due to the depletion layer extending from the new (bottom) membrane surface. This is supported by the following analysis.

If L is the surface depletion width, a the thickness of the membrane and, if the depletion from the front and bottom surfaces are assumed to be equal, the ratio of the saturated drain current of the membrane device to that of the solid substrate device is

$$r=(a-2L)/(a-L). \qquad (1)$$

From equation (1), the depletion width was calculated to be 17nm for $r=0.5$ and $a=50$nm (NB the saturated drain current for the membrane and solid substrate devices were defined as $nev_d(a-2L)w$ and $nev_d(a-L)w$ respectively, where n is the doping density, e the electronic charge, w the channel width and v_d the saturated electron drift velocity). This compares favourably with the theoretical value of 18nm assuming that the surface barrier potential is 0.7V (see Chapter 5, Section 5.2).

The results indicated that the electrical characteristics of the membranes were suited to active devices.

High resolution patterning on membranes of the fine drain–source contacts, the gates and the gratings were performed individually at X5000 magnification (25 X 19 μm frame). The patterns were aligned to the coarse drain–source contacts using alignment

markers contained in the ohmic contacts pattern. The alignment method is described below.

4.2.2.1 High Resolution Alignment

The alignment was performed in the STEM mode using a 50 kV electron beam with a spot size of either 8 nm or 16 nm. The specimen was moved approximately to the exposure site by aligning the centre of the drain and the source to the middle of the SEM VDU at x160 magnification (0.8 X 0.6 mm frame) with the beam unblanked. The magnification was then increased to X320 and the above positioning repeated.

Fine alignment was carried out at X5000 magnification (25 X 19 μm frame). The beam blank was turned on at this stage. The alignment pattern which contained partial outlines corresponding to the ohmic alignment markers was scanned at a rate of 2 μs per pixel. The two were made to coincide by adjusting the X– Y Varymag, the stage rotation and the beam shifters. When this was done, the patterns were deemed to be aligned.

The processes required for fabricating MESFETs and LSSLs are described separately from this point onwards.

4.2.3. Fabrication of MESFETs

4.2.3.1 High Resolution Patterning of Drain– Source Contacts

The high resolution alignment described in Section 4.2.2.1 was carried out using a 16 nm beam spot. Once aligned, the pattern consisting of two closely spaced rectangles was exposed. This procedure

was repeated at all the device sites on the membranes. The metallisation consisted of 100nm:20nm:50 nm of $Au_{0.88}Ge_{0.12}$/Ni/Au. Figure 4.10.a is a micrograph of the metallisation on a membrane.

The effect of annealing the ohmic contacts (at 250– 275 ^{o}C) is shown in Figure 4.10.b. It can be seen that a break had developed between the fine drain– source contacts and the coarse drain– source contacts. Electrical testing showed that an open circuit existed between the two sets of contacts for all samples. Since it was considered of greater priority to fabricate working devices, the high resolution patterning of the drain– source contacts on membranes was not pursued further. Instead, it was adequate to use the coarse drain– source contacts.

4.2.3.2 Gate Level

The gate level was aligned to the ohmic contacts using the high alignment resolution alignment technique described previously. The alignment and exposure of the gate pattern was carried out using a 8 nm spot at 50 kV.

4.2.3.3 Gate Metallisation

Evaporation of Ti was commenced when the pressure inside the evaporator was about 10^{-6} Torr. Due to the strong affinity of Ti to O_2, Ti was evaporated for a short period to getter any residual O_2 in the chamber. A shutter was used to shield the sample from the partly oxidised Ti. A 60 nm thick Ti layer was evaporated onto the sample and liftoff was performed in acetone.

Finally, the sample was annealed at 250–275°C to alloy the ohmic contacts. Micrographs of some of the MESFETs fabricated are shown in Figure 4.11.

4.2.4 Fabrication of LSSLs

The processing which followed the low resolution steps (Section 4.2.1) are described here. The process steps were the same as the ones carried out at the gate level of the membrane MESFETs except that a grating pattern was exposed instead of a gate.

4.2.4.1 Grating Patterning and Metallisation

The 25 X 19 μm exposure frame was aligned to the drain–source contacts using the method described in Section 4.2.2.1. A 50 kV beam with 8 nm spot size was used for the alignment and the subsequent writing of the grating pattern. Following the procedure described in Section 4.2.3.3, a 60 nm thick Ti layer was metallised onto the sample and liftoff was performed in acetone. Finally, the ohmic contacts were annealed at 250–275°C for 30s. A STEM micrograph of a LSSL fabricated is shown in Figure 4.12.

4.3 Electrical Testing

In this section, the results of d.c. measurements on the devices are presented. The results are discussed later in Section 4.5. The figures of merits quoted i.e. transconductance and output conductance are defined in Chapter 6.

4.3.1 Membrane MESFETs

The first batch of membrane MESFETs fabricated had a gate–length of between 0.1 μm to 0.5 μm, a gate width of 10 μm and a drain–source gap of 2 μm. It was necessary to pulse the devices to test their characteristics. The method used is illustrated in Figure 4.13. The I–V characteristics of a 0.5 μm gate–length membrane MESFET is shown in Figure 4.14. The transconductance of the device was estimated to be about 50 mS/mm (of the gate width).

Devices with smaller gate–length (< 0.5 μm) were also tested but no results were obtained because the gates were open circuit and did not control the drain current. The gate of a device which had been tested is shown in a SEM micrograph in Figure 4.15. It was very likely that the gate was blown by the step voltage applied to it during testing. Consequently, a ramp bias was used but to no avail.

Due to the difficulties involved in fabricating the above MESFETs and the problem associated with the testing of short gate–length devices, a novel membrane MESFETs fabrication method was developed. The process is described later in Section 4.4.

4.3.2 LSSLs

LSSLs with 100 nm pitch grating and 50 nm linewidths were made. The devices had a drain–source separation of 4 μm and a channel width of 10 μm. The total width of a grating pattern was 2.5 μm. For comparison, membrane MESFETs with 2.5 μm gate–length (i.e. the same size as the total width of the gratings), 10 μm gate width and a drain–source separation of 4 μm were also fabricated. It was possible to test these devices using a HP4245A Semiconductor

Parameter Analyser. All devices were tested at room temperature.

The I– V characteristics of the devices are shown in Figures 4.16.a– b. The transconductance of the LSSL and the MESFET were 21 mS/mm (of the channel width) and 28 mS/mm respectively.

4.4 Alternative Membrane MESFET Fabrication Method

An alternative technique for fabricating membrane MESFETs using an undercutting etch process was developed. The fabrication procedure involves etching the $Ga_{0.3}Al_{0.7}As$ etch stop layer (Figure 3.1) underlying the top active GaAs layer through windows opened into the GaAs layer. This method is illustrated in Figure 4.17.

The process steps are:

1) deposit ohmic contact pattern together with registration marks
2) fabricate MOP mask to protect drain– source channel
3) implant sample with boron ions
4) pattern etch windows on the front (membrane) surface
5) etch active GaAs and then underlying GaAlAs layer selectively to form membranes
6) alloy ohmic contacts
7) deposit gate.

The isolation pattern in step (2) and the etch window pattern in step (4) were aligned to the ohmic contacts using registration marks contained in the ohmic pattern. The alignment and exposure were performed at X160 magnification (0.8 X 0.6 mm frame size). A 1 μm thick PMMA (185,00 MW) layer was used as the positive resist throughout except for patterning the gate. Again, baking of the resist overnight at 180°C was essential if etching was involved.

The above patterns and process steps, except (4) and (5), have

been used for fabricating MESFETs on solid substrate. A detailed account of these is presented in Chapter 6. As such, only brief description of the process is given below.

4.4.1 Fabrication Procedure

The starting material was part of the MBE grown wafer used in Section 4.2.

Ohmic Contacts Level

The ohmic contacts pattern was exposed with a 50 kV beam with 0.25 μm spot size. The sample was etched in 1:1 HCl:H_2O for 60s to remove surface oxide before coating it with 100 nm/20 nm/50nm of $Au_{0.88}Ge_{0.12}$/Ni/Au.

Isolation Level

Once the exposure frame was aligned to the ohmic pattern, the MOP mask pattern was written into the bilayer resist (0.3 μm/1 μm polyimide/PMMA) used for making the masks. A 50 kV electron beam with 0.25 μm spot size was used. MOP masks were fabricated using the standard technique.

Isolation was achieved by boron implantation. The dosages were 2 X 10^{13} $\mu C/cm^2$ at 40 KeV and 80 keV. Afterwards the MOP masks were removed by dissolving the polyimide layer in boiling acetophenone.

Pattern Etch Windows

The etch windows pattern was aligned to the isolated ohmic contacts and then written into the PMMA resist layer which had been baked overnight at 180°C. A 64 nm spot at 50 kV was used. Development of the exposed resist was carried out in 1:1 MIBK:IPA for 60s.

Selective Etching

Windows were opened into the active GaAs layer by etching in 95:5 H_2O_2:NH_3 (a GaAs selective etch) for 5s using the resist layer as the mask. Membranes were then formed by etching the underlying GaAlAs through the openings in the GaAs layer in 20% HF (which etches GaAlAs selectively) for 40s.

After forming the membranes, the ohmic contacts were annealed at 250–270°C for 30s.

Gate Patterning

The gate resist used was the high resolution bilayer resist consisting of 20 nm/100 nm 350,000MW/185,000 MW PMMAs. The gate pattern was aligned and exposed individually in a 100 X 76 μm frame using a 50 kV beam with 32 nm spot.

The gate metallisation consisted of a 30 nm thick Al layer on a 30 nm thick Ti layer. Liftoff was performed in acetone.

All the membrane MESFETs fabricated had a channel width and a drain–source separation of 5 μm and 1 μm respectively. A micrograph of a membrane MESFET is shown in Figure 4.18.

This method for manufacturing membrane MESFETs offers many advantages over the old method. Firstly, the process is simpler involving fewer steps. Handling of the sample is easier (compared with the old method) as the heterostructure need not be thinned down. Gates can be patterned on the membranes after annealing the ohmic contacts. This is because the membranes are more robust due to their smaller sizes (typically 10 X 8 μm). The obvious disadvantage is that the membranes formed this way cannot be viewed using transmission electron microscopy.

4.4.2 Electrical Testing

D.C. testing of the membrane MESFETs was carried out using a HP4145A Semiconductor Parameter Analyser and an Omni–probe probing system. The I–V characteristics of identical gateless MESFETs, one on a membrane and the other on solid substrate, are shown in Figure 4.19. The saturated drain current of the membrane device was about 30% of the device on solid substrate. As will be discussed later, there are evidence which suggest that the larger drain current reduction (compared with membrane devices fabricated by etching from the back surface) may be due to combination of depletion from the bottom surface and thinning of the membrane.

The I–V characteristics of membrane MESFETs with 0.1μm, 0.3μm and 0.5μm gate–length and solid substrate MESFETs with 0.1μm and 0.5μm gate–length are shown in Figure 4.20 (gate width and drain source separation of 5 and 1 μm respectively in both cases).

The transconductance of the membrane MESFETs were between 60 to 120 mS/mm, while the values for solid substrate MESFETs were

between 100–200 mS/mm (transconductance values were measured typically from Vg= 0 to Vg= −0.1 V). Breakdown of gates occurred before pinch–off for all the solid substrate devices. Good pinchoff and saturation characteristics were obtained for the membrane MESFETs apart from the 0.1 μm gate–length device.

Summary of Results

The results of electrical testing on MESFETs is summarised in Table 4.1 below.

Membrane MESFETs

Gate Length (μm)	Gate Width (μm)	Drain/Source Gap (μm)	g_m Vg=0 (mS/mm)	g_D Vg=0 (mS/mm)	Vg at pinhoff (Volt)
0.1*	5	1	54	5	-
0.3*	5	1	112	7	-1.5
0.5*	5	1	61	-	-1.5
0.5	10	2	60	-	-1.5
2.5	10	4	30	0.5	-
3.0	10	4	26	0.4	-

* denotes membranes were formed by etching from the front surface (Section 4.4). Otherwise, membranes were formed by etching from the back surface.

Solid Substrate MESFETs

Gate Length (μm)	Gate Width (μm)	Drain/Source Gap (μm)	g_m Vg=0 (mS/mm)	g_D Vg=0 (mS/mm)	Vg at pinchoff (Volt)
0.1	5	1	100	5	Gate Breakdown
0.5	"	1	180	4	"

Table 4.1

4.5 Discussions

4.5.1 Device Operation and Interface Quality

The membrane devices fabricated by etching from the back surface failed to pinchoff completely. Their transconductances became progressively smaller as gate bias approached pinch-off. This transconductance compression phenomenom was also observed in solid substrate MESFETs fabricated on the same material (Figure 4.20b). Kopp et. al. (4.10) observed this phenomenom in MESFETs fabricated on similar MBE grown heterostructure grown and attributed this to interface quality (active GaAs/undoped GaAlAs interface) effects.

Details on the growth of the heterostructure used in this work are contained in the thesis by Frost (4.11). However, the growth of the last two layers which were critical to the device operation, namely the undoped $Ga_{1-x}Al_xAs$ layer underlying the active GaAs layer, is worth noting. The diffraction pattern obtained by in situ reflection high energy diffraction (RHEED) gives information on the surface structure and morphology during growth (4.12). A smooth surface is indicated by a well defined RHEED pattern (i.e. large oscillation in the intensity of the specular reflected electron beam with a slowly decaying amplitude envelope). The growth of the GaAlAs layer was characterised by such a RHEED pattern, with slight loss of clarity through the layer. On recommencing GaAs growth, the surface smoothness rapidly improved to give a sharper and brighter RHEED pattern. These results show that the n-GaAs/GaAlAs interface was rough. It is known that, during the growth of GaAs on GaAlAs, impurity buildup occurs at the interface (4.13-17). The combined effects of surface roughness and interface impurities result in

degradation of carrier mobility in the GaAs layer near the interface (4.17−8). For the membrane material, a low carrier mobility region is believed to extend from the GaAs/GaAlAs interface into the active GaAs layer. The transconductance compression is attributed to the effect of this layer. This explanation is consistent with the following experimental observation.

Transconductance compression was less severe in the membrane MESFETs fabricated by etching from the front surface. In this case, the membranes were formed by etching the GaAlAs layer beneath the active GaAs layer (for 40s in 20% HF). In contrast, the membrane devices exhibiting transconductance compression were formed by etching the GaAlAs from the back surface (10s). The former membranes looked yellow whereas the latter were orange. A membrane etched in 20% HF was observed (under an optical microscope) to change in colour with increasing etch time from orange to yellow and then to white before the membrane was etched through, indicating that the 20% HF does etch GaAs, albeit slowly. Suppression of the transconductance compression near pinchoff is therefore attributed to the etching away of the low mobility layer.

Further evidence indicating the presence of a low mobility region are presented in Chapter 6.

4.5.2 Comparisons of Device Operation of Substrated and Unsubstrated MESFETs

In Table 4.1, the membrane MESFETs labelled (*) had nominally identical structures to the solid substrate devices (differing only in the absence of a substrate for a membrane FET). The operation of the substrated and the unsubstrated devices can therefore

be compared.

4.5.2.1 Substrate Effects

In a membrane device, the active channel was constricted by an additional surface depletion layer formed from the bottom surface. Thus the channel current density (of gateless MESFETs) was reduced to between 30% to 50% of that found on solid substrate. This bottom depletion layer enabled the membrane MESFETs, except the 0.1 μm gate–length device, to pinch–off at a lower reverse gate bias than that required for the solid substrate devices. But this same depletion layer results in loss of carriers accounting for the drastic drop in transconductance compared with solid substrate MESFETs (maximum g_m of about 300 mS/mm and 700 mS/mm have been measured on planar and recessed gate MESFETs respectively – see Chapter 6).

The injection of carriers into the substrate of a conventional (substrated) GaAs MESFETs has an adverse effect on device operation, one of which is increased output conductance (4.20). As a consequence, $Ga_{1-x}Al_xAs$ buffer layers have been used in place of the more conventional GaAs buffer layers (4.21). The band–gap mismatch at the GaAs/GaAlAs interface provides a barrier potential which confines carriers to the active GaAs layer. No carrier injection can take place in the absence of a substrate, as is the case in membrane MESFETs. The interesting observation from Table 4.1 is that the output conductance of the substrated and unsubstrated MESFETs are of the same order of magnitude. It can inferred that nearly total confinement of carriers is provided by the $Ga_{0.3}Al_{0.7}As$ buffer layer. This result is of particular relevance to the work in Chapter 6.

4.5.2.2 Gate–length and Surface States Effects

The 0.3 and 0.5 μm gate–length membrane devices exhibited good saturation and pinch–off characteristics. However this was not observed for 0.1 μm gate–length MESFETs whose gates showed poor control.

Shortening the gate–length has two major effects on the gate depletion layer. First, the depletion layer becomes less abrupt (in transition between $n = 0$ and $n = N_D$ where n = carrier concentration and N_D = doping concentration) (4.22). Second, the depletion layer becomes increasingly circular (instead of flat) when the gate–length becomes smaller than about the channel thickness (4.22–3). The width of a circular depletion layer changes less for a given change in gate bias compared with the case of a flat depletion layer (i.e. circular depletion layers are less effective in depleting the channel) (4.23).

The above short gate–length effects are further worsened by free surface depletion layer resulting from Fermi level pinning by surface states. The surface barrier height has been measured as 0.6 to 0.8 eV (4.24). This is comparable to an unbiased Schottky gate on GaAs. As the gate is shortened the gate depletion layer becomes "softer" (i.e. less abrupt) and more circular. It might be expected that by decreasing the gate–length a stage is reached whereby the gate depletion and its effect are masked by surface depletion. As the gate gets less effective in depleting the channel, the application of a gate bias might do little to overcome the surface states effect. This might explain the lack of control exercised by the 0.1 μm gate in membrane MESFETs. This argument is consistent with the following experimental evidence.

Transconductance compression (near zero gate bias), as determined from transconductance– gate bias plots (Figure 4.21), was observed in the solid substrate MESFETs with 0.2 and 0.1 μm gate– lengths and membrane MESFETs with 0.1 μm gate– length. The longer gate MESFETs on membranes and on solid substrates did no exhibit this phenomenom. It has been proposed by Chen and Wise (4.25) that, at a small reverse gate bias, the surface depletion near the drain may be wider than the gate depletion as shown in Figure 4.22. Under this condition, the drain current is controlled by the surface depletion layer rather than the gate thus giving rise to transconductance compression.

Solid substrate recessed gate MESFETs with 0.08 μm gate– length which showed very high transconductance and good saturation and pinch– off characteristics had been fabricated on the heterostructure used for membrane fabrication (see Chapter 6). This device is different to the 0.1 μm gate– length device in two respects. First, the device has a larger aspect ratio of the gate– length to channel thickness. Second, the recessed gate structure is thought to diminish the effect of the surface depletion as shown schematically in Figure 4.22. This is supported by experimental results which indicate that transconductance compression is a diminishing function of gate recess depth (presented in Chapter 6).

4.5.3 LSSLs

The d.c. characteristics of the LSSL with 10 nm pitch grating of 50 nm lines and 2.5 μm wide channel and the 2.5 μm gate– length membrane MESFETs were similar. It is likely that the individual Schottky junctions of the grating were blurred by surface depletion so

that the resultant depletion profile resembled that formed under the gate of the MESFET as illustrated in Figure 4.23.

The fingers of the grating are twice as small as the gate of the 0.1 μm gate length membrane MESFETs. The depletion under each finger was therefore likely to be worse affected by the adverse short gate– length and surface depletion effects. Therefore, the periodicity of the grating was more than likely to be masked by the surface depletion even with application of a bias. This problem could well be solved by using a recessed structure. However, it was decided that forming a recessed structure in a 50 nm thick GaAs membrane would be extremely difficult, if not impossible.

It was concluded, based on the above and the membrane MESFET results, that there was little prospect of observing superlattice effects on the grating structures fabricated on the membranes. This work was not pursued further because of this and due to shortage of time.

4.6 Summary

The fabrication of FET devices on 50 nm thick GaAs membranes has been demonstrated. The use of these membranes facilitates very high resolution electron beam lithography.

Experimental evidence was presented indicating that transconductance compression near pinchoff in GaAs MESFETs with undoped $Ga_{1-x}Al_xAs$ may be due to degradation of carrier mobility in the active region near the GaAs/GaAlAs interface. This compression is believed to be caused by interface impurities and surface roughness. With a membrane device it was demonstrated that these effects can be eliminated by etching the thin surface layer containing the defects (i.e.

surface roughness and impurities).

Comparisons between d.c. performance of substrated ($Ga_{0.3}Al_{0.7}As$ buffer layer) and unsubstrated (membrane) GaAs MESFETs were presented. It was shown that performance of membrane devices was affected by an additional depletion layer extending from the back surface. This surface depletion enabled the unsubstrated devices to be pinched off at smaller reverse gate bias but at the same time reduced the value of the transconductance through loss of carriers. The output conductance of substrated and unsubstrated devices with nominally identical structures were found to be similar, indicating that good carrier confinement in the active layer was provided by the $Ga_{0.3}Al_{0.7}As$ buffer layer.

One result in reducing the MESFETs gate–length was loss of gate control. This was thought to be due to the combined effects of short gate–length and free surface depletion. At small reverse gate voltages, the operation of short gate–length devices was dominated by surface depletion giving rise to transconductance compression. For a grating–gate, the Schottky junctions formed by individual fingers were believed to be masked by the surface depletion such. Thus the depletion profile under the grating resembled that which would be formed under a solid gate with length equivalent to the total width of the grating.

In conclusion, the effect of surface states prevented exploitation of very high resolution capability of electron beam lithography to fabricate high speed or novel FET devices, namely ultra–short gate–length MESFETs and LSSLs, on the GaAs membranes.

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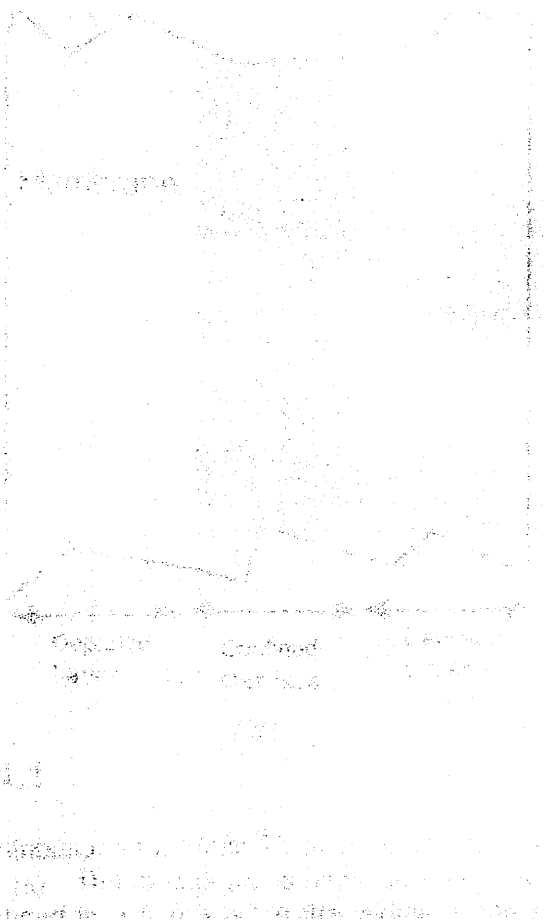


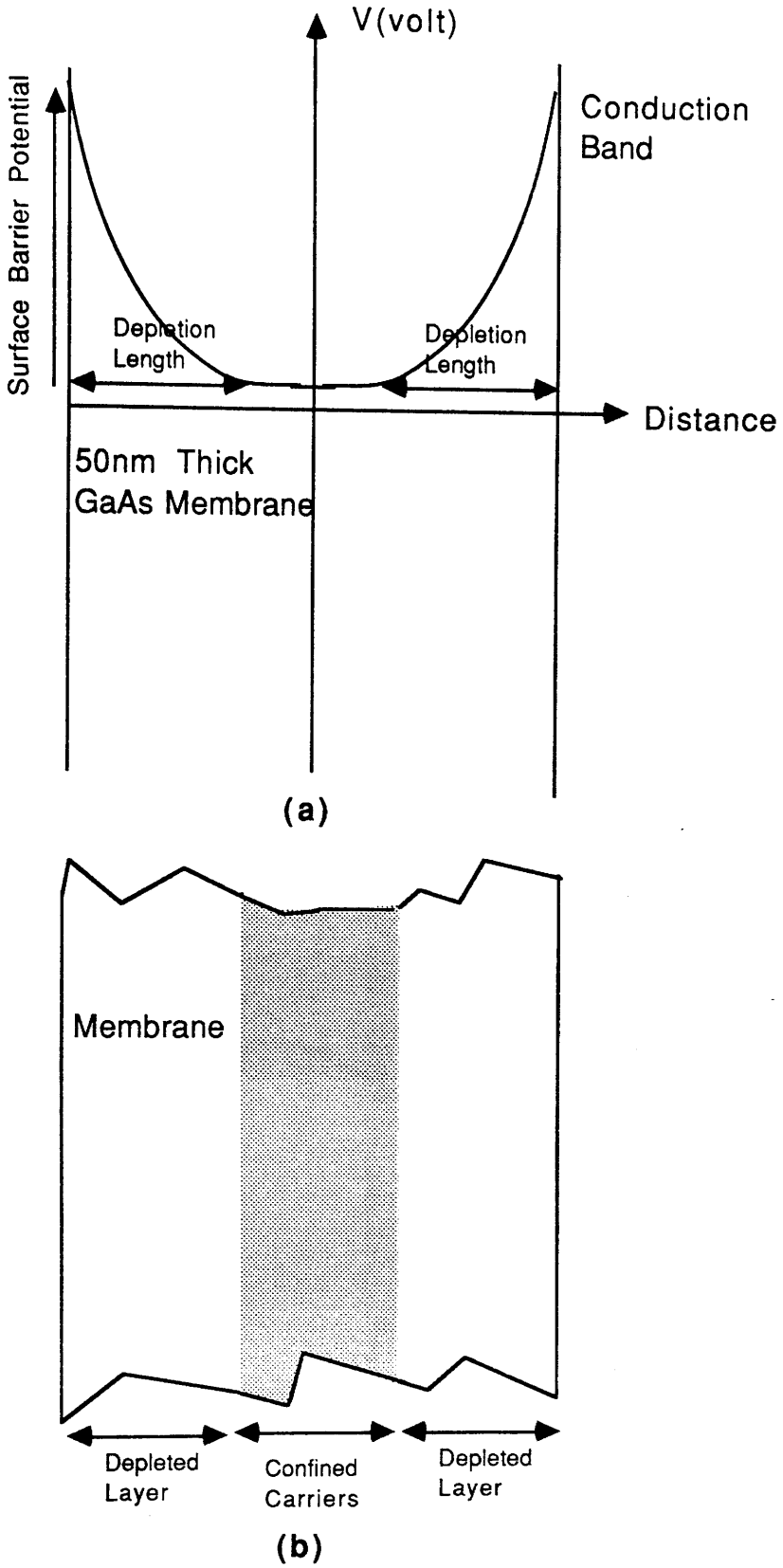


Figure 4.1

The potential distribution in a 50nm Thick GaAs membrane is shown schematically in (a). The membrane is depleted from both surfaces so that carriers are confined in a thin layer in the middle of the membrane (b).

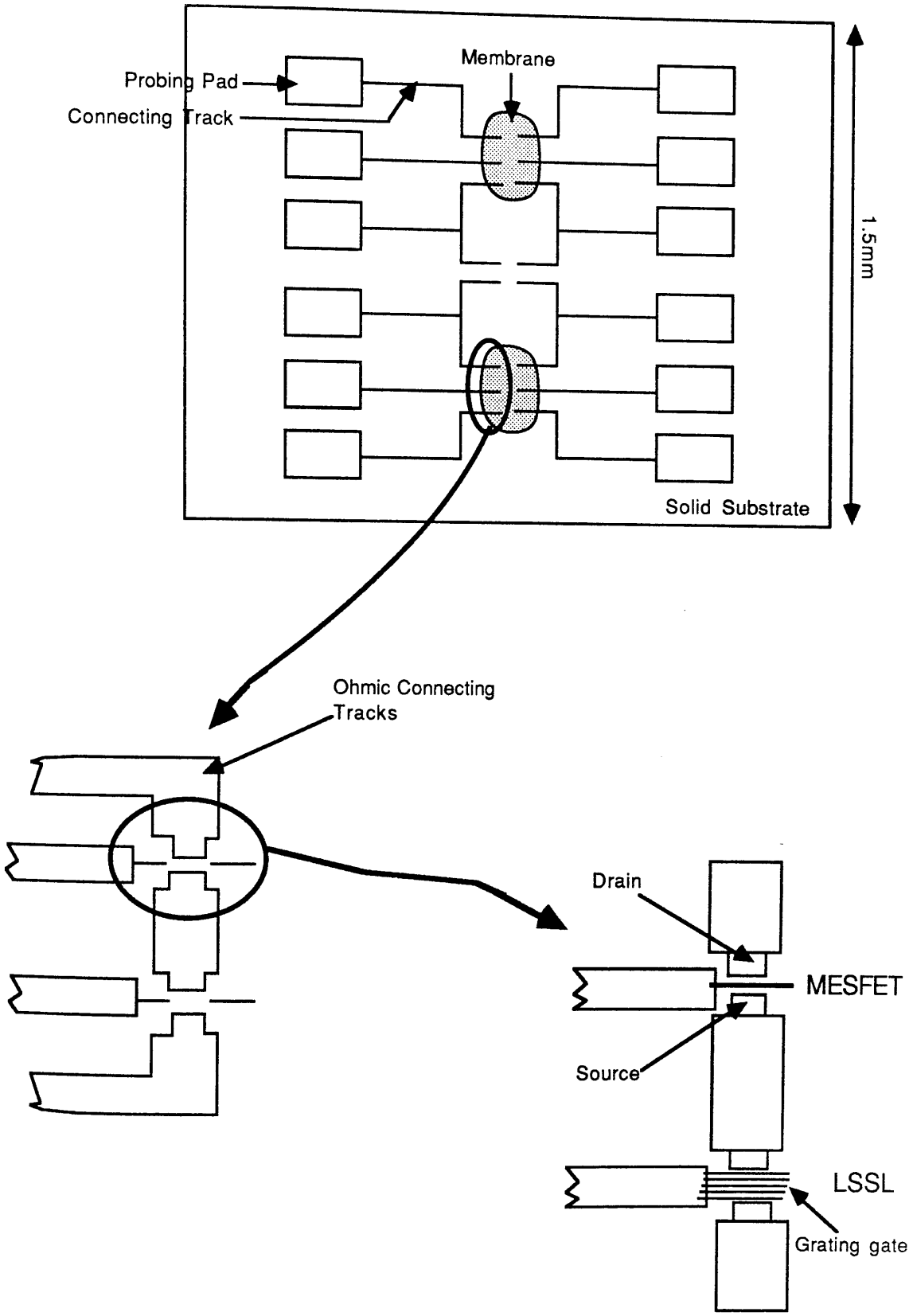


Figure 4.2

Layout of Membrane devices on a 1.5x1.5 mm chip containing two membranes. The membrane devices are connected to the probing pads located on solid substrate via ohmic connecting tracks.

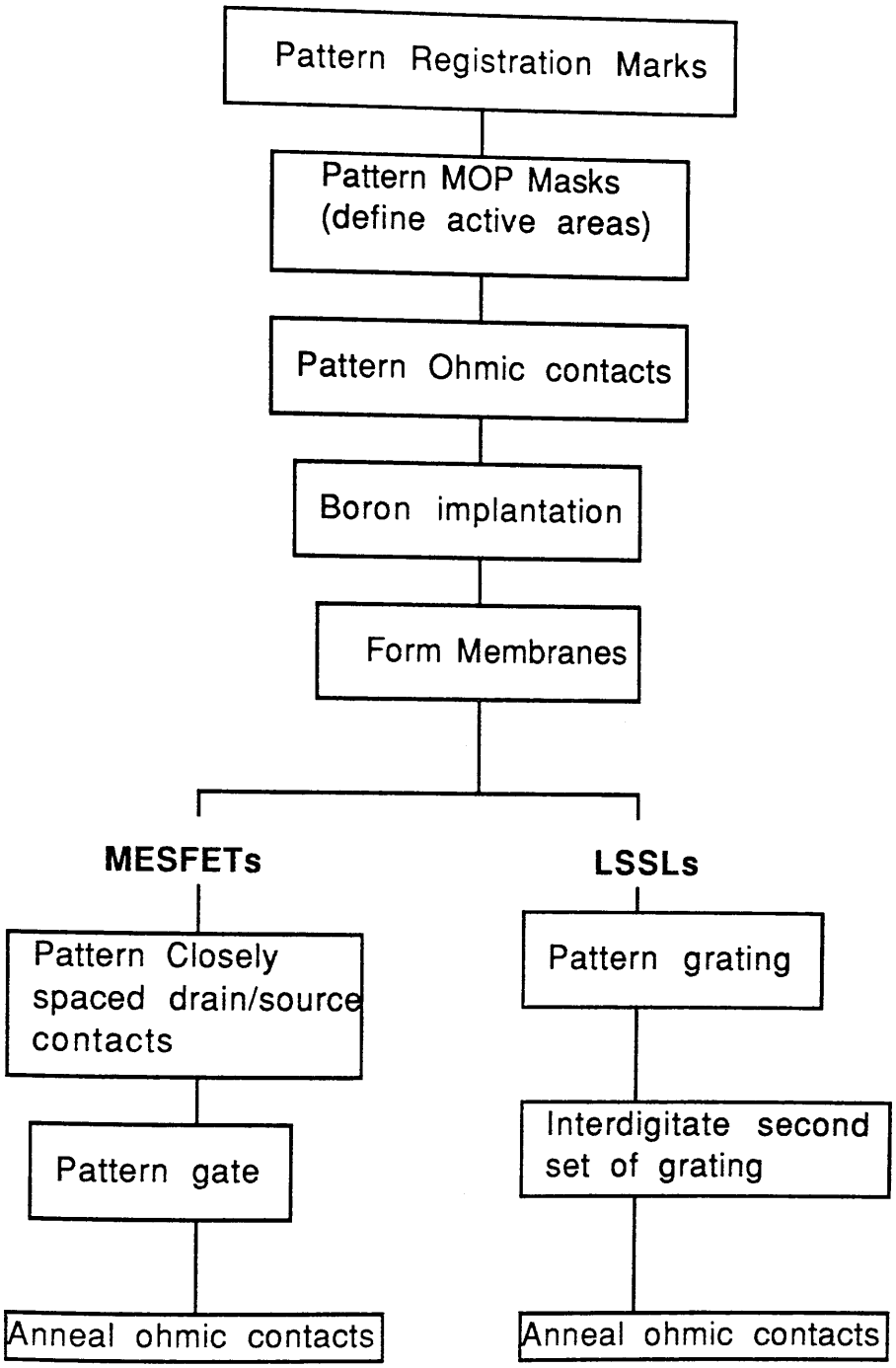


Figure 4.3 Fabrication of Membrane FET Devices

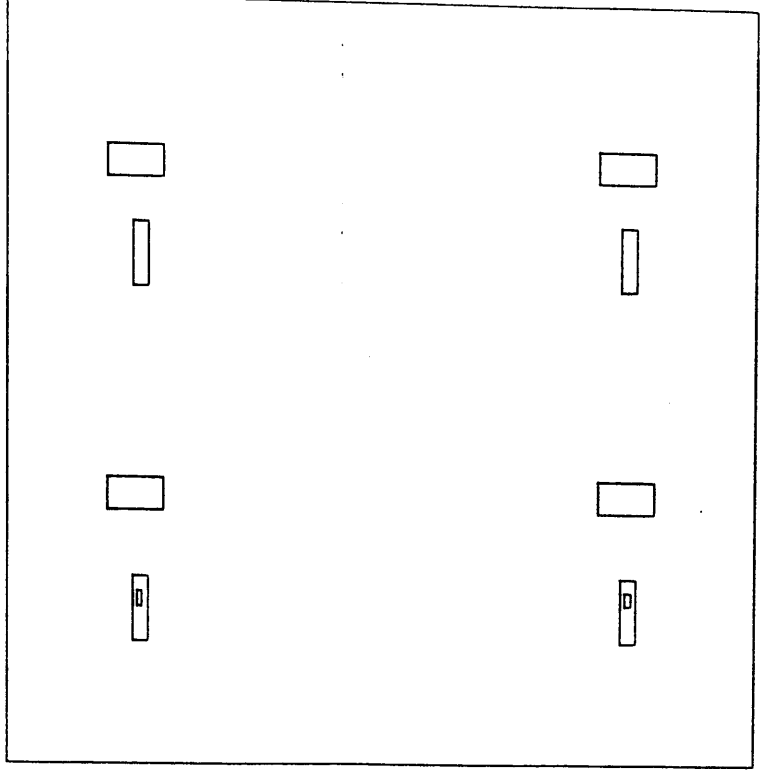


Figure 4.4 Registration Mark Pattern

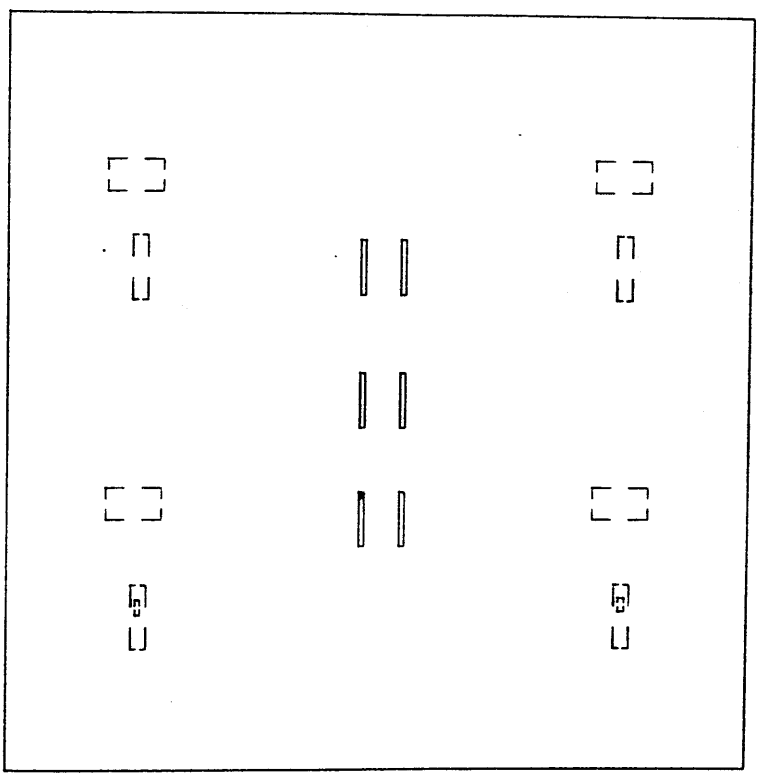
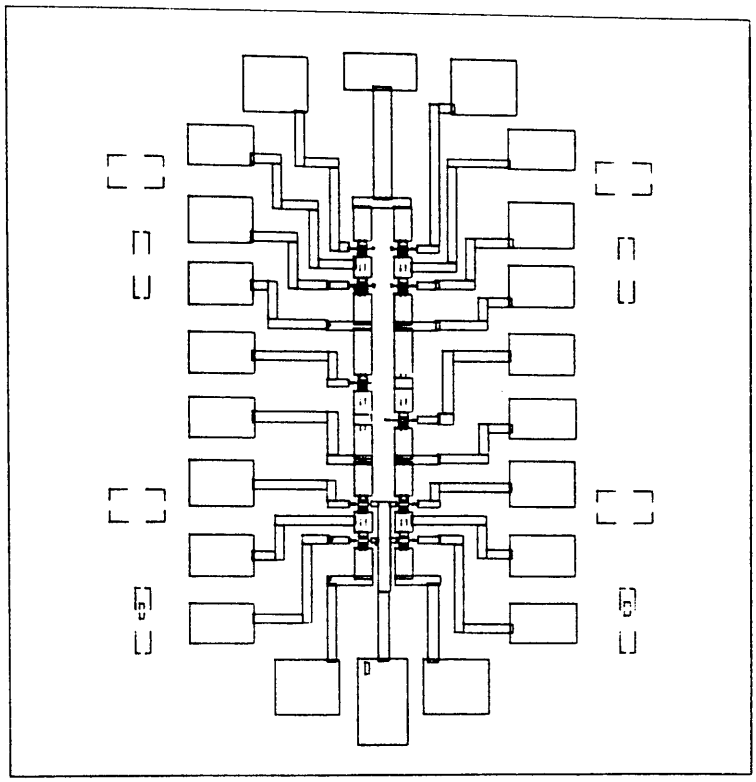
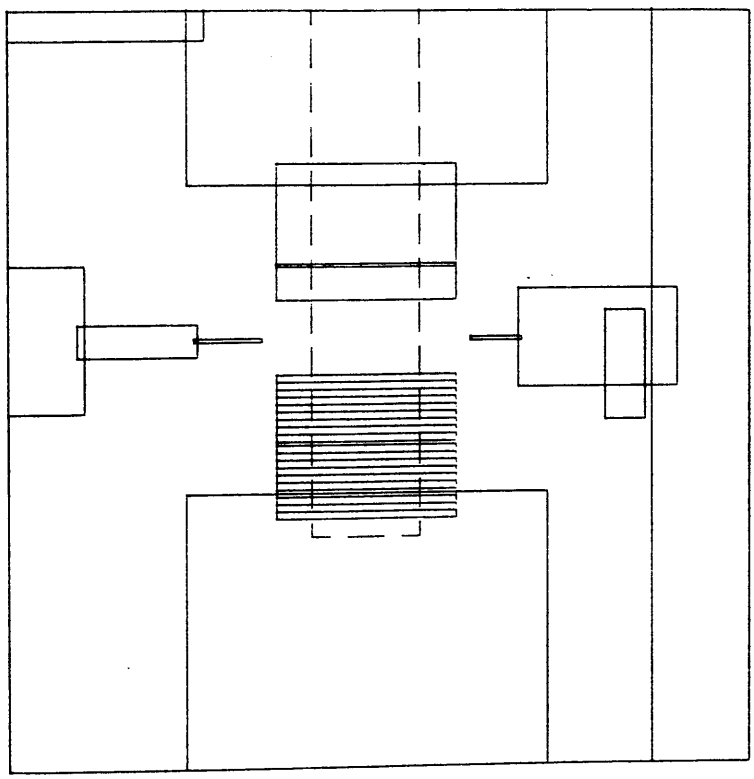


Figure 4.5 MOP Mask Pattern



(a)



(b)

Figure 4.6

a) Ohmic Contact Pattern (b) Magnified view showing alignment markers for gate alignment (the registration and MOP mask patterns are outlined-dashed line)

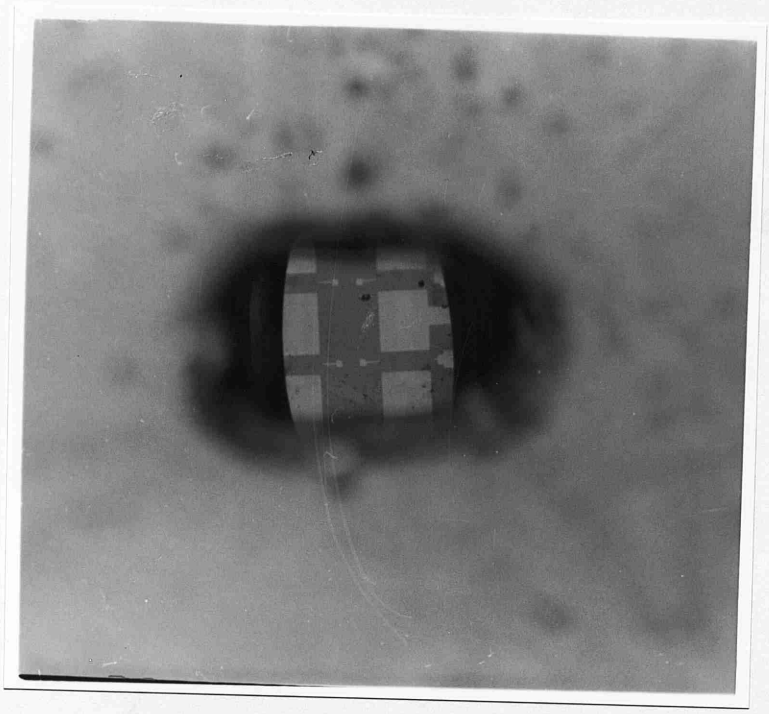


Figure 4.7

Photograph showing metallisation on a membrane viewed through the etch well

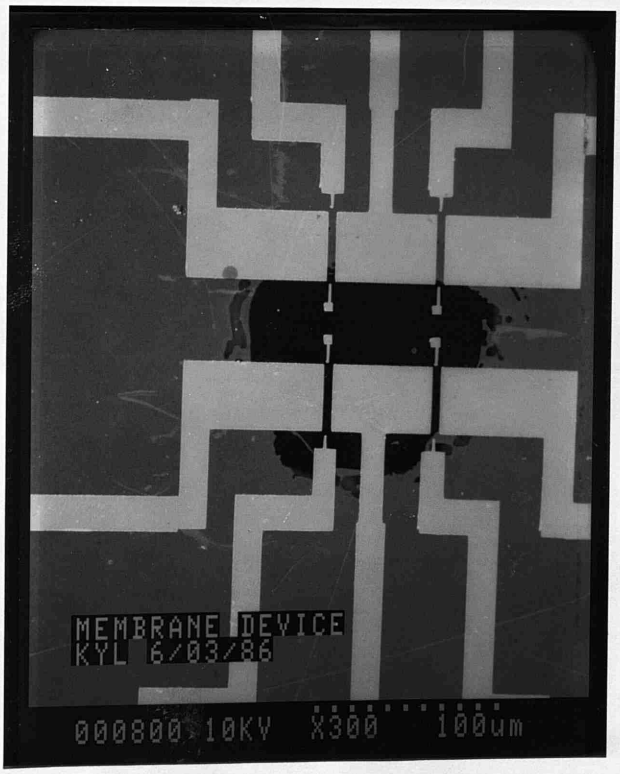


Figure 4.8

SEM micrograph of ungated membrane MESFETs

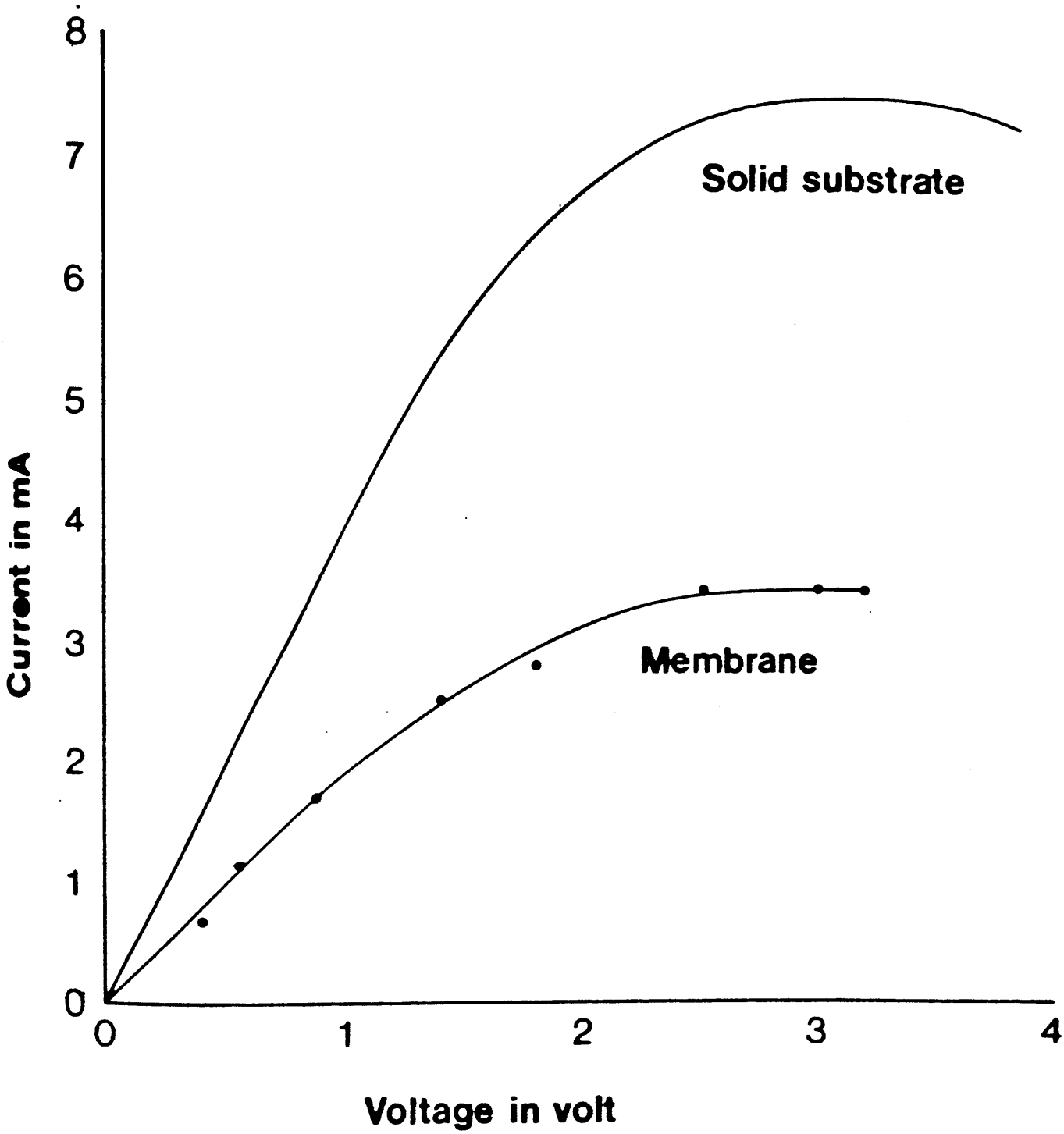
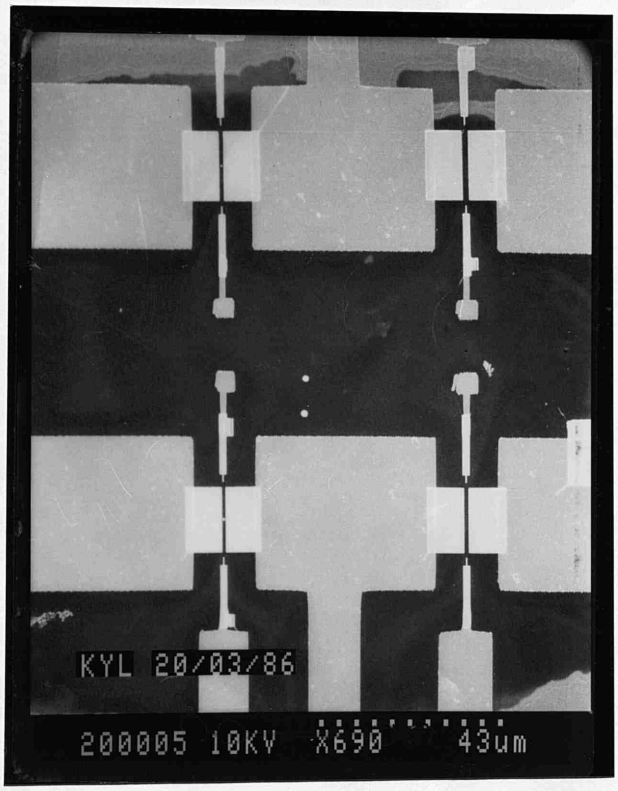
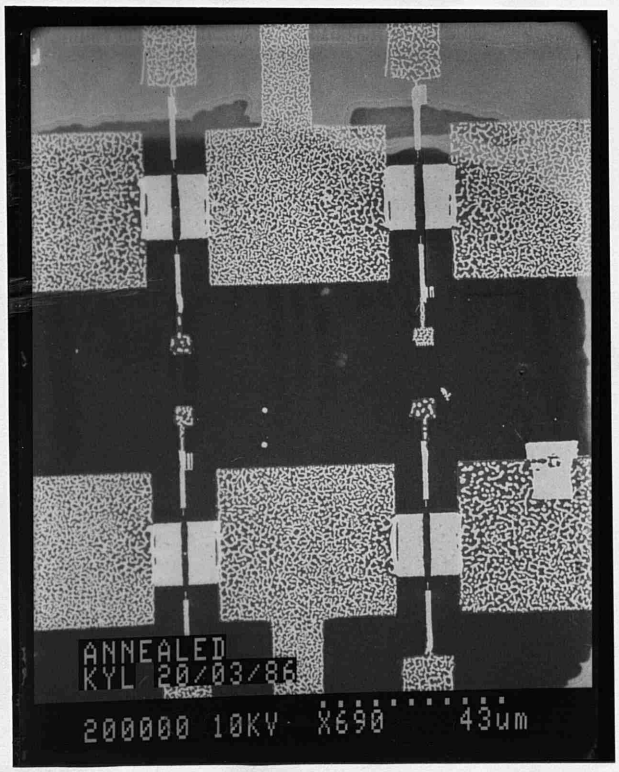


Figure 4.9

I-V characteristics of gateless membrane and solid substrate MESFETs. The membrane results were obtained by using single 2μs pulses.



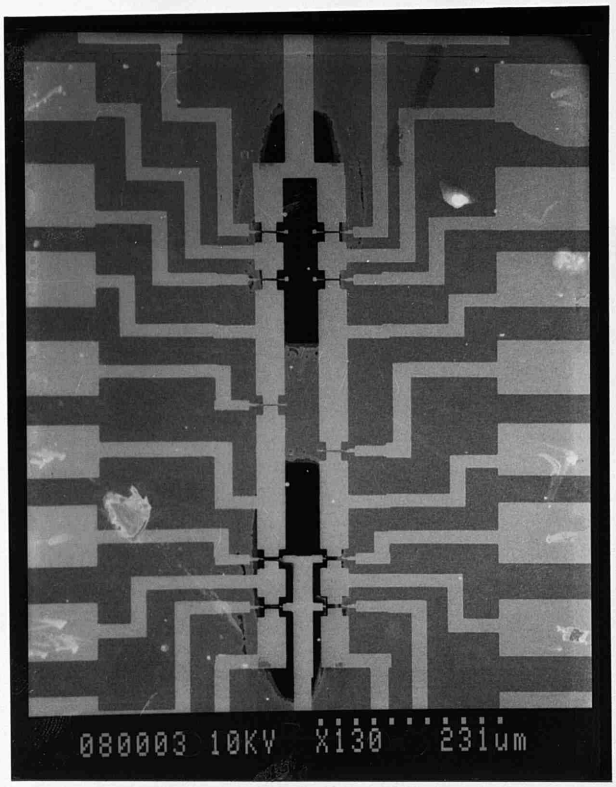
(a) Before Annealing Contacts



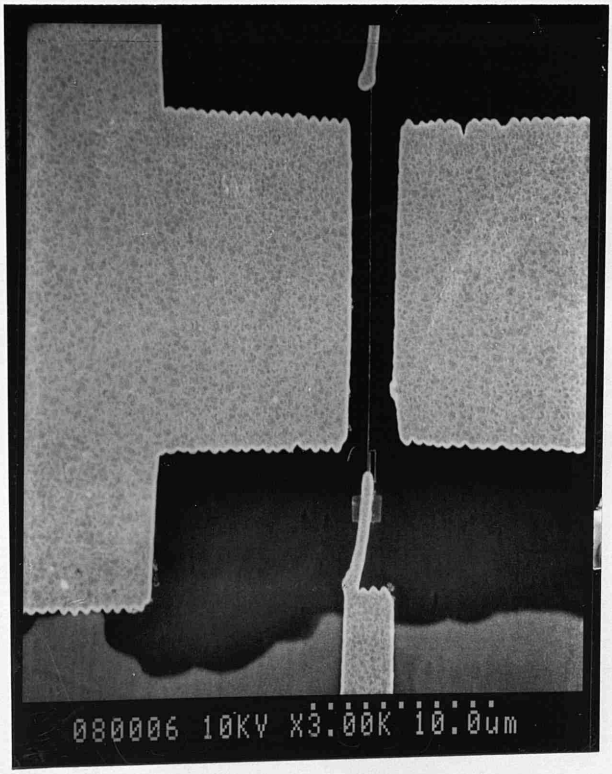
(b) After Annealing

Figure 4.10

SEM micrographs showing closely spaced drain-source contacts patterned on a membrane.



a) micrograph of a chip with two membranes, each with 4 devices and 2 solid substrate devices



b) micrograph of a membrane MESFET with 60nm gate

Figure 4.11 SEM micrographs of Membrane MESFETs

Figure 4.12

STEM micrograph of a FET device with a grating gate.

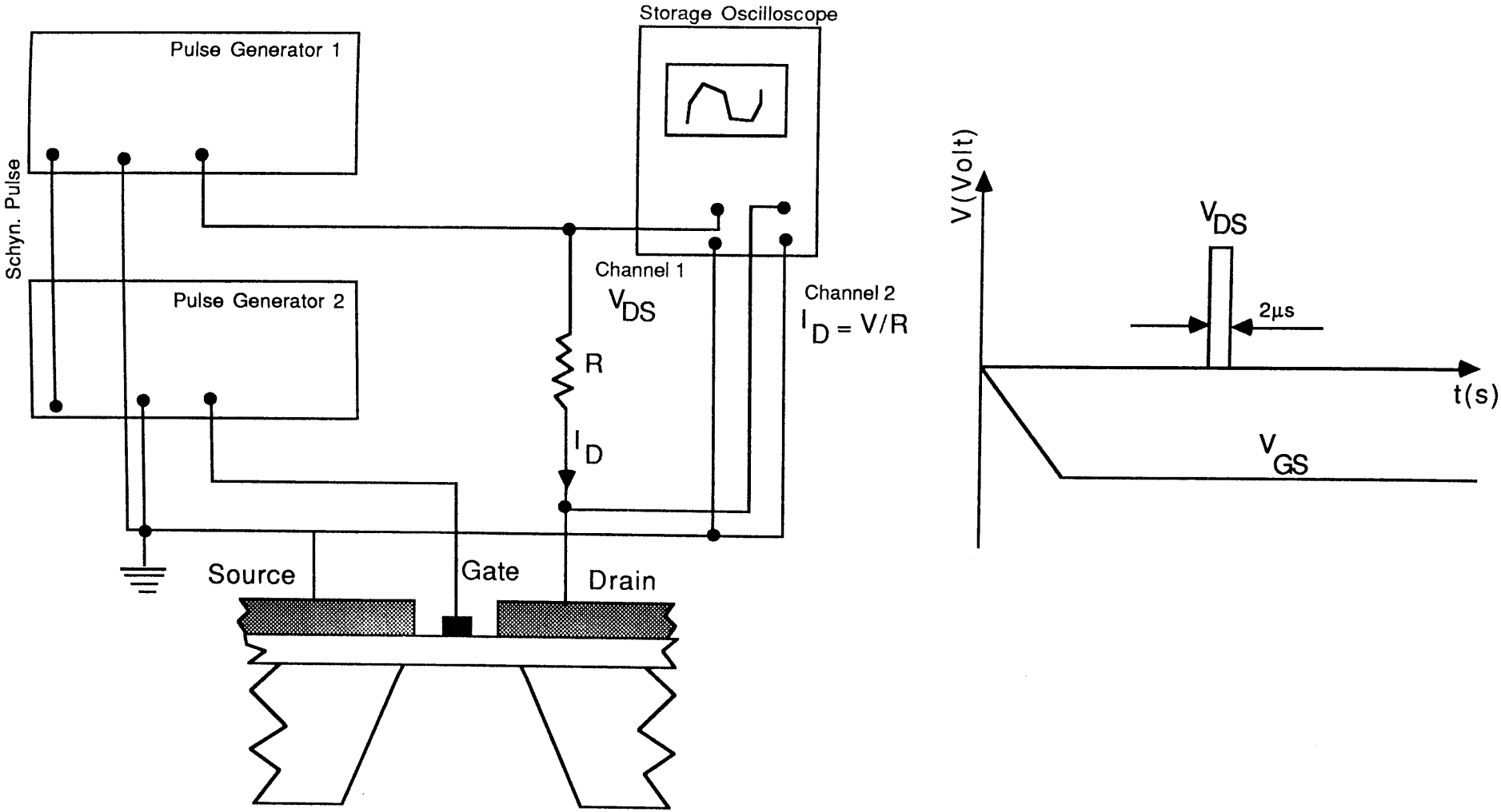


Figure 4.13 Electrical Testing of Membrane MESFET by Pulsing

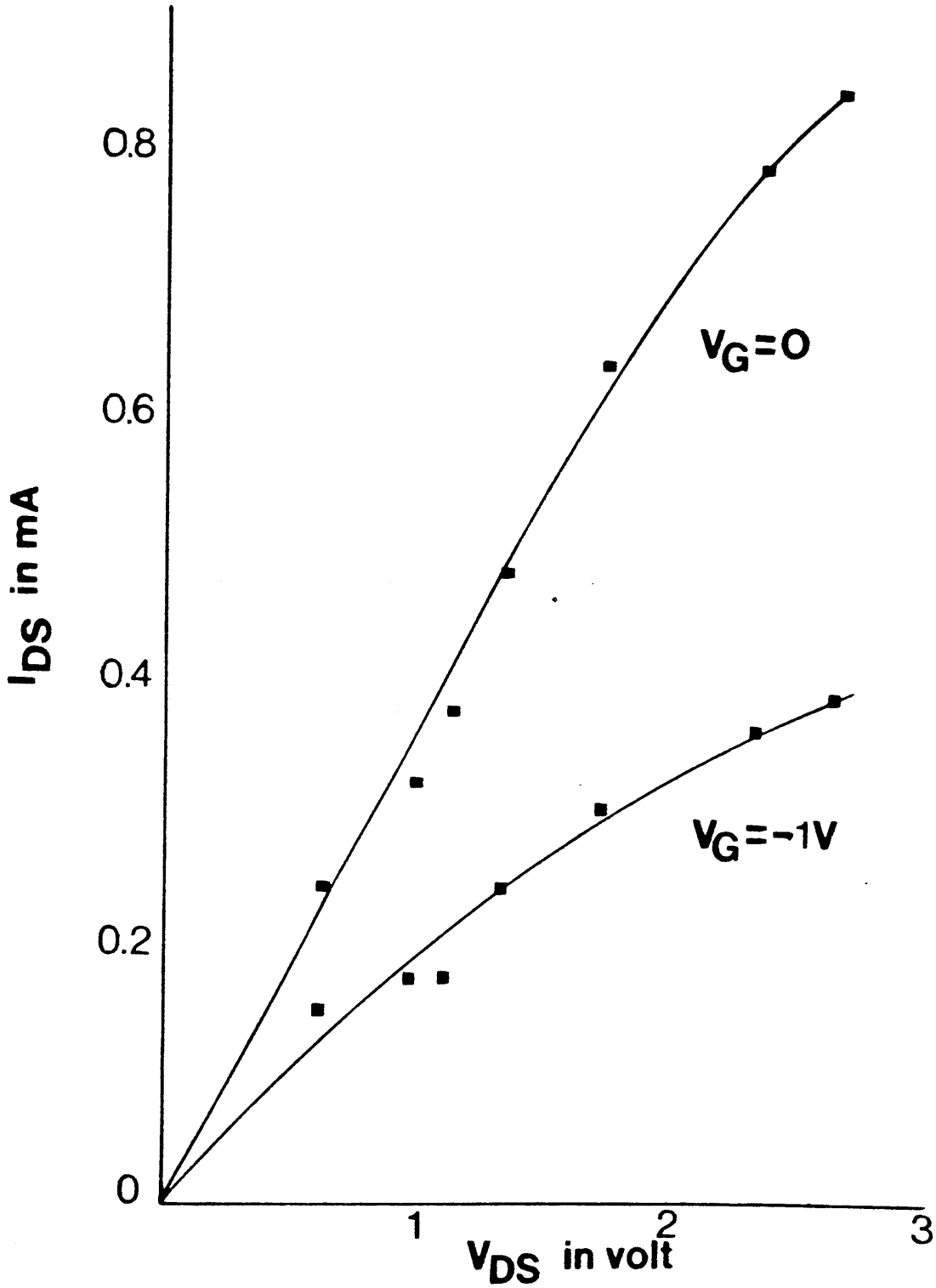


Figure 4.14

Pulsed I-V Characteristics of a 0.5μm gate-length Membrane MESFET.
Gate width=10μm
Drain-source gap=2μm

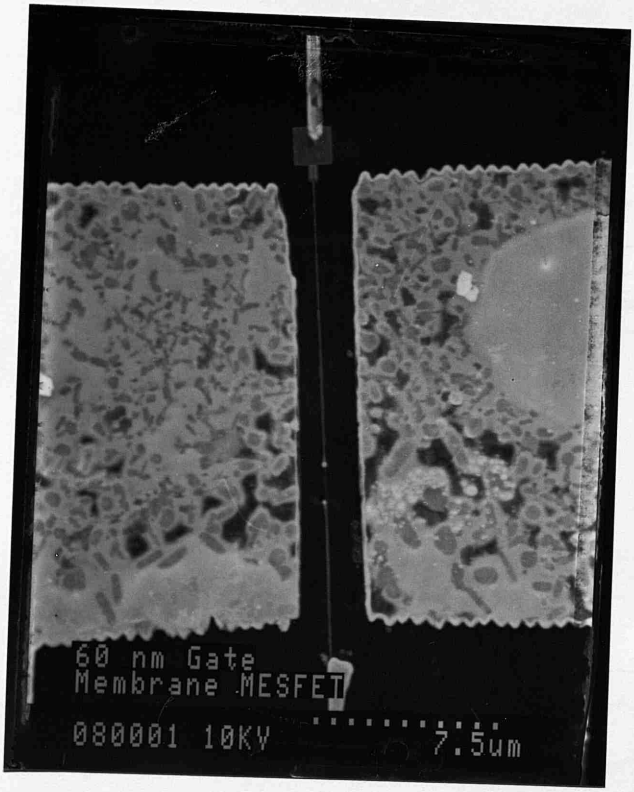
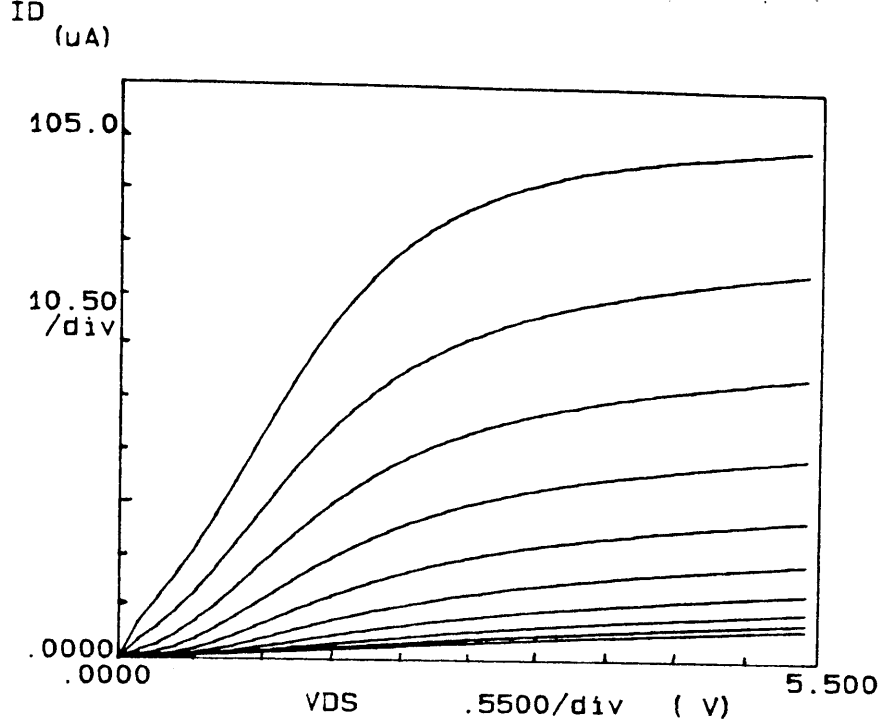
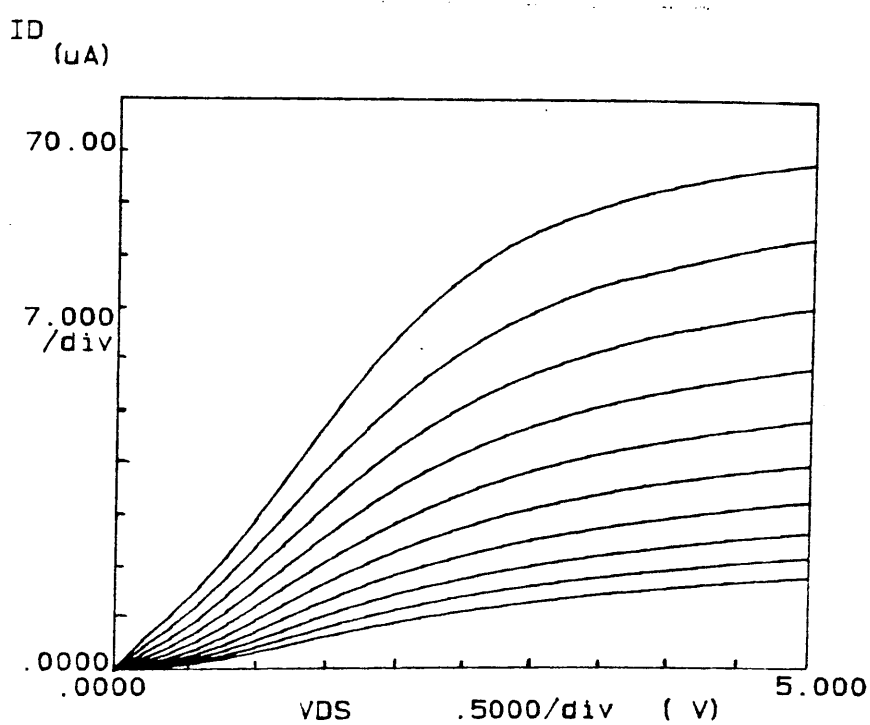


Figure 4.15

SEM micrograph of a membrane MESFET with a blown gate



(a) Gate bias V_{GS} = 0, -0.1, -0.2, -0.3,.....-0.9.



(b) Bias applied to Grating V_{GS} = 0, -0.05, -0.1, -0.15, -0.2,.....,-.0.45.

Figure 4.16

I-V characteristics of (a) MESFET with 2.5μm gate-length, 10μm gate-width and drain-source gap of 4μm (b) LSSL with 100nm pitch grating, 50nm wide fingers, 10μm channel width and drain-source gap of 10μm. The devices were fabricated on 50nm thick GaAs membrane formed by etching from the back surface.

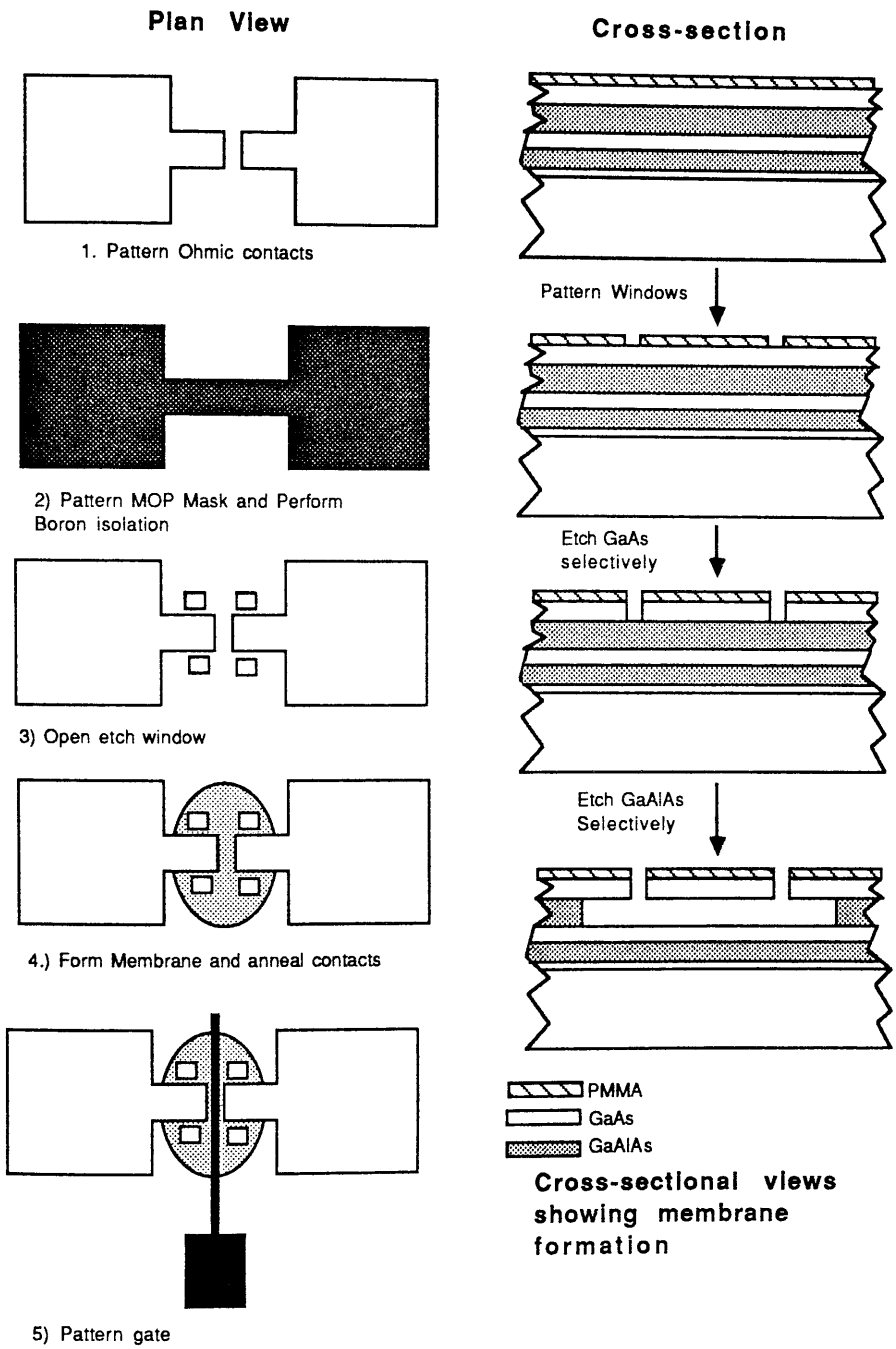


Figure 4.17 Novel Membrane MESFET Fabrication

(a)

(b)

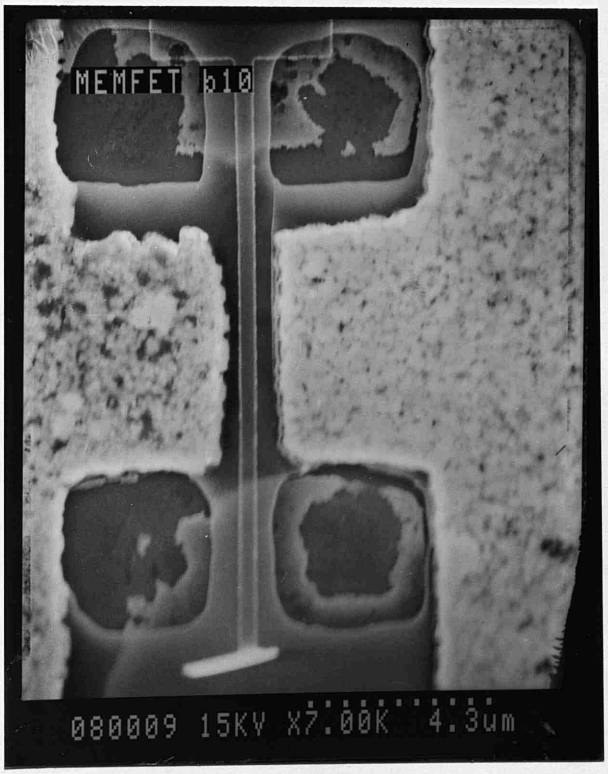


Figure 4.18

SEM micrograph of (a) a membrane fabricated by etching from the front surface (back scattered electron image) (b) a MESFET fabricated on such a membrane.

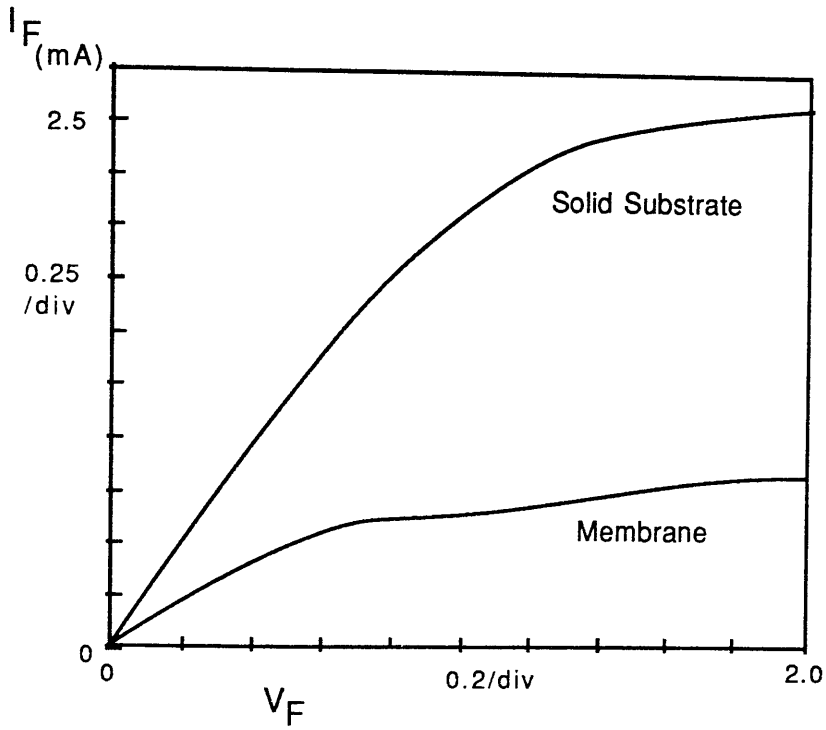
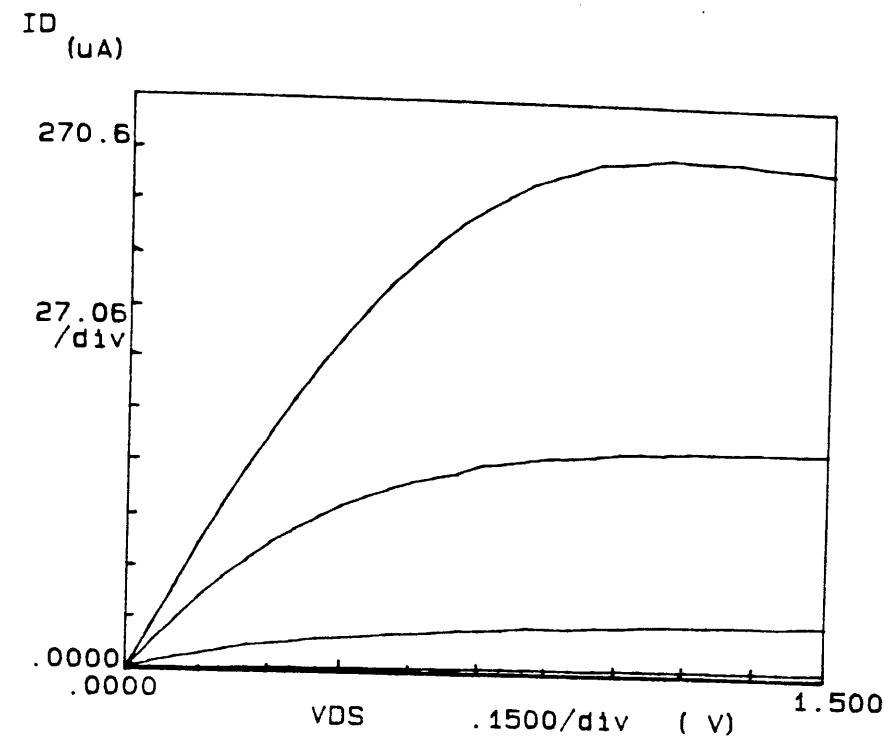
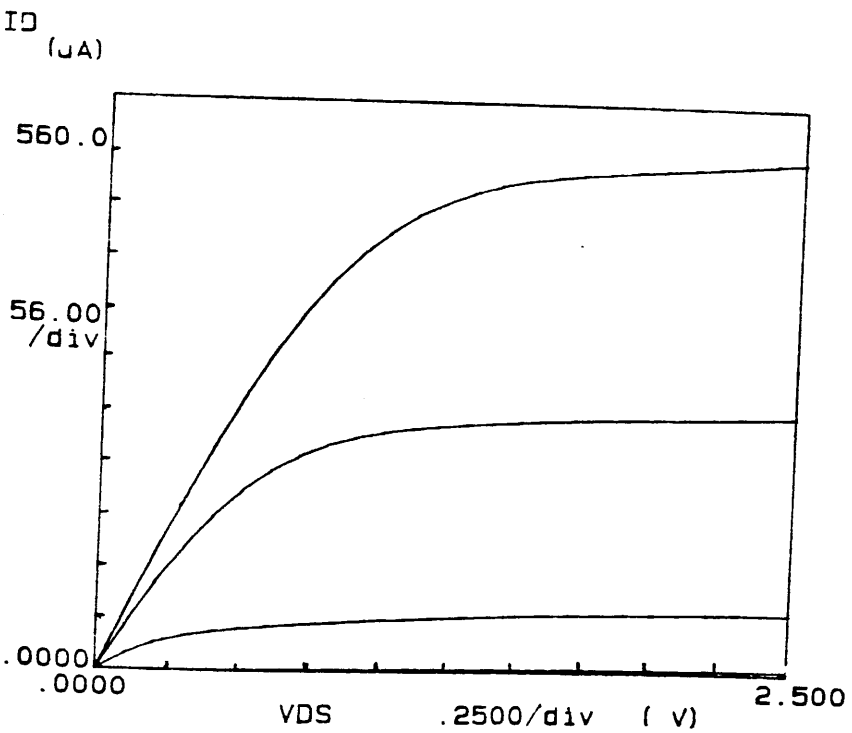


Figure 4.19

I-V Characteristics of nomianlly identical ungated MESFETs, one fabricated on 50nm thick GaAs membrane, the other on solid subtrate. The drain-source separation was 1μm and the channel was 5μm wide. The membrane was formed by etching from the front surface



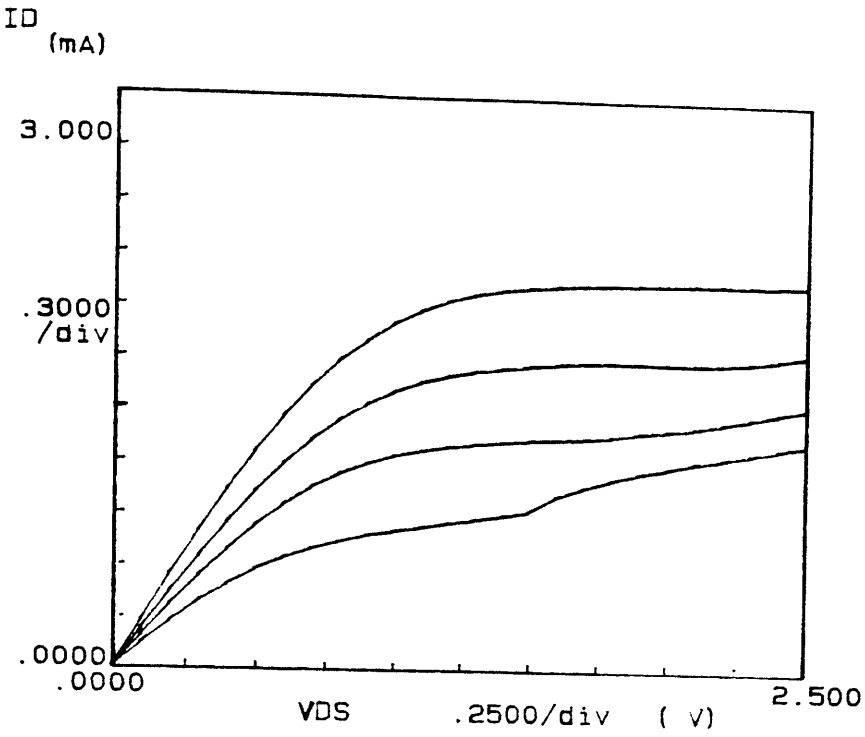
(a) V_{GS} = 0, -0.5, -1.0,.....,-1.5V.



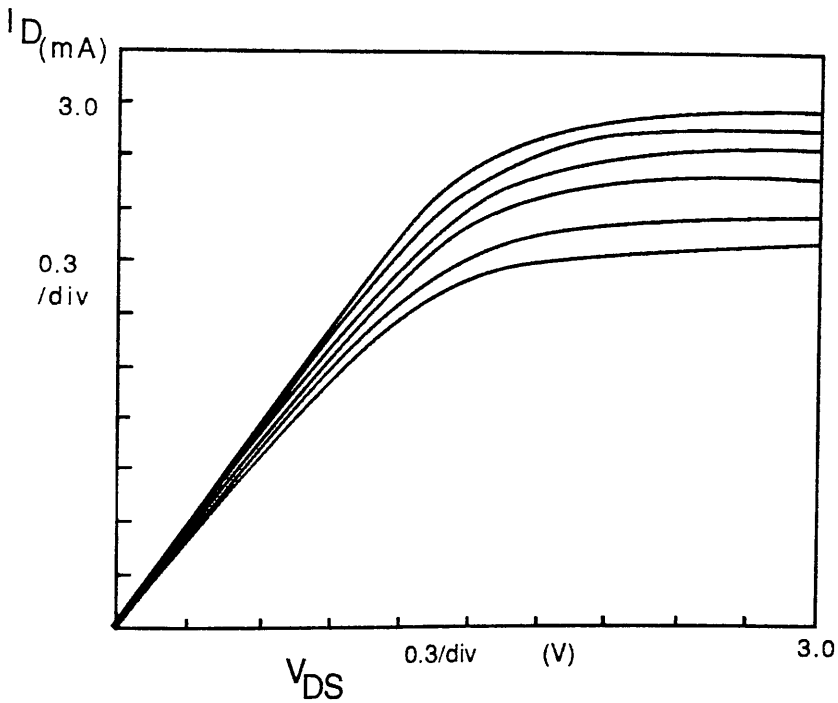
(b) V_{GS} = 0, -0.5, -1.0,.....,-1.5V

Figure 4.20a-b.

I-V Characteristics of GaAs Membrane MESFETs
(a) 0.5μm gate-length (b) 0.3μm gate-length.



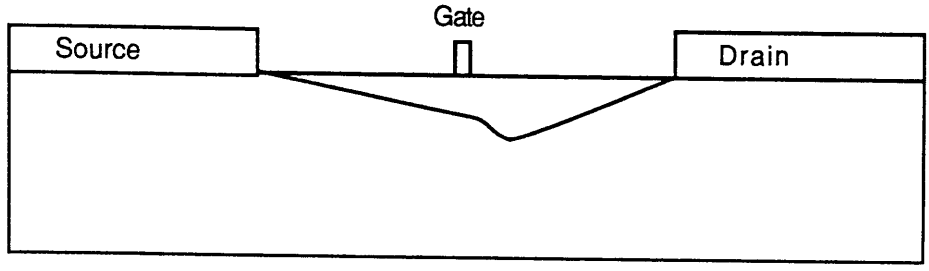
(d) V_{GS} = 0, -0.5, -1.0, -1.5V



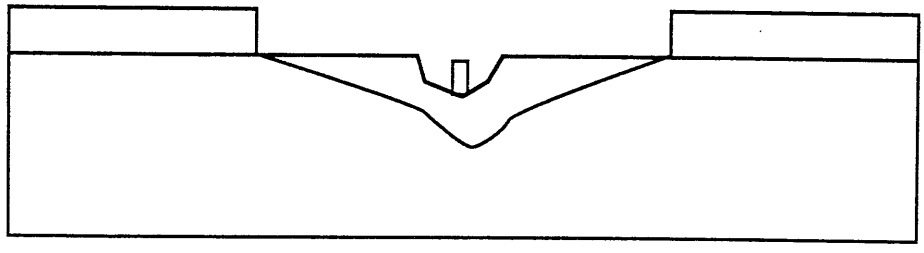
(e) V_{GS} = 0.5, 0, -0.5, -1.0,.....,-2.0V

Figure 4.20d-e

I-V Characteristics of Solid Substrate GaAs MESFETs
(d) gate-length = 0.5μm (e) gate-length = 0.1μm



a) At a small gate bias, the free surface depletion layer between the gate and the drain may be wider than the gate depletion. Under this condition, the drain current is controlled by the surface depletion rather than the gate, resulting in transconductance compression.



b) The effect of the surface depletion layer can be diminished by using a recessed gate structure. This is because the gate depletion layer extends deeper into the channel with respect to the surface depletion layer in doing so (i.e the channel under the gate is narrower than the case in (a)).

Figure 4.22

Schematic representations of effects of surface depletion layer.

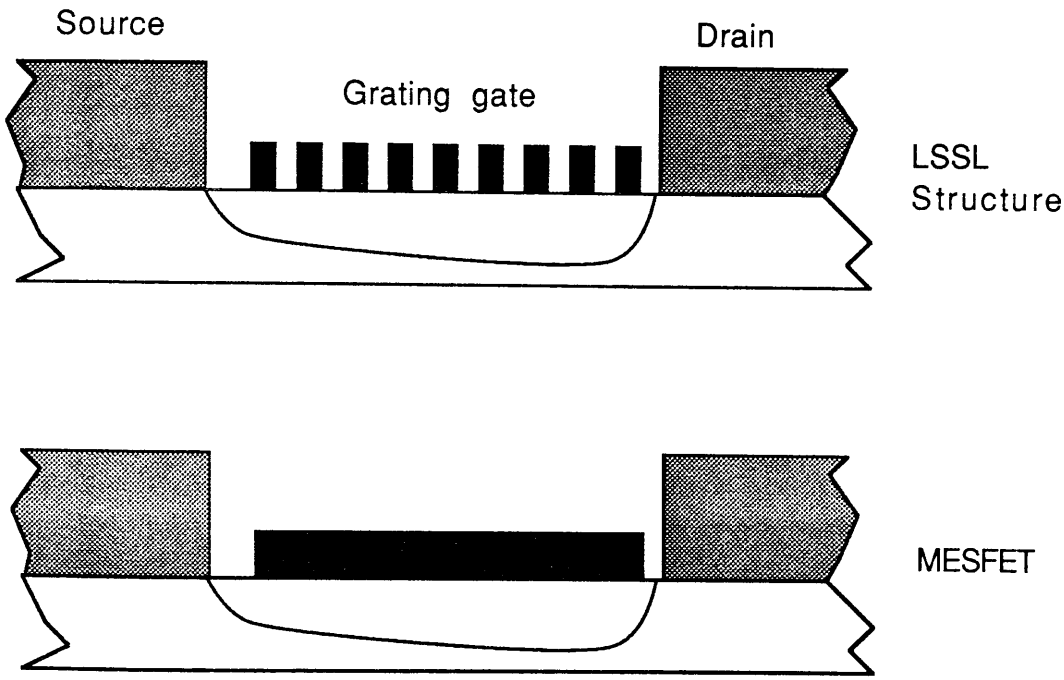


Figure 4.23

Surface depletion blurs the indivdual Schottky junction of the grating so that the resultant profile resembles that formed under the gate of a MESFET.

5.1 Introduction

The work presented in this chapter concerns the study of the band structure of 50nm thick n^+-GaAs ($N_D=3\times10^{18}$ cm^{-3}) membranes and was carried out in collaboration with Dr. John Davies of this Department and with the Physics Department of Nottingham University.

GaAs Membrane As a 2– Dimensional Quantum Structure

It was observed in Chapter 4 that the saturated drain current of ungated MESFETs fabricated on GaAs membranes was 30% to 50% that of nominally identical solid substrate devices. In GaAs, pinning of the Fermi level by surface states in the forbidden gap (5.1) results in carrier depletion in the region below the surface. For solid substrate devices, only the top surface is depleted. In membrane devices, an additional depletion layer extends from the bottom surface which accounts for the reduced drain current. Therefore, electrons in a GaAs membrane may be seen to be confined to a thin centre layer (Figure 4.1). A theoretical investigation indicates that the confinement results in quantisation of electron energies in the direction normal to the membrane surface (while electrons are free in the other two directions). This is demonstrated next in section 5.2. In order to probe these bound states, absorption and photoconductivity measurements were carried out.

5.2 Calculation of Confined Energy States in a 50 nm Thick GaAs Membrane

Potential Distribution in a 50nm thick GaAs membrane

In GaAs, pinning of the Fermi level by surface states results in band bending at the surface of between 0.6 and 0.8eV. The surface depletion width L is given by the abrupt depletion edge approximation (5.1):

$$L = \left[\frac{2\epsilon V_B}{qN_D}\right]^{\frac{1}{2}} \qquad (1)$$

where V_B= surface barrier height

q = electronic charge

ϵ = absolute permittivity of GaAs

N_D= donor concentration.

If a V_B of 0.7eV is assumed, L will be 18nm. In Chapter 4, L was estimated to be about 17nm from the saturated drain currents measured on membrane and solid substrate ungated MESFETs (for the case in which the saturated drain current of a membrane device was 50% that of solid substrate device– Section 4.2.2). A simple model, shown schematically in Figure 5.1, may then be used to represent the potential distribution in the membrane. In this model, the membrane is divided into an undepleted region (14nm wide) sandwiched between two depletion regions (each 18nm wide). The conduction and valence bands are flat in the central region but are bent in the depletion regions. The potential distribution v(z) in these regions are defined as follows.

In the Flat Region

$$v(z) = 0 \qquad ; -s<z< s \qquad (2)$$

In the Depletion Region

Starting from Poisson's Equation

$$\frac{\partial^2 v(z)}{\partial z^2} = \frac{-\rho}{\epsilon} \qquad (3)$$

where ρ= space charge density
$= qN_D$

Integrating equation (3) twice gives

$$v(z) = \frac{A(|z|-s)^2}{2} \quad ; s<z<d \text{ and } -d<z<-s \qquad (4)$$

$(|d|-|s|=L)$

where $A= qN_D/\epsilon$.

Restriction of electron motion in the potential well leads to quantisation of electron energies in the conduction band. In the valence band, quantisation of hole energies occurs in the depletion regions due to confinement of holes between the curved part of the valence band (this represents a potential barrier to holes) and the surface.

Confined electron and hole states are calculated below using the WKB (Wentzel, Kramers and Brillouin) approximation method (5.2). This method is chosen because of its simplicity.

Calculation of Confined Electron States

In a uniform potential V, the Schrodinger Equation appropriate for 1− dimensional quantum well is given by (5.3)

$$-\frac{d^2u}{dz^2} = \frac{2m_e^*}{\hbar^2}(E_n-V)u = k^2u$$

where k is the wave vector in the z-direction defined as

$$k^2 = \frac{2m_e^*(E_n-V)}{\hbar^2}$$

In a non-uniform potential an approximation of the wave vector is given by

$$k(z)^2 = \frac{2m_e^*(E_n-V(z))}{\hbar^2} \qquad (5)$$

u = wave function in the z-direction
E_n = nth energy level
$\hbar$ = reduced Planck's constant
m_e^* = electron effective mass
n = 0,1,2,3,4,5,6.....

The WKB approximation for bound states is given as (5.2)

$$\int_{-z_n}^{z_n} k(z)dz = (n+\tfrac{1}{2})\pi \qquad (6)$$

where z_n and $-z_n$ are classical turning points indicated in Figure 5.1. (*A similar application of the WKB approximation can be found in (5.2), pp 275 to 277*). The contributions to the integral in equation (6), say I, from the flat (I_{flat}) and parabolic ($I_{parabolic}$) band regions are evaluated separately.

Flat Region $-s<z<s$

Substituting (2) and (5) into (6)

$$I_{flat} = 2s\left[\frac{2m_e^*E_n}{\hbar^2}\right]^{\frac{1}{2}} \qquad (7)$$

Parabolic Regions

As the well is symmetrical, it is adequate to consider only the case $z>s$. Substituting (4) and (5) into (6)

$$I_{parabolic} = \int_s^{z_n} dz\left[\frac{2m_e^*(E_n-A(z-s)^2/2)}{\hbar^2}\right]^{\frac{1}{2}} \qquad (8)$$

V(z) is equal to E_n at the turning point i.e. at $z= z_n$. Therefore, from (4)

$$E_n = \frac{A(z_n-s)^2}{2} \qquad (9)$$

To solve equation (8) let

$$\xi = \left[\frac{A}{2E_n}\right]^{\frac{1}{2}}(z-s) \qquad (10)$$

Substitute (10) into (8). The limits of the integration are found as follows:

At $z = s$, $\xi_{min} = 0$
At $z = z_n$, $\xi_{max} = 1$ (from (9) and (10))
The integral (8) then becomes

$$I_{parabolic} = \left[\frac{2m_e^*E_n}{\hbar^2}\right]^{\frac{1}{2}}\left[\frac{2E_n}{A}\right]^{\frac{1}{2}}\int_0^1 d\xi(1-\xi^2)^{\frac{1}{2}} \qquad (11)$$

The solution below is obtained by substituting $\xi = \cos\theta$ into (11)

$$I_{parabolic} = \frac{\pi}{4}\left[\frac{4m_e^*}{\hbar^2 A}\right]^{\frac{1}{2}} E_n \qquad (12)$$

Therefore the solution to equation (6) is given by

$$I = I_{flat} + 2xI_{parabolic} = (n+\tfrac{1}{2})\pi$$

$$I = 2s\left[\frac{2m_e^* E_n}{\hbar}\right]^{\frac{1}{2}} + \pi\left[\frac{m_e^*}{\hbar^2 A}\right]^{\frac{1}{2}} = (n+\tfrac{1}{2})\pi$$

which results in

$$E_n + \beta E_n^{\frac{1}{2}} - \varepsilon_n = 0 \qquad (13)$$

$$\text{where } \beta = \frac{(2s)(2A)^{\frac{1}{2}}}{\pi} \qquad (14)$$

and

$$\varepsilon_n = (n+\tfrac{1}{2})\hbar(A/m_e^*)^{\frac{1}{2}} \qquad (15)$$

The confined electron energy levels in the conduction band are given by the solutions to the quadratic equation (13),

$$E_n = \varepsilon_n + \beta^2/2 - \beta(\varepsilon_n+\beta^2/4)^{\frac{1}{2}} \qquad (16)$$

The electron energy levels for n= 0,1,2 and 3 were calculated and the results are presented in Table 5.1.

n	E_n
0	0.005eV
1	0.032eV
2	0.068eV
3	0.109eV

Using V_B=0.7V, L=18nm and N_D=3X10^{18}cm^{-3}

Table 5.1.

Calculation of Confined Hole States in The Valence Band.

The quantum hole states in the depletion regions i.e. in the parabolic regions, are calculated below. The potential distribution is defined by equation (4). As v(z) is symmetrical, the case $z>s$ (Figure 5.1) is considered. To simplify analysis, substitute

$$z' = z-s$$

into (4),

$$v(z') = \tfrac{1}{2}Az'^2 \qquad (17)$$

The turning points occur at $z'= z'_j$ and $z'= d-s= L$. At these points

$$v(z') = E_j \qquad (18)$$

E_j is the quantised hole energies. The WKB approximation in this case is given as

$$I = \int_{z'_j}^{L} dz'\ k(z') = (n+3/4)\pi \qquad (19)$$

Equate (17) to (18),

$$z'_j = \left[\frac{2E_j}{A}\right]^{\frac{1}{2}} \qquad (20)$$

Let

$$z' = \left[\frac{A}{2E_j}\right]^{\frac{1}{2}} \psi \qquad (21)$$

Substitute (5), (20) and (21) into (19)

$$I = \left[\frac{2m_h^* E_j}{\hbar^2}\right]^{\frac{1}{2}} \left[\frac{2E_j}{A}\right]^{\frac{1}{2}} \int_1^a d\psi\ (\psi^2-1)^{\frac{1}{2}} \qquad (22)$$

$$\text{where } a = \left[\frac{AL^2}{2E_j}\right]^{\frac{1}{2}} \qquad (23)$$

m_h^* = effective hole mass
= m_{hl}^* for light holes
= m_{hh}^* for heavy holes

Equation (22) is solved by substituting

$$\psi = \cosh\theta$$

which gives

$$I = \left[\frac{4m_h^*}{\hbar^2 A}\right]^{\frac{1}{2}} E_j \{\tfrac{1}{2}\Psi(\Psi^2-1)^{\frac{1}{2}} - \tfrac{1}{2}\ln(\Psi+(\Psi^2-1)^{\frac{1}{2}}\} \qquad (24)$$

$$\text{where } \Psi = \left[\frac{AL^2}{2E_j}\right]^{\frac{1}{2}} \qquad (25)$$

Put $\epsilon_j = E_j/\hbar w_o$, $w_o = (A/m_h^*)$ into (24)

$$I = \epsilon_j\{\Psi'(\Psi'^2-1)^{\frac{1}{2}} - \ln(\Psi'+(\Psi'^2-1)^{\frac{1}{2}}\} = (n+3/4)\pi \qquad (26)$$

where

$\Psi' = (\nu_B/\epsilon_j)$
$\nu_B = V_B/\hbar w_o$

Equation (27) is finally solved numerically for light ($\nu_B = 26$) and heavy ($\nu_B = 11$) holes. The results (j= 0,1,2 and3) are presented in Table 5.2 below.

j	E_j Light Holes	E_j Heavy Holes
0	0.249eV	0.151eV
1	0.351eV	0.234eV
2	0.409eV	0.288eV
3	0.449eV	0.328eV

E_j measured from the top of the valence band at z=L,
$N_D = 3X10^{18}cm^{-3}$ and
L = 18nm

Table 5.2

The confined electron and hole states in the GaAs membrane is shown schematically in Figure 5.2.

5.3 Experimental

The experiments described below were performed at the Physics Department of Nottingham University. It is not intended here to provide in depth descriptions of the experimental apparatus nor detailed principles of the experimental methods. These are only treated briefly but interested readers may refer to the thesis of Halliday (5.4) for details .

5.3.1 Basic Principles of Photo–absorption and Photoconductivity Measurements

The Excitation Process (5.5)

In bulk GaAs, a direct transition of an electron from the valence band to the conduction band may take place by absorbing a photon whose energy hf satisfies the condition

$$hf > E_G$$

where h is Planck's constant, f the photon wave frequency and E_G the fundamental energy gap of the semiconductor. In the case of the GaAs membrane, a photon may similarly excite a valence electron to the nth energy level if $hf > E_G + \Delta E_n$, where ΔE_n is the energy gap between the $n=0$ and the nth states. Some of the possible transitions are indicated in Figure 5.2. A photon which lacks the minimum energy required for the transition process is transmitted without being absorbed. The band structure of a semiconductor may therefore be determined by measuring the transmission of light through the semiconductor as a function of wavelength. Energy gaps are established by noting the wavelength at which absorption commences

(i.e. reduction in transmitted light intensity). The ratio of the transmitted light intensity through a semiconductor, I_o, to incident light intensity, I_i, is given by the Beer– Lambert law as

$$I_o/I_i = \exp(-\alpha t)$$

where α and t are the absorption coefficient and thickness of the semiconductor respectively. The absorption coefficient is given as

$$\alpha = \text{constant} \times (hf - E_G)^{\frac{1}{2}}$$

for allowed direct transitions (5.5).

In elevating a valence electron to a higher enery level, a hole is created in the valence band. Thus, continuous illumination of the semiconductor results in the generation of electron– hole pairs provided the photon energies $hf > E_G$, otherwise the photons are transmitted. As a consequence, there may be a net increase in the steady state electron and hole concentrations over the quiescent concentrations in the dark. The gap between two energy levels may therefore be determined by noting the photon energy at which increased photo– current is detected (5.6).

Exciton Formation (5.7)

The Coulomb interaction between an electron and a hole may lead to the formation of exciton states. A quantum of energy hf less than E_G may be absorbed generating an exciton rather than a electron– hole pair according to the following equation:

$$hf = E_G - E_{EXC} \qquad (27)$$

where E_{EXC} is the exciton binding energy and is given by

$$E_{EXC} = \frac{-m_r^* q^4}{2h^2 \epsilon^2} \frac{1}{n^2} \qquad (28)$$

where m_r^* is the reduced mass defined as

$$1/m_r^* = 1/m_e^* + 1/m_h^*, \qquad (29)$$

and n= 0,1,2,3,....

An excitonic transition is illustrated in Figure 5.3. In this case an absorption line spectrum similar to the hydrogen series appears at the long wavelength side of the fundamental absorption edge.

5.3.2 Photo– absorption Measurement

5.3.2.1 Method

50 nm thick GaAs membranes were fabricated by selective etching using the method described in chapter 3 (Section 3.2). The samples were mounted on special copper holders which facilitated transmission spectroscopy.

The light source used for the optical absorption experiment was a 150 watt tungsten lamp. The light was dispersed by a 0.75 m SPEX spectrometer and was then focussed on the membrane. Using a very

high power lens an image of the membrane was produced about 1.5 m away. On this image the membrane appeared about $3mm^2$. This image was passed through a pinhole on the front of a detector. This ensured that only light transmitted through the membrane was incident on the detector. The detector was a Ge detector made by North Coast (model E0817L). A series of Schott glass filters (long wavelength pass) were used to remove second order effects from the spectrometer. The samples were cooled in an Oxford Instrument gas flow cryostat (model CF1204). The light incident on the spectrometer was chopped and a phase sensitive detector used to detect the signal. The transmission was measured with and without the membrane and the ratio of the two spectra gave the membrane absorption.

5.3.2.2 Results

The absorption spectrum (presented as the ratio of transmitted light intensity to incident light intensity) of a 50 nm thick GaAs membrane in the range 1.40 to 1.80 eV at 300K and 5K are shown in Figures 5.4.a– b.

The absorption edge at 300K was broad due to the thermal motion of the carriers but was estimated to be at 1.45 eV. In the 5K spectrum, a sharp edge was resolved at 1.51 eV with absorption coefficient of 9100 cm^{-1}. This absorption coefficient is in agreement with that measured by Sturge (5.8) for intrinsic GaAs which was 9400 ± 400 cm^{-1}.

Three interesting observations can be made from the 5K absorption spectrum. Firstly, the energy of the absorption edge of the $n^+ - GaAs$ membrane is similar to bulk *intrinsic* GaAs. The calculated edge for intrinsic GaAs at 5K was 1.52eV using the empirical formula

due to Thurmond (5.9) (equation 31 in Section 5.3.2.2). Secondly, the absorption was seen to increase well below the main absorption edge i.e from 1.4 eV. Thirdly, neither an excitonic peak nor absorption due to discrete states were resolved in the spectrum.

Figures 5.5.a and 5.5.b show the absorption spectra in the range 2.4 to 3.4 eV at 290 and 4K respectively. Both spectra show a broad absorption edge which was estimated to be at 2.7 eV. This absorption was due to the transition across the gap at the L− valley (Figure 5.6). The absorption coefficient was estimated to be 2 X $10^5 cm^{-1}$.

5.3.2.3 Discussion

Absorption Spectrum in the Range 1.40 to 1.80 eV

The membrane may be viewed as consisting of a centre layer with absorption coeffiecient α_1 sandwiched between two depletion layers, both with absorption coefficient α_2.

The path of a photon through the GaAs membrane is represented schematically in Figure 5.7a. If the length of the centre and depletion layers are l_1 and l_2 (l_2= 2L) respectively then the transmission of the photon may be expressed as

$$T = \exp-(\alpha_1 l_1 + \alpha_2 l_2) \qquad (30)$$

$T = I_o/I_i$ (transmitted light intensity/incident light intensity)

The features in the 5K spectrum are interpreted in terms of absorption by the different layers.

In bulk n^+-GaAs with $3X10^{18}$ cm^{-3} doping density, Bohr radii of the donor electrons overlap so much that the donor electron delocalise and the system is metallic (the condition for this to occur is given by the Mott criterion $N_D^{1/3}a^* > 1/4$ where a^* is the Bohr radius defined as $4\pi\epsilon\hbar^2/m^*q^2$). The Fermi level in such a system is about 110meV above the conduction band. One effect of this degenerate doping is to shift the absorption edge to a higher energy, the so called Moss–Burnstein shift (5.10). In this case, a shift of 110 meV may be expected, as illustrated in Figure 5.7b. This is because all the states up to the Fermi level are filled. However, no such shift was observed in the GaAs membrane.

In the centre layer of the membrane, the Fermi level was within the conduction band (Figure 5.7c) and hence the transitions here were subjected to the Moss–Burnstein shift. However, the conduction band was bent above the Fermi level in the depletion layers due to the effects of surface states. The main absorption edge in these regions would therefore correspond to E_G if the conduction and valence bands are assumed to be continuous. This assumption is valid as the absorption profile was smooth. If the states were quantised, the profile should reveal a series of steps corresponding to the transitions between discrete energy levels. The reason why these were not resolved may be due to the large number of possible transitions between the discrete energy levels which smooth out the steps. This will be discussed later. The fact that the position of the absorption edge was similar to that for intrinsic GaAs suggests that the absorption occured mainly in the depletion layers. This may be expected from equation (30) as $l_2 > l_1$ (i.e. 36 nm compared with

14 nm).

Absorption At Energies Below the Main Absorption Edge

The increase in absorption below the main absorption edge, at between 1.4 and 1.5 eV, was attributed to the combined effects of high doping density and surface fields.

One would expect perturbation of the bands by the donor states to result in the formation of tails of states which extended the band edges into the forbidden gap as shown in Figure 5.8 (5.11). The transition gap (between the band tails) was reduced as a consequence. The band–tailing is expected to be less pronounced in the centre layer due to the high carrier density which screened the fields produced by the donor states.

Carriers in the depletion layers should be under the influence of a strong surface electric field. This field (obtained by differentiating equation 4) had a maximum value of over 700 kV/cm at the surface, dropping to zero at the edges of the depletion layers. The presence of the surface fields resulted in quantum penetration of the discrete energy levels into the forbidden gap. This is known as the Franz–Keldysh effect (5.12). The extent of the penetration of the wavefunction into the forbidden gap δ is given by

$$\delta = \left[\frac{\hbar^2}{2m^* qF}\right]^{1/3}$$

where F = the electric field strength
and $m^* = m_e^*$ for electron states
$= m_h^*$ for hole states.

The amount of penetration of the discrete levels into the

forbidden gap is shown graphically in Figure 5.9a. δ was obtained by assuming a uniform field of 350 kV/cm (which is the average field in the depletion layers). Due to the asymmetry of the potential profile in the depletion layers, there is unlikely to be a selection rule on the transitions between the energy levels (5.13). Therefore, an electron from a discrete hole level could be raised to any of the overlapping electron energy levels. It can be seen from Figure 5.9b that some of the transitions involved the absorption of photons with energies less that E_G. These transitions may account for the increased absorption below the band edge observed in the 5K optical absorption spectrum.

Excitons and Quantum Confined States

The absence of an excitonic peak in the absorption spectrum is attributed to the effects of screening in the centre layer and the surface fields in the depletion layers. In the centre layer, electron–electron coulombic repulsion reduces the range over which the attractive coulombic interaction required for forming excitons could occur. Excitons were therefore unlikely to form in this layer. Excitons formed in the depletion layers were expected to be short lived due to the ionising effect of the surface fields. Consequently, the absorption peak due to these excitons was likely to have been broadened out.

The absence of absorption edges corresponding to the confined states may be explained as follows. In the depletion layers, the large number of possible transitions from each level results in aperiodic, closely spaced steps in the absorption. Combining transitions from all levels results in a near continuous absorption profile. This is illustrated in Figure 5.9c. The absorption edges due to the confined electron states in the centre layer were likely to be masked by this depletion

layer absorption.

L– L Band Transition

The increase in absorption between 2.4 and 2.9 eV in the 4.2K and 290K spectra was due to L– L interband transition. It is difficult to pin– point the absorption edge as the absorption was broad even at 4.2K. The edge was estimated to be at 2.7 eV at both temperatures. The absorption coefficient was about $2X10^5$ cm^{-1} at this point. These figures are the first reported for single crystal GaAs obtained by transmission. (Transmission spectroscopy is rarely used for the study of transitions above the smallest GaAs bandgap. This is because of the very high absorption at higher energies and the difficulty involved in preparing good quality thin substrates by standard polishing techniques.)

It is interesting to note that the absorption edge differed from that reported by others. Using the transmission method, Cardona and Harbeke (5.14) measured the edge at 2.97 eV at room temperature for a 0.24 um thick polycrystalline GaAs film obtained by evaporation. The band edge had also been measured by reflectivity at 2.896 eV and at 2.94 eV (5.14). The reason for the discrepancy seen in the GaAs membrane is not well understood.

5.3.3 Photoconductivity Measurements

5.3.3.1 Method

Photoconductivity measurements were performed on ungated membrane MESFETs at temperatures between 4.2K and 300K. The

samples were prepared using the alternative membrane device fabrication technique described in Section 4.4 of Chapter 4.

The light source used was the same as for the absorption experiment. The light was focussed on the sample through which a constant current of 10 μA was passed through two ohmic contacts on each membrane. The incident light was chopped by an optical chopper and the modulated photo–signal was detected by a phase sensitive detector.

5.3.3.2 Results

Photoconductivity spectra obtained at 4.2, 20, 30, 50 and 300K are presented in Figures 5.10.a–e. Excitonic peaks were resolved at 4.2, 20, 30 and 50K but the sharpest peak was at 50K. The peaks became broader and less pronounced below 50K. Oscillations were observed in all the spectra except at 300K. The oscillations were most pronounced between 30 and 60K. The drop in photo–current in the spectra at energies above 2 eV was due to the response of the system (i.e. the tungsten lamp and the spectrometer grating). The photoconductivity results are summarised in Table 5.3. The photon energies at which the first three oscillatory peaks occured are shown in the table.

Temp. K	Exciton Peak (eV)	Measured Absorption Edge (eV)	Calculated Absorption Edge (eV)	Oscillation Peaks (eV) 1	2	3
300		1.41	1.42			
290		1.41	1.43	1.62	1.77	1.89
70		1.52	1.51	1.70	1.82	1.97
50	1.50	1.51*	1.51	1.69	1.83	1.95
30	1.50	1.51*	1.52	1.68	1.82	1.95
20	1.51	1.52*	1.52	1.70	1.82	1.95
4.2	1.51	1.52*	1.52	1.70	1.82	1.96

* denotes band gap E_G was calculated from

$$E_G = hf_{peak} + E_{EXC}$$

E_{EXC} was calculated from equations (29) and (30) and hf_{peak} is the photon energy at which the excitonic peak was measured (this method was used because the excitonic peaks in the photoconductivity spectra are well defined compared with the main absorption edges)

Table 5.3

The theoretical band gaps in Table 5.3 were calculated using the empirical formula for bulk intrinsic GaAs due to Thurmond

$$E_G = 1.519 - 5.405X10^{-4}/(T+204)\ eV \qquad (31)$$

where E_G and T are the band gap and the temperature in Kelvin respectively.

5.3.3.3 Discussion

It can be seen from Table 5.3 that the main absorption edges at various temperatures agreed with that for bulk intrinsic GaAs. The reasons have been discussed earlier.

Excitonic Peaks

The excitonic peaks obseved in the photoconductivity spectra were probably due to dissociation of excitons formed in the depletion regions (in the absorption experiment, the ionisation of an exciton resulted in a broad peak which was not resolved whereas here the ionisation resulted in a sharp increase in photocurrent). No excitonic peak was observed for the spectra obtained at above 70K probably because the excitonic life−time was either too short to be resolved or the peak was masked by thermally excited photocurrent. It is not well understood why the excitonic peaks became less pronounced at temperatures below 30K.

Oscillations

The oscillations observed in the photoconductivity spectra cannot be due to interference effects as the photon wavelengths (>700 nm) were very much longer than the membrane thickness. For constructive interference, the wavelength of the photons has to be 340 nm or shorter, assuming a membrane thickness of 50 nm (the condition for constructive interference is given by $t=(2m+1)\lambda/2\mathbf{n}$, $t=$ membrane thickness, $\lambda=$ wavelength, m an integer and **n** the refractive index of GaAs). Some possible explanations for the oscillations are considered below.

Quantum Confinement

As discussed earlier, the large number of possible transitions between the confined states in the depletion layers was thought to blur

out the absorption edges associated with these states. In the centre layer, the average gap between the electron energy levels had been calculated to be about 30 meV (Section 5.2). But the average period of the oscillation was more than 100 meV. Maximum separations between the quantised electron states are obtained if the potential well was parabolic i.e. if the depletion layers equalled the membrane thickness (2L = membrane thickness). The separation between the quantised electron states in the parabolic well ΔE would be

$$\Delta E = \hbar w_o = 50.8\text{meV}$$

($w_o = A/m_e^*$)

which is still smaller than the period of the observed oscillations.

Transverse Bands

Next, the energy gap resulting from transitions from the light hole band to the quantised electron energies in the centre of the membrane is considered. The transitions under consideration are illustrated in Figure 5.11.

The wave vector of the nth energy band, k_n, is given by

$$E_F - E_n = \frac{\hbar^2 k_n^2}{2m_e^*}$$

where E_F and m_e^* are the Fermi energy level and effective electron mass respectively. The gap between the light and heavy hole bands and E_n is

$$\Delta E = \frac{\hbar^2 k_n^2}{2m_h^*} = \frac{m_e^*}{m_h^*} \times (E_F - E_n)$$

$m_h^* = m_{h1}^*$ for transitions from the light hole band

$m_h^* = m_{hh}^*$ for transitions from the heavy hole band

Because of the symmetry of the system, the transitions are subjected to selection rules. Only transitions from the valence band to E_0 and E_2 were allowed (5.13). The energy gap resulting from the transition from the light hole band is considered as these resulted in a larger separation due to the curvature of the band. In this case, ΔE due to E_0 and E_2 transitions were calculated to be 90meV and 39meV respectively (assuming $E_F = 110$meV), giving a difference of 51meV. Therefore, these transitions could not be responsible for the observed oscillations.

5.4 Conclusions

Photo–absorption experiments in the energy range 1.45 to 3.4 eV on a 50 nm thick GaAs membrane were presented. The results do not show conclusive evidence of the existence of states due to quantum confinement.

Using the membrane, it was possible to observe the band edge due to the L–L band transition. The absorption edge at 290 and 4.2K was estimated to be at 2.7 eV and the absorption coefficient was estimated to be 2×10^5 cm^{-1}. However, the measured band edge did not agree with published results. The reason for this is not clear.

Photocurrent oscillations were observed in the photoconductivity spectra measured at temperatures between 290 and 4 K. The oscillations could not be attributed to confined quantum states as the period of the oscillations were two to three times larger than the calculated energy gaps. The cause of the photocurrent peaks is not

clear.

In order to probe the confined states of the membrane, absoption in the infra-red range should be carried out. Transitions between the the discrete electron states (Figure 5.12) may then be observed. This does not involve transitions from the quantised hole levels which were thought to smooth out the absorption due to the confined states. Using infra-red absorption, direct interconduction band transition between confined states in a square well have been observed by West and Eglash (5.15).

Chapter 5 References

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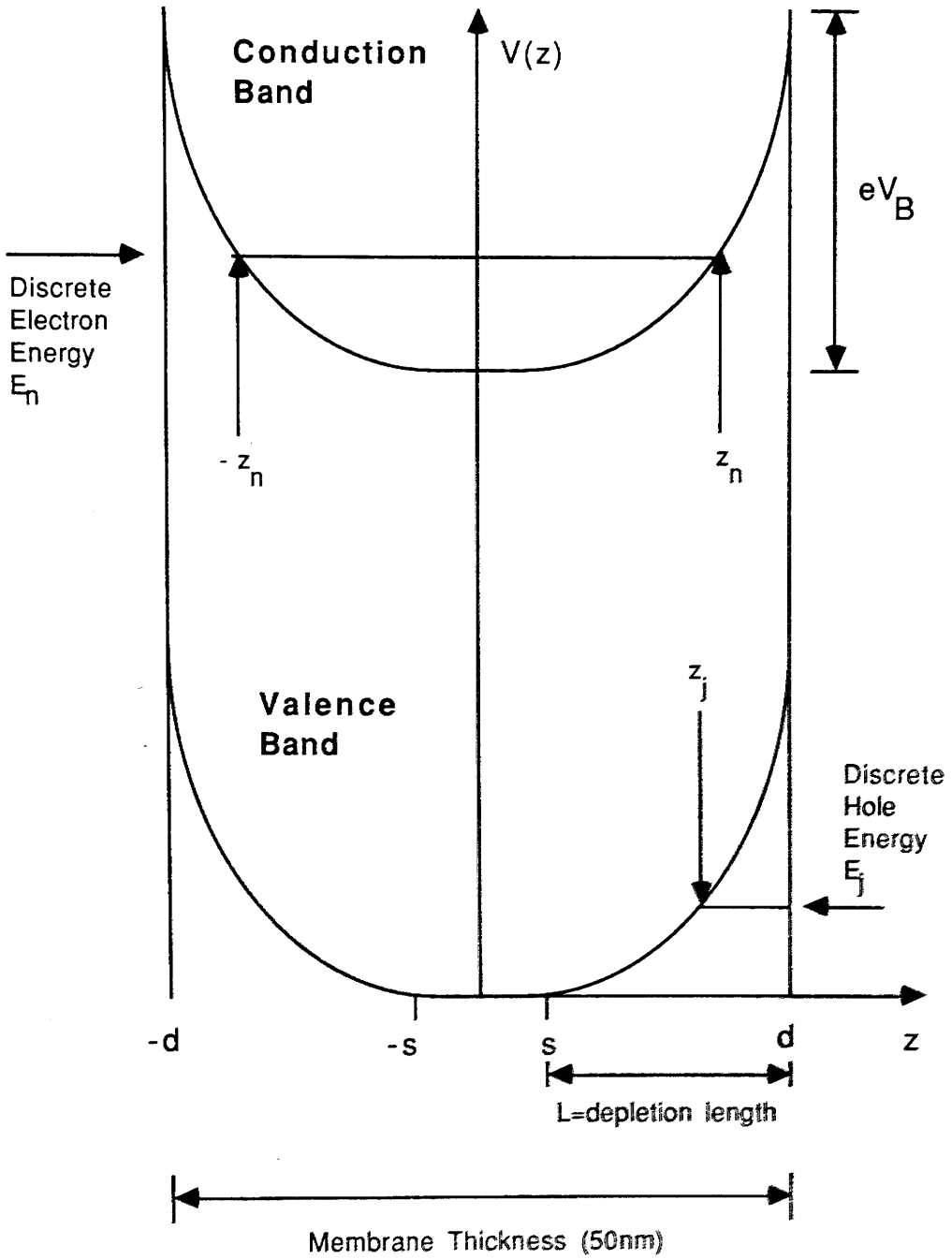


Figure 5.1 Potential Distribution in a 50nm Thick GaAs Membrane

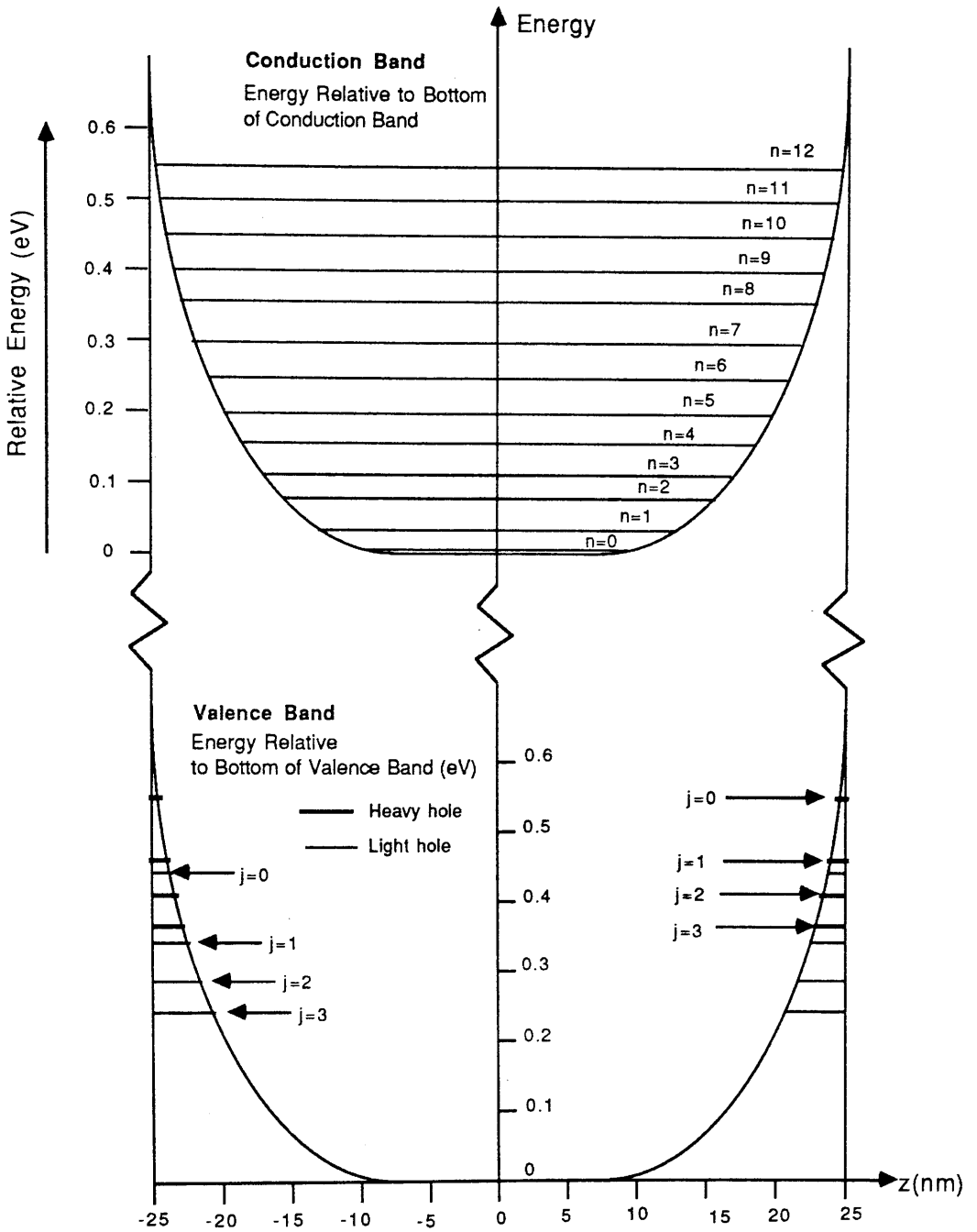


Figure 5.2 Confined States in 50nm thick GaAs Membrane.

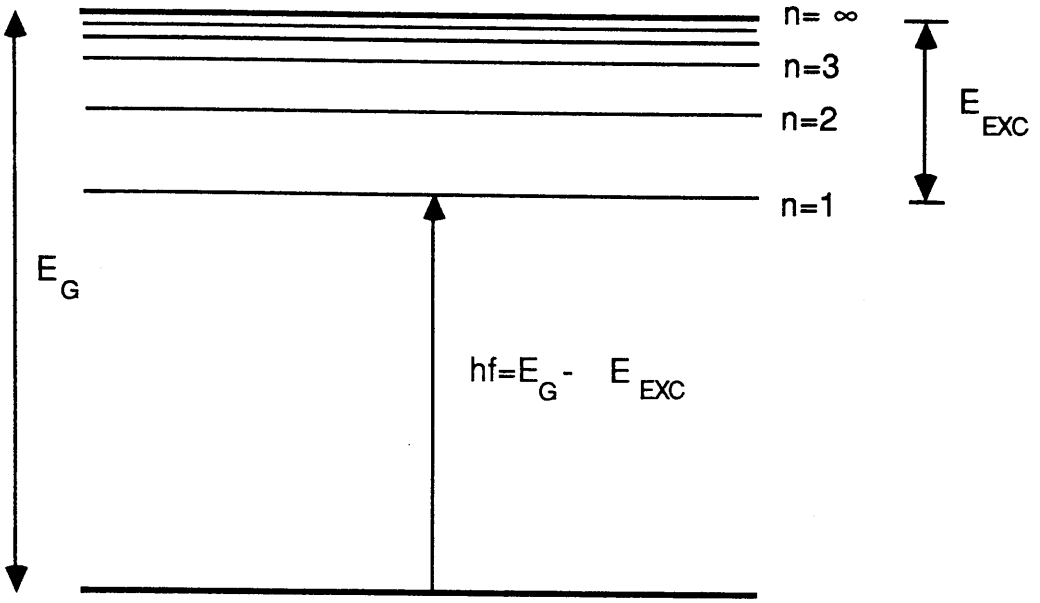


Figure 5.3 Excitonic Energy Levels and Transition

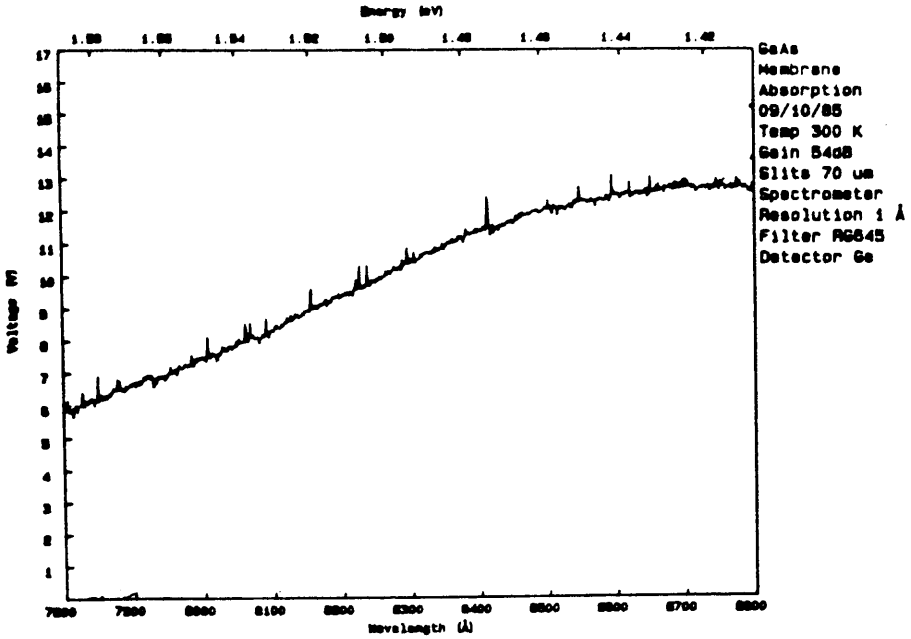


Figure 5.4a

Absorption Spectrum in the range 1.4 to 2.8eV, T=300K

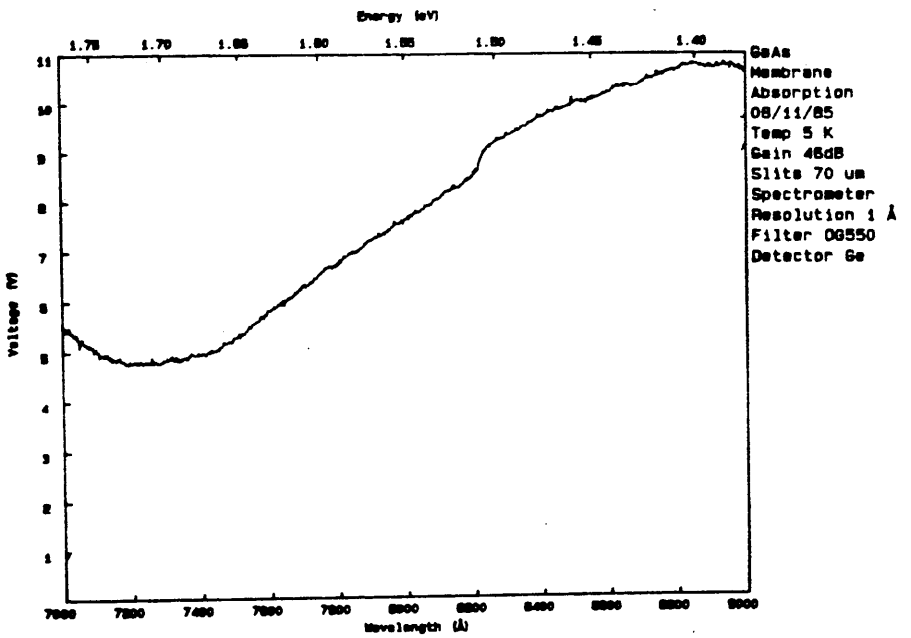


Figure 5.4b

Absorption Spectrum in the range 1.4 to 2.8 eV, T=5K

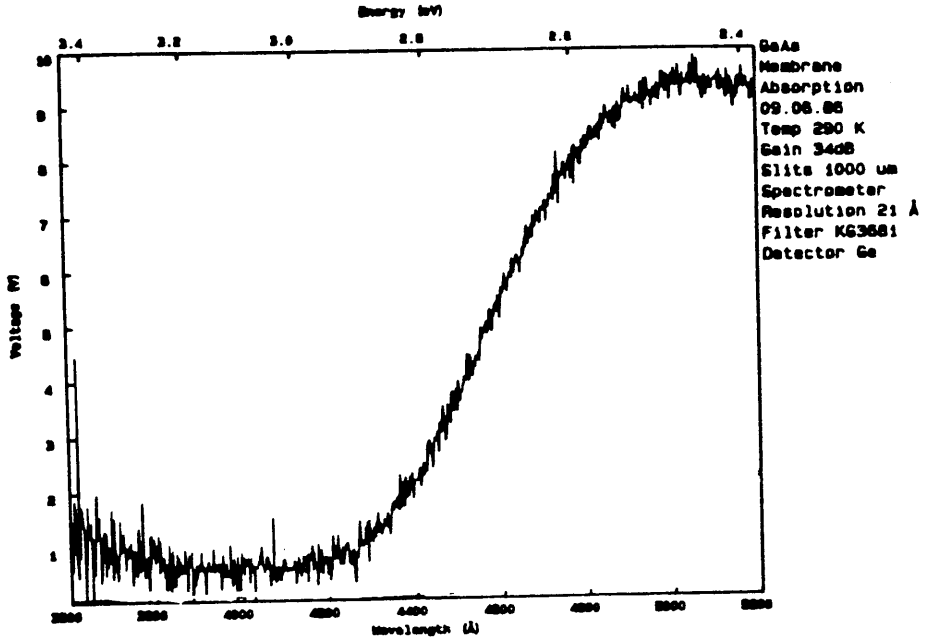


Figure 5.5a

Absorption Spectrum in the range 2.4 to 3.4eV, T=300K

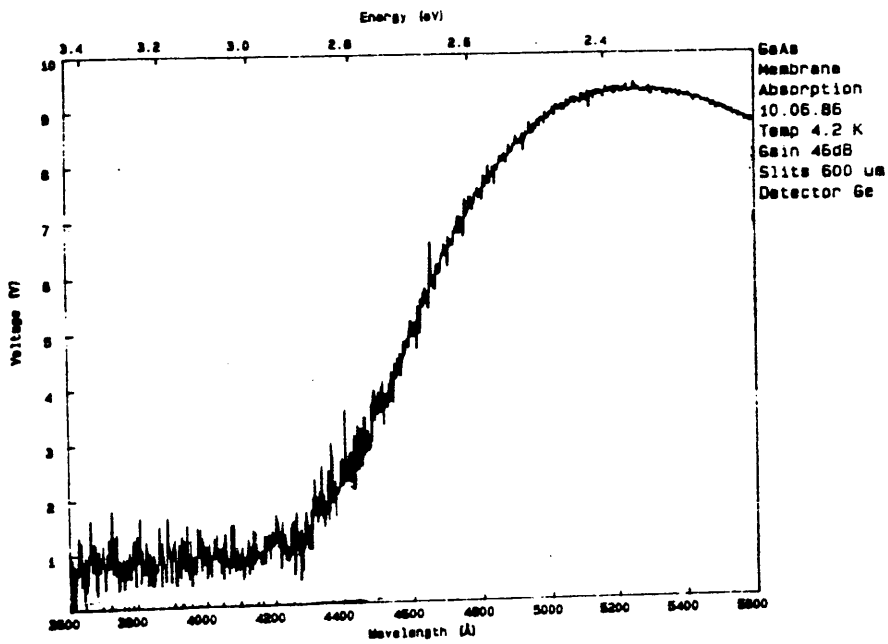


Figure 5.5b

Absorption Spectrum in the range 2.4 to 3.4 eV, T=4K

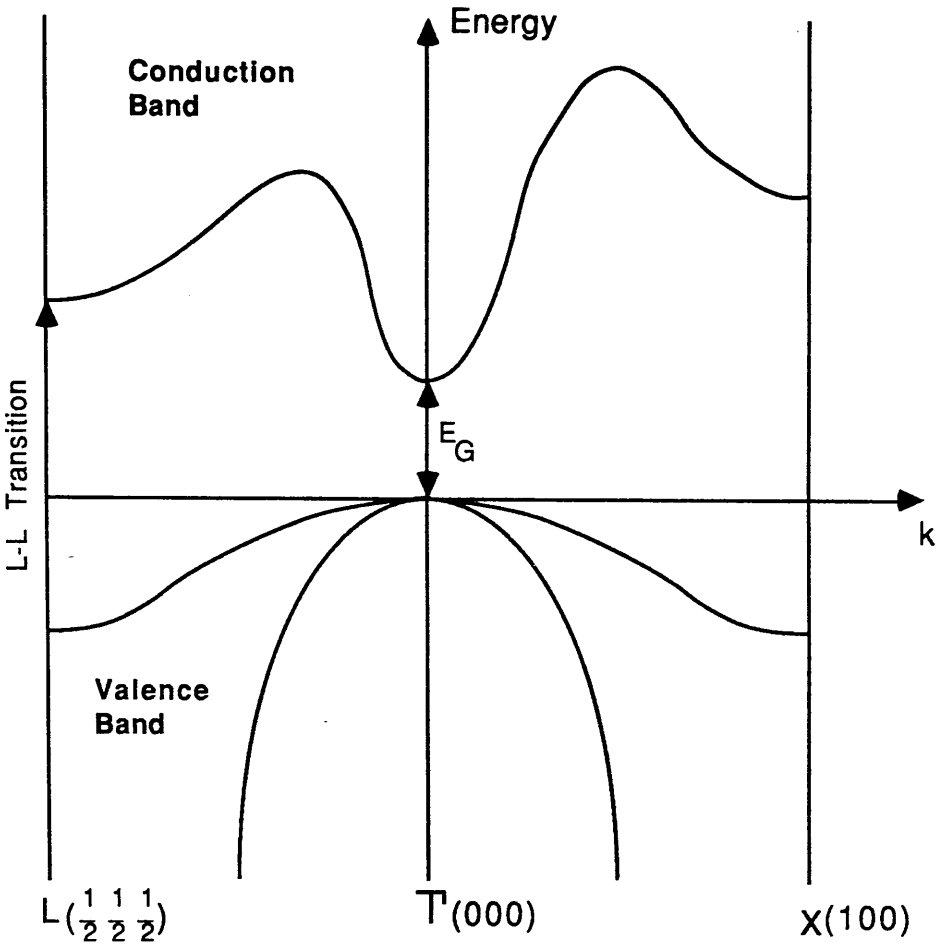


Figure 5.6

Schematic Representation of the Band Structure of GaAs. (reference 5.16).

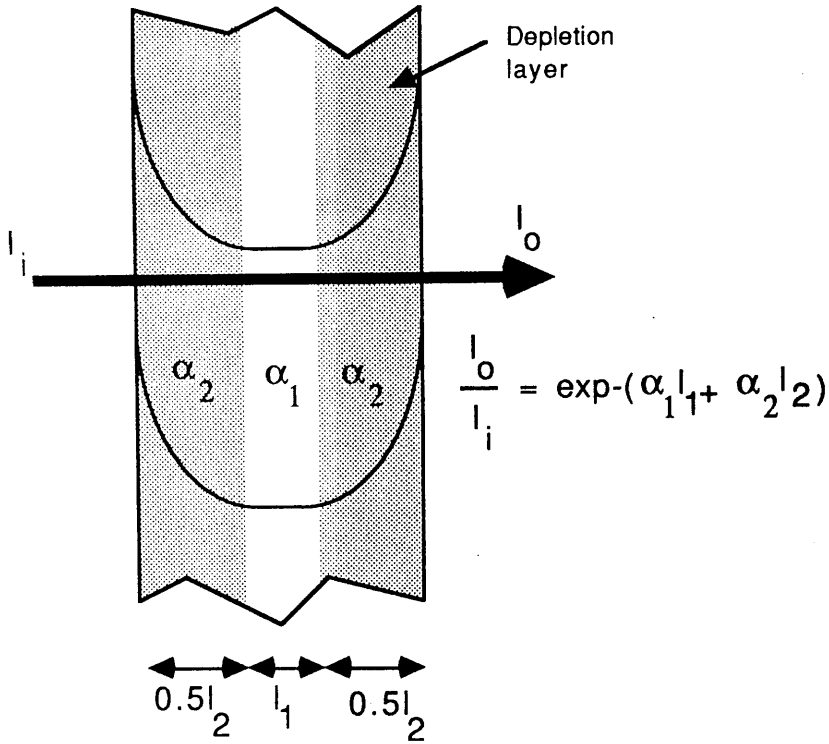


Figure 5.7a

The membrane may be thought of as consisting of a centre layer sandwiched between two depletion layers.

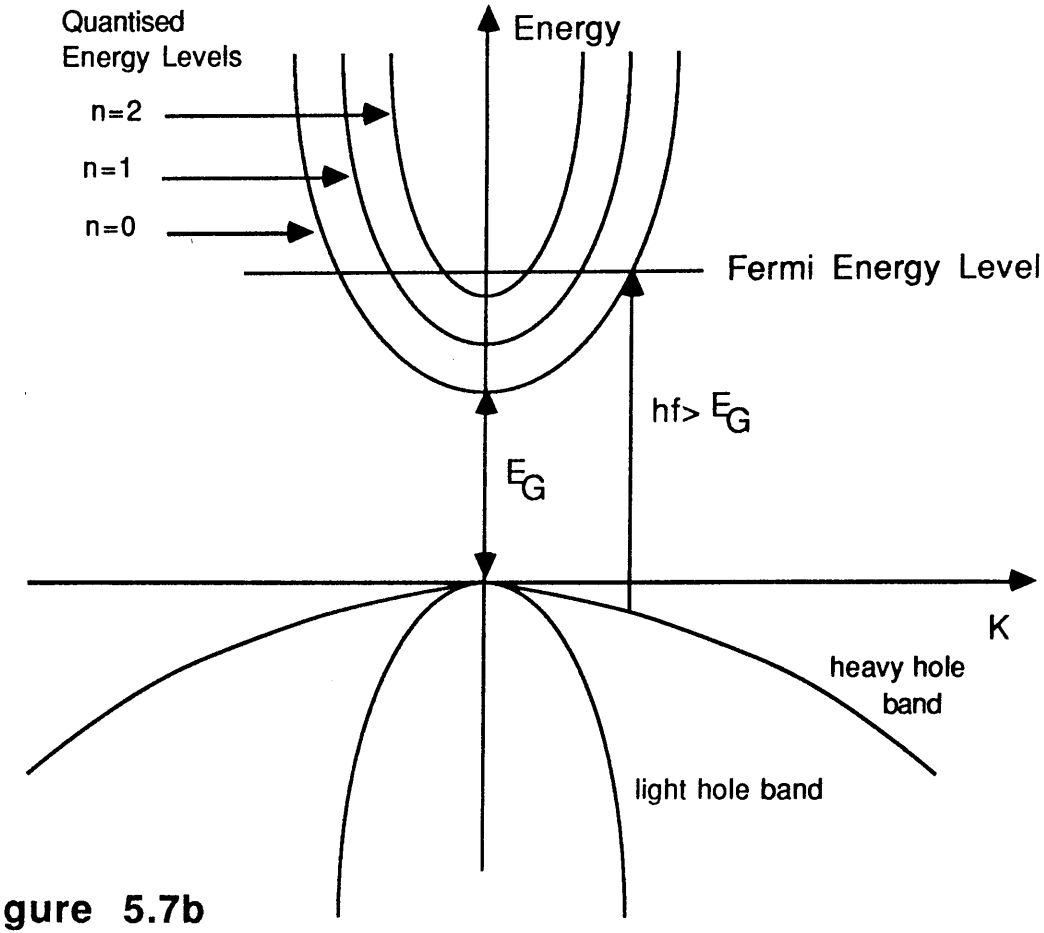


Figure 5.7b

E-K diagram showing the Moss-Burnstein shift. All states up to the Fermi level are filled up. Consequently, transitions can only take place at $k \neq 0$. The minimum energies required for these transitions are greater than E_G due to the curvature of the bands.

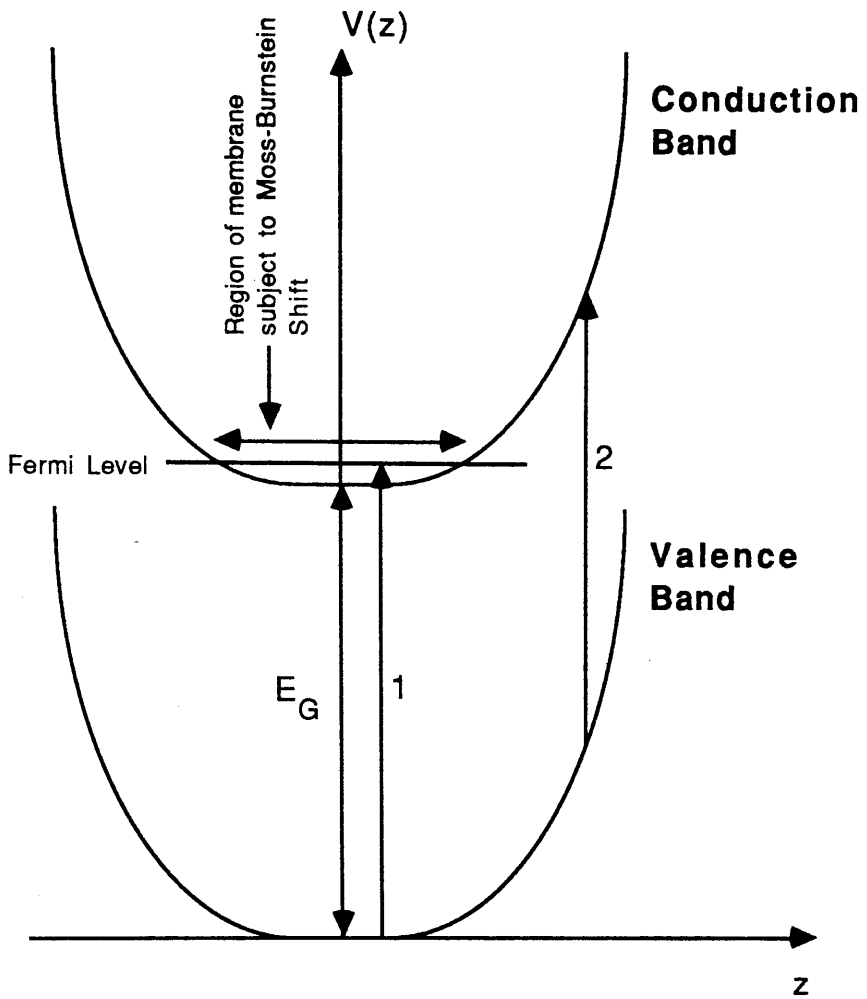


Figure 5.7c

Illustration indicating membrane region subject to Moss-Burnstein Shift. In this region, an excitation process requires an energy greater than the band gap (transition 1). In the depletion layers, the conduction band bends above the Fermi energy level. Here, the minimum energy for a transition is E_G (transition 2).

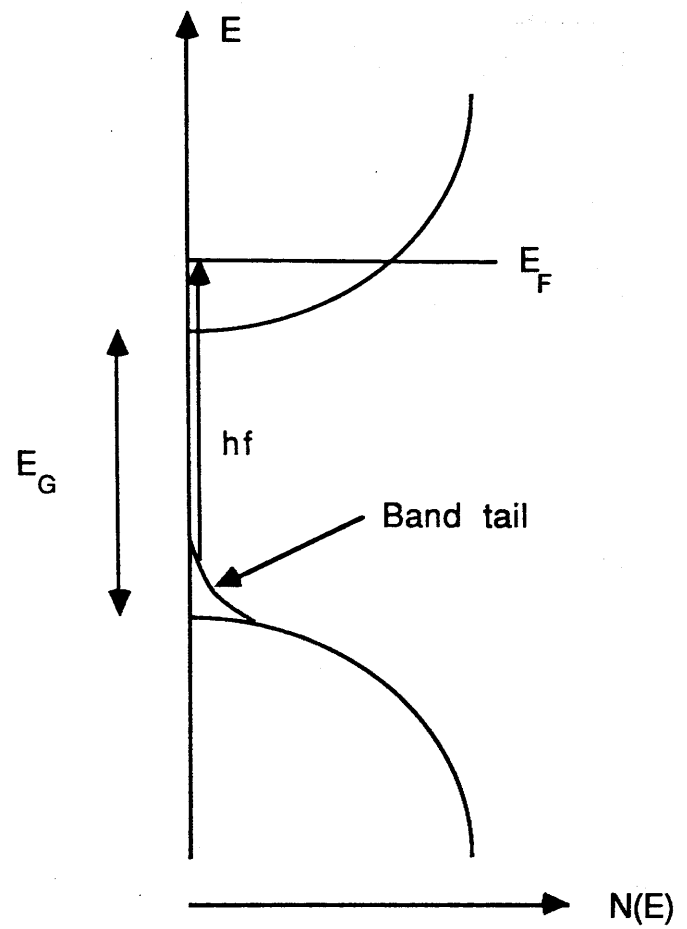


Figure 5.8 Band Tailing

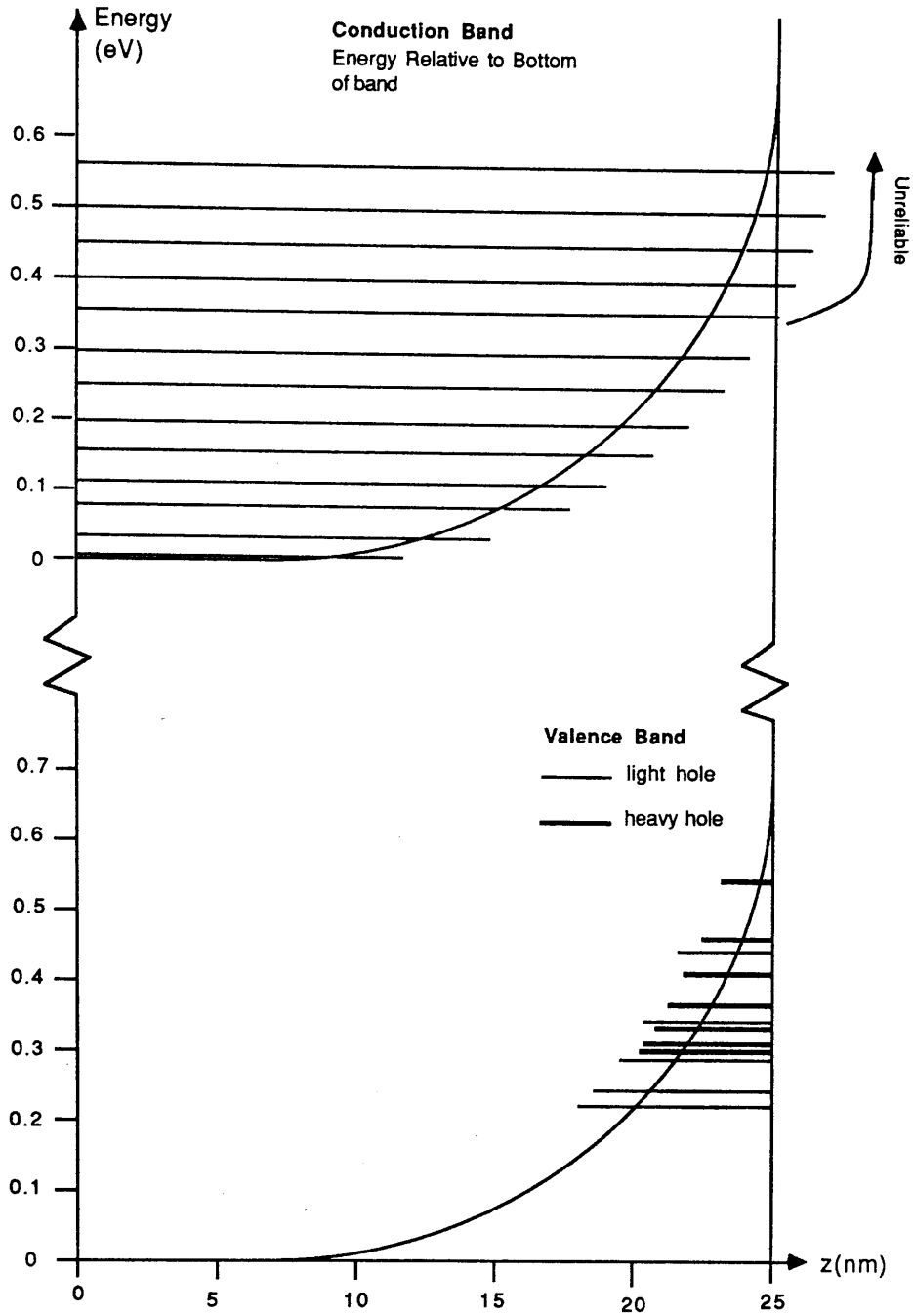


Figure 5.9a

Graph showing penetration of discrete energy levels into forbidden zone due to Franz-Keldysh effect.

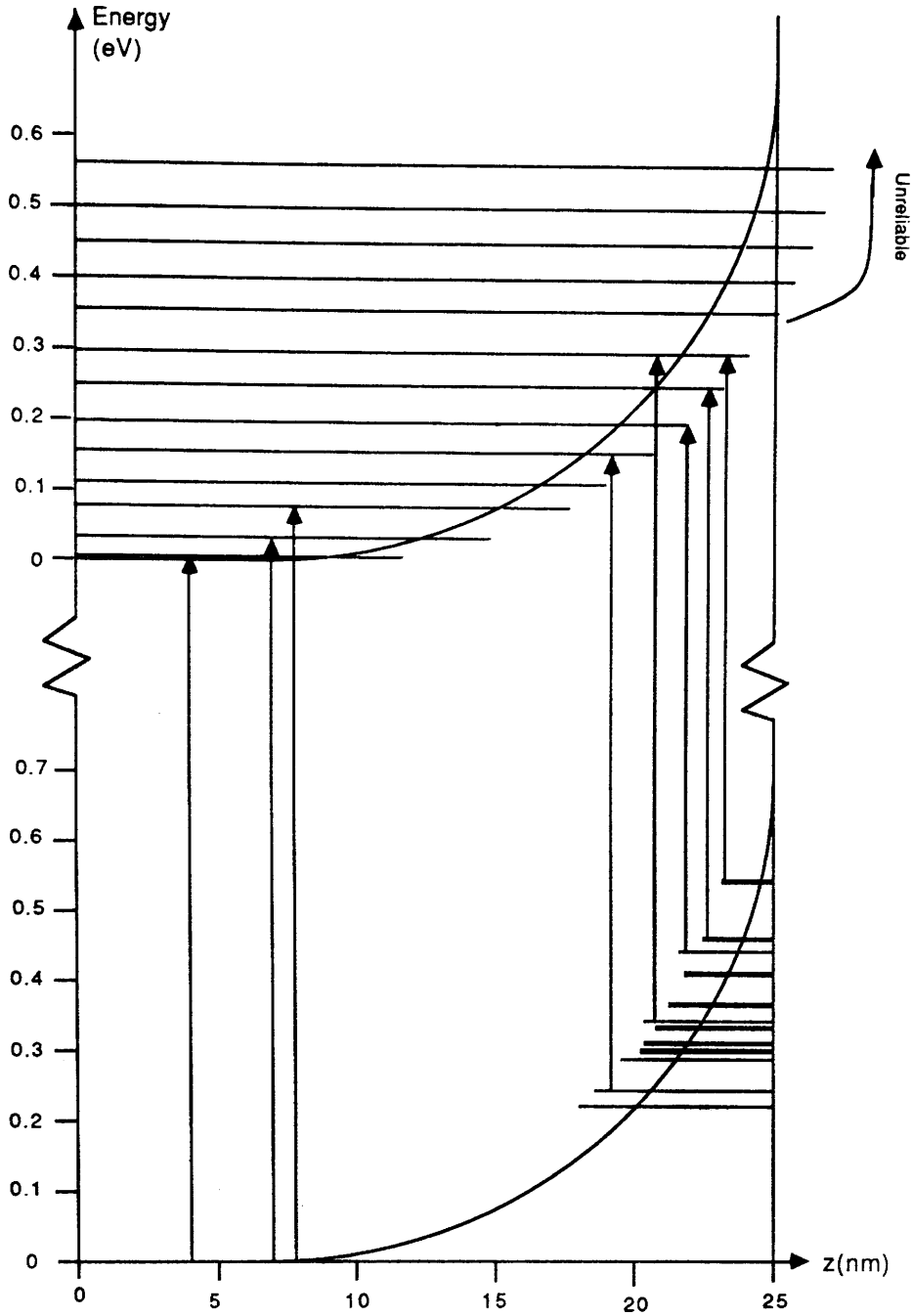


Figure 5.9b

Some of the possible transitions between discrete states are shown. In the depletion region, penetration of quantum states into the forbidden gap results in transitions involving energies smaller than the band-gap.

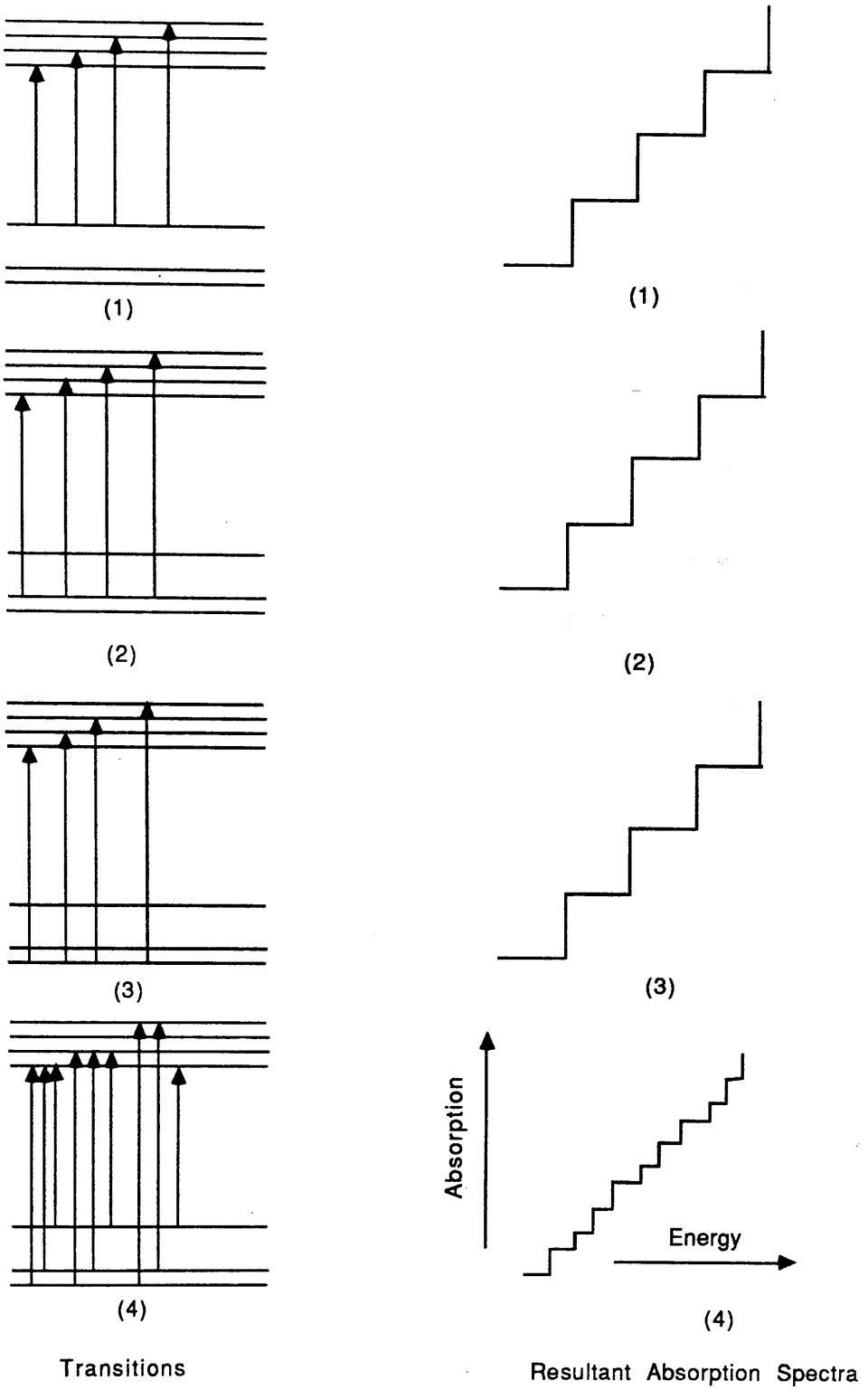
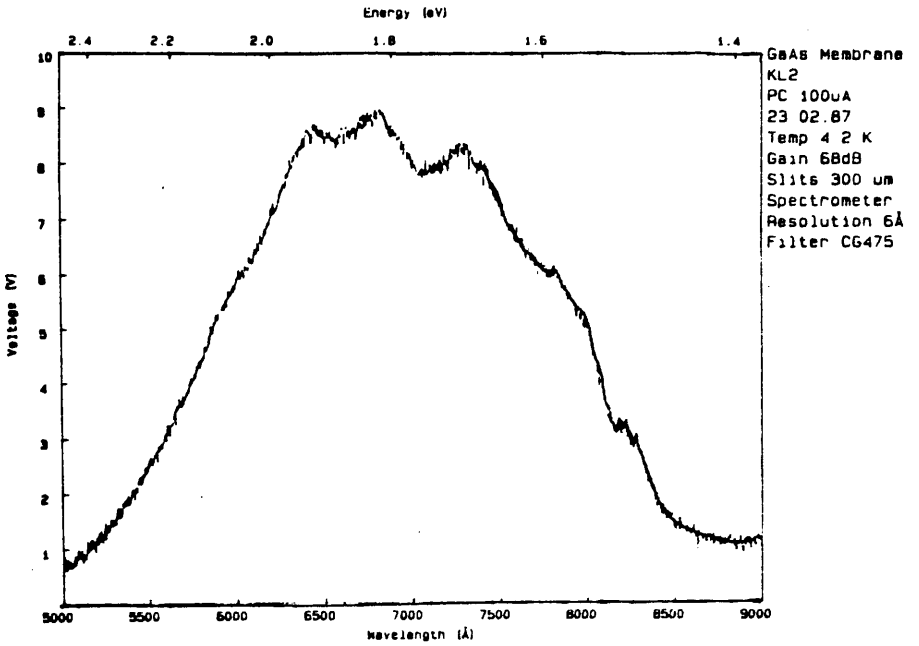
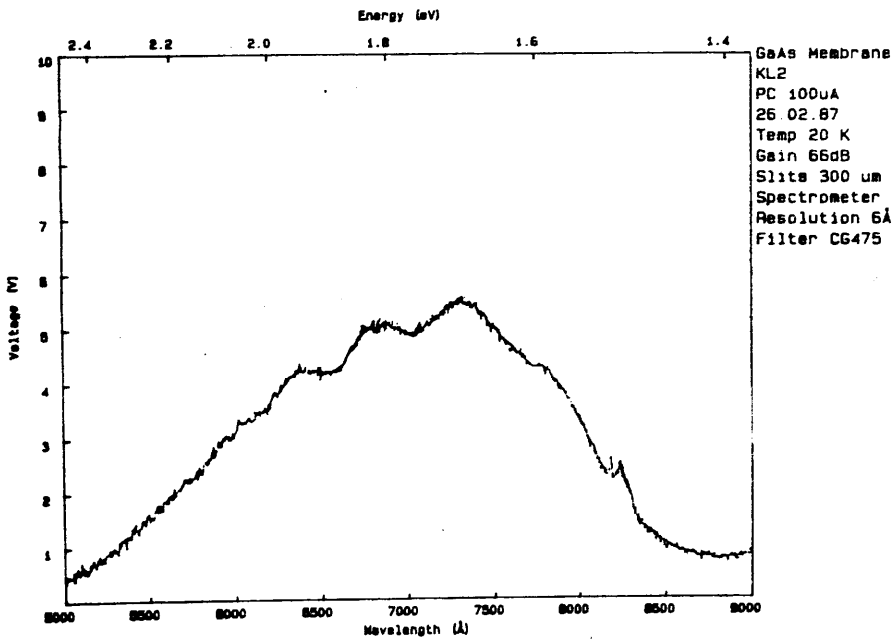


Figure 5.9c

Schematic representations of transitions between discrete levels and resultant absorption spectra. Transitions from a discrete valence band to all electron energy levels result in a step profile(1,2 &3). However, combining all possible transitions (from all valence levels to all conduction levels -(4)) results in closely spaced (in energy) steps.



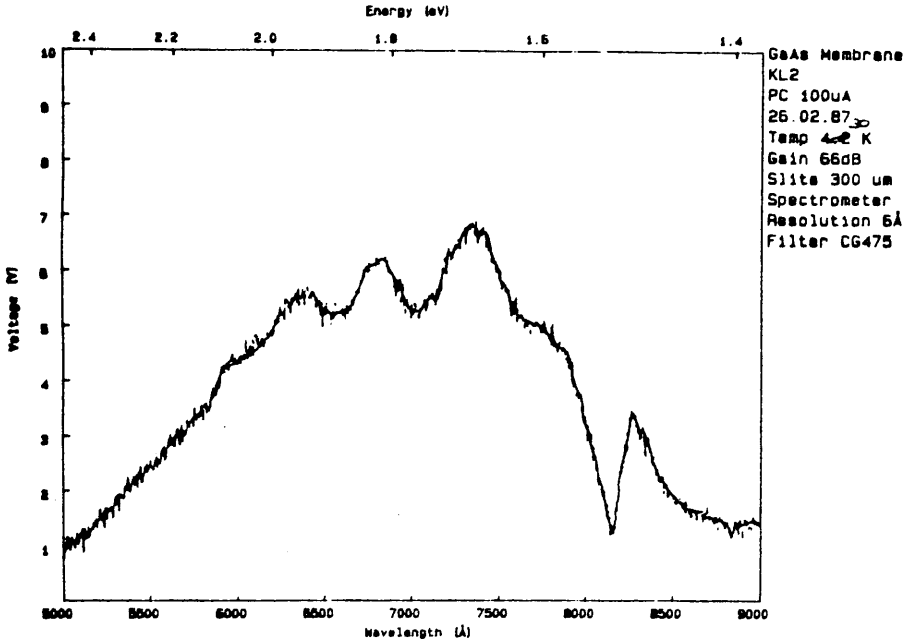
(a) T=4.2K



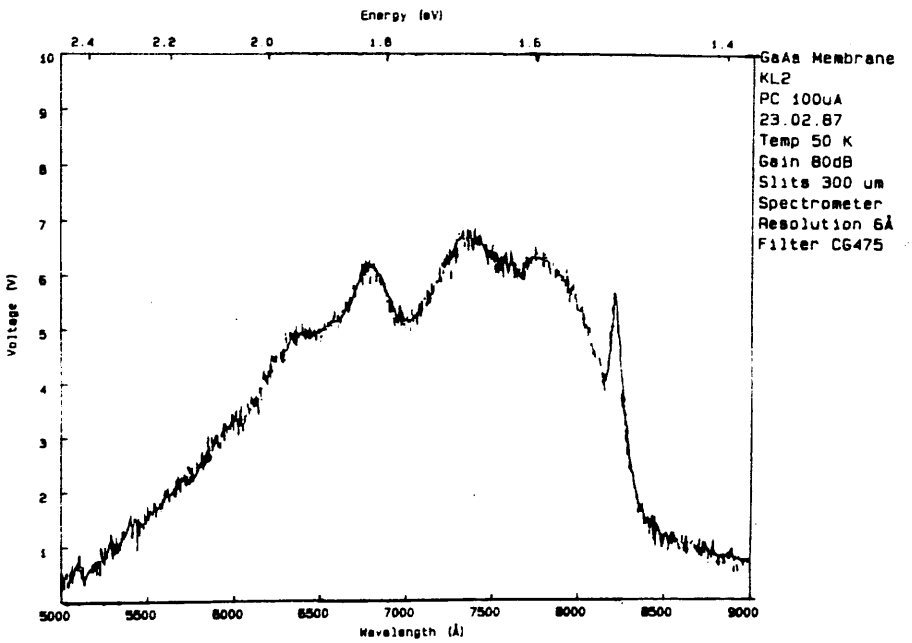
(b) T=20K

Figure 5.10

Photoconductivity Spectra



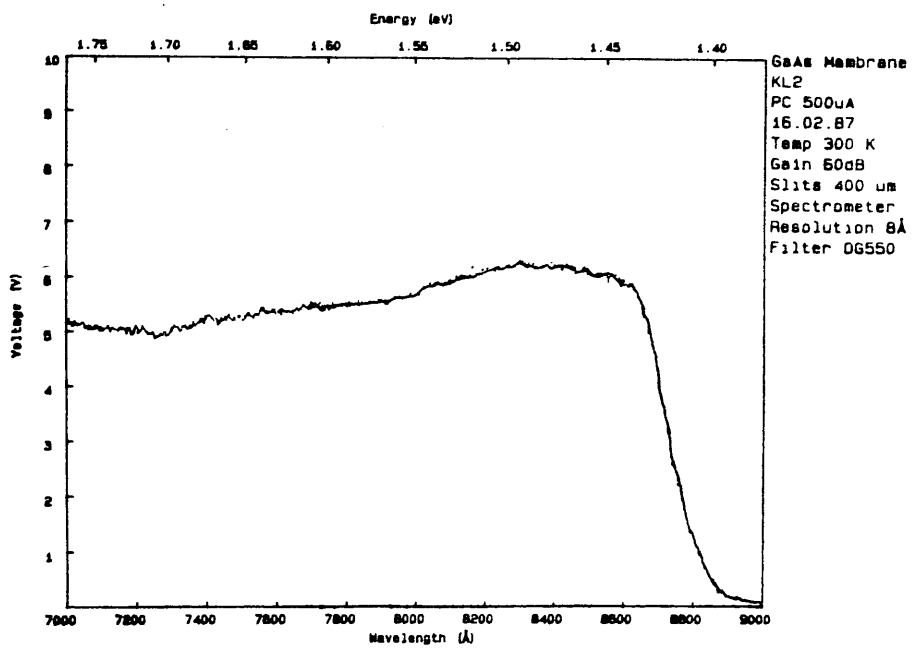
(c) T=30K



(d) T=50K

Figure 5.10

Photoconductivity Spectra



(e) T=300K

Figure 5.10

Photoconductivity Spectra

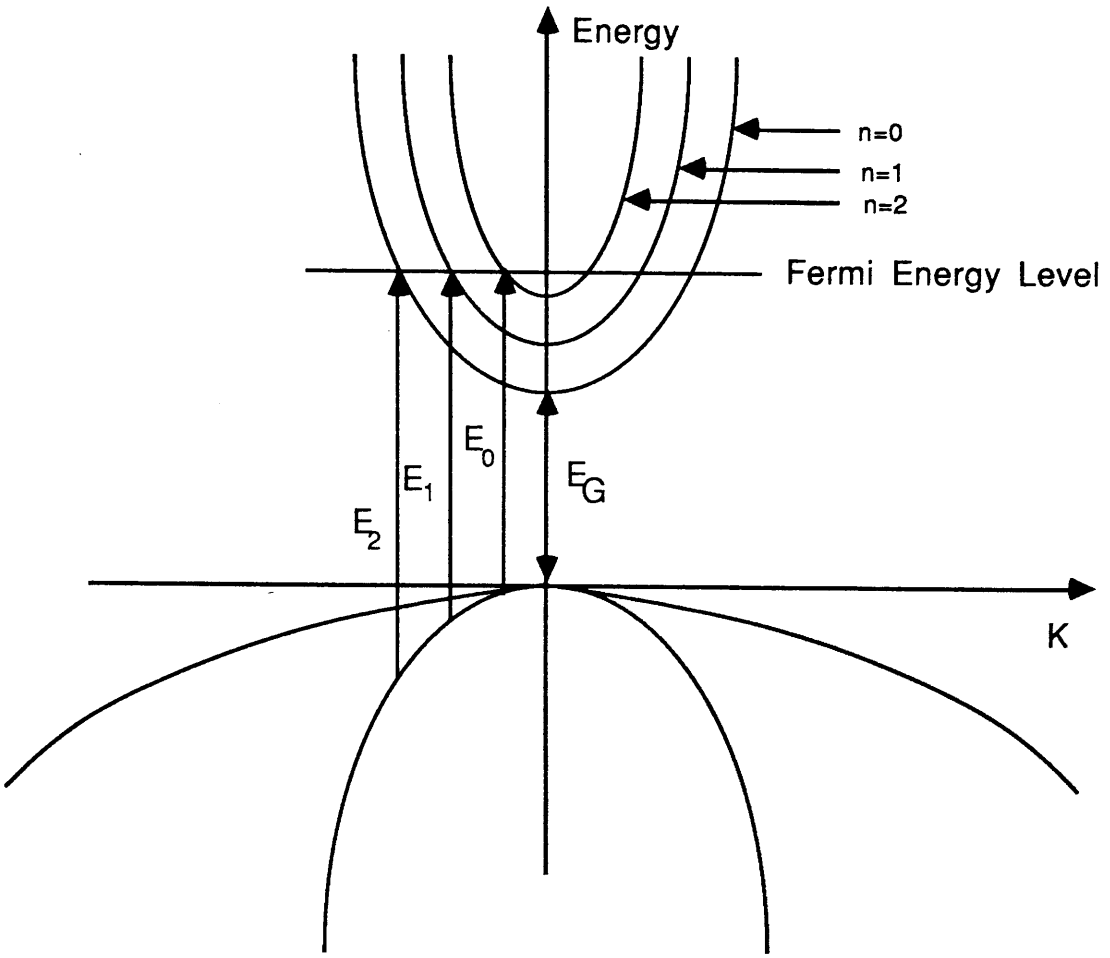


Figure 5.11 Transverse Band Transition

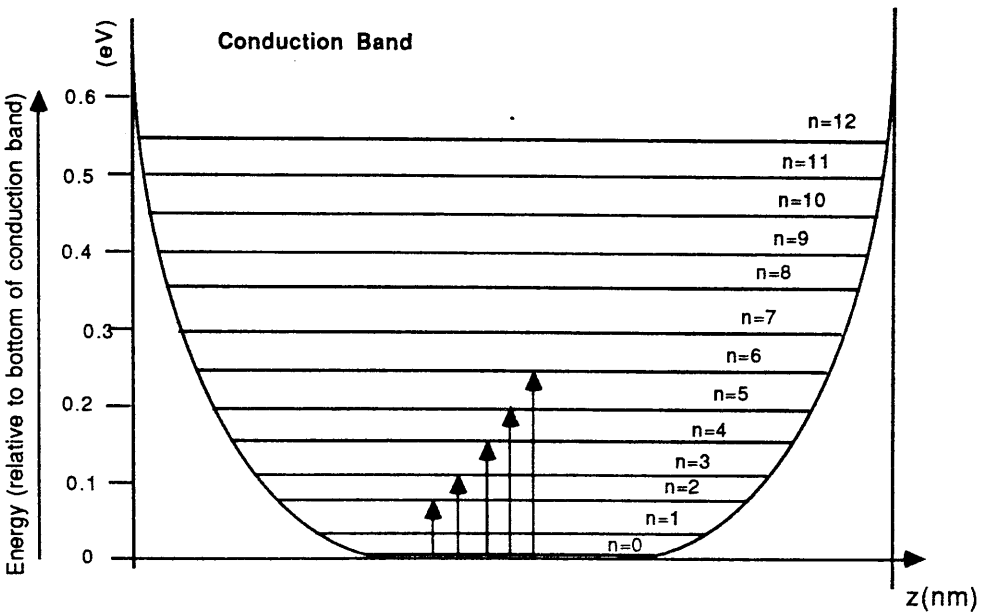


Figure 5.12 Intersub-band Transitions

Using infrared, interconduction transitions between confined states in 50nm thick GaAs membrane (shown above) may be observed.

Chapter 6 The Fabrication of Very High Transconductance Short Channel GaAs MESFETs with $Ga_{0.3}Al_{0.7}As$ Buffer Layer

6.1 Introduction

The structure of a conventional GaAs MESFET is shown in Figure 6.1 (6.1). Current flows through a thin n− type GaAs channel between two ohmic contacts known as the source and the drain. A third electrode, called the gate, forms a Schottky junction with the channel. The magnitude of the current flowing in the channel is determined by the depth of the gate depletion layer which is controlled by applying a voltage to the gate. Such a device is commonly fabricated with a material consisting of an active GaAs layer with 10^{17} cm^{-3} doping density and an undoped GaAs buffer layer (Figure 6.1). GaAs/GaAs is referred to as the conventional material structure here.

The most effective way to increase the operational speed of a MESFET is by reducing its gate− length. However, submicrometre gate− length devices can in fact exhibit worse d.c. characteristics with gate− length reduction typified by increased output conductance and poor saturation and pinchoff characteristics (6.2− 4). These are due to the short gate− length effects and carrier injection into the GaAs buffer (6.2,6.5,6.6). However, some improvement has been obtained by using a $Ga_{1-x}Al_xAs$ buffer layer (6.7− 10). The band gap mismatch at the GaAs/GaAlAs interface results in a barrier potential which confines carriers within the active layer. Recently, a theoretical investigation by Daembkes et. al. (6.11) indicates that the performance of short gate− length devices also improves with higher channel doping. Device performance of very short gate− length MESFETs may

therefore be optimised by using a very highly doped GaAs active layer with GaAlAs buffer layer. This was the subject of investigation in this chapter.

Chapter Outline

This chapter is divided into two parts. The first concerns a simple theoretical treatment on how the performance of a short gate–length MESFET is determined by the channel doping concentration (10^{17} cm^{-3} and 10^{18} cm^{-3}) and the buffer layer (undoped GaAs and $Ga_{0.3}Al_{0.7}As$). The analysis includes modelling the device using Monte Carlo simulation methods. The second part is concerned with the fabrication and evaluation of very short gate length MESFETs. The devices were fabricated on a MBE grown heterostructure consisting of an active GaAs layer with 3 X 10^{18} cm^{-3} doping density and an undoped $Ga_{0.3}Al_{0.7}As$ buffer layer.

Unless stated otherwise, all simulated results presented in this chapter were due to Al–Mudares (6.12), based on fabrication data supplied by the author.

6.2 Device Operation of Short gate–length MESFETs

The figures of merit which are conventionally used to compare the performance of FET devices are the transconductance, g_m, and the output conductance, g_D, which are expressed mathematically below:

$$g_m = \partial I_{ds}/\partial V_{GS} \qquad (1)$$

$$g_D = \partial I_{ds}/\partial V_{DS} \qquad (2)$$

Here I_{ds}, V_{GS} and V_{DS} are the drain current, the gate–source bias and the drain–source bias respectively.

The transconductance of a MESFET is predicted to increase with shorter gate–length but starts to fall when the length of the gate, L, becomes smaller than the channel thickness a. The reason is that the shape of the depletion layer is now circular rather than flat (6.5). The width d of a circular depletion layer varies with gate bias V_{GS} as

$$V_{GS} \propto d^2 \ln(d/L),$$

while for a flat depletion, d varies with V_{GS} as

$$V_{GS} \propto d^2.$$

The rate of change in depletion width with gate bias is therefore smaller for the circular depletion layer, i.e. a smaller transconductance, compared with the flat case.

In the absence of a substrate, the rise in saturated drain current with higher drain–source bias (with an output conductance of g_D) can be explained by the concept of velocity rotation (6.13). The output conductance increases with decreasing gate–length (6.14–15), but the increase can be significantly larger in the presence of a substrate. The reason for this is discussed next.

6.2.1 Substrate Effects: Undoped GaAs Buffer Layer vs Undoped $Ga_{0.3}Al_{0.7}As$ Buffer layer.

The drain current of a substrated MESFET is made up of two components, the channel current and a current which flows in parallel in the substrate (Figure 6.1).

In a MESFET with undoped GaAs buffer layer, a large carrier density in the buffer layer results from diffusion of carriers from the active layer to the buffer layer. Equilibrium is established at low drain–source voltages when further carrier diffusion is prevented by a diffusion field. However, at a sufficiently large drain–source bias the diffusion field is weakened by the transverse component of the drain field (6.5). This results in injection of carriers into the buffer layer which increases exponentially with the transverse field. The substrate current therefore increases with higher drain–source bias which in turn can increase the output conductance significantly. Shortening the gate–length has the effect of increasing the number of injected carriers, and hence the output conductance, due to reduced shielding of the channel from the drain field by the gate (6.5). Therefore, a device made with GaAs/GaAs exhibits higher output conductance compared with an unsubstrated device because of carrier injection. Further, output conductance of the substrated device increases faster with gate–length reduction. This is evident in Figure 6.2 which shows simulated output conductance versus gate–length for a MESFET with GaAs buffer layer and a device without a substrate.

In a MESFET with an undoped $Ga_{0.3}Al_{0.7}As$ buffer layer, the band gap mismatch at the GaAs/GaAlAs interface results in a barrier potential (Figure 6.3) which confines most of the carriers within the active channel in the absence at low drain fields. At high

drain–source voltages, carriers with sufficiently high energy to surmount the barrier potential at the interface may be scattered into the GaAlAs buffer layer (6.16–17).

Simulations of the carrier concentration under the gate at zero gate bias and a drain–source bias of 1 volt were performed. The carrier concentration versus depth profiles for MESFETs fabricated on materials with both GaAs and $Ga_{0.3}Al_{0.7}As$ buffer layers are plotted in Figure 6.4. For a comparison, the carrier distribution for an unsubstrated device was also shown. Figure 6.4 shows that at a given drain field, fewer carriers are transferred into the $Ga_{0.3}Al_{0.7}As$ layer by thermionic emission compared with the number of carriers injected into the GaAs layer. This combined with the low mobility and low saturation velocity of the carriers in GaAlAs (6.15–17) results in a small substrate current. Therefore, the effect of the GaAlAs buffer layer on the output conductance is small. It was demonstrated in Chapter 4 that the output conductance of a 0.1 μm gate–length device with a $Ga_{0.3}Al_{0.7}As$ buffer layer was comparable to that of a membrane MESFET in which the substrate was absent.

Carriers penetrate less deeply into $Ga_{0.3}Al_{0.7}As$ buffer layer than into GaAs buffer layer (Figure 6.4). Consequently, a smaller gate bias is required to pinch off a device with $Ga_{0.3}Al_{0.7}As$ buffer layer compared with a similar device with GaAs buffer layer.

It should be pointed out that the simulated carrier distribution profile for the unsubstrated device is not representative of the real case. It was shown in Chapter 3 that, in an unsubstrated (membrane) device, there is an additional surface depletion layer extending from the bottom surface. This was not taken into consideration in the simulation.

6.2.2 Effects of High Carrier Density

Simulations of MESFETs fabricated with $n^+ - GaAs$/undoped $Ga_{0.3}Al_{0.7}As$ with channels of 10^{17} cm^{-3} and 10^{18} cm^{-3} doping densities were carried out. The transconductance versus gate bias plots of MESFETs with 0.5 μm and 1 μm gate-lengths are shown in Figure 6.5. Very high transconductance (800 mS/mm) was predicted for a 0.5 μm gate-length MESFET fabricated with active layer with 3 X 10^{18} cm^{-3} doping density. The results also show that the increase in transconductance with higher doping density is more pronounced for the shorter gate device. This has been previously predicted by Daembkes et. al. (6.11) who attributed the results to velocity overshoot effects which, although is less pronounced at high doping density (Figure 6.6), is nevertheless significant in aggregate due to a larger number of carriers undergoing the overshoot effects.

In the absence of carrier injection, the output conductance increases less rapidly than the transconductance with higher doping density (6.11). Therefore, increasing the channel doping density results in an increase in open circuit voltage gain (g_m/g_D). The gain-bandwidth product, defined as $2\pi g_m/C_{GS}$ (where C_{GS} is the gate-source capacitance), determines the performance of a device in microwave and switching applications (6.1,6.6). For devices with short gate-lengths (< 0.25 μm) the fringing capacitance is important and this is only weakly dependent on the channel doping density (6.11). Consequently, C_{GS} increases gradually with increasing doping density as shown in Figure 6.7. The gain-bandwidth product of a short gate-length MESFET is therefore expected to increase with higher doping density due to the rapid rise in transconductance with doping density.

The parasitic source capacitance is reduced with higher channel doping density resulting in higher extrinsic transconductance. The n^+ active layer effectively extends the ohmic contacts to the region next to the gate edges, forming a short channel (6.18).

To summarise, the advantages of fabricating short gate–length MESFETs with highly doped active channel and undoped $Ga_{1-x}Al_xAs$ should be:

1. Higher transconductance resulting in increased open circuit voltage gain and higher gain–bandwidth product
2. Good saturation and pinchoff characteristics due to diminished carrier injection into the substrate.

6.3 Experimental: Fabrication of GaAs MESFETs

GaAs MESFETs with gate–lengths of between 0.08 μm to 0.2 μm and a drain–source separation of 1 μm were fabricated. The device material used was part of the MBE wafer designed for producing membranes (Figure 3.1). The structure of the material consisted of an active GaAs layer with 3 X 10^{18} cm^{-3} doping density and a nominally undoped $Ga_{0.3}Al_{0.7}As$ buffer layer. The active and the buffer layers were 50 nm and 0.15 μm thick respectively. At room temperature, the Hall mobility of the carriers in the active layer was measured to be 1250 Vs/cm^2. This low value is attributed to increased impurity scattering rate resulting from high channel doping density. The figure is in good agreement with the calculated value (μ) of about 1500 Vs/cm^2 using the empirical formula proposed by Hilsum (6.19) written below (appropriate at room temperature).

$$\mu = \frac{\mu_L}{(1+(N_D/10^{17})^{\frac{1}{2}})}$$

where μ_L= mobility limit due to lattice scattering

= 10^5 Vs/cm^2 for GaAs

6.3.1 MESFET Design and Fabrication Outline

The design of the a MESFET fabricated is shown in Figure 6.9. A flow diagram outlining the process steps required for making such a device is shown in Figure 6.10. The main steps are:

1) deposit ohmic contacts and registration marks

2) fabricate MOP masks for boron isolation

3) anneal ohmic contacts

4) pattern gate and perform gate recessing

Electron beam patterning was used at all levels. Alignment between the ohmic pattern in step (1) and the MOP mask pattern in step (2) was facilitated by the registration marks contained in the ohmic pattern. The alignment and the patterning were performed in a 0.8 X 0.6 mm frame using a 50 kV beam with 0.25 μm spot size. The positive resist used was a 1 μm thick PMMA layer which had been baked overnight at 180^{o}C. This was developed in 1:1 MIBK:IPA for 60s after exposure. The patterning of the gate in step (4) was carried out in a 100 X 76 μm frame using a 50 kV beam with 32 nm spot size. A high resolution bilayer resist consisting of 20nm/100nm 350,000MW/185,000MW PMMAs was used and this was developed in 1:3 MIBK:IPA for 30s followed by a 30s rinse in IPA after exposure. Prior to all metallisation steps, the sample was etched in 1:1 HCl:H_2O to remove the surface oxide layer. All lift–off steps were performed in acetone.

Devices with gate lengths ranging from 0.08 μm to 0.2 μm were fabricated. All were processed identically except at the gate level. This was done by carrying out steps (1) to (3) on a wafer before dicing it into smaller chips. As the rate at which a gate is recessed varies with the size of the opening in the resist, only devices with the same gate length were fabricated on individual chips.

Electrical isolation was achieved by boron implantation with MOP masks used to define the active areas.

6.3.2 Fabrication Procedure

6.3.2.1 Ohmic Level

The ohmic pattern contained a matrix of 4X4 sets of drain–source contacts and registration marks (Figure 6.11). The pattern was exposed on a 12.5 X 12.5 mm wafer at 4 by 4 sites using POSITION to calculate the exposure positions. The metallisation consisted of 100nm/20nm/50nm of $Au_{0.88}Ge_{0.12}$/Ni/Au which was the composition optimised for low temperature ohmic contacts formation.

6.3.2.2 Isolation Level

The bilayer resist used for making MOP masks (0.3μm/1μm polyimide/PMMA) was coated on the wafer. At each exposure site, the exposure frame was aligned to the ohmic registration marks. Although these differed from the standard registration marks, the alignment procedure was similar (as described in Chapter 2). In this case, the pattern shown in Figure 6.12 which contained partial outlines corresponding to the registration marks used were scanned at 2 μs/pixel. The two were made to coincide by adjusting the stage rotation, the X–Y Varymag and the beam shifters. Once this was done, the MOP mask pattern shown in Figure 6.13 was exposed.

MOP masks were fabricated using the technique described in Chapter 2. The wafer was subsequently implanted with boron ions with doses of 2 X 10^{18} cm^{-3} at 40 and 80 kV. Afterwards, the masks were removed by dissolving the polyimide layer in boiling acetophenone.

The ohmic metallisation was annealed at this stage in a reducing atmosphere (95:5 Ar:H_2) at 250–275 ^{o}C for 45s. In order to check

the uniformity of the ohmic contacts formed (over the wafer), the saturated drain current of randomly selected gateless devices were measured. It was important to ensure that the saturated drain current was maintained constant across devices on the wafer as this was used as reference for comparing the amount of gate recessing. Variation can be caused by non– uniformity in heat distribution across a sample during annealing. This problem is usually solved by subjecting the sample to a second annealing cycle, usually at a slightly elevated temperature or over a longer anneal time or combination of both. Such measure was however not necessary here.

The wafer was coated with the resist for patterning gates and then diced into four 3.1 X 12.5 mm chips, each containing 48 gateless devices.

6.3.2.3 Gate Level

The pattern at this level consisted of the gate as well as the probing pad (Figure 6.14). In order to pattern gates of the required lengths, resolution tests were performed. The results are shown in Figure 6.15.

The gate pattern was exposed individually between the ohmic drain– source contacts using the alignment technique described below.

6.3.2.3.1 Gate Alignment

An approximate alignment was made by aligning the centre of the VDU screen to the edge of a set of drain– source contacts, centralised in the drain– source gap, at X80 magnification and then at X320 magnification. This was performed with the beam blank switched

off.

Fine alignment was performed with the beam blank on at X1250 magnification (100 X 76 μm frame). A pattern which consisted of partial outlines corresponding to the edges of the drain–source contacts was scanned at 2 μs/pixel. Once these were made to coincide, the gate pattern was exposed.

6.3.2.3.2 Gate Metallisation

The gate metallisation consisted of 30 nm of Al on 30 nm of Ti. For planar devices , the sample was etched in 1:1 H_2O:HCl for 60s before introducing it into the evaporator. Ti was evaporated at about 10^{-6} Torr. Due to the strong affinity of Ti to oxygen, it was necessary to shield the wafer from the partly oxidised Ti with a shutter. The shutter was removed after a short period of time when most of the residual oxygen in the evaporator had been absorbed by the Ti.

Electrical Characteristics of Planar MESFETs

All electrical testing of devices was carried out using a HP4145A Semiconductor Parameter Analyser and Omni–probe probing system.

Planar MESFETs with 0.2 μm gate–length were fabricated on one of the chips. The I–V characteristic of a Schottky contact formed is shown in Figure 6.16. The diode had an ideality factor of 2.2 with a reverse breakdown voltage of 4V. These figures were typical of the planar devices fabricated. The high ideality factor and relatively small reverse breakdown voltage were due to high channel doping density. Higher doping density results in narrowing (also lowering) of the

Schottky barrier height. As a consequence, thermionic field emission becomes more pronounced in the conduction process of the diode. In an ideal diode (ideality factor of 1), the conduction mechanism is purely by thermionic emission; deviation from this (ideality factor > 1) results if other conduction mechanisms (thermionic field emission in this case) are involved. The probability of carriers from the metal tunneling through the barrier increases with higher doping. Thus, for highly doped material, reverse breakdown mechanism by thermionic field tunneling breakdown instead of avalanche breakdown. This accounts for the low breakdown voltage measured here (6.20).

The I–V characteristics of a planar device with 0.2 μm gate–length is shown in Figure 6.17. Breakdown of gate took place before the device could be pinched off. This was the case for all the planar devices. A reverse gate bias of about 4.5V (calculated) is required to pinch off the devices. Gate recessing was therefore necessary to do this.

Maximum transconductance of 300mS/mm was obtained for the planar devices and this occurred at a reverse gate bias of typically 1V.

6.3.2.3.3 Gate Recessing

Recessing of the gate was performed after development of the gate pattern. Using the developed resist as the mask, the wafer was etched in 1000:20:7 H_2O:NH_3:H_2O_2 at 4^{o}C for 5s periods. The etch solution was designed to leave the etched surface oxide free (6.21). Before each etch step, the sample was immersed in IPA to wet the PMMA. This was to ensure that the etch solution could reach into the the narrow openings in the resist. After every 5s of etching, the

saturated drain current was measured in order to monitor the amount of recessing.

0.08 μm, 0.17 μm and 0.2 μm wide gate patterns were exposed on the remaining three chips. These were recessed until the saturated drain currents of control devices (two to four on each chip) were reduced respectively to 0.3, 0.1 and 0.75 times the unrecessed (saturated) drain current. However, on completion of recessing, a significant variation in the recessed drain current was measured on devices on the same chip. This was attributed to non−uniformity in the recessing. The chip which contained devices with the narrowest gate opening, i.e. 0.08 μm, showed the widest recessed drain current distribution. The range of the recessed drain current was 0.1 to 0.75 times the unrecessed drain current. More uniform results were obtained for the 0.17 μm and 0.2 μm wide gates, the range of recessed drain current measured was respectively 0.7 to 0.8 times and 0.1 to 0.2 times the unrecessed saturated drain current. The results indicate that the recessing of a very narrow gate (<0.2 μm) is difficult to control. Nevertheless, the range of recessed depths obtained proved useful for analysing the effects of different recessed depths on device performance.

The chips were metallised with 30nm/30nm of Ti/Al after the recessing step. A SEM micrograph of one of the MESFETs fabricated is shown in Figure 6.18.

6.4 Results and Discussions

6.4.1 I– V Characteristics

The I– V characteristics of recessed gate MESFETs with 0.08 μm, 0.17 μm and 0.2 μm gate– lengths are shown in Figures 6.19.a– c. The devices showed good saturation characteristics with very low output conductance. The average output conductance at zero gate bias for all the devices was about 10 mS/mm. MESFETs with deep recess (i.e. with recessed drain current reduced to below about 75% of the unrecessed drain current) showed good pinchoff characteristics even for the devices with 0.08 μm gate– length. However, compression of the transconductance near pinch– off was observed in all the devices. This was attributed to the effects of the interface quality as discussed in Chapter 4. For the 0.2 μm gate– length devices (with recessed drain current/unrecessed current of more than 0.75), breakdown of the gate took place before the devices could be pinched off completely. This can be seen in Figure 6.19.d which shows that the sudden increase in the drain current near pinchoff coincided with a large increase in the gate current.

No correlation between recessing depth and transconductance was observed in devices on the same chip. On the chip containing 0.17 μm gate– length and 10% recessing, the devices exhibited extremely high transconductance at room temperature. A maximum of more than 700mS/mm and an average value (over the devices fabricated) of 600 mS/mm were measured. These are the highest transconductance values reported for GaAs MESFET. Maximum g_m of 600 mS/mm was obtained for the chips containing 30% (0.08 μm gate– length) and 75% (0.2 μm gate– length) recessing, with respective average value of

450 and 400 mS/mm. In Figures 6.20.a– c transconductance versus gate bias for some of the devices are presented.

6.4.2 Effects of Recessed Depth on Device Operation

In Figure 6.21, the gate bias at which maximum transconductance occurred ($V_{GS'}$) was plotted against the recessed drain current (I_{dsrec}). Two interesting observations can be made from this plot.

Surface Transconductance Compression

For depletion type MESFETs, maximum transconductance is predicted to occur at zero gate bias. This is demonstrated as follows. The gate depletion width d of a MESFET varies with gate bias V_{GS} as

$$d = \text{constant} \times (V_{GS} + V_B)^{\frac{1}{2}} \qquad (3)$$

where V_B is the built– in potential of the Schottky junction.
The drain current I_{ds} is related to d according to the expression (to a first approximation)

$$I_{ds} \propto (a - d). \qquad (4)$$

Here a is the channel thickness. Differentiating (4) with respect to V_{GS} gives

$$\partial I_{ds}/\partial V_{GS} = - \text{ constant} \times \tfrac{1}{2}(V_{GS} + V_B)^{-\frac{1}{2}} \quad (5),$$

which is equal to transconductance g_m according to equation (1). It is obvious from equation (5) that g_m is maximum when V_{GS} is zero. For submicrometre gate– length MESFETs, g_m may however peak at a negative gate bias ($V_{GS} < 0$). A device which shows this characteristics is said to be suffering from transconductance compression. It can be seen from Figure 6.26 that this phenomenom is present in depletion

devices (i.e. devices with $V_{GS'} < 0$) fabricated.

As discussed in Chapter 4, transconduction compression may be due to free surface depletion between the gate and the drain. At a small gate bias, the surface depletion layer may be wider than the gate depletion (Figure 4.22a). Under this situation, the drain current is controlled by the surface depletion rather than the gate resulting in the compression effect. This has been modelled by Chen and Wise (6.22) but, to the best of the author's knowledge, is yet to be substantiated experimentally. The explanation is however consistent with the following experimental observations.

Firstly, it can be seen from Figure 6.21 that transconductance compression became less pronounced with deeper gate recessed depth (i.e. V_{GS} at which g_m peaked approached zero with deeper recessing). This may be explained thus. Deeper recessing results in the gate depletion layer extending deeper into the channel with respect to the width of the surface depletion layer (Figure 4.22b). Consequently, the influence of the surface depletion layer on drain current, and hence transconductance compression, diminishes.

For planar devices, transconductance peaks at a sufficiently high negative gate bias when the gate depletion layer is wider than the surface depletion layer. A higher reverse gate bias, however, implies a smaller transconductance according to equation (5). In contrast, for recessed gate devices, g_m peaks at lower reverse gate bias and hence, higher transconductance, with deeper gate recessing (correct only if $d < a$). The maximum transconductance measured on planar devices was about 300mS/mm compared with an average of 450mS/mm or higher for recessed gate devices (meaured in the depletion mode). Similarly, transconductance may be expected to increase with deeper recessing due to lowering of gate bias at which transconductance peaks (which

according to equation (5) results in larger g_m). However, no correlation was found between transconductance and recessed depth. One explanation may be non-uniformity in processing; to investigate this, a more controlled experiment should be carried out.

Interface Effects

It is interesting to note that the transconductance of the devices with deep recess peaked in the enhancement regime ($V_{GS'} > 0$) even though none of the devices were pinched off at zero gate bias. This happened for devices with drain current reduced to below 40% of the unrecessed drain current. Moreover, a higher positive $V_{GS'}$ was measured for a device with a a smaller recessed drain current (or a thinner channel). This may be due to the same interface effects which cause compression of transconductance near pinch-off(6.8).

A region of low carrier mobility was more than likely to exist in the GaAs layer near the interface. As discussed in Chapter 4, this is attributed to the effects of interface quality associated with growth of GaAs on GaAlAs, namely surface roughness and interface impurities effects. For a device with a deep recessed gate structure, the gate depletion layer may only modulate carriers within the low mobility region as illustrated in Figure 6.22. In such a case, maximum transconductance occurs at a forward gate bias when the depletion layer was brought away from the low mobility region into the high mobility region. A device with a deeper recessed gate would require a higher forward gate bias. This argument is consistent with simulated results using an analytical model described in the next section.

6.4.3 Quasi– Two Dimensional Analytical Model of GaAs MESFETs

Transconductance values were calculated using a quasi 2 Dimensional Diffusion Model developed by Al– Mudares (6.12). The model is based on that proposed by Yamaguchi and Kodera (6.13) modified to include the following:

a) non abrupt transition between active channel ($n= N_D$) and depletion region ($n= 0$) under the gate (6.24); where $n=$ carrier density and $N_D=$ doping density

b) modified velocity– electric field characteristics that include velocity overshoot caused by the effect of a short gate length. These were used in a similar way to that considered by Feng (6.25) after having determined the time dependence of the velocity using Monte Carlo calculations.

Using the model, the transconductance of a 0.17 μm gate– length device was calculated at various gate voltages with the drain– source biased at 1V. It was assumed that all carriers are confined in the active GaAs layer. As it was not possible to determine the actual recess depth, the active layer under the gate used in the calculation was estimated from the gate pinchoff voltage obtained from I_{ds} versus V_{GS}.

Agreement between the calculated and experimental results could only be obtained by assuming that the carrier mobility in the channel was inhomogeneous. If a uniform mobility of 1250 cm^2/Vs (measured value) was used, the calculated transconductance at a given gate bias was higher than the experimental result e.g. 1000 mS/mm compared with 300 mS/mm at zero gate bias.

A 15 nm layer extending from the interface was assigned a mobility of 700 cm^2/Vs. This figure was arrived at by iteration i.e. by

feeding a series of mobility values into the computer program until the calculated transconductance at a given gate bias equalled an experimental point. Using this mobility value, and assuming the mobility of carriers in the remaining channel thickness was 1250 cm^2/Vs, the transconductance at other gate voltages were calculated. The choice of the thickness of the low mobility layer was arbitrary as it is the mobility– thickness product that matters in the calculation of drain current in the low mobility region.

Figure 6.23 shows experimental and theoretical g_m versus V_{Gs} plots for the 0.17 μm gate– length devices. It can be seen that the calculated and experimental plots are in good agreement. The spread in experimental g_m values seen in the plot in Figure 6.24 is due to non– uniformity in the gate recessing over the chip on which the devices were fabricated.

The main characteristics of the MESFETs fabricated are summarised in Table 6.1 below.

GATE-LENGTH (μm)	V_{CS} (PINCHOFF)	CHANNEL THICKNESS	MAX g_m (mS/mm)	AVERAGE g_m (mS/mm)
0.2	-1.8V	35nm	600	500
0.08	-1.0V	29nm	600*	450*
0.17	-0.7V	27nm	700*	600*

*Denote g_m measured in the enhancement mode. Channel thickness calculated from gate pinchoff voltage.

Table 6.1

6.5 Conclusions

The work presented here demonstrated that the d.c. performance of very short gate length GaAs MESFETs can be greatly improved by using a very highly doped channel and $Ga_{1-x}Al_xAs$ buffer layer. Very high transconductance values were obtained for MESFETs fabricated with a GaAs active layer with 3 X 10^{18} cm^{-3} doping density and an undoped $Ga_{0.3}Al_{0.7}As$ buffer layer. The highest transconductance measured at room temperature for a 0.17 μm MESFET was 700 mS/mm which is the highest transconductance for GaAs MESFET reported so far. In addition, the devices fabricated showed good saturation and pinchoff characteristics. Very low output conductance was also measured, of less than 10 mS/mm at zero gate bias.

Experimental evidence which suggests that transconductance compression was due to surface depletion layer was also presented. It was demonstrated that the compression diminished with deeper gate recessing.

Device simulations using both Monte Carlo and analytical methods predicted higher transconductance values than the measured results. The lower experimental values may be due to degradation of carrier mobility near the GaAs/GaAlAs. When this was taken into consideration, the calculated results using the analytical model were in good agreement with the experimental results. The poor carrier mobility near the interface was attributed to interface effects which also accounted for transconductance compression near pinchoff. Therefore, further improvement in device performance may be obtained by improving the quality of the inverted GaAs/GaAlAs interface.

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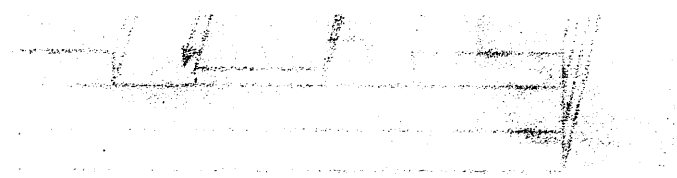
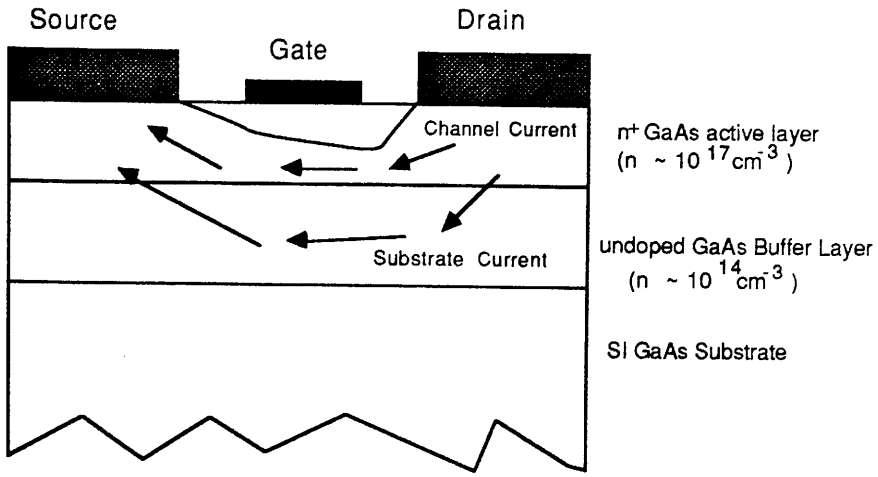




Cross-sectional View

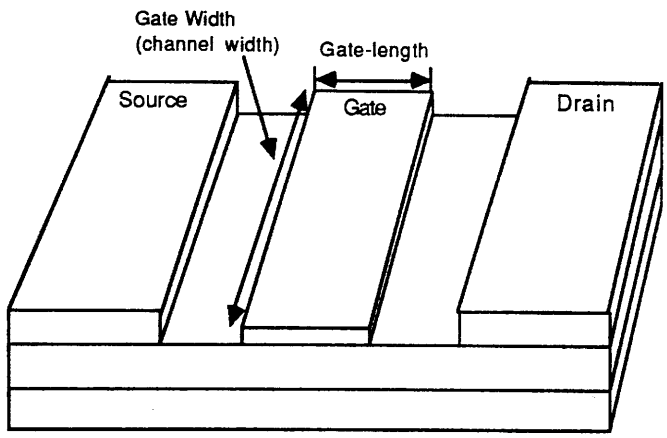


Figure 6.1

Structure of a Conventional GaAs MESFET

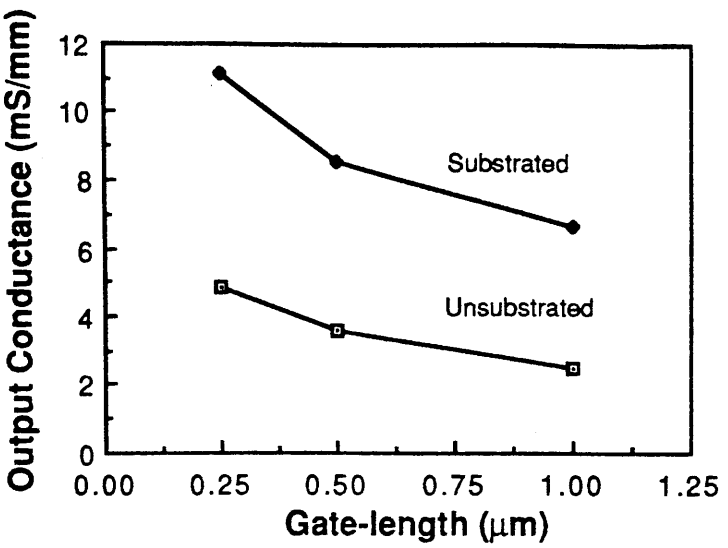


Figure 6.2

Simulated output conductance vs gate-length for substrated and unsubstrated GaAs MESFETs (After Al-Mudares, ref. (6.15)).
Active Layer Doping Density= 1E+17 cm^{-3}
n- GaAs buffer layer (n=1E+14 cm^{-3})
Drain/source gap=3μm
Drain/source bias=5V
Gate Bias = 0 V.

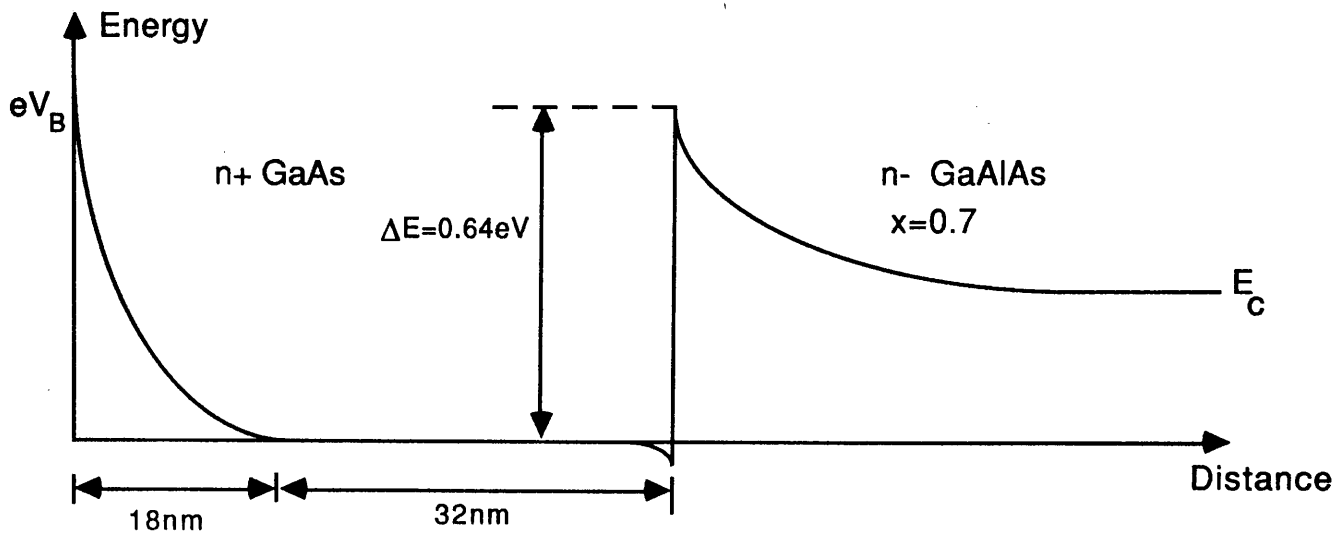


Figure 6.3

Band Diagram of GaAs on p- GaAlAs
(After Patrick, ref. 6.21)

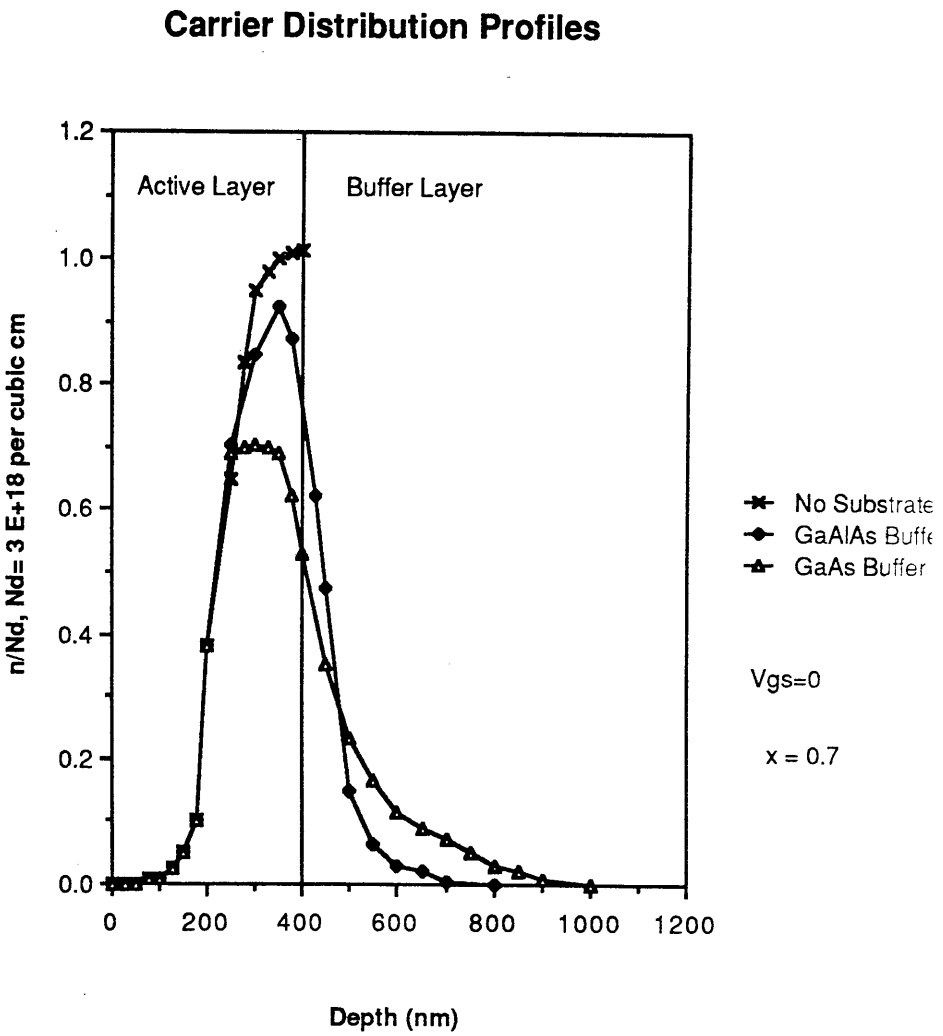


Figure 6.4

Calculated Carrier density vs depth profiles in n+ GaAs ($N_D = 10^{18} cm^{-3}$) on GaAs and $Ga_{1-x}Al_x$ As substrates. The case in which the substrate is absent is also shown.
Gate-source bias=0V
Drain-source bias=-1V

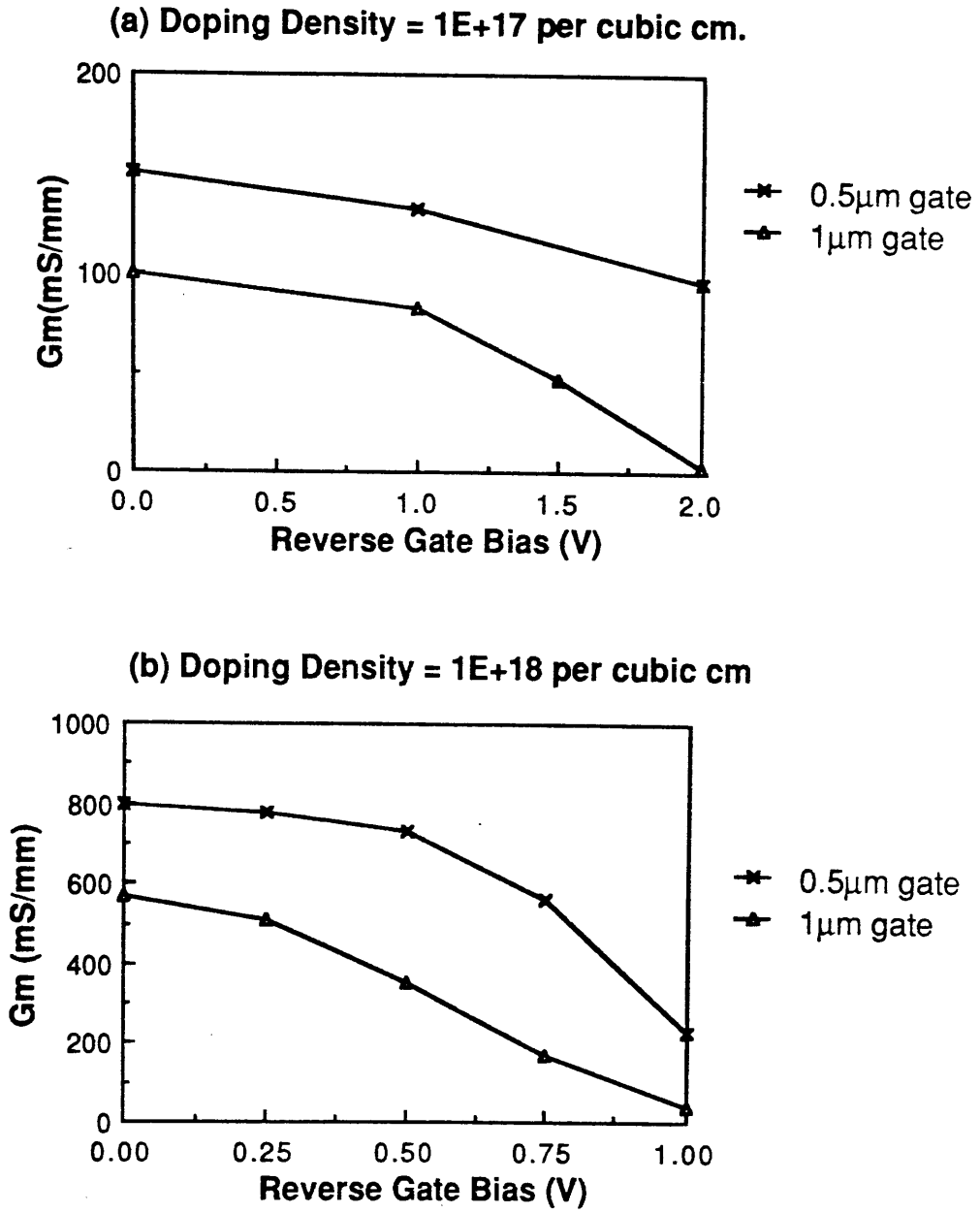


Figure 6.5

Calculated transconductance vs gate bias plots for 0.5μm and 1μm gate-length MESFETs.

(a) $N_D = 10^{17} cm^{-3}$
(b) $N_D = 10^{18} cm^{-3}$

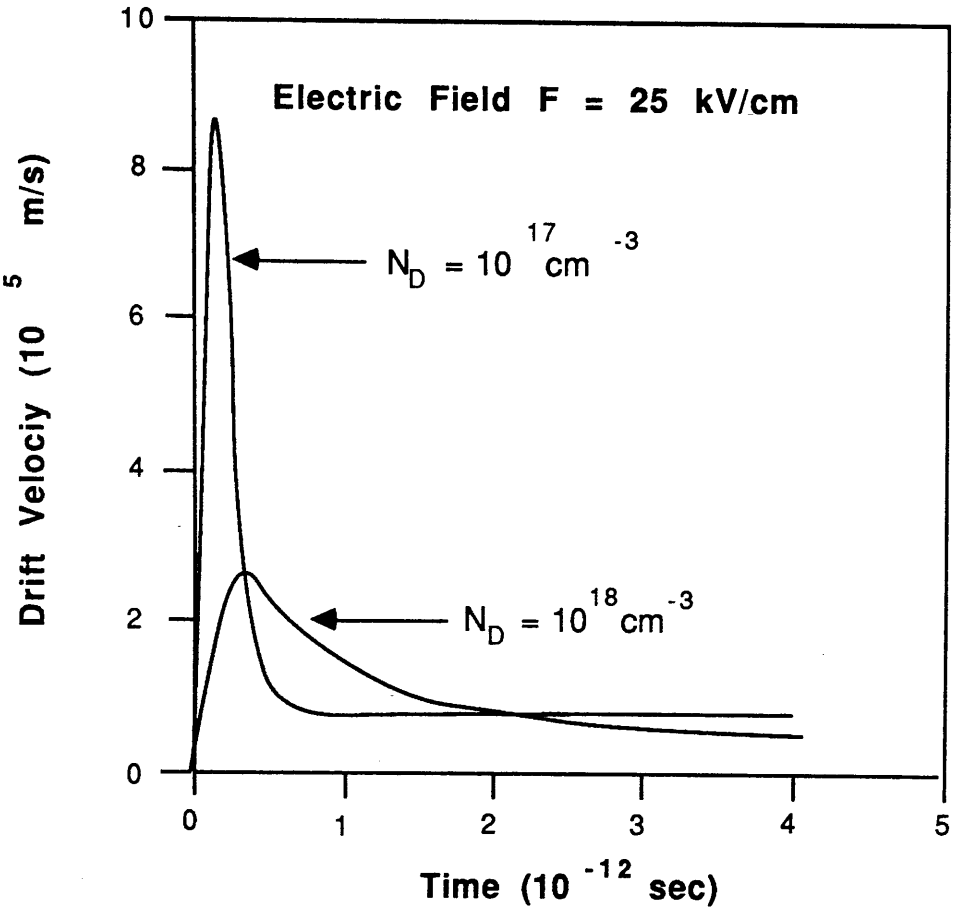


Figure 6.6

Simulated Drift Velocity vs Time Plot of an electron in GaAs of 1E+17 and 1E+18 cm^{-3} doping density when subjected to a step field of 25kV/cm..

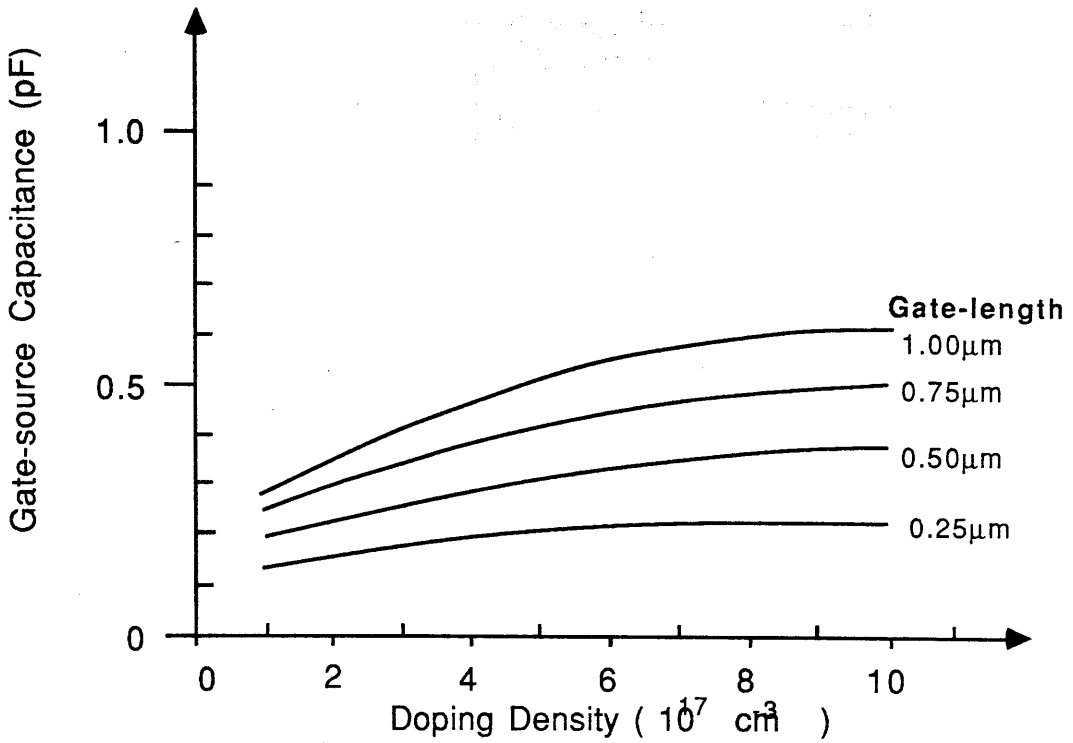
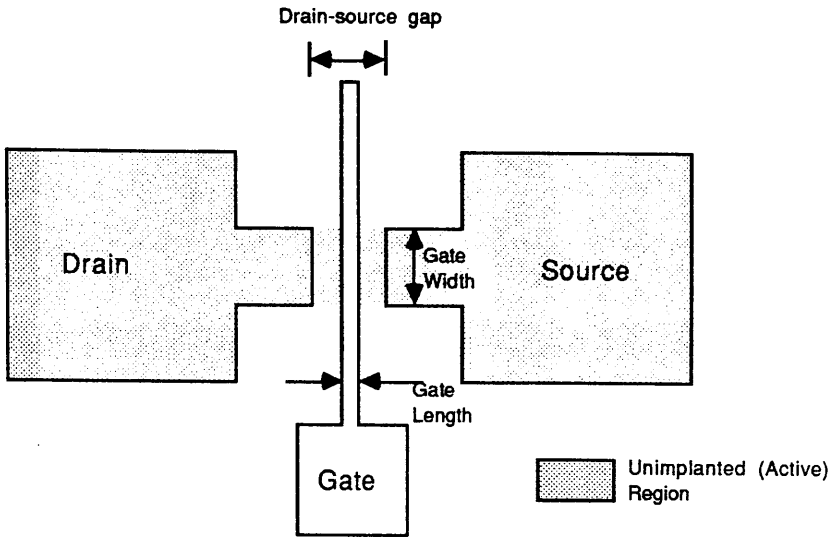
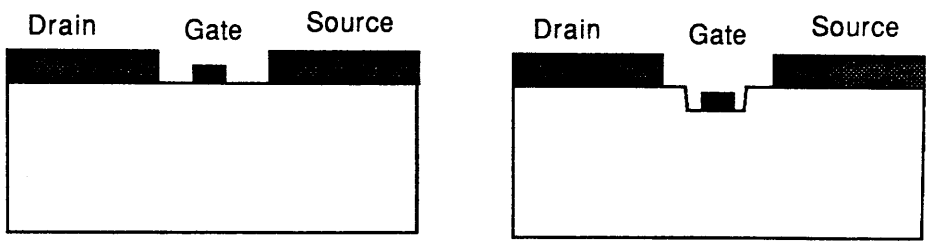


Figure 6.7

Calculated gate-source capacitance for different gate-lengths
Pinchoff Voltage=2V, Drain-source bias=-0.5v
Gate-width=300µm
(After Daembkes et.al , ref. 6.11)



Plan View



Planar MESFET

Recessed Gate MESFET

Cross-Section

Figure 6.9 Design of MESFET

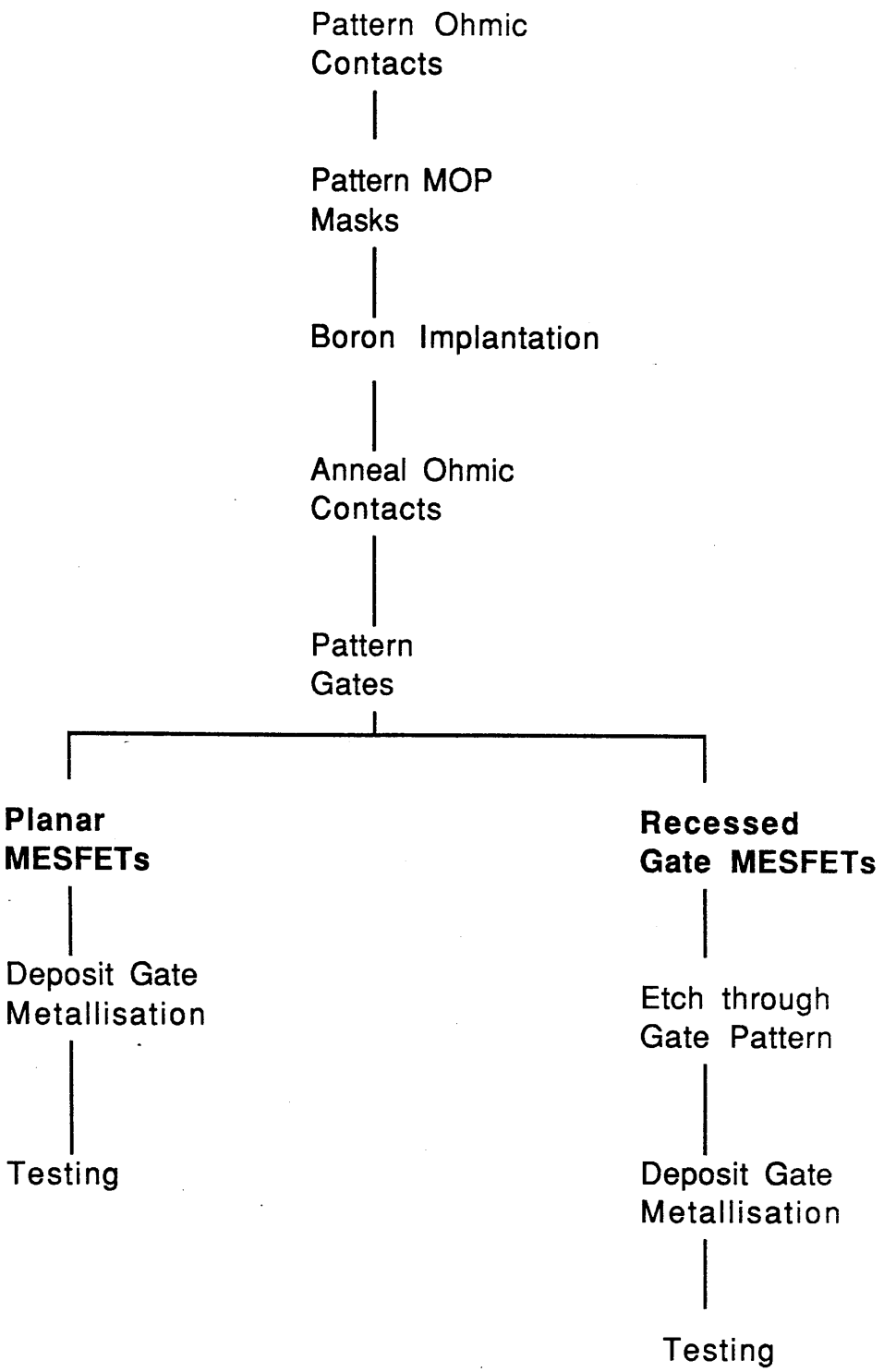


Figure 6.10 Fabrication of GaAs MESFETs

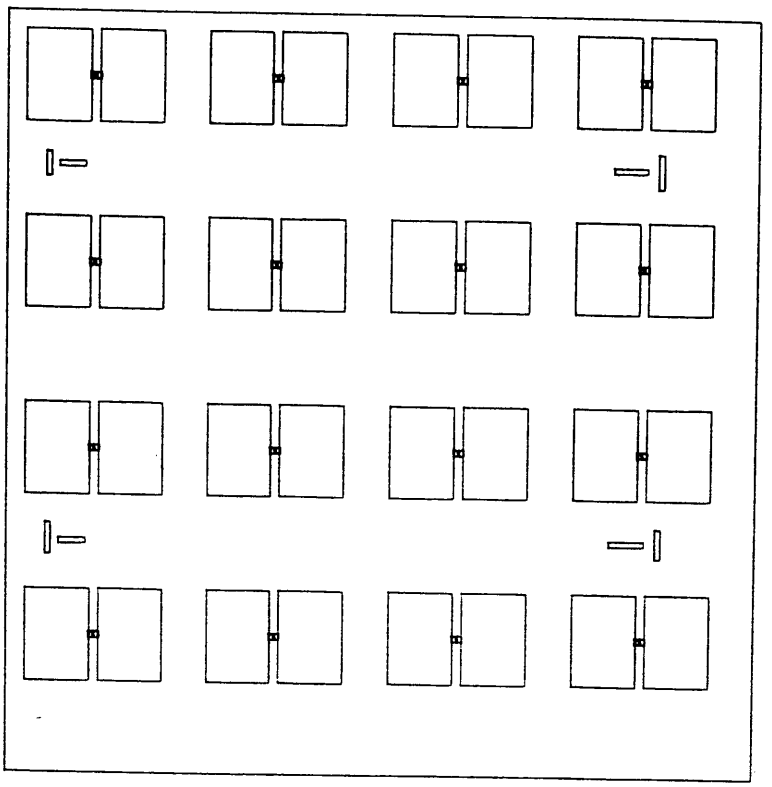


Figure 6.11 Ohmic Pattern

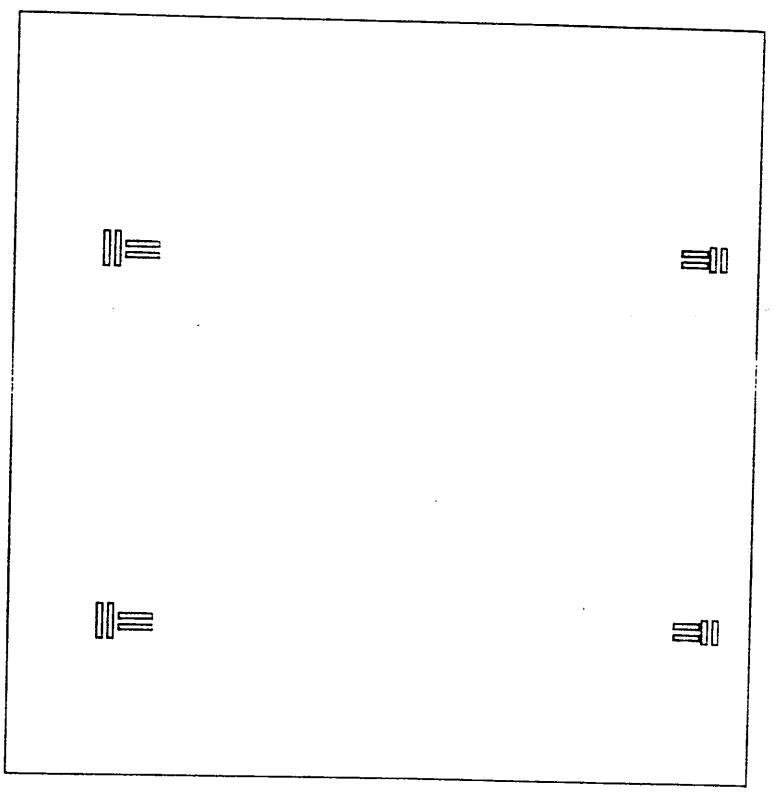


Figure 6.12 Scanned Pattern For Alignment

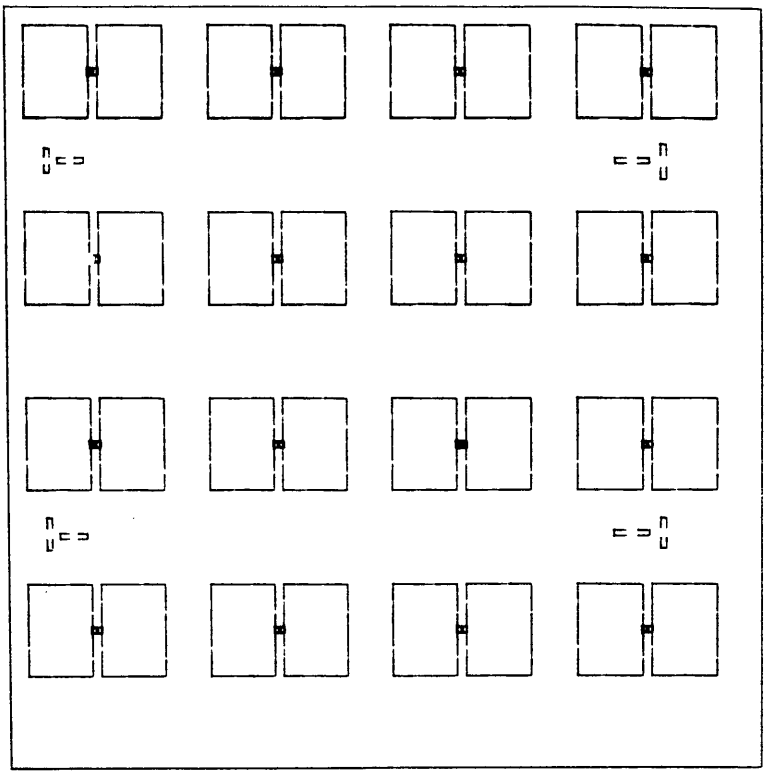


Figure 6.13 MOP Mask Pattern

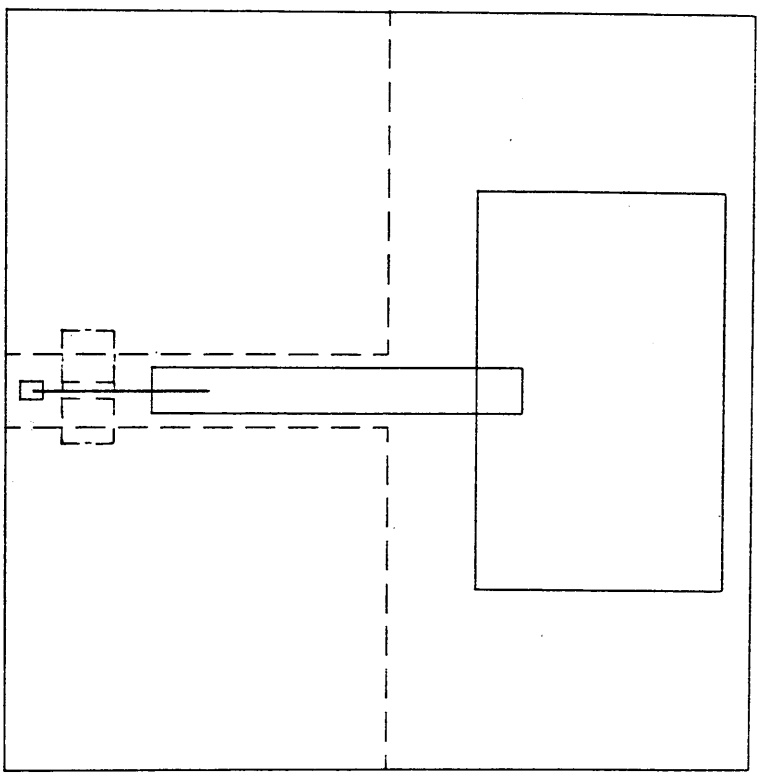


Figure 6.14 Gate Pattern

(ohmic and MOP mask Patterns are outlined-dashed line)

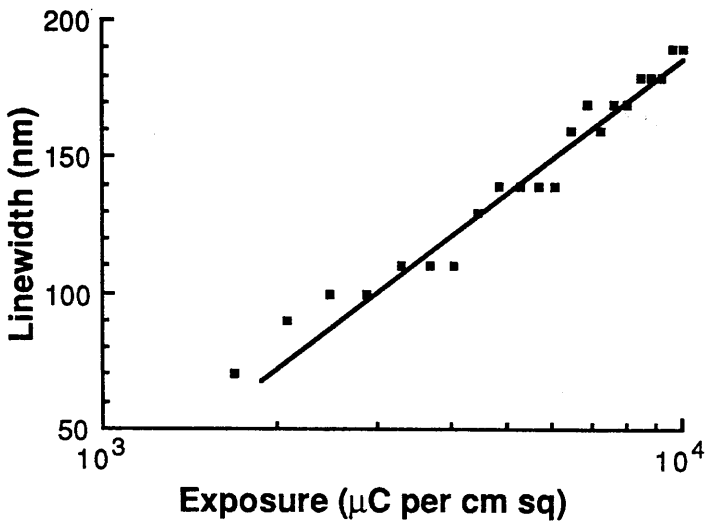
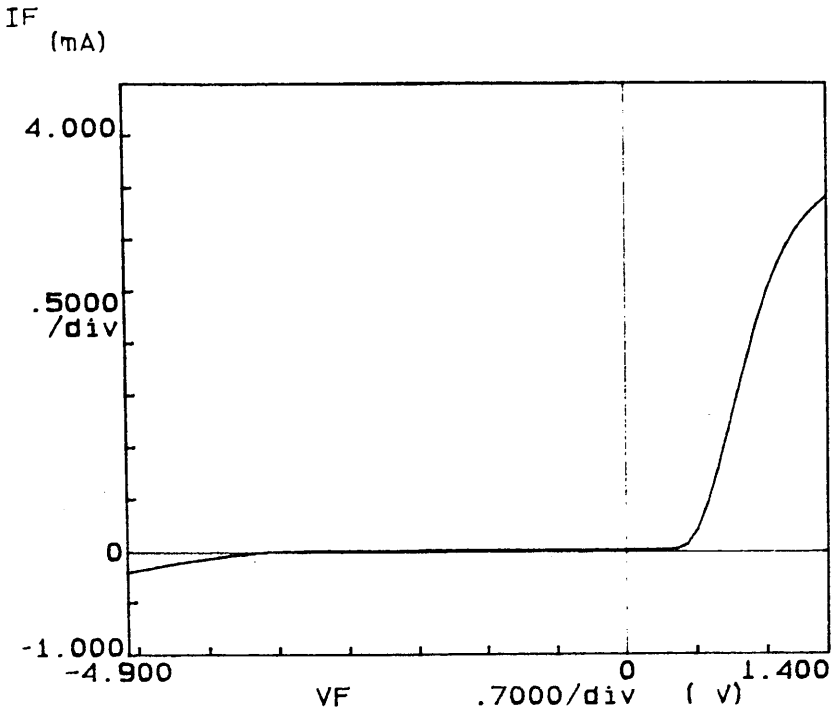
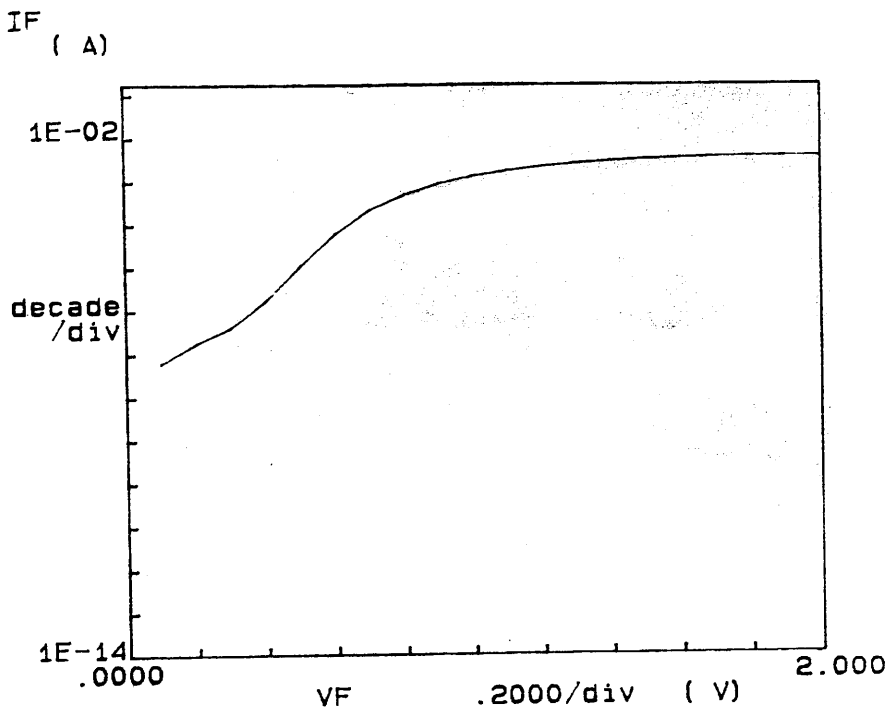


Figure 6.15 Linewidth-Exposure Plot.

20nm/100nm 350,000MW/185,000MW PMMAs,
Single Line Scan
Metallisation: 30nm/30nm Ti/Al



(a)



(b)

Figure 6.16 Schottky Characteristics

(a) I-V Plot and (b) logI-V Plot

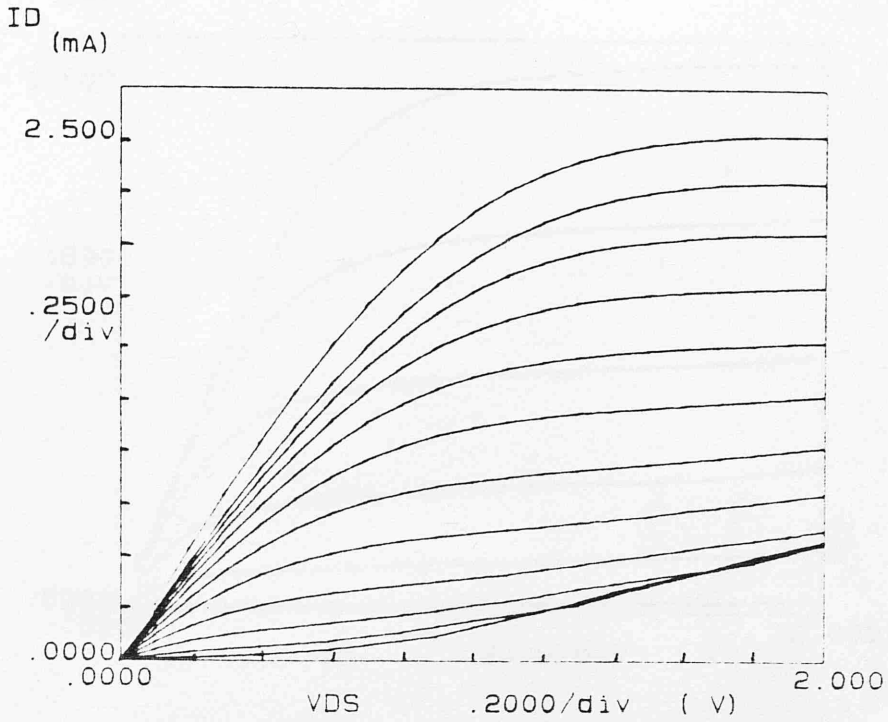
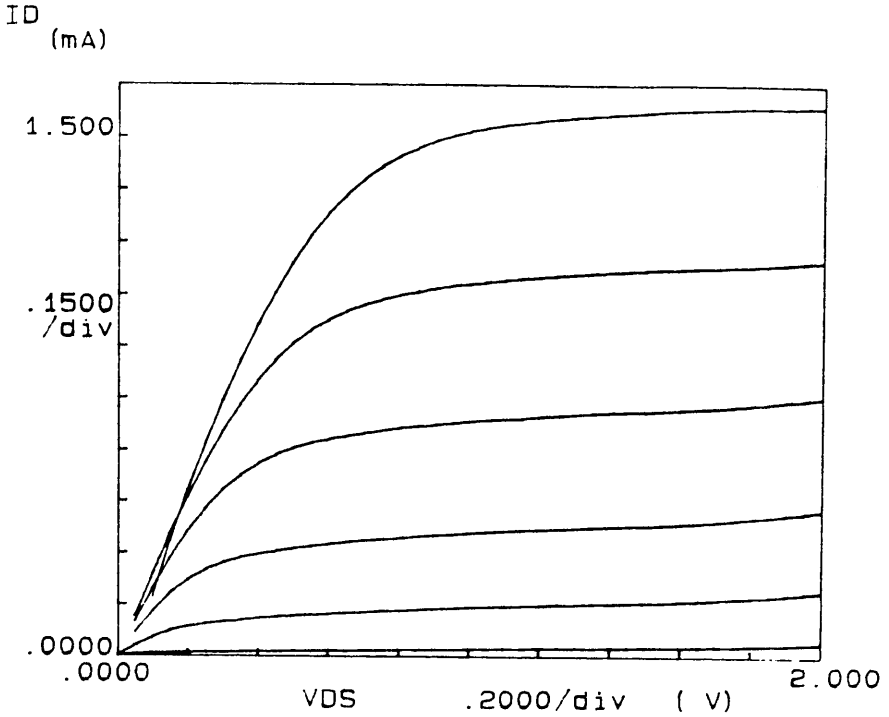


Figure 6.17

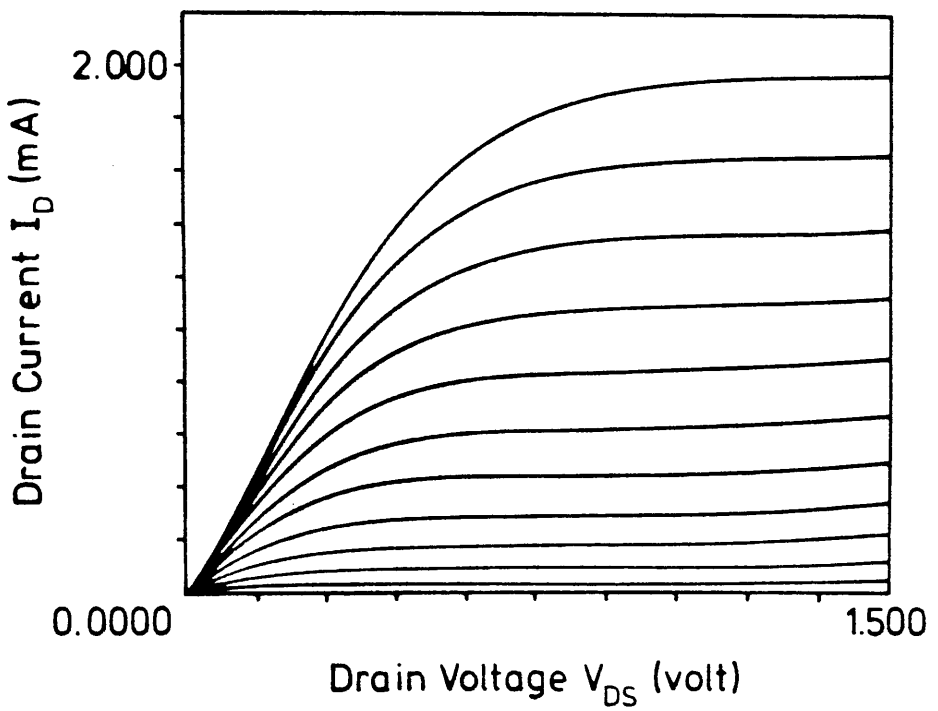
I-V Characteristics of 0.2μm gate-length, planar MESFET.

Figure 6.18

SEM micrograph of a 0.2μm Gate-length recessed Gate MESFET.(Gate Width of 5μm and drain-source gap of 1μm)



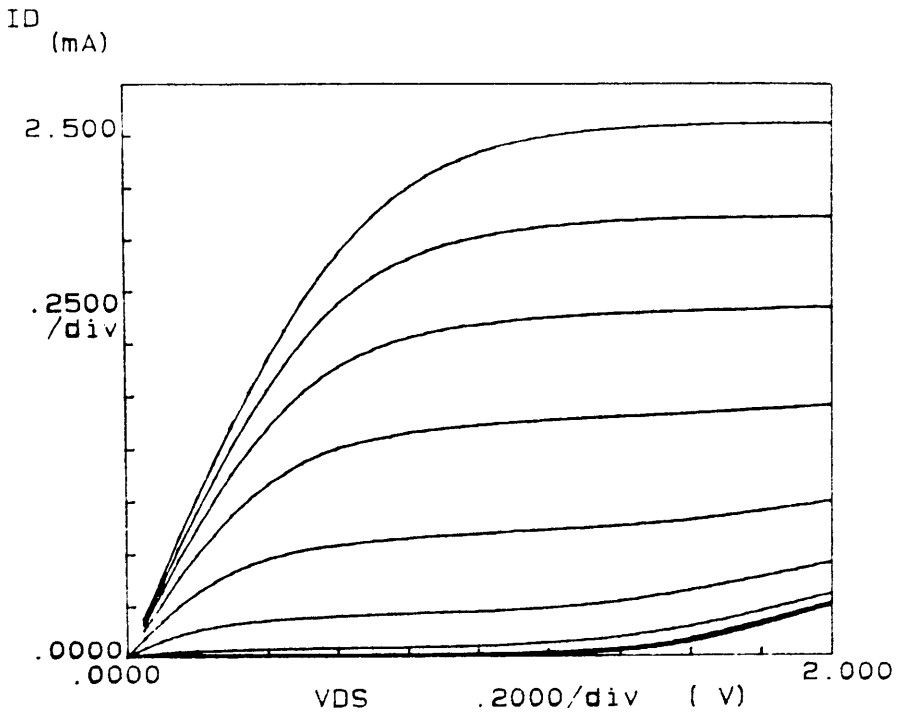
(a) V_{GS} = 0.6, 0.4, 0.2, ..., -0.4V



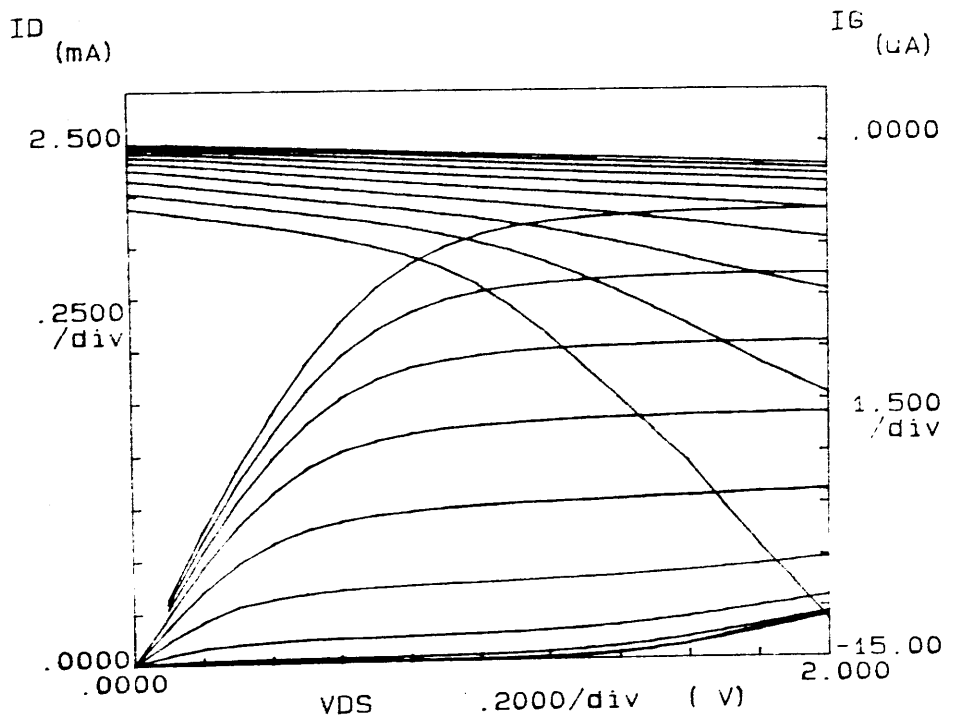
(b) V_{GS} = 0.6, 0.5, 0.4,.....,-0.5 V

Figure 6.19

I-V Characteristics of Recessed Gate MESFETs
(a) 0.08μm gate length, ~10% recessing (b) 0.17μm gate-length, 10% recessing.



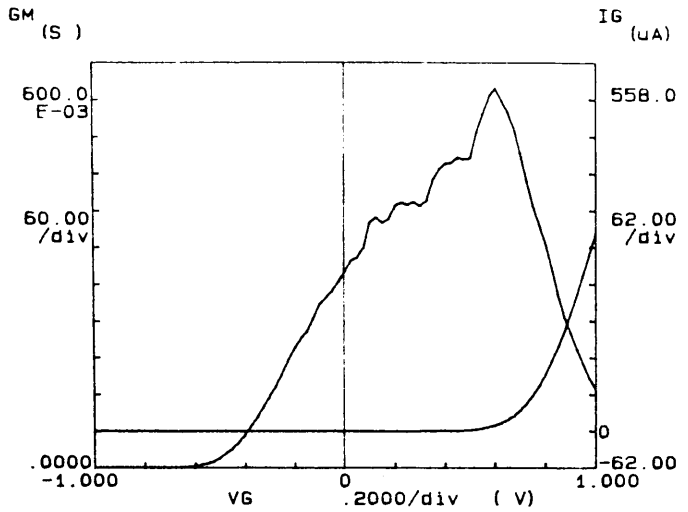
(c) V_{GS} =0, -0.2, -0.4, -0.6,.....,-1.8 V



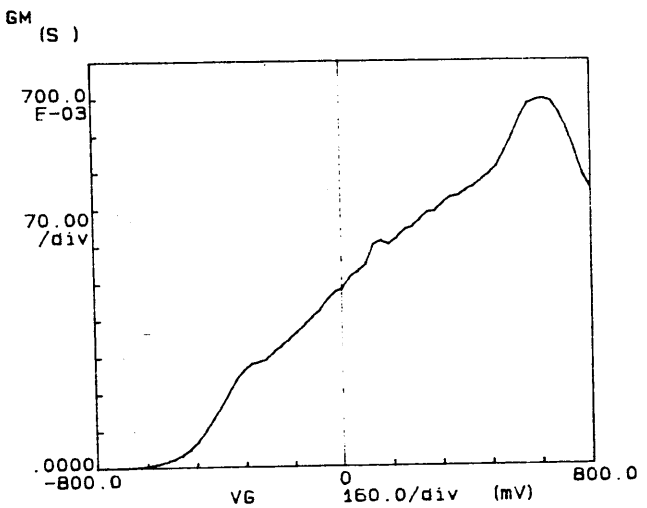
(d) V_{GS} =0, -0.2, -0.4, -0.6,.....,-1.8 V

Figure 6.19

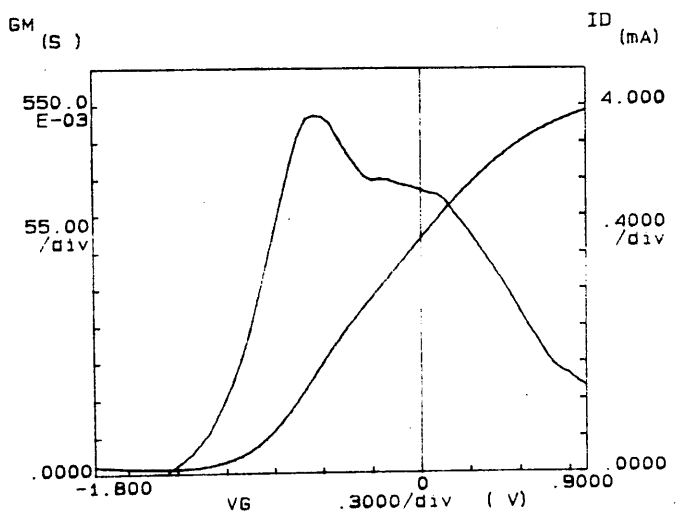
I-V Characteristics of Recessed Gate MESFETs
(c) 0.2μm gate length, ~75% recessing (d) 0.2μm gate length, ~75% recessing.



(a) 0.08µm Gate length, 30% recessing



(b) 0.17µm Gate length, 10% recessing



(c) 0.2 µm Gate length, 75% recessing

Figure 6.20

Transconductance vs Gate Voltage Plots (at drain-source bias of 1.5V).

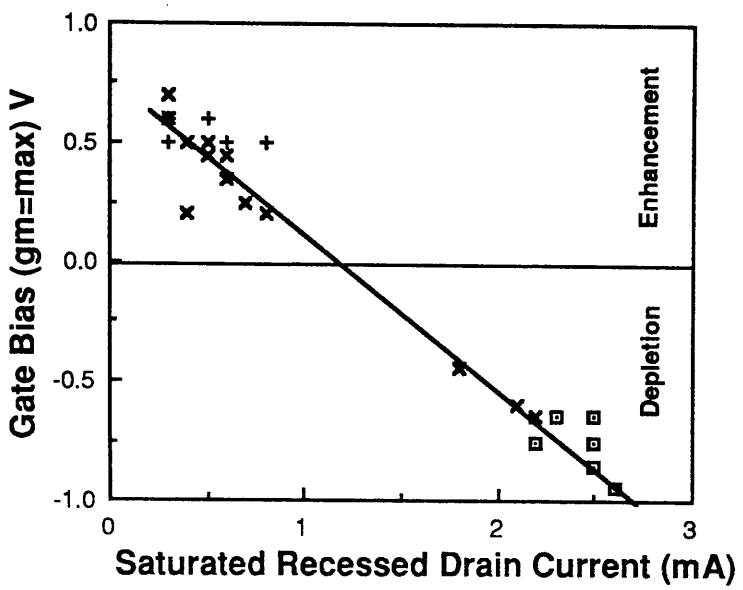


Figure 6.21

The gate bias at which transconductance peaked is plotted against the saturated recessed drain current above.
Gate-length: + 0.17μm
x 0.08μm
⊡ 0.2μm

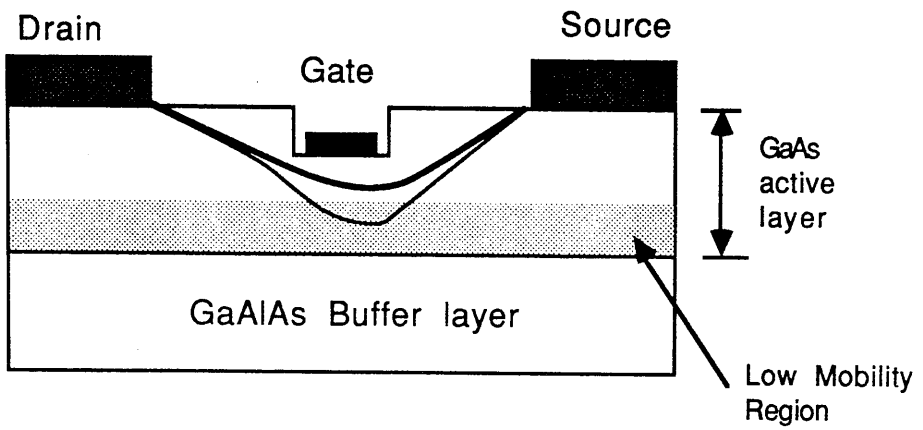


Figure 6.22

At V $\leq$ 0, the depletion layer (light curve) may be within low mobilty region near GaAs/GaAlAs interface. To achieve maximum transconductance, a positive gate bias is applied to bring the depletion layer out of the low mobility region (dark curve).

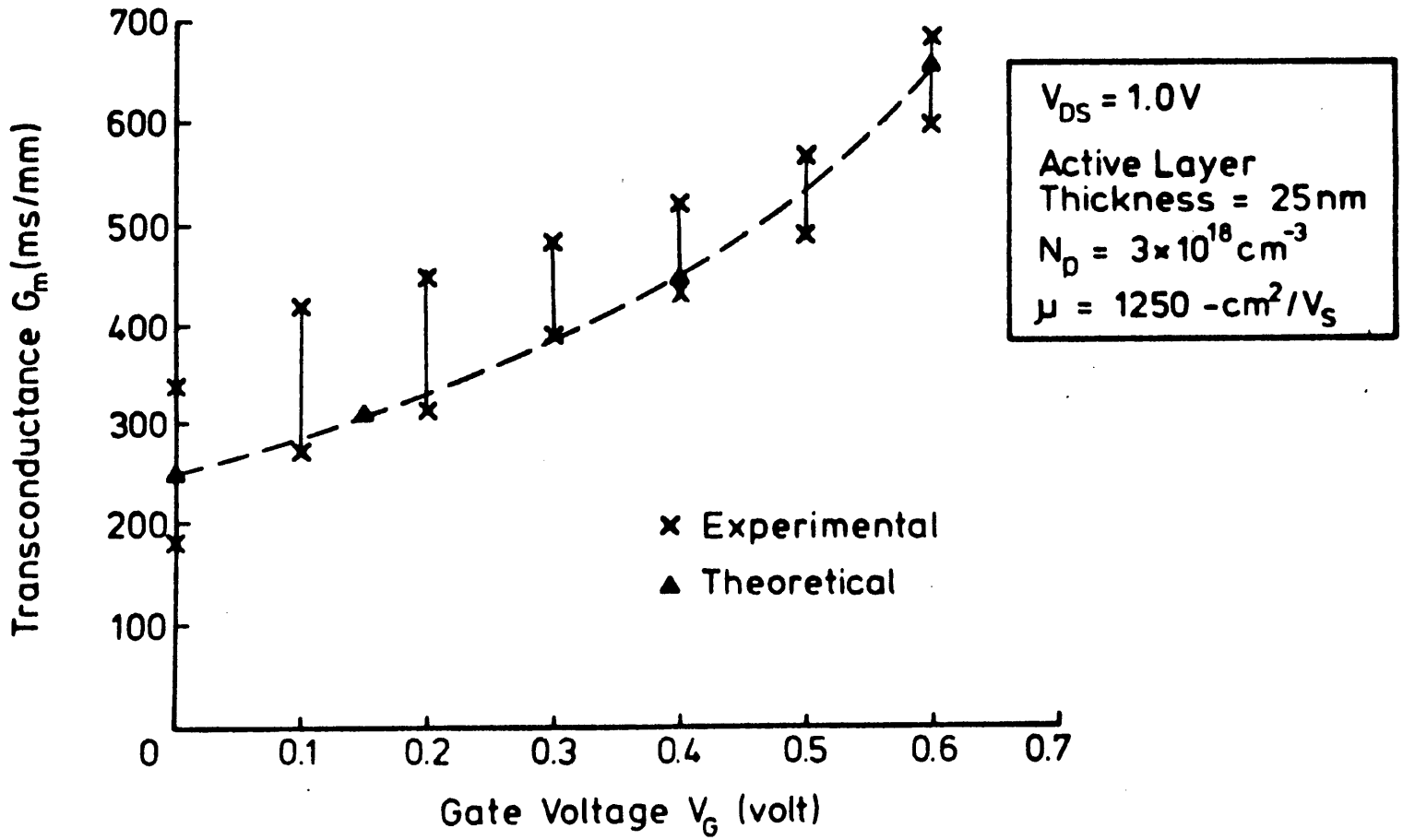


Figure 6.23

Experimental and theoretical Transconductance gm/gate voltage plots for 10% recessed gate MESFETs (gate length=0.17μm, gate width=5μm and drain-source gap of 1μm

A complete process technology for membrane devices was established. Fabrication of MESFETs and grating–gate MESFETs (LSSL structures) on 50nm thick n^+-GaAs membranes has been demonstrated. The performance of these devices were dominated by surface effects. In membrane MESFETs, the presence of a bottom surface depletion layer resulted in reduced drain current and transconductance (compared with nominally identical solid substrate devices).

Surface states effect resulted in loss of gate control in short gate–length unrecessed MESFETs (both membrane and solid substrate devices). This was indicated by the presence of transconductance compression near zero gate bias. For LSSL structures, the periodic potential induced by small pitch metal gratings (100nm) was thought to be masked by surface depletion.

Transconductance compression was less pronounced on recessed gate MESFETs. The effect was found to diminish with deeper gate recessing and was reflected in higher transconductance compared to planar (unrecessed) devices (maximum of over 700mS/mm compared with 300mS/mm).

Recessed gate MESFETs with gate–length of between 0.08μm and 0.2μm have been fabricated on a heterostructure consisting of an n–GaAs active layer with $3X10^{18}$ cm^{-3} doping density and an undoped $Ga_{0.3}Al_{0.7}As$ buffer layer. These devices showed excellent d.c. characteristics with very high transconductance (maximum of 700mS/mm) and low output conductance (average of 10mS/mm at zero gate–bias). It was observed that the output conductance of nominally identical heterostructure and membrane MESFETs were similar. This

indicates that very good carrier confinement was provided by the $Ga_{0.3}Al_{0.7}As$ buffer layer.

However, the heterostucture devices suffered from transconductance compression near pinchoff. Moreover, devices with deep gate recesses were found to operate as enhancement type devices. These were attributed to an interfacial low mobility region associated with the growth of GaAs on GaAlAs. Using a quasi two dimensional analytical model, it was predicted that higher transconductance could be obtained by elimination of the low mobility region.

A theoretical investigation indicated that the GaAs membrane may be viewed as a quantum structure in which energy states are quantised. However, results from photoconductivity and absorption measurements did not show evidence to support this. Nevertheless, several interesting observations were made. Absorption due to interband transition at the L−valley and oscillations in the photoconductivity spectra were observed.

Proposals for Future Work

This project demonstrated the importance of gate recessing for improved short gate−length MESFETs performance. For circuit applications, the ability to recess the gate uniformly over a wafer will be important. Conventional wet etching technique was shown to be unsuitable for recessing gates with length of less than 0.2μm. Gate recessing by dry etching, however, is worth considering especially in the light of recent work on low damage reactive ion etching of GaAs by Cheung (7.1) of this Department. Structures with vertical walls have been formed using a combination of hydrogen and methane

gases. More importantly, the etching is highly reproducible and uniform, while damage to the crystal structure is low. On n−GaAs with 10^{17} cm^{-3} doping density, the ratio of photoluminescence intensity measured on etched surface to that on unetched surface was 0.94 (compared with a ratio of 0.3 obtained by using $SiCl_4$ gas). Schottky junctions formed on the etched GaAs broke down at −16V compared with −17V on the unetched GaAs.

It may still be possible to observe superlattice effect in LSSLs if recessing of the grating gate can be performed. Such structures may be formed in membranes by using the dry etching technique. This is because of the high resolution achievable (currently about 40nm) together with very slow etch rate (20nm/minute).

In order to probe the quantum confined states predicted in GaAs membranes, far infrared absorption measurement should be performed. GaAs membranes may be useful for characterisation of dry etching damage as these allow TEM microscopy for studies of crystal structure (from diffraction patterns).

Future work should also involve modification of the heterostructure design in order to achieve further improvement in MESFET performance. Interface roughness can be eliminated by using a $Ga_{1-x}Al_xAs$ buffer layer with smaller x (7.2−5) (although decreasing x results in poorer carrier confinement), while interface impurities can be reduced by the use of a superlattice buffer layer or GaAs quantum wells (7.6−8).

Chapter 7 References

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