University of Glasgow

InAlN/AlGaN/GaN High Electron Mobility Transistors on Si Substrates

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Abstract

Nowadays, improvements in the energy efficiency of silicon (Si) power electronics are becoming less substantial, as Si is approaching its theoretically predicted limits. Gallium nitride (GaN) transistors are candidates for the next era of power electronics due to a unique set of properties that enable increased power per unit area compared to Si. The industry transition to GaN is also cost effective, as GaN can be run on existing Si process lines using GaN-on-Si heteroepitaxy.

This work investigates a "dual barrier" InAlN/AlGaN/GaN-on-silicon high electron mobility transistor (HEMT) technology with respect to its suitability for power electronic transistor development and reports routes to the realisation of enhancement mode and depletion mode transistors through its use. The material structures were grown to satisfy high conductivity in the access regions and compatibility with several gate process modules which can allow for normally-off operation.

Experimental testing of material and transistor properties was performed through parametric studies aiding process optimisation. Carrier transport characteristics were obtained and material sheet resistances as low as 258 Ω/sq were determined. Mesa etch isolation over a 3 µm x 100 µm gap and HEMT off-state leakage were in the order of 100 nA/mm for a 200 V sweep. Access to the 2DEG was obtained through thermally optimised ohmic contacts of as low as 0.44 Ω mm contact resistance.

Depletion mode (normally-on) devices fabricated on 8 nm InAlN/3 nm AlGaN/GaN-on-Si wafers exhibited maximum drain-source currents of 1A/mm, transconductance ~203 mS/mm and nearly ideal subthreshold swing ~65.6 mV/dec at 300 K. A two order of magnitude reduction from in gate leakage currents was achieved via the incorporation of Pt-based gate contacts compared to Ni gate stacks. For gate-source voltage V_{GS} = -4 V, gate leakage current was 0.6 mA/mm for Ni/Au gate contacts, whilst this metric was $3.4 * 10^{-4}$ mA/mm for Pt/Au contacts. For gate-source voltage V_{GS} = 3 V, the Ni/Au based gate contacts exhibited 1 mA/mm gate leakage current, compared to $3.7 * 10^{-6}$ mA/mm gate leakage current when Pt/Au gate contacts were used. Passivation via ICP SiN_x

was found to greatly enhance the channel conductivity, a property that was reversed via the use of SiN_x bilayers of different stress. The performance of InAlN/AlGaN/GaN HEMT was compared to AlGaN/GaN devices for reference.

Gate process engineering techniques were developed, as means for shifting the threshold voltage of InAlN/AlGaN/GaN devices. Enhancement mode (normally-off) devices were demonstrated, exhibiting threshold voltage of +4.5 V via a selective wet etch process, based on ethylenediamine and free from plasma induced damage. Achieving a positive threshold voltage is critical for fail-safe operation. Compared to depletion mode devices fabricated on the same wafers, enhancement mode InAlN/AlGaN/GaN devices incorporating a $SiCl_4$ based gate recess etch process showed a ~50% increase in extrinsic transconductance which is attributed to the decrease of the separation of the channel from the gate contact and the subsequent increased gate control.

As mentioned above, normally-off operation of GaN based transistors is important for power transistors and as such there is merit in performing ohmic contact optimisation work directly on enhancement mode materials. Evaluation of ohmic contacts was performed using gated TLM structures. The impact of these structures was analysed as it was found to significantly influence the extracted contact and sheet resistance characteristics due to the gate potential.

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Author's Declaration

Unless otherwise acknowledged, the content of this Thesis is the result of my own work. None of this material has been submitted for any other degree at the University of Glasgow or any other institution.

Konstantinos Floros

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List of Acronyms

2DEG	2-Dimensional Electron Gas
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
ALE	Atomic Layer Etching
AlGaN	Aluminium Gallium Nitride
BFOM	Baliga Figure of Merit
BJT	Bipolar Junction Transistor
CO_2	Carbon Dioxide
CCFL	Cold-cathode fluorescent lamp
d-mode	Depletion mode
e-beam	Electron beam
e-mode	Enhancement mode
GaN	Gallium Nitride
FET	Field-effect Transistor
HEMT	High Electron Mobility Transistor
HS	High stress
ICP CVD	Inductively Coupled Plasma Chemical Vapour Deposition
IGBT	Insulated Gate Bipolar Transistor
InAlN	Indium Aluminium Nitride
IPA	Isopropanol
JWNC	James Watt Nanofabrication Centre

LED	Light Emitting Diode
LPCVD	Low Pressure Chemical Vapour Deposition
MIS	Metal-insulator-semiconductor
MOCVD	Metal-organic Chemical Vapour Deposition
MOS	Metal-oxide-semiconductor
MS	Medium stress
PE CVD	Plasma Enhanced Chemical Vapour Deposition
PVD	Physical Vapour Deposition
PMMA	Poly (methyl methacrylate)
RF	Radio Frequency
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
Si	Silicon
SiC	Silicon Carbide
TLM	Transfer Length Method
TMAH	Tetramethylammonium Hydroxide
UPS	Uninterruptible Power Supplies
VdP	Van der Pauw structure

1 Introduction and Thesis Outline

1.1 Introduction

The environmental and economic impact of inefficient power conversion has resulted in an increasing demand for more intelligent and efficient use of energy resources. An estimated 10% of the total generated electrical power is lost as heat during power conversion; this translates to hundreds of terawatts of lost power or more than double the globally installed capacity for non-hydro renewable electricity generation [1]. With the current power conditioning approaches being used, energy consumption will rise by 35 % in the next 20 years [2]. As a result, governments have made their environmental policies more strict; the UK government has set a target for a 34 % reduction in CO_2 emissions by 2020 and 80 % by 2050 [3].

Power electronic switches, i.e. semiconductor devices, are at the heart of most power conversion systems. Through the management of key electrical attributes such as voltage, current, frequency and waveform, power electronic switches control, transform and process electric energy in applications such as the electricity grid, renewables, electric motors and consumer electronics [4]. In addition to global CO_2 emissions reduction, an improvement in the efficiency of power electronics could offer financial savings to the consumer.

Among the candidate material systems for the future of power electronics, such as SiC or Si, GaN possesses a favourable set of properties. Due to its large bandgap and high critical electric field, it can sustain high voltages. Its high breakdown strength can minimise the channel length requirements for a given blocking voltage. This in turn reduces on-resistance and the storage of minority carriers. The low minority carrier storage and the high mobility allow for high frequency operation and subsequently a reduction in the required passive component cost, weight and size. Another advantage is that GaN wafers can be grown at competitive prices due to the possible heteroepitaxial growth on silicon.

Power devices need to provide fail-safe (normally-off, enhancement mode) operation. The strong piezoelectric and spontaneous polarisation effect causes

AlGaN or InAlN based GaN transistors to exhibit a negative threshold voltage (i.e. need to provide negative gate bias to turn them off) [5]. This makes normally-off operation challenging.

InAlN can be grown lattice matched to GaN, thus reducing wafer strain when epitaxially grown, improving surface morphology and potentially decreasing defect density. The large difference between the spontaneous polarisation of GaN and lattice matched InAlN (~0.044 C/m^2) introduces channel electron densities in the excess of 10^{13} cm^{-2} [6]. Larger channel electron density can allow for higher HEMT current density and lower sheet resistance. If AlGaN is inserted as an interlayer between InAlN and GaN channel, electron mobility can be increased [7]. For AlGaN/GaN heterostructures, the critical AlGaN barrier thickness below which a 2DEG is not inherently present is around 4-6 nm for $Al_{0.25}Ga_{0.75}N$ [8]. Devices making use of an ultra-thin AlGaN barrier have been previously demonstrated and require a gate overlapping the area between the drain and source contacts for operation. Breakdown voltage of these devices is limited to the dielectric strength, because the gate to drain contact distance is minimal. With regards to the substrates, the utilisation of silicon substrates is necessary for future large scale production and cost reduction.

1.2 Thesis Outline

This work summarises the efforts focused on evaluating custom designed growth material platforms, based on InAlN/AlGaN/GaN on Si substrates, and developing novel process modules for power transistor fabrication. This thesis is structured as follows.

Chapter 2 will provide background information on the material properties of group III-nitrides, their advantages and disadvantages and compare them with competing materials for power transistor fabrication. The formation of 2-dimensional electron gas (2DEG) during heteroepitaxy, the influence of charge transport on the transistor operation and its control via metal-semiconductor junctions will be discussed. An initial linkage between device performance and transistor design will be presented in a qualitative manner to provide a context for results shown in the following chapters. Important device metrics, such as threshold voltage, breakdown voltage, on-resistance, and transconductance will

be derived. Finally, some key application areas suitable for group III-nitride based HEMT will be summarised.

In Chapter 3, attention will be paid on the device fabrication processes used along with a brief description of the operation of the tools employed in the cleanroom. Also, the methodologies and practices for electrical characterisation of different structures (such as Van der Pauw, circular and linear TLM, transistors) will be presented. The measurement apparatus used will be briefly described.

In Chapter 4, a review of the most common fabrication techniques, which enable enhancement mode operation in GaN based transistors, will be presented along with the challenges faced when realising each approach.

In Chapter 5, focus will be placed on depletion mode InAlN/AlGaN/GaN HEMTs on silicon substrates. Firstly, a description of the design goals and the proposal of associated material and device structures will be presented. Following this, the specific processes and the characterisation outcomes derived from test structures fabricated on these materials will be summarised. This includes parametric studies on carrier transport properties, ohmic and gate contacts, buffer leakage measurements, dielectric films, and device geometries.

In Chapter 6, different process modules for achieving a positive threshold via recess etching will be presented. The aim being to remove the top InAlN barrier but maintain the AlGaN barrier. The relative advantages and disadvantages of each method will be analysed. Characterisation of enhancement (e-mode) devices fabricated using these techniques will be shown.

In Chapter 7, transistor data extracted from fabricated AlGaN/GaN materials will be presented. Characterisation data extracted from low temperature annealed ohmic contacts suitable for these structures will be shown. Ohmic contact evaluation on normally-off material has not been previously standardised or extensively researched, especially on GaN related materials. For this reason, gated TLM structures were fabricated and measurements were taken under different bias conditions to investigate their impact on sheet and contact characteristics.

In Chapter 8, the main experimental findings will be summarised and discussion will be initiated on research areas which can be investigated in the future.

2 Group III-Nitride HEMT Principles

This chapter aims to provide an introduction to the structural and electrical properties that enable III-nitrides to be suitable for the fabrication of power electronic switches. Key material parameters will be used to elucidate this. Background knowledge on the crystalline structure of GaN and the heterostructure formation when epitaxially grown with other alloys of the III-nitride system will be provided, as these, in combination, enable most of the favourable properties that are exploited in group III-nitride transistors. A brief summary of key semiconductor layer structures and description of their suitability for transistor operation will be presented.

2.1 Power Electronic Switches

Power electronic switches are classified with regards to their number of terminals, the type of charge carriers they employ and their degree of controllability. They comprise diodes, thyristors and transistors. Diodes are two terminal devices and their state is dependent on the circuit they are connected to, i.e. uncontrollable. Schottky diodes are majority carrier devices, whilst p-n diodes are minority carrier devices, i.e. current is controlled by the diffusion of minority carriers [9]. Thyristors are minority carrier three terminal devices that use multiple p-n junctions in series and can withstand very high voltages and conduct very high currents. Once turned on thyristors hold their fully on-state until manually reset, thus act as a semi-controllable electronic latch. Due to their high power handling capabilities, they are usually found in applications such as HV-DC electricity transmission systems. Finally, transistors are controllable three terminal devices. Field-effect transistors (FET) use one type of carriers for conduction, whereas bipolar transistors involve both holes and electrons. The insulated-gate-bipolar-transistor (IGBT) is a bipolar transistor that is designed by combining a bipolar junction transistor (BJT) and a FET.

The ideal power electronic switch can conduct current with zero-voltage drop across it in the on-state. In its off-state, zero-current passes through it and it can handle any voltage. However, in real life applications, the physical limitations imposed by the semiconductor material of choice compromise the electronic switch performance. There is a non-zero leakage current in the off-

state and the resistance (R_{on}) is non zero during on-state, as depicted in Figure 2-1. Both are major problems for power electronic applications. The next section will introduce an assessment of semiconductor materials with regards to their suitability for power electronics.

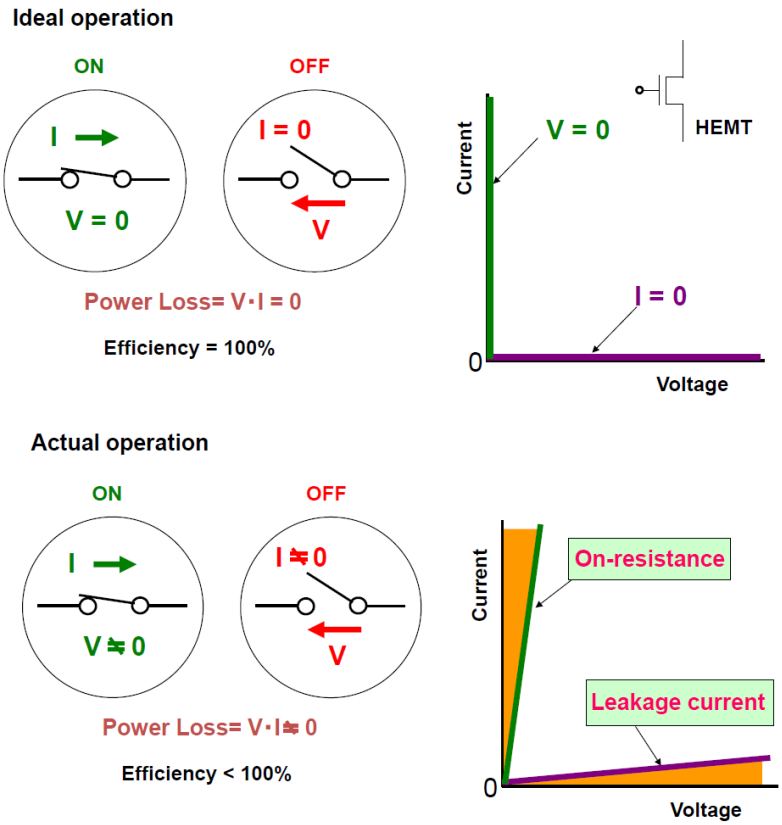


Figure 2-1: HEMT power switching operation [10].

2.2 Material Suitability for Power Electronic Applications

Two important parameters to assess the suitability of semiconducting materials in meeting specific performance targets are the lattice parameter and the energy bandgap. Well-structured periodically placed atoms form a crystal structure, with the smallest repeating arrangement of atoms being called a unit cell. The dimensions of the unit cell are characterised by the lattice parameter. Bandgap is a representation of the minimum energy required to excite an electron to a conduction permitting state.

In Figure 2-2, the relationship between bulk (equilibrium) lattice constant and energy bandgap for different semiconductors is displayed. Hexagonal and cubic crystal structure semiconductors can be directly compared in terms of the

atomic bond length parameter, which denotes the average spacing between the nuclei centres of two bonded atoms in the molecule using a geometrical transformation relationship [11]. The III-V nitride semiconductors possess small bond length between atoms compared to silicon and can be grown to possess bandgap energies as high as 6 eV [12]. In III-N materials, a small bond length is the result of strong bonding energy between neighbouring atoms in the crystal structure and the subsequent very high chemical stability arising from the light effective mass of nitrogen [11]. The high bonding energy and low mass lead to large phonon energy, so lattice scattering is minimal [13]. Consequently, high saturation drift velocity and high thermal conductivity are observed. High thermal conductivity of the materials involved enables dissipated power to be conducted efficiently.

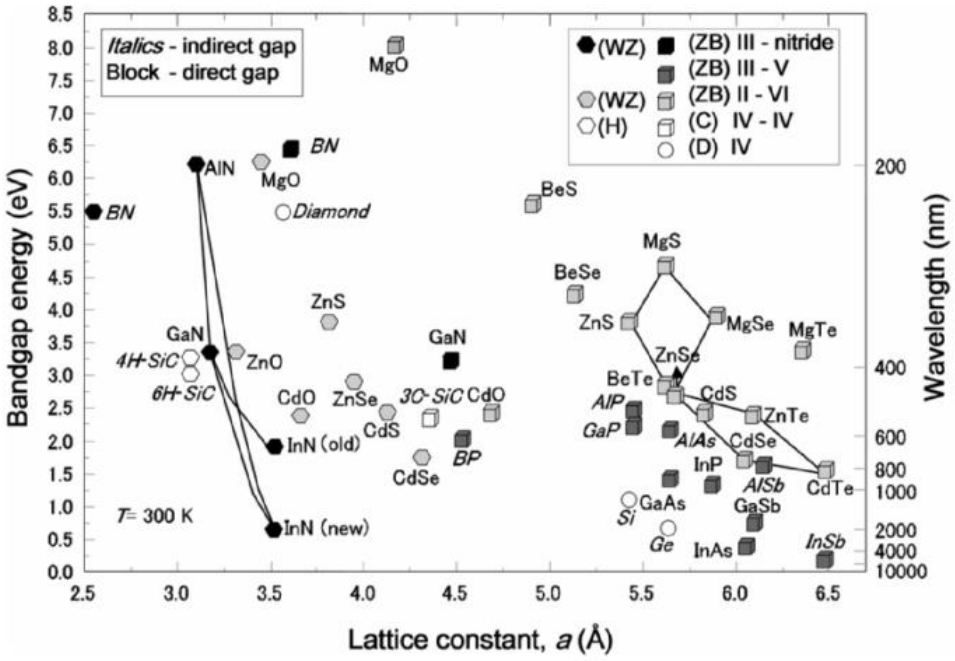


Figure 2-2: Relationship between bandgap and lattice constant for semiconductor materials. Cubic and hexagonal crystal structures are represented with square and hexagon symbols [11].

Large bandgap energy (E_g) and high critical electrical field (E_c), which is the minimum electric field at which avalanche breakdown effect occurs, allow for high voltages to be sustained. The high breakdown strength of GaN requires shorter drift regions for a given blocking voltage compared to Si or SiC, thus reducing the specific on-resistance ($R_{on,sp}$) and the minority carrier storage [14].

During switching operation, a device alternates between the low impedance on-state, when a plurality of carriers flows through it and the high impedance off-state which is characterised by the blocking of carriers through the channel. Lower levels of minority carrier injection signify that the transition from the on-state to the off-state can be achieved faster, because minority carriers need to be removed from the voltage blocking region during off-state. As a result, switching losses are reduced, enabling higher switching frequencies and allowing a reduction in weight and size of the passive components in power switches. Large bandgap energy also lowers the intrinsic carrier generation at high temperatures, which subsequently reduces thermally induced leakage current [13].

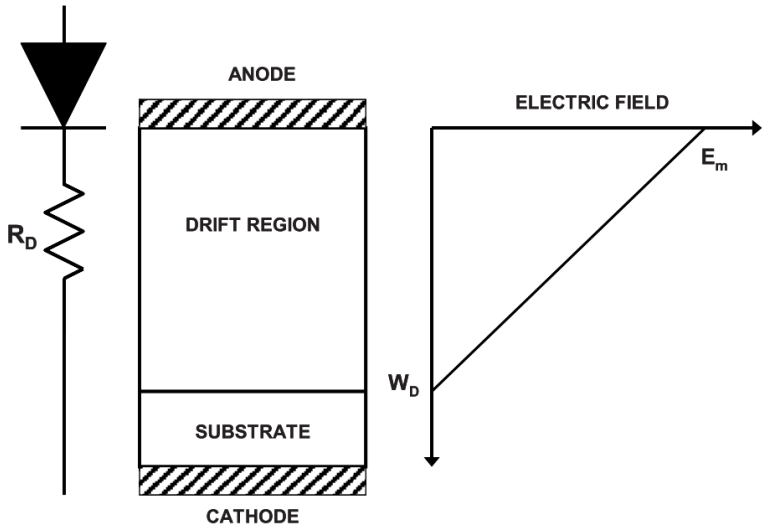


Figure 2-3: Ideal drift region and electric field distribution [15].

To theoretically illustrate the trade-off relationship between device on-resistance and breakdown voltage through the employment of different semiconductors, a lightly doped drift region to sustain the device off-state voltage can be assumed. As seen in Figure 2-3, distribution of electric field is linear along the drift region with its slope being dependent on the doping concentration. The drift region can support a maximum blocking voltage that is correlated with the semiconductor critical electric field. The reverse bias blocking voltage and the maximum electric field that can be sustained are given by:

$$V_B = \frac{E_{max} W_D}{2} \tag{2-1}$$

$$E_{max} = \frac{q N_D W_D}{\varepsilon_s} \tag{2-2}$$

where W_D is the depletion width noted in Figure 2-3, i.e. the semiconductor region depleted of free carriers to sustain the blocking voltage, N_D is the drift region doping concentration and ε_s is the semiconductor dielectric constant.

As E_{max} reaches the critical electric field E_c, impact ionisation leads to significant carrier generation and avalanche breakdown in the depletion region. At this condition, blocking voltage V_B is the device's breakdown voltage B_V and Eq. (2-1) and (2-2) become:

$$B_V = \frac{E_c W_D}{2} \tag{2-3}$$

$$E_c = \frac{q N_D W_D}{\varepsilon_s} \tag{2-4}$$

A maximum depletion width can be derived as a function of the critical electric field and doping concentration by rearranging Eq.(2-3).

$$W_D = \frac{2 B_V}{E_C} \tag{2-5}$$

The drift region doping concentration required to obtain breakdown voltage can be obtained by solving Eq. (2-4) and (2-5):

$$N_D = \frac{\varepsilon_s E_c^2}{2q\, B_V} \tag{2-6}$$

The ideal drift region resistance R of area A satisfy:

$$R\, A = \int_0^{W_D} \rho(x) dx = \int_0^{W_D} \frac{dx}{q \mu_n N_D(x)} \tag{2-7}$$

The ideal resistance per unit area (specific resistance) of the drift region is calculated by substituting Eq. (2-5) and (2-6) into (2-7):

$$R_{on-ideal} = \frac{W_D}{q\mu_n N_D} = \frac{4{B_V}^2}{\varepsilon_s \mu_n {E_c}^3} \tag{2-8}$$

In 1983, Baliga derived the above relationship that relates the on-resistance (per unit area) of an ideal semiconductor drift region and its breakdown voltage [15]. The denominator $\varepsilon_s \mu_n {E_c}^3$ is the Baliga's figure of merit (BFOM), which indicates the impact of the material properties on the drift region resistance. It is a useful metric for benchmarking power semiconductor materials. Higher BFOM values are desirable, so semiconductors that reach high channel carrier mobility values are favoured. Moreover, the cubic dependence on the critical electric field is indicative of the preference for wide bandgap semiconductors for power switching applications.

A summary of a key metric comparison between GaN and other power semiconductor materials can be found in Table 2-1.

Table 2-1: Electrical properties of semiconductor materials. Adapted from [16] and [17].

	Metric					
Material	**Bandgap (eV)**	**Critical electric field (MV)**	**Electron Mobility (cm^2/Vs)**	**Electron Saturation Velocity (x 10^7 cm/s)**	**Thermal conductivity (W cm^{-1} K^{-1})**	**Baliga FOM (normalised to Si)**
Si	1.12	0.3	1350	1.0	1.5	1
GaAs	1.42	0.4	8500	2.0	0.5	17
SiC-4H	3.26	2.0	720	2.0	5.0	134
GaN	3.44	3.0	2000	2.5	1.3	537

From Table 2-1, the higher GaN BFOM can lead to a theoretical improvement of a factor of 537 compared to Si-based device performance. GaN performance can be further enhanced by utilising the ability to form heterostructures with Al- and In- based nitride compounds, such as AlN. The resulting 2-Dimensional Electron

Gas (2DEG) formed at the interface of the heterojunction can further enhance the majority carrier mobility. This in turn decreases $R_{on,sp}$ and the switching losses in power switches are further decreased, thus reducing the passive component size and weight. In the next sections, the structure of group III-nitride materials resulting from material growth as well as the 2DEG formation process between a wider bandgap (such as AlGaN) and a narrower, in comparison, bandgap material (GaN) will be described.

2.3 Group III-Nitride Crystal Structure

III-nitride materials crystallise in either hexagonal "wurtzite" or cubic "zincblende" structure. The wurtzite structure can be analysed as two interpenetrating hexagonal close-packed lattices consisting of group III atoms and nitrogen, having tetrahedral arrangement of four equidistant closest neighbours. The nitrogen atom's $1s^2 2s^2 2p^3$ electronic configuration and the lack of electrons occupying the outer orbitals lead to strong Coulomb potential in the III-nitride covalent bond. Thus, nitrogen atom's electronegativity leads to iconicity in the III-nitride covalent bond and local charge dipoles are formed [18]. The centres of positive and negative charges from the ionicity of the Ga-N bond are displaced from each other. Therefore electric charges appear at the opposite surfaces of the crystal, which manifest as spontaneous polarization macroscopically, because the wurtzite crystal lacks inversion symmetry [19].

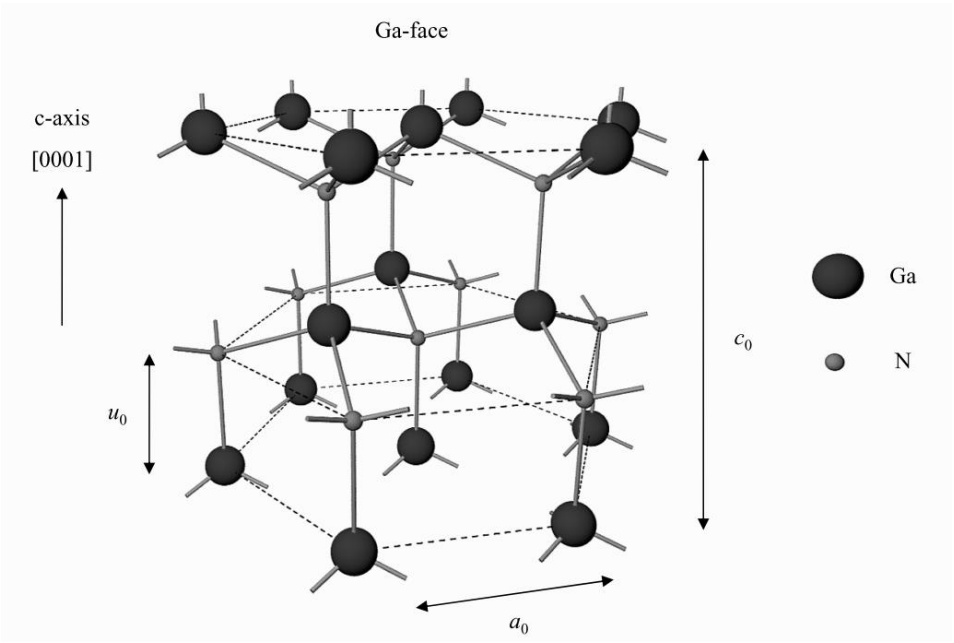


Figure 2-4: Ga- face GaN wurtzite crystal atom arrangement [20].

The zincblende structure employs two interpenetrating face-centered cubic lattices, similar to diamond structure but with different sublattice atoms. Overall, the higher thermodynamic stability of wurtzite makes it the preferable crystal structure for use in power applications.

2.4 AlGaN/GaN Heterostructure 2DEG Formation

A basic HEMT structure and a simplified layer structure can be found in Figure 2-5. The metal-to-semiconductor contacts are placed on top. The heterostructure is formed between a wider and a narrower band gap material and in the bottom there is a semi-insulating substrate (eg. Si or SiC). Shown in Figure 2-2, the direct bandgap energy of the group III-nitride system can range from 0.7 eV (InN), 3.4 eV (GaN), to 6 eV (AlN). The element mole fractions in the crystal can be adjusted during epitaxial material growth, so that ternary alloys (AlGaN, InAlN and InGaN) are synthesised. The alloy bandgap and crystal lattice parameters can be selected according to their dependence on the element compositions, resulting in fine-tuned properties.

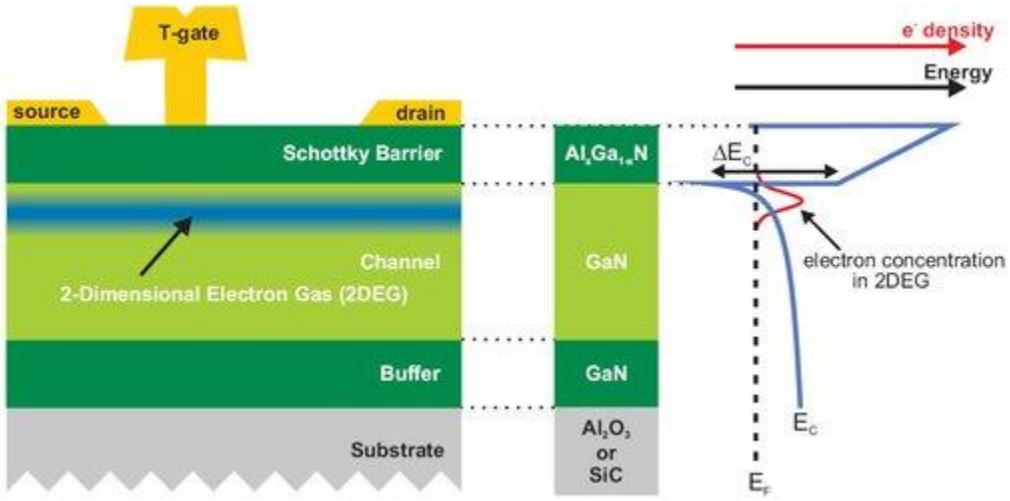


Figure 2-5: GaN HEMT structure and associated band diagram [21].

Using the AlGaN/GaN heterostructure as example, the 2DEG is formed as follows. When the heterojunction is grown, the electrons of donor impurities in the AlGaN barrier move towards the GaN layer to minimise their energy. As a balance between the Fermi levels of the two materials gets established, the quasi-triangular quantum well is formed at the GaN side of the interface, where electrons can be confined.

As mentioned in Section 2.3, the Ga and N atoms possess different electronegativity which causes every bond between them to be partially ionic and with a certain dipole moment. In wurtzite crystal structures, the bonds along the c-axis have a different length than the bonds which are nearly perpendicular to the c-axis, hence a net dipole moment along the c-axis is created. As a result, one face of the GaN or AlGaN crystals gets positively charged, whilst the opposite face becomes negatively charged. This polar nature gives rise to spontaneous polarisation (Figure 2-6a). Furthermore, there is tensile stress present near the heterojunction interface due to the different lattice constants of GaN and AlGaN crystals. A static charge and a built-in polarisation field in the barrier layer are created [22]. This is called piezoelectric polarisation and has the same direction as the spontaneous polarisation (Figure 2-6b). The two fields cause an induction of a net positive charge at the heterostructure interface, thus forming a polarisation dipole (Figure 2-6c). The 2DEG electrons likely originate from donor-like states near the top of the AlGaN barrier layer [23]. To generate the final charge distribution, a complementary opposing dipole is required. This dipole contains the 2DEG and a thin channel of hole-gas at the top of the barrier layer (Figure 2-6d).

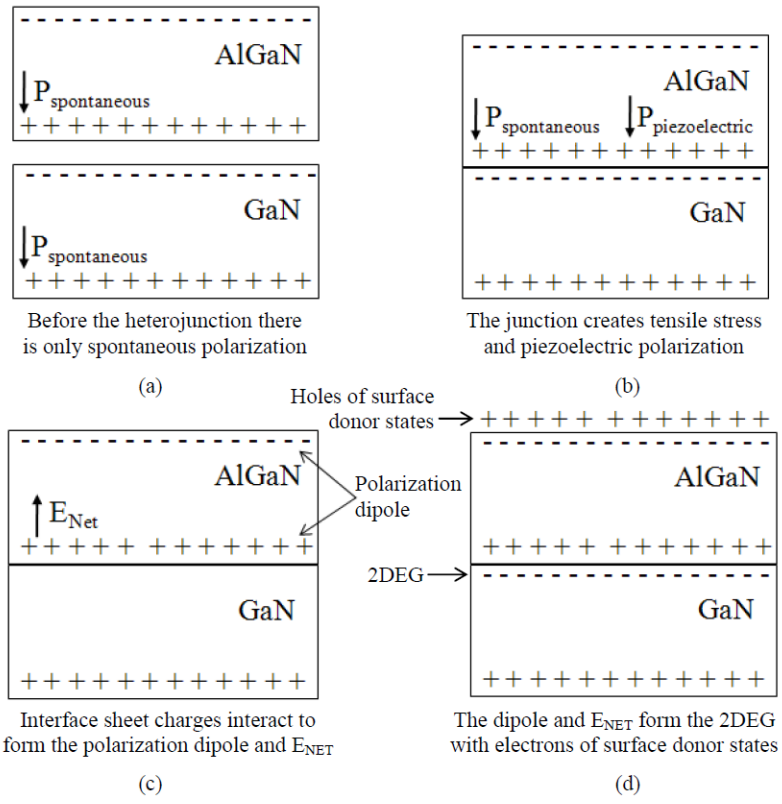


Figure 2-6: 2DEG formation process [24].

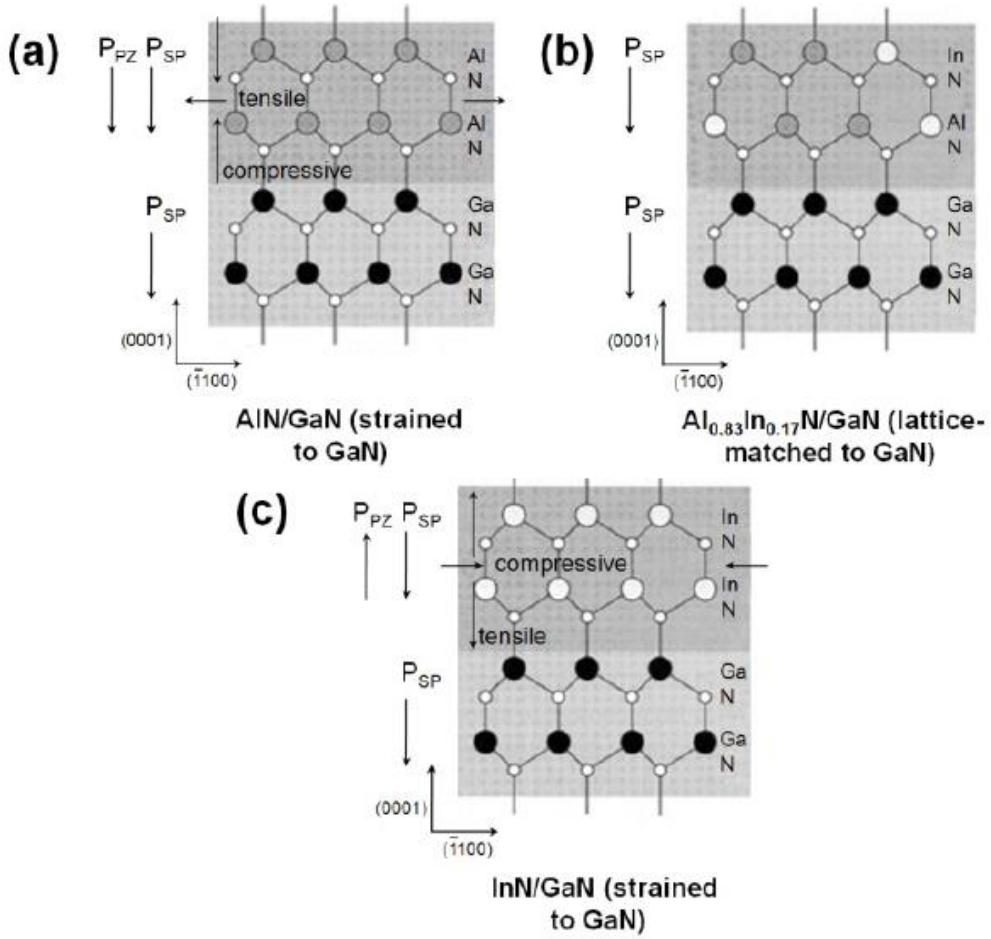


Figure 2-7: Direction of polarisation for (a) AlN/GaN, (b) lattice matched InAlN/GaN and (c) InGaN/ GaN [24].

2.5 GaN-on-Semiconductor Heteroepitaxial Growth

As mentioned earlier, GaN greatly benefits from the viability of heteroepitaxial growth [25]; it is possible to grow GaN substrates on non-GaN substrates, therefore it is viable to fabricate devices utilising established GaAs, Si or other material process lines. In contrast, native GaN substrates are still very difficult to fabricate and they are very limited in sizes at this stage.

Heteroepitaxial growth is mainly focused on growing GaN-based substrates on silicon carbide (SiC), sapphire (Al_2O_3) or silicon (Si). The first advantage of using silicon carbide is that its lattice mismatch with GaN is very low, so growth of GaN-on-SiC is relatively easier compared to GaN-on-Si. Another advantage is its great thermal conductivity (Table 2-1), as maintaining low temperature (being able to sufficiently transfer the generated heat out of the device) is very important in power electronics. On the other hand, its cost is high.

The lattice mismatch of sapphire is compressive relative to GaN (results in a compressed epilayer). This means the chance of growth resulting in a cracked epitaxial layer is significantly lower when using sapphire substrate. Its disadvantages are that its thermal conductivity is relatively low (κ ~ 0.3 W cm^{-1} K^{-1} [26]) and substrate costs are significantly higher than silicon (but lower than silicon carbide).

Silicon has long history of growth optimisation, which allows large wafer sizes to be grown and can be used as substrates on which GaN-based heterostructures can be produced. It has reasonable thermal conductivity κ ~ 1.5 W cm^{-1} K^{-1}, though much lower than silicon carbide. Growth of excellent quality wafers is challenging though due to high lattice mismatch with GaN, although nowadays 8" GaN-on-Si wafers have been demonstrated [27]. The viability of integrating GaN growth into standard Si process lines, which allow wafer production at a very small cost per unit area have made devices built on GaN-on-Si wafers highly preferred for most applications. A future projection of GaN epitaxial wafer market share is presented in Appendix A.

2.6 GaN HEMT Layer Structures

A GaN based HEMT cross section indicating the 2DEG is depicted in Figure 2-8. The current path is from the source terminal through the 2DEG region to the drain electrode. The source and drain contacts are ohmic to the 2DEG. The gate contact is a rectifying contact that can accumulate or deplete electrons in the channel underneath it, thereby changing the channel resistance and switching the device on and off. As a result, the HEMT current modulation is dependent on the modulation of the 2DEG channel's carrier concentration.

The layer structure is based on the AlGaN/GaN heterostructure grown on a Si substrate. The nucleation layer(s) is incorporated to suppress high leakage currents that are due to high applied electric fields and can extend to the substrate materials, thus providing breakdown voltage enhancement. The buffer layer(s) provides strain relief by reducing the dislocation density due to the different lattice constants between substrate and GaN channel layers. They are followed by the GaN channel layer. The GaN layer is n-doped unintentionally to

a typical concentration between 10^{14} cm^{-3} and 10^{16} cm^{-3} due to impurities during material growth (e.g. defects, contamination, O, Si).

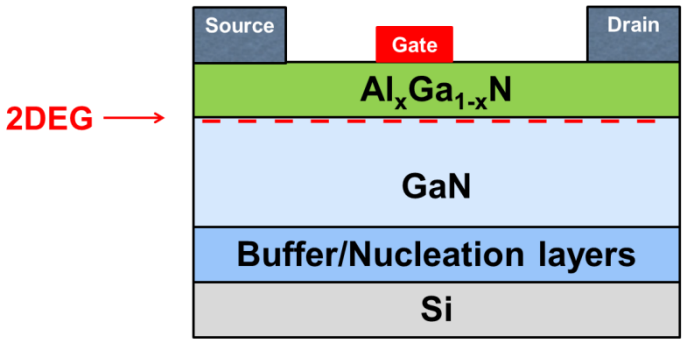


Figure 2-8: Layer structure of generic AlGaN/GaN HEMT.

The AlGaN layer supplies mobile electrons to the 2DEG. An increase in AlGaN n-doping can raise the 2DEG electron density n_s, but also decreases electron mobility and deteriorates the gate leakage characteristics of Schottky gate type devices. The Al mole fraction x in $Al_xGa_{1-x}N$ also affects the channel mobility and carrier concentration levels.

An aluminium mole fraction in AlGaN between 20 and 30% offers a good balance between high mobility and carrier concentration [28]. Higher Al content increases 2DEG channel carrier concentration and leads to better carrier confinement, but carrier mobility decreases due to elevated levels of alloy scattering. In contrast, for Al mole fractions lower than 20%, mobility is similar however sheet charge decreases.

The AlGaN layer thickness also plays a role in the heterostructure characteristics. Brown (2015) conducted a theoretical study about the effect that a variation of aluminium concentration as well as the barrier thickness has on the AlGaN/GaN channel carrier concentration [29]. There is a critical value of AlGaN thickness, which is the maximum allowed AlGaN thickness required to achieve a positive threshold voltage, i.e. enable normally-off or enhancement mode operation. In order to increase the critical barrier layer thickness, the Al composition should be lowered [30]. These properties were used in the design of heterostructures suitable for providing the HEMT threshold voltage characteristics, as will be discussed in later chapters.

The gate barrier height can get tuned by adjusting the material compositions of the layers above AlGaN. A GaN capping layer (shown in Figure 2-9) above AlGaN can be placed to increase the Schottky gate barrier, thus reducing the gate leakage current and also heal surface homogeneities and passivate the semiconductor surface [25]. Another benefit of using a GaN cap layer is the prevention of oxidation of the AlGaN layer [31].

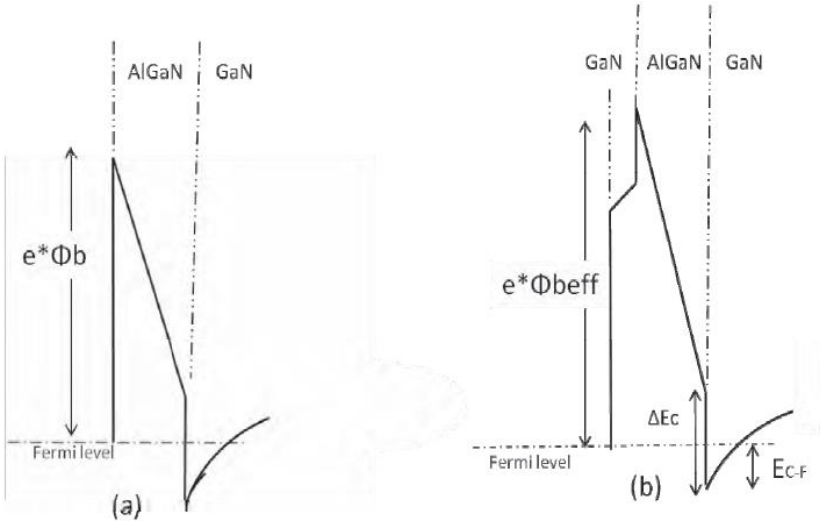


Figure 2-9: Effect of GaN capping layer on the gate Schottky barrier [32].

The surface of the semiconductor can be a source of device current collapse, i.e. drain current reduction, through donor-like surface states which capture and release charge (Section 2.10). Hence, a surface passivation dielectric film can be used to improve some HEMT characteristics. The type of the dielectric and the deposition method may lead to some improved characteristics, such as reduced current collapse, but could deteriorate others, such as reduced breakdown voltage and larger gate leakage current [33].

As discussed in Section 2.2, the ability to sustain high voltages is limited by the avalanche breakdown phenomenon, which depends on the electric field distribution under operating conditions. The conventional metal-semiconductor gate contacts, as shown in Figure 2-8, possess potential weak points due to large electric fields being developed at the drain side of the gate that can cause early breakdown [34]. For this reason, extended gates on top of the dielectric layer on the drain side can be used, called gate field plates [35]. These structures reduce

the peak electric field at the gate edge (from the drain side) caused by high drain voltages, by spreading the voltage drop across a larger area (Figure 2-10).

Due to the higher polarisation of InAlN compared to AlGaN, the critical value of InAlN thickness required to achieve enhancement mode operation is lower in InAlN/GaN compared to AlGaN/GaN heterostructures. Simulations have estimated the InAlN critical barrier thickness to be 2nm in $In_{0.18}Al_{0.82}N$/GaN heterostructures [36] and 4-6 nm in $Al_{0.25}Ga_{0.75}N$/GaN heterostructures [29].

The presence of a large number of structures on each semiconductor sample for large die-per-wafer (DPW) usage creates the need for each fabricated device to be substantially electrically isolated from adjacent structures. For this reason, a mesa etch is used to remove the most conducting parts of the material from the area in between these structures. As with every other pattern definition, mesa etch is defined by lithographic processes that will be described in Chapter 3.

By taking into account the considerations mentioned in the last paragraphs, a slightly different layer and device structure to fit the high power operation criteria can be derived.

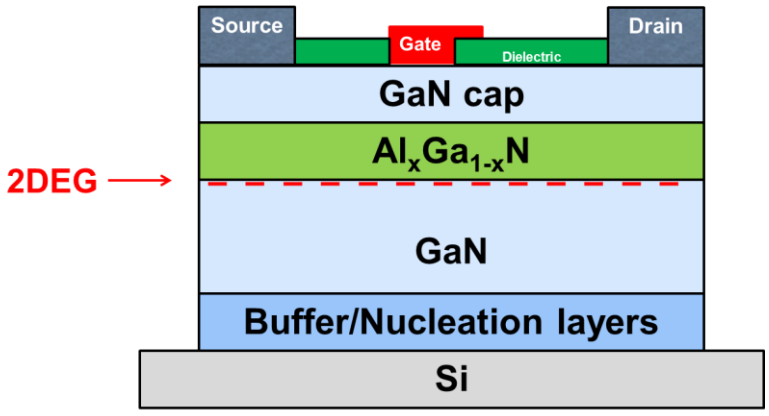


Figure 2-10: High voltage AlGaN/GaN HEMT layer structure.

In order to improve or adjust the performance of GaN based HEMTs to meet certain performance criteria more complicated band structures can be utilised by inserting new layers or modifying material compositions or geometrical characteristics [20]. The overall principles of designing the layer structures however remain the same.

To summarise, the transistor structure areas can be analysed in a qualitative manner with respect to the performance metrics they primarily affect:

- Source and drain ohmic contacts: Required to demonstrate good ohmic (linear) behaviour with low resistance. Surface should be smooth. High mechanical and thermal stability are also required. Their performance primarily affects device on-resistance.

- Gate contact: To allow very low gate and drain leakage currents and provide high breakdown voltage and stable threshold voltage. Gate resistance should be low. Metal adhesion as well as thermal and mechanical stability should be excellent.

- Surface passivation dielectric: To minimise surface leakage current and current collapse phenomena. Also, to lower the device on-resistance if possible, by decreasing semiconductor sheet resistance. The dielectric should sustain high voltages to prevent drain- gate field plate region breakdown.

- Gate (and possibly source) field plates: To increase breakdown voltage by reducing the peak electric field at the gate edge (from the drain side) caused by high drain voltages.

- Gate dimensions: Gate area should cover any possible conduction route between the drain and source contacts, so that the device can be switched off. Gate length should be minimal to minimise gate capacitance that can affect switching speed, but at the same time be capable of withstanding high bias stresses. Yield after lithography processing should be excellent, as it is typically the smallest defined transistor feature. Gate width should be sufficient to support the specified device current rating. This can lead to very large HEMT footprints if the conventional single gate finger approach is followed. In contrast, power density can be increased and gate resistance can be reduced if a multi-finger gate design is implemented instead (Figure 2-11). Due to the multi-finger

configuration compact design, heat dissipation issues such as thermal crosstalk between gate fingers can become apparent [22].

- Gate to drain distance: To provide high breakdown voltage without significantly compromising on-resistance. The critical electric field of GaN (~3MV/cm) should not be surpassed under operation, otherwise the device will exhibit breakdown.

- Mesa etching: To electrically isolate the active devices on the wafer, by greatly increasing the resistivity of the semiconductor material between them. Etched surface should be uniform and smooth to minimise leakage effects. Etch chemicals used should not form conductive compounds on the etched surface or with any passivation films.

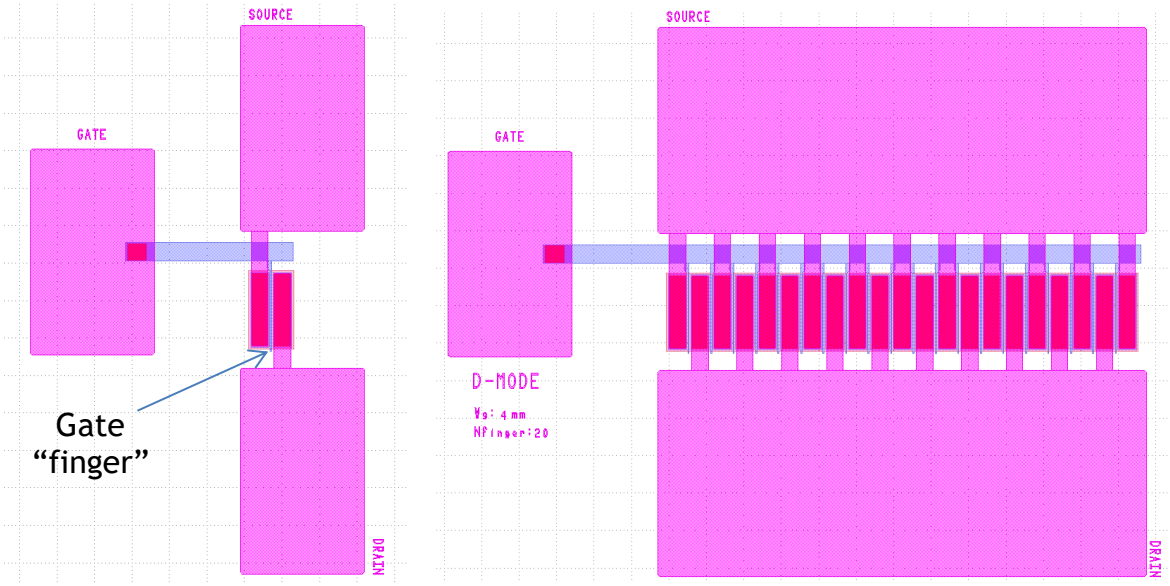


Figure 2-11: Single finger gate and multi-finger gate type device mask layout.

2.7 GaN HEMT Operation Principles

The drain-to-source current vs drain-to-source voltage characteristic of a depletion mode transistor biased in the common source configuration is shown in Figure 2-12. The source is connected to a common terminal, gate is the input and the output terminal is connected to the drain. The gate’s input signal can control the resistivity of the GaN channel, hence switching the device on and

off. These characteristics are obtained through the sweeping of drain-to-source voltage whilst gate-to-source voltage is kept constant for each sweep step.

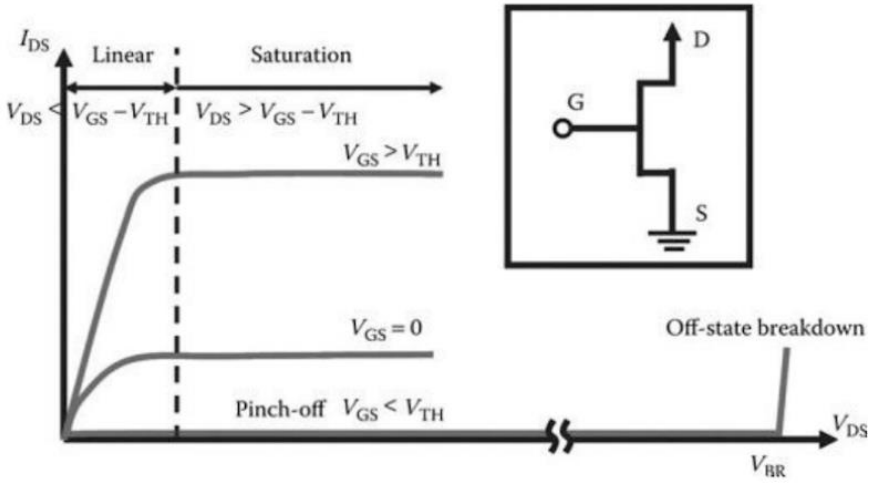


Figure 2-12: Drain-to-source current vs drain to source voltage characteristics of a depletion mode AlGaN/GaN HEMT in common source configuration [37].

Since the AlGaN/GaN HEMT is an electron majority carrier controlled device, a more negative gate voltage than the device threshold voltage can deplete the 2DEG region under the gate from carriers, hence obstruct the source-drain electron flow and turn the device off.

The conduction band profile of the AlGaN/GaN heterojunction is shown in Figure 2-5. The sheet carrier density, n_s, with applied gate-to-source potential V_{GS} can be obtained by a self-consistent solution of Poisson's and Schrodinger's equations in the quantum well [38]:

$$n_s = \frac{\varepsilon_{AlGaN}}{q d_{AlGaN}} (V_{GS} - V_{th}) \tag{2-9}$$

where d_{AlGaN} and ε_{AlGaN} are the AlGaN barrier layer thickness and permittivity respectively. V_{th} is the heterostructure threshold voltage, which is expressed as [39]:

$$V_{th} = \varphi_B - \Delta E_C - \frac{q n_s}{\varepsilon_0 \varepsilon_{AlGaN}} d_{AlGaN} \tag{2-10}$$

where φ_B is the Schottky barrier height and ΔE_C is the heterojunction conduction band discontinuity between GaN and AlGaN.

When $V_{GS} \leq V_{th}$, no 2DEG carriers are present and the device is kept in off-state. When $V_{GS} > V_{th}$, 2DEG is present. The device channel starts accumulating electrons and current flows between the source and drain contacts under drain bias. For $V_{DS} < V_{GS} - V_{th}$, the device is operating in the linear region, where an increase in the drain-to-source voltage leads to a linear increase in drain-to-source current. The linear region current is expressed by [37]:

$$I_{D-lin} = qn_s v_{eff} W_G \tag{2-11}$$

where v_{eff} is the effective 2DEG electron velocity and W_G is the gate width.

The electron velocity in the channel depends on the electric field applied and their mobility:

$$v = \mu_n E \tag{2-12}$$

where μ_n is the electron mobility and E is the applied electric field.

Scattering effects reduce mobility and will be discussed later in this chapter. As the applied electric field increases with increased drain-to-source biasing conditions, carriers gain sufficient energy to be scattered by optical phonons, resulting in a decrease of their mobility [40]. Eventually, when $V_{DS} > V_{GS} - V_{th}$, the electron velocity becomes independent of the applied electric field and saturates. As the drain voltage increases the lateral bias under the gate depletion region pinches the channel off at the gate edge. The pinch point limits the source-to-drain carrier number due to the continuously constricted channel width and the current saturates. This long channel model is valid for the devices that will be under investigation.

The saturation current is approximated by [38]:

$$I_{D-sat} = \frac{\mu CW}{2L}(V_G - V_{th})^2 \tag{2-13}$$

where L and W are the gate length and width respectively and C is the gate capacitance.

The HEMT transconductance is the ratio of the relative change of drain current to the relative change of gate-to-source voltage, i.e.

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const} = \frac{\mu CW}{L}(V_{GS} - V_{th}) \tag{2-14}$$

Since the gate capacitance is;

$$C = \frac{\varepsilon_0 \varepsilon_{AlGaN} WL}{t_{AlGaN}} \tag{2-15}$$

the separation between the gate and the channel t_{AlGaN} can affect the HEMT transconductance, with smaller gate-channel distances increasing its value if the other parameters are constant.

System safety in a potential gate driver malfunction can be ensured be higher through the use of normally-off transistors. Referring to Eq. (2-10), three ways of obtaining a positive threshold voltage are by increasing the work function of the gate metal, by lowering the channel carrier concentration through reducing Al mole fraction and by reducing the barrier thickness. These properties will be investigated in more detail in later chapters.

The off-state breakdown voltage is defined as the voltage when the drain current reaches 1 μA/mm at the off-state condition (when $V_{GS} < V_{th}$).

In the next sections, a closer look will be taken on metal-semiconductor junctions and their role in HEMT performance.

2.8 Metal-Semiconductor Junctions

Metal-semiconductor junctions can be either ohmic or Schottky, depending on the semiconductor work function with respect to the metal. When metal and semiconductor come into contact, the Fermi levels must align at equilibrium according to Anderson's rule [41]. As carriers reach the junction under an applied electric field linear conduction (ohmic) or rectification (Schottky) is observed. Ohmic contacts are generally used for low resistance access region carrier paths, even though Schottky source contacts have seen situational use to allow for high breakdown fields with the unavoidable consequent maximum current and on-resistance compromise [42]. Schottky contacts are utilised as gate contacts to control the channel current flow using a field-effect and simultaneously minimise charge flow through the gate terminal under any biasing conditions.

2.8.1 Schottky Contacts

If the metal work function is greater than the semiconductor work function a Schottky junction is formed. Gate contacts on transistors can be formed by the deposition of metals with high work function. Transistor gates can be modelled as capacitors when they are biased. They locally deplete the semiconductor under the gate, therefore obstructing the flow of charge between the drain and source contacts. Taking as an example the classical representation of a Schottky contact on n-type semiconductor in Figure 2-13, electrons in the conduction band of the semiconductor can move to the unoccupied energy states above the metal Fermi level. The resulting positive net charge on the semiconductor side and the net negative net charge on the metal side lead to a contact potential. Some degree of Fermi level pinning can also be present shifting the contact built-in potential accordingly.

In contrast to metal-to-metal contacts where charges reside on surfaces due to high electron density found in metals, in metal-to-semiconductor contacts electrons are removed from the surface as well as a certain depth of the semiconductor, hence a depletion region of a certain width is formed. The depletion region causes bending of the energy bands on the semiconductor side

as the metal-semiconductor Fermi levels line up. Energy bands bend in the direction of the electric field, as shown in Figure 2-13.

High work function metals are typically used as gate metals in direct contact to GaN in order to obtain a large Schottky barrier height. Most typical gate metal is Ni, which enables a useful combination of high work function and good adhesion to GaN. Oxidation prevention and low gate resistance can be achieved through the incorporation of Au on top of Ni.

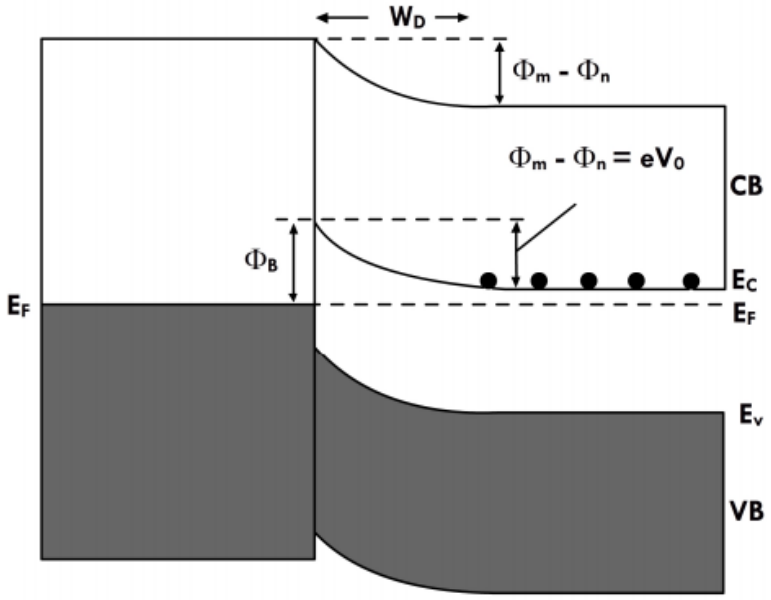


Figure 2-13: Schottky metal-semiconductor junction. Semiconductor work function is smaller than metal work function, resulting in electrons moving to metal forming a contact potential [43].

Transistor gate leakage levels should be as low as possible, as it degrades its power efficiency. The dominant physical mechanisms that dictate gate leakage are dependent on temperature, biasing conditions, polarisation effects, defect states and may be device specific [44]. An overview of the possible carrier transport mechanisms across a Schottky barrier can be found in Figure 2-14(a-c). Gate dielectrics, such as SiO_2, Al_2O_3, SiN_x, HfO_2, can be used to mitigate gate leakage problems, which in turn give rise to additional emission and tunnelling processes through the insulator barrier (Figure 2-14d).

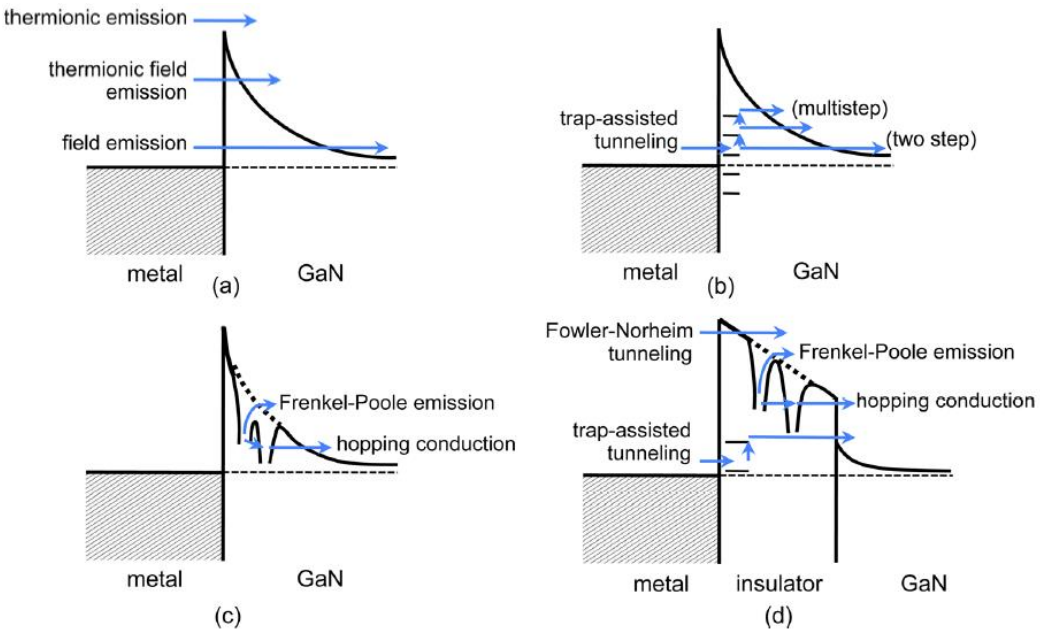


Figure 2-14: Possible metal-semiconductor (a-c) and metal-insulator-semiconductor gate leakage mechanisms [44].

2.8.2 Ohmic Contacts

Source and drain ohmic contacts, as the name suggests, follow ohmic (linear) current-voltage behaviour. They are used to provide a low resistance path between the electrode and the semiconductor below. A theoretical n-type ohmic contact band diagram is depicted in Figure 2-15.

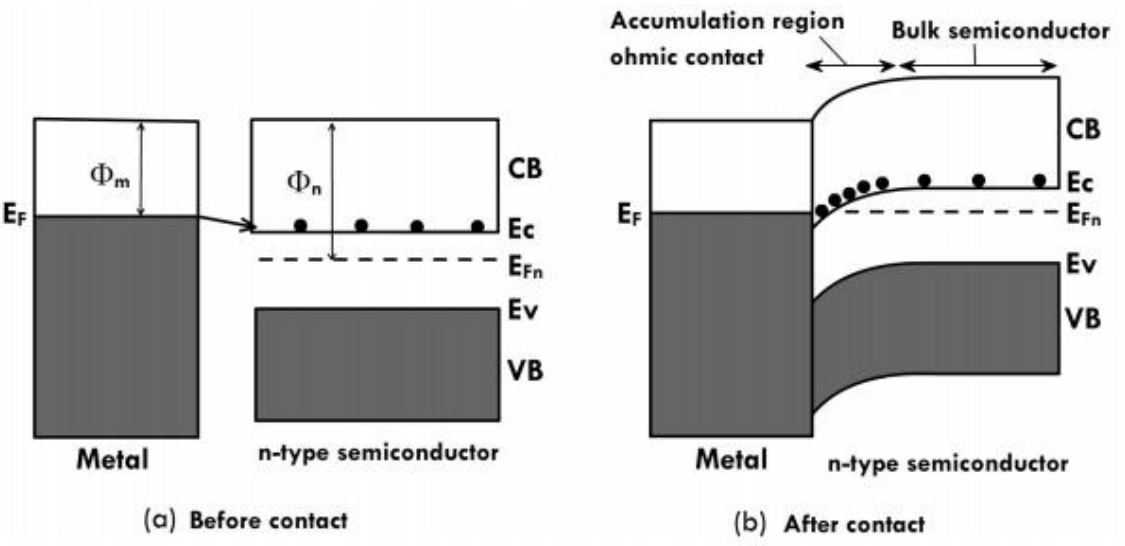


Figure 2-15: Ohmic contact on n-type semiconductor band diagram. Shown (a) before and (b) after contact [43].

The semiconductor possesses a greater work function than the metal. At equilibrium, an accumulation region is formed close to the interface on the semiconductor side due to the transport of electrons from the metal, which fill empty states in the semiconductor conduction band. The accumulation region's higher electron density, when compared to the bulk semiconductor, results in increased conductivity and the ohmic junction equates to a resistor, which conducts in both forward and reverse bias. This realisation is not very practical for ohmic contact stack formation on GaN based heterojunctions due to the barrier layer. Hence, annealing is required to take place in order to form ohmic contacts. Additional considerations need to be taken into account and are described below.

The majority of the ohmic contact metal stacks used for AlGaN/GaN based transistors are titanium/aluminium (Ti/Al) based, although there are always new proposed schemes. Ti has a work function of 3.83–4.33eV and it is very effective at forming low resistance ohmic contacts to AlGaN/GaN through the titanium nitride (TiN) "spike" mechanism which will be explained later. The work function of Al is 4.18eV [45], which is similar to the affinity of GaN. The formation of $TiAl_x$ alloy is reported to start at 660 °C and stabilises the contact, because it has a higher melting point than Al [46].

Al oxidises easily though, thereby gold (Au) can be used to prevent oxidation. Au also has very low bulk resistivity ($\rho_{Au} = 2.4 * 10^{-8} \Omega\, m$). In order to prevent indiffusion of Au and outdiffusion of Al, a thin metal layer with low bulk diffusivity is commonly used, resulting in a Ti/Al/metal/Au stack. Mohammed et al. (2006) tested different diffusion barrier metals and concluded that the lowest contact resistance was achieved using Ni or Mo or Pt [47].

Mohammed et al. (2007) reported two different mechanisms for ohmic contact formation on AlGaN/GaN based heterostructures. The first is carrier tunnelling, which is based on the outdiffusion of nitrogen from AlGaN/GaN and the subsequent creation of N-vacancies. The N-vacancies act as a heavily n-doped layer, which increases the tunnelling probability. In addition, the tunnelling probability increases by the consumption of AlGaN during the alloy reactions, because the barrier thickness decreases.

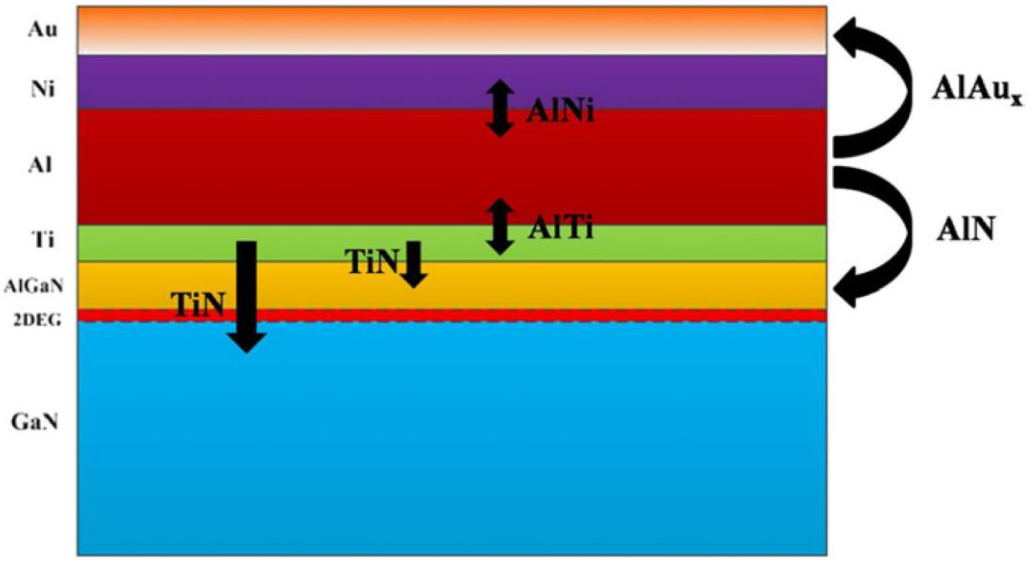


Figure 2-16: Ti/Al/Ni/Au metal stack reactions during Rapid Thermal Annealing (RTA) [48].

The second (and more effective) mechanism is the so called “spike” mechanism. TiN protrusions can penetrate through the AlGaN layer, hence forming a direct link to the 2DEG (Figure 2-16). The resistivity of TiN is lower than the resistivity of Ti, allowing a very low resistance path to the 2DEG. TiN has a work function of ~3.74 eV when annealed at 800-900 °C, which is close to the electron affinity of GaN. Moreover, it is thermally stable and hard [49]. Al lowers the aggressive Ti-GaN reaction levels, because excessive Ti (relative to Al) would result to Ti void formations underneath TiN, thereby engendering uniform current flow and maximum contact area.

Improvement of the contact resistance and the surface roughness can involve optimising metal thicknesses, annealing conditions (temperature and time) and can benefit from etching the upper epitaxial layers (eg. barrier layer) to decrease the distance between contact and the channel. Recessing the barrier layer can lower the metal-semiconductor potential, but will also cause a 2DEG reduction under the contact, potentially increasing contact resistance. However, if the barrier layer becomes thin enough or is completely removed, a low metal-semiconductor potential is present for lateral contact formation to the 2DEG, greatly reducing R_c [39].

Silicon can be included in a metal stack to further optimise the ohmic contacts. It can form a eutectic melt, allowing alloy formation with lower melting

temperatures, hence ohmic contacts can be formed at lower temperatures as well [39].

High temperature annealing used for ohmic contact formation can have negative effects on the gate leakage characteristics. For this reason, gate contacts are usually deposited after the source and drain contacts. This can limit the fabrication process flow possibilities during fabrication, by allowing only a gate last approach. In contrast, a gate first approach can significantly improve yield and threshold voltage stability, as the semiconductor surface can get encapsulated and essentially protected immediately after wafer growth. The development of low thermal budget ohmic contacts that can allow a gate-first approach to be realised is discussed in later chapters. Characterisation of ohmic contacts is performed using circular and linear transfer length method structures, described in Chapter 3.6.

2.9 Carrier Transport Degrading Mechanisms

Every semiconductor is affected by scattering phenomena that compromise the theoretically predicted ideal carrier transport. During growth, the large lattice mismatch between GaN and the substrate (eg. Si, SiC, sapphire, diamond) introduces threading edge dislocations, typically formed at the nucleation layers between GaN and substrate and may extend all the way to the surface by penetrating through subsequent epitaxial layers. Lattice strain may induce some degree of dislocation related defects. A dislocation concentration greater than 10^{10} cm^{-2} can cause serious degradation in the DC behaviour of AlGaN/GaN HEMTs, by decreasing maximum drain currents and transconductance by a factor greater than two [50]. In contrast, dislocation density lower than 10^{8} cm^{-2} was found not to have significant contributions to device performance compared to other scattering phenomena.

Carrier mobility is negatively influenced by a number of other scattering mechanisms. The non-abrupt interface between AlGaN and GaN causes interface-roughness scattering for electrons flowing in the 2DEG channel. Alloy disorder scattering is another mobility limiting short range scattering source. It occurs when the 2DEG wavefunction, which is mostly confined in GaN, penetrates the AlGaN barrier [51]. An ultrathin AlN layer between AlGaN and

GaN has been found to minimise alloy scattering and improve mobility, carrier confinement and overall conductivity.

High semiconductor crystal thermal energy at elevated temperatures gives rise to phonon scattering. This is due to interactions between electrons or holes and the vibrating lattice atoms which disrupts carrier transport [52].

The spatial separation of the 2DEG from ionised donors benefits electron mobility by reducing scattering. However, unintentional residual background donors, most commonly oxygen and silicon atoms, incorporate during the growth process and give rise to ionised impurity scattering.

2.10 Current Collapse

Dispersion phenomena can be observed due to surface or bulk epitaxial layer traps and can affect the breakdown voltage and the switching speed of the device.

As mentioned earlier, the device on-resistance R_{on} can be a significant detrimental factor in power HEMT characteristics. During actual operation, additionally increased dynamic R_{on}, i.e., current collapse is regarded as one of the most critical issues to be solved [53]. After switching from high voltage off-state to on-state, HEMT on-resistance (dynamic R_{on}) becomes larger and its output current lower (current collapse) than the on-resistance measured at low voltage DC conditions. An increase in off-state voltage or switching frequency can result in elevated dynamic R_{on} and current collapse [54]. The knee voltage at which the device current saturates also increases (knee walk-out). The phenomenon is also referred to as DC-RF dispersion (Figure 2-17).

One of the main reasons for dynamic R_{on} occurrence is trapping effects. In the off-state condition, the device is under reverse bias and electrons are injected into available electron states either at the surface or the bulk layers of the device. As the device is turned on, only free charges can respond nearly instantaneously (with ps timescales), whilst trapped charges remain trapped for periods related to the emission times of the traps (μs timescales). If charges are trapped at the surface states, this results in virtual gate formation, which causes

partial or full depletion of the GaN 2DEG and degrades the drain current [55]. Predominantly surface trap related current collapse can be minimised by the use of passivation layers, such as Si_3N_4 [56], surface cleaning [57] or the incorporation of field plates [58], [59]. Bulk trap induced current collapse can be primarily restrained through buffer growth optimisation [60].

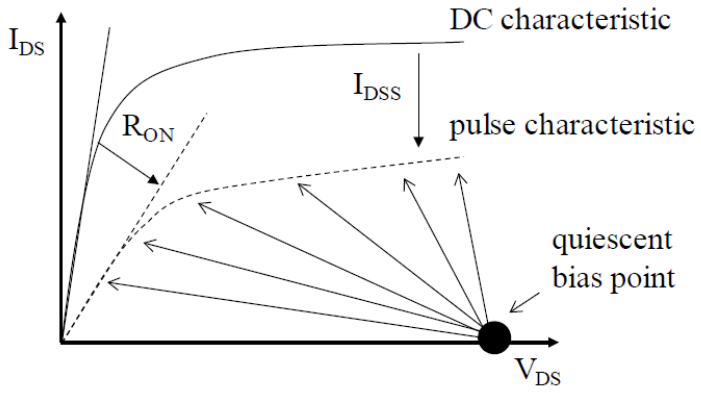


Figure 2-17: Schematic comparison of DC I-V characteristics and pulsed I-V characteristics exhibiting DC-RF dispersion phenomena [12].

2.11 Applications

Group III-nitride materials are well suited for a broad range of applications. The most notable area to date has been the solid-state LED market, where GaN-based LEDs have been replacing incandescent and fluorescent light bulbs, due to the significant electricity savings they can provide, enabled by their high efficiency at a low cost. Another application is high data storage Blu-ray discs, which use GaN-based violet laser diodes to read stored data. GaN diodes are also used for screen display backlighting providing size and energy efficiency advantages compared to cold-cathode fluorescent lamps (CCFL). High radiation tolerance, thermal stability and power efficiency of GaN related materials extend application areas to the communication, aerospace and defence sectors, with examples such as cell phone infrastructure systems, radars and solar arrays for satellites. The most widely used application of GaN based transistors in the RF and microwave field is the power amplifier. As high frequency switches are key elements of attenuators, phase shifters and other microwave components GaN technology is used to optimise their performance.

With regards to power conversion, III-nitride applications range from household appliances and consumer goods to hybrid/electric vehicles, data centres, industrial motor drives and modern power grids that incorporate renewable energy. First generations of GaN powered power supply units (PSU) have been introduced in the market and the growing demand for wireless charging systems can benefit from the high efficiency of GaN technology [61]. Another area of benefit has been identified in the growing hybrid/electric vehicle market, with the subsequent increased demand for low loss automotive power conversion during charging and power distribution. Data centres, hospitals and several other industries use Uninterruptible Power Supplies (UPS) to protect equipment in case of an outage or provide enough power to safely shutdown machinery. III-nitride power inverters can be used to transform the DC current generated by photovoltaics into AC current for grid integration. Most industrial, commercial or residential motors run pumps, fans, compressors or some type of mechanical movers and demand large amounts of electricity (approximately 40% of total electricity consumption in the US [62]). Variable frequency drives (VFD) are in the centre of many power conversion processes involving AC motors and the adoption of high efficiency semiconductors, such as GaN can reduce up to 1% the total electricity consumption even without further VFD adoption by applicable motor systems (US data) [62]. Overall, new III-nitride applications are frequently being discovered and the constantly expanding market is set to show accelerated growth. Figure 2-18 depicts an overview of current GaN-based power electronic applications.

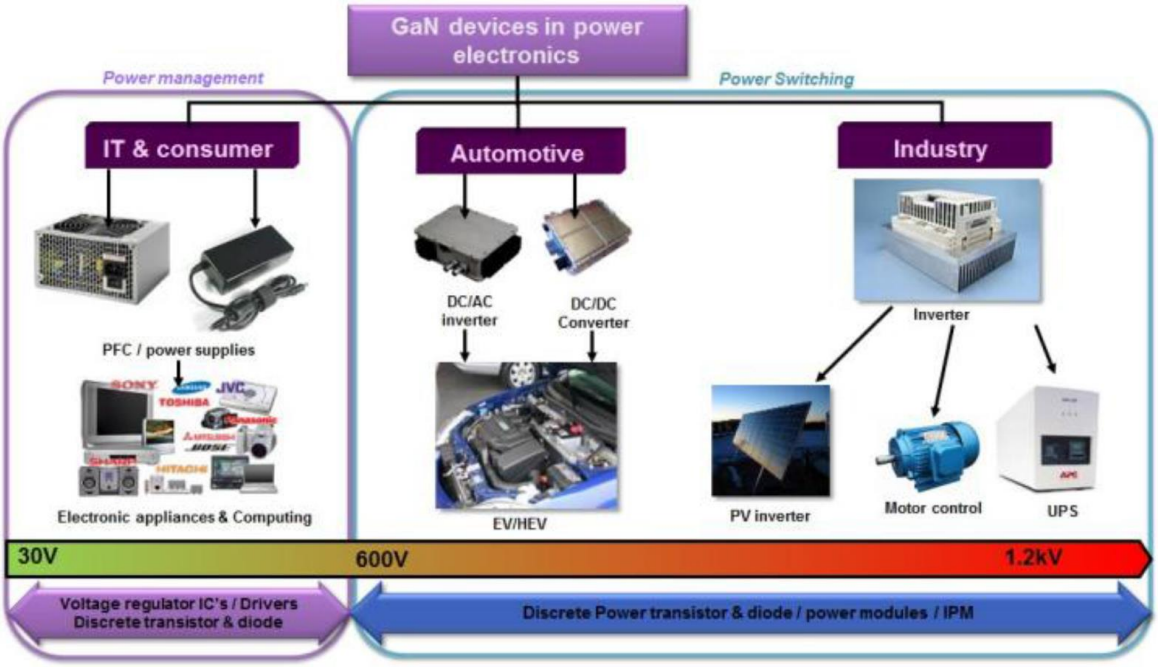


Figure 2-18: Key applications for GaN power devices [63].

2.12 Conclusion

In this chapter, the operation principles of group III-nitride HEMTs grown on Si have been discussed with regards to the physical phenomena that enable or obstruct their functionality. The material properties that allow 2DEG formation have been presented as well as the metal contacts to the semiconductor that can access its capabilities in a device concept. Performance comparisons with other material systems have been drawn. Suitable semiconductor layer structure designs and their influence on HEMT performance metrics have been introduced. References to the background content and the problems identified in this chapter may be used in the sections involving experimental results to validate their purpose and highlight their impact.

3 Fabrication & Characterisation Methods

In this chapter, attention will focus on material growth and device fabrication techniques along with a brief description of the operation principles of the tools employed in the cleanroom. Characterisation methods will be also presented.

3.1 Group III-Nitride Growth

Gallium nitride synthesis was first reported by Johnson et al in 1930, who realised it through the passing of ammonia (NH_3) over metallic Ga at 900-1000 °C [64]. In 1969, GaN was epitaxially grown by Maruska and Tietjen through means of hybrid phase vapour epitaxy (HVPE) [65], and by metal-organic chemical vapour deposition (MOCVD) in 1971 by Manasevit [66]. In the field of optics, the violet GaN light emitting diode (LED) was first demonstrated by Maruska and Panvoke in 1972. A technology breakthrough for increased photoluminescence efficiency was achieved by Amano et al in 1989 through *p*-type doped GaN [67], and ultimately led to the InGaN-based high brightness blue LED [68]. These developments significantly intensified research efforts on group III-nitride material growth, from which the power GaN HEMT development immensely benefitted.

Currently, the most widely used growth technique for commercial applications of III-nitride materials is MOCVD. MOCVD growth of III-nitrides is typically a high-temperature (800-1100 °C) and moderate pressure (2-100 kPa) process. The substrate is heated up whilst gaseous reactants pass over it and through chemical reactions lead to semiconductor layer formation. The group III metal atoms (i.e. Ga, In, Al) are provided in the form of metal-organic compounds (precursors), such as trimethylgallium (TMGa), triethylgallium (TEGa), trimethylindium (TMIn) and trimethylaluminium (TMAl), since they cannot be brought in the gas phase in their elementary form. The metal organic compounds are transported to the heated substrate through a carrier gas, typically H_2 or N_2. The nitrogen atoms are provided to the reaction chamber by means of ammonia according to the simplified reaction:

$$(CH_3)_3Ga(g) + NH_3(g) \rightarrow GaN(s) + 2CH_4(g) \quad (3\text{-}1)$$

Optimisation of MOCVD growth is done through empirical studies of parameters such as temperature, V/III ratio, substrate orientation and mass flow rates of the reactants [69]. A schematic of a MOCVD reactor is presented in Figure 3-1. The substrate is positioned on a rotation disc and an RF induction coil is used to increase its temperature. The precursors used as group-III element sources are diluted in a carrier gas, whilst NH_3 is used as the nitrogen source. Monitoring of the growth parameters and their effect on crystal quality can be indicated through reflectivity measurements performed in situ.

Growth of the wafers presented in this thesis for HEMT development was implemented at the Cambridge University's Centre for Gallium Nitride MOCVD reactor facilities and commercially at NTT-AT and IQE.

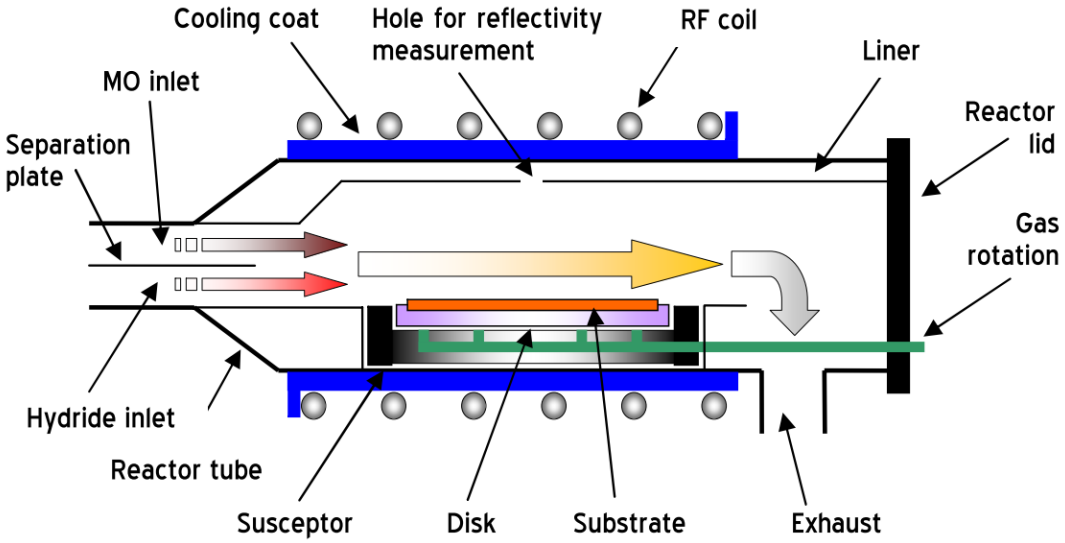


Figure 3-1: Schematic of MOCVD reactor [70].

Upon delivery, the wafers were covered by a protective photoresist layer and were commercially diced to chips. This serves the purpose of performing fabrication processing using different conditions whilst maximising the utilisation of the wafer surface area.

3.2 Photolithography

The foundation of a fabrication sequence is the photolithography process, during which an ultraviolet (UV) light source is used to define photoresist patterns on the semiconductor material surface. The resist undergoes a chemical reaction

during exposure to light. If a positive resist is used its polymer chains break in the areas exposed to light, whereas a negative resist becomes hardened in the same areas.

Initially, the surface of the semiconductor sample is cleaned to remove any traces of contamination, including dust, organic, ionic or metallic compounds. A spin coating apparatus is used to apply photoresist. The sample is held using a vacuum, and the resist is dispensed on its surface. The sample is then rotated at high speed, which results in a relatively uniform and fit for purpose resist thickness. The thickness is also determined by the viscosity of the resist used. Shortly afterwards, the sample is transferred to a pre-heated hotplate or an oven, where heat causes the resist to be solidified.

The next step involves the use of a mask aligner, so that features (e.g. etch area patterns or metal contact footprints) can be transferred from a photolithography mask to the sample surface. There, one of three photolithography methods may be engaged, depending on the relative position between mask and surface. The mask may be in contact with the sample surface (contact method), close to the surface (proximity method) or may be used to project features to the substrate allowing scalability of features (projection method). Figure 3-2 shows simplified schematic diagrams of the three methods. The diffraction limit of the light source used determines the limit of the feature size that can be resolved. The overall contributions from the resist, development and etching processes come also into play.

The photolithography masks' geometrical layout design was completed using Tanner L-Edit software and the mask plates were commercially procured. These masks were developed using an e-beam lithography process on a glass substrate. The sample-mask alignment was performed using a Karl Suss MA6 mask aligner, which features x-y and rotational alignment. It allows for 1:1 mask to sample feature printing in five contact exposure modes; hard contact, soft contact, vacuum, flood and proximity [71]. When hard contact is used, the sample is physically pressed against the mask using springs and then pneumatic brakes are used to secure its position. During UV light exposure, the vacuum that secures the sample to the holder switches to N_2 pressure bringing the wafer into further contact with the mask. For the MA6 mask aligner a theoretical <1.5 μm

resolution can be achieved, dependable on wafer dimensions, resist type, and clean room conditions [71]. Soft contact is almost identical, but without N_2 pressure applied (<2.5 μm resolution). The vacuum mode may enable the highest resolution (<0.8 μm theoretically); however it can only operate for larger sample sizes and could potentially diminish the mask lifetime. In this mode, the pressure between the mask and the sample is regulated by a slowly established vacuum chamber. The mask and sample are held firmly due to the pressure difference between the chamber and the atmospheric environment outside the mask and on the back side of the wafer holder. The proximity mode enables exposure when the mask is in close proximity to the wafer without actual contact. It prevents mask wear and tear, however the transferred patterns may exhibit lower resolution compared to other modes (<3 μm for 20 nm wafer-mask distance). Finally, flood mode can be used to expose the sample without previous alignment between wafer and mask or without even a mask.

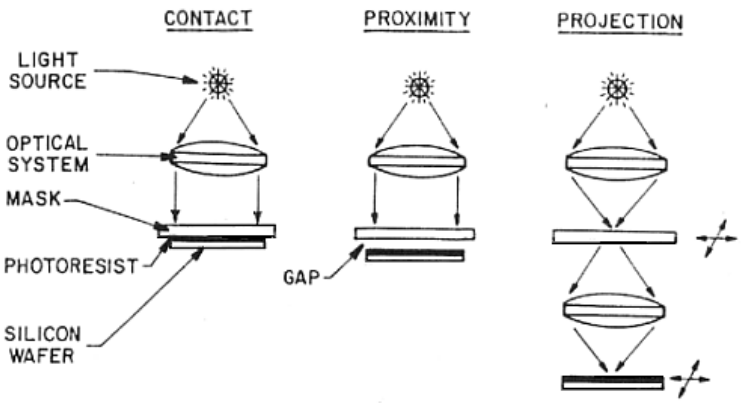


Figure 3-2: Contact, proximity and projection lithography [72].

After each exposure step was completed, the sample was transferred to a development solution for a predefined time period. As mentioned, depending on the tone of the photoresist, the UV light source hardens (negative photoresist) or weakens (positive resist) the exposed resist areas. The less soluble resist areas remain intact after development; whereas the weaker bonded resist areas are soluble to the photoresist developer.

Metallisation steps were completed using a lift-off process. Following the definition of a resist pattern through standard photolithography, thin metallic films are blanket deposited over the samples, covering both resist areas and

areas that the resist has been dissolved in the developer solution. When the actual lifting-off process takes place, the resist under the metallic film is removed in a solvent, taking the metal deposited on top with it. The film deposited on areas that no photoresist is present remains intact, so the end result is a metallic pattern on the substrate.

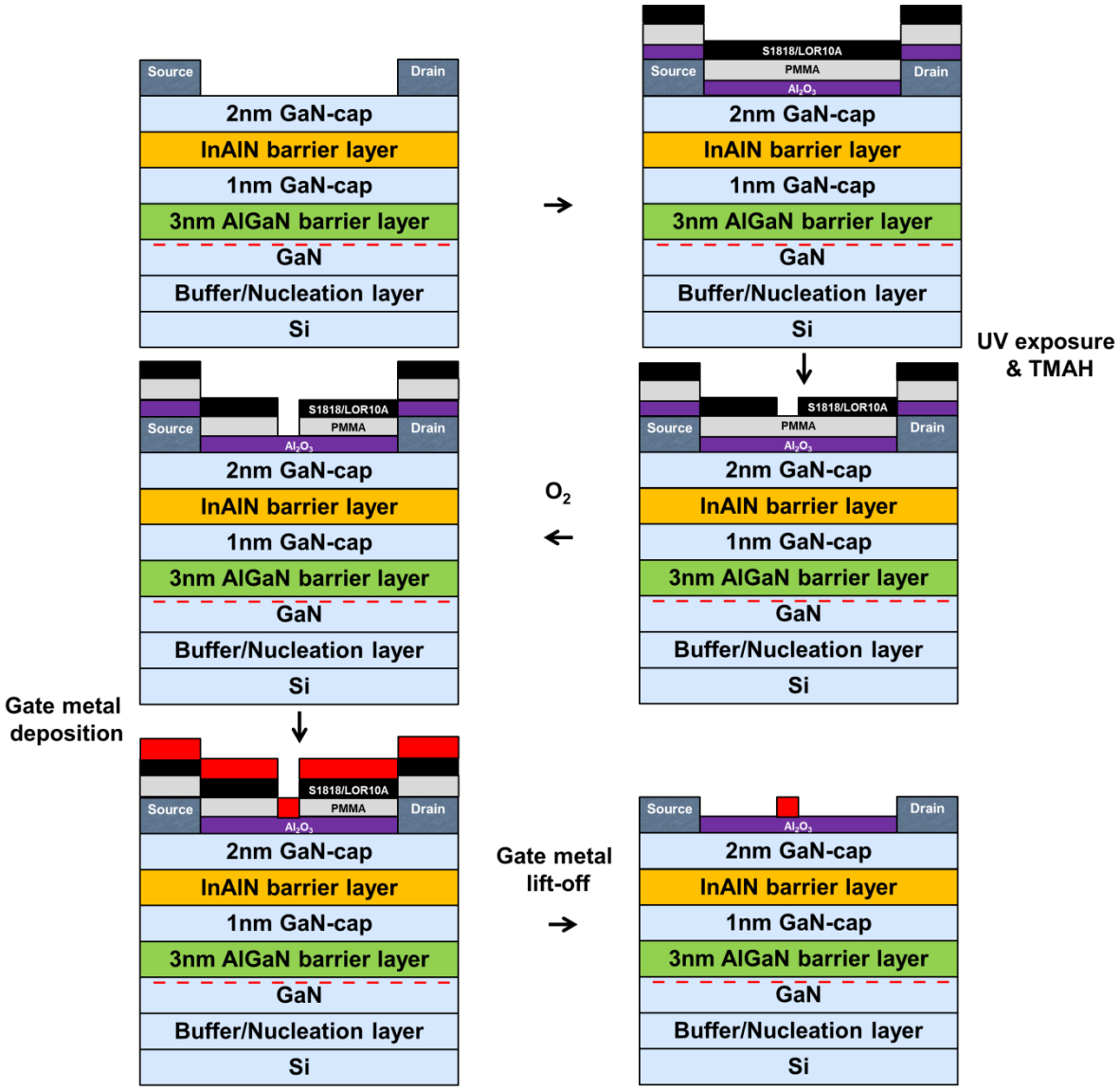


Figure 3-3: PMMA-based gate process flow for Al_2O_3 dielectrics.

In this report, S1818 and LOR10A positive photoresists as well as PMMA e-beam positive type resist were used in various stages of the lithography processes. S1818 was the main resist used in etch and metallisation stages. LOR10A assisted metal lift-off as the bottom part of a bilayer involving S1818. PMMA resist was used for gate metallisation in some processes involving Al_2O_3 dielectrics. The tetramethylammonium hydroxide (TMAH)-containing Microposit MF319

developer, commonly used for resist patterning prior to metal deposition, etches the Al containing Al_2O_3 dielectric. One of the solutions to this is to use PMMA before the LOR10A/S1818 lift-off bilayer is spun. In this case, the resist patterning on the photoresist bilayer can be implemented in MF319 solution as the dielectric is still protected by the PMMA resist. After this is completed, the sample is transferred to a vacuum chamber tool where O_2 plasma is applied to remove the PMMA resist from the gate area. Metallisation on the Al_2O_3 dielectric is then possible, as outlined in Figure 3-3.

Similarly to the PMMA gate process, an alternative route to a non-destructive gate procedure involving Al_2O_3 dielectrics is through the use of SiN_x instead. The SiN_x film can be deposited prior to the deposition of the lift-off resist bilayer, so that the Al_2O_3 film does not come in direct contact with the TMAH-containing developer. The LOR10A/S1818 resist development is followed by low power SF_6 plasma treatment to selectively remove SiN_x on Al_2O_3. Metal contacts can be then deposited on the dielectric film to form the gate stack.

3.3 Thin Film Deposition

Thin film deposition processing is required in many stages of GaN HEMT development; from growing substrate material crystals to passivating surfaces for electrical or mechanical purposes and to depositing contacts that enable access through external electrode connections. Some of the most prevalent thin film technologies will be presented below.

3.3.1 Plasma Enhanced Chemical Vapour Deposition

A method for depositing thin material films is Plasma Enhanced Chemical Vapour Deposition (PECVD). Its operation relies upon the use of a plasma source, which produces energetic electrons, ions and free radicals, assisting the chemical reactions. Compared to Low Pressure Chemical Vapour Deposition (LPCVD), it benefits from low temperature processing. Deposition rates are higher, at the expense however of typically lower film quality with higher defect density. In this work, deposition of SiO_2 dielectrics was implemented through an Oxford Instruments PECVD 80+ PECVD tool.

The simplified chemical reaction for SiO_2 deposition is:

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2H_2 + 2N_2 \quad (3\text{-}2)$$

For silicon nitride a typical chemical reaction is:

$$3SiH_4 + 2N_2 \rightarrow Si_3N_4 + 6H_2 \quad (3\text{-}3)$$

The use of an inductive coupled plasma (ICP) in a PECVD technique utilises plasma generation through electromagnetic induction (Figure 3-4). A time varying electric current passes through a coil and it creates time varying magnetic field around it, which in turn induces azimuthal current in the chamber rarified gas leading to breakdown and plasma formation. High density plasmas that typically produce good uniformity and lower defect counts can be obtained through the use of this technique. Room temperature deposition of SiN_x dielectrics was realised through an Oxford Instruments System 100 ICP PECVD 180 tool.

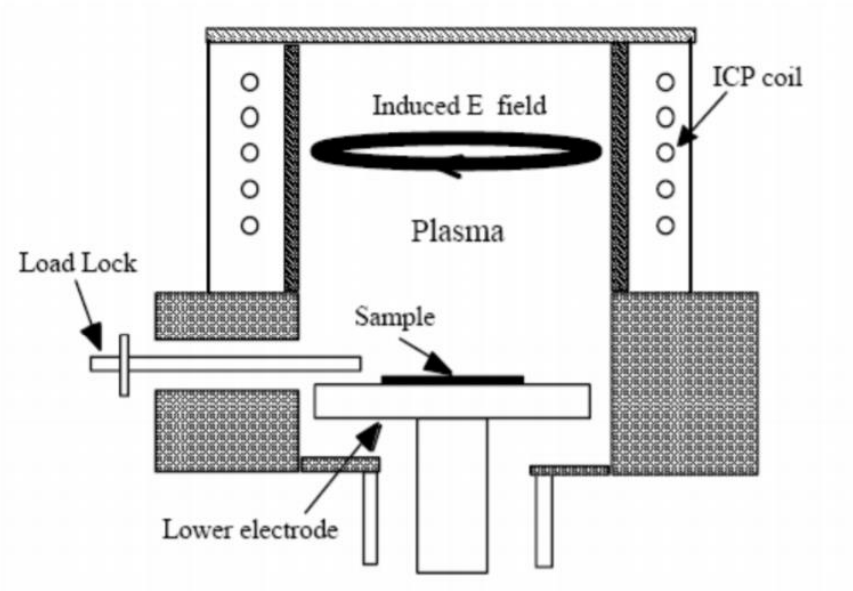


Figure 3-4: ICP PECVD schematic diagram [73].

3.3.2 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a film deposition technique used for tuneable material composition and even angstrom level precision. It is based on self-

limiting reactions, through sequential deployment of gaseous chemical precursors that react with the substrate, as illustrated in Figure 3-5. First, a chemical precursor is pulsed on the substrate and once absorbed at one semiconductor monolayer, it reacts with the surface. No absorption on the layers underneath take place. Excess precursor and reactant by-products are removed through the flow of an inert carrier gas. Then, another precursor is pulsed, reacting with the heated surface and another purge step for chemical by-product removal follows. The first precursor steps are conventionally referred to as modification half-cycle and the second precursor half-cycle is the reaction half-cycle. The result is the formation of a desired material layer. The process is then repeated until the desired film thickness is obtained.

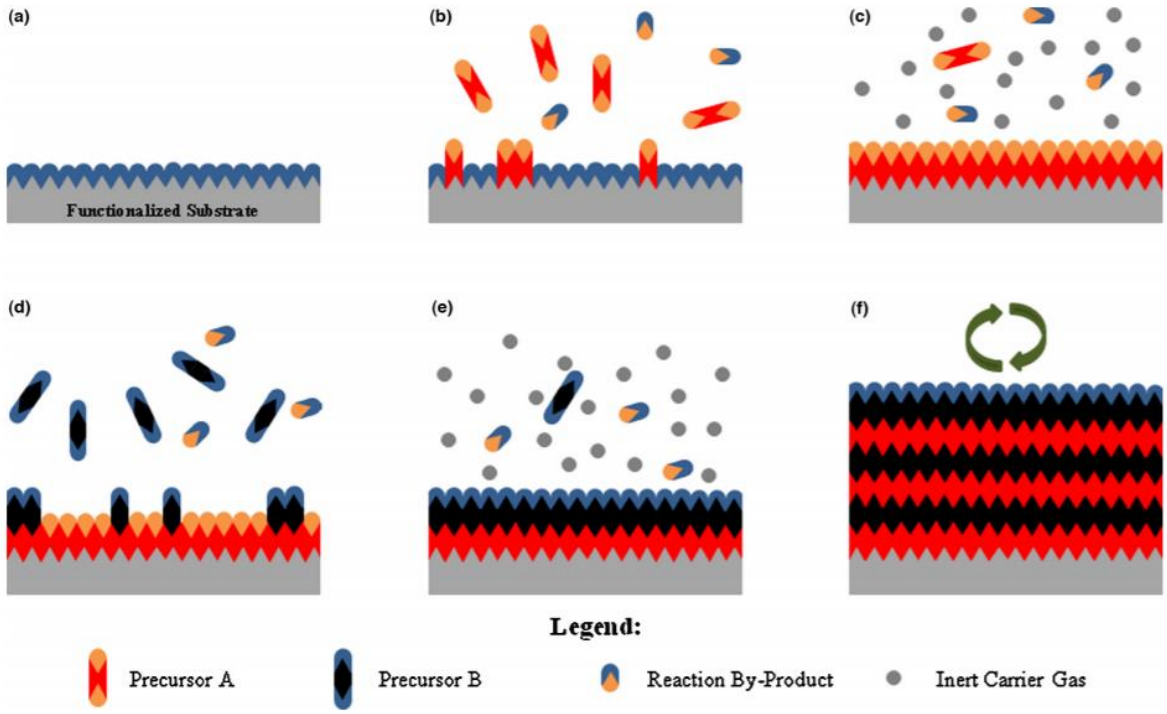


Figure 3-5: Diagram of a single cycle sequence of Atomic Layer Deposition [74].

A common ALD process is the deposition of an Al metal-organic precursor, which upon oxidation leads to Al_2O_3 formation. With regards to thermal-type ALD processes, substrate heating is used to provide the means for reaching the required activation energy for chemical reaction during the reaction half-cycle. In contrast, during the reaction half-cycle in plasma-assisted ALD, a plasma source is employed to enable or accelerate chemical reactions. Typical plasmas used are generated in H_2, N_2, or O_2 reactant gases or their combinations. Also,

plasmas generated in gases or vapours such as H_2O or NH_3 may be used, for which there can be coexistence of plasma and thermal ALD surface reactions [75].

The high reactivity of the plasma species during plasma assisted ALD processes may provide greater flexibility in the choice of processing conditions and at even room temperatures. It may also allow the incorporation of reactants that are not available for thermal processing due to their high thermal requirements for sufficient reactivity [76]. However, the complexity of the reactions involved makes it apparent that a direct comparison of film properties is required to determine the method of choice for specific intended purposes.

For this work, ALD Al_2O_3 dielectrics were deposited by the Functional Materials group at Liverpool University's thermal and plasma enhanced ALD reactors.

3.3.3 Physical Vapour Deposition

Deposition of metal contacts on group III-nitrides is performed via Physical Vapour Deposition (PVD) techniques, specifically evaporation and sputtering. For evaporation, the source metal atoms get heated from solid phase to a gas phase and then diffuse to the substrate through a vacuum chamber, coating with a thin metal layer. E-beam evaporation relies on electrons being radiated from a heated tungsten filament. The electron beam is deflected and accelerated towards the metal by means of electric or magnetic fields where the electron kinetic energy gets transformed by the impact into thermal energy that provides the solid-to-gas phase transition (Figure 3-6). A high voltage DC supply is used to obtain the required electron energy which vaporises the target material and the coating growth is typically controlled by a quartz crystal microbalance which monitors thickness and evaporation rate.

Sputtering techniques are based on ions gaining enough energy to remove atoms from the material to be deposited. The ions are generated by means of an inert gas, such as Ar, and the bombardment of the target material results in a high number of inelastic collisions, which sputter particles in a charged plasma and travel towards the substrate surface [77]. Sputtering allows the generation of

more dense coatings compared to evaporation techniques, with a better step coverage, as the charged sputtered particles possess higher energy and can be more densely arranged when growing a thin film. Also, compared to evaporation, sputtering is less sensitive to the target's stoichiometry, which greatly affects deposition rates, thus allowing several substances or alloys with complicated stoichiometry to be deposited [78]. However, sputtering can destroy the structure of some other films, such as fluorides [77]. Furthermore, films of higher purity can be obtained by evaporation due to the low pressures involved in the process, a very important consideration factor for Schottky contact development.

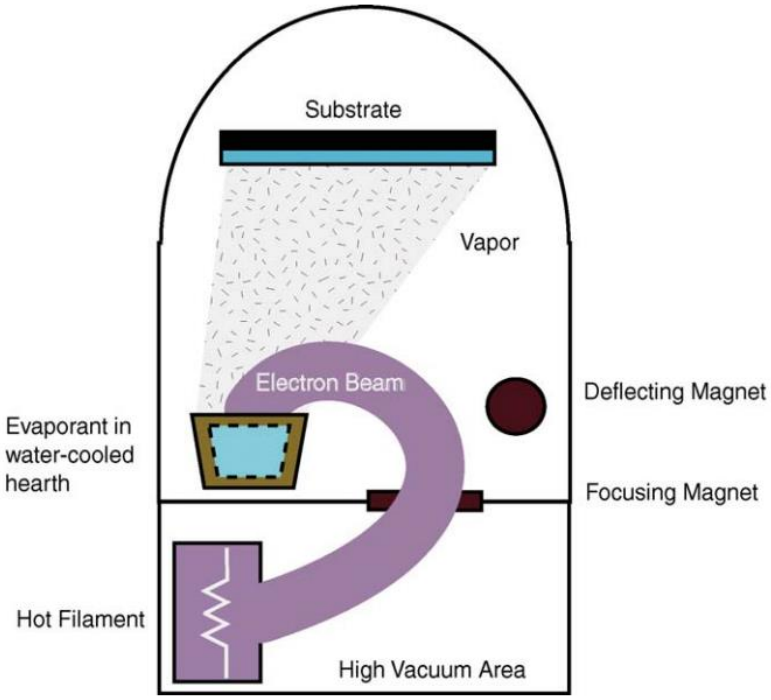


Figure 3-6: E-beam evaporator schematic diagram [79].

Two Plassys e-beam evaporators (Plassys MEB 400S and 550S) were operated for metal deposition. They contain eight crucibles storing different metals, including Pt, Au, Ti, Ni, Al, Mo, Pd that were used for GaN HEMT processing. The MEB 550S evaporator is equipped with an ion gun which is used to pre-treat material surfaces prior to deposition or increase the density of the coating material.

3.4 Group III-Nitride Etching

Etching of GaN and related materials is mostly achieved through chlorine and bromine based dry etching processes. In 1993, Adesida et al first demonstrated Reactive Ion Etching (RIE) of GaN using $SiCl_4$ based plasma chemistries and achieved 50 nm/min etch rates [80]. Pearton et al (1993) established BCl_3 and CCl_2F_2 etching at low power and pressure conditions and demonstrating 20 nm/min etch rates and a year later Lin et al achieved etch rates in the excess of 100 nm/min through the use of BCl_3 [81].

Common etching attributes include the degree of isotropy (directionality of etching; isotropic refers to single direction etching whereas anisotropic is multi-directional and uniform, result in undercutting), selectivity (ratio of etching rate of target material to another one, typically a photoresist or a semiconductor layer underneath), etching rate, aspect ratio (depth-to-feature size) and surface roughness. The etching process can be either chemical, where chemical reactions take place or physical, where some mechanical interaction is involved.

3.4.1 Reactive Ion Etching

Reactive Ion Etching (RIE) is a type of ion-enhanced plasma etching process. During its operation, RF discharge-excited species (ions, radicals) etch material surfaces in a low-pressure environment. Inside the etching equipment (Figure 3-7a), when an RF source is connected to an electrode pair in the presence of a low-pressure gas, electrons accelerate due to the applied electric field and collide with molecules and atoms. If their kinetic energy exceeds the ionisation energy, an outer electron gets excited leaving behind an ion. The increasing number of excited electrons results in an accelerating number (avalanche) of new collisions and new ions being generated. The phenomenon is called RF discharge and results in a macroscopically neutrally charged gas (a plasma), with almost equal electron-ion numbers [82]. The RF power applied controls the density of the charged species. A plasma has conductive properties, due to electrons being able to travel freely within it. As soon as a plasma is established, a DC bias voltage is generated, which extracts ions from the plasma and energises them. The DC bias contributes to the etching directionality as well as the desorption of reaction by-products from the target material surface. The

surface to be etched gets bombarded by the reactive species and the material is removed by forming a volatile component [83].

The overall etching mechanism can be either chemical, where the ions react with the surface to form a volatile compound, physical (sputtering), or both. In addition to RF and DC power, equipment parameters such as gas flow, and chamber pressure can assist the adjustment of the etch parameters. RIE methods can be utilised to achieve relatively high aspect ratios and the obtained etch rates through their use lie between the ranges of chemical and physical etching.

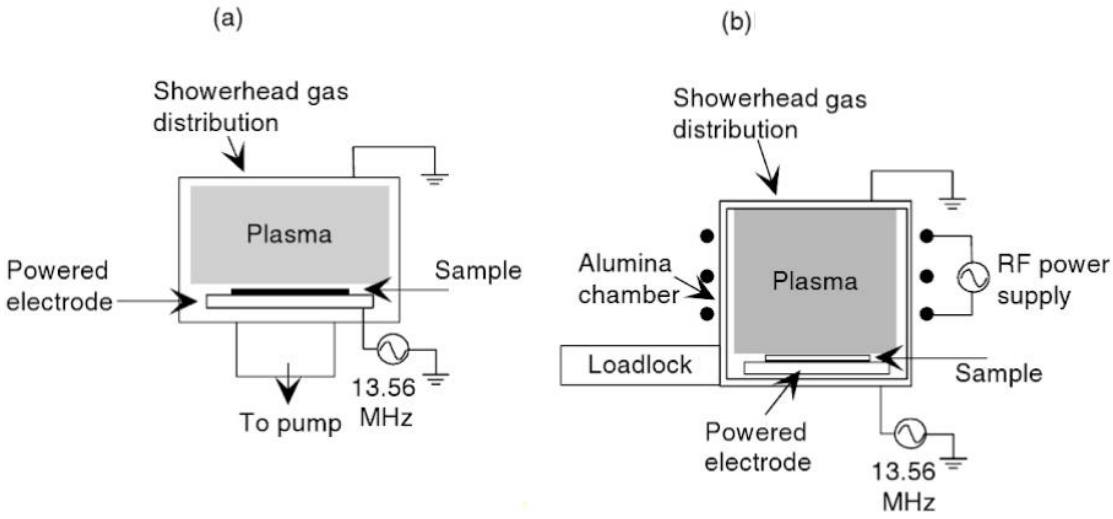


Figure 3-7: Schematic diagrams for (a) RIE (b) ICP-RIE etching equipment [84].

In ICP-RIE technology, an additional and separate RF power supply is used to generate high-density plasma with a magnetic field (Figure 3-7b). The RF power source, connected to the cathode, is applied to an inductive coil. The alternating coil electric field induces an alternating magnetic field, which energises electrons that participate in the ionisation of gas molecules and atoms [85]. The higher generated plasma densities, compared to RIE processes, lead to improved efficiency of group III-nitride bond breaking and sputter desorption of etch products for the surface [86]. Also, the incorporation of the separate ICP source permits the decoupling of ion density and ion energy applied to the surface, allowing higher process flexibility compared to RIE.

Regarding processing in the James Watt Nanofabrication Centre, RIE processing for primarily SiN_x dielectric etching (SF_6 chemistry) was implemented through an

Oxford Instruments RIE80+ tool. An Oxford Instruments PlasmaPro System 100 ICP180 RIE tool was suited for shallow, low damage III-nitride etching as well as dielectric etching (Cl_2, BCl_3, HBr, $SiCl_4$) chemistries. Both tools are equipped with interferometer ports, to monitor etch depths.

3.4.2 Atomic Layer Etching

A dry etching technique for high precision removal of very thin semiconductor material layers is Atomic Layer Etch (ALE) [87]. This technique is based on first applying a precursor to modify the targeted surface and subsequently apply another reactant to remove the modified layers (Figure 3-8). These two steps comprise an ALE process cycle and they are repeated until the desired etch depth is attained. The challenge is to ensure that both modification and modified layer removal steps are self-limited. The former because it will determine the etch rate in each cycle, the latter to ensure that only the modified layer is removed and not the non-modified layers underneath.

ALE is particularly useful for transistors employing a gate recess process, due to its high precision. Nearly single monolayer removal per ALE cycle can be achieved based on careful choice of chemical precursors. Regarding group III-nitride materials, two chemistry approaches were tested with similar positive results using a cluster tool from Oxford Instruments Plasma Technology. This tool contains an ICP etching chamber with repeat loop function and a Scienta Omicron NanoSAM surface analysis tool, including an Auger spectrometer. The clustered setup enables under vacuum transfer of samples from plasma processing into the analysis chamber.

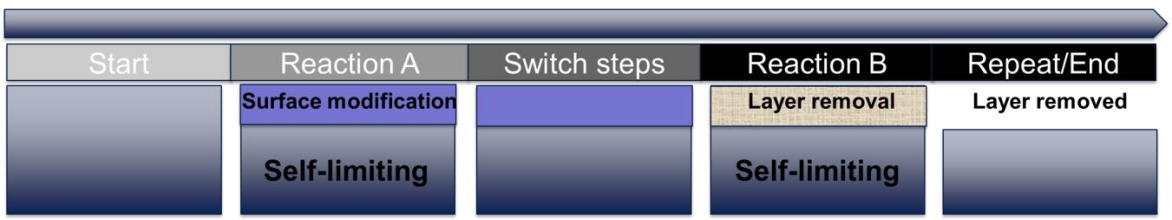


Figure 3-8: Illustration of an ALE sequence flow diagram.

Two ALE chemistries were tested on InAlN/AlGaN/GaN materials. The first was through the application of ICP-RIE Cl_2 plasma cycles which leads to the formation of GaCl and NCl species on the surface. Then, ICP-RIE Ar plasma exposure was

applied through a source of optimised RF power levels to remove the GaCl and NCl species, but not induce damage to the underlying semiconductor materials. Another choice of chemical precursors involved a repeating procedure of HBr bromination to form self-limited Ga, In and Al bromides on the semiconductor surface. This modified surface species were then removed using an Ar plasma source and the process was repeated until the desired etch depth was obtained.

3.4.3 Wet Etching

Wet etching is performed by immersing samples or wafers in liquid etchant solutions, where chemical reactions take place between the etchant and the surface layer. Due to the chemical nature of the reactions, wet etching processes can be highly selective. High isotropy is typically present, as all surfaces are exposed to the solution. This can lead to significant undercut formation, and use in highly scaled-down patterns can sometimes be problematic. Cost is smaller than dry etching solutions.

The high bond strength of group III-nitrides significantly restricts flexibility of etching processing and as a result material etching is usually restrained to dry etching. However, highly selective low damage plasma techniques on GaN and related materials have not been developed or have been underutilised, so chemical wet etching methods are still being studied. In Chapter 6, the use of ethylenediamine in the fabrication of recessed gate InAlN/AlGaN/GaN based HEMTs will be analysed.

3.5 Rapid Thermal Annealing

As described in Chapter 2, metal contacts on AlGaN/GaN or InAlN/GaN HEMT structures are subjected to thermal annealing in order to reduce any barriers to current flow and effectively access the highly conductive 2DEG channel. For this process step, the samples undergo rapid heating from ambient conditions to elevated temperatures and are held in these temperatures for set time periods. There is a temperature and time window during which optimised contacts can be obtained with other influencing factors being metal stack choice, semiconductor material choice and growth conditions, surface pre-treatment conditions, previous processing steps etc. Due to the plethora of potential conditions under

test, a design of experiments (DOE) that can systematically isolate the most favourable outcomes can be beneficial. Then, trial and error testing of the selected conditions is performed to optimise the contacts.

A Jipelec JetFirst RTA was used for ohmic contact annealing. It makes use of infrared heating lamps and the temperature of the stage over which the samples are placed is monitored and calibrated by a thermocouple and a pyrometer (Figure 3-9). Stage cooling is provided through inlet gases.

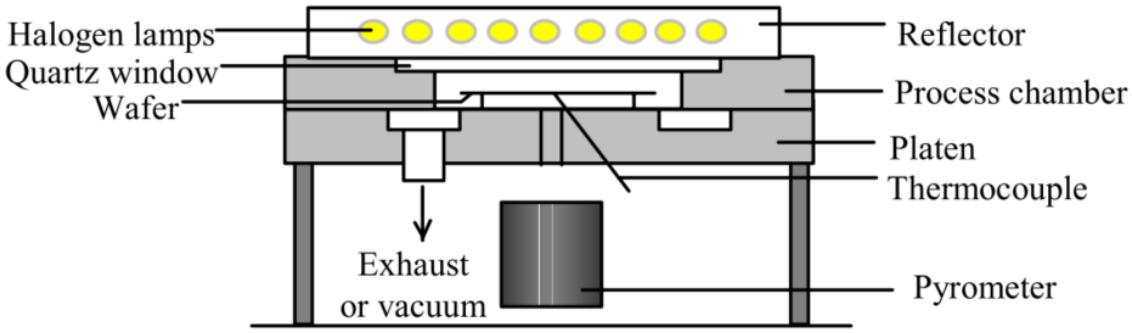


Figure 3-9: RTA schematic diagram [88].

3.6 Characterisation

In this section a summary of characterisation methods involved in GaN power HEMT development will be described. Acquiring and extracting accurate datasets through various metrology methods is the key point for process optimisation, benchmarking and ultimately device performance maximisation.

3.6.1 Transfer Length Model

The performance and quality of ohmic contacts is assessed through the use of the Transfer Length Method (TLM). The simplest geometrical structures employed in this characterisation model utilise rectangular metal pads, which are separated by different distances, as seen in Figure 3-10. The structures are isolated from any other structures on the chip by a mesa etch. Low field (linear) resistance measurements are taken between adjacent pads. According to the equivalent circuit, each resistance measurement is equal to the sum of the contact and substrate resistances.

$$R_{total} = 2R_c + R_s \tag{3-4}$$

where R_c is the contact resistance and R_s is the semiconductor resistance in Ω.

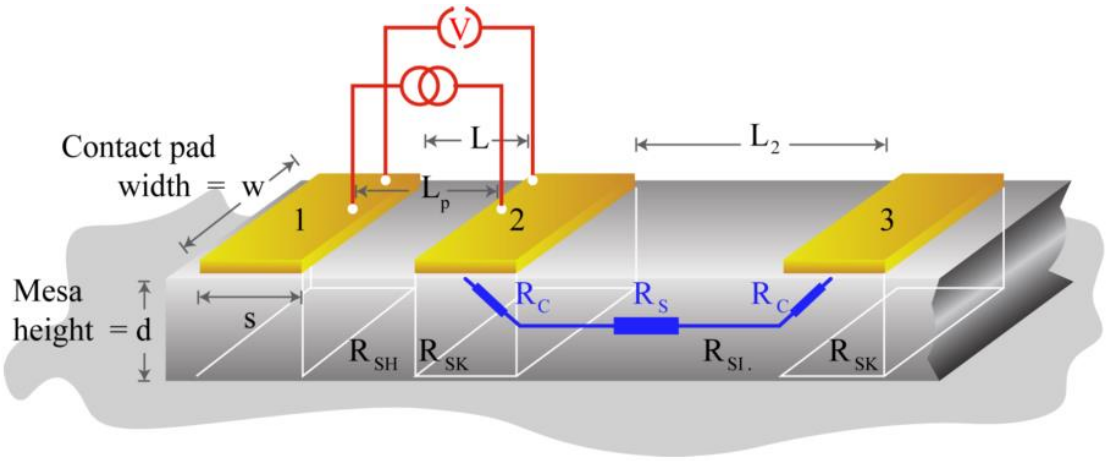


Figure 3-10: Linear TLM characterisation structure [29].

The semiconductor resistance is given by:

$$R_s = R_{sh}L/W \tag{3-5}$$

where R_{sh} is the semiconductor sheet resistance, L is the pad spacing and W is the metal pad width. The total resistance becomes:

$$R_{total} = 2R_c + R_{sh}L/W \tag{3-6}$$

This algebraic expression can help decoupling the influence of the contacts and the semiconductor material. Each resistance measurement can be plotted against gap distance, as illustrated in Figure 3-11. The gradient is R_{sh}/W and the line intercepts in x and y axis at L_x and $2R_c$ respectively. $L_T = L_x/2$ is a first approximation of the transfer length, assuming that the sheet resistance under the contact R_{sk} is the same as between the contacts. It represents the average distance that a carrier travels in the semiconductor under the contact before it flows up into the contact.

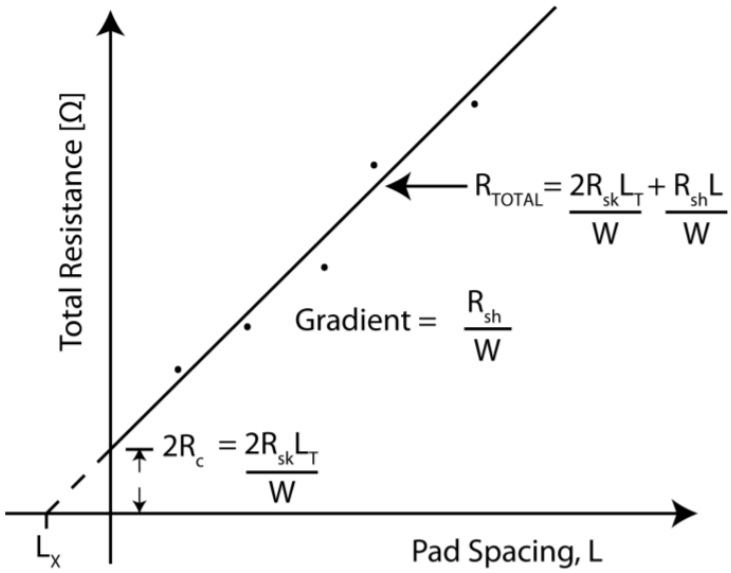


Figure 3-11: Resistance vs pad spacing [29].

An alternative TLM method of obtaining the contact resistance without the requirement for mesa etch is through circular TLM patterning and is described in [29]. Ohmic contacts are circular and are separated by a ring-shaped gap (Figure 3-12).

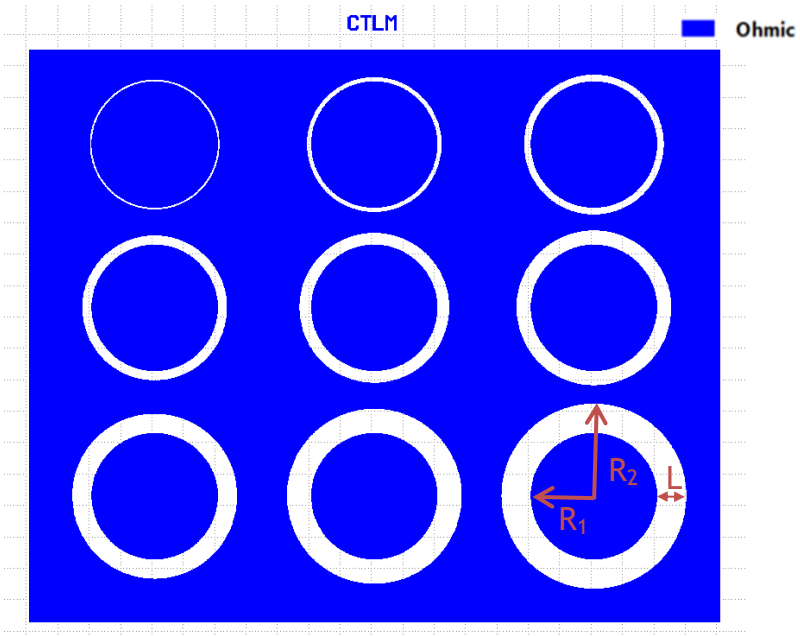


Figure 3-12: Circular TLM structures.

A geometrical transformation is used to extract the equivalent resistance. Assuming the inner contact pad radius is much longer than the pad distance, the resistance measured is equivalent to;

$$R_{total} = \frac{R_{sh}}{2\pi R_1}(L + 2L_T)c \tag{3-7}$$

where c is the correction factor;

$$c = \frac{R_1}{L} ln \frac{R_1 + L}{R_1} \tag{3-8}$$

From the above relationship, a different value of correction factor is applied when ohmic pads separated by different distances are measured.

3.6.2 Hall Measurements

Semiconductor sheet resistance as well as carrier transport properties can be obtained via Hall measurements of Van der Pauw structures. The principles of operation outlined in [19]. Hall measurements enable the carrier type to be identified and the carrier concentration, sheet resistance and carrier mobility to be extracted.

When an applied magnetic field is perpendicular to the direction of current flow it causes charges to be deflected from their straight path charge build-up at the material edges. The voltage difference across the two edges of the electrical conductor is the Hall voltage (Figure 3-13). The Hall Effect can be applied to a Van der Pauw structure (Figure 3-14).

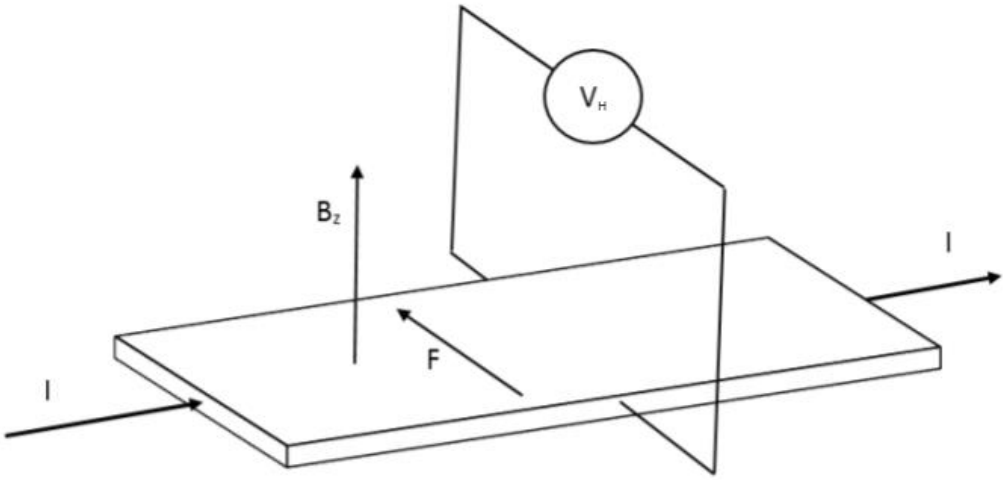


Figure 3-13: Diagram of a Hall Effect example showing current I, magnetic field B_z, Hall voltage V_H and force F on majority carriers [89].

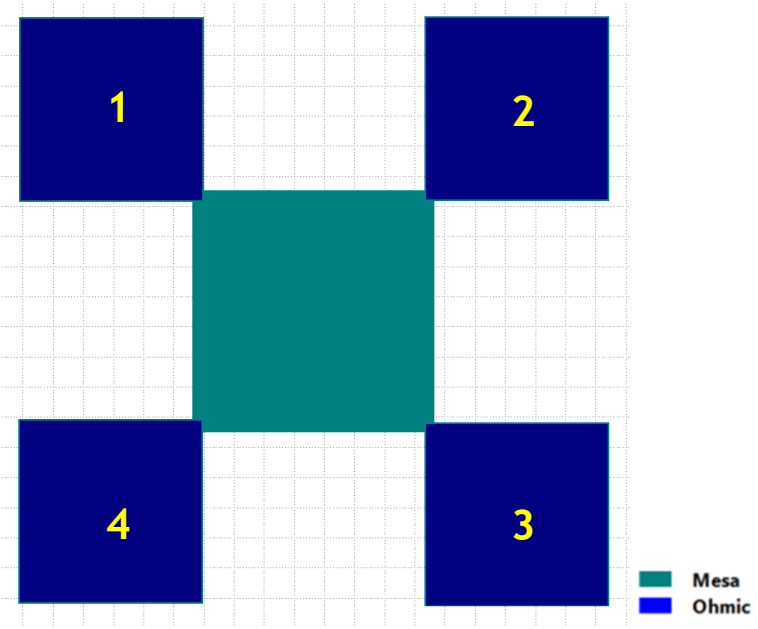


Figure 3-14: Van der Pauw structure.

Initially the material sheet resistance is extracted. A current is injected between two contacts, such as 1 and 2, which gives rise to a corresponding voltage across the two other contacts. The corresponding resistance can be calculated using two such measurements, one vertical and one horizontal, which should be identical as the structure is symmetrical [90]. The sheet resistance can be calculated as;

$$R_{sh} = \frac{\pi R}{ln2} \tag{3-9}$$

Following the calculation of the sheet resistance, a current is injected between two non-adjacent contacts while a magnetic field is applied, perpendicular to the sample surface. The voltage potential is measured between the other two contacts. Another measurement is then repeated for a magnetic field of the opposite direction and the difference in measured voltages is the Hall voltage and its sign indicated the majority carrier type. Using the current, the magnetic field and the Hall voltage, the Hall coefficient is defined as;

$$R_H = \frac{V_H}{IB} \tag{3-10}$$

The carrier concentration is then calculated as;

$$n_s = \frac{1}{qR_H} \tag{3-11}$$

The Hall carrier mobility can be calculated as;

$$\mu_H = \frac{R_H}{R_{sh}} \tag{3-12}$$

Other DC measurements are performed on wafer using a semi-automatic Cascade Microtech Summit 12000 probe station connected to a Keysight B1500A semiconductor parameter analyser, which runs Keysight Easyexpert software. The test setup is used to measure the output characteristics I_{DS} - V_{DS}, gate transfer characteristics I_{GS} – $V_{GS,}$ gate leakage characteristics I_{GS} - V_{DS}, transconductance characteristics g_m – V_{GS}, off-state leakage, buffer leakage and breakdown voltage characteristics. Device biasing for each measurement presented will be described in chapters 5 and 6.

3.6.3 Atomic Force Microscopy

Atomic Force Microscopy (AFM) is a type of scanning probe microscopy that is utilised for high resolution topographic imaging [91]. In an AFM, a sharp fabricated tip, which is attached to a cantilever, is employed and it gets pushed to a surface (Figure 3-15). In the most common measurement technique, the deflection of the cantilever, caused by the force between the tip and the

surface, is monitored using a laser and a photodiode. A feedback circuit keeps the cantilever deflection nearly constant by adjusting the voltage that controls the height of the tip. The topographic mapping of the mechanical forces across the surface is used to generate an image of the surface under study. The AFM can extract the image in a number of ways using contact mode, an oscillating technique where the tip taps the surface, or completely contactless mode. In this work, a Bruker Dimension Icon AFM and a Veeco Dimension 3100 AFM were used to monitor the effect of etch processes on surface morphology, etch heights and trench profiles.

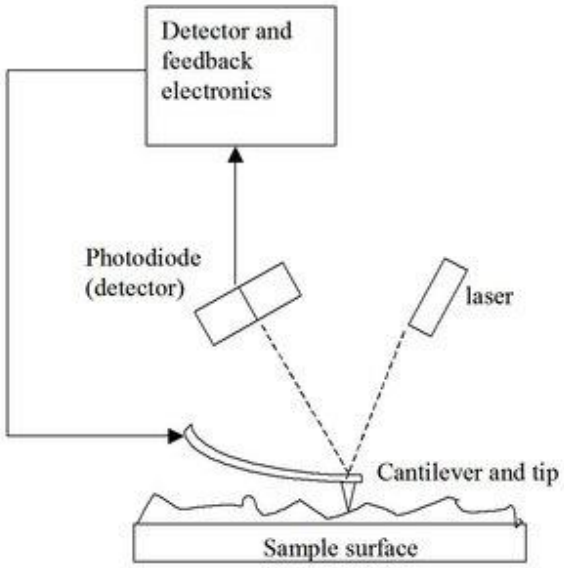


Figure 3-15: Atomic Force Microscope block diagram incorporating beam deflection detection [92].

3.7 Conclusion

In this chapter, the growth, fabrication and characterisation technologies involved in this work for GaN HEMT development have been introduced. The operation principles of these techniques have been studied and a connection to each cleanroom tool associated with them has been made.

4 Enhancement Mode GaN HEMT Techniques

Epitaxial layer engineering for tuning the threshold voltage can be provided either during growth or at the fabrication processing level. As discussed in Chapter 2, polarisation phenomena dictate the inherent 2DEG carrier concentration in the channel of GaN-based HEMT devices. The general means for obtaining positive threshold voltage as required for enhancement mode (e-mode) device operation, is to engineer the channel conduction band to be above the Fermi level at zero gate bias. In this chapter, some of the reported techniques to achieve e-mode operation will be presented.

4.1 Recess Etching of Barrier Layer

A reduction of the barrier layer thickness in a GaN-based heterostructure can lower polarisation induced 2DEG density hence enabling enhancement mode operation. Typically, dry or wet etching is performed to thin down the semiconductor region under the gate, until the conduction band in the channel shifts above the Fermi level at zero gate bias. Transistors fabricated by fully removing the barrier under the gate have been reported [93]. Etching is typically only applied under the gate, so that device on-resistance is kept low.

The gate recess etch depth can be adjusted so that barrier layer is only partially removed and the gate to channel distance is reduced. The remaining barrier layer thickness should be smaller than a critical thickness that can enable 2DEG generation. A complete barrier removal causes etch related damage on the GaN layer and may increase the surface roughness of the etched area, hence lower the device electron mobility and increase on-resistance.

Thus, the presence of at least a thin barrier layer is beneficial for e-mode device development, as high mobility 2DEG would still be present under operating conditions and full channel depletion would be ensured under no gate bias (see Figure 4-1).

Plasma dry etching methods are predominantly employed for barrier layer thinning and some typical fabrication procedures were described in Chapter 3. Regarding wet etching, the high inertness of GaN makes wet etching application

challenging. However, considering the high degree of threshold voltage deviation with small barrier thickness variations, other unexplored means of etching needed to be assessed. This led to the adoption of a novel platform based on a dual barrier epitaxy with a GaN layer for etch stop. Etching processes on these materials, including a damage-free plasma etching technique are described in Chapter 6.

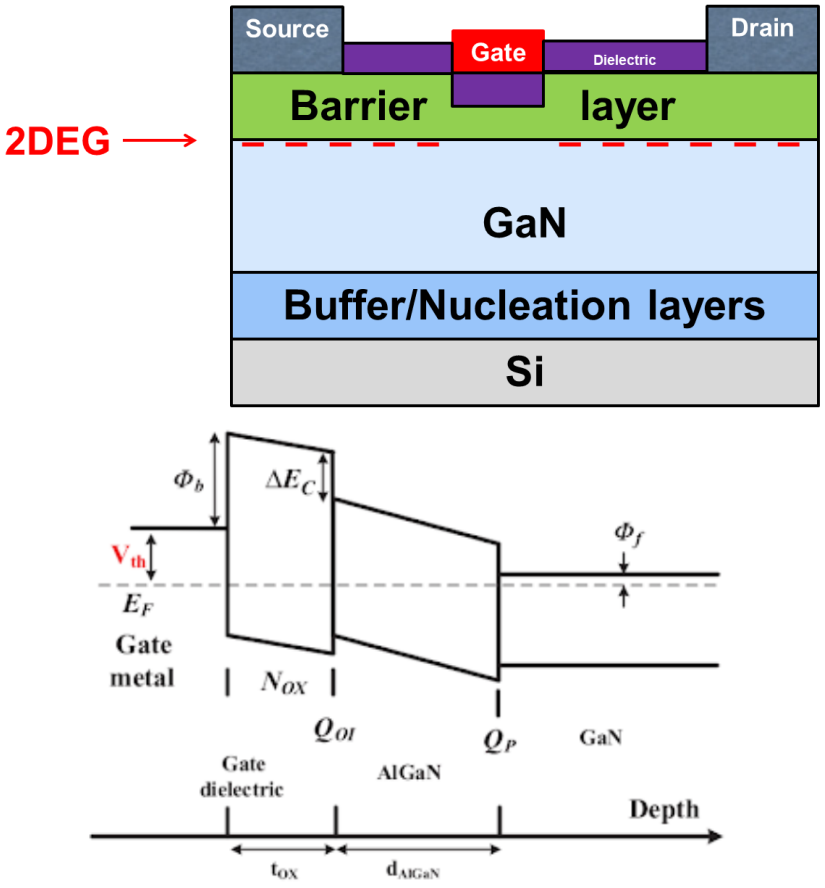


Figure 4-1: Gate recessed GaN MOS-HEMT and its associated band diagram [94].

4.2 Sub-critical Thickness Barrier Layer

As mentioned in the previous section, a gate recess process for the realisation of enhancement mode operation relies on thinning down the barrier layer underneath the gate below a certain thickness. Nevertheless, the growth of semiconductor wafer of sub-critical dimension barrier is also generally possible, thus eliminating the necessity for a gate recess etch process. Devices fabricated on an ultra-thin AlGaN barrier have been previously demonstrated [95]. They require a gate overlapping the area between the drain and source contacts for

operation, due to the barrier thickness being inadequate for a conductive access region (Figure 4-2). Breakdown voltage of these devices is limited to the dielectric strength, because the gate to drain contact distance is minimal. A workaround of this issue is through selective regrowth of the barrier layer; however this can introduce further processing complications. Sub-critical barrier thickness transistors can be used as low voltage HEMTs in a cascode configuration as will be described in Chapter 7.

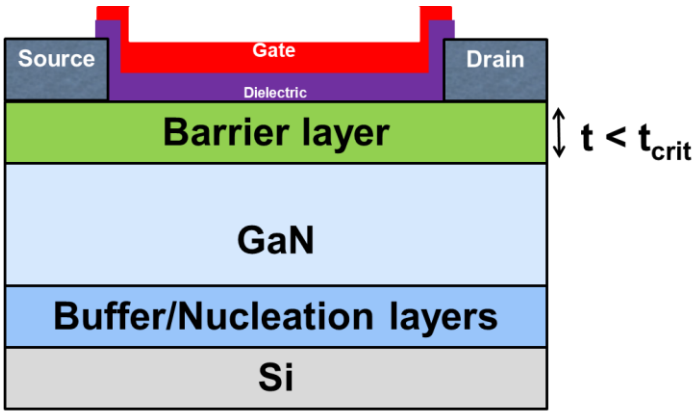


Figure 4-2: Sub-critical barrier layer thickness MIS-HEMT.

4.3 Fluorine Doping

A shallow fluorine ion implantation into the barrier layer under the gate can be applied through means of plasma (e.g. CF_4) [96]. A layer diagram of an e-mode device with substrate fluorine doping is depicted in Figure 4-3. Fluorine atoms possess the strongest electronegativity among chemical elements, which makes them a good choice for charge engineering the group III-nitride heterostructures by modulating the local potential. When F- doping is applied, it is believed that the F- ions introduce negatively charged acceptor-like states close to the mid-bandgap of the barrier layer [97]. These negative charges lead to an upward bending of the barrier layer conduction band and an increased barrier height [98]. With sufficient F- ion levels, the channel 2DEG can be completely depleted under zero bias conditions, hence enabling normally-off operation. Thermal stability of fluorine atoms in the doped region has been largely considered the cause of non- reproducible processing and unstable operation, however there have been significant improvements over the years [99]. Combination of recess etched and fluorine doped heterostructure has also been demonstrated to

provide e-mode operation [100]. Fluorine doping can also be employed in gate dielectrics to shift threshold voltage positively, as will be seen in Chapter 6.

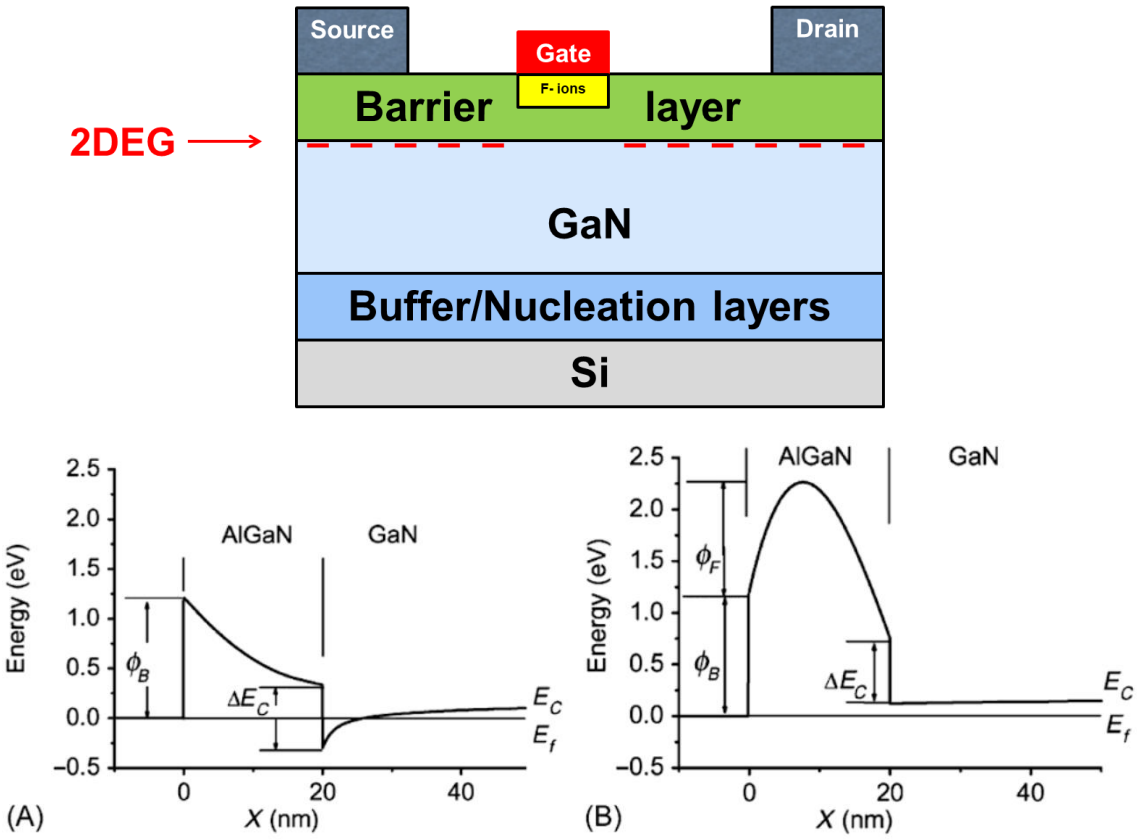


Figure 4-3: Normally-off fluorine treated GaN transistor and the effect of fluorine on the energy band diagram of an AlGaN/GaN HEMT [94].

4.4 p-AlGaN and p-GaN Gate

Gate injection transistors (GIT) make use of a p-type doped GaN or AlGaN layer under the gate to lift the conduction band of the heterostructure, resulting in a completely depleted 2DEG at zero gate bias. The p-type dopant is typically magnesium. The p-type doped layer is etched outside the gate region, so that the 2DEG depleting effect remains limited to the gate area. Overgrowth of a p-type semiconductor layer has been also demonstrated as a technique for p-type layer incorporation [101].

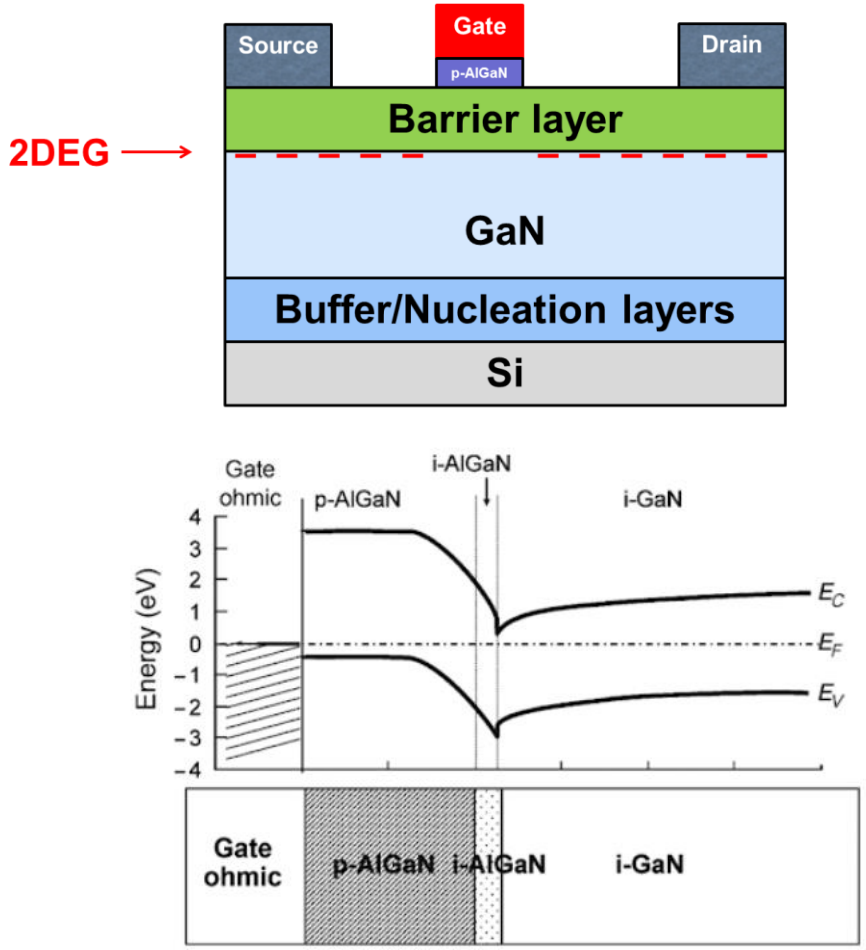


Figure 4-4: p-AlGaN enhancement mode HEMT structure and the band diagram of a p-AlGaN/AlGaN/GaN heterostructure [94].

A layer schematic of a p-AlGaN based HEMT is illustrated in Figure 4-4. With a positive gate voltage being applied, holes from the p-type semiconductor layer are injected into the channel region. The holes attract an equivalent number of electrons in the channel. Due to the effective mass of holes being much larger than that of electrons, the injected holes remain in the gate vicinity whereas the high mobility electrons, due to drain bias, are swept across and flow into the drain electrode increasing the drain current [102]. Since its proposal by Hu et al [103] and the demonstration of high voltage operation by Uemoto et al [104], this technique has been proven popular in the industry and transistors utilising it have been available commercially. Technological issues specifically related to the p-type layer incorporation that can limit device operation are described in [105]. Fabrication of p-type (Al)GaN devices typically requires recess etching of the p-type layer from the device access regions. This process can induce etch damage on the device [106]. Compared to MIS-HEMT type devices threshold

voltages are typically lower in p-type (Al)GaN devices, a factor which can limit their suitability for high voltage applications.

4.5 Other Normally-off Transistor Fabrication Methods

Similar principles involving charge management and polarisation engineering have been reported in the literature. Incorporation of an InGaN cap to raise the conduction band of the AlGaN/GaN interface leads to a threshold voltage shift to the positive direction [107]. Thermal annealing cycles were found to enhance positive dielectric/semiconductor interface fixed charges when a recessed channel is already established, hence shift the HEMT threshold voltage positively [108].

Vertical type HEMTs are attractive for power applications owing to their theoretically higher output power density per wafer area compared to lateral variants [109]. Due to the 2DEG not being formed vertically during growth as well as many vertical device structures requiring p-type GaN or epitaxial regrowth, the complexity and device fabrication cost is very high. N- face oriented GaN devices are also being studied as they give good grounds for expecting lower resistance contacts since the channel can be accessed through a lower bandgap material (GaN) [110]. As with sub-critical barrier thickness Ga-face devices, the gate region may be designed to be etch-free, with only modification of the access region being necessary. However, material growth of N- face GaN has been proven more challenging than the growth of Ga- face counterparts and this factor has limited to an extent their traction in the research domain. Comparable to the cascode structure (see Chapter 7), other enhancement mode dual-gate designs can be found in the literature, employing a normally-off transistor that is required to control the operation of another device [111].

4.6 Conclusion

In this chapter, a brief summary of the current state of group III-nitride normally-off device fabrication efforts reported in the literature is presented. The common theme in the purpose of these methods is direct charge introduction in the semiconductor and/or polarisation tuning through mechanical

or electrical means. All current e-mode device fabrication techniques present unique challenges either during post growth fabrication processing (e.g. fluorine treatment, gate recess) or even or even during growth (e.g. p-type AlGaN). In gate recess techniques, selectivity in removing barrier material is desirable for accurately controlling HEMT threshold voltage. In the next chapter the design choices and fabrication techniques of transistors realised in this work will be detailed.

5 Depletion Mode InAlN/AlGaN/GaN Transistors

This chapter is dedicated to the development and performance analysis of depletion mode InAlN/AlGaN/GaN on Si transistors. This includes a description of the design goals and required tools to fulfil them, the dedicated fabrication procedures followed and the characterisation results obtained.

Characterisation outcomes obtained include buffer leakage measurements, optimisation of ohmic contacts using different metal stacks and annealing temperatures, a study of the role of InAlN layer thickness on device performance and the assessment of the impact of different gate metals on threshold voltage and gate leakage current characteristics. The effect of SiN_x dielectrics deposited on the gate stack or the active region of InAlN/AlGaN/GaN devices was assessed. The influence of SiN_x stress on material transport properties was also explored.

5.1 Epitaxial Layer Design of Material Structures

First step in realising GaN HEMT device technologies is identifying suitable material structures for transistor development. As discussed in Chapter 2, polarisation phenomena dictate the inherent 2DEG carrier concentration in a group III-nitride heterojunction. The AlGaN/GaN heterojunction has been the most extensively studied due to the high electron mobility and saturation electron velocity in the 2DEG channel, the large breakdown field of the alloys involved and its long history of growth. Compared to AlGaN/GaN, the higher spontaneous polarisation of InAlN enables the InAlN/GaN heterojunction to induce higher quantum well charge density, hence reducing channel resistance and allowing for higher transistor drive current [112]. Amongst alloys in the nitride system, InAlN possesses the widest range of bandgaps, which can be valuable for good carrier confinement to the HEMT channel [113]. As InAlN can be grown to have the same lattice constant as GaN, i.e. lattice matched, wafer strain can be reduced, surface morphology can be improved and lower defect density can be obtained [114]. Choice of Ga- face crystal orientation is determined by a higher material growth reliability standpoint.

Hiroki et al [7], [115]–[117] have previously demonstrated the growth of InAlN/AlGaN/AlN/GaN on sapphire (Al_2O_3) substrates. By testing Schottky gate

HEMT based on these structures, they reported an improvement in gate leakage current and sub-threshold swing compared to devices that use an InAlN/AlN/GaN based structure with a similar barrier height. AlGaN as an interlayer was reported to improve surface morphology and led to increased electron mobility in InAlN/AlGaN/AlN/GaN structures.

As discussed in Chapter 2, substrate choice is important for the potential that group III-nitride materials, such as multi-barrier layer GaN heterostructures, present in power electronics applications. As Baliga suggests [118], an extension of the technology to silicon substrates will be cost-effective and important for future commercialisation.

With regards to threshold voltage, transistors based on an InAlN/AlGaN/GaN structure are normally-on. Several approaches have been demonstrated to develop GaN based enhancement mode devices; fluorine doping [5], [96], p-AlGaN [119], p-GaN [120] or InGaN cap layer [121] at the gate region, gate recess [122], sub-critical barrier thickness AlGaN [8] among others.

The latter technology incorporates thin (~3nm) AlGaN barrier on GaN, which is below the critical thickness required for enhancement mode operation [8]. Metal-oxide-semiconductor (MOS) HEMT that make use of a thin AlGaN barrier exhibit a +3 V threshold voltage [8]. This reveals that if the InAlN layer of an InAlN/3 nm AlGaN/GaN dual barrier structure can be removed, an enhancement mode transistor can be fabricated when the transistor gate is fabricated over a 3 nm AlGaN/GaN structure as shown in Figure 5-1.

The GaN interlayer depicted between InAlN and AlGaN can serve as a potential etch stop layer if suitable etching techniques are applied, and this will be examined in Chapter 6. Another incentive behind this choice is that, if dielectrics are deposited on the semiconductor, their screening on both the etched and the non-etched areas would be compatible with the more widely used GaN/dielectric interface rather than the less widely reported AlGaN/dielectric boundary.

Compared to a plethora of reports that incorporate a thin AlN interlayer in AlGaN/GaN heterojunctions, there is no AlN grown between the AlGaN and GaN

layer in this layer structure, so that the surface morphology is not compromised due to the greater lattice mismatch between AlN and GaN. The absence of the AlN layer was also important for maintaining a positive threshold voltage after the etching of InAlN.

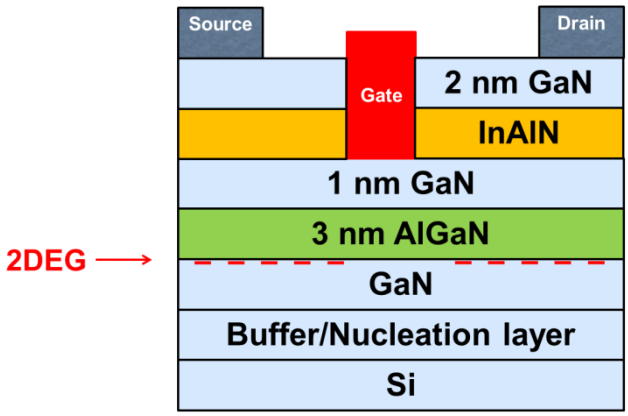


Figure 5-1: Enhancement mode GaN HEMT employing an InAlN layer and a thin AlGaN layer.

In comparison to devices fabricated on inherently enhancement mode materials, such as 3 nm AlGaN/GaN wafers, there is no requirement for a gate overlapping the source and drain of the transistor to enable normally-off operation. When a gate overlap topology is incorporated (Figure 5-4), gate-to-drain breakdown voltage is determined by the dielectric strength. Since obtaining positive threshold voltage requires depositing gate dielectrics of typically < 100 nm thicknesses, high voltage operation is non-achievable even if high-κ dielectrics are used. Without this restraining factor being present, higher breakdown voltages can be enabled.

From a device modelling standpoint, material properties and geometrical characteristics were used as an input to simulate the band diagram of the heterostructure under the gate in an as-grown (InAlN is present) structure and a structure that has the InAlN layer removed. Without any gate bias applied, there is 2DEG present before etching (Figure 5-2), whereas removal of the InAlN barrier under the gate leads to a depleted heterojunction (Figure 5-3).

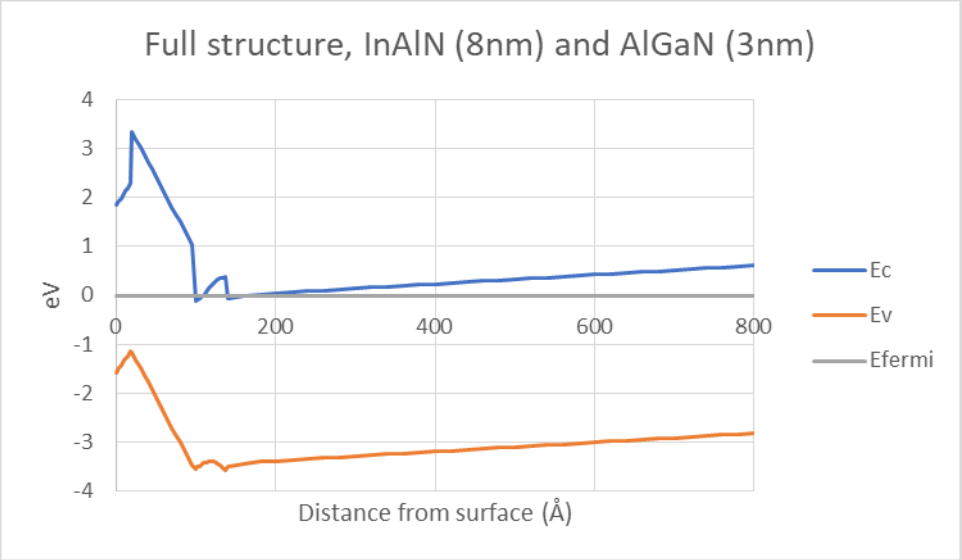


Figure 5-2: Simulated band diagram of the dual barrier HEMT structure (courtesy of Dr Matthew Smith).

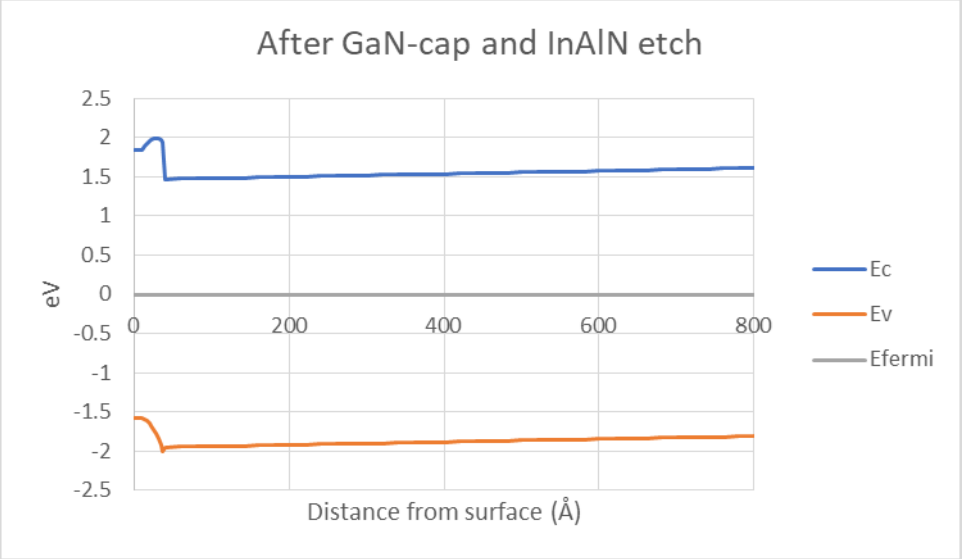


Figure 5-3: Simulated band diagram of HEMT structure with a recess etched gate (courtesy of Dr Matthew Smith).

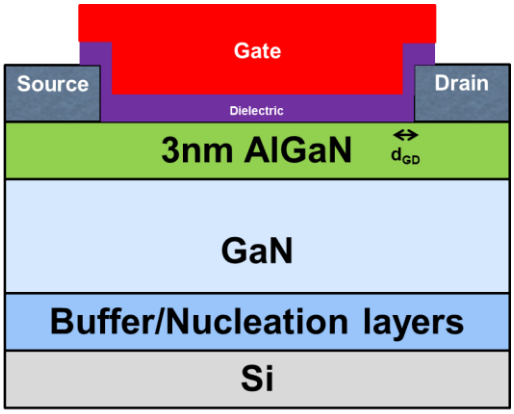


Figure 5-4: HEMT device on normally-off 3nm AlGaN/GaN material with a gate overlapping the source and drain contacts.

5.2 Material Growth

Following material design considerations for the InAlN/AlGaN/GaN epitaxial layers, multiple wafers were grown in a MOCVD reactor at the Cambridge Centre for GaN on 6" Si substrates. The wafers differed in terms of the thickness of the InAlN barrier layer (Table 5-1). From the surface, the epitaxial layers consisted of a 2 nm GaN capping layer, the InAlN barrier layer, lattice matched to GaN, a 1 nm GaN layer, a thin 3 nm $Al_{0.25}Ga_{0.75}N$ layer, a 200 nm GaN channel layer, a total of 3.6 µm carbon-doped GaN buffer and compositionally graded $Al_xGa_{1-x}N$ transition layer and a 250 nm AlN nucleation layer. The C- doped buffer structure was adopted to improve the breakdown voltage and its development was optimised among project partners at Cambridge, Bristol and Sheffield universities.

Table 5-1: InAlN/AlGaN/GaN wafer ID and InAlN thickness.

Wafer ID	InAlN thickness (nm)
P793	8
P794	6
P795	5

Growth temperature was 1130 °C for AlN, 980 °C for the graded AlGaN transition layer, 970 °C for the C- doped GaN buffer layer, 1045 °C for the GaN capping layer as well as $Al_{0.25}Ga_{0.75}N$ layer and 795 °C for the InAlN layer.

Upon delivery, wafers were covered by photoresist and were then commercially diced by Loadpoint or at the Particle Physics Experiment group within the School of Physics and Astronomy at the University of Glasgow. Chips of 18mm x 18mm, 20mm x 20mm or 35mm x 35mm were produced, depending on photomask dimensions, ease of processing, compatibility with the maximum loading stage sizes of tools, such as the equipment used for forming gas annealing.

5.3 Device Structure Layout and Photomask Design

Design of photolithography masks were realised using Tanner L-Edit CAD (computer aided design) software. The software enables design of separate layers, called cells, each corresponding to a processing step that requires resist exposure. The photomasks were commercially sourced and fabricated via e-beam lithography process on quartz substrates.

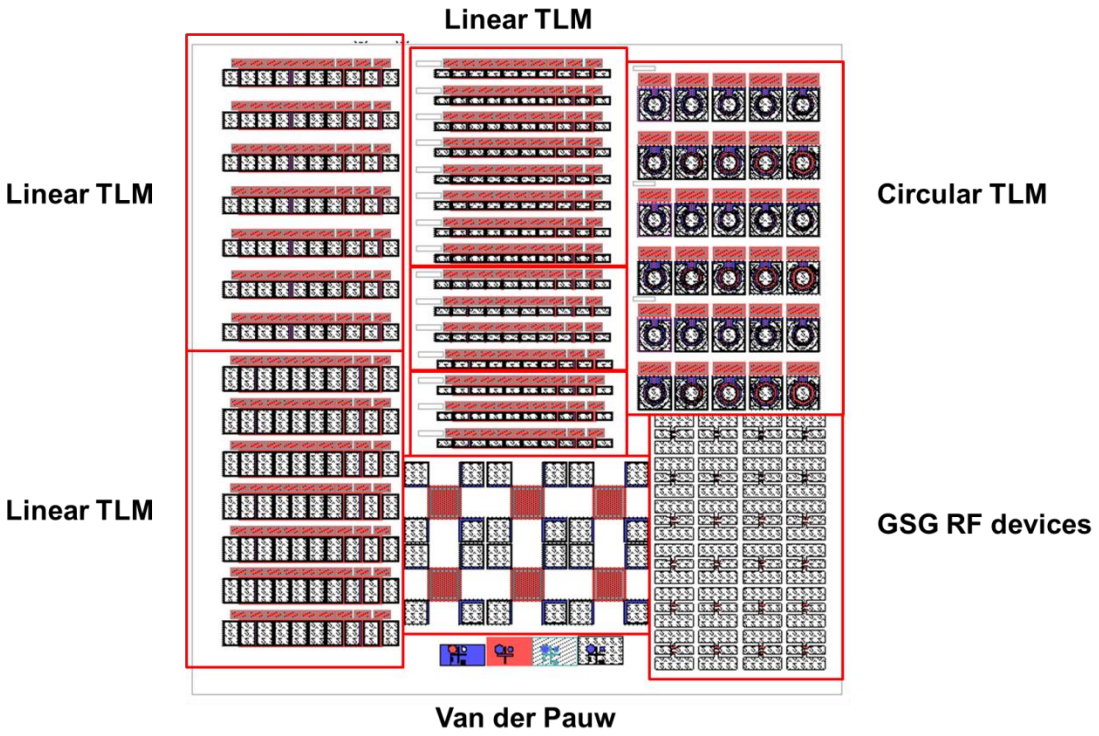


Figure 5-5: Screenshot of ohmic contact optimisation mask design, depicting linear and circular TLM structures of different physical dimensions, Van der Pauw structures and RF device characterisation structures. Different colours represent separate photolithography steps.

Multiple layers were fabricated on the same substrate depending on the mask plate and layer dimensions. This was deemed useful for small area mask designs, such as for the mask set fabricated for ohmic contact optimisation and material transport characterisation (Figure 5-5).

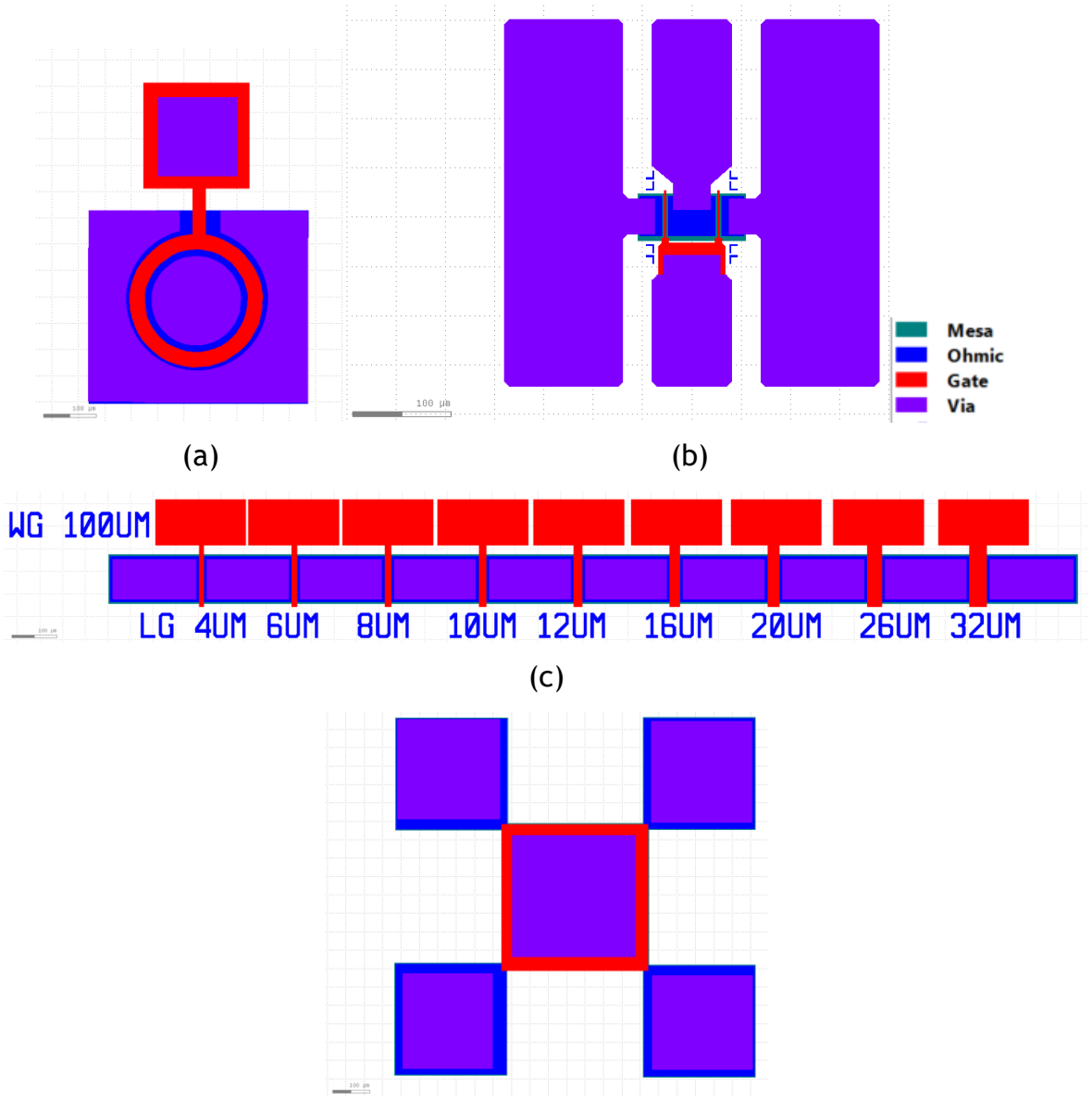


Figure 5-6: (a) A circular Transfer Length Method structure. (b) RF ground-signal-ground transistor, (c) Gated linear Transfer Length Method structures, (d) Van der Pauw structures.

This design layout of the ohmic contact optimisation mask is 18 mm × 18 mm in size and includes sets of alignment markers, circular and linear TLM structures, Van der Pauw structures, and RF ground-signal-ground (GSG) structures (Figure 5-6). Alignment markers are features of high precision which are used as

reference when positioning subsequent patterns using the mask aligner tool. Vias refer to dielectric film etching processes which allow for metal contact probing.

Each layer of the ohmic contact optimisation photomask is divided in four areas of equal dimensions. This was so that sample cleaving after any processing step can enable the examination of the effect of consequent processing steps, given that the four areas have been exposed during the same processing steps prior to cleaving. Prior to cleaving, photoresist was spun onto the samples to protect the sensitive surfaces.

5.4 Fabrication Process

A simple process for fabricating depletion mode GaN HEMT is described below. The sample is first cleaned in acetone, before photoresist is spun on its surface to prepare for the first photolithography step. The appropriate photomask is loaded on the mask aligner and the sample goes through UV exposure and resist development. It is then transferred to an etching tool for mesa etching using chlorine or bromide-based etch process. Subsequently the remaining resist is removed in acetone. The etching of a mesa structure is followed by the ohmic contact lithography step, using the appropriate photomask and it is followed by the metal deposition and rapid thermal annealing steps to form the ohmic contacts. Next lithography step leads to the formation of the gate Schottky contact and may be preceded by dielectric deposition. In order to aid the measurement of the device electrical characteristics using measurement probes, a metal deposition step of a non-annealed metal is followed to form metal pads.

A simplified process diagram depicting the resulting HEMT structures in the end of each photolithography step is shown in Figure 5-7. The layout design for a HEMT device used for this process is also presented. This process flow can act as a baseline from which other process variations can be derived and performed. If additional passivation layers are deposited after metals, then via openings of the dielectrics are required prior to the metal pad lithography step. In this chapter, where a process for fabricating a particular device differs from the base process, this will be distinctly described in the relevant section.

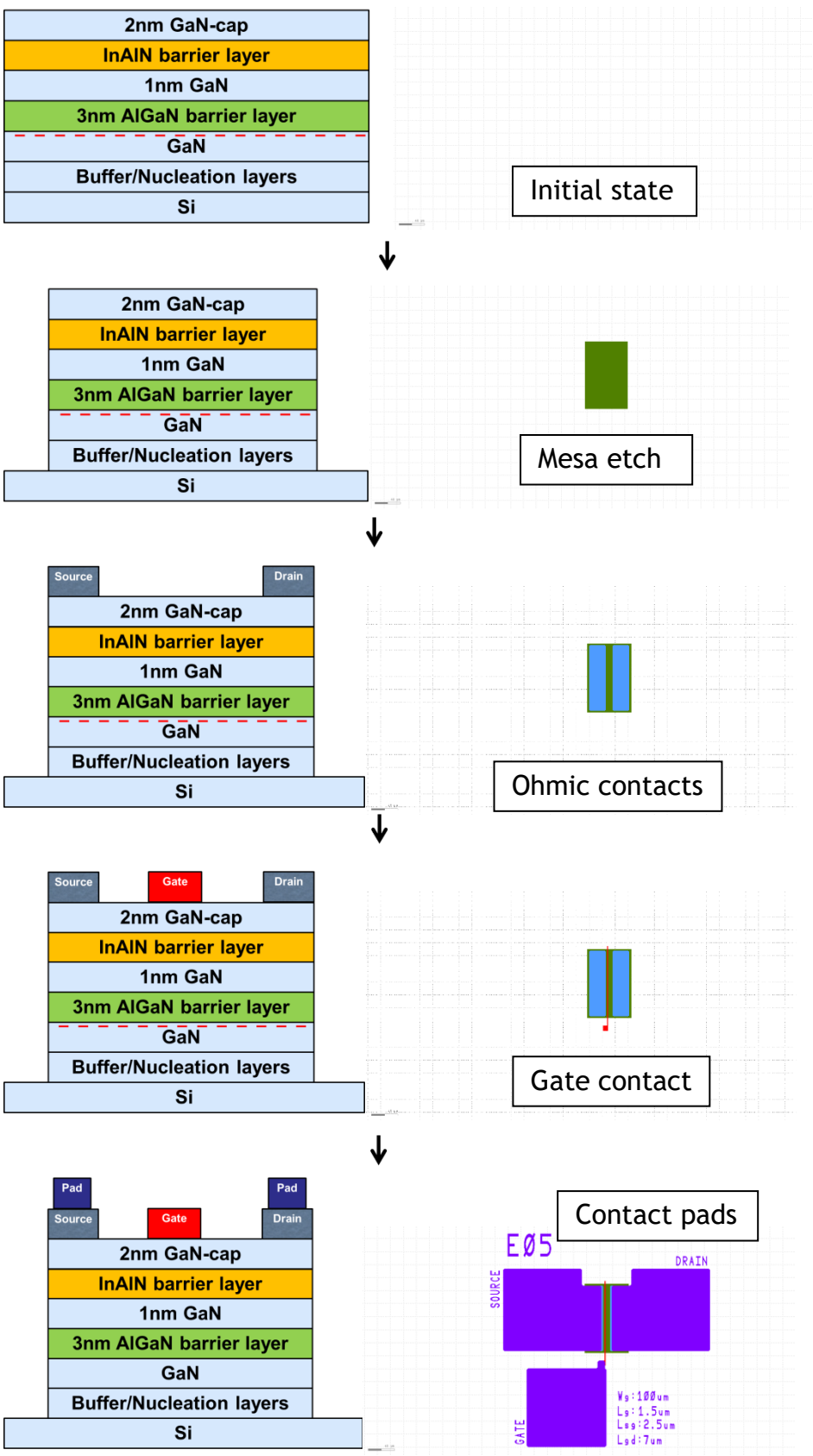


Figure 5-7: Simplified process flow for a Schottky gate device, showing mesa etch, ohmic contact & annealing step, Schottky gate and ohmic contact pad steps and corresponding photomask design used to fabricate it.

5.5 Transistors on InAlN/AlGaN/GaN-on-Si Materials

5.5.1 Ohmic Contact Development and Material Characterisation

Three samples were taken from diced InAlN/AlGaN/GaN-on-Si wafers, depicted in Figure 5-7, and device structures were fabricated on them. Each sample differed only on the thickness of the InAlN layer (5, 6 and 8 nm). The fabrication process started with a 630 nm mesa etch which was performed using $SiCl_4$ based RIE chemistry to electrically isolate each device's active area on the sample. Then, a Ti/Al/Ni/Au contact scheme with 30/180/40/100 nm metal thicknesses was evaporated and lifted-off and the contacts were annealed in ambient N_2 environment at 730-850 °C RTA temperatures for 30s. Van der Pauw and Transfer Length Method structures, the latter with contact pad separations from 4 to 32 μm were measured before and after annealing the contacts and the contact resistance and material transport properties were extracted.

Hall measurements taken at room temperature prior to annealing are shown in Table 5-2. An increase in Hall carrier concentration was generally observed with increased InAlN layer thickness, which is attributed to an increase in the heterojunction spontaneous polarisation induced charges for thicker barrier layers. An increase in Hall carrier concentration was correlated with a decrease in Hall electron mobility.

Table 5-2: Hall measurements taken via Van der Pauw structures prior to contact annealing.

	Pre-annealing Hall measurements		
Wafer barrier layers	**R_{sh} (Ω/sq)**	**μ_H (cm^2/Vs)**	**n_H ($x10^{13}$ cm^{-2})**
5nm InAlN / 3nm AlGaN	258.4	1700	1.417
6nm InAlN / 3nm AlGaN	266.4	1500	1.557
8nm InAlN / 3nm AlGaN	290.4	1200	1.798

As shown in Figure 5-8, for annealing temperature in the 730 °C to 800 °C range an overall trend towards increased sheet resistance values was observed when the InAlN barrier thickness is increased. In the same 730 °C to 800 °C range any

increase in electron concentration is correlated with a simultaneous decrease in Hall mobility (Figure 5-9), perhaps because electrons cannot be fully contained in the quantum well [28].

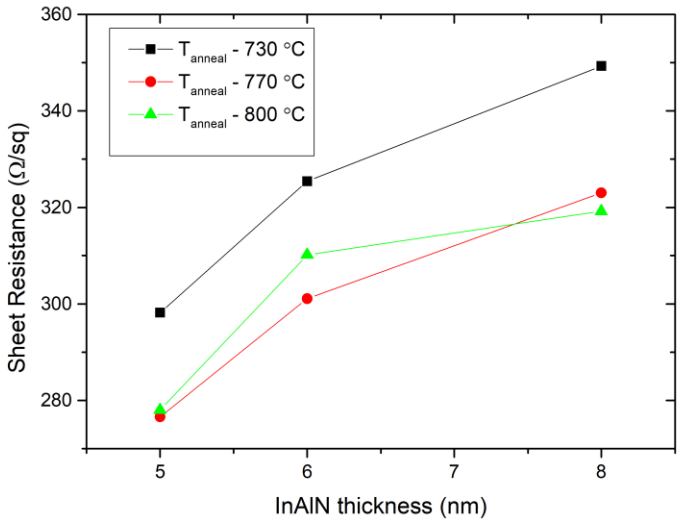
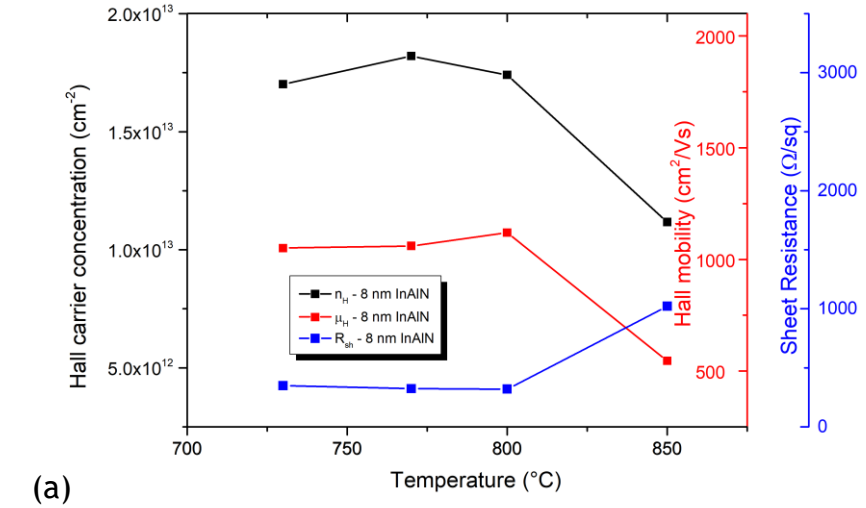
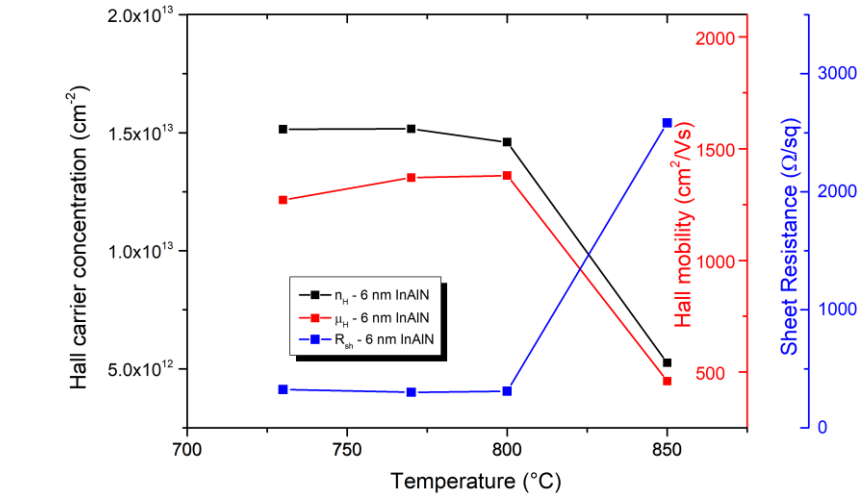


Figure 5-8: Variation in InAlN/AlGaN/GaN material sheet resistance with different InAlN thicknesses, as extracted via Hall measurements.

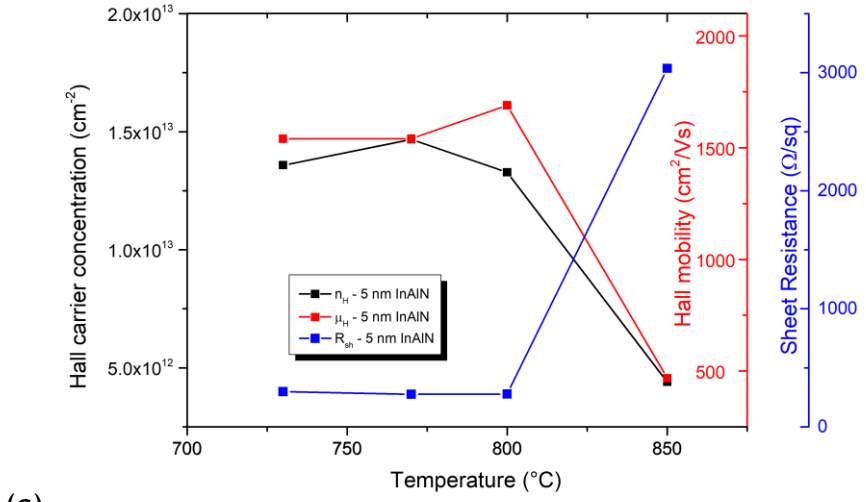
Annealing contacts at 850 °C led to a great increase in sheet resistance. It is worth pointing out that the InAlN layers were grown at 795 °C and that the samples that use the thickest 8 nm InAlN layer are the least affected by 850 °C annealing temperatures, whereas the most affected samples were those utilising the 5 nm InAlN barrier, the thinnest barrier layer of the three. This indicates that the wafers incorporating a thicker InAlN layer exhibit higher thermal stability.



(a)



(b)



(c)

Figure 5-9: Hall measurements, depicting sheet resistance R_{sh}, carrier concentration n_H and mobility μ_H for different annealing temperatures for wafer incorporating (a) 8 nm, (b) 6 nm and (c) 5 nm InAlN barrier layer.

Table 5-3: Summary of TLM measurements on dual barrier wafers for different annealing temperatures.

		Transfer Length Method	
Wafer	**Ti/Al/Ni/Au RTA conditions**	**R_c (Ω mm)**	**R_{sh} (Ω/sq)**
5nm InAlN / 3nm AlGaN	730°C 30s	0.837	388.2
	770°C 30s	0.948	272.5
	800°C 30s	0.557	300.5
6nm InAlN / 3nm AlGaN	730°C 30s	0.823	308.7
	770°C 30s	0.67	300.1
	800°C 30s	0.727	317
8nm InAlN / 3nm AlGaN	730°C 30s	0.902	340.4
	770°C 30s	0.674	306.7
	800°C 30s	0.544	344.6

As deposited, metal contacts exhibited Schottky-type characteristics. Contact annealing was required to obtain ohmic dependence, which allows TLM structures to be measured. A summary of TLM measurements after contact annealing is shown in Table 5-3. The lowest contact resistance values were obtained at either 770 °C or 800 °C annealing temperatures. As previously discussed, annealing at 850 °C induced thermal damage on all samples, which manifested as severe deterioration in sheet resistance. For these temperatures, contact resistance values were not accurately extracted.

5.5.2 Buffer Leakage Measurements

If leakage current levels are suppressed by growth and processing means, breakdown voltage scales with increased gate-drain distance [123]. In order to assess the suitability of InAlN/AlGaN/GaN wafers for sustaining high breakdown voltages, buffer leakage test structures were fabricated. These structures consisted of ohmic metal contacts, deposited on as-grown substrates, with the substrate material around and between them etched (Figure 5-10). The contact distances were in the range 3-12 μm. The process steps followed were ohmic contact formation, by depositing Ti/Al/Ni/Au metal stacks on the semiconductor surface and then annealing them using RTA at 770 °C. Each ohmic contact was then isolated from other structures via a ~ 600 nm mesa etch, performed by $SiCl_4$

-based RIE. The etch process involved 15 minute plasma exposure at 200 W RF power and 8 mTorr pressure.

Then, if a voltage is applied between two of the contacts the current measured is the leakage component that corresponds to the semiconductor layers present, i.e. through the surface and the bulk of the buffer layers, since the upper semiconductor layers have been etched. Buffer leakage measurements for varying distances between the metal contacts are shown in Figure 5-10c. Maximum currents measured when a 200 V voltage was applied were in the order of 10^{-4} mA/mm for all pad separations. Keeping buffer leakage currents below 10 μA/mm is important for transistor development, as it is the influencing the drain-source off state leakage characteristics in HEMT.

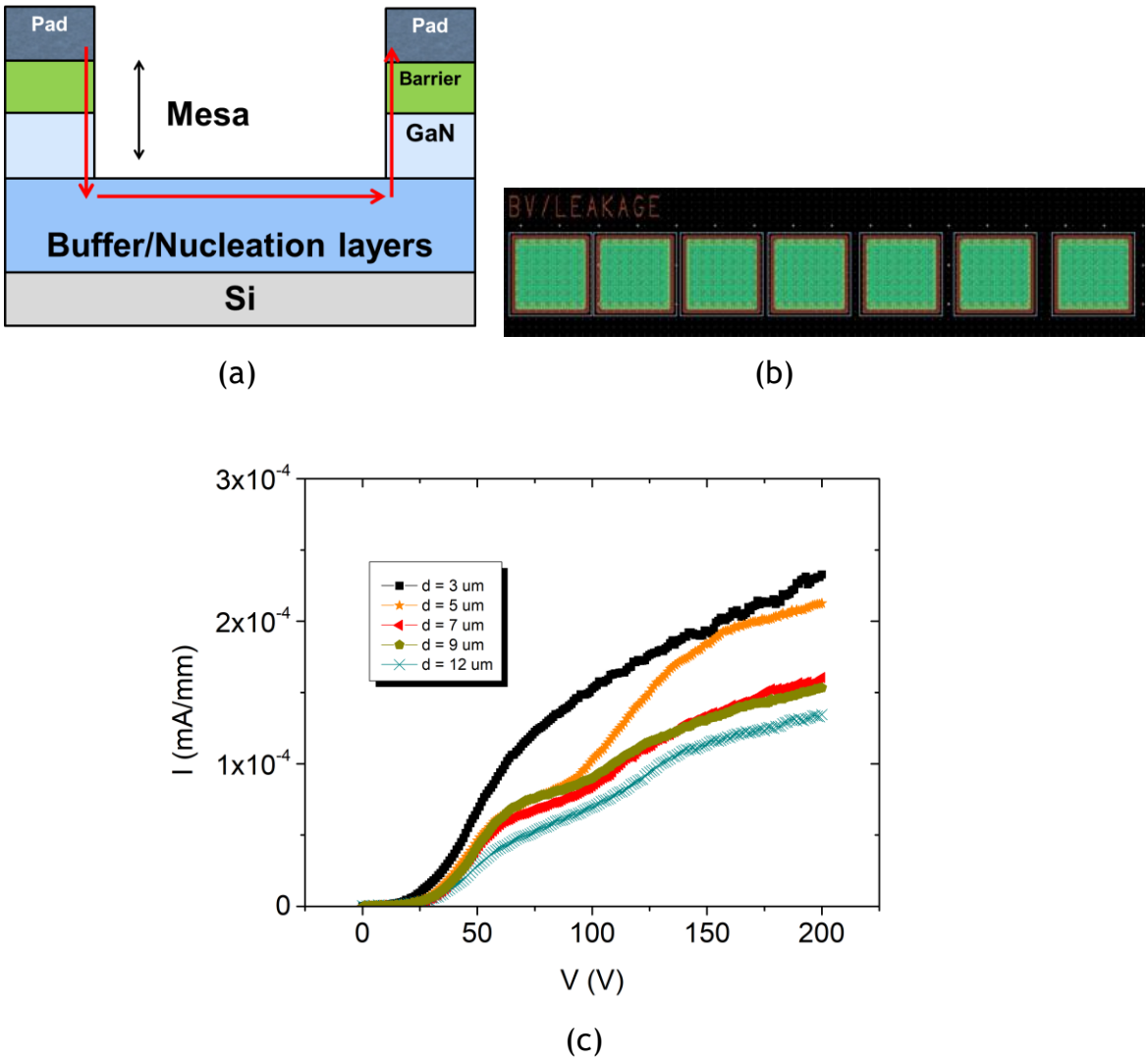
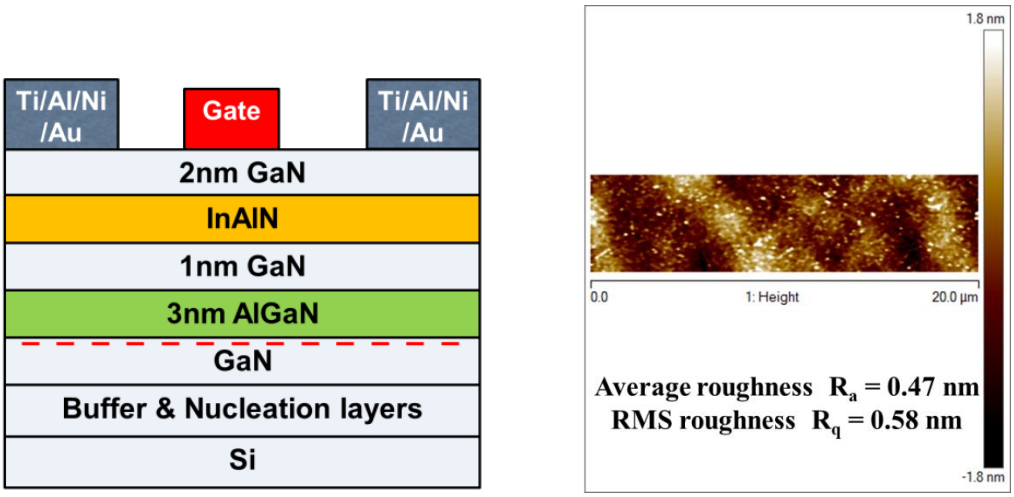


Figure 5-10: (a) Buffer leakage test structure layer diagram, (b) mask design. (c) Buffer leakage current vs applied voltage for different pad distances.

5.5.3 Normally-on Transistor Characterisation Data

High electron mobility transistors were fabricated initially on samples taken from InAlN/AlGaN/GaN wafers of 8 nm InAlN thicknesses. Device fabrication process began with a ~600 nm mesa etch, patterned using optical lithography and defined by RIE $SiCl_4$ chemistry. Electron beam evaporated Ti/Al/Ni/Au metal stacks of 30/180/40/100 nm thicknesses respectively were lifted-off and then thermally annealed at 770 °C for 30s in N_2 environment. Gate contacts of Pt/Au metal stacks, of 20/200 nm thickness were e-beam evaporated and lifted-off.



(a) (b)

Figure 5-11: (a) HEMT layer diagram. (b) Surface AFM scan of wafer.

Carrier transport measurements were taken at room temperature by Van der Pauw measurements. Hall channel electron density was ~1.6 x 10^{13} cm^{-2}, Hall mobility μ_H was ~1290 cm^2 V^{-1} s^{-1}, resulting in a sheet resistance R_{sh} ~ 301 Ω/sq. Transfer length method evaluation of ohmic contacts at room temperature showed a contact resistance of 0.44 Ωmm and a sheet resistance R_{sh} ~277 Ω/sq.

DC measurements were taken from transistors of 3 µm gate length, gate width of 100 µm, 3 µm gate-source distance and gate-drain distances ranging from 4 µm to 26 µm. A summary of the performance metrics extracted from these measurements is presented in Table 5-4.

Table 5-4: Summary of parameters of 8 nm InAlN/AlGaN/GaN HEMT.

Metric	InAlN/AlGaN/GaN-on-Si HEMT
Contact resistance	~ 0.44 Ω mm
Sheet resistance	~ 277-301 Ω/sq
Hall carrier concentration	~ 1.60 *10^{13} cm^{-2}
Hall mobility	~1540 cm^2/Vs
Maximum drain-source current	~ 1 A/mm
Maximum transconductance	~ 198 mS/mm (L_{GD} = 4 µm)
Sub-threshold swing	~ 65.6 mV/dec (L_{GD} = 14 µm)
On-resistance	~ 4.07 Ω mm (L_{GD} = 4 µm)
Threshold voltage	~ -3.4 V (L_{GD} = 4-26 µm)

Transistor on-resistance was extracted from the gate transfer characteristics for 50 mV drain bias. Drain currents, threshold voltage and maximum extrinsic transconductance were extracted from the gate transfer characteristics for 10 V drain bias.

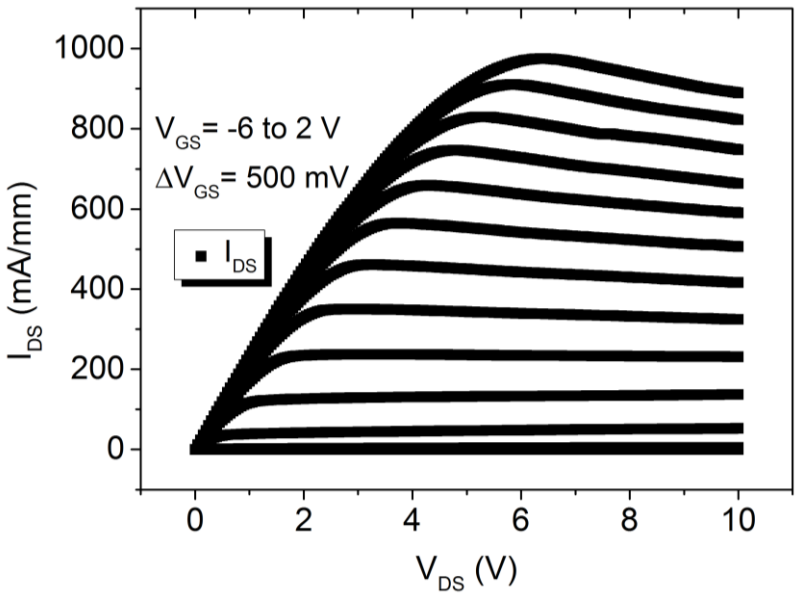


Figure 5-12: DC output curves of 8 nm InAlN/AlGaN/GaN-on-Si transistor with Pt- based gate metals. Device dimensions were W_G = 100 µm, L_G = 3 µm, L_{GD} = 4 µm, L_{GS} = 3 µm.

The current–voltage output characteristics are depicted in Figure 5-12. The drain-source voltage was swept from 0 to 10 V whilst the gate-source voltage was kept constant for each sweep. After each drain voltage sweep was finished, the next sweep was performed for a 500 mV increments of gate-source voltage.

Transfer characteristic curves of five devices, which utilise source-drain ranging from 4-26 µm, are depicted in Figure 5-13. The other geometrical characteristics, including gate width, length and gate-source distances were identical. As seen in the figure, maximum currents, as extracted at V_{DS} = 10 V and V_{GS} = 3 V, were reduced by ~40 % when source-drain distance increased from 4 µm to 26 µm. The transconductance values extracted for higher (V_{GS} > 0.5 V) voltages showed significantly more variance compared to those extracted for lower V_{GS} values. As the gate leakage currents were maintained low across all gate voltage ranges, some possible causes include drain-source related scattering or self-heating effects. Other potential causes include probing or measurement issues, as a small gate voltage step size has been used.

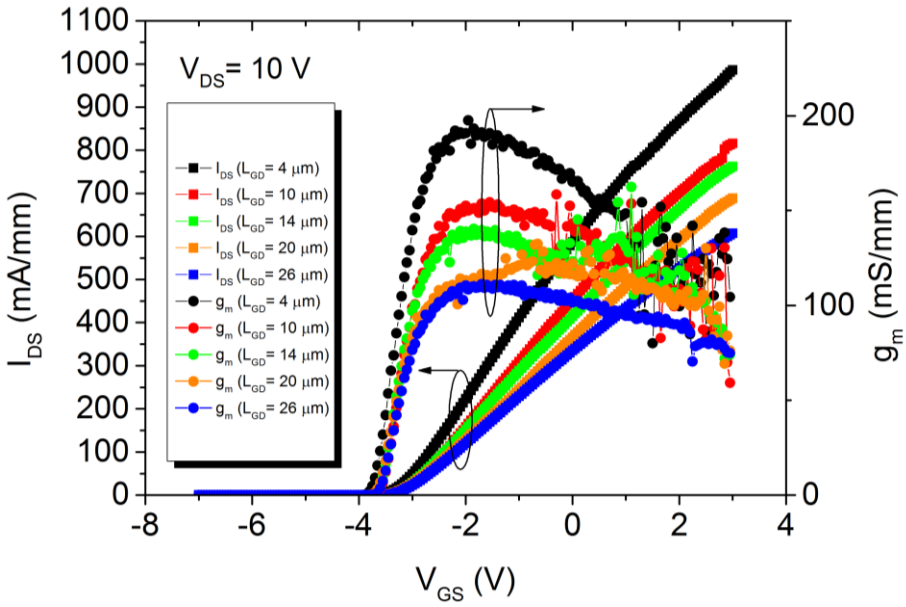


Figure 5-13: Transfer characteristics of 8 nm InAlN/AlGaN/GaN-on-Si HEMT as source-drain distance increases. Device dimensions were W_G = 100 µm, L_G = 3 µm, L_{GD} = 4 µm, L_{GS} = 3µm.

Transfer characteristic curves of these devices in semi-logarithmic scale, also depicting gate leakage currents, are illustrated in Figure 5-14. Gate leakage currents and drain-source off-state leakage currents were largely lower than 1 µA/mm values. As seen in the transistor off-state region, gate and drain-source off-state current leakage values were identical. This indicates that gate leakage was the dominant factor that determined off-state drain-source leakage.

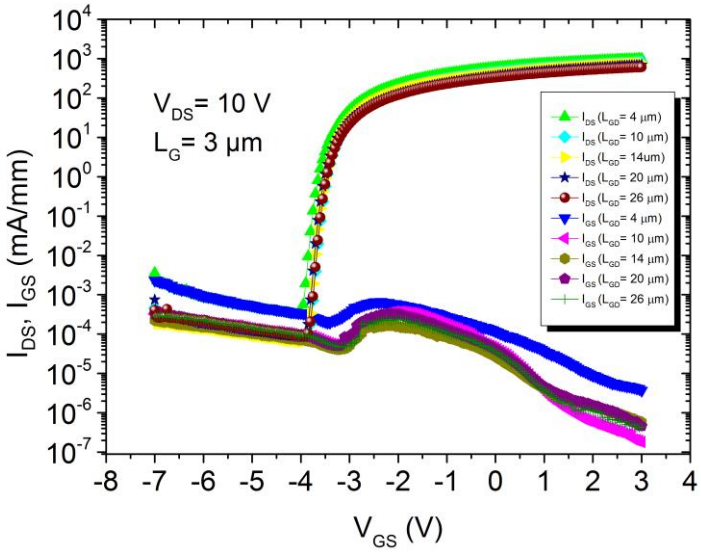


Figure 5-14: Transfer characteristics of 8 nm InAlN/AlGaN/GaN-on-Si HEMT for different source to drain separations in semi-logarithmic scale. Also depicted are gate leakage currents with respect to gate voltages. Device W_G = 100 µm, L_G = 3 µm, L_{GD} = 4 µm, L_{GS} = 3 µm.

5.5.4 Influence of Gate Metals on Device Characteristics

Metals possessing high work functions are commonly used as transistor gates, due to their larger Schottky barrier, which keeps gate leakage currents low. Nickel is the most commonly used metal, as it combines high work function with strong adhesion to GaN.

Two metal stacks, Pt/Au and Ni/Au of 20/200 nm thicknesses, were evaporated by e-beam as Schottky gates of 8nm InAlN/AlGaN/GaN-on-Si transistors. A comparison in HEMT gate leakage characteristics is shown is shown in Figure 5-15. A greater than two orders of magnitude reduction in gate leakage was observed via the use of Pt-based contacts across all gate voltages and there were not any adhesion problems observed. For gate-source voltage V_{GS} = -4 V, gate leakage current was reduced from 0.6 mA/mm for Ni/Au gate contacts to 3.4 * 10^{-4} mA/mm for Pt/Au contacts. For gate-source voltage V_{GS} = 3 V, the Ni/Au based gate contacts exhibited 1 mA/mm gate leakage current whereas the gate leakage current for the Pt/Au gate contacts was 3.7 * 10^{-6} mA/mm.

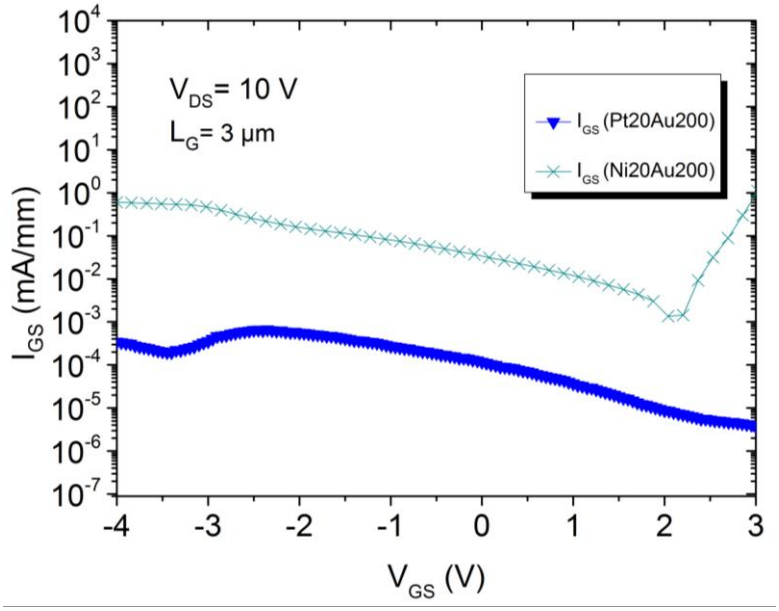


Figure 5-15: Comparison of Ni/Au and Pt/Au Schottky gate leakage currents. Device dimensions were W_G = 100 µm, L_G = 3 µm, L_{GD} = 4µm, L_{GS} = 3 µm.

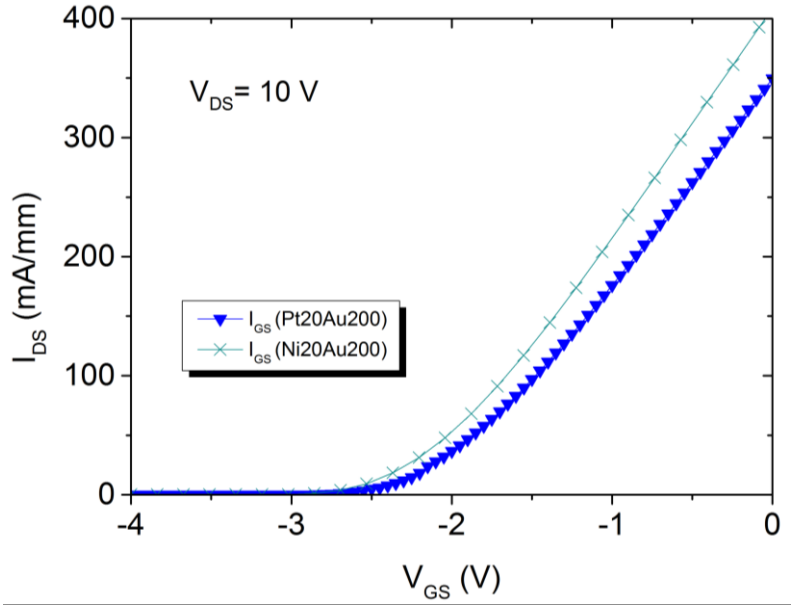


Figure 5-16: Transfer characteristics of transistors employing Pt/Au and Ni/Au gate metal stacks. Device dimensions were W_G = 100 µm, L_G = 3 µm, L_{GD} = 4 µm, L_{GS} = 3 µm.

As Pt possesses a higher work function than Ni by ~0.5 eV, the Schottky metal-semiconductor barrier height becomes higher and may result in a lower 2DEG density underneath the gate, which can manifest as a threshold voltage shift. This is observed in Figure 5-16, where the transfer characteristics of HEMTs employing the two metal stacks are compared. The device employing Pt/Au gates showed a positively shifted threshold voltage.

5.5.5 Influence of InAlN Thickness on Device Characteristics

The influence of InAlN thickness on HEMT device transfer characteristics is depicted in Figure 5-17, where two Schottky gate devices are compared. The gate metals were Ni/Au of 20/200 nm thicknesses. These devices differ only on the InAlN barrier thickness, which were 5 nm and 8 nm InAlN. As seen in Section 5.5.1, the incorporation of a thicker InAlN layer leads to increased 2DEG carrier concentration due to its higher heterojunction spontaneous polarisation. In fabricated transistors, this effect demonstrates itself as a shift in threshold voltage. Threshold voltage was ~ -3 V for the device fabricated on the 8 nm InAlN-based sample and ~ -1.6 V for device on the 5 nm InAlN wafer. For these devices peak extrinsic transconductance g_{max} values, ~ 203 mS/mm and ~ 194 mS/mm for 8 nm and 5 nm InAlN respectively, were observed. Given the higher sheet resistance of the 8 nm InAlN wafer, these results are due to a lower ohmic contact resistance measured compared to the 5 nm InAlN wafer (0.95 Ωmm for the 5 nm InAlN sample and 0.67 Ωmm for the 8 nm InAlN sample).

In this section, electrical characterisation data from transistors fabricated on InAlN/AlGaN/GaN-on-Si wafers were presented.

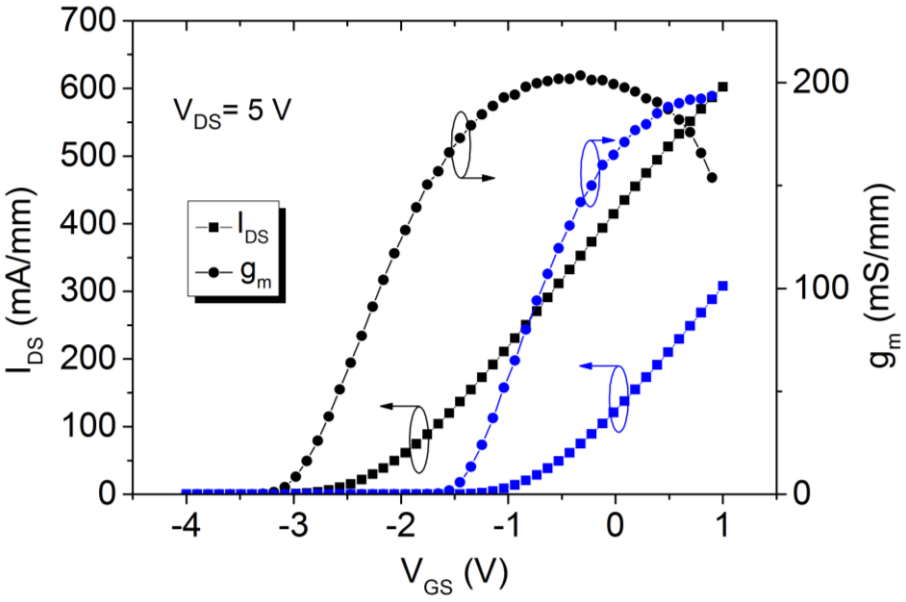


Figure 5-17: Transfer characteristic curves for 5 nm InAlN (blue) and 8 nm InAlN (black) wafers. A reduction in polarisation-induced charge for thinner (5 nm) InAlN, results in more positive threshold voltage. Device dimensions W_G = 100 µm, L_G = 3 µm, L_{GD} = 12 µm, L_{GS} = 3 µm.

5.6 SiN_x Passivation and Etching Effect on Devices

The effect of SiN_x on the current levels of InAlN/AlGaN/GaN devices was studied. For this experiment, Schottky gate devices were fabricated on an 8 nm InAlN barrier substrate of Figure 5-11. The fabrication process started with a mesa etch and was followed by Ti/Al/Ni/Au contact deposition of 30/180/40/100 nm thicknesses, annealing at 770 °C and deposition of Pt/Au contacts of 20/200 nm thicknesses to form the gate.

Following this, 70 nm SiN_x films were deposited on the surface by ICP CVD at room temperature. Deposition conditions were ICP power 200 W, platen power 0 W and chamber pressure was 5 mTorr. Current-voltage measurements were taken prior and after dielectric deposition. Subsequently, SiN_x dielectric was etched by SF_6, in order to examine whether the transistor state prior to passivation was recoverable.

A comparison of DC output characteristics for each process stage is shown in Figure 5-18. A slight increase in on-current levels for a given gate bias were observed after SiN_x deposition. The SF_6 etching process resulted in increased on-resistance, which indicated that the device active region was affected, most probably due to fluorine, essentially acting as a virtual gate which reduces channel 2DEG density. A further observation is that dielectric deposition followed by etching using SF_6 did not bring the semiconductor to the state it was prior to dielectric deposition.

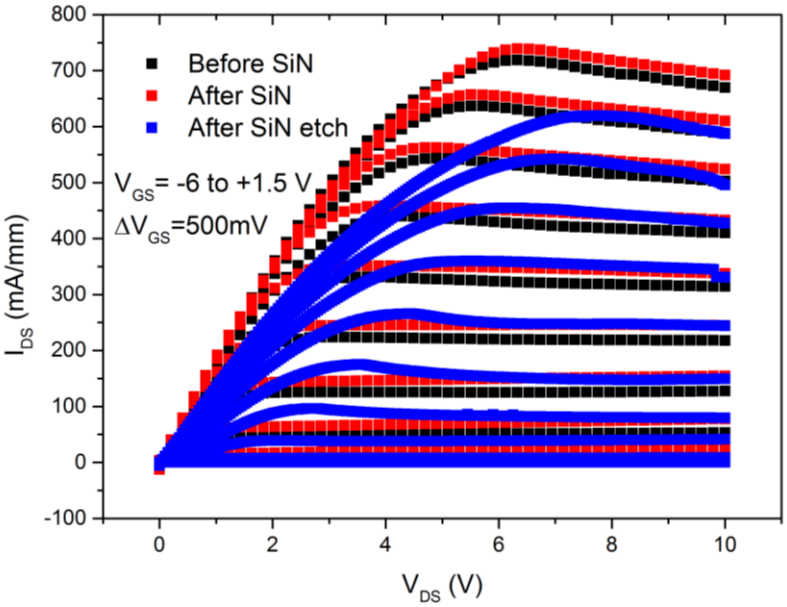


Figure 5-18: DC current-voltage characteristics of Schottky gate devices, before and after SiN_x passivation deposition and after SiN_x passivation etching.

5.7 Stress of SiN_x and Material Carrier Transport Properties

In the design of GaN transistors, there are many instances where 2DEG charge engineering may be desirable without vastly invasive procedures such as etching or material regrowth. For example, threshold voltage and off-state leakage currents can be tuned to suit the designer's needs. Dielectric films have been reported to suppress surface charge trapping effects or directly influence the surface and 2DEG charge density through their bulk charges [124], [125].

For this experiment, Van der Pauw structures were fabricated on 8 nm InAlN/AlGaN/GaN materials via conventional fabrication process methods and SiN_x passivation films were deposited at room temperature by ICP CVD on the surface. Fabrication started with a mesa etch and was followed by Ti/Al/Ni/Au contact deposition of 30/180/40/100 nm thicknesses, annealing at 770 °C for 30 s in N_2 environment.

Hall measurements were taken prior and after passivation deposition. Mechanical stress of passivation films can be modified if the ICP and RF platen powers are adjusted. Two different stress conditions were tested, where platen

power was 0 or 4 W. These conditions corresponded to ~ 280 and ~ 616 MPa compressive stress levels respectively when deposited on Si substrates, which will be referred to as “medium stress” (MS) and “high stress” (HS) in this thesis. Chamber pressure was 5 mTorr and ICP power was 200 W for both conditions.

Single deposition step and bilayer films were deposited on the Van der Pauw structure surface and Hall measurements were taken before and after each dielectric deposition step. Deposition conditions and SiN_x thicknesses used are summarised in Table 5-5. Conditions #2 to #4 were based on “medium stress” deposition. Conditions #5 and #6 were depositions of bilayer films with the “high stress” film following the deposition of the “medium stress” dielectric.

Table 5-5: Thicknesses and deposition conditions of ICP CVD SiN_x dielectrics

Condition	ICP CVD SiN_x deposition thickness (dielectric stress)
#1	non-passivated
#2	10 nm (MS)
#3	30 nm (MS)
#4	70 nm (MS)
#5	10 nm (MS) / 60 nm (HS)
#6	30 nm (MS) / 40 nm (HS)

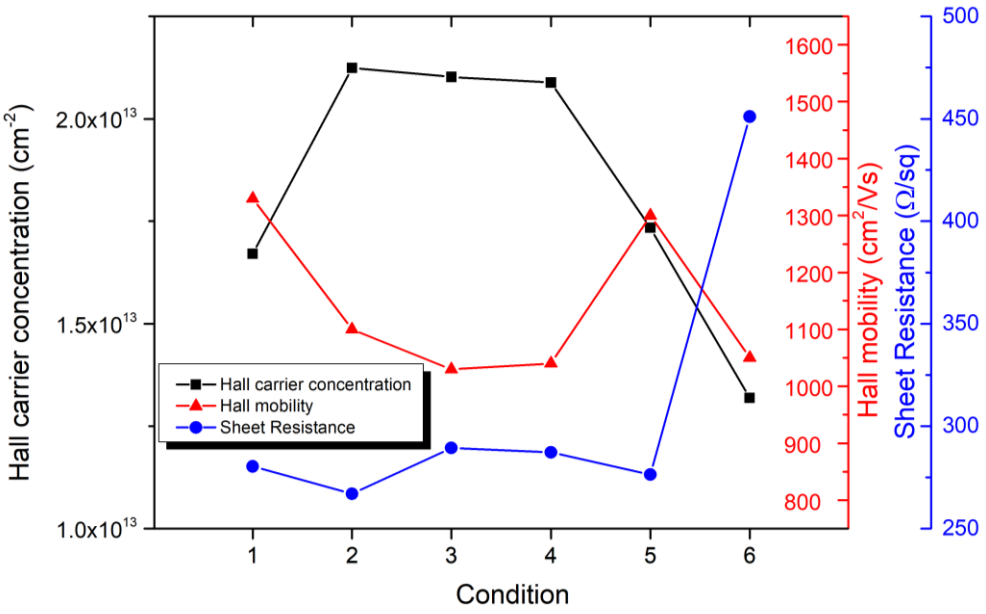


Figure 5-19: Carrier transport properties of InAlN/AlGaN/GaN materials with regards to ICP SiN_x deposition of different stresses.

In Figure 5-19, Hall measurements obtained for each deposition condition are displayed. Compared to the non-passivated sample for which ~ 1.6 x 10^{13} cm^{-2} carriers were measured, when "medium stress" SiN_x dielectrics were deposited, baseline carrier concentration increased by at least 4 x 10^{12} cm^{-2} and carrier mobility decreased. When "high stress" films were deposited to form bilayers, carrier concentration was significantly reduced, to pre-deposition levels. In the case of the 30 nm "medium stress" / 40 nm "high stress" bilayer carrier concentration was even lower than the pre-deposition measurements (~ 1.3 x 10^{13} cm^{-2}). The reduction in carrier concentration for the 30 nm "medium stress" / 40 nm "high stress" bilayer resulted in large increase in sheet resistance, from ~ 289 Ω/sq for 30 nm "medium stress" SiN_x dielectric to ~ 451 Ω/sq after 40 nm "high stress" SiN_x deposition.

This experiment demonstrated that InAlN/AlGaN/GaN material properties can be adjusted via depositing ICP CVD SiN_x bilayers of different stresses. A study on the effect of stressed SiN_x film depositions on single barrier AlGaN/GaN materials can be found in another work of our group [126]. In both material structures a significant reduction in 2DEG carrier density was observed when SiN_x passivation schemes of highly compressive stress were used. The most probable mechanism of operation is that the net negative charge effect of SiN_x films can be lowered or even reversed when a highly compressive dielectric is used. These results can

be used to engineer the off-state leakage characteristics in device structures so that they are reduced (drain-source and gates-source leakage current reduction by more than 3 orders of magnitude in AlGaN/GaN HEMT) compared to even non-passivated structures.

5.8 Conclusion

In this chapter the design, fabrication and electrical measurements of depletion mode InAlN/AlGaN/GaN-on-Si transistors were presented. The design procedures which led to the development and growth of the semiconductor materials were presented as well as the fabrication processes associated with them.

Experimental testing of material and transistor properties by varying InAlN thickness in InAlN/AlGaN/GaN-based materials during growth was performed. Substrate buffer leakage measurements for high voltage device development were obtained. The effect of applying different annealing temperatures on contact, sheet resistance and carrier transport properties were presented. The influence of drain-source distance scaling on transistor characteristics was discussed. A comparison between gate Pt and Ni based gate contacts showed significantly reduced leakage currents when Pt based contacts were used, under all bias conditions (off and on-state).

Material transport properties were vastly modified when SiN_x films of high compressive stress were deposited as the upper part of a SiN_x dielectric bilayer. The influence of SiN_x dielectrics deposited under the gate or on the active region of InAlN/AlGaN/GaN devices was assessed.

Some of the key outcomes and achievements of this work include;

- Fabrication of the first devices on a “dual barrier” InAlN/AlGaN/GaN structure grown on silicon. These devices exhibit high drain currents (I_{DS} >1 A/mm) and transconductance (g_m >200mS/mm) and nearly ideal sub-threshold swing of 65.6 mV/dec.

- The lowest contact resistance (R_c ~ 0.437 Ω mm) achieved on a dual barrier structure grown on any substrate.

- The lowest sheet resistance (R_{sh} ~ 258.4 Ω/sq) obtained on an InAlN/AlGaN/GaN dual barrier structure grown on Si.

- Fabrication and evaluation of Platinum (Pt) based gate contacts on InAlN/AlGaN/GaN dual barrier materials. The Pt based gate stack showed a greater than two orders of magnitude reduction in gate leakage compared to Ni based gate stacks.

- Parametric studies on different devices in terms of drive current, transconductance, threshold voltage, on-resistance and gate leakage current that helped observing a number of important trends.

- Material transport modification on InAlN/AlGaN/GaN materials through the use of compressively stressed SiN_x dielectrics as part of a passivation bilayer, which may effectively reduce transistor leakage currents.

Next chapter is dedicated to the development of normally-off InAlN/AlGaN/GaN-on-Si transistors.

6 Enhancement Mode InAlN/AlGaN/GaN-on-Si High Electron Mobility Transistors

The threshold voltage of heterojunction-based GaN devices is dependent on the design of the epitaxial structures, namely the choice of barrier materials, their thicknesses and alloy composition. Modifications to the intrinsic threshold voltage of the material can be implemented through a variety of methods during device fabrication. Tot douhe “gate recess” method relies on the reduction of the barrier thickness under the gate, which results in lower polarisation induced 2DEG density. A deep-enough recess and the use of gate metal of high work function can lead to a threshold voltage of positive value and the formation of a normally off, enhancement mode HEMT. In this chapter, process modules that led to the fabrication of normally-off devices will be presented. The influence of dielectric deposition on normally-off AlGaN/GaN materials and on recess etched InAlN/AlGaN/GaN materials will be summarized with regards to their suitability for HEMT fabrication.

6.1 Normally-off GaN HEMT via Dry Etch Gate Recess

The first approach for fabricating normally-off devices on the dual barrier wafers was via a technique that involves $SiCl_4$ RIE etching in the gate area. The fabrication process started with a ~600 nm mesa etch, patterned via standard photolithography and performed by RIE $SiCl_4$ chemistry. Following this, Ti/Al/Ni/Au metal films of 20/180/40/100 nm thicknesses were deposited using lift-off technique and subsequently annealed at 770 °C for 30s in N_2 atmosphere to form the ohmic contacts. Contact resistance R_c ~0.84 Ω mm and two-dimensional electron gas channel sheet resistance R_{sh} ~391 Ω/sq measurements were determined using the TLM method described in Section 3.6.1. At this point, two samples were taken forward. Sample A had 20/200 nm Pt/Au Schottky gate contacts defined using photolithography and lift-off techniques. The gate region of Sample B was locally recessed using $SiCl_4$ RIE prior to implementing an identical gate metal process as for sample A. Etch depth and profile of $SiCl_4$ etching conditions were optimised using reflectometry and AFM measurements before being applied to Sample B. Plasma exposure for 70 seconds at 100 W RF power and 50 mTorr pressure was used to remove ~10 nm of substrate material, which approximately the sum of the 8 nm InAlN and 2 nm GaN capping layer

thicknesses. A schematic cross section of the locally recessed device structure (Sample B) along with an SEM image of the device and an AFM measurement of the local recess are depicted in Figure 6-1.

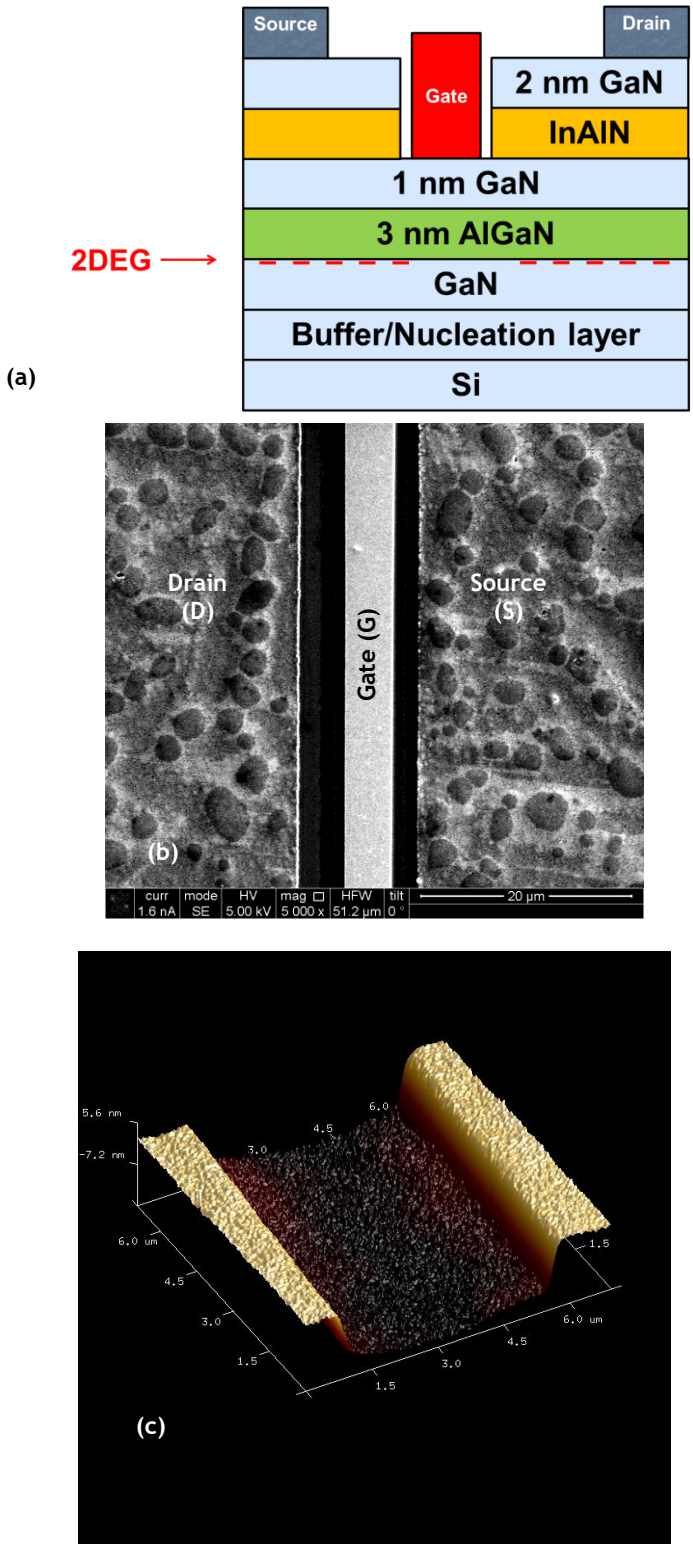


Figure 6-1: (a) Schematic cross section of the InAlN/AlGaN/GaN-based HEMT structure. (b) Top-view SEM image of proposed HEMT. (c) Atomic-force-microscope image of the gate recessed area.

Transfer Length Method measurements were taken from linear TLM structures. Contact resistance R_c ~ 0.84 Ωmm and 2DEG channel sheet resistance R_{sh} ~ 391 Ω/sq were extracted. Hall measurements were taken from Van der Pauw structures. Hall mobility μ_H ~ 1100 to 1300 $cm^2\ V^{-1}\ s^{-1}$ and 2DEG electron concentration n_H ~ 1.55 to 1.6 $*10^{13}\ cm^{-2}$ were obtained.

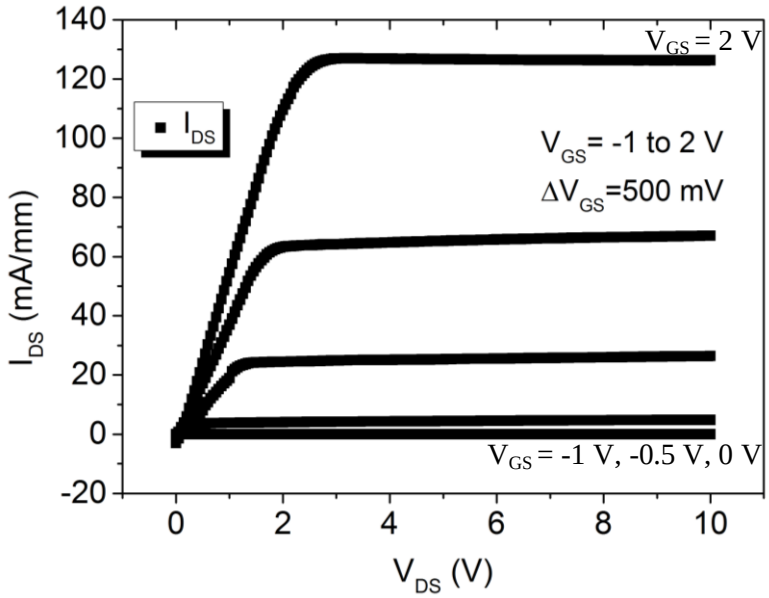


Figure 6-2: I –V characteristics of e-mode InAlN/AlGaN/GaN HEMT using $SiCl_4$ RIE gate etch process.

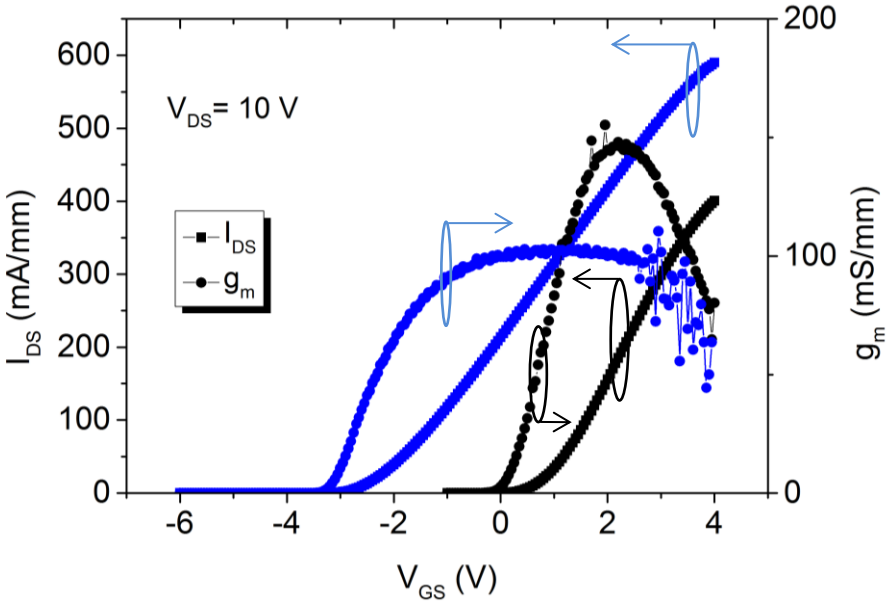


Figure 6-3: Comparison of transfer characteristics between d-mode (in blue) and e-mode (in black) devices at V_{DS} = 10 V.

The current-voltage DC output characteristic of a device from Sample B is illustrated in Figure 6-2. A comparison between the transfer characteristics of devices from samples A and B are shown in Figure 6-3.

As observed from the transfer characteristics plot, one effect of $SiCl_4$ dry etch under the gate area was a shift of threshold voltage towards the positive direction. A threshold voltage of ~ +0.5 V was obtained for devices from Sample B, indicating a change from a normally-on to normally-off device as a result of the gate recess etch. Compared to the depletion mode device, maximum drain currents of the enhancement mode device were reduced from ~ 600 to ~ 400 mA/mm, due to two potential reasons. First, the presence of only a thin barrier layer under the gate reduced the maximum current handling capabilities of the e-mode device structures, which have undergone the dry etch plasma process. Secondly, due to the Schottky gate structure of the devices, the channel may not have been fully populated with 2DEG electrons for a gate-source voltage that does not cause significant Schottky gate forward bias leakage current.

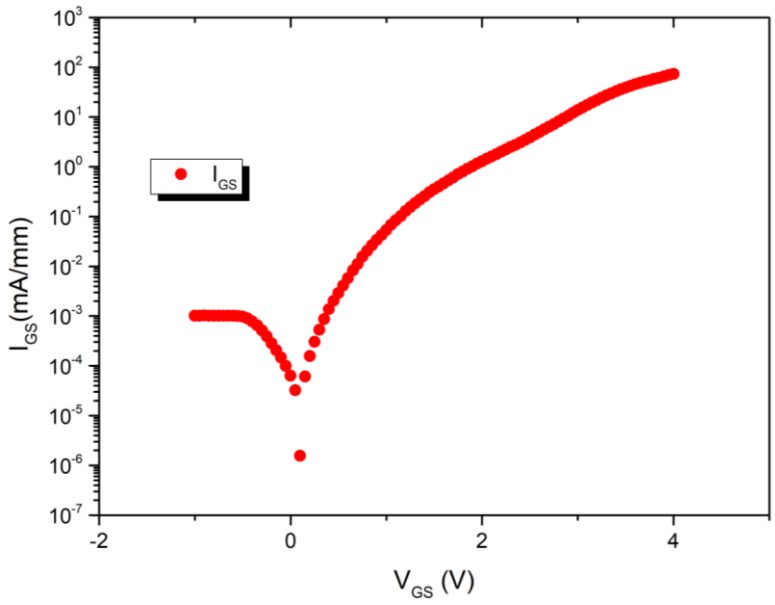


Figure 6-4: Recess etched Schottky gate leakage current.

Gate dielectrics can help reduce the forward gate bias leakage and their incorporation in enhancement mode HEMT can be found in Section 6.2.3. Compared to enhancement mode devices fabricated on 3 nm AlGaN/GaN-based wafers, the active regions of recessed gate InAlN/3 nm AlGaN/GaN materials are less resistive due to higher 2DEG densities induced by InAlN. In terms of

transistor performance, incorporation of InAlN/3 nm AlGaN/GaN materials results in higher drain-source maximum drive current densities and lower on-resistances as theoretically predicted and also measured in the previous chapter.

As discussed in Chapter 2, HEMT transconductance is dependent on the barrier layer thickness, with thinner barrier layer resulting in higher transconductance values. This is reflected on the maximum extrinsic transconductance of the enhancement mode device which was ~50% higher than the obtained value for the depletion mode HEMT.

As HEMT transconductance is;

$$g_m = \frac{\mu C_{GS} W_G}{L_G}(V_{GS} - V_{th}) \tag{6-1}$$

The ratio of the peak transconductances for the enhancement mode and the depletion mode device will be;

$$\frac{g_{\max(e)}}{g_{\max(d)}} = \frac{\mu_{(e)} C_{GS(e)}}{\mu_{(d)} C_{GS(d)}} \frac{(V_{GS1} - V_{th(e)})}{(V_{GS2} - V_{th(d)})} \tag{6-2}$$

Rearranging and substituting voltage values and the transconductance ratio from the I-V characteristics;

$$\frac{\mu_{(e)}}{\mu_{(d)}} = 4.05 \frac{C_{GS(d)}}{C_{GS(e)}} \tag{6-3}$$

The gate-source capacitance is;

$$C_{GS} = \frac{\varepsilon_0 \varepsilon_{Barrier} W_G L_G}{t_{Barrier}} \tag{6-4}$$

As the InAlN, AlGaN, and GaN permitivities are quite close in value [127], Eq. (6-3) can be simplified as;

$$\frac{\mu_{(e)}}{\mu_{(d)}} = 4.05 \frac{t_{barrier(e)}}{t_{barrier(d)}} \quad (6\text{-}5)$$

Assuming no 2DEG conduction on the GaN layer between the InAlN and AlGaN barriers for the depletion mode device and substituting the material thicknesses, the electron mobility ratio becomes $\mu_{(e)} \sim 1.17\mu_{(d)}$. If there is 2DEG conduction on the GaN layer between the InAlN and AlGaN barriers for the depletion mode device, the electron mobility ratio becomes $\mu_{(e)} \sim 1.5\mu_{(d)}$. Both results confirm that there is a high mobility channel present for the enhancement mode device. Overall, there is a trade-off between maximum drain current and peak transconductance in recess etch HEMT technologies, as both metrics depend on the barrier thickness under the gate.

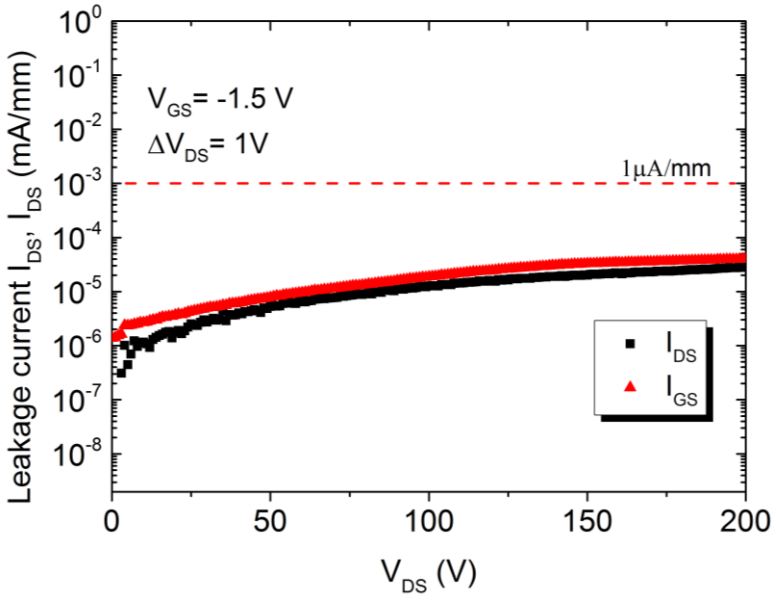


Figure 6-5: Off-state leakage current characteristics of recessed gate HEMT.

The off-state drain-source leakage characteristics of the Sample B are illustrated in Figure 6-5. Low leakage (< 5 x10^{-5} mA/mm) currents were observed for up to 200 V of applied drain-source voltage and indicate a high drain-source blocking voltage, suitable for >200 V switching applications.

As demonstrated, a $SiCl_4$ RIE process can provide the means for the development of a gate recess etch, hence enabling enhancement mode operation on InAlN/AlGaN/GaN materials. An alternative etch technique will be presented in the next section. Dry etch-based processes possess insignificant etch selectivity

on materials of the III-nitride system and, as a result, extremely accurate etch conditions need to be established prior to its application for precise processing. Otherwise, reproducibility of results in terms of threshold voltage may vary from an etch run to another. The alternative technique used to improve e-mode device fabrication is based on ethylenediamine solution wet etching and a description of its development stages will follow.

6.2 Normally-off GaN HEMT via Selective Wet Etching

As previously discussed, in order to fabricate an enhancement mode transistor using the InAlN/3nm AlGaN/GaN structure as a substrate, the InAlN layer needs to be accurately removed under the gate, due to its high spontaneous polarisation induced channel carrier density. There is no low damage selective dry etch process to implement this in the literature, though Rizzi et al [128] have demonstrated a wet etch process for etching 70 nm InAlN layers using $C_2H_4(NH_2)_2$ (ethylenediamine or 1,2- diaminoethane) as a wet etchant. They found that the etching process was nominally vertical, with lateral etching also being present through recessing the sidewalls of InAlN surface pits in InAlN/GaN crystals. These pits are mainly caused by threading dislocations in the layers below and will extend to InAlN. The applications targeted were MEMS and photonic device structures.

The ethylenediamine compound is an organic alkaline etchant with has a pH of ~ 12.3 in 1M solutions. Compared to other wet etchants, such as potassium hydroxide (KOH), the lower pH of ethylenediamine resulted in a slower etching of InAlN, with less roughening of the underlying GaN surfaces.

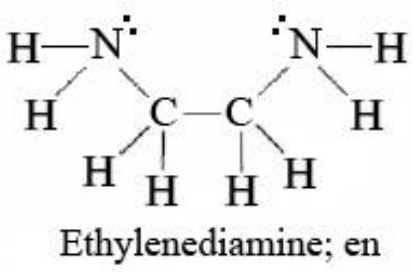


Figure 6-6: Ethylenediamine molecular diagram [129].

Ethylenediamine is a bidentate ligand, i.e. has two donor atoms which can bind to a metal atom or ion at two points (Figure 6-6). The nitrogen atoms in the

ethylenediamine molecule possess two free electrons each, allowing them to form two bonds with metal ions. A stable complex can then be formed and this property can be used to occupy and stabilise In^{3+} ions around the two adjacent co-ordination sites, thereby solubilising the indium component in InAlN [130].

Reference [130] reports the removal of 70 nm and 130 nm thick InAlN layers using ethylenediamine. The process etch rate is approximately ~6 nm/hr, however for very thin InAlN layers the etch rate is reduced. The optimal InAlN thicknesses for transistor operation are much smaller (< 10 nm) to ensure appropriate values of threshold voltage [131]. The next section will describe ethylenediamine wet etching experiments performed on GaN and thin InAlN/GaN layers.

6.2.1 Ethylenediamine Wet Etching Experiments

Experiments were carried out to examine whether there is an etching effect of 1M ethylenediamine (of at least reagent grade purity, diluted in reverse osmosis (RO) water) on GaN and InAlN. Photoresist (S1818) was patterned on the surface in order to be used as an etch mask and the samples were subsequently placed in a screw-top jar containing the solution. The container has a tight-sealing lid, a perforated sample platform was situated inside it to allow a magnetic stirrer bar to rotate underneath samples. The samples were exposed to ethylenediamine for times in the range of 2h to 48h and the magnetic stirrer was used for the experiment duration.

After ethylenediamine was applied for set time periods, the photoresist was removed. Even after a 48h etchant application there was no etching effect or surface roughening detected on the GaN surface, by the use of AFM (Figure 6-7b).

Following this, the effect of ethylenediamine on 8nm InAlN layers needed to be determined. In order to implement this, the GaN capping layer of the samples needed to be locally removed. Low power $SiCl_4$ plasma dry etch processing were applied for 30, 32, 35 and 40 seconds at 100 W RF power and 50 mTorr pressure.

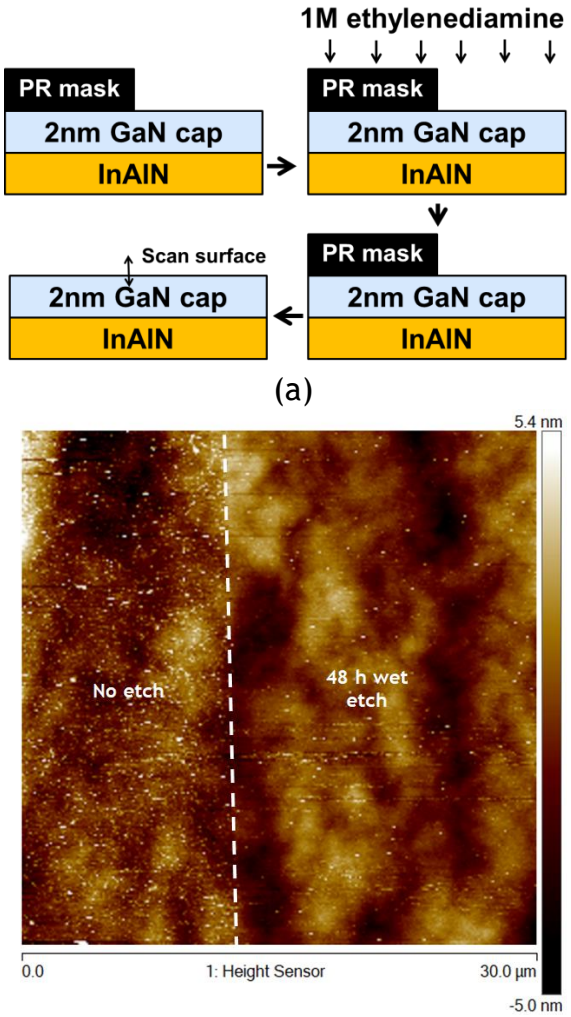


Figure 6-7: (a) Experiment to check the effect of 1M ethylenediamine on GaN-capping layer. (top left) Mask patterning on surface, (top right) application of solution on sample, (bottom right) sample removed from solution, (bottom left) photoresist cleaning and subsequently surface scanning for GaN removal or GaN surface roughening. (b) AFM scan after 48 hours wet etch.

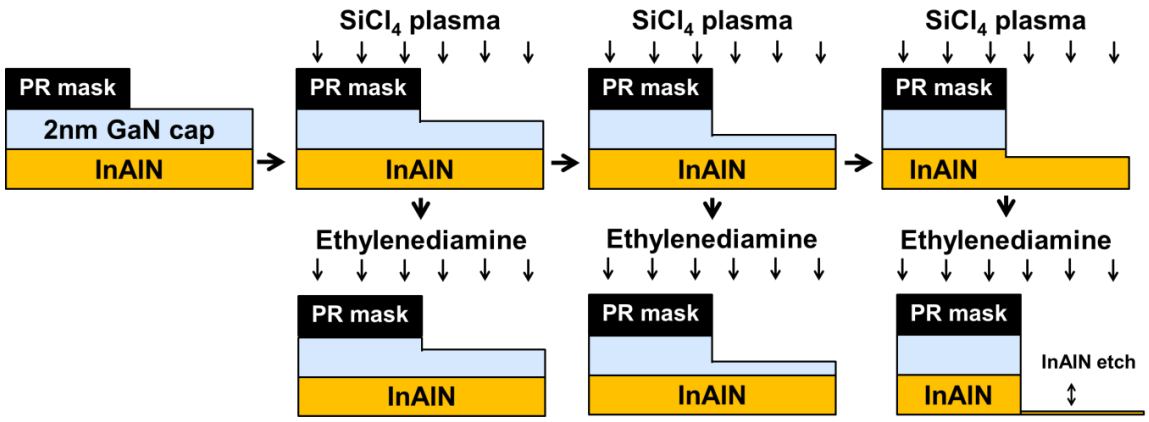


Figure 6-8: Dry etching optimisation process for removing GaN capping layer.

To test the etching of the GaN capping layer, each of the dry etched samples was immediately transferred to the ethylenediamine etchant solution. By knowing that the GaN surface had not been modified by the wet etchant, exposure to dry etch plasma for a time period longer than that required to remove the GaN capping layer would result in a surface that can been modified by the wet etchant (Figure 6-8). Samples that had been through etch processes of shorter time periods than the duration required for GaN capping layer complete removal would not show any surface modification after wet etching. After the completion of the etch trials, a $SiCl_4$ based plasma etch for 35 s was measured to have completely removed the 2 nm GaN capping layer (Figure 6-9). A root mean square etched surface roughness R_q < 0.5 nm was measured.

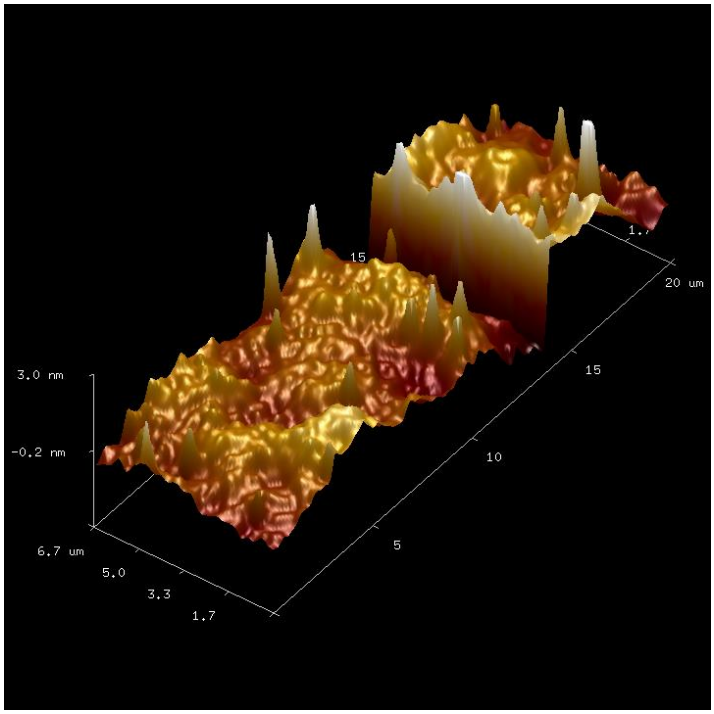


Figure 6-9: AFM scan of GaN capping layer etching. The etched area is in bottom left.

Following dry etching of the GaN capping layer, a new photoresist patterning as an etch mask within the dry etched area was performed (Figure 6-10).

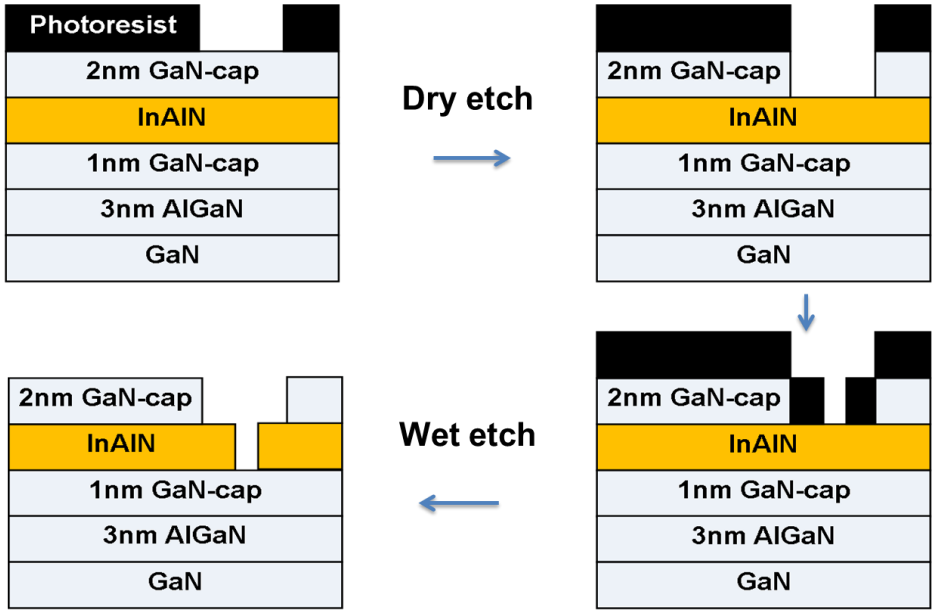


Figure 6-10: Etch process - (Top left) Photoresist patterning as dry etch mask, (Top right) SiCl4 based dry etching to remove GaN cap, (Bottom right) Photoresist patterning as wet etch photo-mask, (Bottom left) Ethylenediamine wet etching and etch mask removal.

After resist patterning, samples were then placed in the ethylenediamine solution for different time periods (20 minutes to 66 hours) after which the resist was removed to measure etch depths. It was found that significant InAlN removal begins after a 40 min etching. As previously mentioned, because the etching method is selective and self-limited, no etching should occur on the GaN layer below InAlN. Only InAlN is removed by this process. AFM measurement scans for a 120 minute etch can be found in Figure 6-11. In the figure, the results of the two-step process resulting from the dry etch and the wet etch processes can be seen. The AFM results following the etch processes are shown in Table 6-1.

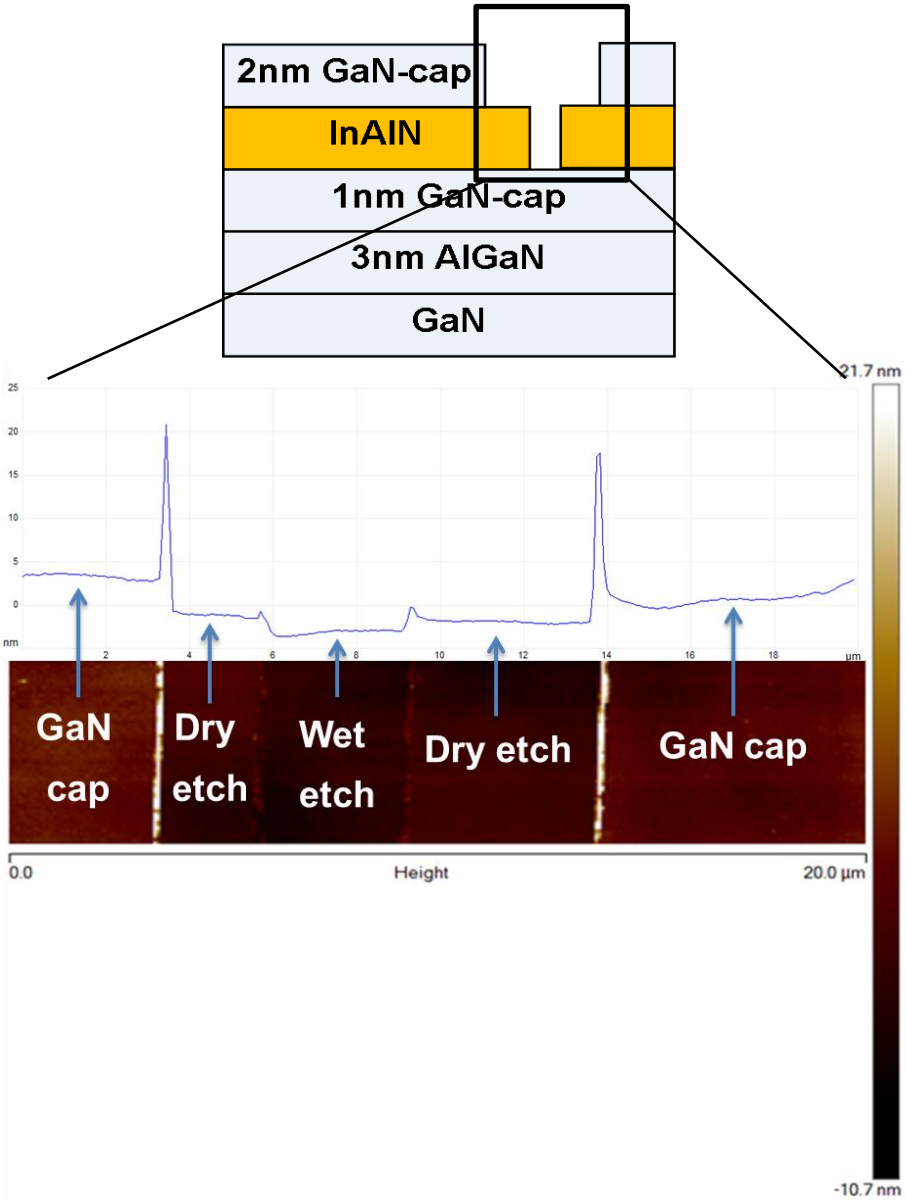


Figure 6-11: AFM scan and measurements of etch profiles (100 W, 35 s $SiCl_4$ dry etching followed by 120 minutes 1 M ethylenediamine wet etching).

Table 6-1: AFM roughness over a 2 µm x 2 µm etched area.

	RMS surface roughness R_q (nm)	
	2h wet etch	**66h wet etch**
Dry etched area	0.568	0.719
Dry etched + Wet etched area	0.594	1.04

6.2.2 Influence of Wet Etching on Current-Voltage Measurements

Next step in developing the wet etch process was to correlate etch depths and electrical parameter changes. Electrical measurements were performed before and after etching to measure whether the wet etchant can significantly reduce currents flowing through the etched semiconductor. For this experiment, Ni/Au metal contacts were deposited 18 μm apart and were isolated from neighbouring structures via a ~ 630 nm mesa etch. The contact pads were protected by photoresist during etching. The test structure used along with DC current-voltage measurements taken prior to and after etching are depicted in Figure 6-12.

As extracted from the measurements, a current reduction of five orders of magnitude was observed after the application of the ethylenediamine-based etchant for 2 hours and a seven order reduction after 66 hours of wet etching. The results show that the application of ethylenediamine can practically limit current leakage to levels suitable for enhancement mode operation in ungated structures. This is a strong basis for realising normally-off devices, by gating the InAlN-etched area of the dual barrier structure, as will be discussed in the next section. An SEM image of the sample which was wet etched for 66 hours, depicting each region of the test structure is found in Figure 6-13.

In the next section, the application of the ethylenediamine wet etching technique for fabrication of enhancement mode devices on InAlN/AlGaN/GaN-on-Si materials will be presented, along with electrical characterisation results extracted from these devices.

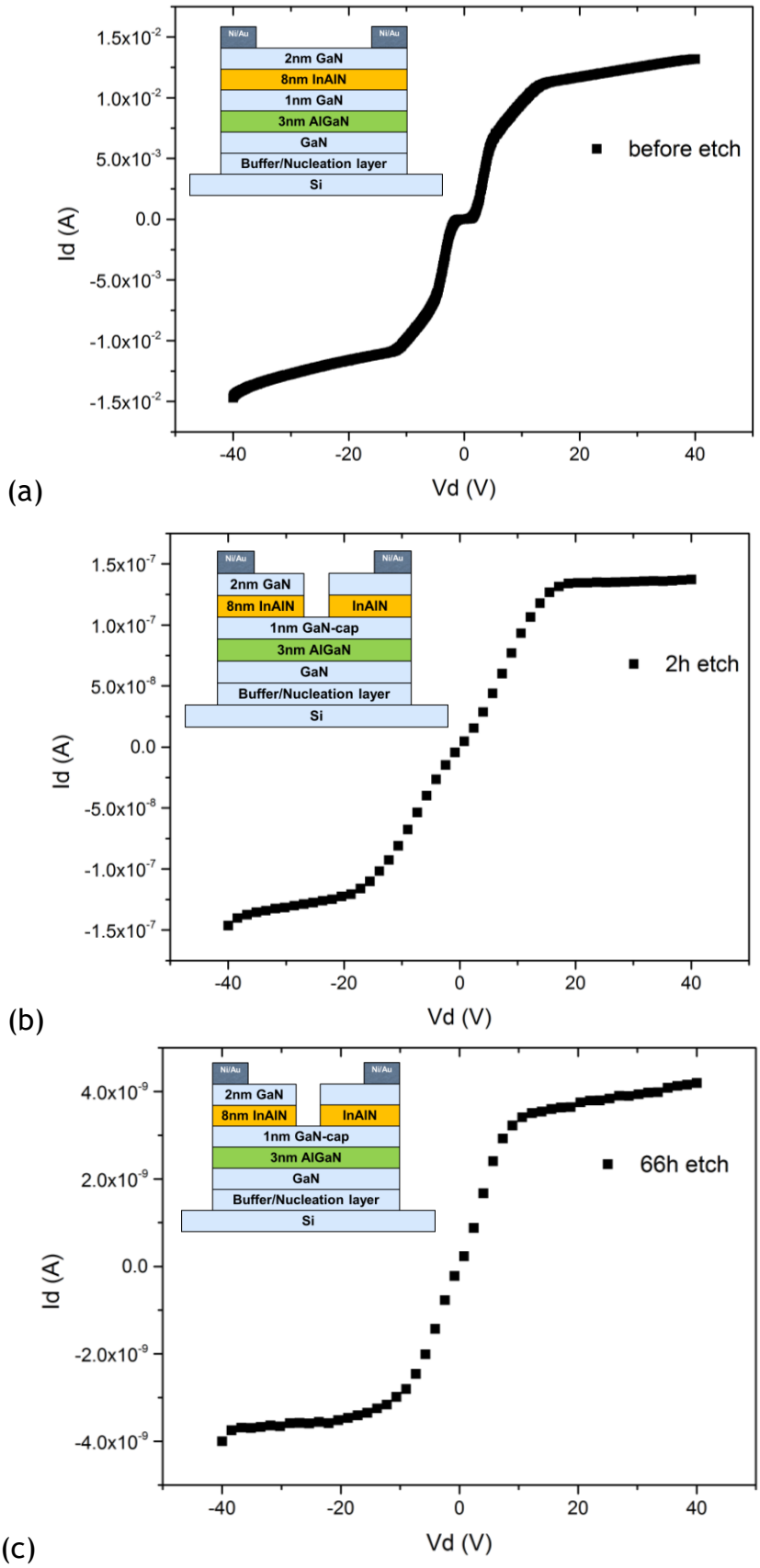


Figure 6-12: Leakage current measured (a) before etching, (b) after GaN cap removal and ethylenediamine wet etch for 2h, (c) after GaN cap removal and ethylenediamine etch for 66h. The separation between the contacts is 18 µm and the contact dimensions are 42 µm (length) 192 µm (width).

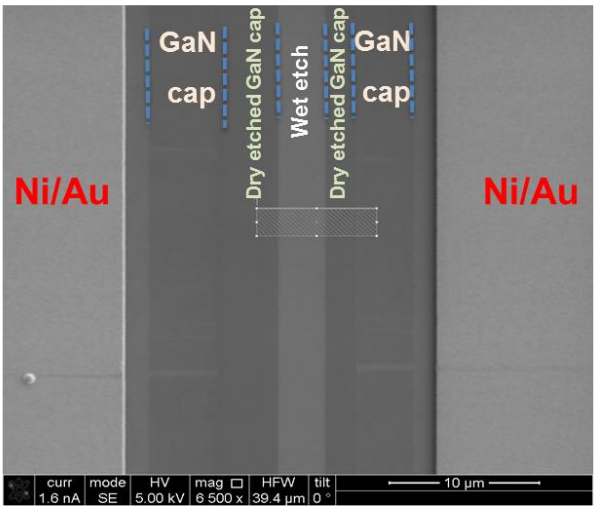


Figure 6-13: SEM scan showing contacts, etched profiles and corresponding semiconductor layers (66 hour wet etching).

6.2.3 Fabrication of e-mode GaN HEMT via Selective Wet Etching

Stemming from the ethylenediamine wet etching experimentation on the InAlN containing wafers, device fabrication via ethylenediamine gate recess as a process module was initiated. For the fabrication of these devices, Ti/Al/Ni/Au ohmic contacts of 30/180/40/100 nm thicknesses were first deposited. These were then annealed at 770 °C for 30 seconds in N_2 environment. The devices were then mesa isolated to a depth of 600 nm using a $SiCl_4$ plasma etch. A low power $SiCl_4$ dry etch technique was locally applied to remove the GaN capping layer in the gate region of the devices of the sample.

Following this, the sample was immediately transferred to a beaker containing a 1M ethylenediamine solution and a similar procedure to that described in Section 6.2.1 was performed. Etching duration was 6.5 hours, which was expected to recess etch InAlN based on the experiments described above. Photoresist was then removed prior to any further processing.

The sample was sent to the Functional Materials group at the University of Liverpool for Al_2O_3 gate dielectric deposition and post dielectric annealing. Prior to dielectric deposition, the sample was cleaned using acetone and IPA. Following this, N_2 plasma pre-treatment at 150 W for 5 minutes was performed. A NH_4F:H_2O solution replaced the H_2O precursor used for undoped dielectric deposition. Each deposition cycle consisted of: 0.03 s TMA - 4 s 100 sccm Ar

purge - 0.02 s NH_4F:H_2O - 4 s 100 sccm Ar purge. 59 growth cycles were run and the average growth rate was 0.85Å/cycle. A film thickness of 5.35 nm was extracted via spectroscopic ellipsometry. Development and optimisation of the in situ fluorine doped dielectric conditions was previously developed amongst Glasgow, Liverpool and Sheffield university project partners, with results reported in [132] and [133].

Upon return of the ALD passivated samples, 70 nm ICP SiN_x was deposited on the sample for additional surface passivation and to place the gate field plate at an appropriate distance from the semiconductor surface. This also protected the Al_2O_3 in the gate region from etching in TMAH developer when the gate foot was defined.

The gate metal formation comprised photolithography to define the gate feature, which was then transferred into the SiN layer by a 5 minute low power, low damage SF_6 plasma etching with conditions of 50 W RF power, chamber pressure of 50 mTorr and 50 sccm SF_6 gas flow. Following the SF_6 etching, a Pt/Au metal stack of 20/200 nm thicknesses was deposited, similar to that described in Section 3.2. The formation of gate contacts was followed by the local application of SF_6 plasma over the ohmic contacts to open vias, so that access to the device contacts can be achieved through probing tips. A layer diagram of the HEMT structure is shown in Figure 6-14. Gate recess was applied on a 3 µm length x 100 µm gate width area and the gate field plate was extended 3 µm on the drain side of the gate. The gate-to-source spacing was 3 µm and the gate field plate-to-drain distance was 20 µm.

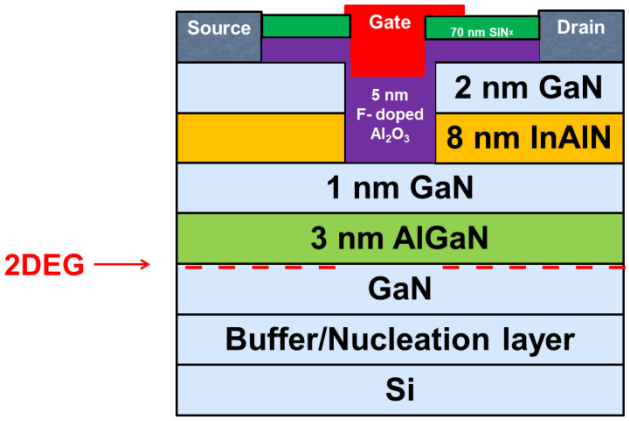


Figure 6-14: Enhancement mode InAlN/AlGaN/GaN HEMT emloying an ethylenediamine gate etch process and fluorine doped Al_2O_3 gate dielectric.

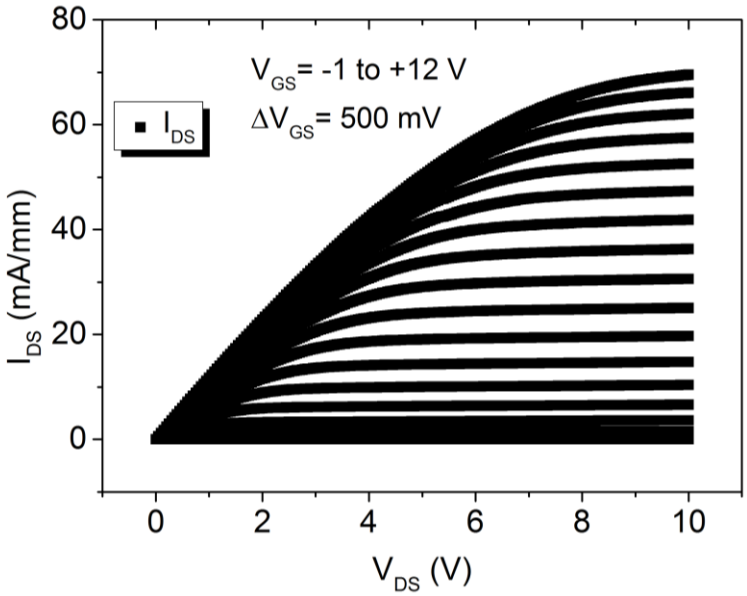


Figure 6-15: I –V characteristics of e-mode InAlN/AlGaN/GaN HEMT via ethylenediamine gate recess and fluorine doped Al_2O_3 gate dielectric.

The current-voltage output characteristics of a device can be found in Figure 6-15, which demonstrates a threshold voltage of ~ +4.5 V. The demonstration of a normally off GaN platform that allows a selective and self-limited etch technique to be applied is very promising for fail-safe device development. Low values of maximum saturation current I_{DS} ~ 72 mA/mm and peak extrinsic transconductance g_{max} ~ 13.8 mS/mm were exhibited. Fluorine atoms on the semiconductor surface provide a positive shift in threshold voltage but may have also deteriorated the low resistance characteristics of the access region as they are situated onto the non-etched semiconductor region surface.

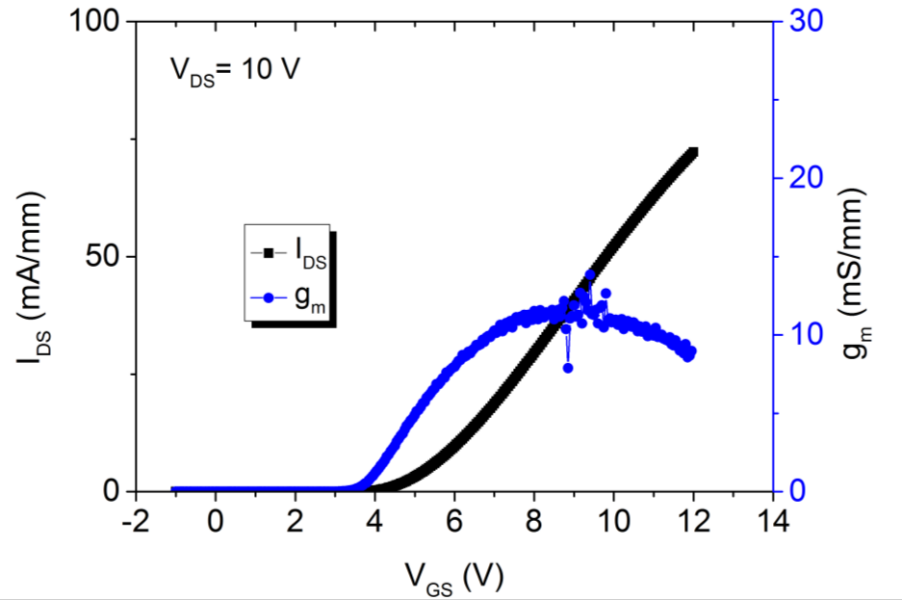


Figure 6-16: Transfer characteristics of e-mode InAlN/AlGaN/GaN HEMT with wet etch gate recess and fluorine doped Al_2O_3 gate dielectric.

6.2.4 Ethylenediamine Experiments on Commercial Materials

Ethylenediamine wet etching experiments were repeated for commercially sourced custom layer designed materials by NTT grown on 1 mm thick Si wafers. From the top, the epitaxial layers consisted of a 2 nm GaN capping layer, an 8 nm InAlN layer, a 1 nm GaN layer, a 3 nm AlGaN layer, a 1 µm GaN channel, and transition/buffer layers.

Electrical measurements were taken between ohmic contact pads separated by fixed etched distance (Figure 6-17). The fabrication process started with 600 nm deep mesa etching, Ti/Al/Ni/Au contact deposition of 30/180/40/100 nm thicknesses deposition which were subsequently annealed for 30 s at 770 °C in N_2 environment. Following this, a 70 nm SiN_x dielectric was deposited by ICP CVD. The SiN_x dielecteric was first etched locally between the pads via SF_6 chemistry and then the GaN capping layer was removed via $SiCl_4$ plasma. The etching conditions were adjusted for the substrates involved and were based on 2M ethylenediamine solution etching for up to 260 hours. Electrical measurements were taken prior to the GaN capping layer etch and after etching has occurred.

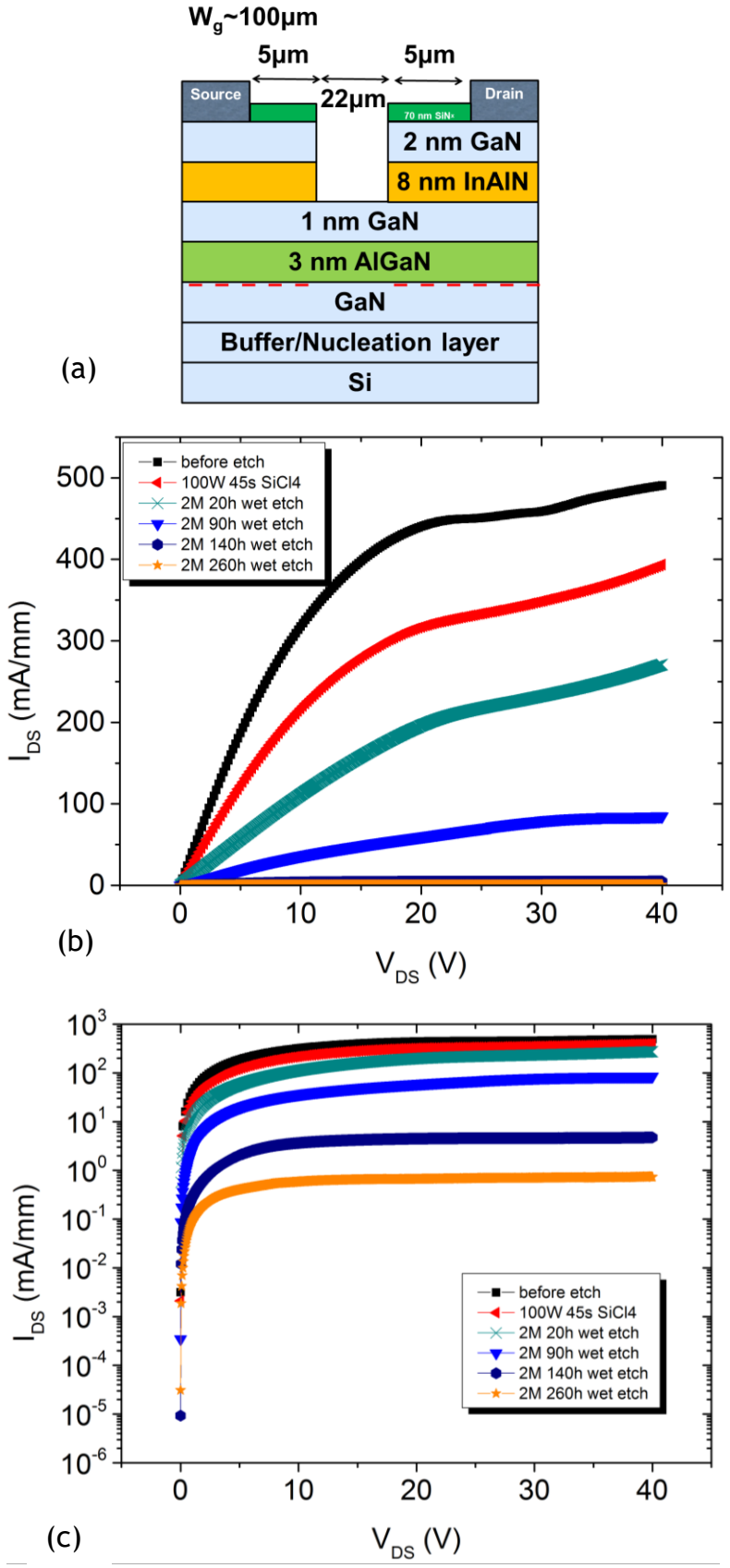


Figure 6-17: (a) Structure for testing ethylenediamine wet etching on NTT InAlN/AlGaN/GaN materials. Leakage currents measured prior to etching and for varying etching steps (b) in linear scale (c) in semi-logarithmic scale.

The etching properties of the ethylenediamine compound were demonstrated with a reduction in semiconductor current leakage levels with applied voltage. In this instance though, the leakage current levels saturated to levels unsuited for enhancement mode device fabrication. Upon further investigation, very high Schottky contact leakage was observed for devices fabricated on these materials and this may have indicated a strong top barrier layer leakage component. It may be also possible that the AlGaN/GaN heterojunction formed below the InAlN layer induces a large 2DEG electron concentration, due to thickness or compositional variations in the AlGaN layer, which cause high leakage currents.

6.3 Dielectrics on Etched Barrier Layer

An experiment that supported the use of fluorine doped dielectric films was based on the fabrication of devices that incorporated $SiCl_4$ plasma etching of the barrier layer in the gate area and the use of SiN_x dielectrics of different thicknesses under the gate metal. The material structure and the fabricated device are depicted in Figure 6-18.

The fabrication process began with a Ti/Al/Ni/Au metal stack deposition of 30/180/40/180 nm thicknesses, which was thermally annealed for 30 seconds at 770 °C in N_2 environment to form ohmic contacts. The samples were subsequently isolated by a $SiCl_4$ plasma based mesa etch process. Photoresist was then patterned in the gate area and a $SiCl_4$ RIE process was used to remove the GaN capping layer and the InAlN layer, similarly to that described in Section 6.1. Immediately after the etch was completed and with the photoresist still present, each sample was transferred to an Oxford Instruments ICP180 tool for ICP CVD SiN_x dielectric deposition of 5, 10 and 20 nm thicknesses. The samples were then transferred to a Plassys MEB 400S e-beam evaporator tool where Pt/Au gate contacts were deposited. The lift-off process that followed led to the formation of the device structure depicted in Figure 6-18.

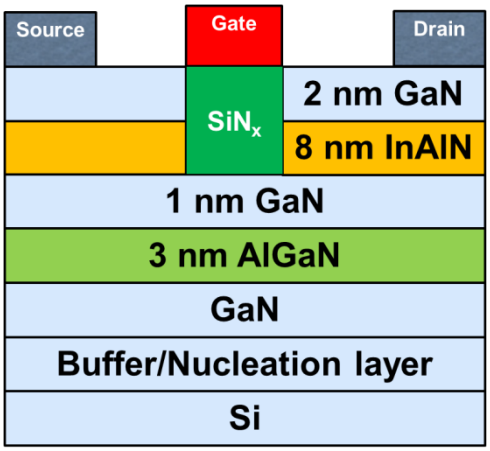


Figure 6-18: Recessed gate InAlN/AlGaN/GaN HEMT structure with ICP CVD SiN_x gate dielectric.

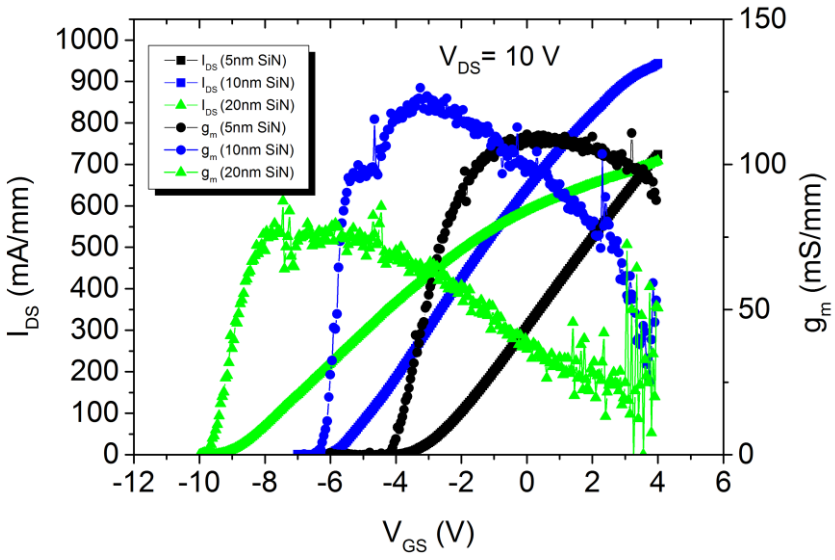


Figure 6-19: Transfer characteristics of InAlN barrier recess etched InAlN/AlGaN/GaN transistors incorporating ICP CVD SiN_x gate dielectrics of different thicknesses.

The device structures were then electrically tested (Figure 6-19). Threshold voltages obtained from devices taken from each sample are summarised in Table 6-2. As shown, threshold voltages were shifted more negatively as the SiN_x thickness increased. For the transistor incorporating 5 nm SiN_x gate dielectric threshold voltage was ~ -3.95 V. By increasing SiN_x thickness, threshold voltage was shifted to ~ -6.2 V for 10 nm SiN_x and ~ -9.5 V for 20 nm SiN_x.

Table 6-2: Threshold voltage vs ICP CVD SiN_x gate dielectric thickness for recessed etch MIS-HEMT. Device dimensions were W_G = 100 µm, L_G = 3 µm, L_{GD} = 4 µm L_{GS} = 3 µm.

Wafer	$SiCl_4$ barrier etch conditions - SiN_x gate dielectric thickness (nm)	Threshold voltage V_{th} (V)
8nm InAlN /3nm AlGaN/GaN	100 W 45 s No dielectric	+0.5
	100 W 45 s 5 nm SiN_x	-3.95
	100 W 45 s 10 nm SiN_x	-6.2
	100 W 45 s 20 nm SiN_x	-9.5

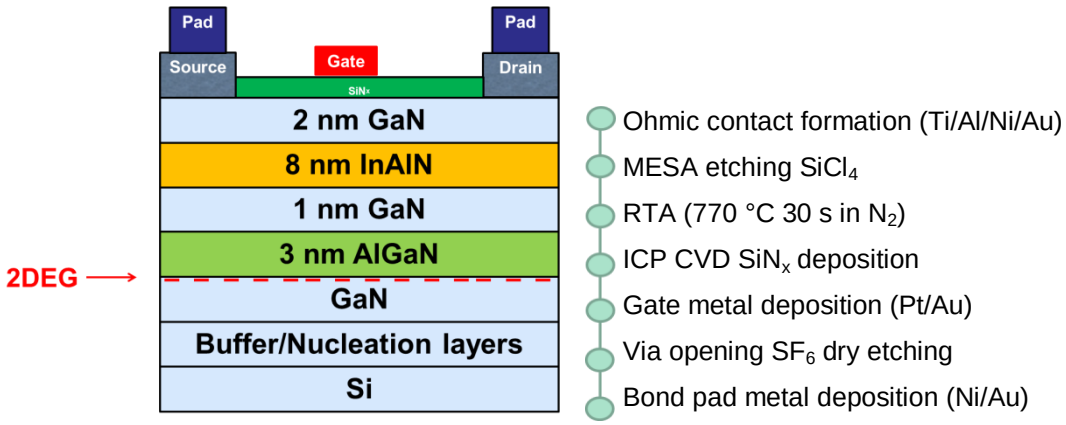
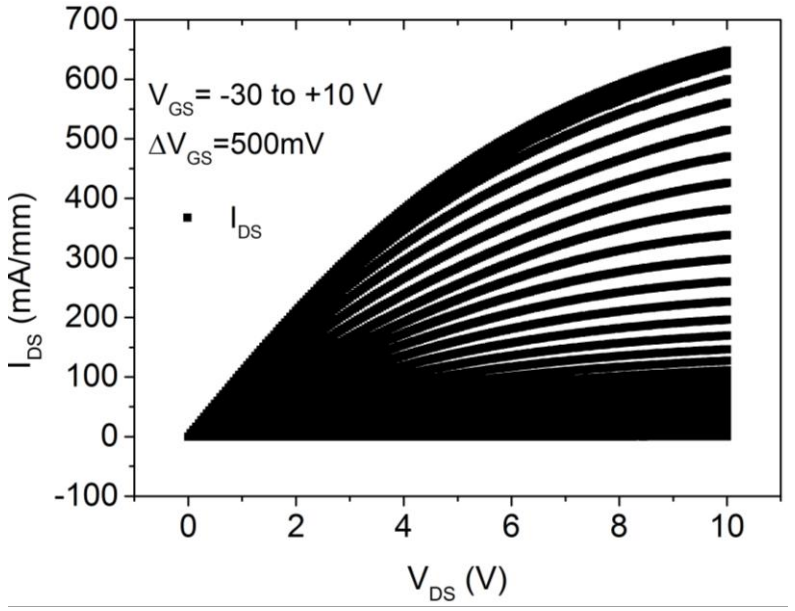
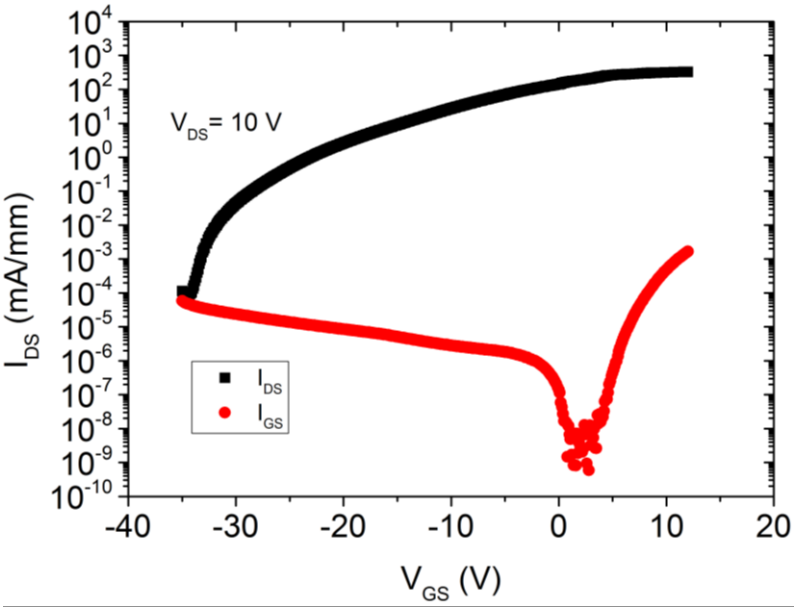


Figure 6-20: Layer structure of device incorporating SiN_x as gate dielectric and associated fabrication process.

Previously, a negative shift in threshold voltage was also observed for samples fabricated with SiN_x dielectric process, but which had not previously undergone a barrier layer etching process e.g. the device depicted in Figure 6-20 which incorporated a 70 nm SiN_x gate dielectric deposited by ICP CVD. The physical dimensions of the gate on the transistor active area were 100 µm gate width and 3 µm gate length. The transistor gate-to-source distance was 3 µm and the gate-to-drain separation was 12 µm. Potential reasons for using thick dielectric films for power device development include improved gate related breakdown voltages and low gate leakage currents between transistor gate and drain, gate-source and drain-source. A depiction of the negative shift in threshold voltage in this device is found in the figure below.



(a)



(b)

Figure 6-21: (a) DC output and (b) transfer characteristics in semi-logarithmic scale of InAlN/AlGaN/GaN HEMT employing a 70 nm SiN_x dielectric.

Elsewhere in the wider PowerGaN project, some encouraging results had been obtained with Al_2O_3 films used as gate dielectrics [134]. These experiments led to the incorporation of fluorine doped Al_2O_3 dielectrics for GaN HEMT as means for obtaining a positive threshold voltage.

6.4 Conclusion

In this chapter, demonstration of normally-off InAlN/AlGaN/GaN-on-Si based HEMT was presented. Process modules involving SiCl4 RIE dry etching resulted in normally-off devices (V_{TH} ~ +0.5 V) exhibiting maximum drive current densities I_{DS} > 600 mA/mm. Compared to depletion mode devices of the same wafers (V_{TH} ~ -3.4 V), these enhancement mode devices have shown a ~50% increase in extrinsic transconductance which is attributed to an increase in channel electron mobility due to the decrease of the separation of the channel from the gate contact and the subsequent increased gate control.

Also, an etching process for selectively removing InAlN on GaN was developed for HEMT device fabrication. This self-limiting process can lead to improved repeatability in the control of threshold voltage with no plasma induced etch damage. Devices fabricated via ethylendiamine solution wet etching and fluorine doped Al_2O_3 gate dielectrics exhibited threshold voltage V_{TH} ~ +4.5 V, which is very desirable for fail-safe normally-off operation.

The threshold voltage of recess etched MIS-HEMT which were fabricated using ICP CVD deposited SiN_x gate dielectrics were shifted towards the negative direction for increasing dielectric thickness. For a 20 nm SiN_x dielectric deposited on a $SiCl_4$ etched barrier layer, threshold voltage was -9.5 V, compared to -6.2 V for 10 nm SiN_x and -3.95 V for 5 nm SiN_x.

7 AlGaN/GaN-on-Si Heterostructures

In this chapter, process modules developed on AlGaN/GaN materials will be presented. This was a prerequisite work for developing InAlN/AlGaN/GaN-on-Si transistors, as it provided the basis for the design of the layer structures and validated the assumptions made before carrying on with the d-mode and e-mode dual barrier device work. Under this context, characterisation data from transistors fabricated on most commonly used AlGaN/GaN commercial materials will be depicted presented. Data extracted from low temperature annealed ohmic contacts will be shown. Evaluation of ohmic contacts on enhancement mode AlGaN/GaN materials using gated TLM structures will be also exhibited.

7.1 Transistors on AlGaN/GaN-on-Si materials

Prior to the development of InAlN/AlGaN/AlGaN based materials, HEMT devices were fabricated on 3 nm AlGaN/GaN-based materials and 20 nm AlGaN/GaN materials (Figure 7-1). Fabrication processing was partially carried out by Dr Gary Ternent, who also aided my fabrication training at the same time. The rationale behind this was to study the effect of a thin 3 nm AlGaN barrier layer on device characteristics in comparison to devices fabricated on the more standard 20 nm AlGaN/GaN heterostructure. The transistors were fabricated according to a mask layout design which sets the transistor gate to be overlapping the transistor drain and source. This particular structure (referred in this thesis as gate overlap structure) ensured that the transistor fabricated on the 3 nm AlGaN-based materials can turn on, as the thin barrier material structure was designed to be normally-off. A 30 nm thick SiO_2 dielectric deposited by PECVD at 300 °C, was used for both structures.

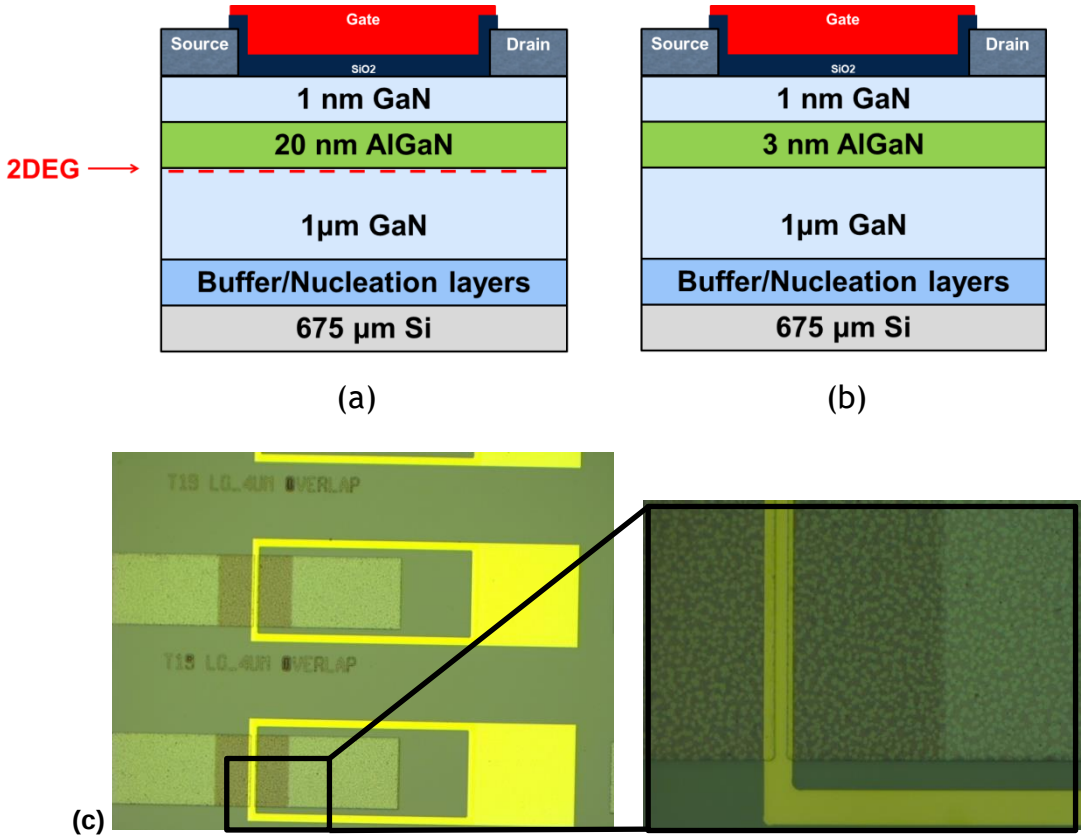
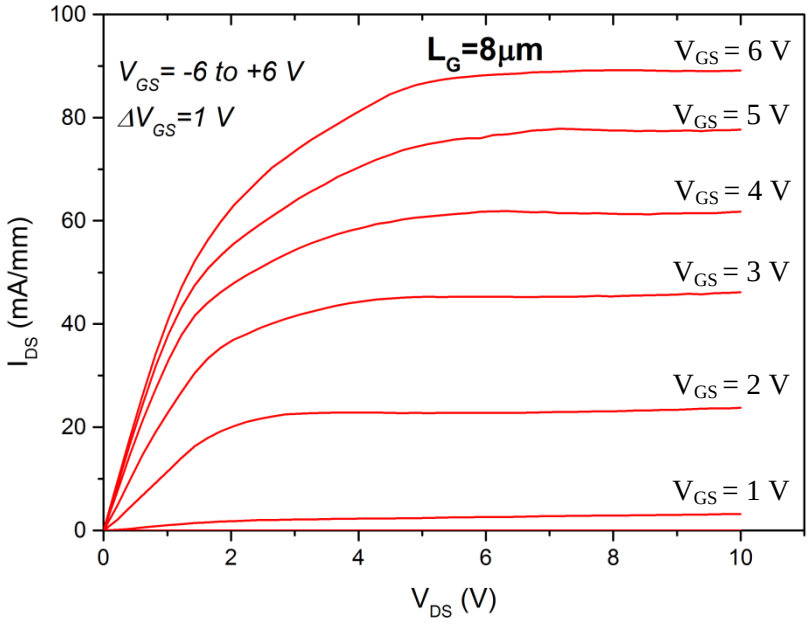
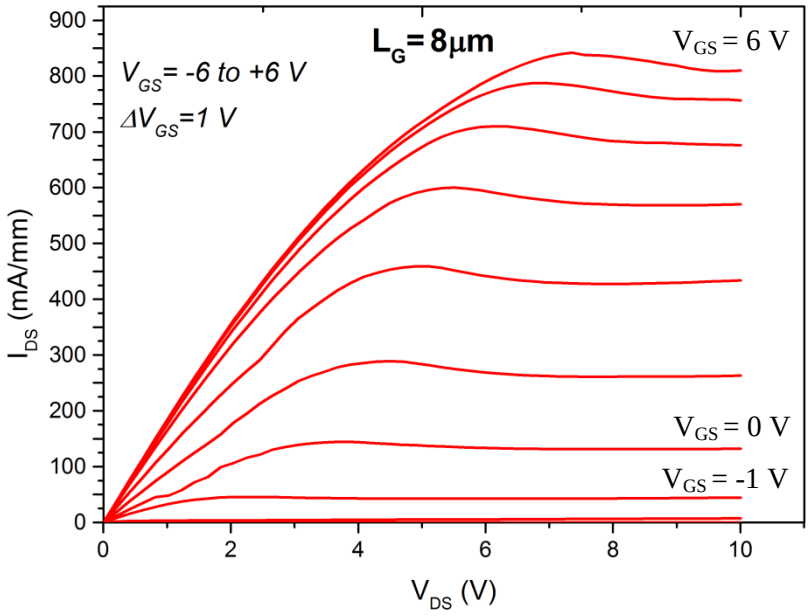


Figure 7-1: (a) Depletion mode transistor and 20 nm AlGaN/GaN-based growth structure. (b) Enhancement mode transistor and 3 nm AlGaN/GaN-based growth structure. (c) Gate wrap-around transistors showing gate overlapping the ohmic contacts.

The DC output measurements of these devices are illustrated in Figure 7-2. Transistors fabricated on the 20 nm AlGaN-based structure were shown to sustain higher currents. This was expected, as the stronger polarisation effect enabled by the thicker AlGaN increases the maximum channel 2DEG density. In contrast, this was much less of an issue for the short gate length devices fabricated on the dual barrier InAlN/AlGaN/GaN materials, such as the device structure shown in Figure 5-1, as the active regions strongly benefit by the strong polarisation induced 2DEG that InAlN generates.

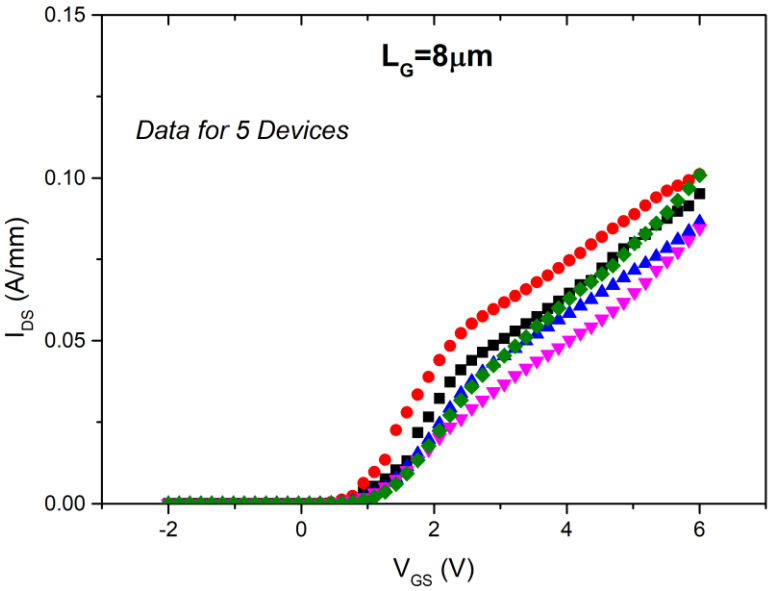


(a)

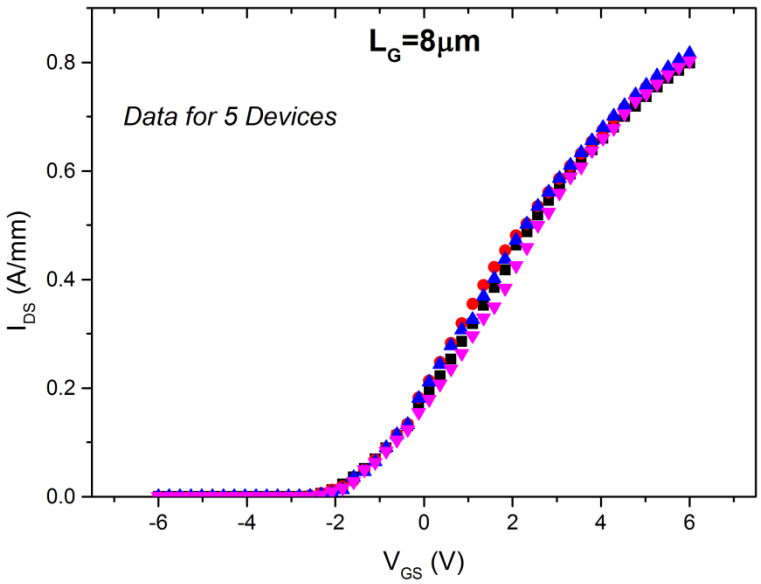


(b)

Figure 7-2: DC output measurements of depletion mode device with gate overlap topology on (a) 3 nm AlGaN/GaN and (b) 20 nm AlGaN/GaN wafer.

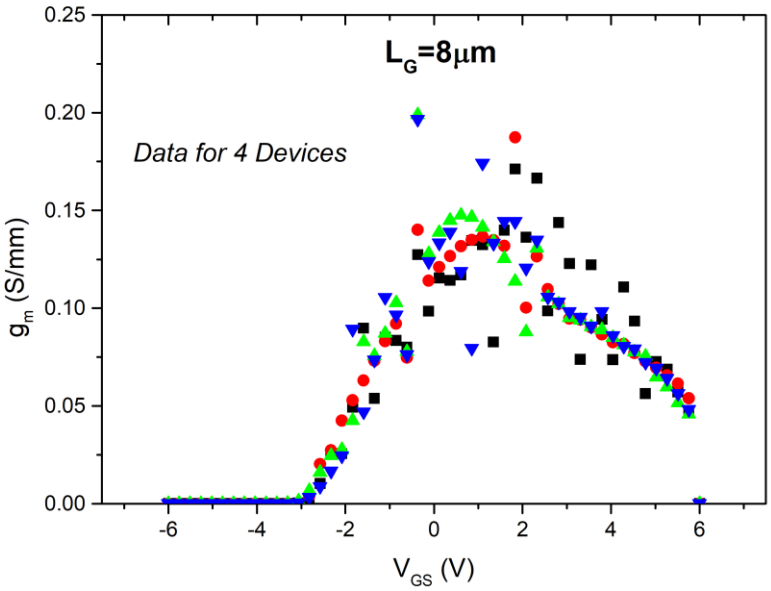


(a)

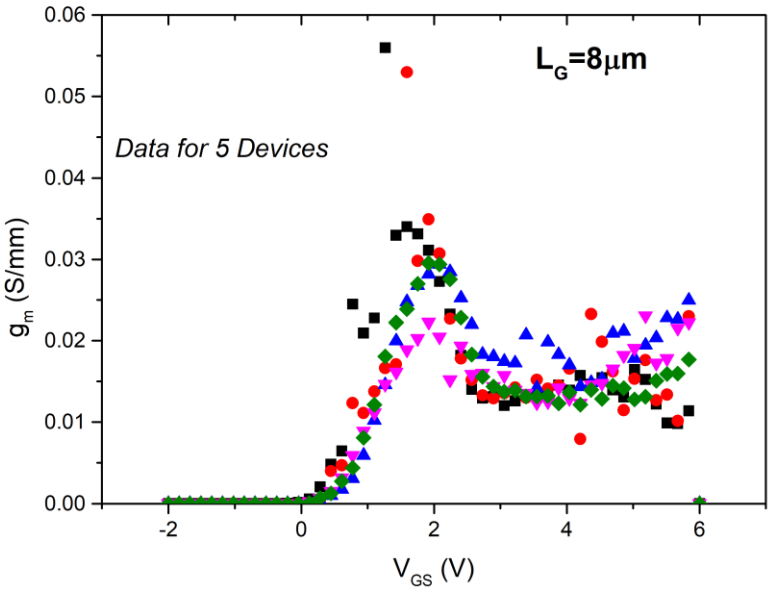


(b)

Figure 7-3: Gate transfer measurements for five depletion mode devices with gate overlap topology on (a) 3 nm AlGaN/GaN and (b) 20 nm AlGaN/GaN wafer. Drain-source voltage I_{DS} = 10 V.



(a)



(b)

Figure 7-4: Extrinsic transconductance measurements of transistors employing gate overlap topology, fabricated on (a) 3 nm AlGaN/GaN and (b) 20 nm AlGaN/GaN wafer. Drain-source voltage V_{DS} = 10 V.

As extracted by the gate transfer characteristic curves (Figure 7-3), threshold voltage V_{TH} ranged from ~ -3.5 to -2.9 V for the 20 nm AlGaN/GaN heterojunction and from ~ -0.2 to +0.3 V for the 3 nm AlGaN/GaN, indicating that fabrication of normally-off devices can be achieved through the use of thin AlGaN barrier layer. This was a prerequisite for the development of InAlN/3 nm

AlGaN/GaN materials presented in Chapter 5, because an etched InAlN layer under the gate stack would result in an enhancement mode device. The development of the enhancement mode devices on the dual barrier materials is presented in the Chapter 6 of this thesis.

Compared to the AlGaN/GaN depletion mode devices, the enhancement mode devices fabricated on the 3 nm AlGaN/GaN sample exhibited a greater deviation in performance with regards to their maximum drive current density. This may be related to thinner barrier materials being more difficult to grow, hence being more prone to relative barrier thickness deviation across a wafer/sample. Higher barrier thickness variation can result in higher variation in transistor performance. It may be also related to processing issues, e.g. thickness uniformity of the dielectric.

The relationship between extrinsic transconductance and gate voltage when drain-source voltage V_{DS} = 10 V is found in Figure 7-4. The use of a gate dielectric resulted in leakage currents well below 1 μA/mm levels for both gate-source and drain-source leakage paths (Figure 7-5). Off-state drain-source leakage currents were also kept below 1 μA/mm. Similarly to the observations for InAlN/AlGaN/GaN devices presented in Chapter 6, peak transconductance is higher for the devices fabricated on thinner barrier materials, with all other processing and device structures being identical. This is due to the gate contact coming in closer proximity to the channel and the subsequent increased gate control. Lowest on-resistance measured was 4.67 Ωmm for an AlGaN/GaN depletion mode device with drain-source separation of 4 μm. This was moderately higher than the lowest on-resistance measured for InAlN/AlGaN/GaN devices (4.06 Ωmm), which had a 10 μm total drain-source separation.

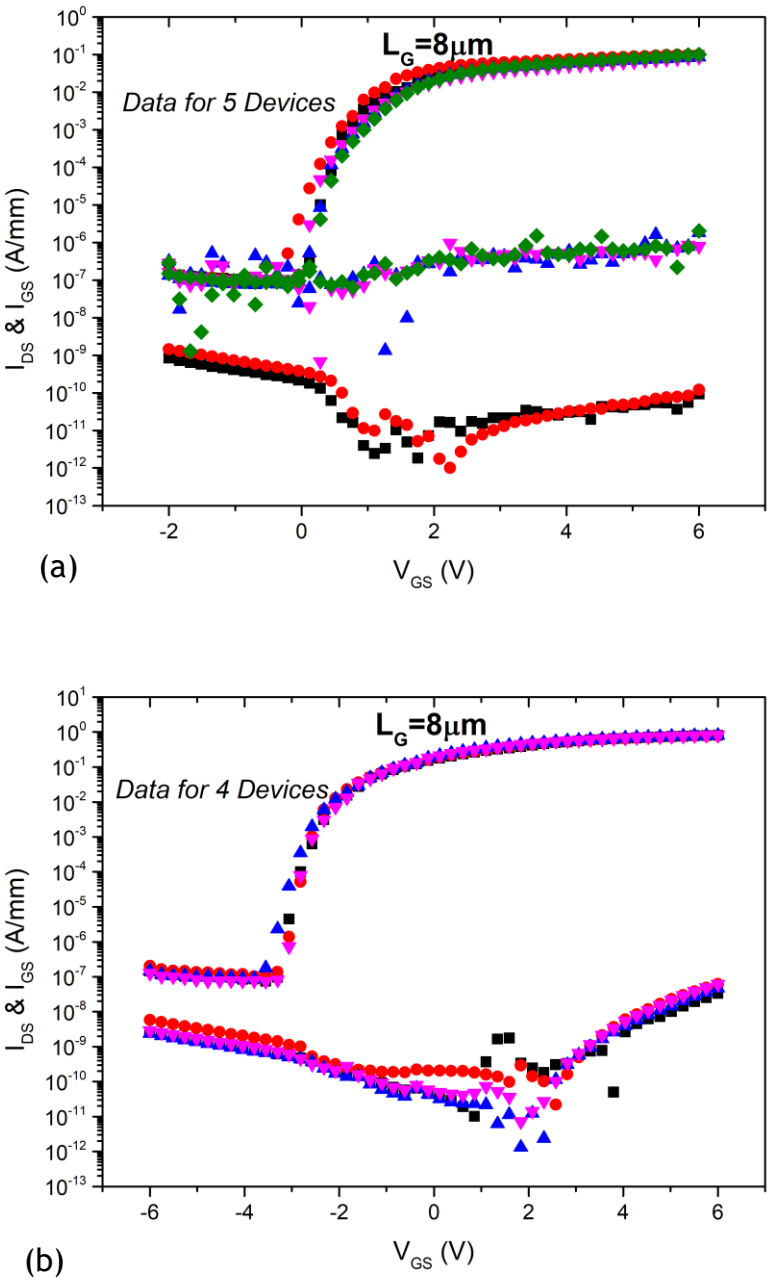


Figure 7-5: Pinch-off leakage measurements of (a) 3 nm AlGaN/GaN and (b) 20 nm AlGaN/GaN transistors. Drain-source voltage V_{DS} = 10 V.

7.2 Dielectrics on Enhancement Mode Materials

It is widely reported that dielectric films can significantly impact the transport properties of group III-nitride based heterostructures ([135], [136]). A common mechanism of this influence is through the introduction of surface charges which can heavily influence device threshold voltage and leakage currents. Thin AlGaN barrier (~3 nm) GaN materials are intrinsically non-conductive, and as such, passivation could potentially amend their insulating behaviour.

For this study, Van der Pauw structures were fabricated on enhancement mode materials, grown by IQE (Figure 7-6). Subsequently, SiN_x dielectrics were deposited by PECVD on the semiconductor surface. From the top, the epitaxial layers grown on a 675 µm Si layer consisted of a 1 nm GaN capping layer, a 3nm AlGaN layer, a 1 µm GaN channel layer, and transition/buffer layers.

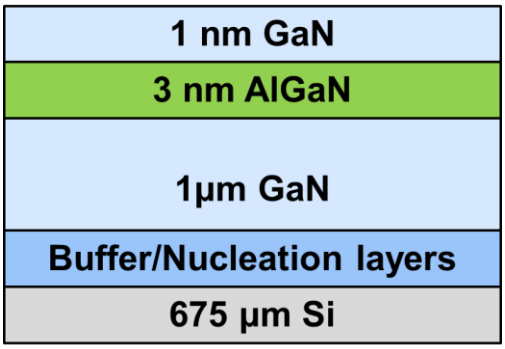


Figure 7-6: Enhancement mode 3 nm AlGaN/GaN-based layer structure (IQE).

Fabrication process steps included a Ti/Al/Ni/Au metal stack of 30/180/40/180 nm thicknesses which was deposited by e-beam evaporation prior to rapid thermal annealing for 30 seconds at 770 °C in N_2 environment to form the ohmic contacts. The samples were subsequently isolated by a shallow ~40 nm mesa etch process. The complete fabrication process is described in Appendix B. An optical image of a fabricated Van der Pauw structure is shown in Figure 7-7. The vertical distance (height) between points 3-4 (i.e. combined thickness of dielectric and mesa) was measured with the Dektak surface profiler system to be 65 nm, 75 nm and 93 nm for the 15 nm, 30 nm and 50 nm SiN_x PECVD passivated samples respectively.

Hall measurements, summarised in Table 7-1, were taken from each sample at room temperature. As expected, for the reference non-passivated sample, conductivity between probes placed on the metal pads was non-detectable (sheet resistance greater than 107 Ω/sq), hence confirming that the materials possess normally-off properties due to the barrier layer being of sub-critical thickness.

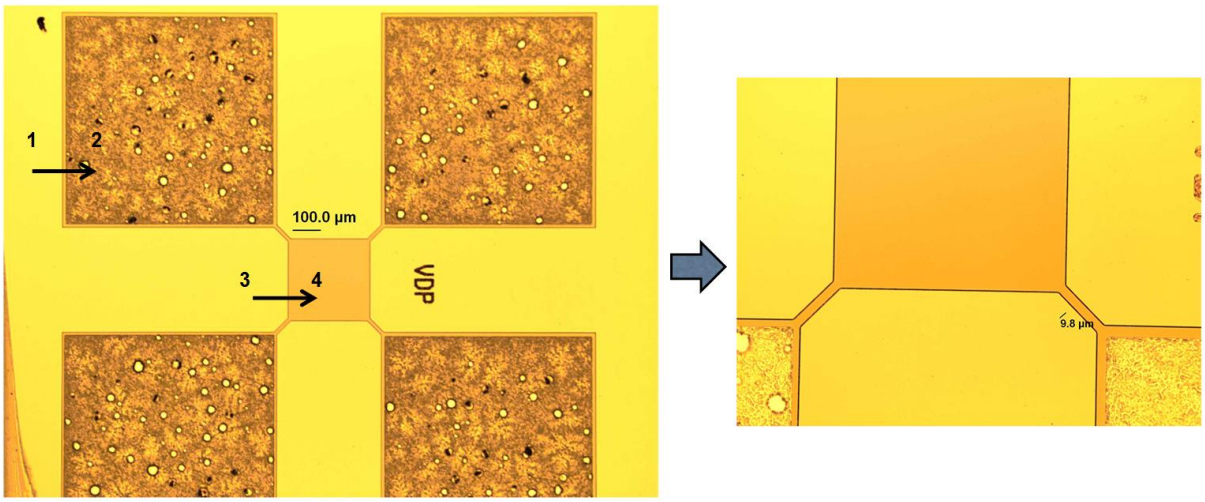


Figure 7-7: Optical microscope images of fabricated Van der Pauw structures (left), zoomed mesa area (right).

Regarding the passivated samples, each SiN_x dielectric deposited on the semiconductor surface led to 2DEG charge enhancement, essentially converting the normally-off material to normally-on. There was no correlation between dielectric thickness and change in transport characteristics, only the notion that PECVD deposited SiN_x enhanced the 2DEG carrier density in all cases compared to a non-passivated reference sample. This indicates the presence of positive charges in the SiN_x film [137].

Table 7-1: Effect of PECVD SiN_x dielectrics on normally-off material transport properties.

	PECVD SiN_x thickness (nm)			
Metric	0	15	30	50
Sheet resistance R_{sh} (kΩ/sq)	$>10^7$	62.2	39.1	100.2
Hall mobility μ_H (cm^2/Vs)	-	105	165	87.7
Hall electron concentration n_H (cm^{-2})	-	$9.5*10^{12}$	10^{12}	$7.1*10^{11}$

This observation led to the use of fluorine doped dielectrics for device fabrication of recess etched InAlN/AlGaN/GaN-based transistors as mentioned previously, as a means of ensuring a positive threshold is achieved, due to the negatively charged fluorine ions present in these dielectric films.

7.3 Low Temperature Annealed Ohmic contacts

As previously observed, in order to obtain the optimum contact resistance using a Ti/Al/Ni/Au stack the contacts need to be annealed at around 770 – 800 °C. Gate dielectrics and passivation layers are sensitive to high temperatures and the optimum forming gas annealing conditions after dielectric depositions are at much lower temperatures (for example 430 °C forming gas anneal for Al_2O_3). This limits the process flow possibilities, by allowing only a gate last approach when fabricating transistors.

In contrast, a gate first approach can significantly improve yield and threshold stability, as the semiconductor surface gets encapsulated immediately after wafer growth. If charges are trapped at the semiconductor surface states, this may result in virtual gate formation, which causes partial or full depletion of the 2DEG and will degrade drain current [55]. This effect can be suppressed through the use of passivation layers, such as Si_3N_4 [56], surface cleaning treatments [57] and the incorporation of field plates [58], [59]. A gate first process flow can help reducing surface exposure to process related chemicals (e.g. protect from contamination during high temperature RTA). It may also permit achieving shorter gate to source distances using self-alignment, thus lowering the transistor on-resistance [138].

After conducting a literature review on the positive influence of Si-based dopants on ohmic contact performance, its incorporation in ohmic contact stacks in the form of SiH_4 was investigated. Subsequently, characterisation of TLM structures was performed on single barrier 27 nm AlGaN/GaN samples. These structures were fabricated by Dr Xu Li. The fabrication process flow along with the TLM characterisation results are summarised in Table 7-2.

The processes involved made use of recess etching of the ohmic contact area via $SiCl_4$ RIE, in order to reduce the effective distance between the contacts and 2DEG and increase the carrier tunnelling probability to the channel. Also, Molybdenum based contacts were employed, as they can be annealed at lower temperatures compared to Ti based contacts and possess a high melting point, low work function of ~4.6 eV and low Au solubility [139]. Annealing at temperatures lower than the melting point of Al (~ 660 °C) may reduce the risk

of lateral overflow of the contact metals [140]. Moreover, silane (SiH_4) ICP pre-treatments were involved prior to depositing the metal contacts, as Si had been widely used as an n-type dopant for group III-V semiconductors.

As seen in the table, contact resistance values R_c of below 0.8 Ω/mm were extracted following three process flows, which were based on RIE contact area recess, SiH_4 pre-treatments and two different metal contact stacks. Pre-treating with SiH_4 was crucial for lowering the contact resistance of the Mo/Al/Mo/Al/Ti/Pd metal stack. A SiH_4 pre-treatment of 3 seconds resulted in the lowest contact resistance obtained via the Mo/Al/Mo/Au contacts. The extracted sheet resistance was much smaller for conditions #3 and #5 compared to the other conditions. This is due to sourcing the substrate materials from two different wafers even though they were nominally identical in their structures.

Table 7-2: Contact screening conditions and TLM measurements.

	Conditions					TLM	
ID	**Mesa (nm)**	**Ohmic recess (nm)**	**SiH_4 (s)**	**Metallisation (nm)**	**RTA 60 s (°C)**	**R_c (Ω mm)**	**R_{sh} (Ω/sq)**
#1	500	35	3	Mo/Al/Mo/Au 10/40/20/30	550	0.793	875.1
#2	500	35	2	Mo/Al/Mo/Au 10/40/20/30	550	0.8	886.9
#3	500	35	4	Mo/Al/Mo/Au 10/40/20/30	550	1.328	365.9
#4	500	35	4	Mo/Al/Mo/Al/Ti/Pd 10/40/20/20/40/50	650	0.73	965.3
#5	500	35	0	Mo/Al/Mo/Al/Ti 10/40/20/20/50	650	2.38	374.6

Obtaining low contact resistance values through the use of ohmic contact stacks that are annealed at low temperatures can provide greater process flexibility whilst achieving low transistor on-resistance values. Process flows involving contact recess etching, SiH_4 pre-treatment and molybdenum based contacts can play a significant role in in realising this.

7.4 Ohmic Contacts on Enhancement Mode Materials

Ohmic contact evaluation has been generally well studied when it applies to depletion mode materials, however there are no reports on contact evaluation performed directly on normally-off materials. TLM structures cannot be used for contact evaluation in this case, as there is no current flowing between two TLM pads when low electric fields are applied. As such, ohmic contacts have to be evaluated on normally-on materials and then then the ohmic contact fabrication process is transferred to a different substrate.

In this work, linear gated TLM structures were fabricated on sub-critical barrier thickness 3 nm AlGaN/GaN materials for ohmic contact evaluation. Similar to linear TLM structures, the contacts are isolated via a mesa etch and are separated by different distances, which are used to extract the ohmic contact metrics. However they are reliant on a gate contact to turn the channel on. The gate overlaps the drain and source pads to enable conduction along the channel semiconductor region. A gate dielectric is used in order to prevent a short circuit between the gate and ohmic contacts. The gate dielectric is etched above the contact region and a via is opened, which allows contact access for probing.

First tested structures were circular gated TLMs, which incorporated a 20 nm PECVD SiO_2 gate dielectric and were fabricated on 3 nm AlGaN/GaN materials. Resistance measurements for different ohmic contact separations were measured and TLM evaluation was performed.

At gate voltages lower than the HEMT structure threshold voltage, as there is no intrinsic channel underneath the gate due to the sub-critical thickness of the barrier layer, current flow is essentially low field leakage current flowing between the ohmic pads. The currents detected at these bias conditions are noisy and are not adequate to extract accurate TLM metrics.

Some raw data extracted for gate-source voltage V_{GS} = -2V are presented in Table 7-3. As shown, no meaningful data can be extracted in this region. When the test structures operate in the pinch-off region the sheet resistance is very high compared to the contact resistance and it dominates the overall resistance measured. Also, resistance readings do not accurately scale with TLM pad

distances as they may have been significantly dependent on localised defects related leakage paths rather than conduction in the channel.

Table 7-3: Resistance values measured for gate-source voltage V_{GS} = -2V.

Gap (μm)	Resistance (MΩ)
4	7.2
8	1.04
12	0.46
16	1.07
20	0.73
24	0.73
32	0.05
40	0.42

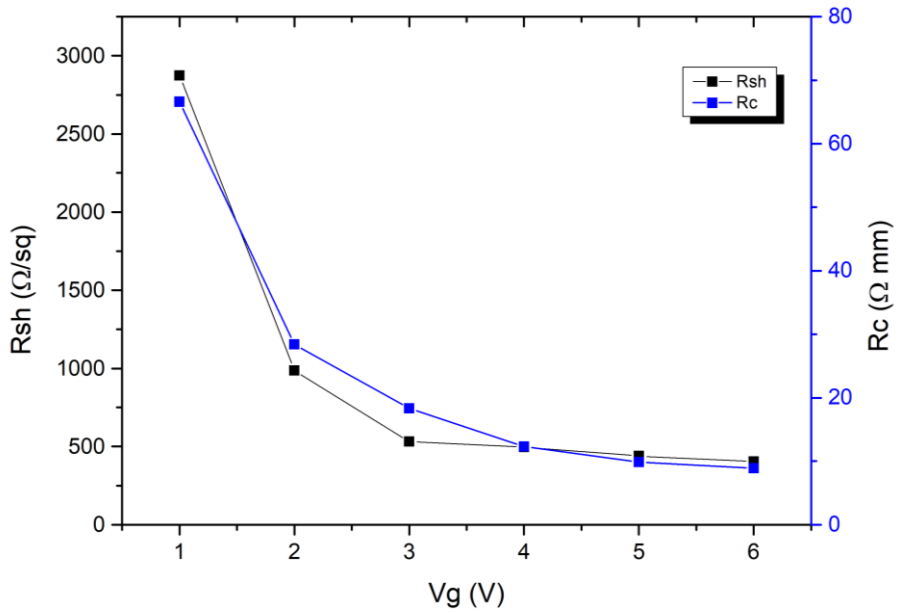


Figure 7-8: Variation in sheet and contact resistance for different gate voltage biases. Circular gated TLM structures, fabricated on 3 nm AlGaN/GaN materials, were tested at V_{DS} = 100 mV. Gate dielectric was 20 nm PECVD SiO_2.

With increased gate voltage, sheet resistance reduces and low field current can flow between the ohmic contacts. A plot depicting the contact and sheet resistance values extracted for varying gate voltages is found in Figure 7-8.

For V_{GS} = 1 V, which is typical for threshold voltage of these HEMT structures, there is some conduction but not at high enough levels to turn the channel fully on. This is reflected by the sheet resistance R_{sh} ~ 2873 Ω/sq extracted by TLM. Under these conditions a very high contact resistance is extracted R_c ~ 66 Ωmm.

As gate bias increased to V_{GS} = 2 V, the 2DEG is populated by an increased number of electrons, and a three-fold reduction in sheet resistance was observed (R_{sh} ~ 987 Ω/sq). Contact resistance in these bias conditions reduced to R_c ~ 28 Ωmm.

Further increase in gate voltage resulted in decreased sheet resistance, though R_{sh} reduction was much smaller than what was observed for lower gate biases. The same trend was observed for the contact resistance values extracted by TLM, with contact resistance values dropping by a progressively smaller factor. When the channel is fully opened, the sheet resistance saturates and contact resistance approaches a minimum value of 8.9 Ωmm.

Another fabricated sample was tested to verify these results. Again, a sub-critical barrier thickness HEMT structure with a 3 nm AlGaN/GaN heterojunction was used. A 30 nm SiO_2 dielectric, deposited by PECVD, was incorporate in the gate stack. Linear gated TLM structures of 200 µm gate width were tested at drain-source voltage V_{DS} = 60 mV. The TLM characterisation results obtained from these structures are presented in Figure 7-9.

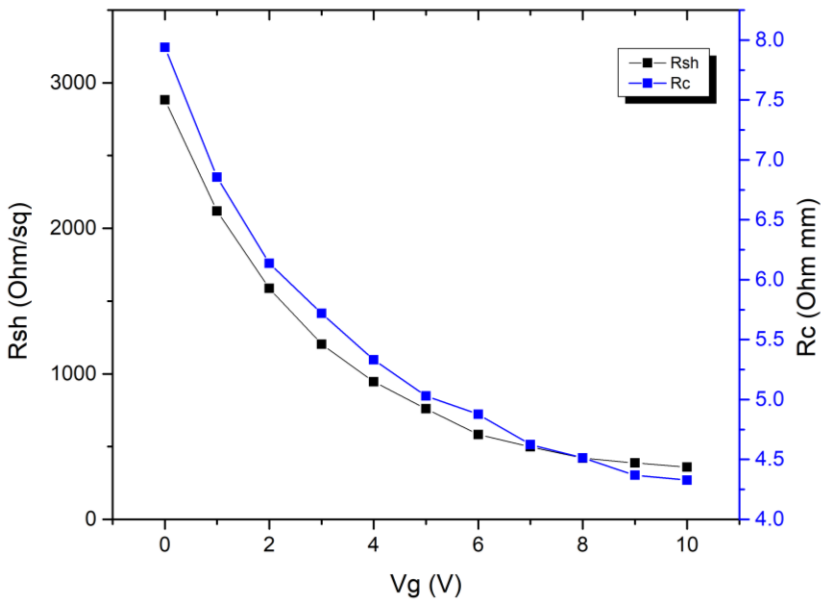
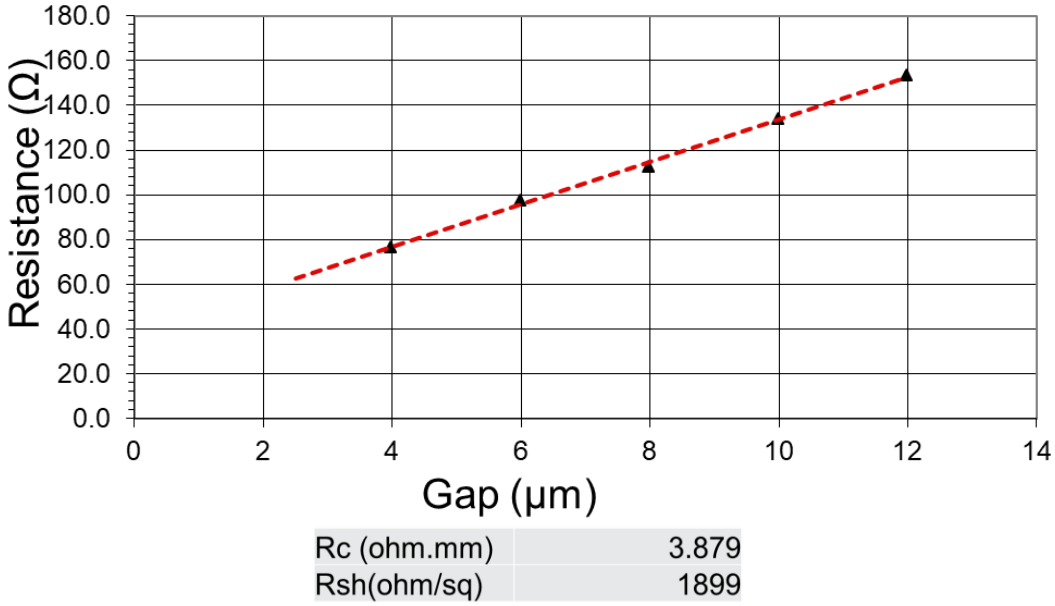
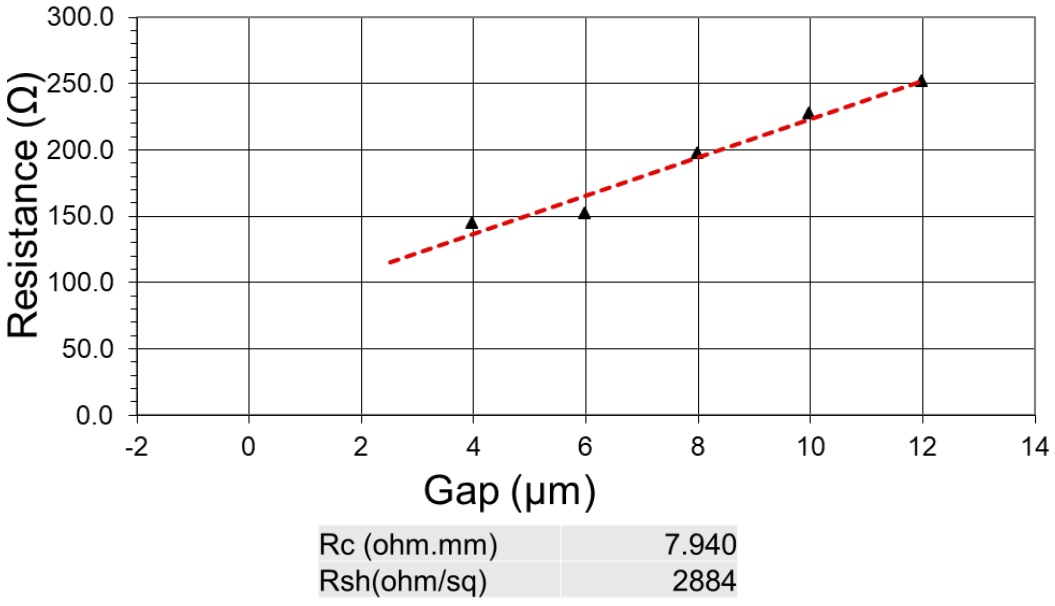


Figure 7-9: Relationship between sheet and contact resistance when different gate voltage is applied and V_{DS} = 60 mV. Linear gated TLM structures of 200 µm gate width were tested. Material layer structures were based on 3 nm AlGaN/GaN and gate dielectric was 30 nm PECVD SiO_2.

As depicted, the gate bias dependent TLM measurements exhibited a similar trend to that observed before. With increased gate bias, the material sheet resistance becomes smaller. Also a reduction in contact resistance is prevalent in this case too. Both metrics approach a fixed value. For gate-source voltage V_{GS} = 10 V, sheet resistance R_{sh} ~ 358 Ω/sq and contact resistance R_c ~ 4.32 Ω mm were extracted.



(a)



(b)

Figure 7-10: TLM measurements if (a) gate is floating, (b) at 0 V gate voltage.

The same TLM structures were tested with the gate floating. The comparison in TLM metrics when the gate is biased at 0 V and when the gate is floating is seen

in Figure 7-10. Gate potential was found to influence the measurements, by significantly modifying the sheet resistance and contact resistance metrics.

Contact evaluation on normally on materials via gated TLM measurements was also carried out. The gate dielectric was 20 nm SiO_2 deposited by PECVD. A comparison between the extracted gated TLM measurements for 20 nm AlGaN/GaN-based materials is shown in Figure 7-11. The main difference compared to those obtained from enhancement mode 3 nm AlGaN/GaN-based materials was that TLM extraction was valid for negative gate-source voltages. For V_{GS} = 6 V, sheet resistance R_{sh} ~ 411 Ω/sq and contact resistance R_c ~ 1.0 Ωmm were obtained. Similarly to the observations for enhancement mode materials, contact resistance and sheet resistance extracted from the gated TLM structures both lower in value and saturate at larger gate bias conditions.

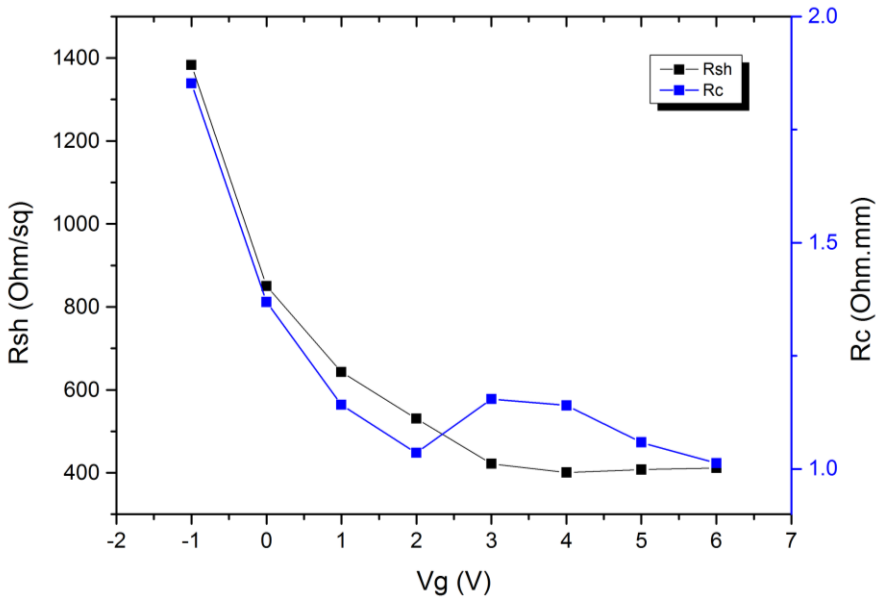


Figure 7-11: Variation in sheet and contact resistance for different gate voltage biases. Linear gated TLM structures, fabricated on 20 nm AlGaN/GaN materials, were measured at V_{DS} = 100 mV. Gate dielectric was 30 nm SiO_2 and was deposited via PECVD.

In this section, ohmic contact testing conditions via gated TLM measurements performed on enhancement mode 3 nm AlGaN/GaN-based materials were evaluated. In order to undertake characterisation of Ohmic contact formation to normally-off materials, a gate voltage more positive than the threshold voltage ought to be chosen. As with ungated TLMs, low field V_{DS}, such as 50 mV, need to

be applied to extract the TLM characteristics, in order to ensure ohmic behaviour.

Selecting different gate voltages can have significant influence on the contact resistance values obtained. Both contact and sheet resistance decrease and approach a saturated value as gate bias increases. The gate overlap structure may have influenced contact resistance by altering the fringing electric field near the ohmic contact edges, where current crowding occurs [141]. This can also modify the constriction (spreading) of contact resistance, hereby altering the contact transfer length. It is therefore an inherent disadvantage of using gated TLM structures of this specific type, which rely on a gate overlapping the drain and source contacts. However, this remains the sole method of evaluating contacts deposited directly on normally-off materials.

7.5 Conclusion

In this chapter, fabrication of enhancement mode and depletion mode AlGaN/GaN-on-Si devices was demonstrated. The processes were etch-free and relied on different AlGaN layer thickness to control the threshold voltage. Dielectric films deposited on normally off 3 nm AlGaN/GaN materials were shown to increase carrier density and decrease sheet resistance, as measured by Van der Pauw structures.

Ohmic contact evaluation work was performed in order to enable low contact resistance and low annealing temperatures which can in turn enable gate-first process flows to be incorporated. Another ohmic contact optimisation experiment presented in this chapter was the development of electrical measurement conditions on normally-off AlGaN/GaN materials. For consistency, both linear and circular gated TLM structures were measured and different gate dielectrics were also tested. In all cases, contact evaluation work cannot be successfully carried out when the channel is pinched-off. With a conducting channel, contact resistance decreases towards a saturated value as gate bias increases.

8 Conclusion and Outlook

8.1 Conclusion

Owing to its favourable material properties, GaN-based technology has shown great potential to complement silicon as a leading semiconductor for power electronics. This prospect has encouraged research and development activities within the industry and the academic world and the reported work in this thesis is one of the many contributions to this goal. Within this thesis, fabrication process modules that led to the development of InAlN/AlGaN/GaN-on-Si based HEMT were presented. The wafer materials were designed with compatibility with these process modules in mind. The fabrication steps which are related to epitaxial layer processing, e.g. substrate etching, dielectric deposition, ohmic, gate contact development were demonstrated on Si-based substrates. An extension of these techniques to other substrate materials would require new cycles of process development which may be limited or aided by the substrates, e.g. by enabling more efficient heat extraction when diamond substrates are used, or having to take into account the absence of buffer structures in the case of sapphire.

For this work, the InAlN/AlGaN/GaN-on-Si material carrier transport properties were characterised and it was found that ICP SiN_x passivation films increase their channel conductivity. This property was reversed when SiN_x bilayers of different stress were incorporated. The performance of InAlN/AlGaN/GaN HEMT was compared to AlGaN/GaN devices. The depletion mode InAlN/AlGaN/GaN devices benefit from the inclusion of an InAlN layer, lattice matched to GaN, which induces high GaN 2DEG densities via spontaneous polarisation. Regarding the enhancement mode InAlN/AlGaN/GaN transistors, the semiconductor underneath the gate utilises an ultra-thin AlGaN barrier layer, as means for the device threshold voltage to be shifted positively. The presence of a barrier layer along the HEMT channel during the transistor on state ensures high electron mobility 2DEG conduction. A thin barrier layer also correlates with higher transconductance metrics.

Fabrication processing of depletion mode devices is completely non-invasive with regards to the semiconductor materials. The enhancement mode devices

rely on barrier removal processes for operation. Several process modules were developed for InAlN removal. A gate recess etch via an ethylenediamine based solution was shown to be self-limited and highly selective to GaN, which can significantly lower the fabrication degree of difficulty. Demonstrating a threshold voltage of as high as +4.5 V, as shown in Chapter 6, is highly desirable for transistor development. The devices demonstrated in this work can be incorporated in discrete enhancement mode and depletion mode modules and could also in future be integrated to realise an all-GaN cascode configuration, as shown in the following section.

This thesis also included the first data of its kind on ohmic contact characterisation fabricated directly on GaN-based enhancement mode materials. It has identified limitations on using gated TLM structures to carry out contact evaluation, as contact resistance extraction can be modified due to the gate potential.

8.2 Integrated Cascode

A commonly used topology for commercial GaN device packages is based on the cascode topology. In the cascode configuration a low voltage e-mode FET can control the operation of a high voltage d-mode FET. Utilising an all GaN cascode architecture compared to a Si FET driver transistor of similar voltage ratings in converter applications can result in lower turn off losses, drive losses and conduction losses, resulting in higher energy efficiency [20]. A circuit diagram of this topology is shown in Figure 8-1.

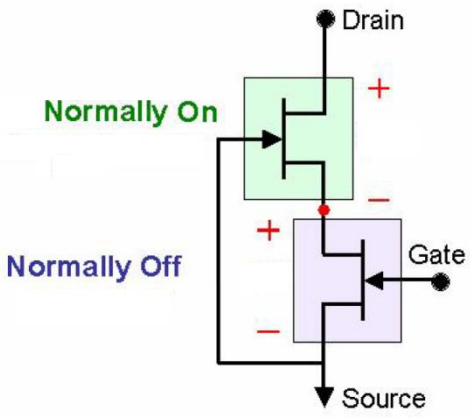


Figure 8-1: Cascode circuit (similar to Baliga-Pair configuration [118]).

The cascode configuration comprises of two transistors, so that $V_{GS,d}$ of the d-mode transistor is the negative of the $V_{DS,e}$ of the e-mode device. This configuration works as follows; the d-mode device is on when its gate to source voltage $V_{GS,d}$ is greater than its threshold voltage $V_{th,d}$. The source of the normally on and the drain of the normally off device are on the same node, hence their voltage is the same ($V_{GS,d} = V_{SD,e}$). Also, the source of the normally off device is connected to ground, so $V_{S,e} = 0\,\mathrm{V}$. This means that the d-mode device is on when its source voltage $V_{S,d} < -V_{th,d}$. As mentioned earlier, because the source of the d-mode device and the gate of the e-mode device are connected, the condition to turn on the normally off transistor becomes $V_{D,e} < -V_{th,d}$.

The e-mode device drain voltage $V_{D,e}$ can become less than $-V_{th,d}$ if a positive gate voltage greater than its threshold is applied to turn the transistor on, thus if $V_{GS,e} > V_{th,e}$.

In most current applications, the cascode topology is developed as two chips, a GaN normally-on HEMT and a Si based normally-off FET that are interconnected and co-packaged. The inclusion of the Si FET as the e-mode device is due to the robustness of the long-time established e-mode Si technology. Also, it offers the possibility to make use of a standard Si gate driver circuit, hence offering increased ease of usage.

More recently, single-chip all-GaN arrangements have also been realised, with a GaN HEMT replacing the Si FET to increase power efficiency [142]. This report was based on conventional AlGaN/GaN materials.

The InAlN/ultrathin AlGaN/GaN based material layer structures presented in this thesis can host two transistors in a cascode topology on the same chip (Figure 8-2). Compared to utilising AlGaN/GaN materials, the proposed materials can provide a theoretical advantage in power density, due to the high induced spontaneous polarisation charges via InAlN and are compatible with the ethylenediamine wet etch technique described in Chapter 6.

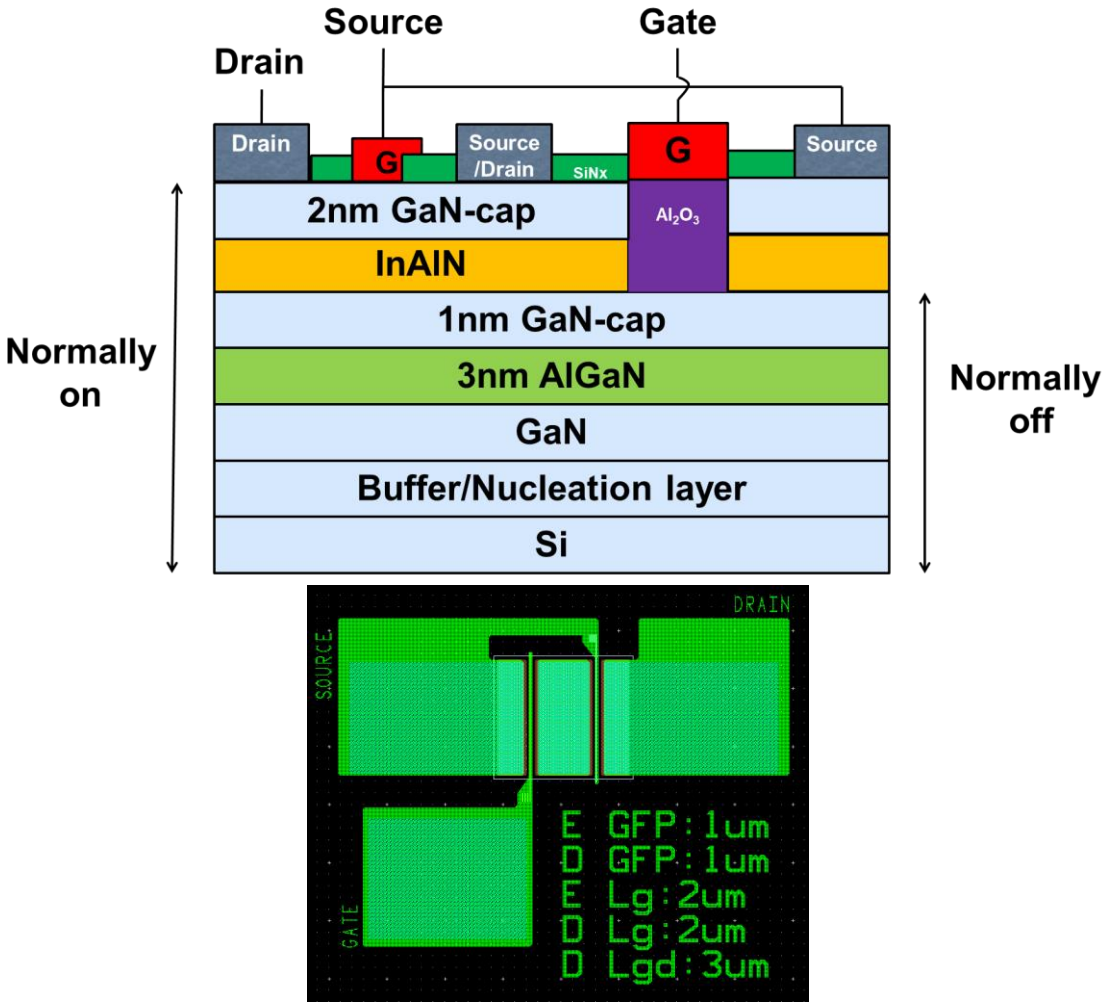


Figure 8-2: Cascode topology layer structure and mask design.

8.3 Gold-free Ohmic Contacts

Lowest specific contact resistance reported incorporate gold within the ohmic contact stack and low ohmic contact resistance was reported in this thesis. Although gold was only deposited as the metal furthest from the semiconductor material, complete silicon compatibility may require total absence of gold within the process line. For this reason, additional ohmic contact stacks can be developed to exclude gold from the processes. The low annealing temperature ohmic contact stacks presented in this thesis can be transferred to InAlN/AlGaN/GaN-on-Si substrates with the ultimate goal being the elimination of Au from the process. This can also allow for a gate first process development, which is compatible with InAlN/AlGaN/GaN-on-Si wafers.

Appendices

A. GaN Epitaxial Wafer Market Share

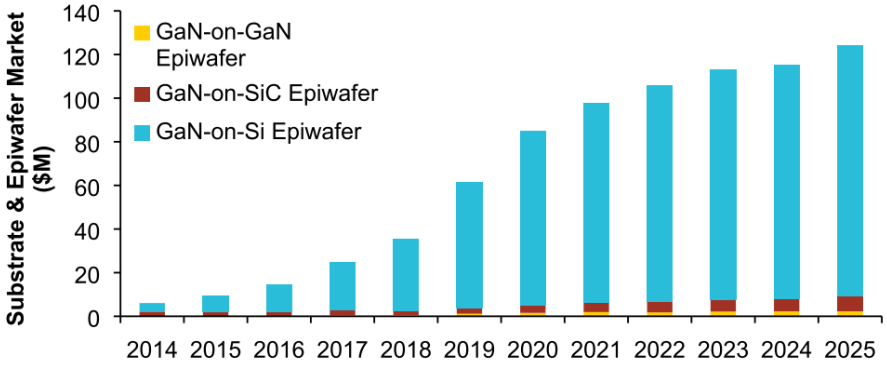


Figure A-1: Breakdown of GaN epitaxial wafer market share, reported in 2016 [62].

B. Van der Pauw Structure Fabrication Process

CLEAN	
1.1 Sample cleaning	
1.1A	Immerse sample in acetone
1.1B	Ultrasonic 5 mins
1.1C	Rinse in IPA
1.1D	Blow dry N_2 gun
OHMIC LEVEL	
2.1 Photolithography	
2.1A	Spin LOR 6000 rpm 30 seconds
2.1B	Bake hotplate 2 minutes at 150 °C
2.1C	Spin S1818 4000rpm 30 seconds
2.1D	Bake hotplate 3 minutes at 115 °C
2.1E	MA6 exposure 6 seconds in Hard contact
2.1F	Development using MF319 2 minutes 30 seconds
2.1G	Rinse RO water
2.1H	Blow dry N_2
2.1I	Visual inspection and take images
2.2 Deposit metal	
2.2A	RIE 3 minutes 80+ O_2 10 W, 10 sccm, 50 mTorr
2.2B	De-Ox HCl:RO 1:4 60 seconds
2.2C	Rinse RO water
2.2D	Blow Dry N_2
2.2E	Evaporate Ti/Al/Ni/Au 30/180/40/100
2.2F	Lift off in 1165 at 50 °C, sample vertical in beaker for at least 3 hours
2.2G	Rinse well in RO water

2.2H	Blow dry
2.2I	Visual inspection and take images
2.2J	Dektak
2.2K	Anneal 770 °C 30 seconds in N_2
2.2L	Visual inspection and take images
DIELECTRIC DEPOSITION	
3.1 Deposit dielectric	
3.1A	SiN_x PECVD and ICP CVD 15, 30, 50 nm deposition
MESA ETCH	
4.1 Photolithography	
4.1A	Spin S1818 4000rpm 30secs
4.1B	Bake hotplate 3mins at 115 °C
4.1C	MA6 exposure 6 seconds in Vacuum contact
4.1D	Development using Microposit Developer 1:1 H_2O 75 secs
4.1E	Rinse RO water
4.1F	Blow dry
4.1G	Visual inspection and take images
4.2 Mesa etch	
4.2A	Mesa etching Cl_2/BCl_3-based inductively coupled plasma reactive ion etching
4.2B	Ash 5 min 60 W Gala Asher or in dry etch
4.2C	Resist Strip in 1165 at 50 °C, sample vertical in beaker at least 3 hours
4.2D	Rinse RO water
4.2E	Blow dry
4.2F	Visual inspection and take images
4.2G	Dektak

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